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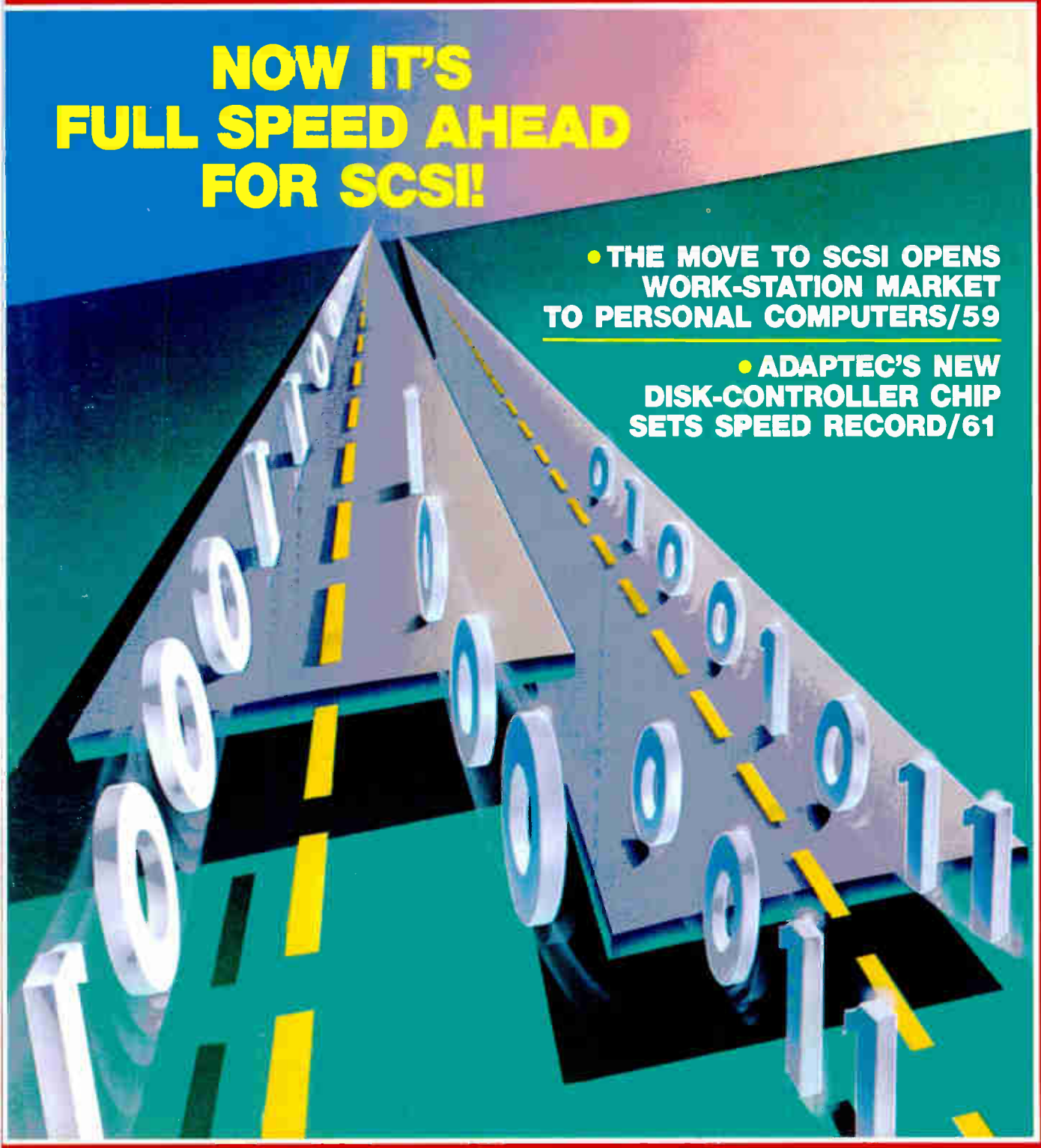

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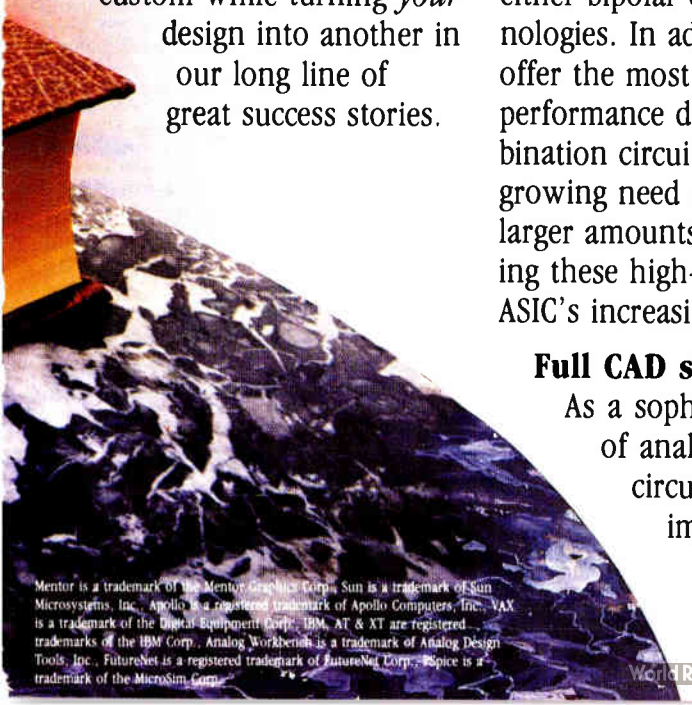

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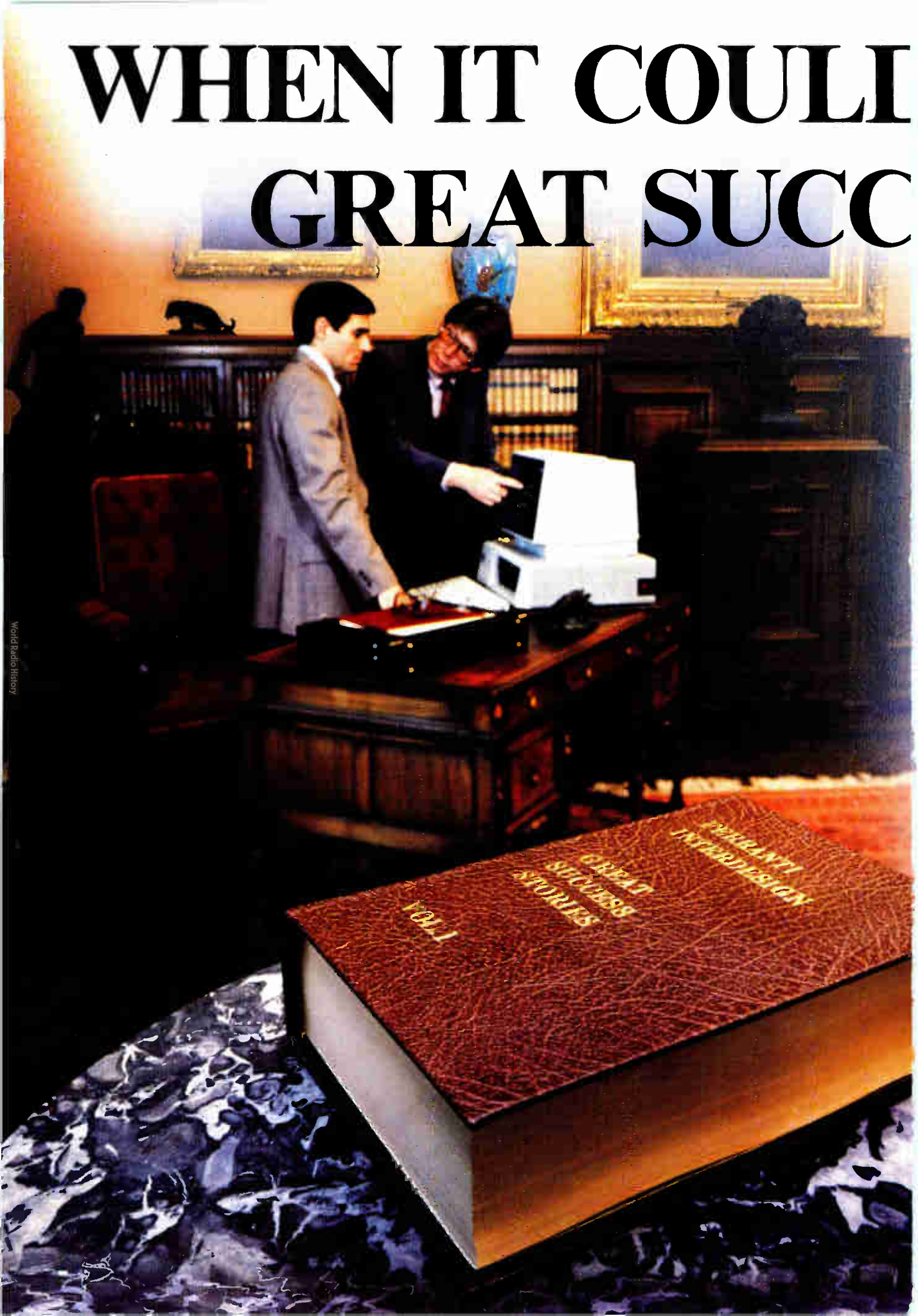

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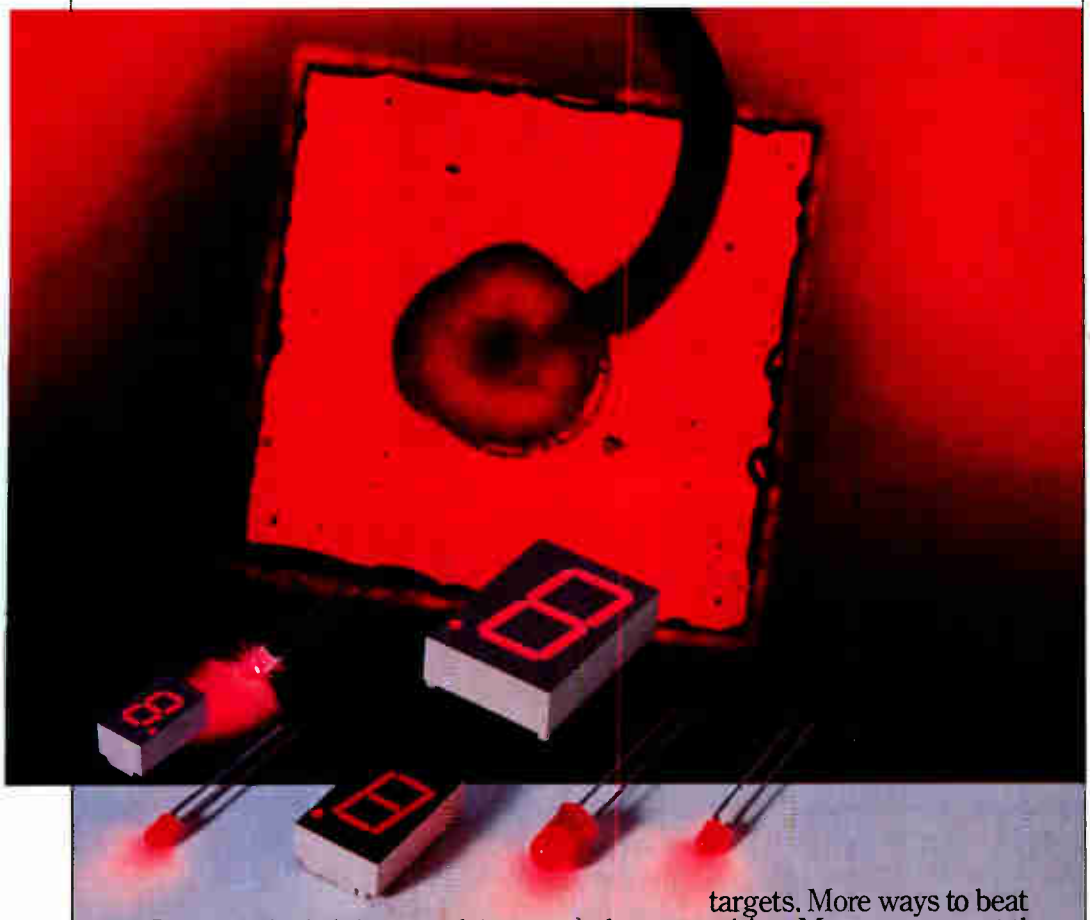

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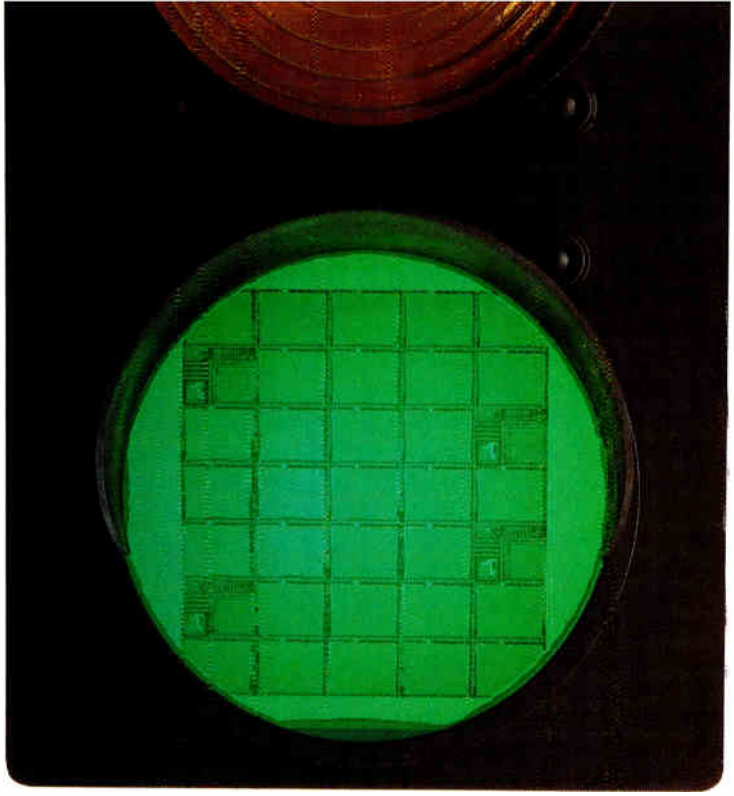

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Whether they're Pulitzer Prize-winning veterans or tyros fresh out of school, most journalists worry about whether anyone out there is reading their stories. For that reason, letters to the editor, even if they're not complimentary, are an important element of the feedback journalists get. *Electronics* is no exception: we love to get letters, even if they are of the "dear sir you cur" stripe.

O'NEILL: She loves to get those letters from our readers.

"Letters are music to our ears," says Kathy O'Neill, who sees to it that the communications selected for publication get into print. That's a job that is anything but dull. "I like to read a lot," says Kathy, who has a bachelor's degree in English, "so I'm not easily impressed. But some of the letters I see are truly impressive for their command of the facts, as well as for their eloquence."

Letters to the editor generally make up one of the best-read sections of the issue, and the best-read letters are those that press new or unusual points of view. "In fact," says Kathy, "like most publications—except perhaps major national newspapers like *The New York Times* or magazines like *Time and Newsweek*—*Electronics* never seems to get enough of the kind of letter that can clearly and logically lay out a point of view that is opposed to the one that has been printed in a particular article."

But perhaps the very best letters of all are those that carry on a debate in print. In this issue, on p. 12, we have the latest example of that form of communication, with two readers arguing the relative importance of bus speed. The two—Cipriico's Donald Peterson and Interphase's Michael E. Cope—may not have realized it when they were writing their letters, but they are serving a dual purpose: not only are they espousing a strong point of view in an interesting manner, but they are also helping to convey knowledge to their fellow *Electronics* readers.

So to sum up and make the point succinctly, which is what the best of the letters to the editor that we publish do, *Electronics* welcomes your letters and will gladly publish any that promise to make the jobs of our 375,000 readers easier and better.

Certain to help you on the job is the package of articles, featured on the cover, that begin on p. 59. They discuss the fast-growing world of the Small Computer Systems Interface and the impact that new implementations are having on the work-station picture. The fast, new chips for SCSI—pronounced "scuzzy" although it is anything but—are going to make it possible for personal computers to do the jobs of low-end work stations without the price premium of the work stations.

The key is speed. Up to now, the dilemma for the system designer has been that top-of-the-line personal computers bulge with lots of computing muscle, but they are slow of foot and do not offer the fast input/output channel for disk access that lets a work station zip along in multitasking and networked environments. The articles, by Jonah McLeod and Larry Waller, cover the latest developments in the field that are designed to overcome that obstacle.

Laurence Altman

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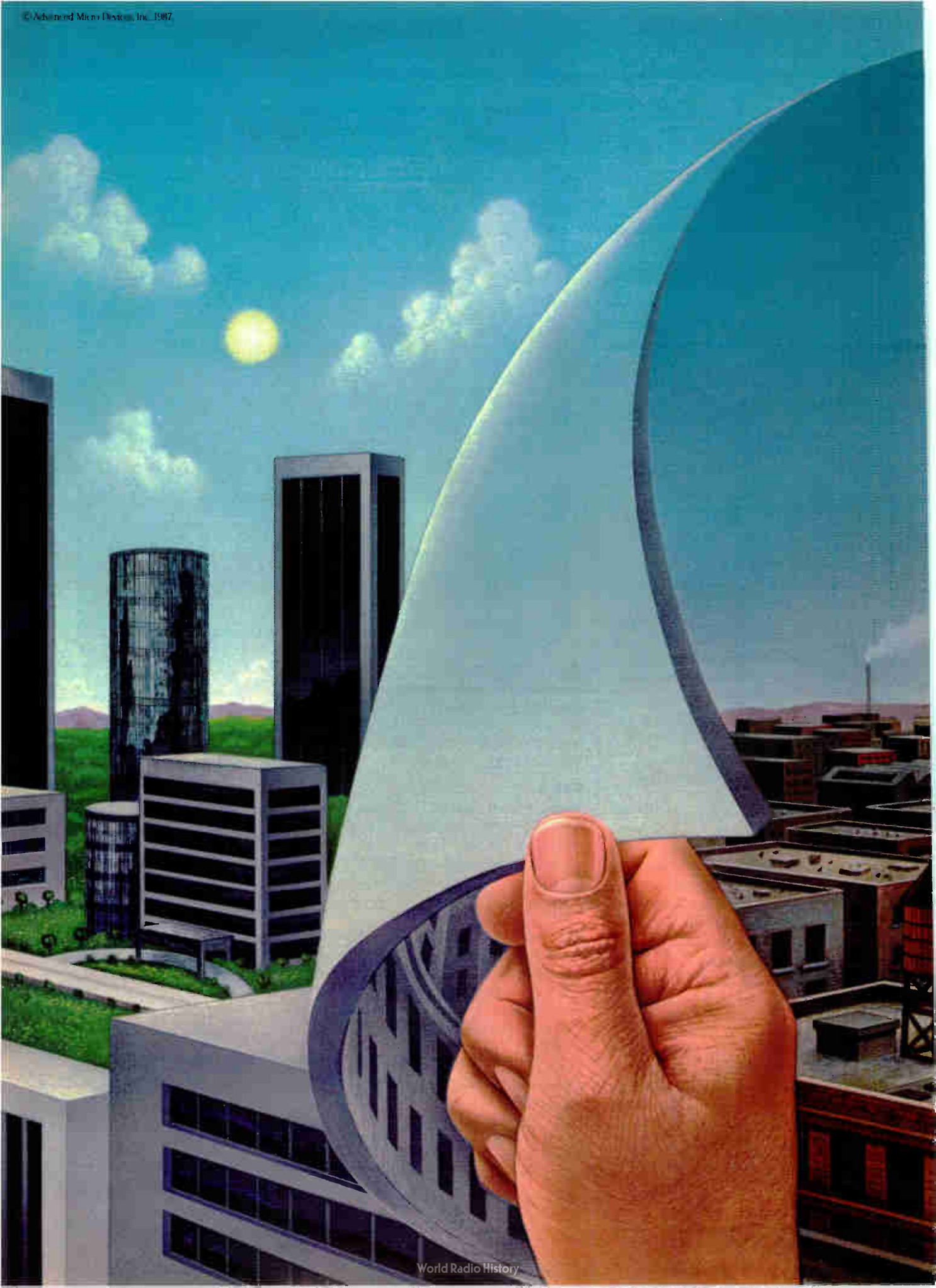

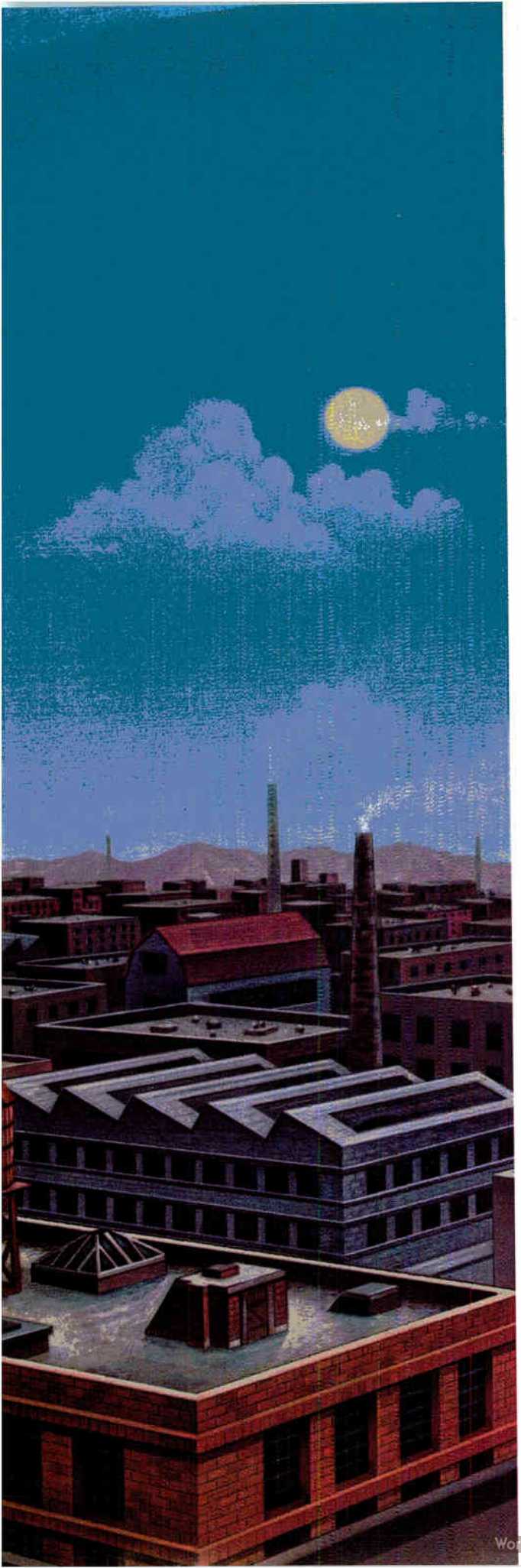

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In-stat's Jack Beedle, the bear who had earlier predicted a 1% downturn for 1988 U.S. semiconductor sales, now looks for a 12% to 13% growth rate

For those market forecasters who were conservative in their outlook for 1987 U.S. semiconductor sales, preliminary July numbers were much better than they expected. For the more bullish, July was right on track or maybe a little disappointing. Industry stats for July show the business remaining strong, despite expectations from many that chip makers were headed for the traditional summer slowdown. Bottom line: experts are bunching together on the 1987 outlook. The bulls are coming down and the bears are moving up—they're now in the 15.5% to 17.5% range.

The book-to-bill ratio in July was 1.15, reports the Semiconductor Industry Association, just about flat with June's revised 1.16 ratio. In-stat Inc.'s Jack Beedle, the biggest bear among industry forecasters, had expected the book-to-bill to dip below the 1.10 range, even though he had turned more bullish last spring. Jack had raised his 1987 estimate from 4% growth to a rise of 15.5%. He is now sticking to this figure, cautioning that this level of growth "is still not a shoo-in."

The most bullish forecaster, with the exception of the SIA, was Ed Henderson of Henderson Ventures. To him, the strength in July bookings wasn't surprising—"that still fits with my scenario," he points out. This spring he had raised his estimate from an 18% to a 19% hike.

But now Ed has cut back his 1987 estimate to a 17.5% growth rate. What's worrying him is the recovery of computer order rates. He is "worried about the computer business, because it's improving more slowly than we had anticipated. Seasonally unadjusted, June computer numbers look good; adjusted they don't look nearly as hot." As a result, he expects August to be a little soft for semiconductor bookings. Jack, too, is concerned about slow growth in computers: "The computer industry really bothers me."

Most forecasters still believe the computer business will pick up in the fall, and this should help make 1988 a good year for semiconductors. Ed had looked for 13.8% growth; now he likes the 19% to 20% range. Jack, who had predicted a 1% downturn earlier, now feels bullish about 1988. "The entire industry is looking much better," he says; "Import/export looks better, and the strength of the electronics industry looks better." As a result, assuming no change in the overall economy, Jack is predicting a 12% to 13% growth in U.S. semiconductor sales next year.

ROBERT W. HENKEL

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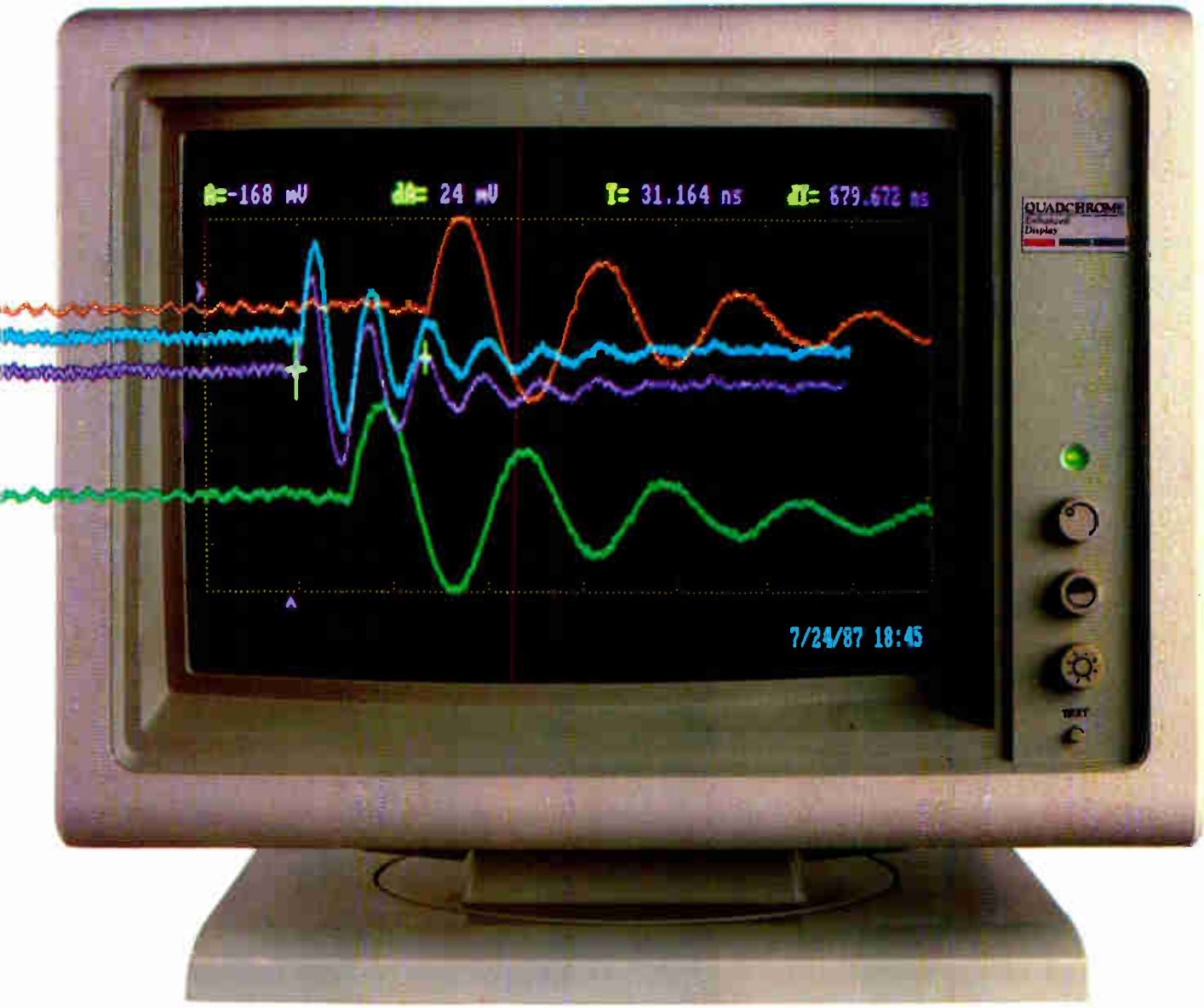

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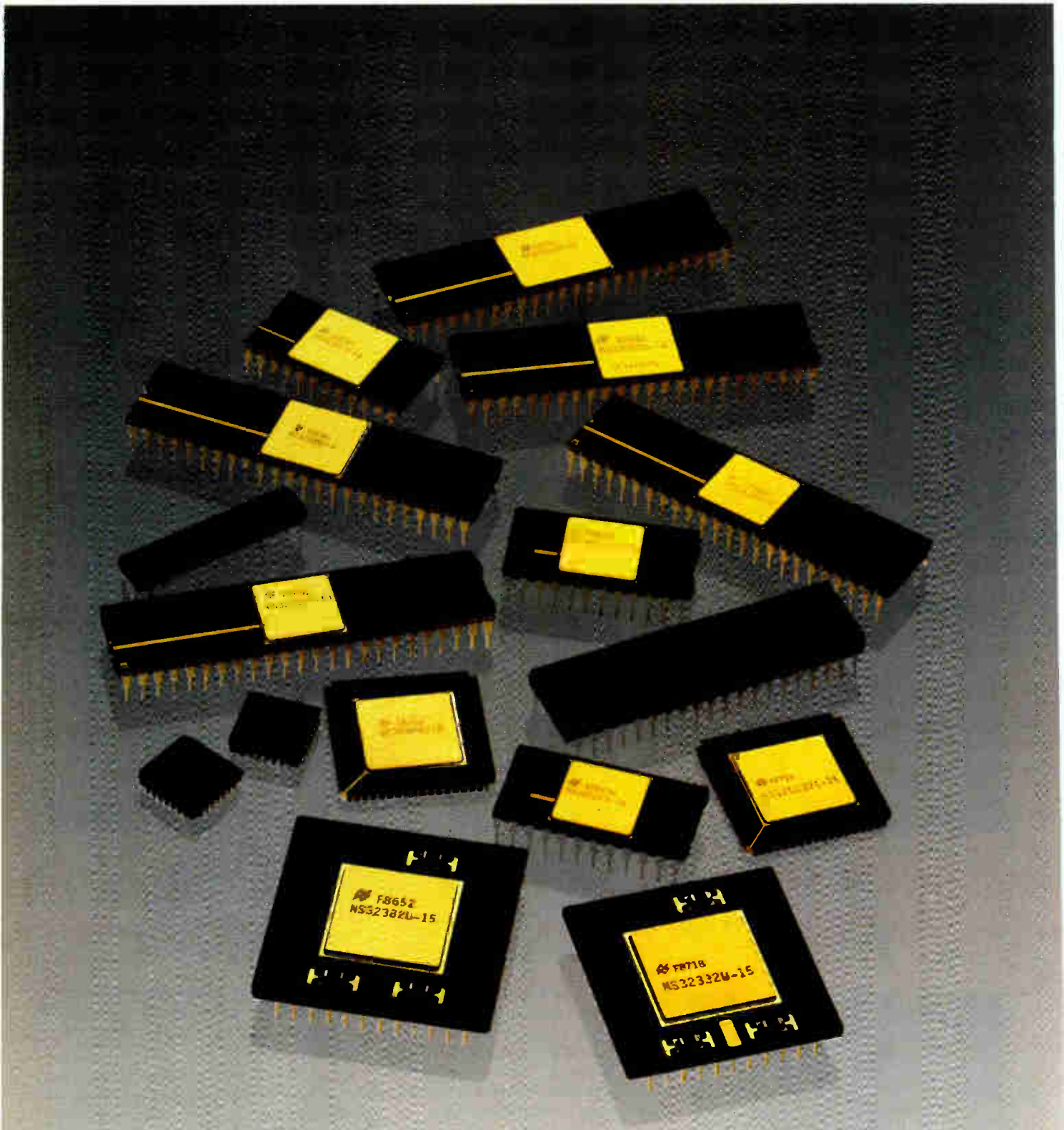

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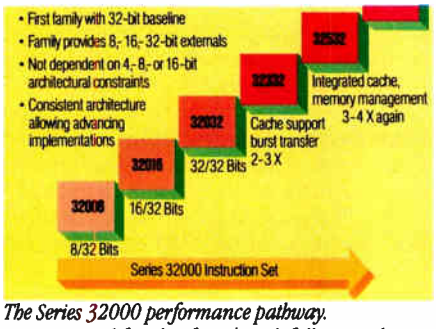

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LETTERS

It isn't all speed...

To the editor: Some of the comments made in the article "Update: Bus Interface Scores for Interphase" in the July 9th issue [p. 91] are quite misleading.

Although VMEbus speed certainly has some effect on performance, disk I/O throughput is dependent on the total time elapsed between the host's signal indicating an available command and the controller's signal that the command is complete. The amount of time spent transferring data and/or commands over the bus is typically less than 5% of this total. Most of the time delay is in disk access and rotational latencies, and a lesser amount in the software overhead.

Few applications are so heavily loaded that having a faster VMEbus interface will noticeably improve performance. Reducing firmware overhead, optimizing cache management, and using a command-queueing software interface that allows combining and ordering of commands all have much greater impact on increasing the system disk I/O throughput than the bus transfer rate does.

Although Interphase's BUSpacket interface is touted as providing 30-Mbyte/s performance on the VMEbus, this is possible only with memory boards that provide 25-ns access times, of which there are none currently available. Given present memory-board technology, realistic transfer rates tend to run in the 10-15-Mbyte/s range.

As an Interphase competitor, Ciprico has been actively upgrading its earlier VMEbus performance. Over a year ago, we incorporated a custom gate array into our VMEbus approach and can now achieve 34 Mbytes/s using the burst-mode capability of the VMEbus. But again, with the currently available memory, this is not usable performance.

Donald C. Peterson
Director of Marketing
Ciprico Inc.
Plymouth, Minn.

...but speed is a factor

To the editor: I agree that many factors affect disk controller performance, including advanced features such as caching, zero-latency operation, and many others. In fact, Interphase was first to market with almost all of those features years ago, and now all the major players, including Ciprico, have comparable features. I even agree that many applications with modest bus-utilization requirements see little advantage to higher bus speeds. Indeed, our first-generation VME products have these advanced features but lower bus speed, and they still have a thriving market.

As to the implication that bus speed is really not very important and cannot truly be achieved anyway, I totally disagree, as apparently does the entire market that is designing-in second-generation products. The whole name of the game in these very-high-performance platforms is maintaining massive data flow from multiple sources without saturating the bus. To do this, you must minimize bus overhead and maximize bus rate. These are exactly the issues that BUSpacket addresses.

As to the reality of our 30-Mbyte/s number, our published spec clearly states that to achieve it the target memory space must have a 30-ns access time. First-generation systems could not take advantage of the speed, I agree, but the nature of development is to remove obstacles one at a time, and the controller data rate is no longer the obstacle. Many of our customers are already taking advantage of the higher data rates, and several new standard memory boards and subsystems are currently entering the market specifically to address this issue.

Michael E. Cope
President, C. E. O.
Interphase Corp.
Dallas, Texas

Remember last year?

To the editor: Crediting GE/Intersil with the first commercial introduction of a sub-2-μm analog VLSI chip [*Electronics*, May 28, 1987, p. 84] is a mistake. The ADC-207 20-MHz flash A/D converter was introduced to the market by GE-Datel one year ago. The chip uses a 1.2-μm analog process developed at GE Corporate R&D, a predecessor to the Intersil process. It is in production at GE's Research Triangle Park, N. C., center.

Mike Demler
Group Leader, IC Design
GE-Datel
Mansfield, Mass.

Nothing added

To the editor: In your otherwise flawless explanation [*Electronics*, May 14, 1987, p. 38] of how our service operates, there was one error. The annual cost of $3,000 to $10,000 for unlimited access is an all-inclusive fee; there is not a $75 per call add-on as indicated by the article.

R. K. Helgeson
V. P., Corporate Communications
Teltech Resource Network
Eden Prairie, Minn.

Coming soon

An Aug. 6 article on Digital Signal Equipment's Codetext error-correction software [p. 110] incorrectly attributed a 12-dB encoding gain to competitive products. The 12-dB spec refers to a product under development at the company.

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Circle 13 on reader service card

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Before millions of people picked Macintosh,™ Apple® picked Motorola's M68000 Family—the brains behind one of the most successful computer products ever launched.

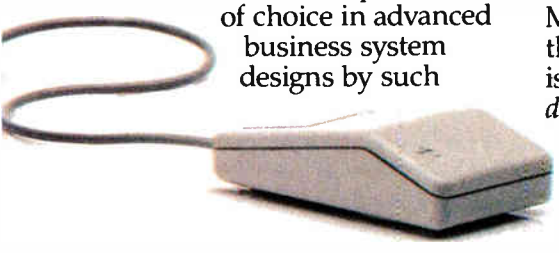
Now Apple has tapped the brainpower of the Motorola MC68020 microprocessor for the Macintosh II, bringing the high performance of a graphics workstation to business desktops everywhere.

72% of all 32-bit systems ever shipped included at least one MC68020. That's more than half a million high-performance systems.

The high-performance business solution.

The MC68020 is not just the overwhelming choice in workstations—it is now setting new performance standards in the office—where it is essential to the computation, graphics and communication necessary for interconnected systems.

While Apple's choice of the MC68020 was a smart move, there's no license on genius: the '020 is the microprocessor of choice in advanced business system designs by such industry leaders as Altos, Alpha Micro, Casio, C.Itoh, Fujitsu, Honeywell Bull, NEC, NCR, Olivetti, Plexus, Ricoh, Sanyo, Sharp, TI, Toshiba and UNISYS.



The graphics solution.

The M68000 family helped Apple implement the visionary "point and click" graphic workstyle that has driven productivity up while driving training costs way down. Businesses of all sizes are discovering dramatic productivity increases in office computing through innovations such as desktop publishing.

The software solution.

Among programmers and designers dedicated to creating the best, most innovative applications, the M68000 architecture has been the leading choice by far—with over *seven million M68000* systems installed since 1979.

Meanwhile, the MC68020, on the market now for three years, is already backed by *two billion dollars worth* of 32-bit software. This is more 32-bit software than all competitive products combined!

The Brain Trust: Where M68000 microprocessors predominate.

Engineering Workstations
Apollo, Hitachi, HP, Sony, Sun, Tektronix.

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Apple, Canon, HP, IBM, QMS, Ricoh.

Departmental Computers
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PBX and Telephone Systems
AT&T, Northern Telecom, Siemens.

Fault Tolerant Systems
IBM, NCR, Stratus, Tandem.

Supercomputers
Alliant, BBN, Caltech, Fifth Generation.

Factory Automation
Allen-Bradley, ASEA, Bailey Controls, GM, Mitsubishi, Square D.

Join the Brain Trust.

Challenge us to persuade you of the sound business and technical reasons to join the M68020 Brain Trust. Write to us at Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

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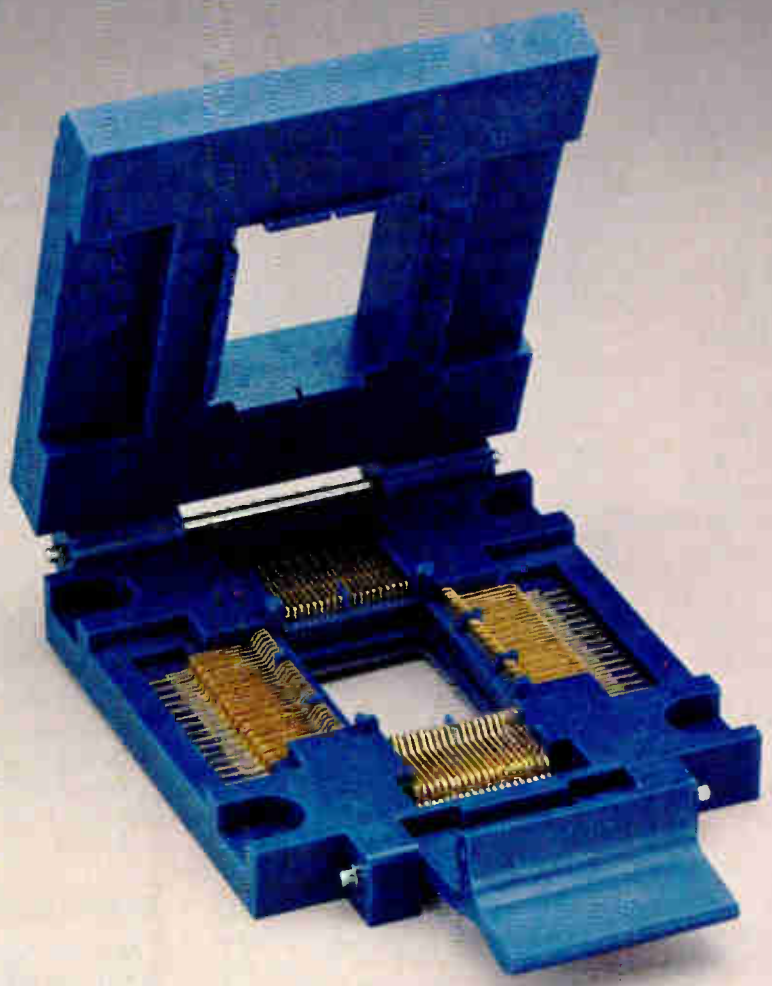

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In fact, our IC 51/53 family alone offers over 360 basic configurations. And with package variations, the number moves well into the thousands.

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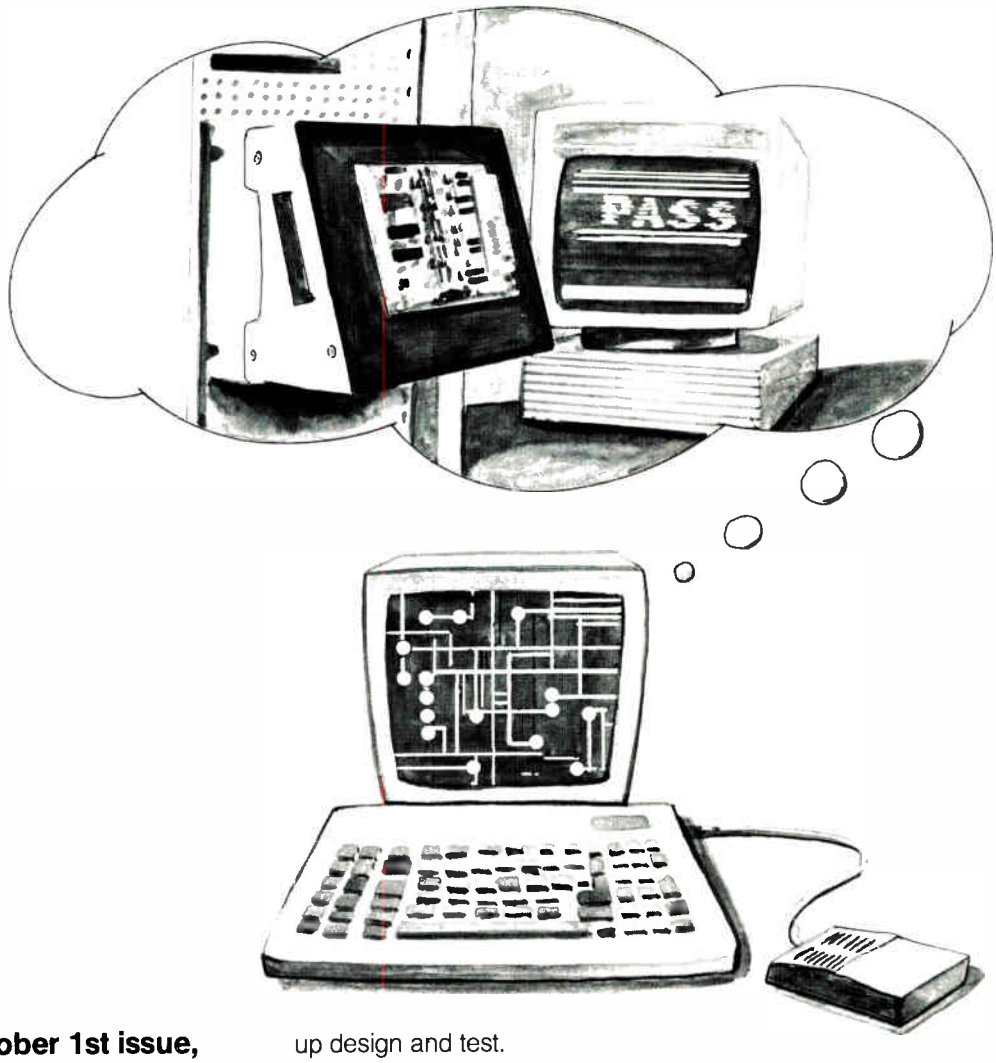
Integrating CAD with ATE— a dream come true?



In the October 1st issue, the editors of *Electronics* magazine examine the new technologies bridging the gap between computer-aided design and automatic test.

They reveal that new technologies emerging to improve relationships between CAD and ATE are no daydream. And they'll open your eyes to a new generation of simulators specifically geared at speeding up design and test.

There's more. Major coverage of the continuing explosion in microcontrollers. Plus an exclusive look at new single-chip micros targeted for specific functions and applications. And that's not all. Our look at the progress being made in ISDN, predicted to be the next big commodity market, will really wake you up.

It's an issue packed full of important information that will keep more than 131,000 technical managers and senior engineers reading late into the night. And an issue that will provide advertisers looking to reach them with a dream opportunity.

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Electronics

ELECTRONICS NEWSLETTER

AFTER TWO BLAH YEARS, U.S. ATE SALES MAY GROW 12% A YEAR THROUGH 1991

Renewed electronics-industry demand and an improved foreign-trade climate are boosting prospects for U. S. makers of automated test equipment, says a study released this month by The Freedonia Group Inc., a Cleveland market-research firm. Following sluggish growth in the 4% to 5% range during the 1985-1986 recession in the electronics industry, ATE shipments by U. S. firms will grow at 12.7% per year through 1991 to $2.9 billion, the report says. Integrated-circuit test equipment will show the fastest growth within the category at 14.6% annually, producing a $1.3 billion market by 1991. The Freedonia Group also foresees an improved market for all kinds of test and measurement gear, for which it projects a 9.8% yearly growth, with shipments by U. S. vendors totaling $10.4 billion by 1991. □

CONSORTIUM SET TO CHOOSE VENDOR FOR ITS VMEBUS INTERFACE CHIP

A consortium of 20 or so board makers formed in March to develop an interface chip for the VMEbus has completed its specification and expects to select a vendor by next week. The consortium was organized by Joseph S. Ramunni, director of marketing and sales for Heurikon Corp., Madison, Wis., when VMEbus originator Motorola Inc. said it would not sell its own VMEbus interface chip. Motorola has since joined the group and expressed a willingness to sell its chip, but the group went ahead with plans for its own chip, which will have more functionality than the Motorola part. Prototypes of the 6,000- to 8,000-gate device will be ready by April, with production availability for group members by the third quarter. Pricing target is about $50 per chip in lots under 1,000 for members. The VMEbus interface chip is important, says Ramunni, because discrete implementations take up 15% to 25% of board space. Meanwhile, Force Computers Inc. of Los Gatos, Calif., has designed a VMEbus interface chip of its own (see p. 66). □

AT&T IS USING ASIC TEST GENERATOR THAT WORKS WITH ALL ITS DESIGN TOOLS

AT&T Co. has developed and begun to use an integrated test-generation program for its CMOS application-specific integrated circuits. The system, called TPG2 (for Test Program Generator), is linked directly to AT&T layout and simulation tools, providing an automatic data-capture facility that cuts down design time and reduces errors, says Donald Denburg, a Bell Laboratories engineer. TPG2 generates full-production test programs, a probe-card design, a wiring diagram for a load board, and specifications for burn-in and reliability testing. Automatic test generation is ideal for ASICs, Denburg says, because they require such great flexibility from design equipment. □

HELICAL-SCAN TAPE DRIVE COULD MAKE IT BIG IN DATA STORAGE

A new kind of computer tape drive is likely to shake up the booming tape business by 1990. The helical-scan tape drive, a technology spinoff from digital audio tape, should be selling 200,000 units a year by then, says a report compiled by the consulting firm Peripheral Strategies Inc. Its advantage is that tape wrapped in helical fashion at a 6° or 7° bias permits higher track densities, through a better head/tape reading angle, than horizontal-scanning drives allow. Videotape machines have used helical scanning for years, but DAT optimizes the technique for digital, rather than analog, recording. A survey of 30 original-equipment manufacturers, the potential buyers, revealed "serious enough interest that helical-scan tape drives will be the next major tape technology," says Lee Elizer, president of the Santa Barbara, Calif., firm. If nagging political problems do not delay DAT, revenues for helical-scan computer drives should top $555 million by 1992. □

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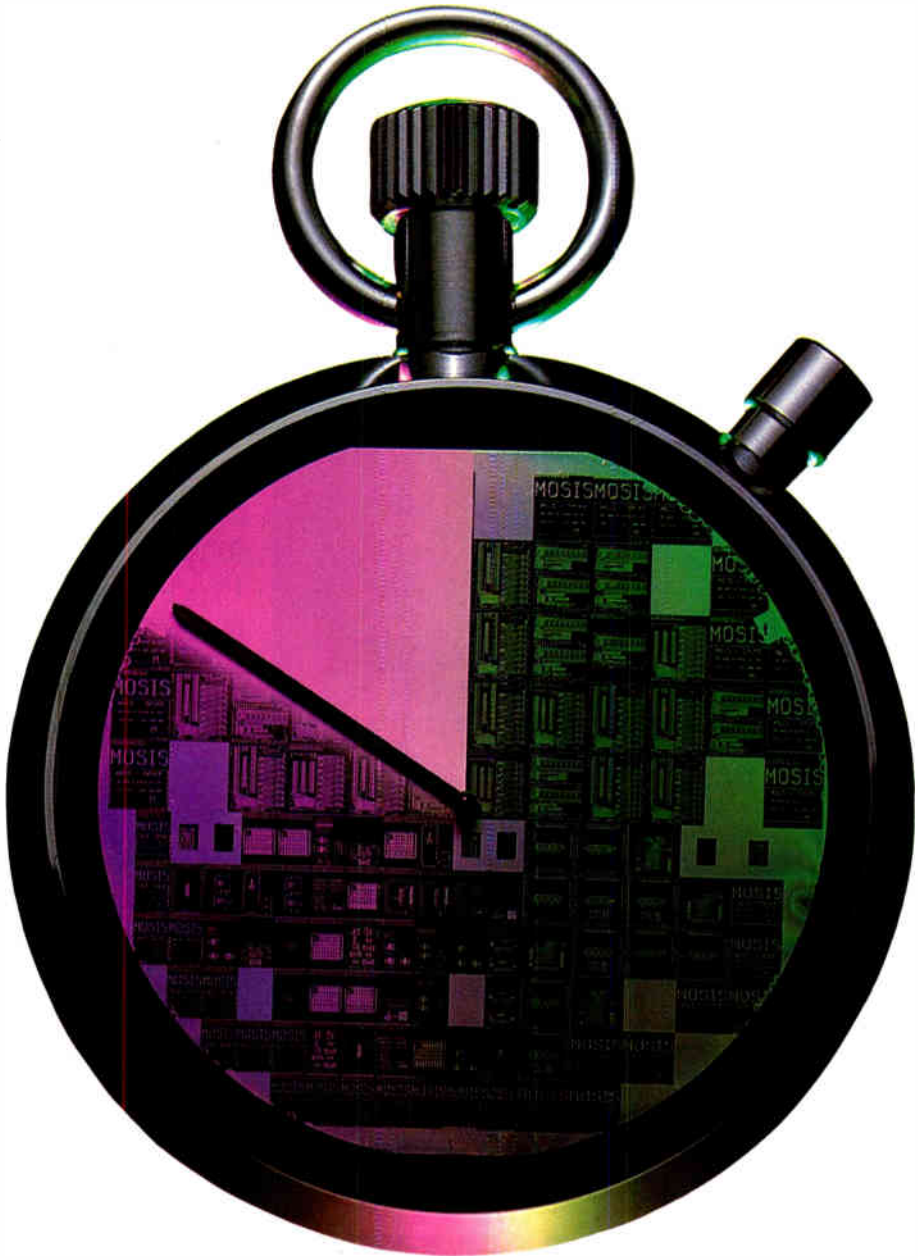

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PRODUCTS NEWSLETTER

LSI LOGIC BOOSTS CHANNELLESS ARRAY SPEED UP TO 40%

System designers can squeeze high-performance logic and up to 16 Kbits of read-only memory on a single semicustom chip with LSI Logic Corp.'s newest channelless arrays. Typical internal gate delays for a two-input NAND gate are 0.57 ns, compared with 1 ns for the company's low-density channeled arrays, increasing speed by about 40%. Fabricated in the Milpitas, Calif., company's advanced 1.5-μm, double-level-metal CMOS process, the LMA9000 series can implement up to 4 Kbits of 15-ns random-access memory or as much as 16 Kbits of read-only memory because of innovative transistor placement. The LMA9000 family has 700 to 10,000 usable gates and up to 158 input/output pads. The LMb6000 family has 700 to 6,700 usable gates and up to 82 I/O pads. Pricing varies with design complexity and packaging. □

LOCAL NETS CAN TRANSMIT UP TO 2,400 FT WITH EXAR TRANSCEIVER CHIP SET

Local-area networks using either a star or a bus topology can triple their maximum transmission distance with Exar Corp.'s transceiver chip set, stretching as far as 2,400 ft. for the star, 1,600 ft. for the bus. Designed to support Starlan controllers such as Intel Corp.'s 82586 and 83588, the two-chip Exar set achieves its performance advantage by segregating appropriate functions on one bipolar analog chip and one CMOS digital chip, instead of opting for a bipolar single-chip solution [*Electronics,* June 25, 1987, p. 89]. Segregating the functions leads to line-reflective indexes two to three times lower than competing systems, says the San Jose, Calif., company. The digital CMOS XRT82C516 contains Manchester encoding and decoding logic, clock and compare circuitry, collision detection, carrier sensing, and transmission control logic. The analog bipolar XRT82515 contains variable-gain and summing amplifiers, filters, level detectors, and phase comparator circuitry. Available now, each chip set costs $17 in 1,000-unit purchases. □

AT&T OFFERS COMPACT FIBER-OPTIC TRANSMIT/RECEIVE MODULES

A set of 1.3-μm-wavelength transmitter/receiver modules simplifies fiber-optic systems design. The modules arrive in fully functional packages just half the size of a board designed using discrete components. The newest additions to the Astrotec family of lightwave products from AT&T's Components & Electronics Systems Division also boast 1-gigabit/s transmission and 1.7-gigabit/s receiving capability. The 1218-Type Astrotec Lightwave Transmitter uses an indium gallium arsenide phosphide laser and can be individually specified for output power, bit rate, and spectral options. The Astrotec 1306AA Lightwave Receiver has a high-performance, low-capacitance avalanche photodiode and a GaAs preamplifier circuit with adjustable transimpedance for extra sensitivity. Depending on specification, the transmitters cost $2,500 to $4,500 and the receivers $2,850 each, in lots of 100. □

NORSK'S 3.5-MIPS SUPERMINI FITS UNDER A DESK

Norsk Data A. S. is stepping up its invasion of the U. S. with a line of 32-bit superminicomputers that compete with IBM Corp.'s 9300 and Digital Equipment Corp.'s VAX on price and performance but fit into a smaller package. Up to 50 users can network on the Compact ND-5000 system, which runs at 3.5 million instructions/s and fits in a box about the size of a two-drawer file cabinet—compared with the refrigerator-sized competition. The Oslo-based company's U. S. subsidiary, Norsk Data N. A. in Westboro, Mass., says five models will be available in October and will cost from $51,500 to $317,150. □

PRODUCTS NEWSLETTER

CHIP BOOSTS RESOLUTION OF IBM'S VIDEO-GRAPHICS ADAPTER 250%

Aggressive chip-design houses are already supercharging IBM Corp.'s Video Graphics Adapter standard. Tseng Laboratories Inc.'s 15,000-gate chip delivers 2.5 times the resolution—1,024 by 768 pixels, compared with IBM's 640 by 480. The ET3000 offers 16 colors from a 256,000-color palette in its high-resolution mode and 256 colors in its 800-by-600-pixel mode—16 times the VGA standard. Fabricated in 1.5-μm CMOS technology, the Newtown, Pa., company's chip is register-level compatible with IBM's VGA and EGA modes and BIOS-level compatible with all other standards. Its 65-MHz video clock rate supports interlaced and non-interlaced displays, including IBM's $1,500 Model 8514. Samples will be available to selected original-equipment manufacturers in September. Production chips will cost $40 in November. □

TWO HP WORK STATIONS NOW DO MATH NEARLY THREE TIMES FASTER

A floating-point accelerator from Hewlett-Packard Co. puts the company's mid-range and high-end work stations on a faster math track, increasing speed almost threefold. With the 98248A board installed, HP's model 330 performs 236,000 full-precision floating-point operations/s using the Linpack benchmark—compared with 97,000 flops without the board. Model 350 runs 330,000 flops with the board and 123,000 flops without it. Available now, the 98248A costs $5,800. HP has also introduced an error-checking and error-correction random-access-memory board set for the 350 that means users can configure RAM systems of up to 48 Mbytes without worrying about memory failures because of soft errors. The boards correct single-bit errors without notifying the user, but double-bit errors are reported to the user. The Fort Collins, Colo., division estimates mean-time between double-bit errors at five years. The 8-Mbyte HP98264A card costs $12,800 and the 16-Mbyte HP98264B costs $20,000. Delivery time is eight weeks. □

200-MHz ADVANTEST TESTER CAN HANDLE THE FASTEST VLSI CHIPS

Using an advanced test head based on emitter-coupled-logic technology, Advantest America Inc.'s T3381 system hits speeds up to 200 MHz—fast enough to test the fastest new VLSI chips and application-specific integrated circuits. The Lincolnshire, Ill., company's ECL-based test head boasts overall timing accuracy within ±400 ps while its general-purpose test head offers accuracy within ±500 ps. The tester's 512-pin input/output capacity makes it capable of testing the largest VLSI and ASIC chips. Testing efficiency is enhanced by an architecture that integrates device design with testing and evaluation. A 32-bit processor uses a specialized test-programming language to boost throughput. The system can also serve as a virtual terminal for test-system operation through an Ethernet network. Available now, the T3381 ranges in cost from $1 million to $6 million depending on configuration. □

MEGATEK'S 200,000-VECTOR/S SYSTEM RUNS 33% FASTER

Megatek Corp. has dealt itself into the burgeoning market for high-end graphics packages with two systems. Model 9100 renders 3-d color wireframe objects at a rate of 200,000 vectors/s—performance about one-third better than the competition. Model 9300, a surface-rendering display system for creating solids and shaded objects, paints 20,000 polygons/s; that performance is comparable to Sun Microsystems Inc.'s 4/260CXP work station. The products use VLSI circuitry and a 32-bit floating-point engine for real-time object manipulation, says the San Diego, Calif., company. Available now, a base-priced 9100 costs $24,000, and the 9300 starts at $35,000. □

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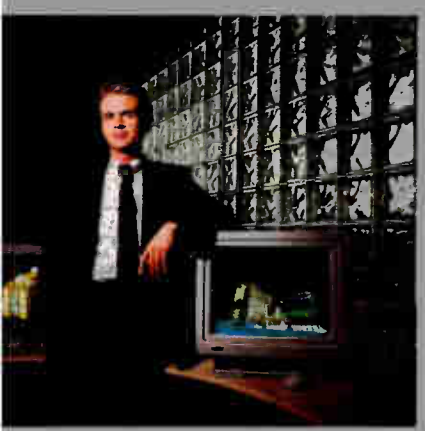
Circle 27 on reader service card

Digital has it now.

"It's access – fuller, easier information access that's at the heart of our success in selling Digital's networked desk-top computing," states Tom Curry, vice president of Marketing at McDonnell Douglas Manufacturing and Engineering Systems Company. "Architectural engineers now realize that the isolated PC is not the answer."

In Mr. Curry's view, Digital's ability to network, plus compatibility from individual workstations to huge processors are ideal for the architectural community. "For any building project to progress smoothly, there has to be a coordinated effort. The group working on lighting, for example, needs to share information



"With Digital's networked desk, McDonnell Douglas is giving architectural engineers a more productive way to build."

with those designing heating and ventilation. In the Digital environment, that's exactly what they do."

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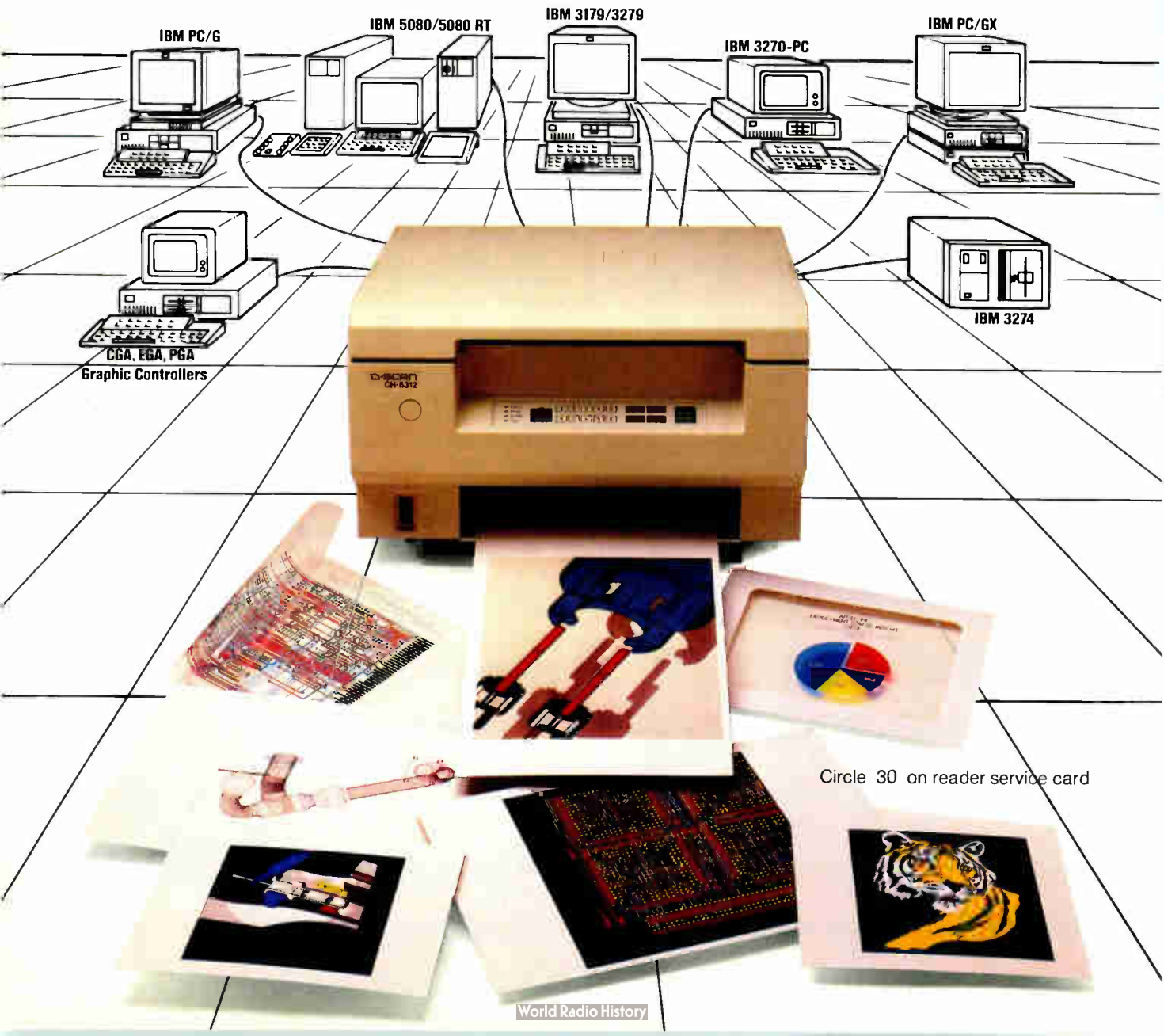

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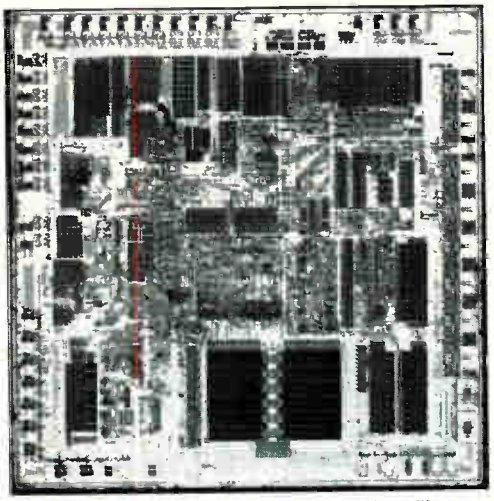
Electronics

ATTACK ON 386 TERRITORY OPENS A MARKET—AND A WAR

AMD's 16-MHz 286 CHIP IS JUST THE BEGINNING; HOW WILL INTEL RESPOND?

NEW YORK

A new segment of the personal computer market, the high-end 16-bit IBM-compatible PC, is attracting companies the way a pond draws kids in August. Earlier this month Advanced Micro Devices Inc. and Chips & Technologies Inc. staked out the territory. Now Intel Corp. is not expected to leave AMD unchallenged in microprocessors for the segment, and Faraday Electronics is getting set to offer support chips rivaling those from Chips & Technologies. The first system-level entries should show up by early next year—or even as soon as November's Comdex/Fall show—and further developments in the support-chip arena promise to usher in IBM-compatible systems with high-speed Microchannel expansion buses like the ones in IBM's high-end PS/2 models.



MARKET MAKER. AMD's 16-MHz 80286 will serve high end of the 16-bit IBM PC-compatible market.

AMD started it all with its 16-MHz version of Intel's 16-bit 80286 microprocessor. Intel, for the record, says it has no plans to produce a 286 that runs faster than its current 12.5-MHz version, citing a lack of customer interest. But the company also has its market for the 32-bit 80386 to protect, and the new 16-bit high end invades that chip's turf.

Also, AMD has increased its pressure on Intel through a long-term second-sourcing agreement covering Intel microprocessors, and it seems likely that Intel will be forced to respond. AMD has pushed 286 prices down and performance up, and its 16-MHz part ups the ante even higher. Further spicing the brew, the two companies are engaged in a heated legal battle. AMD is trying to force Intel to hand over the 386 design for second sourcing, and Intel is attempting to end all AMD second sourcing of Intel parts.

NOT WAITING. However, the legal wrangle may not be resolved for some time, and industry insiders say that Intel is working on another response to AMD, a microprocessor nicknamed "the AMD killer." Reportedly designated the P9 and scheduled to go on the market early next year, the chip is supposedly a step down from the 32-bit 386, with a 32-bit internal architecture and a 16-bit external data path. It is said to be software-compatible with the 286 and aimed at systems based on the bus used in IBM's PC AT. Intel won't comment.

Meanwhile, the others are plugging away. With the help of support-chip vendors like Chips & Technologies and Faraday, PC vendors can use AMD's 16-MHz 286—and presumably the Intel P9, if and when it appears—to build systems that outperform the 286-based members of IBM's PS/2 line by a substantial margin, and that even run neck and neck with such 32-bit PCs as the Compaq Deskpro 386, so long as the 32-bit system is running 16-bit software.

And 32-bit software for IBM and compatible PCs may be a long time coming; the operating system that will unlock the power of the 386, Microsoft's OS/2, is still not due to appear for another five or six months. Application software won't follow for another six months or a year. The PC software base that exists now is composed of 16-bit applications written to run under the MS-DOS operating system, and the coming generation of fast 16-bit machines will pick up this software and run with it.

Cost is another important factor. The 386 is a pricey piece of silicon, about $250 in quantity (the 16-MHz part), and it is likely to remain expensive for some time due to its sheer complexity. The 286 is a much smaller chip, and AMD will sell even its premium 16-MHz part for $150 in lots of 100. Until truly compelling 32-bit products appear from software houses, the price-performance of high-end 16-bit systems is going to be far more attractive.

The new generation of high-end 16-bit PCs is likely to be defined relative to IBM's entries, models 50 and 60 in its PS/2 line, which are about 50% faster than the latest PC AT with its 8-MHz 286 processor. With a boost from the performance-enhancing features of the 16-MHz 286 support chips Chips & Technologies introduced earlier this month, a 16-MHz 286-based system will outperform a PS/2 model 50 or 60 by a factor of 50% or better, says Diosdado Banatao, vice president of systems logic.

Last week Faraday disclosed plans to introduce a support-chip set for 16-MHz 286-based PCs in the third quarter. The Sunnyvale, Calif., firm has also developed enhancements to the basic PC AT architecture that allow hardware vendors to squeeze more performance from their systems.

One potential limit to performance of systems compatible with the PC AT is the expansion bus of the IBM system. The Microchannel bus IBM developed for its higher-performance PS/2 systems is far faster than the PC AT bus, but builders of compatible systems face some problems in moving to the Microchannel. IBM has applied for a number of patents on the technology used in the Microchannel bus, patents that the company is expected to protect vigorously. Furthermore, there are no support chips for building interfaces to the Microchannel.

Both problems will be resolved fairly soon, spokesmen from both Faraday and Chips & Technologies believe. When IBM receives its patents, it will license those patents to makers of Microchannel-interface chips, which can then pass on the rights to their customers, says Banatao. Thus IBM, rather than stopping makers of compatible systems from basing their products on the Microchannel, will simply derive some income from those sales.

–Jeremy L. Young

PACKAGING

TAB FOR VLSI COMING FROM FAIRCHILD

PALO ALTO, CALIF.

Tape-automated bonding has been around for 15 years, but it has been called upon only recently to attack the problem of housing VLSI chips. In fact, progress in VLSI has been so swift that circuit density has outstripped the input/output-connection and heat-removal capabilities of available integrated-circuit packages. Those limitations will soon be stripped away if the TAB work at Fairchild Semiconductor Corp. pans out.

The Fairchild TAB process, called Delta (for dense lead tape), has been under development for several years, and one version—with a lead pitch of 100 μm and 300 to 400 pins—will become a production system by the middle of 1988 in Fairchild's digital-circuit-packaging facility.

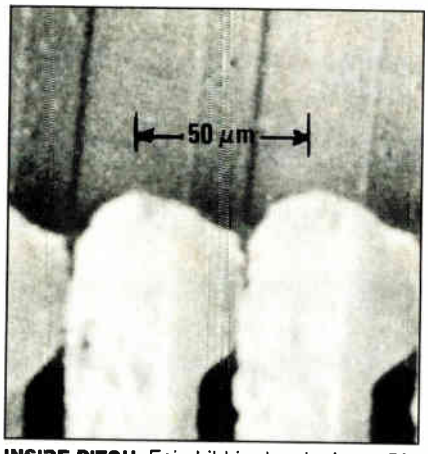
More dramatically, a Delta system under development with 50-μm pitch (about 2 mils), can accommodate an IC structure containing more than 400 leads. That system should be in place about a year later. By comparison, the current VLSI leader, the 100-μm pin-grid array, can accommodate only 256 pins in its standard package. So with Delta, chip size will no longer depend on bond-pad real estate. The process is also faster than other bonding techniques.

DESIGN CHORES. To achieve the density, Fairchild engineers had to design their own tape, which is manufactured for them by 3M in Austin, Texas, says Bill Phy, manager of packaging technology research at Fairchild. They also had to redesign extensively a commercial bonding station to get the needed transport, resolution, and heating characteristics. "There's not much left of the original machine," Phy says.

The tape and bonding processes contain many new features aimed at providing the high density and other benefits for various packaging needs. Among them: forming before individual sections are excised from the parent tape; testing after interleaf bonding; a carrier that ensures tape flatness during bonding; floating alignment to allow the tape to move around within the carrier without damage; and high-adhesion bumping, with minimal undercutting.

In the 50-μm system, each lead exiting a device is 25-μm wide and 25-μm thick. The pitch, or standard lead density, in production today for TAB is 150 to 200 μm. For example, 3M has been shipping custom tape with up to 600 leads; however, the pitch is 4 mils.

Delta makes use of the pulse-reflow heating method, with a gold-tin eutectic formation. The method can apply heat quickly, in a burst mode, to metallic objects with low thermal mass—like the thermode—thus speeding the bonding process. The specially designed thermode acts like a resistive element, permitting the bonding rails to heat to a uniform temperature. Thus the thermode temperatures can be maintained to within ±5°C. Additional proprietary methods eliminate one objection to tin-plated tape: tin whisker growth, which can eventually result in short circuits.



INSIDE PITCH. Fairchild is developing a 50-μm pitch version of its Delta TAB process.

In the modified bonding station, the thermode sits above the circular bonding table, and a slide carrier containing the tape is positioned with 1- to 2-μm accuracy—twice as good as other bonders. Because standard optical microscopes cannot resolve the dimensions, Fairchild designers have come up with a high-resolution charge-coupled-device camera containing an image intensifier. A high-intensity fiber-optic light source feeds the periscope used for alignment.

DESIGN DRAWBACK. Although the equipment can assemble extremely dense packages faster than conventional wire bonding, it still has some limitations. One drawback is the fact that each individual tape must be custom designed for a particular IC, and its wiring pattern and die holder may need a redesign for even minor deviations. By contrast, wire-bonding machines can be reprogrammed easily for various bonding patterns.

Another limitation rests in the tape manufacturing. The yield at high-pitch densities needs improvement if the system is to become economical. Fairchild designers are now using the 100-μm TAB technology on a 12,000-gate bipolar array and are taking advantage of TAB's speed to package a fast biCMOS 256-Kbit memory. *–Stan Runyon*

COMPUTERS

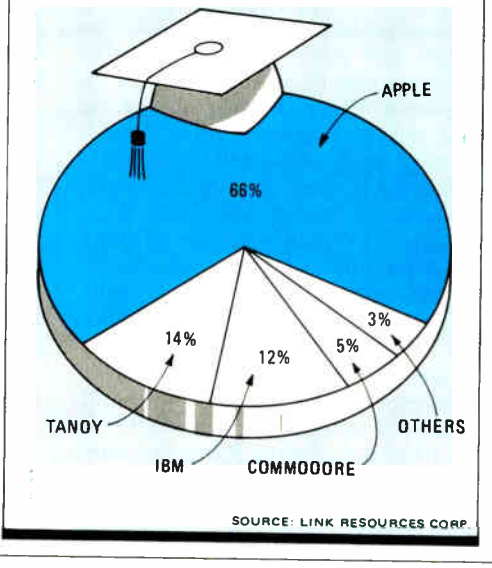
CAN IBM CATCH UP WITH THE APPLE SCHOOL BUS?

NEW YORK

Despite its tremendous marketing clout, IBM Corp. is not a strong favorite to unseat Apple Computer Inc. in U.S. classrooms. IBM jumped into the educational computer market this month with a new low-priced version of its Personal System/2. The Model 25 is the company's first low-end offering since it dropped the unsuccessful PCjr two years ago.

At best, one analyst says, IBM has no better than an even chance in this market where price, not performance or service, is paramount. And while skeptics might wonder why IBM is so concerned over getting a piece of what is a relatively small and low-margin market segment—less than a half million units were sold in 1986, according to one industry analyst—IBM's motives are clear: it wants students, the PC buyers of the fu-

APPLE DOMINATES THE SCHOOL MARKET



ture, to train on IBM machines.

So far, IBM hasn't been able to accomplish that. It trails Apple and Tandy Corp. of Fort Worth, Texas, in computer sales to educational institutions. In the year that ended June 1986, IBM accounted for just 12% of the 447,000 machines shipped to public schools, according to Link Resources Corp., a New York market researcher. By contrast, Apple sold 66%, and Tandy 14% (see chart, p. 32). Now, despite IBM's aggressive marketing plan, "I'd say they have a 50-50 chance," says George Colony, an analyst with Forrester Research Inc. of Cambridge, Mass.

IBM also faces an uphill battle because it is essentially starting from scratch. Some 58% of the installed base of 1.363 million personal computers in U. S. schools are Apples. Only 7% of the total—95,410 units—are IBM PCs.

That doesn't faze IBM, though. The market is ripe with potential for bulk sales, declares Proctor Houston, director of IBM's Educational Systems Marketing Operations in Atlanta. He points out that there are 44 million students attending public schools throughout the U. S., plus another million students in the nation's private schools, leaving ample room for growth.

FEEDING GROWTH. IBM's strategy is to feed that growth with high-volume sales. It isn't just hoping that the Model 25 will attract the interest of schools, and eventually the students that will then learn to use it, with its new system's compact, Macintosh-like design and low price—about $1,350 with a black-and-white monitor. The company is also pressing its point with cut-rate offers, including discounts of about 20% on sales to schools, colleges, professors, and even students and staff.

To do that IBM is extending its direct-marketing sales techniques, which have been successful in the business world, to schools as well. Colony points out that most school computer purchases are through dealers, such as ComputerLand and Tandy's Radio Shack, where more-expensive IBM products get overlooked by frugal buyers. Direct sales could counter that disadvantage.

An executive at Apple, who asked not to be named, says IBM is also spending heavily to seed the higher-education market with gifts of equipment and software—perhaps by as much as $250 million in the past year. With the announcement of the PS/2 Model 25, the executive says, "it looks like they're doing something in the kindergarten-through-12th-grade category."

In its standard configuration, the Model 25 comes with an 8-MHz Intel 8086 central processor; 512 Kbytes of random-access memory; and a 720-Kbyte 3.5-in. floppy disk drive (a second drive is optional). Also included are a monochrome display; IBM's dual-mode Multi-Color Graphics Array chip, which offers either 320-by-200-pixel resolution and up to 256 colors or 640-by-480 resolution with two colors; and two expansion slots. A prepackaged version aimed at college students adds a second 3.5-in. floppy disk drive, the DOS 3.3 operating system, Microsoft Windows 1.04, and a mouse. *–Tobias Naegele*

CONVERTERS

TRW'S 10-BIT ADC LEADS THE PACK

LA JOLLA, CALIF.

In the fiercely contested converter business, the leader is usually the one with the hottest new part. Right now that's probably TRW Inc., whose LSI Products Division has beaten the rest of the field to market with a key product that its rivals have been trying to develop for years: a 10-bit "flash" monolithic analog-to-digital converter.

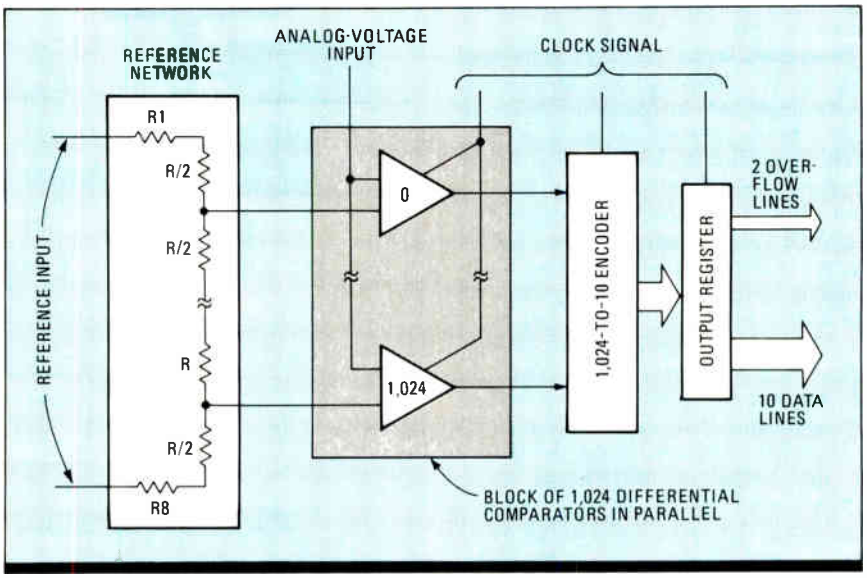
Its 10-bit resolution and its flash conversion speed of 25 megasamples/s give the part more importance than just an incrementally improved product, says consultant William I. Strauss, president of Forward Concepts Inc., Scottsdale, Ariz. Rather, the TRW ADC represents "one more step, and a big one at that, up the performance ladder" in a conversion market that holds much opportunity, he says. With the 10-bit part, TRW can carve out a "conversion leadership role once again," he predicts. The La Jolla, Calif., division showed the way with the first monolithic 8-bit converters in the late 1970s, but since has been passed by its competitors.

Strauss, who closely follows the conversion field, says the monolithic ADC market will grow at nearly 28% annually over the next five years from a $223 million sales base in 1986. Digital-to-analog sales are growing slightly slower, but both types of monolithic parts are eating rapidly into bulkier and more expensive hybrid converters that until recently held the lion's share of this business. The impetus largely comes from advances in digital signal processing, particularly commercial video and military radar equipment, which "can't do anything without fast conversion," says Strauss.

TRW's new 1-μm TDC1020 is its second pass at the 10-bit target; an attempt in 1979 failed because, among other reasons, the 2-μm technology then available resulted in a very large chip. In the meantime, the division came out with a successful 1-μm 9-bit device dubbed the TDC1049.

"But the difficulty of adding just one more bit to a flash converter remained a formidable challenge," says Willard K. Bucklen, director of analog products. The bedrock problem is doubling the entire on-chip comparator network (to 1,024 differential comparators) to get the extra bit, which would double the 254-mil-by-254-mil die size as well as the power, he explains. Obviously, circuitry had to be simplified without sacrificing performance, a problem TRW engineers have managed to solve.

Bucklen credits improvements that in-



FLASH. TRW's 10-bit analog-to-digital converter can turn out 25 megasamples/s.

clude a refined comparator design that benefits from "extremely good transistor matching across the entire die" and proprietary differential-decoding circuitry. Also, "our decoding method reduces the magnitude of errors due to extremely high input slew rates," he says. The result is a slightly larger chip at 264 by 264 mils. Its 25-megasample/s rate comes with ±½ least-significant-bit differential linearity error and ±1 LSB integral linearity error. Signal-to-noise ratio is 54 dB on 3.58-MHz input, with power dissipation of 4.6 W. This permits the converter to be operated without forced-air cooling over a range of 0 to 70°C.

TRW marketers are keeping an eye on Sony Corp., which at last fall's Electronica show in Munich announced a 10-bit ADC. The Japanese company says it has been selling the part domestically, but rivals say they see no sign of it. Also, Honeywell Inc.'s Solid State Electronics Division in Colorado Springs, Colo., is known to be nearing introduction of 10-bit ADCs and DACs using its VHSIC Phase 1 1.25-μm technology. Sony and Honeywell officials decline to discuss details.

Bucklen says that video-equipment manufacturers, who now use two 9-bit chips cascaded to get 10-bit resolution, already are showing a good deal of interest in the TDC1020. Not only does the jump to 10 bits have tangible results in better image quality in black-and-white transform contours, he says, but the price is right: at $295 apiece in thousands, the new ADC represents a savings over two 9-bit parts at $125 each because of the additional cost of integrating two of them. He adds that volume production of the 10-bit converter has already started.

–Larry Waller

MICROSYSTEMS

A NEW WAY TO GET MORE FROM ETHERNET

DALLAS

Don't automatically blame the communications link if Ethernet local-area networks are not delivering the promised 10-Mbit/s data transmissions. The problem is more likely to be in the architecture of node-attachment hardware, according to Interphase Corp., a maker of hard-disk controllers. The Dallas company is using lessons from fast computer drives to design a speedy 32-bit VMEbus-based board for Ethernet connection.

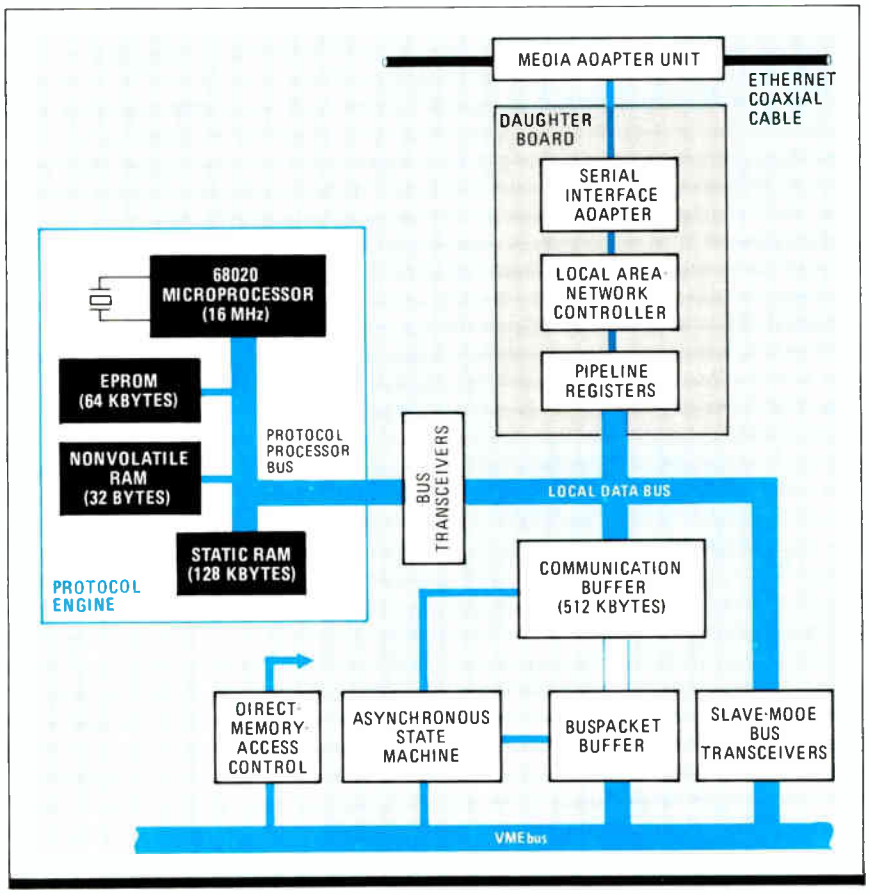
Bit streams—whether they come from hard disks or local-area networks—can make computers sluggish when the disk or LAN controller seizes access to data buses for inordinate periods of time, notes Ernest E. Godsey, product marketing director at Interphase. He says some Ethernet users conclude wrongly that they need faster fiber-optic links or a completely different networking scheme to avoid performance losses due to the LAN's collision-sense multiple-access with collision detection (CSMA/CD) protocol. Instead, the problem is data-movement bottlenecks inside computer nodes, he says.

TOKEN-RING MYTH. Network consultant Harvey A. Freedman of Architecture Technology Inc. in Minneapolis agrees that there is no need for most users to fret about loss of performance due to Ethernet's CSMA/CD, saying it is a myth spread by those promoting token-ring nets. Freedman says the largest factor in Ethernet performance is the amount of protocol processing done on the controller board. "Ideally, you want to divorce the communications aspects from computing aspects" so that the central processing unit handles less of the communications overhead, he says.

Interphase has worked out the divorce on its V/Ethernet 4207 Eagle board, which carries a self-contained protocol-processing engine having a highly partitioned architecture and the 32-bit wallop of Motorola's 16.7-MHz 68020 processor. Godsey believes the board to be the first 32-bit Ethernet platform for VMEbus. Interphase consulted with several technology partners during the development of the board. These system integrators, whom Godsey won't identify, are Ethernet users, and most have concluded that available controller architectures limit throughput to only a fraction of Ethernet's available bandwidth.

"Our technology partners tell us that even with quiescent nodes—meaning no data collisions—they are getting no better than between 56 and 100 Kbytes/s utilization out of the 10-Mbit/s Ethernet-... Many of them are only getting 50 Kbytes/s, which is very, very poor," he says.

Interphase predicts that the $3,500 board, slated to reach the market toward the end of the year, will speed up data flow by as much as 10 times and will help give Ethernet a second chance with some disgruntled VMEbus users. The Eagle prevents system central processors and Ethernet controllers from rendering each other inefficient on the VMEbus, the company claims. What's more, the board utilizes Interphase's



FAST FLYER. The Eagle features a protocol engine partitioned from the rest of the board.

TEXAS INSTRUMENTS REPORTS ON NETWORKING

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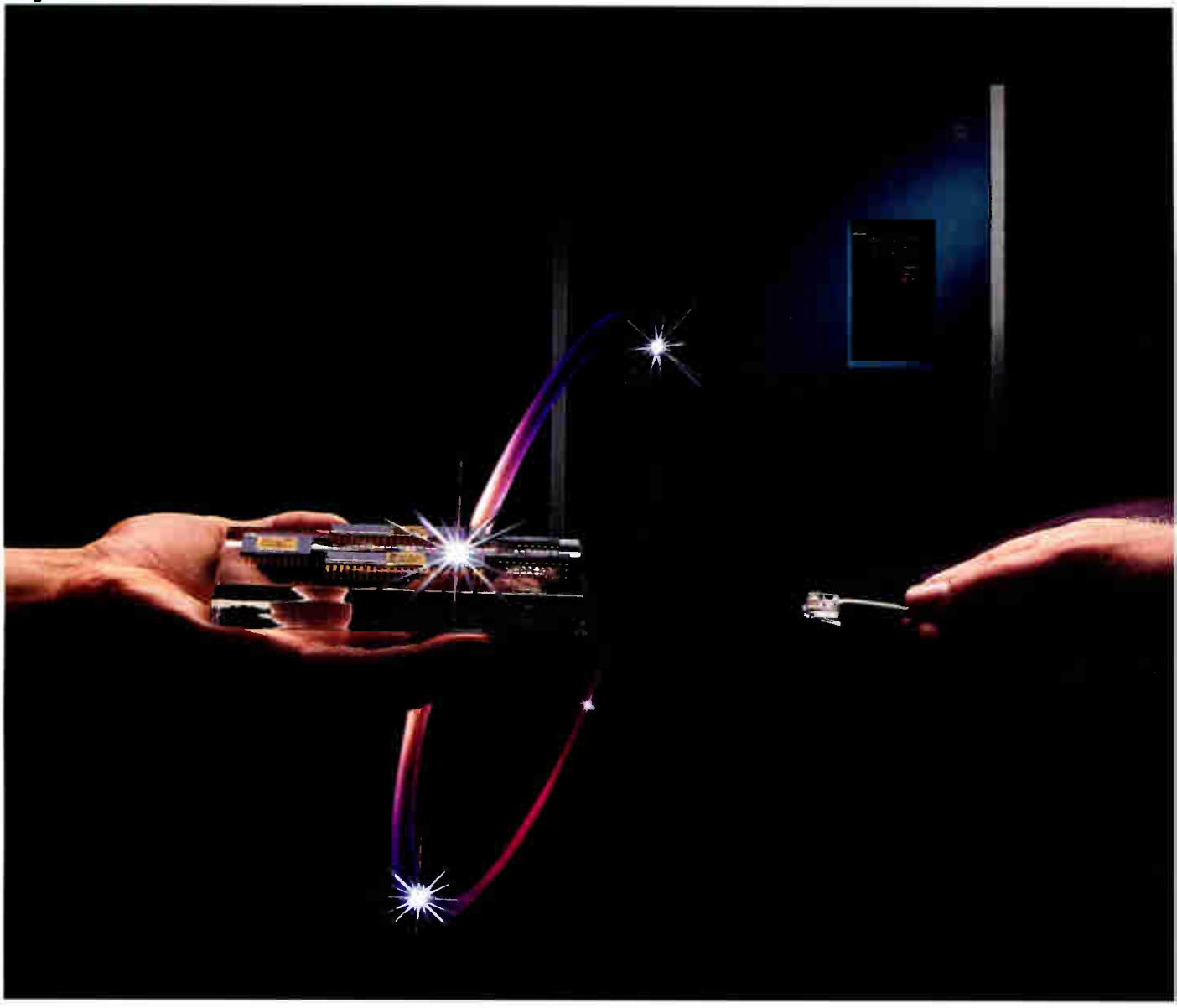

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Howard Salwen,
Chairman and Founder, Proteon, Inc.

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For more information on the broad TMS380 support, turn the page.

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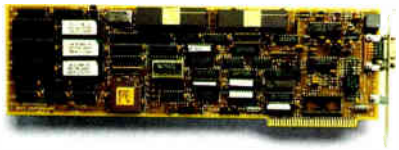

neering debug software with User's Guide, and an interconnect schematic.

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TEXAS INSTRUMENTS

Buspacket interface, which sends preformatted packets across the bus at more than 30 Mbytes/s, more than triple the speed of conventional data streams. The theoretical limit for the VMEbus is 40 Mbytes/s. Interphase first used the Buspacket in its disk controllers [*Electronics*, July 10, 1986, p. 58].

The protocol engine, which has its own dedicated block of fast static random-access memory for downloaded Ethernet protocol programs, is partitioned from the rest of the board by bus transceivers (see figure, p. 54). Thus the 32-bit local data bus, the Ethernet chip set, and the 128-Kbit-by-32-bit communications buffer can handle data to and from the network while the 68020 processes protocols.

In addition, the Ethernet chip set—made up of a serial interface adapter and the 7990 LAN-control integrated circuit from Advanced Micro Devices—is attached to the local data bus with programmable-logic-based pipeline registers. The pipeline registers provide a large buffer for the chip set, which helps to keep the 68020 or the host central processor's access to the 512 Kbytes of communications RAM open.

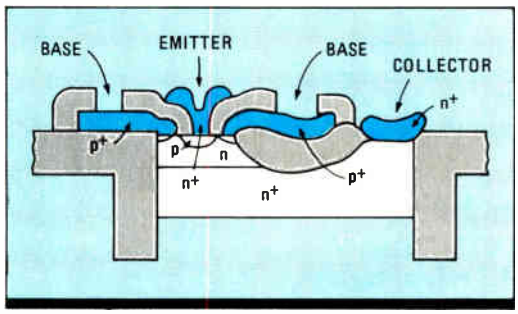
In a direct-memory-access mode, the new Ethernet controller acts as a VMEbus master, making data transfers without host intervention at over 30 Mbytes/s. The board can operate as a bus slave with the system's central processor. The board also features a mixed slave/master mode that saves time by allowing a central processor to read header packets of Ethernet data in the communications buffer. The controller board, using its DMA features, then places data in the correct system memory locations, eliminating one intermediate transfer of data over the VMEbus. *–J. Robert Lineback*

INTEGRATED CIRCUITS

PLESSEY CLAIMS A BIPOLAR SPEED MARK

CASWELL, ENGLAND

Not all the news about semiconductor processing has to come from the U. S. and Japan, maintain the semiconductor folks at The Plessey Co. plc in the UK. To back their claim, they cite the company's Allan Clark Research Centre at Caswell, which has just developed the fastest silicon bipolar process anywhere. What's more, they add, transfer of the process from the labs to Plessey Semiconductors' production facility at Swindon has begun, and the first products could come off the line in early 1988.



RAPID. Trench isolation and two layers of polysilicon are two keys to Plessey's high-speed bipolar process.

Even if it does get edged out by a Japanese or U. S. maker, Plessey's HE process certainly rates as world class. Plessey developed it in the framework of Britain's Alvey fifth-generation-computer project and has another year of Alvey support to tweak the process for full speed. But already divide-by-8 prescalers that have been made with an interim version of the process are achieving toggle frequencies of 6.4 GHz. Ring oscillators checked out at gate delays of less than 50 ps.

At that speed, Plessey outdoes the two best gate-delay times reported so far by chip makers for bipolar circuits: Matsushita Electric Industrial Co., Osaka, described in May at the VLSI Symposium in Japan a technology that achieves minimum delay time of 53 ps/gate; NEC Corp.'s 1st LSI Division, Kanagawa, reported a 52-ps gate delay at the International Electron Devices Meeting in Washington, D. C., last December. Fastest to date, but still in the development labs, is a self-aligned technology from the Atsugi Electrical Communications Laboratories of NTT Corp. that has a basic gate delay of 26 ps.

William Holt, manager of silicon IC development at Caswell, attributes the blazing speed of the HE process—currently implemented with 1-μm lithography—to trench isolation and an emitter structure that's fabricated with two overlapping layers of polysilicon (see drawing). The double-polysilicon structure keeps the emitter/base capacitance low, which in turn boosts the cutoff frequency of the transistors. Holt figures that over the next year the transistor design can be improved enough to boost the performance another 10% to 20%. The cutoff frequency for the final version of the process will be 14 GHz, Holt estimates.

Although still wringing out the process, Plessey already has begun to look at some possible leading-edge products for use in high-speed systems such as computers, electronic switching, and fiber-optic communications. In addition to the 6.4-GHz prescalers, the company has fabricated high-speed gate arrays (240 gates) with gate delays of 80 ps at 8 mW power dissipation and an 8-bit latched digital/analog converter. These will be followed by a high-speed comparator, three types of emitter-coupled-logic (100-K ECL) logic circuits, a complementary current-output dual exclusive-OR/NOR gate, and a limiter. But, Plessey officials insist, there is not yet any firm list of products for them to take to market. *–Arthur L. Erikson*

NETWORKING

HERE COMES TRANSPARENT DISTRIBUTED COMPUTING

NEW YORK

A new style of computing that could wipe out the specter of incompatibility in networks is beginning to fulfill its promise. Called transparent distributed computing, it permits a machine to take over part of a task from a machine of a different make without being told to do so by the operator.

Leading what appears to be the beginning of a tidal wave of such mix-and-match computing is Apollo Computer Inc. and its Network Computing System. On Aug. 10, the Chelmsford, Mass., company and Multiflow Computer Inc. announced that they will connect their systems for transparent distributed computing and market them jointly. This connection closely follows similar Apollo agreements with Alliant Computer Systems and Concurrent Computer Corp.

The new marriage unites two approaches to computing that are really useful together only if they work transparently. Multiflow, based in Branford, Conn., last spring introduced its Trace family of cost-effective supercomputers with a new very-long-instruction-word architecture that can dramatically speed the execution of existing programs [*Electronics*, April 30, 1987, p. 83].

This is accomplished by compiling programs with the firm's special trace-scheduling compiler to take advantage

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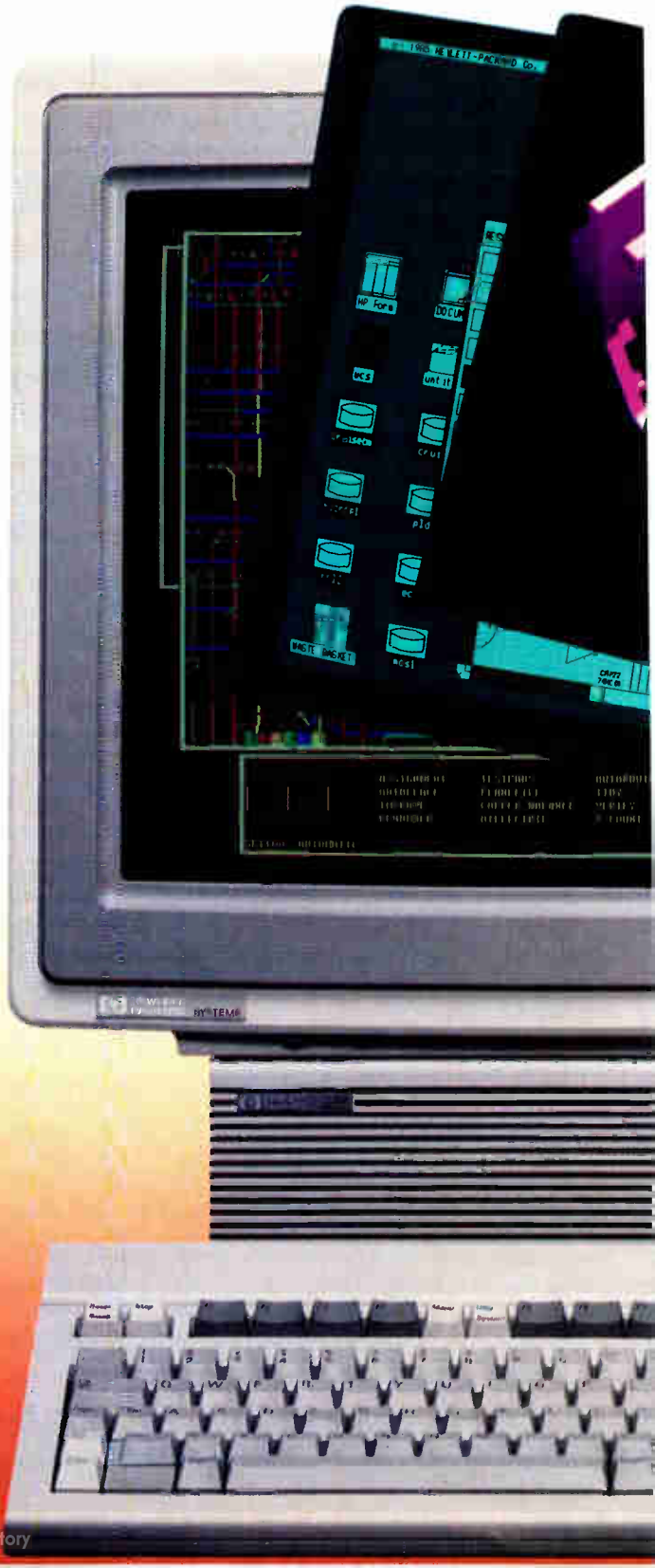

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of the fine-grain parallelism of the machine's very long instruction word. The computers are well suited to big computation-intensive jobs and the heavy numerical-computation parts of applications programs.

On the other hand, Apollo's Domain system of networked work stations and server computers excel at developing programs, running the interactive parts of applications, and providing graphic visualization of computational work.

But two such different computers would not work together at all if not for Apollo's Network Computing System [*Electronics*, March 5, 1987, p. 32.]. The system is basically a standardized programming interface that different computers can use to hand off tasks to one another and to receive results. All of the work is handled compatibly by the NCS interface. In the combined Apollo Domain-Multiflow Trace environment, the Trace supercomputers will be offered as servers for the Apollo work stations.

The first target of the Multiflow-Apollo joint marketing effort is mechanical computer-aided design. The two companies are working closely with leading vendors of mechanical-engineering application programs to provide versions of those applications that will efficiently use transparent distributed computing. Other market areas such as electronic CAD are also on the menu.

–Tom Manuel

SEMICONDUCTORS

SGS-THOMSON KEEPS 2 GATE-ARRAY LINES

CARROLLTON, TEXAS

Two series of CMOS gate arrays that were going to knock heads in the worldwide semiconductor market have been tossed into the same portfolio by the unpredictable paroxysms of international big business. With the merger of SGS-Microelettronica SpA and Thomson Semiconducteurs SA, SGS's ISB9000 and Thomson's 12000 series are suddenly members of the same product line, and the two European chip makers are convinced that their different approaches to dense sea-of-gates arrays can work well under a single market strategy.

There are few similarities. Both series will be made with double-level-metal CMOS, each consisting of 10 base arrays, and will eventually be implemented on the same computer-aided design tools. That's about it. But the differences are the best part of the marriage, say marketing officials at Thomson's Mostek Corp. subsidiary in Carrollton, which will introduce the 12000 series in December.

The 9000 series—developed by SGS's Innovative Silicon Technology SpA in Agrate, Italy—will have arrays with 288 to 20,574 total gates surrounded by 30 to 194 input/output cells. The architecture features "hidden" routing paths leading through functional macrocells that can ease global wiring interconnects across the die. The available channels make the 1.5-μm arrays most suitable for random-logic designs, such as glue-logic consolidation and the control of industrial-automation equipment.

Conversely, Thomson's 1.2-μm 12000 has jam-packed arrays: 8,000 to 128,000 gates. Rows of gates are sacrificed, as needed, for wire-routing paths, making the channelless arrays better for semicustom designs with structured blocks of logic and memory, says Tim Chambers, marketing manager of application-specific integrated circuits at Mostek. That means high-performance data-processing and military chip markets, where semicustom chips are now taking on greater number-crunching duties. "I think we've got the competition sandwiched," exults Chambers.

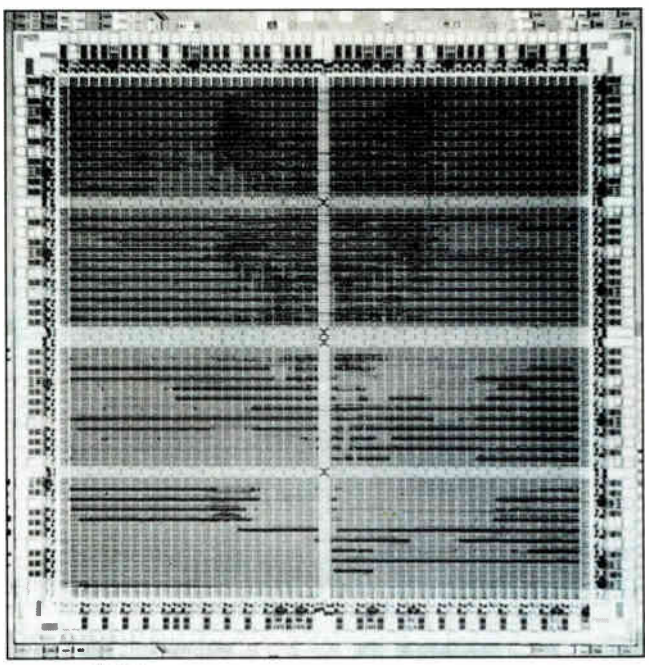
Mostek also has a 12000 processing trick up its development sleeve: an optional third level of metal interconnection. It is expected to boost gate use to 90% from the initial 50% range of the double-level process. Triple-level metal is also aimed at moving sea-of-gates arrays into semicustom markets served mostly by standard cells, which can usually pack more onto smaller dice.

The semicustom families borrow from two different camps in the emerging sea-of-gates, or channelless-logic-array, movement. SGS's Innovative Silicon Technology licensed its channelless architectural concept from California Devices Inc. in San Jose, Calif. The approach folds global interconnections onto the active gate area via available empty area. The availability of interconnects without using up a lot of cells makes this approach ideally suited for random logic, says Chambers. The 9003 will be the smallest array in the series: 288 gates with 95% usable, and 30 I/O pads. The top of the series will be the 9205 with 20,574 gates—60%, or 12,344, usable—and 194 I/O pads. The 9000 series is expected to have typical gate delays of 700 ps for a two-input NAND.

Meanwhile, the 12000 series has been developed along the lines of a Channel-Free architecture introduced in 1985 by LSI Logic Corp. of Milpitas, Calif. The arrays have no predefined first-metal routing channels. After macrocells are placed, first-level interconnection is routed by software, running metal over selected columns of cells. This way, silicon real estate is not wasted on predefined but unused routing channels.

However, the Mostek design adds a number of twists to the standard concept. Chief designer Charles Waggoner says the key improvements include I/O cells that are easy to customize; slew-rate control over driver signals in both up and down directions; a 1.2-μm CMOS process producing high-performance p-transistors; multiple "hit" points for cells that improve software-routing of design; and the use of efficient cutoff-transistor isolation over oxide-isolation techniques.

The smallest array in the 12000 series is the 12008, sporting 8,000 gates—3,200 usable—and 80 I/O pads. The densest array will be the 12128, containing 128,000 gates—51,200 usable—and 320 I/O cells. The double-level-metal process, called HCMOS III, yields typical internal delays of 282 ps with two-input NAND gates. *–J. Robert Lineback*



TOGETHERNESS. Thomson-Mostek's new sea-of-gates array finds itself in the same catalogue as an erstwhile rival from SGS.

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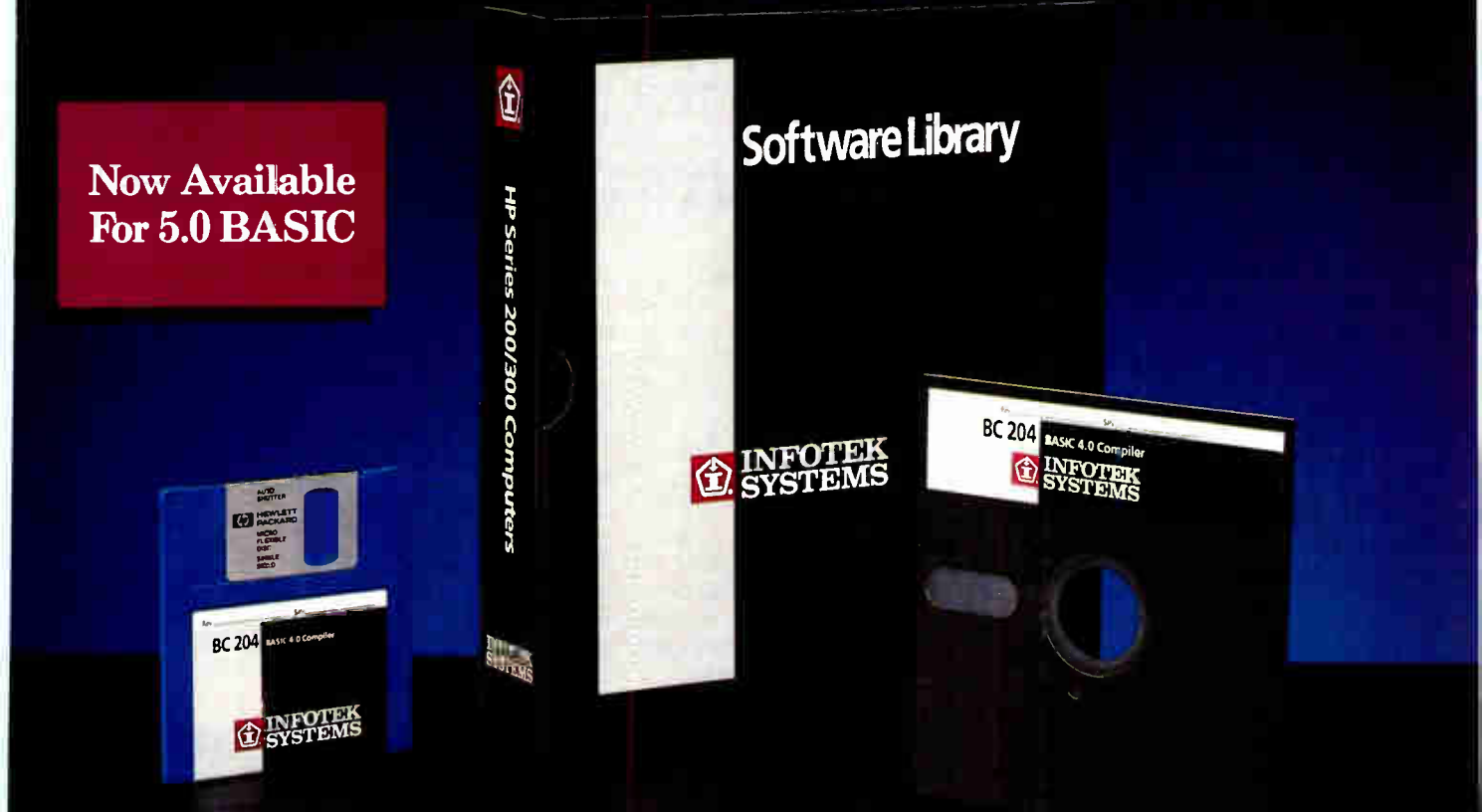

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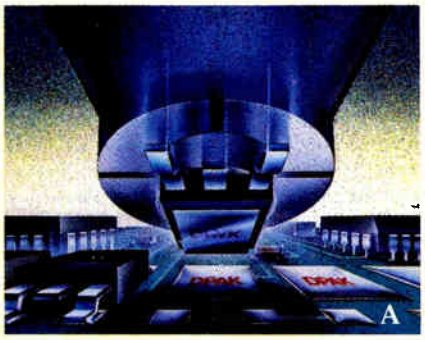

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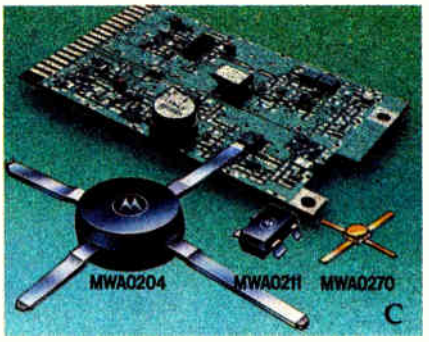
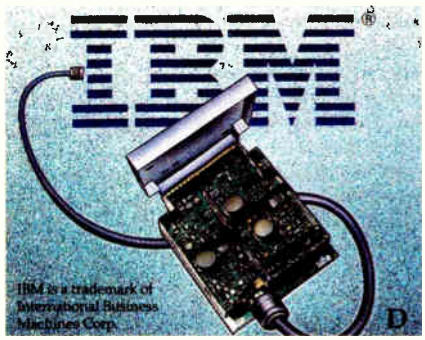


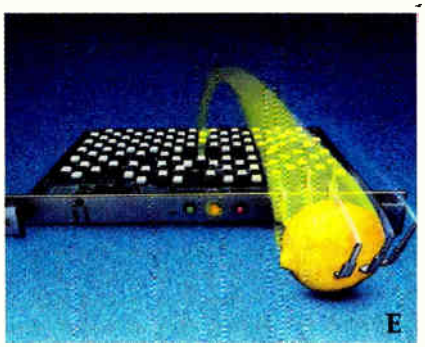
Monolithic RF amplifier now available three ways.

Have it your way in packaging with the MWA-series of wideband RF amplifiers for industrial/commercial use up to 3 GHz. Besides the recently-introduced MWA0204 MACRO-S stripline and MWA0211, SOT-143 SMD devices, the new MWA0270 is available in a 70-mil ceramic metal hermetic package for extreme environmental applications. It's fully cascadable, provides 50 Ω input and output impedances and 12 dB typical gain at 500 MHz. A further derivation in all three packages, the MWA03 series provides similar gain and noise figure specs but with higher output power and better linearity.



RF broadband module implements IBM PC nets.

This full-duplex, continuous mode frequency shift keyed transceiver (CPSFK) looks complicated. Just remember it operates somewhat like an A-D/D-A converter but in addition provides all RF functions needed to implement the modems on IBM PC networks. In significantly less space and lower price than others, saving space on the network adapter board. The MHW10000 provides high spectral purity (it doesn't spill over onto other channels from either the T-14 transmit- or J-receive modes), it's only 7.5" square and ¼" thick, far less than comparables. Other frequency bands are available.



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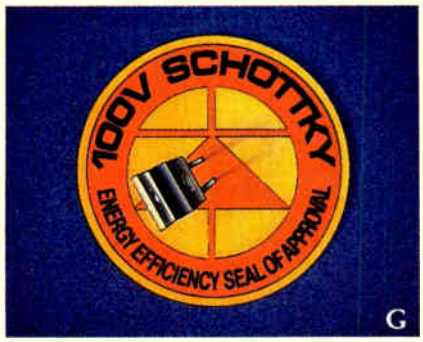
Design News



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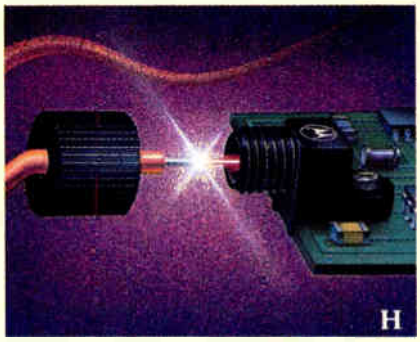

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Max. Clock Freq. (typ) J/K F•F (C_L = 15pF)	60MHz	45MHz	20MHz	2MHz
Quiescent Power Diss. (typ) (GATE)	0.01 μW	8mW	0.01 μW	0.01 μW
Noise Margin V_{IH}(min)/V_{IL}(max)	3.5V/1.5V	2.0V/0.8V	4.0V/1.0V	3.5V/1.5V
Output Current I_{IOH}I (min)/I_{OL} (min)	4mA/4mA	0.4mA/4mA	0.36mA/ 0.8mA	0.12mA/ 0.36mA
Op. Volt. Range	2-6V	4.75-5.25V	2-8V	3-18V
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PROBING THE NEWS

COMING AT ITC: LANs THAT LINK TEST WITH DESIGN AND FACTORY

SIMULATORS DRIVE TEST PROGRAMS; ATE GEAR HOOKS INTO DATA ANALYSIS

by Lawrence Curran and Paul Angiolillo

Local-area networks are taking an increasingly important role in design, test, and test-data analysis, judging by the products on display at the International Test Conference, to be held Sept. 1-3 at the Sheraton Washington Hotel in Washington, D. C. Perhaps most prominent among the new network-oriented technology is the thrust toward closer integration of testers with the simulation models developed during design—data that describes the devices and boards to be tested.

ITC will also offer evidence of an industry shift away from proprietary networks and toward industry standards, notably Ethernet, as a vehicle to integrate computers from multiple vendors into ATE networks. There will also be a number of new products and enhancements announced as vendors look for fresh sources of revenue during one of the most devastating recessions in the ATE industry. The market for board testers has dropped from more than $640 million in 1984 to about $540 million last year; yearly sales of semiconductor testers declined from just over $1 billion to around $850 million during the period.

That three-year slump most recently has caused GenRad Inc., Concord, Mass., to drop out of the VLSI test system business to concentrate on board testing [*Electronics*, Aug. 6, 1987, p. 126] in the wake of heavy losses attributable to the discontinued Semiconductor Test Division in Milpitas, Calif. Teradyne Inc., GenRad's neighbor and competitor in Boston, has also felt the sting, reporting two consecutive quarterly losses this year—the company's first losses in 16 years.

Both companies will be looking for better things at ITC—GenRad with a low-end version of its recently introduced GR2750 combinational (functional and in-circuit) board-test system [*Electronics*, June 11, 1987, p. 59] and Teradyne with links to both the design and factory-control realms.

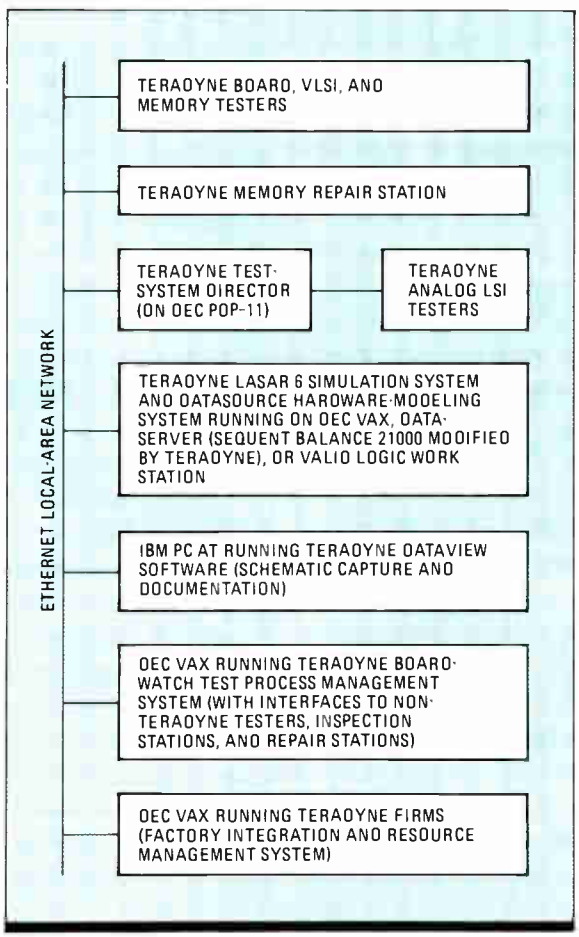
Several vendors are squarely in synch with the ITC theme: "integration of test with design and manufacturing." Michael Bradley, Teradyne marketing manager for analog VLSI test systems, says that while discussions about and support for integrating design, test, and factory management abound, "We're doing it now and will demonstrate that [integration] at the show."

In a first-time demonstration, Teradyne's A500 analog VLSI test system, introduced in January [*Electronics*, Jan. 22, 1987, p. 55], will be the centerpiece in an Ethernet that links the company's Lasar (logic automated stimulus and response) simulator, the tester, and factory management via Teradyne's Firms (factory integration and resource management system). Bradley says the test vectors for a digital device will be generated using Lasar and transferred to a work station on the A500 for conversion into a test program. The device will be tested, and test data will then be logged into Firms for analysis.

Another aspect of Teradyne's ITC demonstrations also echoes the conference theme of network-based integration (see figure, left). The company's Boardwatch software system centrally stores and controls test-job plans, and collects and analyzes board-test data to develop statistical and process-control profiles. Boardwatch uses Ethernet-based DECnet for communications and VAX systems from Digital Equipment Corp.

One of three new Boardwatch modules to be shown at ITC is called Testlink, an interface module that allows for the first time inclusion of non-Teradyne ATE equipment in the data collection and analysis loop. Steven DiAntonio, Boardwatch product manager, says the MicroVAX-based interface will link three Teradyne L200-series test systems in a network that uses standards, instead of a proprietary network.

An approach that allows simulator-generated test vectors to be translated automatically into test programs will be shown by Zehntel Inc. of Walnut Creek, Calif. The product is called Simlink, which will be running on the Zehntel 850 F/I combinational board tester. Simlink runs on Zehntel 850 and 875 test systems and on the IBM PC AT, says Koorosh Nazifi, product manager in the automation systems divi-



INTEGRATION. Teradyne can link design, test, repair, and other functions via a nonproprietary Ethernet network.

sion. It is particularly useful for speeding up the generation of test programs to test application-specific integrated circuits on a board (see figure, right.)

To date, Simlink will accept test vectors from GenRad's Hilo simulator and Daisy's Design Logic Simulator for automatic conversion to test programs for the Zehntel testers; Nazifi says Simlink will support more simulators soon.

Also alert to the need to speed test-program generation, Hewlett-Packard Co. will take the wraps off software that compiles CAD data into test programs for the HP 3065 family of board testers. The HP EDS/3065 test-program generator takes input from the HP 74200 electronic design system. The software then "writes a compilable test that can be ported directly to the 3065 series," says Rick Robinson, applications engineering manager in the manufacturing test division, Loveland, Colo.

NEXT GENERATION. In addition, the 3065 will provide the first board-test platform for what Robinson describes as "a next-generation test generator." The software was developed by Test System Strategies Inc., Beaverton, Ore. It will analyze simulator output from various design work stations, including Apollo, DEC VAX, and Sun Microsystems, and tell users if models from those simulators will run on the target test system.

Bruce Hadley, manager of marketing operations at Test System Strategies, explains that the company's Test Development Series software accepts input from just about any simulator, translates the simulator model to a standard events format, and will automatically generate a test program for the target test system. It will alert the designer to any incompatibility between the simulator and target tester, such as a mismatch in timing, so that the designer can specify a different tester or modify the design.

The need to connect ATE to computers—work stations or larger machines—other than those incorporated into the ATE hardware itself has spurred several vendors to demonstrate their nonproprietary networking schemes. LTX Corp., Westwood, Mass., will use an Ethernet LAN to download test vectors from a VAX system to an LTX 90 tester equipped with the DX90 digital extension, which allows the tester to accommodate mixed-signal devices.

The LTX Ez-net configuration allows for off-line programming and real-time data collection from test systems via a VAX system. LTX will also demonstrate Ez-net's versatility by linking an Apollo work station, a VAX, and an LTX tester.

Axiom Technology Corp., Newton, Mass., will demonstrate the AT100 linear and mixed-technology device tester linked in a LAN to different computer architectures for the first time. The Ethernet-based LAN will link Sun, IBM, or VAX systems with the AT100. With a Sun 3 work station in the loop, the digital pattern files generated on the work station will be moved to the tester and incorporated into test programs. One AT100 will be shown testing telecommunications devices, and another will mark the first demonstration of the AT100's smart-power test capability.

The ability to connect multivendor hardware in an Ethernet-based test system network will also be featured by Megatest Corp., San Jose, Calif. The company's hardware previously communicated with other vendors' computers, but now it can incorporate them into the testing process more thoroughly. Megatest will demonstrate a network at ITC linking one of its testers, a Sun network file server, and a Sun work station. While the tester is executing test programs, one user can be working—performing graphics-enhanced debugging, for example—at the work station.

Use of the file server allows users to work transparently on different nodes on the net, executing programs at any of three locations while accessing other computer resources on the network.

Links to simulators and multivendor nets will pervade ITC, but attendees can also expect to see important product announcements. Close on the heels of its introduction of the GR2750 board-test system, GenRad will add another platform to what eventually will be a broad family of testers. The GR2750 combines functional and in-circuit board testing; the GR2751, to be unveiled at ITC, will be the low-end family member, devoted to in-circuit testing only.

John Zapf, director of marketing for the electronic manufacturing test group, says the 2751 is intended for customers who have historically performed in-circuit testing "but who recognize a need to be able to migrate to functional testing. They can get into high-performance in-circuit testing on a platform that will allow them to grow—to add functional testing later." Although pricing for the 2751 isn't set, Zapf says it will be about 20% less than the 2750, which costs $600,000 to $1 million.

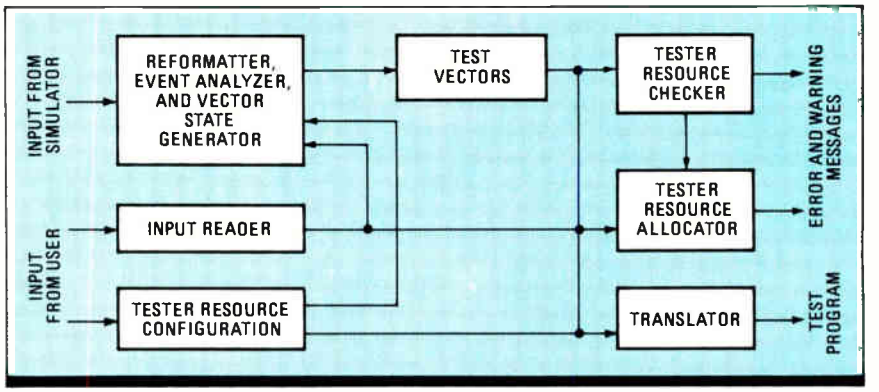
Another new system—the Genesis II memory tester from Megatest—will bow at ITC. This high-performance memory tester will sell for about half the price of competitive systems and will test nonvolatile memory devices, the company says.

700 SERIES. The ATE operation of Schlumberger Technologies (formerly called Factron/Schlumberger), Latham, N.Y., will introduce the series 700S board-test system, which becomes the basic platform in the 700 series. The 700 series ranges from a simple low-profile digital in-circuit tester to a high-pin-count combinational tester with up to 28 application-specific instrument modules. In the 700S, a DEC VAXstation 2000 replaces a MicroVAX II front end and allows test engineers to bring test programs on line faster from an off-line VAX.

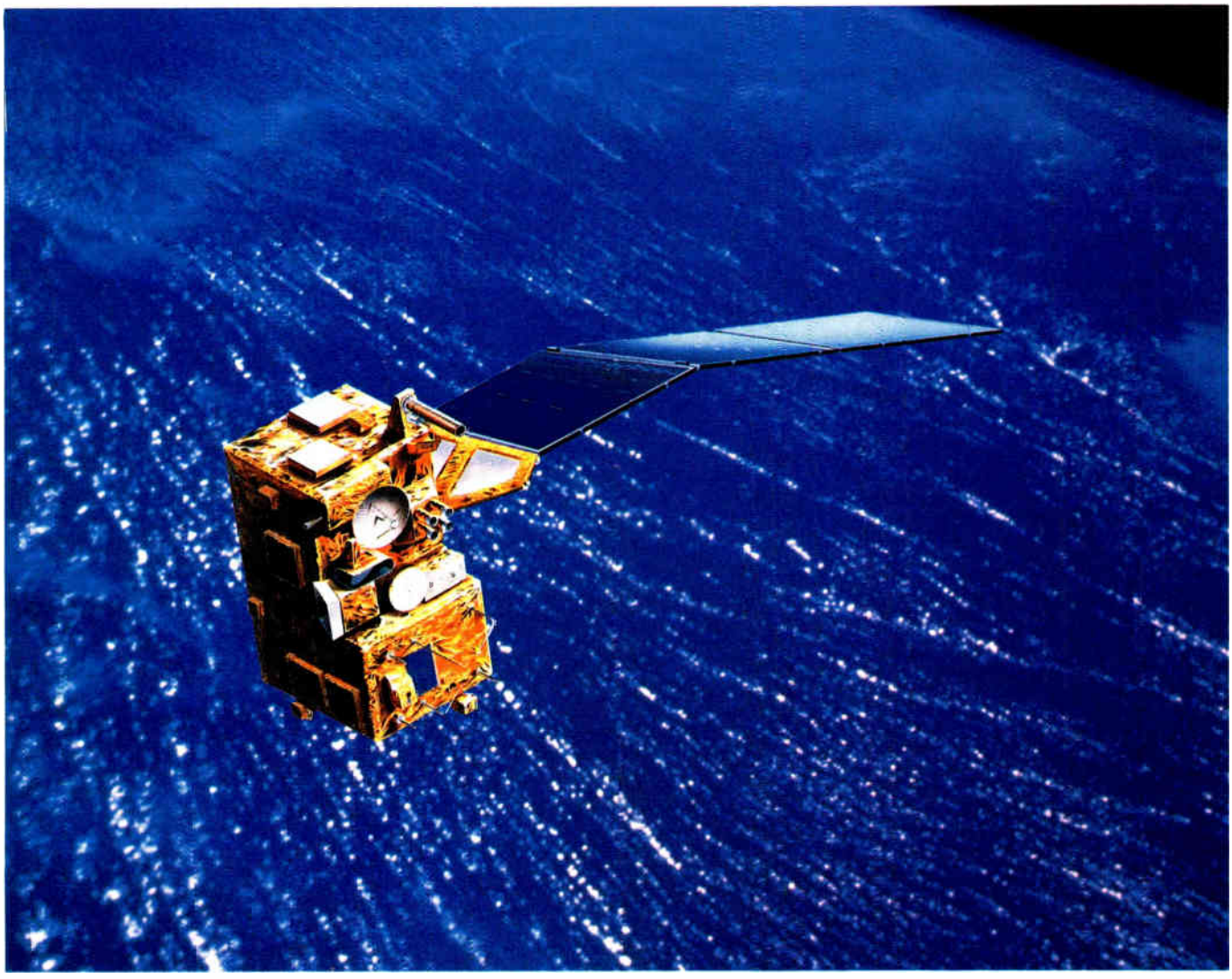
Enhancements are coming from several companies, including Attain Inc., Milpitas, Calif., and Tektronix Inc., Beaverton, Ore. Attain's 2000-series analog and mixed-signal device testers will get three new modules to test smart power devices. A high-power unit covers ±300 V dc at ±20 A. A high-voltage extension goes to ±1,350 V at ±2 mA, and a high-current module hits 50 A at 0 to 7 V.

The power modules can be turned on and off rapidly—at rates of better than 10 V/μs and 10 A/μs—and do not encumber the test head with bulky bolt-on circuitry, as is often the case with power add-ons, says James Clouser, Attain's chief financial and operating officer.

Tektronix has doubled the speed of its LT-1000 VLSI logic test system, first introduced at Semicon West in May as a 50-MHz system. The frequency has been increased to 100 MHz because "devices are running at higher speeds in end-user applications, and 100 MHz gives us some headroom," says product manager Alan Whiteside. Tek will also demonstrate the DAS-9200 digital analysis system, a logic analyzer, in ASIC prototype-verification and board-test configurations. □



SOFTWARE LINK. Zehntel's Simlink produces test programs based on simulator data.



JAPAN LAUNCHES INTO A NEW ERA IN REMOTE SENSING.

Japan's first Marine Observation Satellite-1 (MOS-1) is now circling around the globe, covering its entire surface in 17 days from 909km up in space.

With three sensors aboard, the new remote sensing satellite beams back an enormous volume of data on diverse aspects of the sea, land and atmosphere. One of the sensors, MESSR (Multispectral Electronic Self-Scanning Radiometer) senses colors of the sea and land, and recognizes surface features 50m by 50m, utilizing CCD (Charge-Coupled Device) image sensing devices. The MOS-1 is expected to contribute greatly to fishery, agriculture, forestry, resources finding and environment preservation worldwide.

As the prime contractor to the National Space Development Agency of Japan (NASDA), NEC was engaged in system design, system integration and manufacture of key subsystems including major bus subsystems, the MESSR sensor, the DCS (Data Collection System) repeater, ground receiving system and image data processing system.

With more than 30 years of experience in space development, NEC has been involved, as a prime contractor or system integrator, in 23 of the 37 satellites placed in space by Japan.

NUMBER 138

DIGITALIZATION EXPANDS IN LATIN AMERICA.

In keeping with the ultimate goal of a global ISDN, telecom authorities in Latin America are stepping up their digital network programs.

Telecomunicações Brasileiras S.A. recently awarded NEC do Brasil S.A. a giant order for state-of-the-art digital equipment. It includes NEAX61 digital switching systems (360,000 lines), 5GHz 140M-bit digital microwave communication equipment (1,800 sets), fiber optic communication equipment (200 sets) and PCM transmission equipment (1,300 sets). Most of the systems are to be produced locally with delivery starting this year.

Meanwhile, Empresa Nacional de Telecomunicaciones, Argentina has awarded PECOM-NEC S.A. a contract for NEAX61 digital switches (300,000 lines) and PCM transmission equipment to be installed in the metropolitan and northern areas of Argentina. Local production is scheduled to begin soon. In 1982 NEC constructed a 320-km fiber optic digital telephone system, interconnecting 6 tandem exchanges and 60 telephone offices in the metropolitan area.

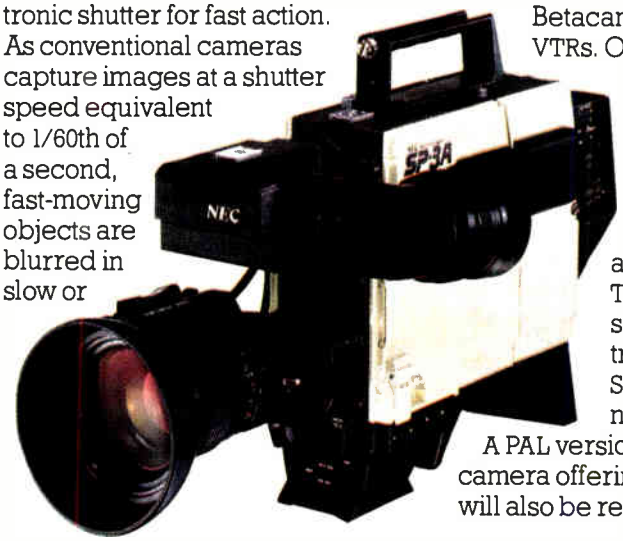
NEC is also contributing to the 5-year telecom digitalization project by Compañía Anónima Nacional Teléfonos de Venezuela by supplying NEAX61 digital switches to 97 exchanges in Maracaibo, Puerto La Cruz, and other important areas. For interconnection of these exchanges NEC will supply a 200-km fiber optic communication system.

As one of the world's leading suppliers of digital exchanges, microwave and fiber optic systems, NEC is helping to further the digital revolution throughout the world.

NEW CCD CAMERA STOPS ACTION ELECTRONICALLY.

The trend in color cameras for broadcast use is irrevocably "solid-state". CCD cameras are more compact, dependable and durable than tube types and have no comet tails and burn-in when shooting extremely bright objects.

On top of these inherent benefits, NEC's new SP-3A CCD Color Camera has an exclusive feature—the electronic shutter for fast action. As conventional cameras capture images at a shutter speed equivalent to 1/60th of a second, fast-moving objects are blurred in slow or still playback on VTR. To remedy this problem, our SP-3A stops the action electronically at 1/60th to 1/2000th of a second, offering precise, clear-cut images.



The SP-3A uses 3 new CCD chips that are anti-smear and -blooming—two for the green channel and one for the combined red/blue channel. This dual green system provides much higher resolution and sensitivity than the conventionally-structured RGB system.

The new CCD camera displays widespread versatility. Besides standalone use it forms an efficient shoot/record system with integral Betacam, MII or 8mm-format VTRs. Options are available for multi-core or triax remote control.

Users' acceptance of this versatile new camera has been remarkable. NBC, a major U.S. TV network, recently sealed a five-year contract to purchase the SP-3A for electronic news gathering.

A PAL version of NEC's CCD color camera offering broadcast quality will also be released.

WORLD'S FASTEST ECL GATE ARRAYS.

The performance of high-speed silicon logic LSIs is rapidly accelerating. NEC's new ECL-4 gate arrays are the swiftest in the world with a 100ps basic gate delay or 220ps fully loaded.

Combining unprecedented speed and flexibility, the ECL-4 family includes the μPB6312 with 1,200 gates (400 Full-adders) and the μPB6303 with 600 gates (200 Full-adders). Both offer 100K or 10KH interface options and ample I/O up to 108 pins.

NEC's ECL-4 gate arrays are available in a choice of 72- or 132-pin PGA packages, and operate in ordinary forced-air-cooling environments since sophisticated heat sinks are standard.

NEC offers 61 internal macros and 33 I/O blocks plus complete CAD tools. The ECL-4 family should hasten the development of speed-oriented computers, graphic terminals, LSI testers and telecom equipment.

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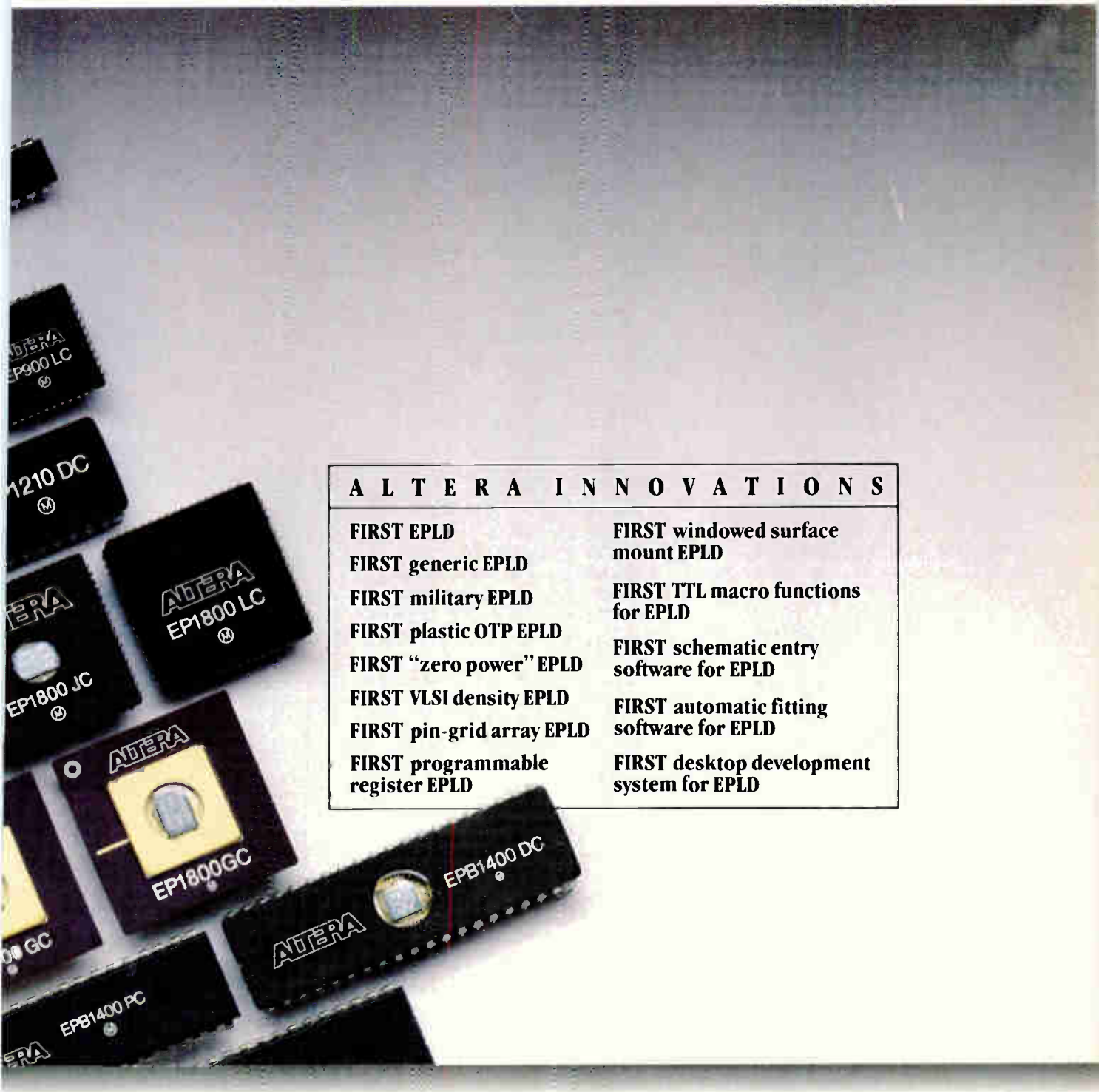

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INTERNATIONAL NEWSLETTER

NEC TURNS TO SOFTWARE TO BLOCK SEIKO EPSON'S CLONE

NEC Corp. is fighting back against Seiko Epson and its clone of NEC's PC-9801, Japan's best-selling personal computer. The Tokyo company has started to sell its MS-DOS package for the PC-9801 separately from application packages and plans to produce a future MS-DOS version with a guard program that will prevent its use with clone personal computers. Seiko Epson, of Suwa, Japan, released its PC-286 three months ago, setting off a furor at NEC [*Electronics*, May 14, 1987, p. 49]. Even though the PC-286—the first and only clone of the PC-9801—can run only about 400 of the nearly 6,000 software packages available for NEC's PC, sales have been brisk: the company originally hoped to sell 10,000 machines in the first year, but reached that level after just three months. Fighting to protect itself, NEC says all future application software will include an embedded guard program that will prevent its use on anything but a NEC machine. □

PHILIPS PUTS A COLOR LCD INTO ITS UPCOMING POCKET TV

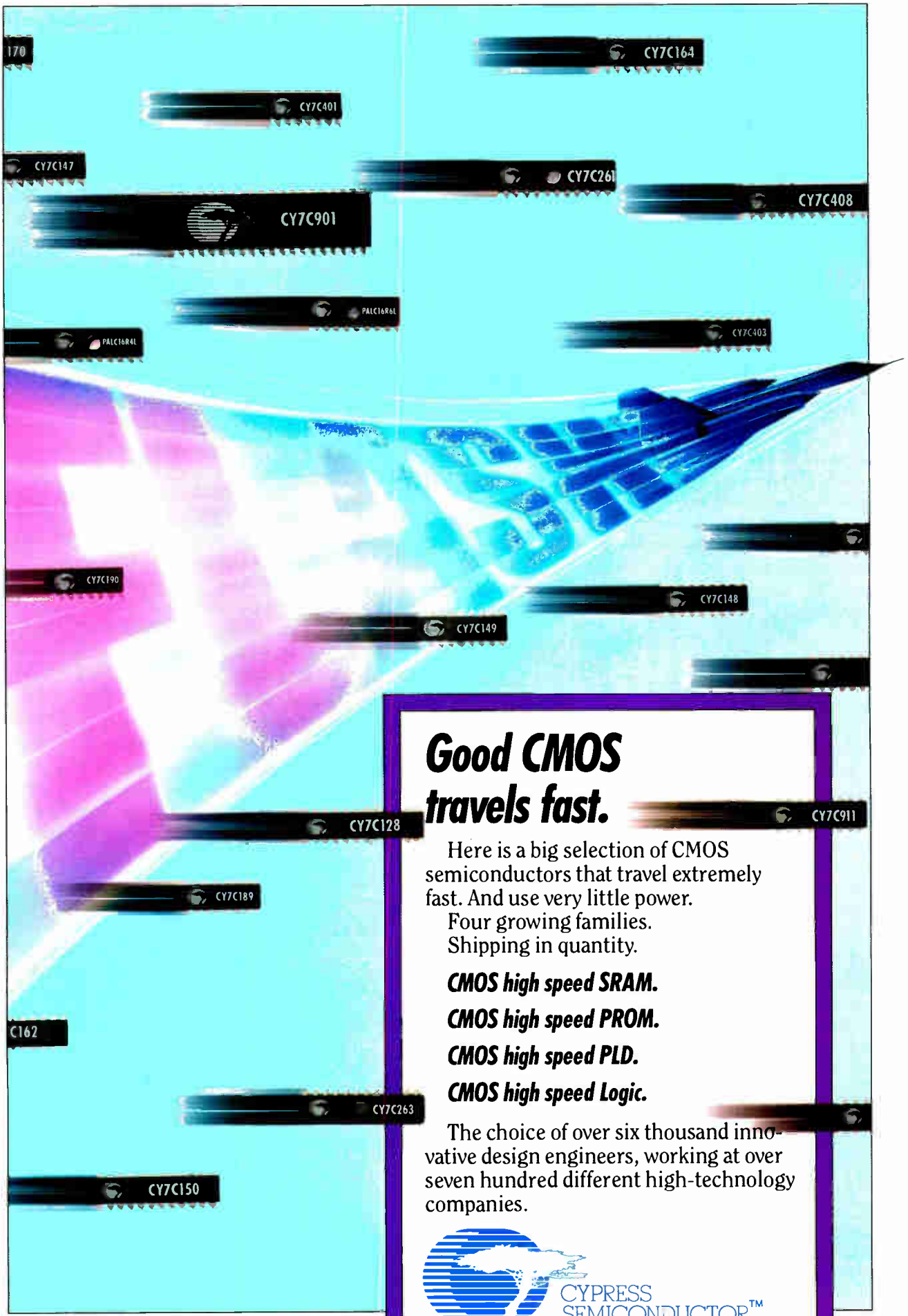
Philips of the Netherlands will introduce a pocket TV later this month that could be the world's first to use a color liquid-crystal display. Based on technology acquired from Japan's Sharp Corp., the 3-in. display is only 2.5 mm thick, but it doesn't sacrifice picture quality, Philips says. The screen has 106,752 pixels organized in a 278-by-384-pixel matrix. Backlighting ensures high picture quality but can be turned off to save power under battery operation. Without backlighting, the set consumes only 1.3 W and can run for 5.5 hours on the built-in battery. Turning on the backlight boosts dissipation to 2.5 W. The thin-film-transistor technology Philips is using holds out promise for larger LCD screen sizes too: TFT technology allows transistors to be integrated into large panels, meaning display size is virtually unlimited. □

TAIWAN SEMICONDUCTOR SETS ITS SIGHTS ON THE U. S. MARKET

Taiwan Semiconductor Manufacturing Corp. is getting ready to establish a U. S. beachhead. The foundry-services company, a joint-venture between Philips of the Netherlands and the Taiwan government, will set up U. S. offices in the San Francisco and Boston areas, says vice president of marketing Steve Pletcher. Dubbed Fab Centers, the offices will be manned by test, process, and design engineers who will mesh customers' designs with TSMC's 1.5-, 2-, and 3-μm CMOS processes. Chairman Morris Chang, meanwhile, reports that the foundry is getting "good yields"—between 30% and 40%—on its most complex products, five peripheral logic chips for clones of IBM Corp. PC ATs. Yields are in the 60% range for some less complicated controller chips, he says. □

MOTOROLA RADIO SYSTEM GETS A LIMITED OK FROM JAPAN

Motorola Inc. will get a share of the market for multichannel-access radios in Tokushima, a city in the Shikoku district, an island in western Japan. The Ministry of Posts and Telecommunications has given preliminary licenses to 40 area businesses to use Motorola's MCA radio system, a small-capacity system with eight channels, starting in October. Motorola's system, which is not compatible with Japan's current MCA radio systems, will be used exclusively by those businesses and will operate only within 30 km of a stationary relay station operated by Nippon Motorola Ltd. of Tokyo. Current Japanese MCA radio systems, supplied by NEC, Mitsubishi, and Matsushita, use 16 channels and share compatible relay stations. Motorola's MCA radio system cannot share relay stations, but it can let users access public telephone networks, in effect working like a cellular mobile telephone. □



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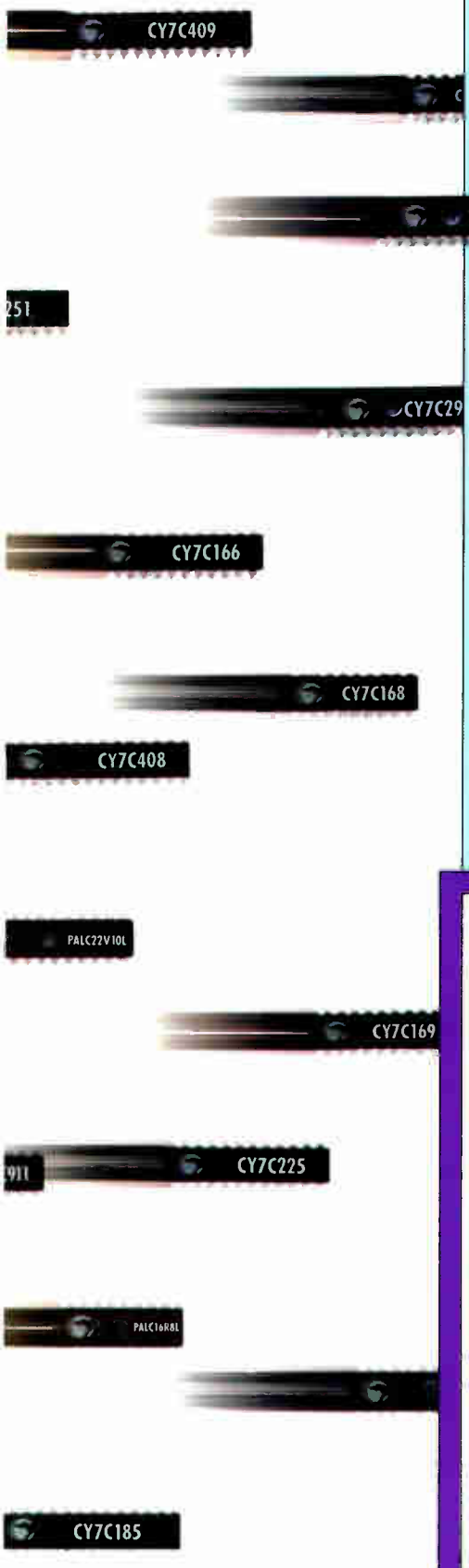

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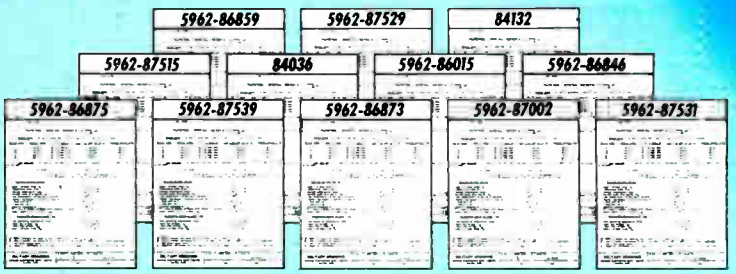

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That capability is paying off. We have twelve products certified or pending certification, with many, many more scheduled in the near future.

And we intend to see that they become JAN slash sheets as quickly as possible.

Our growing list of SMD parts means you can take advantage of the enhanced quality rating (MIL-HBK-217) of SMD product more and more, as you design with Cypress products.

Is it important to you to have a certain part available under the SMD program? You won't find a more cooperative or better equipped vendor to help you than Cypress Semiconductor.

Military quality is not a sideline at Cypress.

Our automated U.S. plants were designed to pass the stringent JAN requirements.

And our products are designed to pass the most stringent JAN performance demands, 100%.

Our wafer facility is a Class 10 manufacturing environment, and even our assembly areas are clean rooms.

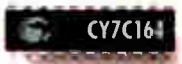
Our flexible packaging automation systems let you take advantage of the LCCs and flatpacks you want, easily. And our 1.2 and 0.8 micron processes deliver record performance.

A few military programs benefiting from Cypress Semiconductor CMOS technology:

AHEP	AL-131	ALQ-141	ALR-56C	AMRAAM
ANDVT	AP-102	ASR-9	AWACS	B-52
C-17	E2-C	EA6B	EMSP	F-111
F-14	F-15	F-15E	F-16	F-18
HAWK	ICNIA	JTIDS	LANTIRN	MAVERICK
MILSTAR	MILVAX	Patriot	Space Shuttle	
Sparrow	V22			

64K SRAM: 25ns!

65,536x1 Static RAM 25ns



16,384x4 Static RAM 25ns

16,384x4 Static RAM w/Output Enable 25ns

16,384x4 Static RAM Separate I/O 25ns

16,384x4 Static RAM Separate I/O 25ns

8192x8 Static RAM 35ns

8192x8 Static RAM 35ns

If you're looking to crank up the clock in your system, here is the SRAM speed and capacity you need.

We offer a variety of configurations—nibble-wide, bit-wide, byte-wide, and separate I/O—to give you *choice*.

Seven different 64K parts, all TTL-compatible, all with the lowest active power requirements available at this level of performance, and all with automatic power down.

And, our 0.8 micron process means very small die, so you can take advantage of board-saving skinny DIP packaging on *any* configuration. In fact, only Cypress offers high performance 8Kx8 SRAMs in 300 mil DIPs.

The net result: High performance, higher density, lowest power, and a cooler system, for greater reliability.

Who uses Cypress Semiconductor circuits? Anyone who needs performance.

One example: Workstations with high computational demands and high throughput graphics.

Virtually every high performance engineering workstation company uses our high speed, low power CMOS circuits.

A program that extends 38510 conformance to every part at Cypress, commercial or military.

And that program goes on to include:

Comprehensive Reliability Monitoring programs. . . .

Extensive Commercial Assurance screening. . . .

Military Product Assurance Programs, including Standard Military Drawings, JAN facility certification, and JAN parts. . . .

Total Individual Control, giving any individual the *obligation* to halt a design or process if quality is threatened. . . .

And Top-Down Quality Training, an ongoing series of management sessions ensuring that quality—conformance to specifications—always has top share of mind.

As a result, the Assembly Traceability Code marks the commitment of top management at Cypress Semiconductor to provide the highest quality in the semiconductor business. To have the programs in place to constantly drive toward Zero Defects.

Do your other IC suppliers offer you the same assurance?

Look for an Assembly Traceability Code on all the circuits you see in your own product, and see just how fully committed your IC suppliers are to quality, and to accountability.

Quality is not an abstract or merely esthetic issue. Quality is a *measurable* conformity to standards that translates into measurable benefits for our customers.

So as long as you see that Assembly Traceability Code, you see the most visible evidence of our aggressive quality program. And our commitment to *your* product's quality.

128K PROM: Reprogrammable!

Yes, the photograph you see is actual size. Our CMOS processing means we can pack a full 128K into board-saving 300 mil-wide packaging.

The benefits continue: 45ns gives you the speed you need for highest performance firmware. And, of course, CMOS means very low power. Combined with our power-down standby mode, you enjoy a significant power savings for each and every part you install, compared to any other non-volatile, high speed memory.

16,384x8 Reprogrammable Power Switched PROM 45ns

16,384x8 Reprogrammable PROM 45ns

Now, let's talk *reprogrammability*. A windowed part can save you time and trouble in the development lab.

And windowed parts can save you considerable time and trouble in production, protecting you from expensive inventory obsolescence when firmware changes.

And even if you don't pick a windowed package, you still benefit from the technology. The floating gate process lets us test each and every memory cell on each and every part we ship, so you get the convenience of the highest incoming quality available.

64x8, 64x9 FIFOs: 35MHz!

Our dual-port SRAM technology sets these FIFOs apart from all others.

By combining this SRAM technology with control logic and a read and write pointer, we've virtually eliminated the bubble-through delays associated with traditional FIFO parts.

The delay for input data to appear at the output is simply the time required

Cascadeable 64x8 FIFO 35MHz

Cascadeable 64x9 FIFO 35MHz

to move a pointer and propagate an Output-Ready (OR) signal.

You can tie multiple FIFOs together on a common bus to increase word width. And you can increase depth with minimal performance penalty, because our FIFOs are cascadeable.

The parts deliver full 35MHz performance—up to 40% faster than competing cascadeable FIFOs.

And you get it all with the low, low power of our CMOS technology.

The Cypress Semiconductor quality advantage: The Assembly Traceability Code.™ *

Unique to Cypress, the Assembly Traceability Code is written proof of our unmatched quality and measurability commitment.

You'll find the ATC on every Cypress Semiconductor part.

Find that code on any other IC. If you can.

Here's why that Assembly Traceability Code is of measurable benefit to you:

Quality, according to Philip B. Crosby, is tangible.

Quality is *conformance to requirements*.

In the semiconductor business, absolute conformance to requirements translates into the absolute minimum number of defects in parts shipped to customers, and into first-time-right customer service.

To achieve the *highest* quality, by this definition, a company requires complete commitment at all levels, including a commitment to *measuring* conformance.

100% traceability of every part through the Assembly Traceability Code is an extensive quality *discipline* that provides the necessary measurability.

It means every part shipped to every customer or distributor can be traced back to the original wafer lot, and thus to every operator, every supervisor, every machine, and every process that played a part in that lot.

That control contributes to better quality.

And the only way a semiconductor manufacturer can get that control is to control wafers *and* assembly, in house.

We do.

That code is a personal quality signature from every individual at Cypress Semiconductor.

Not just because any defect can be traced back to the individual operator or supervisor on a given process or assembly step, important as that is.

But because personal accountability for corporate quality is the only way to set the highest corporate standards.

So that laser mark isn't just the signature of the process operators.

It is the signature of the designers who create parts that exceed conformance specifications instead of merely meeting them. Designers who help ensure at the outset that there is a *guard band*—sufficient to allow our parts to exceed data sheet specifications even given correlation variances between our test equipment and yours.

That same *guard band* mentality pervades our testing department, where a part we measure at exactly 25 nanoseconds would *never* qualify as meeting a 25ns spec. No guard band, no qualification. To pass for 25ns here, a part has to run fast enough that acceptable correlation variations between different test equipment won't fail the part.

A meaningful mark. Read on.

That Assembly Traceability Code is also the signature of the manufacturing engineers who designed quality procedures *into* the Cypress Semiconductor facilities from the ground up. So quality is designed into the production flow, not something to be added later.

One example—the Assembly Traceability Code is automatically marked on the package *immediately* after molding or sealing. No alternatives. Quality assurance designed in.

Those quality engineers were able to achieve JAN certification of the Cypress Semiconductor fab facilities for JAN level B on the first try!

How? Because these engineers, supported by management, use MIL-M-38510 and MIL-STD-883 as baselines, on which to build a true quality program.

Good news: The new Cypress Semiconductor Data Book is available now.

SRAM Whoosh List

CY7C189
16x4 Static RAM
Inverting 15 ns

CY7C190
16x4 Static RAM
Non-Inverting 15 ns

CY74S189
16x4 Static RAM
Inverting 35 ns

CY27S03A
16x4 Static RAM
Inverting 25 ns

CY27S07A
16x4 Static RAM
Non-Inverting 25 ns

CY7C122
256x4 Static RAM
Separate I/O 15 ns

CY7C123
256x4 Static RAM
Separate I/O 7 ns

CY93422A
256x4 Static RAM
Separate I/O 35 ns

CY7C148
1024x4 Static RAM
$\overline{CS}$ Power Down 25 ns

CY7C149
1024x4 Static RAM 25 ns

CY7C150
1024x4 Static RAM
Separate I/O 15 ns

CY2148
1024x4 Static RAM
$\overline{CS}$ Power Down 35 ns

CY21L48
1024x4 Static RAM
$\overline{CS}$ Power Down 35 ns

CY2149
1024x4 Static RAM 35 ns

CY21L49
1024x4 Static RAM 35 ns

CY7C147
4096x1 Static RAM
$\overline{CE}$ Power Down 25 ns

CY7C130
1024x8 Dual Port
Static RAM 35 ns

CY7C132
2048x8 Dual Port
Static RAM 35 ns

CY7C140
1024x8 Dual Port
Slave Static RAM 35 ns

CY7C142
2048x8 Dual Port
Slave Static RAM 35 ns

CY6116
2048x8 Static RAM
(600 mil) 35 ns

CY7C128
2048x8 Static RAM
(300 mil) 25 ns

CY7C168
4096x4 Static RAM
$\overline{CE}$ Power Down 25 ns

CY7C169
4096x4 Static RAM 25 ns

CY7C170
4096x4 Static RAM
w/Output Enable 25 ns

CY7C171
4096x4 Static RAM
Separate I/O 25 ns

CY7C172
4096x4 Static RAM
Separate I/O 25 ns

CY7C167
16,384x1 Static RAM
Separate I/O 25 ns

CY7C185
8192x8 Static RAM
$\overline{CE}$ Power Down 35 ns

CY7C186
8192x8 Static RAM
$\overline{CE}$ Power Down 35 ns

CY7C161
16,384x4 Static RAM
Separate I/O 25 ns

CY7C162
16,384x4 Static RAM
Separate I/O 25 ns

CY7C164
16,384x4 Static RAM
$\overline{CE}$ Power Down 25 ns

CY7C166
16,384x4 Static RAM
w/Output Enable 25 ns

CY7C187
65,536x1 Static RAM
$\overline{CE}$ Power Down 25 ns

JM38510/28901
4096x1 JAN Static RAM
$\overline{CE}$ Power Down 35 ns

LOGIC Whoosh List

CY2901C
CMOS 4-Bit Slice 31 ns

CY2909A
CMOS Microprogram
Sequencer 40 ns

CY2911A
CMOS Microprogram
Sequencer 40 ns

CY2910A
CMOS Microprogram
Controller 50 ns

CY3341
64x4 FIFO Serial
Memory 2 MHz

CY7C401
Cascadeable 64x4 FIFO 15 MHz

CY7C402
Cascadeable 64x5 FIFO 15 MHz

CY7C403
Cascadeable 64x4 FIFO
w/Output Enable 25 MHz

CY7C404
Cascadeable 64x5 FIFO
w/Output Enable 25 MHz

CY7C408
Cascadeable 64x8 FIFO
w/Output Enable 35 MHz

CY7C409
Cascadeable 64x9 FIFO 35 MHz

CY7C510
16x16 Multiplier
Accumulator 45 ns

CY7C516
16x16 Multiplier 38 ns

CY7C517
16x16 Multiplier 38 ns

CY7C901
CMOS 4-Bit Slice 23 ns

CY7C909
CMOS Microprogram
Sequencer 30 ns

CY7C911
CMOS Microprogram
Sequencer 30 ns

CY7C910
CMOS Microprogram
Controller 40 ns

CY7C9101
CMOS 16-Bit Slice 30 ns

PROM Whoosh List

CY7C225
512x8 Registered PROM 25 ns

CY7C235
1024x8 Registered PROM 30 ns

CY7C281
1024x8 PROM (300 mil) 30 ns

CY7C282
1024x8 PROM (600 mil) 30 ns

CY7C245
2048x8 Reprogrammable
Registered PROM 25 ns

CY7C291
2048x8 Reprogrammable
PROM (300 mil) 35 ns

CY7C292
2048x8 PROM (600 mil) 35 ns

CY7C261
8192x8 Reprogrammable
Power Switched PROM (300 mil) 40 ns

CY7C263
8192x8 Reprogrammable
PROM (300 mil) 40 ns

CY7C264
8192x8 Reprogrammable
PROM (600 mil) 40 ns

CY7C268
8192x8 Diagnostic
Registered PROM 40 ns

CY7C269
8192x8 Diagnostic
Registered PROM 40 ns

CY7C251
16,384x8 Reprogrammable
Power Switched PROM (300 mil) 45 ns

CY7C254
16,384x8 Reprogrammable
PROM (600 mil) 45ns

PLD Whoosh List

PALC16L8L
Quarter-Power PAL20
Reprogrammable
PAL™ 25 ns

PALC16R8L
Quarter-Power PAL20
Reprogrammable
PAL 20 ns

PALC16R6L
Quarter-Power PAL20
Reprogrammable
PAL 25 ns

PALC16R4L
Quarter-Power PAL20
Reprogrammable
PAL 25 ns

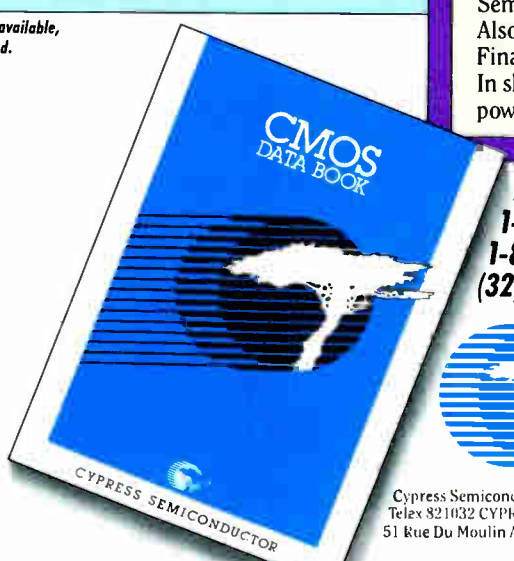
PLDC20G10
Quarter-Power Generic 24-Pin
Reprogrammable PLD 25 ns

PALC22V10L
Quarter-Power
Macro-Cell Configured
24-Pin PAL Device 25 ns

Variety of speeds available, best speed is listed.

Yours for a fast, toll-free call:

You get full specifications on all these parts.
Plus, preliminary specs on our newest parts.
And, the Data Book includes full details on the Cypress Semiconductor Military program.
Also included are full descriptions of our packaging options.
Finally, the Data Book includes all our current Application Briefs.
In short, everything you need to take advantage of high speed, low power, ultra reliable CMOS.



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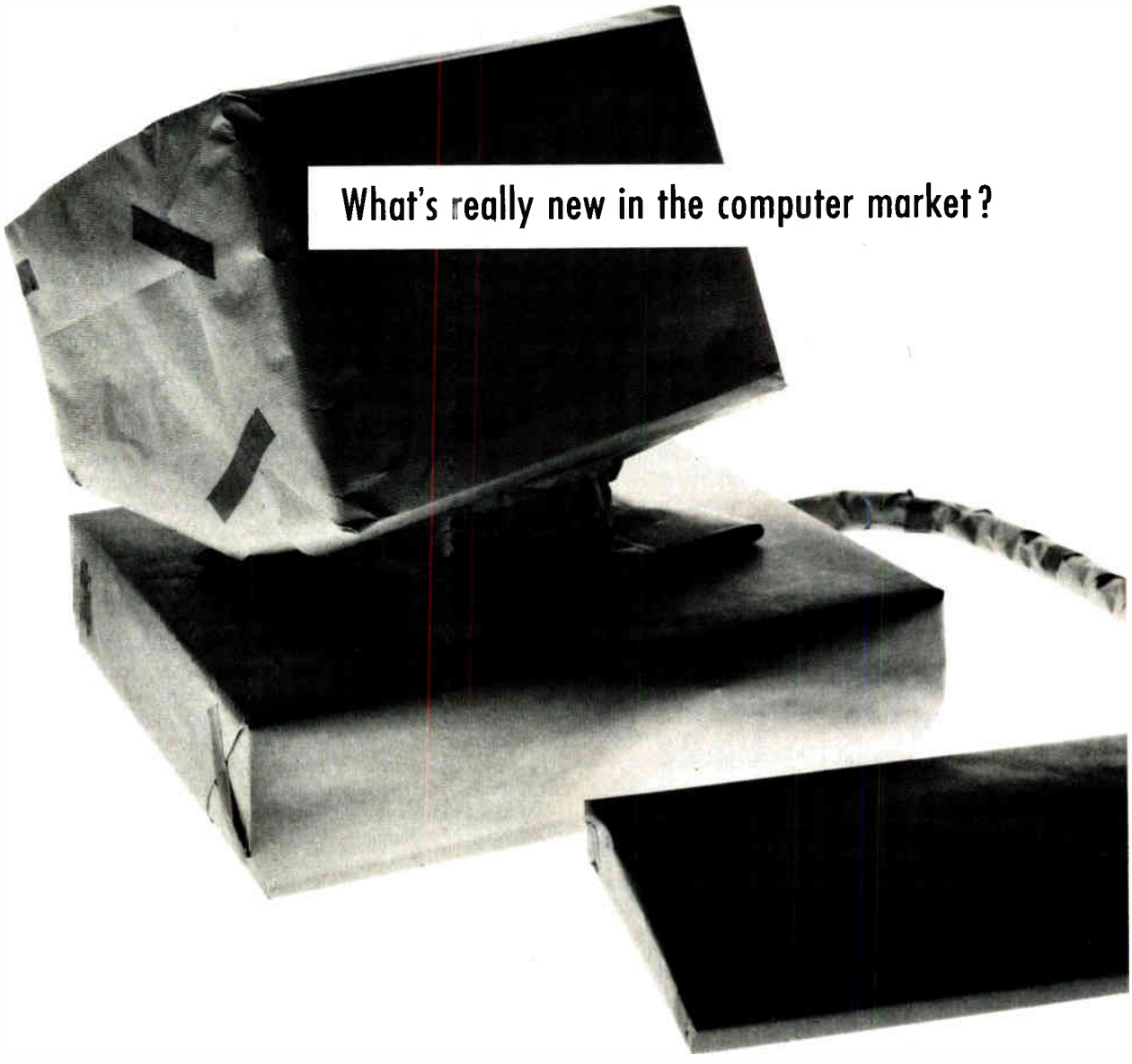
Cypress Semiconductor, 3901 North First Street, San Jose, CA 95134. Phone (408) 943-2666. Telex 821032 CYPRESS SNJ UD. TWX 910-997-0753. Cypress Semiconductor International, 51 Rue Du Moulin A Papier, BTE 11, 1160 Brussels, Belgium. Phone (32) 2-672-2220.



SYS® SYSTEMS 87
Munich, 19 - 23 October 1987

SYSTEMS answers this question and others. Like "what are the latest trends in the computer business?" "Which are the systems of the present and which of the future?" "Which hardware should you use? And which software?" SYSTEMS is unique in Europe. It is both a trade fair and a congress. There are more than 1.000 exhibitors from 16 countries. The range of products will appeal to DP-beginners and experienced users alike. It is the user-friendly trade show par excellence. SYSTEMS 87 – the trade fair for professionals. For decision-makers. For state of the art computer technology. Call us or write to us. We will give you all the information you need.

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STATE OF THE ART

BBM/PUBLICIS

Circle 116 on reader service card

INTERNATIONAL WEEK

HUNGARY BUILDS SPACE COMPUTER

A 45-member team at the Central Physical Research Institute in Budapest expects by the end of the year to complete the on-board computer for the long-life landing unit of the two Soviet space probes that will set out next July to Phobos, Mars's moon. The computer will not only collect data, as did the same team's computer on a Halley's Comet probe, but will also control all operations of the landing unit. The hardware is built by Hungarian members of the team; the software is being worked out jointly with the Soviets. For the same probe, the team is also developing the electronics for the five detectors that will measure space plasma en route. This is part of a package in which West German, Austrian, American, and Dutch scientists cooperated.

SIEMENS UPGRADES ITS UNIX PC-MX2

Siemens AG has added more capacity to its multiuser computer system PC-MX2, the hottest-selling Unix machine on the West German market. Users now have at their disposal a second 5¼-in. disk drive whose 73.7 Mbytes double the MX2's capacity. The Munich company sold more than 7,500 MX2s in West Germany in the period between last fall, when the computer hit the market, and June.

SEL PHONE ORDER WORTH $216 MILLION

Standard Elektrik Lorenz AG, the West German member of France's Alcatel NV telecommunications group, has won an order for 400 million DM, or about $216 million, worth of digital-exchange systems for West Germany's Bundespost, the communications authority. The order, for 79 of SEL's System 12 switches, is the biggest the Stuttgart firm has received. SEL, with several other firms, developed the System 12 switch while still part of ITT Corp. [*Electronics*, Jan. 22, 1987, p. 48A].

SATELLITE PAGER TO BE TESTED

Trials of the first satellite radiopaging service, by British Telecom, are expected to start at the end of the year. The service will enable drivers of long-distance trucks to be contacted immediately by their companies while they are on the road—particularly on routes across Europe, the Middle East, and Africa. The service will also provide another international extension to the existing radiopaging service operated in the UK by British Telecom Mobile Communications.

UK SKYPHONE IS SET FOR TAKEOFF

The final countdown has started for British Telecom's Skyphone with the award of a £2.6 million contract for the equipment that will automatically connect airline passengers' phone calls to the ground. The contract, with EB Communications Ltd., means that BTI has completed the purchasing of all major equipment and software. Trials of Skyphone, with calls connected by the operator, will begin in April on three British Airways 747s, allowing passengers to make international phone calls in flight.

4 FIRMS JOIN ON MISSILE PROJECT

Four leading European aerospace and electronics companies are forming a joint venture to compete for the European manufacture and in-service support of the Advanced Medium Range Air-to-Air Missile. The company, called Amraam Ltd., is based in Hatfield, UK. It comprises British Telecom and Marconi Defence Systems of the UK and Messerschmidt-Bölkow-Blohm and AEG of West Germany. The high-performance AIM 120, the next major beyond-visual-range air-to-air missile for the UK and West Germany, is also intended for other NATO users.

TALKS FAIL TO SET UP KDD COMPETITOR

Negotiations between International Telecom Japan Inc. (ITJ) and International Digital Communications Planning Inc. (IDC) to form a consortium to compete with Kokusai Denshin Denwa Co. (KDD), a monopoly in Japan's international telecommunications business [*Electronics*, March 19, 1987, p. 54], have broken down after five months. Instead, the two Tokyo companies will apply separately to the Ministry of Posts and Telecommunications for approval of their own new businesses. IDC insisted that a unified telecom firm should build and own a North Pacific cable, but ITJ rejected the proposal. ITJ plans to begin its own new business with Intelsat communications-satellite services and acquisition of the right to use the TPC-3 cable connecting Japan with Hawaii and San Francisco.

NEC MAY ASSEMBLE ITS 32-BIT PC IN U. S.

NEC Corp. will start assembling its desk-top 32-bit personal computer, the Powermate 386 series, in the U. S. this fall unless the U. S. government abolishes its trade sanctions against Japan. The 32-bit personal computer, which was at first scheduled to be exported to the U. S. starting last month, will be assembled at NEC Information Systems, Boxborough, Mass. The Tokyo company has been assembling its 16-bit personal computers at NEC Information Systems and NEC Home Electronics U.S.A., Atlanta, since the U. S. slapped 100% import tariffs on personal computers, power tools, and color-TV sets in April. [*Electronics*, May 28, 1987, p. 53].

MATSUSHITA TO SELL 16-BIT PC

Matsushita Electric Industrial Co. is marketing a 16-bit personal computer compatible with Fujitsu Ltd.'s FM-R series. The Osaka company's new personal computer will use a basic input/output system chip supplied by Fujitsu, which will give it complete software compatibility with the FM-R series. Matsushita aims to promote the sales of the new computer by taking advantage of FM-R's abundant software products. More than 1,000 software packages for the FM-R series are currently on the market. Matsushita and Fujitsu expect to make inroads in NEC Corp.'s domination of the 16-bit personal-computer market by selling compatible computers under their brand names.

SONY OPENS CD PLANT IN AUSTRIA

Sony Corp. of Tokyo has opened a plant for compact-disk production in Salzburg, Austria, the first such Japanese factory in Europe. Its initial capacity will be 12 million CDs a year, and that is expected to double to 24 million by next year. Sony expects European consumption of CDs to total about 80 million units this year, twice the number of 1986.

NIXDORF TERMINAL TRANSLATES CHINESE

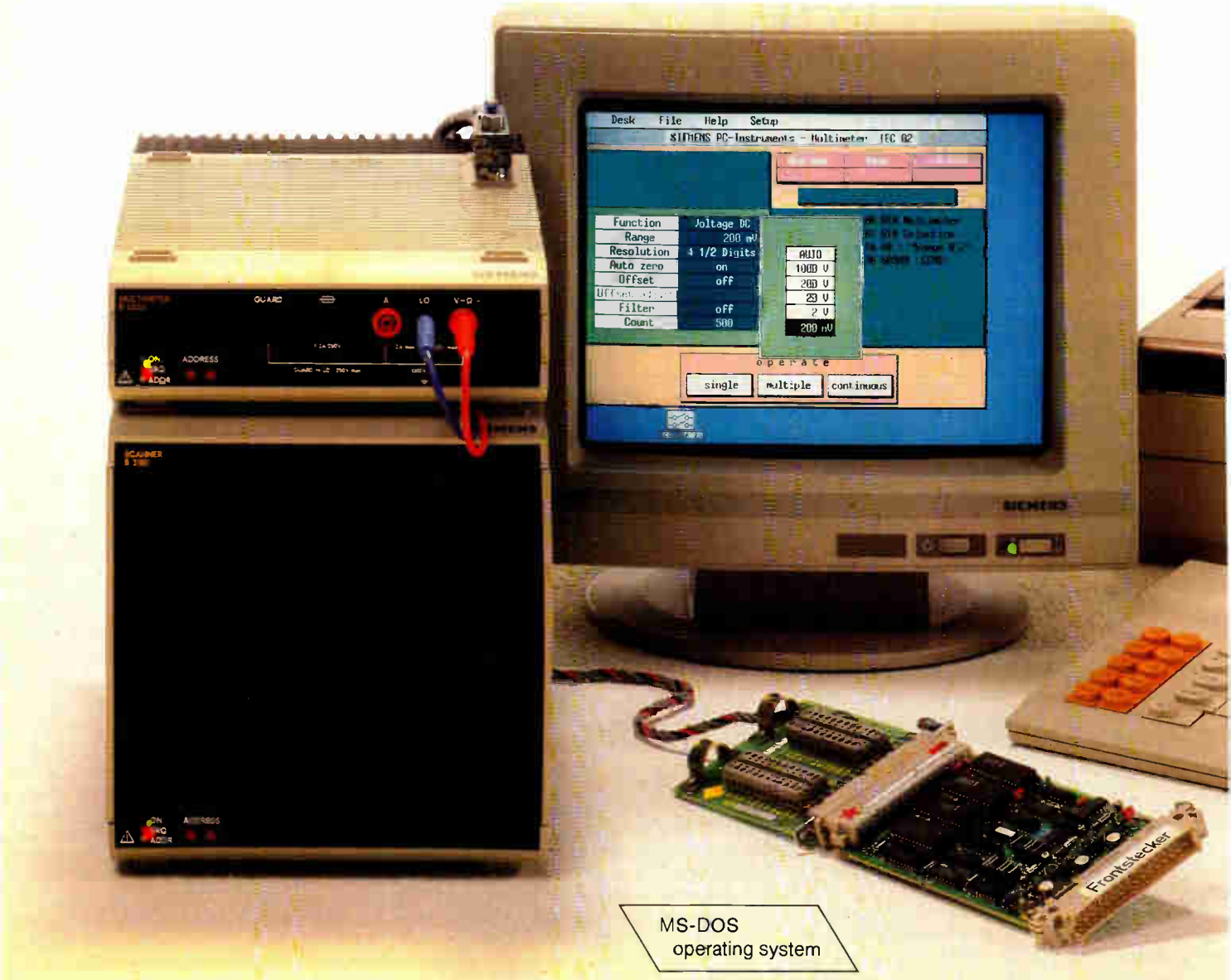
Nixdorf Computer AG has announced a terminal system that automatically converts Roman characters into the symbols used in China. The system, called CTS, was developed at Nixdorf's subsidiaries in Hong Kong and Japan for the model 8810 M35 of the West German company's personal-computer family.

SIEMENS

How can you track adjustments if these new measurement instruments lack operating elements?

SIEMENS

No need to...
the PC's got them in storage.



Now, you can stop worrying about misplaced paperwork when repeating specific measurements. How? With Siemens' newly-developed measurement instruments that cooperate with personal computers over an IEEE 488 bus. And that makes "take it from the top" a thing of the past. Not to mention situations for which the paperwork no longer exists.

What's more, our new instruments make setup, parameter adjustment, and measurement execution easier than ever before. At the touch of a button. And just as quickly, the PC converts units and results into the form you choose. You don't need programming experience to reconstruct earlier measurements as often as you like. With computer support, once is enough. Our standard program generator takes care of the rest.

All this adds up to less routine, more time for what really counts – and better results. The kind of convenience that's fast becoming the hallmark of advanced measurement technology.
From Siemens.

Measurement's never been easier.
With PC instruments from Siemens.

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Circle 117 on reader service card

PHILIPS

PHILIPS

The 32-bit Philips VMEbus CPU packs such incredible power on one board.

INDUSTRIAL AUTOMATION - VMEbus

Yes indeed, Philips offers you more:
To design high performance VMEbus boards Philips applies all its know-how from silicon to system.
One result is the PG2100 VMEbus single board computer offering:

- A 68020 Microprocessor unit (MPU) with 32-bit address and data path
- A 68851 paged memory management unit (MMU) which provides address translation and access protection for the entire address range of the MPU
- A 68881 floating point co-processor
- 4 Mbyte dual ported RAM including a 1 Kbyte location monitor
- 256 Kbyte EPROM
- 3 serial interfaces
- VMSbus interface
- SCSI-bus interface

Only a few suppliers work from silicon to system – Philips is one.
So just ask yourself:
Who offers more?

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05-28 32 98

India
022-4 92 15 00
Italy
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Netherlands
040-78 83 25
New Zealand
09-89 41 60

Norway
02-26 62 00
Portugal
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INTERNATIONAL PRODUCTS

HOW HITACHI's MICROPROCESSOR WILL SPEED VCRs TO MARKET

ON-BOARD PROM IS FASTER WAY THAN ROM TO MOVE INTO PRODUCTION

Designers of consumer-electronics products that feature fluorescent displays can significantly speed up product-development time by using a new programmed microprocessor from Hitachi Ltd. to run the display instead of following the more conventional method of using custom-masked read-only memory. They can cut five weeks off development time by using the 4-bit HD4074709 microprocessor with 16 Kbytes of programmable ROM to create the display's firmware.

In the fast-moving consumer market, designers "can move quickly from system program development to the production stage, because system programming of a PROM takes less than a week," says Kazuo Sato, manager of Hitachi's Strategic Planning Department. Developing masked-ROM versions often takes 45 days or more.

By using programmed HD4074709s during the early stages of mass production, manufacturers can get at least a five-week head start on their competition, the company claims. For low-volume products, the PROM-based microcontroller can continue to be used throughout the product's life-cycle.

Hitachi recommends a more cost-effective solution for high-volume products. Although the product may enter the market with the PROM-based part, Hitachi can typically replace it with a masked-ROM version that costs roughly 30% less than the PROM version within 45 days, says Sato. Hitachi's masked-ROM replacement device is the HD404709.

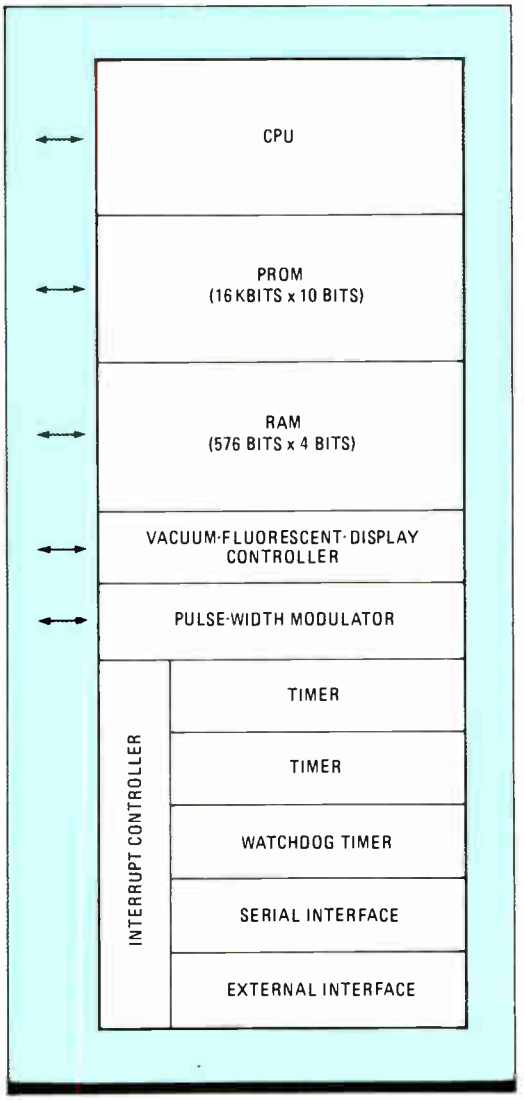
Fabricated in 2-μm CMOS technology, the newest member of the HMCS400 microprocessor family boasts on-chip driver and controller circuitry that operates at −40 V—enough to drive fluorescent display tubes directly. Its 16 Kbytes of one-time electrically programmable ROM breaks new ground in memory size for microprocessor-PROM devices, packing enough memory to handle the firmware for the most sophisticated VCRs, says the Tokyo company.

Since both the PROM and masked-ROM devices have the same outer dimensions—740 by 2,256 mils—and the same pinout, replacing one for the other during production is both simple and safe. Debugging at the system level need be done only once.

Hitachi expects its microprocessor to find ready markets in VCRs, compact-disk players, automotive audio components, and other products that use fluorescent display tubes.

VCRs and CD players account for the lion's share of the market for vacuum fluorescent displays. More than 30 million VCRs and 7 million CD players will be produced worldwide in 1987, Hitachi estimates, and the majority will incorporate vacuum fluorescent displays. To address this market, Hitachi expects to produce 500,000 HD7074709 chips by March 1988.

The HD4074709 can run as fast as a 0.5 μs cycle time or as slow as 250 μs. This flexibility has two advantages. It suits the devices for a wide range of products, and it reduces power consumption. Cutting the cycle time in half when the display is relatively static, for example, reduces power consumption by one half.



ENERGY MISER. Three timers in Hitachi's smart PROM help minimize the IC's energy dissipation.

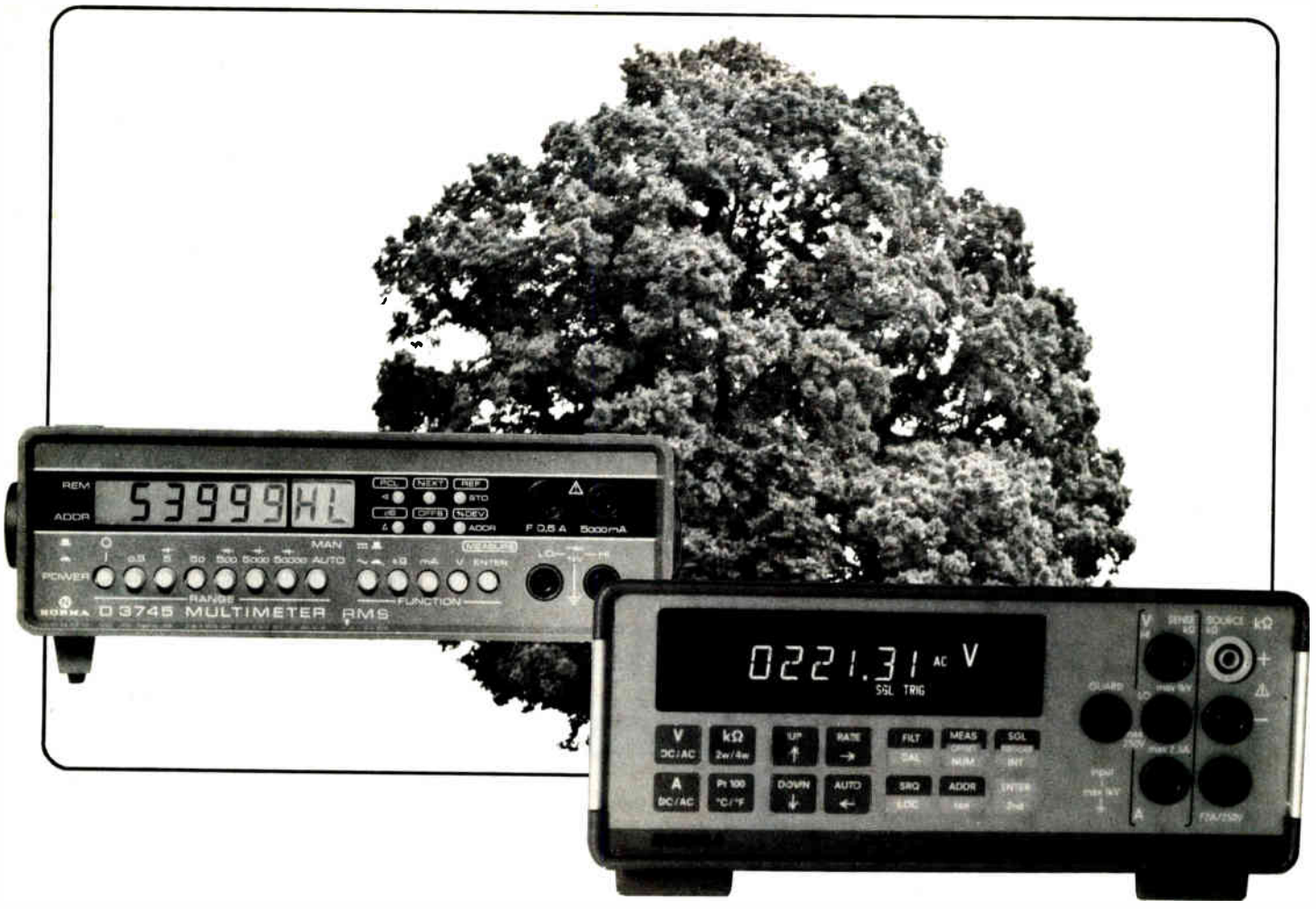
Making the chip capable of intermittent operation is another way Hitachi reduces overall power needs. There are three power-saving modes: standby, watchdog, and stop. Although Hitachi has not yet released data on power consumption under maximum active-state load conditions, it claims power consumption is reduced by 80% in the standby mode and by 95% in the watchdog and stop modes.

To implement these modes, three timers are included on-chip: a watchdog timer monitors system activity and resumes operations quickly from the standby mode; an 8-bit free-run-time or timer base is used as the microprocessor's clock; and another 8-bit timer with an event counter resets the system when it changes modes.

Similarly, the chip implements a range of interrupt factors. Four external and three internal interrupt functions are included.

The chip's controller/driver design can handle up to 16 columns by 16 segments, and any unused display-driver channels can be used as general-purpose input/output ports. An eight-step dimmer function is included, and static display is also supported by the controller.

There are a total of 56 ports, 34 of which are high-voltage



YOUR REQUIREMENTS KEEP GROWING – HERE IS OUR SOLUTION

PRECISION MULTIMETER D 4845
A Concept for Superiority

500 measurements per second and a display range up to 240,000 measuring points are examples of this superiority. The integrating charge-compensation method is supported by multiprocessor technology, ensuring fast A/D conversion, high measuring accuracy and stability. The foil-type keyboard, the special alphanumeric display and user-friendly prompting make for simplicity of handling. Full overload protection and high noise voltage suppression afford measuring comfort in practical service.

Fascinating Features

Its many measuring mode make the PRECISION MULTIMETER D 4845 outstandingly suitable for universal applications in laboratories and testing-rooms. Besides measurements of voltage and current, this meter offers measurement of resistance (in both two-wire and four-wire mode), measurement of temperature (°C / °F) and an offset function (measurement/numeric). The Standard IEC 625/IEE 488 Interface with its simple but versatile programming facilities endows the PRECISION MULTIMETER D 4845 with full systems capability.

MULTIMETER D 3745
The Key to Perfect Measuring

Tested and trusted worlwide, its problem-oriented software will solve a wide range of applications. Besides the standard quantities, the MULTIMETER D 3745 measures deviations from entered reference operations (e. g. the computation of logarithmic ratios). It stores measured data and outputs them again on request. There is an additional display area for complete information on measured data and operational status.

A leader in meter design

New technologies, state-of-the-art design and more than 60 years experience in electrical measuring instrument manufacture combine to guarantee quality and reliability.

Worldwide sales and service network

Our sales organization is in touch with customers all over the world and ensures high workmanship in servicing. We export to 70 countries.

NORMA

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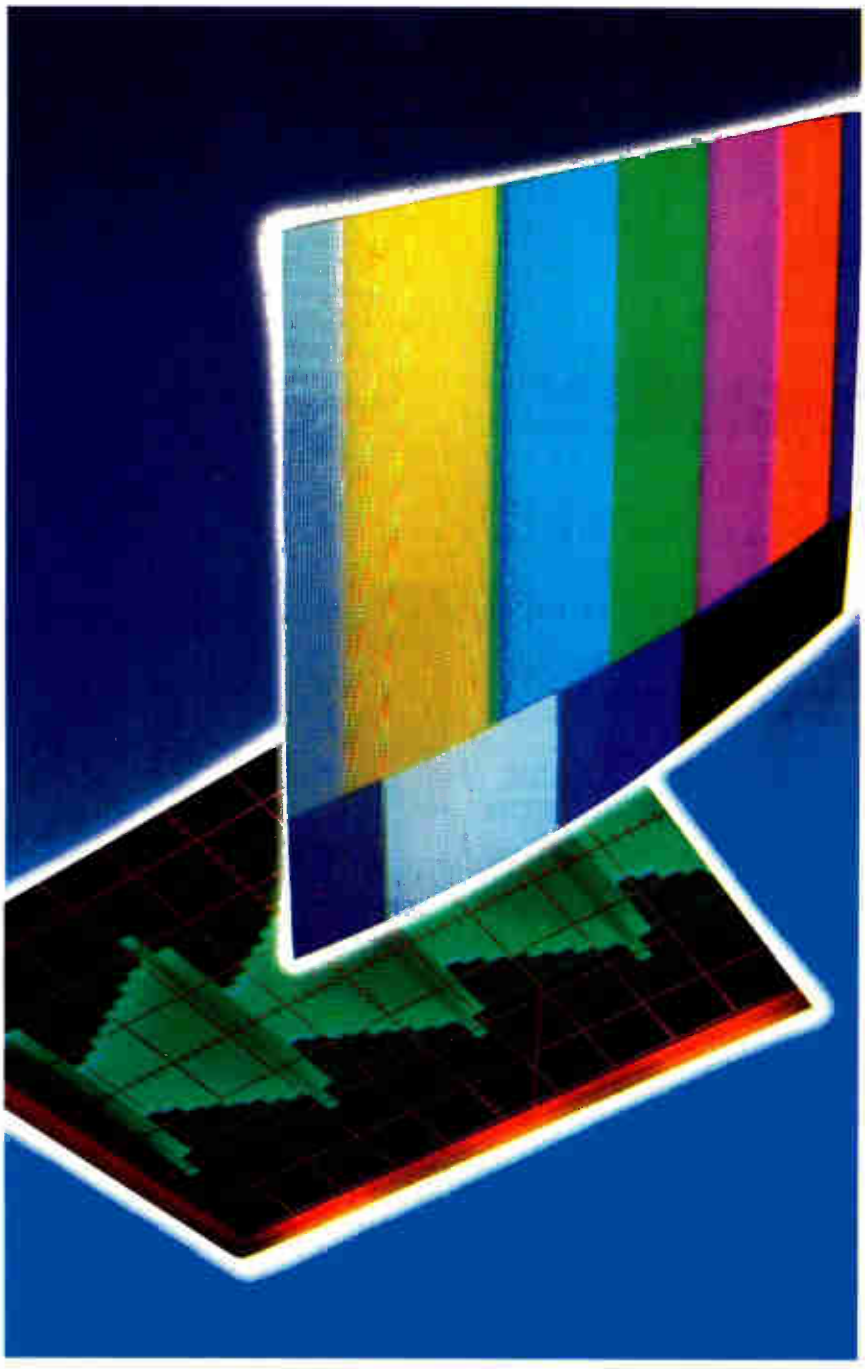
NORMA Messtechnik, Optik, Elektronik, Gesellschaft m.b.H., A-2351 Wiener Neudorf, Austria, Eumigweg 7, POB. 81, Telephone: (2236) 61 530-0, Telex: 79316, Teletex: 32 21 427, Telefax: (2236) 61 530/584 Cables: NORMAMETER WIEN

Circle 119 on reader service card

ANRITSU CREATES NEW POSSIBILITIES WITH VIDEO MODULATION



Signal generators that perform in any band from radio to TV.

Anritsu, seeking to satisfy the needs of the mobile radio, mobile phone and audio-video industries, presents two new synthesized signal generators with the best performance in their class. The MG3601A and MG3602A offer many features not available in any other equipment.

Because they have the ***highest spectral purity*** *in their class, the MG3601A/3602A generate the most reliable signals for precise evaluation of any type of receiver. They serve a tremendous variety of equipment too, since they cover the* ***widest frequency range****. The MG3601A offers output from 100kHz to 1.04GHz, and the MG3602A provides 100kHz to 2.08GHz, both tunable within 10 Hz. Modulation includes video, ØM, AM and FM, for complete analysis of radio, CB, pager, mobile phone, or even video systems. Moreover, automatic calibration for greater* ***DC FM stability*** *is as easy as pushing one button.*

The MG3601A/3602A also include a valuable ***memory function*** *that stores up to 100 frequencies and 30 programs to reduce setup time. They are easy to operate, and feature a frequency tuning knob for faster settings. These lightweight (less than 16kg) synthesizers are even equipped with GP-IB for remote control.*

Choose the signal generators with the highest cost performance for any purpose.

MG3601A/3602A Signal Generators

Anritsu

ANRITSU CORPORATION 10-27, Minamiazabu 5-chome, Minato-ku, Tokyo 106, Japan Phone: 03-446-1111 Telex: 0-242-2353 ANRITU J
ANRITSU AMERICA, INC. 15 Thornton Road, Oakland, N.J. 07436, U.S.A. Phone: 201-337-1111 Sales & Service 1-800-255-7234 Telex: 642-141 ANRITSU OKLD
ANRITSU EUROPE LIMITED Thistle Road, Windmill Trading Estate, Luton, Beds, LU1 3XJ, U.K. Phone: (STD0582) 418853 Telex: 826750 ANRSEU G
ANRITSU ELEKTRONIK GmbH Grafenberger Allee 54-56, 4000 Düsseldorf 1, F.R. Germany Phone: (0211) 679760 Telex: 8584904 ANRI D
ANRITSU ELECTRÔNICA S.A. Av. Passos, 91-Sobreloja: 203/205-Centro, 20051-Rio de Janeiro-RJ, Brasil Phone: (021) 224-6086, 224-9448 Telex: 2131704 ANBR BR

Circle 120 on reader service card

ports that can handle signals of –40 V.

The HD4074709 comes in a 64-pin plastic dual in-line package or in a 64-pin flat plastic package.

Engineering samples of the HD4074709 are scheduled to be released in Japan in September. Samples in plastic DIPs will cost 4,000 yen each. Samples of a ceramic windowed DIP cost 15,000 yen. In 10,000-unit lots, the plastic production devices will cost 2,500 yen each. Engineering samples of the device are scheduled to go on the market outside Japan in the first quarter of 1988.

–Ayako Hayashihara

Hitachi Ltd., International Sales Division III, 1-5-1 Marunouchi, Chiyoda-ku, Tokyo 100, Japan.
Phone 81-3-212-1111 [Circle 500]

10-MIPS CPU POWERS UNIX WORK STATION

A graphics work station from Whitechapel Workstations Ltd. offers 10 million instruction/s CPU performance, compatibility with AT&T Co.'s Unix 4.2 operating system, and a 20-in. color monitor.

Based on the R2000 reduced-instruction-set chip set from MIPS Computer Systems Inc., Sunnyvale, Calif., the work station performs 1.78 million floating-point operations/s using the Linpack benchmark.

It supports industry-standard software such as TCP/IP, NFS transparent file-access protocols, X Windows, and NeWS distributed window-management systems. Target applications include 3-d modeling, simulation, circuit design, and artificial intelligence. Slated for introduction in September and for volume production by January 1988, it will cost $30,000 U. S.

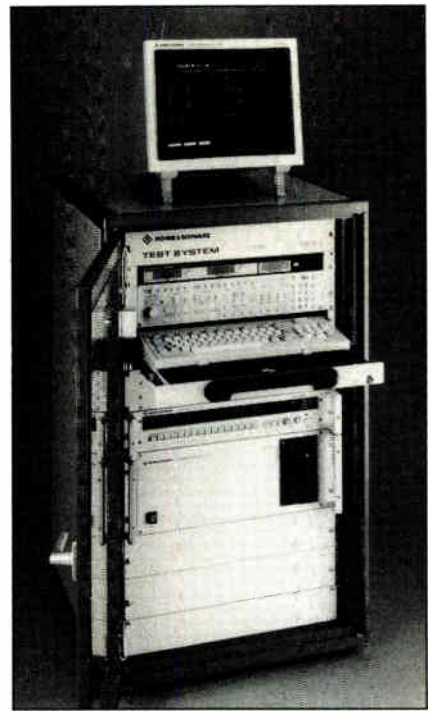
Whitechapel Workstations Ltd., 75 Whitechapel Rd., London E1 1DU, UK.
Phone 44-1-377-8680 [Circle 701]

VERSATILE TESTER HANDLES VCRs, TAPES

The TS6010 automatic test system from Rohde & Schwarz features system software flexible enough to handle any task in quality-control inspections of audio and video recorders and tapes.

The software, written in Pascal and Basic, comprises user-friendly editors and problem-oriented test programs, and it can adapt the computer-controlled system to customized applications. A plain-word test language in Basic yields test programs that can be easily followed and modified.

The TS6010 measures voltage level from 10 μV to 300 V, frequency response at 10 Hz to 100 KHz, frequency from 10 Hz to 250 KHz, distortion as low as 0.003%, and signal-to-noise ratio.



The integrated wow and flutter meter determines pitch variations, wow, and flutter. It uses different weighting criteria in accordance with international standards.

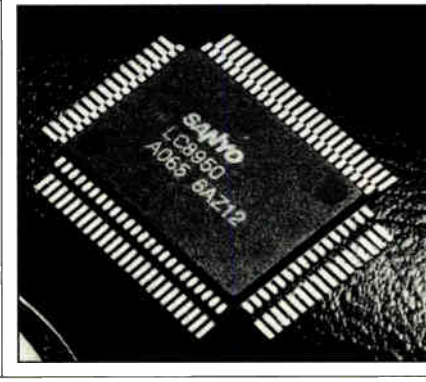
Delivery time for the TS6010 is three months. It costs 140,000 DM in West Germany.

Rohde & Schwarz, Muehldorfstr. 15, D-8000 Munich 80, West Germany.
Phone 49-89-41292625 [Circle 702]

CD-ROM CHIP IS QUICK AT ERROR CORRECTION

Sanyo Electric Co.'s LC8950 integrates on a single chip real-time error correction and interface functions for compact-disk-ROM machines. It corrects errors 5 to 20 times faster than conventional control microcomputers and offers a transfer rate of 2.3 Mbytes/s.

The chip combines a microcomputer with a 64-Kbyte memory buffer that is needed to handle the digital-signal-processing techniques used in error correction. It maintains compatibility with low-speed host computers by caching up to 27 disk sectors.



A high-speed first-in, first-out memory interfacing with the host makes compatibility with the Small Computer Systems Interface easier. The LC8950 runs on a conventional flashlight battery and will be available in production quantities in October for 5,000 yen each.

Sanyo Electric Co., VLSI Sales Div., 180 Ohmori, Ampachi-cho, Ampachi-gun, Gifu 503-01, Japan.
Phone 81-58464-4899 [Circle 704]

FIBER-OPTIC LINK CARRIES TV SIGNALS

Foundation Instruments' T3/R3 video fiber-optic link transmits high-quality analog signals over distances up to 3 km with the exceptionally low signal distortion characteristic of optical fiber.

The link consists of the T3 transmitter module and the R3 receiver module. Each module carries its own power supply and is small enough to be mounted in a TV camera enclosure.

Targeting both teleconferencing and closed-circuit TV applications, the T3/R3 communications link is particularly useful in areas where electromagnetic interference is a problem or where the small size of optical fibers offers an installation advantage. The fiber-optic link is

available now and costs $470 U. S.

Foundation Instruments, Lightwave Division, 24 Colonnade Rd., Ottawa, Ontario, Canada K2E 7J6.
Phone (613) 226-4000 [Circle 703]

PCB PLATING SYSTEM BOOSTS THROUGHPUT

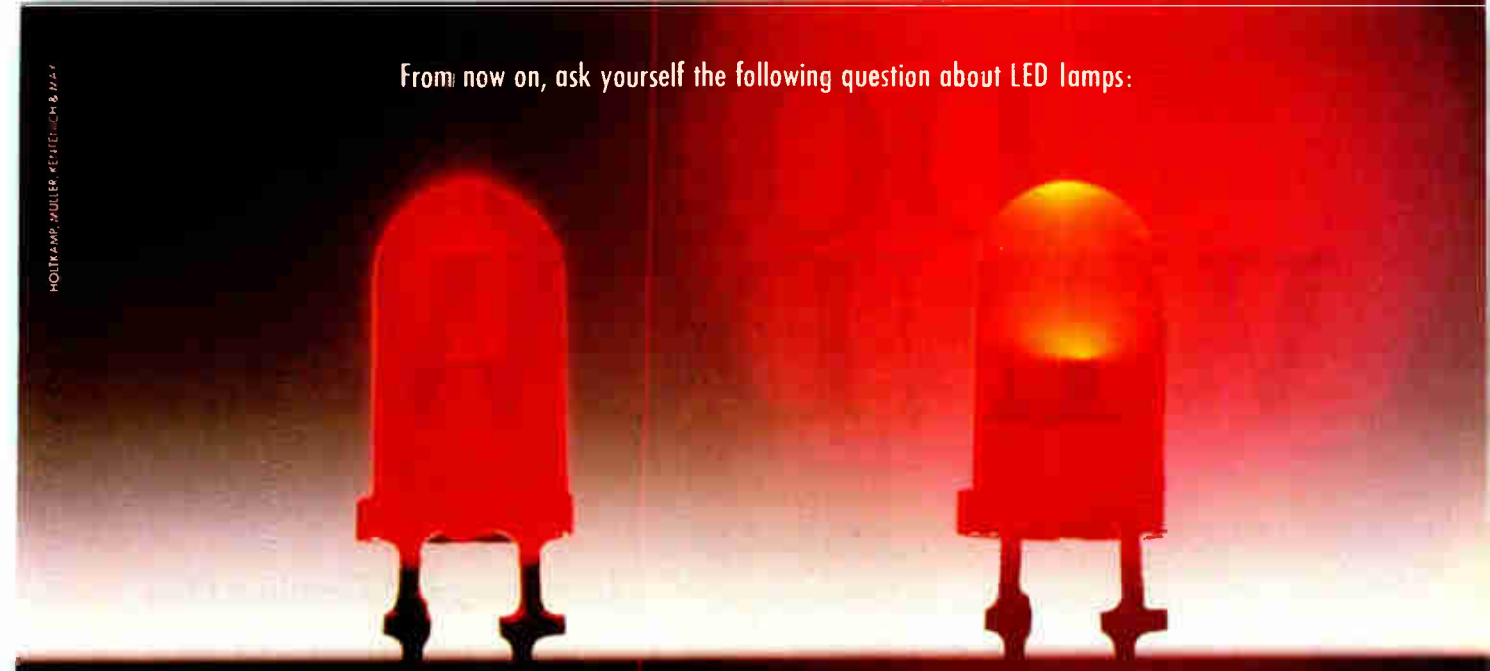
Mega Electronics Ltd.'s through-hole plating system for printed-circuit boards uses just two process tanks—as opposed to multiple tanks in competing products—to provide faster processing.

Specially formulated chemicals are the key to reducing the number of process tanks. Besides the two process tanks, the PL901 consists of a plating bath and two spray-wash tanks.

Tank cleaning and recharging is simplified by a drain in the base of the process tanks. The unit measures 900 by 900 by 600 mm deep. It is available now for £2,000, including chemicals.

Mega Electronics Ltd., 9 Rainwater Rd., Saffron Walden, Essex CB11 3HU, UK.
Phone 44-7-992-1918 [Circle 705]

From now on, ask yourself the following question about LED lamps:



STANDARD?

The standard version of Toshiba's LED lamps has proved itself repeatedly in practice as being just what's needed in most applications. Nonetheless a new generation of Toshiba LED lamps means that you should reconsider your requirements.

OR SUPER?

The brightness of Toshiba's new generation of LED lamps is striking: up to 1,000 times brighter than the standard version. So light, so brilliant that optimum luminosity is guaranted from every viewing angle. As for application, be it stadium or Hi-Fi displays, Toshiba's ultra-bright LED lamps are ideal.

All of this is backed up by Toshiba's know-how, service and production capacity. Find out more by sending us this coupon.

Please send me more information on the new generation of Toshiba LED lamps.

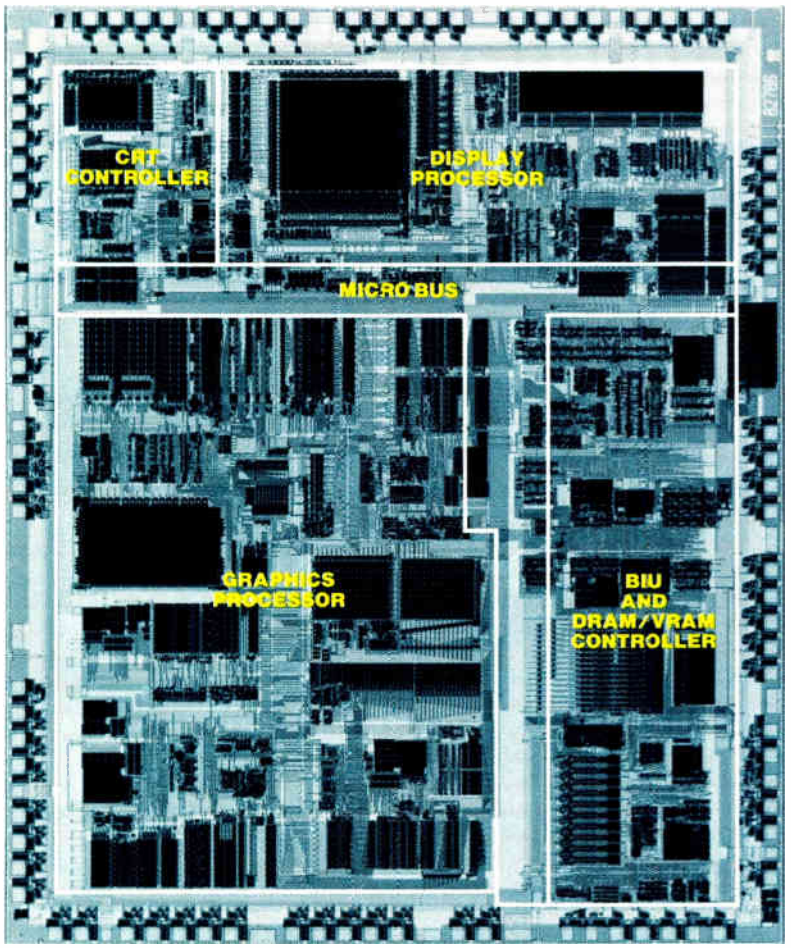
Name:	Company:
Tel.:	
Address:	

In Touch with Tomorrow

TOSHIBA

TOSHIBA EUROPE (I.E.) GMBH, Görlitzer Str. 5–7, 4040 Neuss 1, Tel.: 0 21 01/1 57-0; München, Tel.: 0 89/92 80 91-0; Stuttgart, Tel.: 0 71 52/2 10 61-66 · TOSHIBA UK LTD, Tel.: 00 44 2 76/6 22 22 · TOSHIBA EUROPE I.E. GMBH, Paris, Tel.: 00 33 1 48 55/56 56 · TOSHIBA ELECTRONICS ITALIANA S.R.L., Milano, Tel.: 00 39 39/63 88 9[illegible] · TOSHIBA ELECTRONICS SCANDINAVIA AB, Stockholm, Tel.: 00 46 8/14 56 00

DOES WINDOWS.



Intel's 82786 graphics coprocessor supports its family of 16- and 32-bit central processing units.

Intel Designs A Graphics Chip For CAD And Business Use.

"Two completely different kinds of end customers seem to be fueling the embryonic graphics chip market: the personal computer user in business, and the designer on a work station. Intel Corp., long reported to be developing a graphics-oriented microprocessor, is finally announcing its 82786 graphics coprocessor for both applications.

Demand for multiple-windowing capability is on the rise, especially for multitasking chores in the office environment. The 82786 implements this capability in hardware. Each application can have its text and graphics drawn into separate regions of memory, which are then combined within windows of the same display..."

Excerpted from an exclusive article in the May 19, 1986 issue.

Electronics

THE LEADER IN NEW TECHNOLOGY COVERAGE

Introducing a new desktop plotter that's small enough to fit in this magazine.

Fujitsu's new FPG-310 plotter is truly compact: it needs only 420 × 260 mm, which leaves you plenty of elbow room. The FPG-310 weighs less than 5 kg and draws less than 35 watts of power.

A wide variety of media

Now you can print figures and text on almost any medium — coated paper, OHP films, tracing paper and, of course, standard paper. And the medium can be any size from postcards to A3 sheets.

Superb graphics

Precise 0.025 mm resolution and 6 bright colors raise your computer's graphics to new heights of effectiveness. The FPG-310 gives you the flexibility of a dot matrix printer but provides far superior quality.

Full compatibility

Three standard interfaces — Centronics, RS-232C and GP-IB — let you connect the plotter to virtually any personal or business computer.

Amazing versatility

Applications include business graphs, education, measurement systems, FA — and even personal CAD. Hobbyists also find the plotter useful for a wide variety of tasks.

Whether you use the FPG-310 in your home office or in a workstation, no job is too big for this little plotter.

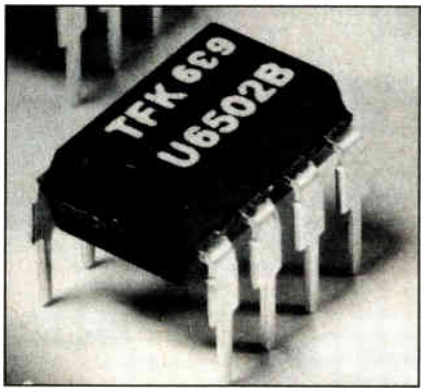
Fujitsu Color Plotter FPG-310

FUJITSU MIKROELEKTRONIK GmbH:
Arabella Center 9. OG/A, Lyoner Straße 44-48, D-5000 Frankfurt am Main 71, F.R. Germany Phone: 069-66320 Telex: 0411963 Fax: 069-6632122
FUJITSU COMPONENT OF AMERICA, INC.:
3320 Scott Blvd., Santa Clara, California 95054-3197, U.S.A. Phone: 408-562-1000 Telex: 910-338-0190 Fax: 408-727-0355
FUJITSU LIMITED (Electronic Components International Marketing Div.):
Furukawa Sogo Bldg., 6-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100, Japan Phone: National (03) 216-3271 International (Int'l Prefix) 81-3-216-3211
Telex: 2224361 Fax: (03) 216-9771

FUJITSU

PRESCALER HANDLES 5-GHz SIGNALS

The U6502B prescaler from Telefunken electronic GmbH can handle frequencies up to 5 GHz. The silicon IC constitutes a low-cost alternative to expensive frequency dividers based on gallium-arsenide technology.



Operating with a divider factor of 2, the U6502B can be used in 4-GHz satellite TV, telecom systems, and test equipment. The device augments Telefunken's lineup of 1- and 2-GHz dividers. The U6502B is available now. Price depends on importing country.

Telefunken electronic GmbH, P.O. Box 1109, D-7100 Heilbronn, West Germany.
Phone 49-7131-672230 [Circle 706]

INTERFACE GIVES PCs UP TO 8 I/O CHANNELS

A buffered interface system from Alfatron Ltd. extends the functional reach of personal computers by providing up to six serial and two parallel channels for peripherals. In addition to linking computers to peripherals, it can be configured to allow computers to communicate with each other without switching or recabling.

The A2000 offers buffer sizes ranging from 256 Kbytes to 1 Mbyte. Buffer allocation is dynamic to maximize memory utilization. Serial channels run at speeds up to 38.4 Kbits/s.

The system is available now, and carries an export price of U.S. $330.

Alfatron Ltd., 1761 Ferntree Gully Rd., Ferntree Gully, Victoria 3156, Australia.
Phone 61-3-758-9000 [Circle 707]

INTERFACE CHIP RUNS OFF 5 OR 12 V

The MAD 430 hybrid RS-232-C interface chip from Mitsumi Electric Co. eliminates the need for a separate 12-V power supply for the interface by integrating a 5-V-to-12-V dc voltage converter on the chip.

Besides operating from a single 5-V power supply, the chip has a built-in quad line driver and receiver to satisfy the requirements of standard data-terminal interfaces.

Target applications for the chip include printers, personal computers, and laboratory instruments. It consumes 300 mA of current. Samples are available now for 500 yen each.

Mitsumi Electric Co., 8-8-2 Kokuryo-cho, Chofu, Tokyo 182, Japan.
Phone 81-489-5333 [Circle 708]

EPROM ADAPTER CUTS PROGRAMMING COSTS

An adapter for programming 32-pin, 1-Mbit erasable programmable read-only memories can be used with any programmer that handles 28-pin paged 1-Mbit EPROMs. Stack Ltd.'s 32-pin adapter eliminates the need to purchase a separate programmer for 32-pin devices.

For ease of gang programming, the adapter is designed to be easily installed in adjacent sockets. Its design also allows it to program 2-Mbit devices. The adapter costs £75 and is available now.

Stack Ltd., Unit 8, Wedgewood Rd., Bicester, Oxfordshire OX6 7UL, UK.
Phone 44-869-240404 [Circle 709]

LINE SELECTOR WORKS WITH ANY SCOPE

The PM8917 video-line selector from Philips can display video waveforms from a standard composite-video input signal on virtually any oscilloscope without the need for additional special interface devices.

Using a 0.5-to-3-V input, the selector generates sync signals for the display of frames, fields, and lines, plus any selected line of a complete video frame.

Trigger outputs of 1 V are provided for any selected line, frame, and field signals.

A rear-panel switch selects frame or field outputs, while line signals are available at a fixed output. The PM8917 automatically selects 625- or 525-line broadcast-system standards, and a front-panel LED indicates which standard is selected.

The PM8917 can be delivered in two months. It has a domestic price of about 1,000 Dutch guilders. Export price depends on exporting country.

Philips I&E Division, P.O. Box 218, 5600 MD Eindhoven, The Netherlands.
Phone 31-40-788620 [Circle 710]

Faster!

CMOS at speed.

A few more fast, fast reasons to call for our new databook:

1. New 64K SRAM. 25ns. Seven configurations—including bit-wide, nibble-wide, byte-wide, separate I/O, and all with low, low, power. As low as 50 mA active at 45ns.

2. New 128K Reprogrammable PROM. 45 ns. 100 mA active, 30 mA standby.

3. New 64 x 9 and 64 x 8 FIFOs. 35 MHz. Virtually no bubble through. Cascadeable.

4. Fastest 22V10 Reprogrammable PLD. 25ns. 55 mA. And we have the board to turn your PC into a PLD/PROM programmer, too!

5. *High speed CMOS SRAM.*

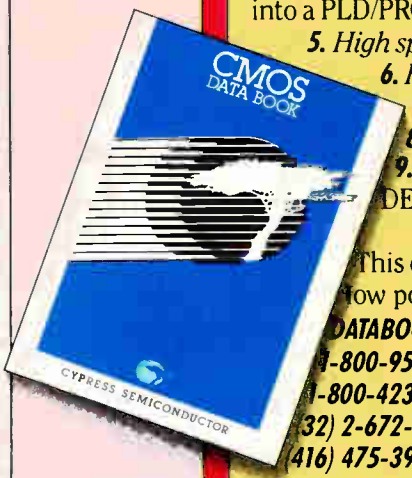
6. *High speed CMOS PROM.*

7. *High speed CMOS PLD.*

8. *High speed CMOS LOGIC.*

9. Fabricated and assembled in our DESC-certified U.S.A. facilities.

This databook, packed with high speed, low power parts, is yours for a phone call.



DATABOOK HOTLINE:
1-800-952-6300, Ask for Dept. C60
1-800-423-4440 (In CA), Ask for Dept. C60
(32) 2-672-2220 (In Europe)
(416) 475-3922 (In Canada)

CYPRESS SEMICONDUCTOR

We illustrate the Lockheed SR-71 Reconnaissance aircraft, holder of the world's air speed record: 2,193 miles per hour. We're fond of speed records. Over 30 of our parts have broken or still hold speed records for integrated circuits.

Cypress Semiconductor, 3901 North First Street, San Jose, CA 95134.
Phone (408) 943-2666 Telex 821032 CYPRESS SNJ UD, TWX 910-997-0753.

CODEC IC PROGRAMS QUICKLY FROM A PC

The ADA-5011 convolutional coder/decoder chip from Elgal Instrumentation & Systems Ltd. offers coding gains as high as 7 dB. All parameters are fully programmable on the fly over the RS-232-C port of a personal computer.

The codec's quick programmability allows designers to build systems that adapt coding parameters to line conditions. Fabricated in 1.5-μm CMOS for low power consumption, it targets satellite communications and military applications.

Designed to minimize external peripheral circuitry, the codec requires just three external memory chips and operates as a microcomputer peripheral for on-line parameter programming. Its maximum data rate is 7.5 Kbits/s.

An evaluation board including the codec, controller, interface, and menu-driven software for the IBM Corp. Personal Computer is available for evaluation purposes. The chip costs 942 Israeli shekels in single-unit purchases and 330 shekels in 1,000-unit purchases. It is available now with delivery 60 to 90 days after order. Export price for single units is $585; and $205 each in 1,000 unit quantities.

Elgal Instrumentation & Systems Ltd., P. O. Box 494, Carmeil 20101, Israel.
Phone 972-4-902972 [Circle 711]

MEMORY CARDS SPEED NETWORK TEST UNITS

A network analyzer from Anritsu Corp. features a memory-card capability that allows users to store complex measurement programs so they can respond quickly to production-line changes.

The MSD3401A handles clock rates from 10 Hz to 30 MHz and is intended mainly for production testing of electronic components. It handles tests 10 times faster than the company's comparable predecessor network analyzer.

The instrument also offers an automatic scale function that simplifies production-line measurements. The MSD3401A is available now; price depends on the importing country.

Anritsu Corp., 5-10-27, Minamiazabu, Minato-ku, Tokyo 106, Japan.
Phone 81-3-446-1111 [Circle 712]

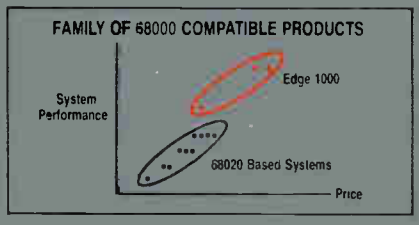
68000™ FAMILY UPDATE

AUGUST, 1987

COMPUTER DESIGNER HOLDS KEY TO 68000-FAMILY SYSTEM MARKET GROWTH

OEMs and System Integrators designing their systems around microprocessors in the 68000 family now have a cost-effective low-risk expansion path into the high performance market arena. By implementing the Motorola 68000 family instruction set in CMOS VLSI gate arrays, Edge Computer Corporation has set in motion a continuum of 68000-compatible computing. Current Motorola customers can economically add a high-end system to their product family almost immediately—without compromising software compatibility. By adapting a new design element concept now available from Edge Computer Corporation, OEMs, and SIs can offer their customers more than 11 sustained MIPs performance, 30MB/sec I/O bandwidth, 64MB of main memory, GSX (AT&T™ UNIX™ V.2 with Edge and Berkeley enhancements), 38 8″ disk drives, and 500+ user capability.

Equally important, the modularity of the Edge design element (which is offered at a more sophisticated completion level than merchant chips), allows customers to add value (peripherals, controllers, software, etc.) in those areas that are most profitable. The Edge design element insures the current Motorola customer continued software compatibility and performance growth without costly architectural redesigns.

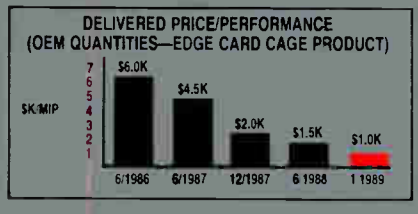


MOTOROLA CISC INSTRUCTION SET MACHINE WITH RISC-LIKE EFFICIENCY

The best performance features of CISC and RISC have been combined to produce a SIP (Streamlined Instruction Processor). At 1.5 Cycles Per Instruction, the new processor, developed by Edge Computer Corporation, has a lower AIT (average instruction time) than any current CISC or RISC system. Furthermore, Edge delivers RISC-like performance without the "risk" of 68000 software incompatibility. Edge's performance and compatibility advantages result from an advanced CMOS VLSI implementation of a Harvard supercomputer architecture that simultaneously fetches instructions and operands over multiple 32-bit buses. The high-performance dual 4-staged pipelined processor is specially designed to execute 68000 family instructions extremely efficiently. In fact, most instructions are executed in one cycle.

1 MIP PER $1K SYSTEM PERFORMANCE BEFORE 1990

As the chart indicates, Edge Computer Corporation has already lowered the high cost of high performance computing. But the company is equally dedicated to the future needs of its customers. Edge's continuum of compatible computing strategy will not only guarantee sustained 68000 family software compatibility, it will enable the OEM to economically capitalize on the market's ever-growing demand for increased number of users and computational power. Before 1990, prices for Edge technology (in OEM quantities) will have been cut to $1K per MIP. OEMs will be assured the winning edge essential to their profitability, even the future, of their companies.

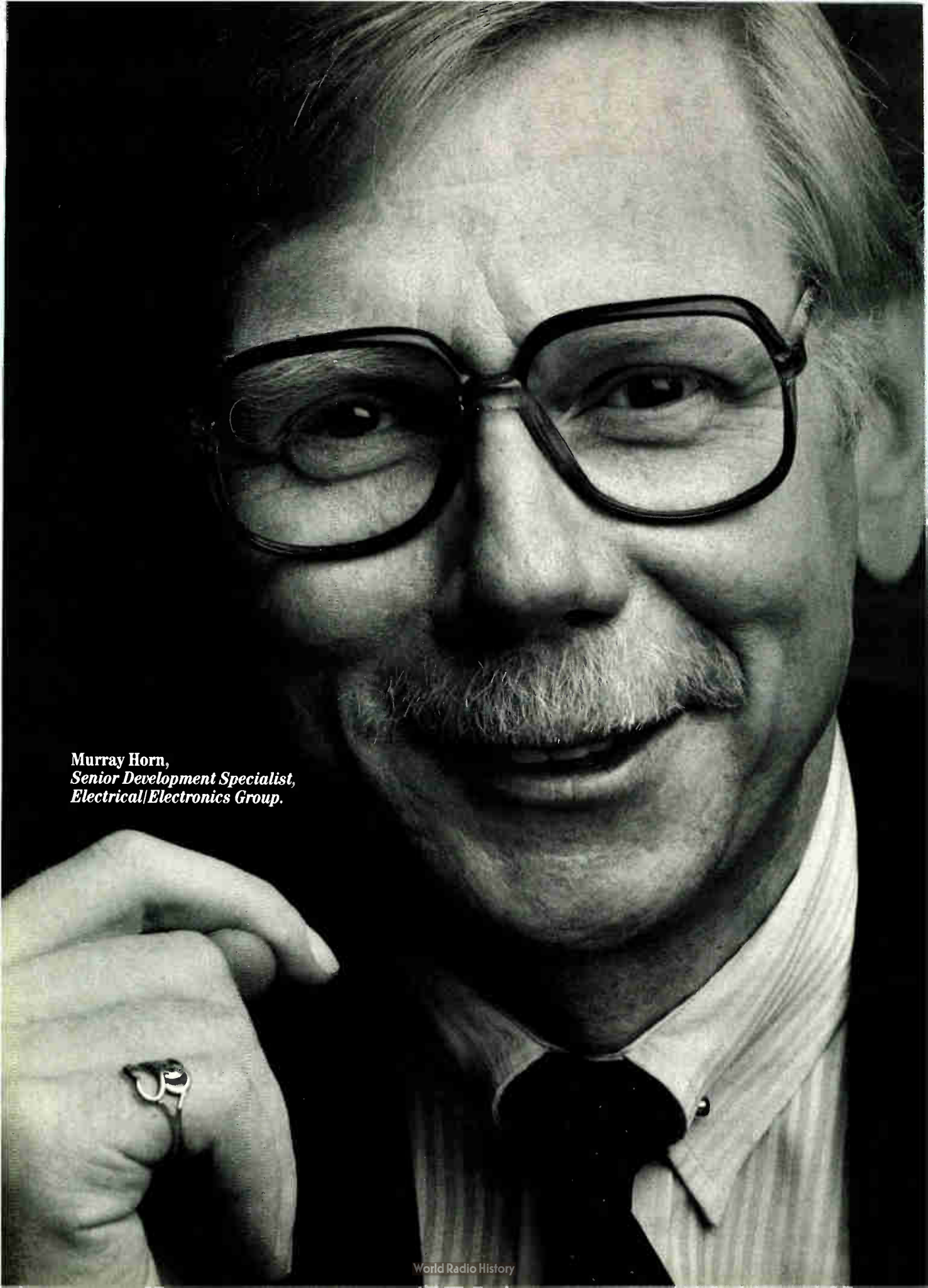


EDGE COMPUTER

Compatible With Your Future

For more information on how Edge's Continuum of 68000 Compatible Computing can give your product family the Winning Edge today and tomorrow contact: Pamela Mayer, Edge Computer Corporation, 7273 E. Butherus Drive, Scottsdale, AZ 85260, 602/951-2020. European Sales Office: 5, Avenue des Jordils CH 1000 Lausanne 6 Switzerland

Circle 55 on reader service card



Murray Horn,
Senior Development Specialist,
Electrical/Electronics Group.

"It's hard for me to take no for an answer...

I know you can't win 'em all...but that never stopped me from trying.

...like the first time I met Fred, I almost didn't...he was too busy to see me, so I suggested we meet in the lobby...five minutes tops.

...he came armed with big problems molding his connectors, lots of technical questions, and very little time...I came with samples, product specs, everything but my technical rep...so I became tech rep for a day... I set up his molding machine...and showed him how dropping the temperature and increasing the pressure could help him mold his parts to spec.

To this day, we laugh about our three hour 'five minute' meeting...sometimes, we even meet in the lobby...just for old time's sake."

DuPont Engineering Plastics

It all starts with a phone call...(302) 999-4592

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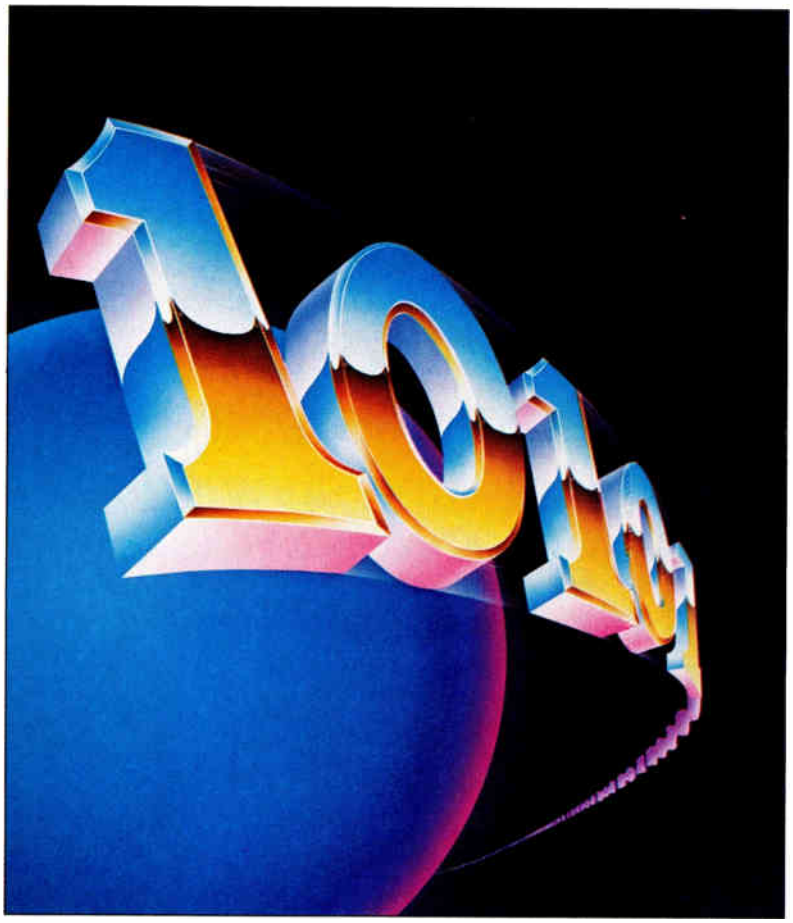

AMD's 32-bit chip uses an enhanced RISC design to run at a sustained performance level of 17 mips; it can hit a peak execution rate of 25 mips.

AMD Develops The Fastest, Most Powerful 32-bit CPU.

"In the high-stakes race to produce ever-faster microprocessors, AMD is about to blow past the rest of the field with the first microprocessor ever designed by the company. Using an enhanced RISC design, the Am29000 stakes a claim to the title of the world's fastest 32-bit μp. The company regards the new microprocessor as its most significant product in a decade.

AMD thinks its μp can be a formidable contender against the swelling ranks of RISC-based chips. The company believes the chip can outrun a whole host of similar products: the popular RISC chip set from MIPS Computer Systems; the Clipper 32-bit μp from Fairchild; and upcoming releases reportedly on the way from DEC and IBM..."

Excerpted from an exclusive article in the March 19, 1987 issue.

McGraw-Hill Electronics

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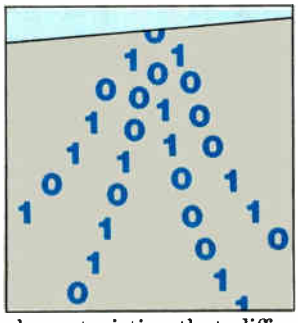
INSIDE TECHNOLOGY

SCSI IS PUSHING PCs INTO THE WORK-STATION MARKET

New high-speed controller chips for the Small Computer Systems Interface boost PCs into the work-station realm with fast, low-cost disk input/output

by Jonah McLeod



The arrival of fast chips for implementing Small Computer Systems Interface controllers is promising to vault PCs into territory held by low-end work stations—without exacting a big price premium from the user. One of the few remaining performance characteristics that differentiate high-end PCs from work stations is the rate at which a personal computer can move data to and from its hard-disk drive. Top-of-the-line PCs have lots of computing muscle, but they have lacked the fast input/output channel for disk access that makes a work station hum in multitasking and networked environments.

Apple Computer Inc. was the first big PC maker to tap SCSI for disk I/O, in its high-end Macintosh products. Apple's choice of SCSI has been a big boost for the SCSI-chip market, where very high growth rates are being seen (see chart). The optimistic projections of ongoing meteoric market growth assume that IBM Corp. will also adopt the SCSI standard for its new PS/2 line of PCs. Sources say that IBM is seriously considering SCSI. Healthy disk-I/O performance becomes especially important in keeping PCs on their toes as true multitasking operating systems place their big disk-transfer burdens on the system.

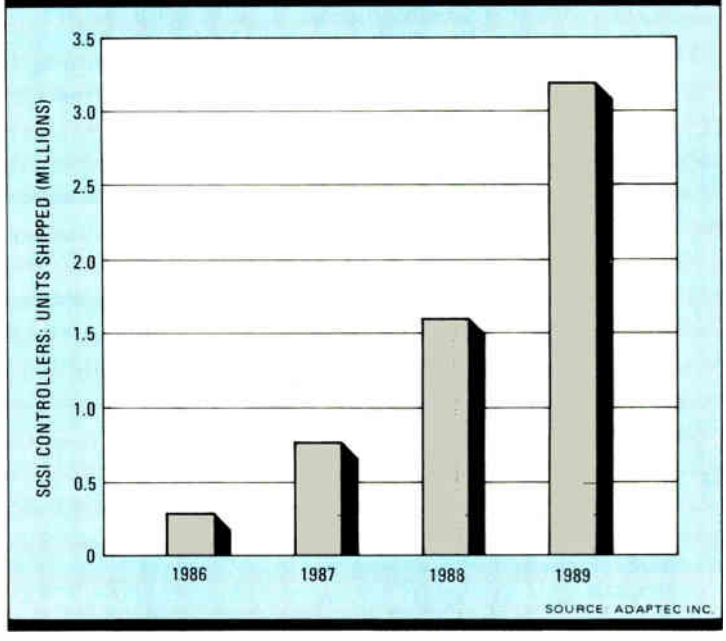
The strong market prospects are attracting a number of chipmakers, who are introducing chips that will replace fast but expensive board-level implementations of a SCSI controller. Adaptec (see p. 61), Western Digital (see p. 64), Emulex, NCR Microelectronics, and Logic Devices [*Electronics*, Aug. 6, 1987, p. 110] are all betting on this burgeoning market.

SCSI evolved under the care of the American National Standards Institute, beginning as the Shugart Associates System Interface in 1979. ANSI work made the interface more universal, able to handle more kinds of peripheral devices than just hard disks. Read-only and other types of optical disk drives can be accommodated, for instance, as well as tape drives, printers, scanners, and other input and output devices.

The principal difference between the SCSI bus and other interfaces designed for disk drives, like the ST-506 interface and the Extended Small Device Interface, is that SCSI is a system-level interface, and the others are all device-level interfaces. This means that for every new device, such as a bigger disk drive, the interface between ESDI or the ST-506 interface and the computer's system bus will likely have to be redesigned. But from the system's point of view, a SCSI bus remains unchanged no matter what the characteristics of the devices that are tied to it.

So companies whose systems carry SCSI interfaces, like Sun Microsystems and Apple Computer, can quickly drop in new disk drives and other peripherals as they appear on the market with

THE MARKET FOR SCSI CHIPS IS SET TO BOOM



SCSI interfaces built in. Companies using device-level interfaces, such as Apollo Computer and IBM, have a lot more time-consuming work to do for each new peripheral they want to offer.

The disadvantage of SCSI is that it has been costly to achieve performance parity with device-level interfaces, because the interface's generality results in a handshaking overhead penalty during

Early SCSI implementations moved data at a slow 200 Kbytes/s, but chips now coming on the market are pushing speeds to 5 Mbytes/s—the SCSI maximum

operation. With the arrival of high-speed SCSI controller chips, however, it appears that the cost of overcoming SCSI's performance penalty is dwindling. Thus SCSI, with its flexibility advantages, is looking more and more attractive.

Early low-cost SCSI implementations in PCs do not fulfill SCSI's full promise: data-transfer rates of less than 200 Kbytes/s are typical. Apple has now pushed its SCSI rate to 1.4 Mbytes/s. Chips coming on the market now, however, will help push data-transfer rates on the SCSI bus to 5 Mbytes/s, the SCSI maximum.

The worldwide market for SCSI chips and boards is expected to grow at a 100% rate through the end of 1989, believes G. Venkatesh, manager of the IC Product Line at Adaptec Inc. in Milpitas, Calif. Market research done by Adaptec, which claims 80% of the SCSI controller chip market, indicates that the industry shipped 300,000 SCSI interfaces, including drives and controllers, in 1986. Over half of the 800,000 SCSI interfaces Adaptec expects to be sold in 1987 will be for drives shipped in Apple Macintosh computers, Venkatesh says.

However, continuation of this growth rate is based on the assumption that IBM Corp. will be a major consumer of SCSI chips. Although IBM has announced no SCSI-based PS/2 products, the assumption has strong logic behind it. IBM has a problem when potential customers compare its PS/2 models, whose ESDI disk controllers can handle only 1.2 Mbytes/s, with Apple's Macintosh II. The Mac's current 1.4 Mbytes/s doesn't represent a big lead, but a card could be plugged into a slot in the Mac's NuBus that implements a SCSI interface running at 5 Mbytes/s and bursting blocks of data into main memory at 10 Mbytes/s. This gives Apple the potential for work-station-level performance that IBM cannot match with its current PS/2 products.

IBM has not announced any plans to incorporate a SCSI bus into a PS/2 motherboard, as Apple has with the Mac, but an IBM spokesman does point out that a SCSI card could be plugged into a PS/2 system's Microchannel bus, where transfer rates of 20 Mbytes/s and higher can be achieved.

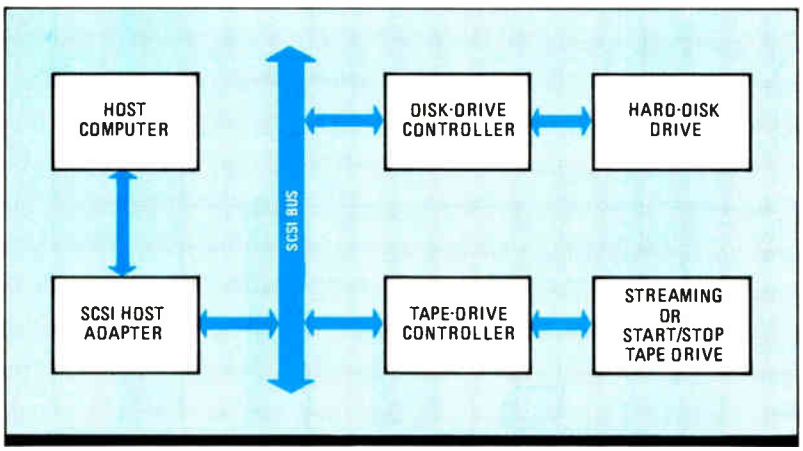
Multitasking operating systems, such as IBM's upcoming OS/2, make many more disk accesses than a single-tasking operating system, placing heavy demands on disk I/O. They are a big reason for SCSI's popularity. Moreover, when an application program requests a sector of data from disk, the operating system typically transfers more than one sector into main memory to anticipate a request for the next sector—another burden for the controller chip to bear.

The latest generation of SCSI chips get their performance improvement from sophisticated state machines or high-speed embedded microprocessors that perform the overhead processing for each SCSI bus phase. In the past, up to 10 ms was consumed in overhead between the time the host requested an operation from a peripheral and the time the operation was completed. An external microprocessor on the host moved the bus-transfer process from one phase to the next; the performance drag came from having to interrupt the microprocessor to process each phase.

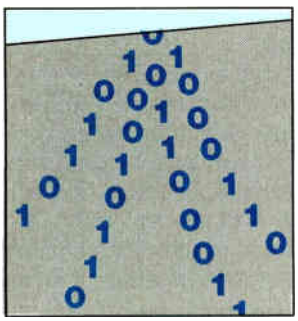
Adaptec and Emulex Corp., Costa Mesa, Calif., have built high-speed state machines into the SCSI chip to handle the bus-phase processing. And NCR Corp.'s Microelectronics Division is selling a version of Emulex' SCSI Processor as the NCR 53C300.

In its latest SCSI chip, Western Digital Corp., Irvine, Calif., cut command overhead by reducing the number of interrupts issued to the microprocessor overseeing the SCSI controller's operations. The company built into the SCSI chip a microprocessor and firmware that cut overhead time to 0.5 ms.

All the new chips can connect a host computer bus to the SCSI bus (see figure). The chips also make the connection between the device-level interface used by the disk or tape drive and the SCSI bus. The Emulex chip has for the first time increased SCSI bus throughput up to 5 Mbytes/s at the 20-ft. bus-length limit set by ANSI. Other chips on the market allow 4- to 5-Mbyte/s transfers at cable lengths under 1 ft. □



FLEXIBLE BUS. Eight varied peripheral devices can be tied to one SCSI bus; SCSI controller chips provide interfaces on both the host and peripheral sides of the bus.



ADAPTEC'S DISK CONTROLLER SETS SCSI SPEED RECORD

The AIC-6250 gives a 500% boost in host input-output performance, using its 16-bit-wide data path to hit a 20-Mbyte-per-second transfer rate—the first SCSI chip to do it

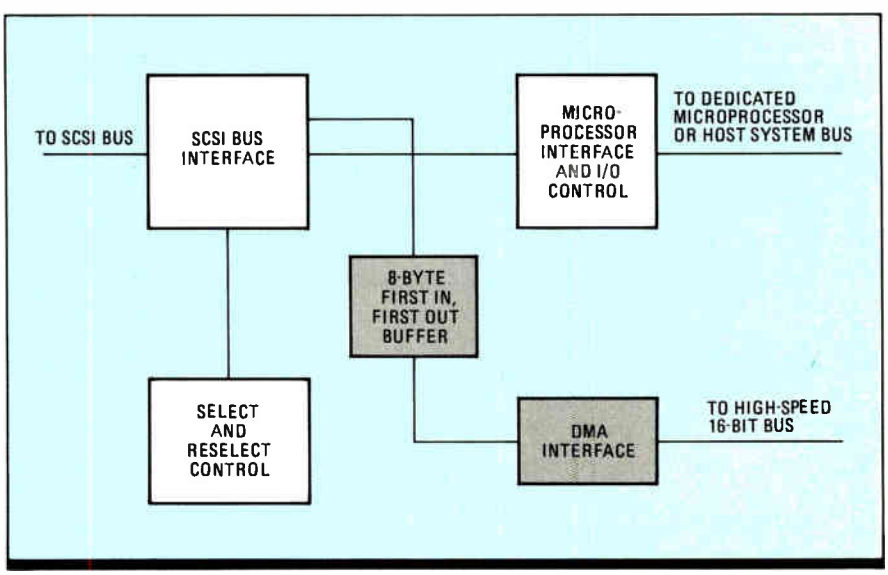
by Jonah McLeod

Personal computers are rapidly closing the performance gap separating them from more expensive low-end Motorola 68020-based work stations. The buses of both IBM Corp.'s Personal System 2 and Apple Computer Inc.'s Macintosh II, for example, can transfer data at more than 20 Mbytes per second. Yet both models still come with disk controllers that can't transfer data across this high-speed bus at more than 2 to 3 Mbytes/s. The reason for this lower transfer speed—which is the main reason why PCs still don't measure up to work stations in performance—is the lack of an inexpensive disk-controller chip that could interact with the computer bus at the bus's maximum transfer rate.

PC makers now have a solution to this problem. Adaptec Inc. is introducing a Small Computer Systems Interface chip that the Sunnyvale, Calif., company says is the first of its kind to achieve 20-Mbyte/s operation with the host computer bus. Up to now, most existing SCSI controller chips could manage no more than 4 Mbytes/s on the host computer bus, so the AIC-6250 SCSI Protocol chip provides a 500% increase in host input-output performance. This will enable a PC, with its bus and SCSI controller chip both operating at a 20-Mbyte/s transfer rate, to provide performance equal to that of a low-end work station.

The AIC-6250 should help push SCSI toward high-end applications. Originally designed as a low-cost interface between a computer and a peripheral, SCSI has generally been used in PCs—the low-cost end of the computer spectrum. But as designers figure out ways to get more and more speed out of the interface—the AIC-6250 being a prime example—it increasingly will enable PCs to perform more high-end applications (see p. 59) and will be used in more powerful systems, such as work stations.

The impact of the AIC-6250 will be heightened by its price—$20 each in lots of 1,000, inexpensive enough to be used in virtually any PC system design. Small quantities are available now; Adaptec expects production to ramp up in the last



1. ON THE BUS. The AIC-6250's bus interface handles getting on and off the SCSI bus; a microprocessor interface and I/O-control function routes command packets to and from the bus.

quarter of this year. When it does, the chip should open up a far greater range of high-performance SCSI operations. Previously, a system designer who wanted to get more performance out of SCSI had to create his own printed-circuit board, adding anywhere from $200 to $500 to the system's cost.

To achieve high peformance, the AIC-6250 (see fig. 1) is the first SCSI chip to offer a 16-bit-wide data path for connecting to host computer-system buses. "Competitive chips have 8-bit data paths," says Jeffrey Miller, vice president of marketing at Adaptec. "Designing these chips into an 80386- or 68020-based system with a 16-bit bus requires circuits external to the chip to convert from an 8- to 16-bit data path."

The three buses permit multitasking—two can transfer data between the host and peripherals while the third helps to configure another transfer

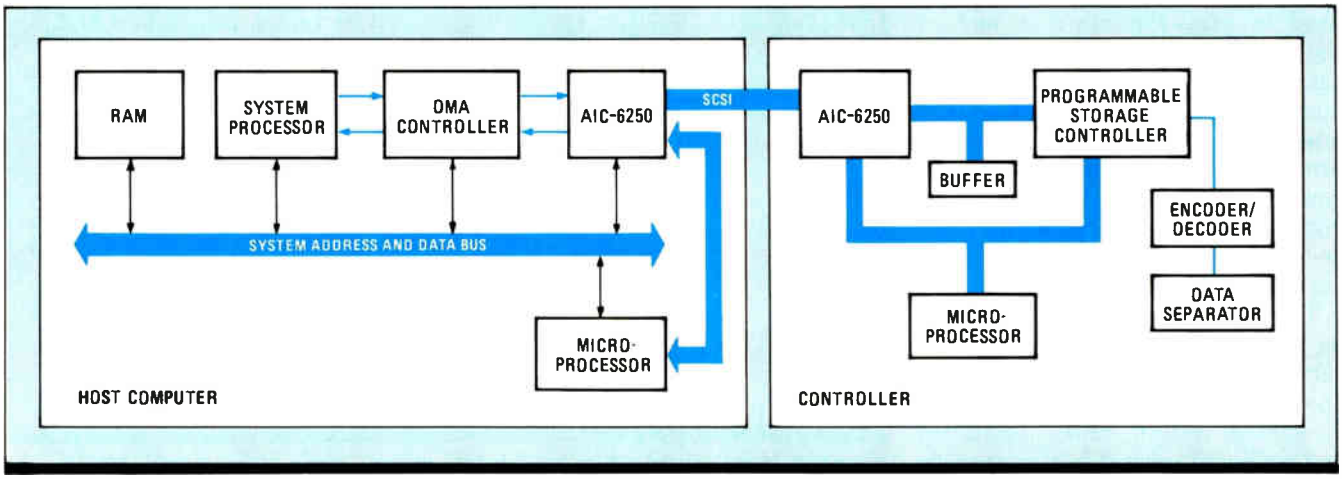
Also, the AIC-6250 is the first chip to offer three bus connections: the 16-bit data port, for connecting to the host computer system bus; an 8-bit data port for connecting to the SCSI bus, and an 8-bit control port to allow the host computer to communicate with the chip, even when a data transfer is occuring on the other two buses. Other SCSI chips currently available provide only an 8-bit data port to the host computer and an 8-bit port to the SCSI bus. In addition, the AIC-6250 is the first SCSI controller that can operate with a 20-MHz external clock; all other chips now handle only a 10-MHz external clock.

The three I/O buses on the chip permit multitasking operation—they allow more than one task to be processed at once. Two can transfer data between the host computer and peripherals, while the third can provide concurrent communications between the host CPU and the chip to configure yet another transfer. "Up to now, because other chips have no separate data path to their SCSI controller chip, if the CPU wants access to the SCSI chip, it has to halt any ongoing data transfer," says G. Venkatesh, manager of Adaptec's IC product line. "The sustained data rate on the CPU bus goes down. We get around the problem by having the separate data path for the host CPU to access the SCSI controller chip while a data transfer occurs on the other two buses."

At any time, all three buses can be active, because each is being driven by entirely different, autonomously operating elements in the system. To accommodate all three buses, the chip performs the bus arbitration operations for all three buses automatically, and in real time. To bring order to I/O operations, a priority scheme was established by the SCSI specification. Up to eight devices can be on the SCSI bus. Each is assigned a logical unit number, with seven being the highest and zero the lowest. The host CPU usually has the highest priority, so it can always access the SCSI bus. Next in priority is typically the disk controller, with logical unit 6. Peripherals such as a tape controller are usually given the lowest priority, logical unit 0.

The AIC-6250 achieves its fast system throughput by implementing all the functions needed to provide an initiator or target by a host computer system and any peripheral device on the SCSI bus. SCSI protocol requires that an initiator select a device to perform some operation—read, write, seek, and so on. The selected device becomes the target. Once the target has been selected, it carries out the rest of the operations on the bus.

In a typical system configuration, one AIC-6250 interfaces between the host computer and the SCSI bus and a second AIC-6250 connects the SCSI bus and a peripheral device such as a Winchester, optical-disk, or tape drive (see fig. 2). Depending on system configuration, the controllers can operate in synchronous or asynchronous mode. In synchronous mode, the chips transfer data on the SCSI bus at the maximum rate of 5 Mbytes/s. In asynchronous mode, they transfer data at a maximum rate of 3 Mbytes/s. "Mainframe I/O channels typically



2. INTERFACING. Typically, one AIC-6250 interfaces between the host and the SCSI bus and a second AIC-6250 connects the bus and peripherals.

run at 3 Mbytes/s, and with bus contention it is much lower than this," Miller says.

That speed makes the AIC-6250 faster than the transfer rates of most 5¼- and 3½-in. disk drives used today in work stations and personal computers; their top speed ranges from 930 Kbytes to 1.2 Mbytes/s. It does not, however, mean the chip is far faster than it needs to be. For one thing, the coming generation of drives will be considerably faster—the new 760-Mbyte EXT 8760 from Maxtor Corp., in San Jose, Calif., for example, has a 1.9-Mbyte/s transfer rate. Some 8-in. Winchester drives already offer 2.5- and 3-Mbyte/s rates.

Also, newer drive designs incorporate a cache that can contain upwards of a full track of data. "If the computer requests data from the disk that is already in cache, the SCSI controller chip can access data from the cache and transfer it at the full 3-Mbyte or 5-Mbyte/s transfer rate of the SCSI bus," says Venkatesh. "The AIC-6250 can serve this application today."

The reason for driving the SCSI bus at 5 Mbytes/s is the same as the reason for driving the host CPU bus at 20 Mbytes/s. "In complex systems, there can be multiple devices sitting on the system bus—a DMA controller, SCSI controller, Ethernet, and so on," says Miller. "The faster a disk drive can access the bus, make its transfer, and get off, the faster the overall system throughput will be."

Because the AIC-6250 chip can handle a data transfer at up to 20 Mbytes/s, it can also accept the relatively slow 90-Kbyte/s transfer rate of a tape drive on the SCSI bus, store up to 8 bytes at a time, and then burst 8 bytes across the system bus at 20 Mbytes/s.

The 6250 transfers data at 20 Mbytes/s when the system connects to a computer with a 16-bit data bus. A microprocessor interface and I/O control function serve to route command packets to and from the SCSI bus and to and from a microprocessor on the peripheral controller or host computer.

Unlike other SCSI controller chips, most of which were designed for controlling a peripheral device on the SCSI bus, the AIC-6250 was also designed to control host computer access to the SCSI bus. When the AIC-6250 is connected on the host side of the SCSI bus, it can receive SCSI command packets directly from the host CPU, which is the case with most PC implementations. Or the system can be designed with a separate microprocessor dedicated to handle the I/O channel—typical of a work-station design.

Inside the chip, a direct-memory-access counter also allows the chip to transfer up to 16 Mbytes of data without requiring the host CPU to become involved. To move such a large amount of data, the host CPU issues the SCSI commands to effect the transfer. The AIC-6250 on the host side sets up to perform the transfer by sending a command to an AIC-6250 connected to, say, an optical disk. The two then begin transferring bytes across the SCSI bus. A counter inside the chip sending the data counts down with each byte transferred. Its maximum count is 16 million. To support the two most popular microprocessor buses, those of the 8086 and 68000 families, the chip has two addressing schemes. With one pin on the 6250, the host system can identify itself as a multiplexed or separated address and data bus, and the chip can configure itself to operate accordingly. □

For more information, circle 480 on the reader service card.

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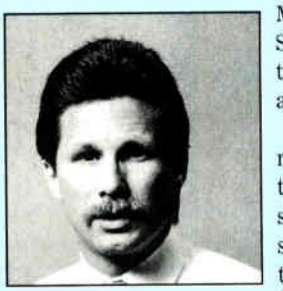
ADAPTEC BROADENS THE ROLE OF A SCSI CHIP

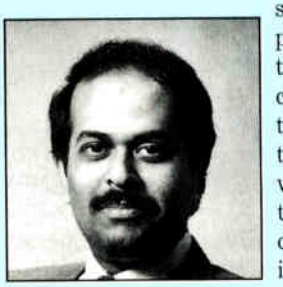
Since its inception, the Small Computer Systems Interface has imposed a speed limit on system buses of 5 Mbytes/s—the speed at which data can be transferred on the SCSI bus. But the Adaptec Inc. team that designed the AIC-6250 SCSI Protocol Chip realized it could raise the speed limit by accelerating the data as it came off the SCSI bus and hit the high-speed system bus. It did that by developing a fast chip that works on both the system and the peripheral side of the SCSI bus to move data quickly.

"We knew from the start that the chip had to operate equally well on both sides of the SCSI bus and that it had to have separate interfaces for both the SCSI and the host buses," says Jeffrey Miller, vice president of marketing at Adaptec.

To achieve the necessary levels of performance in its chips, Adaptec involved its system designers in the final design of the 6250 chip. "They pointed out where the bottlenecks were in the design," Miller says. Getting designed into both the host computer side of the SCSI bus—especially by leading computer manufacturers—would convince a lot of drive manufacturers to design the chip into their embedded SCSI drives as well. "By dropping the chip onto both sides of the SCSI bus, a system designer gets the fastest possible throughput: 20 Mbytes per second on the computer bus, and 5 Mbytes per second on the SCSI bus," says G. Venkatesh, IC product line manager at Adaptec.



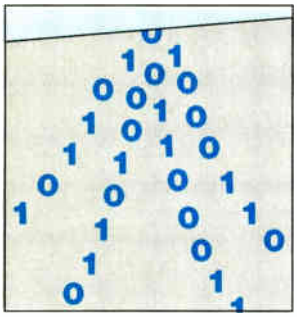
JEFFREY MILLER



G. VENKATESH

One of the problems remaining with SCSI—one that tends to encourage system builders to use the same chip on both sides of the bus—is that the interface specification is still subject to individual interpretation by chip manufacturers. "But the system customers want a solution that optimizes overall throughput. They don't want to deal with inconsistencies between different chip manufacturers' SCSI implementations," Miller asserts.

WESTERN DIGITAL SLASHES SCSI BUS OVERHEAD TIME



Western Digital Corp. is about to slash the overhead time it takes to get on and off the Small Computer Systems Interface bus by more than half. An enhanced A version of its WD33C92/93 promises to cut the time for hopping on and off the bus to as low as 0.5 ms. The original WD33C92/93, now more than a year old, is a second-generation SCSI controller chip that took 1.2 ms, compared with 5 ms or more for the first generation of all SCSI parts.

The Irvine, Calif., company achieved the reduction by increasing the clock rate of the chip from 8 MHz to 16 MHz and optimizing the microcode of the on-chip microprocessor for better SCSI protocol management. In the first Western Digital version, some high-level commands implemented in the microcode had been combined, reducing their number, compared with other SCSI parts. The optimization combines still more commands and eliminates others. As before, the high-level commands handle all SCSI bus control, says Brad Masters, manager of LSI product development for storage management, but the controller now operates even faster, since the need for interruptions by a host computer is further reduced. The company also added various other enhancements. It enlarged the number of bytes the chip can send in a burst over the host bus from 5 to a maximum of 12—in effect, increasing the direct-memory-access bandwidth—and implemented parity checking on both the SCSI and host buses.

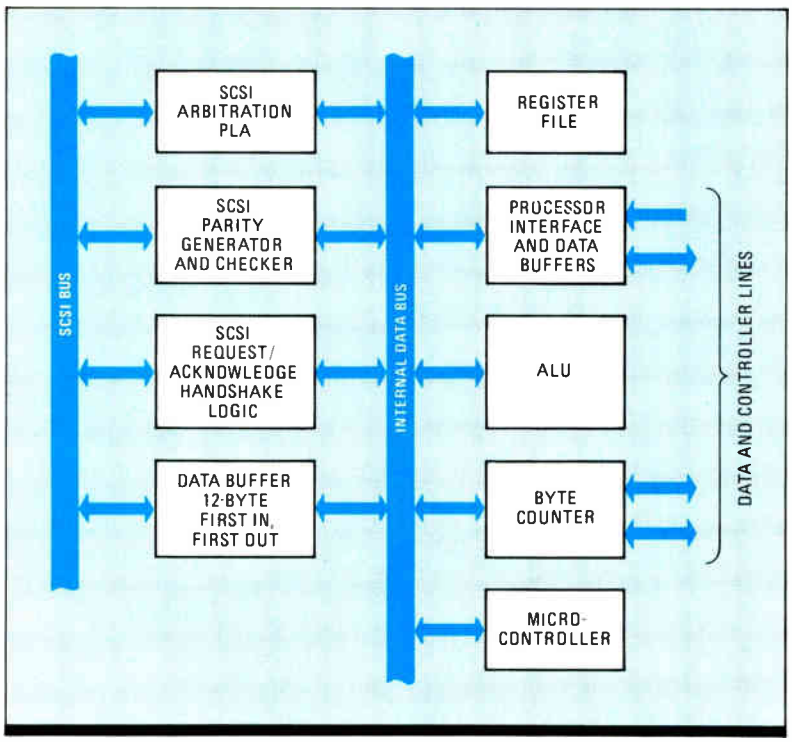
Speed has been increased across the bus. Although both the old and new version of the SCSI chip can act as a bus master or a bus slave on a host bus, the original version acting as a bus slave could transfer data no faster than 2.5 Mbytes/s, compared with 4 Mbytes/s acting as master. As a bus slave, it had to function with another chip on the host bus, a DMA controller. After getting a request for a byte transfer from the DMA controller, the chip would send a byte and an acknowledgement that it had sent the byte. The new version of the chip, by contrast, can burst several bytes across the bus in response to the DMA controller's request. It follows the burst with a single acknowledgement—speeding up the process to 4 Mbytes.

But in Western Digital's approach to SCSI, the transfer rate on the bus is a secondary consideration. Low bus overhead is more important, since the SCSI specification limits transfer rates to 5 Mbytes/s in any case. Improvements, in Western Digital's view, must come through more efficient SCSI protocol management.

The 92/93 controller chip (see fig. 1) implements full SCSI bus features: arbitration, disconnect, reconnect, parity, and synchronous data transfers. The device is designed to meet handshaking and communications requirements over a wide range of SCSI bus applications. These range from simple data transfers using a single drive to interleaved multiple-device communications. The 92-option version needs external amplifiers to connect with the SCSI bus, whereas the 93 has internal 48-mA drivers, allowing direct connection to the SCSI bus. This distinction continues with the enhanced chip.

The controller chips are fabricated in a CMOS 3-μm process and operate from a single 5-V supply. Geometries will drop to 1.25 μm sometime in the next year, when AT&T Corp. starts building the SCSI controller family, under contract with Western Digital. The scaling down should boost the chip's performance considerably. Samples of the 3-μm chip are available now. In quantity, its price will be $18.50, compared with $16.50 for the original version.

The key to the performance of both the original and the enhanced version of the controller is its on-chip processor. For the most part, competing chips lack onboard computing—they use a separate processor dedicated to protocol control functions, in



1. FULL FEATURES. The WD33C92/93A implements the full range of SCSI bus features, including arbitration, parity, and synchronous data transfers.

both host systems and peripheral equipment, says Richard E. Rutledge, product manager for the line.

Employing the on-chip processor for overall control permits bundling operating microcode into high-level command procedures that streamline protocol management. With the high-level commands, bus overhead is kept to a minimum, so overall throughput of SCSI-based systems, or the number of SCSI instructions executed in a given period, can be maximized. "That's what we bring to the SCSI party," says Masters.

In the enhanced version, the microprocessor is faster, thanks to its higher clock rate of 16 MHz; the first version of the chip had a clock rate of 8 MHz. The higher speed has no effect, for all practical purposes, on data-transfer speeds. Both the old and new versions can be divided to allow a 4-Mbyte data-transfer rate on the SCSI bus.

Western Digital's reduction of bus overhead to 0.5 ms comes from reworked protocol management. For every operation that occurs over the SCSI bus—read, write, and so on—there is a prescribed protocol that both the devices involved in the operation must follow. An initiator—the central processing unit, for example—wants data from a disk drive. It arbitrates for the SCSI bus, gains control, and then selects a target device to provide the data. Once the initiator has selected a target, the target takes control and carries out all remaining operations to complete the transfer. The target initiates a command transfer phase in which it reads a SCSI command packet from the initiator—CPU memory in this example—into the target's memory.

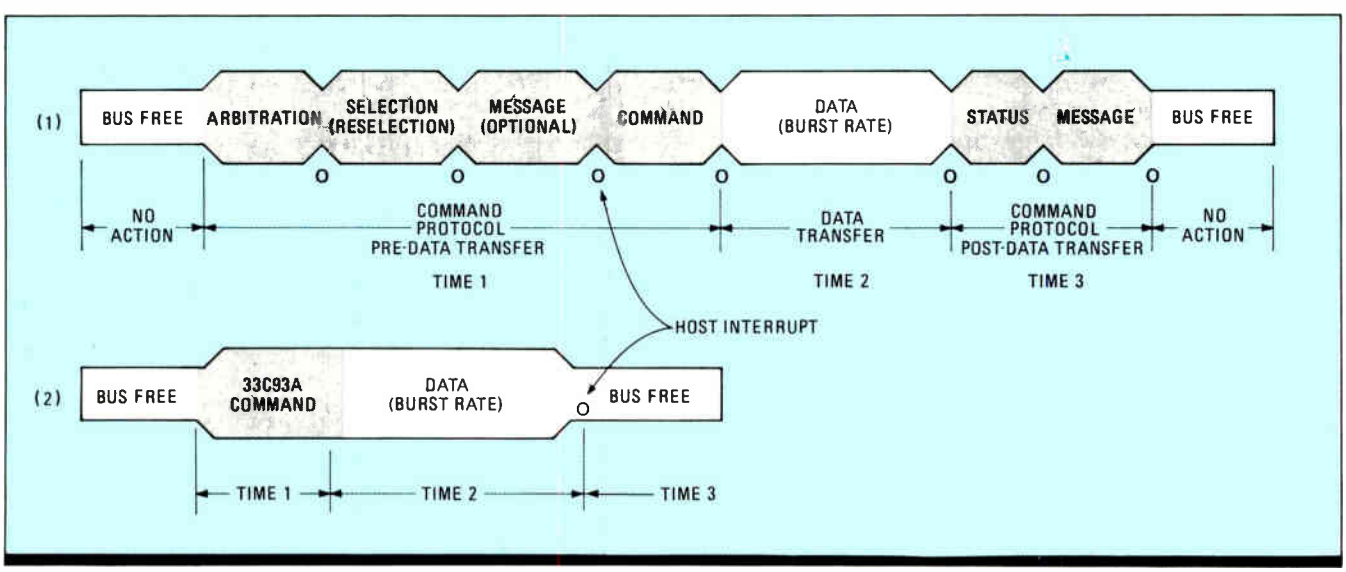
The target decodes the SCSI command and determines what operation to perform. The target then goes into a data phase, in which it acquires the desired data and transfers it to the random-access memory of the CPU. The target next enters a status phase to receive a status message from the CPU telling it if the transfer was completed successfully. If it wasn't, the target goes into a message phase to find out, for example, the cause of the faulty transfer. Finally, the target initiates a bus-free phase.

The total time it takes to carry out all of these phases is the overhead that Western Digital is now reducing to 0.5 ms. One way the company achieved this reduction was the higher clock rate; a second way was to group the phases together into sequences. In first-generation SCSI chips, each phase required an interrupt to the host CPU, a time-consuming operation. In the original version of the Western Digital chip, the chip performed several phases together before an interrupt was required. In the A version, the company has added new sequences and provided the capability to string sequences together (see fig. 2).

Rutledge singles out the key "Read Command with Disconnect" as a representative example of how the changes work. Eleven separate SCSI bus sequences required to carry it out are combined into two commands programmed into the chip. Using competing controllers without a high-level command structure, designers would have to write microcode for each of the individual sequences. Combining the sequences cuts bus overhead time for the command from more than 1 ms to 372 μs.

Other enhancements to the chip include a bigger data buffer, boosted from 8 to 12 bytes. The larger buffer holds more information until the SCSI bus or host is ready to accept a transmitted or received data byte. The effect of this change is to increase the DMA bandwidth. Another new feature is what Western Digital calls Thru Parity. A parity generator/checker now can check for data errors on either the host CPU bus or the SCSI bus. On the original WD33C92/93, parity was generated only for data placed onto or received from the SCSI bus. *–Larry Waller and Jonah McLeod*

For more information, circle 481 on the reader service card.



2. COMPACT. Early SCSI chips (1) put an interrupt between each phase; the WD33C92/93A (2) squeezes phases into sequences and links the sequences.

VMEBUS GETS A MID-LIFE KICKER

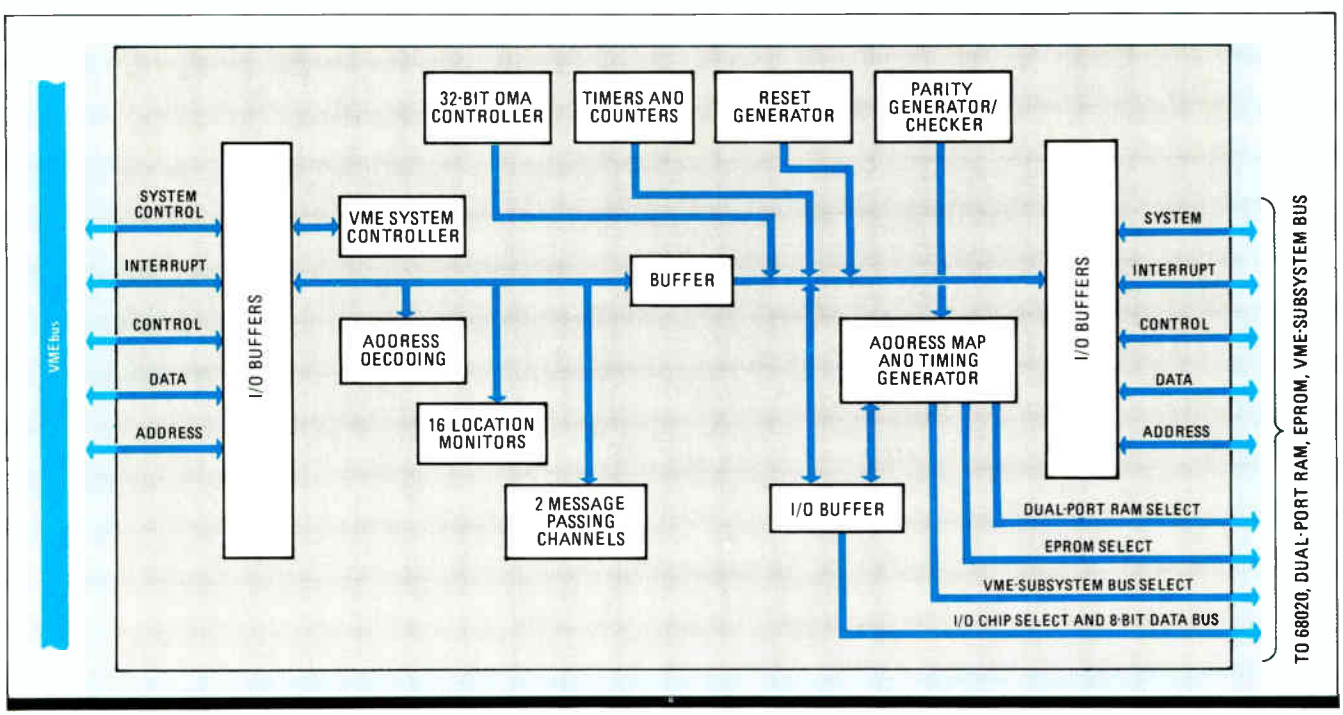
Force Computers expects its VME/Plus to move VMEbus into multiprocessing in a big way; its new message-passing VMEbus processor comes on just one board

by Tom Manuel

The VMEbus standard, currently the most popular bus system for high-performance microprocessor systems, is getting a big boost from Force Computers Inc. The Los Gatos, Calif., company is launching a new generation of 32-bit VMEbus technology that's aimed at moving the current architecture into the worlds of multiprocessing and parallel computing.

The 5½-year-old designer and producer of VMEbus products, which is the No. 2 VMEbus supplier worldwide after Motorola Inc. (see p. 69), has added message-passing to make this big move into new applications. Force has implemented the new technology, called VME/Plus, by designing a gate-array chip. In addition to message-passing, the new chip (see fig. 1) also includes a direct-memory-access controller and a dual-port memory controller, putting all of the bus-to-microprocessor interface features on-chip instead of filling up four printed-circuit boards.

The FGA-002 interface chip connects directly to a microprocessor on a single-board central processing unit without requiring any additional logic. This significantly cuts the cost and complexity of a VMEbus board. And the system still retains full compatibility with the IEEE-1014 VMEbus standard. The new technology will open up new horizons for system designers, since VMEbus systems will have board space available



1. VME POWERHOUSE. The FGA-002 VMEbus interface chip adds message passing, DMA, interface functions, and location monitors.

to add such things as multiple processors, additional memory, or more peripheral controllers.

Force Computer figures that the performance and features of its VME/Plus will enhance the competitiveness of the widely used VMEbus and extend the life cycle of the VME standard by up to a decade. "We wanted a quantum jump over the highest-performance VME products now in the market, and we think we achieved it," declares Sven Behrendt, president.

The VME/Plus technology blends multiprocessing, message passing, system control, multilevel interrupt handling, location monitoring, and direct memory access on the single proprietary gate-array chip. To make the chip, Force selected a 20,000-gate, 1.5-μm CMOS array with a 1.4-ns internal gate delay made by NEC Corp. in Tokyo. The FGA-002 chip designed by Force engineers uses about 18,500 of the available gates and is packaged in a 280-pin ceramic pin-grid array.

MAKING IT EASIER

The message-passing facilities in VME/Plus will make it far easier for system builders to support complex multiprocessing applications (see fig. 2). Multiple CPUs can freely exchange messages and share memory using the FGA-002's message passing, seven VME hardware interrupts, and 16 software-driven location monitors for additional interrupts. The location monitors, which are like 32-bit special registers that hold addresses, monitor the bus traffic for those addresses, and when finding one, direct a software interrupt to the local processor, allowing construction of many simultaneous message capabilities and status-monitoring capabilities. With 16 of these per processor board, a 21-processor system, for example, would have 336 software interrupts in addition to the standard seven VME hardware interrupts—enough to allow up to 21 processor boards on a VME backplane instead of the maximum seven processors that the standard seven VME hardware interrupts now impose.

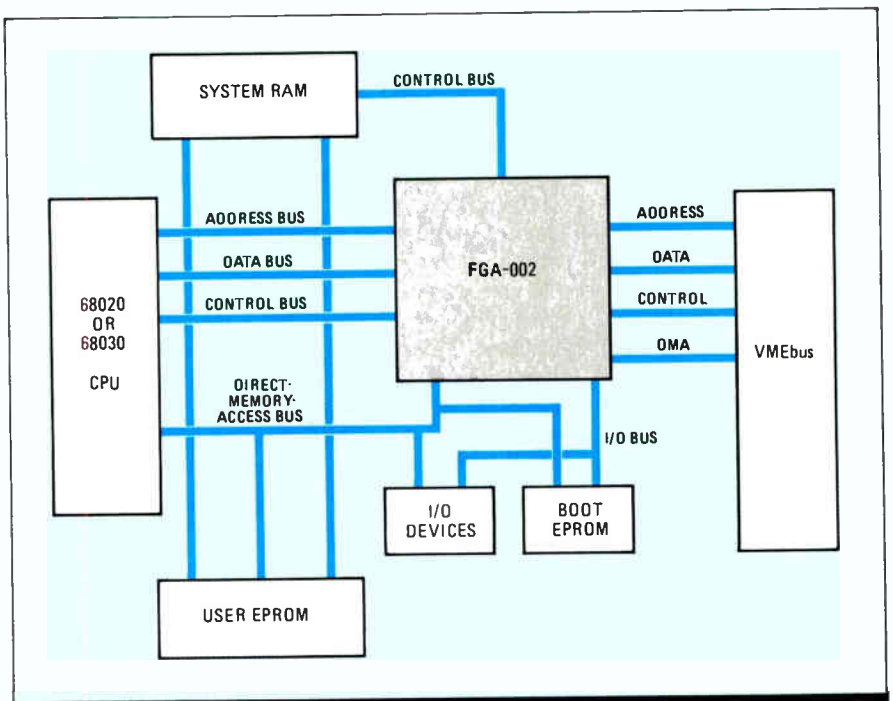
The FGA-002 also includes a 32-bit software programmable DMA controller—the first DMA controller for the VMEbus. In addition, the gate array contains the complete standard VMEbus master and slave interfaces for control of CPU-to-bus transfers and memory accesses. There was even room on the chip for a controller for dual-port random-access memory.

Along with the VME/Plus technology and the FGA-002 gate array that implements it, Force is introducing its first product using this technology. The CPU-22/23 (see fig. 3) is a message-passing computer engine with a 68020 microprocessor running at 16.7 or 20 MHz. The processor, gate array, dual-port memory, and bus drivers are mounted on a high-density board, using surface-mount-technology, in the standard VMEbus form factor.

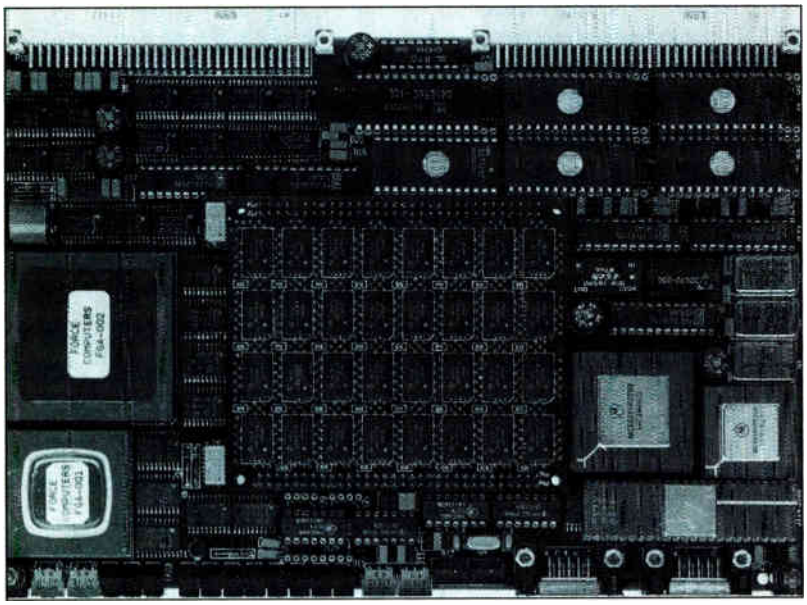
Message passing and multilevel interrupts are crucial to multiprocessing systems. The idea of message passing is to permit any processor at any time to broadcast status, data, interrupt, or other messages to a set of other processors in the system. The Force message-passing scheme allows any CPU acting as master to broadcast an 8-bit message to up to 20 other processors on the same bus at the same time. Each FGA-002 has two independent 8-bit message-passing channels, each with an 8-byte first-in, first-out buffer for storage. Two channels allow each CPU to receive and send messages simultaneously.

Just as the passing of messages among CPUs makes multiprocessing possible, a complex interrupt-management structure is also required, to keep the various processors doing the right things at the right time. The FGA-002 handles a total of 37 different interrupt requests, each providing software programmable levels and an interrupt vector or external vector fetch.

Location monitors are used to force an interrupt to the CPU on the board. These are done by software if a specific address on the VMEbus is forced. Because each of the 16 location monitors on the FGA-002 chip is provided with its own interrupt vector for the local CPU, these monitors are able to interrupt it. The location monitors allow user programs to trigger any board in the whole VMEbus system individually because the



2. SIMPLIFIER. A typical application of the FGA-002 would only need to add a 68020 or 68030 microprocessor, system memory, and EPROM chips to complete a VMEbus processor board.



3. HOT SHOT. The FGA-002 chip goes on an 18-layer SMT board to make the CPU-22/23 compute engine.

base address of the software-programmable location monitors is the same in all the FGA-002s.

Besides adding more features to its VMEbus chip, Force has eased the interface requirements all VMEbus system builders must provide. It collects virtually all the VMEbus glue logic onto one chip and also provides an electrical interface to outboard driver chips on heat sinks close to the board's connectors, an IEEE-1014 requirement.

To handle the necessary memory-addressing and access cycles to and from the local on-board portion of system memory and the VMEbus, there are two fully independent address-decoding ranges defined inside the FGA-002. The chip decodes all the address and address modifier signals. Each of the two decoding ranges are able to force and access requests to the memory. They can also be programmed to allow read-only, read-and-write, or write-only memory cycles. This allows protection of on-board memory against overwriting through access requests coming in over the VMEbus.

The FGA-002 is not connected directly to the VMEbus. Designing the gate array to drive the bus directly would have used up too many of its gates. Instead, special driver and receiver circuits connect the gate array. This technique allows direct control of these circuits to attain maximum speed. Using advanced CMOS buffers, such as the 74ACT series of standard devices from Integrated Device Technology Inc., Santa Clara, Calif., for these driver and receiver circuits reduces the propagation delay to as low as 6 ns with a drive capability of 48 to 64 mA per line.

For providing the interface and control functions for the VMEbus, the FGA-002 supports the 32 address signals, 32 data signals, and all the control signals of the VMEbus. All the VMEbus Slot 1 functions such as the single-level arbiter, power monitor, and the system reset generator are included. The on-chip bus release functions are fully programmable from the local CPU. The bus release functions that can be selected are release after timeout, release when done, release on repeat, and release on bus clear. In addition, the FGA-002 allows its local CPU to request master status on the VMEbus if no other bus request is pending.

Force is also introducing another first to the VMEbus board market: a 32-bit DMA channel in VLSI. One high-speed DMA channel is provided on the FGA-002 gate array with all the other features. This channel is capable of transferring data at speeds of up to 30 Mbytes/s over the VMEbus. The design allows real-time operation because the local CPU is fully operational while data is being transferred on the VMEbus. It will perform block transfers between the VMEbus and the dual-port memory, between the bus and secondary memory (devices attached to the VME subsystem bus or memory on the VME Memory Extension), and between the dual-port memory and VSB and VMX devices. Data to be transferred is staged or received in a 32-byte FIFO which is burst onto or from the VMEbus.

Another FGA-002 feature is a controller for dual-port static random-access memory. The dual-port architecture avoids processor stop states while permitting any two processors to have virtually simultaneous access to the same memory locations. The SRAM itself is on the board.

The CPU-22/23 message-passing compute engine, the first VME/Plus product using the FGA-002 gate array, was designed for original-equipment manufacturers building multiprocessing systems in a 3- to 15-mips range. In addition to the 68020 MPU, the new engine includes a 68020 processor, 68882 floating-point coprocessor in either the 16.7-MHz or 20-MHz versions, up to 1 Mbyte of dual-port SRAM, up to 4 Mbytes of one-wait-state erasable programmable read-only memory that is 2 to 3 times faster than standard implementations, and the FGA-002 gate array with all its features. The initial version of this CPU board also uses the prototype of the FGA-002, the FGA-001, for testing purposes—production versions, due out in the fourth quarter, will drop the FGA-001. Up to 21 CPU-22s or 23s can share one VMEbus backplane. The model CPU-22 supports the VMX secondary bus, whereas the CPU-23 supports the VSB.

The board product, which will begin shipping in the fourth quarter, uses surface-mount technology in the highest component density ever achieved on VME on an 18-layer, two-sided board. It will cost $6,475 in single quantities for the 16.7-MHz version with 256 Kbytes of dual-port RAM. □

For more information, circle 482 on the reader service card.

FORCE QUIETLY BUILDS ITS VMEBUS LINE

When a consortium of 20 companies was formed early this year to develop a control chip for VMEbus boards, Force Computers Inc. was conspicuously absent. The Los Gatos, Calif., company's absence was notable because it claims to be the No. 2 supplier of VMEbus boards, second only to the bus's inventor, Motorola Inc.

The fact that Force did not join in the effort to develop a control chip led many in the industry to suspect that the company was working on its own chip. These suspicions proved true. But instead of a control chip, Force had something else in mind: the FGA-002, the company's first chip, which is 15 times more complex than the consortium's proposed chip and integrates the functions of four VME cards (see p. 66).

"We had started our own gate-array development 18 months ago," says Force executive vice president Martin J. Weisberg. "We felt it would be dishonest to sit in on meetings of the consortium and in effect spy on them without contributing anything."

The consortium rose to counter a similar move by Motorola, which announced last January that it would develop a gate-array control chip but would not make it available to the industry. Motorola has now agreed to make its chip available to outsiders next year, but the consortium effort continues. Now that its gate array is ready, Force has offered to join the consortium and to license and sell its VME/Plus products to members of the consortium.

After all, Force was founded in 1981 by Sven Behrendt, now president, and Max Loesel, vice president of research and development, to build VMEbus products. These two executives from Motorola in Europe had been influential in the development of VMEbus there. Loesel, in fact, headed the VMEbus design team for Motorola.

Force has grown quietly, funding itself from the sale of products with no external stockholders or venture capital. It has recorded 18 consecutive profitable quarters since first turning the corner in January 1983. Rick Main of Zebu Corp., Sunnyvale, Calif., a follower of the VMEbus market, pegs the 1987 market for VMEbus boards at $300 to $325 million. "I believe that Motorola and Force underestimate the total market, making their estimates of their market shares higher than ours,"

VME/Plus should help it hold on to the No. 2 spot in world VMEbus market

says Main. Force claims about 18% of a $170 million market this year. However, Main agrees with the line-up of the major players, with Motorola as the leader and Force a clear No. 2, followed by the next seven, who are about equal. The top nine suppliers together have half of the market (see chart).

One of the reasons is what Weisberg describes as a new generation of VMEbus products.

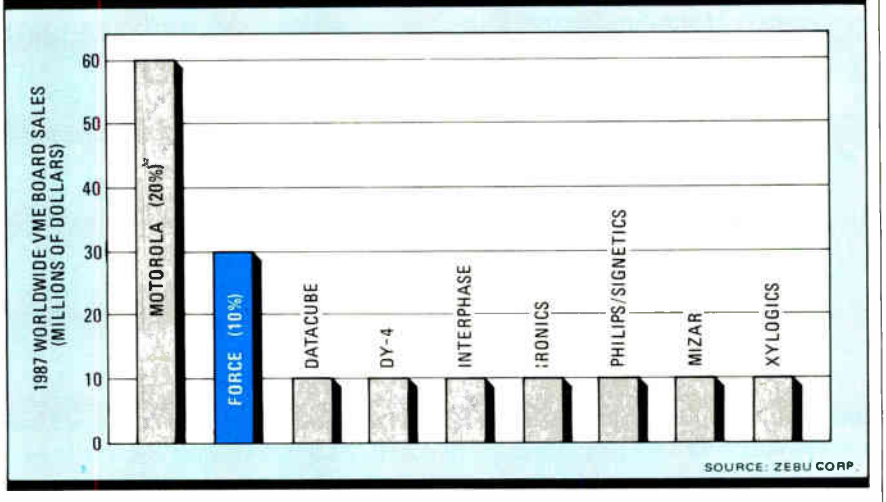
Current VMEbus technology, Weisberg says, has been pushed as far as it will go, because the mandated Eurocard form factors are crammed to the edges. Force's current VMEbus cards include piggybacked integrated circuits and an extra connector for interboard communications, allowing functions to be spread over two boards without using the bus for traffic.

The real-estate problem prompted Force to begin gate-array development. The results of that and similar programs by other VMEbus suppliers will have a big impact on systems houses. The availability of highly integrated VMEbus boards means that the bus becomes a high-speed I/O path, Weisberg says. He expects proprietary systems to give way to special-purpose supermicrocomputers that use plug-in VMEbus boards to attain needed functionality. In effect, the boards become elements in a build-it-yourself computer. Such equipment is expected to be used in factory automation, robotics, and military applications.

In fact, one of the first customers of this VME/Plus technology is Litton Data Systems in Pascagoula, Miss. Litton and Force engineers worked together on the design of a board for Litton to apply in a proposed military application, a combat-simulation training system.

Force thinks it can more than hold its own in the new VMEbus world. "Our whole history has been as a performance leader, even though we were always two or three years behind Motorola in knowing what would be available in silicon," Weisberg says. "Now we'll have our own silicon." □

FORCE RANKS NO. 2



HILEVEL'S SOLUTION TO THE ASIC VERIFICATION PROBLEM

The rapidly growing use of application-specific integrated circuits in a widening circle of equipment has created a strong demand for faster, more complex chips. But with these ASICs comes the problem of verifying and testing prototypes: The systems fast enough to test them are high-volume production equipment costing upwards of a million dollars; the ASIC verifiers that a development lab can afford aren't nearly fast enough. Now, an Irvine, Calif., test-equipment maker called Hilevel Technology Inc. says it has come up with an ASIC verifier that can keep up with today's complex, high-speed chips.

Testing the new ASICs coming off the production line is getting tougher by the day. This is evident in CMOS gate arrays and standard cells with gate delays below 1 ns that are now available, and biCMOS arrays that feature gate delays of 800 ps and I/O buffer delays of 1 to 3 ns. Recently introduced emitter-coupled-logic arrays [*Electronics*, June 25, 1987, p. 67] claim sub-200-ps gate delays, and new programmable logic devices guarantee full propagation delays below 10 ns. And ASICs are getting denser as well. Devices with 50,000 to 100,000 gates are now available, allowing more complex designs to be integrated onto a chip [*Electronics*, Aug. 6, 1987, p. 57].

The new speed and complexity place a heavy responsibility on the engineering team, which must verify its ASIC prototype prior to releasing it to production. For that purpose, the team has a number of choices. Unfortunately, these choices often end up forcing engineers and their managers to compromise between ATE production systems that can effectively test ASICs but cost too much to be practical, and less expensive ASIC verifiers that cannot thoroughly test the new ASICs.

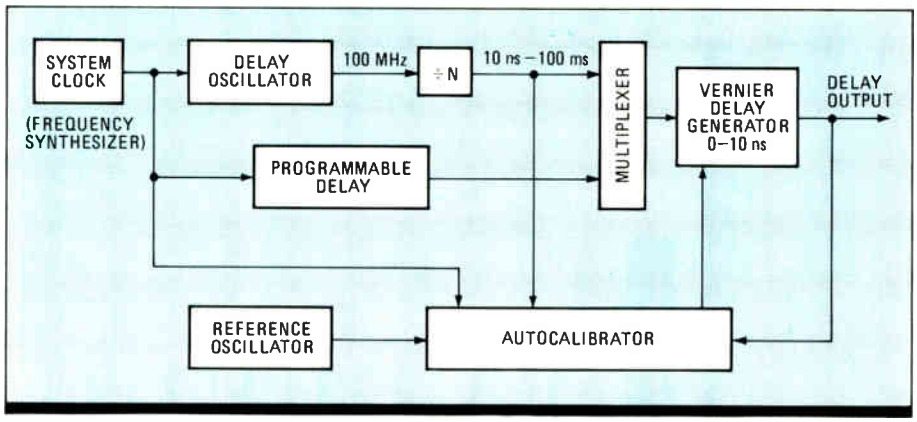
The Topaz-II ASIC verifier meets these testing challenges, maintains Norbert Laengrich, Hilevel's vice president of marketing and sales. "It bests its competition in timing and clock-rate resolution and goes on to offer more programmable delay generators," he says. And it sports the first full-color screens in an ASIC verifier, he adds.

Yet Topaz-II costs much less than a production ATE system. Its price tag runs between $50,000 and $350,000, depending on the number of pins (up to 288), depth of memory (up to 64,000 vectors), and other available options.

Scheduled to be unveiled at the International Test Conference in Washington, D. C., in September, the verifier resolves 100 ps on all 16 of its delays—compared with 500 ps for competing testers—and 100 kHz on its testing rate, or 0.2% at 50 MHz. The best the competition can resolve is tens of megahertz, depending on the test rate, Laengrich says. Topaz-II offers full timing resolution and formatting at that rate, and the verifier can generate clocks up to 100 MHz. Unlike competing testers, there is no dead time within the test cycle.

Verifying ASICs calls for functional operation at speed and for establishing the timing parameters and margins and the margins of the critical delay paths. It also means determining the characteristics of critical interface ports and the effects of environmental changes. But the semiconductor vendor often does not perform functional testing on ASICs at the prototype stage. When it does, the testing is limited by the speed of the production ATE available at its foundry. Even when semiconductor vendors conduct functional tests, these tests may be at reduced data rates. Because the vendor assumes the submitted design is correct, it concerns itself only with testing for process errors, not design errors. As a result, speed-related failures resulting from design errors—race conditions, gate contentions, glitches, and delay mismatches—will generally not be uncovered during production tests. That's why the ASIC design team must verify its prototype.

Moreover, as the data rates of ASICs increase, the need to verify prototypes at rated operating speeds becomes more acute—and even crucial. With 50- and 100-MHz rates, an engineer can test devices with internal clock dividers—especially important in meeting the testing requirements of devices under Phase II of the Pentagon's Very High-Speed Integrated Circuits pro-



1. HIGH RESOLUTION. Critical data paths on high-speed ASICs can be verified because delays can be set to within 100 ps on Hilevel Technology's ASIC design-verification system, the Topaz-II.

gram. Previous design-verification systems provided only 5- or 10-ns cycle-time resolution when operating at less than a 10-MHz test rate (100-ns cycle time), which amounts to about 5% or 10% steps in the test frequency. However, for higher-speed devices, 5-ns steps represent 20% resolution at 50-MHz test rates—a totally inadequate situation. In contrast, the 100-kHz resolution of the Topaz-II allows the operating data rate of the test device to be characterized to within 0.2% at 50 MHz.

With individual gate delays of 100 ps to 800 ps, newer ASIC devices permit delay paths to be balanced much more closely than permitted by the resolution typically available on other verification systems. In order to properly verify critical data paths, the test equipment must adequately resolve all data and clock edges and compare delays with a resolution equal to or better than the individual gate delay. The 100-ps timing resolution on the Topaz-II is more than adequate.

To achieve this high resolution while maintaining monotonic control—that is, the delay always consistently increases or decreases as commanded by the program—Hilevel chose the fastest available ECL gate array, the Motorola SC36161GW, a 2,500-equivalent-gate unit, for the 16 timing generators within the Topaz-II. The generators resolve 100 ps over a 0- to 100-ms range (see fig. 1). Synchronizing the delay oscillator to the system clock at the beginning of each test cycle eliminates both aliasing and cycle-to-cycle delay errors. The built-in autocalibration ensures delay accuracies with changes in temperature and power, and can be automatically invoked before each test.

Measuring the output timing parameters of newer high-speed ASIC devices is difficult even with expensive production ATE systems. Dead time within a system often prevents the designer from sampling the device outputs over the complete output cycle. In addition, delays within a test system often create dead-time bands. Stimulus edges cannot be placed within these bands, nor can delays be compared. Topaz-II's proprietary arbiter software/hardware feature (see fig. 2) compensates for system and device delays to eliminate dead time. The arbiter is software-driven but implemented in hardware; it uses an algorithm that monitors the system clock setting and internal system delays and also looks at where the compare-strobe delay has been set. It uses these three values to pipeline the expected response, to move it backward or forward in time, and to reposition the compare strobe to compensate for system delays.

After verifying the functional and timing parameters of an ASIC prototype, designers must verify that the part will work correctly with other design elements within the target system. This requires dynamic speed verification of the input and output high and low logic-level limits and static verification of dc parameters. For this purpose, the Topaz-II provides 10-mV resolution on driver levels and receiver thresholds. Windowed displays allow the operator to actively adjust these levels while observing the results of the functional tests.

All operations of Topaz-II can occur in an interactive mode with color-enhanced control windows, so engineers can breeze through set-ups or change test vectors easily

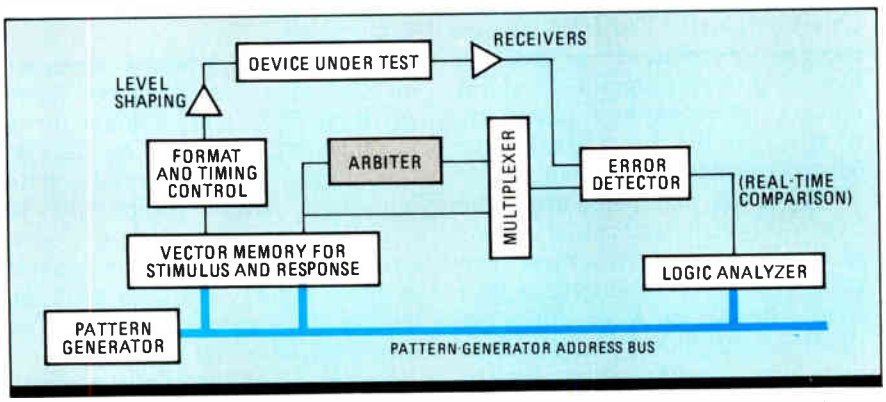
Shmoo plots also may be created to automatically characterize these device parameters.

Color-enhanced Shmoo-plot operations automate the measurement of interrelated parameters and display the test device's operational envelope on easy-to-read color graphs. For example, a designer can plot maximum data rate against V_{cc}, or propagation delay versus signal drive levels.

All operations of Topaz-II can occur in an interactive mode with color-enhanced control windows, with color-coded prompts to guide the user. This capability allows engineers to breeze through set-ups or change test vectors easily when performing diagnostic tests or "what-if" studies. Color displays ease the task of identifying and analysing test results.

Because ASICs work in the real world, environmental margins may need to be determined under varying conditions such as temperature, radiation, and power-supply levels. For such testing, the Topaz-II's enhanced programming language teams up with its fixturing arrangement to allow connection and control of the IEEE-488 standard interface bus or other instrumentation, as well as environmental chambers, controllers, and wafer probers. *–Stan Runyon*

For more information, circle 483 on the reader service card.



2. NO DEAD TIME. An arbiter circuit compensates for delays in both the test system and device under test, thereby removing dead time over the entire output cycle.

HOW HILEVEL WINS BY LEVERAGING HI-TECH

To Bjorn Dahlberg, the name Hilevel Technology Inc. says it all. "That's what we're doing here: leveraging technology from one launch pad to the next higher level," he says. The step-like growth of the Irvine, Calif., company that Dahlberg formed in 1979 to exploit a market niche for quality microcode development gear reinforces this strategy.

The technology leveraged in Hilevel's newest ASIC design-verification system, Topaz-II, for example, has its roots in the company's first products—memory emulation units. Dahlberg, president and acting vice president, built the first emulators in his garage for clients who could not find microcoding tools for bit-slice processors. From this beginning, "in the classic Hewlett-Packard progression," and with the help of Dahlberg's wife, Gloria, who is now vice president of finance and administration, Hilevel moved into more sophisticated digital test equipment.

The timing was right, too, because the rapid growth of ASICs was creating the demand for effective methods to test prototypes. The established test firms lagged in filling the demand for flexible equipment that could handle ASICs, Dahlberg says. Therefore, Hilevel's size and the team he put together enabled the company to score quickly with timely products. The DT3700 logic analyzer introduced in 1985 enhanced previous microcode development offerings and paved the way in 1986 for the original Topaz 50-MHz verification system.

"There are many similarities between the VLSI verification market and microcode development systems," observes Dahlberg. A principal thread between the two fields is the logic analysis function, which constitutes a separate product and common module in the Hilevel lines.

Another positive link is the customers themselves, familiar faces that tend to move up the product scale with Hilevel. "Sixty percent of our business is repeat orders," says Norbert Laengrich, who is vice president for marketing and sales. Selling new gear to satisfied customers also helps hold down marketing costs, among the other benefits.

Hilevel keeps its customers coming back with a commitment to service and support that has almost become an obsession, Laengrich says. "From the president to the janitor, we spend a fair amount of time making sure we're all working toward the same goals."

HILEVEL MANAGEMENT. Leading the way for Hilevel are, from left, Arch Conway, Bjorn Dahlberg, and Norbert Laengrich.

For example, when a customer on the East Coast called Laengrich at 5:30 p.m. Friday for a multiple trigger option for his logic analyzer that he needed for an important demonstration by 10 a.m. Monday, the Hilevel executive rounded up the option himself from inventory. He then sent the trigger by express mail and followed up with the paperwork.

Laengrich is one of the test and instrumentation veterans who joined Hilevel in early 1984, before the second growth phase started. Arch Conway, vice president of operations, is another. Both served in top executive posts at nearby Racal-Dana Instruments.

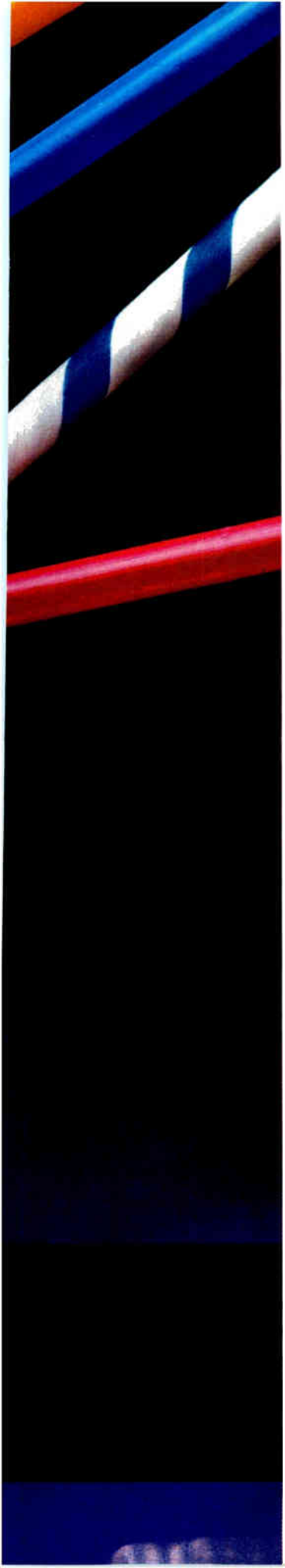
Hilevel equipment's reputation in the industry is paying off: orders are taking off, and so are profits. In 1986, the privately held company chalked up about $7.5 million in sales. It has set a $15 million goal for this year, and so far, orders for 1987 are already running at a rate of almost $18 million, "which shows we're on target," Laengrich says.

Dahlberg and his executives keep a constant eye on the bottom line, which has also paid off; Hilevel has been profitable throughout its history.

Furthermore, tight management policies have permitted growth to be largely financed by cash flow. The only equity financing took place in 1983, when a venture-capital firm put in $3 million. Dahlberg recalls that the capital was not really needed at the time, but he foresaw that financing accounts receivable and parts inventories could be a problem for his young company as the next phase of growth took place. "Besides," he explains, "during the venture-capital boom, anyone not taking their money would have been under suspicion."

Dahlberg is emphatic in singling out the dominant management philosophy of Hilevel, which is ingrained and will not change. "We're opportunistic, there's no doubt about it," he says, because the company management is decisive and moves quickly toward advances in its own niche, not veering off toward trendy goals. "But we've stayed extremely focused on our core technology through the years. You'll never see us doing a PC clone, for instance, as others have done—to their detriment." *–Larry Waller*

AT&T introduces the answer to multiusers' thirst for speed.



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It's the no-wait-state of the art in multiuser, multitasking performance—AT&T's third generation chip set—the WE® 32200 Microprocessor and peripherals.

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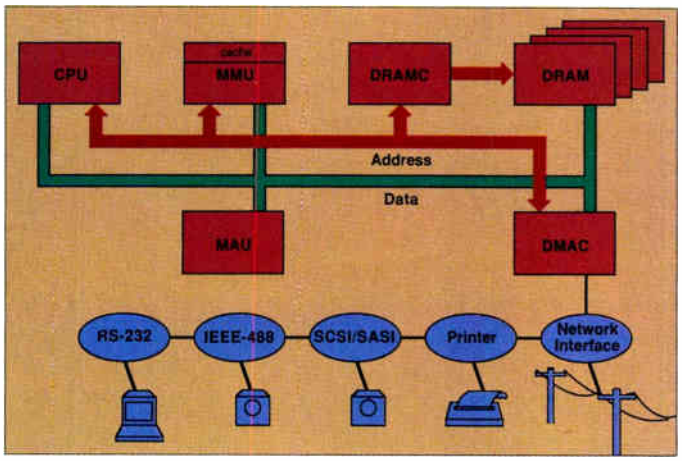
But with a system so advanced, the heart is only the start of it.

AT&T's WE 32201 Memory Management Unit (MMU) incorporates an unprecedented 4 Kbyte on-chip data cache, supports zero-wait-state virtual accesses at up to 30 MHz, and greatly reduces CPU overhead. This MMU has a variety of protection mechanisms to maintain system integrity. It is a 400,000-transistor testimonial to AT&T's technological leadership.



AT&T's newest system design offers a cache memory that runs at 20 to 30 MHz.

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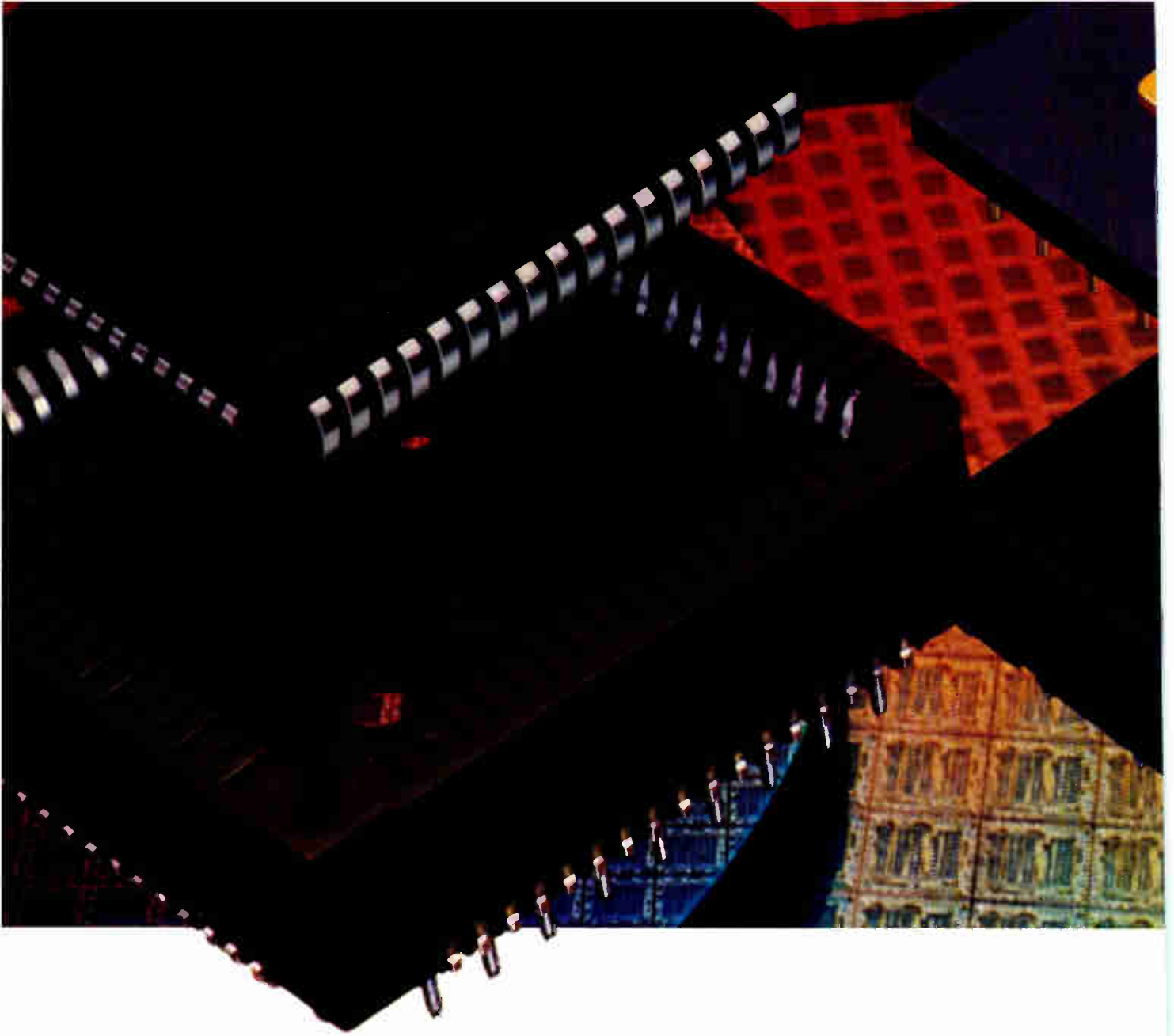

How we've made sure the chip's locked in, but you're not.

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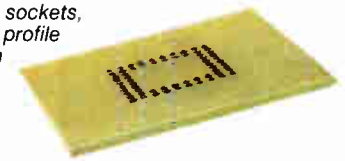

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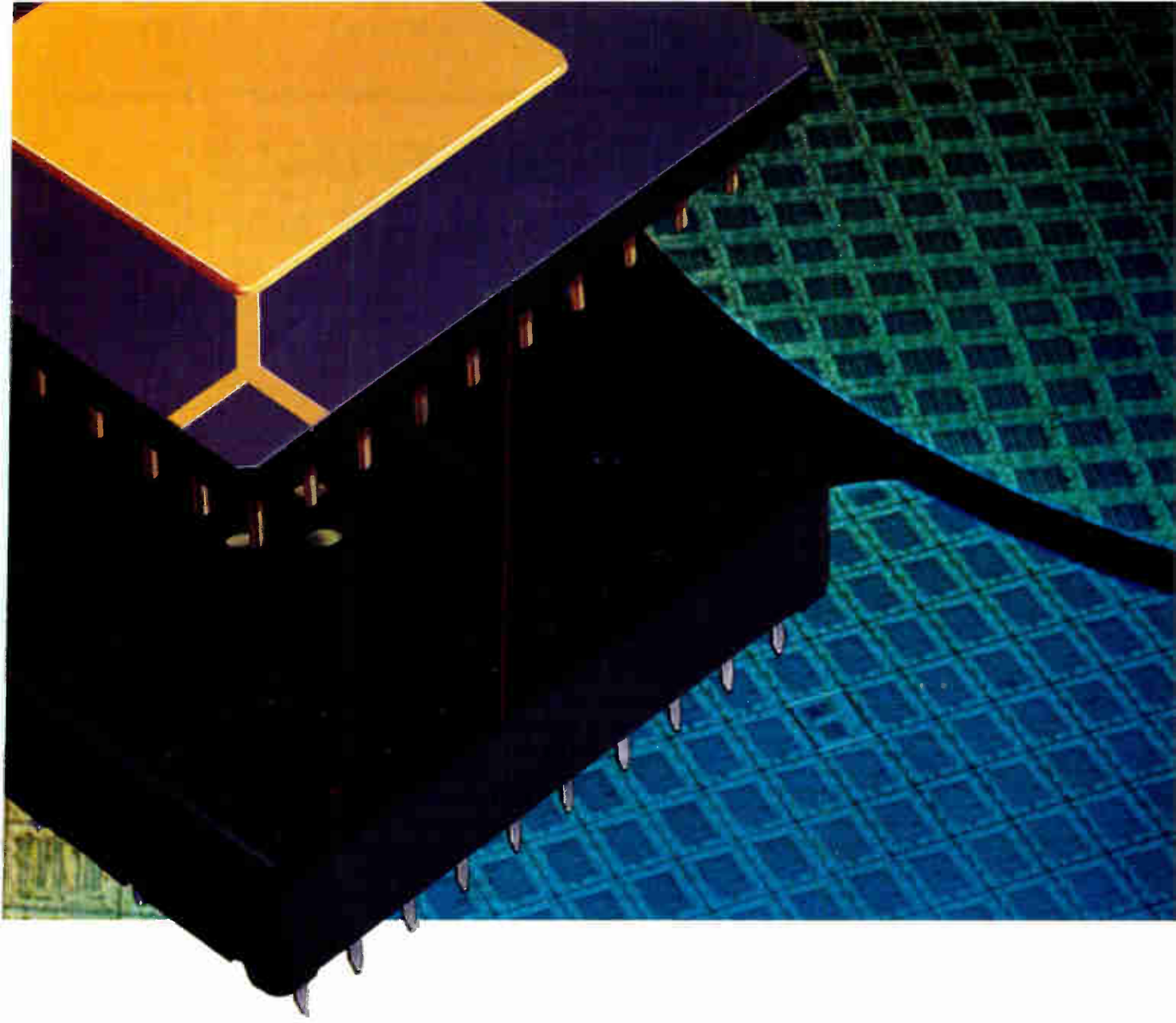

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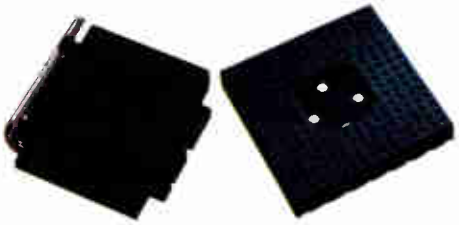
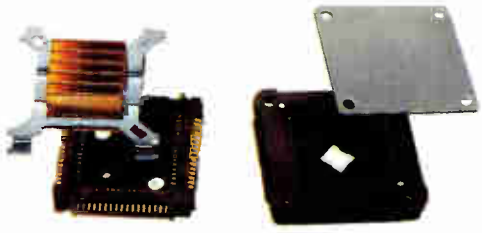


Low-height sockets in all standard sizes (JEDEC A, B, D), with duplex-plated contacts for sure performance. High-speed, surface-mount sockets feature 0.5pF, 1.4nH contact characteristics.



Circle 77 on reader service card

THE TRANSPUTER FINALLY STARTS LIVING UP TO ITS CLAIMS

Inmos Ltd.'s offbeat but super-fast 32-bit microprocessor has been slow to catch on; but now it's beginning to be designed-in to a wide range of systems around the world

by Tom Manuel and Steve Rogerson

When Inmos Ltd. introduced the first transputer microprocessor in 1983, it was providing hardware support for the Occam parallel-processing software it had completed a year before [*Electronics*, Nov. 30, 1982, p. 89]. The T414 transputer was designed from the ground up to be a fast parallel processor—10 million instructions/s was unprecedented in 1983 and is still superfast today—and it incorporated nearly everything a designer could want on a chip, including 4 Kbytes of static random-access memory [*Electronics*, Nov. 17, 1983, p. 109]. Then, last year, the Bristol, UK, company announced a mighty new transputer—the T800—that carries a floating-point unit on board and posts speeds of 4 million Whetstones, about 12 times faster than the Intel 80386/87 set and some six times the performance of Motorola's 68020/881 combination. Despite the awesome performance and intriguing potential of the transputer, though, real-world design-ins were slow to appear, perhaps because many software writers balked at learning the intimidating Occam.

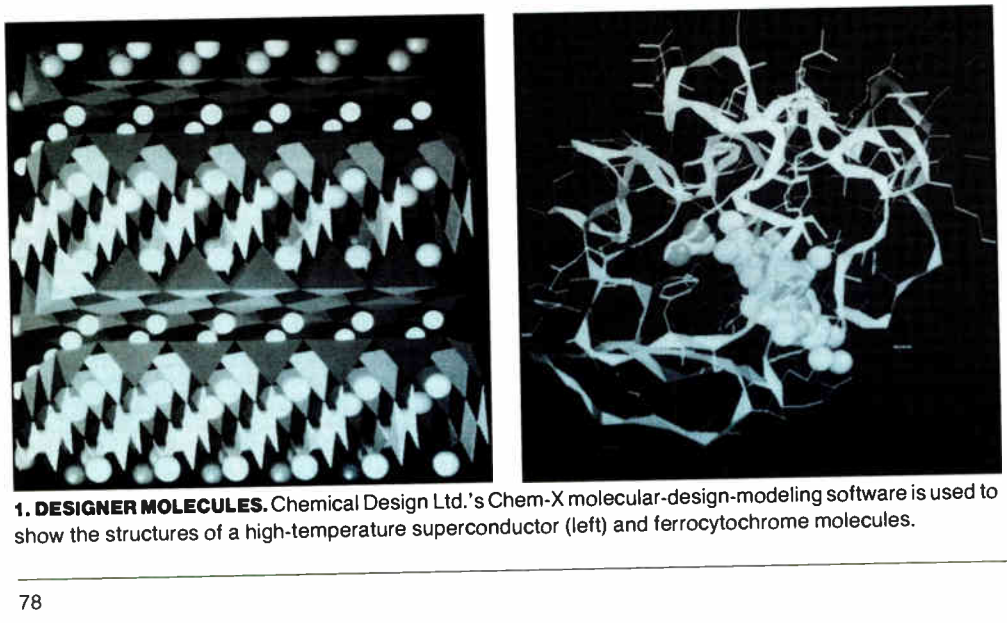
But now things seem to be looking up. At a time when speed is king, the T800 transputer and its parallel-processing capability are beginning to pop up in a widening variety of new systems, and a bunch more applications are in development.

Designs furthest along come from around the world. Chemical Designs Ltd., a British chemical firm, has developed a molecular-modeling work station that can be used for chemical, drug, and genetic design applications; Kokusai Denshin Denwa, the Japanese international telecommunications company, has developed an image-processing video telephone using transputers to manipulate and condense images for transmission over telephone links; and Intelligent Peripherals Inc., a California company, is building a multipurpose raster image processor that is the heart of a laser-printer controller. In addition, two U. S. companies, Microway Inc. and Micropar, are marketing single-board accelerators for IBM Personal Computers.

Most of the new systems are designed to use the T800 floating-point transputer [*Electronics*, Nov. 27, 1986, p. 51], and their developers are waiting until the T800 is available in volume to announced their products, says Iann M. Barron, managing director of Inmos. "We know of applications under development in such areas as process control and specialized control systems for engines, airplanes, and missiles; vision, sensing, and motion control for robots; graphics engines of all sorts, including radar processing; digital switches and picturephones in the telecommunications field; and multiprocessor supercomputers." Additional applications include a submarine command system for the Royal Navy and central processing units for conventional multiuser computing, he adds. And Inmos itself is busy building the T800 into its in-house computer-aided design system (see p. 81).

The T800 was due to go into volume production early this year, but so far designers only have access to engineering samples and evaluation boards. Now Inmos says the T800s will not be available in volume until September at the earliest.

The manufacturers of the new transputer-based



1. DESIGNER MOLECULES. Chemical Design Ltd.'s Chem-X molecular-design-modeling software is used to show the structures of a high-temperature superconductor (left) and ferrocytochrome molecules.

systems are anxiously awaiting shipment, says Steve Woods, VLSI franchise manager for Hawke Components Ltd., Inmos's top distributor in Europe. "They have designed the product in, but Inmos cannot yet ship it," he says. "Demand is outstripping supply. People who have done design work using the earlier T414 transputer have placed their orders for the T800 and are waiting for delivery."

Among the companies awaiting the T800 is Chemical Designs of Oxford, UK. It has built a molecular-modeling work station it calls Mitie, which has up to 72 times the computing power of a Digital Equipment Corp. VAX 8600 at less than half the price. The speed has been achieved by integrating a transputer-based minisupercomputer with a DEC MicroVax II processor, a Sigmex or General Electric high-performance graphics display, and the Chem-X modeling software. The system lets chemists design molecules and manipulate them using three-dimensional color graphics (see fig. 1).

GOING TO THE BOARDS

Meiko Ltd. of Bristol, UK, is supplying the transputer boards for the Mitie system. Meiko specializes in supercomputing applications [*Electronics*, Nov. 27, 1986, p. 56], and its transputer hardware was used by both of the major television stations in the UK during the general election broadcast in June to give graphical and statistical information as the results came in.

The first Japanese application of the Inmos transputer is an image-processing communications system—essentially, a video telephone—developed by KDD in Tokyo. It was a joint effort between KDD and Tokyo-based Kashiwagi Laboratories, a manufacturer of image-processing equipment.

The CP200 image communications system uses 32 of the T414 transputers to process images about 200 times faster than a minicomputer can do it. There are two models, one for transmission of still images, and another for video. KDD began selling the systems in June at a base price of about $30,000. The CP200 can be connected to personal computers to transmit images over telephone lines, or to function as a video phone (see fig. 2). It can also be used for other image-transmission applications, because it can be programmed to match the specifications of the receiving equipment, such as facsimile machines and TV monitors.

In another imaging application, Intelligent Peripherals, a Los Angeles engineering design and development company, has developed a generic raster image processor using transputers. It is used for calculating the image in fast, high-resolution printers—such as laser printers, where a lot of data manipulation is required. The Grip, as company president Sarkis Lalabekyan calls it, uses the transputer as the driving engine for a very software-intensive printer controller.

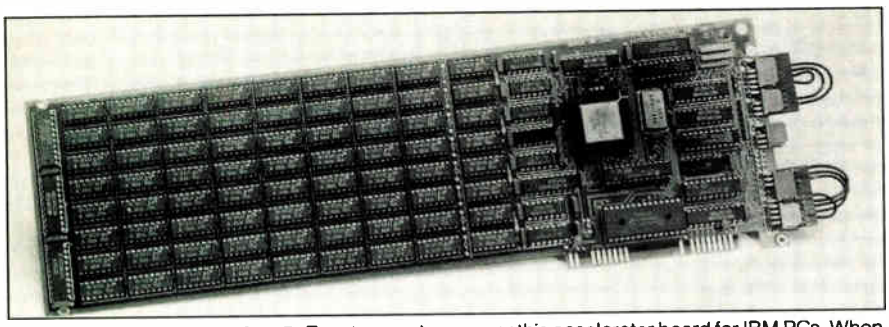
In this application, a single transputer serves as a stand-alone CPU. It was chosen because of its wealth of on-chip features. "The beauty of the transputer is that it has so many built-in resources," says Lalabekyan. Essentially, the only other hardware the product needs is a 10-Mbit/s programmable I/O bus, implemented with a Xylinx gate array, and some memory—up to 8 Mbytes, he says.

Intelligent Peripherals may go to multiple transputers in the future. The Grip is designed with an expansion bus to hold multiple processor boards, which could be used to control a fast color printer—one processor for each color plane.

Because the controller is controlled by software, it is easy to customize for a wide variety of laser-printer engines, Lalabekyan says. IPI has developed versions for the most common print engines in use today, and the company has an agreement with CCS Labs Inc. in Tustin, Calif., under which CCS will manufacture the Grip controller for original-equipment manufacturers.

The biggest use of the transputer up until now has been in embedded systems, such as the KDD image phone, the Intelligent Peripherals' Grip controller, and single boards to turbocharge IBM PCs. There are two companies doing such PC accelerator boards, says Ian Pearson, Inmos director of microcomputer operations. "Microway in the U. S. is the first to get its board on the market," he notes.

2. PICTURE COMMUNICATOR. The transputer-based image communications processor built by KDD teams with personal computers to send still or motion pictures over telephone lines.



3. SUPERBOARD. Four transputers power this accelerator board for IBM PCs. When the T800 transputer is installed, the Microway Monoputer matches a VAX 8600.

Two U. S. systems companies are building single-board accelerators for the IBM PC; one such board with four transputers can turn the PC into a desktop superminicomputer

Microway, is more a software than a hardware company, says Stephen Fried, vice president for research and development at the Kingston, Mass., company, even though it packages its language expertise (Occam, Pascal, C, and Prolog) with various transputer-based boards of its own design. The current boards use the T414 chip, and T800 boards are on deck.

One of the Microway boards, the $1,995 Microway Monoputer (see fig. 3), is based on the T414-20—a 20-MHz, 32-bit transputer that is optimized as a communications coprocessor in a transputer network. One Monoputer can be linked to as many as four others, which can be further connected in networks of hundreds to offer parallel processing.

Microway is close to introducing a T800-based board that will deliver throughput approaching that of a VAX 8600 for a price in the $3,000 range, Fried says. It will offer "roughly the throughput of an 80386 with a Weitek 1167—or 3,700 K-Whetstones," he adds.

Another PC accelerator using transputers is Micropar's T4. Like Microway's Monoputer, it is an integrated hardware and software subsystem for developing parallel-processing applications on an MS/PC-DOS computer. Micropar is a subsidiary of Definicon Systems Inc. in Newbury Park, Calif.

The T4 product consists of four processing units on one PC bus board. Each processing unit can be either a 15- or 20-MHz T414 or a T800 plus 1 Mbyte or 4 Mbytes of memory. Several T4 multiprocessor boards can be used together to build a large multiprocessor network. Users have complete control, through software, of the interconnection of the transputers via the four on-chip transputer links.

"These PC accelerator boards are what I would call fairly low-end products. But they are offering a lot of computing power," adds Pearson of Inmos. "They are designed to run existing applications packages much faster. They can reduce a spreadsheet run from minutes to seconds—about 50 to 60 times faster than the PC CPU."

This is where Pearson sees a tidal wave of transputer sales coming from. He does not believe the IBM 386-based PC is much better than the 286. "It's not that much faster," he says. "For a spreadsheet program, you can take a coffee break while it's working out the program. With the transputer, you can boost it so you don't need to wait. It cuts out user frustration."

Unlike some other coprocessors, the transputer accelerator boards don't use the host processor for any processing. The software is downloaded onto the transputer board, which takes it from there.

"The market is enormous," says Inmos's Pearson. "There are so many PCs out there. Why buy a whole new system when you can just stick a board in the back? I think we will have the lion's share of that market."

Another boom area Pearson expects for the transputer is the work-station market, both for CAD and in the financial sector. "The T800 is a very good digital-signal-processing device for work stations," he says. "There will be DSP work stations based on the T800. We will see these this year; I expect them to be announced any time now."

Pearson also foresees widespread use of the T800 in robotic systems, for three major uses: in the central control area for dumb robots; in multijointed robots; and in machine vision systems. "The transputer is used because of its communications ability," he says. "It can easily communicate between one control center and another."

The transputer also is being enlisted by the military. The Royal Navy plans to equip its submarines with a transputer-based command system made by Gresham-Cap Ltd. of New Malden, UK, under an £85 million contract. The new system will be better able to handle the complexity of undersea tactical operations.

One big transputer user could be Smiths Associates Ltd., Guilford, UK, which has "at least 12 projects ongoing using the transputer," including one for the European Space Agency, says director Chris Elliot. "These range from scientific computing to spacecraft control systems." Asked why he considers the transputer to be important, Elliot says, "I share the view that the transputer is the greatest breakthrough in computing ever. I don't know of any other way to get the power of a Cray on my desk for £100,000. It gives supercomputer power at minicomputer prices. It is a considerable breakthrough." □

INMOS PUTS TRANSPUTERS INTO ITS OWN CAD SYSTEM

In its long and difficult drive to get product developers to design-in its transputer microprocessors, Inmos Ltd. has been practicing what it has been preaching. At the Bristol, UK, company's microprocessor design center, the CAD group is ready to install the new Inmos T800 transputers into its homegrown computer-aided-design system, on which it will design the next generation of the lightning-quick parallel-processing chips. The group has already demonstrated the feasibility of using a cluster of five T414 transputers in a new super work station. Now, three of the faster T800s are being used in logic simulations, and more of the T800s will be plugged in as soon as they become available in volume, within the next month or two. Each super work station will incorporate five of the T800s and up to 8 Mbytes of memory.

The T800 is a 32-bit processor with an on-chip 64-bit floating-point unit. The chip can execute 4 million Whetstone instructions/s [*Electronics*, November, 27, 1986, p. 51]. "The complete work station has processing power equivalent to at least five [Digital Equipment Co.] VAX 11/780s equipped with a floating-point accelerator, for a cost of less than $20,000," says Clive Dyson, head of the Inmos CAD design group. In addition, any work station will be able to tap into the power of the transputer clusters of any other work station on the network for added performance when needed. Thus equipped, and when the simulation software has been redesigned to take full advantage of the parallel architecture, the machines will fly through circuit and logic simulations about 100 times faster than Inmos's current CAD system, which is made up of a DEC VAX and work stations based on the Motorola 68000 microprocessor.

Not only will the transputer clusters offload simulation chores from the VAX and take over the other ECAD tools from the 68000, but their processing power will also begin to unburden each work station's CPU even further by running the user-interface and system-control functions as well. At the same time, the mixed-mode circuit and logic simulator and other ECAD programs, which have already been rewritten to transport them from the VAX to the transputers, are now being redesigned to take advantage of the transputer cluster's parallel computing environment.

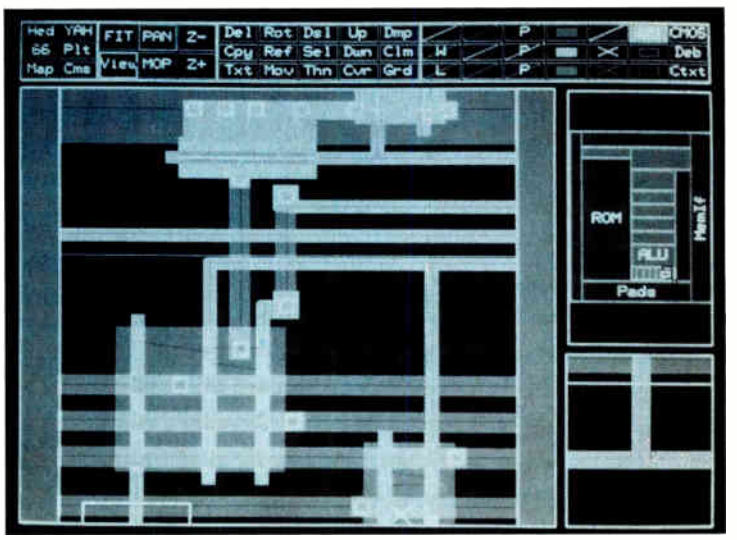
Work on Inmos's CAD system began in 1980, four years before the first transputers came on the market. In 1982 the engineers started to move all the CAD-system applications software except the simulators from the VAX superminis to the work stations. "We decided the VAX wasn't adequate for high-speed video interactive work," Dyson recalls. From then until mid-1986, the CAD system went through a process of continuous improvement, with additions such as local place-and-route and schematic capture, plus improved user interfaces.

The next step was to move this CAD software from the work stations—and the simulation packages from the VAX—into the transputer clusters. "We sat back for about nine months and during that time proceeded to move to transputers," says Dyson. "We haven't just ported the systems; we have rewritten all the system support software below that. We have now moved the whole CAD system onto transputers."

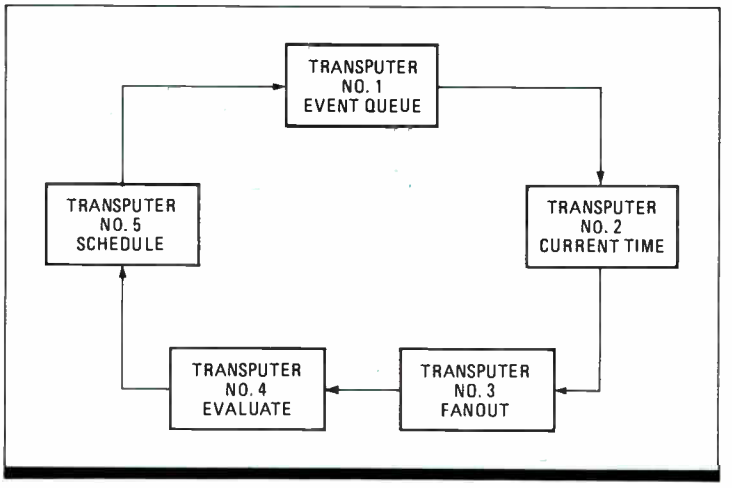
Now that the basic design tools have been rewritten for the lavish processing power of the transputer clusters, "the next step is to make more use of the transputers," says Dyson. "We want to add more services, such as windows, file systems, and process control. We will then add new algorithms to the existing design system. This will change the design methodology to run all the design and simulation algorithms on multiple transputers."

The window addition (see fig. 1) will let a programmer run two programs concurrently—one on his own cluster and one on another—while watching the progress of both programs on the terminal. Although Inmos has designed its own window system, it is not planning to use it but instead will add one of the two emerging commercial window standards, either X Windows or Sun Microsystems's NeWS. The X Windows system will be used initially. "Our own windowing system is limited, and rather than extend it, we might as well adopt an industry standard," says Dyson.

The X Windows program ties in well with the transputer model of distributed computing. The X Windows base system is defined by a network



1. DOING WINDOWS. The Inmos in-house design system is undergoing a major overhaul; one of the improvements is a window-system user interface.



2. CLUSTER. The event-driven logic simulator gets a big boost from concurrent processing in a five-transputer pipeline.

protocol. Unlike the procedure-call or kernel-call interface used by other windowing systems, X Windows is based on asynchronous communications streams between processes. Since the transputer model of distributed computing is also based on the concept of interprocess communications, the match is convenient. Communications between processes consisting of self-contained chunks of program code are carried out over a channel connecting the processes. If two processes are running on the same transputer, the interprocess communications-channel link is accomplished by a block move of data in memory. If the processes are on different chips, the data passes through one of the four transputer links to one of the links on the other chip.

"The event-driven logic simulator is running now on a regular basis on a transputer cluster," says Dyson. Some finishing touches are being made to the circuit-simulation part of the full mixed-mode simulator.

Each transputer cluster has a pipeline of five transputers working concurrently on a single job (see fig. 2). High-speed processing is achieved, because as soon as a step is passed from transputer 1 to transputer 2, transputer 1 can then start working on the next step, and so on. The same pipeline supports event-driven circuit and logic simulations. During simulation, transputer 1 acts as an event queue, listing changes to a node in the circuit under test as they occur. Transputer 2 performs node-strength resolution—in other words, when a node is being forced in opposite directions by two or more different inputs, the transputer performs a computation to decide which is the stronger.

Transputer 3 is called the fanout processor, because it maintains a fanout data structure or circuit map of the circuit being simulated. For each node change, it requests transputer 4 to evaluate each connected element. Transputer 4 then determines the effect of input on the element's output and sends the resulting change of output to transputer 5, which in turn translates an element output change into a node change.

More details on the mixed-mode system that will allow circuit and logic simulation to be performed concurrently on the same cluster are to be presented in a paper at the International Conference on CAD (ICCAD), to be held in Santa Clara, Calif., in November.

The mixed-mode system shows how programs will have to be rewritten in the future to run on parallel-processing hardware. Basically, the Inmos system is an event-driven mixed-mode simulator supporting functional, circuit, and logic-level simulations. The functional simulation predicts a circuit's overall performance from its initial specification and requires no knowledge of the chip's internal workings. In contrast, logic-level simulation represents the circuit as a network of logic gates and can be used to model noncritical circuit elements. And the circuit-level simulation, which predicts a node's behavior from a nonlinear model of the transistor, is accurate—but it is computer-intensive and hence notoriously slow.

With mixed-mode simulation, as in the Inmos CAD system, the whole process can be speeded up. Parts of the circuit that are not of immediate interest can be modeled at the logic level, while only critical parts are simultaneously and precisely modeled at the transistor or circuit levels. This approach reduces the computational power the simulator program requires.

In an event-driven simulator, as logic transitions propagate through the circuit—causing transitions or events at other nodes—each event is individually analyzed. In contrast, a time-driven simulator evaluates all nodes at fixed time steps, regardless of whether or not a logic transition has occured. An event-driven simulator is therefore far more economical in terms of processing power.

A NEW SET OF ALGORITHMS

Now that the simulator is up and running on the transputer clusters, Inmos software engineers are rewriting the core of the mixed-mode simulation system in the Occam language, with new algorithms. This effort is where most of the future speed improvements will come from.

The rewriting is being done in three steps. The first, which is essentially completed, is to reconfigure the simulation system to run on the transputers. One transputer alone runs simulations 8 to 10 times faster than a VAX 11/785 with a floating-point accelerator, says Dyson. The second step, which has been demonstrated with the T414s, is to run the simulator on a five-transputer cluster, boosting speed another fourfold, for a total of 32 to 40 times the simulation performance. The CAD group expects the final step, adding new algorithms to the simulator core to exploit the parallel hardware, to boost performance again, but it is too early say by how much. *–Steve Rogerson*

For more information, circle 484 on the reader service card.

MIPS CHIP SET BREAKS MOS FLOATING-POINT RECORD

The ante has just gone up in the competition to be No. 1 in MOS floating-point performance. MIPS Computer Systems Inc. is producing a 2-μm double-metal-CMOS single-chip floating-point processor—the R2010—which, when paired with the Sunnyvale, Calif., company's 32-bit R2000 reduced-instruction-set central processing unit, can perform single- and double-precision calculations two to 10 times faster than previous implementations.

The 2000/2010 CPU/FPU combination comes in 8-, 12.5-, and 16.7-MHz versions and is available as components, on boards, and as complete systems. MIPS sells the two faster versions, but reserves the 8-MHz chip set for its own products. In 5,000-quantity lots, the CPU costs $195 for the 12.5-MHz version and $295 for the 16.7-MHz version. The FPU cost $295 in the 12.5-MHz version and $450 in the 16.7-MHz version.

The replacement of MIPS's original floating-point processor board by the FPU chip greatly improves floating-point performance in MIPS systems. In the company's M/500 system, where the FPU and the CPU operate at a 8-MHz clock rate, floating-point operations have increased from 1.6 million Whetstones/s, single precision, to 5.8 million Whetstones/s with the separate FPU. That's about three to five times faster than a Digital Equipment Corp. VAX 11/780, twice as fast as the Fairchild Clipper operating at 30 MHz, three times faster than a 25-MHz Motorola 68020 32-bit CPU operating in combination with the Weitek four-chip FPU board, and eight to ten times faster than the Intel 32-bit 80386 and its 80387 floating-point coprocessor. The entry-level price for the M/500 is $20,900.

In the 12.5-MHz, $25,900 M/800, single-precision operations rise to 8.9 million Whetstones/s. In MIPS's top-of-the-line 16.7-MHz, $35,900 M/1000 system, floating-point operations improve further to 10.7 million Whetstones/s, single precision.

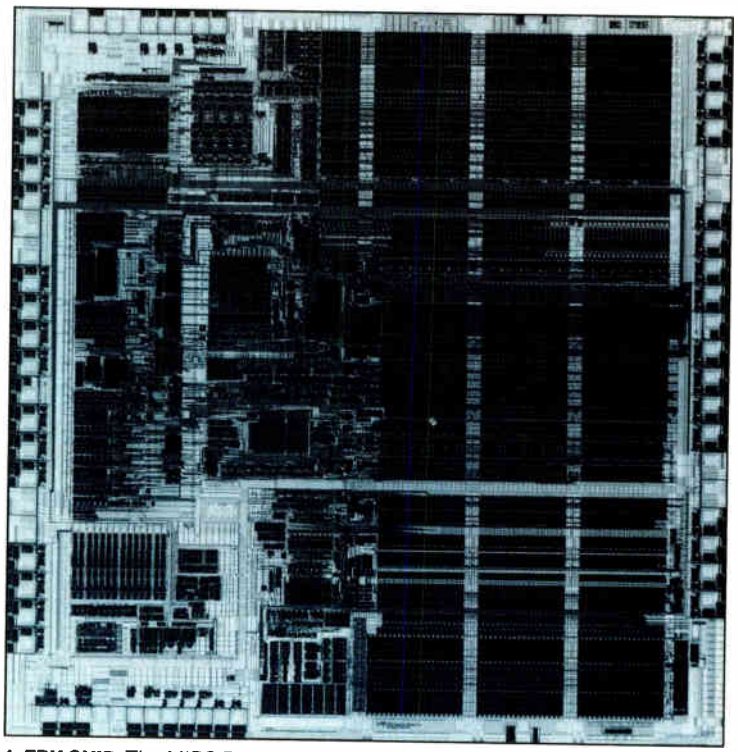
A contender likely to break that record is the two-chip set from Bipolar Integrated Technology [*Electronics*, Feb. 19, 1987, p. 88], but BIT says it hasn't yet had reports from its customers of benchmark figures. However, the bipolar BIT chip set is targeted at applications like graphics displays and minisupercomputers, where MIPS is aiming at work stations and similar applications.

The 2010 (see fig. 1) is also two to four times faster than the full-board FPU, built around the industry-standard Weitek floating-point chip set, that MIPS originally introduced with its 32-bit RISC chip. The single-chip FPU replaces up to 150 integrated circuits, so power dissipation is reduced from 50 to 60 W in the full-board implementation to no more than 2 to 3 W. In addition, the Weitek-based FPU board peaks at 8 MHz, because it is not possible to run the interface any faster.

The chip's designers achieved this improvement in performance by designing in key architectural, circuit, and software enhancements—including the use of a closely coupled interface that allows the FPU and CPU to operate in parallel; the use of sophisticated exception- and stall-handling protocols to eliminate bottlenecks; and a dramatic reduction in the number of cycles required to execute typical floating-point instructions.

The 400-by-400-mil FPU incorporates on-chip all the logic necessary for performing all the requirements and most of the recommendations of the IEEE-754 floating-point specification. It performs floating-point operations using 32-bit single-precision and 64-bit double-precision formats. Included on the chip (see fig. 2) are sixteen 64-bit registers constituting the main data path, which has been split into a 53-bit-wide mantissa portion and an 11-bit-wide exponent portion, plus several bits for rounding, according to the IEEE specifications. In the board-level implementations of the same architecture, as much as 16 Kbits by 8 bits of external SRAM would be required.

Also included on-chip are three independent functional units: the add, divide, and multiply blocks, which can operate in parallel while doing loads and stores out of the register file. In the earlier board-level FPU, floating-point instruc-



1. FPU CHIP. The MIPS R2010 floating-point coprocessor draws only 2 to 3 W and replaces 150 ICs on a board that dissipates 50 to 60 W.

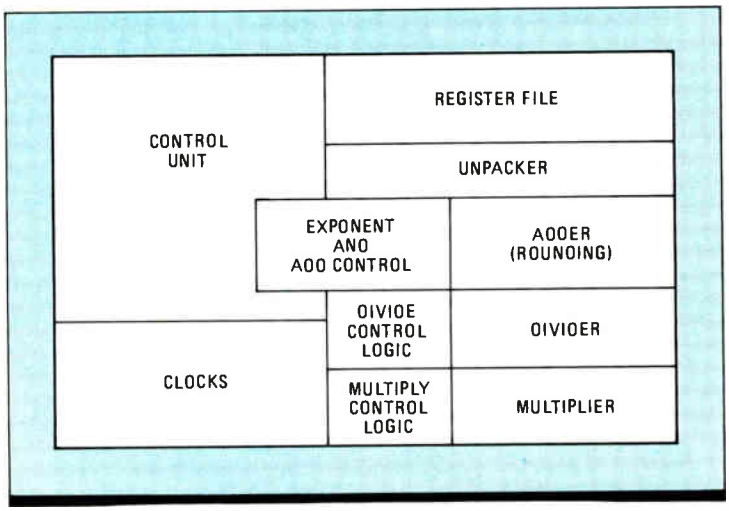
tions are executed serially, but the R2010 allows floating-point operations to be performed, not only in parallel with load and store operation, but concurrently with fixed-point instructions.

Operands flow from the register file into "unpacker" logic, which splits the 64-bit word into mantissa and exponent. From there the data goes to the add, divide, or multiply blocks. Also

The new single-chip floating-point unit and a faster CPU work in parallel on the same instruction stream to hit 10.9 million Whetstones a second, single-precision

contained on-chip is the control unit, which performs instruction decoding, exception, and stall-condition control functions and instruction staging. Incorporated into the same area on the die are all the instruction-interpretation and pipeline-control logic, which in the board-level FPU must be implemented with random logic or with the use of programmable logic devices.

Where the MIPS FPU differs from other closely coupled implementations is that it is a co-interpreter rather than a coprocessor; that is, it sees instructions at the same time as the CPU does and executes them in parallel with the CPU. By comparison, in many current floating-point schemes the CPU picks an instruction from the microcode stream on the bus and, if it determines it is a floating-point function, sends it to the coprocessor. The coprocessor performs the appropriate operation on the data and sends the result back to the CPU. In the MIPS implementation, the CPU and FPU interpret the same instruction stream, executing instructions simultaneously. As a result, values can be stored and loaded from the FPU and to the cache or main memory without having to go through the CPU, which forms a great bottleneck in other approaches.



2. IN PARALLEL. The add, multiply, and divide blocks on the R2010 work in parallel with the register file for a throughput of up to 10.7 million Whetstones.

A second factor contributing to the 2010's impressive performance is the use of an exception scheme that eliminates the delays that can occur when an unusual instruction sequence is encountered. When the FPU decides it cannot execute a specific instruction properly, it can shut down the pipelines of both machines, making it possible to restart the instruction sequence without any anomalous results. This is a problem for floating-point units having very long pipelines: for example, the FPU may get to the end of a calculation and discover there is an overflow condition, while in the meantime the CPU has executed six instructions. Under such conditions it is not possible to back up and do things all over again. With MIPS's exception scheme, however, the FPU and CPU stop cleanly and then restart exactly on the faulty instructions. A tightly coupled handshaking scheme enables the two processors to signal exceptions to each other quickly and directly.

An analogous handshaking scheme handles stall conditions—a situation in which, for some reason, either unit decides it must wait before going on with an instruction. For example, if the FPU is executing an operation, and another floating-point instruction is fetched when the FPU needs the result of an operation in progress, the FPU will recognize that the second cannot be executed until the first is completed and will signal the CPU to stall until this is done.

The combination of the exception- and stall-handshaking schemes allows the FPU and CPU to operate in parallel while chaining operations back to back, without the possibility of a glitch at one stage slowing down or completely disabling a particular operation. In current CPU/FPU implementations, highly parallel operations and chaining are mutually exclusive for the most part. The handshaking capability is particularly important in chained operations, where the result from one operation is the starting point for the next.

Another contributor to the improved performance is a significant reduction in the number of cycles needed to execute a typical floating-point instruction. For adds and subtracts, the average number of cycles required is two, versus about 12 to 15 for the company's previous board-level solution. This is almost a 75% reduction in execution time: 120 ns versus 400 ns. Multiplies and divides require four and five cycles, for single- and double-precision operations, respectively, compared with 16 and 20 cycles for the board-level solution. At 16.6 MHz this is a total execution time of only 240 to 300 ns, compared with 1,600 to 2,400 ns.

Incorporating the new FPU into MIPS's current R2000 32-bit RISC processor board has required no hardware revisions whatsoever, since the system was designed to accommodate the FPU when it became available. In early versions, a ribbon cable ran from the FPU socket to the Weitek-based multichip FPU board. *–Bernard C. Cole*

For more information, circle 485 on the reader service card.

ZYMOS TOOLS LET USERS CUSTOMIZE PC-CLONE CHIPS

A bunch of companies are offering chips now that reduce the component count of an IBM Corp. PC AT motherboard from a hundred or so integrated circuits down to a half dozen or less. But Zymos Corp. has distanced itself from the crowd by taking a semistandard approach: it will offer a catalog product called PC-On-A-Chip, or Poach, that lets a chip customer do some customizing. Working with a new custom Poach tool kit, the customer can now add his own "AT personality" to the Poach 1 and 2 AT chips in a matter of mere days.

The tool kit represents a set of board-level emulations of the Sunnyvale, Calif., company's Poach 1 and 2 AT chips [*Electronics*, July 1, 1985, p. 23], says Robert Andrews, director of technical marketing at Zymos. The boards allow the designer to modify quickly those random-logic portions of the basic Poach chip architecture that relate to timing and refresh operations, as well as certain interface functions.

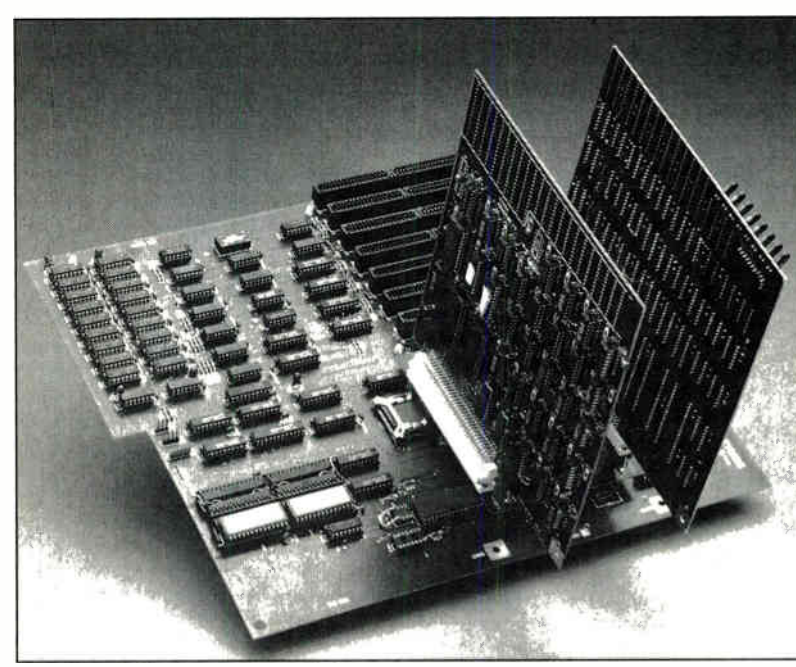
The tool kit replaces the usual CAE design task with one of working on a printed-circuit board, says Andrews. Both Poach 1 and 2 have been implemented as emulator boards—that is, boards built up out of discrete logic that function in a similar manner to the Poach chips. "As such, they can be plugged into sockets on the system board in the same way chips would be, and proposed design changes can be checked for software and hardware compatibility," he says. "This allows a convenient separation of tasks between the customer and Zymos." The customer's systems engineers modify the emulator boards, and then Zymos converts the revised emulator boards to silicon. As a result, the system design engineers need not learn Zymos's design software in order to customize the Poach chips.

Together with a memory-buffer chip, the Poach 1 and Poach 2 chips replace between 50% and 75% of the logic devices on the original PC AT motherboard. The Poach chips are fabricated using Zymos's 1.8-μm CMOS Supercell library of LSI and VLSI functions. Poach 1 replaces the AT functions of the clock generator and ready-signal interface, the bus controller, the real-time clock, the dual programmable interrupt controllers, and the random logic for the command-delay, shut-down, address, and data-control functions. The Poach 2 chip incorporates a programmable interval timer, a clock generator, a memory mapper, and dual direct-memory-access controller functions, as well as the random logic needed for such operations as timing, refresh generation, and DMA arbitration.

The hardware in the tool kit consists of the ZyAT-1 evaluation motherboard for the Poach/AT chip set, a daughterboard that plugs into the Poach chip sockets, and two emulator boards, one for each of the Poach chips (see fig. 1). The emulator boards are hardware implementations of the two Poach chips, with enough board space for wire-wrapped models of intended modifications (see fig. 2). In the motherboard, the plug-through sockets into which the Poach chips are normally inserted are replaced with emulator boards attached to the daughterboard.

In addition to the hardware, the tool kit contains a PC AT-based schematic-capture package from Case Technology that includes schematics for the Poach 1 and 2 chips, and the entire Zymos standard-cell library from which the chips were developed. Also included is the company's AT-based simulator, which provides local simulation of the proposed designs.

Zymos's semistandard approach puts design options back in the hands of the engineer, Andrews says. "When designing a PC AT product, the engineer is already boxed in by the need for compatibility with the IBM architecture, the existing software, and the expansion bus," he says. The standardized solutions offered by competitors, he says, essentially force the designer to accept a fixed design. "What this does is take away options that may help him differentiate his product."



1. EMULATION SET. Zymos's tool kit includes a motherboard, a daughterboard that plugs into the chip-set sockets, and two boards that emulate the Poach chips.

As an alternative, semicustom companies have entered the market with semistandard PC AT chip sets, built with gate-array and standard-cell techniques, that can be customized to customer needs. Nevertheless, "considering that the typical turnaround time for a clone manufacturer, from design to finished product, is now as short as three months, even the semicustom approach based on gate arrays and standard cells is too long," says Andrews.

The Poach semistandard approach to making 'custom' PC AT chips cuts the design cycle from months to weeks; its new tool kit trims that to a matter of days

In the original Zymos semistandard approach, in which designers were required to use Zymos CAE software and modify the Poach structure to their own requirements, development time was reduced to a matter of weeks rather than the months it takes with semicustom methods. "The tool kit further reduces the design time to a matter of days," says Andrews. "First of all, because the designer uses a printed-circuit-board-based emulator to test and modify the basic architecture, he works in a familiar environment and does not have to spend time learning to use a computer-aided-design methodology. Second, the job of testing out the modified architecture is done before the chip is committed to silicon." In traditional semicustom approaches, a customer gets a chance to test the architecture only after the chip has been fabricated. And depending on how well the customer and vendor communicate, getting the final chip to work in the system is a process that can take additional weeks and months. "In the custom-tool-kit approach, Zymos commits nothing to design until the customer has tested out the board-level emulation and modified it to suit his purposes," says Andrews.

The customer modifies the schematics to incorporate or change the logic on the emulator boards. He can verify the new logic functions through simulation and then modify the emulator board to reflect the schematic changes. "Once this has been done, the system designer has at hand a worst-case chip design—based on voltage and temperature considerations and timing performance—that is accurate to 0.1 ns," says Andrews. "He also has a working hardware implementation of his system, with the proposed changes actually realized in hardware."

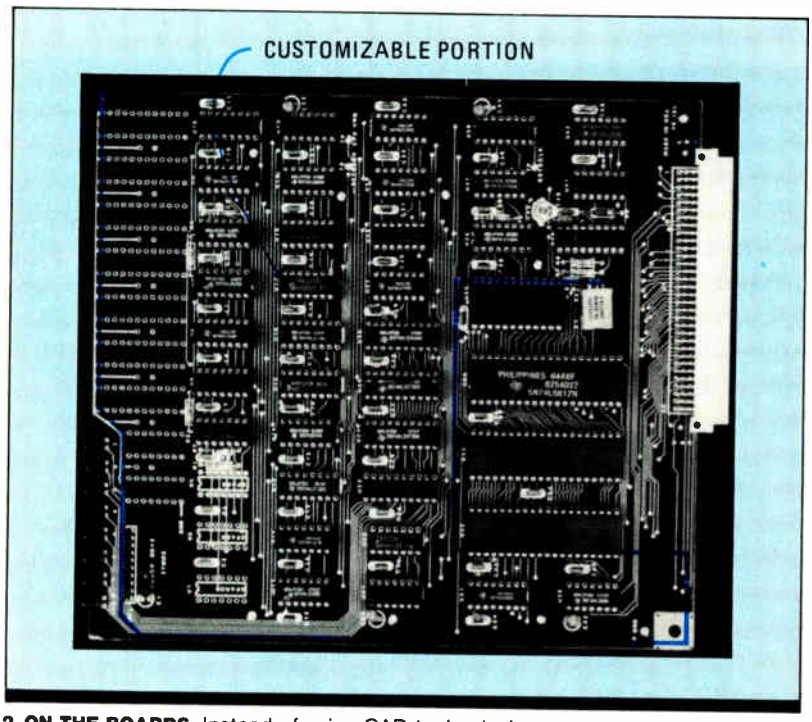
With the working emulator boards in hand, the customer transfers the design task to Zymos—shipping one set of the emulator boards, suitably modified, along with a floppy-disk copy of the new schematics and any pertinent information, such as timing specifications. Zymos converts the emulator boards and schematics to silicon, using its in-house design tools to combine the revised glue-logic with its SuperCells and to route the resulting circuit as a chip.

Simulations are run at each stage to ensure compliance with customer specifications, and simulation results are submitted for customer approval. Since both the customer and Zymos are working with the same set of schematics, the same schematic-capture package, and the same terminology and node names, and since both have hardware implementations in the form of emulator boards of the proposed chips, communication is facilitated at all levels.

When the customer has approved the simulations as run by Zymos, the devices are fabricated, and prototypes are delivered for customer verification. Upon approval of the original 10 prototypes, Zymos then delivers an additional 250 qualification samples, which are used to provide a pilot run for the customer's system.

The Zymos custom Poach program allows for the customization of the random logic on the Poach chips without involving the systems designer in the SuperCell design, repartitioning of the chips, or packaging concerns, says Andrews. The tool kit will be packaged as part of the total nonrecurring engineering costs of a custom design, and there will be little if any difference in parts costs from those of standard parts, says David Guzeman, vice president of marketing. *–Bernard C. Cole*

For more information, circle 486 on the reader service card.



2. ON THE BOARDS. Instead of using CAD tools, designers test out Poach chip-set designs using emulator boards, which can be wire-wrapped for intended changes.

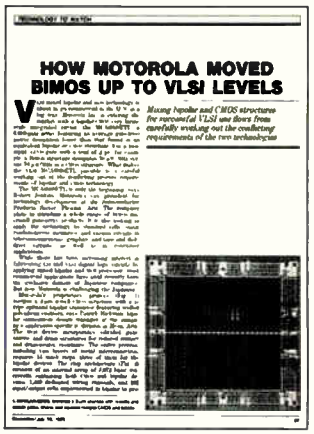
UPDATE: MOTOROLA ADDS TO BiCMOS PRODUCT LINE

Motorola's 2-μm biCMOS ECL- and TTL-compatible gate array has been slow in gaining industry acceptance, a year after it was introduced [*Electronics*, July 10, 1986, p. 67]. But John Carey, merchandising manager for Motorola's ASIC division in Phoenix, Ariz., is not surprised. "BiCMOS is still a niche product," says Carey, "attractive mainly to those who need the low power of the CMOS and the speed of the bipolar and are willing to pay the extra premium."

Of the several hundred inquiries, Carey says, perhaps a half dozen have ended up at the design-in stage. "Overall, I don't believe there have been more than two dozen or so design-ins in the U. S. for all digital biCMOS gate-array vendors."

Despite slow sales, Motorola continues to expand the product family beyond the original BCA6000ETL (formerly called MCA6000ETL). At the beginning of this year the firm introduced a 4,000-gate device, the BCA4000ETL, with about half as many input/output lines as last year's design. Motorola has also developed the BCA8000RAM, an ECL/TTL/CMOS biCMOS device that incorporates a 4-Kbit static random-access memory and 8,000-gate array; and the BCA10000TTL, a higher-density CMOS/TTL version.

The BCA700ETL and the BCA1800ECL—two lower-density versions aimed at various applications in telecommunications, test instrumentation, and automatic test equipment—augment the product line. The 700-gate device is available in a 28-pin dual in-line package with 20 I/O lines, up to 52 pins, and 44 I/O lines in a plastic leaded chip carrier. The 1,800-gate packages, on the other hand, range from a 40-pin DIP with 28 I/O lines up to 88 I/O lines in a 100-pin grid array.


HOW MOTOROLA MOVED BIMOS UP TO VLSI LEVELS

Mixing bipolar and CMOS structures for sub-micrometer VLSI was driven from carefully working out the conflicting requirements of the two technologies

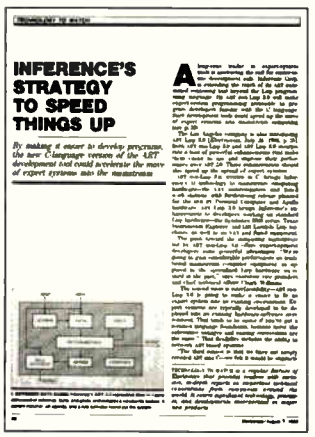
Carey expects business to pick up once computer-aided design tools become available, allowing designers to work with the unfamiliar biCMOS technology. In anticipation, Motorola plans to offer such capabilities as schematic capture, timing simulation, and test-program generation software for the biCMOS devices. These capabilities were scheduled to become available on Daisy work stations in August and on Mentor Graphics systems this month. *–Bernard C. Cole*

UPDATE: MAJOR GLITCHES HIT NON-LISP AI TOOL

Last year, Inference Corp. of Los Angeles, a maker of artificial-intelligence software-development tools, introduced two new versions of an expert-system development tool called ART: one written in Lisp, the most commonly used AI language, and the other in C, one of the most popular languages in conventional computing [*Electronics*, Aug. 7, 1986, p. 66]. Since then, the Lisp version has demonstrated a strong showing in the market, but ART in C has caused embarrassing failures in large expert systems—forcing Inference to temporarily halt distribution.

In developing the C version, Inference designers built a translator to translate the Lisp version to C, figuring it would be much simpler to maintain and develop just one version of ART under the Lisp development environment. Developers of expert systems, Inference believed, would find it easier to fit in new and existing applications if there was a common language base between them.

But problems with the first non-Lisp version of ART, a C version for Digital Equipment Corp. VAX superminicomputers, started to show up within a couple of months after the first deliveries in late March. The software glitches were subtle—they did not show up during beta tests, becoming apparent only when big expert systems that were already written with the Lisp version of ART were later translated to the C version.


INFERENCE'S STRATEGY TO SPEED THINGS UP

By making it easier to develop programs, the new Clearpoint version of the ART development tool could accelerate the move of expert systems into the mainstream

"The system is not as graceful in failure as a robust commercial system must be," says Inference president Alex Jacobsen, who has been busy analyzing the flaw since late June. The problem, Jacobsen says, seems to be a result of intrinsic differences between the programming styles of Lisp and C.

Not ready to abandon the idea of a non-Lisp version of ART, Inference engineers are trying to fix the problem. But the translation approach may prove too costly. "We may have to fall back on Lisp compiler technology to solve the problem," says Jacobsen. "The decision will depend upon the estimated costs of the alternatives—it is a development-resource spending issue." *–Tom Manuel*

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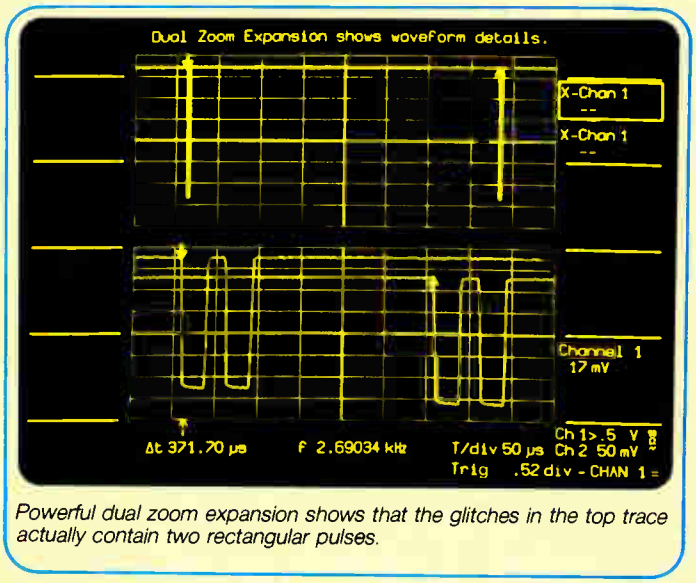

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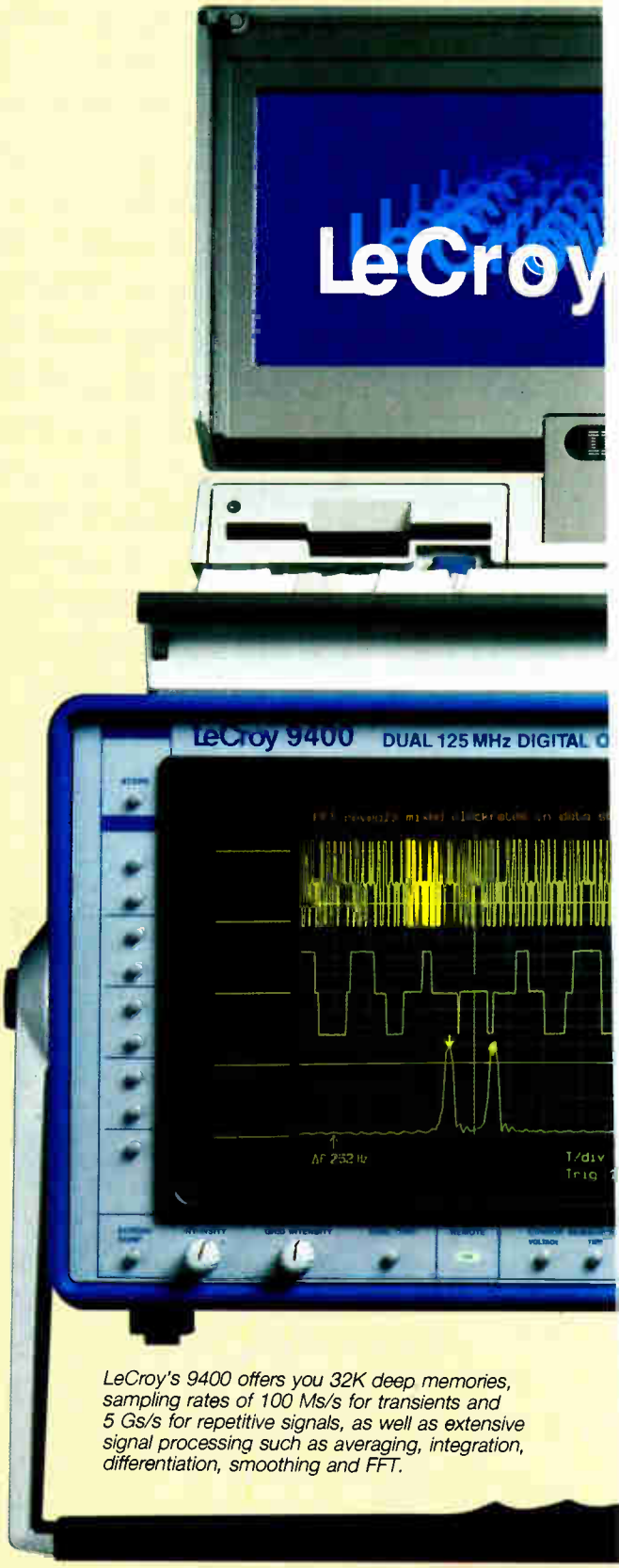

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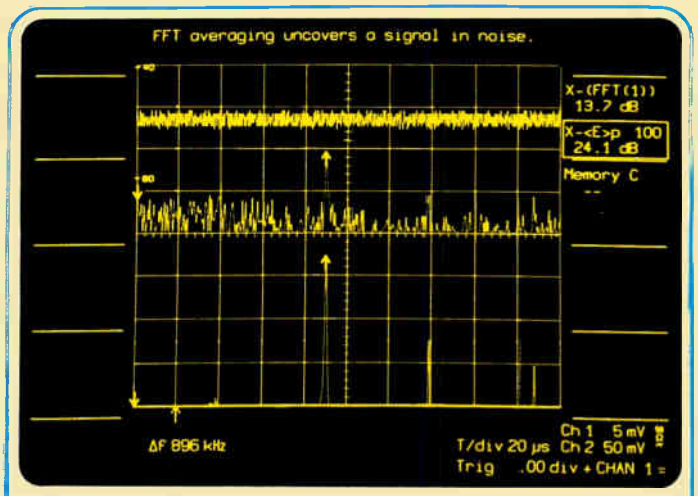

FFT averaging of apparent random noise reveals a 896 KHz signal not visible in the time domain record (top trace).

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MILITARY/AEROSPACE NEWSLETTER

PENTAGON TO FUND 5-YEAR R&D EFFORT ON PHASE-2 VHSIC MANUFACTURING

As a follow-on to the Defense Department's Very High-Speed Integrated Circuits program, the Air Force says it is seeking proposals for a jointly funded, five-year project "to establish and demonstrate a domestic integrated-circuit manufacturing capability that will ensure the availability of circuits needed to field Air Force systems in the 1990s and beyond." The proposals are due by Sept. 28, and contract awards are expected by mid-February. Two contracts are to be awarded, according to one potential bidder. One will be worth about $75 million, the second about $50 million. The manufacturing initiative is apparently aimed at ensuring the availability of chips developed under Phase 2 of the VHSIC program. Funding sources for the effort, called the Microelectronic Manufacturing Science and Technology program, will include the Defense Advanced Research Projects Agency, as well as the Air Force. Goals for the program include the development of a computer-integrated processing system that would work under expert-system control to support a flexible, cost-effective manufacturing capability for low-volume, military application-specific chips with minimum feature sizes of 0.5 μm or smaller. The Air Force is seeking "the ability to produce different chips, . . . run different processes, . . . and produce first-pass working chips with good yield." □

SEMATECH COULD GET $200 MILLION FROM DOD OVER TWO YEARS...

Federal funding for Sematech, the joint government and private industry manufacturing-research program designed to help make U. S. chip makers more competitive in the world semiconductor market, is still tied up in the federal budget bills on Capitol Hill. The House of Representatives has already approved $25 million in its version of the Defense Authorization Bill, but the Senate version, which recommends a $100 million investment in the program, is tied up in a filibuster over arms control that could drag on until September. Informal discussions between House and Senate conferees indicate Sematech will win a two-year appropriation worth $200 million, according to an aide to Sen. Jeff Bingaman (D-N.M.), chairman of the Senate Subcommittee on Defense Industry and Technology. But how that money will be spread out over fiscal years 1988 and 1989 is still up for grabs. If the final 1988 defense budget is worth $289 billion, the aide says, Sematech will get $75 million from the Pentagon the first year and $125 million the second. But if the defense budget is approved at a $296 billion spending level, the money would be split evenly, at $100 million each year. □

...AND IT MAY BE MANAGED 'FLEXIBLY' BY AN INTERAGENCY GROUP

While Sematech officials await Congressional approval of federal support for their program, they're also waiting to see just whom in the Federal government they will have to work with. A section of the Omnibus Trade and Competitiveness Act of 1987, the trade bill opposed, at least in part, by the Reagan Administration, calls for the establishment of an Interagency Coordinating Committee on Federal Participation in Sematech. The committee, to be chaired by the Secretary of Defense and to include the Secretaries of Commerce and Energy, the director of the National Science Foundation, and the chairman of the Federal Laboratory Consortium for Technology Transfer, would have broad responsibility to define the government's role in the program. If passed, the bill will empower the interagency committee to recommend the level of government spending for Sematech for each year through 1992 and to develop an arrangement through which government and Sematech officials will communicate. An aide to Sen. Jeff Bingaman (D-N.M.) stresses that a firm contractual relationship is not what Congress is after. "You need flexibility in running this thing. You can't strait-jacket it." □

MILITARY/AEROSPACE NEWSLETTER

FAST DEPLOYMENT OF SDI MAY SACRIFICE LONG-TERM RESEARCH GOALS

The Strategic Defense Initiative Organization, the office in charge of developing the "Star Wars" missile-defense system, is moving toward a near-term deployment that will sacrifice long-term research goals, according to a report released by Sen. William Proxmire (D-Wis.). The report concludes that early deployment—by 1994 or 1995—will result in a defense that is only 16% effective. Such a system would trade long-term research projects, such as development of laser or particle-beam weapons, for short-term development of "space-based kinetic kill vehicles . . . that would likely be able to destroy no more than 11% of the Soviet offensive threat;" ground-based interceptors would stop another 5%. The proposed system would also scrap plans to develop a "mid-course kill vehicle" that would track and destroy missiles after the critical boost phase of their flight. Mid-range technology was not expected to be workable until the end of the century. "There is evidence that [SDI] already is siphoning off funds from far-term technology research efforts to pay for increased emphasis on the near term," the report warns. □

GENERAL DYNAMICS TO GET ANSWER BY MARCH ON BID TO BUILD ADVANCED F-16

The Air Force Systems Command plans to complete and deliver by next March its evaluation of a proposal from General Dynamics Corp. to develop an advanced version of the F-16 fighter aircraft. General Dynamics, which builds the F-16 in Fort Worth, Texas, made the unsolicited proposal to the Air Force late last month. Dubbed the Agile Falcon, the enhanced fighter would have larger wings, more thrust, and improved avionics. Development costs would be $600 million, of which a third could be funded by Belgium, Denmark, the Netherlands, and Norway, which would also participate in production. General Dynamics says that if it gets the go-ahead, research and development work could begin by 1990, with first production deliveries in 1995. The proposed changes would add about $2 million per plane to the cost of today's $13 million F-16. General Dynamics is pitching the Agile Falcon as a low-priced complement to the Air Force's $35 million Advanced Tactical Fighter, which will go into production around 1995. □

GROUND COLLISION AVOIDANCE SYSTEM PASSES FINAL TESTING PHASE

The Air Force Ground Collision Avoidance System got through final flight tests in July and, if approved for installation, could soon be incorporated into large numbers of U. S. military aircraft. The system was developed by Cubic Corp. of San Diego, Calif., under a $1.5 million contract with the Aeronautical Systems Division at Wright-Patterson Air Force Base, Dayton, Ohio. Based on an algorithm that incorporates factors such as altitude, flight-path angle, and air speed, the system alerts pilots with visual and auditory warnings when a collision with the nearby terrain is imminent. No decision to incorporate CGAS into military aircraft has been made yet, but the system has strong support within the Air Force and Congress. For now, a user package including the algorithm is being assembled for evaluation. □

AIR FORCE INCHES TOWARD A LAN STANDARD

The Air Force will begin testing a local-area network scheme late this year that could become an Air Force standard. Four companies are bidding to run the tests and develop a catalog of hardware and software that could be used to support the Unified LAN Architecture. The winner, which should get the word shortly, will have three months to set up and begin an eight-month test at Gunther Air Force Base, Ala. The Air Force will then decide whether to proceed with the program, which could be worth $200 million. □

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NEW PRODUCTS

HP'S MODULAR LOGIC ANALYZER TESTS 400 CHANNELS AT 100 MHz

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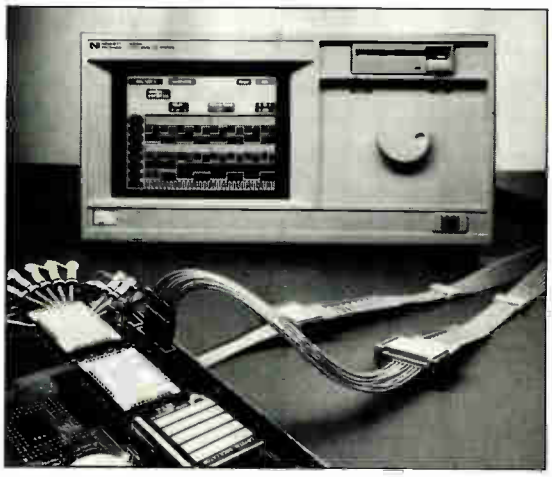
By building its new generation of high-performance logic analyzers around proprietary "analyzer-on-a-chip" technology that lets every channel operate at 25 MHz for state analysis or 100 MHz for timing analysis, Hewlett Packard Co. eliminates multiplexing, which is used with multiple channels to achieve high performance on other analyzers.

Moreover, the new chip reduces instrument size and costs because it replaces boards that are populated with more expensive emitter-coupled-logic parts. Although HP's three new instruments offer up to four hundred 100-MHz channels—50 times more than the company's 1630 series—they cost less than half as much per channel.



SOFT TOUCH. Designers can control up to 400 state-and-timing analysis channels with the 16500A's touch screen.

At the high end, HP's 16500A mainframe model can be loaded with five plug-in cards to get a total of 400 of these two-way channels. Each card provides five 16-channel chips organized as two coordinated analyzers. Both can operate as state or timing analyzers, or one can operate in the state mode while the other operates simultaneously in the timing mode.

Rounding out the family are two smaller units, the 80-channel 1650A and 32-channel 1651A, for applications where portability is important.

MIX AND MATCH. Users can configure a variety of logic-analysis systems in the five-slot mainframe by mixing and matching an 80-channel card, the 16510A, with three other plug-in instruments. These instrument cards include 16 channels of a 1-GHz timing analyzer; 12 or 48 channels of a 50-Mbit/s pattern generator; and two channels of a digital oscilloscope with single-shot and repetitive-input bandwidths to 100 MHz at sampling rates of up to 400 megasamples/s.

The key component of all three instruments is the Elan "analyzer on a chip," a 140,000-transistor circuit produced with HP's 1.5-μm n-MOS III technology. The instruments derive their flexibility from multiple Elans—two in the low-end 1651A, for example, and five each in the 1650A and the 16510A card for the mainframe unit.

Each 16-channel chip operates on all channels in either of two modes: as a 25-MHz state analyzer, or as a 100-MHz timing analyzer. The Elan also contains a high-speed recording memory with 1 Kbit/channel. Producing an instrument with comparable power using emitter-coupled logic would cost up to 12 times as much, according to estimates by Daniel Ackerhelm, the engineering project manager at HP's Instruments Division in Colorado Springs, Colo.

Taking a closer look at the 16500A bench model shows it to be the size of a conventional logic analyzer. Configured as a 400-channel logic analyzer using the 16510A card, the system costs $65/channel, plus the $7,200 cost of the mainframe, for an average of $83/channel. The 1-GHz analyzer, pattern generator, and oscilloscope also expand at a declining cost per channel. An intermodule bus enables all the card-instruments to trigger one another and to make time-correlated measurements.

The 16500A has just one control knob. Menus appear on a color-coordinated display. Selections are made through a touch screen or by using a mouse-controlled pointer, instead of a conventional front panel. Optional software packages integrate the 16500A with HP's Electronic Design System, a work-station-based system for computer-aided engineering. For example, the work station can be used to program and control the instruments, exercise a prototype design with test vectors derived from the CAE simulation programs, and feed back measurement data from the instruments into the CAE design models.

HP recommends the portable, 32-channel 1651A for debugging and troubleshooting 8-bit microcomputers. With its two 16-channel pods, for example, the 1651A can simultaneously monitor a microprocessor's program execution in the state mode and check the input/output ports in the timing mode.

The 1650A's five pods give it enough channels and flexibility for 8-bit to 32-bit microcomputers and minicomputers, HP says. And to leave bugs no place to hide in multiprocessors, 16500A users can organize the mainframe's 400-channel capacity into as many as 25 pods and 10 correlated analyzers.

The 1650A and the 1651A portables have a front-panel keyboard and pop-up menus. They cost around $100/channel.

All three instruments have the same basic triggering and control functions. These include five clock inputs, four clock qualifiers, eight sequence levels, eight pattern recognizers, and a range recognizer. Also, users can specify which states or software routines will be stored in memory. Likewise, they all have a transitional recording mode (logging only state changes) to extend recording time during timing analysis. At 100 MHz, recording time ranges from 10.24 μs to 5,000 s, depending on input activity.

All three instruments also have a 3½-in. disk drive for storage of setups and measurements, and an RS-232-C port. The 16500A also interfaces with the HP-IB and IEEE-488 instrumentation buses.

The instruments can be ordered now for delivery in 4 to 12 weeks. The 16500A mainframe costs $7,200. The standard 16510A 80-channel logic-analysis module costs $5,200. The 1-GHz tim-

ing analyzer starts with 16 channels on a $7,800 master card and expands up to 80 channels by adding 16-channel cards at $6,500 each. The 50-Mbits/s pattern generator starts with 12 channels on a $3,700 master card and expands to 204 channels with 48-channel slave cards at $4,000 each. The 100-MHz oscilloscope requires a $1,500 timebase card and expands to 8 channels with 2-channel cards at $4,800 each. The portable 1650A costs $7,800 and the 1651A, $3,900. The CAE link software and the data-file comparator cost $2,000 each.

–George Sideris

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Rd., Palo Alto, Calif. 94303. [Circle 380]

3-IN-1 TESTER HANDLES CHIPS, BOARDS, SYSTEMS

A triple-threat tester from Step Engineering lets designers verify each level of their designs—chips, boards, and systems—with just one instrument. By eliminating the expense of purchasing separate application-specific integrated circuit verifiers, board testers, and system testers, the $53,000 Step Design Analyzer delivers considerable savings—a comparable dedicated ASIC verification system alone, for example, could cost more than $100,000.

Testing is controlled with an IBM Corp. Personal Computer AT or compatible. The PC AT—which is not included in the system's base price—handles the test program, the sequence of stimuli to apply to the device under test, and the response information. Up to 384 stimulus channels and 256 response channels can be configured inside the analyzer's desktop chassis.

FAST. The tester can simultaneously produce a stimulus and acquire a response at a rate of 50 MHz. In addition, the tester can determine the setup-and-hold time of a device under test with a resolution of 500 ps. Responses from the unit under test are captured in a buffer of 4 Kbits. An optional 16-Kbit buffer is also available.

Test heads are not provided with the tester, so customers can configure their own test heads for chips, boards, and systems.

The analyzer comes with special pods for connecting the stimulus and response electronics to the pins of the designer's test fixtures. The stimulus and response electronics have built-in compensation for the length of the cable, to provide maximum signal integrity and to allow the tester to operate at its high 50-MHz data rate.

In developing the system, the Sunnyvale, Calif., company used expertise it has already developed internally in three areas: designing high-speed memory, handling high-speed signals over cables, and developing software for capturing randomly occurring events.

User software includes the SDA Monitor, which executes on the PC AT. It provides the user access to system resources, such as the company's high-level test-programming language called AutoStep, an automatic test-creation software package called Script, and several editors for defining symbolic names and manipulating the test data.

AutoStep is a structure-test program language that the designer uses to direct the application of various tests in a suite developed for the unit under test. Script is an automated editor that tracks and records all keyboard sequences the designer goes through in debugging a test sequence. The sequences can then be edited by the designer to create a final test program.

For writing test patterns—the 1s and 0s used to stimulate the unit under test—the system offers MetaStep, a high-level language that speeds test-pattern development. Another software package called DefUDS—user-defined symbolics—allows the designer to define symbolic labels that may be used instead of binary and hexadecimal representations to manipulate data. Finally, EdStim (for editor stimulus) and EdResp (for editor response) allow the designer to modify stimulus and response data easily. Although designed as a functional tester, the system can be configured to perform parametric testing as well. It is available now.

–Jonah McLeod

Step Engineering, 661 E. Arques Ave., P. O. Box 61166, Sunnyvale, Calif. 94088. Phone (408) 733-7837 [Circle 381]

INTEGRITY. Built-in cable-length compensation helps the tester to operate at its high 50-MHz data rate.

BOARDS GIVE MAC II INSTRUMENT CONTROL

The Analog Connection, a set of add-on boards and associated software from Strawberry Tree Computers Inc., gives Apple Computer Co.'s Macintosh II data-acquisition and control capability.

By taking advantage of the Macintosh's easy-to-use graphical interface and a mouse, the software lets users set up a laboratory or factory-floor control system the same way a draftsman would create a block drawing of the application.

Six add-on boards for the Macintosh II offer up to 16-bit resolution on up to

16 analog input channels, as well as 16 digital input/output lines and optional analog output channels.

Available now, the boards range in price from $795 for the ACM2-12-8 (eight 12-bit analog inputs and eight digital I/O lines) to $1,845 for the ACM2-16-16 (sixteen 16-bit analog inputs and 16 digital I/O lines). Analog Connection Workbench software costs $495.

Strawberry Tree Computers Inc., 150 N. Wolfe Rd., Sunnyvale, Calif. 94086. Phone (408) 736-3083 [Circle 385]

OPTICAL CONVERTERS CUT COSTS BY 66%

A pair of probe-sized optical/electrical converters from Tektronix Inc. allows the company's 11000 Series oscilloscopes to analyze mixed analog and digital electrical signals and optical signals simultaneously for as little as one-third the price of competing products.

The P6701 offers a bandwidth of dc to 700 MHz, and a waveform response of 450 nm to 1,050 nm. The P6702 has a dc to 500-MHz bandwidth and a waveform response of 1,000 to 1,700 nm. Together, they cover the optical characteristics of most popular fiber-optic communications bands. Available now, the P6701 costs $1,800; the P6702, $1,995.

Tektronix Inc., P. O. Box 1700, Beaverton, Ore. 97075. Phone (800) 547-1512 [Circle 386]

The device's EPLD core, says Laws, allows the user to implement any mix of combinatorial and sequential logic. The programmable core consists of two identical macrocell blocks and can be independently configured as combinatorial output or as D-, T-, JK-, or SR-flip-flop outputs. Each flip-flop has its own programmable asynchronous clear, and two product terms with programmable output polarity for individual clock generation.

The bidirectional generic slave interface on the bus port, Laws says, can be user-defined for virtually any microprocessor.

Multiple devices can be operated in parallel to allow interfacing with 16- or 32-bit processors for more complex functions.

The byte-wide input registers on the EPB1400 can be configured to operate in either a flow-through or edge-triggered mode. Synchronous strobe signals from designated pins allow high-speed control of transfers to and from the processor.

Special feedback options optimize macrocell operation. One option allows the register contents to be buried, freeing the register output pin as an input. Another uses these input pins and transforms the output latch into another input latch. A third option controls the macrocell output with an independent three-state control function.

Packaged in a 40-pin dual in-line plastic or Cerdip, samples of the EPB1400 are available now for $25 each.

–Bernard C. Cole

Altera Corp., 3525 Monroe St., Santa Clara, Calif. 95051.
Phone (408) 984-2800 [Circle 362]

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Plessey Semiconductors' 700-MHz emitter-coupled-logic line receiver/driver for clock buffering and distribution boasts rise/fall times and propagation delays of just 800 ps—twice as fast as the 1,500 ps of competitive devices.

The SP92701 offers differential inputs and outputs and an on-chip reference, permitting every combination of single-ended, differential, inverting, and noninverting operation.

A current source provided in the input stage makes the part suitable for more general applications, such as operational amplifiers, where low propagation delays are required.

The SP92701 is available in 8-pin plastic and ceramic packages priced at $2.20 and $3.30, respectively, in quantities of 1,000 and up.

Plessey Semiconductors, 3 Whatney Ave., Irvine, Calif. 92718.
Phone (714) 951-5212 [Circle 365]

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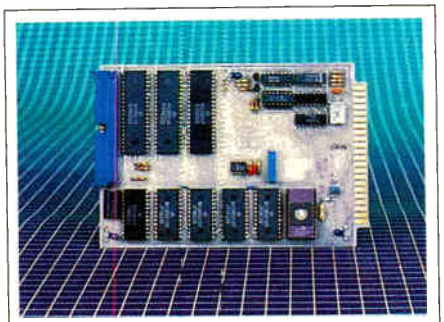

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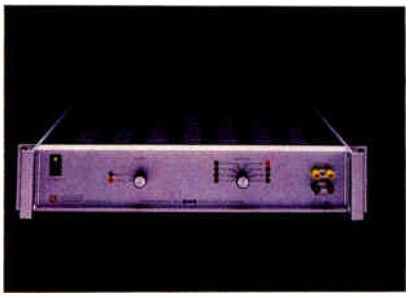

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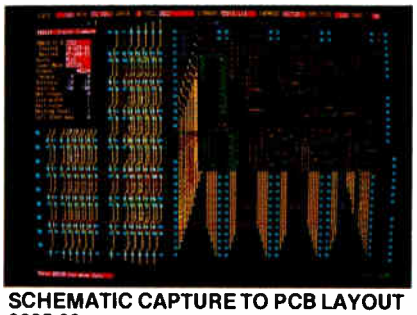

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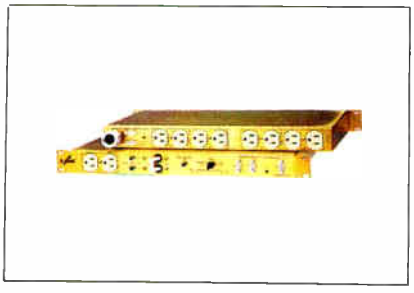

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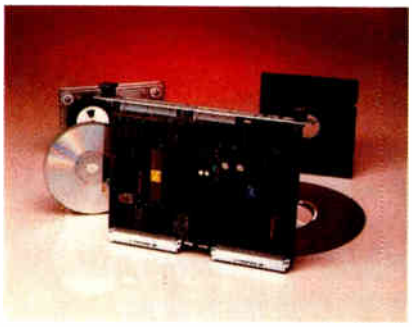

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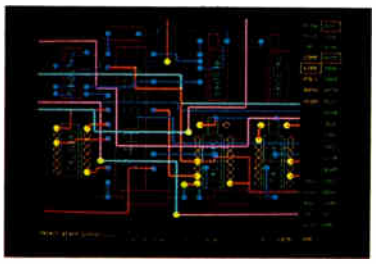

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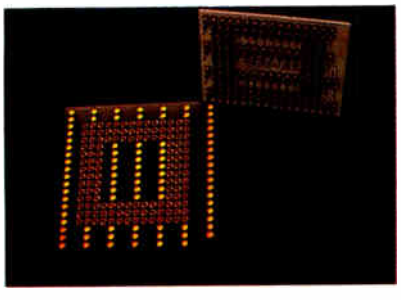

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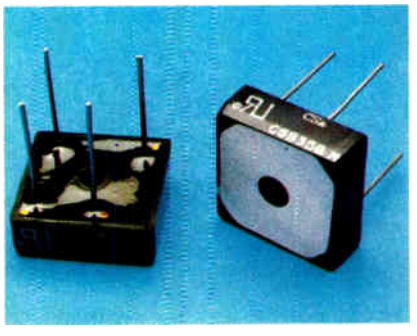

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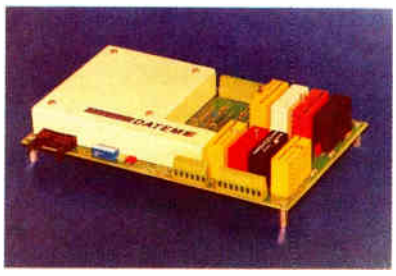

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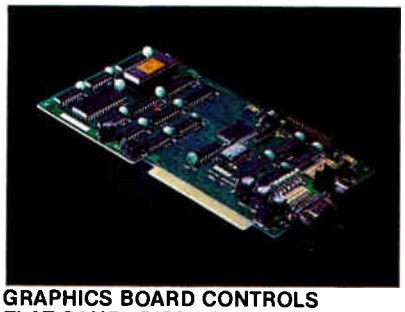

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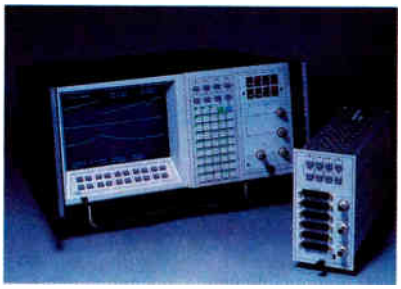

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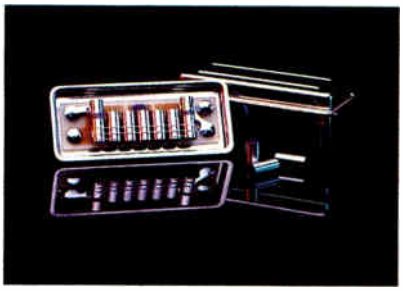

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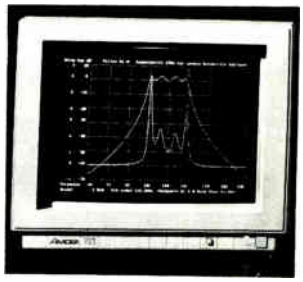

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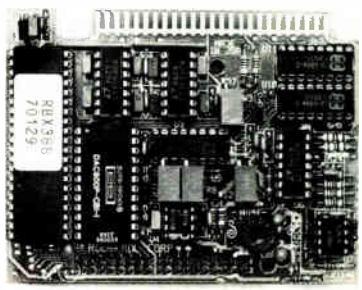

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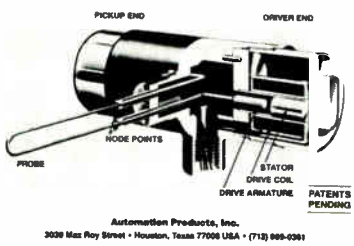

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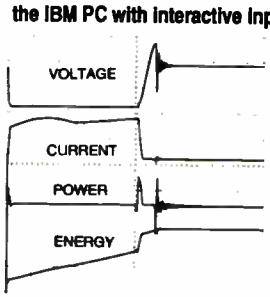

These waveforms show an IS_SPICE analysis of a power supply snubber. Intu_Scope was used for display and computation of power and energy. The output shown used an Intu_Scope plotter utility

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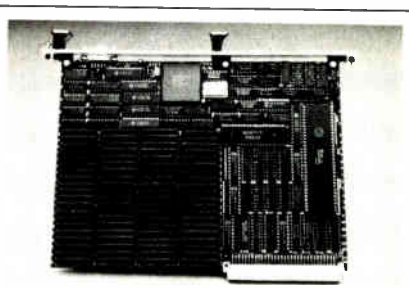

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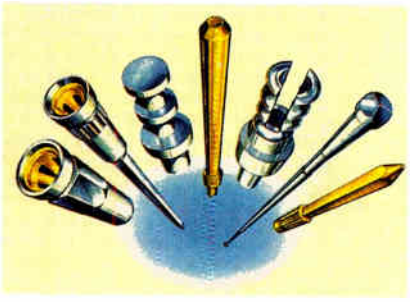

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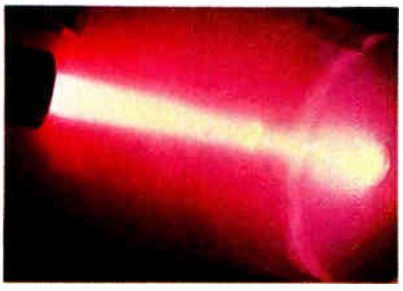

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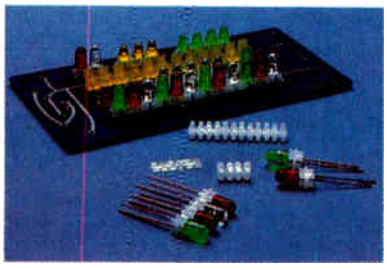

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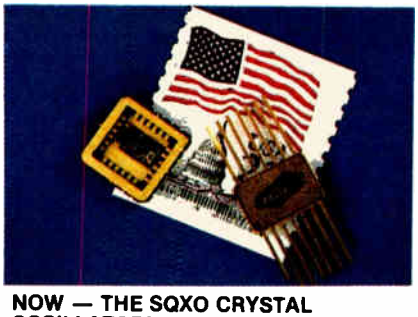

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Negotiate, monitor and oversee OEM and development contracts. Experience in administering S/W development contracts required.

Senior H/W-S/W Applications Engineers

Support the design-in of the Am29000 using your experience in H/W and S/W design of digital systems in computers and imbedded controllers. System architecture, strong communication skills and strength in H/W and S/W system performance optimization are a big plus.

Software QA Applications Engineers

Develop test plans and perform S/W QA testing, develop and implement test suites for O/S, compilers and assemblers and develop tools and utilities to aid in testing.

Applications Engineers

Join in the design and support of Am29000 demo/evaluation boards and systems, do customer support and publish documentation. You will need experience in H/W design of digital systems and familiarity with assembler, C, UNIX, and MS DOS.

Documentation Specialist

Maintain the documentation for Am29000 support tools as well as generate documentation for user and reference manuals for new tools. Technical writing with emphasis on S/W tools such as compilers, assemblers, debuggers is required.

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ELECTRONICS WEEK

IBM RESEARCHERS BUILD ULSI DEVICES

Scientists at IBM's Thomas J. Watson Research Center have opened the age of ultra-large-scale integration with experimental chips made in 0.1-μm technology. The Yorktown Heights, N.Y., researchers employ electron-beam lithography to build n-MOS FETs with gate lengths down to 0.07 μm and switching times as fast as 10 ps when operated at a temperature of 77.5 K. Transconductance of the devices is 750 mS/mm. That's the highest value ever measured for a silicon transistor, says IBM.

INTEL FILES PATENT SUITS

Intel Corp. has filed actions in U.S. District Court in San Jose, Calif., charging Hyundai Electronics America Inc. and other defendants with patent infringement. Intel has also asked the U.S. International Trade Commission to initiate an investigation of alleged patent infringement in the importation of erasable programmable read-only memories. George Perlegos, president of Atmel Corp., a U.S. design firm, has been named as a co-defendant in one of the suits; a former Intel employee, Perlegos's name appears on several Intel EPROM patents. The other suit involves dynamic random-access memories and names Vitelic Corp. and Hyundai as codefendants.

ZENITH LANDS DOD LAPTOP CONTRACT

Zenith Data Systems, No. 1 in laptop computers, has bagged another major government contract—this time to supply machines to the Pentagon. Under the $104 million pact, Zenith will supply 90,000 Z-180 laptops [*Electronics*, June 16, 1986, p. 26] over the next three years. Its Japanese-built, 80C88-based Z-180 machine reportedly beat out Toshiba Corp.'s entry. Last year the Zenith Electronics Corp. subsidiary won a $27 million contract to supply laptops to the Internal Revenue Service [*Electronics*, March 3, 1986, p. 16].

AT&T GETS MS-DOS FOR 386 SYSTEMS

AT&T Co. has licensed software jointly developed by Phoenix Technologies Ltd. of Norwood, Mass. and Interactive Systems Corp. of Santa Monica, Calif., that will transparently run MS-DOS applications under Unix on AT&T's 80386-based systems. VP/ix software integrates DOS into the Unix operating environment by connecting Unix to Phoenix's IBM PC emulation environment, enabling Xenix/Unix users to run multiple DOS applications simultaneously on an 80386-based system.

TI CHIP GROUP REORGANIZES

Six months after he was named president of Texas Instruments Inc.'s Semiconductor Group, corporate executive vice president William P. (Pat) Weber has reshuffled the top ranks so that top managers now exercise global control over products, rather than divvying up portfolios by world regions. Wally Rhines, ex-president of TI's Data Systems Group in Austin, who is back in the Semiconductor Group as senior vice president, is now worldwide strategic manager for system-level integrated circuits. The move parallels TI's effort last year to reduce its bureaucracy by centralizing memory-chip management in Japan [*Electronics*, June 2, 1986, p. 11].

BELLCORE FILES BATTERY PATENT

Bell Communications Research, also known as Bellcore, has filed a patent for a new rechargeable lithium battery that is both compact and efficient. Unlike previous lithium batteries, this one uses a cathode of silver molybdenum sulfide, and it is easily recharged and operated at room temperature. The batteries have a higher power-to-weight ratio than conventional rechargeables, and they can be easily formed into a thin-film cell. Applications range from maintaining information in integrated circuits to providing more energy-efficient automotive batteries.

A LEANER LATTICE FINE-TUNES FOCUS

Lattice Semiconductor Corp. is set to emerge from Chapter 11 this fall, and the company is taking austerity measures to ensure profitability and competitiveness. A departmental reorganization has cut the number of employees from 82 to 70, and company-wide reductions in overhead will let Lattice continue to invest in manufacturing and in research and development. The company will focus primarily on manufacturing its Generic Array Logic, or GAL, devices to meet growing demand.

ZENITH BUILDS VERTICAL VCRs

Zenith Electronics Corp. has a new angle on video cassette recorders. The Glenview, Ill., company's 1988 consumer-electronic product line includes two vertical VCRs—a configuration believed to be an industry first. The two VHS units, designed as space-saving alternatives to conventional horizontal VCRs, are 6 in. wide and 1 ft. tall. They will sell for $600 and $900.

SPRINT UPGRADES WITH GTE SYSTEM

Long-distance carrier US Sprint will install a new network-management system later this year to oversee its nationwide switching network. All calls from Sprint's 5 million customers will go through a new control center in Kansas City, Kans. Built by GTE Government Systems Corp. of Waltham, Mass., the $6.1 million management system allows operators to isolate problems in individual switches or regions, automatically reroutes traffic, and provides surveillance capability for regional US Sprint centers.

SEQUENT WON'T SHIP SYMMETRY YET

Sequent Computer Systems Inc., Portland, Ore., is delaying shipment of its Intel 80386-based Symmetry line of computers, citing limited performance of the machine's proprietary copy-back cache [*Electronics*, May 28, 1987, p. 76]. The parallel-processing Symmetrys are designed to match mainframe performance—up to 81 million instructions/s with 30 processors—at a fifth the cost, but the crucial CMOS chip developed for the copy-back cache can't keep up with these speeds yet. Symmetry systems equipped with a write-through cache will be shipped this fall, and Sequent spokesmen say the copy-back cache will appear when the bugs are out; the target date they've set is spring 1988.

STERN RESIGNS POST AT UNISYS

In a move that took industry analysts by surprise, Unisys Corp. president and director Paul G. Stern, 48, has resigned. Word of Stern's departure, effective Dec. 31, came as part of an announcement that the Detroit computer maker is realigning its management structure. An eight-man management board will be formed, with each man having responsibility for a major segment of the company, and each reporting directly to chairman W. Michael Blumenthal. Until now, a four-man executive board, including Blumenthal and Stern, has been responsible for all top-level decisions. Stern was an executive with Burroughs when it merged with Sperry to form Unisys.

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2	17	32	47	62	77	92	107	122	137	152	167	182	197	212	227	242	257	272	349	364	379	394	409	424	439	454	469	484	499	704	719
3	18	33	48	63	78	93	108	123	138	153	168	183	198	213	228	243	258	273	350	365	380	395	410	425	440	455	470	485	500	705	720
4	19	34	49	64	79	94	109	124	139	154	169	184	199	214	229	244	259	274	351	366	381	396	411	426	441	456	471	486	501	706	900
5	20	35	50	65	80	95	110	125	140	155	170	185	200	215	230	245	260	275	352	367	382	397	412	427	442	457	472	487	502	707	901
6	21	36	51	66	81	96	111	126	141	156	171	186	201	216	231	246	261	338	353	368	383	398	413	428	443	458	473	488	503	708	902
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14	29	44	59	74	89	104	119	134	149	164	179	194	209	224	239	254	269	346	361	376	391	406	421	436	451	466	481	496	701	716	959
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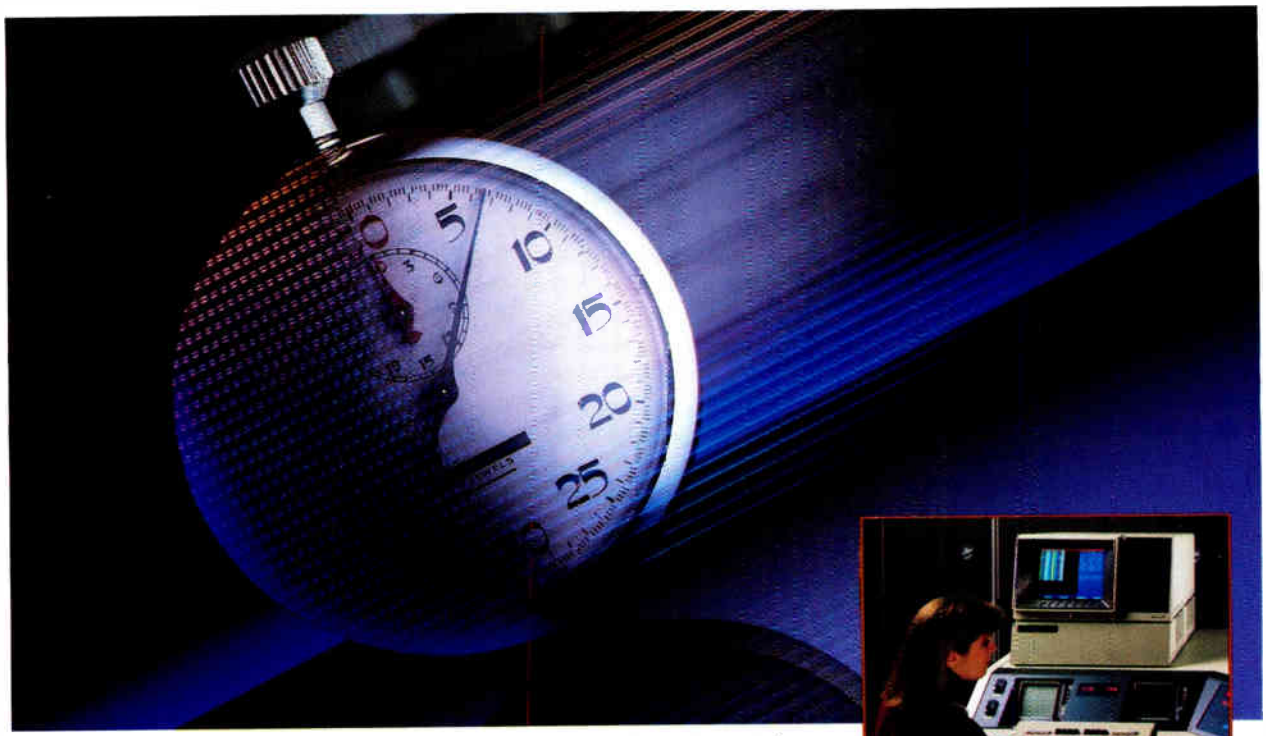

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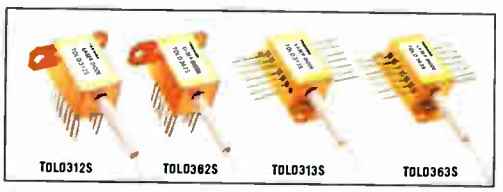

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