SPECIAL ISSUE

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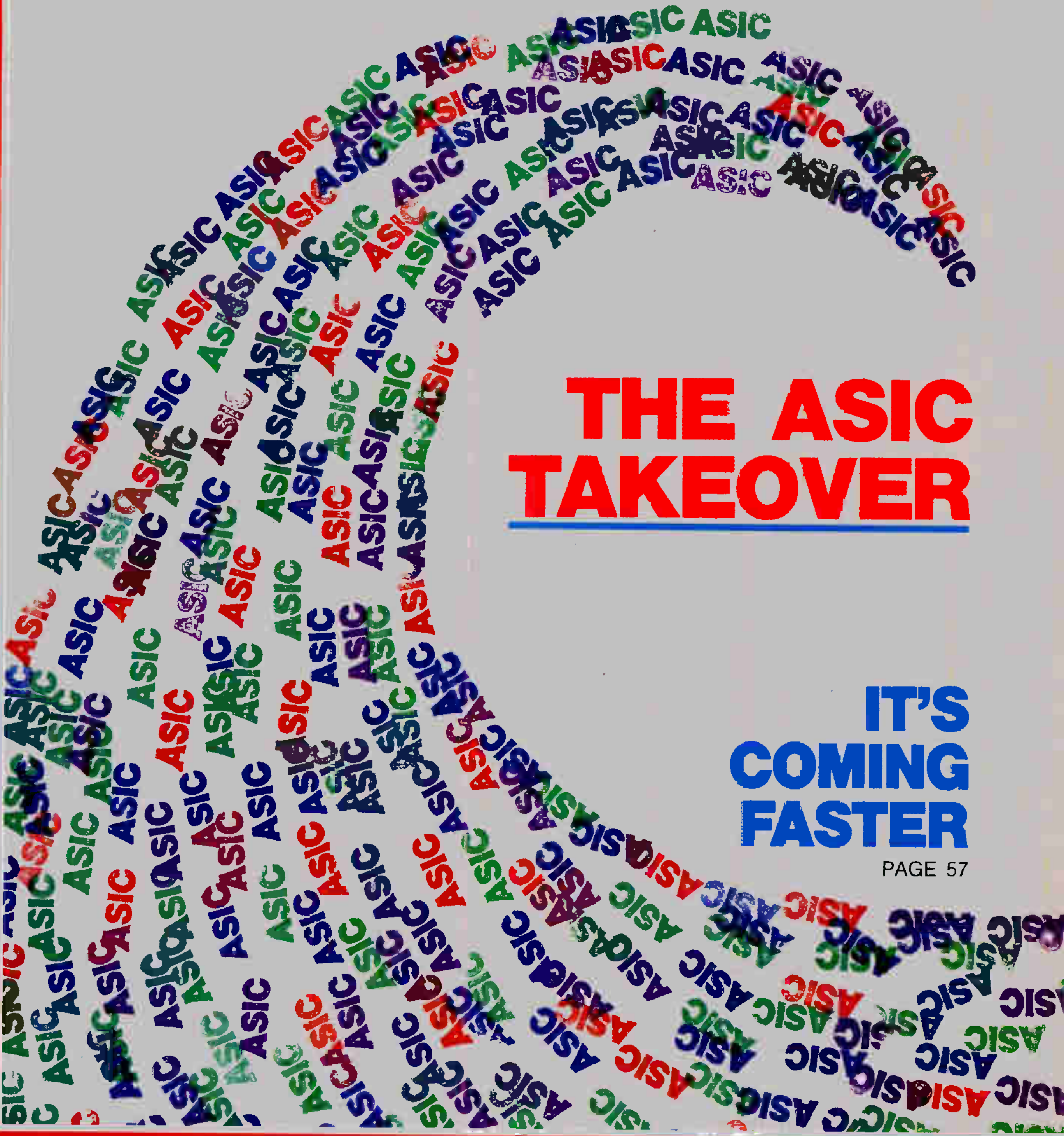

THE ASIC TAKEOVER

IT'S COMING FASTER

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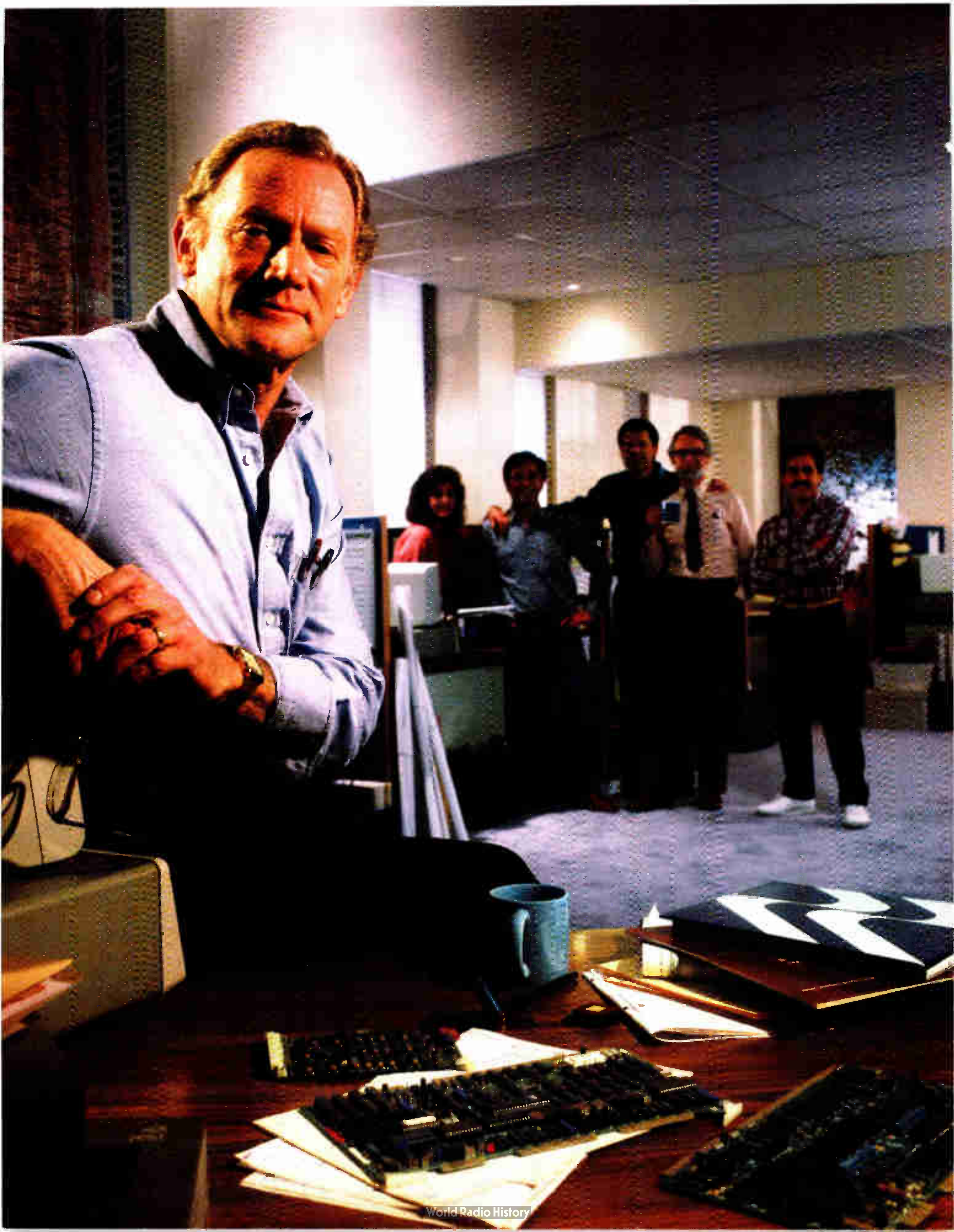
National Semiconductor



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And you're not "stuck" at any level. Once you're comfortable with your programmable-logic design, for example, you can integrate the PLDs and glue logic into a gate array.

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We get downright finicky when it comes to deciding whether to label an upcoming issue of *Electronics* as a Special Issue. While other publications may append such a superlative to cover a multitude of stories, we do it only when we feel the topic is of critical significance to our readers and to our industry. Until this issue, for example, the only subject in 1987 to earn this appellation was our special semiconductor issue in April. We now publish our second special issue this year on application-specific ICs. It's our kind of story—no other publication could cover the multifaceted panorama of ASICs from technology to marketing.

Our timing couldn't be better. No one development is having a more significant impact on our industry and its products now than are ASICs. As Stan Runyon, who managed this special issue, puts it, "For our readers, the users, it's time to rethink how they do things. They must either increase their investment in computer-aided engineering and design their own or else form a close alliance with an ASIC house.

"In working on this issue, we picked up two major trends. First, in four years at least half the standard-logic market of $16 billion will be taken over by ASICs. Second, although ASIC gate arrays now have the major share of sales over standard cells, that lead is shrinking as standard cells come on strong. The result is that chip vendors are scrambling to build libraries of standard cells.

"This is causing a realignment of the big chip makers, as well as the appearance of new players: system houses, such as NCR, that have been doing semicustom work internally and now see a chance to market their products. And it leaves the original semicustom chip producers like VLSI Technology and LSI Logic looking for new avenues. What they're coming up with is 'semistandard ASICs'—in effect, catalog parts. Ironically, that's just what their new, big rivals are getting away from."

This special issue is impressive in size as well as scope. There are 14 articles taking up 24 pages, covering everything from chip architectures to company strategies. It all got started just three months ago when Los Angeles bureau manager Larry Waller discovered the ASIC work of the large chip makers was quietly becoming very significant.

The editorial team that covered this was directed by Runyon and Jeremy Young and included Waller, Tobias Naegele, Bernie Cole, George Sideris, Jonah McLeod, Rob Lineback, Steve Rogerson, John Gosch, and Charlie Cohen. Add production editors, and you get upwards of a dozen people involved, or more than some competitors have on their entire staffs.

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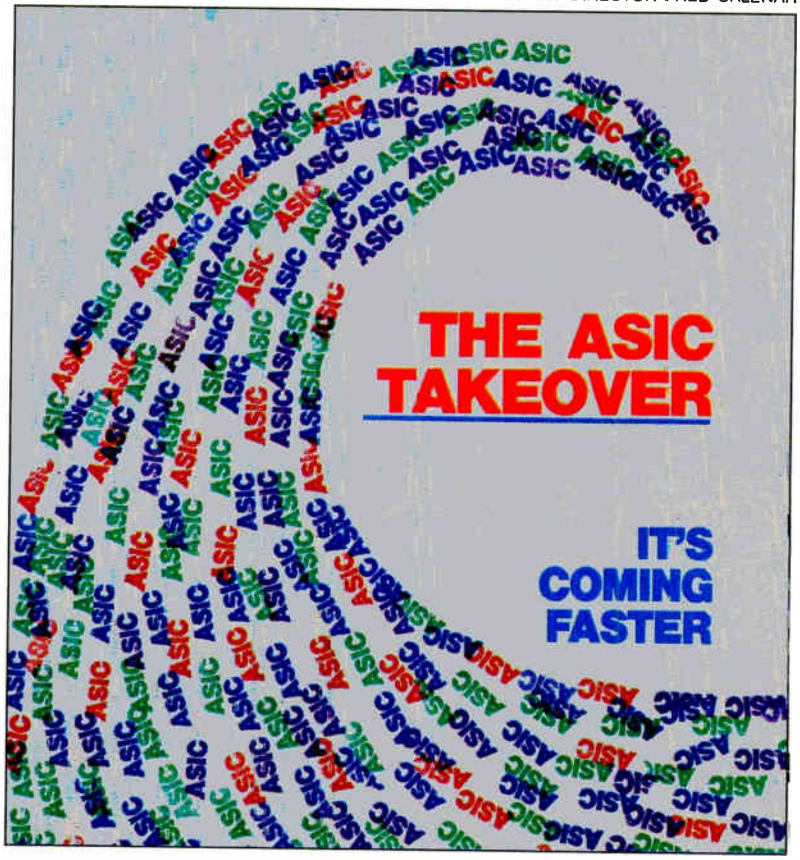
NEWS

SPECIAL ASIC ISSUE

INSIDE TECHNOLOGY

COVER: ART DIRECTOR FRED SKLENAR



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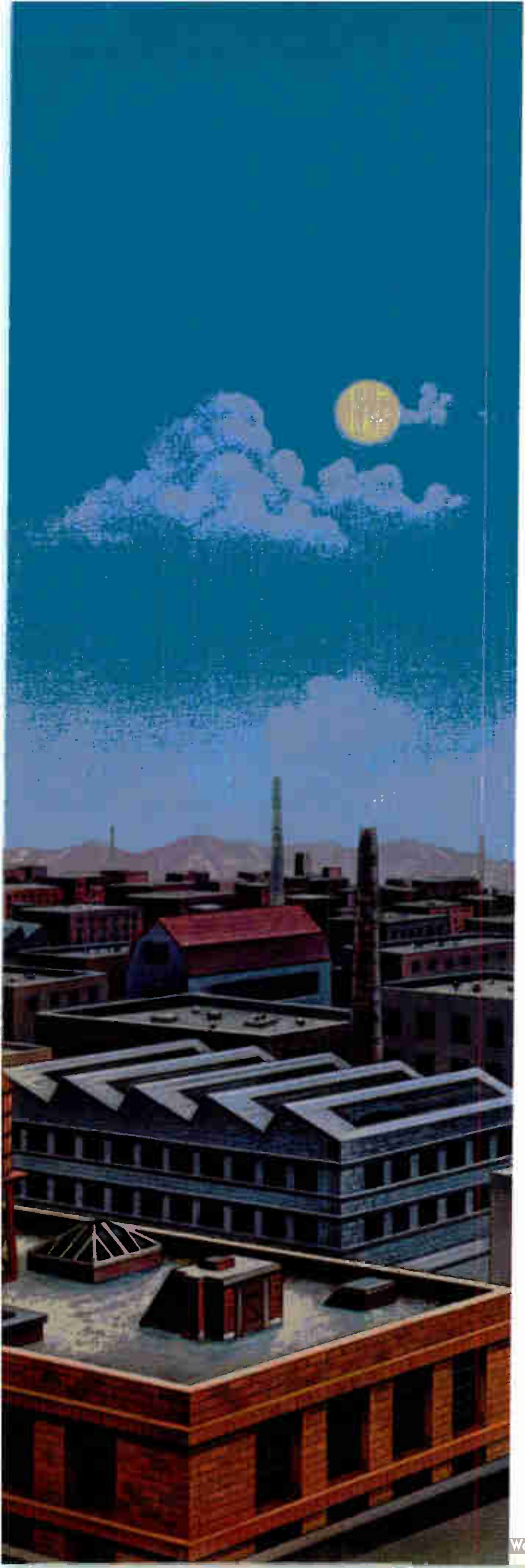
NEW PRODUCTS

DEPARTMENTS



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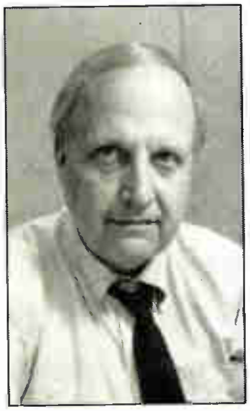
Sematech is on its original schedule, if not ahead of it; the chip-manufacturing consortium has informal commitments for money from 80% of the U.S. production base



I don't have to be hit on the head with a hammer too many times to get the picture. A veteran production expert had told me earlier [*Electronics*, June 25, 1987, p. 8] that Sematech, the proposed U.S. semiconductor manufacturing consortium, could not have an effective demonstration program with the modest production rates it currently plans. Several senior industry executives have since told me that's baloney. Developing high-volume production processes, they insist, doesn't have to be done in a high-volume environment.

One of those executives is Gil Amelio, president of the Semiconductor Products Businesses at Rockwell International, who is spending much of his time these days on Sematech. "Under our current plan, Sematech will be pushing production equipment to the maximum," he maintains; "100 to 200 wafer starts a day will pretty much exercise this equipment."

Three months have gone by since industry leaders laid out their plans to set up a consortium aimed at turning U.S. chip making into a basic commodity and reaching the same level of manufacturing capability as the Japanese. While we expected to hear more details on financing and startup plans by now, Amelio maintains that things are moving right along.

"We're on our original schedule, if not ahead of it. We have informal commitments for money from 80% of the U.S. semiconductor base." On matching funding from the government, he insists that "government money is not a gating item; I'd be tickled if we got something by January." Such funding was always expected from state and local, not just federal, governments, he notes. And Sematech has already received 50 proposals from state and local governments to set up the consortium locally, with "most of them proposing to make significant financial contributions." Sematech still expects to announce where it will be located as well as its two senior operating executives by the end of the summer. "We're on track here," Amelio says. "For one thing, we were flabbergasted by the number and quality of senior job applicants.

"We've plotted our course to intersect where the Japanese will be in 1992," Amelio says. "Our production process will be clearly below 0.5 μm, which presupposes X-ray lithography or something like that." And although chip makers are concentrating now on the start-up phase, "there's a good chance of Sematech going beyond six years," he says. "If it works well, it could go on forever."

ROBERT W. HENKEL

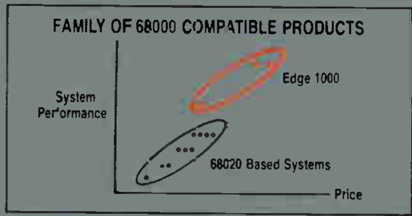
68000™ FAMILY UPDATE

AUGUST, 1987

COMPUTER DESIGNER HOLDS KEY TO 68000-FAMILY SYSTEM MARKET GROWTH

OEMs and System Integrators designing their systems around microprocessors in the 68000 family now have a cost-effective low-risk expansion path into the high performance market arena. By implementing the Motorola 68000 family instruction set in CMOS VLSI gate arrays, Edge Computer Corporation has set in motion a continuum of 68000-compatible computing. Current Motorola customers can economically add a high-end system to their product family almost immediately—without compromising software compatibility. By adapting a new design element concept now available from Edge Computer Corporation, OEMs, and SIs can offer their customers more than 11 sustained MIPs performance, 30MB sec I/O bandwidth, 64MB of main memory, GSX (AT&T™ UNIX™ V.2 with Edge and Berkeley enhancements), 38 8" disk drives, and 500+ user capability.

Equally important, the modularity of the Edge design element (which is offered at a more sophisticated completion level than merchant chips), allows customers to add value (peripherals, controllers, software, etc.) in those areas that are most profitable. The Edge design element insures the current Motorola customer continued software compatibility and performance growth without costly architectural redesigns.

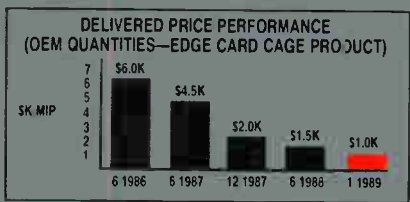


MOTOROLA CISC INSTRUCTION SET MACHINE WITH RISC-LIKE EFFICIENCY

The best performance features of CISC and RISC have been combined to produce a SIP (Streamlined Instruction Processor). At 1.5 Instructions Per Cycle, the new processor, developed by Edge Computer Corporation, has a lower AIT (average instruction time) than any current CISC or RISC system. Furthermore, Edge delivers RISC-like performance without the "risk" of 68000 software incompatibility. Edge's performance and compatibility advantages result from an advanced CMOS VLSI implementation of a Harvard supercomputer architecture that simultaneously fetches instructions and operands over multiple 32-bit buses. The high-performance dual 4-staged pipelined processor is specially designed to execute 68000 family instructions extremely efficiently. In fact, most instructions are executed in one cycle.

1 MIP PER $1K SYSTEM PERFORMANCE BEFORE 1990

As the chart indicates, Edge Computer Corporation has already lowered the high cost of high performance computing. But the company is equally dedicated to the future needs of its customers. Edge's continuum of compatible computing strategy will not only guarantee sustained 68000 family software compatibility, it will enable the OEM to economically capitalize on the market's ever-growing demand for increased number of users and computational power. Before 1990, prices for Edge technology (in OEM quantities) will have been cut to $1K per MIP. OEMs will be assured the winning edge essential to their profitability, even the future, of their companies.



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PEOPLE

WHY PAMPEL WON'T CHANGE THINGS AT APOLLO

CHELMSFORD, MASS.

Although Roland D. Pampel has just succeeded Thomas A. Vanderslice as president at Apollo Computer Inc., don't expect any major changes in strategy or direction. But if what's past is prologue, as Shakespeare wrote, look for an even firmer commitment to network computing and Unix at the Chelmsford, Mass., work-station leader.

While Vanderslice relinquishes the presidency to Pampel, he remains closely involved in the company's direction as chairman and chief executive officer. Pampel, an engaging and loquacious 52-year-old "going on 29," came to Apollo in January 1986. Before his promotion, he was serving as senior vice president for technology, manufacturing, and marketing. "His appointment early last year was a key element in my long-term corporate strategy, aimed at integrating marketing, research, plus sales and service activities, into focused, cohesive units," Vanderslice said in the announcement.

For his part, Pampel says his stewardship will foster a continuum. "Tom and I have worked hand in glove in the last year and a half. Our employees won't notice any change." His specific duties now include directing and overseeing activities of the marketing, manufacturing, R&D, North American sales, North American customer services, and Federal Systems organizations.

NETWORKING. Significantly, his experience includes a vice presidency for systems marketing and development at the company that pioneered the Unix operating system—AT&T's Computer Systems Group. And his 22 years at IBM Corp. included a stint as the general manager and laboratory director for the Kingston, N. Y., facility. There Pampel managed the initial development of the Systems Network Architecture.

It isn't surprising, then, to hear Pampel say, "I'm a hawk on network computing and Unix. I come from a strong systems and communications background, and will continue Apollo's strong emphasis in those areas." In fact, Pampel is credited with having a major role in starting Apollo on a course to bring Unix aboard its work stations as a native operating system [*Electronics*, May 28, 1987, p. 45].

Pampel recognized early that Apollo needed to spend "a lot more money" to fully support Unix System V.3, and he made sure that commitment was made. Similarly, Pampel was an early backer

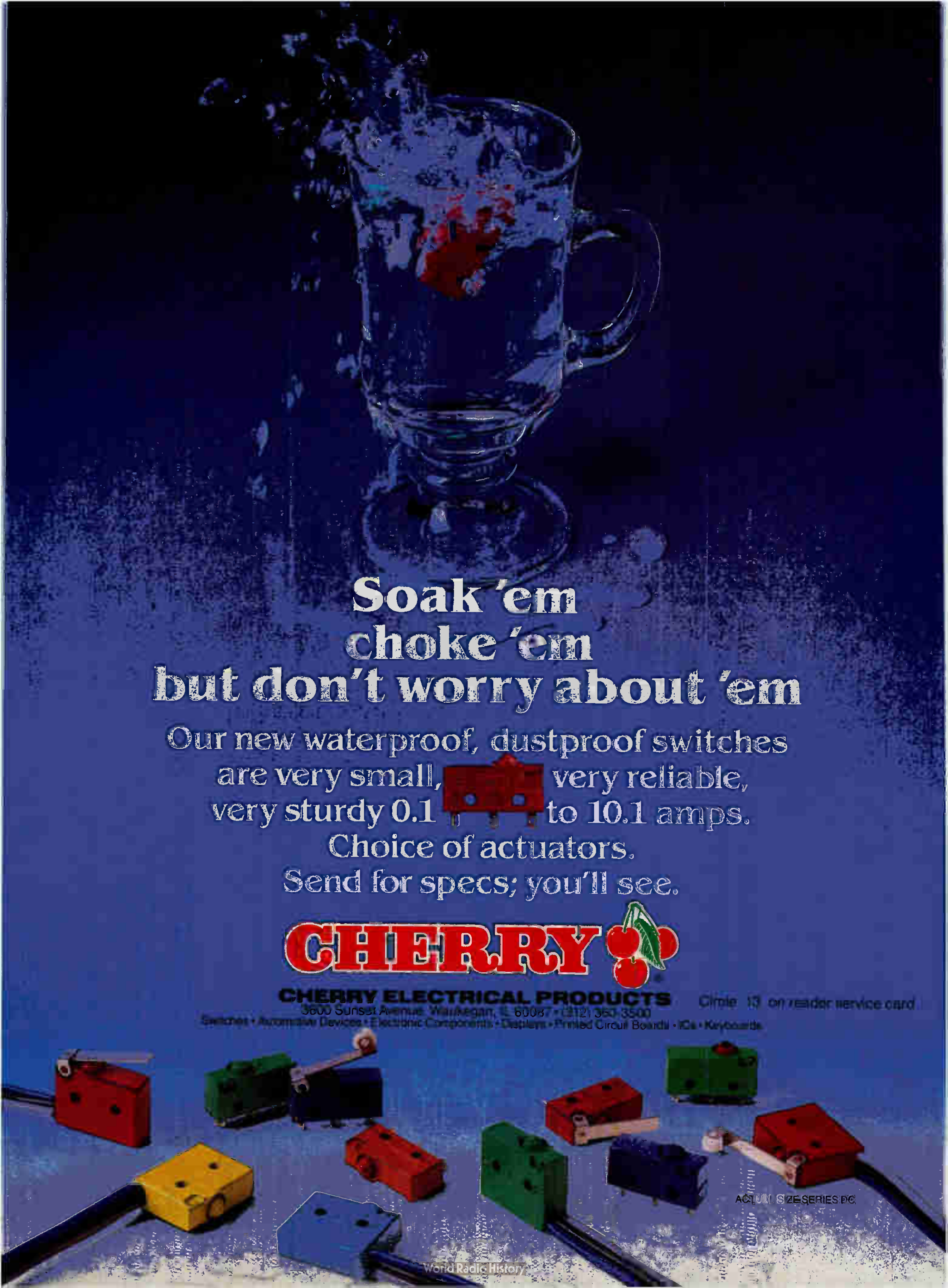
PAMPEL: "Tom [Vanderslice] and I have worked hand in glove in the last year and a half."

of Apollo's Network Computing System concept [*Electronics*, March 5, 1987, p. 9], which wasn't fully funded when he arrived. NCS makes it possible to write application programs that can be distributed for execution across a broad variety of multivendor networks. Not long after he arrived, Pampel boosted NCS funding to raise the number of people working on the project from nine to fifteen.

"Our customers keep asking how they can integrate all these heterogeneous resources into true network computing, and I'll keep pushing us to come up with the most effective ways to do that," Pampel asserts.

LEAPING COMPUTERS. Nor does he see an end to the leapfrogging that has characterized the work-station business this summer. Apollo, Digital Equipment, and Sun Microsystems successively announced either lower-priced or higher-performing entries in their product families.

Responding to the introduction of the latest competing product—the Sun 4, a 10-million-instruction/second machine—Pampel says that Apollo has had a plan in place "for some time that will leapfrog them. We're strong in graphics, and there's more to graphics than mips," he maintains. "Screen management, windows, network management, and security have to be considered. We have an aggressive target at the high end of the line that you haven't seen yet." —*Lawrence Curran*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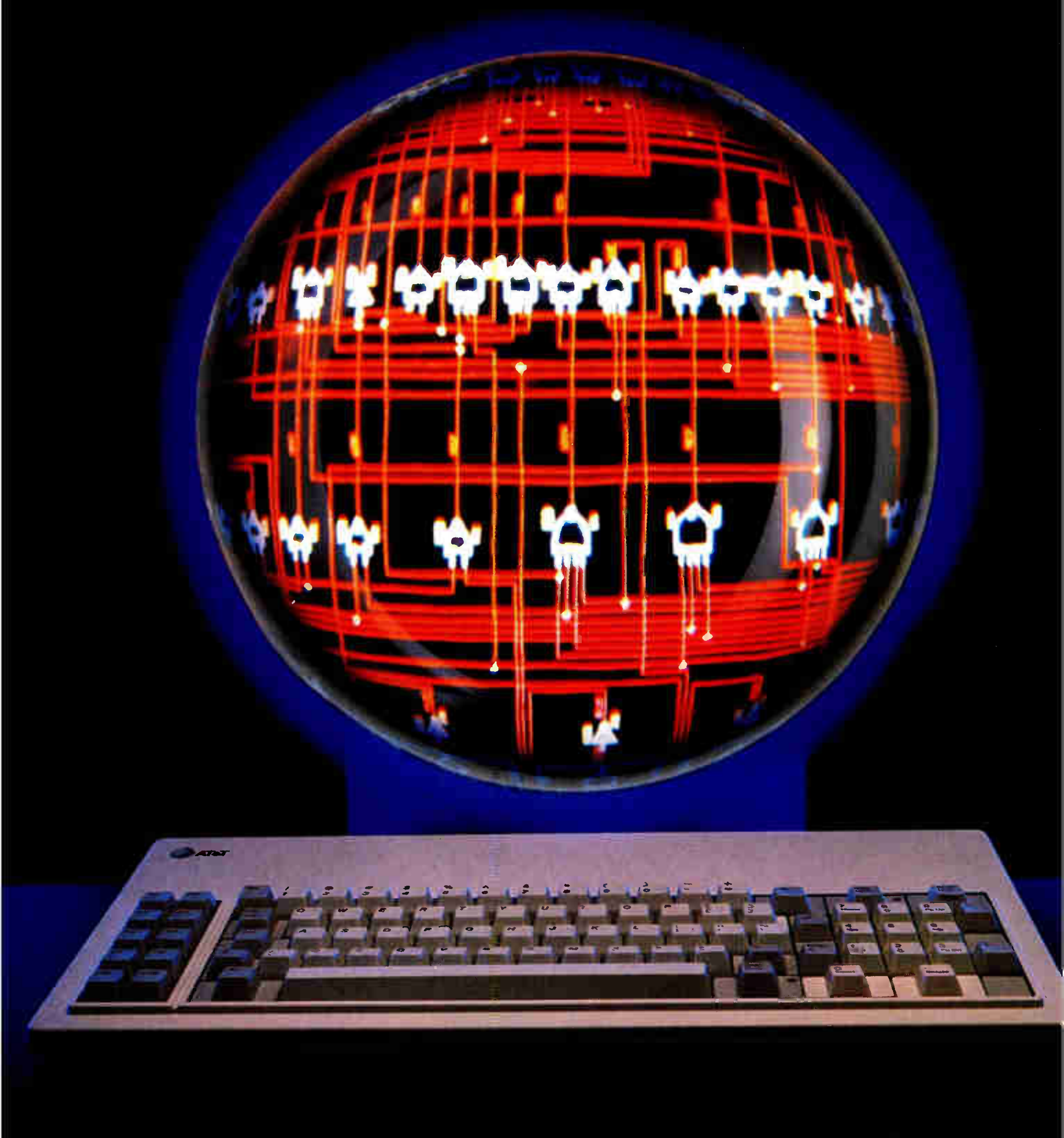

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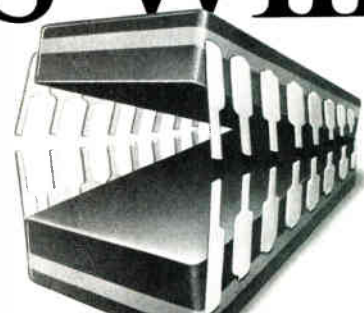

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ELECTRONICS NEWSLETTER

TANDY ATTACKS IBM AGAIN, WITH A LOW-COST, 80386-BASED PC

Tandy Corp., which became the nation's largest seller of IBM Personal Computer clones by sharply undercutting prices, is about to strike again. Four new PCs are debuting in August—the most extensive change to Tandy's product line since it entered the personal-computer market a decade ago. Hottest product is expected to be the Model 4000, based on the 16-MHz version of Intel's 32-bit 80386 microprocessor. It will sell for only $2,599 with 1 Mbyte of main memory, about $4,500 less than the comparable IBM Personal System/2 Model 80. The Model 4000 does not follow IBM's Micro Channel bus, but it does offer a 32-bit slot for up to 16 Mbytes of expansion memory, six 16-bit slots compatible with IBM's XT and AT cards, and two 8-bit slots. Like the PS/2, it uses 3½-in. disk drives. The Fort Worth company will also introduce a PC-compatible laptop priced at $1,599, an 80286-based unit selling for $1,199, and a consumer system, listed at $699. □

NETWORK SYSTEMS WILL MARRY ITS HYPERCHANNEL TO ETHERNET AND TCP/IP

In a sharp break from past policy, Network Systems Corp. will introduce in September the first in a series of products compatible with networking schemes other than its own Hyperchannel networking system. The Brooklyn Park, Minn., company has carved out a leading position in high-speed, 50-Mbit/s networking systems [*Electronics*, July 22, 1985, p. 36] by staunchly sticking to a proprietary product approach. But now, after spending more than $20 million on research and development over the last 18 months, it is creating a new line of open-systems products. First out will be a series of bridge offerings that will allow devices on separate Ethernet networks to communicate with one another over a Hyperchannel net, regardless of protocol. Also bowing in September is a family of router products to accommodate transmission of TCP/IP messages over a Hyperchannel. The company promises several more announcements later in the year. □

ROCKWELL'S FIVE-CHIP V.32 MODEM RUNS ON JUST 2 W

Rockwell International expects to upstage other modem makers at the late-September Tele-Communications Association Show in San Diego with a five-chip modem that meets the international CCITT V.32 standard for 9,600-bit/s full-duplex operation—the world's most advanced modem, according to Rockwell's Semiconductor Businesses president Gil Amelio. Instead of the usual 40 W that a V.32 modem consumes, Rockwell's hardware requires less than 2 W. Rockwell says the modem incorporates three new technologies, including an echo canceller on a single chip, an integrated 9,600-bits/s analog/digital converter, and a digital signal processor that can run at 6 million instructions/s. □

FIVE FIRMS RALLY BEHIND VXIBUS STANDARD FOR INSTRUMENTS ON A CARD

Instrument-on-a-card technology could take off now that five instrumentation heavyweights have endorsed the open architecture of a new standard—the 32-bit VXIbus, a version of VMEbus designed for instrumentation. Colorado Data Systems, Hewlett-Packard, Racal-Dana Instruments, Tektronix, and Wavetek have all cozied up to the standard, which can support up to 256 instruments at once. The VXIbus connector specification supports clock speeds of up to 100 MHz, and accommodates both ECL and TTL triggering. In addition, it supports four board sizes: two identical to VMEbus cards and two larger cards that match standard Eurocard sizes. VXIbus instrumentation can be controlled with an external computer using the IEEE-488 standard, which is the primary instrumentation bus worldwide. □

PRODUCTS NEWSLETTER

MONOLITHIC MEMORIES GOES TO CMOS FOR ITS PALs

The siren call of 75% power-consumption savings from using CMOS technology has ended Monolithic Memories Inc.'s policy of using only bipolar and emitter-coupled logic in its programmable-array-logic parts. The Santa Clara, Calif., inventor of PALs is going to CMOS with three erasable PAL families. The 24-pin PALC20R8Z zero-standby-power ZPAL family is a pin-compatible version of MMI's bipolar parts but offers a standby supply current of less than 10 μA typical and 100 μA maximum. Active power is only 3 mA/MHz up to 25 MHz. Available now in 35-ns and 45-ns versions, it costs $9.85 each in 100-unit quantities. The 20-pin PALC16R8Q family is equivalent to MMI's other 25-ns bipolar parts, but at 40 mA, dissipates 75% less power. It costs $5.50. MMI's PALC22V10H is the CMOS equivalent of a bipolar PAL device from Texas Instruments Inc. that has 10 input/output macrocells. It consumes 90 mA active—50% of the bipolar drain—and costs $11.60 each. □

STEREOGRAPHICS GIVES ANY MONITOR DISPLAY A TRUE 3-D LOOK

Liquid-crystal-shutter technology, polarized eyeglasses, and an advanced display controller combine to give a real three-dimensional appearance to monitor displays outfitted with StereoGraphics Corp.'s ZScreen. Although not the first to use the technology [*Electronics*, March 19, 1987, p. 107], the San Raphael, Calif., company's product has the advantage of working with any graphics monitor. Images are created by a controller that presents alternative left and right viewpoints to the monitor. Simultaneously, a liquid-crystal shutter called the LC modulator fitted over the screen circularly polarizes the two separate images in alternate directions, which means each polarized eyeglass lens "sees" only the left or right view. Available 60 days after order in 14- to 19-in. diagonal screen sizes, its prices start at $5,900. □

PAINT 13 MILLION PIXELS/S WITH METHEUS' $2,500 BOARD...

Two proprietary CMOS chips developed for high-end graphics controllers by Metheus Corp. have now been incorporated into standard VMEbus-format boards that draw random vectors at a rate of 13 million pixels/s. That's five times faster than Intel Corp.'s 82786 graphics processor, a popular benchmark product. The chips combine a 4-million-instruction/s general-purpose processor optimized for graphics with a control unit that handles raster memory and carries out low-level graphics tasks such as vector drawing, polygon filling, and pixel-block transfers. They are implemented in 8,000-gate CMOS gate arrays from Fujitsu Ltd. The Hillsboro, Ore., company's 1000VM-Series offers two resolutions—1,024 by 768 pixels, and 1,280 by 1,024 pixels. Each can have a pixel depth of 4 or 8 bits. Prices range from $2,495 for the 1,024-by-768-pixel system with 4 bits/pixel to $3,995 for the high-end 1,280-by-1,024-pixel system with 8 bits/pixel. All are available now. □

...OR GET 2 MILLION PIXELS/S FOR $1,500 FROM CONTROL SYSTEMS

A monochrome graphics controller board for IBM Corp. Personal Computers XT and AT provides switchable 1,660-by-1,280 or 1,280-by-1,660 resolution and drawing speeds 10 times faster than comparable boards, claims Control Systems Inc., St. Paul, Minn. Key to the Artist Publisher's speed is Texas Instruments Inc.'s TMS34010 graphics processor running at 50 MHz, which lets the board paint 2 million pixels/s. Other features include on-board support for Direct Graphics Interface Specification, an emerging hardware standard that saves users the trouble of writing software drivers for popular electronic-publishing packages. The board will be available in September for about $1,500 in 100-unit quantities. □

PRODUCTS NEWSLETTER

AUTOMATIX'S MAC II SYSTEM DELIVERS A $1,000 FACTORY-FLOOR SAVINGS

Add factory-floor management and process control to the list of applications for Apple Computer Corp.'s Macintosh II—and chalk up a $1,000 savings over the competition to boot. Automatix Inc.'s AI 90 industrial computer marries the Mac II to Texas Instruments Inc.'s NuBus to yield an open-architecture industrial 32-bit system that runs all Mac II software and provides optional support for Microsoft Corp.'s MS-DOS and AT&T Co.'s Unix operating systems. Automatix claims the AI 90 is the first Mac II system for the industrial market. The Billerica, Mass., company expects it to be used as a smart terminal on the shop floor, as a laboratory instrument controller, and for production monitoring and data acquisition. The system sells for $8,500, which Automatix says is about $1,000 less than the closest competitive industrial personal computer—a 16-bit system. The AI 90 is industrially packaged in a NEMA 2 enclosure, with EMI/RFI noise immunity, and is available now. □

APOLLO TO USE X WINDOWS TO LINK ITS STATIONS TO SUN, DEC, AND IBM UNITS

Applications developers won't be struggling as hard to tailor software interfaces among work stations built by more than one vendor, thanks to Apollo Computer Inc.'s Open Dialogue. Designed for creating common interfaces across all major Unix-based work stations, this software links Apollo units to Unix machines from Digital Equipment Corp., IBM Corp., and Sun Microsystems Inc.—and what's more, Apollo will support the software on its competitors' machines. Its versatility is derived from its incorporation of X Windows, the widely used public-domain windowing standard. Using a language similar to C, Open Dialogue creates interface programs that act as prototypes of applications. Versions can be created without rewriting the entire application. Copies cost $2,000 and will be available in early 1988 from the Chelmsford, Mass., company. Source code will cost $30,000. □

SWITCH TO STATIC RAMs BOOSTS CRAY-2 PERFORMANCE BY UP TO 40%

In a move to boost system performance by 25% to 40%, Cray Research Inc. is replacing the 256-Kbit dynamic random-access memory chips in most models of its Cray-2 line with faster 256-Kbit static RAMs. Compared with the 1.8-billion floating-point-operations/s peak performance of the DRAM-based Cray-2s, the new Cray-2S family will peak at 2.25 to 2.5 gigaflops. The improvement comes from a combination of the faster SRAMs—which have access times of 55 ns, compared with 120 ns for the old DRAMs—and reduced memory contention. The Cray-2S line will be available in the first quarter of 1988 in a four-processor model with 1 gigabyte of common memory, and in two-processor versions with either 1-gigabyte or 512-Mbyte memory. Prices will range from $12 million to $17.5 million. □

LAN WILL RUN 10 TIMES FASTER ON UNSHIELDED TWISTED-PAIR PHONE LINES

Look for SynOptics Communications Inc. to grab the lead in the local-area-network wars with an extension of its LattisNet product that will transmit 10 Mbits/s over unshielded twisted-pair telephone wire—that's 3 to 10 times better performance than the competition [*Electronics,* April 30, 1987, p. 26]. Part of the Mountain View, Calif., company's secret is to use fiber-optic cable for its backbone data lines, then run up to 350 ft. of the less-expensive twisted-pair medium from wiring closets to the nodes. It has already fielded a working, 10-Mbit/s shielded-pair version of LattisNet—an Ethernet implementation of a star topology. The unshielded-pair version is undergoing beta-site testing now and should be in production in the fall. Pricing is not available. □

E-R-X Emulators from ZAX: FOUR reasons why THREE letters make remarkable sense

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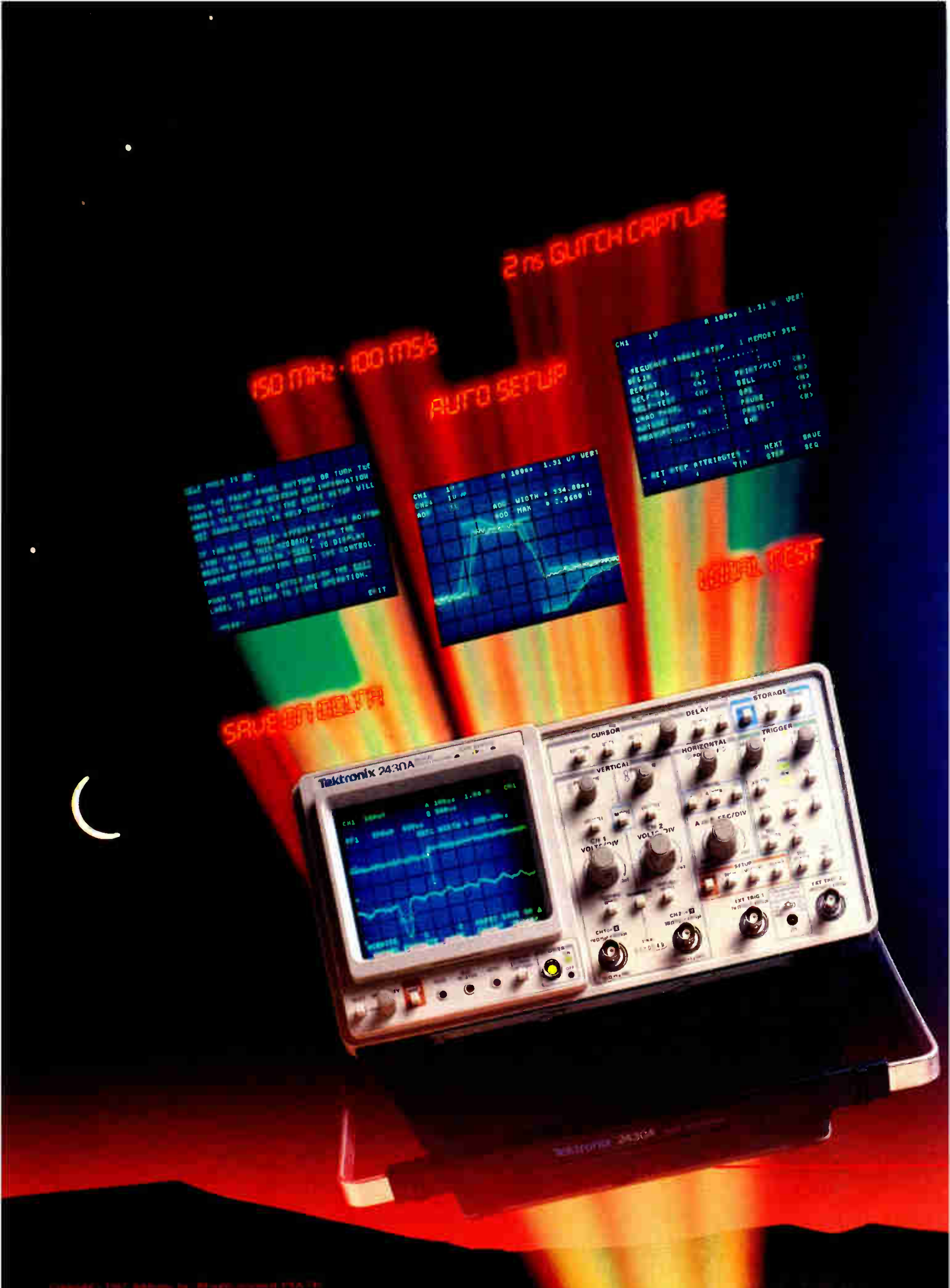
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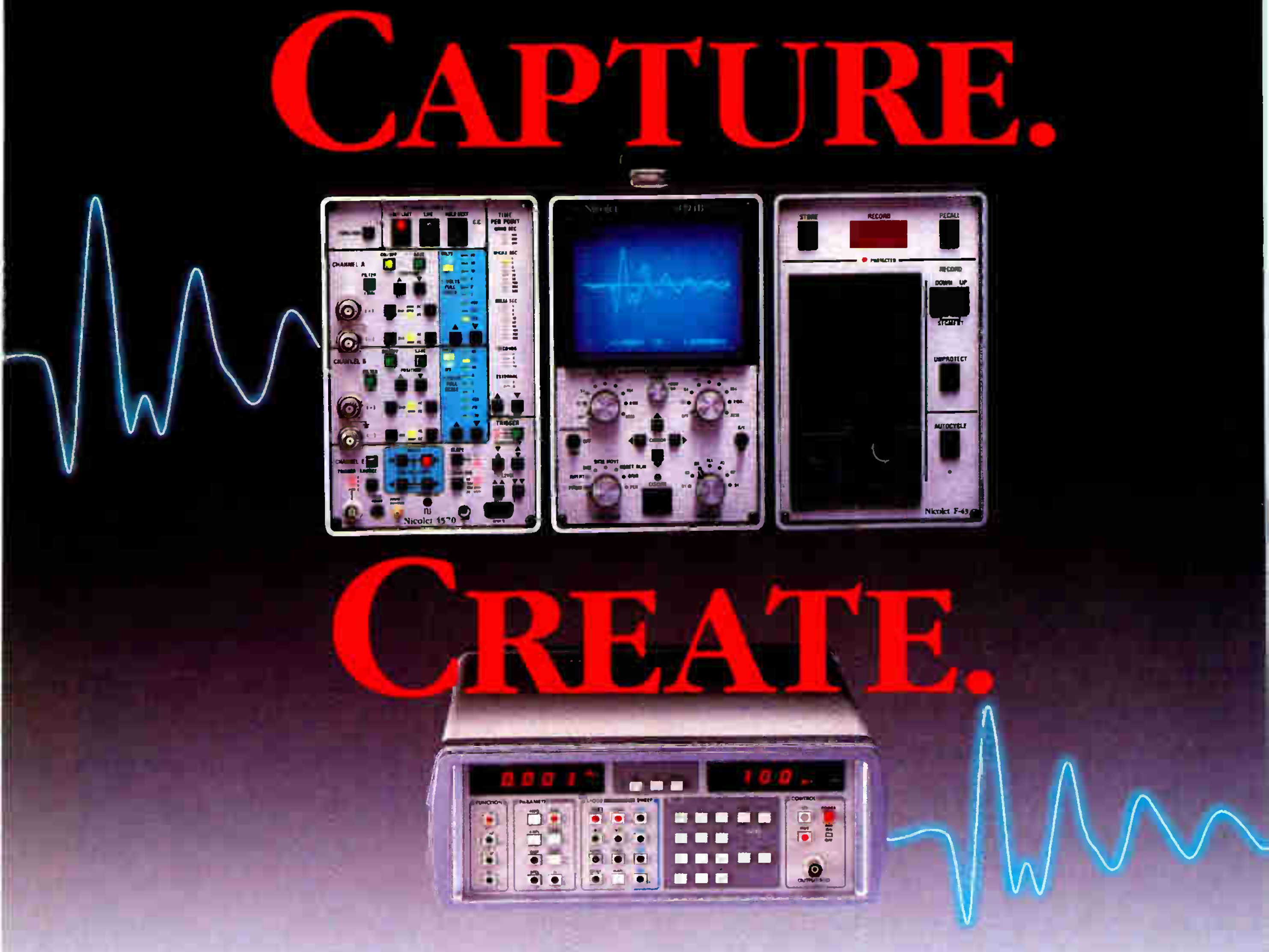

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Electronics

COMPUTER INDUSTRY SQUABBLES OVER NEW FORTRAN STANDARD

CAMPAIGN SEEKS TO STALL FORTRAN 8x, WHICH SOME THINK TOO COMPLEX

RICHARDSON, TEXAS

A decade-long effort to revamp Fortran programming standards for technical computing is turning into a major brawl as the software industry wrestles with proposals that would modernize the language.

Proponents of extensive additions to the aging Fortran 77 standard say new features are needed to broaden Fortran's scope and keep it in the mainstream of scientific and technical programming. Opponents feel that some ideas have been taken too far, standardizing unproven programming practices and creating essentially a new language that is unfamiliar to thousands of Fortran users, and potentially incompatible with the installed base of application code and too complex for low-end computers. After three decades of use, Fortran accounts for nearly 90% of technical and scientific code.

READY. A four-month public review of the Fortran 8x draft from the American National Standards Institute, expected this fall, has united Digital Equipment, IBM, and Unisys, among others, in opposition. But a majority of ANSI's X3J3 technical committee, including representatives from Cray, Control Data, Data General, and Hewlett-Packard, thinks 8x is now ready for public review.

One 8x opponent, minisupercomputer maker Convex Computer Corp., is preparing a "Fortran 8x Awareness Campaign" aimed at generating 2,000 letters from concerned users. Under ANSI bylaws, complaint letters must be individually answered in writing by X3J3. A flood of complaints could cause the panel to rewrite the draft proposal, says Presley Smith, development software manager at Convex. The Richardson, Texas, company hopes to get the 8x draft changed, but if it finds widespread support for 8x as it is, it will get in step and implement an 8x compiler.

The votes of ANSI's X3 management committee on whether to approve the public-review process will be counted in August; approval appears likely. The expected review of the draft will come seven years after the X3J3 body started work (see box, right).

The opposition to Fortran 8x frustrates X3J3 leaders. "Nothing is going away. Nothing will change from the programmer's viewpoint. There only will be more available to them," says Jerrold Wagener, vice chairman of ANSI's X3J3 committee. Wagener, the research director for the Amoco Production Co. in Tulsa, Okla., represents a large Fortran user. He labels most of the objections as "red herrings or scare tactics" by compiler suppliers who want to avoid the cost of reworking products.

Most objections center on additions to the language, which, opponents say, make the language too large and complex for its own good. Fortran 8x adds 33 statements to the current standard, bringing the total to 84, nearly double that of Ada. The major additions include array operations, numerical computation controls for programmer-specified precision, derived data types, and program module definitions.

Critics say the new features will inflate compilation time by as much as a factor of three. Proponents agree that Fortran 8x compilers will run more slowly, but expect higher hardware speeds to offset this problem. There is disagreement, however, over a more important performance issue: whether or not the new features will slow execution of the code generated by compilers.

Another source of stiff objections is the marking in 8x of 14 Fortran 77 statements as "decremented" features, recommending that they be considered for removal in the future. Wagener assures users that the more widely used decremented statements—like Common and Equivalence—will not be eligible for removal until 2010. Convex's Smith worries that the mere threat of losing statements could cause thousands of lines of code to be rewritten at high cost to users and at the risk of software errors. Wagener is sure this will not happen.

DEC executives object to the exclu-

THE LONG ROAD TO FORTRAN 8x

The drive to revamp Fortran started in 1979, the year after Fortran 77 (officially called X.3.9-1978) won final acceptance from the American National Standards Institute. At the time, the ANSI Fortran technical committee, X3J3, set its target as updating the standard within five years. It is coming under increasing pressure to get a new draft out for review, after a history of delays:

- **1979.** The X3J3 committee starts processing proposals for a new Fortran.
- **1981.** X3J3 adopts a proposal document known as S6.
- **1982.** Proposals in S6 are combined with existing Fortran 77 standard.
- **1983.** X3J3 approves S7, representing the combination of the proposals and Fortran 77.
- **Late 1983.** Complete rewrite of S7 document begins.
- **1985.** The rewrite, S8, wins X3J3 approval.
- **Early 1986.** Letter ballot for public review of S8 document fails: 20 against, 16 in favor, and 1 abstention.
- **Mid 1986.** X3J3 members reduce the size of proposed language, removing features in order to win enough votes to allow public review.
- **December 1986.** Letter ballot approves S8 draft 29 to 7.
- **May 1987.** Roll-call vote passes to forward S8 document for public review: 26 for and 9 against.
- **August 1987.** ANSI's X3 management committee is expected to approve public review of S8 draft.
- **Fall 1987.** A four-month public review period is expected to start with X3 committee approval. Depending upon the response from the Fortran community, the 8x draft could become an ANSI standard as early as next summer or delayed as much as three years, say X3J3 members.

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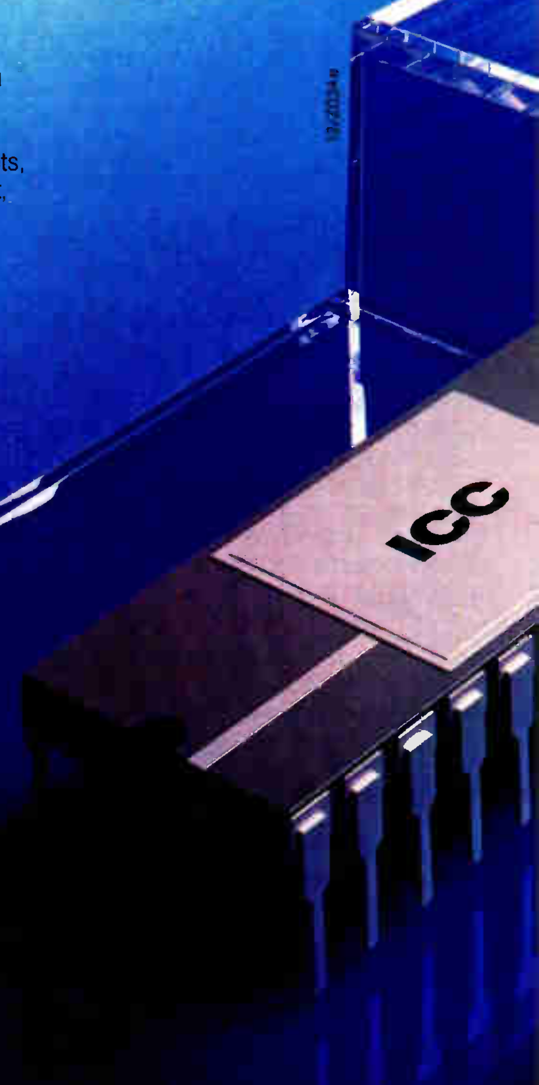

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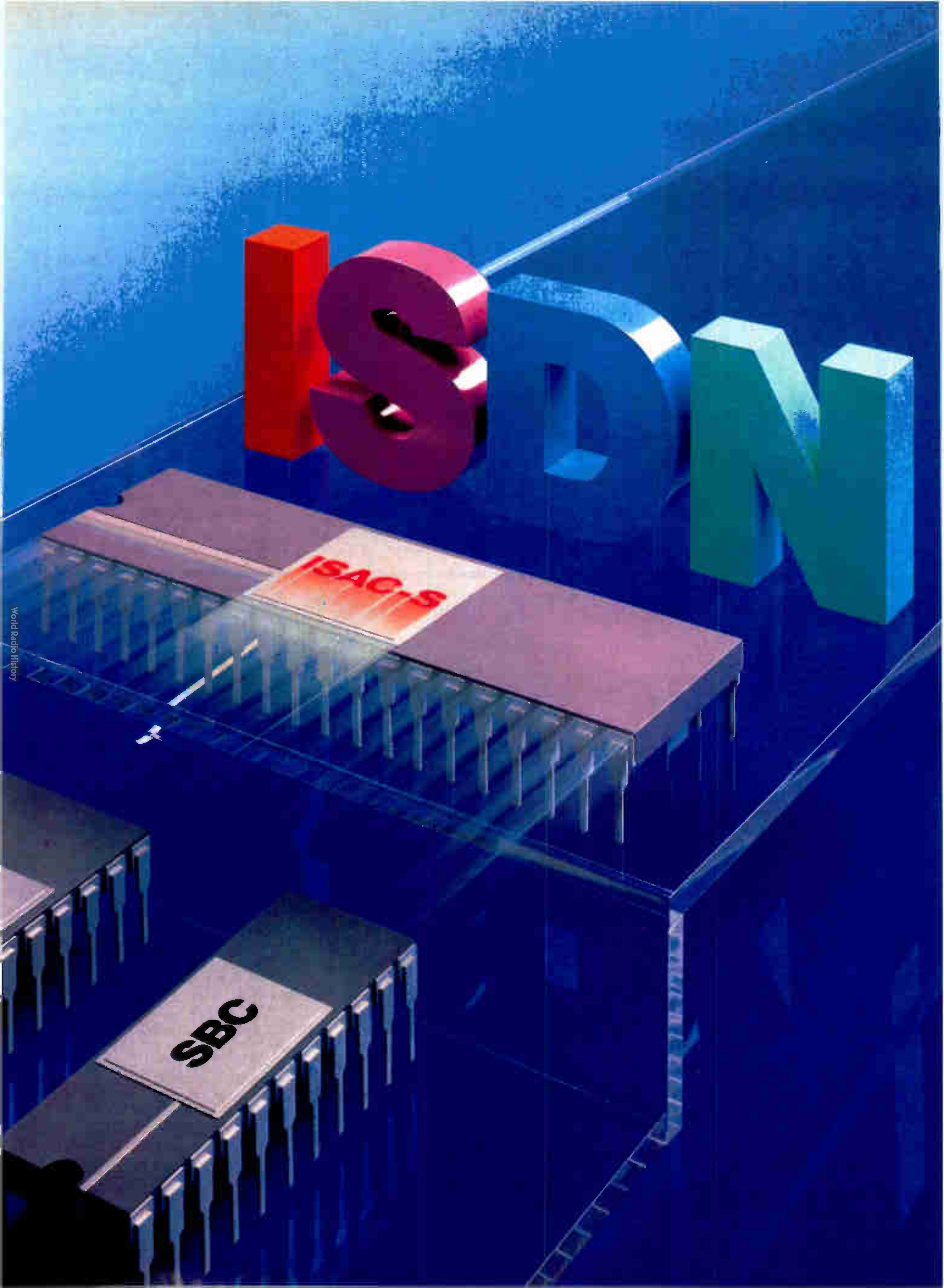
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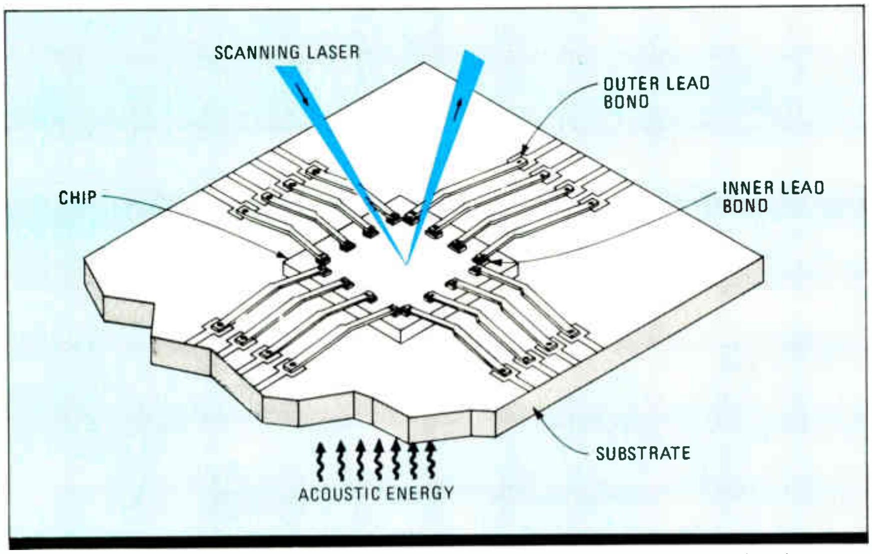

BAD BOND? By beaming acoustic energy onto the chip from below and scanning the upper surface with a laser, Sonoscan checks both through-the-bond and surface conditions.

with the TAB system," Traub says. He adds that a slew-scanning technique, in which an entire row of bonds would be scanned instead of stopping at each joint, could lead to a rate of several hundred joints per second. Eugene Blackburn, a RADC materials research engineer, says that Vanzetti's technique has proven it can immediately detect totally or poorly registered TAB lead bonds, or insufficient amounts of solder, without any problems.

Blackburn says that Vanzetti used the first contract phase to optimize its system. The company now will work closely with TAB bond suppliers to correlate the results obtained using the IR system to prove that the faults it identifies truly are defects.

Sonoscan uses a modified version of its System 2140 scanning laser-acoustic microscope in the work for RADC. Lawrence Kessler, Sonoscan president, says the first contract phase had Sonoscan modify the equipment—boosting the ultrasonic frequency from 100 MHz to 200 MHz, increasing the magnification from 70× to 140×, and adapting the system to accommodate the slide carrier required to transport the TAB ICs without damaging them.

Sonoscan's equipment produces visual images of the surface being inspected, as well as ultrasonic images of the solder-bond interface indicating good or bad bonds. Kessler says the next phase will focus on showing that the system and the new techniques can handle large numbers of inspections to differentiate good from bad bonds. *–Lawrence Curran*

TELECOMMUNICATIONS

COMING: IMAGE-TRANSMISSION STANDARDS

MUNICH

Worldwide standards for image representation and communication are in sight—they could be adopted internationally by late 1988 or early 1989—and they should open up promising new markets. Standards are what many firms, particularly companies with innovative designs on their drawing boards, have long been waiting for [*Electronics*, Feb. 19, 1987, p. 65].

Then new, global integrated-image communications services will begin to appear. With the standards, they will make possible applications like continuous gray-scale and multilevel color facsimile, quick access to facsimile data banks, digital photo telegraphy, and other services that take image data from a camera or scanner and process it for transmission to terminals or data bases.

For equipment vendors, worldwide standards and thus global markets will push sales in still other ways, mainly through economies of scale that will make equipment less expensive. This in turn will lead to a greater opening of markets such as newspaper publishing, printing, medical imaging, and facsimile data banks.

The standards being drawn up cover compression rates, storage capacities, and transmission times needed for various services, and specify compression algorithms and coding schemes. They are being worked out by a joint group of the International Standards Organization and the International Telegraph and Telephone Consultative Committee, which pushed them a big step closer to their final form at meetings in Copenhagen and Geneva that ended in early June.

Global standards should spawn many new markets

"If everything goes well, the ISO and CCITT will finish their technical work by January next year," says Istvan Sebestyen, an official of the CCITT image-standards subgroup. The proposals will then be put to a vote before the ISO for approval as an international standard. At the CCITT's plenary assembly in Melbourne late next year, that standard should wind up in the CCITT's recommendation T.80, to become effective by 1989.

Surprisingly, a large segment of the image-processing industry is unaware of the ongoing standardization efforts. Sebestyen says that many small companies, especially those that are not in the telecommunications business, "apparently have not heard of the CCITT and ISO work." Indeed, the roster of the working groups shows that members are primarily large network operators or are from big companies or national research institutes.

As Sebestyen and many CCITT and ISO experts see it, the standards will ring in a new era in communications that will take off steeply with the introduction of integrated services digital networks by the mid-1990s. Hungarian-born Sebestyen—he works in Siemens AG's Communication Terminals Division in Munich—believes that "without standards for new architectures in equipment for public use, tomorrow's image-communication services like gray-scale and color facsimile will not be possible."

Among other things, the targets for image compression and progressive picture buildup have been pretty well firmed up. For example, for continuous color images with an original 16 bits/pixel compression rate, the initial buildup calls for 0.125 to 0.25 bits/pixel. In successive stages, the pixel count rises to as high as 8 bits/pixel for an image identical with the original.

As for image compression and coding techniques, the ISO and CCITT members have submitted 10 methods, of U. S., European, and Japanese derivation. After evaluation, these techniques were divided into three groups.

The transform group, as it is called, is led by a European technique called the

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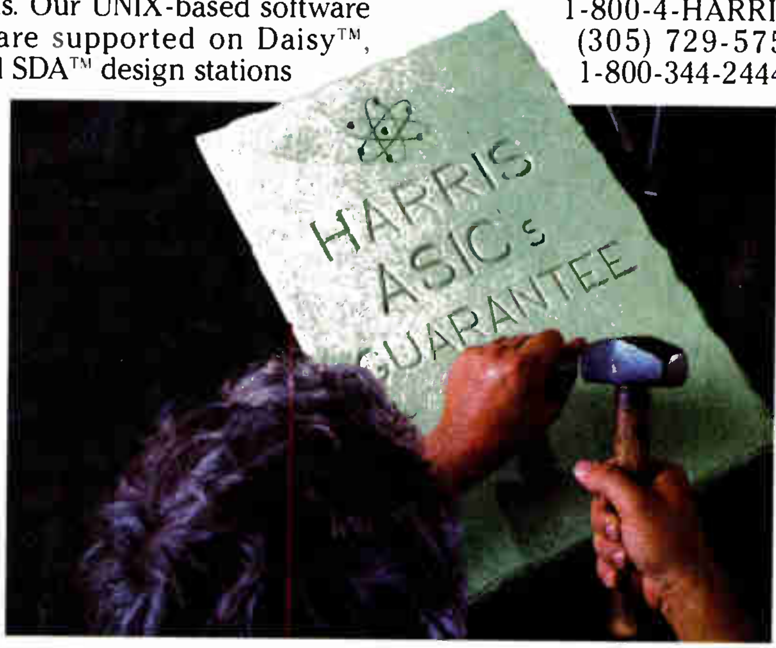

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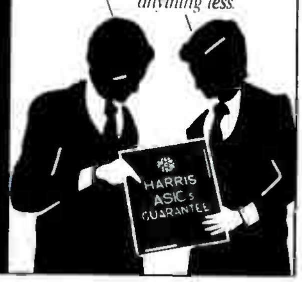

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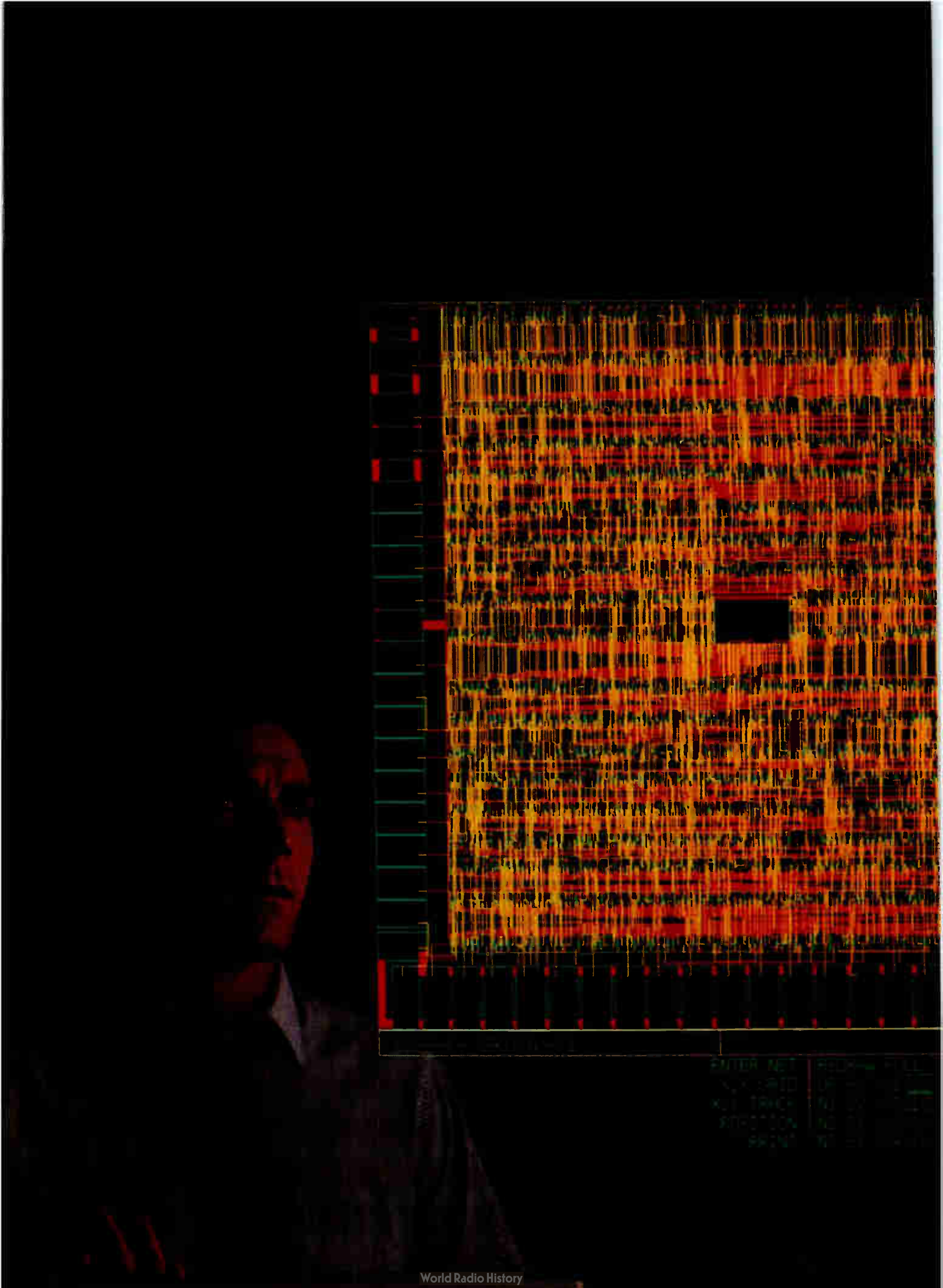

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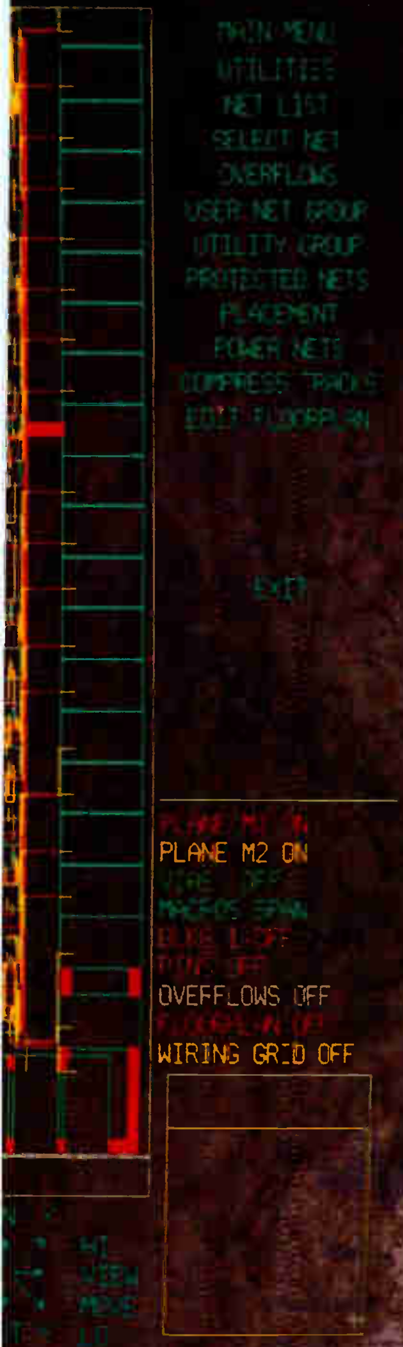

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Adaptive Discrete Cosine Transform. The predictive group is led by IBM Corp.'s contribution, a differential pulse-code-modulation scheme using Adaptive Binary Arithmetic Coding. Chief proposals from the joint Japanese natural-image standard group include techniques called the Progressive Coding Scheme and Generalized Block Truncation Coding. At the final test phase, each of the leading proposals may incorporate the best features from similar methods worked out in the three geographic regions. Current discussions within the joint CCITT/ISO group are aimed at an agreement on a single compression and coding method by January of next year. *–John Gosch*

MAGNETICS

PERKIN-ELMER GETS CLOSE TO NEW KIND OF DETECTOR

EDEN PRAIRIE, MINN.

Like a billiard ball caroming off a table cushion at an angle governed by its spin, low-energy electrons scatter back from an atomically clean gold target according to the direction of their magnetic spin orientation. Perkin-Elmer Corp.'s Physical Electronics Division aims to take advantage of that fact to build instruments that could point the way to higher bit density in magnetic computer storage and even to new types of magnetic microcomponents.

The Eden Prairie, Minn., division next year will introduce a new type of electron spin detector that will make practical the use of electron microscopy to study microminiature magnetic domain structures. The technique is called Sempa, for scanning electron microscopy with polarization analysis.

A somewhat similar method known as Mott analysis requires electrons to be accelerated to about 120,000 V. But Sempa is based on a 1982 discovery by researchers at the National Bureau of Standards that electron-spin polarization analysis can also be done at low voltages. Whereas Mott analyzers require bulky, somewhat hazardous, room-size equipment, a 150-V Sempa detector is about the size of a fist. This makes for easy attachment to a SEM system.

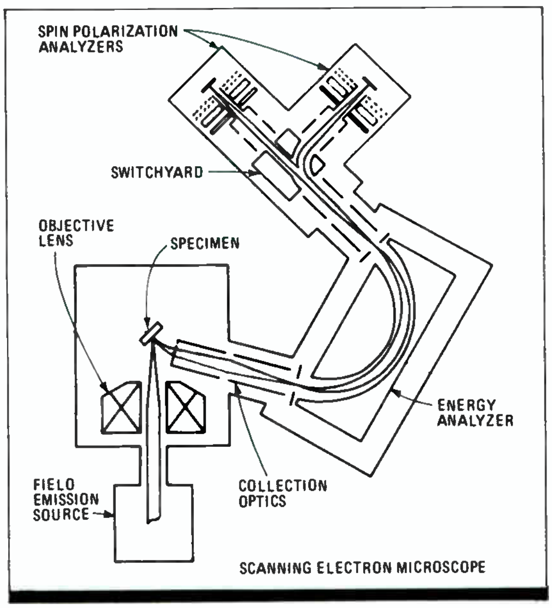
Resolution is theoretically limited only by the size of the incident electron-beam spot size. So Sempa may allow researchers to see details of tiny magnetic domain structures on thin-film recording heads or media, for example, as much as 100 times more clearly than with most common optical techniques.

As such, Sempa could prove a crucial research tool in the quest to achieve the extremely high bit densities envisioned for future-generation disk- and tape-drive systems, industry officials say. The method could likewise aid in developing submicron domain-based bubble-memory chips, new kinds of microparticulate-based magnets, and other tiny magnetically based devices.

The Sempa technique relies on the character of the low-energy (0 to 100 electron volts) secondary electrons that are emitted from the surface when a magnetic sample is bombarded by an incident e-beam. These electrons maintain the magnetic spin polarization that they had in the sample.

They are collected in the Sempa detector and directed against an amorphous gold target. They scatter back from this target at between 130° and 160°—depending on their spin orientation—against a four-quadrant gold detector anode. By measuring the difference in signals on each of the four quadrants, it is possible to determine the relative strength and direction of the sample magnetization.

Along with Perkin-Elmer, Control Data Corp. and Honeywell Inc. both see big potential in Sempa. The two firms, in fact, collaborated with Perkin-Elmer beginning



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in March 1986 to develop two prototype Sempa detectors based on the original NBS design.

Honeywell and Control Data each kicked in the equivalent of about $60,000. And they have been sharing time on one of the two prototypes, which Perkin-Elmer delivered to Honeywell last March, says Don Krahn, a principal development engineer at Honeywell's Solid State Electronics Division in Plymouth, Minn.

Since Sempa offers theoretical resolution down to 100 Å, it should prove a big advantage over current techniques for looking at magnetic domains. Commonly used optical techniques such as those based on the Kerr effect are wavelength-diffraction limited, with minimum resolution of about 1 μm, says

Pointing the way to new classes of magnetic components

Patrick Ryan, a Control Data engineer in Minneapolis. Ryan is using the Sempa prototype for work on an advanced magnetoresistive thin-film head that the company plans to introduce next year [*Electronics*, May 14, 1987, p. 31].

For its part, Perkin-Elmer has obtained exclusive worldwide marketing rights to the Sempa technology from the three NBS inventors. The firm plans to offer a commercial version by "late next year," says Rolf Olson, Auger product manager in Eden Prairie. The detector will be offered as an attachment to Perkin-Elmer's PHI 660 Scanning Auger Microprobe system, which is used for surface-layer chemical analysis. The system sells for about $520,000 in a typical configuration. Pricing for the Sempa attachment has not yet been set, but could come in at between $150,000 to $200,000 or higher, sources say.

Olson says it's too early to estimate the potential market for the Sempa detector. But he notes that "demand has been very high" for an analytical service Perkin-Elmer has been offering to firms wishing to experiment with the Sempa technique, using the other of the two prototypes. Among the companies that have used the service or are on the waiting list are Exxon, General Motors, Hewlett-Packard, IBM, Kodak, Polaroid, and Varian. "And we've got people pounding on our doors," Olson says.

As noted by Control Data's Ryan, "When you're in a competitive business like we are, whatever you can have that's going to give you more information, to give you that competitive edge, you want. And this technology is a front-runner." *–Wesley R. Iversen*

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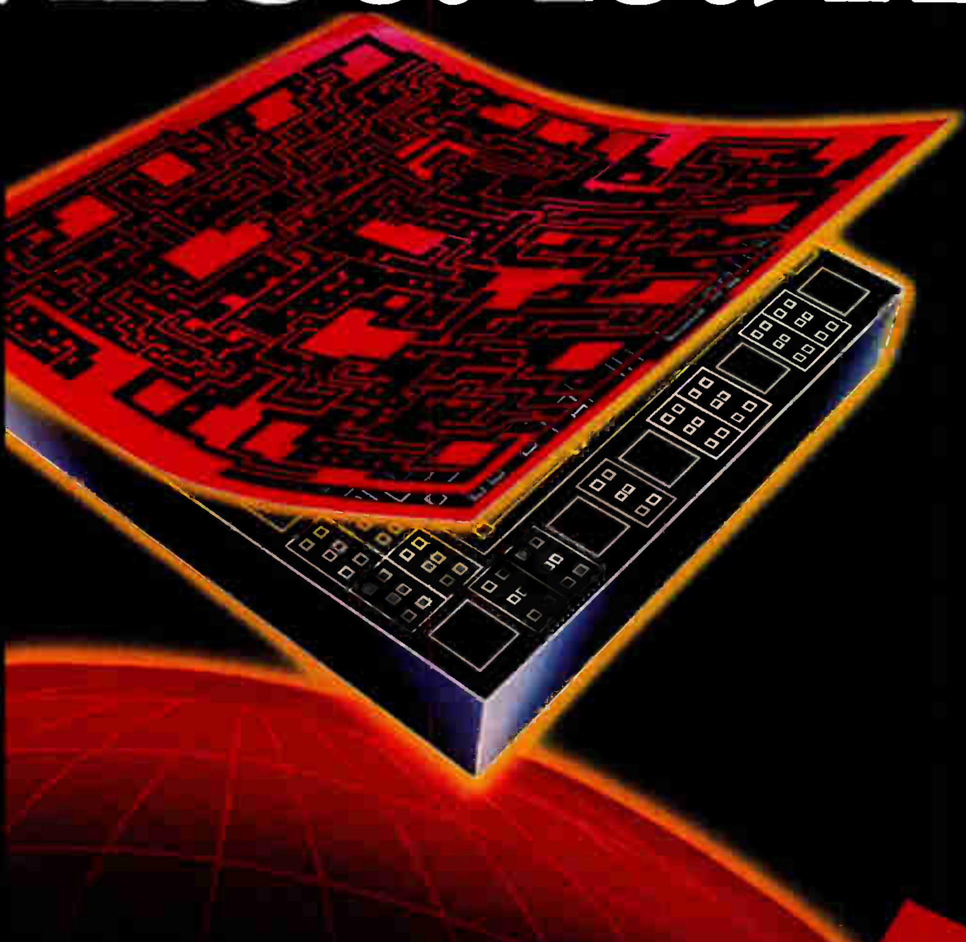

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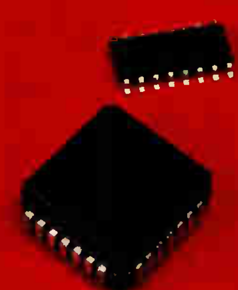

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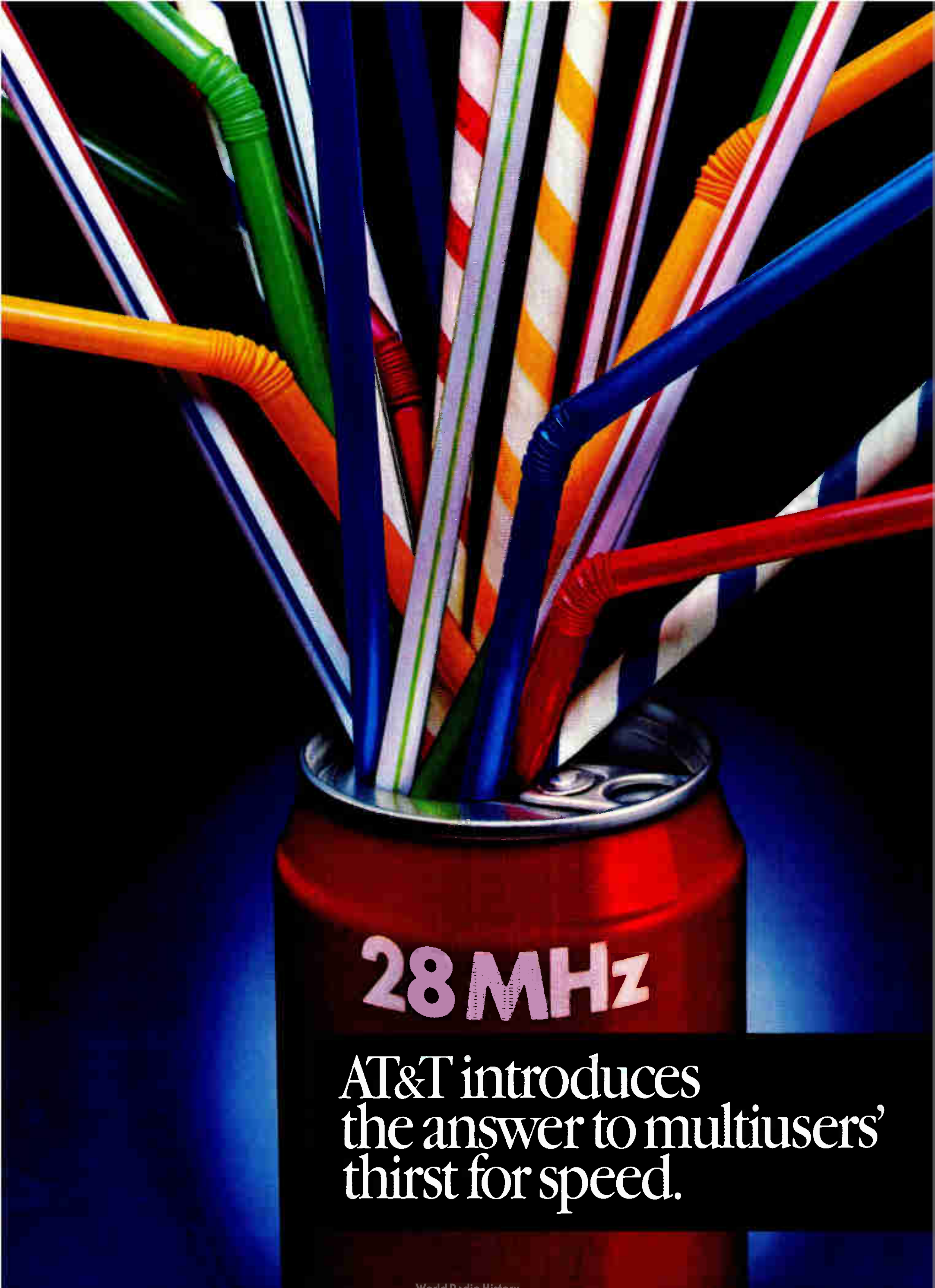
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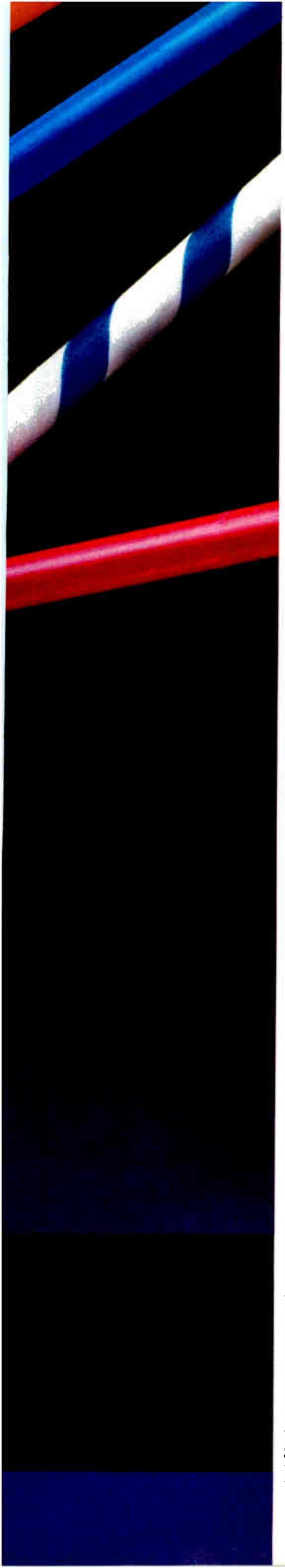

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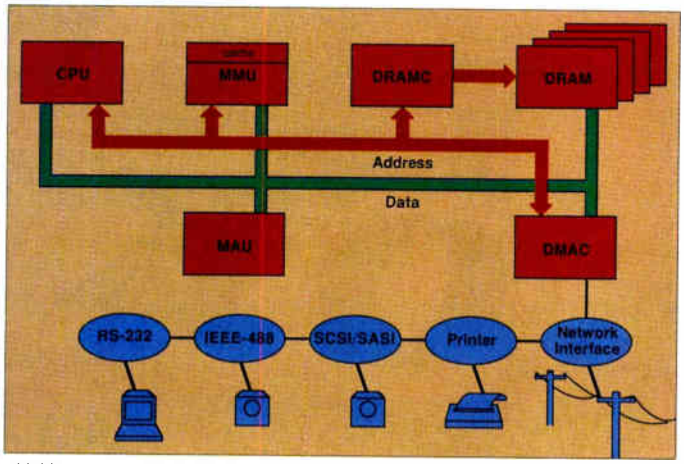

AT&T's newest system design offers a cache memory that runs at 20 to 30 MHz.

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INTERNATIONAL NEWSLETTER

MITSUBISHI WILL DOUBLE OUTPUT OF 1-Mbit DRAMs

Mitsubishi Electric Corp. will double its output of 1-Mbit dynamic random-access memories over the next six months to meet a burgeoning demand in domestic and overseas markets. As part of this expansion, the Tokyo-based firm will make a shrink version, with 100- and 120-ns access times, that measures about 80% less than the original 1-Mbit DRAM, which is 4.73 by 13.84 mm. Volume production will begin this fall at Mitsubishi's Saijo plant, with first samples set to ship late in July 1988 to Japanese customers. The company will begin assembling the shrink version in the U. S. in January at its Durham, N. C., plant. The Saijo facility, which is turning out 500,000 of the larger DRAMs a month, will increase output to 1 million of the shrink version by January. □

ARE FAR EASTERN COMPANIES DUMPING CD PLAYERS IN EUROPE?

The Commission of the European Communities is investigating charges that Japanese and South Korean makers of compact-disk players are selling them in Europe ,at below-market prices. An association of CD-player companies known as Compact says Far Eastern manufacturers are charging 30% to 60% less in Europe than for identical equipment in their native markets. In effect, Compact says, they are subsidizing exports, and that amounts to dumping. Far Eastern companies have dominated the European CD player market almost from the beginning, boosting their market share from 50% in 1984 to 75% by the end of last year. Total sales of CD players in the EC have risen 12-fold since 1984, and Far Eastern exports have shot up more than 16-fold in the same span—from 96,400 to almost 1.6 million units. □

INTEL TURNS TO MITSUBISHI TO HELP CRANK OUT ITS POPULAR EPROMS

Unable to meet the increasing demand for its 256-Kbit and 512-Kbit CMOS erasable programmable read-only memories, Intel Corp. is turning to Japan for help. Mitsubishi Electric Corp., of Tokyo, is now beginning to manufacture the Santa Clara, Calif., company's EPROMs because, according to insiders, Intel is doing all it can just to meet the demand for its 32-bit microprocessors. The company has no spare capacity to increase production of EPROMs. Mitsubishi is already producing parts with access times of 200 and 250 ns at its Kumamoto works, and worldwide distribution of the parts should begin soon under the Intel brand. Mitsubishi will not disclose the production rate for Intel's chips, but it is believed to be more than 200,000 units per month. The Kumamoto works is already producing Intel's 8-bit microcontroller, the 8051. □

PHILIPS CLAIMS IT'S FIRST TO BUILD TEST FUNCTION INTO STATIC RAM

Philips of the Netherlands says it is the first chip maker to implement a test mode on static random-access memories. Test modes have previously only been designed for dynamic RAMs. Philips says the test function will be implemented on the submicron 256-Kbit SRAM it is developing as part of the Mega Project [*Electronics,* July 23, 1987, p. 36], its joint development deal with West Germany's Siemens AG. The test mode can determine whether redundant circuits on the chip have been used. It can also be used while the part is in a system. Moreover, it bypasses peripheral circuitry to perform such checks as stress and hot-electron tests on the memory matrix. It can also be used on smart SRAMs to bypass unusual logic and perform electrical characterization. Early samples of the new part are expected by the end of the year, and Philips expects other memory makers to follow suit with similar parts in the next 12 months. □

INTERNATIONAL WEEK

BOOK-TO-BILL IN UK CHIPS SLIPS IN JUNE

Although the UK book-to-bill ratio slipped considerably in June, the Semiconductor Group of the Electronics Components Industry Federation, whose members account for about 75% of semiconductor sales in the UK, is not overly concerned. After the exceptional May figure of 1.35, the 1.06 provisional figure for June was no surprise. Orders remain at a high level, the federation reports, adding that there is "nothing in these figures to indicate that the upward trend seen so far this year is coming to an end."

SANYO AIMS TO SIGN WITH TI OR VITELIC

Sanyo Electric Corp., out to strike a deal with a U. S. chip maker, is negotiating with two companies: Texas Instruments Inc., Dallas, and Vitelic Corp., San Jose. The U. S. company with which Sanyo comes to terms will design bipolar chips, particularly for use in video cassette recorders; the Osaka company will manufacture and market them in Japan. Sanyo also intends to set up a joint venture between its future partner and its subsidiary, Sanyo VLSI Engineering Co., Gifu, to manufacture and market ICs.

SOFTWARE TIES IBM PC INTO NEC PC LAN

East will meet West in local-area networks, now that Custom Technology Corp., Tokyo, and Retix Corp., of Santa Monica, Calif., have developed Open Systems Interconnection software that can tie IBM Personal Computers into LANs for NEC Corp.'s PC-9801s, the best-selling Japanese personal computer. The pair expects to have its OSI software, the first such package for Japanese personal computers, on the market by October. It will come as a read-only memory incorporated into a network control board priced from 70,000 to 100,000 yen. Custom Technology plans to offer similar OSI software packages for other brands of personal computers—including IBM Japan, Fujitsu, and Hitachi—next year.

UK PLANS TO EXTEND ALVEY R&D 5 YEARS

Prospects are bright for a follow-on to the UK's Alvey program, a five-year, £350 million, information-technology research and development effort funded by the government and industry. At a mid-July Alvey conference, Kenneth Clarke, minister for Trade and Industry, said the government plans to continue funding collaborative programs and will respond to the IT86 committee's report as soon as possible. Set up by the information-technology industry, the committee wants a further five-year program and £425 million in government funding.

BRITISH CLAIM AI RECORD FROM JAPAN

British Aerospace plc believes it has jumped in front of the Japanese with its declarative language machine (DLM) by running the Prolog "Determinate Concatenate" benchmark at 620,000 logic inferences per second. This doubles the 280 klips reported by the Institute for New Generation Computer Technology (ICOT) in Japan for its equivalent fifth-generation hardware, the High-Speed Prolog Machine. The British machine was developed by the Naval and Electronics Systems Division in Bracknell, UK.

IN JAPAN, CANON TO SELL SIEMENS PBXs

Canon Inc. of Japan has signed a deal to buy 500 digital private-branch exchanges from Siemens AG to resell in the Japanese telecommunications market. The small- and medium-capacity equipment, for voice and data, will be delivered over the next three years. The Munich company is not the first foreign manufacturer to have its PBX gear sold in the 50-billion-yen market. Toshiba markets AT&T's PBX, Oki Electric handles Northern Telecom's, and Mitsubishi Electric and Omron Tateishi Electric sell Rolm units.

FRENCH PEDDLE HI-TECH IN JAPAN

Technology developed by the Centre National d'Etudes Spatiales, France's national aerospace research and development institute, is now on the market in Japan. Nippon Eurotec Corp., Tokyo, an electronic-products trading firm, has bought the rights to sell licenses for the technology from Novespace SA, Paris, and will start looking for customers in September. Novespace is a joint venture between eight major French banks, a government agency that commercializes research, and CNES. Novespace plans to peddle French technology in electronics, optics, new materials, machinery, and process control to high-technology firms in the European Community, the U. S., and Japan.

UK VIDEOTEX NOW ON TAP IN JAPAN

Japanese personal-computer users will soon be able to access Britain's Prestel videotex service via Venus-P, an international packet-switching service run by Kokusai Denshin Denwa Co., Tokyo. KDD has developed software that allows the best-selling NEC PC-9800 series to access the popular videotex services offered by British Telecommunications plc, using a standard modem or an acoustic coupler. Prestel offers more than 1,200 sources of information, including message services, banking, teleshopping, and weather reports, says KDD. The software will be marketed for 50,000 yen starting next month. KDD plans to develop similar software for the IBM PC AT and XT later.

W. GERMANY FUNDS SUPERCONDUCTORS

West Germany's Ministry for Research and Technology has earmarked 6.5 million DM for some 30 university groups to emphasize basic research in superconductivity at elevated temperatures. Previous government spending in this sector—23 million DM during the past five years—has led to the development of a superconductive generator, a prototype of which may be tried out in 1989 or 1990. The generator is expected to be used in a power plant in 1992.

HUNGARY, USSR SET IC JOINT VENTURE

Hungary's two major chip-making firms, MEV Microelectronics Co. and the Hungarian Telecommunication Cooperative, have joined with the Soviet foreign trade group Electrozagranpostavka to set up Intermos Microelectronics Ltd. Owned half by Hungary and half by the Soviets, the firm will first coordinate the chip-making facilities of its founders, but next year it will start building $100-million-plus production facilities in Hungary. MEV, HT, and Intermos will have an annual capacity of 180,000 150-mm wafers.

SUMITOMO, MIPS INK WORK-STATION DEAL

Mips Computer Systems Inc. has allied itself with Sumitomo Electric Industries Ltd., Osaka, in a bid to break into the Japanese work station market. Initially, the two will explore possibilities for Mips's line of computer systems and application servers in Japan, and Sumitomo will develop new compute servers based on the Sunnyvale, Calif., company's reduced-instruction-set technology.

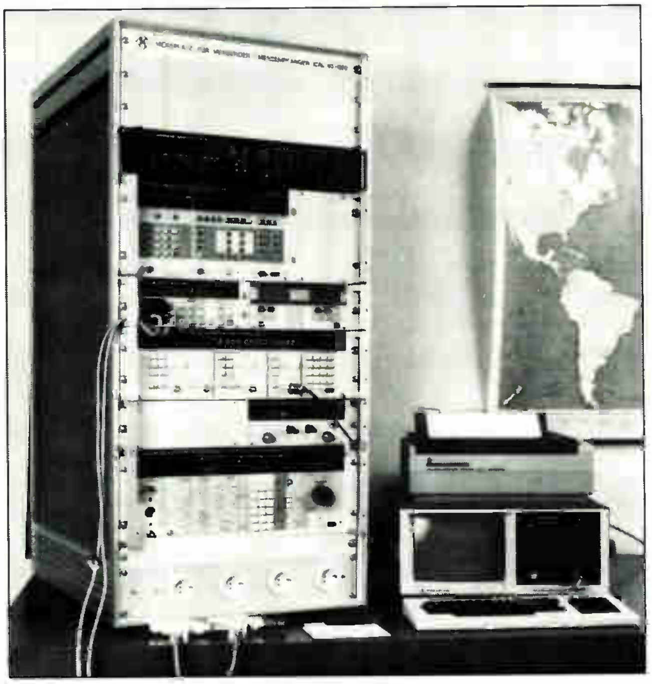
INTERNATIONAL PRODUCTS

CALIBRATION SOFTWARE CUTS INSTRUMENT DOWNTIME BY 80%

CHECKING OUT MULTIMETER IN 20 MINUTES WITH ROHDE & SCHWARZ'S TS9000

A computer-aided calibration system from Rohde & Schwarz can reduce instrument downtime for calibration by up to 80%. It does this by letting users calibrate several popular types of instruments on-site, instead of following the common practice of shipping them to calibration centers.

The TS9000 family consists of four sophisticated software packages, including applications libraries that can be tailored to work on specific calibration hardware. The software packages, which are designed to run on a 16-bit process controller from Rohde & Schwarz such as the PCA15 model, provide universally applicable calibration systems for instruments including multimeters, signal generators, power meters, and oscilloscopes.



WIDE RANGE. The TS9020 calibrates and adjusts signal generators and test receivers operating at audio through radio frequencies.

Calibration accuracy depends on the calibration hardware the user chooses—not Rohde & Schwarz's software packages—but it can easily equal the results of a calibration center. Since cost savings flow from reduced downtime, they differ from user to user. At a calibration center, however, the work is often done manually. Checking out a multimeter may take 4½ hours, compared with 20 to 30 minutes with the Rohde & Schwarz package.

The software is written in Pascal and Basic with some elements of C. It provides several ease-of-use features, including a graphics editor that tells users how the instrument to be calibrated must be interconnected with the calibration system.

FOUR PACKAGES. The TS9000 hardware-software packages include the TS9010 for multimeters; the TS9020 for signal generators and test receivers; the TS9030 for power meters and attenuators; and the TS9040 for oscilloscopes.

The technological underpinning of each package is software derived from expertise Rohde & Schwarz developed while operating its calibration center in Cologne, West Germany. The software can run on the PCA15 process controller [*Electronics*, May 14, 1987, p. 50L], which is based on Intel Corp.'s 80286 microprocessor.

Designed for controlling high-performance test and measurement systems, the PCA15 also incorporates an 80-bit Intel 80827 math coprocessor to speed up calculations and an Intel 80186 chip to handle input/output operations. In standard configuration, the PCA15 comes with 1 Mbyte of random-access memory. Other PCA models can also be used with the software.

On the software side, users can modify the basic applications libraries to build a system that works with calibration equipment supplied by any vendor, not only Rohde & Schwarz. The software also facilitates efficient operation with easy-to-use menus. Dialog is possible in four common languages: English, Spanish, French, and German. Users do not need to have a working knowledge of programming languages or of operating systems. The software automatically checks the dialog for plausibility to avoid erroneous inputs.

Graphics routines with easy-to-understand symbols display test setups on the screen, instructing the user on how to hook up the system to the instruments that are to be calibrated. Test reports and acceptance test forms are printed out for documenting measured results.

Basic operating data and control-parameter data for the system hardware are stored on a 1.2-Mbyte floppy disk or 20-Mbyte Winchester drive. It can be altered by the user or at Rohde & Schwarz after a test setup is modified. Test-item data, such as test parameters, test sequence, and specifications, can be recalled any time. This allows the user to create an equipment-specific library permitting fast system setup without dialog.

If a test routine or a test parameter must be modified, only the data record in question must be corrected. The TS9000 software thus dispenses with the time-consuming and costly generation of new program routines every time the setup is modified.

OPPORTUNITY. The advent of powerful process controllers and IEEE-bus systems opened the door for computation-intensive turnkey computer-aided calibration systems. Taking off from a low base, computer-aided calibration systems sales should rise steeply in the near term, "scoring annual growth rates up to 25% during the next half-decade," says Franz Dosch, head of test systems development at the West German company. Pushing the market are user demands for an on-site instrument calibration capability.

Any of the TS9000-family systems fits into a standard 19-in. rack. For users without an adequate pool of calibration instruments, Rohde & Schwarz will configure a system using its calibration devices. To build a TS9010 system for multimeters, for example, the company will provide a voltmeter, a digital multimeter, and a master calibrator.

Similarly, for the TS9020 system—for calibrating signal generators and test receivers—the firm will provide a signal generator, power-reflection meter, power meter, modulation analyzer, radio-frequency step attenuator, and test receiver.

The TS9020 is used for the calibration, adjustment, and service of signal generators and test receivers working in the audio frequency up to 2.5-GHz. A spectrum analyzer permits rf sources to be examined for spectral purity.

The TS9030 for power meters includes a signal generator, a test receiver, a power meter, a power reflection meter, an rf relay matrix, and an rf step attenuator. It handles precise measurements at frequencies up to 18 GHz. Attenuation measurements exceeding 100 dB are possible at frequencies up to 1.3 GHz.

The TS9040 for oscilloscopes includes a selective voltmeter and a frequency counter. It calibrates a scope's rise time, time base, input level, and bandwidth.

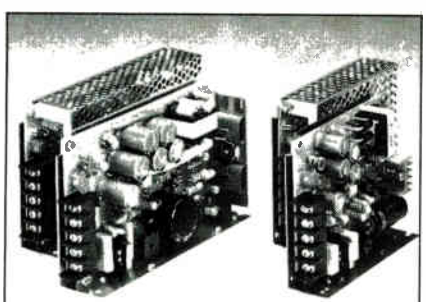
System costs depend on what hardware the user chooses to run the software packages on. The calibration program, though, is the same for all systems; it sells for 12,600 DM on the German market. The TS9010 multimeter library costs 8,400 DM. The TS9020 signal generator library is 11,200 DM, and the TS9030 power-meter and attenuator library costs 9,800 DM, as does the TS9040 oscilloscope library. The PCA15 process controller is priced at around 22,600 DM. *–John Gosch*

Rohde & Schwarz, Muehldorfstr. 15, D-8000 Munich 80, West Germany.
Phone 49-89-41292625 [Circle 500]

POWER UNITS BOAST 82% LOAD EFFICIENCY

The ERB-SA series of switching power supplies from ETA Electric Industry Ltd. features load efficiencies as high as 82% and an industry-standard mounting system.

The power supplies achieve their performance largely through the utilization of low-impedance electrolytic capacitors rated for 105°C. All five models conform to the Federal Communications Commission's Class B standard for electromagnetic emissions.



Model ERB05SA offers 75% load efficiency and is rated for a 5-V, 10-A output. Model ERB12SA, rated for 12 V and 4.2 A, has a load efficiency of 78%; model ERB15SA, at 15 V and 3.4 A, 79%; model ERB24SA, at 24 V and 2.1 A, 82%; model ERB48SA, at 48 V and 1 A, 82%.

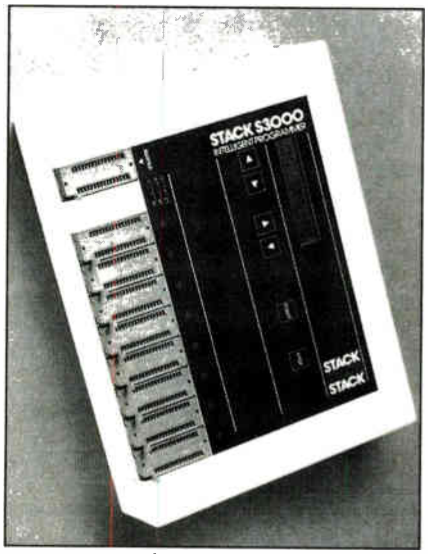
All five models are available now. Prices range from 2,900 to 5,800 yen.

ETA Electric Industry Ltd., 4-8-13 Kitashinagawa, Shinagawa-ku, Tokyo, Japan.
Phone 81-3-443-5201 [Circle 701]

GANG-PROGRAMMING EIGHT 1-MBIT EPROMS

The S3000 erasable programmable read-only memory programmer from Stack Ltd. can gang-program up to eight 1-Mbit devices based on 8-, 16-, 32-, or 64-bit data words.

On a production line, the 32-pin S3000 can be used as a stand-alone unit or linked to two slave programmers to process up to 24 devices at a time. Processing is controlled though an interactive 40-character light-emitting-diode display.



The completion of each programming operation is confirmed by an audible tone. With the addition of adapters, a wide range of microprocessors with on-chip EPROMs can be programmed.

Available now, the S3000 costs £1,000.

Stack Ltd., Unit 8, Wedgewood Rd., Bicester, Oxfordshire OX6 7UL, UK.
Phone 44-8692-40404 [Circle 702]

1-IN. COLOR CRT AIMED AT MILITARY USE

A 1-in.-diameter color CRT from the Electron Tube Division of Thomson-CFS achieves a line brightness of 10,000 candelas/m^2 and 35-μm line widths through the use of a high-voltage electrostatic focus gun and fine-grain phosphors.

Aimed primarily at military applications, such as helmet-mounted displays, the CRT has a limiting center resolution under night-vision TV-scan conditions of 900 (red) and 1,300 (green) pixels with 150 candelas/m^2 brightness.

The rugged tube assembly is 100 mm long and is 26 mm in diameter, including metal shielding, deflection yokes, and socket and high-voltage leads.

Prototypes are available now for an export price of $4,100 each. Production models will be available in September for $3,200 each in 50-unit purchases.

Thomson-CFS, Electron Tube Division, 38 rue Vautheir, BP 305, 92102 Boulogne-Billancourt Cedex, France.
Phone 33-46-04-81-75 [Circle 703]

STEPPER-MOTOR DRIVE HAS POWER SUPPLY

The PK2 packaged drive system for single-axis stepper-motor control from PKS-Digiplan Ltd. comes complete and ready to use with an integral power supply, I/O connectors, and control switches in a rugged metal extrusion.

The drive delivers a maximum output current of 2 A. Current can be selected with a DIP switch to match the drive to a wide variety of low-to-medium-power stepper motors.

Motor clock pulses supplied by an internal ramped oscillator cover speeds from 40 to 10,000 steps/s in two ranges. Maximum stepping rates are 10 KHz for full-step operation or 20 KHz in the half-step mode.

Available now, the K2 drive costs £98.

PKS Digiplan Ltd., 21 Balena Close, Creekmoor, Poole BH17 7DX, UK.
Phone 44-202-690-911 [Circle 705]

MULTIMETER INCLUDES TEMPERATURE MODE

The 6031 integrating digital multimeter from Prema GmbH handles seven different functions, including temperature measurements from –200°C to +850°C.

The 6½-digit instrument achieves its performance through a multiple-ramp analog-to-digital conversion technique and by integrating all the functions on a single chip.

The 6031 multimeter also offers automatic null-point correction, effective-value measurements, and an IEEE-488 bus interface. The instrument's integration times are selectable from 20 ms to 20 s;

resolutions are as good as 100 nV and 10 μA, and 100 μΩ.

The base accuracy for dc voltage and for resistance is 0.003% over one year and better than 0.001% over 24 hours. Available now, the 6031 sells for about 6,000 DM.

Prema GmbH, Robert-Koch-str. 10, D-6500, Mainz 42, West Germany.
Phone 49-6131-50620 [Circle 704]

LED LAMP LASTS 10 TIMES LONGER

By implementing an indicator lamp in four long-life LEDs instead of conventional LED lamps, MAF's Division Appareillage Electrique has achieved a tenfold increase in lamp life.

Besides lasting more than 30,000 hours, the C-22 simplifies maintenance and trims operating costs because it can be changed without turning off system power.

The light operates on 48 V dc or 125 V ac and is available in red or green. It fits into a standard 22.5-mm drill hole and requires a depth of only 56 mm. Its operating temperature range is –25°C to +40°C.

The C-22 is available now. Price depends on importing country.

MAF, Division Appareillage Electrique, Chimilin 38490, Les Abrets, France.
Phone 33-76-32-07-33 [Circle 706]

NETWORK DEVICE LETS PCs SHARE PORTS

The Adamux PC model LN-208 address-bidding communications controller from Adacom Communications Ltd. saves hardware costs in designing links between IBM Corp.'s 3270 mainframe and personal-computer networks by eliminating the need for installing a separate controller port for each PC.

Equipped with the Adamux PC, up to eight personal computers can share a single port of the 3270 mainframe. This leaves ports free for peripheral devices and also saves on coaxial-cable costs. The Adamux PC can be connected to the mainframe or used as part of a local-area network.

The address-bidding device distributes controller ports to the PCs according to three user-definable priority levels. If all available ports are busy, the PCs are queued according to the priority status set by the user. A password security feature is also available.

The Adamux PC measures 24 cm by 22 cm and weighs 1.6 kg. Available now, it costs £1,380.

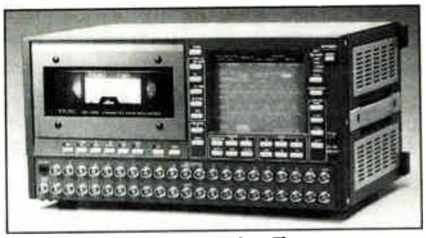
Adacom Communications Ltd., Laser House, 408 Peartree St., London EC1V 3SB, UK.
Phone 44-1252-5191 [Circle 707]

CASSETTE RECORDER SHOWS 2 WAVEFORMS

A VHS-format video-cassette data recorder from TEAC Corp. gives users interactive control of two waveforms simultaneously displayed on an electroluminescent screen.

Operators can instantaneously change the XR-7000's recording parameters, including I/O range, I/O zero shift, and automatic zero settings. Calibration, self-testing, and timer control can also be set from menus on the display screen.

The XR-7000 also offers seven tape speeds, ranging from 1.19 to 76.3 cm/s, and 21 input channels—each recorded



on its own tape track. Frequency response is dc to 150 KHz, depending on the operating band.

The unit is 36% smaller and 25% lighter than its predecessor, the XR-710. It measures 440 by 220 by 300 mm and weighs 19.5 kg, making it convenient for field as well as laboratory use.

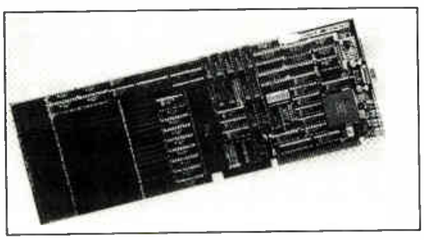
A 14-channel unit, the XR-5000, is also available. Shipments will begin in October. Price will depend on the importing country.

TEAC Corp., 3-7-3 Naka-cho, Musashino, Tokyo 180, Japan.
Phone 81-422-53-1111 [Circle 708]

BOARD DRAWS UP TO 2 MILLION PIXELS/S

Real World Graphics Ltd.'s AT 2500 graphics board for IBM Corp. Personal Computer ATs and compatibles boasts a drawing speed of 2 million pixels/s and supports resolutions of 1,280 by 1,024 pixels.

Targeted at computer-aided-design applications, the AT 2500 also offers 256 on-screen colors from a palette of 16



million colors, 2 Mbytes of memory, and advanced video-RAM processing. The main image is eight planes deep, with two additional planes for masking and menus.

The AT 2500 is available now. Single units cost £2,595, and original-equipment-manufacturer discounts are available.

Real World Graphics Ltd., 5 Bluecoats Ave., Hertford, Herts. SG14 1RB, UK.
Phone 44-9925-54442 [Circle 709]

MONITOR DETECTS 500-mV GLITCHES

The S2862 power-supply-monitor IC from Siltronics Ltd. is sensitive enough to detect glitches that can cause data errors in computer systems. It can monitor up to three power supplies.

The IC contains three window comparators, a precision voltage reference, a latch-and-hold comparator, and four output drivers. It detects both positive- and negative-going transients and can monitor both positive and negative supplies.

The internal voltage reference is accurate to 1%, and the overall device is accurate to 1.25%. Minimum glitch width is typically 100 ns for 500-mV overdrive and 400 ns for 100-mV overdrive.

Available now in 16-pin dual in-line or Small Outline packages, the S2862 costs U. S. $3.20 each in 1,000 units for either package type.

Siltronics Ltd., 436 Hazeldean Rd., Kanata, Ontario K2L 1T9, Canada.
Phone (613) 836-5003 [Circle 710]

RECORDER FEATURES PRETRIGGER STORAGE

Enertec Instruments' model 8200 digital two-channel chart recorder offers two advantages over analog instruments: pretrigger data storage and a direct means of processing data with a digital computer. The pretriggering capability lets users see the causes of an event instead of just the results.

The digitized signals have an 11-bit resolution—10 times more accurate than an 8-bit instrument. Input and recording parameters are programmable via RS-232-C and IEEE-488 interfaces.

The instrument measures voltage, temperature, and transients. A single input stage handles both voltage and temperature inputs, and in the temperature mode it is compatible with most standard thermocouplers.

Opto-isolators protect the input stage against voltages as high as 500 V. The recorder uses 250-mm-wide plain paper and color felt-tipped or ballpoint pens.

The 8200 is available now. Price depends on importing country.

Enertec Instruments, 5, rue Daguerre, 42030 Saint-Etienne Cedex 2, France.
Phone 33-77-25-22-64 [Circle 712]

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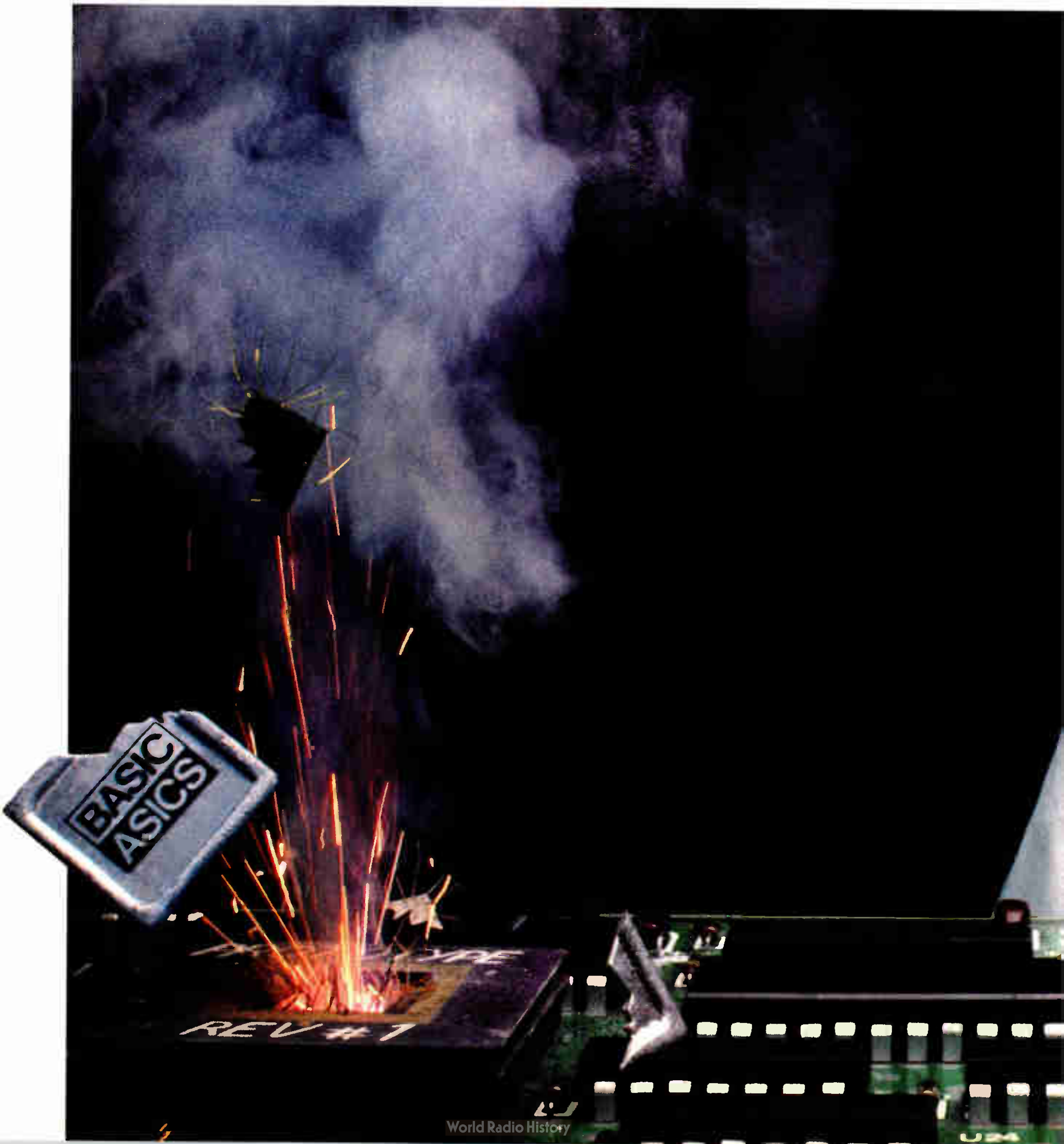

You see, we've been refining our design tools for the past fifteen years. And because they verify your input to worst case specs, as well as scrutinize every detail from spike analysis to bus contention, all the guesswork is eliminated. Our simulations are closely correlated to silicon (with a 99% hit rate). Plus, all prototypes and wafers are tested exactly like production units. So you know what you'll get. Before you get it.

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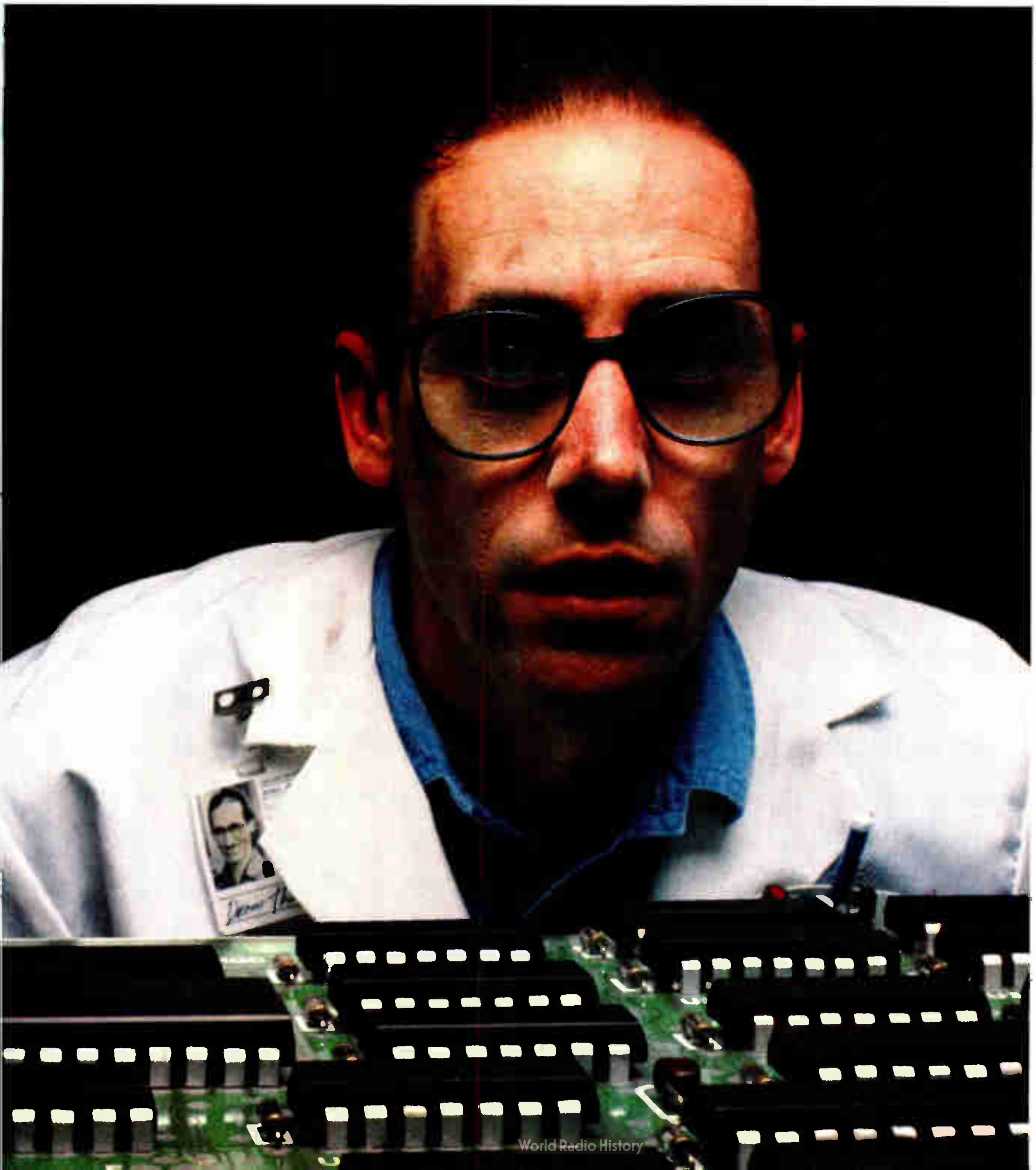

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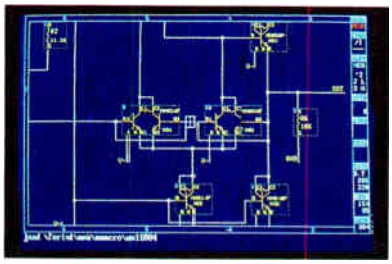

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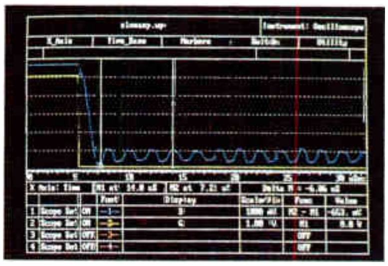

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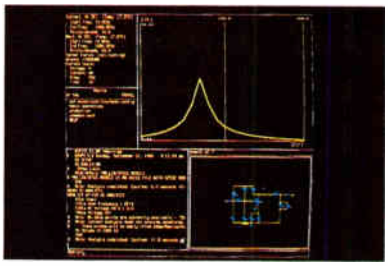

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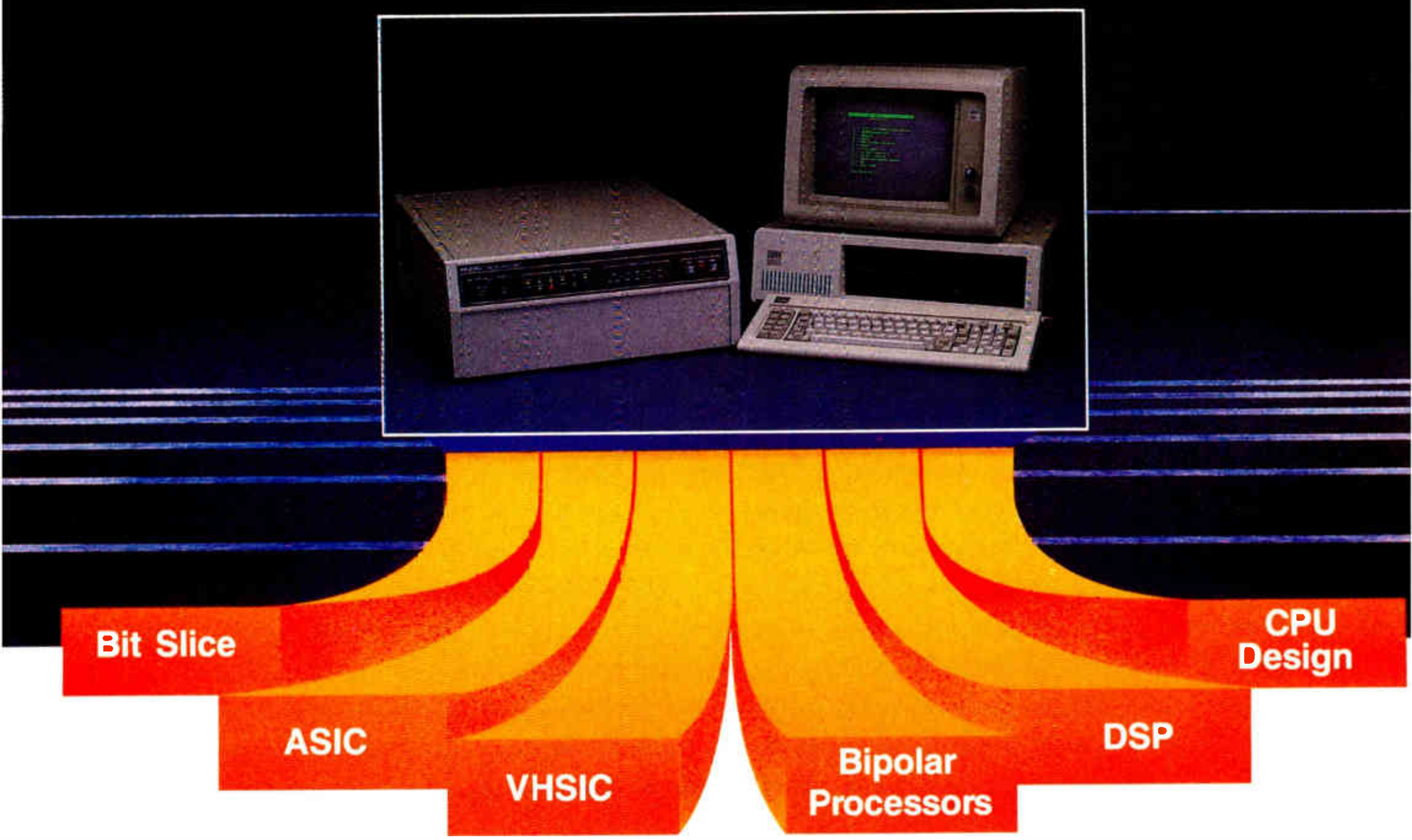

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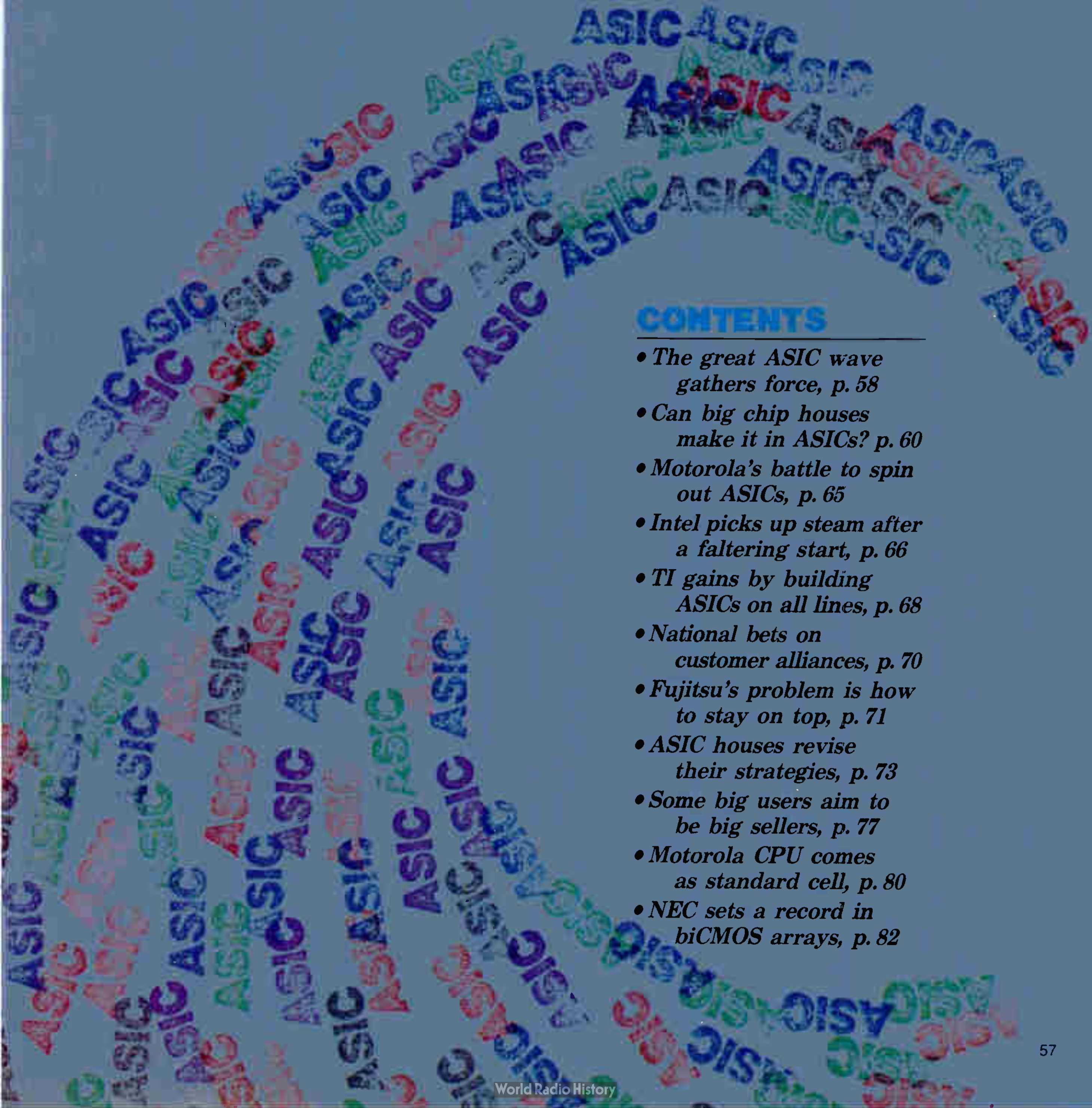
SPECIAL ISSUE

THE ASIC TAKEOVER: IT'S COMING FASTER



CONTENTS

THE GREAT ASIC WAVE GATHERS FORCE

The takeover is coming faster; big chip makers go all out to establish themselves, and semicustom houses try to hold on to what they've got

by Stan Runyon

Application-specific integrated circuits are a tidal wave about to break over the semiconductor industry. In fact, the takeover is coming faster now than most people had expected. ASICs are selling so fast that within three or four years they should constitute more than half of the $15 billion worldwide logic market. Because of this acceleration, the big semiconductor houses are going all out to establish themselves in the surging market. At the same time, the semicustom houses that pioneered this market are looking hard for ways to hold on to what they've got.

Along with this accelerating growth is rapidly broadening ASIC usage. A spreading universe of customers is expected to fuel exploding sales. Dataquest Inc., for example, predicts that in four years ASIC sales will nearly quadruple (see figure). Today, most ASICs are gate arrays sold in vast quantities to a small number of customers, notably computer makers. The new users are equipment makers capitalizing on the advantages of ASICs to build unique performance features into their products and to get to market faster. The number of worldwide ASIC design starts will zoom up dramatically from 6,000 in 1985 to 90,000 in 1990, predicts Technical Insights Inc., an Englewood, N. J., technical publishing house. That total includes design starts from both the systems and equipment suppliers as well as the semiconductor houses.

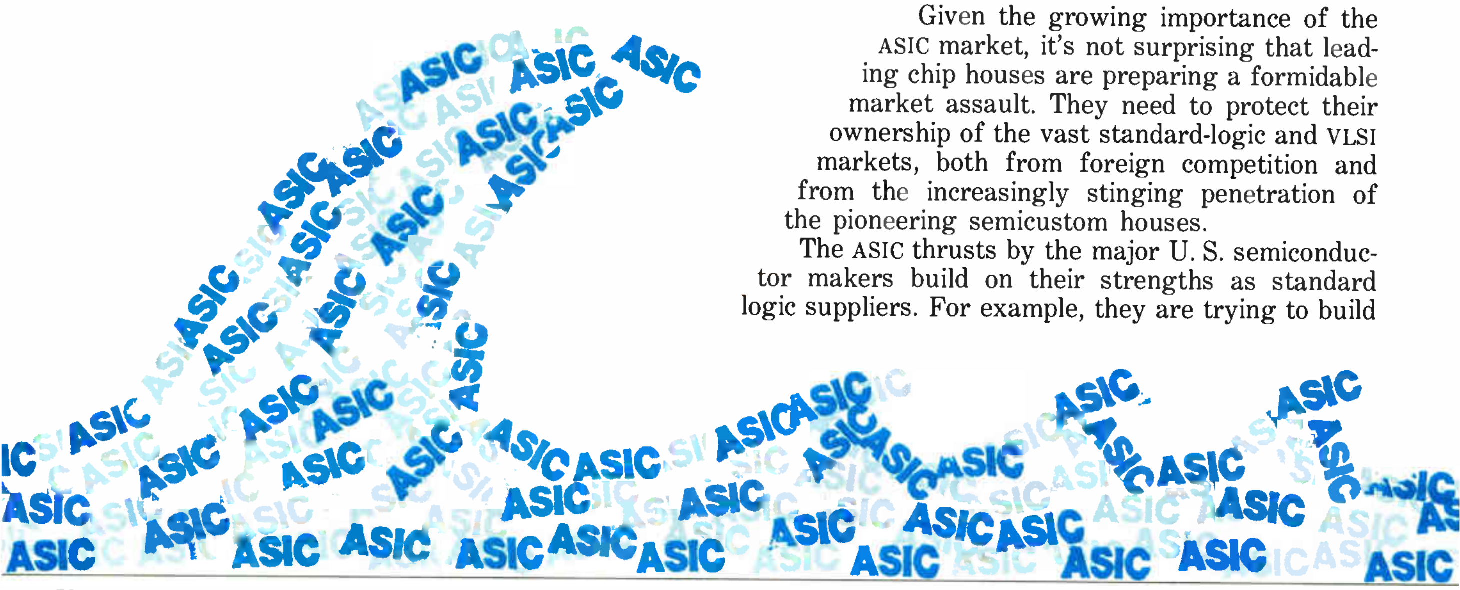
Equipment suppliers are turning to ASICs even faster than expected because they find themselves in an increasingly competitive situation. Product life cycles keep shrinking, spurring the need for ever more rapid product turnaround. The availability of improved computer-aided engineering tools—fast, powerful computers along with impressive applications software—means that equipment designers need no longer wait for standard ICs. They not only can do it themselves, but they can also do a better job of differentiating their products from the competition. All this leads to accelerating equipment obsolescence, heating up product development even more.

The ASIC market itself is changing, too, making it that much trickier for users, chip makers, and semicustom houses alike to figure out what to do next. Top industry executives point out that the dominant ASIC market segment, gate arrays, is maturing and price-cutting is rampant—just as the next wave of ASICs is coming to market. Standard-cell-based designs are assuming new importance, and their growth rate will soon outstrip arrays.

For that matter, it's pretty hard to figure out what is and is not an ASIC, much less how to make, sell, or buy them. By the most common definition, "ASIC" means only gate arrays or standard-cell parts. But a fair number of people expand the definition to include programmable logic devices in the ASIC camp. Others argue strongly that the PLD is not an ASIC, because, by definition, it is a commodity device that comes off the assembly line with no specific functions in silicon. If PLDs are included as ASICs, that adds another $417 million or so to the value of 1987 ASIC revenues, and also changes the lineup of players. For example, Monolithic Memories Inc. is a preeminent PLD supplier, with 1986 sales of $150 million—about half the PLD market.

Given the growing importance of the ASIC market, it's not surprising that leading chip houses are preparing a formidable market assault. They need to protect their ownership of the vast standard-logic and VLSI markets, both from foreign competition and from the increasingly stinging penetration of the pioneering semicustom houses.

The ASIC thrusts by the major U. S. semiconductor makers build on their strengths as standard logic suppliers. For example, they are trying to build



large libraries of standard cells based around their existing standard lines, including their 32-bit microprocessors. With these broad-based product lines, they hope to compete in every segment of the ASIC market. They also hope to beat back the growing foreign competition in ASICs, mostly from the Japanese semiconductor houses that already are among the world leaders in gate arrays.

This is the second time around for most of the U. S. majors. They first jumped into ASICs in the early 1980s, when the semicustom houses opened up the business. But almost without exception, they stumbled, fell back, and regrouped. Now companies such as Motorola, Intel, Texas Instruments, and National are solidly back in ASICs with new strategies for success.

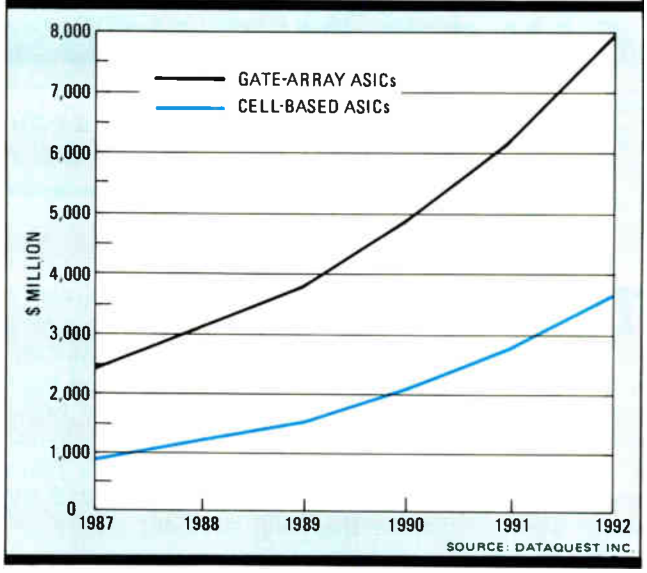
However, executives at the semicustom houses believe that the majors will never take over in ASICs because they can't provide the kind of services that their customers will need. The startup ASIC outfits of the early 1980s, LSI Logic Corp. and VLSI Technology Inc., to name two, were organized expressly to pursue the semicustom business, mainly gate arrays and standard cells. They were the innovators and provided the vital software tools necessary to carve functional designs in silicon. The cornerstone of the newcomers' approach was twin design bombshells: the ability to emulate virtually any logic device and to integrate entire systems within one or just a few chips.

But their real strength came from building customer relationships. Not having a standard catalog of off-the-shelf functions like those from the major IC houses, the semicustom intruders broke new ground—they worked closely with customers to define, design, and supply working silicon. Working so closely amounts to handholding—it makes the customer feel that he has selected a stable semiconductor vendor with the right technology and fast turnaround of reliable parts.

This, say the major semiconductor suppliers—who have yet to make a big dent in ASICs—is something they now understand after several false starts into ASICs. They say they will bring a barrage of technology to the fray, and match prototype turnaround times and production runs more closely to customers' needs; they will provide design training and help with the systems implementation, too.

Even if the established semicustom houses are skeptical about the latest efforts of the big chip firms, they are not taking any chances. They are seeking haven in niche markets or moving up in technology, toward gate arrays with 200,000 gates or ones with on-board memory or programmable logic; or they are unwrapping new ASIC alternatives sporting new terminologies: semistandard, value-added semicustom, or customizable standard ICs. The idea here is to leverage ASIC technology into the VLSI arena and to tailor or customize chips to greater degrees of functional specificity.

WORLDWIDE ASIC USE WILL SOAR



Of course, the major semiconductor houses can try to make their chips easier to customize more fully, too. But they are likely to take a different route—by way of PLDs or gate arrays, or by incorporating customer-alterable sections into standard products, through mask-programmable circuits or compiled cells.

The following special issue discusses the megatrends in the ASIC market. The first article concentrates on the expanding role and general strategies of the major semiconductor companies. Then, an eight-page profile section delineates the individual plans and strategies of five major contenders: Motorola, Intel, Texas Instruments, National Semiconductor, and Fujitsu. These five, say many observers, are the companies most likely to succeed in ASICs. Then another article delves into the responses of the original ASIC startups and briefly discusses the plans of an entirely new breed of ASIC contenders—systems companies that are trying to turn in-house ASIC capabilities into successful commercial ventures. Some side issues covered in the reports include CAE tools, ASIC testing, and what users feel about ASICs. Finally, a pair of Technology to Watch articles introduces two fresh ASIC offerings that aptly illustrate some of the big players' significant moves into ASICs: the largest biCMOS gate array, from Fujitsu, and a standard-cell microcontroller, from Motorola.

CAN BIG CHIP HOUSES MAKE IT IN ASICs?

They're optimistic as they go all out now to make it big, but doubts remain; those that fail could be shut out of half the logic market

by Larry Waller

The major semiconductor vendor that ignores ASICs is courting oblivion. ASICs are eating into the multibillion-dollar standard-logic market that until now has belonged to the big chip houses, and they are beginning to threaten the more lucrative high-end market for bigger chips and microprocessors. The question is not if the major semiconductor players will become ASIC houses, but how they will go about it—and whether they will succeed.

The first half of the question is easier to answer than the second. The major chip companies are pursuing strategies as varied as the companies themselves, but their plans have some traits in common. The big guys are all trying to build larger libraries of standard cells, including the all-important 32-bit microprocessors. They hope to offer broad-based product lines that compete in every segment of the ASIC market. To a large extent, they are counting on sheer size to give them an edge—the size of their investment in ASIC projects, the breadth of their varied manufacturing capacities, and the magnitude of the services they can offer. Most of them are scrambling to extend their ASIC capabilities still further through networks of strategic alliances, not only with other suppliers but with their customers. Each company is trying to accommodate the changing nature of the market; each is learning how to appeal to ASIC users.

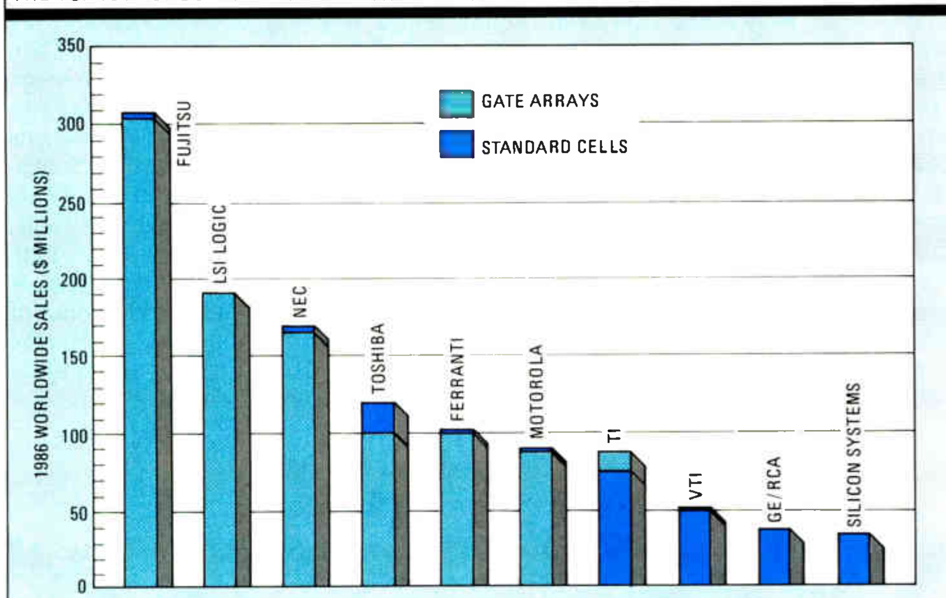
But the second half of the question is the subject of considerable debate. The major semiconductor companies, of course, think they're going to succeed. Industry observers, however, cite previous ASIC efforts by the major companies, dating back to the early 1980s, that fell apart. They point out that serious obstacles still confront the big chip houses. Chief among these is one of the factors the chip makers are counting on—their size. Big companies are slow-moving and inflexible, many analysts say, making them ill-suited to providing the close attention that ASIC customers demand. The major companies also face problems in trying to field broad-based product lines in a volatile market. And they must reconcile their budding ASIC businesses with established standard-parts operations—they have to figure out how to avoid competing with themselves.

They have plenty of competition elsewhere to contend with. The semicustom houses that have latched onto the U. S. ASIC business aren't giving up without a fight (see p. 73). Overseas, the Japanese semiconductor companies are already counted among the world leaders in ASICs, largely in gate arrays, as measured by the dollar volume of sales (see chart, below). European companies are coming up fast, mostly by concentrating on the high end, on systems on one or just a few chips.

The pace of activity among the many ASIC players is picking up speed because it is becoming increasingly clear just how high the stakes are. Both Integrated Circuit Engineering Corp., Scottsdale, Ariz., and Dataquest Inc., San Jose, Calif., predict that half of the $15.5 billion logic market in 1991 will belong to ASICs, up from 32% in 1986. Dataquest says 1987 will be a watershed year, marking the point at which more gates will be shipped in array form than in standard-logic form.

At the same time, another factor is working to shrink shipments of standard logic: higher levels of integration. Gate counts per device keep growing, says Dean A.

THE TOP 10 PRODUCERS: ONLY TWO U.S. MAJORS MAKE IT



SOURCE: INTEGRATED CIRCUIT ENGINEERING

Winkelmann, an ASIC watcher for ICE—going from a maximum of 10,000 gates in 1984 up to 50,000 in 1986. "These higher gate-count devices permit original-equipment manufacturers to use fewer units to accomplish the same tasks," he says, and that, of course, means chip houses sell fewer units, too.

So excelling in the ASIC market is nothing less than "a survival issue," says Kenneth G. Wolf, until recently the ASIC general manager at Motorola Inc., in charge of establishing the separate division Motorola has set up for ASICs (see p. 65). Lending urgency to the effort is the sense that no one has much time left to get into the market. "The clock is running," says Tom Miller, director of strategic marketing and business at Fairchild Semiconductor Corp. "By the end of next year, there will be many changes."

Right now, industry watchers are most interested in Intel, Motorola, and Texas Instruments. All of them are spending millions of dollars and untold man-hours to establish ASIC operations.

Both Intel and Motorola believe ASICs must make up about a third of their total semiconductor sales by the early 1990s. This figure represents a consensus culled from major forecasts, says Jack C. Carsten, the senior corporate vice president assigned two years ago to get Intel Corp.'s act together. "Some forecasts project ASICs taking over up to 60% of all logic. Some say lower than one third," he says. "We think that latter figure makes sense."

The magnitude of the big chip makers' investments underscores their determination—Intel, for example, has already shelled out $75 million (see p. 66) to carve out a chunk of the ASIC market. New organizations and product lines are in place. Nearly all the big guns have stepped up efforts in CMOS gate arrays, as they try to challenge LSI Logic Corp.'s No. 1 position. (Such houses as Motorola and Fairchild have been leaders for years in bipolar arrays.) And there's a surge of activity in the newest type ASIC to hit the market—the proprietary cell-based ICs, especially microprocessors and microcontrollers.

Most of the large companies started exploring ASICs early in this decade, although several of those first projects went nowhere. The latest efforts generally began about 1985, and since then they have evolved, often by a painful process of trial and error, into the current strategies.

Now both Intel and Motorola have offerings in the three major ASIC segments: programmable logic (which is not universally regarded as application-specific); arrays; and the new proprietary cell-based ICs. With the wide-ranging agreement signed by Intel and TI in July, TI will get access to the Intel processor cells, filling in missing key parts of its lineup (see p. 68).

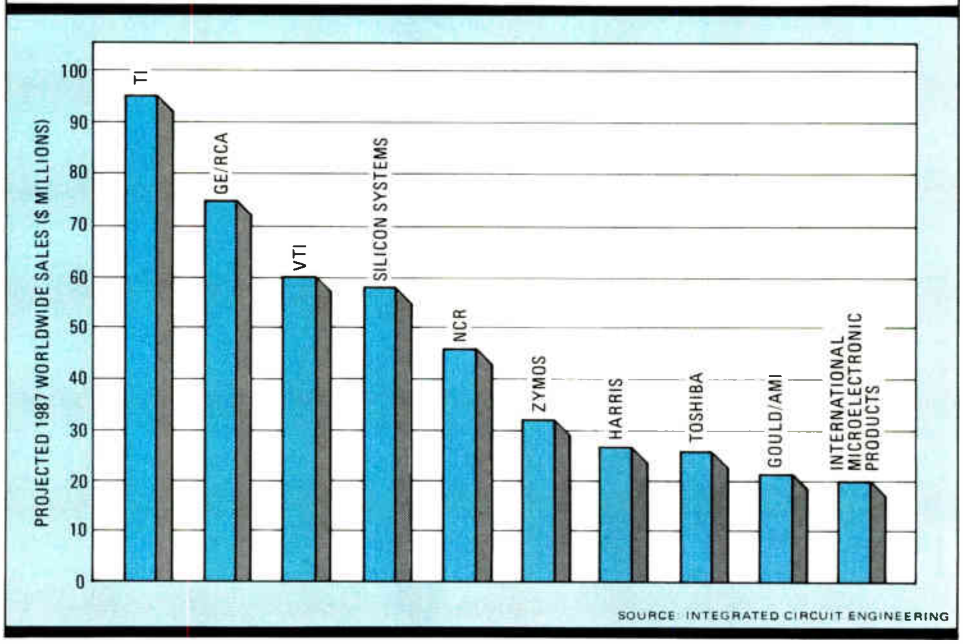
As they worked out their strategies, the companies found themselves adjusting to changes in the market they were preparing to assault. The leading semicustom market segment, gate arrays, is already showing signs of maturing. Heightened competition is driving the price per gate to such low levels—as little as $0.001 per gate last year for the most popular 2,000-gate CMOS chip—that profits are tough to come by. Libraries of standard cells look like the coming high-growth segment. Preeminent among these are new proprietary microprocessors and microcontrollers in a core-cell format, which can readily be integrated on-chip with key peripherals.

The shift could provide a major opportunity for the major companies. Gate arrays are where they're struggling hardest (see chart, left). In standard cells, the No. 1 and No. 2 suppliers this year are expected to be large companies—TI and the GE/RCA Solid State Division in Somerville, N. J.—although most of the other top 10 are semicustom companies or system houses (see chart, below). More important, the major companies have an edge here—they lead in microprocessors. "I think we're going to see a shift to the big guys," says William Groves, technology vice president at In-Stat Inc., the Scottsdale, Ariz., market researchers.

As expected, microprocessor leaders Intel and Motorola are at the head of the pack here. Their proven operating and application software, along with the vast numbers of users, should guarantee them a fast takeoff in core-cell offerings.

One of the first such products off the drawing boards was Intel's: the company early this year introduced its first core cell, the UC51 version of its popular 80C51 microcontroller. The product was an immediate hit with users—a graphic illustration of

U.S. FIRMS DOMINATE THE STANDARD-CELL MARKET



the power of proprietary technology. Motorola's comparable MC68HC05 one-chip microprocessor in cell format is now coming to market and evoking similar interest (see p. 80).

These proprietary architectures are important components of the strategy being followed by most of the major U. S. houses, but they're not the whole story. In varying degree, the big companies are trying to strike a balance among all the ASIC categories—standard cells, arrays, and programmable logic.

One way they're doing that is through strategic alliances. For example, two of the top three standard-cell suppliers—GE/RCA Solid State and VLSI Technology Inc. in San Jose, Calif.—are now sharing gate-array technology. They announced in late July that GE/RCA will act as a second source for VLSI Technology's VGT 10 CMOS gate arrays. Starting next year, it will also offer VLSI Technology's VGT 100 series, with up to 67,000 gates.

One important reason the big companies want broad product lines is to appeal to as many different ASIC users as possible. That's no small task, since exactly what those users want is open to question. The experience of both Motorola and TI, and a formal survey by Intel of user needs, challenge the conventional wisdom. Specifically, they challenge the notion that prospective buyers always put the latest technology and high density at the top of their shopping lists. Nor is low development cost a prime consideration. "To the contrary, customers will sacrifice higher complexity for timely delivery of a reliable product," says James A. Norling, vice president and general manager of Motorola's Semiconductor Products Sector, Phoenix, Ariz. H. Wayne Spence, vice president of TI and the head of its ASIC division in Dallas, says it a bit differently: "Number one is manufacturing capabilities and the ability to deliver a quality product on the day promised."

Intel's study buttresses this view. It shows that 65% of users believe getting a working prototype on the first pass is the most important criterion (see chart, next page). Quick turnaround (now about four weeks without paying a premium) is a close second, followed by high performance at 49%. Low development cost is less important; only 28% list it as a high priority.

SYSTEM DESIGNERS' GROWING LOVE AFFAIR WITH ASICs

System designers increasingly are embracing ASICs. Their love affair, in part, has driven systems companies to abandon standard chips for ASIC parts. They are especially committed to gate arrays right now—CMOS, emitter-coupled logic, and even some relatively high-density gallium arsenide arrays. "Gate arrays are the wave of the present," says Len Schar, vice president of development for Elxsi, a San Jose, Calif., minisupercomputer maker. "We use gate arrays heavily, and we will continue to use a lot of them far into the future."

Like all ASICs, gate arrays shorten the time to market for new products, improve performance and reliability by putting more functions on-chip, and reduce the number of boards in a system. System makers prefer arrays because they have had more experience with them than with standard-cell ASICs, and because more design tools are available for them.

Without ASICs, some new computers could not have been built in the time required or at the price-performance levels they achieved. One example is the C1 family of minisupercomputers by Convex Computer Corp. in Richardson, Texas. The C1 is built around VLSI CMOS gate arrays that at first had 8,000 gates and now have 20,000.

Another example is the recently introduced Sun-4/260 super work station. Sun Microsystems Inc. designers chose VLSI CMOS gate arrays to implement the first version of the reduced-instruction-set central processor and the floating-point coprocessor for the Sun-4. "Very simply, the choice of gate-array ASICs was dictated by wanting to be first with a very-high-performance RISC work station," says Arun Taneja, product marketing manager for high-end systems at the Mountain View, Calif., maker of work stations and network systems.

Systems designers also like the increasing number of gate-array sources, as well as the upward trend in densities and speeds and the downward trend in prices. But however much designers love arrays, one issue bothers them. They would like to see some standardization of interfaces and design tools. "If you use three ASIC vendors, you need three different sets of design tools for three different interfaces," says Steve Wallach, Convex Computer's vice president of technology.

But because of the lack of standardization, designers usually stick with a single ASIC vendor. That places some limitations on their design, cost, and time-to-market flexibility.

Although working with a single vendor may prevent shopping around for the lowest possible price for each type and size of gate array, one company, at least, sees a tradeoff. "We tend to just focus on one gate array vendor at a time for a given design," says Bill Ward, vice president of development at Gould Inc.'s Computer Systems Division, another maker of minisupercomputers. "There are two main reasons for this focus. One is that each gate array requires different tools and interfaces. The other is that going to multiple vendors reduces the volume from any one of them, which means less leverage on pricing," says Ward, whose development group is in San Diego, Calif.

Given the tendency to stick with just one vendor, says Dave Rodgers, vice president of engineering at Sequent Computer Systems in Beaverton, Ore., "a key limiter or, on the other side, a predictor of success for ASIC vendors is the accessibility of their design tools by the customer. Most successful ASIC vendors are those with easy-to-use, accessible tools. An obvious example is LSI Logic. We also believe that Intel has very powerful tools, but it's not clear how easy to use they will be by people outside Intel."

An ASIC trend that several system designers view as very important is the combination of random-access memory cells with logic gates on ECL gate arrays. For the performance levels the high-end systems builders are reaching for today, "we need local RAMs on the chips with the [logic] gates—most importantly for register files," says Ward. – *Tom Manuel*

National Semiconductor is taking a more direct route toward finding out what its users want—it's making allies out of its customers. In 1986, it signed a deal with Xerox Corp., whereby National gets a significant part of Xerox's business and in return grants Xerox the right to produce a percentage of National designs (see p. 70). The two also work closely to define and design new cells for the CMOS library, even sharing confidential product plans.

With strategies in place and product lines readied, the big companies believe they're ready to make their move. They also believe they've got some built-in advantages as they do. TI's Spence lists them: better capability for developing new technology; a standard product base to drive complex functions into products; designers who fit these products into systems; and, in particular, plenty of manufacturing lines. The breadth of these fab lines could give the big manufacturers an edge over the smaller semicustom houses. "The market previously has been divided among many vendors of partial solutions," says Intel's Carsten. "But the major opportunities exist for a broad-based supplier with products and expertise in standard components, as well as all major technologies."

Besides the obstacles U.S. chip makers face simply to establish themselves as strong ASIC competitors, they must also confront a strong Japanese presence

Besides manufacturing capability, the big companies believe they can offer better service, including field sales and design centers. Contrary to those who wonder if a large chip house can attend to an ASIC user's needs, TI's Spence argues that "we may be slow, but we've got very large, well-trained, field-support organizations. As we come up to speed, that will be a big leverage in the marketplace."

However, industry watchers with vantage points above the ASIC battle aren't sure all that optimism is justified. They are still skeptical because of the missteps the big U.S. firms made in the early 1980s, for one thing. These observers still think large, inflexible organizations can't provide customized service along with the customized parts, for another. And they point out there are problems with various aspects of the strategies the major companies are currently pursuing.

For example, balancing product lines among all ASIC categories is easier said than done—it's hard to field winners in each category. At least one major manufacturer agrees: "We're all looking for that path through the tulips," says Fairchild's Miller. The difficulty is "having to find some significant value-added products while playing catch-up in the face of tremendous competition." Fairchild has reacted successfully by pushing its line of 2-μm CMOS arrays, whose 0.5-to-1-ns gate speeds give them the performance of 1.25-μm-level devices, Miller says.

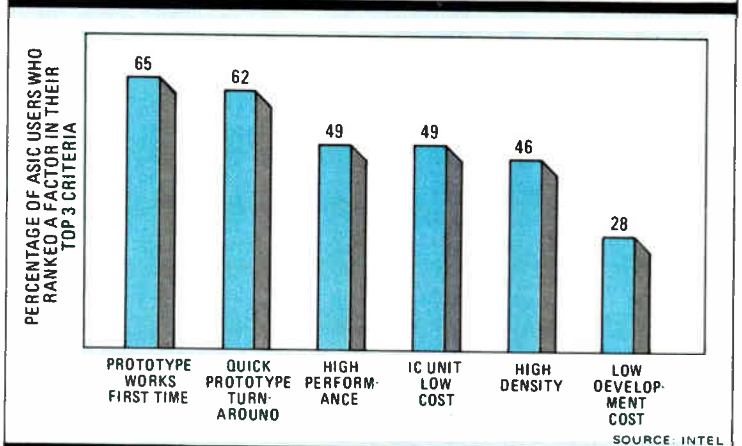
Then there's the tricky balancing act of positioning ASICs against standard-logic parts, which can be like robbing Peter to pay Paul for the big houses trying to protect an existing market. National Semiconductor meets this threat head-on, turning a potential liability into an asset by giving users a choice. "We are trying to offer them the alternative of having the same function in an ASIC as opposed to a standard product," Horne says. That way, the user can "further integrate his design without having to change the software or the size of the hardware."

A potentially more serious problem for all the big companies is that the important standard-cell libraries so far can't compare to those assembled by the leading semicustom firms. VLSI Technology Inc., for example, has some 400 cells at the LSI level already in its library, one consultant estimates. The TI-Intel libraries combined have only about half that number, discounting duplication, the consultant says. In general, the semicustom outfits also have pushed cell complexity far ahead of their larger competitors.

But besides the obstacles they must overcome simply to establish themselves as competitive ASIC vendors, all of the major U.S. chip houses face the formidable threat of the Japanese. Fujitsu, NEC, and Toshiba already are among world leaders in ASIC sales for 1986, according to ICE. It must be disconcerting for the U.S. to realize those companies got to be leaders by taking an approach diametrically opposed to the strategy of most of the U.S. companies. In Japan, ASIC operations are working smoothly within the structure of the parent chip company, not segregated from the mainstream business as are most U.S. ASIC projects.

However, the Japanese approach is not foolproof, to judge by Fujitsu Ltd. Although it leads the world in ASIC sales, few of its products are visible overseas (see p. 71). This is because Fujitsu sells mostly to a few large firms in the U.S., including the Amdahl Corp., in which it has a 47% interest. Also, Fujitsu owes much of its success to an early start—it began selling TTL arrays as early as 1977. It has mounted an effort to expand its business with improved array lines, five U.S. design centers, and an assembly op-

WHAT'S IMPORTANT TO ASIC USERS



eration in San Diego. But analysts say Fujitsu is losing ground to NEC Corp. and Toshiba Corp. as its growth slows, albeit from a wider base.

NEC is pushing its overseas operations because growth rates are higher abroad than in its domestic market. Foreign sales could amount to 20% of its ASIC business this year, says Kodo Kimura, manager of the Customized LSI Department, Application-Specific LSI Products Division, Kawasaki. NEC has eight design centers in Europe and four in the U. S., with three more ready to come on line in the U. S. Designs can be done on most work stations, then sent to Japan by satellite network for processing. NEC's ASIC products include arrays and standard cells in many processes (see p. 82), but mainly in CMOS.

Toshiba has benefited greatly from its role as a gate-array manufacturer for LSI Logic, although it has not been a supplier to that company since mid-1986. Not only are its computer-aided design tools ahead of Japanese competition because of the LSI Logic association, sources say, but designs formerly supplied to LSI Logic are now becoming standard Toshiba offerings.

The Japanese are not the only foreign competition facing U. S. chip houses. European companies are working hard to field their own ASIC product lines. European manufacturers have lagged behind the U. S. and Japan in both production and use of ASICs—Kurt Friedl, product manager for semicustom ICs at West Germany's Siemens AG, pegs Europe's ASIC consumption at only 10% to 15% of the world market. But awareness is picking up, according to both Friedl and his counterpart at the Dutch giant Philips, Tom Keve, manager of the business unit, and so are both companies' ASIC efforts.

Philips got an earlier start in the business than Siemens, with designs for in-house use in 1974, using standard cells and MOS silicon-gate technology. Its present commercial effort is led by the SystemCell line of CMOS standard cells. Siemens started working on ASICs in the early 1980s.

Both companies have design centers throughout Europe, and Siemens is building a semicustom unit in Santa Clara, Calif. Siemens' activities are limited to bipolar types, but it is building a CMOS capability.

Playing a central part in both companies' strategies are alliances with other firms. Philips has worked with TI since 1984, in a deal expanded last year to include European Silicon Structures. Siemens has formed an alliance with Toshiba and GE.

Both Friedl and Keve agree that big companies will be the winners in ASICs. "Only they can afford to invest heavily in CAD systems and other equipment needed to make devices of higher and higher complexity," Friedl says. □

ASIC TESTING STARTS TO GO ITS OWN WAY

Silicon foundries are able to test advanced ASICs in production quantities today only because the manufacturers of automatic test equipment have pushed their systems' performance to keep up with all VLSI circuits, including ASICs. Now, though, ASIC testing is changing from simply one aspect of VLSI testing to a kind of testing based specifically on ASIC production economics.

Industry estimates of VLSI testing costs now range from 30% to 50% of total production costs, around twice that of LSI chips. ASICs usually involve higher costs than standard ICs because ASIC production volumes as a rule are less, which adds to the cost per chip for test engineering and other ATE overhead.

To help users reduce test-engineering costs, manufacturers of computer-aided design systems, ASIC design-verification equipment, and ATE systems are pursuing design-to-test strategies. The goal is to use testing data developed during CAD in production testing of the resulting chips. For example, some ATE systems can now generate test vectors from the patterns that designers originally develop to check chip operation during a computer-simulation run or to debug prototype chips with ASIC verifiers.

ATE manufacturers are also striving to reduce the hardware costs of general-purpose systems as another way of making low-volume ASIC production less costly. This is leading to a split between high-end systems for component characterization and other engineering work and slower systems costing under $1 million for routine production testing.

At the high end, the tester-per-pin architecture is coming to the fore as a way of testing high-performance circuits with greater precision. Instead of sharing central test resources, each test channel contains its own test-pattern-timing generators and other resources. Teradyne Inc., Woodland Hills, Calif., for example, went to the tester-per-pin architecture in its J953 VLSI test system to achieve an overall system timing accuracy of 250 picoseconds [*Electronics*, Nov. 13, 1986, p. 72].

Some companies are modifying this architecture to develop lower-cost systems for particular testing applications. For instance, Tektronix Inc.'s $800,000 LT-1000 is designed to test CMOS ASICs with up to 256 pins at clock rates to 50 MHz.

In contrast, high-end VLSI testers generally range between $1 million and $3 million. The typical system now runs at test-data rates to 50 MHz on up to 256 channels, or to 100 MHz with channel multiplexing, and some expand to as many as 512 pins. In this class of system, the pace is being set by Advantest Corp. and Ando Electric Co., both based in Tokyo. Both companies have new 100-MHz systems that reach 200 MHz with multiplexing.

That further increases are likely is indicated by the Department of Defense's Very High Speed Integrated Circuits program. The Rome Air Development Center, Rome, N. Y., which is responsible for VHSIC test techniques, has called for 512-pin systems operating at 250-MHz data rates [*Electronics*, Feb. 3, 1986, p. 42].

However, there's a growing consensus that standardized chip self-test techniques will be the key to efficient testing of future ASICs. Test circuitry has already been built into some ASICs to make these chips easier to test and to expedite the testing and maintenance of end equipment. For similar reasons, the VHSIC program also calls for chips with built-in self-test circuits and standardized test interfaces [*Electronics*, June 11, 1987, p. 68].

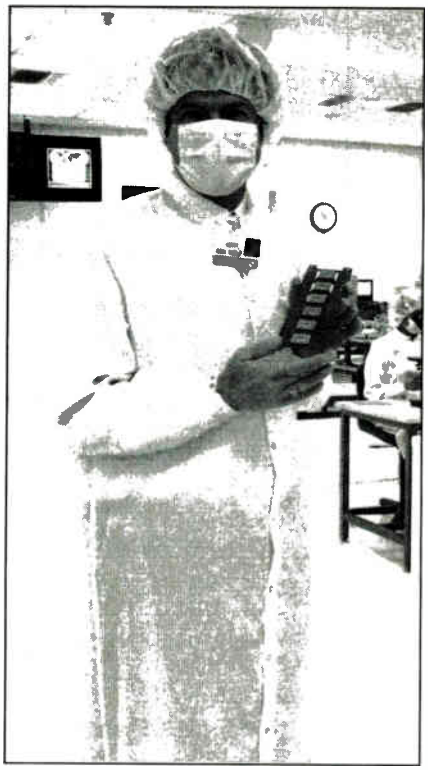
–George Sideris

MOTOROLA's BATTLE TO SPIN OUT ASICs

Moving its semicustom products out of a standard-products business to an independent unit is far more difficult than the firm had expected

If any doubts still linger about the challenges posed by ASICs for the major chip makers, consider the changes they have forced at Motorola Inc. during the past two years. In 1985, Motorola's management came to a painful decision, made even tougher by a business downturn: a semicustom business cannot be built within a company framework geared to standard products.

So late last year, Motorola pulled its ASIC operations together in a single division, set up as a separate entity in Chandler, Ariz., some 25 miles south of the Semiconductor Products Sector's Phoenix headquarters. Now in place are the needed ASIC elements: a quick-turnaround front-end fabrication line; dedicated sales and service staffs; new computer-aided-design tools. But spinning them smoothly out of an entrenched organization has proved to be far more difficult than anyone expected.



FORMER ROLE. The masked man is Kenneth G. Wolf, the former general manager of Motorola's ASIC division. His departure could mean trouble for the fledgling operation.

"Breaking something away is hard to do," observes James Norling, the Semiconductor Sector's general manager. The toughest task of all, he says, is "dealing with the problem all big companies have [going into ASICs]—minds imbued with the standard-parts orientation." Reeducating semiconductor people with big-company backgrounds to perform effectively in a business that depends on heightened levels of customer service remains a daunting job, Norling admits.

But the steady inroads that ASICs are making into bread-and-butter, standard-logic markets mean that changing the corporate culture is imperative. "Success in ASICs is a survival issue," says Kenneth G. Wolf, who until last month was general manager of Motorola's ASIC division [*Electronics*, July 23, 1987, p. 32]. "We cannot be a major player without it."

Wolf's resignation, in fact, has industry watchers wondering about Motorola's ASIC strategy. A highly regarded executive with an entrepreneurial flair rarely found inside Motorola, Wolf left to head a Silicon Valley startup. The timing of his departure indicates to financial analysts that Motorola corporate officials are not satisfied with the slow pace of ASIC sales so far, and are increasing pressure for performance. The analysts tend to think that it is critical for Motorola to name quickly a successor cast from the same mold as Wolf.

The reason is that last year, ASIC revenues amounted to about $89 million, less than 5% of Motorola's total semiconductor sales, according to Integrated Circuit Engineering Corp., a Scottsdale, Ariz., consulting firm. Although its ASIC sales place Motorola among the top 10 ASIC suppliers in the world, they largely result from sales of only one line, the established bipolar Macrocell gate arrays, to computer makers.

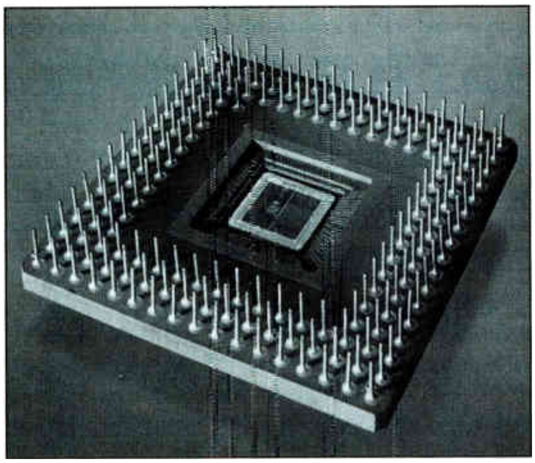
To broaden its sales, Motorola went to centralization in Chandler, in part to solve problems stemming from Motorola Semiconductor's widely spread manufacturing operations. Microprocessors and MOS technology are centered in Austin, Texas; other operations are scattered throughout the sprawling Phoenix area. That's not a problem with standard parts, but ASIC customers want fast turnaround, "and the logistics were killing us," says Wolf.

The decision to bring all ASIC operations under one roof was the first step in solving the problem. Then the ASIC team went further, rethinking all phases of device sales, design, and production. Most of the recommended changes are now in place or being made; the result is that the Chandler setup bears little resemblance to a conventional Motorola semi-

In this eight-page section, *Electronics* look at how five big chip makers—Motorola, Intel, Texas Instruments, National, and Fujitsu—are going about getting established in the ASICs business. Several tried and stumbled and started over, some formed alliances with each other or with customers, and one has already been in the ASICs business for over a decade. What all of them are proving is that for the big merchant companies, the ASICs field is a difficult one to cultivate, and that there is no one strategy that everybody agrees on.

conductor operation. For openers, the revered economies of manufacturing scale—standard designs crafted for high volumes—do not apply.

Instead, the emphasis is on front-end fabrication with a flexibility tailored for a changeable mix of small lot sizes and fast cycle times. "In prototyping ASICs, one wafer is the ideal lot size," says Wolf. "And for production, 10,000 chips is a large order." When the choice is between volume and flexibility, "smaller is better," he adds.



PUTTING IT TOGETHER. Motorola has achieved in the lab up to 10,000 gates with its new biCMOS arrays.

The flow chart tracing a chip's trip from post-fabrication through shipment also has undergone radical surgery. "We analyzed the flow and threw out the manual," says Wolf. The result is travel distance reduced from 1.5 miles to 900 ft, and cycle time cut from 28 to 3.6 days, excluding burn-in. In the process, all chip assembly and test operations have been reduced to eight jobs, all of which every worker can perform, in an area that allows all tasks to be in sight.

Company strategy calls for attaining balance by adding CMOS arrays, standard cells, and, most important, microprocessor-based core cells built on the firm's highly successful proprietary technology. The goal, when the operation hits top speed in three years, is for a third of all semiconductor sales to be in semicustom work.

To that end, Motorola since 1985 has poured more money into ASICs than any other operation of the Semiconductor Sector, according to Wolf. In his view, the thorniest challenge is "to crack the CMOS nut in 1987–88." By its own admission, Motorola lags in CMOS process technology.

The company seems to be making some progress in CMOS, though the going is tough as the firm scurries to make up for a late start. Its CMOS gate arrays have moved up the density ladder, to 8,500 equivalent gates at the 2-μm level.

Further along is the core-cell-microprocessor effort. The company has just introduced its first such product, the top-of-the-line standard-cell core of a popular stand-alone microprocessor chip, the MC68HC05 (see p. 80). The next cell core, due next year, is the 68HC11, the microcontroller with an array of electrically erasable programmable memory that currently is in such demand that its supply is limited.

For other standard-cell functions, Motorola continues to expand its library in concert with NCR Corp., with whom it has worked since mid-1985 under a joint development and technology-exchange pact. However, contrary to industry perception, NCR has little direct impact on Motorola's proprietary-cell development, reports John Carey, Motorola's ASIC merchandising manager. Rather, each firm's specialties are brought to bear by dividing design and research chores, a process that exploits strengths such as Motorola's prototype-testing capabilities and NCR's software-simulation tools.

In gate arrays, Motorola's strategy is to continually upgrade the Macrocell bipolar line by moving to higher densities, while gaining credibility as a CMOS supplier. With its new biCMOS arrays, which combine the two processes, Motorola has achieved lab versions of chips with densities of up to 10,000 equivalent gates.

The phase-in this year of Mosaic III 1-μm technology, which upgrades the 2-μm Mosaic II process in use since 1982, maintains Motorola's leading-edge role in bipolar technology. Mosaic III can now produce emitter-coupled-logic Macrocells with 10,000-gate densities, and devices with 40,000 equivalent gates perhaps next year, says Carey. Also, the division has employed its semicustom techniques to spur development of the new Eclips (ECL in picoseconds) family of standard ECL logic—an example of ASIC work that feeds back into Motorola standard lines. The family boasts 500-ps gate delays and 600-MHz speed. *–Larry Waller*

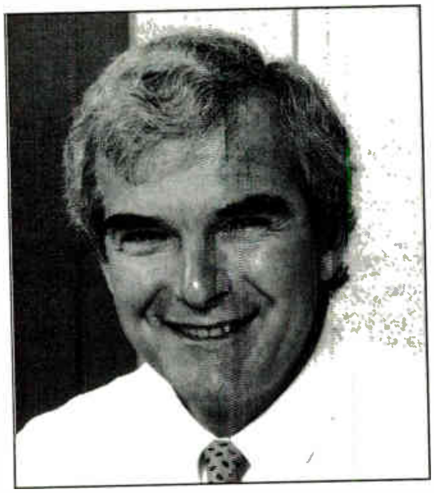
AFTER FALTERING START, INTEL PICKS UP STEAM

Like archrival Motorola Inc., Intel Corp. got off to a faltering start with ASICs. It, too, had to shut down its initial ASIC operation in late 1985, rethink the issue, and start all over again. And the Santa Clara, Calif., giant came to the same conclusion as its Phoenix counterpart: ASICs should be produced in their own facility, separate from standard parts.

Early last year, Intel's self-contained ASIC Components operation was established, and it now appears to be gathering steam. "We're getting the first onslaught of design wins, and recurring orders," says Intel president Andrew S. Grove, who has staked $75 million and considerable corporate prestige on the venture.

Grove's charter to senior vice president Jack C. Carsten, the architect of the ASIC unit and the man who runs it, was "to rethink the problem and begin anew with a clean slate, as an independent business, almost like a startup," Carsten recalls. He could pick from Intel products and resources, and go outside to fill in the blanks.

Both men are upbeat about how well the resulting scheme is work-



CARSTEN: His bosses at Intel told him to "rethink the ASIC problem and begin anew with a clean slate, as an independent business, almost like a startup."

ing. Although Intel does not disclose ASIC revenues, financial analysts believe they could reach $25 million to $30 million this year, a sharp increase from less than $10 million in 1986. But the real takeoff will occur in 1988, when sales of $75 million to $90 million are predicted. Grove is even more optimistic: he says ASIC operations could be in the black in 1988.

Moreover, ASIC Components has just introduced its first powerhouse standard ASIC part: dubbed the UC51, it is a version of the best-selling 8-bit 80C51 microcontroller, with most of its peripherals, in the core-cell format most useful for fast-turnaround semicustom work. Creating such parts—which are based on the company's muscular microprocessor line, and which can be infinitely varied to customer requirements—is Intel's bedrock ASIC strategy.

In addition, the company on July 7 signed a sweeping ASIC pact with Texas Instruments Inc. [*Electronics*, July 23, 1987, p. 32]. The joint approach in CMOS devices by two of the largest U. S. chip houses should speed standardization, which figures to help the biggest suppliers—like Intel.

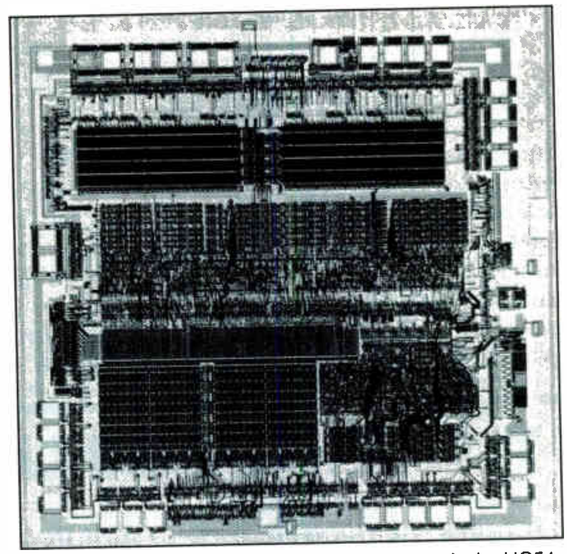
Indeed, Intel sets great store on being a broad-based ASIC supplier, spanning the major product technologies. Besides the obvious revenue potential inherent in size, the wide range of choices also makes sense strategically. Intel sees the now-fragmented ASIC marketplace moving toward fewer players.

So demand may best be served by a supplier that has not only the widest selection of products, but compatibility with numerous standard design tools. That happens to describe Intel.

Separating the ASIC effort from standard-product divisions was a radical departure for highly integrated Intel, and to make sure it worked, the ASIC team was handpicked from top to bottom—from management through design, sales, service, and manufacturing personnel. According to Carsten, the split was the only way to adapt to the nature of ASICs, "which is, passionately, a service business."

As a result, the ASIC group "becomes part of the customer's critical path," says Jeffrey Katz, director of marketing and design center operations. Because the parts are unique and Intel is the sole source, company engineers consult closely with the customer all the way through product development. With standard products, the relationship usually ends with delivery of devices. "We have put special capabilities in place and go to great lengths to reduce waiting time," Katz says.

Building an ASIC strategy around its popular microprocessors came naturally to Intel. In fact, Carsten considers the processors "one of our unfair advantages—and our Intel birthright." But turning them into ASICs was a stumbling block in the abortive 1982–84 attempt. When Grove concluded nearly two years ago that ASICs could not be intertwined with standard parts, he says, "I sent Carsten out to see what the [ASIC] business is about. What we were trying to do can't be done in an established [company] architecture." Carsten says Intel learned that, in part, from a very good teacher—IBM Corp.



POWERHOUSE. Intel's first standard ASIC part is the UC51, a version of the best-selling 8-bit 80C51 microcontroller.

In October 1986, Intel forged a deal with IBM permitting use of IBM's time-proven computer-aided-design tools and gate-array cell designs. "We're fortunate in having them as partners, because IBM is the granddaddy of the ASIC business," says Carsten. IBM has used its semicustom development tools successfully on more than 15,000 internal designs since 1980, and employed the arrays on its products for a decade. Part of the advice from Big Blue was to proceed with caution, Carsten says, taking products outside to customers only when all elements are firmly in place.

Intel's ASIC revenues could triple this year to $25 million or more, but the real spurt may come in 1988

Intel has heeded the message: an example is the 1.5-μm CMOS process offered for all Intel ASIC devices. It is well proven, and no other big U. S. company is using one like it for its semicustom products, Carsten says. And although some 1-μm CMOS lines are already running at Intel, Carsten says the company will "wait until the process settles down," and offer it next year in ASICs.

Intel is bringing its ASIC philosophy to bear on a wide range of products at whose center are the cell-based ASICs, like the UC51 microcontroller. These will be fully characterized cells providing logic, memory, input/output, and special functions. The UC51, for example, integrates about 2,000 gates of user-defined control logic and 8 Kbits of programmable read-only memory. The Intel Integrated Design Environment Library runs on several industry-standard CAD platforms, including those from IBM, Digital Equipment, Daisy Systems, and Mentor Graphics.

The gate-array offerings include two families, ranging in complexity from about 2,500 to 19,000 equivalent gates. At the lower end of the complexity spectrum are Intel's programmable logic devices, consisting of six erasable PLDs with densities of 300 to 1,800 equivalent gates.

Interestingly enough, the newly separated ASIC division is generating substantial business internally from standard-product operations, which often cannot turn a new design into finished silicon fast enough to meet a customer's demand. The ASIC prototyping setup can perform the turnaround cycle in four months, from mask making to final testing. Intel's term for this process is application-specific standard products, and its designs go into the ASIC cell bank.

–Larry Waller

TI GAINS BY BUILDING ASICs ON ALL LINES

It takes the opposite tack to Motorola and Intel; it also targets 3 separate ASIC businesses

In rebounding from its own initial ASIC debacle, Texas Instruments Inc. is following a route markedly different from that taken by Motorola and Intel. While these two big producers decided they couldn't make ASICs in the same fabs that turn out their commodity parts and so set their ASIC manufacturing operations apart, TI instead augmented its standard lines to accommodate the fast turnaround that semicustom work demands. Now all the Dallas company's lines are turning out both standard parts and ASICs.

"We've stopped talking about 'the ASIC market' and have started talking about three [ASIC-market] segments as separate businesses," says H. Wayne Spence, the TI semiconductor vice president for ASICs. Four different new product lines are now aimed at those segments (see table). And TI is backing them up with fast-stepping fab lines, an arsenal of design tools, and its globe-spanning army of semiconductor salesmen.

TI is bringing to bear on this effort its considerable production muscle, largely the result of a move that put all the firm's manufacturing schedules onto a weekly, instead of a monthly, cycle. "For several years we have been on weekly operating plans in the fabs, and we are now moving rapidly toward a daily operating plan across all of TI," says Spence, noting the benefits to the fast-turnaround ASIC world.

"We find we are able to respond better in fast cycle time than many of the small [ASIC] firms, which must go through several outside operations to get photomasks or assembly," he adds. To prove their point, TI managers cite a crash-schedule job for Seagate Technology, the Scotts Valley, Calif., disk-drive maker. TI says it delivered a prototype logic-interface chip based on a standard cell just 22 days after Seagate engineers phoned in a design.

TI POSITIONS ITS ASIC PRODUCTS FOR THREE MARKET SEGMENTS

Target market	Technology focus	Products	Gate density
Logic consolidation	Low cost, fast turnaround	TGC100 series CMOS gate arrays	3,200 – 8,900
High-end CPUs, proprietary architectures	Density, speed, flexibility	TGC500 series CMOS gate arrays	3,200 – 16,000
		TGE8000 series ECL gate arrays	8,500 (other sizes in development)
System consolidation	System integration	TSC500 series standard cells	50,000 and up

SOURCE: TEXAS INSTRUMENTS INC.

Another fast-reaction stratagem involves designer tool kits that team standard components and ASIC chips for specific applications. The first such product to appear is aimed at consolidating the needed glue logic for token-ring local-area-network adapters based on TI's TMS380 chip set. Using "soft macro" blocks from TI's 2-μm standard-cell library, designers can cut the adapter-card size by half. The company is planning a similar tool kit for memory-system design, bundling ASICs with dynamic RAM controllers and specialty memories.

The tool-kit concept enables TI to take advantage of its traditional strengths in commodity IC products. The company, like other commodity suppliers, is also moving its standard product designs into its CMOS standard-cell libraries for eventual use in semicustom circuits.

TI won't say what its ASIC sales goals are beyond predicting that the five semiconductor product categories in which ASICs are included will account for more than half of its chip business by the early 1990s. The company does allow that it expects its ASIC sales percentage to match the industry's, estimated variously as a third to a half by 1991.

To hit that mark, Spence has carved up the ASIC business into two distinctive market segments built around gate arrays and one on the newly emerging standard-cell ASICs. The first gate-array segment is focused on low cost and fast turnaround, or what the company calls the cost-sensitive logic-consolidation market. The second aims at density, speed, and flexibility, the market that TI identifies as high-end CPUs and proprietary architectures. The standard-cell segment is system integration—TI refers to it as system consolidation.

To market them, the company is pulling on strength from a worldwide sales force that is in touch with nearly every corner of the electronics industry. Just as it does in the commodity market, TI is counting heavily on its global presence, especially in the Far East. "We feel a significant percentage of the electronics market will be centered in the Asian-Pacific basin, and a presence there is key," says Spence, pointing to TI design centers in Hong Kong and Taipei as well as several in Japan.

The company is also touching all technology bases. In gate arrays, TI has introduced a new series of fast-turnaround 1.2-μm CMOS arrays, the TGC100 line, featuring what TI managers say are three of the most commonly used logic densities: 3,200, 5,400, and 8,900 gates. Production volumes are beginning to ramp up, and TI promises prototypes within 14 calendar days.

To compete with high-end processor architectures, TI is readying the TGC500 series of 3,200- to 16,000-gate CMOS arrays. The 1.2-μm CMOS family will be available in the third quarter, with prototypes available 21 days after final sign-off of design. And on June 28 TI disclosed it will be reentering the bipolar-array arena with a new emitter-coupled-logic series, the TGE8000. The 8,500-gate ECL array will be made from TI's triple-level metal 1.5-μm process, known as ExCL [*Electronics*, March 19, 1987, p. 73]. Also, TI will introduce a 12,000-gate ExCL-based array, parts with embedded random-access memory, and ECL parts featuring standard TTL input-output levels.

For the standard-cell ASIC market, TI is honing a 1-μm CMOS standard-cell library with its new

SPENCE: For all its manufacturing schedules, TI is bringing its production muscle to bear by moving toward a daily operating plan after several years of using a weekly plan.

ASIC partner, Intel (see p. 66). Under the five-year agreement, TI and Intel will develop common cell libraries and the compatible CMOS processes needed to provide alternate-source manufacturing.

Initially, the two will make available by year's end a CMOS library of common small- and medium-scale integrated logic functions as well as a number of large-scale blocks, such as microprocessor peripheral functions, bit-slice-processor components, register files, and memory circuits. They will be produced with CMOS technology ranging from 1.5 μm to 1.2 μm, and prototypes are expected in the first half of 1988. Besides developing 1-μm CMOS technology for the standard cells, the two partners will develop a common gate-array macro library.

TI's now-robust ASIC effort comes on the heels of a particularly painful beginning. The company eased carefully into the business in January 1981, selling small bipolar logic arrays of 540 and 1,008 gates. But two years later, its portfolio lay in a shambles after photolithography problems prevented it from shipping 2,500-gate TAT020 arrays made from 2-μm advanced Schottky transistor logic. The commercial ASTL arrays were dropped as TI retrenched, leaving a number of major minicomputer houses angry and many scrambling for replacement parts.

"The trials and tribulations are always there in any startup, whether it is inside a large company or a small one," admits Spence, who in 1983 took over the crippled semicustom-product thrust. "The TAT problems probably hurt us more than anything else." The demise of the TAT arrays also left TI's bipolar second source, Harris Corp., suddenly alone in trying to unscramble the mess.

TI quickly shifted its semicustom-product efforts to standard-cell technology as it began a corporate-wide drive into CMOS. In mid-1983, the ASIC operation was combined with TI's full-custom business and given a new divisional status under the name of Custom Components. That name was later changed to ASIC Components as semicustom sales grew.

Then, TI announced in early 1984 that it was second-sourcing CMOS arrays from Fujitsu Ltd. of Japan; it is still making them today. In the meantime, company engineers began turning their full attention to standard cells. "We chose to go after a position we thought would be long-term—what we now call the system-consolidation phase of the market, which is going to be served by 1-μm CMOS standard cells," says Spence.

Today, not everyone is convinced that TI's new efforts guarantee success. One market watcher, Michael A. Gumport, semiconductor industry analyst at Drexel Burnham Lambert Inc. in New York, believes TI, like others deeply rooted in the commodity chip markets, faces manufacturing challenges in addition to the more obvious design-service difficulties of ASIC markets. "It is not clear that the things that made TI big and strong are going to help make it succeed in ASIC."

But Gumport does concede that TI's new agreement with Intel gives both of the companies unprecedented power. He says TI

For the standard-cell market, TI and its new ASIC partner, Intel, are readying a 1-micron CMOS library

provides the strength of one of the top three commodity-chip producers and a leading-edge technologist, while Intel is the industry's "most important standard-cell 'librarian.' "

However, Gumport also notes that the companies will face the hurdle that has stymied other cooperative efforts, such as the one between Intel and Advanced Micro Devices. "That was a partnership, and the two were going to exchange products on a value-for-value basis," he says, referring to this year's clash between AMD and Intel over trading rights for the 80386. *–J. Robert Lineback*

NATIONAL BETS ON CUSTOMER ALLIANCES

It views its partnership with Xerox as the next best thing to vertical integration

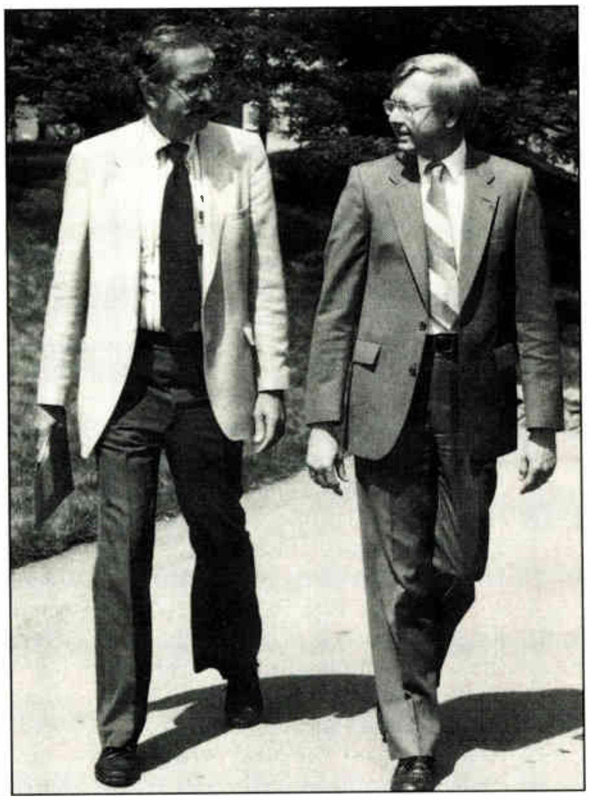
The best ASIC strategy for merchant chip makers is neither to go it alone nor to form alliances with other chip makers, argues National Semiconductor Corp. Instead, the path to success is to form alliances like National's semicustom-chip pact with customer Xerox Corp. This partnership [*Electronics*, Feb. 17, 1986, p. 64] has sparked the kind of user-maker relationship that is hard to find outside of vertically integrated Japanese giants, says Fred W. Horne, vice president of National's ASIC Division in Santa Clara, Calif.

CMOS standard cells designed by Xerox system architects have been placed in National's 2-μm cell library. National has sent chip designs to Xerox's in-house fabrication lines as part of the unusual alliance. The agreement allows Xerox to be its own second source in return for directing the majority of its business in ASICs to National.

National executives believe they have found a formula more successful than the traditional second-source agreements between competing chip suppliers, such as the deal between Intel Corp. and Texas Instruments Inc. National learned about the pitfalls of such joint ventures the hard way. Its 1982 comprehensive gate-array ASIC deal with Motorola, covering ECL, TTL, and CMOS, crumbled in just three years when National decided to limit itself to CMOS arrays and engineers from both companies found they couldn't work together.

"With the Xerox relationship, we have synthesized the vertically structured company," says Horne. "It happens naturally in the Mitsubishis, the Toshibas, and the Hitachis of Japan. It almost never happens in a Western company. We have taken a semiconductor company and stacked on top of it a systems company."

National has produced a number of semicustom circuits for Xerox in the past year. New design-automation software has been developed for the partnership. Tools have been adapted to various mainframes used by Xerox's Microelectronics Center in El Segundo, Calif. Small- and medium-scale integrated functions defined by the center have joined National's library—some for use exclusively in Xerox products. And large-scale integrated blocks are now being readied for use in the partnership, says Horne, who adds that the cooperation has broadened beyond ASIC products to include standard products.

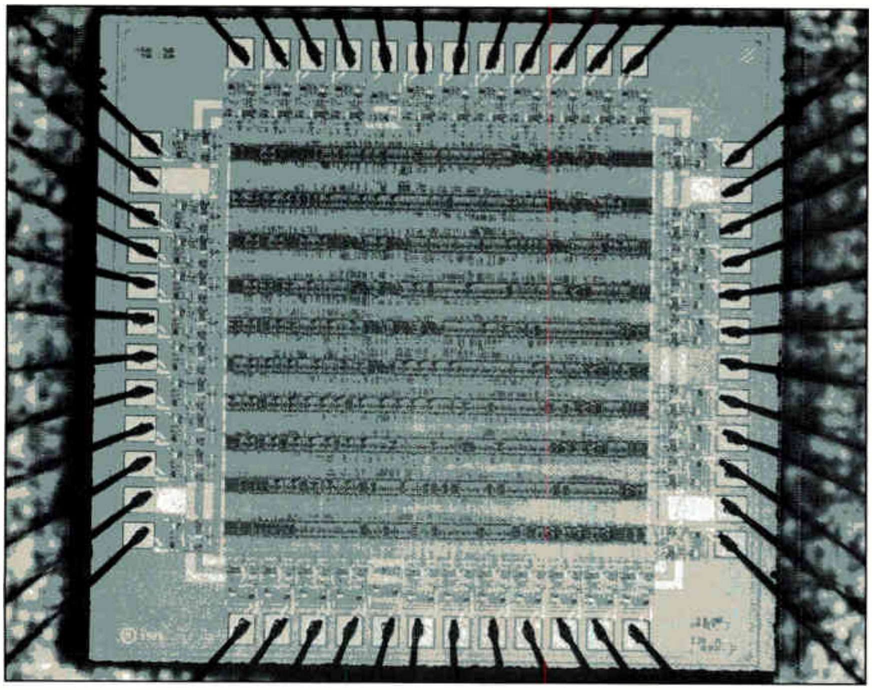


CAN THEY STAY IN STEP? That's the question for Charles E. Sporck, left, National's president and CEO, and James C. Vesely, vice president of Xerox's Microelectronics Division.

To some, such alliances are the wave of the future. Chip makers will have to follow National's example to make their ASIC business grow, says Dean A. Winkelmann, market research analyst at Integrated Circuit Engineering Corp. in Scottsdale, Ariz. He estimates that National's ASIC sales last year totaled $24 million in gate arrays and $2 million in standard cells. If $40 million in programmable logic devices is included—not everyone considers them ASICs—National now would rank ninth in the world overall.

The relationship has worked so well that National is planning similar customer ASIC accords in the future. "We are fairly far down the road in discussions with other companies," Horne says.

National first ventured into the emerging ASIC markets nearly five years ago, offering its first CMOS and bipolar gate arrays in a defensive move aimed at protecting its share of solid-state logic revenues. In 1983, it created its first ma-



STANDARD. National's SCL standard-cell family now includes more than 150 logic functions.

jor new product division in 15 years—known then as Customer Specific Products—folding in gate arrays and a group of handcrafted custom-IC services. It beefed up its standard-cell efforts under a contract with International Microelectronic Products Inc. in San Jose, Calif.

When Horne took over in 1985, he concluded that National needed to phase out its bipolar arrays and stop courting full-custom business in order to do a better job on CMOS arrays and standard cells. Today, National has shrunk the original 3-μm double-level-metal CMOS for standard cells and logic arrays down to 2 μm. A compatible 1.5-μm series of CMOS gate arrays will be introduced in the next several months.

National plans to add its first microcontroller core and analog circuits to its standard-cell library by fall. Other VLSI functions will be introduced in the next six months, including networking blocks and peripheral controllers for processors and memory blocks, such as electrically erasable programmable read-only memories.

Not that creating the ASIC strategy was easy. "One of the difficulties that any large semiconductor player had—whether we realized it at the time or not—was the struggle of integrating this thing called ASIC into the company's fabric," says Horne. "If you decide to be opportunistic and pounce on it for the moment, hanging it on your corporate shell, [the ASIC effort] is likely to fall off in the first windstorm. That happened to quite a few people."

Horne believes that many chip customers have had an equally difficult time understanding the difference between buying ASICs and commodity chips. Customers are still trying to play semicustom houses against each other for a lower price, he says. And that often results in production delays, causing buyers to cross off some ASIC vendors.

As customers trim down their vendor lists, Horne believes, the big silicon houses carry a decisive advantage because of name recognition and past business dealings. Horne says National, Motorola, and Texas Instruments Inc. have all faced up to the task of integrating ASICs into their corporate fabric, and he views them as the "dominant players three to five years out."

"I think it is inevitable," he adds, citing huge resources for research and development, standard product portfolios to draw upon, and a new sense of process synergy at the large chip houses. National, like other commodity-based giants, has directed its standard-product designers to use a common CMOS process so that circuits can be quickly incorporated into its standard-cell library. The standard-product design teams have also been told to load behavior models and test vectors into the ASIC data base.

"It is a fundamental part of our fabric and design flow to consider any new VLSI product as a megacell in our library. It's the closest we've been able to get in this company to working together since three days after we started," he adds with a smile.

–J. Robert Lineback

FUJITSU'S PROBLEM IS HOW TO STAY ON TOP

When you're No. 1, there's no place to go but down. Just ask Fujitsu Ltd. The Japanese company stands as the premier ASIC supplier in the world, but competitors are increasingly cutting into its market share.

Market analysts believe the root of the problem is that the Kawasaki company's biggest strength is also its greatest weakness: sales in the U. S., where the major ASIC action lies, are mostly to Amdahl Corp., the U. S. computer maker of which it owns 47%, and a small number of large companies, so that it is not as visible as some of its competitors. In Japan, on the other hand, the opposite is the case. Fujitsu has a broad customer base, with some users ordering only one or two designs a year. In addition, it sells to its own divisions. The result is that market share is slipping even as its sales increase, while both NEC Corp. and Toshiba Corp. gain.

There are two big reasons for

the success Fujitsu has enjoyed. First, it got into the game early with Amdahl, making ECL gate arrays customized for each company's computers and also assembling them into computers for the Sunnyvale, Calif., company. Then, in 1977, it jumped into the market with TTL gate arrays. "We have secured the trust of customers by being pioneers," says Hirofumi Takeda, manager of the ASIC engineering-support department. Second, Fujitsu is comfortable with ASIC-style marketing arrangements because it started as a captive manufacturer for itself and Amdahl.

Fujitsu's strength is also its greatest weakness: sales go to a handful of large U.S. companies; hence it's not visible

The Amdahl influence has gone beyond mere sales: because Fujitsu had to make leading-edge gate arrays for the U. S. company, it was able to take a more aggressive technical position with its own M series computers.

The entire Fujitsu product line is made in Japan, with manufacturing organized so that turnaround time is fast (now, says Takeda, it's three weeks for gate arrays). Preproduction work is done in Kawasaki; and the main production center for both CMOS and bipolar ASICs is in Aizu Wakamatsu, along with a third fab line that functions as a second source.

The administrative arrangement is kept simple. Until June, everything was done by ASIC Design Departments in the MOS and Bipolar Divisions at Kawasaki, while ASIC Engineering Support tied things together. Now, each division is looking after its own ASIC operations, and Takeda is being reassigned to develop new bipolar ASIC designs.

Now Fujitsu must move to retain its market-leading position in gate arrays. "The reason NEC and Toshiba are gaining is that they've greatly improved their software, particularly their emulation systems, which means they can serve their customers better at a lower cost," says Alan Bell, vice president at the investment house Salomon Bros. Asia Ltd. in Tokyo. "Toshiba in particular surely has learned a lot from its association with LSI Logic Inc.," with which it has an agreement covering gate-array design and fabrication.

Another market observer believes that Fujitsu need not worry too much at present. "It's gate arrays that count, and Fujitsu has about 20% of the world market," says securities analyst Sharil Osgood of James Capel & Co. in San Francisco. "I don't see NEC, with 14% of the array market, or Toshiba, with 10%, catching up in the foreseeable future—that is, the early 1990s," she adds. "Although NEC is making progress, it is more likely that it will first overtake suppliers like LSI Logic."

Against that background, Fujitsu is doing well. Last year, ASICs accounted for about 30% of the $1.25 billion it racked up in semiconductor sales. This year, dollar volume is expected to go up by 30% to 40%, and the number of devices sold by 70% to 80%. Overseas sales represent about a quarter of the total. Those numbers are especially impressive considering that Fujitsu ranks no better than fourth in total semiconductor production in Japan, and that the $11.4 billion company won't make money in semiconductors this year for the third year in a row.

A linchpin of Fujitsu's strategy to maintain its lead is to play the time-honored trump card of ASIC houses: customer support. The company has design centers around the world, including five in the U. S.—in Atlanta, Boston, Dallas, and Newport Beach and Santa Clara, Calif.—three in Europe, and three of its own in Japan, plus five more under contract. "The design centers are part of our plan to make it easier for our customers to access Fujitsu," says Takeda.

The company also provides necessary design tools, supporting Viewcad, the ASIC-design version of its 16-bit personal computer, as well as engineering work stations from Daisy, Mentor, and Nippon Data General. Customers will soon also be able to use Digital Equipment Corp.'s VAX line, plus Hewlett-Packard and Tektronix machines.

Backing up the effort is the Fujitsu product line: 70 series of gate arrays, 3 lines of standard cells, 3 series of analog designs and 4- and 8-bit versions of its flexible microcontroller.

Takeda says Fujitsu's best-selling ASIC is its AV series CMOS gate array with 350 to 8,000 gates and a propagation time of 1.4 ns per gate. By the end of 1987, and early 1988, the UHB series will debut. It will feature chips fabricated with a 1.5-μm process having 330 to 12,000 gates, and a propagation time of 0.9 ns per gate.

Following that will be the AUH line of devices, with its features reduced to 1.3 μm and a propagation time of 0.7 ns per gate. Also coming are new sea-of-gates products, which are needed for circuits of more than 20,000 gates, and more products with built-in RAMs, ROMs, and electrically erasable ROMs.

–Charles L. Cohen

TAKEDA: "We are pioneers." But for Fujitsu, one of the key strategies in the battle to stay on top and in front of NEC and Toshiba is to offer even better service to its customers.

ASIC HOUSES REVISE THEIR STRATEGIES

As the big chip makers swagger into semicustom, ASIC houses go for VLSI density, customizable standard ICs, and niche expertise

by Bernard C. Cole

Many of the smaller companies born and bred in the semicustom business are taking very seriously the arrival of the big standard-product semiconductor houses, who are now entering the booming ASIC business in a big way. But some of these pioneering ASIC companies are still highly skeptical about the semicustom efforts of the big standard-chip companies.

The big companies have big resources, however, and they are deadly serious about making it big in the ASIC market (see p. 60). And those ASIC houses that expect the big guys to gain some degree of success in ASICs are now looking around for new worlds to conquer and new ways to keep ahead of this potentially powerhouse competition.

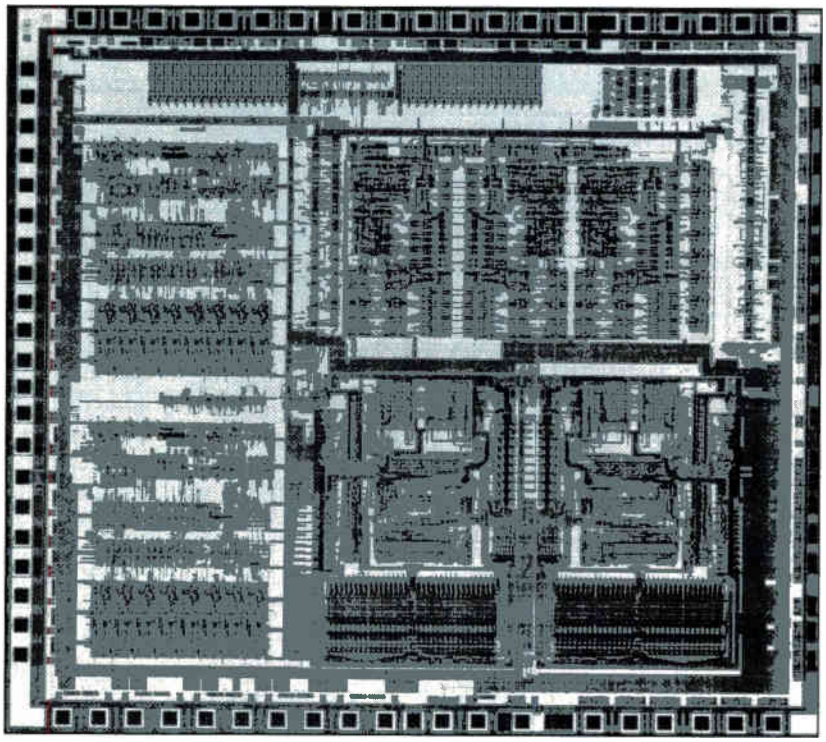
The main focus of the recent gate-array offerings from the big standard-IC houses has been to protect their market share in standard logic at the small-, medium-, and large-scale-integration levels, says Robert Walker, vice president and chief engineering officer at LSI Logic Corp., Milpitas, Calif. This market has growth potential, but the environment is already very competitive, he says—an environment that must be shared with as many as 100 firms, including the mainstream U. S. and Japanese semiconductor manufacturers. "It is turning into a real bloodbath in gate arrays, with prices dropping—especially at the low end of the density spectrum, below 15,000 gates."

As a result, many custom and semicustom firms, such as Cirrus Logic, LSI Logic, and VLSI Technology Inc., are moving to the less crowded high-density end of the market—for parts with from 50,000 to 200,000 gates. Their targets are VLSI functions—such as proprietary processor and graphics architectures, high-performance processor peripherals, and systems consolidation with all-in-one systems solutions—using advanced compiler-based design-automation systems and applications expertise as the means of differentiating themselves from their competition.

To address this market, new ASIC alternatives are emerging. They are known variously as semistandard ICs, value-added semicustom, and customizable standard ICs. All of them are standard-chip offerings that the vendor is willing to customize for the particular requirements of individual customers.

Another survival strategy for ASIC houses is to develop application, circuit-design, and process expertise in niches that are less prone to cutthroat competition. A number of companies are specializing in chips that mix digital and analog circuitry, for example. A few offer the cachet of electrically erasable programmable read-only memory in standard-cell libraries. Others have hitched their wagons to less common process technologies, such as biCMOS.

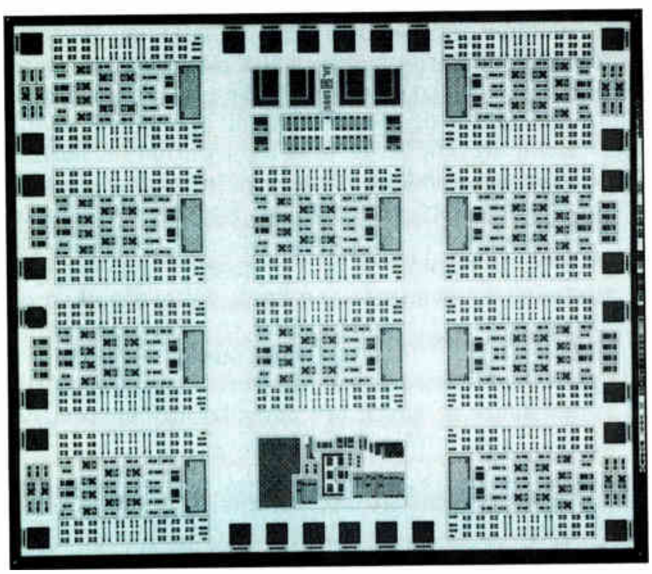
Some companies in the ASIC business, such as Gould Inc.'s Semiconductor division in Santa Clara, Calif., are extremely doubtful about the efforts of the big companies. The large IC houses will find it hard if not impossible to adapt to the ASIC environment, with its close customer relationships and high levels of service, says Peter Richmond, director of strategic marketing at Gould. "It is a matter of mind-set and institutional momentum," he says. "When you have spent years operating according to a certain set of rules, it is difficult to transform yourself—let alone a company—and operate according to a totally new set of rules, many of which are diametrically opposed to what you have always been taught."



1. SEMISTANDARD. Users can modify VLSI Technology's VL82C100 PC chip with tools.

But there are many important players in the ASIC business who are taking the challenge of the big semiconductor houses much more seriously. These companies have been working for some time to develop strategies that will allow them to survive despite the new giants moving in. The semicustom houses will succeed to the degree that they can come up with strategies that play off their traditional strengths while allowing them to differentiate themselves from the new competitors in terms of circuit, process, application, or design-automation expertise, says Andrew Haines, director of strategic marketing at VLSI Technology Inc., San Jose, Calif.

The VLSI end of the market—50,000 gates and above—holds major opportunities for companies that can develop appropriate strategies and technologies. VLSI has been the exclusive domain of traditional semiconductor houses, with their standard solutions. But many executives, including Michael Hackworth, president of Cirrus Logic Inc., Milpitas, Calif., view this segment as the one offering the most opportunities for future growth. According to Haines of VLSI Technology Inc., the single-chip VLSI and high-performance sector of the ASIC market can be expected to grow dramatically, from about 35% of the market today to about 65% of the market by 1990.



2. LINEAR NICHE. Micro Linear specializes in ASICs with linear circuits, such as this FB300 bipolar tile-array master slice.

Complicating the situation, says Haines, are long-term trends indicating that the main thrust of many low- to medium-density gate arrays and standard-cell offerings—glue-logic consolidation and replacement—is aimed at a market that is expected to decline from 60% to 65% of the worldwide ASIC total in 1986 to no more than 30% to 35% in 1990.

It is not surprising, then, that a number of ASIC specialists are concentrating on the advantages of semicustom technologies tailored to the VLSI density spectrum. They recognize, on the one hand, that standard products are a reliable and cost-effective means of achieving higher levels of integration. But systems made with standard parts begin to look as if they all come from the same mold, says Hackworth. "It is extremely difficult to differentiate a system product when the competition is designing in the identical VLSI circuits," he says.

While gate arrays and standard cells have provided the system designer with some degree of product differentiation, he continues, they have done little to replace the main ingredients in any system: the standard VLSI parts. "Most engineers use semicustom ICs to replace glue logic around the standard ICs."

The first steps toward combining the advantages of standard and semicustom methodologies are the megacell and macrocell approaches now coming into widespread use. Making catalog LSI and VLSI standard products available as a library of core cells allows the designer to put together semicustom ICs with a large portion of vendor-supplied applications expertise, says Robert Andrews, director of technical marketing at Zymos Corp., Sunnyvale, Calif. "But the megacell approach generally limits customization to additional logic around the core cell," notes Hackworth. "The design engineer does not generally have the ability to customize the function of the core cell itself."

To address this shortcoming, companies such as Cirrus Logic, LSI Logic, and VLSI Technology Inc. are turning to advanced design-automation systems built around silicon-compilation methodologies. Semistandard ICs built with silicon compilers provide complete architectural solutions for particular systems, says Haines of VLSI Technology. In some cases, semistandard functions can even be offered as off-the-shelf standard products.

"But what makes these circuits especially useful is that the implementations can be modified for the unique requirements of different applications," says Hackworth. "Thus the standard product becomes the starting point for a customized version, a semistandard product. In some cases it may be quite appropriate to purchase an off-the-shelf implementation of the vendor's architecture in semistandard form, for quickest development and time to market, while the ability to further customize the design remains a means of proliferating a family from the original product, or extending the life of the original product with unique functional and performance additions as new competitors enter the market."

Critical to making the compiler-based semistandard approach work is the vendors' insight into systems issues, says LSI Logic's Walker. In fact, adds Hackworth, "the level of systems and applications expertise in a semistandard vendor must reach far beyond that of a semicustom vendor. The semicustom vendor is only responsible for developing a part that functions according to specifications provided by the customer. The semistandard vendor, on the other hand, is responsible for a part that meets the system requirements."

For this reason it is important that vendors of semistandard circuits choose the markets they enter even more carefully than the traditional semicustom vendor does, says Walker. "Quite obviously, one does not attempt to go head-to-head with a standard IC company where it is strongest, where it has already established market share and has economies of scale going for it. Rather, what one looks for is niches in the market where the value-added architectural approach offers market advantages."

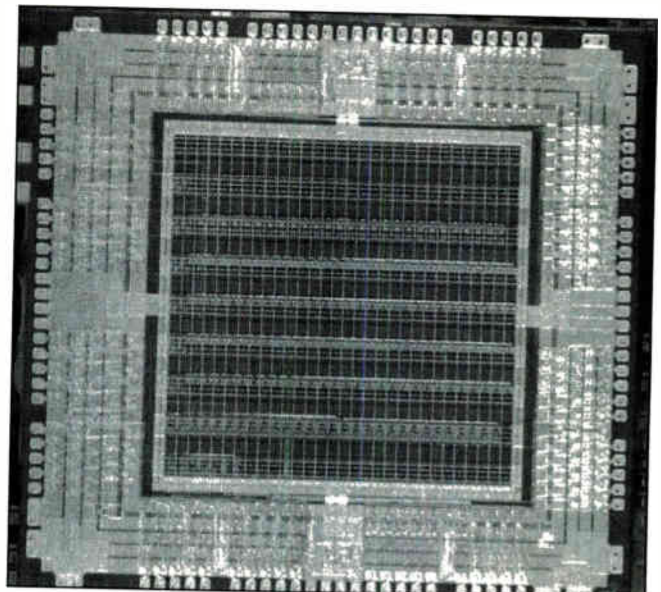
For example, Cirrus Logic is focusing on high-performance microprocessor-peripheral circuits for data communications, disk controllers, and graphics applications designed with its proprietary storage/logic-array compiler [*Electronics*, Jan. 20, 1986, p. 29], Hackworth says. One of the first applications of the semistandard approach using the company's S/LA technology is a Winchester-disk-controller chip set: a buffer storage manager and a disk formatter.

Offered as off-the-shelf components, the functions of the two devices can be customized and reconfigured to give the systems designer a high degree of product differentiation, says Hackworth. For example, with the compiler the two functions can be integrated onto a single chip, or the on-chip error-correction-code circuitry can be expanded. Also, the bus interface can be modified for direct connection to a specific printed-circuit-board bus. Special logic can be added to count sectors, and the on-chip writable-control-store memory can be expanded. The processor interface can be modified, as can the direct-memory-access scheme. Because it relies on a proprietary compiler technology, Cirrus' ability to modify the design is not restricted by a library of predesigned cells, nor is there any prohibition against reaching deep into the heart of the design to make fundamental changes.

LSI Logic is another important player that has entered the semistandard market in part through the use of compiler technology, with its cell-compiler-based Modular Design Environment [*Electronics*, May 14, 1987, p. 67]. The company is offering a variety of VLSI-level products as stand-alone devices or as megacells or megafunctions for larger customized designs. Among them are a two-chip processor that implements the MIL-STD-1750A military instruction set; 16- and 32-bit multipliers and multiplier-accumulators; a 32-bit floating-point processor; and a family of video image-processing circuits.

VLSI Technology Inc. has been quietly developing silicon-compiler technology for a number of years and is now joining the semistandard club along with Cirrus and LSI Logic. It has a family of proprietary data-path, state-machine, and full-chip compilers [*Electronics*, Feb. 7, 1987, p. 62]. Using these and other advanced tools, the company is moving into production with the first in a projected series of semistandard products. The initial effort in this area is a five-chip set that reduces the chip count on the motherboard of an IBM Corp. PC AT-compatible computer from 110 to 16 [*Electronics*, June 11, 1987, p. 81]. For example, the VL82C100 replaces two direct-memory-access controllers, two interrupt controllers, a programmable counter, a memory-mapping IC, two octal latches, and a 3-to-8 decoder, among other circuits (see fig. 1). The company is leveraging its expertise in cell-based compiler technology, says Haines, by offering original-equipment manufacturers its existing cell library and design tools so that users can provide unique features and special functions for their markets.

Zymos is another company with an evolving semistandard strategy, but silicon-compiler technology is not yet part of the picture there. Zymos offers the Poach AT, a two-chip set that integrates more than 50% of the logic on the PC AT motherboard. But to give customers access to the random-logic portion of the two chips, Zymos offers not compilers but a custom tool kit that consists of a motherboard, a daughterboard that plugs into the Poach chip sockets on the motherboard, and two emulator boards. The emulator boards are hardware emulations of the two chips, with board space for wire-wrap modeling of intended modifications. "We take the wire-wrap version and modified schematics and apply the same expertise we use to design our custom products in implementing the customer's design," says Andrews. "We also run full simulations on our in-house computer system, autoroute the design, and run post-route simulations before producing the first prototype."



3. BiCMOS ARRAY. Applied Micro Circuits expects price competition to be less fierce in ASICs made with biCMOS, such as this fast gate array.

A number of other ASIC houses are basing their survival strategies on specialized capabilities, such as combined analog and digital design, the ability to add EEPROM to an ASIC, and less common process technologies. Micro Linear Corp., in fact, combines its expertise in linear and mixed analog and digital applications with a semistandard strategy.

The San Jose company offers a linear CMOS standard-cell family, the SCM2000, and the FB300 linear bipolar tile-array family (see fig. 2). But it also uses them to build standard parts, such as a family of servo-demodulator products for disk drives. "On two counts, the semistandard approach is particularly valuable in the linear market," says Charles Gopin, vice president of marketing. "On the design side, linear circuitry is much more touchy than digital devices and usually requires several iterations to get it right. Fabricating such circuits using cells or tiles speeds up the design process. On the customer side, such tile- or cell-based semistandard designs allow us to offer a product at a much lower cost than the traditional semicustom approach. Moreover, when and if the customer wants a modification to be made, this is much more easily done."

Exar Corp., of Sunnyvale, is also marketing its expertise in combining analog and digital on one chip, although it is not yet explicitly working on a semistandard approach. In addition to its existing bipolar master-slice and linear arrays, Exar is moving into production with a 2-μm CMOS standard-cell family, the N2000. In addition to digital functions, the N2000 family incorporates many of Exar's standard linear products, such as telephone line drivers and receivers, voltage-controlled oscillators, phase-locked loops, and filters.

To add flexibility to its offering and to gain entry to a few more applications niches, Exar has added EEPROM cells to its library. "What EEPROMs allow is the development of a design that is less application-specific," says product marketing manager Jim Nickerson. "In effect, it means that rather than develop a number of different designs that are specific to particular needs, a customer can implement a more generalized design and use the EEPROM cells to customize the devices." Other companies that have followed similar strategies include WaferScale Integration, Fremont, Calif.; Sierra Semiconductor, Sunnyvale, [*Electronics*, March 17, 1987, p. 30]; and International Microelectronic Products, San Jose.

Another ASIC tactic is to add a number of specialized process capabilities through pacts with other semiconductor companies, and International Microelectronic Products Corp. is doing just that. For example, International CMOS Technology Inc., of Santa Clara, is the source of IMP's EEPROM capability; IMP got its high-voltage CMOS capability from Ixys Corp., San Jose, and its one-time-programmable capability from Zoran Corp., of Santa Clara. Furthermore, IMP is itself developing an advanced 1.2-μm CMOS mixed linear and digital cell library aimed at digital signal processing.

Another company that seeks to compete through specialized process technology is Applied Micro Circuits Corp. The San Diego company is moving to expand its product line beyond its existing emitter-coupled-logic and CMOS gate arrays to establish a niche in the much less crowded biCMOS arena (see fig. 3). The first offerings in its high-performance Q12000 biCMOS family are arrays of 2,100 and 9,072 equivalent gates with internal flip-flop toggle frequencies of 240 MHz. □

SYSTEM-SIMULATION TOOLS SPEED ASICs INTO PRODUCTION

Despite the claim of first-time working silicon by ASIC foundries, quite a few ASIC chips do not work the first time in the application for which they were designed. Only about 50% of ASIC designs go into production after first silicon, says Michael Turner, director of marketing at Logic Automation Inc. in Beaverton, Ore. But there's an answer to this problem: simulation tools that let a designer simulate the working of an ASIC design in its final system environment—well before first silicon.

ASIC tool suppliers—and some foundries—are moving to address the problem by offering simulators that allow the designer to simulate the entire system in which the chip will operate. In this way, the designer can determine whether an ASIC design will operate in that system. LSI Logic Inc. of San Jose, Calif., for example, already offers its multichip simulator, MSIM [*Electronics*, May 15, 1987, p. 67]. The company claims a first-time successful-completion rate of nearly 100%.

SMOS Systems Inc., too, has been performing multichip simulations for several years now with a small number of off-the-shelf LSI and VLSI devices, says John Conover, director of engineering at the San Jose company. "In a typical system comprising, say, a Z80 and a couple of ASICs, the ASICs could all be simulated at the gate level," he explains.

Simulators can use both gate-level simulation and behavioral models, but gate-level simulation is time-consuming. "Behavioral models run two orders of magnitude faster than gate models," explains Matthew Goldstein, vice president of engineering at Quadtree Corp. in Bridgewater, N. J. Also, in some cases, where a system simulation using gate-level models might require a mainframe or accelerator to execute, a simulation with behavioral models runs on a work station.

Quadtree plans to have 1,000 behavioral models in its library by October. The company thinks it can achieve this ambitious goal thanks in part to a tool called the code-generation system, which speeds up the generation of behavioral models. Goldstein says the company will release the tool as a product by the fourth quarter of the year. With it, he says, a designer can develop a behavioral model of an ASIC in less than 10 days. Another approach is to break the ASIC into its component parts and use existing behavioral models of these parts—but that makes for a slower simulation.

Some foundries have been providing some system-level multichip simulation capability, but it is not a pervasive practice, because libraries of behavioral models for LSI and VLSI devices are not available. Logic Automation and Quadtree, which are both vendors of behavioral models, have made their libraries compatible with popular simulators such as Hilo from GenRad Inc. of Concord, Mass. And now they are beginning to adapt their model libraries to proprietary simulators used by ASIC foundries. "We have signed agreements with both Logic Automation and Quadtree to provide their models of off-the-shelf LSI and VLSI devices in our design-system environment," says Van Lewing, LSI Logic's director of software marketing.

Logic Automation has also announced that it will convert its SmartModel line of models to run on the Lasar simulators from Teradyne Inc. of Boston. And Logic Automation and Mentor Graphics Corp., of Beaverton, have signed a technology-exchange agreement that in part calls for converting the SmartModel line for use in the Mentor design-tool environment.

–Jonah McLeod

SOME BIG USERS AIM TO BE BIG SELLERS

These systems companies want to sell their ASIC technology, and they have the expertise and financial backing to be tough competitors

by Tobias Naegele

Some of the biggest consumers of ASICs are striving to become some of the biggest producers and marketers of the technology as well. Having already invested hundreds of millions of dollars to develop in-house design and process capabilities, several large systems houses are trying to leverage their investments by selling ASIC technology.

Whether their business is in computers, industrial control, avionics, or telecommunications, these companies were among the first to recognize the inherent advantages of using custom and semicustom chips to make their products unique. Unable to buy that technology elsewhere, they built up ASIC expertise—and now they are swooping into the commercial market.

Whether their strategy is based on standard cells or gate arrays, in-house designs or licensed technology (see table), what these companies all have in common is excess capacity, a marketable expertise, and the kind of financial backing that makes them look like pretty tough competition. Summing up what is essentially a universal philosophy among these several competitors, Gene Patterson, director of NCR Corp.'s semicustom business unit, emphasizes the advantages of a vertically integrated company. "We focus on the overall business," he says. "We do not make exorbitant sums of money on design services. We make money in the overall program."

ASICs will make up half the total logic market by 1991, estimates Martin Geller, director of marketing at Raytheon Co.'s Semiconductor Division in Mountain View, Calif., a gate-array vendor. He admits that gate arrays will gradually lose market share to standard cells, but he says his CMOS and ECL parts will still find favor because they can be produced more quickly and, when they are not needed in volume, at a lower price than standard-cell designs.

Honeywell's ASIC strategy also focuses on gate arrays. The company's CMOS gate-array technology, in fact, is an outgrowth of its involvement in the Defense Department's Very High Speed Integrated Circuits program.

SYSTEMS HOUSES MARKETING THEIR IN-HOUSE ASIC EXPERTISE

Company	Year entered ASIC market	Technologies offered
AT&T	1984	1.5-μm bipolar gate arrays, 1.25-μm CMOS standard cells, bipolar and CMOS full-custom
Harris Corp.	1982	1.5-μm CMOS standard cells
Honeywell Inc.	1983	1.25- and 2.5-μm bipolar gate arrays, 1.2-μm CMOS gate arrays
NCR Corp.	1982	2-μm CMOS gate arrays and standard cells
Raytheon Co.	1974	1.25-μm CMOS gate arrays

SOURCE: *ELECTRONICS*

Like other systems companies entering the ASIC field, Honeywell is seeking large customers in the defense, aerospace, and computer businesses. Smaller ASIC companies tend to look for numerous customers with a large volume of small jobs, but these vertically integrated systems makers seem more interested in stability—they are accustomed to dealing on a long-term basis with their internal customers and seek similar arrangements on the outside. Honeywell's typical accounts, such as one with ETA Systems, the Minneapolis supercomputer maker, are worth about $5 million a year.

AT&T has "a half dozen" such customers, including one unnamed European partner for whom it has produced 15 designs in three years, says A. Edward Walker, ASIC product manager for AT&T Co.'s Components and Electronic Systems Division. About 90% of AT&T's ASIC business is in digital CMOS standard-cell designs, he says, with the remainder split between full-custom designs and linear and digital gate arrays.

Another standard-cell vendor is Harris Corp.'s Semiconductor Products Division, in Melbourne, Fla. Harris offers a collection of macrocells to complement its large library of primitives, including core cells based on Intel Corp.'s 8086 and 8088 microprocessors.

Harris recently introduced a family of standard parts integrating the Forth programming language with a reduced-instruction-set architecture built around a 16-bit core microprocessor licensed from Novix Inc., of Cupertino, Calif. It plans to offer ASIC versions in 1988.

NCR Corp.'s Microelectronics Division, in Fort Collins, Colo., is following a similar strategy, drawing on the strengths of partners to expand its presence in the ASIC market. Last year the division branched out with a second-source agreement with Motorola Inc. in which it traded access to its 2-μm cell library for Motorola's gate arrays. NCR also has a 1.5-μm CMOS library in beta test.

The Motorola deal has opened up a whole new world for NCR. "Motorola is a commodity supplier with access to almost every customer in the world," Patterson says. "We pick up business as a second source, [and get] access to customers that we would not normally get." □

NEC's BiCMOS ARRAYS SHATTER RECORD

The company packs 10,348 gates on a single chip; more complex circuits can now go on a single biCMOS chip, avoiding interchip delays

by Charles L. Cohen

BiCMOS has got plenty of people excited. A growing number of designers believe that once mixed bipolar and CMOS circuits are combined routinely into VLSI chips, biCMOS will emerge as a mainstream process that will be used to build a wide array of products. Because such circuits are now hard to build, progress has been slow going. Most of the action to date has been in Japan, though Motorola Inc. brought home the cup a year ago [*Electronics*, July 10, 1986, p. 67] when it announced the biggest biCMOS array, a 6,000-gate device.

Now NEC Corp. in Tokyo has jumped out in front by developing the two largest biCMOS gate arrays yet, one at 6,372 gates and the other at 10,348 gates. The big circuits promise systems designers the ability to escalate circuit complexity while retaining the speed and power benefits of biCMOS. The NEC arrays feature high speed, high drive, and freedom from latchup; both the μPD67060 and μPD67100 more than double NEC's previous limit of 3,140 gates for biCMOS arrays.

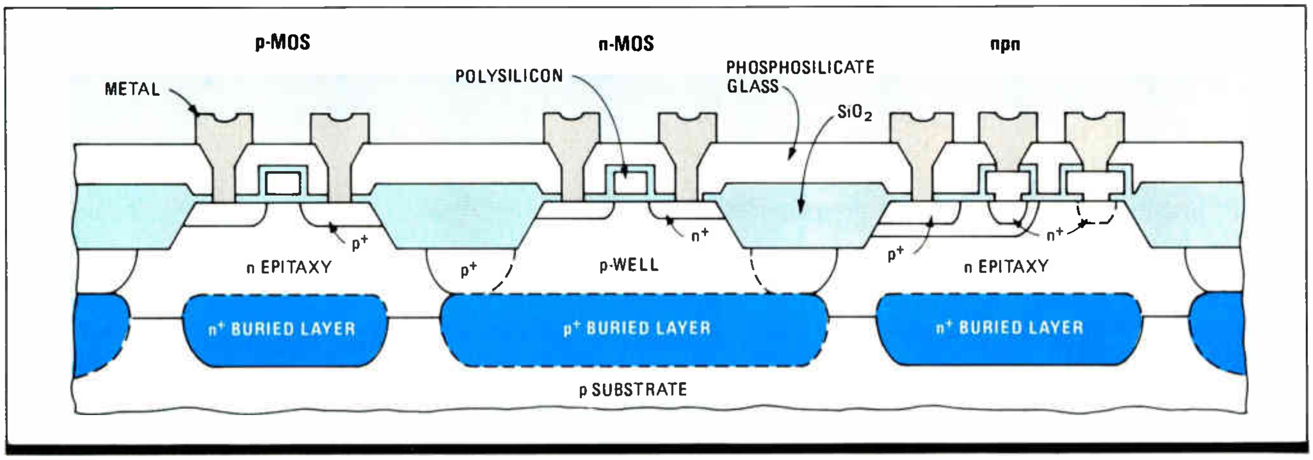
NEC's ability to leap from 3,000 to 10,000 gates springs from advances it has made in processing technology that keep the size of the chip down. The processing steps include shrinking the interconnection wiring pitch and the use of some nonactive cell areas. Also helping to compress the chip are a simplified logic circuit and a clever current-booster design.

By enabling designers to put more complex circuits on a single chip, the new chips can speed things by eliminating interchip delays. With the earlier 3,000-gate biCMOS part, it's possible to build an error-correction-code circuit that operates to clock frequencies of 20 MHz for 16-bit processors. A 32-bit error-correction-code circuit designed with 3,000-gate parts will operate only to 10 MHz. That's because the smaller the arrays used in a system, the slower overall speeds will be, as a result of time delays in output and input buffers, and between chips on a printed-circuit board. Thus, for equivalent gate delays, the larger arrays provide the highest circuit speed for complex applications such as ECC circuits—those requiring larger gate counts.

With the 10,000-gate array, it's possible to build a 32-bit error-correction circuit with about 7,000 gates that runs at 20-MHz. Of course, ECCs are mostly combinational logic, but a complex circuit requiring flip-flops also would benefit from biCMOS's superior speed.

The larger NEC parts retain the key specs of the earlier arrays. Internal gate propagation delay is only 0.8 ns for a NAND gate with a fan-in of two and fan-out of three. External drivability and output levels match those of advanced low-power Schottky TTL, with 24-mA buffers standard and 48-mA buffers available. Propagation delay is only 3 ns when driving a 15-pF load, and 4.3 ns for a 50-pF load.

With the process it had used to build 3,000 gates into one chip, NEC couldn't deliver reasonably sized 6,000- and 10,000-gate arrays, so it had to shrink the pitch of its aluminum interconnections. It also shrank nonactive portions of the cell, such as the insulating regions between active devices. The MOS channel length and width were not altered. Size of the 6,000-gate array is 9.5 by 9.31 mm; the 10,000-gate part measures 11.68 by 11.47 mm. The 3,000-gate array made in the previous process is 7.6 by 7.32 mm. NEC is aiming at 20,000-gate arrays as its next step; this will require shrinking the design rules from 1.3 to 1



1. NO LATCHUP. The largest biCMOS gate array puts all transistors into a thin epitaxial layer, with both n+ and p+ buried layers, to ensure freedom from latchup—freedom so complete that NEC rates the arrays for live insertion and removal.

μm and speeding up the gates into ECL territory. It is also looking to design upcoming devices so that external I/O levels can be either TTL- or ECL-compatible.

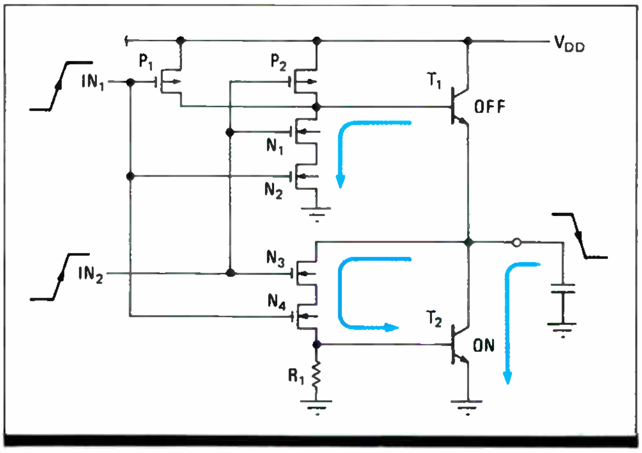
Processing of the large arrays considers future large-scale applications. Fabrication of all active elements in a thin epitaxial layer, with both n^+ and p^+ buried layers, provides complete freedom from latchup and enhances bipolar transistor performance (see fig. 1). NEC designers, confident of latchup avoidance, have rated the arrays for live circuit insertion and removal, says Kodo Kimura, manager of the Customized LSI Department, Application-Specific LSI Products Division, in Kawasaki.

The n-type epitaxial layer is kept to 1.5 μm to permit fine design rules—at the level of 256-Kbit memory—and thus high packing density. For high speed, CMOS devices have short channels, and bipolar devices shallow junctions. Effective channel lengths are 1.3 μm. Minimum bipolar transistor emitter size is 1.5 by 3 μm, while emitter and base junction depths are 0.15 and 0.3 μm, respectively. Bipolar-transistor cutoff frequency is 4 GHz.

Compared with NEC's earlier designs, wiring pitch of the first layer was reduced from 7 to 5.4 μm, and that for the second layer from 9 to 7 μm. These reductions permitted an increase in the number of wiring channels from 29 to 40 on the first layer, with the second layer remaining the same at 13, for increased interconnectivity. The reductions also allowed cell size to shrink from 117 by 188.5 μm to 91 by 216 μm. The width of the free channels between cells also decreased. Cell density rose from 45 to 51 per square millimeter. A redesign of the 3,000-gate using the new rules reduced that chip's size to 74.3% of the original design. Since the 3,000-gate does not need the interconnectivity, the number of first-layer wiring channels could be kept at 29. Consequently, the size of the new 3,000-gate chip shrank from 7.6 by 7.32 mm to 6.43 by 6.43 mm.

Circuit design is intentionally kept simple (see fig. 2). A two-input NAND gate requires only six MOS transistors, one resistor, and a two-transistor bipolar current booster. Chip area is kept down by a design that provides one current booster for each internal cell of two gates. Since during static conditions one of the two bipolar transistors in the current booster is always off—just as one of the two transistors in a CMOS pair is always off—no current flows when the gates are not switching.

The four MOS transistors in the upper half of the biCMOS cell have the same configuration as a standard CMOS NAND cell. When one input goes low, the output goes high and drives the upper npn transistor. All of the output current flows into the succeeding gates, which require negligible current once capacitances have been charged. The lower n-channel MOS transistors and npn transistor are off. When both inputs go high, the upper CMOS gate output goes low and the upper npn transistor is turned off. The lower npn transistor is biased on. If there is a positive voltage at the output terminal, it flows through the two lower n-channel transistors to drive the base of the lower npn transistor, and the output is pulled down.



2. KEEP IT SIMPLE. The internal two-input NAND gate requires only six MOS transistors. The bipolar pair forms a current booster.

For low standby current, the output-circuit driver operates as a biCMOS totem-pole inverter. Moreover, the use of a clever circuit configuration to clamp the output voltage at 0.5 V^f keeps the lower bipolar transistor out of saturation while eliminating the need for the Schottky barrier diode usually used for this purpose. V^f is the terminal voltage across a forward-biased emitter junction.

Key to the operation of the clamping circuit is a transistor connected to a voltage divider, providing half of V^f at the collector-to-base junction and V^f at the base-to-emitter junction. Kimura says that on a small- or medium-scale IC fabricated with a relatively short process, it would be simpler to add a mask and a Schottky barrier process than to add the clamping circuit. But because the process for fabricating the biCMOS part is already quite long, using the complex circuitry avoids the extra mask and keeps the process from becoming even longer.

20,000-gate arrays are the next goal, and NEC plans to make the external I/O levels of future parts either TTL- or ECL-compatible

The μPD67100 features up to 228 I/O pins; the μPD67060 up to 180. Both have power dissipation low enough to permit the use of plastic pin-grid-array packages. NEC will also offer ceramic PGA packages with 72 to 280 pins, plastic leadless chip carriers with 68 to 84 pins, and flatpacks with 120 to 160 pins.

NEC will start accepting orders for the new arrays in September. The development charges are about $45,600 for the 6,000-gate part and $56,600 for the 10,000-gate piece. Turnaround time is four weeks after customer approval of post-layout delay simulation. The price of the 6,000-gate devices in a 132-pin ceramic PGA is about $70 each when purchased in quantities of 1,000 per month. The 10,000-gate devices in the same package and in the same quantities will sell for about $106 each. □

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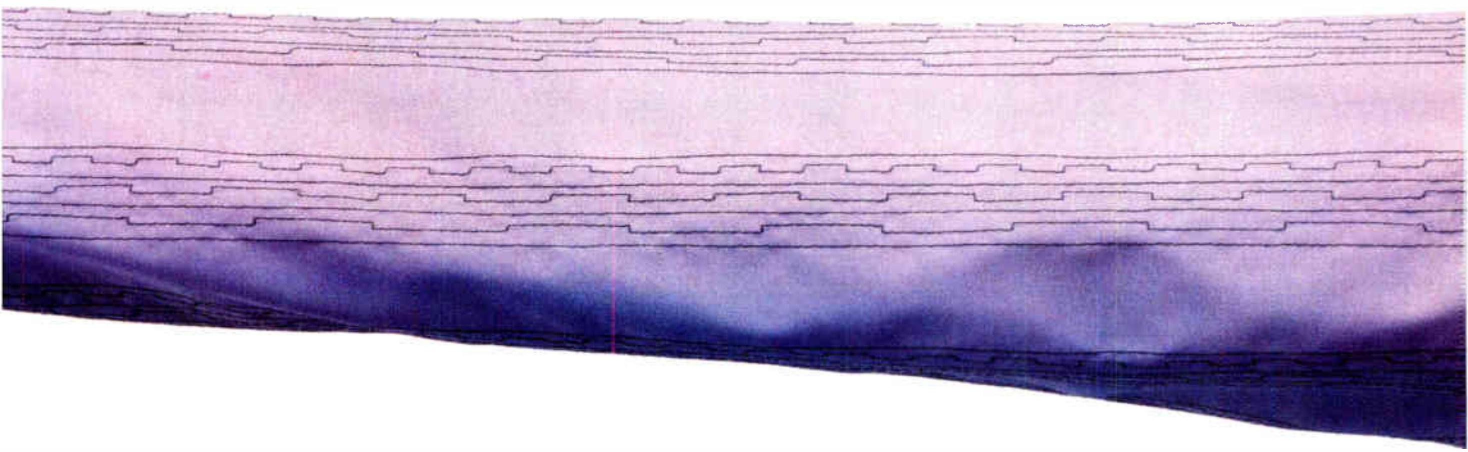

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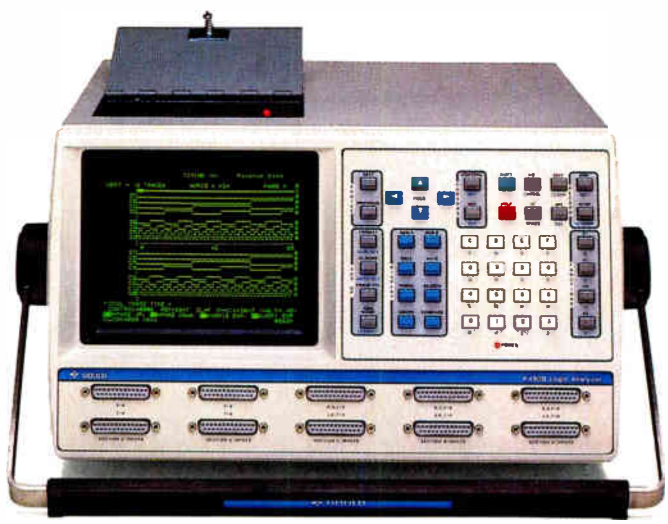

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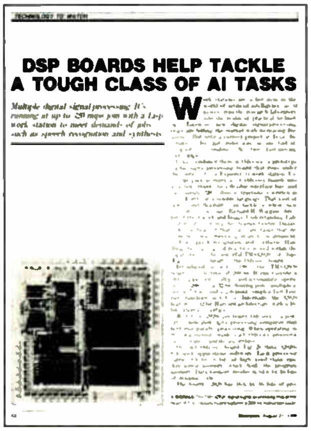
UPDATE: TI'S DSP BOARD PIERCES AI RESEARCH NICHE



Texas Instruments Inc.'s signal-processing board, Odyssey, has ventured quietly out of the computer lab and into artificial-intelligence research markets. "The market is currently a small niche of researchers and developers," says Guy Hogle, product marketing manager, "but we think it is a promising area of business."

Odyssey is a parallel signal-processing board computer that plugs into TI's Lisp-based Explorer work station, combining the power of symbolic AI-processing and real-time DSP [*Electronics*, Aug. 21, 1986, p. 64]. Odyssey contains four of TI's TMS32020 DSP chips, an 8-bit coder-decoder port, a 10-megabyte/s port for data acquisition, and a highly flexible interface to the Explorer's Nubus. The Nubus interface allows an Explorer to have up to 16 Odyssey boards, each executing up to 20 million instructions/s written in Lisp, Forth, or assembly language.

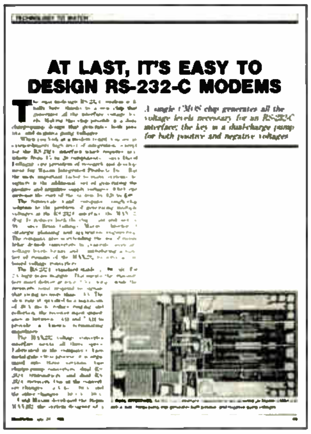
A prototype one year ago, Odyssey quietly hit the market early this year under the guidance of TI's Data Systems Group in Austin, Texas. TI officials report the board is receiving most of its early attention from labs researching and developing neural networks. Other promising applications appear to be in speech synthesis and recognition research, image understanding, and real-time DSP systems.

Odyssey sells at a suggested retail price of $12,500. The option kit includes software, comprising a TMS32020 assembler and linker for the Explorer; a multiprocessor window debugger; a Forth interrupter, which is downloaded from the work station to any of the 32020 chips; hardware diagnostics and drivers for application development; and a master control program for communications between the board and the host system's codec.

The power of Odyssey was recently demonstrated at July's American Association for Artificial Intelligence conference in Seattle, where TI workers attached two video cameras to the system and focused them on a goldfish swimming in a small tank. The Odyssey-equipped Explorer tracked the fish in three dimensions, displaying digital images on its screen. *–J. Robert Lineback*

TECHNOLOGY TO WATCH

UPDATE: MAXIM EXPANDS ITS SINGLE-VOLTAGE LINE



Introduced a year ago, the MAX232, the first single-voltage, RS-232-C interface chip, is now a "moderate success," according to its designers, Maxim Integrated Products Inc. of Sunnyvale, Calif. Declining to cite exact figures, Brian Gillings, Maxim's director of strategic planning and application engineering, says that on a scale of 1 to 10, the MAX232's sales performance rates between a 3 and a 4. Nevertheless, the company is expanding the product line to include 10 new devices.

The expansion is intended to counteract the plans of Intersil, of Sunnyvale, Calif., which recently announced a competitive product, the ICL232. In response, Maxim is adding to its own product family MAX230 through MAX239. Each is a variation of the MAX232, offering different features to serve various market niches. The MAX233, for example, has external capacitors mounted to its lead pins to save board space; the MAX230 comes with five transmitters and no receivers, for transmit-only operation.

The original MAX232 is a single CMOS chip that generates all the voltage levels necessary for an RS-232-C interface [*Electronics*, July 24, 1986, p. 89]. The chip contains two transmitters and two receivers, level shifters, and an oscillator—replacing 15 to 20 discrete components as a whole. More important, with its on-chip dual-charge pump, the MAX232 eliminates the $20 to $30 worth of circuitry needed to generate the positive and negative 5- and 15-V supply voltages required by the interface.

The MAX232 is aimed at a niche market where designers need to fit the function into a small physical space, Gillings says, or have access to only a single 5-V power supply. "There appears to be a trend toward single-supply designs," says Gillings. Designers, he points out, are migrating away from RS-232-C—which requires multiple voltage supplies—to newer RS-422 and RS-485 standards, which require a single positive and negative voltage, typically ±5 V.

Maxim admits its product is not a runaway success. But the new products, plus a one-year head-start, should ensure that the MAX232 will be far from a money-losing venture. *–Jonah McLeod*

MONOLITHIC MICROWAVE ICs MOVE INTO PRODUCTION AT TI

Automated large-scale manufacturing is starting up for upcoming military programs needing the superior performance that GaAs MMICs can provide over hybrids

Monolithic microwave integrated circuits based on gallium arsenide technology have long had the potential to do for military electronic systems what monolithic digital and linear ICs based on silicon have done for commercial systems. Now GaAs MMICs may be on the verge of realizing that potential, as Texas Instruments Inc. moves into automated large-scale production in order to increase yield and lower costs. A big impetus is advanced military programs now coming on stream that need the superior performance that MMICs offer over hybrids.

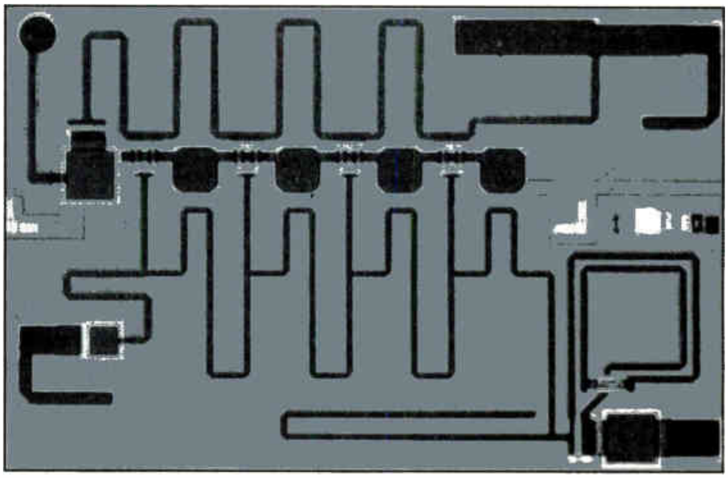
"In fact, for some applications with difficult-to-meet technical specifications, monolithic technology is the only method that can be used," says D. Gary Lerude, engineering manager of TI's Microwave Military Components Department in Dallas. "The classic hybrid techniques that have been predominant in the past are just not up to the job." This is because in MMICs all the matching elements are defined photolithographically, affording greater control and consistency in lead lengths and structural dimensions; in hybrids, leads are generally wire-bonded by hand. A microwave circuit at 18 GHz is extremely sensitive to variations of these elements, Lerude says.

As with any IC, MMICs can lower costs, by reducing the number of components and interconnections, compared with the equivalent hybrid assembly of, say, a typical amplifier. Another important key to lowering costs is designing the chips for automated production, and this is a major focus of the TI MMIC campaign—an example being the work done on the multiple broadband Lange couplers used in microwave amplifier design. TI is also easing the MMIC design effort with extensive computer-aided-design libraries. However, the MMIC technology throughout the microwave industry still has a way to go, Lerude says. More improvements in design, processing, packaging, and testing are necessary to achieve the goal of affordable MMICs, he notes.

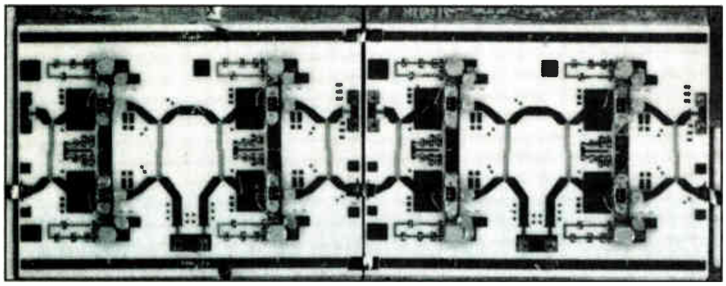
One TI goal is to develop a line of MMIC building blocks that can be used for multiple system applications in electronic warfare. The TGA8300, a 2-to-18-GHz distributed amplifier MMIC, is one of these building blocks (see fig. 1). Besides its 6.5-dB average gain and +18-dBm compression point, its input/output standing-wave ratio is less than 2:1, making it a useful amplifier in a variety of system architectures.

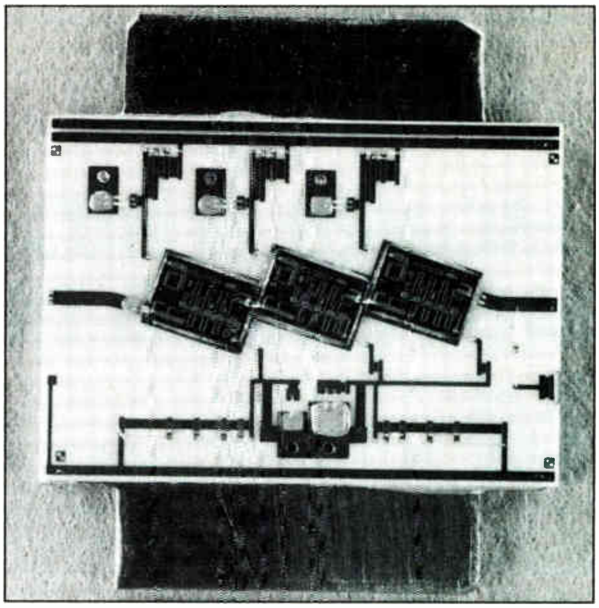
Another generic device, targeted for electronic-warfare applications in the 6- to 18-GHz region, is the TGA8014. It is the first medium-power amplifier available as a commercial GaAs MMIC. Previous commercial GaAs MMIC amplifiers have consisted of discrete GaAs FET circuits with 10 to 20 dBm output power. In contrast, the TGA8014 MMIC amplifier delivers an unheard-of 26 dBm (0.4 W) at 1-dB gain compression from 6 to 18.5 GHz. Outputs of these MMICs can be added with passive devices to achieve amplifiers with 1 W of output power.

Such amplifiers and other MMIC devices in the 6-to-18-GHz range and even wider bandwidths will appear in electronic-warfare applications such as phased-array jammers, expendable decoys, and shared apertures. For all of these applications, the production volumes of MMIC components will be several orders of magnitude above those of current hybrid components, and



1. BUILDING BLOCK. Consistency of operating characteristics suits the TGA8300 MMIC distributed amp to many electronic-warfare applications.





2. MMIC IS BETTER. A hybrid broadband amplifier (above) and an easier-to-produce MMIC (right) differ significantly in the number of components and interconnections (see table, below).

COMPARING HYBRID AND MONOLITHIC TECHNOLOGY

Component count	Hybrid	MMIC
Alumina substrates	2	1
Discrete GaAs FETs	8	0
GaAs MMICs	0	3
Chip capacitors	40	6
Total components	**50**	**10**
Interconnections		
Number requiring skilled manual labor	136	0
Number suited to automated equipment	106	44
Total interconnections	**242**	**44**

costs will be several orders of magnitude lower.

A comparison of comparable hybrid and monolithic amplifiers clearly illustrates the differences between the two. Both circuits have equivalent electrical performance, but the differences in complexity between the two are marked.

The hybrid implementation of a broadband, high-frequency GaAs FET amplifier (see fig. 2, top photograph) is representative of what is produced today by the microwave industry. It consists of four balanced amplifier stages achieving about 20 dB of gain. Discrete GaAs FETs are used for the active devices, and the matching circuits, Lange couplers (microstrip structures that combine or split power between ports while maintaining an impedance match), and thin-film bias resistors are fabricated on alumina substrates.

The equivalent MMIC amplifier (see fig. 2, right photograph) is representative of circuits that are now in limited production. Three monolithic distributed amplifiers are assembled with a single thin-film network on a carrier. The distributed amplifier MMICs have very flat gain with a low I/O SWR and can be directly cascaded without Lange couplers.

A comparison of circuit complexity of the hybrid and MMIC implementations of the amplifier yields some striking differences in component count and interconnection count (see the table). Further, the critical interconnections associated with the Lange couplers and the FETs require manual bonding by a very skilled assembly operator. In contrast, the MMIC amplifier can be assembled using automated equipment, eliminating the need for highly skilled assembly workers.

All the MMICs that TI is developing are being designed for low-cost, high-volume production following strict design rules. One key goal that must be reached is to achieve minimal human interaction in amplifier assembly and test. Therefore, for reliability and cost control, all MMIC thin-film networks and other parts must be designed to be assembled by automatic placement and wire-bonding equipment. In the first step of assembly, for example, all amplifier MMICs, device pedestals, and thin-film networks are soldered to a carrier plate in a single operation.

A typical production problem with hybrid microwave circuits that is solved with MMICs is represented by multiple broadband Lange couplers. The fine-line crossovers on the microwave thin-film circuits that implement these couplers are usually formed by bonding one wire at a time (see fig. 3, top photograph). This is a labor-intensive, costly process, and the production throughput is low—especially for small-geometry circuits in the 6-to-18-GHz range that can require interconnection between lines with 25-μm geometries.

But reliable techniques are now available that, on a production basis, allow air bridges to be made efficiently. With these new techniques, plated-gold air-bridge crossovers replace the manual interconnection operation (wire bonding). These plated crossovers (see fig. 3, bottom photograph) are formed during a thin-film circuit's fabrication by various precision photolithographic patterning techniques, sputtered metal deposition, and gold-plating processes.

The advantage of the new approach is an absolute yield improvement. And what loss there is occurs on inexpensive fabricated parts rather than complex module assemblies. At TI, the interconnection cost associated with Lange couplers is reduced by a factor of seven when plated crossovers replace wire-bonded crossovers.

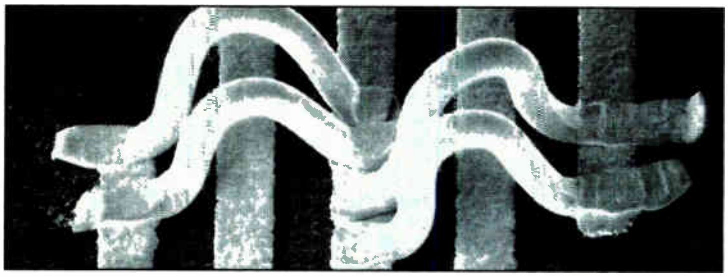
Aided by an ever-growing data base of GaAs, FET, and other component and circuit attributes, characteristics, and procedures, MMIC performance is proving to be consistent both on-slice and from slice to slice. The MES FET is the basic building block of GaAs MMICs, and designs with it are based on standard-cell libraries of MES FETs. Similar libraries are available for other passive devices, microstrip transmission lines, and microstrip discontinuities.

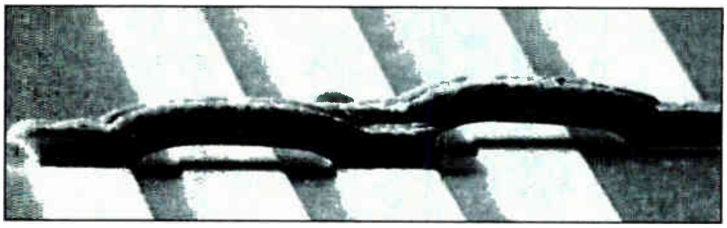
Despite a continuing evolution in the maturity of GaAs MMIC technology and the development of devices that can be system solutions, major technical and affordability issues must still be addressed. Improvements in MMIC design, processing, packaging, and testing are necessary to achieve a more viable technology base. Improving the odds of a first-pass MMIC design success requires the development of more sophisticated CAD programs. Existing linear-analysis programs require improved models for microstrip discontinuities and coupling effects. And designing broadband nonlinear circuits, such as GaAs FET power amplifiers, requires that nonlinear CAD programs become available to designers. Such programs, not commercially available, have been under development at TI and other firms for several years and have proven to be essential.

Further advances in materials and processing technology are needed to improve processing yields, reduce processing costs, and increase production capacity. Recent advances in packaging technology give promise that a low-cost, high-performance MMIC package usable to 20 GHz will soon be available. To further minimize cost, an optimum test sequence for GaAs MMICs must be defined. It must combine both on-slice and in-package dc and rf testing. The need for 100% on-slice rf probing remains an open issue, depending upon whether dc data will prove sufficient to gauge rf performance. The MMIC process flow complicates the task of achieving 100% on-slice rf probing of MMICs at microwave frequencies, especially on thin (0.10-mm) wafers.

The next major step in the technology development is largely a manufacturing-technology effort. This is a critical transition period in which the technology emerges from limited production to full-scale manufacturing.

During this phase, monolithic-circuit cost and yield goals must be defined for each market. Initial production runs of MMICs will determine the critical yield and cost drivers and establish the correlation and sensitivities between processing parameters and electrical performance. Following this identification effort, process controls and refinements must be implemented, and yield and cost improvements will have to be demonstrated. □





3. CROSSED BRIDGES. Bonding 0.007-in. wires (top) to interconnect Lange couplers requires a skilled operator. Air bridges (bottom) formed in a thin-film process eliminate this bonding.

For more information, circle 482 on the reader service card.

WHY GARY LERUDE IS BULLISH ON MMICs

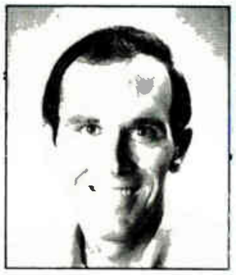
For D. Gary Lerude, two important questions have been facing Texas Instruments and other makers in the military microwave business: can monolithic microwave integrated circuits be produced in volume at a price a system purchaser can afford, and can they overcome the traditional problems that microwave devices have always had?

"Today the answer [to both questions] is yes for a wide variety of simple parts, and if developments in the MMIC industry continue as they have, more complex MMICs will become effective," says Lerude, engineering manager of TI's Microwave Military Components department in Dallas.

"The MMIC industry is only in the early stages of its life," he adds. "Despite the progress we've made, it should not be thought that GaAs-based MMICs are anywhere up to the level of what has been achieved by silicon-based ICs."

Lerude points out that the microwave industry, highly dependent on government contracts, has long been associated with low production volumes and a high component cost. And the emphasis has been on performance, with cost secondary. "Another factor is that military requirements have not yet provided sufficient production volumes to yield the learning-curve improvements that drive the silicon technology or to justify capital investment in large-scale automation." So military microwave systems have gone the hybrid route, with more costly hand-wired operations and chancier yields.

Lerude is a prime mover in TI's attempt to move MMICs into high gear. Joining TI in 1978 as a microwave design engineer supporting the high-speed anti-radar missile (HARM) program, he has been involved in military microwave-component development ever since. He is currently responsible for the technical development and support of GaAs foundry services, GaAs FETs, and MMICs. He holds a BSEE from the University of Denver, an MS in systems engineering from Wright State University, and an EE degree from Southern Methodist University.



D. GARY LERUDE

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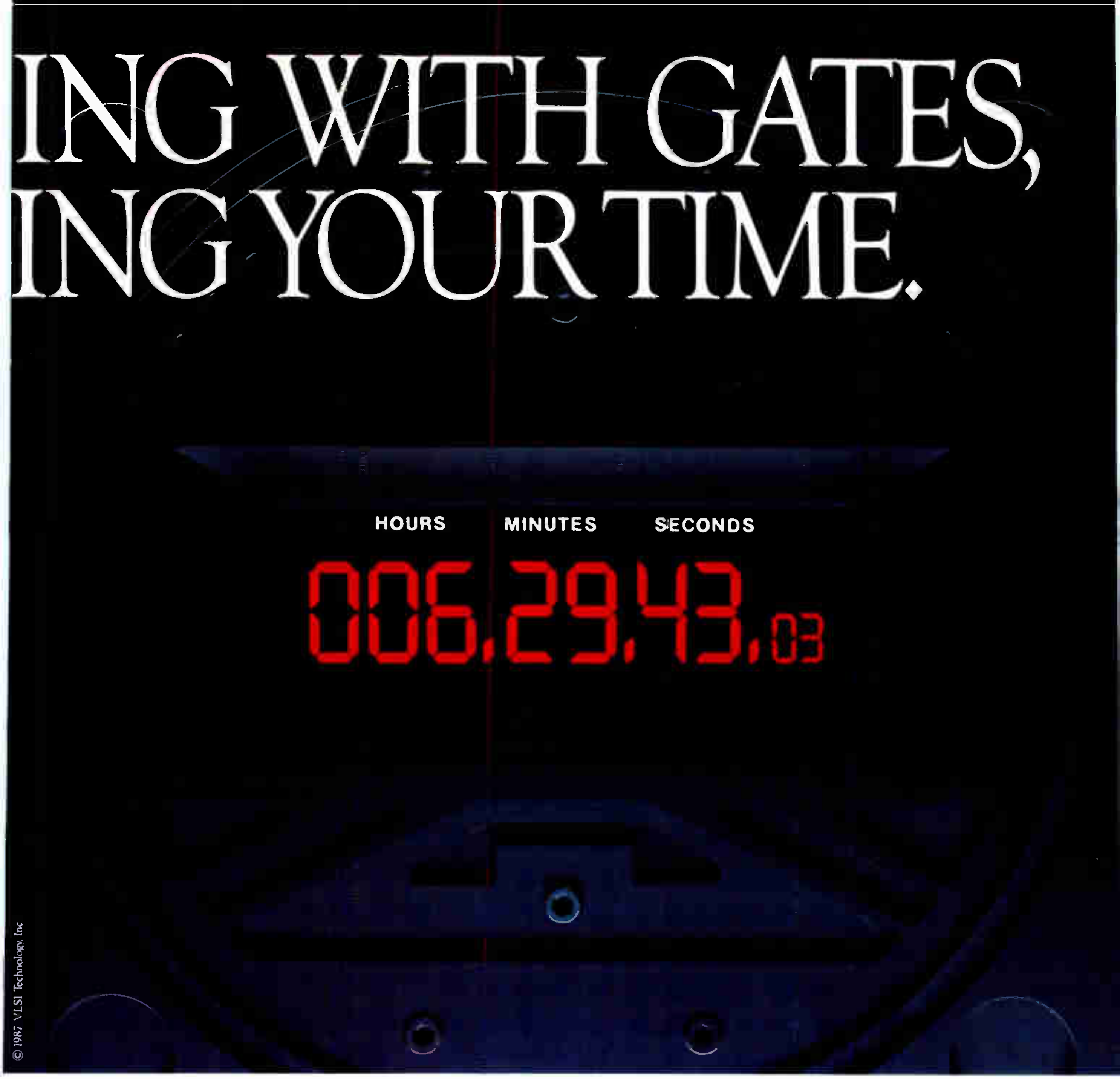

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MILITARY/AEROSPACE NEWSLETTER

HUGHES TO BUILD INTEGRATED PROCESSOR FOR ADVANCED TACTICAL FIGHTER

The high-stakes battle to win a development contract for the Common Integrated Processor in the Air Force's YF-22 Advanced Tactical Fighter program heated up when GMHE/Hughes Aircraft Co. was chosen in late July to develop the processor for the Lockheed-Boeing-General Dynamics team. The other competitor in the YF-22 program, a team of Northrop and McDonnell Douglas, is expected to announce its choice of a processor developer shortly. The processor, which is the core computing element for all avionics subsystems in the fighter, will integrate signal- and mission-processing functions that are currently handled by dedicated processors. The processor's hardware will draw heavily on Very High Speed Integrated Circuits technology. The known contenders vying for the yet-to-be-awarded Northrop-McDonnell Douglas development contract are Hughes, AT&T, IBM, and Westinghouse. Westinghouse has already won contracts to develop the rf portion of the radar subsystem from both teams. Why so much interest? Insiders say the winning production contract could be worth $1 billion. □

GRUMMAN TO ROLL OUT A-6F, BUT PRODUCTION IS UNCERTAIN...

The first of five pre-production A-6F Intruders was scheduled to be rolled out on Aug. 3 for flight testing at Grumman Corp.'s Calverton, N. Y., operation, and Grumman may have learned by then whether the program has a future beyond that. The Navy has requested $702.2 million to buy 12 new A-6Fs, complete with upgraded avionics and a new radar system, during fiscal 1988, but the funds may not be forthcoming. The House Armed Services Committee supports the program, but its Senate counterpart is trying to shoot it down in favor of additional funding for the Navy's next-generation attack plane, the Advanced Tactical Aircraft. Grumman has been working on the A-6F since August 1984 under a no-profit, fixed-price, full-scale development contract. The company originally expected a production buy of more than 150 Intruders. □

...WHILE ITS F14D AVIONICS DEVELOPMENT MOVES AHEAD

The $984 million program to develop the next generation of the Navy's F14 tactical interceptor and fighter moved a step closer to a prototype in July when Grumman Corp. established the F14D Avionics Development Laboratory. The program began in July 1984. Prototype avionics subsystems are due to Grumman from subcontractors by September, and Grumman figures to spend a year testing the units. Integrating the systems, however, won't go so fast. A spokesman says software development and integration will likely continue through flight tests and right up until March 1990, when the Navy is set to take delivery. Five planes will be built—one to test the new F14 engines, three to test the flight systems, and one fully operational model. □

PENTAGON HAS UNDER WAY OVER 100 PROGRAMS USING FIBER OPTICS

Fiber-optic sales to the U. S. military are booming. New applications, as well as such optical-fiber features as light weight, radiation resistance, and immunity to electromagnetic interference, are resulting in an almost 50% gain over 1986 in U. S. military budgeting this year, to an estimated $90 million. Currently, there are more than 100 programs under way within the Pentagon that involve optical fiber, according to Steven B. Searcy, chief of the electro-optics branch of the Defense Electronics Supply Center, Dayton, Ohio. One military contractor, Corning Glass Works, Corning, N. Y., is proposing several new applications, including fiber-tethered torpedoes, roving fiber-optic robotic anti-tank weapons, and submarine detection and location networks. □

MILITARY/AEROSPACE NEWSLETTER

EPITAXX READY TO BUILD DETECTOR THAT SENSES BOTH IR AND VISIBLE LIGHT

Epitaxx Inc. is developing an indium-gallium-arsenide photodetector for the National Aeronautics and Space Administration that can detect both visible and near-infrared light. NASA is looking for ways to calibrate and characterize light sources with outputs in the 0.5-to-1.7-μm wavelength. Current methods require two sets of detectors for that range—a silicon detector for visible light, and a germanium detector for infrared. Gregory Olsen, president and chief executive officer, says Epitaxx has already demonstrated feasibility and is now awaiting NASA's go-ahead to develop a production version of the device, which will be the biggest InGaAs device ever built. To accommodate production volumes of the 5-mm-diameter detector, Olsen says the company may switch from conventional 1-in. wafers to 2- or even 3-in. wafers. □

MILITARY SALES OF FLAT-PANEL DISPLAYS ARE EXPECTED TO QUADRUPLE BY 1990

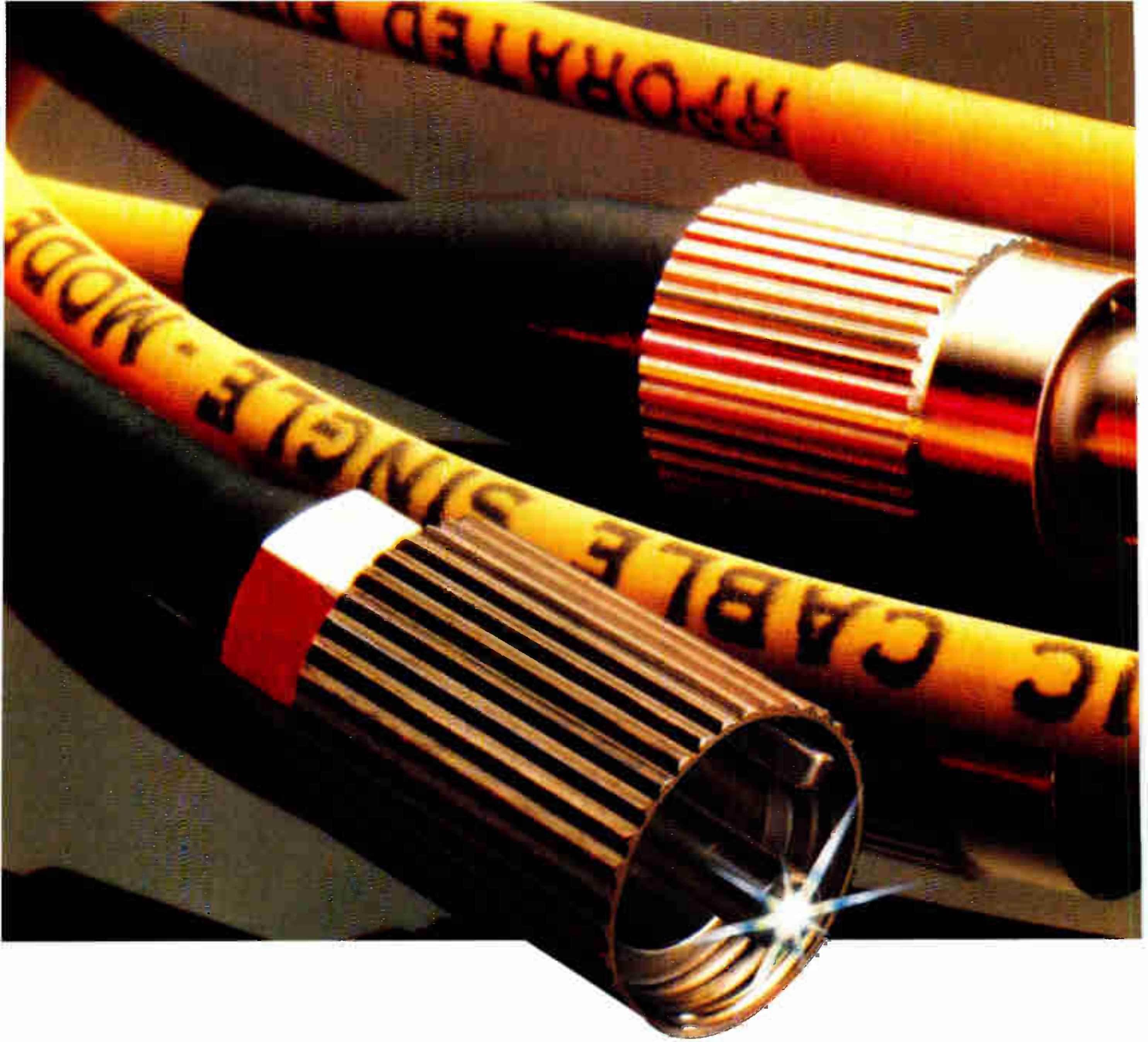
CRTs represent more than 85% of the value of the military display market, but by 1990 the rapid market growth of flat-panel displays will reduce that lead to only 51%, according to a study by Stanford Resources Inc., San Jose, Calif. The study forecasts the CRT market shrinking, in constant dollars, from $727 million in 1986 to $615 million in 1990. In the same period, the flat-panel market is expected to grow from $124 million to $587 million. One reason for this growth is the ongoing replacement of the traditional analog displays in aircraft cockpits by electronic digital displays. But the study predicts that the Army will purchase the most flat-panel displays over the next eight years, putting them in tanks, personnel carriers, command posts, and rugged field computers. Plasma, which is the more mature technology, has captured the major portion of current applications, but Stanford Resources says electroluminescent displays will gain in popularity as they become more reliable. □

SANDERS SOLVES ALQ-126B PROBLEMS; NAVY ONCE AGAIN STARTS BUYING

Satisfied that earlier problems Sanders Associates was having with the production of the AN/ALQ-126B Electronic Countermeasures System were solved, the Naval Air Systems Command is now buying more units. Sanders had previously delivered 350 systems. Being employed as a defensive system for Navy fighters and attack aircraft, the units are in production at the Lockheed division in Nashua, N. H. The ALQ-126 was one of several programs that had unspecified problems when Lockheed acquired Sanders last year. The latest order—a $75 million award out of an overall $149 million contract—calls for production of 151 ALQ-126B units and 74 pod-mounted (ALQ-164) versions for Navy and Marine Corps aircraft. □

DEFENSE CONTRACTORS INCREASINGLY TO LINK UP WITH ELECTRONICS FIRMS

Defense electronics companies are attractive takeover targets because they benefit from a growth market in world defense budgets, according to Prudential-Bache Securities' recently published Aerospace/Defense World Review. The report says the advantages of vertical integration, coupled with the increasing role electronics plays in defense industries, will increasingly drive defense contractors to link up with electronics operations—either as acquisitions or as strategic partners. Prudential is betting, for example, that "Boeing Co. will likely combine the electronic surveillance equipment built by ARGO-Systems Inc. with airframes built by de Havilland, creating a presence in the low-cost airborne-surveillance market." However, the report notes, defense electronics firms will generally not be the targets of hostile takeovers, since their most valuable assets are often employees, who could be scared off by a hostile takeover. □



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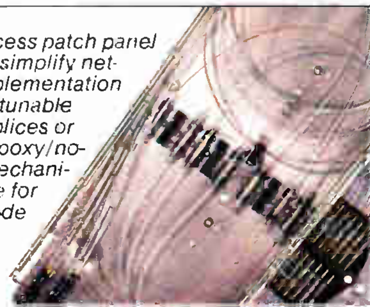
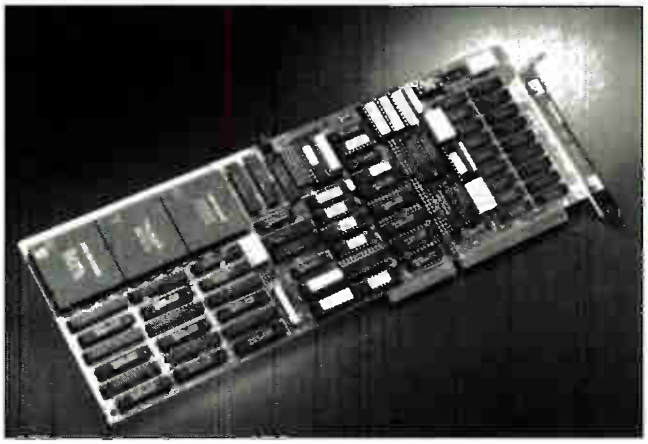


NEW PRODUCTS

MERCURY'S 10-MIPS COPROCESSOR TRANSFORMS VECTORS FAST, TOO

MEMORY CACHE, WEITEK CHIPS BOOST ACCELERATOR'S POWER

The versatility of general-purpose computers and the vector-processing performance of array processors have been combined into a single-board coprocessor described by its developer as a microsupercomputer that offers greater performance—10 million instructions/s—than many systems of either type.



EXPANDABLE. The MC3200's 2 Mbytes of on-board main memory can be augmented in increments of 2, 4, or 8 Mbytes.

The MC3200, from Mercury Computer Systems Inc., is designed for accelerator applications, including simulation, signal processing, and image processing, on the IBM Corp. Personal Computer AT and compatibles, Apollo Computer Inc. DN 3000/4000 work stations, and computers compatible with Motorola Inc.'s VMEbus.

The MC3200 executes scalar and vector instructions at a rate of 10 million instructions/s, or a peak of 20 million floating-point operations/s. That translates into a benchmark of 5 megaflops Linpak with coded linear algorithm subroutines. John Nitzsche, vice president for product planning, says the MC3200 achieves its performance by combining a fast cache memory with an integer-processor unit (IPU) and a floating-point unit (FPU). The latter two devices are the 32-bit Weitek Corp. 8032 XI chip set.

The coprocessor can be programmed in C, Fortran, or Mercury's MC assembly language. A library of scientific algorithms is available; additional software includes an assembler, a parallelizer for code optimization, C and Fortran compilers, a librarian, a linker, an interactive debugger, and a disassembler.

The MC3200 is Mercury's first application accelerator. Since the Lowell, Mass., company's founding in 1983, most of Mercury's boards have been array processors, and the MC3200 comes at a time when the market for accelerators is forecast to grow substantially faster than that for array processors. Jeffry Canin, an analyst with Hambrecht & Quist Inc., San Francisco, estimates that application accelerators will grow from $50 million in 1986 to $210 million in 1990, while the array processor market will grow from $210 million to $375 million over the same period.

John Montelione, marketing manager and a cofounder of Mercury, says the company sees an opportunity to expand in a market closely aligned with its traditional business, and a chance to take advantage of the market's growth.

An early MC3200 user, Cubicomp Corp., Hayward, Calif., has boosted performance 10 to 15 times in a product called the Render Acceleration Compute Engine. It will be used, among other things, to speed three-dimensional animation of graphics, such as the flying logos used as introductions for television newscasts. The Mercury accelerator replaces an Intel Corp. 80287 math coprocessor in Cubicomp's PC AT-based engine.

SCALAR MODE. Nitzsche says the MC3200 is a low-power (15 W peak) board that offers "strong vector processing and is also good in the scalar mode," which is unusual, he adds. A similar product [*Electronics*, March 5, 1987, p. 69] from Sky Computers Inc., also in Lowell, offers faster vector processing, but at a higher price—$10,000 for Sky's product versus $8,000 for the MC3200. Sky's product does not offer scalar processing.

Nitzsche points out that the MC3200, unlike array processors, not only accelerates a mix of vector and scalar operations but also eliminates the need for using the host processor for decision making and data management. "Big chunks of a user's application can now be brought down to the coprocessor, instead of being done on the host," he says, because on-board memory enables users to load a complete program. There's no need to transfer data via the host bus.

The FPU is a dedicated floating-point processor that performs 32-bit arithmetic operations at a maximum rate of 20 megaflops. The 32-bit IPU has a reduced-instruction-set computer architecture that offers 10-mips performance. There is also a 32-bit program sequencer unit, another member of the Weitek family, that operates at 10 mips and includes on-chip address-holding registers to support pipelining instructions—one instruction is executed while the next is fetched.

MEMORY. On-board main memory in the MC3200 ranges from 512 Kbytes to 2 Mbytes of dynamic random-access memory; increments of 2, 4, or 8 Mbytes can be added by installing an optional daughterboard. The two-way interleaved main memory is organized as a 64-bit array; it can output 32-bit data at a peak rate of 40 Mbytes/s or one word transfer every 100 ns. Nitzsche says these rates are a good match for the speed of the Weitek chips.

The 8-Kbit by 8-bit (8,192 instructions) cache memory is implemented in high-speed Fujitsu Ltd. CMOS static RAMs. It holds the most recently executed instructions. If a cache miss occurs, stalling the MC3200, 16 instructions—including the next required instruction—are automatically fetched from main memory into the cache, restarting the MC3200.

Multiprocessing is enhanced in the VME version of the coprocessor, because one MC3200 can autonomously control the bus. In this bus-master mode, one MC3200 can read and write data directly to the memory of another MC3200 without involving the host. Nitzsche says this feature will be beneficial in traditional signal and image processing, as well as in real-time simulation.

The PC AT and Apollo versions of the MC3200 are available immediately. The price of one unit, which includes 2 Mbytes of main memory, is $8,000. The VME version will be available early in the fourth quarter at $10,000. Software run-time licenses range from $300 to $1,500 per board; a complete development environment can be obtained for $7,500 for any version of the board. That environment includes C and Fortran compilers, an assembler, an interactive debugger, a standard mathematical algorithm library, and a driver/executive.

–Lawrence Curran

Mercury Computer Systems Inc., 600 Suffolk St., Lowell, Mass. 01854.
Phone (617) 458-3100 [Circle 341]

CDC'S CAD/CAM SOFTWARE RUNS THREE TIMES FASTER

By shifting its mainframe software for computer-aided design applications to a virtual operating system, Control Data Inc. has improved response time nearly threefold in multiuser systems compared to the company's NOS operating system.

Its ICEM Plus—for integrated computer-aided engineering and manufacturing system—software runs under the company's NOS/VE mainframe operating system. It is complemented in the multiuser environment by four new Unix-based 3-d graphics work stations.

BOARD DESIGN. ICEM Plus includes an advanced design and drafting package known as DDN Version 2.0—for design, drafting, and numerical control—as well as ICEM Electronics, which includes schematic capture, layout, and routing packages for printed-circuit-board design. Data from these two packages can be merged, eliminating data reentry when moving between systems.

Another key ICEM Plus feature is a suite of information-management software that Alan M. Christman, general manager for CIM market planning, contends is the best in the industry. "Managing enormous amounts of product and project data is one of the most crucial and difficult tasks facing manufacturing engineers today," he says.

The ICEM Plus offering includes a new package called ICEM EMS, for environment management system, that runs at the work-station level as the designer's personal information controller and administrator. Other packages run at the mainframe or departmental-computer level to support data management in a multivendor environment, with support for machines built by Apollo Computer, Digital Equipment, and IBM.

Control Data's work stations include two reduced-instruction-set-computer-based machines designated the Cyber 910 series 500. They and the two low-end 300-series models are made by Silicon Graphics Inc., Mountain View, Calif.

The 500 series combines a 12.5-MHz RISC processor and floating-point coprocessor to execute 10 million instructions/s, as well as 1.9 million floating-point operations/s (single-precision) or 1.08-megaflops (double-precision). Model 520 has a 19-in. monitor, 8 Mbytes of random-access memory, and two Control Data Corp. 182-Mbyte disk drives. It costs $84,900, complete with DDN and EMS software. The model 537 has one hard-disk drive and costs $72,400 without software.

At the low end, the Cyber 910 model 315 with a 15-in. monitor, 4 Mbytes of RAM, and one hard-disk drive costs $25,545. The model 320 adds a floating-point accelerator, a 19-in. monitor, 8 Mbytes of RAM, and DDN and EMS software, for $48,545. The 1.8-mips series 300 machines are 68020-based. All four will be available in October.

ICEM Plus software will be available next month. ICEM DDN costs $5,000 for the first user and $4,000 for each additional user up to a ceiling determined by the mainframe being used. The ceiling on the Cyber 180 model 930, for example [*Electronics*, April 2, 1987, p. 113], is 15 users or $61,000 for an unlimited license.

–Wesley R. Iversen

Control Data Corp., CIM Division, 1450 Energy Park Dr., St. Paul, Minn. 55440.
Phone (612) 642-3801 [Circle 342]

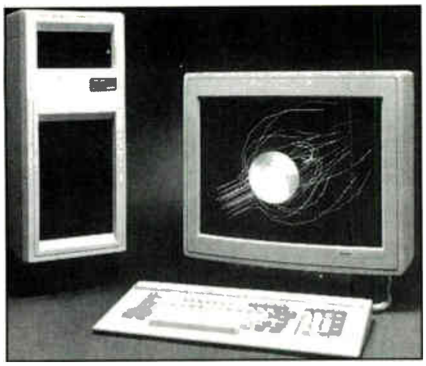
PROCESSOR DOES 140,000 VECTORS/S

To meet the growing demand for highly realistic, true-color three-dimensional computer graphics, Raster Technologies Inc. has designed a 32-bit floating-point display processor that executes 140,000 10-pixel 3-d vectors/s—2.5 times the speed of its predecessor.

The Model One/385 display processor also offers 16.7 million displayable colors, and it can be configured into many high-performance computer systems. It targets original-equipment manufacturers who design systems to handle such demanding applications as molecular and chemical engineering, atmospheric research, and mechanical computer-aided engineering.

The controller's 2-d capabilities also make it useful for large cartographic applications and training systems that require simultaneous displays on two monitors. Its 2-d vector-transformation performance is nearly triple the rate of previous models, says the Westford, Mass., company.

By using a buffered direct-memory-access and interface boards tailored to specific computer systems, the Model One/385 can be linked to a wide variety of host central-processing units and their data bases, including Digital Equipment Corp.'s VAX and MicroVAX as well as computers from Convex Computer, Data General, Gould, and Prime Computer. The system maximizes flexibility so that users can buy an entry-level model and upgrade easily as processing requirements grow.



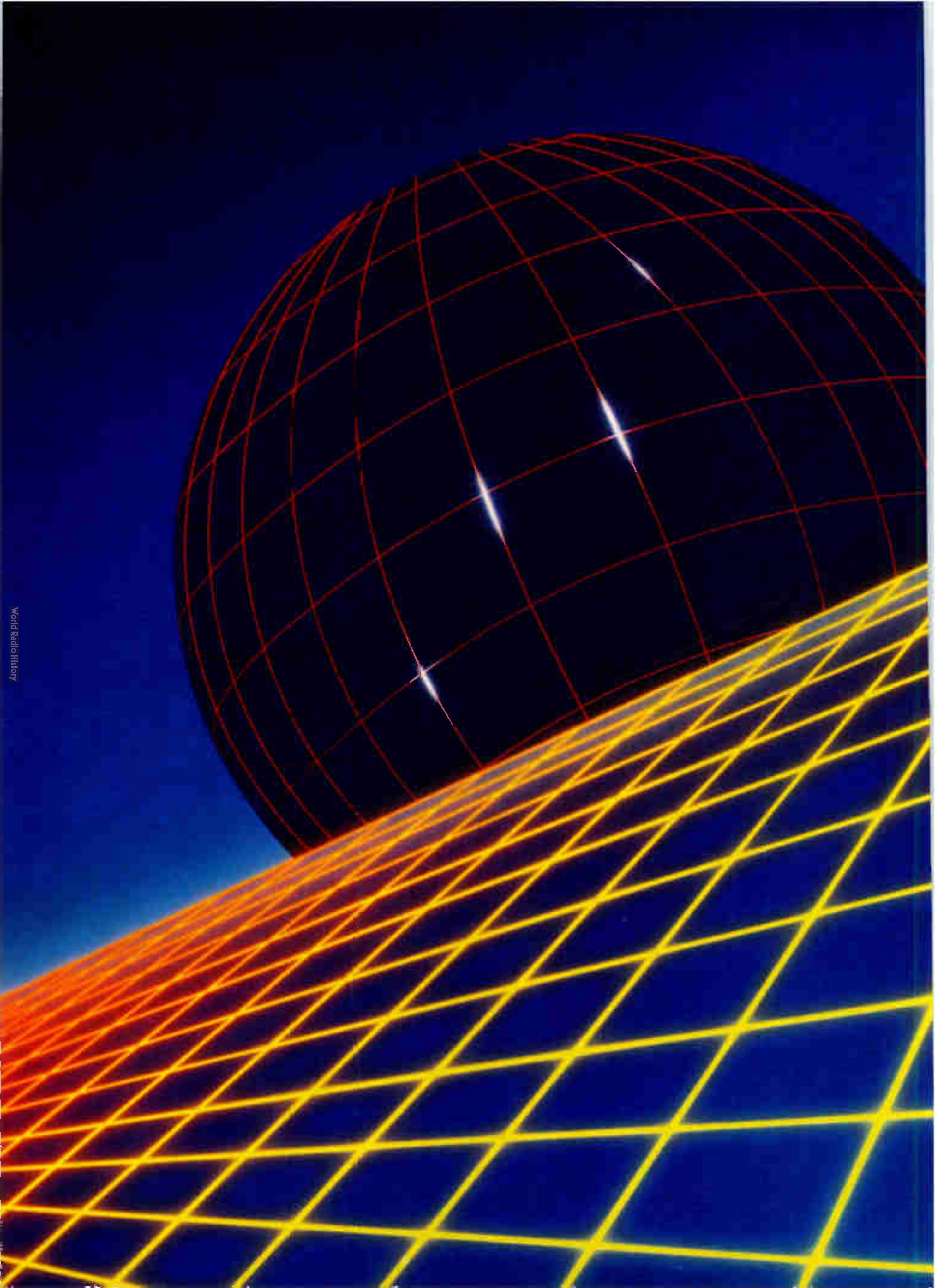
COLORFUL. Raster's graphics processor boasts a palette of 16.7 million colors.

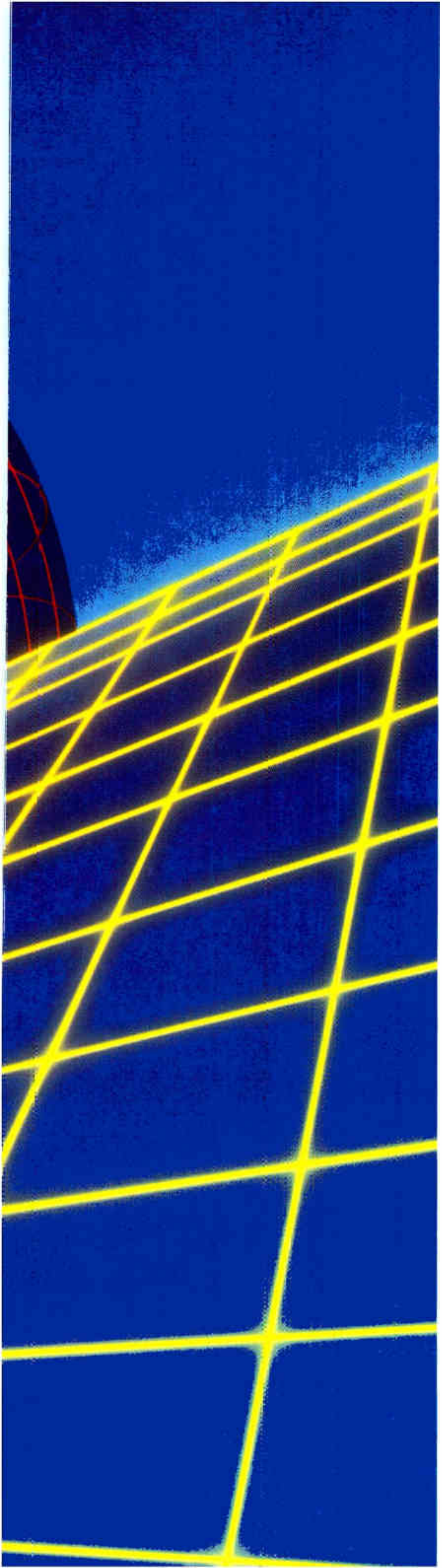
The standard Model One/385 processor includes 3-d modeling features, such as up to eight light sources of different colors, hidden-surface removal, and Gouraud shading; 1,280-by-1,024-pixel resolution; 4 Mbytes of memory; 2-bit alphanumeric overlays; 2-d transformation support; 60-Hz noninterlaced refresh rate; emulation of Digital Equipment Corp. VT100 terminals; and RS-232-C and direct-memory-access interfaces.

OPTIONS. Higher-priced configurations include double-buffered overlays, 24 bits of true-color image memory, and a displayable palette of 16.7 million colors. "To get realistic shading, you need 32 levels of color to show gradations for just one color," says Whitney Harris, product manager at Raster Technologies. "With 16.7 million, you don't have to worry about running out."

The controller will be available starting at $33,000 in November. A monitor, a keyboard, an input device, and software libraries are not included in the price. *–Paul Angiolillo*

Raster Technologies Inc., Two Robbins Rd., Westford, Mass. 01886.
Phone (617) 692-7900 [Circle 343]





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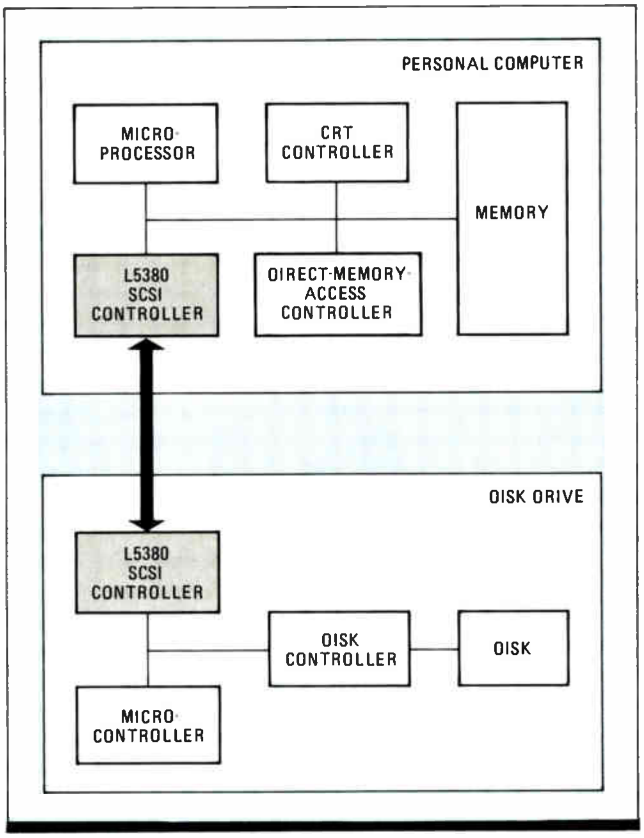
SCSI CONTROLLER CHIP BOOSTS SPEED 5-FOLD

LOGIC DEVICES' 4-MBYTE/S DEVICE USES 1.5-MICRON TECHNOLOGY TO GET SPEED, 90% POWER REDUCTION

By combining 1.5-μm CMOS technology with design techniques developed for digital-signal-processing circuits, Logic Devices Inc. has turned out a Small Computer Systems Interface controller that offers both asynchronous operation and 4-Mbyte/s performance—2.5 to 5 times faster than previous asynchronous devices.

Besides boosting performance, the L5380 SCSI controller's double-level metal, single-polysilicon process means the device draws just 75 mW—one tenth the power of competitive devices fabricated in n-channel MOS technology, says Joel Dedrick, director of product development.

"Until the introduction of this device," says Dedrick, "it was believed that the upper limit on the original asynchronous SCSI controllers was about 1.5 to 2 Mbytes/s. As a result, some manufacturers have taken to using the synchronous protocol to achieve higher throughputs. Although this has allowed rates of up to 4 Mbytes/s, these controllers are not compatible with the earlier [asynchronous] devices. This forced [end] users to completely redesign their systems in order to take advantage of the higher performance, defeating the whole purpose of the SCSI standard."



INTERFACE. Logic Devices' SCSI controller chips transfer data between personal computers and disk drives at 4 Mbytes/s.

The L5380 is fully compatible with the original 750- to 800-Kbyte/s first-generation controllers from NCR Corp., Dayton, Ohio, and Advanced Micro Devices Inc., Sunnyvale, Calif., as well as both companies' 1.5-Mbyte/s asynchronous upgrades.

The L5380's design improvements eliminate eight architectural defects in the original design of the NCR and AMD parts while maintaining full plug-in compatibility. For example, the NCR and AMD parts had prevented designers from using the block-mode direct-memory-access feature of the devices, says Dedrick.

Internal registers allow the L5380 to function as either an initiator or a target. When connected as an initiator, the L5380 arbitrates for the SCSI bus and allows for selection of a target. When connected as a target, the device supports SCSI bus arbitration and reselection of an initiator.

Direct microprocessor interfacing allows for easy reading and writing of the internal registers, says Dedrick. The L5380 also generates interrupts to allow the microprocessor to handle error conditions and monitor the overall status of transactions on the bus. "With the L5380 supporting the SCSI physical layer," says Dedrick, "users can implement a low-cost host-to-SCSI adapter by embedding the full SCSI protocol subset in firmware."

As in the AMD and NCR parts, the L5380's single-ended drivers can handle up to 48 mA, allowing it to drive the SCSI bus directly.

The L5380 is available now in 2- and 4-Mbyte/s versions packaged in 40-pin plastic dual in-line packages or in 44-pin plastic leadless chip carriers for surface mounting. The DIP-packaged 2-Mbyte/s L5380PC costs $8.53 each, and the L5380JC in the PLCC costs $9.71 per piece—both in 100-unit quantities. The 4-Mbyte/s L5380PC-4 costs $17.53; the L5380JC-4 is $18.71, also in 100-unit purchases. *–Bernard C. Cole*

Logic Devices Inc., 628 East Evelyn Ave., Sunnyvale, Calif. 94086.
Phone (408) 720-8630 [Circle 440]

SOFTWARE CUTS ENCRYPTION COSTS

Dual-purpose error-correction and encryption software from Digital Signal Equipment Inc. can encode a typical two-page document of 4,000 bytes in about 30 seconds. Decoding and error correction after transmission take about one minute. This performance is on a par with stand-alone hardware systems.

By running the $490 Codetext software package on an IBM Corp. Personal Computer AT equipped with a math coprocessor, instead of using the present solution of purchasing single-purpose stand-alone hardware, users can save as much as the cost of a PC yet obtain equivalent performance. The software also codes and error-corrects digital voice messages.

The Houston-based startup guarantees complete correction of transmission-noise errors for error rates ranging as high as 2.5%. What's more, Codetext handles the job with one-way communication—eliminating the return link generally required for verification on other systems.

Company president George D. Doland invented a new block code for Codetext. It is a 280-bit block consisting of 35 bytes of coded information. Embedded within each coded block are 15 bytes of "real" information. The code is a "hard-decision" type that accords each bit of information equal weight in the decoding process.

The software uses 160 encoding-decoding equations that can be altered to produce 2^{160} variations without impeding performance, says Doland. With this capacity, an extra layer of security can be implemented through customized software packages. Customization costs an additional $250. Exact matches of the tailored encoding-decoding algorithms must be installed on both the sending and receiving links.

The software boasts superior tolerance to transmission-line noise. Codetext is guaranteed to correct all blocks of transmitted bits with up to 2.5% errors and typically will correct all blocks with three times that error rate, says Doland.

The software's algorithm offers a 9-dB asymptotic decoding gain—that's a measure of how much signal power can be decreased without increasing errors due to noise. Other hard-decision encoding schemes require a 12-dB decoding gain to achieve the same error-correction performance, says Doland.

This performance edge means lower-quality phone lines can be used for data transmission with the same accuracy.

Once a data file is ready for encoding, the program reads in information bits from memory, block by block. Code bits are then generated and scrambled in with the information bits. After a new encoded file is created, the data is ready for transmission via modem. The receiving system reads the incoming encoded file and unscrambles the stream by separating information bits from code bits. Information bits are recoded and then compared to the received bits, resulting in a syndrome for subtracting everything but errors. Doland's proprietary process corrects only the information bits, and the system readies a file for display or printout.

The standard Codetext package, written in Fortran, and customized versions are available now.

–J. Robert Lineback

Digital Signal Equipment Inc., P.O. Box 890584, Houston, Texas 77289-0584. Phone (713) 480-7496 [Circle 441]

CONVERTER FREES HOST FROM PERIPHERAL CHORES

By integrating a microcomputer and a 256-Kbyte random-access-memory buffer, National Instruments Corp.'s GPIB-PRL converter helps free host computers from the task of monitoring printers, plotters, and other slow-running peripherals.

The GPIB-PRL, a data-communications converter bridge between IEEE-488 bus systems and Centronics ports, can be configured to handle transparent data and protocol conversion in either direction simply by setting a switch. It is the first in a series of intelligent data converters that will eventually provide bridges between the IEEE-488 bus and RS-232-C ports and the IEEE-488 bus and IEEE-422 ports. The GPIB-PRL can also be addressed by multiple computers on the IEEE-488 bus.

Based on Hitachi Ltd.'s 8-bit 64180 microcomputer, it includes on-board controllers for direct-memory access. A firmware-based operating system loaded into programmable read-only memory enables the converter to perform all of the IEEE-488 protocols and system upkeep. Integrating the microprocessors, controllers, and operating system in the converter means host computers don't have to execute special commands or controls. It may also be dedicated as either a bus "talker" or "listener."

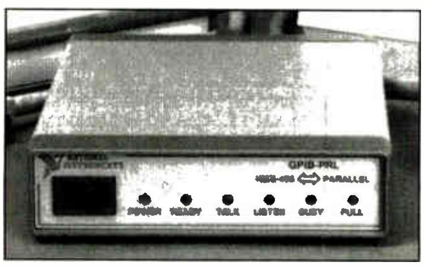
BLOCKS OF DATA. If the file to be transferred is larger than the converter's buffer memory, it automatically takes data from the computer host in blocks. The standard data buffer for "byte spooling" is 64 Kbytes, which can be expanded to 256 Kbytes, says Bob Summersett, product design engineer. When all the buffered data has been sent to the peripheral, the converter will alert the host that it is ready for another block, using the service-request-on-empty feature of the IEEE-488 bus—also known as the General Purpose Interface Bus, or GPIB.

The converter performs direct-memory-access control for 900-Kbyte/s transfers over the GPIB, says Summersett. It takes only 300 ms to fill the 256-Kbyte buffer. The Centronics interface handles data rates of up to 700 bytes/s. Most printers or plotters run much slower than the maximum throughput, Summersett notes.

The standard GPIB-PRL converter, with 64 Kbytes of buffer memory, is now available for $495 each. Models with the 256-Kbyte expansion memory cost $695.

–J. Robert Lineback

National Instruments Corp., 12109 Technology Blvd., Austin, Texas 78727-6204. Phone (512) 250-9119 [Circle 442]



FAST BRIDGE. National's GPIB-PRL can handle 900-Kbyte/s transfers to peripherals.

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TC511000 - 12	1 Mb x 1	CMOS	120 ns	Fast Page	18 pin
TC511001 - 85	1 Mb x 1	CMOS	85 ns	Nibble	18 pin
TC511001 - 10	1 Mb x 1	CMOS	100 ns	Nibble	18 pin
TC511001 - 12	1 Mb x 1	CMOS	120 ns	Nibble	18 pin
TC511002 - 85	1 Mb x 1	CMOS	85 ns	Static Column	18 pin
TC511002 - 10	1 Mb x 1	CMOS	100 ns	Static Column	18 pin
TC511002 - 12	1 Mb x 1	CMOS	120 ns	Static Column	18 pin
TC514256 - 85	256K x 4	CMOS	85 ns	Fast Page	20 pin
TC514256 - 10	256K x 4	CMOS	100 ns	Fast Page	20 pin
TC514256 - 12	256K x 4	CMOS	120 ns	Fast Page	20 pin
TC514258 - 85	256K x 4	CMOS	85 ns	Static Column	20 pin
TC514258 - 10	256K x 4	CMOS	100 ns	Static Column	20 pin
TC514258 - 12	256K x 4	CMOS	120 ns	Static Column	20 pin

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Circle 113 on reader service card

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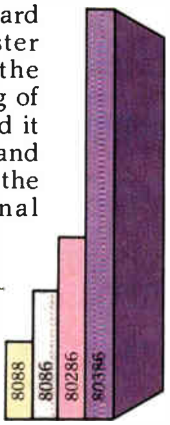

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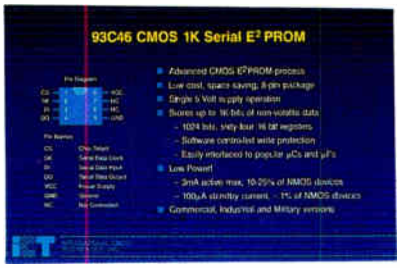

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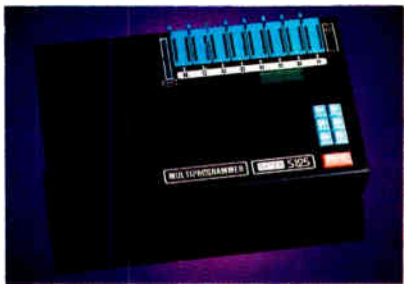

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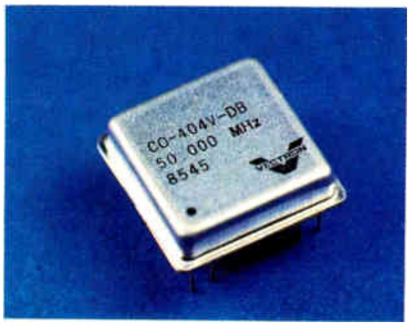

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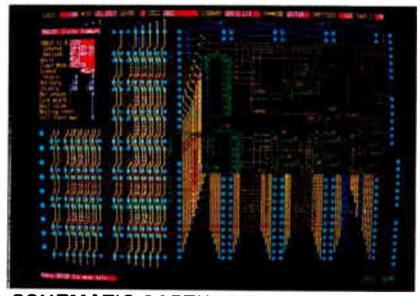

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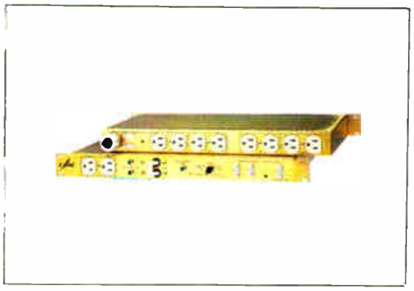

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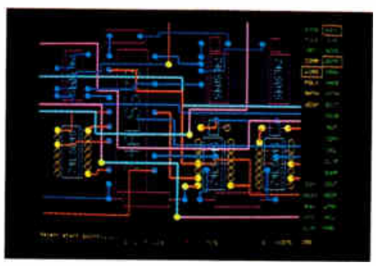

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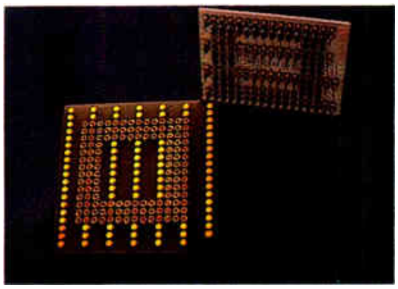

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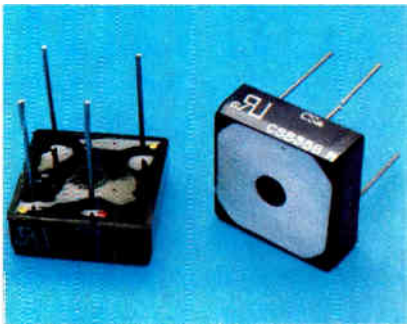

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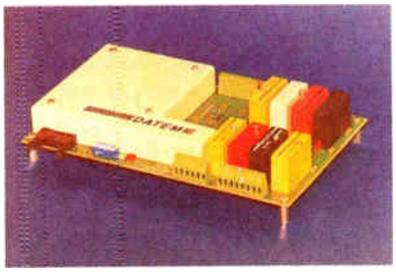

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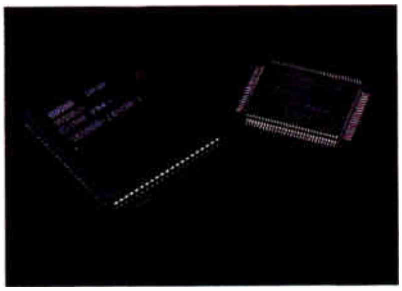

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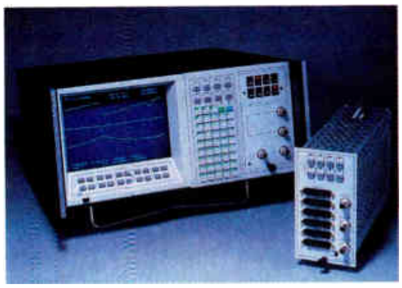

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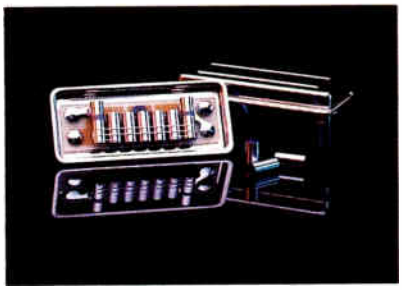

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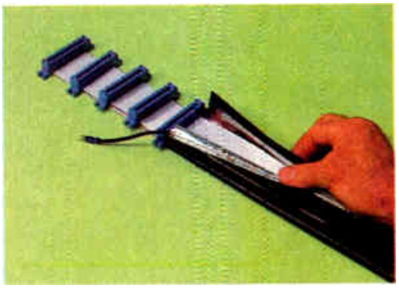

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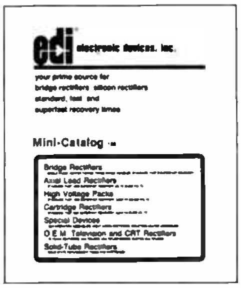

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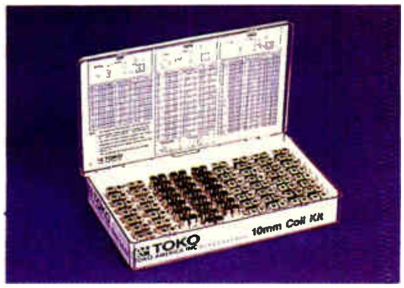

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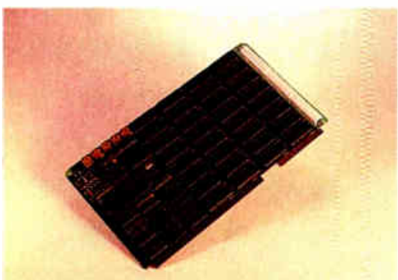

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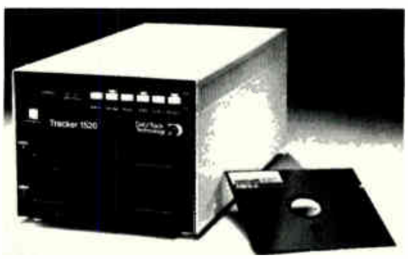

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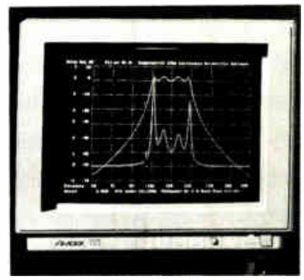

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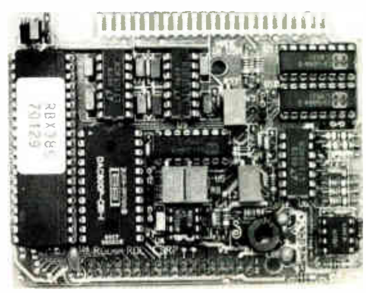

SBX ANALOG I/O

The RBX388 has 16 S.E. or 8 diff. analog inputs and 8 analog outputs, all on a single width SBX module of approx. 10 sq. inches. 12 bit resolution on both inputs and outputs. Resistor programmable gain for inputs. Several jumperable ranges for outputs. On-board microprocessor provides optional continuous automatic scanning of inputs. ROBOTROL CORP., 16100 Caputo Drive, Morgan Hill, CA 95037. (408) 778-0400.

RBX388 CIRCLE 209

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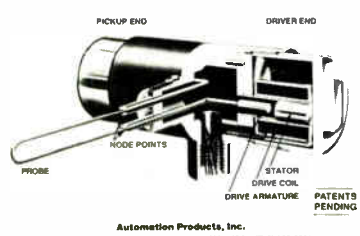

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AUTOMATION PRODUCTS, INC. CIRCLE 242

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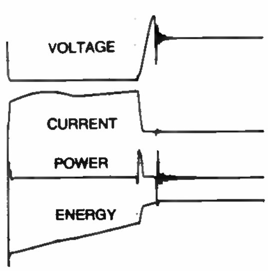

These waveforms show an IS_SPICE analysis of a power supply snubber. Intu_Scope was used for display and computation of power and energy. The output shown used an Intu_Scope plotter utility

PRE_SPICE, $200.00: Interactive control, Monte Carlo Analysis, Optimization, libraries and parameter evaluation.
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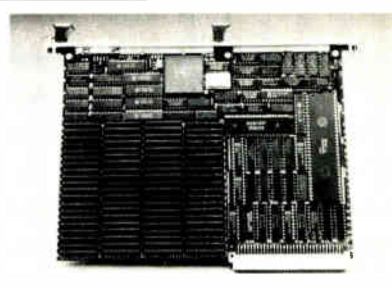
INTUSOFT CIRCLE 229



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ELECTRONICS WEEK

GENRAD WILL LEAVE VLSI TEST BUSINESS

GenRad Inc., a Concord, N. H., manufacturer of automatic test equipment, has decided to shut down its Semiconductor Test Division in Milpitas, Calif. The move takes GenRad out of the VLSI test business, where it had begun to gain market share, but where profits had proven elusive. The company will now focus primarily on board testing, which has historically accounted for more than half its revenue. The company is looking for a buyer for the division, whose products include the recently introduced GR300 VLSI test system [*Electronics*, May 28, 1987, p. 23].

IBM FORMS NEW SOFTWARE UNIT

Applications software development at IBM Corp. has often taken a back seat to hardware development, partly because it was scattered throughout the computer giant. Now that will change, as IBM combines all these activities under one roof in a new Application Systems Division. The new unit, based in Milford, Conn., will develop and acquire application software for all IBM hardware on a worldwide basis and will also provide support for companies developing applications software for IBM systems.

HARRIS SUPERMINI TAKES ON VAX

The newest member of Harris Corp.'s Unix-based HCX family of superminicomputers is an entry-level model aimed at Digital Equipment Corp.'s VAX machines. Harris's Computer Systems Division, Fort Lauderdale, Fla., is putting the HCX-5 up against DEC systems in both end-user software-development applications and in the value-added reseller market. The machine includes a 32-bit central processor—built in Schottky TTL bit-slice logic—that can handle 5 million instructions/s, and a 40-Mbyte/s VMEbus that is nearly four times faster than the 12-Mbyte/s I/O subsystems found in most superminis, says Rick Maule, the division's director of product marketing. The HCX-5, which supports up to 128 users, will be available in October for $124,500 and up.

XEROX ENHANCES PUBLISHING SYSTEM

Xerox Corp. is introducing several enhancements to its XPS 701 electronic-publishing system. The 7650 Pro Imager graphics scanner, used with the new XPI Version 2.0 software for the Xerox Publishing Illustrator's Workstation, offers 600/1,200-dot-per-inch resolution, as well as image cropping and editing capability. Another software package connects XPIW and Xerox 6085 work stations to the XPS 701 via Ethernet. The new Peripheral Expansion Cabinet, with four 300-Mbyte disk drives, provides the necessary memory.

STEREO SOUND BOOSTS TV SALES

The widespread move to stereo TV broadcasting is fueling a record pace in U. S. factory sales of color TVs. Of the 8.8 million color sets shipped during the first half of the year, 1.6 million have built-in stereo capability—29% more than 1986's first half, according to the Electronic Industries Association. Total sales are up 8% over the first six months of 1986, when sales hit a record 18.1 million units annually, and the EIA believes some 18.3 million color sets will be sold this year. The EIA also predicts shipments of stereo units will hit 4.3 million this year, or about 23% of the color TV total.

PRIME TO SELL SUN WORK STATIONS . . .

Prime Computer Inc., Natick, Mass., has agreed to buy $75 million worth of Sun Microsystems Inc. products over three years. Sun work stations will be platforms for Prime's computer-aided design and engineering software. For starters, Prime will adapt its Medusa 2-d and 3-d mechanical design and drafting software to the new 3-mips Sun 3/60 work station. Prime will sell the hardware and software package as the Prime WS3600 for $39,900. The pact also allows Prime to purchase any Sun product, including work stations and Sun's library of 900 third-party software packages.

. . . AS IT DOUBLES SPEED OF ITS OWN

The Turbo Option, a single-board central-processing-unit upgrade from Prime Computer Inc., boosts the performance of the Natick, Mass., company's PXCL 5500 3-d work station from 5 million instructions/s to 10 mips. The board also allows the work station to perform 1 million floating-point operations/s. The Turbo Option sells for $7,500 and is available now.

LSI LOGIC GETS INTO PC GRAPHICS

LSI Logic Corp., of Milpitas, Calif., and Video Seven Inc., of Fremont, Calif., are joining hands to develop and manufacture chips for enhanced graphics and other personal-computer applications. The partnership will provide volume manufacturing and time-to-market benefits for Video Seven and will open up application-specific IC markets for LSI's HCMOS technology.

VTI GATE ARRAYS GET SECOND SOURCE

GE/RCA Solid State Division has signed an agreement with VLSI Technology Inc. to become an alternate source for the San Jose, Calif., company's 2-μm VGT10 and 1.5-μm VGT100 CMOS gate arrays, which are capable of densities of up to 10,000 and 67,000 gates, respectively. VLSI Technology's proprietary continuous-gate technology allows up to 75% gate utilization, compared with an industry average of about 50% for comparably sized circuits.

BRIDGE TO MERGE WITH 3COM

Bridge Communications Inc. and 3Com Corp. have agreed to a merger. Both companies make computer networks; Bridge retails network-to-host systems, whereas 3Com supplies office networks to value-added resellers. The merged companies will continue under the name of 3Com, headquartered in Santa Clara, Calif.; Bridge will become a subsidiary that will continue to operate in Mountain View, Calif.

CYPRESS LICENSES SUN'S SPARC

Cypress Semiconductor Corp., of San Jose, Calif., and Sun Microsystems Inc., of Mountain View, Calif., will jointly develop a new high-performance reduced-instruction-set-computer chip based on Sun's Scalable Processor Architecture, or Sparc. Built under license, the chip will be a 0.8-μm dual-metal CMOS version of the 10-million-instruction/s, 1.5-μm microprocessor at the heart of the Sun-4/200 family of work stations and servers.

10-MIPS MS-DOS BOARD COMING

Definicon Systems Inc. will use Fujitsu Microelectronics' 2-μm CMOS gate-array-based 32-bit RISC chip—which is built around Sun Microsystems' Sparc—to build an MS-DOS-compatible coprocessor board capable of over 10 million instructions/s. In an agreement worth more than $3 million, the Newbury Park, Calif.-based Definicon will use the Sparc chip plus Fujitsu's 32-bit floating-point interface chip on the board, which will be introduced later this year.

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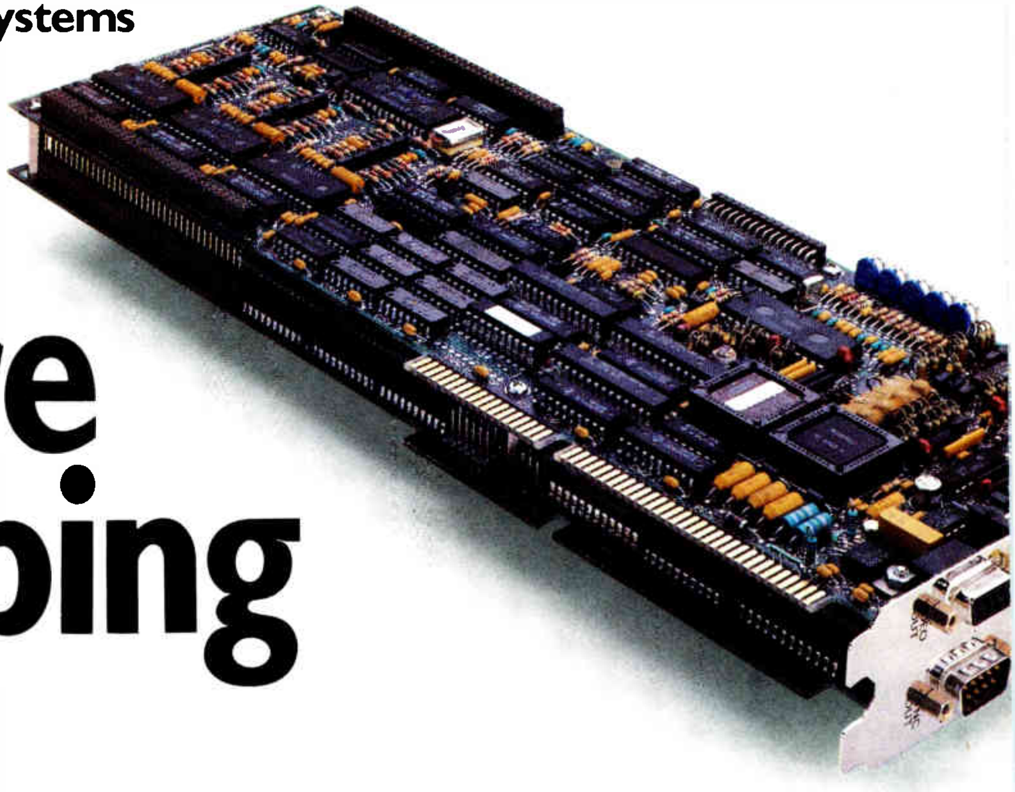

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