SYSTEM PROBLEMS SHOULDN'T SLOW STATIC RAM BOOM/60

MOTOROLA'S RADICAL SRAM DESIGN SPEEDS UP SYSTEMS/66

A McGRAW-HILL PUBLICATION SIX DOLLARS JULY 23, 1987

Electronics®

THE HORSEPOWER RACE IN 3-D GRAPHICS

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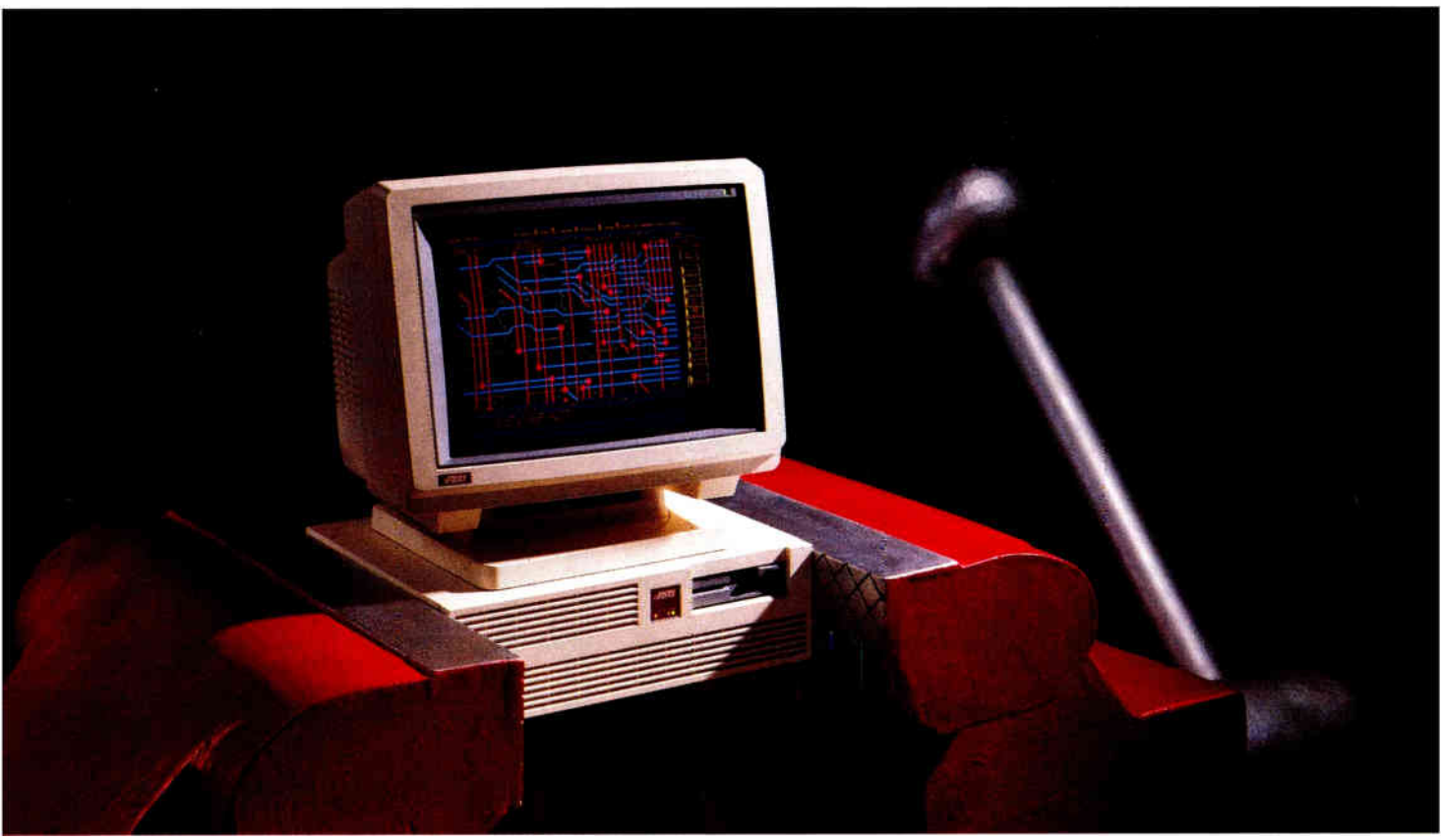
Only Mentor Graphics stands up to the pressures on PCB layout.



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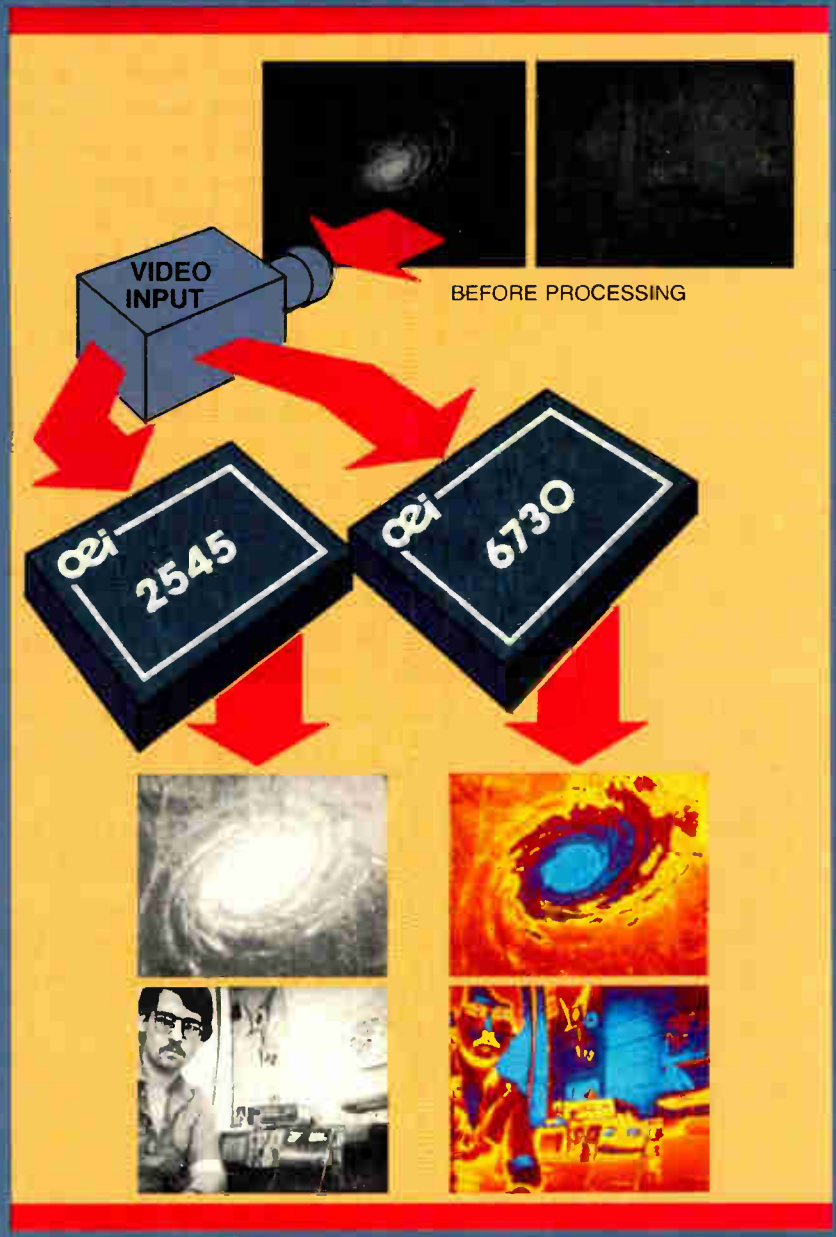
The illustration at right and diagram 'A' below are examples of gray scale enhancement via the OEI #2545 Video Enhancement Module. The basic operational function of this device is logarithmic conversion. The photos illustrate the power of logarithmic expansion for resolving information out of black level or low gray level signals. The #2545 module is equipped with an adjustable signal splitter. This gives the user the option of adjusting the point or level at which the signal is expanded or compressed. The illustration at right and diagram 'B' below portray the log expanded video colorized. This is accomplished by first digitizing the expanded video to 8 bits and inputting the digitized video into the OEI #6730 Calorized Module. The coloration is determined by a user accessible Eprom.



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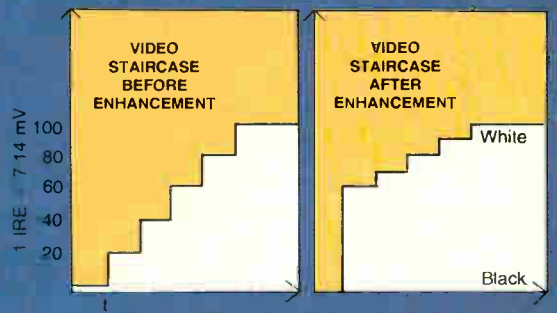
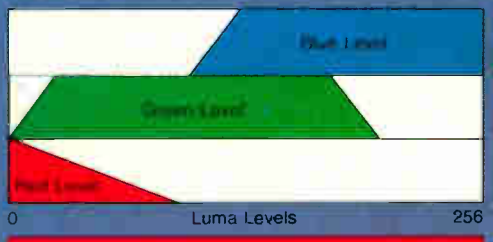


DIAGRAM B



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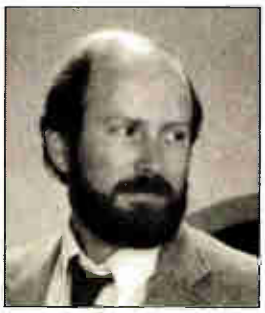
PUBLISHER'S LETTER

In this issue we show off two of our unique strengths: the ability to turn around fast with an in-depth treatment of a subject, and the knack for spotting trends and following them. The subject is fast static RAMs; the coverage package begins on p. 60.



J. ROBERT LINEBACK

As we've said many times, our readers gain a lot by our newsweekly editorial closings; we constantly write late-breaking stories that our readers will see just a few days later. Not one of our magazine competitors can do this. Though some of the industry tabloids can turn around as fast, they do it only with announcements, no value-added interpretation or analysis.

Many of our competitors, in fact, have to finish writing and editing their stories a month or two before their readers see them, actually before the *Electronics* staff even begins work on most of its editorial pages. This point was never driven home harder than by the nine-page package on fast static RAMs starting on p. 60. Some parts got started in late May, but we didn't decide to do a full-blown worldwide overview with several articles until late June; work didn't begin on several stories until that time.

Consider also the way we adhere to that oldest of journalism rules: a good reporter follows up. We said a year ago [*Electronics*, Aug. 7, 1986, p. 121] that the static RAM business is a fast-moving, fast-changing market. That's why a good reporter by the name of J. Robert Lineback, our Dallas bureau manager, was the lead man on the package.

"When I did the piece last summer, I knew that I'd be working on this one again. Everyone I talked to was full of enthusiasm," he says.

"Last year, the big story was that more than 20 companies were crowding into a small but rapidly growing segment of the semiconductor industry. There were two interesting questions then: why were they doing it, and would they make any money at it? Each of them was jumping into what amounted to a speed race, and they were all very aggressive about turning out 256-Kbit devices with 25-ns access times.

"Now the tune is somewhat slower and more serious. They have found out all that work to design faster SRAMs than the next guy isn't enough; now they have to deal with the problems we explore in our stories. Basically, in 1986 everyone was talking about what was *going to be* shipped; now they're talking about what *is* being shipped."

Another important aspect of Rob's follow-up is marketing strategy—what might be called the TI factor. He says, "Since TI appeared in the story last year, every SRAM producer I've visited in the course of covering my beat has wanted to know what the big guys in Dallas were up to. You could sense a certain apprehension that TI might be shifting its emphasis from dynamic to static RAMs." So we have not only updated the overall picture, but we have done a story on TI's marketing strategy [p. 65] as well as one on its technology [p. 63]. And rounding out the package is Bernie Cole's piece on the Motorola chip architecture [p. 66].

Needless to say, this isn't the end of the story. As Rob puts it, "This is shaping up as one of those ongoing stories where the follow-ups can be more interesting and exciting than the original story. I'm still following up."

Laurence Altman

July 23, 1987 Volume 60, Number 15
149,677 copies of this issue printed

Electronics (ISSN 0883-4989). Published biweekly by McGraw-Hill Inc. Publication office: 1221 Avenue of the Americas, N. Y., N.Y. 10020; second class postage paid at New York, New York and additional mailing offices. Postage paid at Montreal, P. Q. Registration Number 9034.

Executive, editorial, circulation, and advertising addresses: Electronics, McGraw-Hill Building, 1221 Avenue of the Americas, New York, N.Y. 10020. Telephone (212) 512-2000. Teletype 12-7960 TWX 710-581-4879. Cable address: M C G R A W H I L L N E W Y O R K.

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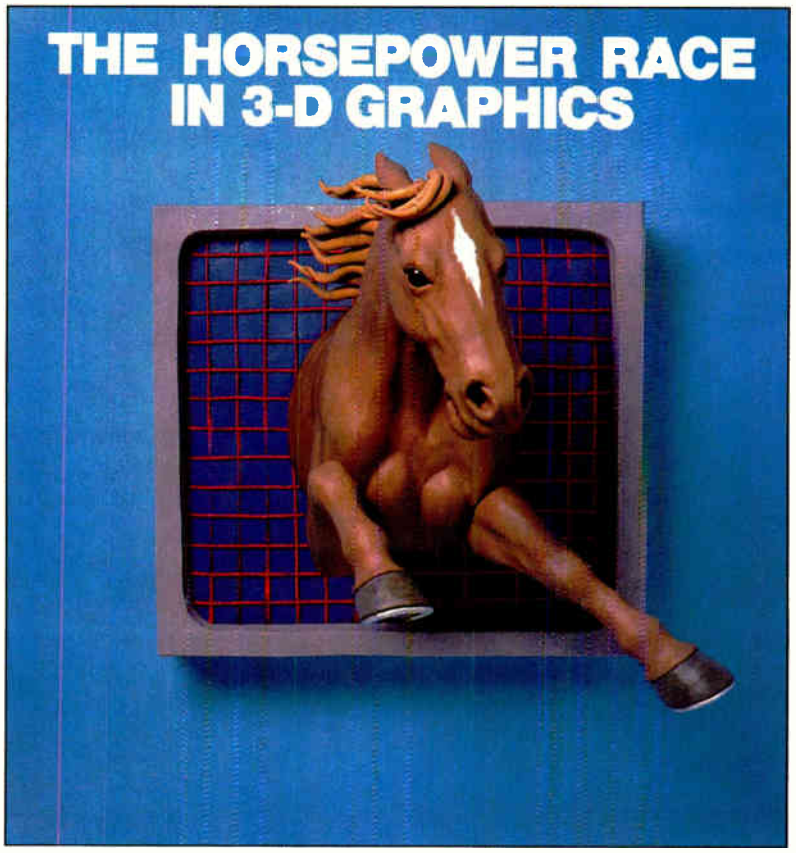

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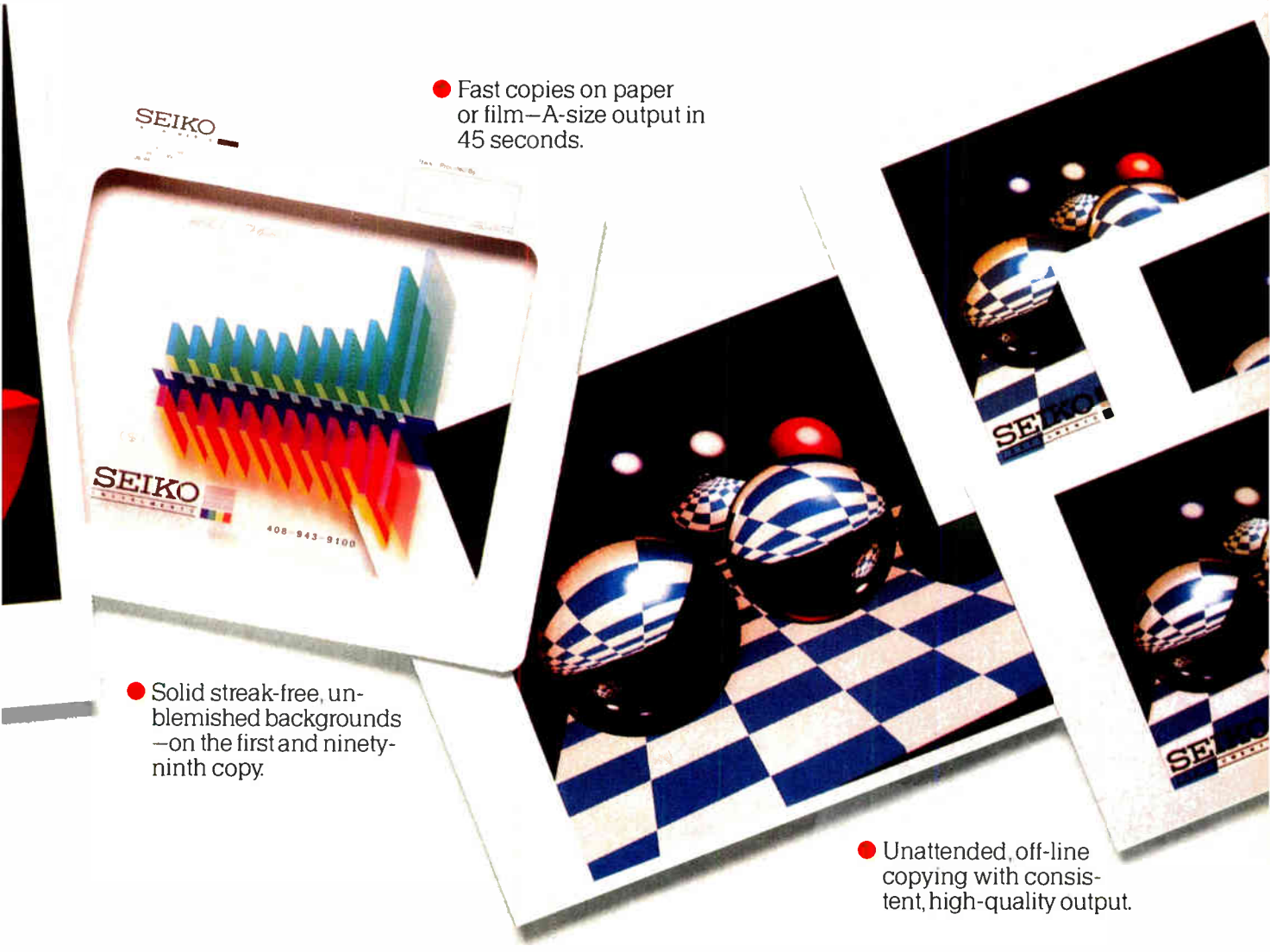

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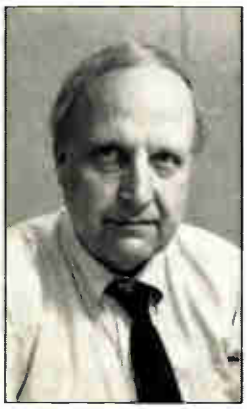
FYI

National's Sporck: The assumption that processes intended for high-volume production can be learned adequately by Sematech only in a high-volume environment is wrong



Charlie Sporck, National Semiconductor CEO and spark plug behind Sematech, writes: "I was distressed at the reservation you expressed [*Electronics*, June 25, 1987, p. 8] about the consortium's chances for success. Your consultant appears to believe that processes intended for high-volume production can be learned adequately only in a high-volume environment. This assumption is wrong. It's possible to learn and prove new manufacturing processes in a small-scale piloting facility, as long as the processing equipment and operating conditions are properly selected. Sematech intends to use such a facility, operating it seven days a week to simulate the intensity of large-volume manufacturing. Small-scale piloting offers the most efficient way to achieve Sematech's goal."

And David J. Littleboy, NEC Corp. researcher, writes from Tokyo to grump about our June 11 column. "The highly questionable conclusion that a growing emergence of nationalistic feelings [in Japan] is becoming a serious problem for U. S. companies is based on an event in which management of a Japanese company decided to purchase an American product, then claimed it was forced to back down because of worker and middle-management opposition. I find this story hard to accept.

"My NEC group conducts work on Sun, DEC, and Symbolics equipment, and a nearby group purchases Motorola 68020s as fast as it can get them. Despite stories of consensus decision making, there seems to be very little real decision-making power at the lower levels of the system. Thus the excuse 'our workers wouldn't let us do it' rings extremely hollow to my ears. Invoking worker nationalism was most likely merely a facile excuse and should not be used as a basis for generalizations about Japanese society.

"While there is room for improvement on the Japanese side, even within the present economic constraints, until the U. S. institutes policies that make it favorable for Japanese multinational firms to repatriate their U. S. earnings, the bottom line will be that with the profits of their labor remaining in the U. S. financial markets, the Japanese worker and company alike do not have the option of substantially increased consumption of imported goods. And our trade negotiators and salesmen will continue to hear easily misinterpretable excuses."

ROBERT W. HENKEL

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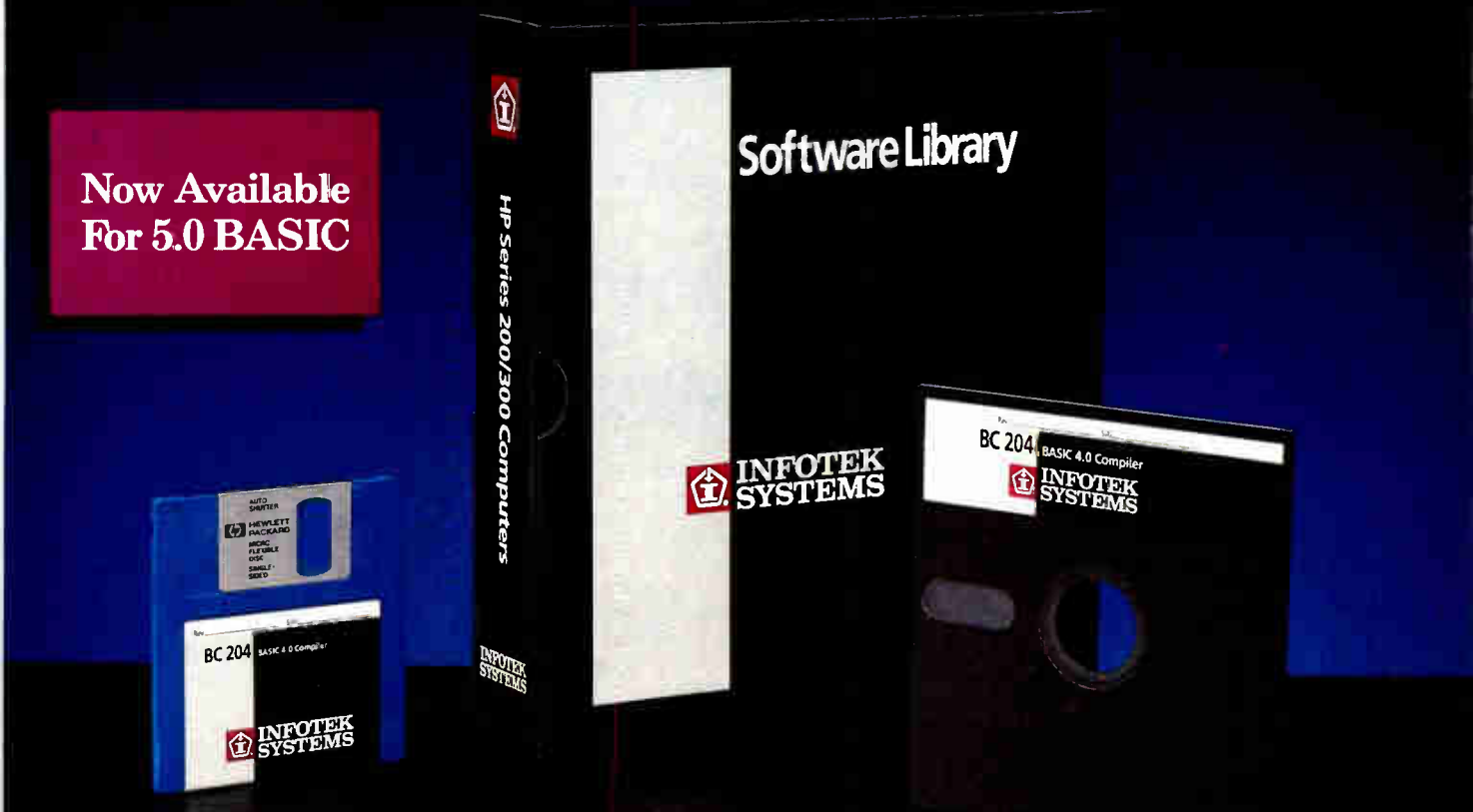

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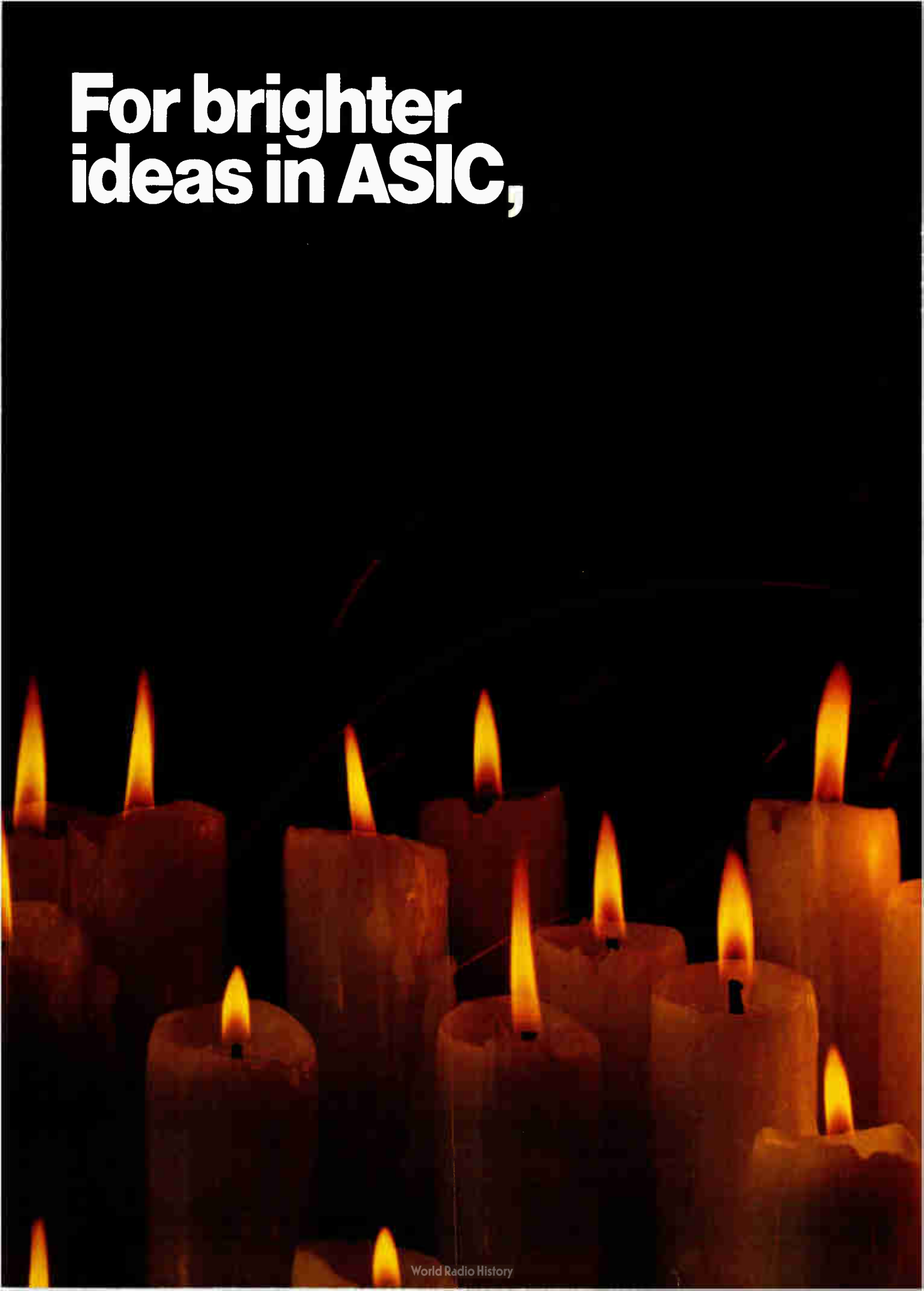

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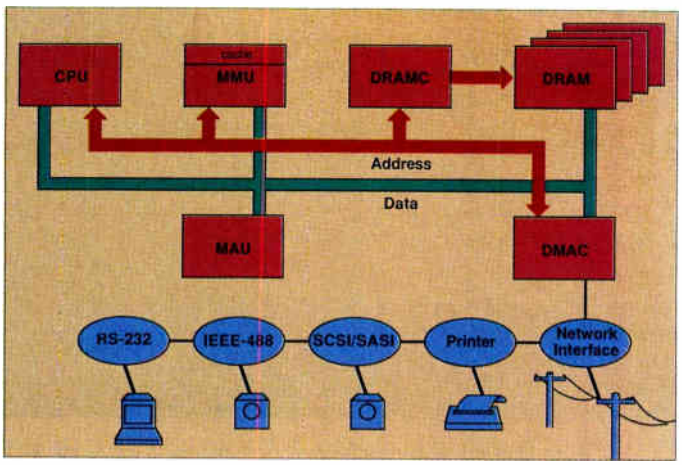
But with a system so advanced, the heart is only the start of it.

AT&T's WE 32201 Memory Management Unit (MMU) incorporates an unprecedented 4 Kbyte on-chip data cache, supports zero-wait-state virtual accesses at up to 30 MHz, and greatly reduces CPU overhead. This MMU has a variety of protection mechanisms to maintain system integrity. It is a 400,000-transistor testimonial to AT&T's technological leadership.



AT&T's newest system design offers a cache memory that runs at 20 to 30 MHz.

AT&T's WE 32206 Math Acceleration Unit (MAU) is today's fastest floating-point co-processor that meets the IEEE 754 standard. It performs at 3.5 MWhets/sec.

Add to this a 32-bit DRAM Controller that supports 1 MEG DRAMs and a DMA Controller with a super-high transfer rate: 14 Mbytes/sec. memory to memory at 18 MHz.

The final thirst quencher.
Upwardly compatible with the WE 32100 CPU, the WE 32200 Microprocessor chip set runs over 1,500 application programs, with more on the way. And AT&T offers all software development tools—including UNIX Operating System with optimized compilers for C, Fortran, Pascal, BASIC, and Cobol.

For more on how AT&T's WE 32200 Microprocessor chip set can help you bring top-line computer solutions to the multiuser/multitasking marketplace, call **1 800 372-CHIP.**

In Canada, call (collect) **215 266-2975 or 2977.**

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Or write to AT&T, Dept. LT, 555 Union Blvd., Allentown, PA 18103.

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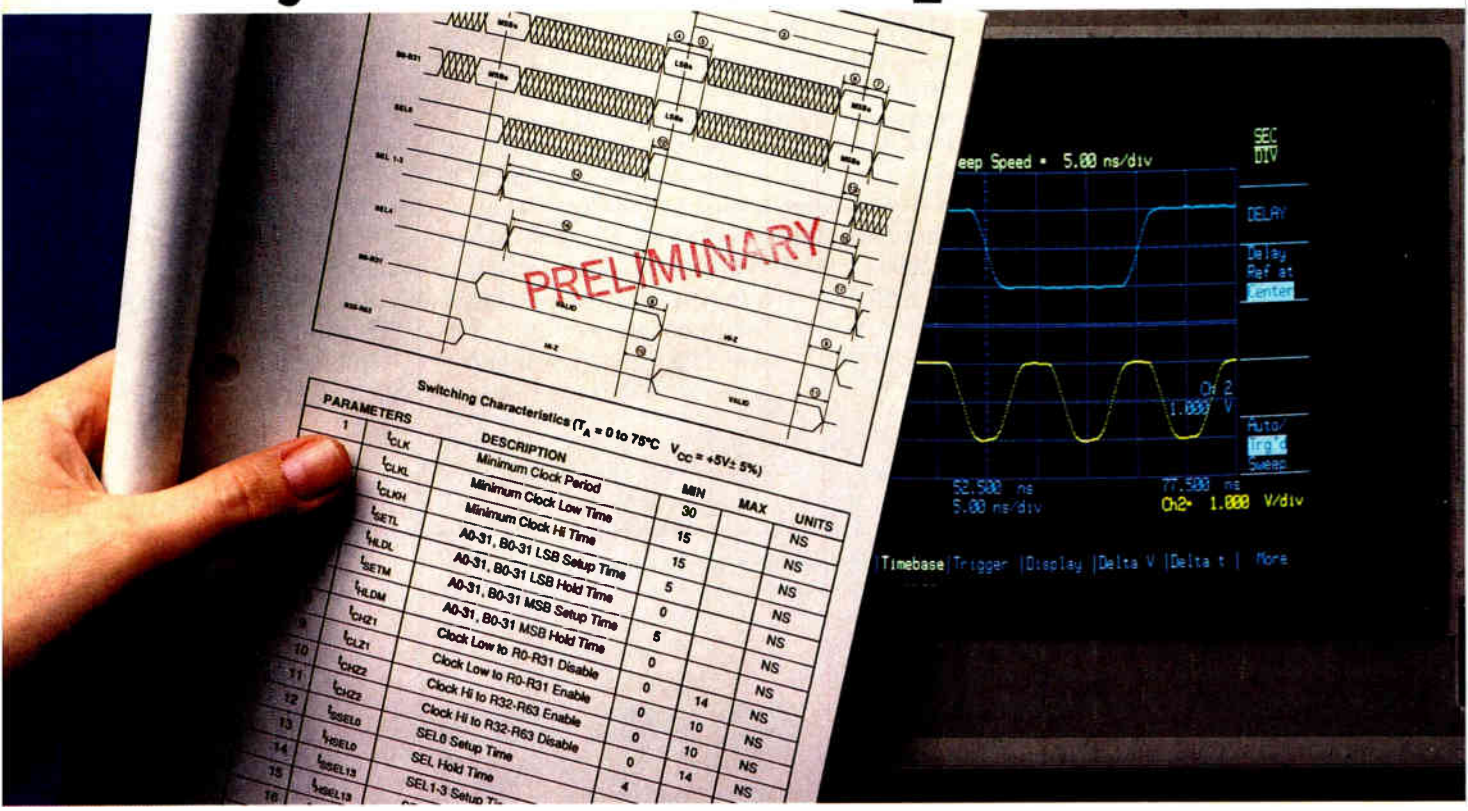

Teradyne J953 VLSI test system waveforms observed with a 1GHz digitizing oscilloscope.

The fastest silicon debug and characterization—that's what you get with Teradyne's new J953 VLSI test system. It moves your advanced devices to market faster, and gets them there fully tested and guaranteed to meet every parameter of every specification.

The J953 is faster than any other test system because its full performance hardware and innovative software remove the obstacles that slow down verification of specs.

A 100 MHz timing system, with independent timing generators for each pin, tests your parts at full speed, putting the edges precisely where your spec sheet requires them. Waveforms on every pin can be changed on the fly, in every cycle. And guardbanding can be virtually eliminated, because test system edges are always placed where you want them, with fewer than 250 picoseconds of error.

The software is Teradyne's IG900, a mouse-driven, graphics-oriented, interactive interface. IG900 organizes your test plans in the form of spec sheet data, using the same spec sheet language consistently for creating, debugging and characterization. IG900 lets you see and analyze relationships in your devices faster than you ever have before.

So, if you are in a hurry to get your fastest, most advanced devices into your customers' hands, get your hands on the J953. Call or write Teradyne today.

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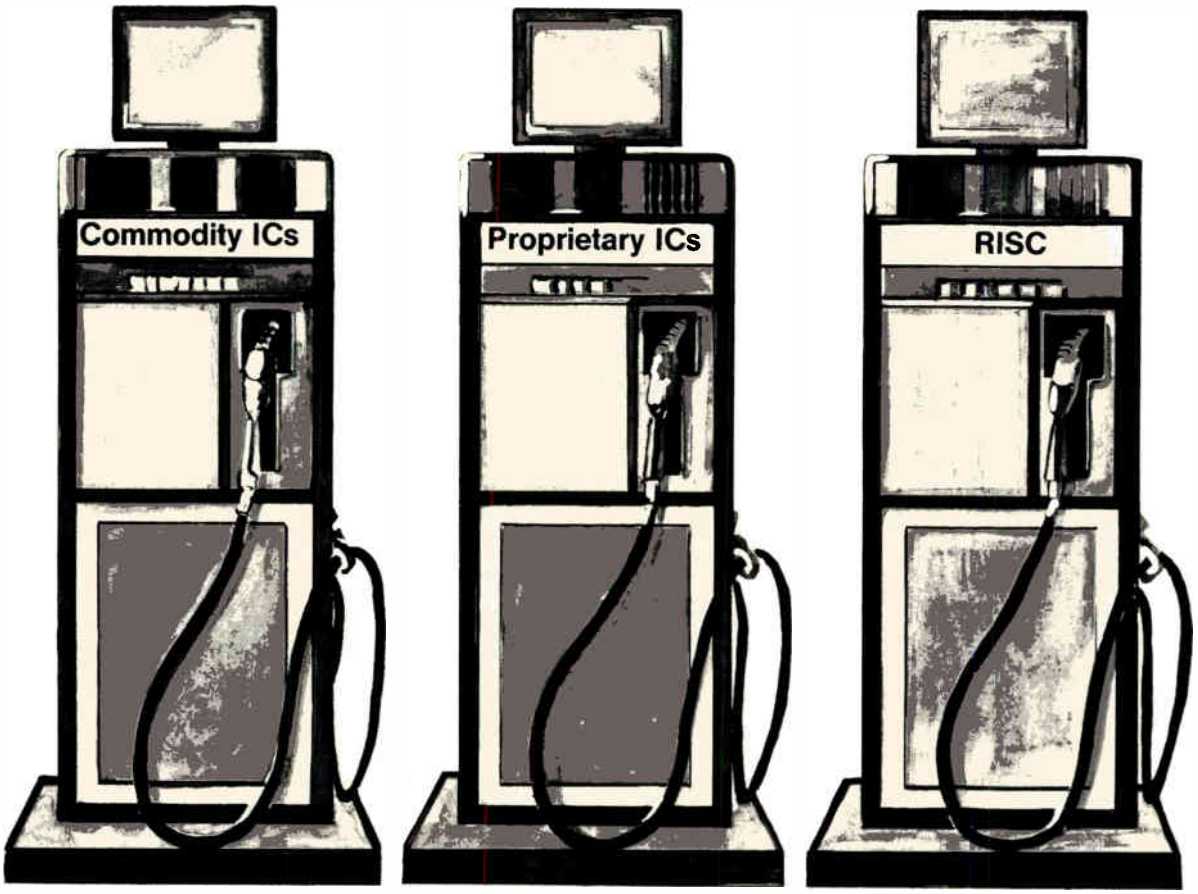

In the September 3rd issue, the editors of *Electronics* magazine take a close look at what's fueling the drive for better performance in computer systems.

Commodity ICs?

Proprietary ICs?

RISC?

Today's systems designers are faced with a myriad of choices when looking to design in greater performance for their computer systems. Should they wait for IC manufacturers to develop the next generation of devices? Should they design their own? Or develop systems based on Reduced Instruction Set Computer (RISC) architectures?

In this special report, readers will get an in-depth look at the pros and cons of the various approaches being considered in the U.S. and in Europe.

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8086	8035	68HC11A2	6801		6301X		6504		1806		Z80H
8088	8039	68HC11A8	6802		6301Y		6505		CDP6805C4		Z180
80186	8344		68B02		6303R		6506		CDP6805C8		Z8001
80188	8048	68000	146805E2		6305V		6507		CDP6805D2		Z8002
80286	8049	68008	6803		63705		6512		CDP6805E3		
	8050	68010	6808		6309		6513	**Harris:**	80C86	**NEC:**	V20
	8051		68B08		6309E		6514		80C88		V30
	8085A		6809		64180R		6515	**National:**		**Signetics:**	8X300
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ELECTRONICS NEWSLETTER

MACHINE-VISION SALES FORECAST WILL BE SCALED BACK...

The Automated Vision Association, Ann Arbor, Mich., is expected to scale back growth projections for machine-vision sales when a revised AVA-commissioned market study comes out this fall. The original report, issued more than a year ago [*Electronics*, April 7, 1986, p. 11], was based on surveys taken before the bottom dropped out of the machine-vision business when General Motors Corp. and others cut back automation spending and cancelled orders. The 1986 report—the first industry-generated study of the machine-vision business—projected 62% annual growth for machine-vision sales, from $58 million in 1985 to $457 million in 1990. The revised study, however, is expected to project annual growth in the 20% to 30% range through 1995. Others paint a rosier picture. Electronic Trend Publications, a Saratoga, Calif., market research firm, projects that machine-vision sales will grow 48.3% annually, from $85 million in 1986 to $610 million by 1991. □

...AS THE FIRST STEPS ARE TAKEN TO ESTABLISH INDUSTRY STANDARDS

A subcommittee of the Automated Vision Association is about to produce the first in a planned series of draft performance standards for machine-vision equipment. The document is a first step in helping users and vendors to match a given vision system to a specific factory task. Standard test methods for measuring accuracy, repeatability, cycle time, and steady-state rate will be specified for two-dimensional machine-vision systems. The draft, which has been in the works for about a year [*Electronics*, July 10, 1986, p. 19], will be sent to AVA members and to the American National Standards Institute for public review by late September. It could become an official standard next year. Additional documents covering other kinds of equipment, such as three-dimensional systems; components, such as cameras; and target applications, such as printed-circuit-board inspection, are expected to follow quickly, some before year-end. □

RPI DEVELOPING 'SUPER MICRO' THAT WOULD RUN 125 MIPS

Researchers at Rensselaer Polytechnic Institute, in Troy, N.Y., are using wafer-scale integration to develop what they call a "supermicrocomputer" capable of running 125 million instructions per second. With funding and technology provided by General Electric Co., Tektronix Inc., and others, the RPI research group is implementing a reduced-instruction-set architecture on 11 silicon chips, which are then bonded to a silicon substrate using a boron-nitride polymer film. The substrate, a 3.4-by-3.4-cm wafer, acts like a printed-circuit board, connecting the 11 logic chips that make up the central processing unit. "Our goal is to produce a supermicrocomputer that you could hold in your hand and that would be suitable for work-station applications," says John McDonald, a professor in RPI's Electrical, Computer, and System Department. In a parallel effort, another RPI group is trying to implement the identical architecture in gallium arsenide technology. □

PRIME BROADENS 50 SERIES WITH NEW LOW-END COMPUTER

In a move to boost the performance of its low-end computer offerings, Prime Computer Inc. has added a third "desk-side" model to its 50 series of minicomputers. The model 2455 is a 32-bit machine that's capable of running 1.6 million instructions per second, outperforming its predecessor, the 2450, by 23%. The new model also has 50% more main-memory capacity than the 2450, offering 12 Mbytes of main storage. Priced at $62,810 for a typical configuration, the system is being marketed against Digital Equipment Corp.'s popular MicroVAX II minicomputers. □

ELECTRONICS NEWSLETTER

A PORTABLE AI STANDARD GETS CLOSER: COMMON LISP

IBM Corp. announced its support for Common Lisp, an artificial intelligence programming language, giving a huge boost to the drive toward a single, portable AI standard. Industry insiders are hoping IBM's blessing will do for Common Lisp—and AI in general—what it did for the personal-computer industry by making MS-DOS a de facto standard operating system. IBM is purchasing Common Lisp from Lucid Inc., the Menlo Park, Calif., AI software vendor that is already supplying IBM with a version of Common Lisp for its RT PC. IBM is releasing two Common Lisp programs: an Application Environment that lets users run existing Common Lisp applications, and a Development Environment that lets them develop new applications. The packages will cost $10,000 and $22,000, respectively. □

TI AND SYMBOLICS TAKE THEIR LISP CHIP BATTLE TO THE WORK STATION MARKET

The Lisp-chip processor war between silicon giant Texas Instruments Inc. and artificial-intelligence-hardware pioneer Symbolics Inc. is about to spill into the standard work station market. TI intends to use its new 32-bit Lisp chip to produce a series of plug-in coprocessor boards for popular work stations, such as those based on the Intel 80386 or Motorola 68020 microprocessors. Officials at TI's Data Systems Group in Austin, Texas, are now working on cooperative marketing pacts, which are expected to be announced in the next three to six months. Symbolics, of Concord, Mass., disclosed its "Ivory" Lisp-based chip in May. Engineers who were recently briefed on the subject say Symbolics is also aiming to have its circuit embedded as a coprocessor in standard engineering work stations. Symbolics officials, however, will say only that the Ivory chip will not be used in a product until 1988, when it debuts in the company's 3600 series. □

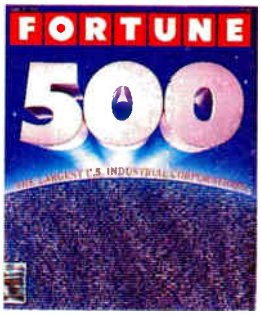
NATIONAL SEMICONDUCTOR PUSHES HARDER IN 32-BIT MICROPROCESSORS

National Semiconductor Corp. is stepping up its efforts to compete in the hotly contested 32-bit microprocessor market with a series of moves aimed at extending the reach of its 32000 family. First silicon is finally coming through on the company's high-end 32532 chip, and the company is planning to release a series of new products, including development tools, an Ada compiler validated by the Defense Department, a VME board based on the 32532, and a floating-point coprocessor. Both the 532 and its coprocessor, the 32381, will be offered in sample quantities this fall in 20-MHz versions; 30-MHz versions will follow later. The VME board is also slated for fall arrival.□

IS LOCKHEED GETTING OUT OF COMMERCIAL ELECTRONICS?

Lockheed Corp. may be backing off its efforts to build a stake in commercial electronics. Analysts familiar with the company say Lockheed is on the verge of selling its CalComp subsidiary, which accounts for a little more than half of its Information Systems Group's $700 million in annual sales. Lockheed announced in mid-July that it plans to sell most of its shipbuilding businesses, the first phase of a restructuring plan aimed at focusing the company's business on the defense industry. A graphics equipment maker, CalComp has had pre-tax profit margins of more than 10% since William Conlin took over as president in 1983. The company was a subsidiary of Sanders Associates Inc. until Lockheed acquired Sanders last year. Lockheed won't say what else is on the auction block, but Lawrence Harris, an analyst with Bateman Eichler, Hill Richards Inc. of Los Angeles says he believes Lockheed plans to sell most of the Information Systems Group. Harris says Lockheed is afraid that it might be the target of an unfriendly takeover. □

THINK...



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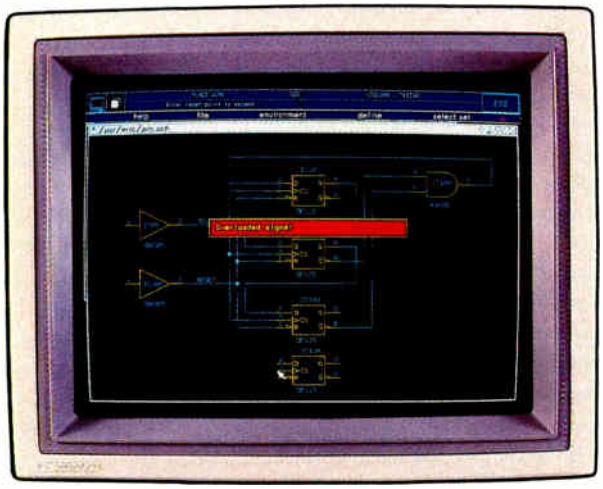
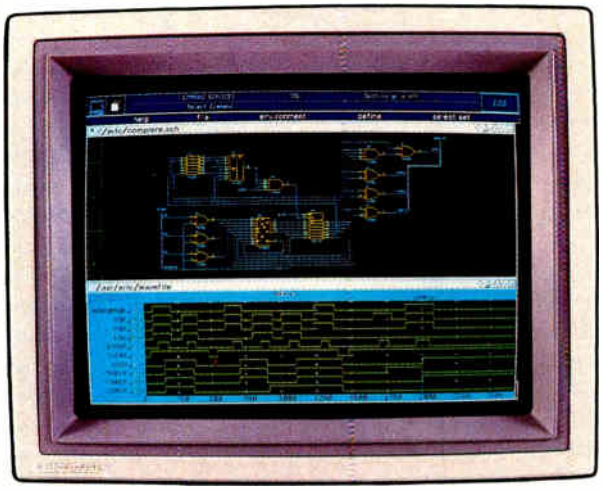
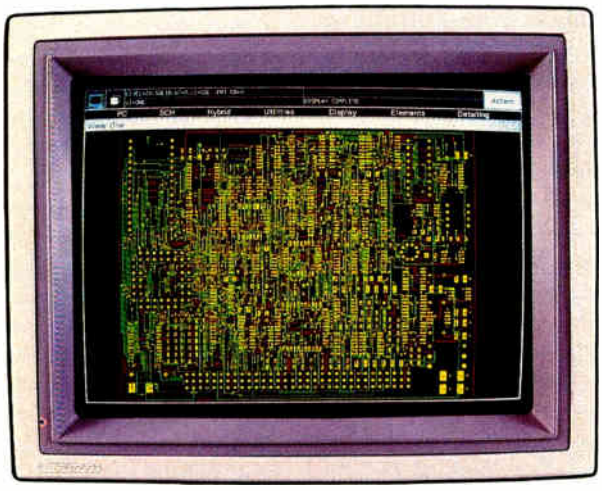


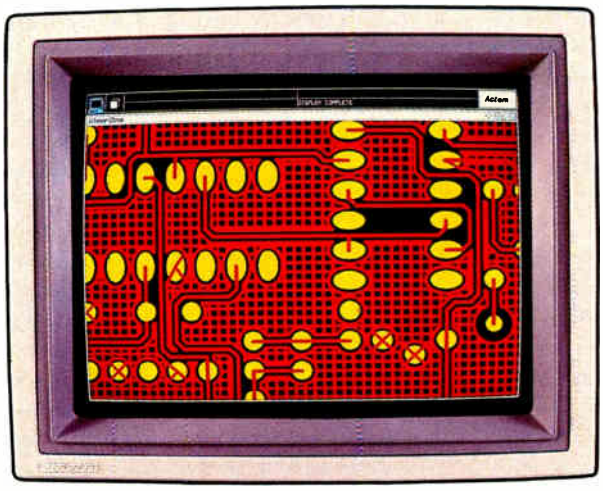
Create schematics faster with correct-by-construction design and on-line Electrical Rules Checking



Logic analyzer type display for interactive digital analysis using HILO-3®



Begin PCB design with a feasibility check, then rely on a full suite of tools for autoplacement, high-completion autorouting, and design rule checking



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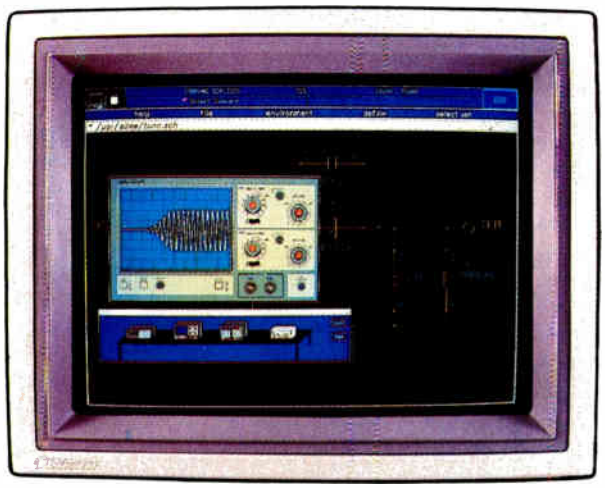
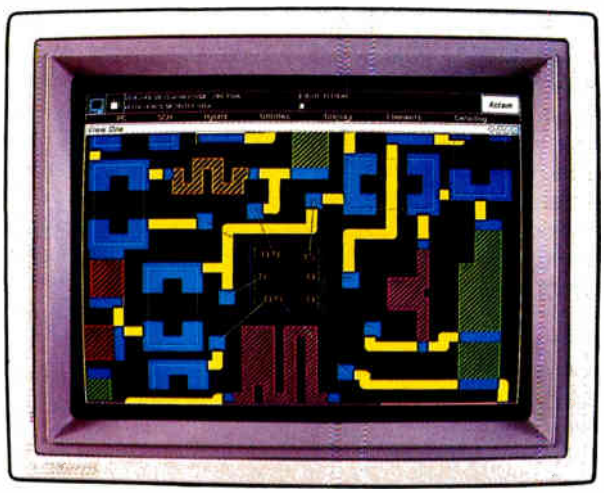
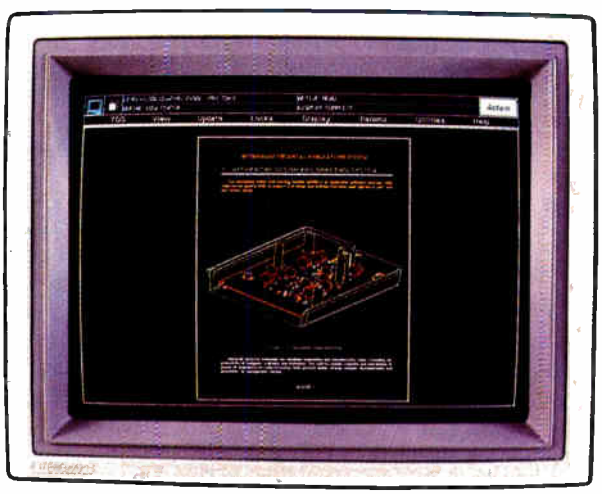


Easy-to-use virtual instruments provide a familiar interface for analog analysis using Intergraph's Cspice or ACS

Reduce ASIC die size and improve yield with Tangent Systems' timing-driven layout, automatic design for testability, and test pattern generation



A dedicated package for thick and thin film hybrid design features automatic resistor generation and automatic routing of chip and wire parts and SMDs



64-bit mechanical design packages and electronic publishing software round out a system for total product development

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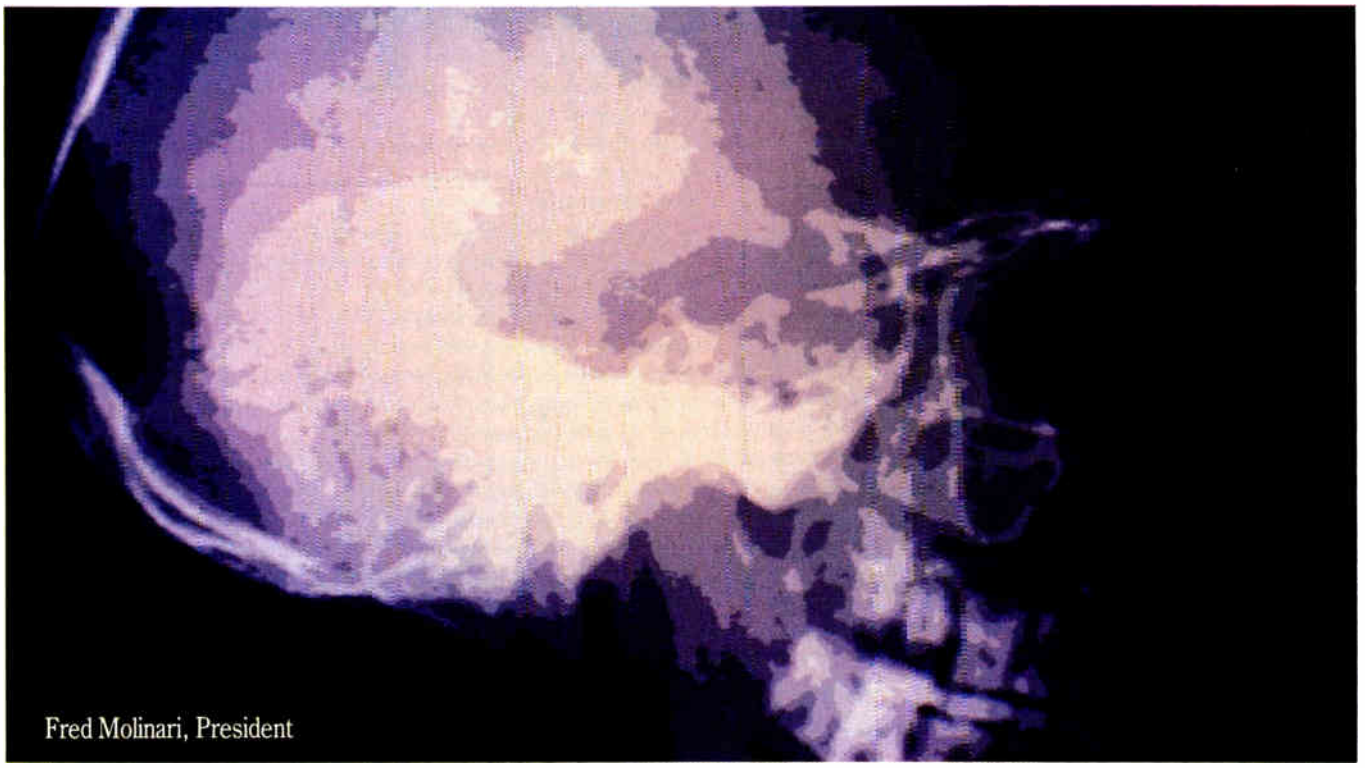

Model	Resolution	On-Board Memory	Real-Time Processing	On-Board Processor	Software Support	Price
DT2861 Frame Grabber	512x512x8	4 Mbytes (16 images)	✓	8-bit ALU	IRIStutor (free) DT-IRIS ($995)	$4995
DT2858 Frame Processor		512 Kbytes		16-bit ALU		$1695
DT2861 Frame Grabber	512x512x8	4 Mbytes	✓	8-bit ALU	IRIStutor (free) DT-IRIS ($995)	$4995
DT7020 Array Processor		4 Mbytes		32-bit AM 29325	Vector Library ($1495)	$6595
DT2851 Frame Grabber	512x512x8	512 Kbytes (2 images)	✓	LUT Processor	IRIStutor (free) DT-IRIS ($995) PC Semper ($1995)	$2995
DT2858 Frame Processor		512 Kbytes		16-bit ALU	DT/Image-Pro ($1495)	$1695
DT2851 Frame Grabber	512x512x8	512 Kbytes	✓	LUT Processor	IRIStutor (free) DT-IRIS ($995)	$2995
DT7020 Array Processor		4 Mbytes		32-bit AM 29325	Vector Library ($1495)	$6595
DT2853 Frame Grabber	512x512x8	512 Kbytes	✓	LUT Processor	IRIStutor (free) DT-IRIS ($695) DT/Image-Pro ($995)	$1595
DT2803 Frame Grabber	256x256x6	64 Kbytes			Videolab ($995) PC Semper ($1495)	$M95

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Are we out of our skull? Data Translation's Image Processing boards and software for the IBM PC, XT, and AT are priced below the competition's, but offer a wider range of functions.

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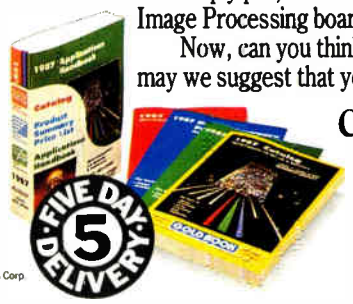
And so is Data Translation. We're selling a lot of Image Processing boards and software for PCs, for reasons other than price: Full-functionality-on-one board; Real-time processing; Different resolutions for different applications; Standard video, VCR, or slow-scan capability; Application and subroutine library software.

Simply put, Data Translation has the best values on Image Processing boards and software for PCs.

Now, can you think of using anyone else's? If so, may we suggest that you have your head examined?



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PRODUCTS NEWSLETTER

CLONE CHIPS BOOST PERFORMANCE 25% OVER IBM'S PS/2 MODEL 30

A new family of ICs from Chips and Technologies Inc. gives clone makers a clear shot at IBM Corp.'s 8-MHz PS/2 Model 30 while hiking performance 25% and cutting chip count in half. Using the 10-MHz 82C100 logic chip, the 82C606 peripheral-controller chip, and the 82C764A floppy-disk data-separator chip, a complete PS/2 Model 30-compatible system needs fewer than 25 chips (plus memory) instead of the PS/2's 45 chips, says the Milpitas, Calif., company. The 82C100 runs with Intel Corp.'s 8088 and 8086 microprocessors and NEC Electronics Inc.'s V20 and V30 microprocessors. It can also support an expanded memory capability—2.5 Mbytes instead of the standard 640 Kbytes—and incorporates dual-clock and power-management features for laptops which will help reduce battery consumption. Clone makers targeting IBM's 5-MHz PC XTs can harness the new 10-MHz 82C101 logic chip to the 82C606 and 82C764A and double the XT's performance. Available in sample quantities in August, the 82C100 will cost $51.30; the 82C101, $41.10; the 82C606, $23.40; and the 82C764A, $7.80. □

TI's 6-ns PROGRAMMABLE LOGIC GOES HEAD-TO-HEAD WITH NATIONAL'S LINE

Texas Instruments Inc. has jumped into the market for programmable emitter-coupled-logic arrays with a 6-ns device that poses a head-on challenge to National Semiconductor Corp.'s 10-K ECL parts. Pin- and fuse-compatible with National's 16P8 series, which follow Monolithic Memories Inc.'s Programmable Array Logic architecture, TI's 24-pin TIEPAL10H16P8-6 features a dozen dedicated inputs and four standard outputs, plus four input-output ports. Its programmable output-polarity fuses let designers change output polarity from active high to active low. Security fuses also can be set to prevent duplication of the designs. TI product engineers say the 10H16P8-6 has shown 99% programming yields. Available now, it costs $19.78 each in 1,000-piece quantities in 300-mil-wide ceramic dual in-line packages. Look for TI to unveil a programmable 6-ns 100-K ECL device late this summer. □

ARRAY PROCESSOR MAKES SYMBOLICS LISP COMPUTER RUN AT 20 MEGAFLOPS

An array-processor board from Symbolics Inc. gives a 40-fold number-crunching boost to the company's 3600-series Lisp computers—providing graphics-oriented performance 2 to 10 times greater than general-purpose computers that cost three to seven times as much. The Aproc 110's parallel-pipelined design can transform 200,000 3-d vectors/s. It handles up to 20 million 32-bit single-precision floating-point operations/s—10 million multiplications/s and 10 million additions/s when the two functions run simultaneously. Up to four boards can be added to attain 80 megaflops, with the boards communicating at 40 Mbytes/s over a private bus. Pricing is not yet set, says the company's Los Angeles graphics division, but the 110 will cost less than $20,000 when it arrives in the third quarter. □

RASTER TECHNOLOGIES BOOSTS ITS GRAPHICS PROCESSOR SPEED BY 133%

A floating-point processor architecture optimized for running three-dimensional graphics algorithms is the key to increased performance in Raster Technologies Inc.'s Model One/385 graphics processor. The 385 executes 140,000 10-pixel 3-d vectors/s—compared with 60,000 vectors/s for its predecessor, the Model One/380. Compatible with previous Model One family members, the 385 is especially suited for 2-d and 3-d applications. Prices for the six-slot, rack-mounting device begin at $33,000, substantially less than the 380's $39,550 price tag, and $2,000 under the closest competitive processor, says the Westford, Mass., firm. Deliveries will begin in the fourth quarter. □

PRODUCTS NEWSLETTER

CDC'S 8-IN. DISK DRIVE BEATS OUT FUJITSU ON CAPACITY

The Sabre-IV 8-in. disk drive from Control Data Corp. packs 750 Mbytes of unformatted capacity—9% more than industry leader Fujitsu Ltd.'s M2344K drive. Sabre-IV's 19.72-Mbyte/s data-transfer rate and price also compete favorably with the M2344K, says the Minneapolis firm. It joins three other Control Data 8-in. drives, known previously as the EMD family, and will provide an easy upgrade path for users of the Sabre-II, a 500-Mbyte system introduced last November that also supports 19.72-Mbyte/s transfers. Other family members have 368 Mbytes and 741 Mbytes of unformatted capacity and a 14.52-Mbyte/s transfer rate. The Sabre-IV will support any of three interfaces—SMD-E (Storage Module Drive—Enhanced), SCSI (Small Computer Systems Interface), or IPI-2 (Intelligent Peripheral Interface). It is available in evaluation quantities now, with production deliveries set to begin in the fourth quarter. In quantities of 250, the Sabre-IV will sell for $4,260. □

SIEMENS CUTS COSTS 20% BY SQUEEZING TWO ISDN ICs ONTO ONE CHIP...

Designers of communications equipment for Integrated Services Digital Networks can save about 20% on chip costs and 50% on space requirements with Siemens AG's PEB2085 ISDN subscriber-access controller. The new device does it by integrating all the functions on two ISDN chips that Siemens introduced last year: the PEB2070, which switches the two 64-Kbit/s user channels, and the PEB2080, which organizes four-wire connections. Fabricated in 2-μm CMOS technology and housed in a 40-pin dual in-line package, the PEB2085 integrates 31,000 transistors on a 31-mm^2 chip. Samples costing $30 each are available now in the U. S. from Siemens' components marketing headquarters in Santa Clara, Calif. The price will drop to $21 each in 1,000-unit buys when production gears up early next year. □

...AND REPLACES DISCRETE MODEM CIRCUITRY IN MAP SYSTEMS WITH ONE IC

Implementing the Manufacturing Automation Protocol will be less expensive with a new chip from Siemens AG that does away with expensive discrete modem circuitry by modulating and demodulating signals between terminals and a token-bus local-area network. The 36-mm^2 bipolar SAB82511 integrates the complete first layer for seven-layer Open Systems Interconnection communications. Coding, transmitting, and station-management circuitry, as well as a clock generator, are also on the chip. A 2½-by-2½-in. board holding the 82511 and six passive devices consumes 1.5 W—compared with 10 W for a discrete modem using dozens of chips. The Munich, West Germany, company's 44-pin MAP modem IC corresponds to the IEEE 802.4 standard and is compatible with any token-bus controller with a standard interface. Samples will be available this summer for about $75 each, with production set for early next year. □

REGULUS SYSTEMS MARRIES VMEBUS TO MULTIBUS

Systems designers with an extensive inventory of board designs compatible with Intel Corp.'s Multibus I architecture now can migrate to Motorola Inc.'s advanced VMEbus in a snap. Just by snapping Regulus Systems Corp.'s VMA1 board in between the two systems, they can bridge them with little performance degradation. Conversion typically takes no more than 10 clock cycles, or about a microsecond, says the Foster City, Calif., company. The VMA1 board plugs directly into one VME slot, and the Multibus board plugs into a multibus connector on the larger board. Controlled by a finite-state machine implemented in programmable logic arrays, the VMA1 card translates memory address and interrupt vectors, and maintains byte/word orders between the VME and Multibus. The board costs $600 and is available now. □

ROGERS Q/PAC® COMPONENTS SUPPRESS NOISE

Q/Pac® components from Rogers. High capacitance, ultra-efficient power distribution for today's increasingly dense logic and memory boards. All in a single, compact package. Here's how.

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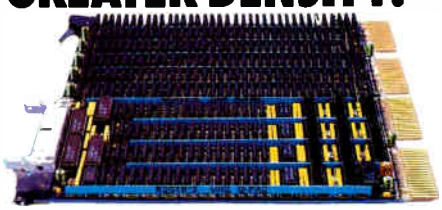

Board courtesy of *Intergraph*

Q/Pac makes it simple. You put the power distribution on top of your board. So you save board space for signal traces. With no wasted space for power and ground traces. Makes your boards simpler, more compact, more efficient.

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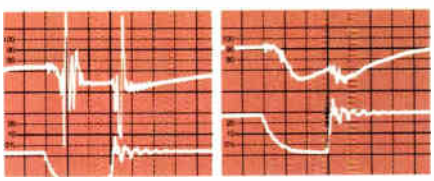

Left trace: Shows 2-layer board noise with .1 μF ceramic monolithic capacitor at every RAM.
Right trace: Shows .04 μF Q/Pac at every RAM.

Only Q/Pac gives you low inductance. And, high capacitance. For quiet, error-free operation. Now, 2-layer boards perform electrically as well as 3 and 4-layer boards of similar density.

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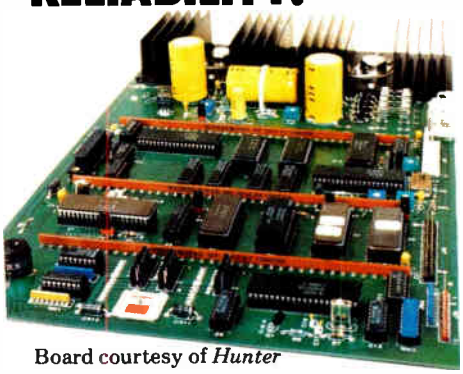

Board courtesy of *Hunter*

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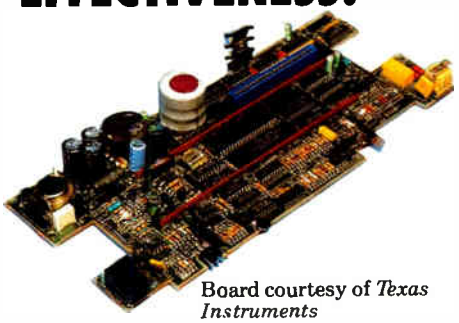

Board courtesy of *Texas Instruments*

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Electronics

INTEL LAUNCHES MAJOR ASSAULT ON REAL-TIME SYSTEMS BUSINESS

ITS 386-BASED PRODUCTS GO AFTER MARKET LEADERS—DEC, IBM, GOULD

HILLSBORO, ORE.

Intel Corp.'s 80386 32-bit microprocessor chip has already had a profound influence on what people can do with general-purpose microcomputers. Now Intel hopes to have the same impact on real-time computing with 80386-based boards and systems, plus an enhanced real-time operating system.

The company's Systems Division, in Hillsboro, Ore., has its eye on a healthy market. According to Dataquest Inc., the market for real-time systems is $2.6 billion; boards add another $600 million to that. The growth rate for the market as a whole is 9% to 10% in revenue but 30% in unit volume. This reflects increased sales of less expensive single-board models.

What's more, the market has a very broad base, buffering it against the slides that niche markets can suffer. An analysis of Intel's design wins in 1986 showed that 35% of real-time applications were for machine controllers, 22% for military and government, 16% in data acquisition, 8% in data communications, and 7% in office and business.

Now, armed with the 80386 and a leading real-time operating system, the company intends to make a real run at the market, where it currently ranks behind Digital Equipment Corp., IBM Corp., and Gould Computer Systems (in boards, Intel leads with a 35% share).

Brad Smith, associate director of Dataquest, says the iRMX-386 operating system makes Intel a formidable competitor in the real-time embedded-systems marketplace. "With the 80386 and iRMX-386, Intel is doing to the real-time computer market what the personal computer did for the general-purpose computer market," he says. "They are providing a $3,000-to-$5,000 solution to problems that up to now were solved with minicomputers and superminis costing over $100,000."

Smith believes all of Intel's competitors are now threatened. "Digital Equipment has a single-board computer that competes against the Intel board products, but it provides 0.9-mips performance, as compared with the 3 to 5 mips of the 80386," he explains. And Motorola—which in its 68020 microprocessor has a chip in the performance range of the 80386, and which offers a line of board-level products—does not offer a real-time operating system.

PUTTING IT TOGETHER. Intel, as part of its drive in real-time processing, is packaging its iRMX-386 operating system with its 80386 microprocessor into the System 320 microcomputer.

Smith says Hewlett-Packard Co. remains competitive with its 68020-based real-time computer systems costing $5,000 to $10,000. They run a real-time operating system called MPE.

Then there is the formidable presence of IBM, which has moved into the real-time arena with a ruggedized version of its Personal Computer. "The drawback IBM has is the PC bus," says Smith. "It was not designed as a real-time bus, as the Multibus was." Nor can the MS-DOS operating system handle true real-time processing. Smith points out that even should IBM build a rugged version of the Personal System 2 with the 80386, it would need a real-time operating system to be truly competitive with the new offerings from Intel.

In unveiling the iRMX-386 on July 7, Intel surrounded it with the makings of a complete real-time line. That includes a 386-based microcomputer system, the System 320, and networking software.

The operating system offers a richer set of services for real-time applications than those found in previous versions. For example, a key concern in real-time processing is interrupt handling. The iRMX-386 deals with that by immediately switching control to the user-written interrupt-handler routine when an interrupt occurs. The result is an average interrupt latency—the time it takes to process an interrupt—of 10 μs.

BETTER PROTECTION. Also, the iRMX-386 speeds chip performance by supporting 32-bit protected-mode 80386 operation and the 4-gigabyte unsegmented main-memory address space of the 32-bit chip. Previously, the main memory was segmented into 64-Kbyte sections, which slowed chip performance on larger applications.

Task management with the new operating system provides system calls to create, manage, and schedule tasks in a multitasking environment, while time management contains extensive alarms and a real-time clock. Inside the kernel are also mailboxes and semaphores to synchronize and communicate among tasks. *—Jonah McLeod*

WILL INTEL-TI DEAL SPEED STANDARDS?

SANTA CLARA, CALIF.

Everyone in the application-specific IC business is trying to figure out just what impact the sweeping five-year agreement closely linking the fortunes of Texas Instruments Inc. and Intel Corp. will have. To begin with, observers expect the joint approach in CMOS devices by two of the largest U. S. chip houses to speed standardization in a field that sorely needs it, fragmented as it is among upwards of 200 vendors and a dizzying selection of design options. On the negative side, they question whether two huge companies, each of which considers itself a top gun, can coexist peacefully, regardless of what the July 7 agreement says.

For the two companies, standardization assumes the highest priority. "Putting TI and Intel's name on a standard will help set a clear direction for the ASIC market," says Jack C. Carsten, Intel senior vice president and general manager of its ASIC Components organization. "This agreement can help allay customer confusion by establishing new ASIC standards for all maker to work toward," he adds. But their motivation isn't pure altruism: they know that a better-ordered ASIC business can only help the biggest suppliers.

Industry analysts agree on the need for standards, but they are equally intrigued by other provisions of the agreement. Among these are developing a common cell library, making current CMOS processes compatible, and jointly developing a 1-μm process by next year. Combining the 150 cells in Intel's VLSiCELL library with the 200 in TI's TSC500 library should result in 200 small- and medium-scale-integration-level cells immediately, they say. As for processes, the 1-μm goal is likely to center around TI's more scalable EPIC technique (Enhanced Performance Implanted CMOS), which currently is in production at 1.2 μm. Intel's 445 CMOS process is at 1.5 μm.

But the question of whether the agreement can work remains. It may be "the most significant semiconductor agreement I've heard of," says William R. Strauss, president of Forward Concepts Inc. of Scottsdale, Ariz. But based on the evidence of the past decade, the odds are against such alliances between big chip companies. An ASIC deal in 1983 between National Semiconductor Corp. and Motorola Inc. failed, for example. A second-source link between Intel and Advanced Micro Devices Inc. broke up. Deals between supplier and customer, such as the one involving National and Xerox Corp., have a better chance, say the experts.

Not surprisingly, TI and Intel executives maintain that they have a good chance to succeed, for several reasons. For one thing, they say, they do not for the most part compete head-on. For another, their product lines complement each other: TI has what is probably the most comprehensive library of logic functions, and Intel needs those functions to support its industry-leading microprocessors and controllers.

Also, the new partners have put an immense amount of advance work into identifying differences and removing obstacles, says Wally Rhines, senior vice president of the TI Semiconductor Group. The joint work, which amounts to several man-years of effort, includes identification of the most difficult parts to reconcile, detailed process comparisons, and thorough analysis of key software simulation and verification tools.

The agreement does not initially include all the ASIC offerings of both. In fact, the most advanced items are held back: Intel's processor and controller line, and TI's TMS320 digital signal processors (see table). However, both explain that, near the end of the year, they believe things will be going smoothly enough to discuss the phase-in of processor cells from both sides. TI says it expects the joint library to be ready by the start of 1988 and first customer designs to be received during the first half of next year.

From the customer perspective, such major buyers as John R. Wallace, president of Ford Microelectronics Inc., are rooting for the marriage to last. "To the extent that it helps in the multiple-source area, it could be a powerful agreement," he says. Wallace was program manager for Intel standard cells in 1982 before joining Ford Microelectronics, which procures ASIC chips for its parent, Ford Motor Co., and accounted for about 6% of Intel's sales last year, second only to IBM Corp.'s 6.7%.

Wallace says that if better standards evolve, he would like to drop the internal cell library and computer-aided-design tools he is forced to support because of incompatible libraries, processes, and software. But he is not about to start celebrating yet. "Agreements have come and gone and I have not seen much results."

The alliance will trigger similar stra-

INTEL-TI DEAL INCLUDES...

From Intel	82xx peripherals	8237A, 8254, 8259A, 82284, 82288
	Compilers	RAM, ROM, PLA
	SSI/MSI cells	From 150 cells in the VLSiCELL library
From TI	Bit-slice components	2901, 2902, 2904, 2910
	Register files	16 by 8 bits through 64 by 9 bits
	FIFO buffers	32 by 8 bits through 128 by 9 bits
	SSI/MSI cells	From over 200 cells in the TSC500 library

...BUT EXCLUDES FOR NOW

From Intel	Processors and controllers	8088, 80186, 80286, 80386 processors; 8051 controller
From TI	Digital signal processors	TMS320

SOURCES: INTEL AND TEXAS INSTRUMENTS

MOTOROLA'S ASIC BOSS RESIGNS

Just as Texas Instruments and Intel took what could be a big step forward together in application-specific ICs, Motorola may have taken a big step back by losing the boss of its ASIC Division. Kenneth G. Wolf, the vice president and general manager, resigned earlier this month, Semiconductor Product Sector executives confirm. They would give no reason, but financial analysts who follow Motorola report that corporate officials were disappointed with the division's sales.

Wolf is a highly regarded executive who was instrumental in organizing the separate ASIC operation last year, after an abortive earlier attempt to mesh semicustom chips with standard parts. He reportedly will be involved with a startup company in the San Francisco Bay area that will be dedicated to fast bipolar memories. Thomas George, assistant general manager of Motorola's Semiconductor Product Sector, will be acting general manager for ASICs until a successor is named. *–L. W.*

tegic moves by other ASIC competitors within months, predicts Richard L. Horton, Honeywell Inc.'s business development director for ASIC products in Colorado Springs, Colo. Besides the creation of new teams of merchant suppliers, he expects "smaller and medium-size ASIC companies to become more focused or specialized" in order to survive.

The pressure is now on ASIC firms to get the deals done, notes financial analyst Michael Kubiak, based in San Francisco for New York's Kidder, Peabody and Co. "The others have to start pulling rabbits out of the hat," he says. Kubiak expects LSI Logic Corp and VLSI Technology Inc. to lead the way in order to fill out their semicustom lines and add manufacturing muscle.

–Larry Waller and J. Robert Lineback

MICROPROCESSORS

INTEL BUILDS CUSTOM CHIP FOR CANON WITH CPU CORE

TOKYO

Microprocessor-rich Intel Corp. is collecting dividends by offering its designs as cores in custom chips. Now its Japanese arm, Intel Japan KK, has gotten into the act by developing a full-custom microcontroller for Canon Inc. to replace electromechanical gear in a photocopier. But the microcontroller could find use in other office machines, as well as in sequential industrial-control applications.

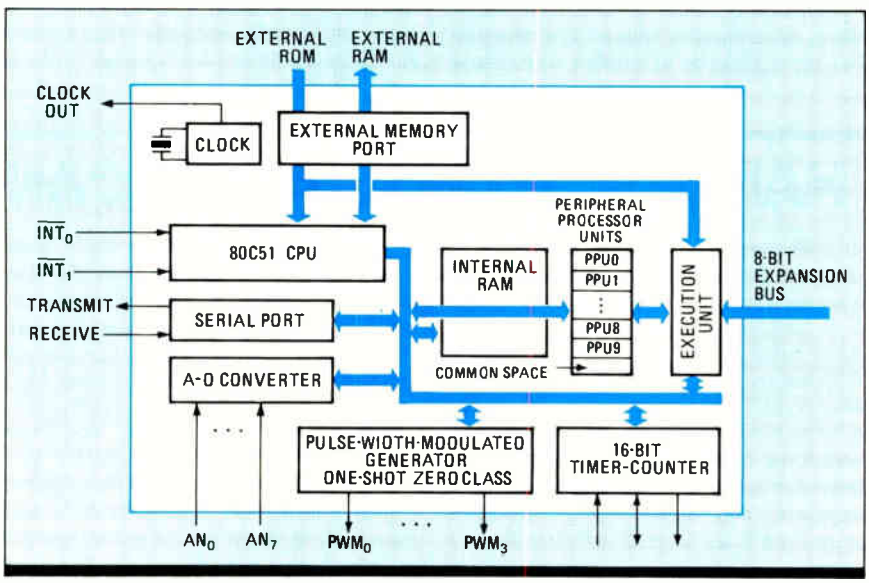
The cooperative effort highlights a business that Intel has been quietly pursuing for years: what it calls very customer-specific chips. The Canon part is among the first of these started by Intel Japan with a processor core [*Electronics*, July 9, 1987, p. 51]. It uses an 80C51 CPU core to supervise the operation of 10 slower coprocessors, called peripheral processor units (see diagram), in what can loosely be described as a form of multitasking implemented in hardware.

Canon's contribution to the design includes an 8-bit bus expander that can offload high-speed repetitive or sequential tasks from the controller. It has also developed an 80C531 in-circuit emulator personality module and software, including an assembler, a reverse assembler, and emulation software.

The 10 peripheral processors are implemented on a time-sharing basis by an execution unit that is a second CPU simpler than the 80C51 core. It steps through one instruction for each individual peripheral processor in rotation in successive 8-μs time slots. Dedicated on-chip register blocks for each processor contain eight registers for that processor, including a program counter, a flag register, and a timer counter, so that no time is lost during task switching. A given register block and the processor execution unit constitute a unique processor. The CPU communicates with the processors via the register block, which is dual-port random-access memory.

Intel itself has no plans to mass-market the new chip in Japan or the U. S. But a spokeswoman for the Santa Clara, Calif., company points out that it retains marketing rights to all its custom parts. Also, Canon may use its part in other systems.

–Charles L. Cohen



CORE OF THE MATTER. Using an 80C51 CPU core, Intel and Canon have designed a full-custom microcontroller that features a form of multitasking implemented in hardware.

TELECOMMUNICATIONS

A VERSATILE SWITCH FROM N. TELECOM

NASHVILLE, TENN.

Telephone companies are getting another opportunity to loosen their links to AT&T Co. with Northern Telecom Inc.'s DMS-Supernode. The new digital switching device will permit Bell operating companies to custom-design their networks and provide new customer services. They also will be able to cut themselves in for a piece of one of AT&T's more profitable services.

Supernode can help consolidate the current system of signal-transfer points, service-control points, and cross-connects into a single network node, says Steve Tsui, director of technology at Northern Telecom in Nashville, Tenn. "It gives the operating company control of the network instead of individual switches."

DMS-Supernode itself functions as an open network, fully compatible with its DMS-100 predecessors and the equipment of other manufacturers. It has three parts: DMS-Bus, a 128-Mbit/s hardware bus; DMS-Core, a 32-bit microprocessor and control center; and DMS-Link, a networking software package based on Signaling System No. 7 and the public standards and protocols of the Integrated Services Digital Network.

ADDED SERVICES. For the operating companies, the most attractive feature of Supernode is the capability it provides to upgrade services to customers throughout the network. Call waiting, for example, would be available between different central switches; currently, it must be done on a switch-by-switch basis. Equally important, with Supernode the regionals would be able to route their own 800 calls instead of paying for access to AT&T's lines and data base.

AT&T maintains that it's still in front with a comparable product, its No. 5 ESS architecture. Jerry Johnson, manager for product planning, says that the No. 5 ESS switch also allows customers to develop their own services. But that switch sells mainly to non-Bell operating companies, leaving room for the Northern Telecom equipment—in fact, the first Supernode is due to be installed in August by Bell South.

At Northern Telecom, the view is that the Supernode will tend to push AT&T toward providing more services itself rather than simply selling access to its network. "Should they make it in services, or make it on the network?" says Roger Schwantes, vice president of marketing and technology at Northern Telecom. "That's the dilemma they always face."

–Alan Burdick

OPTICAL MEMORIES

CONTROLLER MAKES WORM DISKS EASIER TO USE

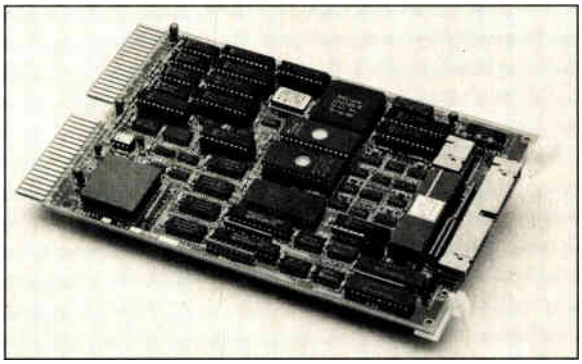
SAN JOSE, CALIF.

Computer-system builders who want to capitalize on the capacity of write-once, read-many optical disks by using them to emulate magnetic disks have a big job ahead of them. For one thing, they must write complex software drivers so the system can make changes in existing files, because WORMs, unlike magnetic media, are not erasable. And because that slows the computer—a WORM takes longer to alter files—builders must figure out a way to pick up speed another way.

Now Qualogy Corp. has come to the rescue with a $1,300 controller board that provides a time-saving way to link WORMs to computers: instead of emulating a magnetic disk drive, the San Jose, Calif., company's QLC1000 emulates a tape drive. Although tape is erasable, computers generally do not look for and overwrite data. Instead, the computer saves time by simply rewinding and rewriting the entire reel of tape. The software commands are correspondingly simple. So by being able to emulate them for WORMs, programmers spend much less time writing software. More important, machine speed increases.

The controller now emulates a magnetic tape on Digital Equipment Corp.'s Q-bus and operates with DEC's VMS or RSX operating system. This opens the door to integrating WORMs into DEC's VAX machines and computers compatible with them. In addition, Qualogy plans to issue versions of the board for other SCSI peripherals that it declines to name.

In operation, the computer, thinking it is working with a tape drive, behaves as it would to erase and overwrite a tape. Thus, a request for a "tape" rewind actually prompts the controller to reposition the beginning of the data. But since the optical disk cannot be erased and overwritten, the controller actually skips to the next open sector. If, for example, the system has written data in sectors 1 through 100 of the first track on disk, a change in that data will trigger a rewind-and-overwrite command from the computer. The controller will reposition the start of the "tape" from track 1, sector 1 to track 1, sector 101. The computer system then gets an almost immediate response indicating that the beginning of the tape has been reached and the write operations can begin.



DIRECTOR BOARD. Controller emulates a tape drive instead of a magnetic disk drive, easing the job of using a WORM.

In reading from the QLC1000 optical drive, the computer uses all the tape-positioning commands associated with a tape drive, such as fast forward and fast reverse. But because an optical disk is a random-access rather than a sequential-access device, these operations occur much faster. "A DEC TK50 tape drive takes 35 minutes to search to the last file on tape," says Steve Davis, director of marketing for Qualogy. "Our controller and an optical-disk drive can perform the operation in under eight seconds."

On the board, a V50 microprocessor from NEC Semiconductor directs the operations of the gate array. The V50 also handles the Small Computer Systems Interface with the optical disk drive. Thus, no hardware changes are required in the optical disk drive for it to operate with the controller. Firmware loaded into erasable programmable read-only memory directs the V50. By changing the firmware, the QLC1000 can control other peripherals, such as a tape drive.

An on-board 64-Kbyte memory cache significantly improves read/write performance by acting as a buffer between the 1.4-Mbyte/s transfer rate of the Q-bus and the optical disk drive's 300-Kbyte/s speed. The controller can transfer data from the cache to the optical drive at a fast 800 Kbytes/s.

Because writing many small records can waste space on the disk, the buffer gathers a full sector worth of data before writing. "All write operations are cached in the buffer," says Davis. "This improves performance, because the controller issues a write-complete status as soon as the data has been written into cache, even though the cache is still being emptied to the disk. With the write-complete issued, the host can then immediately start another write operation without having to wait for the disk to finish unloading the cache." The controller will then issue write-complete status until the cache is filled. *—Jonah McLeod*

TRADE

KOREANS 'TRY HARDER' TO BUY AMERICAN

NEW YORK

Worried that its growing trade surplus with the U. S. will cause the same kind of friction that has disturbed U. S.-Japanese trade relations, South Korea is moving aggressively to redress the imbalance. The Seoul government is opening new markets to U. S. goods, reducing import tariffs, encouraging its business sector to "buy American," and promising to keep the 1987 trade gap at or below the 1986 level of $7.4 billion.

Key to the new program is South Korea's electronics industry, which is now its biggest exporter with about $6.3 billion in 1986 overseas sales. Because much of the manufacturing equipment and materials needed are already imported from the U. S. and Japan, the Electronic Industries Association of Korea is encouraging members to buy from U. S. makers wherever possible. The organization sponsored a buying trip early in July in which representatives of more than 20 Korean electronics firms toured U. S. plants, met with suppliers, and signed purchase agreements worth an estimated $300 million or more.

But although the companies say the trip has been a success, they wonder if U. S. suppliers are pursuing the Korean market with enough vigor and if they are as committed to the market as Korea's Japanese neighbors. Given the current trade situation, at least one Korean company, GoldStar Semiconductor Ltd., is spending more for U. S.-made goods than comparable supplies he could get in Japan. GoldStar Semiconductor is a joint venture between Korea's GoldStar Co. and AT&T Co., and part of a conglomerate that will spend more than $50 million on semiconductor manufacturing equipment and materials worldwide this year.

"We can sustain this [buy American] mode for maybe the next few years," says Hee-Gook Lee, director of strategy planning for GoldStar, but not forever. Unless the Americans learn to compete with the Japanese, he says, balanced trade between the U.S. and Korea will never amount to much more than a dream.

According to EIAK figures, Korea spent almost $1.1 billion on U.S.-made industrial electronics equipment, consumer electronics, components, and parts in 1986. But purchases from Japan were more than twice that, approaching $2.7 billion. Because Korea is suffering its own trade deficit with the Japanese—about $5.4 billion last year—it is encouraging businesses to buy items in the U.S. instead, thereby fixing two problems with a single solution.

By and large, most businesses are willing to help out in this regard, Korean businessmen say. "Given the present economic situation, we will buy American-made equipment," says Lee. "In several instances recently, I made the decision to buy American equipment even though [competitive] Japanese equipment might have been more attractive. But if I see a definite advantage in Japanese equipment, then I'd be crazy to buy American."

A July buying trip by the Koreans nets U.S. firms $300 million in orders

He says the Japanese are "more experienced at selling in foreign markets," and that they are more willing to negotiate a lower price and to provide extra service than the U.S. competitors. "Servicewise, the Japanese have been better, especially when problems arise," says Lee, who signed deals for $17 million in materials and equipment during his week-long whirlwind trip to Los Angeles, Chicago, New York, and Washington. "They seem to go one step further."

A major goal of the EIAK's buying trip, for which it published a 76-page shopping list, is to encourage U.S. companies to compete in the Korean market. The number of U.S. firms with operations in Korea is still small, and only a few have factories there. Among them is Corning Glass Works, which has a joint venture with Samsung to make color-TV picture tubes for Korea's domestic TV market. The venture has managed to compete favorably with companies that make their tubes in Japan.

But Keun Sun Choi, president of the consumer products sector at GoldStar Co. in Seoul, says the U.S. has been slow to recognize the market potential Korea has to offer. His hope is that these buying trips—other industries are sponsoring similar trips later this year, and the EIAK plans an even larger spending spree in 1988—will spur interest. Other programs will also try to lure U.S. electronics producers to Korea. Choi says sales assistance and consultation offices will be set up at Korean Trade Association locations in major U.S. cities to help match U.S. producers with Korean customers. A U.S. Products Show will be sponsored by the EIAK this fall, and the government is doing its part by eliminating local-content requirements for its purchases.

–Tobias Naegele

SEMICONDUCTOR PROCESSING

THIS FURNACE ADDS METAL WHILE IT PULLS THE INGOT

WALTHAM, MASS.

Researchers at GTE Laboratories are not ready to suggest that diffusion furnaces are about to become a thing of the past, but such thoughts would be understandable after what they've seen in a dramatically different process that could yield economical power transistors and photodiodes.

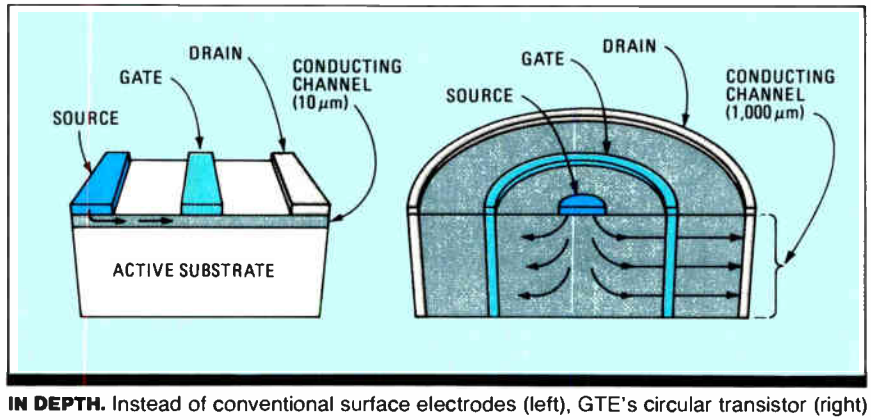
The engineers in Waltham, Mass., combined single-crystal silicon and high-purity tantalum in a small Czochralski furnace. They produced ingots in which the metal elements for circular transistors, made of the eutectic metal tantalum disilicide, are grown volumetrically while the ingot is being pulled from the melt. Early measurements on some of the wafers indicate blocking voltages as high as 300 V, suggesting power-transistor applications. Results with other devices show their potential as light-sensing photodiodes in the 350- to 1,100-nm (high-ultraviolet to near-infrared) portions of the spectrum [*Electronics*, July 9, 1987, p. 112].

Instead of depositing the metal elements atop a thin (10-μm) conducting channel on the upper side of the wafer, GTE Labs grows the metal as tantalum disilicide rods that extend from top to bottom inside the wafer because of the way they grow within the silicon.

Brian Ditchek, the principal investigator for the project, explains that the process starts by putting single-crystal silicon and high-purity tantalum into the furnace's crucible. Because of the phase relationship between the metal and the silicon, "the two materials separate in a controlled manner, so that the metal rods grow in the direction the ingot is being pulled," Ditchek says.

GTE Labs has used a pull rate of 20 cm/hour, which Ditchek says is a little faster than for conventional silicon-crystal pulling. He's produced ingots that are 1 in. in diameter and 4 in. long in about 30 minutes. The tantalum disilicide rods extend from top to bottom throughout the ingot at a density of 2 million rods/cm², with an average of about 7 μm between them.

SLICED AND ETCHED. After wafers measuring 10 to 20 mils thick are sliced from the ingot, contact holes are etched in the oxide layer for the source, gate, and drain regions of the transistors, and a cobalt metal layer is evaporated onto the surface in an electron-beam process. Ditchek says the transistors behave like Schottky-type junction field-effect transistors. All the metal rods under the annular gate contact, which is 20 mils in diameter, are energized when a bias voltage is applied. This changes the relative potential of the metal and the silicon, causing current to flow between the source and drain. Because the metal rods extend the electrodes defined by the top metal completely through the wafer, the conducting channel can be 100 times thicker than that of conventional devices, which have thin conducting channels and sur-



IN DEPTH. Instead of conventional surface electrodes (left), GTE's circular transistor (right) has gate and drain structures grown as the ingot is pulled from the melt.

face contacts. The thicker channel improves power-handling capacity.

The electrical properties of the transistors on these wafers include pinch-off voltages of 8 to 15 V and maximum blocking voltages of 300 V—"which make them promising for high-current, high-voltage applications," Ditchek says. One of the pleasant surprises the team has encountered in the project is that the tantalum doesn't contaminate the silicon sufficiently to interfere with electrical properties. "There is some tantalum solubility in the silicon," Ditchek says, leading to dislocation or defect densities that might ordinarily degrade the silicon's performance in detecting light. But the 50%-to-70% quantum efficiencies GTE has measured for photodiodes are similar to those for conventionally produced devices, he notes.

Ditchek emphasizes that he's a materials researcher, not a device expert, and therefore he hasn't extrapolated potential cost savings for the process.

This radical new process could yield cheaper power transistors

But he and John Gustafson, manager of the labs' Electronic Materials Department, are convinced that the capital equipment and materials costs would be substantially less than they are for conventional semiconductor processing.

Among the reasons are the fact that there is no diffusion or implantation of the wafers after they're sliced from the ingot. And subsequent photolithography steps are reduced to a minimum, because only a top metal layer must be applied to the wafers. "Everything is there except for the metal contacts," Gustafson says.

"We're very happy with our results," Ditchek says. "I'm probably as surprised as anyone else that the devices work so well. We haven't seen anything discouraging yet." For his part, Gustafson says that the next step is to turn Ditchek's results over to device specialists, and let Ditchek get back to materials research. "There's a lot of gold to be mined from Brian's materials work," Gustafson says, "especially in III-V compounds and in other silicon and germanium systems." *–Larry Curran*

MEMORIES

PHILIPS' 1-Mbit SRAM CHALLENGES JAPAN

EINDHOVEN, THE NETHERLANDS

With Japanese producers leading the way in designing denser fast static random-access memories (see p. 60), a European challenger is coming up fast on the outside with a 1-Mbit SRAM, the first from a major commercial supplier not based in Japan. The challenger is Philips of the Netherlands, and judging from what was announced earlier this year [*Electronics*, March 5, 1987, p. 58], the Dutch company's device outdoes the Far East competition on several counts.

But the chip's significance goes beyond that. Philips' biggest single development effort in ICs—its researchers are also working on a 4-Mbit version—underscores the firm's determination to become a technology leader and remain a top IC player. "It's also a milestone in the submicron cooperative project" carried out with West Germany's Siemens AG, says George van Houten, a member of Philips' board of management who is responsible for corporate research.

SAMPLES. The company's Eindhoven Research Laboratories has made working samples of the SRAM, and claims it is the world's first 1-Mb model produced in full CMOS submicron technology with six-transistor cells. Its minimum features are 0.7 μm, and it packs 128,000 memory positions, each for 8 bits, onto a 7.7-by-12.2-mm chip. That, van Houten says, "means Philips is number one in packing density as well." The cell size is 5 by 12 μm.

The memory is also the fastest announced 1-Mbit chip. It accesses in 25 ns, which compares with 35 ns for one described by Sony Corp. Active current and power at 20 MHz typically check in at 30 mA and 150 mW, respectively, which "we think is the lowest achieved for a 1-Mbit SRAM," says Hans Ontrop, manager of the design team. In standby, current and power consumption are typically 0.1 μA and 0.5 μW, values up to 10 times less than the competition's.

The first engineering samples will be shipped late in 1988 or early in 1989, says Roel P. Kramer, director of IC technology development. Volume production is expected to begin around mid-1989. Working samples were fabricated on 4-in. wafers, but production types will be made on 6-in. wafers.

The SRAM is a result of the Philips-Siemens Mega project, begun in 1984 as an effort to match U. S. and Japanese IC technology. The $1 billion project calls for Siemens to produce 4-Mbit dynamic RAMs by 1989 and for Philips to produce the 1-Mbit SRAMs the same year.

VAN HOUTEN: "Philips is number one in packing density" with its 1-Mbit static RAM.

In their SRAM, the Dutch researchers focused their efforts on minimizing power, rather than increasing speed—thus bucking the current trend. This makes them well-suited where low power consumption counts: in battery-operated consumer goods, portable office equipment, and hand-held applications such as cellular radio—all Philips domains. The low standby power comes in handy in battery backup systems for data processing and communications, and the high capacity is an advantage in video cassette recorders or digital TV sets for economically storing picture frames to obtain flicker-free images.

WORKING TOGETHER. The key to low power, explains Ontrop, is the way the CMOS and the six-transistor cell design work together. Linked in a double cross-connection scheme, the gates of the two p-channel transistors hook up with the drains of two of the four n-channel transistors. In operation, one p-channel transistor is always off, and that means little power. What also helps is a divided-word-line architecture in which only part of the memory cell is accessed.

In fabrication, Philips uses a single-polysilicon double-metal twin-well process on an epitaxial substrate that requires only 13 masks. The device has 32 pins and will be available in both a standard dual in-line package and a small-outline package.

Design work at Philips is going in several directions, says technology development director Kramer. One is toward 4-Mbit SRAMs with 0.5-μm features; another is to more economical processes and fewer masks. Also on the list are nonvolatile memories combined with bipolar circuits as a base for functional add-ons. *–John Gosch*

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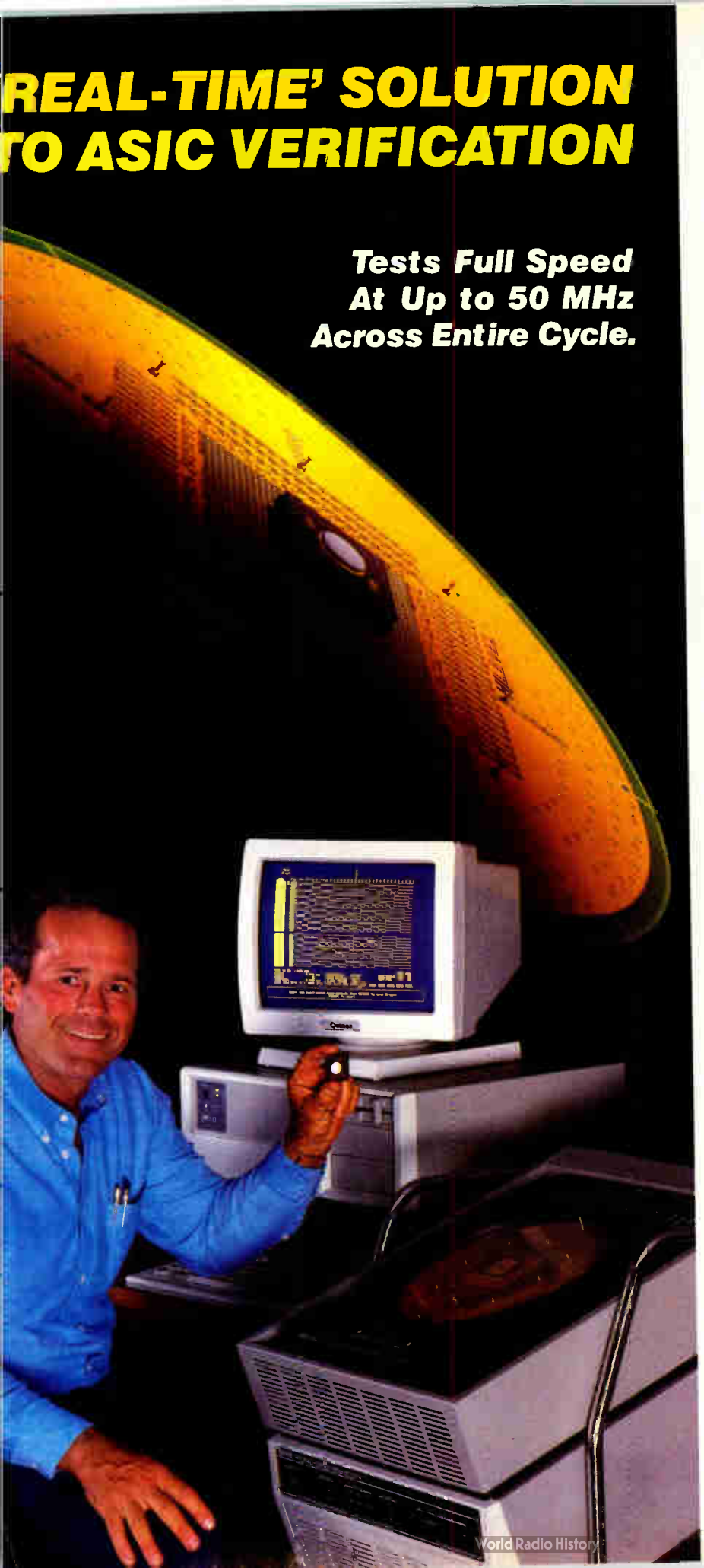

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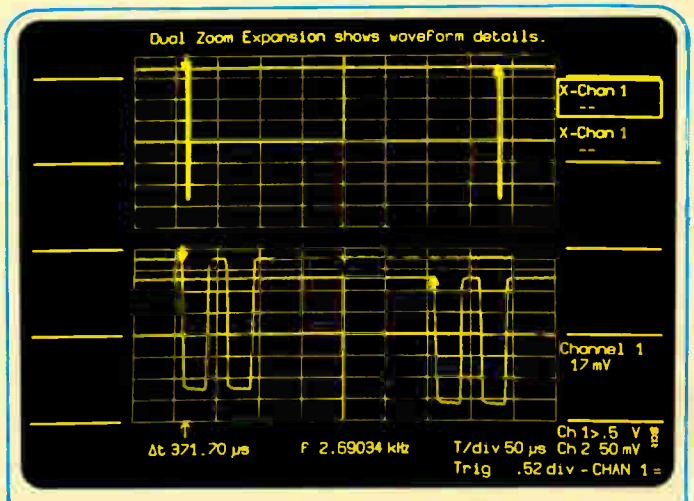

Powerful dual zoom expansion shows that the glitches in the top trace actually contain two rectangular pulses.

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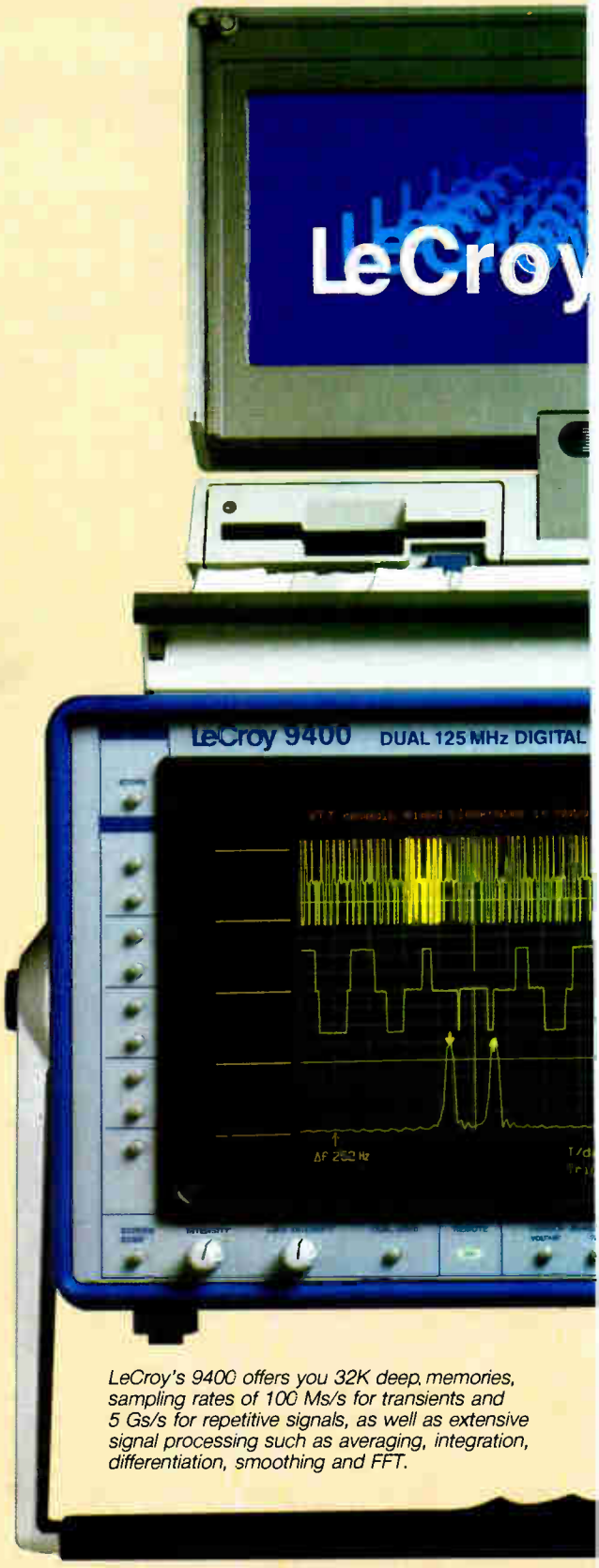

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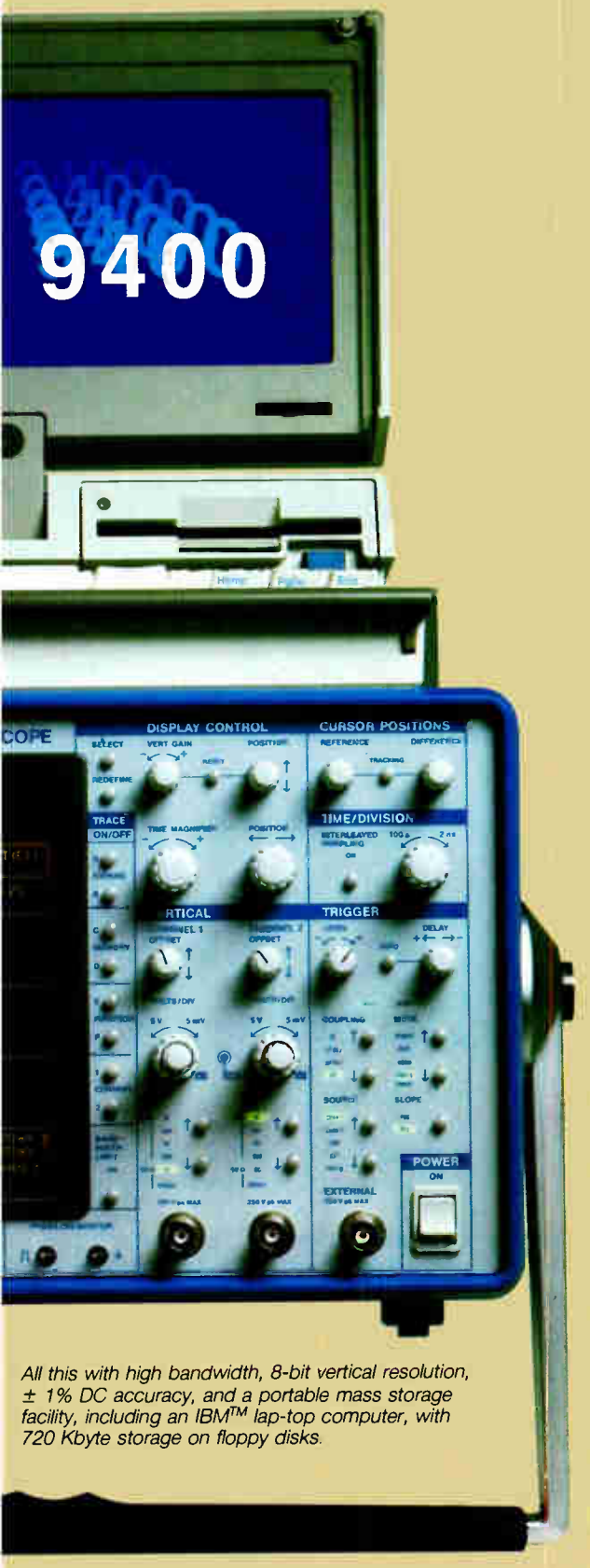

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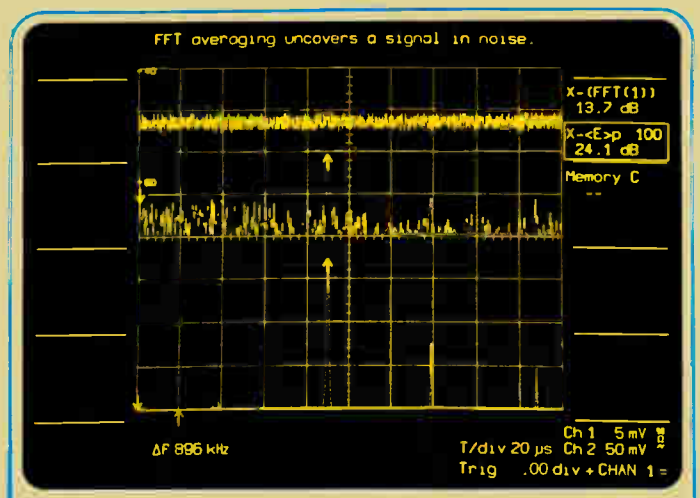

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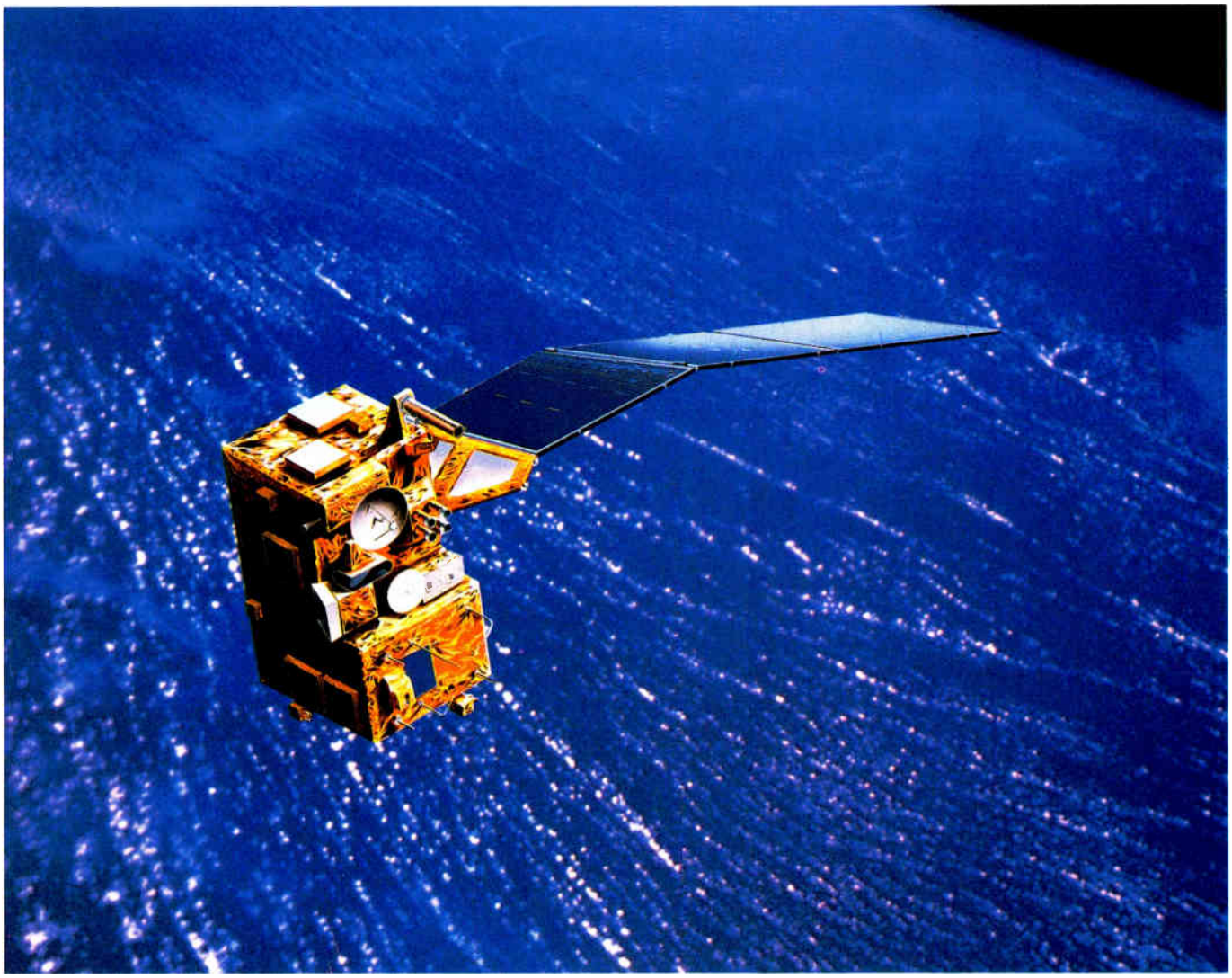


JAPAN LAUNCHES INTO A NEW ERA IN REMOTE SENSING.

Japan's first Marine Observation Satellite-1 (MOS-1) is now circling around the globe, covering its entire surface in 17 days from 909km up in space.

With three sensors aboard, the new remote sensing satellite beams back an enormous volume of data on diverse aspects of the sea, land and atmosphere. One of the sensors, MESSR (Multispectral Electronic Self-Scanning Radiometer) senses colors of the sea and land, and recognizes surface features 50m by 50m, utilizing CCD (Charge-Coupled Device) image sensing devices. The MOS-1 is expected to contribute greatly to fishery, agriculture, forestry, resources finding and environment preservation worldwide.

As the prime contractor to the National Space Development Agency of Japan (NASDA), NEC was engaged in system design, system integration and manufacture of key subsystems including major bus subsystems, the MESSR sensor, the DCS (Data Collection System) repeater, ground receiving system and image data processing system.

With more than 30 years of experience in space development, NEC has been involved, as a prime contractor or system integrator, in 23 of the 37 satellites placed in space by Japan.

NUMBER 138

DIGITALIZATION EXPANDS IN LATIN AMERICA.

In keeping with the ultimate goal of a global ISDN, telecom authorities in Latin America are stepping up their digital network programs.

Telecomunicações Brasileiras S.A. recently awarded NEC do Brasil S.A. a giant order for state-of-the-art digital equipment. It includes NEAX61 digital switching systems (360,000 lines), 5GHz 140M-bit digital microwave communication equipment (1,800 sets), fiber optic communication equipment (200 sets) and PCM transmission equipment (1,300 sets). Most of the systems are to be produced locally with delivery starting this year.

Meanwhile, Empresa Nacional de Telecomunicaciones, Argentina has awarded PECOM-NEC S.A. a contract for NEAX61 digital switches (300,000 lines) and PCM transmission equipment to be installed in the metropolitan and northern areas of Argentina. Local production is scheduled to begin soon. In 1982 NEC constructed a 320-km fiber optic digital telephone system, interconnecting 6 tandem exchanges and 60 telephone offices in the metropolitan area.

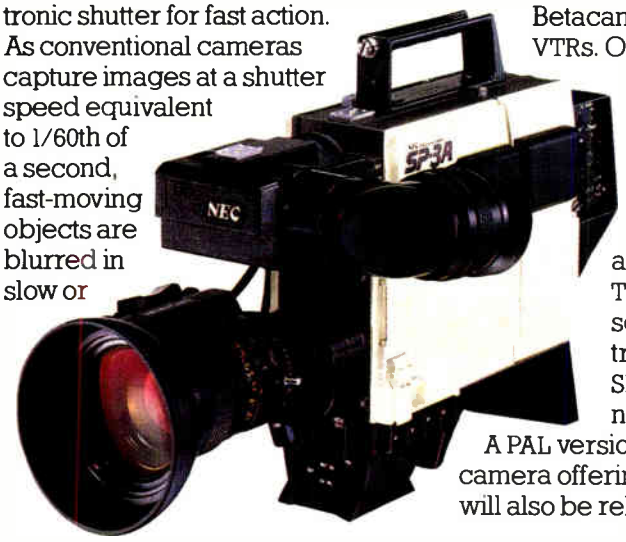
NEC is also contributing to the 5-year telecom digitalization project by Compañía Anónima Nacional Teléfonos de Venezuela by supplying NEAX61 digital switches to 97 exchanges in Maracaibo, Puerto La Cruz, and other important areas. For interconnection of these exchanges NEC will supply a 200-km fiber optic communication system.

As one of the world's leading suppliers of digital exchanges, microwave and fiber optic systems, NEC is helping to further the digital revolution throughout the world.

NEW CCD CAMERA STOPS ACTION ELECTRONICALLY.

The trend in color cameras for broadcast use is irrevocably "solid-state". CCD cameras are more compact, dependable and durable than tube types and have no comet tails and burn-in when shooting extremely bright objects.

On top of these inherent benefits, NEC's new SP-3A CCD Color Camera has an exclusive feature—the electronic shutter for fast action. As conventional cameras capture images at a shutter speed equivalent to 1/60th of a second, fast-moving objects are blurred in slow or still playback on VTR. To remedy this problem, our SP-3A stops the action electronically at 1/60th to 1/2000th of a second, offering precise, clear-cut images.



The SP-3A uses 3 new CCD chips that are anti-smear and -blooming—two for the green channel and one for the combined red/blue channel. This dual green system provides much higher resolution and sensitivity than the conventionally-structured RGB system.

The new CCD camera displays widespread versatility. Besides standalone use it forms an efficient shoot/record system with integral Betacam, MII or 8mm-format VTRs. Options are available for multi-core or triax remote control.

Users' acceptance of this versatile new camera has been remarkable. NBC, a major U.S. TV network, recently sealed a five-year contract to purchase the SP-3A for electronic news gathering.

A PAL version of NEC's CCD color camera offering broadcast quality will also be released.

WORLD'S FASTEST ECL GATE ARRAYS.

The performance of high-speed silicon logic LSIs is rapidly accelerating. NEC's new ECL-4 gate arrays are the swiftest in the world with a 100ps basic gate delay or 220ps fully loaded.

Combining unprecedented speed and flexibility, the ECL-4 family includes the μPB6312 with 1,200 gates (400 Full-adders) and the μPB6303 with 600 gates (200 Full-adders). Both offer 100K or 10KH interface options and ample I/O up to 108 pins.

NEC's ECL-4 gate arrays are available in a choice of 72- or 132-pin PGA packages, and operate in ordinary forced-air-cooling environments since sophisticated heat sinks are standard.

NEC offers 61 internal macros and 33 I/O blocks plus complete CAD tools. The ECL-4 family should hasten the development of speed-oriented computers, graphic terminals, LSI testers and telecom equipment.

NEC

INTERNATIONAL NEWSLETTER

SANYO SAYS ITS VIDEO-DISK PLAYER GIVES A BETTER 3-D PICTURE

A prototype of a new three-dimensional video-disk player offers a brighter picture and less flicker than 3-d video disk systems already on the market. The result of a joint development project between Sanyo Electric Corp. of Osaka and the Science and Technical Research Laboratories of NHK, of Tokyo, Japan's largest broadcaster, the system uses four-way interlace to display 120 fields/s—30 frames of 60 fields/s each for the right and left eyes. Systems using the VHD standard are now being marketed in Japan for about $700 by Victor Co. of Japan, Sharp, and Matsushita [*Electronics*, June 9, 1986, p. 11], but they display half as many fields. Sanyo has not yet decided when to begin marketing the new system, which requires liquid-crystal shutter goggles, a special video-disk player, and a special monitor that can display fields at twice the normal rate. The company will probably develop 3-d systems for professional applications before going after the consumer market. □

NTT AND SONY BATTLE MITSUBISHI OVER STILL-VIDEO PHONE STANDARD

A fight could be brewing over competing standards for still-video telephones, much like the struggle earlier between the VHS and Beta formats for video cassette recorders. As with VCRs, Sony Corp. is again a major player, this time lining up with Nippon Telegraph and Telephone Corp. The two have developed a low-cost still-video phone system that is incompatible with an older, more expensive system made by Mitsubishi Electric Corp. The $335 Sony-NTT unit costs about one-quarter of the Mitsubishi system. Both transmit and receive still images over existing telephone lines, but Mitsubishi's system incorporates a telephone, whereas the Sony-NTT system connects to a telephone with a modular plug. Not to be outdone, Mitsubishi is developing its own low-cost model at Mitsubishi Sales America, of Cypress, Calif. The new unit will cost less than $400 when it hits the U. S. and Japanese markets later this year. □

JAPAN WILL RUN A NATIONWIDE TEST OF HIGH-DEFINITION TV NEXT YEAR

Japan's Ministry of Posts and Telecommunications will conduct a nationwide broadcast test of high-definition TV during next year's Olympic Games in Seoul, South Korea. The test will be conducted on one channel of Japan's BS-2b broadcast satellite, which operates in the 12-GHz band. About 200 TVs will be included in the trial, using an HDTV system developed by Japan Broadcasting Corp. that features 1,125 horizontal scanning lines—more than twice the number used in the NTSC system in Japan and the U. S. The Japanese government is pushing the new standard hard and hopes to have 30% of Japan's viewers watching HDTV by the year 2001. Its reasoning is simple: the government figures HDTV will represent an $80 billion market by then. □

ES2 TAKES A CRACK AT JAPAN'S ASIC MARKET WITH HELP FROM MITSUI

European Silicon Structures Ltd., known as ES2, is trying to crack the toughest chip market of all—Japan. But the Luxembourg company has a strong ally in Mitsui & Co., a Tokyo trading firm that is already marketing ES2's Solo series of automatic design software for custom large-scale integrated circuits. Mitsui is now negotiating with an unnamed software company to set up jointly a design center in Japan to produce designs, based on Solo software, for manufacture at ES2's factory in Luxembourg. The Solo series is intended for developing full-custom large-scale integrated circuits with 5,000 to 10,000 gates. Mitsui projects the Solo series to bring better than $3.3 million in sales in its first year on the Japanese market. □

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INTERNATIONAL WEEK

IBM JOINS MITI's SOFTWARE PROJECT

IBM Japan Ltd. is joining the Sigma Project to promote computer software development in Japan. The project, begun in April 1985 by the Ministry of International Trade and Industry, aims to increase the productivity of software development in Japan with the investment of $166 million, or 25 billion yen, over five years. The government contributes about half, and member companies the balance. IBM Japan, the country's third largest supplier of computers, is the 166th member. It joins arch rivals AT&T, Unix Pacific, and Nihon Digital Equipment, among other foreign firms or joint ventures.

JAPANESE VENTURE TO IMPORT U.S. ICs

Teksel Co. of Tokyo, Japan's 28th largest semiconductor distributor, and Arrow Electronics of New York, the second largest semiconductor distributor in the U.S., will form a joint venture in Tokyo later this month. The new company, to be called Arrow-Tek, will import chips from major U.S. manufacturers, including Texas Instruments Inc. and Motorola Inc. Arrow-Tek expects to deliver products a week after receipt of order, which is possible because of a satellite telecommunications network and air-courier shipment.

MITSUBISHI TO MAKE 1-Mbit DRAMs IN U.S.

Mitsubishi Electric Corp. will be the third Japanese chip manufacturer to assemble 1-Mbit dynamic random-access memories in the U.S., following Toshiba and Hitachi. The Tokyo company will convert its assembly line at Mitsubishi Semiconductor America in Durham, N.C., from 64-Kbit to 1-Mbit DRAMs. Assembly, to begin early next year, will initially yield 300,000 units a month. Because assembly of its 64-Kbit DRAMs at the U.S. subsidiary will stop by the end of this year, the Tokyo parent will export complete 64-Kbit units to the U.S. market with a 13% tariff. In addition, Mitsubishi is building a $33 million wafer-fabrication facility for ASICs this month in Durham. Its ASICs, including 8- and 16-bit microprocessing units, gate arrays, standard cells, and full-custom integrated circuits, will be marketed in the U.S. starting in April of 1989.

SAMSUNG, FILIPINO FIRM TEAM UP ON TVs

South Korea's Samsung Co. has entered into a joint venture with Mabuhay Electronics Corp. of Manila to produce color TV sets for domestic and export markets. Described as the first Korean-Filipino joint venture in electronics manufacturing, it has built a new plant in Sucat, a suburb of Manila, with a capacity of 10,000 sets per month. Samsung also has plants in Portugal and the U.S.

PHILIPS AND SIEMENS JOIN ON STANDARDS

Philips of the Netherlands and West Germany's Siemens AG have agreed to cooperate in finding common standards and interfaces for digital image-processing systems used in medical diagnostics. The project aims to make it possible for diagnostic equipment from both companies to work together in an integrated system. So far, the lack of a common interface has prevented Philips and Siemens gear from working together in integrated systems.

3 FIRMS FORM U.S. OPTICAL-IC VENTURE

Nippon Telegraph and Telephone Corp. of Tokyo is jointly establishing a U.S.-based company with Mitsubishi Corp. of Tokyo and Battelle Memorial Institute, the world's largest independent nonprofit research organization, in Columbus, Ohio. The new firm, to be called Photonic Integration Research Inc., will develop and commercialize basic optical integrated-circuit technology invented by NTT. Since 1970, Mitsubishi Corp. has acted as a go-between for Japanese manufacturers and Battelle on the research and development of these companies' products. Photonic is 49% owned by NTT, 41% by Mitsubishi, and 10% by the institute.

SIEMENS DEVELOPS FAST 3-d SENSOR

Researchers at Siemens AG have developed a sensor system for applications in robotics and production control that recognizes objects in three dimensions in fractions of a second. The 3-d sensor uses a computer-controlled laser beam that scans the object and, from a known baseline, calculates the coordinates of different points on the object's surface. The system can determine 200,000 x, y, and z coordinates/s, and it takes only 0.2 s to completely recognize an object about 10 by 10 by 10 cm. A big advantage of the Siemens system is that it is not sensitive to variations in contrast, to ambient light conditions, or to the optical characteristics of the object's surface.

CONNECTOR MARKET TO BOOM IN EUROPE

The European connector market is set to reach $2 billion by 1990 at an annual average growth of 4.5%, according to market watchers Benn Electronic Publications of Luton, UK. Although surface-mount connectors are gaining in importance, they will only hold 5% of the market by 1990. Benn blames this on lack of standardization. West Germany will still be the top individual market with a predicted increase from $450 million last year to $560 million by 1990. The UK will stay second, and France will come in third.

SIEMENS TURNS OVER ITS FIRST U.S. SWITCH

Siemens AG of Munich, through its U.S. subsidiary Siemens Communications Systems in Boca Raton, Fla., has turned over its first digital switch to a U.S. telephone operating company—Wisconsin Bell. The system will handle 4,200 subscribers. Six other Bell operating companies have chosen Siemens as a potential third supplier of digital switches, after AT&T and Canada's Northern Telecom.

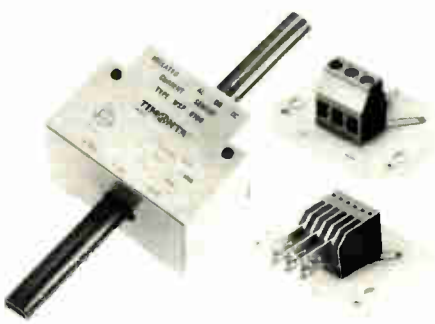
NIXDORF REGISTER IS BEST-SELLER

Nixdorf Computer AG says its 8812 has become Europe's hottest selling computer-based cash register. The Paderborn, West Germany, company has delivered 50,000 of its model 8812—after a slow start in 1977 when the 8812 hit the market. Production that year came to a mere 23 units. By 1983, the 10,000th unit had been delivered, and by the end of this year the company hopes to have sold its 75,000th unit.

SCHOTT, ZEISS SET OPTICS DEVICE FIRM

Two West German heavyweights in optical equipment, Schott Glaswerke and Carl Zeiss, have established a joint venture to develop the technologies needed for integrated optic components. The new company, called IOT GmbH, for Integrated Optics Technology, and founded in Heidelberg on July 1, will develop sensors, couplers, and other devices integrated on a glass substrate and used in optical communications and data-processing systems.

TIMONTA technology a bound forward



CURRENT SENSOR FOR DC, AC, PULSE CURRENTS

- Measuring range: ± 100 A linear
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- Output current at 100 A nom.: 100 mA
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Switzerland

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Tel. (091) 46 10 21, Tlx. 842 248, Fax (091) 46 26 59

INTERNATIONAL PRODUCTS

1-KW AMP SHRUGS OFF OVERLOAD AND DELIVERS TOP PERFORMANCE

POWER MOS FETS, COOLING SYSTEM KEEP THE JERICHO 1000 ON LINE

A 1-kW amplifier from Tunewell Transformers Ltd. combines low-current-density MOS FETs in its output stage with an innovative cooling system for protection against current overload in harsh environments—while offering high-end electronic characteristics for applications such as sonar systems.

Using 16 Hitachi Ltd. CMOS power MOS FETs in the Jericho 1000's output stage accomplished two things, the British company says. It reduced thermal stress, and it provided more time for electromechanical overload-protection devices to react.

SPACE SAVER. Measuring 500 by 170 by 109 mm, the Jericho 1000 is about half the size of 1-kW amplifiers offering comparable performance.

"We use a very large amount of silicon in the output stage to handle current," said Phil Rimmer, chief of the Jericho 1000 design team. "Because there is so much silicon, it takes a long time for it to reach a critical temperature." The power MOS FETs in each of the amplifier's 16 output channels incorporate 20 mm^2 of silicon, compared with 16 mm^2 in the MOS FETs used in competing high-end 1-kW amplifiers. The MOS FETs are rated at 100 W each. For 100-W, 7-A devices, says Rimmer, the amount of silicon in the Hitachi MOS FET is 50% more than average.

TIME TO SPARE. Although the critical temperature of the output stage is 200°C, Tunewell has specified the product at 150°C. In a typical overload, the amplifier reaches 150°C in about half a second. Since the amp's circuit breakers react in about 100 ms to shut it down, the Jericho 1000 has a comfortable margin for protection. Competing systems using bipolar implementations, by contrast, would leave only a few microseconds for protection devices to kick in.

The amp is further protected by innovations in the design of its cooling system. These include a high-volume fan and an unconventional heat sink.

The fan is rated at 30 V dc and can move 25 liters of air per second. It was chosen over an ac fan of similar size because the dc fan runs at higher voltage levels.

The heat sink weighs 1 kg and is configured as heat-dispersal pins in a staggered array instead of the conventional fin arrangement. The chief problem with the fin configuration is that air in contact with the fin is relatively motionless. That means heat initially has to conduct through the air—a very good insulator—before being blown away. Tunewell's staggered-pin array creates turbulence, an effective way to circulate air and dissipate heat, says Rimmer.

The Jericho 1000 targets a wide range of industrial applications where temperature is a problem. It also is intended for scientific applications, such as sonar systems in seagoing vessels. It is also tough, versatile, and small enough for use in high-power sound systems.

The amplifier measures 500 by 170 by 109 mm and weighs 14 kg. That is no more than half the size of comparable units from most rivals, the company claims. And it is only about a third the size of the 1-kW amplifier from Electronic Navigational Instruments Inc., the U. S. company that Tunewell regards as the market leader. "We believe the Jericho 1000 is the smallest amplifier in the world for what it offers," Rimmer says. "ENI can offer amps as robust, but they are much bulkier."

Tunewell got the size down primarily by integrating customized components and optimizing the cooling system so components could be packed closer together. "Since we specialize in transformers, we have been able to optimize that component for this specific task," says Rimmer.

The Jericho 1000's performance characteristics rank it in the top range of 1 kW amplifiers, according to the London company. A slew rate of 30 V/μs gives the Jericho 1000 phase-accuracy performance at high freqencies that is good enough for sonar applications. The slew rate also minimizes audible distortion in sound systems.

Low distortion—better than 0.01%—was achieved by using a high negative-feedback circuit. Most other 1-kW amplifier manufacturers have not used high negative-feedback techniques because of timing problems, says Rimmer, but Tunewell design engineers put extra effort into minimizing the propagation delays that cause timing problems. "The feedback signal arrives quickly and accurately to give low distortion figures," says Rimmer. Voltage gain is 23 dB. Maximum output voltage is 45 V.

The Jericho 1000's signal-to-noise ratio of 110 dB means it supports the high dynamic range required for spectral recording with the Dolby system, for example, says Rimmer.

MANY MOUNTINGS. Its compact design fits a standard 19-in. rack but also provides "a lot of mounting variations," Rimmer says. "It is not tied to the 19-in. rack. It can, for example, be wall-mounted next to circuit breakers." In scientific applications, it can be used as a benchtop device. The thermal protection built into the output stages means units can be stacked on each other. In high-performance sound systems, it can be attached to the back of a loudspeaker.

The Jericho 1000's single-unit price is £650. Samples are available now. Pro-

duction quantities will be ready by August. Tunewell specifies 124 V, 50 Hz or 60 Hz, for power input, but customized dc versions are also available.

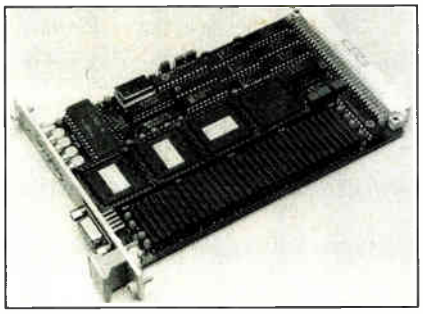
– *Steve Rogerson*

Tunewell Transformers Ltd., 115A Myddleton Road, Wood Green, London N22 4NG, UK. Phone 44-1-888-6044 [Circle 500]

BOARD DRAWS UP TO 2 MILLION PIXELS/S

The single-height Eurocard VGPM graphics board from PEP Modular Computer GmbH draws 2 million pixels/s, boasts pixel frequencies of up to 64 MHz, and offers other performance features formerly seen only on double-height boards.

Based on Hitachi Ltd.'s 63484 Advanced CRT Controller, the VGPM also incorporates three proprietary application-specific integrated circuits and 1 Mbyte of high-speed random-access



memory. The board's speed and memory capacity combine to eliminate flicker—even on 20-in. display screens. Bit-block transfer operation provides flexible generation of graphics as well as text characters.

Resolution is fully programmable. Users can address up to 2 million pixels in resolutions up to 1,280 by 1,024 pixels, and can choose 16 colors from a 4,097-color palette.

Writing extensive applications software is reduced by the board's direct access to three split screens and high-level graphics commands such as Paint, Rectangle, and Polygon.

Available now, the VGPM costs 2,950 DM. Delivery takes four weeks.

PEP Modular Computers GmbH, AM Klosterwald 4, D-8950 Kaufbeuren, West Germany. Phone 41-8341-8974 [Circle 701]

REGULATOR FEATURES RESET CAPABILITY

A single-chip voltage regulator from Sanyo Electric Co. features a reset-pulse capability that designers can use to automatically turn off a microcomputer when supply voltage exceeds a preset range.

Seven reset threshold voltages ranging from 3 to 4.8 V are available. In addition to normal packaging, the L78LR05 also comes in two surface-mount versions—one for conventional mounting, the other allowing the IC to be mounted on its side.

The L78LR05 operates at 5 V. Line regulation is within 1 mV and load regulation within 3 mV. Reset output-delay time is 1 ms. Available now in sample quantities, the L78LR05 costs 100 yen.

Sanyo Electric Co., Semiconductor Business Headquarters, Sakata 180, Gunma, Japan.

Phone 81-276-63-8055 [Circle 702]

OPTICAL MULTIPLEXER RUNS AT 20 MBITS/S

The K2000 fiber-optic multiplexer from Centec International Corp. Pty. Ltd. offers 48-channel, interference-free communication at a 20-Mbit/s data-exchange rate for distances up to 4 km.

A built-in autoset feature automatically adjusts the system's operating parameters for the length of the fiber-optic cable being used. The K2000 accommodates fibers engineered for wavelengths up to 200 μm with standard connectors. It costs about one-half as much as coaxial cable systems of comparable performance.

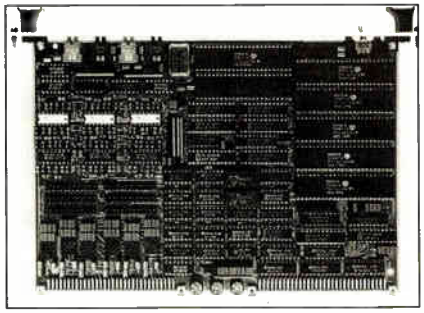
The 260-by-130-mm unit comes ready for mounting in 19-in. racks and is available from stock. The 48-channel version costs 4,500 Australian dollars; a 24-channel model, 3,300 Australian dollars.

Centec International Corp. Pty. Ltd., 5 Allen St., Waterloo, N.S.W. 2017 Australia. Phone 61-2-319-2355 [Circle 703]

I/O BOARD OFFERS 6 SERIAL CHANNELS

The SYS68K/SIO-2 module from Force Computers GmbH offers up to six serial input/output channels, each controlled by Motorola Corp. 68561 multiprotocol communications controllers. Communications interfaces can be either RS-232-C or RS-422-compatible.

Each channel can generate an interrupt to the VMEbus and drive three different interrupt vectors. All the communication signals generated by the Motorola controllers are available on the board's P2 connector. The board can be used as a low-cost multichannel serial I/O controller or as a multichannel synchronous protocol controller. Available from stock, the SYS68K/SIO-2 costs 2,390 DM.



Force Computers GmbH, Daimlerstr. 9, D-8012 Ottobrunn, West Germany.

Phone 49-89-600910 [Circle 704]

RUGGED TESTER USES MENU PROGRAMMING

Wandel & Goltermann's DT-10 data tester boasts compact design and rugged construction that target the needs of service engineers.

Designed for testing CCITT V.24 and RS-232-C interfaces, the DT-10 uses large, high-contrast liquid-crystal displays and clear menu-oriented programming via soft keys.

Other ease-of-use features are com-

prehensive self-test routines, an auto-configure mode that automatically recognizes various transmission parameters, and up to eight prestored instrument settings.

For versatility, the unit offers eight measurement modes, including bit-error rate, timing, and distortion, and a built-in breakout box. Transmission speed can be set anywhere within the range of 50 bits/s to 20 Kbits/s.

The DT-10 is available now, and the price depends on the importing country.

Wandel & Goltermann, P.O. Box 45, D-7412 Eningen, West Germany.

Phone 49-7121-1570 [Circle 706]

MULTIPLEXER CUTS 64-KBIT/S LINE COSTS

Dowty Information Systems Ltd.'s KMX1000 multiplexer saves users the cost of leasing separate lines for data and voice transmissions on 64-Kbit/s service.

The KMX1000 handles asynchronous or synchronous transmission from 1,200 bits/s to 19.2 Kbits/s. It can be used with devices such as Digital Equipment Corp. VT100 terminals, IBM Corp. Personal Computers and compatibles, minicomputers, and mainframes.

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7. High speed CMOS PLD.

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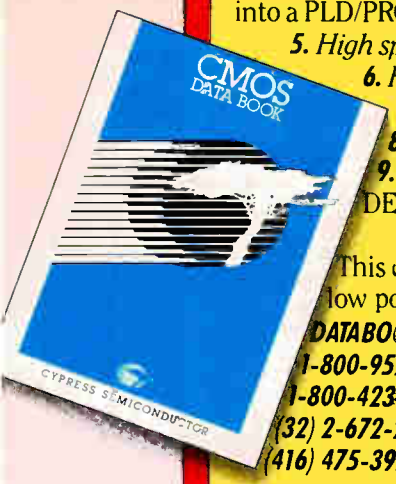


CYPRESS SEMICONDUCTOR

We illustrate the Lockheed SR-71 Reconnaissance aircraft, holder of the world's air speed record: 2,193 miles per hour. We're fond of speed records. Over 30 of our parts have broken or still hold speed records for integrated circuits.

Cypress Semiconductor, 3901 North First Street, San Jose, CA 95134.
Phone (408) 943-2666 Telex 821032 CYPRESS SNJ UD, TWX 910-997-0753

It comes in three versions: a basic four-channel multiplexer; a four-channel plus digitized voice-channel multiplexer; and an eight-channel multiplexer.

The digitized-voice option supports 32-Kbit/s transmission. Available now, the basic unit costs £775, the four-channel plus voice version, £1,250, and the eight-channel version, £995.

Dowty Information Systems Ltd., Steebek South, Newbury Business Park, London Rd., Newbury, Berkshire RB13 2PZ, UK.
Phone 44-1-351-2400 [Circle 705]

FIBER-OPTIC MODEM RUNS AT 20 KBITS/S

Seiko Instruments Inc.'s fiber-optic modem for RS-232-C ports converts digitally coded electrical signals into optical signals for 20-Kbit/s transmission.

The fiber-optic cable minimizes noise and can extend transmission as far as 1 km. The SFC-1100 Fiber-Optic Link Adapter handles full duplex, double-fiber bidirectional transmissions under the CCITT V.24 and V.28 standards.

The unit weighs 70 g and measures 67 by 57 by 22.5 mm. Available now, it costs 22,500 yen.

Seiko Instruments Inc., Electro-Optic Systems Department, 6-31-1 Kameido, Koto-ku, Tokyo 136, Japan.
Phone 81-3-684-2010 [Circle 707]

GRAPHICS BOARD CAN HIT 6 MIPS

The RPB40.8 graphics board from Rasterex AS offers 6-million-instruction/s operation, high-resolution color, and the ability to support all IBM Corp. Personal Computer graphics standards with a single PC-format board.

The board plugs into any IBM PC or compatible and features a 720-by-512-pixel resolution and a 256-color palette. It supports IBM's CGA, EGA, and PGA standards without adding hardware, and the board automatically detects the operating standard.

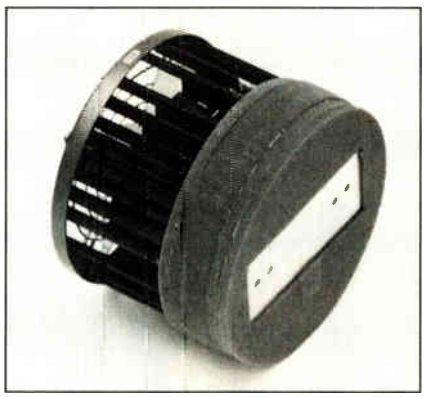
Built around a Texas Instruments Inc. TMS34010 digital signal processor and 512 Kbytes of dual-port video random-access memory, the RPB40.8 boasts drawing speeds of up to 12.5 million pixels/s. The board is available now. The price depends on the importing country.

Rasterex A.S., Gjerdrumsvei 12, N-0486, Oslo 4, Norway.
Phone 47-2-23-92-90 [Circle 709]

COMPACT COOLER HANDLES 25 W

Despite a compact design, the SC25-D1 thermoelectric cooler from Sweden's Supercool AB removes 25 W of heat at a 12-V dc, 3-A input.

Applications for the 123-by-120-mm



device include direct cooling of electronic components and cooling a surface of an insulated container. Cold-surface temperature is controlled by an integrated electronic thermostat.

Delivery time for the SC25-D1 is four to five weeks. The industrial version of the cooler sells for 1,225 Swedish crowns. Unit prices drop 40% for purchases in 100-unit lots and 55% for purchases in 1,000-unit lots.

Supercool AB, P.O. Box 27, S-40120 Göteborg, Sweden.
Phone 46-31-420530. [Circle 708]

QUIET KEYBOARD SPEEDS DATA ENTRY

By using capacitive switching instead of metal-to-metal electrical contacts, Mors Composants has reduced the distance keys travel in its model SR keyboard to 2 mm instead of 3 mm or more, which speeds data-entry and reduces operator fatigue.

Capacitive-switch technology also produces a quieter keyboard and extended life. Mors will modify the SR keyboard by changing the number of keys, layout, and color to suit original equipment manufacturers.

Standard units that are compatible with IBM Corp. Personal Computers and Hull Ltd. computers are available now. Versions for the Digital Equipment Corp. VT220 and VT100 terminals will soon be available.

Availability and price depend on configuration and importing country.

Mors Composants, 42, rue Benoit Franchon, Z.I. Les Vignes, 93000 Bobigny, France.
Phone 33-48-43-58-22 [Circle 710]

STEBUS BOARD MIXES EPROMS AND RAMS

A memory board for the STEbus from Arcom Control Systems Ltd. can handle up to 256 Kbits of battery-backed random-access memory, erasable programmable read-only memory, or electrically erasable ROM.

The SeeRAM board comes with eight 28-pin sockets that accept 8- or 32-Kbit devices and an on-board nickel-cadmium battery with trickle-charger circuitry.

EEPROMs and RAMs can be mixed on the board, provided that the memory chips are all 8- or 32-Kbit devices. Total memory can be positioned anywhere within the STEbus address range with switches that also provide the ability to route the board's trickle-charger current to other modules. Available now, the SeeRAM costs £135.

Arcom Control Systems Ltd., Unit 8, Clifton Rd., Cambridge CB1 4WH, UK.
Phone 44-223-242-224 [Circle 711]

FIFO MEMORIES RUN AT 30 MHz

Two first-in, first-out memories from Philips Elcoma feature independent shift-in and shift-out controls that allow for high-speed synchronous and asynchronous data transfers at 30 MHz. The 74HC7030 and 74HCT7030 FIFO memories have a 64-by-9-bit capacity. They are additions to the company's high-speed CMOS logic range.

The devices afford considerable power savings because current consumption in the steady-state mode is nearly zero. Applications for the FIFOs include high-speed tape or disk controllers, video time base correction, analog-to-digital output buffers, voice synthesis, and bit-rate smoothing.

The FIFOs come in 28-pin dual-in-line or small-outline packages for surface mounting. Corresponding input and output pins are positioned opposite each other to ease pc-board layout. The 74HC7030 has CMOS-compatible inputs and outputs; the 74HCT7030s are TTL-compatible. Samples are about $40 each.

Philips Elcoma, P.O. Box 523, 5600 AM Eindhoven, the Netherlands.
Phone 31-40-757005 [Circle 712]

SIEMENS

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Because PC graphics display more... and better.

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Federal Republic of Germany

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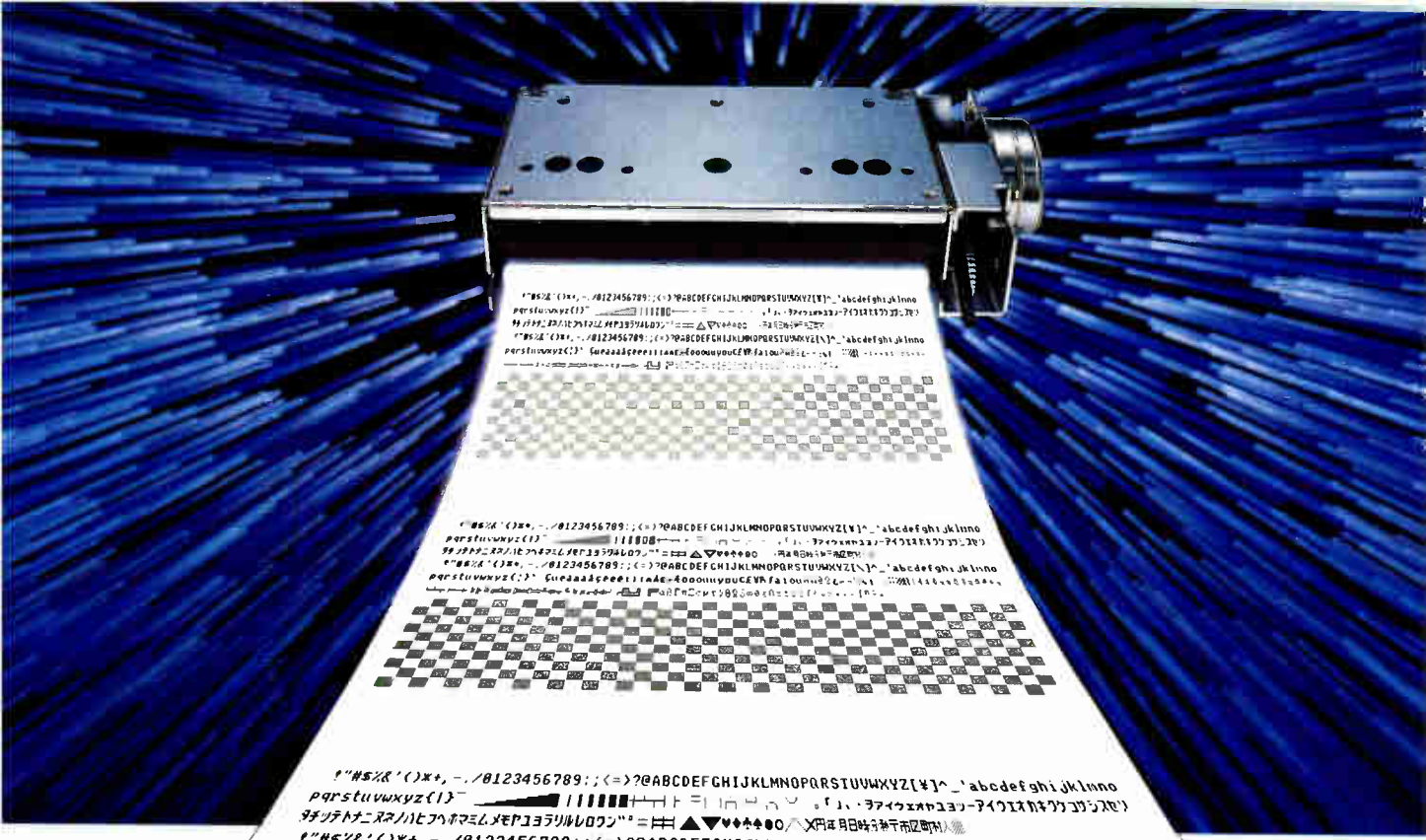
Circle 88 on reader service card

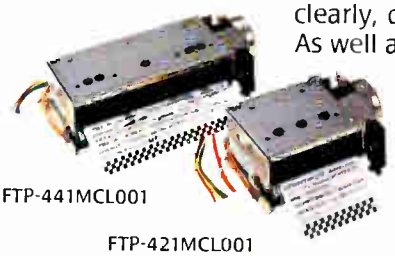


Incredible Speed! 250 dot lines/s

Ultra-high-speed High-resolution Thermal Printer FTP-441MCL001/FTP-421MCL001

Fujitsu has developed the ultra-high-speed thermal printers, the FTP-441MCL001 and the FTP-421MCL001, which can print up to 250 dot lines per second. Fujitsu's unique pressure support structure helps the head to print clearly, and the thermal head makes the printer quiet and unobtrusive.

The FTP-441MCL001 and FTP-421MCL001 print clearly, quietly, and quickly. As well as printing hard copies, they are useful for data communication, instrumentation, analysis, and medicine.



FTP-441MCL001

FTP-421MCL001

FEATURES

- High printing speed (250 dot lines/s)
- Long service life (30km: 30million pulses)
- Clear printing
- Two paper paths (One for thick paper)
- Low noise

SPECIFICATIONS

	FTP-441MCL001	FTP421MCL001
Printing method	Thermal line dot	
Dot matrix	640 dots/line	320 dots/line
Effective print width	105.6 mm	52.8 mm
Horizontal dot pitch	0.165 mm (6 dots/mm)	
Printing speed	250 dot lines/s (at 25°C and 60% RH)	
Paper width	114 mm	60 mm
Exterior dimensions (W) × (H) × (D) mm	160 × 40 × 60	107 × 40 × 60
Weight	Approx. 600 g	Approx. 300 g

FUJITSU MIKROELEKTRONIK GmbH:
Arabella Center 9, OG/A, Lyoner Straße 44-48, D-6000 Frankfurt am Main 71, F.R. Germany Phone: 069-66320 Telex: 0411963 Fax: 069-6632122
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3320 Scott Blvd., Santa Clara, California 95054-3197, U.S.A. Phone: 408-562-1000 Telex: 910-338-0190 Fax: 408-727-0355
FUJITSU LIMITED (Electronic Components International Marketing Div.):
Furukawa Sogo Bldg., 6-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100, Japan Phone: National (03) 216-3211 International (Int'l Prefix) 81-3-216-3211
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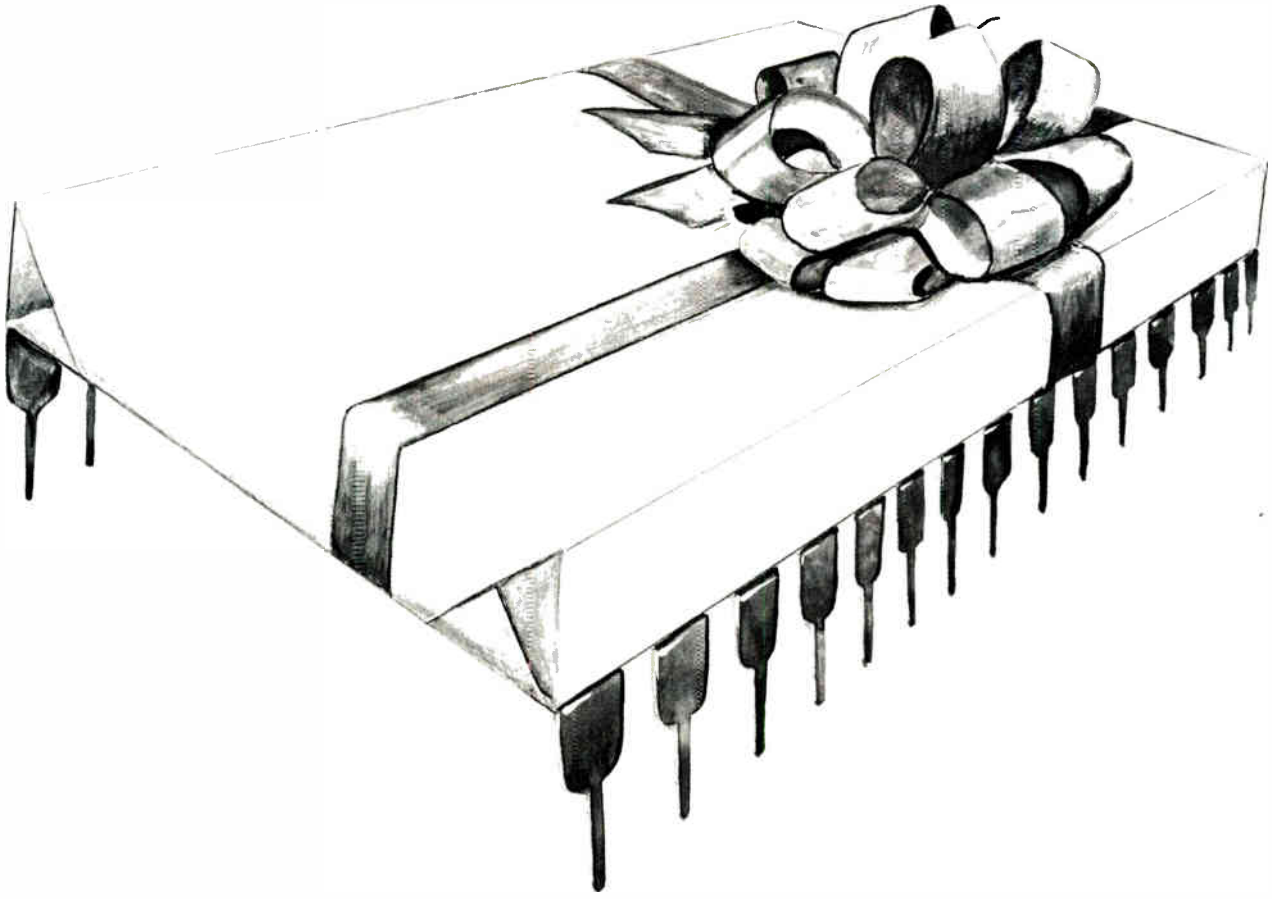
FUJITSU

Circle 89 on reader service card

Packaged To Go.



In the August 20th issue, the editors of *Electronics* magazine unwrap a major report on a new generation of VLSI packaging.

In this special issue, our editors will bare the facts for specifiers of semiconductors faced with a staggering number of new packaging choices. They'll expose what the commodity IC companies in the U.S. and Japan are doing to advance VLSI packaging technology, why the new plastic quad flat pack may displace the leaded plastic chip carrier, and what the industry thinks about copper/polymide packages. In addition to tying up loose ends on tape automated bonding.

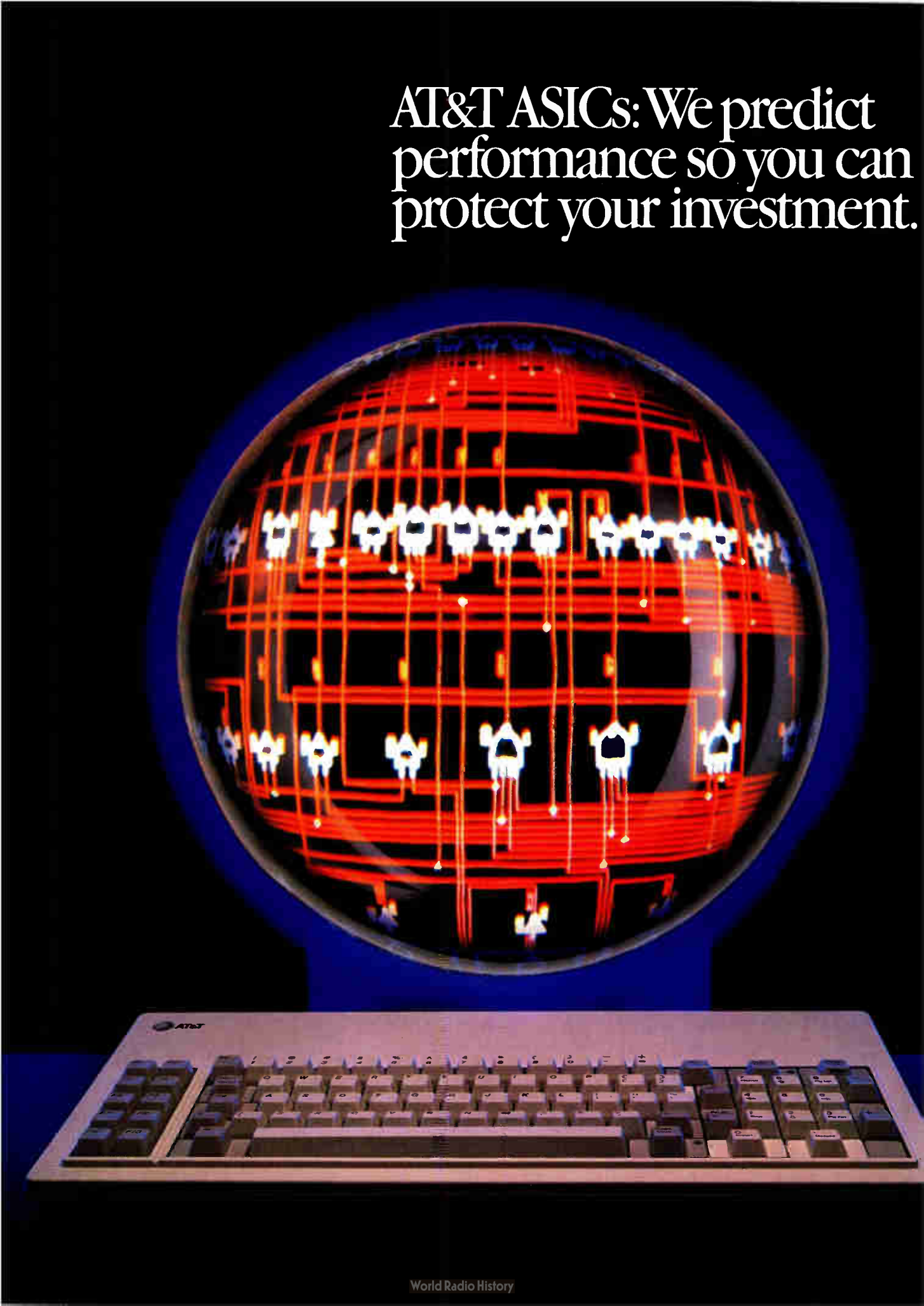
It's a report that uncovers it all.

So if you're a manufacturer of VLSI components, make sure your advertising message is showcased in this issue that opens up exciting new packaging technologies to our more than 131,000 technical management and senior engineering readers.

Ad Closing: July 27, 1987
Recruitment Closing: August 6, 1987

Electronics

AT&T ASICs: We predict performance so you can protect your investment.



Advanced CAD tools, developed by AT&T Bell Laboratories, accurately predict "real-life" ASIC performance.

Sure, you want on-time delivery. Obviously, you want a competitive price. And with an AT&T ASIC, you're assured of both.

But the real bottom line is silicon assurance.

Will your chip work right the first time? Under "real-life" operating conditions? So you don't have to go back to square one?

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In Europe: AT&T Microelectronics GmbH, Freischützstrasse 92, 8000 Munich 81, West Germany
Please send me complete information on AT&T's standard-cell ASIC capabilities.

Name _____
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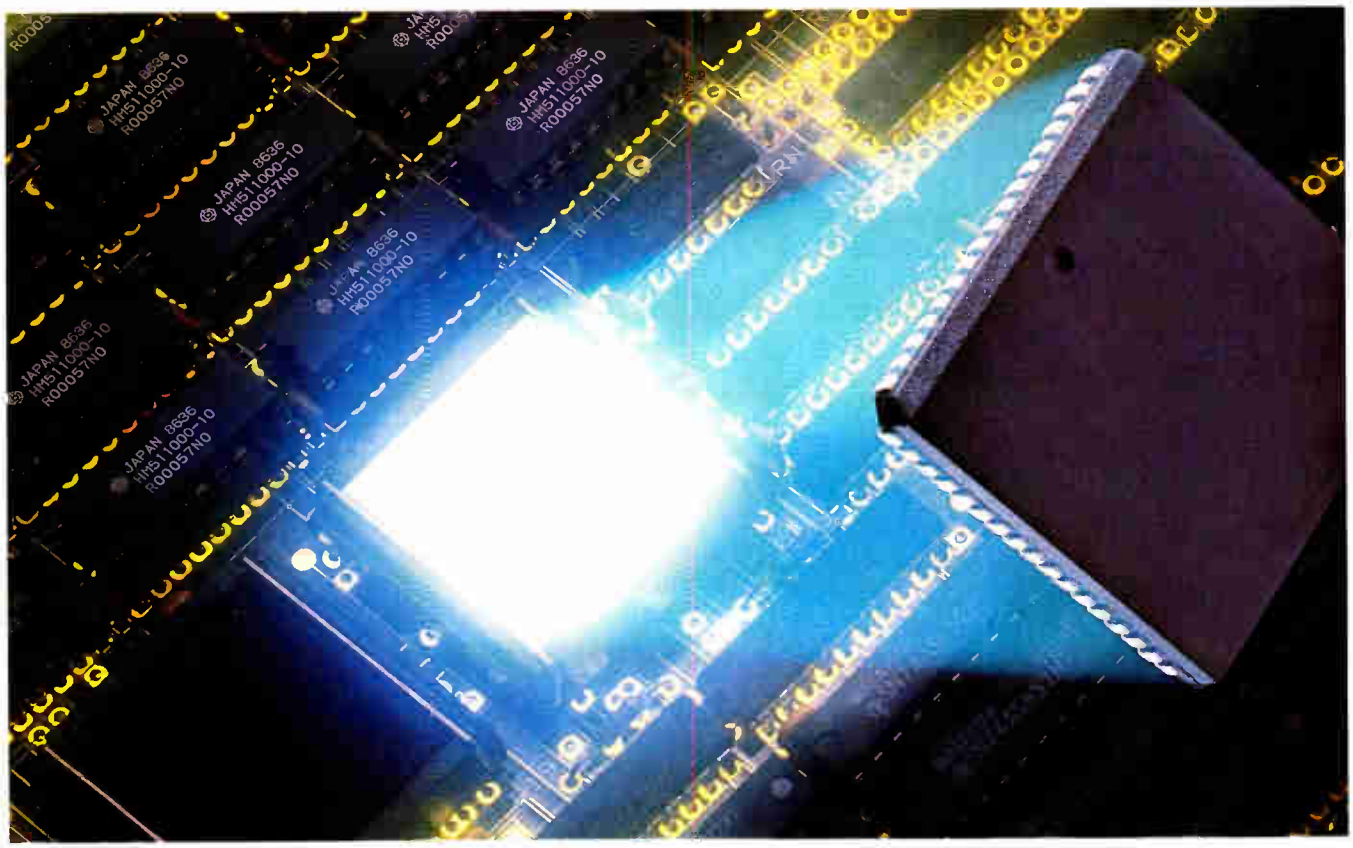

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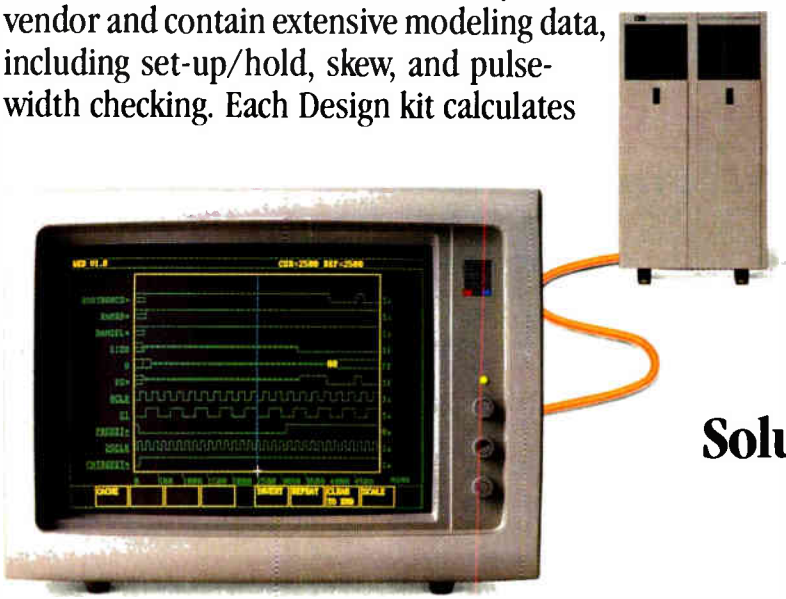

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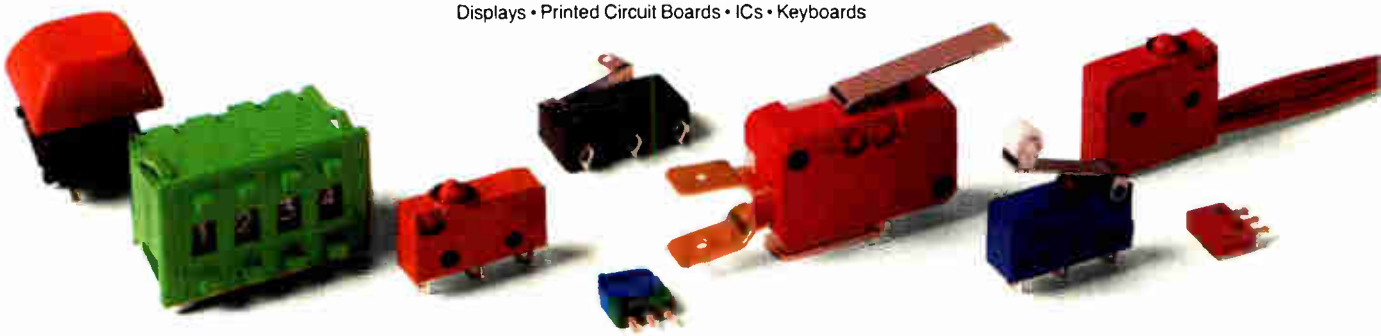

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INSIDE TECHNOLOGY

THE HORSEPOWER RACE IN 3-D GRAPHICS

Manufacturers battle to meet the fast-growing demand for high-powered systems in fields ranging from television to computer-aided design and engineering

by Tom Manuel

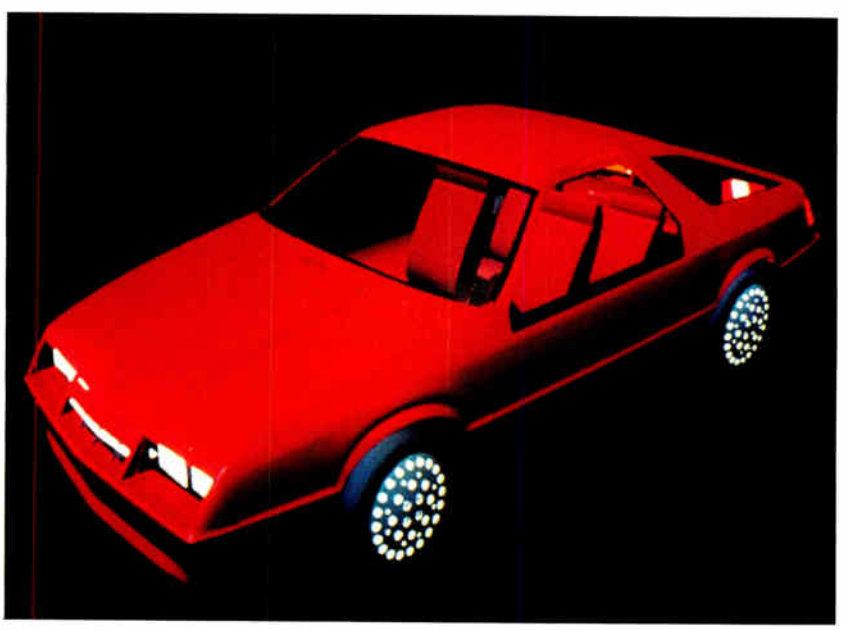
A host of eye-teasing, three-dimensional images generated by computers now pop out of the nation's television screens, obvious proof that 3-d images are fast becoming the most popular feature in computer graphics. And the race is on to deliver the horsepower that 3-d needs: a bevy of manufacturers are vying to produce systems powerful enough to generate and manipulate realistic 3-d images fast enough for interactive operation without costing an arm and a leg. Besides the entertainment world, numerous other important uses for this technology are beginning to show up. The use of 3-d graphics is growing rapidly in such varied disciplines as mechanical and architectural computer-aided design and engineering, cartography, training through simulation, scientific research, and medicine.

The reasonable cost of many of these new products is helping to spread 3-d graphics into new applications. Even the highest-performance products are getting more affordable; many now run around $100,000 instead of hundreds of thousands of dollars. As prices drop and the number of products grows, the market for 3-d-capable work stations will expand dramatically—going from $225 million last year to $2.5 billion in 1990, according to Palo Alto Management Group Inc. in Mountain View, Calif.

The most common form of 3-d output is simulated 3-d on a 2-d cathode-ray-tube screen. The players in this segment are designing more complex and faster integrated circuits, developing more powerful graphics accelerator engines, building 3-d graphics subsystems into work stations, and integrating graphics hardware into large computers. It is this push for high-horsepower 3-d graphics that is yielding both ever-higher realism and more affordable systems.

Besides this traditional simulated 3-d output, another form is now arriving on the market: computer-controlled model fabrication. At least one startup company has developed a computer-output device that produces solid models out of plastic directly from computer data. The rapid model-fabrication process promises to revolutionize the production of prototypes in mechanical CAD.

Complex 3-d images require performance in



1. DESIGN VISUALIZATION. 3-d graphics, like this Chrysler Corp. image produced on a Raster Technologies terminal, allow a designer to visualize a design before models are built.

WHAT EATS UP THE MOST POWER

A substantial portion of the computing power required to produce 3-dimensional graphics is devoted to shading, which creates the appearance of depth in a object displayed on a flat screen. Shading is achieved by filling the polygons making up the screen image with various colors (shades) that represent light reflecting off the surfaces.

The most basic and simple shading technique is called faceting. This takes few computer resources since it involves just filling the polygons with one shade each of a single hue. But faceted shading looks primitive; curved surfaces are no longer smooth-looking, but look as if they were covered with fish scales.

Linear shading, which requires more processing than faceting, produces more realistic images by varying the light intensity across each polygon. The shading is linearly graded from computed values at the polygon's corners. Objects take on a surrealistic artificial smoothness, as though indirectly lighted.

More realism results from grading a polygon's light intensity along its edges as well as at its corners. Called Gouraud shading, this method's drawback is the Mach band effect: a distracting discontinuity between abutting polygon edges. Nevertheless, Gouraud shading is replacing linear shading in work stations as their power increases.

Phong shading eliminates much of the Mach band problem by grading not just along a polygon's edges but across the surface itself. However, the Phong technique requires hardware that can process data at 100 million pixels/s.

Ray tracing offers the most realistic shading in 3-d computer graphics. Its computing-power requirements are still too large for most desktop work stations. However, the extremely complex calculations needed to color each pixel can now be handled by the latest, most powerful graphics engines, collections of networked high-end work stations, and some massively parallel computers.

more areas than just high resolution. For example, millions of colors and complex shading and lighting combinations are needed to produce realistic images. Several different techniques for shading have been developed. As they progress upward in realism, these techniques involve steeply increasing demands for processing power (see "What eats up the most power," above). The most advanced of these techniques, ray tracing, will be a major topic of the technical sessions at this year's Siggraph Conference in Anaheim, Calif., July 27-30 (see "Ray tracing leads the way at Siggraph," p. 53).

2. COMPUTER DRAMATICS. The eye-catching punch of 3-d images like this one by Symbolics are widely recognized in the entertainment industry.

One example of the new high-performance 3-d hardware is the AT&T Pixel Machines graphics engine, which handles both image processing and graphics for host computers (see p. 54). In its top configuration, this system can process 820 million floating-point operations/s: at that speed it can draw and render 3-d images 10 times faster than any competing graphics accelerator.

The push for affordable systems is behind a new frame-memory architecture that Fairchild Semiconductor Corp. says will significantly reduce the cost of high-performance 3-d graphics (see p. 57). Designers at the Cupertino, Calif., company expect the new architecture to achieve drawing speeds in the neighborhood of 15 million pixels/s—fast enough for 3-d wire-frame graphics and inexpensive enough for personal computers.

Realistic visualization is the prime reason for using 3-d graphics in design and engineering applications. Through 3-d visualization, a designer and his clients can see a design more clearly before it is built (see fig. 1). By modeling with a computer, many variations of a design can be evaluated. Often physical modeling can be entirely dispensed with, or at least the number of prototypes and models built can be greatly curtailed, thereby increasing productivity. Interactive 3-d solid modeling will soon be available to designers, engineers, and architects in CAD and computer-aided-manufacturing facilities.

For scientists, interactive 3-d graphics turns large amounts of data from experiments, observations, and theoretical calculations into pictures so that results can be better and more quickly understood. A researcher can watch a theoretical calculation and make changes if it is not going as expected.

In medicine, visualization is also the key; 3-d graphics is being used to create internal body images that can be rotated, panned around, and zoomed in upon, using the data from a variety of scanning techniques such as nuclear magnetic, ultrasonic, and computerized axial tomography.

Computer-generated video images are also being used more frequently in television, especially in TV station and program logos, as well as extensively in advertising, and in movies. These are very often some of the most dramatic examples of computer-generated 3-d pictures (see fig. 2).

Applications using 3-d graphics all require very complex pictures, and most of them need or

can benefit from some amount of animation or real-time interaction—for example, rotating an image. For interactive 3-d and animation, frames must be produced quite rapidly—up to 30 frames per second for real-time animation—and that takes stupendous computer performance.

In fact, users of 3-d graphics systems are always clamoring for more performance. "A consistent cry from customers is that today's products are 10 times to 100 times underpowered for what they need for interactive modeling," says Louis J. Doctor, president of Raster Technologies Inc., a Westford, Mass., maker of high-end graphics engines and terminals.

But where does this kind of performance come from? High-speed numerical-calculation engines are needed to produce an initial image; then many complicated shading and lighting adjustments must be done. A large frame memory—or two or three of them for double or triple buffering—which can be accessed very quickly, is also needed. A Z buffer for keeping depth information is also often included. At the output end, the pixel data in the frame memory must be transformed to analog information and transferred to the display device quickly.

Already the hardware for high-performance 2-d graphics is in place—and is appearing in 3-d systems. Fast microprocessors, floating-point accelerator chips and engines, and minisupercomputer processors can provide the raw computation power needed to execute graphics algorithms. The newest of these processors are getting fast enough for 3-d. Low-cost and dense image-memory chips that have spawned many popular bit-mapped 2-d graphics systems can be useful for 3-d as well. Special multiported video random-access memories for frame memories and Ramdacs (which combine RAM and digital-to-analog converters) for the output stage have pushed 2-d graphics performance higher.

Yet, in spite of all this progress in graphics integrated circuits, there are no VLSI solutions for the very high-bandwidth image memories needed for 3-d. Indeed, even interactive 2-d graphics feels the pinch. And the bandwidths of current image memories and controllers limit most desktop graphics systems to 1 million pixels/s—at least a hundred times too slow for highly realistic, interactive, 3-d graphics.

By far the largest group of vendors and the greatest number of 3-d graphics products are directed towards solids modeling on a color CRT. Among the latest offerings are some new graphics engines and terminals such as the AT&T Pixel Engines PXM 900 graphics display engine and a new graphics terminal engine from Seiko Instruments U. S. A. Inc.

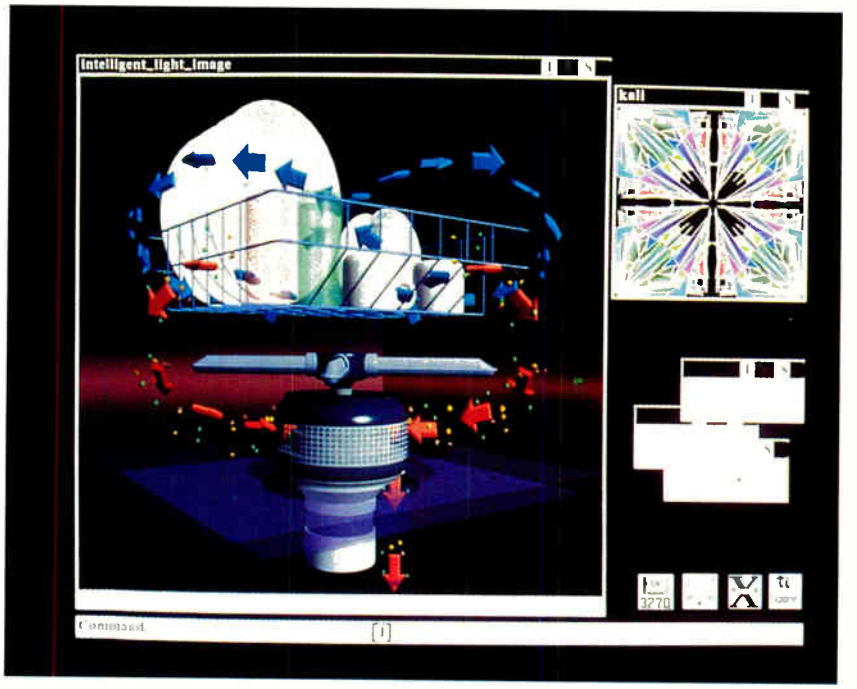
With products like these, designers no longer have to shell out up to $50,000 to buy a 3-d color graphics terminal and display system. For example, Seiko's D-Scan GR-4416 system [*Electronics*, June 25, 1987, p. 95] will sell for only $32,000—underselling rivals by 20% or more.

The rendering of high-resolution 3-d graphics is no longer limited to expensive specialized terminals. Vendors of engineering and technical work stations are driving the power of their work stations high enough to include interactive 3-d graphics in their high-end products (see Fig. 3). One of the latest of these is a new line of work stations from Intergraph Inc. of Huntsville, Ala., which contains a graphics processor for state-of-the-art 3-d display [*Electronics*, June 25, 1987, p. 87]. The new Intergraph line starts at less than $30,000.

The horsepower race in 3-d graphics continues to heat up with a new work station from Silicon Graphics Inc., Mountain View, Calif. The Iris 4D/60T sports a pair of new processors—a 32-bit reduced-instruction-set central processing unit and floating-point coprocessor—from MIPS Computer Systems running at 12.5 MHz to grind out 10 million instructions/s (see p. 80).

Also recently joining the power struggle is Sun Microsystems Inc. The Mountain View, Calif., company has a 10-mips work station, the Sun 4/260CXP, with a new RISC processor that includes Sun's latest GP2 graphics accelerator.

The new Silicon Graphics and Sun work stations should be able to draw 150,000 3-d wireframe vectors/s. The Sun work station steps out in front in rendering 20,000 shaded polygons/s compared to the approximately 5,000 polygons/s from other high-end graphics work stations.

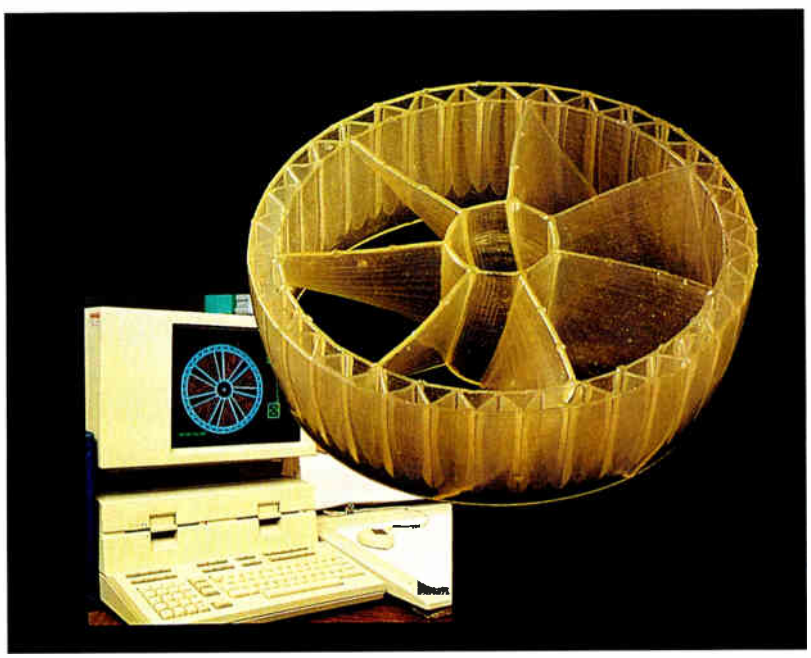


3. 3-d ON A WORK STATION. Apollo Computer's DN590T is an example of the growing breed of high-end technical work stations capable of high-resolution 3-d color graphics.

Those speeds are typical of today's high-end 3-d graphics systems.

Two other work-station companies boast strong entries in the 3-d sweepstakes. Apollo Computer Inc., Chelmsford, Mass. comes in at 4 mips with the DN590T 3-d graphics work station [*Electronics*, May 28, 1987, p. 46]. And Hewlett-Packard Co. put its latest Precision-architecture RISC-style processor in the HP 325SRX work station to deliver 8 mips and 3-d graphics [*Electronics*, May 28, 1987, p. 80].

Another work station that's making a splash in 3-d graphics is the model 3600 from Symbolics Inc. The Westwood, Calif., arm of the Cambridge, Mass., maker of symbolic-processing Lisp computers has developed high-end paint and animation for the 3600. Its four packages include programs for modeling, animation, and image rendering.



4. INSTANT MODEL. 3-d Systems has demonstrated a process that builds accurate 3-d models in plastic from data in a mechanical CAD system, slashing prototyping costs.

In the fourth package, S-Dynamics, Symbolics has developed what it calls behavioral animation. With it, the user specifies rules of behavior for a group of objects. One example is a set of rules for a school of fish or a flock of birds, specifying speed, turning radius, avoidance of obstacles, and group configuration. An animator then can put as many fish or birds in a scene as he wants and tell the whole school or flock to swim or fly past an obstacle.

Terminals and work stations are not the only kinds of hardware used for 3-d graphics. The tremendous horsepower of some very powerful parallel-processing computers is being harnessed to do 3-d graphics. For example, the CM-2 Connection Machine, a 2,500-mips supercomputer with up to 65,536 processors made by Thinking Machines Inc., of Cambridge, Mass., has a graphics display as a built-in feature. The integrated graphics allows CM-2 users to monitor computations as they run.

Since the Connection Machine has a data-parallel architecture, which associates elements of processing power directly with elements of data and operates on all those data elements at once, the graphics window into the machine gives users the ability to see the ongoing progress of complex calculations and gain immediate feedback and understanding of how they are proceeding. Users can intervene if a computation is not progressing towards a solution, make changes, and then proceed.

Another parallel computer that is being used as a graphics engine is the Computing Surface made by Meiko Ltd. of Bristol, England [*Electronics*, Nov. 27, 1986, p. 56]. The general-purpose Meiko Computing Surface can start small at $10,000 with a few Inmos T800 floating-point transputer processors and grow to a few thousand processors. So it can be a powerhouse server for work stations with 3-d graphics—it can do the calculations for complex ray-traced images in tens of seconds instead of hours and days.

Perhaps the ultimate 3-d output is one that users can not only see, rotate, and zoom into, but one they can touch as well. Such an output has been demonstrated. Computer-generated models were converted to solid plastic models in the lab (see fig. 4), thanks to an output device made by a year-old Sylmar, Calif., company, 3-d Systems Inc. The company has developed a computer-driven technology for making models, which it calls "stereolithography."

The technique produces actual parts in minutes by projecting the pattern for successive thin layers of the model upon the surface of a vat of photosensitive liquid plastic. The ultraviolet laser used in this process solidifies the plastic only where it touches the surface of the material. The model is built up one layer at a time, and successive layers quickly build up a plastic solid model.

Making plastic models for mechanical CAD is only the beginning of the possible applications for stereolithography. A proposed medical application would be making models of fractured bones from CAT scans for physicians to study before surgery. And architects should welcome the opportunity to make models of their structures directly from CAD data. In the realm of science, photolithography can be used as a 3-d plotter to show data relationships or to make maps.

Feasibility of the 3-d Systems' process has been demonstrated, and a developmental prototype has been built and is being shown to key prospects. Deliveries of the first systems is expected sometime in 1988. □

RAY TRACING LEADS THE WAY AT SIGGRAPH

Ray tracing is the hottest area in three-dimensional computer graphics, and as such it will be one of the most discussed topics at the Siggraph '87 conference in Anaheim, Calif. In ray tracing, rays from simulated light sources are traced along their paths in a simulated 3-d space to see where they will strike objects and how they will reflect. It produces very realistic images, but places heavy performance demands on the computer.

As with most other topics to be discussed at the July 27-31 conference hosted by the Special Interest Group on Computer Graphics, two basic goals are driving the ray-tracing work: reducing the amount of computer power it takes to generate complex images, and improving the realism of the images generated. Key papers will report on clever new algorithms speeding up the execution of graphics tasks. Other papers will tell how the accuracy and realism of computer-generated images are being improved by applying the principles of physics, both the physics of light and basic Newtonian physics, to model the behavior of moving objects.

The ray-tracing performance issue is one of how much detail can be rendered by a computer in a specified period of time. Ray-tracing algorithms have gotten much faster over the last five years, leading up to this year's *tour de force*, an image ray-traced in 12 hours by an IBM 4381 computer and containing about 400 billion polygons. The image, a sea of grass with tens of millions of blades (see photo), was made by John Snyder, a graduate student in the California Institute of Technology's Computer Science Graphics Group in Pasadena. In a paper coauthored by Alan Barr, an assistant professor at Caltech, Snyder will describe how he organizes data structures to speed up image generation by making it easier to find objects in the data base.

But faster ray tracing won't go into widespread use unless it can be done with far less of the expensive computer power that it now takes. That's why "the hottest areas in ray tracing have to do with optimizations—speeding up the technique," says James Arvo, a software engineer from Apollo Computer Inc., Chelmsford, Mass. "Ray tracing would find its way into many, many applications if it weren't so expensive." For example, it renders the reflections of light in glass windows in architectural computer-aided design and light reflecting from curved surfaces in the modeling of cars.

Arvo and David Kirk, another software engineer at Apollo, are coauthors of a paper that describes a new way to organize the data used to generate the image, speeding up the process about four times compared to what could be done a year ago, Arvo says. The algorithms he uses take advantage of the fact that a ray in 3-d space is mathematically equivalent to a point in five-dimensional space: that is, a ray is represented by three coordinates for its starting point and two angles that define its direction of travel. Many of the problems of ray tracing become simpler with this mathematical foundation, says Arvo, and many new optimizations are possible.

RAY-TRACED. This image of a grassy field from Caltech contains 400 billion polygons.

But light in the real world does more than travel in straight lines and bounce off smooth surfaces. It passes through air, and scatters as it does so; reflections from surfaces like painted walls are diffuse, complicating realistic simulation. Papers in the Lighting Models session address these issues. Two of them are from Cornell University, Ithaca, N. Y., where a group of computer graphics researchers are working to match image synthesis with the the way real light propagates and reflects.

These are some of the fine points of image synthesis, and the Siggraph papers covering them show how mature this technology has become. "Rendering—making pictures of objects—is almost a completely solved problem," says Caltech's Barr, citing an influential paper given by Caltech associate professor James Kajiya at Siggraph '86. That paper, "The Rendering Equation," describes a methodology for simulating complex light behavior. Computer-graphics modeling of solid objects that move over time, on the other hand, "has been in a hopelessly primitive state," says Barr.

But he and Caltech graduate student Ronen Barzel hope to usher in the next generation of computer-graphics modeling in a Siggraph tutorial. "Graphics has all along dealt with shapes—shapes without physics," says Barr. Now he and Barzel have developed the mathematics for what they call physically based modeling. It takes into account the physical forces that act on objects being modeled, as well as the elasticity of materials and stresses and strains.

"We're able to do inverse dynamics," says Barr. "That is, we calculate the forces that result in the motions we want. Previously we only had a kinematic description of what an object was doing—its position and orientation." With physically based modeling, the user can specify a goal, such as "put the cube on the table," and the computer calculates the forces that must act on the cube to get it there. It can then model the way the cube would move. This kind of modeling will be vital in simulating the motions of robots and in computer vision, says Barr. *–Jeremy Young*

AT&T GOES TO 'WARP SPEED' WITH ITS GRAPHICS ENGINE

It can draw and render 3-d images 10 times faster than any competing graphics accelerator, thanks to a parallel architecture that speeds access to the frame buffer

by Stan Runyon

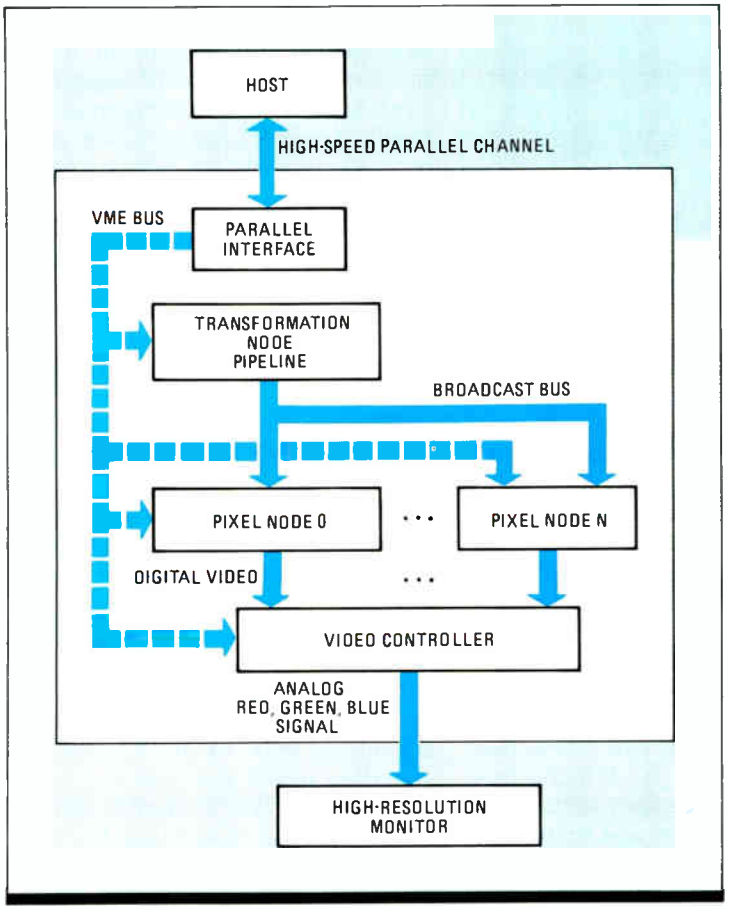
A new high in high-performance, three-dimensional graphics processing is on the way from AT&T Pixel Machines. The Holmdel, N.J. unit of AT&T Co. says its PXM 900 series graphics engine can draw and render 3-d images 10 times faster than any competing graphics accelerator.

The top-of-the-line PXM 964 zips along at 820 million floating-point operations/s. Put another way, it can transform 200,000 vectors/s and display 16 million Gouraud-shaded pixels each second. It is so fast, in fact, that it manipulates and shades color images as fast as any competing graphics work station rendering just wire-frame images.

To achieve the impressive speed, the PXM 900's designers went to a parallel architecture. Their goal was to eliminate one of the major bottlenecks in graphics displays—accessing the frame buffer. The parallel architecture consists of up to 64 distributed digital signal processor chips that take the place of the typical single processor found in other graphics engines. Each of these processors addresses its own portion of the frame buffer, which greatly speeds up access. Distributed addressing also allows for a hefty 48 megabytes of frame buffer—and the larger the buffer, the more realistic the image.

These distributed processors are AT&T's DSP32, a programmable 32-bit floating-point DSP chip. There are from 16 to 64 of them in the different models of the PXM 900 line. In effect, they serve as a multiple-instruction, multiple-data-stream machine—each runs the same algorithm. But the algorithms, which are resident in each processor, run independently, and the data varies from processor to processor.

The PXM 900 is modular: users can add more processors and expand the frame buffer in order



1. PARALLEL ARCHITECTURE. Independent pixel nodes drastically speed up image drawing and rendering.

to boost speed or produce better images. Software compatibility is preserved across the different configurations. Users also can program the machine to match particular applications and so run a variety of algorithms.

Unusual is the 900's ability to handle both image transformations and graphics, or pixel, operations. Typically, the host computer performs the image-processing transformations.

The PXM 900 series is linked by a VMEbus to a host work station, such as a Sun series 3/100 or 3/200. Its speed will suit it to applications involving animation, simulation, modeling, CAD/CAM, and scientific research. AT&T Pixel Machines will introduce the new line at Siggraph '87, July 27 through 30, in Anaheim, Calif. It will go on sale in the fourth quarter at prices ranging from $45,000 to $100,000.

Display resolution can go as high as 1,280 by 1,024 pixels, at 32 bits per pixel, in the fully-configured PXM 964 displaying 16 million Gourald-shaded pixels/s. (Gouraud shading is a widely used algorithm that interpolates light intensities of adjacent pixels on polygon-based images.)

Running the more sophisticated Phong-shading algorithm slows the PXM 964 to 2.25 million pixels/s, but produces more realistic images. The Phong algorithm derives its shading information, not only from the edges as does Gouraud shading, but also from across the surfaces of the polygons themselves for far more realistic images.

Another example of the 964's blindingly fast performance is its ray-tracing speed of 1 million intersections each second. To trace the same number of rays, a VAX minicomputer needs hours; a Cray supercomputer, minutes.

The parallel architecture of the PXM 900 series is a sharp departure from the configuration of present-day graphics engines. Some accelerators use a single processor—but one processor working alone soon runs out of steam because it must handle too much data in too little time: 8 Mbytes for a double-buffered, 1-Kbit-by-1-Kbit, 32-bit/pixel display. Other engines use a series of processors, with each taking care of its own operation, such as drawing lines or moving blocks of data. Performance is usually better than in a single-processor machine; however, processing still proceeds sequentially and that limits maximum speed. Also, the specialized processors of this setup cannot run one another's operations.

The Pixel Machine approach (see fig. 1) attacks the bottleneck with its distributed processing method. Graphics information from the host is fed to a processor pipeline, called the transformation pipeline, which manipulates the data and passes it to an array of processing elements, or pixel nodes. Each processor in the array is dedicated to managing a portion of a very large frame buffer, 48 Mbytes in the largest configuration, and each connects to its buffer portion via its own bus. Once the nodes have worked over the data, they send it to the video controller through a high-speed backplane, or bus, called the pixel funnel.

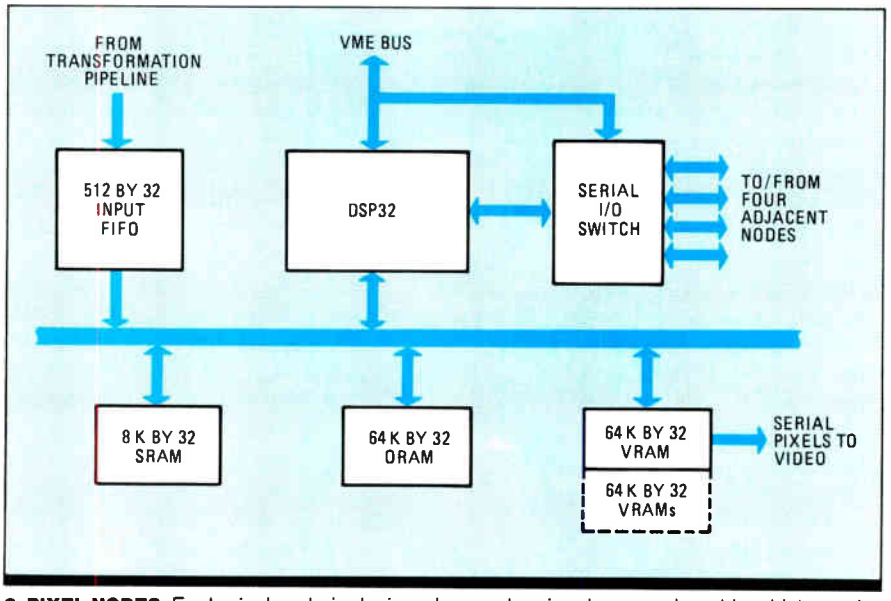
The processors in the pipeline and in the nodes are AT&T's DSP32, executing instructions at 10 megaflops. AT&T is just launching an enhanced version of the DSP32 (see p. 00), which should considerably boost the speed of the PXM 900. With individual programmable processors working over individual buses, bandwidth is stretched; there is a better balance between memory and processing; and a variety of algorithms can be implemented directly in the frame buffer—there is no need for a separate floating-point number cruncher. The result is improved efficiency, higher throughput, and greater interactivity.

The transformation pipeline accepts high-level geometric primitives from the host and computes all necessary transformations for manipulating an object in three dimensions—rotation, clipping, scaling, shading, and the like. It maps 3-d object space to 2-d screen space and broadcasts the results to the pixel nodes.

The pipeline consists of either 9 or 18 DSP32 processing elements, connected sequentially. Each processor performs its function and passes the data to the next processor.

The pipeline processors are mounted on a VMEbus-based board, nine to a board. Two pipeline boards can be connected and configured for serial or parallel operation under software control. Since each processor is programmable, the user can reconfigure the pipeline for various functions, such as rotation, scaling, or translation of the image.

Taking the data from the pipeline, the pixel



2. PIXEL NODES. Each pixel node is designed around a signal-processing chip which can be reprogrammed to run various algorithms.

nodes (see fig. 2) compute pixel colors and intensity, with each node controlling its portion of the bank of video random-access memories that make up the frame buffer.

One of the key innovations in the PXM 900 is the pixel interleaving scheme through which the sharing of the frame buffer takes place. This scheme achieves uniform load balancing among the processors by arranging the DSP32 chips in an n by m array, with each processor in the array controlling the nth pixel on the mth scan line. The result: speed increases almost linearly with the number of processors.

The pixel-node array can address up to 32 Mbytes of self-contained frame-buffer memory and 16 Mbytes of off-screen (external) memory. The basic configuration, the PXM 916, contains 16 pixel nodes, with 96 bits per pixel—64 for a double-frame buffer and 32 for a Z buffer, which stores each pixel's screen depth (Z value).

Because the parallel architecture speeds up access to the frame buffer, the 900's designers could implement the deep, 32-Mbyte buffer without sacrificing update speed. With 32 bits per pixel, 24 can be devoted to color, and 8 to overlays, all consuming just 4 megabytes of the buffer.

The Z buffer improves the image even more by contributing a three-dimensional effect to each pixel. Again, because of the buffer's great speed, each pixel can carry 32 bits of Z buffering instead of the usual 8 or 16. The advantage is realized with images in which the edges of objects overlap. Z buffering consumes another 4 megabytes of the frame buffer.

Yet another benefit of the buffer's size is improved animation speed. Instead of the conventional double buffering scheme, the 900 has the capacity to step up to quadruple buffering in the top three models. With double buffering, as the video controller removes data from one frame buffer for display, the display processor can begin to work on the other buffer, getting ready for the next screen update. But once the processor finishes with the backup buffer, it has to wait until the current buffer empties—up to 15 ms at a 60-ns refresh rate. Triple or quadruple buffering eliminates the idle time; the processor can go right to the third and fourth buffers.

Another key element is the PXM 900's pixel funnel. Its job is to accept the information from the pixel nodes' frame buffers, multiplex it, and pass the stream to the video controller. This is no mean feat because of the speeds at which the information must be concentrated. Since the pixel-node array is reconfigurable, so must be the funnel. This is done through software.

The video controller, the last stop for data before the color monitor, receives 32 bits of information from the funnel—8 bits for each of the primary colors and 8 for an alphanumeric overlay. It delivers a 30-bit video signal. With 30 bits, dynamic range is wider than that provided by standard 24-bit video, and the picture quality is better. □

AT&T RACED THE CLOCK WITH THE PXM 900

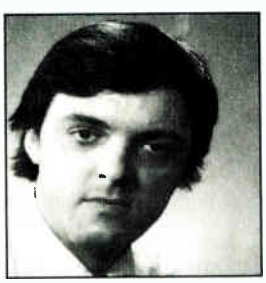
For the designers of the AT&T Pixel Machines' PXM 900 graphics display engine, it was a race against the clock—and a risky race, at that. The goal was a showing at Siggraph '87, the premiere graphics conference. By the time the design team was in place, the July conference was less than a year away.

"The innovative design involved in the parallel architecture—and especially the pixel node and funnel designs—involved considerable risk for the designers, given the relatively short time we had to produce a working product," says Alessandro Piol, marketing director for Pixel Machines. "We were not sure whether this idea would work or not."

AT&T had assembled a diverse design team, drawing from various research and development activities at Bell Labs. James Conant, 33, for instance, Pixel Machines' director of engineering and one of the two leaders of the team responsible for the PXM 900's development, ran a VLSI system design group in Bell Labs' Government Systems Division. The other principal, Michael Potmesil, 34, codesigner of the PXM 900 architecture with Leonard McMillan, 26, came out of the Bell Labs Computer Systems and Robotics Research Lab. Potmesil has spent the last 12 years working on computer graphics. McMillan and others hailed from Bell Labs' development group for digital signal processors. Before that, McMillan worked on advanced parallel machines at Georgia Tech.

JAMES CONANT

LEONARD McMILLAN



MICHAEL POTMESIL

The plan for the PXM 900 was to leverage the speed and power of AT&T's DSP32 signal processing chip into an advanced graphics system. Naturally, the chip's designers were the best source of knowledge for that. As for graphics knowledge, there could be no better fountain than Bell Labs.

Luckily—or cannily—designers on the graphics side had experience in implementing algorithms on parallel machines. Others had been involved with hypercubes, software, image processing, and the like. Marc Howard, 30, the creator of the Pixel Funnel, had 13 years of computer graphics under his belt, and Eric Hoffert knew all about video animation: his work has been displayed in the Museum of Modern Art in New York, and elsewhere.

Did AT&T win its race against the clock? A demonstration at Siggraph, July 27 through 30, in Anaheim, Calif., should tell.

TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*

FAIRCHILD AIMS TO MOVE HIGH-END GRAPHICS TO PCs

It has a new concept in frame-buffer architecture that can be implemented with garden-variety DRAMs, yet provides the speed needed for 3-d image drawing

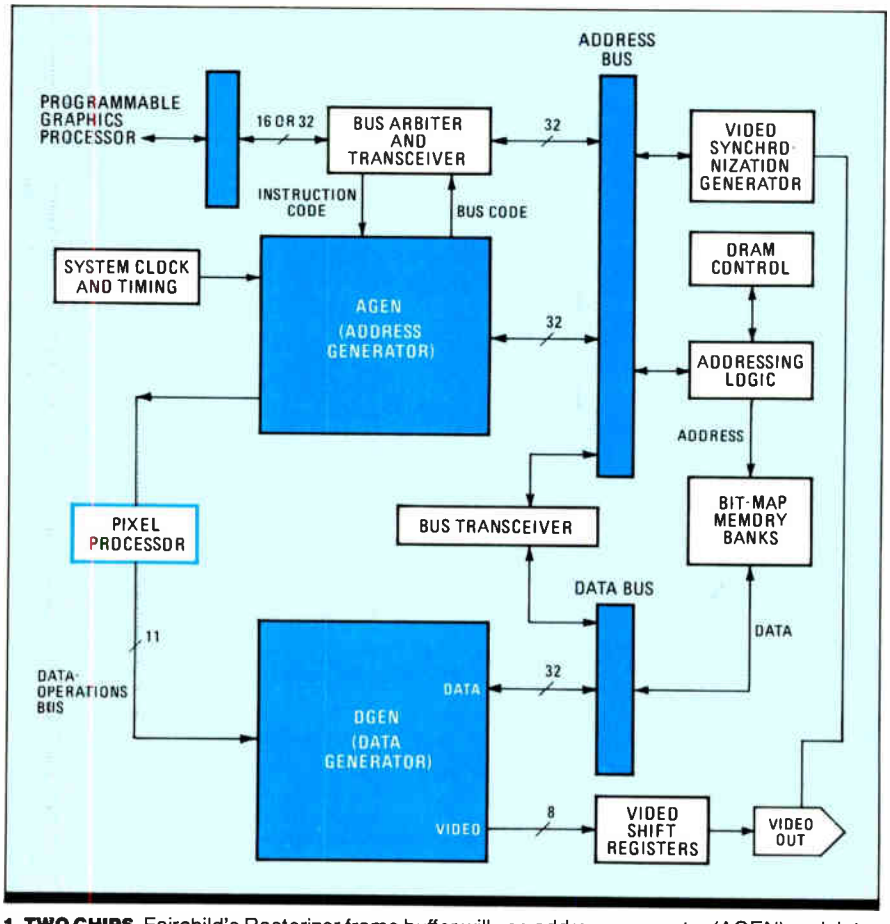
by Samuel Weber

Desktop computer graphics, long mired in the flatness of a two-dimensional world, is on the threshold of the third dimension thanks to a new concept in frame-buffer architecture. Fairchild Semiconductor Corp. has devised a low-cost, reconfigurable frame-buffer architecture having sufficient bandwidth to provide a fast enough read/write access time for 3-d graphics on personal computers. Called the Rasterizer, the Fairchild hardware dramatically slashes the time needed by the image memory to refresh the screen of a cathode-ray tube. The Cupertino, Calif., company is now working on the two integrated circuits that are the key to the new architecture.

The Rasterizer's architecture will be inexpensive enough for personal computers because it can be implemented with garden-variety dynamic random-access memories. Such a frame buffer, capable of performing primitive 3-d graphics, will cost no more than current 2-d implementations, Fairchild says. However, it's also possible to use faster RAMs for even higher performance, and so the new architecture can be applied to graphics applications on all levels, not just to PCs.

But it is the reconfigurability that gives the Rasterizer its speed: the new ICs can dynamically reconfigure the RAMs that make up the frame buffer to the most efficient structure for each type of line or shape. When populated with 100-ns DRAMs, the Rasterizer can operate at a rate of 15 million pixels/s for drawing vectors (screen refresh included). This is an average of 7.27 pixels/s per write cycle and a peak of 16. If static RAMs replace DRAMs, the average vector-drawing rate rises to between 20 and 25 million pixels/s.

Translating pixel drawing rates to wire-frame vector-writing rates, the Rasterizer populated



1. TWO CHIPS. Fairchild's Rasterizer frame buffer will use address-generator (AGEN) and data-generator (DGEN) chips: one AGEN per system and one DGEN for each memory plane.

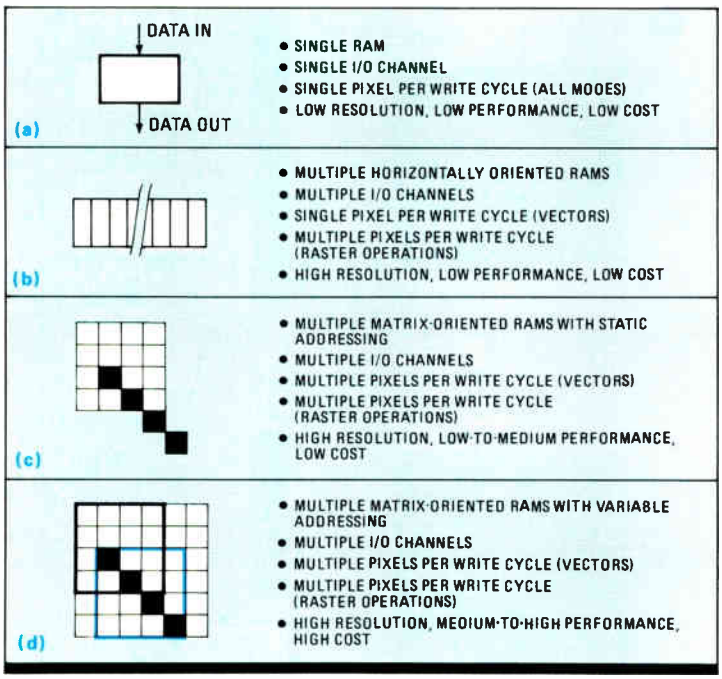
with garden-variety 100-ns DRAMs can write vectors to the screen at a rate of 1 million/s. The speed of the typical high-end 3-d systems is between 100,000 and 200,000 vector/s.

The Rasterizer architecture also speeds through other graphics operations: 80 million pixels/s for a bit-block transfer, 80 million pixels/s for filled polygons, and 45,000 characters/s for text. These are average, not peak speeds—peak speeds range from double to triple the average figures.

In computer graphics, video-output devices perform such back-end operations as digital-to-analog conversion, selecting colors from the available pallette, and display management. In all this, the key to high performance is in the frame buffer and its control. The frame buffer, also known as a bit map or image memory, stores all pixel information needed to describe images on standard raster-display CRTs.

The immediate impact of the Rasterizer frame-buffer design will be felt on wire-frame 3-d graphics drawn on a screen with vectors that are simply straight lines and faceted shading, says Michael L. Fowler, advanced product planning manager at Fairchild's digital and analog division in South Portland, Me. Many 3-d CAD/CAM applications ranging from electrical schematics to mechanical drafting use wire-frame images rather than Gouraud or Phong shading.

A wire frame describes the edges and envelope of an object's geometry. It is essentially a collection of polygons whose boundaries are defined by vectors—the entire area within a polygon need not be filled in. "But the chips we are planning for this architecture will provide hardware and software interfaces or 'hooks' for implementing displays with more realistic shading techniques, such as Gouraud or Phong shading," he says.



2. FOUR GENERATIONS. The first frame buffer was just a single RAM (a). Next step (b) was to gang RAMs together to generate multiple pixels during each write cycle. The third generation (c) opened the way to efficient writing of vectors while the fourth generation (d) speeds the vector writing process for 3-D graphics.

The Rasterizer hardware (see fig. 1) will span a range of applications, from low-cost personal computers to sophisticated high-end work stations. It implements four fixed graphics functions applicable to 2-d and 3-d systems: vector, polygon, bit-blt (bit block transfer) and char (characters). These functions are hard-wired to provide high-speed operation.

The heart of the Rasterizer concept is two very large-scale ICs, the address generator (AGEN) and data generator (DGEN). The AGEN is the element that controls frame buffer addressing. In the simplest Rasterizer configuration, a single AGEN controls all the frame-buffer memory planes, and a single DGEN modifies frame-buffer data and composes this data for video output. Fairchild plans to implement these chips in 1.5-μm advanced CMOS; they should be available early next year.

For high-performance graphics applications, the new Fairchild frame buffer can be populated with video random-access memories, but for the majority of microcomputer graphics, standard dynamic RAMs with 100-ns access times are adequate. For the highest-performance graphics systems, the Rasterizer can use fast CMOS static RAMs, now offering 25-ns access times.

Even with the fastest RAMs, most low-cost frame buffers used in 2-d graphics subsystems are inefficient at drawing 3-d wire frames. The way in which these buffers store 2-d pixel data, a method called word mode, works best for generating horizontal lines. "But lines are rarely horizontal; in most cases, they cut across the screen at an angle," Fowler points out. "So the frame buffer must read out data for as many horizontal lines as a vector cuts through before completing a single vector."

The data for the entire horizontal line must be read even though just a single pixel of information is required on each line. In effect, this amounts to drawing a single pixel for each write cycle. But such an operation slows the system's writing speed, making conventional frame buffers inefficient in 3-d applications.

To speed the writing process, two approaches compete: reorganizing the storage of data in the frame buffer or speeding up the graphics hardware. A reorganized buffer scheme is attractive because it hikes the rate of obtaining the data needed to draw vectors—so it increases the bandwidth efficiency of the graphics systems without the costly tactic of adopting sophisticated hardware.

A reorganized frame buffer usually can optimize a graphics system for the relatively low bandwidth needed for 3-d wire-frame graphics. Because wire-frame graphics involves envelopes

rather than filled-in areas, it can be handled by an effective bandwidth in the range of 10 to 20 million pixels/s. Of course, for maximum writing speed, both a reorganized frame buffer and enhanced hardware can be adopted.

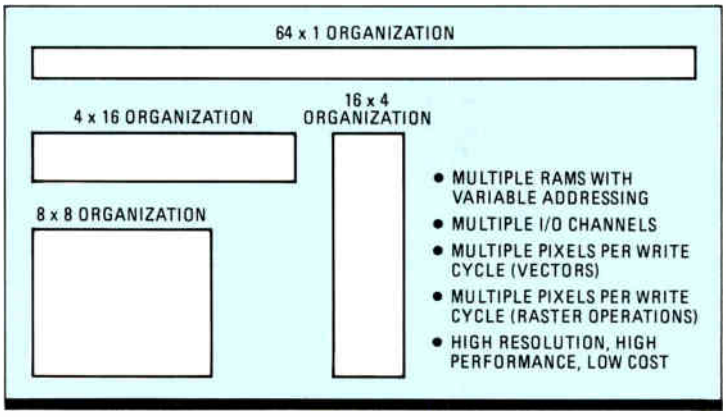
Today's complex frame-buffer designs are a far cry from the first crude attempts to use a single memory chip to store information for graphics displays. This lone DRAM (see fig. 2a) is, in reality, a graphics memory with a single input/output channel and an output of a single pixel per write cycle. It has extremely poor resolution, and its speed is so slow as to prevent the actual display of information on a CRT.

The second generation of graphics memories was a chain of DRAMs (see fig. 2b). In this multiple-I/O-channel scheme, multiple pixels can be written to the screen during each write cycle. This configuration is suitable only for writing pixels horizontally. Resolution increases with the number of DRAMs in the chain—but system performance remains relatively poor since this scheme can still draw only one pixel per line scan. For vector operations, second-generation frame buffers can generate about 1 to 2 million pixels/s.

Third-generation architecture is identified with the concept of a 2-d cell: a matrix of DRAMs configured for graphics (see fig. 2c). In a 2-d system, a cell can be a 4-by-4 array of DRAMs, an 8-by-8 array, or an asymmetrical arrangement, and it can generate data for multiple pixels during each write cycle. Each RAM chip within a cell is assigned to a specific pixel location on the screen, a technique called static addressing. The cell concept permits high-performance images to be produced at low system cost: a third-generation frame buffer operates at rates in the range of 6 million pixels/s. But this type of cellular graphics is not well-suited to such raster operations as refresh, bit-blt, and polygons because it, too, can draw only one pixel per line scan.

The cell concept is taken a step further in fourth-generation frame-buffer architecture (Fig. 2d), where the address of each RAM chip is variable. This allows a given cell to be assigned to various pixel locations on the screen. The fourth-generation architecture can write vectors to the screen at typical speeds of 10 to 20 million pixels/s. The drawback—particularly for microcomputer-based systems—is its high cost, a result of the overhead needed to support variable addressing of DRAMs within a cell.

All of the benefits embodied in third- and fourth-generation architectures are incorporated in the Rasterizer fifth-generation frame buffer (see fig. 3). However, this architecture goes further in terms of optimum flexibility. Through a combination of the Rasterizer's chip-set design and its built-in algorithms, the cell orientation can be dynamically configured four different ways, depending on the type of vector to be drawn. To draw horizontal vectors, a 4-by-16 array of RAMs is the most efficient since it delivers the maximum number of pixels (16) per write cycle. Similarly, to draw vertical vectors, a 16-by-4 array optimizes performance by drawing 16 vertical pixels per write cycle. And when vectors must be drawn at an angle—cutting through horizontal lines—the 8-by-8 array provides the best results. Finally, the word mode, which was lost in the previous two generations, is reinstituted in the Rasterizer in the form of a 64-by-1 array of RAMs. □



3. RECONFIGURABLE. The fifth-generation Rasterizer frame buffer dynamically organizes memory into various array sizes.

For more information, circle 481 on the reader service card.

HOW FAIRCHILD FOUND A NICHE IN GRAPHICS ICs

When planners at Fairchild Semiconductor Corp. decided to jump into the graphics market about 2½ years ago, they recruited Michael L. Fowler to define a graphics strategy for the company. Fowler's first conclusion was a negative one: it was already too late for the Cupertino, Calif., company to come into the market with a graphics engine, unless it could bring something special to the party.

So he set about talking to graphics systems designers to find out what they wanted. "The thing almost everyone wanted most was flexibility of the system interface," he says. "They wanted to be able to match the graphics engine easily to the specific system they were designing." His recommendation was to concentrate on optimizing the performance of the frame buffer.

It took two years to come up with the reconfigurable architecture embodied in the Rasterizer. When it's fully implemented, Fowler says, system designers will be able to achieve a wide range of graphics performance levels—up to 10 times that of currently available sytems, without any need for special high-speed memories.

Fowler, 34, has a BSEE from Southwestern Louisiana University, He had almost six years of graphics-design experience behind him—as a work-station system designer, then a hardware design manager at now-defunct Phoenix Computer Graphics in Lafayette, La., and at Day Telecommunications in Raleigh, N. C. He is now advanced product planning manager for Fairchild's digital and analog unit.

MICHAEL L. FOWLER

SYSTEM SNAGS SHOULDN'T SLOW THE BOOM IN FAST STATIC RAMS

Growth continues at 17% annually, as makers maneuver around noise and test problems

by J. Robert Lineback

Static random-access memory makers have the pedal to the floor in their race to cut access times and grab shares of a market growing almost 17% a year. But even as the devices gain speed, and strengthen their position as the advanced CMOS technology driver, a bunch of nagging problems are cropping up.

The biggest problems are how to maneuver around noise problems caused by fast-switching output pins and how to clear the speed barriers encountered in system design. As a result, many companies in the growing ranks of fast-SRAM manufacturers are working hard on new pinout schemes and self-timing architectures.

Another growing problem that SRAM makers are attacking is testing: the mixture of higher densities and speeds is proving more difficult to test as transistor geometries drop below 1 μm. At the same time, lack of fine-line production capacity is forcing some manufacturers to put off the introduction of new chips, even as the Japanese—led by Fujitsu and its promised 1-Mbit SRAM—and Philips of The Netherlands set a brisk design pace.

Despite all that, fast SRAMs remain one of the best commodity sectors for American silicon houses, says Victor de Dios, senior industry analyst at Dataquest Inc. in San Jose, Calif. Dataquest predicts world sales of fast MOS-based SRAMs—those topping 70 ns—will rise by an annual rate of 16.8% from the mid-1980s to 1991, even though wider use will make them susceptible to general industry cycles, beginning with the flat 1988-89 period (see chart, below). Average MOS memory growth for the same period will be 15%, says de Dios.

Moreover, "the U. S. market for fast SRAMs is reasonably protected from the Japanese competition, compared to other memory devices," de Dios believes. Strong emerging military markets and the kind of commercial companies buying fast SRAMs are helping to keep sales squarely in the domestic corner, he adds. "SRAM markets are closely tied to mainframe makers, who are showing preference for American suppliers because many of the Japanese suppliers are also competing computer companies," he notes.

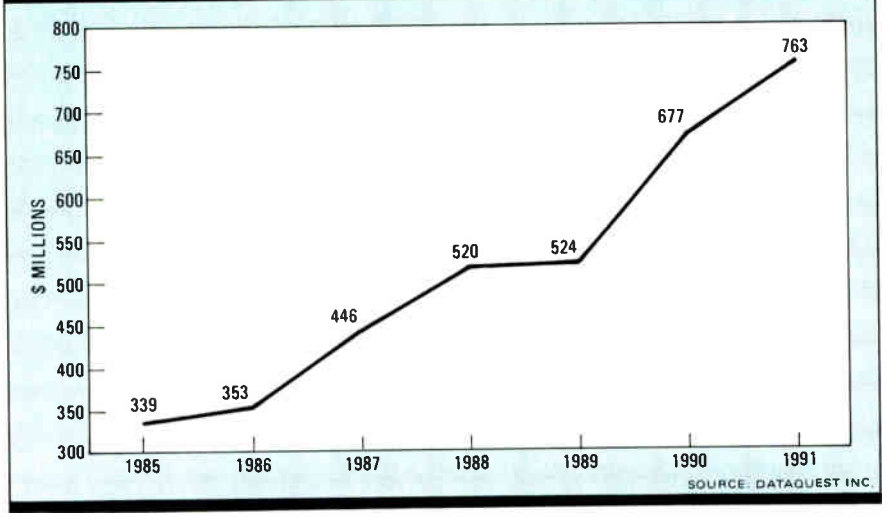
Also making the fast SRAM market more attractive these days is pricing, which has firmed somewhat. Prices have generally bobbed up 10% to 20%, partly because of the U. S.-Japan semiconductor agreement, says Tom McInerney, manager of U. S. distribution for memory products at the GE/RCA Solid State Division in Somerville, N. J.

With access times for 256-Kbit SRAMs getting down to the 25-ns level, SRAM makers are finding that all that speed is creating barriers in systems. This is particularly true for noise caused by SRAMs' fast-switching output pins. For CMOS SRAMs in conventional dual in-line packages, inductance along leads amplifies ground-bounce spikes. A pinout battle—similar to one in advanced CMOS logic markets between TI and Fairchild Semiconductor Corp.—looms, as a few suppliers suggest new standards may be needed to increase ground and power pins, with some determined to move the pins to the center of DIPs.

For example, Integrated Device Technology Inc. of Santa Clara, Calif., has given its designers the freedom of moving ground and power pins to the center on specialty SRAMs. "In areas where we don't have a Jedec [Joint Electron Device Engineering Council] standard to conform to, we will consider putting the ground pins in the center of the DIP," explains Bill Snow, manager of strategic marketing.

In San Jose, Calif., Cypress Semi-

WORLDWIDE SALES OF FAST SRAMs CLIMB



conductor Corp. has employed a double ground- and power-pin configuration in its 7-ns 1-Kbit SRAM. The 24-pin package splits the power and ground on two separate pairs of pins—one at the end of the package, the other in the center.

Design changes may deal with speed-related noises, but the speed race has also given some customers the wrong impressions about what's available, complains David Chapman, new-product definition manager at Thomson Components-Mostek Corp. The Thomson-CSF subsidiary in Carrollton, Texas, is shipping 20-ns 16-Kbit devices, and 25-ns 64-Kbit parts are slated to be shipped by year's end. Mostek managers are skeptical about claims of higher speeds. "What is news in fast SRAMs is the growing delta between what is actually available and the perception of what is out there," Chapman says. "I think the gap is bigger than it should be."

Until the noise problem is solved, fast-SRAM suppliers are bragging less about their efforts to move to sub-20-ns speeds and have begun listening to frustrated system designers who are finding it more difficult to reap the benefits as parts hit ever-higher speeds. So some suppliers of supercomputers, minisupers, and superminis have designed custom SRAMs that may be slower but are more closely tailored to applications than commodity parts are. At least a dozen static-memory merchants—including Advanced Micro Devices, Fairchild, Fujitsu, and Motorola—are hosting talks with major equipment makers in attempts to identify new self-timing or self-clocked features that will help solve the problem of system synchronization.

One company that's firmly in the synchronous SRAM camp is Motorola Inc. "Many of our fast-static customers are telling us the first thing they must do is apply external latches to the outputs. They say they must either lengthen the cycles to keep the data valid or add latches," says Bill Lane, strategic product planning manager at Motorola's MOS memory operation in Austin.

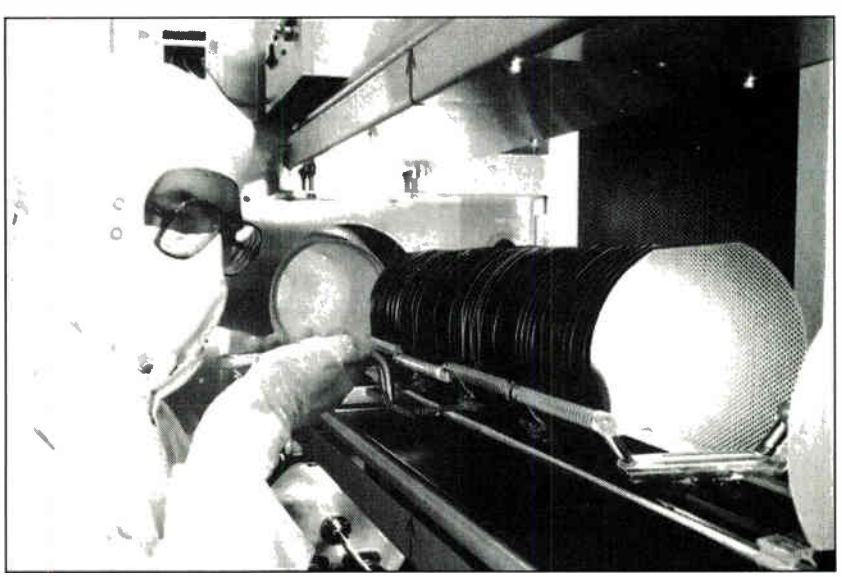
Motorola is adding latches with four new fast 64-Kbit SRAMs that have a synchronous-clocked architecture. The design employs on-chip latches, replacing the off-chip type, to deliver data available when fast central processors are ready (see p. 66). Motorola product engineers in Austin, Texas, are proposing that scheme and a double-ground pinout as a standard before the 42.3 MOS memory panel of Jedec.

At Fairchild, new 256-Kbit chips are likely to have customer-defined synchronous features. "I believe the synchronous, or self-timed or -clocked, SRAM will become a standard-bearer for high speed within the next couple of years," says Charlie Hochstedler, memory-product planning manager in Puyallup, Wash. Fairchild is readying a new 1-μm biCMOS process, using double-level metal and double polysilicon, especially for 256-Kbit chips to make them faster than existing 35-ns 64-Kbit ECL devices, Hochstedler promises.

Another company reportedly working on a synchronous SRAM is Advanced Micro Devices Inc. The Sunnyvale, Calif., company is said to be working on a 4-Kbit-by-16-bit synchronous SRAM targeted at writable control-store applications. The company is talking with potential customers about CMOS and biCMOS chips featuring self-timed input and output ports.

Some suppliers admit that the mixture of higher densities and speeds is proving more difficult to build and test than expected as transistor geometries edge below 1 μm. For example, executives at Performance Semiconductor Corp. say it faces new challenges in testing each time it pushes speeds another notch. The Sunnyvale, Calif., company says it is shipping 12-ns 64-Kbit SRAMs, and it plans to ship a 10-ns 1-Kbit-by-4-bit chip. It also has produced a 1-Kbit CMOS SRAM with 8-ns speeds. These chips, all CMOS, would go faster if noise were not a concern, says Sam Young, marketing manager. "Because of our speeds, we are pioneering testing methods, both in-house and at customer sites. Using the chips is not so much of a problem as testing high-speed parts," he says, adding that engineers have been fooled into testing harmonic ringing of test fixtures instead of the memories themselves (see photograph, below).

The noise and testing problems are solid reasons for chip makers to turn out more supercharged biCMOS statics sporting I/O signal levels compatible with superfast ECL. And they are planning more new architectures with self-timing features, pipelining glue-logic, and synchronous-clocked circuits—all tailored to superfast SRAM applications or system designs.



ON THE LINE. Performance Semiconductor uses 6-in. wafers on this fab line for its 12-ns, 64-Kbit SRAMs. The company finds testing the parts more difficult than using them.

Another fly in the ointment for chip makers is shortages in fine-line CMOS capacity, caused by revived sales of advanced CMOS logic products. Such shortages have delayed shipments of planned 25-ns 256-Kbit SRAMs from Cypress, Motorola, and Vitelic. These production woes are making life difficult in a business that has seen several contenders—notably Harris Corp. and GE/RCA—crowd onto the fast track a year ago [*Electronics*, Aug. 7, 1986, p. 121], only to drop by the wayside.

'What is news in fast SRAMs is the growing delta between what's available and the perception of what's out there; the gap is bigger than it should be'

For example, Harris' Semiconductor Sector is forgoing the speed race, leaving its military-class 64-Kbit SRAMs at 150 ns. Harris is instead concentrating on low power dissipation and radiation tolerance for its six-transistor-cell SRAMs.

GE/RCA acquires its SRAMs from a Japanese foundry, packages them, and resells parts in the U. S. A year ago, RCA had planned to offer a 55-ns static, but it decided to stay in the 100-to-150-ns range because its customers are more interested in density than speed.

At all speed levels, "there is clearly no shortage of products in the world of static SRAMs, nor is there a shortage of static RAM suppliers," says Alan Ankerband, marketing manager for MOS memories at National Semiconductor Corp. in Santa Clara, Calif. "Our last count had something like 35 companies competing in the entire market." National had hoped to be in the running for fast 8-Kbit-by-8-bit and 32-Kbit-by-8-bit SRAMs, but reports production difficulties at its Japanese foundry [*Electronics*, July 9, 1987, p. 22]. National still hopes to sell 45- and 55-ns 64-Kbit and 256-Kbit parts, and it is zeroing in on 25-ns SRAMs.

Like National and GE/RCA, a growing number of U. S. vendors are selling repackaged Japanese parts. The Japanese—including the likes of Fujitsu, Hitachi, NEC, and Toshiba—are still regarded as the pacemakers in SRAM markets ranging from consumer products to the highest-performance computers.

Fujitsu Ltd. says it is planning to introduce next year a 1-Mbit SRAM—using a cell made of four transistors and two poly-load resistors. The chip, like other four-transistor-cell designs, mixes CMOS and n-channel technology. It will have 35-ns access times and an active power dissipation of 660 mW.

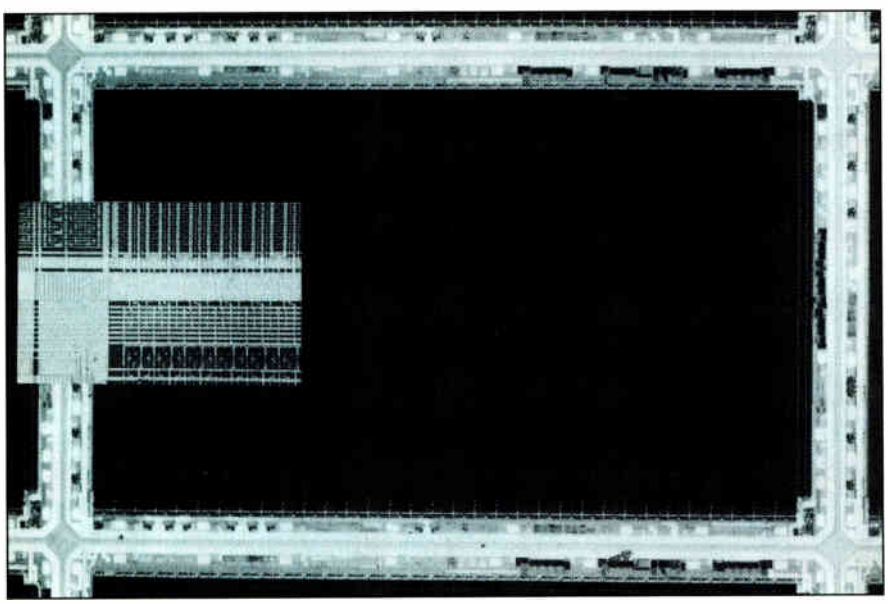
Hitachi Ltd. continues its aggressive push in BiCMOS statics, recently introducing a 16-Kbit emitter-coupled-logic-compatible part with 10-ns access times [*Electronics*, June 25, 1987, p. 25]. Hitachi is working on 256-Kbit BiCMOS statics as fast as 15 ns.

The Japanese are being challenged by Philips of the Netherlands, which says it has working samples of a 25-ns 1-Mbit CMOS SRAM made with a six-transistor cell on a 90-mm die (see photograph, below). The 0.7-μm CMOS chip [*Electronics*, July 9, 1987, p. 51] is expected to enter volume production within the next two years.

In fact, the established players are finding that the growing SRAM market has attracted new competitors in both the 256-Kbit and 64-Kbit market. Giant Texas Instruments Inc. is ready to enter military markets with a 256-Kbit CMOS design. The Dallas firm will eventually use a new local-interconnection scheme to reduce the size of a 35-ns 256-Kbit die (see p. 63).

And semicustom-chip maker VLSI Technology Inc. is preparing to introduce a 25-ns CMOS 64-Kbit SRAM with a novel design technique that allows it to use a 1.5-μm process, says Louis Williams, memory marketing manager. Late last year, VLSI Technology acquired SRAM-startup Visic of San Jose, Calif., in its efforts to jump into the high-speed chase.

One reason SRAM makers are pushing development of faster and denser parts is that fast 32-bit microprocessors are starting to set the stage for new sales, says Don Carrigan, director of memory marketing at Inmos Corp. in Colorado Springs, Colo. Inmos is offering samples of a new 256-Kbit part that has dipped below 20 ns using a current-sensing scheme [*Electronics*, April 16, 1987, p. 34]. □



FAST AND DENSE. The 1-Mbit static RAM from Philips accesses in 25 ns and uses feature sizes as small as 0.7 μm. The inset details the coarse (periphery) and fine (memory) features.

TI FINDS A NEW WAY TO SHRINK SRAM CELLS

It can save up to 25% of the chip area by replacing buried contacts with a self-aligning local interconnection scheme that uses straps made of titanium nitride

by J. Robert Lineback

A little titanium nitride goes a long way in clearing a key hurdle that faces chip makers as they attempt to shrink the cell size of fast static random-access memories and quadruple their bit count. Memory-technology researchers at Texas Instruments Inc. in Dallas have produced what they believe is the industry's smallest six-transistor SRAM cell, only 104 μm^2. They did it by introducing a tiny, scalable TiN strap that cross-connects polysilicon gates and the n+ and p+ junctions of six-transistor storage cells in CMOS SRAMs.

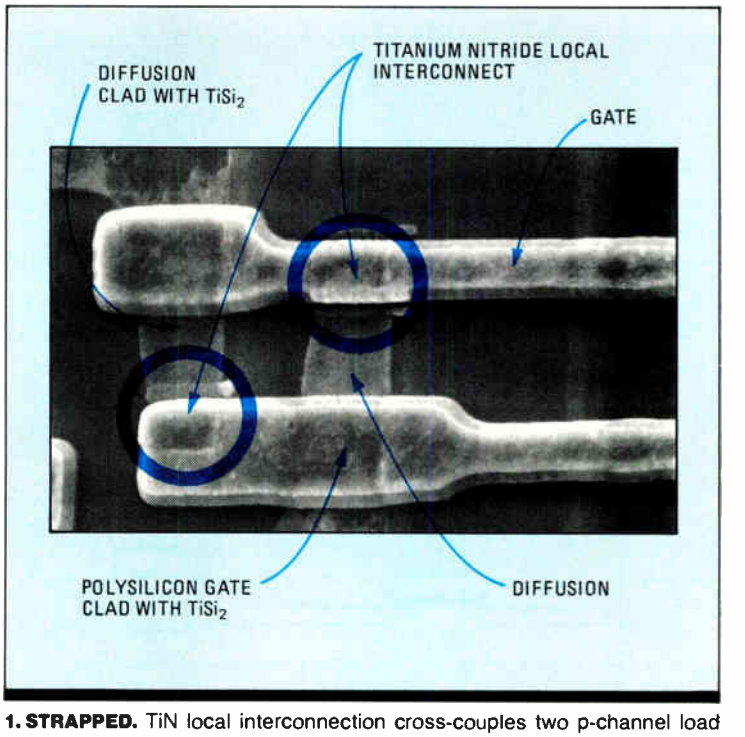
This novel self-aligning local interconnection scheme can save up to 25% of the chip area, because the size of the transistor drains can be reduced. The drains can be smaller because they don't have to accommodate the relatively large buried contacts traditionally used for cross-coupling in fast SRAM products. Also, reductions in source-drain junction areas lowered parasitic capacitance. As a result, TI's SRAM designers say they were able to boost device speed by 15% compared with memories with full buried contacts.

The new local interconnection scheme promises to keep the path open for higher-density, fast six-transistor SRAMs that are more closely aligned with standard-logic processing than are cells with four transistors and two poly-load resistors, notes Roger A. Haken, a TI Fellow who in 1984 first identified the potential of forming TiN local interconnections. "If you start going to a four-transistor poly-load process for smaller SRAM cells, the path will lead to a highly specialized resistor process technology," says Haken, who is also manager of submicron CMOS technology development in the Semiconductor Process and Design Center in Dallas. "This [strap interconnection] is an enabling technology in high-density logic where you can avoid using critical metal layers for cross-coupling the cells in on-chip SRAM." And that means the new interconnection scheme will benefit memory-intensive logic ICs of the future, he adds.

The six-transistor cell is also preferred by military markets as a higher-performance, lower-power SRAM with higher immunity to single-event upsets because of soft errors and radiation, he adds. The TiN local connection will likely be used for the first time in a 35-ns 256-Kbit SRAM, to be introduced in military markets in 1988 (see p. 65). Eventually, the interconnection mechanism may be used in TI's planned 0.8-μm biCMOS Epic IIB technology for a 256-Kbit SRAM with targeted 6-ns access speeds and 1-W power dissipation. And the technique may eventually be applied to save space in high-density logic.

The TiN local interconnection in TI's Epic 1-μm (drawn gate length) full-CMOS technology, its most advanced production process, uses the highly conductive refractory nitride layer usually stripped off dice and discarded as unwanted process trash. The new local-connection technique patterns and etches straps using the 1,000-Å layer of TiN, which forms as a byproduct of Epic's self-aligned titanium disilicide process (see fig. 1).

The TiN straps replace the conventional buried



1. STRAPPED. TiN local interconnection cross-couples two p-channel load transistors, and TiN straps connect the poly gates to junctions.

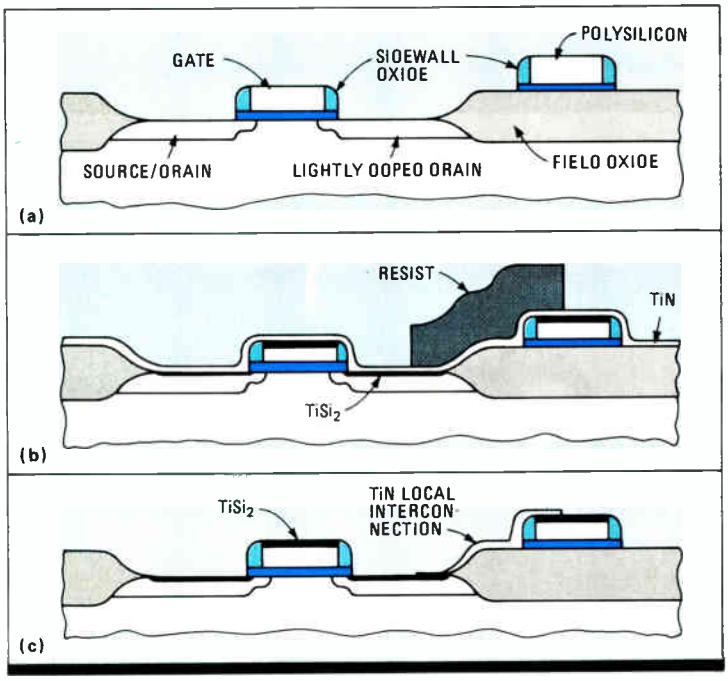
contacts, which once helped SRAM makers save die area in memory arrays as their photolithography capability extended minimum line widths to below 2 μm. Today, however, buried contacts themselves present a major barrier, because they can't be easily scaled when other circuit features are reduced to less than 1 μm, says Haken. The key problem with smaller buried contact regions is that junction capacitance rises, and higher doping levels are needed.

"In some respects we are performing the buried-contact function on top of the substrate. The result is a tremendous improvement in packing density," says Haken. At the Center, the TiN local-interconnection technique is now being readied for second-generation Epic II, which will also have 0.8-μm design rules, a bipolar module, and a triple-level-metal option.

TI started looking for a buried-contact replacement in early 1983, Haken says. "We looked at a similar approach using titanium silicide straps, but the boron of the phosphorus junctions diffuses very rapidly through the $TiSi_2$ straps whenever you have any high-temperature process." In this approach, the phosphorus outdiffusion at the gate can counter-dope p+ junctions, resulting in a diode, as opposed to an ohmic, contact, he adds.

TI developed the $TiSi_2$ technology in the early 1980s to achieve a needed low sheet resistance of 1 Ω/sq for gates and junctions in high-density memory and logic integrated circuits. "We knew we ended up with a material—which we disposed of—and if left on, it shorted out everything on the die. Actually, it took us some time to determine it was TiN," Haken recalls.

Producing TiN local interconnections requires no extra deposition or etch steps in wafer fabrication, Haken notes. Before the TiN byproduct is stripped off the $TiSi_2$ process, a photoresist mask is used to pattern the local interconnection. "What we needed to develop was a different etch step, and that is where the trick was: how we utilize this layer without upsetting the others, like the $TiSi_2$," Haken says.



2. PROCESS. TiN local-interconnection process goes from poly-gate formation (a), to deposition and patterning (b), to dry-wet etching and annealing (c).

WET AND DRY ETCH

The TiN technology uses a dry and wet etch combination to form the cross-coupling strap (see fig. 2). Fluorine is the base of the dry portion of the etch, and the liquid part is a mixture of NH_4OH, H_2O_2, and water.

"The layer of TiN is very thin, only 1,000 Å, so it does not introduce the topology difficulties that a normal layer of metal would," Haken says. The TiN layer is a diffusion barrier, stopping phosphorus from leaving the polysilicon material and counterdoping the p+ junctions of transistors. Junctions in transistors can also be extended out over isolation oxide areas. This reduces the junction area and trims parasitic capacitance. For example, junction capacitance was reduced 50% in CMOS inverter chains, which demonstrated reductions in propagation gate delays of 20% to 25%. The TiN local connection also features self-aligned junction contacts. The local-connect process has a clean-up process compatible with MOS fabrication, and researchers believe it can replace barrier metal to prevent unwanted junction spiking.

In addition to performing the cross-coupling function in six-transistor storage cells, the TiN local-connect strap also promises to be applicable to poly-load-resistor four-transistor SRAMs. It also could serve as a patterned interconnection option for logic-chip designers who can use a material with a medium sheet resistance as an alternative to more complex multiple-level-metal technologies. TiN connections have a resistance of about 14 Ω/sq, compared with 20 Ω/sq for most polysilicon.

To demonstrate the TiN local interconnection, researchers have produced a prototype representing the 114 Kbits of pseudo-static RAM contained on TI's Lisp processor chip and a standalone full CMOS-six-transistor-cell 16-Kbit SRAM. Using 1-μm design rules, six-transistor cells measured 130 μm^2, compared with 160 μm^2 using buried contacts, Haken says. With 1-μm CMOS, TI engineers believe a military-grade six-transistor-cell SRAM of 256 Kbits can be produced on an 85,000-mil^2 die.

On a new process-grading test chip, the lab has produced what researchers believe is the industry's smallest six-transistor SRAM cell, measuring 104-μm^2 using 0.8-μm Epic II, compared with a previously reported 109-μm^2 cells in an experimental 256-Kbit SRAM at IBM Corp. that used more aggressive 0.7-μm CMOS. □

For more information, circle 482 on the reader service card.

TI AIMS ONLY AT MILITARY WITH SRAM LINE

What is America's staunchest proponent of dynamic RAM-process drivers doing in static random-access memories? Plenty of research, development, and designs. But for now, DRAM-driven Texas Instruments Inc. wants only military duties for its soon-to-be-announced line of fast CMOS static RAMs.

What has caught TI's attention is a military memory market needing six-transistor cell designs for reliable, fast SRAMs. Most commercial fast-SRAM suppliers are using four-transistor cell designs with two-poly-load resistors which yield smaller dice for the price-competitive commercial markets. Six-transistor-cell SRAMs are believed to be more reliable because they are less susceptible to single-event upsets and soft errors. TI aims to use a number of new processing technologies to narrow the die-size gap between four- and six-transistor chips.

The Dallas company's initial goal is to march into military markets and establish a secure foothold in the 25-ns, 16-Kbit markets by using a standard six-transistor-cell design fabricated with its current 1.2-μm Epic I technology. In August, it will introduce a 4-Kbit-by-4-bit SMJ64C16 and a 16-Kbit-by-1-bit SMJ61CD16 in 20-pin ceramic dual in-line packages and surface-mountable chip carriers. A scaled version of Epic I, called IA, will be used later this year to introduce military 64-Kbit SRAMs with 30-ns speeds.

In early 1988, the new titanium nitride local interconnection technique will be used in 35-ns 256-Kbit full-CMOS SRAMs to reduce die area of six-transistor cell arrays using the 0.8-μm micrometer Epic II. (see p. 63).

"The commercial business is heavily populated and simply does not offer the opportunities we would require," says Jim Watson, vice president and U. S. strategic marketing manager of the Semiconductor Group in Dallas. "The military market is not as crowded and therefore offers many opportunities. There is always the possibility of a change, but I don't see anything today that would point us in that direction."

Industry estimates place the 1988 market for military CMOS SRAMs at about $70 million, compared with $45 million in 1986 and a projected $54 million this year. TI believes digital-signal-processing applications will be a key consumer of many fast military SRAMs (see chart).

TI hopes to cash in on that expanding market. Since the late 1970s, the company's Central Research Laboratory and its Semiconductor Process and Design Center have pushed ahead with SRAM developments. Few have made it to the market—military or commercial—because the company dropped several 16- and 64-Kbit SRAM designs in favor of an all-out push in 256-Kbit and 1-Mbit DRAMs. One ongoing project using SRAMs is aimed at pushing radiation-hardened silicon-on-insulator processes closer to TI's product-fabrication lines [*Electronics Week*, Oct. 1, 1984, p. 11].

Another research effort, using 1-Kbit SRAM design, has produced working memories in a mixture of silicon atop gallium arsenide [*Electronics*, Sept. 16, 1986, p. 31]. TI has seen working 1-Kbit GaAs SRAM prototypes as part of an entry into emerging digital GaAs markets.

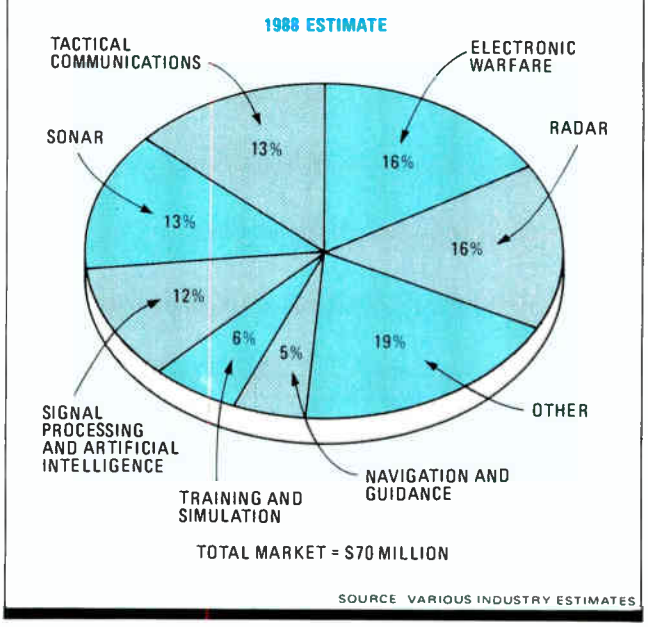
One 1980s development project has resulted in a radiation-hardened 72-Kbit SRAM made with 1.25-μm n-MOS developed under Phase 1 of the Defense Department's Very High-Speed Integrated Circuits program. The 8-Kbit-by-9-bit SLC2189 costs $225 each. TI saw the end of the density line for n-MOS with this product and then swung its process efforts behind CMOS.

TI's Semiconductor Group remains resolutely focused on using commodity DRAMs as its principle technology vehicle for next-generation chip processes and learning-curve cost reductions. But TI's latest SRAM work is likely to become a key supplemental technology driver for future mixtures of biCMOS technologies.

A speedy experimental biCMOS 256-Kbit SRAM is now in development at TI, and targets are set on 6-ns access times with 1-W power dissipation. Hitachi of Japan has produced a commercially oriented 64-Kbit biCMOS SRAM with 7-ns speeds and less than a 0.5-W power dissipation, say TI researchers, who are aiming to leapfrog competitors in the mixing of the two technologies.

TI's next-generation biCMOS will be realized by adding a bipolar-process module to a future 0.8-μm CMOS technology, known as Epic II. The 0.8-μm biCMOS blend will be called Epic IIB, adding only three or four extra mask steps to the Epic II CMOS core process. *–J.R.L.*

WHERE MILITARY SRAMs ARE GOING



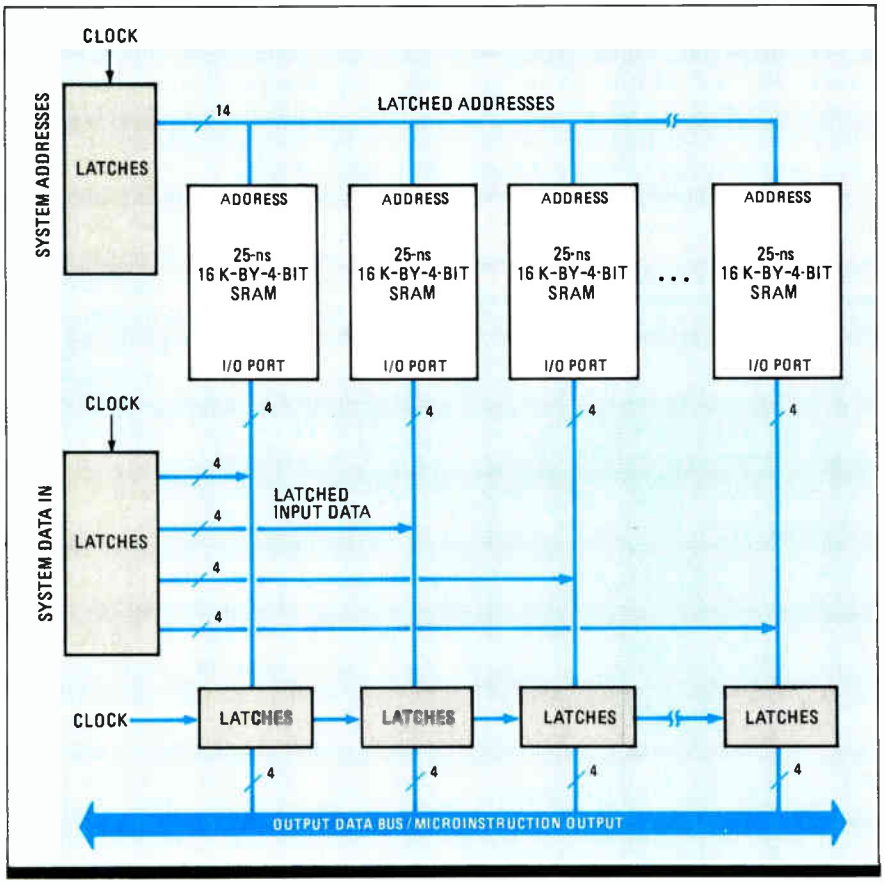
MOTOROLA'S RADICAL SRAM DESIGN SPEEDS SYSTEMS 40%

Key to higher throughput is a synchronous clocked architecture and on-chip I/O latches; the combination cuts interconnection delay by up to 20 ns

by Bernard C. Cole

Engineers at Motorola Inc.'s MOS Memory Products Division are taking a radically different approach from the current asynchronous architecture for static random-access memories. They are developing a synchronous architecture the company claims will improve system throughput by as much as 40% and will reduce system component count by as much as 50%.

The keys to the Austin, Texas, division's new architecture are: replacing the traditional self-clocked address-transition-detection circuitry, found in conventional asynchronous SRAMs, with a synchronous clocked architecture, and adding critical input and output latches on-chip. The combination of these features eliminates as much as 8 to 10 ns of interconnection delay on input and on output, says William Martino, the division's design manager for specialized memories. It also eliminates circuitry often required to make asynchronous devices appear synchronous in high-performance cache-memory systems, which depend heavily on the synchronization of critical timing parameters. Also incorporated on the chip are drive transistors capable of driving buses with capacitive loads of up to 130 pF without additional external circuitry. Motorola designers also enlarged the geometries to increase the inherent drive capability of the devices without increasing the chip size.



1. ASYNCHRONOUS. Using asynchronous SRAMs, designers of high-performance synchronous systems must incorporate latches on the inputs and outputs, adding 15 to 20 ns of delay.

The new architecture has been incorporated into four initial products that are members of a new family of 16-Kbit-by-4-bit SRAMs with cycle times ranging from 10 to 25 ns and access times in the 15-to-35-ns range. This equals that of comparably sized asynchronous SRAMs fabricated with the same 1.5-μm single-metal CMOS process [*Electronics*, Aug. 7, 1986, p. 81], says Frank Miller, synchronous SRAM project leader at the division. But Miller emphasizes that the elimination of as much as 20 ns of interconnection delay can at least double system-level performance.

Motorola expects to offer samples of the four clocked synchronous SRAM parts within about a month and plans to be in volume production by the beginning of the fourth quarter. Two of the devices, the MCM6292 and 6295, incorporate level-sensitive transparent latches,

whereas the MCM6293 and 6294 use positive-edge-triggered latches. Also the 6293 and 6295 each have a special chip-select pin that allows the user asynchronous control of the output buffers, allowing the parts to be used in common I/O at the board level. All the devices feature an active ac power dissipation of 600 mW and an active dc power of only 100 mA.

The advantages of Motorola's new family of synchronous SRAMs outweigh the advantages of asynchronous devices, Martino says. In asynchronous devices, great reliance is placed on address-transition detection, a self-clocking scheme that uses the address-signal transition, or edge, as a reference to synchronizing all operations on the chip to that signal. Martino says that asynchronous SRAMs are widely used because they allow and recognize address changes at any time. As a result, no external global clock is necessary to access data, making them easy to use. Also, compared with dynamic RAMs, asynchronous SRAMs take much less external circuitry, says Miller. Because they are free-running, the addresses can be changed whenever needed, and they are very easy to control.

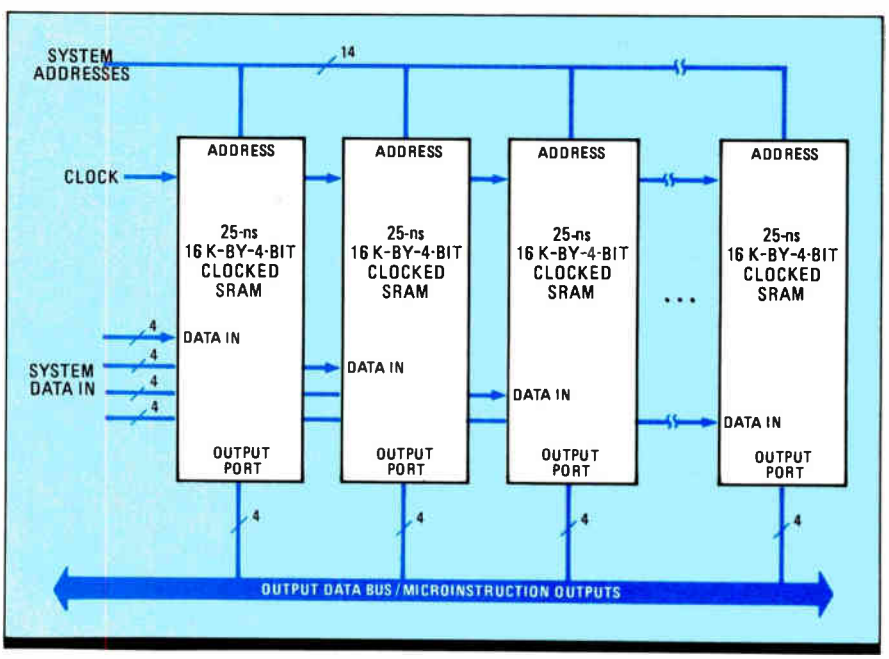
Although they are easy to use, asynchronous SRAMs must be surrounded by considerable external logic (see fig. 1) in many applications in high-performance processor systems such as writable control stores, data caches, and cache-tag memories [*Electronics*, June 11, 1987, p. 78] that require synchronous operation. The extra circuitry imposes a considerable performance penalty, and that can be a problem in cache applications in particular, says Martino, where the speed of memory typically must be at least an order of magnitude faster than main memory. Also, for a cache to work properly, critical timing relationships must be preserved so that a variety of simultaneous operations can be coordinated, such as searching the tag store, getting data out of cache, and replacing proper entries in the cache. The added delay of the external logic can make it difficult to preserve these relationships.

When system speeds were in the 200-ns range, Miller says, the additional 10-to-20-ns penalty of this external logic could be tolerated. "But with processor speeds improving so dramatically, now pushing below 100 ns toward 50 ns, this is a penalty that is critical, especially since the speed of the external logic has not kept pace with the improvements in speed at the chip level."

Depending on the type of register involved and the process used, the delay time, even with high-performance logic families, can be reduced to no more than 7 to 10 ns, says Martino. As a result, most speed improvements have come by pushing the speed of the memory chips themselves. But, as processors speed up, memories with sufficiently low access times are getting harder and harder to produce inexpensively, Martino says. Current 25-to-35-ns asynchronous SRAMs are barely adequate, he says. And newer processors will require a system throughput of no more than 35 to 40 ns. For such throughputs, SRAMs must be pushed to below 10 ns, only achievable now with bipolar and BiCMOS circuits, but at much higher power. "However, even if parts are pushed down to 1 ns and under, there is still that 10 ns on the input and another 10 ns on the output to deal with," says Martino.

The most important element in Motorola's new SRAM architecture (see fig. 2) is the incorporation of the external input and output latches necessary for synchronous operation on board. This design considerably simplifies system design and reduces interconnection delay. "By pulling all of that glue logic on board, it is no longer necessary to drive a large bus to TTL levels," says Martino. "It is now done on-chip, reducing the 10-ns delay down to picosecond levels. This allows the design of a 25-ns part for a 25-to-30-ns bus, rather than using more expensive, power-hungry 10- and 15-ns parts for the same chore."

The Motorola architecture uses address-input latches to hold the address-valid signal so that the processor does not have to hold the addresses valid for the entire cycle. A similar function is served by the data latches on the input. The latches on the output, however, serve a dual function. First, they provide a longer setup and hold time over which the data is valid on the bus, necessary in most processing systems. With a



2. SYNCHRONOUS. By incorporating latches and drivers on-chip, Motorola's synchronous SRAM reduces chip count by more than 50% and reduces interconnection delay.

standard SRAM at minimum cycle time, that time is about 5 ns without any external latching. This is not enough time for most systems, which require the data to be on the bus for at least 15 to 20 ns, for the processor to receive the valid data. The other function of the latches is to provide the extra 100 pF needed to drive the buses with capacitive loads of up to 130 pF.

The designers of the new SRAMs have eliminated the address-detection-transition circuitry; now they use on-chip clock input for a synchronous clocking scheme

Also incorporated on-chip to support the synchronous operation of the latches is a clock input that controls when the latches are transparent and when they are brought into play. Usually this clock input is a derivative of the system clock; that is, the latches are controlled by the edge of the system clock.

The Motorola designers have eliminated the address-detection-transition circuitry in the new SRAMs. Instead, they use the on-chip clock input to incorporate a synchronous clocking scheme in which the necessary address, data, chip-select, and write-enable information previously brought on board the chip by the address-detection-transition circuitry is now accessed at the beginning of the cycle in reference to the external clock, rather than to the address edge as in the asynchronous scheme. The technique, says Martino, is similar to how a DRAM brings in its addresses with setup and hold times in relation to a read-access or column-access signal input. "Since this device employs a clock with a high-going edge at the beginning of each cycle, it is no longer necessary to detect address-window transitions," he says. "The system will tell the chip when to supply the necessary information by providing the clock at the appropriate time."

To eliminate the external drive circuitry, the inherent drive capability of the devices was increased fourfold, says Miller. So Motorola designers enlarged the geometries used to fabricate the pull-up and pull-down transistors, typically on the order of 1,500 μm wide, compared with 400- to 600-μm widths on the standard 30-pF devices, and as small as 6 μm in the memory array and 80 μm in the peripheral circuitry. Moreover, to achieve higher speed in spite of the higher drive currents, n-channel devices, which are only output devices, were used rather than the slower p-channel devices. Furthermore, these output devices were speeded up by incorporating a separate ground-supply pin for the output drivers. "This allowed us to burn more current in the output drivers without corrupting the operation of the rest of the circuit," Miller says.

Although this required a substantial increase in the area devoted to the drive circuitry, the chip size, 146 by 404 mils, is not substantially larger than comparable 64-Kbit asynchronous SRAMs. The extra area required for the larger drivers and for the internal clocking circuitry is offset by the area eliminated by removal of the address-transition-detection circuitry required on asynchronous parts, Martino says. □

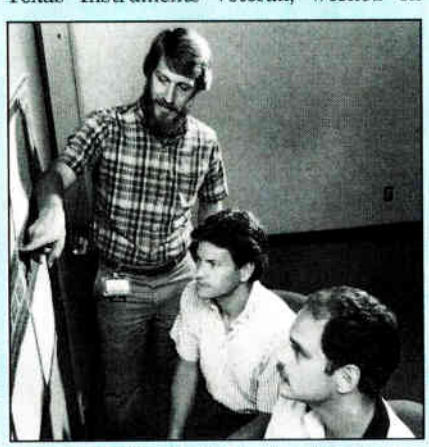
For more information, circle 483 on the reader service card.

INGENIOUS SRAM DESIGN WAS DONE IN REMARKABLY SHORT TIME

For a memory device of such complexity and ingenious design, Motorola's new clocked synchronous static random-access-memory design was completed in a remarkably short time—only 12 months. Moreover, most of the work was done by a four-person design team: William Martino, design manager for specialized memories; Frank Miller, synchronous SRAM project leader; chip designer Scott Remington; and layout engineer Richard Southerland.

One reason for the fast turnaround was that the array and much of the peripheral circuitry is identical to what was used in the company's family of asynchronous 64-Kbit SRAMs, says Miller. "All we had to do was strip off those portions of the circuit relating to the asynchronous operation and replace them with new synchronous elements."

The team drew from two sources for the features incorporated into the synchronous design—including their cumulative design experience. Miller has seven years' experience in memory design. Remington, an eight-year Motorola veteran, worked on the company's 64-Kbit and 256-Kbit asynchronous SRAMs and a 1-Mbit DRAM. Southerland, a five-year Texas Instruments veteran, worked on most of Motorola's asynchronous SRAMs in his two years with the company.



EXPERTS. Miller, Southerland, and Remington, from left, are old hands at memory design.

The other source was extensive input from Motorola's customers. "We spent several months defining a variety of special-application memory devices, from dual-port SRAMs and video DRAMs to content-addressable memories," says Miller. "But when we started taking these designs around to customers for input, we found they were most concerned with ways to make standard parts work better. For designers of high-performance systems using cache architectures, one of the largest common denominators was complaints that they had to surround the asynchronous parts with a variety of glue logic to operate appropriately in a synchronous environment.

"The key is listening to the customers, finding out what their specific complaints are, and coming up with parts that satisfy those needs."

A NEW VERSION OF AT&T's DSP WILL PEAK AT 25 MEGAFLOPS

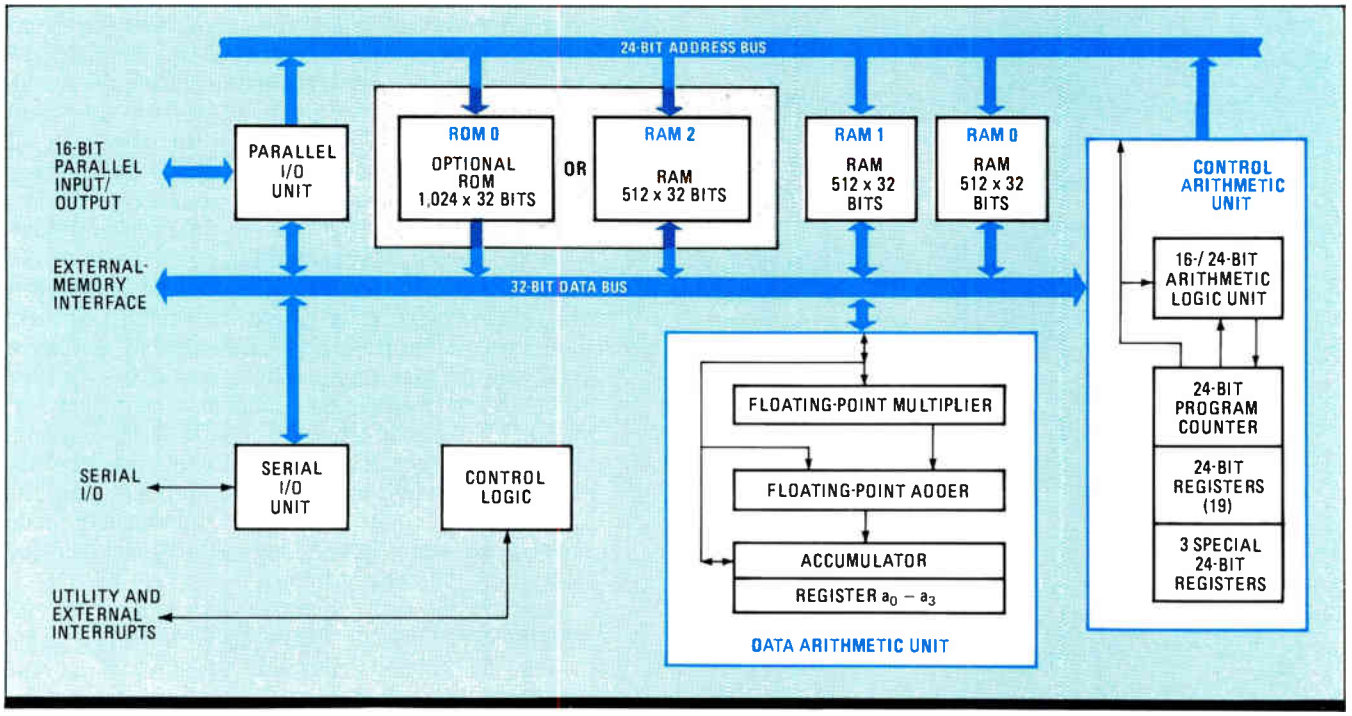
Due out early next year, the DSP32C gets its speed from a new 0.75-micron CMOS process, new single-cycle instructions, and a 32-bit bus that handles four memory accesses per cycle

by George Sideris

AT&T Co. is betting that a submicron CMOS version of its DSP32 digital signal processor will challenge microprocessors in applications such as scientific computing, graphics processing, and high-speed control systems. With throughputs as high as 25 million floating-point operations per second, the new DSP32C will outperform microprocessors and match all but the fastest board-level array processors, the company says.

One reason AT&T thinks the chip can compete in those kinds of number-crunching applications, as well as in filtering and other telecommunications signal processing, is its enormous throughput. Besides the 25-megaflops throughput, the DSP32C can execute 6.6 million Whetstone instructions/s, perform a 1,024-point complex fast-Fourier transform in 4.4 ms, and do finite-impulse-response filtering in 80 ns per tap, and adaptive filtering in 160 ns per tap. The Whetstone rating is some 4 to 18 times higher than throughputs reported for the most popular combinations of 32-bit microprocessors and math chips, and about 50% more than a 32-bit transputer with built-in floating-point unit [*Electronics*, Nov. 27, 1986, p. 51].

The DSP32C owes about half its throughput advantage to the new 0.75-μm CMOS process and half to powerful new single-cycle instructions

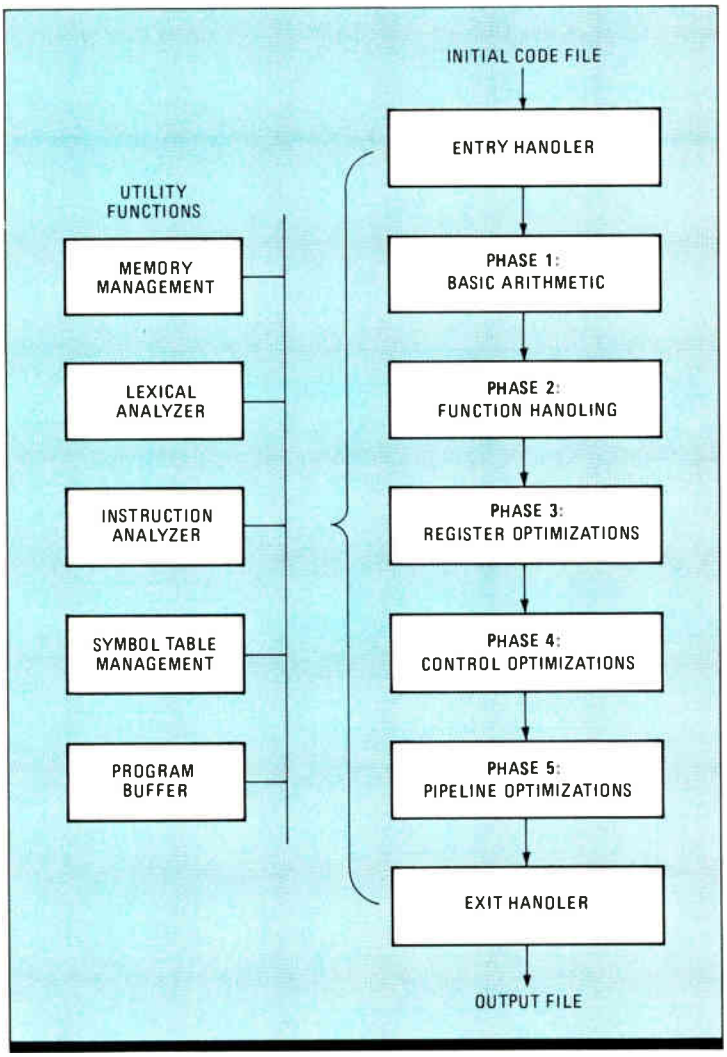


1. ARCHITECTURE. The DSP32C's single-bus architecture resembles that of a microcomputer with a built-in, floating-point arithmetic unit; its data arithmetic unit does floating-point operations, while the control arithmetic unit handles functions such as integer operations.

and a 32-bit bus that supports four memory accesses during each cycle. It can, for instance, fetch two 32-bit numbers from random-access memory, multiply and accumulate the result, and write the result into memory during one 80-ns instruction cycle.

Samples of the new chip, along with a C compiler and a development system, will be available in the second quarter of 1988. It is two to three times as fast as AT&T's DSP32 floating-point processors (see p. 54), which also have a multi-fetch architecture but are 2-μm n-MOS devices with 16-bit buses and memories. Besides a wider architecture, the DSP32C has numerous enhancements to speed programming and reduce software overhead. A new loop-control instruction, for instance, replaces the branching instructions usually needed to repeat programmed functions.

AT&T is not banking on speed alone to win sockets. Since designers accustomed to conventional microprocessors have generally shied away from DSP programming in the past, Bell Labs is also readying an optimizing compiler for programs written in the C language, with the goal of making the new chip as easy to use as a microprocessor. AT&T expects the optimizing C compiler to be the main wedge to open up mainstream computing and control applications. The compiler will take advantage of the enhancements to produce code 90% as efficient as handwritten code.



2. OPTIMIZER. After the basic compiler translates the C source program into code, a five-phase optimizer improves code efficiency.

Architecturally, the DSP32C resembles a one-chip microcomputer with a built-in 32-bit floating-point arithmetic unit (see fig. 1). This data arithmetic unit performs floating-point operations and integer and linear conversions. A control arithmetic unit handles memory addressing, data transfers, 16- and 24-bit integer operations, and other microprocessor-like functions.

The internal floating-point format—a 24-bit normalized mantissa for a number's fractional part and an 8-bit exponent for its magnitude—keeps precision independent of magnitude and provides more than 1,500 dB of dynamic range, making overflow unlikely. A 40-bit adder and a 40-bit accumulator with four registers eliminate rounding-off problems to ensure 24-bit precision and high throughput. Optional configurations will allow users to download programs and data into three 512-word random-access memory banks on the chip, or to substitute a 4-Kbyte read-only memory for the third RAM bank.

Increasing the bus width from 16 bits to 32 bits for data and 24 bits for addresses will speed floating-point operations, allow sharing of a system bus with advanced microprocessors, and boost external memory capacity to 16 Mbytes. Other major enhancements include the 24-bit arithmetic logic unit (the DSP32 has a 16-bit ALU) two external interrupts, and six interrupts to monitor I/O and floating-point operations.

As in the DSP32, the single bus helps simplify programs by allowing the programs to treat memory as a common resource. In contrast, DSP chips usually have a Harvard architecture—multiple buses access separate instruction and data memory spaces. To make up for the lack of simultaneous accesses, the DSP32C's bus makes four memory accesses in one instruction cycle.

Although the DSP32C has its own internal floating-point format, it is compatible with the standard IEEE format. On-chip hardware converts between the two formats in a single instruction. Several functions that often add considerable software overhead are also handled automatically with new hardware or instructions. For instance, post-normalization logic transparently shifts decimal points and adjusts exponents to prevent inaccurate rounding off when floating-point numbers are added or multiplied. A bit-reversed addressing mode saves time when processing algorithms call for that form of data shuffling.

Since the DSP32C operates with single-cycle instructions, additional instructions to repeat programmed operations could use up as much as half the throughput during repetitive operations. The new chip solves this problem with a loop-control instruction that sets a program counter to repeat

blocks of up to 32 instructions up to 255 times automatically. This technique can also save much of the memory space needed for in-line code expansions—that is, storing multiple copies of the same block in memory so that blocks will repeat without the usual branching instructions.

The C compiler being developed will take advantage of such enhancements and also perform the kinds of optimizations generally provided by mainframe-computer compilers. The compiler will enable programs written in C to run with nearly 90% of the efficiency of handwritten code, say Frank Ferro and Kreg Ulery, of the technical support staff at AT&T Technology Systems. Such efficiency will make compiled high-level-language programming suitable for real-time applications. The compiler currently produces code that runs on the DSP32 and is being upgraded to handle the DSP32C enhancements. Code written for the DSP32 will run on the DSP32C.

After the compiler translates a C-language source program into an initial code file, similar to code produced by an assembler, the file is processed by an optimizer subsystem (see fig. 2). Critical program segments can be rewritten in assembly language and linked into the program. Or, the designer can start with programs from AT&T's DSP32 library. The older chip lacks many of the DSP32C's functions and instructions, so the object code needs optimization to run efficiently on the new chip. The optimizer does that in five phases, aided by the compiler system's utilities.

After generating code for arithmetic functions not available on the DSP32, the optimizer changes function handling, register, control, and pipeline operations to suit the new design. For instance, the control-loop instruction is not necessarily the best way of repeating functions—in-line expansion can actually shrink a C program if most functions are used only once. During its function-handling phase, the compiler takes that into account when deciding whether to expand functions.

To optimize register usage, the compiler identifies often-used arguments and variables and moves them from main memory to registers to save access time. Also, it cuts parameter-passing overhead by, for instance, utilizing registers instead of a memory stack for parameters accessed through function calls, or by putting parameters directly into functions for use when the code segments are reached.

The large set of general-purpose registers gives the compiler more room to maneuver than typical dedicated DSP registers would provide. To make the most of them, the compiler employs a technique known as register overloading—to handle variables active at different times during program execution without save and restore operations, it can use one register to store more than one variable.

The new chip and compiler are being developed by AT&T Bell Laboratories. The submicron CMOS process is being developed jointly by Bell Labs and AT&T Technology Systems, Allentown, Pa., which will produce and support the chip. Chip samples, along with the compiler and a development system, will be available in the second quarter of 1988; volume deliveries should start four to six weeks later. Two versions will be offered, one with 80-ns instruction cycles and the other with 100-ns cycles. High-volume prices for the 100-ns version will be around $50; other prices have not been set.

The C compiler will do the same kind of optimization as mainframe compilers—programs written in C should be 90% as efficient as handwritten code

A software package with an assembler, linkage editor, and simulator will be available by the end of this year. One version runs on AT&T's Unix System 5 operating system and costs $1,500; another runs on personal computers with Microsoft Corp.'s MS-DOS system and costs $500. □

For more information, circle 484 on the reader service card.

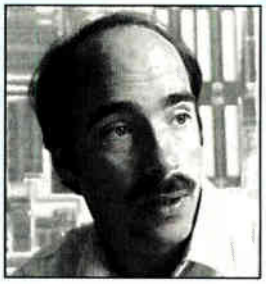
SECOND-GENERATION CMOS OPENS NEW DOORS

Chip designers who have not yet worked with submicron CMOS have a treat coming to them, says Michael Fuccio, 29, the lead designer of AT&T Co.'s DSP32C digital signal processor, a successor to the DSP32. Direct comparisons between the first and second generations of the device demonstrate the new technology's power to improve designs, says Fuccio, a staff member at the AT&T Bell Laboratories facility in Holmdel, N.J.

The DSP32, developed with 2-μm n-MOS in 1984, is still a formidable design, and Fuccio notes it's improving with age. Planned scaling-down will boost its clock rate from 16 MHz to 25 MHz and raise peak throughput to some 12 million floating-point operations per second.

But with n-MOS, just squeezing a floating-point DSP onto a single chip was a notable achievement. In contrast, the higher-density, lower-power CMOS technology gave the design team leeway to go beyond essential functions. Instead of simply moving up to 50 MHz—the new clock rate—the team attacked ease-of-use issues that have limited DSP applications. "We got the feedback from customers, we found out what new features they needed, and we put them in," Fuccio says.

The team wound up with a baker's dozen of major enhancements. The new bus structure, for example, is not only wider for higher throughput but also is designed to work with other devices in shared-bus systems and is supplemented with a memory interface that accommodates a variety of main memories.



MICHAEL FUCCIO

Fuccio joined Bell Labs in 1980 with a BEEE (Bachelor of engineering, EE) from the University of New York at Stonybrook, Long Island. He got his MSEE at Georgia Institute of Technology under the labs' graduate education program and is now working toward his doctorate at Rutgers University, N.J.

CAN ASICS DRIVE AT&T'S CHIP BUSINESS?

AT&T Co. set out to conquer the semiconductor market four years ago with an arsenal of commodity memory products. By every account, the strategy failed. The phone company's chips were greeted skeptically, well-entrenched Japanese suppliers held their ground, and within two years, AT&T had changed its focus to niche markets.

Now old Ma Bell is revamping its efforts again. With a new management team at the helm and a new charter in its grasp, AT&T's Components and Electronic Systems Division in Berkeley Heights, N.J., is setting its sights on the burgeoning market for application-specific integrated circuits.

The division's new strategy is based on two premises. The first is that whether or not AT&T sells chips on the outside, it must produce them for internal use in order to be competitive in its equipment markets. Second, AT&T has unique design, development, and manufacturing capabilities that are valuable commodities in their own right. The idea now is to market those talents to the growing number of companies that are abandoning standard ICs in favor of semicustom designs—designs that offer higher functionality and that can help differentiate a product from its competition.

AT&T, though, has a long way to go. Last year, only 17% of the component division's $1 billion in sales went to external customers. And even though half of the division's total business is semiconductors, chips represented only about 5% of its 1986 sales. The division's other products include power supplies, connectors, printed-circuit boards, and other components.

The division's goal is to grow the entire business "dramatically," paying special attention to semiconductors, says William J. Warwick, the new division president. He expects to double chip production overall by 1995, with about two thirds of that growth coming from outside sales, particularly ASICs. ASICs currently account for about 30% to 40% of AT&T's MOS chip business, a figure the company hopes will grow to at least 50% by 1990. AT&T is betting that total chip sales will reach about $400 million by 1995.

To reach those goals, Warwick has left no stone unturned. He has streamlined the marketing operation and imposed a new Japanese-style business philosophy. Internal sales no longer must generate a profit; it is enough if they just generate technology. "We were not optimizing the value of vertical integration," he explains. "We're trying to bring that back."

CUSTOM MADE. AT&T is trying to leverage its ASIC technology in the merchant chip market.

The key to attacking the competitive ASIC market will be AT&T's ability to cultivate more relationships like the one it now enjoys with Hughes Aircraft Co. of El Segundo, Calif. AT&T has completed three designs for Hughes in three years, and a fourth is in progress, says ASIC product manager A. Edward Walker. "We have a half-dozen" similar arrangements, he adds, including an unnamed European partner for whom AT&T has produced 15 designs. These long-term deals are being used to complement sales of the division's standard products, such as digital signal processors, microprocessors, and other linear and digital devices.

Warwick says it takes high-level executive sales to negotiate ASIC deals, especially with a buying public that has its doubts about AT&T. "You don't [get a long-term deal] by sending the marketing guy to the purchasing agent," he says. "The fundamental thrust is at the top of the corporation."

AT&T's ASIC line is built around digital standard cells in 1.25-μm CMOS technology but also includes bipolar digital gate arrays and full-custom capabilities for digital and linear chips built in either bipolar or CMOS technology. The division expects to unveil its 0.9-μm cell library in less than a year.

Bill McLean, of market researcher Integrated Circuit Engineering, Scottsdale, Ariz., praises AT&T's ASIC capability—even as he wonders about the company's resolve to compete nose-to-nose with market leaders like NCR Corp. He notes that AT&T has five plants on three continents, plus design centers in the U.S., Europe, and the Far East—all the tools to be a strong competitor, except sales expertise and a presence in the marketplace. He gives AT&T "a 50-50 chance of staying in the market."

The perception that AT&T is not committed to its outside semiconductor business won't go away overnight—and it will hamper Warwick's efforts to sign the long-term contracts he yearns for. But he says he has no intention of dropping out, and he's got a 29-year track record that bears him out (see p. 12).

"People viewed AT&T as a startup [chip seller]," recalls Thomas V. Gates, a product marketing manager for MOS Communications Devices at AT&T. "And a lot of startups die in the first two years. We've been here almost four—I think we've gotten over the 'sudden infant death syndrome,' and I think customers are starting to recognize that." *–Tobias Naegele*

UPDATE: ZORAN MOVES UP WITH IMAGE COMPRESSOR

Following up on the initial success of last year's vector signal processors and digital filter processors [*Electronics*, July 24, 1986, p. 59], Zoran Corp. is now poised to introduce a powerful new image-compression processor designed to reproduce high-quality images 10 times faster than any digital signal processor available.

Last year's products combined vector-handling techniques with application-specific algorithms, enabling them to execute complex signal processing functions from only a few high-level instructions. Like the earlier products, the new ICP incorporates a proprietary algorithm that allows progressive reconstruction of images. It relays data step by step—initially sending only a fraction of the information needed to form a recognizable image and eventually sending the information needed to complete the image.

The ICP will fit into a broad range of new and existing image processing appplications, says Mike Stauffer, marketing director at Zoran. "It provides designers with high levels of rapid image processing in a single device." Priced at $99 in OEM quantities, the ICP's capabilities will be applied to such areas as electronic publishing, video conferencing, military satellite reconnaissance, broadcast-quality still-frame compression, and in electronic cameras and compact-disk read-only memories, says Stauffer. The ICP, says Stauffer, provides a much needed solution for the user faced with limited storage space or speed, since it can significantly reduce both the required disk space and transmission bandwidth. It also speeds up viewing time: instead of waiting for a complete line-by-line reconstruction, the user can quickly obtain a general outline of the image, allowing him to sort through a large group of images quickly.

Zoran's designs are already appearing: three DFP products went into production in September of 1986, followed in December by the more complex and sophisticated VSP. A fourth DFP is scheduled for introduction within a month. Prototypes of the ICP are available immediately, with production quantities available at the beginning of the fourth quarter of 1987. *–Bernard C. Cole*

UPDATE: TRW'S SUPERCHIP PROJECT FORGES AHEAD

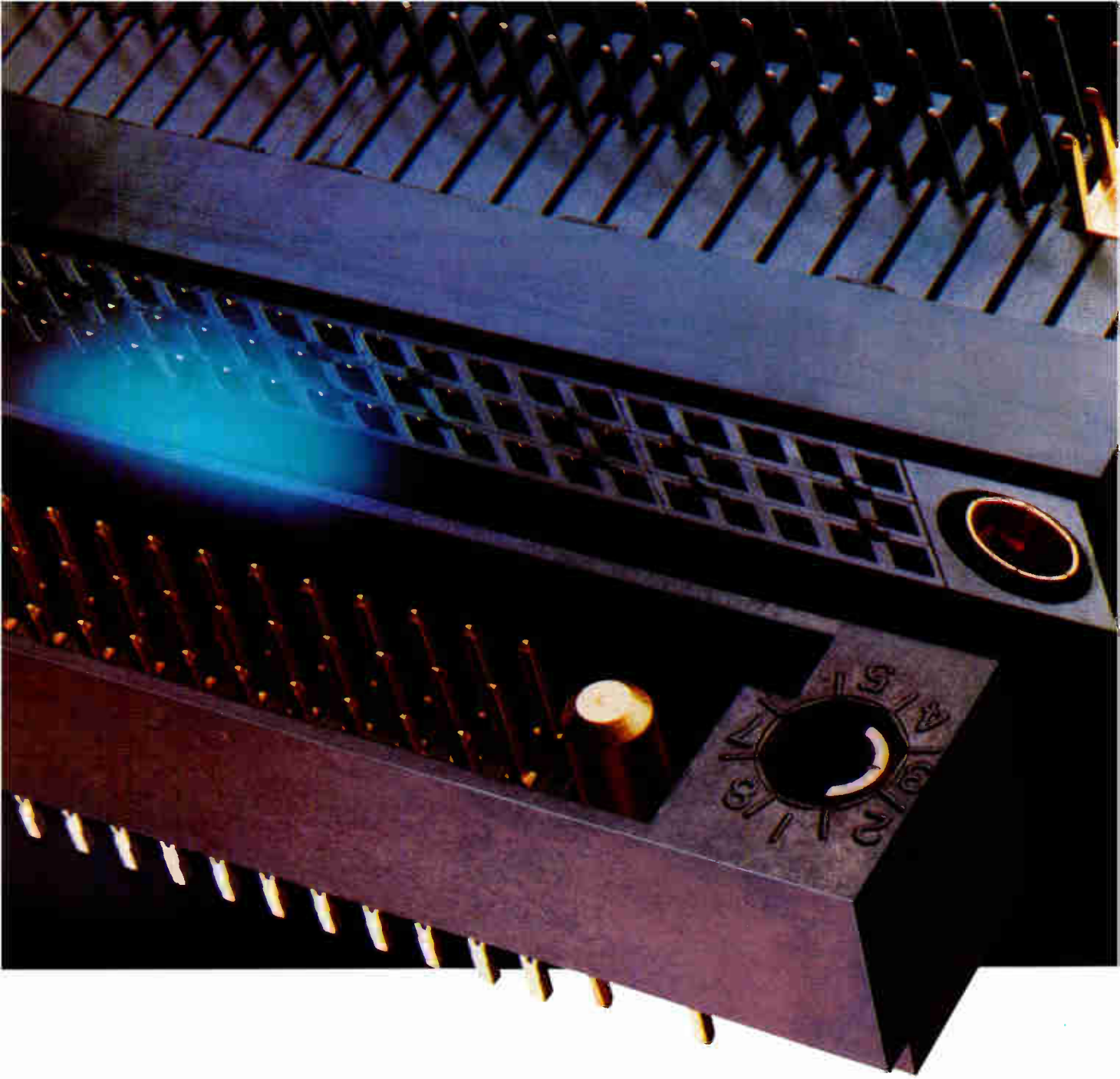
Enthusiasm at TRW Inc. continues to build as the company's ambitious superchip project [*Electronics*, July 10, 1986, p. 49], ticks off scheduled goals. After a year of work on the technology, says Thomas A. Zimmerman, director of Very High-Speed Integrated Circuits programs at the firm's Electronic Systems Group, "we haven't found any big holes or barriers."

TRW last year disclosed details of its new superchips, noteworthy for their size—as small as 1.4 by 1.4 inches—and densities as high as 18.8 million active devices. The most eye-catching aspect of the design, however, is its self-diagnostic capability. Incorporating newly developed built-in testing and automatic-software-configuration concepts, the chip essentially heals itself by identifying and bypassing its faults. This more reliable superchip, with 0.5-μm feature sizes, will be built according to specifications for Phase 2 of the Defense Department's Very High Speed Integrated Circuits program.

Developers have been moving steadily ahead from simulation to fabrication of working parts. TRW and its VHSIC Phase 2 partner, Motorola Inc., have designed and verified the first two macrocells. These are being tested now, before being fabricated at the 0.50-μm CMOS facility of Motorola's Semiconductor Products Sector in Phoenix.

The companies plan to have four macrocells ready for fabrication by August of 1987, and design of all 29 cells completed and in some stage of production by the year's end. The macrocells, along with the 2-Mbit static RAM, will be contained in the key signal processor chip. Zimmerman notes that the convolver correlator, the only bipolar device proposed for the superchip family, has been shelved by the VHSIC program office: a survey of potential military users indicated little interest in anything other than CMOS.

Commercial applications of the superchip are becoming apparent. The button-board multilayer interconnection for connecting the devices, in which randomly crumpled wads of wire form the contacts, is attracting interest from equipment companies. TRW predicts the button board may " soon be a big winner." *–Larry Waller*



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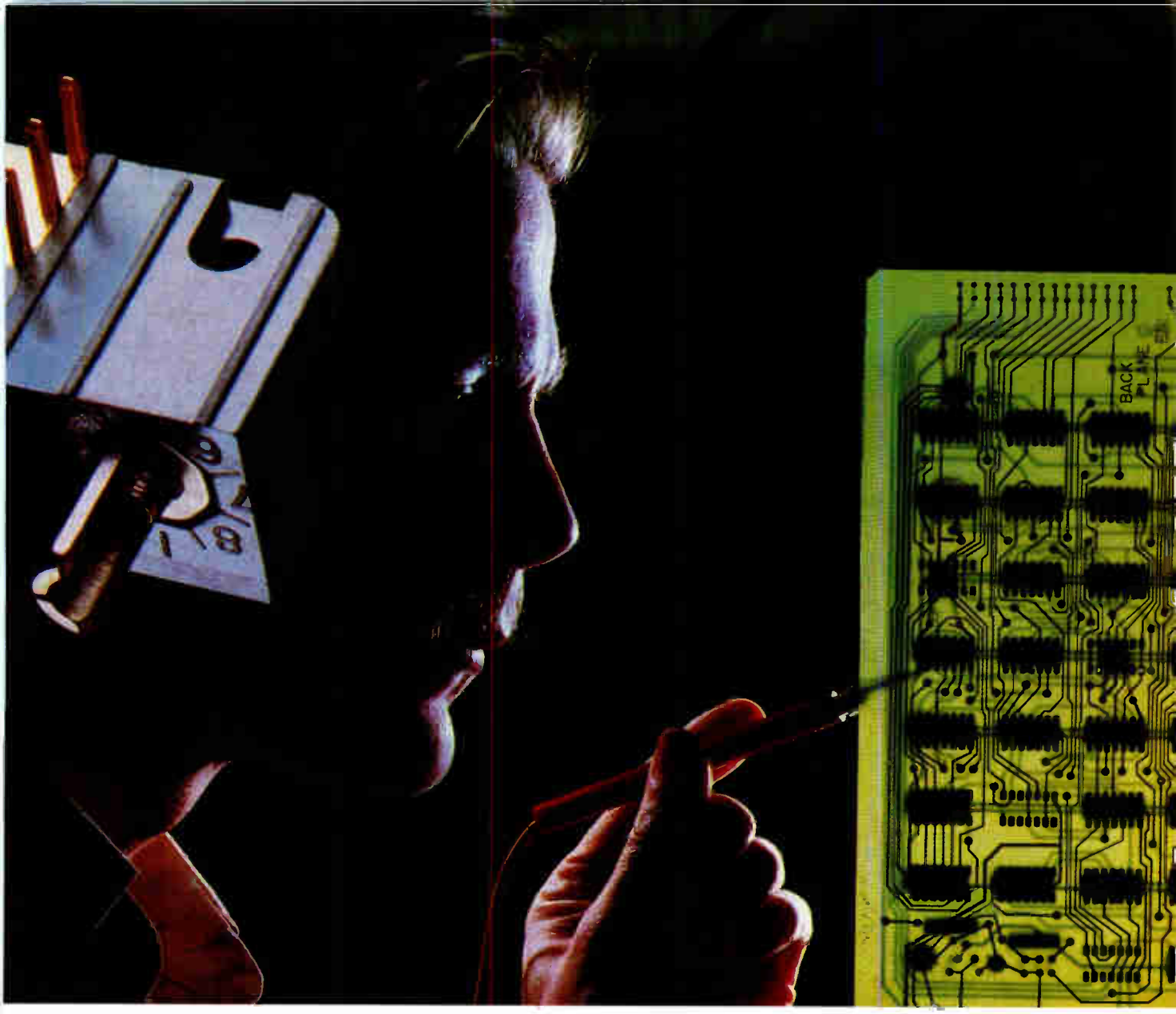

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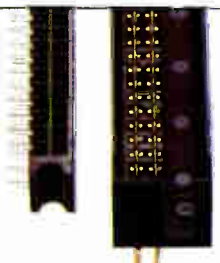

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MILITARY/AEROSPACE NEWSLETTER

PENTAGON TO FUND STUDY FOR REDESIGNING OBSOLETE COMPONENTS

A request for proposals to redesign obsolete components, mainly discontinued gate arrays, is expected in the second phase of a Pentagon program to ensure that the military has a continuing supply of outdated electronic devices. The request should come by the end of September, as the next step in the Microcircuit Emulation Program of the Defense Electronics Supply Center in Dayton, Ohio. In the program's first phase, the DESC awarded a $2.9 million contract to Science Applications International Corp. in Los Angeles to reverse-engineer and produce several obsolete, but relatively high-demand, components. The program follows an earlier, successful effort by the DESC to reverse-engineer and produce some 20 older bipolar parts. It is aimed at helping the Pentagon maintain a steady supply of older devices for still-active weapons systems. The DESC says the program is necessary because rapidly changing technology and the competitive environment in which chip makers operate often make them reluctant to maintain certain parts. □

LOCKHEED PUSHES HIGH-SPEED AVIONICS BUS AS DE FACTO STANDARD

Lockheed-California Co. is tapping Harris Government Aerospace Systems Division, Melbourne, Fla., to produce and supply its bus-interface module for Lockheed's Advanced Tactical Fighter. Lockheed has been promoting the 50-Mbit/s linear token-passing data bus as the military-standard high-speed data bus. The bus, which is expected to replace MIL-STD-1553B in mission-critical avionics applications, will use optical-fiber media. The Society of Automotive Engineers subcommittee SAE-AS2B (formerly SAE-AE9B), meanwhile, has published a version of the high-speed avionics bus in draft standard form, and has asked for comments. □

USING IR AND ULTRASONIC TO DETECT FAULTY BONDS IN TAB ICs

The Air Force is giving high marks to two new techniques for detecting faulty bonds in tape-automated-bonded integrated circuits. One of the techniques uses infrared light; the second is based on ultrasonics [*Electronics,* March 31, 1986, p. 9]. Vanzetti Systems in Stoughton, Mass., developed the first, which is a modified version of its so-called Laser Inspect infrared system. It can detect totally unregistered or poorly registered lead bonds. Sonoscan Inc. in Bensonville, Ill., devised the second method, which employs scanning laser acoustic microscopy principles. Both are being evaluated at Rome Air Development Center, where Eugene Blackburn, a materials research engineer in the Microelectronic Reliability Branch, says each has demonstrated its ability to detect bad bonds. The evaluation formed the year-long first part of two-year Air Force contracts. Now both companies will refine their test methods and instruments, after which both should qualify under MIL-STD-883 for TAB-bond inspection in DOD's VHSIC program. □

MILITARY AI MARKET EXPECTED TO MORE THAN DOUBLE BY 1992

The military artificial-intelligence market will more than double over the next five years, from $218 million in fiscal 1987 to more than $529 million by fiscal 1992, reports Frost & Sullivan. And the New York market-research firm says those numbers may be deceiving—the total spent on AI could go much higher. For example, the Defense Advanced Research Projects Agency's Strategic Computing Program alone accounts for 40% of the fiscal 1987 AI market dollars, or about $86 million. But Darpa will actually spend about 40% more than that, in in-house government laboratories or universities. Also not included in the estimate is non-DOD funding that may be spent by contractors on in-house development programs. □

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NEW PRODUCTS

SILICON GRAPHICS REVS UP A 10-MIPS WORK STATION

32-BIT PROCESSORS, HIGH-SPEED CACHE TURBOCHARGE IRIS 4D/60T

Keeping up in the graphics work-station race takes fast footwork, and Silicon Graphics Inc. will make its bid to stay a front-runner next week by trotting out a 10-million-instruction/s machine at the 1987 Siggraph conference. Other contenders are Sun Microsystems, Hewlett-Packard, and Apollo Computer.

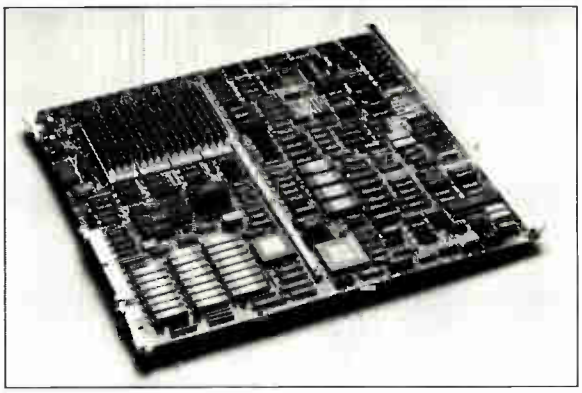
The 4D/60T super work station couples a new, single-board central-processing-unit powerhouse called the Turbo Upgrade with the high-level three-dimensional graphics performance of the Mountain View, Calif., company's Iris 4D/60. The new CPU board has 8 Mbytes of memory (upgradable to 16 Mbytes); it replaces the CPU board of the 4D/60, which was just introduced in March. In the 5-mips 4D/60, the floating-point coprocessor and 4-Mbyte memory occupied separate boards.

The 10-mips rating is based on the Dhrystone integer-calculation benchmark. The baseline is the 1-mips sustained performance of Digital Equipment Corp.'s VAX 11/780. The 4D/60T's 10 mips therefore reflects sustained performance 10 times that of a VAX 11/780.

The 4D/60 gets its speed from a CPU board consisting of two 32-bit processors from MIPS Computer Systems Inc., Sunnyvale, Calif., a high-speed dual memory cache, and up to 16 Mbytes of on-board main memory. The processors tightly couple a 12.5-MHz reduced-instruction-set computer architecture CPU to a 12.5-MHz floating-point accelerator running as a synchronous coprocessor.

By having all the major CPU components on one board, data transfer rates between components are not limited by the system bus bandwidth, which in the 4D/60T is a VMEbus. This helps to maximize system performance.

An additional performance boost comes from the 64 Kbytes of instruction-cache memory and 32 Kbytes of data cache. These large caches allow very large applications to gain the high performance that smaller programs enjoy on systems with smaller caches or none at all.



ANIMATION. The 4D/60T renders 5,500 Gouraud-shaded polygons/s—enough to display moving solid 3-d objects.

In addition to its appetite for integer calculations, 3-d graphics has a big appetite for floating-point computation. Measured on the Linpak benchmark, the floating point coprocessor in the 4D/60T delivers more than one million floating point operations/s—three times the floating point performance of the Iris 4D/60.

Other super work stations in the graphics marketplace include the 10 mips Sun-4/260CXP, which will be introduced at Siggraph. The 4/260CXP is a high-end graphics version of the Sun-4/260 super work station that Sun unveiled July 8. The Sun-4 super work stations employ RISC processor technology developed by Sun Microsystems Inc. and implemented initially by Fujitsu Ltd. in CMOS gate arrays.

Mips and megaflops are often used to gauge graphics performance, but they are geared to calculation speeds, so they offer only an indirect yardstick. There are no standard benchmarks yet for measuring graphics performance.

One fairly common measure of 3-d graphics performance is how fast the machine can draw the vectors for a 3-d wireframe image. The Iris 4D/60T can deliver over 145,000 vectors/s, fast enough for real-time rotation of complex 3-d wireframe pictures and images.

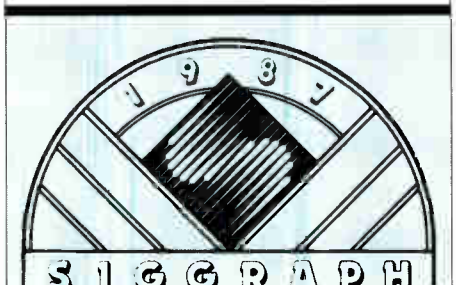
The Sun 4/260CXP is a bit faster at 150,000 vectors/s. Hewlett-Packard's HP 325SRX and Apollo Computer's DN590T both draw vectors at a 135,000 to 140,000/s rate.

POLYGON SHADING. Another commonly used measurement is the rendering speed for shaded polygons. Such performance depends heavily on the type of shading and the mix of polygon sizes—a difficult measure to standardize.

Silicon Graphics is very explicit about shading performance. It claims the Iris 4D/60T can render more than 5,500 Gouraud-shaded, Z-buffered 10-by-10 polygons/s (with smooth shading and hidden surface removal). That is sufficient to display moving, solid 3-d objects. Without specifying the type of shading and size of polygons, Sun claims 20,000 shaded polygons/s for its 4/260CXP work station. The Apollo 590T and HP 325SRX match the 4D/60T in polygon shading.

The Iris 4D/60T will be available in September from Silicon Graphics, initially only as an upgrade CPU board for the Iris 4D/60. The board will cost $7,500. The 4D/60 work station starts at $74,900. *–Tom Manuel*

Silicon Graphics Inc., 2011 Stierlin Rd., Mountain View, Calif. 94043.
Phone (415) 960-1980 [Circle 480]



The 14th annual conference of the Special Interest Group on Computer Graphics (Siggraph) promises to stir up a lot of product excitement this year. With 255 exhibitors and 25,000 attendees expected in Anaheim, Calif., on July 27-31, Siggraph will showcase the cutting edge of a rapidly expanding technology, including work stations that run as fast as 10 mips and semiconductors that cut costs while boosting graphics performance.

AMD CHIP CALMS JUMPY WINDOWS

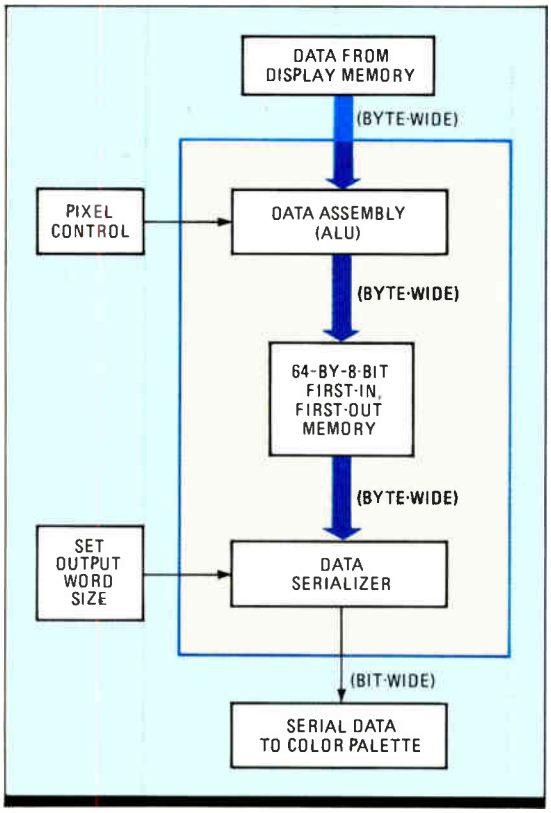
A video-data assembly chip from Advanced Micro Devices Inc. provides graphics-hardware designers with a means of smoothing out the often jerky panning and windowing performance of graphics systems employing video dynamic random-access memories. The Am8172 does it by integrating three functions that break long words into a stream of bits: an arithmetic-logic unit for data assembly; a first-in, first-out memory buffer; and a data serializer.

In bit-mapped graphics applications, the 24-pin Am8172 sits between the display memory and color palette or monitor. Through selective manipulation of the data stream, it overcomes the display glitches that until now have been part of the price designers paid for using video DRAMs.

MIXED BLESSING. Video DRAMs are widely used because they boost the speed of high-resolution bit-mapped computer graphics. Their role is primarily to decouple the refreshing of CRTs from the updating of bit maps. But the on-board shift registers of video DRAMs have been a mixed blessing, says Steve Dines, director of strategic marketing for peripheral processors at AMD in Sunnyvale, Calif.

"The very nature of a shift register makes it difficult to get access to pixels in the video screen along the boundaries," says Dines. "The video DRAM shift registers are typically organized on row boundaries, and they therefore support panning and hardware windows on word boundaries."

Since information from the shift register arrives in big chunks, including some unwanted pixels, this can make for jagged transitions. Depending on the video DRAM system, 4 to 32 pixels can be contained in a single word. That's where the Am8172 comes in. The data-assembly ALU removes unwanted bits—those along the boundary of a window, for example—from the display-memory words. Taking either one 8-bit byte or two 4-bit nibbles at a time, the ALU uses control data to determine which of the leading or trailing pixels are not needed for display, and it removes them from the word. It then organizes the pixel bits for further processing.



PIXEL FILTER. Controlled by the processor, the 8172 eliminates unwanted pixels and buffers the rest in a first-in, first-out memory for reassembly into a video-data stream.

The data serializer concatenates the pixels into a fast serial stream. In between, the 8172 provides for a temporary buffer in its 64-by-8-bit FIFO between the system's memory and display.

"It will fit in with any graphics engine," says Dines, "and it is intended for designers working on 'video-level' operations in bit maps."

The chip performs TTL-to-ECL translation. Its 10-Kbit ECL serial output supports up to 200-MHz speeds. The 8172 is available now for $31.43 each in 100-piece quantities. AMD is also planning to introduce a TTL-level output part, which will be called the Am8171, to perform serial bit speeds of up to 75 MHz for displays of 800- to 500-pixel resolutions.

–J. Robert Lineback

Advanced Micro Devices Inc., P. O. Box 3453, Sunnyvale, Calif. 94088.
Phone (408) 732-2400 [Circle 481]

135-MHz RAMDAC TARGETS TRUE GRAY-SCALE DISPLAY

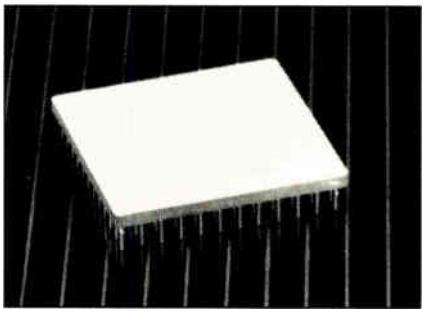
The latest addition to Brooktree Corp.'s Ramdac family of video postprocessing CMOS chips for bit-mapped graphics combines a 256-color-by-8-bit color-lookup table with an 8-bit digital-to-analog converter to target high-resolution gray-scale graphics, an important but often overlooked segment of the work-station market.

Because it was primarily designed for monochrome displays, the Bt457 has just one analog-to-digital converter instead of the three—one each for red, blue, and green signals—used in Bt450-family chips that target color graphics.

The Bt457 boasts the same 135-MHz speed of other family members, however, and is entirely software- and pin-compatible with the higher-performance Brooktree devices already incorporated in new work-station lines, an important attribute for original-equipment manufacturers.

Its 256-color-by-8-bit palette offers a gray-scale display that cannot be handled by conventional monochrome display controllers. It can display 1,280-by-1,024-pixel bit-mapped graphics with up to eight bits per pixel, along with up to 2 bits of overlay information.

The device "is in line with the original intent of our Ramdac family, which was set up to differentiate products without the necessity to redesign equipment," says Loren Schlicht, product manager. It addresses a growing "customer interest in the gray scale, which is very efficient in data transfer," says Schlicht.



COMPATIBLE. The Bt457 will run software written for Brooktree's color-graphics chips.

Ramdacs are back-end or postprocessing devices. Once a digital image has been stored in a frame buffer, the Ramdac converts it to a video—that is, an analog—signal for display.

By integrating color-lookup tables, digital-to-analog converters, and inter-

face circuitry to the frame buffer on a single chip, Ramdacs simplify DAC design, reduce component count, and reduce power consumption.

Other Brooktree Bt450 family chips oriented toward color graphics offer triple 4-bit DACs and triple 8-bit DACs. The Bt451, for example, uses three 4-bit DACs plus a dual-port 256-by-12-bit palette and can support 259 colors at a time out of a possible 4,096 [*Electronics*, April 14, 1986, p. 56].

CUTS ECL. Since its introduction in 1985, Brooktree's proprietary Ramdac architecture has established itself as the best way to provide back-end color-graphics generation, say industry sources. Among other benefits, its on-chip high-speed logic cuts the need for costly interfacing with power-hungry emitter-coupled-logic devices.

Multiple pixel ports and internal multiplexing enable TTL-compatible interfacing of up to 32 MHz to the frame buffer, says the company. The 135-MHz pipelined operation can then be maintained for video data rates needed for the newest color graphics. The Bt457 generates a RS-343-A compatible video signal and is capable of driving double-terminated 75-Ω coaxial cable without external buffering.

Engineering samples are available now for the new Ramdac, with production quantities scheduled for September. Samples of the 135-MHz device cost $130 in 100-unit quantities. Versions running at 110 MHz and 80 MHz also are offered.

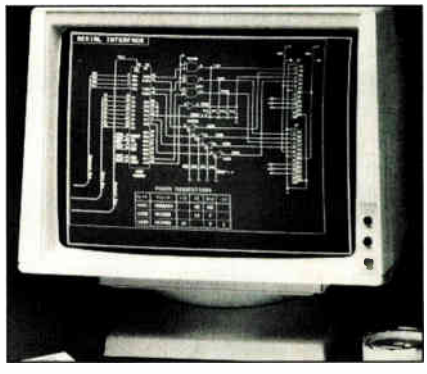
– *Larry Waller*

Brooktree Corp., 9950 Barnes Canyon Rd., San Diego, Calif. 92121.
Phone (619) 452-7580 [Circle 482]

MONITOR USES VARIETY OF GRAPHICS ADAPTERS

A 19-in. high-resolution color monitor from Conrac Display Products Inc. automatically locks onto horizontal frequencies, allowing it to operate with a wide variety of graphics adapters.

The 7250C19 Auto-Trak is compatible with every popular IBM Corp. graphics standard, including Monochrome Display Adapter, Color Graphics Adapter, and Enhanced Graphics Adapter, as well



as Hercules Inc.'s monochrome adapter in high-resolution and emulation modes.

The monitor provides 1,024-by-1,024-pixel resolution, interlaced, at scan rates from 15.75 to 37 KHz. Available now, the 7250C19 costs $2,995.

Conrac Display Products Inc., 600 N. Rimsdale Ave., Covina, Calif. 91722.
Phone (818) 966-3511 [Circle 486]

BOARD SET DELIVERS 8-FOLD SPEED BOOST

A three-board set from Vista Computer Systems Inc. combines a high-performance graphics engine with data compression and decompression technology to store, retrieve, and manipulate optically stored data eight times faster than present systems.

The VCS-2000 compresses images at 20 million pixels/s and decompresses them at 16 million pixels/s—conforming to CCITT compression/decompression standards. It is particularly suited to storing and retrieving large amounts of information from an optical disk: a document the size of a business letter can be retrieved in less than 0.5 s.

The graphics engine, based on Intel Corp.'s 82786 graphics coprocessor, provides up to 8 Mbytes of bit-mapped memory and 1,728-by-2,200-pixel resolution.

Designed for the IBM Personal Computer AT or compatibles, the board set lets system integrators build high-performance document-imaging systems on a reasonably priced platform.

Available now with drivers and software, the set is available in many configuration options. Base price for original-equipment manufacturers is $6,500.

Vista Computer Systems Inc., 860 Crusoe Circle, Thousand Oaks, Calif. 91362.
Phone (805) 894-1411 [Circle 485]

SOFTWARE GENERATES GRAPHS AT A TOUCH

Charts and graphs can be generated automatically from numerical data in any of nine chart styles with WinGraph, a graphics windows-compatible program from Media Cybernetics Inc.

Data can be entered from files created by popular spreadsheet programs such as Lotus 1-2-3, VisiCalc, and dBase III, or from mainframes in ASCII format. WinGraph supports multiple graphs in a window and uses all fonts of Microsoft Corp.'s Windows.

A special file format is included for interfacing WinGraph with other Media Cybernetics graphics software. WinGraph will be available in September for less than $200, but the exact price has not been set.

Media Cybernetics Inc., 8484 Georgia Ave., Silver Spring, Md. 20910.
Phone (301) 495-3305 [Circle 489]

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ELECTRONICS WEEK

THORN-EMI PUTS INMOS UP FOR SALE

Thorn-EMI plc, London, has signed on an investment banker, Goldman Sachs, to find a buyer for its struggling chip-making subsidiary, Inmos International plc, of Bristol, England. Thorn previously had been shopping for a minority partner, but now that Inmos has been downsized and has moved to the edge of profitability [*Electronics*, June 25, 1987, p. 34], Thorn wants to sell Inmos outright if it can.

U.S. SEMI MARKET STILL RIDING HIGH

The U.S. semiconductor market is continuing its recovery, according to figures released by the Semiconductor Industry Association. The book-to-bill ratio for June was 1.17, down slightly from May's revised 1.25. Billings rose 18.2% from May to June, to $933.4 million from $789.8 million, as shipments played catch-up with the high rate of bookings this year. Bookings for June did slip slightly from May's $1.023 billion to $980 million, a loss of 4.2%. Still, bookings finished out the second quarter a good 7.4% higher than the first.

WAFER PACT JOINS SPIRE, SUMITOMO

Spire Corp., Bedford, Mass., a U.S. wafer supplier, has ensured itself access to the Japanese market for gallium arsenide epitaxial wafers by becoming an exclusive marketing partner of Sumitomo Electric Industries Ltd. The agreement calls for Spire to grow specialized GaAs and aluminum gallium arsenide epitaxial layers on Sumitomo-supplied GaAs substrates.

WANG OFFERS 3RD PARTY SOFTWARE

In a move that should encourage more third parties to write software for its VS computers, Wang Laboratories Inc., Lowell, Mass., has begun a software marketing and distribution program for developers whose VS utilities complement strategic Wang products. Wang will become a distributor of the third-party software, listing it in its catalogs and including it in telemarketing efforts.

AI MAKER ENTERS THE MAINSTREAM...

Symbolics Inc., a Cambridge, Mass., specialist in high-end, Lisp-based artificial-intelligence work stations, is offering several new products to put its work stations into mainstream computing environments: a coprocessor board that allows Unix and MS-DOS applications to run on its work stations, a software package that lets applications developed on its work stations run on 386-based personal computers, software to link up with IBM SNA-based networks, and a C language environment.

...WHILE DEC, BBN ADD AI PRODUCTS

Digital Equipment Corp. of Maynard, Mass., and BBN Advanced Computers Inc. of Cambridge, Mass., have both strengthened their hand in the artificial-intelligence market. DEC is offering a more powerful version of its Vax Lisp software and is marketing an expert-systems development tool. Meanwhile, BBN says it has developed Butterfly Lisp, the first large-scale, shared-memory multiprocessor version of Common Lisp, which it runs on its high-performance Butterfly parallel processors.

IBM'S PS/2 IS TAKING OFF

IBM Corp.'s Personal System/2 is accounting for a hefty 38.2% of IBM's microcomputer sales, says IMS America Ltd.'s Computer Markets Division, Plymouth Meeting, Pa. The PS/2 is running second to the PC and PC/XT models, which together hold a 46.5% share, and ahead of the PC AT and XT/286 class. Meanwhile, the Armonk, N.Y. computer giant has outfitted its PS/2-compatible, 12½-lb portable PC Convertible with a bright, backlit liquid-crystal display and an enhanced power supply. The Convertible model 3 is available now for $1,695; earlier models can be upgraded for $350.

COMPAQ EMBRACES MICROSOFT'S OS/2

Rod Canion, the outspoken president of Compaq Computer Corp., may not be bullish on IBM Corp.'s new PS/2 computer [*Electronics*, May 14, 1987, p. 140], but he sure likes its operating system, Microsoft Corp.'s OS/2. At a recent briefing in New York, Canion said that "like DOS before it, OS/2 is an operating system around which the personal computer industry will grow." And he announced that Compaq will offer OS/2 and make it available for all its 80286- and 80386-based PCs in 1988.

CONTEL IN VSAT BUYING SPREE

Atlanta-based Contel ASC, a wholly owned subsidiary of telecommunications giant Contel Corp., plans to acquire Equatorial Communications Co., the leading supplier of C-band very small-aperture terminals, known also as microearth stations. VSATs are used in terminal-to-host locations to transmit and receive data quickly and efficiently. Contel also has agreed to purchase Communications Satellite Corp.'s (Comsat) Ku-band VSAT business.

CDC HIKES OUTPUT OF THIN-FILM HEADS

Control Data Corp., Minneapolis, will boost its thin-film-head manufacturing capacity by 40% to capitalize on an anticipated doubling in worldwide demand next year for the advanced heads, from 6 million to 12 million. Peripheral Components International, the Control Data division that makes disk-drive components, expects the biggest jump in demand to be from manufacturers of high-capacity 5.25-in. drives. PCI is producing thin-film heads at a rate of about 3 million per year and has capacity for about 5 million units. The division plans to boost that capacity to 7 million by the end of next year.

CUSTOMS NETWORK TO FOIL SMUGGLERS

The U.S. Customs Service has awarded Eaton Corp.'s Command Systems division, Farmingdale, N.Y., a $25 million contract to develop a C^3I system—command, control, communications, and intelligence—that is meant to combat drug smuggling. In partnership with Harris Corp.'s Government Electronics Systems division in Melbourne, Fla., and Eaton's Information Management Systems division in Westlake Village, Calif., Command Systems will tap its experience in air and vessel traffic control systems, radar displays, and signal processing to build the C^3I network.

AMD'S SCALISE IS NEW MAXTOR CHIEF

Maxtor Corp., San Jose, Calif., has a new president and chief executive officer: George Scalise, former senior vice president at Advanced Micro Devices. Scalise succeeds Maxtor cofounder James McCoy, who voluntarily stepped aside and who remains chairman. Scalise will initially face supplier-induced production problems: the company isn't getting enough thin-film disk-drive heads and has had to delay production of its 380- and 760-Mbyte 5.25-in. Winchester drives.

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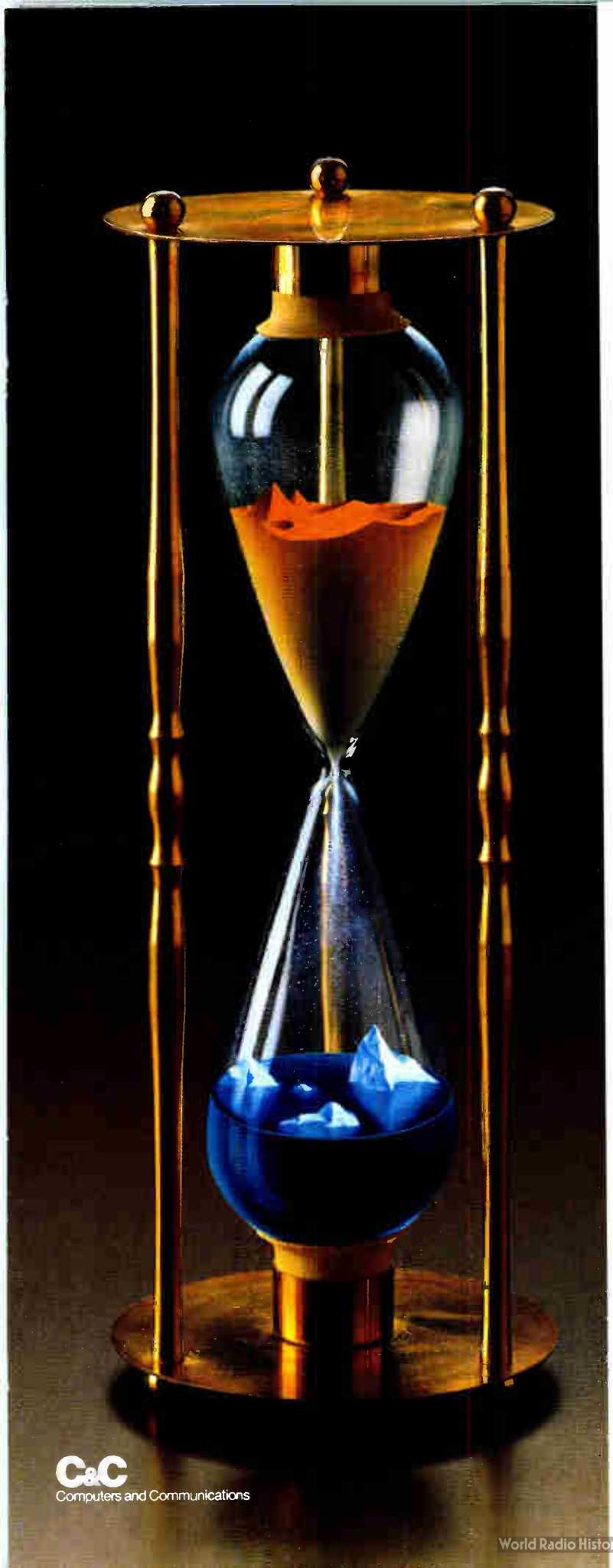

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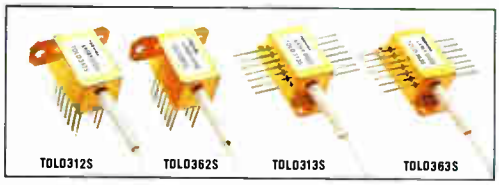

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