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Electronics

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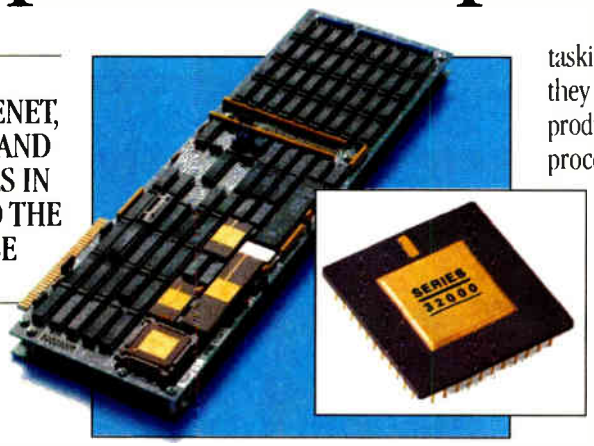

There are over 10.7 million* IBM® personal computers and compatibles in use today. That's the largest "installed base" in the world — an enormous pre-existing market that represents an enormous marketing opportunity. And National Semiconductor is leading the way for OEMs, systems integrators, VARs and VADs to take full advantage of it.

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Source: Infocorp 1987

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Experience: Cervantes called it "the universal mother of sciences." No matter what the field, there is no substitute for it. So when we at *Electronics* reorganized our news-gathering operation on the East Coast to expand and sharpen coverage of the region's technology, we decided to build on experience. The next step was a natural one: we turned to Larry Curran, a seasoned journalist who has been writing about electronics in all its phases and covering the computer and communications industries for more than 25 years.

CURRAN: A voice of experience returns to *Electronics*.

From his Boston base, Larry will cover a territory stretching from New England to the southeastern technology outposts in Georgia, North Carolina, and Florida. That territory includes some of the places where much of the most advanced technology that will take the electronics industry into the next century is being developed. For example, there is Route 128 around Boston, Research Triangle Park in North Carolina, the Atlanta area, and the east coast of Florida from Melbourne in the north to Boca Raton and Miami in the south.

Larry has the seasoning that makes him particularly well suited for the job. He has spent a dozen of his 25 years in the business in various capacities on *Electronics*, working on both coasts. Included are stints as bureau chief in Los Angeles and Boston and news editor in New York.

More recently, he served as editor-in-chief of a trio of major computer magazines: *Byte*, *Mini-Micro Systems*, and *Systems & Software*. And back in the heady days of massive expenditures on space and missile programs, when so much of the foundation for the solid-state era was being built by the Pentagon, he was a Washington-based editor on *Missiles & Rockets* magazine before coming to *Electronics* for his first tour of duty.

A native of Pittsburgh, Larry received his bachelor's degree in English from Washington & Jefferson College near his hometown.

He returns to *Electronics* after being away for about eight years. During that time he was involved not only with editing, but also with public relations. To take the maximum advantage of his expertise and years in the business, we have created a new job for him as eastern regional editor, with a particular emphasis on computer and communications technology. In addition to having responsibility for technology coverage, Larry will become a member of the magazine's Managing Editors Group.

We are glad to have him back. As for Larry, "It feels great to be back. My previous 12-year association with *Electronics* is a very special part of my career. I learned a great deal about technical journalism in the early years, and I think my contributions from Los Angeles and Boston were important.

"It's especially good to be part of an editorial team that still practices good journalism. In almost two years in public relations, I found precious few publications that prided themselves for journalistic enterprise and thorough reporting the way *Electronics* does."

Laurence Altman

April 16, 1987 Volume 60, Number 8
138,582 copies of this issue printed

Electronics (ISSN 0883-4989). Published biweekly by McGraw-Hill Inc. Publication office: 1221 Avenue of the Americas, N.Y., N.Y. 10020; second class postage paid at New York, New York and additional mailing offices. Postage paid at Montreal, P.Q. Registration Number 9034.

Executive, editorial, circulation, and advertising addresses: Electronics, McGraw-Hill Building, 1221 Avenue of the Americas, New York, N.Y. 10020. Telephone (212) 512-2000. Teletype 12-7960 TWX 710-581-4879. Cable address: M C G R A W H I L L N E W Y O R K.

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APRIL 16, 1987

Electronics

NEWS

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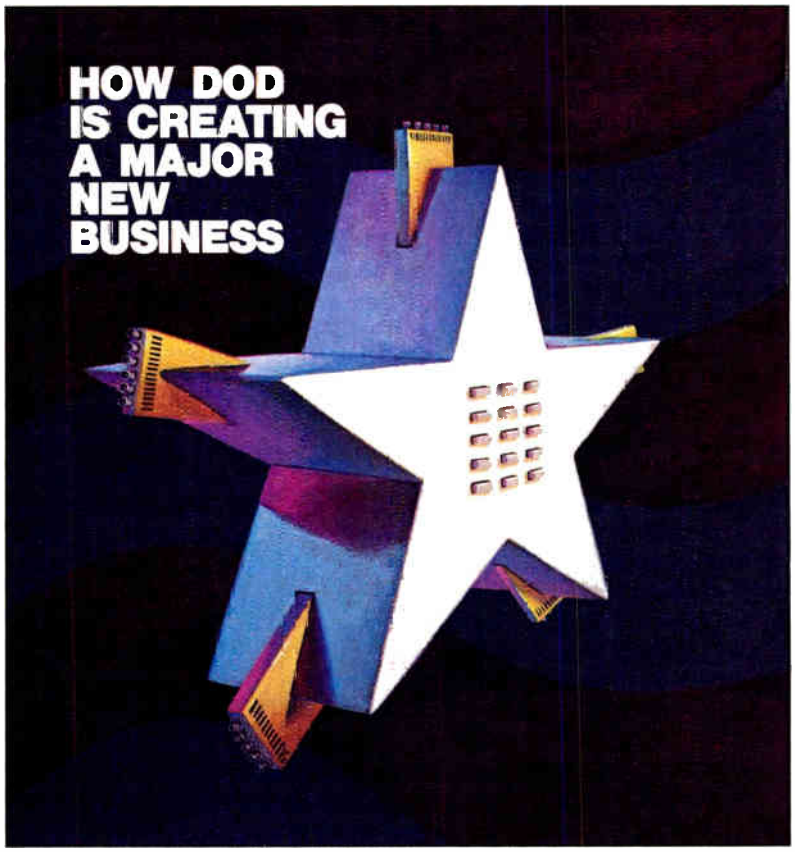

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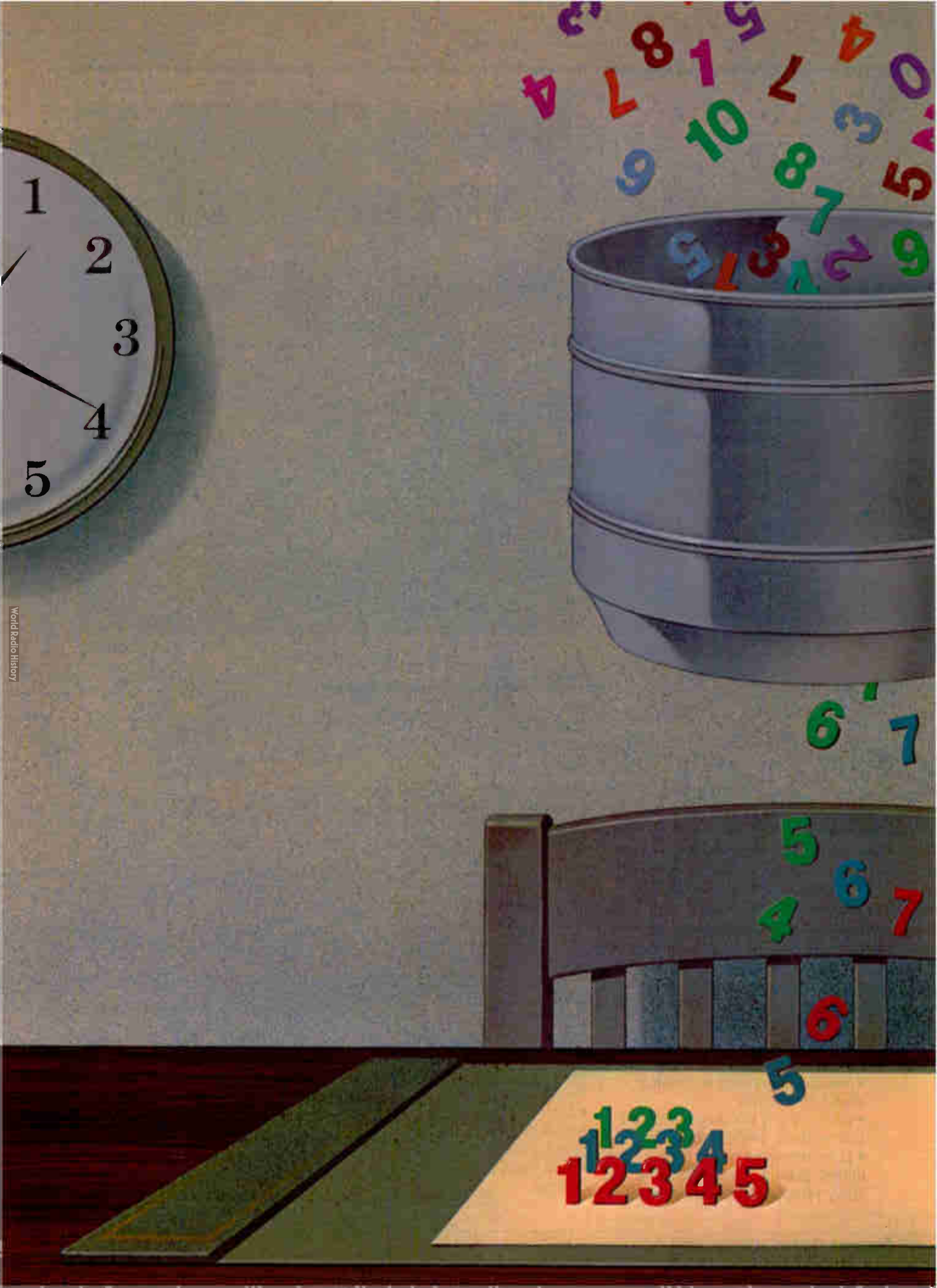
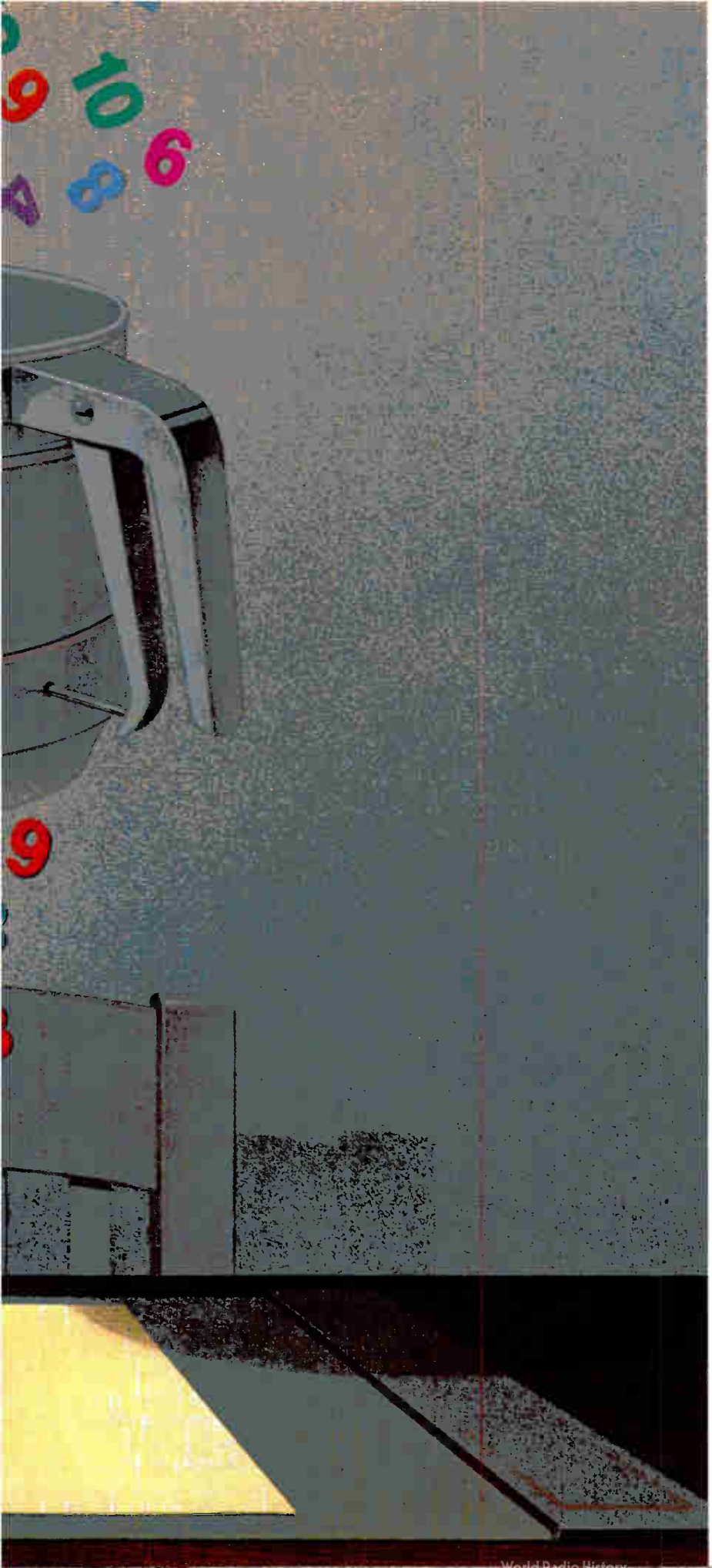
NEW PRODUCTS

DEPARTMENTS





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LETTERS

It's not materials . . .

To the editor: I am writing in reference to the February 19, 1987, article on the Josephson-junction-based Picosecond Signal Processor recently announced by Hypres Inc. This instrument represents an important achievement in the area of superconducting electronics. However, the article [p. 49], along with the accompanying one on superconductor research and development [p. 54], incorrectly emphasized difficulties IBM Corp. is supposed to have had with materials.

As a member of the IBM Josephson program, I would like to try to correct this error, which has contributed to general misunderstanding of the problems encountered in trying to fabricate large-scale Josephson circuits. The opinions expressed here are my own and do not represent an official position of IBM.

The Hypres article contains the statement that Hypres can "produce reliable, repeatable Josephson junction circuits—something that IBM, which used lead and lead alloys, was never able to do, according to Sadeg M. Faris, Hypres's president and a former IBM staff member." The accompanying superconducting R&D article refers to "the kinds of difficulties IBM was having with materials."

The IBM Josephson effort after 1981 was based on niobium-edge-junction technology, which uses niobium base electrodes and lead-alloy counterelectrodes for the junctions—and not on lead and lead-alloy devices. The use of niobium for the base electrode eliminates the problem of poor thermal cyclability, which limited the usefulness of lead-alloy-based junctions. Niobium-edge-junction technology was demonstrated to yield reproducible, reliable circuits, as first described at a Josephson workshop in August 1983.

Josephson technology has advanced significantly since IBM dropped its program in 1983. However, it was difficulties inherent in the use of Josephson devices as digital circuit elements, not materials problems, that caused IBM to abandon the technology for large-circuit-count applications. We continue to apply niobium-edge-junction technology internally for scientific and instrumentation applications, and we share the general enthusiasm for such small-scale applications that was expressed in your article.

Alan Kleinsasser
IBM T. J. Watson Research Center
Yorktown Heights, N. Y.

. . .Yes it is

Sadeg M. Faris, the president and chief executive officer of Hypres Inc., responds:

Producing reliable, repeatable Josephson junction circuits is something that IBM, which used lead and lead alloys, was never able to do. Researchers may not appreciate what it means to have a manufacturing line producing chips on a daily basis with run-to-run repeatability, a stage that IBM never approached. For instance, when I was at IBM, it took us four to five weeks to complete one fabrication run. At Hypres, a fabrication run takes four days and we come to within a few percent of a nominal target current density.

Also, IBM stuck to its guns to the end in using lead as a counterelectrode. The edge-junction Squids [superconducting quantum interference devices] failed, and the failure was attributed to the lead counterelectrode.

There was no question that IBM had a materials problem. For example, if it wasn't for the niobium oxide and its high capacitance, IBM would not be going to the edge junction to make the area very small. The edge junctions can excite very bad resonances that ultimately affect the operating margins.

Hypres is managing to make all-niobium junctions repeatedly and reproducibly without having the capacitance problem because we use a different barrier.

Who's on first?

To the editor: We must take issue with the comments made about market share in Japan for disk-drive testers [*Electronics*, Feb. 19, 1987, p. 77]. There, it is reported that "By its own estimate, Toyo [Corp. of Japan] has 50% of the Japanese market for disk-drive test equipment." My company, Applied Circuit Technology Inc., is the world's largest supplier of disk-drive test equipment—as market researcher Peripheral Research confirmed in your article. Two years ago, ACT entered the Japanese market via an exclusive distribution, support, and service agreement with Mitsui & Co., Japan's second largest trading firm. At the same time, we established the basis for our joint-venture corporation, and I am pleased to report we are on target in establishing our subsidiary.

While Toyo has been in the market for some time, it is clear that ACT, given its product range and customer base, has extended its superiority to Japan.

José C. Elaydo
President
Applied Circuit Technology Inc.
Anaheim, Calif.

Call Mizar for MDX

Correction: *Mizar Digital Systems Inc. of St. Paul, Minn., is now the manufacturer of the MDX line of STD-bus board computers [*Electronics, *March 19, 1987, p. 90]. It bought the line from Thomson Components-Mostek.*

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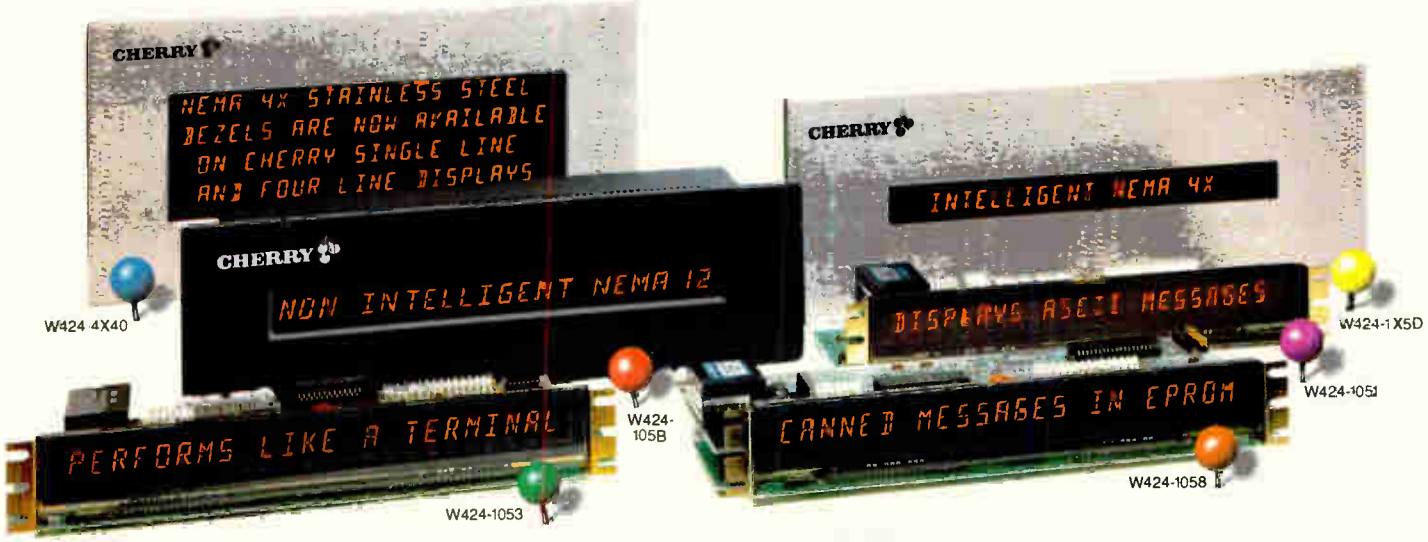

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TRADE RELATIONS MAKE BRIGHTMAN'S JOB HARDER

PLANO, TEXAS

After the Reagan Administration slapped tariff sanctions on a list of Japanese electronic products, Thomas A. Brightman was among those anxiously waiting to see what would happen next in the uncertain trade relations between the U. S. and Japan. Brightman, the vice president of operations at Visual Information Technologies Inc., was sweating out trade relations because he has to map out a global strategy of product assembly and chip procurements for the image-processing startup.

The Plano company's aim is to eventually sell powerful image-processing computers for less than $5,000. Visual Information Technologies is already on the right path with custom chips and a highly parallel architecture, known as the VITec Image Computer [*Electronics*, Feb. 19, 1987, p. 62], says Brightman.

Brightman believes the timing is right for the proper strategy in low-cost, powerful image computers. "Today, the mathematics are well understood, and the key enabling technologies are getting in place. Applications are forming up around the new technology," he notes.

Now what's needed, Brightman adds, is an international manufacturing and procurement strategy to drive $100,000 image processing below $5,000 and put it into personal computers. But how and where to build? "If I wanted to be some kind of wise guy I would say, 'Ask Ronald Reagan what he is going to do next,' because [sanctions are] creating a very turbulent situation," notes Brightman, who once headed procurement and planning for Atari Inc.'s plant in Taiwan.

The 32-year-old Brightman, who holds a BSEE from Yale University, believes volume-selling image computer systems can be assembled in Japan, Germany, or along the Texas-Mexico border. But higher tariffs on Japanese chips could change that lineup. "Is the U. S. going to create a situation where chips are selling in Japan for one third of what they cost elsewhere?" Brightman asks. "If so, then I cannot very well go to Mexico. It is a difficult situation, and we will have to maintain a flexible posture."

FROM SPEECH TO IMAGES. Brightman, a native of Syracuse, N. Y., started his career in 1976, developing microcomputer-based controls for home appliances at P. R. Mallory & Co. in Burlington, Mass. A year later, he joined the sales force of Texas Instruments Inc. in the Boston area. He eventually became a product-engineering manager for synthetic-speech products.

In 1982, Brightman went to work for a startup operation formed by Commodore Business Machines Inc. in Dallas to develop speech peripherals for its line of home computers. Two years later, a change in Commodore management shut down the operation.

Brightman then joined a team of a dozen managers formed in 1984 by Jack Tramiel, who left his post as president of Commodore and acquired Atari. For a year Brightman was vice president of engineering, and in 1985 he got his first taste of international dealings in the electronics trade as head of procurement and planning.

"Jack Tramiel is one of the great teachers in how to buy," Brightman says. "One of his mottoes is you cannot ever count on selling, but you know for sure that if you can buy something for a dollar today, you will be able to buy it for 70 cents a year from now."

At his new company, Brightman thinks he can bring "an international experience, certainly from the Asian basin. I hope I can contribute here with the ability to strike a few strong strategic alliances with some big players." And the first step will be to settle on a good location—or locations—for manufacturing. *–J. Robert Lineback*

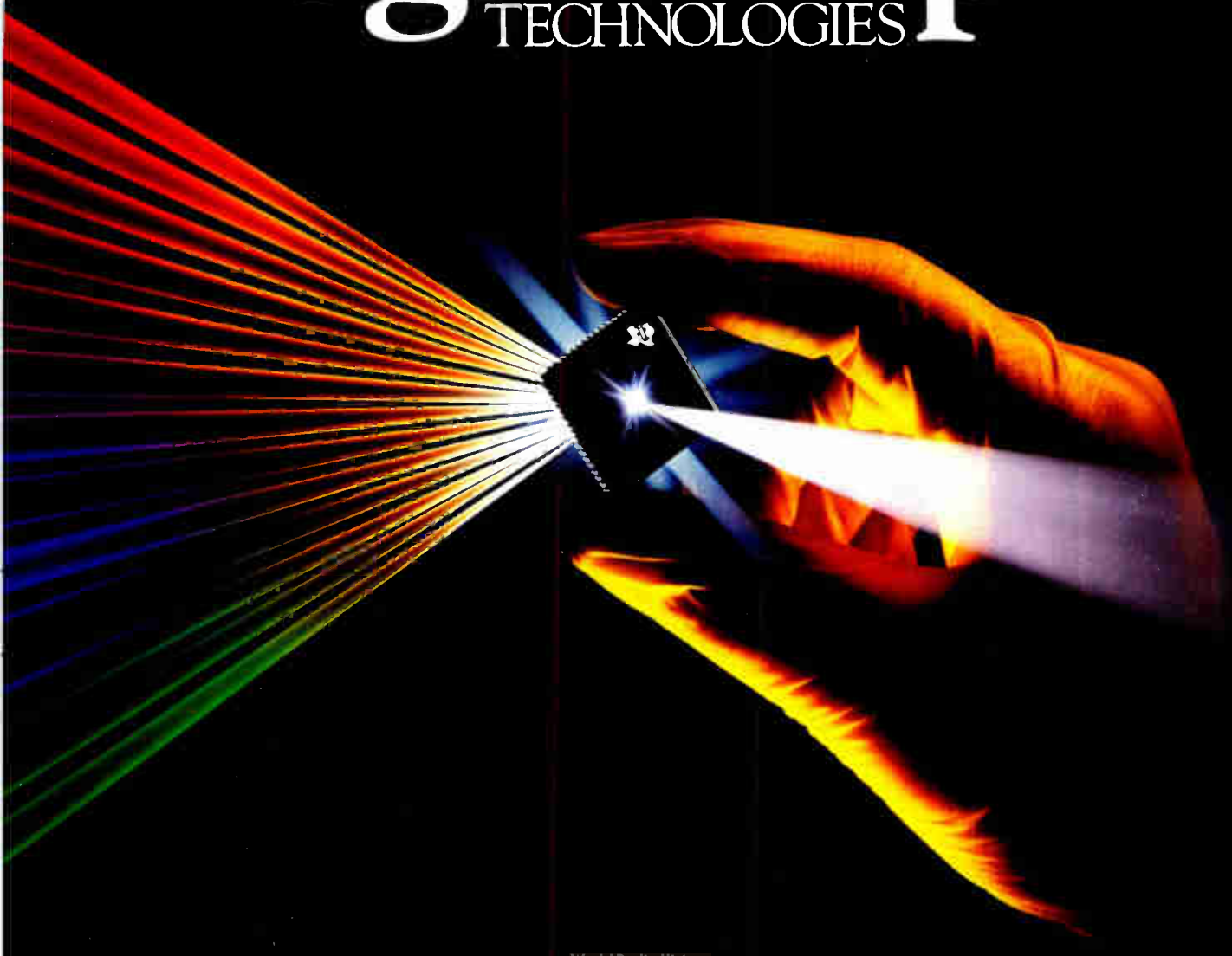
BRIGHTMAN. Divining a global manufacturing strategy in a period of flux.

TEXAS INSTRUMENTS REPORTS ON

GRAPHICS

IN THE ERA OF

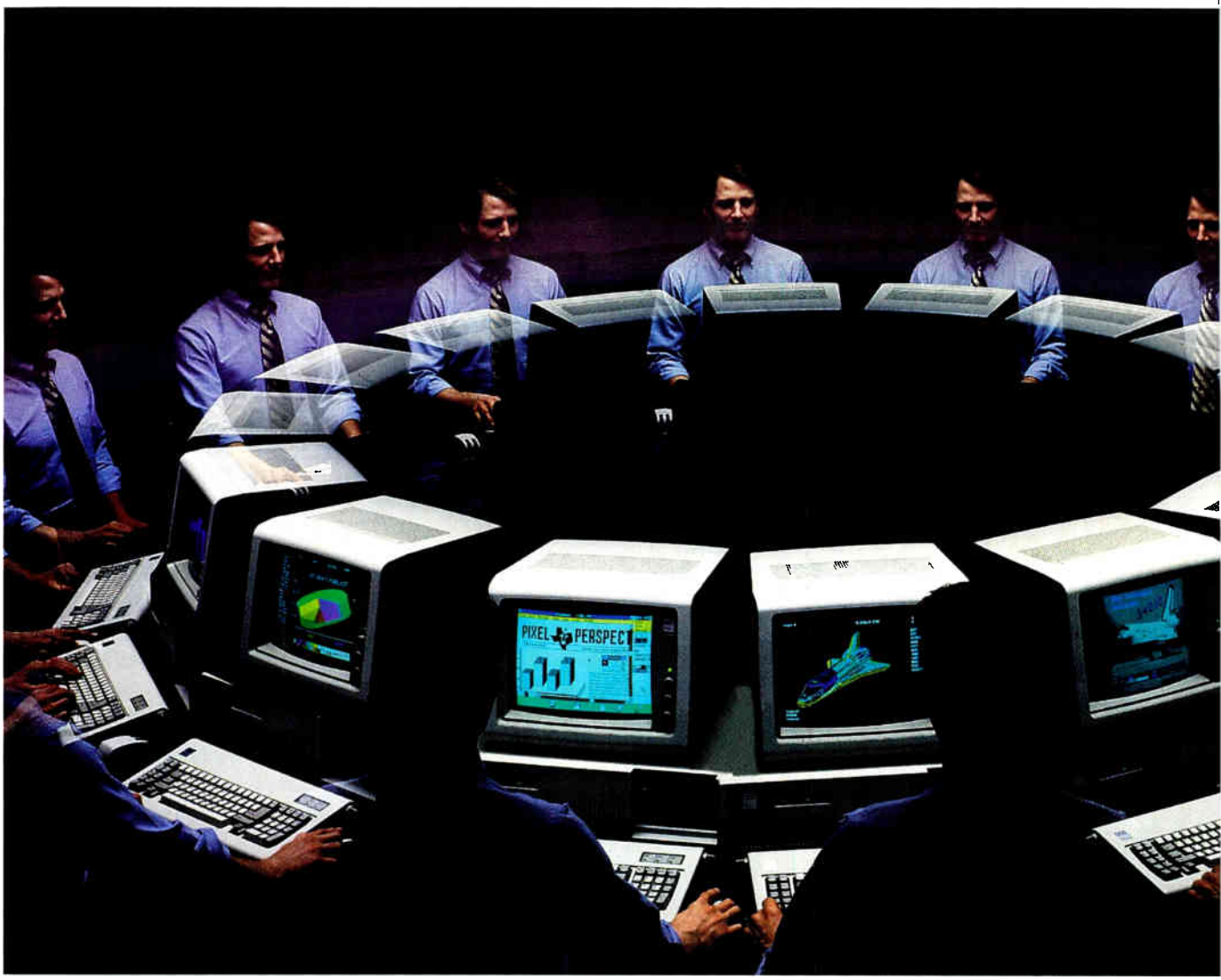
MegaChip TECHNOLOGIES



Graphics in the Era of MegaChip Technologies:

New Texas Instruments lets you program circles

plus filled polygons, spline curves, antialiased lines,



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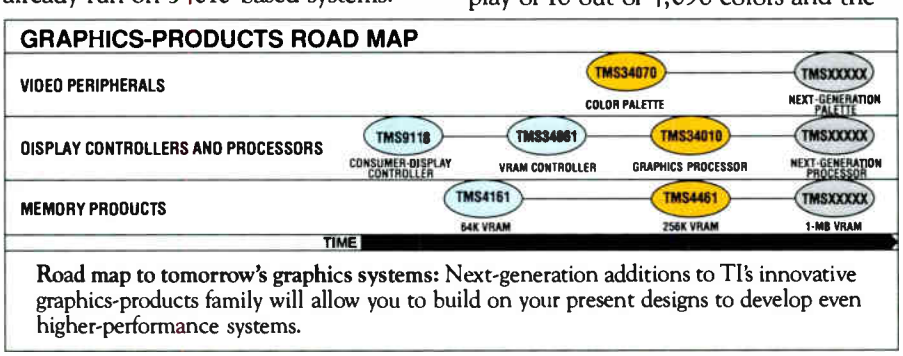

Road map to tomorrow's graphics systems: Next-generation additions to TI's innovative graphics-products family will allow you to build on your present designs to develop even higher-performance systems.

"You would think TI designed the 34010 with our technology in mind."

Luis Villalobos, Conographic president, refers to the power of the 34010 to process font outlines for desk-top publishing. Resolution up to 64K × 64K means no hardware limits for laser printers and other hard-copy devices.

Host independence and the flexibility of a device programmable in "C" language make TI's 34010 the cost/performance leader for PC displays, laser printers, desk-top publishing,

"Texas Instruments had ready the full set of development tools we needed."

As William Frentz, executive vice president at Number Nine Computer, points out, TI has ready the hardware, software, and documentation you will need to make designing in the 34010 as fast and as easy as possible.

TI's 34010 software includes a full Kernighan and Ritchie "C" compiler with extensions and an assembler package for both MS-DOS™ and VAX™ operating environments.

A graphics/math library provides source code for more than 100 functions, whereas a typical controller chip offers only 15 to 20. A special font library contains more than 100 type fonts to expedite development of desktop publishing applications.

The TMS34010 XDS/22 Emulator is a flexible, realtime, in-circuit emulator. It can be used in a stand-alone mode through a standard terminal or through a host computer with a powerful debugger interface.

To see immediately what TI's new graphics processor can do for you, just plug the TMS34010 Software Development Board into an IBM® PC-compatible or TI Professional computer. The board is populated with TI's 34010 Graphics Processor, Color Palette, and VRAMs. It provides an ideal environment for developing your own high-performance graphics applications.

For more information on TI's total graphics-system solutions, including details on TI's Graphics Design Kit and design training courses, complete and return the coupon today. Or write Texas Instruments Incorporated, P.O. Box 809066, Dallas, Texas 75380-9066.

FOR FREE ON-LINE INFORMATION, dial 1-800-345-7335 with any 80-column ASCII terminal or PC and a 300 or 1200 baud modem (EVEN or IGNORE parity, 7 data bits, 1 stop bit). At "Enter Response Code," type TIGRAFX. In Conn. dial (203) 852-9201.

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To speed the design of your graphics system, TI's range of development tools includes a comprehensive design kit (*left rear*), a realtime emulator, and a plug-in software development board. On floppy and magnetic disks: "C" compiler, assembler package, and function and font libraries. User's guides, development books, product bulletins and data sheets, and TI's newsletter, *Pixel Perspectives*, are all readily available.

Hundreds of designers must be right. Hundreds of hardware and software designers are making TI's 34010 the new graphics standard. Among them are leading board-development houses and major software vendors.

In fact, the wide range of graphics standards and application software already written for TI's 34010 makes it the easiest-to-use new graphics chip ever introduced. Here's just a sampling of the software that will run on top of Graphic Software Systems DGIS* 34010:

Software Products	Company
AutoCad™	AutoDesk
GSS*CGI™†	GSS
Master Series™	Ashton-Tate
Freelance Plus™	Lotus GPG
Graphics Development Toolkit™†	IBM
Harvard Presentation Graphics™	Software Publishing Corp.
ProDesign II™	American Small Business Computers
VersaCad™	VersaCad Corp.
Windows™†	Microsoft
Symphony™, 1-2-3™	Lotus Development
P-CAD™	Personal CAD Systems

™Trademarks are as noted.

†More than 100 graphics applications are currently available for these operating environments.

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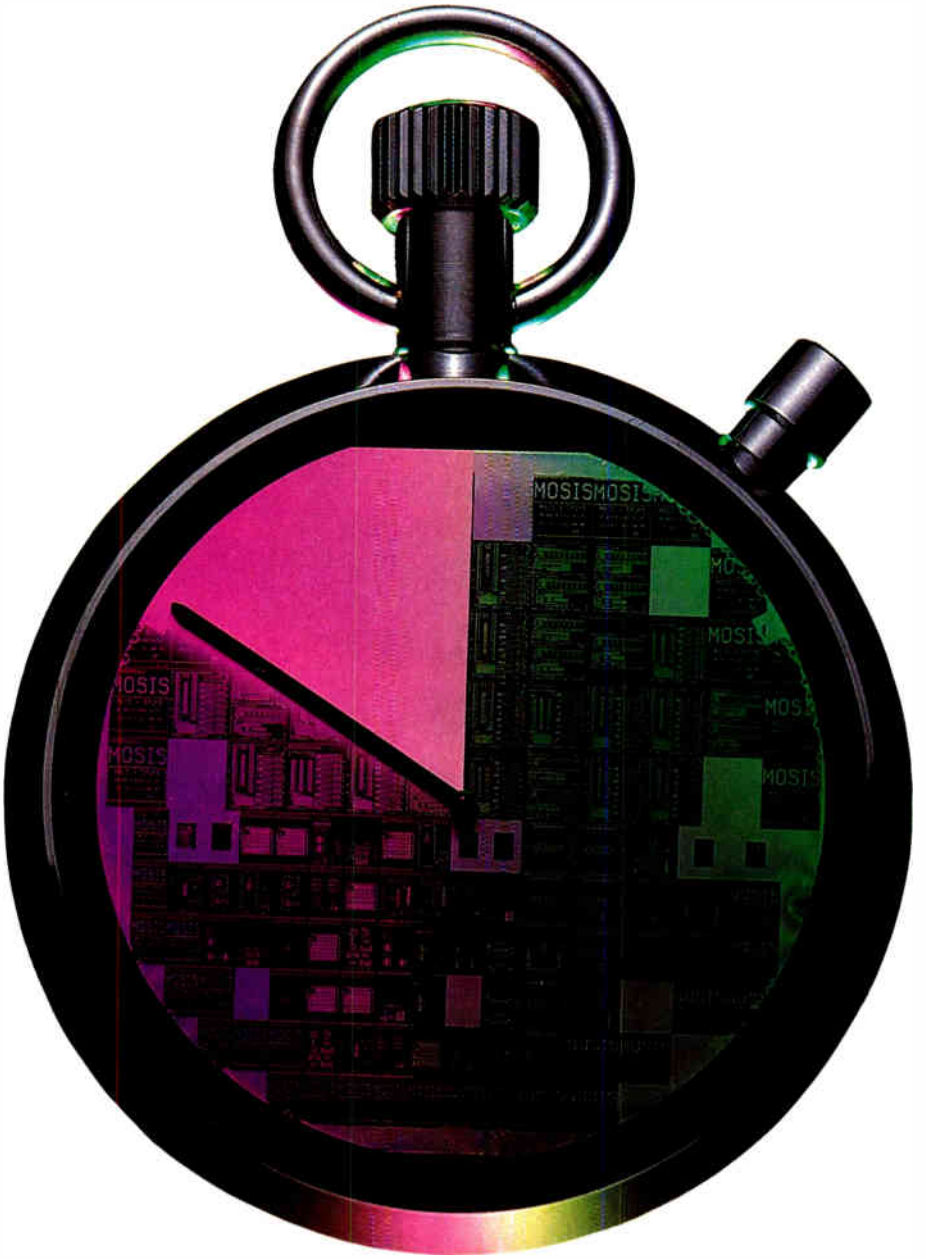

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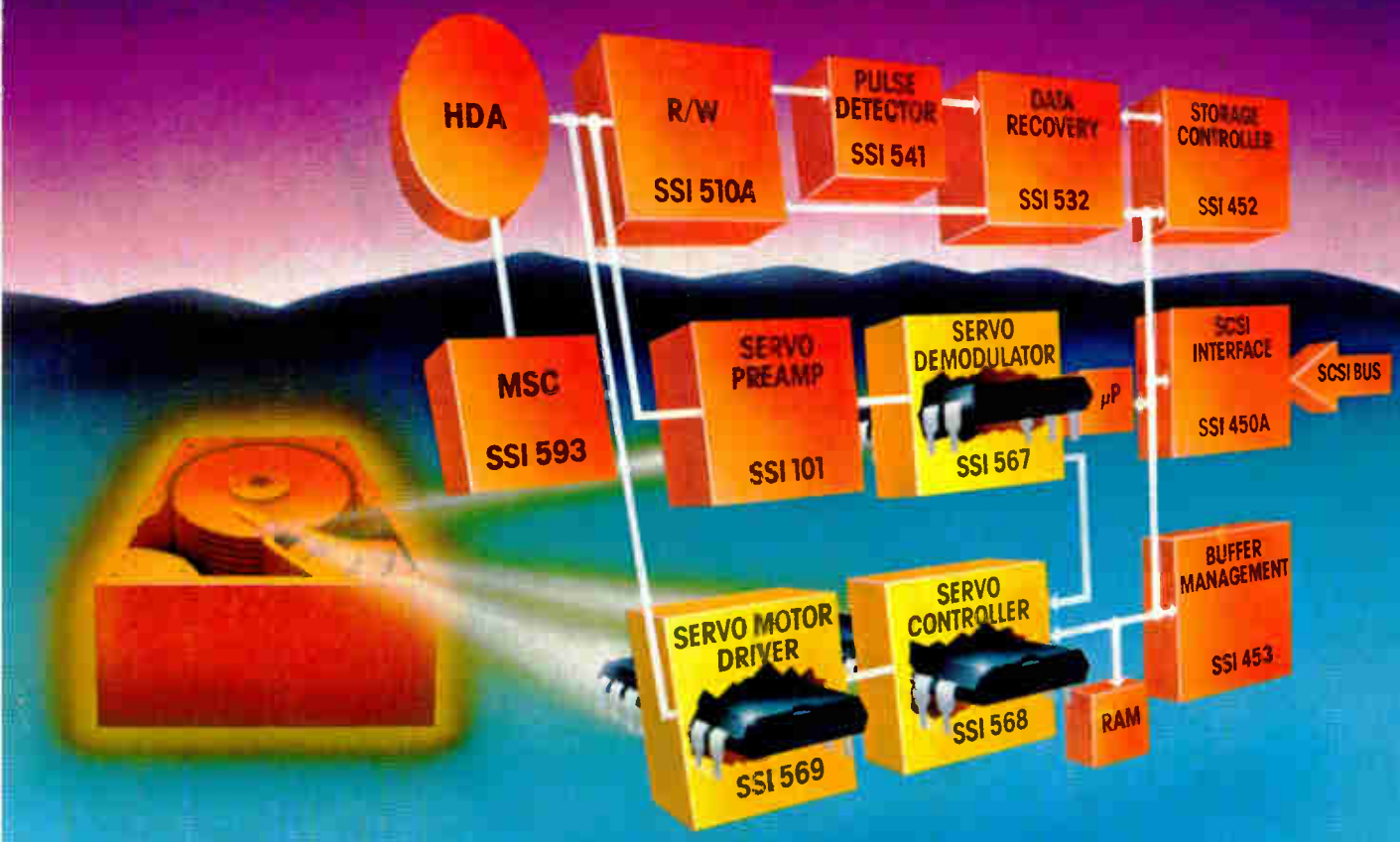

Silicon Systems now introduces the SSI Servo Chip Set. It is a 3-chip servo set for precise head positioning in the new high-performance hard disk drives. This is just the latest development in the company's program for the full integration of disk drive electronics.

The new set consists of the SSI 567 Servo Demodulator, which provides servo demodulation for dedicated-surface servo systems; the SSI 568 Servo Controller, which provides servo control; and the SSI 569 Servo Motor Driver, which is a voice coil servo motor predriver that is compatible with complementary power FETS. The chip set includes all the functional building blocks required in the servo channel, and is easily controlled via the microprocessor interface.

This chip set will break down major barriers to entry into the development of high performance hard disk drives. With its high level of integration, it provides superior performance and features for lower power, reduced board space, and lower cost.

For more information on the new SSI Servo Chip Set and the other exciting product families in the complete ESDI and SCSI Chip Sets for HDD and FDD disk drive electronics, contact Silicon Systems today.

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Circle 22 For Product Information

ELECTRONICS NEWSLETTER

AT&T AIMS TO MATCH SPEED OF TI'S NEXT DSP CHIP

Bidding to win the next round in digital signal processing, AT&T Co. is promising a new CMOS 32-bit design, which equals the more than 33 million floating-point operations/s slated for market leader Texas Instruments Inc.'s latest DSP. Like the Dallas company's future TMS320C30 [*Electronics*, March 19, 1987, p. 21], AT&T's DSP32-C is slated for early 1988 delivery. The competing designs are targeted to perform 60-ns single-cycle executions, and both have a floating-point math unit on board. AT&T is starting off with an existing n-MOS 32-bit floating-point DSP, which executes 12.5 megaflops at a top cycle time of 160 ns. The much faster CMOS version will get a bundle of new features, including 24-bit addresses instead of 14-bit, the ability to access 16 Mbits of external memory compared with 56 Kbytes, and interfaces for 8- and 16-bit microprocessors. It will be packed inside a 133-pin grid array instead of the 100-pin packages in use now and will likely take aim at advanced image-processing environments. □

GE/RCA FIRES ANOTHER SHOT IN THE BATTLE OF THE PINOUTS

It's been nine months since Texas Instruments Inc. of Dallas fired the first shot in what turned out to be a bitter summer-long skirmish between Fairchild Semiconductor and TI over the package type and pinouts used for certain advanced CMOS logic devices [*Electronics*, Aug. 7, 1987, p. 29]. But the war isn't over yet. The GE/RCA Solid State Division in Somerville, N. J., another of TI's opponents in the squabble, has completed changes to its Advanced CMOS Logic, or ACL designs, that it says have cut the ground-voltage bounce almost in half. GE/RCA has also developed a test method to measure the simultaneous switching transient that had caused problems. The problem led TI to abandon the industry-standard 20-pin package and switch to a 24-pin carrier, while moving the ground pins from the corner to the center pins. At the time, TI claimed the move would allow it to cut the transient from the 1.9-to-2.0-V range to 0.4 V. GE/RCA disagreed, and now, through redesign, has managed to cut the transient to just 1.08 V—low enough, according to Dick Funk, manager of IC applications, to eliminate any worry users might have. TI says it has made samples available of more than two dozen center-pin prototypes since the beginning of the year and that five devices are ready in volume. The Dallas company says the transient voltage for its parts is under 1.0 V. □

SUN CLIPS THE PRICE OF ITS LOW-END WORK STATION

Sun Microsystems Inc. isn't going to sit by while new high-end personal computers cut into its work-station business. Instead, Sun is slashing 37% off the price of its entry-level work station, dropping it from $7,900 to $4,995. Sun says the price cut was possible because production costs for the one-year-old Sun 3/50M fell. But executive vice president Bernie Lacroute acknowledges that one of the company's motives is to provide an alternative to machines such as Apple Computer Inc.'s Macintosh 2, and to ward off competition by the rash of upcoming work stations based on Intel Corp.'s 80386 microprocessor. Apple called the price cut "significant" but says it won't prevent the Mac 2 from carving out a chunk of the market. The Mac 2 is attractive because, with Unix operating-system software, it can act as a work station on a Sun network. Other high-end personal computers—such as IBM Corp.'s RT PC and Personal System/2 model 80 (see p. 46)—offer business software that Sun doesn't provide. But Sun points out that personal computers don't offer the multitasking and distributed computing capability afforded by work stations. Sun's move may also be the prelude to a series of higher-performance machines expected later this year. □

ELECTRONICS NEWSLETTER

NOW THE SIA WARNS AGAINST MITI-IMPOSED PRODUCTION CUTBACKS

Concerned about possible chip shortages, the Semiconductor Industry Association is taking a firm stand against limitations imposed by the Japanese government on memory chip production there. SIA president Andrew Procassini warned recently that Japan must not intervene "to restrict the flow of semiconductors to world markets." He added: "Quantitative restrictions by Japan on semiconductor exports would threaten to create artificial semiconductor shortages outside Japan," and would be "counterproductive" in resolving the trade dispute between the U. S. and Japan. "We did not ask for artificial restrictions, we asked for no more dumping," says one SIA official at the group's Sunnyvale, Calif., headquarters. □

MOTOROLA IS LATEST TO ADOPT NATIONAL'S TAPE PAK CHIP CARRIER

National Semiconductor Corp.'s Tape Pak, a small, leaded plastic chip carrier based on a single-layer tape-automated-bonding process [*Electronics*, Aug. 21, 1986, p. 74], is gaining support. The latest chip maker to adopt the package is Motorola Inc., the second-largest integrated-circuit producer in the U. S. The Phoenix, Ariz., company will use the tiny square packages with leads on 20-mil centers to house high lead-count VLSI circuits. Motorola is the second company to adapt National's packaging technology; about four months ago, the Delco Products Division of General Motors Corp., in Kokomo, Ind., also agreed to use Tape Pak. The list of supporters is expected to grow, especially now that it has been registered by the Joint Electronic Device Engineering Council (JEDEC) committee for mechanical standardization and second sourcing. □

SAPC SLAPS LOTUS WITH 1-2-3 'LOOK-AND-FEEL' COPYRIGHT SUIT

Lotus Development Corp. doesn't see much merit in the $100 million copyright-infringement lawsuit brought by SAPC Inc. The action is "an ill-considered first strike by parties who have been preparing to release their own clone of Lotus 1-2-3," according to Henry Glutman, Lotus' litigation attorney. The suit resurrects a controversy over whether Lotus and its founder, Mitchell Kapor, who has since left, substantially copied the "look and feel" of Software Arts' VisiCalc spreadsheet in developing Lotus 1-2-3. Lotus bought VisiCalc last June from Software Arts Products Corp., since renamed SAPC. SAPC is suing to rectify infringements that allegedly occurred before Lotus purchased the VisiCalc. "We don't bring lawsuits that don't have substantial chances for success," says Mark Michelson, SAPC's lawyer. □

AMD ADDS PROTOCOL CONVERTER TO ITS ISDN CHIP SET

Advanced Micro Devices Inc. won't see first silicon for at least eight months, but buoyed by support from AT&T Co., the Sunnyvale, Calif., chip maker has announced what it claims is the industry's first single-chip protocol controller for the integrated services digital network. The new part, offered with the five existing members of AMD's ISDN chip family, will provide a "total solution" to both ends of ISDN's "S" interface, which connects terminal equipment with a digital private branch exchange. The AM79C401, which will be fabricated in 1.2-μm double-metal CMOS technology, will replace a board full of components and cut hardware costs in half. Software development costs would also be cut, AMD says, because the chip has built-in real-time management functions, well-defined interfaces, and an overlying software module. AT&T is supporting development of the controller by providing documentation for its Digital Multiplexed Interface, part of its ISDN solution, and will share in testing and certifying the new part. □

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Introducing Data Translation's new iSBX compatible data acquisition module series. Now IBM PC users can have analog I/O flexibility tailored to fit their needs.

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The chart below shows you some of the available capabilities. All the DTX modules can be interfaced with the IBM PC, XT, or AT, and are ideal for industrial, factory or laboratory applications.

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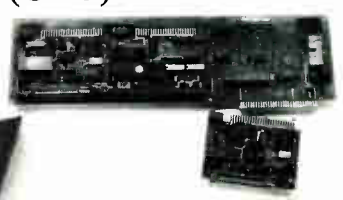

DT2806 mother board with A/D module (DTX311) and D/A module (DTX328) shown installed and digital I/O module (DTX350) separate.

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DT2806*	295	to 80	–	–	to 24	–	–	to 72	3
DTX311 A/D	425	16SE/8DI	12	20	–	–	–	–	–
DTX311EX A/D Expander	385	48SE/24DI	12	20	–	–	–	–	–
DTX328 D/A	425	–	–	–	8	12	5	–	–
DTX350 DIO	199	–	–	–	–	–	–	24	–

*The DT2806 has 3 iSBX compatible connectors for any mix of DTX modules

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Circle 26 on reader service card

PRODUCTS NEWSLETTER

NEC'S 32-BIT MICROPROCESSOR OUTSPEEDS RIVALS AT 6.6 MIPS

Japan's first microprocessor with 32-bit data and address buses runs at a maximum rate of 6.6 million instructions per second—4 mips is typical of 32-bit chips. Fabricated in 1.5-μm CMOS, the NEC Corp. V 70 has a dynamic bus sizing that enables it to match input/output with 8-, 16-, and 32-bit buses. Its TRON operating system will make it shine in real-time control and robot applications. The 20-MHz V 70 also incorporates floating-point facilities on-chip and has a function redundancy monitor for fault-tolerant computing. Sample price of the device is $687.52. Prices will be lower for production quantities. □

CHIP INTEGRATES PERIPHERAL BUFFER, SCSI INTERFACE TO SAVE BOARD SPACE

Designers of controllers for half-height disk drives, where board space is at a premium, can save precious real estate with NCR Corp.'s latest CMOS Small Computer Systems Interface circuit, the NCR 53C300, which integrates two chips into one. While providing the same SCSI control functions found on NCR's year-old NCR 53C80, the new chip also has dual-port peripheral interface buffers ranging from 256 bytes to 64 Kbytes. Developed originally for Rodime Europe Ltd., Glenrothes, Scotland, the 53C300 is now being brought to market by NCR Corp.'s Microelectronics Division, Colorado Springs, Colo. Available now, it comes in an 84-pin plastic leaded chip carrier for $21.50 each in 1,000-unit quantities. □

WANG ADDS LOW-END TEMPEST MINIS

An expanding government and business market for secure computer systems has prompted Wang Laboratories to add two entry-level 32-bit minicomputers to its Tempest systems product line. Available from the Lowell, Mass., company in May, the $13,500 VS 5T supports as many as eight users and 16 peripheral devices; the $21,500 VS 6T supports 16 users and 24 peripherals. Other machines in the Tempest line include the $38,000 VS 65T, which supports 40 users, and the $89,000 VS 85T, which supports 64 users. The new VS 5T and VS 6T feature fully removable storage media in the central processing unit and intelligent peripherals that can be taken out and locked up when the system is shut down. Both minicomputers can be used either as stand-alone systems or as end-node systems in large distributed networks, and neither requires special housing, power, or air-conditioning. The proprietary VS architecture allows the machines to interactively process data, text, voice, and images—a feature that Wang claims is unique to this architecture. □

CDC PLUNGES INTO 1-GIGABYTE DISK-DRIVE FRAY

Competition in the market for 1-gigabyte 9-in. half-rack disk drives for mainframes is heating up with Control Data's Corp.'s entry. The FSD III (for Fixed Storage Drive) provides 1.03 gigabytes of unformatted storage capacity and a 2.4-Mbyte/s transfer rate. Its cost is about $6.80 per megabyte, which the Minneapolis company says puts it in the same league as NEC's D2363, a 1.13-gigabyte 9-in. half-height drive, and Hitachi's 1.05-gigabyte DK-815-10. An improved oxide media and better thin-film head design mean the FSD III can handle nearly twice as much data as its predecessor, the 515-Mbyte FSD II. It records on seven disk platters with 26 heads at densities of 1,283 tracks/in. and 20,254 bits/in. The unit supports three interfaces: SMD, SMD-E (for storage module drive with ECL drivers and receivers), or IPI (for intelligent peripheral interface). Available in the third quarter, it will sell for $6,990 in quantities of 250. □

PRODUCTS NEWSLETTER

VIDEO CONFERENCING SYSTEM PROMISES TO SLASH COSTS

Look for full-motion color video conferencing to become more affordable April 21 when Compression Labs Inc. unveils a system that uses switched 56-Kbit/s telephone lines, costing $50 per hour, instead of T1 lines that rent for up to eight times more. The Rembrandt 56's motion-compensation technique squeezes 40-Mbit/s full-motion color video frames down to 56 Kbits/s for transmission primarily by predicting movements within the frame. But it limits the number of people in the picture to just two or three. A video conferencing pioneer, the San Jose, Calif., company also offers 1.5-Mbit/s T1 systems and 384-Kbit/s systems with the same proprietary differential-transform coding now used in the 56-Kbit/s system. The Rembrandt 56 codec costs $68,000—the same as the company's T1 codec. A complete 56-Kbit system, including five personal-computer-based stations, cameras, and the codec, costs $113,500. The product is available this month. □

PERFORMANCE SEMICONDUCTOR PUSHES CMOS SRAM ACCESS UNDER 10 NS

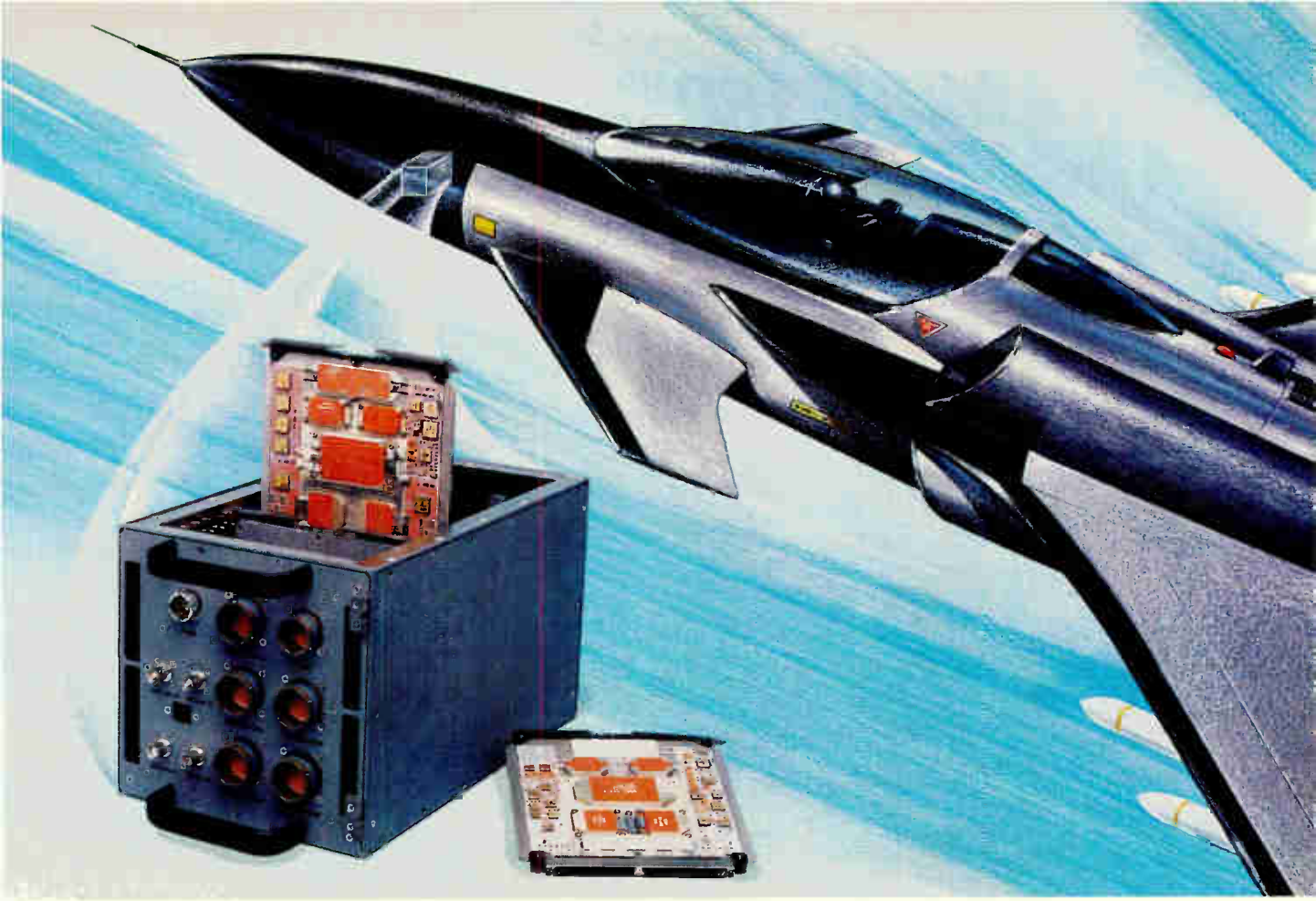
With its 8-ns access time, Performance Semiconductor Corp.'s 1-Kbit CMOS static random-access memory is fast enough to challenge super-fast bipolar ECL circuits and 25% faster than the fastest TTL input/output SRAM. Organized into 256 by 4 bits with six-transistor cells, the P4C422-8PC aims at replacing ECL bipolar devices in such applications as high-speed caches, writable control stores, and lookup tables. Besides its speed, the device offers better electrical margins and better protection against single-event upsets than conventional four-transistor cells, says the Sunnyvale, Calif., company. Available now, the part costs $19.95 each in 100-piece quantities, and delivery takes two to eight weeks after receipt of order. □

TOOL KIT SPEEDS DEVELOPMENT OF MULTIBUS II COMPUTERS

Designers of Multibus II-based single-board computers can now get all their development tools in one package, thanks to the Micro Industries MIB II 186/110 I/O Development Kit. Engineers can use it to design and debug Multibus II computers on either an Intel Corp. Series II or Series IV Development System or on a standard RS-232-C terminal. The MIB II 186/110 contains both hardware and software, says the Westerville, Ohio, company. Hardware includes an Intel 80186 microprocessor, a separate configuration processor, up to 256 Kbytes of electrically programmable read-only memory, up to 512 Kbytes of DRAM, an Intel 82258 direct-memory-access controller, an Intel 8259 interrupt controller, a serial communications port, and prototype space occupying about one third of the board area. The software includes the mSDM-186 Monitor/Debugger, a debugging monitor compatible with Intel's iSDM-86 Monitor/Debugger. Available now, the kit is priced at $2,000 for single units. □

SIMULATOR LIBERATES MICROWAVE DESIGNERS FROM THE LAB

Microwave circuit designers can throw away their breadboards and lab instruments and for the first time simulate their nonlinear circuits on personal computers with Eesof Inc.'s new design tool. The Westlake Village, Calif., company's Microwave Simulator Spice 1.1 can display signal power at specific frequencies, sweep power levels and frequencies over specified ranges, and compute relative signal strengths. It also allows multiple waveform inputs to compute intermodular distortion instead of having the engineer run each signal separately and compute the composite algebraically. The licensing fee starts at $8,450, and the tool runs on the IBM Corp. PC/XT, PC AT, and compatibles. □



TI high-density power supplies; the performance edge in military electronics packaging.

Power supplies are the heart of every electronic system. But power supply packaging hasn't kept pace with the higher density requirements of today's military systems.

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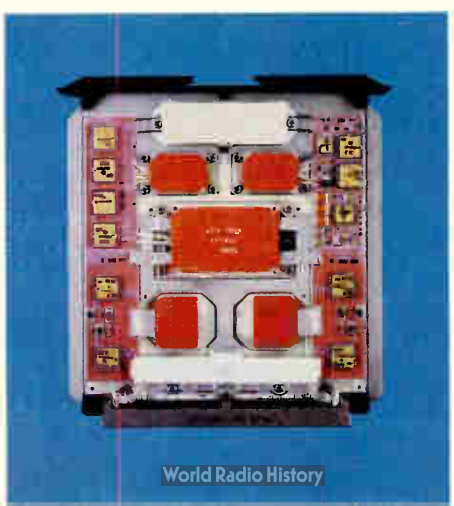

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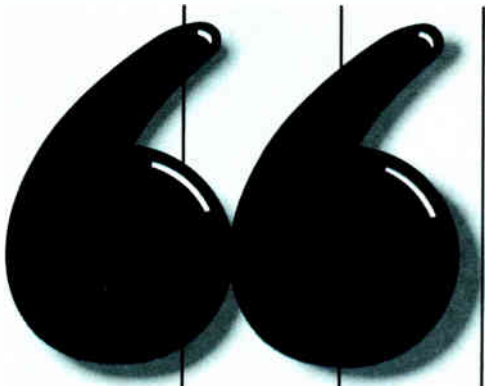

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MB81C86
-55, -70 64Kx4
MB81C84
-45, -55 64Kx4
MB81C81
-45, -55 256Kx1
MB84256
-10L/LL 32Kx8
MB84256
-12L/LL 32Kx8
MB84256
-15L/LL 32Kx8
MB81C71A
-25, -35 64Kx1
MB81C71
-45, -55 64Kx1
MB81C74
-25, -35 16Kx4
MB81C75
-25, -35 16Kx4
(w/OE)
MB81C79A
-35, -45 8Kx9
MB81C79
-45, -55 8Kx9
MB81C78A
-35, -45 8Kx8
MB81C78
-45, -55 8Kx8
MB8464
-12L/LL 8Kx8
MB8464
-15L/LL 8Kx8
MB8464A
-10L/LL 8Kx8
MB8464A
-12L/LL 8Kx8
MB8464A
-15L/LL 8Kx8
MB8464A
-80L/LL 8Kx8
MB8464A
-10W, -15W 8Kx8

MB8167A
-55, -70 16Kx1
MB8167
-35, -45 16Kx1
MB8167
-45W, -55W 16Kx1
MB81C67
-35, -45 16Kx1
MB81C69A
-25, -30, -35, -45 4Kx4
MB81C68A
-25, -30, -35, -45 4Kx4
MB8168
-55, -70 4Kx4
MB81C68
-45W, -55W 4Kx4
MB81C68
-55, -70 4Kx4
MB8422
-90, -120 2Kx8
MB8421
-90, -120 2Kx8
MB8417A
-12, -12L 2Kx8
MB8417A
-15, -15L 2Kx8
MB8417
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MB8416A
-12L, -15L 2Kx8
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MB70802
-20 512x9
MBM7700H
-5 256x16
MBM100422A
-5, -7 256x4
MBM10422A
-5, -7 256x4
MBM100490
-15 64Kx1
MBM100490
-25 64Kx1
MBM10490
-15, -25 64Kx1
MBM100480
-15, -25 16Kx1
MBM100480A
-10 16Kx1
MBM100484A
-10 4Kx4
MBM100484
-15 4Kx4
MBM10480A
-10 16Kx1
MBM10484A
-10 4Kx4
MBM10480
-15, -25 16Kx1
MBM7750
-10 1Kx16
MBM100470
-10, -15 4Kx1
MBM100474A
-5, -7 1Kx4
MBM100474A
-10, -15 1Kx4
MBM10470A
-10, -15 4Kx1
MBM10474A
-5, -7 1Kx4
MBM10474A
-10, -15 1Kx1
MBM10415AH
1Kx1

PROMS

MBM7226RA
-20, -25 512x8
MBM7226RS
-20, -25 512x8
MB7123E/H
-35, -45 512x8
MB7124E/H
-35, -45 512x8
MB7115E/H
-35, -45 512x4
MB7116E/H
-35, -45 512x4
MB7117E/H
-35, -45 256x8
MB7118E/H
-35, -45 256x8
MB7113E/H
-35, -45 256x4
MB7114E/H
-35, -45 256x4
MB7113L
LOW-PWR 256x4
MB7114L
LOW-PWR 256x4
MB7212RA
-20 32x8
MB7212RS
-20 32x8
MB7111E/H
-25, -35 32x8
MB7112E/H
-25, -35 32x8
MB7111L
LOW-PWR 32x8
MB7112L
LOW-PWR 32x8
MB7143E/H
-55, -65 8Kx8
MB7144E/H
-55, -65 8Kx8
MB7144Y
-45 8Kx8
MB7242RA
-20 4Kx8
MB7242RS
-20 4Kx8
MB7141E/H
-55, -65 4Kx8
MB7142E/H
-55, -65 4Kx8
MB7142E/W
-55, -65 4Kx8
MB7151E/H
-45, -55 4Kx4
MB7152E/H
-45, -55 4Kx4
MB7152Y
-35 4Kx4

MB7133E/H
-45, -55 4Kx4
MB7134E/H/Y
-35, -45, -55 4Kx4
MB7238RA
-20 2Kx8
MB7238RS
-20 2Kx8
MB7137E/H
-45, -55 2Kx8
MB7137E/H/SK
-45 2Kx8
(Skinny DIP)
MB7138E/H
-45, -55 2Kx8
MB7138E/H/SK
-45 2Kx8
MB7138Y/SK
-35 2Kx8
MB7138E/W
-55 2Kx8
MB7127E/H
-45, -55 2Kx4
MB7128E/H/Y
-35, -45, -55 2Kx4
MB7128E/W
-55 2Kx4
MB7232RA
-20, -25 1Kx8
MB7232RS
-20, -25 1Kx8,
MB7131E/H
-45, -55 1Kx8
MB7131E/H/SK
1Kx8
MB7132E/H/Y
-35 1Kx8
MB7132E/H/Y/SK
1Kx8
MB7121E/H
-35, -45 1Kx4
MB7122E/H/Y
-30 1Kx4

DRAMS

MB85227
-10, -12 256Kx9
MB85226
-10, -12 256Kx9
MB85225
-10, -12 256Kx8
MB85224
-10, -12 256Kx8
MB85214
-12, -15 256Kx8
MB85213
-12, -15 256Kx8
MB85211
-12, -15 512Kx4
MB85210
-12, -15 512Kx4

MB85206
-10, -12 256Kx4
MB85205
-10, -12 256Kx4
MB85204
-10, -12 256Kx4
MB85203
-10, -12 256Kx4
MB81C4257
-10, -12, -15 256Kx4
MB81C4256
-10, -12, -15 256Kx4
MB81C4258
-10, -12, -15 256Kx4
MB81C4259
-10, -12, -15 256Kx4
MB81C1000
-10, -12, -15 1Mx1
MB81C1001
-10, -12, -15 1Mx1
MB81C1002
-10, -12, -15 1Mx1
MB81C1003
-10, -12, -15 1Mx1
MB85208
-10, -12 1Mx1
MB85201
-10, -12 1Mx1
MB81C258
-10, -12, -15 256Kx1
MB85108A
-10, -12 256Kx1
MB85103A
-12, -15 64Kx8
MB85101A
-10, -12 64Kx4
MB81C466
-10, -12, -15 64Kx4
MB81464
-10, -12, -15 64Kx4
MB81461
-12, -15 64Kx4
MB8266A
-10, -12, -15 64Kx1
MB8265A
-10, -12, -15 64Kx1
MB8264A
-10, -12, -15 64Kx1
MB85237
-10 256Kx9
(CMOS)

NON-VOLATILE MEMORY

MBM2212
-20, -25 256Kx8
MB831000
-15, -20 128Kx8
MB831124
-35 128Kx8

MBM27C1000
-20, -25 128Kx8
MBM27C1001
-20, -25 128Kx8
MBM27C1028
-15, -20, -25 64Kx16
MBM27C1024
-20, -25 64Kx16
MB83512
-15, -20 64Kx8
MBM27C512
-20, -25, -30 64Kx8
MB27C256H
-10, -12 32Kx8
MB83256
-25 32Kx8
MBM27C64
-20, -25, -30 32Kx8
MBM27C64
-25X, -30X/W 32Kx8
MBM27C256A
-20, -25 32Kx8
MBM27C256A
-20W, -25W 32Kx8
MBM27256
-17, -20, -25 32Kx8
MBM27256
-20X, -25X, -30X 32Kx8
MBM27C128
-20, -25 16Kx8
MBM27128
-20, -25, -30 16Kx8
MBM27128
-25X/W, -30X/W 16Kx8
MBM28C64
-25, -35 8Kx8
MBM28C65
-25, -35 8Kx8
MBM2764
-20, -25, -30 8Kx8
MBM2764
-30X, -30W 8Kx8

4-BIT MICRO-CONTROLLERS

MB8840 SERIES
48-PIN FPT
42-PIN DIP
28-PIN DIP
MB8850/H/B SERIES
48-PIN FPT
MB88200/H/B SERIES
16-PIN DIP
16-PIN FPT
MB88210 SERIES
20-PIN DIP

MB88400/H SERIES
48-PIN FPT
MB88410/H SERIES
42-PIN DIP
48-PIN FPT
MB88420/H SERIES
64-PIN DIP
MB88500/H SERIES
48-PIN FPT
42-PIN DIP
MB88510/B SERIES
64-PIN DIP
42-PIN DIP
MB88520/B SERIES
64-PIN DIP
64-PIN FPT
MB88530 SERIES
42-PIN DIP
48-PIN FPT
MB88540 SERIES
70-PIN FPT
80-PIN FPT
MB88550 SERIES
80-PIN FPT
MB88560 SERIES
80-PIN FPT
MB88P500/H SERIES
48-PIN FPT
MB88700 SERIES
64-PIN FPT

8-BIT MICRO-CONTROLLERS

MBL8749
EPROM
40-PIN DIP
MBL8742
EPROM
40-PIN DIP
MBL8649
40-PIN DIP
MBL80C39
CMOS SINGLE CHIP MCU
MBL80C49
CMOS SINGLE CHIP
MBL8039
MCU 128B RAM
MBL8C49
2KB ROM 128B RAM
MBL8035
MCU 64B RAM
MBL8048
1KB ROM 64KB RAM
MBL8042
UNIVERSAL PERIPH. INTERFACE
MBL8051AH
256B RAM
MBL8031AH
4KB ROM 245B RAM

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NMOS MPU 68-PIN LCC
MB8089/-2
I/O 40-PIN DIP
MB8088/-2
NMOS 40-PIN DIP
MBL80286
NMOS MPU 68-PIN LCC
MBL80186
NMOS MPU 68-PIN LCC
MBL8086/-1/-2
MPU 40-PIN DIP

PERIPHERALS

MB8868A
MOS UART (TR1602A COMPATIBLE)
MBL82288
BUS CONTROLLER
MBL82284
CLOCK GENERATOR
MBL82C43
INPUT/OUTPUT EXPANDER (CMOS)
MBL8243
INPUT/OUTPUT EXPANDER
MBL8289
BUS ARBITER
MB89289
BUS ARBITER (CMOS)
MBL8288
BUS CONTROLLER
MB89288
BUS CONTROLLER (CMOS)
MBL8287
BIPOLAR OCTAL BUS TRANSCEIVER
MB89287
BIPOLAR OCTAL BUS TRANSCEIVER (CMOS)
MBL8286
BIPOLAR OCTAL BUS TRANSCEIVER
MB89286
BIPOLAR OCTAL BUS TRANSCEIVER (CMOS)
MB89237A
DMA CONTROLLER (CMOS)
MB89251A
SERIAL DATA TRANSMITTER (CMOS)
MB89254
PROGRAMMABLE INTERVAL TIMER (CMOS)
MB89255A
PARALLEL DATA INPUT/OUTPUT UNIT (CMOS)
MBL8284A
CLOCK GENERATOR & DRIVER
MB89284A
CLOCK GENERATOR & DRIVER (CMOS)
MBL8283
BIPOLAR OCTAL LATCH
MB89283
BIPOLAR OCTAL LATCH (CMOS)
MBL8282
BIPOLAR OCTAL LATCH
MB89282
BIPOLAR OCTAL LATCH (CMOS)
MBL8259A/-2
PROG. INTERRUPT CONTR.
MBL89259A/-2
PROG. INTERRUPT CONTR. (CMOS)
MB88308/9
CMOS OUTPUT EXPANDER
MB88306/7
CMOS OUTPUT EXPANDER
MB88304/5
NMOS 4/8-BIT I/O EXPANDER
MB4107
DATA SEPARATOR
MB1412AC
LS-TTL ERROR CHECKING/ CORRECTION CIRCUIT (ECC)
MB1426
16-BIT ECC

SPECIAL CONTROLLERS (ASIC)

MB8877A
FLOPPY DISK CONTROLLER
MB8876A
FLOPPY DISK FORMATTER
MB89322
CRT CONTROLLER (6845 COMPATIBLE) (CMOS)
MB89321
CRT CONTROLLER (6845 COMPATIBLE) (CMOS)
MB89311
FLOPPY DISK CONTROLLER
MB88303P
TELEVISION DISPLAY CONTROLLER

TELECOM

MB87006
PLL
MB87004
DTMF/PULSE DIALER
MB87003
DTMF/PULSE DIALER
MB87001
SYNTHESIZER SYSTEM BLOCK
MB6024
CODEC
MB6022
CODEC
MB6021
CODEC
MB501/L
TWO MODULUS PRESCALER
MB503/504/506
TWO MODULUS PRESCALER

LINEAR

MB3712
POWER AMP
MB3713
POWER AMP
MB3722
POWER AMP
MB3714A
POWER AMP
MB3737
POWER AMP
MB3730
12W BTL AUDIO AMP
MB3731
18W BTL AUDIO AMP
MB3752
VOLTAGE REGULATOR
MB3759
PULSE WIDTH MODULATION (PWM) CONTROL
MB3760
PWM CONTROL CIRCUIT

DSP (DIGITAL SIGNAL PROCESSORS)

MB8764CR
-001 88-PIN PGA
MB8764CV
-001 84-PIN LCC
MB8764PR
-001 88-PIN PLASTIC PGA
MB87064P
42-PIN PLASTIC DIP
MB87064C
42-PIN CERAMIC DIP
MB87069C
64-PIN CERAMIC PGA

SCSI

MB87030
SYNCHRONOUS S.P.C.
MB89351
ASYNCHRONOUS S.P.C.

CONVERTERS

MB40547
-7/-8 8-BIT UH SPEED A/D
MB40576
6-BIT UH SPEED VIDEO A/D
MB40748
-8/-9 10-BIT UH SPEED D/A
MB40776
6-BIT UH SPEED D/A
MB40778
8-BIT HIGH SPEED D/A
MB40788
10-BIT UH SPEED D/A
MB88301A
6-BIT PWM NMOS D/A
MB4052
4 CHANNEL 8-BIT A/D
MB4053/63
6 CHANNEL 8-BIT A/D SUBSYSTEM
MB4072
8-BIT HIGH SPEED MULTIPLYING D/A

ETHERNET

MB8795
ETHERNET CONTROLLER
MB87012
802.3/ETHERNET CONTROLLER
MB502
MANCHESTER ENCODER/DECODER

CMOS GATE ARRAYS

UH SERIES:
C20000UH
20,160 GATES
UM SERIES:
C15006UM
15,120 GATES + 6K RAM
C10012UM
10,080 GATES + 12K RAM
UHB SERIES:
C12000UHB
12,734 GATES
C8700UHB
8,768 GATES
C6000UHB
6,000 GATES
C4100UHB
4,174 GATES
C3000UHB
3,066 GATES
C2200UHB
2,220 GATES
C1700UHB
1,724 GATES
C1200UHB
1,233 GATES
C830UHB
830 GATES
C530UHB
530 GATES
C330UHB
336 GATES
AV SERIES:
C8000AV
8,000 GATES
C6600AV
6,664 GATES
C5000AV
5,022 GATES
C3900AV
3,900 GATES
C2600AV
2,640 GATES
AVB SERIES:
C2000AVB
2,052 GATES
C1600AVB
1,674 GATES
C1200AVB
1,245 GATES
C850AVB
852 GATES
C540AVB
549 GATES
C350AVB
357 GATES

C4002AVM
4,087 GATES +2K RAM
C2301AVM
2,375 GATES + 1K RAM
C1502AVM
1,564 GATES + 2K RAM

CMOS STANDARD CELLS

AV SERIES:
1.8μ 2-LAYER METAL
16K RAM, 64K ROM, PLAs, REGISTERS
SPECIAL LSI FUNCTIONS
>13K GATES
2 INPUT GATE EQUIVALENT
<1.4ns TYPICAL
<2.2ns WORST CASE
AU SERIES:
1.3μ DUAL-WELL, 2 AND 3 LAYER METAL
32K RAM, 128K ROM, PLAs, REGISTERS, MULTIPLIERS, ALU
STANDARD LSI EQUIVALENT FUNCTIONS
>40K GATES
2 INPUT GATE EQUIVALENT
<0.8ns TYPICAL
<1.3ns WORST CASE

BIPOLAR LSTTL GATE ARRAYS

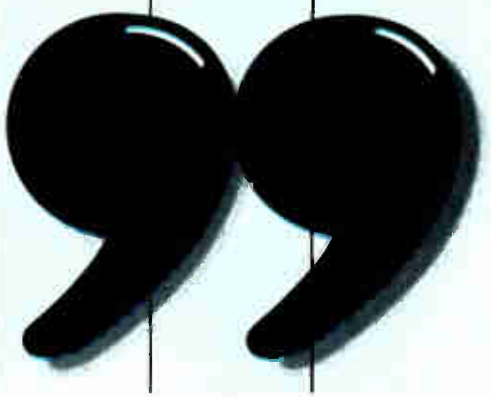
EQUIVALENT GATES (2 INPUT GATES)
B240
360 GATES
B350
540 GATES
B350B
528 GATES
B600
924 GATES
B700B
1,080 GATES
B1100
1,680 GATES
B2000
3,162 GATES

BIPOLAR ECL GATE ARRAYS

EQUIVALENT GATES (2 INPUT GATES)
ET750
1,136 GATES
ET1500
2,192 GATES
ET3000
4,344 GATES
ET4500
6,280 GATES
ET2009
2,640 GATES + 9K RAM
ET3004
3,960 GATES + 4K RAM

PACKAGING

PLASTIC PIN GRID ARRAYS
FLAT PACK GULL WINGS
256-PIN CERAMIC GRID ARRAYS
SMALL OUTLINE J LEADS (SOJ)
PLASTIC ZIG-ZAG IN-LINE (ZIP)
SHRINK DIPs
SKINNY DIPs
SMALL OUTLINE DIPs
SINGLE IN-LINE PACKAGE (SIP)
SINGLE IN-LINE MODULES
PLASTIC GRID ARRAYS (PGA)
CERAMIC GRID ARRAYS (PGA)
PLASTIC LCCs
CERAMIC LCCs
PLASTIC FLAT PACK
CERAMIC FLAT PACK
FLAT PACKS w/ HEAT SINKS
SMALL OUTLINE DIP



Circle 31 on reader service card

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- Time Histograms
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- Second Disk Drive

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Timing Channels	16	16	16	16	16
Maximum Speed:					
Internal clock (async.)	100 MHz	100 MHz	200 MHz	200 MHz	200 MHz
External clock (sync.)	40 MHz	40 MHz	75 MHz	75 MHz	75 MHz
Main & Reference Memories	1000 x 16	1000 x 16	1000 x 16	1000 x 16	1000 x 16
Glitch Capture	5 nsec	5 nsec	3 nsec	3 nsec	3 nsec
State Channels	32	48	48	48	N/A
Maximum Speed	20 MHz	20 MHz	20 MHz	25 MHz	
Main & Reference Memories	1000 x 32	1000 x 48	1000 x 48	1000 x 48	
16 level triggering	✓	✓	✓		
Advanced nonsequential triggering (IF.THEN.ELSE)				✓	
Microprocessor Disassembly	8 bit	8, 16 bit	8, 16 bit	8, 16 bit	
Trigger Linkage	Link to/from State, Timing, Waveform, or External input				
Price	$8900.	$10,900.	$12,900.	$13,900.	$9,900.

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Electronics

MAGNETO-OPTIC MEMORIES BEGIN TO LOOK LIKE A GOOD BET

SIMPLE NIKON TECHNIQUE PERMITS ERASE AND WRITE IN ONE PASS

TOKYO

The race for dominance in the upcoming generation of high-capacity optical memories is heating up, and a flurry of recent activity is moving magneto-optic disks out of the shadow of magnetic disks. Work in the U. S. and Japan aimed at wiping out the major disadvantage of magneto-optic memories—they require two passes to overwrite, one to erase the old data and the other to record—could at last let eager computer designers take advantage of the considerable edge in density that magneto-optic disks have over magnetic memories.

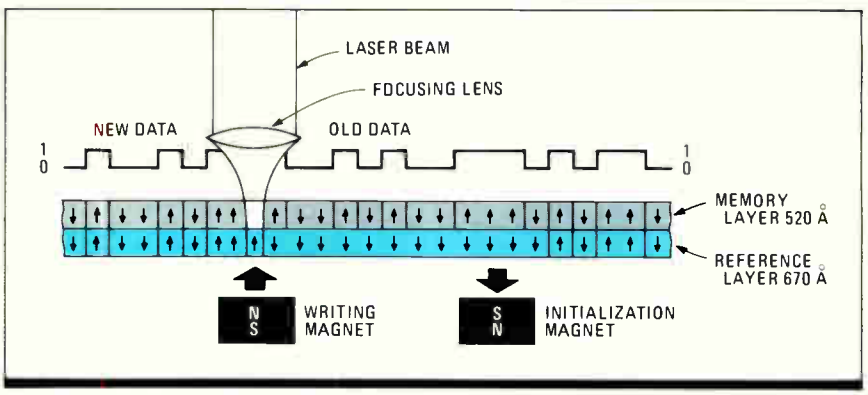
The most recent developments come from Nippon Kogaku K. K., known as Nikon, in Japan; Carnegie Mellon University in Pittsburgh; and IBM Corp. The Carnegie Mellon and IBM techniques require the use of two lasers or of one laser with a split beam. So perhaps the most promising new technique is that of Nikon, a newcomer to the disk-drive business, which has perfected a relatively simple and straightforward one-laser solution.

ONE PASS. Nikon engineers made one-pass writing possible by going to a medium with two thin-film magnetic layers (see diagram). The magnetization of the lower layer, terbium iron cobalt, is repeatedly initialized to a downward reference on each pass. This gets it ready to erase 1s, which are stored as magnetization in the upward direction in the upper layer.

The lower layer has the relatively low coercivity of 3.5 kilo-Oe, permitting it to be magnetized in a single direction by a fixed field of 7 kilo-Oe. The upper layer, terbium iron, is the usual film used for magneto-optic recording. It has the high coercivity of 13 kilo-Oe and thus its magnetization is unaffected by that of the lower film at room temperature.

Immediately before writing starts, a given point on the disk always passes over the initializing magnet that resets the magnetization direction in the reference layer. This point then passes under the laser head, at which position there is a relatively weak field of 200 Oe pointing upward.

The laser may have one of two power levels, 9 mW to write and 5 mW to erase. At the 5-mW power level, only the upper layer reaches its Curie temperature (the point at which a material no longer exhibits ferromagnetic properties) of 140°C. As it cools down, it is magnetized in the zero state by the reference film. At the 9-mW power level, the lower layer passes through its Curie temperature of 200°C. The low field is sufficient to magnetize both films in the upward direction, the 1 state.



PASSING THROUGH. Nikon's system does one-pass erase and write by using a medium with two magnetic layers. The lower layer does the erasing of the 1s stored in the upper layer.

Disks are read at a power level of 1.5 mW. Kerr-effect rotation is 0.3°. Tests show a carrier-to-signal ratio of 54 dB at 1 MHz and 44 dB at 8 MHz. Information density is about one bit/square μm. Experiments were conducted with a track pitch of 1.6 μm and a linear recording density of one bit per 0.84 μm.

In the conventional configuration, an erase head precedes the write head. The track is erased only prior to writing; at all other times the erase laser must be kept off to prevent destruction of data. Moreover, the system must account for the difference in position between the two heads along the track. The Nikon configuration requires no intelligence or control—operation is automatic. The write head has two states, 0 and 1, which is identical with the operation of a magnetic head.

One of the Nikon system's strong points is its compatibility with computer operating systems written for magnetic disks. Development manager Hideki Akasaka's group has developed a magneto-optic disk that looks to a computer's operating system like a magnetic disk with greatly increased capacity. Experimental disks and a drive have been developed at Nikon's Information Storage Products Division; Akasaka says that "it will take two or three years to complete development, check reliability, and start production of a commercial product."

In the meantime, Nikon can expect to see some competition emerge. Indeed, most of Japan's major electronics companies—including Fujitsu, Hitachi, Mitsubishi, NEC, Sanyo, Sharp, and Sony—are working on erasable magneto-optic disks. And Sony says it will begin shipping samples this fall and production units by this time next year.

ALTERATIONS. In the U. S., Carnegie Mellon University researchers have come up with a lab technique based on their discovery that the inherent demagnetizing field can be used to erase and write directly [*Electronics*, Feb. 5, 1987, p. 76]. Altering the magnetic media's formulation with a laser raised the compensation temperature and made possible a read-before-write scheme. Program managers are now talking with commercial licensees.

IBM received a patent March 10 for a technique that is similar to the Carnegie-Mellon system in that the magnetic state is flipped with a laser beam.

–Charles L. Cohen

DESIGN TRICKS SPEED UP INMOS'S SRAMS

COLORADO SPRINGS

Inmos Corp. has done a topsy-turvy act with its fast 256-Kbit static random-access memories that should make possible faster, smaller, and more producible CMOS SRAMs. The trick is the layout of sense amplifiers. Some of the SRAM's MOS circuits are turned around, hooking inputs to sources rather than gates.

The layout resembles techniques normally associated with bipolar circuits, which are current-sensing, rather than MOS, which is voltage-driven. Inmos intends to use the design to avoid speed-hampering capacitance that can crop up on long bit lines with the voltage-sensing technique. Portions of the CMOS memories operate more like emitter-coupled logic, quickly sensing bit lines by reading current rather than voltage differentials.

FASTER. Access times of 18 ns can be accomplished with the 256-Kbit chips because current-sensing circuits quickly detect slight differences in the flow of electrons. With voltage sensing, more time is needed to detect bit-line capacitance, because it takes longer to reach voltage differentials sufficient for sensing. And a simpler clocking mechanism used in current sensing also adds speed, because extra cycles are no longer needed to clear out voltage differentials from lines before the next memory access.

The move to MOS current-sensing circuits also cleans up the circuit design. It enables Inmos to forgo more than a thousand pre-sense amplifiers typically wedged into the pitch between bit lines on a 256-Kbit chip. Normally, these are used to boost differential reading from cells and are placed directly at the end of bit lines to cut capacitance.

Since bits are read internally when using current-differential levels, the length of lines and the amount of capacitance are less critical, notes Ken J. Mobley, one of the principal design engineers for the 256-Kbit fast SRAM. A soon-to-be-announced 64-Kbit-by-4-bit design contains only 32 pre-sense amplifiers instead of the 1,024 that would have been used in a voltage-sensing design. That means the die is smaller by 3,000 mil^2. More important, most of the reduction was made by trimming the width of the 172-by-404-mil chip, making it possible for Inmos to offer it soon in a standard 300-mil-wide plastic dual in-line package.

The 64-Kbit-by-4-bit memory—plus a 256-Kbit-by-1-bit chip and two 64-Kbit SRAMs—will reach market later this year with worst-case access times of 25 ns. Typical access times have been clocked at 18 ns with a 5-V power supply at room temperature. Essential to keeping the resistance low for the current-sensing technique is a new double-level metal 1.2-μm CMOS technology, called Process '86 by Inmos for the year it was first put into pilot production.

"If we had stayed with a single-metal process, we would have had a lot of parasitic resistance, which would have detracted from the ability to perform current sensing," says Larry F. Childs, another principal designer.

MAKING IT. The elimination of the pre-sense amplifiers and the die reduction have also eased manufacturing. "The sense amp in any memory device is absolutely the most sensitive area of a die in terms of process variations," explains Mobley, referring to the difficulty in matching MOS transistors for linear duties. The chips are also going to feature a proprietary sensing circuit that self-generates a reference signal from a bit line rather than use duplicate mirror-reference circuits, which are susceptible to mismatching with each bit line.

To develop the MOS current-sensing circuits, engineers had to reinvent the amp, so to speak, and forget standard voltage-sensing amplifiers used in memories for the past 15 years. "Once you start designing any kind of differential amplifier, you start to worry about all the basic things such as common mode rejection and differential gain," says Mobley in explaining the departure from common memory-layout practices.

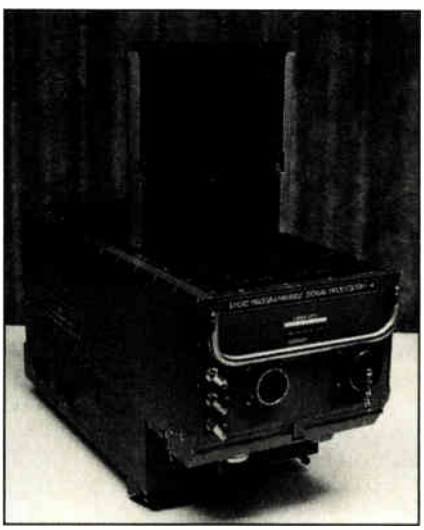
"The normal voltage-sensing technique, which is well understood, fixes the source of two transistors at an identical voltage and then applies an input signal to the gate. Because gates of MOS circuits are by nature high-impedance devices, they are strictly capacitive and there is no current flow into the input," Mobley says. "We have turned that around and fixed the gates of two input devices at an identical potential, which is generated through a reference path. The inputs are made to the sources." A difference in gate-source voltage still exists, but current flows through the inputs, and there is a dc path to the amplifiers.

–J. Robert Lineback

A BILLION-DOLLAR PROGRAM EXCITES THE INDUSTRY

LOS ANGELES

A new procurement is exciting the military electronics industry. Not only is it the only big avionics program around in a period of tight budgets, but it is the first major military project to specify the use of Very High Speed Integrated Circuits from the start, and it is a departure from the customary contracting procedures.



VHSIC BOX. Westinghouse's entry in the competition for the VHSIC-loaded ATF radar.

The procurement is the programmable signal processor for the Air Force's Advanced Tactical Fighter. It's a dedicated computer that will serve the aircraft's multiple sensors, mainly radar. As decision time nears, the competitors are three heavyweight companies, one a relative newcomer to the radar business. And not only is the program worth upwards of $1 billion through the next decade, it also is being watched for clues to the changes in procurement and design that VHSIC creates.

One apparent difference is that the project is drawing new players. For the ATF processor, IBM Corp.'s Federal Systems Division is competing with the two major producers of military radar, GMHE/Hughes Aircraft Co. and Westinghouse Corp. The radar competition is a natural battleground because most of the VHSIC Phase 1 chips, from six contractors, are aimed at better signal processing. Also, where processing tasks and front-end functions ordinarily are bundled in the same system, VHSIC capability permits them to be split to boost performance.

All three will submit their final proposals before the end of April to both potential prime-contractor teams: Lockheed and Boeing-General Dynamics, and Northrop and McDonnell Douglas. Each prime contractor will pick a processor subcontractor and begin development by late summer. This is uncommonly fast for military work, one of VHSIC's goals. Ultimately, the winner is to be chosen after a flyoff some five years from now. Under the old system, one prime contractor would already have been selected.

Although the Air Force and the two prime-contractor teams are not divulging details about the processor, enough is known to understand general structural and performance goals. A major advance appears to be an architecture of common modules that will best support design flexibility and device improvements as they occur. This "building block" approach, long sought by military planners but held back by lagging military semiconductor work, is made possible by the density of VHSIC Phase 1 chips that replace many component boards and have clock speeds up to 50 MHz. To support the multiple sensors, the system must perform up to 100 million complex operations per second (COPS), about 10 times faster than current operational processors.

Hughes, Westinghouse are upgrading existing processors

The three contenders will take somewhat different approaches, but Hughes and Westinghouse closely follow processor improvements that both have in the works. IBM's design is based on 13 new 1-μm Phase 1 chips being developed for ATF, says Robert Estrada, VHSIC program manager at the IBM Federal Systems Division in Manassas, Va.

Hughes already has started low-rate production on a unit for other craft that uses 1.5-μm CMOS gate arrays with 10-Kbit gate-complexity levels in a parallel-processing scheme. Though these arrays are not yet qualified to VHSIC standards, Hughes expects them to pass muster before the end of 1988, says Milton E. Radant, vice president and director of technology of the Radar Systems Group in El Segundo, Calif. The processor, which Hughes calls its fourth generation, has a computational core shrunk to one third that of the previous generation; signal-processing speed is 40 million COPS, up from 7 million. Reliability is put at 750 hours mean time between failures, up from 460 hours.

For the ATF, Radant says, Hughes cuts the size of the processing element once again by two thirds and doubles the speed. Its proposal has three basic module types. The Hughes group already has next-generation hardware well along in the lab, using available VHSIC devices and working toward the 100-million-COPS goal. It will be at the demonstration stage by late next year.

Westinghouse is building a VHSIC-based programmable signal processor for the F-16 fighter. The processor is to reduce the number of boards from 31 to 14, increase performance from 16 million to 40 million COPS, and lower the power requirement from 2,948 W to 725 W. Westinghouse expects to have the go-ahead by late this year. *–Larry Waller*

ARTIFICIAL INTELLIGENCE

PROCESSOR LINKS NUMBER CRUNCHING AND SYMBOLICS

ANAHEIM, CALIF.

A new startup has produced a fast 40-bit inference machine that links conventional number crunching with the kind of symbolic processing typically used in artificial intelligence. Integrated Inference Machines Inc. has just delivered its first production unit to the National Aeronautics and Space Administration, and in so doing becomes a standard bearer for the combinational approach that some observers believe is the next wave of symbolic processing.

The company joins the field at a time when the makers of symbolic processors—including Lisp Machine Inc., which has filed for Chapter XI protection from its creditors (see p. 110), and Symbolics Inc.—are finding it tough to increase sales and profits. But Robert T. Wang, president and founder of Integrated Inference Machines, is undaunted. He believes the promise of symbolic processors will be realized as integrated coprocessors in systems, not in standalone computers.

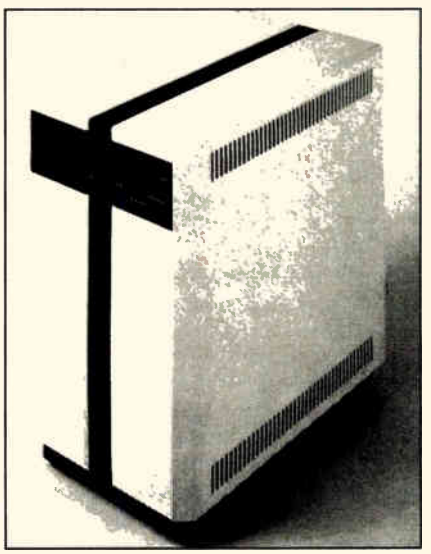
The Anaheim company's strategy is to build a high-performance, low-cost symbolic processor that is tied to a numeric accelerator and a general-purpose computer and that readily runs multiple symbolic processing languages. The price for its SM45000 will be $39,000 to $44,500, and the company claims the machine runs 1.3 to 8 times faster than current symbolic computers, such as the $50,000 to $80,000 Symbolics 3600.

Clearly, airborne and space-borne applications will require high levels of intelligent symbolic processing plus fast numeric computation, which is one reason why the company's first unit went to NASA's Ames Research Center in Mountain View, Calif. NASA plans to use the machine as an experimental prototype for space-borne computers for the proposed U. S. space station and the national aerospace plane. In addition, NASA will use the SM45000 for software development in a joint project with the British Aerospace Agency.

The trend toward combining number crunching and symbolics is unmistakable in other applications as well. Wherever rapid analysis and decision making are required in fast-moving control situations, a very fast reasoning computer or inference engine must work with fast number crunching to augment human decision and reaction. Other companies are working in this direction, including Texas Instruments Inc.

TAGGING WORDS. The symbolic processor in the SM45000 was designed for fast response. The architecture that works best for symbolic processing is called a tagged architecture, since tags are attached to each word to characterize them. Most current Lisp machines are 32-bit machines with the tag included in the 32 bits. But the SM45000 has 40-bit words—32 bits with an 8-bit tag. The engineers at Integrated Inference Machines developed proprietary high-speed hardware for tag decoding, which helped them make such a fast machine.

This performance is just from the symbolic part of the machine. The SM45000 also has a mathematics accelerator option that does numeric processing at the rate of 4 million floating-point operations per second, and an enhancement is on the way to increase that to 8 megaflops. In addition, the design incorporates an Intel 80286 processor that han-



TOGETHER. Inference machine combines number crunching with symbolic processing.

dles all input/output, including file storage. The file system is compatible with the PC DOS file system used in IBM Corp. Personal Computers and compatibles. This means that PC files can be loaded into the machine and that, conversely, the SM45000 can generate files that can be loaded into a PC.

Also making the machine ideal for real-time embedded work is the availability of large amounts of memory at a low price. This means that real-time applications will not be slowed by swapping chunks of programs between disk drives and main memory—big chunks or even whole programs will fit into the large memory. The machine supports a linear address space for a virtual memory of 4 billion words, 20 gigabytes. The basic machine comes with 10 or 20 Mbytes of real memory with expansion slots for up to 240 Mbytes.

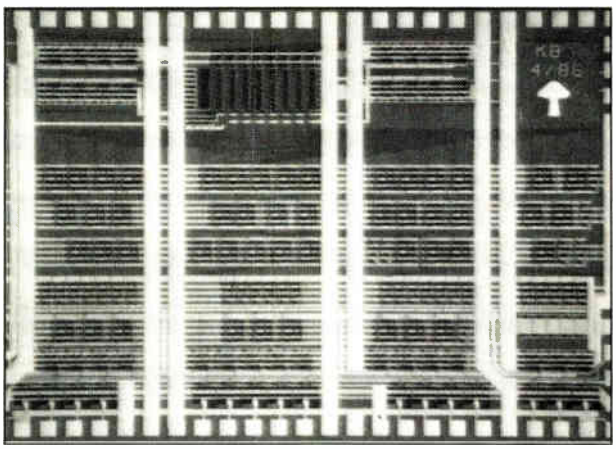
The SM45000 symbolic process runs an extended version of Common Lisp, and a Prolog language will be available next month. The I/O processor and numeric accelerator support standard languages. And the low price of the machine should keep the integration trend rolling along. *–Tom Manuel*

INTEGRATED CIRCUITS

A FASTER GaAs CHIP NEARS PRODUCTION

BLOOMINGTON, MINN.

Digital integrated circuits based on gallium arsenide modulation-doped field-effect transistors are moving rapidly toward commercial density levels. Honeywell Inc. has developed a chip with 1,350 gates—the densest GaAs MOD FET logic circuit ever built. This technology is very significant in that it is seen by many as the heir apparent to today's production GaAs ICs based on metal-semiconductor FET processes. This is because they are faster and show less leakage. MOD FETs are a kind of HEMT (high-electron-mobility transistor).



RECORD SETTER. Honeywell's 1,350-gate 8-by-8-bit parallel multiplier is densest GaAs MOD FET logic circuit to date.

The Pentagon's Defense Advanced Research Projects Agency is also jumping on the bandwagon. On March 30, the agency awarded a contract to a team headed by AT&T Bell Laboratories to develop a pilot line for digital chips that is based on ultrafast heterostructure-based GaAs technology (see "Bell labs to set up pilot line for Pentagon").

The Honeywell chip is an 8-by-8-bit pipelined parallel multiplier that was built in Honeywell's 1-μm aluminum gallium arsenide/GaAs heterostructure technology with self-aligned gates [*Electronics Week*, May 13, 1985, p. 19]. "This is the biggest MOD FET logic circuit we've ever seen reported or talked about," says Nicholas C. Cirillo Jr., who heads GaAs work at the Honeywell Physical Sciences Center in Bloomington.

SPEEDY. Honeywell was able to break the 1,000-gate barrier without making any sacrifices in speed. The circuit also exhibits the shortest room-temperature propagation delays of any working chip in any technology. Gate propagation delay at room temperature is 70 ps per gate, and power dissipation on the chip built came in at 1.4 mW per gate. All gates were built using direct-coupled FET gate logic.

The complexity record for a MOD FET logic circuit was held by Fujitsu Ltd., which in February 1986 reported an 8-by-8-bit parallel multiplier that integrated 970 gates and exhibited room-temperature propagation delays of 245 ps per gate, at about 6 mW/gate. Before that, Honeywell's 370-gate, 5-by-5-bit parallel multiplier was the speed king, with delays of 73 ps/gate. So at 70 ps, the latest device is comparable in speed, but the device is nearly quadruple the complexity of its predecessor.

On the memory side, Fujitsu has already reported on a fully functional 1-Kbit static random-access memory chip that is based on HEMT structures that integrate 7,244 transistors, and others, including AT&T Bell Laboratories, Hughes, McDonnell Douglas, Rockwell, and NTT, are also working in the field.

Unlike MES FETs, in which channels are formed in a GaAs substrate by ion implantation, MOD FET channel structures are grown by use of molecular-beam epitaxy or by use of metal-organic chemical vapor deposition. This means that in a MOD FET structure, electrons can be made to flow in a pure, undoped GaAs buffer layer, unimpeded by the dopant atoms that can lead to electron

BELL LABS SETTING UP GaAs MOD FET PILOT LINE

Honeywell Inc. isn't the only one interested in pushing gallium arsenide modulation-doped field-effect transistor ICs out of the lab and into production. The Pentagon's Defense Advanced Research Projects Agency is giving the technology a shove with a four-year, $19.8 million contract awarded late last month to AT&T Bell Laboratories. Hughes Aircraft Co. and McDonnell-Douglas Corp. are subcontractors.

The DARPA deal calls for Bell Labs to develop a pilot line for heterostructure-based AlGaAs/GaAs ICs that can turn out 100 wafers per week within three years, says Robert C. Vehse, program manager for the contract at Bell Labs' Compound Semiconductor Integrated Circuit Laboratory in Reading, Pa. The contract calls for the design of six digital logic ICs, each with between 3,000 and 5,000 gates, which will be built in Bell Labs' submicron SDHT process (for selectively doped heterojunction transistor). Bell Labs is also to develop a 4-Kbit static random-access memory using the SDHT process.

The six logic chips are aimed at digital-signal-processing applications, Vehse says. Two will be custom devices; the others will be based on standard-cell technology. Two of the standard-cell chips will be designed by Hughes, which will also be responsible for developing computer-aided design tools. McDonnell-Douglas will provide testing and analysis of the chips' radiation hardening.

The pilot line will use molecular-beam epitaxy and will begin operation by July, Vehse says. A second pilot line will also be established by Hughes in El Segundo, Calif. Besides the initial $19.8 million, the contract also contains a DARPA option worth an additional $10 million that would aim at even more advanced circuits based on AlGaAs/GaAs superlattice quantum-well structures, Vehse notes. *–Wesley R. Iversen*

scattering in MES FET channels. Also, because of the higher Schottky barriers that result from putting the gates in an AlGaAs layer, MOD FETs exhibit much less leakage than MES FETs.

The result, says Cirillo, is the potential for circuits about twice as fast as today's MES FET ICs, and with four to five times higher noise margins. That translates into four to five times higher integration levels.

Honeywell pulled out of the merchant GaAs IC business last year, closing down its MES FET digital-circuit production line in Richardson, Texas [*Electronics*, Dec. 18, 1986, p. 21]. But the company is continuing GaAs efforts with an eye toward meeting internal and possible future merchant-market needs.

"True production of MOD FET ICs across the industry, I think, is two to three years away, barring a major technology breakthrough in the use of metal-organic chemical vapor deposition to grow wafers," Cirillo says. In the meantime, Honeywell will continue to work on problems associated with molecular-beam-epitaxy approaches to growing MOD FET structures, he says, such as material-defect density and throughput.

Honeywell plans eventually to use the same 1-μm self-aligned process for production that it used for the demonstration 8-by-8 multiplier, Cirillo says. The company will continue to push device complexity with the process, and it has plans to build additional developmental chips, including an 8-by-8 multiplier/accumulator at about 2,300 gates, followed by a 16-by-16 multiplier/accumulator that will integrate more than 4,000 gates. *–Wesley R. Iversen*

CONSUMER

FMX IS THE SOUND OF A NEW MARKET

BLOOMINGTON HILLS, MICH.

FM stereo broadcasting is headed for its first major improvement since it was adopted in 1961. Delivery of a final specification for the FMX Extended Range Stereo System is now expected by mid-May, an upgrade that would significantly reduce noise and extend the reception area up to four times. FMX now appears headed for commercial reality. And at least two semiconductor manufacturers plan to capitalize on it.

About 30 million FM stereo receivers are sold annually in the U.S., all eventual candidates for FMX chips. But the initial target of the two manufacturers—Sanyo Semiconductor Corp. of Santa Clara, Calif., and Sprague Electric Co.'s Semiconductor Group in Worcester, Mass.—is the auto market, which accounts for about half the U.S. radio sales.

Both are developing single-chip receiver-decoder circuits for the proposed FMX system. Sanyo plans first samples as soon as late May, with production quantities for less than $2 each by October, says Aki Goto, executive vice president. Sprague is taking a more conservative approach. "We'll have samples by the end of this year or early next year, and if there's interest from customers, we could gear up for production by late 1988," says Robert F. Milewski, linear products manager at Sprague. The Sprague chip will integrate linear and digital BiMOS circuitry and will be a medium-scale circuit of about 15,000 mil^2, Milewski says.

The patented FMX technique was developed jointly by CBS and the National Association of Broadcasters [*Electronics*, June 17, 1985, p. 18]. It uses a unique compressor/expander system in which the compressor works with an adaptive expander in a receiver that can conform to any transmitted compression curve. Conventional expanders must be carefully tuned to a set compression ratio.

Though the drive to commercialize the technology was stalled by the closing of the CBS Technology Center in Stamford, Conn., last September, it gained new impetus April 1 with formation of a partnership backed by Detroit-area investors to complete FMX development and handle licensing. The partnership, Broadcast Technology Partners, is based in Bloomington Hills, Mich.

CBS and NAB sponsored the first successful field tests of FMX more than two years ago. But the closing of the CBS center prevented the delivery of a final specification, says Emil Torick, coinventor of the system and former vice president at the center. CBS has permitted Torick, president of the new partnership, to set up shop with his FMX team in another CBS facility in Greenwich, Conn. He expects to deliver the final FMX specs within weeks.

TORICK: Most U.S. stations will be broadcasting in FMX in two to three years.

Sanyo and Sprague aren't the only ones waiting for that document. "We've got four manufacturers of FM broadcast equipment just waiting for us to give them the go-ahead," Torick says. If all goes as planned, commercial FMX broadcast equipment could be available by this fall, and FMX stations could be on the air by late 1987, Torick notes. The first receivers based on the new FMX chips could be available early next year, he adds.

Broadcast Technology Partners plans to license receiver and broadcast equipment manufacturers for a nominal fee and then reap royalties on hardware sold. Partnership officials won't provide financial details, but Brown says the group hopes to break even on its investment in two to three years. The partnership will initially pursue the U.S. market, where no Federal Communications Commission rule change is required to implement FMX. It is compatible with existing FM stereo, Brown says.

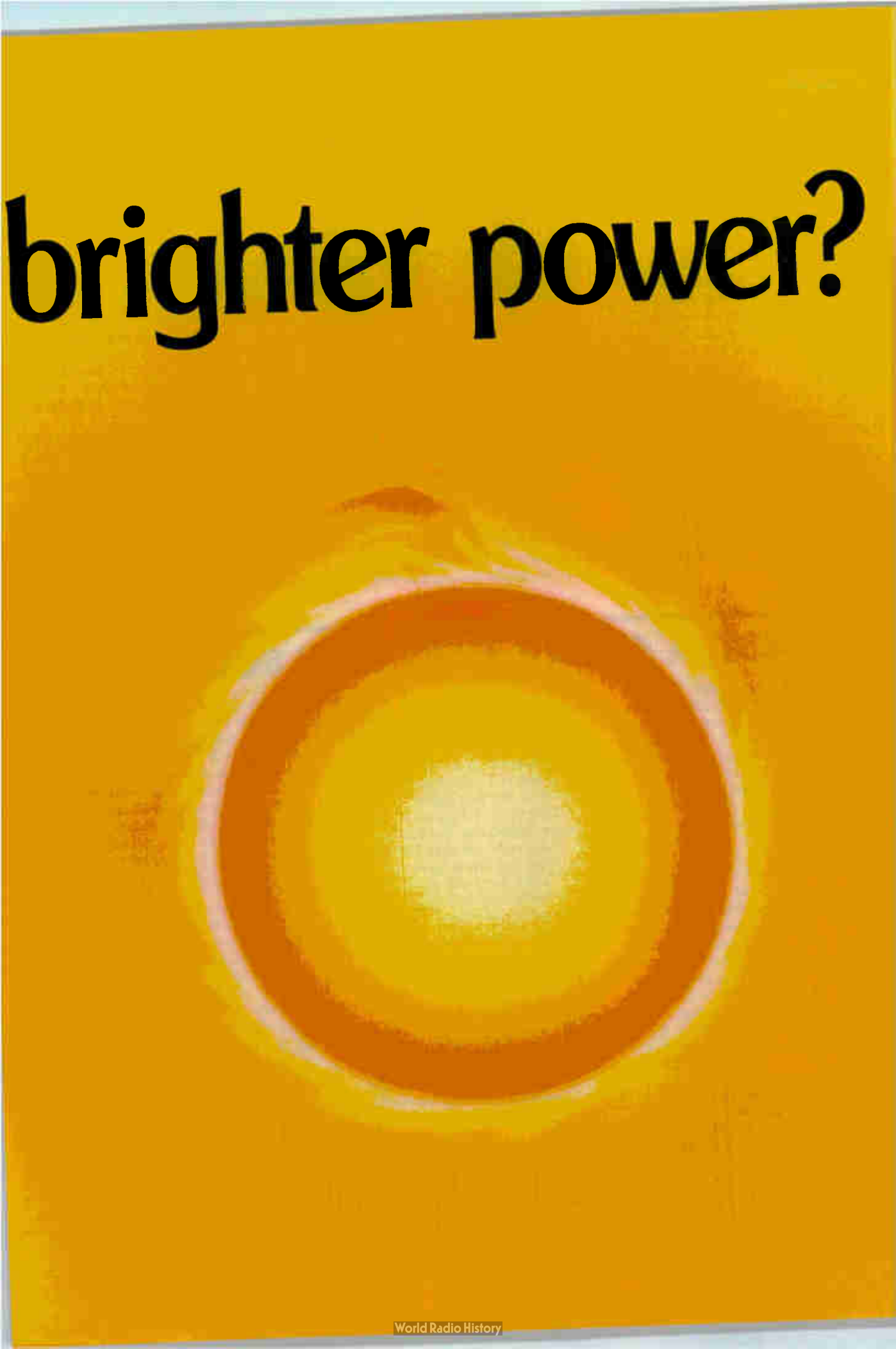
BANDWAGON. The FMX chips from Sanyo and Sprague are designed to replace the existing stereo-decoder circuit in FM receivers and will receive FMX as well as conventional FM stereo broadcast signals. Though only about a half dozen FM stations have so far tested prototype equipment, Sprague and Sanyo are hoping for a rapid commercial FMX deployment by broadcasters and that FM-receiver manufacturers will jump quickly on the FMX bandwagon.

Torick predicts that most U.S. FM stations will be broadcasting in FMX in two to three years, given the improvement offered and the relatively low entry price. Torick likewise believes that FMX-receiver chip sales could hit 1 million units within one year of production availability. Within five years, he adds, "I expect we'll see the majority of receivers being FMX equipped."

Given those kind of prospects, Sanyo and Sprague could see some competition as the FMX market develops. "I think in the near future, others might be getting into this," says Sanyo's Goto. In high volume quantities, the new FMX receiver circuits are expected to sell for about $1 each, compared with about 50 to 75 cents for today's conventional FM stereo decoder circuits. *–Wesley R. Iversen*

Which is the

brighter power?



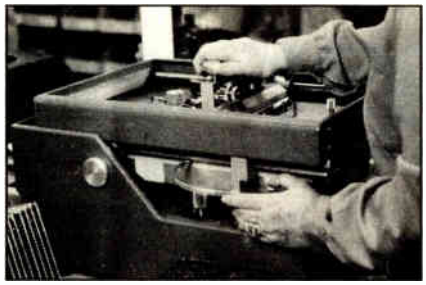
PRODUCTION

AUTOMATING A PC-BOARD HOLE-MASKING PROCESS

HAVERHILL, UK

The people at Philips Radio Communications Systems Ltd. were having problems spot-masking printed-circuit boards for mobile radio equipment at their Haverhill factory in the UK. Most of the components were assembled, inserted, and soldered automatically, but trouble started when the boards were masked for secondary components that would be added later: the work had to be done by hand to keep holes from filling with solder.

This meant the mask had to be positioned very accurately so that it did not overlap nearby pads. For small holes, the solder resist had to completely block the hole, with the area around large holes accurately covered by a ring of resist. The operator also had to work to a pattern of hole masking that was often very complex and varied from one board to another.



FAST MASKS. Philips and its allies have found a way to automate spot masking.

The procedure was time-consuming and prone to errors. So a research project was set up involving Philips; Kenco Ltd. of Chatham, which makes masking paste; and DEK Printing Machines Ltd. of Weymouth. They came up with a semiautomatic system, including a new, accurate water-resistant solder resist, that can handle several hundred boards a week of up to 20 different types. Masking time for each board was reduced considerably—for example, a 200-hole board that took 5 to 6 minutes by hand can be done in 20 seconds by the automated method—and errors virtually disappeared. The system is available commercially from Philips.

Philips and its partners decided to develop their technique so that it would run on Philips' DEK 240 screen-printing machine. But Kenco's Aqua-strip resist, developed for hand masking, ran into problems when used with automatic machines. Viscosity and drying had to be carefully controlled. Being water-soluble, the resist was sensitive to changes in humidity. Kenco managed to retard the resist's evaporation rate and adjust the water content.

A polyester screen with 100 strands per inch was found to be best. It was placed across the frame at a 45° angle and given an emulsion coating of 100 to 300 μm, depending on the thickness of the mask required. The modified paste could then be printed without difficulty. DEK produced a number of different screens to suit the different boards used by Philips. *–Steve Rogerson*

SOLAR CELLS

AT LAST, A CHEAP, EFFICIENT SOLAR CELL

ERLANGEN, WEST GERMANY

The twin thrusts of solar-cell development have been toward lower price and greater efficiency—and usually they have been mutually exclusive. But now researchers in West Germany have taken both routes and come up with a two-sided silicon cell that is both efficient and inexpensive to make.

The researchers, at the University of Erlangen-Nürnberg, believe their experimental devices have pushed solar cells a big step closer to economically viable photovoltaic energy conversion by achieving efficiencies up to 24%. Their goal is 30%; today's one-sided silicon cells are in the 14% range. Though 20% has been achieved before, getting there required costly materials such as gallium arsenide, expensive processing, or elaborate concentrators that focus light onto the cells' surface.

The key to the high efficiency that Konstanze Jäger and Rudolf Hezel have achieved at the university's Institute for Materials Research in Erlangen is true double-faced construction. Light hits not only the cell's front, but also is reflected onto the specially prepared back surface. Thus, depending on the background, the cell's efficiency is 15% on its front and 13% to 14% on its rear surface. The two values do not exactly add up but amount to 20% to 24% depending on how the cell is positioned.

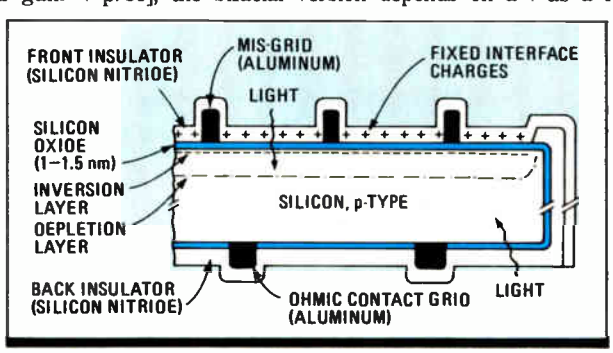
The difference between the Erlangen bifacial cell and others developed elsewhere is in the fabrication. The others use elaborate and expensive high-temperature techniques; the Erlangen process is a simple one that involves very thin silicon and low-temperature doping steps. Hezel, the head of the Semiconductor Technology and Photovoltaic Research Group, will discuss it at the 19th IEEE Photovoltaic Specialists Conference in New Orleans, May 4-8.

Like a one-sided cell developed earlier at Erlangen [*Electronics*, Aug. 7, 1986, p. 38], the bifacial version depends on a silicon-nitride inversion layer for its operation. But it uses a single- or polycrystalline silicon substrate so thin that the finished cell is only 50 to 80 μm thick, five to eight times thinner than the earlier cell.

The cell's rear side is passivated with a silicon nitride insulator film that limits the recombination of charge carriers. This permits the light incident on that side to be used for the photovoltaic conversion at only 10% less efficiency than that obtained at the front. The transparent film serves as an antireflection layer and also guards the cell against foreign matter, particularly moisture.

The contribution of the rear surface, Jäger explains, depends on the background's reflection capacity, measured as a ratio of the backscattered light to the light perpendicularly hitting the surface. For both snow and clouds, she says, the value is up to 0.9, for chalk it is 0.85, and for water the ratio can reach 0.7.

The cell's thinness has several advantages, Hezel says. It uses less silicon and is lighter—a big plus for solar panels in space. Also, the cell's operating temperature is reduced, and therefore its efficiency increased, because the sunlight's infrared components go through the cell without being absorbed. *–John Gosch*



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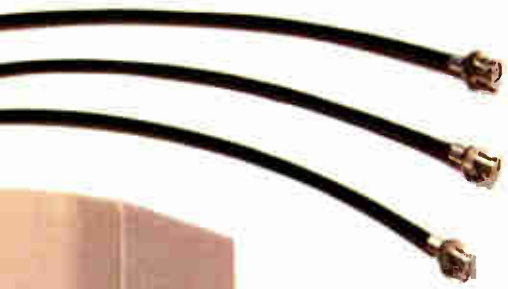

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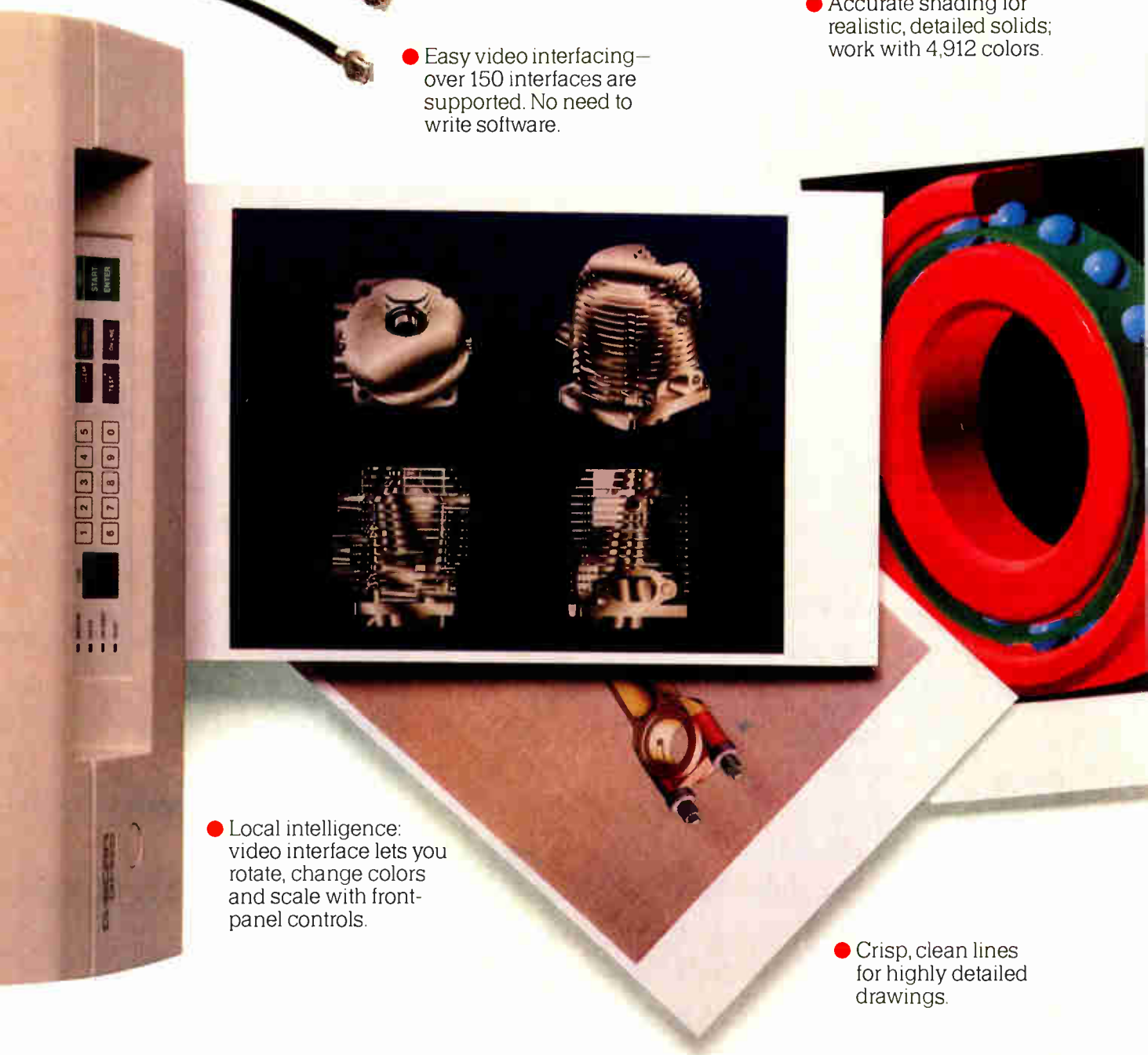

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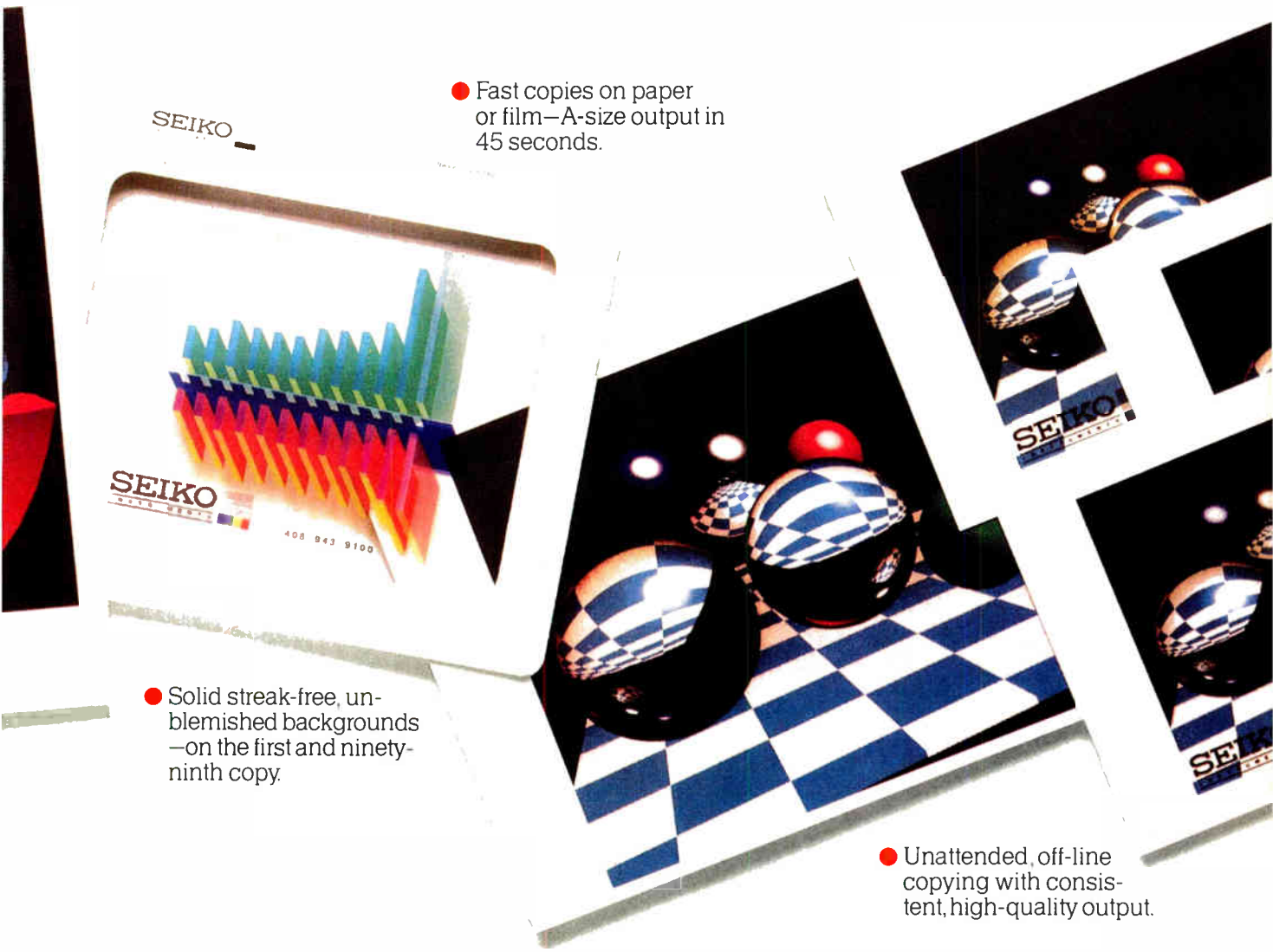
SEIKO INSTRUMENTS



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PROBING THE NEWS

WHY IBM'S NEW PS LINE IS GOOD NEWS TO THE INDUSTRY

IT DOESN'T CLOSE PC MARKET, OPENS UP NEW BUSINESS, AND WILL BE LATE

by Tobias Naegele and Jeremy Young

NEW YORK

For months, April 2 was circled in red on most computer industry calendars. That was widely expected to be Introduction Day for IBM Corp.'s new line of personal computers. Rumors ran wild before the announcement that the Armonk giant was going to move from an open to a closed system. The new machines were going to be clone-killers, difficult if not impossible for other manufacturers to copy. And there was plenty of speculation that IBM would bring out a proprietary operating system that would both stymie competition and ultimately cut Microsoft Inc.—supplier of PC-DOS, the PC operating system—out of the picture.

But IBM's new Personal System/2 ends up being mostly good news for the electronics industry. Most important, the new line will effectively keep the huge PC market wide open for competition. It should also generate several new submarkets. The computer industry was also happy because it sees the computer giant primarily targeting Fortune 1,000 companies and concentrating less on the personal and small business markets. On top of that, IBM is not being very aggressive either on prices or delivery schedules. It will be July before the high-end 386-based system is shipped, and the operating system that puts its power to use won't arrive until early next year. Pricing starts at $1,600, a far cry from the less than $1,000 now being charged for many PC clones.

While parts of the new machines will call for some fast engineering before copies can be built, the obstacles do not appear to be insurmountable. Both operating systems for the new machines, PC DOS 3.3 and the new multitasking OS/2, are from Microsoft, which can sell them to all comers. Even under OS/2, the new machines will run programs written for PC-DOS, so users of the old PCs can bring their old software to the new machines, a big advantage from their point of view.

GRAPHIC IMPACT. The feature that promises to have the broadest impact is a combination of built-in graphics hardware and a graphics-based user interface based on Microsoft's Windows software. Together, IBM and Microsoft have set a new graphics standard for personal computers that takes on Apple Computer's Macintosh in terms of functionality and wipes away the confusion that plagued earlier generations of IBM PC graphics. Software houses can now focus their efforts on the new standard, and the result is likely to be a large body of programs as easy to use as Macintosh software.

At the same time, the graphics hardware, called VGA, for video graphics array, is going to make chip manufacturers and board-level subsystem builders scramble. Clone-builders will need VGA-compatible chips; owners of PC ATs and AT clones will want VGA-compatible cards so they can run software written for OS/2 at the same level of resolution, 640 by 480 pixels. Markets for both chips and boards will develop rapidly.

All four models of the Personal System/2 (see chart) have built-in 640-by-480-pixel graphics, although the low-end Model 30 has a watered-down version with only two-color capability. Nor does it share the new expansion bus IBM has developed: the 32/16-bit Micro Channel, used in Models 40, 50, and 80. All four machines, however, move to 3½-in floppy-disk drives similar to those in IBM's Convertible portable computer.

The new line spans a broad range of performance. The various models make use of three different Intel microprocessors and offer hard-disk drives from 20 to 115 Mbytes in size. The Model 30 is built around an 8-MHz 8086 and has a 20-Mbyte hard disk; Models 40 and 50 are based on 10-MHz 80286s and a choice of hard-disk drives; and the Model 80 sports either a 16- or a 20-MHz 80386 processor to cap the power spectrum. All are available now except the Model 80, due for shipment in July.

However, the full potential of the 286- and 386-based machines will not be unleashed until early next year, when IBM delivers the multitasking OS/2 operating system. OS/2 allows the 286 and 386 to run in the more powerful protected mode, in which they can address a full 16 Mbytes of memory. OS/2 also brings into full play the new graphics interface, which will be bundled into it as the Windows Presentation Manager.

So users will not see the full benefits of either the powerful microprocessors or the graphics environment until OS/2 and applications software written for it hit the market. That gives the mak-

IBM DEFINES A NEW WORLD FOR THE PC INDUSTRY

	Microprocessor (clock rate)	Potential system throughput	Standard memory: Expandable to (Mbytes)	Floppy disk size: Capacity (Mbytes)	Available hard disk drives (Mbytes)	Operating system(s)	Base price (without monitor)
Model 30	8086 (8 MHz)	up to 2½ times PC XT	0.640 / —	3½" / 0.720	20	PC DOS 3.3	$1,695
Model 50	80286 (10 MHz)	up to 2 times PC AT	1 / 7	3½" / 1.44	20	PC DOS 3.3, OS/2	$3,595
Model 60	80286 (10 MHz)	up to 2 times PC AT	1 / 15	3½" / 1.44	44, 70, 115	PC DOS 3.3, OS/2	$5,295
Model 80	80386 (16 or 20 MHz)	up to 3½ times PC AT	up to 2 / 16	3½" / 1.44	44, 70, 115	PC DOS 3.3, OS/2	$6,995
PC AT	80286 (8 MHz)	—	0.256 / 0.512	5¼" / 1.2	20	PC DOS 3.0, 3.1, 3.2, 3.3, OS/2	$4,595

SOURCE IBM CORP

ers of compatible systems plenty of time to come up with competitive hardware.

Makers of IBM-compatible PCs feel that IBM has left them a lot of room to move. Among other things, they point out that IBM's lineup ignores the low end of the market, abandoning that segment to the companies that serve it best—the clones.

"I don't see anything that could be considered a 'clone killer,'" says Tandy Corp.'s Ed Juge, director of market planning at the Fort Worth, Texas, company. Michael Dell, chairman and founder of PC's Limited, a division of Dell Computer Corp. in Austin, Texas, says his company will produce PCs using IBM's Micro Channel bus architecture and VGA graphics within just nine months—roughly the time it will take for IBM and Microsoft to ready OS/2.

HIGH END. Model 80, shown with a 16-in. display and an external 5¼-in. floppy-disk drive, tops IBM's Personal System/2 line.

"We were not surprised by anything we saw," says Mike Swavely, vice president for marketing at Compaq Computer Inc., by far the most successful builder of compatible hardware. "But we were surprised that IBM was not more aggressive in terms of pricing or performance of the product they introduced. I might also add that they were not very aggressive in terms of a delivery schedule."

The makers of compatible systems won't be the only ones burning the midnight oil. Vendors who make add-on boards for PCs, particularly those that specialize in graphics subsystems, are going to be working overtime to adapt to IBM's new world.

The new IBM products have made this expansion-board market a whole new ball game, says Kimball Brown, a computer analyst at Dataquest Inc. in San Jose, Calif. "The whole idea is to get OS/2 to run on current cards of 80286 and 80386 boxes," he says. "As they sit, they will not run OS/2." There are two ways to do this, he says: hardware vendors will try to tweak their boards for the VGA standard, while software companies will try to write programs compatible with Windows 2.0 and the Windows Presentation Manager.

Eager as they are, board and system makers may not be able to get to work right away. IBM is not making hardware manuals for the new systems available until mid-May, and the full specification for the Micro Channel bus will not be forthcoming until August. Board makers will have to wait for this information, says Howard Charney, engineering vice president of 3Com Corp., Mountain View, Calif., which makes Ethernet cards for IBM PCs. They will also have to wait for new chips, he points out.

Notably, companies that had been using standard graphics controllers on their boards are likely to find themselves searching for new parts that allow them to emulate the VGA. "I think the graphics improvements and enhancements over the EGA [Enhanced Graphics Adaptor] will prove to be a killer in the graphics controller market," says Ahmed Nawaz, graphics chip marketing manager for Texas Instruments Inc., Houston. "The flexibility and programmability of the new IBM machines will mean death to the hardwired controllers as users move beyond the EGA."

Competition will be fierce in the rush to respond to IBM. Paradise Systems Inc., San Francisco, says it will have a single-chip video controller compatible with VGA within 90 days. The stakes are high: Dataquest's Brown says that if a company like Paradise can make a VGA look-alike, "they could be a $100 million company in a year."

Additional reporting by J. Robert Lineback and Clifford Barney

MICROSOFT PULLS ANOTHER WINNER OUT OF THE HAT

Reports that IBM Corp. would be abandoning Microsoft Corp. have been greatly exaggerated. IBM's dependence upon the Redmond, Wash., company for basic software for its new Personal Systems is greater than ever. Microsoft assured its position as a leading microcomputer software company when it provided the operating system to IBM for the first IBM PC back in 1981. The subsequent success of the IBM PC established the operating system IBM PC-DOS and the MS-DOS version offered by Microsoft as the industry standard.

The latest announcements from Microsoft and IBM clearly establish a close and enduring relationship between the two companies. The system software offerings cement Microsoft's standard-bearer role in microcomputer operating software. Microsoft is now not just supplying the PC-DOS and OS/2 operating systems for the Personal System/2 products, but also the user interface and basic graphics software.

OS/2 is a "very full-blown" multitasking operating system supporting shared memory, threads, queues, and advanced scheduling, says Bill Gates, chairman of Microsoft. It takes up at least 400 Kbytes of memory, calling for a system memory of at least 2 Mbytes, preferably four. An application written for the MS-DOS environment can run as one of OS/2's tasks. "OS/2 is the biggest piece of work we've ever done," says Gates.

The Microsoft Windows Presentation Manager is included as part of OS/2, which both IBM and Microsoft will be offering. This will firmly establish the new Windows and its graphics services as the user interface and graphics standards for the next generation of single-user microcomputers. OS/2 and the Windows Presentation Manager were developed under a joint development agreement between Microsoft and IBM that began in 1985.

IBM's adoption of OS/2 alone would have been big news for Microsoft. But its endorsement of the Microsoft's Windows system in its second-generation form as the Presentation Manager is an even bigger boost. The inclusion of the Presentation Manager as an integral part of OS/2 virtually assures its status as an industry standard. IBM and Microsoft will use the Presentation Manager for their applications; third-party applications-software vendors are unlikely to try to buck that trend.

"From a hardware point of view, they [IBM] have done exactly what we wanted to make these machines good for a graphics interface," says Gates. "Two and a half years from now, virtually all office machines will use the graphics interface and OS/2."

–Tom Manuel

UNDER THOMSON'S WING, MOSTEK IS BEGINNING TO FLY

NOW GROWING TWICE AS FAST AS U. S. MARKET, IT AIMS TO HIT TOP 10 LIST

by J. Robert Lineback

CARROLLTON, TEXAS

Mostek is still haunted by memories—not the unprofitable dynamic random-access memories that once helped it lose an incredible $1 million a day, but the industry perception that little remains of the one-time memory leader, which France's Thomson-CSF purchased in the fall of 1985. The industry seems unable to forget the staggering losses and the exodus of engineers that eventually derailed Mostek when it was part of United Technologies Corp.

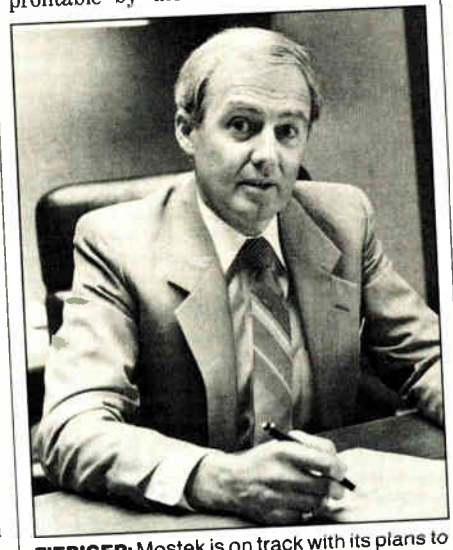
But now the Carrollton, Texas, company has been successfully reincarnated as Thomson Components-Mostek Corp., a subsidiary of the French electronics giant. The slimmed-down Mostek is now set to launch a flotilla of CMOS products, including tailorable 16-bit microcontrollers, specialized fast static RAMs, enhanced telephone-dialer chips, local-area-network circuits, and an entire family of large semicustom logic arrays using sea-of-gates technology.

Mostek's new 1.2-μm CMOS logic arrays will contain as many as 127,680 gates, with upwards of 57,000 being routable. By June, Mostek plans to start shipping prototypes of a 20,000-routable-gate array containing a sea of 45,000 continuous gates. Thomson engineers in France are working with Mostek to create products that allow customers to use LSI-level macrocell functions when designing with these arrays.

Now fueled by technology developed for fast SRAMs, the Mostek subsidiary is also taking the lead on Thomson's forthcoming 1.2-μm double-level CMOS process, which is earmarked for a new wave of chips, including digital signal processors and 64-Kbit SRAMs, as well as for build-to-suit foundry business. In addition, Mostek plans to start running a three-level-metal 0.8-μm process at its Fab 6 research and development center this year.

With the $71 million purchase of selected Mostek assets, Thomson has gained a key foothold in U.S. markets and an American fabrication presence, says Kathleen Killian, a London-based analyst for Dataquest Inc., San Jose, Calif., who tracks the French electronics giant. "It also got a world-class mask-making facility [capable of 0.5-μm geometries] and an automated diffusion center in Carrollton," she says.

Clearly, what was United Technologies' loss is Thomson's gain. Following a dramatic metamorphosis, Mostek turned an unexpected profit of $1.1 million in 1986, partly on the sale of unneeded assets and partly on sales of a product portfolio in which commercial DRAMs are conspicuously absent. That compares with a loss of $328 million in the first 10 months of 1985, when Mostek was still part of United Technologies. Now, Mostek executives expect the unit to become operationally profitable by the end of the year. "We



FIEBIGER: Mostek is on track with its plans to grow twice as fast as the U. S. market.

are right on track with our plans to grow at more than twice the rate of the U.S. market," says James R. Fiebiger, president and chief executive officer of Mostek. At that growth pace, Fiebiger figures the subsidiary will grab 2% of North American chip sales by 1990. Mostek will also sell semiconductors fabricated by sister Thomson operations, and it will keep a finger on the pulse of IC engineering trends in the U.S. Thomson is counting heavily on Mostek to help it make the Top 10 list of global semiconductor suppliers by the beginning of the next decade.

In the latest move to increase its size, Thomson has agreed to merge its nonmilitary chip-making operations with SGS Microelettronica of Italy, pending approval by the French and Italian governments [*Electronics*, April 2, 1987, p. 55]. The merger would not have much effect on Mostek, since there is little overlap between it and SGS, says Michel Motro, international vice president at Thomson Components. But he does expect the SGS sales force to strengthen Mostek's international marketing resources.

Back in Texas, Mostek has begun untangling the maze of different MOS processes that evolved during the six-year stint with United Technologies. To Fiebiger's dismay, the task of standardizing Mostek's process technologies has proven to be a major task in itself. "When we got into the consolidation phase, we found out we had 68 different process flows for 80 products," Fiebiger groans. He was recruited from Motorola Inc.'s Semiconductor Sector by United Technologies shortly before Thomson stepped in.

During the United Technologies era, some products were even running on more than one wafer line, and thus being produced with dissimilar processes. Fabrication engineers would often attempt quick fixes to get designs to work and to boost yields. And while the proliferating morass of process flows was bogging down yields, prices were nosediving in saturated commodity markets.

"We nearly had a unique process for every product," Fiebiger recalls. Today, Mostek has reduced the number to 20 process flows for about 90 products. It is now aiming to be down to just a dozen process flows by mid-summer. "The yields we are running today are at levels that previous management thought were impossible until the 1989 timeframe," he says, saying as many as 90% of the processed dice are now good when probed. Also, Mostek and Thomson operations are standardizing on a common 1.2-μm CMOS process developed by the Carrollton operation.

Few of Mostek's new designs were in working order at the time of Thomson's purchase. Executives at Thomson in France and at Mostek moved in to reorganize the company's semiconductor strategy, carving up and consolidating product lines into centers of expertise at either Mostek or Thomson. Now Mostek is focusing on fast SRAMs, specialized static memories, chips packaged with embedded lithium battery cells, gate ar-

rays, networking chips, telephone dialers, and 16-bit microcontrollers. Thomson engineers in France have been given responsibility for microprocessors, erasable programmable read-only memories, telecom chips other than dialers, digital signal processors, smart power devices, and standard-cell parts.

In the microcontroller market, this month Mostek is unveiling a redesigned CMOS version of its three-year-old 16-bit MK68200 [*Electronics*, Apr. 2, 1987, p. 22]. The chip's speed has been doubled, and the die has been laid out in a modular fashion so customers will eventually be able to tailor the chip.

In telecom markets, Mostek will introduce a new line of enhanced dialer chips. For data networking, the company is working on additional ICs for the Starlan local-area network. The company expects

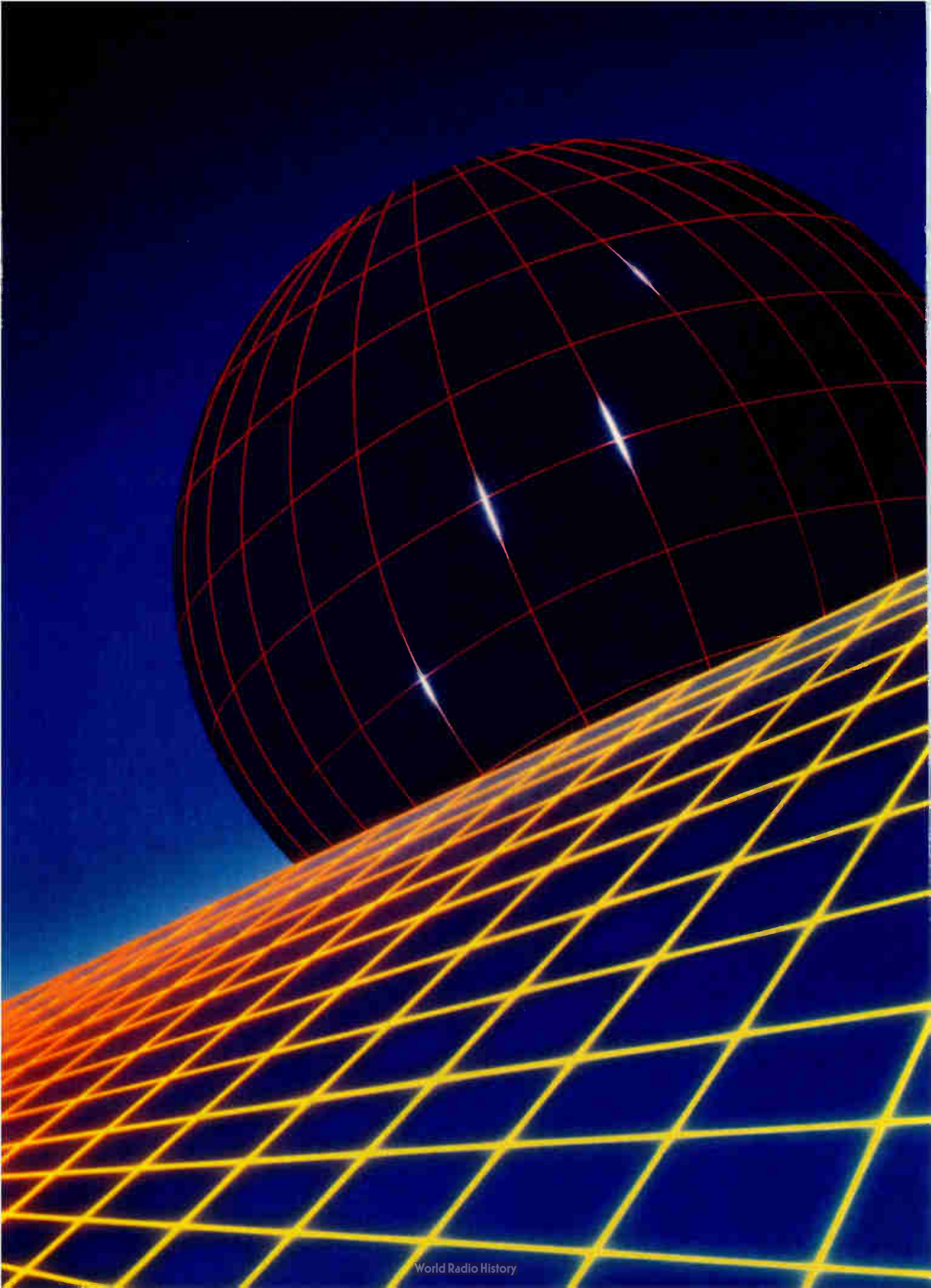
After losing $1 million a day in 1985, Mostek made money last year

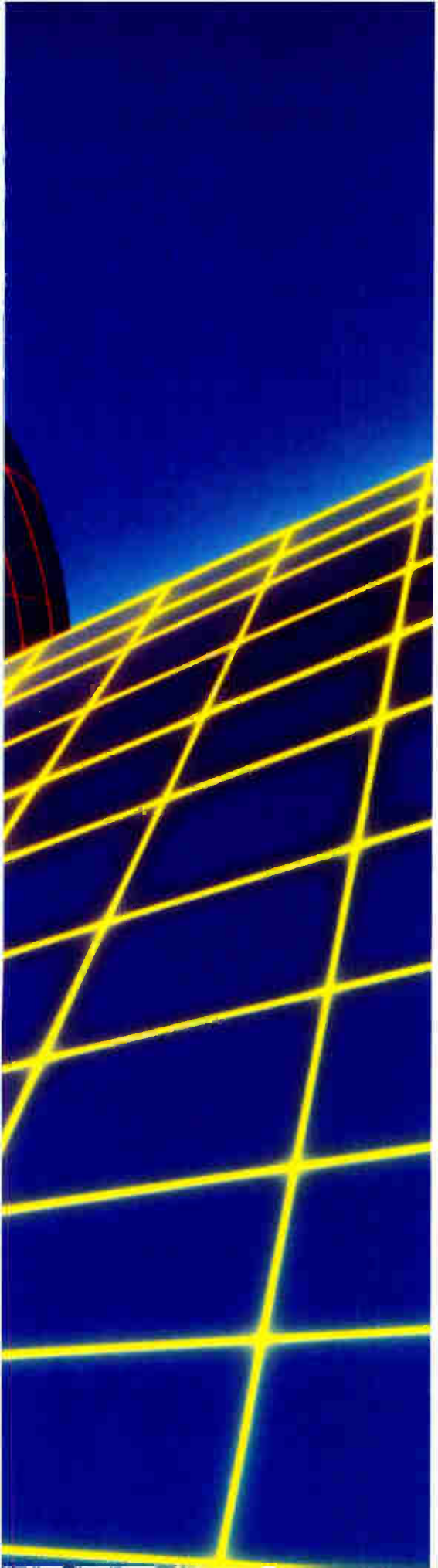
it will be able to provide samples of a variable-bit-rate LAN chip by midsummer.

In fast SRAMs, Mostek continues to emphasize six-transistor cell designs for low power. Spinoffs of standard SRAMs are targeted at first-in, first-out market segments, traditional areas for Mostek. The new 1-K-by-5-bit MK4505 FIFO, which is about three times faster than Mostek's older 4501 chip, is due soon. The SRAM operation also recently secured a critically needed second source for its specialty memories in a strategic pact with VLSI Technology Inc. of San Jose, Calif. Under the agreement, Thomson—along with Mostek—and VLSI Technology will second-source parts from each other, including FIFOs, dual-ported RAMs, cache-tag memories, and battery-backed SRAMs. The Mostek operation also continues to sell DRAMs in military markets, including a new 256-Kbit chip.

Excluding the unprofitable commercial DRAMs, Mostek had 1985 sales of about $50 million, according to Fiebiger. The operation's sales grew by about 20% in the U. S. last year, but more encouraging to Fiebiger were the size of orders and the arrival of new customers. "We more than doubled the number of accounts that were entering $1-million-plus orders in 1986 compared to 1985. And that was in a time frame when chip customers were trying to reduce the number of their suppliers," adds Fiebiger.

Although Mostek's recovery now seems to be on track, Fiebiger does not expect to get a nod of approval from major IC customers until 1988, when "we have shown that this was a successful turnaround." □





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INTERNATIONAL NEWSLETTER

NEC ASKS COURT TO BLOCK SALES OF SEIKO EPSON PC

The copyright dispute between Tokyo's NEC Corp. and Seiko Epson Corp. of Suwa [*Electronics*, April 2, 1987, p. 55] is now spilling into the courts. NEC says that Seiko Epson infringed on its rights with a personal computer that is fully compatible with NEC's PC-9801, Japan's best-selling personal computer, and the company has gone to court to ask for a provisional injunction to suspend sales of the disputed machine, Seiko Epson's PC-286. But NEC didn't stop there. The company also asked for a similar injunction stopping sales of Seiko Epson's 20-Mbyte external hard-disk drive, the HDD-20, a peripheral for NEC's PC-9801 that Seiko Epson began selling last December. NEC claims that software on the drive's interface board also violates its copyrights. Seiko Epson, meanwhile, says it plans to go ahead with delivery of the PC-286 late this month. □

TI JAPAN BEEFS UP BIPOLAR CAPACITY AND SIGNS ON ASIC PARTNERS

Texas Instruments Japan Ltd. of Tokyo is stirring things up in the Japanese chip market. TI is enlarging its manufacturing capacity for bipolar logic integrated circuits at its plant in Hiji, Oita, doubling output from around 22,000 advanced Schottky, advanced low-power Schottky, and TTL ICs per day to about 44,000. And the company is not ignoring its other business lines—TI Japan has signed Japan LSI Co., also of Tokyo, to act as a marketing arm and design center for TI's application-specific ICs and standard products. TI will provide Japan LSI with its standard-cell library but may also offer full-custom devices and gate arrays. The deal is TI Japan's second since November, when it signed Ascii Corp. of Tokyo to distribute graphic-system processors, digital signal processors, and other standard large-scale ICs [*Electronics*, Nov. 27, 1987, p. 48]. □

HITACHI TAKES AIM AT NETWORKS WITH HIGH-BIT-RATE LASERS

A multiple-quantum-well semiconductor laser with the 30-MHz resonant frequency needed for modulation rates up to about 11 Mbit/s has been developed at the Central Research Laboratories of Hitachi Ltd. This high-speed response will be needed for faster communications, including telephone company trunk lines, value-added networks, and local-area networks. Hitachi is using selective ion doping to speed the electron transitions that drive the laser for faster response. Initial work has involved gallium arsenide and aluminum gallium arsenide to fabricate lasers that operate in the 0.8-μm band. But light-scattering losses are lower at wavelengths of 1.3 and 1.5 μm, so Hitachi researchers plan to apply the new technology to indium gallium arsenide phosphide/indium phosphide lasers that will operate in the 1.3-μm band, and InGaAs/InP lasers for the 1.5-μm band. □

NEW VENTURE AIMS TO MAKE LCDs WITH 1,000-LINE RESOLUTION

Image Displays Ltd.—a new joint venture of London-based STC plc, Alcatel NV of the Netherlands, and venture capitalists—is aiming to turn the liquid-crystal-display market on its ear with a line of smart, high-resolution displays based on Smectic A technology. STC says the displays will be the first LCDs available to offer a full 180° viewing angle, and they will also have on-screen memory, meaning the screens will not need refreshing every 200 lines as do conventional LCDs. That will help Image Displays to produce screens with more than 1,000 lines resolution, much higher than is currently available. Samples of the new display will be available from STC Technology Ltd. in Harlow, England, this year, but production displays will not be available until next year, when a new production facility in Cambridge will be ready. □

INTERNATIONAL NEWSLETTER

NEC PAIRS A MES FET WITH AN INDIUM PHOSPHIDE PHOTODIODE

A new heterogeneous substrate, made by growing gallium arsenide epitaxially on selected areas of an indium phosphide wafer, is providing researchers at NEC Corp.'s Ultra High Speed Device Research Laboratory with a new way to build optoelectronic integrated circuits. The first device includes an InP PIN photodiode, a gallium arsenide metal semiconductor field-effect transistor, and load resistors for the diode and the transistor. The PIN diode provides a high-sensitivity photodetector in the 1.3- and 1.5-μm optical communications bands. The development is a boon to NEC, because it allows the company to build on its experience with GaAs technology. The company says it might otherwise take years to develop complex ICs on InP substrates, because that technology is so new and there is no commercial experience on which to build. □

WILL WEST GERMANY OPEN UP THE MARKET FOR TERMINAL EQUIPMENT?

Bowing to pressure from the U. S., West Germany's communications authority, the Bundespost, is considering new regulations that would make it easier for foreign companies to sell terminal equipment used in public networks. The regulations, which could go into effect this fall, would relax acceptance procedures so that foreign suppliers without domestic standing would be on equal footing with native German suppliers. The rules also seek to shorten the arduous approval process from as much as a year or longer to as little as four months. The U. S. has pressed West Germany in recent years to open its terminal market to foreign producers, but the Germans have maintained that the U. S. already enjoys a trade surplus for communications equipment. The Bundespost says the U. S. registered big surpluses in the past three years—$140 million in 1984, $145 million in 1985, and $130 million during the first eleven months of 1986. □

BASF TAPE CARTRIDGE PACKS 2 GIGABYTES—BUT YOU CAN'T BUY A DRIVE

Anticipating the kind of high-density backup tape drives users will be demanding in about two years or so, West Germany's BASF AG has developed a tape cartridge that holds as much as 2 gigabytes—about 10 times the capacity of most current cartridges. The 185-foot-long, ½-in.-wide chromium-dioxide tape will not find a use for some time, however, since drive equipment for the new cartridges will not be available until late 1988, according to BASF, of Ludwigshafen. BASF achieved the high density step by step. By doubling the number of tracks on the tape from 18 to 36, doubling the write density from 24,000 to 48,000 flux changes/in., halving the thickness of the tape itself—thus permitting more tape in the cartridge—and developing data-compression techniques, BASF achieved its goal of putting 2 gigabytes of data on one cartridge. □

WILL TOSHIBA AND SANYO JOIN THE LASER VIDEODISK CAMP?

Competition between laser-disk players and capacitive-pickup video home disk players in Japan is heating up, as Toshiba Corp. and Sanyo Electric Co. begin to straddle both camps. Since 1983, Toshiba, of Tokyo, has offered VHD machines; now the company is starting to market a combination player for laser video disks and audio compact disks made by Pioneer Electronic Corp., also of Tokyo. Toshiba was attracted to the laser-based video system by the advent of the compact disk with video, a new CD format called CD-V [*Electronics*, March 19, 1987, p. 53]. Sanyo, of Osaka, is also expected to sell a laser video/CD audio player. Toshiba says it expects to sell as many as 1,000 to 2,000 a month in Japan. □

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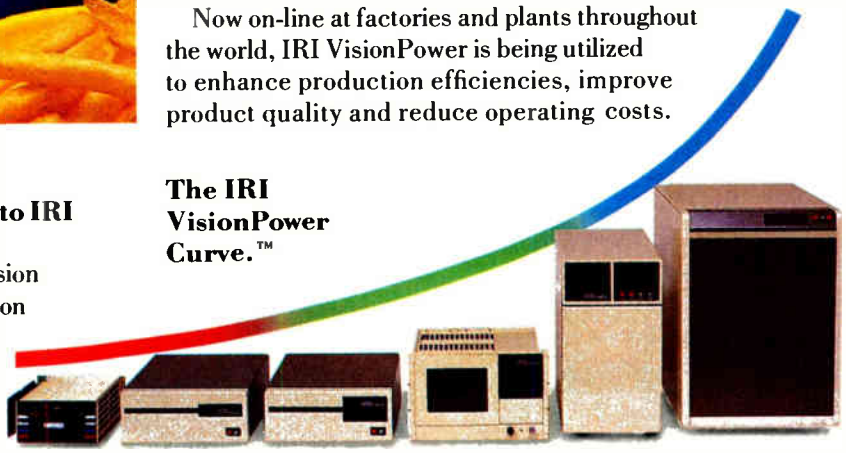

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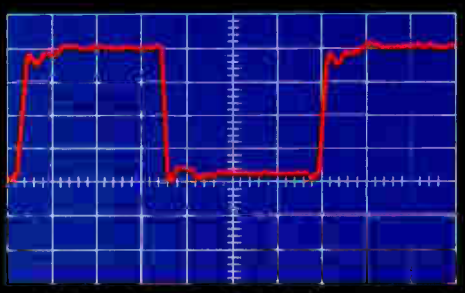

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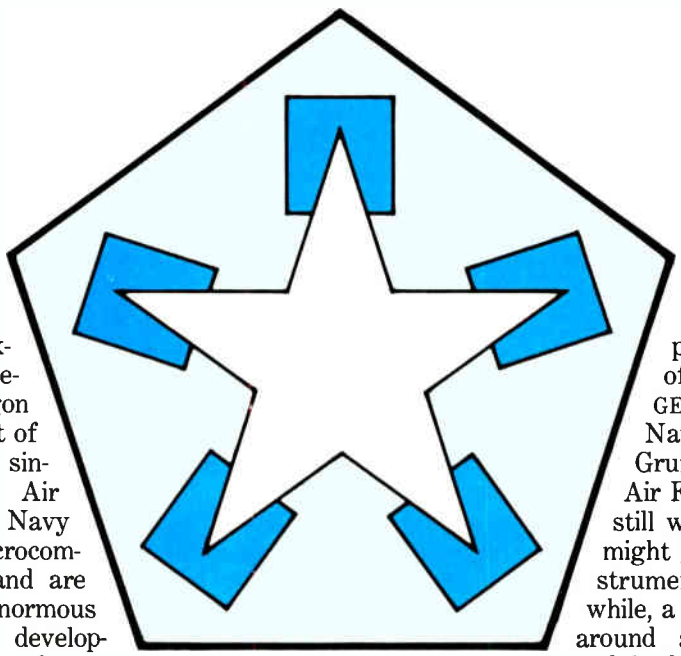
INSIDE TECHNOLOGY

HOW DOD IS CREATING A MAJOR NEW BUSINESS

All three services push major instrument-on-a-card programs, and only a lack of standards is holding back a flood of commercial business

by George Sideris



Drawn by the lure of extremely flexible and relatively inexpensive test-and-measurement systems, the Pentagon is pushing the development of test instruments built on single-card modules. The Air Force, the Army, and the Navy are all working on the microcomputer-controlled systems and are devoting much of their enormous purchasing power to the development of a new generation of automatic test equipment based on instruments on cards.

One likely result of the military's drive will be the creation of a major new commercial market for a new breed of card-based instruments. But that won't happen until the military eliminates a major stumbling block: so far, no military standard for instrumentation buses or card formats exists. All three military services are currently pursuing slightly different approaches, a course that instrument vendors find very frustrating. A single standard still looks doable, but many problems have to be solved first.

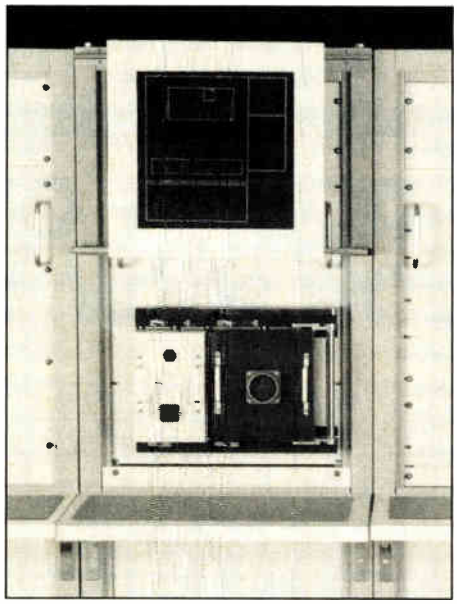
Many instrument vendors are already building instruments on cards that are compatible with IBM personal computers and other machines. But because of the lack of standardization in the military realm, instrument makers are by and large steering clear of the Pentagon's instrument-on-a-card programs. They do not see a broad market developing behind the service-specific systems. Thus the development of the cards for the new military systems is being done almost entirely by prime contractors instead of instrument companies—GE is doing the job for the Navy, for example, and Grumman for the Army. The Air Force, on the other hand, is still working on a standard that might gain the support of the instrumentation industry. Meanwhile, a few companies have rallied around a VMEbus-based one-card module developed for the Air Force by Wavetek Corp., San Diego (see p. 60), in an effort to make it a de facto standard.

But until a single standard is worked out and given the stamp of approval, traditional instrument makers are not likely to show much interest in the military's efforts. Particularly in the Army and Navy cases, "we can't do much for them because those are sole-source contracts with nonstandard instrument buses and card sizes," says Marlyn Huckeby, military/aerospace program manager at Tektronix Inc., Beaverton, Ore.

But Huckeby recognizes that the military has different goals it must pursue, goals not necessarily compatible with the interests of instrumentation manufacturers. For instance, to get rid of a "logistics tail" that now stretches over the waves to many commercial instrument manufacturers, the Navy wants its test equipment built like a weapons system and supported by a prime contractor. On a ship at sea, "the captain doesn't want to call an 800 number for service when

an instrument breaks down," Huckeby says.

Although the commercial instrument-on-a-card market is growing rapidly, it is still small compared with the total military ATE market. Prime Data, a San Jose, Calif., market researcher, estimates the computer-dependent instrument market, which includes instruments on cards, was $191 million in 1986 and will grow to $485 million by 1990, a rate of 26% a year. Of 1986 sales, $18 million were low-end test instruments, mostly cards used with PCs; $54 million were high-end test instruments, which are not by and large card-based; and the remainder were card-based data-acquisition instruments. Industry sources estimate the total military ATE market at $3 billion.



1. SEAWORTHY. GE's system for the Navy is being built using instrument-on-a-card modules.

Instruments on cards will challenge in the military market conventional instruments from such old-line manufacturers as John Fluke, Hewlett-Packard, and Tektronix—the big three in the military ATE market. Industry sources say that HP reaps about 40% to 50% of military instrument sales because it continually pushes the state of the art in rf testing.

MEETING RF REQUIREMENTS

But cards can already meet some of the requirements of rf testing, as demonstrated by a signal-generation unit using eight instruments on cards that Wavetek introduced in early April at the Electro show in New York [*Electronics*, Apr. 2, 1987, p. 107]. It puts out complex waveforms for such jobs as radar-receiver testing and boasts a precision of 100 ps at a signal delay of 1 μs.

The unit is being used by Honeywell Inc. in an Air Force system known as GATE, short for Generic ATE, because it will be the first to test many kinds of avionics systems. Moreover, cards have helped improve system performance, says Trygve Svard, the GATE project's technical director at Honeywell's Test Systems and Logistics Operations in Minneapolis, Minn. Although Honeywell began developing GATE a year ago, Svard started asking instrument makers to work on instrument-on-a-card technology well before that.

"We started talking to vendors three or four years ago, and one that listened a lot was Wavetek," says Svard. "We generally use four or five of their instruments in a bay. They only cost around $5,000, but the bay costs $50,000 with all the power, cooling, shielding against electromagnetic radiation, and so forth. With eight cards in a module, you get a good cost ratio."

Honeywell is developing specialized instruments on cards that will fit into a Racal-Dana signal-switching chassis with a VMEbus backplane. Plugging cards into the chassis, which routes test signals, minimizes signal-path lengths and thereby eliminates most performance losses caused by the long cables in traditional rack-and-stack systems. Putting the cards close together improves signal fidelity and frequency response, says Svard.

To the Air Force, a GATE system using instrument-on-a-card technology is just another evolution of MATE, the Modular-ATE program that regulates procurement and provides system-integration guidelines and standards. The Air Force has not yet required contractors to use card-based modules but is nudging them in that direction.

For the Navy, the Consolidated Automatic Support System, or CASS, in development at General Electric Co. is based on card-level instruments and will be "completely modular—from the built-in-test level to complex test functions, from dc to light," says John E. Barker, GE's program manager. GE will supply the modules. CASS will go into production in the early 1990s and will become the fleet's standard ATE system (see fig. 1).

Aircraft carriers are now loaded with 95 kinds of test equipment and must carry 30,000 spare parts and 21 civilian ATE workers. CASS will reduce that to five test systems, 3,800 spares, no contractor personnel, and will cut training programs from 185 to five. The Navy selected GE's Federal Electronic Systems Division in Philadelphia as the prime contractor in December, after GE won a design competition against Grumman Corp. of Bethpage, N. Y.

CASS will have a general-purpose core system, specialized test stands for applications such as electro-optical testing, and a portable unit for the flight deck. The system uses VMEbus at the instrument-control level and Ethernet at the station-control level.

The Army's instrument-on-a-card project aims to build what it calls Intermediate Forward Test Equipment. Grumman is set to start production early next year of IFTE, an evolution of System X, an ATE system Grumman built as part of a $50 million investment to start up its Electronic Systems Division and win military ATE orders. The company expects orders to exceed $1 billion.

With IFTE, an ATE system can go into a battle zone, something not possible with current Army ATE. The main system, called a shop tester, fits in

a shelter on a truck (see fig. 2). IFTE, like CASS, uses a modified VMEbus, but its cards are not compatible with those built for CASS. IFTE will replace an ATE system too big to move and dozens of small systems. A portable field unit will be used to make on-the-spot repairs. A system equivalent to the shop tester but built with commercial equipment will be used in depots.

Though Grumman will use cards for other instrumentation, it chose the HP 71000 modular spectrum-analyzer system for rf measurements. Each stage of the analyzer is separately packaged and plugs into a chassis.

And HP studied the possibility of building such instruments with cards and found that cards ran into a "microwave barrier" between 1 and 2 GHz, according to John Knobel, marketing manager for modular measurement systems in HP's Signal Analysis Division, Rohnert Park, Calif. Multiple cards would be needed, he says, and in that frequency range, shielding and matching requirements for cards become so hard to meet that building an instrument in the usual way becomes more cost-effective. The modular approach was adopted so modules could be mixed, matched and upgraded, which, he argues, provides the same benefits as cards.

There are no HP instruments in the Navy's CASS system, says Knobel. "GE intends to design every piece of test equipment themselves, including microwave. It's a big challenge."

IFTE and CASS have attracted few instrument companies. Racal-Dana Instruments Inc. was invited to participate in the IFTE program, "but we looked at the economics and declined," says Brian Hull, vice president of the Irvine, Calif., company. "It's not an open architecture that will be accepted by industry. Grumman has had to develop most of the virtual instruments."

Instrument makers are, however, ready to build instruments on cards for the military as soon as a single standard emerges. The search for a standard began in 1985 when the MATE program office asked its users group to recommend one. The task was assigned to a subcommittee headed by Louis Klahn, sales manager of Colorado Data Systems Inc. The group agreed that the VMEbus should be upgraded for instrumentation. "We had a fairly final version in November, and then the vested interests came out of the woodwork," Klahn says. "In my opinion and that of several others, this is a good standard. You can't optimize for everything."

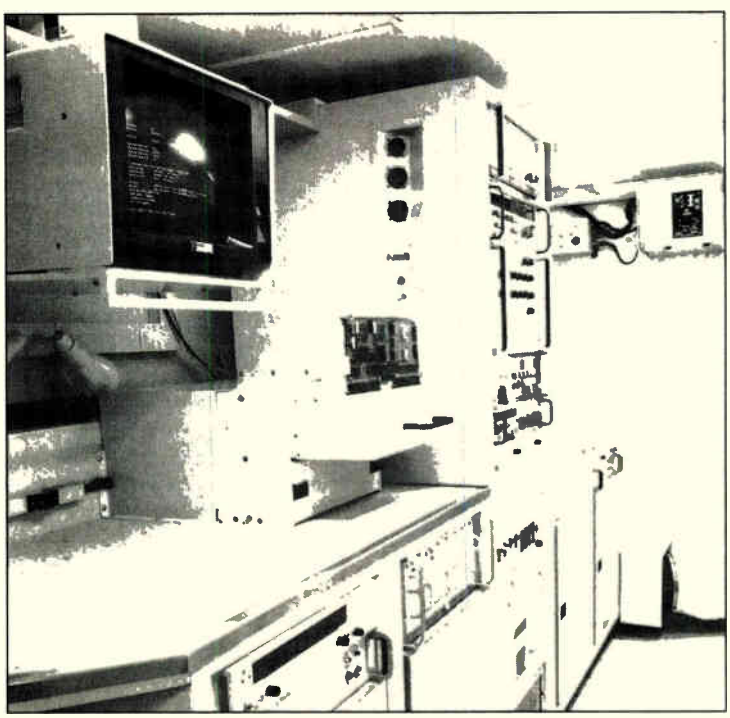
The draft is in review but may not be adopted, says Col. George Wright, MATE program director at the Aeronautical Systems Division, Wright-Patterson AFB. "This would be the first standard that broaches major new territory for the MATE standards. While we are anxious to get it out, we are also anxious that we don't design ourselves into a technical-obsolescence box."

"Our first-order concern is whether or not we need to establish a standard at all, then whether we should establish an interface at that level. It might not be necessary, it might be too detailed and limit freedom to innovate," Wright adds. "Our concern is whether or not that's the place to standardize and only secondarily whether or not that's the right bus. Most of the work on the standard has been at that second level." If those issues are resolved, Wright says, the standard could be adopted in June.

The flexibility of card-based instrument systems makes it possible to replace a wide range of existing equipment and cut down on training programs

Wavetek's bus is compatible with the standard recommended by the MATE Users Group, according to Fred Bode, the company's business unit manager for system products and instrumentation computers. In addition to the two standard VMEbus buses, the Wavetek version includes a third bus for high-speed analog signals. "In fact, Lou Klahn talked at the last [users' group] meeting about some of the limitations that he found in using just the two VMEbuses. So I think that will probably be changed."

Instruments compatible with Wavetek's system are on the way from Racal-Dana and Datron Instruments Inc., Stuart, Fla. If more companies climb aboard, they may be able to establish the card size and bus structure as de facto standards for military and commercial applications. □



2. TRUCK-MOUNTED. This instrument-on-a-card system Grumman is building for the Army rides into battle on a truck.

CARD-BASED ATE SYSTEM COULD SET A STANDARD

Wavetek's instrument-on-a-card system replaces a rack of instruments for ATE applications with eight plug-in modules

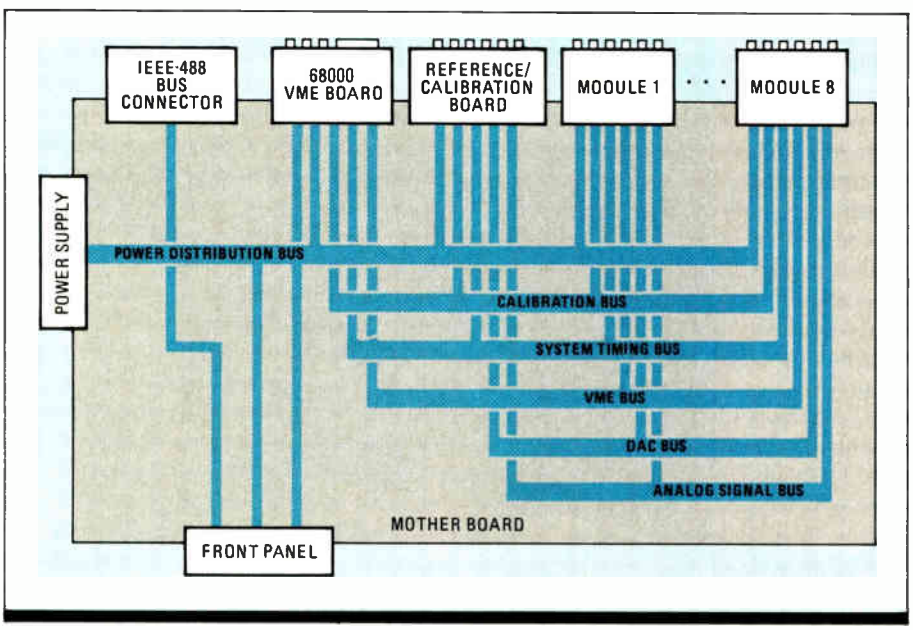
by George Sideris

A young contender is pushing its way to the forefront of the emerging market for instruments on cards. The 680 system from Wavetek Corp. uses cards in a package that can replace a rack of conventional instruments—and Wavetek's approach is already making a strong bid to become a de facto standard in its market.

The 680 already is off to a flying start. The system is being introduced at Electro, [*Electronics*, April 2, 1987, p. 107], but the first 680 was delivered to Honeywell Inc. in December, for use as a subsystem in a project for the Air Force.

More important, San Diego-based Wavetek has been joined by Racal-Dana Instruments Inc. of Irvine, Calif., and Datron Instruments Inc. of Stuart, Fla., in a campaign promoting the 680's design as a standard for high-performance, instrument-on-a-card systems, says Mathieu van den Bergh, system products manager at Wavetek. If the campaign is successful, it could make Wavetek a major player in the instrument-on-a-card segment of the ATE market—particularly the military segment, where growth has been hampered by a lack of standards (see p. 57).

The 680 is built around an open-architecture mainframe, the size of a conventional rack-mountable instrument, that supports independent or interactive operation of up to eight plug-in instruments on cards. At the heart of the mainframe is an upgraded VMEbus, upgraded with a high-speed instrumentation bus and analog buses that carry signals in the 100-MHz range. The new buses are built with impedance-matched striplines, a printed-circuit version of coaxial cabling. Van den Bergh says the bus outperforms the IB 1 design that has been proposed as an Air Force Modular Automatic Test Equipment, or MATE, standard, but that it is compatible with the proposed standard. Wavetek's architecture (see fig. 1) was aimed at military ATE systems and, in particular, MATE-compliant avionics systems.



1. PICK A CARD. The 680 system's architecture includes a 68000 microprocessor and an upgraded version of VMEbus. The upgrades include instrumentation and analog signal buses.

The first 680 System Wavetek delivered, in fact, is intended for a military application. Honeywell is using it as the video stimulus subsystem of the Generic ATE system, a general-purpose avionics test system being developed for the Air Force. Van den Bergh says it may be used in as many as 120 test stations.

And Wavetek hopes that the

push to make the 680 a standard will dramatically boost its use in other military ATE systems. Its two allies are doing their part by designing new cards that are compatible with the 680 system—and which widen its applications. Racal-Dana has developed a card version of its Model 1994 1.3-GHz microwave frequency counter/timer. Datron has a card equivalent of its Model 1602 6½-digit multimeter. To attract other instrument makers, Wavetek offers its software and documentation to them for a nominal fee.

The trio expects competition from larger companies but, says van den Bergh, they are a year or two ahead of the pack. And each is a leader in a different military ATE niche—Wavetek in signal sources, Racal-Dana in frequency counters and timers, and Datron in digital voltmeters.

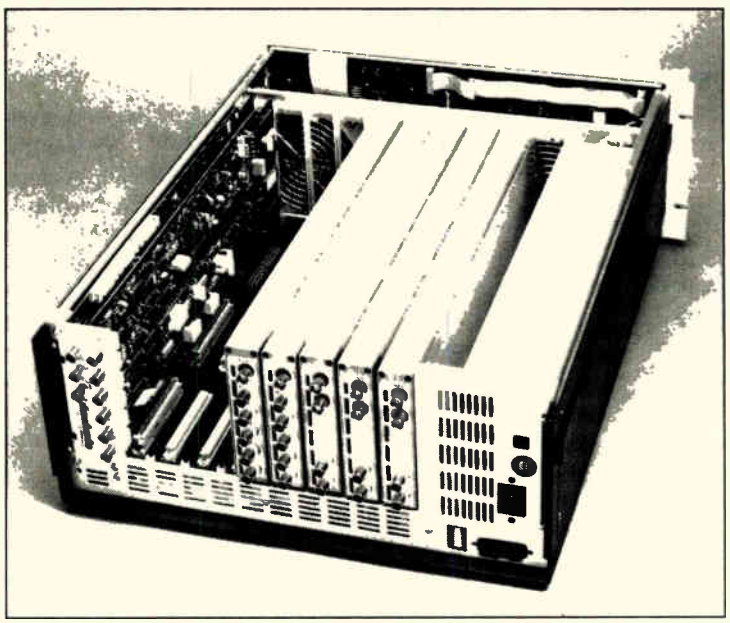
The system they are all banking on, the 680, is based on a mainframe that comes in a 7-inch-high unit that fits into a standard instrumentation rack. Eight cards, each shielded by an aluminum housing, plug endwise into a backplane in the mainframe's floor (fig. 2). Each card's far end projects through a rear opening, so that coaxial cables and other test-signal lines can be connected to it. Internal temperature is maintained by three variable-speed cooling fans regulated with the aid of a temperature sensor in the switching power supply.

The cards share a host processor, called the VME board, based on Motorola Inc.'s 68000 microprocessor. Standard memory includes 512 Kbytes of dynamic random-access memory, 128 Kbytes of nonvolatile static RAM and 1 Mbyte of programmable read-only memory. Among the input/output ports is a 16-bit analog port for testing VLSI circuits, digital signal processors, and other components. A reference/calibration board provides a 10-MHz clock and a phase-locked-loop-controlled 100-MHz clock, both accurate to within ±1 part per million, a trigger source that can be set to 5 digits and which has 0.1% frequency accuracy, and an external trigger input with programmable delay.

The reference/calibration board is controlled by a 6803 8-bit microprocessor. Programmed auto-calibrations are based on a zener voltage reference and a crystal clock that the user can align with external references. The 6803 uses the on-board references to align a digital voltmeter, counters (application-specific integrated circuits), system clocks, and other on-board circuitry. That done, it checks the card instruments and stores correction factors in the VME board's nonvolatile RAM. To maintain accuracy, the system generates an alarm if the operating temperature goes 5°C above or below the calibration temperature.

The front panel subsystem is designed for stand-alone operation and system troubleshooting. Its 6803 microprocessor can store and recall instrument-on-a-card setups and display the instruments' functions and test parameters. It communicates with the VME board via an optically isolated data link. Panel I/O routines were written in assembly language for speedy execution. Other system firmware is programmed in the C language. Programs are compiled with the Greenhill C compiler from XEL Inc., Cambridge, Mass., and run on the PSOS real-time multitasking operating system from the Software Group Inc., Santa Clara, Calif.

Wavetek's system bus uses all three connectors and buses allowed by the VMEbus (IEEE-1014) structure. Only two connectors are employed by a combination VMEbus and instrumentation bus, known as IB 1, proposed last year as an Air Force standard by an instrument-on-a-card subcommittee of the National Security Industrial Association's MATE Users Group. Wavetek added a third section



2. CHASSIS. The instrument cards plug vertically into a VMEbus backplane and are controlled by the microprocessor.

that provides a variety of analog buses. One analog bus, for example, sums the output of up to eight cards. In the signal-generator version, this allows the system to generate very complex wave forms with much greater precision than a set of conventional signal generators.

Besides the third bus, the major difference between Wavetek's bus and IB 1 is the backplane construction. Wavetek went to an 8-layer backplane with stripline conductors and ground planes on the top layer, fourth layer, and bottom layer of the printed-circuit board. Analog lines are kept well away from the noisy power and digital lines. Each signal pin is isolated by grounded pins. The analog-line design rules are also stricter. For instance, there can be no more than a ½-inch stub between the trigger driver/receiver circuit and the connector. The striplines are conductors sandwiched between shielding, as usual, but advanced layout and termination techniques impedance-match the lines so they would not "ring" (generate noise by reflecting signals), says Kwok Lo, system products engineering manager.

Van den Bergh says Wavetek abandoned a more efficient, less costly proprietary bus to con-

more efficient, less costly proprietary bus to converge on the proposed IB 1 standard, and developed its backplane to boost performance over the VMEbus-based standard. "We found that IB 1's trigger buses work fine up to few hundred kilohertz," he says, "but if you go up in frequency, the triggers become ambiguous." Lo explains, "The pulse-transition time, not frequency, is the critical thing. If it's faster than a few nanoseconds, IB 1 causes a lot of ringing. To 20 ns, it's fine. Faster, you can cause multiple triggering. You send out one trigger pulse and you may get several in the bus line."

Wavetek fashioned its upgraded VMEbus, with added instrumentation and analog buses, to hew as closely as possible to the proposed Air Force MATE standard

Like IB 1, Wavetek's design follows the VMEbus standard for the microprocessor bus. That is, a 96-pin connector P1 (3 rows of 32 pins) defines a basic 16-bit system bus with 16.7 megabytes of address space. Also, it expands to a 32-bit system bus with 4-gigabyte addressing by using one row of P2, a second 96-pin connector, for 8 upper address bits and 16 upper data bits. The other rows of P2 provide the instrumentation bus.

Wavetek's 32-bit digital-instrumentation bus has 4 lines for module identification codes, 20 lines for data at transistor-transistor-logic levels, and 8 lines for emitter-coupled-logic signals that can be converted to TTL levels by the individual modules. The 20-bit bus allows modules to transfer data without tying up the VMEbus. The ECL lines provide for such functions as slicing up time intervals to increase timing precision. P2 also provides bus sections, constructed as analog lines, for synchronizing the system, triggering the various modules, and distributing the 10- and 100-MHz system clocks. System modules are synchronized within 1 ns; the card instruments can be triggered within 1 ns of each other.

Overall, the 680's design makes it well suited for military ATE applications, especially the avionics-oriented MATE systems. Military ATE systems usually contain low-frequency analog, radio-frequency and microwave test sections. Like the conventional instruments in MATE systems, the card instruments communicate via an IEEE-488 port. Programming options include English-like commands and, with an optional test module adaptor, the MATE Control Intermediate Interface Language. A MATE requirement that instrumentation automatically find 95% of all instrumentation problems with 98% confidence is met by the 680 with built-in test functions. □

For more information, circle 480 on the reader service card.

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FOR WAVETEK, CARD-BASED ATE IS A WAY TO COMPETE WITH LEADERS

For Kwok S. Lo, the exciting thing about instrument-on-a-card systems is that one and one add up to more than two. "Two signal generators linked together in the same place can do more things than two independent instruments could ever do in the past," says Lo, Wavetek Corp.'s system products engineering manager.

For Mathieu van den Bergh, system products manager, there's another attraction: the technology is an equalizer. It's a way for smaller companies to compete in the automatic-test-equipment market with industry leaders like Hewlett-Packard Co.

Lo, born in Hong Kong 49 years ago, joined Wavetek in 1969, the year he got his MSEE at California's San Jose State University (he got his BSEE at University of California, Berkeley, in 1966). "We talked about building a multisource instrument four years ago," Lo says. However, the project was shelved as too costly. Then van den Bergh, a 40-year-old native of the Netherlands (he got his BSEE at Arnheim College in 1968) joined Wavetek early in 1984.

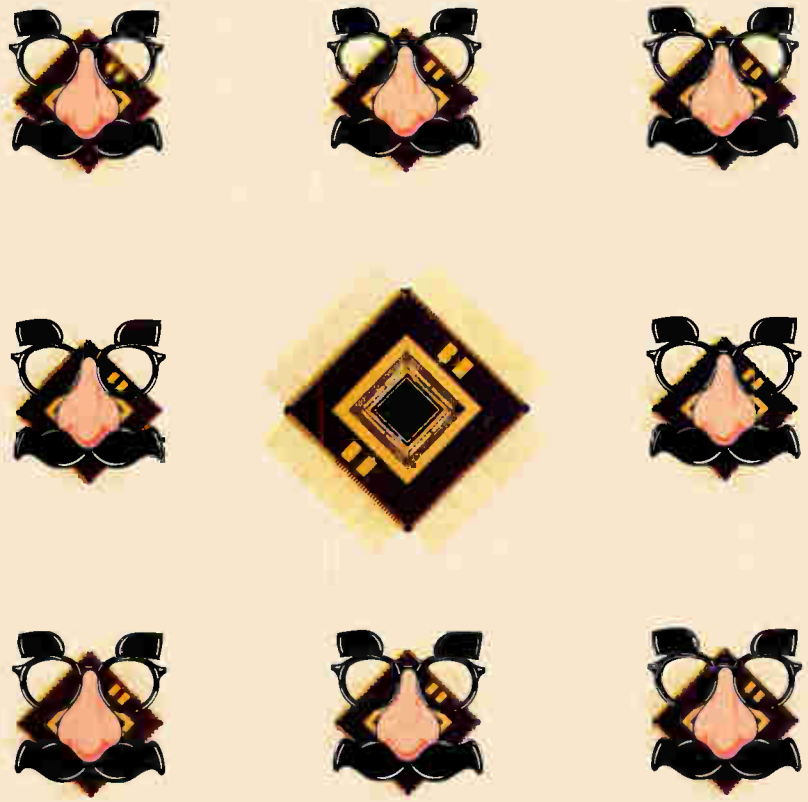
He soon won management's backing for the project. One reason: suitable application-specific integrated circuits were becoming available. Previously, only large firms could afford to develop custom components for high-performance instruments, he says. "ASICs made it possible for smaller companies like Wavetek to compete on an equal level in technology and performance." With gate arrays and other ASICs, Lo's team could squeeze high-performance instruments into a card system. The team had set as its goal tying at least eight signal generators together.

CARD PLAYERS. Wavetek's Matheiu van den Bergh (left) and Kwok S. Lo

Wavetek had another advantage, van den Bergh adds. The Air Force's Modular Automatic Test Equipment program was creating a demand for highly modular systems, and Wavetek had begun to develop MATE-compatible instruments. Lo laid some of the groundwork by working on an industry committee defining CIIL, the program's Control Intermediate Interface Language that all MATE-compatible instruments must now "speak."

Wavetek went to an open-architecture system so that MATE prime contractors could use instruments on cards in the same mainframe. But the 680 System still met the original goal—the first version links eight signal generators.

Not just another face in the crowd.



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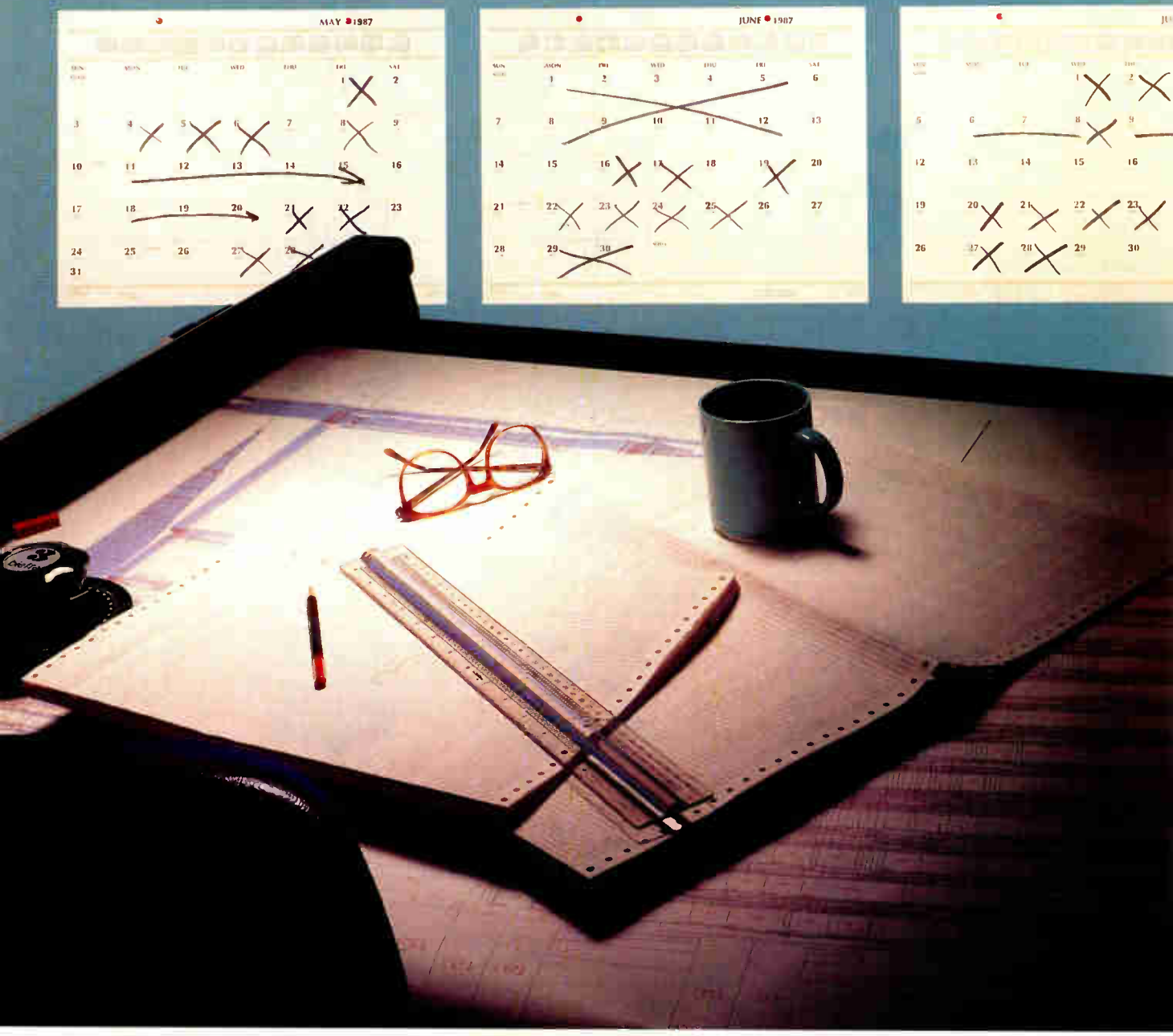

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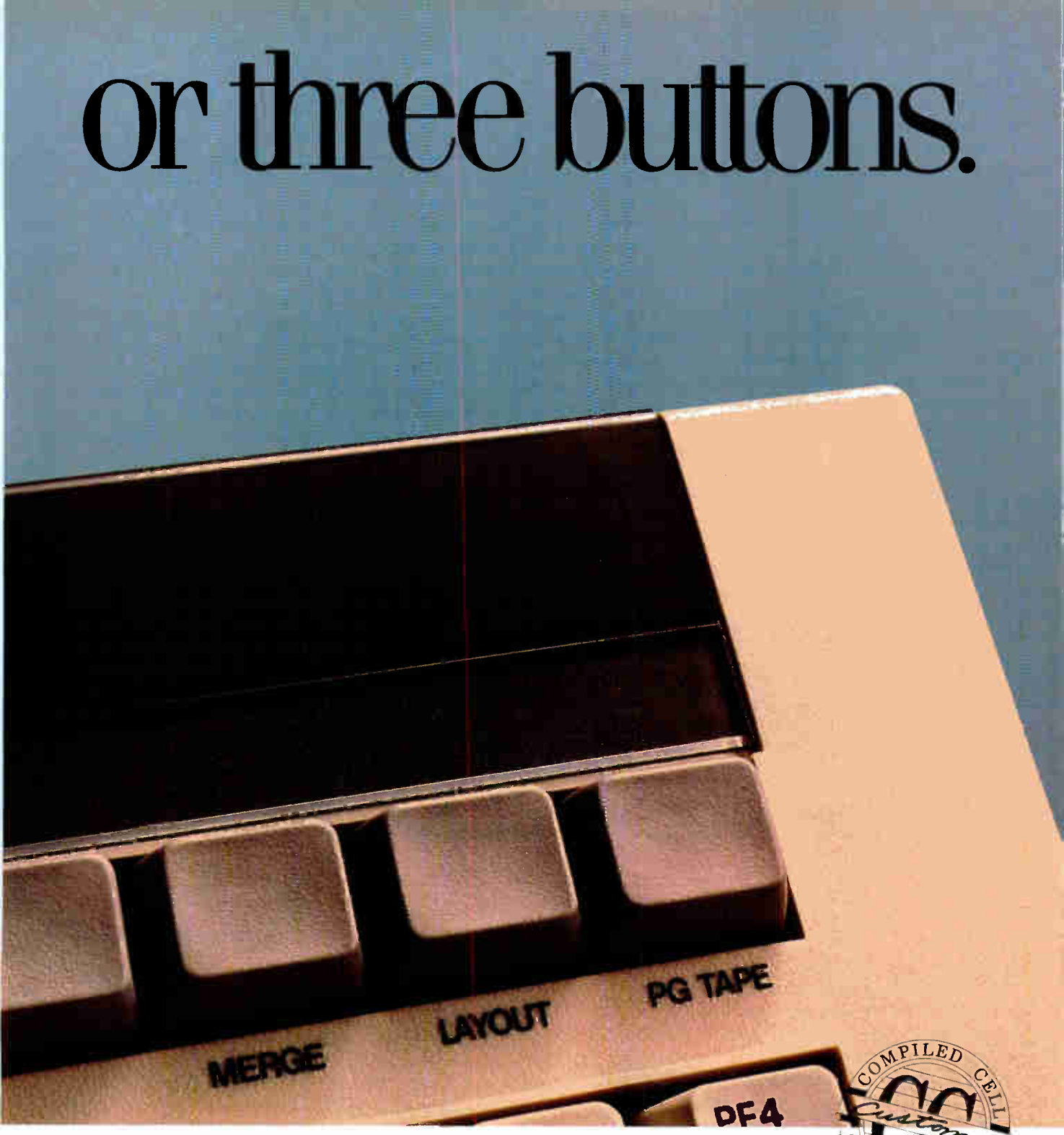

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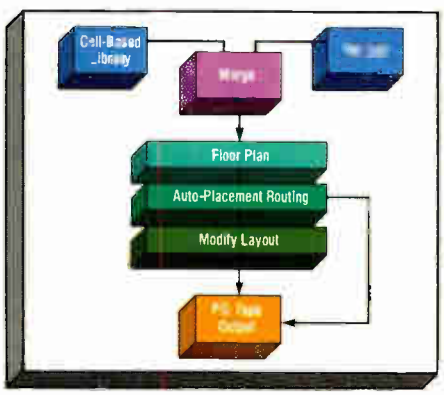

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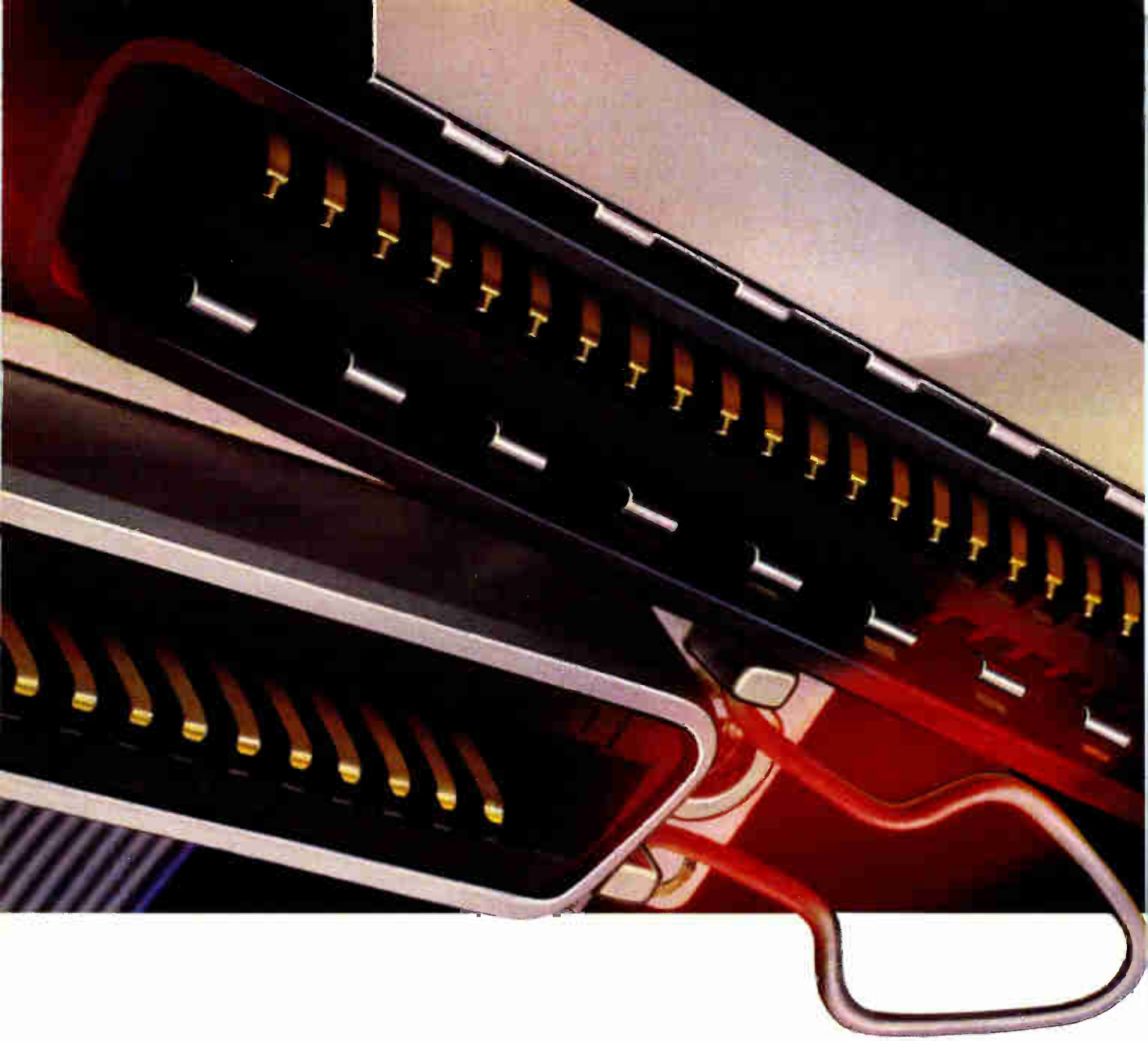

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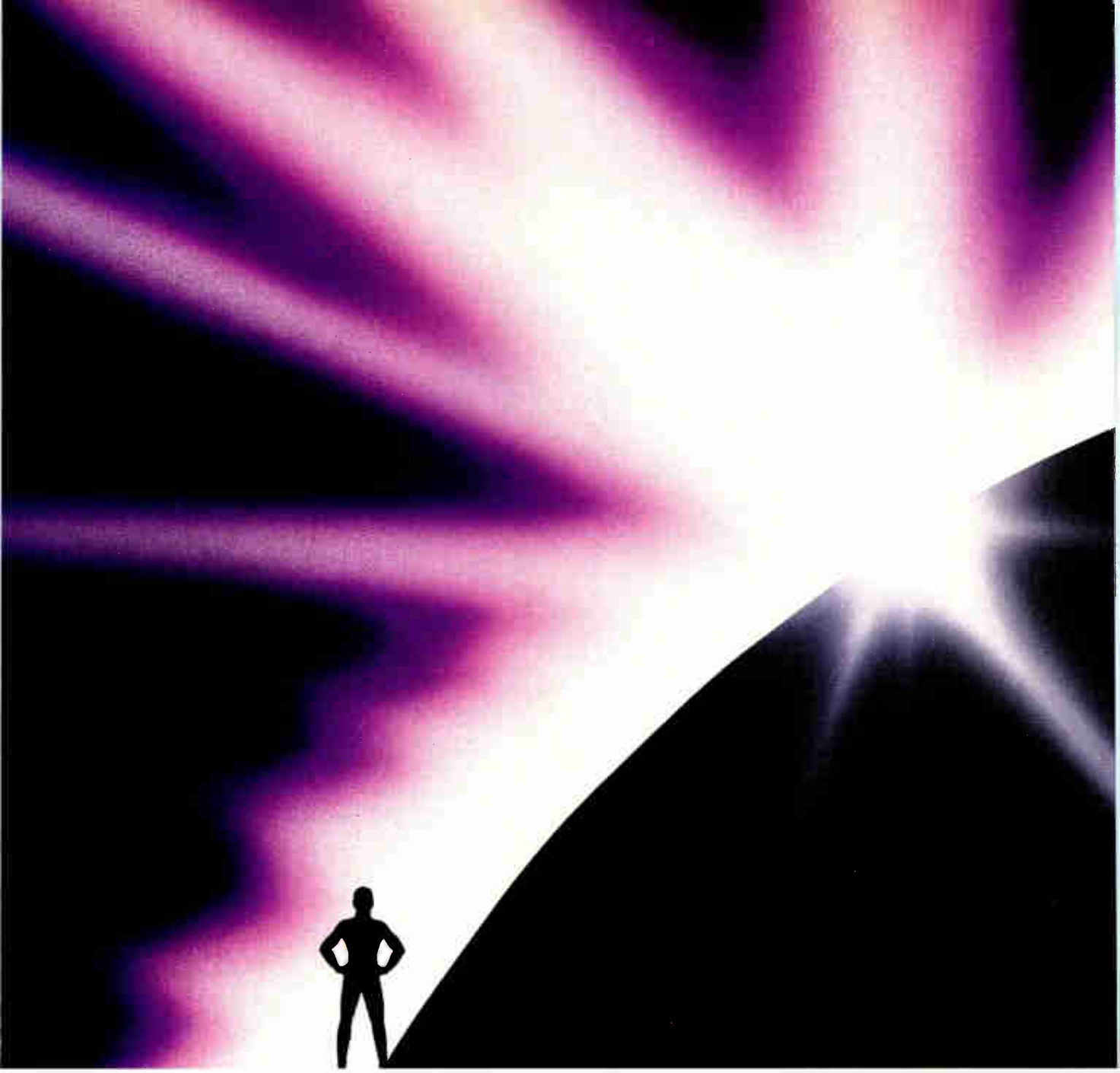

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THIS BIPOLAR PROCESS GIVES DENSITY AND DYNAMIC RANGE

By combining highly doped, buried layers with thin epitaxial layers, Fairchild gets practical linear circuits without sacrificing LSI densities needed for digital functions

by Bernard C. Cole

A new process from Fairchild Semiconductor Corp. seems to resolve what has always appeared to be an irreconcilable problem for chip designers: how to get high-performance analog and high-density digital functions to reside on the same chip. The new process, called LFAST, is a 5-μm linear bipolar process from Fairchild's Linear Division in Mountain View, Calif.

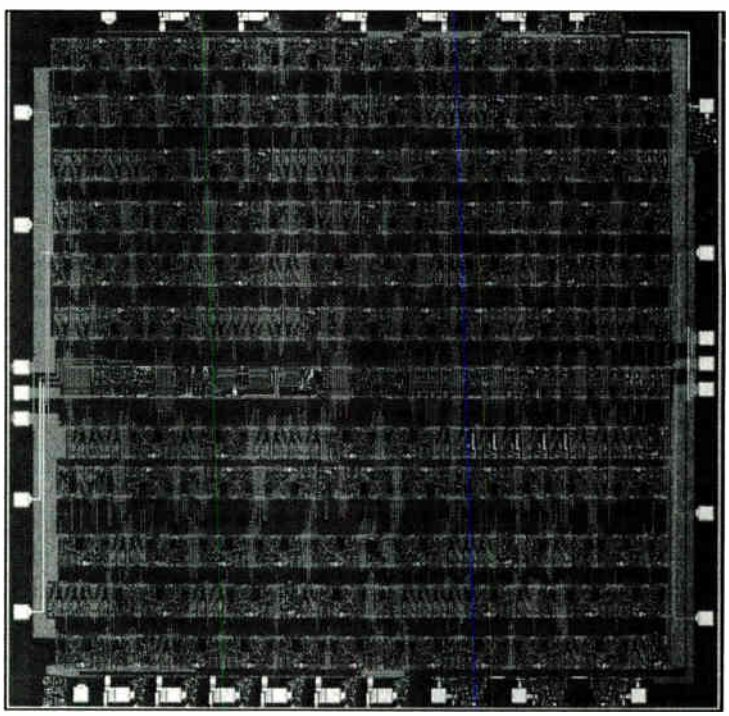
The process achieves a tenfold increase in density over existing linear bipolar approaches without sacrificing speed. The supply voltage, breakdown voltage, current density, and other key specifications are well above the minimums required for analog functions. And Fairchild engineers have been able to fabricate circuits with internal emitter-coupled-logic digital functions whose switching does not affect the noise figures of the analog circuitry.

LFAST blends existing techniques into a process combining highly doped buried layers with thin epitaxial layers, plus an unconventional isolation method with self-aligned processing. It also features composite masking and platinum silicide metal interconnection.

Before LFAST, any process capable of producing linear circuits with enough dynamic range to be useful in practical analog applications had to sacrifice the density required for large-scale integration, says Kulwant Egan, manager of bipolar process development. Moreover, few digital processes, either bipolar or CMOS, bring together the elements needed to fabricate high-performance operational amplifiers, comparators, multiplexers, and other linear functions—nor do these processes operate at sufficiently high supply voltages, he says. In addition, most digital processes cannot be used to fabricate the fast-switching pnp transistors, high-value matched transistors, or precision capacitors needed in many high-performance applications.

With LFAST, high-performance applications needing both high density and high performance—such as data-acquisition systems, computer peripherals circuits, and communications ICs—no longer require discrete linear components or multiple hybrid circuits to fill key system sockets, says Surinder Krishna, manager of advanced technology development.

Fairchild designers aimed at optimizing the linear portion of LFAST while maintaining the density and performance of the digital portion. "Of course, some sacrifices had to be made, and the

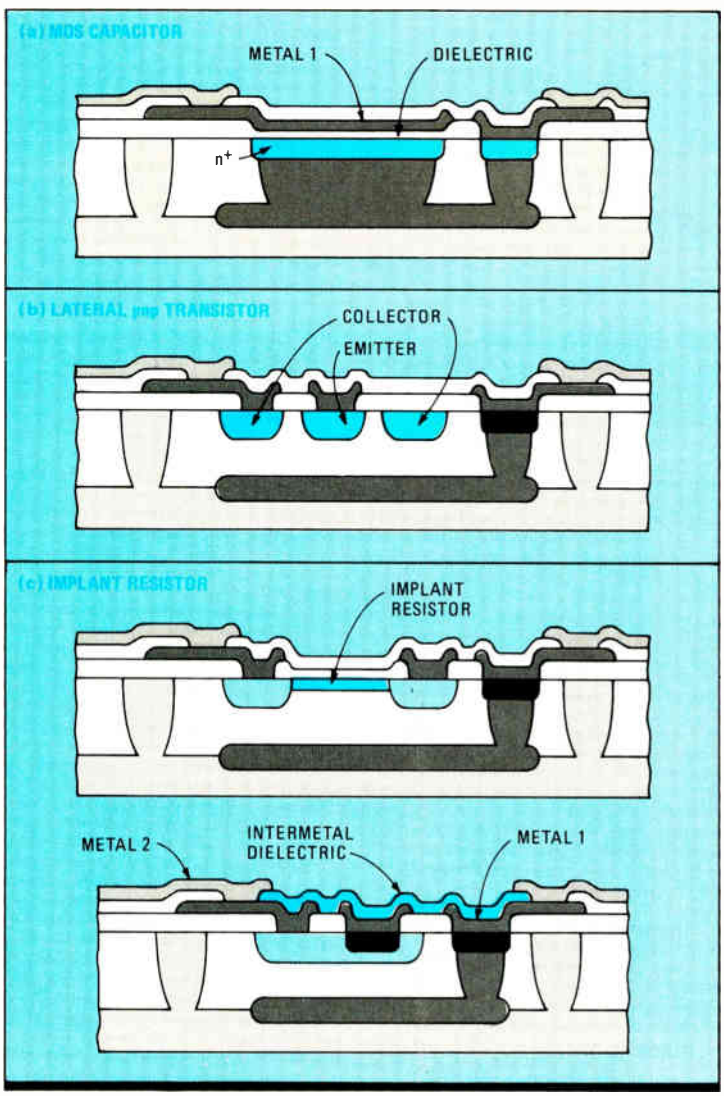


1. QUICK CHIP. Built with the LFAST linear bipolar process, the μA2490 data separator/encoder-decoder chip is capable of transmission rates up to 25 Mb/s.

LFAST TRANSISTORS WITHSTAND HIGH VOLTAGE		
	npn	Lpnp
LV_{CEO}	15 – 19 V	19 – 27 V
BV_{CBO}	33 – 39 V	33 – 39 V
H_{FE}	60 – 100	55 – 100
f_T	1.9 – 2.5 GHz	40 – 50 MHz
V_A	55 – 70 V	35 – 55 V

ECL portion of LFAST should not be compared with a process dedicated to digital ECL," says Egan. "But while LFAST ECL is not fully optimized, it offers respectable specifications." Typical gate delay is 1.8 ns at a 200-μA current level, and this improves to 1 ns at a current of 1 mA. The ECL devices in Fairchild's CLASIC, or custom linear application-specific IC, cell library do not operate at the high levels of standard ECL. They are characterized for lower-current operation to permit operation with linear devices.

LFAST is already used internally at Fairchild to build a range of standard and semicustom mixed analog/digital products, Krishna says, including a data separator/encoder-decoder (see fig. 1), a data-line interface family, a series of advanced Winchester-drive chips, and several high-performance comparators. In addition, the process will be used to make a range of custom and semicustom CLASIC circuits. "It is now possible to create custom LSI devices by selecting analog functions from a cell library," Krishna says.



2. INSIDE LFAST. This cross section of a chip fabricated in the LFAST process shows the structure of (a) a MOS capacitor, (b) a lateral pnp transistor, and (c) an implanted resistor.

LFAST is able to use tiny transistors without sacrificing performance or power-handling capacity, Krishna says. The transistor density of LFAST is more than 10 times that of conventional 10-μm to 15-μm bipolar processes: an LFAST transistor occupies about 1,100 μm^2, compared with 16,000 μm^2 for devices found in standard linear components. The process also incorporates Schottky diodes constructed with the usual platinum silicide materials. Its high-valued resistors, however, are anything but conventional, since they result from a unique implanting method. And the thin oxides that are used allow the construction of feedback capacitors for on-chip op amps.

LFAST fills a number of voids in conventional semiconductor processes that attempt to mate analog and digital circuitry, says Egan. For example, the supply voltage at which the linear devices operate poses a problem. To obtain reasonable dynamic range, the supply voltage must be greater than the 5 V used for the logic portion; at least 15 V is required. "To run at this level, conventional processes rely on stacking 5-V transistors—a risky procedure, since it is difficult to guarantee that phase relationships among the various voltages on the chip will not produce levels that exceed the breakdown voltage of individual transistors," says Egan.

LFAST, on the other hand, is a true 15-V process: all transistor breakdown voltages are 15 V or greater (see table). "What's more, LFAST does not rely on thicker, deeper junctions or wider spacings to ensure the breakdown voltage," says Krishna. "If it did, the process would no longer be suitable for building LSI digital logic on the same chip."

Current density of the LFAST transistors for peak f_T is 7,000 A/cm^2, compared with 500 A/cm^2 for conventional linear bipolar transistors, which means it is not necessary to increase the area of the transistors to boost their current-handling capability. With pnp transistors having a gain-bandwidth product of 40 to 45 MHz, LFAST devices are 15 to 40 times faster than any similar linear structures. And when used to fabricate digital transistors, LFAST can yield structures with typical gate delays of 1 ns at 1 mA. In LFAST, highly doped buried layers coexist with a thin, low-temperature-deposited epitaxial layer, giving the process its high packing density.

For op amps having a wide dynamic range, LFAST optimizes both the supply voltage—ampli-

fiers can swing to 15 V—and the equivalent noise voltage. To pull ac signals out of noise, LFAST op amps are specified for a noise voltage of just 1 nV/(Hz)$^{1/2}$. On the dc side, an amplifier must provide a very low input offset voltage, V_{OS}. Conventional op amps offer V_{OS} specifications of 1 to 10 mV, but Fairchild designers aimed for 1 mV or less with the LFAST process. "Actually, the offset-voltage parameters came out better than expected, ranging between 0.5 and 0.6 mV," says Krishna. It is important to hold V_{OS} as low as possible, since an op amp with a gain of 1,000 amplifies a 10-mV V_{OS} to 10 V, driving itself into saturation.

SMALLER AND FASTER

A key factor in the gain of an amplifier is the Early voltage, the voltage needed to remove the charge from a transistor's base to reach zero current. When the collector-to-base voltage increases, the base width is reduced; this alters the output characteristic by changing the collector-to-base voltage. Early voltage and output impedance are closely related: the larger the voltage, the greater the output impedance. LFAST amplifiers exhibit a large Early voltage, because high-impedance amplifiers also happen to be high-gain amplifiers. A large Early voltage also improves an amplifier's common-mode-rejection ratio.

In general, an LFAST-implemented line driver or receiver is about 20% faster and consumes only one-fourth the power of a conventional single-chip IC. And with LFAST's smaller transistor size and 4-μm design rules, an ASIC version is about 10 times as dense as its IC counterpart. An LFAST device can dissipate up to 1 W, but greater power dissipation is possible; the tradeoff is usually a larger package having greater heat-dissipation capability. Egan says LFAST is the first process to apply high-performance digital fabrication techniques to linear devices (see fig. 2). For example, the low-temperature epitaxy growth is borrowed from digital-device construction. The problem, he says, is that the heavily doped buried layer must coexist with the thin epitaxial layer. Ordinarily, the buried layer moves into the epitaxial layer while the latter is grown. However, the low-temperature growth prevents movement of the buried layer during the epitaxial-growth step.

At the first mask level is a buried layer, over which is grown a thin epitaxial layer at low temperature. A composite masking technique is then used to define isolation islands, base islands, and the isolation sinker, all of which are self-aligned. The self-aligned regions of p^+ isolation, n^+ sinker, and p base give LFAST its high packing density. The three regions are implanted, along with the n^+ emitter.

Prior to implanting the emitter, however, a field oxide must be grown over it. Then the emitter is opened to allow implanting to take place through the emitter. The structure is then annealed in nitrogen, yielding a so-called washed emitter that serves as a self-aligned contact.

The result is that, in addition to their extremely small size, LFAST transistors operate at a current density of more than 10,000 A/cm^2 when the beta value—the ratio of the change in collector current to the corresponding change in base current—is at its maximum value. This is important for small-geometry transistors, says Egan, since it guarantees that the device will maintain its gain even at large collector currents. □

For more information, circle 481 on the reader service card.

WHY FAIRCHILD RUNS LFAST BIPOLAR ON ITS CMOS LINE

The primary aim that Surinder Krishna and Kulwant Egan had when they started the LFAST project two years ago was to develop a linear bipolar process that could match the density of linear CMOS but would not sacrifice any of bipolar's performance advantages. Krishna, 46, is manager of advanced technology at the Mountain View, Calif., company, and Egan, 36, is manager of bipolar process development in the advanced technology group.

What they came up with is a process that uses many of the same steps as CMOS. Indeed, parts being fabricated with LFAST are run on the same line as Fairchild's double-polysilicon CMOS process, and achieve the same yields, Krishna says. Moreover, many of the mixed analog/linear parts fabricated on the line to date have about the same die size.

The key to LFAST is a modular approach to processing, in which a basic set of process steps are developed to achieve a specific set of performance goals and then frozen, says Krishna. "Unlike traditional approaches to processing, where steps and parameters are modified to meet the needs of the circuit designer, LFAST was developed with exactly the opposite philosophy in mind," he says. "To achieve various levels of performance and density, we subtract and add steps or modules to the [core] process, but we leave the basic parameters untouched," adds Egan.

LFAST TEAM. Krishna (l.) and Egan squeezed linear bipolar performance into CMOS density.

Krishna graduated from the University of Edinburgh, UK, in 1963 with MSEE and BSEE degrees. After stints at Marconi Research Laboratories in Essex, UK, General Electric's Research Laboratory in Schenectady, N.Y., and Westinghouse Research Center in Pittsburgh, Pa., he joined National Semiconductor Corp. in Santa Clara, Calif., in 1979. There he met Egan, who had been at National since 1975 after graduating from San Jose State University with an MSEE.

The close working relationship has continued at Fairchild, where Krishna started in 1981 as device engineering manager. Egan followed in 1982 as manager of bipolar process development.

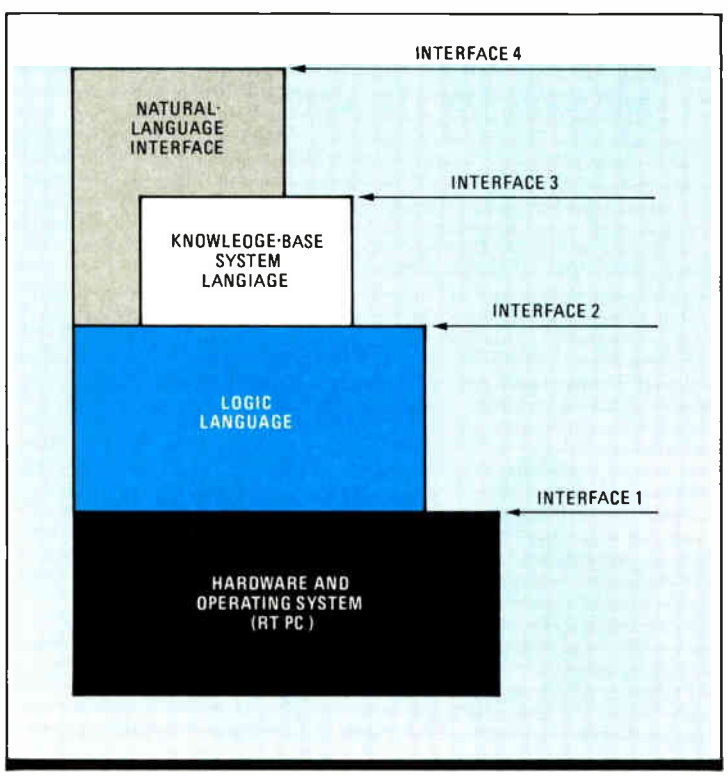
PROLOG COMPILER IS KEY TO IBM-JAPAN AI RESEARCH

IBM Japan Ltd.'s Tokyo Research Laboratory is developing an optimized Prolog compiler that could play an important role in artificial-intelligence work stations. The compiler runs on an IBM RT PC enhanced with experimental versions of two other key AI work-station components: a multiwindow user interface and a new operating system.

Tetsunosuke Fujisaki, the lab's software technology manager, chose Prolog over the most commonly used language for AI, Lisp, because "I have a feeling that the research phase of Lisp has ended. For Prolog, there is much to be done, including language specifications and machine architecture."

Because the project's current Prolog compiler is still experimental, it lacks many functions, among them run-time check, garbage collection, and a large number of built-in predicates. But in a benchmark test with basic predicates only, it achieved a maximum speed of 87,000 logical inferences per second for a simple append operation, which exceeds the value on existing dedicated Prolog machines.

The Prolog compiler for this machine is based on the instruction set of an abstract machine proposed in 1983 by David H. Warren, the developer of DEC-10 Prolog. The IBM-Japan researchers chose the Warren abstract machine because they were familiar with it, not because it offered any performance advantages over other schemes. In fact, Warren's proposal was for a machine dedicated to symbolic processing, and it is not necessarily suited for general-purpose machines.



1. HIERARCHY. The plan for user and programming interfaces of the AI work station has only been completed up to Interface 2.

The Prolog source code is ultimately compiled into RT PC object code, but it is optimized numerous times in intermediate steps to improve execution performance. To prepare for optimization, the researchers added two declaration types to the mode declarations previously used in the source code. The no-trail declaration simplifies the processing of predicates that do not require backtracking. Data type declarations declare for the various parameters of the predicates what type of data they will input or what type of output data they will handle.

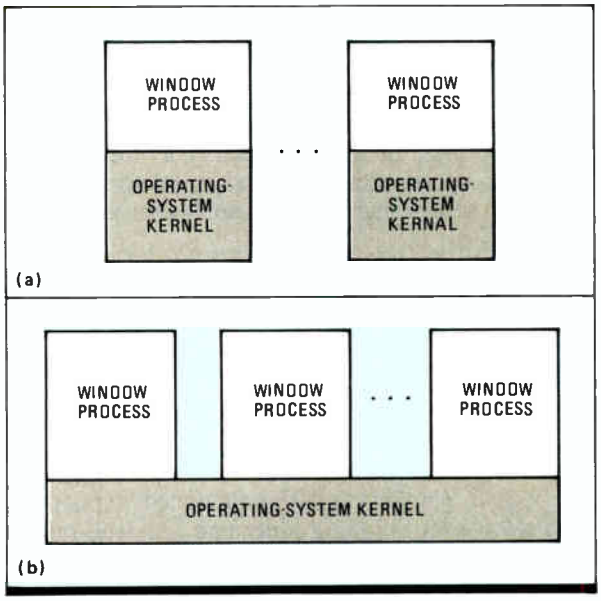
The Prolog source code is first converted into the Warren intermediate language based on the Warren abstract machine. Data type and other declarations are used for simultaneous optimization of Prolog language dependencies. Next the Warren intermediate language program data flow is analyzed, and optimization independent of the target machine is performed.

The Warren intermediate language code is then converted into PL.8 machine-dependent code, at which time machine-dependent optimization is performed. For example, code is created that takes into account factors such as the necessary number of cycles for tag tests or memory accesses. Finally, compilation is done from PL.8 to machine code.

In addition, the researchers at the Tokyo lab intend to port software from the IBM System/370 software to the RT PC, including the Prolog debug environment Proedit 2, the object-oriented knowledge representation language Spool, and the Ink environment on top of which Spool runs.

The RT PC is an engineering work station with a 32-bit reduced-instruction-set computer microprocessor [*Electronics*, May 5, 1986, p. 34]. The laboratory chose the new IBM machine primarily for cost reasons; it was less expensive to use an existing general-purpose machine than to developing a special-purpose machine.

The RT PC RISC architecture includes a 40-bit-address, single-level, nonhierarchial memory system in which each process has a 32-bit address that the memory management unit converts to a 40-bit address. The 4 most significant bits of the 32-bit process address are used to select one of sixteen 12-bit registers. These 12 bits are added to the 28 remaining least significant bits to obtain a 40-bit virtual-memory address. Since the maximum main memory of the RT PC is 16



2. WINDOW PROCESS. The operating-system kernel has a common portion in every process as part of the window manager.

Mbytes, the MMU converts the virtual address to a 24-bit real-memory address.

The advantage of a single-level memory is easier programming. Files and main memory can be placed in the same space, and file input/output does not have to be considered a different kind of operation. Common address space among processes can be used effectively in the development of AI application programs.

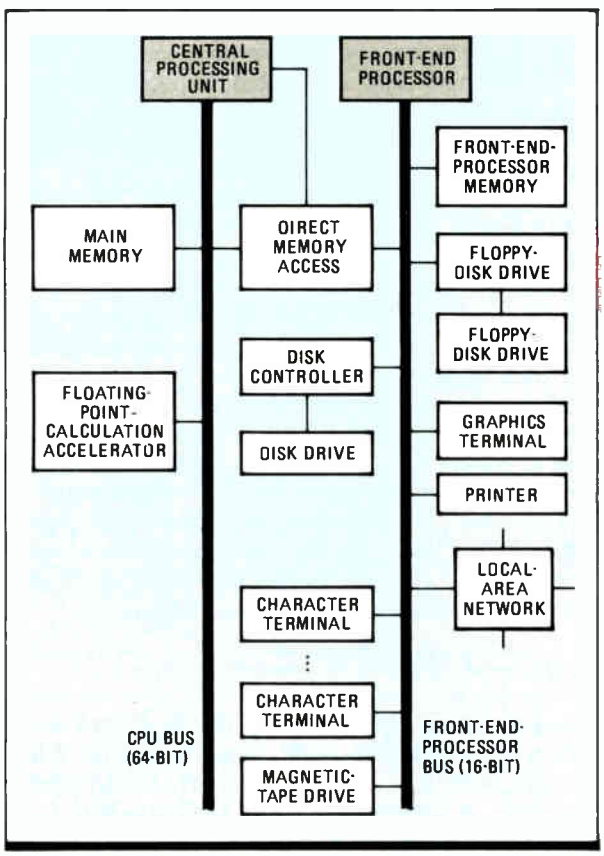
The plan for the user and programming interfaces of the AI work station (see fig. 1) has been only partially implemented. It is currently completed only as far as the logic language on Interface 2. Above this, the knowledge base, the system language, and natural language interfaces will be implemented and tested.

The operating system used is the AIX OS developed at IBM's Watson Research Center in Yorktown Heights, N. Y. The kernel of this operating system has a common portion in every process (see fig. 2), included as part of the window manager. Fujisaki says that this configuration was selected because response is faster and overhead smaller. Processes running under control of Unix and other operating systems typically share one copy of the kernel.

An accurate evaluation of the compiler cannot be obtained because it does not have a complete array of functions. But the lab has taken the first steps toward building an AI work station with reasonable functionality on top of a general-purpose work station.

For more information, circle 482 on the reader service card.

TECHNOLOGY TO WATCH



'DUALING' PROCESSORS. ELIS's dual-processing system comprises a 64-bit CPU bus and a 16-bit front-end processor.

JAPAN'S NTT HAS WORLD'S FASTEST LISP PROCESSOR

A high-powered Lisp computer built by Nippon Telegraph & Telephone Corp.'s Electrical Communication Laboratories is now leading the pack as the world's fastest commercial Lisp machine. Called ELIS, the desktop computer can execute 1 million basic Lisp instructions per second, which is up to six times better than existing Lisp machines and minisupercomputers. It achieves this with extensive microcode for critical Lisp functions and a dual-processor architecture.

ELIS incorporates up to 128 Mbytes of main memory and a 540-Mbyte disk drive. Its multiple-paradigm programming language, Tao, was built upon Lisp and supports the Common Lisp standard. It also provides a logic language like Prolog and an object-oriented language like Smalltalk with which to write programs.

A microprogram-controlled machine, ELIS has a very large working control store: 64 Kbits of 64-bit words of writable control storage and a register stack of 32 Kbits of 32-bit words. These are both implemented in high-speed static random-access memory. Tao functions, written in microcode to speed up the interpreter, achieve

performance comparable to commercial Lisp compilers. Other functions are incorporated in a Common Lisp-compatible package. These functions are only about 10% of the total number of functions in Common Lisp, and the overhead is negligible. Although Common Lisp is a compiler-oriented language, preprocessing and other measures enable the Common Lisp interpreter to equal the performance of the Tao interpreter.

The ELIS system uses a dual processor-configuration with a central-processing unit and a front-end MC68010 microprocessor to control input-output processes (see figure). Peripherals are connected to the front-end processor, and the bus and front-end processor bus are connected through a direct memory-access channel. The system program and library routines for ELIS are mainly written in Tao, with some speed-critical portions in microcode. The front-end processing system software is mainly written in C.

For more information, circle 483 on the reader service card.

TECHNOLOGY TO WATCH

JAPAN'S ICOT TRIPLES SPEED OF ITS INFERENCE MACHINE

Tokyo's Institute for New Generation Computer Technology is speeding ahead with its second sequential inference computer. The PSI-II, being developed by ICOT, Mitsubishi Electric Corp., and Oki Electric Industry Co., uses revised software and 8,000-gate CMOS gate-array technology to attain an execution speed in the KL0 machine language of 100,000 logical inferences per second (100 klips), on the average, three times the speed of the original PSI.

ICOT, which is charged with developing Japan's fifth-generation computer technology, will use PSI-II as its software development machine, both for single- and parallel-processor systems. The new machine can serve as the building block in a system of 16 to 64 inference machines. The processor was completed at the end of March; the system is to be finished by the end of the year.

COMPARING THE TWO ICOT INFERENCE MACHINES

	PSI	PSI II
Maximum performance	about 33,000 logical inferences per second	about 100,000 logical inferences per second
Machine language	KLO (based on DEC 10 Prolog)	KLO (based on Warren instruction set)
Processor technology	high-speed Schottky TTL	CMOS gate array Am29300 series, etc.
Processor board count	12	3
Cache	4-K words x 2	4-K words
Real address space	24 bits	26 bits
Maximum main memory	16 megawords	64 megawords
Number of processes that can be simultaneously generated	64	no limit
Branch dispatch memory	12 patterns	32 patterns
Processor cycle time	200 ns	200 ns
Word configuration	32-bit data 8-bit tag	32-bit data 8-bit tag
Operating system	Simpos	Simpos
Programming language	ESP	ESP

The PSI machines use their own operating system, called Simpos, and the extended version of the Prolog programming language ESP (see table). In the list-append function that is used with high frequency in Prolog, PSI-II reaches 300 klips.

Two changes from the original design tripled the inference speed. The Warren instruction set, first proposed as a Prolog instruction set in 1983 by David Warren, the developer of DEC-10 Prolog, was adopted as the new base for the machine language; and the architecture was reworked.

ICOT also took several steps to improve the execution speed of the code generated by the Prolog compiler. The speed of the built-in predicates was boosted by changing the way their parameters are stored in registers. The researchers streamlined the instruction that extracts the nth element from a list by reducing the number of microsteps from 17 to 13, and they eliminated unnecessary cuts. They speeded up mode selection by incorporating a preselection process that can select the node for execution based on parameter value.

The processor is built around nine 8,000-gate CMOS arrays and fits on three boards. Three internal buses are used: two source buses and one destination bus. The machine's 40-bit word has 32 bits for data and an 8-bit tag, two of which are used for garbage collection and six for identifying the data type.

Major changes in the second PSI are the expansion of the real address space from 24 to 26 bits and enhancement of the tag architecture. Main memory size was quadrupled to 64 megawords, or 320 Mbytes. Furthermore, multiple name space was adopted with logical space allocated to each process generated, increasing the number of processes from 64 in the PSI to no limit. □

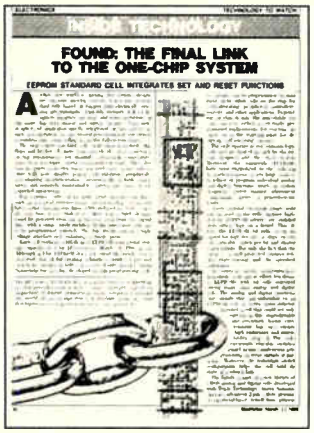
For more information, circle 484 on the reader service card.

The preceding three Technology to Watch articles were originally published in Nikkei Electronics, which is published by Nikkei-McGraw-Hill Inc., a joint venture of McGraw-Hill Inc., publisher of Electronics, *and Nihon Keizai Shimbun. They were translated by Charles L. Cohen.*

UPDATE: SIERRA'S EEPROM CELL MOVES INTO DESIGNS

Industry response to the Sierra Semiconductor Corp.'s single-bit, electrically erasable programmable-read-only memory has been "overwhelming," says Tom Reynolds, vice president of marketing and sales at Sierra Semiconductor. Since the EEPROM cell family's introduction about a year ago [*Electronics*, March 17, 1986, p. 30], the company has begun incorporating varying degrees of cells in the design of systems for about 10 to 15 customers. It has also talked seriously with at least 100 potential clients interested in using the Sierra approach. Moreover, efforts to make the nonvolatile memory-cell family available to users of a range of popular computer-aided-design workstations is approaching the final stages.

In addition, the company is moving beyond its initial family of single-cell EEPROMs and has developed a series of small EEPROM standard-cell arrays up to 200 bits in density, with no penalty in die size or performance. Also being added to the family are a set of high-voltage interface cells, which allow generation of both 5- and 18-V programming voltages on-chip or the use of an external 18-V source. In development is a set of EEPROM standard cells aimed at portable applications, which allow operation down to 3 V, as well as larger EEPROM cell arrays up to 4,000 bits.


FOUND: THE FINAL LINK TO THE ONE-CHIP SYSTEM

EEPROM STANDARD CELL INTEGRATES SET AND RESET FUNCTIONS

The cell family has already been adapted for the work station from Mentor Graphics Corp., of Beaverton, Ore.; beta-site tests are under way. Testing on versions for the workstation from Daisy Systems Corp., Mountain View, Calif., is expected to begin in April. General release is expected in April for the Mentor version and in June for the Daisy version. *–Bernard C. Cole*

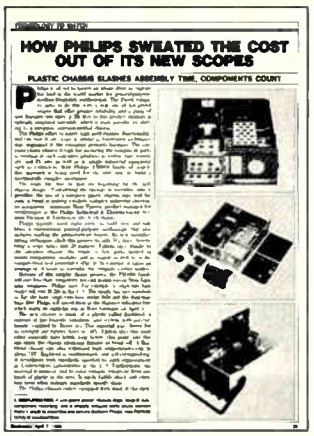
UPDATE: PHILIPS SCORES WITH LOW-COST SCOPES

A year after Philips announced its PM3050 family of 50-MHz oscilloscopes, it looks as if the $5.4 million that the Dutch company invested in its development is paying off, says Pieter Fips, product marketing manager for general-purpose oscilloscopes at the Philips Industrial and Electroacoustical Systems Division in Eindhoven, the Netherlands. Philips set out last year to grab the lead in the world market for general-purpose, medium-frequency scopes [*Electronics*, April 7, 1986, p. 39]. That ambitious goal has not yet been reached, Fips says, "but we have come a big step closer. It's turning out to be a big success."

A key to that success has been the fact that the Dutch engineers departed radically from conventional scope construction. They turned to a one-piece plastic chassis for mounting all component parts, betting that they could cut assembly time by up to 30 times for the 3050 family.

The bet has paid off. Fips thinks the single-chassis construction for the 3050 family puts his company years ahead of its competitors. The savings achieved with it are so encouraging that the firm may use the one-chassis concept for future instruments as well.

Building, testing, and calibrating the new models and stuffing the printed-circuit boards needed for them takes a bit more than five days, compared with about eight weeks for a conventional Philips scope. Computer-controlled components-sequencing for the pc boards and automated processes for components placing and soldering shorten the flowthrough. Automated testing and the use of click-fit mountings, snap-in fixtures, and stops and posts instead of screws, rivets, and metal supports also help. And the one-chassis concept means actual assembly takes only 20 minutes instead of around 10 hours for other scopes.


HOW PHILIPS SWEATED THE COST OUT OF ITS NEW SCOPES

PLASTIC CHASSIS SLASHES ASSEMBLY TIME, COMPONENTS COUNT

The savings help keep the scope's price low—$1,245 for the single-time-base PM3050 and $1,345 for the dual-time-base PM3055, which Fips says is less than most other general-purpose models. The low price, combined with such user features as a clear display and a microprocessor-controlled autoset key that automatically optimizes various settings, has been a big factor in the success of the 3050 family so far. "We have about doubled the quantity shipped," Fips says.

Actually, the company would have performed better had it not been for the drop in value of the U. S dollar. "That has given [market leader] Tektronix a big pricing edge on European markets with a low-cost scope it introduced last year," the Philips manager says. *–John Gosch*

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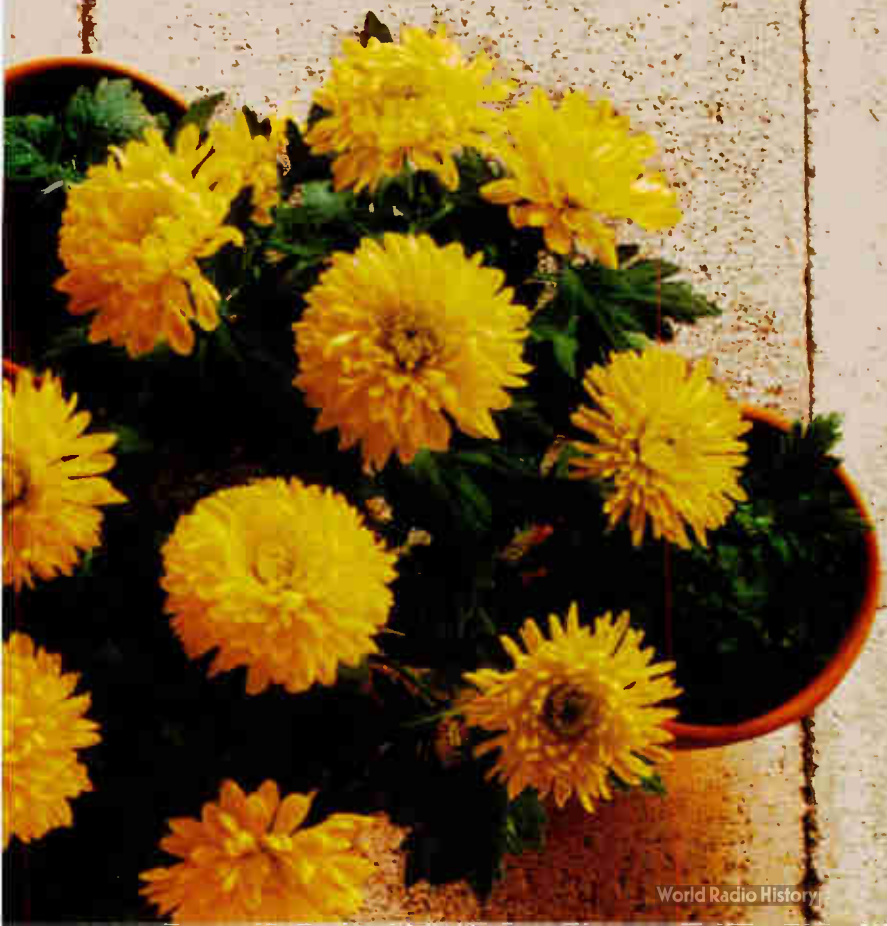

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Circle 77 on reader service card

A MAJOR FACELIFT STARTS FOR STRATEGIC RADAR NETS

Recent advances in solid-state phased arrays and power devices and in pulse compression and signal processing are reshaping U.S. defenses against aircraft and missile attacks

by Marce Eleccion

In a major revamping of its continental defense system, the U.S. Department of Defense has begun a multibillion-dollar program to replace or supplement its aging strategic radar networks with the newest radar technology. What's making this revamping possible is the application of state-of-the art electronics technology—both to update or replace decades-old radar systems and to provide the circuitry and computing needed to implement highly advanced systems.

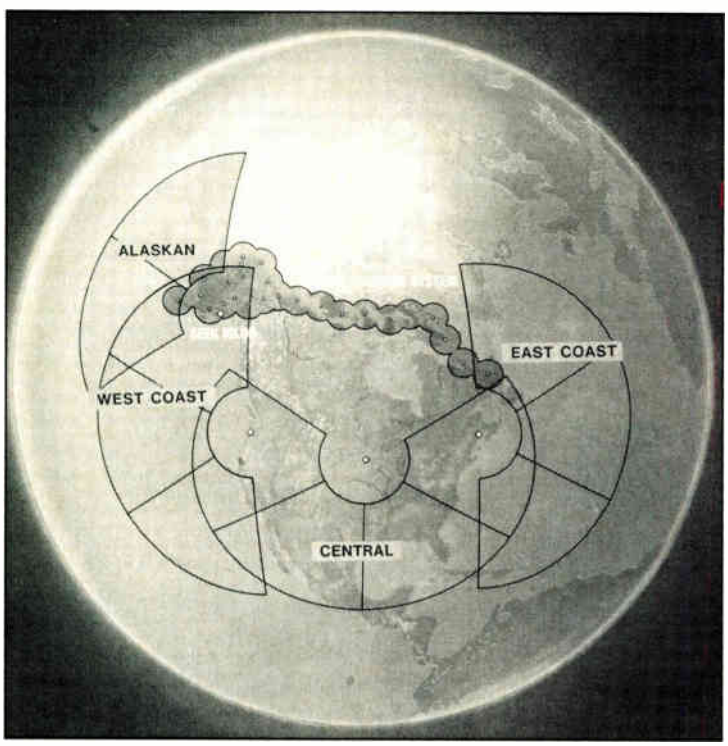
Playing major roles in the new radars are fully solid-state phased arrays that include solid-state power generation, pulse-compression techniques, and digital signal processing. Other factors expected to influence future radars are monolithic microwave integrated circuits; adaptive arrays; fiber optics; and new VLSI fabrication methods, some of which are derived from the Pentagon's Very High-Speed Integrated Circuits program. Not only do these technologies greatly enhance radar performance, versatility, and reliability, they also make systems that are smaller, lighter, and less power-hungry. Above all, today's systems can be built at dramatically lower costs.

As a prime thrust of the revamping, the U.S. is installing a new radar system based on over-the-horizon backscatter technology, which can detect objects at far greater distances than conventional radars can. A related radar system, the North Warning System (see fig. 1) is replacing the Distant Early Warning, or DEW, Line that has stretched across northern Canada since the mid-1950s. These radars search for aircraft and cruise missiles that fly in the atmosphere.

The DOD also is about to begin its second upgrade of the Ballistic Missile Early Warning System, or BMEWS, which was built in the 1960s to detect high-flying missiles reentering the atmosphere from the north. And it is modernizing the Perimeter Acquisition Vehicle Entry Phased-Array Warning System (PAVE PAWS), which watches the eastern, western, and southern perimeters of the U.S. PAVE PAWS, which dates only from the early 1980s, is another system that searches above the atmosphere for intercontinental or submarine-launched ballistic missiles.

The most advanced radar of all is still under wraps. It is the Terminal Imaging Radar, which is part of the Reagan Administration's massive Strategic Defense Initiative.

One key existing radar is the Joint Surveillance System, or JSS, which monitors all airspace



1. GUARDIANS. The North Warning System, monitoring the electromagnetically noisy Arctic skies, will supplement four over-the-horizon backscatter radar systems.

within 200 miles of the North American continental borders for low-flying supersonic aircraft and cruise missiles. Developed and built by Hughes Aircraft Co.'s Ground Systems Group, Fullerton, Calif., the JSS integrates existing U. S. Air Force and Canadian surveillance radars with the enormous coverage afforded by the Federal Aviation Administration's civil air-traffic control system. The JSS saves $100 million a year in operation and maintenance costs over the Semi-Automatic Ground Environment and Back-Up Interceptor Control (SAGE/BUIC) systems it replaced, says a Hughes Aircraft spokesman.

However, despite the extensive coverage provided by JSS, its 200-mile coastal range was not considered adequate for early warning against the new breed of low-flying aircraft and cruise missiles. As a result, two major programs are under way: an over-the-horizon backscatter (OTH-B) radar network designed to detect low-flying missiles and aircraft approaching the continent from the east, west, and south, and the North Warning System, aimed at northern approaches.

UPGRADING ATMOSPHERIC SYSTEMS

Comprising 12 sectors, each radiating 60 degrees outward from the boundaries of the U. S., the OTH-B effort represents the first major attempt to detect targets by reflecting high-power, high-frequency signals off the ionosphere and using the returning backscattered data to determine target range and bearing. In each sector, twelve 100-kW transmitters bounce 5-to-28-MHz signals off ionospheric layers 50 to 250 miles above the earth's surface. OTH-B radars can detect objects at a range of 500 to 1,800 nautical miles.

To avoid signal interference, each OTH-B radar is separated into transmit and receive sites situated some 50 to 100 miles apart in a technique known as bistatic radar. A third site serves as an operations center to process signals, control radar activities, and provide accurate target discrimination.

OTH-B technology has been available for more than a decade, says program director Col. James A. Lee of the Air Force, but "only recently have the signal-processing and computer capabilities been developed to make such a system practical." OTH-B systems use Doppler radar, which discriminates targets by speed. They also must be able to separate the enormous amount of civilian traffic (both planes and ships) and environmental clutter (birds and large waves, for example) from true incoming threats. Such discriminatory capabilities and the complex modes of OTH-B operation require great computational power.

The OTH-B network is grouped into the East Coast Radar System (ECRS), the West Coast Radar System (WCRS), the Central Radar System (CRS), and the Alaskan Radar System (ARS). The ECRS consists of three sectors in Maine: three transmission sites in Moscow, three receiver sites near Columbia Falls, and an operations center at the Air National Guard base in Bangor (see fig. 2). Being built by General Electric Co. under a $550 million contract issued by the Air Force in June 1982, the ECRS provides 180° coverage and is to be completed by 1988.

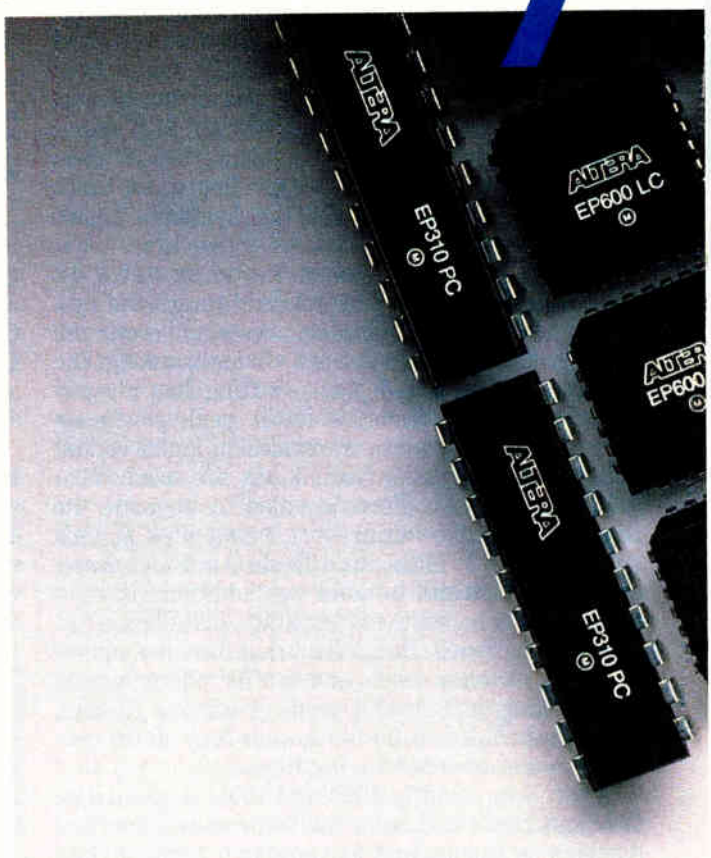
The WCRS, which also has three sectors, will provide 180° coverage from three transmitters in Buffalo Flats, Ore.; three receivers in Rimrock Lake, Calif.; and an operations center at Mountain Home Air Force Base, Idaho. Construction on the operations center began in July 1986, and work on the transmit/receive sites begins this spring. A $315 million contract for hardware, installation, and testing of WCRS was awarded to GE last December.

Although funding for the other two OTH-B systems has yet to be approved by Congress, $600 million for the CRS and $450 million for one sector of the ARS have been requested by the Air Force in the fiscal 1989 budget. Four sectors, plus an operations center at Grand Forks Air Force Base, N. D., have been slated for CRS, which will provide 240° southern coverage. Two sectors have been planned for ARS, which will face 120° northwest and will have its operations center at Elmendorf Air Force Base, Alaska.

It has been impossible to design an OTH-B system that can operate effectively to the north, because of electromagnetic disturbances in the Arctic atmosphere, as manifested by the aurora borealis. To span the northern approaches between the eastern and Alaskan OTH-B systems, work has begun on a series of 52 radars across the outer edges of Canada: the North Warning System, or NWS. Designed to replace the aging DEW Line and to supplement the Air Force's 13 SEEK IGLOO solid-state radars built in Alaska in 1979, the NWS will consist of 13 minimally attend-

2. OTH-B OPERATIONS. The first sector of the east coast OTH-B system in Maine should be fully operational late this year. Display and processing are conducted at this operations center in Bangor.

Quantity



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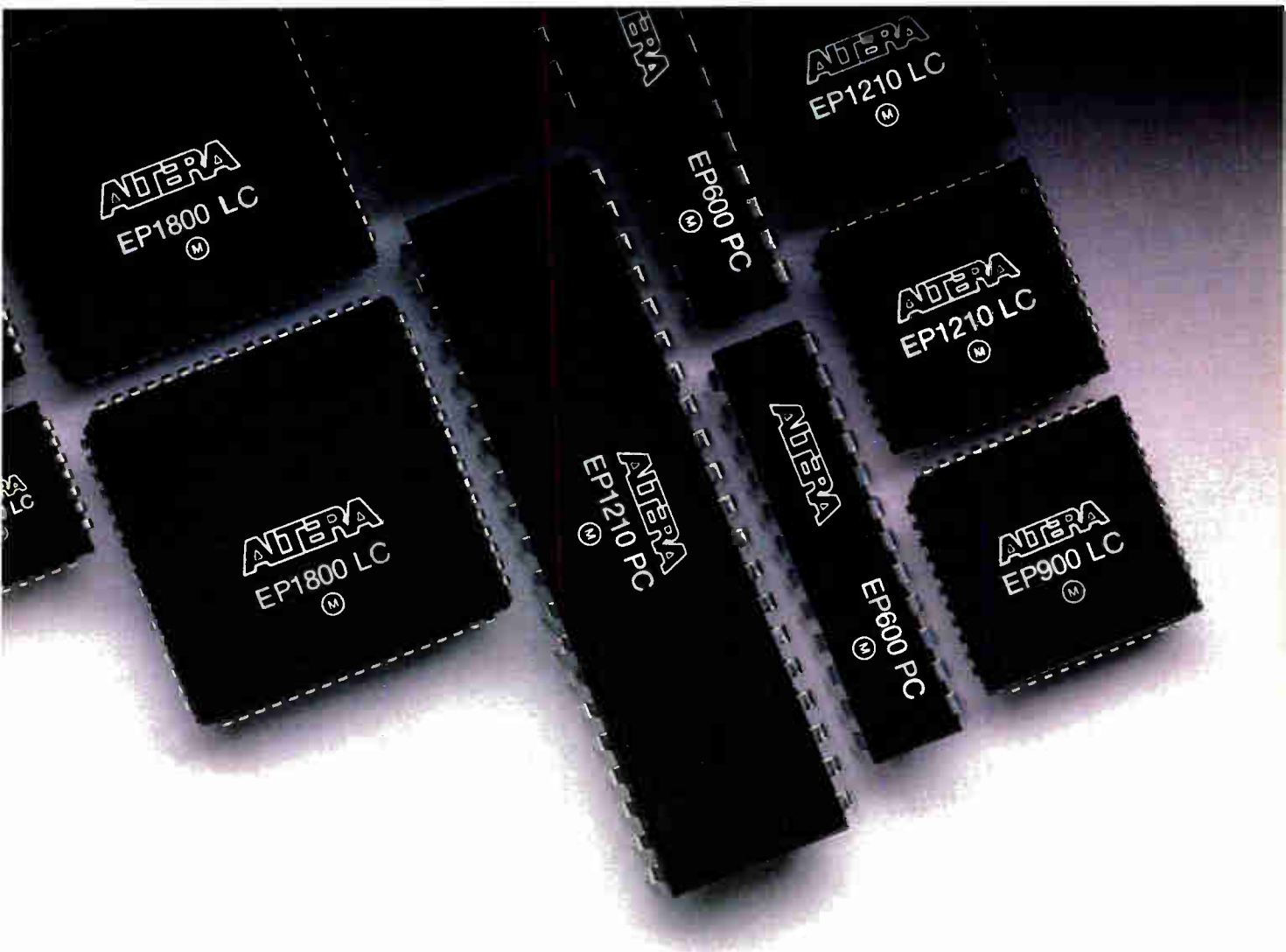


VHSIC FINALLY BUILDS A HEAD OF STEAM

Phase 1 got off to a slow start, but the controversial Pentagon R&D program is now rapidly moving the advanced chips into military hardware

by Larry Waller

The Pentagon's controversial and expensive Very High Speed Integrated Circuits project has finally gotten its act together. Following some midcourse disappointments with the program, on which government and the industry have spent more than $1 billion in its first seven years, 1986 saw VHSIC make real progress toward the primary goal: placing advanced chips into new designs or improving existing designs by retrofitting the chips. At the same time, technological fallout is adding to the program's benefits (see report card, below).

There was a great deal of early enthusiasm for VHSIC, but that had worn thin because of delays in delivering samples of the chips developed in Phase 1 for evaluation. One result of these lags was that sockets earmarked for VHSIC devices were filled instead with semicustom gate arrays. The picture changed rapidly in the past year. Managers of 37 electronic weapons system programs for all three branches of the armed services have committed to the chips, under heavy prodding from the Department of Defense. And the best times for VHSIC are ahead. For example, none of the current contracts covers the huge Air Force Advanced Tactical Fighter program, for which VHSIC technology will likely be used in a big way.

The brighter outlook comes none too soon for VHSIC supporters, who have had little to crow about in recent years. "During 1986, a number of significant milestones were passed," reports E. D. (Sonny) Maynard Jr., who has directed the VHSIC Program Office, in the office of the Undersecretary of Defense Acquisition, since 1982. Maynard was recently promoted to director of computer and electronics technology, but he still oversees VHSIC.

The big news is that the 1.25-μm chips from Phase 1, which started in 1981 and is now winding down, are now in good supply from six contractors. Furthermore, "the performance advantages of the chips have been demonstrated in operational systems," Maynard says. Now, lessons learned from patch-

REPORT CARD: GRADING THE VHSIC PROGRAM

Subject	Grade	Comments
Insertion of high-performance VLSI in military systems	I	(Incomplete) Prototypes are just arriving on the scene. But prospects look good as the military becomes aware of the chips' potential
Actual design-ins	B	There has been a lag of up to two years in chip delivery; doubts about availability remain
Cutting weapons-systems development time	I	(Incomplete) It is too early to judge
Reducing custom-chip cost for military	B+	Even present lofty VHSIC-chip prices—$3,000 and up—are lower than custom ICs of the past; prices will drop sharply if volumes rise as planned
Pushing the state of the VLSI art	B+	Many advances have been made
Bipolar processes	A	The commercial state of the art has been leapfrogged; VHSIC serves as a process driver
MOS processes	B+	VHSIC has paced commercial development
Architecture	C+	An early compromise on general-purpose structure led to an extensive redesign to meet specific requirements
Feature sizes	A	For now, military devices are equal to production commercial devices
Computer-aided-design tools	A	Users claim efficiencies higher than those gained in the commercial world. The program could help set future CAD standards
Electron-beam lithography	D	The 0.5-μm line-width goal was probably too ambitious for the program's tight schedule
Manufacturing	B+	Yields are acceptable, after a slow start
Self-testing ICs	A	The program has been so successful in this area that it is being copied by commercial IC houses
Packaging	A	High-pin-count and surface-mount techniques have been developed by most suppliers

ing up Phase 1 have been cycled into the planning and structure of the more ambitious Phase 2 (see p. 91), which specifies 0.5-μm features.

Of particular interest to users is the fact that Phase 1 ICs from all six contractors are well on their way to being added to the Qualified Parts List for military procurement, says Maynard. The six are Honeywell, Hughes, IBM, TRW, TI, and Westinghouse.

Although the VHSIC insertion program is still in its earliest stages, most participants are confident it will be successful, given the strong backing of the DOD and the military systems manufacturers. But it is becoming clear that the VHSIC effort will have an even broader effect, as a technology and business driver for the U. S. semiconductor industry. Not only are useful technological advances emerging, but formerly uninterested companies are now seeking an eleventh-hour entrée to the VHSIC program. For example, Intel is qualifying its 80286 and 80386 microprocessors to Phase 1 requirements; National Semiconductor is offering a VHSIC foundry service; and systems maker Raytheon has invested $40 million in a new VHSIC-oriented Microelectronics Center.

The reason for the wave of interest is obvious to Dallas Burns, director of digital technologies at the research and development operation of Honeywell Inc.'s Solid State Electronics Division in Plymouth, Minn. The company is a prime contractor for VHSIC Phase 1 and Phase 2. "Just as important as specific VHSIC chips, the program has raised the technology stakes when it comes to competing in military chip markets," he says.

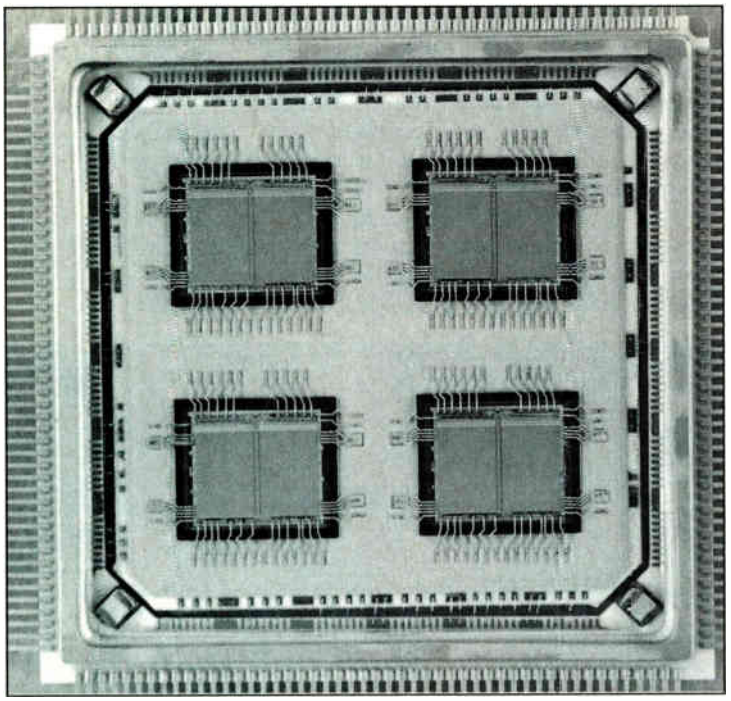
At Texas Instruments Inc., Dennis Best, manager of IC development for the Defense Systems & Electronics Group in Dallas, notes that VHSIC played a pivotal role in pushing commercial processing to the 1.25-μm region more rapidly.

VHSIC contractors and program managers offer further examples of the technological fallout:

- Advances in bipolar processing. VHSIC became the main bipolar driver during the early 1980s, says Best. Consequently, TI is benefiting in non-VHSIC devices, he says, and he thinks Honeywell is, too. The Honeywell chips "are generally considered to be the most complex bipolar logic chips ever produced," says Burns. To be able to fabricate these chips in integrated Schottky logic and current-mode logic, Honeywell developed its VHSIC 1.25-μm bipolar process with three layers of metal—a major improvement over the standard two layers.
- Computer-aided design tools. Developed by individual contractors, VHSIC CAD has achieved productivity levels beyond those attainable with commercial packages, the contractors say. At Honeywell, for instance, "one-pass success" through the CAD system is now considered the norm. Program managers at both IBM Corp.'s Federal Systems Division in Manassas, Va., and TRW Inc.'s Electronic Systems Group in Redondo Beach, Calif., report similar experiences.
- The VHSIC Hardware Description Language. The cornerstone for the Phase 2 design-automation system, the VHSIC HDL could become a standard for CAD. Not only does it help standardize software development among contractors, it is also precipitating many proprietary products. IBM, for instance, is producing an HDL version of all its VHSIC chips for a cell library. And Honeywell is working on a "behavioral VHDL synthesis system" that will generate a chip architecture from a processor's instruction set.
- Commercial fallout. Honeywell is energetically transferring its VHSIC experience to commercial developments, and TRW is marketing its line of 13 Phase 1 VHSIC devices. A prime example of commercial fallout is Motorola Inc.'s 32-bit 68020 microprocessor. VHSIC research in Motorola's Semiconductor Products Sector led to significantly increased performance, says a Motorola executive.

1. CLASS 10. A worker at Honeywell's facility in Colorado Springs, Colo., prepares to insert a 6-in. wafer in a thin-film analyzer.

All this is a sweet victory for those who have insisted all along that VHSIC was the answer to the lack of interest by semiconductor makers in the advanced digital signal processors needed by military systems. The program was set in motion in 1979, when the Defense Science Board judged that such action, financed and directed by the



2. A BARGAIN. Texas Instruments Inc.'s VHSIC 72-K n-MOS static random-access memory chip now sells for only $2.25.

DOD, was the only way to get the needed DSPs.

But, as has happened before in military R&D, to justify the program, planners set goals that were too lofty. VHSIC fell into this trap by attempting a task that was difficult to do in the time allotted. The program made its debut in 1980 with great fanfare, promising brassboard prototypes by 1984 and expecting to leapfrog the commercial state of the art in design and production. But, for instance, proven 1.25-μm bipolar processes did not even exist then.

The ensuing technical shortfall caused scheduling delays that were impossible to make up. Says one VHSIC program director, "it was a bad tactical error, ballyhooing too soon, then not being able to supply devices on schedule." Participants think two things saved the program: the impressive performance of the Phase 1 chips, and deft management by Maynard.

Maynard is credited with an accomplishment more common in the commercial arena than in military contracting. When he took control, Maynard recognized that key parts of VHSIC were in deep trouble.

One obvious gap was that the initial Phase 1 program did not provide for chip "interoperability," or device compatibility—a mix-and-match feature many users needed. "They were literally building a Tower of Babel for themselves," says one executive at a VHSIC contractor. To correct it, Maynard instituted a program to establish a functional standard that would enable VHSIC chips to work together. In Phase 2, IBM, TRW, and Honeywell have a bus interface, known as the Pi-Bus standard, that does this job.

Also, a yield-enhancement effort was started at about the same time, and is now paying off. IBM, for one, believes that this manufacturing research could lead to the most significant technology fallouts of all. The company points out that for signal-processing elements, VHSIC yields climbed from 1% or 2% all the way to 34%. And Honeywell says its 6-in. wafer front-end is now seeing 40% yields (see fig. 1).

Reacting to the arrival of commercial gate arrays, which had not been foreseen by the original VHSIC planners, VHSIC officials encouraged contractors to add them to their programs. One example is Hughes Aircraft Co., which developed a channelless array with up to 40,000 equivalent two-input gates. With such additions, VHSIC exhibited a flexibility rare to such programs, industry veterans agree.

Still, some problems persist. The prices of certain VHSIC chips are still high. The initial plans contemplated premium prices but figured that increased sales would keep prices within range of commercial levels. However, TI, for instance, has to sell its bipolar version of a processor meeting the 1750A military standard for $3,200 each. The company hopes that higher volumes by 1990 will bring that price down to $400 or $500. Thanks to the economies of scale of n-MOS production, TI has been able to price its VHSIC 72-Kbit n-MOS static random-access memory at $2.25 (see fig. 2).

DISPELLING RESISTANCE

The limited-payoff scenario is a classic one in military procurement and is used to justify reluctance to take the risks inherent in technology improvements. That resistance is exactly what VHSIC's organizers were aiming to dispel, recalls Richard D. DeLauer, who was one of the program's earliest champions, first at TRW Inc. and later at the Pentagon as assistant secretary for technology. "We wanted to make the services step up to [IC technology] and kept pounding on them to do it," says DeLauer.

Not surprisingly, Maynard believes that the fact that substantial progress has taken place stands out dramatically. "We have succeeded in raising [the military's] level of consciousness. There is a clear recognition that this semiconductor technology is something that they must pay attention to, and not just because [the Office of the Secretary of Defense] will be looking over their shoulders. They're also aware of VHSIC's vast increase in performance in terms of reliability and capability. To that degree, the program has been wildly successful."

VHSIC has indeed pushed military chip technology a big step forward. But it remains to be seen whether military procurement policies can be updated as well, to offer hope that VHSIC chips can be put to use before they become yesterday's technology. □

Additional reporting came from Wesley R. Iversen, J. Robert Lineback, Tobias Naegele, and Ron Schneiderman.

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TS2915A – Quad 3-State Bus Transceiver with Interface Logic
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TS2918 – Quad D Register with Standard and 3-State Outputs
TS2919 – Quad D Register with Dual 3-State Outputs

6800 FAMILY

EF6800 – 8-Bit Microprocessor
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EF6840 – Programmable Timer
EF6850 – Asynchronous Com. Interface Adapter (ACIA)
EF6852 – Synchronous Serial DATA Adapter (SSDA)
EF6854 – Advanced Data-Link Controller (ADLC)
EF6810 – 128 x 8-Bit Static RAM

68000 FAMILY

Device	Description	Clock Frequency	Clock Period (Max)	Processed or Qualified to
MKB/J68000	16-Bit MPU	6, 8, *10, *12.5 MHz 10, 12.5 (DESC)	250ns	JAN *Add'l JAN Versions to be Intro DESC 82021 Avail Q1 '87, MIL-STD-883
MKB68901	MFP	4, 5 MHz	100ns	MIL-STD-883
TS68008	16-Bit MPU 8-Bit DATA BUS	8, 10 MHz	500ns	MIL-STD-883 Version to be Intro Q1 '87
TS68230	Parallel Interface/Timer	8, 10 MHz	500ns	MIL-STD-883

SEMICUSTOM

Device	Process/Technology	Gate Count[1]	Processed or Qualified to
GB Series Gate Array	2 Micron, Double Level Metal, HCMOS	1,000 to 10,000 Gates	DESC Line certification JAN Qualification in Progress MIL-STD-883
GC Series Gate Array	1.2 Micron, Double Level Metal, HCMOS	1,000 to 10,000 Gates	MIL-STD-883 Qual in Progress

MEMORIES

Device	Description	Organized	Access Time	Processed or Qualified to
MKB/J4501	Biport FIFO	512 x 9	*65, *80, 100, 120, 150ns	JAN MIL-STD-883, *Add'l JAN Versions to be Intro
MKB41H67	CMOS	16K x 1	25, 35, 45ns	41H67 Avail Q2 '87
MKB41H68	Fast SRAM	4K x 4		41H68 Avail Q1 '87 MIL-STD-883
MKB4801A	Fast SRAM	1K x 8	70, 90, 120, 150ns	MIL-STD-883
MKB6116	CMOS SRAM	2K x 8	250ns	MIL-STD-883
MKB/J4116	DRAM	16K x 1	150, *200, *250ns	*JAN Version, MIL-STD-883
MKB/J4564	DRAM	64K x 1	150, 200ns	JAN, DESC 82010, MIL-STD-883
MKB/J45F56	DRAM	256K x 1	100, 150ns	DESC Line certification JAN Qual in Progress DESC 85152 Avail '87 MIL-STD-883 Avail '87

Note 1: 1 gate is the equivalent of a 2 input NAND or NOR gate.

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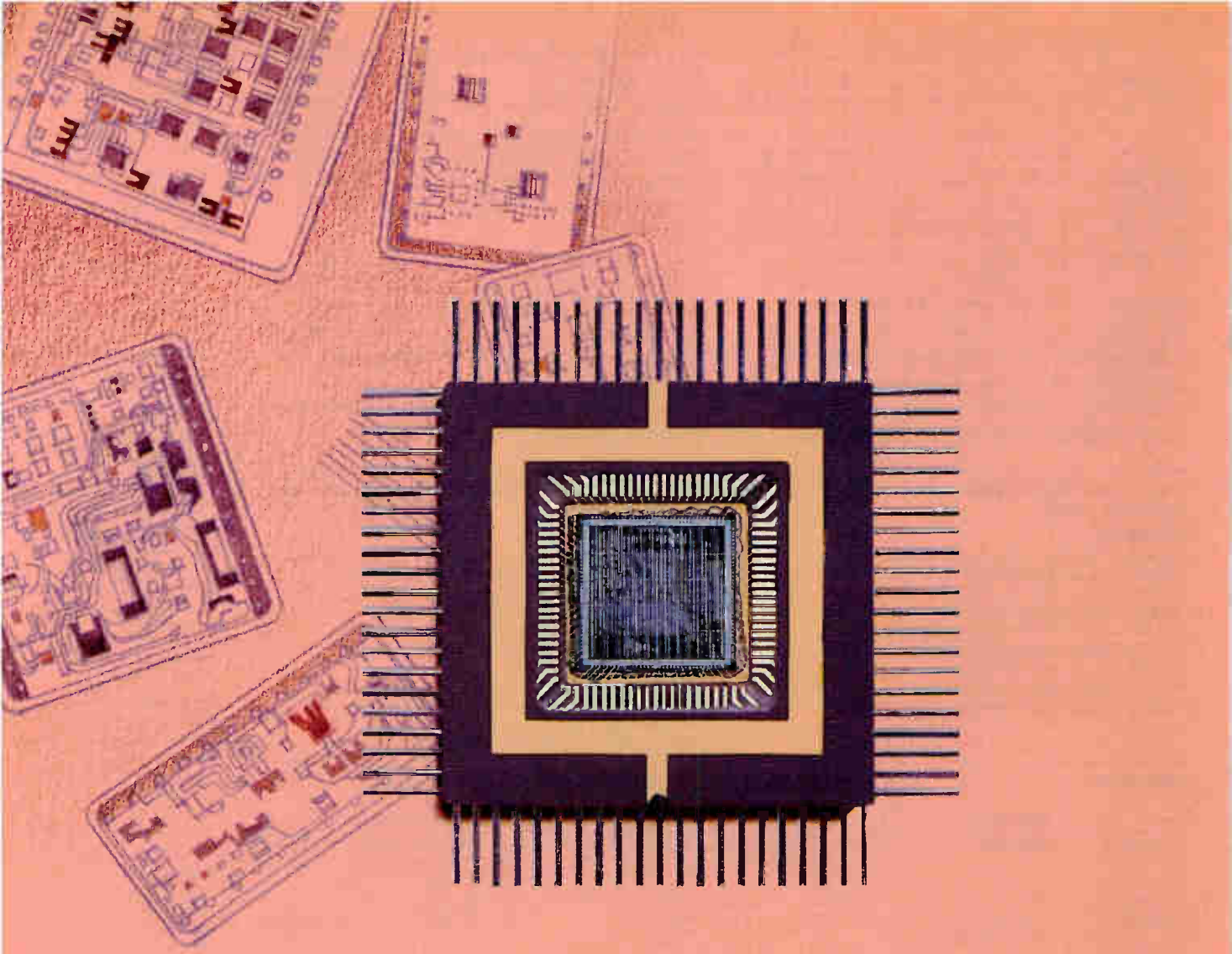

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VHSIC MOVES HEADLONG INTO THE SUBMICRON STAGE

Building on a successful Phase 1, Phase 2 is aimed at 0.5-micron geometries that clock at 100 MHz, chip densities of more than 500,000 devices, and pinouts over 300

by Jerry Lyman

Building on a slow but very successful Phase 1 effort, the VHSIC program is moving full speed ahead into its second phase. At least 16 companies can now turn out chips to meet the Phase 1 specifications for the Defense Department's Very High Speed Integrated Circuits; already they have produced some 40,000 chips. Phase 2 takes VHSIC from a technology of 1.25-μm geometries and chips with clock rates of 25 MHz to chips with 0.5-μm geomtries that clock at 100 MHz. In Phase 2, chip density is escalating from 100,000 devices to more than 500,000 per chip, and chip pinouts from 100 to more than 300.

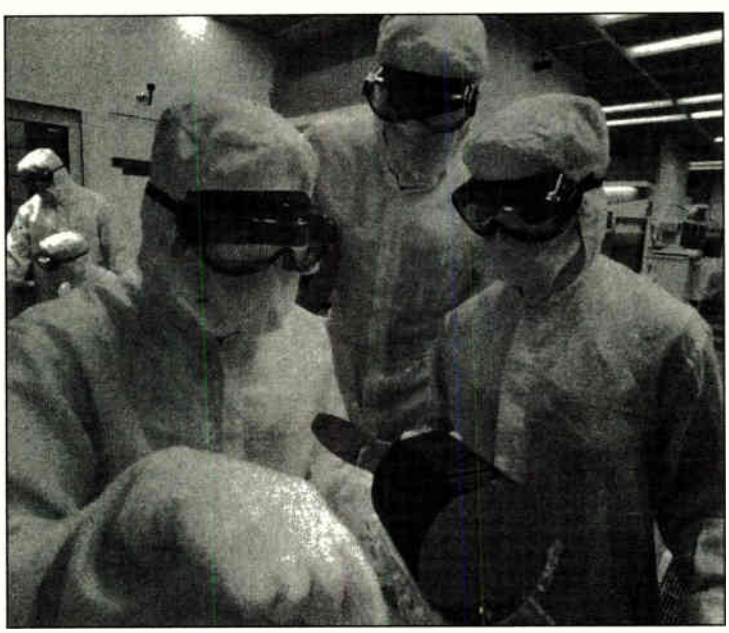
These performance breakthroughs flow from advances in IC processing, lithography, and packaging. Phase 2 has already seen the introduction of extremely large "superchips" with up to 34.7 million devices, including self-contained spares for chip self-repair; complex chips with built-in test; complex multichip packages; extensive use of electron-beam direct writing; and the introduction of three new high-resolution, high-throughput lithography tools based on e-beam, X-ray, and optical lithography.

So far, Phase 2 has avoided the delays that slowed Phase 1. The first phase is now making real progress (see p. 84). And the technology is spreading: the Pentagon's VHSIC Program Office reports that 10 chip makers besides the original six Phase 1 contractors can turn out 1.25-μm integrated circuits.

THREE PHASE-2 CONTRACTORS

VHSIC's second phase has only half the number of contractors Phase 1 had. The three participants are TRW teamed with Motorola, Honeywell, and IBM. TRW's Phase 2 family of devices is the most advanced of the three competitors, being based on the superchip concept and 0.5-μm CMOS technology. Honeywell, on the other hand, will make its VHSIC devices with a 0.5-μm four-layer bipolar process, but it is using the most advanced packaging technology in its multichip, multilayer module. IBM has chosen the most conservative approach by developing its ICs from a 1-μm CMOS process and then migrating to a final 0.5-μm version after design verification. IBM uses its established flip-chip and multilayer ceramic technology for its multichip module.

TRW has designed six superchips, of which three—a mass memory, a signal processor, and a convolver correlator—are being funded by the



1. VHSIC PROCESSING. TRW fabricates its VHSIC Phase I and II chips in its Class 10, vibration-isolated processing line in Redondo Beach, Calif.

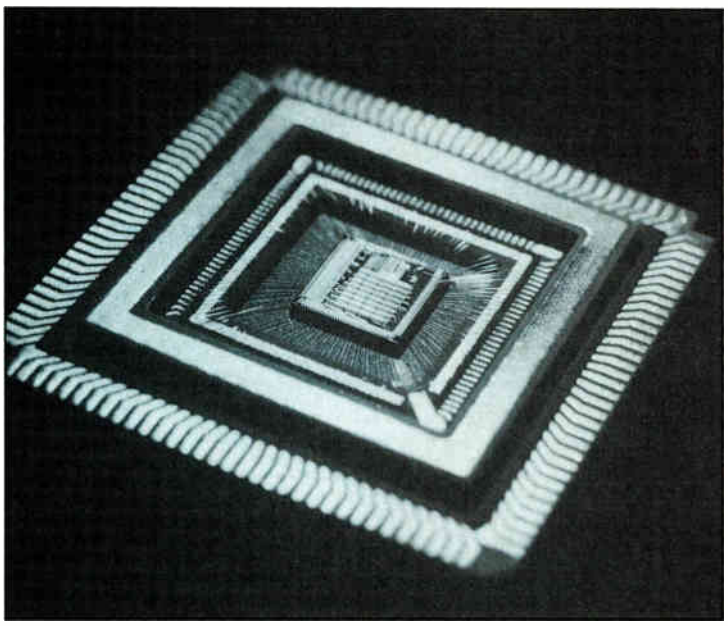
Pentagon [*Electronics*, July 10, 1986, p. 49]. It's up to the Defense Department to decide whether to fund the remaining three—a Fast Fourier transform chip, a data processor, and an associative processor. Originally, TRW had planned to implement two of the chips with a bipolar process and to use a CMOS process on four of the functions, but the company now has switched to an all-CMOS approach.

Phase 2 packaging is 'a very important part of the program in terms of achieving the high speeds needed,' says Honeywell's Anderson

The superchips will range from 1.4 by 1.4 in. to 1.2 by 2.4 in. in size and could carry up to 30 million devices per chip. By comparison, TRW's largest Phase 1 chip has 74,000 devices on a chip about a quarter of an inch on a side. A single 30-million-device superchip would be able to do the work of sixty 500,000-device chips typical of the VHSIC Phase 2 chips, or the work of more than 400 Phase 1 chips.

The superchips incorporate three key concepts that improve reliability and manufacturing yields: self-contained spare components, built-in testing, and software reconfiguration. This new approach to on-chip redundancy enables a superchip to identify its faults, bypass failed devices, and form new interconnections using spare devices, all without user intervention. With this method, TRW believes it can obtain chip yields of 20% to 50%—comparable with the best commercial results for LSI chips.

Another source of superchip reliability is the reduction in the number of interconnections. One superchip does the work of many Phase 1 chips, so interconnections between chips, the weakest point in any electronic system, are greatly reduced, as fewer chips are necessary.



2. FLATPACK. For Phase II, TRW will use a larger version of this four-sided ceramic flatpack with leads on 25-mil centers that was used in Phase I.

All of TRW's Phase 1 and 2 chips are being fabricated in its D1 facility in Redondo Beach, Calif. (see fig. 1), which is a vibration-isolated Class 10 IC processing line. Direct-writing e-beam lithography based on a Cambridge Instruments system is used to expose 0.5-μm details. TRW and Perkin-Elmer Corp. of Norwalk, Conn., are in the process of an acceptance phase for Perkin-Elmer's Aeble 150 direct-writing e-beam system. This unit is slated for pilot-line production of superchips.

The superchips will be housed in large single-layer four-sided flatpacks with up to 320 leads on 25-mil centers. This package is simply an extension of the same technology used on TRW's 132-lead Phase 1 chip (see fig. 2). Because of the efficiency of the superchips' interconnection, the Phase 2 package will probably not have to use its full input-output capability, which is well above 320 leads.

TRW has produced a proof-of-concept 1-μm superchip, a 700-Kbit dynamic random-access memory with 9.8 million devices. This unit demonstrated redundancy and built-in test features. Prototype superchips are expected in late 1988, a brassboard in 1989, and sample availability for other contractors in 1989.

HONEYWELL'S EFFORT

Honeywell, unlike TRW and IBM, is taking a bipolar approach with its Phase 2 devices. Honeywell's current-mode logic is a 0.5-μm process with four-layer planar metal and grooved isolation. However, Honeywell is working, on its own, on a 0.5-μm CMOS VHSIC-like technology.

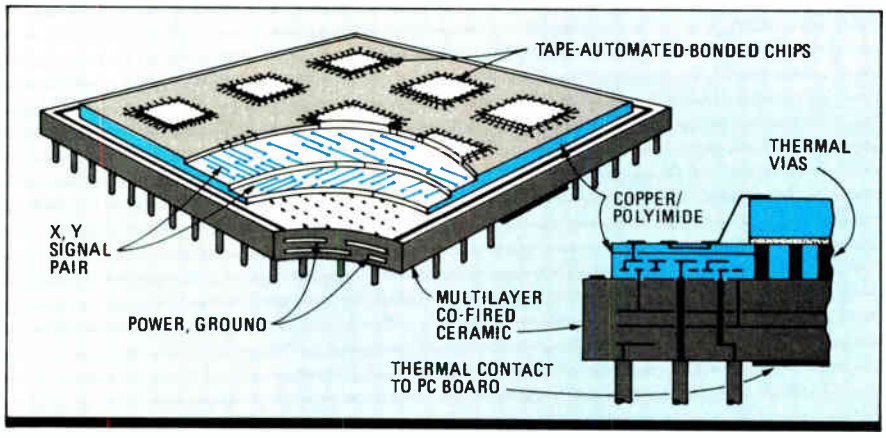
The company is fabricating three basic chip types that will be used to make a Phase 2 electro-optical signal-processor brassboard: a bus-interface unit of about 45,000-gate complexity that is a custom design, a 50,000-gate configurable array, and a 70,000-gate configurable array. The two large configurable gate arrays will be used to make four circuit designs for the brassboard.

Packaging is "a very important part of the program in terms of achieving the high speeds needed," says George Anderson, VHSIC submicron program manager at Honeywell's Solid State Electronics Division in Plymouth, Minn. "As we get to faster circuits, the interconnect becomes more and more of a factor."

This is why Honeywell has developed for its Phase 2 effort a multichip package (see fig. 3) based on an alumina substrate with alternating layers of copper conductors and polyimide dielectric. These layers are used to fabricate a multilayer structure with signal interconnections and power and ground planes.

This package delivers better electrical charac-

teristics than the conventional co-fired multilayer ceramic types that IBM uses. For example, by using polyimide rather than alumina as the insulator, signal propagation in the Honeywell package is about 60 ps/cm, compared with about 100 ps/cm in a conventional co-fired ceramic package. In addition, since the Honeywell copper/polyimide substrate uses IC-type processing, it is relatively easy to put down 1-mil-wide copper conductors, as compared with 5 mils or wider with co-fired ceramic. For its brassboard demonstration in October 1988, Honeywell plans to use a 3.25-by-3.25-in. package carrying seven tape-bonded Phase 2 chips.



3. COPPER POLYIMIDE. To overcome the speed limitations of an all-ceramic package, Honeywell developed a multilayer copper on polyimide structure.

Honeywell has set up a pilot production line in Plymouth with three JEOL Ltd. e-beam systems. The plan is to start with e-beam direct write for all layers and then mix optical lithography steps on the less critically aligned portions of the large configurable arrays.

The company is working on the bus-interface unit, the first deliverable chip in the submicron program. "We will be delivering that chip to the government during the third quarter," Anderson notes, adding that the Plymouth pilot line is running at full speed. He plans to transfer this technology to Honeywell's 6-in.-wafer facility in Colorado Springs perhaps next year.

THE IBM TWO-STEP

IBM, which does all its VHSIC work at its facility in Manassas, Va., is first developing a 1-μm version of its 0.5-μm CMOS chip set. These interim chips will be available as samples from a pilot line in May and June. After IBM completes this interim phase, a design effort to shrink the 1-μm chips to their final submicron dimensions will begin. Pilot-line samples of the final chips are scheduled for mid-1988.

IBM has already fabricated four Phase 2 chip types in the intermediate 1-μm stage: a systolic processor, an address generator, a static 18-Kbit configurable RAM, and a bus-interface unit. These chips, all 5.5 mm², can have up to 220 I/Os. The lithography for these chips was done on IBM's internally developed EL-3 e-beam direct-write systems.

Like Honeywell, IBM's multichip package will accommodate up to 16 chips on a multilayer ceramic substrate in a pin-grid array. However, the IBM chips use the company's C-4 flip-chip process for face-up reflow attachment to the multichip substrate rather than Honeywell's TAB-type attachment. The multilayer ceramic substrate is based on proven IBM technology.

The work of all three contractors will benefit from extensive preparation and support by the Defense Department. Pentagon planners of VHSIC Phase 2 realized that high-speed, high-resolution lithography systems would have to be available for pilot-line production of the Phase 2 devices. To provide them, the DOD awarded contracts to Perkin-Elmer for the Aeble 150 and an X-ray stepper and to GCA Corp. of Andover, Mass., for an advanced optical stepper.

Perkin-Elmer's Aeble 150 has design goals of 0.5-μm resolution, 0.15-μm alignment accuracy, and a throughput as high as 20 wafer exposures per hour (VHSIC's original goal was four wafers per hour). It is now being qualified for two VHSIC participants, TRW and Motorola.

Perkin-Elmer's X-ray stepper is now about to go into acceptance testing. This unit, with 0.5-μm resolution, will have a throughput of about 20 wafer exposures per hour and an alignment accuracy of 0.15 μm.

The most intriguing new lithography tool is GCA's Advanced Wafer Imaging System, or AWIS, a 10 : 1 optical stepper capable of 0.5-μm resolution, a throughput of twenty-five 4-in. wafers per hour, and an alignment accuracy of 0.25 μm with a global-type alignment. With a 0.1-μm die-by-die alignment accuracy, this system could be the submicron aligner everyone's looking for. It also could cost substantially less than its competitors' machines.

To meet tight price and delivery specs, GCA replaced the light source of one of its DSW 8000 aligners with an excimer laser and the optics with newly designed Tropel lenses. These two features have pushed the optical aligner into the submicron region. The AWIS is being assembled and tested at GCA's Fairport, N. Y., facility for shipment to IBM in May.

In an AWIS-related development, the Army's Harry Diamond Laboratories in Adelphi, Md., recently purchased a KLA/Micrion 808 focused ion-beam mask-repair system for repairing defects on reticles for the VHSIC program, such as those the AWIS stepper uses. This Army facility will support any VHSIC Phase 2 reticle activity. □

Additional reporting by Wesley R. Iversen and J. Robert Lineback

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MILITARY/AEROSPACE NEWSLETTER

SEMATECH PLANNING IS RUNNING AHEAD OF SCHEDULE AT SIA

The Semiconductor Industry Association's Sematech task force will beat its own June 1 deadline to produce a formal operating and funding plan for the proposed semiconductor manufacturing technology consortium. In fact, the SIA expects to hold a special board of directors meeting no later than mid-May to act on the task force's plans. Funding, establishing operational priorities, government oversight, and creating a tax-exempt status for Sematech have taken up most of the SIA task force's time. One of the group's major concerns when it met in early March to formulate plans for Sematech—how to persuade Congress to grant Sematech an antitrust waiver—apparently is no longer considered a problem. "If Congress decides that it [Sematech] is in the national interest, they'll make it happen," says an industry source close to the task force. Congressional action will have to be taken by July 4 for the consortium to get started this year. □

DOD PICKS CANDIDATE PROJECTS FOR CONVENTIONAL DEFENSE INITIATIVE

The Department of Defense has singled out five major categories of projects it wants to work on for its Conventional Defense Initiative: smart weapons, battle management, high-power microwaves, armor and anti-armor technology, and special technology opportunities—among them "high-temperature" superconductivity. Some 250 candidate projects have been identified among the major categories, say Pentagon officials, who add that a significant portion of CDI's proposed $5.4 billion 1988 budget will go for target recognition and surveillance, information management, and optical signal processing. CDI program managers will shortly announce an "informational" meeting to discuss the program in detail with potential contractors. □

NAVY SETS ITS PRIORITIES FOR NEAR-TERM R&D

Low-frequency radar and fiber optics, along with antisubmarine warfare, have been given top priority among the Navy's near-term research programs. Richard Rumpf, principal deputy assistant secretary of the Navy for research, engineering, and systems, says the Navy considers the radar work as crucial to an arsenal of techniques it must develop to counter the threat of stealth aircraft and missiles. As for fiber optics, the key concentration will be in missile guidance systems. Rumpf revealed the Navy's R&D thrust at an early-April meeting in Alexandria, Va., cosponsored by the Defense Advanced Research Projects Agency and the Electronic Industries Association. □

SIA NOW ACKNOWLEDGES MIL-SPEC CHIP STANDARDS NEED REVISING

The Semiconductor Industry Association has revised its position on a proposal by a Defense Science Board study group to eliminate most mil-spec components. The SIA last September opposed the recommendation of the DSB, which claimed that state-of-the-art commercial devices have outpaced military-qualified production lines. At the time, the SIA warned that commercial devices wouldn't offer the same reliability as mil-spec semiconductors. However, in a letter mailed in early April to Assistant Secretary of Defense for Acquisition and Logistics Robert Costello, SIA president Andrew A. Procassini called for the modernization of the Pentagon's semiconductor procurement regulations. Among the suggestions from the SIA's Government Procurement Committee: the Pentagon should adopt commercial process-control-qualification techniques and reduce the number of test steps currently used on mil-spec devices. "The mil-spec system is 25 years old and needs to be revamped," says Jon E. Cornell, senior vice president of Harris Corp.'s Semiconductor Sector and chairman of the committee. □

MILITARY/AEROSPACE NEWSLETTER

INTEL, ARTHUR ANDERSEN, AND WIZDOM JOIN TO IMPLEMENT ICAM

Intel Corp., Arthur Andersen & Co., and Wizdom Systems Corp. have joined forces to develop for builders of advanced tactical weapons systems a version of the Air Force's Integrated Computer Aided Manufacturing model. For this first implementation of ICAM, Arthur Andersen's Defense Computer Integrated Manufacturing Group in Dallas will serve as project manager; in that capacity, it will provide planning assistance, software development, and productivity tools. Wizdom Systems, Chicago, the principal architect of ICAM, will provide technical assistance in the design of subsystems and integration. The system will be based on Intel's Series 300 Microcomputer, with real-time control and monitoring for assembly and manufacturing operations. Intel also is providing Ethernet-based network services. □

CONCURRENT'S ADA LETS USERS WORK WITH FORTRAN SUBROUTINES

System developers can use their Fortran programs and subroutines and still meet the Defense Department's requirement that they use Ada, the DOD's programming language. Concurrent Computer Corp.'s version of Ada, C³Ada, features an interface that lets users work with the company's Fortran VII Run Time Library and their own Fortran VII subroutines as if they had been written in Ada, says the Tinton Falls, N. J., company. C³Ada's interface also contributes to impressive processing speeds. Running on the company's 3280MPS computer, C³Ada executes 5,000 Dhrystone instructions/s—at the top of the mips range for comparable systems—using a single processor. As many as six processors can run simultaneously in large systems, boosting the performance to more than 25,000 Dhrystones. □

DARPA EYES A BROADER ROLE IN SEMICONDUCTOR R&D

Watch for the Defense Advanced Research Projects Agency to expand its efforts in semiconductor research and development. Darpa already has a $19.8 million gallium arsenide pilot line under way (see "Bell Labs Setting Up GaAs MOD FET Pilot Line," p. 36), and the director of the agency, Robert C. Duncan, told a Darpa-Electronic Industries Association meeting held in early April in Alexandria, Va., that Darpa had started investigating several potential new semiconductor R&D programs. The agency's emphasis in semiconductors, he explained, is shifting from basic research to prototype programs. One obvious indication of the shift: Darpa has decided to open its own contracting office and has started looking for someone to head it, Duncan says. He expects the agency will eventually manage up to one third of the R&D contracts that are now being handled for it by the U. S. Army, Navy, and Air Force. □

HARRIS AND SILICON COMPILER ADAPTING GENESIL TO RAD-HARD CMOS

Aiming at what it sees as a growing market for customer-designed integrated circuits for the military, Harris Semiconductor's Custom Integrated Circuits Division, Melbourne, Fla., has agreed to help Silicon Compiler Systems Corp., San Jose, Calif., adapt its Genesil design system for Harris' radiation-hardened CMOS design techniques. Harris will fabricate rad-hard chips designed using the new system in a 2-μm double-level-metal process. Meanwhile, an agreement between the companies will allow designs completed on the existing Genesil systems to conform to Harris process-design rules. IC designers will use the Genesil system to define circuit functions and translate these definitions into a custom silicon layout. The finished layout will then be transferred to Harris, along with a formatted test program, for fabrication. □

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NEW PRODUCTS

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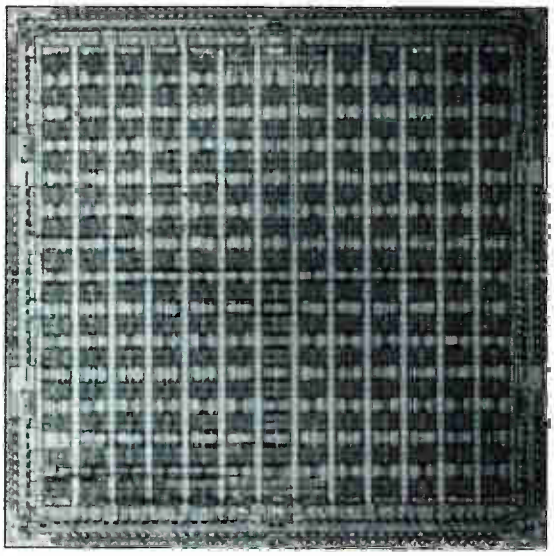
APPLIED MICRO CIRCUITS DOES IT BY SCALING DOWN BIPOLAR PROCESS

By scaling down its 3-μm oxide-isolated bipolar process to 2 μm, Applied Micro Circuits Corp. has boosted the performance of the new Q5000T logic-array series by as much as 25% over its predecessor, the Q3500 series.

Reduced feature sizes in the internal core of the 2-μm arrays yield die sizes that are 30% smaller than the Q3500 family of arrays, says Bernie Rosenthal, product marketing manager.

DENSE. "This allows the Q5000 arrays to have higher densities and speed/power savings over anything Applied Micro Circuits offered previously," says Rosenthal. Internal equivalent gate delays of 210 to 545 ps are 10% to 25% faster than the company's comparable earlier macros, for example, and overall power savings of about 10% can be expected. "The reduced power also helps achieve the better reliability of the new family," he adds. Average utilization of total cell count is 95%. Input/output cells on the arrays provide both emitter-coupled logic and TTL compatibility.



EASY I/O. Input/output cells on the arrays provide compatibility for both ECL and TTL external circuitry.

The arrays have been designed to permit direct access to core logic. In the ECL mode, signals can bypass the input buffers and interface directly to the high-speed clock inputs of selected macros. With this technique, differential ECL input and output frequencies of up to 600 MHz can be attained. In TTL circuits, maximum input and output frequencies of 160 MHz and 90 MHz, respectively, can be supported.

In the logic core of the new family, as with the existing product series, densities are achieved with triple-level series-gated structures, Rosenthal notes. In his opinion, these triple-level structures have the advantage of providing higher functional density than cascaded, two-level structures used for equivalent gate densities by competing array manufacturers.

To provide compatibility for the off-chip drive features, the I/O cells have characteristics and feature sizes that closely resemble those of the current Q3500 series. All I/O cells are universal—capable of input, output, or bidirectional operation.

TWO LAYERS. The new array family uses the two-layer-metal interconnect scheme employed by the Q3500 series, except for the top-of-the-line Q5000T (AMCC uses a T to differentiate the new series), which has three-layer metal throughout.

The first array, the Q3500T, is now available, and four other devices are slated to debut through the third quarter of this year. The Q3500T has 3,500 equivalent gates, 120 usable I/O channels, and typical power dissipation of 2.5 to 6.0 W. The dissipation specification is at 95% utilization and is based on complex macros and the availability of speed/power options, the company notes. Prices are identical to the Q3500's 3c to 4c per gate for an order of 10,000 units.

–Larry Waller

Applied Micro Circuits Corp., 5502 Oberlin Dr., San Diego, Calif. 92121.
Phone (619) 450-9333 [Circle 360]

DIODE STACKS HANDLE HIGH VOLTAGES

A new range of extra-high-voltage diode stacks from Philips can be customized for current ratings from 0.1 A to 1.5 A and voltage ratings from 2 kV to 20 kV. According to the Dutch company, they offer better reliability and performance than competitive products provide.

The devices, which amount to as many as 30 diode crystals stacked on top of each other to provide the specified voltage rating, boast reverse-recovery times as fast as 30 ns, says Graham Hine, international marketing manager for diodes at Philips's Electronic Components and Materials (Elcoma) Division in Eindhoven, the Netherlands.

Philips's glass-bead encapsulation technology accounts for performance improvements over conventional plastic-bodied diode stacks. The moisture-tight hermetic glass seal ensures high reliability and also provides better junction passivation, which leads to better stability. These features are combined in devices that Hine says are the only medium-power ultrafast diode stacks available in glass encapsulation.

Tests with the new stacks have shown the failure rate to be just 1 per 1 billion device hours at maximum ratings. This failure rate is one to three orders of magnitude lower than that achieved with ordinary plastic-encapsulated stacks, says Hine.

Reverse-recovery times of as fast as 30 ns are achieved by diffusing platinum into the silicon at high temperature. By shortening charge-carrier lifetime, this platinum-killing process improves switching speed.

The fast switching speed is well suited to the latest generation of 128-kHz switched-mode and series-resonant power supplies. Control of the platinum-kill-

ing process enables Philips Elcoma to offer a choice of speeds other than 30 ns. Customers can specify 75-, 150-, 350-, and 5,000-ns devices—a wider choice than that offered by plastic-bodied diode stacks.

Typical applications for the diode stacks are microwave ovens, X-ray equipment, and automobile ignition and distributor circuits. Their hermetic glass seal makes the stacks suitable for high-reliability medical, industrial, military, and aerospace applications. Because of its high current ratings, a single stack can replace two or more paralleled low-current devices, saving in cost and in space.

Depending on the current rating, the devices come in SOD-61, SOD-88, or SOD-89 packages. The length of the glass body depends on the number of crystals in it.

The devices are designed for each user's applications, so prices depend on customer specifications of current, voltage, and reverse-recovery time. Minimum order, including engineering and fabrication, is about $20,000.

Samples of custom diode stacks are available three months from receipt of customer specifications, Hine says. Production can start two to three months after a customer accepts the samples.

–John Gosch

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Philips, Elcoma Division, 5600 MD Eindhoven, the Netherlands.
Phone 31-40-723623 [Circle 362]

WAFERSCALE MULTIPLIERS BOAST 30-ns CYCLE TIME

Looking to jump out in front of the competition in the market for the multiplier-accumulators widely used in digital-signal-processing applications, Waferscale Integration Inc. has introduced a parallel 16-by-16-bit device that it claims is 25% faster than competitive designs.

The 1.2-μm CMOS WS59510-30J boasts a total throughput clock cycle of only 30 ns—10 ns faster than its nearest competitor, says Dale Prull, director of marketing.

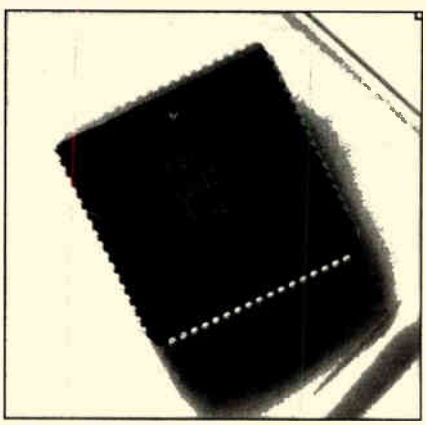
NOT PIPELINED. The WS59510 has a 16-bit-by-16-bit parallel multiplier and a 35-bit accumulator. It owes its speed to its nonpipelined architecture. Whereas pipelined approaches require two clock cycles to process new data, the WS59510 requires just one. The architecture provides for two's-complement or unsigned-magnitude 16-bit operations. Multiplications are based on a modified Booth's multiplication algorithm.

Also contributing to performance are a parallel addition array in the multiplier—structured as a Wallace tree—and the use of carry-select logic in the final-add stage.

The major advantage of the WS59510 over competitive devices is that it requires the least delay to calculate *X*, *Y*, and *P* parameters, says development engineer Yoram Ceder.

"The device enables data to be evaluated one step closer to real time, which is essential in such high-performance applications as 3-d color graphics, military real-time control and guidance systems, array processing, telecommunications, and other DSP applications," Ceder says.

All inputs—both data and instruction—and all the bidirectional outputs are registered. Independently clocked, these registers are positive edge-triggered D-type flip-flops. Designed to be preloaded through the bidirectional output ports, the 35-bit accumulator/output register is divided into a 3-bit extended product (XTP), a 16-bit most-significant product (MSP), and a 16-bit least-significant product (LSP). The XTP and MSP have dedicated ports for three-state output, and the LSP is multiplexed through the *Y* input.



The WS59510-30J is pin-compatible with such devices as Advanced Micro Devices Inc.'s AM29510 and Texas Instruments Inc.'s TDC1010. It is now available in 68-pin plastic leaded-chip-carrier packages, starting at $34 each in quantities of 1,000 or more. The circuit is also available in ceramic dual in-line packages and ceramic leadless-chip-carrier packages, as well as in macro cell form as part of the company's semicustom cell library. *–Bernard C. Cole*

Waferscale Integration Inc., 47280 Kato Rd., Fremont, Calif. 94528.
Phone (415) 656-5400 [Circle 363]

EDGE'S DUAL-PROCESSOR 1200 RUNS AT 11 MIPS

32-KBYTE INSTRUCTION CACHE, EQUAL BUS LOADING DELIVER SUPERMINI PERFORMANCE FOR $128,000

Edge Computer Corp.'s newest superminicomputer achieves a sustained performance of 11 million instructions/s—and a 16-mips peak—by harnessing a pair of proprietary 10-chip, 2-μm CMOS processors to a pipelined, dual-bus architecture and then maximizing bus utilization with a two-pronged design strategy: equalizing bus loading and using a 32-Kbyte instruction cache.

Although the Edge 1200's blazing speed matches high-end superminicomputer performance, its $128,000 price tag is about one-sixth that of a high-end supermini, says a spokesman for the Scottsdale, Ariz., company. The 1200 offers original-equipment manufacturers the opportunity to configure a system compatible with Motorola Corp.'s 680X0 instruction set but with performance that is superior to the 5-mips 68020 microprocessor.

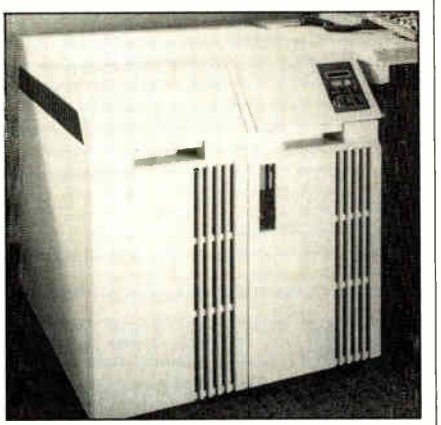
BUS LOADING. Maximizing throughput on the two 30-Mbyte/s buses became a key element in the design strategy, because simply adding another processor to the company's existing 32-bit, 6-mips Edge 1 would have resulted in bottlenecks, says Robert W. Crawford, vice president of development.

Edge designers began by equalizing bus loading. In the company's dual-bus, single-processor Edge 1, the A bus handles instruction/fetch functions and the B bus does operand/execute functions. This architecture allows both an instruction and data to be accessed in a single clock cycle, says Crawford, but it also loads the buses unequally.

Typically, the instruction bus runs at 45% capacity and the operand bus at 60%. But by reversing bus assignments for the second processor—the A bus for operands and the B bus for instructions—designers reduced the likelihood of bottlenecks. Edge further unburdened the buses by implementing a two-way set, 32-Kbyte instruction cache for each processor. By fetching instructions from the cache, the system cuts loading from 45% to 5% of each instruction bus, says Crawford.

I/O CAPABILITY. The two-pronged strategy results in 65% loading on each bus, leaving 35% for the input/ouput operations critical in departmental computing.

For customers who now need single-processor performance but expect their computing needs to grow, Edge offers a new, single-processor Edge 1100 that can be upgraded by adding another processor board.



CUTTING EDGE. The 10-chip central processors are implemented in 2-μm gate arrays.

Edge's dual-processor system retains the same proprietary 10-chip central processor design, 7-chip floating-point coprocessor, and 3-chip memory-management and control units used in the Edge 1. All 20 chips are implemented in a 2-μm CMOS channelless gate array having 8,500 gates.

While almost doubling performance over its previous offering, Edge maintains its commitment to a small, open-architecture 32-bit computer with advanced networking capabilities. Edge's GSX Unix operating system is an enhanced version of AT&T Co.'s Unix System V. The 1200 has eight I/O channels, each with a 6-Mbyte/s transfer rate, and can handle up to 512 terminals. It operates on 110 V and fits in a 17 in.-by-29-in.-by-32-in. cabinet.

Edge sees a growing market in applications such as calculation-intensive scientific computing and departmental networks that are saturating the 68020's performance capabilities. President Alex Cimochowski says that by offering "continuity of compatible computing" for the 680X0 instruction set, Edge provides the same performance-upgrading opportunities now offered only by Digital Equipment Corp. and IBM Corp.

In addition, he says, although reduced-instruction-set computers offer price/performance ratios comparable to Edge's, users of 680X0-based products must change operating systems, compilers, and data formats to switch to RISC systems.

Available in June, a 1200 system with 8 Mbytes of system memory, 337 Mbytes of hard-disk storage, and the GSX Unix operating system will cost $128,000. The single-processor 1100, similarly configured, will cost $104,000.

Edge Computer Corp., 7273 E. Butherus Dr., Scottsdale, Ariz. 85260.
Phone (602) 951-2020 [Circle 340]

NEW SOFTWARE SIMPLIFIES DOCUMENTATION CHANGES

A major enhancement to Context Corp.'s document-management software makes it possible to incorporate alterations and additions into a report, manual, or other engineering document by electronically tagging each amendment and automatically tracing its implications through the entire document.

The new package—called Change Control—becomes part of Context's series of Documentation Workstations, a hierarchical engineering documentation system in which a large document can be broken up into a smaller pieces, or modules, that can be worked on individually. Typically, Context software is used for in-plant publishing of product proposals, engineering specifications, and manuals. Its output is sent to a laser printer.

The Beaverton, Ore., software developer is a spinoff of Mentor Graphics Corp. Like Mentor's computer-aided-design software, Context's documentation software runs on an Apollo Domain work station.

The new Change Control software package eliminates the time-consuming task of searching out and manually changing each reference to a change in design, text, or graphic in the documentation of a new product, making it much simpler to update manuals, reports, or any other printed document derived from the electronic original.

WHODUNIT. Alterations—including overlapping and conflicting changes—are identified according to who made a change, and when and why it was made.

Individuals are tagged according to a specific color or overlay pattern—a process Context refers to informally as a "computer-aided magic marker." System administrators can accept or reject changes, or even tailor the changes to particular versions of a document. Some manuals, for instance, need different versions for the different countries in

which a product is sold. With the Change Control software, all versions can be maintained as a single electronic document that is automatically and selectively edited when the time comes to produce a manual, report, or other end product.

Pictures, tables, and other documents are included by reference, so that changes made to any given module will be reflected in all documents containing that module.

Control software can be added to Context's documentation packages at no cost. Prices for the basic software range from $4,900 for a text editor to more than $30,000 for a full package.

The Change Control packages will be available on a limited basis in the second quarter of this year, with regular shipments due to commence in the third quarter.

Context Corp., 8285 S. W. Nimbus Ave., Beaverton, Ore. 97005.
Phone (503) 646-2600 [Circle 341]

CONTROLLER CUTS I/O INTERRUPTIONS

A multiport VMEbus peripheral controller card from Interphase Corp. shares direct-memory-access management duties with the host system's processor to achieve as much as a tenfold reduction in the number of times the host is interrupted while transferring data files to printers, plotters, or small-computer-system interface (SCSI) ports.

Once the host initiates DMA sequences, the V/MIX 3210's state machine finishes the task, issuing a single interrupt when the transfer is complete. The performance advantage is considerable, because plotter data files, for example, can be as large as 100 Kbytes.

The controller has three ports for SCSI interfaces, printers, and plotters. Available now, it costs $995 each in volume purchases.

Interphase Corp., 2925 Merrell Rd., Dallas, Texas 75229.
Phone (214) 350-9000 [Circle 345]

FLEXIBLE NETWORK MIXES COAX AND FIBER OPTICS

SYSTECH NET SUPPORTS A WIDE RANGE OF CONFIGURATIONS: OPTICAL TRANSMISSION CABLES EXTEND IT UP TO 4,000 FT

A distributed communications subsystem from Systech Corp., San Diego, does away with modems, dedicated plug-in connection boards, and signal repeaters in connecting a host computer to as many as 128 terminals.

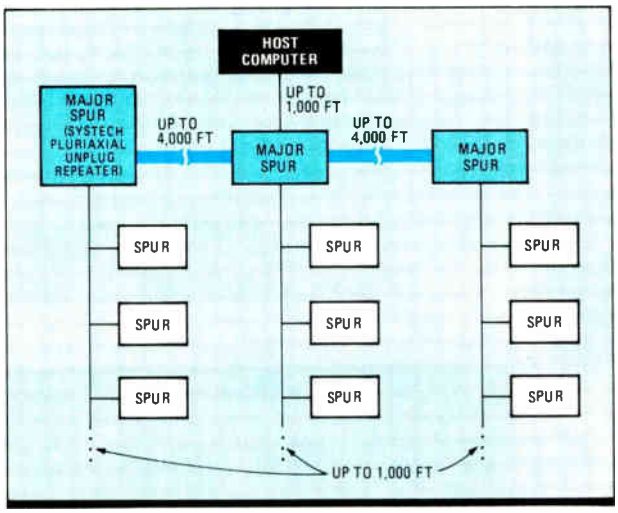
The system offers original equipment manufacturers two advantages: configuration flexibility and fiber-optic transmission compatibility. Using a token-passing bit-serial bus system, it offers 2.5-Mbit/s data transmission rates with either the coaxial or fiber-optic transport interfaces.

Systech Pluriaxial Unplug Repeaters, or SPURs, consist of a line driver and receiver compatible with Systech's existing host adapters and cluster controllers that handle up to 16 terminals each. Every SPUR has six coaxial ports.

Flexibility is the system's main advantage, says Robert A. Hahn, vice president of marketing. A simple serial bus can be modified to a star topology, for example. "Permutations and combinations of configurations using SPURs are almost limitless," he says.

With SPURs and coaxial cabling, a fan-out of up to five separate segments of 1,000 feet each can be installed. Converting from coaxial to fiber-optic cables means each segment can extend up to 4,000 ft.

With fiber-optic cabling, a chained series of SPURs can stretch as far as three miles from the host computer to the most distant cluster controller, says Hahn. Fiber-optic cable can also be used in segments where electrical isolation is important.



EXTENDED. Fiber-optic cables (in color) can be combined with coaxial links to form extended networks.

Both types of transmission media can be mixed in the same installation, and maximum distances are achieved by chaining together a number of SPURs. "Without SPUR, distances of this magnitude [up to three miles] would require a much more costly approach, using modems and telephone lines or similar approaches," Hahn says.

For a 16-terminal configuration of 1,000-ft. lines, the modem/phone line approach would cost about $20,000, compared with about $6,500 using SPURs, and that includes about $5,000 for cable, says Hahn.

Each SPUR measures 2⅞ in. in height, 10⅛ in. in width, and 10 in. in depth. It weighs 3.9 lb and operates from 115- or 220-V sources. Indicators are tricolor light-emitting diodes.

The company says that the subsystem must do more than just pass along a signal, because of the long distances of the data transmission. Built-in circuitry to reduce any inherent data-transmission "jitter" continually cleans and regenerates the signal.

Founded in 1981, Systech specializes in communications subsystems that increase performance of large computer systems by offloading communications functions. SPURs are available in three formats: HPS-5580, with six coaxial ports, at $610; HPS-5581, with an added fiber-optic port, $1,505; and HPS-5582, with two fiber-optic ports, $2,205. *–Larry Waller*

Systech Corp., 6465 Nancy Ridge Dr., San Diego, Calif. 92121.
Phone (619) 453-8970 [Circle 440]

UNIT GIVES PCs FAX CAPABILITY

Brooktrout Technology's Fax-Mail products eliminate the personnel costs associated with facsimile-machine transmissions of data and graphics by providing hardware and software that let IBM Corp. Personal Computers or compatibles double as facsimile machines.

Using board-level digital-signal-processing technology, bit-mapped pages of text and high-resolution graphics can be transmitted between fax machines and PCs at up to 9,600 baud without the blurring caused by light-scanning techniques. As many as 10 letter-size pages can be stored on a single floppy disk. Fax-Mail is CCITT Group II and III compatible.

The great bulk of business information exists on paper, says the company, and Fax-Mail provides a low-cost means of transmitting it throughout an installed base of millions of personal computers.

Available now, the 9,600-baud Fax-Mail 96 costs $995; the 4,800-baud Fax-Mail 48 is $795; and the Fax-Mail 24 is $595. Prices include software. By contrast, facsimile machines cost around $3,000.

Brooktrout Technology Inc., 110 Cedar St., Wellesley Hills, Mass. 02181.
Phone (617) 235-3026 [Circle 445]

FASTNET CONNECTS MACINTOSH TO LANs

Dove Computer Corp.'s FastNet system provides Apple Computer Corp.'s Macintosh family access to mainframe computers over Ethernet local-area networks.

FastNet's Communication Control Unit is built around a Motorola Corp. 68000 microprocessor and comes equipped with 512 Kbytes of random-access memory. It is available for small computer-system interface connections with the Macintosh 512E, Macintosh Plus, Macintosh SE, and Macintosh II.

Network file transfers, file access, and mail transactions are controlled using familiar Macintosh icons. Transmission rates up to 19.2 Kbaud are supported. Available now, the control unit costs $1,099. Modules for connecting it to Ethernet LANs cost $399 each.

Dove Computer Corp., 1200 N. 23rd St., Wilmington, N.C. 28405.
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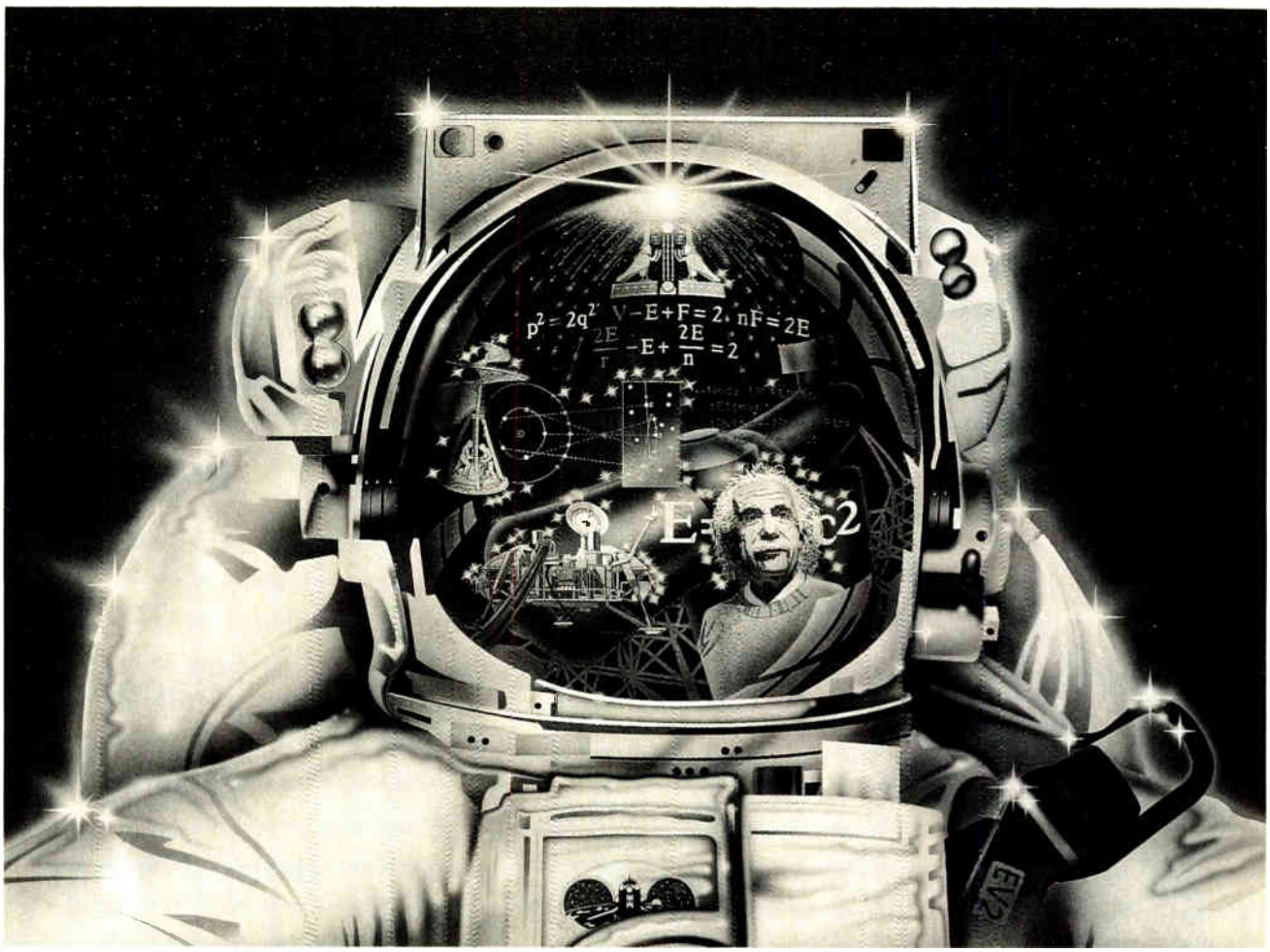

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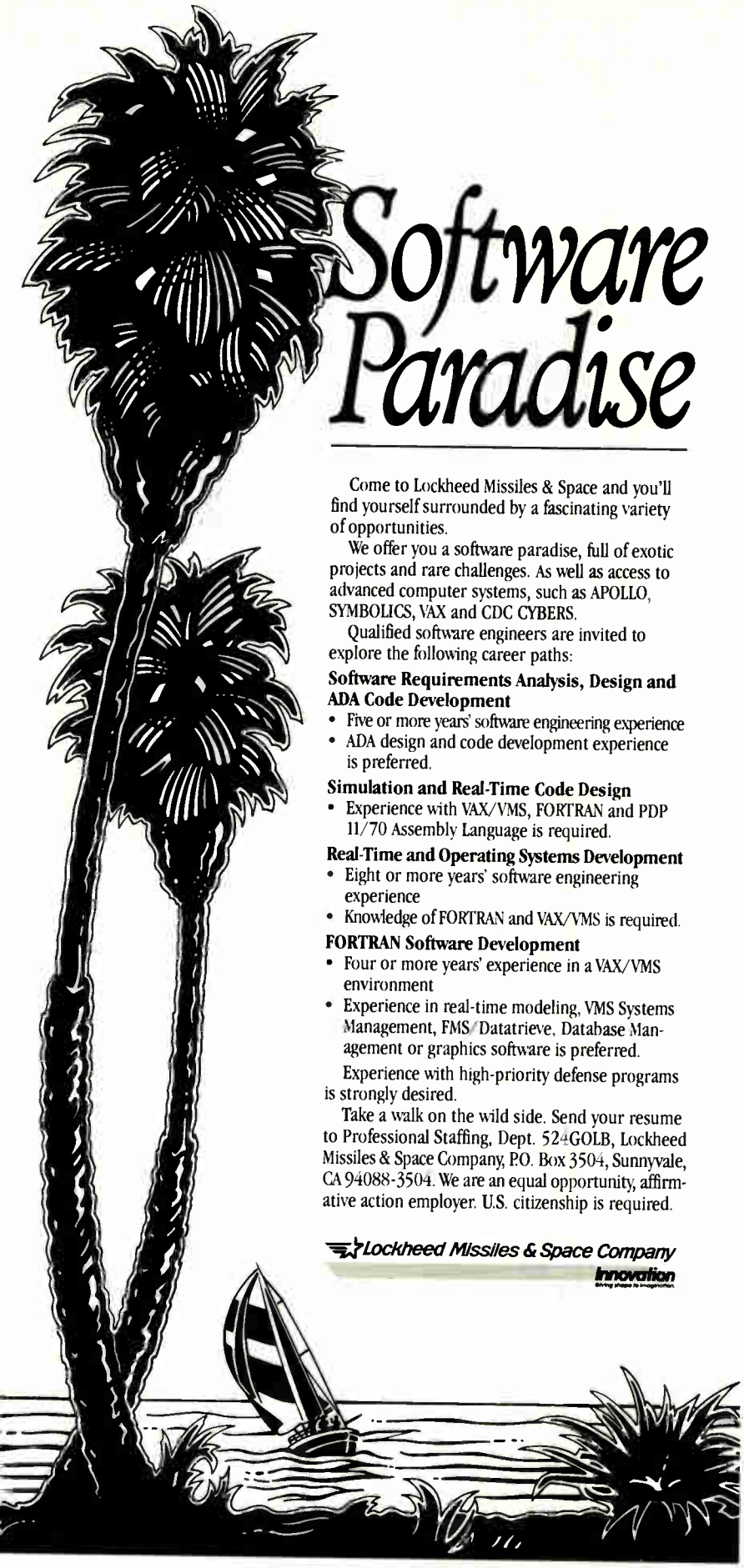

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ELECTRONICS WEEK

CHINA MARKET GETS GOOD REVIEWS

It appears the time is ripe for foreign companies to make strategic commitments in China. In a recent study, half of the foreign investors responding said their joint ventures there had exceeded performance targets; 28% reported that they had greatly exceeded their goals; 44% said they had met targets; and only 6% said they fell below targets. In 1985, U.S.-based investors contributed $357 million—more than 37% of all foreign investment in China. The study was conducted by A. T. Kearney Inc., New York, and the International Trade Research Institute of Beijing, China.

GE EXPECTS VHSIC FAB CERTIFICATION

General Electric Co. is awaiting certification of one of its fabrication lines to make chips for the Pentagon's Very High-Speed Integrated Circuits program (see p. 84). The U.S. Defense Electronics Supply Center has just completed an audit of GE Semiconductor's fabrication line in Research Triangle Park, N.C., for VHSIC-compatible 1.25-μm circuit production. The company is in the process of qualifying a 1.25-μm butterfly chip for radar applications, and it says it will pursue generic qualification of the 1.25-μm line later this year.

MMI, ALTERA SETTLE PATENT SUIT

Monolithic Memories Inc., of Santa Clara, Calif., has reached a settlement of its programmable-logic patent case against Altera Corp., also of Santa Clara. MMI claimed basic rights to programmable array logic in suits against both Altera and Lattice Semiconductor Corp., Beaverton, Ore., last September. This month Altera and MMI settled their dispute and licensed each other's technologies, with Altera agreeing to provide an unspecified financial consideration for the benefit of MMI. No money or royalties were involved. Lattice, which had countersued, says it has been unable to come to terms with MMI.

NOW SHOWING: THE THREE AMIGAS

Moving to broaden the appeal of its Amiga, a home-oriented microcomputer based on the Motorola 68000 microprocessor, Commodore Business Machines Inc., West Chester, Pa., is expanding the line to include low- and high-end versions. Commodore will offer a stripped-down machine for the home, the $649 model 500, and a more powerful machine for business, the $1,500 model 2000. In addition, the Amiga operating system software now resides in read-only memory rather than on floppy disk.

DG OFFERS TO BUY AI FIRM IN CHAPTER 11

Just days after Lisp Machines Inc., a maker of artificial intelligence hardware and software, filed for Chapter 11 protection, Data General Corp. of Westboro, Mass., offered to buy all of its technology and assets and hire its remaining 50 employees. Lisp has appointed as interim president Patrick Kareiva, a merger and acquisitions specialist, to review Data General's offer and solicit other offers. The $10 million Lowell, Mass., company struggled for months to gain market share in such AI areas as factory automation and process control against stiff competition, including Symbolics Inc. and Texas Instruments.

AMPEX IS SOLD TO LANESBOROUGH

Ampex Corp., a pioneer in video recording technology, will retain its present management after being sold by technology conglomerate Allied-Signal Inc. of Morris Township, N. J., to Lanesborough Corp. for $479 million. Rolm Corp. founder M. Kenneth Oshman headed a venture group that tried to buy Ampex, but the group lost out to Lanesborough, a privately held New York chemical firm. Ampex president Charles A. Steinberg says the Redwood City, Calif., company will function as a stand-alone corporation.

HONEYWELL BULL UNVEILS PRODUCTS

A week after Honeywell Inc. sold 57.5% of its computer business, Honeywell Information Systems, to Compagnie des Machines Bull of France and NEC Corp. of Japan, the new company—Honeywell Bull, of Minneapolis—announced its first new products. A new line of high-end mainframes, the DPS 7000 Series, replaces the current DPS7 line. The five new models, designed and built by Bull, use Honeywell 22,000-gate CMOS chips. The sale of Honeywell Information Systems represents what Edson Spencer, Honeywell's chief executive officer, says is his company's "last major step in restructuring." Honeywell, Bull, and NEC jointly manage Honeywell Bull.

ROBOT ASSISTS BRAIN SURGEON

Being demonstrated at this month's Robots 11 show in Chicago is a Westinghouse Unimate Puma 200 robot that assists a neurosurgeon performing simulated brain surgery. In the operation, the robot replaces part of the stereotactic head frame used in conventional neurosurgery to position surgical probes for insertion into the brain. The robot can position a probe to within 0.1 mm accuracy at the desired trajectory to hit an intercranial target, based on computerized tomographic scanning data. The probe is then inserted manually by the surgeon. The technique, developed at Long Beach Memorial Hospital in California, has been used on 24 patients during the past year.

VLSI TECHNOLOGY SIGNS SCHWEBER

VLSI Technology Inc. has signed Schweber Electronics, the third largest U.S. electronics distributor, to handle its memory and ASIC-derived standard products in Minneapolis, Baltimore, and San Jose and Irvine in California. Schweber distributes rival LSI Logic Inc. parts in Boston, New York, and Atlanta. VLSI Technology retains Aero Electronics, the second largest distributor, in San Jose and in Fairfield, N.J.

SEMICONDUCTOR RESEARCH IN SPACE

Rockwell International has signed an agreement to perform experiments with semiconductor materials in space aboard one of the National Aeronautics and Space Administration's space shuttles. The experiments are planned to begin in February 1988. Rockwell researchers will use the floating-zone crystal-growth process on indium and selenium, and NASA scientists will investigate polymer materials. Both experiments aim at developing structural integrities that can't be achieved on earth because of gravity.

GaAs MARKET TO BE $4.4 BILLION IN 1991

The worldwide market for gallium arsenide semiconductors will be $4.4 billion in 1991, says San Jose, Calif., market researcher Dataquest Inc. That's nearly triple the $1.8 billion recorded in 1984. Dataquest pins the growth on the fact that GaAs devices are moving out of the lab and into commercial applications, notably fiber-optic and satellite communications, supercomputing, and electronic test and measurement.

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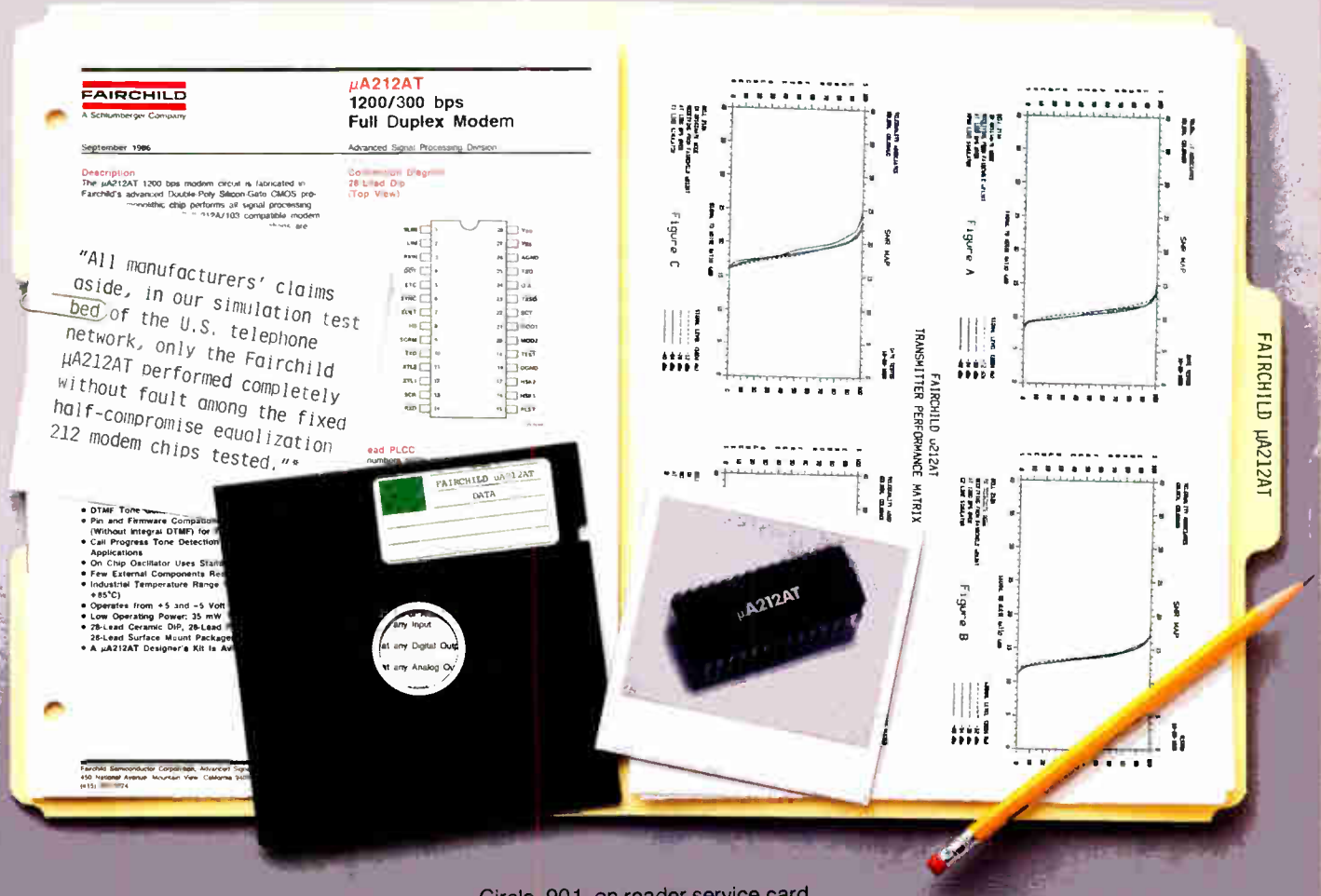

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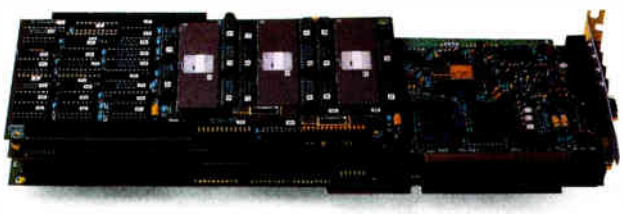

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