ISSCC STARS: 16-MB DRAM, 4-MB EPROM, 32-BIT CPUs/58

VECTOR PROCESSING COMES TO THE DESKTOP/69

A McGRAW-HILL PUBLICATION SIX DOLLARS MARCH 5, 1987

Electronics

DESIGNER'S DREAM MACHINE

PAGE 53

DALLAS SEMICONDUCTOR'S MICROCONTROLLER UPDATES ITSELF ON THE FLY

The Source for High Performance

... in interconnection/packaging products for microcomputer bus systems

An experienced engineer knows that **safe noise margins must be "designed in,"** reliability of operation depends on it.

Inadequate margins are eroded by:

- Production tolerances
- Traffic density
- Coincidence of signal currents
- Optional hardware additions

... which could lead to failure of a normally operating system. Hybricon products are **designed to maintain noise immunity** by taking into account the factors which affect them, such as:

- Backward and forward crosstalk
- Differential ground signals
- Rise time distortion and ringing due to reflected waves
- Signal propagation delay
- DC voltage drops

We're your design-in source and deliver products configured to your exact specifications. Customizing to special needs is an integral part of the Hybricon process, which is:

- Cost effective: Starts from extensive CAD data base
- Interactive: Continuous communication with customer

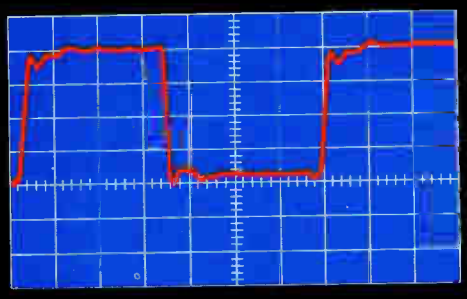
Hybricon manufactures an extensive line of standard and customized products specifically for bus based systems, and they are available world wide. Send for the name and address of your local Hybricon representative or international distributor.

Customer evaluations rate Hybricon's VME Backplanes high in performance.

Hybricon's engineers have optimized:

- Signal transmission integrity
- Propagation time
- Reflections
- Power distribution
- Crosstalk

... to produce a family of standard VME backplanes unsurpassed in their ability to support clean transparent transmission of signals between function boards.



Exceptionally clean signals characterize Hybricon's backplanes. (Illustrated from actual customer photos.)

Excellence of Design

Hybricon Engineers understand your problems; they have direct experience in high speed system design. Hybricon backplanes rate high in performance because they incorporate **basic and solid engineering principles.**

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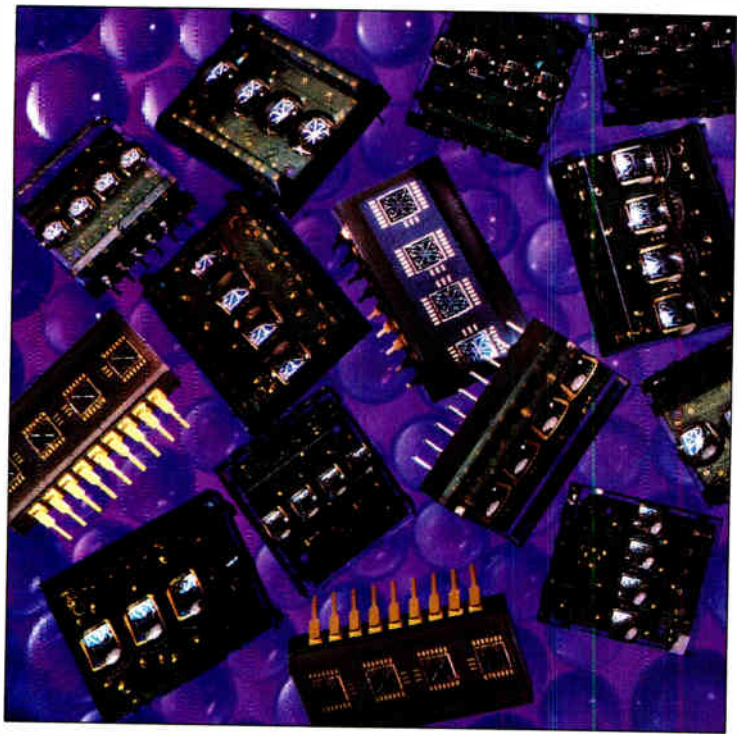
Circle 900 on reader service card

SURPRISE!

You don't have to pay more to get more.

More performance.
Our new smart displays have built-in RAM, ASCII decoder, and LED drive circuitry.

They also feature a super-fast access time of 160 ns, full TTL compatibility, and a wide range of operating temperatures.



More reliability.

Large built-in input protection diodes help eliminate the possibility of electrostatic damage. And a special package design ensures excellent temperature cycling performance.

The HPDL-1414, HPDL-2416, and HMDL-2416 are all wave-solderable.

The HMDL-2416 is especially designed for high-reliability applications and conforms to military specification MIL-D-87157.

More choices.

With the addition of these three new products, Hewlett-Packard now offers you a complete line of alphanumeric displays. All at competitive prices.

Choose one of these new smart displays or one of our other displays. Choose dot matrix or segmented displays. Choose your color. Choose character heights of 0.112 inch to 0.27 inch. Or choose special features such as extended temperature ranges, sunlight viewability, or hermetic sealing.

More for your money.

Prove the value of our new displays for yourself. Return the coupon with your check for $20 and we'll send you the smart display of your choice along with a free demo box.

For more information about our complete line and the name of your authorized distributor, call the Hewlett-Packard sales office listed in your white pages and ask for the Components Department.

I want more. Please send me the display checked below along with my free demo box. I've attached my business card and enclosed my check for $20 made out to Monte Smith, Hewlett-Packard, 370 W. Trimble Road, San Jose, CA 95131.

- ☐ HPDL-1414 (0.112" epoxy sealed)
- ☐ HPDL-2416 (0.16" epoxy sealed)
- ☐ HMDL-2416 (0.16" hermetically sealed

Limit one per customer. Offer good in U.S. only. Expires April 30, 1987.

3/5/87

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CG08509A

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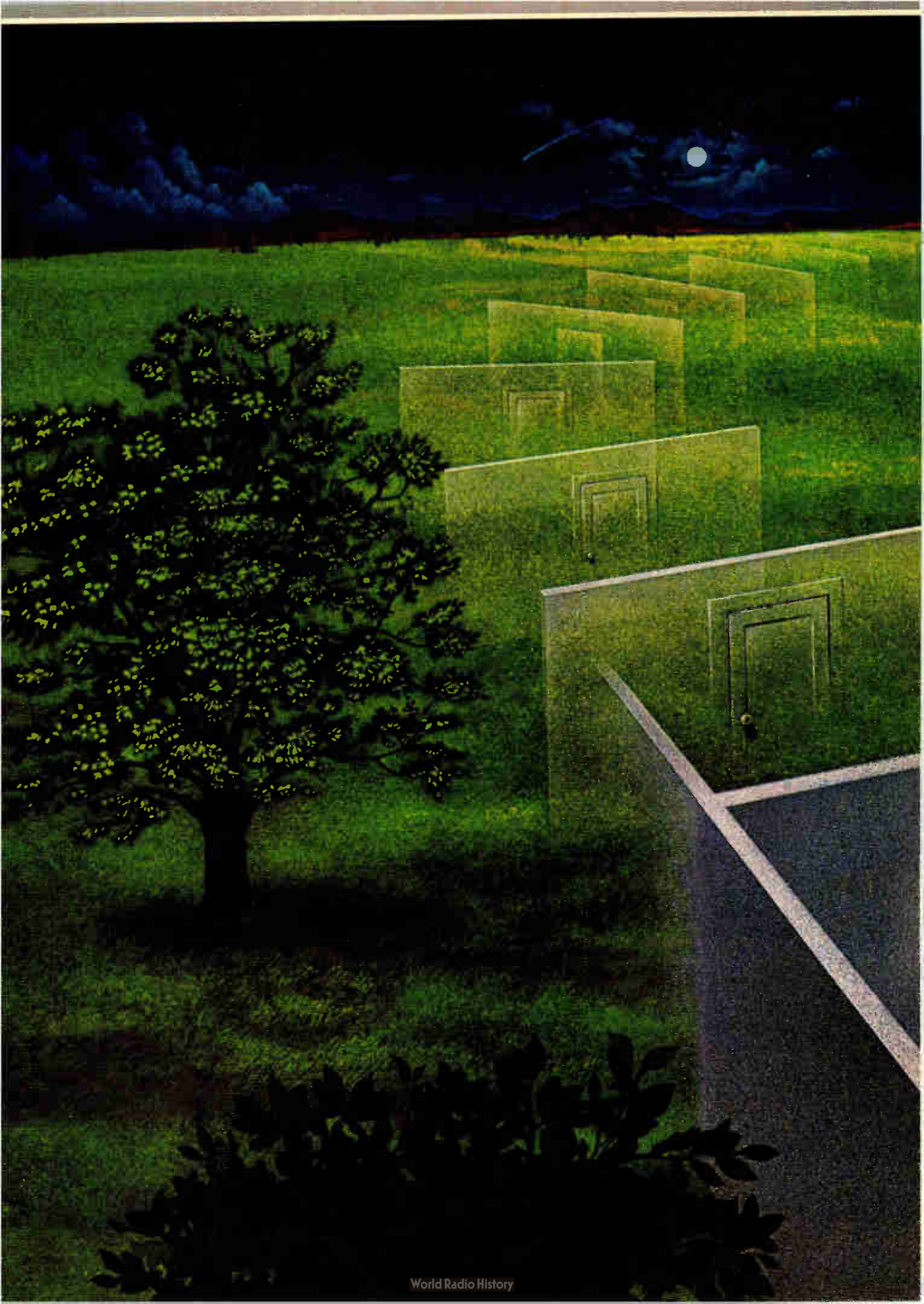
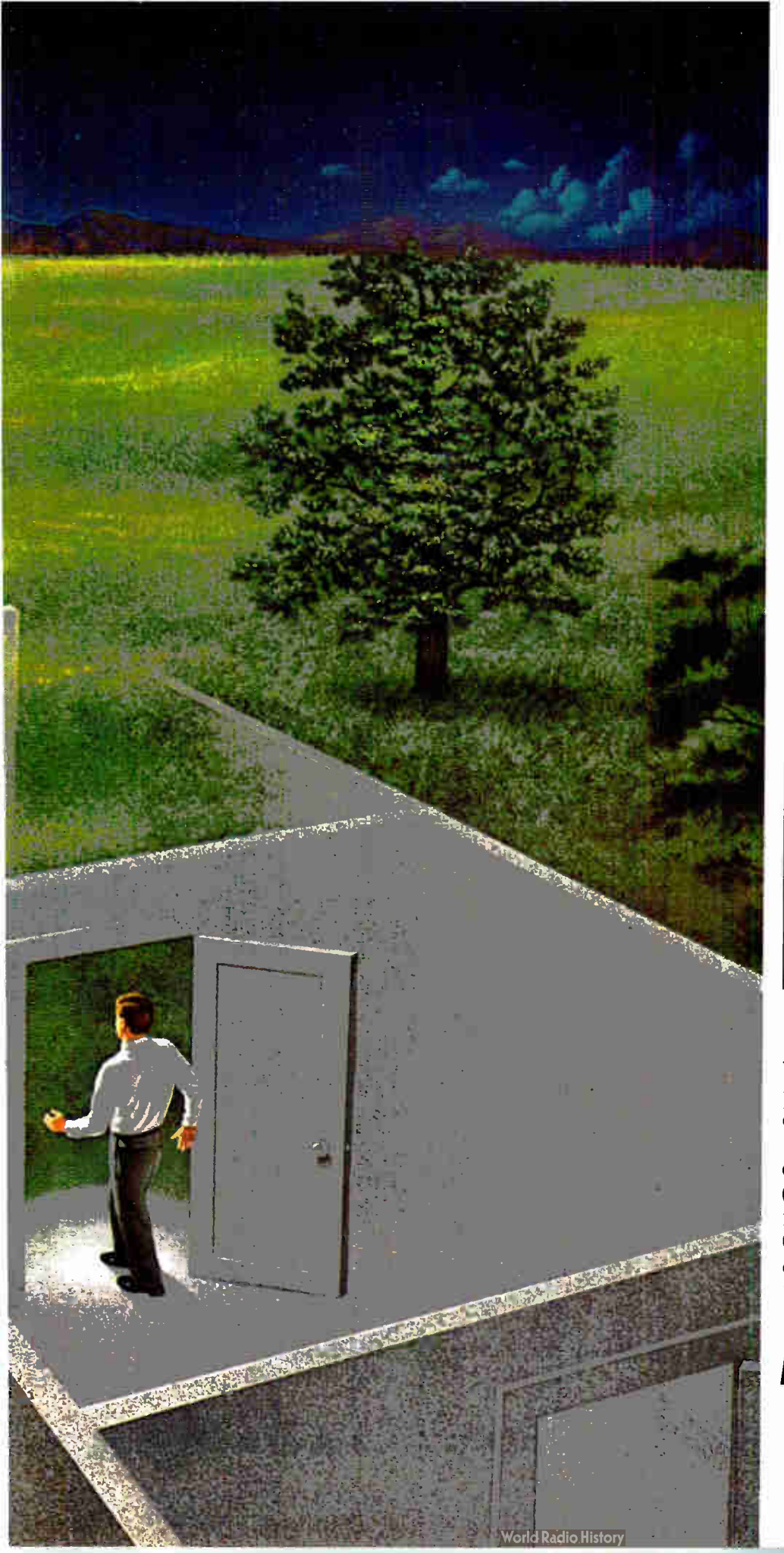




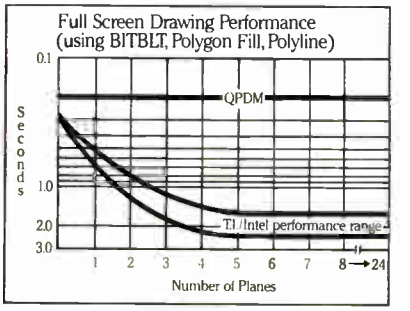
Don't let reality stop you.

Grab a pad and get to work on tomorrow.

That's how we designed the Am95C60 Quad Pixel Dataflow Manager, a CMOS graphics coprocessor that proves "high performance graphics" is no longer a contradiction in terms.

With a polyline draw speed of 110,000 vectors per second, a BITBLT transfer of 55ns per pixel, and a polygon fill of 20ns per pixel, QPDM can change a screen faster than the speed of thought. (It can redraw a 1K X 1K screen in 0.2 seconds.)

Besides being powerful, this animal is highly trained. The instruction set for full graphics and text primitives is already on the chip. There aren't any extra programming hurdles to slow it down.



Each QPDM addresses four planes. It's cascadable, too. With no degradation in performance. And it can deliver all the color you need.

Get ahead of the market by designing it in now. Call us at (800) 255-DRAW to find out more about QPDM and QPDM seminars. Then discover the rush of designing the future.

Advanced Micro Devices

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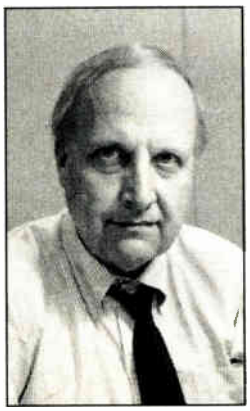
FYI

What really hurts is that industrial automation and productivity still have no real champion—either in government or even in the electronics industry itself



It seems like most everyone these days worries a lot about America's lack of international competitiveness. And well they should. But what really hurts is that industrial automation and productivity still have no real champion—either in the federal government or in the electronics industry itself.

To begin with, Washington could have done a lot to jump-start industrial automation in a big way. But the track record indicates no inclination to do much of anything, according to a study made by *Managing Automation* magazine. And it's no secret that manufacturers in general have slowed their automation equipment buying.

President Reagan had an opportunity in 1984 when Congress passed a bill that would have set up the Manufacturing Sciences and Robotics Research and Development Act. The bipartisan bill would have authorized $250 million over four years, something that would have been a big lift for automation. But the President vetoed the bill, claiming it would lead the federal government into an "unwarranted role."

More, too, could have come from the National Science Foundation by taking its computer-integrated manufacturing grant program off its starvation diet, says the study. The government doesn't seem to be laying any significant foundations for the future in automation and CIM. The $14 million now being spent by the NSF on CIM could easily be doubled.

Congress certainly isn't providing much in the way of either help or leadership. It could have passed a tax bill, for example, that was not so tough on equipment-buying incentives, and a report issued last fall by the Senate Democratic Working Group on Economic Competitiveness amazingly does not even mention automation.

In fact, no one in industry has even been asking the Administration or the Congress for help. Automation industry lobbyists are conspicuous by their absence on Capitol Hill. Digital Equipment Corp., the No. 3 computer maker, has no lobbyist in Washington, according to the magazine study. Industry needs to push Washington to aggressively promote manufacturing technologies with dollars and whatever else it takes. Otherwise, this country's spectacular bid for competitiveness could end up a spectacular bust. While the trade bill is expected to pass this year, it is aimed at hindering foreign competition. That's curing the symptom, not the cause.

ROBERT W. HENKEL

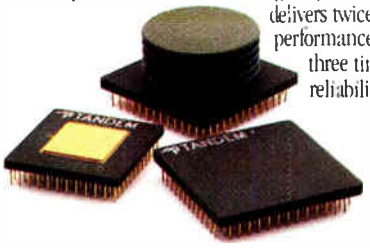
NonStop VLX.™

Tandem technology sets the new standard for large applications in on-line transaction processing.

More transactions per second at a lower cost per transaction than any system in the world.

THE CIRCUITRY'S FAST.

We designed the system in our own laboratory, right down to our own unique VLSI chips. The result is more circuitry in less space. With fewer components than our next largest system, the VLX delivers twice the performance and three times the reliability.



PROCESSORS WITH LARGE APPETITES.

The VLX processors move transactions in 32-bit chunks. They reach into main memory in 64-bit chunks. Because this happens in parallel, more work gets done in less time at a lower cost per transaction.

THE SERVICE IS EASY.

All critical components are field replaceable. When service is required, it's faster. You don't even have to stop an operation to add or replace components.

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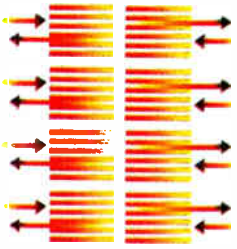
In a conventional database, I/O requests must be handled sequentially. This creates queues that slow response time. In the VLX system, there are multiple paths to multiple disks. Data enters and leaves the database simultaneously. No time is wasted, and all disk space gets used.

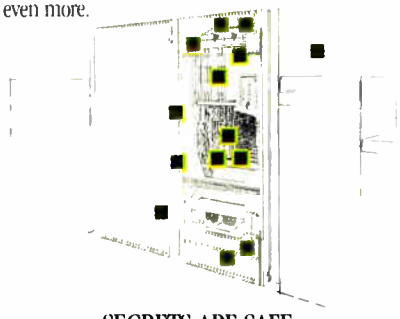


DIAGNOSTICS FROM A DISTANCE.

An integrated microprocessor allows us to monitor the system environment from anywhere in the world. We can even run stress tests remotely. If a failure does occur, the VLX has the capability to automatically dial out to remote centers anywhere in our worldwide network.

THE SYSTEM KNOWS THE SYMPTOMS.

Expert systems software, using fault analysis, directs the problem diagnosis systematically. It also allows us to analyze it and shorten service time even more.

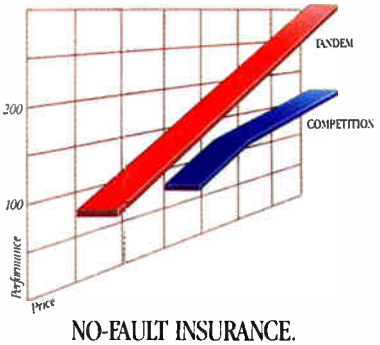


SECRETS ARE SAFE.

We offer software that will protect the security of your data whether it's in the VLX, in another Tandem system or in transmission.

NO GROWING PAINS.

To add power, just add processors. You can grow from a base four-processor system to 16. From there, you can expand in whatever increments you choose, all the way to 255 systems. You never buy more than you need, and you'll never have to rewrite a line of applications code.



NO-FAULT INSURANCE.

Tandem systems achieve fault-tolerance with a unique, parallel processing architecture. There are no idle back-up components. Instead, multiple components share the workload. If one goes down, the others pick up the slack, and application processing is uninterrupted.

HERE TODAY. HERE TOMORROW.

The VLX is compatible with any Tandem system and with all major communications standards—SNA, X.25, MAP and O.S.I. And by acting as a gateway to other vendors' systems, the VLX can link them and enhance their value as well.

WE HAVE EXCELLENT REFERENCES.

Tandem systems are at work for Fortune 500 companies in banking, telecommunications, manufacturing, transportation, retailing and energy, as well as several branches of the U.S. Government.

To find out what we can do for you, call 800-482-6336 or write to us. Corporate Headquarters: Tandem Computers Incorporated, 19191 Vallco Parkway, Dept. 752-M, Cupertino, CA 95014

TANDEMCOMPUTERS

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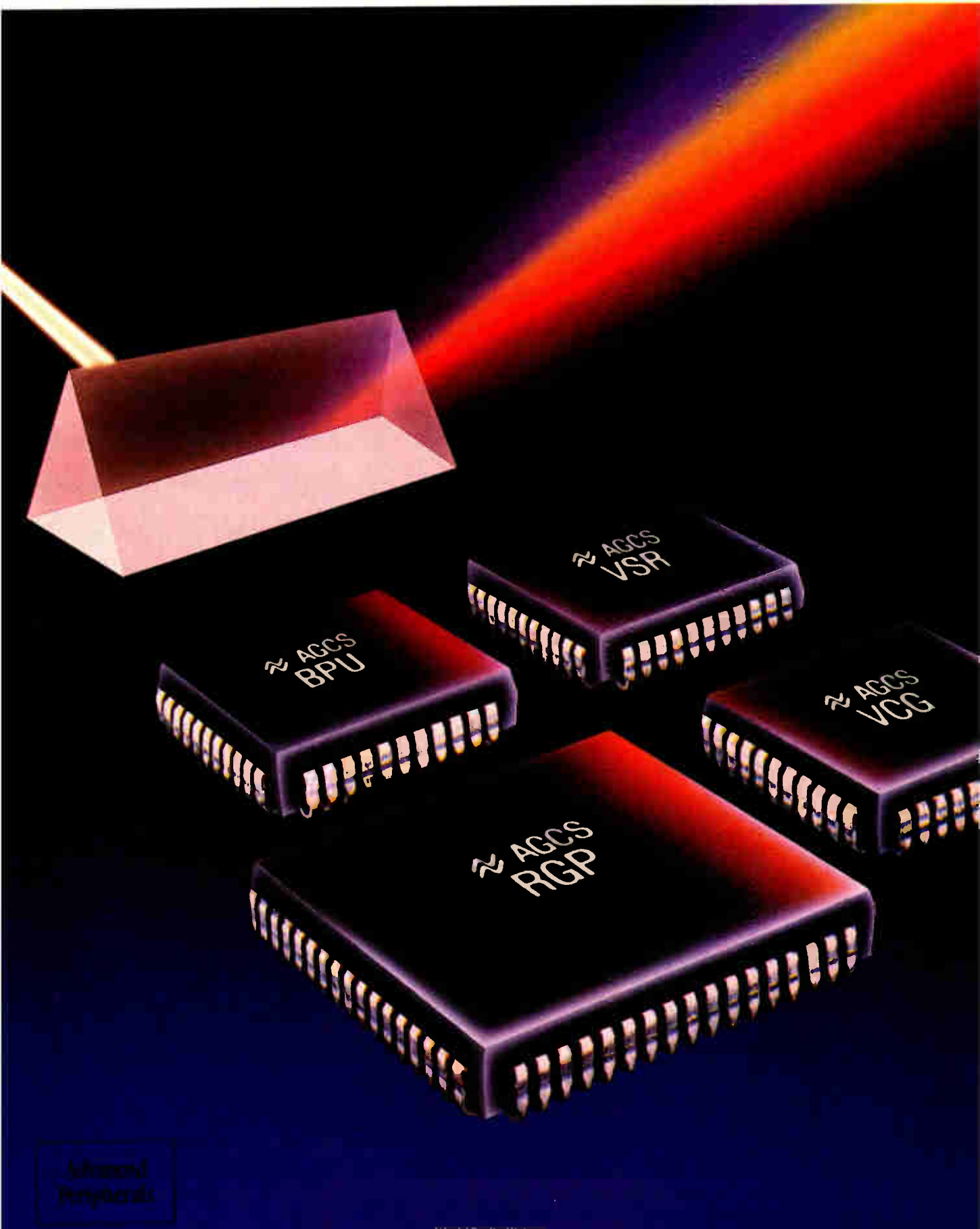
National Semiconductor



Advanced Peripherals

Finally, graphics to match your imagination.

INTRODUCING THE FIRST EFFECTIVELY PARTITIONED VLSI ARCHITECTURE FOR TRULY FLEXIBLE GRAPHICS SYSTEMS DESIGN

Imagine a graphics architecture so powerful, you can achieve 16K-by-16K resolution. So effective, you can add virtually unlimited planes of color without degrading performance. So flexible, you can integrate it into an existing design or use it to build an entire range of new systems.

That's the Advanced Graphics Chip Set from National Semiconductor.

By using a multiple-chip, modular approach, the Advanced Graphics Chip Set avoids the design compromises and limitations of single chip solutions.

That gives you two unprecedented benefits: *performance* and *flexibility.*

Which means you can design exactly the type of system you need with exactly the level of performance your application demands.

For example, you can integrate part of the chip set with an existing general-purpose microprocessor for a low-end display.

Or you can utilize the chip set's full capabilities for a high-end, high-performance, high-resolution CAE/CAD workstation or laser printer — with virtually unlimited planes of color. Yet with the same high-speed performance as a black-and-white application.

In fact, you can design an entire range of graphics systems without having to "reinvent the wheel" each time, by using the same hardware building blocks and the same central software in each of the systems.

THE ADVANCED GRAPHICS CHIP SET

Raster Graphics Processor (RGP). A fully programmable, high-performance microprocessor engine specially tuned for graphics applications. Samples available Second Quarter, 1987.

Bitblt Processing Unit (BPU). A 20-MHz data chip that controls data movements within its dedicated memory plane and between it and other memory planes in a multi-color system. Available now.

Video Clock Generator (VCG). A timing and control generator providing all of the synchronization signals needed by a graphics system, with a pin-programmable pixel frequency of up to 225 MHz. Available now.

Video Shift Register (VSR). A parallel-to-serial shift register capable of serial output shift rates up to 225 MHz. Available now.

All devices available in PLCCs.

THE MULTIPLE-CHIP SECRET

The secret to all this flexibility and performance is our unique multiple-chip, modular approach. Rather than trying to squeeze all the important graphics functions onto a single chip — which would require some significant design and performance compromises — we've partitioned appropriate functions onto individual building-block ICs. This allows us to optimize the design of each chip, and allows you to optimize your own design for your particular application.

GRAPHICS WITHOUT LIMITS

What matters most about the Advanced Graphics Chip Set, of course, is what it does for *you.* And that answer is clear when you consider its high performance, its modular approach, its open architecture, and its programmability: It gives you graphics without limits. It gives you true design freedom. It gives you the opportunity, for the first time, to design a graphics system "custom fit" to your exact specifications.

So what are you waiting for? If you're tired of those limited single-chip solutions bogging down your designs, take a look at the Advanced Graphics Chip Set. And learn how you can design a graphics system to match your needs . . . as well as your imagination.

For more information and availabilities, just contact your local National Semiconductor Sales Engineer or write:

National Semiconductor
Advanced Graphics, MS 23-200
P.O. Box 58090
Santa Clara, CA 95052-8090

National Semiconductor

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LETTERS

Keeping an eye on a trend

To the editor: Your recent article [*Electronics*, Feb. 19, 1987, "Intel Enhances 80386 with DMA, Cache Chips," p. 88] covering Intel's family of new 80386 products was reported and written well. However, an inaccuracy appeared which we would like to correct.

My comments had no reference to future products from any supplier.

The article incorrectly interpreted my comments that work-station manufacturers, such as Sun Microsystems and Apollo Computer, are offering 80286-based coprocessor boards in order to run DOS and Unix in the same system. This example was used to illustrate what Intel sees as a trend toward a standard platform, based on very large-scale-integration technology, and that the coexistence of Unix and DOS is now a requirement rather than an option in this market segment.

Dana Krelle
Product Line Marketing Manager
Advanced Processors
Microcomputer Group
Intel Corp.
Santa Clara, Calif.

It was right the first time!

To the editor: Your original story about Honeywell's decision to phase out our commercial-product effort in digital gallium arsenide integrated circuits [*Electronics*, Dec. 18, 1986, "Honeywell drops product efforts in commercial digital GaAs," p. 21] is accurate. Unfortunately, your brief reference in the Jan. 8 issue, p. 24, is inaccurate.

In paraphrasing your Dec. 18 story, you leave readers with the impression that we are dropping the technology entirely. Nothing could be further from the truth. Our activities in gallium arsenide will be consolidated at our Physical Sciences Center in Bloomington, Minn., where GaAs research and development will focus on aerospace and defense applications. The Physical Sciences Center currently makes both digital and analog integrated circuits.

We believe GaAs ICs will be critical components for many Defense Department systems related to our aerospace and defense business. Therefore, Honeywell is continuing to make substantial investment in GaAs and to aggressively pursue programs of mutual interest with the DOD and other industrial organizations.

We hope this clears up the confusion some of our customers have shown over the January 8 reference.

Susan M. Eich
Corporate Public Relations Manager
Honeywell Inc.
Minneapolis, Minn.

Cramped for space?

Ultra-miniature snap action switch. Fits where other switches won't ...or can't. So small, a lot of them will fit into your densely packed PC board.

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C&C is in-depth integration of computers and communications
to make information interchange between nations
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Dramatic proof of NEC's powerful resources
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Find out for yourself why the best links are by NEC.

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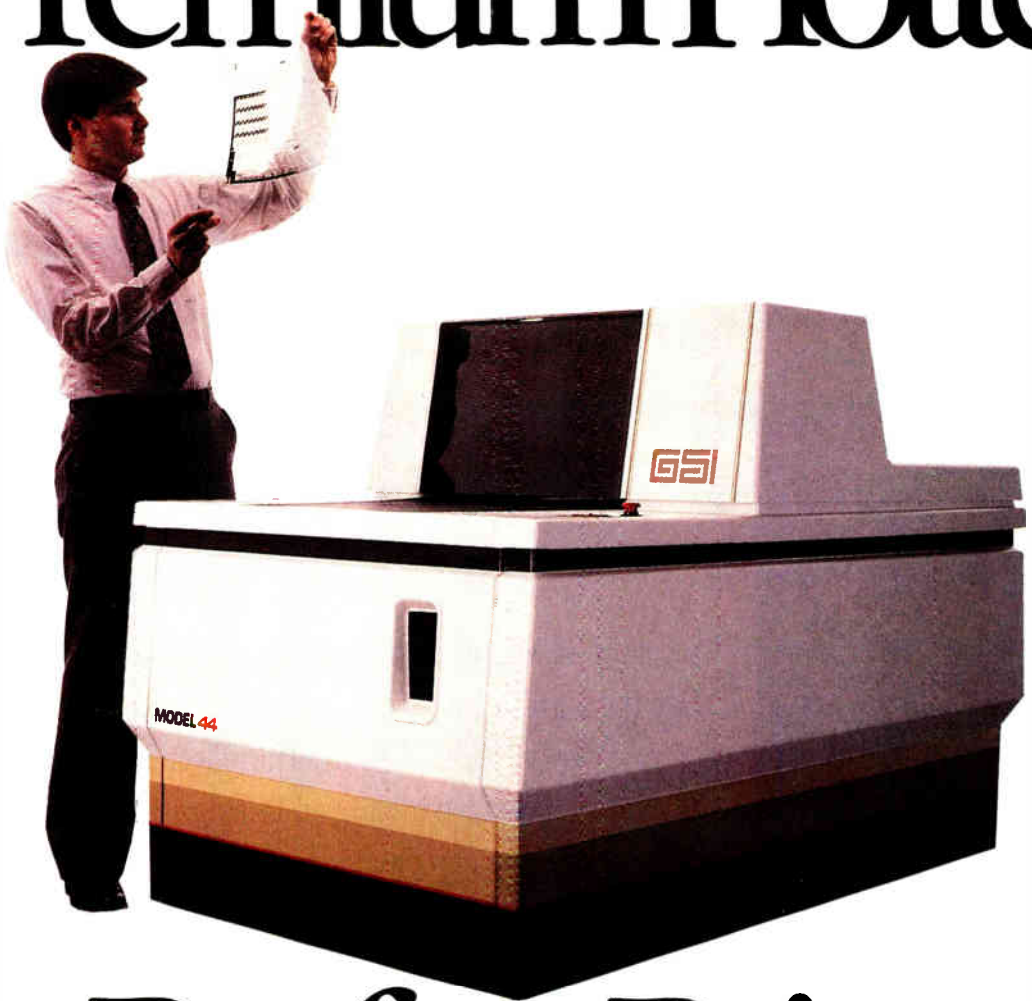

Perfect Price.

The Gerber 3244 photoplotter represents a brand new approach to photoplotting. We created new optics, new mechanics, a new generation in software, all for only $34,750!* And, the Model 3244 has simple pushbutton operation too. Now, precision artwork generation is within the reach of every serious PC designer.

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*Price in U.S.A.

All Life Insurance Lets You Provide For Your Children. Ours Lets You Buy Toys Of Your Own.

Tiny pianos are fine for three-year-olds. But we can help you get one that's really grand.

Vrooom!! Model cars were never like this.

Why settle for being the first kid on the block when you can be the first one over it.

Every kid wants a bike. We'll help you get one that's just your size.

Don't take a bath. Get the boat of your dreams.

It's very commendable to provide for your children. But with an Integrity Single Premium Life insurance policy, you can provide for yourself.

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Simple. You pay your premium in one single payment. From that instant, your money grows substantially. As long as your policy is in force, all gains are completely tax-deferred.

A loan with real interest—it's free.

If you wish to borrow against your policy, you can do it at a cost that nets out to zero. You suffer no adverse tax consequences. And you never have to pay back any of the money (although your loan does affect the amount of your death benefit or cash surrender value).

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It's risk free! Your principal and interest are guaranteed against loss by contract with Integrity Life. And they're *always* available to you (less, of course, any surrender charges where applicable).

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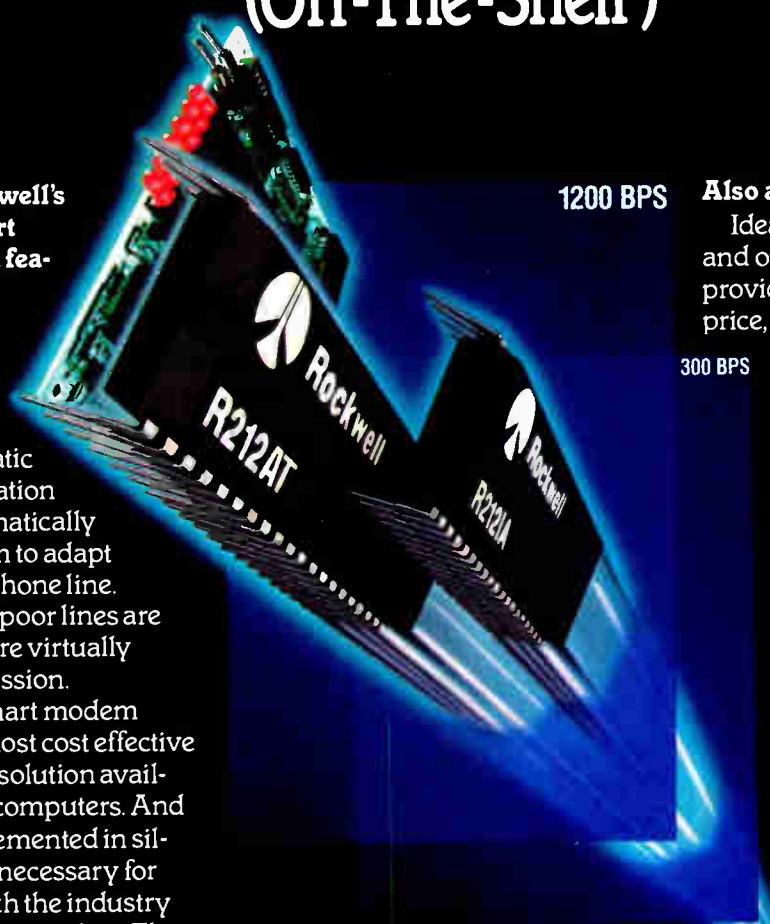


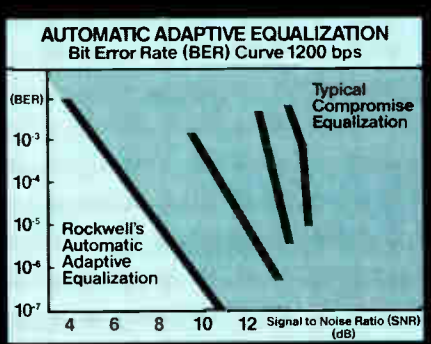
Introducing Rockwell's new R212AT smart modem device set featuring Automatic Adaptive Equalization.

Rockwell International's exclusive Automatic Adaptive Equalization Algorithms automatically enable the modem to adapt to any quality of phone line. Even signals over poor lines are enhanced to ensure virtually error-free transmission.

The R212AT smart modem device set is the most cost effective communications solution available for personal computers. And R212AT has implemented in silicon the software necessary for compatability with the industry standard "AT" command set. This allows quick design-in because we've presolved all the "AT" dialing functions. It incorporates auto dial, auto answer and can dial DTMF tones or pulses.

The R212AT smart modem offers lower system cost because it incorporates the controller and analog filter circuitry required for modem communications in the device set itself. This reduces parts count, enhances total system reliability and meets low power requirements for portable applications.

As well as operating asynchronously, the R212AT has synchronous mode operation for higher transmission throughput.



Also available: Rockwell's R212DP.

Ideal for remote diagnostics and other integral applications, it provides specific advantages in price, performance and system cost savings.

The R212DP, like the R212AT, has automatic fall back to slower speeds and an RS232C interface. Both these Bell 212A and 103 compatible device sets are available at any level of integration from devices to boards or customized private label systems.

For ease of evaluation, Rockwell provides a board level evaluation modem for laboratory analysis to assure the performance and quality of R212AT and R212DP.

Call your local Rockwell distributor today for off-the-shelf delivery of an evaluation board complete with a Designer's Guide Kit.

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ELECTRONICS NEWSLETTER

APPLE SLICES OPEN THE MAC TO TAKE ON SUN AND IBM

Apple Computer Inc. is moving to break Sun Microsystems Inc.'s grip on the low-end work-station market and IBM Corp.'s dominance in corporate personal computing with the announcement of its long-awaited Open Macintosh hardware. The Macintosh II is controlled by a 15.67-MHz Motorola Inc. 32-bit 68020 microprocessor and features six expansion slots that allow users to transform the machine into a Unix or MS-DOS work station. The Unix add-on will be developed jointly by Apple and Unisoft Systems Corp., Scotts Valley, Calif., and will be based on AT&T System V Unix plus enhancements from the Berkeley 4.2 Unix version. MS-DOS plug-in boards are expected from Phoenix Technologies, AST Research, and Radius. Priced from $4,000 to $10,000, the Mac II comes with a 68881 floating-point coprocessor, up to 8 Mb of random-access memory, 256 K of read-only memory, an 800-K 3.5-in. minifloppy-disk drive, optional 20-, 40-, or 80-megabyte Small Computer Systems Interface hard-disk drives, and monochrome or color monitors displaying up to 16.8 million colors at 640-by-480-pixel resolution. To reach business users, Apple is launching the under-$3,000 Macintosh SE. The 68000-based machine comes with one expansion slot, up to 4 Mb of RAM, two double-sided 800-K 3.5-in. drives, two RS-232-C ports, and a 9-in. monochrome screen. □

TI's LISP CHIP COULD SPUR BOOM IN AI APPLICATIONS DEVELOPMENT

In packing the power of its Explorer artificial intelligence work station onto a single-chip Lisp microprocessor, Texas Instruments Inc. is setting the stage for a boom in AI applications development. The 32-bit VLSI chip, formally announced at ISSCC in New York (see p. 58), is at the heart of the Compact Lisp Machine, a set of four 6.5-by-5.9-in. circuit boards with 2 Mb of random-access memory and a 40-ns cycle time. The Dallas company will deliver the board set, which will allow expert systems to be crammed into tight spaces aboard aircraft and tanks, to the Defense Advanced Research Projects Agency in June. Commercial AI developers expect the same power in a single-board version that is reportedly under development. □

AT&T UNVEILS NEURAL-NETWORK ASSOCIATIVE MEMORY AT ISSCC

The AT&T Bell Laboratories announcement at ISSCC in New York that it has developed a CMOS associative-memory chip based on neural networks indicates the direction that electronic circuits will be taking in the future. Fabricated using relatively conservative 2.5-μm design rules, the 75,000-transistor chip implements an algorithm based on biological neural networks that can recall 10 vectors stored in the memory within 500 ns. Dissipating only 500 mW, the chip contains 54 amplifiers, 6-K of static random-access memory, and programmable interconnections. Nipping at AT&T's heels are about half a dozen startups, such as Synaptics Inc. and Nestor Inc., that are trying to commercialize neural-network technology. □

NEC RAMPS UP U.S. PRODUCTION OF 256-K DRAMs BY 50%

NEC Corp. of Japan is moving more aggressively into the U. S. memory market through its wholly owned U. S. subsidiary. NEC Electronics Inc. is increasing production of 256-K dynamic random-access memories at its Roseville, Calif., plant by 50% and plans to make 3 million chips a month there by June—enough to supply 15% to 20% of U. S. demand. The U. S. subsidiary, which had been pricing its parts at the Department of Commerce's foreign-market value levels intended for its Japanese parent, is now cutting prices to between $1.70 and $1.80. □

ELECTRONICS NEWSLETTER

IT'S AN ALL-OUT RACE TO ADAPT UNIX TO INTEL'S 80386

Just days after AT&T Co. and Microsoft Corp. launched a bid to nail down an industrywide standard for Unix, Microport Systems Inc. added its name to a growing list of vendors racing to be first to market a version of the operating system tailored for Intel Corp.'s powerful 32-bit microprocessor, the 80386. Microport, of Scotts Valley, Calif., plans an April release of Runtime System V/386, a $299 operating system based on AT&T's Unix System V. Previously, Interactive Systems Corp., Santa Monica, Calif., said it would offer an 80386-based Unix release late this year [*Electronics,* Feb. 5, 1987, p. 31]. AT&T and Microsoft have not set a release date for their package, but they say it will incorporate features of Microsoft's System V-compatible Xenix and AT&T's Unix System V, Release 3. If the joint effort works, software developers will be able to market Unix applications for all 80386-based systems. □

GAIN ELECTRONICS STARTS SAMPLING A 3,456-GATE GaAs ARRAY

Gain Electronics Corp., a Somerville, N. J., startup, says it's entering the sampling stage with what it claims is the world's largest commercially available gallium arsenide gate array. The 5-by-5-mm chip has 3,456 equivalent gates and 140 input/output pins and is being touted as a high-speed, low-power alternative to emitter-coupled-logic silicon parts. Gain is incorporating its own device architecture, called GaAs FET logic, or GFL, into the new gate array, which will feature gate delays of only 100 ps and will be able to handle frequencies up to 1 GHz. But the chip's greatest advantage is that it dissipates just 2 W, much less than ECL parts, which can dissipate up to 15 W or more. The new gate array is compatible with ECL, TTL, and CMOS technologies, and Gain says it will be priced just less than double the going rate for the ECL gate arrays it aims to replace. □

CDC TO USE THIN-FILM SPUTTERING TO TURN OUT DENSER 8-IN. DISKS

High-capacity 8-in. magnetic disks could become a lot more common next year as a result of a deal between Control Data Corp. and Varian Associates Inc. to develop thin-film sputtering technology. Varian's Thin Film Technology Division, Santa Clara, Calif., is shooting to deliver an 8-in. disk-sputtering system to Magnetic Peripherals Inc., Control Data's captive disk-drive maker, by January. Magnetic Peripherals will pay $2 million to help Varian develop the system. Varian uses a circular source to sputter disks one at a time, an approach Control Data believes offers the most potential to improve yields on high-quality sputtered disks. □

KODAK TARGETS EMERGING MARKET FOR MOLDED PC BOARDS

Eastman Kodak Co. is taking aim at an emerging technology market that is rapidly becoming crowded with big-name competitors. Kodak's new venture, called Pathtek, will address the market for molded plastic printed-circuit boards that has already been targeted by the likes of DuPont, General Electric, and ICI Americas [*Electronics*, April 21, 1986, p. 63]. Kodak hired David C. Frisch—a pioneer in plastic-pc-board technology when he was with PCK Technology of Melville, N. Y.—to be vice president of marketing at Pathtek, which, like its parent, will be based in Rochester, N. Y. Pathtek is the latest in a string of new ventures for Kodak, which is slowly moving to become a broad market supplier of specialty electronics goods. Previous ventures, all started in the past two years, include Fastek, which makes dielectric thin-film materials; Videk, a machine-vision firm; and Ultra Technologies, which makes nickel-cadmium batteries. An electronics components venture is also likely. □

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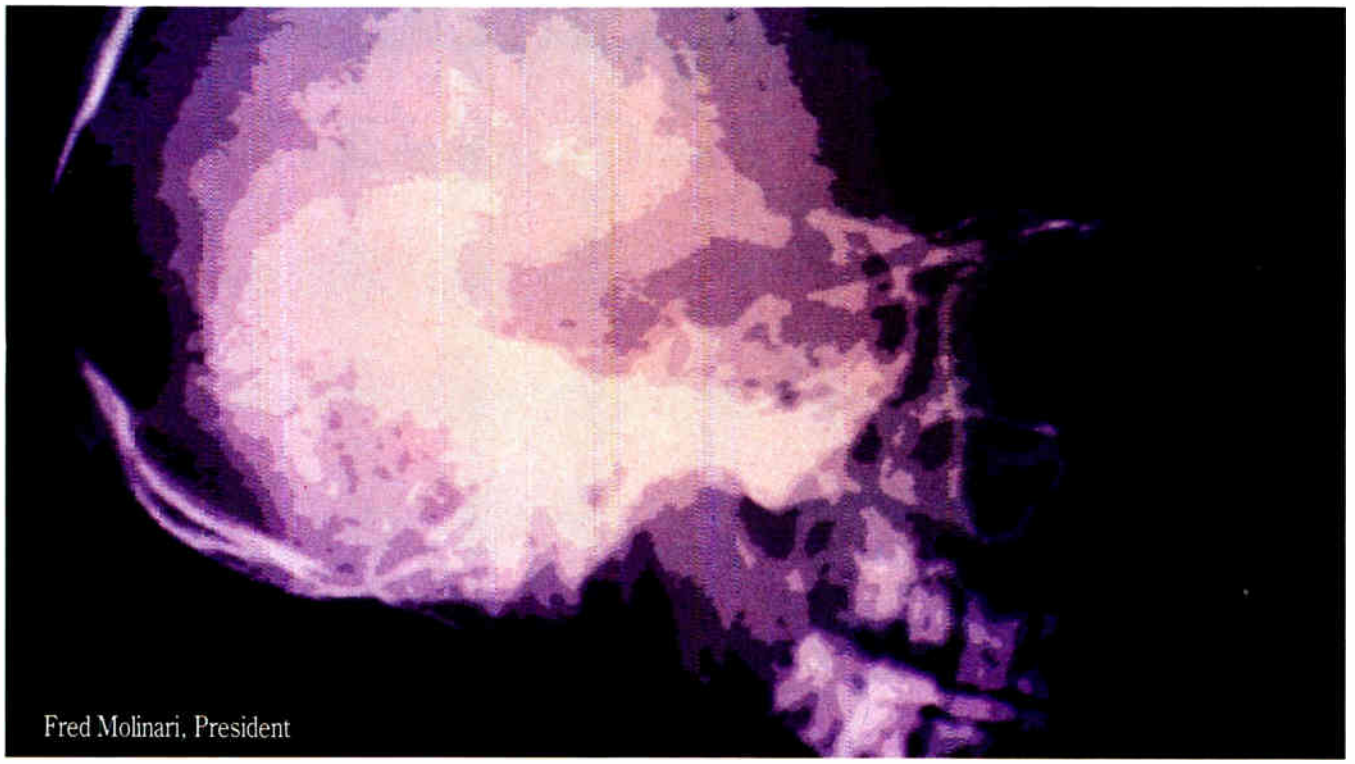

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DT2803 Frame Grab	PC, XT, AT	256x 256	64	✓	✓		8*	✓	✓	1 Buffer, 256x256x8 (64 KB)			VIDEOLAB ($995) PC SEMPER ($145)	1495
DT2851 Frame Grab and DT2858 Frame Proc	PC, AT	512x 512	256	✓	✓	✓	8*	✓	✓	2 Buffers 512x512x8 (512 KB) and 1 Buffer, 512x512 x16 (512 KB)	✓	✓	IRISutor (free) DT IRIS ($995) PC SEMPER ($195) DT Image Pro ($1495)	2995 1695

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PRODUCTS NEWSLETTER

SILICON COMPILERS UNBUNDLES GENESIL INTO FIVE PRODUCTS

By unbundling and networking its $200,000 Genesil silicon compiler into five less expensive products, Silicon Compilers Inc. is opening a window of opportunity for many more chip designers—those who don't need all five of these advanced design tools. The San Jose, Calif., company's $79,500 Logic Designer lets designers perform the front-end circuit design. Silicon Compilers does the final layout. The $119,000 Chip Builder runs on Digital Equipment Corp. MicroVAX II and provides the physical layout service for designers using Logic Designer. The $159,000 Mentor Series lets designers run Genesil on Mentor Graphics Corp.'s Idea work stations. A fourth product, Server, ports the Genesil compiler to a DEC VAX on the Mentor network. Licenses cost $450. With the fifth product, Microcompiler, designers can compile random-access memories, read-only memories, and other logic functions and transfer the layout to a design containing standard cell and macrocell library functions. All products are available now. □

NCR COMPUTER GOES FROM 2 TO 8 MIPS WITH PLUG-IN PROCESSORS

NCR Corp.'s Tower 32/800 quadruples the high-end performance of the multiuser, Unix-based computer line—while creating an easy-upgrade path for 32/800 users. Users can plug in additional 32-bit processors and boost performance to 8 million instructions/s, four times the performance of the previous high-end Tower, the 32/600. The new system from the Dayton, Ohio, company can be configured with up to four Motorola Corp. 68020-based applications processors, which work with a variety of specialized, 68010-based processors in a loosely coupled architecture. Pricing ranges from $85,000 for a one-processor system with 4 megabytes of main memory to $250,000 for four processors, each with 16 megabytes of internal memory and 850 megabytes of integrated hard-disk memory. One- and two-processor systems will be available next quarter, the others in the third quarter. □

HP PRINTERS AND SCANNER ARE AIMED AT DESKTOP PUBLISHING

Hewlett-Packard Co., following up on its desktop publishing alliance with Microsoft Corp. and Aldus Corp., has introduced two printers and a scanner for personal-computer users. The Series II printer, rated at 8 pages/min., is priced at $2,495. The desktop ScanJet costs $1,495 and can be linked to an IBM Corp. PC AT/XT or compatibles, or to an HP Vectra using a $495 interface card. The system supports Microsoft Windows and the Aldus Pagemaker composition system. The midrange printer, the LaserJet 2000, has a speed of 20 pages/min. The LaserJet 2000 costs $19,995. All three of the products are available now. □

WAVE TECHNOLOGIES TIMER HANDLES INTERVALS DOWN TO 50 ps

The Timing Measurement Unit from Wave Technologies Corp. can accurately measure intervals of time on a single reading down to 50 ps, with 1-ps resolution—a single-shot accuracy about five times better than competitive equipment, says the Edina, Minn., company. By taking multiple readings and averaging, users can push accuracy down below 5 ps, a company official adds. The timer relies on an Intel Corp. 80286/80287-based single-board computer to handle timing-algorithm number crunching, and comes complete with an IEEE-488 interface. Wave sees applications in high-speed integrated-circuit testing, radar calibration, and communications. Initially to be marketed as a portable unit, the timer will be sold to chip manufacturers as an upgrade for their existing very large-scale-integration test systems. It is priced at $41,950 and will be available in late April. □

PRODUCTS NEWSLETTER

NEC's SMART CACHE CHIP BOASTS 95% HIT RATE

A 95% hit rate in NEC Corp.'s new 8-K-byte general-purpose cache memory chip—comparable to the hit rates in application-specific cache subsystems—promises to boost throughput for computers using the latest high-speed microprocessors. The intelligent μPD43608R cache memory works with popular 32- and 16-bit microprocessors, including Intel Corp.'s 80386, Motorola Inc.'s 68020, and NEC's V series. The high hit ratio is achieved with the same kind of four-way-set associative-placement algorithm that is used for cache-memory subsystems in mainframe computers and superminicomputers. □

GENOA SYSTEMS BACKS UP LAN DATA WITH TAPE DRIVE

A new breed of tape backup from Genoa Systems Corp. harnesses the San Jose, Calif., company's 120-megabyte Galaxy II tape drive and new NetSafe software package to create a shared tape server for local-area networks of personal computers. Until now, each LAN computer would have required a separate backup. The Netbios-compatible server performs real-time backup and restore functions while operating from a background-mode process on the computers. Models of Galaxy II, available 30 days after order, cost $1,145 to $1,395. The NetSafe package costs $449. □

20-MEGAFLOPS MINISUPERCOMPUTER COMING FROM PRIME

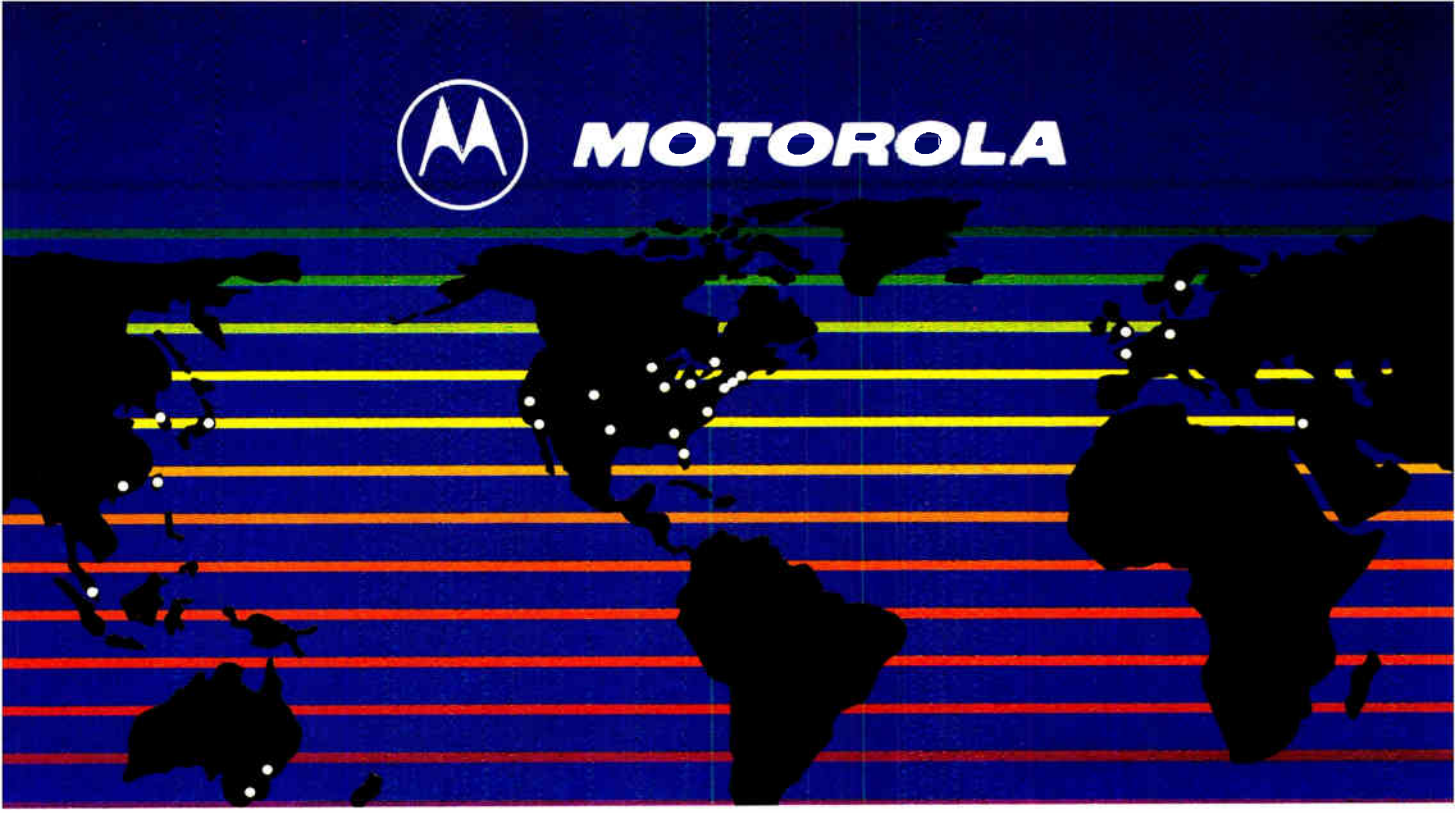
Prime Computer Inc., Natick, Mass., will jump into the minisupercomputer market by early May with a machine that executes from 5 million to 20 million floating-point operations/s. The Unix-based machine will cost upwards of $500,000 and is being built in a cooperative effort with Cydrome Inc. of Milpitas, Calif. It will be among the first in a series of major product announcements from Prime in the near future. Waiting in the wings are a new high-end product for the Prime 50 minicomputer series and a reduced-instruction-set-computer work station. □

MASSCOMP BOOSTS MICROSUPERCOMPUTER PERFORMANCE 35%

Masscomp will boost performance of its line of microsupercomputers by 20% to 35% with three new models incorporating the Motorola Inc. 68020 microprocessor. Base prices for the MC5350, MC5450, and MC5550 are $15,250, $22,750, and $29,750, respectively. Customers can upgrade older MC5300, MC5400, and MC5500 models, which will continue to be sold, with performance-enhancement packages priced from $4,250 to $5,000. In addition, the Westford, Mass., company says its multiprocessor MC5700 will now support up to six central processing units, as opposed to an earlier limit of four. Additional CPUs for the 5700 will cost $16,000 each. □

APPLIED PHYSICS CARD MONITORS PC BUS LINES WITH LESS HASSLE

Personal-computer service technicians and hardware and software engineers can quickly and conveniently monitor bus lines on IBM Corp. Personal Computers with the BusMate card from Applied Physics Inc. Rows of pins on each side of the card connect to bus lines in the system. With an oscilloscope or bus analyzer, users can monitor activity without probing the system motherboard, an approach that would require removing any expansion cards. BusMate can be used as an accessory to the West Lafayette, Ind., company's $249 Crowcard [*Electronics*, Oct. 16, 1986, p. 138], which does not have probe pins. BusMate will be available late this month, at $79 for the PC and XT versions and $89 for the AT model. □



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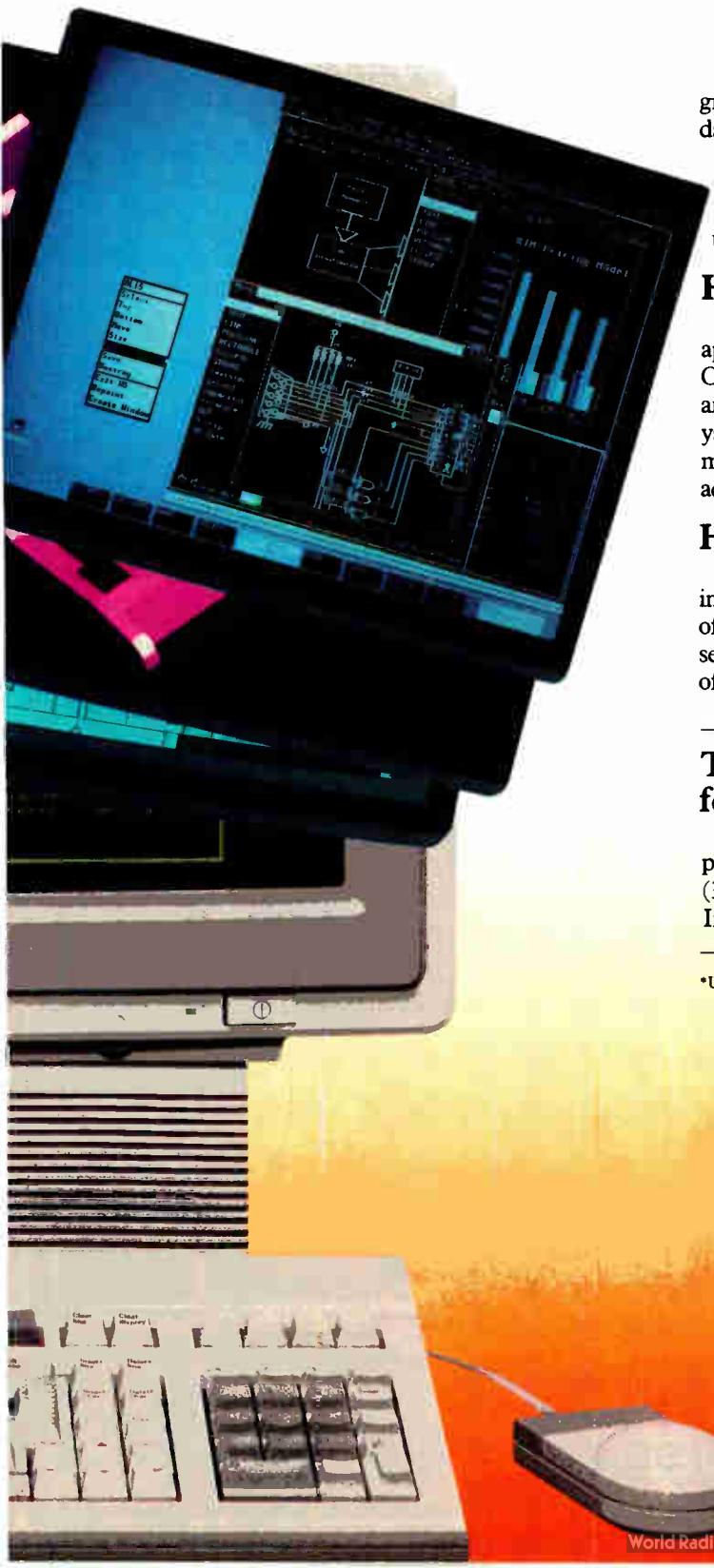

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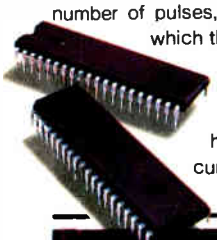
ESS-910G



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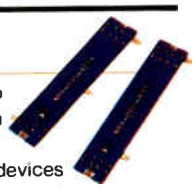
NOISE CANCELER



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Electronics

U.S. INC.: IC MAKERS STILL DEBATE ROLE OF PRODUCTION CONSORTIUM

SHOULD SEMATECH MAKE MEMORIES FOR THE OPEN MARKET?

WASHINGTON

The public should soon get its first peek at the outlines of Sematech, the proposed government-industry consortium to develop advanced semiconductor manufacturing techniques for U.S. chip makers. But even as plans for the consortium are firmed up for presentation at the Semiconductor Industry Association's annual meeting on March 4, one major issue has yet to be resolved: should the consortium manufacture products for the open market?

An SIA task force is to report on the technical and funding aspects of Sematech at the meeting in Washington, D.C. Reportedly, the group will propose that Sematech be funded both by merchant suppliers of semiconductors and by their customers, with annual dues amounting to 1% of sales.

That would raise about $100 million; another $100 million to $200 million would be provided by the Department of Defense. But despite a widespread feeling that the embattled U.S. chip industry needs some sort of government support to avoid being swallowed up by Japanese competitors, SIA members remain divided over the question of manufacturing.

A government panel has already come out on the side of manufacturing in its Sematech report. The document, issued last month by a Defense Sciences Board task force, envisions the consortium developing manufacturing techniques for a 16-Mb dynamic random-access memory. To test the technique, the report says, Sematech would have to sell in the open market.

MAYNARD: "It's not aimed at saving the semiconductor industry or reversing trends."

This appraisal was part of the Defense panel's recommendation that the Pentagon support some kind of manufacturing consortium to the tune of a billion dollars over the next five years. The DSB justifies its support on the grounds that a healthy commercial semiconductor industry is necessary to ensure a supply of chips for the military. "It's not aimed at saving the semiconductor industry or creating jobs or reversing global economic trends," says E. D. Maynard Jr., executive secretary of the task force.

The sum proposed in the report is deemed sufficient by the industry, but the question of how to use that money is still far from settled. The idea of a government-sponsored consortium competing against some of its members has proved divisive among potential members. Accordingly, the SIA is exploring ways to satisfy both sides.

"There may be room, as we develop the Sematech concept, for a second phase," says one SIA task force member, George Scalise, vice president for government affairs at Advanced Micro Devices Inc. "Phase 1 would develop the technology, manufacturing, and software needed for submicron products. It would include the folks who do not want a large manufacturing facility. Phase 2 may entail the formation of another entity, a genuine manufacturing facility for semiconductor commodity production, separate from Sematech."

Individual companies are also reportedly divided on whether the consortium should develop actual process technology or stick to automation, shop-floor control, and computer-aided manufacturing. Process development would require the inclusion of equipment makers and enforce the development of equipment standards, a move opposed by some of Sematech's most vigorous supporters.

Both industry and government panels are under the pressure of time, since they agree that some kind of consortium has to begin this year to have much effect. The panel hopes to have a more detailed plan within 60 days, Maynard says. *–Clifford Barney*

MITI MOVES TO HEAD OFF THE THREAT OF U.S. PROTECTIONISM

The U.S. electronics industry's disenchantment with the U.S.-Japanese pact on semiconductor trade continues to grow. The Semiconductor Industry Association says that the U.S. government and chip makers are losing $750,000 a day in foregone dumping duties and lack of increased sales opportunities in Japan. At the same time, the Japanese are trying to head off what they now perceive as a growing threat of protectionist backlash from Congress. The Ministry of International Trade and Industry is making two moves.

MITI is asking that Japan's six leading memory makers—Fujitsu, Hitachi, Mitsubishi Electric, NEC, Oki, and Toshiba—reduce by 20% production of selected memories for the rest of the quarter. Affected are 256-K dynamic random-access memories and 64-K, 128-K, and 256-K erasable programmable read-only memories. MITI also announced plans to help U.S. manufacturers sell in Japan by providing information on the Japanese market, putting on exhibitions and symposiums, and evaluating the quality of foreign semiconductor products with a new International Semiconductor Cooperation Center.

But the Japanese have previously used the strategy of limiting production after first capturing a market by overproducing—for example, Japan's major integrated steel makers announced plans to shut down a number of blast furnaces within days of each other. However, in that and other cases, they were still able to retain market share. *–Charles L. Cohen*

WILL DEC PUSH MULTIVENDOR COMPUTING?

BOSTON

The drive to set a *de facto* standard for multivendor computing, which got a recent push from Apollo Computer Inc., looks as if it will get a major shove from an unlikely source: Digital Equipment Corp. A standard for multivendor computing would let a user execute a single program across a network of computers from different companies. It would obviate the need for a customer to buy hardware from a single vendor and would allow smaller companies to compete with industry giants on a more even footing.

Work-station companies in particular are competing to set this standard. Right now, the strongest contender to lead the drive is Apollo Computer Inc., with a new distributed-processing multivendor environment called the Network Computing System [*Electronics*, Feb. 19. 1987 p. 18]. Sun Microsystems Inc. earlier proposed its own scheme.

Apollo's environment product is scheduled for delivery in the third quarter, but DEC hints it may be on the scene at the same time with its own offerings. "If you were to look to DEC at the same time Apollo promises [to deliver] its product, you might find that its product doesn't stand alone," says Steve Wendler, a DEC product marketing manager.

The Maynard, Mass., company has apparently decided this advanced form of distributed-processing computing is on the horizon and must be embraced quickly. Such software could negate DEC's proprietary advantage, which has been a comprehensive single-architecture line of computers.

Some measure of customer interest in this area should come at an Apollo-sponsored forum in Boston on March 4 to foster practical applications for network computing. Scheduled to attend the meeting are representatives from General Electric, Rockwell International, Motorola, and Westinghouse, as well as Alliant, Convex, Concurrent, and several software applications companies.

NEEDED FOR GROWTH. At least one analyst sees the drive for a distributed computing standard as a key to the future of the work-station business. "[It's] the single largest roadblock to long-term sustained growth," says Mark Stahlman, a research analyst with Sanford C. Bernstein and Co. in New York. Major computer users will buy quantities of work stations from the smaller vendors only if they are confident that these work stations will tie into machines from the big mainframe and minicomputer makers, he says.

APOLLO'S NELSON: "A year from now we'll see applications based on this technology."

Apollo's NCS includes a remote procedure call specification, which makes it possible for one computer to request a second computer to run a procedure for it. The Chelmsford, Mass., company couples it with tools that make it easy for a software developer to write applications using multivendor computing resources.

Apollo plans to aggressively market the Network Computing System by working with the major applications programmers to develop versions of their software that are tailored to multivendor computing, says David Nelson, vice president and chief technical officer. "A year from now, we'll start to see some applications based on this technology," says Nelson.

Caught off guard by the drive to commercialize the concept—and also by the strategy of taking the idea directly to applications programmers—is Sun Microsystems Inc. The Mountain View, Calif., work-station maker for two years has been quietly promoting its own multivendor computing protocol, Remote Procedure Call Specification.

"That's a very different slant [Apollo is] taking, but we feel until you have the vendors agree on a communications standard you don't have anything to bring to people," says Martha Vivoli, Sun systems software product manager.

But with Apollo's hard push in this area, Sun is coming under pressure to push its remote-procedure-call spec harder. Even some licensees of Sun's system now say the company could have done a better job of promoting its remote-procedure-call spec.

"Sun has not marketed it well," says Christopher Gregory, a marketing specialist at Computervision in Bedford, Mass. "Sun should have been trying to tell people you can communicate on an applications level, not just on the operating system level." *–Craig Rose*

AUSSIES EMPLOY OLD IDEA IN NEW NONVOLATILE CHIP

NEW YORK

An Australian company has resurrected an old idea that could lead to a new nonvolatile semiconductor memory type. The ferroelectric random-access memory, or FRAM, has cell areas equivalent to those of dynamic RAMs—4 μm^2. It also boasts significantly faster read-erase-rewrite cycles than electrically erasable read-only memories—on the order of 100 ns for production devices.

Prototypes of 256-bit and 1-K FRAMs with 20-ns access times should be ready late this year, says Ross Lyndon-James, deputy director of Newtech Development Corp. of Pymble, Australia; production should begin in 1988 or 1989. Newtech and its U.S. subsidiary, RAMtron Corp. of Colorado Springs, Colo., are fabricating the devices by implanting a potassium nitrate (KNO_3) film on a conventional silicon or gallium arsenide substrate.

Newtech has initially targeted the EEPROM market, but FRAMs should lend themselves readily to application-specific design. Lyndon-James admits that at 30 to 40 ns, EEPROMs read faster than FRAMs, but they take milliseconds to erase and write. This is where the FRAM shines. It erases and writes at the same speed it reads because the ferroelectric material can be selectively addressed: changing polarity involves just that cell. In EEPROMs, every cell must be erased to change just one.

Besides their speed and density, FRAMs offer numerous other advantages. They are inherently radiation hard, can easily be scaled up to 1 Mb, are substrate-independent, and offer an extended programming capability of

10^{14} read/write cycles compared with 10^6 for EEPROMs, says Lyndon-James.

Access times depend on film thickness and voltage. Laboratory devices that achieved 20-ns access times used 700-Å films and 6 V. The 256-K devices envisioned for demonstration prior to licensing for production probably will have thicker films and operate at 2 to 5 V, yielding 100-ns access times, says Newtech consultant James Scott, a physics professor at the University of Colorado.

FRAMs still have a few bugs to be worked out, says vice president Robert Venos. First, KNO_3 is hydroscopic, which means it must be hermetically sealed with a passivation layer guarding against atmospheric exposure. Second, 1,500- to 2,000-Å films have resulted in 10^6 erase-write cycles—not the 10^{14} of the lab device. But the thicker films are primarily being used because they make characterization easier, and Venos believes higher performance is attainable. "Speed seems to be a function of thickness, too," he says.

SECOND TRY. FRAM development efforts undertaken in the late 1950s by Bell Laboratories and IBM Corp. were abandoned when the silicon technology of DRAMs succeeded. In the past two decades, small companies and individual researchers have slowly chipped away at the problems of FRAMs. A thin-film processing technology has been developed, and the problem of memory bits changing polarity when only half voltage is applied has been solved by a proprietary architecture, says Scott.

Newtech is not saying much about that architecture except that the KNO_3 film holds the charge by internally polarizing its structure. Most ferroelectric materials lose this charge-holding capability when reduced to a thin film. KNO_3 chips made a decade ago still hold their charge, says Scott.

Applying the KNO_3 film is a post-production process: tiny cells of KNO_3 are implanted on top of the silicon logic produced at a conventional fab house. The film can be applied either by thermal evaporation or sputtering. Process temperature is proprietary—KNO_3 vaporizes at 375°C—but is less than the 1,000°C that would harm the silicon substrate, says Scott. Structural problems such as lattice mismatch are avoided by using a metalization layer—prototypes using gold and production metalization techniques are still secret.

Lyndon-James says it's too early to talk about pricing. "The devices will be a little more expensive than EEPROMs at first," he says. "But we are starting with an inexpensive material and will use three to five mask steps on top of the silicon, so in terms of process steps it will not be expensive."–*Jack Shandle*

WORK STATIONS

IBM PLAYS CATCH-UP WITH NEW RT PC

NEW YORK

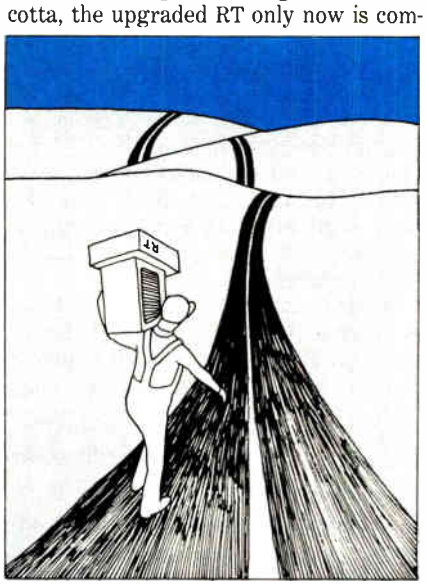
IBM Corp.'s latest effort to crack the market for work stations—an area in which it has long been vulnerable—is meeting with a lukewarm response, at best. IBM reported late in February that it had nearly doubled the speed and power of its work-station entry, the RT Personal Computer, but most observers say the enhancements were no more than what IBM should have offered in the first place.

The Unix-based RT so far has done poorly against the popular work stations of Apollo Computer, Digital Equipment, and Sun Microsystems, and the recent announcements were not unanticipated. "This is pretty much what we expected last year with the original RT," says Jim Ricotta, product manager for high-end work stations at Sun Microsystems Inc. in Mountain View, Calif. He says a performance boost was expected several months ago.

KEEPING UP. Meg Lewis, vice president at market watcher Future Computing Inc. in Dallas, says that "this is not a tremendously exciting announcement, [but] it is important to IBM. Basically, what they're doing is keeping up."

The enhanced RT is built around a new IBM 32-bit microprocessor that incorporates the same reduced instruction-set computer architecture that IBM used in the original RT. But by switching from 1.8-μm n-MOS technology to a 1-μm CMOS process, IBM was able to put more transistors on a smaller chip, thereby nearly doubling the RT's speed while reducing its appetite for power.

Incorporating the same 1-Mb dynamic random-access-memory chips that are used in IBM's newest 3090 mainframes [*Electronics*, Feb. 5, 1987, p. 45] also helped to boost the RT's performance. But that performance level is still not earth-shattering. According to Sun's Ricotta, the upgraded RT only now is competitive in terms of performance with the Sun 3 work station, a midrange offering introduced more than 18 months ago.



Although IBM claims the RT is exceeding its sales goals, Lewis estimates fewer than 20,000 machines were sold in 1986, and Brad Smith of Dataquest Inc., San Jose, Calif., puts last year's sales as low as 3,000. Both analysts and competitors seem to think the RT will carve out a small segment of the $1.54 billion work-station market—perhaps 5% or so.

"The RT is a vague threat, but it's certainly not an Apollo killer or a Sun killer," says George Colony, an analyst with Forrester Research Inc. of Cambridge, Mass. "It's an irritant to them." Lewis, of Future Computing, adds that IBM is probably not very worried about competition from Apollo and Sun, which are relatively specialized firms, but "would prefer to clobber Digital, because it has traditionally been strong against IBM in the midrange market."

NO CHALLENGE. No one seems to think the RT offers a major challenge to the Apollo, DEC, or Sun products. For example, only about 200 application packages currently support the RT and the Advanced Interactive Executive, or AIX, the version of Unix that IBM developed for the RT. Sun, on the other hand, says more than 800 application packages from more than 400 vendors run on its work stations.

Colony says AIX, which he refers to as "IBM's oddball Unix," has thus far been a major hindrance to the success of the RT. Nevertheless, he adds, it plays an important part in IBM's plans for the machine, beyond whatever success it may have in the work-station market. He sees the RT as IBM's way to climb aboard the Unix bandwagon.

"In the first go-round of the RT, I believe IBM was really just testing the water," Colony says. "The major reason they decided to expand the system is that customers are demanding Unix." Colony adds that he believes AIX will eventually become the standard form of Unix "in all IBM environments in the future." –*Tobias Naegele*

TAB + WIRE BONDING = VLSI CONNECTIONS

CARLSBAD, CALIF.

Harried chip makers, looking for a better way to automate the interconnection of hundreds of leads in the newest very large-scale integrated circuits, may have a solution at hand. A new technique called single-point tape-automated bonding is getting a trial run at semiconductor plants, and packaging engineers say it shows considerable promise.

It combines the speed and precision of tape-automated bonding with wire bonding's ability to handle a wide variety of chip shapes, all in one piece of equipment, says the supplier, the Industrial Products Division of GMHE/Hughes Aircraft Co. Single-point TAB can connect 8 to 10 inner or outer leads per second, and it will get faster when improvements—mostly in software—are implemented.

It's that kind of production rate that makes the technique usable for TAB, a goal "that everybody wants," says consultant William I. Strauss of Forward Concepts Inc. in Tempe, Ariz. Some form of TAB is indispensable, he says; because the technique can handle mass bonding while maintaining separation of leads in dense chips, "it is the only way to get the [input/output] count up."

Moreover, the wire-bonding feature of the Hughes unit goes a long way toward correcting the biggest drawback of TAB: its inability to operate at peak speeds on anything but flat chip surfaces. Since the latest chips not only are larger and hold more leads but have a variety of surfaces, overcoming that limitation is a major advance.

FLEXIBILITY. Gary D. Smith, the product's marketing manager at Hughes, emphasizes that this "flexibility to meet this packaging barrier" is the prime attraction of the Hughes bonder. As it is, chip makers "lack development tools for this task, so there is no question about the need," he adds. Hughes has sold six of the initial development units for $110,000 each. These are installed at user sites, where engineers are evaluating them and feeding back comments and suggestions for improvements.

Among the operations trying out the Hughes bonder are Microelectronics & Computer Technology Corp., the research cooperative in Austin, Texas, and Honeywell Inc.'s Solid State Product Center in Colorado Springs, Colo. Although engineers at both places decline to discuss their work with the bonder, other sources confirm it is performing well, though not yet perfectly. One drawback is the familiar TAB limitation of less-than-ideal operation when leads are not laying flat on the package. Another is that alignment of the TAB overlay is still being done manually, which is difficult. A pattern-recognition feature will correct this, Hughes says.

The new bonder is built around the Hughes HMC-2460 automatic wire bonder. The Industrial Products Division, which has wire bonders for hybrid production gear installed at more than 600 sites worldwide, began adapting the machine for single-point bonding on tape in late 1985, after a sister Hughes division asked for packaging help with its Very High Speed Integrated Circuit Phase 1 program. "We've had the knowledge for years, but nobody was interested in it," Smith recalls.

The most difficult task was changing the operating software package, and it is still being rewritten. In addition, ultrasonic gear for TAB connections replaced the wire-bonding tooling, and a better staging area to precisely rotate and position the IC die was provided. A single-frame format, resembling a 35-mm slide, was fitted to the bonder, since the tape medium is different from the reel-to-reel format for ordinary TAB, which tends to bend leads on very dense chips, Smith says. 3M Corp., a major tape supplier, is interested in developing the new format as a product, he adds.

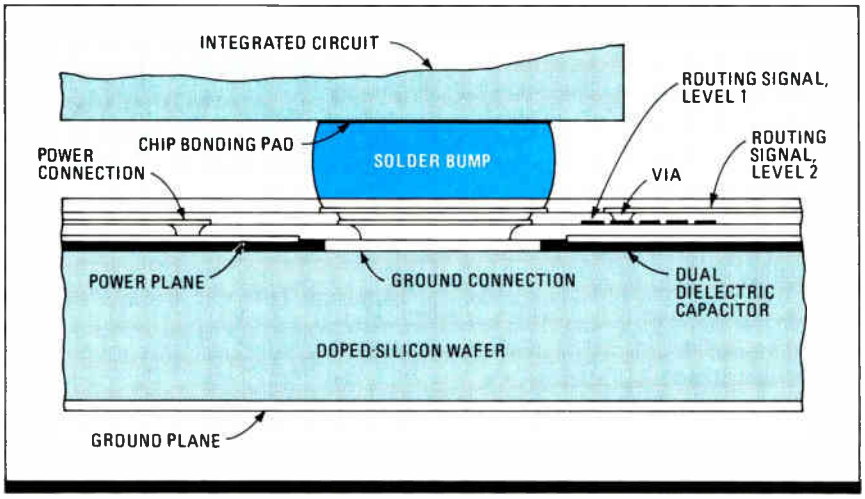
The various adaptations and additions gave Hughes a working single-point bonder last year, and potential users found out about it by word of mouth and from demonstrations at small packaging shows. But Hughes doesn't consider the bonder a finished product yet, Smith says, and it expects to incorporate many more changes as users come up with suggestions. *–Larry Waller*

PACKAGING THAT MEETS THE CHALLENGES OF VLSI

Making very large-scale integrated circuits is one thing, and packaging them is another. As VLSI spreads into systems, package designers face daunting demands: packages must be able to handle up to 500 inputs and outputs, operation at up to 100 MHz, propagation of pulses with rise times of less than 2 ns, and cooling at thermal loads greater than 1 W/cm². Now three Bell Labs engineers have come up with an approach that can stretch to handle those requirements.

Working at AT&T Bell Laboratories in Murray Hill, N.J., Hyman J. Levenstein, Charles J. Bartlett, and Walter J. Bertram are using solder-bumped chips mounted to a multilayered silicon substrate. Describing their work in a paper given at last week's International Solid State Circuits Conference in New York, they say that their new technology, which is a hybrid approach to wafer-scale integration, has the potential to handle more than 200 I/Os, operate at up to 100 MHz, propagate pulses with rise times under 2 ns, and cool at better than 1 W/cm².

Starting with a substrate that is a silicon wafer, an integral bypass capacitor with a value of 25 nF/cm² is fabricated on the wafer surface with a dual dielectric process. Copper power and ground planes are then sputtered to



BUMPING ALONG. Bell Labs' scheme depends on solder-bumped chips on a silicon substrate.

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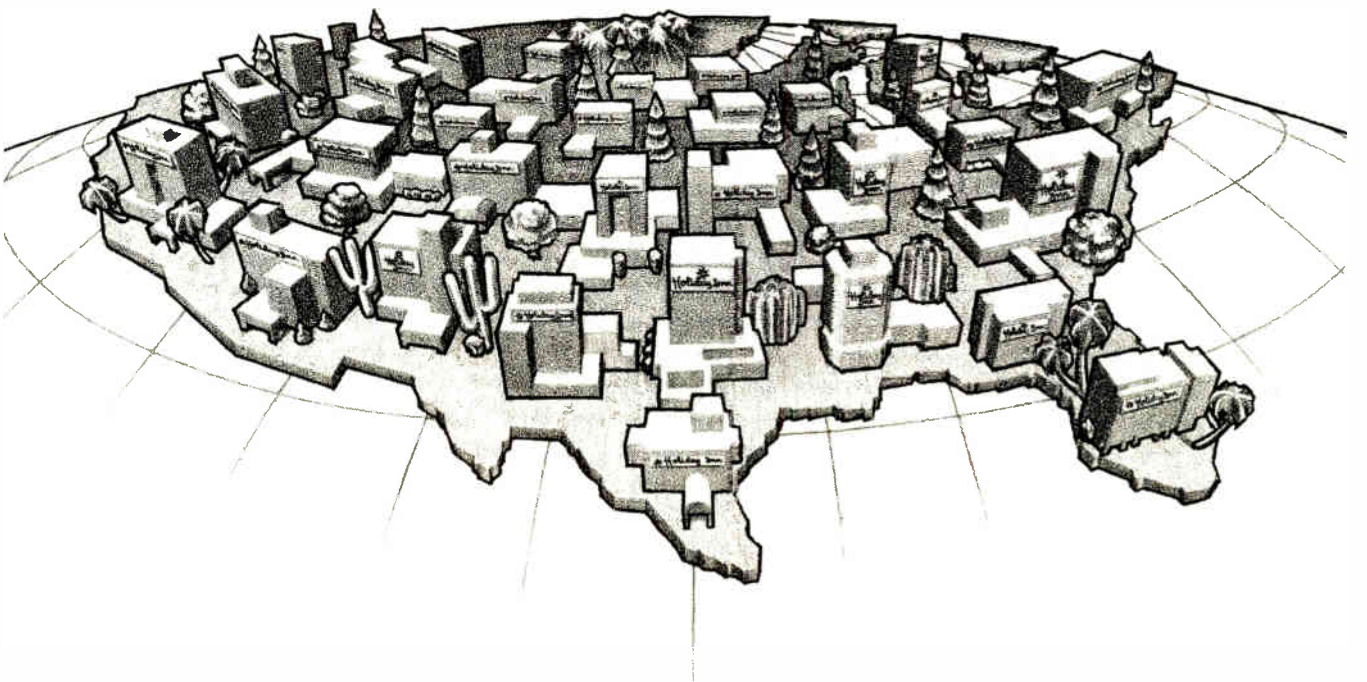

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both sides of the substrate.

Next, two signal layers are positioned above the power plane using a polyimide dielectric material. With 10-μm-thick polymer, the characteristic impedance of the minimum-width, first-level signal leads is 50 Ω, and the capacitance is 1 pF/cm. Copper metalization is used to achieve a resistance of 10 Ω/cm for the minimum-width (10 μm) second-level signal leads, which are 2 μm thick. A second 5-μm-thick polyimide layer separates the signal layers. Vias are etched into the polyimide and filled with nickel.

Solder-bumped chips are then reflowed to the substrate. Soldering was selected over wire bonding because it is repairable, provides a low inductance connection between chip and substrate, and enables chip I/O pads to be positioned directly over the corresponding pads on the substrate.

PROTOTYPE. A prototype has been built with three chips from the Western Electric 32100 32-bit microprocessor interconnected on a 1.3-by-3.0-cm substrate. The assembly is next to a metal heat sink using a compliant adhesive. Chip-to-heat-sink thermal resistance is 5°C/W.

That unit is mounted to a multilayer printed-circuit board that has 20 rows of four pins down each side on 100-mil centers. The silicon hybrid's I/O pads are wire-bonded to pads on the pc board. These pads are then fanned out to the pins, forming a split-grid grid-array package.

Significant improvements in system performance can be achieved with the package. For example, a general-purpose signal processor using the same basic chip set and packaged conventionally attained a system frequency of 30 MHz, whereas the multichip package allowed the same chips to operate at 100 MHz. System power dissipation was cut 30%, and board area was slashed by a factor of seven. *–Jerry Lyman*

COMPUTER-AIDED ENGINEERING

FACTORY CAE ENTERS THE FOURTH DIMENSION AT NEC

KAWASAKI, JAPAN

By adding the fourth dimension—time—to its computer-aided-engineering software package for designing automated assembly lines, NEC Corp. figures it will be able to cut design time by at least half.

The computer-controlled factory lines that NEC has in mind consist of multiple flexible-manufacturing-system cells, along with the materials-handling systems that connect them. CAE programs that speed floor layouts for factory cells are fairly common, but so far none has tackled the need to synchronize the movement of different parts, according to Tatsuo Ishiguro, general manager of the firm's C&C Laboratories in Kawasaki. So when the individual operations have been worked out by computer, the design usually needs to be checked out on paper to make sure there is no danger that swinging robot arms or parts moving down the line will collide. The first pass must be checked, too, for time-wasting gaps in the manufacturing process.

Software package cuts design time by at least half

CUT BY HALF. "We can cut back the three months or so it now takes to design a [factory-automation] system by at least half," says Ishiguro. With the design done, it takes an another three months or so to deliver, install, and test the production equipment, he adds.

Ishiguro's people managed to eliminate manual checks by adding a simulator to the usual two parts of a factory-automation software package—a floor-plan tool and a production-scheduling tool. Their simulator, which required 20,000 lines of code in "C" language, is experimental, but NEC executives say it could turn up in a commercial package in a year or two.

The simulator works with a CAE application system that is designed to be independent of individual machine-cell specifications as well as the individual application programs for them. In order to achieve that, the four-dimensional model of the line is constructed with three basic elements. Those elements consist of descriptions of how the motions of production machines and of manufactured parts should be made, of what motions should be synchronized, and of what conditions should be satisfied at the start and stop of motion.

The 4-D simulation provides a graphic representation of the assembly line for consecutive time slices. Motion description is given as data in three spreadsheets, one for each basic element. The simulator interprets the descriptions and generates the geometric information needed to display the line's operations in 3-D.

For their first go at the experimental system, Ishiguro's staff worked with NEC's 9801 personal computer—which can simulate about 50 factory operations per second—and a companion, 3-D display. However, the personal computer does not have the computing power to handle collision avoidance and checking for gaps, so for those tasks NEC uses a mainframe. *–Charles L. Cohen*

PRODUCTION

MOLECULAR-BEAM GaAs LEAVES THE LAB

PARIS

A seven-person French start-up is pushing molecular-beam-epitaxy production of advanced gallium arsenide out of the lab and into mass production. The company, Picogiga SA, is already shipping wafers to component makers in the U.S., Canada, and Europe.

Lihn T. Nuyen, company president and former chief of the Thomson CSF team that in 1981 came up with the high-electron-mobility transistor, estimates the worldwide market for wafers in military, telecommunications, supercomputer, and consumer-product applications to reach about $150 million by 1990. Picogiga's objective is to capture 10%; estimated first-year sales are $1.5 million. "There are about 60 gallium arsenide programs, and we have about 12 as customers," says Nuyen.

Picogiga opened a subsidiary last month in Oxnard, Calif., in an attempt to further penetrate the U.S. market, especially in the military area. "We are going in the same direction as the [Defense Department]—higher speed," says Nuyen. "If you can detect your signal even one second before your enemy, you have the chance to send up a lot of missiles."

Nuyen insists that his process involves no secrets—it was simply a question of "very, very hard work." He adds: "We have so far increased by a factor of three what could be done in the research state," which means 80 wafers a month. The throughput is expected to double each year, along with sales.

He calls the wafers he is producing "second-generation GaAs." That, he says, is to differentiate them from "the thick-layered ordinary GaAs wafers people are making today." Picogiga's wafers are a complex heterostructure of GaAs and gallium-aluminum-arsenide with very thin layers.

Nuyen proved the effectiveness of thin layers while working at Thomson-

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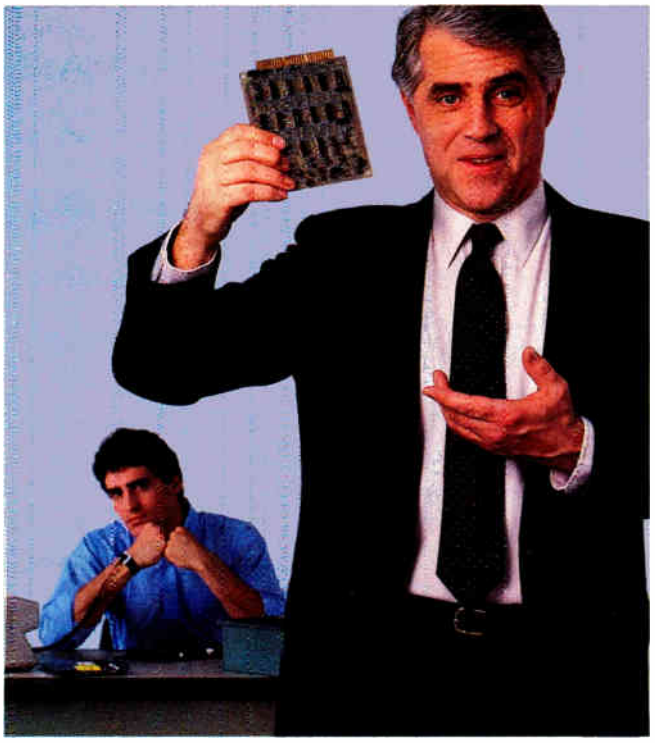

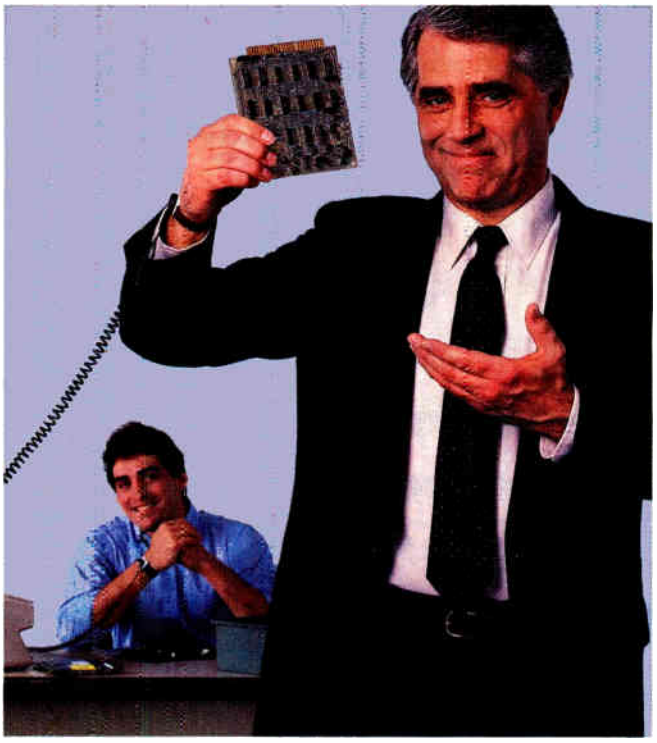

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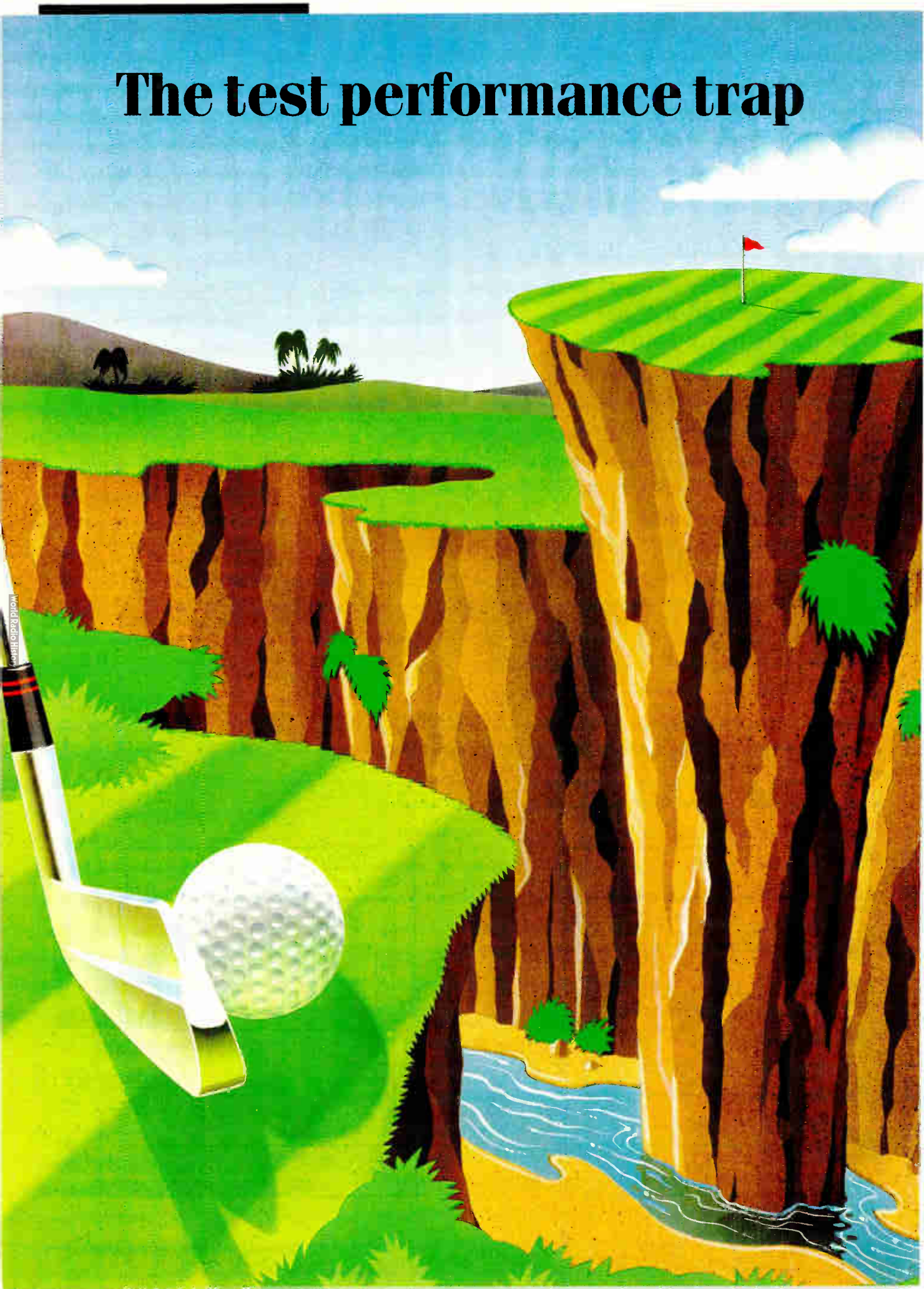
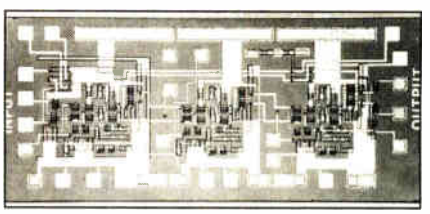


man communications-equipment maker. Its job is to boost weak variable signals from a system's preamplifier several hundred times to a large constant-output voltage swing. With European communications agencies considering links with rates of 2.4 to 2.8 Gb/s to replace the present 560 to 680 Mb/s, the amplifier should receive a warm welcome.

The amplifier's large input dynamic range of 52 dB produces a 400-mV peak-to-peak constant output voltage from a variable input voltage as low as 1 mV peak to peak. Driven by a single 5-V supply, the amplifier sports a maximum voltage gain of 54 dB.

CIRCUIT NEEDED. The device contains three amplifying cells, an emitter-follower input stage, and an output buffer—all dc-coupled and integrated on the chip. The dc coupling and high gain necessitate a circuit that automatically eliminates offset voltage. This circuit's capacitor is the only external element.

Performance was enhanced at every step. For example, at the maximum possible bit rate, the amplifier produces an optimum opening of the eye pattern, which is made up of a large number of superimposed signal trains. And for transistor dimensions, numerous network simulations were used to find the best possible compromise between the transistors' base-spreading resistance and their junction capacitance, a compromise that adapts transistor sizes to the amplifier's speed demands.



LIGHT CHIP. The high-gain circuit from Ruhr University has three amplifier cells.

Even the chip's elongated shape helps. It keeps the input and output well separated to eliminate the parasitic circuit interactions that may lead to unwanted oscillations. Also, the input stage is shielded by a grounded frame in the first metalization level. Each stage has separate internal-bias voltage generators and power-supply bonding pads.

The 4-Gb/s main amplifier is the latest device for future optical-fiber cable systems to come out of the university's Institute of Electronics. There have been, for example, a 3-Gb/s laser driver, a 6-Gb/s time-division multiplexer, and a 6-Gb/s signal-regenerating demultiplexer [*Electronics*, Oct. 16, 1986, p. 50]. These three devices, using the same 2-μm standard bipolar technology as the new device, have also established speed records, Rein says. —*John Gosch*

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We developed the 256K ROM, and within a year of its introduction, we were supplying over 50% of worldwide demand. In CMOS we created and are now producing in volume the 1MB and 2MB high-speed CMOS mask ROM.

EPROMs in NMOS and CMOS

Toshiba was first in the world to introduce the 256K CMOS EPROM. And we can meet all your EPROM needs today with high density products, including the 512K and 1MB EPROM, that can accommodate an entire utility program.

TOSHIBA IS MPU POWER

Toshiba offers a CMOS Z80® MPU and peripherals that are hardware and software compatible with the Z80 family, and they are second sourced.

In addition, we have high volume production now on CMOS and NMOS 8048 and 8049 products. We're also in volume production with the 8085 and peripherals. In fact, Toshiba has one of the world's most comprehensive lines of CMOS and NMOS MPUs.

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Toshiba has been manufacturing CMOS logic since the early 70's. We introduced the first high-speed series, and today are #2 worldwide in CMOS logic production.

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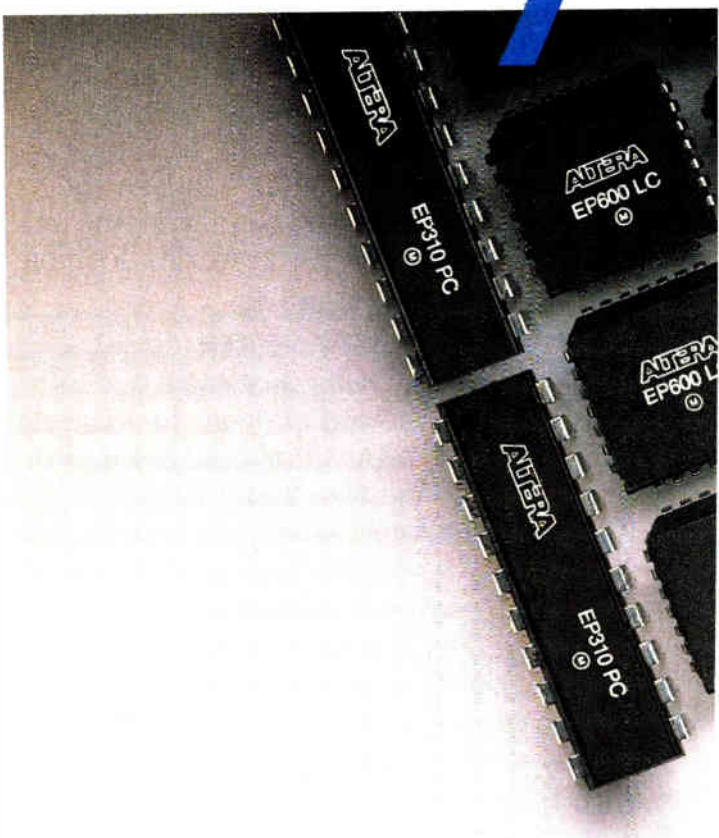

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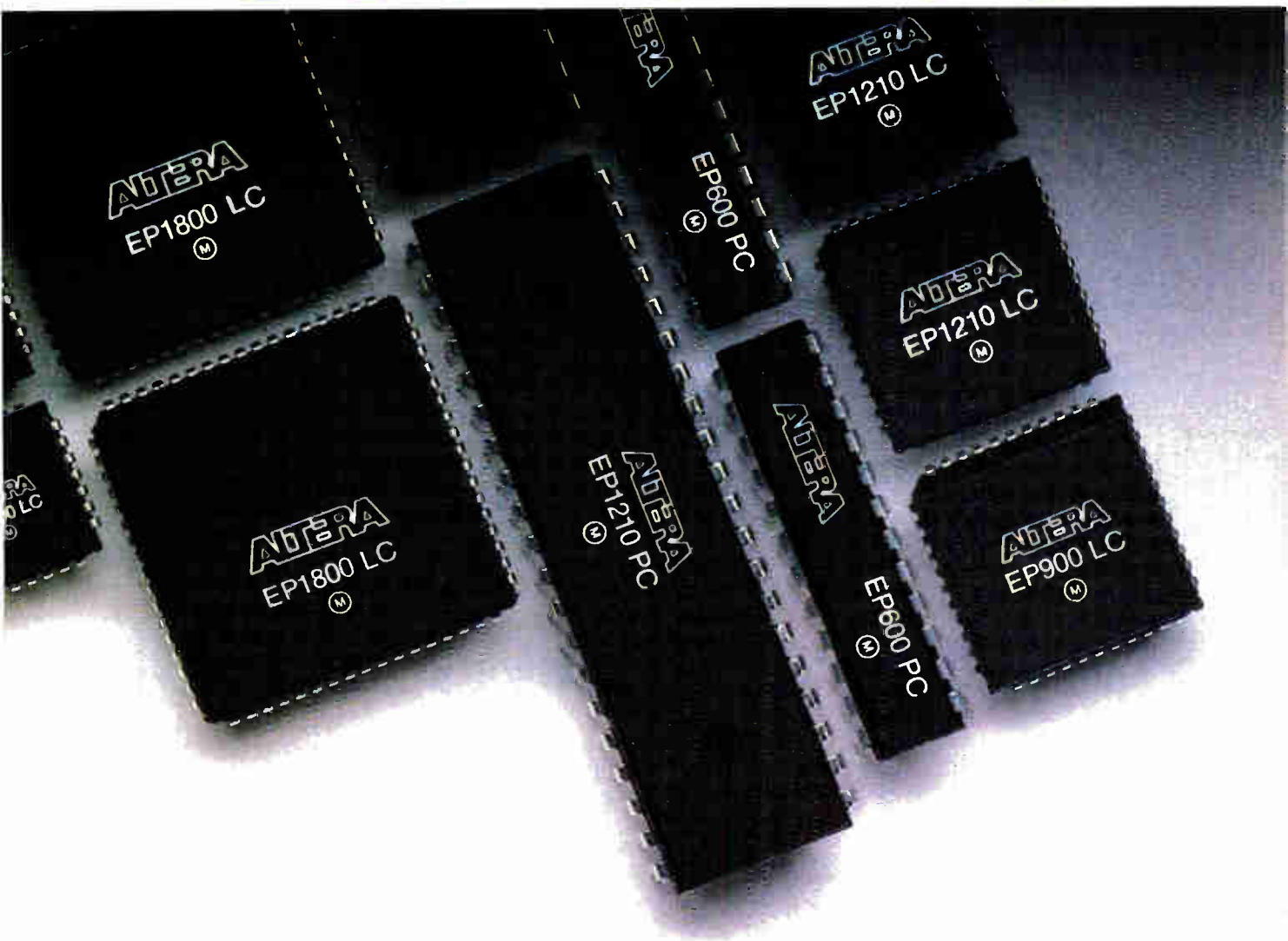

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INTERNATIONAL NEWSLETTER

INMARSAT PLANS EXPERIMENTAL AIRCRAFT-TO-SATELLITE COMMUNICATIONS

The International Marine Satellite Organization of London will use 9.6-kb voice-encoding equipment for its experimental aircraft-to-satellite international telephone service, scheduled to begin at the end of this year. The highly efficient voice encoding equipment, developed by Japan's Kokusai Denshin Denwa Co., enables users to transmit voice and high-speed data and image signals on a single 64-kb digital circuit. More than 10 voice channels can be transmitted on one 64-kb circuit using digital speech interpolation. KDD will ship seven sets of voice encoding/decoding equipment to Inmarsat by the end of May for ground stations and aircraft. The Tokyo equipment manufacturer also plans to start experimental aircraft-to-satellite international telephone service this fall, working with Japan Air Lines Co. and Japan's Ministry of Posts and Telecommunications. □

DIGITAL-SWITCH ORDER STRENGTHENS SIEMENS HOLD ON NO. 3 SPOT IN U. S.

A $12 million order for ISDN-compatible digital-exchange equipment is helping Siemens AG solidify its position as the No. 3 supplier of digital-exchange equipment in the U. S. The order—placed by Chicago's Ameritech, one of the seven regional Bell operating companies—boosts the total number of subscriber lines in the U. S. serviced by the Munich company's EWSD electronic digital dialing switches to about 30,000. That number is small when compared with the total U. S. market but is proof to Siemens that it has been accepted as the No. 3 supplier in the U. S., behind AT&T Co. and Canada's Northern Telecom, and ahead of the several Japanese, Swedish, French, and British suppliers vying for a foothold in the multibillion-dollar U. S. switch market. Siemens and others began competing in the market, long dominated by AT&T, after the breakup of the Bell System in 1984. In addition to Ameritech, Siemens has delivered equipment to Nynex, Southern Bell, Bell Atlantic, and Southwestern Bell. □

WEST GERMAN RESEARCHERS CLAIM RECORD IN MAGNETIC FLUX DENSITY

As superconductivity research continues to heat up worldwide, the Nuclear Research Center is claiming a world record in magnetic flux density. Researchers at the Karlsruhe, West Germany, center's Institute for Technical Physics have achieved a flux density of 19.3 tesla—roughly 350,000 times the density of the Earth's magnetic field—with a superconducting magnet kept in continuous operation. Such strong superconductivity-induced magnetic fields are used, for example, in high-resolution magnetic spectrometers. □

ES2 SIGNS GOTHIC CRELLON TO HELP IT REACH LOW-VOLUME ASICs USERS

European Silicon Structures has signed Gothic Crellon Ltd., of Wokingham, UK, to spearhead its effort to bring SystemCell, a 2-μm CMOS process for application-specific integrated circuits, to the low-volume market. Until now SystemCell has been available only to high-volume customers, but ES2, of Germering, West Germany, has joined with Philips International's London subsidiary, Mullard Ltd., and Texas Instruments Ltd. of Bedford, UK, in an effort to make the system a de facto European standard. Gothic Crellon will help ES2 to target customers, develop circuit designs, and manufacture prototypes. By sharing with ES2, [*Electronics,* Nov. 27, 1986, p. 48], Mullard and TI make the SystemCell library available to the low-volume users—those with the most to gain from ASIC technology. ES2 uses electron-beam direct-write techniques and has already implemented SystemCell at its London, Munich, and Paris design centers. Mullard, TI, and ES2 are now developing a compatible SystemCell library in 1-μm CMOS. □

INTERNATIONAL NEWSLETTER

PHILIPS AND TAIWANESE JOIN TO START INDEPENDENT VLSI CHIP FAB

Taiwan is moving into the chip-making business. The island nation's government has joined Philips International NV of the Netherlands and a group of private domestic companies to establish the Taiwan Semiconductor Manufacturing Corp., a fabrication facility for very large-scale integrated circuits. The $145 million venture, which will be 48% owned by the government, 27% by Philips, and 25% by the others, will concentrate on manufacturing for other companies. "This is a unique concept and one that I think will be very effective," says president James E. Dykes, who was vice president and general manager of General Electric Co.'s Semiconductor Business Division until that group was made part of the GE/RCA Solid State Division after GE merged with RCA Corp. "Semiconductor companies can utilize our resources without fear that we will take their technology and run to the market." Morris Chang, 55, who has been president and chief operating officer of General Instrument Corp. and a senior vice president at Texas Instruments Inc., will chair the company's board of directors. Taiwan Semiconductor expects its Chutung facility to be capable of producing 10,000 6-in. wafers per month by the end of this year. A second plant of equal size is planned for 1989. □

MATSUSHITA AGREES TO PAY IBM FOR INFRINGING ON BIOS COPYRIGHTS

In the latest trade difference between U. S. and Japanese electronics companies, Matsushita Industrial Co. reportedly will pay IBM Corp. about $2 million in damages for infringing on IBM's BIOS copyrights with its FX-800 Business Partner personal computers imported into the U. S. and Europe. Matsushita has already sold about 2,000 units, but has agreed to ship another 2,000 units now sitting in warehouses back to Japan. The agreement will have no effect on continued sales of Matsushita's FX-600 Business Partner, its Executive Partner, and its Senior Partner PCs in overseas markets. □

EAST GERMANY PREDICTS RAPID RISE IN PERSONAL-COMPUTER PRODUCTION

Demand for microcomputers, although tapering off in the West, is booming in East Germany. Sketchy government reports, which do not include exact figures, predict a "double-digit" rise in the production of 8- and 16-bit personal computers in 1987. Last year East German manufacturers produced 21,000 personal computers, bringing the installed base to 35,000. By 1990, East Germany, whose population of 17 million is roughly equal to that of Kentucky, hopes to have 160,000 to 170,000 machines in use. The bulk of the production is by Robotron, the Dresden maker of data-processing equipment employing nearly 70,000 people in 20 plants in East Germany. □

IBM BEGINS TO IMPORT ITS JAPANESE-BUILT 5550 KANJI PCs TO U. S.

IBM Corp. has long taken technology developed for the U. S. market to Japan, and now IBM Japan Ltd. is starting to market its popular 5550 multistation Personal Computer in the U. S. The high-performance 16-bit MS-DOS system is designed to process Kanji and other characters used for writing Japanese, Chinese, and Korean. It will be sold mainly to Japanese companies operating in the U. S. by Management Information Science International of Torrance, Calif. Demand is growing in the U. S. for Kanji PCs because so many Japanese manufacturers and financial companies have recently started subsidiaries there, says Nippon Office Systems Ltd., a sales agency for IBM in Japan. Meanwhile, there is a growing market in Japan for IBM PC ATs for engineers' work stations to operate the latest U. S. design software. Industry sources predict that IBM Japan will enhance the 5550 to allow it to use PC AT software. □

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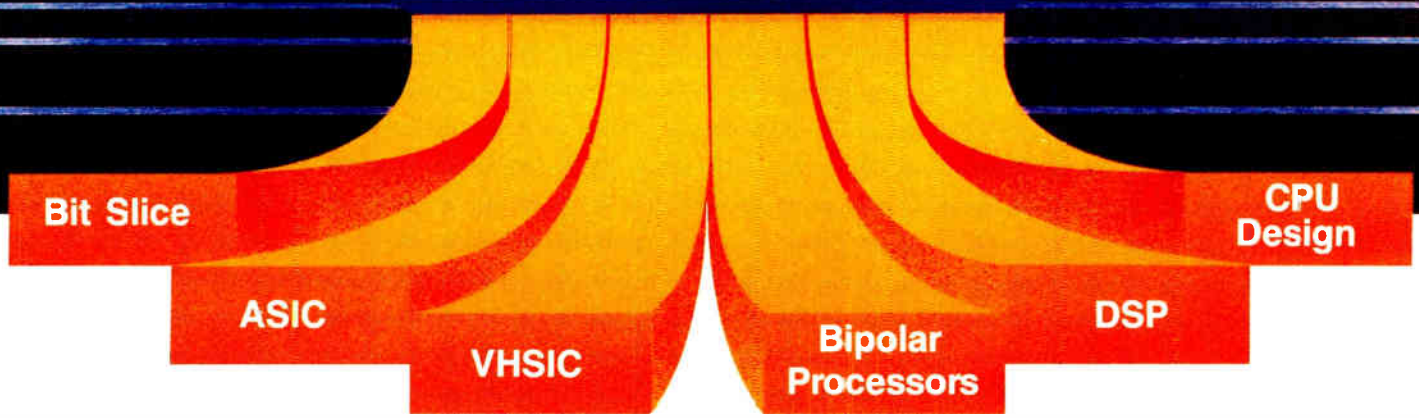

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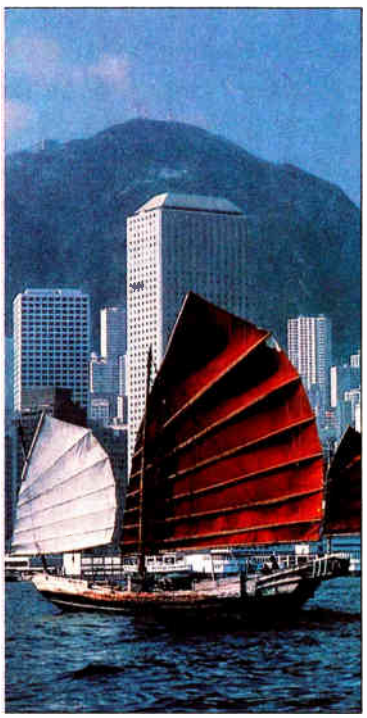

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NORTHWEST

INTERNATIONAL WEEK

1987 LOOKS STRONG FOR UK BOOK TO BILL

The Electronics Component Industry Federation, whose data accounts for 70% of UK semiconductor sales, predicts that the UK book-to-bill ratio will stay above parity for at least the next six months. This follows a provisional January figure of 1.1, the second month in a row the ratio has been above parity [*Electronics*, Jan. 22, 1987, p. 48A]. The ECIF bases its prediction on two factors: the first six months of a year have traditionally higher book-to-bill ratios and the slight but noticeable improvement in semiconductor sales.

FRENCH TO DESIGN EUREKA NETWORK

Groupe Bull and the computer engineering house Copernique of Paris are forming Architecture Multi-media Européenne, or Archimede, to carry out the Multi-media Open Standard European System, or Moses, project of the Eureka research program. Moses, an $82.5 million project, will provide a network architecture for processing and managing texts, computer data, images, graphics, and voice. The Moses project is expected to yield a pilot system by 1988, and the system should be available by 1990. Archimede, of La Celle Saint-Cloud, is equally owned by Groupe Bull and Copernique.

PHILIPS WINS ISDN CONTRACT IN CHINA

Philips International NV of the Netherlands was awarded a $700,000 contract to set up the first phase of a private integrated services digital network in China. The project will link all government research organizations in China's main cities. The first of three phases, expected to be completed in 1988, is installation of eight Philips Sopho-S systems, a fully ISDN-compatible PABX system, and 2,800 lines. Eight more systems are scheduled to be installed in the $650,000 second phase, expected to begin in 1988. Sopho-S is a private exchange being used for the government contract.

NIHON DEC MARKETS NTT SOFTWARE TOOL

Add Nihon Digital Equipment Corp. of Tokyo to the list of companies that will market NTT's expert-systems development tool [*Electronics*, Feb. 19, 1987, p. 45] beginning this month for 6 million yen (about $39,000) each for its Microvax II and 10 million yen (about $65,000) each for its VAX8000 group and VAX-11 series. A spokesman for Nihon DEC says that the company will not develop an English version and will not sell the system abroad. Nihon DEC hopes to sell 100 units this year.

PHILIPS PUSHES INTO UNIX MARKET

Philips Telecommunication and Data System, a division of the Dutch electronics giant, has launched a new stand-alone microprocessor-based work-station line. The P9000 heralds the company's move into the Unix market. It is using Philips microprocessors that the company makes under second-source agreements with U.S. companies. The equipment offers advanced open-ended architecture for connection to Philips and other suppliers' office equipment. Integrating data processing, office communications and telecommunications facilities, the P9000 allows users to work on different applications at a work station.

DATABASIX, HP SIGN MINICOMPUTER PACT

Databasix Ltd. of Newbury, UK, and Hewlett-Packard Ltd. of Bracknell have signed a cooperative marketing agreement for plant and quality monitoring, logging, display, and process control based on the HP1000 minicomputers. Databasix will also become the first Hewlett-Packard OEM in the UK to distribute CIM-Link, a data-acquisition and management-information system for personal computers. Databasix specializes in data acquisition, transformation, and retrieval systems.

2 FIRMS TO MINE FINE-GRADE SILICA

Sumitomo Corp. of Osaka and Kyoritsu Ceramic Materials Co. of Nagoya are establishing K. & S. Minerals Pty in Australia to mine and refine fine-grade silica. The Sydney company will build a refinery in Tasmania and will start mining the silica in June in cooperation with Monier Ltd. of Sydney, a large building materials company. The company expects to produce 20,000 to 25,000 tons for sales of 500 million to 600 million yen ($3.26 million to $3.91 million) in the first year.

SALES SOAR FOR SIEMENS SWITCH

Siemens AG will install its EWSD Digital Telephone Exchange System this year in three more South American countries—Colombia, Uruguay, and Venezuela. The system will then operate in seven of South America's 11 countries. So far, the Munich company has signed up 52 telephone-operating companies and postal-communications agencies worldwide for a total of 6.8 million lines.

DENATIONALIZATION IN CANADA TELECOM

In the latest in a series of denationalizations of Canadian industries, Memotec Data Inc. will take over Teleglobe Canada, the government company that provides all overseas telecommunications services, at the end of March. The $488 million deal is being financed by major shareholders in Memotec, including pension funds and financial institutions. Memotec, an Ottawa telecommunications company, earned $3.3 million during the first nine months of 1986. Teleglobe earned $45.7 million. And in another development, Teleglobe has awarded a contract worth a total of $3.5 million to Telecast Canada and TIW Systems Inc. of Ontario for a satellite earth station on the grounds of the 1988 Winter Olympics in Calgary.

CMOS ASIC SALES TO ZOOM IN EUROPE

The total European CMOS ASIC market will increase from $210 million in 1985 to about $675 million in 1988 and will top $1.44 billion by 1991. Philips International NV, Texas Instruments France, and European Silicon Structures attribute this growth to the demand for ASICs in European systems engineering houses—in machinery, communications, machine tools, and processing equipment for industries such as chemicals and steel. TI and Philips have signed on ES2 as a partner to provide customers with prototyping services for their jointly developed range of CMOS standard-cell ASICs.

AMSTRAD PROFITS INCREASE SHARPLY

Amstrad plc, a leading personal-computer maker based in London, recorded a larger profit in the last six months of last year than it did in all of 1985. Profit from July to December 1986 was nearly $75 million, compared with about $28 million for the same period in 1985 and about $70 million from January to June 1986. Chairman Alan Sugar attributes the increase partly to last year's purchase of Sir Clive Sinclair's computer company, Sinclair Research Ltd.

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INTERNATIONAL PRODUCTS

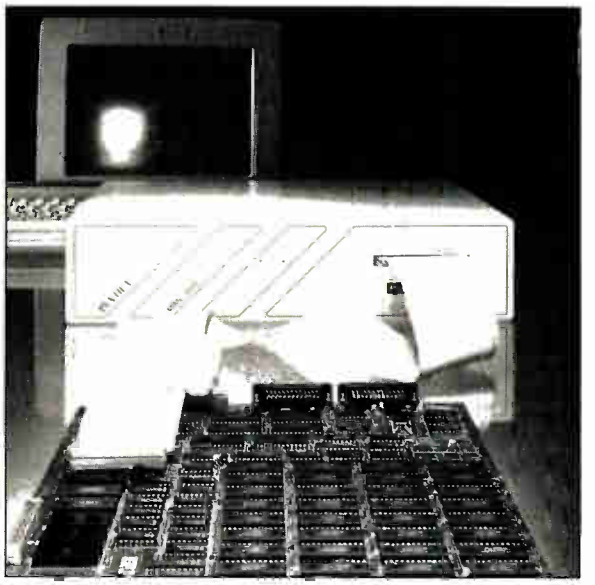
MORE RAM IN 8-BIT EMULATORS SPEEDS PROGRAM DEVELOPMENT

256-K OF RAM ELIMINATES NEED FOR EXTERNAL PROM

The Mime 600 series of in-circuit 8-bit emulators from Pentica Systems Ltd. now offers 256-K of random-access memory, a jump up from the 64-K in earlier versions. By increasing the amount of RAM, Pentica enhanced the emulators' functional capabilities for developing applications for target microprocessors.

The series includes emulators for many popular 8-bit microprocessors, including Motorola Inc.'s 6800 family, Zilog Inc.'s Z-80 family, and Intel Corp.'s 8085. It can be interfaced with most host computers.

Typically, 8-bit emulators must store programs exceeding 64-K in external programmable ROM. The Mime 600 emulators eliminate the need to alter the PROM to account for changes in the development program. Problems can be fixed on-line, but reductions in development time are difficult to quantify, says Mike Ellis, company marketing director.



VERSATILE. Mime 600 in-circuit emulators handle full-speed, real-time emulation for many 8-bit microprocessors.

The additional memory capacity also means more memory breakpoints are available for logic analysis. "These can be used, for example, as triggers to provide a pulse to an oscilloscope," says Ellis. The emulators are as sophisticated as any available, he claims.

TRACE MEMORY. For logic analysis, the emulators have a 48-bit-by-8-K real-time trace memory that can be reconfigured as 96 bits by 4-K. In this configuration, 48 bits by 4-K can be assigned for time stamping. The system can trace between two trigger points, or on selected cycles, such as the input/output cycles.

To ease integration into existing engineering computing systems, Pentica designed all Mime emulators to interface any host computer with an RS-232-C port, including IBM Corp.'s Personal Computer AT and Digital Equipment Corp.'s VAX machines.

In addition to 256-K of RAM, the emulators feature three programmable pulse-rate generators, a digital voltmeter input, battery-powered backup memory, symbolic assembly/disassembly, full-speed emulation, and a large nonvolatile symbol-table memory.

Pentica has also introduced an optional software package called Microlex-600 that offers a range of assemblers and C-language compilers to run with the emulators.

The Professional Cross Assembler package includes an assembler, a common linker, and a library manager. Users choose the software assembler appropriate to the target microprocessor. Pentica's use of a common object code, however, means the same linker and library manager are used for all the assemblers.

The library manager offers separate code and data facilities. Users can create and manipulate libraries of relocatable code and can generate Motorola S and Intel Corp. hex object-file data records. Symbol-table information can be produced in a variety of formats for downloading to the emulators.

Pentica has targeted European sales first but expects to enter the U. S. market later this year, says Ellis. Prices in the UK range from £4,300 to £5,300 for the emulators and from £295 to £825 for the software. *–Steve Rogerson*

Pentica Systems Ltd., Station Industrial Estate, Oxford Rd., Wokingham, Berkshire RG11 2YQ, UK.
Phone 44-734-792101 [Circle 500]

GRAPHICS CHIP RUNS FOUR DISPLAY TYPES

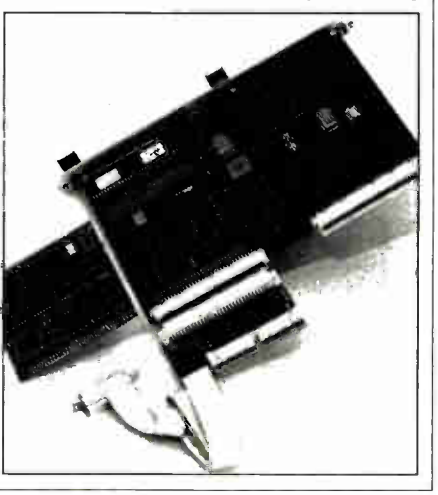
To help designers add advanced graphics to portable and desktop computers, Nippon Gakki Co.'s single-chip controller handles four types of displays.

The Panel and CRT Display Controller works with thin liquid-crystal, electroluminescent, and plasma displays in addition to conventional red-blue-green cathode-ray tubes.

The CMOS chip controls the color intensity of each pixel and provides 640-by-400-pixel resolution. Ideograms can be displayed in three different dot-character format sizes: 16 by 16, 24 by 24, and 32 by 32.

It comes in 84-pin plastic-leaded chip carriers and 100-pin flat packs. Samples, priced at 6,400 yen, are available now. Volume shipments will begin at the end of March, with delivery in eight weeks.

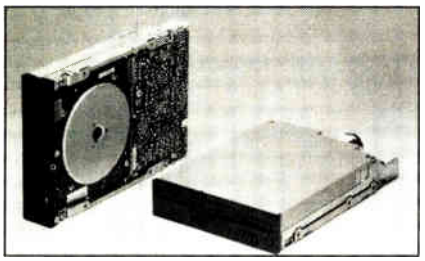
Nippon Gakki Co., Sales Engineering Dept., Semiconductor Division, Matsunokijima 203, Tyookamura, Iwata-gun, Shizuoka, Japan.
Phone 81-53962-3125 [Circle 701]



2 MEGABYTES FIT ON 3.5-in. DRIVE

New and existing technologies provide a 3½-in. floppy-disk drive with a 2-megabyte capacity. Y-E Data Inc.'s YD-701 uses a new, high-performance read circuit and an existing tunnel-erase ferrite head.

The drive is fully read/write-compatible with 2- and 1.6-megabyte media formats when using high-density media, and with the 1-megabyte format when using normal-density media.



The YD-701's anti-noise construction is dustproof and shock- and vibration-resistant. Samples, priced at 35,000 yen, will be available in March, with volume shipments to follow in April.

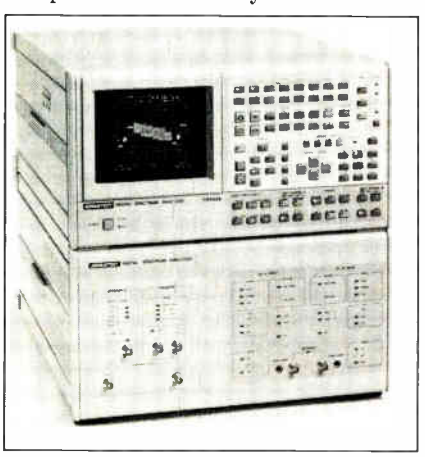
Y-E Data Inc., Sunshine 60, P. O. Box 1171, 3-1-1 Higashi-Ikebukuro, Toshima-ku, Tokyo 170, Japan.
Phone 81-3-989-8001 [Circle 702]

ANALYZER OFFERS 10-BIT RESOLUTION

Avantest Corp.'s digital spectrum analyzer can handle 10-MHz signals with 10-bit resolution when used as a fast-Fourier-transform analyzer.

The TR9408 also offers a 25.6-MHz sampling rate, color signal displays, a 512-K memory, and a wide range of trigger functions. With an optional signal generator, the analyzer can perform spectrum and time-domain analysis of video signals, including frequency-response testing of video tape and digital image-processing applications.

The one-channel TR9408A and the two-channel TR9408B will be available in April for 6.5 million yen.



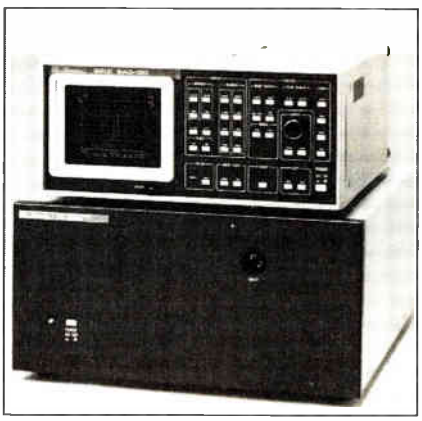
Advantest Corp., Foreign Trade Sales Section, 2-4-1 Nishi Shinjuku, Shinjuku-ku, Tokyo 163, Japan.
Phone 81-3-342-7500 [Circle 703]

OPTICAL ANALYZER ACCURATE TO 1 nm

Spectral characteristics of light sources forming wavelengths that range from 0.5 to 1.7 μm can be measured to within 1 nm with the HK-5400 Spectrum Analyzer from Shimadzu Corp.

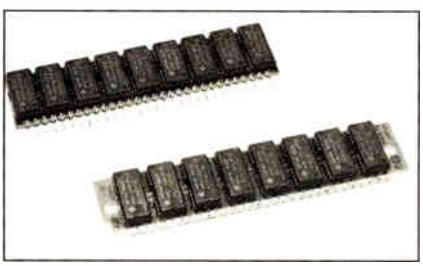
A built-in mercury-vapor light source automatically calibrates wavelengths, providing measurements with a sensitivity of -70 dBm over the entire 1.2-μm range. Spectrograms are displayed on a 7-in. screen, but the analyzer also has a built-in thermal printer. The HK-5400 is priced at 4.5 million yen. Delivery is 15 weeks after receipt of order.

Shimadzu Corp., Opto-Electronics Dept., Shinjuku-Mitsui Bldg., 2-1-1 Nishi Shinjuku, Shinjuku-ku, Tokyo 163, Japan.
Phone: 81-3-346-5760 [Circle 704]



DRAM MODULES HIKE DENSITY

Two dynamic RAM modules from Hitachi Ltd. increase the packing density of dual-in-line packages without requiring special surface-mounting equipment.



The HB56A18A and B modules are built with eight 1-Mb DRAMS in a J-bend package; their memory is organized as 1 megaword by 8 bits. The HB56A19A and B modules have nine 1-Mb DRAMs and a 1-megaword by 9-bit organization.

The leaded versions—HB56A18A and HB56A19A—offer a packing density as much as 3.7 times that of a DIP-style 1-Mb DRAM having the same functions. The leadless versions, designated by the letter B, are 3.2 times as dense as their DIP counterparts.

Samples are available now, at 39,000 yen for the HB56A18A/B and 42,000 yen for the HB56A19A/B. Production prices for 1,000-piece lots will be 32,000 yen and 35,000 yen, respectively.

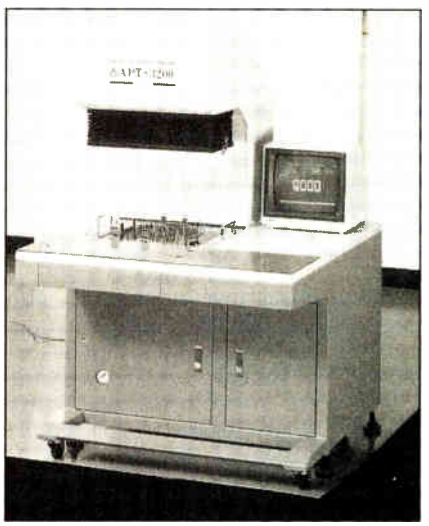
Hitachi Ltd., Semiconductor Division, New Marunouchi Bldg., 1-5-1 Marunouchi, Tokyo 100, Japan.
Phone 81-3-212-1111 [Circle 705]

IN-CIRCUIT TESTER CHECKS 512 PINS

Takaya Inc.'s in-circuit tester for printed-circuit boards performs short-circuit and open-circuit tests on 512 pins in as little as 2 seconds. The APT-3200 also performs on-board component testing at a rate of 10 ms per step for as many as 3,700 steps.

A CRT display showing the location and type of each defect makes the APT-3200 suitable for users who have little technical background. Software can automatically set guarding points, optimum measuring time, measuring mode, allowance, and discharge time.

Prices for the APT-3200 standard press version range from 7.2 million yen to 9.6 million yen, depending on options. Delivery is within two months of receipt of order.



Takaya Inc., 661-1 Ibara-Cho, Ibara-City, Okayama 715, Japan.
Phone: 81-08-666-2-1870 [Circle 706]

1-Mb SRAM MODULE BUFFERS INPUTS

The 1-Mb static RAM module from Hybrid Memory Products Ltd. features buffered inputs that make it appear as a single CMOS load, even though it is composed of four memory devices. It is available with access times of 120 or 150 ns.

The HMS41664 module combines four

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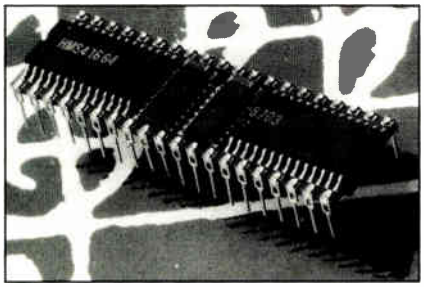


32-K-by-8 small-outline devices, plus decoders and decoupling capacitors. The 1 Mb of memory is configured as 65,536 by 16 bits. The HMS41664 consumes 150 mW at 1 MHz. Available now, the 150-ns version costs £60 each, and the 120-ns version costs £65 each, both in 100-unit purchases.

Hybrid Memory Products Ltd., Elm Rd., West Chirton Industrial Estate, North Shields, Tyne and Wear, NE29 8SE, UK.
Phone 44-091-258-0690 [Circle 707]

32-BIT SUPERMINI FITS ON ONE BOARD

A new CPU chip set on which input/output functions are independently handled by their own controllers is at the heart of the ND-5000 series of 32-bit, single-board superminis. They double the performance of the company's previous model.

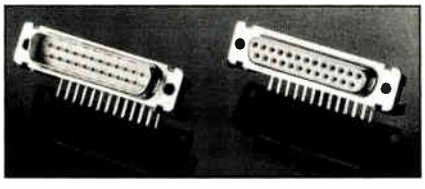
The series includes two single-processor machines. In Whetstone benchmarking, the ND-5700 is rated at 3.5 million operations/s and the ND-5800 6.5 mips. The ND-5700 costs £150,000 and the ND-5700 sells for £260,000. The ND-5900 Models 2, 3, and 4 are double-, triple-, and quadruple-processor versions of the ND-5800. They're priced at £380,000, £480,000, and £615,000, respectively. All are available now.

Norsk Data Ltd., Olaf Helsets VEI5, P. O. Box 25, Bogerud N0621, Oslo 6, Norway.
Binns Cornwall & Partners Ltd., 36 St. Andrews Hill, London EC4V5DE, UK.
Phone 44-148-91441 [Circle 708]

FILTER CONNECTOR SLASHES COST

The Silent D filter connector from ITT Cannon (UK) Ltd. attenuates incoming radio-frequency noise arising from connections between computers and peripherals. It is designed to meet radio-frequency-leakage regulatory requirements recently enacted in the UK.

In 90% of all applications, the company says, 10 or 15 dB of attenuation is sufficient to meet those regulatory requirements. However, most filters are now designed to achieve 40 dB or more attenuation, and building in the superfluous capability drives up their cost.



Silent D is available in plug-and-socket 9-, 15-, and 25-way right-angle printed-circuit-board versions. The 25-way connector costs £4.31 in purchases of 1,000 units.

ITT Cannon (UK) Ltd., Jays Close, Viables Industrial Estate, Basingstroke RG22 4BW, UK.
Phone 44-0256-23356 [Circle 709]

SCSI ADAPTER SPEEDS DATA-TRANSFER RATES

A Small-Computer-Systems-Interface adapter from Dean Microsystems Ltd. increases data-transfer speeds between VMEbus and SCSI buses in host computer systems. Data moves to and from the VMEbus at more than 2.2 megabytes/s; it moves to and from the SCSI bus at more than 1.4 megabytes/s.

The PT-VME400 adapter owes its speed to a Motorola Inc. 68010 microprocessor, a direct memory-access controller, and 512-K of memory. The 68010 supervises all SCSI-bus activity; the host computer's CPU communicates with the adapter via high-level macro commands for lower VMEbus overhead. The DMA controller moves data from the SCSI bus to local on-board memory, or vice versa. Available now, the adapter costs £1,676.

Dean Microsystems Ltd., 7 Horseshoe Park, Pangbourne, Berkshire RG8 7J2, UK.
Phone 44-07357-5155 [Circle 710]

DESKTOP MACHINE RUNS TEST PROGRAMS

The LTS-2020TDS personal computer-based work station from Analog Devices Ltd. enables users to move programming of the company's LTS-2020 components tester from the production floor to the test engineer's desk.

The computer is programmable in both the BASIC language and a fill-in-the-blanks system developed by the company. Any test program previously written for the LTS-2020 can be loaded on the work station for debugging or enhancement.

The LTS-2020TDS offers 512-K bytes of system memory, two floppy disk drives and two RS-232-C serial ports. It can communcate with the components test system over Analog Devices' LTSNetwork.

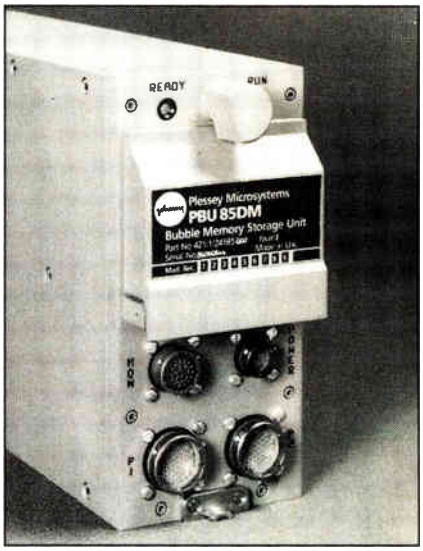
Available now, the LTS-2020TDS costs £6,248. Delivery takes approximately eight weeks.

Analog Devices Ltd., Admirals Quarters, Portsmouth Road, Thames Ditton, Surrey, KT7 OXA, UK.
Phone 44-398-9636 [Circle 711]

BUBBLE MEMORY BUILT TO TAKE A BEATING

Plessey Microsystems Ltd.'s new bubble memory is designed for environments where vibration, shock, and ambient temperature conditions limit the reliability of mass-storage devices that rely on mechanical drive mechanisms.

The PBU 85D provides up to 2 megabytes of storage in bubble memory car-



tridges. Average access time is 10 ms. Memory-block sizes are software-programmable from 256 to 4,096 bytes. The cartridges measure 4.5 by 2.7 by 0.9 in. and are available in storage capacities of 1 megabyte or 512-K bytes.

The unit has a standard RS-232-C interface. Data-transmission rates can be programmed at any value between 75 baud and 76.8-K baud. Operating temperature range is -55°C to 80°C. Available now, the device costs from £3,000 to £10,000, depending on optimal temperature range.

Plessey Microsystems, Water Lane, Towcester, Northants NN12 7JN, UK.
Phone 44-327-50312 [Circle 712]

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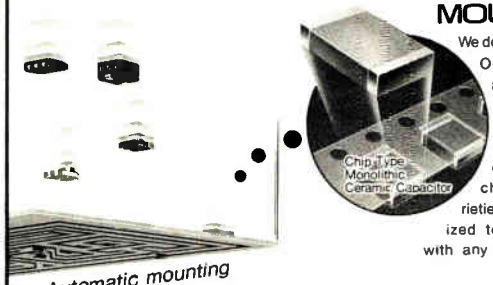
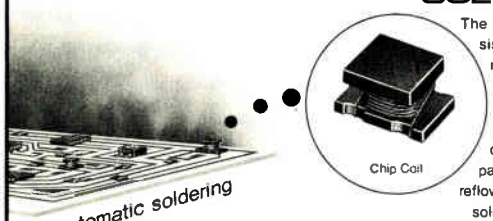


▲Automatic mounting

SOLDERING

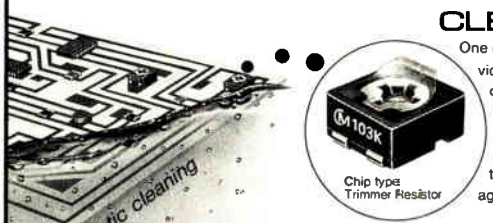
The special, heat-resistant designs of most of our chip types ensure that you receive chips with excellent solderability and compatibility with flow, reflow and vapor phase soldering operations.



▲Automatic soldering

CLEANING

One more way we provide reliability is by completely sealing most of our chips to prevent damage from detergents and from agitation during the cleaning process.



▲Automatic cleaning

CHIP COMPONENTS

For further information, contact

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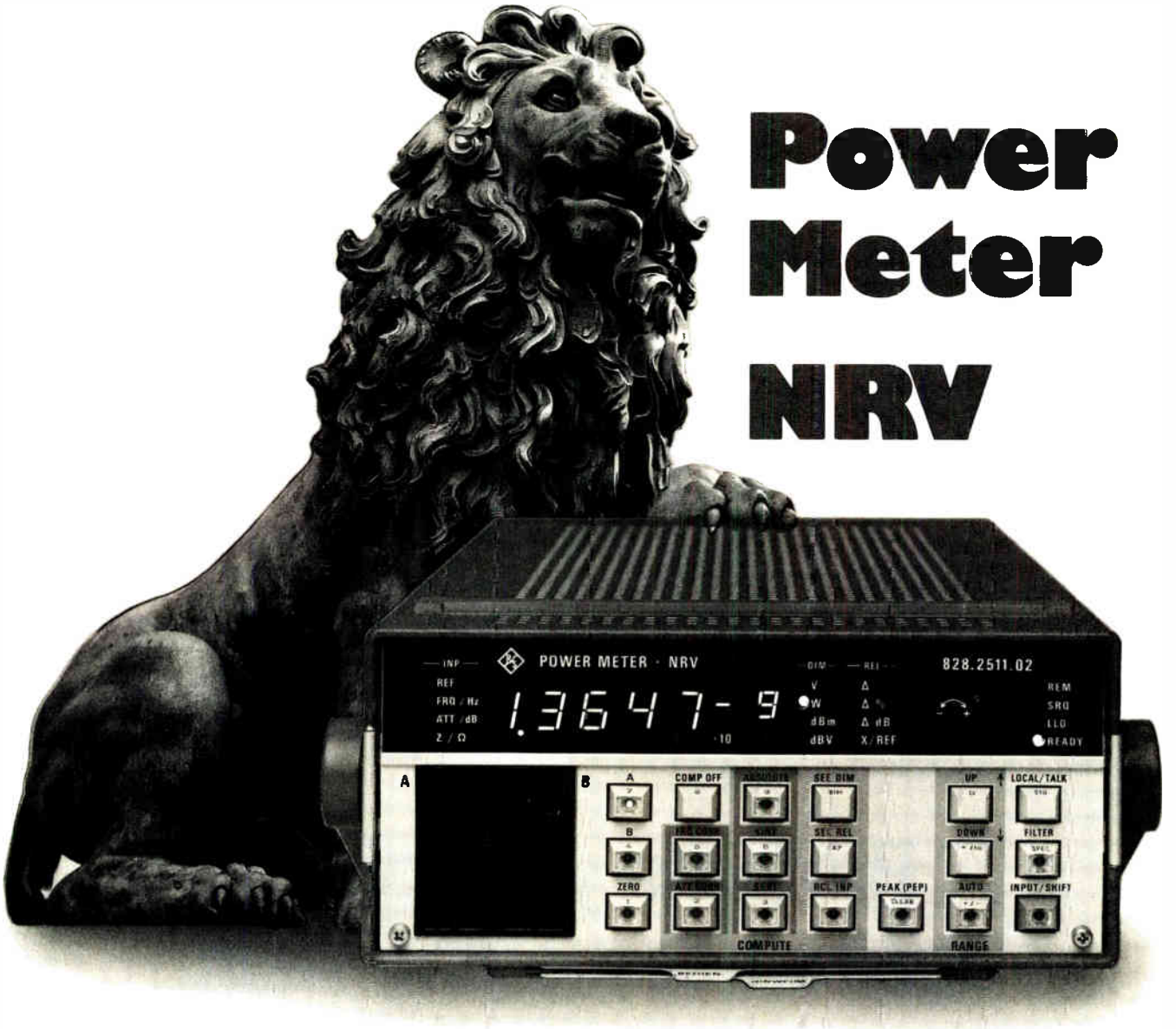

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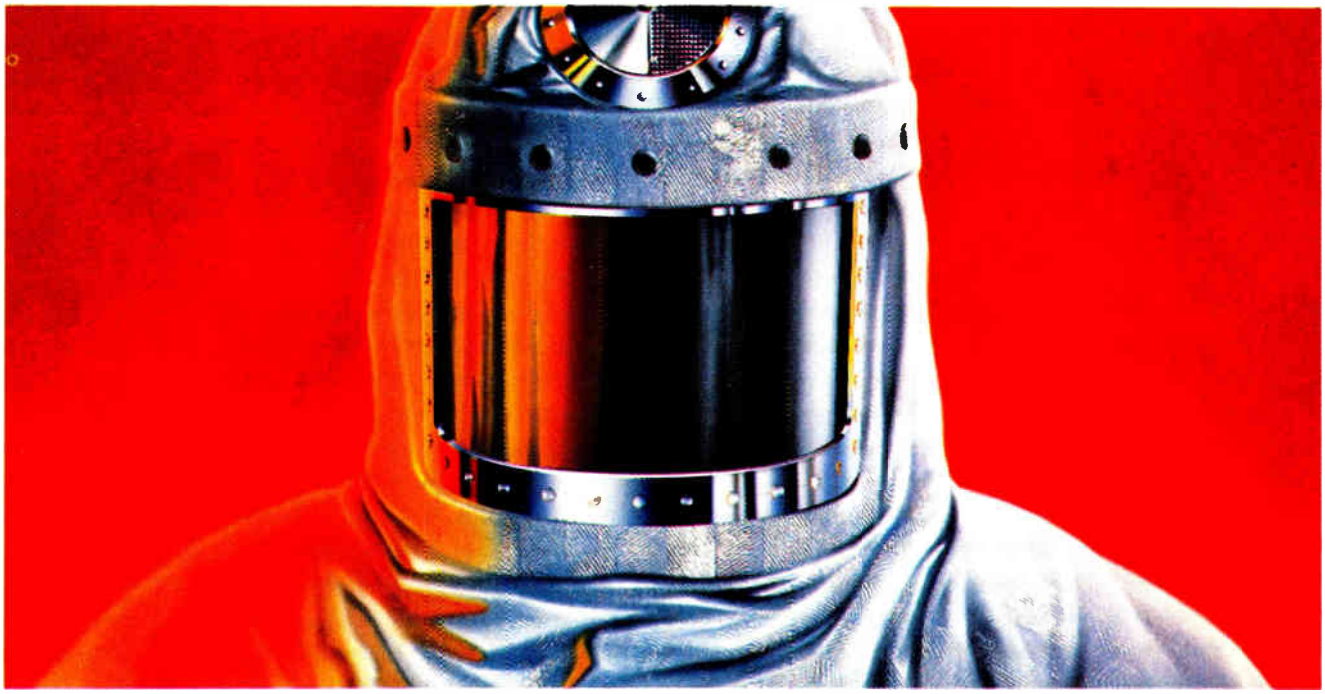

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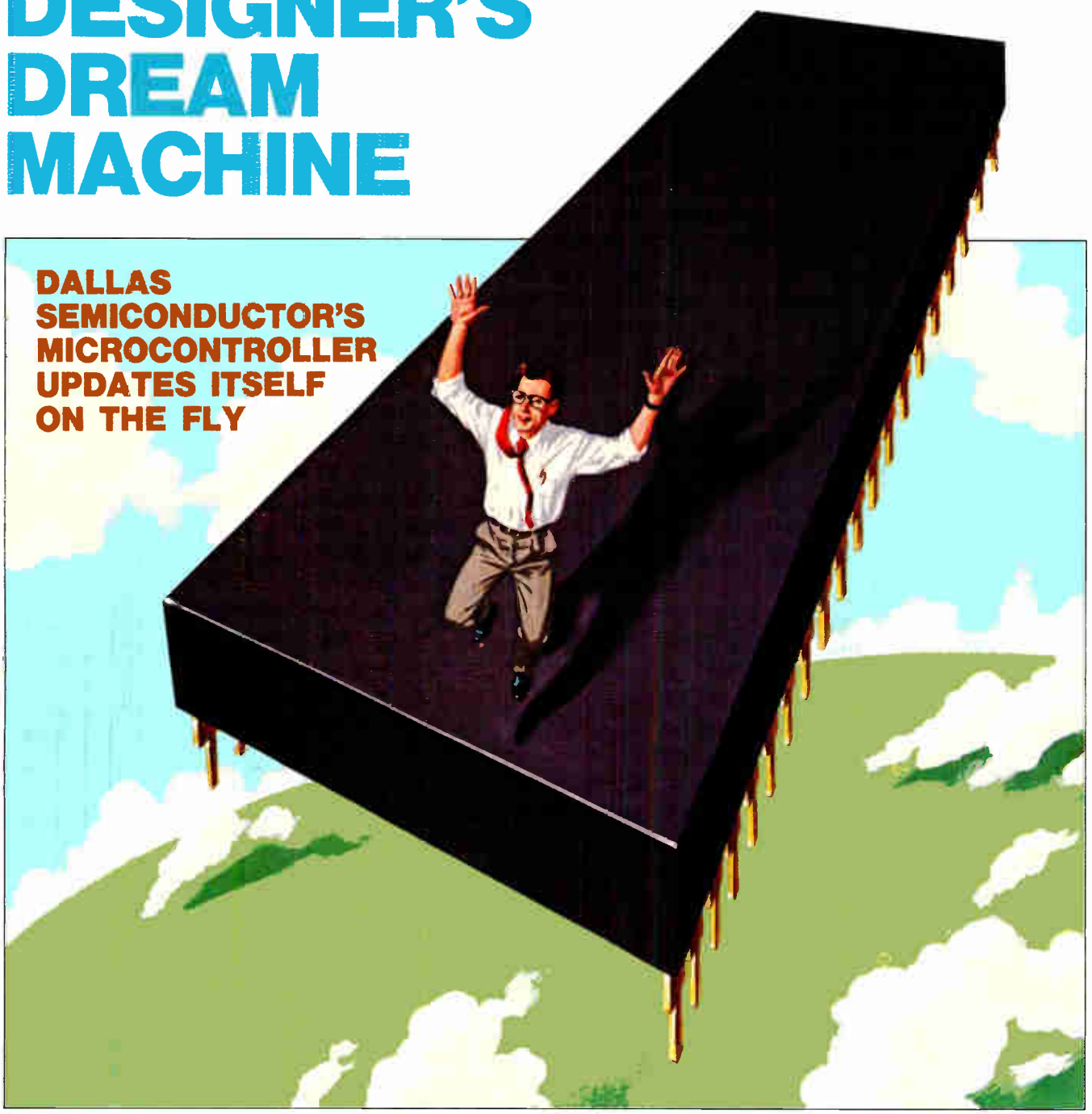
INSIDE TECHNOLOGY

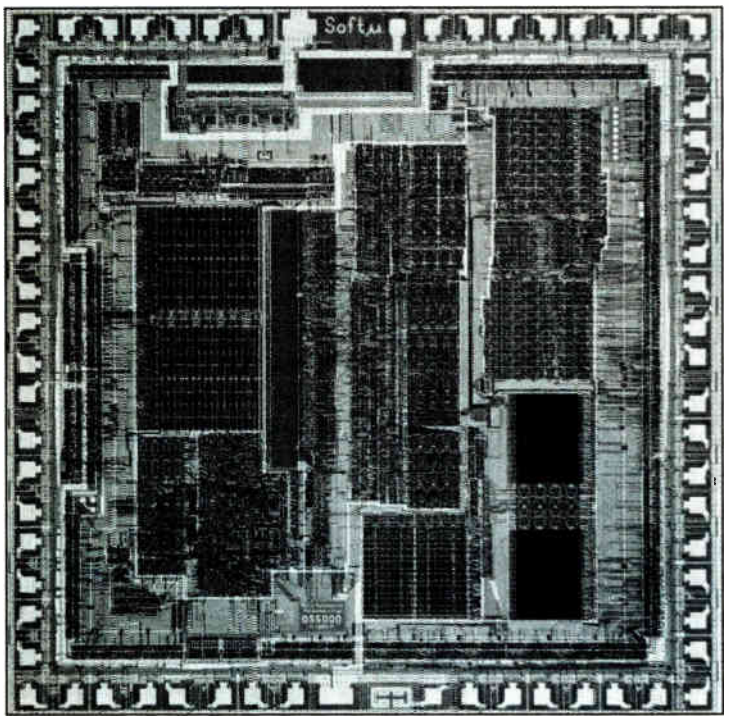
DESIGNER'S DREAM MACHINE

DALLAS SEMICONDUCTOR'S MICROCONTROLLER UPDATES ITSELF ON THE FLY



by Bernard C. Cole

Take a standard microcontroller chip, piggyback a fast static RAM on top so it can be reprogrammed remotely or on the fly, add a tiny lithium battery to make the package



1. COMBINATION. The DS5000 combines an 8051-compatible 8-bit CPU with logic expanding on-chip memory to 32-K bytes.

nonvolatile and some logic to make the data and microcode secure from prying eyes, and the result is a product that system designers dream about. That's exactly what Dallas Semiconductor Corp. has done with its new 8-bit CMOS DS5000 Soft Microcontroller.

Not only is the DS5000 pin- and function-compatible with Intel Corp.'s 8051/8751 microcontrollers, the industry standard, but it incorporates 4 to 16 times as much built-in program and data memory space. It can be read and erased in nanoseconds, unlike controllers based on electrically erasable programmable read-only memories, which typically take 10 ms. Moreover, the amount of data and program memory can be varied on the fly as a particular application dictates, using standard erasable-programmable-read-only-memory programmers, and done remotely, over a telephone line. Besides the security functions that guard proprietary application-program code, features are incorporated that save both data and program memory if external power fails, helping to ensure operation in harsh electrical environments.

The result is a versatile device that can make a system extremely reliable and completely upgradable from remote locations. The system can even improve its own performance, based on cumulative data captured in memory. The company believes the DS5000 (see fig. 1) is well-suited for a wide range of system designs, including systems that can reprogram themselves whenever operating conditions change. Among applications it cites are self-programming industrial controllers, handheld inventory-tracking terminals, data-encrypted bank-teller machines, trouble-reporting vending machines, and reprogrammable coin-operated telephones (see "Applications galore for a designer's dream," p. 57).

A number of these applications resemble those being targeted by makers of EEPROM-based microcontrollers. However, the density of on-chip EEPROM is about one eighth the density of the 32-K bytes of SRAM in the DS5000, and the write and erase times of EEPROM are much slower. The speed of the DS5000's SRAM, in particular, makes the device ideal for self-configuring microcontroller applications, says Don Folkes, product manager at the company.

TWO STEPS FORWARD

To make the DS5000, Dallas Semiconductor first took one step back, by developing an 8051/8751-compatible microcontroller without on-chip SRAM-based data memory and EPROM-based program memory. This allowed the company to then take two steps forward, offering an array of features not available on any other 8-bit microcontroller, using the chip area freed by removing the on-chip memory and its associated control logic and fitting it all in a 40-pin package with a pinout identical to that of the 8051/8751 (see fig. 2).

Among the features are the lithium battery proprietary circuitry that links the controller to up to 256-K of external embedded SRAM piggybacked atop it, and the power-protection and security functions. Other circuitry ensures that certain internal registers, configuration data, and key variables are also nonvolatile.

Operating on a 12-MHz clock, the DS5000 has a machine cycle time of 1 μs and can perform two read or write operations during each cycle, which is equivalent to that of an EPROM-based design of comparable memory size. The DS5000 comes equipped with 32-K bytes of SRAM, which can be dynamically partitioned into program and data storage—something not possible with ROM- or EPROM-based designs.

Fabricated using 3-μm, single-poly CMOS, the DS5000 contains a central processing unit that incorporates the 8051/8571 instruction set in more compact, hardwired random logic, instead of the more commonly used microcoded programmable logic array. The current version of the device, now available in sample quantities, measures 98,000 mil^2. The production version, available midyear, will be fabricated using 2-μm design rules, which will reduce the die area to 44,000 mil^2.

A total of 128 general-purpose registers and 28 special functions are included on the chip, as well as a serial input/output port and the standard 8051 set of parallel I/O lines. On-chip circuitry logically separates the memory space for the application software into program and data memory space. Seven additional special-function registers have been added to the original comple-

ment of 21, including a timed-access register that interfaces to logic and prevents unintentional access to key internal resources in the event of loss of software control caused by power-supply problems; a nonvolatile-status word register, which indicates the current status of the battery, and five encryption key registers that hold the 40-bit key word when operating in the encryption mode.

A total of 68 connections are present on the die itself, of which 40 are used to form the pinout, which is functionally identical to that of the industry-standard 8051, including the power supply, time base inputs for the on-chip crystal oscillation circuit, control and status signals, and four 8-bit I/O ports. As in the 8051, two of the ports can serve as an expanded bus, providing address, data, and control signals for interface to extended memory and I/O. In the expanded bus mode, up to 64-K bytes of program memory and 64-K bytes of data memory can be accessed through this bus.

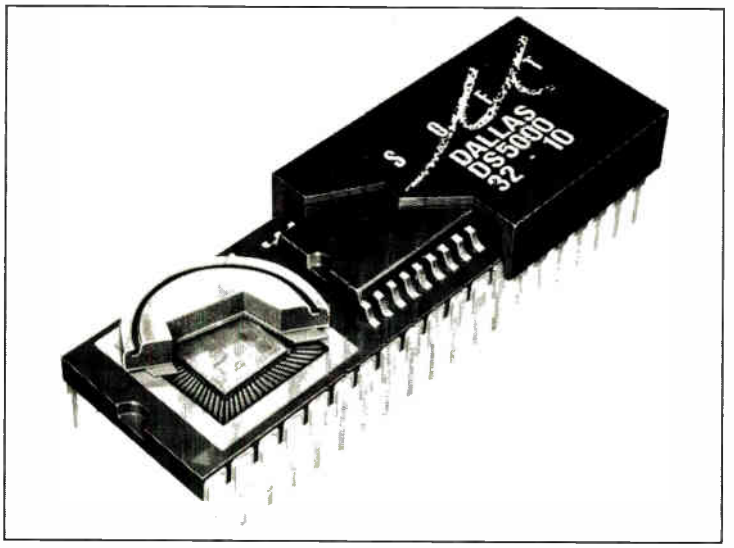
The DS5000 also has 28 additional connections internal to the package, which are used to provide nonvolatile control of I/O functions and for an embedded memory bus. The DS5000 uses the bus for access to the embedded program and data RAM in the same fashion as an 8051 would access internal ROM or EPROM. Using on-chip logic, application programs can partition this memory into variable portions of program or data memory.

As with the 8051/8751, four special function registers provide access for four parallel I/O port latches, through which a total of 32 bits of parallel I/O is available. The serial I/O port is implemented on the DS5000 with a receive-data buffer, a transmit-data buffer, and a control register. When the serial I/O function is enabled, two external I/O pins are reassigned in hardware to serve as the transmit- and receive-data functions.

ON-CHIP LOADER

The DS5000 program and data memory areas are loaded through an on-chip loader ROM, which accepts incoming data in either serial or parallel form and loads it into the program memory, the data memory, or the internal registers. Serial loading uses the on-chip serial I/O port to accept incoming data from a host computer with an RS-232-C port, such as a development system. Not only is it possible to initially boot up via the serial port, but any subsequent software reloading can be made at will during system operation. In parallel loading, the DS5000 emulates the 8751 programming mode so that industry-standard EPROM programmers can be used.

Among the key features of the DS5000 design are the various program and data security measures built into the device. These features guard against security breaches in several ways.

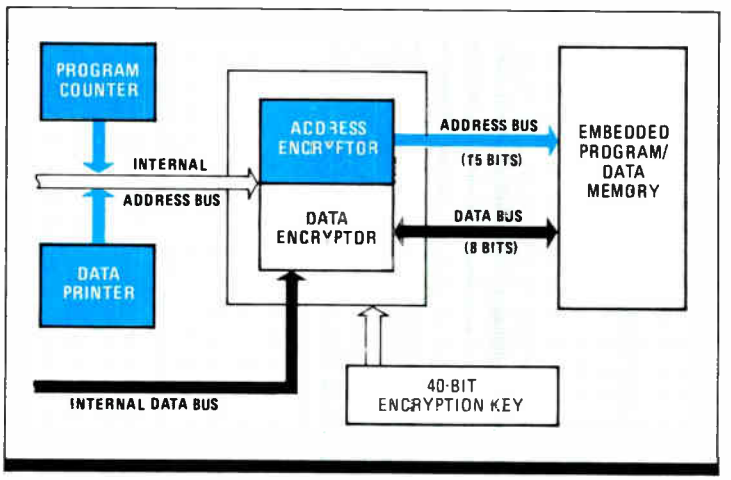


2. PIGGYBACK. A lithium battery and 256-K SRAM are piggybacked on the microcontroller chip in a 40-pin package.

In conventional microcontroller-based systems, for example, a complete listing of a program in machine-code form may be obtained by reading the contents of the memory in which it is stored. This makes understanding and duplication of firmware possible, and could permit the duplication of entire systems using that firmware.

Unrestricted knowledge of the algorithm that is implemented by the microcontroller can also cause problems. An instruction in its sequence can be disassembled or converted back to mnemonic form from its machine code representation. The instruction sequences for complete programs may be traced from their reset and interrupt vectors. Through disassembly of the machine code, it would be possible to determine the complete flow of the program as well as the algorithm it implements.

The first problem is solved in the DS5000 with encryption and decryption logic (see fig. 3). When the device is operating in the encryption mode and executing code from the embedded



3. SECURE. Application programs are protected from unauthorized copying with proprietary encryption and decryption logic and with a 40-bit-word key built into its DS5000 microcontroller.

memory, the address encryptor transforms logical addresses on the internal address bus into encrypted addresses, which appear on the embedded memory bus to the RAM. Similarly, the data encryptor transforms data on the internal data bus into encrypted data during write operations on the embedded memory bus. When data is read back, the data encryptor restores it to its true value. Although each encryptor uses its own algorithm for encrypting data, both depend on the 40-bit key word which is contained in the encryption key registers.

The second problem is solved with a special vector-RAM location on the chip, which stores the reset and interrupt vector code when the DS5000 is in the encryption mode. If these vectors were accessed from embedded RAM during the execution of the program, it would be possible to determine the encrypted value of known addresses, by forcing an interrupt or reset condition and then observing the resulting addresses on the external embedded memory address bus. By using on-chip RAM to contain the interrupt and reset vectors, the relationships are concealed.

In addition, partition address-locking logic protects the state of the partition address bits. It allows only authorized users to define the address boundary between the program and data memory areas in the embedded memory.

Even though the device's lithium battery is guaranteed to work for 10 years, Dallas Semiconductor engineers have incorporated proprietary on-chip logic to provide crashproof operation when system power is momentarily disrupted or removed entirely. These functions include a power-fail-warning interrupt, automatic power-down, and power-on restart. The power-fail-warning interrupt provides an early warning of a potential power failure so that the operational state of the system may be stored prior to a complete removal of system power. The automatic power-down feature causes all nonvolatile resources to be sustained at low current from the lithium battery while system power is removed. When the supply voltage is applied once again, the processor is automatically restarted with an internal flag set indicating that a power-on sequence has just been performed.

Regardless of whether the power merely fluctuates or stays off for years, the DS5000 can resume execution when power is reapplied, as if the failure had not occurred at all. Not only is on/off power cycling feasible, but it is a practical way of dramatically reducing power consumption when

A FREEWHEELING APPROACH PLAYED A MAJOR ROLE IN PRODUCT DESIGN

The development of the DS5000 microcontroller had its roots in the beginnings of Dallas Semiconductor itself. "Early on, we began discussing the impact of uninterruptible power sources and how these concepts could be incorporated into microcontrollers," says Wendell Little, who headed the design team. The original ideas about power protection were soon coupled with a far more complex concept: designing a microcontroller that can deal with change, or perhaps be smart enough to change itself—a cost-effective chip that can be adapted just before it gets shipped to the customer, or even after it has been installed in a system.

Taking off from those early discussions, the team soon developed a freewheeling approach that Little now says was a large factor in its success. "We all came here with different perspectives," Little says. "As each team member was brought in, he was invited to participate in the on-going, informal dialogue to improve the design."

Little, who received his BSEE in 1976 and his MSEE in 1978 from Colorado State University, brought to Dallas from Motorola Inc. microprocessor design expertise that was vital to the development of the product. At Motorola, he had been instrumental in bridging the gap between the use of custom integrated circuits and standard microprocessors in pager circuits. "The design time for custom ICs was an obvious bottleneck for product introduction," he says; his work applying microprocessors in place of custom circuits helped break that bottleneck.

On the DS5000 project, Little initially was in charge of the system and circuit design. Soon after, Matt Adams joined the design team, adding his circuit design and simulation expertise. Adams, who got a BSEE from Stanford in 1982 and an MSEE in 1984, took the assignment to begin using computer-aided-design equipment to validate the design concepts developed for the DS5000 chip.

DESIGN TEAM. Front row, from left, Don Folkes, Wendell Little, Steve Grider, and Matt Adams; back row from left, Mike Barnes and Richard Priddy.

Steve Grider joined the team next, and set about devising the test disciplines necessary to make the chip worthy of production. A graduate of Purdue University with a BSEE in 1978 and an MSEE in 1979, his previous microprocessor experience was at Mostek Corp.

Don Folkes, who gained microprocessor experience at both Motorola and Mostek, was brought in to do software development, documentation, and systems applications. Folkes received his BSEE from Iowa State University in 1976. Richard Priddy and Mike Barnes worked with the CAD tools to design the mask set.

The complete team blended easily into the looser, more personal working environment of the small startup company, Little says. And that environment help the team members create the streamlined product-development style that made it possible to develop a complex product in a relatively short time. "We can make decisions on products at Dallas Semiconductor without long, lengthy meetings," Little says. "We let those close to the product make the decisions. As a result, we were given a tremendous amount of individual freedom with the development of this product."

processing is not required.

In addition to the natural advantages of CMOS for low-power operation (50 to 100 mW active and as low as 50 nW standby), two modes initiated through software—idle and stop—enable the DS5000 to run at reduced power consumption when processing is not required and the supply voltage is within normal operating ranges.

The idle mode suspends operation of the CPU only, by halting its clock, reducing the number of switching nodes within the circuit. In the stop mode, the operation of the oscillator is halted, so that no internal clocking signals are produced for either the CPU or the I/O circuitry. Once in effect, the contents of the nonvolatile special-function registers and the data registers remain unchanged. Since the oscillator is disabled, the watchdog timer also stops operation. When the external reset signal terminates this mode, a delay is generated so the clock oscillator can start up and its frequency stabilize. In the idle mode, the DS5000 has a power dissipation of 31 mW. In the stop mode it is 400 microwatts.

Circuitry has also been incorporated to help ensure orderly execution of the application software in harsh electrical environments. In such environments, electrical transients such as a glitch on the clock or a noise spike on an I/O pin can cause software problems, among them the loss of key variables in some internal registers and the execution of code out of its logical sequence. Such transients can send the microcontroller into an indefinite period of seemingly random software execution.

Another feature ensures that electrical irregularities will not disrupt critical configuration registers in the DS5000. Timed-access logic on the chip permits protected bits to be written after execution of a specific multiple instruction sequence triggered by a timed-access register. This prevents a potentially catastrophic change in configuration by an inadvertent write when software control has been lost. □

APPLICATIONS GALORE FOR A DESIGNER'S DREAM

The people at Dallas Semiconductor Corp. think their static random-access memory backed with a lithium battery is going to reshape the use of reconfigurable 8-bit microcontrollers. They say that applications for the DS5000 cover a wide range of possibilities, from rugged systems built for military and industrial use to pay telephones that can be serviced remotely.

The DS5000, a low-power SRAM made nonvolatile by the embedded battery, has higher densities and stores bits much faster than electrically erasable programmable read-only memory. On the fly, the 40-pin DS5000 can dynamically repartition allotted memory space for more data or program storage, increasing its ability to reconfigure itself, compared with more conventional devices that rely on fixed amounts of ROM, EPROM, or RAM. The program and memory data stored in the SRAM is highly secure, since the chip can lock out unauthorized access to the program space with an encrypting 40-bit word. It is also protected from power failures and line glitches by features the company says make it virtually "crash-proof."

All of this—embedded battery power, fast-writing SRAM, security-lock features, and crash protection—combine to make the DS5000 immediately suitable for a range of self-configuring microcontroller applications, says the company's product manager, Don Folkes.

Among those applications will be various systems intended for use in harsh environments. Upcoming versions of the DS5000 will take advantage of high-temperature, solid-state batteries now under development by lithium cell vendors. The reliability and nonvolatility they offer will help the DS5000 to work in heavy-duty industrial and military systems. The device's crash-proof features enhance its value for such systems.

Beyond its stability under adverse conditions, the DS5000 offers an unusual degree of flexibility. That makes it useful in any applications that require fast reprogramming capabilities—many of which are similar to the applications envisioned by the makers of EEPROM-based microcontrollers. The difference is that DS5000 has eight times the on-chip density of EEPROM microcontrollers. Also, such EEPROM devices usually have erase-write cycles that are measured in milliseconds, not nanoseconds.

With its superior flexibility, say Dallas Semiconductor executives, the DS5000 will spark a number of innovative system designs, including systems that can reprogram themselves as the conditions under which they operate change. With the speed of the SRAM working in its favor, the device is able to load new programs far faster than can EEPROM-based devices. Also, the fast SRAM enables the DS5000 to reprogram itself with new software transmitted over phone lines at speeds of up to 9,600 baud. EEPROMs typically have writing cycles in the 10-millisecond range, which means that microcontrollers based on them would be overwhelmed by any phone-line transmission rates that reach 1,200 baud or greater.

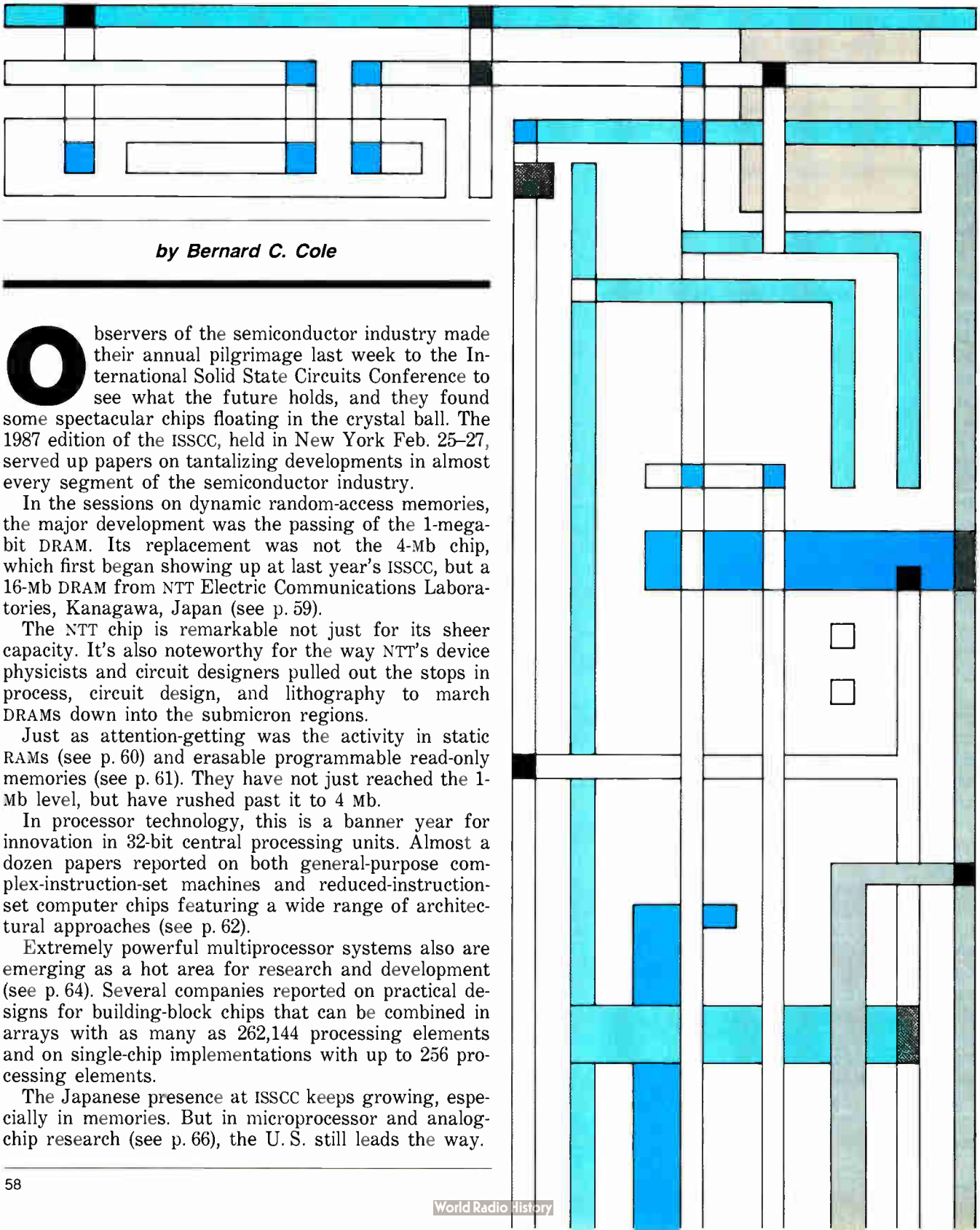
The speed with which the DS5000 stores data and programs also lies behind its crashproof features. "When you power down, you want to save things as quickly as possible," says Folkes. When the device senses an interruption in system power, it quickly stores away its work in the battery-backed SRAM. It can resume work whenever an acceptable level of system power is restored. Before the end of the year, an option in the DS5000 will be available to record time and date of power failures or system crashes.

One benefit of the power-protection capabilities is that the DS5000 is particularly suited for remote applications, where it is impractical to send human operators to reboot the system software. For example, "there are 12.5 million pay telephones in the U. S., and the owners want to teleservice them all as opposed to sending out repairmen," says Michael Bolan, vice president of marketing and one of the company's founders.

All in all, Bolan expects the DS5000 to be suitable for most microcontroller applications except for those that have no need for new software, data and program security, or event-logging capability. "A microwave manufacturer, who knows he is going to make 300,000 units with set firmware, will not be likely to use this chip," Bolan says.

"We will tend to go after applications where at least one of the attributes of the DS5000 will give it an overwhelming advantage," he adds. "It could be the ability to change its onboard software, or the ability to maintain and accumulate knowledge throughout the life of a system, or the security and the protection of programs." —*J.R.Lineback*

RECORD-SETTING CPUs, DRAMs, AND SRAMs STAR AT ISSCC



by Bernard C. Cole

Observers of the semiconductor industry made their annual pilgrimage last week to the International Solid State Circuits Conference to see what the future holds, and they found some spectacular chips floating in the crystal ball. The 1987 edition of the ISSCC, held in New York Feb. 25–27, served up papers on tantalizing developments in almost every segment of the semiconductor industry.

In the sessions on dynamic random-access memories, the major development was the passing of the 1-megabit DRAM. Its replacement was not the 4-Mb chip, which first began showing up at last year's ISSCC, but a 16-Mb DRAM from NTT Electric Communications Laboratories, Kanagawa, Japan (see p. 59).

The NTT chip is remarkable not just for its sheer capacity. It's also noteworthy for the way NTT's device physicists and circuit designers pulled out the stops in process, circuit design, and lithography to march DRAMs down into the submicron regions.

Just as attention-getting was the activity in static RAMs (see p. 60) and erasable programmable read-only memories (see p. 61). They have not just reached the 1-Mb level, but have rushed past it to 4 Mb.

In processor technology, this is a banner year for innovation in 32-bit central processing units. Almost a dozen papers reported on both general-purpose complex-instruction-set machines and reduced-instruction-set computer chips featuring a wide range of architectural approaches (see p. 62).

Extremely powerful multiprocessor systems also are emerging as a hot area for research and development (see p. 64). Several companies reported on practical designs for building-block chips that can be combined in arrays with as many as 262,144 processing elements and on single-chip implementations with up to 256 processing elements.

The Japanese presence at ISSCC keeps growing, especially in memories. But in microprocessor and analog-chip research (see p. 66), the U. S. still leads the way.

A 16-Mb DRAM GRABS THE SPOTLIGHT

The star of last year's ISSCC—the 1-Mb DRAM—was passé by the time the 1987 meeting was held. In this year's DRAM sessions, five out of the seven papers were on 4-Mb devices. Of the remaining two, one was a blockbuster—a 16-Mb chip from NTT Electrical Communications Laboratories. The other concerned a high-speed, low-power 1-Mb bi-CMOS DRAM from Hitachi Ltd.

To achieve its unprecedented density, the NTT 16-Mb chip (see fig. 1) stretches the limits of semiconductor technology in virtually every area: processes and lithography; cell, memory-array, and sense-amplifier designs; and error correction.

First of all, the team from the NTT lab in Kanagawa, Japan, used a 0.7-μm n-well CMOS process to fabricate the basic transistor structures with electron-beam direct-write lithographic techniques. For the memory cell itself, an isolation-merged vertical capacitor structure is used to achieve a cell size of only 4.9 μm^2. In this structure, a lattice trench 4-μm deep is formed to define each cell island, and an isolation region is merged into vertical cell capacitors formed on each cell island's sidewalls. The result is a cell capacitance of about 70 femtofarads, equivalent to that of cells about four times larger.

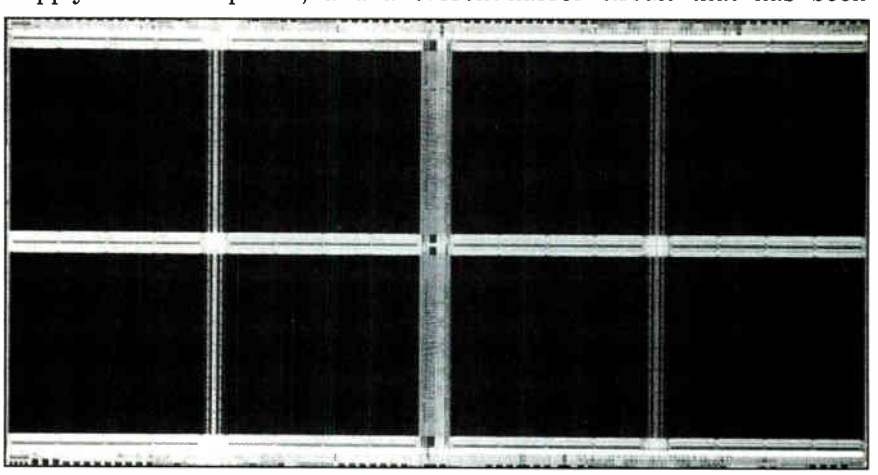
At the array level, NTT engineers have used what they call a main/sub bit-line structure, which consists of eight 2-Mb arrays. Each main array is divided into four sub-blocks, and each sub-block has a pair of sub-sense circuits arranged in 4-bit-line pitches, making it easy to lay out sense circuits in very small cell pitches. In this structure, the capacitance ratio of a bit line to a memory cell is cut to 6:1, so that very large bit-line signals—approaching 200 mV—can be generated.

The NTT 16-Mb circuit also represents the first major departure from the 5-V operating supply that has been the standard in the industry for almost 10 years. To avoid such device-physics constraints as punch-through, gate-dielectric breakdown, and hot-electron effects, the chip has been designed for 3.3-V operation. By doing so, the NTT engineers also reduced peak current and power consumption. At 500 mW, the 16-Mb device equals or betters many 1- and 4-Mb devices in these respects.

However, the lower voltage impairs the chip's ability to deal rapidly with the large word-line loads found in megabit memories. So to keep access times in the 80-ns range and cycle times to no more than 180 ns, the NTT design uses a new sense circuit that incorporates n-channel cell transistors, p-channel flip-flops for data sensing, and pseudo-grounded bit lines for initialization. The result is operating speed—including the rise time of the word line—about 10 ns faster than that of conventional sense-amplifier circuits.

Finally, to deal with the reduction in chip yield because of increased memory-cell defects as array sizes increase, the NTT engineers use selector-line merged error-checking-and-correction circuitry, assigning 33 parity cells to every 256 memory cells. Current error-correction approaches have an access penalty of as much as 20 ns, but the NTT approach uses transmission parity checkers and selectors to reduce this penalty to no more than 5 ns. Data from cells in either horizontal or vertical parity groups are arranged into column circuits without long bus lines by a diagonal assignment technique that assigns each cell in one selector to different horizontal and vertical groups. In such a structure, a parity-checking operation can be carried out at the same time as a data-reading operation. And because these error-correction circuits need no long bus lines—which keeps their load capacitance very small—the access penalty they exact is drastically reduced.

Another DRAM standout at the other end of the megabit spectrum—Hitachi Research Laboratory's 1-Mb bi-CMOS DRAM—is remarkable for its combination bipolar speed and power-frugal CMOS. It combines a typical access time of 35 ns with a typical power dissipation of only 450 mW. Key breakthroughs that allow such a combination of high performance and low power dissipation include a bi-CMOS device structure that uses twin wells formed in a 1.5-μm epitaxial layer; the use of fast bipolar transistors throughout for word and column drivers, main amplifiers, and clock drivers; a bi-CMOS clock driver designed to limit on-chip voltage while also reducing power dissipation; and a current-mirror circuit that has been

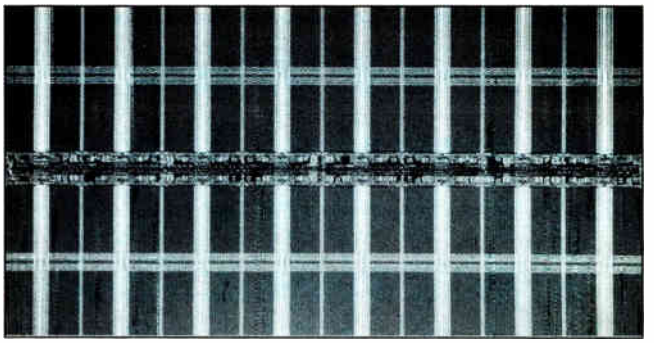


1. BIG ONE. NTT has pushed DRAM density out to the 16-Mb level with its experimental chip, built with e-beam direct writing, trench capacitor structures, and other advanced techniques.

combined with a voltage-limiting comparator to reduce power dissipation without slowing down the circuit.

Battling it out at the 4-Mb level for fastest access time are chips from Fujitsu, Hitachi, IBM, and Mitsubishi Electric. Checking in with a 90-ns row-address access time, Fujitsu Ltd.'s 4-Mb device uses an 0.8-μm CMOS process and a folded-bit-line, adaptive-sidewall, isolated-capacitance cell that measures only 10.9 μm^2. Hitachi Ltd.'s quicker 70-ns device is fabricated using tighter, 0.7-μm CMOS design rules to achieve a cell size of only 7.5 μm^2.

At the 65-ns level, Hitachi and IBM Corp. stick with traditional DRAM structures. In its 0.8-μm double-well CMOS device, Hitachi achieves its speed with a twisted-drive-line sense amplifier scheme and a multiphase drive-sense circuit. The amplifier setup allows faster operation of the sense amplifiers by effectively halving the load capacitance associated with their drive lines, and the multiphase drive-sense circuit suppresses the power-supply peak current—a significant problem for 4-Mb DRAMs operating from 5-V supplies. The chip is divided into four arrays, with row and column decoders in the middle. The two drive lines for the CMOS sense amplifiers are twisted at the middle of the array, and two p-MOS drivers and two n-MOS drivers are connected to each end of the drive lines. This cuts the capacitance of the drive lines in half, decreasing the associated time constant and yielding sense amplifiers that are twice as fast as those in traditional configurations.

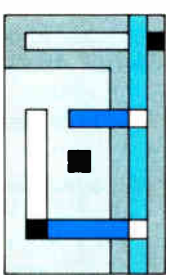


2. A FAST 4 Mb. IBM has built a 65-ns 4-Mb DRAM with a 0.8-μm, 3.3-V CMOS process and small cells based on trench capacitors.

To achieve high speed in its 4-Mb DRAM (see fig. 2), researchers at IBM's General Technology Division in Essex Junction, Vt., combine an 0.8-μm, 3.3-V, n-well CMOS process with a substrate-plate trench cell, formed from a trench capacitor that extends from the surface through the well, through the epitaxial layer, and into the doped substrate. The polysilicon inside the trench is the storage node, and the bulk silicon surrounding the trench is the plate electrode. While the resulting small cell size—about 11 μm^2—would normally reduce the signal level, thus slowing down the circuit, IBM designers counteracted this effect with thick interlevel insulators and narrow metal lines that reduce the bit-line capacitance.

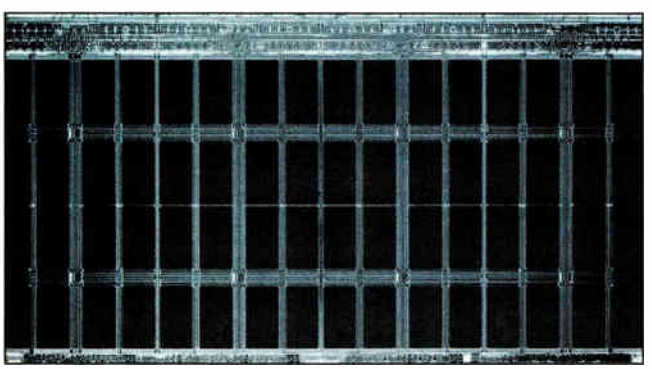
STATIC RAMs

MANY PATHS LEAD TO 1-Mb SRAMS



The news that several companies have hit the 1-Mb level in static RAMs generated almost as much excitement at ISSCC as the move of much simpler dynamic random-access memories toward the 16-Mb level.

Building a 1-Mb SRAM with conventional cell techniques is an impressive achievement, and Hitachi and Sony have done just that. But other papers described different approaches needed to push beyond the 1-Mb level—two of which, Oki Electric's and Hitachi's, incorporate elements of DRAM design.



3. DUAL-MODE RAM. Oki Electric's 4-Mb RAM uses DRAM cells but operates in either a pseudostatic or virtually static mode.

Staying with traditional SRAM cells, Hitachi Ltd. has built a 128-K-by-8-bit chip, using an 0.8-μm triple-poly CMOS process. The Tokyo company's chip achieves a typical address access time of 42 ns with an active power dissipation of 200 mW by combining a double-polycide word-line technique and a multiple-by-eight sense-amplifier design. The memory is organized into eight subplanes with common data lines divided into eight segments, each of which is connected to its own sense amplifiers and multiplexers. The first polycide level is used for the transistor gates, the second for the supply-voltage lines.

Edging out the Hitachi chip in both speed and power dissipation, Sony Corp.'s 128-K-by-8-bit SRAM boasts a 35-ns address access time at 100 mW. It is also built with conventional cells, using a 1-μm double-poly, double-metal CMOS process. The Kanagawa, Japan, company's chip achieves its speed through the use of a divided word-line technique: the array is partitioned into 16 sections with 8 input/output lines and 8 amplifiers so that only 8 pairs of short data lines are connected to one sense amplifier.

SRAM technology has achieved its current density partly by using ion-implanted polysilicon load resistors instead of the two pull-up transistors, reducing

the cell from six to four transistors. But going beyond 1-Mb densities in SRAMs will require a fundamental rethinking of cell design.

For example, researchers at Oki Electric Co. in Tokyo have moved away from the traditional SRAM structure because of the difficulty in fabricating the submicron-geometry resistors with megohm impedances needed in megabit SRAMs. They devised a hybrid design that incorporates DRAM cells and the refresh circuitry on chip.

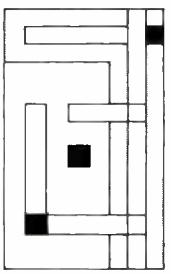
Using a buried stacked-capacitor DRAM cell fabricated with 1-μm n-well polycide CMOS, they have built a 512-K-by-8-bit RAM that operates as a 60-ns virtually static part or as a 95-ns pseudostatic RAM (see fig. 3). Both types use on-chip refresh circuits, but in the virtually static mode refreshing is interleaved with device operations, making it transparent at the system level, and in the pseudostatic mode refreshing occurs in the same kind of sequence as in systems using DRAMs.

A SRAM cell from Hitachi VLSI Engineering Corp., Tokyo, shows promise of pushing SRAMs even farther into the megabit range. The chip does not require polysilicon load resistors; refresh is totally transparent and requires virtually no overhead circuitry. A switched-capacitor load technique, which will reduce cell sizes by 30% to 50% without further scaling, is the key to this capability.

The basic SRAM cell contains four n-MOS flip-flops. An on-chip refresh oscillator generates a refresh-address signal continuously in an asynchronous mode, from which a refresh-address-valid signal is extracted. This permits the transfer of the refresh address to the row decoders and word drivers. The technique, used in a 256-K SRAM fabricated using a 0.7-μm CMOS process, results in typical access times of 43 ns.

ERASABLE PROMs

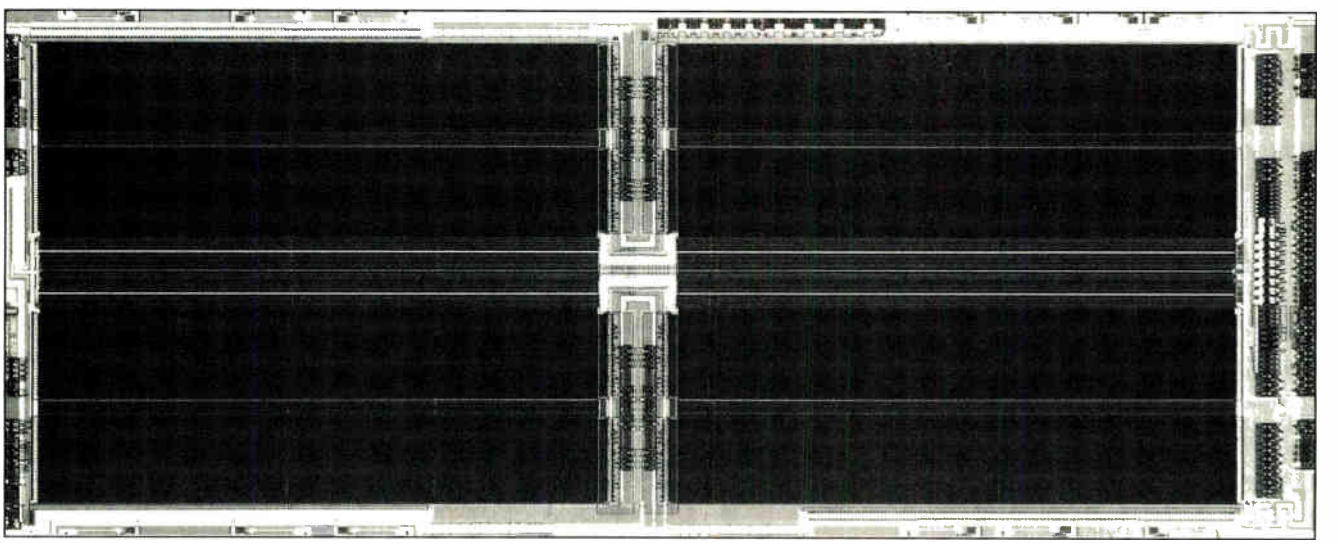
EPROM DENSITY RECORD SOARS TO 4 Mb



Nonvolatile memory is moving away from its traditional "also-ran" position, trailing both static and dynamic random-access memories in terms of density and speed. At the ISSCC, Toshiba described how it has pushed the EPROM density limit out to 4 Mb through aggressive process scaling. The densest EPROMs now available are at the 256-K level. Engineers from Fujitsu and Texas Instruments reported on parts that have reached the 1-Mb level, but Fujitsu emphasizes speed, with an 80-ns access time. Both companies stress wide-word organizations for compatibility with 16- and 32-bit microprocessors.

The 4-Mb EPROM from Toshiba Corp., Kawasaki, Japan, uses an 0.8-μm double-polysilicon CMOS process to move EPROMs past SRAMs and to achieve parity with DRAMs in terms of density (see fig. 4). The basic EPROM cell measures only 9 μm^2, matching that of many DRAM cells. Both the first gate oxide and the interpoly dielectric thicknesses have been scaled down to no more than 200 Å. The reduced size of the gates tends to reduce capacitive coupling, but the coupling between the floating gate and the control gate has been kept strong enough to maintain a reasonable 10-μs/byte programming time. Programming voltage drops from the traditional 25 V down to 10.5 V, and the 512-K-by-8-bit part boasts a high cell current of about 100 μA, resulting in a typical access time of 120 ns.

Contributing to the relatively short access time and to low operational power, a new sense-amplifier circuit combines a traditional differential amplifier and a new bias circuit. In addition, the memory array has been organized into two sets of 1,024 columns by 2,048 rows, with common sense amplifiers



4. NONVOLATILE DENSITY. Toshiba's 4-Mb EPROM uses a 0.8-μm double-polysilicon process; its cells measure only 9 μm^2 in area.

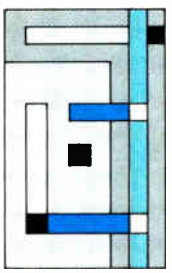
down the center and common row- and column-address logic at the top and bottom. This arrangement minimizes bit-line division and word-line delay.

By using a multiplexed address/data-bus scheme, designers at Fujitsu Ltd., Kawasaki, were able to achieve access times of about 80 ns in their 1-Mb EPROM chip. This scheme also controls the output data width to accommodate either word-wide or byte-wide buses. Another speed boost comes from a precharge-circuit design that eliminates the time wasted waiting for the sense amplifiers to charge the bit and sense lines. Access time is, for all practical purposes, independent of the mutual conductance of the cell transistor—a roadblock to speed enhancement in traditional designs. To achieve megabit density, Fujitsu engineers have used an advanced 1.5-μm tungsten polycide n-well CMOS process to achieve a cell size of about 18 μm^2.

Texas Instruments Inc. of Dallas has built a slower 1-Mb chip—access time is 150 ns at an operating power of 220 mW—but it is fully static and drops data on a bus 16 bits at a time to feed today's processors, just as the Fujitsu EPROM does. TI has taken a more aggressive approach to cell density than Fujitsu, as well, combining a 1.5-μm twin-well CMOS process with a self-aligned thick-oxide floating-gate avalanched-MOS EPROM cell with buried n^+ sources and drains. The result is a cell size of about 14 μm^2 with interpoly dielectric and first-gate-oxide thicknesses of 350 Å. Tungsten silicide is used on the periphery gates and word lines to reduce propagation delay.

MICROPROCESSORS

RISC CHIPS SET PACE FOR 32-BIT CPUs

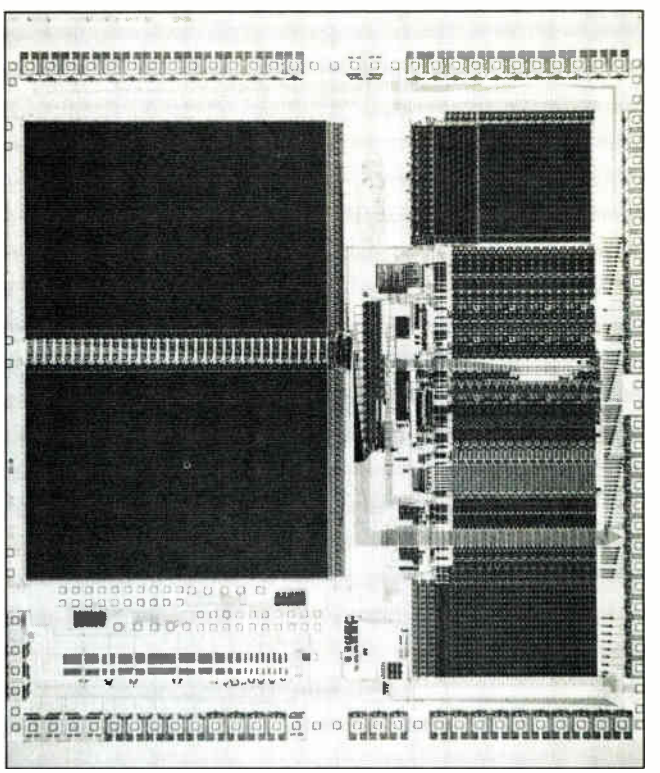


The pace of experimentation and innovation is fast and furious in the world of 32-bit microprocessors, as the wide array of specialized architectures disclosed at the ISSCC shows. Half a dozen papers report on designing single-chip reduced-instruction-set computers, and two are on language-specific machines. In traditional complex-instruction-set computers, three papers report researchers' efforts to reduce multiboard mainframe central processing units to no more than two or three integrated circuits.

The researchers are taking advantage of the densities available with advanced very large-scale integrated CMOS processes to devise architectures that boost throughput ever higher—into the millions-of-operations-per-second range. In the RISC designs, the aim is to improve throughput by reducing the number of complex memory-fetching instructions. In the language-specific machines, designers are incorporating high-level-language instructions directly in microcode on chip. This approach eliminates the time required to translate a high-level instruction into a machine-level instruction. The CISC machines employ a variety of complex architectural innovations such as on-chip cache, memory management, and pipelining to boost their speed.

From one of the schools that started the trend toward RISC technology—Stanford University's Center for Integrated Computing in Stanford, Calif.—comes the MIPS-X, a third-generation 32-bit RISC chip with 2-K bytes of on-board instruction-cache memory (see fig. 5). Even when compared with earlier-generation RISC machines, MIPS-X uses a simple instruction format that can be decoded quickly, allowing an instruction to be issued every cycle. Most instructions require an average of two cycles each in most complex-instruction-set machines and some RISC processors. MIPS-X uses a load/store architecture similar to other RISC machines and a speed-enhancing repertoire of only thirty-seven 32-bit instructions. But the key to its high throughput is a large on-chip instruction cache to fetch two words per cycle, reducing the off-chip instruction bandwidth by a factor of five and the overall bandwidth by 2.5. The 150,000-transistor CPU has a peak operating frequency of 20 MHz using a two-phase clock and dissipates less than 1 W. It is fabricated using 2-μm double-metal n-well CMOS.

One of the leaders in commercializing RISC architectures, Hewlett-Packard, is not resting on its laurels. HP described at ISSCC two new RISC machines it



5. CACHING IN. The MIPS-X 32-bit RISC chip from Stanford University uses a simple instruction format that can be decoded quickly.

is working on. A 32-bit CPU, under development at its Fort Collins, Colo., facility, is capable of up to 15 million instructions per second. It is designed to implement a set of 140 instructions using direct hardware decoding and execution. A 1.5-μm n-MOS process with two levels of tungsten metallization lets the 115,000-transistor chip operate at 30 MHz and dissipate 10 W.

Other speed-enhancing features are 32 general registers; 25 control registers; a five-stage, three-word-deep instruction pipeline; a shift/merge unit; and a 32-bit arithmetic logic unit—all of which communicate with one another via seven internal 32-bit buses. The chip includes logic for decoding and prioritizing traps and interrupts. It has a special bus interface that supports data transfers among the cache, the CPU, and its coprocessors, and which can handle the copy-in and copy-back traffic between cache and main memory.

HP takes a different tack with a 32-bit RISC chip from its Palo Alto, Calif., facility. The chip not only eliminates many instructions that require more than a single clock cycle to execute, but it also reduces the total number of instructions to an absolute minimum. The chip uses a common multiplexed data and address bus and incorporates a five-stage pipeline to allow most instructions—excluding memory, coprocessor, and branch instructions—to execute in a single clock cycle.

Fabricated using a 1.6-μm n-well CMOS process with two levels of metal and polysilicon gates, the 164,000-transistor chip features a peak performance of 8 mips and dissipates about 1 W. It incorporates a 32-bit ALU, a 256-byte instruction cache, and a memory-management unit made up of a two-set, 32-entry-table lookaside buffer.

Designers at AT&T Bell Laboratories presented two papers describing their high-speed, low-power 32-bit Crisp, or CMOS reduced-instruction-set processor (see fig. 6). Crisp can execute instructions at up to 16 mips using a 16-MHz clock—yet it dissipates only ½ W. Fabricated using a 1.75-μm twin-tub process with three levels of interconnection, the 172,000-transistor CPU is a memory-to-memory registerless machine with only 25 instructions and four addressing modes.

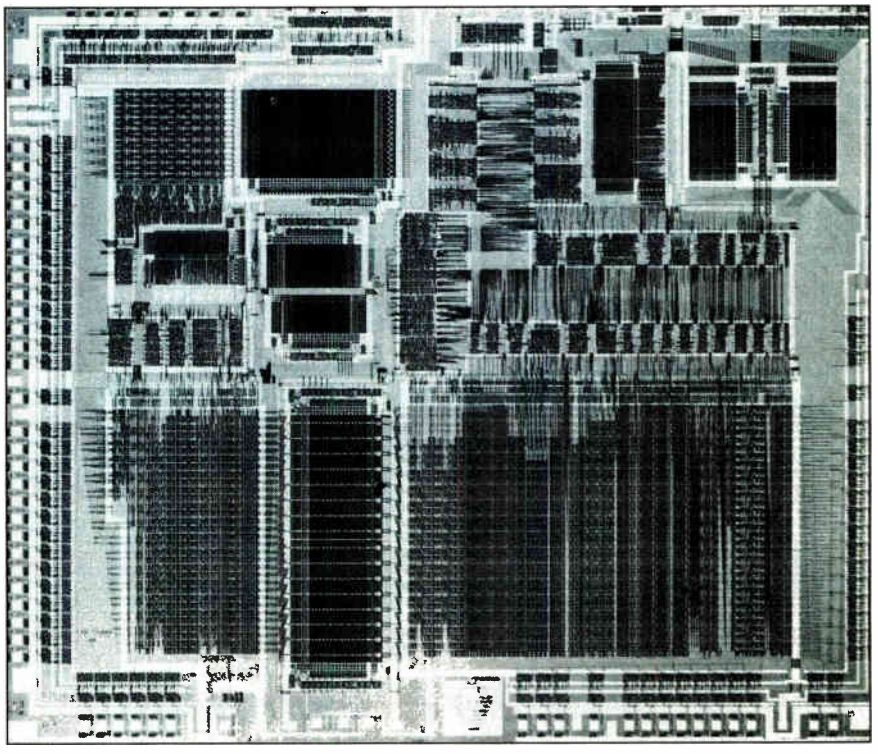
To give it speed, Crisp is organized into two logically separate machines, a prefetch decode unit and an execution unit, each with a three-stage pipeline. It contains seven static random-access memory arrays, for a total of 13-K. Unlike most processors, the machine has no visible address or data registers. Instead, 32 internal stack-cache registers are automatically allocated and mapped into the on-chip SRAM, allowing the number of registers to be increased in future implementations without software changes. The Crisp chip, using a technique called branch folding, can execute branches simultaneously with other nonbranching instructions, so they can be executed in essentially zero time.

One alternative to reducing the number of instructions to speed a computer's throughput is to make it more language-specific. Texas Instruments Inc. of Dallas and NTT Electrical Communications Laboratory, Tokyo, have taken this route with their Lisp CPUs. TI offers a 1-cm² chip fabricated in 1.25-μm CMOS and containing 553,000 transistors. With 114-K bits of on-chip RAM, it is designed to run both on-chip and external microcode and can execute instructions in a single 40-ns clock cycle.

NTT engineers, taking a more conservative approach, have used 2-μm CMOS to fabricate a 2.25-cm² device with only 80,000 transistors and a more modest 180-ns instruction cycle time. The NTT design contains a 32-bit ALU with two modes, for tagged and untagged data, and a 32-word-by-32-bit two-port RAM. It requires several external SRAMs for writable-control-store microcode and some bus-transceiver circuits to operate as a complete Lisp machine.

As popular as RISC and language-specific machines have become, complex-instruction-set computers are still the main thrust of developmental efforts at most computer and electronics companies. Designers are squeezing all the speed they can out of current processes to boost performance of CISC machines. They also are taking advantage of the high densities of current MOS processes to incorporate architectural features that boost performance even farther.

For example, designers at Digital Equipment



6. FOLDS BRANCHES. Combining a prefetch-decode unit with an execution unit, AT&T's Crisp RISC processor executes branching instructions in what amounts to no time at all.

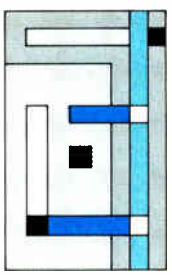
Corp. in Hudson, Mass., described a VAX-compatible 32-bit single-chip microprocessor with such advanced architectural features as an on-chip 1-K-byte instruction and data cache with tag and data parity, pipelined microinstruction execution, overlapped instruction prefetching, parallel instruction decoding, and on-chip memory management. The 180,000-transistor chip has a set of 304 instructions and a 100-ns cycle time using a 25-MHz clock. It is fabricated with a 2-μm double-metal CMOS process.

And engineers from Hitachi Ltd. described a set of three VLSI circuits fabricated with 1.3-μm double-metal CMOS designed to implement a full set of mainframe instructions. The Kanagawa, Japan, company's chip set has a general processing unit for arithmetic and logic operations, an instruction processing unit for instruction decoding, and an address unit for cache control and address translation. It is capable of instruction cycle times as low as 60 ns when used with external cache and control-store memory implemented using the company's high speed bi-CMOS SRAMs.

Going all out for speed are two high-performance gate-array macros—a five-port general-purpose register file and a 32-bit ALU—from IBM's Thomas J. Watson Research Center in Yorktown Heights, N. Y. The register file has an access time of 6.5 ns, and the ALU has an add-instruction speed of 8 ns, operating at a clock rate of 50 MHz. It is fabricated using a 0.5-μm CMOS process.

MULTIPROCESSOR CHIPS

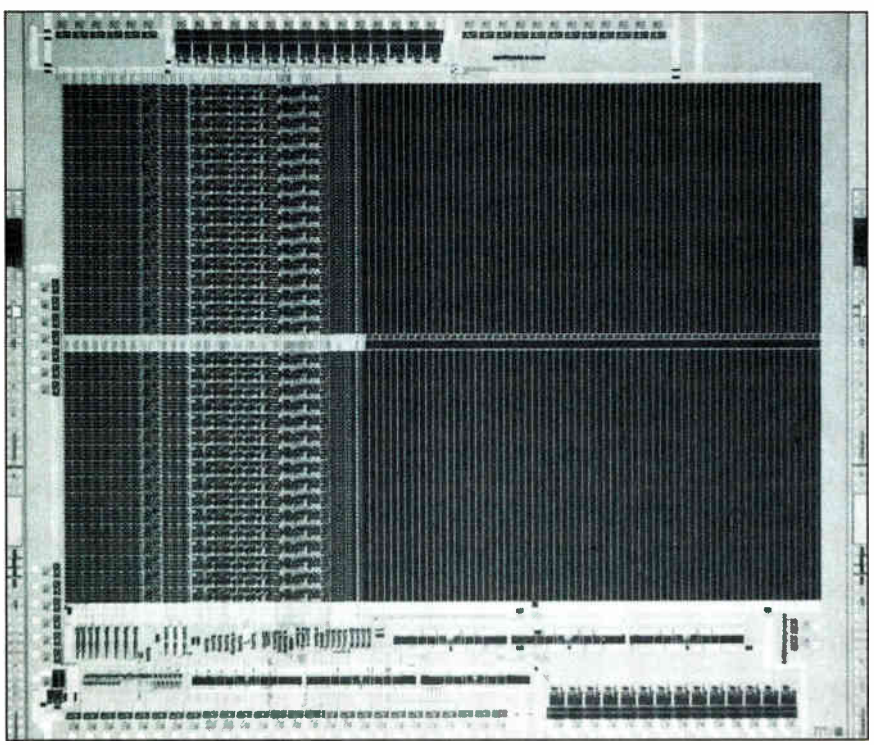
CPU ARRAYS GO FOR 10 GIGAFLOPS



Four designs for large and powerful multiprocessor arrays stood out among the many general-purpose central processing units and special-purpose processor chips that were described at this year's ISSCC. One of the designs, a two-chip configuration from Digital Equipment Corp., is remarkable for the sheer number of operations per second that a full-scale array built from these chips can pump out: up to 10 gigaflops. Another intriguing design, from the UK's Brunel University, combines multiple computing elements with multiple on-chip memory elements. And researchers from General Electric Co. and Hitachi Ltd. both presented papers on digital-signal-processing chips that are designed for multiprocessing configurations.

The general-purpose two-chip set from DEC's Hudson, Mass., operation consists of a 32-processor chip (see fig. 7) and a router, both fabricated in 2-μm double-metal CMOS. It is intended for a massively parallel architecture with up to 262,144 processing elements: 8,192 of the 32-element processor chips, and 384 router chips. This configuration would have a peak performance of 2.6 trillion 4-bit operations/ s or 10 billion floating-point operations/s.

The processing-element chip has 242,000 transistors and dissipates only 0.5 W. Each of the 32 individual processing elements on the chip has 1-K of static random-access memory, two shift registers whose size is programmable, a 4-bit adder, an arithmetic logic unit, two 1-bit registers, and neighbor and router communications paths.



7. MASSIVE PARALLELS. DEC has designed a chip with 32 processors on it and a companion chip for routing signals in a system harnessing up to 8,192 of the processor chips.

A 4-bit operation in each processing element requires 100 ns to execute; therefore one chip can handle 320 million 4-bit operations per second. Operations greater than 4 bits are performed in nibble-serial fashion; for example, 40 million 32-bit operations can be executed in 1 second. Also contained on chip is logic that allows a processing element to operate in a 4-K memory mode by connecting it to the memory of three other processing elements.

Dissipating less than 1.5 W, DEC's companion router chip contains 64 data inputs and 64 data outputs. It allows any processing element to communicate directly

with any other element in the overall machine.

An equally impressive chip, aimed at more specialized image-processing tasks, is a 256-element single-instruction-, multiple-data-stream parallel processing chip from Brunel University that contains not only eight times as many computing elements but on-chip associative memory as well. Designed for such applications as image enhancement, scene analysis, and pattern recognition, the single-chip array-processing element, or Scape, can execute more than 262 million 8-bit addition operations per second. The 145,000-transistor chip uses a 2-μm double-metal bulk p-well CMOS process and incorporates 256 fine-grained associative-processing elements. Using a 10-MHz clock, a Scape chip can do a three-by-three 8-bit spatial convolution in 95 μs, and an 8-bit contrast-switching operation in 8.4 μs.

Each Scape chip dissipates less than 1 W and contains four types of functional blocks: a single central micro-order generation logic block, four associative memory arrays, two bit-column logic blocks, and four word-control logic blocks. The generation logic block contains a two-level programmable logic array that generates four internal control states per major bus cycle; this block provides overall control of the other processing elements on the chip.

Each associative-memory block contains 64 word rows of 32 data bits each and five flag bits. Each word of local store constitutes an associative-processing element supporting bit-serial and bit-parallel associative-match, write, and read operations. Bit-column access to these blocks is via the two bit-column logic blocks, which incorporate bit-serial data-routing logic and byte- and word-parallel data input/output channels. Conditional bit-masking data-interpretation logic is also incorporated to support bit-serial column addressing over dynamically programmable serial fields set up in the on-chip field-partition register.

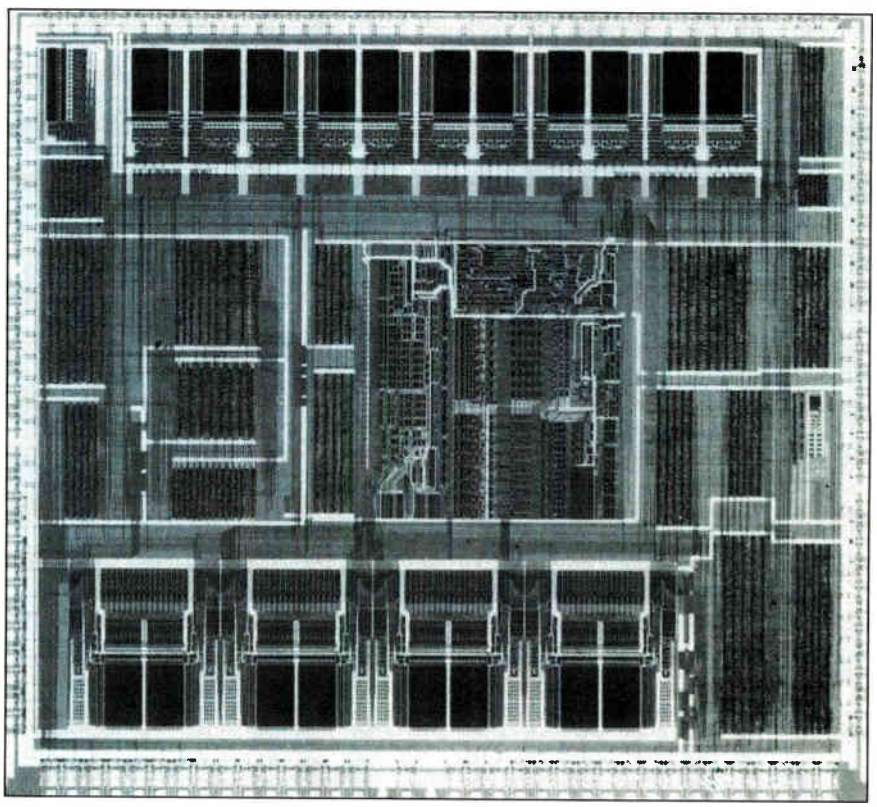
The word-control logic blocks do word-row interfacing with the associative-memory blocks. These comprise 256 bit-slice elements that activate word rows of the associative-memory blocks for read or write operations according to a selected mapping of the response to a preceding content search.

The world of digital signal processing also saw the arrival at ISSCC of two building-block chips for multiple-processor arrays of potentially spectacular performance. Researchers at General Electric's Electronics Laboratory in Syracuse, N. Y., have designed a programmable signal-processing chip for large arrays of 100 to 1,000 elements. Preprogrammed with algorithms for many basic signal-processing functions, the architecture not only supports many filter topologies but can be used in such applications as fast Fourier transforms, two-dimensional convolutions, and matrix operations.

Using a single one of these chips, a 256-point complex floating-point FFT can be completed in less than 400 μs, and a 256-point finite-impulse-response filtering operation can be performed in 256 clock cycles. Fabricated using a 1.25-μm double-metal, single-polysilicon CMOS process, the 155,000-transistor chip contains a 16-by-16-bit multiplier, a 62-by-52-bit control ROM, dual 4-K data-RAM arrays, a 15-word-by-35-bit programmable delay circuit, and miscellaneous adders, registers, and multiplexers.

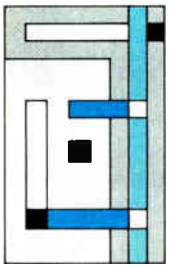
Hitachi Ltd. is taking aim at multiprocessing applications with its 50-ns DSP chip with a 145-command instruction set (see fig. 8). A single DSP chip from the Tokyo company is capable of performing transversal-filter computations at a rate of 50 ns per tap, a 512-point complex FFT in 1.5 ms, and spatial-filter operations at a rate of 600 ns per pixel. Any array of up to 64 by 64 of the Hitachi chips can be connected into a multiprocessor configuration using a host CPU interface. In such a configuration, processing commands can be directed to either individual processors or to rows or columns in the array.

Fabricated using a 1.3-μm double-metal, single-polysilicon CMOS process, the 430,000-transistor chip contains a 32-bit ALU with eight 16-bit accumulators, a 16-by-16-bit multiplier, 48-K of internal memory, a barrel shifter, and a parallel I/O interface for communications with a host CPU in multiprocessor applications.



8. FOR DSP ARRAYS. Hitachi has developed a 430,000-transistor digital signal processor that can be used in powerful multiprocessing arrays of up to 64 by 64 chips.

U.S. IS STILL KING OF THE ANALOG HILL



The one area of technology where U.S. companies still hold an undisputed edge is analog circuit design. Only eight of the papers on analog technology scheduled for this year's ISSCC were Japanese. Sixteen of the papers were from the U.S.

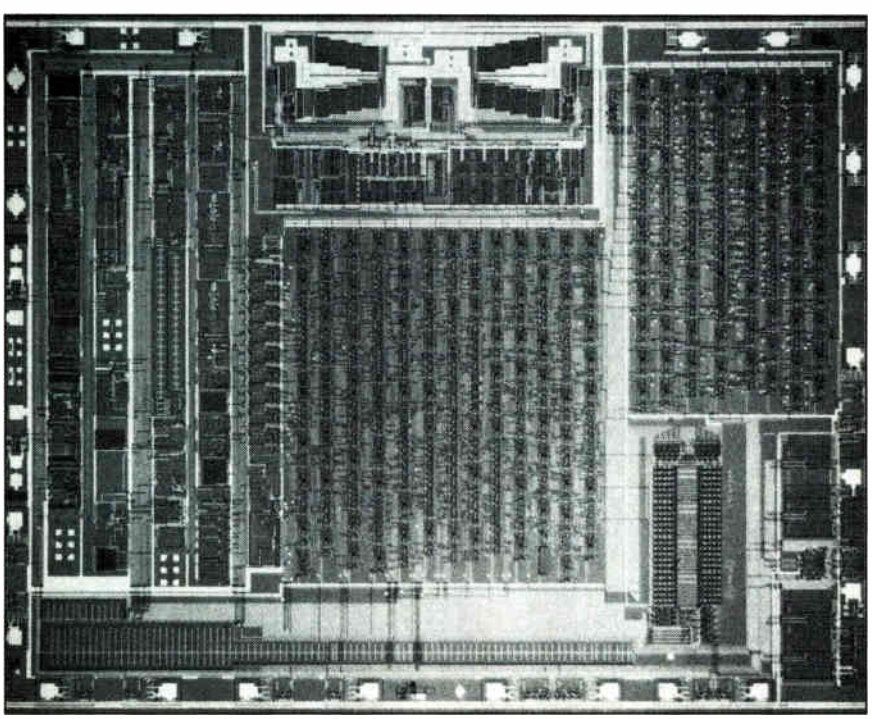
Among the analog highlights was an AT&T Bell Laboratories' gigahertz automatic-gain-control amplifier that outperforms bipolar and gallium arsenide devices. Other conference standouts included a CMOS line interface for T1 terminals that is as fast as bipolar interface chips, from Crystal Semiconductor; a switched-capacitor bipolar voltage converter with world-beating performance, from Linear Technology; and an algorithm-based self-calibrating eight-channel analog-to-digital interface processor, from Microlinear.

Using a 0.75-μm n-MOS process, researchers at AT&T Bell Laboratories, Murray Hill, N. J., have succeeded in building a single-chip agc amp that is competitive with bipolar and GaAs implementations in some respects and superior in others. Automatic gain control is a key element in the design of fiber-optic receivers, which must handle wide variations in input optical power. Because of the combination of high bandwidth, low noise, and high gain with a wide dynamic range needed to handle these variations, bipolar silicon and GaAs have been the preferred solutions. But the AT&T device has a bandwidth in the 1.0-to-1.5-GHz range, equivalent to bipolar and GaAs implementations. What's more, its dynamic range is 70 dB, almost three times better than bipolar implementations and almost seven times the performance of GaAs devices. Moreover, power dissipation is only 250 mW, one fourth that of bipolar and one tenth that of GaAs equivalents.

Also invading a traditional bipolar domain, designers at Crystal Semiconductor Corp. of Austin, Texas, have developed a monolithic 3-μm CMOS line interface for T1 digital communications terminals (see fig. 9). Incorporating a phase-locked loop, a controlled-slew switched-capacitor digital-to-analog converter, a read-only memory for storage of coefficients, a bandgap reference, crystal-controlled time base, and peak-detection and comparator circuitry, the device can drive a 25-Ω equivalent load with a 10-MHz cutoff frequency. That's performance equal to bipolar implementations.

From Linear Technology Corp., Milpitas, Calif., comes a bipolar voltage converter circuit with a 100-mA output capability over a 3.5-to-15-V range, a tenfold improvement over current designs. Moreover, voltage losses are a tenth that of other designs, about 1.2 V at 100 mA over the 3.5-to-15-V range versus about 1 V of loss at 10 mA and 5 V. The key to this performance is switched-capacitor networks, a technique usually associated with CMOS, rather than bipolar, technology. It hasn't been used with bipolar transistors because bipolar switched-capacitor circuits suffer problems traceable to emitter-base breakdown and the poor current-handling capabilities of lateral pnp devices. To overcome these problems, Linear Technology has developed a new bipolar process with an implanted-base transistor to achieve 15-V operation with emitter-base breakdowns in the 25-V range.

Finally, from Microlinear Corp., San Jose, Calif., comes a radical departure in the design of self-calibrating analog-to-digital converters. The design uses an algorithmic technique rather than the traditional switched, or weighted-capacitor, technique to achieve 13-bit integral linearity with a conversion time of 25 μs. The algorithmic approach was chosen because it requires 25% to 40% less area. So Microlinear had room to incorporate a processor-like architecture in which most system attributes are reconfigurable under the control of an on-board programmable sequencer. All this has been fit on the chip despite the use of a relatively conservative 3-μm CMOS process. □



9. SAVED BY CMOS. Crystal Semiconductor's interface chip for T1 digital communications terminals brings power-saving CMOS technology to an application dominated by bipolar parts.

This announcement appears as a matter of record only.

February 11, 1987

$1,175,000,000

Limited Partnership Interests

Warburg, Pincus Capital Company, L.P.

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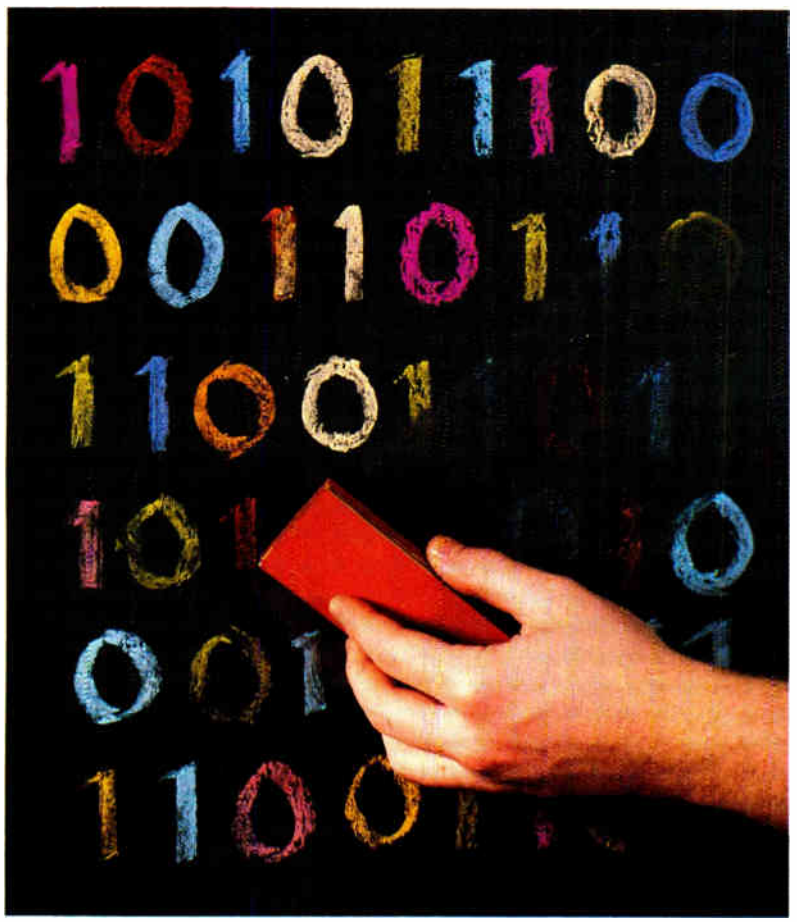
ERASES IN A FLASH.



Combining the fast programming techniques of EPROMs with the erasure mechanism of EEPROMs results in a high-density device with the best of each.

How Seeq is pushing EEPROMs to 1-Mb densities.

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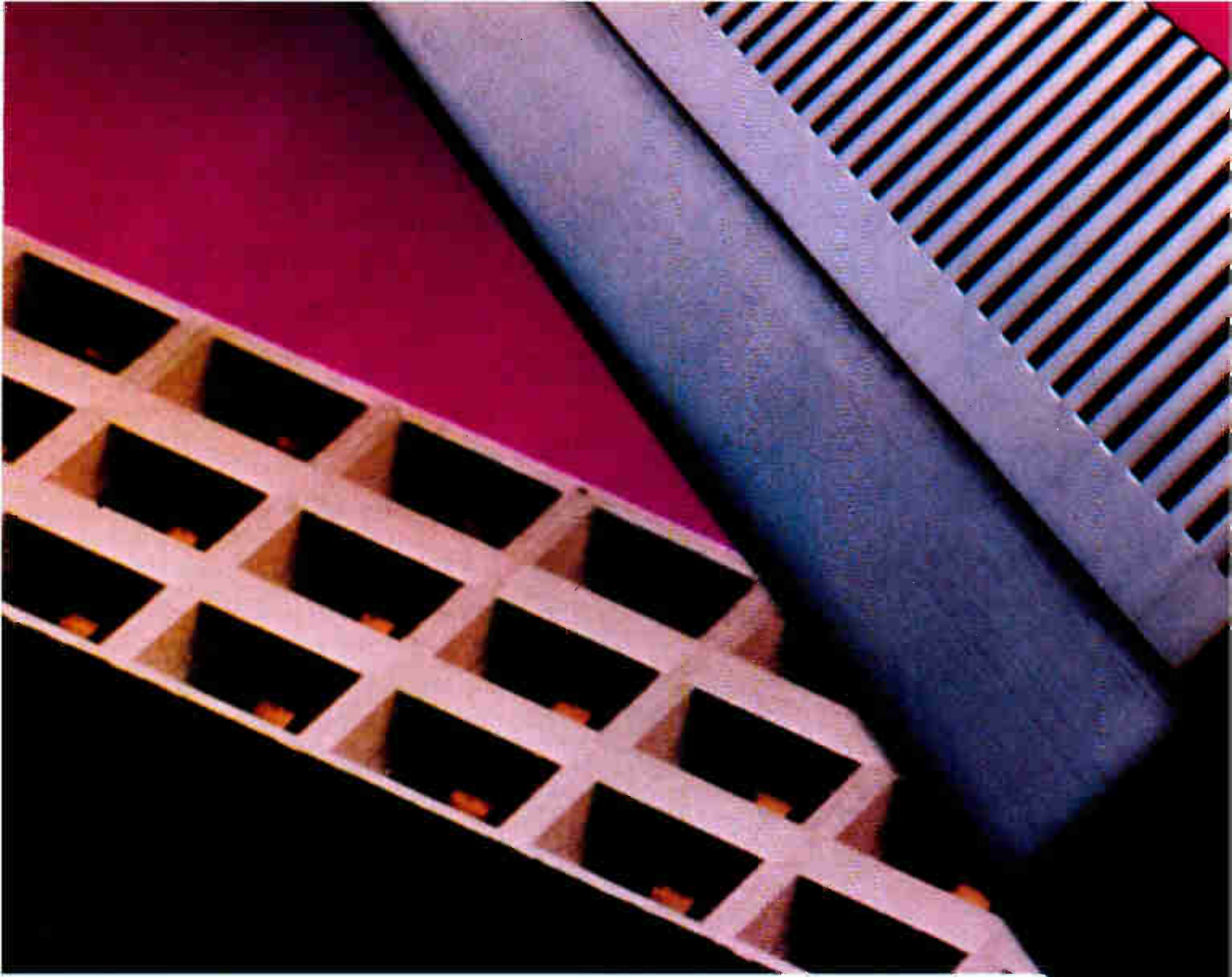
Excerpted from an exclusive article in the August 21, 1986 issue.

McGraw-Hill Electronics

THE LEADER IN NEW TECHNOLOGY COVERAGE



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A new strategy speeds up expert systems into the mainstream.

"A long-time leader in expert-system tools is answering the call for easier-to-use development aids. Inference Corp. is extending the reach of its ART automated reasoning tool beyond the Lisp programming language.

ART non-Lisp 3.0, written in C, brings Inference's AI technology to mainstream computing hardware—the VAX minicomputers and Sun-3 work stations, with forthcoming release planned for the IBM RT Personal Computer and Apollo hardware. ART Lisp 3.0 brings Inference's enhancements to developers working on standard Lisp hardware—the Symbolics 3600 series, Texas Instruments Explorer, and LMI Lambda Lisp machines, as well as on VAX and Sun-3 equipment..."

Excerpted from an exclusive article in the August 7, 1986 issue.

McGraw Hill **Electronics**

THE LEADER IN NEW TECHNOLOGY COVERAGE

VECTOR PROCESSING COMES TO THE DESKTOP

Sky Computers fits a 64-bit vector accelerator onto a board that plugs into one slot on an IBM PC AT; the $10,000 unit competes with $1,000,000 minisupers

by Tom Manuel

When the personal computer first ushered in desktop computing a few short years ago, no one expected supercomputer performance at that level any time soon. But now supercomputer power on a desk is at hand, thanks to what can now be packed onto a single board of very large-scale integrated circuits. Sky Computers Inc. is launching the 64-bit Vortex vector accelerator that it claims will let personal computers and work stations hold their own against minisupercomputers costing up to $1,000,000.

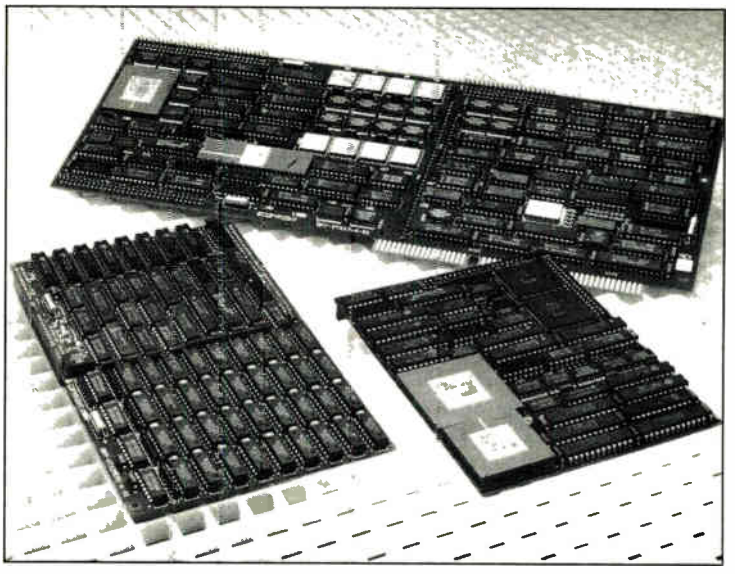
For around $10,000, a Vortex system occupying a single slot in an IBM Personal Computer AT (see figure) turns it into a vector processor. And this dramatic improvement in price/performance for numerically-intensive computing is not restricted to PCs. The Lowell, Mass., company is making versions available for Multibus II, VMEbus, and NuBus 32-bit computer systems and technical work stations, as well as planning custom versions for some work station vendors.

By adding one or more Vortex boards, builders of these products now can offer floating-point performance of tens of megaflops. Such performance matches that of small minisupercomputers and meets a growing demand by users of work stations and microcomputers for high-speed numerical processing. The AT, Multibus II, and NuBus versions are available now; the VMEbus version will be available in the fourth quarter.

The key to the board's performance is its vector-processing capability, a technique for parallel operations on matrices of numbers. Vortex is rated at 20 million 32-bit single-precision operations/s and 10 million 64-bit double-precision floating-point operations/s. To achieve these rates, the designers used both off-the-shelf and custom ICs.

The latest in high-density packaging such as surface-mount technology and daughterboards helps squeeze the circuitry onto a multiboard module requiring a single slot. Software technology is also an important part of the Vortex product in the form of a vectorizer, a preprocessor for source-code programs that finds vectorizable code sequences and converts them into vector form before the program is compiled.

The Vortex board is implemented with multiple computational ICs, a combination of fast and slow memories, and an 80-megabyte/s internal bus. The architecture is a block structure with five major blocks tied together with the 80-megabyte/s bus. The blocks are a system bus interface, program memory, control processor, data



VECTOR PC. A motherboard and two daughterboards form the Vortex vector processor, which plugs into one slot of an IBM PC AT or equivalent.

memory, and the heart of the machine, the vector arithmetic unit.

Included in the vector arithmetic unit are Analog Devices' 10-MHz AD3210 and AD3220 floating-point adder and multiplier chips; a Wafer Scale WS5903 32-bit register, arithmetic, and logic unit; the AD1401 sequencer chip; and a custom VLSI pipeline register and buffer chip developed by Sky Computers.

Supporting the vector arithmetic unit is a dual-speed data memory. By putting 1 megabyte or more of memory on the accelerator board and mapping it into the main memory of the host, the designers have made the delivery of data to and from the ALU fast and simple.

The data memory combines 80-megabyte/s static random-access memories and 40-megabyte/s dynamic RAM chips in order to get the highest speed at the lowest cost. The fast memory is used when data must flow into and out of the vector arithmetic unit as fast as possible. The lower-cost, slower memory bank is used where memory speed is not so critical, such as transferring data to the system bus interface.

The Vortex board includes a program memory and control processor to handle the extensive vector processing microcode developed for this machine. CMOS technology is used throughout to keep the board's power requirements low.

Putting so much capability into a board module capable of fitting in a single slot required innovative packaging as well as high-density, low-power ICs. The Vortex designers turned to state-of-the-art surface-mount technology and a daughterboard configuration to squeeze everything in.

The Vortex system is packed on one motherboard and two daughterboards for the PC AT version of Vortex. The current version uses 256-K DRAM and SRAM chips for a total of 1 megabyte of data memory. Future versions of Vortex will employ 1-Mb chips and will offer up to 8 megabytes of on-board memory. Surface mounting these dense memory ICs compactly on daughterboards will let Sky Computers continue to offer large data memory on the accelerator, yet keep it a single-slot product.

To achieve the highest possible performance, Sky Computers opted for vectorized code to accompany the vectorized data. It also opted for automatic vectorization so that Vortex will automatically examine nonvectorized programs and decide which operations are to be sent to the vector processor and then will generate code using the vector commands. Only a handful of big supercomputers and minisupercomputers have offered automatic vectorization in the past.

The Sky Computers team developed a preprocessor to convert vectorizable code in programs to source code that can be handled by standard compilers. The vectorizing preprocessor, called VEX, lets the Vortex accelerator address entire computing problems, handling both vector and scalar computations as efficiently as possible.

The initial version of VEX converts standard Fortran 77 language programs to vectorized source code. It makes it possible to take a program written in standard Fortran, convert it automatically, and then compile it with a standard Fortran compiler. A vectorizer preprocessor for the C language will be available later, say the developers. Eventually, the company plans to develop full-blown vectorizing compilers. □

TURNING A MODEST START INTO A BREAKTHROUGH DEVELOPMENT

When the designers at Sky Computers Inc. sat down in the summer of 1985 to design a new product, they didn't have the Vortex system in mind. "We set out to build an extension of our existing product line [board-level array processors for microcomputers]—to build a smart array processor," says Gerald Shapiro, 45, president, founder, and chief technical officer.

But then the designers at the seven-year-old Lowell, Mass., company decided to add vector processing and to make it easy to use with a vectorizing preprocessor. They also decided to include enough memory so that the management of the high volume of data could be handled on the board itself. So what the close-knit development team of nine engineers came up with was a breakthrough in high-performance numerical computation for low-end computers.

A leading team member was Michael Alperovich, 37, manager of systems and tools, who was responsible for directing the software design. "One of the key goals was to build software to make the product very easy to use," says Alperovich. "The VEX preprocessor was a very important part of this goal." The software designers recognized that beyond providing a standard array-processor library and hardware capable of doing vector calculations, they had to come up with some way of helping users convert programs into vector form. The VEX automatic vectorizer was the answer.

Another goal was to build a facility that could be extended or be capable of emulating existing instruction sets. This led to a microcode-intensive design. Enter another key member of the development team: Charles Valentine, 50, manager of microcode development. Valentine coordinated the overall design of the microcode and was deeply involved in the detailed coding of the vector routines.

"The biggest challenge was to work ahead of the hardware. Since the hardware was being developed concurrently with the microcode, a lot of code had to be written before it could be tested," says Valentine. "That worked out very well." One important reason, he says, was the close working relationship possible with the small team.


ALPEROVICH


SHAPIRO


VALENTINE

AN EASIER WAY TO BUILD A REAL-TIME EXPERT SYSTEM

Gensysm's G2 development tool provides applications developers with a framework with which to build a knowledge base, rules, and an inference engine

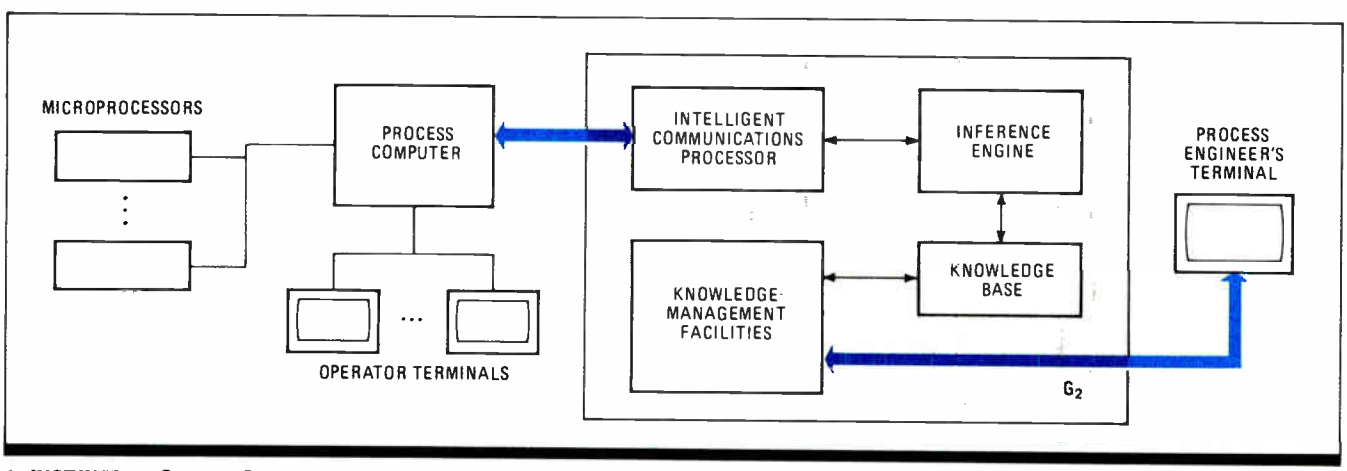
by Alexander Wolfe

Designing expert systems that monitor complex real-time functions in factory, financial-transaction, and communications applications is about to become easier. Gensym Corp., a tiny Cambridge, Mass., startup formed less than a year ago, has devised the Gensym Real-Time Expert System, a versatile framework on which applications developers can construct their expert systems.

Also called G2, the Gensym tool "is the first real-time expert system that allows you to use sophisticated knowledge models," says Robert L. Moore, Gensym's president. For example, it helps users create a comprehensive, detailed knowledge base for a real-time process, and it provides an easy-to-use method of creating the rules that govern expert-systems operation. Also, it supplies an inference engine that can focus on the set of rules it needs to solve a particular problem.

With the G2 framework, developers can build real-time expert systems more complex than those possible with existing tools such as Picon from Lisp Machines Inc. The fastest growth in expert systems likely will come from real-time applications, which are expected to take over a third of the market. They will serve applications in computer-integrated manufacturing, financial-market trading, robotics, and automatic testing. Process control on the factory floor will also be a large market. The chemical, petroleum, glass, rubber, and food industries will increasingly look to expert systems to run their factories.

G2, written in the popular artificial-intelligence programming language Common Lisp, will run on Symbolics 3620 hardware, Texas Instruments Explorer and Sun Microsystems Sun III work stations, the Hewlett-Packard 9000 series, and IBM's



1. JUST IN TIME. Gensym Corp.'s Real-Time Expert System, or G2, provides a framework for knowledge-management facilities, a knowledge base, and an inference engine on which applications developers can build real-time expert systems aimed at process-control applications.

Personal Computer AT and compatible systems. "And we have the first powerful expert system with graphics to be fully supported on Digital Equipment Corp. [VAX] hardware," says Moore. G2 is available now, with prices ranging from $10,000 to $60,000, depending on configuration and quantity.

The analysis of plant data and the formulation of control instructions is the complex job of the real-time expert system built around G2. That system comprises a knowledge base, knowledge management facilities, and an inference engine.

G2 is easier to use because its rules are written in a language similar to English, and it has an icon-based graphical interface to create knowledge frames

An expert system using G2 will hook up to the main process computer that monitors plant operation (see fig. 1). The process computer will send its data, including any warning of problems in plant processes, to G2. In turn, G2 will analyze the data and send control instructions to the process computer. The hardware interface between the process computer and G2 is handled by G2's Intelligent Communication Processor module.

Because it is aimed at a number of wide-ranging real-time applications, G2 creates knowledge bases that represent time. "This whole structure is missing in conventional expert systems," says Moore. The knowledge base acts as a store of all information on a process or plant's operation.

A knowledge base consists of facts and rules for using them. In a real-time G2 knowledge base, timing information is also included. A G2 knowledge base is made up of knowledge frames created using its knowledge-management facilities. Knowledge frames (see fig. 2) contain text describing a rule or rules to be executed by the expert system's inference engine. The knowledge frame must also contain information on the attributes of items referenced in those rules. Because of its focus on timing, a real-time expert system will explicitly represent much of a process flow. "If you need to express a sequence of actions to be done over time depending on various conditions, then you have to write a sequential block," says Lowell Hawkinson, Gensym chairman and chief executive officer. But much of a process's timing remains implicit.

Implicit timing information contained within the knowledge base includes items such as the validity interval. "Every piece of data is stamped with the time at which its validity will expire. Everything has an expiration time, and those expiration times are based on when the data from which they were derived was extracted, plus certain time attributes attached to those sources. For example, a temperature reading is valid for a minute, whereas a pressure reading might be only accurate for 3 seconds," Hawkinson says.

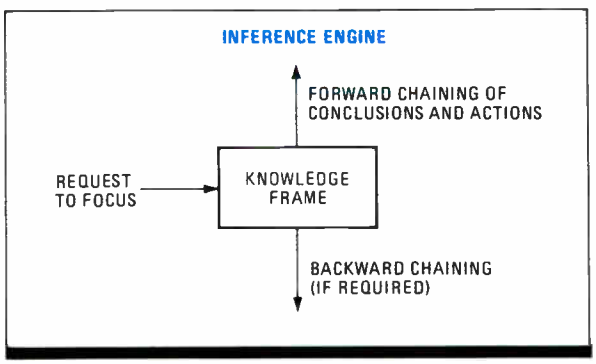
Another of G2's advantages is that it is easy to use. Its rules and associated information that fill a knowledge frame are written in a language similar to English, whereas most expert systems rely on Lisp. Because schematics are entered and edited in a high-level language, "to use our tool, not only need you not be a Lisp programmer, you needn't be a programmer at all," Hawkinson says.

To create knowledge frames, users work with G2's icon-based graphical interface, which uses the concept popularized by Apple's Macintosh. G2 users create procedures, or blocks of knowledge frames, and enter them via the system's graphical interface. The inference engine invokes a procedure—a series of steps to perform an action—when certain conditions are met. "By allowing knowledge to be organized in blocks and to be keyed to events or time duration, it's possible to handle phases of [plant] operations in a very convenient way," Moore says.

Users manipulate the icons to create individual procedures and to string together sequences of different procedures, which creates a schematic diagram of the process the expert system will be monitoring. "Schematics and procedures are entered in flow-chart form," says Hawkinson. "Just as you would enter a schematic graphically with a CAD package, you can also enter a procedure graphically, placing various kinds of flow-chart boxes on the screen and connecting them."

RULE	If P1015 > 14.7 lb/in.^{2} and if P1015 rate of increase per minute over 2 mins. > 1, then conclude 'Tower Flooding Impending' and invoke rules with condition 'Tower Flooding'
OBJECTS	Feed to column B_2
CONDITIONS	Feed composition disturbance
CREATOR	J. Smith
LAST CHANGE	10/17 2:30 pm
INFERENCE	Invoke on focus
SCAN	15 s
PRIORITY	1

2. FRAMED. A knowledge frame contains text describing rules to be executed by G2's inference engine. These frames makes up a knowledge base.



3. TOOLS. G2's inference engine uses focusing and forward and backward chaining to execute the rules in a knowledge frame.

To execute the rules contained within the knowledge frames, an expert system uses an inference engine. Here, too, G2 takes a novel approach. Conventional expert systems search through all their rules, looking for those that are ready to fire. After those rules are executed, the searching process begins again and repeats until no unexecuted rules remain. But searching through hundreds of rules each pass is laborious, much like running through an entire alphabetical list to access names beginning with 'z.' "That's not the way the human mind works," says Moore. "The human mind invokes knowledge that's appropriate to the problem at hand." And so does G2. Using a technique called focusing, G2 pares down the list of rules before it starts a search. Therefore, the search is focused on a small group of likely candidates. Moore and Hawkinson liken this to a driver's peripheral vision.

In addition to focusing, the inference engine uses forward chaining and backward chaining (see fig. 3). "The structure here is totally oriented around our real-time operating system written in Common Lisp. The concept is that a chunk of knowledge—a knowledge frame—can be invoked [by the inference engine] by a number of different methods. It may be invoked by backward chaining, in which case some higher-level test has been requested," Moore says. "For example, is a certain condition true? Or it may be invoked by forward chaining; that is, some data change in the plant may cause invocation. When this knowledge frame is invoked, if it has current values for these antecedents, it reaches its conclusion immediately."

For users intent on building ever-larger real-time expert systems, G2 includes facilities for handling distributed intelligence. As a result, multiple expert systems can be combined. "You can have inferencing done on a global basis, and you can have interconnected expert systems, with local expert systems controlling local parts of a process and global expert systems controlling the overall plant," Moore says. G2 also comes with simulation tools, for debugging systems under development. "If you have a large problem and you want to test it, you can't just go to the plant because you might have to wait for a specific piece of equipment to fail in a certain way," explains Moore. The simulation can replicate those failures, so users can be sure the knowledge base and rules have been properly set up to handle the real-world failure. □

G2's inference engine can pare down the hundreds of rules in a knowledge base to focus on a small group of likely candidates for the task it is tackling

IS THE REAL-TIME MARKET A GOLD MINE? GENSYM IS BETTING ON IT

Last September, the team that led the development of the first real-time expert system decided to strike out on its own. So Robert L. Moore and Lowell B. Hawkinson left Lisp Machines Inc., the company where they had developed that system, called Picon. With four Lisp Machines colleagues—Michael Levin, Brian L. Matthews, Andreas Hofman, and Mark H. David—they pooled their money and founded Gensym Corp.

With its launch product, G2, the Cambridge, Mass., startup intends to pave the way for expert systems in the potentially lucrative real-time arena. "We feel ultimately that a third of all expert systems will be classified as real time," says Moore. By drawing on their experience in real-time process control, Moore and Hawkinson believe they can generate $60 million in annual revenues for Gensym by 1990.

Moore, president of Gensym, recognized the possibilities of real-time and process control long ago. He began his career in 1966 at Foxboro Corp., working on computer control techniques. In 1971, he earned a Ph.D. in electrical engineering from Massachusetts Institute of Technology. He then became director of engineering of Gould Inc.'s Measurement Systems Division in 1979 and president of Sentrol Systems Ltd.'s U. S. subsidiary in 1981. In June 1983, Moore founded AI Systems Ltd., which merged into Lisp Machines, where Moore was a vice president.

Hawkinson, Gensym chairman and chief executive officer, has been involved in the development of sophisticated software systems since his days as an undergraduate at Yale University in the early 1960s. After stints in industry, he joined MIT's Laboratory for Computer Science in 1973 as a research associate, working on a variety of AI-related projects, including a knowledge representation system called XLMS. Hawkinson hooked up with Moore at Lisp Machines, which he joined in late 1983 as manager of expert systems development of the Process Systems Division.

Now he is planning for expansion. "The biggest challenge is adding a group of people who can help us bring this technology to the markets," says Hawkinson. Gensym's staff totals nine. "A year from now I expect we will have 25 to 30 people, and that's a conservative estimate."

The company is already setting its sights on the big four of the expert systems marketplace—Intellicorp, Inference, Teknowledge, and Carnegie Group. "We may have to grow a little faster than projected to be as significant as those companies, but I think the impact of our technology and our product will put us up there," Hawkinson says.

THE CORE. Robert L. Moore, left, Gensym president; and Lowell B. Hawkinson, chairman and CEO.

MOVING WAFER INSPECTION INTO THE FAST LANE

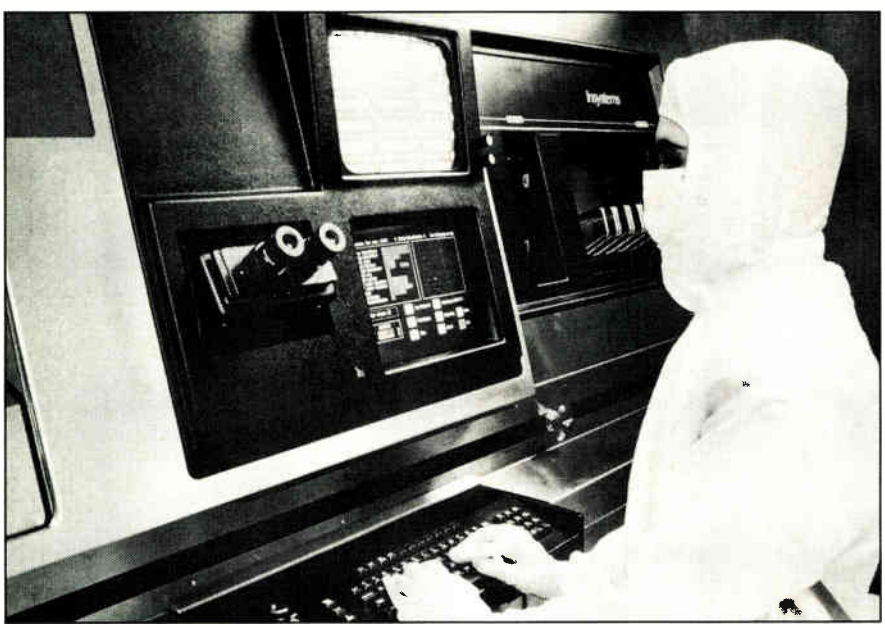
Insystems' unique inspector uses optical signal processing and holography to detect any defects in a patterned wafer in less than 30 minutes—and with far more accuracy

Jerry Lyman

Holography and optical signal processing may seem far removed from the world of integrated-circuit processing, but Insystems Inc. is using these technologies in a radically different wafer-inspection machine that's both faster and more accurate than conventional machines. The San Jose, Calif., company's fully automated model 8600 (see fig. 1) inspects an in-process patterned wafer in less than 30 minutes, versus the several hours required for inspection using conventional optical or scanning-electron-microscope equipment. And in comparative tests at Insystem, the machine found four times the number of wafer defects that an operator using conventional equipment was able to detect.

This level of performance will be essential to achieving acceptable yield in the coming generation of submicron superchips. It will be especially effective in detecting process-induced wafer defects, which undoubtedly will multiply as geometries continue to scale down.

The key to the 8600's performance is the use of parallel optical processing. For one thing, the 8600 can inspect the entire surface of a wafer at once, whereas other machines must check each chip on a wafer one by one. For another thing, by means of optical signal processing, a high-resolution three-dimensional hologram that shows only a wafer's defects is produced. The defects can be viewed by an operator on a display screen, using the 8600's built-in video camera, while the wafer is also viewed under a conventional optical microscope. A second display screen shows a defect map of the wafer under inspection.



1. DEFECT DETECTION. Insystems' model 8600 uses holographic optical processing to display and map an in-process wafer's defects in one operation.

The company has already built a prototype and the first production unit, which will cost around $1 million. A machine will be shown at Semicon West in San Mateo, Calif., May 18-21, and Insystems will demonstrate another unit at their San Jose facility.

Within the 8600, an argon ion laser serves as a coherent light source to illuminate an in-process wafer. The IC pattern thus produced undergoes a two-dimensional Fourier transform through a special lens, yielding its spatial-frequency spectrum, which for most defective wafers does not overlap much with the defects. This spectrum is used to expose a photo-

graphic plate; when exposed, it serves as an optical filter.

Using the same lens, an image of the wafer, including the defects, is passed through the filter, and the defects, along with a coherent reference beam, are recorded in a hologram on a second photographic plate. By means of conjugate wavefront reconstruction and a reverse Fourier transform through the lens, the defects then are projected as a high-resolution hologram in the original wafer plane.

There are three major steps in Insystems' process: creating a filter, recording a hologram of the wafer defects, and creating a holographic image that is scanned by a video camera. In the first step, an in-process wafer is used as the basis for creating the filter.

First, the laser's output is separated into two beams by a variable beam splitter. One beam is used as a reference beam, and the other is used for filter development. The filter-development beam is directed through a beam expander to a mirror, which then directs it to a second beam splitter, near the wafer. The reflected image of the wafer is then sent through a special lens that forms a two-dimensional Fourier transform of the image on a photoemulsion plate in the back focal plane of the lens (see fig. 2a). This plate is developed in about 5 minutes and reinserted to its former position.

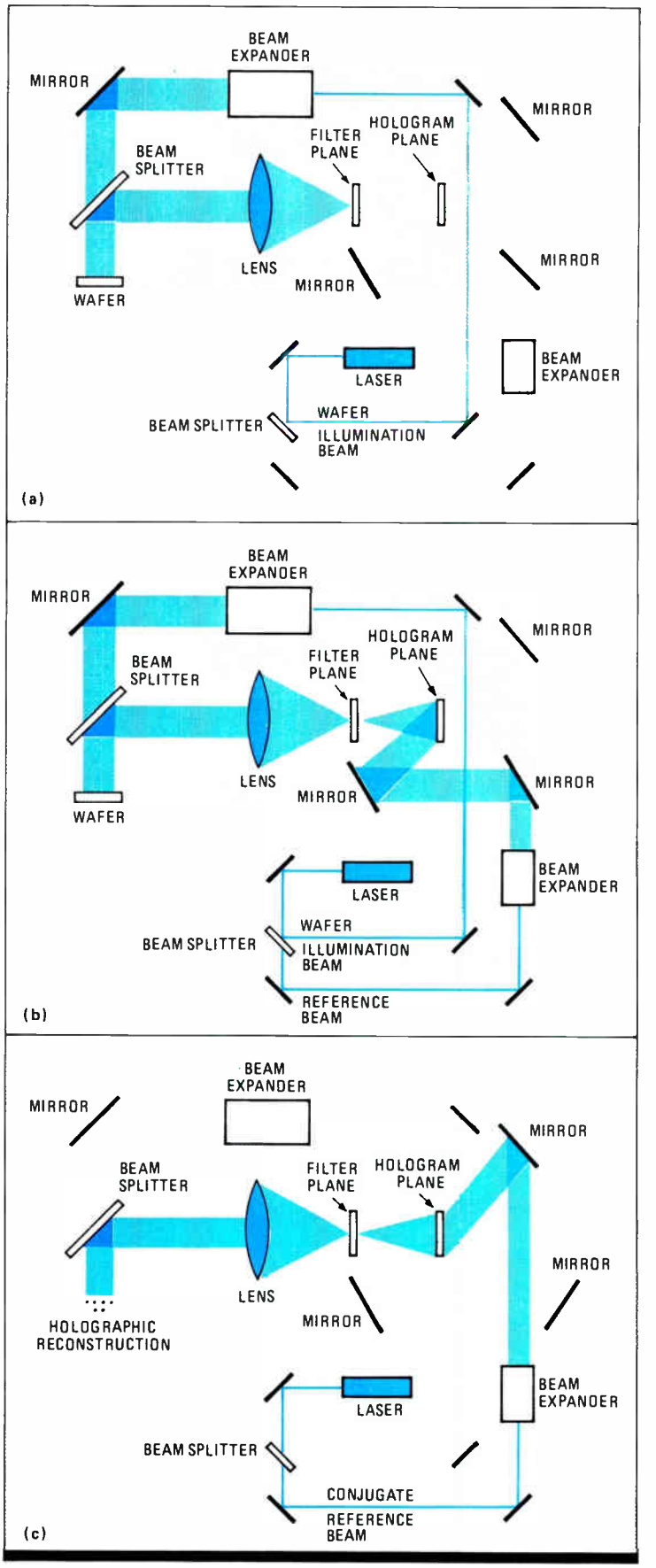
The next step is to generate a hologram. Downstream of the filter plane another photographic plate is inserted and is exposed simultaneously to both the light transmitted through the filter and the collimated reference beam (the second output of the laser's beam splitter in fig. 2b), forming a hologram on the plate. After this plate is developed, it is returned to its original position.

Once the Fourier transform filter and hologram are generated and are in place, the defect-detection process begins. The wafer-illumination beam is shut off, and the wafer is relocated under a conventional built-in optical microscope. At the same time, a scanning video camera is brought into position to view the real holographic image that will be formed in the original wafer plane.

MAKING A HIGH-QUALITY IMAGE

The next step is conjugate wavefront reconstruction, or reverse ray-tracing. The hologram is illuminated by the conjugate to the original reference beam (another collimated beam propagating in a direction opposite to the original reference beam—see fig. 2c). The wavefront reconstructed from the hologram is now also conjugate to the original light wave transmitted through the filter and the lens. The light diffracted from the hologram therefore exactly reverse-traces the original light from the image of the defects, through the filter and lens.

By this process, a real holographic image of the defects is formed at the exact location of the



2. ON THE BEAM. Holographic processing has three steps: making a filter (a), making a hologram (b), and creating a holographic image (c).

original wafer plane. This image is of very high quality, since any aberration or distortion of the wavefront between the wafer and hologram caused by the lens or filter in the path is exactly canceled by the process of reverse ray-tracing through the same refractive elements.

Next, the holographic image of the wafer defects is scanned with a CCD video camera, and this data is used to display a high-resolution picture of the defects on the upper CRT screen. The same data is processed to automatically form a defect map of the wafer being inspected, which is then displayed on the lower screen. After the wafer defect map has been generated, the upper display may be used to show magnified images of the wafer patterns and defects using the system's built-in optical microscope. The microscope can be positioned automatically, or the operator can use a joystick.

TOUCH-SCREEN INPUT

A keyboard and a graphic video-display terminal provide the interface between the operator and the control computer. The graphic display has a touch-screen input for quick access. The control computer consists of a Motorola 68000-based central processing unit with 512-K bytes of memory and a 5-in. hard disk on which all operating software is stored. A 5-in. floppy-disk drive is used for adding software updates to the system and for archiving processed data from the system. A printer provides hard copies of defect reports, which indicate types, sizes, and locations of detected defects. Defect data can be output via a standard SECS II serial interface.

All of the 8600's subsystems—including the graphics-terminal interface, defect memory, camera interface, stage control, micropositioner control, optics and laser control, and the detector digitizer—communicate with the control computer via either a 16-bit or 8-bit data bus, depending on the data-transfer rate required. The controls for the mechanical and optical subsystems operate at slow data rates and therefore use the 8-bit bus. The defect-detection camera interface and memory, on the other hand, must acquire and assemble defect data at high speed, so it communicates with the CPU via the 16-bit bus.

The model 8600 can accept wafers as large as 150 mm in diameter and can be used to inspect silicon, gallium arsenide, and silicon-on-sapphire wafers. The machine can detect submicron defects in high-density, repetitive areas in single and multiple process levels containing photoresist; oxides of all types; polysilicon; metal; and other films, such as nitride, phosphosilicate glass, and polyimide. The data from the video camera allows full-wafer-mapping capability for characterization of defects induced by process equipment. Correlation of these defects on each process layer can then be reconciled with the electrical bit map to improve final yield. □

BUILDING ON A TECHNOLOGY THAT INSPECTS LARGE MIRRORS

When Chris C. Billat recognized there was a need for a system to accurately inspect wafers at all steps in their processing, he decided that holography and computerized optical processing could not only do the job, they could also move inspection procedures into the fast lane. So he founded Insystems in 1981 and went after the best holographic expertise he could find.

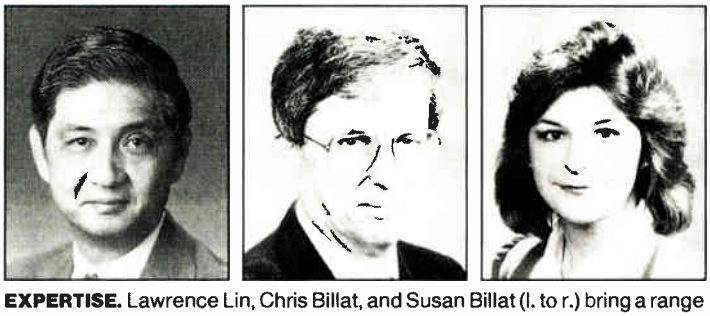
Billat, the former marketing director at Optometrix Corp., of Mountain View, Calif., where he gained valuable lithography experience, first had Insystems fund a program on holographic inspection in 1982 at the University of Dayton, Ohio. He'd heard about work being done at the University of Dayton Research Institute, also in Dayton, on applying holographic techniques and spatial filtering for the purpose of inspecting large curved mirrors for the Air Force. The program Billat funded produced three patents and a working breadboard that demonstrated mask and wafer inspection.

As the sole employee of Insystems at that time, Billat proceeded to secure financing by successfuly demonstrating the breadboard to prospective backers. He was also armed with a business plan he and his wife, Susan, former manager of the Microelectronics Group at Bechtel National Inc. in San Francisco, wrote during a Christmas vacation. Susan, an experienced process-line designer, was recently named Insystems' vice president of technology development; her husband is currently the company's director and chief executive officer.

In 1983 Billat hired his first employee: Lawrence L. Lin, an expert in holography who today is Insystems' vice president of engineering. While at Bell Labs in the late 1970s, Lin had engaged in pioneering research in optical holography. He has also co-authored a standard text in this field. With his extensive experience, Lin directed the effort that resulted in Insystem's first product, the model 8405 Automatic Photomask Inspection system.

Mask inspection was only a step along the way, Billat emphasizes. "The 8405 was really an interim product, and we always intended to focus on the much larger wafer-inspection field," he says. Lin's group was already hard at work on the model 8600, which uses a variation of the same basic holographic display format as the 8045, and finally was able to unleash it last September.

Using optical holography, Billat notes, "allows us to outperform conventional inspection systems in both speed and accuracy. Optical computer processing, rather than electronic processing, allows parallel processing of large amounts of data."



EXPERTISE. Lawrence Lin, Chris Billat, and Susan Billat (l. to r.) bring a range of skills to Insystems, including holography, lithography, and process design.

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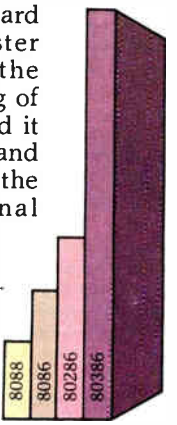

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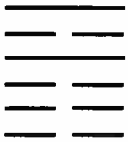

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THIS DISK-DRIVE CONTROLLER CHIP PLAYS IN ANY LEAGUE

AMD's RISC-based controller does what until now took a board full of parts to do: support all popular interface standards and drive four hard or floppy drives at a time

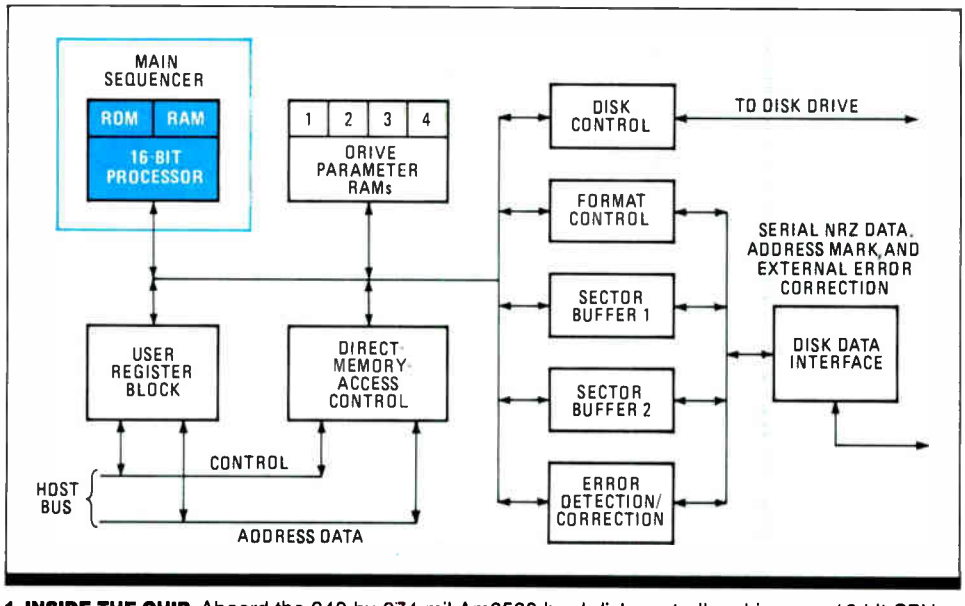
by Bernard C. Cole

An all-in-one disk-drive controller chip from Advanced Micro Devices Inc. resolves a long-standing contradiction facing computer systems designers: how to minimize the number of chips in the controller while maximizing access speed to today's ever-larger disks. The Sunnyvale, Calif., company's solution is a speedy single chip containing a 16-bit microcontroller built with a reduced-instruction-set-like architecture. The Am9590 controller supports several different disk-drive interface standards and can control four drives at once, including floppies. Until now, this kind of flexibility has required a board-level implementation.

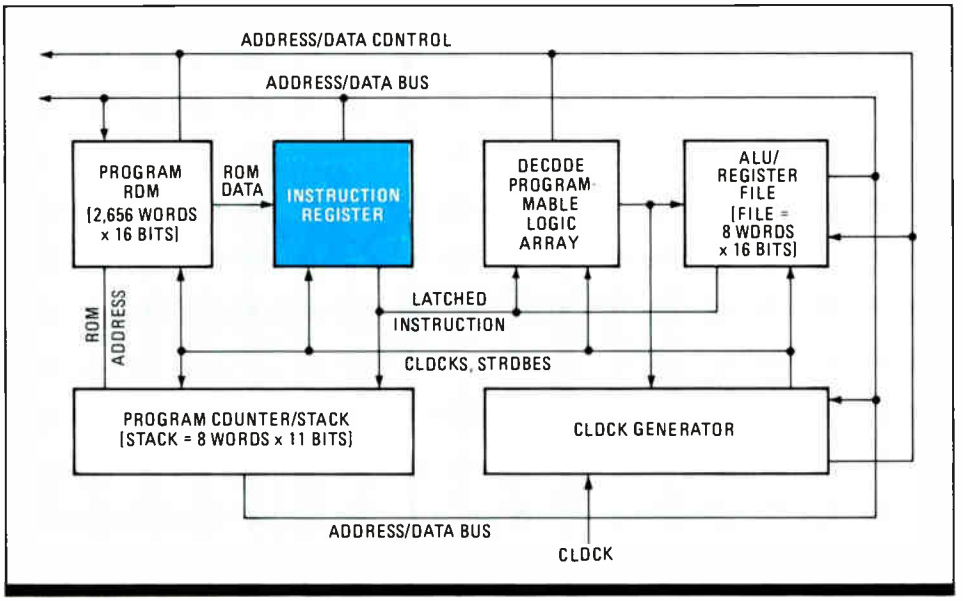
The Am9590's embedded microcontroller incorporates a set of 32 instructions that are optimized for disk-drive control, and it uses a proprietary protocol to perform complex disk-access operations at data rates as high as 15 Mb/s without requiring any intervention of the host computer. To further enhance speed and flexibility, the microcontroller works in conjunction with an on-chip direct-memory-access processor, a data formatter, and sector-buffering logic. In addition, the chip performs sophisticated error detection and correction using two versions of Reed-Solomon coding. The more powerful version can detect and correct double burst errors.

Using the capabilities of the microcontroller, the Am9590 not only supports several disk-drive interfaces, but can also control up to four disk drives, each of which can be independently user-programmable. It integrates the Enhanced Small Device interface, the ST506 and ST412 interfaces, and the Double Density Floppy Disk standard. With the addition of a small amount of external hardware, the Storage Module Drive interface can also be supported.

The Am9590 incorporates a serializer-deserializer to convert the parallel data stream of the host CPU into a serial data stream suitable for the disk drive; a data formatter, which arranges the data into sectors and adds all the necessary control information to each data block; error-detection and -correction logic, which generates certain redundancy bytes, when writing information to the disk, that are used to verify the



1. INSIDE THE CHIP. Aboard the 342-by-374-mil Am9590 hard-disk controller chip are a 16-bit CPU, a DMA processor, a format controller, and error-detection and -correction circuitry.



2. THE MICROCONTROLLER. The Am9590 contains an embedded RISC-like microcontroller with a 16-bit ALU, an 11-bit program counter, a dual-port register file, and 32 instructions.

data when it is read back; and head positioning and head selection of the disk drive. In addition, it has a main sequencer block that contains the proprietary 16-bit microcontroller. Also on the chip (see fig. 1) are the DMA controller, two 512-byte sector buffers, and 8 words by 16 bits of dual-ported static random-access memory for storage of drive parameters.

The heart of the design, and what gives the chip its speed and computational capability, is the microcontroller, which is based on a Harvard architecture and incorporates several elements of a RISC design, including: a small set of simple disk-control instructions; the execution of most instructions in a single clock cycle; and a minimum of instructions that involve external memory references. To further optimize performance, most of the 16-bit main-sequencer microcontroller is implemented with hard-wired control logic. Only a small programmable logic array is used to decode the control lines from the operating code.

The microcontroller, which includes a 16-bit full-function arithmetic logic unit, an 11-bit program counter with an 8-deep subroutine stack, an 8-word dual-port register file, and control logic to generate clocks and control lines (see fig. 2), contains 32 control instructions. All the instructions, except for one directing the microcontroller to return from a subroutine (RTS), execute in two clock phases—the equivalent of one clock cycle. And except for load and store operations, which are performed by the MOV instruction, none of the instructions refers to external memory. Each instruction word is 16 bits wide, with the opcode in the upper 5 bits. Although 2,048 instruction words are directly addressable by the main sequencer, the addition of paging logic to the on-chip ROM means that 2,656 words are actually addressed. As a result, nearly all the instructions execute in 400 ns or less with a 10-MHz clock. Exceptions are the MOV instructions, which reference external memory (in 500 ns), and the RTS instruction (800 ns). The microcontroller can perform, on the average, more than 2 million instructions/s, says Mohammad Maniar, Am9590 program manager.

Incorporated into the controller is a high-level data and command protocol, the basic unit of which is the input/output parameter block, providing the mechanism by which such operations as multisector disk I/O, marginal data recovery, diagnostics, and error recovery are performed. This mechanism allows commands to be linked so they can be executed sequentially by the chip without host intervention.

Under this protocol, the host CPU creates I/O parameter blocks in system memory to pass control and status information to the hard-disk controller. The controller fetches these blocks by using the on-chip DMA controller. Each I/O parameter block specifies one disk command and contains all parameters needed to execute it. After the block is executed, the hard-disk controller reports the status information and waits for further instructions. If an error occurs, the CPU can get detailed status information from the status-result block in memory.

As an option, I/O parameter blocks may be put together in a linked-list format, which the hard-disk controller can interpret sequentially. This offers a predefined and efficient structure for the operating system to handle the disk I/O. The ID field of the parameter block provides the linkage between a particular disk command and the user process that is making a disk request. The jobs can thus be placed in the controller's job queue and then ignored by the operating system unless an error occurs. All the information required to retrace an error is provided by the controller's status result block.

Since the controller manages the disk job queue, it can look ahead in the queue to overlap several time-consuming operations. Head movement, or seeking, can require a major portion of disk accesses. Since the controller controls up to four drives, it can perform an I/O-parameter-block operation on one drive while executing seeks for future blocks on the other drives. This eliminates the seek-time overhead when those subsequent block operations are executed.

According to Maniar, it is the on-chip DMA controller that gives the hard-disk controller the ability to execute complex disk I/O operations

without host CPU intervention. It fetches commands, writes status information, fetches data to be written on disk, and writes data that has been read from disk. DMA operation, he says, can be software-programmed to adjust the bus occupancy and data-bus width (8 or 16 bits). In addition, he adds, not only can a programmable number of software wait-states be inserted by the 16-bit main sequencer into the DMA bus cycle, but hardware wait-states can be incorporated as well. "This allows the user to tailor the hard-disk controller bus timing to the memory-access time of the system," he says.

Two sector buffers are also included on chip to eliminate a common constraint of most disk controllers: the need to "interleave" the sectors on the track, owing to the difference in speed of the host CPU bus and the disk's data-transfer rate. In the hard-disk controller, data is transferred to or from disk without this handicap, since the two sector buffers allow the DMA controller to transfer data between a sector buffer and system memory while data is being transferred between the other sector buffer and the disk. "Because zero-interleave operation is the natural state of the Am9590, the time necessary for read, write, and verify operations is automatically reduced two to six times over present controllers using interleaving," says Maniar.

The Am9590 goes far beyond current disk controllers in the range and sophistication of the on-board error-detection and -correction logic, Maniar claims. Most hard-disk implementations, he says, use the Fire code algorithms for detection and correction of disk burst errors, which are a common problem involving continuous inversion of bit values in the serial data stream. Instead of these more easily implementable algorithms, AMD designers used two types of the more advanced Reed-Solomon error-detection and -correction coding scheme. One version can detect double burst errors and correct single burst errors, and the other, more powerful version can both detect and correct double burst errors. To support floppy-disk drives, the Am9590 also incorporates the 16-bit cyclic-redundancy scheme, an industry standard for floppies. In addition, logic incorporated on the Am9590 allows a system designer to override all of these schemes to implement his own, Maniar says. □

A DESIGN APPROACH THAT COVERS ALL THE BASES

When development began more than two years ago on Advanced Micro Devices Inc.'s Am9590 disk controller chip, there was no way to predict which disk-drive interface protocols the computer industry would prefer, says Mohammad Maniar, program manager and design engineering manager for the new controller. So the Sunnyvale, Calif., company built a controller that would satisfy a variety of interface protocols.

"While it appears that the Enhanced Small Device Interface will be a popular interface for hard-disk controllers and will eventually dominate, the other protocols—both old and new—are not going away for a while," says Maniar, a graduate of the University of California at Berkeley in 1973 with both M. S. and B. S. degrees in electrical engineering. "Thus it only makes sense to design a controller that is flexible enough to work with a variety of formats and interfaces."

The fact that the interface and format protocol issue was, and still is, a "moving target" was a major reason the company decided to use a bus-oriented, microprocessor-based approach, Maniar says.

"The traditional random-logic approach to designing such circuits requires that the end use and interface specifications be reasonably well defined," says Maniar. "Modifying one aspect of a design using this approach usually requires modifications throughout the circuit." In the bus-oriented approach, however, each of the basic elements is designed as a semi-independent module that interacts with the other modules via a common bus. And when modifications are made to one module, there is little impact on the others—as long as each one satisfies the bus requirements. "Thus major changes can be made, and modules can be added or subtracted, without major impact on the overall design," Maniar says. All this, he explains, makes for a much more flexible design—one that better fits the requirements of the applications toward which the Am9590 is aimed.

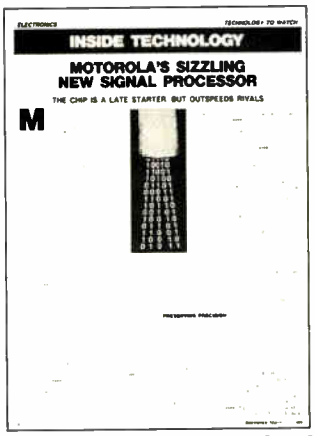
In addition, by taking the modular approach, once the internal bus was defined, the design of the chip could proceed in a much more parallel fashion. "In the more traditional approach, each of the elements in a design has a lot more hooks into other areas of the circuit, requiring that the design proceed much more sequentially," says Maniar. "In the bus-oriented approach, the design turnaround time is not the sum of the elements, but only that required for the most complex and difficult module."

A consequence of this approach, he points out, is that once the basic architecture has been implemented, the design of other types of controllers—such as for networking and any form of mass storage—can be accomplished by a modification of the instruction set and the addition of other modules more suited to those applications.

Working with Maniar are Allan Flippin, chief designer of the chip's microcontroller; Anil V. Godbole, senior design engineer responsible for the disk-control interface; Jochen Polster, senior applications engineer responsible for working with key customers in defining the product specifications; and James Reeves, software application engineer, who was responsible for developing the reduced-instruction-set-like instructions used in the microcontroller.

DEVELOPMENT TEAM. Godbole, Maniar, Flippin, Polster, and Reeves (l. to r.) built the Am9590 hard-disk controller.

UPDATE: MOTOROLA KEEPS TO REVISED DSP SCHEDULE



Motorola Inc., which altered its strategy for entering the digital signal processor market last fall [*Electronics*, Oct. 2, 1986, p. 100], is on schedule with its first DSP under the revised plan. The DSP56001, a random-access-memory-based version of its highly parallel 24-bit DSP design, will be available in sample quantities this month with a price tag of $500.

The strategy shift involved moving the 56001 ahead of the 24-bit read-only-memory-based 56000 that the company's Digital Signal Processor Operation in Austin, Texas, announced a year ago [*Electronics*, March 10, 1986, p. 30]. The decision to rearrange the schedule makes a great deal of marketing sense, say Motorola DSP product managers. They figure the RAM-based 56001 will start off faster in the marketplace, because it is better suited for low-volume shipments and system-design prototyping. Using the 56001, they say, customers can avoid costs normally associated with masked ROM.

Some market watchers maintain that jockeying the RAM-based 56001 ahead of the original 56000 has caused Motorola to slip behind its original shipment schedules. A year ago, Motorola's DSP managers indicated they hoped to have the 56000 in working order by the end of 1986, and today the ROM-based 56000 design still waits for its first production pass.

But Motorola executives say their DSPs aren't late, and the products seem to be moving full speed ahead now. "We cannot at this time find anything wrong with the 56001," says Bryant Wilder, manager of the company's Austin, Texas, DSP operation. The company already has working prototypes of the RAM-based 56001 chip, so when it does make that first pass on the 56000, the company doesn't anticipate many problems.

The 56000 closely resembles the 56001, except for having 2-K words of read-only memory in place of a program-RAM array of 512 by 24 bits. Both chips are based on the same 1.5-μm double-level-metal CMOS technology. Each is an 88-pin processor with the same architecture, containing four 24-bit parallel data buses and three concurrently operating execution units—an address arithmetic logic unit, a data ALU, and a program controller. The data ALU contains a 24-by-24-bit multiplier and a 56-bit accumulator that are designed to perform both math functions in one 97.5-ns machine cycle.

Perhaps more important, Motorola already has a built-in market for the new DSP chip, points out market analyst William I. Strauss of Forward Concepts in Tempe, Ariz. The 56000 architecture was developed by Motorola's Systems Research Laboratory at the Chicago Corporate Research and Development Center, he says, and the company's equipment-making operations intend to be among the early users of the 56000. By doing so, they should help bolster the chip maker's efforts to make the DSP a hit in the merchant chip markets.

All in all, analyst Strauss believes, Motorola remains well-positioned to grab sufficient market share in 1987 to stake out a claim in the crowded DSP markets. And the current leader in that market, Texas Instruments Inc., doesn't take Motorola lightly—one TI DSP product manager says he expects the 56000 to become a formidable competitor when it does start shipping. For now, though, the company has to play a waiting game.

"I don't know how to quantify design-ins until we get more material out there," Wilder says. "Everything we can determine—from the number of customer visits and requests—shows we will have a very good market share."

INQUIRIES ROLL IN

So far, Motorola says, it has received about 300 customer inquries through its DSP computer bulletin board, even though it spent most of 1986 without any working parts. It is selling 56000 development software for IBM Corp. Personal Computers, Digital Equipment Corp. VAX minicomputers, and Sun Microsystem Inc. work stations. The PC software package costs $295. Packages for multiuser VAXes and Sun work stations cost $3,000.

And Motorola already has sample quantities of a spinoff of the general-purpose 56000 architecture—the DSP56200, an algorithm-specific chip tailored for repetitive finite-sum-of-product math [*Electronics*, April 21, 1986, p. 21]. The 1.5-μm CMOS 56200 is being aimed at a range of DSP applications, including filtering, correlation, and transforms, says Garth Hillman, strategic applications manager. Motorola began offering samples of the 28-pin part in late 1986, as planned. Samples cost $100.

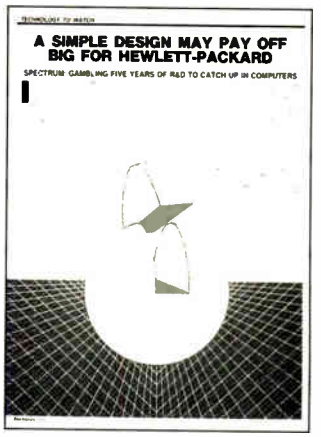
Some tweaks are now being made to the 56200 design, which is intended to perform multiplication, accumulation, and coefficient updates in a single 100-ns cycle. "In the late-1987 timeframe, we fully anticipate that we will have parts that have much faster cycle times than 100 ns," Wilder claims. "We already have parts that are much faster working in the lab." *–J. Robert Lineback*

UPDATE: HP'S SPECTRUM STICKS TO UPDATED PLAN

A year ago, Hewlett-Packard Co. introduced two new HP 3000 business computers, both based on a reduced-instruction-set-computer architecture. Some nine months later, the company had to delay shipping the first of the new machines, pushing back initial deliveries from the end of 1986 to spring of 1987. Today, the company says it is keeping to the revised schedule, and expects to make deliveries to beta-test sites this spring.

The new machines were the first fruits of HP's Spectrum project, a five-year effort to replace its three aging, incompatible computer architectures with a single architecture [*Electronics*, March 3, 1986, p. 39]. Those goals were met, the company says. However, problems developed in coordinating the data-management and data-base structures of the computers' operating system with the memory-mapped data handling of the new HP Precision Architecture. In September, HP postponed shipments of the first machine, the HP 3000 Model 930.

In January, Dean Morton, executive vice president and chief operating officer, said HP should deliver the first 930s this spring. The second machine, the Model 950, should ship, as originally planned, in the second half of this year. A third machine, the HP 9000 Model 840 technical computer, announced after the 3000 machines, began deliveries on schedule in November 1986.


A SIMPLE DESIGN MAY PAY OFF BIG FOR HEWLETT-PACKARD

SPECTRUM GAMBLING FIVE YEARS OF R&D TO CATCH UP IN COMPUTERS

The problems affecting the 930 are on their way to being solved. Michael Mahon, manager of HP's computer language laboratory, says "progress on the software for both the 930 and the 950 is proceeding on schedule." What remains to be done is the reintegration and testing of the complete system software.

Hardware has caused no problems, HP says. The company has made three Precision Architecture processors: a TTL version that runs the Model 840 and 930, and two very large-scale-integration versions. An n-MOS version is up and running in a Model 950 prototype. A 1.6-μm CMOS version is running, but no application for it has been announced.

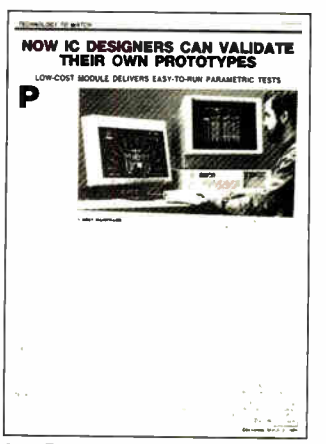
Overall, HP says it is pleased with the Spectrum results. "The first customers are very satisfied with the performance of the 840," says Mahon. "In fact, we underrated the peformance of the 840, our customers say." *–Tom Manuel*

UPDATE: A BANG-UP START FOR IMS DESIGN VERIFIER

Integrated Measurement Systems Inc. was hoping for a good market response when it introduced its design verification system [*Electronics*, March 10, 1986, p. 32], but the Beaverton, Ore., company got even more than it bargained for. "Since the Logic Master was introduced, we have shipped twice the number we projected," says Steve Palmquist, president of IMS. "One customer who made a special visit to the factory to get a demo of the system was so impressed he turned around a purchase order for about a third of a million dollars the following day, for a fully configured system." Following up the introduction of the original Logic Master, IMS has added ac capabilities to the product's dc functions, making it ideal for verifying large application-specific integrated circuits [*Electronics*, June 23, 1986, p. 39]. Now the company is bringing out a desktop version of the system.

ASIC verifiers measure the critical limits of a prototype chip before it is manufactured in volume. The designer can vary clock rates, supply voltages, or signal timing margins to determine the safe and maximum operating limits of a chip. The Logic Master 2000 can verify ASICs built with the latest sub-2-μm-geometry process technology.

"These new ASICs need higher pin counts and finer timing resolution," says Kenneth Lindsay, director of marketing. "Increasing the pin count is easy, but achieving a timing resolution of 100 ps and keeping the maximum skew across all pins to 1.5 ns is the technology edge that keeps us ahead of others in this business." Palmquist adds, "Customers need the increased timing resolution to help determine why a device operating at these higher clock rates has failed."


NOW IC DESIGNERS CAN VALIDATE THEIR OWN PROTOTYPES

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And, trying to stay ahead of the pack, IMS has come out with the Logic Master ST, a desktop version of the Logic Master 2000. "Where the larger system serves state-of-the-art ASIC designs, the ST addresses the needs of the system designer performing his first ASIC designs, using lower-density gate arrays and standard cells," says Lindsay. *–Jonah McLeod*

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256 x 4	HS-6551RH	160 ns
4K x 1	HS-6504RH	150 ns
1K x 4	HS-6514RH	150 ns
64K Module 8K x 8 16K x 4	HS-6564RH	250 ns
Asynchronous		
16K x 1	**HS-65262RH**	**100 ns**
2K x 8*	HS-65162RH	100 ns

*Samples available Quarter 2, 1987

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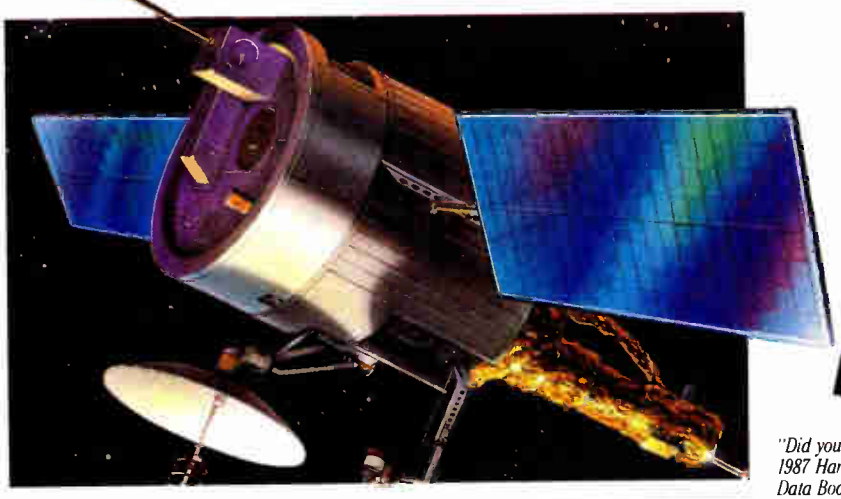

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MILITARY/AEROSPACE NEWSLETTER

PENTAGON BEGINS REVIEW OF VHSIC HARDWARE-DESCRIPTION LANGUAGE

Industry efforts to create a broadly accepted Very High Speed Integrated Circuits Hardware Description Language (VHDL) are beginning to bear fruit. The Pentagon is submitting a paper requiring VHDL documentation for all components procured after July to all three branches of the military for comment. The IEEE, meanwhile, has completed Draft Standard 1076/A, the VHDL Reference Manual, and has sent it out for industry comment. A meeting of the IEEE's VHDL analysis and standards subcommittee is scheduled for March 13 to discuss 1076/A. Industry acceptance of VHDL is expected to speed development of the VHSIC program by creating a common design language for all government agencies and vendors. An updated version of the IEEE draft standard, 1076/B, will be circulated to industry and Pentagon officials for additional comments. □

RADAR JAMMING OPTIONS LIMITED BY CANCELLATION OF F-111 PROGRAM

The U. S. Air Force's cancellation last month of a $1.2 billion program to equip its F-111 fighter-bombers with advanced radar-jamming gear has left the service with only a few alternatives: an updated version of Westinghouse Electric Corp.'s ALQ-131, which has flown on F-16, F-4, and some F-111 aircraft; ALQ-165 jamming pods; and Raytheon Corp.'s ALQ-184, a highly modified version of Westinghouse's ALQ-119 pod. The Air Force said it dropped its F-111 electronics-warfare program because the bids were too high—30% to 70% more than budgeted. The Air Force did not disclose the amount of the bids, but it did identify the bidders: AIL Division of Eaton Corp., Sanders Associates, and the team of Westinghouse and ITT Corp. Industry sources maintain that the Air Force could have awarded a contract for a new system a year ago, but the delay, during which additional testing and development was carried out at contractors' expense, created a $600 million to $700 million shortfall in the F-111 radar-jamming budget. □

NSA COULD FURTHER CLOUD SECURITY PRODUCTS MARKET

The National Security Agency may muddy up the already clouded market for security products when it publishes a new list of "endorsed and preferred" computer and communications security devices and vendors. The new "Information Systems Security Products and Services" will supplement, but not supersede, the Defense Department's "DOD Standard—Trusted Computer Systems Evaluation Criteria," also known as the Orange Book, which describes the Pentagon's criteria for classifying hardware and software and includes an apparently outdated evaluated products list. The new book may be out by the end of next month. The NSA's National Computer Security Center also has been working on an appendix to the Orange Book that would, for the first time, cover security-product standards for local- and wide-area networks. Meanwhile, NATO plans to write its own standards for secure computer and communications devices, apparently in conflict with the Orange Book. □

GTE WINS $870 MILLION PACT FOR MOBILE-RADIO PROGRAM

GTE Government Systems Corp. has won an $870.6 million contract for the second phase of the Army's $4.3 billion mobile-subscriber-equipment program. Awarded by the Army Communications and Electronics Command in Ft. Monmouth, N. J., the contract calls for GTE's Tactical Systems Division in Waltham, Mass., to deliver more than 1,400 switching centers, 8,000 mobile radios, and 25,000 telephones over a 10-year period starting in 1988. The MSE project will provide an integrated digital mobile communications network for the battlefield. □

MILITARY/AEROSPACE NEWSLETTER

TWO-YEAR-OLD HITTITE CO. IS NAMED A MIMIC PRIME CONTRACTOR

Hittite Co., Woburn, Mass., a privately held producer of gallium-arsenide microcircuits, has led a team that includes Eastman Kodak's Government Systems Division, Harris Microwave Semiconductor Division, and Adams-Russell Co. to win a share of the concept-definition phase of the Defense Department's Microwave/Millimeter Wave Monolithic Circuit (Mimic) development program. Founded two years ago by Yalgin Ayasli, who had worked on the Raytheon Research Division's Mimic program, Hittite's contract calls for the development within one year of a comprehensive plan to install Mimic parts in military systems [*Electronics*, Feb. 19, 1987, p. 84]. According to Ayasli, Hittite will design the GaAs circuits for its team, Kodak will act as systems integrator, and Harris and Adams-Russell will produce the chips. □

ARMY SEEKS PROPOSALS FOR NEXT-GENERATION ATE TEST-PROGRAM SETS

The U. S. Army has just issued requests for proposals for the first test-program sets for its next-generation Intermediate Forward Test Equipment, currently under development by Grumman Corp., Melville, N. Y. The initial RFPs call for 48 different software test-set applications for the Hawk missile system, but IFTE is designed to troubleshoot virtually everything in the Army's inventory. To ensure that future weapons systems will be compatible with IFTE, software development by both the Army and ATE vendors will be carried out on equivalent commercial test equipment. Grumman will create some 30 demonstration test-program sets by the end of this year, when its development contract is completed. Eventually, some 200 test-program sets will be developed for the Hawk program alone. Also, in time, the IFTE program will be opened to a second prime contractor, or what Grumman executives call a "leader-follower" arrangement. At the same time, segments of the IFTE program will be opened for competitive bidding, perhaps as early as next year.□

ARMY DEVELOPS INTERIM GUIDELINES FOR NUCLEAR-PULSE HARDENING

Scientists at the Harry Diamond Laboratories, Adelphi, Md., a part of the Army Laboratory Command, have developed an interim set of guidelines for hardening military command, control, communications, and intelligence (C^3I) equipment against nuclear electromagnetic pulses. The guidelines will be used until final standards and specifications are settled. Nuclear radiation hardening has reached a high enough priority that all services are working jointly on it. The Army, however, is already 24 months into its program for hardened mobile, ground-based C^3I. The next step, Army spokesmen say, will be to build a test facility to demonstrate these measures. Several contracts have already been awarded, and the facility is expected to begin operations late this year. Meanwhile, the Air Force Air Logistics Command has awarded a $5.2 million add-on contract to GTE Government Systems, Waltham, Mass., to provide an upgraded design of electrical-surge arresters for the UHF equipment at Minuteman missile-system launch facilities. □

PENTAGON CUTS UNIVERSITY RESEARCH BUDGET FOR FY '88 and '89

The Pentagon's newest program for fostering science and engineering education, the DOD University Research Initiative, will get less in the next two fiscal years than the $125 million it received in fiscal year 1986, when the program was started. The Defense Department has requested only $100 million per year for the program for 1988 and 1989, and Ronald L. Kerber, DOD deputy undersecretary for research and advanced technology, told IEEE Technology Policy Conference attendees in Washington that the long-term outlook for the program is "uncertain." □

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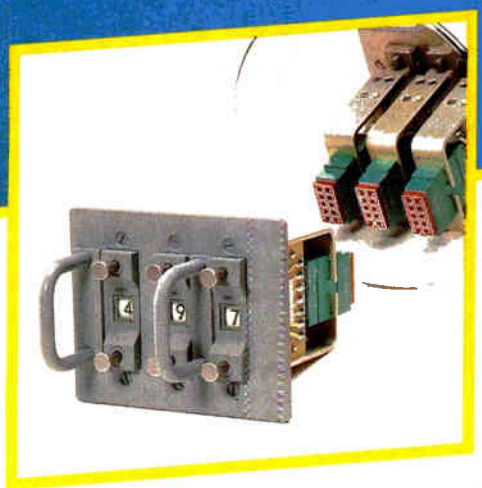

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NEW PRODUCTS

TEKTRONIX HIGH-END GRAPHICS MOVES DOWN TO THE PC MARKET

PLOT 10 COLOR CAPABILITY FOR THE IBM PC COSTS LESS THAN $4,000

High-performance color graphics from Tektronix Inc., a de facto standard for mainframes, are available for the first time on IBM Corp. Personal Computers for less than $4,000. In putting its Plot 10 system on the smaller machines, Tektronix gives PC owners a window into high-end graphics formerly available only on workstations costing five times as much, says Merle Smith, manager of the Tektronix PC Graphics Product Group. The new package does not, however, deliver the speed, resolution, and applications environments of true workstations, he adds.

The package—a Plot 10 PC 4100 graphics coprocessor board, a 640-by-480-pixel color monitor, and terminal-emulation software—costs about $3,250. It can emulate the IBM PC enhanced graphics adapter (EGA) and color/graphics adapter (CGA) boards.

WIDE USE. Since versions of these graphics boards from many vendors have been widely used, their emulation in the PC4100 allows the users of the new Tektronix board to run existing graphics software in EGA or CGA.

The graphics coprocessor board uses the Texas Instruments Inc. TMS34010 graphics-processor chip [*Electronics*, January 27, 1986, p. 15] for quick processing of graphics functions. This chip takes on most of the graphics work, freeing the PC's processor to process the application program. Users can switch among the three modes—PC4100, EGA, and CGA—under software control.

The add-on board has two memory banks. One is a frame buffer for storing the 640-by-480 pixels and color information for simultaneous display of 256 colors from a palette of more than 16 million colors. The other is 1 megabyte of random-access memory to store the graphics programs, such as the Tektronix graphics interface (TGI), microcode for specialized graphics functions, and other interfaces.

EXPANDABLE. The RAM can also extend display storage. Future versions will have larger frame buffers for better display resolution. "The next step is 1,024 by 768 pixels," says Smith. Systems programmers can use the Plot 10 TGI software to build new high-performance graphics applications and device drivers for links to existing applications.

Users who also want to use a PC as a graphics terminal linked to mainframe Plot 10 applications can install one of two Tektronix terminal-emulation programs. The Plot 10 PC-07 package gives IBM PC/XT, AT, or compatibles selected Tektronix 4107 terminal cababilities, while the Plot 10 PC-05 emulates a Tektronix 4105 terminal. Both emulators support graphics input devices, such as tablets and mice, and in an alphanumeric mode they also emulate Digital Equipment Corp.'s VT-100 terminals.

Tektronix is offering a 13-in. 640-by-480 color monitor to match the processor. The monitor requires either a Tektronix PC4100 coprocessor board or an EGA board.

Tektronics also has adapted its 4696 color ink-jet printer for use with a PC through a standard parallel printer interface.

The PC4100 board will be priced at less than $1,800. The emulation packages are priced at $495 and $995 for the PC-05 and PC-07, respectively. The new monitor will be about $950. All will be available March 31. – *Tom Manuel*

CHIP CHOICE. Tektronix' board uses the Texas Instruments Inc. TMS34010 graphics chip.

RISC COMPUTER TRIPLES MAINFRAME PERFORMANCE

The Artemis 8000 reduced-instruction-set computer outperforms general-purpose computers in handling project-management applications for companies such as electric utilities by as much as a factor of 3.5—and it fits into almost any computing environment.

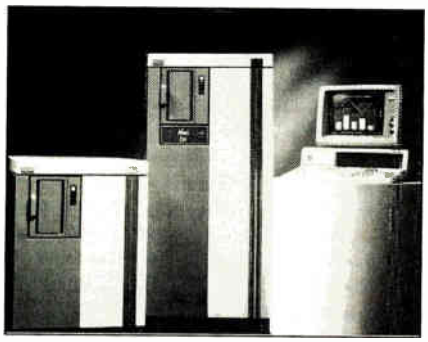
Metier Management Systems Ltd. of Hayes, UK, built a 32-bit superminicomputer by linking 16-bit processors, and then harnessed it to a set of 50 instructions designed to handle project-management applications typical of the public utility, construction, defense, and oil and gas industries.

From a hardware point of view, the supermini boasts an instruction-cycle time of 160 ns, compared with an instruction-cycle time of about 550 ns for conventional mainframes.

Metier boosted performance by reducing the original set of 500 instructions developed at Strathclyde University, in Scotland, by a factor of 10. To enhance performance still further, Metier designed separate processors for input/output channels and disk drives, relieving the main processor of the chore of executing these tasks.

To facilitate its integration into diverse computing systems, the Artemis 8000 is equipped to communicate through Ethernet and IBM Corp.'s Token Ring, among other networks. It will also be possible to update the system to work with the Open Systems Interconnection standard when that is finalized.

"It will communicate to the [IBM] 2780 and 3780 protocols," says Mike Metcalf, senior applications consultant. The Artemis 8000 links with most IBM mainframes and Digital Equipment Corp.



computers, as well as with Hewlett-Packard Co.'s distributed system protocol.

A basic Artemis 8000 system consists of the processor, 60 megabytes of removable disk storage, and 270 megabytes of fixed disk storage housed in a cabinet measuring 1,262 mm by 569 mm by 925 mm. It weighs 200 kg.

Six models are available, supporting from five to 30 concurrent users. Up to 80 users at remote locations can be connected to the system. Users gain access through intelligent work stations such as IBM PCs or compatibles, which function as coprocessors to handle local processing in conjunction with the main system processors.

Major options are: an information control system; a scheduling system; a project graphics system for drawing bar charts and logic diagrams; management graphics providing multicolor graphics and charts; and output devices such as high-resolution color terminals, compact flatbed plotters, and high-speed page plotters.

Other features include a soft instruction set, external disks supported by the standard Small Computer Systems Interface, up to 2 gigabytes of external disk memory, 4-megabyte memory cards with error detection and correction, 350-ns memory-access time, and remote diagnostics capability.

Metier will launch the computer this month, marketing it through a subsidiary in Houston, Texas. Prices start at about $250,000 but can go as high as $900,000 for complex systems that require extensive customization.

–Steve Rogerson

COMPAQ'S NEW PORTABLE BOOSTS SPEED BY 50%

The new Compaq Portable III computer boosts performance 50%, in large part because of six new application-specific integrated circuits designed to handle the full 12-MHz speed of Intel Corp.'s 80286 microprocessor. The new machine from Compaq Computer Corp. also features a bright, crisp plasma display and more memory capacity—up to 6.6 megabytes of system memory and 40 megabytes of disk space—than the Compaq Portable II [*Electronics*, Feb. 24, 1986, p. 64].

COMPACT. Besides boosting performance, Compaq also saved space and weight by incorporating ASICs and surface-mount technology in the design.

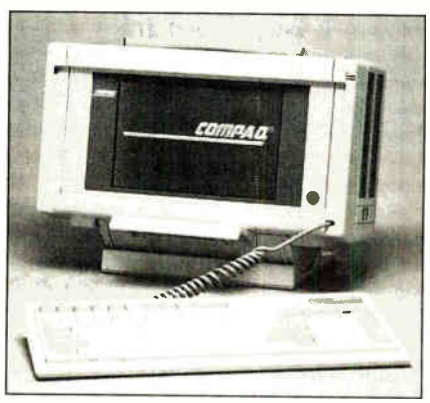
To take advantage of the 12-MHz 80286 microprocessor, Compaq developed six CMOS ASICs. Three of these gate arrays handle the new memory bus. An add-on expansion unit maintains compatibility with 8-MHz PC-bus peripheral boards. Two slots are provided for the add-on boards.

The other three gate arrays perform controller functions. One is a fixed-disk controller for an optional 40-megabyte, 3½-in. drive with a 30-ms average access time. The drive is supplied by Conner Peripherals, Pebble Beach, Calif. The Portable II Model 3 offered a 10-megabyte hard disk.

Another gate array controls the industry-standard 5¼-in. floppy drive—required for standard data and program interchange with other personal computers—and the built-in printer interface. A sixth gate array drives the dual-mode (text and graphics) plasma display. The Portable III's plasma display replaces the II's bulky cathode-ray tube while delivering brighter, sharper text and graphics.

The machine is 9.8 in. high by 17.7 in. wide by 7.8 in. deep and weighs 18 pounds—or 20 lbs. with a hard disk. It comes in three models, each with a basic 640-K bytes of system memory: the Model 1 costs $3,999 with a floppy drive only; the Model 20, with a 20-megabyte hard disk, is $4,999; and the Model 40, with a 40-megabyte hard disk, costs $5,799. System memory can be expanded internally to 6.6 megabytes, compared with a limit of 1.5 megabytes for the Portable II. All are available now.

–Tom Manuel



INTEL'S 80386 TRIPLES DAISY PC'S PERFORMANCE

PERSONAL LOGICIAN 386 HAS IBM PC AT ARCHITECTURE, HANDLES SOLID MODELING AND CIRCUIT SIMULATION

Computer-aided-design work-station vendor Daisy Systems Corp. is boosting performance of its Personal Logician series threefold by incorporating an Intel Corp. 80386 microprocessor and an 80287 floating point-coprocessor in its new Personal Logician 386. The company is also using the 80386 to upgrade its 32-bit work-station extension, the Logician.

With its enhanced computing power, the Personal Logician 386 can perform physical modeling, a capability not available on 286-based work stations, such as the company's Personal Logician 287. The 386 also handles such graphics-intensive operations as chip layout and printed-circuit-board layout and supports the sophisticated graphics interface found on Daisy's larger Logician work stations.

Based on the IBM Corp. Personal Computer AT architecture, the 386 offers IBM's Enhanced Graphics Adapter, or EGA, capability. When used for integrated-circuit design, it performs analog and digital circuit simulation, as well as schematic capture. Previous PC-based systems could simulate only relatively simple circuit designs. Simulations too complex for the Personal Logician 386 can be offloaded to larger computers.

HIGH RESOLUTION. Daisy's 19-in. monitor features 1,024-by-832-pixel resolution.

Daisy has also used Intel's 80386 in the upgraded version of its powerful Logician series. The Logician 386 is a 32-bit work-station extension optimized for physical layout of chips and printed-circuit boards.

It contains the company's own proprietary bit-slice graphics accelerator, which is four to five times faster than the EGA graphics, an essential capability for performing chip and pc-board layout. It offers twice the performance at 60% of the cost of currently available competitive systems from other vendors, the company claims.

286 ENHANCED. Daisy has also upgraded its 80286-based Personal Logician work stations by introducing IBM's EGA graphics capability for the family.

The basic configuration of the Personal Logician 386 comes with Intel's 80287 coprocessor, 2.5 megabytes of random-access memory, a 44-megabyte hard-disk drive, a 1.2-megabyte floppy disk, EGA graphics, and a 13-in. color monitor. It costs $20,000.

The Logician 386 comes with a high-performance graphics accelerator, a 19-in. monitor with 1,024-by-832-pixel resolution, 4 megabytes of RAM, an 85-megabyte hard-disk drive, a 60-megabyte tape drive, and a 1.2-megabyte floppy-disk drive. It costs from $50,000 to $85,000, depending on options and memory.

The Personal Logician 80286 with EGA graphics sells for $15,000. All three products are available 60 to 90 days after order. *–Jonah McLeod*

GENERATOR HIKES BANDWIDTH 100-FOLD

Hewlett-Packard Co.'s HP 8780A vector signal generator reaches almost 100 times the modulation bandwidth of conventional frequency synthesizers and can generate test signals with many types of analog and digital modulations, including combinations of vector, digital, frequency and amplitude modulations.

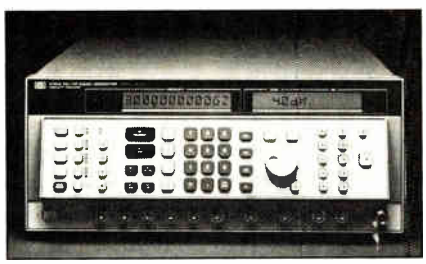
Another new instrument, the HP 8980A vector analyzer, measures and displays the components of actual signals with similar characteristics.

TWO CHANNELS. Like many new communications-, radar- and electronic-warfare systems, the instruments have separate I and Q (in-phase and quadrature-phase) channels. Custom testers have generally been needed to determine the dynamic characteristics of such systems.

But, says HP, the new instruments can replace custom testers because they have comparable architectures and cope with large bandwidths and complex formats of advanced signal-modulation techniques.

The HP 8780A synthesizes carrier signals from 10 MHz to 3 GHz with a resolution of 1 Hz. It modulates a carrier with data streams, pulses, or analog waveforms applied to its I, Q, or both I and Q inputs.

Both channels operate at modulation bandwidths to 350 MHz, allowing total modulations to 700 MHz. Inputs can be



transmitter-baseband signals or more specialized test signals.

Conversely, the HP8980A analyzes an incoming signal's I and Q components, and has probes for system-fault isolation. It is a dual-channel, sampling oscilloscope optimized for automatic measurement and display of phase and magnitude characteristics at per-channel bandwidths to 350 MHz.

Both instruments also feature open architectures so they can be used at intermediate frequencies with the user's choice of frequency converters to handle higher-frequency testing. To emulate a digital microwave transmitter's i-f stages, for example, the HP 8780A would use the transmitter's baseband data stream to modulate the carrier. With an up-converter on its output, the generator can also serve as a calibrated transmitter during receiver testing. Or, the HP 8980A can replace a receiver's i-f stages and, for transmitter testing, operate with a down-converter as a calibrated receiver.

In addition, the HP 8780A can utilize input from digital-to-analog converters. For example, signals with quadrature-amplitude-modulation formats beyond 64 QAM, the most complex now generally used in digital-communications systems, can be generated by converting baseband data streams to analog inputs.

The HP 8780A costs $55,000 and the HP 8980A $19,000. Delivery is 12 weeks after receipt of order. – *George Sideris*

MONITOR ACQUIRES, PROCESSES DATA

Datel's PM-5050 process monitor delivers in a single $395 package the functionality formerly available only with user-configured modules dedicated to each function.

It incorporates a microprocessor and sophisticated software to combine data acquisition, storage, relay, and processing functions for inputs from any of eight types of thermocouples.

A CMOS microprocessor controls basic functions, but the key to the flexibility of the PM-5050, says Ram Appalaraju, product marketing specialist, lies in "the depth of the software." The software resides in electrically erasable read-only memory, which also saves for reuse all control parameters set on the monitor.

The unit not only accepts a wide variety of thermocouple inputs, but also

supports more than 50 commands, which extend the range of configurability. A full five-digit, fluorescent display with 14 segments allows alphanumeric input directly from the front panel. This also provides precise control in high temperature applications.

TESTER. The new offering from the Mansfield, Mass., subsidiary of General Electric Co. targets factory automation or test and measurement applications. It has an isolated analog input section, a microprocessor and control logic, a front-panel display, a serial communications port, and setpoint outputs.

In other applications, the PM-5050 will serve as a remote transmitter for temperature information. Used in data acquisition, it can receive data at intervals ranging from 600 ms to 1 hr.

Four set points on the process monitor can be activated in up-going or down-going modes. Up to 1,400 V isolation is offered at all ends.

The analog-input hardware consists of thermocouple input circuitry, signal conditioning preamplifiers, cold junction compensation circuits, and a voltage-to-frequency converter. Available now, the device costs $395. *–Craig D. Rose*

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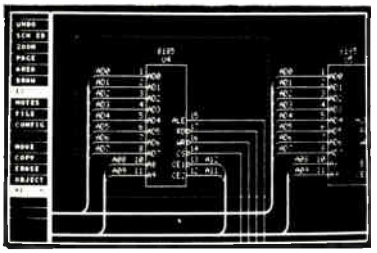

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DISTRIBUTION WEEK

GRAY-MARKET PRICING YIELDS CLUES TO SEMICONDUCTOR PRICE TRENDS

Movement in chip prices on the gray market can give distributors some indications about where manufacturers' prices will soon go, says Michael Gumport, an analyst with the investment firm of Drexel, Burnham, Lambert in New York.

Gumport studies the advertisements gray marketeers run in industry journals. By comparing the price an advertiser asks for a given chip one week with the price quoted the week before, he produces an indicator of how well the chip makers themselves are doing.

Between November 1985 and March 1986, Gumport says, gray-market prices rose at an annual rate of 20%—good news for chip makers' profit picture. But from April through June, prices dropped at an annual rate of 15%. Speculation over the summer that a chip agreement between the U.S. and Japan was imminent helped prices hold at that rate, but by September, when the agreement was signed, prices had begun to tumble at a 45% annual rate. Now, Gumport says, "pricing looks better—nothing's going up, but at least it has stopped plunging."

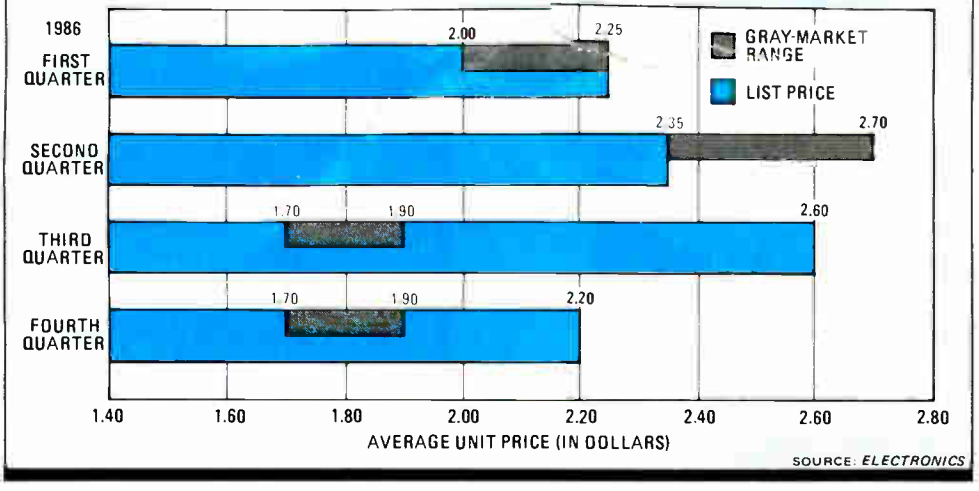
Gumport does not generally track price changes for specific parts, but he does say that the gray-market prices for 256-K dynamic random-access memories are rising, after being essentially flat in the $1.70 to $1.90 range over the past six months. Now prices are edging back toward $1.90, and Gumport offers hope that they could break the $2 barrier in the coming months. "To have been flat for six months is very good, but the level we're flat at is too low," he says. "But it looks like the Japanese are cutting back, and that makes me optimistic—provided demand keeps growing at the [current] modest recovery rate, it should help firm up prices."

Information from Dataquest Inc., San Jose, Calif., shows manufacturers' prices for 256-K DRAMs falling over the last six months of 1986, after rising during the first two quarters of the year. Gumport says those trends could reflect the relationship of manufacturers' prices to prices on the gray market during the previous quarter (see figure). Most manufacturers' orders are on contract rather than by spot pricing, so they lag behind the gray market—changes in gray-market prices in one quarter are generally followed by corresponding changes in contract prices in the next.

"They're speculators," Gumport says of the gray marketeers. "They try to have supply when demand is heavy and not to have too much inventory when demand is weak."

–Tobias Naegele

AVERAGE LIST U.S. PRICES FOR 256-K DRAMS COMPARED WITH GRAY-MARKET PRICES



SOURCE: ELECTRONICS

PHILIPS, E.F. JOHNSON SIGN SALES PACT

Philips Radio Communication Systems Ltd., the Cambridge, UK, subsidiary of Philips NV of the Netherlands, has signed a joint-distribution deal with E.F. Johnson Co. of Waseca, Minn.

The joint agreement lets Johnson sell a number of British-made products in the U.S., including the PF85 and PF88 portable radiotelephones and the FM91 and FM92 series of mobile radiotelephones.

Philips UK in turn will be able to distribute some Johnson products in various countries. The main product will be Johnson's trunked radio systems, which consist of base station, mobile radios, and portable radios, as well as the equipment that links them.

Philips hopes that the agreement will also lead to technology exchanges between the two companies' combined research and devel-

KIERULFF TO SELL INTEL LINE

Kierulff Electronics, Cypress, Calif., has added to its line of very large-scale-integration semiconductor products—including boards, development systems, and original-equipment manufacturing systems—from Intel Corp., Santa Clara, Calif. New market areas that will be served by this agreement are Dallas, St. Louis, Salt Lake City, and Wallingford, Conn. This expansion gives Kierulff 13 out of the 30 franchised territories, including San Jose, Los Angeles, the San Fernando Valley, Orange County, and San Diego, in California; plus Phoenix, Boston, Chicago, and Milwaukee. Kierulff will stock and sell Intel's full line of memory and microprocessor components in all these locations.

WANGTEK TARGETS EUROPE FOR DRIVES

Wangtek Europe, the new London-based operation of the Wangtek division of Rexon Inc., will manage sales and support activities of the company's line of ¼-in. cartridge tape-drive products to major OEM customers and distributors throughout Europe. Rexon's headquarters are in Simi Valley, Calif.

BOCA CUTS MEMORY BOARD PRICES

Boca Research Inc. has cut the price on its BOCARAM/XT 8-bit memory-expansion boards for IBM Corp. Personal Computers and XTs by as much as 29%.

The 1-Mb version, originally $395, has been reduced to $345. The 2-Mb version has been reduced from $740 to $575, and the 1-Mb expansion daughter board drops from $345 to $245.

ELECTRONICS WEEK

ITALY'S SGS RESCUES LATTICE

SGS Microelettronica S.p.A., Italy's leading chip maker, has found a new avenue into semiconductor technology via needy Lattice Semiconductor Corp. The Portland, Ore., maker of advanced programmable logic, reeling from layoffs and a lawsuit, will license its GAL generic-array-logic technology to the Agrate (Milan) firm, receiving in return cash and foundry services. Lattice has now been able to pay its employees all the salary lost last fall when the company could not meet its payroll. Meanwhile, SGS adds programmable logic to its broad portfolio of semiconductors.

10-Mb/s ETHERNET TO USE PHONE LINES

The 3Com Corp. promises to deliver full 10-Mb/s Ethernet capability over unshielded twisted-pair telephone lines with a set of products to be introduced by summer. In contrast, Starlan, the current implementation of the IEEE 802.3 local-area-network standard for twisted pairs, operates at only 1 Mb/s. 3Com says it has found ways to keep twisted-pair radiation and radio-frequency susceptibility within acceptable limits, and to maintain the 10-Mb data rate over distances as great as 75 to 100 meters. It expects to market an interface that will let standard Ethernet controllers plug into phone systems.

OPTICAL DISKS SPEED ID CHECKS

A half-million-dollar optical disk-based system planned by Harris Trust & Savings Bank, Chicago, is being billed as the first to allow bank employees to call up a customer's photo and signature on monitors at each teller's window. Supplied by Instant Identification Images Inc. of Chicago, the system will pay dividends in customer relations and fraud prevention, the bank says, by allowing positive signature verification within 20 to 45 seconds, compared with the 3 minutes it now takes with microfiche.

VLSI TECHNOLOGY, MOSTEK FORM PACT

Two leading players in the fragmented but growing speciality memory market have joined forces to attempt to define standard products by second-sourcing each other's chips and cooperating on developing new ones. Thomson Components-Mostek Corp. of Carrollton, Tex., and VLSI Technology Inc. of San Jose, Calif., will second-source five of each other's first-in, first-out memories, dual-port random-access memories, cache-tag RAMs, and static RAMs. Each company can incorporate the other's products into application-specific products, which can themselves be second-sourced.

3 DRAM MAKERS SETTLE WITH TI

Texas Instruments Inc. recently settled three more patent suits it filed against nine dynamic random-access-memory makers in the Far East. TI executives in Dallas report that the patent-infringement suits have been settled and new cross-licensing pacts have been reached with Oki, Mitsubishi, and Matsushita. Earlier this year TI announced similar settlements with Toshiba, Fujitsu, and Sharp. All agreed to pay TI a fixed royalty for DRAMs and per-unit fees. TI has not disclosed the details of each agreement. Still, complaints against Hitachi, NEC, and Samsung remain unresolved.

SONY TO MAKE FLOPPIES IN U. S.

Sony Corp., Tokyo, will start manufacturing and assembly of high-density 5¼-inch floppy disks in the Dothan, Ala., plant of Sony Magnetic Products Inc. The plant, which has been manufacturing video cassettes since 1977, has an assembly capacity of 1 million floppies per month. Sony will not say when the plant will start making the disks or what percentage of disks to be sold in the U. S. will be manufactured there.

AMNESTY OFFERED TO PAY-TV PIRATES

In a move to promote the legal use of satellite pay television, General Instrument Corp.'s Video Cipher division, San Diego, is offering a no-questions-asked amnesty program for owners of GI decoders whose units have been altered to illegally unscramble signals. Owners have until March 15 to return units for a free retrofit to legal status by calling (619) 535-0244.

IBM PC CAN 'HEAR' 20,000 WORDS

IBM Corp is moving speech recognition forward another square. Moving beyond their last milestone—a Personal Computer-based system with a 5,000-word vocabulary—researchers at the IBM Thomas J. Watson Research Center now have a desktop system that can recognize 20,000 words. The system, which requires the speaker to pause between words, will be tested in IBM offices while the researchers try to eliminate the need for these pauses.

GMFANUC ROBOTICS LAYOFFS CONTINUE

Citing insufficient orders for its factory automation equipment, GMFanuc Robotics Corp., Troy, Mich., laid off another 70 workers last month—12.7% of its work force. The cutbacks follow an earlier retrenchment last year when the company laid off 200 workers as a result of $88 million worth of order cancellations and delays from General Motors Corp., GMF's largest customer [*Electronics*, Aug. 21, 1986, p. 29]. GMF, a joint venture of GM and Fanuc Ltd. of Japan, is the largest supplier of robotics systems to the U. S. Although GMF has for the first time reduced its dependency on the automotive industry to less than half its revenues, this year's gains in nonautomotive business were not enough to avert more layoffs.

U. S. ELECTRONICS IMPORTS, DEFICIT UP

Total U. S. electronics imports were $50.3 billion last year, exceeding exports by $16.9 billion, according to a report by the Electronic Industries Association in Washington. Last year's imports were $43.4 billion while the electronics trade deficit stood at $12.4 billion. The U. S. bought the most electronics goods from Japan in 1986, a whopping $23.7 billion, while Taiwan followed a distant second at $3.9 billion. Meanwhile, South Korea moved up from fifth place on last year's imports list to third this year with $3.3 billion. In exports, the top destination for U. S. products was Canada at $4 billion, followed by the UK at $3.2 billion and Japan at $2.9 billion.

TRW GOES AFTER U. S. SPACE MARKET

TRW Components International Inc., which has supplied high-reliability microcircuits to European, Japanese, and Canadian space markets, is expanding sales and services into the domestic high-reliability space market: it has formed strategic agreements with original-equipment manufacturers and restructured its organization to support the broadened marketing thrust. Under licensing agreements, OEMs will manufacture wafers that TRW Components International will use to produce devices to NASA and Air Force Space Division specifications.

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2 17 32 47	62 77 92 107	122 137 152 167	182 197 212 227	242 257 272 349	364 379 394 409	424 439 454 469	484 499 704 719
3 18 33 48	63 78 93 108	123 138 153 168	183 198 213 228	243 258 273 350	365 380 395 410	425 440 455 470	485 500 705 720
4 19 34 49	64 79 94 109	124 139 154 169	184 199 214 229	244 259 274 351	366 381 396 411	426 441 456 471	486 501 706 900
5 20 35 50	65 80 95 110	125 140 155 170	185 200 215 230	245 260 275 352	367 382 397 412	427 442 457 472	487 502 707 901
6 21 36 51	66 81 96 111	126 141 156 171	186 201 216 231	246 261 338 353	368 383 398 413	428 443 458 473	488 503 708 902
7 22 37 52	67 82 97 112	127 142 157 172	187 202 217 232	247 262 339 354	369 384 399 414	429 444 459 474	489 504 709 951
8 23 38 53	68 83 98 113	128 143 158 173	188 203 218 233	248 263 340 355	370 385 400 415	430 445 460 475	490 505 710 952
9 24 39 54	69 84 99 114	129 144 159 174	189 204 219 234	249 264 341 356	371 386 401 416	431 446 461 476	491 506 711 953
10 25 40 55	70 85 100 115	130 145 160 175	190 205 220 235	250 265 342 357	372 387 402 417	432 447 462 477	492 507 712 954
11 26 41 56	71 86 101 116	131 146 161 176	191 206 221 236	251 266 343 358	373 388 403 418	433 448 463 478	493 508 713 956
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13 28 43 58	73 88 103 118	133 148 163 178	193 208 223 238	253 268 345 360	375 390 405 420	435 450 465 480	495 510 715 958
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4 19 34 49	64 79 94 109	124 139 154 169	184 199 214 229	244 259 274 351	366 381 396 411	426 441 456 471	486 501 706 900
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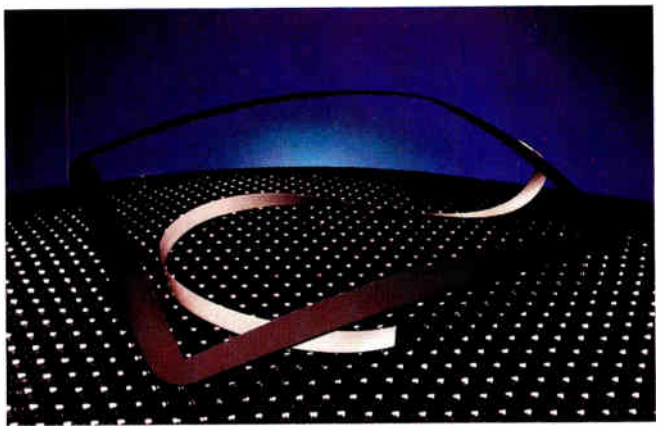

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