HIGH-POWERED IMAGE PROCESSING ON A PC GETS CLOSER/62

MOTOROLA GRABS THE LEAD IN ECL DENSITY/71

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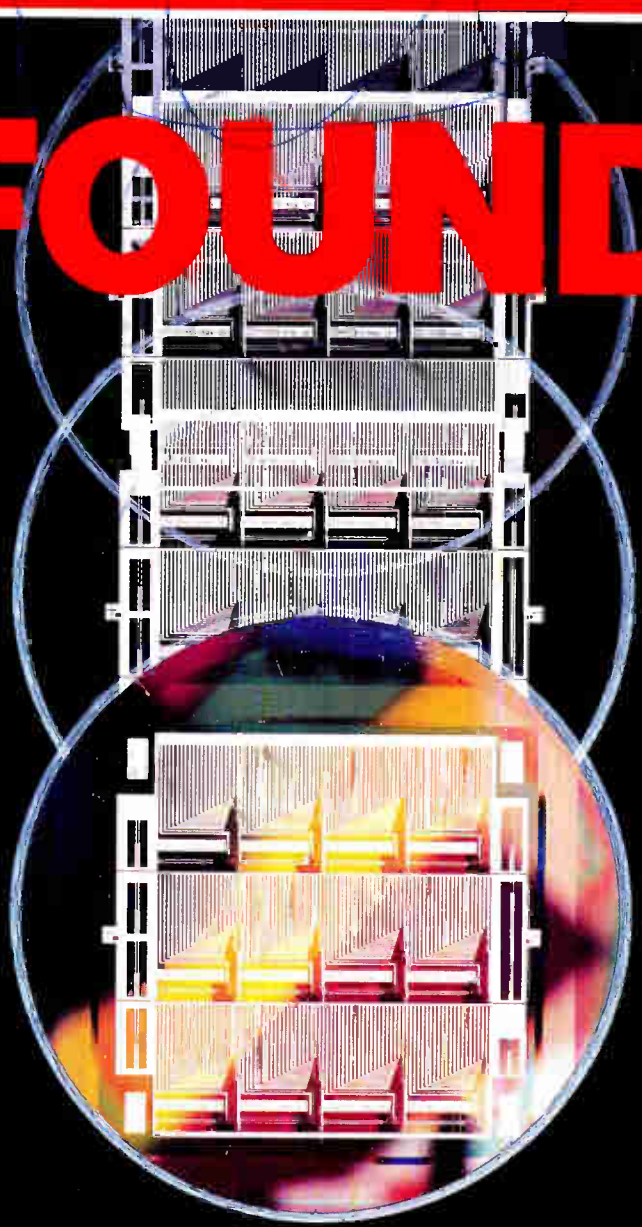

A PRACTICAL WAY TO TURN OUT JOSEPHSON JUNCTION CHIPS

HOW HYPRES USES ITS ICs TO BUILD 70-GHZ SCOPES

PAGE 49

National Semiconductor

"This isn't going to be easy."

"And because we had the edge from the very beginning."

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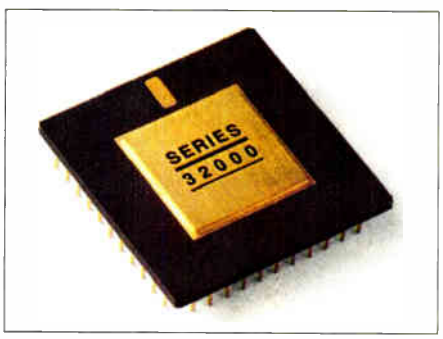

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Journalists, in their unending race to stay ahead of the technology as well as their competitors, can be lucky or good. The lucky ones are those who happen to be standing in the right place when the story breaks. But the good ones do their homework, develop knowledgeable sources, keep abreast of developments, and anticipate just where to stand and when to stand there.

IVERSEN: "Everyone I talk to is excited about its prospects."

Take superconductivity—specifically, Josephson junction circuits. The technology showed great promise in the laboratory 25 years ago, but it has had its ups and downs—mostly downs—since then, reaching its nadir in 1983 when IBM Corp. stopped work on a superconducting mainframe computer based on Josephson junctions.

Now, however, there is once again excitement and anticipation among researchers. Eventually, the word will get around, but you can read the story right now because *Electronics* has been on it all along.

Two years ago, in an article by Wes Iversen, we told you that the technology was on an upswing [*ElectronicsWeek*, Feb. 25, 1985, p. 28], and just last month Tobias Naegele described breakthrough work by IBM and others around the world in superconducting materials [*Electronics*, Jan. 22, 1987, p. 37].

So we were perfectly positioned to cover the resurgence of interest in superconducting, and we're off and running in this issue. Starting on p. 49 we present a three-article package that will tell you just where the technology stands and where it's going. We start with Executive Editor Sam Weber's story of a small company that has finally managed to do what the big guys couldn't with Josephson junction materials and cooling: it has built the technology into an instrumentation work station. Next, Tobias tells why a startup thinks it can succeed with commercial products based on a technology that many have written off as a laboratory curiosity that will never work, and Wes follows with an overview of the latest work.

"The trigger is definitely the new materials that Tobias described in his Jan. 22 story," says Wes. "Everyone I talk to about Josephson circuitry is excited about its prospects, and everyone starts by mentioning the IBM work. One scientist compares it to the running of the first four-minute mile. It was the unattainable goal for a century, a symbol that went beyond track and field to stand for the ultimate performance in any field. Then, once it was done, other milers began breaking four minutes all over the place."

Writing about the technique inevitably leads to the military, which is quite interested in superconductivity, and that creates problems for journalists. "It takes a long time to get anyone connected with leading-edge defense research to talk to journalists," says Wes. "One interview took me two weeks to set up. They wanted to know in advance what I would ask, and then when they finally decided to let the guy talk to me on the phone, there was a security man listening in. But they're an integral part of the story, and you have to play by their rules."

Laurence Altman

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Electronics

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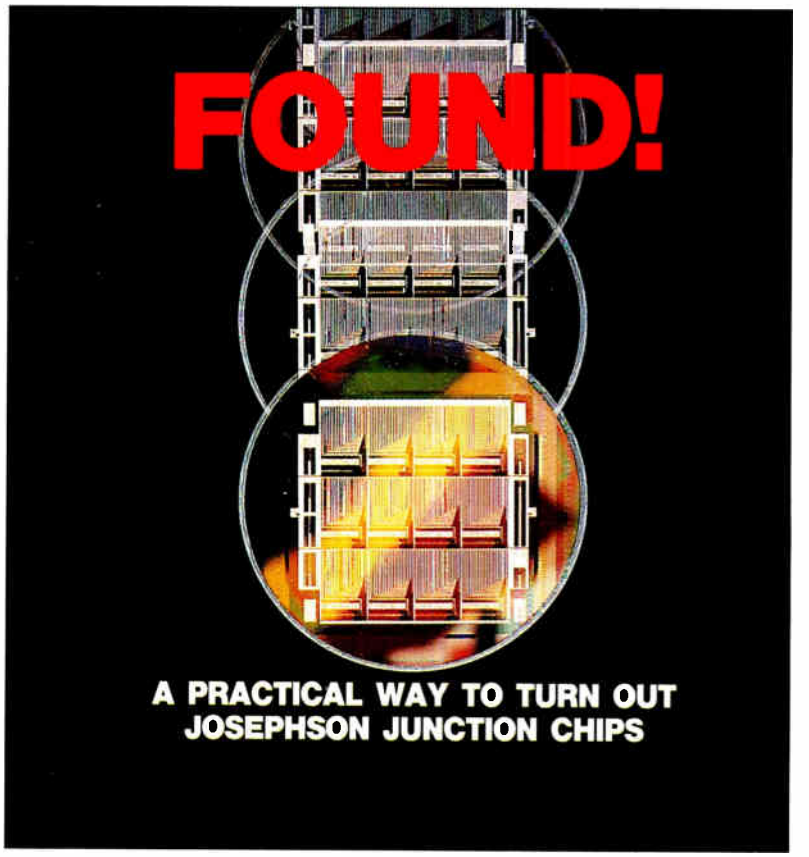

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NEW PRODUCTS

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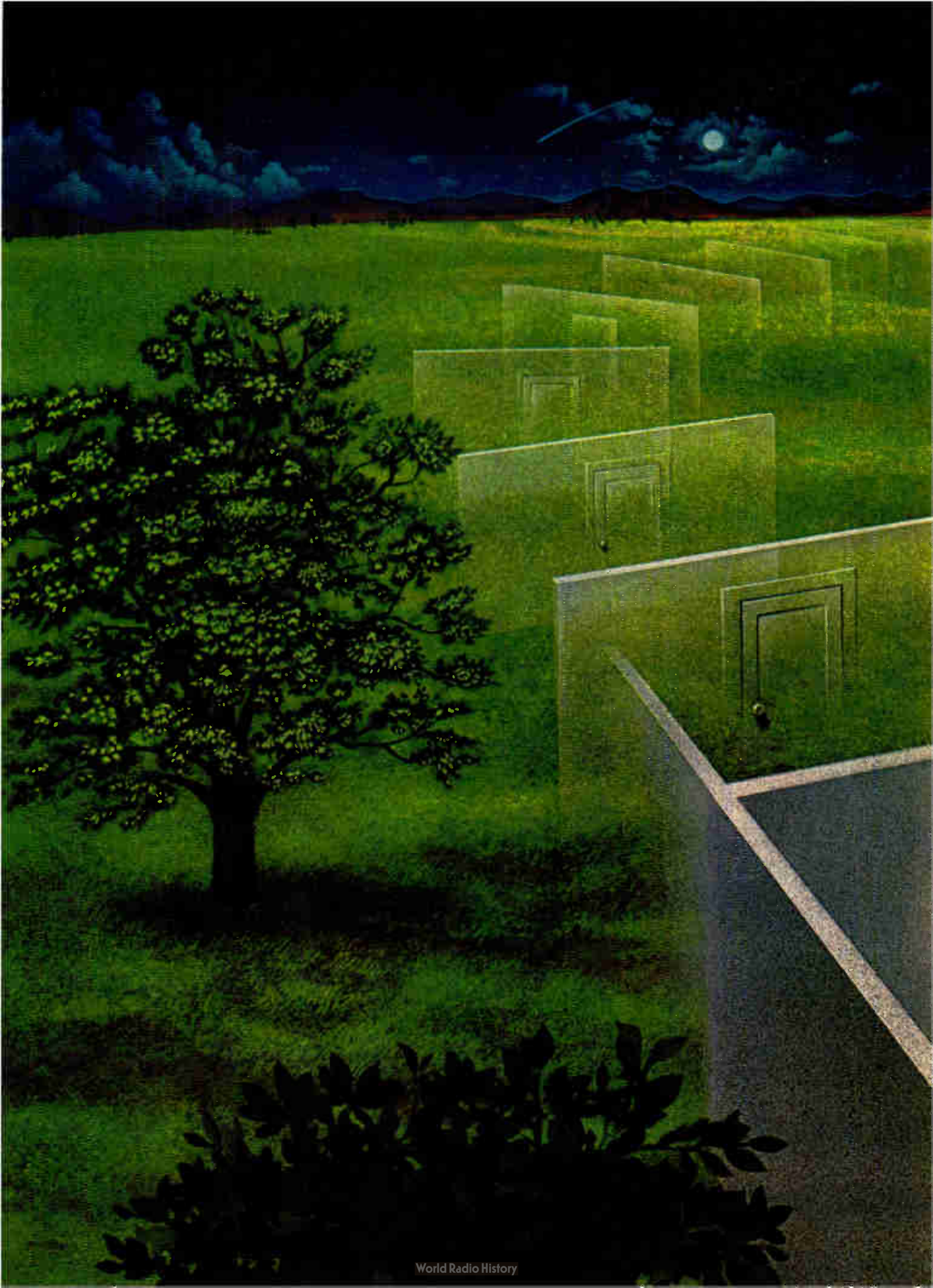

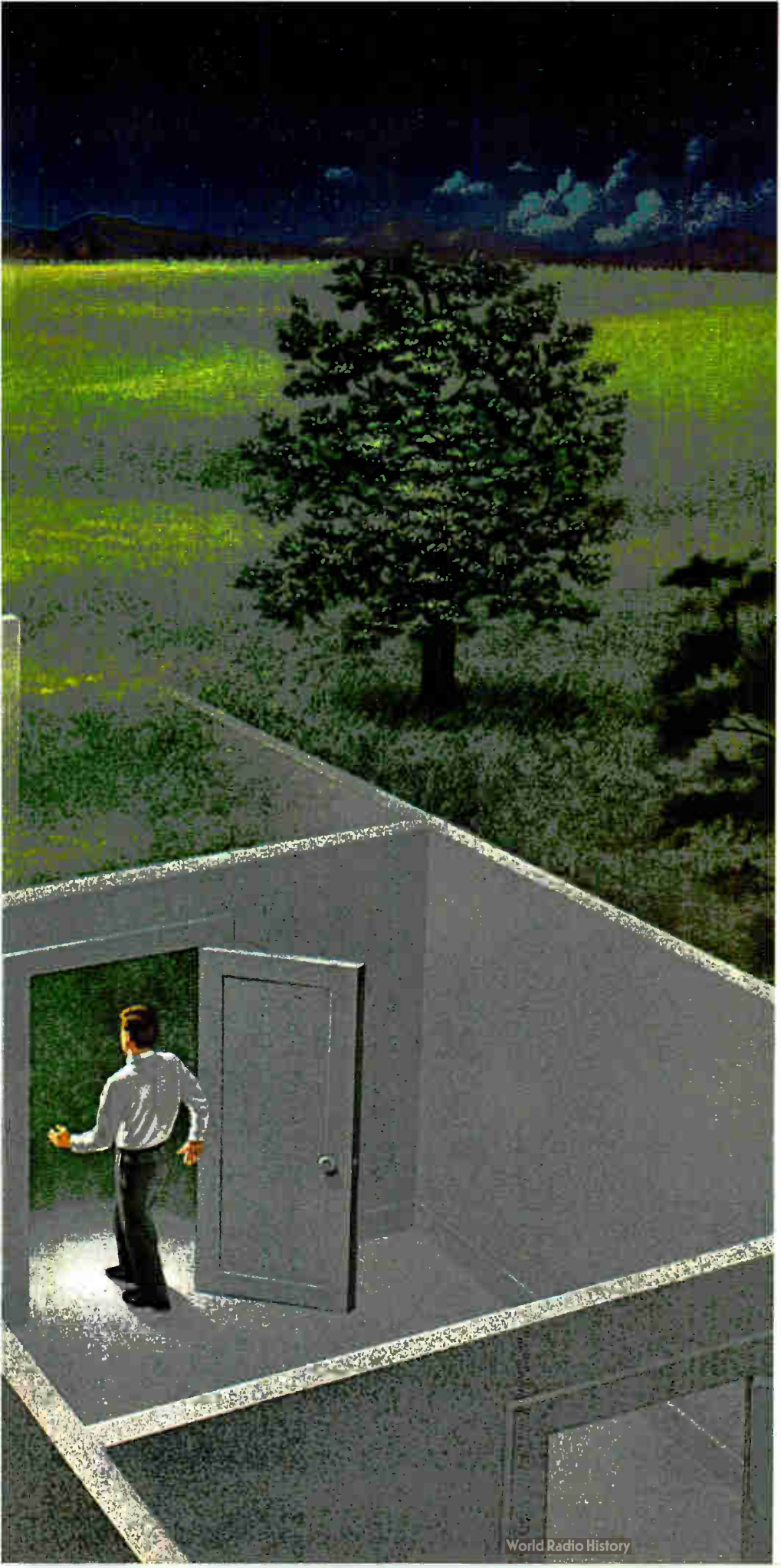

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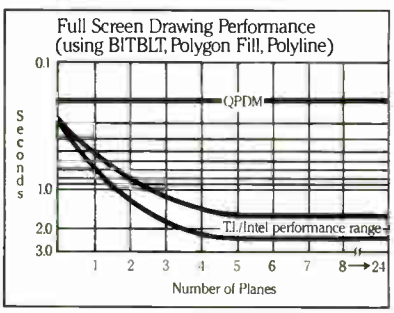

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'There's an incredible amount of money still going into high-tech investments,' says Technologic's Shaffer; venture money for computer deals hit $1.2 billion in 1986

We weren't the only ones surprised to read in *The New York Times* recently—front page, no less—that venture capitalists are rapidly losing interest in funding high-tech startups. Not so, declares one veteran venture capitalist who has scored with several outstanding successes. He figures there were just two things wrong with the *Times*' story: it ran on page one, and it was flat-out wrong.

Other long-time industry watchers feel the same way. "There's an incredible amount of money still going into high-tech investments," maintains Richard A. Shaffer, who writes the influential Technologic Computer Letter from New York. Dick calculates that when his firm finishes toting up 1986, venture financing for computer-related deals alone will exceed $1.2 billion, up from the $1 billion invested in 1985.

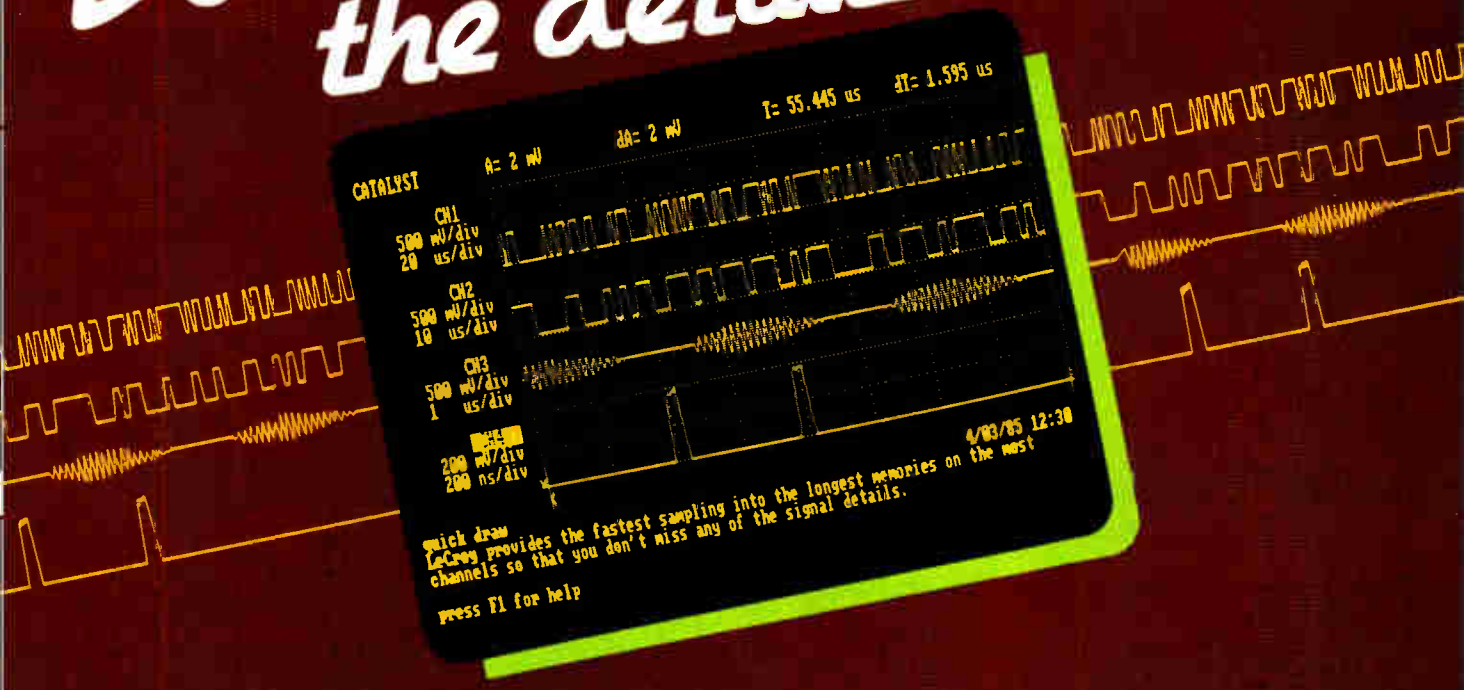
In Technologic Partners' latest survey, venture investments amounted to $367 million in 107 deals in the third quarter of 1986, up from 64 deals worth $320 million in the third quarter of 1985. "We're convinced that computer investment will continue to rise, even during the industry's worst slump," Dick says. "There are few other places to put money that are as rewarding as the information industry."

Most of the computer-related companies that went public in 1986 had been around no more than three or four years, he notes. And yet the typical computer company last year went public at a valuation of slightly less than six times the amount of money that private investors had already put in. Investors on average had put $14.7 million in a company, which was valued at $86.2 million at the time of the offering.

Dick figures that 54 computer offerings were made in 1986. He thinks an even greater number of computer-related companies will go public this year. His preliminary list has 66 candidates that seem to him to be ready for an IPO. Some that appear imminent: Banyan Systems, Brøderbund Software, Corporate Software, and Proteon. Biggest deals ahead in terms of capitalization, Dick says, are probably Teradata, Scientific Computer Systems, and Sequent Computer. And any offerings in the semiconductor industry probably won't show up until the second half: they include Altera, Brooktree, California Devices, Dallas Semiconductor, International Microelectronic Products, Maxim Integrated Products, Micro Linear, Saratoga Semiconductor, Sierra Semiconductor, Vitelec, and Weitek.

ROBERT W. HENKEL

Don't miss the details!



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IMS1624 (OE, x4)	35, 45, 55ns
IMS1630 (x8)	45, 55, 70ns

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Device	Access Times	Idr*
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IMS1601L (x1)	45, 55, 70ns	10µA
IMS1620L (x4)	45, 55, 70ns	10µA
IMS1624L (OE, x4)	45, 55, 70ns	10µA

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MEETINGS

Automated Manufacturing Computers, Communications & Controls, Frost & Sullivan Inc. (106 Fulton St., New York, N. Y. 10038), Don Cesar Beach Resort, St. Petersburg, Fla., March 9-10.

CARTS '87, Components Technology Institute Inc. (Suite 117, 904 Bob Wallace Ave., Huntsville, Ala. 35801), Alicante Princess Hotel, Garden Grove, Calif., March 9-12.

Federal Computer Graphics Conference and Exposition, National Trade Productions Inc. (2111 Eisenhower Ave., Suite 400, Alexandria, Va. 22314), Washington Convention Center, Washington, D. C., March 9-12.

1987 Pittsburgh Conference & Exposition, The Pittsburgh Conference on Analytical Chemistry and Applied Spectroscopy Inc. (12 Federal Dr., Suite 322, Pittsburgh, Pa. 15235), Convention Center, Atlantic City, N. J., March 9-13.

Semicon Europa '87, SEMI (625 Ellis St., Suite 212, Mountain View, Calif. 94043), Zuspa Convention Centre, Zurich, Switzerland, March 10-12.

AES '87, Audio Engineering Society (60 East 42nd St., New York, N. Y. 10165), Queen Elizabeth II Convention Center, London, March 10-13.

Fourth Topical Meeting on Optical Data Storage, IEEE Lasers and Electro-Optics Society, *et al.* (Optical Society of America, 1816 Jefferson Pl., N. W., Washington, D. C. 20036), Harvey's Lake Tahoe, Stateline, Nev., March 11-13.

International Switching Symposium 1987, IEEE Communications Society and the IEEE Phoenix Section (445 Hoes Lane, Piscataway, N. J. 08854), Phoenix Civic Plaza, Phoenix, Ariz., March 15-20.

MFOC-87 The First International Military Fiber Optics and Communications Expo, Information Gatekeepers Inc. (214 Harvard Ave., Boston, Mass. 02134), Hyatt Crystal City, Washington, March 16-19.

Topical Meeting on Photonic Switching, IEEE Lasers and Electro-Optics Society, *et al.* (Optical Society of America, 1816 Jefferson Pl., N. W., Washington, D. C. 20036), Hyatt Lake Tahoe, Incline Village, Nev., March 18-20.

Defence Asia '87, Conference and Exhibition Management Service (1 Maritime Square #09-15, World Trade Center, Singapore 0409), Bangkok International Exposition Centre, Bangkok, Thailand, March 18-22.

CASA/SME's Seminar, Computer and Automated Systems Association of the Society of Manufacturing Engineers (1 SME Dr., P. O. Box 930, Dearborn, Mich. 48121), Chicago, Ill., March 23-25.

Lasers in Manufacturing: SPOT '87, Society of Manufacturing Engineers (1 SME Drive, P. O. Box 930, Dearborn, Mich. 48121), Biltmore Hotel, Los Angeles, Calif., March 23-26.

Stanford Conference on Advanced Research in VLSI, Stanford Center for Integrated Systems (Stanford University, Stanford, Calif. 94305), Room 110, Stanford, Calif., March 23-26.

Advances in Semiconductors and Semiconductor Structures, Society of Photo-Optical Instrumentation Engineers (P. O. Box 10, Bellingham, Wash. 98227-0010), Bay Point, Fla., March 23-27.

1987 IEEE VLSI Test Workshop, IEEE Computer Society, Test Technology Committee, IEEE Philadelphia Section (Naval Air Engineering Center, ATE Software Center, Code: 92514, Lakehurst, N. J. 08733), Bally's Park Place Casino Hotel, Atlantic City, N. J., March 24-25.

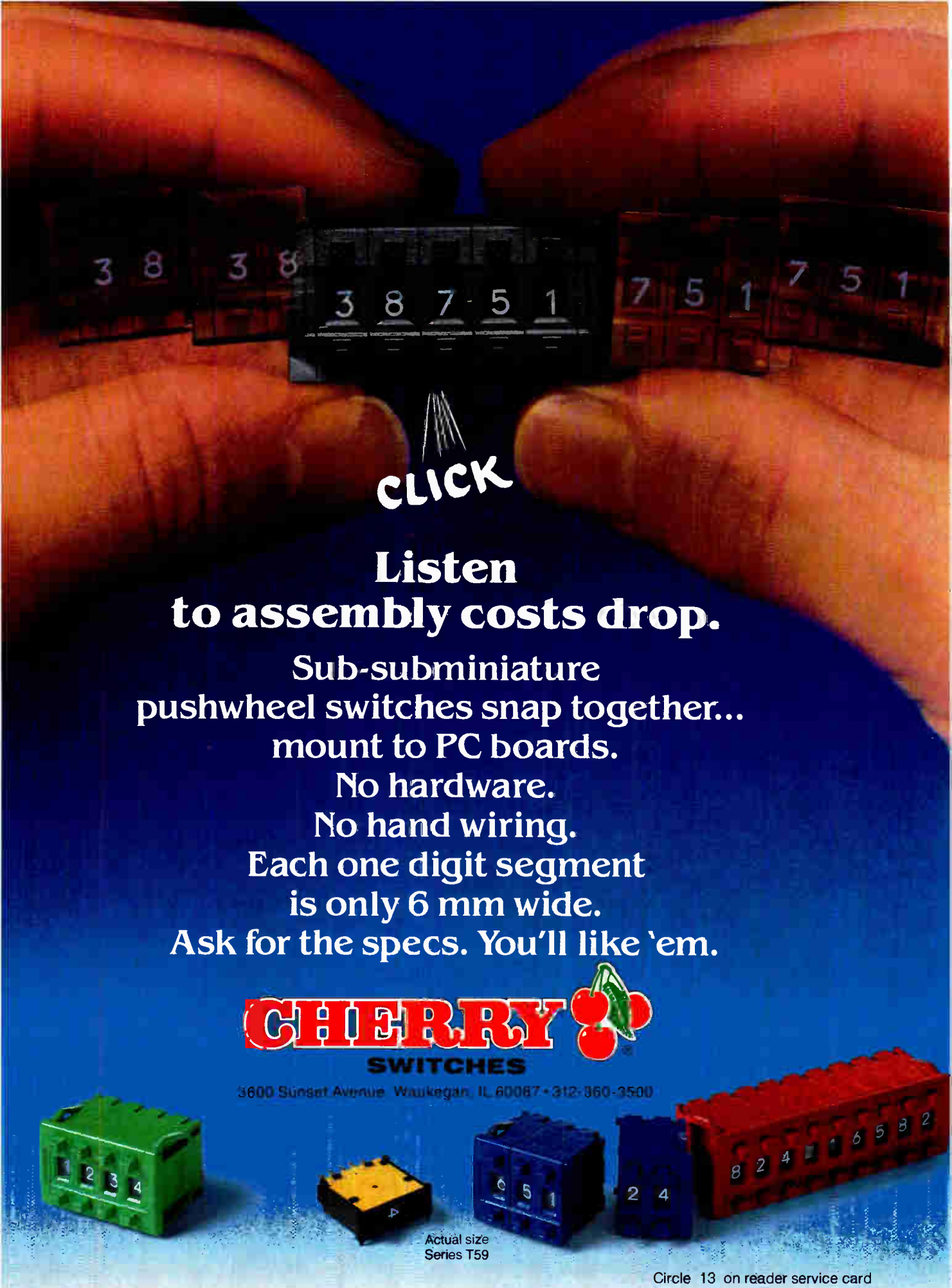
Internepcon Production Exhibition and Conference, Cahners Exhibitions Ltd. (Chatsworth House, 59 London Rd., Twickenham TW1 3SZ, UK), National Exhibition Centre, Birmingham, UK, March 24-26.

Southcon/87 Electronic Show and Convention, Region Three: the Florida Council, and the Atlanta Section of IEEE (8110 Airport Blvd., Los Angeles, Calif. 90045-3194), Georgia World Congress Center, Atlanta, Ga., March 24-26.

National Association of Broadcasters 65th Annual Convention & International Exposition, National Association of Broadcasters (1771 N St., N. W., Washington, D. C. 20036), Dallas Convention Center, Dallas, Texas, March 28-31.

1987 Annual Convention and Exposition of the Electronic Funds Transfer Association, EFT Association (1726 M Street, N. W., Suite 1000, Washington, D. C. 20036), Caesars Palace, Las Vegas, Nev., March 29-April 1.

IPC 30th Annual Meeting, The Institute for Interconnecting and Packaging Electronic Circuits (7380 N. Lincoln Ave., Lincolnwood, Ill. 60646), Westin Peachtree Plaza, Atlanta, Ga., March 29-April 3.



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MC68020 vs. 80386.

How to run apples-to-apples vs. apples-to-oranges benchmarks on these archrival 32-bit MPUs.

Choosing the world's highest-performance 32-bit microprocessor should be as easy as making an apples-to-apples comparison with such industry-standard benchmarks as Whetstone and Dhrystone performance.

How to tell apples from oranges.

When pulling an apples-to-apples comparison, anyone, anywhere, should be able to easily duplicate the comparison factors and results. Repeatably.

Attempt no. 1.

So, when comparing the MC68020 and 80386, the first task is to find one of each.

Motorola shipped over a quarter of a million MC68020s last year, so finding one is easy. Get the fastest available—a 25 MHz—and a 20 MHz Motorola floating-point coprocessor, the MC68881.

Next (things get harder), try to get your hands on a fully functional, bug free 80386 MPU and 80387 floating point.

And now you know why it's so hard to make an apples-to-apples comparison: you can get the Motorola devices, but "comparable" '386 and '387s? No way. You have to settle for the slower '386 and the promise of silicon yet to come on the '387.

Attempt no. 2.

All right, if you can't find the chips, go for readily-available 32-bit systems and compare real, live, '020- and '386-based systems from the commercial market.

Exasperating, isn't it? There are hundreds of choices of commercially-available, '020-based systems. But, finding comparable '386-based systems...?

Attempt no. 3.

Running real benchmarks on real products is the best comparison. We've looked at two questionable comparison attempts. Now it's time to try some industry-standard approaches, such as Whetstone and Dhrystone benchmarking. That should allow an apples-to-apples comparison, shouldn't it? If not, at least it should be apples-to-apples on paper.

Here are currently-available Whetstone and Dhrystone procedures for the MC68020 and the 80386 32-bit processors. To use industry-standard methods of comparison, you'll have to—must—rerun the Whetstones and Dhrystones for the '386 along the same universally-accepted lines as for the '020.

And discover which has the greater potential for being a keystone and which for being a millstone in your new design. The MC68020 is *still* the highest-performance microprocessor no matter how you slice it!

WHETSTONE PERFORMANCE

The Whetstone is a standard double-precision, floating-point benchmark written in FORTRAN.

MC68020/68881	80386/80387
• Execution of standard Whetstone benchmark written in FORTRAN: recognized and run by all leading systems manufacturers (Cray, DEC, IBM, etc.).	• Execution of vendor-modified Whetstone benchmark written in C: nobody else in the industry uses this particular procedure.
• Double-precision floating point: specified by standard Whetstone for high accuracy.	• Single-precision floating point: non-standard Whetstone sacrifices accuracy for "performance."
• Complete, 10-loop-count execution: 1 million Whetstone instructions.	• Incomplete, 2-loop-count execution: only 200,000 Whetstone instructions.
• Unary instructions executed: specified by standard Whetstone; single-operand operations.	• No unary instructions executed: intentional '386-vendor modifications to Whetstone spec avoids single-operand operations.
• Entire Whetstone benchmark procedure was not modified from the original standard: no tricks or tweaks to hype performance. **Result:** 1.24 million Whetstones/second with commercially-available silicon (68020, 68881).	• Altered Whetstone benchmark procedure allowed '386 vendor more favorable results: avoided branch control overhead. **Result:** Claims that provide no ability for apples-to-apples comparison.

DHRYSTONE PERFORMANCE

The Dhrystone Benchmark measures CPU performance on a typical mix of high-level language statements.

MC68020	80386
• Dhrystone results measured on commercially-available system: Sun Microsystems 3/200 workstation.	• Dhrystone results measured on specially-modified "hot box" built by '386 vendor: '386 "starter kit" version not commercially available.
• Commercially-available operating system (UNIX®).	• No operating system used: '386 vendor used own modified debug monitor.
• Commercially-available UNIX® C compiler (cc).	• '386 Vendor used own internal "beta" version of C compiler: not commercially available.
• Real-world memory architecture: Dhrystone WRITE operations must pass through to main-memory DRAM. **Result:** 6362 Dhrystones with commercially-available, real-world systems.	• Utopian memory architecture: zero-wait-state WRITE operations to unlimited cache SRAM —no write through to main memory. **Result:** Claims that provide no ability for apples-to-apples comparison.

UNIX is a registered trademark of AT&T.

For an engineer-to-engineer or senior-manager-to-senior-manager update on the real 32-bit system products, call toll-

1-800-521-6274

free any weekday. If the call can't cover your needs, we'll have the appropriate person get in touch.

For more information on the MC68020, and an apples-to-apples comparison, send the coupon to Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036.

We're on your design-in team.

MOTOROLA

To: Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036

Please send me more information on the MC68020 32-bit system solution and apples-to-apples comparisons.

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Company_____

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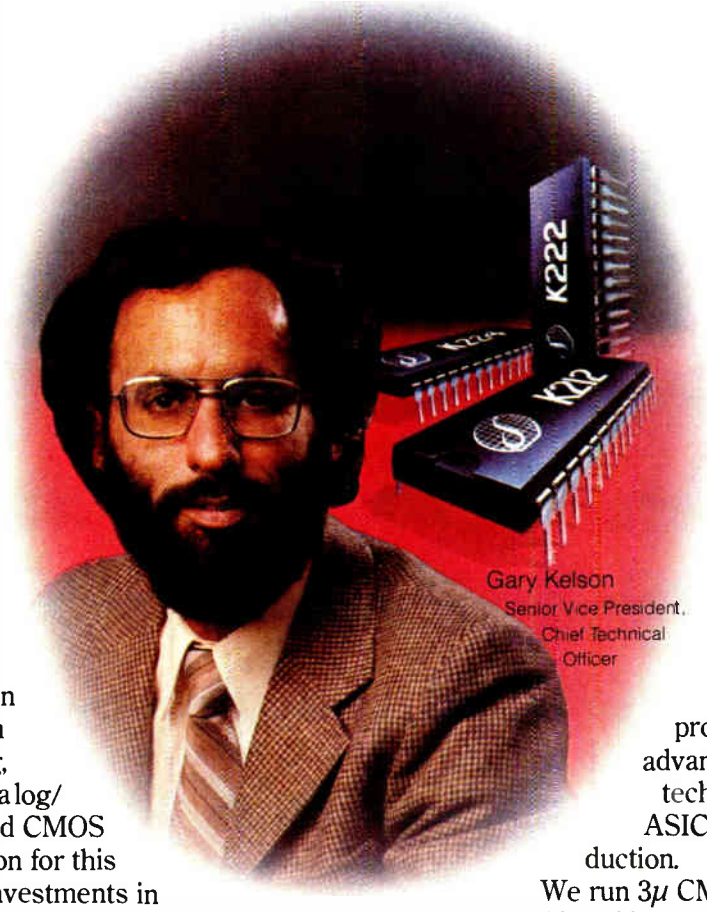
City_____ State_____ Zip_____

Call me (_____)_____

SILICON SYSTEMS— INNOVATORS IN INTEGRATION



Demonstrated Leadership in Combining Analog and Digital Designs on a Single Chip, and Offering Both CMOS and Bipolar Processing in Our Own Advanced Wafer Fab.

DESIGN EXPERTISE

Silicon Systems is years ahead of the competition in the design of custom and semicustom analog, digital, and combined analog/digital IC's in Bipolar and CMOS technologies. One reason for this success is our heavy investments in the most advanced computer-aided design system called IDM— Integrated Design Methodology. This proprietary design tool is the ultimate solution for supporting our customers' requirements. IDM allows auto-routed cells, compiled macros, and full custom circuitry to be intermixed on a single chip. The result: IDM provides faster turnaround, lower cost, and higher performance while eliminating design errors.

This design "edge" has led us into a broad diversity of design applications. However, we aren't resting on our laurels. With a dedicated design automation team with 14 years of experience, we are defining the state-of-the-art for future analog and analog/digital design methodologies. Furthermore, our systems engineering background allows Silicon Systems to live up to its name by providing true systems on a chip performance, thereby affording our customers a true competitive advantage.

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But there's more to a great IC company than just great design. And that's why Silicon Systems developed a multi-process wafer fab running advanced CMOS and Bipolar technologies optimized for ASIC development and production.

We run 3μ CMOS with both high voltage (12V) and low voltage (5V) analog/digital options. We also run 2μ CMOS for digital applications and will soon be scaling these to 1.25μ CMOS with analog enhancements to follow.

In Bipolar, the company has extensive experience producing analog/digital design with our 3μ, 4GHz f_T process. We are ramping up our newest Bipolar technology which will extend our processes to 6 GHz f_T and even lower noise capability.

The point is: there is no company better equipped to provide the right custom/semicustom chip solutions for your most challenging analog, digital, or combination analog/digital design problems. So, if you'd like to give your product a competitive edge, call or write for more information: Silicon Systems, 14351 Myford Road, Tustin, CA 92680. Phone: (714) 731-7110.

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INNOVATORS IN INTEGRATION

Circle 16 For Product Information

Circle 123 For Career Information

ELECTRONICS NEWSLETTER

SEMICONDUCTOR TRADE PACT THREATENED BY NEW CHARGES OF DUMPING

The U. S.-Japan semiconductor trade agreement, only six months old, may be on the verge of collapse. Last week the Semiconductor Industry Association charged that the Japanese government had not fulfilled its commitments to stop the dumping of memory chips and to open up Japanese markets to U. S. products. The SIA formally requested that President Reagan impose "trade measures" to penalize the Japanese for failure to comply with the agreement. Although the SIA refused to specify what measures it is seeking, some industry executives called for the imposition of duties on Japanese imports. The SIA is worried that the current improvement in the U. S. chip business is masking the real danger from the failure of the agreement to resolve trade differences. As if to underline those feelings, the SIA's January book-to-bill ratio rose for the fourth straight month, to 1.11. The increase, however, was due mainly to an 18% decrease in billings, to $646 million, as average bookings rose only 1% for the period. □

PROPOSED STANDARD FOR MULTIPLEXING IN AUTOS NEARS DRAFT STAGE

The Society of Automotive Engineers task force on multiplexed data buses for automobiles will meet this week to work out the final details of a proposed multiplexing standard. The draft will cover Class B automotive nets, linking instrument clusters, engine controllers, trip computers, and other equipment [*Electronics*, Aug. 21, 1986, p. 81] on a two-wire, 10-Kb/s bus that uses a multiple-access arbitration protocol. The document will probably leave some loose ends, but it at least represents some consensus, says Frederick Miesterfeld, the Chrysler Corp. official who chairs the SAE subcommittee on vehicle networks for multiplexing and data communications. His committee will consider the proposal late this month, and if all goes well, a final standard could be ready in about a year, he says. □

NATIONAL SEMICONDUCTOR WILL SELL MITSUBISHI DRAMs

Another U. S. chipmaker may reenter the dynamic-random-access-memory business through the back door. National Semiconductor Corp., which quit making DRAMs last spring because of Japanese competition, is now negotiating to sell 256-K DRAMs from Mitsubishi Electric Corp. under a private label. National is already marketing static RAMs of its own design that are made by NMB Semiconductor Ltd. of Japan. In becoming a DRAM supplier again, National would follow the example of Motorola Semiconductor, which quit the DRAM market in November 1985. Motorola began buying DRAM dice from Toshiba Corp. last August, and is now packaging and marketing the parts under its own label. Analysts say the U. S. companies need memory chips so they can offer a full-service package to accounts and distributors. □

CARNEGIE MELLON RELEASES FIRST VERSION OF UNIX-BASED MACH

Carnegie Mellon University in Pittsburgh, Pa., has reached an important milestone in its three-year effort to develop Mach, an operating-system support environment that will run Unix applications on a variety of multiprocessing computers. CMU is releasing the first version of Mach into the public domain after completing tests on a network equipped with Digital Equipment Corp. VAX multiprocessors and more than 100 work stations from Sun Microsystems Inc. and IBM Corp. Now two computer companies are trying to get the software to run on their own multiprocessor systems. Sequent Computer Systems Inc., Portland, Ore., and Encore Computer Corp., Marlboro, Mass., are working with CMU to develop Mach versions for their Balance and Multimax multiprocessors, respectively. □

ELECTRONICS NEWSLETTER

APOLLO TAKES STEP TOWARD UNIVERSAL COMPUTING NETWORK

A big step toward a universal computing network is coming from Apollo Computer Inc.: a distributed-processing environment that allows users to develop and run applications programs on networks built around disparate hardware. Apollo's Network Computing System, announced last week, divides up large application programs and routes subtasks to those computers on the network that can most efficiently execute them. The Chelmsford, Mass., company says this approach will channel the power of highly specialized hardware, such as artificial-intelligence engines, parallel processors, data-base machines, and supercomputers, to users at desktop work stations. The program is based on standard communications protocols and includes a compiler to convert Apollo's new, high-level network language into portable C-language code. □

GE TECHNIQUE CUTS THE COST AND WEIGHT OF THYRISTOR PACKAGES

An all-silicon packaging technique for power devices developed at General Electric Co.'s Corporate Research and Development Center in Schenectady, N. Y., is at least 3 times less expensive, 6 times thinner, and 20 times lighter than conventional technology. Initially used for housing thyristors, the new package consists of a 15-mil-thick coating of arsenic-doped silicon that is in turn enveloped in a glass seal. Conventional packaging uses a thin coating of refractory metal, such as tungsten, but silicon and glass are better thermal conductors. The packages can therefore be used in hotter operating environments, meaning the enclosed devices can handle higher currents. In addition, GE says that with another layer of metalization, the technology, which was developed with funding from the Electric Power Institute, Palo Alto, Calif., could be adapted for use in packaging integrated circuits, particularly in aerospace systems. □

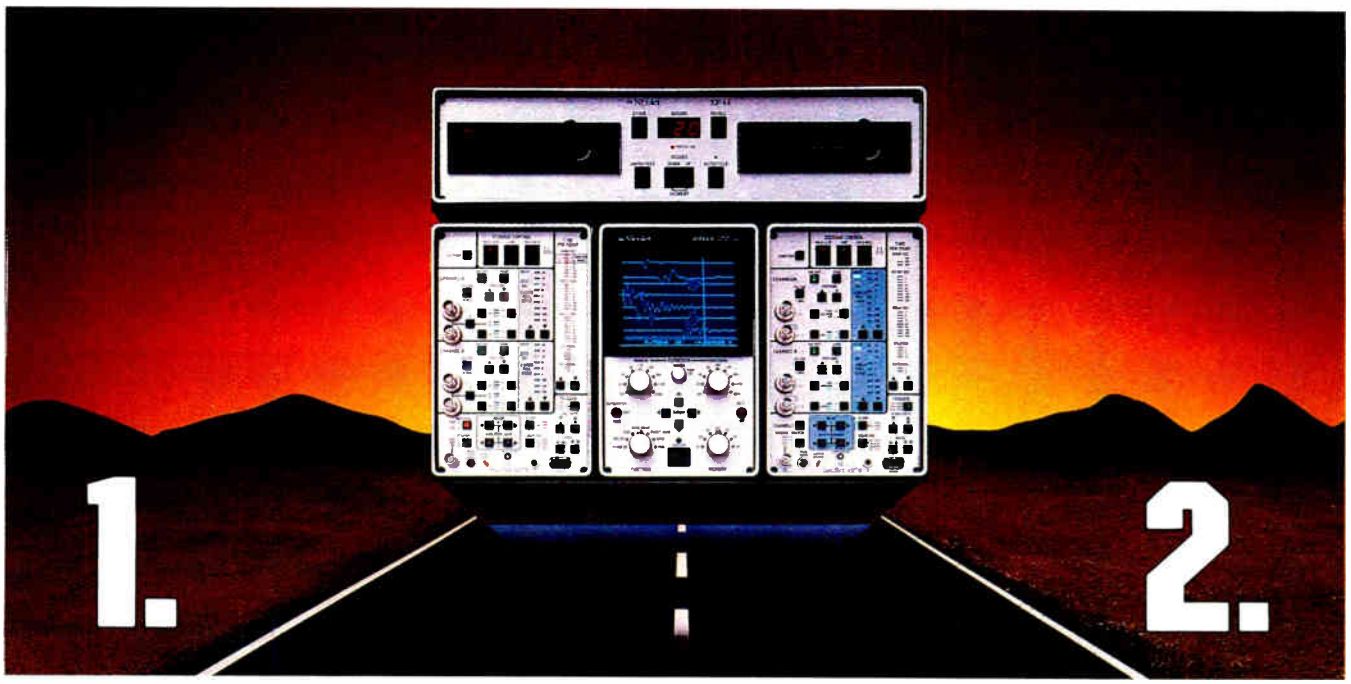
EDS STEPS UP EFFORTS IN SOUTH KOREA AND EUROPE

Electronic Data Systems Corp., the computer-services arm of General Motors Corp., is making an aggressive push to find new foreign markets. EDS and Lucky-Goldstar Group of Seoul, South Korea, will form a computer- and telecommunications-services company called Systems Technology Management. The new firm starts off with a sizable customer base: Lucky-Goldstar and its 20 affiliate companies, which have annual sales topping $10 billion. Earlier this month, EDS formed a joint venture with Ing. C. Olivetti & Co., Ivrea, Italy. The new company, called Integrated Systems Management, will peddle engineering and manufacturing systems in Europe, a market that EDS expects will reach $15 billion in three years. □

AIWA WILL BE FIRST TO FIELD A DIGITAL AUDIO TAPE PLAYER

Aiwa Co. is the first to announce plans to market a digital audio tape player. The $1,224 deck, set for a March release, can play tapes recorded at sampling frequencies of 48, 44.1, and 32 KHz, and record analog or digital material with sampling frequencies of 32 or 48 KHz. But if an attempt is made to record at a sampling rate of 44.1 KHz, the frequency used by digital audio compact disks, the deck automatically reverts to the pause mode and a "copy prohibit" display lights up. The same thing happens when attempting to record from a copy-protected digital tape. Aiwa is buying key components, such as the rotary head and drum assembly and the large-scale integrated circuits needed to process the audio signal, from Sony Corp., which owns more than 50% of the Tokyo company. It will initially sell the unit only in Japan. □

THE FIRST NAME IN DIGITAL SCOPES



TWO DIGITAL SCOPES IN ONE.

The Acquisition.

With sweep speeds from days to nanoseconds and resolution up to 15 bits, the 4094 digital 'scope can capture the most elusive signals. Every plug-in has 16K of memory, viewable trigger set-up and independent pre- or post-trigger delay on each channel. Signal averaging is standard and our latest 10 MHz/12-bit plug-in even offers real time manipulation of the incoming signals. With two plug-ins the 4094 can record four channels simultaneously. Or even monitor two slow signals and capture high speed glitches at the same time. All under computer control or via manual operation: whatever your application demands.

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Expand and examine any waveform feature in detail. Use the dual cursors and numerics to measure the time or voltage of any point. Compare live or stored waveforms with each other or with pre-recorded references. Store signals on disk manually or automatically. Use pushbutton programs to manipulate the data or send it to your computer via GPIB or RS232 interface. Complete your report with a hardcopy plot using the XY/YT recorder or digital plotter outputs.

First Time, Everytime.

Don't miss important data because of set-up errors. From the World's first in 1973 to the latest models, Nicolet 'scopes are easy to use. Find out how they can be the quickest solution to your signal problems. For more information call 608/273-5008, or write Nicolet Test Instruments Division, P.O. Box 4288, 5225 Verona Road, Madison, WI 53711-0288.

Nicolet

Circle 19 on reader service card

Other ASIC companies brag about how many gates they can pack into an array. Or how much logic they can cram on a PLD.

They think it's a big deal if they can shrink 3 boards down to 3 chips.

Let's get serious.

VLSI nails the competition to the wall.

Our tools let you build a chip so far ahead of anybody else's they won't know what hit them.

A single chip with logic, memory, processors, and peripherals.

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Wang, Tandy, and over seventy other leading companies have already used our tools to build hundreds of chips.

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NCUBE developed a chip with over 160,000 transistors that requires no glue logic because the processor, communication logic, and all interface logic are integrated on one chip.

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You can expect chips designed with our tools to work the first time in your system.

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And whether you buy them, lease them, or use them at our design centers, our ASIC team will support you all the way.

If you want the right ASIC solution to your problem, talk to the only place that has them all: Tools. Programmable logic. Gate arrays. Standard cells. Megacells. Compiled silicon. And a complete fabrication facility.

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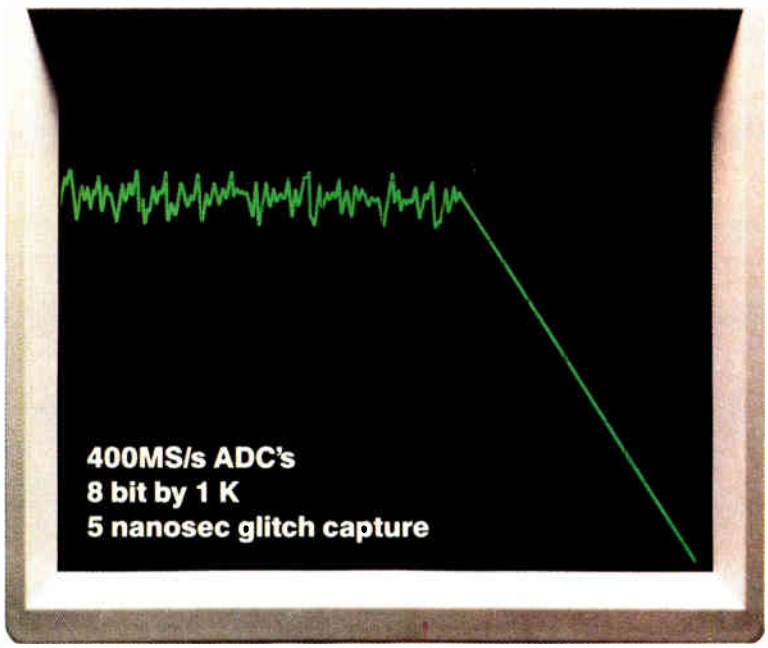
THE ONLY OTHER TOOL THAT COMBINES LOGIC, MEMORY, PROCESSORS, AND PERIPHERALS.



The cost of speed just went down.

Before now, if you wanted a high speed digital storage oscilloscope that didn't sacrifice accuracy, you had to pay an incredibly high price. Not any more. Because Gould's hot new 4070 series is here. Breaking the speed and price barrier with a super fast, super accurate instrument that starts at the unheard of price of $7,990.

2 or 4 channels. Incredible speed and accuracy.

Available in 2 or 4 channels, the 4070 DSO comes with 400 MS/s, 8 bit ADC's per channel. It's also the first portable DSO able to capture single shot signals to 100 MHz bandwidth (3.5 nanosec risetime). Plus Gould's low noise, low jitter design assures high measurement fidelity.

User Friendly.

Even if you've never used a DSO before, you'll find the 4070 easy to operate. As a bench instrument it offers familiar functionality, four reference set ups and a convenient *Auto Set-up*™ feature that automatically determines instrument settings for quick acquisition and display of unknown signals.

Built-in plotter and more.

There's also an optional integral four pen digital plotter for convenient hard copy documentation of test results. Full programmability, including front panel controls and menu selections over the IEEE-488 or RS423 bus. A 170 keypad option that quickly converts it into a powerful signal analyzer. Exclusive triggering capabilities and so much more.

So, if you want a full function DSO with speed, accuracy, and a low price, or information on any of Gould's oscilloscope, logic analysis, or recording products, call 1-800-GOULD-10 or write Gould Inc., Test and Measurement, 3631 Perkins Avenue, Cleveland, Ohio 44114.

GOULD
Electronics

Circle 22 on reader service card

PRODUCTS NEWSLETTER

PERFORMANCE SEMICONDUCTOR CLAIMS FASTEST SRAM

CMOS process specialist Performance Semiconductor Corp. is offering samples of a 64-K-by-1-bit static random-access memory rated at 12 ns access time, which it claims is the fastest SRAM currently available. The chips will find applications in the deep-cache memories of general-purpose computers, the main memories of supercomputers, minisupers, reduced-instruction-set computers, and military systems, says Thomas Longo, president of the Sunnyvale, Calif., company. The chip is made in PACE 2, an enhanced version of Performance Semiconductor's 1-μm, two-layer-metal full-CMOS technology. The company has been building 20-ns SRAMs in the 1-μm technology since last May. The 12-ns SRAM, the P4C187, will be available in the second quarter. The chips will cost about $61 in 1,000-piece plastic-packaged lots. □

TERADATA OPENS ITS RELATIONAL DATA BASE TO PCs AND SUPERMINIS

Teradata Corp. has vastly expanded applications of its relational-data-base computer with a communications processor and software that provide personal computers, work stations, and superminis with direct access to the Los Angeles company's machines. Previously, the DBC/1012 relational-data-base computer linked only to mainframes. Teradata's initial offering includes the Intel 80286/80287-based communications processor, interfaces to IEEE 802.3 Ethernet local-area networks, and DBC/1012 support software. Software for connecting IBM Corp. PCs and compatible machines and AT&T Co. 3B2-series computers running Unix is available now. Software for Digital Equipment Corp. VAX systems is planned for later this year. A communications processor with the Ethernet adapter costs $39,000. DBC/1012 software costs $4,000 per communications processor, and the remote software costs $5,000 for up to 10 PCs and $2,000 for a 3B2. □

PC-CONTROLLED ROBOT CAN REPLACE HUMAN WAFER-LOADERS

Precision Robots Inc.'s PRI-5100 robotic system reduces human contact with toxic chemicals used in chip production by loading and unloading wafer cassettes from plasma-enhanced chemical vapor deposition furnaces. Besides reducing possible health risks, the robot also makes it easier to comply with Class 10 or better clean-room standards. Controlled by an IBM Corp. Personal Computer or compatible machine, the robot can be retrofitted into many existing furnaces in a matter of hours and will maximize furnace throughput. Available now, its base price is $137,500. □

ASIC TOOL KIT ALLOWS MIXING STANDARD CELLS WITH VARIED GEOMETRIES

SMOS Systems, Inc. has radically changed the ground rules of standard-cell design with a tool kit that allows designers to mix standard cells of dissimilar geometries and cell sizes in the same layout. The Compiled Cell Custom tool kit also allows designers to mix compiled cells—complex data paths, random-access memory, read-only memory, and programmable logic arrays—with standard cells and macros. Even the layout of standard microcomputers can be imported into a layout, and the entire layout then automatically placed and routed by the tool kit. With its Compiled Cell Custom system, the company estimates, a custom design now requiring 36 weeks turnaround can be finished in 14 to 16 weeks. The software runs on Intergraph Corp.'s Interpro 32, Digital Equipment Corp.'s MicroVAX II and other VAX computers, and IBM Corp.'s PC AT. The tools are available now. Their use is included in the company's nonrecurring engineering design fees. The cost of a mixed standard-cell/megacell design is less than $75,000. □

PRODUCTS NEWSLETTER

TI's NEW WAVE OF DSPs FEATURES EPROMS AND LARGER ROMS

Texas Instruments Inc. will move to strengthen its hold in the market for low-to-medium performance digital signal processors with a half-dozen additions to its TMS320 family. The Dallas-based company will introduce soon four chips that feature increased on-board read-only memory and follow later this year with two that carry erasable programmable read-only memories. The ROM-based parts have program stores of 4-K words, two-and-a-half times that of current versions, and will cost about $20, low enough to make them feasible for high-volume consumer products, including toys. They will be made available with 200-ns and 160-ns access times The EPROM versions have stores of 4-K by 16 bits, the largest on-chip EPROMs so far, TI officials believe. They will be priced between $40 and $50 in quantities of 1,000 to 5,000 when TI starts delivering them later this year. All six chips have 256 words of random-access memory. □

5¼-in. FLOPPY STORES 2.4 MEGABYTES ON CONVENTIONAL MEDIA

A new floppy-disk-reading technology developed by Y-E Data Inc. boasts formatted capacity of 2.4 megabytes for a 5¼-in. floppy disk—double the 1.2-megabyte formatted capacity of IBM Corp. PC AT disk drives. Just as important, the Tokyo company's new product, the YD-801, maintains compatibility with IBM-compatible drives, controllers, and disks. Although capacity falls short of the 10 megabytes of servo-tracking drives developed by Kodak and Konica [*Electronics*, October 16, 1986, p. 137], it costs only three fourths as much. Because it uses conventional recording media, it should appeal to many users, particularly as backup for hard disks. Y-E Data is using the same technology—details of which it declines to reveal—in 3½-in. drives to obtain formatted capacities of 1.4 and 1.1 megabytes using high-density disks and 720-K bytes using double-density disks. Samples of the YD-801 will be available next month for $280. Volume deliveries—at significantly lower prices—are slated for April. □

CARD TRANSFORMS MICROVAX II TO GRAPHICS WORK STATION

Digital Equipment Corp.'s MicroVAX II computers can turn into stand-alone, high-resolution, color-graphics work stations with the addition of a single plug-in card from CalComp, an Anaheim, Calif., subsidiary of Lockheed Corp. The CGS-4600 subsystem offers 1,280-by-1,024-pixel resolution for applications such as computer-aided design and manufacturing, simulation, and animation. It is available either as the graphics engine alone for $3,995, or as a $6,995 graphics subsystem including color monitor, keyboard, mouse, and digitizing tablet. Shipments will begin in March 1987. □

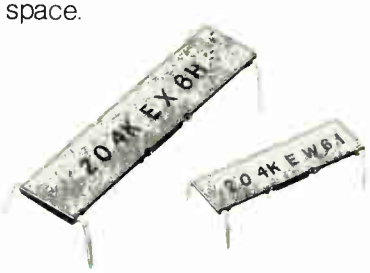
IC LOWERS THE COST OF ROTARY-TO-DIGITAL CONVERSION

The cost of turning rotary motion into digital information will fall dramatically with the introduction of a monolithic resolver/digital converter from Analog Devices Inc. The 2S81 chip will cost $50 in quantities of 1,000, compared with $100 to $600 for systems based on hybrid circuits. The 2S81 can measure position and velocity from single brushless resolvers or synchros. It offers 12 bits of resolution, analog velocity signal linearity to within ±1%, and a maximum tracking rate of 260 revolutions/s. The chip is fabricated with Analog Devices' proprietary BiMOS II technology, which combines low-power CMOS and high-speed bipolar circuitry. The Norwood, Mass., company guarantees repeatability of the converter's position output to within 1 least significant bit, and positional accuracy is rated at 30 arc-min. Samples are available now, and full production is scheduled for the second quarter of 1987. □

NEW

Mil. Spec. IC decoupling

New MICRO/Q II capacitors conform with MIL-C-39014D, STD 202F. Molded construction seals out moisture and humidity. Available in capacitances from .01μF to .30μF. You achieve effective noise control and reduce noise spikes, in conditions from −55°C through +125°C. Mount beneath DIP IC's to save up to 30% board space.



Circle 93 on reader service card

Improve existing board performance

MICRO/Q capacitors can be retrofitted to solve noise problems on existing boards. Because MICRO/Q caps share mounting holes with existing IC pins, no board redesign is required. Effective decoupling becomes a matter of adding one insertion step.

Circle 94 on reader service card

Simplify board layout and get a choice

MICRO/Q ceramic decoupling capacitors share board mounting holes with IC pins. You don't have to waste space on additional holes, as you do for standard caps. Simplifying board design opens up two very attractive options. Add more active devices with increased packaging density in the same space, or design the same package on a smaller board. Either way, you win with MICRO/Q.

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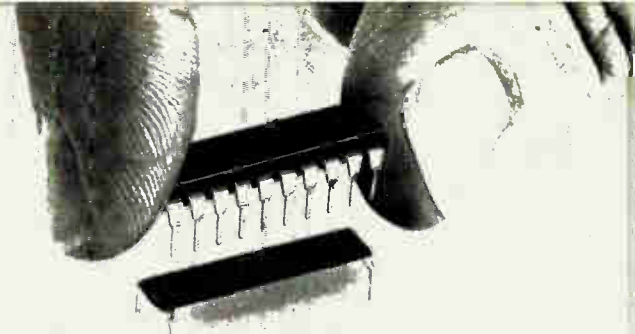

noise problems... space problems...

TOP THIS.

Rogers MICRO/Q® decoupling capacitors reduce voltage noise spikes in IC's, often by as much as a factor of ten. And since they're easily mounted *underneath* the IC, MICRO/Q capacitors conserve valuable board real estate, too. A range of configurations makes MICRO/Q flat capacitors especially effective at reducing noise on:

- 64K RAMS
- Video RAMS
- EPROMS
- Microprocessors
- Bus drivers/buffers
- Other IC's where noise spikes create performance problems
- Boards that need EMI/RFI fix
- CAD/CAM/CAE
- Telecommunications
- Minicomputers
- Printers and copiers
- Single-board computers

Find out how MICRO/Q capacitors reduce noise and provide better board density. Get the full story and a free sample. Call a Rogers MICRO/Q Product Specialist today, at (602) 967-0624.

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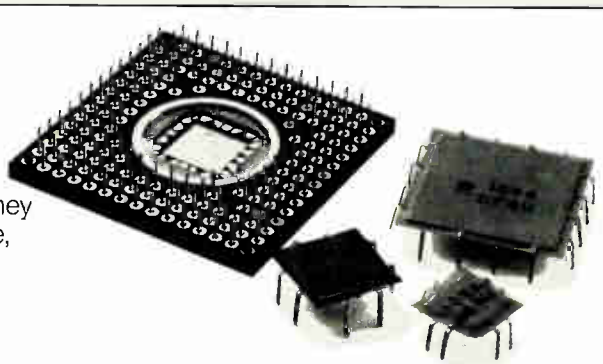
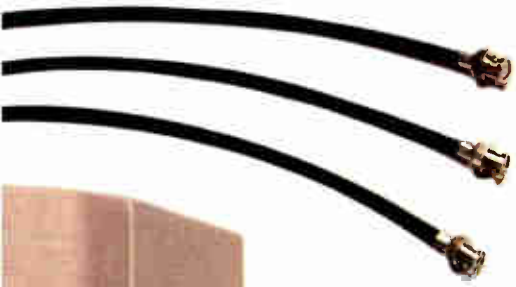
Design noise out of PGA and LCC packages

PGA MICRO/Q capacitors provide effective solutions to noise problems with VLSI PGA packages and LCC sockets. Design effective decoupling on complex multi-layer board layouts by fitting PGA MICRO/Q capacitors under PGA or LCC sockets. They occupy no additional board space and provide the low-inductance, high-frequency decoupling required by today's VLSI packages. Available in a range of pinout configurations.



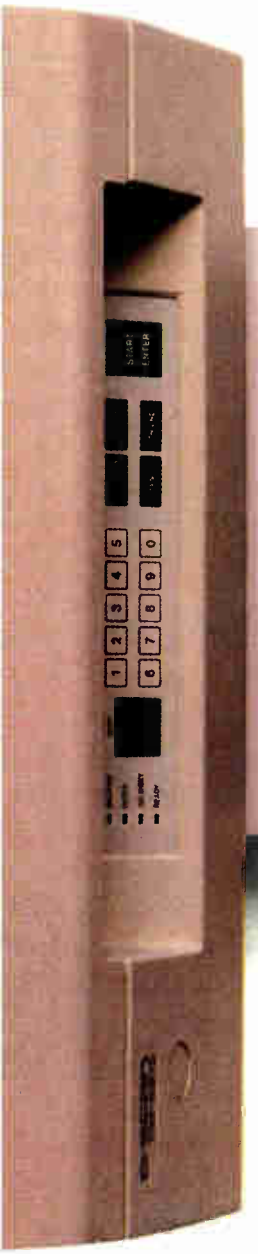
Circle 97 on reader service card

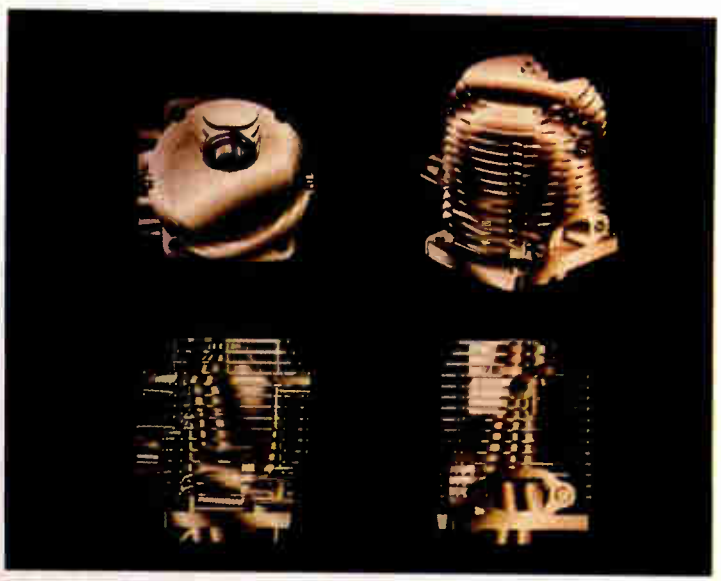
● Both parallel and RS-232 interfaces are supported by a wide selection of software.



● Easy video interfacing—over 150 interfaces are supported. No need to write software.

● Accurate shading for realistic, detailed solids; work with 4,912 colors.





● Local intelligence: video interface lets you rotate, change colors and scale with front-panel controls.

● Crisp, clean lines for highly detailed drawings.

No Other Color Hardcopier Can Make These Points.

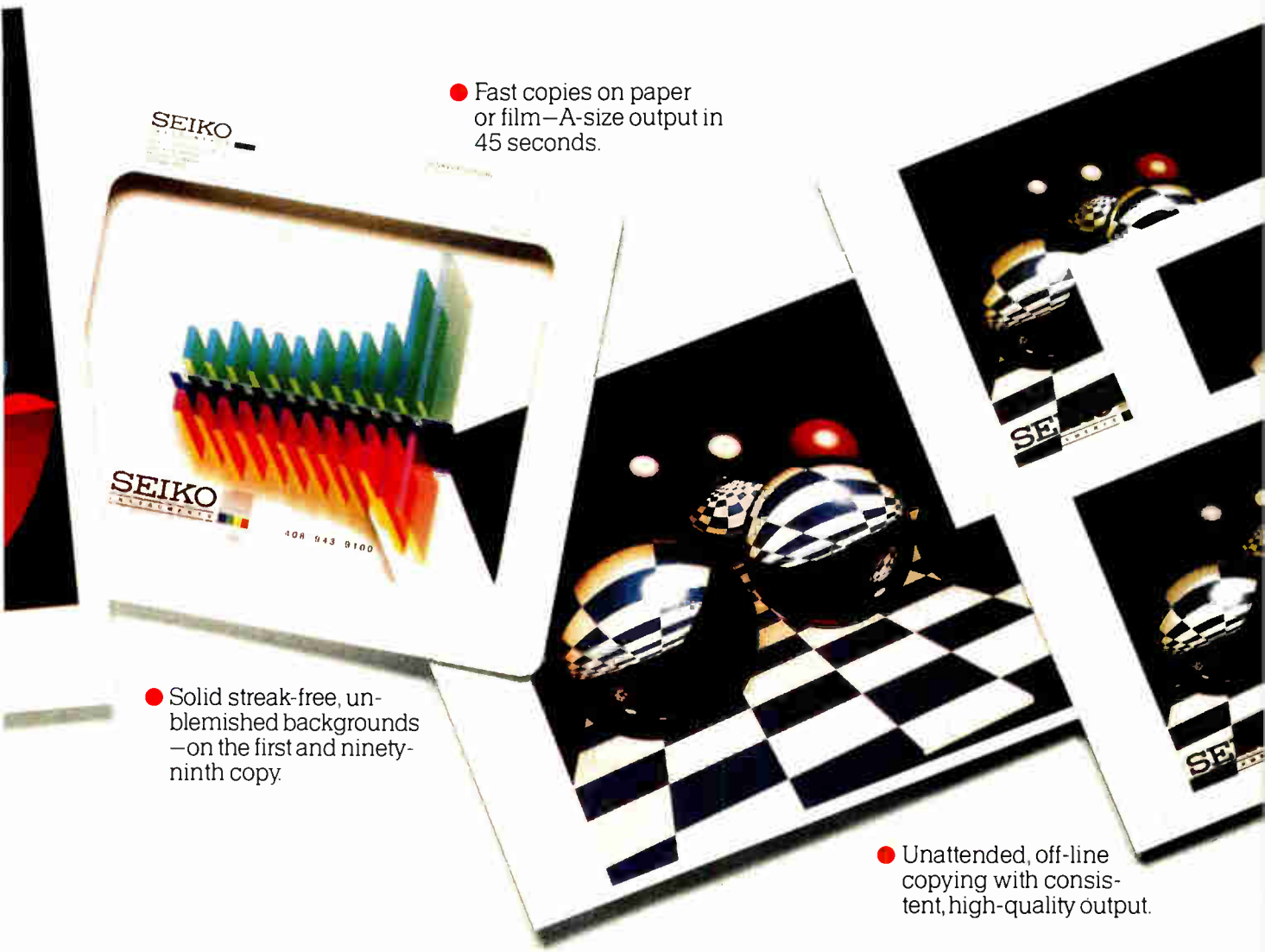
The CH-5300 gives you fast copies. Sharp lines. Realistic gradation and shading. Bright, rich solids. Consistent backgrounds. Built-in intelligence. Easy interfacing to the broadest range of video or parallel sources. And proven reliability.

Plus, with our new multiplexor you can turn your color hardcopier into a shared resource; connecting up to four different input sources at once.

So look into the Seiko CH-5300. You'll see that no other color hardcopier can make these points.

Call Martin Nelson at (408) 943-9100 today.

SEIKO INSTRUMENTS



- Fast copies on paper or film—A-size output in 45 seconds.
- Solid streak-free, unblemished backgrounds—on the first and ninety-ninth copy.
- Unattended, off-line copying with consistent, high-quality output.

Circle 27 on reader service card

To know the environment of your power source is the first step to noise countermeasures

NDR-544 has broadened the power line monitoring range.

Only by connecting the unit to a power line (single phase or 3-phase, AC/DC line), you can obtain accurate data on the power line such as voltage fluctuation, frequency fluctuation and superimposed impulse noise. In addition, the unit catches an abnormal value beyond the threshold and prints data on such an abnormal state.... "When the abnormal value occured", "How long it continued" and "Fluctuation value". The NDR-544 is the latest model with upgraded measuring functions designed to extensively monitor various power line disturbances. You can immediately check and monitor the environmental conditions of electronic devices before installing them and can also clear up the cause of troubles.

Features

- AC voltage fluctuations of single phase and 3-phase can be monitored.
- ON-OFF at 4 places other than power line can be monitored. (Event function)
- Time at which abnormal state occurs and recovers is printed at a unit of 1/100 second or more.
- Editing function enables user to obtain the whole day's accumulated data.
- Clock, threshold and measurement data are backed up by battery.

Main specifications

- Voltage fluctuation measuring range : 600 V AC max.
  Two ranges; 0~±10V DC, 0~±100V DC
- Frequency fluctuation measuring range : 45.0~65.0 Hz
- Impulse voltage measuring range : ±2500 V (Simultaneous monitoring of positive and negative)

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Circle 28 on reader service card

Electronics

BALLISTIC DIODE BURSTS THROUGH FREQUENCY CEILING

HOT-ELECTRON DEVICE SWITCHES AT TERAHERTZ SPEED

URBANA, ILL.

Move over, Impatt diode, Gunn diode, and tunnel diode: here comes the heterostructure hot-electron diode. If its developers at the University of Illinois are right, the device has the potential to produce the highest switching frequency of any diode mechanism yet developed and could open the way to now-unexploited frequency bands.

"What we've got is a new diode phenomenon," says James J. Coleman, one of five researchers involved with the project at the University's Center for Compound Semiconductor Microelectronics in Urbana. Theoretical switching speed for the new diode type could be as fast as 200 femtoseconds, which means it could be used in microwave oscillators with frequencies in the terahertz range, Coleman says, with an output of 25 mW or more. That's more than 10 times the frequency of today's fastest oscillators, based on Impatt, Gunn, and tunnel diodes, which peak out around 100 GHz, he says. Also, the new diode exhibits gain as high as 50 dB at 15 Ω.

HOT PROPERTIES. The speed comes in part from a phenomenon involving thermionic emission—so-called ballistic propagation of "hot," or highly energized, electrons. The device is a cousin to experimental ballistic transistors being developed at IBM, AT&T Bell Laboratories, and elsewhere. The Illinois diode depends on similar principles and is built with a similar epitaxial gallium arsenide–aluminum GaAs structure.

But Coleman says the mechanism of the two-terminal diode device is different from that of ballistic transistors, which are three-terminal devices that rely on hot electrons injected through thin semiconductor layers to switch five to six times faster than other transistors. By contrast, the Illinois diode relies on the energy band-gap between a lightly doped GaAs layer and an AlGaAs layer to get the necessary negative differential resistance for high-frequency oscillation between two conduction modes.

The Illinois researchers use metal-organic chemical vapor deposition to build a sandwich of lightly doped GaAs atop an undoped or lightly doped AlGaAs layer on a heavily doped GaAs substrate.

A negative bias causes electrons to propagate through the diode structure in one of two conduction modes. At low voltages, electrons traverse the top GaAs layer at close to the conduction-band minimum but encounter a barrier at the heterojunction with the AlGaAs, which has a wider energy band-gap than the GaAs. In this mode, there is a significant voltage drop, and resistance is high across the AlGaAs region; current through the device comes principally from quantum-mechanical tunneling. Though electrons at low fields can't get over the barrier, some tunnel through the AlGaAs.

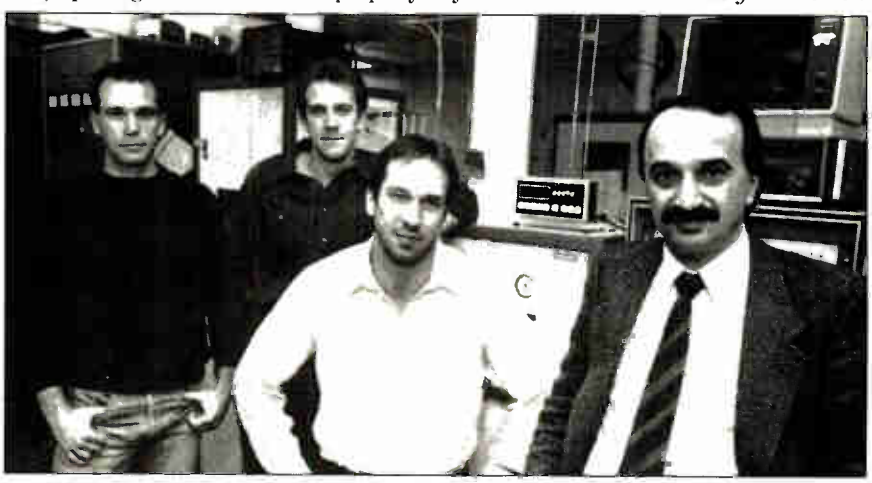
FLYING BY. However, when the voltage is increased, the higher electric fields that are created heat the electrons to energy levels sufficient to cause thermionic emission over the barrier, causing a dramatic switch in the conduction mechanism. "As you increase the voltage, suddenly the fields become high enough that by the time an electron reaches the AlGaAs layer, it's received enough energy from the field to be higher in energy than the barrier, and it just goes flying right by," Coleman explains. As a result, voltage drop and series resistance across the AlGaAs region become negligible, and the diode switches to a conduction mode that is based on thermionic emission.

By placing the diode in a properly tuned microwave cavity and applying the proper bias, microwave oscillators of extremely high frequency can be built, Illinois researchers say. The structure is inherently fast, since its intrinsic speed is limited mainly by the electron transit time across the layers, Coleman says.

Illinois researchers have built 20 to 30 versions, using varying doping levels and thicknesses down to about 900 Å. "We made the layers 2,000 Å thick and it still shows the switching mechanism," Coleman says. But for optimum efficiency, the AlGaAs layer must be less than 1,000 Å to allow adequate tunneling in the low-field conduction mode. Switching voltages vary according to the GaAs/AlGaAs sandwich characteristics but typically have been around 10 V. In order to enhance the switching effect, the Illinois researchers have cooled the devices to 77 K or lower. But, Coleman notes, "We can't see any reason why it won't work at room temperatures."

The researchers have not yet measured the new diode at oscillation frequencies beyond "a few gigahertz," Coleman concedes. But they have calculated that oscillation frequencies could theoretically hit 5 THz with devices built with 50-Å GaAs and AlGaAs layers, Coleman notes. In fact, he says that the technology could be ready for real-world applications within just one to two years.

–Wesley R. Iversen



TEAM. Members of the University of Illinois research team that developed the diode are, from the left, Jack and Ted Higman, Jim Coleman, and Karl Hess. Not pictured is Mark Emanuel.

DEC MARCHES ON: NOW A DESKTOP VAX

BOSTON

Cover the nameplate and what was announced in Boston last week was just another 1-million-instructions-per-second work station for about $10,000. But then tear off the cover and get ready for the impact of the first desktop VAX computers from Digital Equipment Corp.

That the fully VAX-compatible machines—the VAXstation 2000 and the multiuser MicroVAX 2000—will have significant impact is apparent from DEC's announcement that it begins public marketing of the products with orders in hand for 5,000 units. Shipping in April, the small computers will also have a big head start on IBM's midrange 9370, which will not be fully ready to compete until later this year. But whether the machines will cause major disruptions in the work-station market per se is another matter, and one that depends heavily on the importance customers attach to the nameplate on the computer.

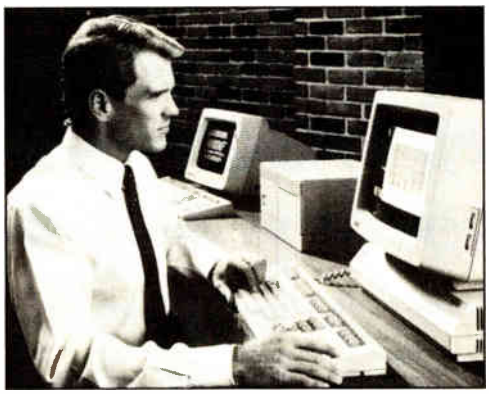
The new computers clearly continue the unprecedented pace of major product announcements that DEC has maintained for the past two years. They also represent an historic milestone in that the power of the first refrigerator-sized VAX introduced a decade ago has now been compressed into a box smaller than an unabridged dictionary.

To create the 2000 line of computers, DEC downsized a MicroVAX II into a package measuring 1 ft by 1 ft by 5 in. and cut the price in half. This required reducing the system's electronics from four boards to just one—which carries more than a dozen new custom CMOS chips, all designed and built by DEC.

DEC's most extensive use of surface-mount technology to date helps pack 4 megabytes of memory into a space 4 by 7 in. And power consumption is half that of the MicroVAX II machines, falling to 160 W for the 2000 line.

BROAD LINE. The new products now stretch DEC's VAX computer family from an entry-level desktop MicroVAX 2000 priced at $11,100 to the largest clustered VAX 8978 at nearly $4.9 million. Included in the purchase price of both new 2000s is a one-year warranty providing on-site hardware support and telephone software support.

The rapidly expanding VAX line—with the appeal of hardware compatibility, extensive applications, and software portability—is enabling DEC to build market share at the expense of other minicomputer vendors and its primary rival, IBM, whose various products run several incompatible operating systems.



VAX ON A DESK. The low-cost 2000 line reduces the VAX to about the size of an unabridged dictionary.

Ironically, the computers most immediately affected by the new hardware announcements will be other VAX products. Hardest hit will be the two-year-old VAXstation II, which the company says will "fade away" as customer attention shifts to the VAXstation 2000. Similarly, the low end of DEC's MicroVAX II business will now migrate to the MicroVAX 2000, at about half the cost. The higher-performance VAXstation II/GPX should continue to attract customers because it offers eight-plane color, whereas the color version of the VAXstation 2000 will provide only four-plane color. A diskless, monochrome version of the VAXstation 2000 is priced at $10,500.

The VAXstation 2000 is being thrust into a burgeoning low-end work-station market. Dataquest Inc. estimates the two leading vendors, Apollo Computer Inc. of Chelmsford, Mass., and Sun Microsystems Inc. of Mountain View, Calif., derive more than 40% of their revenue and 60% of their unit sales from machines priced at less than $20,000. For example, Apollo reports selling 12,000 of its year-old low-end Series 3000s.

But the work-station market is one in which stand-alone product performance—as opposed to a vendor's multisystem solutions—retains great importance. And in one-to-one price/performance comparisons, the leading vendors believe they can more than hold their own against DEC's low-end VAXs.

"We knew about the products for quite some time," says Ed Zander, vice president of corporate marketing at Apollo, "and our business has gotten much better the last few quarters. We would have seen some impact if the product was so exceptional."

Similarly, Sun doubts that DEC's standing in the work-station market will improve. "DEC hasn't announced a new CPU since March 1985, with the MicroVAX II. I'm surprised they haven't kept up in terms of CPU performance," says John Hime, director of product marketing for Sun's work-station division.

But it is also clear that the engineering departments of many DEC customers, in need of a low-end work station, have been shopping at Sun and Apollo for their machines. Now, given the trend to company-wide standardization of computers, those engineering departments will be under pressure to look closely at the low-cost VAXs to tie in with DEC machines elsewhere. *–Craig Rose*

CRAY AIMS AT THE LOW END WITH ITS OWN CRAYETTE

MINNEAPOLIS

In a major strategy shift, supercomputer leader Cray Research Inc. moved last week to stake out new territory at the low end of supercomputing. The $2.5 million price on Cray's new entry-level X-MP/14se chops 37.5% off the $4 million price of Cray's previous low-end single-processor system. And the new system could provide heavy competition for Cray's Twin Cities rival, ETA Systems Inc., of St. Paul, which plans around midyear to bring out a $2.5 million entry-level version of its own ETA^{10} supercomputer.

Cray also announced a new field-upgrade capability for its current X-MP line, a new X-MP model priced at $8.5 million, new two-processor and four-processor versions of its top-end Cray-2 line, and a new high-speed data channel to allow 100-megabyte/s communication among Crays, other computers, and work stations. The company also reduced prices from 3.4% to 25% on four existing models, including its four-processor Cray-2, whose price tag drops from $17.6 million to $17 million.

But Cray's low-end move caused the most stir. "I'm a little surprised that [the X-MP/14se] is that low-priced," says Gary Blauer, an analyst with Min-

neapolis investment house Dain Bosworth Inc. Cray has preferred to focus on large, fast supercomputer systems and has shunned the emerging class of minisupercomputers, or so-called Crayettes, built by firms such as Alliant, Convex Computer, and Scientific Computer Systems. Prices of those systems generally start at around $1 million. But demand for used Cray systems is running high, reflecting increased customer cost-consciousness. And, Blauer says, "I think Cray felt it couldn't let the low end go uncontested any more, and that it had to capture customers at an earlier entry point."

That's close to the mark, says Robert H. Ewald, Cray's vice president of commercial marketing. Cray rates the new machine at about 80% of the performance of a standard, field-upgradable X-MP/14, at less than half the 14's $5.5 million tag. Other X-MPs offer up to 16 million 64-bit words of memory, compared with the X-MP/14se's 4 million words, and unlike other X-MP systems, the 14se will not be field-upgradable.

But for many first-time customers whose supercomputing requirements are not extensive, the 14se may be just the ticket, Ewald says. "People who might otherwise be buying one or two of the Crayettes will have to seriously consider this machine," he notes. Ewald claims the new low-priced Cray has been in the works for about a year, and that its introduction is unrelated to plans for the entry-level version of the ETA[10], known inside ETA as the Piper [*Electronics*, Nov. 13, 1986, p. 22]. But Ewald also says that, based on reports from customers, the ETA system "might have about the same price, but it will have a performance factor two or three times less than our machine."

By contrast, Gary Smaby, an analyst at Minneapolis investment firm Piper, Jaffray & Hopwood Inc., notes that reports he's heard would put expected Piper performance beyond that of Cray's X-MP/14se. "But the price point [on the 14se] is strangely similar," Smaby allows.

An ETA spokesman declines to comment on the latest Cray moves but confirms that Piper target pricing is around $2.5 million. It is to be introduced around midyear, the spokesman says, but performance characteristics have not yet been set. *–Wesley R. Iversen*

DATA COMMUNICATIONS

AT&T GETS A HEAD START ON ISDN

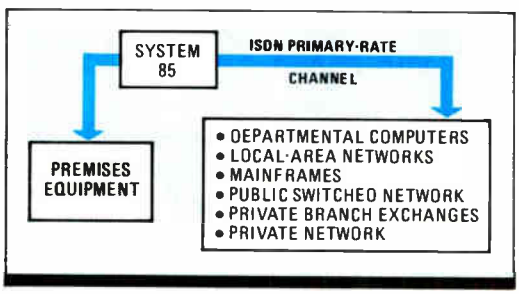
WASHINGTON, D. C.

AT&T Co. moved to take a leading position as a supplier of equipment for integrated services digital networks last week, when it unveiled software enhancements to the System 85, its high-end private branch exchange. The company claims to be the the first supplier of an on-premises PBX compatible with ISDN's 1.544-Mb/s primary rate.

The new software, called PRI for primary rate interface, will be available in December and will permit System 85 users to select a service—such as WATS—on a call-by-call basis, which in many cases will reduce the total number of lines required. Without the interface, lines have to be dedicated to specific services. AT&T has yet to equip its own network to handle the ISDN primary rate, but it expects to offer its first implementations at the end of the year. "We expect to be in 60 metropolitan areas by 1989," says Jack P. Bucter, vice president of product management and business development at AT&T's Business Market Group.

ISDN SUPPORT. The AT&T announcement, made at the Communication Networks Show in Washington, has extra significance as the company's first tangible support of ISDN. It proves the company intends "to be the leader in the ISDN world of services," says Bucter. Industry representatives at the show agreed that AT&T was first with an announcement of a PRI product for ISDN but added that others were working on similar products and could have them on the market soon after AT&T's.

In addition to the interface for the primary rate, which is for heavy users of telecommunications services, AT&T promises one that can handle the basic rate, for the 144-kb/s channels chosen by smaller users, when the ISDN specifications for it are ready. With the newly announced primary rate enhancement, System 85 users will be able to switch over to ISDN services as these become available.



CHOICES: System 85 will permit a call-by-call choice of services. At present, dedicated lines are needed.

The 1.544-Mb/s primary rate is broken down into twenty-three 64-kb/s B channels, each carrying either voice or data, and one 64-kb/s D channel that is used for signaling and performance monitoring. Businesses can use the D channel to gain such capabilities as station identification, where a caller could be identified by the number from which he or she is calling. The new System 85 interface supports bit-oriented signaling, for current 1.544-Mb/s lines, as well as message-oriented signaling for the upcoming ISDN. Among the data-transport modes supported are 64-kb/s clear channels, 56-kb/s channels compatible with Dataphone Digital Service, and data-communications channels at rates of 19.2 kb/s and lower.

AT&T also announced several other software products for System 85 users at the Communication Networks Show, including an automatic call-distribution system for administration and reporting; an upgrade to the Unix-based, centralized system-management application; and a call-detail recording utility.

–Terry Feldt

DISTRIBUTION

WILL NEW BUYING TREND BOOST 1987 CHIP SALES?

LOS ANGELES

U.S. component distributors, the chip industry's early-warning system, are picking up signs of a significant change in semiconductor buying patterns that could spell good news for American distributors and chip makers.

Well-placed distribution sources see signs that manufacturers of IBM Corp. PC clones on the Pacific Rim—South Korea, Taiwan, Hong Kong, Singapore, Indonesia, and Japan—have started to buy hard-to-get Intel Corp. 80286 microprocessors and related chips from U. S. distributors. This is a reversal of the usual buying pattern, in which U. S. personal-computer makers procure cheaper parts offshore and then assemble computers stateside.

"I haven't heard that, but it makes

sense when you think about it," says one close follower of the semiconductor scene, financial analyst Andrew J. Neff of Montgomery Securities Inc. in San Francisco. If the sales to offshore clone manufacturers are more than a brief blip, caused by a temporary shortage, it could turn out to be a boon for overall U.S. semiconductor output, he says. "This could be a very good piece of business," Neff says, and predicts that the trend could raise the 1987 industry growth a few percentage points above his projected 12%.

Driving these purchases is soaring demand for the 16-bit 286 processors, which Intel reportedly is finding hard to meet. The Santa Clara, Calif., chip manufacturer turned out more than 1 million devices in the fourth quarter of last year, its executives say, and the company is maintaining that rate.

But the main customer, IBM Corp., and other U.S. manufacturers are snapping up the chips faster than Intel and its licensed second-source suppliers—Advanced Micro Devices Inc., Siemens AG, and Fujitsu Ltd.—can turn them out. The result is lead times that are stretching longer and longer—and leaving any other potential customers high and dry.

Therefore, the foreign producers of these clones have no one to turn to except the U.S. distributors that handle the chips and can sell them in smaller quantities, typically less than 1,000 pieces. And in another departure, the new customers, who don't usually buy from distributors, are buying through third parties.

Clone makers are being forced to use third parties to get chips

Perhaps the first top distributor to discern what is starting to happen is Pete Heller, chairman of Pioneer-Standard Electronics Inc. in Cleveland. "A lot of the product [that is moving through distribution] is being sold to independent purchasing companies or to some buying agents who represent the offshore clone makers," he says. "This is a relatively new wrinkle in the business.

Intel, as yet, has no evidence that distributor sales to offshore customers are increasing, says a spokeswoman. But Intel has lagged in tracking parts destinations for its chip shipments, she adds, because overall demand has been heavy.

An executive at distribution sales leader Hamilton/Avnet Electronics of Culver City, Calif., confirms the trend, although he says few of the offshore companies are known. "It's tough to identify, since a lot of it comes from the local schlock houses [speculative buyers that are noted for selling scarce products quickly at a profit]. But we definitely see activity starting to churn." "

Top executives at two other Southern California distributors with Intel franchises say they cannot yet verify any significant offshore 286 purchases. But they agree that such an upswing may well be in the offing. "It could be, since the 286 is taking off," says W. Donald Bell, president of Ducommun Inc.'s Kierulff Division in Cypress, Calif. And Charles M. Clough, president of Wyle Laboratories Inc., whose Electronics Marketing Group is at Irvine, Calif., sees the move to buying from distributors as "really a last resort for Asian companies." *–Larry Waller*

DISK DRIVES

ADAPTEC UPS THE ANTE IN CONTROLLERS

The eternal battle for greater disk capacity at a lower cost has spurred Adaptec Inc. to make a good approach better. The result is two controllers from the Milpitas, Calif., company that double the capacity of a disk drive and add a potent new weapon to the business. However, they also present challenges to both the system integrator and the disk-drive maker.

The new controller is based on the popular IBM-developed 2,7 run-length-limited, or RLL, code, used by Adaptec last year in a controller that stored 50% more data on a disk drive. The company increased RLL's density to 13,000-bit/in. from 9,000, and developed advanced RLL. A version supporting two Winchesters costs $160; one that also supports two floppies is $195.

But now the system integrator faces the fact that doubling the capacity of a 20-megabyte Winchester pushes the drive over the 32-megabyte limit that personal-computer operating systems impose on hard-disk storage. "We've addressed this problem by developing an [input/output] driver that can support multiple logical drives," says Edward Turner, Adaptec's director of product marketing.

For the drive manufacturer, the controllers are a mixed blessing. There are three problems: the drive must be built to operate with the controller, and it will be priced slightly higher than the conventional drive; a wider variety of drives must be in inventory; there is the danger of drives being misused by the system integrator.

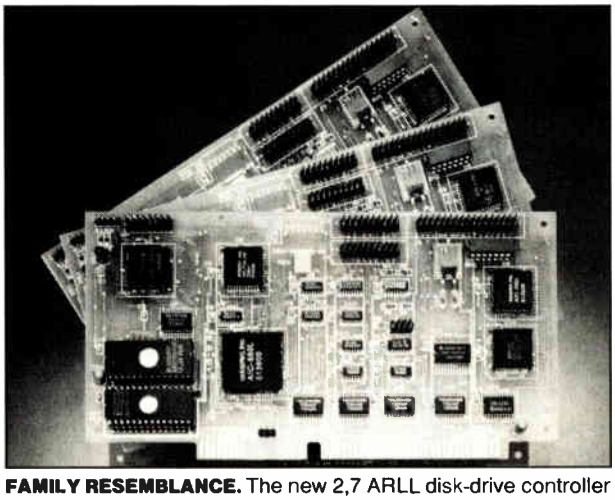
MORE CHANGES. "Building a drive to handle RLL-encoded data required a relatively simple change to the read/write channel," says Carter O'Brian, marketing manager at Seagate Technology Inc. of Scotts Valley, Calif. But increased bit density means more changes, he says.

"Three changes are required to a standard ST506/412 drive to work with the new Adaptec ARLL controller," says Jack Clemens, vice president of engineering at LaPine Technology Corp. in Milpitas, Calif. "First, the drive must use thin-film media to handle the higher bit density. Next, the flying height of the head needs to be lowered to achieve a higher signal-to-noise ratio. Finally, the read/write channel has to be tuned for the higher bandwidth required by the higher data transfer rate of the ARLL controller."

Though most 5¼-in. and 3½-in. drives already can handle the three requirements, disk-drive makers must now widen their inventory. "We already support two different 3½-in. products," says Clemens. "The ARLL will mean supporting yet another."

And then there is the matter of misuse. A system integrator wanting to cut cost could use a standard drive with an RLL or ARLL controller. The drive will probably work—for a while. When it fails, the drive maker will be blamed.

Still, drive makers are getting ready. "We're waiting for a sign from the market to go ahead with ARLL," says LaPine's Clemens. *–Jonah McLeod*



FAMILY RESEMBLANCE. The new 2,7 ARLL disk-drive controller nestles between its older brothers, the ESDI (top), and the RLL.

IBM IC SPEEDS UP OPTICAL DATA LINKS

The lack of reliable and inexpensive hybrid optical receivers has thus far prevented companies from linking computers, work stations, and other peripherals in high-speed fiber optic networks, but IBM Corp. is moving to change that. Researchers at the company's sprawling Thomas J. Watson Research Center in Yorktown Heights, N. Y., have developed a tiny integrated receiver "chiplet" capable of accepting data at up to 3 gigabits/s—more than twice as fast as any previously reported device of its kind, the company claims.

The first in a series of experimental ICs designed for short-distance data communications, the 1-by-2-mm gallium arsenide device consists of a photodetector and a preamplifier. The chip, which is still in the design stage, will eventually contain a post-amplifier and comparator, thereby fully integrating what can now only be produced as a hybrid.

FINDING THE KEY. The integration of a photodetector and logic on a single chip is a key technological breakthrough, says Dennis Rogers, the physicist who developed the device. Previous attempts to implement a detector on a logic circuit failed, since the high-temperature processing of the logic circuits caused surface trapping in the detector. That caused a low-frequency gain that made it difficult to recover the low-level, high-speed signals from the photodetector—rendering the entire circuit useless.

The interdigitized metal/insulator/metal photodetector design IBM chose had been proven effective in conjunction with logic circuitry by researchers at Fujitsu Ltd. of Japan, among others—but only when built with low-temperature processes that offered lower performance than would be acceptable for the applications IBM is looking at.

But by selectively doping the detector portion of the GaAs chip with silicon, Rogers found that the photodetector was able to withstand high processing temperatures without suffering any breakdown in performance. Because of this, both detector and logic can be built using the same refractory-gate, ion-implanted MES FET process—and that can mean a savings in manufacturing costs.

According to Dean Eastman, vice president for logic, memory, and packaging, the need to integrate optoelectronic devices is of greater importance in data communications—where speed, cost, and reliability are of paramount concern—than it is in telecommunications, where bandwith and the ability to

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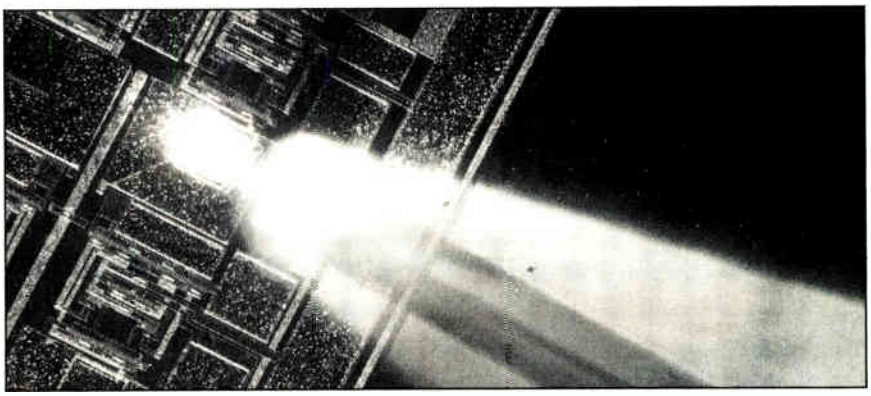
HEWLETT PACKARD

DS15603B

Circle 35 on reader service card



CHIPLET. IBM's integrated receiver measures 1 by 2 mm.

send signals over vast distances supersede other concerns.

"For computer applications, we're not pushing bandwidth," Rogers says. Data links are generally short, so receivers need not be so sensitive nor transmitters so powerful as their telecommunications counterparts. Those devices can be bulkier and more expensive, as long as they can transmit over great distances and thus limit the need for remote signal repeaters, which are expensive to maintain.

The IBM chips are being considered for use in connecting mainframe processors, as well as for networking mainframes and peripherals in networks more than 1,000 times faster than T-1 lines. They could eventually be used for board-to-board communications as well.

Among the other chips under development is a transmitter IC, which represents a greater technological challenge. "We're doing this in steps, and the next step is to integrate a laser and transmitting circuitry on a chip," Eastman says. "It's a harder job—it's more difficult to incorporate a laser on a chip than it is a photodetector." *–Tobias Naegele*

PACKAGING

HOW TO MAKE PIN-GRID ARRAYS AT HALF THE COST

PALATINE, ILL.

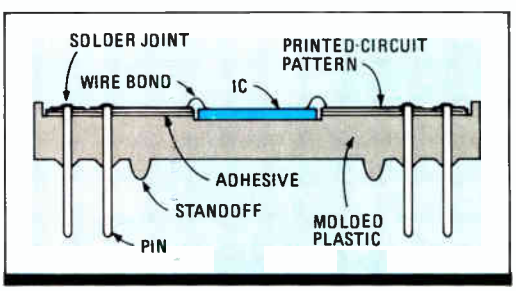
In low-cost semiconductor packaging, the accent is usually on the first two words. That's why Interconnection Solutions Inc. figures it's ahead of the field with a packaging technique intended to cut in half the cost of printed-circuit pin-grid arrays.

The year-old Palatine, Ill., company, which specializes in thermoplastic packaging materials, has managed to cut the number of operations in building a low-cost array by molding the pins in at the same time the package's body is molded, and by using an extremely thin printed-circuit substrate for its plated interconnection (see figure). The standard method involves first making a pc board, then drilling holes in it, press-fitting pins, and finally soldering in the pins. In full production, pin-grid arrays made by the new method should cost about 2¢ a pin instead of about 4¢ for the pc-board version, says Interconnection Solutions.

The potential is enticing. Today, the pc pin-grid array has only about 1% of the total pin-grid array market of $40 million to $45 million. But industry watchers predict that, spurred by increased uses of very large-scale integrated circuits, its share will grow to 50% by 1990.

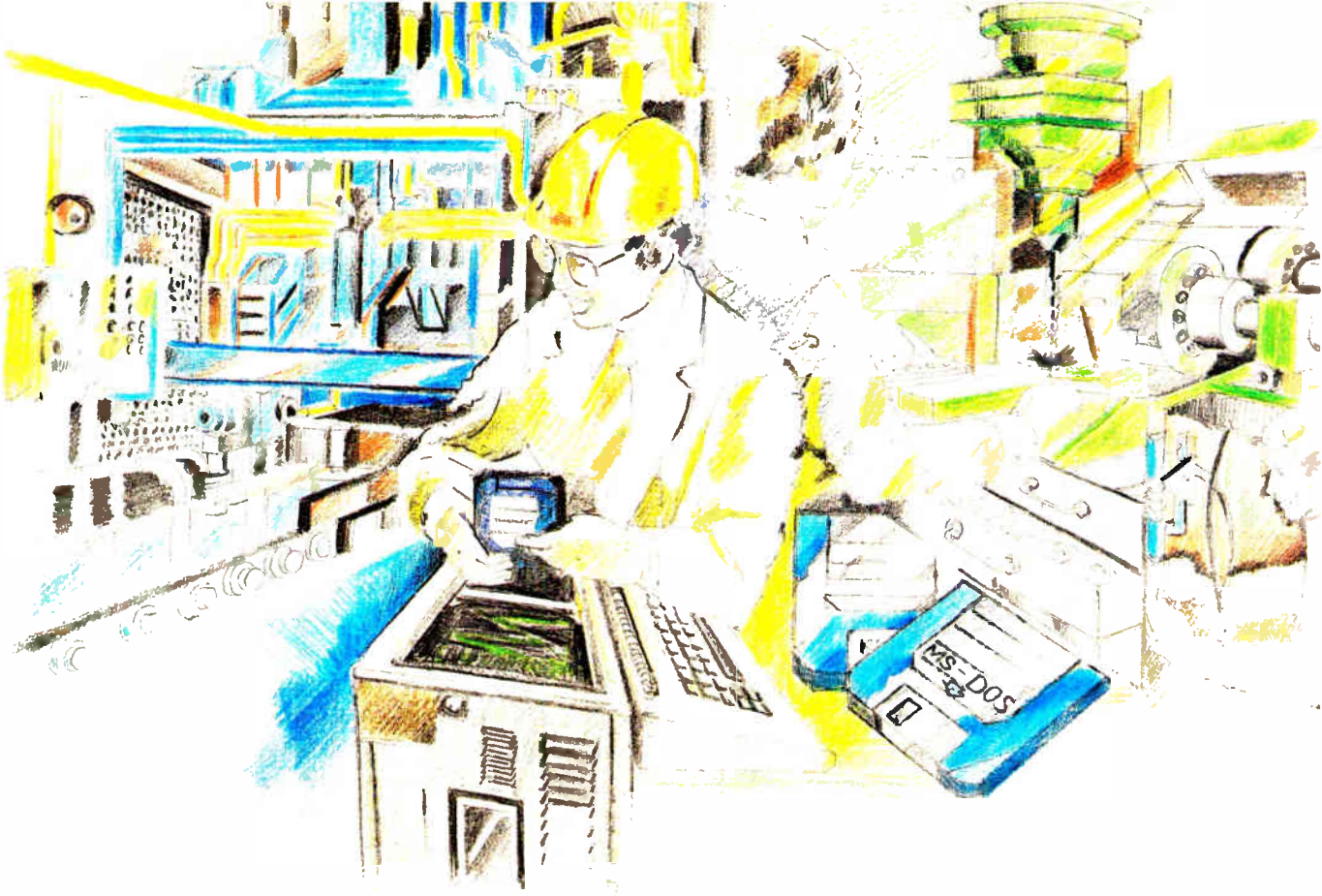
That steep curve is typical of a sector that is as dynamic as any in electronics. The original pin-grid array in the early 1970s was a square, multilayer ceramic package with a grid of pins on 100-mil centers on the bottom. It was heavily used in military equipment and in packages with more than 84 pins that require hermeticity. Then, as VLSI chips went commercial, the lower-cost pc array evolved, based on a small, square, single or multilayer pc board with pins.

Bill Werther, a founder and engineering vice president of Interconnection So-

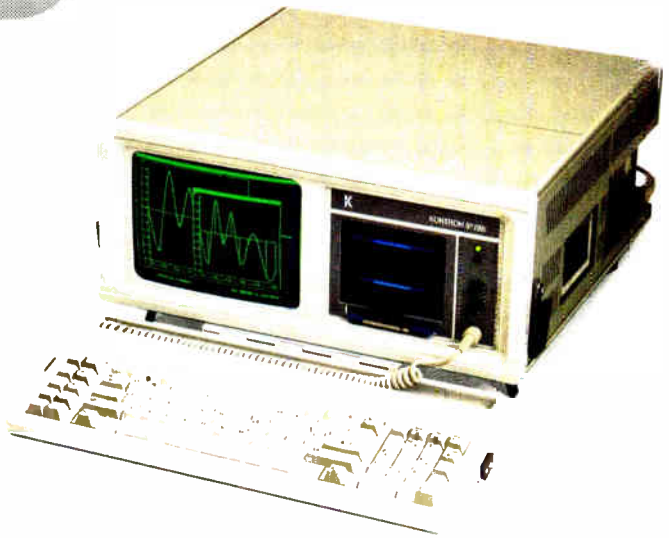


KEEPING IT SIMPLE. In the new package, the pins are molded in at the same time that the body is molded.

COMPUTERS



KONTRON IP286, the portable MS-DOS computer for industry



Down with dust!

This is particularly meaningful for computers in industry. The dust, vibration and temperature of a production environment are just too much for a "commercial computer".

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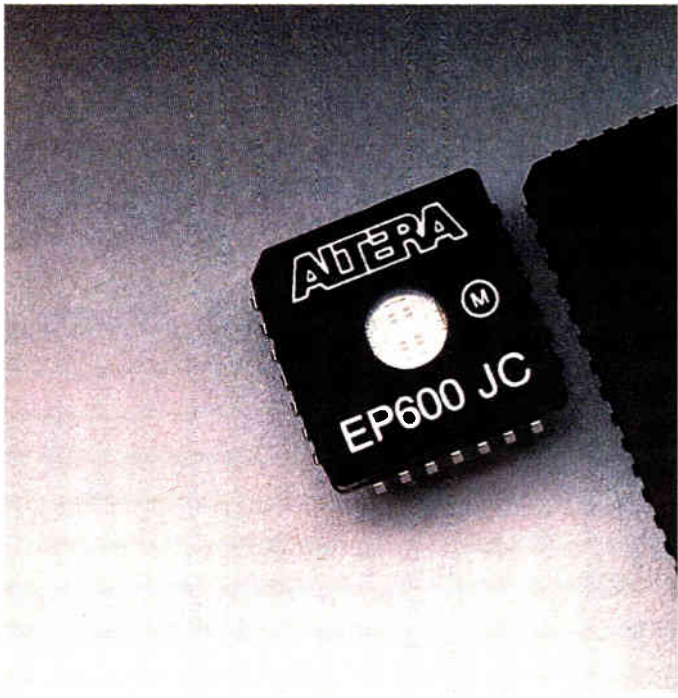

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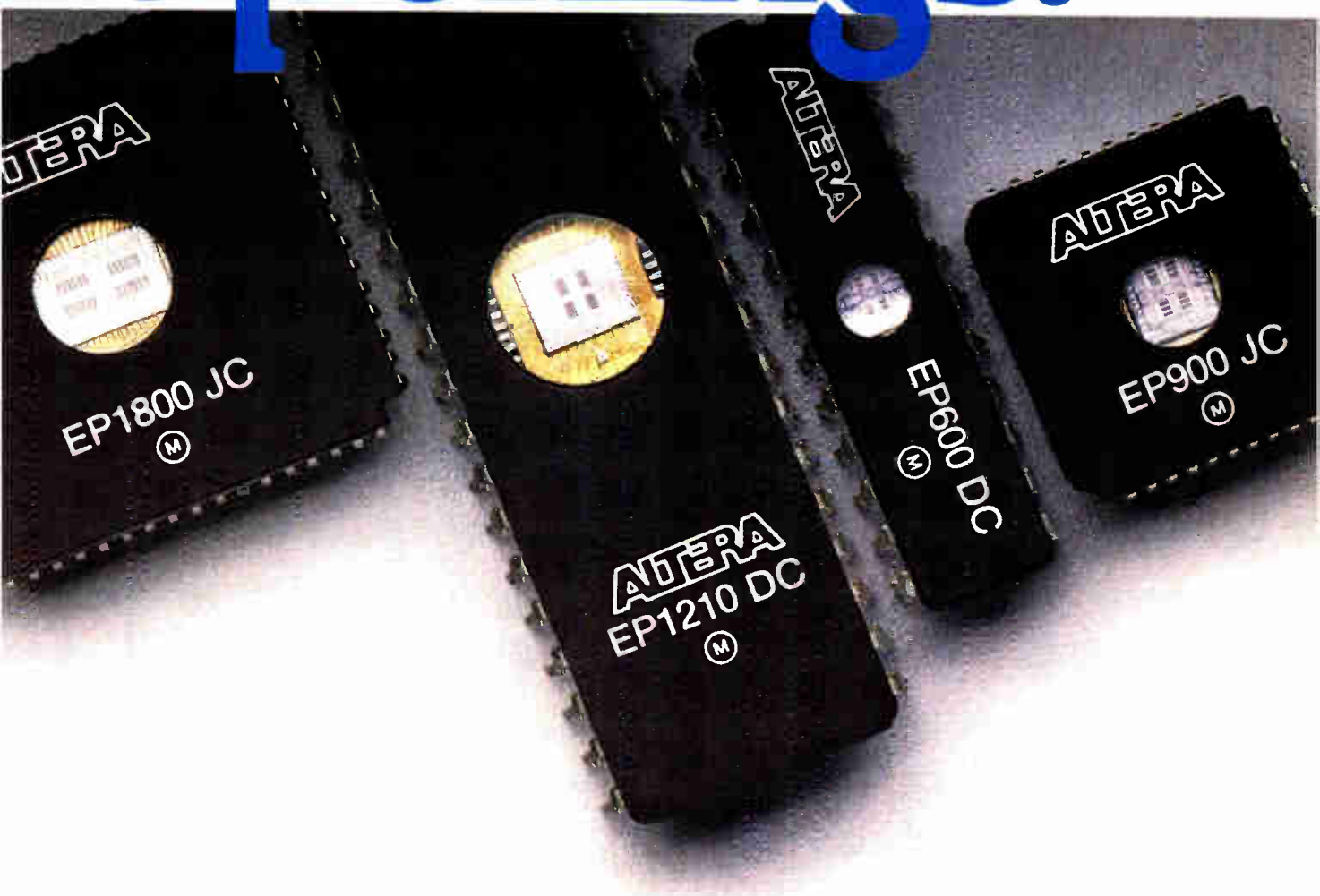


lutions, has been on the trail of the molded-in pin since he was at Photocircuits Inc. in Glen Cove, N. Y., two years ago. He tried plating to plastic but concluded that the pin was too difficult to handle in production—among the problems were getting conductors to adhere to plastic, soldering to plastic, and wire bonding. Instead of plating on the plastic, he decided "to borrow the best of both worlds." He molded an inexpensive pin into the body of the package, making it possible to mold in details such as chip cavities, stand-offs, and heat sinks.

At the same time, Werther made a proven, wire-bondable interconnection with a low dielectric constant by using a 4-to-8-mil-wide polyimide inner-layer pc substrate based on standard print-and-etch pc processing. The inner-layer circuit can easily be multilayered for even denser circuits.

But Photocircuits decided not to manufacture the new package, so last year Werther and Bill Miller, formerly president of Augat Inc. in Attleboro, Mass., formed their own company with Miller as president and obtained an exclusive license on the technology.

Production is simple. A thin pc board is attached to the top of the molded package with a proprietary adhesive. Chip input/outputs are then wire-bonded to pads on the pc board. Package pins pass through unplated or plated-through holes (depending on the number of board layers) in the board and are reflow-soldered to conductors on the top surface of the array's pc.

Werther believes the technology also can be used for other semiconductor packages such as chip carriers, light-emitting diodes, and multichip modules. The company is making its first testable prototypes and hopes for production in the second quarter. *–Jerry Lyman*

RESEARCH

GE GIVES AWAY THE STORE, BUT KEEPS THE BUSINESS

PRINCETON, N.J.

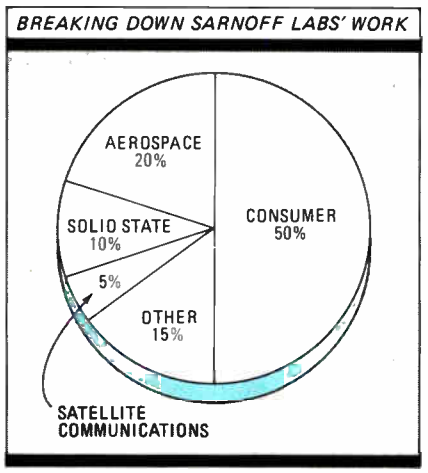
Time has been running out on the David Sarnoff Research Center ever since General Electric Co. took over RCA Corp., which owned the center, nearly a year ago. GE's reputation for no-holds-barred cost-cutting and its investment in its own research facilities seemed to spell doom for the Princeton, N. J. labs—once among the world's premier research institutions. Now GE can have its cake and eat it, too: by agreeing earlier this month to give the facility to SRI International, an independent research house in Menlo Park, Calif., it gets a big tax windfall and can continue to add to an invaluable research base.

The fate of the labs, which spawned technological breakthroughs in black-and-white and color television and commercialized the electron microscope, has been a source of much debate. The betting was that GE would close it, moving the most valuable operations to its Corporate Research and Development Center in Schenectady, N. Y., and selling the 350 acres in Princeton.

But GE did not initially realize the value of the Sarnoff Center's consumer electronics operations, according to James I. Magid, an independent industry analyst based in New York. He estimates that GE/RCA earned about $100 million in patent royalties alone in 1986—including about $2.34 for every video cassette recorder sold in the U. S. Unwilling to let such income potential dry up, he says, GE decided it was best to find a way to maintain the labs' work while cutting operating costs.

That's where SRI, the second largest private research company in the U. S., fits in: by donating the labs to a nonprofit organization such as SRI, GE retains the center's patents and associated royalties, gets a mammoth tax deduction worth about $100 million, and has access, through research contracts, to

CHANGE OF OWNERS. The David Sarnoff Research Center is now part of SRI International.



the same researchers who served RCA so well for all those years.

Key to the arrangement, Magid says, is that GE can support the Sarnoff center's consumer electronics research—which accounts for about half the work there (see chart)—at reduced cost without giving up what is most dear: the potential income from patents for its technology.

"Sarnoff is a patent-oriented lab," Magid says. Indeed, the labs have won 9,515 patents since 1969. GE will retain the royalties from work licensed by the labs, and to support continued experimentation, it will contract for at least $250 million worth of consumer electronics research over the next five years.

STUDY RESULTS. The decision to donate the labs to SRI resulted from a study SRI did for GE last fall on how to merge its technologies with SRI. What the study found, says Dennis Maxwell, vice president for communications at SRI, was that although much of the work at the Sarnoff labs did not fit in well with GE's overall picture, it was complementary with work being performed at SRI. RCA has automation software and communications technology that complements SRI's computer science and artificial intelligence work, says Maxwell.

SRI's research is now more than 40% military, and the acquisition of the RCA lab, which will be operated autonomously, will dilute that. "They don't have a highly [military] environment, and there is no desire on our part to be a general defense contractor," Maxwell says, adding that SRI is now more interested in commercial projects. "Five years ago, the military was a very large factor, [but] that is changing."

GE, meanwhile, did not give away everything. It is keeping two "satellite" new product laboratories, in Lancaster, Pa., and Indianapolis, Ind., which are part of the GE/RCA Consumer Electronics Division. They are responsible for commercializing consumer technology and were apparently considered too valuable to give up. *–Tobias Naegele*

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INTERNATIONAL NEWSLETTER

FEAR OF JOB LOSSES COULD CURB NEW ANTI-DUMPING MEASURE IN EUROPE

The Commission of the European Communities has drafted a proposal seeking to extend anti-dumping levies to include components made overseas that are assembled into finished products in Common Market countries. The proposal, which is aimed at Japanese producers, stems from complaints by European equipment makers. They say there is evidence that Japanese firms are circumventing duties on their products by assembling them in Europe—and, in an effort to gain market share, are selling them below cost. The proposal is opposed by France, the U. K., and Ireland, however, because Japanese equipment makers employ some 70,000 workers in Europe, and the three nations fear such levies could result in devastating plant closings. □

FUJITSU JOINS THE RUSH TO BUILD TELECOM EQUIPMENT IN THE U. S.

The Japanese rush to move production to the U. S.—and shield themselves from potential protectionist trade measures—continues. Now Tokyo-based Fujitsu Ltd. says it will boost manufacturing capacity in the U. S. so that the bulk of the telecommunications equipment it sells in the U. S. will also be made there. NEC Corp. previously indicated that it would expand its U. S. engineering staff devoted to the central-office-switch market [*Electronics*, Feb. 5, 1987, p. 50]. Fujitsu is enlarging its Anaheim, Calif. plant, where it builds private branch exchanges, to develop application software for PBXs. The plant may eventually manufacture central office switches as well, the company says. Fujitsu is also planning to double the capacity of its Dallas facility, where fiber-optic communications systems, digital microwave systems, multiplexers, and mobile radiotelephones are manufactured. □

WEAK DOLLAR HELPS APPLE IN EUROPE, HURTS SIEMENS IN THE U. S.

Apple Computer GmbH, the West German subsidiary of the U. S. computer maker, is taking advantage of the weakened U. S. dollar to spur sales in West Germany. The company cut the price of its Macintosh Plus system by 15% earlier this month. The weakened dollar is having the opposite effect on European manufacturers, whose products have become correspondingly more expensive in the U. S. Siemens AG reports that the lower value of the dollar was in part to blame for flat earnings during the first quarter of its fiscal year 1987, which ended Dec. 31. Net results for the period—about $164 million in profit, on sales of $6 billion—were about the same as last year's first quarter. Still, Siemens is better off than many other European firms doing business in the U. S., since the bulk of the products it sells in the U. S. are manufactured there. Only about 20% of its U. S. sales are imports from West Germany. □

JAPANESE SQUABBLE OVER THE INTERNATIONAL TELECOM MARKET

Japanese government agencies are fighting among themselves over efforts to open up access to the international telecommunications market. The Ministry of Posts and Telecommunications has said it will only allow one new company to join Kokusai Denshin Denwa Co., Tokyo, in serving that market. But the Ministry of Foreign Affairs has asked the Ministry of Posts and Telecommunications to withdraw its objections to investment by Cable & Wireless in a Japanese communications service firm. C&W has a 20% share in International Digital Communications Planning Inc., a joint venture formed last year by a group of Japanese, British, and U. S. companies to compete in the international telecommunications market. The regulatory body hopes International Digital Communications will merge with another firm, International Telecom Japan Inc., a joint venture of seven Japanese companies. □

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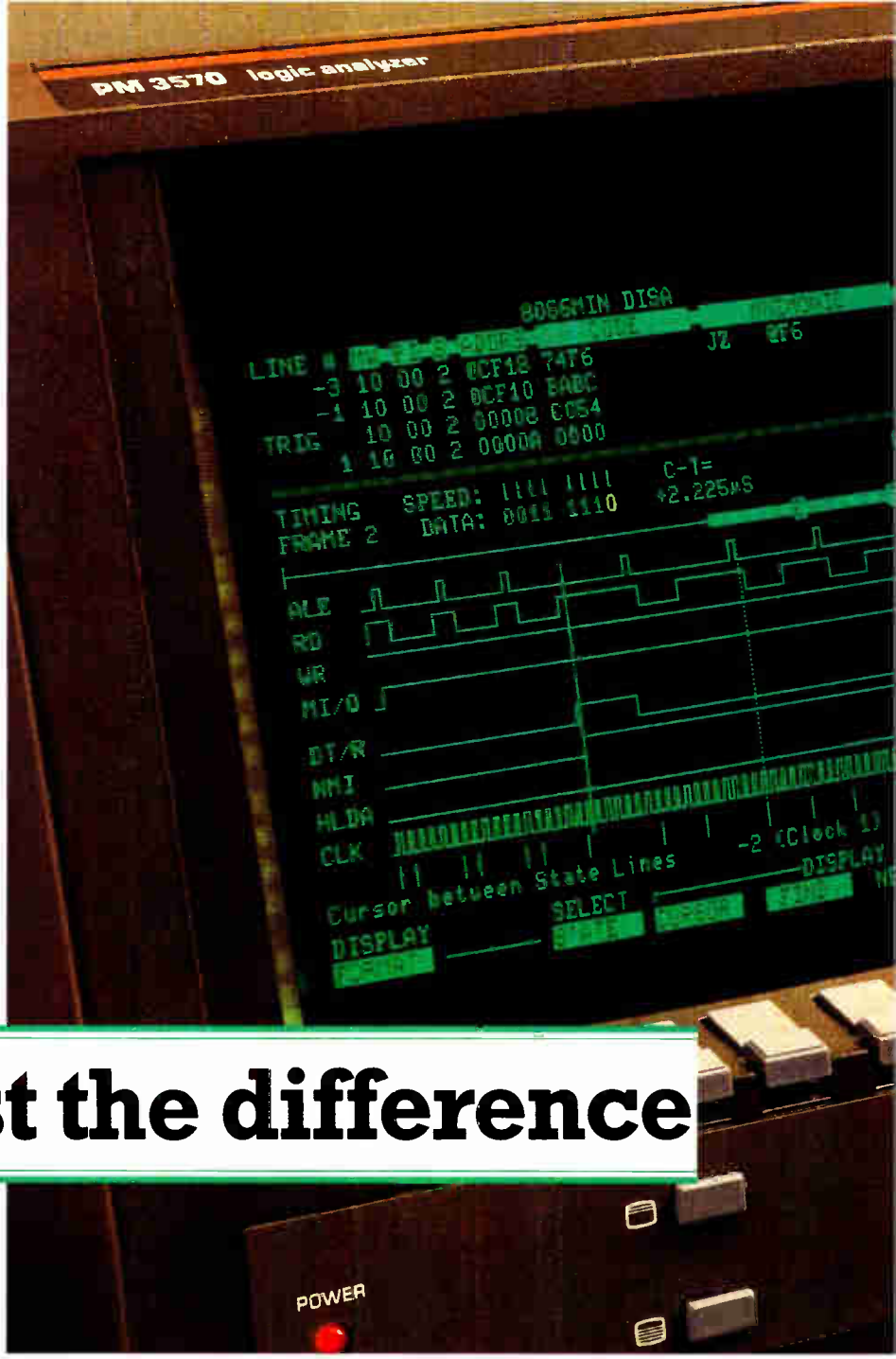

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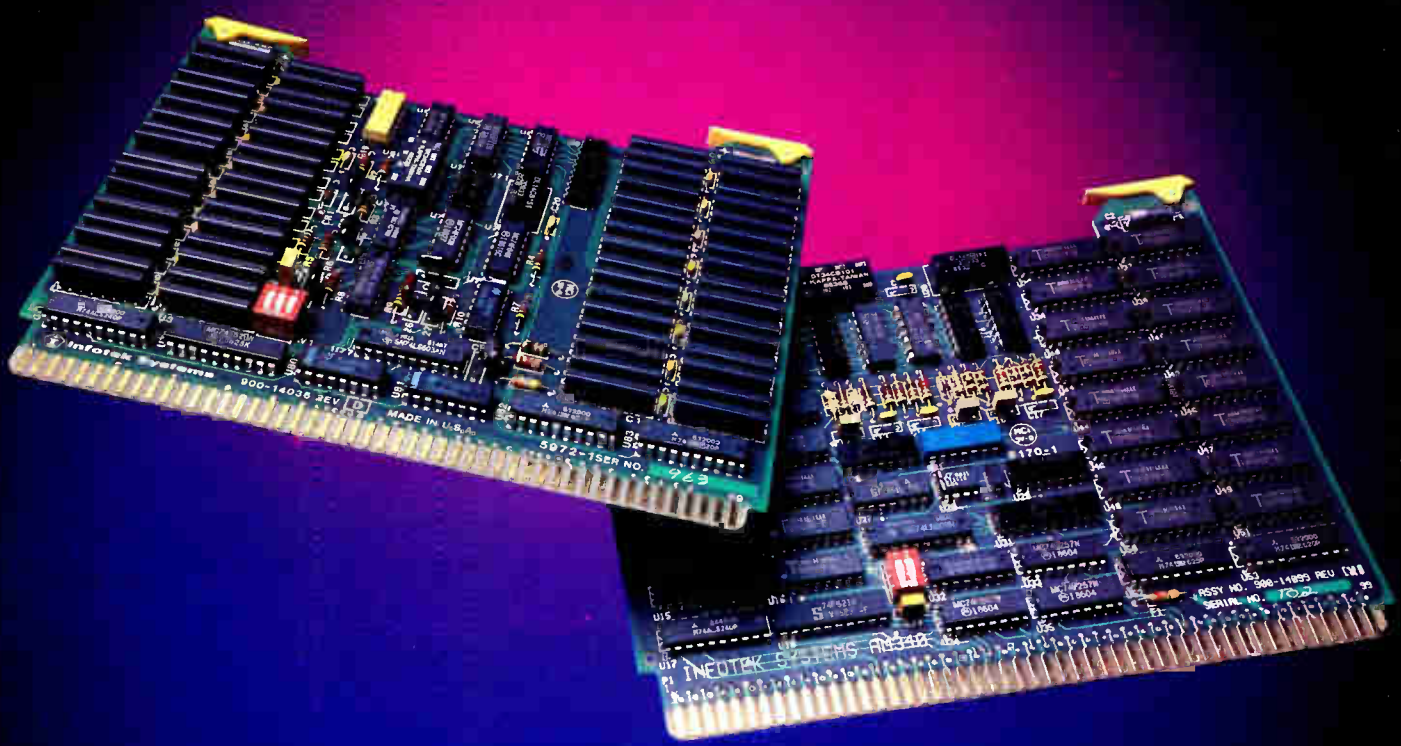

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INTERNATIONAL WEEK

JAPAN CENTER WILL PROMOTE IMPORTS

Japan's Ministry of International Trade and Industry will open a semiconductor trade center on March 1 to promote semiconductor imports. The center will provide information and advice on Japanese markets to foreign semiconductor manufacturers and will coordinate international conferences and exhibitions. The center had been scheduled to open in April, according to the semiconductor trade agreement with the U.S., but U.S. trade negotiators asked MITI to move up the date. A name and location have not yet been chosen.

SATELLITE FAX IS OFF THE GROUND

For the price of a small satellite-receiving station, European users will be able to participate in a 64-K/s facsimile system which interfaces directly with standard personal computers. Speeds for typical fax systems using the phone network are 1,200 or 2,400 b/s. Apollo, a joint project of the Commission of the European Communities and the European Space Agency, is designed to simultaneously fax documents to several locations throughout Western Europe with a resolution of up to 300 lines/in. It is expected to be available in 1989.

UK TO REVIEW EXPORT CONTROLS

The UK's Department of Trade and Industry is asking British companies for ideas to loosen the controls on exporting communications, transmission, and other equipment to Eastern Bloc countries. Controls that the DTI asked Cocom, the International Coordinating Committee, to review this fall are numerically controlled machine tools, fiber-optic manufacturing equipment, cables, telecommunications and transmission equipment, telephone switching equipment, and robots.

SGS SEEMS IMMUNE TO INDUSTRY SLUMP

Despite the slump in the world semiconductor business, SGS Microelettronica SpA, the Italian chip maker, continues to increase its worldwide sales for the sixth consecutive year. The Agrate company topped $375 million in sales last year, a gain of about 23% over 1985. In Europe, SGS pushed 1986 sales to $245 million, a 22% jump, which catapulted the company from the No. 8 spot in 1985 to No. 6 in 1986 among semiconductor suppliers in European markets. SGS attributes its success to its bipolar high-voltage, high-power devices for TV, auto, and computer applications.

PHONE SET IS ALSO VIDEOTEX TERMINAL

West Germany's Bundespost, the country's communications authority, is offering a multifunctional telephone that doubles as a videotex terminal. With Multitel, users can make calls and simultaneously use a videotex service in which a computer can be called to display information such as timetables and stock-market data. Multitel displays the information on a 10-by-11.5-cm monochrome CRT. The set rents for about $25 a month and is currently supplied by Siemens AG.

JAPAN OPTICAL GEAR TO GROW 21%

Despite the lackluster Japanese economy, Japan's Optoelectronic Industry and Technology Association says a poll of 118 companies indicates that sales of optical equipment will grow 21% to 5,432 billion yen during the year ending March 31. Optical disks have been an engine of growth and now account for 30% of all industry sales, with digital compact-disk players leading. But 1985's rapid spurt of 196% will slow down to 19% this year and could be even more lackluster next year. Growth will be less than 10% for laser-beam video-disk players.

DISAGREEMENTS STALL EC PROJECT

Financial disagreements between European governments over a budget figure are delaying the European Communities' Research and Development in Advanced Communications Technologies in Europe. Many European telecommunications and computer companies are banking on RACE to compete with U.S. and Japanese companies. The details won't be sorted out at the earliest until the next meeting at the end of March, which could delay the program's scheduled start this summer.

SIEMENS TO HIRE 2,500 ENGINEERS

Although its overall workforce will remain about flat, West Germany's Siemens AG plans to hire 2,500 to 3,000 engineers this year in addition to 4,000 it hired in 1986. Most of the new employees will work in the computer and semiconductor fields, where Siemens is making big research and development efforts. Worldwide, the Munich company employs about 363,000. Of these, roughly 250,000 are working in West Germany, which makes Siemens the country's largest private employer.

VIDEOTEX GEAR, SOFTWARE OFFERED

Brown's Operating System Services Ltd. is offering users of IBM mainframes and compatible machines new ways to run private videotex systems. The London company is introducing integrated hardware and software products to the British Videotex System. A version for the U.S. will follow later this year.

UTILITY SIGNS UP FOR TRADANET

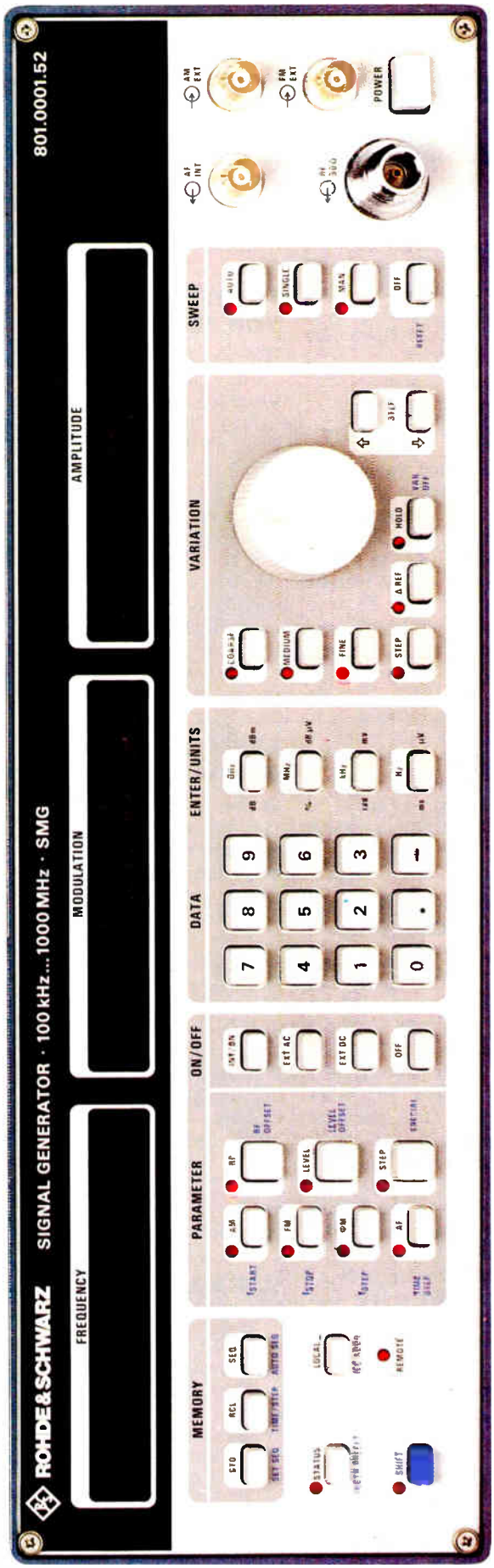
Thirteen of the UK's 15 electricity boards will use an electronic data interchange service from International Network Services Ltd., Feltham, UK, a joint venture formed last month between STC and Geisco Ltd. [*Electronics*, Jan. 22, 1987, p. 46]. The boards are the first British utility to use Tradanet service linking their computers with their suppliers in order to electronically exchange documents such as orders and invoices.

FIRMS JOIN ON CAD SOFTWARE PROJECT

A group of European companies will develop a common software environment for computer-aided design programs. Led by European Silicon Structures, the group met this month at ES2's UK headquarters in Bracknell. Other participants are Bull; CNET; STC-ICL; Imec; Nixdorf-Cadlab; Olivetti; NMP, the Swedish group comprising Saab, Ericsson, and Asea; and Philips. The group will develop a specification, which each participant will use in developing CAD systems. The group is hoping for the cooperation of third-party software suppliers.

U.S. NAVY BUYS UK MINE SYSTEM

The U.S. Navy is ordering 10 Versatile Exercise Mine Systems from British Aerospace's naval and electronic systems division in Bristol, UK, with an option for 15 more. VEMS, a computer-based system capable of simulating multi-influence sea mines, has been adopted as a NATO standard exercise mine. The contract is worth more than $6 million.



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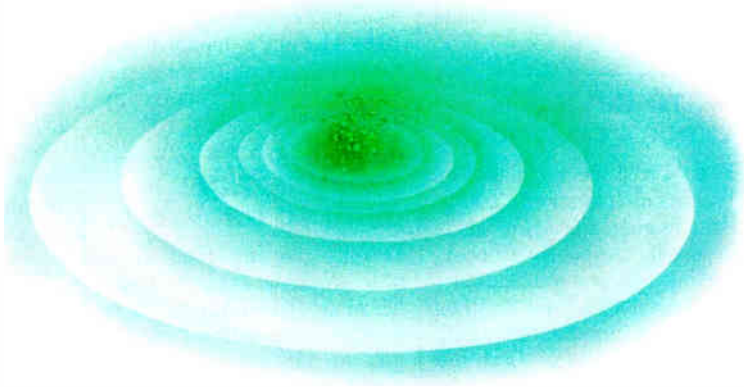

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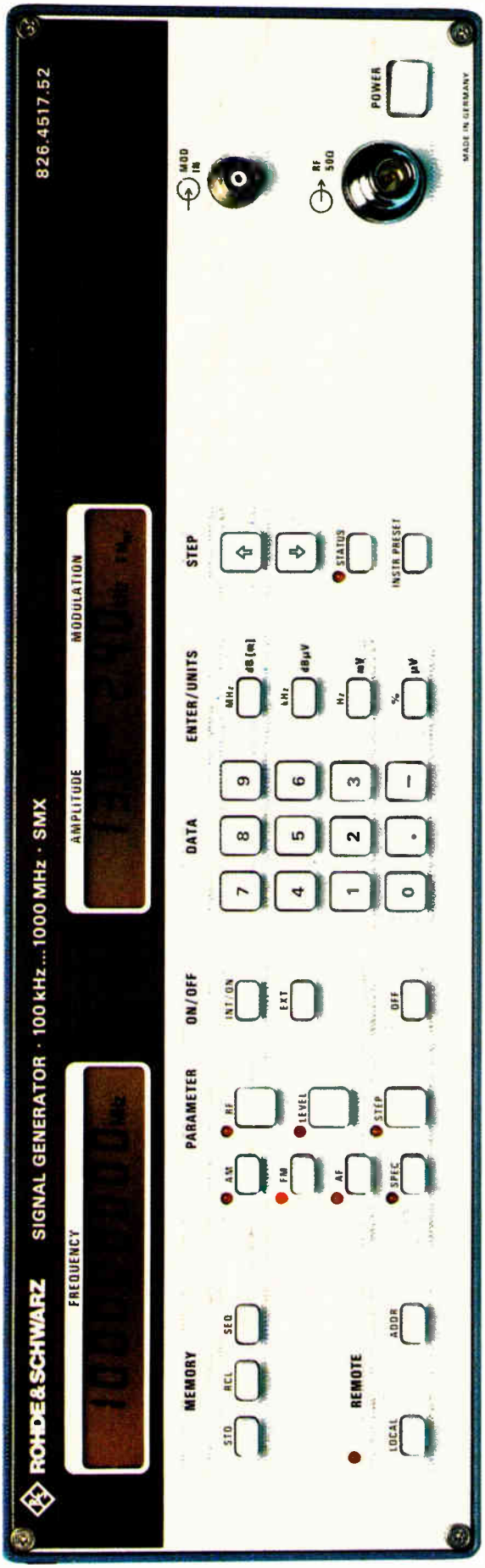

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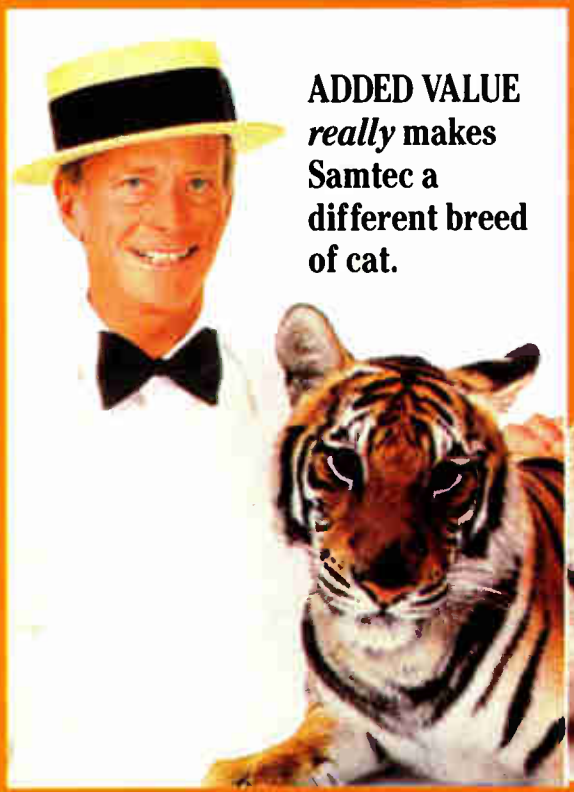

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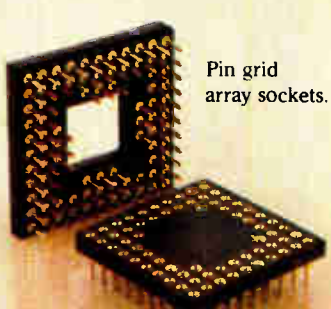

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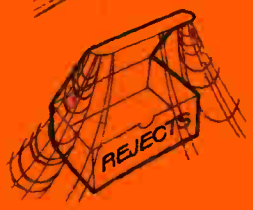

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Interconnect Guide plus New 72-page Catalog. Guide is valuable reference for keeping up with new interconnect products and applications. New Catalog has specs on all Samtec interconnects.

samtec

EUROPEAN HEADQUARTERS: **SAMTEC, Ltd.** 35 Deerdykes View, Westfield, Cumbernauld, Scotland G68 9HN Phone: 02367 39292 FAX: 2367 27113 TLX: 776158

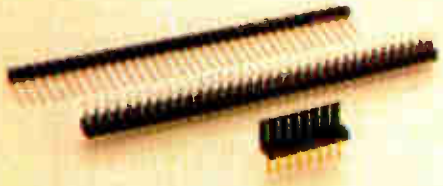
SUDDEN SERVICE

WORLDWIDE HEADQUARTERS: **SAMTEC, Inc.** P.O. Box 1147, 810 Progress Blvd., New Albany, IN 47150 USA Phone: (812) 944-6733 TWX: 810-540-4095 TLX: 333-918 FAX: 812-948-5047

Machined sockets, terminal strips.

Shrouded IDC terminal strips, matching cable strips.

.025" sq. terminal strips, single/double row, shrouded.



Circle 105 on reader service card

The μPD612X Series

Get Going with Remote Control

Remote control is the name of the game when it comes to quick and efficient manipulation of audio-visual equipment and other home or office appliances. And NEC's new CMOS-based μPD6124/5/6 Series is the infrared remote control transmitter that combines programmability with small packaging and low power consumption. Excellent performance stems from a 1024 x 10 bits program memory, 32 x 4 bits data memory, and a large instruction set. A standby mode plus low operating voltage reduces battery design to a minor detail.

The μPD612X Series features 32, 64 or 96 key inputs. All remote control commands and functions are programmable and the transmission format can be customized. The operating frequency is either 38 or 58 KHz.

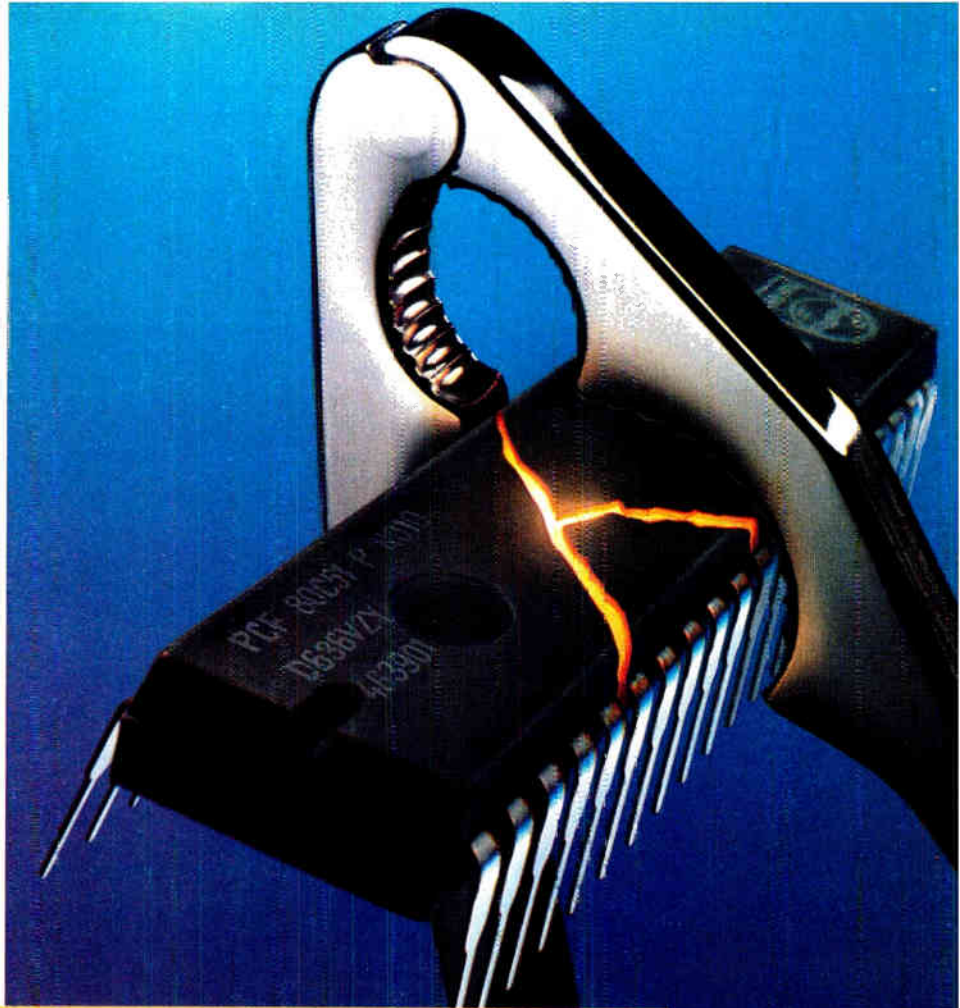
TYPE	KEYS	PACKAGE
μPD 6124	32	20 PIN MINIFLAT
μPD 6125	64	24 PIN MINIFLAT OR SLIM DIP
μPD 6126	96	28 PIN MINIFLAT

West Germany: Düsseldorf 02 11/65 03 01, Telex 8 58 996-0
The Netherlands: Eindhoven 0 40/44 58 45, Telex 51 923
France: Paris 01/39 46 96 17, Télex 699 499
Italy: Milano 02/67 09 108, Telex 315 355
Sweden: Täby 08/73 28 200, Telex 13 839
UK: Milton Keynes 09 08/69 11 33, Telex 777 565

NEC

Circle 106 on reader service card

Get inside the 8051!



Developing products based on the 8051 microcontroller? Then you'll be very interested in our **MAB** (microcomputer adapter box) **80C51**.

Because, used with any of our development systems (PEDS, PMDS-2 or PMDS-3) it actually gets you inside the 8051 chip by providing total access to all internal features.

The **MAB-80C51** allows full real time transparent emulation for 8051, CMOS, NMOS and HMOS microcontrollers plus selected derivatives.

Power down and idle modes are supported and special bonded out lines provide access to program and data memories. You can also break program execution and "freeze" the CPU status (including timer and interrupt levels).

Moreover, the **MAB-80C51** is complemented by a powerful range of cross software and symbolic debuggers, including a PL/M-51 compiler supported on VAX, IBM PC-AT, PEDS and PMDS hosts.

Test the difference

And as Philips is one of the world's leading manufacturers and users of microcontrollers, microprocessors and development tools, you benefit by choosing a single-source supplier who understands your needs perfectly.

VAX – Digital Equipment Corp.
IBM PC – International Business Machines Corp.

Test the difference and you'll agree that Philips wins on price and performance!

Write to: Philips I & E, T & M department, Building HKF70, 5600 MD Eindhoven, The Netherlands or call your local supplier: **Austria** (222) 629141-0; **Belgium** (2) 5256692/94; **Denmark** (1) 572222; **Finland** (0) 5257225; **France** (1) 48301111; **Germany** (561) 5010; **Great Britain** (0223) 358866; **Ireland** (1) 693355; **Italy** (39) 36351; **Netherlands** (40) 782808; **Norway** (2) 680200; **Portugal** (1) 683121; **Spain** (1) 4042200; **Sweden** (8) 7821800; **Switzerland** (1) 4882211

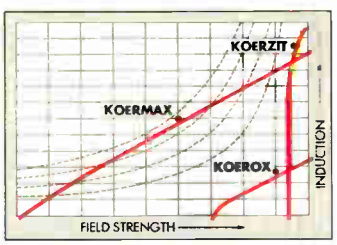
PHILIPS **Test & Measurement**

PHILIPS

Circle 107 on reader service card

KRUPP WIDIA permanent magnets: Shaping tomorrow's world today.

All around the globe permanent magnets from KRUPP WIDIA are continually proving their unparalleled reliability even under the most arduous conditions. Thanks to the wide range of materials available, solutions can be exactly tailored to meet specific requirements. KRUPP WIDIA permanent magnets offer advantages such as high demagnetization stability and high temperature resistance as well as highest possible field strength with smallest possible magnet volume.



Why not benefit from KRUPP WIDIA's wealth of experience? From specialist advice to finished component. For permanent-magnet and soft-magnetic materials.

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Telefax 0201/725-3529

KRUPP WIDIA
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INTERNATIONAL PRODUCTS

SIEMENS-BASF JOINT VENTURE EXTENDS ITS MAINFRAME LINE

BASED ON HITACHI LINE, COMPAREX 7/90-3 HAS 10% EDGE OVER IBM MODEL

Comparex GmbH, a joint venture of Siemens AG and BASF AG, has expanded its 7/90 series of IBM-compatible mainframe computers with the 7/90-3, which can execute 28 to 31 million instructions per second and has up to 256 megabytes of main memory.

This newest version offers a considerable performance jump over the company's previous 17-mips 7/90-1 and 24-mips 7/90-2 machines. The new 7/90-3 boosts performance by combining the 7/90-1 and 7/90-2 into a single package running under the same software. Its central processing unit provides about a 10% performance edge over IBM Corp.'s 3090-200 machine, say Comparex officials.

I/O OPTIONS. Comparex's 7/90-3 can be configured with 16 to 48 I/O channels, each capable of handling 3 megabytes/s.

CLONED. Based on Japan's Hitachi Ltd. M680 Series of computers, the 7/90-3 has a three-stage storage hierarchy comprising up to 256 megabytes of main memory, 0.5 megabytes of work storage, and two 128-K-bytes memory buffers.

Equipped with two input/output processors, the 7/90-3 can be configured with 16 to 48 I/O channels, each capable of handling 3 megabytes/s. An alternative configuration available on all Series 7/90 computers allows as many as 16 I/O channels to operate at a data-transfer rate of 6 megabytes/s.

Comparex will introduce the 7/90-3 at the Cebit show, along with its semiconductor-based storage system, the 6580 Model 6, which boasts a capacity of up to 2 gigabytes. It can be interfaced with the 7/90's high-speed data buses. The 6580 has an access time of 1.6 ms, compared with 25.6 ms for the company's 6480 disk systems.

The first deliveries of the 7/90-3 will be made in the second quarter of this year. It will cost in the neighborhood of 12 million DM, depending on configuration. Deliveries of the 6580 Model 6 storage system will also begin in the second quarter. The smallest configuration—32 megabytes—will sell for 220,000 DM. The largest configuration, 512 megabytes, will sell for 2.3 million DM.

Comparex, Europe's largest vendor of IBM-compatible computers, started operations on the first of this year [*Electronics*, Nov. 27, 1986, p. 48]. The company intends to add the 7/90-4, the -6, and the -8 during the second and third quarters of this year. When the round of offerings is complete, Comparex will be covering a performance span ranging from 17 mips to 77 mips, say company officials. *–John Gosch*

Comparex GmbH, Gottlieb-Daimler-Str. 10, D-6800 Mannheim 1, West Germany
Phone 49-621-601 [Circle 501]

COMPUTER FAIR EXPECTS 350,000 VISITORS

HANNOVER, WEST GERMANY

Cebit, the center for office, information, and telecommunications technology, is off and running Part of the giant industrial Hannover Fair in this northern West German city until 1985, Cebit split off last March, and is now held a few weeks prior to its industrial parent.

Last year, Cebit attracted more than 2,140 exhibitors and 340,000 visitors to 11 exhibition halls. This year's show, from March 4-11, should surpass these figures. More than 2,200 companies from 37 countries are expected to show their wares to at least 350,000 visitors.

Among the highlights will be the "C" technologies, says Jörg Schomburg, executive director of the Hannover-based German Fair and Exhibition Co., Cebit's organizer. In a single hall, nearly 180 exhibitors will display products in computer-aided design, manufacturing, engineering, and computer-integrated manufacturing, with an emphasis on applications.

Microcomputers and software will also figure prominently at Cebit, says Schomburg. About 500 exhibitors will be represented at the Microcomputer Applications Center in four halls. The center will present a range of hardware and software geared to the needs of small and medium companies.

Banking will be another focal point, with 120 companies displaying electronic systems, services, equipment, and software that target the key areas of counter services and banking communications.

With the U. S. setting the pace in information technology, the largest foreign contingent will be American companies—130 so far. All of the products that are featured in this section will be introduced at the Cebit show. *–J. G.*

AEG'S PAGE READER HANDLES SIX FONTS

The PBL6103 page reader from AEG Datasystems reads typewritten pages optoelectronically in any of the six most common typefaces—OCR, Courier 10, Courier 12, Letter Gothic, Prestige Elite, and Pica—and converts them into a code that can be handled by a word-processing system. It thus replaces a keyboard input device.

The PNL6103 reads more than 150 characters/s. Depending on the print quality and the amount of text, it takes from 25 to 50 seconds to read a page. Contrast is automatically adjusted for reading each character.

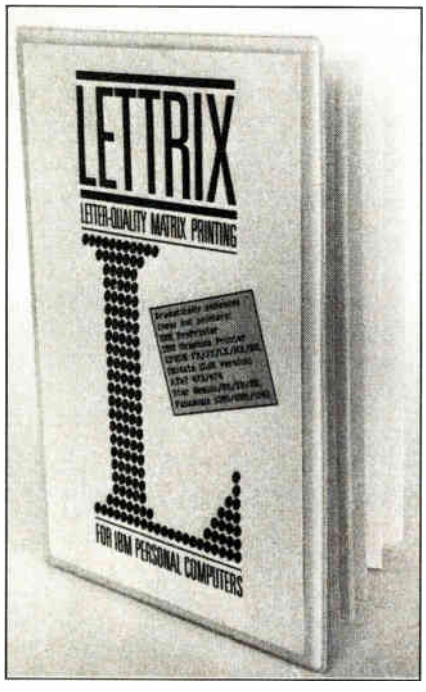
The reader also adjusts to line spacings. A linear array of 2,048 photodiodes is used to read text. The device can be used for entering typewritten manuscripts into word-processing systems, for filing and archiving, and for conversion of typewritten texts into Telex systems. Available now, the optical type reader costs 39,500 DM.

AEG Datasystems, Bücklestr. 1-5, D-7750 Konstanz, West Germany.
Phone 49-7531-862020 [Circle 701]

LETTRIX OFFERS MORE FONTS, IMPROVED TYPE

Compucon GmbH's Lettrix software gives various matrix printers on personal computers from IBM Corp. and other popular printers crisper type and more fonts.

In contrast to other print programs, Lettrix needs no separate text file. It supplies conventional printers with special characters, symbols, and headlines in different letter sizes, boldface type, italics, and other specialties.



Lettrix runs under Microsoft Corp.'s DOS 2.0 operating system and requires 50-K of memory. The package includes a floppy disk and a 40-page handbook in English. A German translation is available. The software package is available from stock for 308 DM.

Compucon GmbH, Jahnstr. 22, D-8037 Olching, West Germany.
Phone 49-8142-28041 [Circle 703]

DIGITIZERS CONVERT GRAPHICS TO NUMBERS

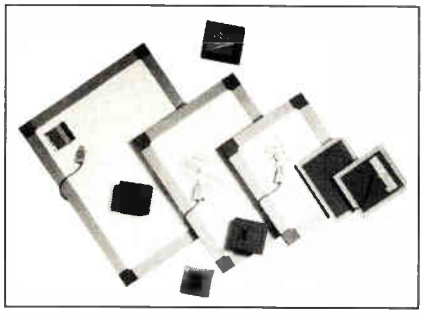
The 2200 and 2500 Series digitizers from Calcomp GmbH, the European affiliate of the Anaheim, Calif., company, are low-cost devices that convert graphic information into digital form for entry into a computer.

Adaptable to a variety of markets, including business, industry, and education, the digitizers target original-equipment manufacturers and end users. Both digitizers are available in two pad sizes: 12 in. by 12 in., and 12 in. by 18 in. The 2200 offers a resolution of 200 lines/in., and the 2500's resolution is 1,000 lines/in.

The digitizers are easy to integrate into work-station environments because they support industry-standard interfaces. All options are selected with soft keys instead of mechanical switches. They can be used with stylus or cursor input devices and feature self-test and diagnostics.

Available now, the 12-in.-by-12-in. and 12-in.-by-18-in. versions of the 2200 sell for 1,480 DM and 1,910 DM, respectively. Those two versions of the 2500 sell for 2,320 DM and 3,230 DM, respectively. The stylus costs 230 DM and the cursor 520 DM.

Calcomp GmbH, Werftstr. 37, D-4000 Dusseldorf 11, West Germany.
Phone 49-211-500920 [Circle 702]



TABLET HELPS INPUT CHINESE CHARACTERS

Chi-Easy is a personal-computer-supported Chinese-character-input system developed by Chinese scientists at Gerb Elektronik. A bar-code reader and a special digitizer tablet are used to simplify input into the PC.

A character is created by using the bar code reader and writing the character—one stroke at a time—on a matrix that recognizes the direction of the strokes. After each stroke, the eight most commonly used characters containing that stroke are displayed for the user. They can be selected with the digitizer pen and transferred to the word-processing system.

With the first stroke, about 40% of the proper characters are found, and after the second stroke about 85%. After the fourth stroke, 99.5% of the 6,763 most common Chinese characters are found, says the company.

The Chi-Easy system can be used with any industry-standard computer that runs Microsoft Corp.'s MS-DOS and has at least 512-K of random-access memory. Available in April, the system will be deliverable from stock and will cost 1,480 DM.

Gerb Elektronik GmbH, P. O. Box 510 230, D-1000 Berlin 51, West Germany.
Phone 49-30-411061 [Circle 704]

AMIGA 500 IS BASED ON MOTOROLA'S 68000

Commodore GmbH's Amiga 500 is the first low-priced computer with a 68000 16-bit central processing unit from Motorola Inc., according to Commodore. Designed as a multitasking keyboard computer with an integrated 3½-in. floppy disk, the unit can be operated with a monitor or a video decoder for a TV set.

It features a 512-K-byte memory, expandable to 1 megabyte with memory on printed-circuit boards. Available in March, the Amiga 500 can be delivered in one week and will cost about 1,300 DM.

Commodore GmbH, Lyoner Str. 38, D-6000 Frankfurt 71, West Germany.
Phone 49-69-66380. [Circle 705]

Fujitsu's latest ergonomically-designed keyboard for PCs

◆Key switches with dome-shaped mechanical contacts guarantee service life of over 50 million operations ◆Synchronous serial data transmission interface ◆Convenient interlock mechanism with N key rollover ◆Key tops with inset LED indicators ◆Two-level tilt mechanism (7° and 12° selectable) ◆8-country key arrangements available (U.S.A., U.K., Germany, France, Italy, Spain, Sweden, Switzerland)

FKB2930 Series

Connector Pin Assignment	
Pin number	Signal
1	CLOCK
2	DATA
3	——
4	GROUND (SG)
5	5V DC
SHELL	(FG)

DIN Connector (shielded)

FUJITSU MIKROELEKTRONIK GmbH:
Arabella Center 9. OG./A, Lyoner Straße 44-48, D-6000 Frankfurt am Main 71, F.R. Germany Phone: 069-66320 Telex: 0411963 Fax: 069-6632122
FUJITSU MICROELECTRONICS PACIFIC ASIA LIMITED:
805, Tsim Sha Tsui Centre, West Wing, 66 Mody Road, Kowloon, Hong Kong Phone: 3-7320100 Telex: 31959 FUJIS HX Fax: 3-7320133
FUJITSU LIMITED (Electronic Components International Marketing Div.):
Furukawa Sogo Bldg., 6-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100, Japan Phone: National (03) 216-3211
International (Int'l Prefix) 81-3-216-3211 Telex: 2224361 Fax: (03) 216-9771

FUJITSU

Circle 109 on reader service card

MICROWAVE UNITS YIELD 10-km LANs

The digital microwave system DRS 2-140/18700 from ANT Nachrichtentechnik extends local-area networks up to 10 km. Depending on configuration, the system handles transmission rates of 2, 8, 34, or 140 Mb/s.

The units, including a 40-cm-wide dish antenna, are in a weatherproof package

that suits the system to outdoor use. It can also be operated with a 60-cm or 120-cm dish.

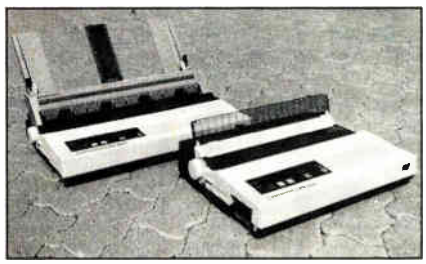
The system can be mechanically adapted for mobile applications. The 2-, 8-, and 34-Mb/s versions will be available later this year, and the 140-Mb/s version in 1988. Price is available upon request.

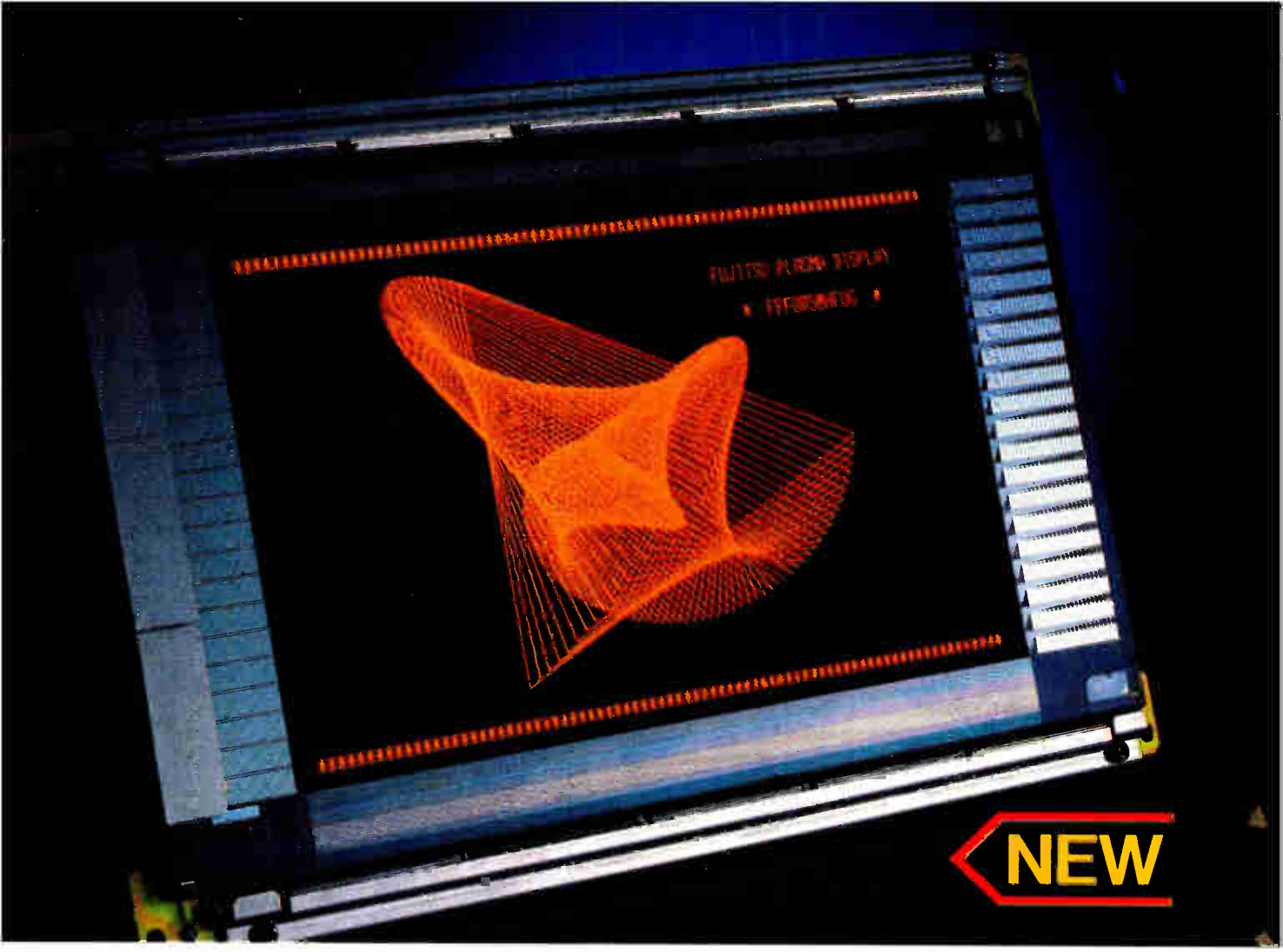
ANT Nachrichtentechnik GmbH, Gerberstr. 33, D-7150 Backnang, West Germany. Phone 49-7191-132051 [Circle 706]

LOW-NOISE PRINTERS RUN AT HIGH SPEED

Centronics' new matrix printers run at 180 characters/s for printing drafts and 45 c/s in their letter-quality printing mode. Ideal for small-business and personal-computing applications, the Printstations 210 and 220 operate at a low noise level of only 59 dB.

With their standard parallel and serial interfaces, the printers can be connected to most data-processing systems. The two models differ only in column width: the 210 has 110 columns at 10 characters per inch, and the 220 has 136 columns, also at 10 characters per inch. Printing is bidirectional, and 8½-by-11-





Crisp Display and Low Profile Panel

CRT-Compatible Fujitsu Plasma Display with Memory Function

Brightness is the foremost feature of the Fujitsu plasma display. A special memory function reduces flicker to nothing. And with the display's high resolution, eye-weariness is now a thing of the past. Even with its built-in drive circuits, the display is integrated into a compact, thin, power-saving package. Try this exciting new panel, which is perfect for the ever-shrinking equipment in personal OA systems, NC machines, and industrial robots.

Demonstration sample
for stand-alone display unit

Features

- Bright, clear memory display that is completely flicker free
- 640 x 400 dot matrix high-resolution display
- Easy-to-use CRT-compatible interface
- Multi-drive LSI that makes the unit compact, thin, and lets it consume little power
- Highly reliable AC memory panel

Specifications

Model	FPF 8050 HFUG
Display resolution	640 x 400 dot matrix (256,000 dots)
Effective display size	210.87 mm (W) x 131.67 mm (H)
Dot spacing	3 dots/mm (dot pitch: 0.33 mm)
Brightness	150 cd/m²
Contrast ratio	20 : 1
Display color	Neon orange
Field of view	120° min.
Exterior dimensions	300 mm (W) x 200 mm (H) x 27 mm (D)
Weight	Approx. 1.5 kg

FUJITSU MIKROELEKTRONIK GmbH:
Arabella Center II, 805, A. Lonner Straße 44-48, D 6000 Frankfurt am Main 71, F R Germany Phone: 069-66320 Telex: 0411963 Fax: #69-6632122
FUJITSU MICROELECTRONICS PACIFIC ASIA LIMITED:
805, Tsim Sha Tsui Centre, West Wing, 66 Mody Road, Kowloon, Hong Kong Phone: 3 7320100 Telex: 31959 FUJIS HX Fax: 3 7320133
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Furusawa Sogo Bldg., 6-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100 Japan Phone: National (03) 216-3211 International (Int'l Prefix) 81-3-216-3211
Telex: 2224361 Fax: (03) 216-9771

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in. A4-format paper loading is simplified by the optional cut-sheet feeder, which accepts A4 paper horizontally.

The 210 costs 1,395 DM and the 220 sells for 1,598 DM. Delivery takes up to 30 days.

Centronics Data Computer GmbH, Oberliederbacher Weg 42, D-6231 Sulzbach, West Germany.
Phone 49-6196-70320 [Circle 708]

PORTABLE COMPUTER OFFERS 50 KEYS

The Portable Transaction Computer PTC 750 from Telxon GmbH has a 50-key alphanumeric keyboard that does not require a shift key to change from letters to numerals. A bar-code reader can also be used for data input.

The memory capacity is 64-K bytes of the user programs and up to 1 megabyte for data. The operating system is written in C and in assembly language for the Intel Corp. 8088 microprocessor. Applications are coded in a Cobol-structured language called TCAL.

Data output is either via the integrated transceiver to a base station at 9,600 bits/s, or via the RS-232-C interface to a modem. For data output, the unit accepts serial printers. Data is shown on a 16-line display; each line has 16 characters. Characters are in an 8-by-8-dot matrix.

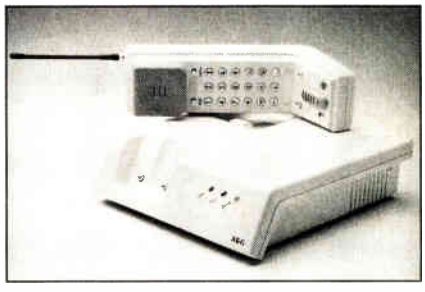
The PTC 750 can be delivered from stock in two weeks. Prices range from 1,000 DM to 10,000 DM for different configurations.

Telxon GmbH, Gutenbergring 1-5, D-2000 Nordernstedt, West Germany.
Phone 49-40-5230630 [Circle 707]

PHONE FEATURES SECURITY SYSTEM

The CLT 1 cordless telephone from AEG enables a permanent exchange of codes between the mobile and stationary parts to guard against its unauthorized use. If the codes do not match, there's no communication. The telephone addresses the problem of someone using a mobile handset for one telephone to establish a connection through a base set owned by someone else, thereby charging the call to the second set of base equipment.

The communications frequencies between the mobile handset and the base



FUJITSU MINI-THERMAL PRINTERS

Easier to read. Harder to hear.

FTP-040 MCS501

FTP-020 MCS501

FUJITSU SYSTEM COMPONENTS

And much more!

Now there are versatile mini-thermal printers with a host of important features you have not been offered before – plus they do graphics and total blackouts!

•CLEARER
An advanced fixed print head and stable-contact forms are the secret. You'll get clarity that no other printer can match – even for detailed graphics.

•QUIETER
Head movement means noise. Fujitsu's stationary head design has virtually eliminated irritating printing noise – a welcome relief to any office.

•FASTER
At 80 characters per second, both models double the printing speed of conventional types so the job is finished in half the time.

•MAINTENANCE-FREE
No head movement, no maintenance problems. And their unique wear-resistant structure provides an operating life of up to 20 million dot lines.

•UL RECOGNIZED
Fujitsu has obtained UL recognition for its mini-thermal printers.

Characteristics	FTP-020 Series	FTP-040 Series
Dot configuration	140 line dots	280 line dots
Dot pitch	70 dots/inch	
No. of printing columns	20 (5 x 7 dots)	40 (5 x 7 dots)
Character size	1.8 x 3.0 mm	
Printing speed	80 characters/sec.	
Printing paper width	60 mm	110 mm
Input interface	8-bit parallel (Centronics Standards)	
Power source	Logic section: 5VDC, 1A (max.) Head section: 24VDC, 2.5A (max.)	

FUJITSU MIKROELEKTRONIK GmbH:
Arabella Center 9. OG./A, Lyoner Straße 44-48, D-6000 Frankfurt am Main 71, F.R. Germany Phone: 069-66320
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FUJITSU

Circle 114 on reader service card

phone set are in the 900-MHz range. Outdoors, a user carrying the handset may be up to 200 meters away from the base. Within buildings, the distance is up to 50 m.

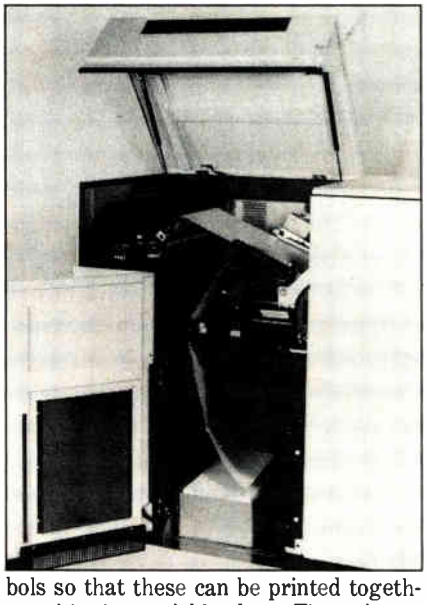
The handset, which integrates the radio circuitry and a keyboard, features special functions such as automatic repeat dialing and abbreviated dialing. The phone will be offered by the Bundespost, West Germany's communications authority, under the name Sinus 1. It will also be sold by communications equipment retailers. The price has not been established.

AEG AG, Theodor-Stern-Kai 1, D-6000 Frankfurt 70, West Germany.
Phone 49-69-6001 [Circle 709]

PRINTER DELIVERS 88 PAGES/MINUTE

The laser printer 6890 from Comparex prints eighty-eight 8½-by-11-in. pages per minute. It can be connected to any of the company's processors or compatible units by the same interfaces used with conventional impact printers.

The machine is 1.4 m high and is compact, occupying 178 cm by 84 cm of floor space. A Winchester disk stores company logos and other graphic symbols so that these can be printed together with the variable data. The orientation of the printed output can also be turned 90°.



Comparex expects the system's least durable part, the drum, to last through at least 1.2 million pages. Several character sets are offered in the standard configuration, and others may be added.

The company will provide software support and training programs. Delivery of the 6890 takes six weeks, and the machine costs 320,900 DM.

Comparex GmbH, Gottlieb-Daimler-Str. 10, D-6800 Mannheim 1, West Germany.
Phone 49-621-601 [Circle 710]

SIEMENS

High performance for low-current applications

Miniature relay D2

Siemens offers a highly extensive range of tried and tested electromechanical components, plus all the experience of a manufacturer who has consistently invested a great deal of know-how in developing and perfecting electromechanical components geared to market requirements.

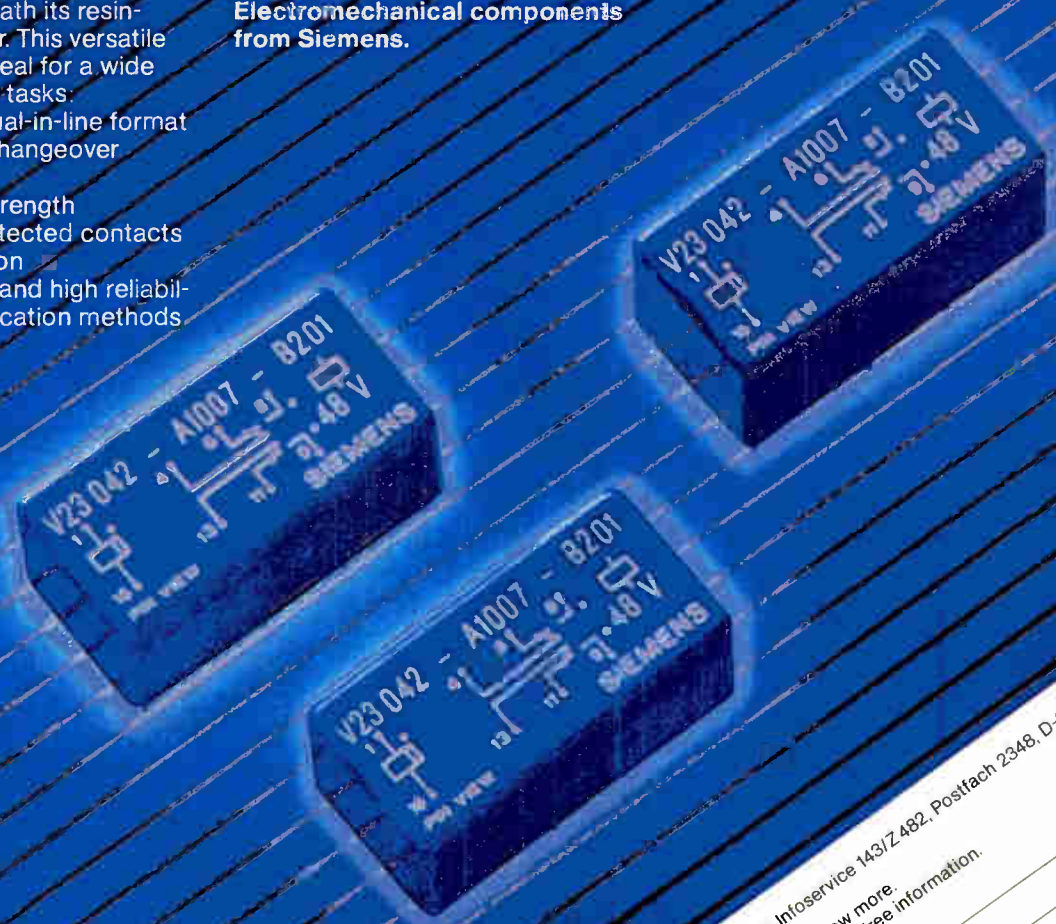
The miniature relay D2 is a typical example. Intelligent technology lies encapsulated beneath its resin-sealed plastic cover. This versatile relay is therefore ideal for a wide variety of switching tasks.

- Terminals with dual-in-line format
- Fitted with two changeover contacts
- High dielectric strength
- Atmosphere-protected contacts
- Slideless actuation
- Long service life and high reliability due to new fabrication methods

This makes the miniature relay D2 the universal interface device in every field of communication engineering.

All the other features of the miniature relay D2 are detailed in a special publication. If you would like one, please use this journal's reader service or send us the coupon.

Contacts you can rely on. Electromechanical components from Siemens.



Circle 113 on reader service card

Coupon: To Siemens AG, Infoservice 143/Z 482, Postfach 2348, D-8510 Fürth 2

Yes, I would like to know more.
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Name _____

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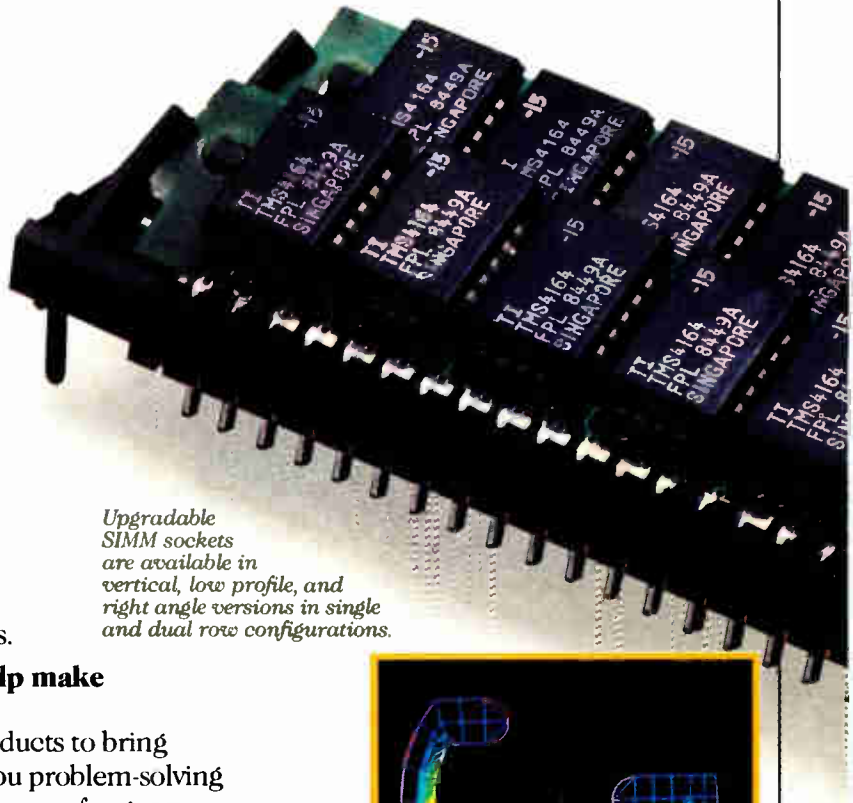

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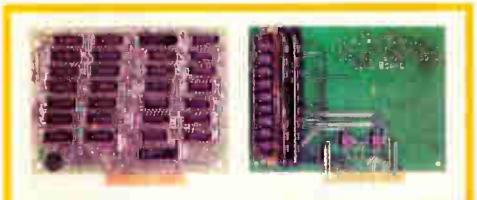
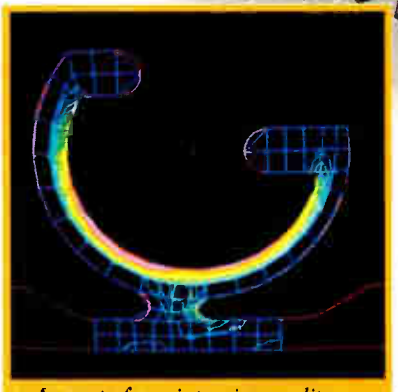


Molex SIMM socket (right) takes up dramatically less board space than DIP packaging (left).



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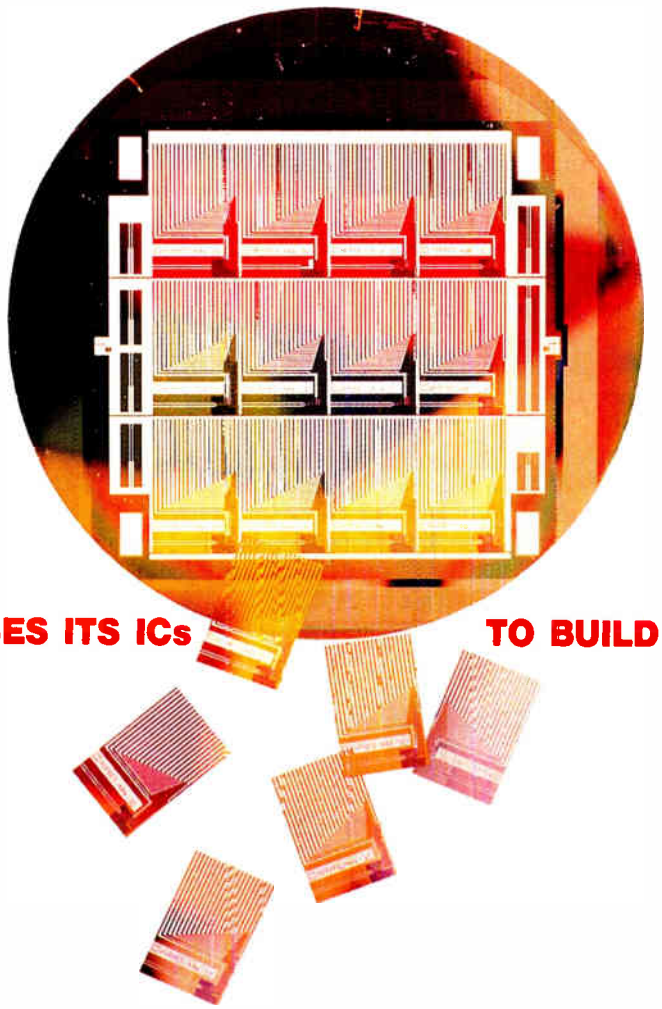
INSIDE TECHNOLOGY

FOUND!

A PRACTICAL WAY TO TURN OUT JOSEPHSON JUNCTION CHIPS



HOW HYPRES USES ITS ICs TO BUILD 70-GHZ SCOPES

by Samuel Weber

Josephson junctions, a technology that could hold the key to the ultimate in speed and density for electronic systems, have been tamed by tiny Hypres Inc. After defying for years every attempt to harness their potential, working Josephson

junction circuits are not only being turned out by the Elmsford, N. Y., company, but it is using those circuits as the heart of a new, blazingly fast instrumentation work station. The start-up company apparently is on the verge of success in a field where it has eluded such giants as IBM Corp., which has largely abandoned its efforts after spending many years and many millions, and the Japanese, who are mounting a major effort as part of the Ministry of International Trade and Industry's supercomputer program.

Hypres appears to be succeeding where IBM and the Japanese have so far failed, building repeatable, reliable devices and finding a practical application for them

The Hypres work station is the PSP-1000 Picosecond Signal Processor (see fig. 1). Operating as a digital sampling oscilloscope, the PSP-1000 far outstrips any of its competitors, exhibiting a system rise time of 5 ps, a sensitivity of 50 μV, and a bandwidth of 70 GHz. The company claims that the work station's performance specifications are five times better than those of its closest competitor.

This performance makes it possible to characterize the performance of high-speed integrated circuits and components such as emitter-coupled-logic or gallium arsenide ICs. For time-domain reflectometry, the PSP-1000 brings to bear a built-in 5-ps step generator and resolution of up to 1.6 mm when measuring the reflections of wideband transmission paths.

The work station's performance requires the blinding speed of Josephson switching devices. To take advantage of that speed, Hypres had to overcome some of the most difficult and persistent hurdles the technology presents. Chief among these were finding a practical way to cool the circuits to the extreme low temperatures necessary for the Josephson junction parts to work, and the task of producing dependable circuits that could be reliably reproduced.

Hypres solved the first problem by developing a new approach to cooling Josephson junction devices—one that eliminates much of the cumbersome equipment and complex procedure that had been needed to keep Josephson junction circuits at the temperatures required to make them function. The Josephson circuitry is all located at one corner of the chip; the rest of the chip architecture performs power operations. Only the corner that holds the logic is cooled. The cooling is done by spraying the circuitry with liquid helium, rather than by immersing the entire device in the helium.

The second obstacle was surmounted by making the circuits with niobium, rather than with lead and its alloys, which have turned out to be brittle and unreliable. Doing so allowed the company to produce reliable, repeatable Josephson junction circuits—something that IBM, which used lead and lead alloys, was never able to do, according to Sadeg M. Faris, Hypres's president and a former IBM staff member.

Measured against the goals of IBM and the Japanese, the PSP-1000 represents a relatively small-scale application of Josephson junction technology. But the successful use of superconducting electronic technology in the system has far-reaching implications.

It could be the first step toward using the devices to build compact but extremely powerful supercomputers. It also could foreshadow Josephson junction technology for a range of important applications—millimeter-wave communications, subnanosecond digital processing and analog signal processing, and high-precision analog-to-digital conversion. The potential for such applications has spurred the ongoing Josephson junction research projects around the world (see p. 54).

Hypres deliberately chose, however, to apply the technology first to a manageable project. Faris says he felt such an approach was vital to Hypres's success—that one reason other projects have failed is that they have been geared toward large-scale applications, forcing the researchers in those projects to attempt to do too much (see p. 53).

Applying the technology to even the simplest system poses enough

1. PICOSECOND PROCESSOR. Based on Josephson junction technology, Hypres's new work station can capture and analyze waveforms with rise times of less than 10 ps.

problems for a designer. Josephson junction devices must operate at near-liquid-helium temperature (4.2 K). The available refrigeration equipment is bulky and inconvenient to use, and it is extremely difficult to transmit wideband signals without significant thermal loss between cryogenic regions of the circuitry and warmer, external areas. The usual methods have been either to immerse the components in liquid helium or to thermally ground the circuit to a cold "finger" while the circuit itself was sealed in a vacuum. Both arrangements required an hour or more to change the sample and allow it to reach the desired cold temperature.

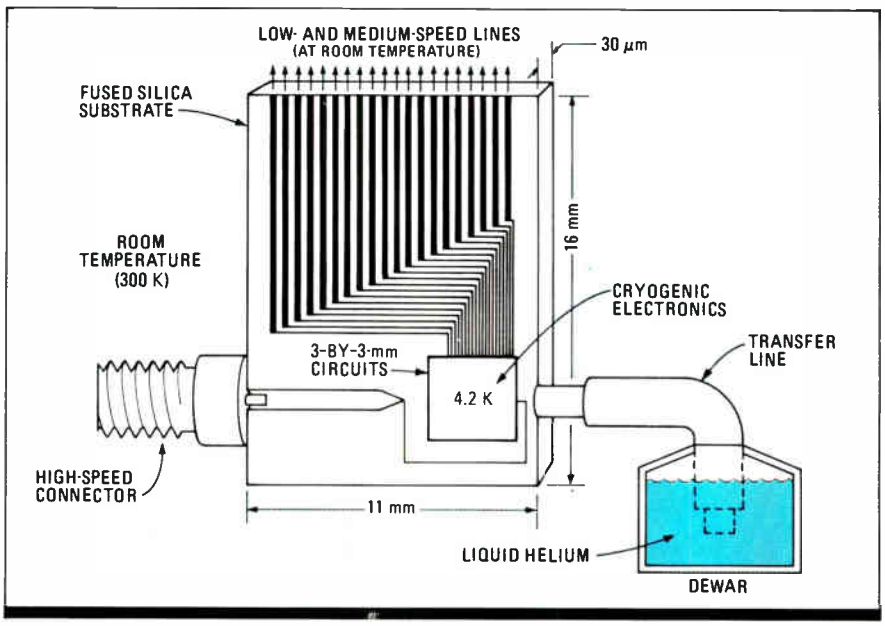
In the Hypres design, the Josephson junction circuits are situated at one corner of the chip, and that corner is cooled to superconducting temperature. The other edges, only a half centimeter away, are held at room temperature (see fig. 2). Instead of cooling the entire chip, a tiny jet of liquid helium from a small reservoir within the proprietary cooling system sprays only the active Josephson junction circuit area.

The active Josephson devices are fabricated in a niobium alloy, the use of which overcomes the problem of failure with cycling encountered when lead and its alloys are used. The circuitry is formed on a fused silica substrate. A coplanar waveguide transmission line links the circuit area to the backside of the wideband coaxial connector to which it is bonded. Low-speed bias and control lines are arrayed across the top of the chip and contact is made via a flexible Kapton substrate.

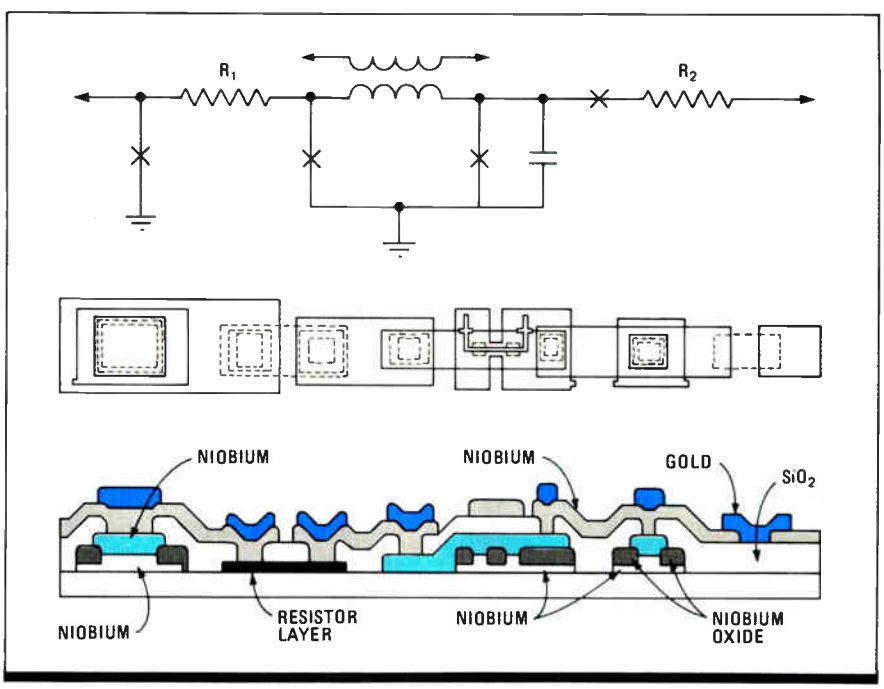
The arrangement gives the user access to the high-speed connector interface without any evidence that a cryogenic environment exists less than a centimeter behind the connector. The cryogenic circuitry consists of a step generator, strobe pulse generator, sampling gate, and electrical delay, all of which are implemented in Josephson junction technology.

The process used by Hypres employs three layers of differing sheet resistivity to form three levels of resistors, and two metal layers for interconnections (see fig. 3). The chip is produced using a conservative 3-μm geometry on a fused quartz substrate. Because Josephson junction devices are a thin-film technology and don't depend on crystalline substrates, the process can produce complex circuits on inexpensive wafers, Faris says.

"With our process and our conservative design rules, we didn't need to use a lot of expensive equipment to produce devices that can maintain highly uniform switching thresholds across the entire wafer, achieving very high yields," he says. "What's more, we'll be able to extend the process to submicron geometries inexpensively, with the capability of integrating—on one relatively inexpensive substrate [glass]—sensors, memory, and digital and analog processors,



3. COOL IT. Cooled by a controlled jet spray of liquid helium, the Josephson junction circuit is kept constantly superconducting while interfacing with room-temperature electronics.



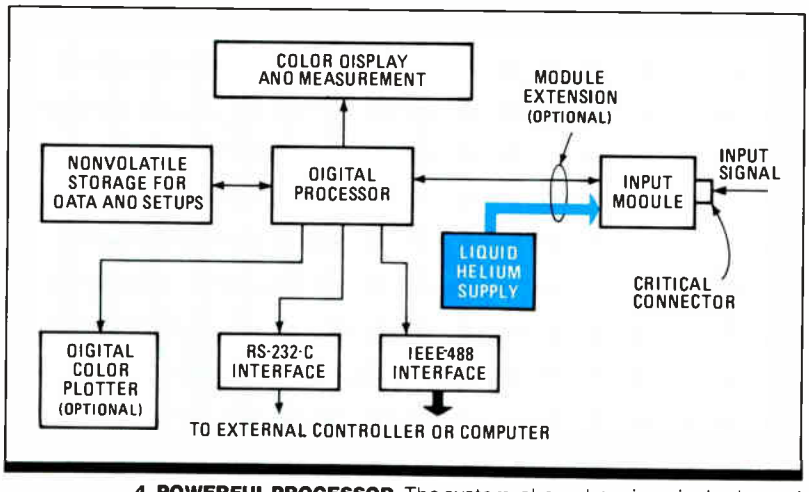
2. LAYING IT DOWN. The Hypres process implements the schematic at right by sputtering and reactive ion etching of thin-film layers of oxides and niobium.

which could open up the way to true wafer-scale integration."

In the PSP-1000, the superconducting chip is mounted in a plug-in, modular, online-replaceable measurement head. The process of changing a head takes less than a minute. Various configurations, including a dual-channel version, are available for different types of measurement samples. Each head also includes a high-speed interface and connector, a printed circuit board and the necessary cryogenic components.

The head takes only 10 minutes or so to cool to operating temperature when the work station is first turned on. When a new measurement head is installed, it comes to operating temperature within two minutes.

Cooling is provided by a helium reservoir in a dewar container mounted inside the console. It gives up to 12 continuous hours of operation or a combination of up to eight hours of continuous operation plus 16 hours of holding without helium refill. Automatic controls prevent excessive helium consumption by turning off the cooling system when the instrument is idle for more than five minutes.



4. POWERFUL PROCESSOR. The system, shown here in a single channel input version, can be configured by various options to fit the application.

The PSP-1000 itself is a fully stand-alone digital instrument that provides waveform processing and storage, powerful easy-to-use measurement and set-up aids and a high-resolution color display (see fig. 4). It consists of a $120,000 mainframe, which is configured to specific applications by the use of various input modules; these range in price from $20,000 to $45,000. It can be configured as a single- or dual-channel sampling oscilloscope or as a time-domain reflectometer, or it can be used in time-domain transmission measurements.

Up to four waveforms can be displayed simultaneously, each annotated in a matching color. All user controls are menu-driven. Each major function is assigned to a dedicated pushbutton, which calls up the desired menu. A maximum of eight soft keys associated with the menus are displayed. The user can enter or change any parameter, value, or text by selecting the appropriate soft key and inputting the desired character via the alphanumeric keys or by selecting the appropriate toggle.

A nonvolatile main memory provides storage for as many as nine waveforms with a resolution of up to 1,024 points per waveform. It can also store nine sets of calibration and setup data.

The user can enter his own formulas to operate on any waveform to present data in the most meaningful form. Built-in operations include fast Fourier transforms, multiply, divide, integrate, and differentiate functions. Two vertical and two horizontal markers facilitate accurate reading of waveform features. Portions of the waveform within either the x or y markers can be magnified for easier viewing.

Each channel in the PSP-1000 can have its own independent time base and can be triggered from its own signal. Alternatively, the two channels can be synchronized via a user-supplied external, independent pretrigger. The horizontal deflection factor with a full scale of 10 divisions can be set from 2 ps to 1 ns/division. The vertical sensitivity ranges from 50 uV to 5 mV for input scales of 10 mV to 1 V.

Time-domain measurements give the user localized information on a device under test. For example, with time-domain techniques, the PSP-1000 can determine impedance and characterize transmission faults in millimeter-wave devices and circuits in the 50-GHz region, which is used in high-frequency radar and communications. With a time-domain-reflectometer module, propagation delay in the order of tens of picoseconds can be measured. The TDR step pulse, with its fast 5-ps rise time, is used both for exciting reflections and to measure the transmission delay and loss.

The work station and the circuitry it uses are just the first step. Faris says Hypres is well along in developing its process so it can utilize niobium nitride, which would raise the critical threshold temperature of their Josephson junction circuits to 16°K. This could lead to more compact, closed-cycle refrigeration systems that would not require the handling of costly liquid helium. And the recent reports of new refractory materials that move the threshold temperatures even higher [*Electronics*, Jan. 22, 1987, p. 37] has him enthusiastic about the future prospects of superconducting electronics. □

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HYPRES: GETTING THE REST OF THE WORLD IN STEP

Starting an electronics company is something like making a soufflé: even if you combine the right ingredients in a controlled atmosphere, the whole thing can cave in before it ever gets out of the oven. For Hypres Inc., an Elmsford, N. Y., startup specializing in ultra-high-speed Josephson junction technology, the recipe for success was particularly complex, since the company's goal is to commercialize a technology that many people believe is impractical.

Convincing them otherwise will be no small task—much larger companies have failed to master Josephson circuitry. IBM Corp., for one, spent several years and hundreds of millions of dollars before giving up and dropping the technology in 1983. "If IBM spends $300 million on a technology and dumps it, guess what?" asks Hypres's founder, Sadeg Faris. "Ninety-nine percent of the people think the technology is a loser."

Faris, in fact, worked on the IBM project; he spent eight years at IBM's Thomas J. Watson Research Center in Yorktown Heights, N. Y., studying Josephson circuits, which rely on the superconductive effects some materials enjoy when cooled to temperatures approaching absolute zero.

The advantages of the technology are ultra-high-speed processing, many times faster than silicon or gallium arsenide circuitry, and minimal power consumption. Faris says his devices have demonstrated switching speeds of 3 ps using 6-μm linewidths. By reducing the geometries to the 1-μm state-of-the-art and taking advantage of recent advances in superconductor technology [*Electronics*, Jan. 22, 1987, p. 37], typical switching speeds could approach 0.05 ps; typical switching speeds for GaAs circuits can range up to 400 ps. At the same time, GaAs power consumption is roughly 1 mW to 5 mW per gate at top speed, while current Josephson circuits dissipate about 1 μW per gate.

The major drawback lies in the need for a low operating temperature. For the circuitry to work, one chip may require several pieces of cumbersome cooling equipment.

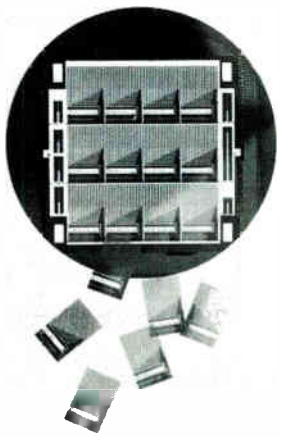
Faris says he decided early on that if Josephson technology were ever to be commercially worthwhile, it would have to sneak into the market in "small-scale applications," much as vacuum tubes and transistors were first popularized as components in radios and the like. He reasoned that to try to build a computer before the technology had earned a chance to mature would be to strike a death blow to the whole idea. That, he says, is what doomed Josephson junction work at IBM.

So in 1983, convinced that his employer was setting its short-term goals too high, Faris set out to do for Josephson junction technology what Texas Instruments Inc. and others did for the transistor: develop confidence in the technology by introducing it in small-scale products. The strategy was to start small—and think big.

Accordingly, Hypres's first product is a high-speed instrumentation work station (see p. 49) that employs a Josephson integrated circuit as its core element. Faris says he's having no trouble finding customers for the $120,000 instrument. And test and measurement will continue to be a major part of Hypres's thrust, since the extreme speed of Josephson technology is particularly well suited to such applications as qualifying gallium arsenide and other high-speed circuitry.

But Hypres, which derives its name from "hyper-performance research," will also seek other applications, as well as going after government business,

SADEG M. FARIS



Faris says. The company currently has four government contracts worth a total of almost $1 million to develop thin-film superconducting materials for Josephson circuits; advanced cryogenics for cooling the circuitry; interconnection technology to allow the super-cooled Josephson devices to communicate with room-temperature circuitry; and advanced integrated circuits that can be used for highly sensitive millimeter-wave communications.

And Faris has not given up his dream of some day building a computer from Josephson circuitry. He says he could build a system as powerful as an IBM 3090, yet as small and portable as a trio of desk chairs.

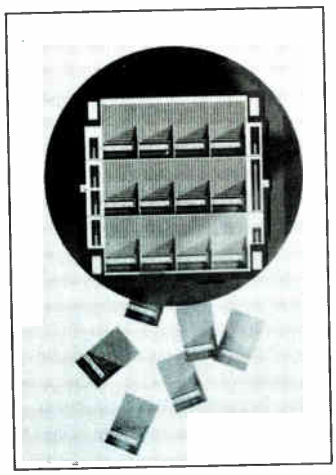
In the meantime, Hypres itself is a dream come true for him. The eldest of seven children, Faris, 41, was born to illiterate parents in Tripoli, Libya. When he was 11, his father died, and Faris was sent to an orphanage, where he was able to earn enough money to help support his family. At the same time, he did well enough in school to place third in a national exam that won him an Exxon Corp. scholarship to study in the U. S. He earned a BA, MA, and PhD in electrical engineering and computer sciences from the University of California at Berkeley, then joined IBM.

Now a U. S. citizen, Faris considers his success the archetype of the American dream. But he is by no means complacent, and hopes to be able to expand his business rapidly. Backed by a venture-capital group led by E.M. Warburg Pincus and Co. of New York, Hypres employs about 50 people. By the end of the year, Faris says, he hopes to have 75 people in his two plants. In the long term, Faris wants to find a partner to help develop and market what would be his crowning glory—a Josephson junction computer. *–Tobias Naegele*

SUPERCONDUCTOR R&D MOVES AHEAD ON SEVERAL WORLD FRONTS

Evidence builds that decades of effort may finally make Josephson junctions practical

by Wesley R. Iversen



It's been a long wait, but more than two decades of worldwide research into superconductive electronics may finally be accelerating toward a payoff. An important milestone for a technology that's always been long on promise but short on practical success is Hypres Inc.'s introduction of a world-beating digital oscilloscope based on Josephson junction devices (see p. 49).

Another positive sign is the progress being made with new materials that are superconductive at higher temperatures. These materials are raising hopes of systems that are much easier to implement because of their simpler cooling requirements.

More encouragement comes from the U.S. military. Defense Department funding of superconductive electronics so far is still small, but interest is growing at the Pentagon—spurred in part by fears that Japanese work in the area will earn them a big lead in supercomputers. Such concerns first arose when IBM shut down its Josephson-based computer program in 1983, although they have abated somewhat as facilities for building the devices have been established at Hypres, TRW, and Westinghouse. Among the military's efforts is the Terahertz Initiative, which will explore the feasibility of Josephson-based imaging radars and other military systems operating in the terahertz region.

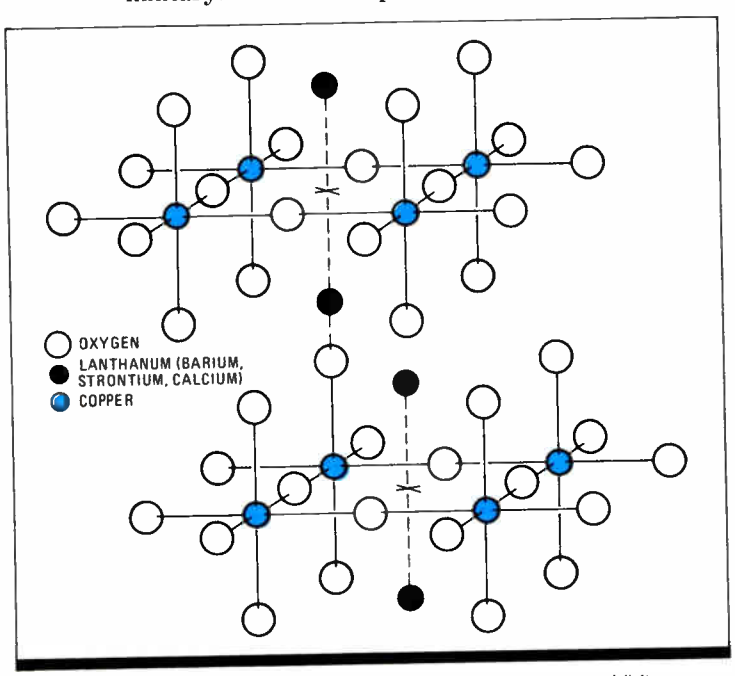
Commercial projects are picking up steam, too—Hypres, an Elmsford, N.Y, startup, isn't the only U.S. company pursuing the current generation of niobium-based Josephson junctions. Biomagnetic Technologies Inc., San Diego, believes that a significant market will develop within two years for ultrasensitive biomedical equipment based on Squids (superconducting quantum interference devices), which are made with Josephson junctions.

Two years ago, the outlook for Josephson junctions appeared to be bright [*Electronics*, Feb. 25, 1985, p. 28], but progress has been at a snail's pace. The lack of major developments in the field can be traced in large part to the damper IBM's decision put on research and the kinds of difficulties IBM was having with materials. Low levels of Pentagon research funding and the extreme cryogenic demands of known superconducting materials were also factors.

So, possibly the most important recent development involves a startling advance in superconducting materials [*Electronics*, Jan. 22, 1987, p. 37]. The discovery last winter of ceramics that superconduct at heightened temperatures captured the attention of the research community.

Building Josephson junctions that work at 30 K to 40 K, the critical temperature (T_c) range being reported for the new materials, could drastically reduce the cryogenics problem associated with superconducting electronics. It would eliminate the 4 K liquid-helium cooling systems required for today's lead- and niobium-based junctions, which go critical at about 7 K and 9 K, respectively. Superconductive systems based on 20 K liquid-hydrogen cooling systems, for example, could be much less costly and complex.

The first of the new ceramics (see fig. 1) was reported last April by IBM Corp. researchers in Zurich, Switzerland. Researchers worldwide have since duplicated the IBM work using compounds of lanthanum, barium, copper and oxygen, or in



1. SUPERCERAMIC. IBM first reported finding a compound that exhibits superconductive properties at much higher temperatures than materials now used.

some cases substituting strontium for the barium. New records for the highest T_c are now being set with regularity. One group at the Institute of Physics at the Chinese Academy of Sciences in Beijing reports a T_c of 70 K.

But if they are ever to be useful, the new materials must first be fabricated in thin-film and wire forms with the high critical temperatures and other properties needed for application work. Researchers are already tackling that task. "A lot of the people we fund have dropped off what they were working on and started working with the new material," says Harold Weinstock, program manager of electronic and materials sciences at the Air Force Office of Scientific Research in Washington. AFOSR annually funds about $2 million worth of superconductive research at about a dozen U. S. labs.

HARD TO WORK WITH?

But the materials may be hard to use, warns Richard D. Blaugher, manager of the Cryogenic Technology and Electronics Department at the Westinghouse Research and Development Center in Pittsburgh. Making wire with them looks particularly difficult, Blaugher says.

Others are more optimistic. "I feel very confident that there will be thin films, and there will be some kind of wires," says Theodore Geballe, a Stanford University professor of applied physics who has already begun thin-film work using sputtering techniques.

In the best case, researchers agree, significant superconductive device work based on the new oxides is still several years away. But in the meantime, some think the materials development will help spur greater funding by the Department of Defense. Pentagon spending dedicated to superconducting research is now only about $5 million per year, says Weinstock. "With these new materials," Weinstock says, "I'm hoping I can convince people that we ought to be putting a big shot of money into this technology."

Another argument for increased Pentagon spending on superconducting research involves the Japanese. NTT, NEC, Hitachi, Fujitsu, and the government's Electrotechnical Laboratory have already grabbed a leading position in work aimed at digital Josephson device fabrication (see "Reports of Japanese project's death are greatly exaggerated," p. 56). If the Japanese can build a Josephson-based computer, some DOD sources fear, it could make the U. S. dangerously dependent on a foreign source for an advanced technology crucial to national defense.

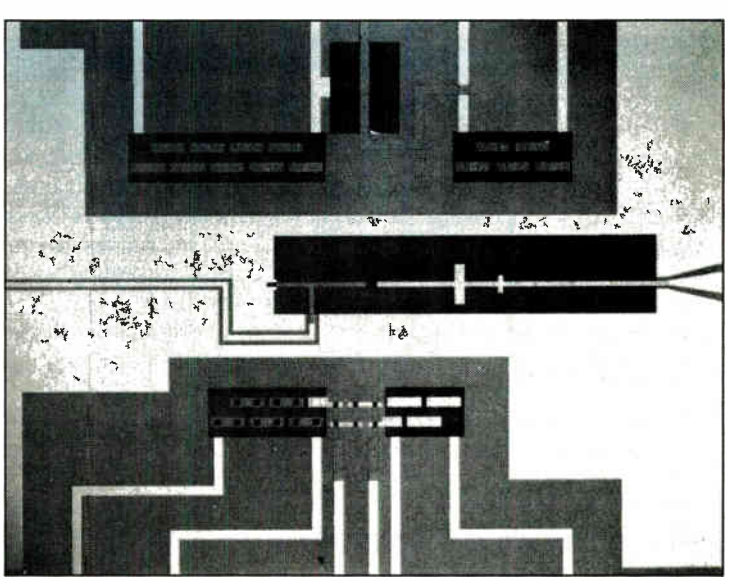
Those concerns began to mount in September 1983, with IBM's decision to scrap its effort. Some say a big part of IBM's problem was its use of lead-based junctions, instead of more advanced devices based on Nb and NbN. These materials are harder to make, but are better able to withstand temperature cycling.

In any case, IBM's decision to quit left the U. S. without a facility for fabricating superconducting logic circuits at the 100-plus-gates level of integration. "The major concern has not been that the Japanese would come up with a novel idea in circuit design, but that if they did, that nobody in the U. S. would able to implement it," says Martin Nisenoff, head of the applied superconductivity section for the Naval Research Laboratory's Electronics Technology Division, Washington. Those fears have abated somewhat as U. S. companies have begun moving into the vacuum left by IBM, developing clean rooms with equipment for Josephson device fabrication that rival those of the Japanese, Nisenoff says, citing facilities at Hypres, TRW, and Westinghouse.

Besides the promise of new superconductors and the threat of foreign domination of the field, another major impetus for military Josephson research is the Strategic Defense Initiative. One SDI program devoted exclusively to Josephson research is the Terahertz Initiative. The program will explore the feasibility of using superconducting signal-processing technology in space-based microwave systems. Terahertz funding began last September and over three years should come to about $4 million, says Dallas Hayes, an official at Rome Air Development Center, Hanscomb AFB, Mass., who is overseeing the effort.

TRW, Westinghouse, Hypres, and several universities are involved in the Terahertz project. TRW plans to develop a 100-GHz receiver on a chip and has already built a Josephson-based parametric amplifier with extremely low noise (see fig. 2). Other work includes development of terahertz-region Josephson devices with high critical current, phase shifters, an analog range doppler processor, arrays of junctions capable of producing high coherent-power output, analog-to-digital converters, wafer-scale-integration techniques, and shift registers.

Josephson junctions will also be one of the



2. AMPLIFIER. This Josephson junction chip built by TRW carries a low-noise parametric amplifier. TRW is working on the Pentagon's Terahertz Initiative.

technologies assessed under a $9.6 million SDI contract awarded to Rockwell International last September. The project will look at the technologies needed to meet SDI goals in on-array signal processing for use in infrared mosaic sensor systems, says an Army source.

Other military projects, and much commercial work, will draw on the promise Josephson technology holds for analog applications that don't require dense circuit integration. Magnetometers and gradiometers built with Squids offer near-ultimate sensitivity. They also offer extreme precision and stability, as well as potential for the lowest noise levels of any circuit type. These properties are already being exploited in applications ranging from submillimeter-wavelength radioastronomy to Squid-based laboratory instrumentation used to detect subatomic particles.

An experimental submarine detector and locator using Squid technology works at sensitivity levels up to 1,000 times greater than conventional magnetic devices

Both the Air Force and the Navy are funding a smattering of projects in analog superconductive electronics research. The Navy, for example, plans to award a "sizeable" contract in August that includes development of Squid-based equipment for submarine detection, says Gary J. Kekelis, a branch head at the Naval Coastal Systems Center in Panama City, Fla. Field tests have already been performed with an experimental Madair (for magnetic anomoly detection and indentification plus ranging) system based on gradiometers built with early-generation Squids. These systems have demonstrated reliable sensitivity levels 100 to 1,000 times better than conventional magnetic detection devices can achieve.

And a major civilian market for medical instrumentation based on Squid-based sensors appears to be just around the corner, says William C. Black, senior vice president at Biomagnetic Technologies. The company makes magnetoencephalography (MEG) equipment using Squid-based magnetometers that can detect magnetic fields in the human brain so small—down to 5 femtoteslas—they can't be detected by other means.

MEG reads the magnetic fields associated with electrical brain signals without the use of electrodes implanted in the brain. It can pinpoint the location of neural firings, which means it has vast potential for understanding neurological disorders. One Air Force project is experimenting with MEG as a way to study the effect of heavy workloads on the brain, with an eye toward improving cockpit design, sources say. □

REPORTS OF JAPANESE PROJECT'S DEATH ARE GREATLY EXAGGERATED

Despite what some recent front-page reports in U. S. newspapers have said, the Japanese are committed to Josephson junction work for the long term. The country's Josephson junction research effort is driven by a government supercomputer project involving four laboratories—the government's Electrotechnical Laboratory, and labs at Hitachi, Fujitsu, and NEC—and also by an independent effort at the Nippon Telegraph and Telephone Corp.

The Japanese will begin designing a supercomputer using high-electron-mobility transistors and more conventional silicon devices, including perhaps cooled CMOS, this April, but work on Josephson junctions will continue. A number of experimental computer building blocks made with Josephson junctions are already working, although the level of integration is still relatively low.

In the government project, it appears that NEC is developing memory and Hitachi and Fujitsu are developing logic. Each company has about 10 researchers working on the project, about the same number as the government lab. NTT, Tokyo, has the largest group, perhaps as many as 40 persons in four laboratories, but it declines to talk about the number of personnel or what they are doing. Some of them belong to basic research and materials groups whose work may be only indirectly related to Josephson junctions.

Hitachi Ltd.'s Central Research Laboratory in Tokyo still favors threshold logic, but it has switched from the niobium-lead junctions that it had used previously to niobium–aluminum oxide–niobium junctions. Capacitance per unit area is about half that of niobium oxide and switching speed is thus about twice as fast. The junction area of current experimental devices measures 1.5 by 1.5 μm, and critical current density is 5,000 A/cm^2. Operation is at liquid-helium temperatures.

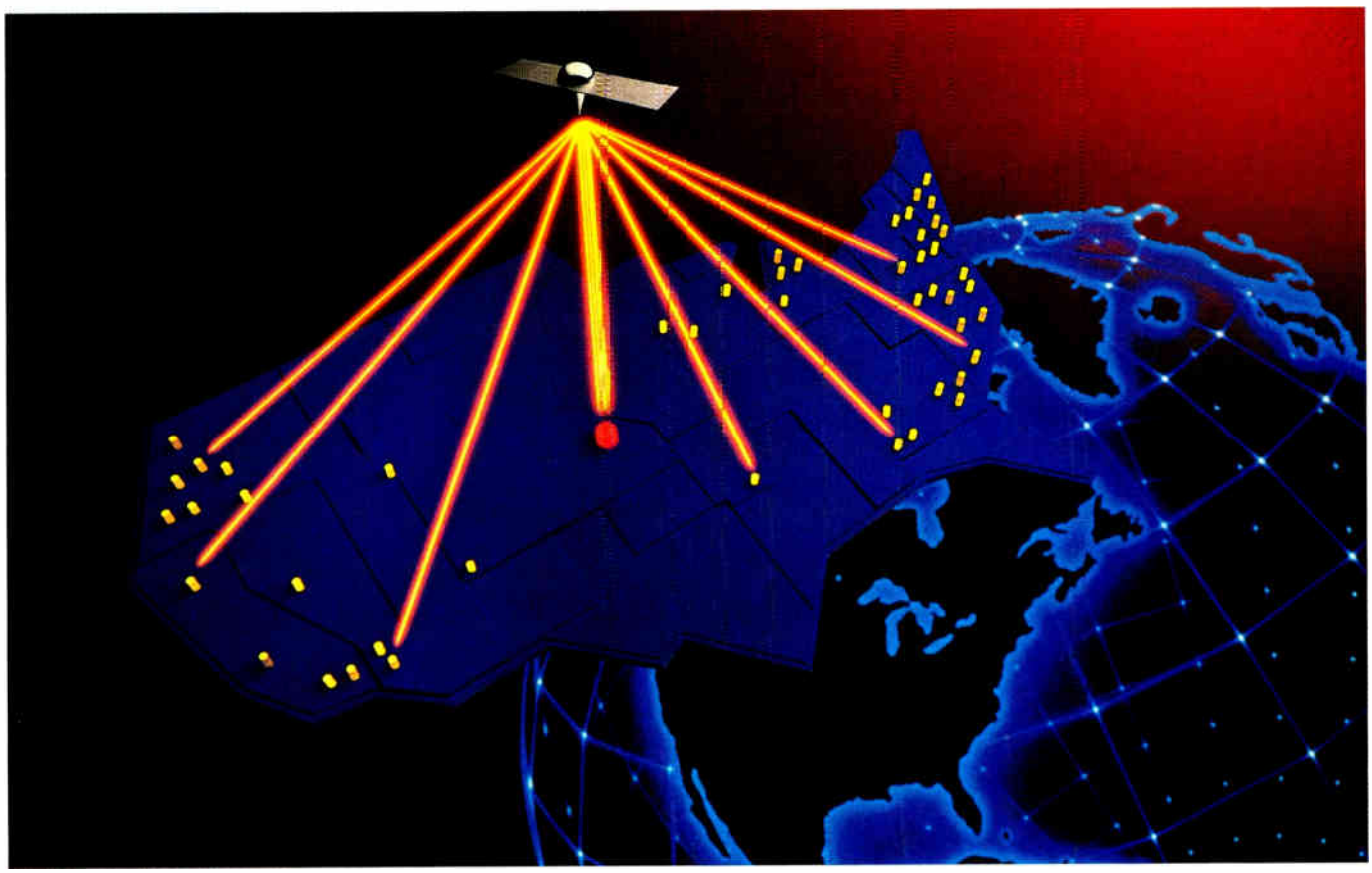
A 4-by-4-bit multiplier Hitachi has built with Josephson junctions has a total of 109 logic elements, critical-path multiplication time of 210 ps, and power dissipation of 3 mW. A scale-of-eight counter with 16 logic elements operates at input frequencies up to 11.9 GHz. Power dissipation is 0.4 mW.

Hitachi has also developed a 3,264-gate array with 544 logic cells. Each logic cell consists of four magnetically coupled Josephson interference devices used as OR gates and two direct-coupled Josphson devices used as AND gates.

Niobium–aluminum oxide–niobium is also favored by the Electrotechnical Laboratory in Ibarakin, Japan, which has developed a 2-bit-slice arithmetic-logic unit that features a new circuit configured exclusively with Josephson junctions. The circuits provide gain and isolation despite the elimination of the inductances previously used to get them; doing without inductors also permits greater integration and makes for higher reliability. The ALU slice is designed for look-ahead-carry adder configurations rather than ripple-carry types to demonstrate its suitability for serious computer designs. The scale of integration is still small, but chips can be cascaded for greater bit width. Propagation delay is about 13 ps/gate and total power dissipation is 270 μW.

The group has also developed other circuits needed for computers, including a multiplier, latches, registers, and program counters—in fact, the government-led group is working to assemble all the building blocks needed for a computer.

–Charles L. Cohen



"NEXTAR" MINI EARTH STATION NETWORK.

Private Ku-band satellite communications networks using mini earth stations on customer premises are poised to take off in the US.

Our advanced mini earth station networking system "NEXTAR" offers unprecedented flexibility for transaction-oriented businesses typically using POS, ECR and ATM systems.

The NEXTAR provides interactive data communications between a central hub and many widely-dispersed remote mini earth stations in a "star" network topology. Our exclusive Adaptive Assignment TDMA system automatically assigns the best pathway for each data message to minimize response time for short interactive messages and increase throughput during long batch transmission. NEXTAR transparently interconnects existing remote terminals and the host's front-end processor thanks to its intelligent network features.

The mini earth station, a 1.2 or 1.8m antenna with an integral RF package and compact indoor unit, takes less than a workday to install. Site selection and licensing are also simplified with the Ku-band. The central hub station with comprehensive monitoring, control and diagnostic capabilities can be located adjacent to a data center or at a shared site.

The NEXTAR network can be custom-tailored to a user's exacting needs—data rates from 75bps to 56Kbps plus voice and video capability. It eliminates the wasted transmission capacity and high cost of traditional alternatives.

C&C
Computers and Communications

NUMBER 137

1.3-MICRON OEICs FOR GIGA-BIT LINKS.

Scientists at the NEC Optoelectronics Research Laboratory have successfully tested the world's first optoelectronic ICs to operate in the 1.3μm band at data rates of 1.2Gbps.

The optical transmitter and receiver chip pair set records of a 12-km communication at 1.2Gbps with a 7.7dB margin, and 22-km transmission at 565Mbps with a 9.9dB margin in the experiment using a single-mode fiber.

The new light-emitting chip incorporates a 1.3μm DC-PBH (double-channel planar buried heterostructure) laser diode and three InGaAsP/InP hetero-junction bipolar transistors on the same InP substrate. Modulation up to 2Gbps is possible in NRZ mode. A peak output of 20mW was marked at 1Gbps.

The optical receiver integrates a PIN photo diode and three low-noise InGaAsP junction FETs on a single chip for sensitivity of −14dBm at 1.2Gbps.

NEC's new OEIC pair will be the ideal workhorse in medium- or short-distance ultra-high speed links including LANs, local subscriber loops and interconnections of computers and peripherals because it promises much lower cost and smaller size than prevalent discrete devices.

These OEIC devices will reach the market within a few years.

NEAX61 NOW IN SERVICE AT 1,002 EXCHANGES.

Our NEAX61 digital switching system continues to play a key role in the phenomenal expansion of digital networks around the world.

Since its implementation in 1979 the NEAX61 has captured the attention of telecommunications administrators globewide for its sophisticated modular hardware and software, advanced service features, and full operation and maintenance support.

Today there are NEAX61 switches in service at 1,002 exchanges in 37 nations—more than 5 million equivalent subscriber lines in all. With recent orders from New Zealand (400,000 lines), Hong Kong (600,000 lines) and Venezuela (330,000 lines) the aggregate orders received now exceeds 10 million equivalent subscriber lines.

NEC OPTICAL REPEATERS GO TRANSPACIFIC AND SUBMARINE.

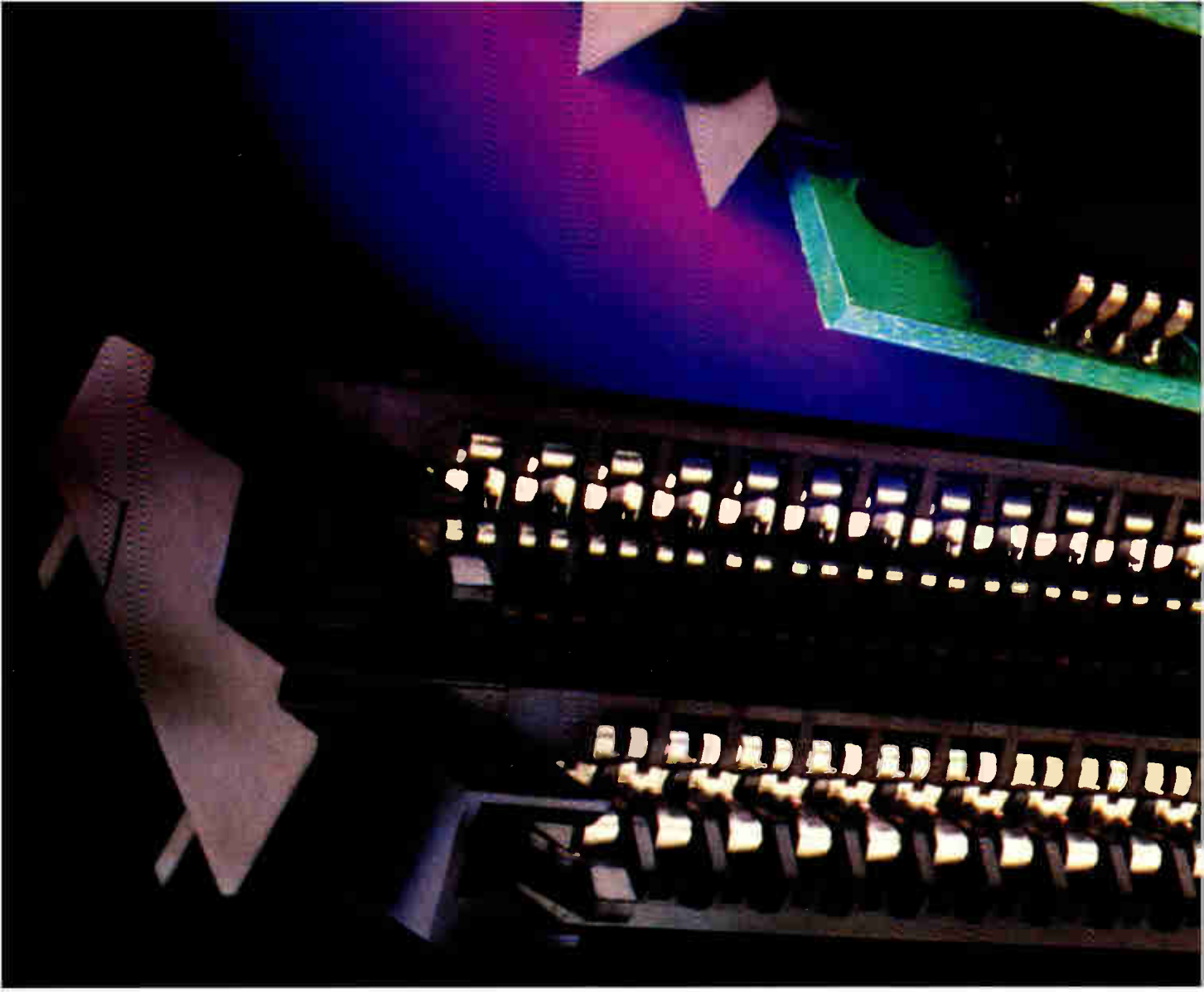
The trend in transoceanic submarine cable systems is undeniably "optical". The use of fiber optic transmission technology increases capacity, extends repeater span and ensures compatibility with land-based digital networks.

Under a contract awarded by KDD, Japan's leading international telecommunications network, NEC is manufacturing optical submersible repeaters and optical terminal equipment for the third Trans-Pacific Cable (TPC-3) which will link Hawaii and Japan with a branch to Guam.

The TPC-3, to be completed in 1988 and owned by 22 telephone operating companies in 10 countries, will have two 280Mbps systems, offering a total capacity equivalent to 7,560 telephone channels—a dramatic increase from 138 channels with TPC-1 and 845 channels with TPC-2.

Incorporating our 1.3μm DC-PBH (double-channel planar buried heterostructure) laser diodes and newly-developed high-speed monolithic ICs, the optical repeaters are designed to maintain high reliability on the ocean floor at a depth up to 8,000 meters.

NEC



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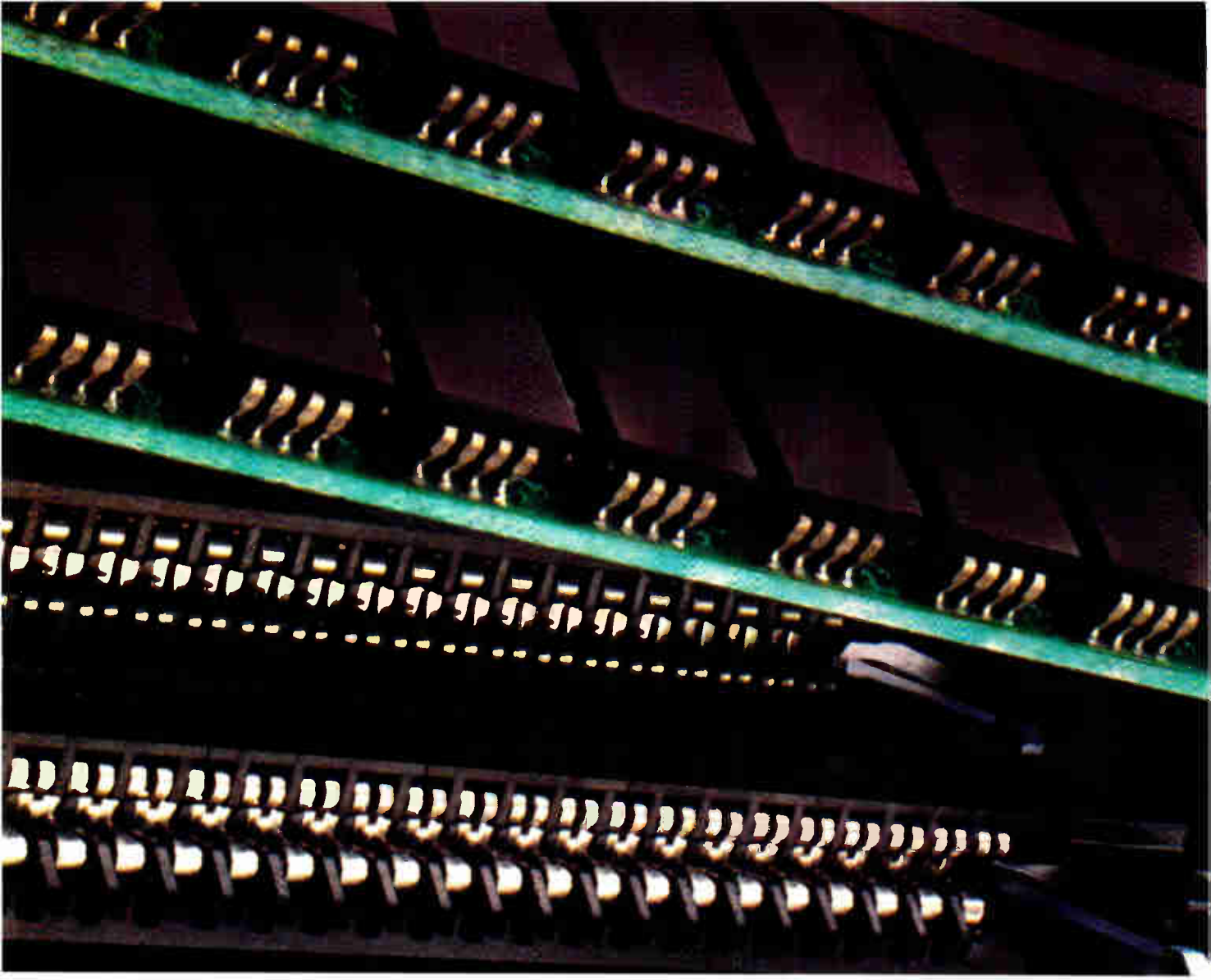

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All utilize our exclusive high-normal-force "floating" contact system, too—positive wipe gas-tight interface, with complete independence from housing materials for long-term integrity.

And all are designed for compatibility with industry-standard processing equipment—with high-temperature materials, close-tolerance soldertail positioning, closed-bottom housings, robotic pick-up details.

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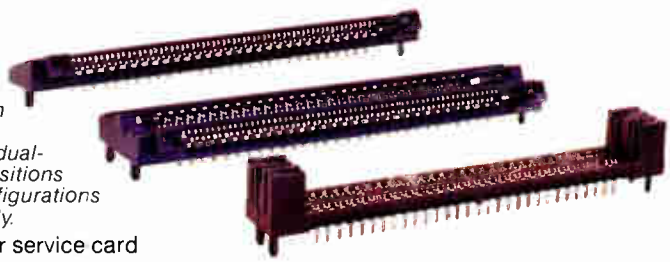
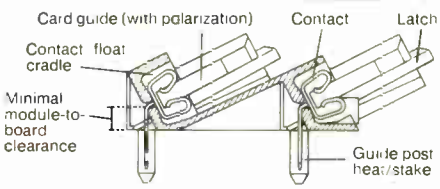


Vertical single-row sockets in 12-42 positions, slanted single-row sockets in 22-42 positions, and vertical and slanted dual-row sockets in 30 positions available. Other configurations to be available shortly.

Circle 61 on reader service card



High-pressure tin-to-tin contacts provide reliable performance. Contacts with select gold plating also available.

HIGH-POWERED DESKTOP IMAGE PROCESSING GETS CLOSER

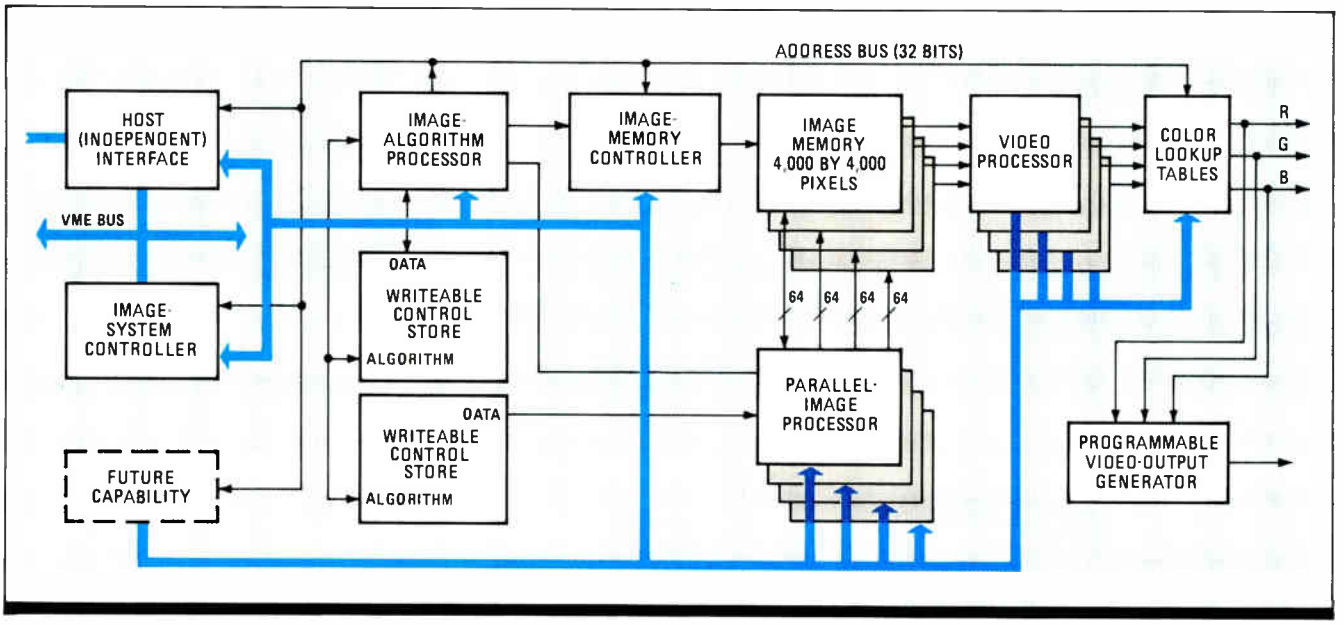
With its custom and semicustom chips, Visual Information Technologies is aiming for a $5,000 desktop computer that can handle high-end image processing

Picture this: a $5,000 desktop machine that can perform high-end image processing tasks at the rate of 500 million operations per second, at least five times the current rate of desktop machines. That's the 1990 goal of Visual Information Technologies Inc., a Dallas-area startup.

VIT plans to make such a system feasible with a fistful of new custom and semicustom very large-scale integrated circuits. It also is creating a universal software environment out of emerging computer-graphics standards to help equipment integrators devise new systems of analysis, enhancement, or modification of stored images.

VIT's first product will be a development system this summer containing the VITec Image Computer. The set of boards and the software that make up the Image Computer will probably cost around $35,000 when they become available during the next year. The company also is developing more custom ICs that will reduce the system to one board. Most customers are likely to use the VITec Image Computer in sophisticated work stations, but VIT or another company probably will turn out an inexpensive desktop image processor based on a personal computer.

Image-processing systems are widely available today, but high performance can cost hundreds of thousands of dollars. Nor do compatible software environments exist across all classes of computers. VIT aims to change that with its universal image-processing environment. Many of its software concepts are drawn from a set of graphics standards



1. COUPLED. The VITec Image Computer's current configuration couples an image memory to four parallel image processor ICs cascaded together.

known as Phigs, which stands for the Programmer's Hierarchical Interactive Graphics System. VIT is also incorporating the proposed work-station windowing standard known as the X Windows System [*Electronics*, Jan. 22, 1987, p. 58].

Unlike computer graphics environments, image processing deals with the manipulation of stored images captured from the real world: a photograph, for example, that has been scanned into the equipment. VIT is one of a number of companies betting that image processing has a big future in applications that range from electronic publishing to satellite mapping (see p. 65).

As well as aiming to put image processing into the computing mainstream, VIT is shooting for a single-board subsystem that will run on a variety of hardware. Officials of the Plano, Texas, company envision a kaleidoscope of compatible image-processing computers using the subsystem that they are calling the VITec Image Computer. Some would be based on personal computers with low-resolution video displays. More expensive image processors could have high-resolution displays, while other VIT systems might be embedded in high-quality printers for full-color hard copies of images.

To that end, the company is now readying the VITec Image Computer. This parallel-processing subsystem will couple multitasking software containing a new set of image-processing primitive routines with new ICs—application-specific processors and a special memory controller—and banks of commodity video random-access-memory chips.

Company cofounder James A. Fontaine, who is chairman and marketing vice president of VIT, says that the VITec Image Computer will be targeted at offices, graphic arts departments, publishing, scientific research, engineering, and medicine. Within the year, VIT plans to ship its first production version of the VITec Image Computer boards, costing about $25,000 a set.

VIT starts its market push with a development system containing a fully operating three-board VITec Image Computer. The $200,000 development system is based on a Sun Microsystems Inc. work station. VIT says its development software provides equipment integrators with 70% of the algorithm and application programs needed to produce a powerful image processor.

"The system is targeted at designers of computer-graphics systems who now want to develop image computing equipment," says David M. Pfeiffer, vice president of engineering who along with Fontaine founded VIT in 1984. "They want to do a little image processing—scale, rotate, and filtering to make an image look better—but graphic standards do not deal with imaging models."

VIT has reduced image-processing algorithms to their simplest terms and loaded them into microcode for fast execution by the 32-bit image-algorithm processor and parallel image processors, known as PIPs (see fig. 1). Both the algorithm processor and the PIP are specialized single-cycle reduced-instruction-set computers. The program sequencer in the algorithm processor controls the PIPs.

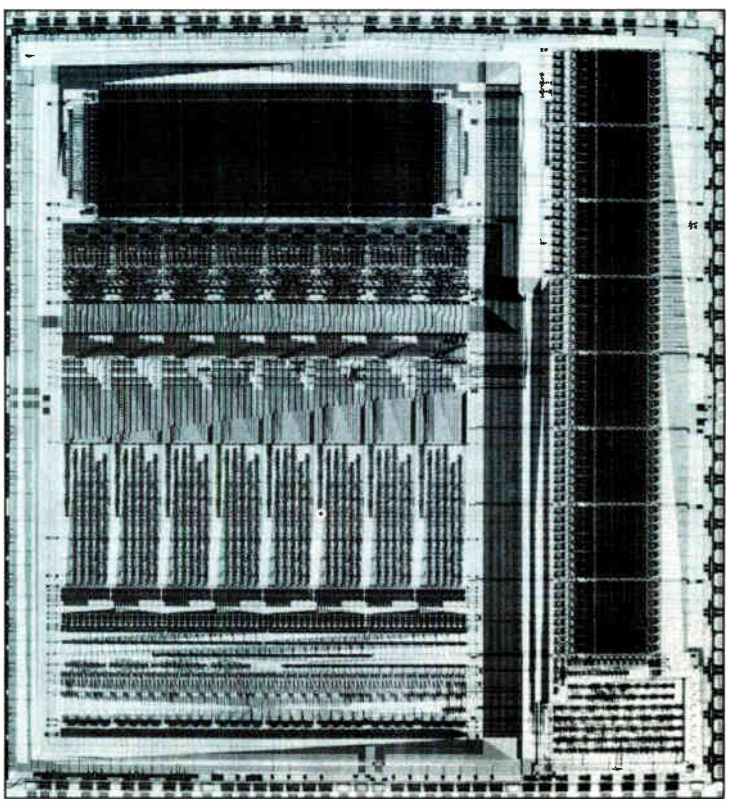
The image computer's current configuration tightly couples image memory, composed of dual-port video RAM chips, to four PIPs cascaded together. The four PIP chips can access 256 bits of pixel data from the image memory at a time.

The first VITec Image Computer will take up three boards, but during the coming year the company plans more custom ICs that will reduce the system to one board

Systems can contain from two to eight PIPs.

The PIP portion of the system acts as a multiple-instruction, multiple-data-stream parallel processor as it computes pixel data. The algorithm processor is a single-instruction, single-data-stream chip performing image processing and graphics address calculations in a single cycle. "The whole idea of this tree-structured parallel-processing architecture is that in image computing you need parallelism in data but not on the address side," explains Pfeiffer. "Image processing typically has a very clean division between address functions and data functions."

The full-custom CMOS PIP chip (see fig. 2) contains a pipeline consisting of a 2-K, four-port



2. PARALLEL WORK. The PIP chip acts as a multiple-instruction, multiple-data-stream parallel processor as it computes pixel data.

register file; eight arithmetic logic units; eight alignment replicators that align pixels; eight replicators to replicate pixels on the screen; eight 10-by-10 multipliers; eight 32-bit accumulators; a convolver; a barrel shifter; the writable control store; and four 64-bit data buses.

A quartet of video processors makes up the heart of the system's video output section. Each 149-pin video processor translates 64 bits of parallel image data from the image memory into 8 bits of digital video-display data. The emitter-coupled-logic processors have an on-board 64-bit shift register. Output serial data from the video processors enters a lookup table made of fast ECL static RAMs that translate and map the stream to 16 million possible color intensities.

Initially, two of VIT's chip designs are being employed inside the development system. One VMEbus board has four PIP chips and four 107-MHz video processors. VIT is getting its CMOS PIP chips made by two silicon foundries, VLSI Technology Inc. and Sierra Semiconductor Corp. The video processors are based on an ECL gate array from Motorola Inc.

A second VMEbus board contains the 32-bit image algorithm processor, which is presently implemented with bit-slice circuits and fast programmable logic. A third board acts as the system's highly specialized image memory controller, which automatically refreshes the large array of video RAMs, generates video signals, and provides timing for the VITec computer.

During the coming year, the algorithm processor and memory controller each will be integrated into a CMOS chip. When those tasks are done, the entire VITec Image Computer will fit on one 14-by-15-in. Eurocard, says Pfeiffer.

VIT expects that designers of present-day computer-graphics systems will be moving into the image processing arena, so it is tailoring its software to these designers. Similar to the Phigs standard used in computer-graphics systems, the VITec Image Computer is display-list driven, using an ordered series of commands and attributes to manipulate, enhance, and change images in a data base. The VITec software has been tailored to handle real-world image data bases instead of computer-created graphics.

And, to ease software development, VIT has borrowed concepts from mainstream memory management techniques to create what it calls Virtual Image Processing. By automatically managing and allocating image memory space, this technique helps application programmers handle images exceeding the system's 8,000-by-8,000-pixel maximum physical storage. The virtual image memory can be as big as 64,000 by 64,000 pixels, with each pixel being as much as 96 bits deep. A big virtual memory is important because it takes a lot of pixels to represent a real-world object. □

HOW FONTAINE AND PFEIFFER GOT STARTED

Once, it was the ambition of two wide-eyed engineering students at Marquette University in Milwaukee. Eight years later, the startup of Visual Information Technologies Inc. is a dream realized for James A. Fontaine and David M. Pfeiffer, both now 29 years old.

Today, the two men and about 20 other VIT employees in Plano, Texas, are aiming to become a dominant force in the image processing arena. Fontaine and Pfeiffer, both former engineers at nearby Mostek Corp., are making the bid with custom chips and new algorithms targeted at a $5,000 image computer system capable of performing 500 million operations per second.

To help VIT realize this goal, the two cofounders last year raised over $3 million in venture capital and recruited a number of key technical leaders including company president Gerald D. Rogers, 43, who while at Texas Instruments Inc. rose from technician to semiconductor vice president.

Pfeiffer and Fontaine both graduated from Marquette with BSEE degrees in December 1980. Fontaine started to work at TI in Dallas as a project engineer designing airborne radar, while Pfeiffer joined Motorola Inc. creating an IBM 3270-compatible graphics terminal. In 1982, Pfeiffer went to work at Mylstar Electronics Inc. in Chicago developing new video game systems. A couple of years later, the two engineers joined up again, working on a Mostek graphics chip project in Carrollton, Texas. By then, the two had conceived a new image-processing system aimed initially at graphic arts and publishing.

During most of their evenings and weekends, the pair developed the concepts and began peddling a personal computer-based prototype, dubbed the waffle machine. "You make the first one and expect to throw it out before getting it [the prototype] just right," quips Fontaine.

Once the basic concepts were set, the firm began implementing the architecture in custom and semicustom integrated circuits. The 350,000-transistor parallel image processor was designed by hand in five months last year. The firm still believes no computer-aided system today can beat the skills of a good silicon designer.

Rogers says the development strategy was to keep spending down while tapping the available resources in the Dallas area. "We don't have all of the capital in place for a one-shot or two-shot deal," explains Rogers, referring to the one-time use of special design systems. "If you look at the design cycle, there is a period when you need a Vax 8600 minicomputer. That's probably two or three months long. Then there is a period you need a Calma layout system. That's another two or three months." The trick, Rogers adds, was understanding each step and having the in-house skills to deal with these contracted services.

AMBITIOUS. Pfeiffer (left), Fontaine, and Rogers (right) aim to bring high-end image processing to the desktop.

HOW LONG WILL IT TAKE IMAGE PROCESSING TO BLAST OFF?

It could be quick, once standards are set and VLSI chips drive down system costs

by J. Robert Lineback

There's a bright new world waiting out there for image processing. Equipment vendors and observers familiar with the field think that image processing is poised for explosive growth. But first a set of standards must be hammered out to span the many segmented markets. Also, manufacturers must continue to drive down the cost of these systems, which deal with image data imported to the processor from a camera or scanner rather than with images generated internally as do graphics systems.

Viable standards hold out the promise of much cheaper hardware through economies of scale in manufacture and highly integrated implementations. But it is by no means clear just when standards will gel sufficiently to allow a major takeoff for image processing. At least one networking scheme is being promoted for image processing, but most participants in the field admit no organized effort is yet underway to set standards for compatible software, image data bases, pixel formats, and digital-video compression. There is perceivable movement, however, toward a group of *de facto* hardware standards taking form now around engineering work stations and machines compatible with IBM's Personal Computer AT.

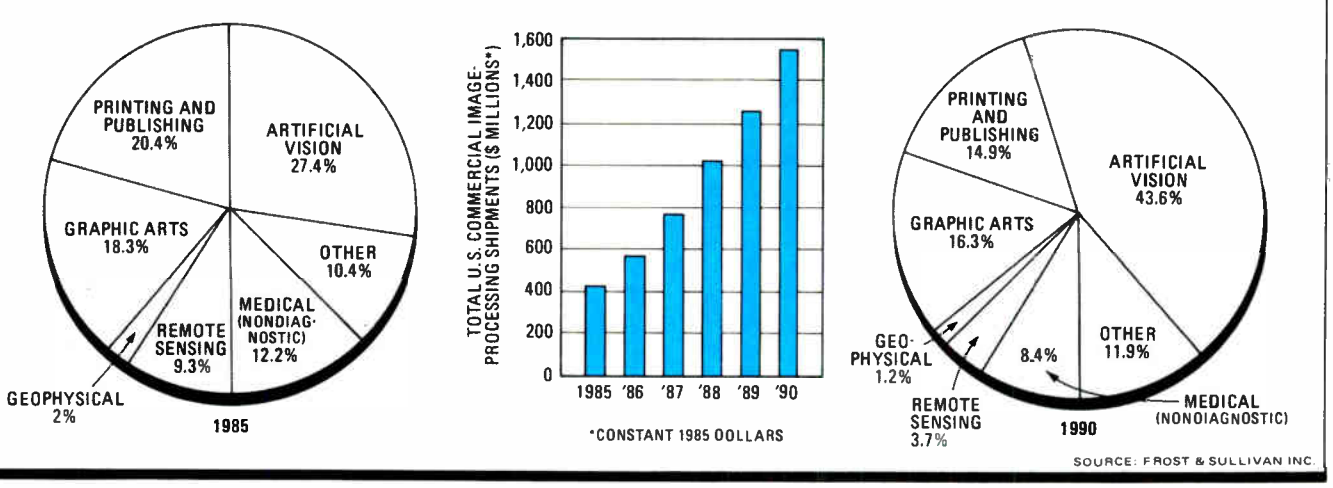
Image-processing vendors envision a tremendous range of potentially lucrative applications opening to low-cost systems. Estimates of the market size a few years out vary, due in large part to the uncertainty caused by the lack of standards. But many analysts think the market could mushroom.

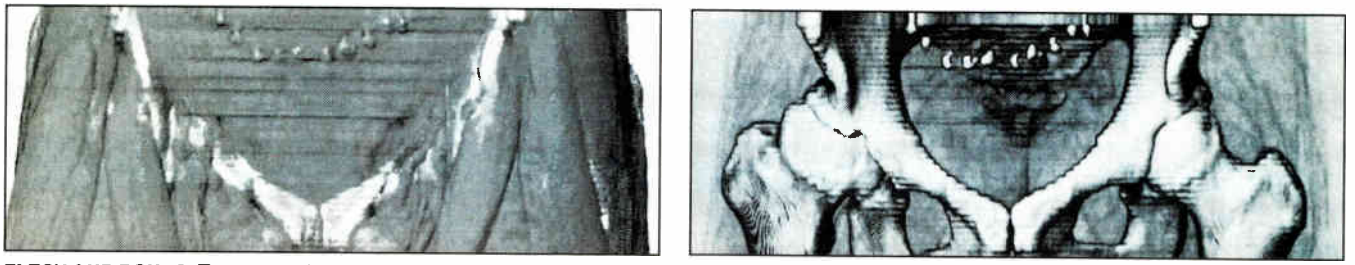
To make image processing live up to its potential, vendors are working to drive its cost down. The latest to make a bid is Visual Information Technologies Inc. of Plano, Texas, which is designing custom and semicustom integrated circuits for its VITec Image Computer system. The goal is to use ICs to drop the cost of a powerful image processor to about $5,000 (see p. 62). High-end image processors today can cost over $100,000.

Driving prices down would be easier if there were standards the industry could rally around. The only firm standard the image-processing industry has had to work with is the aging RS-170 image format for analog television. Starting in the early 1970s, image processing was centered around the TV standard. But since then vendors working different market segments have headed in many directions, with different formats and architectures arising to meet specialized needs.

Moreover, some vendors say the RS-170 standard is outmoded for high-performance image processing. "We are likely to see problems resulting from the TV standard down the road," says Steve Meaders, image-processing product manager at Recognition Concepts Inc. in Incline Village, Nev. For example, image-format requirements stemming from solid-state image

ARTIFICIAL VISION TO PLAY MAJOR ROLE IN GROWTH OF U.S. IMAGE-PROCESSING MARKET





FLESH AND BONES. Tomographic-scanner data can be processed by Pixar's image system to show different physical structures inside the body.

sensors are already derailing RS-170.

Recognition Concepts, which sells a 32-bit imaging processing system, is promoting a new network called VisiNet as a possible standard for transporting image data. The RS-422-based VisiNet runs at 20 megabytes/s and 10 MHz, compared to the 7.5-MHz signal of RS-170.

Another standards push comes from Datacube Inc., which is promoting its fast video bus, called MaxBus, as a method for offloading image data from the VMEbus. Datacube is charging a nominal licensing fee of $1 in order to maintain control over the MaxBus spec, which is finding its way into general-purpose array-processing systems, says Shep Siegel, senior engineer at the Peabody, Mass., company.

Several image-processing vendors hope to follow the lead of emerging computer-graphics standards, such as the Programmer's Hierarchical Interactive Graphics System (Phigs) or the Graphics Kernel Standard (GKS). Others are quick to caution that standards are not settled in the graphics arena either, and some doubt that graphics standards will prove applicable to image processing anyway.

Once key standards take shape, the market for low-cost image processing will go out of sight, say pioneers in the business. Highly pipelined image-processing subsystems will turn up in a wide range of applications, enhancing, altering, and even creating new images from a stored original.

Existing markets include scientific research, medical diagnostics, weapon guidance, satellite surveillance and mapping, machine vision, digital video, computer-aided graphic arts, solid-state photography, and electronic publishing. Image-processing visionaries also see totally new markets. Among them: retail-store color terminals that accurately display clothing hung on an image snapped of the customer, and interior design and landscaping systems that enable designers and architects to work directly on digital snapshots of existing rooms, buildings, or lots.

Lower prices would make possible such applications as color terminals for retail stores that accurately display clothing hung on an image of the customer

Frost & Sullivan Inc., a New York market-analysis company, expects the combined annual sales of image processing systems to grow at an annual rate of more than 30% during the end of the 1980s (see chart, p. 65). The company says total U.S. sales alone will grow to $1.58 billion in 1990 compared to only $414.8 million two years ago.

Frost & Sullivan bases its projection on sizable growth in the U.S. artificial-vision markets. Others disagree with this projection, however. Many participants and some analysts say artificial vision experienced major setbacks in 1986 with large corporations, such as General Motors, retrenching in factory automation efforts. For that reason, many new startups plan to avoid the vision markets during the next couple of years.

In the meantime, they'll be concentrating on cost cutting to help stimulate the growth of image processing. "Everyone knows you have to bring the price down, and everyone is heading for $15,000 and below while trying to maintain high performance," says Alvy Ray Smith, vice president and cofounder of Pixar. The San Rafael, Calif., firm last month cut the price of its Pixar Image Computer from $122,000 to $79,000 after recovering initial startup costs and improving manufacturing efficiencies.

Five-year-old Vicom Systems Inc. has also launched a major cost-cutting program. It aims to reduce the price of its image-processing products about 25% by using new custom processor chips and volume manufacturing techniques, says Albert Winegar, president of the San Jose, Calif., company. Products using the new custom chips will enter volume production in the spring.

Other image-processing houses are turning to silicon integration to reduce the size and price of systems. Data Translation Inc. in Marlborough, Mass., a manufacturer of data-acquisition products that has turned its attention to this market, is using four semicustom CMOS gate arrays on its $2,995 DT2851 frame-grabber board, which fits into the expansion slot of an AT-compatible personal computer.

Imaging Technology Inc., Woburn, Mass., is using about 15 gate arrays on one board of its new Series 200 system, which can be embedded inside Digital Equipment Corp.'s MicroVax II [*Electronics*, Feb. 5, 1987, p. 95]. A MicroVax II-based image-processing system sells for about $50,000, which is only about half the cost of comparable high-end systems, according to the company. □

TOOLS BRING PC-BOARD DESIGN BACK TO THE FUTURE

A wide range of new products is helping pc-board designers to simulate today's complex designs and handle surface-mounted devices, high-pin-count VLSIs, and ASICs

by Jonah McLeod

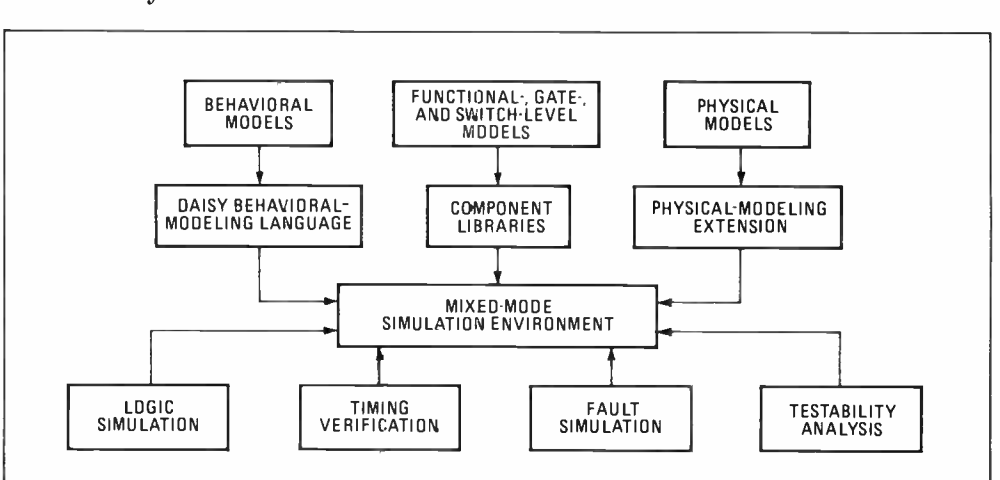
A rising tide of highly complex integrated circuits in new types of packages is threatening to swamp the computer-aided-design systems of most printed-circuit-board designers, because most of their design equipment was built to handle a far simpler generation of boards, not today's. But just in time, a wide range of new tools are coming on stream to help turn yesterday's design systems into tomorrow's.

As it is, few of the current systems have the front-end CAE tools to simulate complex board designs using today's highly integrated chips. "Only about 10% to 15% of all printed-circuit-board designs are simulated," says Kelly Rupp, director of product marketing for Tektronix Inc.'s CAE Systems Division in Austin, Texas. Nor can designers lay out boards carrying surface-mounted devices, high-pin-count very large-scale integrated circuits, and application-specific ICs, not to mention chips built for the Pentagon's Very High Speed Integrated Circuits program.

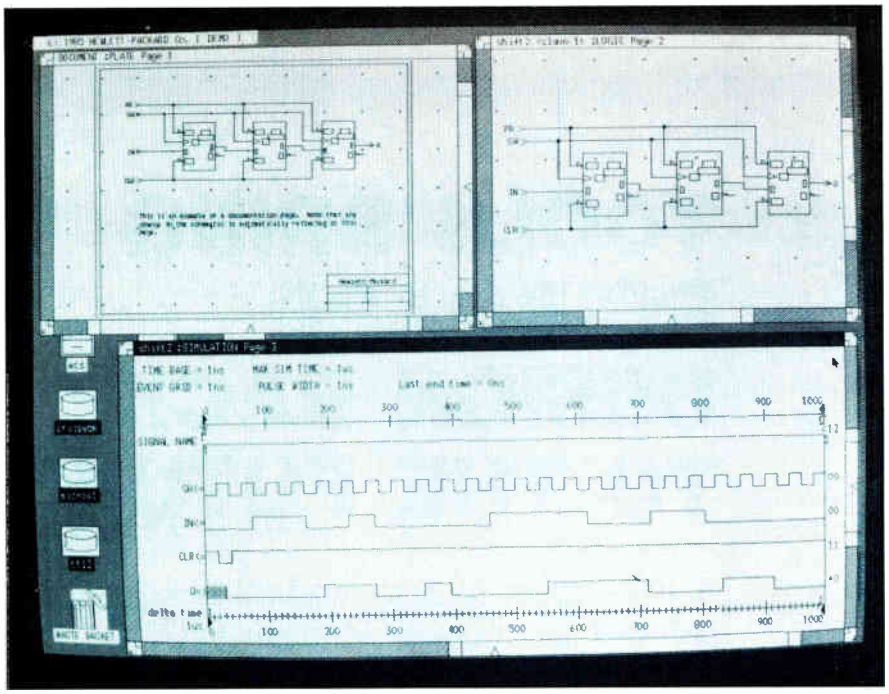
In practice, very little board-level circuit simulation occurs before a pc-board design is prototyped. At the front end of the design process, the circuit designer enters his schematic to the CAE system and thereafter builds a prototype board so he can debug the design.

The tools now arriving on the market provide a wide range of new simulation capabilities. Models of the latest VLSI and VHSIC chips are appearing, along with hardware modelers that allow the actual chips to be used in the simulation. Schematic-entry tools and accelerators speed the conversion of a schematic into data that can be simulated. Faster simulation accelerators can then run simulations in minutes, rather than hours or days. New front-end tools—especially timing simulators—help integrate the front-end circuit-design and back-end board-layout processes.

New interactive tools allow placement of surface-mounted parts—which are rapidly replacing conventionally packaged components—on both sides of a circuit board. Gridless routers route traces to the non-standard packages of surface-mounted devices. To route high-pin-count ASIC, VLSI, and VHSIC chips, a number of routers—including rip-up-and-



1. MODELING. Models operating at several levels—behavioral, functional, gate, switch, and physical—feed the mixed-mode circuit-board simulation environment in the Daisy System Boardmaster.



2. SIMULATION. HP's Electronic Design System simulates the output of three-stage registers—the bottom line of the timing trace—given three inputs.

reroute tools that achieve 100% routing of boards and a program that routes multiple layers concurrently—have been announced.

The latest crop of simulation models (see fig. 1) can fill one of the most pressing needs of designers. "The designer typically wants to use state-of-the-art chips in his board designs, but often the chips are so new that models for them do not exist," says Michael Turner, marketing manager at Logic Automation Inc. in Beaverton, Ore. The designer can write his own model, using the hardware description languages provided with most simulators, but for complex chips this is a very big job in itself. An alternative is to use the actual part in a physical modeler.

ON-TIME MODEL DELIVERY

To provide models of the newest chips, model vendors Logic Automation and Quadtree Software Corp., Bridgewater, N. J., both have agreements with IC manufacturers to produce models of their latest chips before they are commercially available. Quadtree has agreements with Texas Instruments for the 74AS8800 series of bit-slice microprocessors and with Weitek for its floating-point chips. Logic Automation has agreements with Advanced Micro Devices on its 29300 chips, Analog Devices for its digital signal processors, and Fairchild Semiconductor for its Clipper chip set.

Even with more models becoming available, a designer typically cannot find all he needs. In that case, he can use the actual chips as models. Valid Logic Systems Inc. of San Jose, Calif., pioneered this concept with their RealChip hardware modeling system. Now every major vendor of CAE systems offers a version of this product.

But hardware models present their own problems. "Using a physical modeler requires the designer to wire the pins for the chip he wants to model on the modeler hardware unit," says Turner of Logic Automation. One solution is the DataSource Hardware Modeling System from Teradyne Inc. of Boston, which reduces the chore to wiring only power, ground, and clock for most standard chips—but pin-grid arrays still have to be wired completely.

And wiring the modeler is not the only setup task the designer faces. "He must then write a timing shell, which directs the modeler to vary the operating characteristics of the part over its operation range, as specified by its data sheet," Turner says. The timing shell contains information about the component's functional timing variables—setup, hold, and delay times, and values that enable the simulator to simulate worst-case timing. Teradyne provides fully programmed behavioral shells for popular 16- and 32-bit microprocessors and peripheral support chips.

Modelers allow the designer to use more than one chip at a time, and they can be configured to accommodate multiple device types, including standard parts and gate arrays, and different technologies: TTL, CMOS, and emitter-coupled logic. Cadnetix Corp. in Boulder, Colo., has a modeler that can handle up to 30 chips at a time. If a chip occurs more than once in a given design, the designer uses one model—hardware or software type—and tells the simulator to access the same model for different parts of the circuit.

With the various tools available, designers should not have too much difficulty modeling their boards. But the time and effort necessary to set up and run a simulation still limits them. Designers must convert the schematic from a graphical representation to a netlist containing instances of the models of components used in the design. Hours of setup time are followed by hours of running the simulation, and each time an error is detected the entire process must be repeated.

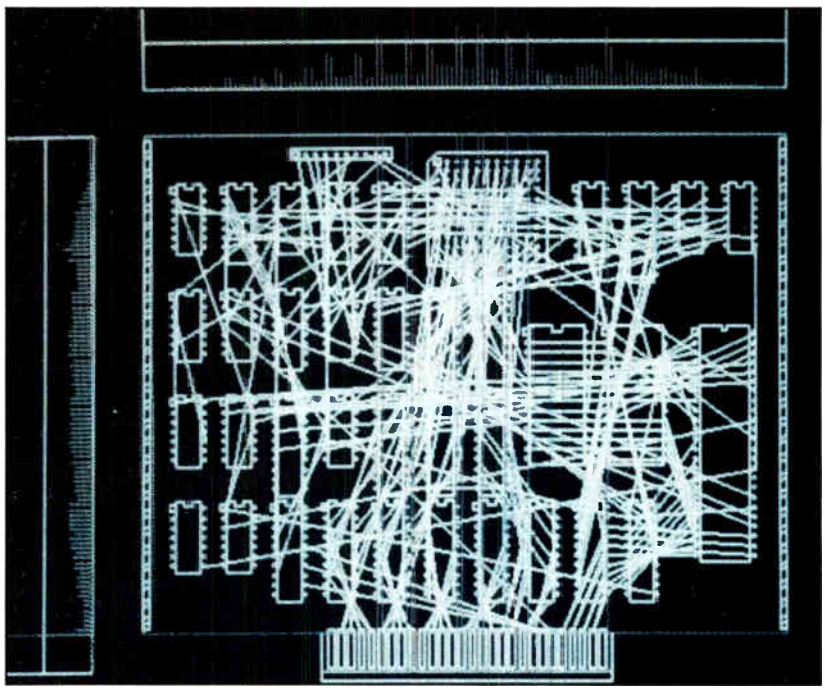
One way to solve the entry problem is with interactive design systems, such as the Electronic Design System from Hewlett Packard Co.'s Logic Design Operations in Ft. Collins, Colo. "As the designer enters his schematic, the system builds the design data base," says David Hardman, product manager at HP. When the designer finishes entering his design, he is ready to simulate (see fig. 2).

Running the simulation itself is the next ob-

stacle. A designer ought to be able to run a simulation until some design error makes it fail, correct the error, and then quickly move on to run another iteration of the process. "A designer using conventional simulators running on a mainframe can get only one to two simulation iterations a day," says R. James Dickie, vice president of marketing and product management at Aida Corp. in Santa Clara, Calif. "Using a work station, he gets one every three days."

Simulation accelerators also help increase the number of iterations a designer can perform each day. Aida offers a product called the CoSimulator Accelerator that can handle designs with complexities of 250,000 to 1 million gates at a speed of 5 million evaluations per second. That means a designer can run 20 to 30 iterations per day. Cadnetix and Mentor Graphics Corp. both offer 12.5-million-instruction/s accelerators.

The iterative process in the front end extends into pc-board layout in the back end, where the layout designer creates a breadboard of the design. Once laid out, the design data is returned to the circuit designer for timing simulation. "Timing analysis is not done well on a breadboard," says Gregory Skomp, manager of strategic planning at Cadnetix. To get around the problems with breadboards, many designs are simulated using a public-domain timing analyzer developed by Valid Logic Systems Inc.'s founder, L. Curtis Widdoes, while he was at Lawrence Livermore Laboratories in Livermore, Calif.



3. ANALYSIS. Histograms on the Tektronix PCB WorkSystem show dense wiring, allowing a designer to relocate parts for better routing.

LINKING FRONT END TO BACK

Often, the front-end CAE and back-end CAD are performed by two different engineers, but this is changing. "Circuit designers will do the layout because of the increasing complexity and higher speed of future-generation boards," says Alberto Jimenez, vice president and general manager of Mentor Graphics Corp.'s Automated Layout Division in San Jose, Calif. "On board designs, the data moving between the designer and layout engineer will be more than circuit components and a netlist. Heat profiles of the board, the length of wires that could affect timing in high-speed circuits, placement of high-speed components relative to one another—these are just some of the additional data that will have to become part of the data base."

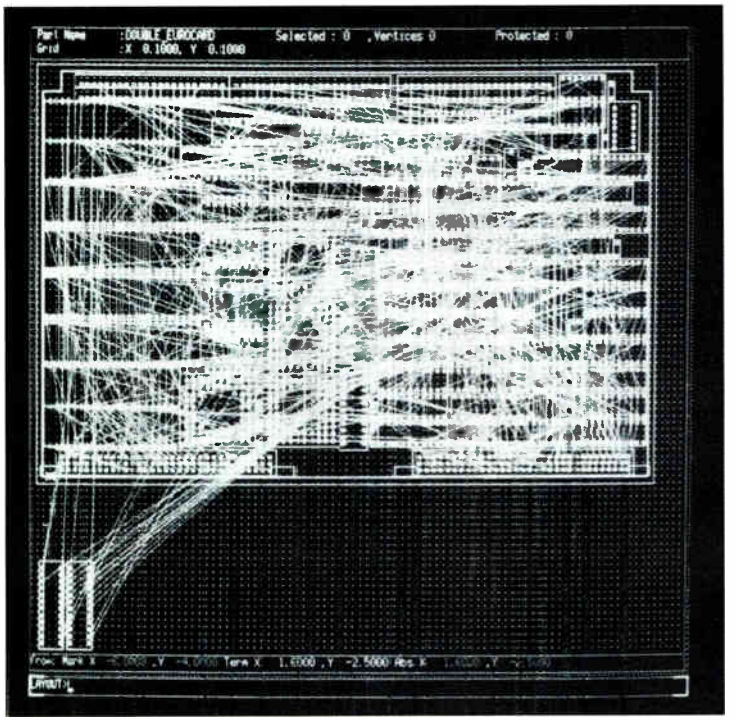
Arne Antos, marketing product line manager at FutureNet, Chatsworth, Calif., agrees: "The centralized data base for both CAE and CAD is the holy grail for pc-board design systems." One level might contain a component's schematic symbol for screen display. Another might contain its package dimensions for layout; another its electrical characteristics for simulation. Each application—simulation, component placement, routing, and so on—only looks at the level relevant to its task. "FutureNet has a data base that contains some layers now, but not to the extent needed for fully integrating CAE and CAD," says Antos.

The solution lies with an object-oriented data base in which graphics circuit symbols are but one type of object, says Hal Barbour, executive manager of electronics marketing at Intergraph Corp., Huntsville, Ala. Other objects could include electrical models, the mechanical characteristics of packages, and so on.

But today, the level of integration between front- and back-end pc-board design is still rudimentary. A layout designer must still place and route components on a pc board from a list of components and a netlist the designer built in the front end of the process.

Increasingly, too, these components will be surface-mounted devices. Robert N. Castellano, author of a study on automated pc-board design published by Electronic Trend Publications of Saratoga, Calif., says, "although they represent less than 20% of all IC packages used today, surface-mounted devices will grow to 30% by 1990." Pushing this growth will be the declining cost of these devices. "1987 will be the year surface-mounted components reach price parity with through-hole components," says Kenneth Butler, Boardmaster product manager at Daisy Systems Corp. of Mountain View, Calif.

The low profile of surface-mounted devices allows them to be mounted on both sides of a pc board. But placing hundreds of components on each side of a circuit board is cumbersome, at



4. MARE'S NEST. Pins on all four sides of pin-grid arrays, shown on the Mentor Graphics Board Station, complicate routing.

best. CAD systems such as the Calay V04 from Calay Systems Inc., Irvine, Calif., can help solve this problem by giving designers a view of the flip side of a board at the flip of a switch.

"To handle surface-mounted devices, the tool needs to be able to place a component on the opposite side of the board so that each is a mirror image of the other and so that they are directly atop one another," says Kevin Kerns, president of Case Technologies Inc., a CAE tool vendor in Menlo Park, Calif. This capability is available on most place-and-route tools, including the Vanguard tools from Case, and is useful, for example, in laying out arrays of memory chips on two sides of a board.

"Surface-mounted devices require routers able to handle components that do not fall on a regular grid," says David Rager, vice president of marketing at Calay Systems. The reason is the lack of uniformity, Butler explains. "Unlike dual in-line packages, which can be uniformly placed on a regular grid, there is little standardization in surface-mounted-device shapes," he says. A new generation of "gridless" routers have emerged for most layout systems to accommodate almost any component spacing.

Gridless routers actually have grids, but the grid spacing is so small—1 mil—it can handle just about any of today's routing requirements. The Tektronix Merlyn-P layout system, for example, allows fine-line routing of up to three lines between pads and a trace width, which can vary from 1 to 127 mils.

Besides surface-mounted devices, pc boards increasingly will use high-pin-count ASIC, VLSI, and VHSIC components housed in pin-grid arrays and other types of packages. "Five years ago, 80% of the components on a printed-circuit board contained no more than 100 equivalent ICs," says Kerns. "Today, 80% of the parts on a board contain much more than 100 equivalent ICs."

High-pin-count chips need especially fine line traces. With the increased use of big ASICs, input/output pins currently on 50- and 100-mil centers will be reduced to 25-mil centers that will require 5-mil lines and spaces on the board.

In addition, unlike surface-mounted devices, these chips call for extra metal layers for interconnection traces. Also, high-pin-count chips make more traces necessary, so they take up most of the time used to lay out a board.

To speed the routing job, there are analysis tools that examine the placement of components on a board. The tool then produces a histogram, which indicates the distribution of routing density in the horizontal and vertical plane (see fig. 3). Reworking congested areas beforehand eases the routing task.

Moreover, with the pin-grid-array packaging, routers will be required to route in both the horizonal and vertical plane (see fig. 4). With DIPs, the router only had to accommodate a single row of pins on two sides of the device. With pin-grid arrays, it must handle multiple rows of pins on all four sides of the package.

REVVING UP ROUTING

To address the problems of routing multilayer circuit boards, CAD companies all offer routing accelerators equipped with algorithms that can handle different kinds of routing requirements. The four most common router types used today are flood, channel, memory, and rip-up-and-reroute types. The first three route 90% to 95% of a board; the fourth routes the remainder.

A flood router, also called a Lee's algorithm or maze router, starts at a source node and "floods" potential routes outward until a connection is made, at which point the process repeats. Channel routers provide fast routing in horizonal and vertical channels on the pc board. A memory router is a channel router that allows close packing of routes and 45° routing in memory arrays.

The rip-up-and-reroute algorithm is what most CAD tool suppliers rely on to reach 100% automatic routing. Usually invoked after other routing algorithms have reached their limits, the rip-up-and-reroute tool removes connections that are preventing other routes from being completed, then reroutes. Calay and Cadnetix use rip-up-and-reroute algorithms in their routers.

Most routing algorithms work with two layers at a time, starting with outside layers and working in. But Cadnetix, for one, has a multilayer routing algorithm, which runs on its CDX75000 routing accelerator. "Our router routes up to eight layers at a time," says Skomp. □

MOTOROLA GRABS LEAD IN ECL DENSITY, USING MOSAIC III

The 10,000-gate array was fabricated with submicron emitter widths, but without submicron lithography; designers can choose from a broad range of speed/power tradeoffs

By Bernard C. Cole

Chip density keeps steadily moving higher in most product families, and nowhere has the job been more difficult than in bipolar emitter-coupled logic. Now Motorola Inc. has grabbed the density lead, at least for now, with its new 10,000-equivalent-gate array.

The chip maker was able to get four times the number of gates in the MCA10000ECL chip as it has in its current state-of-the-art bipolar array. And it accomplished that with only 40% more chip area. The new array is quite a performer: gate delays are as low as 150 ps, while gate power dissipation is as low as 1 mW.

It took Motorola's state-of-the-art Mosaic III process to get this density and performance. The 1.5-μm bipolar technology builds on the company's earlier Mosaic I and II technologies, but adds such new enhancements as a polyelectrode transistor that's crucial to the new array's high speed. The third-generation process can produce structures with submicron emitter widths, using essentially the same 1.5-to-2-μm lithography as the Mosaic II process. The MCA10000 will be fabricated by Motorola's application-specific integrated circuits division in Chandler, Ariz.

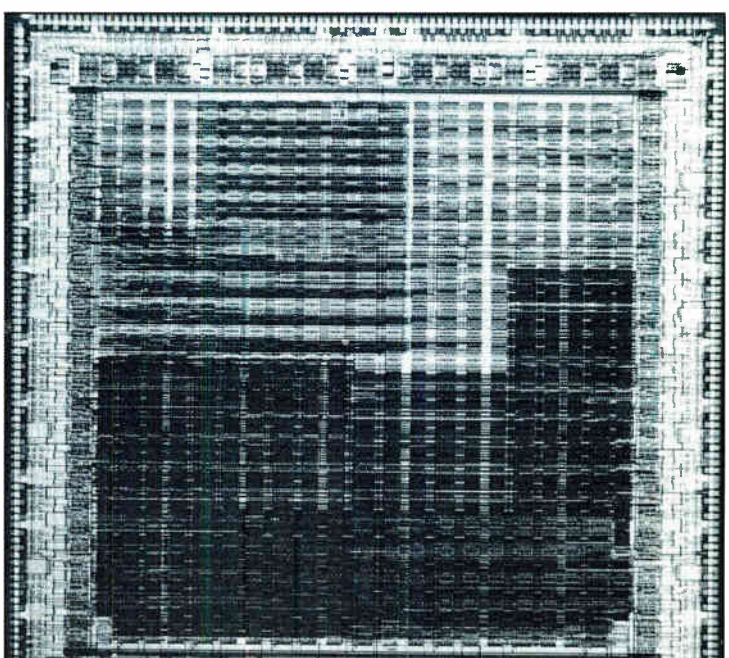
The MCA10000 (see fig. 1) features three levels of interconnection and three-level series-gated ECL structures to achieve an unprecedented level of functional density. It also offers a wider range of power and speed tradeoffs than any other currently available gate array.

In addition, the company is working on a 1-μm enhancement of the Mosaic process with four levels of interconnection. Mosaic IV is expected to yield bipolar ECL arrays with up to 20,000 gates and gate delays of only 50 ps per gate.

In the Mosaic I process, used in the fabrication of Motorola's 1,200-gate MCA1200ECL gate-array family, the company relied on a nonwalled emitter and a walled base. Oxide isolation between devices was achieved with an isotropic etch, and a nitride surface covered the oxide so that the metal system was over the nitride.

The Mosaic II process introduced the use of walled emitter structures to achieve gate delays of about 400 ps, says Patrick Hickman, design engineering manager for gate arrays. "Use of the walled emitter greatly reduced the device area and the parasitic capacitances that normally impact gate delays adversely," he says.

The Mosaic III process (see fig. 2) advances further by using a polyelectrode transistor structure, which uses p^+ polysilicon for extrinsic-based doping and the base electrode, and n^+ polysilicon for the emitter. The extrinsic polysilicon base electrode greatly enhances switching speed

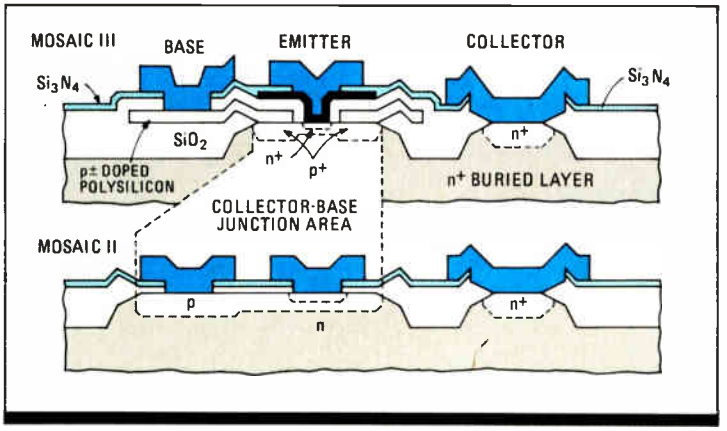


1. TRIM AND QUICK. Motorola's new 10,000-gate ECL array, prior to final metal and passivation. Built with the Mosaic III process, the chip is only 385 mils square.

by reducing the series base resistance and collector base capacitance, says Hickman.

With Mosaic III, the maximum toggle rate per gate is 1.2 GHz, about twice the rate of Mosaic II. At 3 mA of drive current per gate, the worst-case gate delay is 120 ps, versus 200 ps for Mosaic II and 250 ps for Mosaic I. At 0.7 mA, comparable gate delays are 150, 250, and 420 ps, respectively. "When we specified the process we were very conservative," says Hickman. "In practice, performance is much better. In a 23-stage ring oscillator fabricated with the new process, we measured gate delays of about 70 ps at 800 μA."

Although the new array is four times the density of the earlier MCA2500ECL, the chip size of the 10,000-gate device is only 148,000 mil²—less than 50% larger. Key to the higher density is the use of emitter widths that are less than 1 μm, but fabricated using the same 1.5-μm to 2-μm design rules of Mosaic II. This was achieved through the use of a proprietary edge-defined



2. THE KEY. Mosaic III's polyelectrode transistor speeds switching by reducing base resistance and collector-base capacitance.

technique that allows fabrication of submicron emitter widths without the use of submicron lithography, Hickman says.

Another improvement is the use of polysilicon resistors to reduce node resistance. The process also provides for the deposition of gold bumps (see fig. 3), which serve as an interface for tape-automated bonding. Three layers of metalization are used: two for interconnect wiring and one for power-bus distribution.

The array consists of 838 cells of three types: 414 internal cells, 224 input cells, and 200 output cells. The majority of the logic is implemented using the internal cells. Major cells are subdivided into quarter-cells, which allow up to four different logic circuits to be placed within one major cell location to achieve maximum array utilization. All inputs go through the input cells, which serve as input buffers as well as performing useful logic functions, such as a two-input OR/NOR. Any signal leaving the array must go through an output driver macrocell, which is even more flexible than the input interface cells, being capable of performing a variety of logic functions, such as a four-input OR/NOR, a D flip-flop with reset, or a dual D latch with reset.

The three layers of metal interconnect are used for routing and power distribution. As in previous generations of macrocell arrays, each cell location is made up of uncommitted transistors and resistors that are automatically interconnected via first-layer metal to implement a specified logic function. Power distribution is contained almost entirely on the third layer of metal and is common to all array designs. Both cell intraconnection and routing of power signals are transparent to the user. The interconnection among the macrocell functions and the I/O pins is accomplished with a grid of horizontal and vertical routing channels. Vertical channels are positioned between and outside the columns of cell locations, in the first layer of metal. Horizontal channels use the second layer of metal for routing across macrocells and vertical channels. Thus placement of a macro on the array never obstructs routing channels.

To further increase functional complexity, Mosaic III bipolar gate arrays allow the implementation of up to three levels of series-gated ECL structures. In series gating, or cascoding, one current source is used to drive two or more sets of transistors configured so that the collectors of one set are connected to the emitters of the next higher set.

Three-level series gating allows complex macro functions to be implemented with fewer gates while maintaining maximum performance, says Hickman. Various complex macro functions are all built using only the first layer of metal within a cell, thus eliminating the need for the numerous interconnections that usually have to be made in the channels of a gate array, and significantly reducing routing-channel requirements.

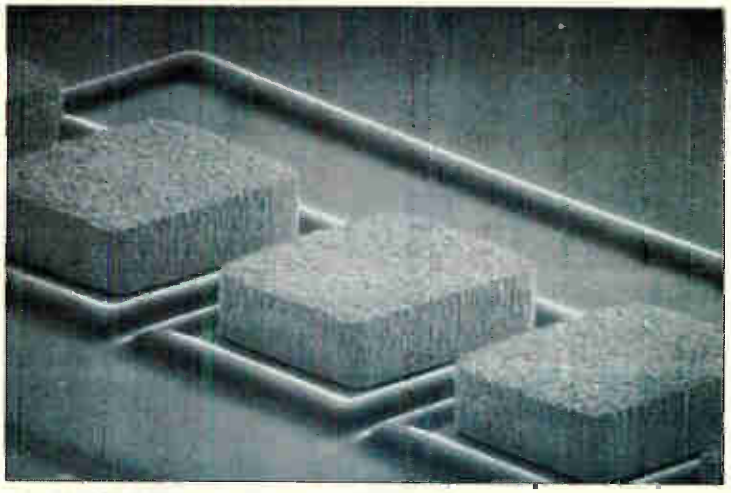
The MCA10000 has been designed so that the circuit engineer can select from a wide range of speed/power alternatives to suit a particular customer's requirements. The array is available with three types of supply voltage: a 5.2-V 10-K voltage-compensated version; a 5.2-V 100-K temperature-compensated version; and a 4.5-V 10-KH ECL version. With each of these, cells can be chosen with either of two speed/power ranges by selection of either a high- or low-value resistor implant. Also, the emitter-follower and current-source structures can be individually modified to one of two additional speed/power levels.

To facilitate multichip designs, as well as to offer additional speed/power programmability, the MCA10000 features a flexible I/O structure. In addition to the 200 output cells and 224 input interface cells, the array also contains 256 I/O ports, which can be used as either inputs or outputs. As ECL outputs, the ports are capable of driving 25, 50, or 60 Ω. "Also, the ECL outputs have been designed with programmable current-source pulldowns and selectable on-chip series-terminated resistors," says Hickman.

Depending on whether it is designed using low-power or high-power programming options, a typical four-input OR/NOR gate is capable of gate delays ranging from 250 to 400 ps. For a D flip-flop, the speed ranges from 200 to 700 ps; for an output OR gate, it ranges from 250 to 500 ps. For an input OR gate, typical delays range from 170 to 290 ps.

Depending on the speed/power range chosen, the MCA10000 has a total power dissipation ranging from 10 to 30 W. While the low-power (10 to 15 W) version requires a heat sink and ordinary air-flow cooling, the high-power, 15-to-30-W versions require the use of nonconventional techniques, such as impinged chilled air with special heat sinks or liquid cooling, to meet the maximum junction temperature limit of 115° C for ac specifications.

Hickman says that Motorola is planning a number of other low-power-dissipation additions to the family during the year, including the 7,000-gate MCA7000ECL, which has about the same toggle frequencies and gate delays, but a power dissipation range from 10 to 15 W—ideal for ordinary air-flow cooling. Also in the works is the MCA7500RAM, a 7,500-gate array with 4-K of on-chip RAM having a typical access time ranging from 1.2 to 1.5 ns. Another part in the works, the MCA1500ECL, will aim at telecommunications applications. The 1,500-gate, 120-ps-per-gate array will have a power dissipation ranging from 3 to 6 W.



3. BONDING BUMPS. This 680× magnification shows gold bonding pads on the die periphery, for use in tape-automated bonding.

And beyond that is the 1-μm successor to Mosaic III, with four layers of metal interconnect, which will be used to fabricate bipolar ECL arrays with densities as high as 20,000 gates. Planned for introduction during late 1988 or early 1989, these arrays will have gate delays of about 50 ps and typical access times for on-board RAM of 1 ns or less. □

MOTOROLA'S NEW ARRAY: DESIGNED TO FIT USERS' NEEDS

Go to the user and find out what he wants, advises Patrick Hickman, design engineering manager for gate arrays at Motorola's application-specific integrated circuits division. That's how the Chandler, Ariz., division determined the parameters of its new generation of 10,000-gate bipolar emitter-coupled-logic arrays.

Starting almost two years ago, Hickman says, he and Roger Hollstein, section manager for ECL arrays, began talking with a wide range of users of bipolar gate arrays and determined there were two main segments: those such as minicomputer, mainframe, and supermini designers, who have a need for higher density and lower power, but not at the sacrifice of higher speed—and those such as telecommunications designers, who place more of a premium on speed and power, and who don't need the density.

Talking to potential users of the new 10,000-gate array, Hickman found that their needs had become more complex. "For one thing, while there still remain a substantial number of systems using liquid cooling to get every bit of performance they can out of a circuit, there is a growing interest in air-cooled systems," he says. "Second, there is a move toward more-compact systems."

Over and above these needs, he says, many potential customers want to retain the cost advantages and fast turnaround of gate arrays, but at the same time get devices aimed more specifically at the needs of their system's speed and power requirements. "Rather than designing around the specifications of a new generation of gate arrays, what they want is a gate-array family that is designed with their particular requirements in mind," says Hickman.

MOSAIC III TEAM. Hollstein, Hickman, and Zdebel (l. to r.) built what users asked for.

Hollstein, a 23-year veteran at Motorola who has been involved in ECL and bipolar gate arrays for most of that time, began work with his design team on the definition of the MCA10000ECL, the main feature of which is a high degree of speed/power programmability. "I think this aspect of the design makes it unique in the industry," says Hickman. "I don't think any other offering, regardless of size, offers as many variations in the way speed and power can be traded off against one another, at the array, cell, and gate levels."

When the features of the 10,000-gate array had been determined, it fell to Peter Zdebel, section manager for bipolar process development, to modify the newly developed Mosaic III bipolar process to the requirements of the circuit. A graduate of the University of Aachen, West Germany, with a doctorate in semiconductor physics, Zdebel joined Motorola in 1984 and was previously responsible for developing the numerical-simulation models necessary to accurately predict device performance for Mosaic III.

UPDATE: COMPAQ FINDS SMALL IS STILL BEAUTIFUL


HOW COMPAQ REDESIGNED ITS TOP-SELLING PORTABLE

FULL-FEATURED MODEL IS 39% SMALLER AND 15% LIGHTER THAN ORIGINAL

Making a good thing even better has profited plenty of companies, but no one has made it pay off any better than Compaq Computer Corp. A year ago, the Houston maker of IBM Personal Computer compatibles upgraded its portable computer, introducing the smaller, lighter, and faster Compaq Portable II [*Electronics*, Feb. 24, 1986, p. 64]. While the new machine was just as successful as the company's first Portable—both are still selling well—another generation, the Portable III, is due out this week.

Like its predecessor, the Portable III has been designed to provide all the features of the *de facto* standard, the IBM PC, sacrificing no feature for the sake of reductions in size and weight. At the same time, the company is incorporating new technology, so it can develop ever-smaller and lighter machines with faster processors and extra features that go beyond the standard. The Portable II was equipped with the 8-MHz Intel 80286 microprocessor; the original Portable uses the 8088.

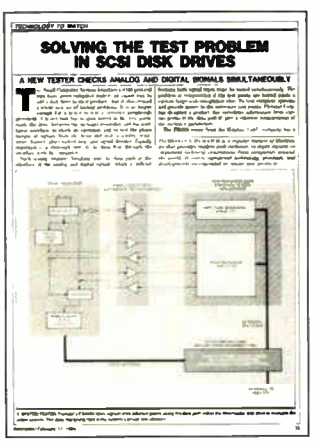
The newest Portable will come equipped with a faster, 12-MHz 80286 processsor and a new, bright flat-panel gas plasma display. It also has a 1.2-megabyte 5.25-in. floppy-disk drive and a 40-megabyte fixed disk drive.

However, the company is eliminating built-in expansion slots, in favor of a plug-on expansion unit with two slots, to make the machine smaller. The choice fits with what Compaq sees as the key to the success of the Portable II. "The most important feature from the standpoint of user-value is its size. It is the simple attribute of a feature-rich 286 computer that can go anywhere—under any airline seat—that makes this an attractive product," says the company's engineering vice president, Jim Harris.

The Portable III weighs in at about 20 pounds, compared with the Portable II's weight of about 27 pounds. Overall, the new machine comes in a smaller package than the Portable II. Its dimensions are: height, 9.8 in., width, 17.7 in., and depth 7.8 in. The comparable dimensions for Portable II are 7.5 in. by 17.7 in. by 13.9 in.

Compaq is aiming both the Portable II and the Portable III at serious business users—those who require high-performance machines that can run a library of standard PC applications, but who also need a small, lightweight portable machine. Along with the original Compaq Portable Computer, which is still in the company's stable of products, the Portable II and Portable III give users a choice of full-function portable machines that cover a price range from $2,000 to about $5,500. *–Tom Manuel*

UPDATE: FLEXSTAR'S SCSI TESTER GETS HIGH MARKS


SOLVING THE TEST PROBLEM IN SCSI DISK DRIVES

A NEW TESTER CHECKS ANALOG AND DIGITAL SIGNALS SIMULTANEOUSLY

In the year since Flexstar Corp. introduced its FS6000, a system for testing disk drives that use the Small Computer System Interface protocol, the company has seen the product flourish. A second version was introduced as planned six months after the initial announcement of the FS6000, and today George Robinson, president of the Milpitas, Calif., company says, "Both products have done as well or better than we expected, and both have changed due to the positive customer response."

The original product is the FS6000 SCSI Bus Analyzer [*Electronics*, Feb. 17, 1986, p. 35]. Used by engineers to evaluate the intelligent SCSI interface, it probes into the drive to test the phase margin of signals from the head/disk interface, read/write channel, phase-lock loop, and data decoder. The tester provides complete analog testing, including missing-pulse detection, extra-pulse detection for media defect mapping, and analog measurements such as 1F/2F amplitudes and resolution. The second product, the FS2500 Multiport Test System, is the production-test version of the FS6000, able to test 1,000 drives at a time.

Both products have been refined since their introduction, as Flexstar's customers, a mix of value-added resellers and disk-drive and storage-controller manufacturers, let the company know in more detail what they wanted from the system. In the case of the FS6000, it became clear that the customers had varying requirements, which dictated that different capabilities be incorporated in the system. "Some wanted to test the full SCSI specification, while others only wanted the SASI subset of the full specification," Robinson says. Shugart Corp., late of Santa

Clara, Calif., originally defined an intelligent interface called the Shugart Associates System Interface, or SASI, which later was extended to become SCSI.

"The FS2500 Multiport Tester changed because customers wanted more data-collection capability, since data cannot be obtained except through the tester," Robinson says. "They are demanding lower per-port test cost. So we are now concentrating on adding more data collection capability at a lower cost per port."

The demand for more and different features led to some complications in the shipment of products. "We shipped both products on time, but the number of new features requested did delay the standard products we are now shipping," Robinson says. The changes had the greatest impact on software development, which ended up being the system component delayed the most. "We shipped the hardware with the original software and then shipped diskettes with the new features," Robinson says.

The changes, however, reflect greater demand for the systems, not disappointment with them. If success can be measured in repeat business, Flexstar is enjoying success. "Our first customers are coming back with reorders for multiple systems, now that they've learned how to effectively use the system to test their products," Robinson says.

And that success has put Flexstar into the upper echelon of the disk-drive test market. "Our competitive position has improved, because we are still the only supplier with full SCSI-testing capability," Robinson says. Peripheral Research, a Santa Barbara, Calif., market-research company, puts Flexstar third behind Applied Circuit Technology Inc. of Anaheim, Calif., and Wilson Laboratories Inc. of Orange, Calif., in the U. S. market.

Flexstar's latest coup was to sign with Toyo Corp. of Tokyo an open-ended agreement that took effect in January and extends over the next several years. The deal makes Toyo the exclusive distributor of Flexstar's full line of test equipment in Japan. By its own estimate, Toyo has 50% of the Japanese market for disk-drive test equipment. Besides the obvious advantage to Flexstar in having the dominant company in the Japanese market distributing its equipment, the agreement seems to signify that Flexstar is an ascending star in that market—Toyo used to be the exclusive distributor in Japan for Wilson Laboratories. *–Jonah McLeod*

TECHNOLOGY TO WATCH

UPDATE: EXAR'S MODEM FILTER IS PAYING OFF

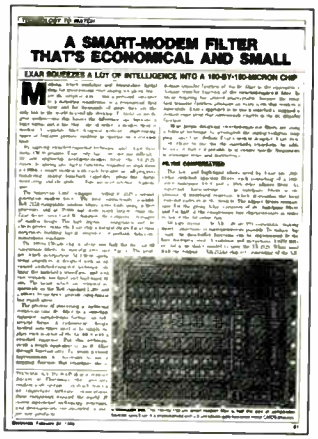
As part of a four-chip modem set aimed at system designers who want higher performance and flexibility than they can get from the low-end single-chip versions that are generally available, the XR-2129 smart-modem filter has exceeded the most optimistic expectations of its manufacturer, Exar Corp. of Sunnyvale, Calif.

Key to the higher performance of the XR-2129 is the use of a proprietary mapping function to ensure closer approximation of specific filter functions. It accomplishes this by translating the s-domain transfer function of an RC filter into the equivalent x-domain transfer function of the switched capacitor filter.

Exar's approach differs from the more commonly used bilinear mapping method, which produces an extra term that renders it inaccurate. The company chose instead to use a matched-z, mapped-z domain equivalent that corresponds exactly to the RC transfer function [*Electronics*, Feb. 24, 1986, p. 61].

Fabricated using a 3-μm silicon-gate CMOS process, the XR-2129 incorporates all the filtering functions required for full-duplex 1,200-bit/s modem operation in either the Bell 212A or CCITT V.22 telephone line environments. At 180 by 150 μm, the filter chip is about half the die size of comparable filters. It is designed to operate as part of a flexible four-chip set—the 212AS—that also includes modulator, demodulator, and buffer circuits.

Exar's approach seems to have paid off: more than one million of the four-chip sets, in a version meeting the Bell 212A line requirements, have been sold in the U. S. market. Now the company is gearing up for production of a version that meets CCITT V.22 line requirements, for sale in Europe.


A SMART-MODEM FILTER THAT'S ECONOMICAL AND SMALL

The XR-2129 has also been joined by three additional filters. The XR-2126 and XR-2127 are aimed at replacing specific competing devices: they are are pin- and function-compatible with the AMI S35212 and S35212A made by what is now Gould Semiconductor, formerly American Microsystems Inc. The third new filter, the XR-2128, is an enhanced version of the XR-2129 containing two additional control pins that allow more accurate call-progress monitoring and easier V.22 implementation than the original version.

In development is a new four-chip set aimed at full-duplex 2,400-b/s V.26/V.29 applications, a V.26 half-duplex 2,400-b/s offering, and a single 5-V two-chip set using a proprietary digital-signal-processing architecture. *–Bernard C. Cole*

MILITARY: SYSTEM HELPS PROTECT A-6 JET IN COMBAT

A microprocessor-based system maintains the right amount of a gas needed to prevent explosion in a tank hit by hostile fire, ending a guessing game for pilots

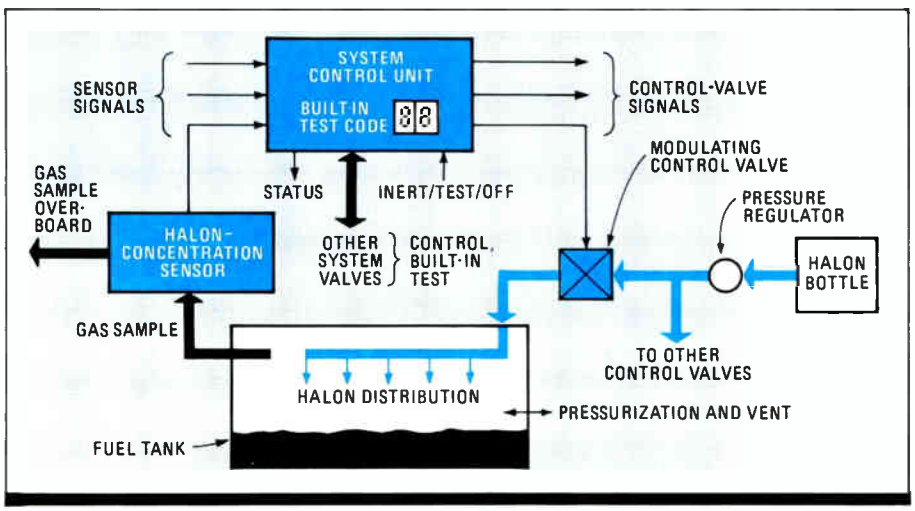
Pilots of U. S. military aircraft will breathe easier during combat now that Gull Inc. has devised a simple, rugged microprocessor-based system that dynamically monitors and controls the ratio of fire-suppressant gas to air in an emptying fuel tank. Special sensors in this closed-loop system are the key to maintaining the gas-to-air ratio, which helps prevent explosions in a fuel tank hit by hostile fire.

The system employs Halon, a fire-suppressant gas in the Freon family that has long been used to extinguish aircraft engine fires. Gull designed a closed-loop system that maintains a 20% Halon-to-air ratio over an entire flight as the air in a tank gradually increases and fuel decreases. Previous open-loop systems in military aircraft would simply empty Halon gas into the fuel tank when the pilot triggered a switch. But in such systems, the Halon-to-air ratio may drop below the critical 20% point as the tank empties.

The explosion-suppression system will be retrofitted to existing A-6 attack bombers and installed in all future A-6s. Gull's staff believes that the unit is a candidate for other military combat aircraft as well. Such a sensing system could also be used in any industrial or chemical process where maintaining an air-to-gas ratio is critical.

The Smithtown, N. Y., company designed the system for Grumman Aerospace Corp. after the Navy demonstrated in a series of experiments that a 20% volumetric ratio of Halon gas to air in the air space of a plane's fuel tanks will suppress an explosion when a 23-mm shell pierces the tank. The government first asked Grumman, of Bethpage, N. Y., a major supplier of military aircraft, to add a control system to its A-6 craft to maintain the correct Halon ratio in the tanks. After two years of work for Grumman, Gull, a manufacturer of flight and electronic instruments for military aircraft, is testing such a unit.

Grumman first explored using laboratory instruments to measure gas concentration before going to Gull. However, it reject-



1. CONCENTRATION CONTROL. Gull's microprocessor-controlled explosion-suppression system keeps a constant Halon/air ratio in the air space of the fuel tanks of Grumman's A-6 attack bomber.

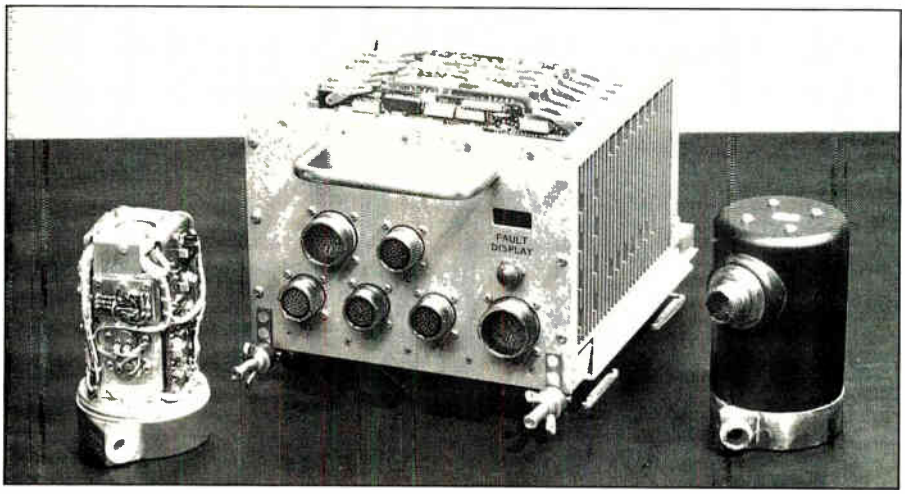
ed this alternative because lab instruments are too large, too sensitive, and too delicate, unlike the rugged militarized unit eventually developed by Gull.

Gull's system comprises a microprocessor-based control unit; four special Halon-concentration sensors, one for each of the A-6's fuel tanks; and four linear control valves that are part of a closed-loop system that maintains the correct Halon-to-air ratio in a fuel tank throughout a typical flight in a full military environment.

In Gull's control system (see fig. 1), Halon gas stored at high pressure is fed through a pressure regulator into one of four modulating control valves, supplied by Valcor Engineering Corp., Springfield, N. J., and into the air space of a fuel tank. A sample of the gas/air mixture in this tank is then sent to a Halon-concentration sensor for analysis. The sensor, in turn, sends three signals proportional to the density, absolute pressure, and temperature of the sampled mixture to the system control unit. Here, an 8088 microprocessor solves the ideal-gas-law equation ($PV/T=k$, where P is pressure, V is volume, T is temperature, and k is a constant). Additional circuitry in the control unit then generates an analog current proportional to the difference between ideal and actual gas concentrations. This current regulates the current controlling each valve's solenoid and maintains the proper concentration of Halon in the tank.

Each of Gull's Halon-concentration sensors (see fig. 2) comprises three different integral sensors and their signal-processing circuitry, all housed in the same sealed cylindrical package. The temperature sensor is a platinum resistance temperature detector, and the pressure sensor is a semiconductor strain-gauge bridge. Both emit an analog signal. The precision gas densitometer is an electromechanical resonator whose output is a variable-frequency signal (compatible with digital circuitry) proportional to density.

One feature Grumman mandated was built-in testing. "Without built-in testing, it would be extremely difficult to maintain the reliability and mean time to repair this unit, since many of the components are difficult to access," says Douglas H. Grundy, technical specialist for fuel systems at Grumman.



2. TRIPLE-HEADER. The concentration sensor, uncovered on the left, contains pressure, temperature, and density sensors plus signal-processing circuitry.

To begin testing, the pilot simply turns a switch. The controller then proceeds to test itself, the Halon-concentration sensors, and all the system's linear control valves. If all components are satisfactory, a special panel light will go off. If there is a failure, the light will stay on and a detected failure will show up as a two-digit coded number on a light-emitting-diode display. Each number will be used to identify the failed component so that it can be replaced. □

WHY DID THIS EE SOLVE THE GAS-LAW EQUATION?

Few electrical engineers ever find themselves in Martin Horowitz's shoes. Gull Inc.'s Horowitz headed the effort to design a concentration sensor to help solve the gas-law equation in the fuel tanks of Grumman's A-6 attack bomber.

Horowitz, senior vice president of Gull, a Smithtown, N. Y., manufacturer of flight and electronic instruments for military aircraft, was in charge of Gull's effort to design and build the control system and sensors for the Halon inerting system. One of Gull's founders, Horowitz has about 30 years of experience with fuel-management systems, engine performance indicators, and fuel-flow monitoring equipment.

MARTIN HOROWITZ

DOUGLAS H. GRUNDY

But it took a combination of fuel-systems expertise and electronics and control-systems know-how to successfully put together the Gull Halon-concentration control system for explosion-proofing the fuel tanks of the A-6, which is manufactured by Grumman Aerospace Corp. The fuel systems expertise for the project was furnished by Douglas H. Grundy, a technical specialist in fuel systems. Grundy, who has been at Grumman since 1958, was responsible for design efforts on the fuel systems of many Grumman aircraft.

Work on the Halon-concentration control system began when the Navy asked Grumman to suggest improvements that would increase survivability of the A-6, a single-engine attack bomber. One suggestion was to inert the plane's fuel tanks with Halon gas. The Air Force had tried this in an open-loop system on the F-16. but Grumman's analysts wanted a more precise control of the Halon/air percentage over the entire mission. Grumman then decided to go for a closed-loop system based on a concentration sensor in which the ratio of Halon to air would be controlled automatically during a flight.

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EF6852 – Synchronous Serial DATA Adapter (SSDA)
EF6854 – Advanced Data-Link Controller (ADLC)
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Device	Description	Clock Frequency	Clock Period (Max)	Processed or Qualified to
MKB/J68000	16-Bit MPU	6, 8, *10, *12.5 MHz 10, 12.5 (DESC)	250ns	JAN *Add'l JAN Versions to be Intro DESC 82021 Avail Q1 '87, MIL-STD-883
MKB68901	MFP	4, 5 MHz	100ns	MIL-STD-883
TS68008	16-Bit MPU 8-Bit DATA BUS	8, 10 MHz	500ns	MIL-STD-883 Version to be Intro Q1 '87
TS68230	Parallel Interface/Timer	8, 10 MHz	500ns	MIL-STD-883

SEMICUSTOM

Device	Process/Technology	Gate Count(1)	Processed or Qualified to
GB Series Gate Array	2 Micron, Double Level Metal, HCMOS	1,000 to 10,000 Gates	DESC Line certification JAN Qualification in Progress MIL-STD-883
GC Series Gate Array	1.2 Micron, Double Level Metal, HCMOS	1,000 to 10,000 Gates	MIL-STD-883 Qual in Progress

MEMORIES

Device	Description	Organized	Access Time	Processed or Qualified to
MKB/J4501	Biport FIFO	512 x 9	*65, *80, 100, 120, 150ns	JAN MIL-STD-883, *Add'l JAN Versions to be Intro
MKB41H67	CMOS	16K x 1	25, 35, 45ns	41H67 Avail Q2 '87
MKB41H68	Fast SRAM	4K x 4		41H68 Avail Q1 '87 MIL-STD-883
MKB4801A	Fast SRAM	1K x 8	70, 90, 120, 150ns	MIL-STD-883
MKB6116	CMOS SRAM	2K x 8	250ns	MIL-STD-883
MKB/J4116	DRAM	16K x 1	150, *200, *250ns	*JAN Version, MIL-STD-883
MKB/J4564	DRAM	64K x 1	150, 200ns	JAN, DESC 82010, MIL-STD-883
MKB/J45F56	DRAM	256K x 1	100, 150ns	DESC Line certification JAN Qual in Progress DESC 85152 Avail '87 MIL-STD-883 Avail '87

Note 1: 1 gate is the equivalent of a 2 input NAND or NOR gate.

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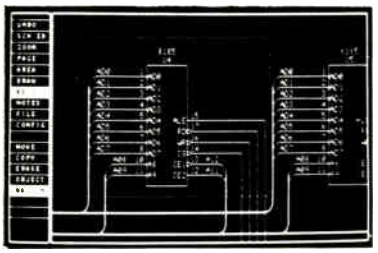

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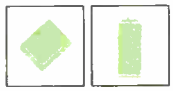

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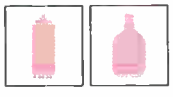

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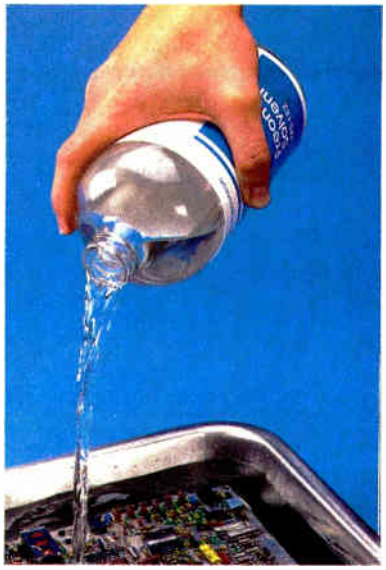

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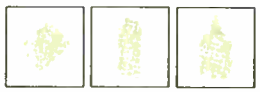

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A two-chip set from Bipolar Integrated Technology executes 60 million 64-bit floating-point calculations per second—more than a third the performance of the original Cray 1 supercomputer.

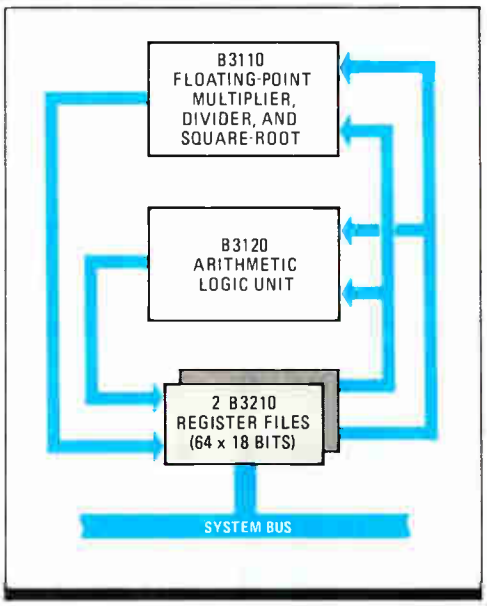
The chips owe their high performance to the advanced BIT1 process, which produces emitter-coupled logic devices that combine high speed, high density, and low power consumption [*Electronics*, April 7, 1986, p. 35]. The chip set will be available from the Beaverton, Ore., company later this year.

TINY. By creating what may be the world's smallest bipolar transistor, Bipolar Integrated Technology has produced VLSI ECL circuits with very reasonable power dissipation. The BIT1 self-aligned polysilicon bipolar process, with its 14-μm^2 transistors, uses two metal layers and produces chips with 300-ps gate delays and power dissipation of 0.3 mW per gate. All this adds up to the fastest VLSI chips on the market, claims the company.

BIT1 is used to make the powerful 64-bit B3110 floating-point multiplier chip and companion B3120 arithmetic logic unit. With 63,000 and 65,000 transistors, respectively, these are the most complex bipolar chips to date. When combined with a couple of BIT's B3210 multiport register-file chips, they produce a floating-point processing subsystem with performance that is about five times faster than the fastest currently available floating-point chips.

The multiplier performs 32-bit single-precision or 64-bit double-precision floating-point multiplications, divisions, and square roots, as well as multiplying two 32-bit integers in a single cycle. Division and square-root instructions do not require external storage of a look-up table. In the worst case, the multiplier takes only 35 ns and 45 ns to do single-precision and double-precision multiplications, respectively. The worst-case square-root times are 170 ns for single and 325 ns for double precision. On division, the worst-case times are 105 and 180 ns for single and double precision, respectively.

The chips avoid the disadvantage of pipeline processing, which requires several cycles to generate the first result: by using a flow-through architecture, BIT ensures that each operation initiated in a cycle is completed and emerges in the same cycle. In addition to being faster, a flow-through design is easier to control, because no software is required to manage several stages in a pipeline.



FLOW THRU. BIT's floating-point chip set completes each operation initiated in a cycle in the same cycle.

Another architectural feature is the built-in error checking. Parity generation and checking are done on all of the data ports. Also, scan paths that are for testing are provided on all of the registers.

There are two versions of each chip. The ECL 10KH-compatible B3110 multiplier and the B3120 ALU represent the top of the line. For those designs requiring TTL compatibility, the company offers the B2110/B2120 TTL versions. Typical power dissipations are 7.8 W for the ECL set and 7.0 W for the TTL version.

Both versions come in 169-pin grid arrays. The B3110 and B3120 chips cost $640 each in 100-unit lots. The B2110 and B2120 models cost $490. Prototypes will be available next month, and the set will become available in production volumes in July.

– *Tom Manuel*

[Circle 360]

INTEL ENHANCES 80386 WITH DMA, CACHE CHIPS

With two new 32-bit peripheral chips, Intel Corp. is aiming to take full advantage of the computing power of its powerful 80386 microprocessor and to push applications for future 80386 versions into the minicomputer and work-station markets.

The new chips are the 82380 direct-memory-access controller, which is capable of transferring data at 40 megabytes/s, and the 82385 cache-memory controller, which can store address tags for 32-K bytes of cache memory. Both chips run at 16 and 20 MHz.

With these chips, plus the 20-MHz 80386 and the 80387 floating-point processor, Intel is in a position to firm up its business-applications base and make inroads into work stations and minis, says Dana Krelle, product-line manager for the 386.

The new peripheral chips will hasten the 80386's migration to more powerful work stations by speeding memory functions. In fact, the migration has begun. Sun Microsystems Inc. and Apollo Computer Corp. have plans for 386-based work stations, says Krelle. Minicomputers are the next step, since 32-bit micros will equal the performance of minis built with discrete devices.

"We want to provide a standard machine for each of these markets," he says. "That means a main central processing unit, accelerators, memory subsystems, and system peripherals. De-

signers can build on these to make their systems more valuable to the end user."

Intel calls its 82380 DMA controller an integrated system peripheral, since it also incorporates most of the peripherals in the previous 8086, 80186, and 80286 microprocessor generations.

The 82380 includes supersets of the 8259 interrupt controller, the 8254 counter-timer, a programmable wait-state generator, and several other system-level functions. The 82380 replaces 25 LSI devices offered with the previous generations, says Krelle. As a DMA controller, it can support eight I/O devices and has a data-transfer rate of 40 megabytes/s.

The 82385 cache controller fills a need imposed by the ever-faster CPUs. At 20 MHz, Krelle says, cache memory will become a virtual requirement to realize the full performance capability of the CPU. The 82385 stores the address tags for caches of up to 32-K bytes. "This gives reasonably nice timing considerations for the data static random access memories," says Krelle. "At 20 MHz, you can use 35-ns SRAMs, which are generally available today."

The cache controller can also monitor the system bus to see what data is changed in main memory and then invalidate corresponding cache data. Using the same technique, it can maintain coherency among several caches in a multiprocessor system.

Intel's current choice for a CPU is the 20-MHz version of the 80386, but Krelle hints that a 25-MHz version is on the way. Intel is also offering samples of its 80387 floating-point processor, which will be in production in three months.

All four new chips will be offered in both 16- and 20-MHz versions, although they are at different states of readiness. Two versions of the 80386 central processor are available in production quantities now, at $299 for the 16-MHz chip and $599 for the 20-MHz version. The 16-MHz 80387 is priced at $500; the faster version has not yet been priced.

The 82380 DMA controller is now available in sample quantities; it will be in production in the second quarter at $149 and $299 for the 16- and 20-MHz versions, respectively. No prices have been set for the 82385 cache controller, which will be offered in sample quantities by midyear and in production by the fourth quarter.

[Circle 362]

CHIPS BOOST COMMUNICATIONS RATES

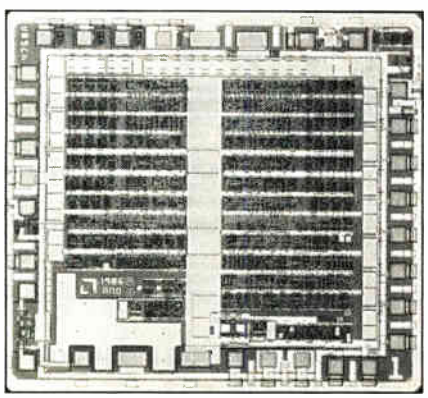
Advanced Micro Devices Inc.'s TAXI chip set, a transmitter/receiver asynchronous interface, performs automatic parallel-to-serial and serial-to-parallel data conversion that supports serial communications rates 10 times greater than current systems.

The set can handle high-speed encoded serial communications ranging from 40 to 120 Mb/s, compared with AMD's industry-standard Am2LS driver/receiver set's 10 Mb/s, according to the company.

Since such high data rates were previously only attainable with multiline parallel transmission systems, the chip set also opens the door to vastly reducing the number of lines in communications systems.

The Am7968 transmitter and the Am7969 receiver are among the first devices that AMD has fabricated with its 1.5-μm bipolar IMOX-III process using current-mode logic instead of emitter-coupled logic. The choice of CML largely accounts for the chip set's higher performance.

CML basically consists of an ECL current-steering structure without emitter followers and output-current sources. In this configuration, gate delays are reduced by as much as 50%, which accounts for the TAXI chip set's high data-transfer rate. The CML gates used in the TAXI chip set are designed for a 340-mV swing, with a 100-μA maximum gate current at 155° C junction temperature, and they have subnanosecond propagation delays.



The choice was also critical in the analog phase-locked-loop circuitry of the transmitter chip, says AMD, because CML provides a jitter performance of better than 200 ps.

CML gates have small switching transients compared with ECL gates, making them ideally suited for high-speed coaxial and fiber-optic communications applications, where internal noise can hinder the performance of the chip.

POWER MISER. In addition to noise immunity, CML offers advantages over ECL in power consumption and density. Eliminating the emitter followers lowers power consumption by as much as 30% to 50%, says the company.

The TAXI chip set operates like a pseudo parallel register, loading data into one side and outputting it on the other, except that the two sides are separated by a long serial link.

Parallel messages are strobed, encoded, serialized, and shifted onto the communications link by the transmitter, which takes its byte-clock rate from an on-chip crystal oscillator circuit.

The chip set supports three transmission modes for serial to parallel conversion: 8 data bits and 4 command bits; 9 data bits and 3 command bits; and, 10 data bits and 2 command bits.

The TAXI receiver decodes and deserializes the bits, and then strobes them out as parallel command or data bits. No complex protocols are necessary, since message transfers are established by employing a simple handshake mechanism. When there are no messages on the link, a unique synchronization pattern is transmitted as a filler to maintain contact for transfers.

The dc input current on each device is 100 mA, and the output current ranges from -30 to +5 mA. The set will be available later this quarter in samples of 28-pin plastic leaded chip carrier, leaded chip carrier, and dual-in-line packages. Each set will cost $50 to $60 in 100-unit purchases. Production quantities are expected to be available by midyear.

–Bernard C. Cole

[Circle 361]

HITACHI 1-Mb SRAM CUTS SPACE NEEDS

A 1-Mb static RAM module from Hitachi America Ltd. packages four 256-K random-access memories together to reduce board space by two thirds over individually packaged chips.

The HM66204 has two 256-K SRAMS surface mounted on each side of a standard 600-mil-wide, 32-pin dual in-line package with a built-in decoder. The module's DIP design offers Jedec pin- and signal-compatibility with future monolithic 1-Mb devices.

The device is available with access times of 120 ns and 150 ns, and in a low-power "L" version that consumes 40 μW in standby mode and 50 mW in active mode. The price ranges from $90 for a low-speed standard power model up to $103.50 for a high-speed low-power model in quantities of more than 100 units. Sample quantities are available now.

Hitachi America Ltd., 2210 O'Toole Ave. San Jose, Calif. 95131.
Phone (408) 435-8300 [Circle 365]

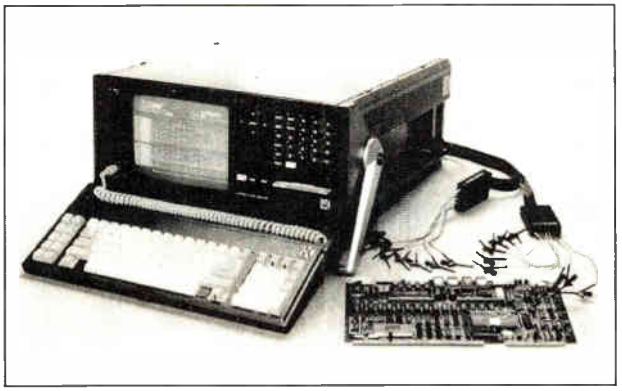
LOGIC ANALYZER DOUBLES AS PERSONAL COMPUTER

KONTRON'S PLA 286 ALSO HOSTS PATTERN GENERATORS, WAVEFORM RECORDERS, AND COLLECTS AND DISPLAYS DATA

Kontron Electronics Inc.'s PLA 286 is more than just a portable logic analyzer. Adding a keyboard, hard-disk drive, and a Microsoft Corp. MS-DOS operating-system package converts it to a portable computer, compatible with the IBM Corp. PC AT, that can host instruments such as pattern generators and analog waveform recorders, collect and display test data, and process the data using PC software.

The PLA 286 is based on the IP 286, a platform developed by Kontron Electronics' parent company, Kontron Electronik GmbH of Munich, West Germany, says James Corioso, product support manager. The IP 286 platform provides a 10-MHz, no-wait-state central processor based on an Intel Corp. 80286 16-bit microprocessor; a PC AT-compatible bus; 1 megabyte of random-access memory; a 3½-in., 700-K-byte flexible-disk drive; an interface for an external 5¼-in. floppy-disk drive; and a slot for a hard-disk drive. Users can also plug in PC cards for such peripherals as video monitors, printers, and modems.

The PLA 286 is set up with soft keys, pop-up menus, and cursors. Users can scroll through the analyzer displays—timing diagrams, data listings, and disassembled code—and can use the cursors to move display information.



POWERFUL. The PLA 286 logic analyzer includes a 10-MHz, no-wait-state central processor, memory, and I/O interfaces.

As a logic analyzer, the PLA 286 is expandable with two kinds of modules: one with 48 channels, for state or timing analysis at 20 MHz; the other eight channels, for timing analysis at 100 MHz. Recording memory depths per channel are 1-K at 20 MHz and 8-K at 100 MHz. The 20-MHz modules come with TTL-compatible probes or optional high-impedance probes.

A triggering subsystem provides two clocks and six qualifiers. For 20-MHz channels, trigger-selection modes include: up to 15 levels with one or two words per level; count-occurrence or windows modes; state or edge triggering; and true or false searching.

The 100-MHz modules operate with one or two trigger levels and feature edge triggering, event counting, and time-window triggering. An event-duration filter allows triggering on programmed pulse widths.

Kontron plans a family of personal instruments based on the IP 286. PLA 286 prices start at $7,400 for a basic system with forty-eight 20-MHz state and timing channels. A second 20-MHz module costs an additional $1,900. One or two 100-MHz modules can also be added at $1,800 each. The PC package costs $2,500. Delivery takes eight weeks. *–George Sideris*

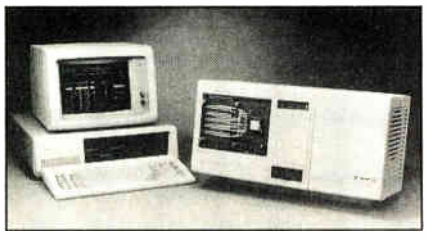
[Circle 380]

$40,000 VERIFIER HANDLES 100 PINS

Logic Master ST from Integrated Measurement Systems Inc. is a low-cost, compact verifier for application-specific integrated circuits that targets the market for moderately sophisticated prototypes—those with about 100 pins and operating around 10 MHz.

Logic Master ST handles chips with as many as 190 pins and operates at frequencies as high as 20 MHz. The basic 32-channel system costs $16,000, and a typical configuration with a 100-pin capability costs $40,000. In general, larger ASIC verifier systems offering 256 and more pins cost $150,000 or more.

Only slightly larger than a personal computer, the system uses an IBM Corp. Personal Computer XT as its controller. Designers configure tests for prototype chips using a simple command language. To ease the task of generating test signals, patterns generated on computer-aided engineering simulators can be transferred to the verifier over a standard personal-computer bus.



SMART. Logic Master ST uses an IBM Corp. PC XT as its controller.

Using the personal computer, pattern-generation channels can be programmed in non-return-to-zero and delayed-non-return-to-zero data formats. Leading edges of formatted data can be adjusted in 1-ns increments for precise measurement.

Logic Master ST also allows the incremental variation of test parameters such as voltage levels of drivers and receivers during the test cycle. This feature gives designers a quick way to determine the prototype chip's operating levels and margins.

To control the application of stimulus patterns, the system provides branching and looping in the test program. By programming the verifier to stop on errors, for example, thresholds are easily and quickly determined. But when dealing with devices that require complex initialization routines, Logic Master ST can be programmed to ignore all errors until the initialization is complete and then branch to begin the test.

Replaceable cards are used to attach any device, including pin-grid arrays, to the tester. Drivers and receivers connect directly to the fixture card to ensure a high-quality signal path to the device.

The verifier's standard power supply is 1 A and is programmable from 3.5 to 7 V. It will be available in March.

–Jonah McLeod

[Circle 381]

SIGNAL GENERATOR RUNS UP TO 2.1 GHz

A frequency generator from John Fluke Manufacturing Co. has signal-generation capabilities from 0.1 MHz to 2.1 GHz and incorporates a high-performance pulse modulator.

The 6062A's modulator uses gallium-arsenide switch technology to achieve rise/fall times of 15 ns and on/off ratios of 80 dB. The instrument's fast rise and

fall times permit high quality pulses of less than 50 ns. It is designed for applications in avionics, communications, and navigation.

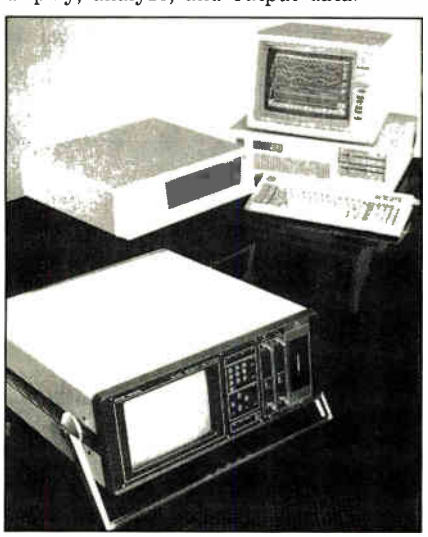
The generator's frequency is adjustable over the range of +16 to −137 dBm to 1,050 MHz, and +13 to −137 dBm to 2,100 MHz. It is accurate to ±1.5 dB. Amplitude measurements can be displayed in volts, dBm, dB uV, or dB mV. In the frequency range of 245 to 512 MHz, residual FM is less than 6 Hz.

Available in April, the 6062A costs $10,750. Delivery is four to six weeks.
John Fluke Manufacturing Co. P.O. Box C9090, Everett, Wash. 98206.
Phone (206) 347-6100 [Circle 385]

RECORDER HANDLES 16 CHANNELS AT 20 MHz

Soltec Corp. of San Fernando, Calif., offers a choice of personal computer-driven or stand-alone recorders with more than 1 megabyte of RAM and a recording capability of up to 16 channels.

Among the features of the stand-alone SMR2 Signal Memory Recorder are a 9-in. high-resolution CRT, 12-bit resolution, more than 1 megabyte of RAM supported by a built-in 10-megabyte hard disk, and programmable 100-mV to 100-V amplifiers. The unit records up to 16 channels of high-speed data at sample rates up to 20 MHz. Information can be downloaded to a fixed disk supported by a floppy disk for archive, backup, and data interchange. It comes with menu-driven software to record, display, analyze, and output data.



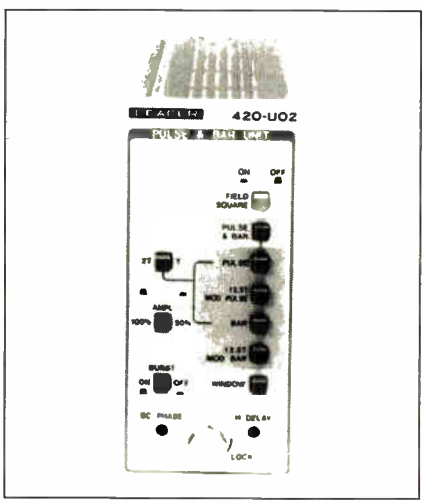
The SDA2000 Transient Waveform Recorder operates at 10 MHz and has a 2-megabyte RAM buffer. The personal-computer-driven model uses 50 mV to 80 V programmable amplifiers. It allows the user to immediately begin testing by connecting it to an IBM Corp. PC/XT or AT or compatible.

The SMR2 starts at $10,000, and delivery takes 60 to 90 days. The basic price for the SDA2000 is $12,395. Delivery takes from 14 to 30 days.
Soltec Corp., Sol Vista Park, San Fernando, Calif. 91340.
Phone (800) 423-2344 [Circle 386]

LEADER OFFERS VIDEO TEST UNITS

The Pulse and Bar Module and the Linearity Module from Leader Instruments Corp. are two plug-in devices for the LCXG-420 Main Frame Video Test Signal Generator that can be added to the signal generator without special tools.

The Pulse Bar Module, Model 420-U02, features selection of T or 2T $\sin^2$ pulse signals, with corresponding changes in rise/fall times. It can be used with 12.5 T signals, unmodulated and modulated bar signals, field square,



and window signals. The Linearity Module, Model 420-U03 has five and ten-step modulated staircase and modulated ramp modes. Chroma, or, standard phase differential, is achieved at 180°, and IRE levels can be selected at 20 or 40. A signal variable ranging from 0 to 100 IRE in increments of 10 may be modulated with single-level chroma, 5 IRE at 90°, or three-level chroma, 20, 40, or 80 IRE at 90°. The device also features alternate switching between selected functions and variable-rate bounce from 0 to 100 IRE.

Model 420-U02 is priced at $1,195 and Model 420-U03 at $1,335. Delivery from stock takes two weeks.
Leader Instruments Corp., 380 Oser Ave., Hauppauge, N.Y. 11788.
Phone (800) 645-5104 [Circle 388]

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DISTRIBUTION WEEK

KEY DISTRIBUTORS SEE ASIC BUSINESS AS LIGHT AT END OF INDUSTRY SLUMP

While the application-specific integrated circuit design business has been one of the few sectors to continue to grow aggressively through the semiconductor business's two-year slump, distributors have been eyeing ASIC design centers as a means not only of hedging against the current downturn, but also of positioning themselves for what some believe will be a major part of the semiconductor business over the next decade.

Hamilton-Avnet's director of ASIC services, Robert Gardner, says the advantage to the customer is that distributors can provide a turnkey service from—in Hamilton-Avnet's case—five gate-array manufacturers, instead of being married to just one. "We see a number of medium- and small-sized customers who would like to deal with an engineering design group to reduce their cost of using ASIC technology, " Gardner says.

Avnet has staffed seven design centers with 14 engineers since Gardner began directing operations two years ago.

So far, however, the ASIC business has not been particularly kind to distributors, according to Dean Winklemann, market research analyst for Integrated Circuit Engineering Corp., Phoenix, Ariz.

Of the dozen distributors operating ASIC design centers at the end of 1986, only one that responded to ICE's questionnaire—Hamilton-Avnet—reported that it was profitable.

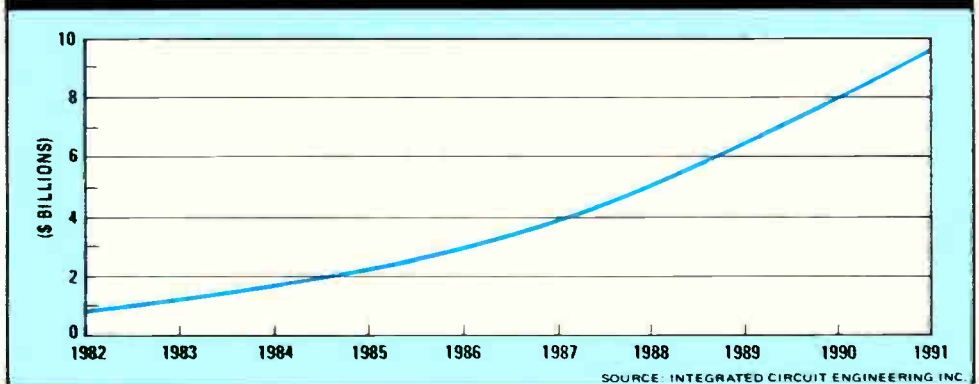
Distributors have been less than enthusiastic about releasing actual profit or loss figures in their ASIC business, but ICE has estimated that distributors had approximately a $20 million share of the $3 billion ASIC market in 1986 (see figure). "We don't project them as having more than 10% of the market by 1991," says Winklemann.

Nevertheless, Wyle Laboratories believes that participating in the ASIC business makes a lot of sense. As the ASIC market grows, so must distributors' interest in it if they are to keep pace, says Charles M. Clough, president and chief operating officer. Wyle has been active in the ASIC market for about two years, and Clough reports that "ASICs are about 10% of our semiconductor business, and by 1992, we project that ASICs will grow to $100 million at Wyle and be 29% of our total semiconductor shipments."

At least one distributor thinks ASICs aren't crucial to long-term growth. "Right now, 35% of the distribution business is semiconductors, including discretes and circuits," says Pete Heller, board chairman at Pioneer Electronics Inc. "Let's say 40% of that goes ASIC. That's 14% of the total distributor TAM [total available market]. So you don't have to be in it to succeed."

On the other hand, Heller acknowledges that distributors who succeed in the ASIC business "have an incremental growth opportunity that others won't." Pioneer will play a limited role, he says, by using suppliers' design centers rather than its own and acting as "a professional information conduit."

APPLICATION-SPECIFIC ICs: PROJECTED U.S. MARKET GROWTH



ASIC DESIGNER SIGNS WITH DOLCH

Valley Data Sciences, a manufacturer of low-cost, entry-level systems for designing application-specific integrated circuits, has given Dolch Instruments of Dietzenbach, West Germany, exclusive rights to market its complete line of products in West Germany and the UK.

Dolch is expected to concentrate its efforts on Valley Data's "concept-to-chip" package, called PASIC, for Programmable Application-Specific Integrated Circuit. PASIC is a microcomputer-based design system that includes the hardware and software needed to design, compile, simulate, and program ASICs. In particular, it is compatible with a wide range of programmable-array logic.

BELL, SANDIA SIGN $10 MILLION DEAL

The Electronics Distribution Division of Bell Industries Inc., Los Angeles, has won an exclusive three-to-five-year contract with a minimum $10 million value to supply electronic components to Sandia National Laboratories of Albuquerque, N. M.

Under the agreement, the company will deliver an annual minimum supply of $2 million of electronic components for Sandia's research and development efforts as a prime contractor to the U. S. Department of Energy. Bell says one reason it won the Sandia contract is the success of its just-in-time program, which saves customers warehousing and other inventory costs through delivery of components on an as-needed basis.

NIPPON MOTOROLA CUTS TTL PRICES

Nippon Motorola Ltd. has reduced the prices of its low-power Schottky TTL devices by an average of 30% in an effort to increase its market share in Japan.

The price cut comes on the heels of gearing up production, which has earned economies of scale. Last September, the Tokyo company increased the assembly capacity of its Aizu plant to 40 million to 50 million devices per month. The company also doubled the throughput of its testing facilities.

MITEL SIGNS SECOND SOURCE

Mitel Corp., Kanata, Ontario, Canada, an international manufacturer of telecommunications equipment and semiconductor devices, has signed a second-sourcing agreement with GTE Microcircuits Corp., permitting the Tempe, Ariz., company to produce the MT8880 single-chip dual-tone multifrequency transceiver.

ELECTRONICS WEEK

EXPORT CONTROLS MAY CHANGE

The U.S. Department of Commerce is proposing drastic changes to its export licensing procedures that could help make U.S. high-technology industries more competitive in world markets. Many U.S. industries are now hog-tied by an export control system that virtually shuts them out of world markets, because prospective customers can never be sure U.S. products will be approved for export. Under the proposed system, general licenses would be issued to "certified end users," beginning with government agencies and government-controlled enterprises in the 16 member nations of the Coordinating Committee on Export Controls, or Cocom, which includes members of the North Atlantic Treaty Organization and Japan.

DATAQUEST SPINS OUT BANKING UNIT

Dataquest Inc. has spun off an in-house operation as DQ Alliances, a specialized investment banking boutique that handles high-tech strategic alliances, mergers, and acquisitions. Heading the new affiliate is David G. Jorgensen, former chairman of Dataquest. Last year the unit handled the divestiture from Kearney-National Inc. of Wabash DataTech, which was sold to Shape Inc.; arranged a strategic alliance for Information Appliance Inc.; and helped Triad Semiconductor arrange startup financing.

IBM HELPED A LOT BY WEAK DOLLAR

The declining dollar kept IBM Corp.'s underwhelming 1986 performance from being even worse. If currency rates had remained constant last year, its $51.3 billion in gross income would have been $4.4 billion less, while the $4.8 billion in net would have been off another $645 million. The bouncing buck, then, earned IBM 10% of its gross and more than 7% of its net in 1986. Revenues for peripherals, office systems, and work stations dropped more than 10%. But two revenue streams showed strong increases: maintenance services were up 21%, and programming increased 34%.

ZIP CODE READERS TO BE UPGRADED

The U.S. Post Office board of governors voted this month to modify an existing contract with ElectroCom Automation Inc. of Arlington, Texas, allowing it to change the design of its single-line readers to handle multiple lines and a nine-digit zip code. Nearby Recognition Equipment Inc. had been competing against ElectroCom to upgrade the gear and ship 290 new systems, for about $320 million [*Electronics*, April 28, 1985, p. 19]. The competition was canceled last year after a postal official pleaded guilty to taking bribes from an agent representing Recognition Equipment. The Irving, Texas, company denies any wrongdoing and still seeks business with the postal agency.

SUN OUTBIDS 3COM FOR CENTRAM

Not the 3Com Corp. but its Silicon Valley neighbor and customer, Sun Microsystems Inc., will probably be the buyer of Centram Systems West, the Berkeley, Calif., supplier of networking software. Sun stepped in with a stock offer valued at $20 million, about a third greater than 3Com's, one day after the 3Com-Centram letter of intent expired [*Electronics*, Feb. 5, p. 110]. Both Sun and 3Com wanted access to Centram's entry-level TOPS software, which permits Unix-based and MS-DOS systems and Apple Macintosh computers to share data files.

TERADYNE GETS BIG ORDER FROM AMD

Spirits are running high at Teradyne Inc., despite a lackluster earnings report for fiscal 1986. The Boston test-equipment vendor landed a $7 million order from Advanced Micro Devices Inc. for VLSI test equipment, including the first orders for Teradyne's new high-performance J953 tester [*Electronics*, Nov. 13, 1986, p. 72].

TI AND TOSHIBA SETTLE SUIT

Texas Instruments Inc. has reached a third settlement in its series of patent suits filed against nine Japanese and South Korean dynamic random-access-memory manufacturers. The Dallas chip maker and Toshiba Corp. have agreed to a new cross-licensing pact, covering DRAM-related technologies, and TI will drop its claims against the Japanese company. Last month TI separately reached similar settlements with Sharp Corp. and Fujitsu Ltd. [*Electronics*, Jan. 22, p. 19].

UNISYS WILL CLOSE MINNESOTA FAB LINE

Unisys Corp. plans to cash in its chips in Minnesota and move all semiconductor operations to the West Coast. Citing a current overcapacity, the Detroit computer maker—formed by the merger of Burroughs Corp. and Sperry Corp. last year—will phase out its chip-fabrication plant, formerly operated by Sperry, in Eagan, Minn., and consolidate circuit design and fabrication at a former Burroughs plant in Redondo Beach, Calif. Unisys says it hopes to convert the plant to other uses.

VALID LOGIC TRIES TO HANG ON IN CAE

Embattled Valid Logic Corp. has taken on a new management team and enhanced its product line in an attempt to hang on to a role in computer-aided engineering. Stung by a loss of $7.8 million in the final quarter of 1986, Valid, of San Jose, Calif., has agreed to merge with printed-circuit-board design firm Telesis Systems Corp., of Chelmsford, Mass. Telesis's president, W. Douglas Haffar, will become president of the combined company, and Valid founder and chairman Jared A. Anderson and president Kenneth B. Fine will resign. Valid has also cut the price of its entry-level work station by $3,000, to $15,950, and has licensed LSI Logic Inc.'s channeled-gate-array technology.

KEY SMART-CARD CONTRACT AWARDED

Micro Card Technology Inc. of Dallas has won from the U.S. Department of Agriculture the largest single contract for smart-card technology. The program will be the first real test to see if reliable smart cards can be produced in the U.S. The contract calls for at least 60,000 cards, which are the size of a credit card and contain an embedded computer chip and support circuitry, and 1,000 readers. The cards will be used by peanut farmers [*Electronics*, Jan. 8, 1987, p. 24] as part of a project to automate their marketing centers.

STEVE JOBS' NeXT PICKS UP PLAYERS

Both Stanford Univeristy and Carnegie-Mellon University have made small investments in NeXT Inc., the educational computer company started by Apple Computer Inc. founder Steven P. Jobs. Each institution has a 0.5% stake in NeXT after investing a total of $1.32 million. The company also announced that H. Ross Perot, recently bought out as head of Electronic Data Systems Corp. by General Motors Corp., invested $20 million in NeXT in return for a 16% interest and a seat on the board.

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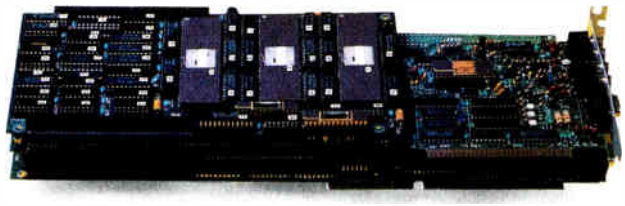

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