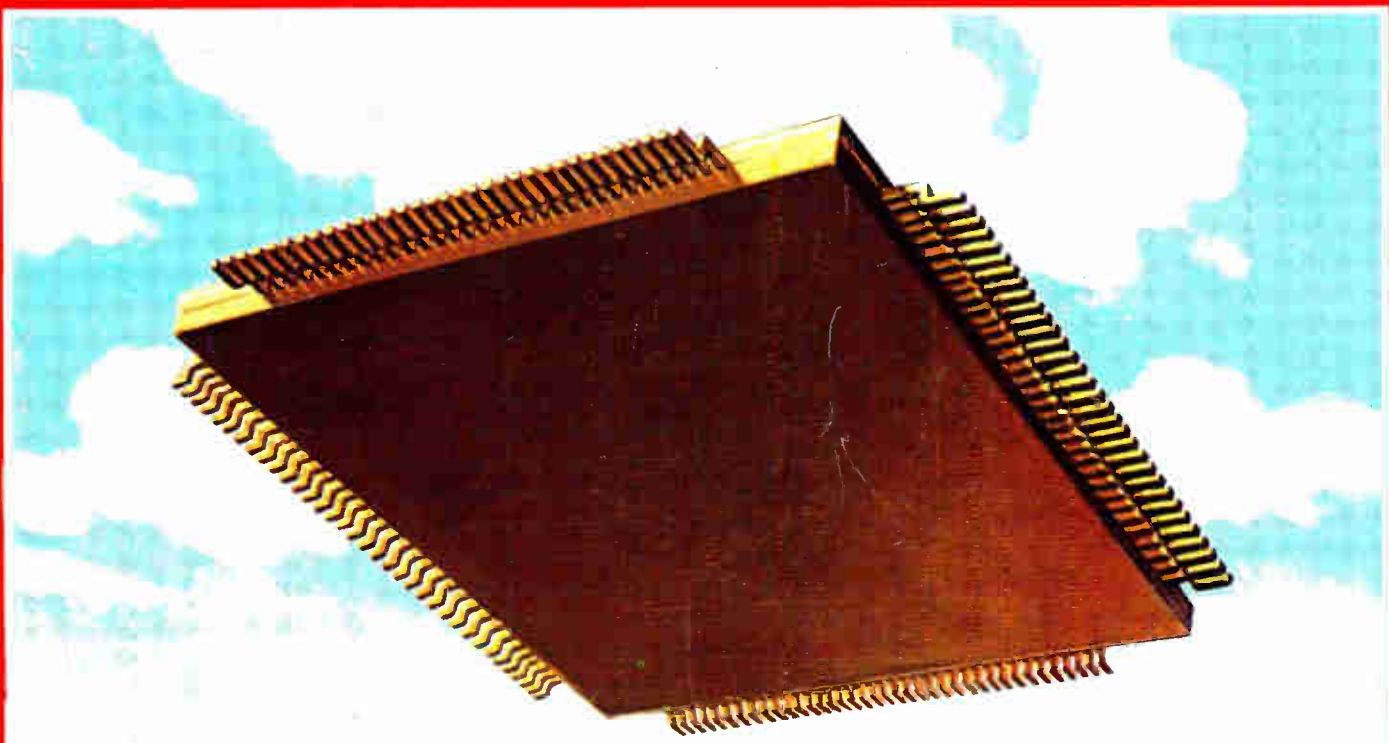
BREAKING THE SPEED BARRIER ON VMEBUS/58

EUROPEANS COUNT ON UNIX TO FIGHT IBM/121

MIDYEAR MARKET REPORT
PAGE 105

A McGRAW-HILL PUBLICATION SIX DOLLARS JULY 10, 1986

Electronics



TRW's SUPERCHIP PASSES FIRST MAJOR MILESTONE

PAGE 49

Take Control!

Chart your own course in CMOS system power and performance.

Harris gives you control. Our static CMOS circuits allow you to match system power and performance to your exact requirements, from DC standby to full-speed operation...

- 80C86 and 80C88 static CMOS CPUs for flexible system design
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Full range operation. Completely static design ensures stable, reliable operation in the toughest applications. And our new 82C85 Static Clock Controller gives you control of four low-power modes: fast for full-speed operation...slow for continuous operation...stop-clock for low power...stop-oscillator for the lowest possible power. You get low-power operation without sacrificing performance.

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Circle 900 on reader service card

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That's what you get from Infotek's new cost and space saving 2 MByte HP 9000-compatible memory.

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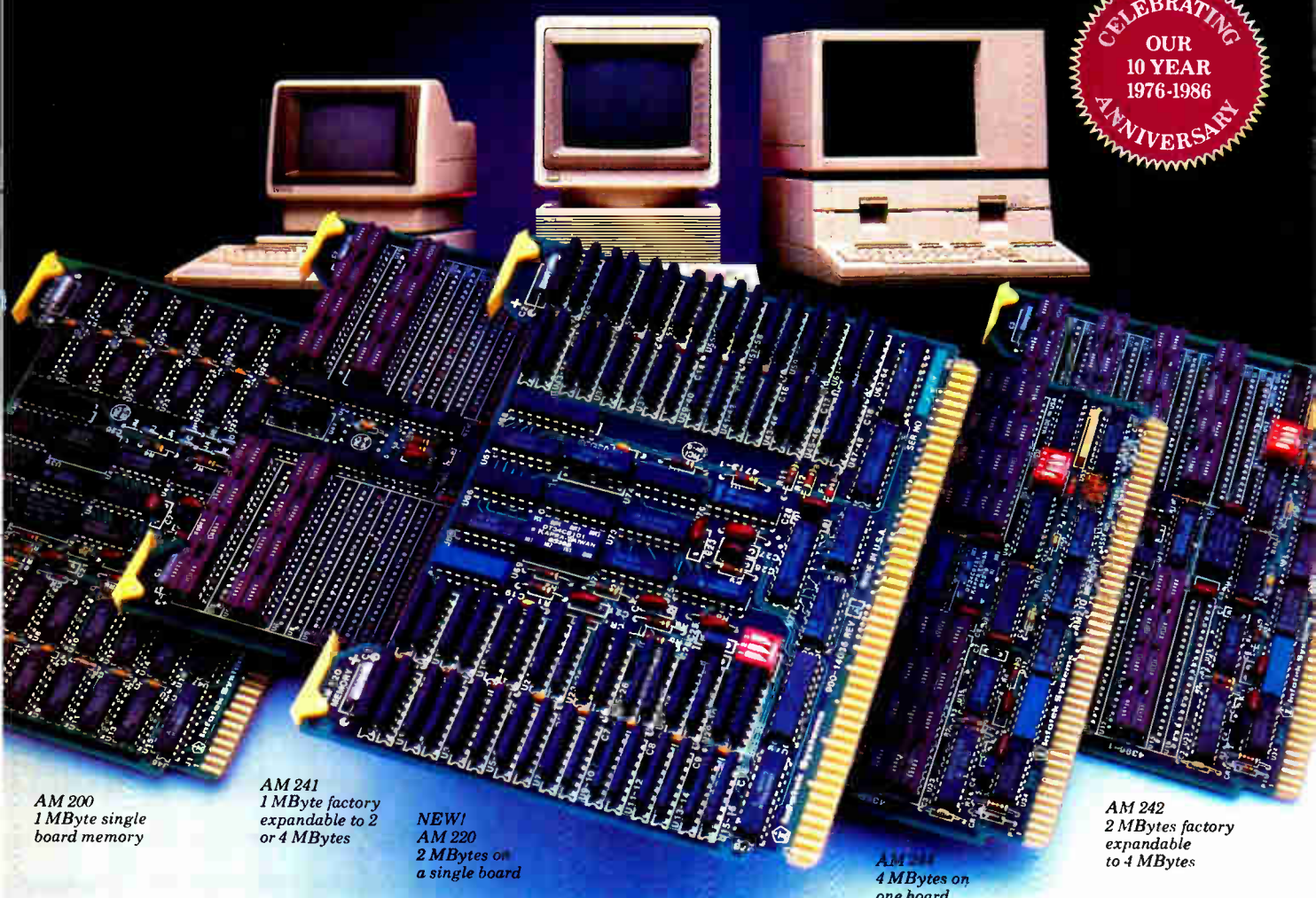

AM 200
1 MByte single board memory

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1 MByte factory expandable to 2 or 4 MBytes

NEW!
AM 220
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AM 241
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Now, you can have a full two megabytes of instantly accessible memory for your HP Series 300 and Series 200 computers for a price you'd expect to pay for 1 MByte. That's like getting half your memory free! And even better, you get those 2 MBytes on a single board, so all that extra capability occupies only one I/O slot. You just plug in the new board in seconds with no special tools required.

The new Infotek AM 220 2 MByte memory board is ideal for all scientific and engineering applications where large memory requirements remain constant. A 1 MByte product is also available at a very reasonable cost; and, for maximum capacity, Infotek offers a 4 MByte single board memory.

If your data storage needs are growing, you can have Infotek's unbeatable price/performance/size benefits in an expandable single board memory—1 MByte of memory upgradeable to 2 or 4 MBytes, or a 2 MByte board which expands to four when memory requirements increase. You can even get a floating point processor and 1 MByte of memory on a single board.

Of course, all Infotek memory boards have the high quality you demand for your HP system. Their exceptional reliability is backed by a two-year warranty. So increase productivity, save time, and enhance the capability of your HP 9000 computer. Call Infotek toll free today. The only way to get MegaBytes without spending MegaBucks.

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MITEL SEMICONDUCTOR

ISDN

COMPONENT NEWS

Vol. 3

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Circle 2 on reader service card

Electronics

PUBLISHER'S LETTER

With this issue, *Electronics* returns to a biweekly publishing schedule, and it seems to be an appropriate time to step back and take a look at you, the reader, and just what you like and expect from your magazine.

We have always maintained that the 300,000 people who make up our readership are unique in our industry. To find out just how special you are, we decided to ask you what you think of the job we have been doing, the information that we bring you in each issue, and the way we present that information. The method was to conduct a detailed telephone survey, calling several thousand readers over a period of several months. Now, with the results in, it turns out that we have been right.

For example, you proved that we are right when we boast of having the most loyal readers in the business. When we asked you if you read your copy of *Electronics* cover to cover, 92% of you replied that you did, while just 5% said no. And what you want to read about most of all in each issue is technology: 81% placed technology news at the top of the list, 79% voted for in-depth technology developments and analysis, 43% said they look for business and industry news, and 22% went for company and marketing strategy.

You are more interested in the type of information we bring you than in the way we present it. In fact, 67% of you want to see both in-depth reporting and brief, quick-paced presentation, while 17% prefer the shorter format and 16% prefer to read information presented in depth.

And you are absolutely sure about what kind of information you need. A resounding 73% of you say what you need is related to technology trends, perspectives, and design implications. And some 19% believe that detailed and application- or specification-oriented articles are required.

It was particularly gratifying for us to find that you are so pleased with what we produce. Your satisfaction level is high: 83% of you say that you are mostly or completely satisfied with the magazine and 11% pronounce yourselves somewhat satisfied. Only 5% are not satisfied—and we're determined to win you over.

But you still have definite ideas about what *Electronics* should do in the future, with most of your preferences having to do with news coverage and analysis of technology developments. Some 71% of you want to see more technology news and developments; 78% prefer more in-depth technology analysis and perspectives; 21% want more detailed design and application information; and 28% seek more industry and business news.

Finally, 82% of you welcome our new biweekly publication schedule. Some 31% prefer to see us every other week, and 51% like us no matter how often we come out. Eighteen percent prefer a weekly.

So we think you're pretty special—even though there are 300,000 of you. We promise to return your loyalty by making *Electronics* more indispensable as the magazine you need and want.

Laurence Altman

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JULY 10, 1986

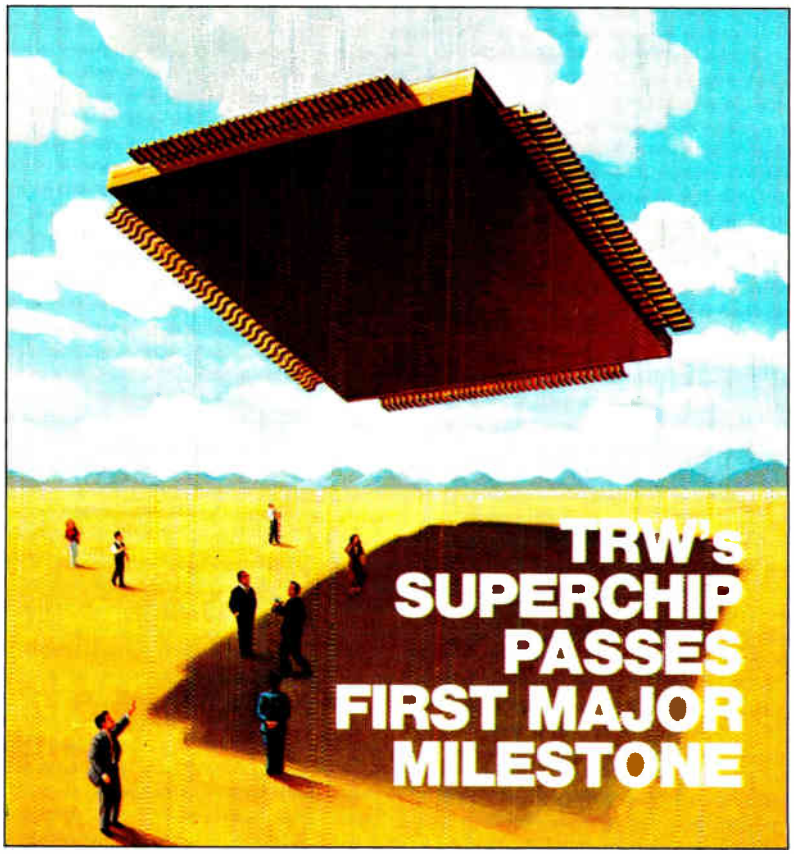
Electronics

NEWS

INSIDE TECHNOLOGY

PROBING THE NEWS

COVER: JOEL NAPRSTEK



PAGE 49

NEW PRODUCTS

DEPARTMENTS

WEEK 38

If you're racing along technology's edge, meet the most powerful 32-bit ALU around. The Am29332. It's the newest member of our Am29300 Family. Besides doing everything a less powerful ALU will do it also has a mask generator, funnel shifter and field logical operations. And it does it all in a single 80ns cycle. And every last nanosecond helps you beat the competition.

Am29332

It helps to know a powerful family.

The single-chip Am29332 uses everything it's got to achieve such incredible speed. To keep data racing through, it's designed with a built-in carry look-ahead and barrel shifter. A priority encoder insures that the most important data gets through first.

Whatever design you're working with, don't worry. The Am29332 is designed to let you emulate almost any system.

The Am29332 sets you free of the bonds of your present architecture. Because of the built-in high level instruction set and the three-bus flow-through architecture you get maximum performance and flexibility. And since correct breeding is important to powerful families, data integrity is insured through chip-level fault detection.

The Am29332 is just one member of a complete family solution to high performance 32-bit processing. A family that's nice to know when you need more power than anyone else.

Design and application seminars are available for this product. Write or call for information.

Circle 151 on reader service card

WEEK 39

AMD announces the Am99C641 64K CMOS SRAM. With access times down to 25ns, no one can beat it.

Am99C641

The pedal hits the metal.

But don't forget, this is a CMOS SRAM. It uses 110mW (max.) on stand-by (TTL-level) and all of 8mW on data retention. Lots of speed and no power dissipation problems.

The Am99C641 has a 64K x 1 organization in a stylish 22-pin 0.3" wide DIP.

Best of all, it's made by AMD, the folks who design what you need to stay as far ahead of the competition as they are.

So when you need 64K of blinding speed married to CMOS cool, check out the Am99C641 64K CMOS SRAM. Because there's no such thing as too fast.

Circle 152 on reader service card

WEEK 40

At last there's a microprocessor that's an arch conservative when it comes to power issues and a flaming liberal when it comes to high performance: AMD's Am29C117 16-bit CMOS Microprocessor. It's fast, but it only uses a frugal 25% of the power of the bipolar Am29117.

Am29C117

Cross party lines.

Get ready to save a lot of time if you're designing a pipeline system. The Am29C117 has two separate I/O ports for simplified timing, so you can achieve up to a 15% increase in throughput on a system basis over an Am29C116. A 16-bit barrel shifter allows you to shift or rotate a word up to 15 positions in a single instruction cycle.

That means you don't have to worry about extra parts or using valuable board space. It's plug compatible with the Am29117 and uses the same instruction set.

It has a 125ns microcycle time. Or an 8mHz data rate.

It's really a very simple concept. When parties cooperate, everybody wins.

Circle 153 on reader service card

WEEK 41

Usually there are lots of IC sources. With a new chip, though, there may be only one place to find it.

Until today, that's been the case with NCR's 5380 SCSI Peripheral Interface. Not anymore. Introducing AMD's 5380 SCSI Peripheral Interface. Strangely enough, it's just like NCR's. As a matter of fact, it's a plug-in replacement. (NCR's meets the ANSI Standard Committee X3T9.2. So does ours.)

5380

To have and have not.

But AMD's 5380 comes with something no one else can offer. It's the International Standard of Quality. It makes a very big promise that we keep with the 5380 and every other IC we sell. We guarantee a 0.05% AQL on all electric parameters, AC and DC, over the entire operating range. Because we think it's no use having the 5380 or any other part if it doesn't come with a promise that means something.

The 5380 with INT•STD•500. Only from AMD.

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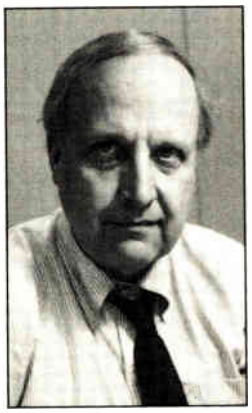
FYI

Adding value is still the prime directive at Electronics; we don't want to contribute to the growing stream of raw data that is being directed at our readers



We had but one major goal in mind 14 months ago when I returned to *Electronics*: restore this magazine to its former greatness. That meant bringing back and updating the interpretive technical coverage it had been famous for over the past half century. Returning to our traditional biweekly publishing schedule is the final step in achieving that goal. Don't look for major changes: we're delighted with the progress we've made to date. So are the readers, based on the letters we've been getting.

Back when the vacuum tube was king, this magazine earned its spurs by breaking important technology news and putting it in focus for all readers. Our editorial niche is still that: analyzing new developments and putting them in perspective. As one longtime reader puts it: "I read *Electronics* cover to cover for the big picture in technology." We've brought all that back during the past year—and more. We're tailoring coverage to fit the changing information needs of technically trained managers as they move into the complex world of the late 1980s and 1990s. These executives need to know more about more technologies than ever. Yet they have less time than ever to keep up. No publication is better equipped to help them than we are.

Competing publications, which have changed little in recent years, fall into two extremes: the technical magazines with their long-winded, narrowly focused "nuts-and-bolts" articles and the tabloids and general news publications that run undigested press releases and nontechnology coverage. The nitty-gritty tech article is understandable only to a narrow band of engineers, while the news story based on a nontechnical announcement or press release doesn't interpret what's happening and often fails to give both sides. The biweekly *Electronics* will carry more of the technology news we're known for—coverage the competition can't provide. More staff-written Technology To Watch articles will announce new technology and put it into perspective. The New Products section will explode in size, and sharp-eyed readers will spot an old friend: the International Newsletter, something only this magazine can turn out, because no competitor has more than a token foreign staff. Adding value is still the prime directive at *Electronics*; we don't want to contribute to the growing stream of raw data that is being directed at our readers.

ROBERT W. HENKEL

DEVELOPMENT TO PRODUCTION IN ONE DAY

Hitachi's 8-bit microcontroller gives you Zero Turn-Around Time.

Now you can have fully-coded 8-bit ROM-on-chip microcontrollers in just one day. Hitachi's ZTAT™ (Zero Turn-Around Time) products make it possible.

ZTAT is a series of 6301/6305 compatible ***all-CMOS*** *microcontrollers* with one-time-programmable ROMs—in *plastic* packages. Since you can program them yourself, there's no turn-around time, no mask charges, and no minimum order quantities. And, the plastic packaging makes ZTAT cost-effective for production runs as small as *one*, or as large as 20,000.

Hitachi has the right CMOS 6301/6305 series device for each phase of your product's life cycle: windowed ceramic package EPROM-on-chip devices for development, ZTAT for pilot production, and plastic package mask ROM devices for large-scale production. All are pin-for-pin compatible.

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Circle 9 on reader service card

At last, the ordinary microprocessor can take its rightful place in history.

It had to happen—the conventional microprocessor has had its day. Relegated to the ranks of yesterday's devices by the new transputer family from INMOS. It's history in the making.

The IMS T414 transputer is a fast, easy-to-use VLSI component, integrating a 32-bit processor, four inter-transputer communication links, 2K bytes Static RAM, 32-bit memory interface and DRAM controller. All on a single CMOS chip—offering execution rates up to 10 MIPs.

While transputers excel in single-processor systems, their real power can be unleashed by connecting any number of transputers together via the high-speed serial links. Multi-transputer systems can deliver the performance you need today, and can be easily expanded in the future as your processing requirements increase.

And there's more. Programming multiprocessor systems has never been easier. The Transputer Development System (TDS) supports C, Fortran, Pascal and OCCAM, providing a complete software development environment, and is available for a number of popular hosts. Software developed on the TDS can be executed on one or more transputers, enabling cost-performance tradeoffs to be made.

INMOS transputers are available now and have already found their way into companies who are evaluating, prototyping and manufacturing transputer-based systems. Applications include supercomputers, DSP, graphics, robotics, AI, distributed control systems and many others.

Write or phone for more information on the transputer family and start making history yourself.

TRANSPUTER PRODUCTS	
IMS T414	32 bit Transputer–2K Ram —4 links
IMS T212	16 bit Transputer–2K Ram —4 links
IMS M212	16 bit Disc Processor–1K Ram—2 links
DEVELOPMENT TOOLS	
IMS D701-2	IBM PC—Transputer Development System.
IMS D600	VAX/VMS—Transputer Development System.
EVALUATION BOARDS	
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IMS B003-1	Double Eurocard + 4 x IMST414 + 4 x 256Kbyte DRAM.
IMS B004-2	IBM PC Formot + IMST414 + 2Mbyte DRAM.
IMS B006-2	Double Eurocord + 9 x IMST212 + 128K SRAM.
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Circle 11 on reader service card

LETTERS

The HP 1000 marches on

To the editor: Hewlett-Packard is not ceasing development of HP 1000 A-series machines used for industrial control [*Electronics*, June 9, 1986, p. 53]. The HP 1000 line will continue to serve factory-floor computer applications for years to come. There will be future products in the HP 1000 product line as well as continued enhancement of the network services and operating system..

The HP 9000 model 840, reviewed in the same article, represents a convergence and an extension of the HP 1000 and HP 9000. In no way does its introduction imply any reduction of emphasis on the existing HP 1000s and HP 9000s. On the contrary, the HP 9000 model 840 has added appreciably to the acceptance of both by presenting tangible evidence of a smooth upgrade path for those that will require it.

Brian Moore
General Manager
Manufacturing Systems Group
Hewlett-Packard Co.
Cupertino, Calif.

Micrion 808 defended

To the editor: The story on Seiko Instruments USA Inc.'s SIR-1000 mask-repair system [*Electronics*, March 10, 1986, p. 71] contained some incorrect technical points about the KLA/Micrion 808. The article states that somehow the 808 damages the substrate in an uncontrolled way, resulting in poorer-quality repairs than can be achieved with the SIR-1000.

The 808 produces very high-quality repairs consistently and is the only production focused-ion-beam mask-repair system operating in the field today. Micrion perfected end-point detection of the mask-repair process early in 1984 and can offer this feature to our production customers at any time, unlike manufacturers that only talk about these topics. Users of the 808 are repairing mask plates on a number of printing systems with no problems. Images printed with repairs from the 808 are indistinguishable from unrepaired chrome.

John A. Doherty
Vice President, Marketing
Micrion Corp.
Beverly, Mass.

We want smart power

Correction: *In "New RCA Process Halves Thickness of Gate-Oxide Layer in FETs"* [Electronics, *May 26, 1986, p. 9*], *we reported that "demand for smart power devices is still small" because of a perception that device reliability is a problem. Demand for smart power is high, RCA Corp. says, but demand for logic-level FETs (L^2FETs) has suffered.*

WHERE

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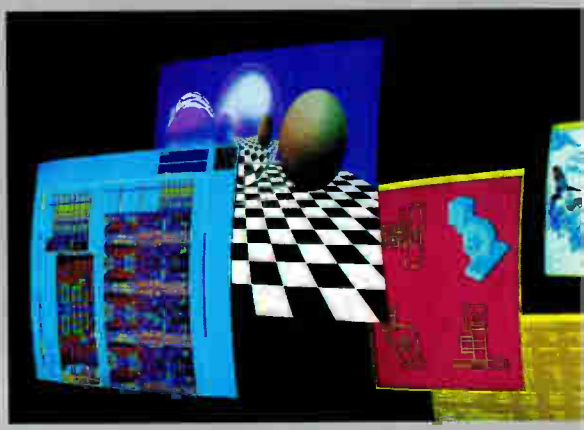

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A different application can run in each window, or within an application, individual windows can be linked to a larger computer. You can also access VAX/VMS™ systems via DECnet-ULTRIX™ networking software, or other vendors' systems via the SNA gateway, X.25 or TCP/IP protocols. And with larger systems handling compute-intensive tasks, the built-in MicroVAX II™ CPU and GPX

VAXstation II/GPX: The first UNIX workstation to put the power of a mainframe in every window.

graphics coprocessor can concentrate on what they do best: delivering exceptional graphics at tremendous speeds.

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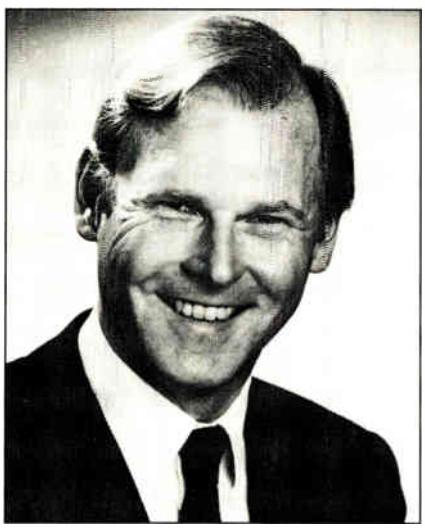
PEOPLE

SODERBLOM RINGS UP TOKEN-RING ROYALTIES



SODERBLOM: Persistence pays off for the inventor of the token ring.

NEW YORK

It was 3 a.m. and Olof Soderblom scurried out of bed to jot down an outline for a network that would come to be known as the token-passing ring. During the 18 years since, Soderblom has scraped and scratched to convince the world that the token ring was his idea.

His story is one of persistence, and for Soderblom, 46, the battle is only now beginning to pay off. With 10 licensees signed up and six more expected to join the fold in the next month or so, Soderblom, whose highest educational degree is a high school diploma, has achieved at least a little vindication.

He says the potential for licensees is limited only by the ability of Willemijn Holding BV to track down the companies that are using and selling token-ring technology worldwide. He shares the patent rights with the Dutch holding company, where he is vice chairman of the board. He estimates that at least 200 companies now use or plan to use the concept. Last year, Willemijn earned about $500,000 in royalties from its various international token-ring patents; this year's royalty income topped the $1 million mark in May.

CLAIMING CREDIT. That money was a long time coming. Svenska Handelsbanken, the Swedish bank where Soderblom was working as a statistical analyst when he developed the token-ring concept, was the first to lay claim to the invention.

Soderblom developed statistical models to help determine the bank's networking requirements. He was part of a group that worked with IBM Corp. and NV Philips on developing an addressed-polling scheme. The network allowed multiple terminals to share a single transmission line, but the computer power required to administer the polling protocols was enormous for the time. Moreover, the network lost much of its transmission time to routine protocol exchanges, and that meant system delays.

Thinking the polling solution inadequate, he was suddenly struck with the idea of having terminals pass a permit—a token—among themselves to use the transmission line to which they were connected in series.

That turned out to be the easy part. Unlike U.S. patent law, an employee in Sweden often has rights to an invention made while working for someone else if it is outside his area of specialization, says George Vande Sande, Soderblom's U.S. patent attorney. Nevertheless, it took almost four years to pry the patent rights from the bank.

ONLY THE START. Once Soderblom had them, however, he found he still hadn't gotten very far. "As a private individual, you can't really support a 26-patent portfolio," he says. While struggling to get approval from the U.S. Patent Office—a drawn-out process that took 13 years to complete—he worked for IBM's Complex Systems Group in Stockholm and set up a pair of air-service companies to help generate extra capital.

By the mid-1970s, IBM was using the token ring in its System 8100, and the company was loath to pay royalties. In 1976, the Patent Office began an interference inquiry to determine whether Soderblom's 1967 patent application had precedence over a patent issued to AT&T Bell Laboratories in 1971. Frustrated, he went back to freelancing and eventually sold his air services business—which held the licensing rights to the token ring—to Willemijn, a specialist in exploiting patent rights.

In 1980, Soderblom got his first license: IBM signed a lump-sum agreement when it appeared that U.S. patent approval was imminent. In 1981, the U.S. granted the patent for which Soderblom first applied in 1968.

Soderblom, who now lives in Surrey, England, with his wife and 12-year-old daughter, travels about 30% of the time, mostly to Europe, the U.S., and Japan. A native of Sweden, he moved to the U.S. in 1953 when his mother, who was in the Swedish foreign service, was sent to Washington.

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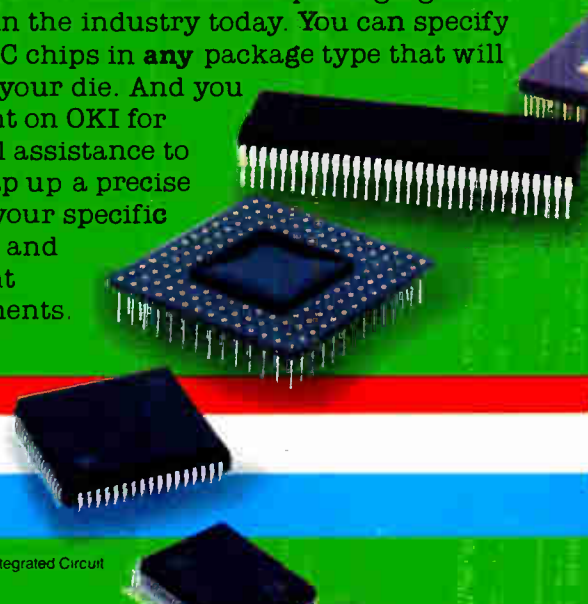

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Soderblom went to high school in Washington, decided he did not want to go to college, and upon graduating headed to Boston in search of a high-technology job. He landed with fledgling Wang Laboratories Inc. in 1958.

He remains something of a free spirit, setting aside about 50 days a year for work as an independent consultant, and he says he misses the nitty-gritty work of designing solutions to technical problems. But Soderblom remains excited by the prospect that token-ring technology could find its way into other applications, such as a possible replacement for the popular RS-232-C interface. "Token-ring would fit the bill," he says, "because its a very simple protocol. If that happens, the licensing opportunities would be limitless." *–Tobias Naegele*

SCHNEIDER'S LETTER GETS A POSITIVE REPLY

POMPANO BEACH, FLA.

Eighteen years ago, Edward J. Schneider wrote a letter to newly formed Computer Products Inc. suggesting that he was the man it needed to get its product ideas into production. Now he is the company's president and chief executive officer.

Schneider, 56, who has a mechanical engineering diploma from the General Motors Institute as well as a BS in mechanical engineering and an MS in production engineering from the University of Michigan, recalls the letter well. "In March 1968, I saw an article about two fellows who had started a new company. One, David C. Yoder, was an engineer. The other, Daniel Wiper, was a marketer. So I wrote them a letter saying, 'Sooner or later you're going to have to make something, and that's my bag.' "

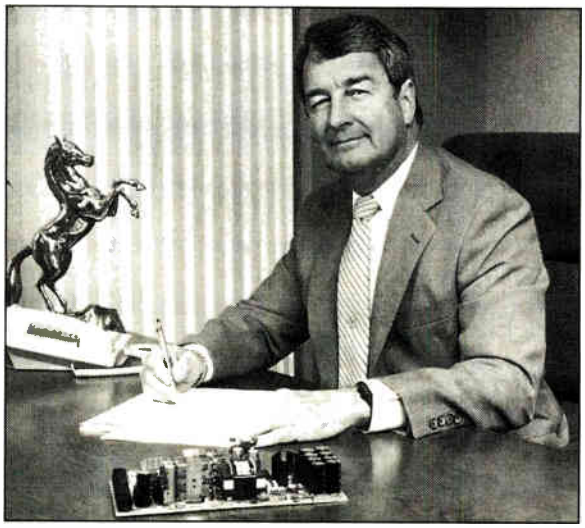
Cofounder Yoder, who preceded Schneider as president and chief executive and is now chairman, says, "He was our first employee in operations, and much of the company's 19-year success can be attributed to his expertise and leadership."

When Schneider wrote his letter, he was working as manufacturing director for the Instruments Division of Electronic Associates Inc., a West Long Branch, N. J., manufacturer of analog computers. Schneider had been there 12 years, starting as a sales engineer. He was promoted to chief of mechanical engineering and director of corporate planning before taking on the division's manufacturing post. Before that, he had served for three years in the Air Force as a research and development contracting officer.

He started at Computer Products in 1968 as director of manufacturing. In 1979, he became director of the Power Conversion Group, which has six manufacturing units in the U. S. plus one in the Caribbean. The group, which makes converters, power supplies, and uninterruptible power supplies, accounts for three quarters of the company's revenue. The Measurement and Control Division, which accounts for the rest, has five manufacturing units that make process control and industrial automation products linking computers to process equipment.

Computer Products today has 2,200 employees and had a net profit of $1.45 million last year on a gross of $88.5 million. But it was a difficult year for the company, says Schneider, because of the discovery of accounting irregularities in the Measurement and Control Division that resulted in a $4 million reduction in the division's revenue from the original results. There is a criminal action pending against the division's former comptroller, says Schneider.

"But that's behind us now and in the hands of the courts," he says, "and we should top the $100 million mark this year. In fact, our Power Conversion Group ranks No. 2 in the market in the country. My goal is to move it to the top spot." *–Howard Wolff*



SCHNEIDER: Computer Products' first operations employee is now president of the 2,200-employee company.

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ELECTRONICS NEWSLETTER

A NEW APPROACH TO DIGITAL SIGNAL PROCESSING TO BE REVEALED BY ZORAN

A new approach to digital signal processing, which promises to perform functions previously attainable only with systems consisting of numerous boards based on general-purpose DSP chips, is said to be scheduled to go into production next week. The manufacturer is Zoran Corp., a Santa Clara, Calif., startup. Industry insiders say the single-chip vector signal processor, or VSP, can perform complex operations such as fast Fourier transforms with only a few instructions and can process a 256-by-256-pixel image at video rates. What's more, the word is that it uses a relatively low integration level: a 2-μm CMOS process for densities of no more than 70,000 transistors. □

U.S. AND JAPAN SET DEADLINE FOR FINAL TERMS ON CHIP DUMPING

Japanese trade authorities have a tense two weeks ahead of them. They must hammer out the details of an agreement by July 26 that will suspend two cases involving the dumping of Japanese erasable programmable read-only memories and 256-K dynamic random-access memories in the U. S. semiconductor market. The Commerce Department and the U. S. Trade Representative's office say they are close to agreement on many issues with the Japanese, but that they are still far apart on U. S. access to the Japanese semiconductor market and regulations to prevent future dumping. □

ESDI TO BE CONSIDERED FOR INDUSTRY DRIVE STANDARD

After more than two years of independent development, ESDI, the Enhanced Small Disk Interface for 5¼-in. Winchester drives, has achieved recognition as a possible industry standard. Next week's meeting of the ESDI steering committee in Irvine, Calif., will serve as an official working group for American National Standards Institute Committee X3T9.3 on device interfaces. Control Data, Electronic Processors, Fujitsu America, Maxtor, Priam, and Western Digital are the first members of the ESDI committee; others will be recruited in Irvine. One issue to be considered: upgrading the interface from 10 to 20 Mb/s. □

MACHINE-VISION STANDARDS COULD APPEAR NEXT YEAR

The Automated Vision Association, Ann Arbor, Mich., expects to start reviewing first drafts of machine-vision standards this summer—which is good news for users frustrated by the myriad nonstandard and expensive custom approaches offered by some 200 vendors. Five subcommittees are working on the drafts. Final standards could be ready as soon as mid-1987, says James C. Solinsky, the Rockwell International official who heads the committee overseeing the work. □

THE FIRST CONDUCTIVE, TRANSPARENT THIN FILM IS DEMONSTRATED

An organic thin film said to be the first transparent polymer capable of conducting electricity has been demonstrated at Honeywell Inc.'s Physical Sciences Center in Bloomington, Minn. One possible use is as a replacement for inorganic transparent conductors used in liquid-crystal displays and photovoltaic cells. Made from the polymer polydiiodocarbazole doped with bromine, the film can easily be formed into layers 1 to 30 μm thick with standard techniques such as spin coating, Honeywell says. The material's conductivity levels, ranging from 0.1 to 1.0 Ω^{-1} cm^{-1}, can't match the 10,000-Ω^{-1} cm^{-1} levels of conventional, inorganic transparent films made from combinations of tin, indium, cadmium, and zinc. But Honeywell says its material is cheaper, and it expects conductivity to improve significantly. □

ELECTRONICS NEWSLETTER

TANDON ABOUT TO INTRODUCE ITS OWN PERSONAL COMPUTER IN THE U. S.

This week should see the long-predicted U. S. introduction of Tandon Corp.'s namebrand personal computer, more than a year after the company hired away some of the manufacturing and marketing talent responsible for IBM Corp.'s Personal Computer. In the interim, Tandon has become a supplier to Xerox Data Systems, Tandem, and Tandy (Radio Shack). The computer is virtually the same machine that Tandon introduced in Europe last autumn but with some slightly different features that the company will bill as improvements. □

OLD RIVALS TI AND HONEYWELL UNITE TO BID FOR GaAs LINE

The Pentagon's latest plans to set up a third pilot production line for fast gallium arsenide chips is resulting in a partnership between two military semiconductor rivals. Texas Instruments Inc. and Honeywell Inc. have submitted one of a handful of bids that are expected. The Defense Advanced Research Projects Agency wants the production line for fast memories and logic necessary to support the 200-MHz 32-bit microprocessors being developed for the Strategic Defense Initiative. "Everything is leading to the GaAs being used on the advanced on-board signal processor [module] of SDI," says Sven A. Rossild, a deputy director in Darpa's Defense Sciences Office. Bidding will end next week, and Rossild hopes for an award by the fall. □

FAIRCHILD SIGNS HITACHI TO MAKE FACT CMOS LOGIC FAMILY

Gaining access and credibility in the Japanese market, Fairchild Semiconductor Corp. has signed a five-year agreement with Hitachi Ltd. under which Hitachi will become the first alternate-source supplier of the Fairchild Advanced CMOS Technology (FACT) family of digital logic circuits. Hitachi will produce and market FACT devices and use the trademark, and both companies will have access to new devices developed for the family. FACT devices are made in a silicon-gate p-well process with a 1.3-μm channel length and double-level metal. Fairchild is producing the family at its South Portland, Maine, facility, and will start manufacturing at its new plant in Nagasaki, Japan, in the first half of 1987. Hitachi expects to have first samples of its FACT products by the end of this year, and it plans to go into production in the first quarter of 1987. □

RAYTHEON GETS RIGHTS TO BIT1 BIPOLAR PROCESS

Raytheon Semiconductor Corp. has locked up rights to use the high-speed low-power bipolar process from Bipolar Integrated Technology Inc., a Beaverton, Ore., startup, in gate arrays and standard cells. Raytheon, of Mountain View, Calif., whose parent corporation has invested in the company, will use the BIT1 process [*Electronics*, April 7, 1986, p. 35] in a series of 3,500- to 5,000-gate products to be announced late this year. The emitter-coupled-logic process is specified at 300 ps for unloaded gate delays and toggle frequencies of 600 MHz, at 300 mW power dissipation. This yields a speed/power ratio of 300 pJ. □

NORTHWEST SIGNS TO MAKE SOFTWARE TOOLS FOR INTEL

Intel Corp. will integrate a family of software tools and debuggers from Northwest Instruments Systems Inc. into its line of microcomputer development tools. Under a two-year $15-million agreement, Northwest, Hillsboro, Ore., will engineer and manufacture Intel-specified instruments that will be marketed by Intel's development system operation, also in Hillsboro. □

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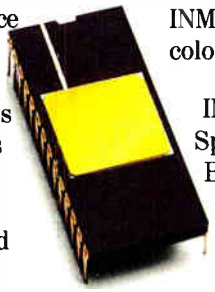

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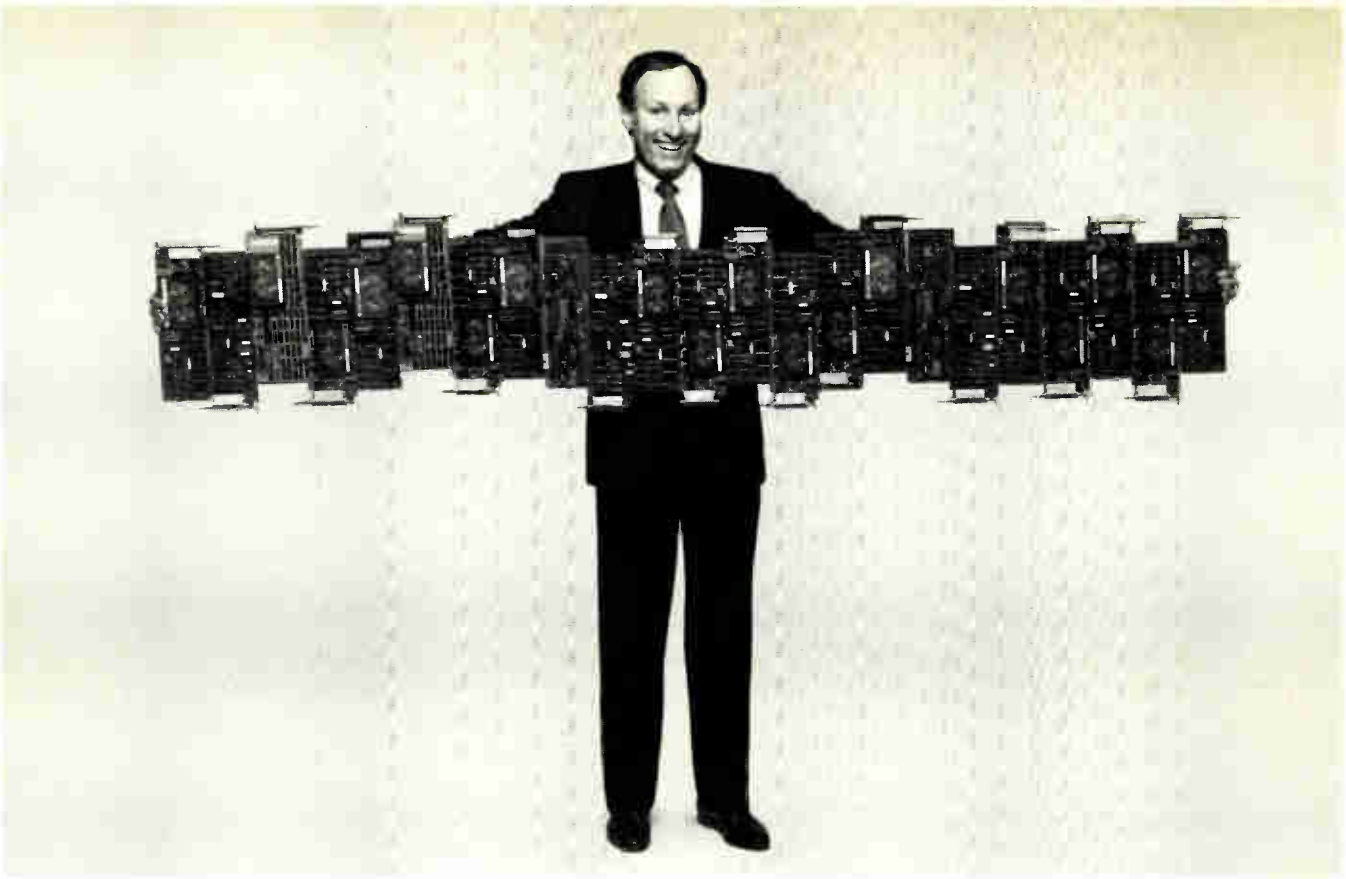

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General Purpose	DT2806	2495	to 80	12	20	to 24	12	to 72	Yes	DT757
General Purpose	DT2808	495	16	10	3.3	2	8	16	Yes	DT707
Low Cost	DT2814	395	16	12	25	–	–	–	Yes	DT757
Low Cost	DT2815	499	–	–	–	8	12	–	–	DT757
Low Cost	DT2817	199	–	–	–	–	–	32	–	DT758
High Speed	DT2821	1345-2495	4-16	12-16	50-130	2	12	16	Yes	DT707

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PRODUCTS NEWSLETTER

ROCKWELL TO OFFER CMOS/SILICON-ON-SAPPHIRE GATE ARRAYS

Gate arrays to be fabricated in CMOS/silicon-on-sapphire technology will soon emerge from Rockwell International Corp.'s Electronics Operation. The new arrays, which will be built in the Anaheim, Calif., division's 1.25-μm process, feature built-in self-test technology from Control Data Corp., Minneapolis. The first array will offer about 6,500 gates. Design support is available from Control Data's Technology Application Center in Plymouth, Minn. Prototypes can be delivered in one month; pricing has not been set. □

BBN IS MARKETING AN ENHANCED VERSION OF ITS PARALLEL COMPUTER

Bolt Beranek & Newman Inc. has enhanced its Butterfly parallel-processing computer and has set up a separate subsidiary to market it. The system can now be fitted with up to 256 nodes that are built around the 68020 microprocessor and 68881 floating-point coprocessor. Each node can now have 4 megabytes of memory and operates at 1 million instructions/s. A four-processor starter system is available from BBN Advanced Computers Inc. for less than $40,000; additional 68000-based nodes are $6,500 each and the new 68020-based nodes are $9,500 each. The Cambridge, Mass., company says a typical 32-node system costs $375,000. A new Fortran 77 compiler is $9,000. □

CHIP LETS SLOWER PERIPHERALS WORK WITH THE NEW, FASTER Z80

A CMOS chip from Texas Arrays Inc. will allow existing 4-MHz peripheral circuits to be used with new 8-MHz versions of Zilog Inc.'s Z80 microprocessor. The 20-pin TA84HC04 emulator chip operates during input/output cycles, issuing wait states to the processor. Slowing down the microprocessor only during the I/O operations lets the Z80 run at full speed 95% to 98% of the time. In lots of 100, the TA84HC04 costs $6.15 each. The circuit is also available in the Carrollton, Texas, company's 3-μm CMOS standard-cell and gate-array libraries. □

DATA BASE CAN HANDLE BOTH PICTURES AND TEXT

Computer Corp. of America is unveiling two products that let its model 204 mainframe data-base-management system handle both pictures and text along with traditional data. The Picture/204 makes it possible to store digitized pictures in the Cambridge, Mass., company's model 204 and to retrieve them from the system, using a personal computer attached to the mainframe. CCA's new Text/204 allows documents to be integrated with the model 204. Text/204 will be available in December for $47,000. Picture/204, which will ship in October, sells for $30,000; the color version of the imaging software is $950. □

COMPUTER*THOUGHT RELEASES NEW VERSION OF ITS EXPERT SYSTEM

Computer*Thought Inc. is releasing a new version of its OPS5+ expert-system development software, following a legal battle with former employees over ownership of the product. The OPS5+ package, which builds an expert system with up to 1,500 rules, was previously marketed by employees who left the Plano, Texas, company and formed Artelligence Inc. OPS5+ is now the exclusive property of Computer*Thought, the company says, and the debugged Version 3.0 is priced at $1,850. OPS5+ is available for the IBM Corp. Personal Computer and the Apple Computer Inc. Macintosh. Versions for Apollo Computer Inc. and Sun Microsystems Inc. work stations will come out in two months. □

PRODUCTS NEWSLETTER

ANALOGIC OFFERS AN INTELLIGENT PROCESS MONITOR

Analogic Corp. is applying its expertise in analog-to-digital converters to a line of intelligent process monitors and controllers for industrial and factory applications. The Danvers, Mass., company's new microprocessor-based Control Master can accept two different types of input signals—current and thermocouple—and provides four programmable digital outputs for controls or alarms. Control Master, the first product in the new line, also includes a 17-bit ADC that runs at 20 conversions/s, 10 times faster than competing products. Control Master will sell for $375 when available next month. □

NEWBURY DATA BUILDS 51-MEGABYTE 3½-IN. WINCHESTER DRIVE

A 3½-in. Winchester disk drive with a 51-megabyte capacity may soon appear in equipment. Newbury Data Inc.'s drive is under evaluation by several major U. S. and European equipment manufacturers. The four-platter Penny drive, announced some two years ago by the Hermosa Beach, Calif., company, was delayed by development problems. It now boasts an average access time of 40 ms, transfers data at 5 Mb/s, weighs 1.65 lb, and consumes 12 W. Newbury Data's parent, Newbury Data Recording Ltd. of the UK, produces the drive. The price in large quantities is less than $1,000 per unit. □

WESTERN DIGITAL'S HARD-DISK CONTROLLER STORES MORE BITS

Western Digital Corp.'s first hard-disk controller using the run-length-limited (RLL) encoding format can record up to 60% more bits than the widely used modified frequency modulation. Moreover, the WD1002-27X transfers data 50% faster than previously possible, says the Irvine, Calif., company. The controller incorporates two proprietary chips: Western Digital's standard WD1010 controller and the new hard-disk RLL device, which integrates a 56-bit error-correction code and support for 7.5-MHz data transfers. Samples of the WD1002-27X will be out next month. Specific pricing varies, but the controller initially will cost more than products now on the market. □

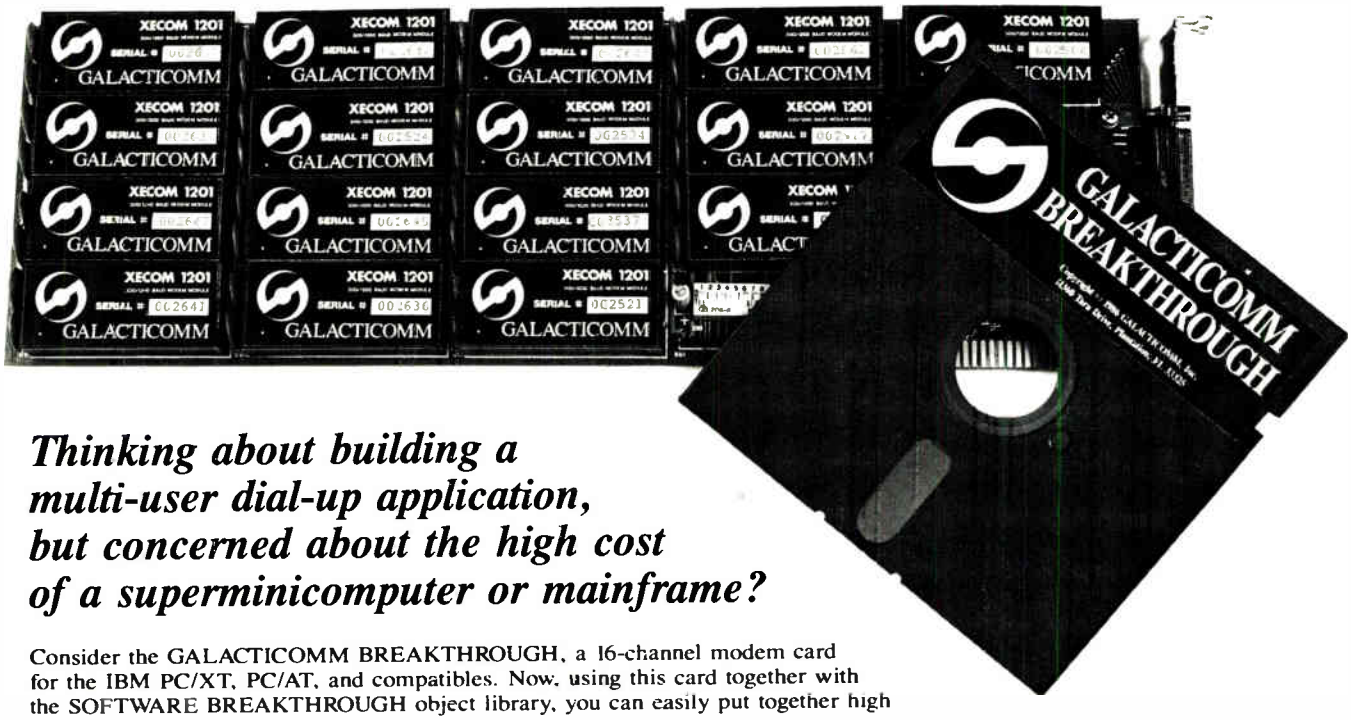
ROCKWELL SHIPS SINGLE-CHIP FACSIMILE MODEM . . .

Rockwell International Corp.'s Semiconductor Products Division is shipping samples of a single-chip facsimile modem that transmits data over the public switched telephone network at 2,400 b/s. The R24MFX will cut the size and cost of facsimile equipment and could give a shot in the arm to the emerging market for personal facsimile machines. Optimized for use in compact Group 3 facsimile machines, the chip has two interfaces—a parallel microprocessor bus interface and an RS-232-C serial port. In 1,000-piece lots, the R24MFX sells for $40 each. The Newport Beach, Calif., division will begin volume shipments in August. □

. . . WHILE AN NEC MEMORY WILL LEAD TO COLOR FACSIMILE

NEC Corp. has boosted the size of its byte-wide dual-port memories fivefold, to 5,048 bytes, which should lead shortly to commercial color facsimile systems. Applications for the μPD42505C first-in first-out buffer also include graphics, data compression and expansion, and buffering for the transmission of data between two systems operating at different speeds. The buffer is suitable for use in Group 3 and 4 facsimile systems, multifunction copiers using digital imaging, image scanners, and other digital systems. The sample price for devices with 50-ns write/read cycle times is $42.68 in Japan. □

BREAKTHROUGH



Thinking about building a multi-user dial-up application, but concerned about the high cost of a superminicomputer or mainframe?

Consider the GALACTICOMM BREAKTHROUGH, a 16-channel modem card for the IBM PC/XT, PC/AT, and compatibles. Now, using this card together with the SOFTWARE BREAKTHROUGH object library, you can easily put together high performance multi-user applications at minimum cost.

The software is the key

- Special interrupt-driven I/O method eliminates 92% of the interrupt overhead of conventional designs
- DOS-bypass subroutines to access all modem functions (e.g. accept a call, place a call, send/receive ASCII data, send/receive DTMF data, check modem status, set baud rate and parity, and much more)
- Assembly language automatic pending-input channel-scanning and circular/linear buffer management
- Supports up to 64 channels (4 BREAKTHROUGH circuit cards) simultaneously at 1200 baud on the PC/AT
- Fully PC-DOS compatible, bindings exist for most popular languages, not copy-protected, no royalties

The hardware is incredible

- The XECOM 1201 is the modem module described in Steve Ciarcia's November 1985 Circuit Cellar column
- Each modem module is complete, USART to DAA, 212A compatible, FCC registered and ready to run
- Adapters available for direct connection via 16 RJ-11's, or a single RJ-21X mass telephone connector
- Port stacking technique allows direct addressing of each modem while consuming only 2 PC ports per card
- DIP-switch selectable port-group addressing on any even boundary in the range from 200H to 3FEH

The applications are limitless

- Multi-user bulletin boards and EMAIL systems
- Multi-user real-time teleconferencing
- Multi-user customer order entry networks
- Multi-user online expert systems
- Multi-user classified advertising services
- Multi-user database search & retrieval systems
- Multi-user interactive adventure games
- Multi-user sales information inquiry systems
- Multi-user online educational services
- Multi-user "simulated CB-radio" networks

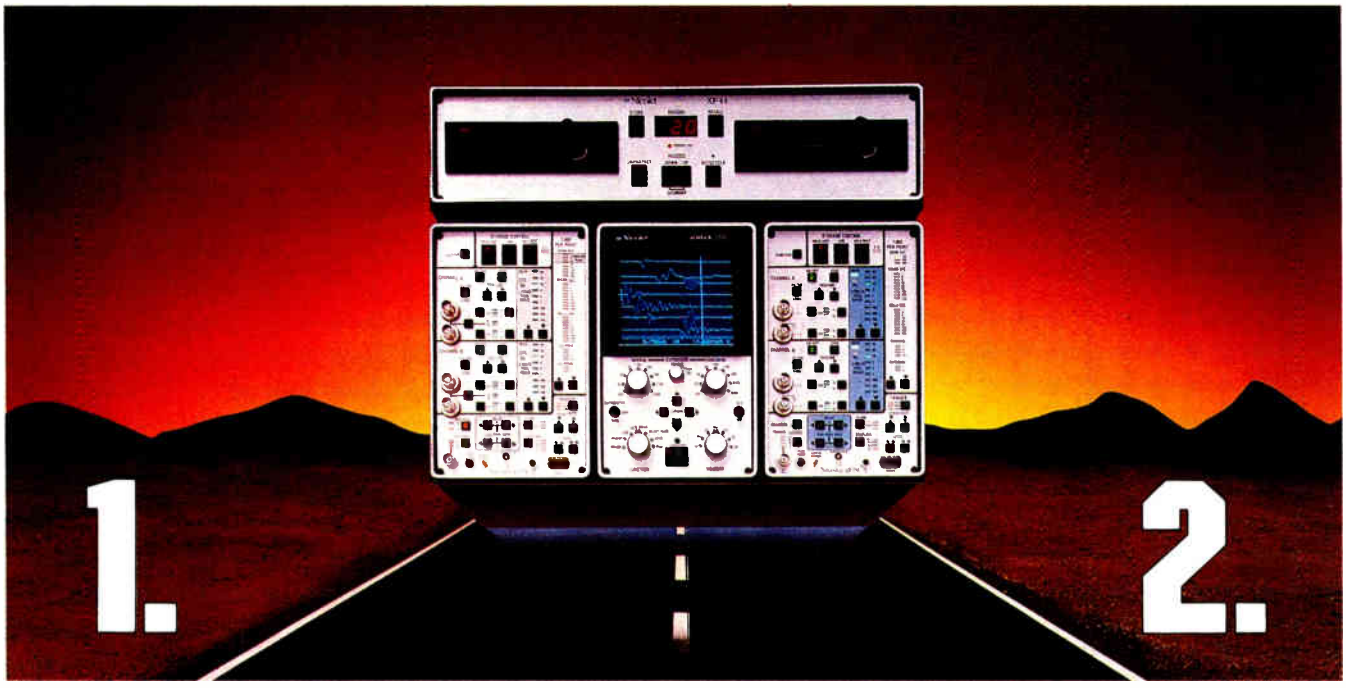
For some free sample time on a PC/XT running the GALACTICOMM BREAKTHROUGH, dial (305) 922-3901 during business hours. Have your modem ready to go online in originate mode at 300 or 1200 baud: 7 data bits, even parity, 1 stop bit.

GALACTICOMM

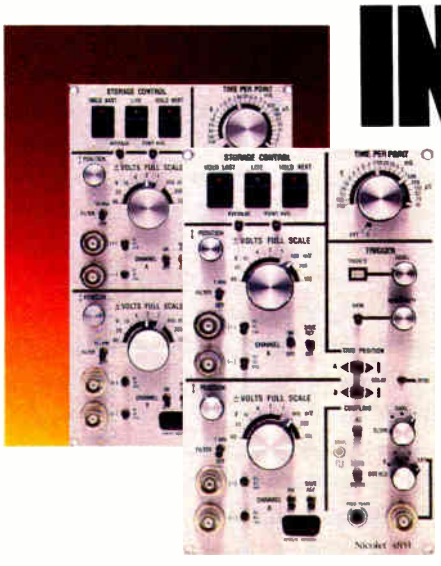
GALACTICOMM, Inc., 11360 Tara Drive, Plantation, FL 33325 (305) 472-9560

Circle 25 on reader service card

THE FIRST NAME IN DIGITAL SCOPES



TWO DIGITAL SCOPES IN ONE.



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Circle 26 on reader service card

Electronics

CONTROL DATA LAUNCHES CMOS/SOS SPACE COMPUTER

1750A MACHINE BEATS VHSIC-PROGRAM PROCESSORS TO MARKET

MINNEAPOLIS

By rolling out a radiation-hardened, spaceworthy computer based on a 2-μm CMOS/silicon-on-sapphire process, Control Data Corp. is hoping to steal a march on contractors involved in the Defense Department's Very High Speed Integrated Circuits program.

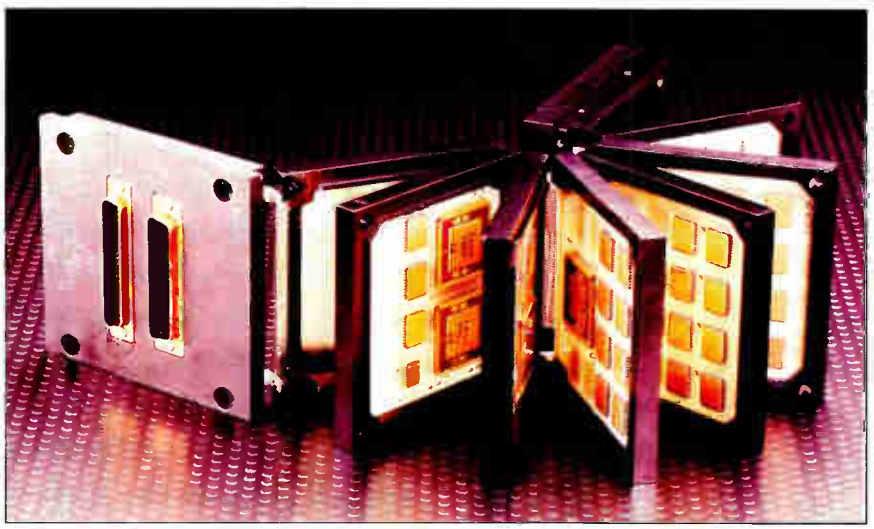
The Minneapolis company this week will unveil its Spacecraft Control Processor, which implements MIL-STD-1750A, the Air Force's instruction-set architecture for 16-bit computers. Set to be ready in next year's third quarter, the SCP could offer a substantial improvement over today's state-of-the-art space machines. At the same time, it could beat to market by two years the first 1750A space computers built in rad-hard 1.25-μm Phase 1 VHSIC technology.

There will be a market for the SCP, predicts Darrell J. Putnam, a member of the professional staff in digital design at the Missile Systems Division for Martin Marietta Orlando Aerospace, Orlando, Fla. "The VHSIC stuff will be a lot better when it does come out, but Control Data is about two years ahead, as far as I can see," Putnam says.

SDI PROOF. In particular, Putnam says, the Control Data machine could play a major role in experimental systems that are aimed at early proof of concepts to be used in the DOD's Strategic Defense Initiative. Such systems might be launched as early as 1988, Putnam says. By contrast, computers built under a year-old DOD program to produce rad-hard 1.25-μm VHSIC-class 1750A space computers are not due to emerge until mid to late 1989 (see "VHSIC computer tests begin this fall," p. 28).

The SCP is actually the first of a new family of planned space-computer modules from Control Data. It will run on a new interconnection platform that Control Data designed to meet the needs of future space programs, such as SDI, which are expected to increasingly require multiple processors on board.

Future Control Data machines will be based on VHSIC-class 1.25-μm technology, the company says. But by establishing a presence and a reputation based on 2-μm technology, the company hopes to get a jump on what could be a $4 billion to $5 billion market for high-performance space computers by the mid-1990s, says Terry Petrzelka, vice president of Program Planning and Development for Control Data's Government Systems Group. Control Data also plans to adapt the SCP technology next year for use in military avionics.



RAD HARD. Control Data Corp.'s Spacecraft Control Processor, with its 2-μm CMOS/SOS technology, will be ready two years before machines based on 1.25-μm VHSIC chips.

Using an 8-MHz clock, the SCP's two-chip central processing unit will execute about 1.75 million instructions per second using a standard floating-point Digital Avionics Instruction Set mix, says Andrew Wardrop, Control Data's product chief engineer for space engineering. Even after it has received its full rated radiation dosage of 200,000 rads, it will still hit 1.75 mips. The addition of single-bit-error correction and double-bit-error detection for memory will bring SCP performance down to 1.25 mips in a space-configured system, Wardrop says.

That's well below the performance of the 3- to 4-mips single-chip processors expected from VHSIC-based space machines. But by offering the SCP in an optional dual-processor version, Control Data figures to boost SCP space-system throughput to 2.5 mips, or more than twice the speed of today's standard space computers, executives say.

Control Data has no plans to fabricate the SCP chip set itself but will instead rely initially on CMOS/SOS chips supplied by Rockwell International Corp., says Curtis L. (Pete) Nelson, the Government Systems Group's manager of new business development. Control Data is also working with RCA Corp. as a second potential supplier, he says.

FIRST PASS. Working versions of the custom two-chip CPU set, each integrating about 10,000 gates, were obtained on the first processing pass, Nelson says. Three simpler circuits—a memory-management chip, a memory interface device, and an input/output chip—are under design using a semicustom gate-array approach. The firm expects to have working versions of all five chips by next year's first quarter.

Engineering units of the SCP should be available in the third quarter of 1987, says Nelson. A brassboard version is scheduled to undergo Air Force 1750A certification tests at Wright-Patterson Air Force Base next month.

The SCP will feature two independent memory-access buses for improved reliability. To be housed on boards measuring 3½ by 3¼ in., a minimum three-board configuration—one board each for CPU, 64-K 16-bit words of error-protect-

VHSIC COMPUTER TESTS BEGIN THIS FALL

While Control Data focuses on the near-term market for space computers built with devices featuring minimum 2-μm geometries, at least four contractors are already hard at work on radiation-hardened space computers made with chips using more advanced 1.25-μm technology produced under Phase 1 of the Very High Speed Integrated Circuits program.

The work is being sponsored by the U.S. Department of Defense under a project known as the Generic VHSIC Spaceborne Computer (GVSC) program. Initial contracts awarded last July went to Harris, Honeywell, IBM, and RCA.

Under the first phase of the effort—to be completed with testing in September—each of the four is to develop a space processor design based on the Air Force MIL-STD-1750A architecture. The contractors also will deliver several lots of test chips and wafers that will undergo government radiation testing, says Capt. Russell R. Herndon, GVSC program manager at Kirtland Air Force Base in New Mexico. Harris, Honeywell, and IBM are working in bulk CMOS processes, and RCA plans to implement its design in its CMOS/silicon-on-sapphire technology.

The radiation data accumulated on each contractor's process under the initial phase will be used in selecting one or two of the four contractors for the second phase of work, Herndon says. Phase 2 aims to produce working space-qualifiable hardware using 1.25-μm technology 30 months after the contracts are let. "We're hoping to start the second phase during the first part of 1987," Herndon says.

GVSC goals include single-processor performance in the range of 3 million to 4 million instructions/s. Herndon declines to reveal GVSC targets for radiation hardness, but the program is believed to be aimed at systems capable of withstanding a total dose of up to 1 Mrad.

VHSIC-class 1750A chips produced outside the GVSC program might also turn out to be suitable for use in space. Texas Instruments Inc., for one, has already produced working 1750A processor chips built in 1.25-μm Schottky-transistor logic.

The Dallas company's single-chip CPU is aimed at avionics applications and has not been tested for radiation tolerance, says Dennis Best, VHSIC program manager for TI's Defense Systems and Electronics Group. But Best notes that STL is inherently rad-hard, and tests run on other devices built with the technology have shown total dose tolerance levels beyond 1 Mrad. *–W. R. I.*

ed memory, and I/O—will cost about $350,000 for an engineering unit. A maximum fully space qualified 12-board system using two CPUs and eight cards of random-access memory totaling a 512-K words will go for about $1.25 million. Control Data says a maximally configured system will weigh about 7 lb, require 10 W of regulated power, and occupy about 120 in.^{3}. For applications that can tolerate 10% to 20% lower performances, an SCP could also be equipped with additional boards, bringing maximum addressable memory up to 1 million words, Wardrop says.

Both logic-design techniques and the inherent radiation hardness of CMOS/SOS are responsible for SCP's 200,000-rad rating, CDC says. Currently available memory devices can't provide equivalent radiation hardness at the 64-K densities and 45-ns access times needed by the SCP. But such chips will be available by the time the system is ready to fly, CDC officials expect.

BEYOND CONTROL. In the near term, Control Data says the SCP will serve as a replacement for its current-generation 10-μm p-MOS-based 469R^2 space computer used for spacecraft navigation and control. For applications beyond control, a second SCP aboard a spacecraft could also be tied in using the Control Data interconnection scheme for handling payload data-processing tasks, and also could work with other specialized processors.

"Our goal is to build a family of products, using the 1750A [SCP] as both the control processor and as a near-term data processor, and then replace it with a larger 32-bit data processor in the future," says Nelson. Beyond that, officials are mum on plans for the company's new space-computer architecture, except to say that future announcements will include a new specialized signal-processing module for crunching satellite-sensor data.

Space-industry officials give Control Data high marks on its game plan. "It looks like they've really put a lot of thought and homework into their architectural design to address a lot of the issues unique to flying computers in space," observes Lt. Col. Ralph Gajewski, SDI manager of signal-processing technology. The SCP is "a start in the right direction," Gajewski says. "You're always ahead by having working hardware."

But to be successful in the long term, the SDI official warns that CDC must keep moving. "Space-computer users are pretty fickle, and they always want the latest and the best," Gajewski notes. "Control Data will have to follow through on their product-improvement programs and be able to adapt to higher-performance circuitry as it becomes available." *–Wesley R. Iversen*

RESEARCH & DEVELOPMENT

PULLING SPACE R&D DOWN TO EARTH

LOS ANGELES

The wealth of technology generated at the nation's heavyweight research centers offers a tempting prospect for industry, particularly smaller companies with limited budgets. But moving that technology from the lab into a commercial-product environment has always proved a difficult task.

Now a nonprofit Los Angeles group called Rimtech (short for Research Institute for the Management of Technology) is launching a new drive to forge a link between small local companies and scientists from the National Aeronautics and Space Administration's Jet Propulsion Laboratories in Pasadena, Calif. Four companies have already signed up in the Rimtech-JPL/NASA Product Development Program since its start earlier this year, and the group plan a stepped-up effort to sell the program to others at a public briefing scheduled for July 7 in which government and industry luminaries extolled the project's virtues.

Prior attempts to get government researchers and private industry executives to join hands have had little success because they've been too limited in scope. In 1980, the federal Technology Innovation Act established the Center for the Utilization of Federal Technology, but since then there have been only a few successful examples of technology transfer, next to none of which has been electronics-related. Other programs went under for various reasons. "Many of these failed in the past because they were some researcher's pet project in search of a market," says Rimtech president Steven M. Panzer. He and other officials make it clear that the developers of valuable research have historically not found success in their attempts to distribute their findings into

the hands of commercial users.

Instead, they say, the impetus for successful transfer must come from individual companies, especially those with strong entrepreneurial spirit and a product and market in mind. What these companies lack is specific technology assistance to get the job done, and that's where Rimtech is seeking to make its presence known—as a technology broker of sorts. Rimtech officials will help companies identify useful technology generated within JPL, and then help arrange to channel that technical know-how into the company's hands. This can involve large or small group presentations, one-on-one engineering laboratory demonstrations, a transfer of documents, or a careful orchestration of any of these methods.

The contract is then sealed with a $25,000 annual fee (regarded as a bargain by all hands, considering time and administration costs alone) and an agreement on a schedule of specific items to be delivered. Rimtech closely monitors the accompanying timetable.

TYPICAL CUSTOMER. Because it carries little risk, Rimtech officials expect the plan to draw widespread interest. Emulex Corp.'s reaction was typical of the four companies to get involved so far. The Costa Mesa, Calif., maker of data-storage subsystems and peripherals quickly opted to take part after an initial presentation on data processing and a follow-up talk.

Specifically, Emulex is looking for advanced work on data compression and encryption, a field in which JPL is an acknowledged leader because of its accomplishments in transmitting data to Earth from unmanned probes in deep space. "This could have real downstream impact for us," predicts Emulex chairman Fred B. Cox. Optical-memory research is another hot topic, he adds, but one that Emulex, with only about $100 million in sales, cannot pursue on its own. "We can't afford to look that far out, so we need to take advantage of [JPL's] forward thinking."

Cox maintains that without a player such as Rimtech organizing the transfer, JPL's technology would be lost to Emulex and others like it. But industry observers familiar with the fate of earlier efforts to merge the labs with industry are not yet convinced this one will succeed. "It's no easy task to take sophisticated technology and convert it to the real electronics world," says Matt Crugnale, a Mountain View, Calif., marketing consultant. For one thing, he says, such an exchange must emphasize verbal communications, "and engineers are terrible at communications."

Moreover, getting the right information often requires more time than either side can devote to digging out facts from records and developing them for a specific purpose. And prickly professional pride can raise a barrier that may go unnoticed until it's too late, Crugnale says. "Lack of mutual respect at the technical level is one of the elements that makes [transfers] most difficult."

Rimtech officials admit success will not come easily. The group notes in its prospectus that "management practices and guidelines for technology transfer—ownership, decision-making, and publication rights—have not been studied, developed, or disseminated in depth." No systematic approach has emerged and techniques vary widely, it continues. But the officials point out that initial responses are encouraging.

JPL is pushing this sharing program and investing some $200,000, in part because getting more deeply involved with industry presents a way to keep its engineering and scientific teams intact in the face of NASA budget uncertainties. Even though no blame was laid on JPL for the Challenger disaster—the Pasadena lab has been very successful with its unmanned missions—a planned schedule of projects is on hold because there are no means to launch. *–Larry Waller*

NETWORKING

LOW-SPEED LANs CHECK IN AT $100 PER CONNECTION

MOUNTAIN VIEW, CALIF.

Just as low-cost local-area-network solutions are beginning to emerge from the haze of protocol wars and competing access technologies, a new class of software-based LANs is appearing to make the job even harder for mainstream networking companies.

The new LANs are slow (115 kb/s and under), they accommodate only a few users, and, because they run under the MS-DOS operating system, they are limited to use with IBM Corp. Personal Computers, PC ATs, and compatibles. But they support the kind of file-transfer and resource-sharing functions that make up the bulk of networking requirements for small installations.

Most important, these new LANs are priced at the magic figure of around $100 per connection. The cheapest mainstream LANs still cost $750 or more per connection, and even the Starlan, backed by AT&T Co. and billed as a low-cost approach, is priced at just less than $600 [*Electronics*, June 9, 1986, p. 20].

"Two thirds of all PCs are in small clusters of two to nine units and have no need for Ethernet or other high-speed, coaxial-cable-based LANs," says Carrel W. Ewing, president of Server Technology Inc. of Sunnyvale, Calif., one of the first companies to market a low-cost network. The main use for LANs in such small clusters is the sharing of printers, backup devices, hard disks, and modems.

"There are a lot of people out there who just want basic connectivity," points out Louise Herndon Wells, an analyst with Dataquest. "Why spend $1,000 so that a PC can share a $500 drive?"

Server Technology, like others in the field, substitutes twisted-pair telephone wiring for coax and links its EasyLAN to a computer through an RS-232-C connector and the serial port, thus eliminating the need for a separate network card. Network control is performed by memory-resident software.

EasyLAN is priced at $180 for the first two connections and $109 for each additional node. But because it is a series of point-to-point connections, it requires the server to have a separate serial port for each node, and these ports add to the overall cost of the network.

UNDER $100? The first true $99 LAN may be a new offering from Applied Knowledge Group Inc. of Mountain View, whose Knowledge Network runs in any configuration—bus, star, tree, or ring—without a server. Stations plug into a simple RJ-11 bus box.

Knowledge Network incorporates a simple form of the Ethernet contention

EWING: Server Technology's president says that two thirds of all PCs are in small clusters and have no need for high-speed LANs.

scheme, carrier-sense multiple-access with collision detection. Remote disk drives and peripherals are identified as virtual devices, and users access them with standard DOS commands. Simple error correction is performed with cyclic redundancy checks, and users may protect or hide files.

Other low-cost LANs that operate as a collection of point-to-point connections from a central server include offerings from Avatar Technologies Inc. of Hopkinton, Mass.; The Software Link Inc. of Atlanta; IDEAssociates of Billerica, Mass.; and Digital Products Inc. of Watertown, Mass. Avatar charges $895 for an eight-user system. Digital Products sells its peripherals-sharing subLAN for about $150 per connection and a version that adds file sharing for about $230. IDEAssociates' IDEAshare is priced at $595 for two users, and LANLink from Software Link at $695 for four users. Cables, in all cases, are extra.

Because they operate with a central controller, these LANs avoid the problem of network contention. But they must accept a star configuration with a multiport server that runs at all times. The servers range in complexity from Easynet's, which is a nondedicated PC with multiple serial ports, to Avatar's Alliance, a separate box that employs an 8-bit Hitachi Ltd. 64180 processor plus a gate array wired as a 1-Mb/s switch.

COLLISIONS. Knowledge Network achieves CSMA/CD operation through a simple switch in the RS-232-C connector that echoes all transmissions back to the sender. If two stations attempt to send at once, the voltage on the circuit will not support the required 7-V peak-to-peak level, and the echo will be squelched. Both stations will then wait for a random time before trying to retransmit.

The speed of the networks ranges from 19.2 kb/s for subLAN and Easy-LAN implemented on an IBM PC, to 57 kb/s for Knowledge Network and Easy-LAN on a PC AT, to 115 kb/s for Alliance and the Software Link's LANLink. Alliance accommodates the most users, 20, though a 31-user Knowledge Network is promised for the fall.

The LANs are all extendable. Knowledge Network, for instance, can use a modem as one of its nodes and through it dial up other network clusters. LANlink, which has eight satellite stations per cluster, allows the satellites themselves to become servers for additional clusters; Software Link says it operates a 42-station system of its own. Avatar's Alliance can also be daisy-chained.

Easynet can also make its node connections through private-branch-exchange switches, increasing the potential number of nodes. Server Technology expects to announce an agreement with a PBX maker within 60 days.

Because the low-cost nets were developed without regard for the transmission protocols being developed by the International Organization for Standardization, they do not interface easily with Ethernet or IBM's Token-Ring Network and PC-Net. Alliance and the Knowledge Network, however, could be linked to such nets by attaching a network controller. And Avatar plans a 3270 link for Alliance. *–Clifford Barney*

SEMICUSTOM ICs

SPEEDING UP PLACEMENT AND ROUTING

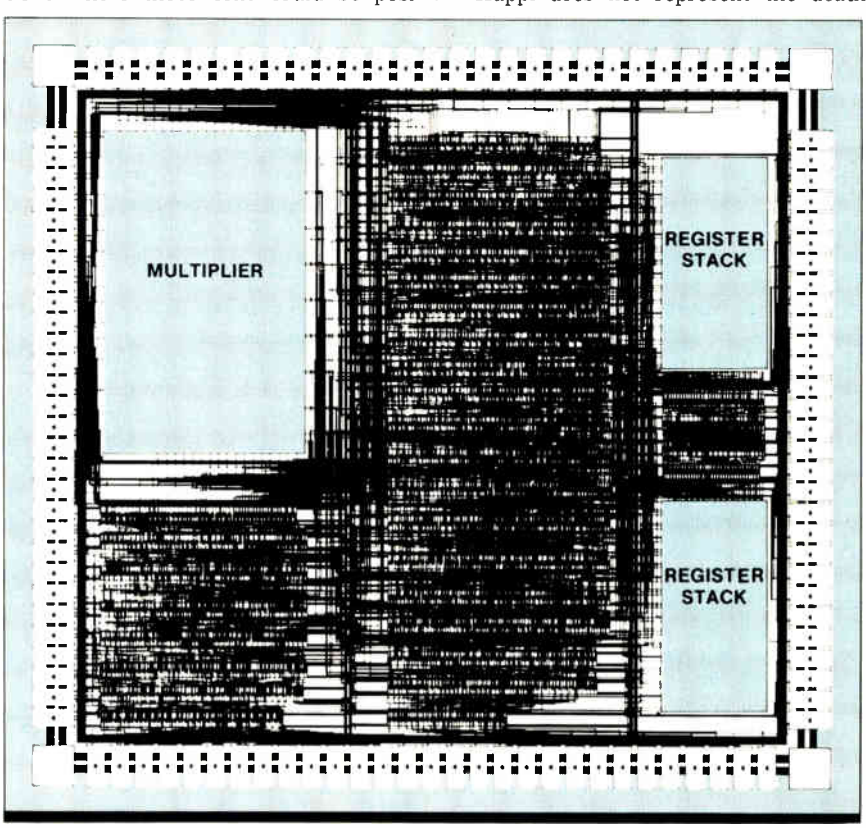
MOORESTOWN, N. J.

RCA Corp. is continuing its drive to become a dominant force in application-specific integrated circuits with a new design tool that can place and route large numbers of standard cells and larger macrocells while automatically designing the chip's power bus. Dubbed Happi, for Hierarchical Automatic Partition Placement Interconnect, the software produces layouts for RCA's double-metal single-polysilicon process and can be adjusted for different geometries.

Happi is embedded into Vital, the system RCA's Solid State Division will use in its upcoming ASIC Silicon Circuit Board products. Communicating with Vital by means of an ASCII data base, Happi uses that program as an interactive front end and is transparent to the user. But the results are far from invisible. Running on a Digital Equipment Corp. VAX 8600, the new program produced one chip design incorporating three macrocells and 1,500 standard cells in 97 minutes—about half the time it took to produce the same design using RCA's older and more established MP2D placement and routing program.

"We are faster than MP2D, there's no doubt about it," says Rathin Putatunda, a technical staff member with the ASIC, CAD, and VLSI Design, Development, and Support Lab at RCA's Advanced Technology Laboratories in Moorestown. "We're about 50% better in speed." But Putatunda adds it's not just speed that makes Happi special. "Our previous programs, like MP2D, could only handle up to four macrocells—and even then, with restrictions on the locations where those cells could be positioned on the chip. This program has more flexible power distribution, more flexible chip topology, and it's much better in terms of placement and routing."

Happi does not represent the death



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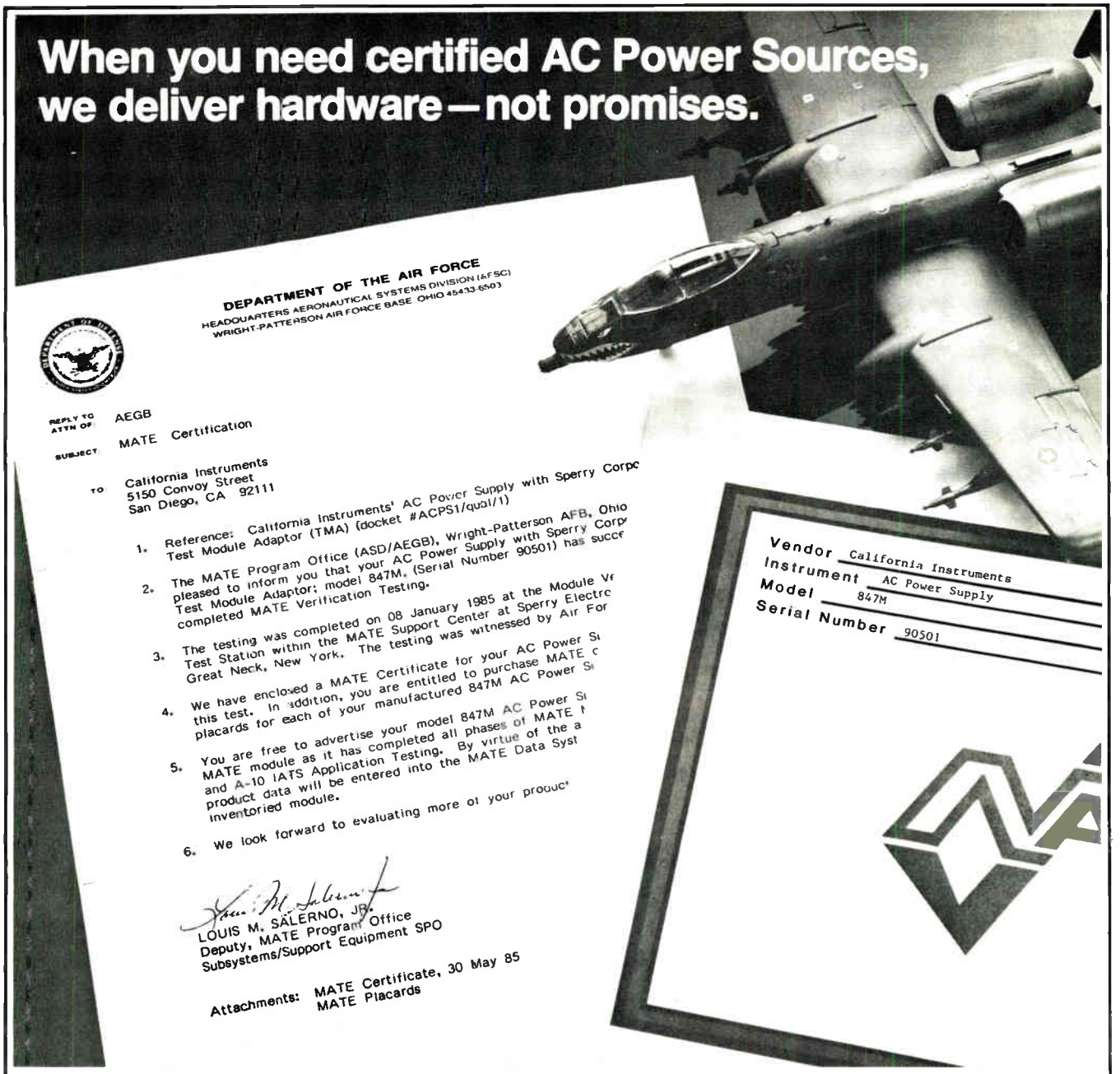

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knell for MP2D, however, says Putatunda. MP2D has a large installed base, both in and out of RCA. And the Happi system is designed for double-metal processes, while MP2D is a single-metal program. RCA has no plans yet to market the program, but that is an option it will study—especially because Happi will be able to interface to Silicon Compilers Inc.'s macrocell library.

Happi's high degree of automation comes from its highly structured topology, Putatunda says. Following a binary-tree pattern, the chip is laid out section by section such that certain domains within the chip's architecture must be in place before the program can proceed to other domains. With this scheme, Putatunda and his research team were able to develop a flexible system that simplified the automatic-routing task.

"We chose structured chip placement to facilitate automatic routing and automatic power bus distribution," Putatunda says. "The binary tree structure also helps to minimize area and the interconnect distance between domains."

"It makes routing much easier—it simplifies it," adds Stephen McNeary, who along with Putatunda and David Smith took the project from start to finish over the last 18 months.

Happi's placement component is responsible for generating and placing the domains and determining the cell-row spans of the standard-cell domains. Macrocells are always domains unto themselves, but the placement program can choose the cell's orientation—whether it is to be flipped or turned into any one of eight positions.

CLUMPS. Standard cells, on the other hand, are arranged in clumps to make the best use of real estate while keeping trace lengths to a minimum. "We like to see the standard cells as a big soup," says McNeary, explaining that standard cells are "malleable" compared to the macrocells, which are fixed in shape and dimensions. "With the standard cells, it's putty logic," he says. "You can squeeze them around the macros."

Happi's routing component generates the power-bus network and performs the detailed routing of signal and power lines automatically. It is here that the responsibility for low channel density falls. Long multiple-connection nets are broken down into segments and assigned to routing channels. Unlike conventional approaches, which use additive power routing, Happi uses a subtractive process, starting out with an overconcentrated power bus and gradually taking out connections when it becomes apparent that they are unnecessary.

"The philosophy behind the power-bus generation method is to maximize the sources feeding power to every domain while attempting to minimize the impact of power bus routing on chip area," Putatunda says. "The channels that affect the X and Y dimensions of the chip are the critical channels. The main aim is to delete as many of the power-bus segments in these channels as possible." *–Tobias Naegele*

TELEPHONY

DSP POACHES ON ANALOG CONFERENCING

DALLAS

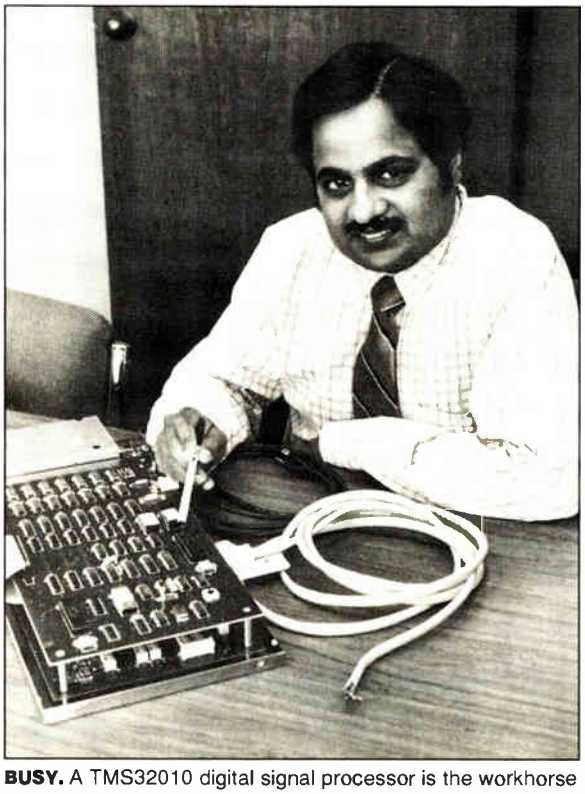
The telephony world is getting a bit dizzy as the digital revolution whirls along. Most digital private branch exchanges implement conference calls by converting voice signals back into analog form for tried-and-true, low-cost analog summing. And now a small Dallas-area company is going the other way—introducing a teleconferencing product that connects to older analog exchanges but makes its line connections digitally.

The digital-analog anomaly results from familiar tradeoffs between the use of new technology and higher costs. DSP Technology Corp.'s digital Confer teleconferencing bridge is further evidence of inroads made by programmable digital signal-processing chips, which were once considered too costly and exotic to be used for end-user telecommunications equipment.

FALLING PRICES. "We aim to take advantage of the falling prices of DSP chips, which until the past year have been too costly to consider for most telecommunications applications," says Paul Pandian, president of DSP Technology, Carrollton, Texas. Texas Instruments Inc.'s TMS32010 DSP chip has dropped from $120 in 1983 to under $10 today in large quantities, according to TI. The growing ranks of DSP suppliers are expected to spark price competition in the coming years.

DSP Technology is applying the TMS-32010 in its six-party teleconferencing subsystem, which will be available next month for $1,495. Pandian says the Confer conference bridge, which installs on the central-office trunk-line side of an analog key-service unit, targets offices with 30 to 50 workers.

The 19-by-10-in. wall unit is controlled by the telephone's tone-key pad. With it, workers can set up conference calls using phones either inside or outside the office. The ideal installation would have a 10-line key-service unit, says Pandian, who notes that about 200,000 analog exchanges are still shipped each year.



BUSY. A TMS32010 digital signal processor is the workhorse of DSP Technology's conferencing system, says Natarajan.

The reverse of DSP Technology's analog-to-digital approach is found in digital PBXs. For example, Shared Resource Exchange Inc., Dallas, has been shipping a small bus-based digital exchange that connects calls in an analog manner [*Electronics Week*, March 18, 1985, p. 17].

Shared Resource uses standard pulse-code-modulation codec chips to change digital voice signals into analog form. The analog signals are then combined using a conventional resistive summing network, says Charles B. Johnson, cofounder and executive vice president. The company's office system has a standard module supporting three-party conferences but more lines can be connected, he adds.

"It is a cost issue," says Johnson, referring to the use of DSPs in conferencing hardware. "It is a nice

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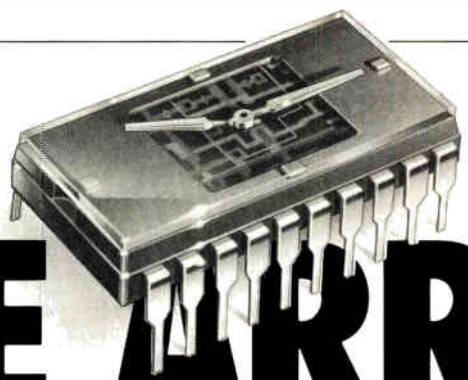

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sophisticated approach, but a lot of times it ends up costing more than the standard analog solution." His company uses three $3 codecs to perform digital-to-analog conversion for conferencing and then analog-to-digital to return the combined conversation to the digital PBX system.

But DSP Technology executives believe the cost barrier is starting to crumble. Inside Confer, the 32010 processor is a multitasking workhorse, not only combining up to six phone conversations but also playing digitized music for those on hold. The chip also handles the complex overhead of converting logarithmically companded voice bits into a mathematical form better suited to its real-time switching algorithms.

The 32010 uses a proprietary algorithm to quickly switch speakers in and out of the conversation. The loudest speaker is switched onto the line at any given time. The chip also automatically adjusts each speaker's volume, compensating for losses in long-distance lines.

The 32010 estimates speech energy levels using the recursive filtering algorithm. It samples speech from each line every 4 ms to decide which party is speaking the loudest. The software is held in 2-K 16-bit words of off-chip programmable read-only memory. But connecting conference callers is the easy part, says T. Raj Natarajan, vice president of engineering.

The toughest part of software development came in the overhead needed to use inexpensive codecs, he says. DSP Technology opted to use single-chip codecs over other ADCs because of hardware costs. The penalty was additional development time needed to write the code for converting the companded digital output of μ-law pcm codecs into the linear values used by the DSP chip. "That conversion is a big task, but we perform it routinely as part of the processing of all six channels," says Natarajan.

Nonconference calls pass through Confer without processing. Calls being connected first pass through an analog interface and then into a bank of six codec chips, which digitize speech.

After voices are digitized by the codecs, a serial-to-parallel shift register sends 8-bit blocks of voice data 8,000 times a second for each of up to six channels to the 32010. The DSP, which has a 200-ns instruction cycle time, converts the μ-law voice data to a linear format, switches in loudest speakers in real time without clipping off the first syllable of words, and then places speech back into a companded form so that the codecs can perform digital-to-analog conversion. The combined conference-call signal is then placed back on the analog network. *–J. Robert Lineback*

OPTOELECTRONICS

DEVICE PROMISES DENSER OPTICAL DISKS

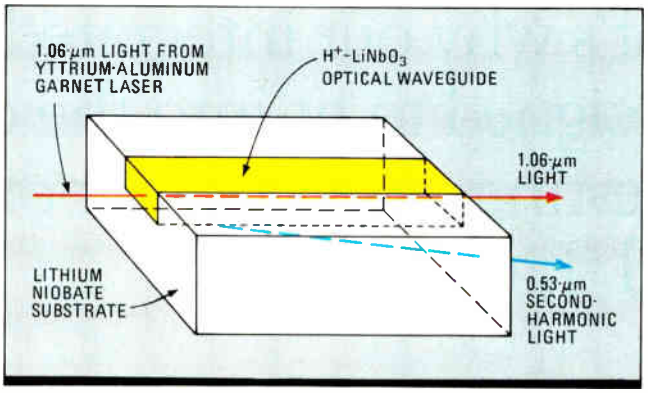
OSAKA, JAPAN

If anyone knew how to make them, short-wavelength semiconductor laser sources would be just the ticket for such applications as higher-density optical-disk recording systems and more efficient laser printers for facsimile and typesetting systems. Another approach promises to become practical in the short term: halving the wavelength of the light from near-infrared laser diodes from 0.84 to 0.42 μm with second-harmonic generators.

Matsushita Electric Industrial Co. will offer samples of its second-harmonic generators later this year [*Electronics*, June 23, 1986, p. 13], heralding the first low-cost, high-efficiency products after more than two decades of development in Japan and elsewhere. Volume production of the chips should bring prices down low enough for use even in such consumer products as Compact Disc players, says Takao Kajiwara, director of the Matsushita Semiconductor Research Center's Optoelectronics Laboratory, Osaka.

Early production devices would provide 1-to-3-mW output levels for a 30-mW input, an adequate efficiency level for playback-only disk systems or optical printers, say the company's researchers. Over the longer term, efficiency will be improved, providing output levels of up to 10 mW for the same input power. The current experimental devices were fabricated by a group headed by Matsushita researcher Tetsuo Taniuchi in cooperation with Yoichi Fujii, a professor at Tokyo University.

The lithium niobate devices have optical waveguides 2 μm wide by 0.55 μm deep that run the chip's full 6-mm length. When an IR beam flows into the waveguide, part of its energy is converted to the second harmonic by the $LiNbO_3$'s nonlinear optical characteristics and radiated at a 12.5° angle from the original beam path. Because attenuation losses are only a fraction of a decibel for a 10-mm length of waveguide, efficiency improves as device length is increased.



HALF AS MUCH. Matsushita has built a second-harmonic generator that halves the wavelength of near-infrared laser light.

Matsushita's present experimental second-harmonic generators use a 1.06-μm input wavelength generated by an yttrium-aluminum-garnet laser. For use with the 0.84-μm light from semiconductor lasers, the depth of the waveguide will be reduced to about 0.47 μm.

Commercial chips will carry input and output lenses. Improved lens design should lead to higher efficiency because the input beam's diameter currently exceeds that of the optical waveguide. Efficiency also increases at higher input power; Matsushita has measured values as high as 25% for a 1-W input. Higher efficiency is the result of increased optical nonlinearity at higher input power.

The optical-grade $LiNbO_3$ wafers used as a starting material are about 2 mm thick. Photolithography processes selectively etch an aluminum mask with a window slit where the waveguide is to be.

The wafer is then immersed in heated benzoic acid for a proton-exchange process that partially replaces lithium atoms inside the waveguide with hydrogen atoms. This step increases the optical waveguide's index of refraction to 2.33 from the 2.2 value of the original $LiNbO_3$. The higher-index waveguide surrounded by the lower-index chip material and air is similar to the core of an optical fiber surrounded by its cladding layer.

Devices for second-harmonic generation that are currently available commercially use bulk single crystals of potassium titanate phosphate or potassium dihydrogen phosphate. The price of such devices is high—about $6,000 each.

In bulk devices, the power density of the fundamental beam is lower, reducing the magnitude of the material's nonlinear behavior because the beam is not confined within a waveguide. Furthermore, the fundamental and second-har-

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monic beams have different phase changes with temperature, necessitating expensive close-tolerance (on the order of 0.1°C) temperature control for phase matching. Even so, efficiency remains orders of magnitude lower than it is for the Matsushita device.

Other researchers have used waveguides, but the mode of operation they have used is different and results have been inferior. Researchers at NEC Corp. have developed a device with a sputtered $LiNbO_3$ waveguide on top of a magnesium oxide crystal, but losses in the waveguide are high. Researchers at the Musashino Electrical Communications Laboratories of NTT Corp. developed a second-harmonic-generation device in which a waveguide is formed by diffusing titanium as a dopant into a $LiNbO_3$ crystal, but it is susceptible to damage from incident light, and the index of refraction varies with wavelength. *–Charles L. Cohen*

CONSUMER

FRENCH SPARK HOME-NET STANDARDIZATION EFFORT

PARIS

The French electronics industry is taking the initiative in establishing a European standard for tomorrow's domestic networks. The move aims to gain an edge on Japanese and U. S. competitors—Mitsubishi, Sharp, Apple Computer, GE, and Honeywell, among others [*Electronics*, July 1, 1985, p. 45]—that are expected to attack the European home-network market with products based on their respective Home Automation and Smart House projects.

Simavelec, the consumer electronics group of France's Fédération des Industries Electriques et Electroniques last month presented a working prototype of a home network put together with the cooperation of more than 30 native electronics firms, including all principal companies. The French will present the prototype to standards organizations in an effort to gain Europe-wide acceptance for the approach. They will also try to put together a project under the aegis of the European Eureka high-technology research and development initiative to promote further home-networking developments.

A great deal is at stake. Though executives hesitate to estimate the size of the market, they generally agree the home network would spur the consumer electronics market out of its doldrums within the next five years by giving consumers a reason to buy goods with more modern features. One beneficiary could be the home computer, which might serve as the network's programming station.

France is in a strong position to push standardization. Some eight years ago, the government accepted the Peritel interconnection system as the national standard for linking TVs with external equipment. More than half of the TVs in France are now equipped with a 21-pin Peritel socket, which was made an obligatory accessory on all sets sold since 1980. The connector was made a European standard in 1984.

REMOTE CONTROL. The Peritel connection makes it possible to receive and transmit signals in a number of formats: composite video, red-green-blue video, stereo audio, switching voltages, and digital data. To exploit the Peritel, the French have now developed a system called Sidav, from the acronym for dynamic audiovisual interconnection system, which can switch the different signals on the plug to and from external devices. Sidav is a programmable network node controlled remotely by a TV system with a more versatile keyboard than is usually found on a set.

Peritel and Sidav form the center of the home-networking proposal. French equipment manufacturers are now in the process of defining links between this Peritel-Sidav audiovisual core and other necessary parts of the home network, such as systems for security and surveillance, domestic robotics, and external communications.

Under development are a gateway to two-wire telephone networks and coaxial video networks, interfaces to electrical power wiring and alarm systems, and a filter for the home's electric meter to prevent commands traveling on the electric wiring from going beyond the home. Electronics executives feel they could be available as early as next year.

The user will be able to configure his electronic equipment any way he wants. He could, for example, watch TV while switching the program's sound so that he hears it through his stereo system. He could watch one program and record another, or broadcast a recorded program to all the TV sets in the house. The connections with the home's electrical power wiring will create an interactive interface with Sidav so that, using the TV remote control, the user can control lights and appliances.

The Simavelec (for Syndicat des Matériels Audio-Visuels Electroniques Grand

USAF WEEDS OUT BIDS TOO GOOD TO BE TRUE

The Air Force has begun to screen out military contract bidders who submit superb proposals but have little capability for executing them. By dispatching what it calls "graybeard" teams—groups of experienced military and civilian personnel—to assess capability prior to awarding contracts, the Air Force has uncovered a host of shortcomings lurking behind slickly written proposals.

The program was instituted late last year at Hanscom Air Force Base's Electronics Systems Division. But it had its first public airing in Newton, Mass., late last month when Lt. Gen. Melvin Chubb Jr., ESD commander, reported on results of the screening program at a conference focusing on future trends in Air Force electronics.

The graybeard teams have uncovered a number of potential problems in submitted proposals. Among them are lack of software-management experience, promises of off-the-shelf availability for hardware still under development, and bidding for Ada work by organizations with no experience with the Pentagon's programming language.

CHUBB: An advance look to assess bidder capability.

Frequently, companies hire consultants to write proposals, but have no in-house team available to execute the work. As a result, "programs usually lose six months in the first six months," Chubb says. Contractors "generally start with the wrong team. Never is there enough talent put in during the first six months to get the program rolling."

But since November, the ESD's graybeard teams have been evaluating bidders. "It's like your oral exam for your PhD," says Dennis Volpe, assistant deputy commander of international programs, who chaired one of the teams. "The proposal is like your thesis, but you've got to defend it." Companies are asked to produce for evaluation the people who will manage and execute the contract if awarded. *–Craig D. Rose*

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Public) demonstrated the equivalent of an apartment whose living room and three bedrooms were wired with a cable network and telephone lines and equipped with a Minitel, France's low-cost videotex terminal. A country home was connected in the same way and the two residences were linked to each other and to a private security agency through a cable network.

Shown in operation were interconnections among a wide range of audio and video equipment as well as sensors to signal intrusions and failures of equipment, such as the freezer. As an example of remote control, the Simavelec showed how the country home's garden could be watered in response to commands issued at the primary residence. *–Robert T. Gallagher*

IC TESTING

A FASTER WAY TO OPEN UP PLASTIC PACKAGES

BERN, SWITZERLAND

If it meets our stringent demands, it is sure to make it on the outside." So argues a small Swiss electronics producer that has developed, originally for its own use, a fast, cost-saving, and environmentally clean etching method for opening up plastic packages so failures can be analyzed on bare chips.

The decapsulation method is the result of a one-year development effort at Gfeller AG, a $65 million communications equipment maker in Bern. It relies on a stream of hot sulfuric acid squirted against the plastic package to etch it away where the circuit is embedded and leave a well-defined hole extending down to the chip's surface. The jet-etch process takes 2 to 3 min.

"We wanted a safe and reliable technique for in-house use to open up plastic-encapsulated circuits for failure analysis," says Hans Köppel, head of Gfeller's materials test laboratories. "The results our technique yields have convinced us that we can commercialize it for the open market." Köppel believes the method is superior to other etching schemes used for this job.

The Swiss technique has been implemented in an experimental etching system called the Jetty, whose manufacture Gfeller will either handle on its own or license to another company. Gfeller says several semiconductor makers, among them West Germany's Siemens AG, are interested in the method.

Quality-control engineers are increasingly turning to this type of fault analysis because electrical tests at the pins often cannot pinpoint the cause of a failure. In such cases, it is necessary to bare the chip so it can be visually examined, viewed through an electron microscope, or tested with microprobes.

TOUGH TO OPEN. Unlike metal or ceramic housings, which can easily be removed or cracked apart in mechanical operations, plastic packages are hard to open because of the material's cohesive nature. Chemical etching must therefore be applied, and of the three techniques that are possible—plasma, ion, and jet etching—the latter is by far the fastest and least costly, Köppel says.

Fully automatic to provide reproducible results, Jetty ensures that the hot sulfuric acid comes in contact with the chip for the shortest possible time to prevent damage to the bonds and passivation layers. After the etching process, the chip is automatically rinsed to remove traces of the acid.

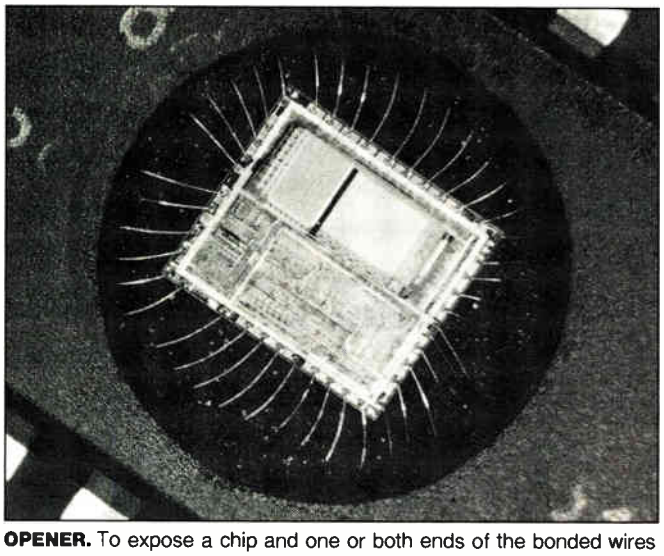
Of particular note, Köppel says, is that the technique is environmentally clean—an important requirement these days, given the sensitivity of governmental authorities, and one that some competing sulfuric-acid-based systems don't meet.

The heart of the Jetty system is the etch head, upon which the package sits with its pins up. Protruding through the etch head is a 1-mm tube inside a slightly larger outer tube. All parts of the equipment that come in contact with the acid are made of glass.

A thin jet of sulfuric acid, heated by a quartz heating system to 285°C, or just below its boiling point, shoots through the inner tube, hits the plastic material, and etches it. A suction pump draws off the waste acid through the outer tube and cools it to about 40°C. The etching process typically stops after 2 to 3 minutes, when the Jetty senses that the electrically conductive sulfuric acid has made contact with the package pins.

GAS CONTROL. A microprocessor controls and monitors the etching, the heating of the acid, the operation of the system's electromagnetic valves, and the level of the acid in its containers. Acid temperature is monitored independently of the other functions to ensure that the acid does not escape as a gas.

Before the package is opened, the chip's location in it must be determined. This is best done, Köppel explains, by means of X-ray equipment with fine focusing; ultrasound methods can also be used. Then plastic is milled off the package to reduce the amount that must be etched away. *–John Gosch*



OPENER. To expose a chip and one or both ends of the bonded wires (above) to allow fault analysis with a microscope or microprobes, Gfeller's Jetty acid stream system (right) can etch away a plastic package.

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INTERNATIONAL NEWSLETTER

CGE, ITT JOIN TO FORM TELECOMMUNICATIONS GIANT

Telecommunications companies the world over will have to rethink their strategies now that ITT Corp. and Compagnie Générale d'Electricité, the nationalized French switch maker, have joined forces to create the world's second-largest telecom-equipment firm. In addition to receiving a $1.8 billion cash payment, ITT will maintain a 30% share in the company. The remaining 70% will belong to a European holding company in which CGE will have a controlling interest. CGE will likely own a full 50% of the new firm; the rest will be held by a consortium that includes the banking group Société Générale de Belgique and Telefonica SA, the Spanish telephone company. With activities in 75 countries and annual sales approaching $9.6 billion, the new company will be second only to AT&T Co. in the world telecom-gear market. □

SIEMENS AND PHILIPS LINE UP TIES IN TELECOM CHIPS

Philips of the Netherlands and West Germany's Siemens AG, which have already teamed up to develop megabit memories, are hammering out details of an agreement to cooperate in telecommuncations chips. Sources close to the two companies expect a second-source deal to be announced later this month. For starters, the Dutch company will produce two of Siemens's chips for integrated services digital networks, the 2070 communicatons controller and the 2080 interface circuit [*Electronics,* Sept. 30, 1985, p. 46]. For its part, the Munich company is likely to second-source certain Philips chips for use in private branch exchanges. The deal is part of a strategy by the two companies to thwart U. S. and Japanese producers that are trying to gain a foothold on the Continent's telecom chip market. □

MINOLTA PITCHES ITS TENT IN THE VHS-C CAMCORDER CAMP...

Victor Co. of Japan (JVC) has signed on a heavyweight ally for its campaign to snare market share in the compact video cassette camera/recorder market from Sony Corp., the pioneer with its 8-mm camcorder. The marketing minds of Minolta Camera Co., Osaka, have followed JVC's lead and become the second Japanese company to produce VHS-C camcorders, which JVC developed to compete head on with 8-mm camcorders. Minolta is buying the mechanical recording and playback deck assembly from JVC on an original-equipment-manufacturer basis and manufacturing the electronics and other parts itself. Major Japanese consumer electronics houses—among them Hitachi, Matsushita, Mitsubishi, Sharp, and Toshiba—plan to sell private-label VHS-C camcorders bought from JVC starting this summer. Both Hitachi and Matsushita intend to go into production themselves next spring, and the others presumably will follow suit if the market takes off. Meanwhile, Minolta plans to make 2,000 units a month, mostly for export to the U. S. □

...AND HITACHI STRADDLES THE FENCE WITH A CLAIM IN 8-MM TERRITORY

Whatever the outcome of the camcorder campaigns, Hitachi Ltd. figures to end up with the winners. Already set to sell JVC's VHS-C gear under its own label, the Tokyo company will start manufacturing 8-mm camcorders in September, but only for private-label products that Japanese camera makers such as Minolta Camera Co. will export. Production will be 5,000 units per month. Hitachi's move follows that of Matsushita Electric Industrial Co., which supplies Eastman Kodak Co. and Olympus Optical Co. with 8-mm camcorders on a private-label basis for the American market. Although Hitachi and Matsushita so far are marketing only VHS-C camcorders under their own names, they are positioning themselves to jump into the 8-mm market, too, if Sony's future success forces them to do so. □

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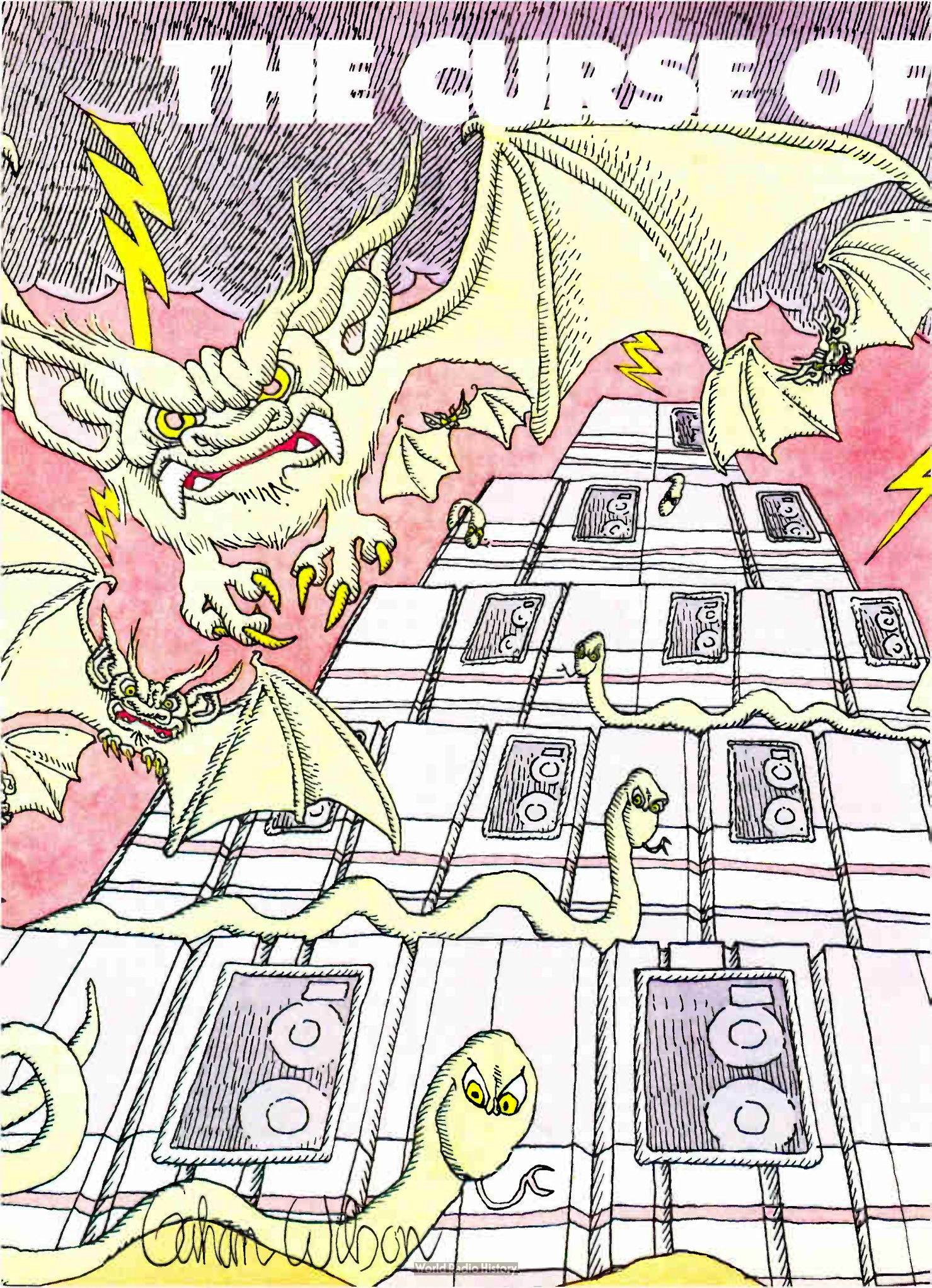
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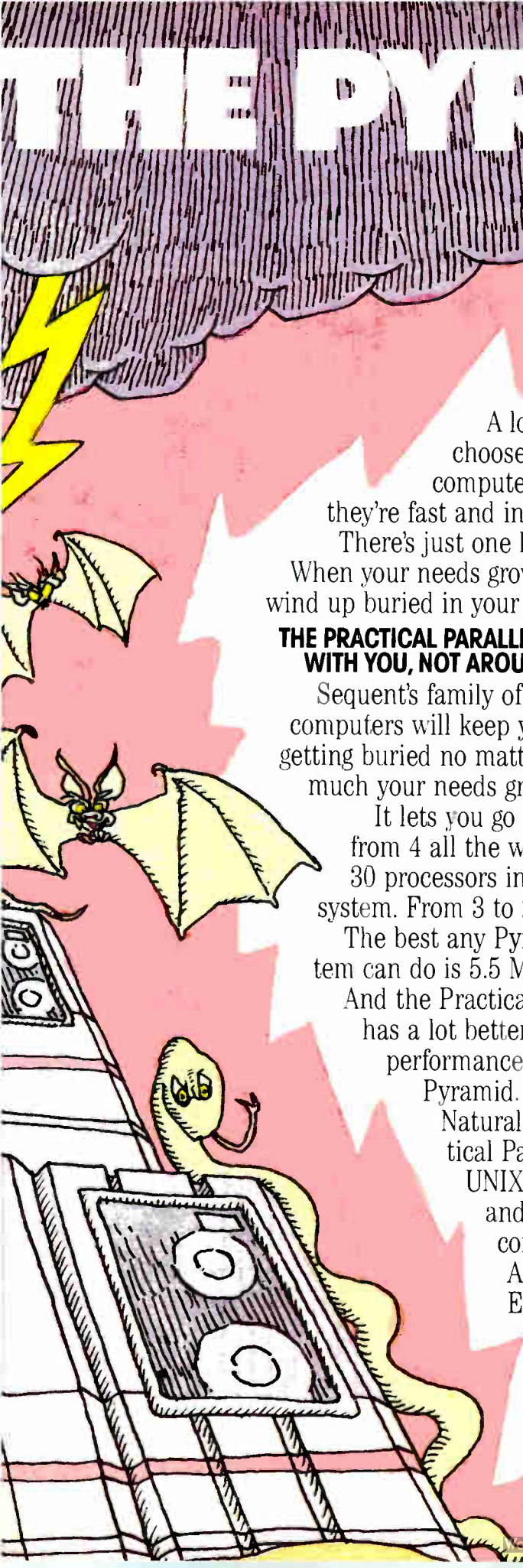

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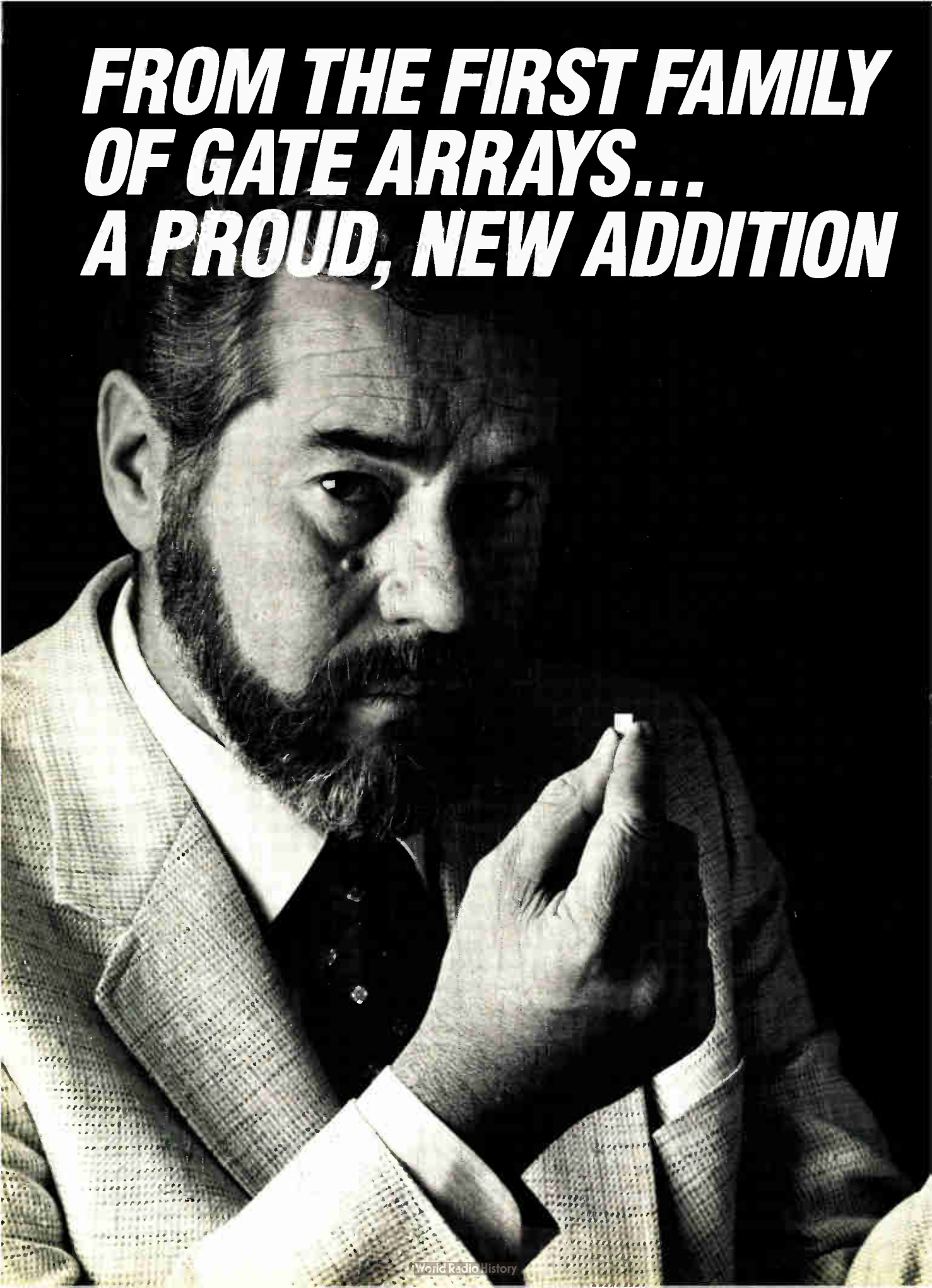
FROM THE FIRST FAMILY OF GATE ARRAYS... A PROUD, NEW ADDITION



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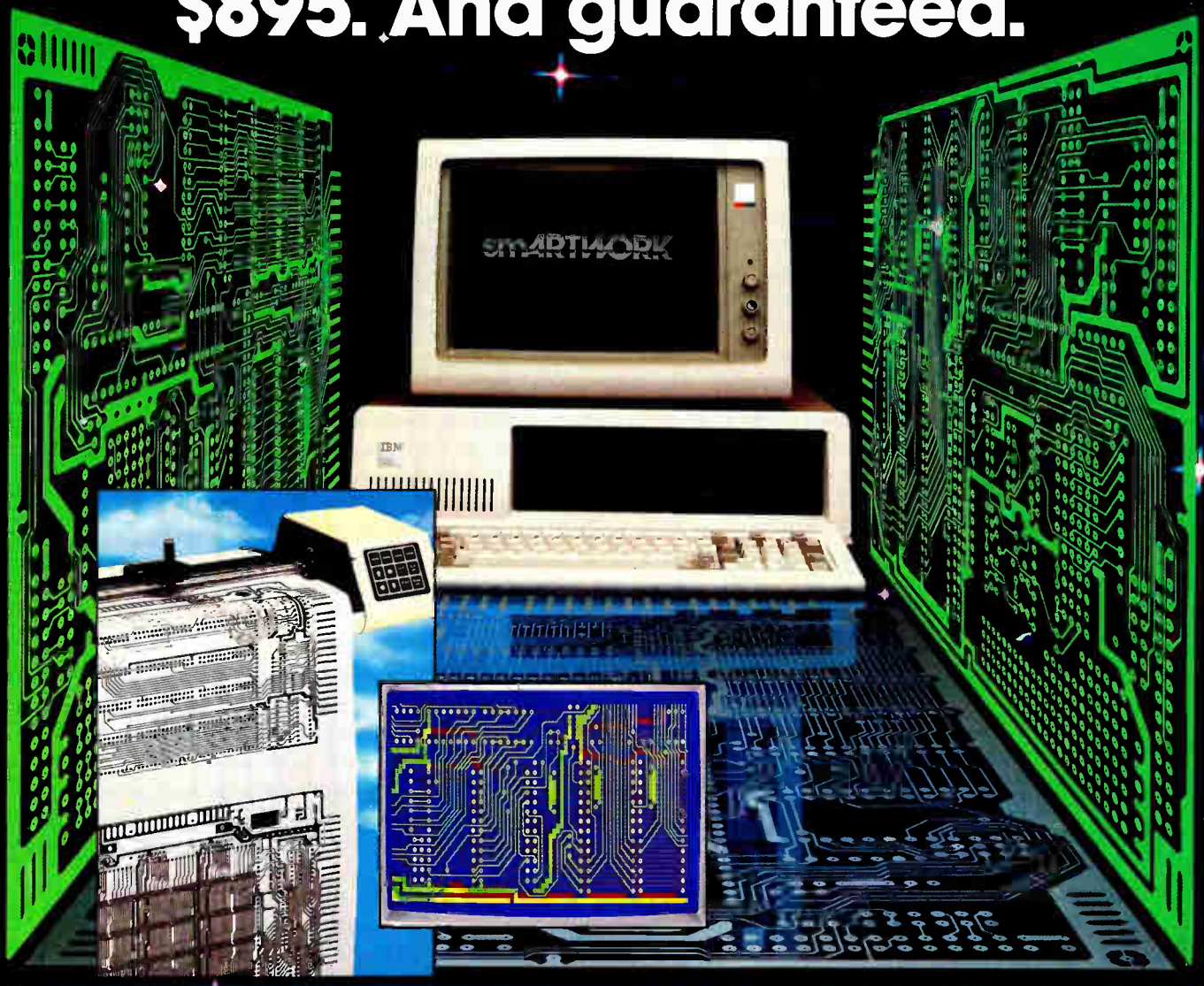

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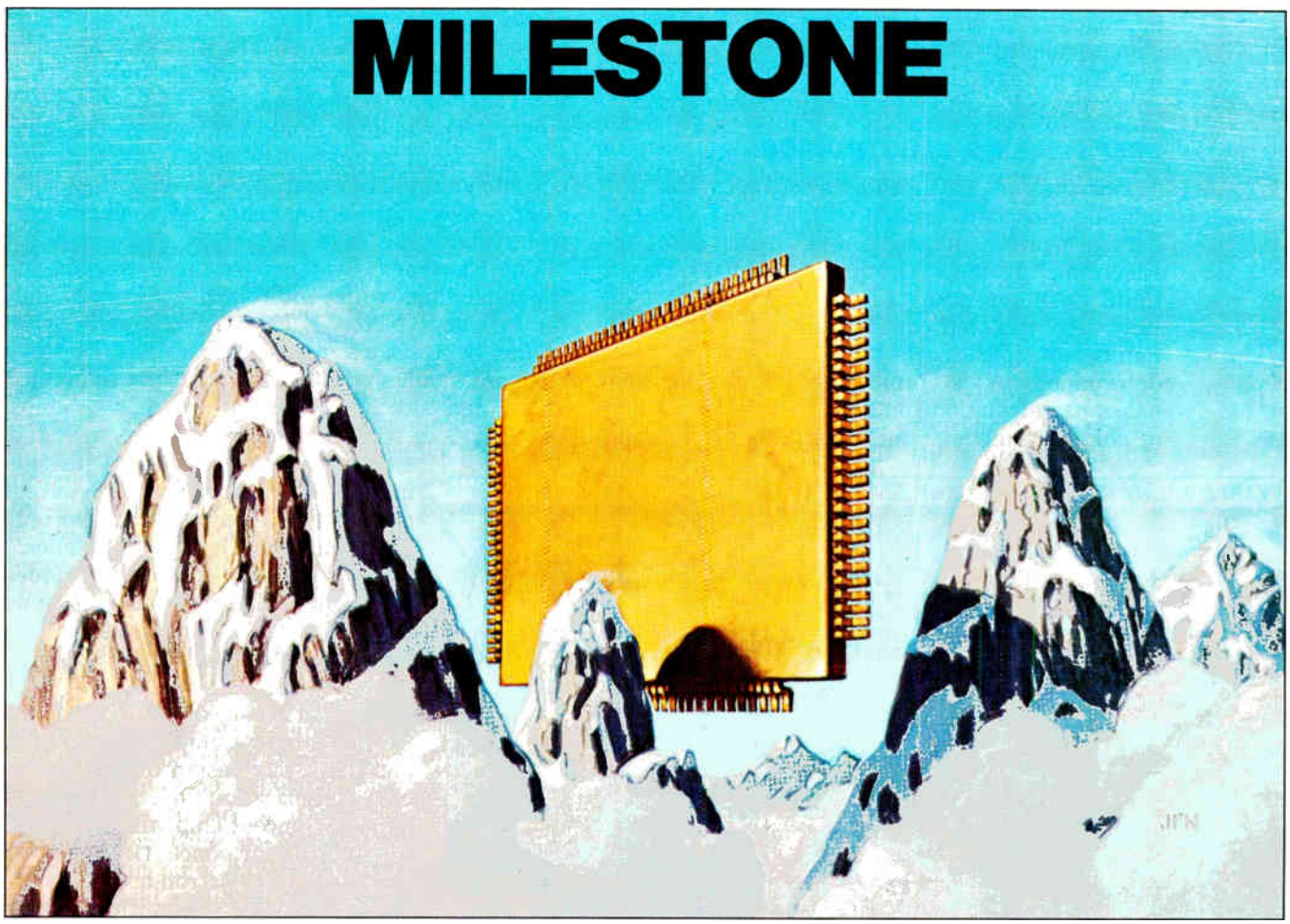
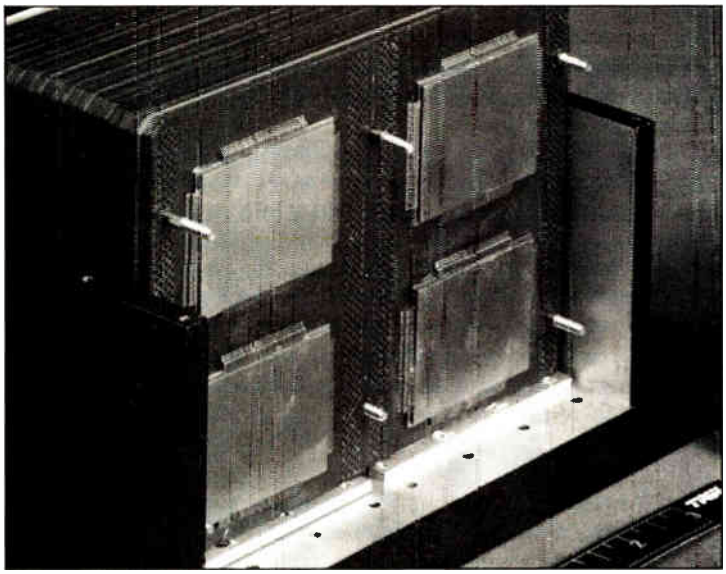
INSIDE TECHNOLOGY

TRW's SUPERCHIP PASSES FIRST MILESTONE



At last, the superchips are solidly on their way. And they bring with them vast improvements in computing power. TRW Inc. has already fabricated process-test versions of the ultrahigh-speed submicron devices. Work on the next step, chips to test the twin concepts of self-diagnosis and software



3. MOCKUP. The cards in a VHSIC Phase 2 signal processor show the packages used for the superchips under development.

also accrue—superchips dissipate only 0.25 W per square inch, against 50 W/in.^{2} for VHSIC Phase 1 packages, according to Zimmerman. The resulting superchip packages are the same as those for Phase 1, only larger (Fig. 3).

Still awaiting approval by the DOD are three other TRW superchips: a bipolar fast Fourier transform circuit, a 32-bit CMOS data processor, and a 1,024-word-wide associative processor, also fabricated using the company's CMOS process. The most impressive of them is the associative processor, which incorporates a parallel architecture. Processors of this type typically incorporate a parallel architecture that consists of a single-instruction, multiple-data-stream array of processing elements and a content-addressable associative memory. The TRW associative processor can execute a sequence of instructions on stored data in parallel at throughput rates of up to 10 billion operations/s and is aimed at artificial-intelligence applications involving complex pattern matching and analysis.

An associative processor executes a sequence of pattern-matching operations on all data within its content-addressable-memory array. Whenever the matching succeeds, some manipulation is performed on those data words found to match. The von Neumann-type architecture used in most general-purpose microprocessor CPUs executes a sequence of arithmetic and logical operations, each containing the memory addresses where the operands are assumed to be stored.

The fast Fourier transform chip is a systolic array that can perform a 1,024-point operation in 41 μs. At the system level, this translates into a throughput of about 1 billion complex operations/s. The chip also provides premultiply and presummation windowing with on-chip trigonometric recombination. The data processor, says Zimmerman, is similar to a reduced-instruction-set computer and has an architecture and instruction set optimized for implementing floating-point functions at data rates up to 20 million instructions/s. It also contains a 1-Mb SRAM with an access time of 20 ns. □

TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*

HOW TWO AT TRW ARE TACKLING A ONCE-IN-A-LIFETIME PROJECT

Both Fred L. Alexander and Thomas A. Zimmerman are keenly aware that the superchip VHSIC Phase 2 project they direct at TRW Inc. is that once-in-a-lifetime opportunity engineers dream about. First of all, the fault-tolerant redundancy feature of the advanced chips involves refinements designed to make concepts first advanced in wafer-scale integration work—a hitherto unaccomplished feat. In addition, the 1.4-by-1.4-in. chip size, larger than anything else in sight, goes against the technology grain of ever-smaller devices.

Enthusiasm for superchips continues to build throughout the large technology team effort orchestrated by the two TRW veterans, they report. It began when military-electronics project leaders were called in to write the formal proposal for the Defense Department in 1984, recalls Zimmerman, who manages the company's Very High Speed Integrated Circuits program projects.

A widespread feeling of taking part in a seminal development effort indeed exists among engineers and scientists involved with superchip, adds Alexander,

SUPERCHIP TEAM. Alexander (left) and Zimmerman direct TRW's VHSIC Phase 2 project on superchip development.

who is vice president and general manager of the Electronics & Technology Division. "It will be a tremendous breakthrough, if we can pull it off," he notes. Though no serious pitfalls now loom, the concept will be proven absolutely only when the devices are built during 1987-88.

Alexander and Zimmerman, both midwestern natives, have been immersed in VHSIC since it began more than five years ago. Alexander, who joined TRW in 1963, managed VHSIC programs before promotion to his present post. He holds BSEE and MSEE degrees from the University of Missouri. Zimmerman was a prime mover in formulating TRW's VHSIC strategy and previously managed the Charge-Coupled Device LSI Products Department. He holds a PhD in electrical engineering from Purdue University. He joined TRW in 1971.

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I hate manuals. Get me a system with drop-in menus. In English.

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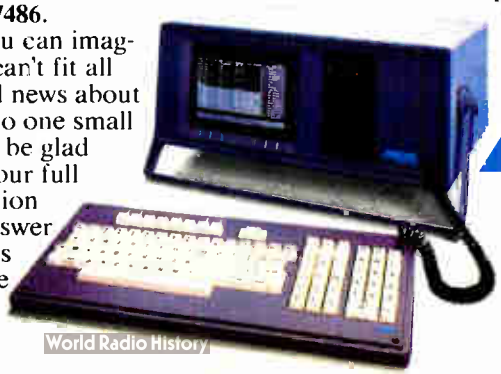

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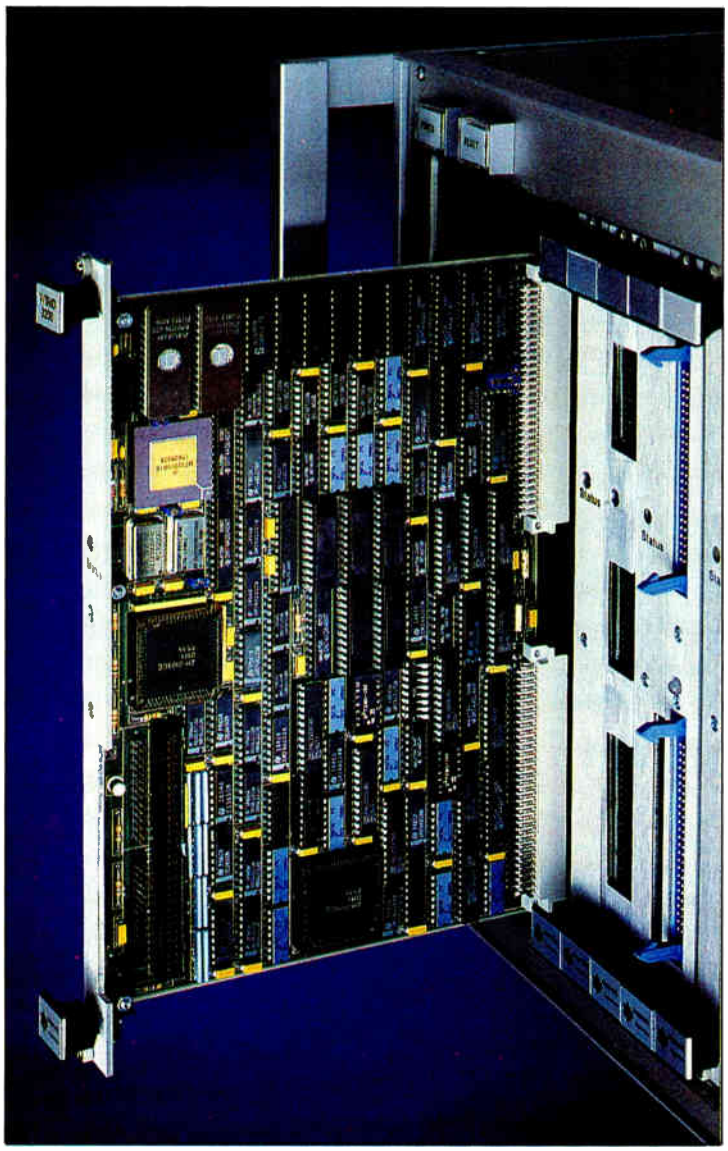
BREAKING THE SPEED BARRIER ON THE VMEBUS

A new bus interface uses packets and a delay-line asynchronous state machine to send data at more than 30 megabytes/s—near the top speed of Multibus II



1. SPEEDY. Interphase's V/SMD 3200H controller uses the BUSpacket to send data between disk drives and the VMEbus at more than 30 megabytes/s.

Interphase Corp. has good news for system builders using or considering the VMEbus. The Dallas company has developed the BUSpacket, a VMEbus interface that more than triples the bus's throughput to more than 30 megabytes/s. That puts the VMEbus neck and neck with rival Multibus II, which boasts a speed of 32 megabytes/s.

The BUSpacket sends preformatted data packets across the VMEbus as fast as the bus can take them. The packet approach keeps the bus-transfer rate from dropping to the speed of the slowest device on a board interfaced to the VMEbus. Interphase, a maker of high-performance peripheral controllers, added the BUSpacket to its existing Storage Module Drive disk controller (Fig. 1) and hiked its throughput from 5 to more than 30 megabytes/s. That performance sets a new speed level for VME peripherals.

The VMEbus's theoretical throughput under ideal conditions is about 40 megabytes/s. Most VMEbus interfaces run at 5 or 10 megabytes/s, however, because they transmit data in streams. If the random-access memory used to buffer data is much slower than the maximum bus-transfer rate, for example, it will lower the bus-transfer rate to its own speed. "It is criminal to use the bus at 10 megabytes/s when it is rated at 40," says Michael E. Cope, Interphase president and founder.

System designers and users seem to agree. They are starting to demand performance as high as 30 megabytes/s on system buses to match new peripherals, such as high-performance disk drives, that are coming along. These peripherals cannot reach their full potential if bus throughput stops at 5 or 10 megabytes/s, as is the current state of the art in VMEbus-based systems.

In such systems, the disk drives often use as much as 35% of the bus time. Therefore, for good system efficiency—or balance—the disk subsystem must make effective use of the bus when it has it. A subsystem that wastes bus time is a drag on a system.

The BUSpacket allows slower devices to work off its first-in first-out bus-isolation buffer at their speeds while allowing the state machine and the VMEbus to work off the other side of the FIFO at their maximum speeds. Thus BUSpacket adds the message-passing features of Multibus

II to the best aspects of the asynchronous VMEbus. Message-passing enhances the performance of multidevice systems by decoupling the operations of the devices from each other, from on-board buses, and from the system bus.

The BUSpacket's two keys to faster bus traffic are the FIFO buffer and an asynchronous state machine (Fig. 2). In the upgraded version of its controller board, Interphase also increased the size of the multiport RAM buffer from 16- to 128-K bytes to add flexibility and efficiency to data buffering between high-speed peripherals and the system bus.

The 256-word FIFO buffer builds up the packets before they burst out on the bus at high speed. Based on a delay line, the asynchronous state machine controls the flow between the FIFO and the bus. It actually controls the active VMEbus signaling, quite unlike its synchronous counterparts in older VMEbus schemes. Synchronous state machines are triggered by a clock signal and must march in step with the bus signaling without exerting any control.

The BUSpacket interface achieves its high rates by formatting data packets and storing them in the FIFO before acquiring the bus. Then it acquires the bus, the FIFO empties at more than 30 megabytes/s, and the bus is released for other uses. Therefore, the bus activity is entirely decoupled from the other functions on the board.

Without decoupling, achieving the VME specification's maximum burst-transfer rate would take RAMs with access times in the tens of nanoseconds. But wringing such performance from the current generation of RAMs is too costly in terms of hardware and board real estate. So slower parts are being used, though throughput suffers because of the coupling between on-board functions and the VMEbus.

The BUSpacket architecture decouples the controller board functions from the bus. This means that the operation of the components on the local buses of the controller card are not tied to the operation of the system bus. Without this independence or decoupling, the slowest function would set the maximum speed. Decoupling allows fast devices to operate at full speed; for example, the interface to the VMEbus can run at the fastest speed that data can be burst onto the bus, even if the buffer RAM is much slower.

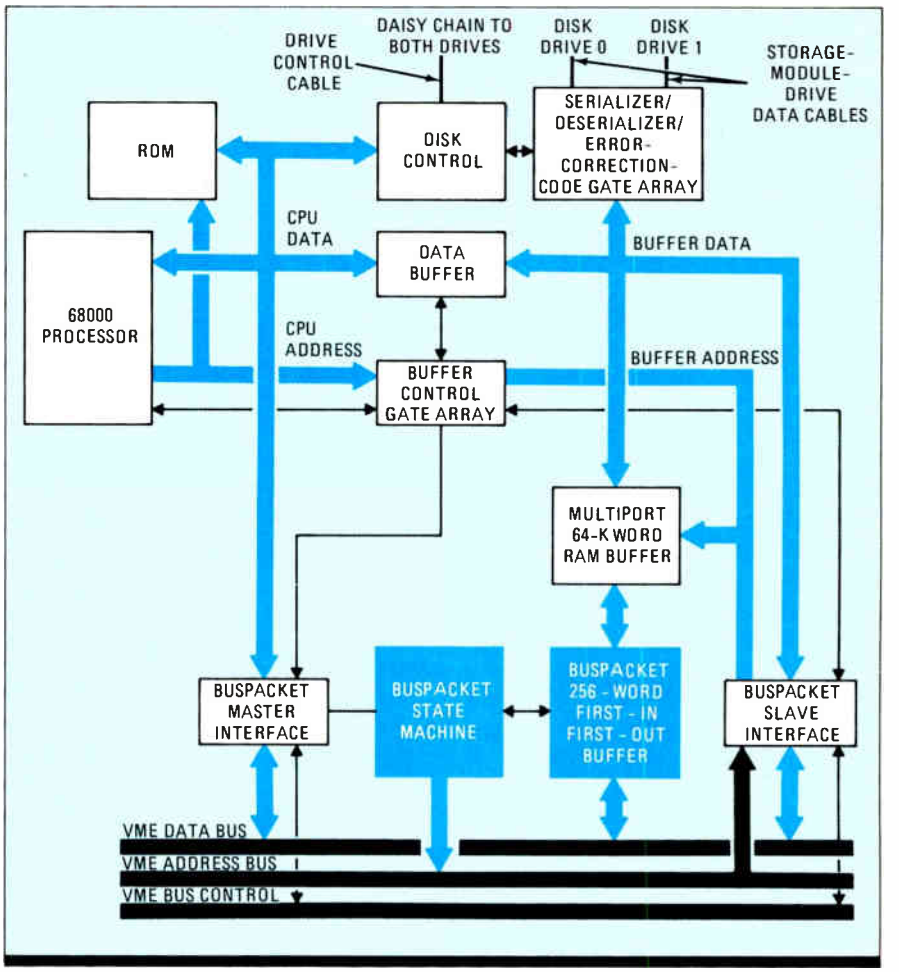
The BUSpacket's FIFO allows the use of slower RAMs and other components on the peripheral controller and interface board without affecting bus speeds. It also frees up the processor time that would be taken by transferring data directly to and from the VMEbus, thus netting more available computing power for the functions on the board such as the peripheral interface and virtual-buffering control.

The decoupling FIFO is made from 40-ns word-wide registers. The words are 2 bytes wide, so the FIFO can put out 2 bytes every 40 ns. But because the bus interface logic introduces delays, the transfer speed drops to between 30 and 33 megabytes/s.

A FAST STATE MACHINE

The asynchronous state machine in the BUSpacket architecture transfers data to and from the VMEbus considerably faster than the synchronous state machine in most architectures, including other VMEbus implementations. Traditional synchronous state machines run off the on-board clock or, alternatively, the bus clock. Running off a clock requires that all devices on the bus conform to the rated clock speed before accessing the bus.

Instead of running off a clock, the BUSpacket state machine runs off a tapped delay line and



2. NEW PARTS. A first-in first-out buffer for assembling packets plus a delay-line state machine dramatically upgrade the performance of this SMD disk controller.

bus signal transmissions. Metastable states common to asynchronous signaling are avoided entirely. At the same time, the delay-line state machine is not loaded with the wasted clock cycles that are tied to an arbitrary clock rate.

The delay-line approach takes better advantage of some VMEbus characteristics. For example, VME is an asynchronous edge-driven bus, so the tapped delay line can sample and set all edges at any time. This gives the state machine control over acquiring the bus and executing burst transfers.

Clock-driven synchronous state machines have finite times—the clock pulses—in which to sample the state. Then the machine has to wait for the next state to start transfering data. This procedure slows down the state machine, making it unable to transfer data as fast as the bus can accept and deliver it. The asynchronous state machine does not incur this penalty.

BIGGER BUFFER RAM

When an event such as the FIFO packet transmission occurs, the new state machine does not have to wait. It can synchronize with a clock so it can act immediately to sample and set the state of the bus and start the data moving. In other words, the delay-line state machine accommodates to the ever-changing bus timing without being constrained by fixed sample points.

To further push performance of the disk controller and to make room for enhancing its functions, Interphase's engineers increased the size of the multiport RAM buffer eightfold—from 16-K bytes to 128-K bytes. This makes available a larger pool of buffers for the controller's virtual buffering scheme as well as creating room for more elaborate caching schemes that can further improve performance.

Users of this product and others soon to follow will have no trouble seeing the current improvement in bus throughput, Cope says. "The FIFO and the new state machine make all the difference in the world. Users will stand up and notice because a 6 : 1 improvement in throughput is immediately noticeable on systems."

Interphase's designers did not have to use faster RAM chips with this new architecture. In the old controller design, the speed of the RAM was the limiting factor in holding the bus transfer speed down to 5 megabytes/s. In fact, the RAM chips used in Interphase's enhanced disk controller, the V/SMD 4200 Cheetah, are slightly slower than those used previously but have no effect on performance.

The first product to use the new interface is a speedier version of the company's Storage Module Drive disk controller. The V/SMD 3200, which runs at 5 megabytes/s, was the first high-performance 32-bit Storage Module Drive disk controller for the VMEbus and became the prominent one in the VMEbus marketplace, the company says.

The high-speed V/SMD 4200 Cheetah continues to offer such proven features of the original V/SMD 3200 as the multitasking virtual buffer architecture, intelligent caching optimized for AT&T Co.'s Unix operating system, and zero latency reading and writing. All this and high speed, too, will be available for $2,350 in 100-piece quantities. □

HOW A SMALL COMPANY'S IDEA TURNED INTO A BREAKTHROUGH

When Tom Thawley identified what could be a breakthrough in VMEbus technology, excitement raced through Interphase Corp. Thawley, who cofounded the Dallas company with Michael E. Cope in 1977, has the commonplace title of executive vice president but the rather unusual role of Interphase's floating creative engineering executive. Freed from everyday project demands, he focuses on the big picture in developing tomorrow's technologies.

Determined to gather elements of a potential new design that would significantly increase VMEbus throughput, Thawley locked himself in a room this past January to be isolated from distractions. Just days later, he emerged with some ideas.

Thawley, who holds a BSEE from the University of Maryland in College Park, showed his findings to Ed Gross, Interphase's peripherals engineering manager. Gross instantly recognized the potential of Thawley's suggested architecture. "It wasn't hard to see that this would create a new performance level for the VMEbus," says Gross, who has been with the company for two years and holds a BSEE from Carnegie-Mellon University.

LEADERS OF THE PACKET. BUSpacket designers Cantrell and Gross worked with Cope and Thawley (left to right).

Cope, as president of Interphase, is excited about the overall potential of the new interface. Cope, who holds a BSEE from Vanderbilt University, says, "this really sets the state of the art where it needs to be to realize the long-range potential of the VMEbus. And it is vitally important to protecting VME markets from competing buses in the future."

In fact, the BUSpacket interface came in part from Cope's urging that one of the primary concepts used in the Multibus II message-passing architecture be applied to the VMEbus. Thawley figured out just how to do it and the result is now ready to go to market.

Design engineer Craig Cantrell is responsible for much of Interphase's bringing the product to market ahead of schedule. Cantrell, who received his BSEE from the University of Texas at Austin, has been with the company for more than two years.

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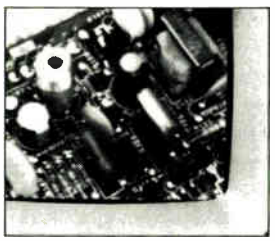

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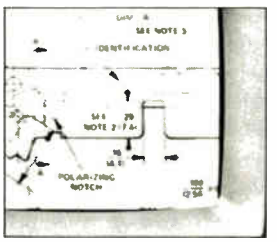

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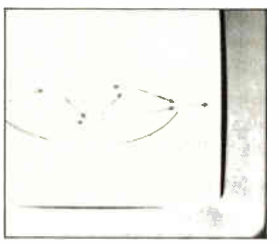

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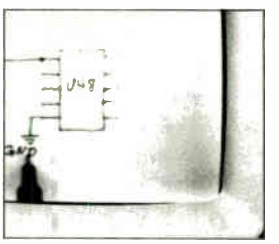

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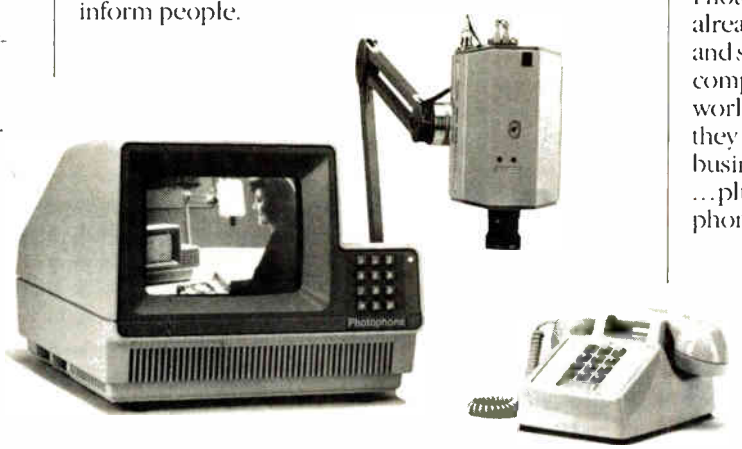

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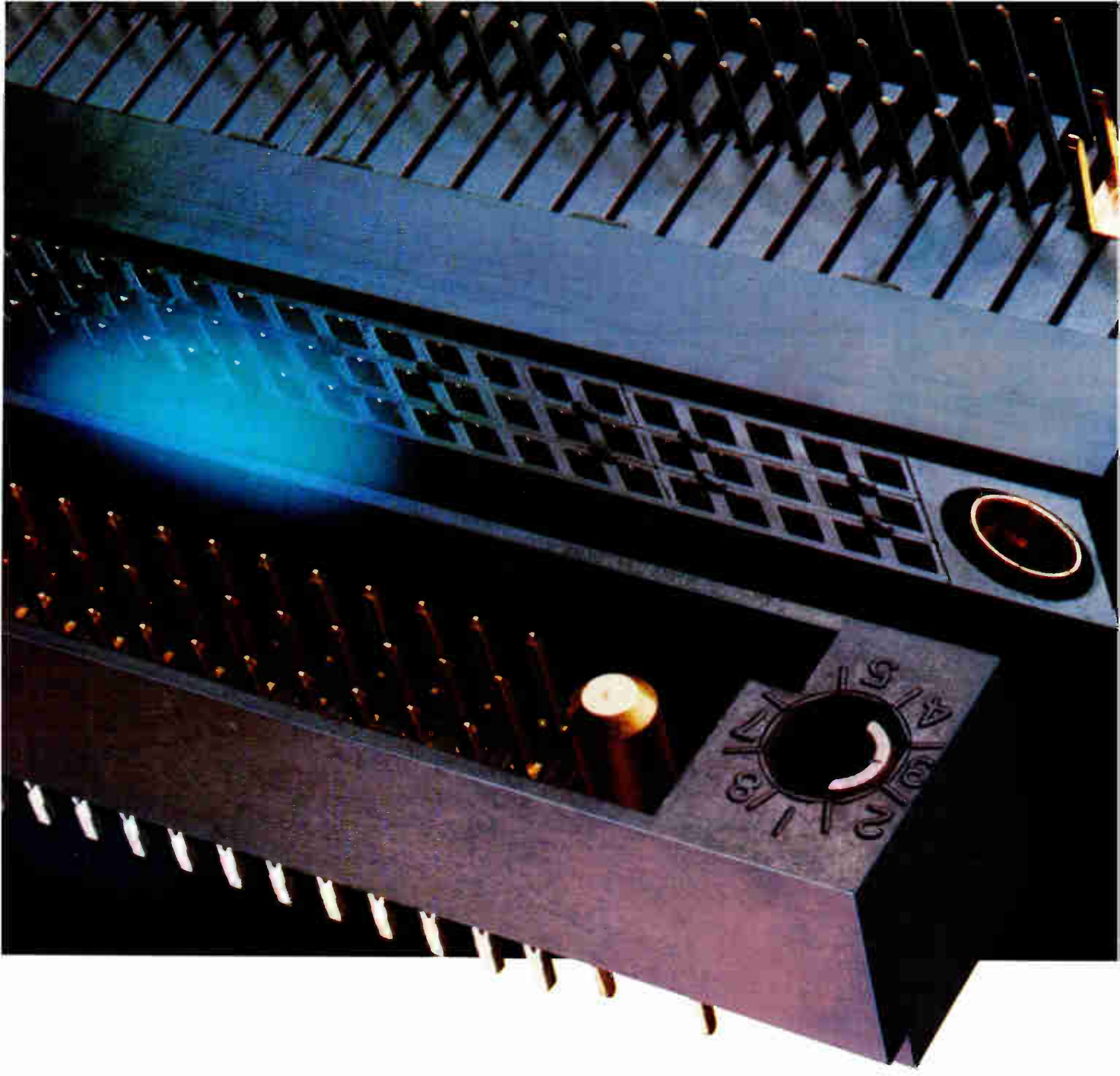

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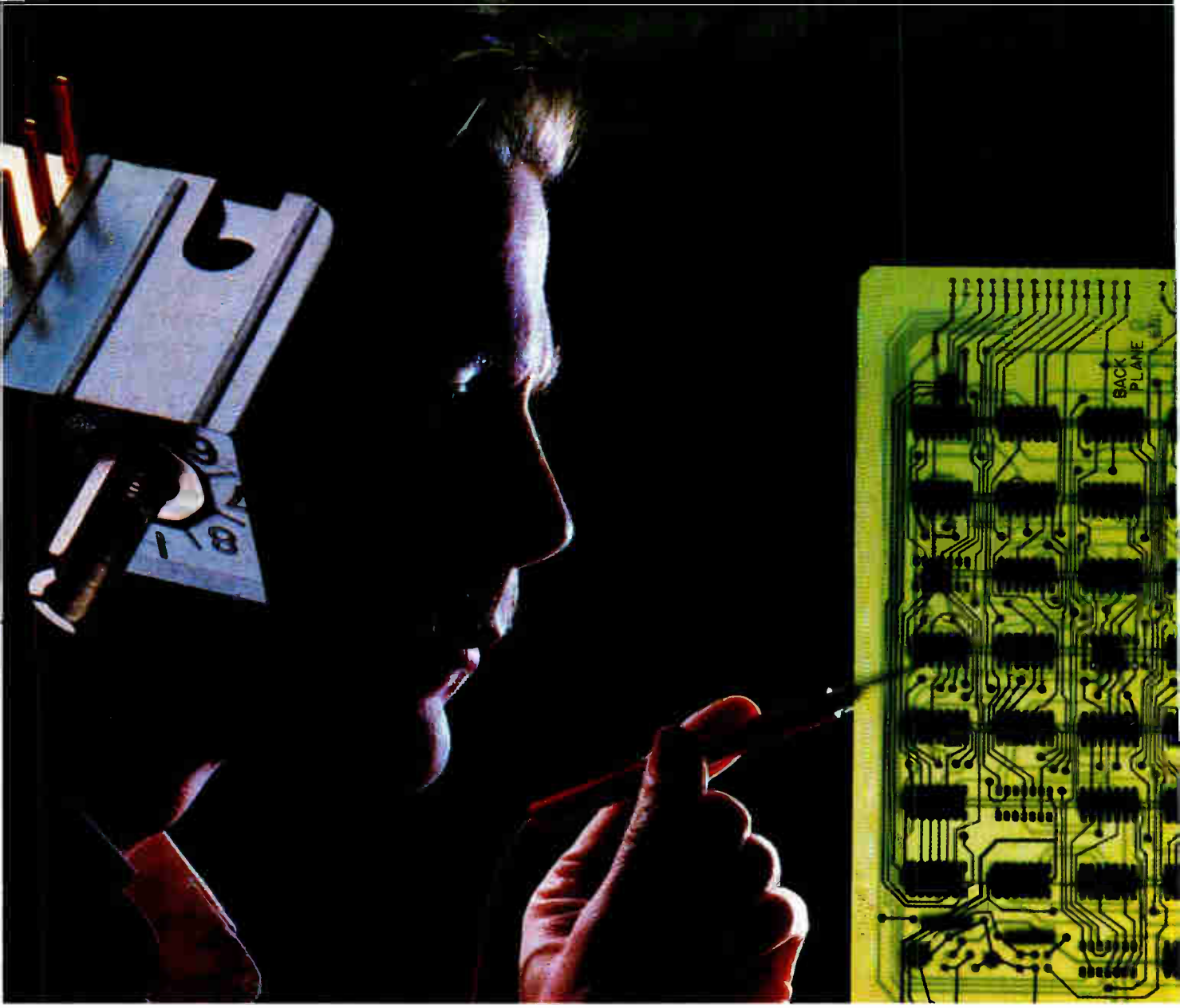

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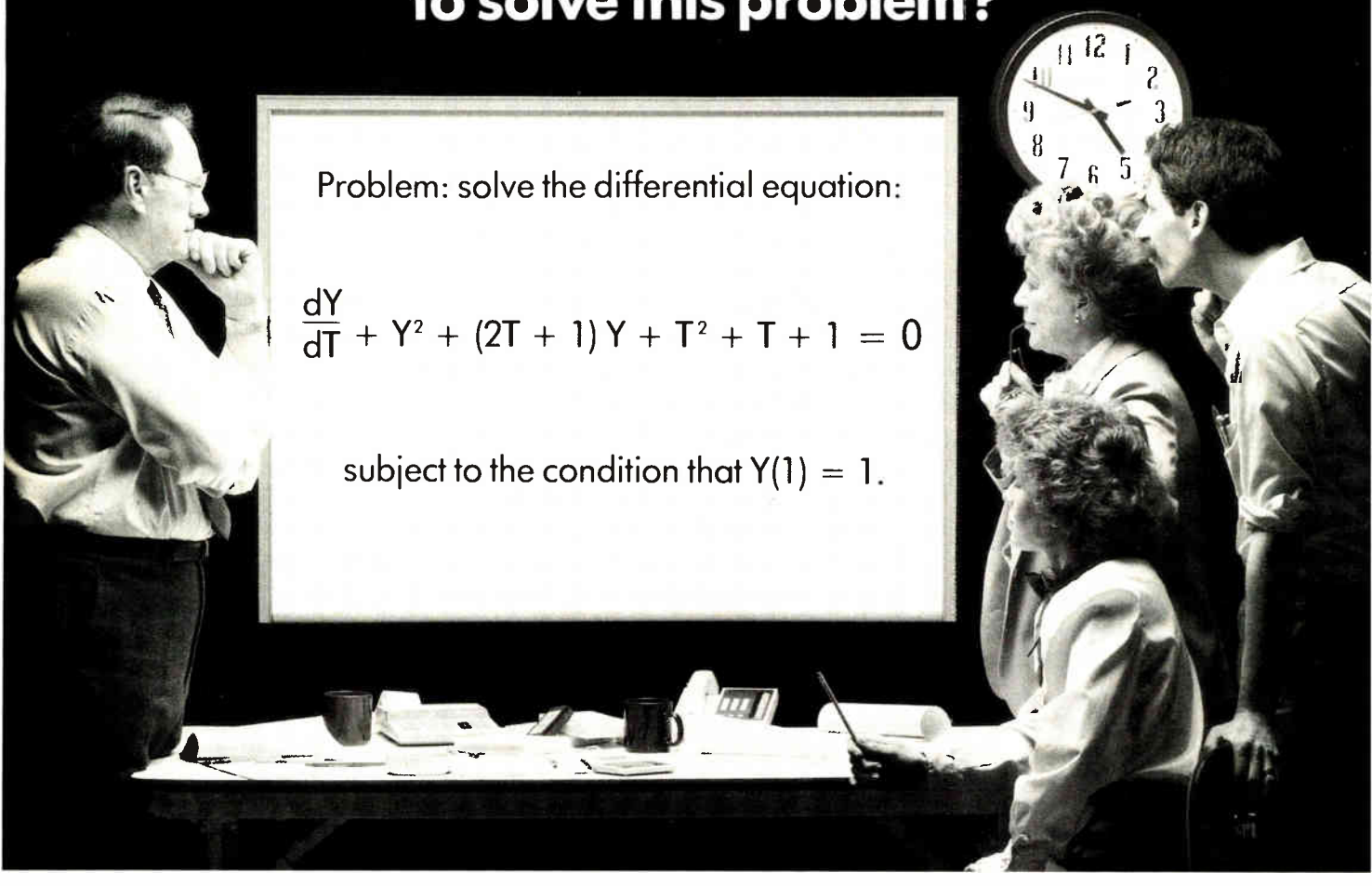

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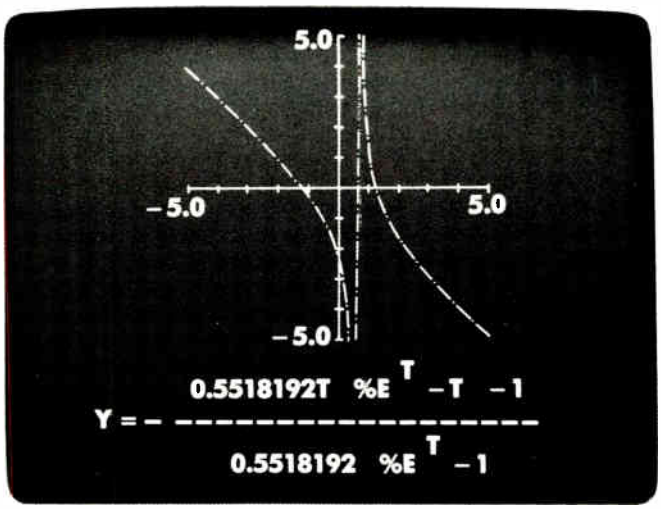
```
(C1) DEPENDS(Y,T)$
(D1)                          [Y(T)]
(C2) DIFF(Y,T)+Y^2+(2*T+1)*Y+T^2+T+1;
                    dY      2          2
(D2)                -- + Y  + (2T + 1) Y + T  + T + 1
                    dT
(C3) SOLN:ODE(%,Y,T);
                                    T
                             %C  T %E  - T - 1
(D3)                  Y = - ------------------
                                  T
                             %C %E  - 1
(C4) SUBST([T = 1,Y = 1], %);
                             %E %C - 2
(D4)                  1 = - ---------
                             %E %C - 1
(C5) SOLVE(%,%C),NUMER;
(D5)                       [%C = 0.5518192]
(C6) SPECIFIC_SOLN:SUBST(%, SOLN);
                                        T
                             0.5518192 %E  - T - 1
(D6)                  Y = - ------------------
                                  T
                             0.5518192 %E  - 1
```

In symbolic form.

```
(C7)  FORTRAN(%)$
      Y =  -(0.5518192*T*EXP(T) - T - 1)
     1          /(0.5518192*EXP(T) - 1)
```

In FORTRAN code.



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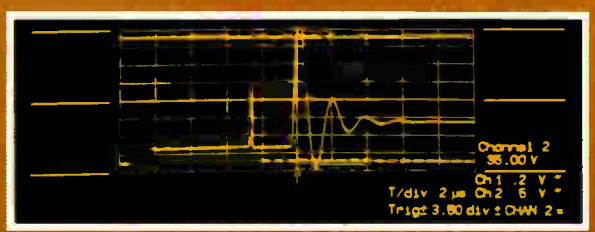

Top: Acquisition Parameters listing enables the 9400 user to precisely set and check front panel settings, all of which can be remotely controlled.

Middle: Window mode trigger set at ± 3,5 divs from center grid captures switching transient. 50% pre-trigger shows contact bounce prior to trigger moment.

Below: Crosshair marker, acting as a precise timer and DVM, gives time from trigger (arrow) and absolute voltage.

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HOW MOTOROLA MOVED BIMOS UP TO VLSI LEVELS

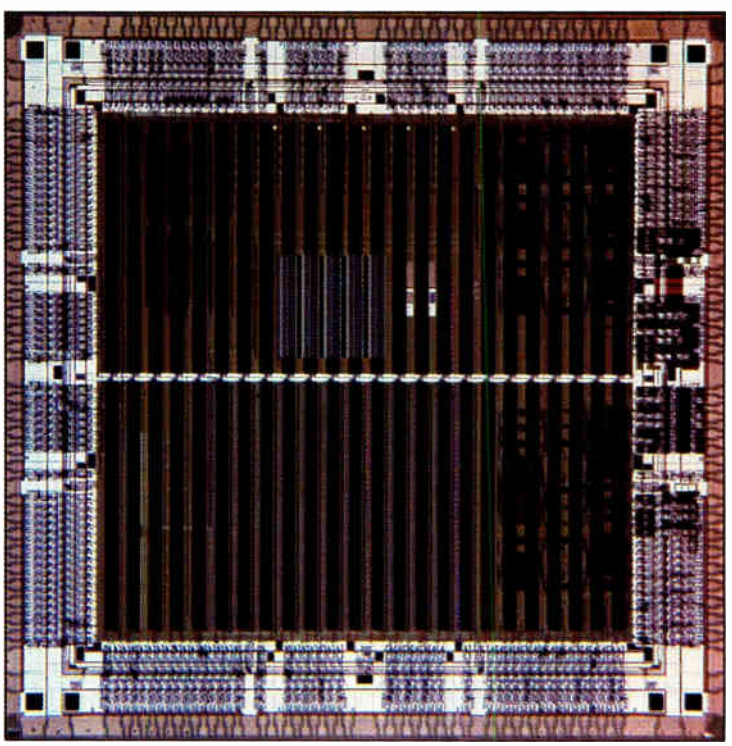
Mixing bipolar and CMOS structures for successful VLSI use flows from carefully working out the conflicting requirements of the two technologies

VLSI mixed bipolar and MOS technology is about to go commercial in the U. S. in a big way. Motorola Inc. is entering the market with a bipolar-CMOS very large-scale integrated circuit: the MCA6000ETL, a 6,000-gate array featuring an average gate-level power dissipation lower than that found in an equivalent bipolar or CMOS structure. For a two-input NAND gate with a load of 2 pF, for example, a BiMOS structure dissipates 50 μW/MHz versus 70 μW/MHz in a CMOS structure. What makes the VLSI MCA6000ETL possible is a careful working out of the conflicting process requirements of bipolar and CMOS technology.

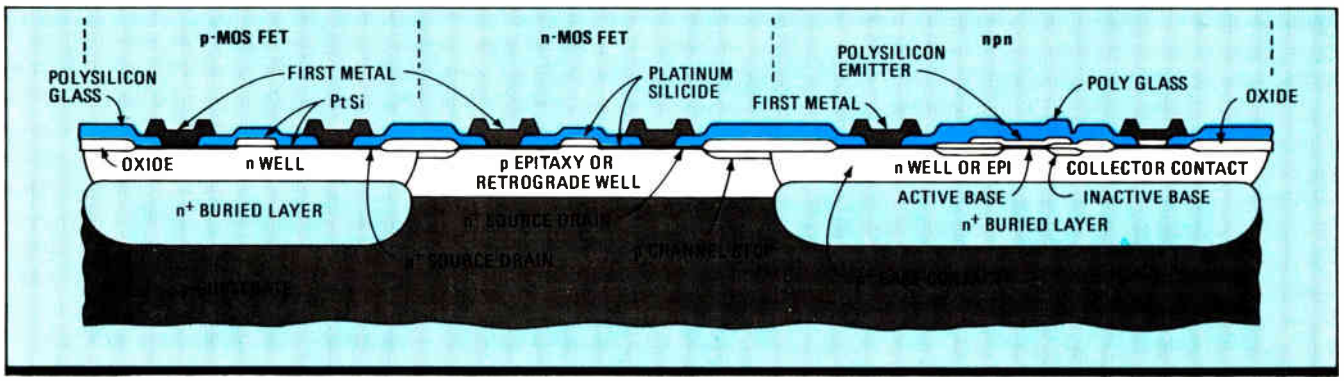
The MCA6000ETL is only the beginning, says Robert Jenkins, Motorola's vice president for technology development at the Semiconductor Products Sector, Phoenix, Ariz. The company plans to introduce a whole range of BiMOS macrocell gate-array products. It is also looking to apply the technology to standard cells, static random-access memories, and custom circuits in telecommunications, graphics, and tape and disk-drive circuits, as well as in consumer applications.

While there has been increasing interest in fabricating LSI and VLSI digital logic circuits by applying mixed bipolar and MOS processes, most commercial applications have until recently been the exclusive domain of Japanese companies. But now Motorola is challenging the Japanese.

Motorola's proprietary process (Fig. 1) merges a 2-μm n-well CMOS structure with a p-type epitaxial bipolar transistor featuring walled polysilicon emitters, says Patrick Hickman, bipolar semicustom design manager at the company's application-specific IC division in Mesa, Ariz. The MOS device incorporates silicided gate, source, and drain structures for reduced contact and drain-source resistance. The entire process, including two layers of metal interconnection, requires 14 mask steps, three of them for the bipolar devices. The chip architecture (Fig. 2) consists of an internal array of 3,072 basic macrocells containing both CMOS and bipolar devices, 1,400 dedicated wiring channels, and 202 input/output cells implemented in bipolar to pro-



1. BIPOLAR-CMOS. Motorola's 2-μm process with n-wells and silicide gates, drains, and sources merges CMOS and bipolar.



2. ARRAY OF 6,000 GATES. A BiMOS gate array from Motorola has 3,072 basic cells, 202 I/O cells, and 1,400 wiring channels.

vide TTL or emitter-coupled-logic compatibility or both, as well as a high off-chip drive capability.

Although the introduction of the BiMOS gate array represents the company's first attempt to use this technology in the digital VLSI arena, "it is not our first effort at mixing bipolar and MOS on the same chip," says Thomas George, vice president of the IC Wafer Manufacturing Group, Mesa, Ariz. "The technique is really far more flexible and adaptable than that [just digital applications] and has been applied within the company to a wide range of products, including discrete power transistors and analog circuits" [*Electronics*, Dec. 23, 1985, p. 35].

In general, Jenkins notes, the company's strategy is to offer BiMOS as one of a number of process solutions. "BiMOS is not being considered as a replacement either for MOS or bipolar but as an alternative and complement. There are places where neither CMOS nor bipolar is suitable, and a combination of the two, taking advantage of different characteristics, is the best fit."

Be that as it may, Kenneth Wolf, vice president and general manager of the division, argues that the application of CMOS technology to VLSI systems has been investigated intensively because of its inherent advantages: low power and high noise immunity. Yet CMOS circuits have only limited drive capability, which degrades performance in systems where signals frequently drive large parasitic capacitances. On the other hand, bipolar circuits can drive the capacitive loads with much less degradation of speed but can achieve only limited integration because of their higher power dissipation. By combining both technologies, designers can attain high output drive, reduced gate-interconnection delays, and lower power dissipation simultaneously.

WALKING A PROCESS TIGHTROPE

Developing a mixed bipolar/MOS process appropriate for digital VLSI applications involved "walking a tightrope, making tradeoffs between conflicting processing requirements," notes Hickman. "The idea was to retain the individual benefits of CMOS and advanced bipolar technologies, without compromising either and without increasing process-flow complexity too much."

In Motorola's approach, where the n-well or n-type epi layer serves as the foundation both for the npn bipolar and MOS transistors, most critical tradeoffs involved the n-well structure. In the p-channel devices, for example, the n-well concentration under the field oxide determines the parasitic field threshold, which in turn sets the minimum n-well impurity concentration deep below the surface. Punch-through voltage requirements also set a limit on the minimum impurity concentration. At the same time, the p-MOS FET's threshold voltage, set by a threshold-adjustment implant, limits the maximum n-well surface-impurity concentration.

Slightly below the surface, a lower level of doping is needed to minimize body effect, junction capacitance, and breakdown voltage. This combination of constraints sets a limit on the maximum concentration of bulk impurities. As a result, the n-well impurity profile is tightly bracketed, with only the threshold dosage open to adjustment by the process engineer.

Motorola designers also faced a number of constraints on the design of the npn transistors. To minimize high-level injection effects in the collector, Motorola uses a thin epi layer and a heavily doped n-well, limiting the doping level possible for a given collector current density. But such considerations conflict with the requirements for npn breakdown voltage and junction capacitance—requirements that demand a high level of bulk n-well doping.

Another problem that must be overcome with BiMOS is the collector impurity gradient, which can create excessive hole storage at the interface of the n-well and the buried layer. The bottom line on the npn structures, says Hickman, is tight bracketing of the optimal n-well impurity profile, with even fewer degrees of freedom available to process engineers than they could get with p-channel devices.

By contrast, n-channel MOS FET structures involve the fewest compromises in the BiMOS environment, he says. The one significant restriction is that the epi layer must be thick enough that autodoping and the n-well diffusion do not cause the bottom buried-layer-to-buried-layer boron channel stop to affect the n-channel device per-

formance. Though the n-MOS FETs are affected by the same restrictions limiting the p-MOS FETs, the impact is much slighter, because these characteristics are coupled only weakly to the n-well.

Motorola's BiMOS process attacks these problems on two fronts. Whenever possible, says Anthony Alvarez, staff scientist and developer of the process, it minimizes performance tradeoffs by merging process steps. The process also reconciles conflicting requirements by decoupling them during processing while adding as few process steps as possible.

This balancing of performance tradeoffs and conflicting requirements is accomplished using a 15-mask, 2-μm twin-tub CMOS process that is coupled to an n+ buried layer with a p-type epi layer, and three mask steps (an n+ buried layer, an inactive base, and an active base) combined with a silicided CMOS process that has a Schottky diode option for the npn transistors.

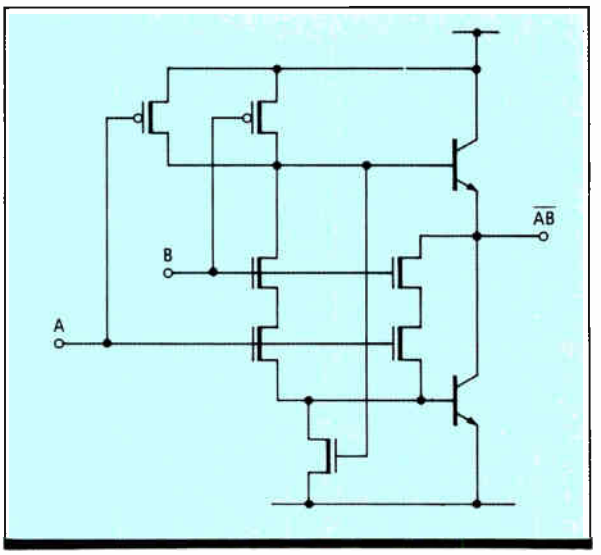
An n+ buried layer runs underneath the p-MOS devices to reduce latchup susceptibility. Though the n-MOS devices are built in the p-epi layer, an n-well diffused into the n+ buried layer serves as the foundation tub for both the npn and p-MOS transistors.

Motorola arbitrated the conflicting requirements in epi-layer fabrication—thin, low-resistivity layers for good bipolar performance versus thicker, higher-resistivity layers for good CMOS performance—by optimizing the n-well drive capability depending on the thickness of the epi layer, says Alvarez. The active base is formed in a way that recalls the n-MOS buried contact step, with the subsequent poly deposition simultaneously forming the npn emitter contact and the MOS gate electrodes.

The process is synergistic, a characteristic illustrated by the n-MOS source and drain implant, which also dopes the emitter, and the p-MOS source and drain implant, which also dopes the base contact. Another example is the platinum-silicon silicide layer, which reduces sheet resistance of the single-crystal and poly regions, while forming Schottky diodes in the lightly doped epi regions. Motorola uses two-layer metalization with a polyimide interlayer and metal pitches of 4 and 5 μm, respectively, on the metal layers.

The designers improved bipolar performance with a thin epi npn structure consisting of a very shallow poly emitter—oxide-walled on all four sides—with silicided sources, drains, and gates used to enhance MOS FET performance. They eliminated latchup by combining the thin epi layer with a retrograde-p-well structure, effectively shunting the parasitic well and substrate resistances that contribute to the problem.

The first array fabricated with this process, the MCA6000ETL, consists of 3,072 macrocells, organized in 24 rows of 128 cells each, connected by 580 first-metal and 896 second-metal routing channels. Usually, says Hickman, the fabrication



3. BIMOS CELL. In a BiMOS internal array, a basic macrocell can be configured either as a two-input CMOS NAND gate or as a one-input bipolar NAND gate.

of any logic circuit, including a macrocell array, imposes certain limitations on device sizing. These limitations create differences in the output impedance of various CMOS functions, and these differences in turn usually cut drive capability. In Motorola's BiMOS gate arrays, the basic transistors are configured as push-pull devices, which isolate the CMOS circuits from loading and therefore make the unit-load degradation both very low and essentially the same for all circuit functions.

Each of the internal array's 3,072 macrocells, containing both gate-isolated CMOS and bipolar devices, can be configured into a two-input CMOS NAND gate or one input BiMOS NAND. The BiMOS NAND gate (Fig. 3) was chosen for high perfor-

The BiMOS process minimizes tradeoffs in performance by merging process steps and reconciles conflicting requirements by decoupling them during processing

mance, low power, and ease of configuration. The circuit uses a pair of push-pull bipolar devices to provide the needed driving capability. However, the low power requirements of CMOS are preserved because the circuit draws no direct current. This allows any CMOS circuit to be modified into a BiMOS structure.

Because the MOS devices drive only local macrocell interconnections, not extended lines or fanout, sizes can be significantly lower than they would be in a purely MOS implementation. Moreover, the performance of mixed-process BiMOS structures is a good deal better than that of CMOS devices of comparable size. For example, while a BiMOS NAND using 30-μm p and n devices

is about the same size as conventional CMOS NANDs made of 60-μm p- and n-channel devices, it will outperform them on all loads above 0.3 pF. Up to loads of 0.3 pF, the CMOS circuit is marginally faster than the BiMOS implementation. In medium to heavy loading conditions—from 0.3 to 4 pF—the BiMOS circuit is two to four times better than CMOS.

The bipolar push-pull devices isolate the CMOS circuits from the loading, so the unit load degradation is the same for all circuit functions. In addition, dissipation is lower than in an equivalent bipolar circuit, and average dissipation is even less than in an equivalent CMOS gate. There are two reasons for the low power dissipation. First, diffusion capacitances are smaller than in CMOS circuits of comparable area. Second, the fast edge rates of BiMOS under loading conditions reduce the through current component, a significant element in CMOS circuits.

To take full advantage of the BiMOS array, the bipolar I/O cells come in either TTL or ECL, as well as in a mixed TTL-ECL mode, and are configurable as inputs, outputs, or bidirectional pins. This combination produces a range of speed and power-dissipation options unmatched by either bipolar or CMOS implementations, says Hickman. For example, in an all-TTL mode (100 high-impedance inputs and 100 outputs), the MCA6000ETL features output delays of 5.5 ns and an active power dissipation of 1.7 W at 50 MHz. In an all-ECL mode with 100 inputs and 100 outputs, output delays are reduced to 1.5 ns, with a total dissipation of 4.7 W. In an all-ECL mode with 150 inputs and 50 outputs, dissipation is cut to no more than 3.3 W. Finally, in a mixed mode (50 ECL inputs and outputs and 50 TTL inputs and outputs) operating with 1.5-ns delays on the ECL outputs and 5.5-ns delays on the TTL outputs, dissipation remains reasonably low: 3.3 W.

SUBMICRON BiMOS COMING

Currently under development and scheduled for introduction later this year are a number of follow-ons using the same 2-μm BiMOS process, says Hickman. They include the MCA6000ALS—identical in configuration to the MCA6000ETL except that its die size is smaller and it is limited to TTL on inputs and outputs—and the MCA3000-ETL, with half the number of configurable ECL/TTL I/O lines.

A 1.5-μm version of the BiMOS process will be used early next year in two additions to the macrocell family: the MCA10000ALS, with 10,000 internal and 220 TTL I/O cells, and the MCA6000-RAM, with 6,000 internal gates, 200 reconfigurable TTL/ECL cells, and 4-K of reconfigurable static RAM with single, dual, or triple port capability.

Motorola is also working on a submicron version of the BiMOS process, which should almost double gate density and further reduce both gate and output delays. Also under investigation is the replacement of local-oxidation isolation techniques by some form of trenched isolation.□

'IN THE MIXED-PROCESS WORLD, EVERYONE'S ON A FIRST-NAME BASIS'

Even among the select group of engineers skilled in developing mixed bipolar and MOS digital VLSI circuits, Anthony Alvarez, staff scientist at Motorola's Bipolar Technology Center, Mesa, Ariz., is a rarity. He has worked on nothing but mixed processes since joining Motorola in 1979 after earning his BSEE and MSEE from the Georgia Institute of Technology. The process used in the MCA6000ETL is the third generation of digital BiMOS processes that he has worked on at Motorola.

"When I started at Motorola, fewer than half a dozen people at the company were involved in mixed-process development," says Alvarez. "And around the world, there could not have been more than five or six centers, academic or industrial, involved in similar efforts." Though the number of engineers involved in such efforts has increased by several orders of magnitude, Alvarez says there are still relatively few: "Everyone knows everyone else on pretty much of a first-name basis."

In the MCA6000ETL project, Alvarez worked with some relative newcomers to BiMOS: Patrick Hickman, design engineering manager for gate arrays; Frank Ormerod, design manager for BiMOS; and Douglas Schucker, ASIC LSI design engineer. Hickman received his BSEE degree from Purdue University in 1977 and joined Motorola immediately thereafter. Ormerod received his BSEE from Strathclyde University, Glasgow, Scotland, in 1979, working at STL Research Laboratories in Harlow, England, for five years before joining Motorola. Schucker received his BSEE degree from Pennsylvania State University in 1982 and has worked at Motorola since graduation. Hickman, Ormerod, and Schucker all have extensive experience in the design of gate arrays.

GOOD MIX. Motorola's BiMOS development team, clockwise from top left, includes Ormerod, Hickman, Schucker, and Alvarez.

As geometries move below 1 μm and the advantages of mixed bipolar-CMOS processes become more obvious, Alvarez expects the tight BiMOS community to expand dramatically. "There is still a substantial difference between the way you build CMOS and bipolar structures. As a result, mixed-process circuits are still more expensive and implemented only where the performance merits it. However, as we move below 1 μm, these differences become negligible." Alvarez believes that at the VLSI level, BiMOS will emerge as a mainstream process used to fabricate a wide array of products including standard-cell ASICs, structured custom circuits, static RAMs, and even microprocessors.

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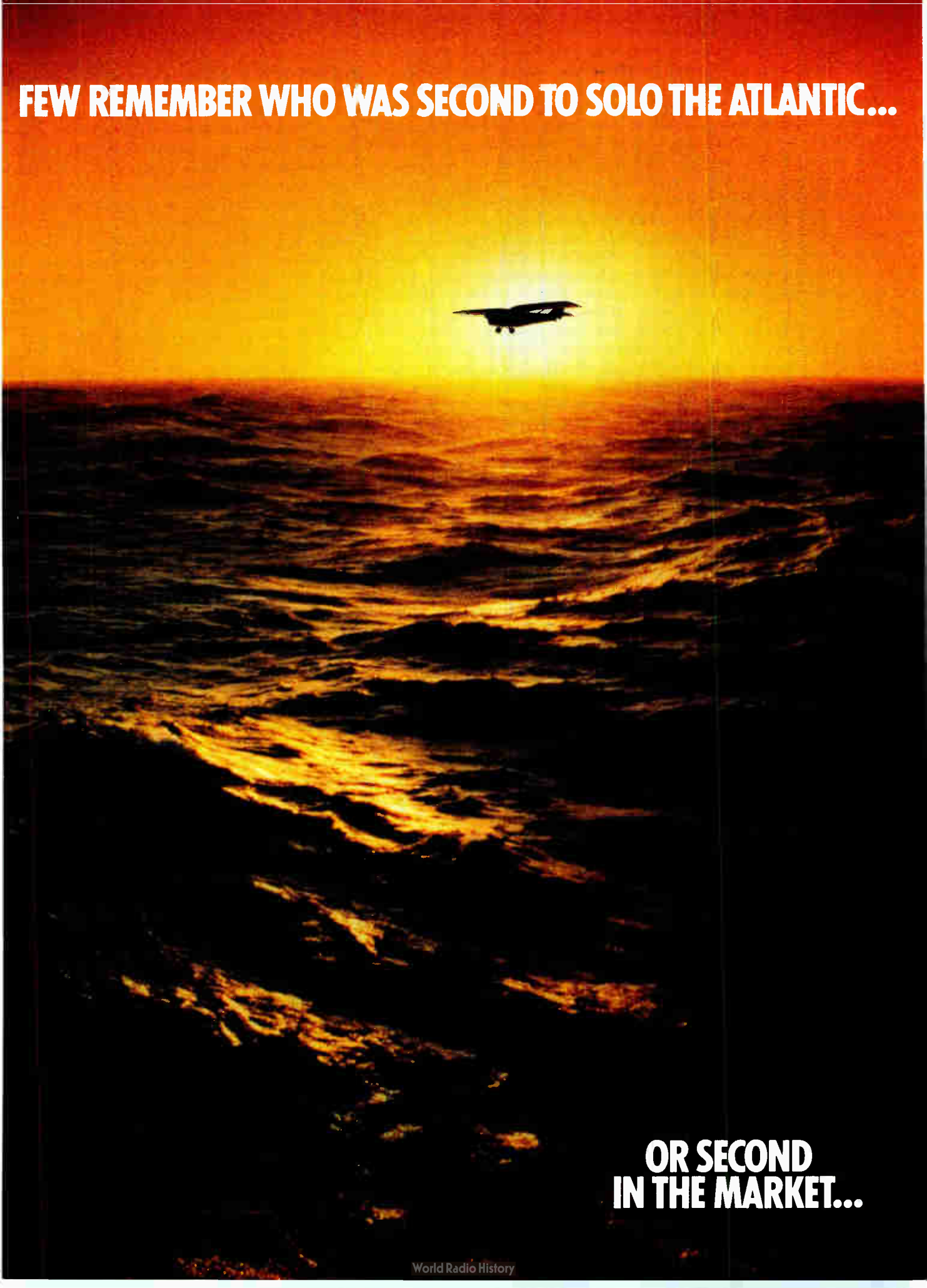

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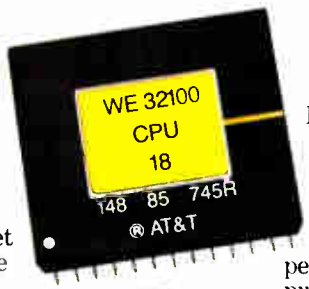

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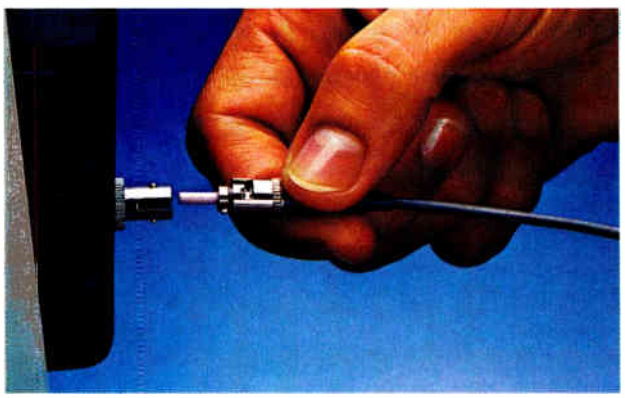

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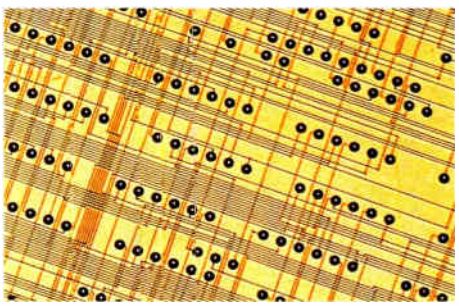

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INTELLIGENCE COMES TO LASER SOLDERING

Vanzetti Systems says its ILS 7000 series will make perfect solder joints every time, thanks to an IR monitor that checks thermal signatures against those in memory

Surface mounting and very large-scale integration have hiked dramatically the density of printed-circuit boards. The ultradense boards now in production carry expensive parts that can be damaged by the soldering process, resulting in costly rejection rates. Vanzetti Systems Inc. claims it has solved this problem with a family of intelligent laser soldering systems that produce perfect joints every time by adjusting the heat they deliver to individual joints.

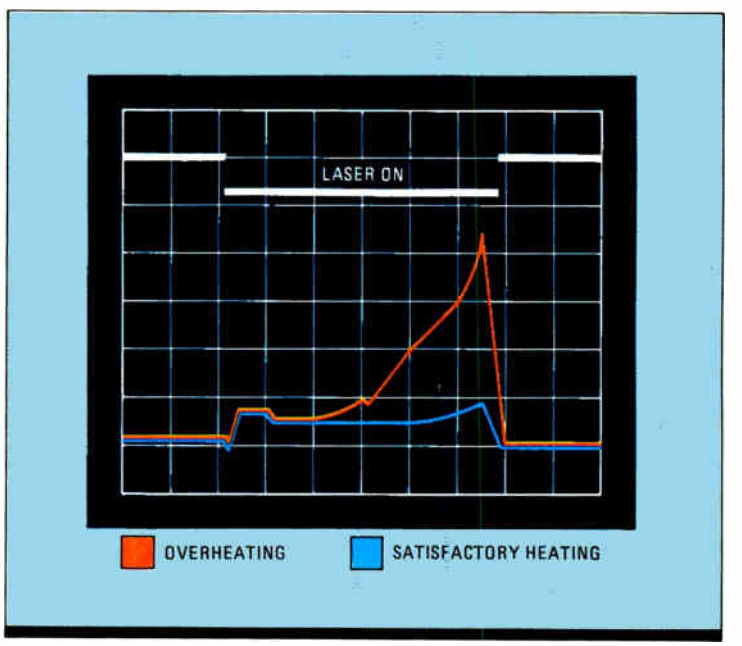
The Stoughton, Mass., company calls its ILS 7000 series of soldering systems intelligent because they use an infrared detector and minicomputer system to monitor and control the laser soldering process. The IR detector monitors the formation of each joint as the laser heats the solder to its melting point and beyond. The detector senses when the optimal solder-joint temperature has been reached—where the solder just becomes molten—and triggers control circuitry that closes a laser shutter.

Vanzetti Systems says its intelligent laser soldering provides several major benefits. For one, the prospect of product damage is virtually eliminated. Also, users can check a joint's formation as the solder process proceeds, eliminating the need for a separate inspection step. Finally, data gathered during the soldering process can be used for immediate process control to track down the cause of solder abnormalities and correct them systematically.

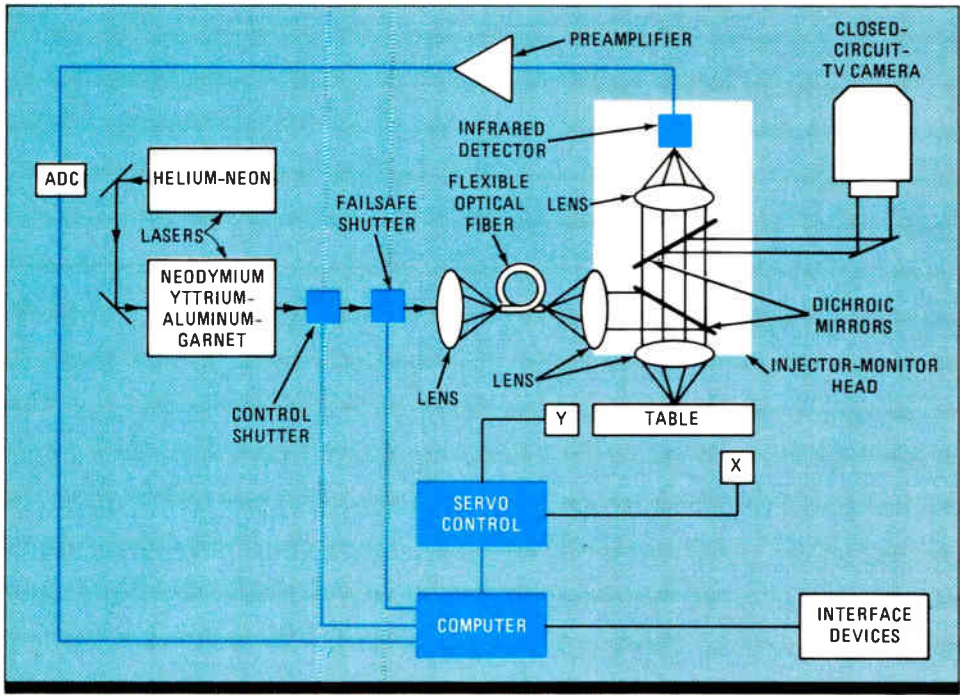
These advantages may well turn into necessities with the advent of extremely dense surface-mounted pc boards. Some board assemblers have already ruled out conventional soldering methods such as IR and vapor-phase reflow for surface mounting, pointing to an unacceptably high level of joint rejects.

Joints done with the vapor-phase or IR reflow method often exhibit undesirable large-grain recrystallization because of the reduced solder mobility at low temperatures and because of the length of time required to cool the joint through the solidification process. In addition, both techniques hold circuit components and boards just above the solder's melting point for several moments, compromising their long-term reliability.

Laser soldering systems do not encounter these problems. Based on carbon dioxide or neo-



1. TIME BASED. The infrared signatures of solder joints with identical laser exposure times show overheating in one. The cause is insufficient solder.



2. SIGNING OFF. In Vanzetti's laser soldering system, an IR detector senses the optimal joint temperature to trigger the laser's shutter when the solder becomes liquefied.

dymium yttrium-aluminum-garnet lasers, these systems afford higher heating rates but use optics to focus the beam only on the solder joints. Boards and components are spared from heat, improving long-term reliability.

In addition, air quenching follows the heating process in laser systems, producing finer-grained, stronger solder joints than can be achieved by either the vapor-phase or IR techniques. The speed of joint formation with laser soldering virtually eliminates intermetallic layers, resulting in solder joints that are less brittle and more ductile.

Nonetheless, appropriate control of the laser is required. Soldering of two nominally identical joints, laser-heated for the same period of time without intelligent feedback, can produce a normal joint in one case and board damage in another (Fig. 1).

Conventional laser soldering systems apply the same amount of heat to each task regardless of the joint-to-joint variations that occur in the real world of board assembly. That means some joints with excess solder or slightly larger surface dimensions won't reach the necessary solder-melting temperature and become cold solder joints. On the other hand, joints with below-average solder coverage, slightly smaller dimensions, or both, are vulnerable to overheating, which can damage a lead, the component, or burn up very expensive boards.

The ILS 7000 series enables a user to thermally characterize the work to be performed based on the usual conditions that will be encountered in a normal solder joint for a specific application. The characterization process takes into account the geometry of the solder joint under test; the mass of the solder, lead, and pads; the heat sinks that may be attached to the pads; and the surface condition of the target. The system is taught to understand the typical thermal-signature variation—the radiation versus time profile—that may be expected. Time limits and thermal thresholds are set up for each type of joint.

By monitoring the amount of available solder, the Vanzetti systems deliver precisely the correct amount of laser energy to form an optimal joint. Comparing the thermal signature of each solder joint to preestablished norms thus makes it possible to flag abnormally formed solder joints. The X-Y coordinates of abnormal joints then are stored in the computer's memory for later reporting or retrieval.

The key building blocks of the 7000 series are a helium-neon laser used for accurate positioning; a dual-shuttered Nd:Yag laser with a typical output power of 12.5 W and a minimum spot diameter of 24 mils for soldering; an IR detector; a servo-controlled positioning table; a computer based on a Digital Equipment Corp. PDP 11/23 minicomputer; and precision optics (Fig. 2).

The systems are designed to work with components that are precluded from a mass-soldering process. The leads of these components must be prepasted to pads. For example, temperature-sensitive components that would not withstand either the heat levels of vapor-phase or IR reflow processes must be attached after these tests have been completed. Also, parts missing at the time of the initial soldering must be attached without reflowing all other joints on the pc board.

IR 'EYE' RUNS JOB

During soldering, a component-laden pc board is inserted into the system's chamber and attached to a fixture plate. Then the positioning table moves to a programmed location and stop. The control shutter then opens, allowing focused laser energy to irradiate the target. At the same time, the IR detector views the target, determines when the solder liquefies, and sends a control signal to close the shutter. The table then proceeds to the next target.

The computer records critical measurements taken during the soldering operation, printing reports that detail abnormal joints and storing

information in its data base for later retrieval. The finished board then passes to an external defect-marking system or rework system. Here the data base would be interrogated and the defective joints either marked for future rework or reworked immediately.

The Vanzetti soldering systems can be used on pretinned parts and with solder forms. They can be applied to most chip packages, connector lead configurations, and passive surface-mounted components. To date, soldering has been done on 12-mil leads on 40-by-100-mil pads and 28-mil lead wire in 37-mil-diameter plated through holes, according to the company.

Soldering speed ranges from 50 to 150 ms. Soldering a small-outline integrated circuit, for example, takes 100 to 150 ms per lead. In a connector-soldering application, the soldering rate was five joints per second.

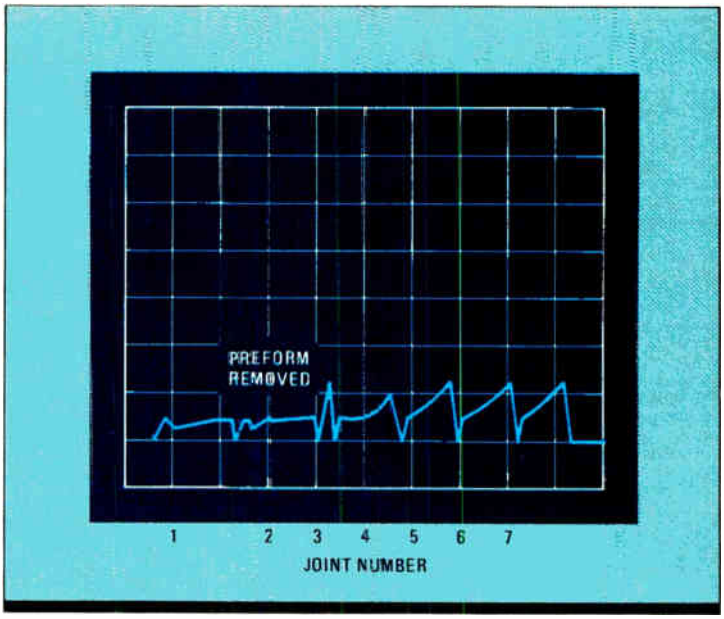
CHARACTERIZATION ON THE FLY

In another case, a Vanzetti system demonstrated its ability to characterize abnormalities when it soldered seven pins on a pc-board connector. It monitored the formation of these solder joints, compared them with the limits established, and found a wide variation (Fig. 3). In joints 1 and 2, the proper thermal level was not reached in the allotted time, so the laser heating was terminated and an abnormal flag set. The cause of the trouble probably was excess solder.

In joint 3, the shutoff thermal level was reached too quickly and laser heating terminated. Again, the abnormal flag was set. The cause of the trouble was determined to be the absence of solder.

Joints 4 to 7 were normal. The thermal shutoff level was reached within acceptable time limits and laser heating terminated.

In practice, Vanzetti's engineers say, soldering is a function of the solder paste type, component type, and the pc board's layout and construction.



3. THERMALLY MONITORED. The monitoring of seven identical joints revealed the probability of excess solder in the first and second joint and the absence of solder in the third.

In a board they encountered having three identical pads, one pad showed a radically different thermal signature. The abnormal signature was caused by a missing via.

The Vanzetti units are ready for delivery and start at slightly more than $200,000 for the fixed-head 7005. Rounding out the series are the 7010, which features a tilting head, and the 7012, which has a tilting head and a larger bed. Vanzetti says considerable interaction will be needed between the machine supplier, paste manufacturers, and the equipment users before optimal thermal signatures can be set up for each application. Also critical are the conductor pattern of the pc board, the type of IC package used, and whether through-the-board assembly or surface mounting is used. □

IR EXPERTISE LEADS TO IMPROVED LASER SOLDERING

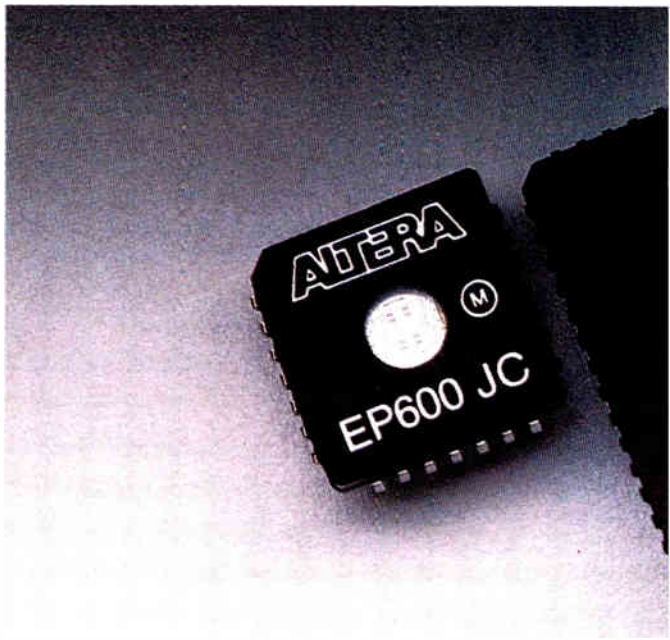
Riccardo Vanzetti came up with the idea for the ILS-7000 in 1982, when Vanzetti Systems Inc. introduced its Laser/Inspect. That system used lasers to illuminate solder joints on printed-circuit boards, thereby generating infrared signatures that were used to check the quality of joints on a production line. The company founder noted that with a higher laser power level, the same principle of operation could be extended to create optimized solder joints.

He assigned chief operating officer Ashod S. Dustoomian to guide the IR-based intelligent laser solder program through development. Dustoomian, who helped found the Stoughton, Mass., company in 1968, is the originator of numerous inventions in both IR instrumentation and applications. His awarded or pending patents include an IR temperature probe for high-pressure use, means for detecting changes in skin temperature, a band-ratio radiometer, a method of controlling quality in spot-welding operations by means of phosphorus and IR thermal sensing, and a laser system for automatic solder-joint inspection.

DUSTOOMIAN: An old hand at IR work.

"Our biggest problem in the development of the laser solderer was to identify the proper thermal characteristics of a good solder joint," Dustoomian notes. He believes this unit will raise solder-joint yield considerably over existing methods, along with radically increasing quality and lowering inspection costs.

Immediate



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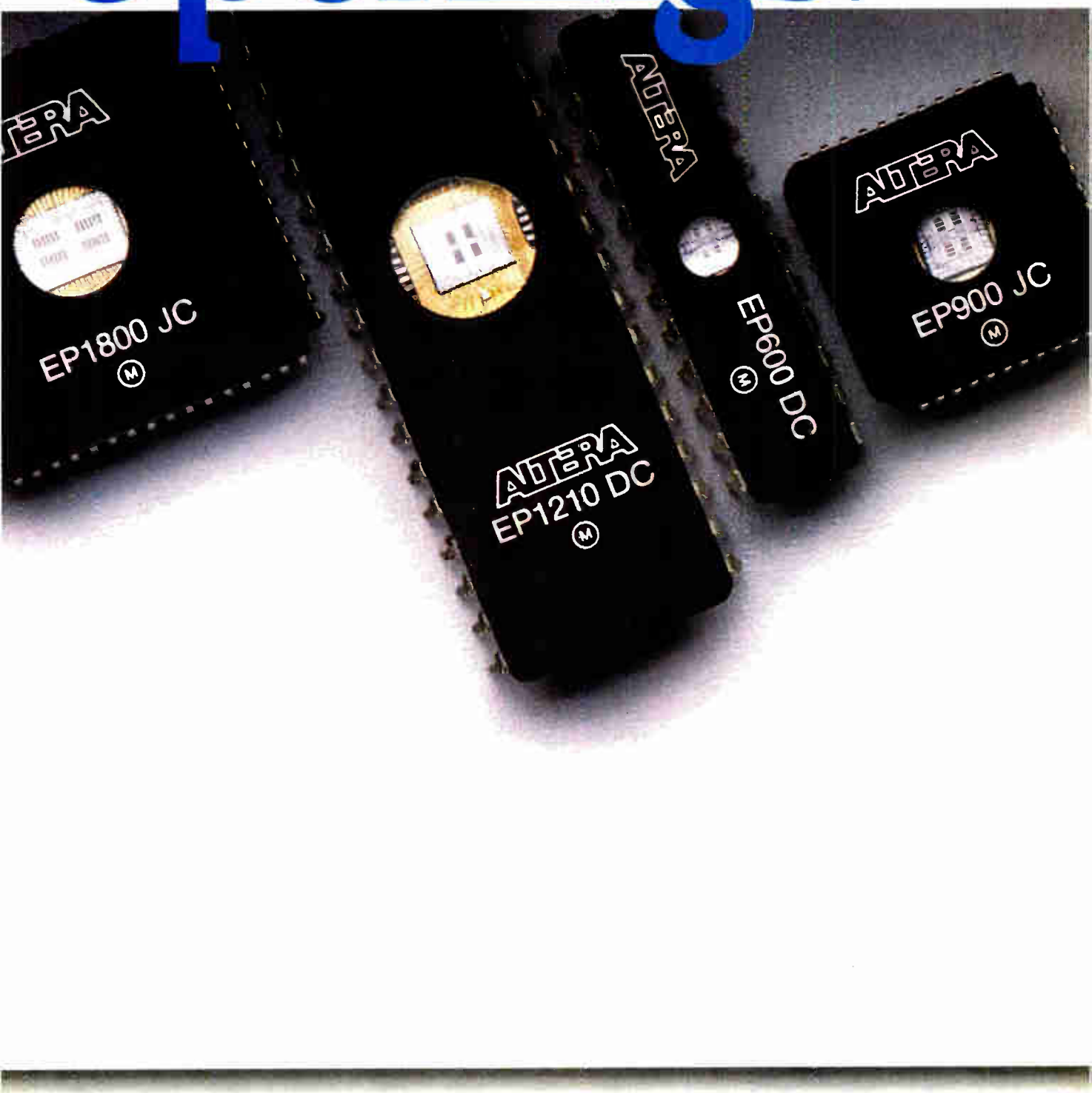


SOFTWARE PRODUCTIVITY MOVES UPSTREAM

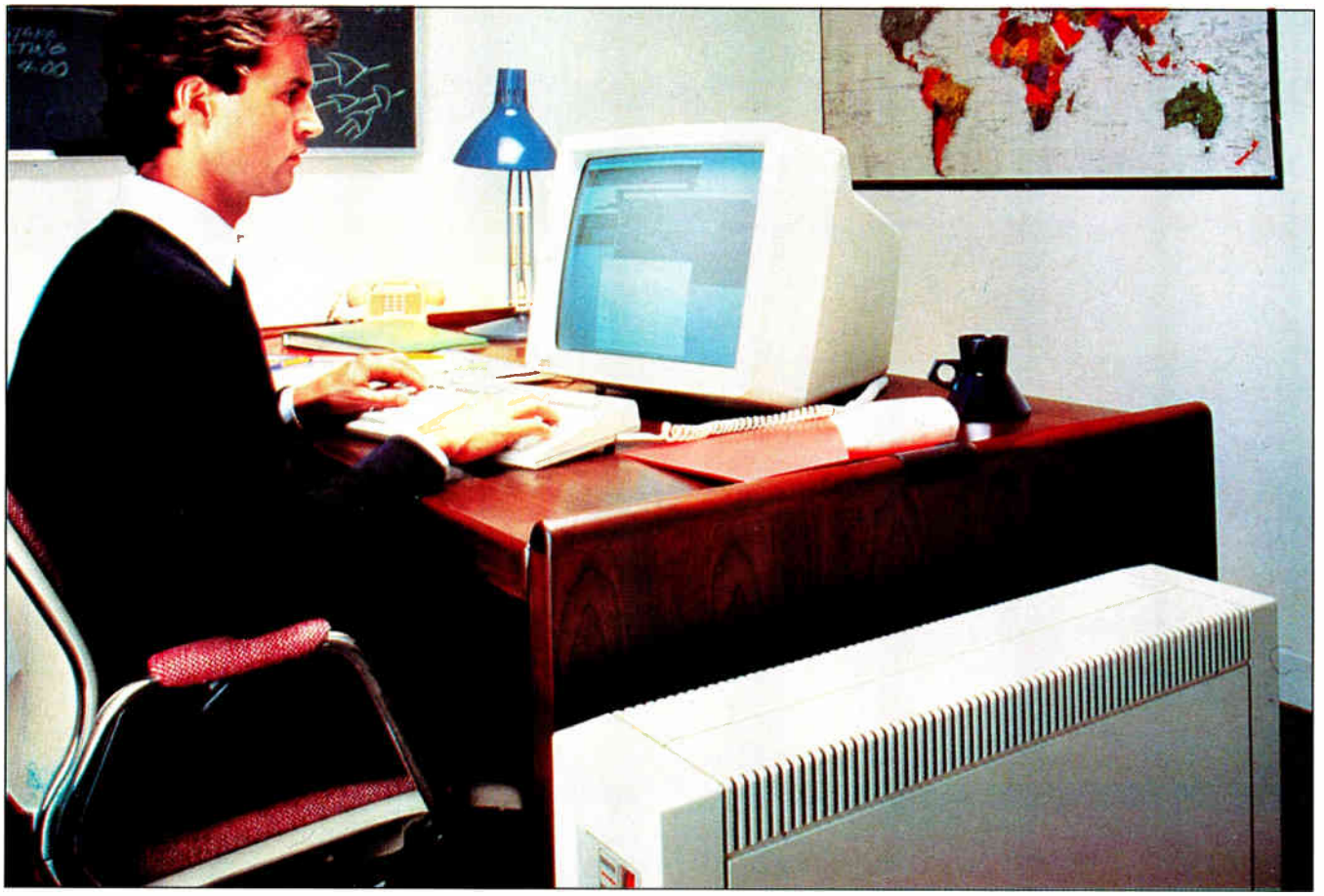
New tools are aiming to automate the entire software life cycle. Right now, automating such tasks as requirements analysis and design pose the greatest challenge

by Alexander Wolfe

Large-scale software projects are still very much hit-or-miss propositions. The reason: though many tools have been available to assist programmers with the downstream, or coding, portion of software development, little help has been around for the more abstract upstream tasks, which demand that software engineers analyze requirements, develop specifications, and come up with workable designs.

"What we have been doing in the large-system area has been by the seat of our pants," declares Laszlo A. Belady, vice president and program director of software technology at the Microelectronics and Computer Technology Corp., Austin, Texas. "Even after 30 years of research, more of the efforts have been directed towards programming," which falls in the downstream area of the software life cycle.

Today, however, many groups are beginning to tackle the upstream problems of software development. They're also taking a big picture approach, hoping to tie together a full range of



ON THE WAY. Programmers will soon be getting help with abstract upstream software-development tasks, such as requirements analysis.

tools to manage projects throughout the entire software life cycle—from its start through its maintenance. High-profile efforts to improve the software-development process—by such research groups as the MCC and the federally funded Software Engineering Institute, as well as by such major corporations as Lockheed, TRW, and IBM Japan—include a work-station-based software-development environment, a generic set of development tools called the software factory, a knowledge-based tool that automatically generates documentation from source code, and a cost model that helps manage software-development projects. Though some of the work is just gearing up, it is sure to have a major impact on software development in years to come.

In late 1984, the MCC's software technology group embarked on the ambitious Leonardo (for Low-cost Exploration Offered by Network Approach to Requirements and Design Optimization) project. Like other MCC projects, it targets the upstream portion of software design. The goal was to develop a complete environment for a team of software engineers to use in designing large software packages of the highest complexity—programs for real-time, embedded, distributed software systems.

The Leonardo environment will be a networked work-station-based system for use in the early stages of a system's design. Through the work stations, software engineers will have access to knowledge bases containing extensive expertise on software development in general as well as on the software project under development. That information will be continually updated as a project progresses to help manage the task; it will also monitor the work stations and automatically determine what activities it should initiate.

"The whole architecture is centered on an information data base, and attached to it is what we call a progress promoter," says Belady. The progress promoter is a large module that manages the Leonardo's activities. For example, it will decide whether there is source code that has to be compiled or whether it must provide information in response to a question asked by one of the software engineers.

The Leonardo system goes beyond the two-dimensional interface of standard work stations. It will support voice communications, provide an electronic blackboard to allow engineers to draw diagrams for one another while sitting at their own computers, and even accept video inputs.

BELADY: The head of the Software Technology Program at the MCC wants to see more effort spent on upstream programming.

One of the best ways of communicating in software design is to use scenarios, or storyboard-like renditions of a complicated design procedure, says Belady, adding that video scenarios could well become part of the knowledge base at the center of a Leonardo-based system.

Though conceived originally as an eight-year project, Leonardo is now open-ended. MCC's 10 sponsoring shareholders have already begun to receive formal transfers of spinoff technologies from the effort. And the MCC's software group is now looking at creating a Leonardo kernel project that could make a subset of the full system available, on a widespread basis, before completion of the project.

'What we have been doing in the large system area has been by the seat of our pants,' and automation of the upstream tasks have been neglected

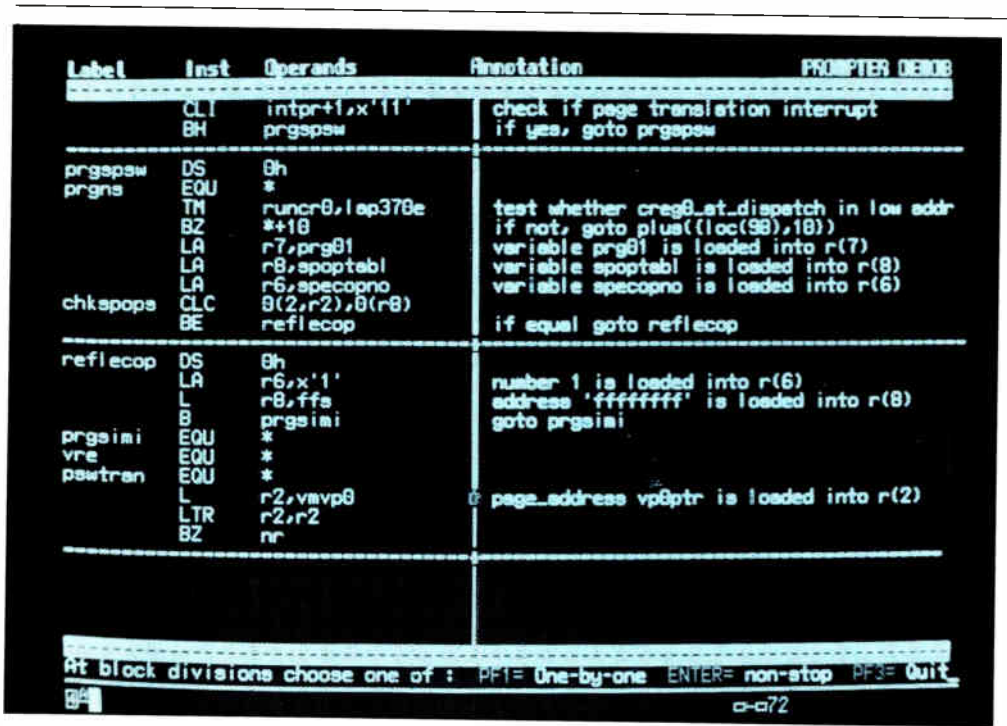
"The Leonardo environment is designed to take on more machine-activated progress as time goes on," says Belady. "So even a system with little machine intelligence today could be helpful in the early stages of software design."

All told, the MCC's software technology program consists of four subgroups: architecture, design information, design process, and design interface. The architecture subgroup is developing the modules of the Leonardo prototype design system.

The design information subgroup is attempting to represent information and software engineering know-how in knowledge bases. They are also researching distributed systems.

The MCC's design process subgroup, which is theoretically oriented, is trying to understand what the software design process really is. To this end, it is tracking existing design technologies under way in other research groups. And the design interface subgroup is working on graphics interfaces and exploring the use of animation and other ways of synchronizing designers on massive projects.

A different type of software-design project is under way at the Software Engineering Institute in Pittsburgh, the nation's first federally funded research and development center for software technology [*Electronics Week*, Feb. 4, 1985, p. 27]. Recently, it completed its software-factory



1. NOTABLE. IBM Japan's Software Engineering Group developed Prompter, a knowledge-based tool that produces comments for actual code on each line of a listing.

project, one of its first important efforts to study software engineering tools.

"We're trying to develop the concept of the software factory as a means to automate all the activities involved in the production of software," says associate director Mario Barbacci. That full range of activities includes the complete software lifecycle: requirements analysis, design, implementation, testing, integration, and maintenance as well as managerial activities such as scheduling and budgeting.

Actually, Barbacci says, "software factory" is something of a misnomer. "There is no word in the English language that will express the concept," he says. Factories, like software developers, use standard components and methods to produce their products. (In software, those standards include languages and design methodologies.) But in a factory, raw materials go in at one end, and finished products come out the other.

When a project gears up, its particular needs will be assessed and the appropriate tools will be selected and added to the software factory

In the case of software, no raw materials are used to reproduce the product—a string of data is simply duplicated. "Instead, a lot of activity goes into things that look more like engineering design than actual manufacturing," says Barbacci. "We've kicked it around for a while. I don't think anybody has come up with a better idea. We're still calling it a factory."

The task of pulling together a full complement of automated aids for the software factory is more difficult than it might first appear. Though the market is chock-full of software tools, many are aimed at the design and implementation phases of the software lifecycle. Lifecycle phases, which entail more abstract thinking—most notably, requirements analysis—are much more difficult to automate.

In addition, many of the currently available tools serve a narrow audience. "We still don't know how to provide the right support for different kinds of users," says Barbacci. "For instance, a lot of work still has to be done on different types of user interfaces. If you're a manager, you want to deal with the computer differently than if you're a programmer."

SHOWCASE ENVIRONMENT

Using development tools already on the market, the Software Engineering Institute has built a prototype software factory, which they call a showcase environment. Using work stations linked by means of Ethernet, it incorporates facilities for coding, debugging, documentation, and communications.

"The factory itself is a generic thing," says Barbacci. So the software factory will be different depending on where it is being used. When a project gears up, its particular needs will be assessed and the appropriate tools will be selected and added to the factory. "For example, if you are building prototypes, perhaps you give less emphasis to formal specifications up front. On the other hand, if you are going to build something that will become commercially available, then you might want to pay a lot more attention to budgets and schedules. All of those things will affect what kind of factory is ideal for you. And there isn't usually a single factory that will solve all problems."

Today, the software factory exists more in theory than in practice. "At the institute, we're using the idea of a software factory as a guiding force to select projects, because building a software factory with today's technology would be very difficult," says Barbacci. "Instead, what we're doing is selecting smaller pieces of what

2. SENSE. Lockheed's Software Technology Center uses new tools, such as the Rational R1000 Ada-language development system from Rational, to increase the efficiency of its software engineers. It is also acquiring technology from a number of other companies.

could be in a software factory in the future."

Right now, the results of SEI's year-long software-factory project are being used to determine where to pursue further investigations. An area under study is the automation of tools that generate software conforming to DOD-STD 2167, a Department of Defense software standard. Another project is evaluating programming environments for use with the Ada programming language. And several researchers are working on applying artificial-intelligence techniques to project-management tools.

Researchers are also looking at AI to automate the requirements-analysis phase at the frontend of the software-development process, where errors are particularly costly. Errors here will ripple through the engineering chain and can crop up as bugs once the software is out in the field, making errors in requirements analysis the most expensive to fix.

A form of AI called knowledge-based design is being used by IBM Japan Ltd. to develop a software productivity tool called Prompter. The still-experimental Prompter, developed by a group led by Koichi Fukunaga at IBM Japan's Software Engineering Group (see "The toolsmith's tale," p. 84), is a support tool for code understanding. As such, it attempts to make programs easier to follow by producing annotations—the comments following the actual code on each line of a listing—that adhere to a uniform style (Fig. 1).

Prompter's knowledge base is an *a priori* collection of information about how programs work. The knowledge base is used by Prompter as a sort of reference book to help understand how the program it is analyzing works, analogous to the real-world information a programmer must possess to be able to comment a program properly. It contains three kinds of knowledge—hardware knowledge, such as storage and instruction formats; programming knowledge, such as coding techniques and control and data flow information; and knowledge of conventions, such as control-block definitions or module structures. Prompter's knowledge base must be customized to enable it to analyze programs written in a particular language.

Prompter simulates the execution of a program. Notably, this simulation is run not at the binary-code level but rather symbolically. "The simulation is at the same level at which a programmer thinks when writing a program," says Fukunaga. So when the program being simulated adds the value 1 to an address, Prompter understands that the program wants to increment that address and will generate a comment accordingly.

Knowledge-based design, the idea behind most expert systems, is being used by IBM Japan to develop its Prompter software productivity tool

"The output comments of Prompter are more coherent than those which a human programmer could produce," says Fukunaga. Typically, a programmer's comments will vary in style from coding session to coding session, and they may become difficult for other programmers to

follow. "The advantage of the computer output is that it is always the same, and even first-time users can soon understand them. The disadvantage of the computer is that it may be verbose."

Uniform comments prove most important in the maintenance phase of the software life cycle, when programmers who often had nothing to do with the software's development must step in and fix bugs or incorporate modifications. Rather than first having to reconstruct a previous programmer's thought processes, these maintenance programmers could get right down to the business of changing code. Notably, Prompter works with assembly language programs—typically the toughest to comment well and the toughest to maintain.

OBJECT ORIENTATION

During symbolic execution, Prompter applies the information in its knowledge base to understand how the program under simulation works. Many knowledge-based expert systems store information using the rule-based approach. For Prompter, Fukunaga decided to use an object-oriented approach, which allows knowledge to be decomposed into collections of objects and classes. This was an ideal fit for software: for example, registers can be classified as objects that belong to the class "storage"; the instruction LDA (load register A) is an object that belongs to the class "load-instruction."

To implement object-orientation in Prompter, Fukunaga developed his own programming language, Spool, an object-oriented extension to the AI programming language Prolog. " 'Object-oriented' is a metaphor to describe a mode of operation similar to a conversation among people," says Fukunaga. "An object does tasks of which it is capable, but for tasks it cannot perform it sends a message to another object asking it to perform the task.

For example, an assembler executes a load instruction by copying data from one location to another. In an object-oriented approach, "load" is represented as an object and both the source and memory locations are also objects. The load object first asks the source object what its content is. Then, after learning the content of the source, the load object asks the destination object to store that value. In addition, Spool incor-

THE TOOLSMITH'S TALE

Koichi Fukunaga is firmly against rushing headlong into building large software tools that could turn out to be white elephants. "Tools are different from other programs," says the head of the group at IBM Japan Ltd. that developed the Prolog and Prompter programs. "You have to work with them before you know if they will be useful." That's why he thinks it's best to start off with a simple version and get colleagues to try it out. Then if it works, enhance it.

The merit of that philosophy was recently borne out in Fukunaga's software group. "One member of our group had an idea for a tool to understand the operation of Prolog programs. The backtracking mechanism in Prolog can make the search for bugs very difficult because the same type of backtracking can be caused by searching for a rule and by a bug." A tracer is available in Prolog, says Fukunaga, but it spews out great volumes of paper as it prints out a complete trace of chronological program execution.

But his colleague thought that a top-down search for the error would be more efficient. "He proposed that the program under test be completely executed but that only the execution of the top level should be checked," Fukunaga says. This would enable the programmer to find approximately where the error is. Then that portion of the program could be reexecuted with the next level checked, and the process repeated until the error is found.

FUKUNAGA: Start with a simple version of the tool. Then if it works, enhance it.

Initially, the software group did not take to the proposal. "I told the person who came up with the idea that the only way to check a tool is to try it, so he quickly made a prototype and showed it to the others. The others tried the prototype, and they all changed their minds," he says.

The proof of the project's success is that the tool, called Proedit, is in widespread use in the group's lab at IBM Japan. A paper on the tool, entitled *Visual Debugger for Prolog* by Masayuki Numao and Tetsunotsuke Fujisaki was presented last December at the IEEE Second AI Applications Conference.

Fukunaga took the team approach in developing his idea for Prompter, and the group labored for 18 months on the project. Prompter's knowledge base was developed with the assistance of a consultant, Yoshinobu Yamamura, who is now studying for a doctorate in computer science at Princeton University. Prompter's syntax analyzer was developed by Linore Cleveland, an American woman who worked on the project. Code for the generation of comments was written by Arthur Ozeki, a colleague at IBM Japan. Fukunaga, who holds a master's degree in computer science from Tokyo University, wrote the preprocessor software.

The big problem in developing successful tools, according to Fukunaga, is the limits of imagination. He says that if an engineer can imagine a tool, it's probably already available. But unconventional tools may be just what industry needs. "A tool that changes one's viewpoint can be very useful. Perhaps what is really needed are tools that are still unimagined, rather than tools that are merely unavailable."

porates the backtracking mechanism that is built into Prolog.

As for Prompter's future, no comments are forthcoming from IBM Japan. For now, Fukunaga has been assigned to other projects as the new manager of the Knowledge-Base Applications Group.

ACQUIRING TECHNOLOGY

Stateside, a number of private corporations are working on products to help engineers develop software more efficiently. Among them, Lockheed Corp. is taking a leading role by aggressively acquiring productivity-improvement technology from a host of smaller firms. Lockheed's Software Technology Center, Austin, makes heavy use of the Rational R1000 Ada-language development system (Fig. 2), acquired from Rational, Mountain View, Calif. [*Electronics*, July 6, 1985, p. 36], and of the Refine knowledge-based software development technology from Reasoning Systems Inc., Palo Alto [*Electronics*, Nov. 4, 1985, p. 30]. Lockheed has also invested in the AI-tools company Inference Corp., Los Angeles, and will use Inference's ART (for automated reasoning tool) to develop expert systems.

In addition, the company is considering investments in four or five other companies, which it declines to name. "What we're looking for are companies that have advanced technologies on how to improve the ability to produce software," says center director Winston Royce.

Those productivity-enhancing technologies are beginning to proliferate, according to Royce. "What's generally happening is that detailed design and coding productivity is improving by leaps and bounds." The improvements have resulted from the increased use of aids such as structured design tools and of better programming languages, including Ada and Lisp.

ROYCE: Structured design tools and better programming languages are boosting productivity, says the director of Lockheed's Software Technology Center.

But a heightened awareness of the problems involved in designing high-quality software could account in equal measure for the gain. "The whole underlying basis of reasoning about computer programs has changed," says Royce. "In the past, all of us looked at computer programs as procedural—devices in which you thought through in a serial way the functions at each step of the computer program. A new philosophy has been developed—the new design approach is based on declarative analysis in which you treat the things being processed as objects and you describe what must be done to them, but not how it's to be done."

The "how" refers to the implementation details, or coding, of a software project. Automating the code-generation portion of software design is something that's within the reach of such current technology as expert systems and Reasoning's Refine. Lockheed is using Lisp to build up a knowledge base in a computer so that it can implement low levels of design and code. The objective is to allow software engineers to work in what is best described as a midlevel design language (as opposed to a very detailed, procedural, Fortran coding approach). Programmers would develop software using this midlevel language. The language would tie in to the knowledge-based system from which the final code would be produced automatically. Using such a system could quintuple overall life-cycle productivity, according to Royce.

Lockheed has already successfully used the Refine technology in Link11, a software-development project for the U. S. Navy. The distributed message- and communications-processing package contained 16,000 lines of code. Because Link11 involved real-time processing with many protocol handling considerations, Royce says it is a serious test of the system. Already, Lockheed is gearing up to start a second project.

The development of an all-purpose system must proceed incrementally, incorporating additions to the knowledge base as software engineers learn more rules about code generation. "In the beginning, although the system is built, there are no rules, so you stick in some rules," says Royce. "As time goes on you put in more complex rules. Over a decade, the rule base will get very complex."

At the beginning of a project, coding proceeds pretty much the way it did in the past, says Royce, because there are very few rules. "But as you build up the domain knowledge base, that allows you to shift up into higher semantically meaningful statements and get a better gain in productivity in comparison with the number of lines of code that are produced."

Gains in productivity do more than lower the cost of developing software. They also help companies cope with the current scarcity of software designers. According to Barry W. Boehm, chief engineer of TRW Inc.'s System Development Division in Redondo Beach, Calif., "Managers still are facing a personnel shortage, so getting productivity out of the people you have is important."

To help use the resources more efficiently, TRW uses cost modeling to help in line manage-

ment of its software projects. Currently, for all large and midsize programs, the company requires its managers to use its Cocomo cost model and to define each program's major milestones: plans and requirements, product design, detailed design, code and unit testing, and integration and testing. They continually compare where they are on the project against where they expected to be in the model. This helps keep them on schedule and supplies data to update the model to match the actual project conditions.

TRW plans to continue to develop Cocomo, which it started in 1981. "It's providing valuable insight on how to reduce costs," says Boehm. Using Cocomo, TRW has realized a 40% productivity improvement over previous programs.

BOEHM: The chief engineer of TRW's System Development Division says productivity gains help in coping with the shortage of software designers.

In the software design phases, TRW is also applying automated design tools. "We find that the formatted structure they impose encourages better and cleaner designs," says Boehm. "We're doing more planning in the design phase for cost reasons because later, when you have to fix something, it's more expensive."

Despite the resolute efforts of software companies to turn the development process into a predictable, easily manageable exercise, large-scale software development is likely to remain problematic. "The reason is that program demands increase as fast as the improved design methodologies—it's a constantly moving target," says Boehm. He points out that programs written for mainframes could evolve into software for mobile computers and then migrate to distributed microcomputers. Each of these machines poses new sets of problems, with different functions and testing requirements. "The typical job is always bigger and more complex than its predecessor."

'What's generally happening is that detailed design and coding productivity is improving by leaps and bounds' with the increased use of development aids

In the past, software managers paid lip service to the need for testing as a way to catch errors before code went out into the field. But testing budgets usually weren't up to snuff, and managers depended on their programmer, not on their test engineers, to make sure that the software worked. That is beginning to change.

Today, testing and quality assurance are becoming critical items on the software manager's agenda. A powerful reason behind the shift, according to Lockheed's Royce, has been the increased awareness generated by complicated upcoming software projects for the National Aeronautics and Space Administration's space station and the Strategic Defense Initiative.

As a result, customers are demanding that higher-level, more thorough tests be run on software. "Furthermore, they're going to demand that logical testing be done to prove that under all possible inputs, certain classes of errors cannot take place—that's a new kind of testing, that's tough," Royce says.

BUILDING IN MAINTENANCE

Maintenance, or the continued monitoring and upgrade of software once it's out in the field, is also becoming more important. Says TRW's Boehm, "In the past, project managers charged with budget and scheduling primarily made it work first and skimped on making it easy to maintain. But recently, maintenance has been built into development plans." Building-in the ability to maintain code requires cleaner design and high-quality documentation—which are easier to do with the generation of automated design tools now becoming available.

Nevertheless, even as the art of software productivity advances, it is the abilities of the people using the tools that count the most. And no matter how advanced the tools, one fundamental rule of software development still seems to hold true: the old saw that 20% of the people do 80% of the work. So though advances in software development can help plodding programmers, their biggest impact is in helping the smart work even smarter. "The difference in people capabilities is still the biggest variant," says Boehm. "It can amount to a 4:1 difference in productivity, even with design aids. As more advanced technology comes along, the variant gets bigger because the good people use the tools better." □

Additional reporting provided by Charles Cohen in Tokyo, J. Robert Lineback in Dallas, and Larry Waller in Los Angeles.

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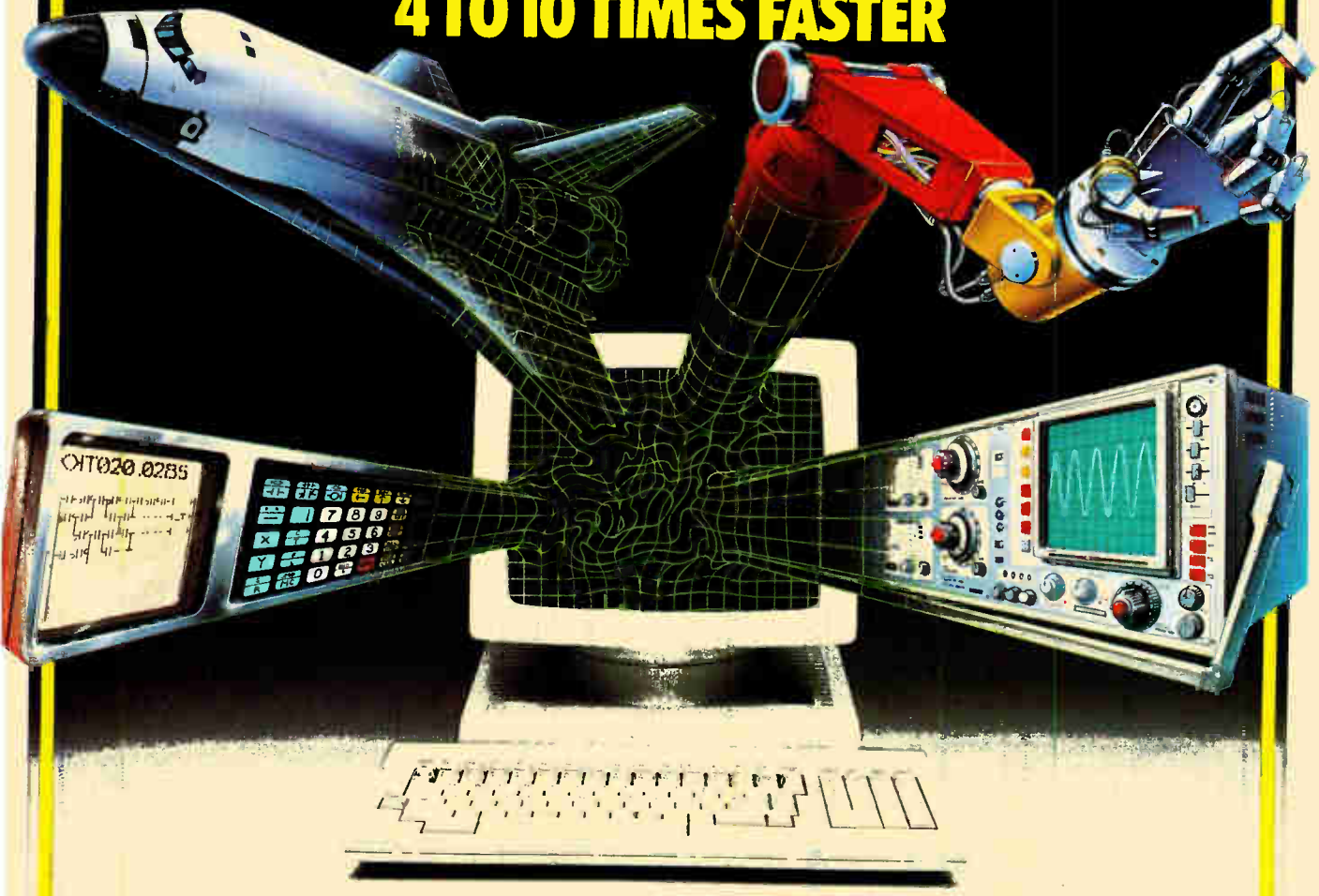

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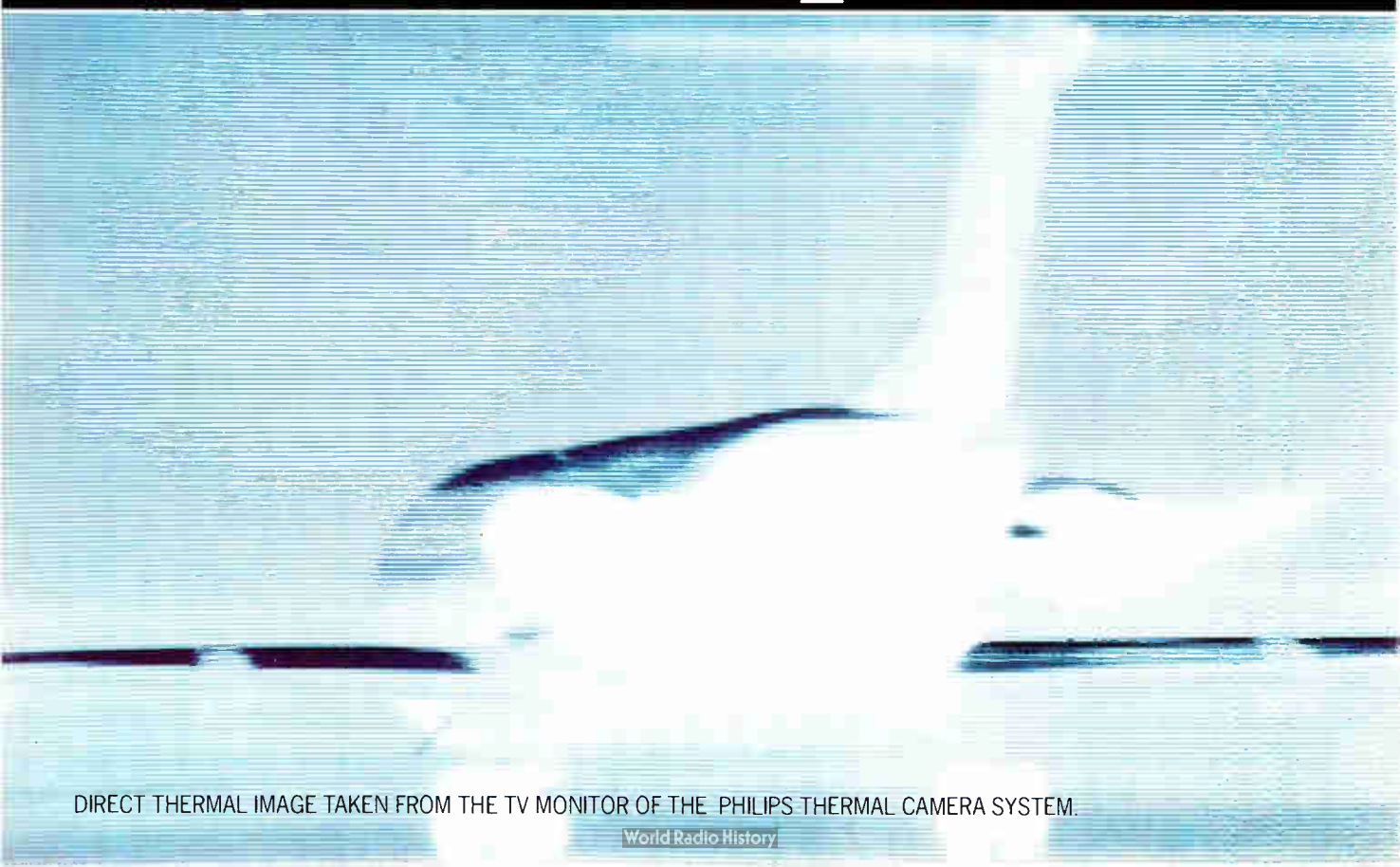

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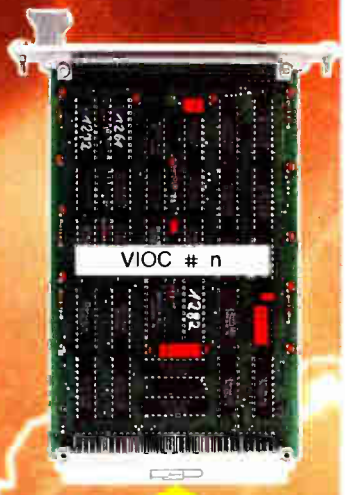

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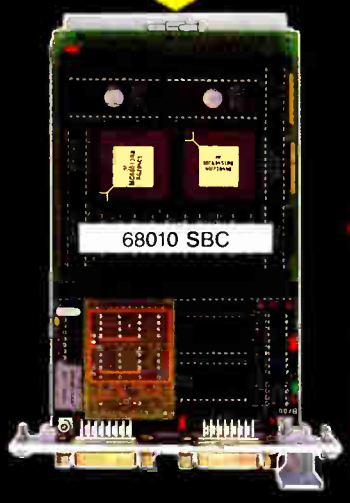

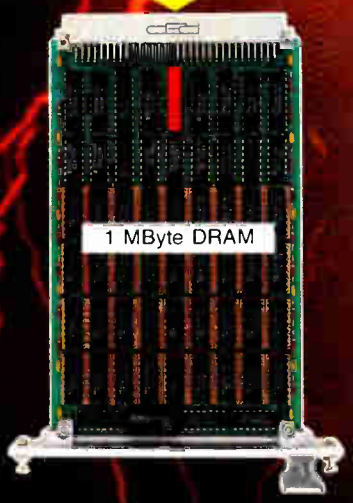

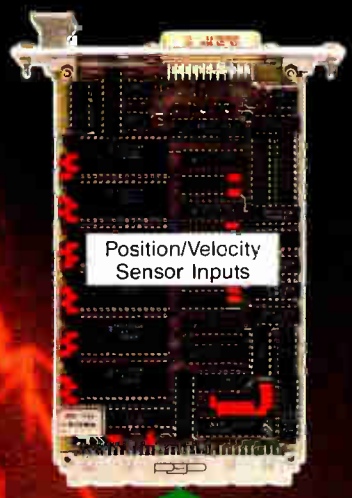

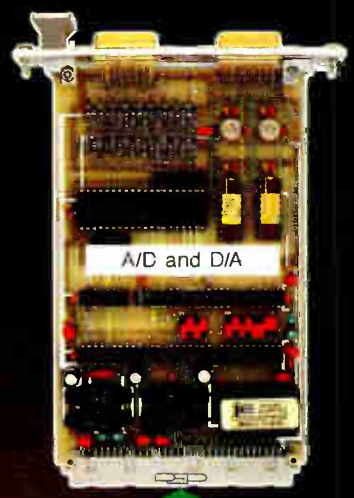

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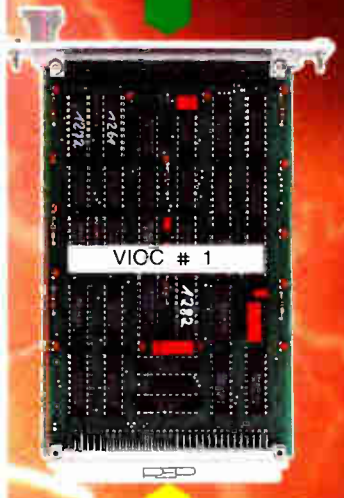

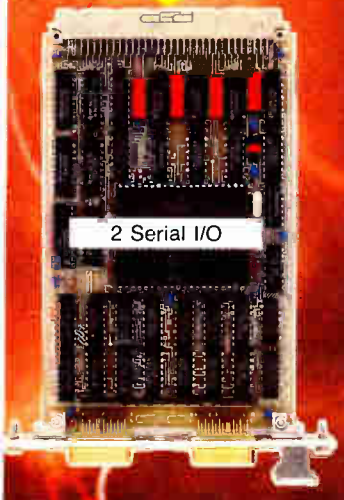

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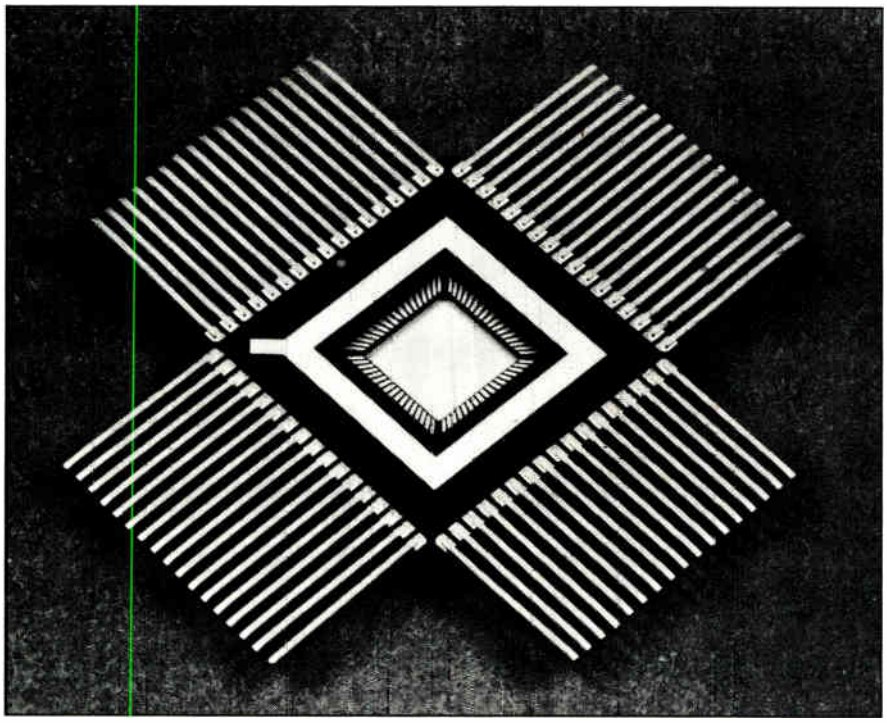


2. LEADED CARRIER. Intel's 68-lead quad pack eliminates the troublesome problem of thermal mismatch between leadless carriers and their boards.

mercial and industrial applications. Because the packaging density of military equipment calls for many interconnections, it relies more and more heavily on multilayer boards and flexible circuitry of all types.

There are several kinds of surface-mounted chip carriers. The original version was the flat-pack—a square package with flattened leads coming out of two opposite sides. This package is no longer recommended for new designs: it is rarely made anymore, it is hard to handle, and it does not lend itself to the automated assembly process.

Today's leader in the military chip-carrier market is the leadless ceramic chip carrier with input/output pads on 50-mil centers. The leadless carrier dominates in spite of certain significant problems. These include a mismatch of thermal coefficients of expansion with standard pc-board laminates, which causes solder-joint failures during thermal shock testing, and solder joints that are difficult to inspect. This unit has the smallest size and weight of all military carriers and can be designed for a fine pitch. It possesses excellent thermal conductance, is easy to heatsink, and imposes no handling problem.

There are four ways to solve the thermal-mismatch problem caused by the leadless ceramic carrier: using a constraining metal core such as copper-Invar-copper or copper-molybdenum-copper; using a low-TCE dielectric such as Kevlar to approximate the TCE of alumina; adding an elastomeric layer to the top pc-board layer; and mounting leadless carriers on a leaded ceramic motherboard.

The most successful and common solution is the copper-Invar-copper method, which has two variations. In the simpler one, two multilayer boards are laminated to a central metal core and communicate through a card edge connector. In the more complex variation, copper-Invar-copper layers are used as ground and power planes in a multilayer structure. Both constrained-core and Kevlar boards, extensively tested by many U. S. companies, have exhibited reliable operation with no solder-joint failures over a wide range of thermal shock (Table).

One of the largest programs using leadless ceramic chip carriers on metal-core thermally compensated multilayer boards is the defensive electronics for the B-1B bomber, which includes 5,000 lb of avionics gear. It is in production at the Airborne Instruments Laboratories (AIL) Division of Eaton Corp., Deer Park, N. Y. In this program, two four-layer, polyimide-glass boards, each with 8-mil printed traces and spaces and 13-mil vias, are laminated to each side of a copper-molybdenum-copper core. A special surface-mounted connector links the two circuit boards to each other and acts as a connection to the backplane. Thermal vias under each chip carrier conduct heat down to the metal core of the composite board.

AIL's designers chose a copper-molybdenum-copper core rather than the more heavily used copper-Invar-copper for two reasons. First, the moly-based material is stronger, with a higher Young's modulus. This results in a thinner core and, in turn, a thinner overall board structure. AIL deliberately kept its boards thin to control impedance and to hold down the aspect ratio of the board's vias. Second, moly has much better thermal conductivity than Invar. Interestingly, these advanced boards plug into wire-wrapped backplanes rather than into a multilayered pc-board backplane—the more modern approach. Finally, a large percentage of the B1-B's other boards are Multiwire types that carry DIPs rather than the leading-edge leadless chip carriers.

THE LEADED ALTERNATIVE

There are about 24 production programs based on leadless ceramic chip carriers and a similar number in preproduction. Many more military programs are in development. However, even the leadless ceramic chip carrier's strongest advocates admit that there are potential attachment problems for very high-power, high-pin-count VHSIC devices. This situation dictates the use of some form of the leaded carrier.

Because of the thermal-mismatch problem with leadless chip carriers, leaded ceramic chip

TEST RESULTS ON COPPER-INVAR-COPPER (CIC) AND KEVLAR PC BOARDS

Manufacturer performing test	Material	Number of layers	Largest package	Number of cycles	Temperature range (°C)	Failures
RI/Collins	CIC/polyimide	4	44 pads	800	−55 to +125	0
General Electric	CIC/epoxy	4	64 pads	1,500	−55 to +125	0
Honeywell	CIC/epoxy	1	84 pads	1,000	−55 to +125	0
TI	CIC/epoxy	1	84 pads	1,000	−55 to +125	0
TI	CIC/polyimide	1	84 pads	1,000	−55 to +125	0
Sperry	CIC/epoxy	8	84 pads	1,200	−55 to +125	0
Plessey	CIC/epoxy	–	84 pads	2,200	−55 to +125	0
Hughes	Kevlar/polyimide	6	84 pads	500	−55 to +125	0
Martin	Kevlar/polyimide	4	64 pads	500	−40 to +87	0
GE	Kevlar/epoxy	8	84 pads	1,000	−65 to +125	0

SOURCE: TEXAS INSTRUMENTS INC.

carriers that are often used in custom versions on supercomputers are now being considered as an alternative to leadless types, particularly when the number of I/O pins exceeds about 44. The leaded carrier should theoretically solve the TCE board-mismatch problem if the right degree of compliance is designed into the unit's leads. And with a J-lead configuration, a leaded carrier has the same footprint as the leadless type.

But the leaded carrier is two to three times more expensive, 1.5 times heavier, and has a vertical profile two to four times higher than the leadless version. What's more, it is difficult to handle, has limited availability, and has yet to be standardized by the Joint Electron Device Engineering Council. Nonetheless, Intel Corp. is already producing standard military versions of its microprocessors in a 68-lead quad pack (Fig. 2), and it appears that the leaded ceramic chip carrier could yet find a place in pc-board applications requiring at least 44 leads.

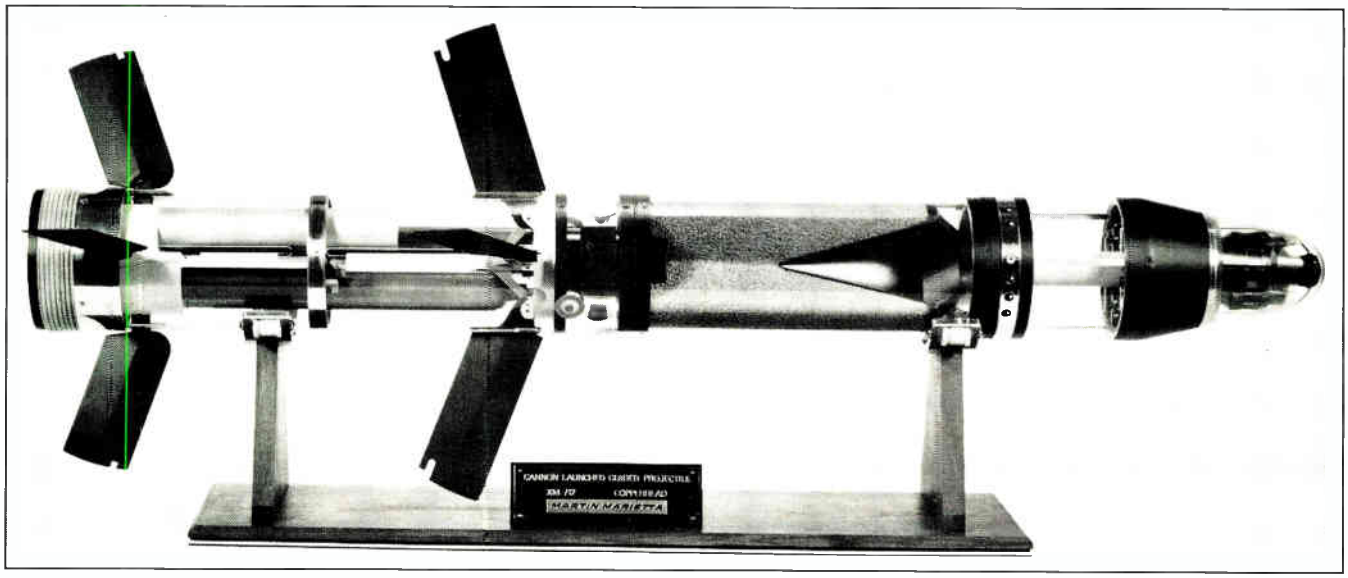
Usually, leaded carriers for surface mounting have their pins shaped into either a gull-wing or a J-lead configuration. The J-lead takes the least space but is not easily inspectable. The gull wing, by contrast, is easy to inspect but has a larger footprint than the J-lead. Both leads have a relatively high profile. Several companies, among them General Dynamics, Fort Worth, Texas, are exploring a solution to this problem: butt mounting. This technique involves mounting a component to board pads on extremely short vertical leads, resulting in a low-profile package with the footprint of a leadless carrier.

One approach to butt mounting shows up in a developmental avionics board being assembled at Hamilton Standard Corp., Farmington, Conn. It combines standard surface mounting of leadless chip carriers that have up to 84 I/O pads with a mix of butt-mounted components such as semiconductors in TO-18 cases, radial- and axial-lead passive components, and a 132-lead ceramic quad flatpack on 25-mil centers. Butt-mounted components constitute about 15% of the total number of components. All components are vapor-phase reflow-soldered.

The finished structure will consist of two polyimide-glass multilayer boards with copper-invar-copper cores laminated to the opposite sides of an aluminum stiffener that also acts as a heatsink. Already, the multilayer boards with a mix of leadless and butt-mounted surface-mounted parts have gone through design and development, notes Jim Long, an assistant design project engineer at Hamilton Standard. Now, they must prove out in thermal shock and vibration tests. Lab tests show promising results. Eventually, Long would like to go to 100% butt-mounting and eliminate the leadless carriers for the avionics board, but for now, component availability limits this possibility.

In butt mounting, packages with short vertical leads are soldered to a board, resulting in a low-profile leaded package with the footprint of a leadless carrier

Although avionics are well into the rush toward surface mounting, there is another class of airborne equipment—missiles—that is much slower to incorporate the technology. But, as missiles are redesigned for greater functionality, surface mounting often finds its way into the new designs. "There are two kinds of airborne equipment: avionics meant to last 10 years or more, and the one-shot missile," says Classon, manager of electronic packaging for Martin Marietta. "The latter is built, tested, stored, and fired. You can't apply the same principles of packaging as used in avionics. This would be a waste of money in expendable equipment. For example, in missile electronics we try to avoid putting in a lot of expensive connectors and only use the minimum number of this type of component." Martin Marietta is currently producing



3. COPPERHEAD. The cannon-launched Copperhead is designed to endure a 13.5-ms 9,000-g force.

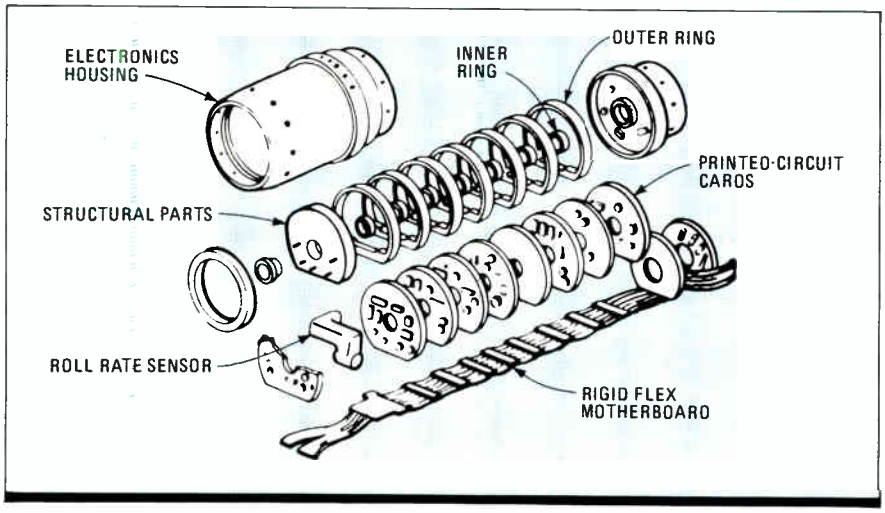
two tightly packed guidance packages—one for the Copperhead guided projectile and another for the Hellfire antitank guided-missile system.

The Copperhead (Fig. 3) is launched from a 155-mm howitzer and must withstand 9,000-g forces for 13.5 ms. In the past, cannon-shell electronics were always packaged in small potted modules, notes Classon. In the Copperhead, there is a sizable amount of electronic circuitry and it is not potted. "The Copperhead was the high point of leaded packaging and it has excellent producibility," says Classon.

A laser receiver in the nose of the shell uses surface-mounted passive components and thick-film hybrids. The guidance package contains interconnected annular pc boards with section interfaces that are connected by a rigid-flex motherboard, which is supported by aluminum rings that transfer the shock load into the housing. The assembly is compressed and bolted to prevent breakup at firing (Fig. 4). Holes in the center of the electronics assembly permit a shaped-charge warhead to pass through without interference.

The Hellfire missile, by contrast, encounters a comparatively normal missile environment: 100 g plus aircraft vibration. Martin Marietta's solution is to repackage the Copperhead's circuitry using simpler circular rather than annular boards plugged into a simpler rigid motherboard. The circular boards could be used because the Hellfire has a fixed warhead behind the laser-seeker section.

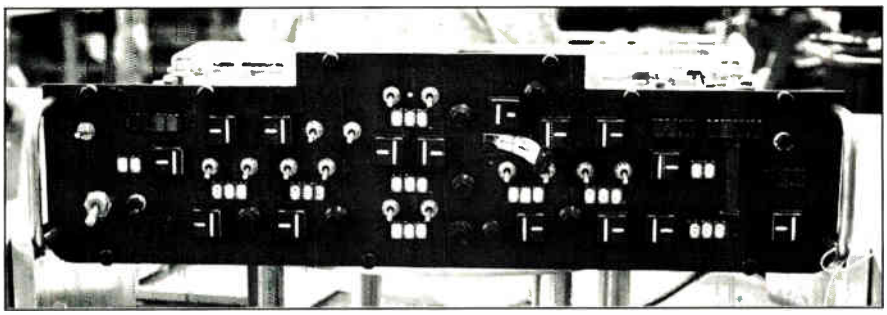
In the late 1970s and early 1980s, Martin Marietta started increasing its use of surface-mount technology. A case in point was the Adats (Air Defense Anti-Tank System) that the company developed with Oerlikon-Buhrle of Switzerland. Martin Marietta initially tried to package the guidance circuitry of the Adats missile using the Copperhead's technology. This resulted in a design requiring 14 Copperhead-like boards where there was room for only 10. A complete redesign using surface-mounted leadless chip carriers on both sides of polyimide multilayer boards with a central copper-Invar-copper core reduced the number of boards from 14 to 4.



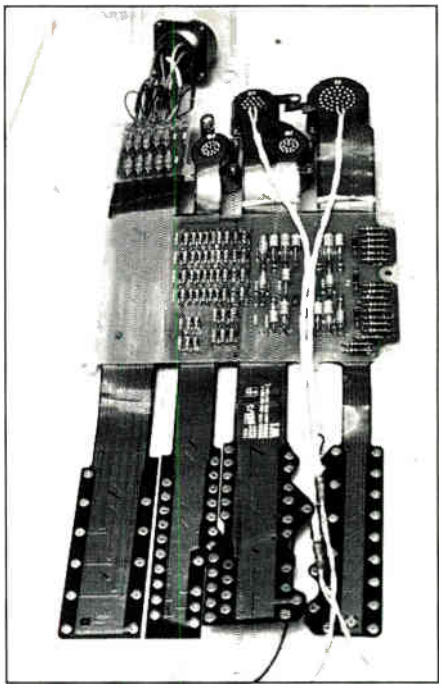
4. SHOCK MOUNTED. The Copperhead's guidance package consists of annular pc boards plugged into a rigid-flexible printed-circuit motherboard.

Martin Marietta has many new programs using surface-mount technology. The most significant is for avionics equipment for the F-16—Lantirn (Low Altitude Navigation and Targeting Infrared for Night System)—using leadless chip carriers on polyimide boards. The company has also done a great amount of development work on all phases of the leadless chip carrier's thermal-mismatch problem.

Packaging large arrays of leadless ceramic chip carriers on com-



5. FUEL MANAGEMENT. Gull Inc.'s Interface Fuel Management Panel for the KC-135 achieves its high packaging density with a combination of rigid, flexible, and rigid-flex boards.



6. RIGID FLEX. On the IFMP, the use of rigid-flex circuitry extends to EMI and surge suppression. Surge-suppressor diodes are located on the rigid board part of the rigid-flex assembly.

pensated boards is still mainly the field of the very large companies, including AIL, Collins, Hughes, Martin Marietta, RCA, and Tracor. Many small to medium-size companies still are turning out cleverly packaged equipment based mainly on ICs in dual in-line packages. But these companies are aware of the advantages of surface mounting and are either working on developmental equipment using chip carriers or are even establishing separate facilities to carefully get the know-how to apply the new techniques needed. A significant part of this expertise involves developing complex interconnections for the increasingly complex chips.

FLEXIBLE CIRCUITRY

A case in point is Gull Inc., Smithtown, N. Y., a midsize company that builds airborne avionics for fuel gauging, fuel management, engine instrumentation, and displays. Equipment in production uses a mix of DIPs and TO-18 packages on pc boards with up to 12 layers. Gull excels in the design and use of flexible and rigid flexible circuitry. It has actually made flexible circuits with up to 26 layers. For example, the densely packaged IFMP (Interface Fuel Management Panel) for the KC-135 tanker is full of both flexible circuitry and rigid-flexible circuitry (Fig. 5). In this equipment, even the circuitry for transient suppression and electromagnetic-interference suppression uses rigid-flexible boards to save space and ease manufacturability (Fig. 6).

Gull is now developing an Integrated Fuel and Engine Indicator for the F-18 fighter; this project constitutes the company's first contact with SMT. The IFEI has a complex liquid-crystal display composed of two separate backlit LCDs with both analog and digital presentations (Fig. 7). Each LCD has more than 100 input connections, forcing Gull to design both a special copper-Invar-copper board to house four leadless chip carriers for custom driver chips. Two of these boards are required to drive each LCD.

In addition, the connectors from the two surface-mounting boards to the LCDs could not be standard connectors because conventional connectors were much too large for the space allotted. Gull's solution was to go to a Zebra-type elastomeric connector (a rectangular strip with alternating layers of conductive and nonconductive silicone rubber) that easily met the F-18's interconnection density, size, and volume specifications.

The rest of this avionics package consisted of two standard non-surface-mounting boards plugged into a rigid motherboard. Gull is already planning to introduce more surface-mounted technology into its next generation of equipment.

Similarly, Telephonics Corp., a subsidiary of Instruments Systems Corp., Huntington, N. Y., is testing the waters of surface mounting. The company is heavily engaged in avionics, aerospace, and Army electronics systems. It builds the sophisticated central integrated test system (CITS) for the B1-B [*Electronics*, June 25, 1985, p. 48D]. As is the case with practically all of this company's equipment, the CITS uses proven through-the-board DIP-based multilayer technology.

Many small to medium-size companies, aware of the advantages of surface mounting, are starting to replace their DIPs with the new technology

But Telephonics has realized that surface-mounted technology would be needed for some of its coming programs, and six months ago it built a small but complete SMT lab-prototype facility with such equipment as a screener, vapor-phase oven, and pick-and-place machine. Soon, engineers at this facility will assemble the first batch of thermally compensated test boards for leadless chip carriers. After the surface-mounting process and boards are proven satisfactory, the new facility will be used to build boards for a new project.

After an extensive survey of existing military SMD work, Telephonics will go to a method similar to that used by AIL on its SMT boards. They build up two separate chip-carrier-laden multilayer boards and then laminate the boards to opposite sides of a copper-Invar-copper core. "We prefer this method because we will be able to test both halves of the board before we laminate them to the core," says Al Comins, director of mechanical engineering at Telephonics. This would not be possible in the other thermally compensated board approach that uses the metal layers as ground and power planes.

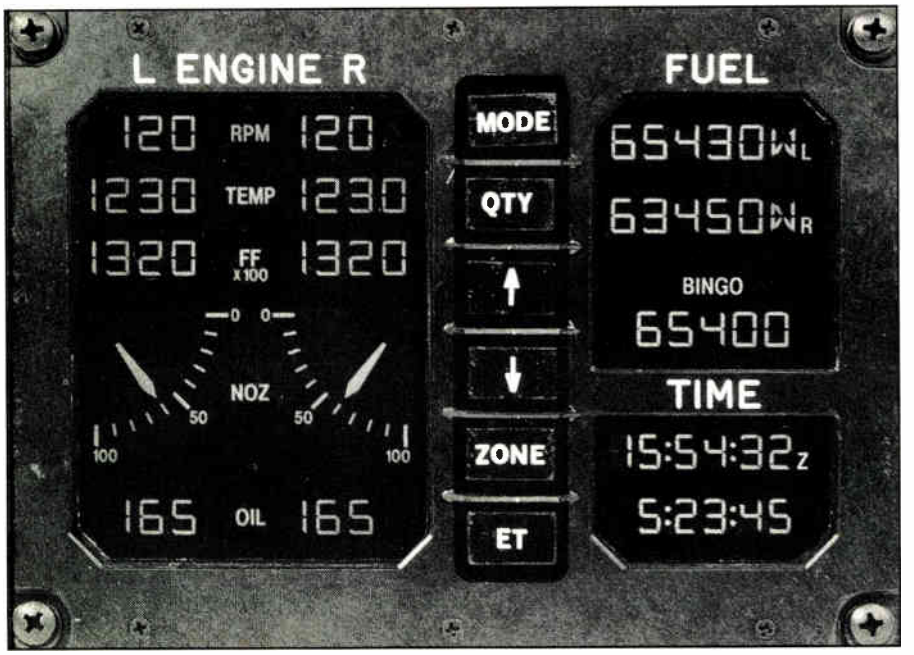
Also moving into surface mounting are makers of militarized microprocessor boards, though the move is slower than elsewhere. Nonetheless, the pace is quickening as companies move into VHSIC design. Bob Harris, director of computer programs at Titan Severe Environment Systems Corp. (Titan Sesco), Chatsworth, Calif., points out that as military systems incorporate increasingly sophisticated technology to improve system technology and as the current fiscal backdrop calls for the leveling of defense expenditures, many defense contractors are turning to militarized microprocessor boards to make the highest technology available for their designs. The use of a sophisticated militarized board allows systems designers to focus their efforts on the design and performance of the system and not on the design of the microprocessor boards.

Titan Sesco is one of the companies that will supply militarized boards and full microcomputers based on ICs from the Intel military operation in Chandler, Ariz. What Titan Sesco does is to repackage Intel's larger microcomputer boards in Sesco's 6-by-9-in. format. These boards have stiffeners to resist vibration and a thermal frame to allow operation at elevated temperatures. On some boards, it has been necessary to replace small-scale-integration glue chips with either gate arrays or programmable logic arrays to maintain the 54-in.^{2} card area. Now there are militarized boards based on the Intel iAPX286, iAPX186, iAPX86, and the 8080 and 8085 processors. In the future, a militarized version of the 32-bit iAPXX386 processor will become available. Ordinarily, the militarized boards are designed for DIP packages. The forthcoming 32-bit processor in a leadless chip carrier will be socketed onto a conventional through-hole board.

VHSIC Phase 1 and 2 devices will radically affect pc-board design, processing, assembly, and even laminates. To prepare, the Aeronautical Systems Division of the U. S. Air Force at Wright-Patterson Air Force Base in Ohio has begun a program for sophisticated electronic assemblies. This program, managed by ASD's Materials Laboratory, is establishing manufacturing techniques, processes, and controls for economical, high-quality production of VHSIC assemblies. The work is being done through a cost-sharing contract with Martin Marietta.

With a team of subcontractors, Martin Marietta is trying to improve production of VHSIC chip and pc-board assemblies. This involves establishing materials, processes, and controls for soldering VHSIC packages to boards and making necessary intrachip connections. The dense boards will use both leaded and unleaded chip carriers. Martin Marietta has over 40 subcontractors, including GE, National Semiconductor, and Westinghouse. All participants will share in the technology transfer and benefits from the program.

Many experts believe that in about five years, packagers will have to go to the chip-on-board technique—wire-bonding bare chips directly to pc-board pads—to cram everything in the volumes called for. This in turn will introduce new problems such as thermally matching a large silicon chip to a pc laminate. Martin Marietta Aerospace and other companies are already looking at chip-on-board and uncased tape-automated chips as possible solutions to tomorrow's even more dense boards. Many aerospace firms are already dealing with VHSIC Phase 1 chips with more than 100 leads, which call for pc boards with increased interconnection density. The high-speed performance and high power dissipation of the VHSIC chips (now readily available) compound the immediate future's packaging problems. Boards for VHSIC chips will have to have finer lines and lower dielectric constants. □



7. DUAL LCD. This complex dual LCD for integrated fuel and engine control necessitates use of an SMT driver board and two special elastomeric connectors.

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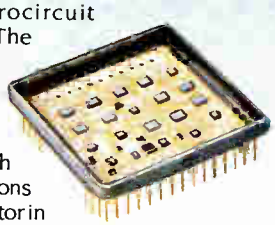

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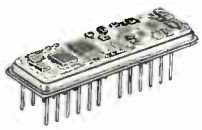

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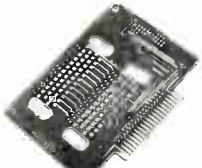

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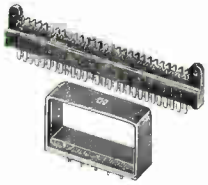

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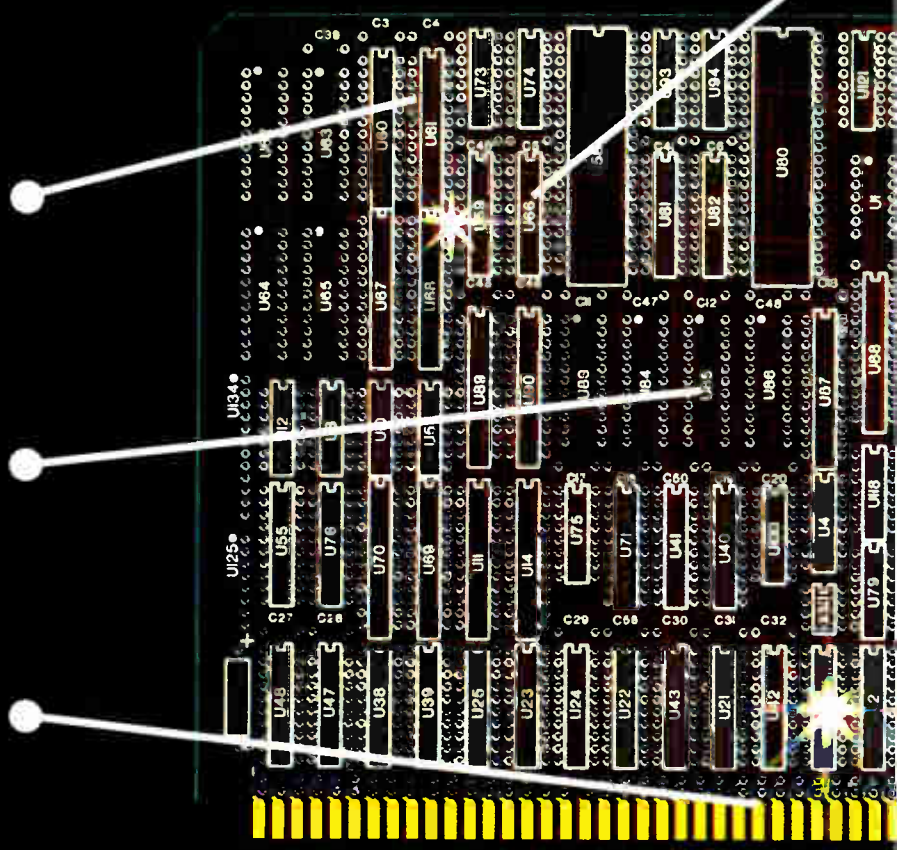

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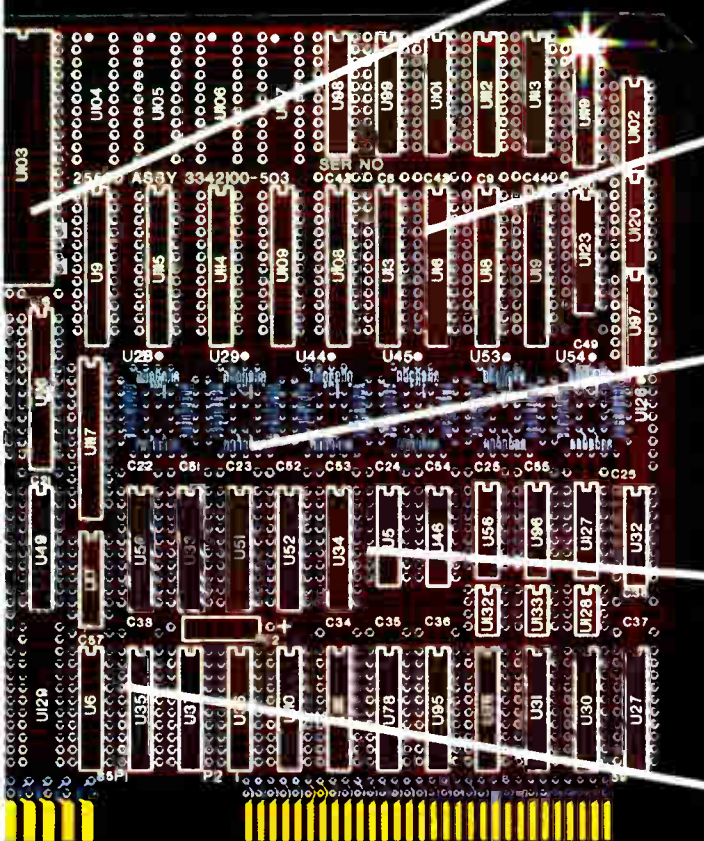

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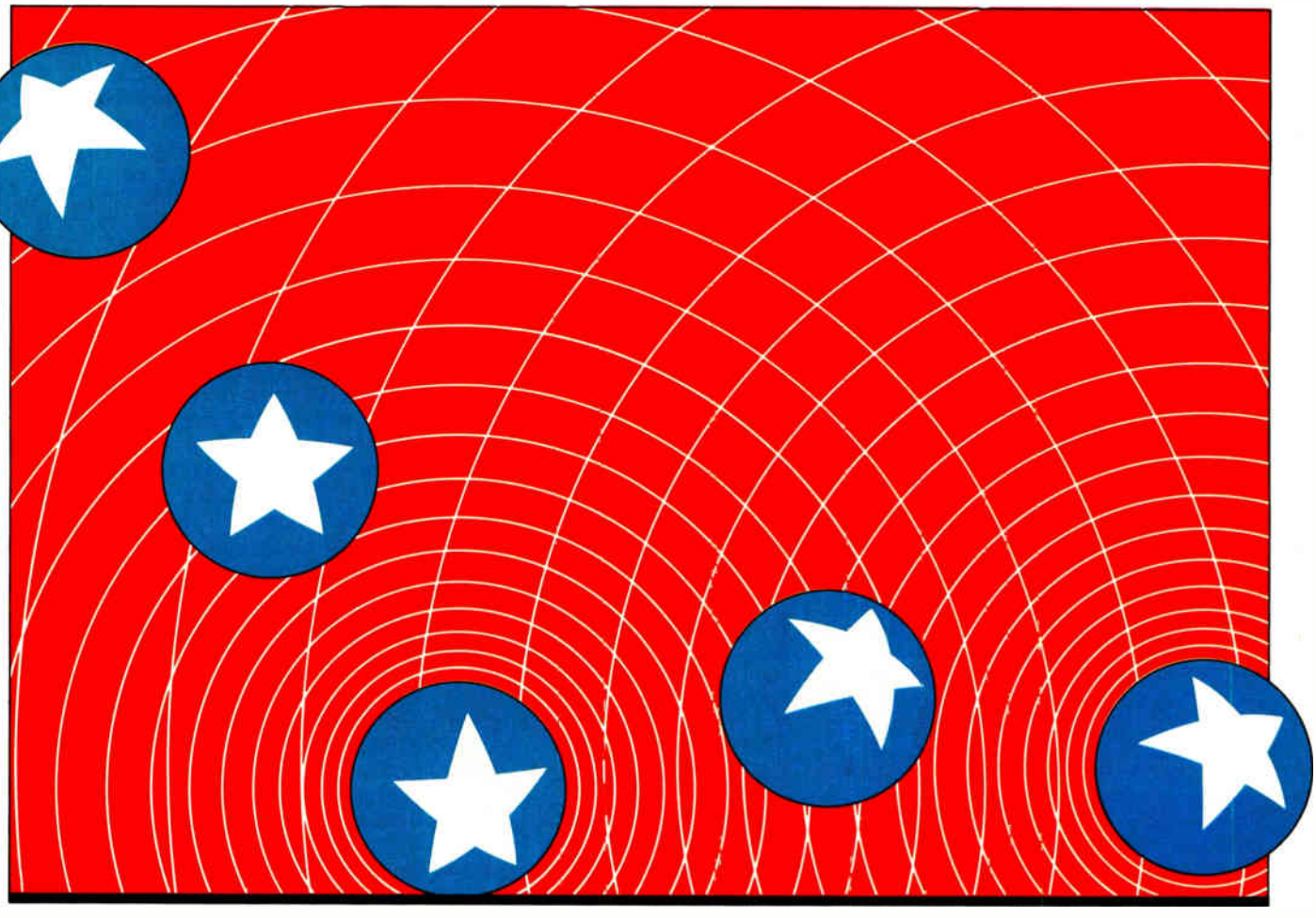


The electronics industry hasn't bounced back as strongly as it had hoped from the down year that it had in 1985. There have been some mildly encouraging results, but the most striking characteristic of the first six months is the way market watchers have been downsizing their growth predictions. What will the second half bring? Most executives once again hope that, led by a recovery in computers, things will get better.

NOW IT LOOKS FLAT

Test and measurement companies expected 1986 to wipe out memories of a 1985 that saw business grow an inconsequential 1%. They figured that U.S. orders for automatic test equipment would lead the way to a 12% overall increase in sales. Now they see a flat year, with only overseas sales keeping the picture from getting worse.

A good indicator of the state of the U.S. market is rentals, which tend to be high in a growing market—and they are down, says Art Husami, vice president of marketing at Electro Rent Corp. in Burbank, Calif. "The decline has been going on since the last quarter of 1984, coincident with the general decline in the computer industry," he says.

However, Husami adds, the market seems to have bottomed out: "There is no shrinkage, but there is no fast growth either." He bases his belief on the behavior of rental pricing. In the throes of the downturn, there was fierce price competition. "Per-month rental charges fell steadily as [rental] companies competed to cover cost of the equipment they had in inventory," he explains. Since then, rental costs have become more realistic. Also, supply is more in line with demand, hence closer to an equilibrium state. But Husami knows the real cure. "What will move the industry out of its doldrums is a recovery in the computer business."

The U.S. test and measurement market is weaker this year than last, agrees Fletcher Chamberlin, corporate communications director at Tektronix Inc., Beaverton, Ore. He says the company's aggregate order rate is down 3% from the same quarter last year. Moreover, he adds, business in Japan is worse than that in the U.S. Comments analyst Daniel H. Rosenblatt, assistant vice president at Merrill Lynch Pierce Fenner & Smith, "Tek management describes a very flat order environment and expresses little hope for a strong near-term recovery."

The only bright spot is the European market, Chamberlin says. "If the local European economy were not strong, the dollar decline would not be helpful. But the economies have been good, hence the business in Europe has been up."

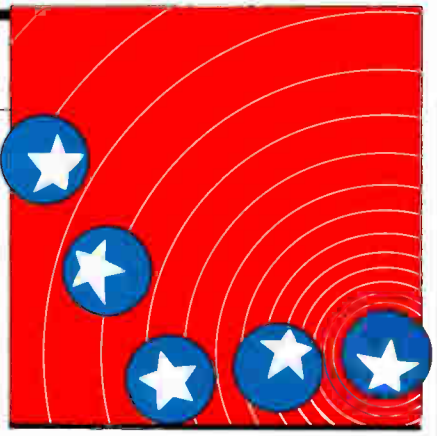
Chamberlin's assessment of general business conditions in the U.S., Japan, and Europe is right on the mark, says William Terry, vice president and general manager of Hewlett-Packard Co., Palo Alto. Terry, however, sees a potential new market in the People's Republic of China. "HP has been doing business for four or five years in China," he says.

The Chinese market is no dumping ground for outdated equipment. "The Chinese have 75 instrument factories of their own turning out equipment," he says. "What they want from the U.S. is the newest, best, and most advanced equipment." The Chinese plan on moving into the 21st century on the leading edge of technology, he adds.

A STRONG SECTOR. Terry says that instruments for engineers is still a good business, but that tools with greater utility will loosen up tight spending policies of companies with frugal capital-equipment budgets. "Bench instruments will always be in demand," he says. "With more engineers coming into the market, each will need the basic tools, so the replacement and outfitting of new employees will keep this market segment growing at a modest 6% to 8% per year."

Chamberlin says digital oscilloscopes are one of Tektronix' stronger product lines among bench instruments. Sales of portable digital scopes are up slightly over last year. One exotic test-equipment area that is expected to show growth near term is tools for fiber-optic systems, he says. "There's somewhere between $60 million and $80 million worth of yearly sales and an annual growth rate of around 20% to be found in this business."

One of the healthiest lines at Tektronix is communications test equipment, says Rosenblatt of Merril Lynch. Terry agrees. He says that segment should grow at an annual rate of 10%.



The general picture for automatic board and IC test equipment is not good. Terry says he sees flat business in the board-test area for the near term. The depressed computer and semiconductor business do not hold out much hope for improvement in this sector.

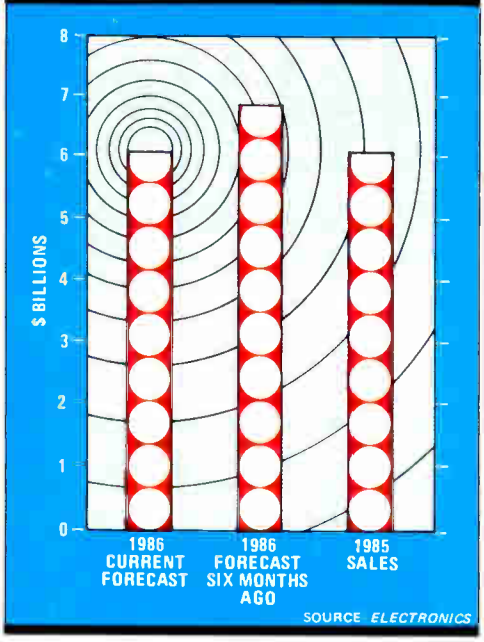
However, there are some small signs of improvement. For example, GenRad Inc. recently received a big order from Jaguar Motors in the UK. The orders were to begin shipping in the second quarter of this year and will be completed in 1986. Rosenblatt sees chances of GenRad breaking even in the third quarter and being profitable in the fourth.

Moreover, the IC test market is on a steady long-term growth trend, according to Tektronix' Semiconductor Test Systems Division. "The worldwide semiconductor market was valued at $21.2 billion in 1985" and will rocket to $70.1 billion by 1990, says Dan Dunachek, an engineering manager at Tektronix. "The future requirement [for test gear] can be estimated by observing that over the past decade, capital spending for ATE has been a relatively constant percentage of total IC volume—between 3% and 5%, with a 10-year average of 3.85% [a year] from 1973 to 1983," he says, quoting Prime Data Corp. of San Jose, Calif.

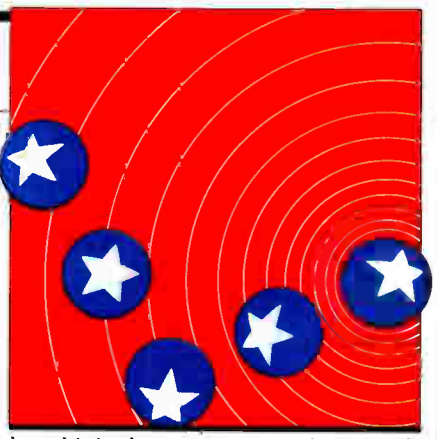
Applying the 3.85% factor to his $70.1 billion IC forecast for 1990, Dunachek concludes that "the total expected demand for semiconductor ATE in 1990 is $2.7 billion. We expect the market for CMOS ICs alone to reach $4 billion by 1990, generating a CMOS ATE demand of $1.5 billion."

Dunachek segments the market further and says the largest demand, $412 million by 1990, will be for memories. "We expect 84% of that demand to be met by Japanese producers. If CMOS memories are subtracted, the remaining market for ATE to test standard logic, custom, and semicustom application-specific ICs, microprocessors, and peripheral chips amounts to $357.3 million."

U.S. T&M EQUIPMENT SALES



AN UPTURN INCHES ALONG



The components business struggled through a forgettable 1985 of barely 2% growth, and manufacturers were hoping for an upswing by the second half of 1986 that would yield a 10% overall increase in business. Now they're beginning to see some evidence of an upswing, with inventories having been worked off, distributors coming back into the market, and end users increasing production. However, the upturn looks more modest than hoped for, in the neighborhood of 6% for the year.

Inventory work-off has meant something of a turnaround for Bourns Inc., the Riverside, Calif., producer of trimming and precision potentiometers, panel controls, and resistor networks. Although there has been improvement, the change has not been spectacular, says Curtis Jones, corporate vice president for electronic component sales. Growth was 5% to 10% in the first half. "Overall, this year will be higher in terms of demand and need for components to supply the equipment manufacturers," he says.

Also experiencing first-half improvement is Burr-Brown Research Corp. in Tucson, Ariz. Shipments will continue to increase in the second half, says Dennis Haynes, manager of applications engineering. However, Haynes refuses to characterize what he calls the slight increase as a turnaround.

"In the past, as soon as people sensed that a turnaround was going to take place, they ordered in anticipation of the wild upswing. That in turn created a wilder upswing," he says. "I believe there's a lot less of that going on now."

For connector maker ITT Cannon Inc., Fountain Valley, Calif., "military funding needs to be released. And, on the commercial side, there needs to be a stronger confidence so that the economy will continue to grow," says Charles Hofbauer, director of marketing and business development.

The first half of 1986 looks as though it will turn out to be very slow, says Hofbauer, particularly among original-equipment manufacturers, which are spreading delivery time over 12 to 18 months. He says he hasn't seen any growth in the first half of this year, but the company expects a 5% to 10% increase in the second half.

Business has been improving gradually since the first of the year for connector maker Molex Inc., Lisle, Ill. Each month's sales through April have exceeded those of the previous month, says board chairman John H. Krehbiel Sr. It has been gradual, and he expects that trend to continue. Krehbiel says Molex's 1986 revenues will be about 14% to 15% ahead of 1985's.

For Allen-Bradley Co., the outlook is a tale of two product lines: resistor networks and surface-mount passive components, both of which it makes in Greensboro, N. C. The resistor network business bottomed out at the end of last year, says marketing director Jack R. Polakowski. The first half of this year has been "flat to maybe showing just a slight improvement." Polakowski attributes this change to some firming in the computer business as well as slight improvements in the automotive business. Telecommunications, the third major application where resistor networks are used, has been "mildly soft."

Surface-mounted components are a different story, however, and have been showing continuing quarter-to-quarter improvements of 10% to 20%. The reason, says Polakowski, is that more companies are taking the plunge into surface-mounted technology. "When a large organization makes a commitment to do it, it comes along with a bang," says Polakowski. However, surface mounted components are still a very small part of Allen-Bradley's business.

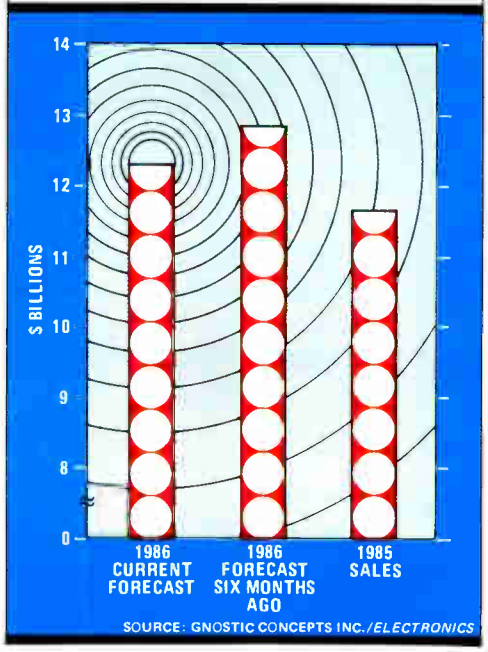
For the second half, Polakowski sees "a little bit of gradual growth. The prospects for the future are better because sooner or later, the computer business has got to get better," he observes. There are some signs of this, he says, in terms of quote activity. Because computer makers' inventories are low, a new product creates an immediate need for components.

There are no signs of an upturn for Peter B. Cherry, president of Cherry Electrical Products Corp., Waukegan, Ill. "I'm really pleased that things have stopped getting worse. But I don't see any reasons for us to be jubliant."

Nevertheless, there are a few bright spots compared with six months ago. The automotive business, to which Cherry supplies components, "continues to be good, but not great," he says. Cherry adds that he does see "some firming" in some of the company's traditional markets such as office equipment, home appliances, and in some segments of the data-processing-equipment business. □

Reporting was provided by Clifford Barney, Wesley R. Iversen, J. Robert Lineback, Jonah McLeod, Tobias Naegele, Craig Rose, and Larry Waller.

U.S. COMPONENT SALES



SELECTED U.S. COMPONENT SALES

	$ Million		
	1985	1986	1987
Passive/electromechanical components	11,622	12,316	13,466
Relays	704	723	738
Switches	193	194	205
Connectors and IC sockets	3,699	4,059	4,551
Capacitors	2,015	2,092	2,203
Resistors	953	957	984
Printed-circuit boards	4,058	4,291	4,785

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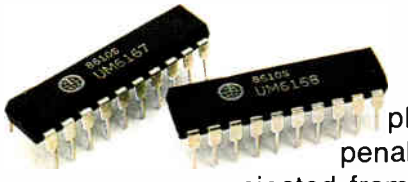

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MULTIBUS II HEADS FOR THE FAST TRACK

MESSAGE-PASSING CHIP THAT SPEEDS BUS ENTICES BOARD MAKERS

by Robert Rosenberg

After a stuttering start, Multibus II has begun to build up a head of steam. Intel Corp., the prime mover behind the synchronous bus standard for 32-bit microprocessors, came through this spring with the crucial chip for Multibus II—a message-passing coprocessor interface that enables both the system and local buses to work at top speed. As a result, Intel's bus has started to find the backing it needs to gain ground against the entrenched VMEbus.

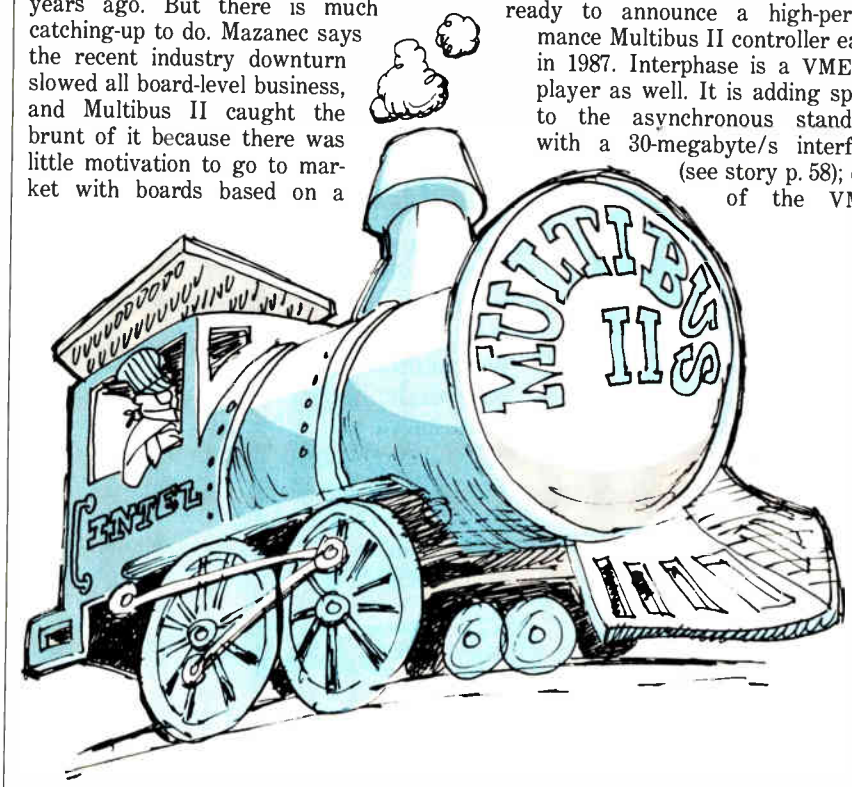
"Our best guess is that there should be about 50 vendors out there waiting to announce Multibus II products," says Fredrick J. Mazanec, president of the Microcomputer Interface Group, San Diego, which publishes several buyers guides for Multibus I, VMEbus, and other board-level products.

If Mazanec's numbers pan out, Intel and its fellow Multibus supporters will have achieved the critical mass they have been striving for ever since they first proposed the standard some three years ago. But there is much catching-up to do. Mazanec says the recent industry downturn slowed all board-level business, and Multibus II caught the brunt of it because there was little motivation to go to market with boards based on a standard that had gotten off to a slower start than the rival VMEbus [*Electronics*, Nov. 25, 1985, p. 48].

VMEbus, which represented a $125 million market last year, now has the backing of over 150 vendors with 1,100 products and is the acknowledged leader so far in the battle of the high-performance buses. Multibus II currently has 40 announced vendors offering some 100 products.

Multibus II's fortunes should see a tremendous turnaround in the next few months, Mazanec predicts. He expects that at least 50 from among the 1,500 board manufacturers he is surveying will be jumping on the Multibus II bandwagon. "By the fall, we should see Multibus with critical momentum," he says.

NEW PLAYERS. Some of the latest Multibus recruits are Siemens AG, Munich, and Interphase Corp., Dallas. The West German firm joined the camp in early April with a line of central processing unit boards, memory and input/output cards, and a line of communications and peripheral controllers. Interphase will be ready to announce a high-performance Multibus II controller early in 1987. Interphase is a VMEbus player as well. It is adding speed to the asynchronous standard with a 30-megabyte/s interface (see story p. 58); one of the VMEbus's weaknesses was its slow speed for many applications. Another prospect for the Multibus II camp is AT&T Information Systems, Morristown, N. J., which is sizing up both competing buses.



The dramatic improvement in Multibus II's fortunes can be traced directly to the long-awaited message-passing coprocessor [*Electronics*, April 21, 1986, p. 17]. Intel is touting the MPC as the keystone in a multiprocessing architecture—a single-chip hardware solution to the problem of controlling the communications between independent processors (be they 8-, 16-, or 32-bit) on the backplane.

"The MPC has changed the picture dramatically," says Rick Main, president of Zebu Corp., Sunnyvale, Calif., and independent analyst who follows the single-board-computer market. "It has changed the opinion of a lot of board makers. If I were starting a new company today, I'd probably do it with a Multibus II system."

A coprocessor like the MPC became essential because systems designers were putting so many intelligent functional elements, such as disk controllers and local-area-network controllers, on the bus that handling communications among them encumbered the host processor. Before the MPC came along, message-passing communcations on Multibus II's parallel system bus were limited.

Intel was not the only outfit to realize that the host processor on a busy bus needs help with communications to prevent contention among the devices tied into it. Central Data Corp., a Champaign, Ill., board maker, was also working on a system bus interface but stopped development earlier this year when it became clear that Intel had its one-chip solution in hand.

NCR Corp. has a three-chip set under development to handle message passing, but the set will not be ready until next year. One chip is already completed, and the other (which will be used twice in the interface) is still under development, according to Rodger Banta, director of external operations at NCR's engineering and manufacturing facility in Columbia, S. C. Banta says the NCR solution will have all the elements of the

Intel implementation as well as a feature to optimize memory-to-memory data transfers.

Previously, Intel was offering a two-chip solution of its own, a Bus Arbiter/Controller and a Message-Interrupt Controller. But the combination did not catch on. "I think a lot of vendors smelled a rat on the BAC/MIC," says Multibus Manufacturers Group executive director, Rob Hughes, in Aloha, Ore., "because the chips didn't go far enough in terms of their functionality. The MPC is what a lot of manufacturers have been waiting for."

INCOMPLETE. The Bus Arbiter/Controller and the Message Interrupt Controller did not have full message-passing capability. (Message passing generates an unsolicited message that is used to set up a data transfer and then transfer the data without the intervention of the CPU.) The BAC controlled the bus in multiprocessor systems by managing control lines and checking for errors, while the MIC generated interrupt messages and handled received messages from processor modules.

"Without message passing, Multibus II really would have little advantage over Multibus I," explains Jack Blevins, manager of new-product development at Central Data. "All Multibus II modules are treated as independent processors, albeit single-function processors. Message passing allows them to communicate without the slowest processor tying up the bus. You are going to get 100-ns transfers regardless of whether you have a 5-MHz, 10-MHz, 16-MHz, or 20-MHz processor. It makes no difference to the bus-transfer cycle."

Before the one-chip solution emerged, message passing typically was treated as a software problem that was solved during system integration. The MPC not only eases the burden on software designers but also ensures that block transfers of data packets will be handled in the same way on boards from different vendors. To do so, the MPC takes over interprocessor communications from the CPUs on the modules tied into the system; it also decouples the local bus from the parallel system bus. The decoupling of the local and system buses frees each bus to operate at maximum speed. Without CPU intervention, the MPC controls both message and data transfers across the bus, handling all the formating, arbitration, transmission, and parity generation needed to send the packets at the maximum bandwidth and speed of the bus.

The MPC interfaces to the on-board CPUs, the parallel system bus, and the interconnect space—the address space reserved in Multibus II for board identification, configuration, and diagnostic functions. The MPC offers its full 32-bit data and burst transfer capabilities to any processor accessing the bus. Small data transfers, such as status or service requirements, are handled as part of an interrupt—Intel says this can save up to three central-processor cycles on an operation. Another lift in performance comes from the message space defined in Multibus II for interprocessor communications. By exploiting this feature, the MPC offloads the CPU and eliminates the bottlenecks associated with a dual-ported architecture.

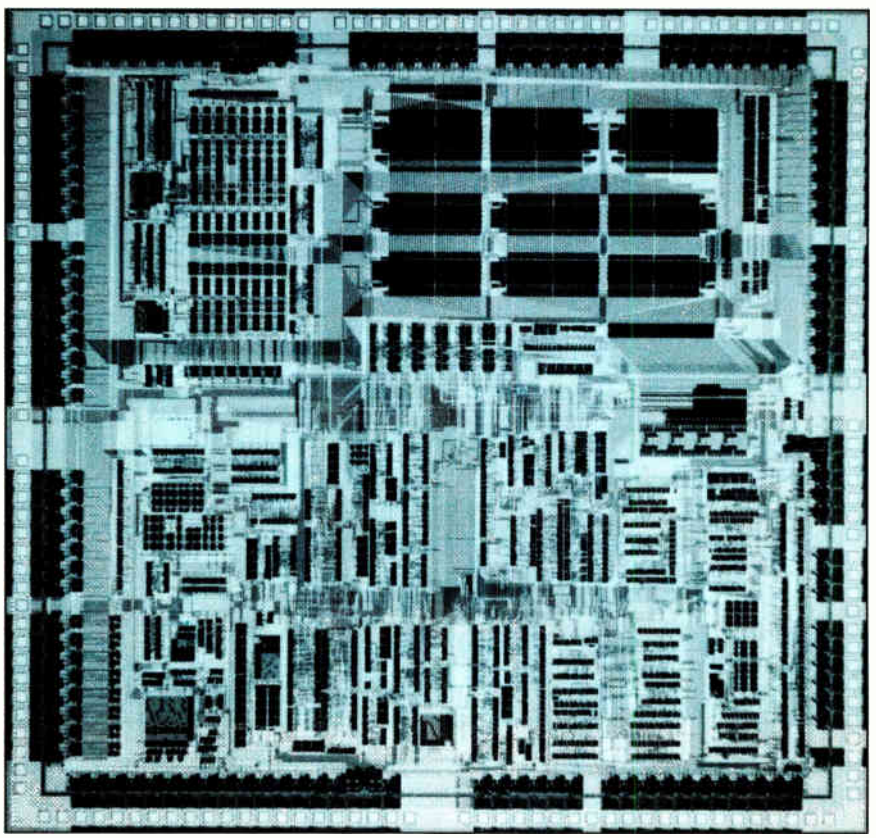
In addition to the extra cycles available from a processor freed from communication chores, the decoupling has other advantages. Resources contending for time on either the local bus or the system bus are not forced into wait states while arbitration is occurring. And because the MPC defines all the protocols for transfers, the system software does not have to coordinate shared-memory structures; this means that software applications can run independently on different processors.

The MPC frees up the increasingly busy host processor

Central Data's Blevins says that Intel's delivery of the MPC came none too soon for the marketplace. He points out that his company was anxious to migrate its Multibus I customers to the newer standard; but when Intel proved slow to deliver the part, other plans were made. "In late November or early December, it wasn't clear that Intel would deliver. They were already late. We began to design our own chip as a fallback position, though we didn't have the buffering or the speed independence of the MPC. We completed our design down through schematic capture and timing, but we stopped in early February when we got assurance that we could get the chip."

Interphase, too, had to bide its time until Intel came through. "We had to wait for the MPC to become available before we could get started" on the SMD controller, says Michael E. Cope, the firm's president and chief executive officer. With the MPC, the controller will be able to take full advantage of the message-passing capability of the Multibus II specification, Cope says.

The chip—packaged in a 140-pin grid array—is produced for Intel by VLSI Technology Inc., Phoenix, Ariz., using 2-μm design rules in a double-metal CMOS process. Sampling is under way and operations are going according to plan, reports Tom Kinhan, general manager of Multibus II operations at Intel. "We are shipping the chip and a board stuffed with an MPC and a 386 [80386 microprocessor]." □



SPEEDY DELIVERY. Intel's message passing coprocessor handles all the tasks that are necessary to send message packets at maximum speed among modules on a Multibus II.

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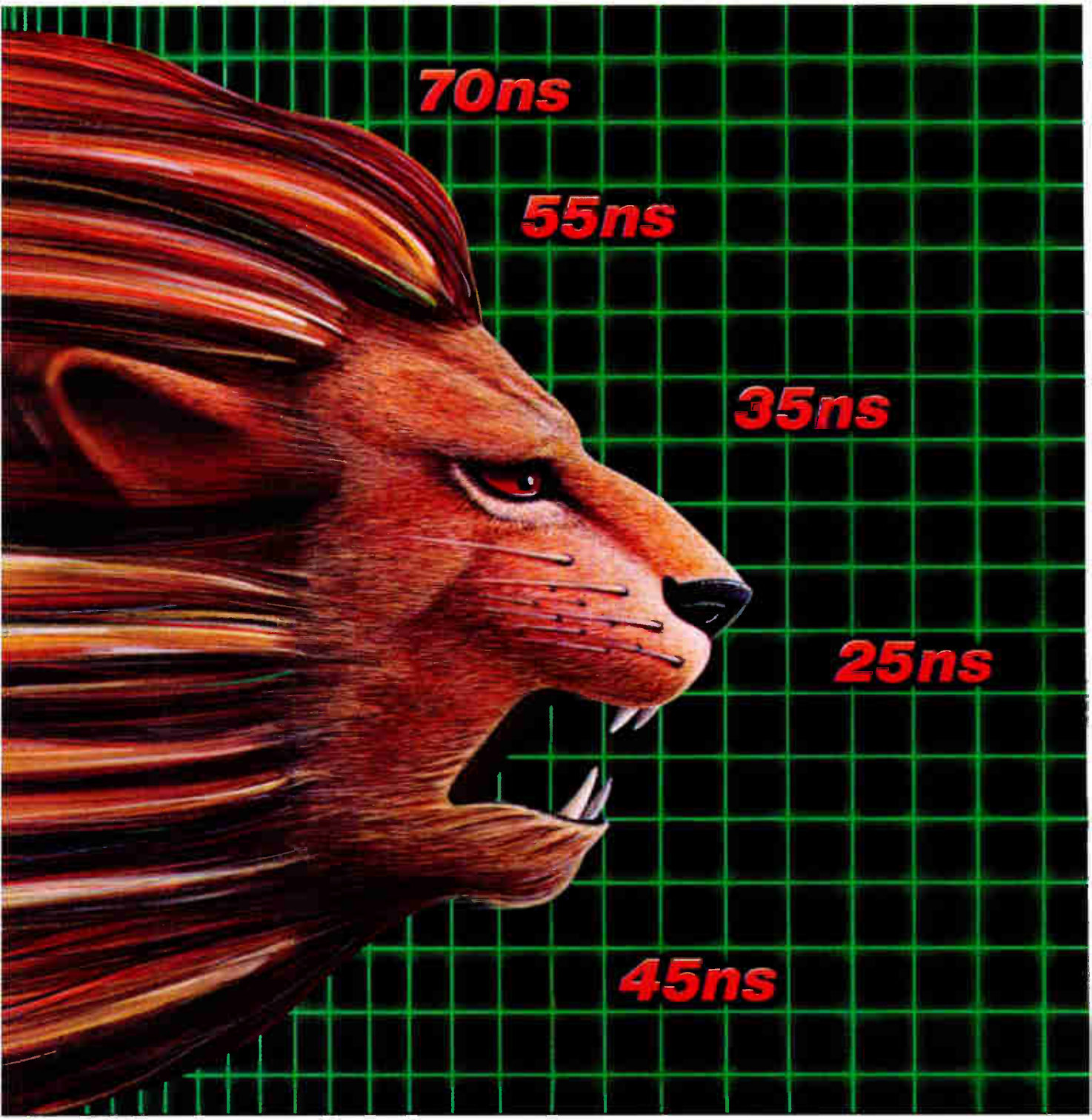

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TMM2078D	4KX4	45	22P	CDIP	NOW	NOW
TMM2078D	4KX4	35	22P	CDIP	NOW	NOW
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EUROPEANS ARE COUNTING ON UNIX TO FIGHT IBM

X/OPEN GROUP WORKS FOR A STANDARD OPERATING SYSTEM

by Robert T. Gallagher

PARIS

European computer makers, with some help from U. S. companies, are once again trying to unite and head off IBM Corp. Although the field is littered with the remains of failed attempts at transnational cooperation, this time the companies have a plan that is simple and so far appears workable.

The manufacturers—seven from Europe plus two from the U. S.—want to keep IBM from dominating the European minicomputer and high-level workstation market as it does the mainframe business (with 65% of the total) on the Continent. They plan to do this by establishing AT&T Bell Laboratories' Unix operating system as a Europe-wide standard. That would enable each company to retain its identity in the fiercely nationalistic European markets even as it produces systems that are compatible with other systems.

To accomplish this, the nine firms have formed the X/Open Group. It is a logical extension of a European standardization movement that is far more advanced than anything that has so far developed stateside [*Electronics*, April 28, 1986, p. 48].

The first major step of that movement was the establishment of the Open Systems Interconnection protocols by the International Organization for Standardization and the International Telegraph & Telephone Consultative Committee. The protocols serve as standards for interfacing and networking data-processing systems, and they have been widely accepted worldwide for all levels of computers.

With the success of OSI in mind, the X/Open group is set on extending the standardization effort to operating systems. The reasoning behind the move is simple enough: with both networking interfaces and operating systems standardized, purchasers of data-processing systems will be able to enjoy a significant degree of supplier independence.

With X/Open, users could connect heterogeneous equipment through OSI links and then achieve applications portability with Unix. European equipment manufacturers reckon X/Open will effectively preempt any attempt by IBM to establish de facto minicomputer standards, as it has for mainframes and personal computers. Many industry observers feel that the move toward Unix is so strong that IBM itself will have no choice but to offer it for its own minicomputer line.

The idea of forming the X/Open Group was a 1984 brainchild of Robb Wilmot, who was chief executive officer of England's International Computers Ltd. plc before cofounding Silicon Structures [*Electronics*, Sept. 8, 1985, p. 25]. It began with only five members. It now includes, in addition to ICL, Dutch multinational Philips, France's Bull, Italy's Olivetti, Sweden's Ericsson Information Systems, and West Germany's Nixdorf Computer and Siemens, as well as the European subsidiaries of America's Digital Equipment and Sperry.

EXCLUSIVE CLUB. The X/Open member firms expect their group to expand over the years, and they already have applications from a number of companies, although they decline to name them. They will make a point of adding new members slowly, however, as they feel that the group's exclusivity has been one of the keys to its operational efficiency.

The group's initial objective was twofold: to promote a standard version of Unix and to foster the acceptance in business applications that it has in the

X/OPEN GROUP MUST DEAL WITH A WIDE RANGE OF SYSTEMS

Maker	Country	Minicomputers and work stations	Operating systems
Bull	France	SPS5, SPS7	Unix
		SPS9	Ridge
		DPS-9	GCOS or Unix
		Questar 400	Unix
DEC	U.S.	VAX	VMS, Ultrix-32
		Microvax	MicroVMS, Ultrix-32M
		VAX stations	MicroVMS, Ultrix-32M
		PDP-11 family	RT-11, RSX-11, RSX-11M, RSX-11M+, RSTS/E, CTS-300, MicroPower Pascal, COS-310, Ultrix-11
Ericsson	Sweden	2500	Eritron
		Work stations (licenses from Sun)	Unix
		286	MS-DOS, Xenix
ICL	England	CLAN 3, CLAN 7	Unix
		DRS 300	Unix and C-DOS
		3300	Unix
Nixdorf	West Germany	8810	MS-DOS
Olivetti	Italy	M-30, M-40, M-60	MOS
		3B2/300, /310, /400; 3B5, 3B15 (from AT&T)	Unix
Philips	Holland	P800	MAS
		P4000	DINOS
		PTS 6000	TOSS
Siemens	West Germany	SICOMP M20, M30, M60-70, R10	AMBOSS-4
		SICOMP R20, R30, R40	ABBOSS-3
Sperry	U.S.	5000/20, /40, /50, /60, /80, /90	Unix
		1100	SX1100

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NEW PRODUCTS

UNIX WORK STATIONS COST ONLY $5,000 PER MIPS

INTERGRAPH USES CLIPPER CHIP SET TO BOOST PRICE-PERFORMANCE RATIO

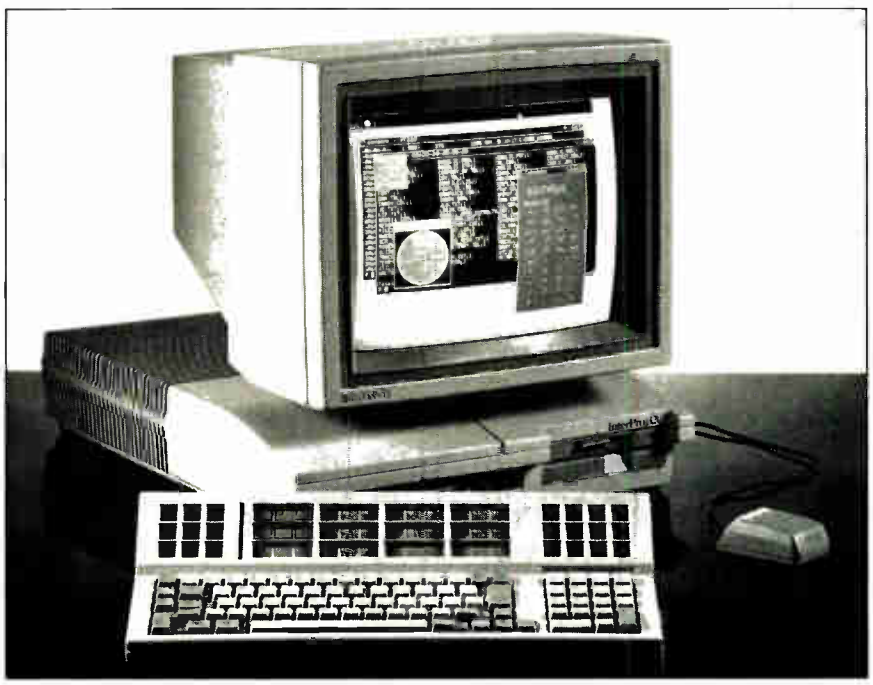
Last spring, a team from Fairchild Semiconductor Corp. flew to Huntsville, Ala., to sell Intergraph Corp. on the idea of designing a new generation of graphics work stations around the chip maker's then-unannounced Clipper 32-bit microprocessor. Thus were born the work stations that Intergraph introduced last week at the Design Automation Conference in Las Vegas.

Not only was the Fairchild trip successful, but the two companies then joined in a strategic partnership that Bruce E. Imsand, Intergraph's vice president for systems development, calls a "true symbiotic relationship." The teaming has already produced an amazingly fast product-development effort. In just one year, Fairchild has won its first Clipper design-in and Intergraph has introduced a low-cost, stand-alone Unix work station it claims will cost customers far less per million instructions/s than any competing product. In addition, Fairchild got an alpha-test customer for the Clipper.

"The Clipper has the speed and horsepower needed for today's design- and analysis-simulation problems," says Hal Barbour, Intergraph's executive manager of electronics marketing. A year ago, customers were demanding a lot more power for stand-alone applications; to accomplish this, Intergraph was looking at microprocessor designs from Intel Corp. and National Semiconductor Corp., as well as from Fairchild.

But when Howard G. Sachs, general manager of Fairchild's advanced processor division, launched his pitch, it sounded very familiar to Imsand; indeed, he had already pitched the same approach to his bosses at Intergraph. "Both Bruce and I had the same idea of architecture," Sachs adds. "We were even planning to use the same operating system [AT&T's Unix System V] and compilers [from Green Hills Inc.]," says Imsand.

The 32C family, which executes instructions at an average of 5 mips, is priced starting at $25,000, or only $5,000 per mips. This figure compares with a cost of $10,000 to $13,000 per mips for such competitive systems as Apollo's, Intergraph engineers claim. The system also performs double-precision floating-point calculations at 2 million whetstones/s, they maintain.



FAST DESIGN. Intergraph's 32C work stations hit an average of 5 mips.

Up until two weeks ago, though, Barbour didn't know if the Clipper-powered work station would be ready in time to announce at the design automation conference. But Intergraph decided to go for it, he says, when it was able "in the past month or so to get some of its applications up and going on Fairchild's first silicon."

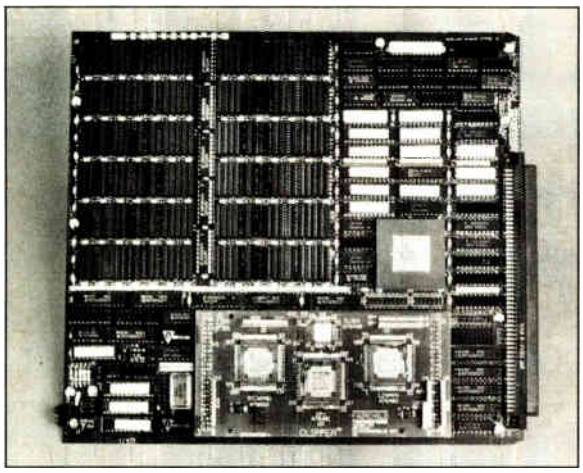
CLIPPERS ARE READY. Teaming up, Barbour says, helped both companies accelerate their product development, each saving from three to six months. Intergraph plans to begin production shipments by October, and Sachs says Fairchild will be in volume production by then. "We've already got several hundred Clipper CPUs built up right now."

Intergraph's InterAct 32 and InterPro 32 work stations, introduced a year ago and designed around National's 32-bit 32032 microprocessor, can be upgraded by simply plugging a Clipper module into the main CPU board. Intergraph's Clipper module is packaged slightly differently than the standard module that Fairchild sells. Intergraph had to write a new code generator for the compiler to produce code for the Clipper instruction set and do a little tweaking of the operating system.

The new work stations run on the basic Unix System V operating system, can emulate Digital Equipment Corp. VT-100 and -220 terminals, and come with screen-management software. Each has 6 megabytes of main memory, an 80-megabyte hard-disk drive, and a 1.2-megabyte floppy-disk drive.

For full-time production environments, the InterAct 32C, starting at $40,000, has dual screens, ergonomic design, and a built-in digitizing tablet. For the designer, the InterPro 32C, beginning at $25,000, features a compact desktop design suitable for the office and is available with either 15- or 19-in. color monitors that can display 322 colors from a palette of 4,096.

Both work stations have addressable resolutions of 1,184 by 884 pixels with



NEW CARD. At Intergraph's request, Fairchild modified the card that holds its 32-bit Clipper chips.

60-Hz noninterlaced refresh rates. A 10-MHz 80186 microprocessor runs all I/O operations and gives them the ability to run PC-DOS applications. Built-in local-area networking is provided through an IEEE 802.3 (Ethernet) link to access a data base in a DEC VAX host computer.

The work station architecture consists of three independent subsystems—processor/memory, networking, and graphics management—with defined interfaces. Users can therefore implement new technology in one subsystem without affecting the rest of the system.

Intergraph is just the first of several customers that will announce commitments this summer to use Clipper in their product families, according to Fairchild. Clipper consists of three CMOS chips, a CPU with on-chip floating-point execution unit, and two combination cache/memory-management ICs. The two cache chips are linked to the CPU over a dual-bus architecture; one 32-bit bus is dedicated to instructions, the other is dedicated to data. *–Robert W. Henkel*

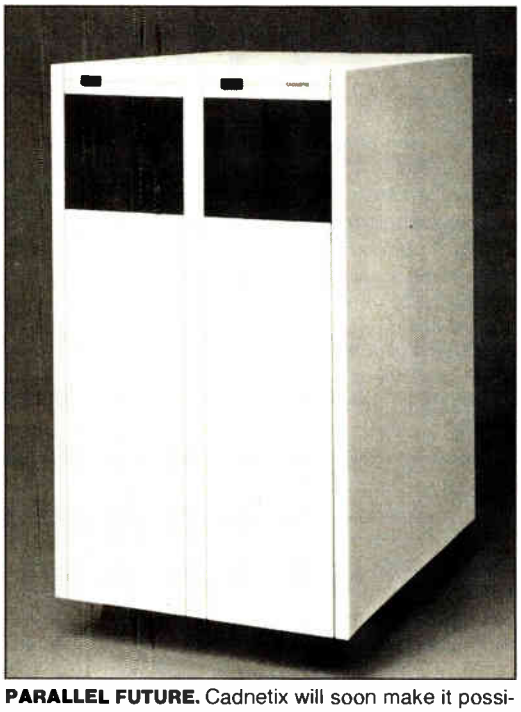
Intergraph Corp., 1 Madison Industrial Park, Huntsville, Ala. 35807. Phone (205) 772-2000 [Circle reader service number 340]

CAD/CAE ACCELERATOR ROARS ALONG AT 10 MIPS

Users of Cadnetix' soup-to-nuts line of computer-aided-engineering and -design equipment can add a general-purpose accelerator that performs 10 million instructions/s. The CDX-760 general-purpose engine, a card with up to 8 megabytes of on-board memory, is the first system to make use of the high-speed, reduced-instruction-set-computer technology chip set from Mips Computer Systems Inc. An option permits the CPU card to be used in parallel-processing applications with other Cadnetix design tools.

The accelerator, one of two major Cadnetix introductions at the Design Automation Conference last week in Las Vegas, is designed to be fully compatible with the company's application-specific engines, such as the CDX-77000 Simulation Engine, the CDX-7900 Physical Modeling Engine, the CDX-79000 Analysis Engine, and the CDX-7100 and 7200 Database Servers [*Electronics*, Feb. 17, 1986, p. 54].

The company also announced a reconfigured version of its analysis engine that allows users to select a configuration exactly suited to their needs. The analysis engine, which can include the CDX-760 GP Engine, comes in setups for simulation, physical modeling, compilation, or any combination of the three.



PARALLEL FUTURE. Cadnetix will soon make it possible to configure up to five engines in a single chassis.

The CDX-760 GP Engine is designed for applications where the overhead required for application-specific engines does not justify their use. That's why the company is initially offering the general-purpose accelerator with Berkeley Spice and data-base compilation—applications where the use of a general-purpose accelerator is most cost-effective.

PARALLEL POTENTIAL. The GP Engine has an interprocessor-communications port built into it, making parallel processing possible. In addition, Cadnetix modified another product, a microcoded bit-slice application-specific engine, to include an interprocessor communications facility.

In the future, it will be possible to configure any combination of up to five engines in a single chassis. This would give the engineer local access to physical modeling and data-base sharing, and local acceleration of compilation, logic simulation, and Spice execution. System performance would be boosted because the user would not encounter network traffic or competition between nodes for remote resources.

The parallel-computing capability is something Cadnetix is now putting into its full product line in anticipation of applications to be released in the future.

The CDX-760 gets its speed from the Mips Computer architecture, which uses RISC technology [*Electronics*, May 5, 1986, p. 56]. The Mips chip set offers high speed at a low price, and Cadnetix says its new system will operate 3 to 10 times as fast as a Digital Equipment Corp. VAX 11/780.

Implementing the Mips RISC architecture in a system compatible with Cadnetix' other products without sacrificing speed was simple, the company says, thanks to Mips Computer's optimizing compiler system, which translates high-level-language instructions into machine code suited to the chip set's RISC design. The compiler consolidates redundancies and passes data to on-chip registers, where it is accessed more easily, to keep processing speed up. Cadnetix also plans to offer a C compiler and debugging utilities for the GP Engine later this year.

The GP Engine is priced from $29,900. The data-base compilation application costs an additional $5,000, and pricing for Spice has not yet been set. A Unix operating system with a C compiler and debugging utilities will cost $120,000. Pricing for the Analysis Engine ranges from $84,800 to $127,900, depending on the configuration chosen. All the new offerings will ship in the fourth quarter. *–Tobias S. Naegele*

Cadnetix Corp., 5757 Central Ave., Boulder, Colo. 80301.
Phone (303) 444-8075 [Circle 343]

MS-DOS PACKAGE WRITES USER INTERFACES

Part of writing any application program is setting up the screens and control routines that form the user interface. This universal programming job is greatly simplified by Trilobyte Software Systems' software-development package called Access, which is now available for MS-DOS-based computers. Access not only automates the processes of designing screens and determining security levels, it also serves later to perform remote maintenance over asynchronous telecommunications links.

Access was originally written to run on IBM Corp. mainframes under the Customer Information Control System. Its author, Stephen J. O'Kane, has now produced a functionally identical version in 8088 assembler language, giving programmers the same capabilities on an IBM Personal Computer or compatible. It's intended for corporate management information system departments, value-added resellers, and original-equipment manufacturers.

Access includes separate modules for security, screen control, and maintenance. The security system, which protects application files from unauthorized access, is an assembler routine that uses hidden directories and files to conceal passwords and data files. Only a sophisticated programmer who knows how to disassemble files can access the data, says Trilobyte president Jerome Draper.

WINDOW CONTROL. The screen-control module lets the programmer set up fields and windows, manage the cursor, define function keys, set system parameters, and do other jobs necessary to let a user run an application. Like the security module, the screen-control segment is menu-driven.

The third module sets asynchronous communications parameters and makes it possible for Trilobyte, or a value-added or OEM reseller, to perform remote support over dial-up lines. Rather than walk a naive user through an unfamiliar program on the telephone, the seller can take control of the remote system and fix bugs on-line.

Access interfaces with compiled programs written in Basic, Pascal, Cobol, and C. With a compiler plus software for manipulating files, the system can be used to write tailor-made applications on the IBM PC, Draper says.

Remote access requires that the remote station have a run-time version of Access, which is provided free by Trilobyte. Access itself, which is not copy-protected, sells for $245 and is available now. The program includes source code for 75 assembler subroutines that set up screens and perform other functions. A 300-page documentation book accompanies the software.

Trilobyte Software Systems, 295 Los Angeles Blvd., San Anselmo, Calif. 94960. Phone (415) 457-3431 [Circle 341]

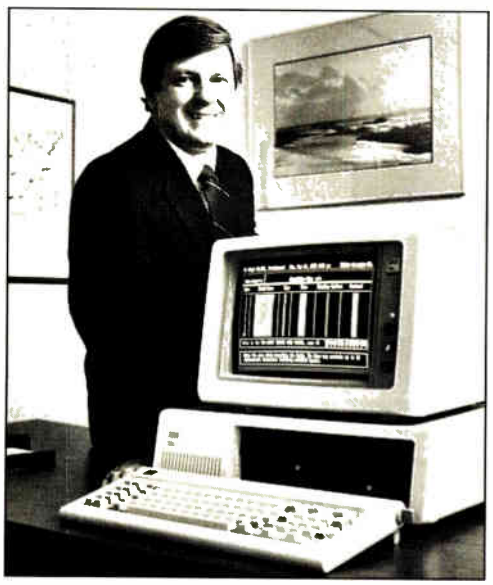
MENUS SET UP UNIX DATA BASES

An application-program generator and data-base manager cuts by 80% the time it takes to develop customized Unix applications. Parameter Driven Software's PDS-Adept Unix product complements the company's earlier Adept packages for MS-DOS and PC-DOS-based machines such as the IBM Corp. Personal Computer, PC/XT, and PC AT, as well as for systems using hardware from Convergent Technologies that rely on the CTOS or BTOS (Burroughs version) operating system [*Electronics*, Nov. 4, 1985, p. 34].

The addition of PDS-Adept Unix to the Adept family will be especially useful to companies that have a variety of small computers based on different operating systems, says PDS president Patrick K. Comeaux. That's because the company offers an optional conversion filter with which programs created with PDS-Adept Unix can be converted automatically for use on systems that run under MS-DOS, PC-DOS, CTOS, or BTOS. Similar conversion filters sold for the company's earlier MS-DOS/PC-DOS- and CTOS/BTOS-based Adept packages also allow automatic conversion from either of those operating systems to either of the others.

Like its predecessors, PDS-Adept Unix enables computer users who are not programmers to create customized, ready-to-run programs simply by filling in the blanks on display-screen menus. For example, the user might be asked, "Should customers' names appear in alphabetical order?" Or the user might be directed to "Fill in the name and model number on this product." The parameters established by the user's answers then drive the Adept package's processing functions for manipulating the data base.

A program that might take two to three months to write using conventional programming languages such as Cobol, Pascal, or C could be created in only two weeks using PDS-Adept Unix, says Comeaux. Some simple programs can be created in minutes, he says.



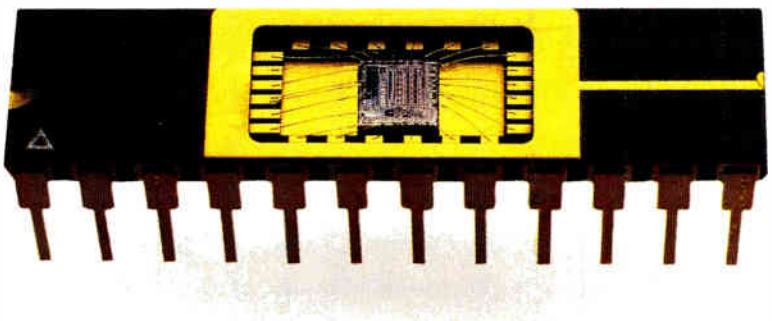
CONVERSION. Filters let PDX-Adept users convert programs from one operating system to another.

PDS-Adept Unix will run on computers operating under AT&T Bell Laboratories' Unix System V, including the AT&T Co. 7300 and 3B series, the Burroughs Corp. XE 550 and Convergent Technologies Inc. Miniframe, Megaframe and Mightyframe series. PDS will also offer a suite of 10 Unix System V-based general-purpose business-application programs created using the Adept package. Business users can use PDS-Adept Unix to easily modify these programs to suit their needs and can also use the new Unix-based program generator to interface Adept-created packages with existing in-house software.

Package prices depend on the target machine. For Unix-based personal computers such as the 7300 or 3B/1, the package is priced at $995. For larger multiuser systems such as the 3B/5, the XE 550 or Megaframe-based systems, the package sells for $4,000. The conversion filter for PDS-Adept Unix sells for $750. PDS-Adept Unix is available now from 180 U. S. dealers, and internationally through a network of distributors and original-equipment manufacturers. *–Wesley R. Iversen*

Parameter Driven Software Inc., 30800 Telegraph Rd., Birmingham, Mich. 48010. Phone (313) 540-4460 [Circle 342]

REVOLUTION BY ANALOGY.



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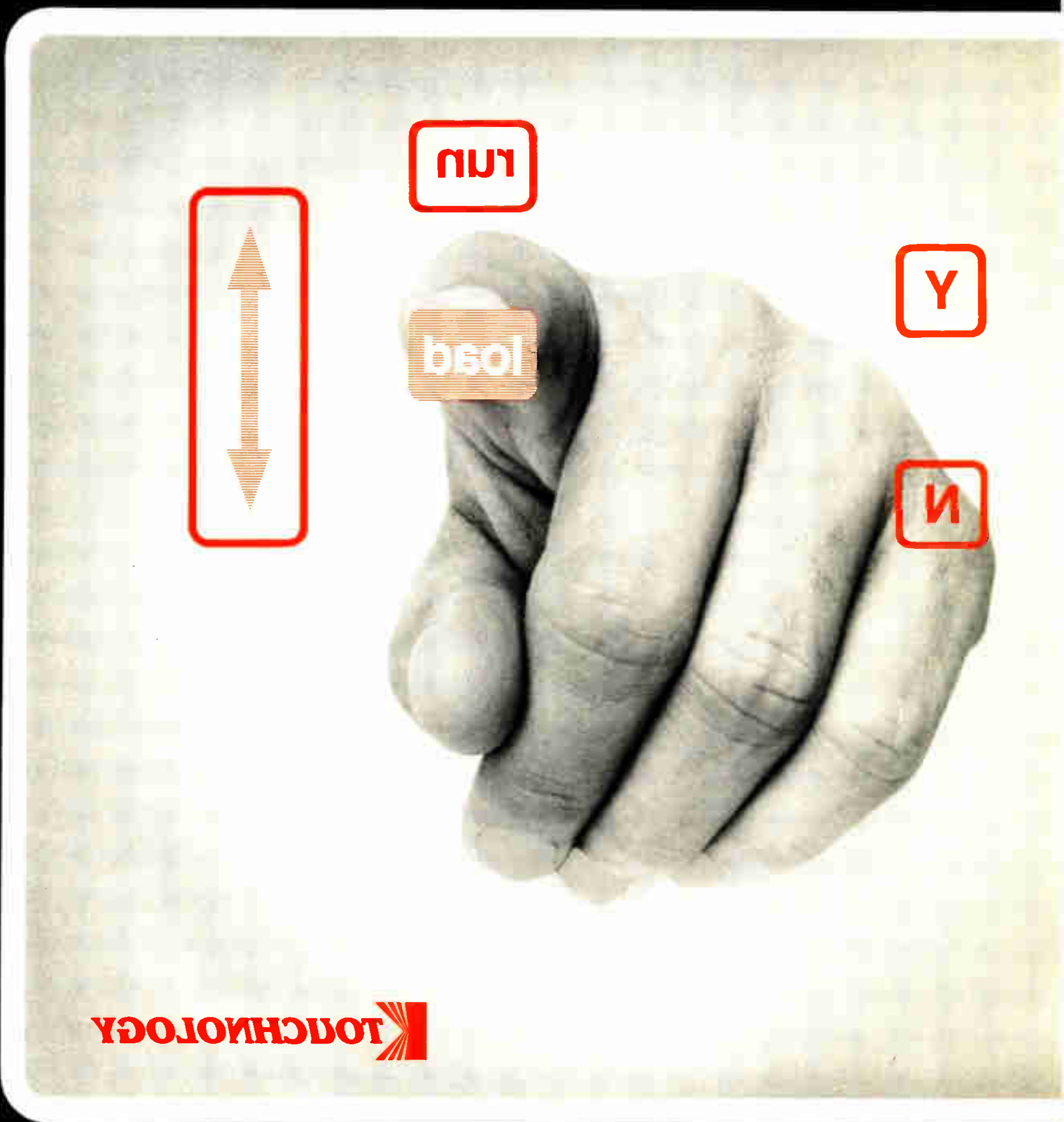

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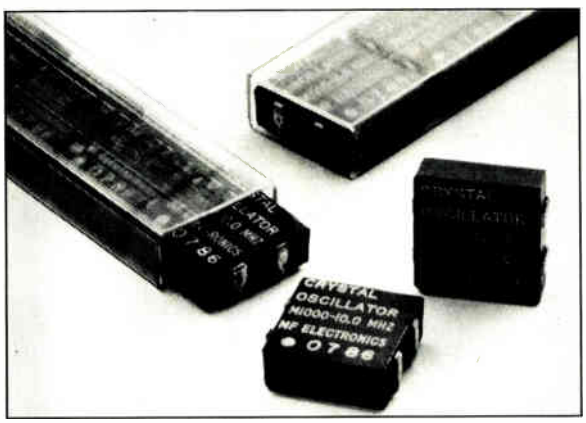
A tiny thick-film hybrid oscillator for computer clocking applications resolves a problem in surface-mount technology. MF Electronics Corp.'s series M1000 crystal-stabilized oscillator is housed in a J-leaded plastic package that is handled without damage by SMT pick-and-place machines.

Other companies have supplied quartz crystals housed by themselves in surface-mount packages. And some complete crystal oscillators are available in 24-pad ceramic leadless chip carriers. But ceramic, unlike plastic, is abrasive, and wears down the pick-and-place system's "fingers." In addition, fragile ceramic packages easily crack during shipping, handling, and assembly on pc boards.

With only three circuit elements—a quartz crystal, a bypass capacitor, and MF Electronics' custom Clockchip—the oscillator is inherently reliable since it minimizes the number of wire-bond connections.



NO DAMAGE. MF's crystal oscillator comes in plastic J-leaded packages for safe handling by pick-and-place machines.

ALL THE CIRCUITRY. The Clockchip contains all the oscillator's analog and digital circuitry. This chip uses an internal reference source to define the crystal-excitation voltage. It also has a gain-controlled amplifier functioning within an error-detecting feedback loop to sustain crystal excitation through temperature and supply-voltage variations and component changes due to aging.

The Clockchip also permits either a fundamental or third-harmonic mode of oscillation to be selected by wire-bond connections to the desired filter. The chip has a Schmitt trigger and Schottky gate to produce fast-rise-time square waves for circuit timing. The Clockchip, along with the other two elements, are attached to a thick-film circuit pattern on an alumina hybrid substrate.

After wire bonding and testing, the finished hybrid is hermetically sealed in a metal can, and the entire assembly is then molded into the plastic surface-mount package. A high-melting-point solder is used in the oscillator's construction, permitting the device to undergo prolonged exposure to the high temperatures of SMT soldering systems.

Overall, the M1000 oscillator, including its J leads, measures only 0.45 by 0.49 in., which amounts to an area of less than ¼ in.^{2} Its seated height is less than 0.2 in. Because the J leads are resilient, they can flex during pc-board insertion into system slots and provide protection against vibration during shipping and field use.

The M1000 parts run at any customer-defined frequency from 4 to 48 MHz and have guaranteed frequency stabilities to within 0.01%, 0.05%, and 0.1%. Power consumption from the 5-V supply is typically 35 mA; the oscillator delivers a 4-V square-wave output that can drive up to 10 TTL loads.

The surface-mount oscillators sell for less than $2 in production quantities. Evaluation units at standard frequencies are available from stock and production orders can be shipped in four to eight weeks. The oscillators are supplied in plastic antistastic tubes, or in 24-mm tape and reel form. *–Jerry Lyman*

MF Electronics Corp., 10 Commerce Dr., New Rochelle, N. Y. 10801.
Phone (914) 576-6570 [Circle 400]

SURFACE-MOUNT AMPS HAVE 9.0-dB GAIN

Two surface-mountable amplifiers have a minimum gain of 9.0 dB. Typically, the PlanarPak devices have gains of 10.0 dB over their full 500-MHz-to-2-GHz frequency range.

The models PPA-2012 and PPA-2013 have maximum noise figures of 4.0 and 5.5 dB and typical power output of +13.0 and +21.0 dB, respectively. Both amplifiers have maximum voltage standing wave ratios of 2.0 : 1.

The PlanarPak package is only ⅜-in.^{2} and weighs 0.5 gram. Its surface-plane leads may be trimmed off for reflow soldering. In lots of one to nine pieces, the PPA-2012 is priced at $290 each and the PPA-2013 at $330 each. Both are available now.

Avantek Inc., 3175 Bowers Ave., Santa Clara, Calif. 95054.
Phone (408) 970-2583 [Circle 403]

DC-TO-DC CONVERTER HAS I/O ISOLATION

By using a new design for the feedback loop, Rifa is able to add input/output isolation to its PKA line of 25-W miniature dc-to-dc converters without cutting back on the targeted reliability level of 200 years (at +45°C) mean time before failure. The isolated versions are available in 24-V and 48-V input ratings.

Three models of each type are available: one with +5 V at 5-A or +12 V at 1-A outputs; one with only 5 V at 5-A outputs; and one with +12 V at 2.5-A outputs.

The converters measure 2.9 by 2.9 by 0.7 in. and are available on printed-circuit boards or as a chassis-mountable version housed in an aluminum case for convection cooling. The isolated PKA power supplies sell for $122 each in small quantities. Samples are available now.

Rifa Inc., Greenwich Office Park #3, P. O. Box 3110, Greenwich, Conn. 06836.
Phone (203) 625-7300 [Circle 404]

PANEL-MOUNT PRINTER USES THERMAL PAPER

The Mini-Printer-24 digital panel printer connects to any Centronics parallel port and produces dot-matrix printouts on thermally sensitive paper. The 24-column printer has a character set that includes 250 letters and symbols.

A built-in memory and character generator simplifies the interface to the computer or data-logging device. The printer allows upright and inverted

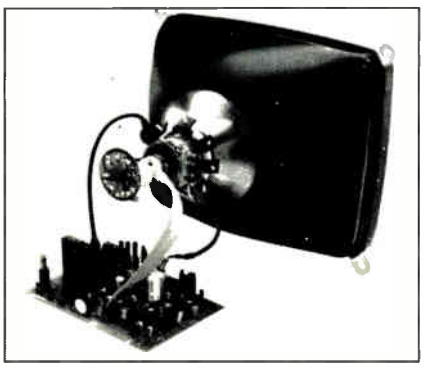
printing and it can also print double-wide characters. Characters are printed in a 5-by-7-dot matrix. Available from stock, the unit sells for $199 each.

MetraByte Corp., 440 Myles Standish Blvd., Taunton, Mass. 02780.
Phone (617) 880-3000 [Circle 405]

$186 CRT DISPLAYS 1,024 BY 1,024 PIXELS

The 300MDX monochrome CRT, which has a 1,024-by-1,024-pixel resolution, is priced as low as $186 each in large quantities. The CRT comes in 9-, 12-, or 14-in. sizes and can be provided in kit, chassis, or cabinet configurations.

The 64-kHz CRT's deflection system is compatible with all popular 90° and



110° CRTs. It accepts either Schottky TTL or emitter-coupled-logic video signal inputs with full gray-scale display and requires a 24-V input. The 300MDX is available now.

Digitran/Computron, 3100 New York Dr., Pasadena, Calif. 91107.
Phone (818) 791-5600 [Circle 406]

THERMAL PLOTTER DOES A PAGE IN 15 S

Superplot-80L, an 80-column thermal printer and plotter, can produce a typical page of graphics in less than 15 seconds, thanks to built-in vector graphics routines. The plotter, which measures 4.2 by 10.7 by 10.5 in., can be mounted in a front panel.

The plotter uses a linear-array thermal printhead that does in excess of 71 dot-lines/s and near-letter-quality alphanumerics at over 500 characters/s. The company says the printhead has a resolution of 100 dots/in. and a life of 100

million dot-lines or 17 miles of paper.

The Superplot-80L has an 8-in.-wide printable field on 8½-in.-wide thermal roll paper. A top-of-form optical sensor indexes page tops for proper alignment. The unit comes with three standard interfaces: Centronics, 8-bit parallel, and page-level vector graphics. Available 90 days after ordering, the Superplot-80L is priced at $2,095 in single quantities.

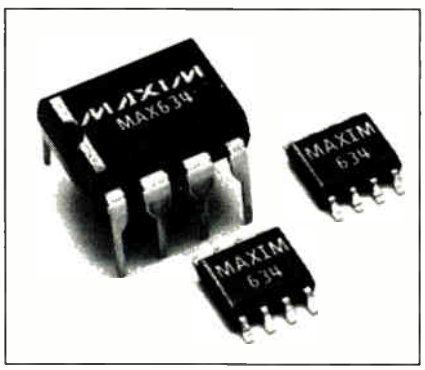
Gulton Industries Inc., Graphic Systems Division, Gulton Industrial Park, East Greenwich, R. I. 02818.
Phone (401) 884-6800 [Circle 408]

CMOS REGULATORS ARE 85% EFFICIENT

Two low-power CMOS dc-to-dc inverting converter/regulators are targeted for operation in the range from 5 to 500 mW. A single inductor, a diode, and two set resistors are the only external components required to convert an unregulated positive voltage to a regulated negative voltage.

The MAX634 and MAX4391 achieve efficiencies up to 85% and can operate over a voltage range of +2 V to +16.5 V and +4 V to +16.5 V, respectively. The output voltage may be up to −20 V, with the restriction that the total input-output voltage differential must never exceed 24 V.

The chips, which can replace bipolar parts, have an operating current of only

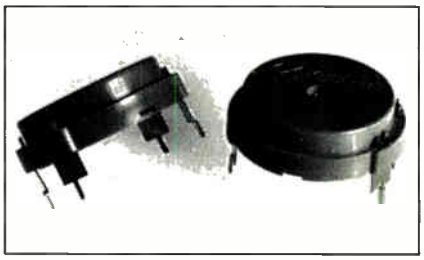


70 μA. Housed in 8-pin Cerdips, the devices are available in the commercial, industrial, and military temperature ranges. The MAX4391 is priced starting at $2.71 and the MAX634 starts at $2.90, both in lots of 100 pieces.

Maxim Integrated Products, 510 N. Pastoria Ave., Sunnyvale, Calif. 94086.
Phone (408) 737-7600 [Circle 411]

TRANSDUCER WARBLES BETWEEN TWO TONES

The KBT-33SB-2T piezoelectric transducer has a dual resonant frequency near 1 kHz and a resonant impedance of 3.5 kΩ maximum. The device's low, easy-to-hear tones are produced when sound is warbled between frequencies.



The solid-state device is designed for computer printers, telephones, modems, and security systems. It features four pins for mounting stability and a 12.5-mm stance for easy insertion in 30-mm lead spacings.

The transducer, which operates without inductive coils, has a sound pressure level of 70 dB minimum and an input voltage of 20 V peak-to-peak. In lots of 10,000 pieces, the transducer sells for 58¢ each. Delivery takes eight to ten weeks after ordering.

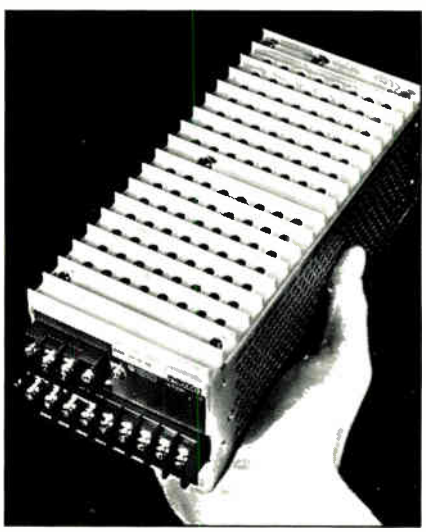
Kyocera International Inc., Electronic Components Group, 11425 Sorrento Valley Rd., San Diego, Calif. 92121.
Phone (619) 454-1800 [Circle 407]

SMALL CONVERTERS PUT OUT 150 W

The ERD series of dc-to-dc converters is available in models that range in power from 30 to 150 W and feature 300-kHz switching frequencies. The 30-W models accept inputs of either 24 V or 40 V and are priced at about $135 each. The 60-W supplies go for $160 each and the 150-W models at $225.

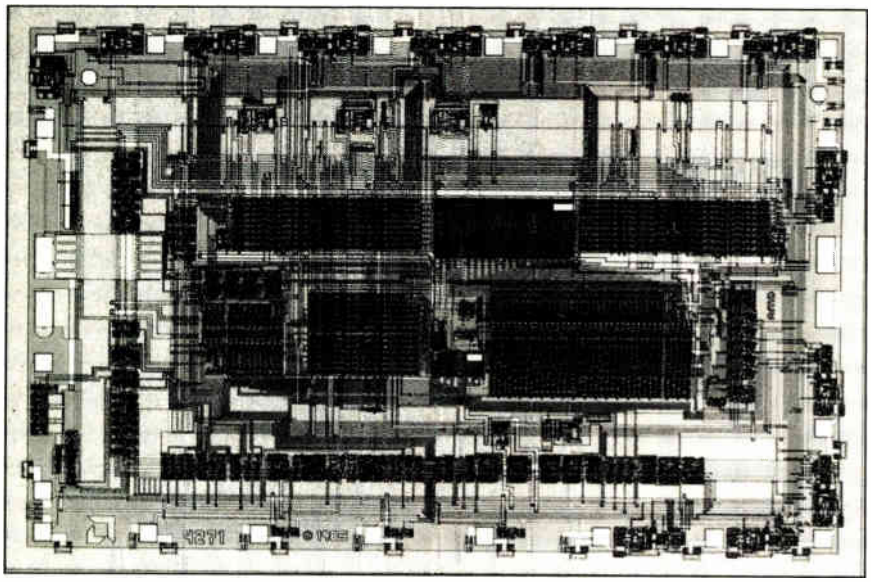
The high frequency results in significant size and weight reductions compared with earlier designs. The converters are hybrid microcircuits containing surface-mounted devices on a ceramic substrate. They boast a mean time before failure of 250,000 h. The converters are available from stock.

Kepco Inc., 131-38 Sanford Ave., Flushing, N. Y. 11352.
Phone (718) 461-7000 [Circle 409]



DIGITAL TIMER CUTS THE ANALOG CONNECTION

AMD's PROGRAMMABLE EVENT GENERATOR PUTS OUT 12 WAVEFORMS TO TACKLE TOUGH TIMING PROBLEMS



BIG SAVINGS. AMD's programmable event generator replaces $30 worth of components.

Even in the most advanced digital systems, analog circuitry plays a major role in timing. But now a monolithic digital timer from Advanced Micro Devices lets engineers rid their designs of hard-to-use analog delay lines, cumbersome counters, and RC networks. In addition, the AM2971 programmable event generator can serve as a general-purpose user-programmable timing and waveform generator.

The Am2971 achieves a resolution as precise as 10 ns between system timing events, enabling designers to tailor system timing for peak performance. It offers 12 programmable, registered output waveforms, giving users the flexibility to define 12 independent timing signals. "The chip is the first in a family of monolithic chips for solving timing problems previously handled by hybrids," says Larry Wittenbaugh, the chip's marketing manager.

START/STOP CONTROL. The chip also features programmable control of the timing sequence for start and stop functions. Users can pick one of eight start addresses to begin the timing sequence. The event generator's programmability and its many outputs mean it can replace several delay lines at one time.

The chip suits a wide variety of timing-control applications in digital systems. It can replace analog delay lines and combinatorial logic required to accurately generate the complex clock signals required by address-multiplexed dynamic RAMs. For example, it can generate timing for the Am2968 Dynamic Memory Controller and Am2969 Memory Timing Controller. Typically, the timing controller generates the row-address strobe input signal whenever a refresh or a memory cycle is requested. This signal provides a leading edge to the Am2971's trigger output, thus initiating the user-defined timing sequence.

The chip is ideal for designing page-mode-addressed systems, according to Bruce Threewitt, manager of product planning. "In that situation, the Am2971 would replace two delay lines and some combinatorial logic. When given the signal from a microprocessor to start, the 2971 bursts out a canned waveform until the processor says stop." In contrast, a delay line only advances one clock edge.

Threewitt says that although the part was originally designed for DRAM timing applications, AMD is finding that it has a number of other applications. These include bus timing, peripheral control, and timing control for bit-mapped graphics.

An on-board 70-to-100-MHz phase-locked-loop crystal oscillator can clock the event generator to an output 1/5 or 1/10 the PLL frequency. Clocking can also come from an existing system.

Programming the Am2971 is done in the same way as a PROM. The chip's fuse links are made using AMD's platinum-silicide fuse technology. The 2971 is available now in 24-pin ceramic DIPs for $17.75 each in lots of 100 pieces. The handful of components it replaces averages between $25 and $30.

In addition to cost savings and increased system reliability through the reduced parts count, there are a couple of second-order benefits, Threewitt says. For one, the part improves system performance. "If you use external logic and delay lines, you are still stuck with skew problems between the individual circuits," he says. "Also, because the Am2971 is purchased blank, parts inventory is reduced since it replaces all of your timing components." *–Steve Zollo*

Advanced Micro Devices Inc., 901 Thompson Pl., P. O. Box 3453, Sunnyvale, Calif. 94088. Phone (408) 732-2400 [Circle 360]

FASTEST MULTIPLYING DAC ACCEPTS TWO INPUTS

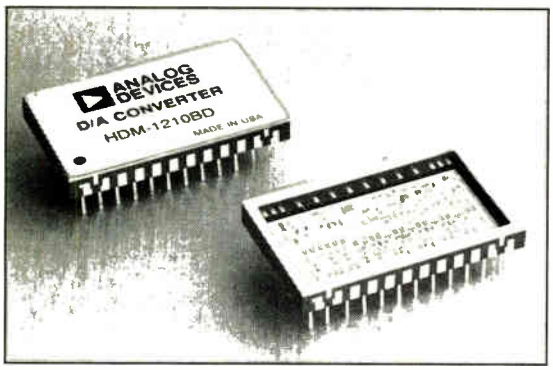
With the introduction of the HDM-1210, Analog Devices Inc. boasts the industry's fastest 12-bit multiplying digital-to-analog converter. Typical analog settling time to within 1% is only 85 ns. Up to now, comparable DACs have been in the 500-ns range. The current-output hybrid DAC has a maximum digital settling time of 110 ns, a maximum analog settling time of 120 ns, and a 10-MHz analog bandwidth.

Because of its small size—just 1.2 by 0.7 by 0.1 in.—the 1210 is an ideal replacement for the converter modules currently used in satellites. The modular converters, commonly called hockey pucks, measure about 2 by 2 by 1 in.

Unlike its fixed-reference counterparts, a multiplying DAC operates with varying (or ac) reference signals. Such DACs put out a signal proportional to the product of the reference (the analog input) voltage and the fractional equivalent of the digital input number.

The 1210 is designed for waveform generation and other applications in which one or two analog inputs must be multiplied by scale factors established with digital input words. The analog input signal can be a sine, triangle, or sawtooth wave. The output is a scaled version of the input, with digital input used as the scale factor.

In a second operational mode, the ana-



VOLTAGE TOO. Analog Devices' 85-ns multiplying DAC has a current output but can be set to put out a voltage.

log input voltage serves as the scale factor for the digital input code. The analog input, digital input, analog output, and external amplifier can be combined by using the hybrid's offsetting capabilities. These features let the 1210 work with unipolar or bipolar inputs.

By itself, the DAC can perform one-quadrant multiplications. In tandem with a second HDM-1210 in a circuit using standard binary coding, two-quadrant multiplication is possible. Users can adjust analog output ranges by changing feedback resistors in the output driver.

Analog Devices' Computer Labs Division in Greensboro, N. C., developed the converter using a thin-film substrate and laser-trimmed resistors. The biggest obstacle in designing the part, says design engineer Larry Barnes, was developing the operational amplifier. "We needed wide bandwidth and fast settling time," says Barnes. He designed the op amp using discrete transistors.

The HDM 1210 comes in 24-pin ceramic or metal DIPs to provide a choice of temperature ranges. The BD grade is said to operate from −25°C to +85°C. Analog says its SD/SDB-grade 1210 will operate from −55°C to +100°C. It is housed in a hermetically sealed ceramic package at a military-standard facility.

The unit puts out 10.24 mA. Designers requiring voltage outputs can connect the signal-out pin to the load-resistor pin. This would yield 1.024 V out, with no degradation in settling time. Running the HDM-1210 output into an amplifier would also yield voltage. Single-quadrant multiplication can range up to −5 V. The HDM 1210 has a guaranteed monotonicity over temperature and maximum gain ±0.5% of full scale. Guaranteed differential and integral linearity over temperature is ±1 least-significant bit at a maximum.

In addition to waveform generation, applications include CRT display, vector generation, and megahertz-rate analog and digital attenuation. The converter is available for immediate delivery at $188 each. *–Craig D. Rose*

Analog Devices Inc., 2 Technology Way, Norwood, Mass. 02062.
Phone (617) 329-4700 [Circle 361]

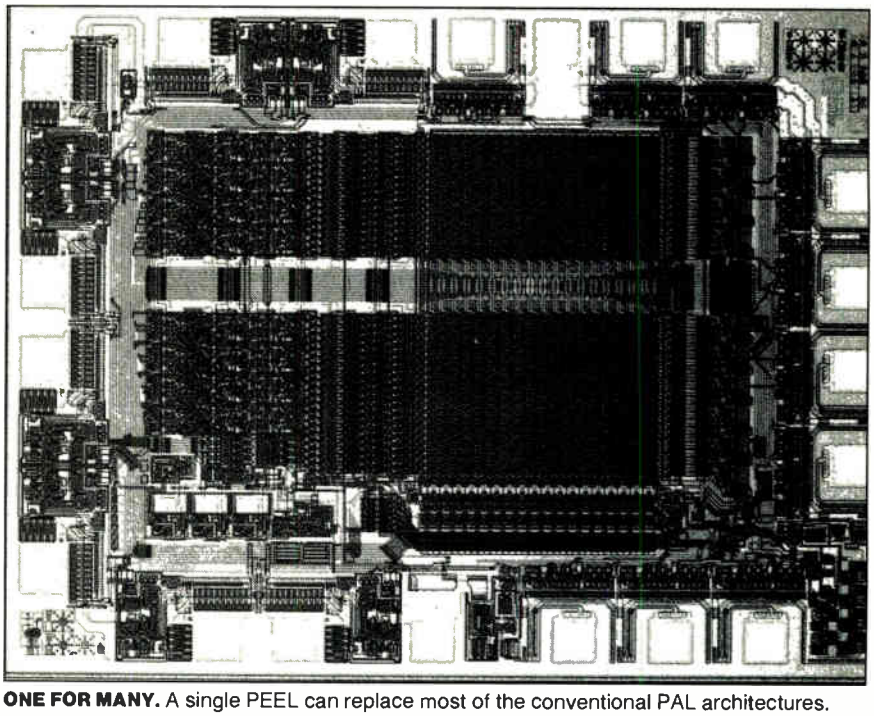
GOULD, ICT TO SELL EEPROM-BASED LOGIC

Two more semiconductor companies have begun offering programmable logic devices based on EEPROM technology instead of fuse arrays. Fledgling IC house International CMOS Technology Inc., San Jose, Calif., has announced a family of products it calls PEELs, for programmable electrically erasable logic. The PEELs will also be available from Gould Inc.'s Semiconductor Division, where they are being fabricated in 2-μm CMOS.

First on the scene was Lattice Semiconductor Corp., Portland, Ore., with its generic-array-logic chips [*Electronics Week*, June 3, 1985, p. 56]. VLSI Technology Inc., also of San Jose, recently added GALs to its portfolio as a second source.

PEELs and GALs both seek to replace PLDs based on fuse arrays, the lion's share of which are the programmable-array-logic parts sold by Monolithic Memories Inc. Unlike PALs, EEPROM-based PEEL or GAL chips can be reprogrammed quickly and repeatedly during the design-and-debug process; they are also useful in low-power designs where bipolar PALs are impractical. PEELs are said to consume only one third the power of their bipolar competition, even at the maximum clock rate.

EEPROM-based PLDs can also be 100% tested at the factory, whereas fuse-based PLDs can only be fully tested after the designer has blown a pattern of fuses on the chip. This eliminates a hidden cost that can crop up with fuse-programmed parts—they may not work properly after programming. "I've heard horror stories where there were 25% programming rejects" with fuse-array parts, says Drew Osterman, president and cofounder of ICT.



ONE FOR MANY. A single PEEL can replace most of the conventional PAL architectures.

Furthermore, one PEEL can emulate some 20 different PALs, thanks to the use of I/O cells that can be configured for bidirectional I/O, registered or combinatorial feedback, and active-high or active-low outputs that are either combinatorial or registered types. This drastically reduces the number of part types that must be kept in inventory. PEEL chips can also implement over 100 logic configurations not possible with earlier-generation PLDs, says ICT.

PEELs and GALs are in many ways similar; current versions of each, for example, are specified as having 25-ns maximum propagation delays. But ICT says it has achieved a PEEL die size

some 50% smaller than Lattice's equivalent GALs, and that it has been able to streamline the production process, reducing the number of masks required for fabrication by about 30%.

The first PEEL to hit the market will be the 18CV8, which has 18 inputs and 8 outputs and can replace 20-pin PALs. Samples will be available in July, and parts in plastic DIPs will cost less than $5 each in lots of 100. Following later this year will be the 22CV10, which fills in for 24-pin PALs, and two PEELs that replace 20- and 24-pin field-programmable logic arrays from Signetics Corp.

Third-party vendors of development tools and PLD programmers will support PEELs, says ICT. In addition, ICT and Gould will offer an evaluation system for about $800 that includes a programmer board for IBM Corp. Personal Computers and compatibles, an external programming module, and software. The software allows designers to develop their own logic patterns, or to translate conventional PLD design files into the PEEL format. *–Jeremy Young*

International CMOS Technology Inc., 2031 Concourse Dr., San Jose, Calif. 95131. Phone (408) 434-0678 [Circle 363]
Gould Inc., Semiconductor Division, 3800 Homestead Rd., Santa Clara, Calif. 95051. Phone (408) 246-0330 [Circle 364]

DENSEST FIFO YET HAS PARITY BIT FOR NETWORKS

Dallas Semiconductor Corp. is jumping into the first-in first-out chip business with the highest-density FIFO on the market. Built in CMOS, the DS2001 has 2-K by 9 bits of FIFO storage and a 120-ns cycle time. Like standard FIFOs, the 28-pin 2001 has two ports and can accept data while emitting bits at a different speed, making the chip suitable as a buffer between asynchronous communications devices.

The Dallas-based company designed the 2001 with transmission and networking applications in mind. The FIFO's 2-K-by-9-bit organization allows an extra error-checking and -correcting parity bit to be added to conventional 8-bit byte-wide systems. Previously, the highest-density FIFOs available were 1-K-by-9-bit parts.

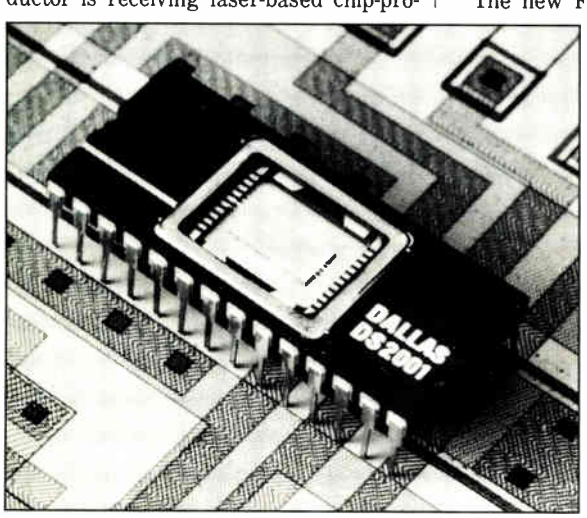
MOSTEK SUPPORT. Thomson Components Mostek Corp., Carrollton, Texas, will second-source the 28-pin FIFO. In return for the support, Dallas Semiconductor is receiving laser-based chip-production equipment. "Swapping a chip design for production equipment is a bit unusual," admits marketing vice president Michael Bolan, who left a position at Mostek in 1984 to help found Dallas Semiconductor.

"System engineers are faced today with the challenge of connecting different types of systems together. FIFOs are a response to that, supplying memory that can be viewed as a connector device or adapter," notes Bolan, referring to the demand by system designers for higher-density FIFOs. The higher densities yield greater tolerance for different input and output data rates in FIFOs, he adds. Dallas Semiconductor is now designing a 4-K-by-9-bit FIFO that will be plug-compatible with the 2001.

The 2-K-by-9-bit FIFO will sell for $42.80 each in 100-piece quantities when it enters volume production in September. Dallas Semiconductor will make samples available this month.

The new FIFO is made from a 2-μm CMOS process that produces a twin-tub, single-metal-layer, double-polysilicon structure. The die measures 44,800 mils^2. It has a 400-mW active power dissipation and 2.5-mW in standby mode.

The chip works in the commercial range of 0°C to 70°C, but the company intends to make industrial-grade chips for operation at -140°C to +85°C. *–J. Robert Lineback*



PARITY BIT. Dallas Semiconductor's dense FIFO is organized as 2-K by 9 bits for parity checking.

Dallas Semiconductor Corp., 4350 Beltwood Parkway, Dallas, Texas 75234. Phone (214) 450-0431 [Circle 362]

DATA-PATH IC HAS THREE PORTS

A 32-bit data-path chip from Weitek Corp., the WTL 3332 offers three ports for I/O-intensive signal-processing applications that also involve the processing of large quantities of data. Such applications include image processing, sonar, radar, motion control, and high-end telecommunications systems.

The chip's architecture prevents I/O bottlenecks and allows most algorithms to run at maximum speed, the manufacturer says. It is fabricated in CMOS technology and comes housed in a 168-pin grid array. The device dissipates less than 1 W.

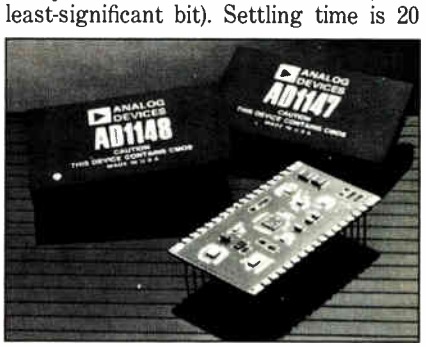
For less computation- and I/O-intensive purposes, Weitek provides the model WTL 3132, a one-port version. Samples of both will be out this month. In quantities of 100, the WTL 3332 costs $425; the WTL 3132, $350.

Weitek Corp., 1060 E. Arques Ave., Sunnyvale, Calif. 94086.
Phone (408) 738-8400 [Circle 365]

16-BIT DAC IS SELF-CORRECTING

The AD1147 16-bit digital-to-analog converter eliminates manual trimming of initial offset and gain errors by performing internal digital correction—an industry first, the company says. Two 8-bit latched-input DACs perform this correction through microprocessor control.

Both differential and integral nonlinearity are ±0.00076% maximum (±½ least-significant bit). Settling time is 20



μs. Data may be loaded into the AD1147's input latches from 8- and 16-bit buses. The analog output range can be set for either voltage or current.

The AD1147, housed in a 32-pin triple-width DIP, costs $152 each in hundreds. A less accurate—15 bits linear—model, the AD1148, features a separate data bus for the correction DACs; this is convenient in automatic-test-equipment applications with different cycles for correction and test functions. The price of the AD1148 in hundreds is $138, and both versions are available from stock.

Analog Devices Inc., Literature Center, 70 Shawmut Rd., Canton, Mass. 02021 [Circle 368]

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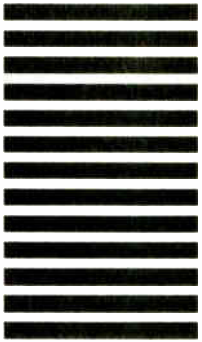

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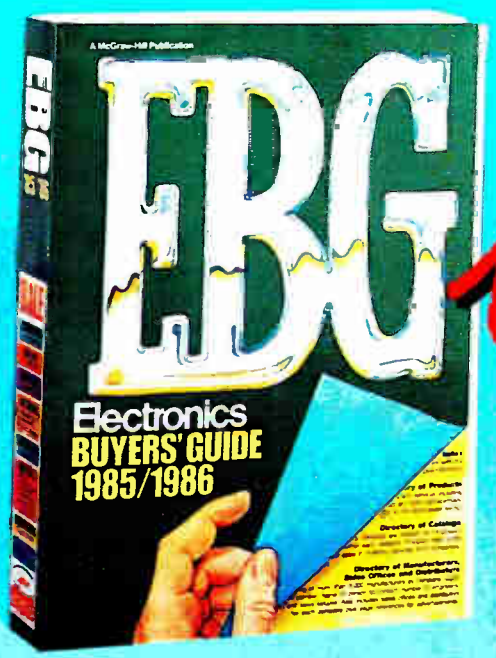

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FILTER CHIP ATTENUATES JITTER IN T1 LINES

CRYSTAL SEMICONDUCTORS' BUILDING BLOCK USES DIGITALLY ENHANCED ANALOG TECHNOLOGY

A single-chip filter from Crystal Semiconductor Corp. automatically attenuates jitter and provides steady clock and data signals for 1.544-Mb/s T1 phone lines. The CSC61600 eliminates jitter with an internal phase-locked loop and an elastic 16-by-1-bit first-in first-out shift register that can get data in at one speed and out at another.

The CMOS filter is the latest addition to the series of digitally controlled analog telecommunications and signal-processing chips that the company is introducing this year. Crystal calls its digitally enhanced analog technology Smart Analog [*Electronics*, Jan. 20, 1986, p. 21]. The new chip, intended to be a building block for T1 applications, is a subset of Crystal's recently introduced CSC61544 monolithic T1 interface.

Earlier last month, Crystal began making available its T1 line interface circuit, which has not only the jitter attenuator on chip but other blocks needed to attach to the phone network. The chip has a digitally programmable pulse-shaping line driver that transmits signals meeting T1 standards. The 28-pin 61544 sells for $23 each in 1,000-piece quantities. In orders of 1,000, the 61600 will sell for $4 each.

Intelligence inside the 61600 attenuator comes in the form of a digital logic block, which detects T1 line jitter and automatically adjusts the frequency of the filter's voltage-controlled oscillator. The chip uses switched capacitors to increase or decrease the capacitance load from the system's crystal, slightly varying the speed of the outgoing clock signal and smoothing out jitter.

ELASTIC. The 16-bit FIFO shift register, which acts as an elastic storage band, also helps smooth the clock frequency on T1 lines. The FIFO has two pointers that keep track of how many bits are held in the shift register. The number of bits in the elastic FIFO depends upon the frequency on the line. The 61600 accepts 1.544-Mb/s data and clock signals as input and removes up to 14 unit intervals of jitter, peak to peak, before putting out the data and clock.

"If bits are coming into the 16-by-1-bit FIFO faster than they are going out, the logic will slightly adjust the outgoing clock," explains Robert F. Bridge, Crystal's telecommunications product marketing manager. "If the FIFO empties out, that means bits are spilling out faster than they are coming in, and the chip very slightly slows the output clock signal." The result is a filter chip that will eliminate jitter with frequencies of 15 Hz.

The chip can be used in systems to clean up T1 transmission lines at the subscriber termination site as well as multiplexing applications, such as converting 1.544 to 45 MHz for T3 systems. In such multiplexers, the 61600 would help compensate for missing bits on the T1 side of the transmissions. The extra bits are part of the multiplexed T3 transmission scheme. When demultiplexed, missing bits can cause jitter at the receiving T1 termination.

The chip, the smallest yet from Crystal at 130 mils on a side, is fabricated from 3-μm p-well CMOS using double-polysilicon, single-metal technology. The chip dissipates 25 mW when active and operates from a single 5-V power supply. The initial versions operate in the commercial temperature range of 0°C to 70°C. Crystal also plans to offer chips that work from −140°C to +85°C. Samples of the 61600 are now available in plastic 14-pin DIPs, and the company plans to begin volume deliveries in early September.

Crystal will soon offer samples of a similar jitter attenuator for token-ring local-area networks, designated the CSC80600. Instead of a 16-bit FIFO, the part will have an 8-bit FIFO and will run at 8 MHz instead of the 1.544-MHz T1 rate. *–J. Robert Lineback*

Crystal Semiconductor Corp., P. O. Box 17847, Austin, Texas 78760.
Phone (512) 445-7222 [Circle 440]

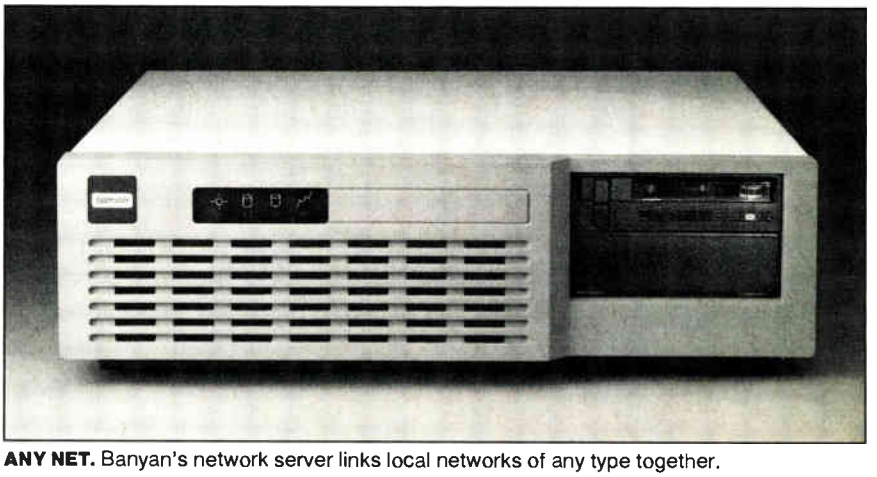
TWO SERVER OPTIONS LINK DIVERSE NETWORKS

Banyan Systems is expanding its line of high-performance wide-area networking products with a software-based network server that runs on the IBM Corp. PC AT and a desktop hardware server. The company targets its networking products at large corporations that demand the integration of numerous local-area networks of various types and want to link those networks to a mainframe computer.

As such, Banyan's networking products have features not typically found on low-priced LANs, including built-in microcomputer-to-mainframe links, server-to-server communications, and a node-naming and addressing scheme called Streetalk that allows users to locate and access any resource without having to know the network topology.

The Banyan/DTS is a high-performance, 32-bit, desktop network server, and the Vines/286 is a software package that converts a PC AT into a multifunction network server. Both products are based on the company's own Virtual Networking Software (Vines). Vines supports multiple LANs, so users can choose networks based on performance and application needs. In addition, Vines lets users migrate to new LAN technologies as they emerge.

Vines currently supports the IBM PC Network, Interlan Ethernet, the Standard Microsystems Corp. version of Datapoint Corp.'s Arcnet, Corvus Omninet, Proteon ProNET, 3Com Ethernet, Ungermann-Bass Net/One, and Allen-Brad-



ANY NET. Banyan's network server links local networks of any type together.

1	Exxon	25	Standard Oil (Ohio)	49	Consolidated Foods	73	American Home Prod.	97	North American Philips
2	General Motors	26	AT&T Technologies	50	Lockheed	74	Litton Industries	98	Agway
3	Mobil	27	Boeing	51	Georgia-Pacific	75	Hewlett-Packard	99	Pfizer
4	Ford Motor	28	Dow Chemical	52	Monsanto	76	Control Data	100	H.J. Heinz
5	IBM	29	Allied	53	W.R. Grace	77	Texas Instruments	101	NCR
6	Texaco	30	Eastman Kodak	54	Signal Companies	78	LTV	102	Pillsbury
7	E.I. du Pont	31	Unocal	55	Anheuser-Busch	79	American Brands	103	PPG Industries
8	Standard Oil (Ind.)	32	Goodyear	56	Nabisco Brands	80	International Paper	104	Int. Harvester
9	Standard Oil of Cal.	33	Dart & Kraft	57	Johnson & Johnson	81	Motorola	105	American Motors
10	General Electric	34	Westinghouse Elec.	58	Coastal	82	Burroughs	106	Borg-Warner
11	Gulf Oil	35	Philip Morris	59	Raytheon	83	Archer-Daniels-Midland	107	American Cyanamid
12	Atlantic Richfield	36	Beatrice Foods	60	Honeywell	84	Digital Equipment	108	Kerr McGee
13	Shell Oil	37	Union Carbide	61	Charter	85	Borden	109	United Brands
14	Occidental Petroleum	38	Xerox	62	General Mills	86	Champion International	110	FMC
15	U.S. Steel	39	Amerada Hess	63	TRW	87	Armco	111	Emerson Electric
16	Phillips Petroleum	40	Union Pacific	64	Caterpillar Tractor	88	Esmark	112	Dresser Industries
17	Sun	41	General Foods	65	Aluminum Co. of Amer.	89	Diamond Shamrock	113	Boise Cascade
18	United Technologies	42	McDonnell Douglas	66	Sperry	90	CPC International	114	Warner Comm.
19	Tenneco	43	Rockwell Int.	67	Gulf & Western Ind.	91	Time Inc.	115	Owens-Illinois
20	ITT	44	PepsiCo	68	Continental Group	92	Deere	116	Carnation
21	Chrysler	45	Ashland Oil	69	Bethlehem Steel	93	Bristol-Myers	117	American Can
22	Procter & Gamble	46	General Dynamics	70	Weyerhaeuser	94	Martin Marietta	118	Reynolds Metals
23	R.J. Reynolds Ind.	47	3M	71	Ralston Purina	95	Firestone Tire & Rubber	119	Campbell Soup
24	Getty Oil	48	Coca-Cola	72	Colgate-Palmolive	96	IC Industries	120	Kimberly-Clark

ley VistaLAN. Banyan is demonstrating its IBM Token-Ring network support at this week's PC Expo in New York.

For connection to IBM mainframes using a Systems Network Architecture/Synchronous Data Link Control protocols, Vines allows PCs to emulate IBM 3270 terminals with the network server emulating a remote IBM 3274 or 3276 cluster controller. Vines also offers DEC VT-100 and VT-52 and TTY asynchronous terminal emulation.

THREE PARTS. A principal feature of the servers is Streetalk, Banyan's global data base used for identifying, locating, and controlling access to users, services, and resources such as printers, plotters, and modems. Each data-base item has a descriptive three-part name. When a name is referenced, hierarchical directories are automatically searched. Because an item is independent of its location, it can be relocated without having to be renamed. Users, devices, or file volumes can be moved around the network without notifying users.

The Banyan/DTS uses a 32-bit 68000-based CPU offering 10-MHz, no-wait-state operation. It has three buses—a Small Computer System Interface bus, a proprietary bus to handle memory management, and a third compatible with the IBM PC expansion bus. The server comes with one 43-, 72-, or 118-megabyte hard-disk drive, upgradable to two. A 60-megabyte ¼-in. tape drive is standard. A single Banyan/DTS can provide internetwork communications between any two of the different types of LANs that Vines supports. The $9,995 server supports up to 30 users.

Vines/286 turns standard PC ATs into network servers and is suitable for networking remote field locations because it includes the micro-to-mainframe link capability. Vines/286 requires a minimum of 512-K bytes of memory.

A PC AT has six expansion slots for network interface cards, memory cards, or serial-communications cards. A Banyan server—including a Vines/286-based server—connects to a LAN simply by installing a LAN interface board into one of the slots. The PC AT becomes a dedicated server and cannot be used for application programs. Priced at $1,895, Vines/286 includes support for one type of LAN, the Streetalk global data base, file sharing, peripheral sharing, diagnostics, and documentation. Both products will be available in October.

Tallgrass Technologies Corp., of Overland Park, Kan., is also introducing the hardware server and software-only version under its label through its dealer and distribution channels. *–Steve Zollo*

Banyan Systems Inc., 135 Flanders Rd., Westboro, Mass. 01581.
Phone (617) 898-2404 [Circle 441]

UNIT RUNS ETHERNETS ON MAP NETWORKS

The Ethermodem Remodulator allows users to operate broadband Ethernets on the same broadband cable as Manufacturing Automation Protocol factory networks. The manufacturer targets the remodulator at broadband network users who also want to add Ethernet connections and for those who want to extend the distance between Ethernet nodes over broadband cabling. The remodulator, which lets Ethernets coexist with all three MAP frequency channels, eliminates the need for guard bands between communication services.

The Ethernet Remodulator lets users select either of two channels for their Ethernets while reserving the three MAP-specified channels. The unit is transparent to high-level network software so networks can run DECnet, XNS, Transmission Control Protocol/Internet Protocol, and Technical and Office Protocol software on broadband nets without modification.

The remodulator costs $5,900 and will be available in September.

Chipcom Corp., 195 Bear Hill Rd., Waltham, Mass. 02154.
Phone (617) 890-6844 [Circle 445]

CONTROLLER CREATES BROADBAND MODEM

Motorola's MC68184 broadband interface controller, when coupled with radio-frequency circuitry, makes up the broadband modem that is needed in each node of a Manufacturing Automation Protocol communications network. It supports 10-megabyte/s data rates.

The broadband interface controller works with the model MC68824 token bus controller over an IEEE 802.4 serial interface to implement high-speed broadband networking for layers one and two of the Open Systems Interconnection communication model. Both are very large-scale-integration devices; the controller is a macrocell array that reduces power requirements and costs for a broadband modem.

Sample quantities of the 40-lead MC68184 in a plastic DIP will be available in September. In quantities of 100, the price will be $40.

Motorola Inc., Microprocessor Products Group, 3501 Ed Bluestein Blvd., Austin, Texas 78721 [Circle 443]

CHIP BUILDS T1 REPEATER

A pulse-code-modulated repeater IC, the MP5262, contains all the active functions required to build one side of a T1 or 2-Mb/s PCM repeater. For stable operation and low temperature drift, the chip uses an advanced thin-film-resistor technology of silicon chrome and bipolar processing.

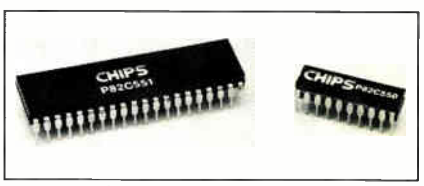
The MP5262 operates with a single 6.8-V power supply and with a typical low-current drain of 13 mA. The bipolar output drivers are designed to go automatically to their off-state when there is no input signal present.

In a 16-pin Cerdip, the 100-piece price of the MP5262 is $6. If the customer wishes it in die form, the company will quote prices. Production quantities take four weeks to deliver, and samples are available immediately.

Micro Power Systems Inc., 3100 Alfred St., Santa Clara, Calif. 95054.
Phone (408) 727-5350 [Circle 444]

HUB CONTROLLER SUPPORTS 8 NODES

The 82C551 Starlan hub controller supports up to eight nodes downstream and one upstream. Up to five controllers can be cascaded to support a maximum of 40 nodes. The IC receives data, retimes it, and transmits it to the other nodes as well as to the next-level hub; the controller performs the reverse function.



The 82C551 features collision detection. Its built-in jabber function detects transmissions over 65 ms, then ignores that line until the transmission ceases, which helps to isolate faulty nodes from the rest of the network. It has a diagnostic loop-back for fault detection and isolation.

The CMOS chip comes in a 40-pin plastic DIP for $56.70 in quantities of 100. Samples are available now.

Chips & Technologies Inc., 521 Cottonwood Dr., Milpitas, Calif. 95035.
Phone (408) 434-0600 [Circle 442]

T1 PROCESSOR LINKS WITH AT&T'S ACCUNET

The AccuPac-1.5, a T1-format processor, creates a direct-access path between high-speed data-terminal equipment and AT&T's Accunet. Typical applications include video teleconferencing, high-speed host-to-host transmission, and terrestrial extension of satellite or microwave circuits. Accupac-1.5 sells for $3,995 in single-port configuration. An internal-line-driver option allows it to be used as a dual-port, high-speed local data-distribution unit. Delivery is in 30 to 60 days.

Avanti Communications Corp., Aquidneck Industrial Park, Newport, R. I. 02840.
Phone (401) 849-4660 [Circle 446]

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STANDARD CONTROLLERS CUT AUTOMATION COSTS

WITH THE BASE CELL LINE, USERS CAN SET UP AUTOMATED FACTORIES WITHOUT ALLEN-BRADLEY SUPPORT PERSONNEL

Allen-Bradley is lowering the price of building automated factories with its line of standard work-cell controllers. The Base Cell line is a low-end version of the company's 16-month-old Vista 2000 cell-control computer, which until now has been used to set up more costly custom implementations.

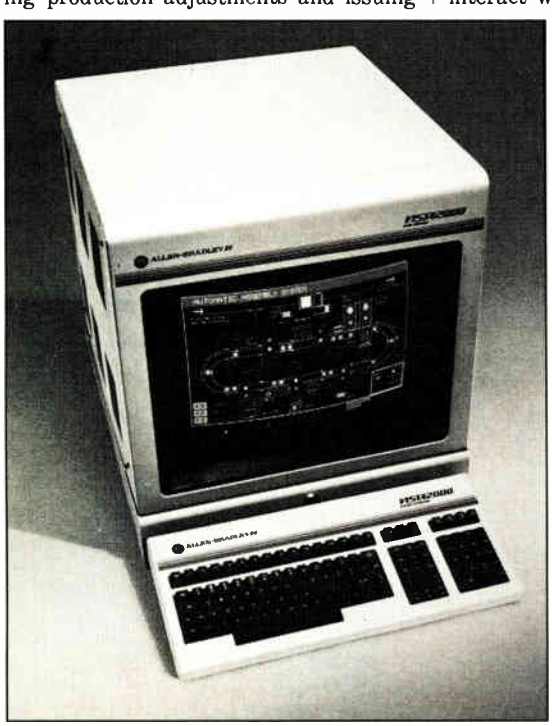
The Base Cell Program features standard hardware and software packages that the customer can configure himself, eliminating the manpower costs associated with customized solutions. Allen-Bradley is also introducing higher-capacity RAM boards and disk drives that further improve the price-performance ratio of the Vista 2000, an industry-hardened version of the 32-bit Masscomp model 500 computer from Massachusetts Computer Corp., Westford, Mass. The machine relies on multiple 68000-family microprocessors.

In the Allen-Bradley scheme, the Vista 2000 oversees a number of programmable controllers, computerized numerical controllers, and industrial personal computers that interface with sensors and machinery in factory work cells. The cell controller coordinates the activities of its lower-level counterparts, making production adjustments and issuing reports, while providing the link between the factory floor and computers at higher levels in the hierarchy.

The combination of reduced Allen-Bradley support requirements and the use of denser RAM and hard-disk technology makes the Base Cell line about 25% cheaper than comparable custom Vista 2000 implementations, says Ralph Waite, vice president and general manager for the company's Industrial Computer Group in Highland Heights, Ohio. Until now, cell-level control has been a custom proposition, he says.

So far, the company has sold about 75 Vista 2000s, but all factory installations required the presence of Allen-Bradley personnel to aid in customizing systems, Waite says. The Base Cell Program represents the experience Allen-Bradley gained in those installations.

MENU DRIVEN. The company developed standard hardware and software packages that can be configured by the customer for basic cell-control tasks without the aid of Allen-Bradley personnel, Waite explains. The Base Cell software features a menu-driven format and graphic aids that walk the user through the setup task. "All the user has to do is interact with the system," Waite says.



EASILY ADAPTED. Allen-Bradley's cell controller is at the heart of its customer-configurable Base Cell concept.

Initial Base Cell products come in two configurations. Vista Base Cell 1 includes a Vista 2000 computer based on AT&T's Unix operating system, software, power supply, hard-disk memory, and a 19-in. color control monitor with 832-by-600-pixel resolution. The package sells for less than $50,500, including a 4-megabyte RAM board and a 71-megabyte hard-disk system. That compares with 1-megabyte RAM boards and a 42-megabyte hard disk in previous Vista 2000 systems, Waite says.

Vista Base Cell 2 adds an Access Machine, a 32-bit computer designed to extend the system's capability. The Access Machine starts at less than $20,000 and acts as a data-base manager while enabling the system to operate on two Data Highways. (The Data Highway is Allen-Bradley's factory local-area network.) The Base Cell 1 can handle one Data Highway and provides monitor and control capability for up to 1,250 functions. With Base Cell 2, the number of functions extends to 5,000.

Though the Base Cell line enables users to configure basic cell-control jobs, more sophisticated applications will still require Allen-Bradley support personnel at the customer site. But as Allen-Bradley gains experience, it plans to likewise convert the more advanced capabilities into standard products in the Base Cell line, Waite says.

Future Base Cell products will interface with both broad- and carrier-band networks based on the Manufacturing Automation Protocol. They will also link to robots and computer-aided design systems from various vendors, allowing users to create true computer-integrated manufacturing systems, Allen-Bradley says. *–Wesley R. Iversen*

Allen-Bradley Co., 747 Alpha Dr., Highland Heights, Ohio 44143.
Phone (216) 449-6700 [Circle 460]

MOTION CONTROLLER IS EASY TO ASSEMBLE

A modular motion-control system that comes with keyed interconnection hardware and a detailed connection diagram enables a designer with no previous experience in this area to quickly assemble a working unit. The BBS/Series components include the motion controller, motor, feedback sensor, and amplifier.

Motors come in torque ranges from 5 to 500 oz-in., with encoder resolutions up to 1,000 pulses per revolution. The user can select controllers for the IBM Corp. Personal Computer and standard bus systems; pulse-input format is also available for applications requiring a direct interface to an indexer or pulse generator. Typical position accuracy at "stop with no load" is 0.18°.

The amplifier puts out up to 10 A at 70 V; higher current and voltage limits are optional. Features such as coordinated motion, nonvolatile memory, uncommitted I/O channels, and sequencing are also available. Systems start at $995, with delivery in three weeks.

Galil Motion Control Inc., 1928-A Old Middlefield Way, Mountain View, Calif. 94043.
Phone (415) 964-6494 [Circle 462]

SOFTWARE ENHANCES IMAGE PROCESSING

An image-processing operating environment called PC Semper contains over 100 image-processing and -analysis functions. The package runs on IBM Corp. Personal Computers and compatibles. The software uses IEEE standard 32-bit floating-point arithmetic for most appli-

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Their processing proficiency is equalled only by their graphics. A monochrome DN3000 exhibits 1280 x 1024 resolution on a 19-inch monitor. While a color version, with its four-bit planes, displays 16 colors simultaneously on a high-resolution, 15-inch flicker-free screen.

While such qualities alone are cause enough for celebration, the DN3000s were notably designed with an understanding that technical professionals work as much with each other as they do with their workstations.

Hence, like all Apollo workstations, DN3000s inherently let you transparently share information and resources across a high-speed local area network.

An IBM PC/AT®- compatible bus assures the ability to integrate options into the system.

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The DOMAIN Series 3000. In monochrome from under $10,000. In color from under $15,000. Proof that it doesn't take a lot of money to attain a position of power.

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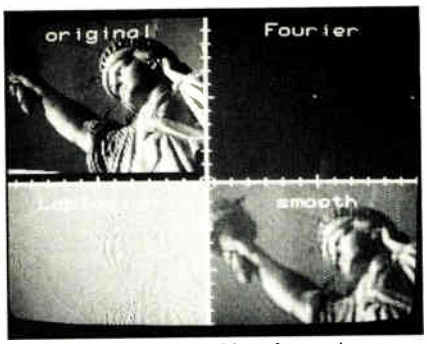


cations to achieve wider dynamic range than fixed-point math.

With facilities for writing programs, archiving images in a data base, and developing new processing algorithms for use with the system, the company says, PC Semper is not only expandable but also simple to program. The package consists of three major components, one of them a high-level interpretive command language that utilizes simple English-language commands. Also included are a file-management system and a system-expansion facility that allows Fortran programmers to write custom algorithms with the IBM professional Fortran Compiler as additional subroutines for the system.

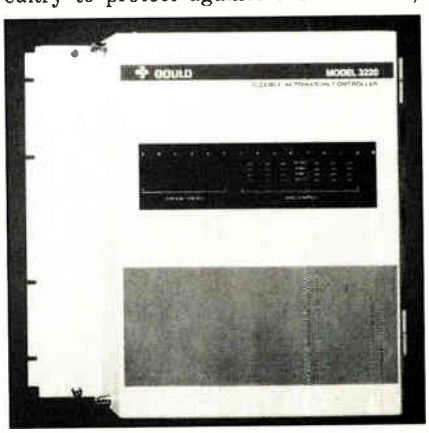
The program comes in two configurations. Set up to support image resolutions of 512 by 512 by 8 pixels, the system costs $1,995. A lower-resolution model (256 by 256 by 6) lists for $1,495. Both are available immediately.

Data Translation, Inc., 100 Locke Dr., Marlboro, Mass. 01752.
Phone (617) 481-3700 [Circle 463]

AMPS DRIVE BRUSHLESS MOTORS

A line of five pulse-width-modulated current-amplifier/motor drives amplifies three-phase torque command signals from Gould's Flexible Automation Controller to drive its brushless motors. The Cyberline 1000 drives use a proprietary direct-numerical-processing technology, and they produce outputs of 1 to 20 kW.

The drives all feature diagnostic circuitry to protect against short circuits,



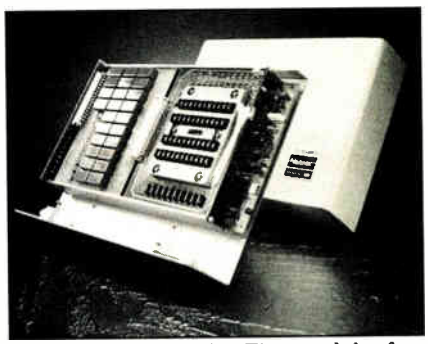
over- and undervoltage, and overheating. They support a maximum bus voltage of 325 V dc and are said to have 30% fewer components than drives in conventional brushless motor-control systems. There are no potentiometers, for example, since the drives amplify torque and command signals rather than generate them, the company says.

Prices range from $1,000 to $4,000. Delivery takes two weeks.

Gould Inc., Industrial Automation Systems, 105 Delta Dr., Pittsburgh, Pa. 15238.
Phone (412) 963-1444 [Circle 464]

DATA COLLECTOR SCANS 100 CHANNELS/S

Increased speed and performance over its predecessor are the calling cards of the Netpac 2 remote front-end module for industrial data measurement and collection. When connected to a host computer or data logger with an RS-422 communication link, Netpac 2 can scan



over 100 channels/s. The module features complete on-board signal processing and can measure a variety of inputs with up to 0.03% accuracy without any preconditioning.

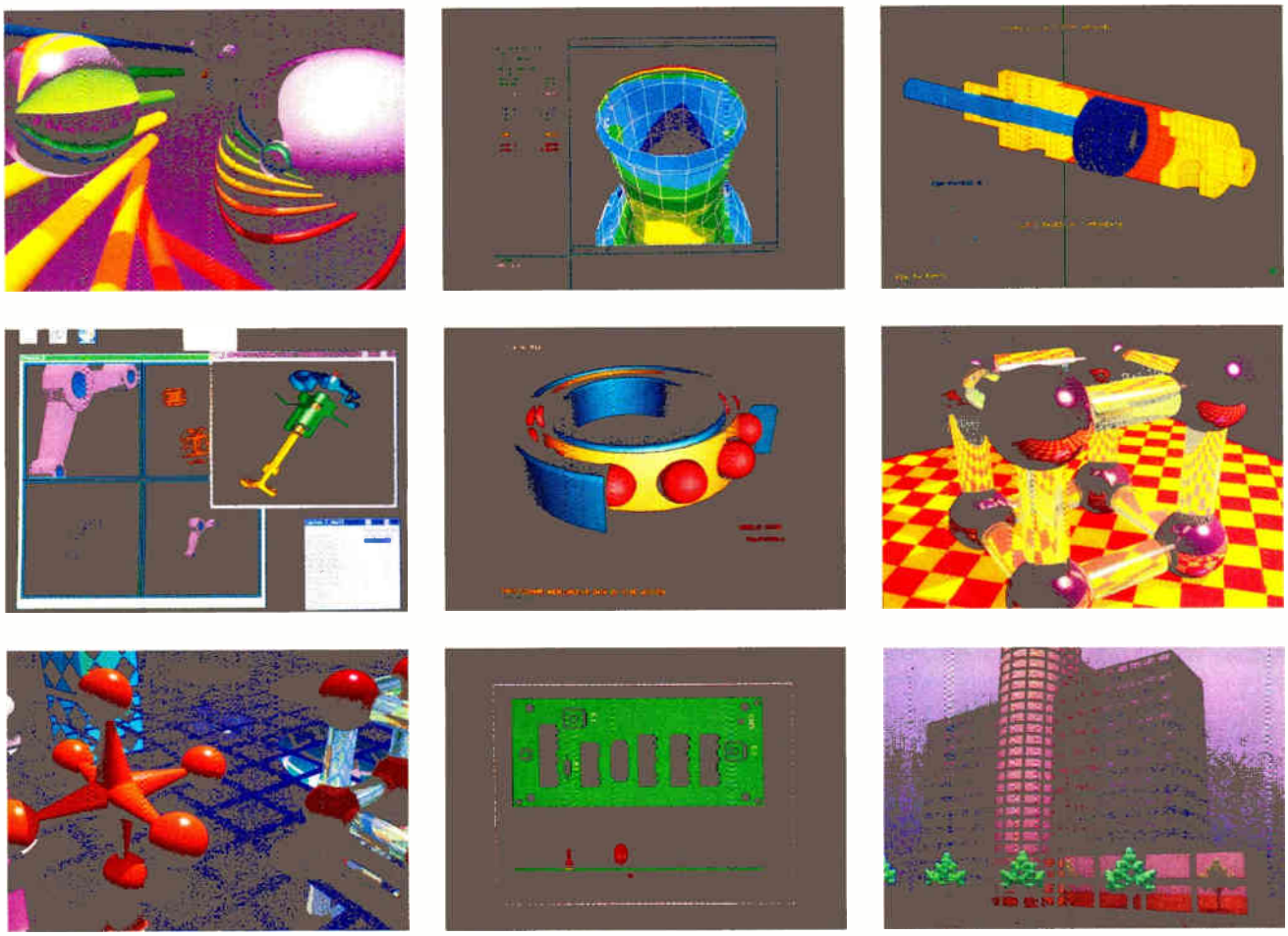
Standard I/O options consist of millivolt, milliampere, contact I/O, and pulse input lines. Users can connect 16 modules to a twisted-pair wire up to 5,000 ft long, and each supports up to 100 I/O lines. Transmission up to 19.2 kb/s is supported and software for host compatibility is available. Pricing and delivery for the Netpac 2 have not yet been set, but the product will be available in both NEMA 2 and NEMA 4 enclosures for use in harsh industrial environments.

Acurex Corp., Autodata Division, P. O. Box 7042, Mountain View, Calif. 94039.
Phone (415) 967-9100 [Circle 466]

IMAGE CARDS WORK IN VMEBUS SYSTEMS

A series of boards for image-processing applications are designed for VMEbus computers and compatible machines. The RTI-400 series includes an intelligent pipeline pixel processor, an analog subsystem for video I/O, and two memory boards. Used together, they form a complete vision-engine

OUR 3D GRAPHICS WORKSTATION IS SO FAST IT'S AMAZING THESE PICTURES AREN'T BLURRED.



Until now, if you wanted realtime 3D graphics on a powerful workstation, you had only two choices. Both of them a compromise.

You could purchase a specialized graphics workstation but sacrifice a compatible product family, software and application choice. Or you could opt for a reputable engineering workstation and settle for color graphics that could only be labeled dull.

Introducing Apollo's new DN580. It asks no sacrifice. Instead, this powerful 32-bit graphics workstation overwhelms anything that claims to be either graphic or a workstation.

Its powerful graphics pipeline processor performs 3D graphics at an amazing 100,000-plus vectors per second, a record well beyond the reach of any other computer or workstation supplier.

Yet despite such speed, the DN580 complies with PHIGS and supports UNIX,™ dispelling the myth that performance and standards are contradictory terms.

Of course the DN580 offers more than alacrity. As part of an advanced distributed processing network, its speed is greatly enhanced by an ability to access other Apollo workstations. As well as systems made by DEC® and IBM.®

And with Apollo's open architecture, you can perform all these stunts with a single system view.

The Apollo DN580. The only thing faster is the rate at which our competitors will have to work to catch up.

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subsystem, according to the company.

All four boards support conditional processing for pixel-by-pixel decision-making in real time as part of a computational pipeline, and all four also have synchronous video bus interfaces that allow high-speed intermodule data transfers without bogging down host bus performance. Software support is provided by RTILIB/400, a $1,500 real-time image-processing/machine-vision package with over 300 callable routines in C language included.

The RTI-400 boards are designed for applications including inspection of semiconductor wafers, machined parts, and pc boards; medical-imaging equipment; and digital microscopy for laboratory research. Delivery is within 30 days of order.

The PX401V, the 10-MHz, 16-bit pipelined pixel processor, costs $3,495 in single quantities. Pricing for the AS401V Analog Subsystem, which digitizes inputs with 512-by-512-by-8-bit resolution, is $2,995. The memory boards—the DS-401V, which stores a single 512-by-512-by-8-bit image, and the DS-441V, which stores four of those images—cost $2,495 and $3,495, respectively.

Recognition Technology Inc., 335 Fiske St., Holliston, Mass. 01746.
Phone (617) 429-7804 [Circle 465]

OPTICAL DETECTOR GAUGES UP TO 18 EDGES

The HVS 256 stand-alone intelligent optical inspection gauge is based on a linear detector array that measures the edge, position, or width of objects. For manufacturing, packaging, and quality control, the system detects and counts up to 18 edges and gauges width or the center of an object from any two edges. The company says that in some cases the sensor can take the place of more costly vision systems.

The HVS 256 contains a microprocessor that can be programmed for a variety of measurement or inspection tasks. It figures the edges, positions, and widths of objects and then puts out the measurements in analog or digital format. Prices for the sensor start at $2,500. It is available now.

Honeywell Visitronic, P. O. Box 5077, Englewood, Colo. 80155.
Phone (303) 850-5050 [Circle 467]

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ACM Conference on Lisp and Functional Programming, Association for Computing Machinery (Robert Halstead, Massachusetts Institute of Technology, 419 Technology Sq., Cambridge, Mass. 02139), MIT, Cambridge, Aug. 4-6.

National Conference on Artificial Intelligence, American Association for Artificial Intelligence (445 Burgess Dr., Menlo Park, Calif. 94025-3496), University of Pennsylvania, Civic Center, and Franklin Plaza Hotel, Philadelphia, Aug. 11-15.

30th International Technical Symposium on Optical and Optoelectronic Engineering, Society of Photo-Optical Instrumentation Engineers (P. O. Box 10, Bellingham, Wash. 98227-0010), Town and Country Hotel, San Diego, Aug. 17-22.

Siggraph '86, Association for Computing Machinery and IEEE (Siggraph Conference Management, 111 E. Wacker Dr., Chicago, Ill. 60601), Dallas Convention Center, Dallas, Aug. 18-22.

International Conference on Parallel Processing, IEEE Computer Society and Pennsylvania State University (IEEE Computer Society, 1730 Massachusetts Ave., N. W., Washington, D. C. 20036-1903), Pheasant Run Resort, St. Charles, Ill., Aug. 19-22.

ICSSDM: 1986 International Conference on Solid State Devices and Materials, the Japan Society of Applied Physics (1986 ICSSDM, c/o Japan Academic Societies Center, 4-16, Yayoi 2-chome, Bunky-ku, Tokyo 113, Japan), Tokyo Prince Hotel, Tokyo, Aug. 20-22.

3rd International Congress on Advances in Non-Impact Printing Technologies, Society of Photographic Scientists and Engineers (Samuel W. Ing, Xerox Corp., 800 Phillips Rd., Webster, N. Y. 14580), Fairmont Hotel, San Francisco, Aug. 24-28.

8th Quartz Devices Conference and Exhibition, EIA (2001 Eye St., N. W., Washington, D. C. 20006), Westin Crown Center, Kansas City, Kan., Aug. 26-28.

Interconnect '86, United States Telecommunications Suppliers Association (333 N. Michigan Ave., Suite 1618, Chicago, Ill. 60601), San Mateo Expo Center, San Mateo, Calif., Aug. 26-28.

IFIP Congress '86: International Federation for Information Processing (Philip H. Dorn, Dorn Computer Consultants Inc., 25 E. 86th St., New York, N. Y. 10028), Trinity College, Dublin, Sept. 1-5.

NCC-Telecommunications Conference, IEEE Computer Society *et al.* (Mike Sherman, 1899 Preston White Dr., Reston, Va. 22091), Civic Center, Philadelphia, Sept. 8-10.

International Test Conference, IEEE *et al.* (Peter Bottorff, International Test Conference, P. O. Box 264, Mt. Freedom, N. J.), Sheraton Washington Hotel, Washington, Sept. 8-11.

16th European Microwave Conference, Royal Irish Academy *et al.* (Microwave Exhibitions and Publishers Ltd., Convex House, 43 Dudley Rd., Tunbridge Wells, Kent TN1 1LE, England), National Concert Hall, Dublin, Ireland, Sept. 8-11.

Symposium on Optical Fiber Measurements, IEEE and Optical Society of America (D. L. Franzen, National Bureau of Standards, Division 724.02, 325 Broadway, Boulder, Colo., 80303), NBS Laboratories, Boulder, Sept. 9-10.

Swissdata '86, Swiss Industries Fair (Secretariat, Swissdata 86, Postfach, CH-4021, Basel, Switzerland), Fairgrounds, Basel, Sept. 9-13.

Symposium on Optical Communication Primary Standards, EIA (G. P. Watkins, Corning Glass Works MP-BH-03, Corning, N. Y. 14831), National Bureau of Standards Laboratories, Boulder, Colo., Sept. 11.

Midcon 86, IEEE *et al.* (Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045), Dallas Convention Center, Dallas, Sept. 9-11.

Mid-Atlantic Electronics Design and Production Conference, International Marketing Services Ltd. (1030 S. LaGrange Rd., LaGrange, Ill. 60525), Valley Forge Convention Center, King of Prussia, Pa., Sept. 11-12.

Intercomm '86: International Communications Exposition and Conference for Science and Technology, Cahners Exposition Group (P. O. Box 70007, Washington, D. C. 20088), Exposition Center, Beijing, China, Sept. 15-20.

IEEE International Symposium on Electromagnetic Compatibility, IEEE (George Ufen, GRU Associates, 1105 E. Commonwealth Ave., Fullerton, Calif. 92631), Town & Country Hotel, San Diego, Sept. 16-18.

Fall National Design Engineering Show & Conference, Cahners Exposition Group (999 Summer St., Stamford, Conn. 06905), Jacob Javits Convention Center, New York, Sept. 16-18.

International Broadcasting Convention, Electronica Engineering Association *et al.* (IBC Secretariat, Institution of Electrical Engineers, Savoy Place, London WC2R 0BL, England), Metropole Conference Centre, Brighton, England, Sept. 19-23.

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MOTOROLA SETS TRANSFER PLANS...

Paving the way for 45-year-old George Fisher to take over Motorola Inc. as president and chief executive officer on Jan. 1, 1988, is a series of moves intended to ensure a smooth transition. After 22 years at the company's helm, chairman Robert Galvin, 63, is relinquishing his second title of chief executive officer to vice chairman and chief operating officer William Weisz, 59. Weisz will hold the post until Fisher, who now becomes senior executive vice president and deputy to the chief executive, takes over in 1988. Previously, Fisher was a senior vice president in Motorola's Communications Sector. John Mitchell, 58, president and assistant chief operating officer, will take sole responsibility for operations until 1988, when he will join Weisz as vice chairman and surrender his operations role to Gary Tooker, 47. For now, Tooker will become senior executive vice president and chief corporate staff officer.

...WHILE RCA PAIR ARE NAMED GE VPs

General Electric Co. is making moves to consolidate in the wake of its merger with RCA Corp. by naming Richard Miller, 45, senior vice president for GE's Consumer Electronics Business, including RCA Consumer Electronics. Miller had been executive vice president for consumer products and entertainment at RCA. Carl Turner, 53, was named vice president of the Solid State Division of GE's Semiconductor Business. Turner continues as division vice president and general manager of RCA Solid State and assumes "some responsibility" at GE Semiconductor.

MATSUSHITA TO MAKE TVs IN MEXICO

Matsushita Electric Industrial Co. plans to decrease color TV exports to the U.S. from its Japanese plant by shifting production to a new facility in Mexico. The plant will produce 250,000 large-screen sets in the first year of operations and is scheduled to ramp up to 400,000 within two years. The company's annual U.S. sales now total 400,000 sets of all sizes.

NTT COULD ADOPT ISDN STANDARDS

A private advisory panel to Japan's Ministry of Posts and Telecommunications is urging the ministry to ask Nippon Telegraph and Telephone Corp. to adopt international standards for its integrated services digital network. NTT had been developing its own standards, but with the expected completion of recommended international standards this month, the panel urged NTT to conform. NTT is expected to agree to the request.

TWO TEAMS VIE FOR MIL CONTRACT

Two industry teams are competing for final development of the joint Air Force/Navy Integrated Electronic Warfare System. TRW and Westinghouse will square off against Sanders Associates and General Electric in a $93.6 million contract for the 31-month Phase 1B, the design and development of components and subsystems. Inews will integrate a number of electronic systems in combat aircraft. One team will be picked to develop the next-generation Inews in Phase 2, and in Phase 3 the teammates will split to compete for production rights.

CMI DROPS DISK DRIVES

Having lost its major customer—IBM Corp.—Computer Memories Inc. is dropping out of the disk-drive business. The Chatsworth, Calif., firm [*Electronics*, Aug. 19, 1985, p. 19] hasn't managed to promote sales of its 20-megabyte 5¼-in. drive to other customers; nor could it introduce higher-performance products. Despite a loss of $18 million on $116 million sales for the year ended March 31, CMI still has about $30 million in capital, officials say. Now two likely scenarios loom: either the company will seek an acquisition or be acquired itself.

ELECTRONICS SHARE OF U.S. GNP SLIPS

With $229 billion in sales, the U.S. electronics industry accounted for 5.7% of the U.S. gross national product in 1985—down from its 6.1% share in 1984, according to the American Electronics Association. The AEA attributes the decline to the slump the industry is suffering and calls the dip "a short-term break" in a long-term upward trend. Electronics is the nation's third largest industry, ranking behind only transportation equipment, at 7.8% of the GNP, and food and related items, at 7.4%.

ROLM REALIGNS MANUFACTURING...

Rolm Corp. is realigning its manufacturing operations. Focusing activities of the newly formed Telephone Products Division in Austin, Texas, and the CBX Division in Santa Clara, Calif., the company is keeping only final assembly and test at the Santa Clara headquarters. Board-level activity will be moved to sites in Colorado and Texas. Analysts say the changes, which put like activities in the same locations, give Rolm a chance to achieve higher efficiency in production.

...WHILE HP SPLITS SYSTEMS SECTOR

In an effort to give greater emphasis to its 3000 line of business computers and to its personal computer line, Hewlett-Packard Co. is splitting its Information Systems and Network Sector in two. The new Business Systems and Personal Computation Sector is headed by senior vice president Douglas C. Chance, 44, a 20-year HP veteran. Executive vice president John L. Doyle will run the new Systems Technology Sector and maintain responsibility for peripherals and computer manufacturing.

AT&T SCALES DOWN OFFICE PBX

Gunning for a bigger share in what it thinks is the fastest growing segment of the PBX market—small-to-medium-sized offices—AT&T Co. introduced the System 25, a scaled-down version of its System 75 digital switch that will replace its analog Horizon system. AT&T has not secured as large a share in this niche as in others, because of competition from ITT, Mitel, and Rolm. The company is positioning the 50-to-200-line switch between two successful systems—Merlin, which can handle up to 80 users, and the System 75, which supports up to 800 stations.

18 NATIONS BLESS EUREKA PROJECT

Research ministers from 18 European countries have approved 62 joint research and development projects worth more than $2 billion under the pan-European Eureka project. Eureka is a French-proposed alternative to the U.S. Strategic Defense Initiative. French companies are the most widely represented, participating in 40 of the projects, while British and West German firms will take part in 29 and 15 of the projects, respectively. With life spans of 2 to 10 years, most of the projects concentrate on software engineering, microelectronics, data processing, and telecommunications.

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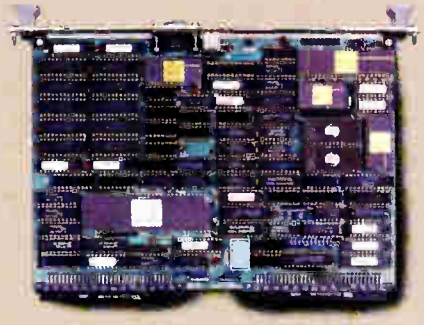

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