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Electronics

THE WORLDWIDE TECHNOLOGY WEEKLY

JUNE 23, 1986

STRETCHING THE LIMITS OF ASIC SOFTWARE

DESIGNERS NEED BETTER TOOLS TO BUILD GIANT ASICs

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65,000 PARALLEL PROCESSORS TACKLE BIG DATA JOBS/45

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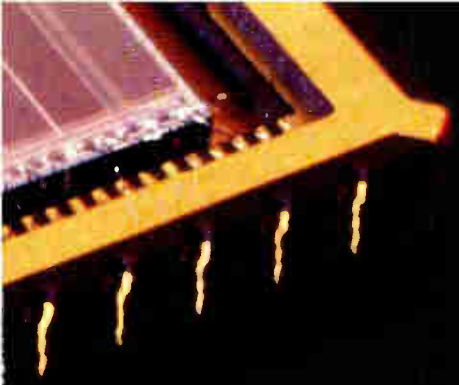

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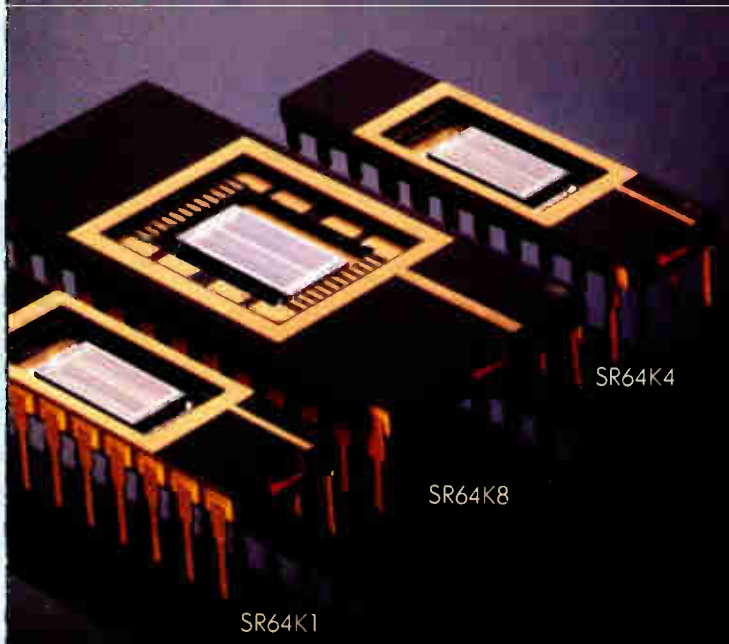

First Again.

Now...

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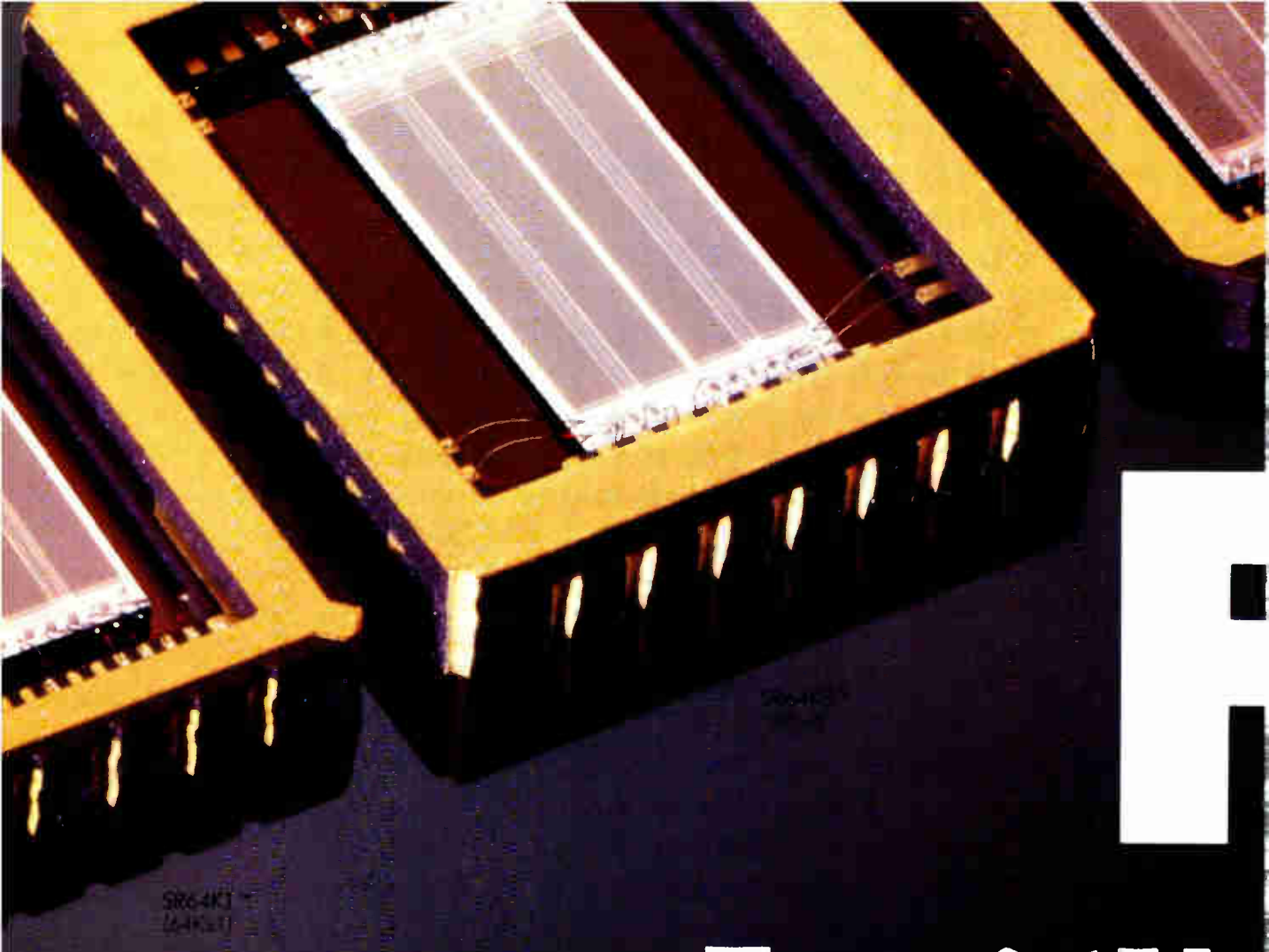

Fast 64K

Unsurpassed Quality and Reliability
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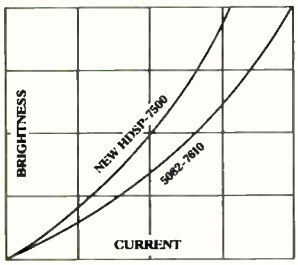

attractive solutions where space is at a premium. They have an eye-pleasing mitered character font that comes in four distinctive colors—red (HDSP-73xx), high efficiency red (HDSP-75xx), yellow (HDSP-74xx), or green (HDSP-78xx). And every one is pin-for-pin compatible with Fairchild's FND 350/360 series.

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JUNE 23, 1986 VOLUME 59, NO. 25

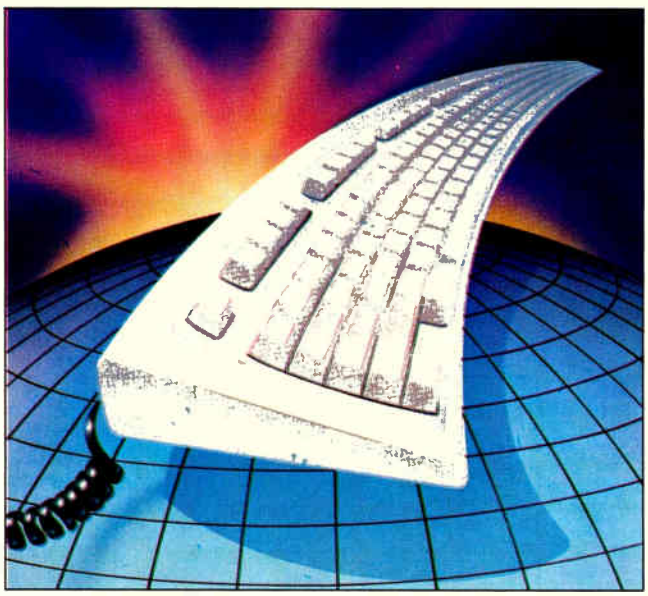
Electronics

NEWS

INSIDE TECHNOLOGY

PROBING THE NEWS

COVER



Cover illustration by Jeffrey Lynch

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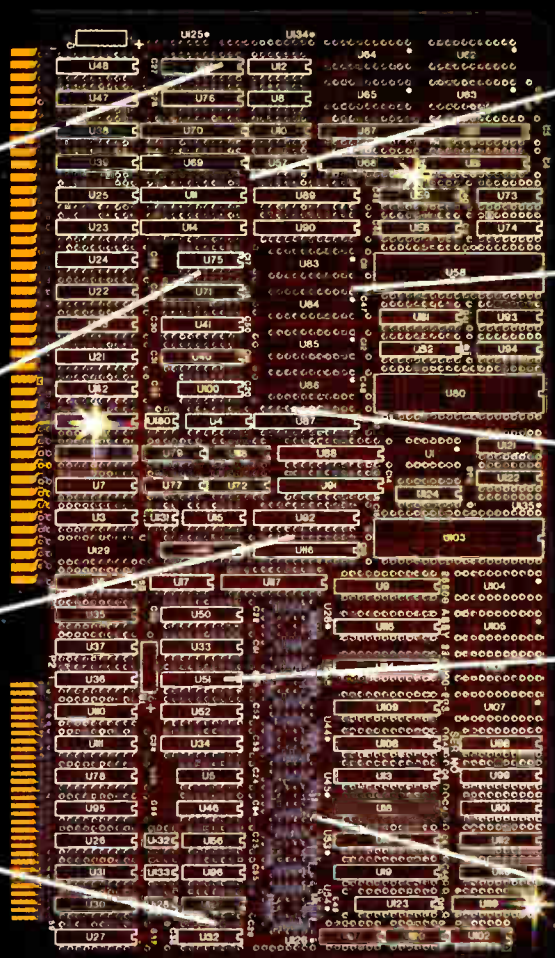

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Electronics

PUBLISHER'S LETTER

When IBM announces a new product, the electronics community listens. But when IBM announces 125 new products, the community gets a little anxious as it tries to interpret the significance of the occasion. Our job is to help our readers do just that: assistant managing editor Tom Manuel has laid it all out for you in a three-page report beginning on p. 50.

MANUEL: Having the right contacts paid off last week.

Tom's background and experience, as well as the contacts he has made over the years, were never more important than they were in doing this Probing the News. "On the day of the announcement—there were news conferences at the National Computer Conference in Las Vegas and at IBM headquarters in New York—I had to call 16 industry analysts before I could find any who were not either at the conference or on the phone discussing the ramifications of the announcement with someone else," he says. "Lucky thing I know so many of them."

Also important was the role of Editor-in-Chief Bob Henkel, who was present at the announcement in Las Vegas. He put on his reporter's hat, got on the phone, and started dictating notes to Tom. "That press conference took place on the opening morning of NCC," says Bob, "and to all intents and purposes, it was the only important event that occurred at the meeting—there wasn't much of the usual hoopla and new products that used to be associated with the NCC."

In fact, says Bob, as one indication of the mood of the computer industry, for the first time in recent memory it was possible during the show to walk into the Hilton, next door to the convention hall, and get a room without having a reservation. "That just isn't supposed to happen during an NCC, but it happened this year."

Beginning with the next issue, dated July 10, *Electronics* will return to biweekly publication. You, our readers, told us in a survey that you preferred your favorite magazine that way and we have responded. The change will give us the extra time and space to add depth to the technology news and reports that are demanded by today's senior engineers and technically trained managers—the kind of writing that has been our hallmark for more than half a century. At the same time, we will be able to continue the fast turnaround that has become the standard of the industry as we report and interpret industry and business issues. And last but not least, the change in frequency will bring with it an expansion of our exclusive coverage of product introductions.

Laurence Altman

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WEEK 35

Announcing the Am29C116: The 16-Bit CMOS Microprocessor that uses only 25 percent of the power of its bipolar counterpart. The rest of the power is yours. And the Am29C116 costs less than the bipolar. The savings are yours.

Am29C116

Satisfy your lust for money and power.

The Am29C116 is one more member of AMD's CMOS Microprocessor Family. It's the pin- and function-compatible version of the bipolar Am29116. Coming from such a heritage, you'd expect the Am29C116 to have the same computing power and flexibility. It does. And it has a system cycle time of 125ns.

It's microprogrammable so you have the flexibility of designing your own instruction codes. Plus, its architecture provides powerful insert/extract and bit manipulation capabilities for complex bit control. It has a three input ALU, barrel shifter and a priority encoder.

If you want to build in blazing speed, another member of the Am29100 Microprocessor Family might be for you. Like the high speed bipolar Am29116A with a system cycle time of 80ns.

And once you've acquired all that power and money from using the Am29C116, you can lust for something else.

Design and application seminars are available for this product. Write or call for information.

Circle 151 on reader service card

WEEK 36

In the daily trial between high performance and low power, a winner has emerged: The Am29C843 9-Bit CMOS Bus Interface Latch. Part of the Am29C800 Family of products, it keeps performance high on a meager power diet.

Am29C843

An open and shut case.

The latch waits patiently on a stand-by current of 80μA. But when it comes to speed, the propagation delay is 11ns.

The Am29C843 can also be used along with or in place of its Am29800 bipolar counterpart. Get just the balance of speed and power you need for your design. The Am29C843 provides 24mA drive, compared to the Am29843 which provides 48mA drive.

When design flexibility is important, the Am29C843 9-Bit CMOS Bus Interface Latch can be just as helpful. It has flow-through architecture. The ninth bit can provide error detection or diagnostics capability.

Why not see the Am29C843 9-Bit CMOS Bus Interface Latch and judge for yourself?

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Circle 152 on reader service card

WEEK 37

The digital telephone and ISDN are going to revolutionize voice and data communications. AMD gives you the cleanest way to go digital. Our ISDN Family of five devices gives you the standard interfaces plus power controllers for Integrated Services Digital Network.

Am7936

The power behind ISDN

The first member of the family is the Am7936 Subscriber Power Controller. It's the world's first ISDN power feed controller on a single chip.

The Am7936 meets the ISDN CCITT power recommendations. Including emergency conditions when local power is lost. As a matter of fact, it works in any phantom-feed system.

By the end of the year our ISDN Family will include the Digital Subscriber Controller, Digital Exchange Controller, ISDN Data Controller, and Quad Exchange Power Controller. They'll use both bipolar and CMOS technology to give you the optimum balance of system performance and efficiency with the lowest chip count.

Check out AMD's ISDN Family. And feel the power.

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WEEK 38

If you're racing along technology's edge, meet the most powerful 32-bit ALU around. The Am29332. It's the newest member of our Am29300 Family. Besides doing everything a less powerful ALU will do it also has a mask generator, funnel shifter and field logical operations. And it does it all in a single 80ns cycle. And every last nanosecond helps you beat the competition.

Am29332

It helps to know a powerful family.

The single-chip Am29332 uses everything it's got to achieve such incredible speed. To keep data racing through, it's designed with a built-in carry look-ahead and barrel shifter. A priority encoder insures that the most important data gets through first.

Whatever design you're working with, don't worry. The Am29332 is designed to let you emulate almost any system.

The Am29332 sets you free of the bonds of your present architecture. Because of the built-in high level instruction set and the three-bus flow-through architecture you get maximum performance and flexibility. And since correct breeding is important to powerful families, data integrity is insured through chip-level fault detection.

The Am29332 is just one member of a complete family solution to high performance 32-bit processing. A family that's nice to know when you need more power than anyone else.

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MEETINGS

Cable '86: 4th International Conference and Exhibition on Satellite and Cable Television, Online International Ltd. (Pinner Green House, Ash Hill Drive, Pinner, Middlesex HA5 2AE England), Metropole Centre, Brighton, England, July 8-10.

PC Expo, PC Expo (Steven Gross, 333 Sylvan Ave., Englewood Cliffs, N. J. 07632), Jacob K. Javits Convention Center, New York, July 9-11.

Britec 1986: British Information Technology Exhibition and Conference on Engineering Software, Computational Mechanics Ltd. (Elaine Taylor, Computational Mechanics Ltd., Ashurst Lodge, Ashurst, Southampton, SO4 2AA, England), Hilton at Colonial, Wakefield, Mass., July 14-16.

Net/Comm Security '86, Computer Security Institute (360 Church St., Northborough, Mass. 01532), Marriott Crystal Gateway, Arlington, Va., July 14-16.

International Computers in Engineering Conference, ASME (345 E. 47th St., New York, N. Y. 10017), Hyatt Regency, Chicago, July 20-24.

7th European Conference on Artificial Intelligence, European Coordinating Committee on Artificial Intelligence and Society for the Study of Artificial Intelligence and Simulation of Behaviour (Conference Services Ltd., 130 Queens Rd., Brighton, Sussex BN1 3WE, England), Brighton Conference Centre, Brighton, July 21-25.

ACM Conference on Lisp and Functional Programming, Association for Computing Machinery (Robert Halstead, Massachusetts Institute of Technology, 419 Technology Sq., Cambridge, Mass. 02139), MIT, Cambridge, Aug. 4-6.

National Conference on Artificial Intelligence, American Association for Artificial Intelligence (445 Burgess Dr., Menlo Park, Calif. 94025-3496), University of Pennsylvania, Civic Center, and Franklin Plaza Hotel, Philadelphia, Penn. Aug. 11-15.

30th International Technical Symposium on Optical and Optoelectronic Engineering, Society of Photo-Optical Instrumentation Engineers (P. O. Box 10, Bellingham, Wash. 98227-0010), Town and Country Hotel, San Diego, Aug. 17-22.

Siggraph '86, Association for Computing Machinery and IEEE (Siggraph Conference Management, 111 E. Wacker Dr., Chicago, Ill. 60601), Dallas Convention Center, Dallas, Aug. 18-22.

International Conference on Parallel Processing, IEEE Computer Society and Pennsylvania State University (IEEE Computer Society, 1730 Massachusetts Ave., N. W., Washington, D. C. 20036-1903), Pheasant Run Resort, St. Charles, Ill., Aug. 19-22.

ICSSDM: 1986 International Conference on Solid State Devices and Materials, the Japan Society of Applied Physics (1986 ICSSDM, c/o Business Center for Academic Societies Japan, 4-16, Yayoi 2-chome, Bunky-ku, Tokyo 113, Japan), Tokyo Prince Hotel, Tokyo, Aug. 20-22.

3rd International Congress on Advances in Non-Impact Printing Technologies, Society of Photographic Scientists and Engineers (Samuel W. Ing, Xerox Corp., 800 Phillips Rd., Webster, N. Y. 14580), Fairmont Hotel, San Francisco, Aug. 24-28.

8th Quartz Devices Conference and Exhibition, Electronic Industries Association (2001 Eye St., N. W., Washington, D. C. 20006), Westin Crown Center, Kansas City, Kan., Aug. 26-28.

Interconnect '86, United States Telecommunications Suppliers Association (333 N. Michigan Ave., Suite 1618, Chicago, Ill. 60601), San Mateo Expo Center, San Mateo, Calif., Aug. 26-28.

IFIP Congress '86: International Federation for Information Processing (Philip H. Dorn, Dorn Computer Consultants Inc., 25 E. 86th St., New York, N. Y. 10028), Trinity College, Dublin, Ireland, Sept. 1-5.

NCC-Telecommunications Conference, IEEE Computer Society *et al.* (Mike Sherman, 1899 Preston White Dr., Reston, Va. 22091), Civic Center, Philadelphia, Penn., Sept. 8-10.

International Test Conference, IEEE *et al.* (Peter Bottorff, International Test Conference, P. O. Box 264, Mt. Freedom, N. J.), Sheraton Washington Hotel, Washington, Sept. 8-11.

16th European Microwave Conference, Royal Irish Academy *et al.* (Microwave Exhibitions and Publishers Ltd., Convex House, 43 Dudley Rd., Tunbridge Wells, Kent TN1 1LE, England), National Concert Hall, Dublin, Ireland, Sept. 8-11.

Symposium on Optical Fiber Measurements, IEEE and Optical Society of America (D. L. Franzen, National Bureau of Standards, Division 724.02, 325 Broadway, Boulder, Colo., 80303), NBS Laboratories, Boulder, Sept. 9-10.

Swissdata '86, Swiss Industries Fair (Secretariat, Swissdata 86, Postfach, CH-4021, Basel, Switzerland), Fairgrounds, Basel, Switzerland, Sept. 9-13.

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20ns 64K SRAM (16K x 4)

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40MHz 16-bit processor with a 32-bit floating point on the same chip

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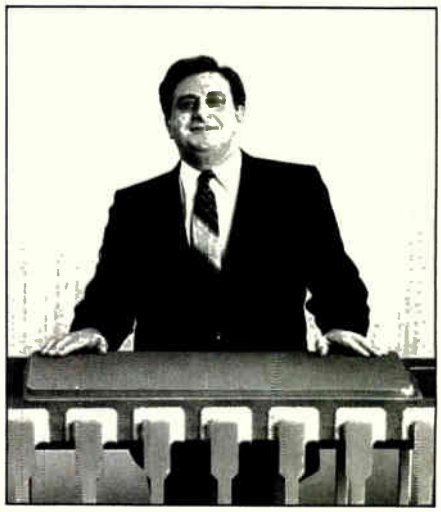

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Electronics
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TECHNOLOGY NEWSLETTER

TRW's PHASE 2 VHSIC CHIPS TEST AND RECONFIGURE THEMSELVES

TRW Inc. expects to occupy a strong position on the leading edge of semiconductor technology with its planned line of Superchips, which pack up to 27.9 million devices on a 1.4-by-1.4-in. die. The large chips, the Cleveland company's $60 million stake in Phase 2 of the Defense Department's Very High Speed Integrated Circuits program, have a lot more going for them than their size and density. An advanced wafer-scale-integration design technique enables them to bypass failed circuits and reconfigure themselves from redundant back-up macrocells—all under the control of on-chip testing programs.

TRW's Electronic Systems Group, Redondo Beach, Calif., already has passed the process test-chip stage and is working on preprototype devices to test the self-diagnosis and reconfiguration features. These are scheduled for completion later this year, with actual fabrication of the Superchips to start in 1987. TRW has Pentagon funding for three devices—a 64-K-word-by-32-bit mass memory and a signal processor, both in CMOS, plus a bipolar convolver/correlator. Three other chips await the DOD's go-ahead. All Phase 2 chips will have 0.5-μm feature sizes, and parts of the circuits will have clock speeds of 100 MHz. □

MATSUSHITA EYES FOURFOLD INCREASE IN OPTICAL-DISK DENSITY

A fourfold increase in the storage density of optical disks could be in the offing. Researchers at Matsushita Electric Industrial Co.'s Semiconductor Research Center have developed a lithium niobate chip that generates the second harmonic of optical frequencies. A laser beam injected into the second-harmonic generator has its wavelength halved and thus can be focused into a spot with one fourth the minimum diameter of the original beam. The Japanese company's experimental generator converts the 1.06-μm wavelength of an yttrium-aluminum-garnet laser to a 0.53-μm beam with 25% efficiency. Crucial to the new device are the nonlinear characteristics of optical-grade single-crystal lithium niobate and an optical waveguide measuring 2 μm wide by about 0.5 μm deep running the 6-mm length of the chip. By year-end, the Osaka research center plans to develop a second-harmonic-generating device optimized to convert to 0.42 μm the 0.84-μm beam from a semiconductor laser of the type used in compact disk players. □

CRAY WILL SHIFT TO HIGHLY AUTOMATED MANUFACTURING FOR THE CRAY-3

Cray Research Inc. intends to drop its traditional labor-intensive approach to building supercomputers in favor of automation. The Minneapolis supercomputer maker has set out to develop a highly automated manufacturing system to build its next-generation Cray-3 supercomputer. Instead of humans hooking up the rat's nest of wires inside the machines, specialized robots built to Cray design will handle a variety of Cray-3 manufacturing jobs, ranging from the dicing of gallium arsenide wafers into the custom GaAs chips to be used in the system to the actual wire interconnection. Prompting the move is the extreme miniaturization of the machine: a full-blown 16-processor Cray-3 system with 64 memory modules will be packed into less than one cubic foot of space, excluding power supply. No wire in the Cray-3 will be longer than 3 in., and because of the dense system packing, manual assembly and connection would be impossible, says a Cray source. So far, Cray has found no vendor that has exactly what's needed and may either modify existing equipment or build its own. The Cray-3, when delivered in 1988 or 1989, is expected to exceed by 10 times the performance of the current-generation Cray-2, which has a peak rating of 1.2 billion floating-point operations/s. □

ELECTRONICS NEWSLETTER

IBM SEES SCANT RISE IN BUSINESS FOR 1986

As IBM Corp. goes, so goes the computer business in the U. S.; and the going looks bleak so far for 1986. The Armonk, N. Y., company now expects the first quarter's lackluster results—earnings per share rose only slightly to $1.65, from $1.61 a year earlier—will continue into the second quarter, says chairman and chief executive officer John F. Akers. "If business doesn't pick up in the U. S., I think IBM will have trouble matching 1986 earnings," Akers told financial analysts last week. Nonetheless, the company's strategy of concentrating on high-margin hardware looks right on. The company captured 41% of the total data-processing revenues in 1985 and parlayed that into more than 71% of the year's operating profits, says Stamford, Conn., market researcher the Gartner Group Inc. in its just-released Top 100 DP Almanac for 1985. □

ETA TESTS PROCESSOR OF NEW SUPERCOMPUTER

ETA Systems Inc., St. Paul, Minn., marked a milestone in mid-June on the way to its planned ETA^{10} supercomputer when it demonstrated a prototype central-processing-unit board. The company says it has successfully executed advanced operating instructions, diagnostic tests, and the benchmark code of a prospective European customer on the prototype. Running in liquid nitrogen at 77K, the prototype CPU houses 240 of the 20,000-gate CMOS array chips that will form the basis of the ETA^{10} [*Electronics,* May 26, 1986, p. 33]. In the final system, up to eight CPUs will work together in the ETA^{10} to produce a peak performance of 10 billion floating-point operations/s. Despite the successful hardware demonstration, ETA is backing off on its earlier-announced plan to deliver the first ETA^{10} by Oct. 1. The company now says the first system—a four-processor machine for Florida State University—will be delivered by year end. □

ALL NIPPON AIRWAYS SWITCHES TO IBM FROM UNIVAC FOR ITS COMPUTER

All Nippon Airways Co., Japan's second-largest airline, will switch computer suppliers when it creates its international reservation system: it will buy the host mainframes from IBM Corp. Only recently permitted to extend operations outside of Japan, All Nippon Airways currently runs its domestic reservation system on a Univac Series 1100 mainframe from Nippon Univac Kaisha Ltd. The Tokyo company switched to IBM because most of the major airline companies worldwide are using IBM computers for reservations and because it plans to use software, developed by British Airways, that runs on IBM systems. The contract for the IBM 3090-200 computers—estimated to run more than $90 million—should be signed this fall. The system will go into service in late 1987 and be fully developed by spring of 1988. □

BERLIN WILL BE FIRST WITH MAGNETIC-LEVITATION TRANSIT SYSTEM

High technology will bring a lot to the party when Berlin celebrates its 750th anniversary next year. On May 1, West Berlin will put into operation an initial one-mile stretch of the world's first full-fledged magnetic-levitation passenger transport system. Experimental systems already exist in Braunschweig and in Japan. The Maglev system, developed by a consortium of companies headed by Magnetbahn GmbH, has trains that require neither wheels nor on-board drive motors. Instead, the vehicles are levitated by permanent magnets on the vehicle. Guide rollers, with the aid of electronic controls, keep the air gap between the guideway and the permanent magnets within 15 to 30 mm. Propulsion is by a linear synchronous motor whose stator lies along the guideway. □

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PRODUCTS NEWSLETTER

SILICON COMPILERS TO UNVEIL UPGRADE AT DESIGN AUTOMATION SHOW...

Silicon compilers are expected to dominate the new product action at next week's Design Automation Conference in Las Vegas. Silicon Compilers Inc., San Jose, Calif., will unveil Genesil 86, an upgrade of its Genesil product. With it, users will be able to design smaller, faster chips than before, as well as to implement more applications and reduce total design time. It can compile designs down to the Very High Speed Integrated Circuit program's 1.25-μm level, and new interconnection algorithms can reduce chip size over previous compilations by 5% to 40%. Genesil 86 also adds such complex functions as asynchronous first-in first-out buffering and parametric multipliers. The speed of the built-in functional simulator has also been doubled to cut design time, and Genesil can now be linked with other vendors' simulators. □

...WHILE THREE OTHER COMPANIES WILL OFFER THEIR OWN COMPILERS

Also at the Design Automation Conference, Silicon Design Labs, Liberty, N. J., will announce several new features added to its $75,000 Generator Development Tools. Among them is one that will save engineering time by automatically compacting circuit designs. Also, NCR Corp.'s Microelectronics Division, Dayton, Ohio, will announce that it is bundling the General Development tools with its cell library. Finally, Seattle Silicon, Seattle, is unveiling three compilers. The $125,000 C.5 lets users design their own compilers for custom modules independent of process; the C.4, at $80,000 enables engineers with little design experience to design ICs using predesigned compilers; and the C.3 handles schematic capture, circuit definition, and simulation. □

ONE SET OF SIMULATION DATA SERVES BOTH DESIGN AND TEST

Test Development Series, a software package from Test Systems Strategies Inc., bridges the gap between design and test by permitting design engineers to use simulation data from their computer-aided-engineering systems on their automatic test equipment. Using the series, engineers can establish test requirements early in the design process, when modification is easier and less expensive. Pricing varies because the Beaverton, Ore., company tailors the basic software to support data entry from a specific CAE environment and to generate tester-specific programs for a target tester. The Test Development Series is available now. □

INTEL CARD ADDS 3.5 MEGABYTES OF MEMORY TO THE PC AT

Users of the IBM Corp. Personal Computer AT can now add a multifunction card that provides up to 3.5 megabytes of RAM. The PS/AT, from Intel Corp.'s Personal Computer Enhancement Operation in Hillsboro, Ore., contains ports, utilities, and up to 1.5 megabytes of RAM (a piggyback card boosts this to 3.5 megabytes). The PS/AT, which starts at $545, can be used to add memory up to the AT's 640-K-byte limit and serve as expanded memory following the Lotus/Intel/Microsoft expanded memory specification or Xenix and other protected-mode operating systems. □

LATTICE SEMICONDUCTOR TO SAMPLE 256-K STATIC RAM IN AUGUST

Lattice Semiconductor Corp. will be ready to ship samples of its first 256-K static RAM by August. The Portland, Ore., company's part will be organized as 256-K by 1 bit and have a 35-ns access time. Samples will be priced at about $150. The CMOS part will consume 600 mW. In addition, the company is willing to work with customers on application-specific RAMs, such as versions with multiple ports for parallel-computer architectures. □

Electronics

HOW IBM IS SHAKING UP THE DISK-DRIVE BUSINESS

ITS LATEST MOVE: AN 8-IN. DRIVE FOR THE OEM MARKET

LAS VEGAS

The disk-drive business is reeling from yet another punch thrown by IBM Corp. Last week, the computer giant quietly entered the market for OEM drives. It was the third in a string of moves that the company has made in this market in recent weeks. In early April, it cut wholesale prices by up to half on its 5¼-in. disk drives for personal computers. Then IBM announced that its new 8-MHz version of the Personal Computer AT would be sold only with a 30-megabyte drive. The result was chaos among value-added-reseller dealers, who stopped ordering drives from the independent suppliers.

The announcement of model 678, an 8-in., 478-megabyte (unformatted) drive for original-equipment manufacturers, did not come at IBM's National Computer Conference product blitz (see story, p. 50). Instead, it was part of a new product announcement at NCC by Britton-Lee Inc., Los Gatos, Calif., which uses the model 678 in its new 1-gigabyte RS-350 relational server data-base system (see "Britton-Lee builds server around IBM drive").

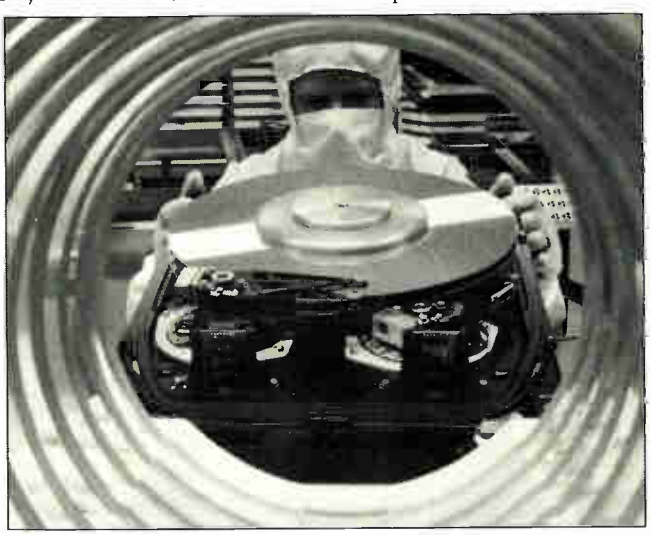
Because IBM has made no official OEM product announcement yet, the model 678's price is unavailable. The drive is an OEM version of the 9332 drive announced at NCC for IBM's System/36 and /38. These drives use IBM's latest thin-film heads and an enhanced particulate oxide medium to attain a density of 26 million bits/in.^{2}—the highest recording density IBM has in use today. Similar state-of-the-art technology is used in a new 14-in., 856-megabyte drive, the 9335 model B01, announced for System/38.

As packaged in subsystems for the IBM computers, the drives employ a high-level interface that is IBM's implementation of the draft American National Standards Institute standard for Intelligent Peripheral Interface-Level 3.

However, to make the 678 as competitive as possible in the OEM market, IBM is offering it with the popular Small Computer Systems Interface. IBM also puts a lot of faith in the reliability of these drives, as evidenced by the one-year warranty it is offering on the disk subsystems for its midrange computers.

The 678 is therefore very competitive in capacity, performance, and reliability. If it is also competitive in price, and there is no reason to believe it will not be, then it should make waves in the drive business, observers predict.

In addition to its plans to sell drives, IBM's drive-procurement practices for its PCs continue to stir up turbulence.



ASSEMBLY. The 14-in. IBM model 9335 drive shown shares technology with the 8-in. 678, which IBM has made available to OEMs.

As industry analyst Jim Porter of Disk/Trend Inc., Los Altos, Calif., has been warning since last year, Big Blue has been moving at a steady pace to tighten control over its drive suppliers. James Stone, an analyst at Shearson Lehman Brothers Inc., New York, backs him up.

The reason, Stone says, is that IBM "believes it should not be dependent upon an outside supplier for a key component. The problems caused by relying on a single source for the PC AT drive were very costly to IBM." The single source he is referring to was Computer Memories Inc., Chatsworth, Calif., which no longer is an IBM supplier.

Because the drive is the single most costly component in PCs—about 20% of the total cost—it makes sense for a company as big as IBM to bring drive manufacturing in-house to capture the value added, Stone points out. This obvious fact seems to have been generally overlooked by those disk-drive makers who had hoped IBM would continue to buy drives in the open market.

Stone and Porter both note that IBM has three plants already churning out 5¼-in. drives for internal use. As a customer, it had been buying a third of all 5¼-in. drives sold, and it will continue to be the biggest influence on the business. Not only will it remain the biggest user, but it likely will start selling its drives to OEMs.

Among value-added-reseller dealers, IBM's lower prices and its bundling of the drive in the AT have resulted in chaos. The dealers stopped ordering from the disk-drive companies for weeks. These actions cut aftermarket sales by 30%—or even more, according to Stuart Mabon, president and chairman of Micropolis Corp., Chatsworth. And IBM doubled the number of its own drives being shipped with PCs.

Seagate Technology, Scotts Valley, Calif., will be the most directly affected, being the leading supplier of 20- and 30-megabyte drives for the PC/XT and AT, both to IBM and for the aftermarket. However, Stone says, Seagate will not be hurt in the short term, and Al Shugart, Seagate's founder and president, agrees. Even though the company loses aftermarket sales due to the IBM moves, it paradoxically is getting more business from IBM because the computer company cannot yet meet its own requirements.

"Funny, eh?" asks Shugart. "We sell to both sides—IBM directly, and the VARs." Even he does not think this happy straddle will continue. But "overall, the effect is good. If it brings the price of computers down, it expands the market. That's very healthy for drives."

But unpleasant surprises are showing

up elsewhere. For example, Priam Corp., San Jose, Calif., has been hurt badly, even though it does not make low-end drives comparable to Seagate's. On June 11, Priam made a surprise announcement that its current quarter will close with red ink due to a 25% revenue shortfall.

Priam's orders slowed while the PC drive aftermarket assessed and adjusted to the announcements that IBM made earlier this quarter, the company says. According to a Priam executive, IBM's bundling a drive with the AT hurt Priam as badly as the lower prices did. And other companies in the aftermarket may suffer as well; for example, companies offering hard-card plug-in drives will have to be on guard.

Mabon of Micropolis sees a silver lining, however. He can afford to be somewhat objective, because his company doesn't sell much to IBM and is not threatened by the 5¼-in. drives IBM now makes for itself. He believes IBM's intention to take all disk drive production in-house is healthy for the drive business.

The change will remove the disruptive effects of IBM on the market and also take away the temptation to sell disk drives to IBM. "You don't have to sell your soul to the devil," Mabon says. Even if IBM introduces 170- and 380-megabyte 5¼-in. drives, as it might, and sells to the OEM market, the effects on suppliers such as Micropolis would not be great. Mabon reasons that OEMs are system companies that compete with IBM, and they would not likely switch to buying disk drives from a competitor.

–Tom Manuel and Larry Waller

BRITTON-LEE BUILDS SERVER AROUND IBM DRIVE

The first product using the model 678, IBM Corp.'s 478-megabyte 8-in. disk drive, surfaced last week at the National Computer Conference in Las Vegas.

Britton-Lee Inc., the Los Gatos, Calif., maker of relational data-base machines, unveiled its RS350 1-gigabyte data-base system, the second and more powerful member of its RS300 family of relational servers for integrated office and shop-floor applications. These low-end servers provide a high-performance data-base management system for networks of personal computers, work stations, and departmental computers.

Britton-Lee has been working with IBM for three years to develop the drive, says president David L. Britton. The company is one of IBM's first original-equipment-manufacturer customers for it.

Britton says his company was very interested in getting a disk drive from IBM, in part because IBM customers represent one of the big markets for Britton-Lee's servers. These customers, Britton-Lee reasoned, would look more favorably on a data-base server that stores the data on IBM drives, which have a reputation for reliability. According to Britton, "this is the first time that IBM is in the OEM disk-drive business, and we wanted to be the first to take advantage of it."

The complete Britton-Lee RS350 product, which includes a 10-MHz data-base processor, 1-megabyte of memory, and 300 megabytes of streaming-tape backup, in addition to the disk drives, will be maintained by Britton-Lee, but with backup support from IBM on the drives. An optional backup system, using a 400-megabyte write-once optical disk drive, is also available. *–T. M.*

IC PROCESSING

WISCONSIN RING SHINES FOR X-RAY WORK

STOUGHTON, WISC.

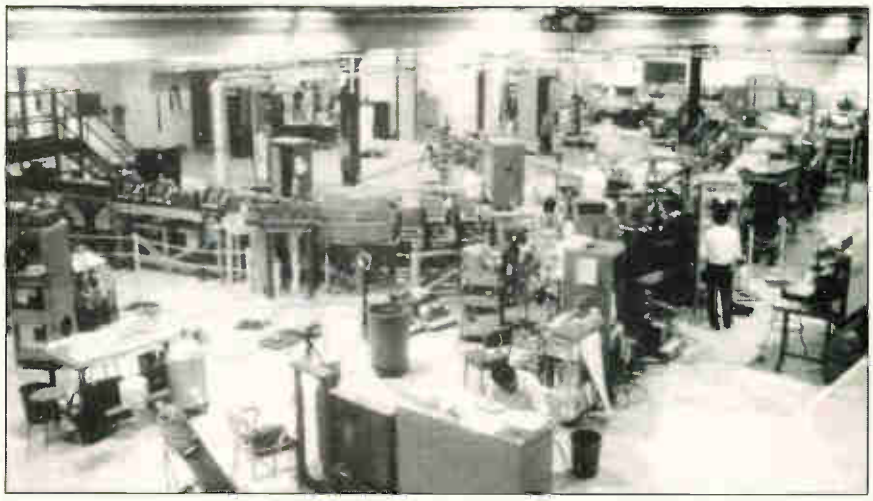
Serendipity could help the University of Wisconsin play an important part in any future U. S. initiatives to head off foreign dominance in high-energy synchrotron-based X-ray lithography. Amid growing cries for stepped-up U. S. research in the field, the university appears well positioned to serve a role.

Indeed, say university officials, the federally supported UW-Madison Synchrotron Radiation Center could provide one of the few outlets for U. S. industrial synchrotron lithography research in the near term. "The Wisconsin ring is one of the few machines—if not the only machine in the world—that currently has an adequate number of uncommitted ports to offer significant access to U. S. companies interested in exploring the potential of X-ray lithography," says Henry Guckel, director of the Wisconsin Center for X-ray Lithography on the school's Madison campus.

HAPPY ACCIDENT. The ring itself is 14 miles away in Stoughton, and is operated by the university under National Science Foundation funding. It was by chance as much as by design that the peak energy levels produced by a new 1-GeV electron-storage ring at the Stoughton facility occur at 11.6 Å, very close to the 10-Å wavelength that researchers think may be ideal for X-ray lithography, says John D. Wiley, associate director at the X-ray lithography center.

Seventeen of the 36 ports on the 1-GeV Wisconsin ring, which has a circumference of 88.9 meters, are committed to physics and chemistry experiments, and five are committed to lithography work. The center already operates a beamline dedicated to X-ray lithography on one port and has fabricated test patterns with line widths of about 0.4 to 0.5 μm on silicon using polymethylmethacrylate resists, Wiley says. A more versatile, second-generation beamline is under construction on a second port.

The university just last month nailed down assurances of continued NSF support for the Stoughton facility, after some early problems in the ring—first made available to experimenters last November—were ironed out. And it comes at a time of growing concern



SPACE AVAILABLE. Ports are free for X-ray lithography work on Wisconsin synchrotron.

over future U. S. competitiveness in advanced high-throughput X-ray lithography [*Electronics*, June 16, 1986, p. 13].

A synchrotron produces high-energy X rays by use of magnetic fields that accelerate electrons around a storage ring. Many think the technology could be vital to fabricating the submicron geometries needed for the ultralarge-scale integrated circuits of the 1990s. By some estimates, West Germany and Japan have a two- to three-year lead over the U. S. in advanced synchrotron radiation development, thanks to state-sponsored efforts in those countries.

In the U. S., only IBM Corp. has done extensive synchrotron-radiation research, using the National Synchrotron Light Source at Brookhaven National Laboratory, Upton, N. Y. Given growing foreign efforts, many U. S. officials see an increasing need for a government- or industry-sponsored consortium to work on development of production-worthy ring-based systems.

At the University of Wisconsin, Wiley says the Stoughton facility could prove complementary to Brookhaven's attempts to promote a joint U. S. effort to develop laboratory-size compact storage rings. A West Berlin company, COSY Microtec GmbH, has already unveiled plans to deliver such a unit, known as the COSY (for compact synchrotron), in 1988 [*Electronics*, May 26, 1986, p. 15].

Wisconsin officials say funding the center is a way for companies to begin participating now in research into X-ray mask fabrication, resists, optics, exposure tools, processing, and process modeling. The energy tunability of the ring, between 700 MeV and 1 GeV, enables it to emulate the spectral distributions of compact rings, says Guckel. This means that processes developed at the Wisconsin facility will be directly transferable to other sources.

AT&T Bell Laboratories has already done some experimental exposure work at the Wisconsin ring on an informal basis and plans to come back for a second time this month, says Wiley. Sperry Corp. has also provided some funding and donated some equipment to the center, though the New York company has not yet made any exposures. Wiley says the center has had contact from other firms, including Intel Corp., which have also expressed interest in doing experimental X-ray work. *–Wesley R. Iversen*

TELECOMMUNICATIONS

ENCRYPTION FOILS CELLULAR SNOOPING

BASKING RIDGE, N. J.

Cellular mobile telephones may have revolutionized telecommunication from the driver's seat, but law and technology have conspired to keep cellular calls from being as private as users would like. As long as unencoded voice signals are carried over the airwaves, they can fall victim to eavesdroppers, who are legally allowed to monitor such conversations.

To foil Peeping Toms of the airwaves, AT&T Information Systems, Morristown, N. J., and Bell Atlantic Mobile Systems, Basking Ridge, offer an encryption service that gives analog mobile phones a new security. It uses AT&T's model 1620E encryption device, an 8-lb unit about the size of a shoe box that fits beside the cellular transceiver in a car trunk, and an accessory to AT&T's standard ESS central-office switch called the Autoplex Telecommunications System. The system also uses a proprietary digital encryption algorithm approved by the National Security Agency, but AT&T is saying little more about the system's operation.

NOISE INSERTION. Virtually invisible to the user, thanks to its high sampling rate, the encryption device first converts the analog voice signal into a digital bit stream, then encrypts it using a random-number generator to add noise to the signal before returning the signal to analog form. The cellular transceiver then modulates the signal up to the cell site, which passes it on to the central switch. Once there, the signal is decoded and launched into the land-line network.

The signal undergoes extensive processing as it travels from point to point, but voices do not lose their personal characteristics, says Beverly Bach, general manager for the Bell Atlantic effort. "This is a technology breakthrough," she says. "The voice sounds human; it's recognizable. It doesn't sound like Donald Duck."

Embedded in the coded bit stream are an encryption key and an initialization vector generated by the encryption device. Without these, the Autoplex system could not decipher the message.

Eavesdroppers would have to know and decipher the encryption algorithm, the encryption key, and the initialization vector to break the code. Otherwise, says Bach, "an eavesdropper would hear nothing but garbage." The mobile phone's signal is only encrypted between the car and the central office. Bach says each user's encryption key "is embedded into the system such that we can't even read the switch to discover it."

The need for secure mobile communications systems is well established, with the heaviest demand coming from security-conscious users in government and government-contract work who discuss classified material on cellular phones. Bach says "90% of the market is going to be in government and government contractors. It's a specialty item for the nongovernmental user, but we feel that up to 50% of the governmental users [of cellular technology] will want it."

Initially available only in the Baltimore-Washington, D. C., corridor, Bell Atlantic will expand its service to Norfolk, Va., this month. In addition, AT&T is studying demand in other cities, including New York, Los Angeles, and Seattle. *–Tobias Naegele*

GRAPHICS

CANON GRABS THE LEAD IN ELECTRONIC CAMERAS

CLICK. Canon's electronic camera shoots up to 10 images/s and stores them on a 2-in. disk.

NEW YORK

In the long drawn-out race to market the first electronic still camera, Canon Inc. seems to have pulled out in front of Sony and Hitachi. In August, it will start selling the first commercial model. Though the Still Video System will offer lower image quality and cost nearly three times as much as top-of-the-line professional 35-mm equipment, Canon is betting that newspapers and other professional markets will be willing to accept the poorer image clarity in exchange for the speed advantage.

SVS records up to 50 photographic images on a 2-in. floppy disk. The system

was used experimentally during the 1984 Summer Olympics in Los Angeles, and the Tokyo company is hoping that the upscale professional market will be attracted to its full-system approach that can transmit images by telephone from almost anywhere in the world. To be sure, the image quality, at 320 scan lines, cannot be classed as high resolution; but it is good enough for most fast-turnaround purposes.

Both Sony and Hitachi said their companies still have no immediate plans to introduce electronic cameras. Sony Corp. was the first to show a prototype when in brought out its Mavica, for magnetic video camera, in 1981. The company tested a black-and-white professional Mavica during the 1984 Summer Olympics in Los Angeles, but a spokesman says that even though development work continues on several different prototypes, Sony is concentrating its efforts on 8-mm full-motion video because "people would rather see movies than stills on their TV."

Hitachi Ltd., which many thought would be the first to market with a still video camera, also has a prototype. But there are no current plans to market it, says Kei Yamashita, a senior researcher at Hitachi's Consumer Products Research Center in Lyndhurst, N. J.

COMPATIBILITY IS KEY. Canon is emphasizing the SVS's compatibility with current technology. The camera has its own set of specialized lenses but can also accept standard Canon lenses, for example, and officials say the transceiver is compatible with virtually all existing wire-photo systems.

The full system lists at about $35,000 and consists of a single-lens reflex camera; a transceiver; a unit for recording, playback, and editing; and a four-color ink-jet printer. Each component is expensive—the RC-701 camera body alone costs $2,595, the RP-601 printer runs $6,950, and the RT-971 transceiver unit needed to transmit images over phone lines costs a hefty $19,900.

At the heart of the SVS is Canon's own image sensor, a tiny full-color charge-coupled device. Just 1/3 in. in diameter, the CCD can digitize up to 10 images/s.

The recording format fits a standard supported by a number of electronics and photography companies, including Sony, Hitachi, and Eastman-Kodak Co., the Rochester, N. Y., photographic giant [*Electronics*, Oct. 21, 1985, p. 20]. Sony and Hitachi offer color printers supporting the format, and Hitachi has a player/recorder similar to the one Canon introduced last week. Kodak's entry into still-frame video was designed for use with another product that used its instant-photography technology, but the status of both was clouded by a court ruling against Kodak in its suit with Polaroid Corp. *–Tobias Naegele*

SEMICONDUCTORS

MOSTEK TURNS TO POWER MOS FETS

CARROLLTON, TEXAS

One important part of Mostek Corp.'s effort to redirect itself from MOS memories has survived some of the roughest times in the semiconductor industry's history. Three long and difficult years after the previous ownership launched an intelligent power-chip project, Thomson Components Mostek Corp. is fine-tuning its first products and a new operation to make a run at a new automotive market for smart high-side load switches.

Mostek's integrated circuits are aimed at intelligent power control in future vehicles containing space- and weight-saving multiplexed wiring systems. Industry estimates say these cars could have 30 or more of these intelligent power-switching ICs to handle headlights, interior lighting, dashboard displays, and other electrical systems drawing power from the battery. Luxury autos could have another 30 to activate electrical motors for adjusting seats, rolling windows, moving mirrors, and operating other power options.

Though high-side power chips are expected to sell for $1 to $1.50, Mostek and its competitors believe the business will reap big profits. Besides the high volumes associated with sales to automakers, they hope to become sole sources for such products. Mostek will run up against competition from the likes of International Rectifier, Motorola, and Siemens (see "The power-FET competition is already intense").

Initially, giant automakers worldwide are treating the high-side multiplexed-wire switches as custom designs. The hope in automotive electronics circles is to have standards that would result in commodity intelligent power ICs by decade's end. Meanwhile, chip makers have been offering samples of core devices that represent products tailored to meet each automaker's system specifications.

Mostek's initial entry into automotive power MOS FETs is the MK5501, which quietly entered the sample stage last year. The 10-A, 60-V part combines a power MOS FET with analog circuits and logic for self-protection as well as diagnostics, which can be reported back to a host microprocessor or microcontroller.

The chip is in the midst of a design

THE POWER-FET COMPETITION IS ALREADY INTENSE

Entrenched competition faces Thomson Components Mostek Corp. in its bid to become a leading supplier of power integrated circuits to the auto industry. Motorola Inc. and International Rectifier Corp. have already made critical inroads in Detroit by qualifying discrete MOS FETs at Chrysler, Ford, and General Motors [*Electronics*, June 2, 1986, p. 16]. And Siemens AG has been pushing a product that competes directly with Mostek's high-side load switches.

"The automotive industry has very long qualification cycles. Sometimes we have to work on a project for years," notes Dan Artusi, strategic marketing manager for discrete products at Motorola's Semiconductor Products Sector in Phoenix. Motorola has been promoting its five-pin MPC1500 Smartpower logic-to-load switch for a couple of years. A derivative of the switch, called the MPC1510, will be aimed at auto applications that have inductive loads or lamps, which do not have big inrush currents.

In the fall, Motorola will offer samples of a five-pin MPC1700 Smartpower permanent-magnet motor controller, targeted at blowers in air conditioners and fuel pumps.

The company expects that some 1987 car models will have some kinds of Smartpower devices. Heavy industrial and mass-transit vehicles are expected to follow suit in the next 18 months.

Siemens has been selectively offering samples of a high-side load switch to about two dozen automakers worldwide; the automakers have about 1,000 preproduction parts, says George Fordor, director of marketing at the Munich company's operation in Broomfield, Colo. The BTS412 is a core device intended to give engineers at car makers an idea of how the Siemens parts perform.

Like other intelligent-power high-side devices, the chip protects itself against overheating, excessive currents, and low-voltage operating conditions. The BT412 can also send back information to the controlling host microprocessor.

A high-side switch set up to be addressed by multiplexed wiring schemes is in Siemens's plans for the near future. *–J. R. L.*

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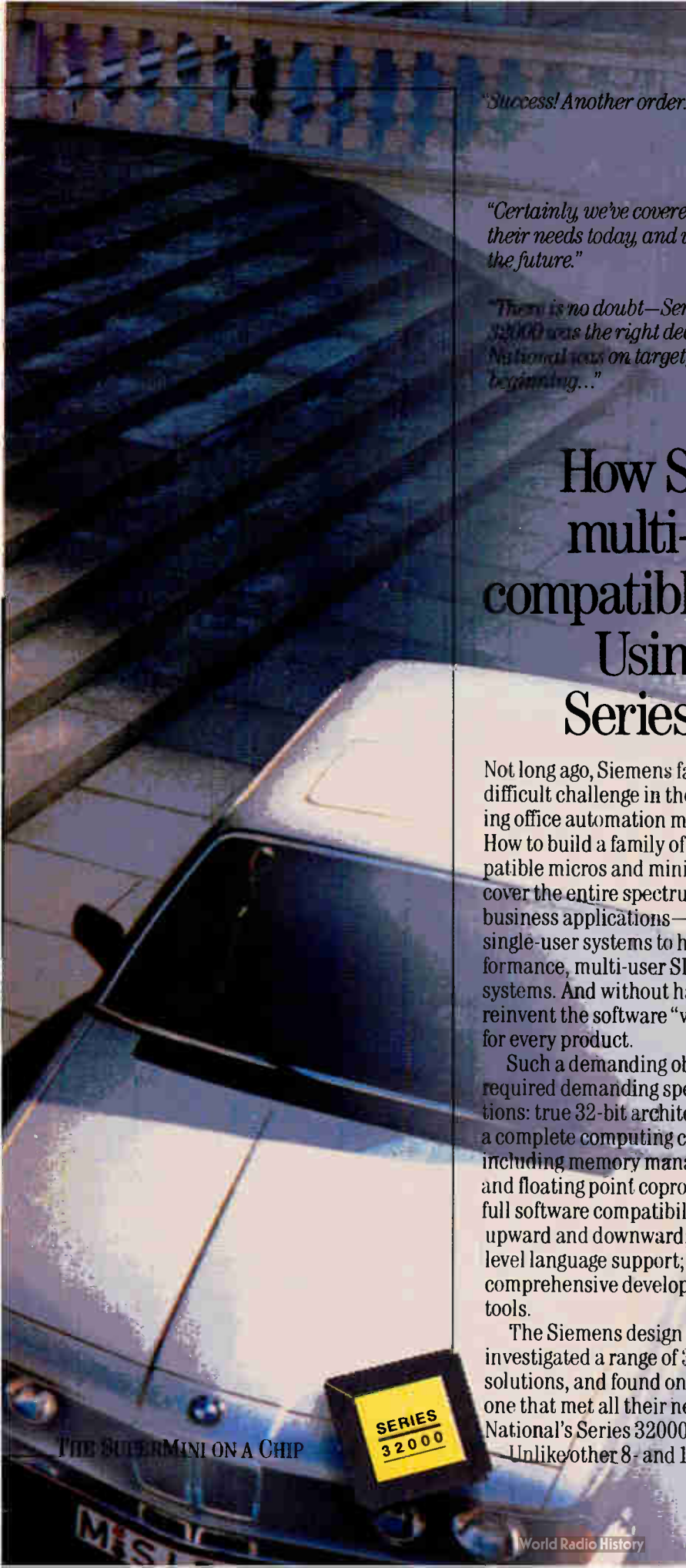

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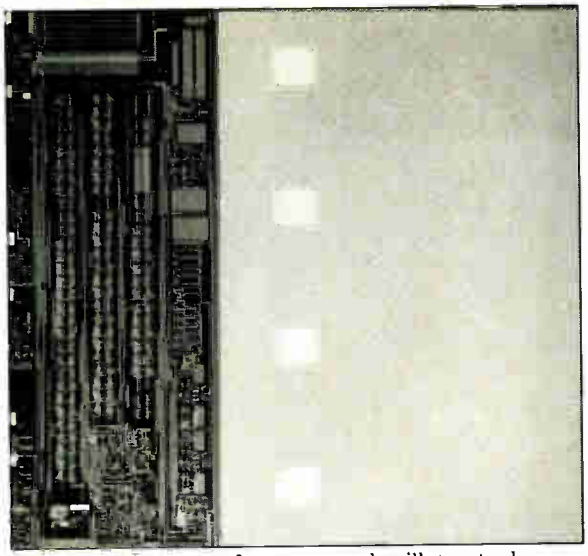

SWITCH. Mostek's high-side load-switching chip carries an n-channel power FET plus analog and digital circuits.

revision to boost performance and will be ready to enter production early next year, says Steve Whipple, director of the power products operation. Mostek officially formed that operation earlier this month.

The automotive chip is the first device from Mostek to combine CMOS and bipolar logic on the same die with a vertical n-channel power MOS FET (photo). Mostek's sudden bid for future automotive sales is perhaps the most significant sign of a changed silicon company.

FOREIGN AID. Just last year, the company was losing $1 million a day before it was shut down by its parent, United Technologies Corp., Hartford, Conn. Then it was saved from closure by Thomson-CSF in an 11th-month purchase [*Electronics*, Nov. 4, 1985, p. 26]. Since then, the Paris multinational has greatly downsized its Carrollton subsidiary and married most of Mostek's product portfolio with its own in an effort to gain market share in the U. S.

The MK5501 has not only survived the transition but emerged as a promising new hope for a rebounding Mostek. "The reason we feel we can make a strong bid from Mostek's standpoint is that we have a very good process technology and process capability," Whipple says. "To drive the cost down, which is a mandate from automotive suppliers, we feel it is key to have a simple, manufacturable, high-yielding technology."

Mostek started developing its power-IC process technology in 1983. United Technologies saw the effort as a way to make the subsidiary profitable by diversifying its product line and reducing heavy dependence on dynamic random-access memories. The power IC product-development thrust began a year later.

Following a period of reorganization under Thomson, Mostek has now placed the activity under a product operation. In addition to the automotive parts, Mostek expects to ship samples this summer of a line of electroluminescent flat-panel display drivers, the MK5563-5566, which are the second-source counterparts to the HV03-06 ICs from Supertex Inc.

In the high-side load-switching ICs, Mostek is using conservative 5-μm minimum feature sizes in its MOS FET technology, but it has developed a process to reduce the number of mask steps in fabrication, says Whipple. "The actual geometry of the power FET is not dictated strictly by the photolithography. It is dictated by the sequence of mask steps," he states. About 65% of the chip is the power FET switch, and Whipple says "we feel we have a technology that will bring the density of the power FET down so far that using 5 μm in the analog and logic areas will have no significant impact." Mostek has applied for four patents in its small-FET construction technique, which the company declines to describe at this time.

The industry's first hurdle for integrated power switches has been cleared: demonstrating the ability to combine power, logic, and analog on the same chip at potentially lower cost than relays and electromechanical switches, "The next hot topic is product reliability," says Whipple.

"These chips are self-protecting," he notes. But before the self-protection features are activated, "you must go up to a certain [high] temperature, current, or voltage, which puts a considerable stress on the product.

"Automotive people are seeing the products, and they meet the specs, but the question is how will it work over the next 10 years. So far, the industry does not have a lot of reliability information." —*J. Robert Lineback*

OPTICAL STORAGE

DUAL-FILM DISK HIKES MAGNETO-OPTIC DENSITY

TOKYO

A disk drive with a dual-film medium demonstrated by Japan's NHK broadcast network could be the route to practical, highly dense magneto-optic storage. The medium uses one film for writing and the other for reading; each is optimized for its purpose. The read layer aligns its magnetization in response to the pattern written in the write layer below it.

With separate layers for reading and writing, materials can be optimized to relax critical tolerances inherent in the reading operation, for example, moving such systems closer to practical use in less-controlled operating conditions outside the laboratory. And freed from worrying about the reading characteristics of the write layer, materials scientists can concentrate on increasing its ability to store densely packed bits.

Separate layers are optimized for reading, writing

NHK's two-disk drive is configured for operation as a video storage unit for fast-access instant replays, editing, and other broadcast purposes. But the video signal is stored digitally, and the technology could be used in the general-purpose digital realm. At a capacity of 4.2 unformatted gigabytes on a 305-mm single-sided disk, its developers say they pack twice the number of bits (over 25,000) into an inch of track that other reported systems have achieved.

Development of the system was coordinated by Tatsuo Nomura, chief research engineer at NHK's Science and Technical Research Laboratories in Tokyo [*Electronics*, June 9, 1986, p. 9].

As in other magneto-optic disks, information is written on the new disks with a high-power semiconductor laser beam operating at 830 nm and read by a lower-power laser beam at the same wavelength. The high-power laser heats the write layer beyond its Curie temperature, so a magnetic field applied as the spot cools can reverse the magnetization polarity of the thin film at that location. Reading is performed by sensing the difference in laser-light polarization rotation in a reading beam reflected (in NHK's case) from the read layer, making use of the magnetic Kerr effect on the reflected light beam's plane of polarization.

Thin film for writing should be capable of recording bits with submicron diameters. And the material's Curie temperature should be high enough to prevent erasure by heat from the reading laser and to ensure long-term stability. The temperature should not be so high, though, that the laser can't write or that the disk substrate deteriorates

from passing through the required temperature range time after time. In the NHK disk, a terbium-iron film with a Curie temperature of 135°C is used for recording.

The read film must have a lower coercivity than the write film so it will magnetize in conformance with the field written in the lower layer, and it should be optimized for a high light-beam rotation-angle difference between its two polarities of magnetization. For the gadolinium-iron-cobalt film used at NHK, reflectivity is 41% and rotation angle for the light beam's polarization plane is 0.5°. Topping the film with transparent materials having different indexes of refraction enhances the angle to 0.8°, but reflectivity is reduced to about 20%.

The read film should also have a high Curie temperature, because the rotation angle decreases to zero as the film temperature rises toward the Curie temperature. The Curie temperature of the read film can be higher than that of the write film because it does not affect the writing process. The writing laser beam strikes the read film and heat is conducted to the write layer below it.

The experimental system is designed to have a recording time of 10 min per 305-mm disk. This is quite ambitious, considering that it has to record a signal with a bit rate of 108 Mb/s. The solution was to spin the disks at the relatively high speed of 2,250 rpm and divide the signal among four sets of tracks, two sets each on two disks. This reduces the recording rate in each track to less than 30 Mb/s, which is close to the physical limits of the recording process.

Thanks in part to the reduced need for high-speed track accessing in the video system, NHK has been able to combine writing, reading, and erasing functions on the same head. Maximum access time is 0.5 s. Magneto-optic systems under development at Hitachi Ltd. and Sony Corp. split up the optical assemblies to reduce the mass of the parts that must move [*ElectronicsWeek*, Oct. 22, 1984, p. 17]. *–Charles L. Cohen*

HOW NHK STORES A TV SIGNAL FOR RANDOM ACCESS

A disk drive optimized for use in TV recording systems—where it may supply instant replays for sportscasts or speed up the editing process for news—does not require the superfast track-access times demanded of systems for on-line digital storage. But it does call for a very healthy throughput rate, compared with general-purpose digital systems, to write the digital representation of a high-bandwidth video signal in real time.

For its experimental magneto-optic disk drive, the Japanese broadcasting network NHK resorts to four heads writing on the surfaces of two disks to achieve the aggregate of 108 Mb/s. That figure corresponds to a standard sampling rate of 13.5 MHz used in broadcasting at a resolution of 8 bits.

NHK is using a format known as 3, 1, 0 to organize the digital storage of a color video signal on its disk system. The designation refers to the ratio between the standard sampling rate and those used for for luminance and color-difference signals.

The 3 is for the three quarters of the standard 13.5-MHz sampling rate—10.125 MHz—used to digitize the 4.2-MHz luminance signal. The 1 is for the one-quarter-rate sampling at 3.375 MHz used to digitize the two lower-resolution color-difference signals.

The color-difference signals (red minus yellow and blue minus yellow) are split up for storage with alternating lines of luminance data; the 0 in 3, 1, 0 represents the color signal omitted from each line. As stored on the disk, ¾ of each line is retimed luminance-signal data, and the other ¼ is devoted to one of the two alternating color-difference signals.

The bit rate of the digital signal stored on the NHK disks is only slightly higher than that of the digitized TV signal. The latter format uses far less space for formatting overhead than do data disks. *–C. L. C.*

INTERNATIONAL

ISRAEL AIDS AILING INDUSTRY

JERUSALEM

The Israeli government has decided to come to the rescue of the country's hard-pressed electronics industry. In mid-June, the cabinet of Prime Minister Shimon Peres approved a plan that allows the country's electronics companies to raise up to $50 million through bond issues on the Tel Aviv stock exchange for badly needed research and development, and to do so on favorable tax terms. Along with the R&D money, the government has earmarked $15 million for grants to bail out troubled companies and will provide several million dollars to promote exports.

The unprecedented government assistance to the Israeli electronics industry could not have come at a more opportune time. The industry is suffering from a drop in domestic and foreign demand, which has depleted profits for many industry leaders.

The Israeli electronics industry had been growing at an average annual rate of 20% in the past five years. Sales in 1985 reached the $2 billion mark, half of which was in the form of exports.

But the growth came to an abrupt halt last year. Yigal Ne'eman, managing director of Tadiran Ltd., Tel Aviv, Israel's largest electronics company, attributes the downturn to a combination of factors: a sharp cutback in orders from the Israeli Defense Ministry, a drop in government export incentives, price and dollar-exchange-rate freezes, a rise in wages and taxes, and a general recession abroad.

"In the past, Israel's electronics industry was in its infancy and was less affected by world trends," notes Uzia Galil, chairman of Elron Ltd., a leading Israeli electronics holding company. But, he adds, "in recent years we have developed an overseas market and have become dependent on world business cycles."

TO THE RESCUE. Peres's cabinet will aid troubled electronics firms.

Companies totally dependent on the civilian export market have been the hardest hit. Elscint Ltd., a Haifa manufacturer of medical imaging equipment, is in the midst of a restructuring [*Electronics*, March 24, 1986, p. 28]. The company was saved from bankruptcy earlier this year when the Israeli government stepped in and forced the banks to wipe out nearly $90 million in debt and pump new capital into the company.

The rescue followed a $33.7 million loss for the fiscal year ended March 31, 1985. Immediately after tallying that red ink, Elscint went on to lose $15.4 million in the first quarter of the current fiscal year.

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2000 — 20,000	84 — 266	1.4 ns	—	70 MHz	X	X	X	X	X
STANDARD CMOS ARRAYS WITH RAM									
2240	120	1.4 ns	2K	70 MHz	X	X	X	X	X
4440	180	1.4 ns	4K	70 MHz	X	X	X	X	X
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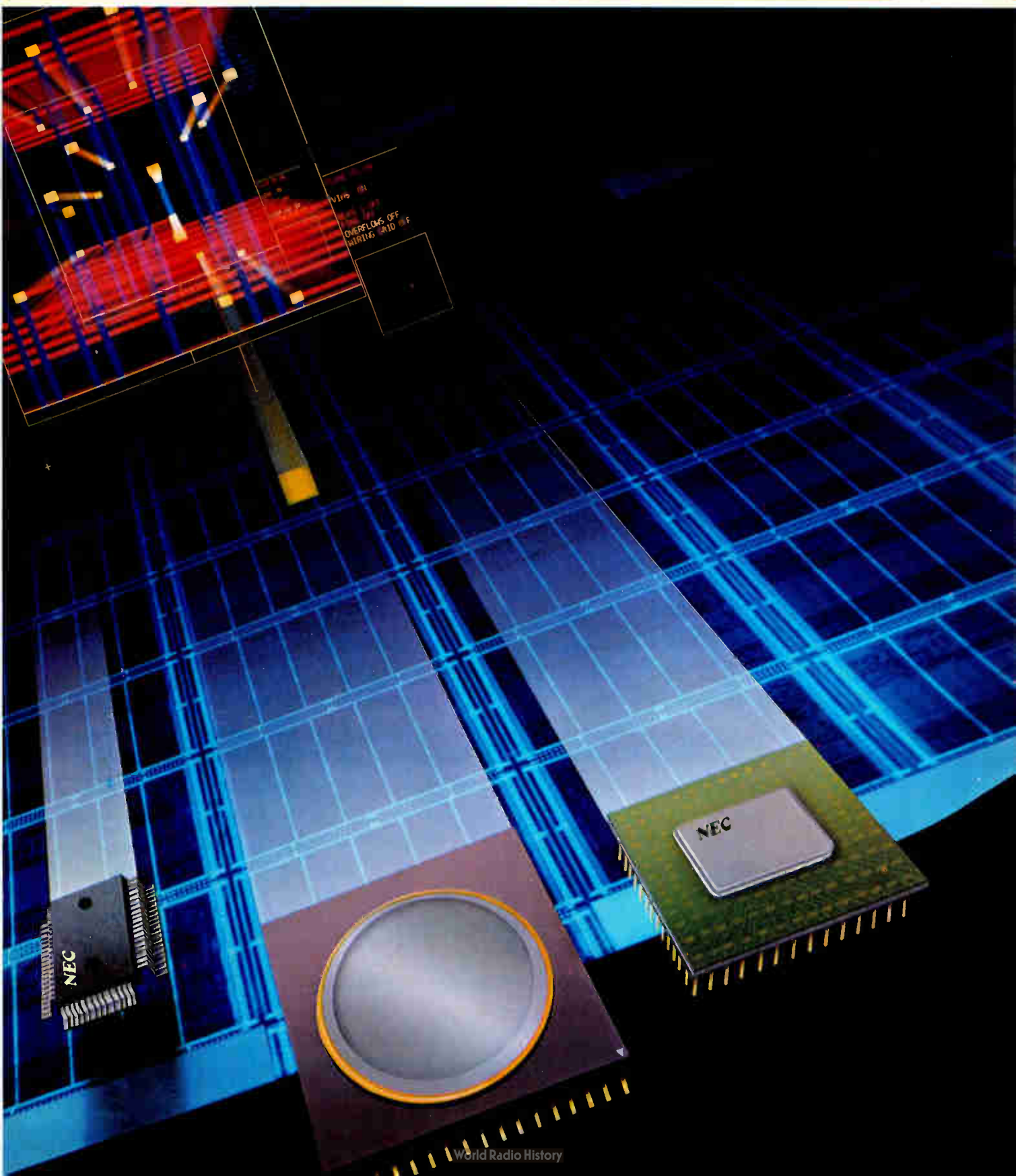

imaging systems used in printing, publishing, board assembly, and seismic exploration—has also reported huge losses. The Herzlia company lost $13 million in the first quarter of 1986, following a similar loss for all of 1985. Both Scitex and Elscint have substantially reduced their work forces and implemented other cost-cutting measures.

Other companies, such as Eci Telcom, Fibrionics, and Optrotech, whose shares are traded in the U. S. as well as in Tel Aviv, have reported losses or a sharp drop in profits. Tadiran has seen net profits drop from $46 million in 1984 to $28.3 million last year. Sales in 1985 were $571.5 million, a mere 3% above the previous year. The company's sales target for this year is $600 million. "At present, we do not expect any considerable growth," Ne'eman says.

There have been some exceptions to the general trend, most notably Elbit Computers Ltd. and Elta Electronics Industries. Both mainly produce military electronics and have long order backlogs that have protected them from the hard times.

SLOW RECOVERY. But the exceptions are few. Elron's Galil says 1986 will be a poor year for the Israeli electronics industry, with more staff dismissals. But he is looking for the industry to recover in 1987.

Galil expects the next boom to come from the huge budgets of the U. S. Strategic Defense Initiative (several Israeli institutions and companies are already taking part), a spurt in the development of software for personal computers, and advances in communications electronics. In the meantime, the government aid is expected to help the domestic industry continue its R&D and marketing efforts to permit future export growth once the market recovers. *–Neal Sandler*

AUTOMATION

AUTOSEQUENCER SPEEDS DECODING OF DNA CHAINS

FOSTER CITY, CALIF.

A bioinstrumentation company has automated a new technique, developed at the California Institute of Technology, Pasadena, for identifying DNA sequences with fluorescent dyes. Scheduled to be available in test sites by fall, the new sequencer can speed up the identification of DNA chains a thousandfold, its designers say.

The sequencer can help researchers find, for example, defects in a given DNA chain, and makes it possible to change the structure of a chain by changing its code. The technique was developed under Leroy Hood at Caltech, which has licensed Applied Biosystems Inc. to automate the process in a commercial instrument. The Caltech prototype can decode portions of a single chain of DNA (deoxyribonucleic acid), the genome that carries the pattern for genetic development. The Applied Biosystems instrument based on Caltech's technique can track up to 16 different sequences at once, says project director William Mordan.

DNA is composed of long chains of alternating sugars and phosphates, to which four types of purine bases—single and double carbon rings—are attached. The sequence of the bases, named adenine, cytosine, guanine, and thymine (A, C, G, and T), determines the molecule's characteristics.

Discovering that sequence is fundamental to DNA research. One method of choice, called dideoxy sequencing, entails painstakingly separating the chains in such a way that different sequences of bases result in chains of differing lengths, each ending in a specific base. Each base is then "labeled" with a different radioactive dye.

These lengths can then be identified by a process called electrophoresis: an electric field is applied to a gel in which the fragments are allowed to settle. Fragments of different lengths will fall at different rates, so the sequence can be decoded by laying film across the gel and observing where the dyes mark the film, indicating how far the fragments travel in a given interval.

Because the Caltech method uses fluorescence instead of radioactivity to label bases, the chains can be read and decoded in real time. (Film exposed to the radioactivity used in dyes, which is kept weak to provide greater resolution, can take two days to develop.)

The dyes Caltech uses show emission peaks between 540 and 600 nm when excited by an argon laser. Each peak, in green, green-yellow, orange-red, or red, is associated with a particular base—A, C, G, or T.

A photomultiplier tube is needed to collect the light, because each base has only one molecule that picks up the fluorescent dye. The tube is part of the Applied Biosystems instrument's scanner, along with a laser and a Z80 microprocessor for control of the voltage, current, power, and temperature parameters affecting electrophoresis. Scanner data is transmitted to an IBM Corp. Personal Computer AT for analysis.

Where Caltech built its fluorescent prototype to operate on a single tube of gel, Applied Biosystems reverted to conventional dideoxy methods of putting the gel between two glass plates, 40 cm on a side, and applying several electric fields across the plates. This process allows multiuple DNA chains to be sequenced.

The instrument, which will cost slightly less than $90,000, will read as many DNA sequences in a day as a trained technician can now do in a year. But even at that rate, DNA still has a few secrets to keep. A human genome is about 2×10^9 molecules long, notes Mordan. To sequence one such chain, even with the automated instrument, would take 10 years. *–Clifford Barney*

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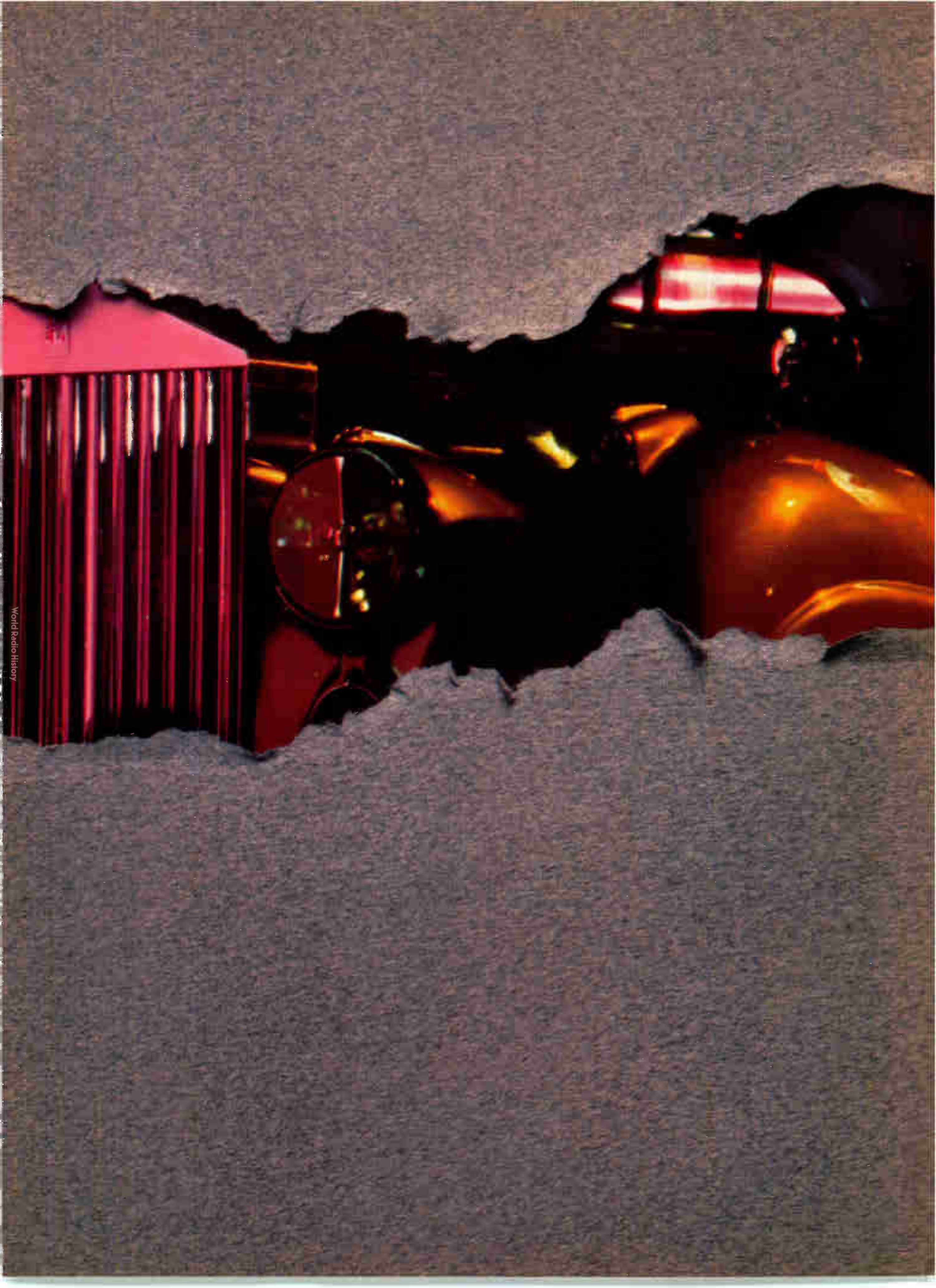

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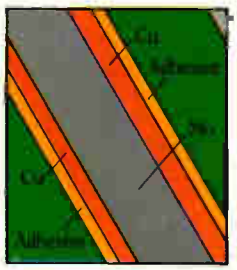
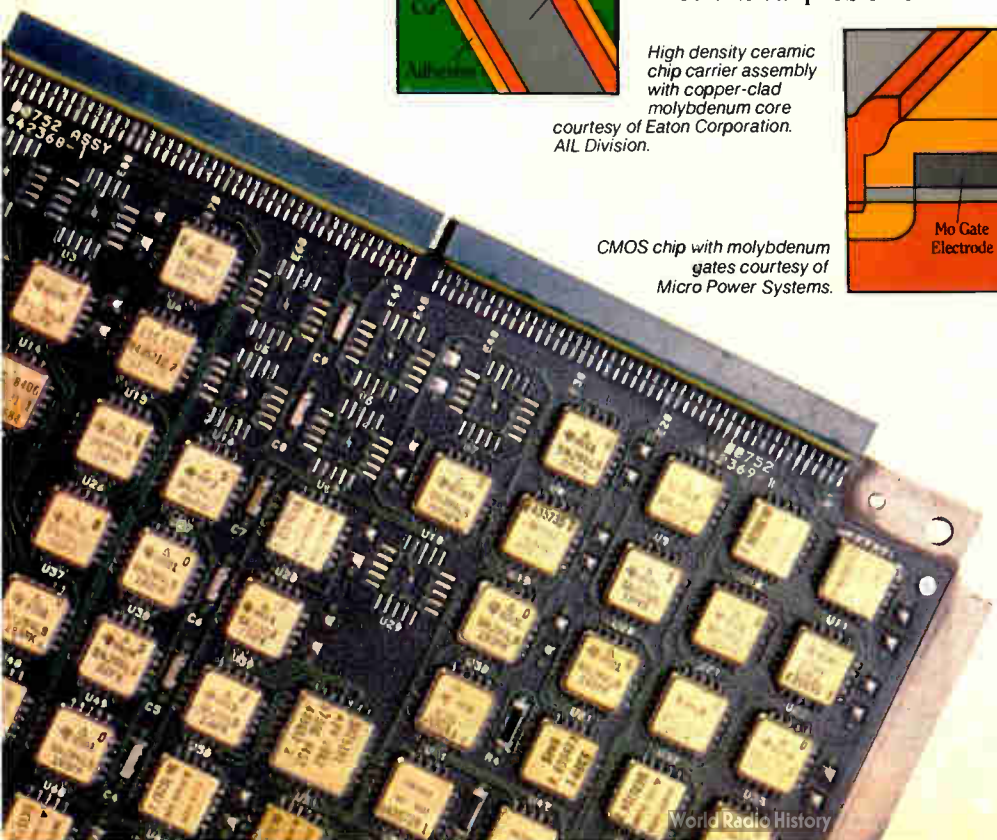


High density ceramic chip carrier assembly with copper-clad molybdenum core courtesy of Eaton Corporation. AIL Division.



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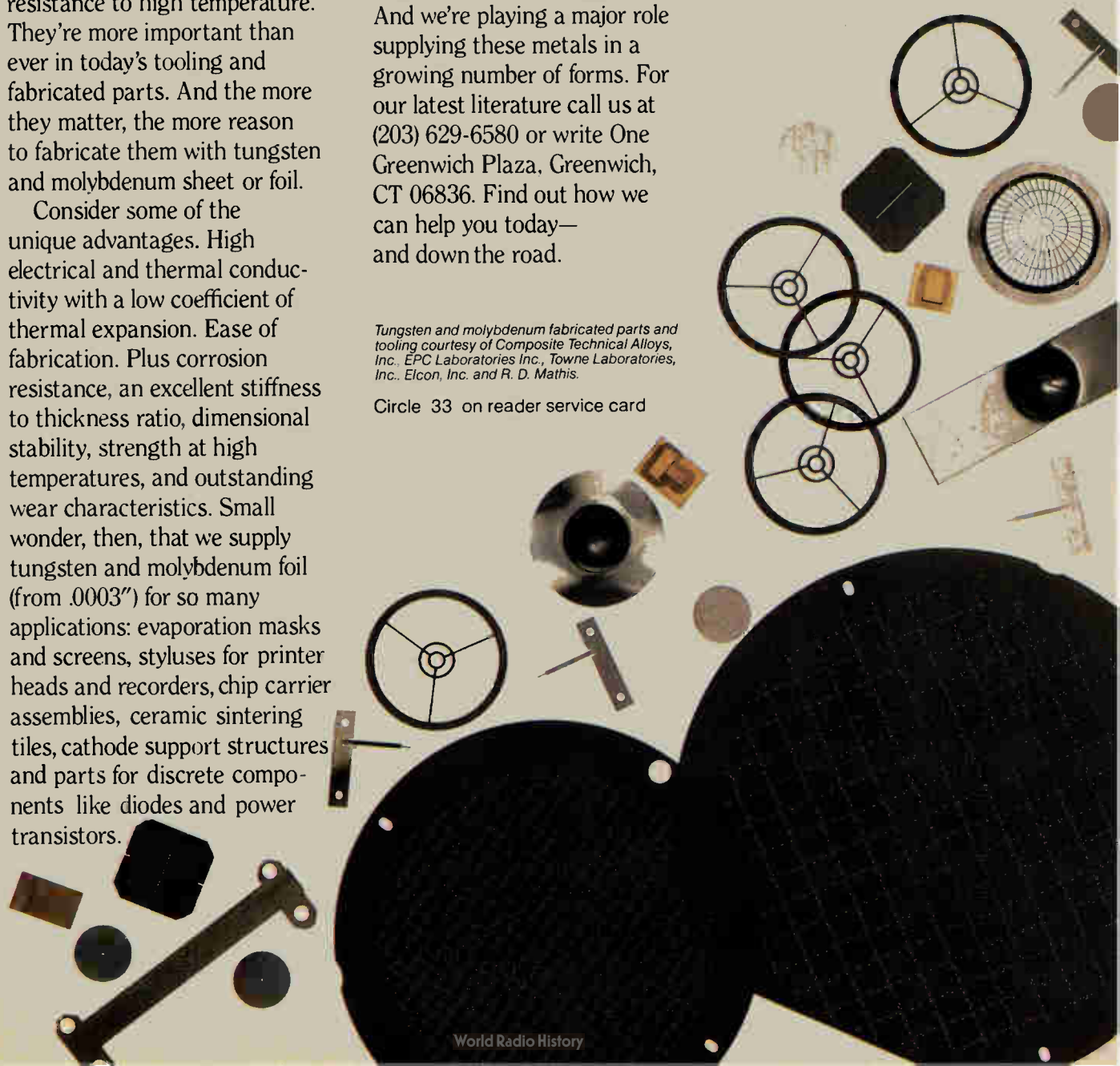
Tungsten and molybdenum fabricated parts and tooling courtesy of Composite Technical Alloys, Inc., EPC Laboratories Inc., Towne Laboratories, Inc., Elcon, Inc. and R. D. Mathis.

Circle 33 on reader service card



INSIDE TECHNOLOGY

STRETCHING THE LIMITS OF ASIC SOFTWARE

DESIGNERS NEED BETTER TOOLS TO BUILD GIANT ASICs

by Bernard Conrad Cole

Users and manufacturers of application-specific integrated circuits are worried that the ability to make very large, high-density chips will outstrip the tools to design them. Densities are already climbing beyond 50,000 gates, they say, and the current generation of design tools is hard pressed by this level of complexity.

But relief is on the way, with development accelerating on such key types of design tools as automatic placers and routers; advanced simulation and test tools; module generators, also called block or megacell compilers; and automatic generators of functional models. Also important will be artificial-intelligence-based "heuristic programming environments" such as rule-based expert systems, says James E. Solomon, founder, president, and chief executive officer of SDA Systems Inc., Santa Clara, Calif. "AI is the glue that will tie all these disparate functions together," he says. Already working is an AI tool that performs hierarchical layout extraction.

From densities of about 10,000 to 15,000 gates using 3-μm CMOS processes, standard-cell and gate-array manufacturers are now moving into volume production of 2-μm semicustom arrays of 25,000 to 50,000 gates. Some vendors, such as LSI Logic Corp., Milpitas, Calif., have moved to 1.5-μm double-level metal processes, which when combined with compacted, or sea of gates, array structures [*Electronics*, July 22, 1985. p. 41] yield densities as high as 125,000 to 150,000 gates (Fig. 1). But the move to 1 μm and smaller geometries will bring the most significant density increases, yielding anywhere from 250,000 to 500,000 gates, says Solomon.

Such densities promise true systems on a chip—not just the equivalent of a single printed-circuit board of large-scale integrated circuits, but of several boards. But they also bring tremendous problems. "It is not unusual today to hear of a 100,000-transistor [25,000- to 50,000-gate] very large-scale-integration design that took 50 to 100 man-years to complete," says Solomon.

If nothing is done to change current design methodologies, ultralarge-scale circuits will multiply design time at least tenfold, taking us "into the 1,000-man-year realm," he says. Design tools are becoming available from ASIC vendors of standard cells, and gate arrays are starting to cut design times in half or by a fifth, but improvements of several orders of magnitude will be required as chip densities approach ultra-large scale, says Solomon.

So it should come as no surprise that the ASIC industry is expending a tremendous amount of manpower and dollars to develop the appropriate design-automation software, says Andrew Prophet, an industry analyst at market researcher Dataquest Inc., San Jose, Calif. In general, he says, most of the research and development dollars at the major ASIC houses go toward software development. "Compared to what is being expended on process development, most companies are expending at least as much on software development," he says. "At some companies the ratio is 5 to 1 and even 10 to 1 in favor of software development."

From the industry side, it's a matter of life and death. "The ASIC vendor who does not put as much effort into developing its software capability as into developing processes to support semicustom products will not survive," says Andrew Haines, strategic marketing manager for application-specific products at VLSI Technology Inc., Milpitas, Calif. Bernard Rosenthal, manager of computer-aided-design products at San Diego-based bipolar gate-array manufacturer Advanced Micro Circuits Corp., puts it this way: "Building a semicustom capability without expending as much effort on software tools as on hardware and process is like buying an automobile but spending nothing on fuel," he says. "Process and hardware are the engine and vehicle. Design software is the fuel."

IMPROVING GATE UTILIZATION

As ICs grow larger, more real estate must be devoted to interconnection wiring at the expense of the area used for active gates. Gate utilization can be as high as 70% to 90% for small circuits. But in VLSI, gate utilization drops to as little as 20% to 30%. In more advanced 125,000- to 150,000-gate arrays, for example, no more than 50,000 are available for chip design [*Electronics*, May 19, 1986, p. 17].

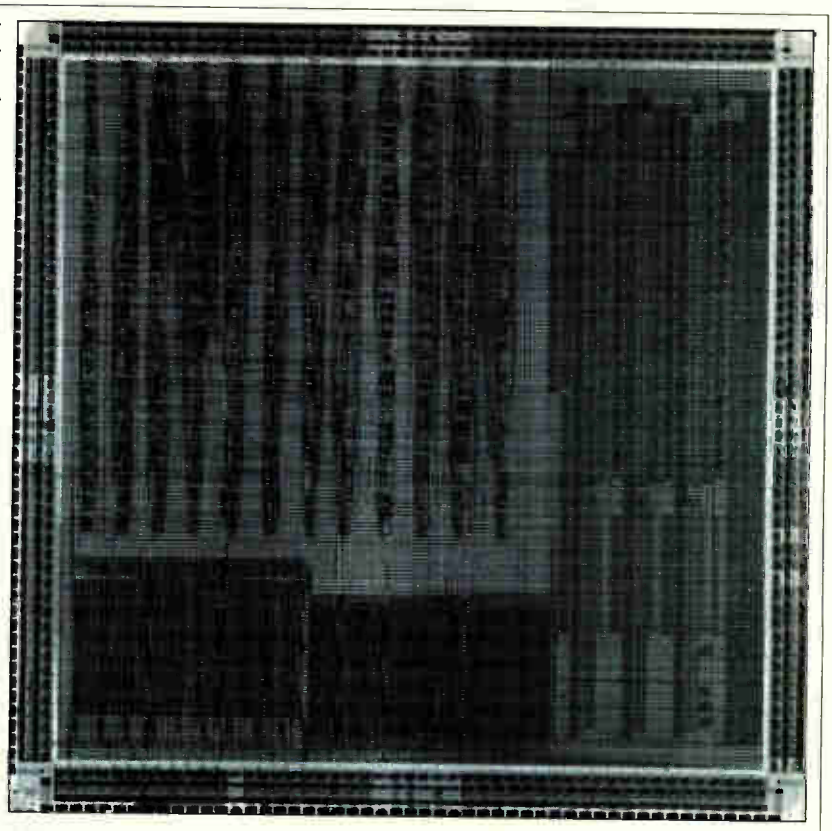
The problem has been further complicated by the megacell and macro-module design methodologies that have evolved to allow design at such high levels of integration. As larger cells are interspersed with smaller ones, longer interconnection paths are required to route signals around them, leading to off-balanced designs—some areas of a chip are sparsely populated by interconnections and others are overly dense. To

improve gate utilization, ASIC vendors are looking to develop more efficient automatic placement and routing programs.

Two such interactive placement systems for gate-array designs were developed at General Electric Co.'s Semiconductor Business Division, Research Triangle Park, N. C. One, called the Hierarchical Interactive Computer Aided Placement (Hicap) program, optimizes initial placement and the second, called ICmove (Interactive Component Movement), iteratively improves the routability of the placement. So far, the tools have been used in placing and routing of more than 30 production gate arrays.

Hicap is a menu-driven, hierarchically structured program in which the basic unit is the module, a basic circuit function that comprises lower-level modules of decreasing size and functional purpose. The first step in using this program is to define the basic circuit function, assign it a module, and then define the submodules. Input to the program can be done using the Tegas Design Language, available on many schematic-capture systems.

The user begins placement by selecting a module name from a menu of all modules in the design. Once a module is selected, Hicap downloads a menu of its submodules and the signals connecting them to the terminal. Hicap calculates the number of inverter equivalents used by the modules. With this information, the user defines a rectangular placement template for the module. The submodules are placed by picking them from a menu and placing their outlines on the module's placement template.



1. VLSI ASIC. LSI Logic's LCA10,000 compacted array combines 1.5-μm CMOS process and channelless structure to achieve 125,000 gates.

When all modules have been placed, Hicap flattens out the design for manipulation by ICmove; that is, the modules are expanded to the submodule or component level. ICmove works interactively with the portion of the design that is not amenable to placement with Hicap, rearranging the design to achieve a chip utilization as close to 100% as possible.

To do this, ICmove allows the user to experiment with the locations of components or submodules within a module by shifting them with a window-move command. The program then analyzes the new arrangement and compares the results to a set of predetermined figures of merit, such as lengths of expected connections and measures of acceptable or unacceptable congestion. If the move is not accepted, the component automatically snaps back to its original position.

ICmove uses several techniques to analyze how efficiently a circuit has been routed. One of the most useful is the figure-of-merit display, which graphs experimental moves side-by-side. Figures of merit are arranged by number, so the best move can be spotted instantly. In addition, a force-vector display indicates where each component should be placed to minimize the forces acting on it. There is also a component-connectivity display that shows the connectedness of the circuit. A congestion display draws in red regions predicted to have dense wiring, those with few wires in blue, and in-between areas with a spectrum of colors. In most cases, the combination of these two programs assures virtually 100% utilization of chip real estate for arrays up to 13,500 gates. Above that, utilization declines somewhat but still remains between 90% and 100%.

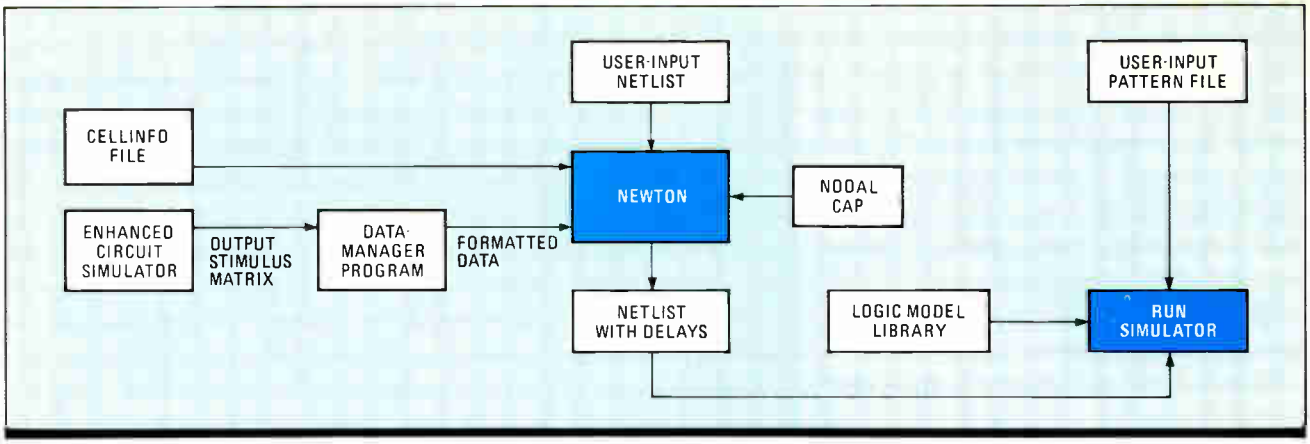
Addressing the same problem in standard-cell designs, engineers at Daisy Systems Corp., Mountain View, Calif., have developed a gridless channel-routing and compaction algorithm that cuts the area channels require by as much as 20%. Applicable to any cell-based IC design using blocks of arbitrary size and shape, this algorithm has been designed to derive channels for an arbitrary floor plan.

The key is the use of a routing scheme in which the interconnections are not compacted with reference to a predetermined grid but to lines on each wiring layer that are similar to the contour lines on a map. Reductions in the routing area range from 10% to 20%. Another advantage is that a customized floor plan using such contoured channels reduces wasted space when an IC is designed with irregularly sized blocks, as often occurs in current approaches.

UNIVERSITY WORK

Efficient gate utilization and ease of use are both important in standard-cell placement and routing software, and just such a combination is found in a package called ThunderBird, which is getting a lot of attention from many companies. Developed at the department of electrical engineering and computer science of the University of California at Berkeley, ThunderBird consists of four basic programs: Flounder, for netlist and cell-data extraction; Timberwolf, for placement and global routing; YACR (for "yet another channel router"); and Termite, for postprocessing and physical routing. Data generated by these programs is coordinated and manipulated using Squid, a CAD data-base-management program.

To begin placement and routing, Flounder extracts the netlist and physical cell data from Squid's library of standard-cell layouts. Timberwolf then goes to work, using these files as input. When finished, Timberwolf invokes Termite, providing it with the files it has produced as input. Termite creates a hierarchical layout description of the chip using placement information contained in the input files. Referring to the standard-cell library to obtain cell layouts, Termite then generates the descriptions of the channels to be routed, repeatedly executing YACR to obtain the routed channels in symbolic form. For each channel, it generates the physical wiring according to user-specified design rules and places the routing in the layout. The blocks of cells are then compacted or expanded as



2. COMBO. National Semiconductor's Newton program combines logic simulation's speed and ease of use with device simulation's accuracy.

necessary so that the channels are as narrow as possible.

ThunderBird handles circuit configurations in which the standard cells, including those of differing heights, are arranged in horizontal rows, and it allows up to 11 functional macroblocks per chip. Results on a variety of circuits, compared with those attained with many types of available automatic and manual layout methods, indicate that ThunderBird yields area savings ranging from 15% to 75%.

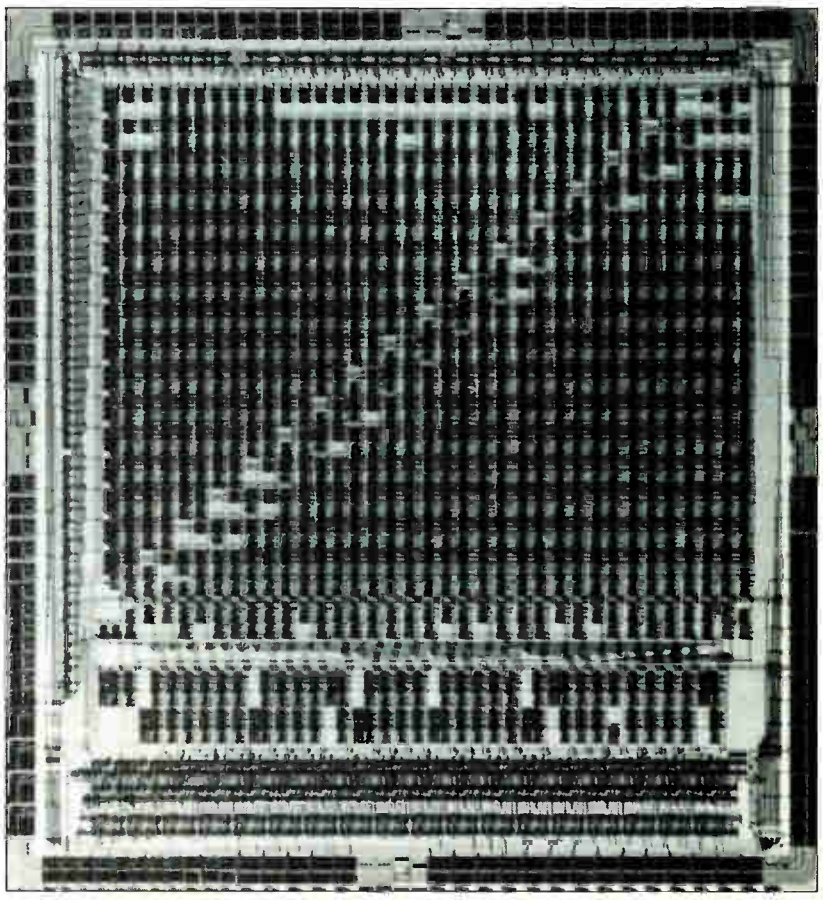
But even before placement and routing enter the picture, designers must verify the performance of complex designs. The timing considerations associated with integrating system-level functions on an IC require accurate circuit performance prediction, especially in the semicustom environment, says National Semiconductor Corp. design engineer Amrish Patel. A high degree of accuracy is necessary to avoid the yield loss experienced when circuits do not match the performance predicted by the simulation.

CAD tools use either device- or gate-level simulation to verify performance. Although desirable for their 95% to 99% accuracy, device-level simulators take an inordinate amount of computer time for an entire design and are therefore usually restricted to critical paths within a chip. And even then, critical paths are not always predictable. Also, their complexity makes these simulators extremely difficult to use by designers not familiar with IC design at the device level.

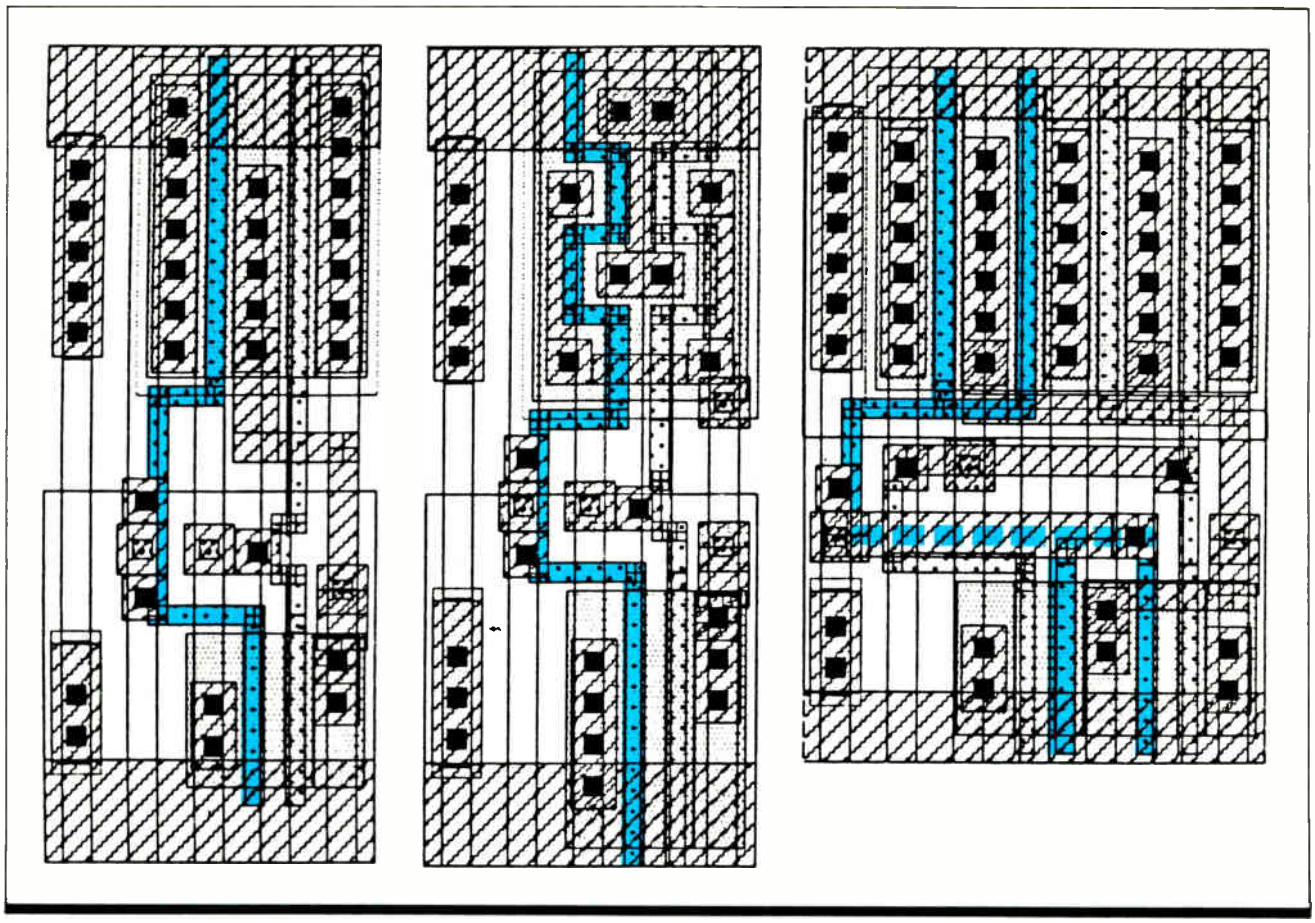
Gate-level simulators are easier to use and take less computing time. However, their accuracy depends on the delay data passed to them and the logic models used in the library. Most of these simulators assume fixed rise and fall times, simulated gate delays that are independent of the specific inputs, and considerably simplified methods of calculating delays—all of which degrade accuracy. As a result, gate-level simulators are typically one-fifth to half as accurate as device-level simulators.

To overcome this problem, National's standard-cell library incorporates Newton, a unique gate-level timing-analysis and circuit-simulation program that predicts delay data with an accuracy of 95% to 99%, compared with the usual 20% to 50%, and at a fraction of the computer run time of device-level simulation. The fully automated simulation program achieves its near device-level accuracy by incorporating logic models that reflect actual circuit operational properties, says Neil Birns, standard-cell design engineering section head. The logic models include multiple paths within a gate. In addition, delays are associated with input signals as opposed to gates. Moreover, Newton calculates delay as a function of varying rise and fall times, gain, and output loading.

In this program (Fig. 2), an existing circuit simulator has been modified to generate an output-stimulus matrix that is automatically collected, formatted, and stored by a data-base manager. Specific macrocell information, the required number of delays, and the input and output pin order are stored in a Cellinfo file, which can handle such large functional blocks as counters and decoders. For a given user input netlist, Newton calculates rise and fall times on nodes and consequently calculates delays using the output stimulus matrices, Cellinfo files, and nodal capacitances derived from place-and-route and mask-parameter extraction programs and other sources.



3. MODULAR DESIGN. LSI Logic built a 32-bit multiplier-accumulator—the L64032—using Macgen, the first in a family of megacell compilers.



4. FAST DESIGN. Gould AMI's Score developes prototypes very quickly, so designers can generate many versions and choose the best.

In addition, Newton automatically decomposes cell hierarchy, if present in the Cellinfo file, and calculates the delays on the flattened netlist. The accuracy of the calculated delays is further enhanced by the use of seven fast, sophisticated algorithms, one of which is automatically selected as the best fit for a given macrocell's output-stimulus matrix.

Use of the program under various loading conditions has yielded results remarkably close to those achieved with a device-level simulator, says Birns—in one case a delay of 10.692 ns compared with 10.60 ns for a device-simulation program, and in another 10.59 ns compared with 10.39 ns. "In general, we have been able to predict delays within an accuracy of 95% to 99% at a fraction of the CPU run time required for device-level simulation," he says.

GOING MODULAR

ASIC manufacturers have been forced to develop methodologies that use larger and larger building blocks to deal with the growing density of semicustom circuits—particularly those based on standard cells. Although this has speeded up and simplified design, it has in a sense made the methodology less flexible and therefore less application-specific, says Robert Kirk, CAD research manager at Gould Semiconductor in Twain Harte, Calif. "As we have moved to larger and larger blocks, we have given up some of the design flexibility available at lower levels in exchange for being able to design faster and easier at ever higher densities," he says.

To retain the advantages of the megacell and cell-library approach, but at the same time win back flexibility and application specificity, ASIC manufacturers are investigating approaches that will also allow them to design at much higher integration levels with even shorter turnaround times.

LSI Logic Corp. takes a very straightforward approach to the problem. The Milpitas company is developing a series of megacell generators that allow the user to optimize particular megacell-type building blocks to his requirements. "In addition to making the design of high-density circuits even easier, this methodology speeds up the design of certain types of functions by as much as 10 times over conventional approaches," says Rick Rasmussen, advanced product development manager.

Where silicon compilers are used to design general-purpose circuits, he says, each of the megacell compilers being planned by LSI Logic will incorporate a set of algorithms whose only function is to generate, optimize, layout, and automatically route a particular megacell function, such as an arithmetic logic unit, based on parameters for a particular application. Depending on the type of function and the level of integration, a megacell compiler can compile a circuit function, fine-tune it for speed, area, or both, and then generate its software representation in only 48 hours.

The first in this family of megacell compilers, called Macgen, works in conjunction with the company's LDS design system to generate complex VLSI functions such as high-speed multipliers, multiplier-accumulators, and adders as either stand-alone ICs or as building blocks in more complex circuits. The resulting customized megacells are not only designed faster, they are usually faster and smaller than comparable circuits developed with conventional standard-cell design methods, says Rasmussen. For example, a 16-bit multiplier-accumulator designed with Macgen is about 2.5 times smaller than an equivalent standard-cell device. And using the company's 1.5- or 2-μm CHMOS processes, Macgen can generate complex blocks such as 16- to 32-bit multipliers with typical execution times of about 40 to 70 ns—directly competitive with bipolar versions, but at much lower power.

Using Macgen, he says, company engineers have generat-

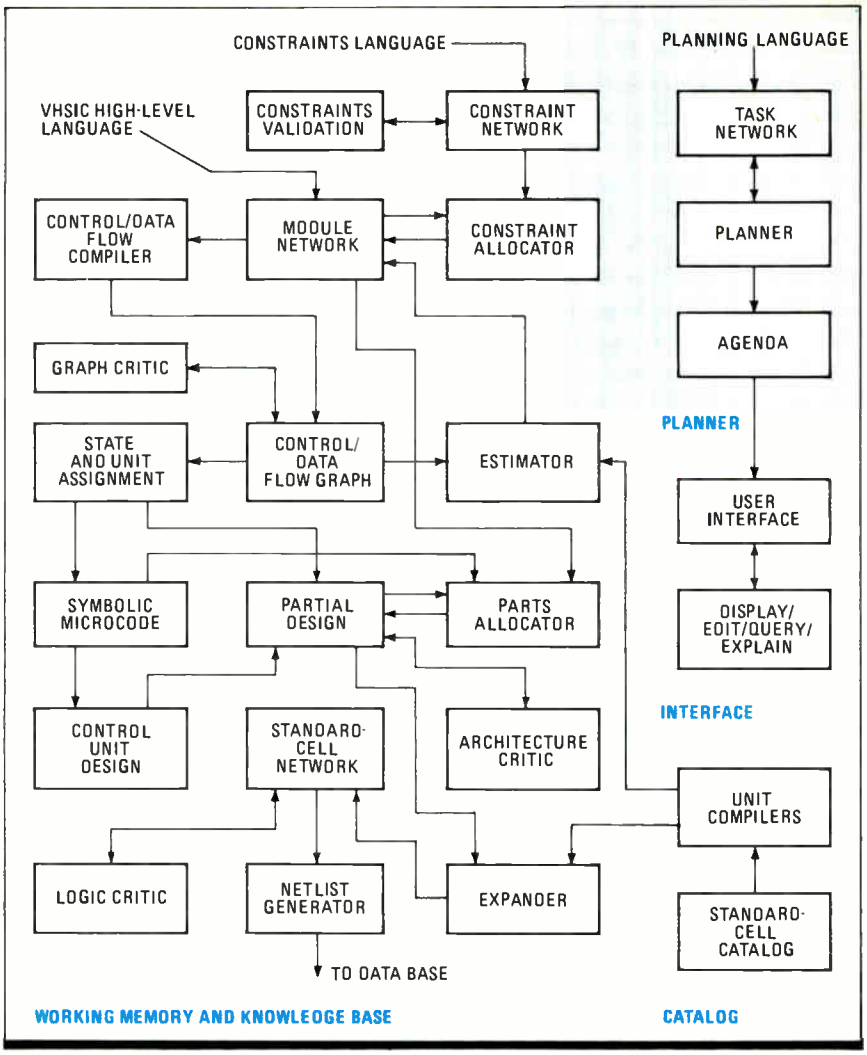
ed a 32-bit multiplier-accumulator (Fig. 3) called the L64032. It uses LSI Logic's 1.5-μm HCMOS process and does 12.5 million 10-digit mathematical calculations per second.

Perhaps the most ambitious effort in restoring flexibility is Score, an AI-based cell-library development system from Gould-AMI Semiconductor. What makes Score unique is that it compiles whole families of standard cells to a customer's requirements and then generates complete circuit layouts as well as all of the appropriate documentation and data-base descriptions, says Kirk.

Score can create cells with unique characteristics because the cell's simulation model and mask layout are not prestored in a data-base library, as is usually done for standard-cell circuits and gate arrays. Rather, says Kirk, customers provide specifications for cell construction, such as propagation delay, load, cell height, function, functional options, and process parameters.

These inputs then drive procedures in the system's cell-compiler software to generate a new cell. Score automatically determines the proper gate sizes for the cell by analyzing input data and calculating the transistor sizes required. Next, Score combines that data with the prescribed cell height and generates the finished layout and simulation model.

Cell layout can be reworked in minutes by changing parameters and reexecuting the cell-generator program. "Because the system is process-independent, cells can be made from 3 μm down to submicron geometries," says Kirk. "With Score, cell-based custom designs are no longer limited to a IC vendor's library. Rather, Gould engineers can offer systems manufacturers the capability to build entirely new cells in a fast, efficient manner. In addition, Score enables us to break the barrier between standard-cell and cell-based structured custom development times by creating cells 10 times faster than conventional approaches."



5. AI AT WORK. Aimed at prototyping and updating parts, the Descart intelligent silicon compiler comprises memory, knowledge base, Planner, Catalog, and interface.

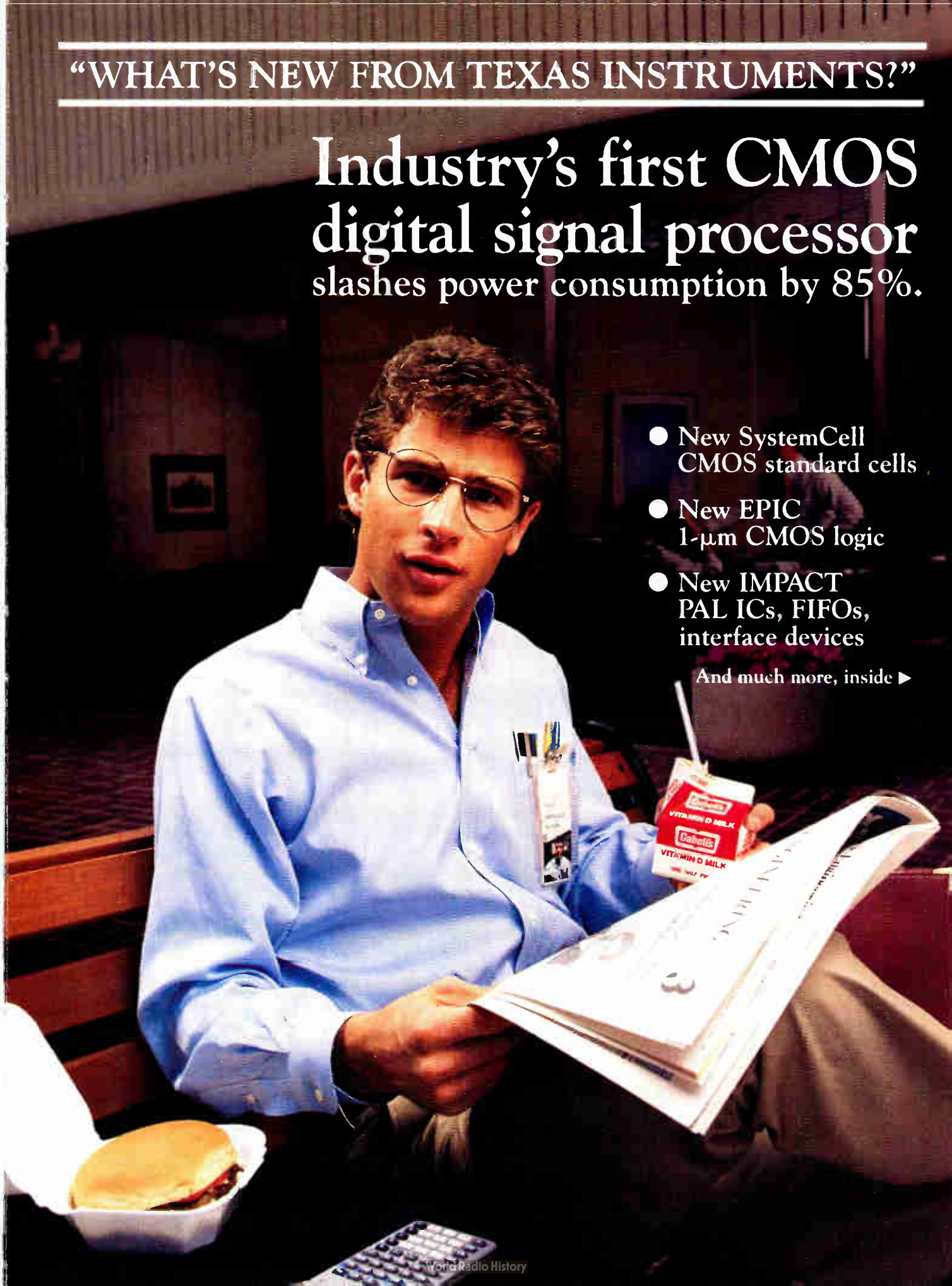
SPECIAL CAPABILITIES

Kirk claims that Score can create layouts that rival hand-crafted designs, thanks to two special capabilities. For one thing, rather than increasing cell height to accommodate transistor sizes, as is conventionally done, Score maintains the prescribed height and changes only cell width. The system then modifies the cell's transistor gates automatically to create what are called bent-gate or split-gate transistors (Fig. 4). Without this technique, says Kirk, cell heights within a row would have to be irregular. Second, Score automatically calculates an optimum height for all cells in each row. The result is that each row has a uniform height, but cell heights may vary from row to row. Key to Score's flexibility and power is the use of a variety of AI techniques based on the high-level Lisp language. Using such techniques, a circuit is constructed with Score using spatial-relationship reasoning to achieve the most cost-effective layout.

AI also comes to the fore in Descart (Fig. 5), an expert silicon compiler under joint development by Gould-AMI in Santa Clara, Gould Research Laboratory in Rolling Hills, Ill., and the U.S. Army's Electronic Technology and Device Laboratory in Fort Monmouth, N.J. Aimed at rapid prototyping as well as at redesigning old parts to make use of more advanced process technology, Descart accepts a chip's behavioral description in a high-level language, modified by the constraints imposed by the designer and the design strategy, and generates a standard-cell representation in terms of a netlist.

Descart consists of five modules: working memory, which contains a partial design that is refined during the design process; the knowledge base, which contains the rule set by which translations and optimizations are performed; Planner, which determines the order in which various design tasks are to be performed based on the status of the design and the designer's strategy; Catalog, which contains a set of unit compilers that translate each functional unit into a network of standard gates; and the interface, a window- and menu-oriented program that serves for entering design specifications, displaying and editing partial designs, and for acquisition of new design knowledge.

The translation process proceeds in two phases—microarchitecture generation and functional unit generation. During microarchitecture generation, Descart makes area and time estimates of each storage element and functional unit, makes tradeoffs based on its stored base of expert knowledge, and optimizes the design according to the design plan. Once the microarchitectural design is completed, says Kirk, Descart uses a set of functional unit compilers to obtain a standard-cell representation for each unit. □



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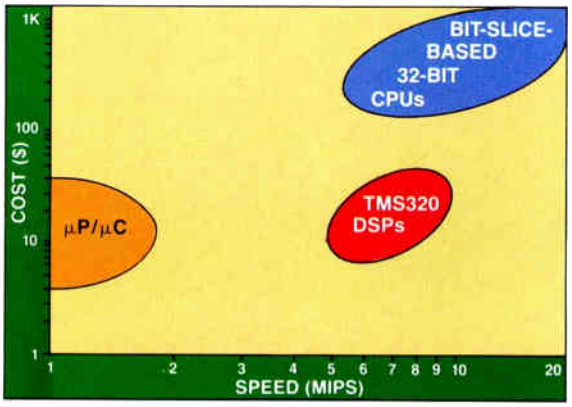

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TI's IMPACT FIFOs: 50% faster than any others.

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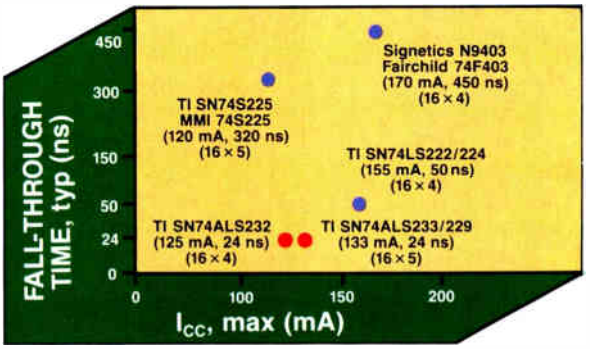
The SN75ALS232/233/229 asynchronous FIFOs feature dual-port-RAM architecture, so there are no ripple-through delays, no address generation required. Their 0- to 30-MHz speed gives you increased system throughput for long data streams. Full/empty status flags may be used as clock-enable signals to control asynchronous timing.

TI's IMPACT FIFOs SET THE PERFORMANCE PACE



New industry leaders: TI's IMPACT FIFOs offer a 50% improvement in fall-through time.

4

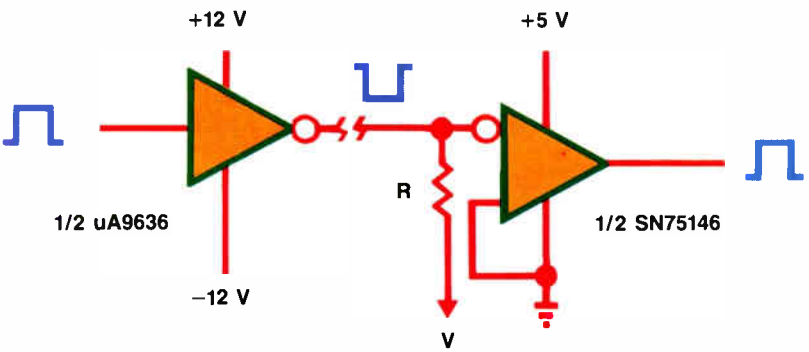
High-speed, low-power IMPACT line drivers and receivers.

Now Texas Instruments utilizes the IMPACT process for the first time in line-interface devices. For high speed and low power.

TI's SN75ALS126 quadruple line driver, designed to meet IBM 360/370 specifications, provides for faster switching with lower power dissipation than the SN75126 and MC3481 drivers for which they are direct replacements.

A new dual differential line receiver, SN75146, is compatible with either single-ended or differential-line systems, to meet both RS-422-A and RS-423-A EIA Standards. With one external resistor, it also meets the requirements of RS-232-C *(see diagram)*. Similar to the uA9639, TI's SN75146 includes additional input filtering, making it ideal for noise-sensitive single-ended applications.

RS-232-C SYSTEM APPLICATIONS, SN75146



Unique new TI line receiver meets RS-422-A and RS-423-A standards. And with a single external resistor (R) it also satisfies the requirements of EIA Standard RS-232-C.

5

High-speed signal conditioners for wide-bandwidth applications.

For compatibility with digital processors, signals from magnetic mass memories and video imaging arrays must be amplified and shaped by circuits capable of very high data rates. Now Texas Instruments introduces five such circuits: Three differential video amplifiers and two differential comparators.

The TL592B is a low-noise, high-gain amplifier with a 50-MHz bandwidth and only 3 μV of broad-band noise. For applications that require automatic gain control, the TL026 and TL027 amplifiers offer a selection of peak gains with 50-MHz bandwidth and 50 dB of AGC.

And TI's new TL712 and TL721 high-speed comparators provide the signal shaping necessary for compatibility with TTL or ECL logic circuits, with propagation delays that can be less than 12 ns.

TYPICAL SIGNAL-CONDITIONING APPLICATION

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1-μm EPIC process enhances TI's CMOS logic circuits.

Enhanced Performance Implanted CMOS (EPIC™) logic, a unique development of Texas Instruments, will bring to silicon-gate CMOS logic the speed of FAST™ high-speed advanced bipolar devices — and 24-mA sink/source current — while retaining the inherently low power characteristics of the CMOS process.

The 1-μm EPIC process is a direct outgrowth of TI's 1-Mb DRAM technology. In fact, the cell design of TI's 1-Mb DRAM was itself strongly influenced by the desire to devise a technology equally applicable to the fabrication flow of high-performance logic.

The outcome is a universal 1-μm flow in which the steps for making DRAM-cell capacitors can be easily skipped when processing logic ICs. This unifying technology is helping TI to respond quickly, sensitively — and economically — to your changing needs.

EPIC products optimized for high quality and reliability

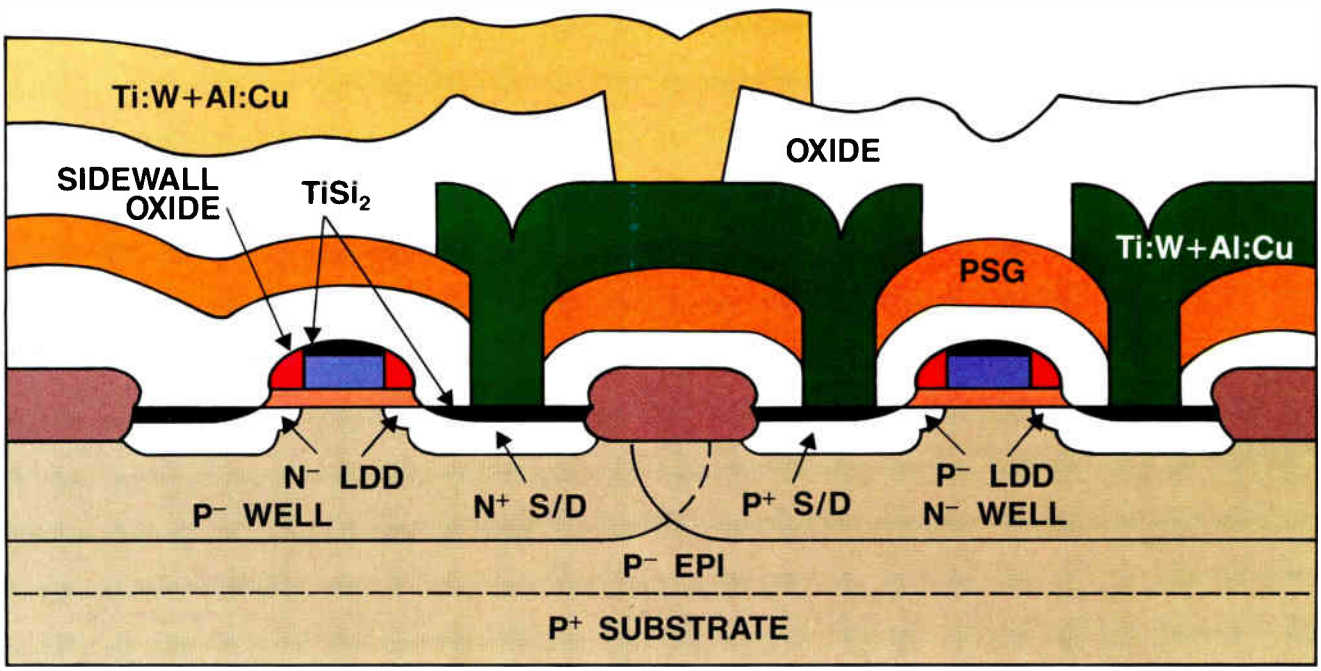
Fundamental physical limitations become critical in the design and fabrication of structures as small as 1 μm: Quantum-mechanical tunneling through thin oxides. High-intensity fields due to hot-electron effects. Latch-up in high-density CMOS circuits. All have been brought under effective control by TI's new 1-μm EPIC design.

Among the features that contribute to optimal reliability in TI's new EPIC CMOS devices: Input and output structures that protect against electrostatic discharge up to ±6 kV, well above the ±2 kV specified by MIL-STD-883. Copper-doped aluminum metal improves reliability by effectively preventing electromigration. The process also features an epitaxial substrate layer for outstanding latch-up suppression (*see diagram*).

A broad family of devices soon to come

With the perfection of TI's 1-μm EPIC processing, a whole new family of advanced CMOS logic (ACL) devices is on the horizon. It is expected to include SSI and simple and complex MSI parts. The 1-μm gate lengths in EPIC devices will permit average propagation delays of less than 3 ns, with subnanosecond internal-gate performance.

Watch for introductions of TI's high-speed EPIC ACL devices. They're coming soon.

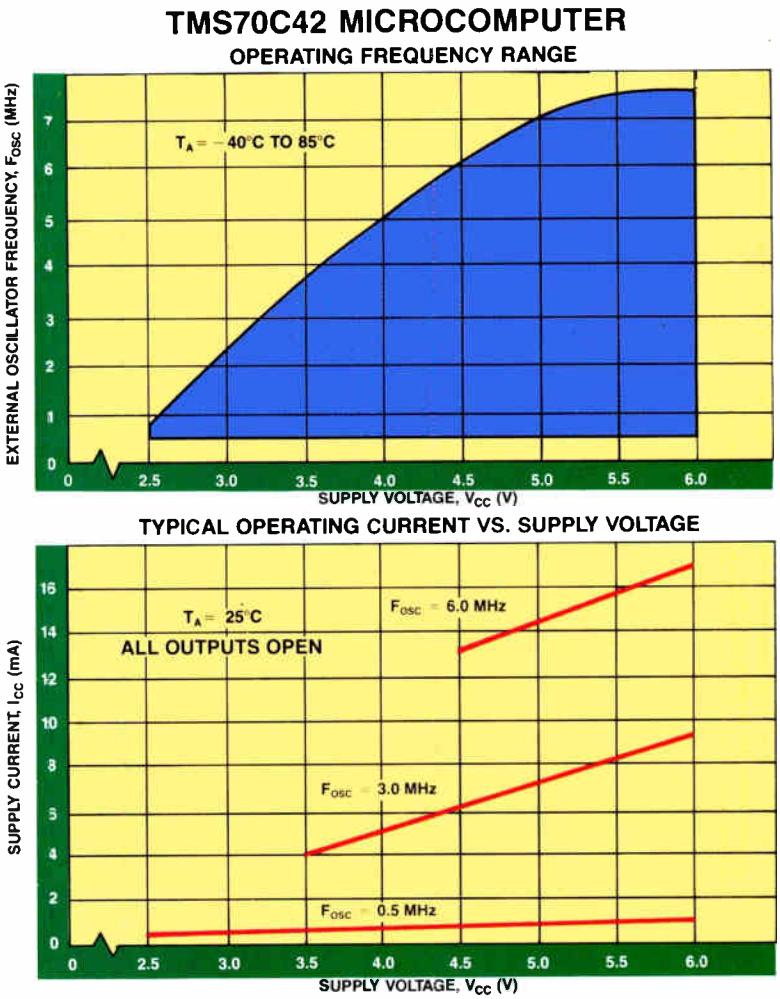


Superior switching time and 24-mA output drive are achieved in TI's new ACL family through 1-μm EPIC CMOS technology. The process is an outgrowth of the CMOS technology developed by TI to support its 1-Mb DRAM.

5 more new routes to high perfo

Texas Instruments continues to develop cost-effective circuits — denser, faster — with lower power requirements and increased functionality. Among TI's latest advances are a new CMOS microcomputer and new A/D converters and high-speed signal conditioners.

And TI's exclusive IMPACT™ (Implanted Advanced Composed Technology) process is the basis for powerful new FIFOs, PAL® ICs, and interface devices.



1

New CMOS microcomputer helps cut system costs.

TI's TMS70C42 CMOS 8-bit microcomputer is designed to help lower your system costs across a broad spectrum of realtime control applications and a wide range of operating characteristics *(see graphs)*. Both the TMS70C42, with its 4K bytes of on-board ROM and 256 bytes of RAM, and its ROM-less TMS70C02 counterpart have features designed to reduce system cost: Two high-resolution 16-bit timers with 5-bit prescale and pulse-width-modulation output. Fully programmable interrupt enable and interface. Integrated hardware UART with baud-rate generator.

And to help get your product to market quickly and economically, these extremely flexible devices are supported by an extensive array of inexpensive development tools.

2

IMPACT PAL ICs are world's fastest, at 12 ns maximum.

TI's exclusive 2-μm IMPACT technology makes possible extremely dense and fast programmable-array-logic (PAL) circuits. Now four new PAL ICs (TIBPAL16XX-12 series) from TI cut propagation delay to an unprecedented 12 ns. And maximum clock-to-output time to only 10 ns. For the first time, you can design in programmable logic that is faster than that provided by high-speed discrete logic products like the 74AS and 74F families.

TI's new IMPACT PAL ICs provide for cost-effective implementation of a wide range of circuits formerly based on SSI/MSI components: Minicomputers, superminis, professional computers, industrial controls, high-end graphics processors — wherever super speed and programmability are important design criteria.

Military IMPACT PAL family continues to grow

For manufacturers of military products, TI now offers a family of 16 PAL circuits which comply fully with the requirements of MIL-STD-883C, Class B. Included are standard and half-power devices with propagation-delay times of 30 and 40 ns, drawing 185 and 95 mA, respectively.

Where power limitations are tight or *super* speed is vital, TI's unique IMPACT PAL ICs can make the difference — whether for retrofitting an existing design or starting from scratch. Because they dissipate significantly less power for the same high-speed performance (30 ns for 105 mA, maximum). Or for approximately the same power (200 mA, maximum), they can give you 20-ns speed *(see table)*.

CHARACTERISTICS OF TI MILITARY PAL ICs

Type	T_{pd} (ns)	I_{CC} (mA)	F_{max} (MHz)
Standard (16XXA)	30	185	25
Low-power (16XXA-2)	40	95	16
High-speed IMPACT (16XX-20)	20	200	40
Lower-power IMPACT (16XX-30)	30	105	25

Texas Instruments quality and service cut your costs.

You can cut your costs of incoming inspection and testing. Diminish lead times and inventories. Reduce board and systems repair and warranty replacements. And make substantial savings, because these expenses may drive the ultimate cost of your components as high as two or even five times what you paid your supplier for them.

At Texas Instruments, we recognize this problem, and we're doing something about it.

TI is committed to improvements in quality and service that can cut your total "cost of ownership" for the components we manufacture. By stressing on-time delivery, so you can shorten lead times and slash inventories. And by delivering only products conforming to the highest standards of quality and reliability, so you may choose to reduce or eliminate incoming inspection and minimize repair and replacement.

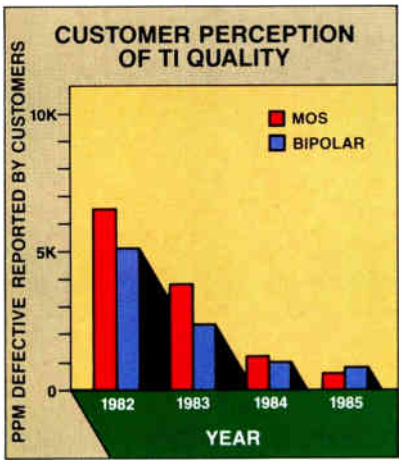
Service partnership with TI makes you the winner

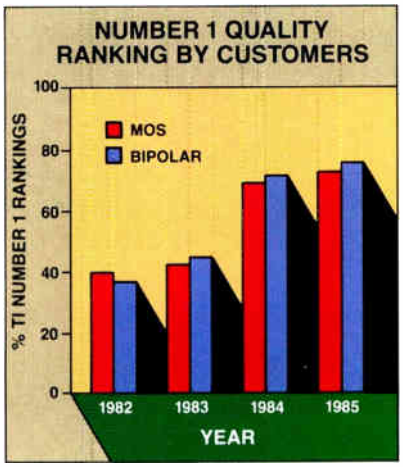
Central to TI's approach is our conviction that supplying semiconductors is more than producing commodities: It is a service that you depend on us for. In order to provide that service, we must establish an appropriate, responsible partnership with you.

To make that partnership work to your advantage, we must provide leadership technology in all areas of your needs — on time. And that is exactly the direction Texas Instruments is moving, to give our customers every benefit of leading-edge technology — including the technology of quality and service.

Quality and reliability: TI's commitment to you

In the era of megabit-class technologies, quality and reliability are increasingly critical. And at TI the bottom line of our quality-improvement program is lower cost of ownership for you. In partnership with our customers, we are making it work. As measured and reported by customers participating in an ongoing feedback program, TI quality — in terms of parts per million (ppm) defective — has reached levels unheard of just a few years ago *(see bar graph below)*.





Among those TI customers taking part in another continuing survey, the number who rank TI's quality first among their semiconductor suppliers shows an impressive and steady increase *(see bar graph above)*. Since 1984 customers in the U.S., Europe, and Japan have presented TI with more than 50 awards for outstanding quality and service achievements.

A record to be proud of? Yes. And we are. But the real payoff from TI's giant steps in innovative technology and service is increased profits and market share for you.

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DPØ2 ☐ 12-ns PAL ICs
GYØ1 ☐ Military IMPACT PAL ICs
DMØ3 ☐ IMPACT FIFOs
LLØ1 ☐ IMPACT line drivers and receivers
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GYØ1 ☐ Military IMPACT PAL ICs
DMØ3 ☐ IMPACT FIFOs
LLØ1 ☐ IMPACT line drivers and receivers
LCØ1 ☐ Signal conditioners

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A FASTER WAY TO DEBUG ASICs WITH HIGH PIN COUNTS

AC CAPABILITY YIELDS 100-PS TIMING RESOLUTION

Application-specific integrated circuits are moving into the 200-pin-count realm, and designers of large ASICs are encountering new problems when they try to verify that prototype devices actually function as they should. These problems are brought on by the sheer pin count of the devices as well as by the characteristics of the technology used to build them. Large devices are more likely to have gross defects and unexpected failure modes, and so parametric characterization is critically important. With increasing numbers of pins, a verification system must provide a large channel-count capacity. In addition, large devices have more complex timing problems created by the long data paths through the device.

The Logic Master 2000 design verification system from Integrated Measurement Systems Inc. addresses these problems head on. The Beaverton, Ore., company's system handles very large devices—it has an input/output channel count of 480—and it now performs ac characterization. To deal with complex timing problems in large devices, the system's ac capability affords 100-ps timing resolution—ideal for verifying large ASICs with sub-2-μm geometries, according to the company. These ac functions have now been integrated with the Logic Master's dc capabilities [*Electronics*, March 3, 1986, p. 32], notably its ability to test for gross leakage (Fig. 1) and to measure voltage and current. The Logic Master provides high-quality connections that are especially useful for measuring very small currents or voltages; even minor changes in capacitance or resistance in electrical connections can result in major measurement changes.

A verification system used to measure such critical ac parameters as setup time, hold time, maximum operating speed, propagation delays, and timing glitches must have an adequate system-wide skew specification. It also needs a straightforward way to verify that the system meets the specification at the device fixture. Only then can designers make timing measurements with confidence.

The Logic Master verification system has a ±1.5-ns skew across all acquisition channels and across all generation channels, thanks to its 100-ps resolution. As a result, both pattern edges and data-acquisition sample times can be placed on an individual pin with 100-ps resolution.

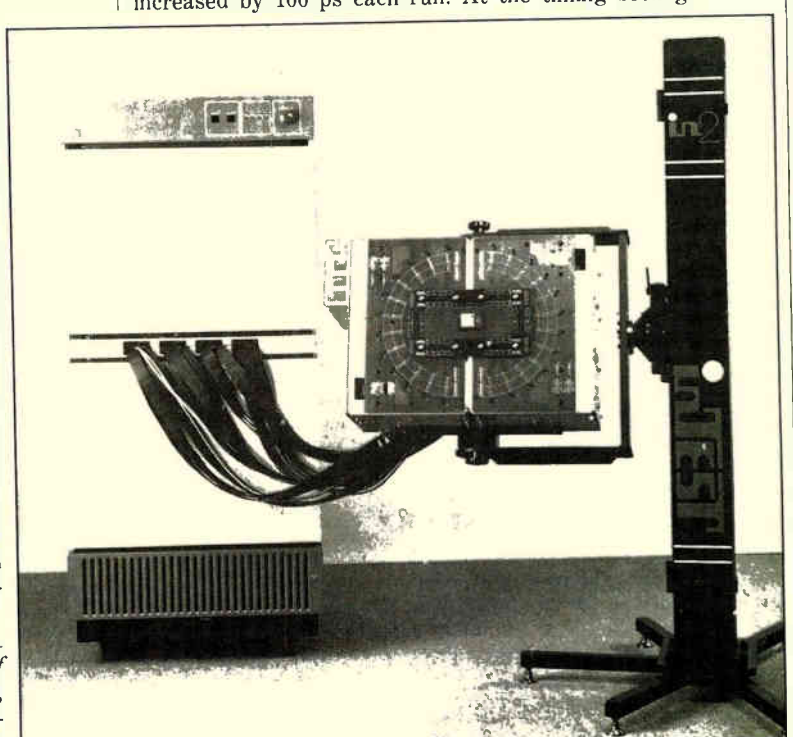
Ac verification measurement requires not only such high resolution and skew but also programmable data formats and flexibility in running multiple passes of a test while varying one or more parameters. On a dual-trace 300-MHz oscilloscope, measured skew of the verification system stimulus is seen when a chosen pattern-generation channel is captured on the B trace and any other pattern-generation channel is captured on the A trace.

Skew on the comparison channels—those that detect the output response of the device under test—can also be checked with respect to a reference timing channel. All compare channels also afford a ±1.5-ns skew. This pattern-generation-to-acquisition skew is a critical value in an integrated system because it determines the accuracy of setup, hold, and delay measurements. With a system skew of ±1.5 ns, the Logic Master's acquisition channels can accurately measure any pulse that is at least 6 ns wide; the verification system's comparator will not detect a narrower pulse.

MEASURING SETUP TIMES

For the device under test, setup times are measured using a delayed-nonreturn-to-zero (DNRZ) format on the input pins being evaluated. DNRZ allows the leading edge of the data to be delayed in 100-ps increments until a failure occurs because a setup time was violated. Verifying setup time of the prototype under test is accomplished using the verification system's programmable formats. Setup time is the maximum length of time the acquired signal must be present before the acquisition is clocked.

The data input (Fig. 2) uses the DNRZ format with a delay programmed to be large enough so that setup time of other inputs will not affect the results. The clock delay is programmed to be the data delay plus the minimum setup time for the input being tested. During test, the DNRZ-formatted pulse transition on the data-input pin can be delayed in 100-ps increments. The test is run repeatedly, with the DNRZ delay increased by 100 ps each run. At the timing settings where



1. LINK UP. To measure gross leakage, the switching matrix connects each input pin to its respective drive channel and disconnects each output pin.

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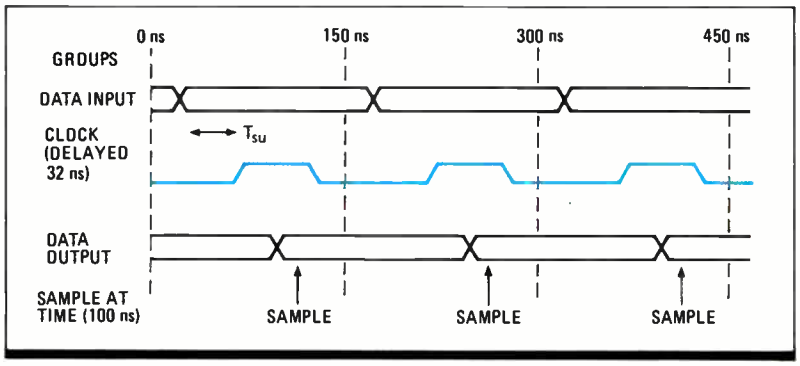
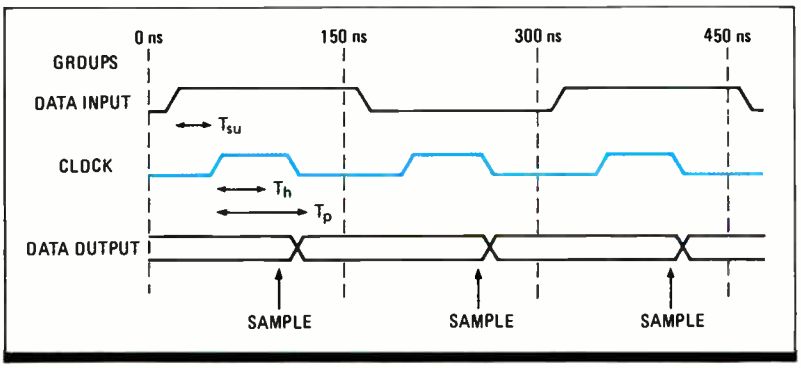
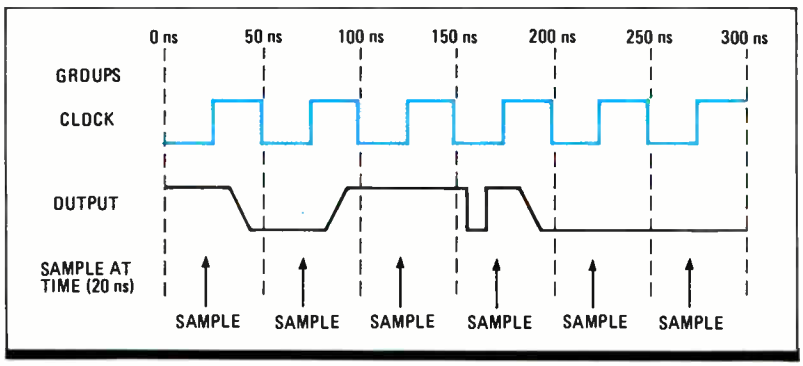


2. MOVING VIOLATION. During test, the system delays the signal on the data input in 100-ps increments until data-input setup time is violated.



3. MINIMUM CLOCK. In a 74LS163 device, the minimum clock rate is determined by the sum of the setup time plus the hold time or the propagation delay, whichever is greater.



4. GLITCH DETECTOR. To find an output glitch in a prototype ASIC, the system performs verification tests while varying the sample time from 5 to 35 ns.

the test fails, the setup time is the difference between the DNRZ delay and the clock delay. Because the data input is delayed, the setup time of other inputs will not affect the test.

To verify the hold-time parameter of the prototype under test, the data-out "sample at" time is move toward the end of the cycle, where output data should be stable. Hold time is the maximum length of time that the acquired signal must be maintained after the acquisition is clocked. Return-to-complement pulses are applied to the data-input pin and delayed to the largest value that meets the prototype's setup time. "Return to complement" means that the data-input signal always returns to the logic state opposite the next pulse in the data stream, thereby ensuring that a logic 1 and 0 each produce a pulse; it is useful for measuring hold times. The pulse width is then programmed to the minimum value that meets the prototype's hold-time specification. The return-to-complement format is used on the data input pins to ensure that the data at the end of the cycle is different from data that is valid through the setup and hold window.

The cycle is run repeatedly, and a data-input pin's trailing edge is pulled from the end of the cycle toward the beginning of the cycle until the output data changes because the hold time of the data-input pin was violated. The number of 100-ps increments required to reach this point is the hold time of the prototype.

Measuring propagation delays for each output pin is a common requirement in the ASIC verification process as well. These delays are measured by moving the output-pin sample time toward the start of the cycle in 100-ps steps until the test fails. In measuring propagation delays, all output pins other than the one under test are masked. The data-output pin's sample time is decreased from late in the cycle while the functional test is run repeatedly. The time from the clock edge to the smallest sample time that passes is the propagation delay for that pin.

The Logic Master can also verify maximum speed (minimum cycle time) of an ASCII device. Because many device technologies—emitter-coupled logic and gallium arsenide, among others—can operate faster than can any available verification, minimum cycle time must be verified by measuring the delay paths inherent in the prototype device. A device will not operate correctly at a cycle rate faster than the setup time plus the propagation delays or hold time, whichever is greater from the clock edge to the appearance of the output.

In the waveform for a 74LS163 device (Fig. 3), the minimum clock rate is determined by the sum of the setup time, assuming it is positive, plus the hold time or the propagation delay, whichever is greater. This means that a system that offers a 100-ps timing resolution can measure minimum cycle time for devices that operate at hundreds of megahertz.

Finally, to detect timing glitches, a verification system needs the ability to sweep the sample time across the clock transition time in small increments. Why this capability is useful is best illustrated with a typical problem in debugging ASIC prototype chips. During simulation of a design, the designer typically produces test vectors that are run on a prototype part at the foundry to ensure that the design meets the functional specification. However, such testing is limited because it looks at only a specific set of conditions to determine that a device meets its specification. It is not uncommon for a prototype to pass the functional test at the foundry but then, during verification testing, to show evidence of a previously undetected timing-related problem.

GETTING THE GLITCH

One common occurrence is an output glitch that occurs on either side of the sample pulse (Fig. 4). The only way to find such a problem is by repeatedly performing verification tests over several passes. On each pass, the designer varies the sample time from 5 to 35 ns in 100-ps increments over the range of time output data. In one of these passes, the glitch will have been detected. Verification testing without being able to vary the sample transition would not have discovered the glitch.

Designers of advanced ASICs have come to depend heavily on dc characteristics as a diagnostic tool to determine how well the device has been built and what its operating tolerances are. The system's integrated dc PMU switching matrix provides a capability never before available in a verification system. The

main purpose of dc parametric testing is to measure the load that a device's input pins present to an external circuit, and to measure the ability of its output pins to drive the load presented by an external circuit. The capabilities required for these measurements are the ability to force voltage and measure current, and the ability to force current and measure voltage, all with high resolution and accuracy. A switching matrix that is compatible with the rest of the fixturing solution is necessary to make these measurements conveniently.

Often, especially when verifying a CMOS prototype device, the first step is to measure its leakage current through the power-supply pin, with all input pins held constant and all output pins disconnected. Called the gross-leakage test, the measurement determines whether there are any major process-related problems in the device. Because gross leakage can be measured quickly, it serves as a rapid method of determining whether or not to perform a functional test.

To measure gross leakage, a switching matrix connects each of the input pins to their respective drive channels, which are automatically set to either a high or a low logic level. The matrix also disconnects each output pin directly. The device power-supply pin is connected directly to the PMU, which serves as a power supply with a very accurate current meter. Because the Logic Master verification system uses an integrated switching matrix, no rewiring of input or output pins is needed to perform PMU measurements. Measuring gross leakage is as easy as pressing the measurement screen function key and selecting the gross-leakage option.

A separate test is run to verify the load presented by the input pins. A prototype device will eventually operate on a circuit board where the device inputs will present a load to the circuits that drive them. In addition, the device outputs must function properly under the load conditions determined by the circuit-board design. If the device offers an excessive load to the driving circuitry, the voltage levels at the device input pins may not attain the correct levels, and the circuit will not operate correctly. As a result, this test is an important step in device verification.

Measuring the loading that is presented by an input pin requires the ability to apply a known voltage to the pin and measure the resulting current. The Logic Master verification system allows the user to perform force-voltage and current-measurement testing automatically on each input pin. To make the current measurement on an input, the switching matrix disconnects the driver pod that is wired to the pin and connects the pin to the PMU. The switching matrix sequentially connects each of the input pins to the PMU. For the first high-to-low transition for each pin, the programmed low input voltage is forced and the resulting current load is measured. Similarly, for the first low-to-high transition, the programmed high input voltage is forced, and the resulting load current is measured. This process proceeds automatically, based on the data pattern, until all input pins have been tested.

It is as critical to check output loading as it is to check input loading. Simulation of loading on an output pin requires the ability to sink or source current to the output pin. The current level depends on the desired load. While the selected current level is being forced, the voltage output from the pin must be measured to verify that it is within allowable limits. To make the measurement as convenient as possible, the verification system should allow the user to program the desired forcing current and range of allowable voltages for each group of simulator pins. The test can then be run, and those pins that fail to pass the allowed voltage range test are flagged.

To make the voltage measurement on an output, the switching matrix disconnects the receiver pod that is wired to the device output pin and connects the pin to the PMU. The switching matrix sequentially connects each of the input pins to the PMU. For the first high-to-low transition for each pin, the programmed low output current is forced and the resulting voltage load is measured. Similarly, for the first low-to-high transition, the programmed high output current is forced, and the resulting voltage is measured. This process proceeds automatically, based on the data pattern, until all output pins have been tested. □

'STAYING CLOSE TO THE CUSTOMER' HELPED DESIGN THE LOGIC MASTER

Roger Hokanson and Ron Gaiser of Integrated Measurement Systems have a number of things in common. Besides being responsible for the Logic Master 2000 design verification system, both are former Tektronix employees, a distinction that they also share with the six founders of the Beaverton, Ore., company at which they work.

The Logic Master 2000 was developed in response to customer demand for a test system able to handle devices with high pin counts. "The way we run the business at Integrated Measurement Systems is by staying close to our customers"—a behavior no doubt acquired at Tektronix, explains Hokanson, product manager. "The reason I'm here is that I have a real strong customer orientation in terms of where I get my information for planning the business."

But ability to test devices with high pin counts was only one requirement. "We realized that not only were they pushing pin counts, they were pushing complexity and process capability as well," says Gaiser, senior engineer for the Logic Master. "So we designed the system to contain those capabilities, the parametrics, the triggering, 100-ps resolution. I helped design the first Logic Master product, and on the latest generation product I added the 100-ps capability to the family."

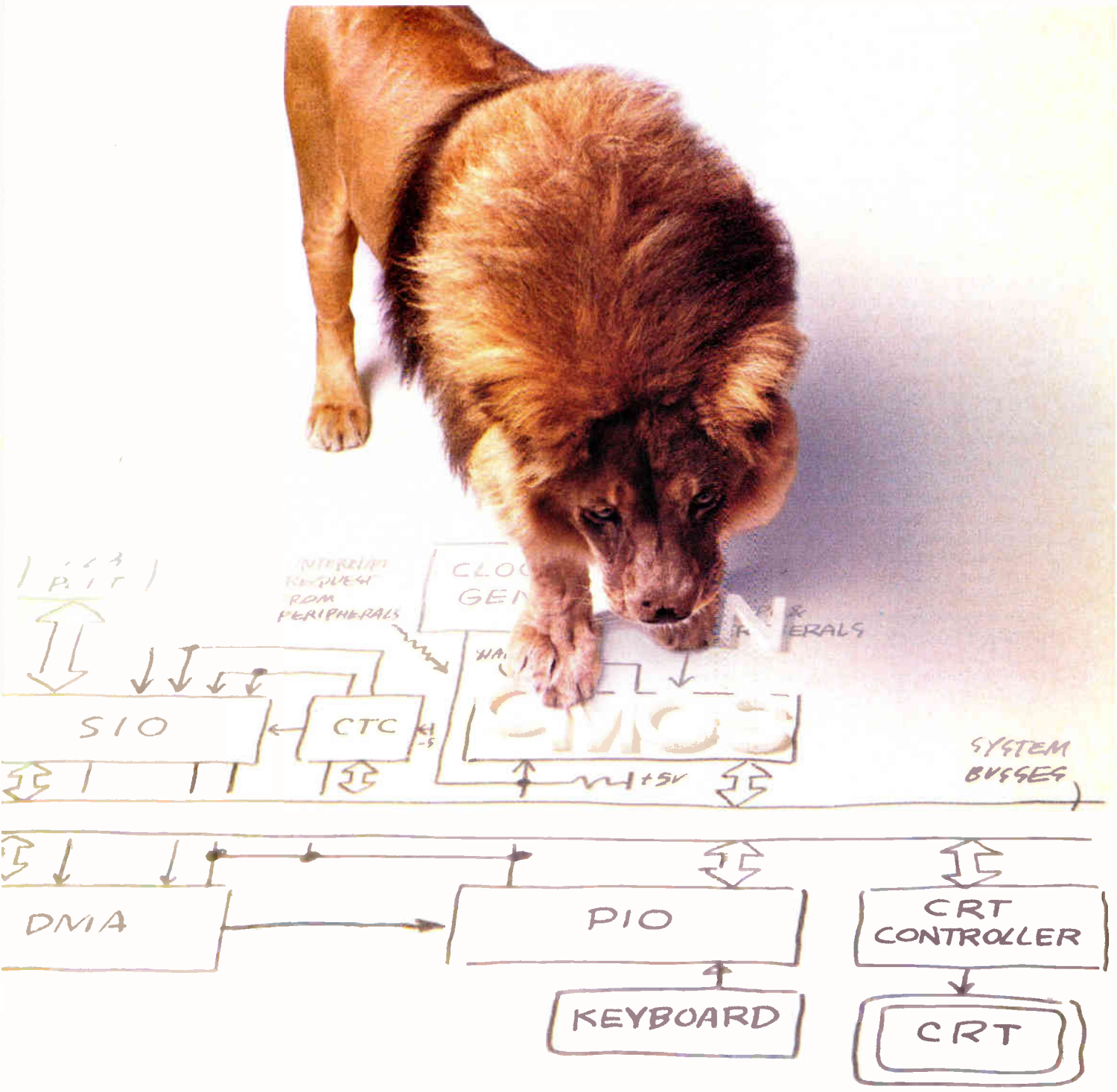
Hokanson left Tektronix in November 1983, having been with the company for nearly 10 years in various marketing positions, and joined Integrated Measurement Systems early in 1984, three months after it opened its doors. He came on board specifically to handle the Logic Master series of products.

LOGIC MASTERS. Hokanson (left) and Gaiser developed a test verification system for ASICs.

Like Hokanson, Gaiser spent a long time at Tektronix. "I started working at Tektronix in 1977 for the semiconductor test system group. In 1979, I joined up with Steve Palmquist and other engineers currently at Integrated Measurement Systems. We worked on a tester for Tektronix and then went on to build the DAS Logic Analyzer. Once the logic analyzer was built, Steve went off to start Integrated Measurement Systems and shortly thereafter asked me to come along."

Hokanson graduated with a MBA from Portland State University in Beaverton. His technical knowledge comes from rigorous self-teaching. Gaiser, too, is self taught in technology. Through on-the-job training, he got enough engineering experience to move up and became a senior engineer. Asked what drew him into electronics, he responds, "I have always liked to tinker in electronics, and it has always felt natural for me."

TOSHIBA CMOS



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Device	Description	Technology	Operating Current at 4MHz	Power-Down Current
TMPZ84C00	4MHz Z80A CPU	CMOS	15mA	< 10μA
TMPZ84C30	CTC: Counter/Timer Circuit	CMOS	3mA	< 10μA
TMPZ84C20	PIO: Parallel Input/Output Controller	CMOS	2mA	< 10μA
T6497	Clock Generator/Controller	CMOS	2mA	< 10μA
TMPZ84C40	SIO: Serial Input/Output Controller	CMOS	25mA	< 10μA
TMPZ84C10	DMA: Direct Memory Access Controller	CMOS	25mA	< 10μA

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3rd (tie)
Company: Philips
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3rd (tie)
Company: Harris Semiconductor
Agency: The Downs Group

65,000 PARALLEL PROCESSORS TACKLE THE BIGGEST DATA JOBS

1-BIPS COMPUTER USES ONE PROCESSOR FOR EACH DATA ELEMENT

A new approach to massive parallelism led Thinking Machines Corp. to a computer that can process as many as 65,536 data items simultaneously at speeds that can blaze well past the billion-instruction-per-second mark. The Cambridge, Mass., company's Connection Machine [*Electronics*, May 5, 1986, p. 16] embodies a technique called data-level parallelism, which runs the same program on all the system's processors, each operating on a unique data element. Until now, all parallel computers executed different programs on different processors simultaneously, a process called control-level parallelism. By contrast, in data-level parallelism each processor is doing the same thing to a different data element.

With its 65,536 processors and 32 megabytes of memory, the computer will execute 1 billion instructions/s in a general-computing application and up to 7 bips for specialized tasks (table, p. 47). With this power, it can add 64,000 numbers together in only 32 μs, and a list of 65,536 32-bit values can be sorted in 33 μs.

That level of performance will make possible a wide variety of new applications in such areas as artificial intelligence, image processing, circuit simulation, and document retrieval—anywhere huge amounts of data must be processed rapidly. The Connection Machine's developers say that its massively parallel architecture is ideal for solving such problems, and they tout the machine's relatively easy programmability. "The Connection Machine most significantly cracks the how-to-program-it problem," says vice president of operations Richard J. Clayton.

The Connection Machine, which comes in a 2,600-lb, 56-by-56-by-62-in. cube (Fig. 1) containing 153 multilayer printed-circuit boards, uses conventional large-scale-integration technology. "We made a conscious choice not to beat our heads against the wall technologically," explains Clayton. Each of the 128 15-by-18-in. processor boards contains 32 multiple-processor chips, and each of these holds 16 individual 1-bit processors as well as one node of the interprocessor communications network. Each processor comes with 4,096 bits of static random-access memory.

The interprocessor communications network connecting the processors on each chip is called the router. Through the router, any processor can send data to any of the other 65,535 processors. All the links are established in software, and they can be changed between programs or during the course of a single program, so the system can configure its processors in a rectangular grid for one problem and in a ring network for the next. This flexibility facilitates quick transfer of data to where it is needed for an upcoming calculation. The router has an overall capacity of 3 billion bits/s.

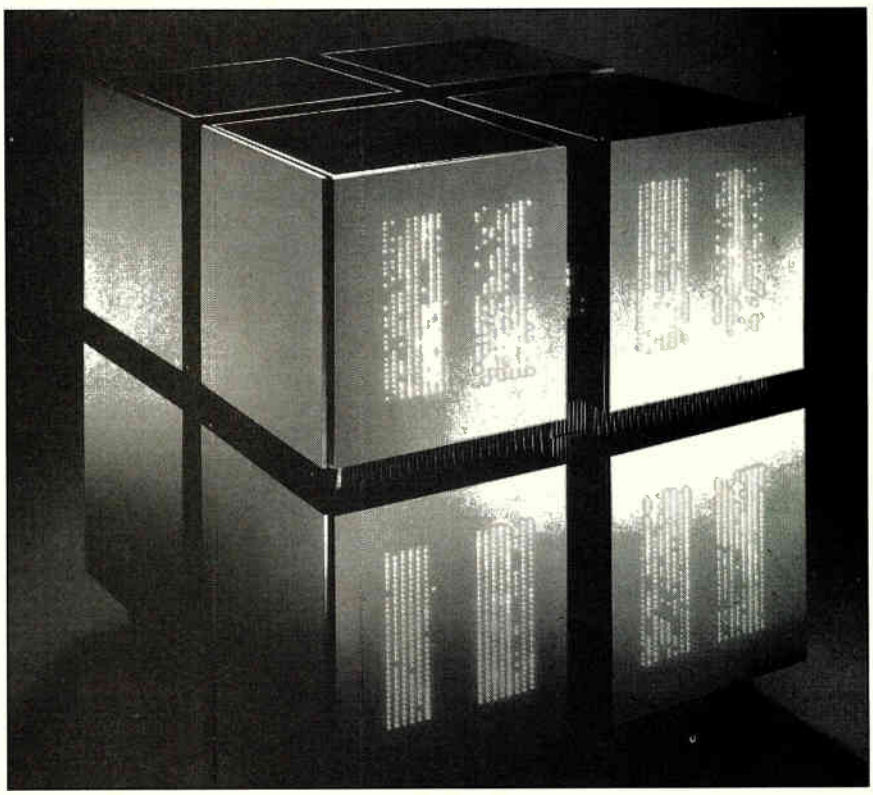
The Connection Machine's microcontroller handles data-storage allocation and distributes data items to each processor. A front-end processor controls program execution.

Data-level parallelism, the basis of the Connection Machine, is a notable departure from the control-level parallelism used in other parallel computers. All computer programs, whether on a parallel or a sequential computer, contain data elements and a sequence of instructions. In moving a program from a sequential machine to a control-level parallel machine, the instructions in the program are divided up so that the independent ones are executed in parallel on multiple processors. Because large numbers of data elements in the original program are also independent, operations on these elements may be carried out in parallel by multiple processors.

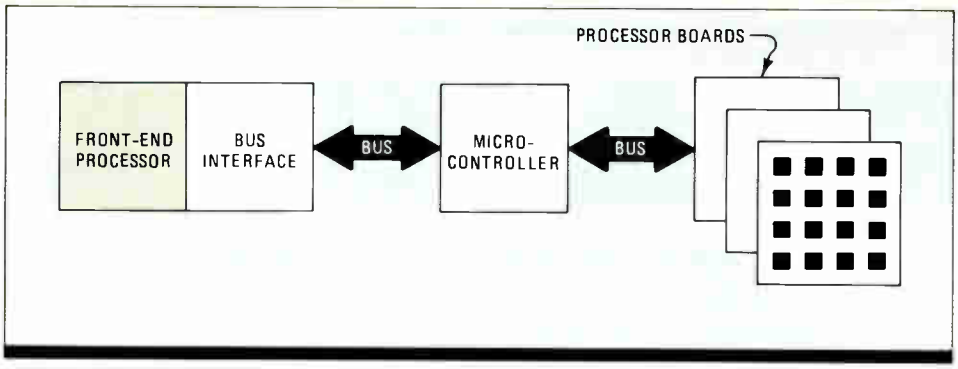
ONLY FOR THE BIG JOBS

Not surprisingly, data-level parallelism works best on programs with large amounts of data; this type of machine is best suited for problems with more than 10,000 data elements, says James Bailey, Thinking Machines' marketing manager. Although the Connection Machine is not cheap—the full-blown version sells for $3 million—the price per mips is actually only about $3,000, compared with up to $150,000/mips for mainframes, according to the company.

To control the operation of the entire system, data-level parallelism uses a single control sequence, or program, and executes it one step at a time. With the Connection Machine,



1. PARALLELOGRAM. Thinking Machines' Connection Machine uses 65,536 processors and a technique called data-level parallelism to execute 1 billion instructions per second.



2. FRAMEWORK. The Connection Machine's main functional blocks are its processor, microcontroller, and external input/output channel. A front-end processor runs the control program.

that program resides on a front-end computer—either a Digital Equipment Corp. VAX or a Symbolics Inc. 3600 series computer. All programs are stored on the front-end machine, whose operating system supports program development, networking, and low-speed input and output.

The program stored on the Connection Machine's front-end computer contains two types of instructions: those that operate on one data element and those that operate on a whole data set at once. All single-data-element instructions are executed directly by the front-end computer. The important instructions—those that operate on a whole data set at once—are passed to the Connection Machine hardware (Fig. 2) for execution.

For example, a key application developed for the Connection Machine is very large-scale-integration simulation. A complete integrated circuit is developed by simulating the thousands of individual transistors that make up the chip. Here, the instructions passed to the Connection Machine would be those that tell each processor to step through its individual transistor simulation process. Each processor executes exactly the same sequence of instructions but applies them to its own unique data. In this way, parameters such as voltage, current, and conductance can be calculated for thousands of different transistors simultaneously.

The machine handles instructions operating on an entire data set

In practice, applications problems for the Connection Machine need not have exactly 65,536 items to match exactly the number of processors. If there are fewer, the system temporarily switches off the processors that are not needed. If there are more data elements, the machine's hardware operates in the virtual processor mode, by which each physical processor simulates multiple processors. A standard feature of the system is that up to one million virtual processors can be supported. In addition, an external input/output channel with a 500-Mb/s capacity can be used to input digitized data to applications from external devices such as video cameras and external disk drives.

"You don't have to force-fit problems to our architecture," says Bailey. Data-level parallelism is inherent in many of the problems themselves. In addition to VLSI simulation, examples developed and tested for the Connection Machine include a fluid-dynamics application, a stereo-image matching application, and document retrieval for data-base searches.

Document retrieval is one application Thinking Machines expects to be particularly important and widely used in years to come. Today, on-line data bases that access newspaper stories and financial, medical, and legal information are moving into offices. But it is often difficult and time-consuming to retrieve the precise information that the user is looking for. The company intends to put an end to that problem with its new Document Retrieval package for the Connection Machine.

Keyword-based searches (common with systems such as Mead Data Central Corp.'s Nexis) are very good at quickly finding all documents that contain the user-entered keywords. The problem is that they often produce too many documents for a user to reasonably look through. At the same time, they miss many documents that cover the desired subject but don't happen to contain the exact keywords the user has entered.

With the Connection Machine document-retrieval program, all documents related to the desired subject are called up, even if they do not contain the exact keywords. In addition, the documents are grouped in order of importance, putting the more relevant items high up in the document queue.

In the document-retrieval program, the complete data base of documents is stored in the machine, one or more documents per processor. (In a demonstration system, Thinking Machines used a data base consisting of stories from the Reuters news wire.) To initiate a search, the user enters one or more keywords. These keywords are used to find the first document, which is selected by the user from a group of documents that contain all or some of the keywords.

DOCUMENT BECOMES THE PATTERN

Once the first document has been selected, the initial keywords are not used anymore. Instead, that first document is used to form a search pattern. The search pattern contains all the content words in the document; conjunctions, prepositions, and other unimportant words and redundancies are not used. One by one, the front-end computer broadcasts the words in the pattern to all the processors at once. Each processor checks to see if its document contains the word. In conjunction with this matching process, the documents are scored according to how closely they match the first document. With each word that matches, the document's score is incremented. When the entire pattern has been broadcast, the document that most closely matches the pattern will have the highest score. This one will be presented to the user first. The remaining documents will be grouped beneath that in descending order by score.

To search, match, and score, the Connection Machine constructs content kernels, which encode the important words and phrases from the source document in a compressed form. Content kernels are created for each source document; each document in the data base is a source document.

The content kernel is produced automatically from the source document through a multistage process. First, the source document is processed by a document-indexer program that marks the most significant terms in the text. Next, these terms are encoded into a bit-vector data structure using a method called surrogate coding, also sometimes referred to as hash coding, which allows the content kernel to be stored more compactly and speeds up the search process. In surrogate coding, each term (word) in the content kernel is mapped into 10 different bits in a 1,024-bit vector. The 10 selected bits in the vector are set to a value of 1 to indicate the presence of that word in the document.

The source document in its original form is available for retrieval and presentation to the user when needed. The original document's location on the system disk is stored in the content kernel. The complete kernel data structure contains three items: Score, Document-id, and Kernel. The document lookup program uses Score to accumulate the ranking of each

kernel in the data base according to how closely it matches the user's search pattern. Each time a match is found, Score is updated.

The Document-id index contains a reference to the original source document from which the content kernel was derived. When a kernel is selected from the data-base lookup, the user is shown the source document referred to by this index. Kernel is a table of the surrogate-coded bit-vectors.

Thinking Machines has extensively tested a production-level version of this application. The system operates on a data base of about 15,000 news-wire articles, which occupy about 40 megabytes of text. An automatic indexing system selects the content kernels for each document; these kernels are about one third the original size of the text. Surrogate coding compresses the data by about another factor of two. Currently, the kernels are encoded, at 30 terms per vector, into as many 1,024-bit vectors as are needed; several vectors are used for a long document.

With this encoding and a 160-megabyte data base, equivalent to an entire year of news from a typical news wire, the Connection Machine can retrieve the 20 closest-matching documents in about 50 ms, according to the company. During this time, the computer performs about 200 million operations, for an effective execution speed of 6,000 mips.

Even larger bases can be handled using the same technique with two enhancements. The first is the use of a very high-speed paging disk. This allows larger numbers of content kernels to be swapped into the system for searching. The second enhancement is the use of cluster analysis.

When the system has many documents on the same subject, it need not store all their content kernels individually. It can store one for the whole cluster and then retrieve the full set of related documents when needed. (A single document can participate in more than one cluster.) As the total data base grows, the size of the average cluster grows with it, making this technique appropriate for large-scale data bases. With the addition of paging and clustering, data bases above 10 gigabytes can be handled easily, according to the machine's developers.

Users can also program their own applications easily by using tools provided with the machine. "Because of the role of the front-end processor, you program the machine in a language and in an environment and with a set of tools that are all eminently familiar," says Clayton. The main tools are the C* and Lisp* compilers. These are extensions to the popular programming languages, incorporating parallel data structures. Using these, "you can say 'I want to create a parallel object,' which means place each occurrence of the object one per processor," says Clayton. "That's all handled automatically by the compiler." With these tools, Thinking Machines believes it has licked the long-time parallel-computing bugaboo: the difficulty of writing parallel programs. Adds Clayton, "There's nothing new about how you program it—but what you program may be different." □

CONNECTION MACHINE PERFORMANCE

Typical applications performance (billions of instructions/s)	
General computing	1.0
Document search	6.0
Fluid-flow simulation	7.0
Stereo-image matching	1.0
Variable-word-length arithmetic performance (bips)	
64-bit integer add	1.15
32-bit integer add	1.98
16-bit integer add	2.60
8-bit integer add	4.60
64-bit move	1.24
32-bit move	2.35
16-bit move	4.10
8-bit move	6.60
Sorting performance	
65,536 32-bit values	33 ms

HOW HILLIS GOT THE CONNECTION MACHINE OUT OF THE LAB

Thinking Machines Corp.'s cofounder W. Daniel Hillis first became interested in massive parallelism as a student at the Massachusetts Institute of Technology. The prospect of building a machine with the power to attack tough problems in such areas as artificial intelligence was so exciting that Hillis developed the idea for his dissertation as well as for a book, *The Connection Machine* (The MIT Press, 1985).

At the school from 1978 to 1983, Hillis worked at the Artificial Intelligence Laboratory and was a Hertz Fellow. Although he was heavily involved in research there, he always had one foot in the commercial world. "I'm somebody who goes crazy unless I can actually see something physical that's coming out of it," he says. "Even while I was at the AI lab, I was working trying to build things. So I'm not a paper and pencil researcher."

He got the chance to move his Connection Machine from paper to practice when Thinking Machines was formed in 1983. "The first six months was figuring out really what we wanted to do. The next two and a half years was doing it."

For Thinking Machines, key ingredients in harnessing the people and organizational resources needed to successfully realize the project were the skills of vice president of operations Richard J. Clayton. Hillis and Sheryl L. Handler, president and cofounder, lured Clayton to Thinking Machines from Digital Equipment Corp., where he had been vice president of computer systems development and vice president of advanced manufacturing technology.

As a 20-year DEC veteran, Clayton has seen that company rise from a start-up to No. 2 in the computer business. At Thinking Machines, he found many parallels with his early days at DEC. "I think there's a crispness of focus that you can have in a small company, especially with a new product and a new mission, that is just very, very difficult to achieve in a very large company." Clayton is an MIT alumnus and holds a master's degree.

For Thinking Machines, the challenge now is to build on the big splash the Connection Machine is making. "This product is only the beginning of a family of computers," says Hillis.

If broadening the product is the recipe for success, Clayton is already mixing the ingredients. "We expect to be bringing in a large number of good people in the next 18 months," he says. "That's going to be a really exciting time to be involved in a new architecture, developing new algorithms and new programming techniques."

W. DANIEL HILLIS

RICHARD J. CLAYTON

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PROBING THE NEWS

WHAT'S BEHIND THE IBM PRODUCT BLITZ

A SPATE OF NETWORKING PRODUCTS AND A NEW MIDRANGE THRUST

by Tom Manuel

It was an unprecedented product blitz from IBM Corp. last week—some 125 new products unveiled at the National Computer Conference in Las Vegas. The announcements covered everything from touch screens to networking software, but the thrust of the message was loud and clear. Now that it has secured the mainframe and personal-computer markets, the Armonk, N. Y., giant is fixing on the midrange computer field as its next target.

IBM has long been a major factor in midrange computers, with its System/36 and /38, but recent developments have upstaged its efforts [*Electronics*, June 16, 1986, p. 49]. So it is shoring up its product lines in three main ways. It is meeting customer demands for connectivity: the ability of dissimilar systems to work together. Greater connectivity also will help end the anarchy of its incompatible computer lines and networks. Finally, IBM is bolstering the System/36 and completely revamping the System/38, as well as unveiling powerful new disk drives.

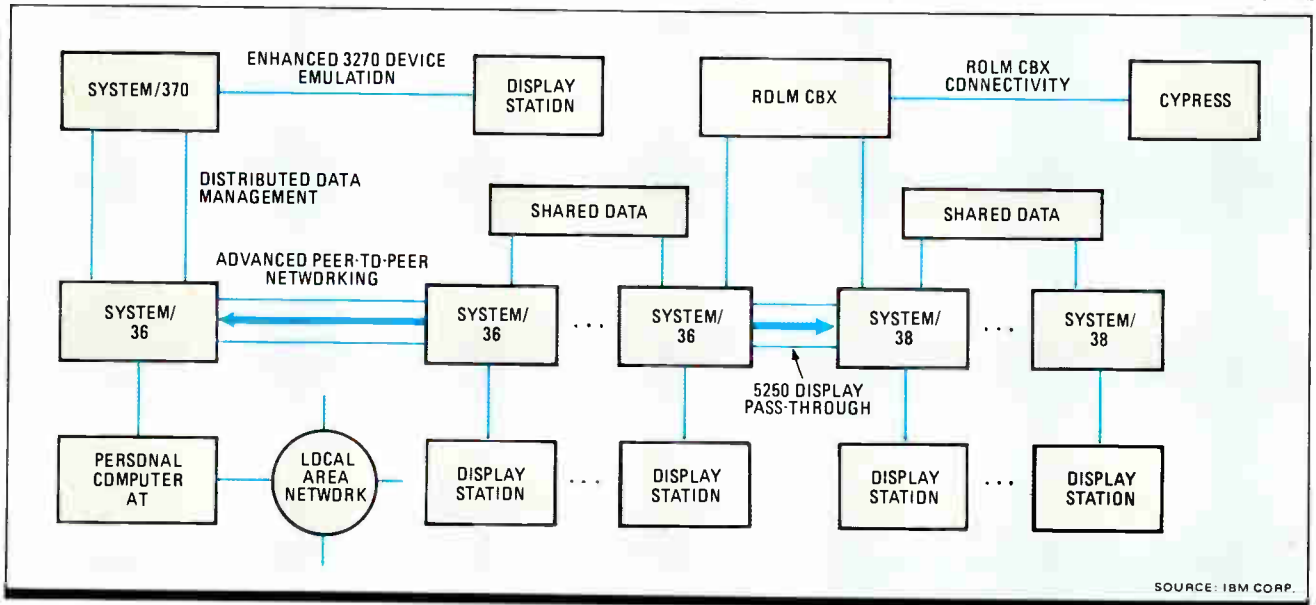
Most industry observers consider the announcements significant both for IBM's customers and the computer industry because they mean much better price/performance ratios and increased functionality for IBM's midrange product lines. Equally important, the interconnectivity features included in the package indicate that the giant is moving toward total interconnection of its many incompatible computer systems and work stations.

Industry observers generally give high marks to IBM's new direction. Analyst Michael Geran of E. F. Hutton Co. in New York says, "IBM essentially accomplished what it set out to do: improve performance of the 36 and 38, enhance connectivity between them, and improve price/performance in the midrange." Another member of the Wall Street community, who requests anonymity, says, "It is a good, smart move. IBM is admitting that customers stress accessing data no matter where it is."

But some analysts say IBM is still moving too slowly to satisfy rapidly advancing customer needs in distributed data processing. For example, William F. Zachmann, vice president for corporate research at International Data Corp. in Framingham, Mass., maintains that the announcements do not add up to any significant changes in midrange departmental computing. "It was just a lot of stuff and it doesn't change [IBM's offering] very much. System/36 and System/38 are still just as incompatible as ever," he says.

Zachmann believes that the product enhancements and new features do not solve the problems of using two fundamentally incompatible small-business and office computer systems as integrated midrange departmental computers in the broad distributed-data-processing environment. "It won't help IBM very much in the midrange," he says, because there are some quite strong competitors there already with better networking functions, such as Digital Equipment Corp. "And these announcements don't change the rules of the game," he concludes.

Nevertheless, IBM is going to remain a strong player in the midrange market simply because of its size and influence in any part of the market in which it chooses to play. A case in point is the recent IBM announcement that it has



BOOSTING CONNECTIVITY. The System/36 and System/38 will now be better able to operate together and with other computers.

shipped 100,000 System/36s, hardly an insignificant number.

Still, there is no question that IBM was lagging behind its customers' perceived needs for greater connectivity. Computer users everywhere are demanding the advantages of easy interconnections and compatibility among all their computer facilities. The reason for their demands is that after years of talk, distributed data processing is finally catching on. Customers want all of their computers, work stations, and terminals to be able to communicate with one another in order to transfer data and messages and to share resources.

But IBM was caught with its pants down because of its snail-like implementation of connectivity. And in a touch of irony, it is the rapid acceptance of the IBM Personal Computer that is a major catalyst of the distributed data processing trend. IBM executives admit that the company was responding to intense customer pressure for more distributed data processing, greater sharing of resources, and the ability to connect any terminal, work station, or personal computer to any other computer and quickly and simply access and use any file, no matter where it is.

IBM's slow pace comes from the fact that it is facing many problems with global interconnection because it had so many product lines and networking schemes, all of which were incompatible. Instead, the company has been making incremental steps toward the goal. But with the flurry of announcements in Las Vegas, and the advances in both interconnectivity among IBM systems and products and in their communications with the outside, Big Blue has lengthened its stride.

WELL ENHANCED. Interconnection enhancements include software products for connections among System/36 and System/38 computers in a mixed network. They also include new links for communications with mainframes and various work stations and personal computers, both IBM's and those from other vendors.

Also crucial for the System/36 and the /38 are new interconnection facilities for asynchronous ASCII terminals and devices, more IBM Token Ring network interfaces, interconnection between terminals and computers through the CBX telephone and data switch from IBM's Rolm unit, and more mainframe links.

The Las Vegas blitz of introductions even included IBM's first direct Ethernet connection—an Ethernet interface board for the IBM RT Personal Computer. IBM claims these interconnection offerings will satisfy most customer demands, but more detached observers say it has yet to achieve total interconnectivity.

TOUCHY. InfoWindow System touch screen handles graphics, full-motion or still video, and high-fidelity audio.

IBM took another step in response to a combination of customer demands, slackening sales growth in the midrange, and competition from successful minicomputer and superminicomputer companies. That is the enhancement of its System/36 and System/38 lines. Both were beginning to show their age; both needed and got better overall price/performance ratios, as well as an extended range of performance with new top and bottom ends.

According to E. F. Hutton's Geran, "IBM has been under pressure from customers not to deadend the System/36." Most of the many System/36 customers probably do not want to upgrade to the System/38 because their software is incompatible. Yet those customers need a growth path. "By improving the performance of both the System/36 and System/38 and providing connectivity between them, IBM is answering the customers' needs," says Geran. "But it's only the first step in a long road IBM must follow to have these midrange systems function efficaciously as nodes, intelligent processors, and stand-alone office systems."

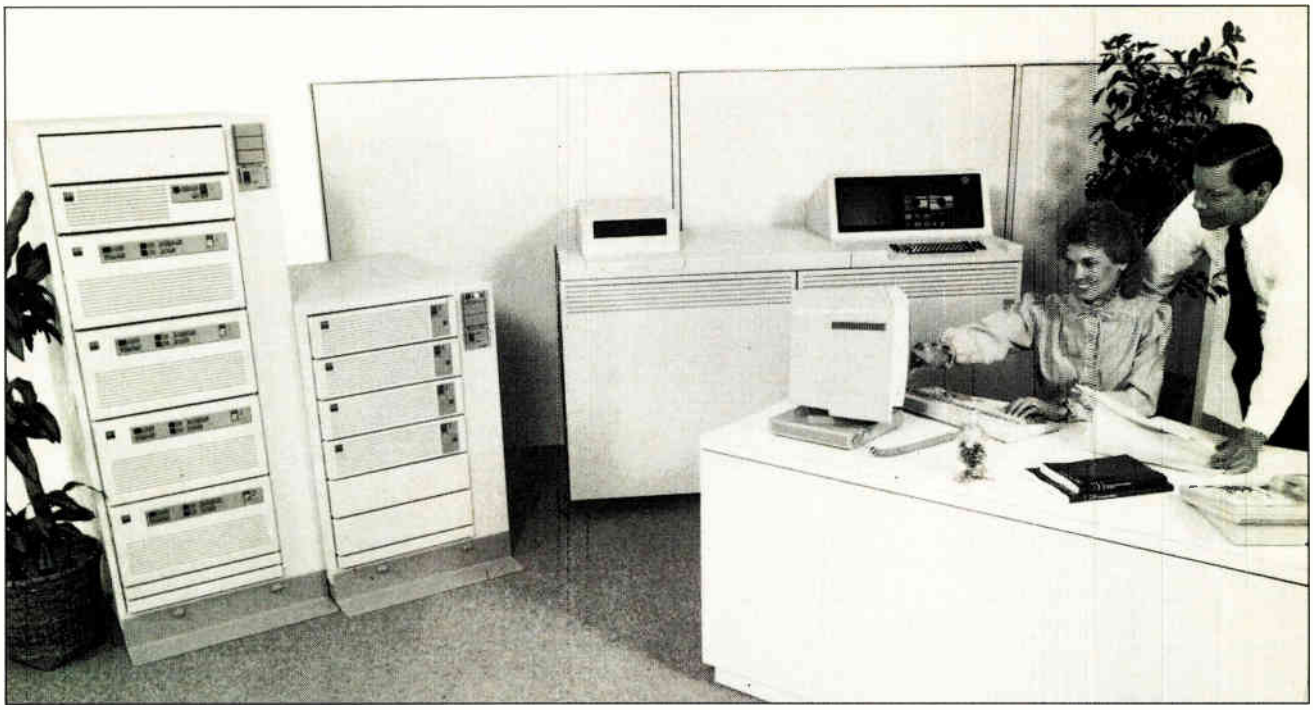
LINEUP. Display stations are, from top, the 3193, which can handle an 8½-by-11-in. page; the 3194 color; the 3191 monochrome.

Still, the sheer volume of new products introduced at Las Vegas is proof that IBM is taking an enormous first step. Highlights of the new connectivity products include an advanced peer-to-peer networking (APPN) scheme for System/36 and /38, a new work station controller to connect them to different types of computers and the IBM Token-Ring Network, the Rolmbridge to connect ASCII work stations and terminals to System/36 and System/38 models, and a uniform structure for exchanging data between IBM PCs and System/370 mainframes.

NEW MACHINES. New computers include three new System/36 models and a complete replacement of the System/38 family with six new models. Also unveiled at Las Vegas were three new disk drives for the midrange systems, the InfoWindow interactive presentation station, and a series of new and enhanced work stations.

As one of the major enhancements of connectivity in its midrange systems, IBM developed the APPN to directly tie the two product lines together without going through a 370 host. The APPN allows users to work on any computer in the network, thus expanding the range of performance and functions when System/36 and /38 computers are networked together.

Another aid to connectivity is a new display station controller, the 3174 subsystem control unit. It connects IBM 3270-type display stations, including terminals and PCs that emulate the 3270, and ASCII terminals, to the System/36 and /38 lines, as well as to 370 main-



BETTER PRICE/PERFORMANCE. For the System/38, IBM has new disk drives, including the 8-in. 9332, left, and the 14-in. 9335, far left.

frames and to the Token-Ring Network.

Another aspect of connectivity is communication through telephone lines, and the Rolmbridge 5250 Link Protocol Converter, developed jointly by IBM and its Rolm subsidiary, addresses this need. The 5250 is a card set for the Rolm CBX family of digital private branch exchanges. It connects System/36 and /38 computers to Rolm ASCII terminals and other asynchronous devices.

To increase PC users' access to 370 mainframe resources, IBM introduced a new uniform data-exchange structure. Called the IBM System/370 to IBM Personal Computer Enhanced Connectivity Facilities, these menu-driven programs give PC users access to files, disk space, and printers on the mainframe. Users can query and extract data from hosts, transfer files between hosts and PCs, and issue host commands from a PC.

FASTER, BIGGER. Of the three new System/36 models, the new high-end 5360 Model D has a faster processor and bigger, faster memory. A maximum 7 megabytes of memory—3.5 times the current model's—is achieved with one of IBM's latest technologies, the million-bit memory chip packaged into a 4-megabyte memory card. Internal performance of the Model D is about 50% faster than the current top-end model.

The other two new machines, the models B and C, are in the midsize slot of the System/36 line, the 5362 family. When new disk drives, expanded office function software, and connectivity enhancements are added, and enhancements announced in January are considered, the System/36's departmental processing performance is improved by 400% over that available in December 1985, according to the company.

The six new System/38 models sport better price/performance ratios across the board. For example, the new low end, the model 100, has 30% more performance than the current model 4 at about a 30% lower price. The memory boards based on the 1-megabit chip offer up to 32 megabytes, double the memory of the former high end, the model 40. Enhancements to the System/38 Control Program Facility (the operating system) support more office applications, new disk drives, the new peer-to-peer networking, and double the number of PC users supported to 200.

To improve performance of the System/36 and /38, IBM introduced three disk drives. Two of the subsystems, for both product lines, use a new 8-in. unit and offer 200 and 400 megabytes of formatted data. An original-equipment-manufacturer version of the 8-in. unit, called the IBM Model 678, is also being offered (see p. 19).

A larger capacity subsystem for the System/38 uses a new 14-in. unit with 856 megabytes. A 19-in. rack and cabinet holds up to four of the 9335 856-megabyte units, giving a storage subsystem of almost 3.5 gigabytes for the System/38 line. Up to four of these can be connected to a system.

To enter a new application area—interactive presentation and information access—IBM introduced the InfoWindow system, a combination of a high-resolution touch-screen color display, an interactive video-disk player, and an IBM PC. An Enhanced Graphics Adapter board in the PC mixes computer graphics and video images on the touch screen. Over 100 InfoWindow systems are providing interactive visitors' guides at Expo 86 in Vancouver, B. C., Canada.

More than half a dozen new and enhanced display work stations were also introduced. They are additions to the IBM 3270 information-display series. Some of them offer a new amber-gold phosphor said to be easier on the eyes. One of the display stations, the IBM 3194 with a 14-in. color display, can run up to four host sessions simultaneously in separate windows on the screen.

LOWER, LONGER. Another bold move on IBM's part is lower maintenance charges and longer warranties for selected products—one year for new disk drives and some display stations and up to three years for several of the new display stations. Typical warranties in the computer industry last only 90 days. "The reduced maintenance costs and longer warranties are a reflection of IBM's quality improvements being translated directly into customer benefits," says Edward E. Lucente, vice president and group executive of the IBM Informations Systems Group.

This new service policy, together with the vast range of new products, adds up to a formidable new weapon in IBM's never-ending quest for control over 100% of the computer market. But to gain control of the midrange market, it must defeat well-entrenched competitors and a host of fledglings with leading-edge technology. So the midrange may be IBM's biggest challenge yet. □

WILL BRITAIN'S AMSTRAD MAKE IT BIG IN THE U.S.?

ITS $799 WORD PROCESSOR IS ONLY THE START OF ITS INVASION

by David Boothroyd

NEW YORK

The stage is set for a British invasion of the U.S. by Amstrad Consumer Electronics plc's word processor, which is billed as the affordable replacement for the typewriter. The London firm's PCW 8256 is already a hit in Europe, and test marketing has started in New York and Los Angeles. The machine could be in stores by Labor Day, and the question is whether Amstrad will repeat its European success.

Amstrad worked to smooth its trip to America this spring by purchasing its chief rival in the low end of the market, Sinclair Research Ltd., for $24.7 million [*Electronics*, April 14, 1986, p. 64]. This consolidated the company's position at home, giving it 50% of the market in terms of value as well as a head start toward the same dominance in the rest of Europe. Now it has a marketing opportunity in the U.S. that it intends to exploit with a complete line of products.

The 8256 has several things going for it. One is merchandising muscle: it is being imported by Sears World Trade Inc., an arm of the giant Sears, Roebuck & Co., the largest retailer in the U.S. The other is its price/performance strength: it has a built-in floppy-disk drive, keyboard, monitor, word-processing software, letter-quality dot-matrix printer, and RS-232-C port—all for $799. It uses the CP/M operating system and has 256-K of read-only memory. And unlike similar products recently introduced by Magnavox Co. and the Smith-Corona Group of SCM Corp., the Amstrad can be upgraded to a computer. That package and price have already made the machine a big seller in Europe for small businesses as well as for use in the home.

Sears has had initial signs of interest from more than 30 mass-merchandisers and business-equipment stores, and already has signed up several, says Otto Georgi, general manager of the Consumer Electronics Group for Sears World Trade in Chicago. He says the list includes Burdines, based in Miami, and Lechmere Sales, a Boston-based consumer electronics chain.

And although the deal with Sears provides for Amstrad to offer the retailer first option on any new computers, "all the product is paid for by Sears before delivery and all promotion and advertising is done by Sears," says Amstrad's Jim L. Rice, group operations director. "We are going into the U.S. market in a safe way."

As for Sears itself, it generally test markets products for about 90 days before before putting them on its shelves. But Georgi says the early word from the test markets, where machines have been displayed for up to four weeks, is that sales have been going well, and he is optimistic that a move will come sooner than usual. He estimates that "well over 100" machines have been sold.

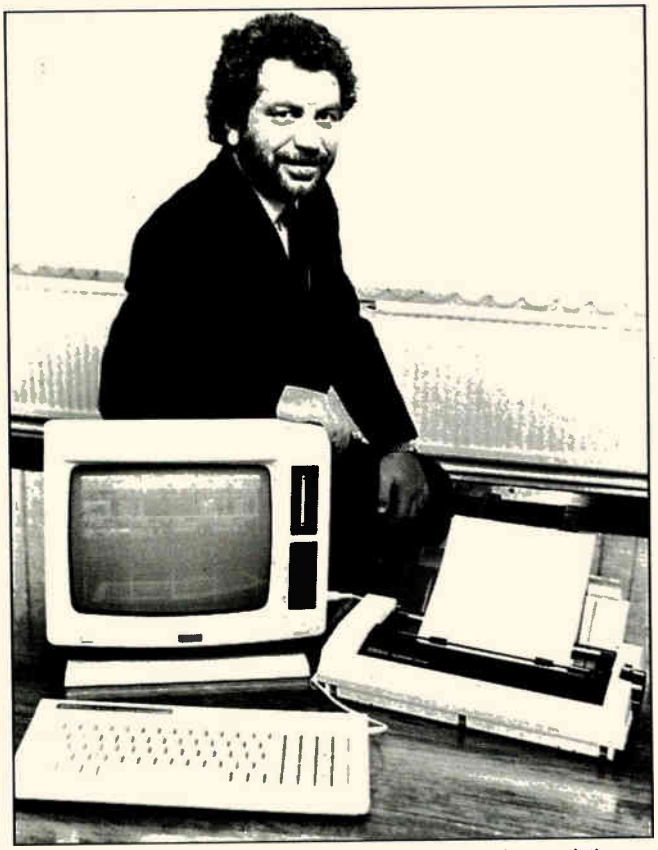
The Amstrad PCW 8256 is selling at a total rate of 40,000 units per month in Britain, France, Germany, and Spain, says Kim Duncan, senior director of the Sears World Trade Electronics Group. He says he hopes to be selling the same number in the U.S. by year end. Sears is committed to buying 100,000 units.

MORE COMING. But as far as Amstrad is concerned, that's just the start. "If the U.S. comes off, it will make European business almost insignificant," Rice says. "However, the U.S. has been a graveyard for several companies in the last few years, not least Sinclair and Acorn [Computers]," he continues.

Nevertheless, Amstrad has no intention of stopping with the word processor. It has set up a subsidiary to handle U.S. marketing, Amstrad International USA Inc., in Northbrook, Ill. President Chris Pullen will organize sales of Amstrad's other products—TV sets, stereo systems, portable audio products, and Compact Disc players—beginning later this year.

That all this is coming to pass can be credited to the aggressiveness of founder and chief executive Alan Sugar (the company name is a contraction of "Alan Michael Sugar Trading"). He built the company by parlaying a knack for understanding what the average consumer wants and sharp negotiating skills that have extracted the lowest possible prices from his mainly Far Eastern suppliers.

In the six months that ended on Dec. 31, 1985, Sugar tripled Amstrad profits to about $70 million—not bad for a man who started out by selling automobile antennas from the back of his car. He moved on to stereo systems that appeared to be separate rack-mounted components but were really a single unit, which cut costs by avoiding duplication of electronics. A range of consumer products followed, from



SWEET DEALS. Knowing what people want and tough negotiating on prices have taken Sugar a long way from selling antennas out of his car.

An ASIC design won't sparkle, if your vendor doesn't cut it.

In application specific ICs, you have two choices—an optimal design or something less brilliant.

That's why you can be shortchanged by a one-product ASIC house. They must sell you what they have—not necessarily what you need. You miss out on the full promise of ASICs. Here's why.

An optimal ASIC design gives you the edge.
An ASIC solution is not just a gate array. Or a standard cell. Or a cell-based custom circuit.

These are simply different approaches to an IC that meets your application requirements. Time-to-market, development cost, production price and performance needs make every job different. No design approach works best every time.

When is that a problem? When a vendor has only one design approach, odds are it isn't the best one for you.

Gould AMI offers all approaches to assure you the optimal solution. And a leg up on competition.

Get an uncompromising team on your side.
Choose a true ASIC house. One with a full continuum of design approaches. The leading design capability. And an experienced team of ASIC professionals committed to making your job easier. That's the best guarantee of getting the results you want. That's Gould AMI.

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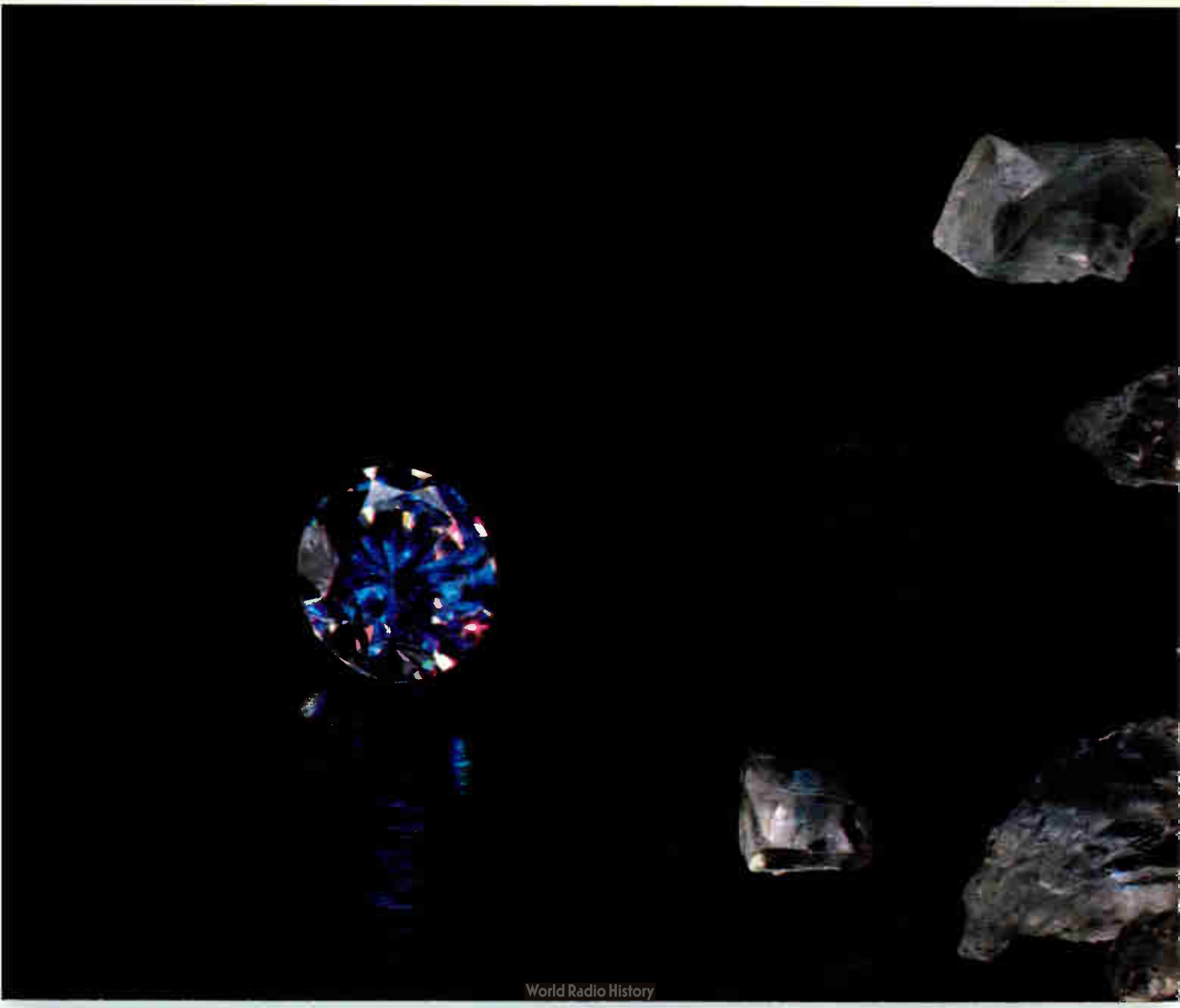

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GOULD
Electronics

TV sets to portable radio cassette players—especially twin-deck models, aimed at the huge tape-copying market.

His purchase of Sinclair meant victory in a bitter battle over the low end of the computer market in Britain. Observers agree that Amstrad won because Sugar proved to be better at marketing and quality control than Sir Clive Sinclair. They say Amstrad's success also has been based on sensible designs and very low prices. And the pragmatic, hard-headed Sugar is not interested in risky innovative ventures like those that have been Sir Clive's downfall. The best known of those was the C5, an electric vehicle that was a disastrous failure.

NAME VALUE. Amstrad's takeover of Sir Clive's company is based mainly on the value of the Sinclair name. Amstrad paid $7.7 million for the rights to the name and all products, plus another $17 million to Sinclair and its main subcontractors for stock, work in progress, and committed orders. Amstrad will have the exclusive right to use the Sinclair brand. Those familiar with both companies say the deal was a bargain for Amstrad, noting that Sinclair was once valued at $210 million.

"We have bought it because we perceive it as an opportunity to exploit the Sinclair name in the computer-games and home-entertainment market, where it has had a worldwide position in the past few years," says Amstrad's Rice. "We don't do things unless we make money out of them, and we see this as a money-making opportunity, particularly with the large software following for Sinclair machines," he says.

New products planned by Amstrad—using the Sinclair name—include a computer and a range of calculators. Amstrad may also market a laptop computer called Pandora from Sinclair, if the latter's research is successful. Amstrad has the right of first refusal.

The laptop machine will use the same flat cathode-ray-tube technology as Sinclair's small TV. The tube's flatness is achieved by positioning the electron gun at the side and deflecting the electrons at right angles to hit the phosphor screen, creating a picture in the normal manner. Pandora will have a 24-by-80-column display and a full-size keyboard, with built-in software for diary, scheduling, and word processing. It will run under CP/M, and peripherals will include a disk drive and printer. The product has been developed at Sinclair Research's headquarters in Cambridge.

Pandora is likely to sell for about $770. It was scheduled to debut in Britain at the end of last year, but was delayed because of the company's financial problems.

OFFSHORE MOVES. Changes that will follow the Amstrad takeover include the dropping of the Sinclair 68000-based QL computer, greater emphasis on European and other foreign markets, and possibly a further shift away from British subcontractors to the Far East, a move that would be consistent with Sugar's reputation as a tough negotiator on prices.

Sugar has said existing Sinclair suppliers will be invited to bid for new contracts, but he has also said that one of the main problems with Sinclair's products has been poor quality control. He is setting up a special quality-control organization to check products.

"The problem is that most of the parts come from Japan," he says, and the UK imposes an 18% duty on imported microchips. But when products are assembled outside the European Community, he says, the duty on the finished product is only 4.9%.

Sugar and Sinclair are now likely to follow very different paths that reflect their contrasting personalities. Sugar will continue to sell products, manufactured mainly in the Far East, in high volume at very competitive prices. His latest offering, for example, is a complete stereo system—including CD player—for about $460.

Sir Clive will concentrate entirely on research projects (see "What Clive Sinclair is up to now"). Some of these will be developments of work already done by Sinclair Research; others will be contract research projects sponsored by outside companies.

Amstrad regards Europe, where the home-computer market is still small compared with that in Britain, as a market with great growth potential. Amstrad is already the market leader in France, and second in West Germany and Spain, and plans to increase its marketing efforts there for both its own brand-name machines and the Sinclair models.

At the same time, the British home-computer market has fallen to half its peak level. It is far from dead, however, and Amstrad will now have one of the broadest ranges in the market. It also perceives an opening as other manufacturers move more upmarket toward the personal computer, leaving for Amstrad the niche for the purely home machine intended primarily for entertainment. □

Additional reporting provided by Wesley R. Iversen in Chicago.

WHAT CLIVE SINCLAIR IS UP TO NOW

Now that Sir Clive Sinclair has sold Sinclair Research Ltd. to Amstrad Consumer Electronics plc, what does the future hold for him? The answer is a series of research projects, further steps on the journey that has taken him from calculator to electric car.

Some of the new projects are already in progress. The most significant of these is in wafer-scale integration, an effort that attempts to succeed where many others have failed. The first product, a 40-Mb, 5-in. disk-drive replacement, will be ready next year, says Sir Clive. One innovation he claims for the project is that the configuration of the chips on the wafer can be altered to eliminate areas that develop faults. The configuration is held in software, and the wafer tests and verifies itself every time it is switched on.

Barclay's, one of Britain's four major banks, has provided initial financing for this project, and Sir Clive is trying to raise further funds to meet the estimated $77 million cost of going into production. He is reported to have recruited a senior executive from a large U. S. company to head the operation, although no announcement has been made.

SINCLAIR: Several research projects are still on the fire.

Another project is likely to be a low-priced cellular telephone aimed at the mass-consumer market. The as-yet-unnamed backer will own a majority of the company, with Sir Clive holding a minority.

Timex Group, Sinclair Research's largest subcontractor, is the likeliest candidate to back the project. The Waterbury, Conn., company has manufactured the small flat-screen TV for Sinclair, which, though not a great market success, is still available. Timex recently took over sole responsibility for the black and white set, and is now considering a color version. The company also built Sinclair's low-cost personal computer and sold it in the U. S.

Sinclair also may pursue other ventures, including a supercomputer. He says it may be based on the Inmos Corp. transputer, which is capable of 1 billion floating-point operations per second. Another venture aims at recycling some of the ideas used in the C5 electric vehicle, despite the failure of that product. *–David Boothroyd*

LSI LOGIC WEDS SOFTWARE TO SILICON AND PROSPERS

THE $140 MILLION COMPANY PUTS EMPHASIS ON SERVICE AND LEAVES OTHER ASIC HOUSES IN THE DUST

MILPITAS, CALIF.

Anyone looking for a bright spot in the current semiconductor doldrums inevitably finds LSI Logic Corp. From a standing start five years ago, it has emerged as the leading supplier of application-specific integrated circuits, and the old-line semiconductor makers—Fairchild, Intel, Motorola, and National Semiconductor—will have to hustle to catch up.

It may not be easy: the lesson appears to be that becoming a leader in ASICs means standing the semiconductor business on its head. Where merchant houses emphasize silicon wizardry and give away the services to access it, LSI Logic tightly couples software to silicon, then sells both at a profit. Other ASIC houses take the same route, but no one does it on quite the same scale as LSI Logic. Last year, half the company's revenue came from software and services and half from chip sales. This year, the chip share will grow to 60% as higher-priced designs move into production.

O'MEARA: The emphasis is on service instead of silicon.

LSI Logic began business in 1981, using Japan's Toshiba Corp. as a foundry for finished wafers. Its initial goal was one design a day; it now turns out five or six. Its $140 million in ASIC sales left Tokyo's Fujitsu Ltd. a poor second with $101.3 million, most of it consumed internally. Its nearest U.S. competitor, Gould AMI Semiconductors, Santa Clara, Calif., had sales of only $30 million. Software and service revenue alone was more than twice the entire MOS gate-array revenue of any U.S. company.

The company's extensive product line—and the merchant semiconductor background of its founders and top executives—makes it look like a chipmaker with a specialized customer interface. But it considers itself a design house—one with a finely tuned foundry at its disposal. "A lot of our competitors say they are in the silicon business," says William O'Meara, LSI Logic's chief marketing officer. "We don't think so. We think we're in the service business."

It's a key distinction, O'Meara says. "Otherwise, design becomes a necessary path that you have to travel in order to get to the silicon. Therefore people will do the design at cost—they want to get over that hurdle to get to the silicon.

"Our perspective is different. We say that design is a business in itself. In many cases, a design doesn't make it to production. The buyer misses a market window. He loses a flyoff with another contractor. He wants to add logic, change the design, and do another chip. If we have been paid for the design, he's not embarrassed and we're not angry."

The tight coupling of design to production is what separates LSI Logic from pure CAE companies, which provide generic tools that can be used with a silicon foundry. LSI Logic's CAE tools, written in C and highly portable, run on a variety of mainframes, minicomputers, and work stations, but they can be used to design LSI Logic chips only. In return for this exclusivity, LSI Logic guarantees that a design will work in silicon.

"Our CAE system is integrated into the manufacturing process," says Keith Lobo, vice president of marketing for advanced silicon and software products. "For example, as technology advances, we develop new libraries for new production processes. We also adjust the way we handle physical characteristics of the circuit—1.5 μm is different than 3 μm. The customer can buy into next-generation technology."

Andrew Prophet of Dataquest Inc. agrees that proprietary software has a built-in advantage over generic CAE because knowledge of how to tailor software to new fabrication techniques takes time to filter out to the generic world. "CAE systems have to be tailored to the processing," he says.

The one CAE area for which LSI Logic does not offer tools to its customers is layout. "After doing a lot of designs, we concluded that the customer should be responsible for simulation and testing, but not layout," says Lobo.

WEAK SPOT. "Most systems designers are not that good at physical layout," explains Lobo. "And in any case, putting layout tools in the hands of the customer means you will have less automation, so as to give the designer as much influence as possible on the chip."

But, Lobo says, automation is necessary to turn out designs in volume. "Our CAE methodology pumps out layouts in a highly automated manner."

This design machine has helped give LSI Logic a huge edge on the competition, most analysts believe. The company is now working on some 3,000 designs, two to five times as many as Gould AMI, estimates analyst Andrew J. Kessler of PaineWebber Inc., New York. LSI Logic's backlog could be as much as $225 million, he says.

It now has 40% of all designs of more than 1,000 gates, a 60% chunk of the gate-array market, says Millard Phelps, who tracks the company for Hambrecht & Quist Inc. This huge backlog, which is just reaching production, will push LSI Logic to $1 billion in sales by 1990, Phelps says. In that period, says Dataquest, the total market for MOS gate arrays will zoom to nearly $3.8 billion from 1985's $722 million level.

LSI Logic's tools cost around $75,000 for a version that runs on a Digital

LSI LOGIC: TOPS IN ASICs IN 1985

Company	Sales ($ million)
LSI Logic	$140.0
Fujitsu	101.3
Toshiba	45.6
NEC	42.8
Seiko	33.8
Gould	30.0
Hitachi	29.1
Hughes	19.2
RCA	19.0
Motorola	15.0

SOURCE: DATAQUEST INC.

LSI LOGIC IS A FIVE-YEAR SUCCESS STORY

Year	1981	1982	1983	1984	1985
Sales	–	$4,974	$34,835	$84,486	$140,012
Net income (loss)	($1,959)	($3,740)	$12,572*	$15,457	$ 10,114
Number of employees	46	114	397	1,077	1,380

*Includes tax credit of $2.62 million
($ thousands)

SOURCE: LSI LOGIC CORP.

Equipment Corp. MicroVAX II or Sun III work station from Sun Microsystems Inc. Break-even point for leasing of the software is four or five designs a year, Lobo says.

Despite this stiff price, customers keep coming back. "I am very positive on them in all ways," says John McMains, vice president of engineering at Paradise Systems Inc. The South San Francisco, Calif., company has used LSI Logic on several of its graphics controller chips. "We have done three designs, and have two more under way," McMains adds. "Each circuit worked the first time. That in itself is remarkable."

WEEKEND WORK. Paradise Systems performed its own circuit design, test-vector generation, and simulation on a 10,000-gate array. "When we finally had the circuit we wanted, they laid it out over a weekend," says McMains.

To match its design-to-production depth in ASICs, LSI Logic has been pulling new design techniques out of its hat like a stage magician. Starting as a pure gate-array company with a single process—CMOS—LSI Logic has added capabilities to match new levels of complexity. The process remains the same, but the ever-bigger chips now come with structured-array memory and standard-cell arithmetic logic units in any floor plan on the chip and built from free-floating channelless gates or compacted arrays.

The compacted arrays are uncommitted transistor pairs that the company connects with two- and three-layer metal to give the highest gate densities. For example, LSI Logic's first compacted array boasted 50,000 connected gates on an array of 139,000.

These techniques are available to all ASIC makers. But LSI Logic has now begun tailoring its own software into a kind of proprietary standard product, such as the 32-bit multiplier-accumulator it introduced last fall.

This circuit performs favorably against the emitter-coupled-logic MAC put out by Advanced Micro Devices Inc., Sunnyvale, Calif., Phelps points out. LSI Logic's part was started nearly two years after AMD's, however, and finished at about the same time. A silicon compiler, called Macgen, allows customers to design their own MACs of any size, and LSI Logic intends to follow up this product with other standard ASICs that are user-tailorable.

Such fast footwork may keep the company ahead of serious competition, Dataquest's Prophet suggests. "Fujitsu and Toshiba have economies of scale in production that could make them a major threat to LSI Logic. Then the battle becomes service-related. How good are your design centers? Do you have the right CAE tools? Are they user-friendly?"

LSI Logic's marketing effort may also dazzle the Japanese, Phelps indicates. Founder and chief executive officer Wilfred J. Corrigan has laid out a global strategy that has LSI Logic cloning itself wherever the market warrants it. It has spawned independent subsidiaries in Canada, Germany, and Japan and has acquired a controlling interest in British chip maker STC plc. Within five years, LSI Logic will do 35% to 40% of its business abroad, according to Corrigan.

LOBO: Automating layout keeps design volume high.

CORRIGAN: A global strategy to get in the hot markets.

He says he sees little to fear from his company's toughest competitors, the Japanese. "All signals we get from the government are that we will not allow Japan to destroy the U.S. semiconductor industry," he says. "The Japanese will be less aggressive."

Corrigan says the stronger yen has hurt Japanese suppliers. "It's hard to take a 40% price cut when your margin is only 5%."

"LSI Logic will be squeezed more slowly than the others in market share because they are aggressive and execute well," says Phelps of Hambrecht & Quist. "And the market is growing so fast that they could lose half of their market share and still triple their business." *–Clifford Barney*

BOTTOM LINES

SILITEC SAYS IT MAY BE ACQUIRED

Siltec Corp., which lost $2.4 million in the first quarter of 1986, indicates that it "has been engaged in ongoing discussions with a major corporation that could lead to the acquisition of the company." Siltec emphasizes that the discussions are very preliminary and no terms have been agreed on. The Menlo Park, Calif., manufacturer of silicon wafers and production systems for them says that although industry conditions have begun to improve, it expects significant operating losses in the second quarter as well.

CONVERGENT TO BUY SYSTEMS COMPANY

Convergent Technologies Inc. will acquire Display Data Corp. in another expansion move. Convergent, of San Jose, Calif., makes computers for original-equipment manufacturers, and Display Data, Hunt Valley, Md., markets turnkey computer systems. The agreement calls for Display Data shareholders to receive 7.6 million shares of Convergent stock. The deal is another step in Convergent's federation of its vertical market: last year it acquired 40% of Baron Data Systems, a vendor of computer support for the legal field, and also bought 3Com Corp., a maker of Ethernet local-area networks.

SALES INCREASE 2% FOR ANALOGIC

Sales by Analogic Corp., a Peabody, Mass., manufacturer of signal-processing and data-conversion instruments and equipment, increased 2% in the third fiscal quarter over the previous quarter. Sales for the period, which ended April 30, totaled $34.4 million, compared with $33.6 million for the second quarter. However, the company's net income of $2.4 million dipped slightly from the second quarter's $2.5 million. Third quarter sales in 1985 totaled $34.7 million.

NTT SETS UP A PAIR OF FINANCIAL UNITS

Nippon Telegraph & Telephone Corp. has set up two financial subsidiaries in England and the Netherlands to boost its overseas fund-raising and investment activities. The two new subsidiaries, called NTT Finance (Holland) BV and NTT Finance (U.K.) Ltd., also will enable the Tokyo parent company to take advantage of favorable foreign exchange rates in paying for its overseas equipment procurements.

HOLLAND GETS EXCITED BY THE PROBLEMS IN CAD

BOULDER, COLO.

Bruce M. Holland values innovation so much that he gives his employees at Cadnetix Corp. a day off on Feb. 11, Thomas A. Edison's birthday. The 34-year-old president and founder hopes that celebrating the birthday of the father of research and development will remind them of the importance of innovation in solving problems.

"One thing that characterizes this business [computer-aided design and engineering] is a lot of unsolved problems. The first phase is putting together an interesting product and making some sales to the so-called early adopters," says Holland, who started Cadnetix in 1981 to automate the design of printed-circuit boards. "A lot of times that first product has not solved enough of the problems to get widespread acceptance."

HOLLAND: Cadnetix' long road ahead excites its founder.

Holland thinks the CAD/CAE market is now in the second phase: technology is clearing enough design hurdles to spark widespread acceptance. "When you finally solve all the problems, it becomes a commodity market. Companies then compete on pricing and ability to manufacture," he says. "We are excited by the fact we are still a long way from that."

Holland, who graduated from the University of Colorado with a BS in electrical engineering and computer science, credits Cadnetix' early success to a focus on pc-board design, which he says was a huge engineering automation market that was largely ignored at the start by other CAD companies. That focus resulted in sales that more than doubled each year. Net sales in the last quarter, ended March 31, climbed to $7.7 million from $3.9 million the year before. Profits more than doubled—$1.1 million, compared to last year's $407,000.

Holland also directed Cadnetix toward the engineering side of pc-board design, as opposed to layout only. The company's portfolio of more than 15 products ranges from specialized routing engines to CAD platform software that runs on IBM Corp.'s Personal Computer AT.

From the start, Cadnetix' founding engineers applied a bit of office automation to the CAD marketplace. When introduced in late 1983, Cadnetix' work stations had an icon-based operating system aimed at boosting productivity of new and occasional users.

"The system was announced a week before Apple announced the Lisa and a year before the Macintosh. We were one of the pioneers of this interface," says Holland. "We applied it to the CAD/CAE industry because it is noted for the incredible long learning curves on work stations." The icons were an immediate hit, recalls Holland, who says Cadnetix' first customer did seven new boards in 12 weeks—before that, eight months to completion was not unusual. "If anything, I am proudest that we have brought to the industry a new sensitivity of the learning curve," says Holland.

Before forming Cadnetix, Holland was director of engineering for word-processing vendor NBI Inc. in Boulder He helped found NBI in 1973 and was the principal architect of its System 3000, an experience that he says taught him the value of user interfaces.

MORE THAN ICONS. "It is not just a matter of some icons on the screen or pop-up windows. You have to think the system through from top to bottom," he says. "Some companies put out a CAD package, believing they could later make systems easier to use with icons. But you end up rewriting almost every line of code, because in CAD nearly everything you do is a user interface."

While competing companies work on creating new user interfaces, Holland intends to aim Cadnetix at other design bottlenecks, with parallel efforts going on in new software algorithms and hardware accelerators.

"Unique hardware architectures [such as for simulation and routing engines] are our forte, and I think this strength sets us apart from those trying to solve design problems only in software," he notes. Once a hardware advance is made, Holland says, Cadnetix refines CAD algorithms to take advantange of it. To Holland, the hardware-software two-step is the best path to make significant strides toward solving the many problems in CAD. *–J. Robert Lineback*

PEOPLE ON THE MOVE

JOHN CONROY

☐ Graphics hardware manufacturer Microfield Graphics Inc., Beaverton, Ore., has named John Conroy president and chief operating officer. Previously, he served three years as president of Santa Barbara Laboratories Inc., which he cofounded. Before that, he was a vice president at Information Magnetics Corp. He has a BSEE from New York University.

RAYMOND M. FRITZ

☐ LSI Logic Corp. has promoted Raymond M. Fritz to vice president and corporate controller. Fritz, 41, replaces D. Scott Mercer, who was named vice president and chief financial officer. Prior to joining the Milpitas, Calif., maker of application-specific integrated circuits (see p. 57), Fritz held financial positions at Xerox, Versatec, and Singer. He has a BS in accounting from Benedictine College in Kansas and an MBA from Atlanta University.

E. E. FERREY

☐ VLSI Technology Inc., Milpitas, Calif., has named E. E. (Ed) Ferrey to its board of directors. Ferrey was president and chief executive officer of the American Electronics Association from 1960 through 1985, the years during which it grew from a West Coast trade group with a few hundred members to an international association with more than 3,000 member companies. A graduate of Indiana University, Ferrey now has a consulting business in Menlo Park, Calif.

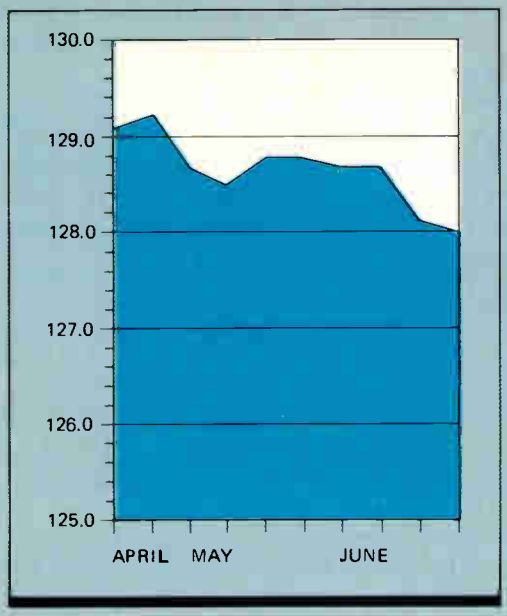
ROLF E. SODERSTROM

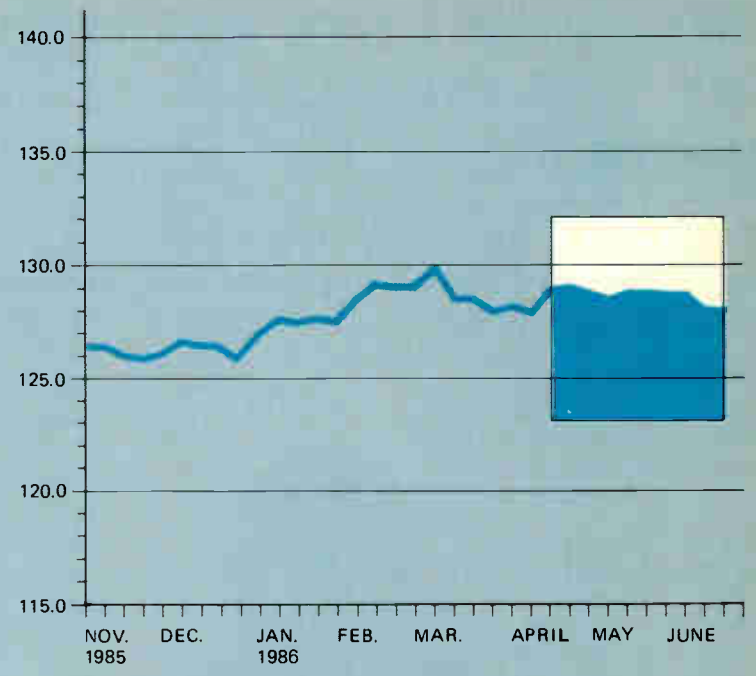
☐ Codex Corp., the Mansfield, Mass., subsidiary of Motorola Inc. that supplies integrated networks for large corporations, has named Rolf E. Soderstrom executive vice president. He will oversee day-to-day business operations. Soderstrom, who has a BSEE from Tufts University and an MBA from Northeastern University, joined Codex in 1969 as vice president of manufacturing.

SAMUEL A. MUSA

☐ Dallas military supplier E-Systems Inc. has named Samuel A. Musa vice president of research and advanced technology. Before joining E-Systems three years ago, he was deputy director of military systems technology in the office of the Under Secretary of Defense for Research and Engineering. Musa, 46, had been director of research at E-Systems before his promotion and is now responsible for all R&D, computer-based information systems, and technology strategic planning. Musa has MS and PhD degrees in applied physics from Harvard and BA and BSEE degrees from Rutgers University.

ELECTRONICS INDEX





THIS WEEK	= 128.0
LAST WEEK	= 128.1
YEAR AGO	= 127.2
1982	= 100.0

The *Electronics* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

U.S. GENERAL ECONOMIC INDICATORS

	May 1986	April 1986	May 1985
Average prime rate (%)	8.5	8.6	10.3
Retail sales ($ billions)	117.053	117.039	114.026
Unemployment rate (%)	7.2	7.0	7.2

U.S. ELECTRONICS INDUSTRY EMPLOYMENT

Production workers (thousands)	April 1986	March 1986	April 1985
Office and computing machines	170.4	171.7	195.1
Communications equipment	275.4	275.8	294.3
Radio and TV receiving equipment	53.5	54.6	54.0
Components	350.7	351.4	389.4

Unable to shake free from its sales slump, the electronics industry cut 3,500 workers in April, the 18th consecutive month in which production employment shrank. This brings the total number of workers down to 850,000, the lowest level since the summer of 1983. And it appears likely that payrolls will remain tight as long as imports continue to hurt domestic producers, a condition that is made worse by soft demand for electronics products. Efforts to automate to lower break-even points are likely to result in further reductions in employment.

During the past year, the computer industry made the deepest payroll cuts, with companies slashing nonsupervisory employment by nearly 13%. What's more, with the increasing popularity of Korean-made models cutting into orders for U.S. companies in the personal computer segment of the business, the end of the slide in the computer industry may not yet be over. So with the industry's order books suggesting it cannot look forward to a near-term pickup, more of the same sort of payroll paring may be in store.

Computer manufacturers are not alone in their less than optimistic outlook. Near-term prospects elsewhere in the electronics industry are looking dim as business spending remains soggy, especially in manufacturing. But there is a bright spot: improvement should come later on as the past year's decline in oil prices, interest rates, and the dollar promises to give both businesses and consumers a shot in the arm.

On February 19th, 1985, we started the process of bringing *Electronics* back...

It took more than a year, but we've finished the job.

With a biweekly frequency and expanded circulation designed for today's marketplace.

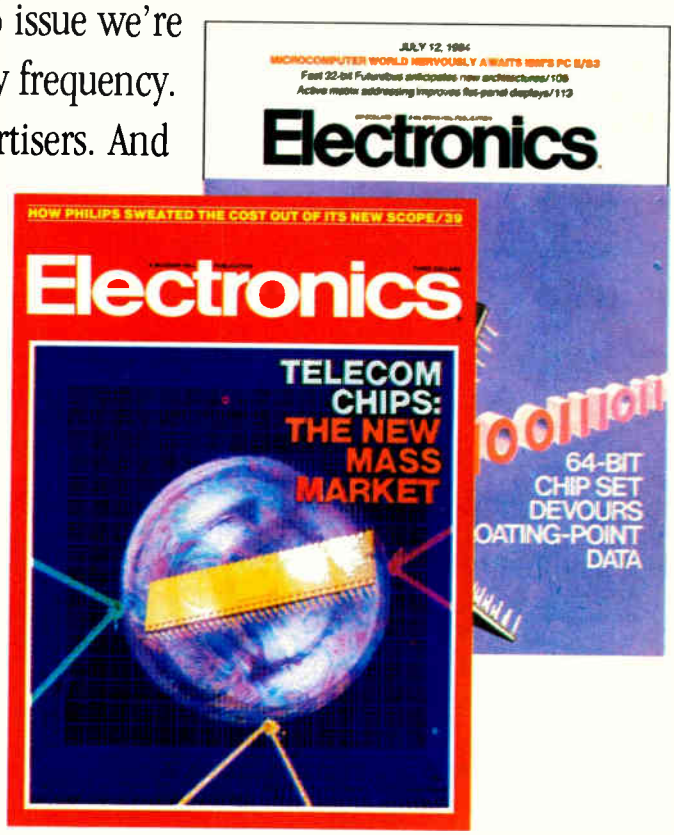
And we've learned a few things along the way.

We've learned that bringing *Electronics* back to its premiere technology position takes millions of dollars in investment. And an unwavering corporate commitment.

We've learned that bringing *Electronics* back takes worldwide editorial clout. So we've built a senior editorial staff (40 strong) and placed them in the hot-spot markets of the industry. In New York, Palo Alto, Los Angeles, Dallas, Boston, Washington and Chicago. In Tokyo, London, Paris and Frankfurt. And in eleven other countries around the world.

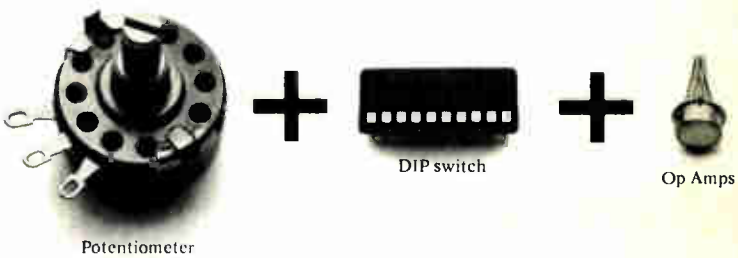
We've listened to our readers. And we've learned that to better implement our present technology format requires a more measured editorial cycle. So starting with our July 10, 1986 issue we're returning to our original biweekly frequency.

We've heard from our advertisers. And to extend our market coverage, we've begun a major circulation expansion by adding more technology managers and senior engineers to our domestic subscriber base, thereby reaching more than 92,000 subscribers in June and well over 100,000 by December 1986. At no additional cost to advertisers.



The job is done.

Simple



The sum of the parts on the left side of the equation approximately equals the Sierra standard cell chip on the right.

But not quite, because less is always more.

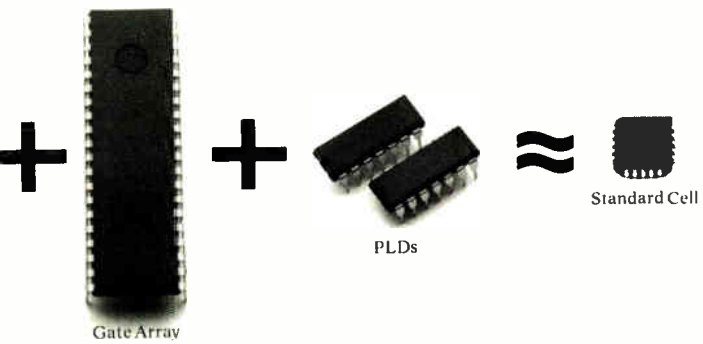
And now Sierra Semiconductor can put more on a chip – analog, digital, plus E^2 functions that replace dip switches and potentiometers – for less than ever before.

How much less? Enough to make our prototyping time and costs competitive with gate arrays.

Enough less to finally make your self-adapting and remotely-maintainable DP, telecommunication and control systems competitive in the market.

The secret? To combine analog, digital and E^2 on a chip, we embed E^2 circuitry in digital flip-flop and latch cells, then provide

Math.



high-voltage generation and timing cells to program them. The result's a price-competitive replacement for dip switches and pots: an E²PROM cell that's as easy to use as a flip-flop. That requires no special testing.

And is available only from us.

Only Sierra offers an E² library. Plus over 250 digital cells. More than 30 analog cells. Plus companion compiler and megacells.

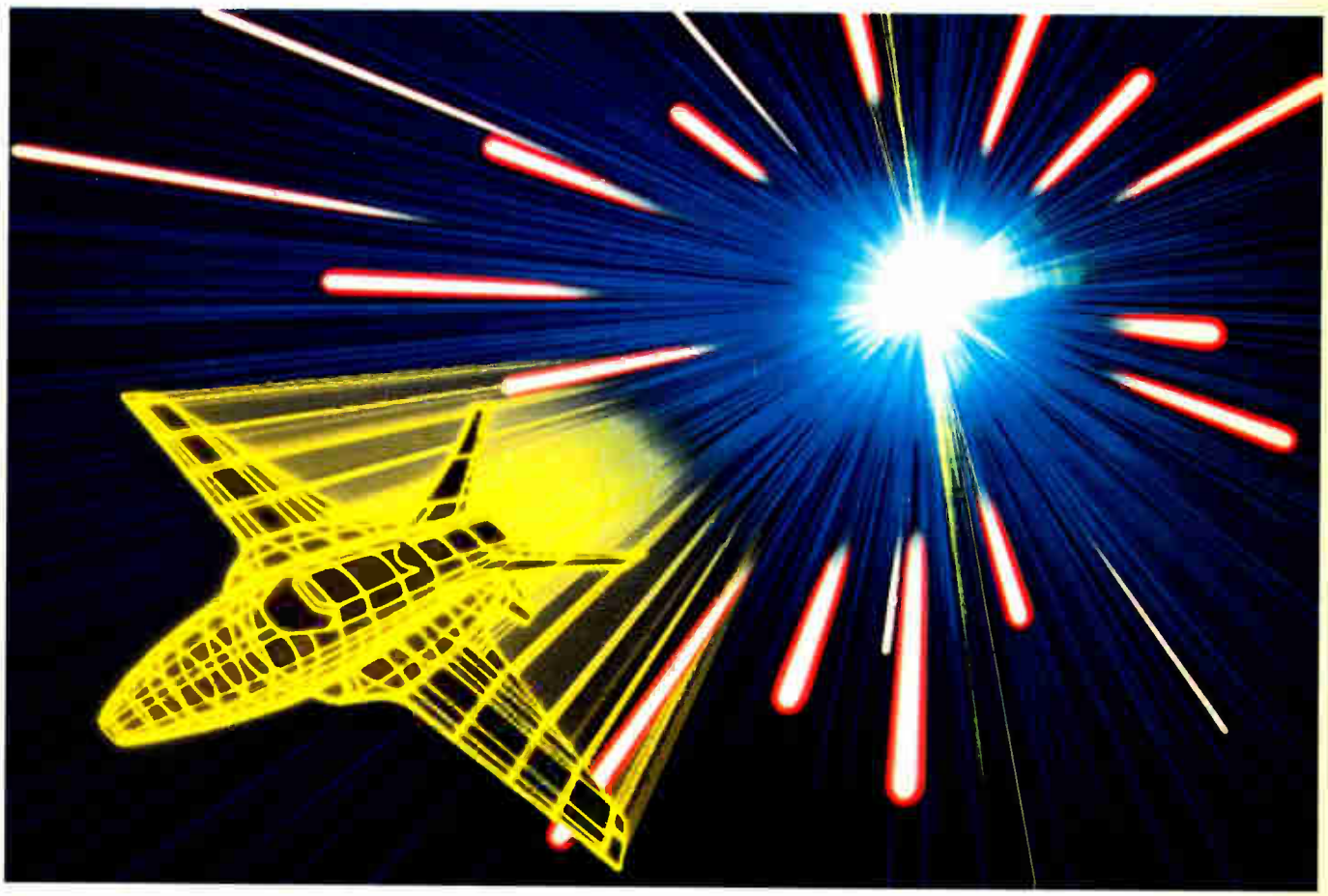
And the complete schematic-to-test CAD, training and sub-2-micron CMOS manufacturing you need along with them.

Add it all up. You'll find our commitment to cell-based design exceeds the sum of its parts. And if you're considering an ASIC, that's more than enough reason to call Sierra Semiconductor, (408) 263-9300. 2075 N. Capitol Ave., San Jose, CA 95123.

Sierra Semiconductor
Custom Technology Standard.

Circle 65 on reader service card

NEC NEWSCOPE



NEC INTRODUCES WORLD'S FASTEST FLOATING-POINT SIGNAL PROCESSOR.

Our μPD77230 Advanced Signal Processor breaks the floating-point barrier in digital signal processing (DSP) with unprecedented speed and accuracy.

The new single-chip CMOS DSP races through 32-bit full floating-point arithmetic at 13.4 MFLOPS. It executes up to 6 concurrent operations, including multiply and accumulate, in a 150ns cycle.

With 32-bit floating-point precision, our advanced signal processor eliminates problems with round-off error, quantization noise, scaling, limit cycles and over/underflow. It is unique in offering a 55-bit multiplier result (8-bit exponent, 47-bit mantissa), with eight 55-bit registers, 47-bit ALU and barrel shifter.

In addition to its large internal memory blocks (512 × 32 × 2 data RAM, 2K × 32 program ROM and 1K × 32 data ROM), the 77230 provides external expansion up to 4K of program RAM and 8K of data RAM. Serial and parallel I/O also add flexibility. The serial interface allows cascading, links with codecs and AD converters while the parallel interface supports master- and slave-mode operations.

The 77230 is ideal for image processing, graphics workstations, telecom and other applications requiring high speed and high precision.

NUMBER 135

NEW ZEALAND GOES DIGITAL WITH NEW FOTS AND NEAX61.

Plans for a nationwide Integrated Digital Network (IDN) in New Zealand, where the telephone ownership rate is among the highest in the world, are rapidly taking shape.

The New Zealand Post Office selected NEC to supply state-of-the-art 140MB fiber optic transmission systems (FOTS) and digital switches that will bring the digital future clearly into view.

NEC will provide all the necessary optical terminal and repeater equipment for the fiber optic systems to be installed in links covering Wellington, Auckland, and other major cities.

NEC's 140MB FOTS provides high-quality communications paths equivalent to 1,920 telephone channels. High-performance optical devices enable long repeater span. It also features in-service system monitoring functions, low power consumption and compact size. A slim rack, measuring 2.75m(H) × 0.12m(W) × 0.225m(D), accommodates three terminal systems.

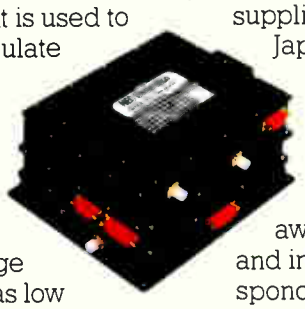
For the development of its ISDN, the New Zealand Post Office selected NEC's enhanced NEAX61 digital switching system with ISDN capability. Nearly 100 systems, including toll and international switches, are to be supplied within a five-year period.

NEAX61 digital switches with an aggregate total of 5 million lines are now in service in 36 countries.

NEC TRANSPONDERS SELECTED FOR INMARSAT-2.

NEC satellite transponders will play a key role in INMARSAT-2, the second generation of international maritime communications satellites.

NEC was recently awarded a contract from British Aerospace Public Limited Company to supply TT&C C-band transponders. This technology-intensive equipment is used to receive and demodulate telecommand signals, to transmit telemetry signals, and for ranging.



The transponder design will include various leading-edge technologies such as low noise amplifiers (Noise figure: 2.5dB), SAW filters to achieve excellent band-rejection performance (60dB min. ±2MHz from center frequency), threshold extension FM demodulation to achieve high sensitivity, and hybrid microwave ICs to minimize equipment size and weight, plus high-efficiency high-power amplifiers (RF output: 6W min.).

As one of the world's leading suppliers of satellite transponders, NEC has contributed to a number of international programs, supplying hundreds of advanced transponders for INTELSAT-IV, IV-A and VI series of communications satellites.

NEC has also integrated and supplied all the transponders for Japan's communications satellites, including the world's first two Ka-band satellites, and various TT&C (tracking, telemetry and command) transponders.

Additionally, NEC was awarded a contract to develop and integrate high reliability transponders for BS-3a and -3b, Japan's next generation of direct broadcasting satellites.

ALL-SOLID-STATE UHF TV TRANSMITTERS.

The latest 30kW UHF TV transmitter from NEC sets a new standard for high output power in all-solid-state design.

The 30kW transmitter incorporates many enhancements including high-performance exciters, powerful transistor power amplifiers, low-loss RF combiners and high-efficiency switching regulators.

The 1.2kW transistor power amplifier, utilizing reliable, high-power and high-gain (120W typical and 7dB min. at 860MHz) bipolar transistors which were developed in-house, features a remarkably reduced component count—only 1.7 times larger than the conventional 300W PA.

Compared to tube types, the new transmitter features greatly enhanced economy and reliability. Safety and maintainability are also improved, while power consumption is reduced by approximately half.

NEC's new all-solid-state UHF TV transmitter series includes 15kW, 10kW, 5kW and 3kW models. A 30kW system is already in satisfactory operation.

NEC

NEW PRODUCTS

STIMULUS TEAMS WITH SIMULATION TO CUT ASIC DESIGN TIME

HARDWARE ACCELERATOR MODELS MINUTES OF REAL-TIME OPERATION

IKOS Systems Inc. is taking a different approach to validating the design of application-specific ICs—it is adding stimulus generation to logic simulation. A hardware accelerator for most computer-aided-engineering work stations as well as the IBM Corp. Personal Computer AT and PC/XT, the IKOS 800 will bow at next week's Design Automation Conference in Las Vegas.

The combination of these two techniques enables the IKOS 800 to generate comprehensive stimulus programs to thoroughly simulate seconds or even minutes of real-time system operation, says William Loesch, president of the Sunnyvale, Calif., company. Other systems model only a few milliseconds of operation, he says. This makes it possible to quickly find subtle design errors so semicustom IC layouts can be reworked before they are committed to mask tooling, he says.

A key feature of the IKOS 800 is the timing template, a powerful stimulus-programming facility that lets the designer enter timing information graphically, using a standard three-button mouse in much the same way the designer would draw a conventional timing diagram. Dedicated function keys support horizontal and vertical zoom and large-scale cursor movement so a complete timing template can be displayed and easily edited.

WINDOWS. A windowing function displays two timing templates simultaneously. Users can enter and edit time and stimulus patterns in either template. Compared with the usual method of entering timing information as text, says Loesch, this timing-template interface speeds up data entry by several orders of magnitude—from hours and days to seconds and minutes.

The IKOS 800 is a stand-alone unit that measures 24.7 by 13.5 by 22.5 in. Its stimulus-processing hardware accelerator supports up to four separate device channels. The stimulus-processing accelerator interprets complex hierarchical stimulus programs at simulation run-time and feeds them directly into the logic-simulation hardware accelerator.

ASICs NOW. IKOS's system can cut down on the number of ASIC design iterations.

Because the stimulus-processing accelerator interprets at simulation run time, extremely large programs—with up to 10 million I/O events—representing several minutes of real-time operation can be stored in program memory. The entire contents of the resident stimulus program can be presented to the logic-simulation hardware accelerator in less than 10 seconds, Loesch says.

The IKOS 800 also incorporates a logic-simulation hardware accelerator that consists of one to four evaluator boards. Each board can simulate up to 16,000 four-input, one-output primitive logic elements at up to 500,000 events/s in timing mode and five million events/s in unit-delay mode. In addition, each board allows the user to model up to 64-K of RAM or ROM.

ANALYSIS. Yet another component of the IKOS 800 is a real-time logic analyzer, which allows state changes on the selected signals to be saved and displayed only for a window of interest around the breakpoint. The analyzer supports up to 20 breakpoints that can be expressed as multivalued functions of input signals, internal signals, and output signals. Analyzer output can be in either timing or state mode.

Loesch says the IKOS 800 will accept semicustom netlists in a variety of formats. It uses a proprietary netlist compiler that combines user netlist information with semicustom library data to create a device-specific data base for simulation purposes. To minimize the time it takes to compile a netlist, the IKOS 800 catches the appropriate semicustom library data in high-speed internal random-access memory. To be available in July, the IKOS 800 is priced at $40,000. *–Bernard Conrad Cole*

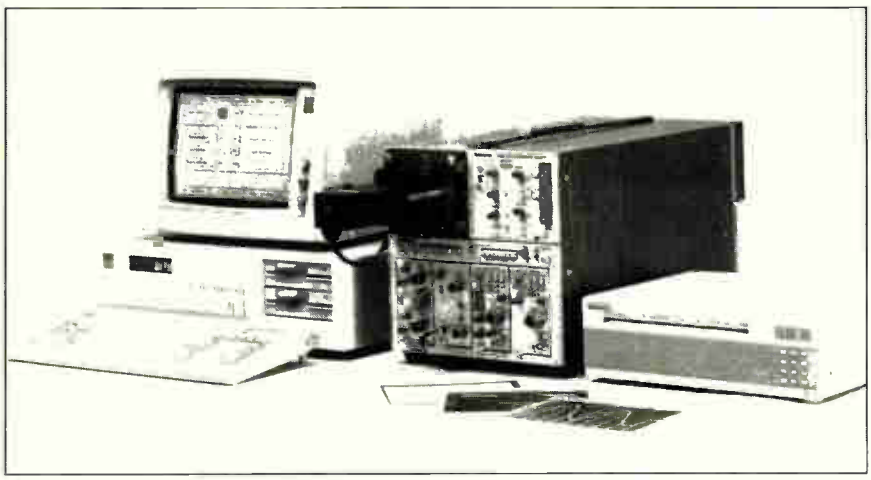
IKOS Systems Inc., 1220 Crossman Ave., Sunnyvale, Calif., 94089. Phone (408) 734-5211 [Circle reader service number 338]

CAMERA DIGITIZES FAST ANALOG-SCOPE SIGNALS

Tektronix has a new solution to the problem of digitizing fast signals from an analog scope. It is introducing a camera that digitizes the captured signal for use by both a computer and a hard-copy-output device. In addition, Tektronix is unveiling two video copiers that provide high-speed, high-resolution, black-and-white paper prints of waveforms or graphics displayed on the scope's CRT.

In introducing the digitizing camera and video copiers, Tektronix is reaffirming its commitment to the analog-scope market, which has been largely abandoned by Hewlett-Packard Co. According to Tektronix figures, analog scopes still make up 68% of the scope market.

The Digital Camera System is targeted mainly at high-performance analog scopes in the 100-MHz to 1-GHz range. At this level, the digitizers common-



PC VERSATILITY. The IBM PC gives Tektronix' digitizing camera system a variety of features.

ly used to obtain digital data from an analog scope begin to run out of steam. The system captures 1-GHz single-shot events, and it samples at 2 GHz.

The inability of digitizers to capture fast analog signals is only one of their drawbacks in converting scope data. Aperture uncertainty causes jitter, and the fastest digitizers are much more costly than the roughly $5,000 price of the camera. In addition, until now the only hard-copy output users could get was film, from scope cameras such as Tektronix' own C30 family of products.

MANY USES. The new camera system combines both the digitizing and hard-copy-output functions so users can capture and digitize a signal, pass it to a computer for later analysis, and then produce a hard copy. Or users can send a graphic image from the computer to the scope so the camera can capture it for hard-copy output on the video copier. And because the system includes an RS-170 video interface, digitized waveforms can be stored on video tape or displayed on a video monitor. The latter application is useful in educational settings where the scope's CRT is too small to be seen by a full classroom of people.

The basic software package, which runs on the IBM Corp. Personal Computer, includes a calibration function for correction of digitized waveforms, a save-on-delta function that allows comparative tolerances to be set for transient analysis of waveforms, and a set of system-maintenance and self-diagnostic functions. Standard waveform-analysis functions such as rise time, fall time, area under the curve, waveform differential, and delta time between two points are also included. Graphics routines for manipulating displayed waveforms include a zoom function that allows enlargement of a target area and a text function that lets users label waveforms.

The system consists of a charge-coupled-device camera, a frame-store card that plugs into the IBM PC, and the optional video copier. Connecting to the scope's bezel like a conventional CRT camera, the system's video camera reads the light given off by the CRT phosphor and transmits a video signal to the frame-store card for analog-to-digital conversion.

The frame-store card has a 512-by-512-by-8-bit resolution. It stores the video image and strips off the waveform. The camera is effective to the full bandwidth on both single-shot events and repetitive waveforms of any of Tektronix' Microchannel plate scopes. On other scopes made by Tektronix or its competitors, the camera is effective to one half the bandwidth for single-shot events and the full bandwidth on repetitive signals.

The camera uses a wide-angle (33°) lens with an aperture of 1.3 and a 10.5-mm focal length. The lens is made of special optical glasses that have a distortion of only 0.3%, compared with the 3% distortion of popular camera lenses.

TRIGGER. To capture what's on the screen, the user can trigger the camera or can set it to use the same trigger-on-delta feature found on digital scopes. Trigger-on-delta features make the scope and camera take a sample when a waveform is outside of set limits.

The video copiers, capable of 16 levels of gray scale, accurately reproduce halftones and generate intermediate levels by electronic dithering. RAM stores video images of up to 640 dots by 512 lines. Photographic-quality prints on thermal paper measuring 4 by 5 in. are available from the HC01 in 17 seconds, and prints measuring 8 by 10 in. are available from the HC02 in 21 seconds. By comparison, prints made by film-based systems take minutes. In addition, prints from the video copiers are cheaper, at 6¢ for the HC01 and 35¢ for the HC02, compared with 75¢ each for film prints.

To use the Digitizing Camera System, the IBM PC must be equipped with 384-K bytes of memory, a 360-K-byte floppy disk, a numerical coprocessor, and an Enhanced Graphics Card. A 10-megabyte disk drive is recommended. In addition, if the PC is equipped with a card that turns it into an IEEE-488 instrument controller, it can be used to run the scope and the camera.

The camera sells for $5,395. The HC01 and HC02 video copiers are priced at $980 and $1,275 each. The camera is available four weeks after ordering, and the copiers are available now. *–Steve Zollo*

Tektronix Inc., P. O. Box 1700, Beaverton, Ore. 97005.
Phone (800) 547-1512 [Circle 339]

ENCODER-DECODER FITS IN STARLAN NETS

The SL4000 CMOS encoder-decoder chip is designed for Starlan local-area networks. Within Starlan, the chip enables conversion of Ethernet or Cheapernet controller boards to the 1-Mb/s data-rate protocol specified in the IEEE 802.3 draft for CSMD/CD local nets. The SL4000, can also be designed into the Starlan hub for carrier sensing, collision detection, and jitter removal.

The SL4000 encoder-decoder is available now in 20-pin DIPs. In hundreds, the chip sells for $15 each.

Semicustom Logic Inc., 50 W. Brokaw St., No. 64, San Jose, Calif. 95110.
Phone (408) 279-4441 [Circle 350]

CONTROLLER CHIP RUNS JOYSTICKS

The L2001-DJ controller chip is designed to work with joysticks using optical encoders in two or three axes. The chip includes a complete high-resolution quadrature-decoding capability suitable for all Apple computers. The joystick may be programmed to emulate a mouse or a tablet. Output is identical to that of the Mouse Systems optical mice,

the Summagraphics MM series of data tablets, or quadrature mice.

The L2001-DJ supports rates from 75 to 75,000 baud. Programmable characteristics include autocentering with center reset, step size and tablet space limits—independent in X, Y, and Z axes—and timing for quadrature mice.

In the low-power mode, the average consumption of the CMOS chip is reduced to 300 μA. The unit price is $25, and quantity discounts are offered. Both military and commercial versions are available. Evaluation boards are available for $110; a 5-V power supply is $20.

Lightgate, 6300 Telegraph Ave., Oakland, Calif. 94609.
Phone (415) 653-8500 [Circle 351]

MULTIPLIER GIVES RESULTS IN 65 NS

A 16-by-16-bit CMOS multiplier-accumulator boasts a 65-ns multiply-accumulate time. The model TMC2210 performs selectable accumulation, subtraction, rounding, and preloading as well as 2's complement or unsigned magnitude operation. All inputs and outputs are registered and TTL compatible.

Typical applications are array, video, and radar signal processing. The TMC-2210 also performs as an accelerator in micro- and minicomputers. Available in plastic and ceramic DIPs, the multiplier-accumulator, which uses just a single 5-V supply, is priced at $28 in thousand-piece quantities.

TRW Inc., Electronic Components Group, LSI Products Division, P. O. Box 2472, La Jolla, Calif. 92038.
Phone (619) 457-1000 [Circle 352]

VTI's GENERIC ARRAYS MIMIC PALs

VLSI Technology is bringing out a line of CMOS 20- and 24-pin generic logic arrays. The arrays can be configured to replace at least 32 different programmable-array-logic parts, the company says. The flexible architecture of GAL lets it handle special applications such as the 16R5 programmable logic architecture that can't be implemented with a PAL.

The GALs are produced in CMOS plus electrically erasable floating-gate technology. Both come in versions with a 25-ns or 35-ns access time and use a maximum of 90 mA.

The 20-pin VP16V8E-25 costs $3.07 in hundreds; the 24-pin VP20V8E-25 costs $3.78 in hundreds. Both parts, which are second sources for Lattice Semiconductor Corp.'s GALs, are available now.

VLSI Technology Inc., 1109 McKay Dr., San Jose, Calif. 95131.
Phone (408) 942-1810 [Circle 353]

WORK STATION ALSO RUNS INSTRUMENTS

The System 488 computer for scientific and engineering applications combines an engineering work station and instrument controller in one unit. The system, which is compatible with the IBM Corp. Personal Computer AT, has a display-interface board with built-in text, monochrome and color graphics, and IBM's Enhanced Graphics Adapter standard.

Instrument-control programming tools for the IEEE-488 standard include an interactive software-development program called Co-Operator and a graphics emulator that features the type of graphics commands used on the Hewlett-Packard Co. Series 80 computer terminals. The system's firmware support eliminates configuration files and device drivers.

System 488 hardware includes an 8-MHz Intel 80286 processor, 512-K bytes of RAM, the display interface, a combined hard-disk and floppy-disk interface, a 1.2-megabyte floppy drive, and a tilt-and-swivel monochrome monitor. Options include additional RAM, ROM, serial ports, hard- and floppy-disk storage, and an enhanced color monitor.

Software includes IEEE-488 applications software, HP-85 graphics emulation, word-processing and Superkey key-programming software, DOS 3.1, and Basic.

System 488 is available now and sells for $3,980.

Capital Equipment Corp., 99 S. Bedford St., No. 107, Burlington, Mass. 01803.
Phone (617) 273-1818 [Circle 354]

RIDGE ADDS HIGH-END RISC SYSTEMS

Ridge is topping its line of superminicomputers with more products based on a reduced-instruction-set-computer architecture. The 3200 model 90 meets the standard that market researcher Dataquest Inc., San Jose, Calif., has defined for the high-availability category, in which critical portions of the computer, such as disks and CPUs, are redundant. A high-availability system should take no longer than 30 minutes to recover from a fault without losing any data. For further reliability, the 3200 model 90 provides automatic single-bit error correction and double-bit error detection in main memory.

As a server for engineering work groups, the 3200 model 90 supports more than 100 users while also performing the floating-point calculations that large simulation tasks require. Integer applications, such as compilation, run in excess of 5 million instructions/s, and in burst mode the sustained I/O transfer rate is 18.3 megabytes/s.

The basic configuration has 4 megabytes of main memory, a 78-megabyte hard disk, eight RS-232-C ports, and a ¼-in. tape-cartridge backup for $36,650. The maximum configuration, with 16 RS-232-C ports expandable to 32, sells for $77,000. The 3200 model 90 will be available in July.

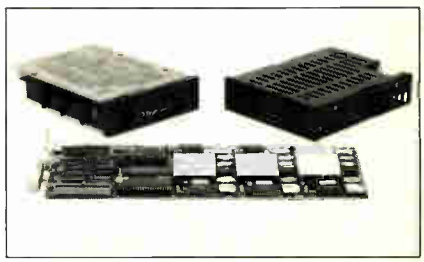
Ridge Computers, 2451 Mission College Blvd., Santa Clara, Calif. 95054.
Phone (408) 986-8500 [Circle 355]

BUBBLE-MEMORY CARD FITS ON IBM PCs

The Solidrive family provides up to 9.5 megabytes of bubble memory for IBM Corp. Personal Computers and industrial computers. The full-size board comes with an expansion bus connector and up to 1.5 megabytes of bubble memory. Expansion packs add 1 or 2 megabytes of bubble memory, and cartridge subsystems contain up to 0.5 megabyte of removable bubble memory. Expansion units can be daisy-chained.

Other features of the board include an RS-232-C communications port, a password protection scheme, and a built-in test. Typical power dissipation of a 1-megabyte system is 8.9 W. Solidrive requires no user-written software.

The board comes in standard and extended temperature-range versions. Prices for the standard model range from $1,195 to $2,955 in quantities of 50. Expansion packs are $1,995 and $3,915.



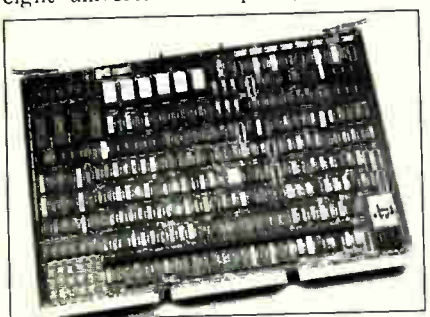
MICROSYSTEMS □ ROBOTS

Removable bubble cartridges are $1,275, and the cartridge holder sells for $315. Units are available now.
Targa Electronics Systems Inc., P. O. Box 8485, Ottawa, Ont., Canada K1G 3H9. Phone (800) 267-9793; in Canada, (613) 731-9941 [Circle 369]

CONTROLLER MOVES 3 MEGABYTES A SECOND

The SC7003 disk controller integrates disk drives with a Storage Module Device or Extended Storage Module Device interface. It has drive capacities from 80 to 850 megabytes and transfer rates from 1.2 to 3 megabytes/s.

The controller features transparent operation and media compatibility, up to eight universal drive ports, and a 28-

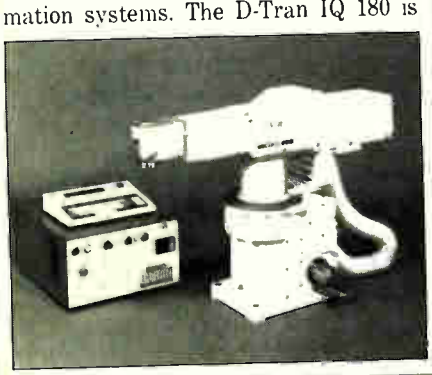


sector RAM buffer. In a cluster environment, a system disk can reside on the same board as shared-data disks. The SC7003 operates in several Digital Equipment Corp. VAX environments.

Scheduled to become available this month, the SC7003 lists for $8,950.
Emulex Corp., P. O. Box 6725, Costa Mesa, Calif. 92626.
Phone (714) 662-5600 [Circle 370]

CONTROLLER DIRECTS TWO ROBOTS

The D-Tran IQ 180 controller can direct two robots, vision systems, I/O sensors, conveyors, numerical control machines, or any other device within a work cell. Intended for light assembly and test applications, the controller replaces personal computers or programmable controllers currently used in factory automation systems. The D-Tran IQ 180 is



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built around the VMEbus.

Expansion slots allow users to select such options as a Manufacturing Automation Protocol interface, a printer interface, 16 megabytes of memory expansion, and I/O expansion cards. The controller can be retrofitted to other robots from the same manufacturer as well as to Z-80-based controllers. The controller can be programmed in a structured Basic that resembles Pascal; in addition, the high-level language accepts calls to external procedures written in Basic, C, or assembly language.

The company will quote price and delivery schedules.

Seiko Instruments USA Inc., Robotics/Automation Division, 2990 W. Lomita Blvd., Torrance, Calif. 90505.
Phone (213) 530-8777 [Circle 357]

5¼-IN. OPTICAL DISK PACKS 220 MEGABYTES

A 5¼-in. write-once optical storage system equipped with the Small Computer Systems Interface gives systems integrators 200 megabytes of storage capacity per disk. The system features 1 : 1 interleaving and multitrack buffering. In addition, the controller has an error-correction-code chip that requires overhead of only 9.4% to correct up to 24 bad bytes per sector. During disk formatting, surface analysis locates about 95% of unusable sectors.

The drive, which has a data-transfer rate of 2.2 Mb/s, comes with software tools, including device drivers for popular operating systems. Up to four drives can be connected to a single controller, providing as much as 800 megabytes of on-line storage. The system uses removable cartridges and has an average access time of 195 ms.

Evaluation kits, priced at $5,000, will be available by early July. In volume production, the drives will sell for $975 to $3,400, depending on quantity, and the controllers will go for $350 to $650.

Optotech Inc., 770 Wooten Rd., Colorado Springs, Colo. 80905.
Phone (303) 570-7500 [Circle 366]

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NEW LITERATURE

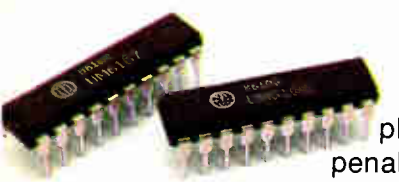
SPECTRUM ANALYZER. A 24-page color brochure describes the model 1201 fast-Fourier-transform spectrum analyzer. In the brochure, the company gives the theory behind signal processing and a number of application techniques. These include modal analysis of structures using integrated software, acoustic measurement of complex sound fields, and rotating-machinery diagnosis. The 1201 spectrum analyzer, which offers 500 lines of dual-channel resolution and a 30-kHz bandwidth, has been optimized for low-frequency analysis. Copies of the free brochure are available from Solartron Instruments, 2 Westchester Plaza, Elmsford, N. Y. 10523. Phone (914) 592-9168. [Circle reader service number 421]

LASERS. A brochure describes the experiments and capabilities of the XLR-100 Excimer Laser Research Center. Experiments with the laser, whose beam is variable from less than 1.0 μm to 100 μm are being done in semiconductor annealing and thin-film deposition. The XLR-100 delivers "cold" ultraviolet energy that does not damage areas adjacent to the beam. The literature includes a drawing of the system, specifications, and color microphotographs. Free copies are available from Leitz-Image Micro Systems Co., 900 Middlesex Tpke., Building 8, Billerica, Mass. 01821. Phone (617) 663-7070. [Circle 422]

SHORT COURSES. The Laser Institute of America is offering a list of its continuing-education programs through the end of the year. Courses include laser safety, fundamentals and applications of lasers, laser optics and beam propagation, and radiometric and photometric measurements. For information, call the institute at (419) 882-8706 or write to the Education Director, Laser Institute of America, 5151 Monroe St., Suite 102W, Toledo, Ohio 43623. [Circle 424]

Score A Winning Touchdown with UMC

With backing from UNITED MICROELECTRONICS CORPORATION, one of our customers scored a winning touchdown with a voice control IC last year. He netted a profit of 2.5 million dollars on just one product. This is one of the many examples of how UMC helps its customers score financial goals.



UMC scored its first touchdown by becoming profitable 6 months after it went into operation and has been making a profit and registering phenomenal sales growth annually since then. Last year, 4 quarters of penalties left most companies sitting on the bench and several others were ejected from the game. UMC, however, still romped to a sales growth rate of 24.4%, which was the fourth best in the world and outscored 92% of the IC industry.

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* Advertisers in Electronics International
‡ Advertisers in Electronics domestic edition

ELECTRONICS WEEK

AMD SCHEDULES 25-NS 64-K SRAM

Advanced Micro Devices Inc. has joined the race for the fastest 64-K static random-access memory. During the third quarter, AMD will make available a 25-ns version of its Am99C641, a 64-K-by-1-bit CMOS SRAM. The Sunnyvale, Calif., company is the latest U. S. chip maker to enter the derby, joining Lattice Semiconductor Corp. of Portland, Ore., and Cypress Semiconductor Corp. of San Jose, Calif. [*Electronics*, June 16, 1986, p. 17]. The CMOS part being introduced this week has a maximum access time of 35 ns and will cost $50.75 each in 100-piece quantities. It has an active power dissipation of 715 mW and is housed in a 22-pin ceramic dual in-line package.

PACEMAKER SETS ITS OWN BEAT

Medtronic Inc. of Minneapolis has received approval from the U. S. Food and Drug Administration to begin marketing what's billed as the first single-chamber pacemaker designed to detect body movement and automatically increase or decrease paced heart rates accordingly. Called Activitrax, the new pacemaker relies on a piezoelectric quartz sensing crystal that is bonded to the inside of the unit's titanium shell. When pressure waves from body activity stress it only a few millionths of an inch, the crystal produces an electrical current that signals the pacemaker's microprocessor to alter the heart rate accordingly, in a range from 60 beats up to 150 beats per minute.

PHILIPS, TAIWAN JOIN IN VLSI DEAL

Philips Electronics Industries Ltd., the Netherlands, is tying up with Taiwan's Industrial Technology Research Institute in a $207 million project to produce very large-scale integrated circuits. Taiwan will have a 48.3% share in the venture, which will result in the construction of a production plant at Hsinchu Industrial Park, north of Taipei. The Dutch multinational sees the arrangement as a way to lower its production costs to better compete with Japanese and U. S. IC manufacturers.

SIEMENS BUYS SITE IN SILICON VALLEY

Siemens Components Inc., the U. S. arm of Siemens AG of Munich, is going to consolidate in Silicon Valley the manufacturing operations of its Semiconductor Group's three divisions. It has bought a 98,000-ft² facility in Santa Clara, Calif., to house its Power Semiconductor Division, now in Broomfield, Colo., and its IC Operation, now in Iselin, N. J. The Optoelectronics Division will stay in the Silicon Valley city of Cupertino.

CASIO TV SCREEN IS 0.54 IN. THICK

Casio Computer Co.'s latest pocket TV set has the thinnest liquid-crystal display yet marketed. The 2-in. screen, measuring 139 by 110 pixels, is just 0.54 in. thick. The set, called the TV-70, weighs 5 oz and can receive both very high- and ultrahigh-frequency channels. Priced at $134 in the Japanese market (export prices will depend on future exchange rates), the new model will be produced at the rate of 10,000 units/month.

FUJITSU SUPPLYING AT&T PRINTER

Fujitsu America Inc. will supply AT&T Information Systems with a 24-wire multifunctional dot-matrix printer under the terms of a recently signed original-equipment-manufacturer contract. The value of the deal was not disclosed. The printer, from Fujitsu's Peripheral Products Division in San Jose, Calif., has been customized and will be sold as the AT&T Model 477. The Fujitsu machine will be the first multifunctional color printer to be sold by AT&T.

ZYCAD, HHB SIGN DEVELOPMENT DEAL

Zycad Inc., the St. Paul, Minn., vendor of simulation hardware accelerators, has hooked up with HHB Systems Inc. in a deal that could make things tougher for Zycad competitor Silicon Solutions Corp. HHB, of Mahwah, N. J., supplies simulation systems; it and Zycad have agreed to develop an interface between HHB's popular Cadet simulator and Cats Modeler and Zycad's products. HHB has been linked to Silicon Solutions, but a lawsuit filed against HHB by the Menlo Park, Calif., company has soured relations between the firms.

SMC TO INTRODUCE A PRODUCT A WEEK

At least 52 new standard MOS very large-scale integrated circuits and board-level system products will be introduced by Standard Microsystems Corp. during its current fiscal year, says Arthur Sidorsky, executive vice president. The Hauppauge, N. Y., company has been unveiling one a week since March 1, and says that many will be made with a new 2-μm n-well silicon-gate CMOS technology, which features high density and high speed. The 52-product campaign is similar to the one under way by Advanced Micro Devices Inc. of Sunnyvale, Calif.

NATIONAL CPU SET IN 15-MHz VERSION

National Semiconductor Corp. has begun shipping samples of the 15-MHz version of its NS32332 32-bit central processing unit. The new part provides full Unix capability, says the Santa Clara, Calif., semiconductor maker, and competes with Motorola Inc.'s 68020 and Intel Corp.'s 80386. The first targets of the new CPU are such applications as high-performance laser printers, factory automation and robotics, and aerospace and military systems.

MICROPRO RECORDS $2.4 MILLION LOSS

Micropro International Corp. continues to struggle as it searches for a followup hit to its all-time best-selling word-processor program, WordStar. Last week, the San Rafael, Calif., company reported losses of $2.4 million on sales of only $6.9 million in the quarter ending May 31. A year ago, the company reported a small profit on sales of $10.3 million. Micropro says that part of the current loss is due to provisions for an expected $1.4 million default by First Software, a distributor that recently filed for Chapter 11 protection from its creditors.

2 IC GEAR MAKERS REPORT LOSSES

The return of the chip business is not coming fast enough for two suppliers of fabrication equipment, which now expect to lose money this quarter. Varian Associates Inc. of Palo Alto says it expects to lose from $4 million to $6 million in its third quarter, which ends July 4. It had made a slim $1.7 million on sales of $448.6 million in the first six months of fiscal 1986, and expected significant second half improvement. It lays most of the blame for the expected loss on the Semiconductor Equipment Group, which is experiencing lower sales. Meanwhile, Lam Research Corp., in nearby Fremont, Calif., says it too will lose money in its fourth fiscal quarter, ending June 30. Lam had sales of $33.4 million last year.

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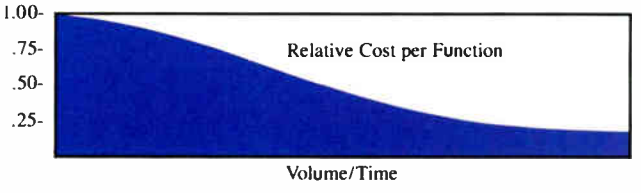

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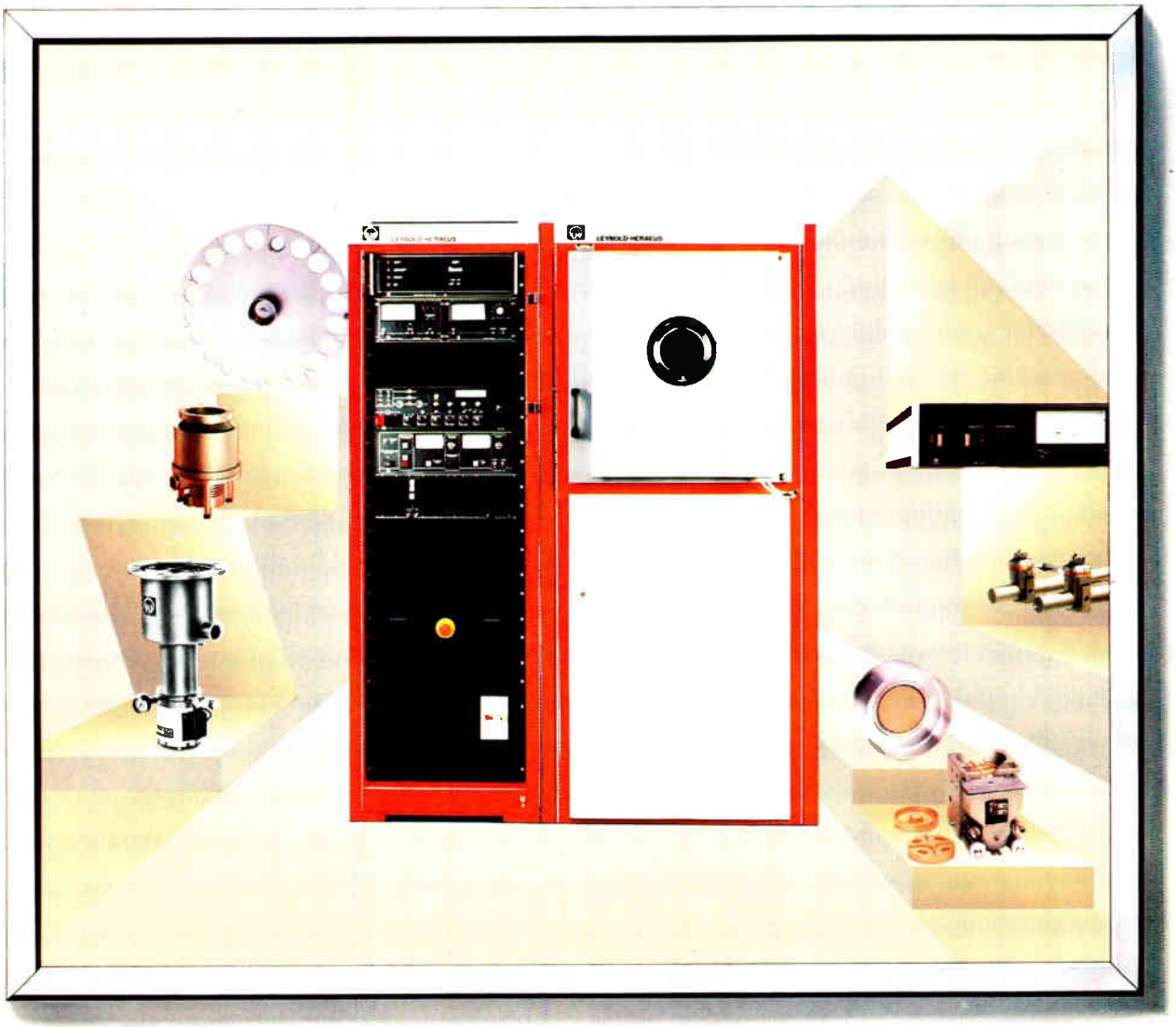

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