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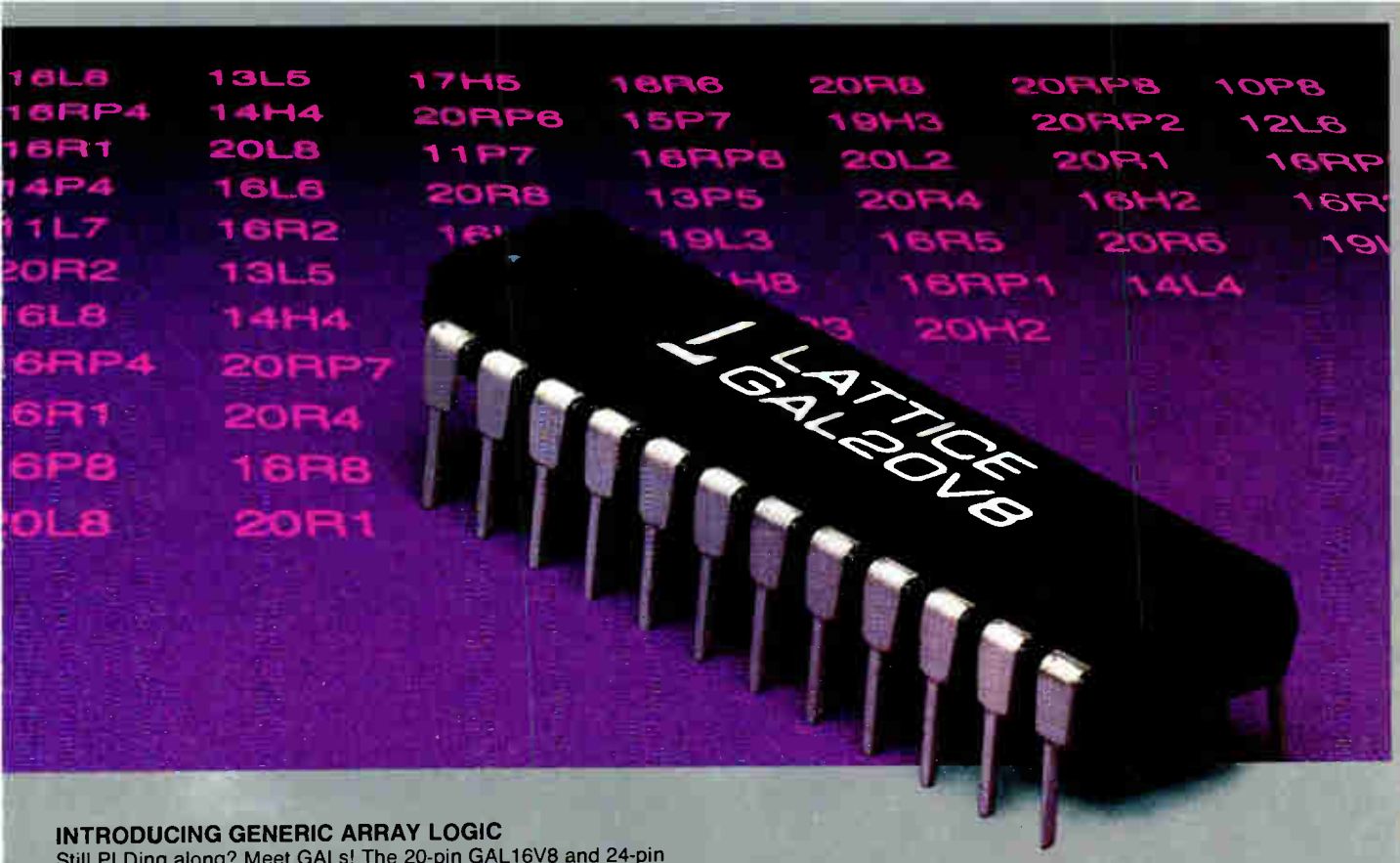
Electronics

THE WORLDWIDE TECHNOLOGY WEEKLY

MAY 26, 1986

HIGH NOON FOR FUJITSU

PAGE 40



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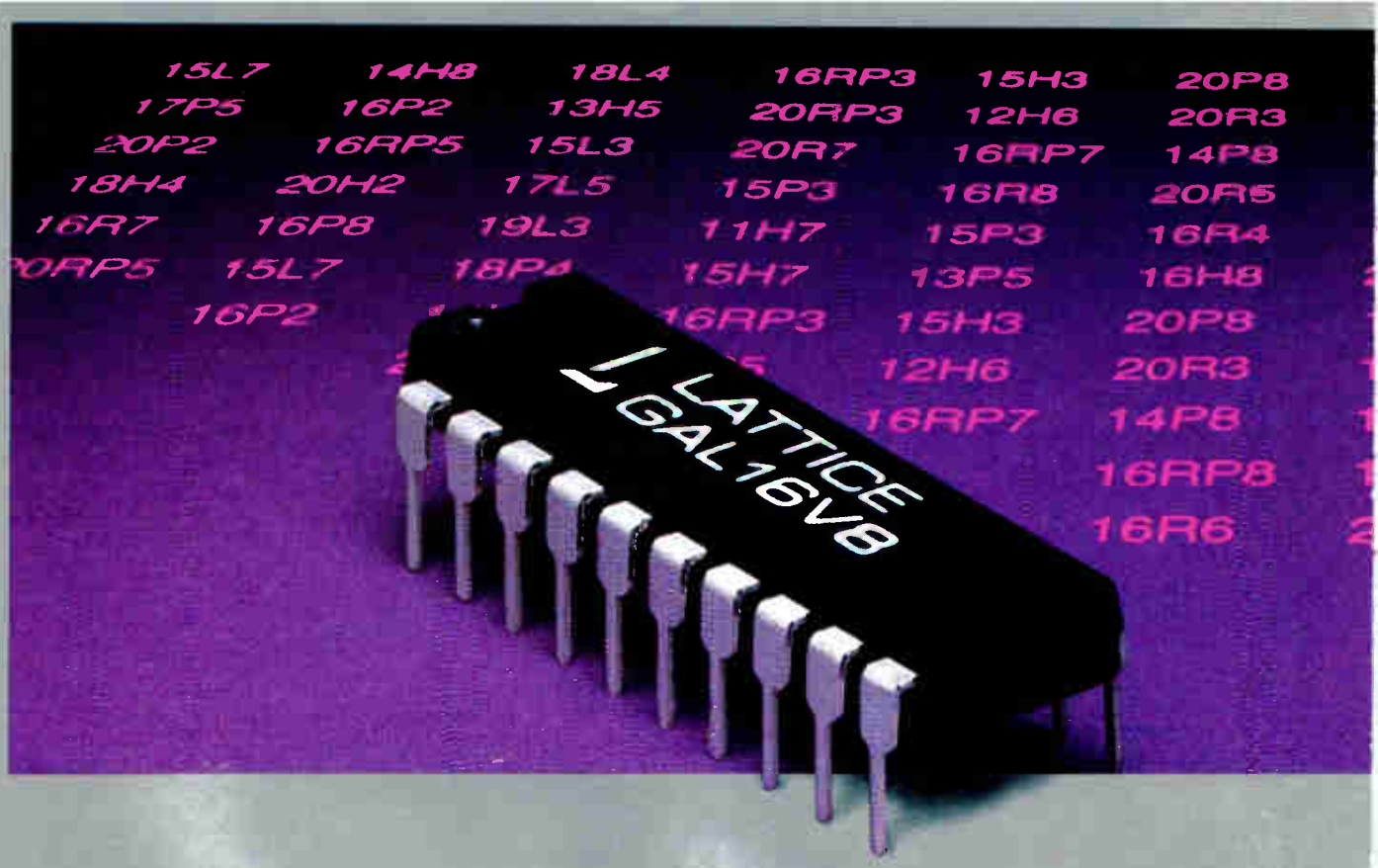

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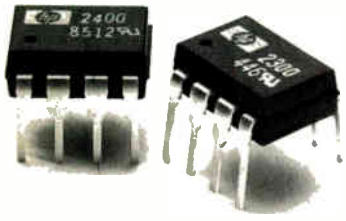

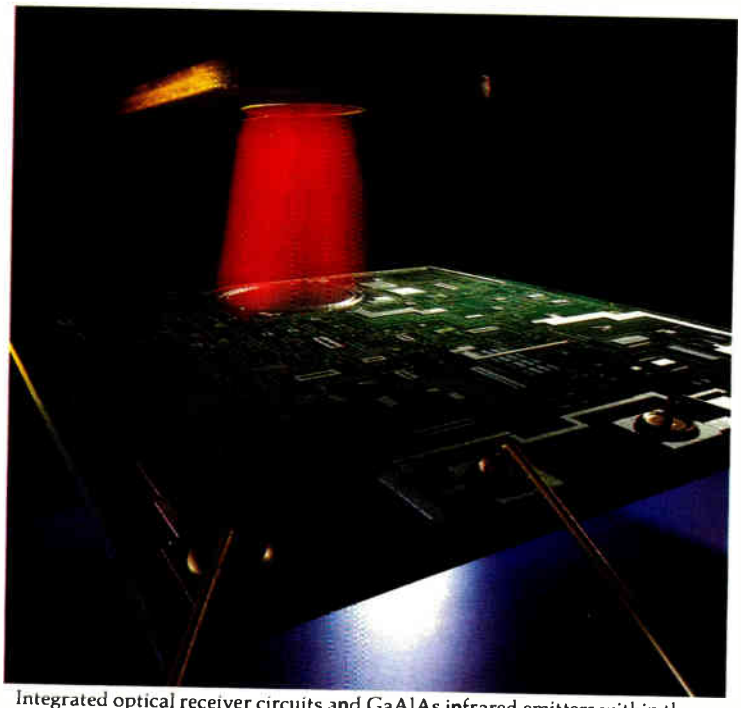

Integrated optical receiver circuits and GaAlAs infrared emitters within the optocoupler provide solutions for high data rate and low power applications.

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For more information, call your local HP sales office. Look in the white pages of your telephone directory and ask for the Components Department.

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MAY 26, 1986 VOLUME 59, NO. 21

Electronics

NEWS

INSIDE TECHNOLOGY

PROBING THE NEWS

COVER

High noon for Fujitsu, 40
IBM's legal attack on Fujitsu, on grounds that Japan's largest mainframe maker is infringing on its software, has the company walking a tightrope. It must devise software that is different from IBM's, yet is still compatible

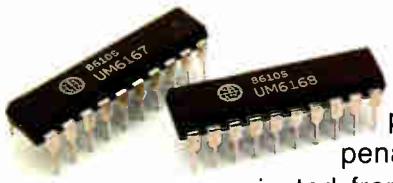
Cover art by Jim Sharpe

NEW PRODUCTS

DEPARTMENTS

Score A Winning Touchdown with UMC

With backing from UNITED MICROELECTRONICS CORPORATION, one of our customers scored a winning touchdown with a voice control IC last year. He netted a profit of 2.5 million dollars on just one product. This is one of the many examples of how UMC helps its customers score financial goals.



UMC scored its first touchdown by becoming profitable 6 months after it went into operation and has been making a profit and registering phenomenal sales growth annually since then. Last year, 4 quarters of penalties left most companies sitting on the bench and several others were ejected from the game. UMC, however, still romped to a sales growth rate of 24.4%, which was the fourth best in the world and outscored 92% of the IC industry.

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We pride ourselves at *Electronics* in having technical editors who can find and report news as well as technology, and news correspondents in the field who can handle a technology report just as smoothly and efficiently as they put together a news story. As a case in point, take Wes Iversen and the Technology to Watch beginning on p. 33, "Checking out VLSI with standard test gear," which covers the latest technology from supercomputer maker ETA Systems Inc.

Wes, a 38-year-old former newspaperman, has been manager of our Chicago bureau since 1981. For a year before that, he held the same title for McGraw-Hill World News. Spending that much time in the Windy City has given him the opportunity to build the contacts and the knowledge to handle such articles. And the challenge of digging deeply into a technology—which he can't do in the relatively limited space of a news story—is something he says he relishes.

Wes also says that he enjoys the change of perspective necessary when switching to the technology section of the magazine. "Not only that, but doing the article helped me get some insights into what the other supercomputer people are doing," he says. "I also like the idea that there is more time to work on an article of that sort."

The piece had its genesis when Wes and senior editor Tom Manuel were in St. Paul, Minn., collecting material for Manuel's special report on supercomputers [*Electronics*, March 10, 1986, p. 44]. When they got to ETA Systems, senior technologist David R. Resnick, the principal designer of what the company calls BEST (for built-in evaluation and self-test) "basically did a two-hour presentation on the self-testing chip scheme," says Wes. "It was a thorough briefing, and Resnick quickly convinced us that this was significant new technology."

Iversen's route to the worlds of magazines and technology took him through the business-reporting side of daily newspapers. He was on the staff of the Dallas *Times-Herald* before joining *Electronics* in 1978 in Dallas. Before that, he worked for the Omaha (Neb.) *Sun* newspapers. He arrived there, newly graduated with a journalism degree from Iowa State University, in time to join a five-person team that received a coveted Pulitzer Prize—and six other national awards—in 1972 for a series of articles on the tangled finances at Father Flanagan's Boys Home, better known as Boys Town.

Says Wes of those early days in the business, "That was quite a heady start for a kid brought up on a farm in Iowa where the nearest town was a place called Shelby. I remember thinking to myself that journalism wasn't a bad profession at all. I also recall wondering why people make all that fuss about winning prestigious awards—heck, here I was fresh out of journalism school and I had a piece of a Pulitzer."

Needless to say, Wes has since learned that it really isn't that easy. He has also developed into a versatile member of our staff, with a reputation as one of the more thorough and accurate reporters covering electronics.

Laurence Altman

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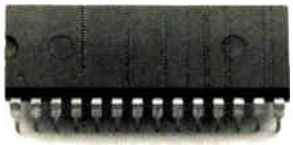
Sierra's controllers, SC11007 for parallel bus and SC11008 for RS232 designs,

Neither does theirs.



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BOOKS

DICTIONARY OF COMPUTING

John Wood, General Editor
IBM Books
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One of six paperback titles from the newly formed IBM Books, *The Dictionary of Computing* is a revised, updated, and illustrated version of the *IBM Vocabulary for Data Processing, Telecommunications, and Office Systems*, which has gone through seven editions under Wood's supervision. Wood is an advisory information developer at IBM Corp.'s Research Triangle Park Facility, Durham, N. C.

IBM has announced that this new department will publish books by IBM authors and others, including *Power Portable Computing, DisplayWrite 3, Networking the PC, Business Graphics with the Personal Computer*, and *Up and Running: Maintaining, Servicing, and Enhancing Your PC*, all scheduled for fall release. IBM Books plans to publish up to 20 titles a year. A department of IBM's North Central Marketing Division, IBM Books is located at 1133 Westchester Ave., White Plains, N. Y. 10604; phone (914) 686-3724.

INTEGRATED PRODUCT TESTING AND EVALUATION

Revised edition
Harold L. Gilmore and Herbert C. Schwartz
Marcel Dekker Inc.
$49.75/350pp

In this revision of their 1968 pioneering work on test and evaluation, the authors point out that though more and more products come to market every year, failure rates remain about the same—an indication of the continuing need for this book. Topics include specific tests and procedures, statistical considerations, and techniques to evaluate product life, and there are many case histories. Software evaluation is covered in 22 pages. Gilmore is a professor of management at Pennsylvania State University-Middletown. Schwartz is senior staff consultant for Avco Systems Division's Safety and Reliability Requirements and Analysis Department.

HOW TO WRITE AND PUBLISH ENGINEERING PAPERS AND REPORTS

Second edition
Herbert B. Michaelson
ISI Press
$21.95 (cloth);
$14.95 (paper)/182pp

In an era of "how-to-write" books that do little more than rehash eighth-grade English, *How to Write and Publish Engineering Papers and Reports* is both an innovative manual and an example of how to approach and create effective technical writing. Professionals will appreciate that Michaelson, formerly associate editor of the *IBM Journal of Research and Development* and now a technical communications consultant, writes as an insider. Thus topics such as the peer-review process and the engineer's place in it, not ordinarily found in style manuals, are included here. Michaelson also deals knowledgeably with the delicate problem of how to work in a high-security organization yet publish results based on confidential data. All in all, this is a manual to use throughout one's professional career.

A GRAPHICAL ENGINEERING AID FOR VLSI SYSTEMS

Paul J. Drongowski
UMI Research Press
$44.95/216pp

This monograph develops an engineering aid for VLSI systems that emphasizes a functional approach to the description, analysis, and synthesis of n-MOS very large-scale integrated circuits. Some experimental software tools were constructed to demonstrate the feasibility of a complete computer-aided design system. The author uses a standard notation, called d-n, to represent a design. Once a common design representation has been created, the tools can be integrated into a self-consistent engineering sketchpad for VLSI design, and the d-n description becomes the reference point for all design tasks. Drongowski, who is a member of the computer engineering and science department of Case Western Reserve University, offers his method as a means of getting a product to market in the least possible time, increasing its reliability, and decreasing nonrecurring engineering costs.

INTERNATIONAL CAD/CAM SOFTWARE DIRECTORY

Philip C. Flora, Editor
TAB Professional and Reference Books
$34/189pp

This paperback directory, one in a series, lists manufacturers' descriptions of their computer-aided design and manufacturing products. The information is derived from the Computerized Manufacturing On-Line Database and includes hardware and software environment, minimum memory required, and delivery medium. Documentation and technical support are also annotated. The directory lists 224 companies, 54 of which offer CAD packages. Other major categories include CAM, graphics, utilities, and manufacturing management. The series also contains directories of engineering and scientific software and of programmable controllers.

TECHNOLOGY NEWSLETTER

32-BIT RISC MICROCONTROLLER GOES TO MARKET NEXT MONTH

The processing power of embedded controllers may be boosted significantly by the use of reduced-instruction-set computing. VLSI Technology Inc., Phoenix, Ariz., plans to offer samples next month of a 32-bit RISC microprocessor originally designed by Acorn Computers Ltd., Cambridge, England. Although the RISC chip is a general-purpose engine, VTI is positioning it against 8- and 16-bit microcontrollers. It can run at speeds roughly equivalent to today's 32-bit microprocessors, such as Motorola Inc.'s 68020. Clocked at 4 million instructions per second, samples will sell for $99 each when available in June. VTI says the 86C010 is fast enough to execute control functions from software rather than relying on dedicated on-chip hardware, as is the case with most microcontrollers. The 84-pin processor, made from 3-μm CMOS, will be targeted at a range of real-time embedded controller applications, including industrial equipment and communications in mainframe systems. Meanwhile, Acorn has three additions to the 32-bit RISC processor family—a video controller, a memory controller, and an input/output controller—forming a chip set that could be designed into a system. □

FINE-TUNING OF BASIC RISC SYSTEM CUTS CYCLE TIME BY A THIRD

By fine-tuning its basic reduced-instruction-set computer, Ridge Computers has cut cycle time by a third and now supports 100 users on its new RISC superminicomputer, the 3200 Model 90. Ridge squeezed the last bit of performance out of discrete logic (Fairchild Semiconductor's FAST TTL) and programmable array logic in a machine that it rates at 5 million instructions/s. Instead of providing a separate processor for floating-point operations, Ridge integrated them into the basic instruction set, which it has kept below 100 instructions. The next model will have a gate-array processor, Ridge says.□

APPLE ENDOWS MACINTOSH PLUS WITH KANJI ABILITY

Apple Computer Inc. is endowing the Japanese version of its Macintosh Plus with the ability to display Japanese kanji characters from phonetic symbols from a keyboard. The Kanji-Talk operating system resides partly on disk and partly in a 1-Mb read-only memory, which includes the kanji font and the logic for processing one- and two-byte characters. Kanji-Talk includes three dictionaries: a 228-K-byte (36,000-word) kanji dictionary, a 40-K-byte special dictionary for industry-specific technical words, and a 40-K-byte dictionary for the user's own additions. The system will sell for 648,000 yen, just under $4,000 at current exchange rates. □

NEW RCA PROCESS HALVES THICKNESS OF GATE-OXIDE LAYER IN FETs

Development of a proprietary gate-oxide deposition process allows RCA Corp. to cut the thickness of the gate oxide layer in power devices it calls logic-level FETs in half, to only 500 Å. The thin oxide level means the L²FETs can be triggered by a 5-V gate rather than the 10-V gates such parts usually need, says Jack Wojslawowicz, engineering manager for power device applications at RCA's Solid State Division, Somerville, N. J. This makes the new parts compatible with both TTL and CMOS, eliminating much of the interface circuitry generally associated with smart power devices. RCA would not give details on the deposition process. Demand for smart power devices is still small, says Paul Thomas, manager of product control for semicustom device operations, mostly because of a lingering perception that they suffer from reliability problems. RCA is hoping, however, that recent government approval—its L²FETs are now on the Qualified Parts List—will "lend credence to the device" and show commercial users that "it's passed the test." □

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IMS1423 4K x 4	25,35,45	660	33 CMOS	CMOS
IMS1600 64K x 1	45,55,70	440	77 CMOS	CMOS
IMS1620 16K x 4	45,55,70	440	77 CMOS	CMOS

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ELECTRONICS NEWSLETTER

NO HDTV STANDARD NOW: A TWO-YEAR STUDY INSTEAD

Disputes among nations did stall high-definition TV standards for another two years, as predicted [*Electronics,* May 12, 1986, p. 19]. The International Radio Consultative Committee's (CCIR) plenary session in Dubrovnik, Yugoslavia, at presstime was expected to pass a motion to establish a special task force to study HDTV for the next two years. The 12 member countries of the European Communities blocked a U. S.-Japanese proposal aimed at adopting Japan's HDTV scheme as a world production standard. Europeans maintain that acceptance of the 60-Hz, 1,125-line system would give the Japanese an unfair advantage and would probably be incompatible with the current European 50-Hz systems. The task force will report to a 1988 CCIR session convened to adopt a standard for both production and transmission. □

KODAK CHARGES INTO THE BATTERY BUSINESS

Eastman Kodak Co. is jumping into the battery business with the introduction last week of a 9-V lithium battery for consumer use. The company claims its lithium battery, the first of its kind to be offered in the consumer market, will have a shelf life of 10 years, an operating lifetime twice that of an alkaline battery, and cost only 1.7 times as much. □

ISDN PICKS UP STEAM AS SOUTHERN BELL LINES UP CUSTOMERS

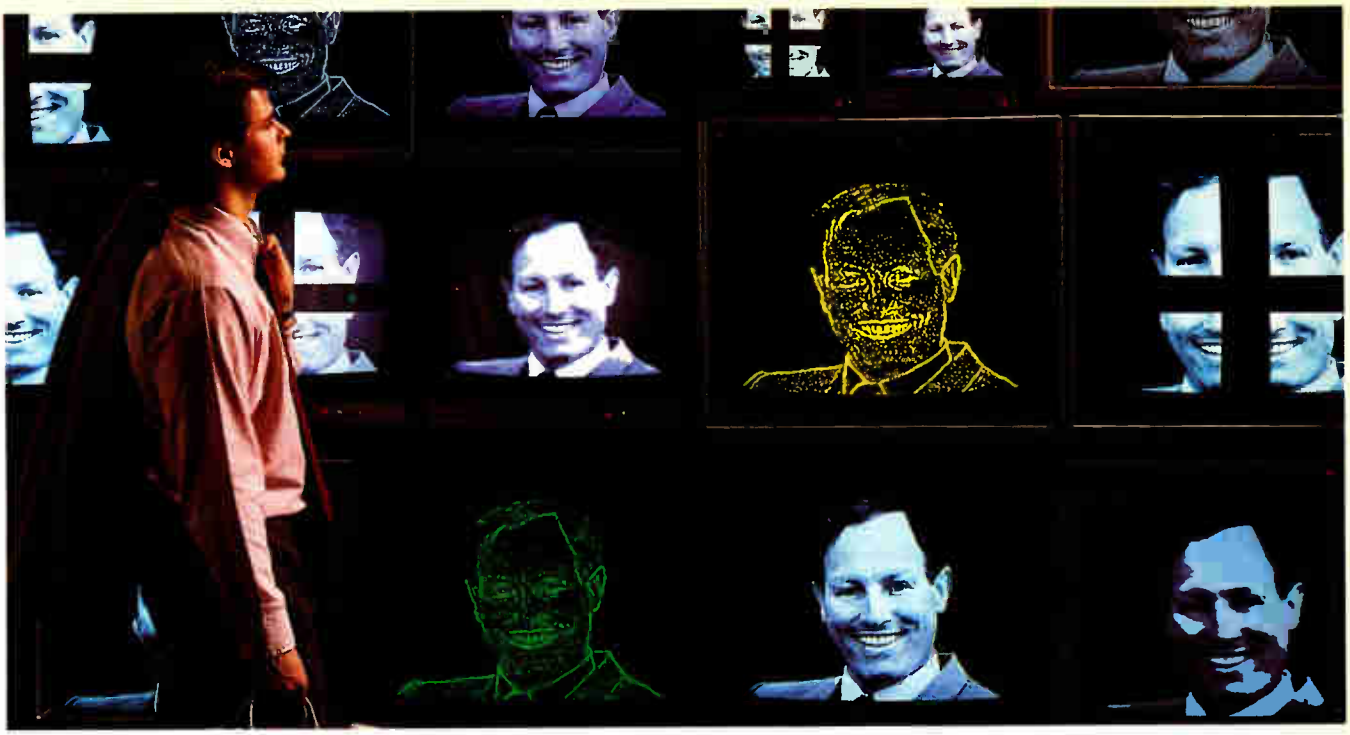
A second U. S. integrated-services digital network is getting off the ground, this one at Southern Bell Telephone Co. The Atlanta-based subsidiary of BellSouth Corp. announced that it has lined up its first two ISDN customers: Prime Computer Inc. and Trust Company of Georgia. They are scheduled to begin transmitting voice and data traffic over an ISDN in the Atlanta area by March 1988. The only other Bell operating company with a ISDN customer is Illinois Bell, which announced the signing of McDonald's Corp. last April. One hangup: standards bodies have yet to reach a consensus on ISDN issues such as signaling standards. James Fitzgerald, Prime's ISDN product manager, says it will use the network for customer service applications and to link branch local-area networks in Atlanta to nets in Natick, Mass. Trust Company of Georgia expects to connect all of its services with ISDN. □

TEKTRONIX WILL CUT ITS WORK FORCE BY 10%

Faced with still-slumping sales and no immediate prospect of an upturn, Tektronix Inc. says that it plans to cut its work force of 19,747 by 10% over the next three months. For the first 41 weeks of its current fiscal year, the Beaverton, Ore., company reported sales of $1.01 billion, down 7%, and earnings of $31.8 million, down 48% from the year-ago period. Tektronix will first offer financial incentives for employees who quit voluntarily. But if the goal of 2,000 is not reached by July 14, it says it will begin layoffs. □

NTT WILL USE DIGITAL SWITCHES FROM NORTHERN TELECOM

In early 1988, Nippon Telegraph & Telephone Corp. of Tokyo expects to begin services that make use of Northern Telecom Inc.'s DMS-10 digital switches. The Research Triangle Park, N. C., company's DMS-10 is a fully-digitized central office switch that can handle 10,000 subscribers. NTT last week announced a $250 million contract for purchase of the switches. "This contract represents the largest single order placed with a foreign company since the introduction of open, fair, and non-discriminatory procurement procedures by NTT in 1981," says Hisashi Shinto, president of NTT. □



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DT2851 + DT2858 High Resolution Frame Grabber and Auxiliary Frame Processor	IBM PC AT	512x512	256			Yes	8*			2 buffers, 512x512x8 each (512 Kbytes), and 1 buffer, 512x512x16 (512 Kbytes)	Yes	Yes	Yes	Yes	DT-IRIS	DT2851 $2995 / DT2858 $1495
DT2603 Low Cost Frame Grabber	MicroVAX II	256x256	64	▼	▼		4	▼	▼	1 buffer 256x256x8 (64 Kbytes)					Coming Soon	$1895

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PRODUCTS NEWSLETTER

TOSHIBA ENTERS 1-MB EPROM MARKET

Toshiba Corp. is tossing two hats into the 1-Mb EPROM ring. The Tokyo company's EPROMs feature an access time of 150 ns and a writing time of 14 seconds. The TC571000D is compatible with the 32-pin Jedec pin-out for 512-K EPROMs. The TC571001D can replace the 28-pin 1-Mb mask-programmable ROMs currently available. Toshiba enters a crowded market that already includes Advanced Micro Devices' CMOS 170-ns part, Intel's n-MOS 150-ns part, and NEC's 150-ns model. Samples of the Toshiba parts, which are fabricated with a combination of 1.2-μm CMOS and n-MOS and consume 30 mA, will be available this month for $120. The company promises production of 10,000 parts a month in September. □

ALCYON TARGETS FACTORY AUTOMATION WITH ITS REAL-TIME UNIX SYSTEMS

There has been a lot of talk but little action—until now—in distributed processing for real-time multitasking process control and factory automation. Alcyon Corp., San Diego, is unveiling 10 computer systems built around the VMEbus for embedded applications that combine the development flexibility of AT&T Co.'s Unix System 5.2 with Alcyon's Regulus real-time kernel. Five of the 68010-based systems have single processors and range in price from $7,490 to $45,490. The multiprocessor systems also come with a second, faster real-time kernel called pSOS. Regulus handles context switching in 450 μs; pSOS takes just 125 μs. Prices for the multiprocessor systems range from $11,990 to $49,990. Delivery takes from 30 to 60 days. □

OPTICAL MASK-MEASURING SYSTEM IS ACCURATE TO WITHIN 30 NM

An optical electronic measuring system developed by West Germany's Ernst Leitz Wetzlar GmbH and Leitz-IMS Co., a joint venture of Wetzlar and Image Micro Systems, Boston, boasts an accuracy of $\pm$30 nm in determining line widths and X and Y coordinates on masks. This accuracy is achieved with laser-based interferometric procedures taking place in a chamber with a maximum temperature fluctuation of just $\pm$0.05°C. The LMS 2000 system takes only 6 seconds to show results with the 30-nm accuracy and handles masks up to 9 by 9 in. Delivery will begin during the second quarter of next year. In the U. S., the system will sell for $985,000. □

MATHSOFT'S PACKAGE TURNS PC INTO SCIENTIFIC SCRATCHPAD

MathSoft Inc.'s MathCAD software turns a personal computer into an electronic scratchpad for scientific and engineering applications. The Cambridge, Mass., company's software does calculations and analyses with a text-editor-style interface that displays the equation and text on the screen. MathCAD runs on the IBM Corp. Personal Computer, PC/XT, PC AT, and on compatibles, under MS-DOS 2.0. The $189 software requires 348-K bytes of RAM and either a monochrome or color monitor. □

CADRE ADDS MODELING PACKAGE FOR REAL-TIME-SYSTEM DESIGNERS

Users of Yourdon Inc.'s structured design methodology for software development will now be able to model real-time systems during the analysis phase of a project. Cadre Technologies Inc.'s Teamwork/RT package, for developing engineering, process control, and other embedded applications, models applications using state diagrams. The Providence, R. I., company's software comes in versions for work stations from Apollo, IBM, and Sun Microsystems. Teamwork/RT will be available in July as an add-on to Teamwork/SA, Cadre's basic analysis tool. It will sell for $3,600. □

Electronics

A NEW TOOL THAT MAY HELP STOP CHERNOBYL-LIKE ACCIDENTS

SIMULATING NUCLEAR DISASTERS FASTER THAN THEY HAPPEN

CHAMPAIGN, ILL.

The disaster at the USSR's Chernobyl plant has focused new urgency on the question of how best to monitor, analyze, and control a nuclear reactor in the event of a serious accident. And researchers at the University of Illinois in Champaign-Urbana now think they have an important part of the answer.

Their idea is to combine the number-crunching power of a parallel-processor supercomputer with the analytical capabilities of artificial intelligence in a system that could simulate and analyze the chain of events in a complex nuclear accident faster than it would actually occur. This would give plant controllers a forecast of where a problem is headed as well as advice on how to handle it. It would also help prevent accidents in the first place.

Researchers at the university's National Center for Supercomputing Applications have already developed from scratch what is believed to be the first knowledge-engineering software to run on a supercomputer. What remains now is to couple AI's symbolic simulation capabilities and a supercomputer's numerical simulation powers. "I would venture to say that this is within our grasp within the next year or two," says Magdi Ragheb, the nuclear engineer and computer scientist who heads up the pioneering project.

Modern nuclear plants are increasingly being equipped with systems based on microprocessors, microcomputers, and minicomputers that can aid a plant operator in analyzing plant data when an abnormal situation occurs [*Electronics*, May 12, 1986, p. 53]. These systems received new emphasis in the wake of accidents such as the one that occurred in 1979 at the Three Mile Island reactor in Middletown, Pa., in which operators made mistakes because they couldn't adequately interpret the reams of complex data that poured in from plant sensors.

Although current-generation systems can give graphic representations that make the data easier to comprehend, they can't make predictions or offer advice. It's here that the speed of a supercomputer could prove invaluable, says Ragheb.

The package being developed on the University Center's Cray X-MP/24 machine is playfully dubbed HAL-1986, after the HAL 9000 computer built in Illinois in Arthur C. Clarke's book *2001: A Space Odyssey*. Basically, says Ragheb, HAL-1986 is "a very general-purpose inference system that does both forward and backward chaining." In other words, it is capable of either starting with an initiating plant accident and determining the likely outcome, or taking a plant failure situation and working its way back to find out what events may have contributed to the situation.

HAL-1986 was written in Portable Standard Lisp. It combines techniques used in conventional rule-based expert systems with numerical modeling of a system based on knowledge of the system's structure and behavior. It is this combination that is unusual, Ragheb ex-

ILLINOIS' FIRST STEP: AI SOFTWARE ON A MINI

The software being developed at the University of Illinois for artificial-intelligence-based nuclear-plant monitoring will soon be put to real-world use by the Illinois Department of Nuclear Safety, which has been funding the work. The software will simplify the task of data analysis at the state's Radiological Emergency Assessment Center (REAC) by alerting officials when abnormalities occur at an Illinois plant and offering information that could help solve the problem spotted. The present REAC system does little more than dump reams of undigested plant-monitoring data on an expert's desk.

Within a year, the IDNS plans to install on a minicomputer a version of the software developed by Magdi Ragheb on a supercomputer at the university, says Michael C. Parker, chief of the IDNS engineering division. The system will be used in the agency's REAC facility in Springfield, where it will replace a Digital Equipment Corp. PDP-11-based system that monitors the state's nine nuclear power plants through dedicated phone lines. Eventually, the new system will include four additional plants now under construction.

The REAC facility is already the only off-site organization in the U. S. that has access to on-line reactor information, says Parker. The state agency aims to use the data in case of a nuclear accident as an aid in determining how to react in protecting the health of the public.

Right now, a REAC decision on whether to order a general evacuation would depend on a human expert's analysis of large quantities of exceptionally complex data coming from a troubled plant. The planned minicomputer system won't be as capable as the supercomputer-based package in development by Ragheb and collaborators. But it will simplify data analysis significantly by spotting plant abnormalities and by providing REAC officials with plant configuration and status information on systems that might be used to mitigate the problem, according to Parker.

IDNS officials have already begun testing a prototype Lisp-based microcomputer system Ragheb's group developed using data from about 80 reactor-system sensors at the Zion One nuclear power plant in Zion, Ill. IDNS plans to port the package for use on a minicomputer. "We hope to get a significant portion of the system running within a year," says Parker. Full implementation tying in all sensor inputs at all Illinois plants is about 2½ years away, he estimates.

Meanwhile, the IDNS will continue to work with the university toward a more advanced AI system. The agency's goal, Parker says, is a system with the simulation and analysis capabilities contemplated for the supercomputer-based HAL-1986 system Ragheb is developing. REAC might be using such a system within about five years, either on a time-sharing basis or using a dedicated REAC supercomputer, says Parker. —*W. R. I.*

plains. "You want not just to write expert opinion in there, but you also want to simulate the system both from the symbolic perspective and from the perspective of numerical simulation, which is basically the normal Fortran approach that you would use to simulate how a reactor functions in a given situation."

This is where the speed of a multiprocessor supercomputer will come in. While taking inputs from more than 1,000 sensors on an operating nuclear reactor, HAL-1986 will perform a real-time simulation of the reactor operation. By comparing the sensor data to the simulation, the AI portion of the program will be able to recognize deviations and alert a plant operator to abnormalities, Ragheb says.

MONITOR. The University of Illinois' Ragheb is combining simulation and AI techniques on a Cray to monitor nuclear plants.

When an abnormality or accident does occur, the system will simulate at faster-than-real-time speeds to forecast developments in the reactor system and the likely results of alternative actions. With a serious reactor accident, "you can lose your plant in a matter of hours, really," Ragheb says. So such a capability would be extremely valuable.

According to work done by Henry Makowitz, formerly with Cray Research Inc. in Minneapolis and now with the Idaho National Engineering Laboratory, Idaho Falls, a four-processor Cray X-MP/48 would be able to simulate a complex reactor accident about 10 times faster than real time, Ragheb notes. Though the Cray X-MP/24 Ragheb uses at the university is only a two-processor machine, an upgrade to a four-processor system is planned by year end.

Ragheb says the knowledge-engineering portion of the HAL-1986 package has been completed, based largely on work done by graduate student Dennis Gvillo beginning last August. Development of software for coupling the AI-based symbolic simulation portion of the package to conventional Fortran-based numerical simulation capabilities is scheduled for completion in 18 months to two years, Ragheb says.

When that's done, HAL-1986 will be offered for use by utilities and state and federal agencies for nuclear reactor monitoring and analysis, Ragheb says. He stresses that the system is not conceived as an automatic control system, but is designed only as a monitoring mechanism and decision aid for human plant operators. *–Wesley R. Iversen*

IC PRODUCTION

X-RAY LITHOGRAPHY GETS CLOSER

SAN FRANCISCO

Submicron lithography using storage-ring X-ray sources may be closer than many industry experts are willing to concede. While they have been predicting that volume production won't begin until the 1990s [*Electronics*, March 17, 1986, p. 46], these experts got proof last week at the Semicon West conference in San Francisco that the equipment makers were moving faster. The main evidence comes from a West Berlin company, COSY MicroTec GmbH.

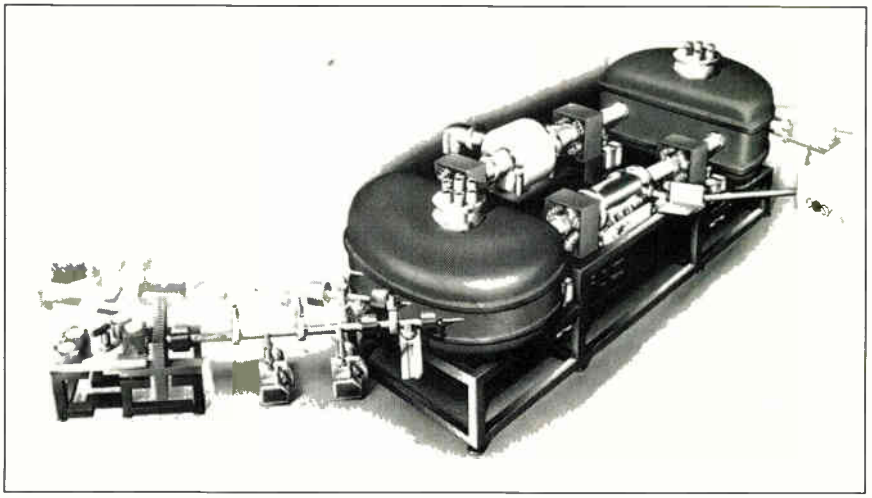
A mockup of the COSY (for compact synchrotron) storage ring [*Electronics*, March 17, 1986, p. 46] was displayed at the show by Leybold-Heraeus GmbH, Hanau, West Germany, which owns a controlling interest in COSY MicroTec and will market the equipment. The mockup included a vertical stepper made by Karl Süss KG GmbH of Munich. A vertical stepper is needed to hold the wafers perpendicular to the horizontal X-ray beams produced by storage rings.

A prototype storage ring will be mated shortly with a vertical stepper at the Fraunhofer Institute for Microstructure Technology in West Berlin, where submicron devices will be made to prove the capabilities of the equipment. The first Karl Süss XRS 200 vertical stepper is slated to be delivered by the end of 1986. Two other steppers are to be delivered in February and March of 1987.

A prototype of the 2-by-4-meter storage ring, with standard magnetic coils and an energy level of 70 MeV, is in test. Work should start next year on a unit with superconductive coils that will produce radiation at a 12-Å wavelength and a 630-MeV energy level. That machine will be shipped in 1988, and will sell for about $8 million, says COSY.

A nonworking stepper model that will be one half of the lithography pair was also on display at Semicon. When mated to the COSY storage ring, the XRS 200 should have 0.2-μm resolution. Two-sigma alignment accuracy is projected to be to within 0.1 μm. The stepper will expose wafers up to 8 in. in diameter.

PLASMA TOO. Karl Süss has a parallel program to mate the vertical stepper to a plasma source developed by the Fraunhofer Institute's branch in Aachen, West Germany. Peter Thompson, product manager for mask aligners at Karl Süss, sees the combination of the plasma source and stepper as a bridge



ON THE WAY. A 2-by-4-meter synchrotron from COSY MicroTec is expected to be available for X-ray lithography work in 1988. It will put out 12-Å radiation at an energy level of 630 MeV.

to the more powerful storage-ring system: the plasma source, which will be mated to a stepper in the fall, has a resolution of 0.4 to 0.5 μm—not as good as the 0.2-μm figure of the combination of storage ring and stepper combination.

The company has an exclusive license for this new source, the LSX 10, and will be willing to quote prices for the combined source and stepper in July, it says. Deliveries are expected in about a year.

The plasma source operates at wavelengths of 7 to 12 A. Goals for the machine include 25 joules of output energy per pulse, a pulse frequency of 1 Hz, and an exposure time of about 1 min per field (of which there are four per wafer). So far, the useful life of the plasma source has been limited to about 800 exposures because of the short lifetime of the special capacitor bank needed to power it. However, new capacitor types now available are expected to increase source lifetime to five times as many exposures.

The plasma-source system is suited to custom ICs and gallium arsenide circuits, Thompson says, whereas the storage-ring X-ray lithography system will be suited to full-scale production of ultra large-scale integrated circuits such as 16-Mb random-access memories.

The plasma-source system will compete with a new stationary-source X-ray stepper displayed a few Semicon West booths away by Micronix Inc. The stepper, which sells for about $900,000, can process six 6-in. wafers per hour and boasts 0.5-μm resolution. A plasma source, providing higher power and greater throughput, will be available for retrofitting to the system by 1988, a Micronix spokesman said. *–Jerry Lyman*

SALES LAG FOR IC EQUIPMENT MAKERS

Improving business in the semiconductor industry will take at least another six months to affect chip-making equipment sales, according to leaders of the Semiconductor Equipment and Materials Institute at last week's Semicon West show. Even then the impact will be modest at best. The 5% to 10% increase in U.S. device sales that SEMI is predicting in 1986 is not enough to boost equipment sales significantly. This is due to underutilized IC production capacity.

The picture is brighter for SEMI's other members. Sales of materials suppliers in all areas—silicon, gallium arsenide, epitaxy, gases, and chemicals—are improving. Sales of chip-making equipment and materials suppliers are expected to hit about $6 billion this year, down slightly from 1985's total.

Sales of production equipment suitable for advanced chips with high pin counts and small geometries are showing the strongest improvement, while sales of equipment for high-volume chips have nose-dived, says SEMI president Sam A. Harrell. European sales have been helped by government funding of efforts to catch up in semiconductor technology, he adds, with Europe accounting for as much as 36% of sales recently, up from a 8% to 10% share.

In the Far East, the weakening dollar is helping U.S. equipment makers, Harrell claims. In contrast, however, LSI Logic Inc., last week announced that it was purchasing $30 million worth of chip-making equipment from Nikon Precision Inc., a U.S. subsidiary of Japan's Nippon Hogaku K. K. *–Clifford Barney*

MATERIALS

TOOLS MAKE THIN FILMS PREDICTABLE

CAMBRIDGE, MASS.

A new set of research tools promises to ease the plight of chip makers working with unpredictable thin films and significantly improve the reliability of certain integrated circuits.

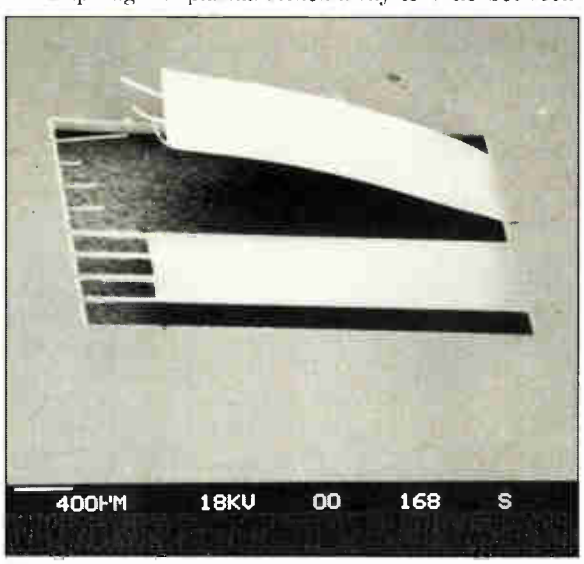
The three tools are microstructures used for studying thin films under tensile stress. Developed by a team at the Massachusetts Institute of Technology, the tools enable users to measure such quantities as residual stress, Young's modulus, and elongation at the breaking point. They can also be used to study the temperature dependence of films and their reactions to moisture.

The research team, which will report in detail on the work next month at the Electronic Materials Conference in Amherst, Mass., concentrated its efforts on polyimide films, but the tools should be feasible for a wide range of thin-film materials used in semiconductor processes.

WORKING IN THE DARK. The problem that confronts users of thin films is that the materials undergo internal stresses that can cause cracking or deformation during semiconductor production or in field use. The thicker the film, the more severe the problems. Until now, there has been no relatively simple way to characterize the materials, a lack that has made thin-film work very difficult.

The structures developed at MIT are called patterned, or release, structures. To fabricate them, silicon is anisotropically etched to create a thin diaphragm, used for initial support. A polyimide film is spin-coated on top of the silicon diaphragm and patterned using photolithography in any one of the three release-structure forms. Finally, the silicon diaphragm is plasma-etched away to release the structure and allow relaxation of the internal film stress. By studying the film's contraction and shape changes after release, its physical properties can be determined.

The MIT team used three basic structures. One is a T-shaped structure fixed at all three points. With supporting silicon removed upon release, the crossbar of the T deflects, and the ratio between residual stress and elastic modulus can be measured from the amount of deflection.



BEAM. One of three structures used at MIT to demystify the behavior of thin films is a beam with thin bands at one end.

Another is a beam structure, solid on one end, with the other end formed into a forklike structure with only the thin bands attached (photo). By using beams with different widths, it is possible to determine the stress-to-modulus ratios at various strains up to the breaking point. The beams are more efficient geometries for getting big extensions. In their research, the team at MIT used beams 1,500 μm long by 700 μm wide, changing to 100 μm wide for a length of 500 μm at

the beam's fork-shaped end.

A third, cantilever structure can be used for cross-checking results.

Wafers with the structures can be fabricated and tested by both the materials manufacturers and the semiconductor or hybrid end-user. "I suspect that from this we'll be able to develop a data base of all the materials that go into IC fabrication and thin-film materials," says Stephen Senturia, professor of electrical engineering, who worked on the project with Mehran Mehregany, Mark Allen, and Roger Howe. Senturia stressed the importance of consistent methodology. "What we've developed is a method for studying materials in situ," he says.

The work in the laboratory, funded in part by Du Pont, IBM, and 3M, has been with structures as small as 5 to 10 μm. "One of the research areas we have to investigate is how to scale down the structures so we can look at the mechanical properties of device-sized features," says Senturia. He adds that in the interim, the larger tools provide at least raw data that simulates actual mechanical properties of IC-sized devices.

The MIT group also wants to investigate composite materials such as polyimide film laced with metal routings, which is how materials typically appear in ICs. Senturia believes future work will be dominated by studies of the interfaces between materials. Through that work, he says, it can be confirmed that composite structures behave predictably. "This will permit us to improve designs for process control and reliability," he says. *–Craig D. Rose*

PACKAGING

REALIGNING BOND PADS HIKES CHIP RELIABILITY

SOMERVILLE, N. J.

The need was old and universal: engineers at RCA Corp.'s Solid State Division wanted to improve the reliability and manufacturability of their semicustom chips. Long bond wires connecting chips to their packages often caused severe yield problems that hung up engineers in lengthy redesign time, forced retooling on the production line, and cost valuable fabrication time. The delicate wires were prone to snapping or shorting out when stretched to reach remote pins on chip packages. Moreover, designers wanted to make better use of the corner regions of their semicustom chips.

The answer was surprisingly subtle: RCA designers realized that if the bonding pads on the chip could be realigned so that they angled out into the far corners of the chip, the lengths of the longest bond wires could be diminished by up to 30%. That helped to minimize the yield problems associated with overly long bond wires—but it had another positive effect, as well. According to Stephen Morris of RCA's Application-Specific Integrated Circuit Development Group, researchers found that by fitting the chip's corners with the bonding pads, they also got a 5% to 7% savings in silicon real estate as a bonus for their efforts.

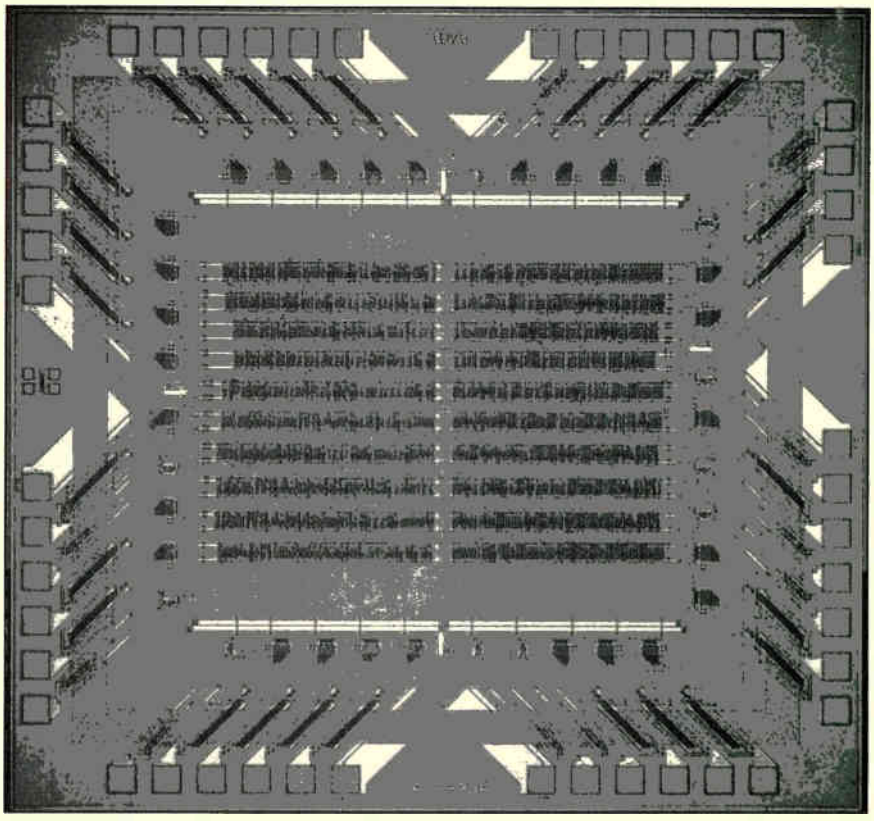
"Most routing programs like to see bonding pads in nice, neat, fit-me-together packages in a rectangular format," Morris explains. "But as geometries get smaller, maintaining those packages gets harder. All these placement and routing programs waste the corners. They want to be symmetrical, and we wanted to get around that." Rather than keeping the pads in dense blocks perpendicular to each edge of the chip, the RCA designers decided that the pads could be implemented at 45° angles from the chip's edges and spread out so each bond pad could be as close as possible to the associated pin on the package.

A spreader program spaced the pads out across the entire length of a chip's side, further minimizing the length of the bond wires. In a typical chip, the longest bond wire lengths can be reduced from about 70 mils to about 50 to 55 mils, Morris says.

Interestingly, the slanted-pad implementation is invisible to RCA's MP2D placement and routing system. "We're still describing boxes so high and so wide to the router," Morris explains. "It doesn't know if they are square or slanted." That's because slanted pads were designed into the division's new 2-μm-cell library so that use of the slanted pads will be automatic when the library, which is undergoing prove-out testing, is made commercially available.

CORNERING. Slanted structures also make it easier for engineers to make use of the corner areas of a chip. Although still limited by its design rules, Morris says, RCA can put power or even logic cells into the corners of the chip, where not even the bonding pads reach. "The corner cell is available," he says. "You could design a nice corner power pad, or even a logic cell if you were very clever. Our only limitation right now is that we'd have to put the identical cell in all four corners."

Gene Patterson, director of application-specific-IC marketing, points out that in devices with high pin counts, this process is especially useful. "The larger



ANGLED IN. Pads are implemented at 45° angles from the chip's edges and spread out so each bond pad can be as close as possible to the associated pin on the package.

the pin count, the more difficult the bonding problem is. When your pad area begins to exceed the core area, you are going to have problems, and you can't afford problems because you're designing for high-volume production and reliability."

The new method also saves design time. In many circumstances, chips designed using conventional bonding pads have to be reworked after prototyping because poorly placed pads have to be moved to improve yields. Because the new placement process is automatic and not manual, Patterson says, RCA can save three to five days in redesign time and anywhere from 2% to 5% in costs.

Fast prototyping is an area of hot contention in the semicustom arena, so the loss of three to five days can be significant when it comes to getting return business, he says. "It's a subtlety that adds to our reliability and manufacturing techniques." *–Tobias Naegele*

TELECOMMUNICATIONS

INDUSTRY SPLITS ON WHAT COMPUTER III ADDS UP TO

WASHINGTON

Industry opinion has split over the Federal Communications Commission's ruling in its Third Computer Inquiry, which would eliminate the need for Bell operating companies to set up arm's-length subsidiaries in order to start offering enhanced telecommunication services, such as packet switching and voice storage. On one hand, some observers approve of the FCC's decision; some in fact want the agency to move faster in order to speed the entry of the BOCs into enhanced services. Other observers maintain the accounting safeguards the FCC proposed as a substitute [*Electronics*, May 19, 1986, p. 13] won't stop cross-subsidization: the BOCs' use of revenues from basic phone services to lower the user fees for enhanced services.

Besides eliminating prior arm's-length subsidiary requirements, the commission formally embraced the murky network-access concept called "comparably efficient interconnection" and ordered AT&T and the BOCs to file plans that meet the requirement by Feb. 1, 1988. These plans must give third parties access to central-office equipment that is comparable to the access enjoyed by AT&T and the BOCs.

The FCC still has some cleanup work to do on Computer III. Among the remaining issues is how protocol conversion should be regulated (see "Protocol conversion at issue"). Several commission members indicated that they favor an alternative that would continue to treat protocol conversion as an enhanced service subject to safeguards.

The BOCs' move into enhanced services still could be slowed by what is known as the Modified Final Judgment, part of the 1982 agreement that brought about the breakup of AT&T and spawned the seven BOCs. That judgment requires the BOCs to obtain the approval of U. S. District Court Judge Harold H. Greene, who oversees their competitive activities, before offering enhanced services.

A ROADBLOCK. "In spite of the giant step we make here today, we have a huge roadblock that still lies ahead: the Modified Final Judgment still restricts the seven regional companies from entering into many of these enhanced services," notes FCC chairman Mark S. Fowler. "This obstruction must be removed." The Justice Department's Antitrust Division is reviewing the continuing need for the line-of-business restrictions and will submit a formal report to Judge Greene on Jan. 1, 1987.

Predictably, the BOCs agree with Fowler. The enhanced-services restrictions of the judgment "cast a shadow over Computer III," maintains W. Roger Burge, director of regulatory affairs for BellSouth Corp. He says the FCC attempted to move telecommunications into the future, but "Computer III leaves us squarely in the present." Still, Burge praises the elimination of the requirement for arm's-length subsidiaries.

Still, critics of the FCC's deregulatory drive contend that the accounting safeguards that will replace this requirement aren't enough to prevent anticompetitive BOC behavior, such as cross-subsidization. They also think that the FCC lacks the resources to enforce them. Edwin B. Spievack, president of the North American Telecommunications Association, a Washington-based trade group representing telecommunications equipment makers, condemns them as "phantom safeguards," adding that the "FCC will be unable to guard against phone company cross-subsidies—at least not without a new army of regulators and accountants."

Auditing separate BOC books will strain the FCC's resources, agrees a staff member of the house subcommittee on telecommunications, consumer protection, and finance. Accounting safeguards are "a long way from being something anybody can rely on," adds Herbert E. Marks, an attorney for the Independent Data Communication Manufacturers Association, Washington. Marks says the FCC must still design new accounting methods for "getting at the audit trail."

By contrast, both sides in the deregulation debate generally approved of the FCC's handling of network-access issues and its requirement that the BOCs and AT&T file Open Network Architecture plans that realize the notion of comparably efficient interconnection [*Electronics*, Feb. 17, 1986, p. 17]. In issuing its ruling, the FCC commissioners said they believe that comparable network access for all parties would prevent discrimination by the BOCs in favor of their own enhanced services. This belief tipped the balance in favor of eliminating structural separation. "The good news is that the FCC is very concerned about comparably efficient interconnection," says Marks. "Open Network Architecture is a very encouraging sign."

Equal access to the phone network represents a compromise, adds William F. Adler, executive director for regulatory matters with Pacific Telesis Group, a BOC. Adler maintains that the BOCs will need the time allot-

PROTOCOL CONVERSION AT ISSUE

As long as there are different systems for networking, which will probably be the case for a long time, protocol conversion will be an essential service. But deciding how to regulate that service remains one of the thorniest issues for the Federal Communications Commission. When the Computer III report and order comes out in several weeks, it will include a supplemental notice asking for, among other things, comments on three alternatives for regulating protocol conversion, now considered an enhanced service subject to safeguards.

Alternative A would treat protocol processing as an adjunct to an underlying basic or enhanced service. It would not change the regulatory status of either service.

Alternative B would continue to classify it as enhanced, but the FCC could classify specific conversions such as asynchronous-to-X.25 and X.25-to-X.75 as adjunct services. Alternative C would retain the enhanced-service label and subject protocol conversion to nonstructural safeguards when provided on an unseparated basis by the Bell operating companies and AT&T Co. Although he supports the third choice, FCC commissioner Dennis R. Patrick notes, "The course the commission ought to take is unclear."

ted by the FCC to formulate Open Network Architecture plans because comparably efficient interconnection is "a framework, not an answer."

Yet the FCC is still considering the possibility of waiving parts of its network-access requirement if a carrier can show that a particular functional parameter can't be provided on an equal basis. "We are requesting that the commission reject an all-or-nothing approach," says Albert Halprin, chief of the FCC's Common Carrier Bureau.

"Of course," reassures FCC commissioner Dennis R. Patrick, "the burden will be substantially upon the carrier to demonstrate that, in fact, it is impossible to comply with what we would like to see in the way of comparably efficient interconnection." *–George Leopold*

THE FRENCH MOVE TO OPEN TELECOM MARKET

PARIS

France's new conservative government is about to begin drafting a law that would open the country's telecommunications infrastructure to competition. If the plan becomes law, it will mean the first break in the government's monopoly on telecommunications services since a 19th Century edict gave the government total control over the national telegraph network.

In announcing the plan last week, Postal and Telecommunications Minister Gérard Longuet said the government wants to create a new, independent organization, the National Committee for Communications and Liberties (CNCL), as the primary regulatory body for communications questions. Moving this function from the Direction Générale des Télécommunications to an independent entity would permit the DGT to compete in the French telecommunications market without bearing the contradictory responsibility for regulating it.

The commission's main role will be to apply the principles defined in what is to be called "the law on competition." Longuet, however, could give few details about that law. The draft is scheduled to be ready in December 1987, and its content will then be the subject of extensive public debate, he said.

Still, several probable directions for the legislation seem clear. For example, the French government will probably renounce its monopoly on the distribution services that are being planned as part of the country's extensive optical-fiber cable program.

EXCEPTIONS. But Longuet was much more reserved on the future of interactive services, saying that the degree to which they will be open to competition will depend on the outcome of the debate preceding adoption of the law. Most observers here see a desire to protect the country's stunningly successful videotex program, which has turned into one of the government's principal revenue sources. Also a doubtful candidate for open competition is intercity telephone communications; Longuet called that area one that seems to be a natural public service.

Enhanced services, on the other hand, seem likely to be opened to competition. Longuet's ministry is already considering two proposals, one from IBM Europe and the French bank Parisbas, and another from Ing. C. Olivetti & Co. of Italy and Indosuez, another French bank, asking for authorization to establish networks offering a variety of enhanced services from electronic mail to accounting and stock-handling applications. Longuet added that he expects an additional proposal from Bull, the country's flagship data-processing-equipment manufacturer. Decisions on these propositions will be announced "within the next few weeks," said Longuet.

Most French observers say purely political obstacles could keep the program from ever getting off the ground. With a deadline for the end of next year and the edges already beginning to fray between conservative Prime Minister Jacques Chirac and Socialist President François Mitterrand, many think the country will be facing new elections before the law is complete.

An election, no matter what the outcome, would hinder progress on the program. A Socialist victory would sink the plan, and even a win by the conservatives could cause an internal reorganization of the government that would, at the very least, slow down the plan considerably. *–Robert T. Gallagher*

PERSONAL COMPUTERS

NOW $505 BUYS AN IBM PC/XT CLONE

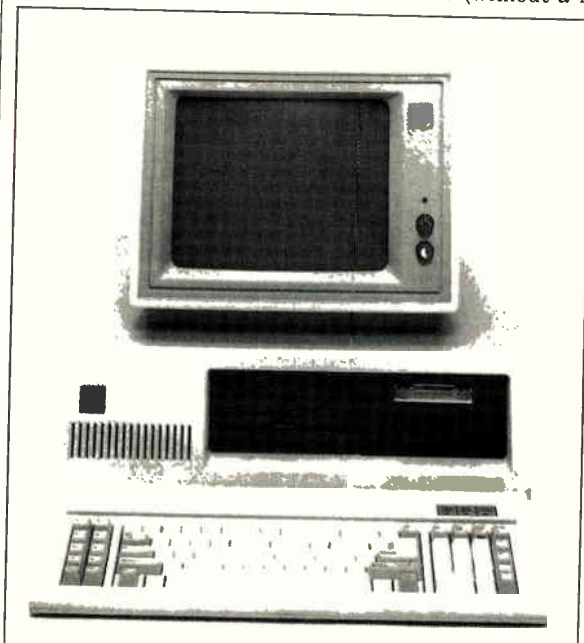
CHICAGO

Thanks to the availability of low-cost Far Eastern components, clones of the IBM Corp. Personal Computers that pack more power than the original machine and sell for a fraction of the price are popping up all over. The latest and lowest-priced entry yet comes from the Windy City.

At $505, a PC/XT clone from Thompson Harriman & Edwards Computer Products Co. will sell for less than a quarter of the $2,145 price of a PC/XT (without a hard disk) from IBM. "We're the lowest price on the market that isn't a [computer] kit," contends president Stephen A. Dukker.

The company's new PC+ comes equipped with a single 5¼-in. floppy-disk drive, 640-K bytes of random-access memory, eight expansion slots, and a PC AT-style keyboard. It also features operation with either a 4.77- or 8-MHz clock. The nearest-priced machine with dual-clock capability sells for $795 (from PC's Ltd., Austin, Texas), Dukker says. "And even without the dual-speed clock, we're close to $100 lower than our nearest competitor."

Thompson Harriman, which is an affiliate of Chicago mail-order house PC Network Inc., will assemble the PC+ in a



XT CLONE. Thompson Harriman & Edwards Computer Products Co.'s entry is $505 with one floppy and no monitor.

45,000-ft² facility in Chicago using components imported from Korea, Japan, and Taiwan. "Our organization has been around for three years working on high volume and low margin and making a profit," says Dukker. That experience, coupled with favorable terms negotiated with component suppliers, allows the low PC+ price, he explains.

Some in the industry question the reliability and true compatibility of low-end clones such as the PC+, which have been emerging in greater numbers over the past few months. But Dukker calls those doubts "sour grapes." The PC+ comes with a 1-year warranty on parts and labor and a 45-day money-back guarantee, he says. Response to the machine—which will be sold both by mail order and through dealer outlets—has been strong. "We've got over 100 dealers signed up," Dukker says. "We expect within 60 days to be delivering 8,000 units a month based on current order volume."

Illinois maker says $300 version is in the works

The PC market is likely to get tougher, with price cuts from established vendors of more expensive PC-compatibles as well as continued investments in automation and price cuts from IBM itself [*Electronics*, April 21, 1986, p. 61]. But Dukker sees a market window of two years for the PC+. And he is already planning an even lower-priced follow-on product. It will feature a 3½-in. floppy-disk drive like those in the new IBM PC Convertible, and for cost reasons, will have only two expansion slots. "We've already got a machine designed that would sell in the $300 price range," he says, "and we're looking at a mid-1987 launch point." *–Wesley R. Iversen*

NETWORKS

CHIP SET SPEEDS UP BRITISH LOCAL-AREA NET

CAMBRIDGE, ENGLAND

A chip set for a new high-speed version of the 10-year-old Cambridge Ring local-area network has been developed in a joint venture by a laboratory at Cambridge University and Acorn Computers Ltd. The chips will increase the LAN's operating speed from 10 Mb/s to at least 60 Mb/s, opening up new applications for ring networks integrating voice and data transmission and those requiring the rapid transfer of detailed images.

The two chips, one built in emitter-coupled logic and the other in CMOS, are expected to be available by the end of the year through Acorn, now owned by Ing. C. Olivetti & Co., Ivrea, Italy. Acorn will not reveal price details yet, but says that the principal aim of the project—to produce a much faster ring at a price comparable to the existing 10-Mb/s LAN—has been achieved.

The chips form the basis of a new version of the well-tested Cambridge Ring, a slotted-ring network whose operation is substantially different from that of token-ring networks from IBM and others. The new version has been developed for local-area applications but coincidentally bears a close resemblance to to the IEEE-802.6 specifications for longer-distance metropolitan-area networks.

"You could use it for metropolitan networks because it has turned out to be quite close in spirit to the IEEE specifications, but that was not deliberate," says Roger Needham, professor and head of Cambridge University's Computer Laboratory. Needham and Andrew Hopper did the basic design work at the lab, and Acorn supervised the implementation in silicon. Cooperation between the two is continuing.

The ECL part functions as a serial/parallel converter and a modem, and it will operate at 100 Mb/s or faster. It is the CMOS device, however, that Needham sees as the major innovation. "This features the address-recognition and transmission/reception logic and can function as the monitor station, which maintains the framing that any slotted-ring LAN depends on," he says. "It also has the logic to allow it to be used as half of a ring-ring bridge."

This chip is currently implemented in 3-μm CMOS and works at 60 Mb/s. However, the design is now being shrunk to design rules of about 2 μm. The 2-μm chip will be considerably faster, at least 80 Mb/s and possibly 100 Mb/s. This chip is the bottleneck: its speed determines the operating speed of the whole ring.

LOW COST. Putting the monitoring and bridge functions on the chip is seen as crucial because otherwise the component count would be high, making the whole system too expensive. "The aim was to create a cheap 100-Mb/s ring," Needham says. "If you are connecting expensive mainframes, the cost of the network may not matter that much. But if you do it in a couple of chips, the applications for the ring are made much broader."

It is unlikely that users of present Cambridge Ring LANs will adapt their systems to use the new chips. Needham said this would be technically possible but not worth the time and expense. The faster ring will likely find use in new systems for applications where the old ring was too slow.

Although the chip set is not yet available to customers, the Cambridge laboratory is satisfied that the devices work. The chip set has been put to work in several experimental systems as part of Unison, a fast-networks development effort that falls under the umbrella of the British government's Alvey fifth-generation computer project.

"Our plan is to validate the fast ring in a real-life environment, and the Unison project is a good way of testing it," says Andrew Hinchley, manager of communications products at Acorn. Besides Acorn and the Cambridge laboratory, other organizations doing work for Unison include Logica Ltd. and the Rutherford-Appleton Laboratory, Cambridge, which is run by the government's Science and Engineering Research Council.

Acorn is discussing marketing arrangements for the chip set with the Cambridge lab. It says it is likely to license silicon-manufacturing rights to others as well as develop its own products. *–David Boothroyd*

AUTOMOTIVE

SMART COMPASS PILOTS A CAR TO ITS DESTINATION

SCHWALBACH, WEST GERMANY

The first self-contained automotive navigation system on the European market is also the least expensive of any type in the world, according to its developer, VDO Adolf Schindling AG. Costing only $400, the system uses the earth's magnetic field as a reference to guide drivers.

Now being launched by VDO, Europe's biggest maker of dashboard instrumentation, Citypilot navigates with on-car devices only. Other schemes being pursued rely on an extensive and costly infrastructure of transmitters along the road, sensors in traffic lights, induction loops in the road bed, or satellites in the sky [*Electronics*, July 29, 1985, p. 28].

The Schwalbach company's tests so

far reveal that drivers using the Citypilot system reached their destinations with an accuracy of 97%, or within 3% of the distance traveled. So if a car travels under Citypilot guidance for 5 km, the driver will reach the destination to within 150 m.

SMART COMPASS. Project leader Helmut Angermüller describes the system as an intelligent electronic compass: in essence, it depends on an earth magnetic-field sensor inside the car roof and a distance sensor in the speedometer drive. Using the sensor inputs and the destination-identifying coordinate data the driver has entered, a microcomputer in the central control unit calculates the vehicle's location relative to the destination as well as the line-of-sight distance to it.

Calculations are performed four times per second, and the results are shown on a liquid-crystal display on the dashboard. Arrows and bearing markings tell the driver which general direction to take to reach the destination, while a three-digit number indicates the distance in fractions of a kilometer. When the car gets within the 3% target area, a beep and a flashing display alert the driver that he is near his destination.

Data is carried in bar-coded form on city maps. Before the journey, the driver picks the starting and destination points on the map with a light pen, feeding them to the microcomputer. This simple method contrasts with that used in expensive self-contained developed or proposed systems in which maps come digitized on compact disks or cassettes [*Electronics*, June, 17, 1985, p. 47].

Citypilot's price is also one third to one fourth that of a cassette-based system developed in the U. S. by Etak Inc., Sunnyvale, Calif. Digitizing road information and keeping updated all the disks and cassettes needed to cover large geographical regions is an enormous and costly task, Angermüller says.

Results of road tests support VDO's conviction that the Citypilot will make it on the market. A project carried out at the University of Tübingen and cosponsored by German automaker Porsche AG showed that drivers heading for a particular spot in an unfamiliar city "reacted calmly to the system's instructions, drove along city streets without strain, and easily found their destination," says Günter Hahlganss, VDO's director of development.

Also, in an effort to test market acceptance, VDO has outfitted nearly 100 private cars with the Citypilot, and response to the system has been favorable, Hahlganss declares. Car makers, too, are said to be interested in the system, and VDO is speculating that it will eventually become standard equipment on top-of-the-line cars. West Germany's Robert Bosch GmbH is readying similar equipment for introduction next year.

RAMBLING WAYS. Data for a journey is picked up from a bar-coded map by light pen and fed into Citypilot's microcomputer. Distance and location information is displayed on an LCD.

For optical data entry, the driver picks off the coordinates of the starting and destination points with the aid of a graduated template, along whose edge the light pen is moved. The data then goes to the computer. The pen also feeds in the map's scale and, for purposes of compensating the car's bearing, the declination—or angular difference between magnetic and geographical north—for the region shown on the map. This data is contained in a bar code printed along the map's edge. So far, appropriately bar-coded maps exist for nine metropolitan areas in West Germany—from Hamburg in the north to Munich in the south.

The driver gets directions from a dashboard LCD

The driver can also use a small keyboard to enter into memory the coordinate, scale, and declination data for multiple destinations. Data for up to 99 destinations can be entered into the system's battery-backed CMOS random-access memory by light pen or keyboard. Destinations can be called up with the keyboard whenever needed.

En route, the distance and magnetic-field sensors continually supply the microcomputer with navigational data. In this process, the distance sensor, a rotating-magnet Hall sensor, generates pulses in accordance with wheel rotation to mark the distance traveled.

The magnetic-field sensor, which uses flux-gate principles and reacts to a field strength one thousandth that of the earth's, measures the horizontal component of the earth's magnetic field. Associated circuits compensate for stray vehicle-induced magnetic fields.

To determine the car's orientation relative to the compass bearing, the sensor measures the magnetic field strength of the horizontal component in both the vehicle's longitudinal and transverse axes. From this measurement, the microcomputer recognizes the north direction and the car's direction of travel. The programs needed for the various calculations are contained in read-only memory.

The LCD gives the driver instant information, recommending the route to take to get to the destination. (If the driver chooses one of the 99 possible programmed destinations, the display will give a number for it.) Compass bearing and direction are displayed, the latter in the form of one of 16 possible arrows on a rosette. Distance is presented in kilometers with a resolution of 10 m.

Should the vehicle enter a zone with strong stray magnetic fields, such as may be caused by streetcars, the system may temporarily go haywire. In this case, a symbol appears on the display telling the driver that for the moment the guidance information cannot be relied upon.

Naturally, the shorter the route chosen for being under Citypilot control, the closer the system will take drivers to their destination. If the target is only 1 km from the starting point, then the system will guide drivers to within 30 m of the destination, given the 97% accuracy. Being that close, drivers should have no problem identifying the places they set out to find. —*John Gosch*

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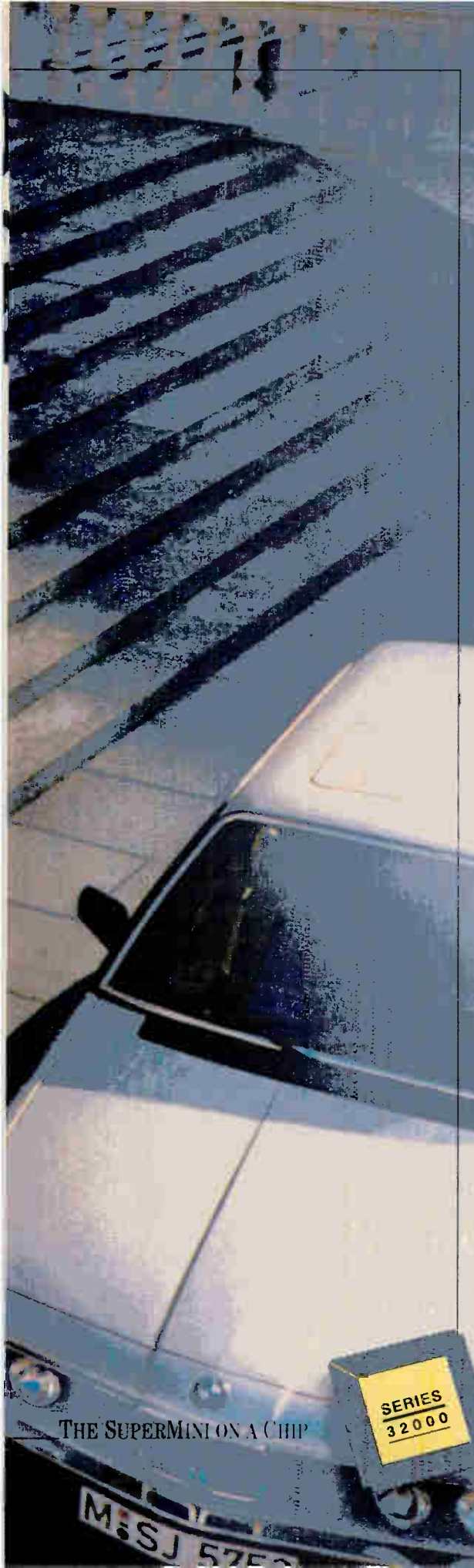

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INSIDE TECHNOLOGY

HOW SURFACE MOUNTING IS CHANGING INTERCONNECTION

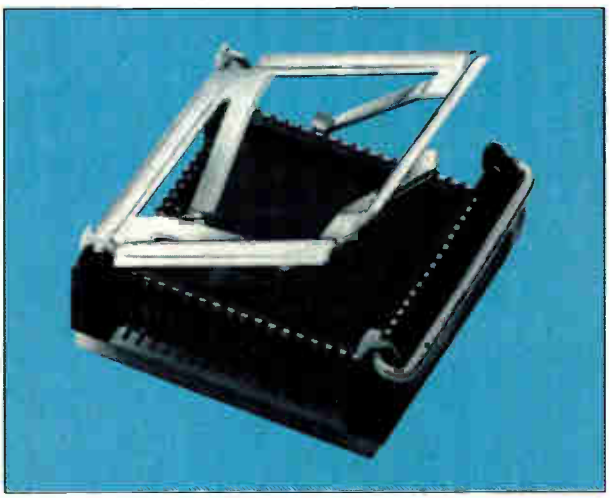
SOCKETS, BOARDS, AND CONNECTORS FEEL THE IMPACT

by Jerry Lyman

Surface-mounting assembly is still a small industry, but it packs a big punch. It is now having a major impact on the entire board-interconnection field because its share is expected to expand from a mere 6% of the U. S. board-assembly market this year to as much as 30% by 1990. Surface mounting is responsible for new families of chip sockets as well as new electrical and mechanical designs for printed-circuit boards. Its biggest effect has been on connectors, where new designs and materials coupled with attention to automatic parts handling have spawned a new type of interconnection component.

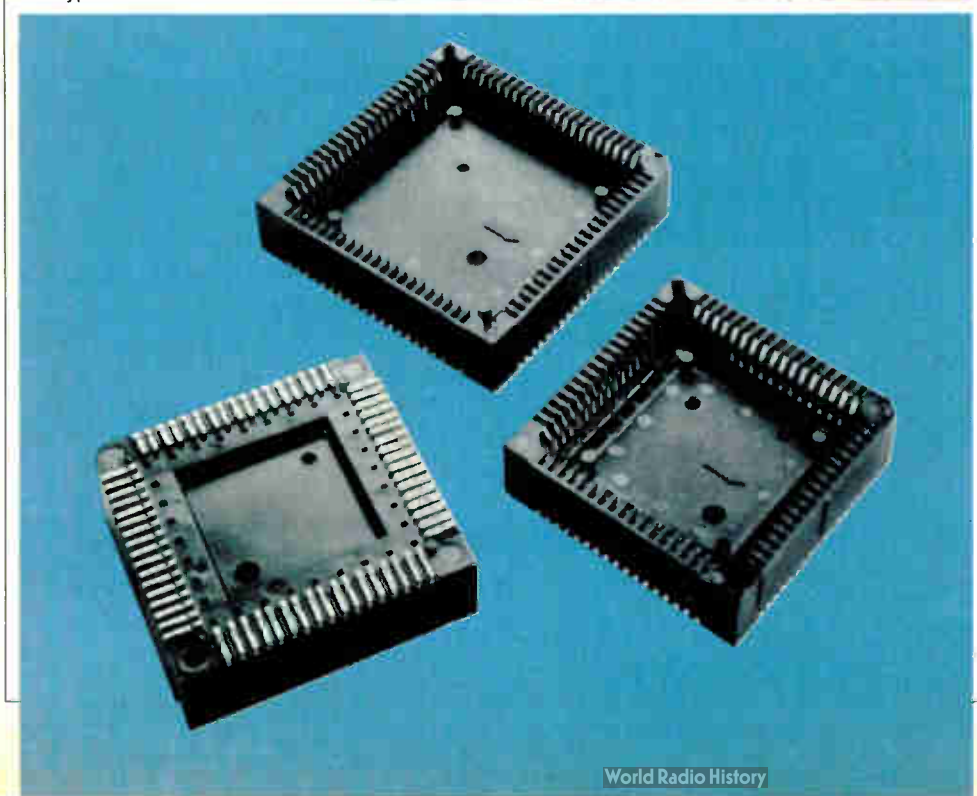
In chip-to-board interconnection, chips may be electrically and mechanically attached to the pc board in such packages as leadless ceramic chip carriers, plastic leaded chip carriers, small-outline chips, plastic and ceramic quad flatpacks, and even the old faithful dual in-line package in 70- and 100-mil lead pitches.

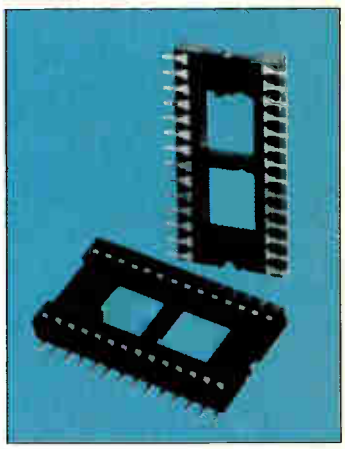
Leadless ceramic chip carriers—now mostly favored by the military and used only in computer and telecommunications applications where hermeticity is desired—require thermally matched or controlled boards and are split by Jedec into two types. Type A carriers require sockets; type Bs may be socketed or soldered directly. All other surface-mounted package types have compliant leads, allowing the use of standard epoxy-glass laminates.



1. LEADLESS. Augat's surface-mounting socket for leadless chip carriers is compatible with both Jedec types A and B.

The surface-mounting socket, such as that from Augat Inc., Attleboro, Mass. (Fig. 1), comes into play when a leadless chip carrier must accompany leaded components on a standard epoxy-glass board; where repairability and replacement of certain chips are mandated; and where a single large expensive part, such as a microprocessor or gate array, must not be damaged during assembly. Amp Inc., Harrisburg, Pa., supplies sockets with leads on 50- or 100-mil centers that accept leadless and leaded chip carriers (Fig. 2). In fact, connector





2. PLASTIC SOCKETING. Amp's surface-mountable sockets (left) accept Jedec-style plastic chip carriers with 50-mil-centered leads.

3. OLD FAITHFUL. Even DIP sockets are available in surface-mounted versions. Burndy supplies units with up to 40 leads (above).

companies now are supplying DIP sockets in surface-mounting versions (Fig. 3).

Chip-carrier sockets are now available with up to 84 leads and often have built-in heat sinks and accessible test points. Unlike through-the-board sockets, surface-mounting sockets require a hold-down mechanism and guide pins for aligning the leads with their mating pc-board pads. Most manufacturers supply sockets with gull-wing leads for easier inspection and testing. However, a few companies, such as Burndy Corp., Norwalk, Conn., and Methode Electronics Inc., Chicago, will supply a J-leaded socket if the customer prefers. This configuration takes up less surface area, but the tradeoffs are more difficult inspection and testing.

As very large-scale integrated circuits increase in power dissipation, size, and input/output-pad count, there is increasing belief that the leadless chip carrier will not be able to handle these future chips under any circumstances. This is why Intel Corp., for instance, houses some military products in four-sided ceramic flatpacks. The ideal package, in terms of both use and cost, would be a plastic leaded package with a humidity-resistant seal.

Soaring I/O count in VLSI chips is a major challenge to package designers. To hold down chip carrier size, package manufacturers are going to 25- rather than 50-mil pin spacing. A case in point is Integrated Device Technology, Santa Clara, Calif., which provides a 25-mil-pitch package for its CMOS multipliers and multiplier-accumulators. The fine-pitch leadless 68-I/O chip carrier is roughly the same size as a standard 50-mil-pitch, 32-pad leadless carrier. This unit now requires an entirely new socket type if it is to be socketed. Another instance is the family of fine-pitch chip carriers from Amp, which culminates in a 320-lead type on 10-mil centers. The company has devised a special socket for this prototype carrier.

As the pitch of package-output leads becomes finer and finer, soldering becomes increasingly difficult. Martin Freedman, a project engineer at Amp, foresees that fine-pitch carriers may require solderless, clamped sockets rather than the standard reflow-soldered types because of the potential problem of solder bridging across the tightly packed leads.

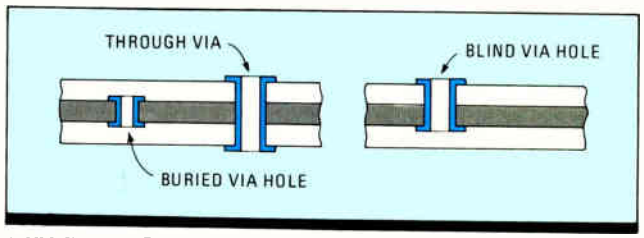
SECOND-LEVEL INTERCONNECTION

At the pc-board level, surface-mounting technology is affecting layout, testing, and even materials. "Surface mounting is becoming even more density-driven, heading toward packages such as leaded and leadless chip carriers with ever-higher pin counts—68, 84, 124, and higher," notes George Messner, senior scientist of PCK Technology, a division of Kollmorgen Corp. in Melville, N. Y. "This means the designer faces a new, complex interconnection environment."

Currently, the entire outer surfaces of the board are committed to I/O pads for carriers and vias—small holes whose only function is internal interconnection. A multilayer approach is needed to raise interconnection density. And as the pitch of chip carriers gradually changes from 50 mils to 25 and even 20 mils, more carriers will be squeezed on a board, compounding the interconnection problem.

New high-density surface-mounted boards may run as many as three to four conductive traces between package pads to meet the density challenge. This in turn will call for 4- to 5-mil conductive traces rather than the 8- to 10-mil traces used on the present generation of much less dense boards, which are based on lower-pin-count (18 to 44) chip carriers and small-outline packages.

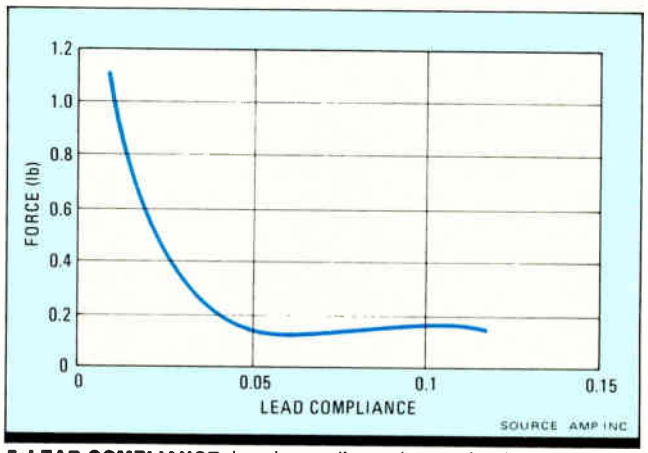
The new boards will require a great many vias—buried (between two inner layers) and blind (between a top layer and an inner layer) as well as regular vias (Fig. 4). The simple X-Y routing algorithms of most computer-aided design systems developed for plated-through holes cannot cope with this need. A more complex vectorial algorithm is necessary and is currently only available from one company, Cadnetix Corp., Boulder, Colo.



4. VIA TYPES. On a true surface-mounted multilayer board, all layer-to-layer wiring is done with either full, buried, or blind vias.

Testability also affects board layout, since it must be designed in. For example, in a board based on either J-leaded plastic chip carriers or leadless chip carriers, the chip-to-board solder joints go under the IC packages, so the board's pads must be extended outward to clear the carrier. And although gull-wing chip carriers have accessible leads, most manufacturers now advise against probing a solder joint. The probe's pressure can make the joint appear good by creating a temporarily good connection. So even a gull-wing leaded carrier must have its pc-board footprint extended.

In the extreme case of a board with tightly packed fine-pitch carriers, judiciously placed test points must be designed in, since the normal bed-of-nails fixture on 100- and even 50-mil centers simply can't access this type of board. Mike Bullock, project manager at Hewlett-Packard Co.'s Manufacturing Test Division in Loveland, Colo., summarizes the situation this way: "The first three rules for testing surface-mounted



5. LEAD COMPLIANCE. Lead compliance has a significant effect on stresses in a solder joint. A high compliance reduces stress.

THERMAL/MECHANICAL PROPERTIES OF PRINTED-CIRCUIT SUBSTRATES

Material	Thermal coefficient of expansion-xy (ppm/°C)	TCE-z (ppm/°C)	Thermal conductivity (W/m/K)	Modulus of elasticity (10^6 lb/in.^{2})	Density (lb/in.^{3})
PTFE/glass	24	261	0.26	0.14	0.079
RO2800	16 to 19	24	0.44	0.06	0.072
Polyimide quartz	6 to 8	34	0.13	4.0	0.07
Polyimide Kevlar	3.4 to 6.7	83	0.12	4.0	0.06
Polyimide glass	11.7 to 14.2	60	0.35	2.8	0.066
Epoxy glass	12.8 to 16	189	0.18	2.5	0.065
Alumina	6.5	6.5	16.8	37.0	0.13
Copper	16.9	16.9	394	17.0	0.324

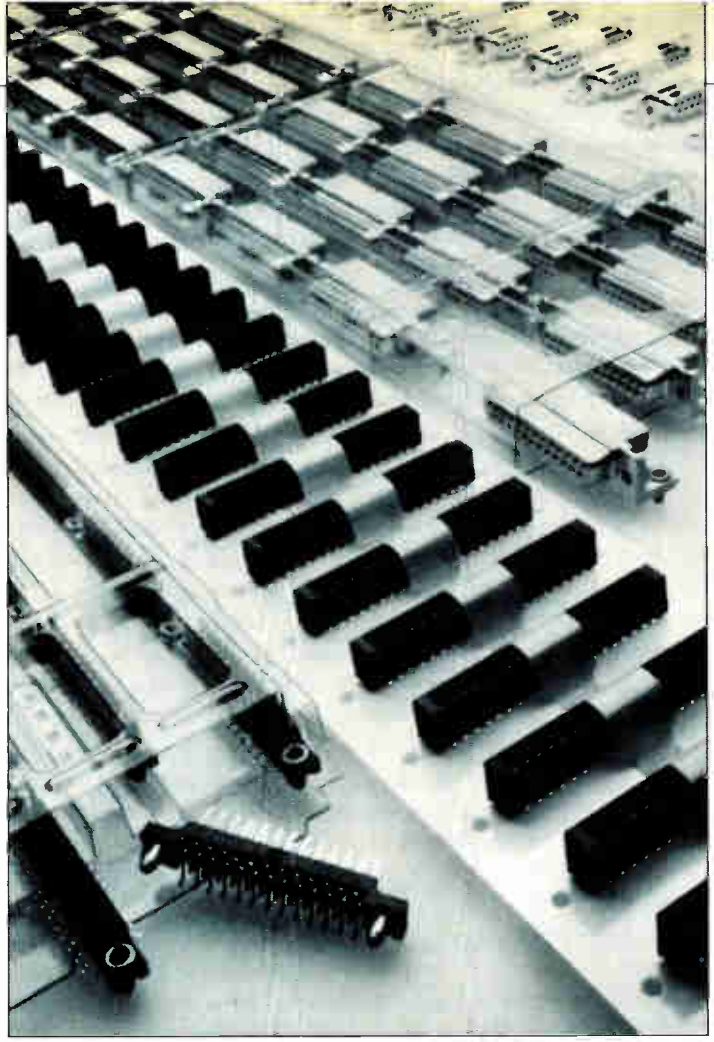
SOURCE: ROGERS CORP.

boards are one, use test pads; two, use test pads; and three, use test pads."

Ideally, all surface-mounted boards could be made of epoxy-glass or occasionally polyimide or polytetrafluoroethylene (PTFE) for high-speed applications. This is the case for the consumer, computer, and industrial fields, where hermeticity is generally not required and plastic carriers with compliant leads can be used.

For the large military electronics market, however, the hermetically sealed leadless chip carrier is mandatory for high-density surface mounting. Unfortunately, the large thermal mismatch between the carrier's alumina body with a thermal coefficient of expansion of 6 ppm/°C and, say, an epoxy-glass laminate with a TCE of about 15 ppm/°C results in stresses that cause solder joints to crack over the military temperature range of −55°C to +125°C.

There are three solutions. The first is a board material that will nearly match the TCE of the alumina carrier. A second is to put leads on the ceramic carrier, but this adds expense to an already costly unit. A third is to replace the leadless ceramic carrier with a plastic leaded unit that contains some sort of humidity proofing. A task force of the Institute of Electrical and Electronics Engineers' Computer Packaging Society is now investigating this approach [*Electronics*, April 28, 1986, p. 18].



6. PACKAGED FOR AUTOMATION. For automated placement, connectors come in tubes, tape, and trays. Robots require special trays.

The military has concentrated on the first method, approximately matching the ceramic's TCE. A popular method is to use either copper-invar-copper, copper-molybdenum-copper, or epoxy-graphite as the inner core of a multilayer structure basically built of epoxy-glass signal layers. The inner core's characteristics dominate the composite TCE and match that of the carrier's ceramic.

This method is being used successfully on several military programs. It adds weight and puts increased strain on plated-through holes, however, because additional strain during soldering or thermal shock is translated into the Z direction because expansion is restrained in the X and Y axes.

A variation is to use rigid composites, such as polyimide reinforced with Kevlar or quartz, to achieve the low TCE required (table). These materials have low enough TCE values to keep shear strains on the solder joint to a minimum. However, routing and drilling of quartz and Kevlar fabric-reinforced composites are extremely difficult. In addition, microcracking of the brittle polyimide matrix resulting from excessive radial expansion of Kevlar fibers has stalled the widespread acceptance of polyimide-Kevlar.

At the Institute for Interconnecting and Packaging Electronic Circuits conference in Boston last month, Dave Arthur, technical manager at Rogers Corp., Rogers, Conn., discussed a new approach based on a new PTFE-glass material called RO-2800. This material lowers TCE to reduce shear strain and also makes the entire pc board compliant enough to absorb stresses.

Preliminary thermal-shock tests on chip-carrier-laden boards of epoxy-glass, polyimide-quartz, polyimide-Kevlar, PTFE-microfiberglass, PTFE-woven glass fabric, and RO-2800 materials showed RO-2800 bettering all the other materials, Arthur said. Interestingly enough, the RO-2800 has a modulus only 2% that of epoxy-glass but a higher TCE. It appears that the added compliancy overwhelmed the effect of the higher TCE of the fluoropolymer material. Rogers is running further tests to better understand the interplay between TCE and compliancy.

The laminate's electrical properties are also becoming more important as VLSI chips continue to accelerate in performance. Using copper-invar-copper or some other constraining material with conventional substrates may not meet the electrical needs required for these chips—the dielectric constant and dissipation factors are too high.

Laminate makers will have to supply low-dielectric-constant, low-loss materials for high-speed VLSI circuitry. As a start of this trend, both Rogers (with its RO-2800) and W. L. Gore & Associates Inc., Newark, Del., are supplying prototype quantities of PTFE-based laminates with dielectric constants of 2.7 to 2.8. By comparison, epoxy-glass rates 4.8.

Besides being suitable to high-speed operation, laminates of this type will allow thinner boards for a specified characteristic impedance and closer spacing of traces for the same impedance built into a board with a higher dielectric constant. Both these factors contribute to higher packaging density. However, this type of board is really optimum for a leaded surface-mountable carrier where no thermal matching would be required.

SURFACE-MOUNTED CONNECTORS

After three to four years of watching surface mounting grow in the U. S. and getting deep into the new technology required for surface-mounting connectors, most of the major connector companies in the U. S.—such as Amp, Amphenol, Burndy, Cannon, Dupont Connector Systems, and many others—are either fully or about to be fully committed to surface mounting.

Conventional pc-board connectors require rather large plated-through holes for their many pins. Surface-mounted connectors, even in 100-mil-pitch types, save all that surface area. However, the real advantage of surface-mounted connectors comes in 50- and even 25-mil centered versions for extremely dense boards. It is considerably easier to design a high-density surface-mounting connector than to use conventional connec-

tor techniques. And the technique allows connectors to be mounted on both sides of a board.

Surface-mounted connectors are not conventional connectors with shaped leads. Rather, they are designed to meet a set of requirements that only apply to surface mounting. For example, selection of the housing material for such a connector is a function of its ability to withstand the soldering temperatures of the vapor-phase (215°C for a dwell time of less than two minutes) or infrared reflow method. This means that high-temperature thermoplastics like Ryton, Rynite, or Ultem must be selected.

Another consideration is the housing material's TCE. Too large a thermal-expansion differential between the pc board and the connector housing can cause thermal stresses on the soldered leads that can jeopardize the reliability of the connector's solder joints.

Lead design must result in good solderability and compliancy to take up much of the thermal mismatch. Because solder joints are rigid, compliance must be designed into the lead. Lead compliance has a significant effect on stresses in the solder joint (Fig. 5). The less thermal-mismatch and mechanical stress in the solder joint, the better its reliability. Compliancy in the lead can significantly reduce stresses at the solder joint, sometimes to a tenth that of a rigid lead.

Lead shape also influences the performance of a solder joint. For example, a toe-down-shaped lead compressed in a board-assembly clamping fixture can exert enough force to fracture its solder joint when the connector is removed from the fixture. Accurate forming of the lead, so it is parallel to the soldering surface, reduces this problem. None of these factors had to be considered in conventional connectors with through-the-board leads.

Surface-mounted connectors, particularly high-density types with leads on 50-mil centers, need a locating feature such as molded-in posts, because alignment of lead to pc-board pad cannot solely depend on solder joints. Finally, connector experts believe that some mechanical supplement is necessary to hold the connector to the board and relieve the stress on the soldered connections. The hold down can be a screw, a latch, or even a heat-staked post.

"About two years ago, nobody wanted to drill holes in a surface-mounting board for the hold downs for connectors, feeling that this type of board shouldn't have through holes," notes Ed Reynolds, principal engineering development manager at Amp. "Now the same people feel that drilling these large holes is simple to do and absolutely necessary."

Not all surface-mounting connectors have soldered connections. Burndy has developed solderless high-density backplane connectors in double- and quadruple-row versions on 50-mil centers. A version of this connector is being used on Digital Equipment Corp.'s recently announced VAX 8200, 8300, and 8800 superminicomputers.

7. ROBOTIC HANDLING. The odd shapes and tight tolerances of surface-mounted connectors suit robots rather than pick-and-place machines.

A big advantage of surface mounting is that it can be automated. Therefore it is not surprising that surface-mount connector design must be compatible with automation, whether it is in the form of pick-and-place machine or robot. In these cases, the connector's shipping or storage media is critical.

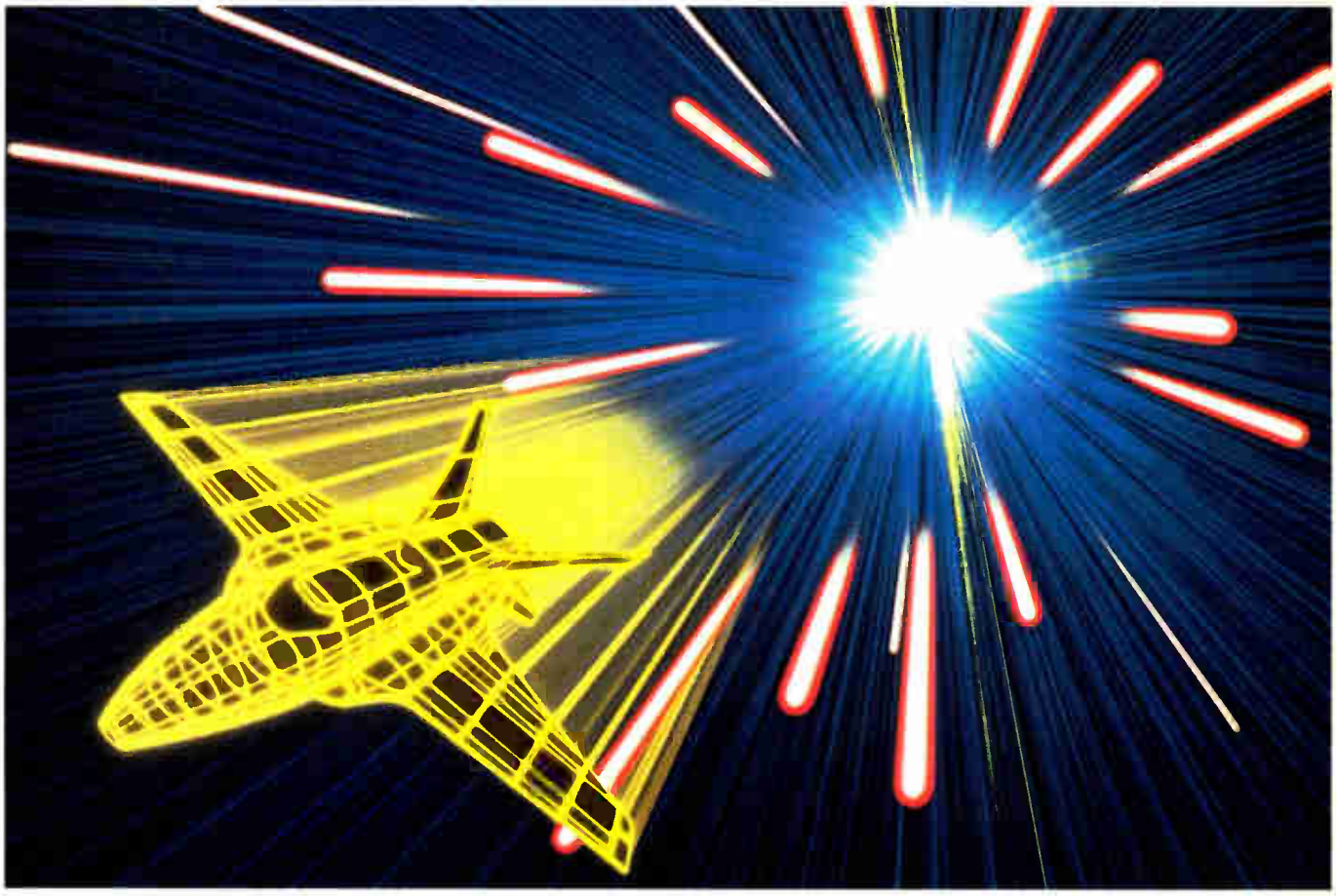
Three methods have emerged to mate the connectors with automation (Fig. 6). The first is to package the connectors in a tube somewhat similar to a DIP tube. This magazine is used to feed connectors to a pick-and-place machine.

A second method used for smaller connectors is to put them on reels of tape similar to those used to feed passive chips and small chip carriers on a pick-and-place machine. Third, for large components that have to be handled by a dedicated robot, connectors can be packaged in special trays. The robot can be programmed to remove a unit and move it to a board being populated with components. Amp goes one step further in helping a customer automate by supplying special grippers for robots and application modules for placement machines handling their connectors (Fig. 7).

It is important to note that whatever packaging and feeding technique is used must not affect the coplanarity of the surface-mount solder tails and must provide easy access for a robot gripper. Some robots may require specific smooth surface areas on the connector for vacuum pickup. Today, practically every type of connector is available in a surface-mounted version. Amp and Burndy have surface-mounting versions of all their products, and the other major connector companies will follow shortly.

With large computer companies such as DEC and IBM Corp. already applying Burndy's surface-mounted connectors in their latest equipment like the new VAX series and the IBM laptop computer, the application of high-density SMT connectors should speed up as the the rest of the electronics industry strives to catch up. □

NEC NEWSCOPE



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Our μPD77230 Advanced Signal Processor breaks the floating-point barrier in digital signal processing (DSP) with unprecedented speed and accuracy.

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In addition to its large internal memory blocks (512 × 32 × 2 data RAM, 2K × 32 program ROM and 1K × 32 data ROM), the 77230 provides external expansion up to 4K of program RAM and 8K of data RAM. Serial and parallel I/O also add flexibility. The serial interface allows cascading, links with codecs and AD converters while the parallel interface supports master- and slave-mode operations.

The 77230 is ideal for image processing, graphics workstations, telecom and other applications requiring high speed and high precision.

NUMBER 135

NEW ZEALAND GOES DIGITAL WITH NEW FOTS AND NEAX61.

Plans for a nationwide Integrated Digital Network (IDN) in New Zealand, where the telephone ownership rate is among the highest in the world, are rapidly taking shape.

The New Zealand Post Office selected NEC to supply state-of-the-art 140MB fiber optic transmission systems (FOTS) and digital switches that will bring the digital future clearly into view.

NEC will provide all the necessary optical terminal and repeater equipment for the fiber optic systems to be installed in links covering Wellington, Auckland, and other major cities.

NEC's 140MB FOTS provides high-quality communications paths equivalent to 1,920 telephone channels. High-performance optical devices enable long repeater span. It also features in-service system monitoring functions, low power consumption and compact size. A slim rack, measuring 2.75m(H) × 0.12m(W) × 0.225m(D), accommodates three terminal systems.

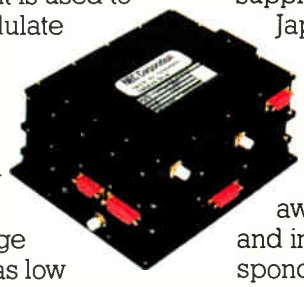
For the development of its ISDN, the New Zealand Post Office selected NEC's enhanced NEAX61 digital switching system with ISDN capability. Nearly 100 systems, including toll and international switches, are to be supplied within a five-year period.

NEAX61 digital switches with an aggregate total of 5 million lines are now in service in 36 countries.

NEC TRANSPONDERS SELECTED FOR INMARSAT-2.

NEC satellite transponders will play a key role in INMARSAT-2, the second generation of international maritime communications satellites.

NEC was recently awarded a contract from British Aerospace Public Limited Company to supply TT&C C-band transponders. This technology-intensive equipment is used to receive and demodulate telecommand signals, to transmit telemetry signals, and for ranging.



The transponder design will include various leading-edge technologies such as low noise amplifiers (Noise figure: 2.5dB), SAW filters to achieve excellent band-rejection performance (60dB min. ±2MHz from center frequency), threshold extension FM demodulation to achieve high sensitivity, and hybrid microwave ICs to minimize equipment size and weight, plus high-efficiency high-power amplifiers (RF output: 6W min.).

As one of the world's leading suppliers of satellite transponders, NEC has contributed to a number of international programs, supplying hundreds of advanced transponders for INTELSAT-IV, IV-A and VI series of communications satellites.

NEC has also integrated and supplied all the transponders for Japan's communications satellites, including the world's first two Ka-band satellites, and various TT&C (tracking, telemetry and command) transponders.

Additionally, NEC was awarded a contract to develop and integrate high reliability transponders for BS-3a and -3b, Japan's next generation of direct broadcasting satellites.

ALL-SOLID-STATE UHF TV TRANSMITTERS.

The latest 30kW UHF TV transmitter from NEC sets a new standard for high output power in all-solid-state design.

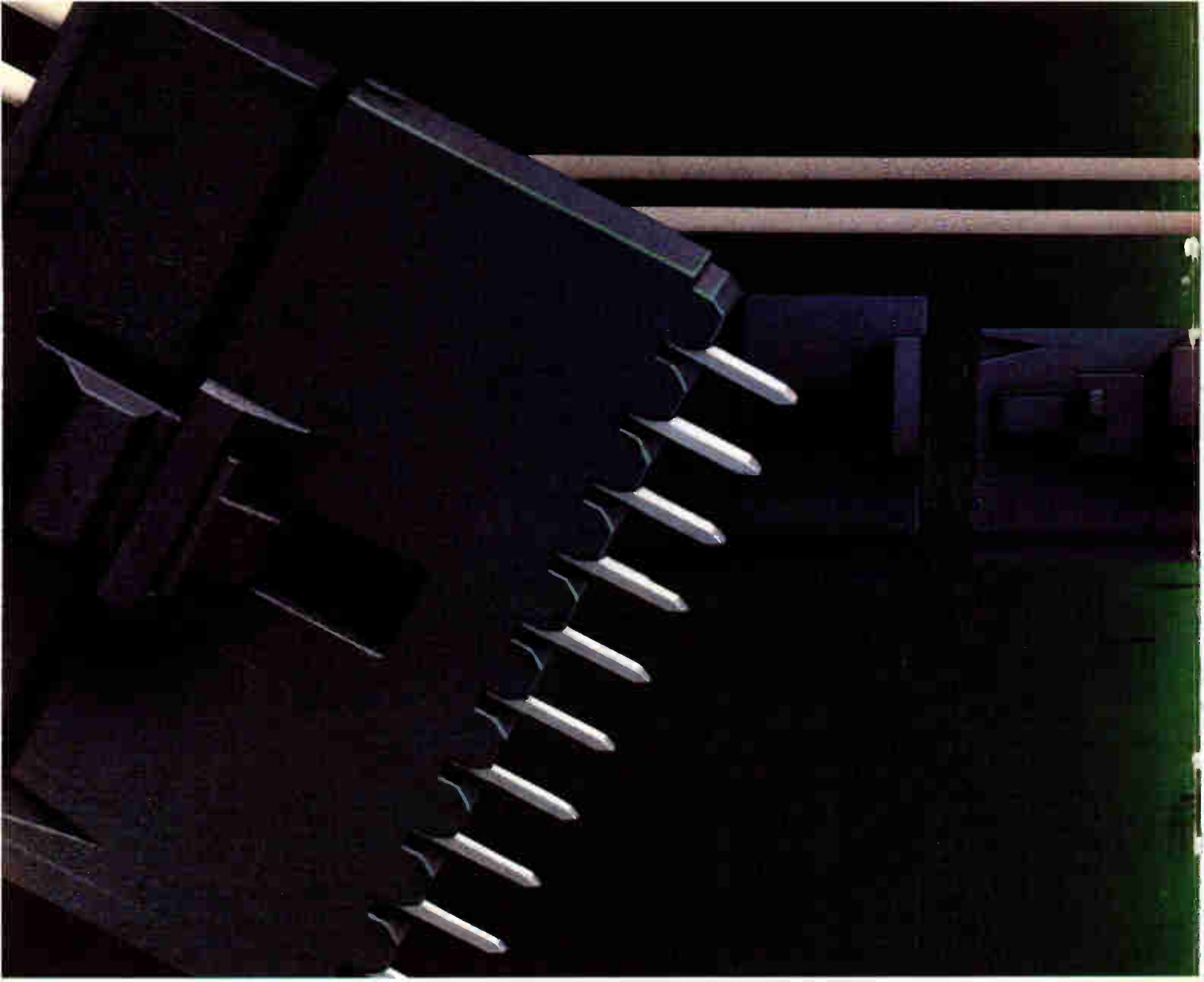
The 30kW transmitter incorporates many enhancements including high-performance exciters, powerful transistor power amplifiers, low-loss RF combiners and high-efficiency switching regulators.

The 1.2kW transistor power amplifier, utilizing reliable, high-power and high-gain (120W typical and 7dB min. at 860MHz) bipolar transistors which were developed in-house, features a remarkably reduced component count—only 1.7 times larger than the conventional 300W PA.

Compared to tube types, the new transmitter features greatly enhanced economy and reliability. Safety and maintainability are also improved, while power consumption is reduced by approximately half.

NEC's new all-solid-state UHF TV transmitter series includes 15kW, 10kW, 5kW and 3kW models. A 30kW system is already in satisfactory operation.

NEC



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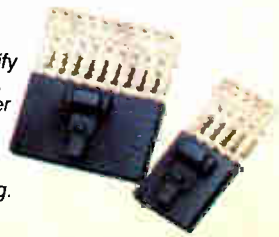
You'll appreciate the design freedom we've added to our line—with mass-terminating AMPMODU MTE connectors. Receptacles stack side-by-side or end-to-end, to take 22-30 AWG wire anywhere on the board with complete modularity.



Pre-loaded assemblies simplify mass termination. Interlocking carrier strips accurately locate insulation-displacement contacts in tooling.

Circle 31 on reader service card

connector.

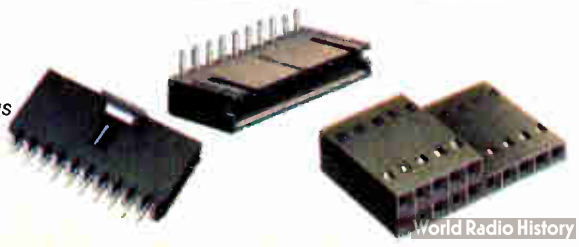
You can also choose polarized or latching receptacles, or special ribbed receptacles that gang into single- and double-row coupling shrouds. Pin contact types and shrouded headers round out the wire-to-wire and wire-to-board picture.

MTE connectors are backed by a full range of application tooling, from hand and semi-automatic to fully automatic, to meet any level of production you need.

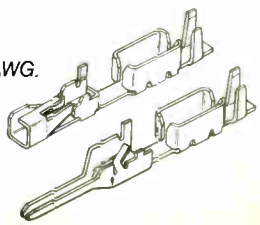
Call (717) 780-4400 to find out more. Ask for the AMPMODU MTE Connector Desk. AMP Incorporated, Harrisburg, PA 17105-3608.

AMP Interconnecting ideas

Vertical and right-angle headers, receptacles, and shrouded housings provide modular approach.



Do it all in two contact sizes— 22-26 AWG and 26-30 AWG. Dual-beam contacts are overstress-protected, and feature post stops for use on long posts.



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12-05.86.02

CHECKING OUT VLSI WITH STANDARD TEST GEAR

ETA'S SELF-TESTING SCHEME GENERATES MOST TEST OPERANDS ON CHIP

When ETA Systems Inc. delivers its first supercomputer in October, clearly the system's single most important attribute will be the extent to which it can check itself out. By taking on more test tasks than any existing scheme, this next-generation design not only extends the reach of on-chip self-testing but also radically simplifies the job of external testing. The ETA 10 is being built with 20,000-gate CMOS arrays that incorporate what the Control Data Corp. spinoff calls BEST, for built-in evaluation and self-test.

The patented self-testing concept is highly important to the St. Paul, Minn., company. "I've had several ETA employees come to me and say that without BEST, we wouldn't have a system," notes David R. Resnick, ETA senior technologist and BEST's principal designer. Unlike other self-test concepts, BEST generates most of its test operands on chip, permitting highly complex arrays to be checked out with standard test equipment. Self-generation of operands means that test engineers won't have to originate so many tests and the resulting test data base will be much smaller. Another way that BEST goes beyond other self-testing approaches is that it pinpoints which chips—and even which wiring between chips—are bad. Such precise fault isolation helps in manufacturing checkouts and will greatly simplify system maintenance, says Resnick.

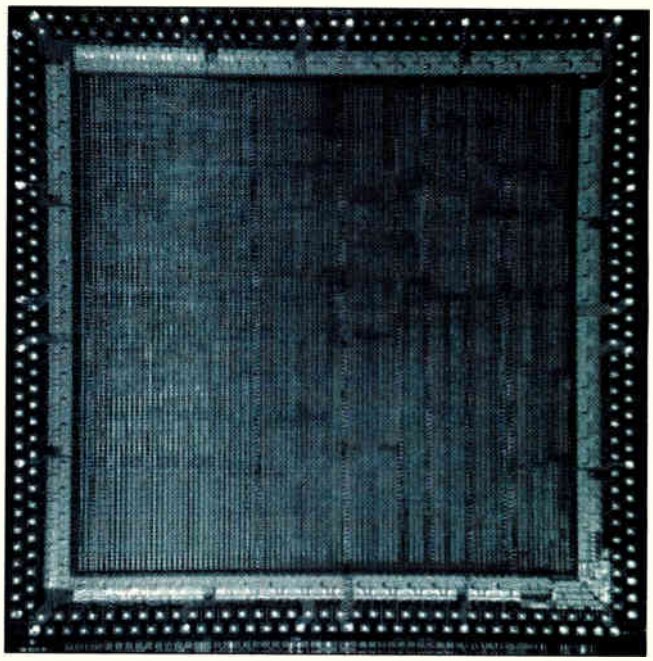
Besides playing a major role in ETA's supercomputer, BEST is soon expected to perform the same sort of job in other systems. The 20,000-gate array [*Electronics*, Feb. 24, 1986, p. 36], which has gate delays in the subnanosecond region, is being manufactured for ETA by Honeywell Inc.'s Digital Product Center in Colorado Springs, with a 1.2-μm single-polysilicon, double-level-metal n-well process. Honeywell is also offering the chip commercially.

Another advantage to the BEST approach is that it's very stingy with real estate, according to Resnick. It takes up only about 6% of the chip area, which compares with a 12% average for other self-testing approaches and as much as 20% for methods such as the level-sensitive scan-detection (LSSD) technique developed by IBM Corp.

Several major design goals were set when ETA initially decided on a strategy calling for testability at all levels of supercomputer design, Resnick says. One was to implement an approach that would allow the testing of complex, high-pin-count chips with today's IC testers. "There are very few testers in the industry that will handle the 238 signals that we needed to connect to," he says. "We needed to come up with a way that would help us test the die using things like existing Sentry testers."

Another goal was to simplify system testing by reducing the number of tests that a large number of chip types in one system would need. The ETA 10 will use more than 90 different versions of the basic array, and BEST will test them all with the same basic test. This eliminates the need for a wide range of tests and the army of test engineers to invent them.

TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*



1. SELF-HELP. Eta Systems' CMOS gate array contains self-test circuitry that simplifies the testing of these complex ICs.

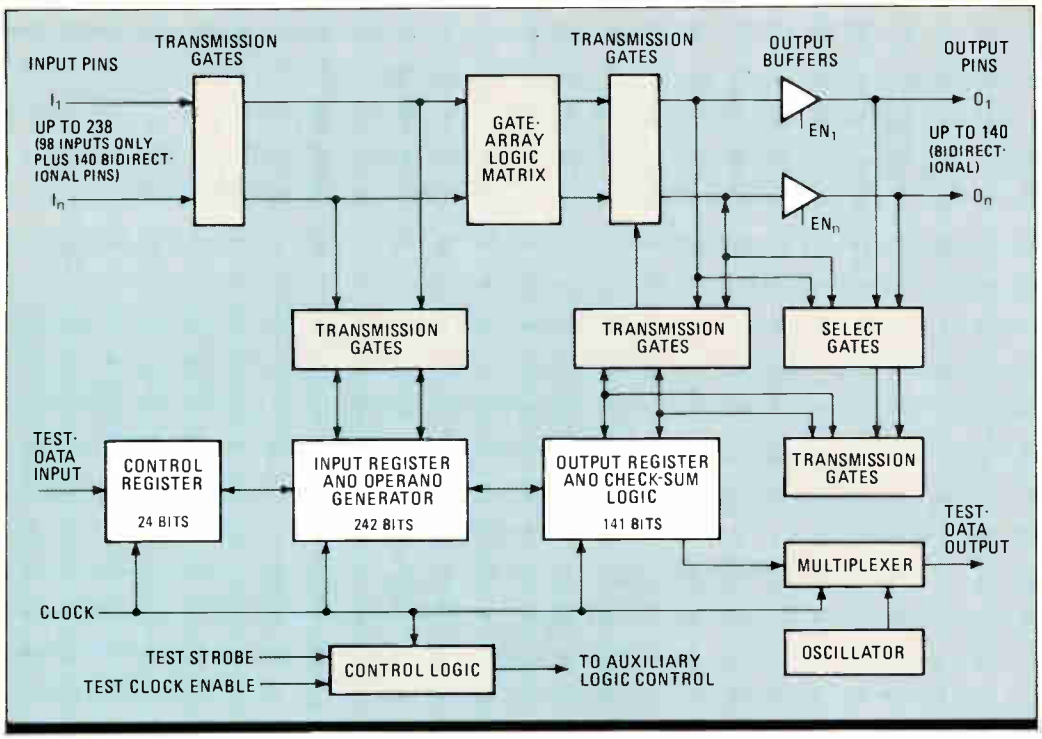
ETA also wanted a self-test setup that would detect and isolate failures in the wiring, even for an intermittent failure that might elude conventional diagnostic tests. This is because experience with earlier supercomputers showed that the majority of failures were not in ICs but rather in wiring, sockets, and other interconnection components, Resnick says. The company also wanted a test technique that could point to which chip on a board is failing—something that other current maintenance systems can't do.

SIMPLIFYING MAINTENANCE

System maintenance also received major emphasis in the development of BEST. ETA wanted to reduce the level of skill required to run checkouts in manufacturing, maintenance, and field repair. Also, self-testing chips would help overcome the obstacles of tight pin spacing on the complex array chips, and a large part of the system will be immersed in liquid nitrogen for cooling.

As a CDC spinoff, ETA employs many key technical people who were involved in the design of CDC's Cyber 205 supercomputer and earlier high-powered machines. So it was natural for ETA to use that work as a starting point. BEST, in fact, is a next-generation version of a self-testing chip technique developed at Control Data called the on-chip maintenance system.

One important attribute that BEST shares with the Control Data technique is implementing the self-test circuitry in 2,000 gates on the chip's periphery (Fig. 1). Every version of the basic array, then, will have the same test logic in place. About 18,000 of the array's 20,000 gates are available for customization; an additional 1,000 to 1,500 gates serve functions such as



2. SPACE SAVER. The BEST scheme occupies 2,000 gates on the array's periphery. Three serial shift registers—input and output registers along with a control register—make up the heart of the self-testing circuitry.

I/O buffers, three-state capability, and clock distribution.

BEST requires four dedicated pins out of the 284 pins on the array, plus a clock pin and appropriate power and ground. Another pin, called the hold-off pin, can be used as an option to prevent short-path problems among chips in a system. The on-chip BEST circuitry includes three serial shift registers: input and output registers, which are associated with the array's 238 I/O pins, and a control register (Fig. 2).

The longest is the input register, which contains 1 bit for each of the 98 input pins plus 1 bit for each of the 140 bidirectional output pins on the IC. Another 4 bits are used when the input register is employed as an operand generator. This generator creates pseudorandom numbers that are sent to all gate-array inputs when the part is under test, instead of applying operands to the input pins from the outside. The input register therefore contains a total of 242 bits.

The output register contains 140 bits, 1 for each of the 140 possible output pins, and an additional bit in a separate 1-bit register. This last bit can be taken off chip through a four-way selector in order to get information such as clock-bus data to aid in clock tuning, input from an on-chip ring oscillator for use in ac part grading, and various types of debugging and status data from the array.

The control register contains 24 bits. Ten of these are used to control the various functions of the I/O registers. The remaining 14 are spares that can be used by the logic designer to implement his own tests.

GENERATING OPERANDS ON CHIP

In its self-test mode, BEST works by having the input register generate operands instead of having them generated from the outside by an external tester. This approach radically simplifies the amount of test data that must be generated and stored in a test system. It also provides for faster testing because there's no need to put in data at a rate limited by the channel speed of the external tester. When beginning the test, the user must supply a seed value as a starting point for the pseudorandom operand generator. Based on this known value, the array logic will respond in a deterministic manner by producing a predictable result if the array is working properly. The array outputs resulting from the operands are check-summed, deposited in the output register, and then checked by the user for the expected result.

Because the different versions of the array vary in the complexity of the testing they require, the user can vary the number of clock cycles in which the internal operands are applied. More complex parts may require a larger number of clocks to ensure sufficient test coverage. "So in order not to have to look at the output register and the check-sum logic in each clock, we fold the operands into a sum, specifically a parallel check sum," according to Resnick.

The BEST control register takes its input from the test-data input pin controlled by two dedicated pins, test strobe, and test-clock enable. When the test strobe is activated, or brought high, the contents of the control register are held, the chip's input buffers are turned off, and control signals from the control register go out to the BEST circuitry. The input register is then connected to the chip array, and the operand generator starts pumping operands through the array.

The test-clock enable pin controls the clock signal to the test logic. When the test strobe is dropped, the enable pin reads out the contents of the output register at the test-data output pin. The user then checks for the proper result.

The upshot is that only three pieces of information are necessary to perform functional tests on a chip that carries BEST logic: the starting operand for the test, the number of clocks required to run the test, and the expected result. "What we have is a test skeleton," Resnick notes. The test sequence is a simple process of applying a sequence of data to the BEST input pin in order to load a seed operand, and then having the part test itself for a certain number of clock cycles.

"During that self-test, you're not interested in looking at any of the input pins or output pins," Resnick says. "You're just sitting there counting clocks. At the end of the test, you take the part out of test mode, shoot the results off, and you look to see if you got the right sum. So this basic test is just about totally independent of the logic function of the part."

This independence means that BEST greatly reduces the need to develop different tests for the different versions of a gate array. Only a seed algorithm is needed to test any array customization, regardless of its logic function. As well as allowing a much smaller test engineering staff, the radical reduction in the number of tests also cuts the size of the test data base.

Because only the single seed algorithm must be supplied to the chip, BEST allows a part to be functionally tested at the full operating rate, even when a much slower tester is being used. That's because the test-clock enable pin can be used to load and unload data at speeds that are compatible with the lower-performance test-clock rate.

In addition to its functional testing capabilities, BEST pro-

vides for parametric testing. "One thing that the control register can do is force output buffers on or off, and one of the bits in the control register that gets fanned out can turn the tristate logic on or off. This means that we can do parametric tests independent of the logic function of the device," says Resnick. "Let's say that you want to force on a particular output pin to the one level, so that you can see the voltage level. What you can do is put all 1s into the output register, put the part into the mode that forces the output register onto the output pins, and have the control register force all of the output pins on and perform your test."

When BEST is in the self-test mode, the input and output pins are disabled, and the parallel check-sum results are dumped to the output register, which can be read from the test-data output. The data collected in the output register also can be forced off the chip through the output pins, and data can also be put into a chip's BEST input register from the input pins. This capability allows BEST to be used to perform dc tests on the wiring between two chips, once self-tests have shown each of those chips to be good. In this mode, a test operand held in the output register of the first chip is forced out through the output pins to the input pins of a second chip to which it is connected. The result is caught in the input register of the second chip and is then shifted off the chip and observed. If it matches the expected result, the wiring is good; if not, the wiring is bad. This test requires only one clock cycle.

ISOLATING INTERMITTENT FAULTS

Using a slightly different approach, tests for sequence-dependent intermittent faults associated with wiring between known-good chips can also be performed. In this case, the first chip is put into its self-testing mode but with the output pins on, so that the data patterns out of the array go to a second receiving chip. The second chip is also put into the self-testing mode, but with the input pins on. This test can be run for any desired number of clock cycles, allowing for a wide range of data patterns. If the result from the second chip doesn't match the expected result, the problem is isolated to the interconnection. The source of the intermittent fault can then be determined through ETA software that simulates the test and allows the results to be examined after each clock cycle.

The same feature that allows data from the input pins to be loaded to the BEST input register also allows the status of the input pins to be captured at any time while the chip is operating. This aids in debugging, since it leads to tests like those a logic analyzer would run, says Resnick. "It's not as good as having all the status data in a chip that a scan design would allow you," he concedes. "However, we can perform the sequence repeatedly, moving the window at which we catch the input register, and thereby build a test-analyzer function just like a Biomation analyzer."

BEST is also designed to ease the task of the maintenance engineer. Chips can be hooked up in serial chains in which the test-data output is simply hooked to the test-data input on the next chip. The BEST output is designed so that when the test strobe is brought up and then back down, it causes a code to be transferred to the control register, overwriting its contents.

The first 2 bits of the code are always a 1 and a 0, so the test-strobe pins on all of the chips in a serial maintenance chain can be raised and lowered, and then the test-clock enable pin can be used to ship the contents of the control registers of the parts through the chain. Using system maintenance tools, an engineer can then determine where a failing component is located in the chain.

The problem is then easily isolated. Because each control register contains 24 bits, the source can be found by simply counting the clocks and looking for the 1-0 code at the appropriate points, Resnick explains. "You can start counting, and a certain number of clocks later, there's a 1-0 code, and a certain number of clocks after that, you get all 0s. That says that between this point and that point, your ring is broken, and you know exactly where to go look."

Part of the code that is overwritten into the control register when the test strobe is brought up and then down is used to identify the chip type. This code segment is specific to the logic option of the array, together with its revision number. (The part-identification data is part of the gate-array netlist specified by the logic designer.) The data can then be read out using the test-clock enable pin. This feature is useful both in board manufacturing and in maintenance, for verifying that the right chip types at the proper revision levels are in the right spots on a board, Resnick says.

BEST's chip testing capabilities and its ability to isolate bad parts and wiring have proven valuable to ETA across a broad range of tasks, from chip debugging to incoming inspection of devices, manufacturing checks, system clock tuning, and maintenance. "What we've done is to expand the system so that it tests both within the chip and outside it," says Resnick. BEST also forms a basis for testability enhancement, he adds. In addition to the basic test modes, "you've got the complete capability of the control register to control each bit individually, so that you can invent your own tests." That capability goes beyond other chip self-test schemes, he says. □

BEST DESIGNER KNOWS WHAT IT TAKES

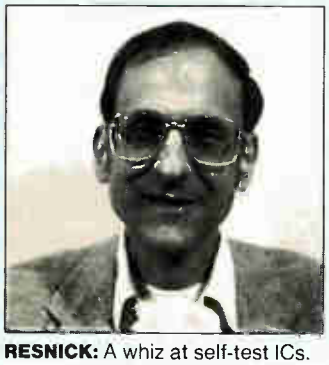
With a career in supercomputers that spans customer engineering as well as extensive work in logic and system design, ETA Systems Inc. senior technologist David R. Resnick knows what it takes to design, support, and maintain a supercomputer. For ETA Systems, that experience seems about to pay off handsomely.

Resnick, 45, was part of the team transferred when Control Data Corp. set up ETA Systems Inc. in September 1983 to design a next-generation supercomputer. At Control Data, Resnick worked on the Cyber 205 and other large systems and was one of the designers of a 6,000-gate array that in 1981 was the first to include a self-testing chip scheme, known as the On-Chip Maintenance System. Now he has taken the concept even further. He has come up with a next-generation chip self-testing scheme known as BEST (for built-in evaluation and self-test) that has been indispensible in the design of the forthcoming ETA 10 supercomputer.

As the principal BEST designer, Resnick's name appears on the patent applied for on the technique, together with Randy Bach, another ETA senior technologist. Resnick already holds two other patents for logic design with another in the application stages.

Logic design is not his only forte, however. After graduating with a BSEE from the University of Arizona in 1968, he joined Control Data as a customer engineer. The first-hand knowledge of customer concerns he gained then helped in later work for the Minneapolis firm. At both Control Data and ETA, Resnick's contributions have spanned work at both the systems and logic level. Besides developing BEST, he is the designer of a number of the logic macros that will be used in the 20,000-gate array chip options.

But Resnick feels that BEST is clearly his most important contribution to the ETA 10 effort. "BEST will be critical to the success of ETA Systems, not only in selling its supercomputers, but in being able to do proper maintenance and other functions," he says.



RESNICK: A whiz at self-test ICs.

MATHEMATICAL PROOF VERIFIES ERROR-FREE PROCESSOR DESIGN

ALGORITHM ENSURES THAT 16-BIT CHIP HAS NO HARDWARE BUGS

Proving out a new microprocessor design is as tough a challenge for hardware designers as coding an error-free program is for software engineers. As a result, hardware designers are starting to pick up new tricks, some borrowed from their software counterparts; they are using mathematical techniques to specify, design, and verify chip designs before fabrication. The goal is to catch problems before a chip hits the market.

Though rarely applied in the past, these techniques are gaining popularity and achieving results. The result of one recent effort is Viper, the 32-bit Verifiable Integrated Processor for Enhanced Reliability developed at the UK's Royal Signal and Radar Establishment [*Electronics*, Jan. 27, 1986, p. 53]. Now researchers on this side of the Atlantic have come up with a chip they describe as a formally specified and mechanically verified microprocessor. Using an automated theorem-proving system, research associate Warren A. Hunt Jr. and computer-science professor J. Strother Moore III of the University of Texas at Austin developed the 16-bit FM8501 microprocessor. It is aimed at critical applications where errors cannot be tolerated.

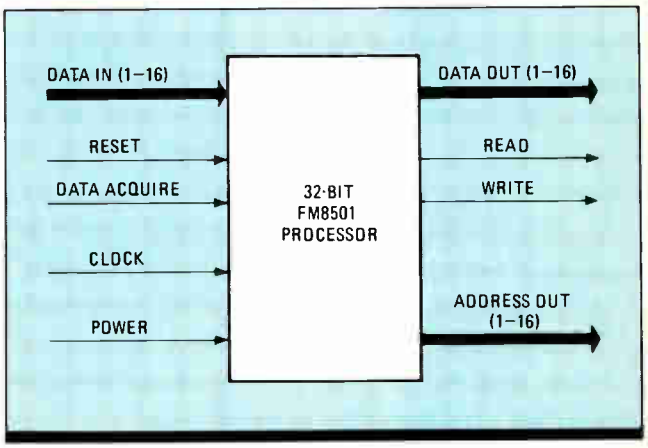
The words "formally specified" in the researchers' claim mean that the design of the FM8501 was expressed as a set of formulas in a mathematical logic. Another set of formulas expressed the functional specification of the device. Hunt and Moore then proved mathematically that the chip, as designed, actually implemented its functional specification. To do this, they used mechanical verification techniques: a mathematical theorem prover in the form of a computer program.

"We wanted to provide a microprocessor free of all logical errors," says Moore. Mechanical verification tools, originally developed for the verification of software, were used for the FM8501. The operation of the FM8501 was specified and verified with respect to all instructions and their effects on three mathematically constructed data types: Boolean bit-vectors, natural numbers, and integers.

Designed for general-purpose applications, the FM8501 features a symmetrically organized instruction set. There are eight general-purpose registers, one of which is the program counter. Register-to-register, register-to-memory, and memory-to-memory operations are allowed with all instructions. Two-address instruction formats, as well as register, register indirect, register indirect with post-increment, and register indirect with predecrement addressing modes, are supported for all instructions. Other features include general-purpose conditional move instructions; Boolean, natural number, and integer operational specifications; a separate arithmetic logic unit for effective address generation; memory-mapped input/output; and 128-K bytes of memory.

Internally, the FM8501 is a microcoded device. The microcode is used to control instruction decoding and internal data movement. A separate ALU is used for effective address calculations, increasing the performance of the microprocessor.

All registers may be used as index registers or as software stack pointers. Four status bits—carry (C), overflow (V), negative (N), and zero (Z)—can be conditionally set by every instruction. The FM8501 can access 2^{16} memory locations, each one word (16 bits) in size; it can manipulate 128-K bytes of memory.



GOING OUTSIDE. Nine functional signal groups connect the formally specified FM8501 to the outside world.

All the instructions are one 16-bit word in size. Every instruction specifies a source and a destination location, each of which is either in a register or in memory. Instructions for the FM8501 specify two kinds of information: the operation to be performed and the location of the operands on which the operation is performed. Every instruction has a source and a destination. If two sources are required, the destination operand serves as the other source before being modified (that is, the FM8501 has a two-address architecture). Because there are no special instructions for input/output, I/O devices are connected to the FM8501 as memory devices (memory-mapped I/O).

Major signal groups for the FM8501 are address outputs, data outputs, data inputs, read- and write-control outputs, reset and data-acquire control inputs, clock, and power (figure). All output signals are bistate and internally synchronized. All input signals are assumed to be bistate, and input values are sampled at the falling edge of the input clock signal.

Formal specification aims at a chip free of logical errors

The hardware-verification methods developed for the FM8501 were constructed in conjunction with an automated theorem-proving system that was already available. Mathematical operations were defined in a formal theory, and then these operations were shown to be equivalent to a graph of gates. The mathematical operations used consisted of common functions such as addition, subtraction, and shifting. The implementation is characterized by nests of Boolean functions applied to components of bit-vectors.

The formal logic used was the Boyer-Moore logic developed by Robert S. Boyer and Moore and described in their work, *ACM Monograph Series: A Computational Logic* (Academic Press, 1979). The logic resembles the programming language Pure Lisp. The computer program that constructs and checks proofs in this logic is called the Boyer-Moore theorem prover. The user of the theorem prover can give commands to define new functions and prove theorems. Each time a user-supplied theorem is proven, the system builds that theorem into an evolving data base, which is used to guide subsequent proofs.

By giving the system a carefully considered sequence of gradually deeper theorems, the user can guide it to discover the proofs of deep theorems. In the past, the theorem prover has proven the correctness of many computer programs and algorithms. For example, it proved that the Rivest–Shamir–Adleman (RSA) public key encryption algorithm [*Electronics Week*, May 20, 1985, p. 30] is invertible.

The formal description of the instruction set of the FM8501 takes the form of a recursive function. The function is, essentially, an instruction interpreter for the FM8501 machine language, written in Pure Lisp. The function takes seven arguments. The first six represent the programmer-visible state of the FM8501, the register file, memory, and four condition flags. The seventh argument represents time and specifies how many instructions are to be executed. The function delivers as its value the final state of the machine. The function is defined recursively: for each instruction to be executed, the new state is specified in terms of the old state.

CASE ANALYSIS

The specification takes the form of a case analysis on the type of instruction addressed by the program counter. This case analysis can be read as a formal programmer's manual because it enumerates all of the instruction types and specifies the effect of executing each. The specification is in terms of familiar math functions defined earlier, such as plus and the 2's complement representation of integers as bit-vectors.

The hardware design of the FM8501 is specified as another recursive function. The function can be thought of as a microcycle interpreter. It has 20 arguments, six of which represent the programmer-visible state, and the remainder of which represent the internal state or time. The function is defined recursively to update the state-holding arguments once for each clock tick. However, all the state-holding arguments contain bits, bit-vectors, and arrays of bit-vectors, and the mathematical functions that describe the arrays' new values in terms of their old ones are all defined in terms of Boolean logic.

Here, the description is unusual in that the sizes of the bit-vectors and arrays are generally unspecified at this level. The combinational logic that determines the new value of an n-bit-wide vector is not given explicitly, because n is unspecified, but is given recursively. If particular sizes are fixed, these recursive functions can be expanded into combinational logic, and the description of the FM8501 hardware then appears as a formally expressed register-transfer model. The advantage to describing the hardware recursively (that is, for arbitrary sizes) is that its behavior can be analyzed elegantly without the explosive-case analysis that would otherwise be necessary.

The verification of the FM8501 required proving the equivalence of the instruction interpreter and the hardware design. The six components in the final state produced by executing n instructions with the instruction interpreter were analyzed. A theorem was proven, establishing that these six components are exactly the same as the corresponding six components in the final state produced by executing a certain number of microcycles. (While the precise number of microcycles required depends upon the number of microcycles spent waiting for memory to respond to read/write requests, these relations were defined explicitly as part of the verification.)

After verifying that the microcycle interpreter is correct with respect to the instruction interpreter, the microcycle interpreter definitions are expanded into a hardware gate graph. These gate graphs can then be implemented with a gate array or full-custom IC.

LOOKING AHEAD

The FM8501 will exist as a prototype built on a 5,000-gate array. In the future, a production chip design will be fabricated either at the University of Texas at Austin or at an Austin research startup, Computational Logic Inc., recently formed by researchers at the school. Moore is director of the new venture, and Hunt is vice president of hardware engineering.

The methods used in the verification of FM8501 can be used to automate the design of other hardware devices. A library of commonly used functions was created during the process of creating FM8501. Using these libraries, verified circuits can be constructed quickly.

The methods developed for FM8501 concern themselves only with the logical specification and correctness of devices. The semantics of hardware gates (AND, OR, and NOT functions) are taken for granted. Issues such as layout and implementation technology are not considered in FM8501 but will be in later systems. □

TWO SPECIALTIES PRODUCE ONE CHIP

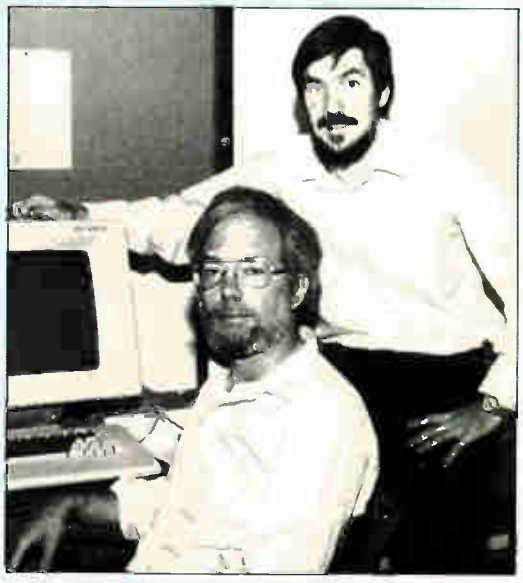
Research associate Warren A. Hunt Jr. and computer-science professor J. Strother Moore III combined two different specialties to design the formally specified and verified FM8501. Hunt is an electrical engineer by training. "I started by trying to describe formally an Intel 8080 microprocessor," he says. "But I quickly realized that I couldn't discern how all its instructions actually worked."

That's where Moore, a mathematician by training, came in. "Designers of circuits rarely start with formal descriptions and convert them into digital circuits," he says. But for the FM8501 project, the two applied Bayer-Moore logic, a formal proof that Moore codeveloped, to make sure they knew exactly how the chip's instructions would work before they built the hardware.

It took nine months to complete the project. Half that time was devoted to developing the chip's specification, and the remainder to proving it out on the computer at the University of Texas at Austin.

Hunt came to the school by way of Cyb Systems Inc., Austin, where he was a hardware and systems manager. Before that, he was a software engineer at Texas Instruments Inc. A National Science Foundation Fellow, Hunt obtained his bachelor's degree from Rice University and, last year, a PhD from the University of Texas. He now works there as a research associate.

Moore joined the school as an associate professor in 1981. Last year, he was made a full professor. He has a bachelor's degree from the Massachusetts Institute of Technology and a doctorate from the University of Edinburgh. He has worked at TRW Systems Group, Houston; the Xerox Palo Alto Research Center; and SRI International, Menlo Park, Calif.



DYNAMIC DUO. J. Strother Moore III (left) and Warren A. Hunt Jr. designed the FM8501.

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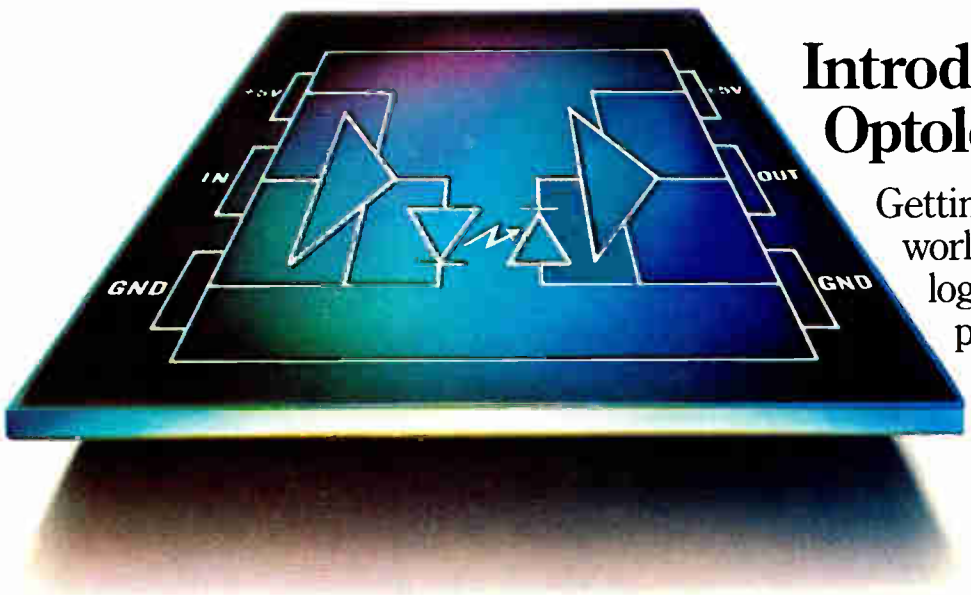

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isolator thinks gital IC.

In another common application, AC/DC precision level sensing is possible because of the well-defined input threshold.

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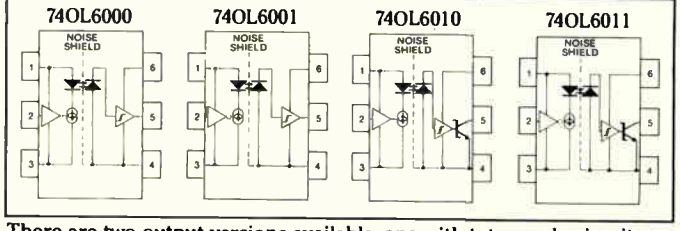
Propagation delay of the Optologic coupler is 60ns and supports datacom to 15 MBaud. The built-in internal noise shield offers 15kV/μs common mode transient rejection. 2500 VAC RMS isolation for one minute corresponds to a 440 VAC working voltage.

PART NUMBER	LOGIC COMPATIBILITY		LOGIC FUNCTION	OUTPUT CONFIGURATION
	INPUT	OUTPUT		
74OL6000	LSTTL	TTL	BUFFER	TOTEM POLE
74OL6001	LSTTL	TTL	INVERTER	TOTEM POLE
74OL6010	LSTTL	CMOS	BUFFER	OPEN COLLECTOR
74OL6011	LSTTL	CMOS	INVERTER	OPEN COLLECTOR



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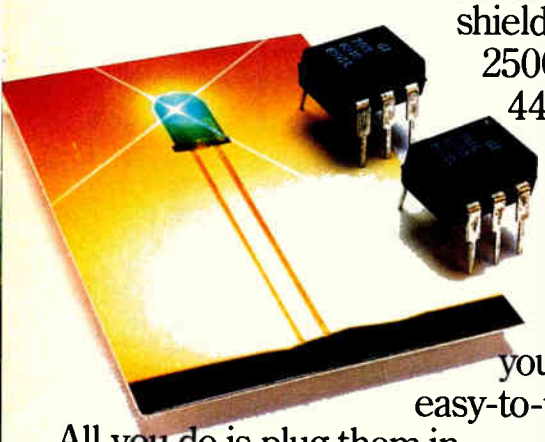

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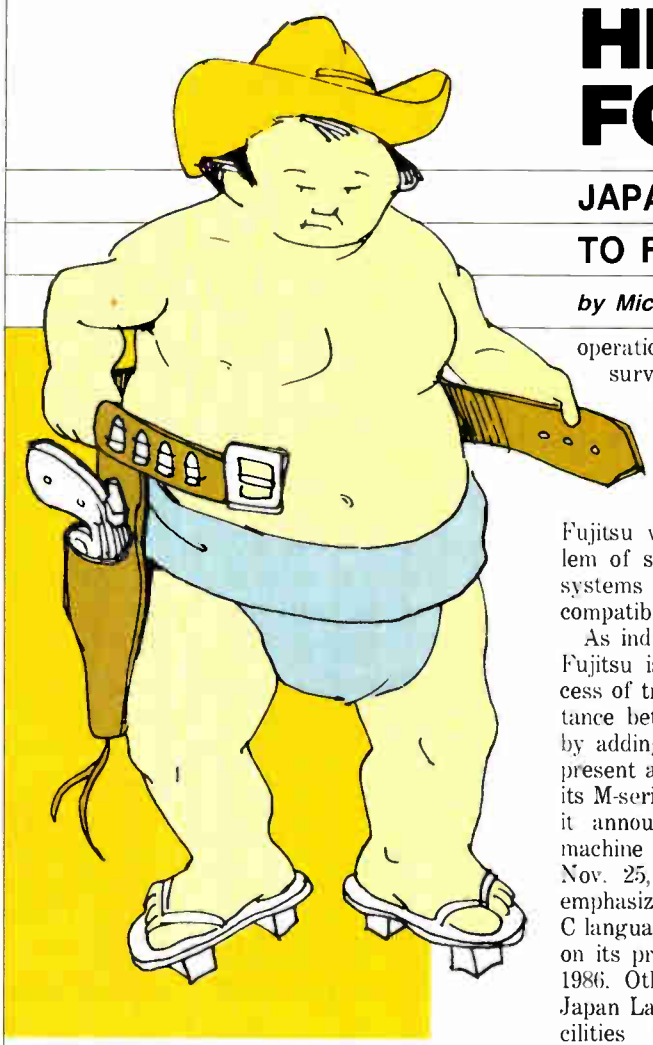


HIGH NOON FOR FUJITSU

JAPAN'S TOP COMPUTER MAKER TRIES TO FIGHT OFF IBM AND KEEP GROWING

by Michael Berger

TOKYO

It's the fear of every company that tries to compete with IBM Corp.—what happens if the computer giant tries a frontal attack? Fujitsu Ltd., Japan's largest mainframe computer company, is finding out first hand, and it's sweating.

Fujitsu has carved out a lucrative position in the mainframe market by not only offering IBM-compatible systems but the software to run on them. Now IBM is threatening this money-making business by claiming that Fujitsu's software infringes IBM's. This places the Japanese company in the excruciating position of trying to develop its own operating system to avoid costly legal battles with IBM, yet devise a system that is IBM-compatible. If it moves too far away from IBM, it risks losing a customer base that could decide to buy software, and then hardware, from IBM.

What to do so that Fujitsu's computer operations will successfully survive IBM's attack is a knotty problem. Neither the Tokyo company nor industry observers can say whether Fujitsu will resolve the problem of selling IBM-compatible systems while avoiding IBM compatibility.

As industry watchers see it, Fujitsu is already in the process of trying to put some distance between itself and IBM by adding its own features to present and future versions of its M-series mainframes. When it announced its new M-780 machine last fall [*Electronics*, Nov. 25, 1985, p. 20], Fujitsu emphasized that it would offer C language and Unix software on its products by the end of 1986. Other features included Japan Language Extended Facilities and artificial-intelligence and supercomputing functions. "We will continue to emphasize our special features," said president Takuma Yamamoto, but he insists his company intends "to continue to produce IBM-compatible products."

These special features may in fact be the limit of Fujitsu's ability to become independent. Having chosen to follow the IBM path, the company is now caught in a profitable but potentially crippling web of circumstances.

The conflict with IBM remains a critical issue for Fujitsu because sales of mainframe hardware and software account for 20% of its business. And even the considerable strength of Fujitsu's other operations—communications and semiconductors—wouldn't offset the financial blow if the company were forced to severely restructure its mainframe operations.

No one at Fujitsu will discuss the IBM problem in detail, but Yamamoto often has accused IBM of "closing its windows to other firms on the issue of interface and other subjects." Yamamoto refuses to comment on the legal challenge from IBM but declares that reports that Fujitsu is moving away from IBM compatibility "are exaggerated. Of course, it's also true that users of Unix are increasing," he adds hopefully. IBM declined to comment about its claims against Fujitsu.

CUSTOMER CONFIDENCE. Fujitsu markets a mainframe based on AT&T Bell Laboratories' Unix operating system and is heavily involved in Japan's national project aimed at developing a Unix-based software-production system. But Yamamoto's statement only seemed to underline Fujitsu's fundamental problem of losing customer confidence, and chairman Daiyu Kobayashi admitted as much when he recently told *Toyo Keizai*, a Japanese economics magazine, that "appearances are vital in the computer business. If a company is not able to present an image that it can supply hardware and software on a long-term basis, clients will not make purchases."

There's another basic problem, even for a corporate giant such as Fujitsu: cold, hard cash. An executive at a rival company, who asked not to be identified, estimates that the day-to-day costs of rewriting the estimated 12 operating-system packages affected by the current IBM legal action, plus an additional 400 applications packages, are running Fujitsu about $50 million annually. And it will take another 10 to 15 years to finish this work, he estimates.

Add to that the millions of dollars Fujitsu is paying in legal fees, and it is clear that the company's IBM-related costs are a serious drag on its finances. "There is an estimate that if Fujitsu loses [its legal battle with IBM], the penalties might add up to more than $200 million," says analyst Peter Rawle of brokerage firm W. I. Carr Sons & Co. (Overseas) Ltd.'s Tokyo office. "That would wipe out the entire company prof-

its last year," or some $197 million.

Fujitsu has generated close to $960 million in seven fund-raising stock issues over the last 16 months, ostensibly to cover its investments in semiconductor operations. However, some see it as a hedge against this uncomfortable prospect. It is an unusually high number of stock issues, notes Charles R. Elliott, vice president of Goldman Sachs International Corp.'s Investment Research Department in Tokyo.

All together, Fujitsu's sales of $4.76 billion in a variety of computer and data-processing equipment—of which an estimated $1.45 billion came from mainframes—accounted for 66% of the $7.22 billion total sales in fiscal 1985 ended March 31. Its communications systems and semiconductor divisions each had sales of close to $1.02 billion the same year. By 1988, according to one forecast, both communications and semiconductors will double their 1985 sales, and computer revenues will top $7 billion. In fiscal 1986, the company should post total sales of about $9 billion, about $5.87 billion of it in computers and data-processing equipment.

The growth of Fujitsu's computer business has significantly changed a company that began life in 1935 as a communications-equipment offshoot of Fuji Electric Co. Fujitsu (a combination of 'Fuji' and the first ideograph of 'tsushin,' the Japanese word for communications) didn't produce its first computer until 1954, when it was still called Fuji Communication Equipment Manufacturing Co. And it wasn't until the early 1970s, when the Ministry of International Trade and Industry (MITI) created three groups of cooperative private research projects, that Fujitsu—working with Hitachi Ltd.—came up with the IBM-compatible models that led to spectacular growth—and legal problems.

By 1979, Fujitsu had taken the top market position from IBM in total computer sales in Japan and gained a dominant position in all but the low-end market for personal computers. In 1982, IBM took legal action against Hitachi, Fujitsu, and Mitsubishi Electric Corp. for software copyright infringements. A settlement followed in 1983 in which all three Japanese makers agreed to pay IBM an estimated $100 million in total compensation—of which Fujitsu's share was about $33 million—and agreed to let IBM periodically inspect their operating-system software.

BEST BEHAVIOR. Hitachi and Mitsubishi have avoided further legal tangles. One reason Fujitsu has run afoul of IBM again, says market analyst David Keller of James Capel & Co.'s Tokyo office, is that it maintains that its operating system is independent. "That's the most dangerous aspect of Fujitsu thinking," says Keller, "and it has led them into trouble."

The trouble began last October, when IBM took further action against Fujitsu, charging that it continued to infringe IBM software copyrights. Both sides are preparing legal cases that will go before the American Arbitration Association in New York. Neither side will comment on the likely outcome, but a possible Fujitsu strategy is counterattacking IBM with a restraint-of-trade charge, hoping to force a settlement with which both companies could live.

'US VS. THEM.' "No one at Fujitsu is worried about the company's survival," said a source close to the company, "but the atmosphere is almost like an armed camp. It's 'us versus them.' "

That's why, despite its impressive sales and profits, Fujitsu is seen as a company with two futures. The near-term, say industry analysts, is bright and full of promise. But the longer term is full of doubts and difficulties, nearly all related in one way or another to the dark shadow of IBM.

Beyond the growth forecasts for Fujitsu—president Yamamoto sees 20% growth this year in total sales and double-digit growth in all major divisions—one topic dominates Fujitsu's strategic thinking: how to deal with IBM.

YAMAMOTO: Despite the IBM problem, Fujitsu's president sees total sales growing 20% this year.

The most immediate challenge is dealing with the strong legal pressure IBM is exerting. The second challenge, which is even more complex, involves balancing the conflicting needs of developing Fujitsu's own, truly independent operating-system architecture while holding on to its IBM-compatible hardware and software business.

"Fujitsu has no choice," says Rawle of W. I. Carr. "It must continue to offer IBM-compatible models while somehow finding a way, probably through some sort of settlement with IBM, to get the software issue off its back."

As Fujitsu seeks ways to get out from under IBM, it is considering new alliances (see "Is an AT&T alliance the answer?" p. 42). But no matter which course Fujitsu takes, "it will take years to work out, and the outcome is very uncertain," says analyst Yuji Ogino, editor of EDP Japan Report, an industry newsletter. Fujitsu also can't count on any help from MITI. Tsutomu Makino, director of MITI's Electronics Policy Division, flatly denies rumors of his organization's involvement in negotiations between the two companies. "This dispute is over an interpretation of the agreement two years ago. It's strict-

FUJITSU LEADS IN COMPUTER SALES IN JAPAN

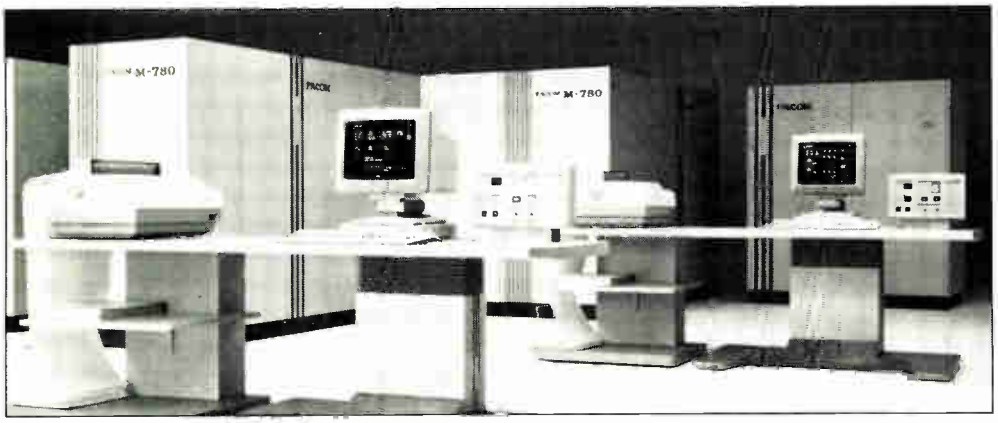
Company	(Billions of dollars)					
	1981	1982	1983	1984	1985	1986
Fujitsu	1.48	1.72	2.03	2.41	3.09	3.99
IBM Japan	1.06	1.32	1.62	1.79	2.21	2.80
Hitachi	0.89	1.02	1.19	1.42	1.74	1.92
NEC	0.85	1.19	1.61	1.70	2.13	2.76

¥ 235 = $1 SOURCE: NIKKEI SANGYO

COMPUTERS ARE THE BIGGEST PART OF FUJITSU'S SALES

Division	(Billions of dollars)				
	1983	1984	1985	1986*	1987*
Computers (data processing)	3.09	3.99	4.76	5.87	7.05
Semiconductors and components	0.926	1.39	1.02	1.36	2.13
Communications systems	0.791	0.897	1.02	1.38	1.97
Car audio and electronics	0.230	0.247	0.264	0.276	0.298
Other	0.105	0.119	0.128	0.136	0.149
Total sales	5.142	6.643	7.192	9.022	11.597

*Estimate Fiscal year ends in March. ¥ 235 = $1
SOURCE: GOLDMAN SACHS INTERNATIONAL CORP. (TOKYO)



LUCRATIVE. Mainframes such as the M-series provide most of Fujitsu's computer revenue.

ly between the companies."

Commenting on Ogino's timetable, Fujitsu's Yamamoto counters, "I can't say how long it will take to rewrite software. We feel that our operating system is our own, not IBM's. Whether or not we must rewrite any software is what this legal action is all about."

The conflict with IBM is not restricted to Japan. Siemens AG, Fujitsu's major customer in Europe, decided two months ago to stop marketing Fujitsu's IBM-compatible OSIV/F4 systems software, even though it accounted for 10% of the Munich company's $1.36 billion in data-processing sales last year.

At the time, both companies said the decision was based on Fujitsu's intention to move away from IBM compatibility, but industry sources in Tokyo think otherwise. They say the real reason was a series of surprise visits made by IBM officials last year to Siemens's customers in Europe, giving buyers the impression that Fujitsu systems software might be infringing IBM's copyrights. After conferring with Fujitsu officials late last year, Siemens apparently decided to stop selling Fujitsu software rather than risk involvement in an international legal suit, sources say.

Insiders cite two reasons why IBM came down so hard on Fujitsu. First, unlike Hitachi, which sells very few computers outside Japan running its own software, Fujitsu was running up millions in overseas sales of its own IBM lookalike software.

COOPERATION. Second, Hitachi and Mitsubishi Electric reportedly cooperated with IBM, allowing the computer giant to examine their software and agreeing to make certain changes. But Fujitsu, although it paid compensation, has not allowed IBM a free hand in looking at its operating system software, continuing to maintain that its operating system is truly independent. IBM, faced with a strengthening Fujitsu position in its overseas software sales as well as in the home market, finally decided to counterattack, and counterattack hard.

Last fall, Fujitsu reportedly sent letters to all its sales agents to ease fears among customers about the IBM legal threat. But even then, it was a mixed message: the company assured that it would continue to produce IBM-compatible equipment but emphasized efforts to develop "original" Fujitsu products to meet customer needs.

The IBM situation is casting the only cloud on what would otherwise be a promising future for Fujitsu. Elliott of Goldman Sachs and other analysts offer convincing evidence that, on balance, Fujitsu is exceptionally well positioned to cash in on strong projected growth in markets that are served by the computer, semiconductor, and communications divisions.

"Nobody's doing any better than Fujitsu in supercomputers," says W. I. Carr's Rawle. "They've got 25 on order and a wide base of customers at rental prices averaging $10,000 a month."

The one threat here is IBM's answer to Fujitsu's VP series, which has an estimated 60% share of the Japanese market. The IBM Vector Facility machine has about two thirds the processing power of Fujitsu's best-selling VP-50 at a lower price [*Electronics*, April 7, 1986, p. 42]. Moreover, the new IBM model includes software changes that make the Fujitsu models incompatible with it.

At the low end, Fujitsu's Computer Division recently introduced an Intel 80286-based 16-bit personal computer with 1-megabyte memory and three operating systems, including Fujitsu's own Japanese-language system and versions of MS-DOS and Unix. Fujitsu has a strong position in the low- and medium-priced Japanese markets partly because IBM is chasing sales in the higher end of the spectrum.

In installed computers of all sizes, Fujitsu had 1,543 models in place in 3,100 companies surveyed by *Nikkei Computer* magazine last fall; IBM's total was 543. On a value basis, Fujitsu's sales at the companies surveyed were close to $1.23 billion; IBM's were $986 million.

Fujitsu's Semiconductor and Electronic Components Division seems headed for a major turnaround this year. In the boom market of 1984, chip sales accounted for nearly 21% of company sales and 40% of pretax profits. But last year, when company profits fell 67%, the big loser

IS AN AT&T ALLIANCE THE ANSWER?

Looking for a way out of its IBM problem, Fujitsu Ltd. has entered into a number of strategic alliances, but none is more alluring than the possibility of a relationship between the Japanese computer leader and AT&T Co.

The two companies, say Japanese computer industry sources, have not held formal talks but have exchanged ideas about possible relationships. Fujitsu officials will not comment on the reports. AT&T International-Japan president William Moody is noncommittal: "We're interested in talking with all the major players in Japan. I wouldn't close the door to any relationship."

Both sides have good reasons for such interest. For AT&T, weak in computer hardware but trying to broaden markets for its Unix operating system, a link with a major maker like Fujitsu would have obvious merit. For Fujitsu, which already sells Unix-based computers through its Amdahl Corp. affiliate, it could lead to alternate markets if non-IBM U. S. and European makers are effective in seeking new standards.

Fujitsu and other Japanese makers, in cooperation with 12 major European companies, have formed a study group to promote standards for the open-systems interconnection reference model in an effort to force IBM to alter its exclusive Systems Network Architecture to allow freer interconnection among currently incompatible systems.

Fujitsu and AT&T also are deeply involved in the government-sponsored Sigma Project, which aims at developing a Unix-based software production standard for Japan. "The reasons why Unix was chosen are clear," says market analyst Yuji Ogino. "It's the only operating system that can compete with IBM and that is compatible with various computers with different architectures." The project, he says, "is a way for Japanese makers to get out of the IBM software bind."

–M. B.

was semiconductors.

"Fujitsu's sales exposure of nearly 40% in the memory market meant they were hammered much more than their competitors," says W. I. Carr's Rawle. A just-published survey by his company forecasts 20% growth in Japanese semiconductor sales for the current fiscal year, based on 3% to 4% growth in the U. S. economy.

The company's weakness in the depressed semiconductor market will turn into a strength with a general recovery, says Rawle, because of its strength in mass-production memory technology, plus its growing CMOS gate-array business, which earned close to 30% of the division's $1.02 billion in sales last year, mostly for industrial applications such as telecommunications products.

The expected semiconductor recovery, slow though it may be, will restore that Fujitsu division as a major profit-maker, one with a reputation for exceptionally high quality and productivity. And the company's relatively low ratio of overall export products—only about 21% of its chips go overseas—means it will be less exposed than its competitors to the profit-squeezing effects of yen appreciation.

The turnaround is linked, of course, to strengthened sales in the U. S. computer market. But even if recovery doesn't pick up until late this year or early next, as Rawle suspects, other basic strengths are driving Fujitsu growth.

"Japan's computer and chip markets have held up better than America's because Japanese capital spending has been higher as a percentage of gross national product than it is in the States," says analyst Elliott of Goldman Sachs. "Much of that money is being spent on computer systems for office and factory automation, plus installation of digital communications networks."

Fujitsu's Communications Division, which accounts for about half of Nippon Telegraph & Telephone Corp.'s upper-end market purchases, has seen a 30% increase in telecommunications sales to NTT, mostly in connection with the long-range Information Network Systems project, a Japanese version of the integrated services digital network. Fujitsu also is moving strongly into the U. S. fiber-optics market, where it has a reported 90% share of the market for 410-Mb/s equipment and recently began delivering an even more advanced 810-Mb/s system.

U. S. FAX. Fujitsu's latest U. S. ventures include its purchase of Burroughs Corp.'s imaging systems division for an estimated $20 million and the creation of a subsidiary to produce and market digital facsimile systems in the U. S. Fujitsu already has almost 10% of the U. S. fax market. The most recent move was a memorandum signed earlier this month with GTE Corp., under which Fujitsu will take a majority share in a new company that will develop digital private branch exchanges and related communications systems for North American markets. The major competition, as Fujitsu sees it, is once again IBM.

Fujitsu also is heavily involved in developing value-added networks, with its own network linking 20 cities in Japan, mostly serving Fujitsu offices. The company plans to start marketing communications services on its network to banks and distribution businesses this year. By 1987, the company predicts it will have VAN sales of close to $500 million annually, at current rates.

DATA BASES, TOO. In yet another emerging market, data-base and electronic information services, Fujitsu has joined forces with Nissho-Iwai Corp., a leading trading company in Tokyo, to form N. I. F. Corp., which will market CompuServe Information Service products in Japan. Fujitsu expects to build that business to 60,000 subscribers and more than $30 million in sales within four years.

Despite its IBM problem, Fujitsu has held on to the top spot it grabbed in 1979 as the total computer market sales leader in Japan, and now dominates most of the upper-end market sectors. Growth in peripherals also has been strong, especially in hard disks. That business showed 40% growth last year and will be less profitable this year only because the stronger yen is pinching export margins. Fujitsu is acting to alleviate that currency squeeze with the startup of its U. S. hard-disk production base near Portland, Ore., which should lead to strong profit growth for its U. S. subsidiary starting late this fiscal year.

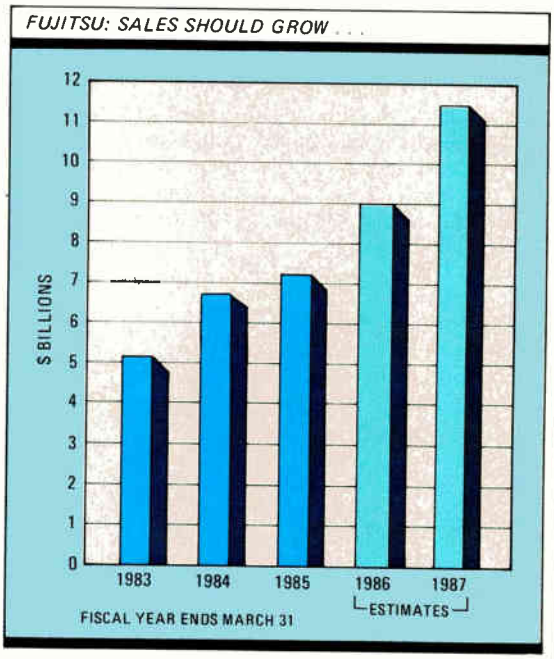
Fujitsu also owns 48% of Amdahl Corp., the Sunnyvale, Calif., company that makes its own line of IBM-compatible mainframes. Fujitsu credits Amdahl with contributing about 5% of last year's total income, says Yamamoto. To boost that contribution, Amdahl increased its marketing staff by 50% last year, hiring several IBM alumni who were offered higher commissions to switch companies.

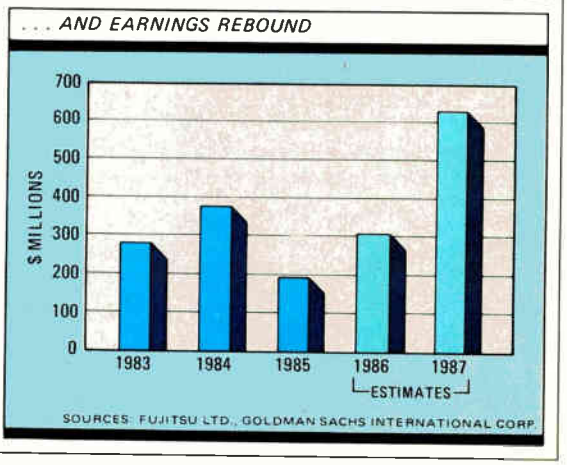
A weak point in the Fujitsu-Amdahl relationship is the European market, where Amdahl competes directly with Fujitsu-made hardware for Siemens. But this is outweighed by the benefits, including Fujitsu's healthy U. S. sales and strong links to U. S. market trends through Amdahl, as well as an extensive research and development relationship.

Some persons see the situation as a crisis with no end, and others think the worst is upon the company. "Fujitsu is facing a severe test in the near-to-mid-term," says Capel analyst Keller. "For the next 5 to 10 years, it's going to be next to impossible to build any kind of market in non-IBM compatibles."

After that, says Keller, there will be fundamental market changes spurred by the emergence of the more open Ada language. "The U. S. Department of Defense likes Ada," Keller said, "and that's going to push more makers into adopting it. That's why I think long-term that Fujitsu could be in a very strong position because of its strong telecommunications as well as computer know-how."

But no matter how well Fujitsu performs this year, or in the next several years, one fact remains: that Big Blue shadow isn't going to go away. □





WHAT WILL GE DO WITH RCA SOLID STATE?

FOR ONE THING, THE SOMERVILLE OPERATION MAY NOT SURVIVE

by Tobias Naegele

SOMERVILLE, N. J.

No one knows for sure what General Electric Co. is going to do with RCA Corp.'s Solid State Division, but there is a strong possibility that the days are numbered for the division's headquarters and design facilities in Somerville. Indications are strong that the new owners will keep the division's factories elsewhere but dismantle the Somerville operations.

The final decision has not yet been made, and there are still almost as many strategies being offered as there are strategists. In fact, since GE agreed to buy out RCA for more than $6.28 billion late last fall [*Electronics*, Jan. 6, 1986, p. 73], perhaps no aspect of the acquisition has triggered more speculation in the electronics industry than the fate of the Solid State Division, which was once an industry leader but more recently has struggled with a reputation for plodding management and poor reflexes.

Some say RCA Solid State is doomed and will be chopped apart just like a wrecked car that's worth more in pieces than as a whole. Others say the companies do not have to destroy either Solid State or GE's Semiconductor Business Division to piece together one cohesive unit. Still others, notably RCA Solid State executives, say GE would be crazy to tamper with their division just when it is starting to get on track.

But the notion that GE will close the Somerville operation, coming as it does from an observer who is close to both companies, carries a good deal of weight. "RCA has just about wrung all the juice out of its technology," he says, adding that "RCA offers GE high-quality low-cost manufacturing, and GE brings software design and process technology." That implies strongly that GE, looking on RCA's manufacturing facilities as the Solid State Division's greatest assets, will latch onto the plants in Mountain Top, Pa., and Findlay, Ohio, while gradually dismembering the Somerville parts of the division.

Under such a plan—which sources say would take at least 12 to 24 months to implement—GE's Semiconductor Business Division, based in Research Triangle Park, N. C., would swallow up RCA's custom and semicustom chip designers and move them down to North Carolina, where the bulk of GE Semiconductor's design staff is now located. In the power semiconductor area, GE would incorporate its standard power product group, which is preparing to leave its Syracuse, N. Y., home, into RCA's power unit. The new group would consolidate at the Mountain Top fabrication site, to bring design and manufacturing talent together.

G. Dan Hutcheson, executive vice president of VLSI Research Inc., a San Jose, Calif., market researcher, sees it differently. He thinks that GE will leave RCA alone. When GE bought Intersil Inc., a Sunnyvale, Calif., chip maker that now accounts for about 48% of GE Semiconductor's annual business, "they made some management changes—and they had all kinds of problems.

"I think, if anything, they're going to leave RCA alone and take a hands-off attitude. So far as I know, there are no plans to insert GE management into RCA Solid State," he says. In fact, the two operations are complementary, he maintains.

SIMILARITIES. To get a better idea of how these two companies fit together, it is helpful to look at their comparative strategic setups. Both divisions are dominated by CMOS technology: RCA, which invented the process, says it does more than 50% of its business in CMOS devices. While VLSI Research says GE does 10% of its business in CMOS technology, company executives dispute that, giving a figure approaching 65%.

The Solid State Division, which did an estimated $341 million in business in 1985, aims for the military, automotive, and industrial market sectors with heavy concentrations in power devices and application-specific integrated circuits. So does GE Semiconductor, which took in about $294 million in 1985.

The similarities do not stop there:

- Both eschew the cutthroat commodity-chip market, preferring to woo more stable niche markets such as ASIC products.
- Both say they derive about 12% of their business from ASIC work, and both see that mar-

WHAT THEY DO AND WHERE

	RCA Solid State Division	GE Semiconductor Business Division
Headquarters	Somerville, N.J.	Research Triangle Park, N.C.
Vice president and general manager	Carl Turner	James Dykes
Annual revenue ($ million)[1]		
n-MOS	14	100
CMOS	127	26
Linear	92	41
Bipolar	7	15
Discrete/power	101	112
Total	341	294
Number of employees		
domestic	3,274	N/A
total worldwide	4,700	4,500
Wafer-fabrication plants		
domestic	West Palm Beach, Fla.[2]	Research Triangle Park
	Mountain Top, Pa.	Sunnyvale, Calif.[3]
	Findlay, Ohio	
	Camus, Wash.[4]	
offshore	Kuala Lumpur, Malaysia	Dundalk, Ireland
		Singapore

[1] Based on 1985; furnished by VLSI Research Inc., San Jose, Calif.

[2] Will cease production in July

[3] Manufacturing facility of Intersil Inc., a wholly owned subsidiary

[4] Part of a 50–50 joint venture with Sharp Corp. of Japan called RCA/Sharp Microelectronics Inc. Under construction, it is expected to produce wafers by early 1987.

SOURCE: *ELECTRONICS*

ket growing at a 24% to 30% annual rate.

- Both have singled out the smart-power market niche as a lucrative future business.
- Both recognize the military market's importance in stabilizing business, an important factor in the topsy-turvy chip business.

But most important, each has strengths that complement the strengths of the other: GE has new technology, RCA has quality manufacturing; GE has the money to be a market force, RCA has the broad product line a sizable entry would need. Indeed, the groups may be more compatible than was originally believed.

Military ICs, for example, account for 23% of RCA's business, says Carl Turner, vice president and general manager of RCA's Solid State Division, and 10% to 15% of GE's semiconductor operations are devoted to military ICs, according to Steve Pletcher, general manager of the Sales Department at GE's Semiconductor Business Division and formerly vice president of marketing at RCA Solid State.

GE pushed into the military high-reliability market earlier this year, says Pletcher, who expects the division to gain joint Army-Navy and Defense Electronic Supply Center certification this year. GE is now taking initial orders for semicustom ICs listed on the military Qualified Parts List.

That's where RCA's Findlay manufacturing facility fits in. Turner says Findlay's yields are among the best in the country. The site has a brand-new clean room outfitted with automated line steppers for high-volume 1.5- and 2-μm work, he says, adding that "in the last couple of years, it has developed a very good low-cost reputation." But what really excites GE Semiconductor management is Findlay's Class-S certified fabrication line for high-quality high-reliability IC manufacturing. Findlay also boasts a second line for custom chip fabrication and assembly for military parts that must be produced entirely within the U. S.

Yet another new manufacturing site for the new combination will be the $400 million RCA/Sharp Microelectronics design center and fabrication facility in Camus, Wash., a joint venture of RCA and Sharp Corp. of Japan. Construction on the production facility was delayed this winter so GE could study the need for yet another fab line—GE says the Research Triangle Park unit is operating at only 50% of capacity. But after a close look, sources say, GE has decided to continue with the project, though perhaps on a smaller scale.

GE's long-term strategy, according to Pletcher, is rooted in increasing the application-based portion of its business from a minority share of 12% to a majority portion of 60% or better. What's more, Pletcher says, he wants to do that by 1990. ASICs will make up a healthy share of the application-based business, but Pletcher also includes GE's new GE-Smart line of intelligent power devices that implement both logic and power on the same chip. "We envision a whole family of intelligent power devices, most of which will be application-based," he says.

RCA Solid State is making an all-out effort to show GE its mettle

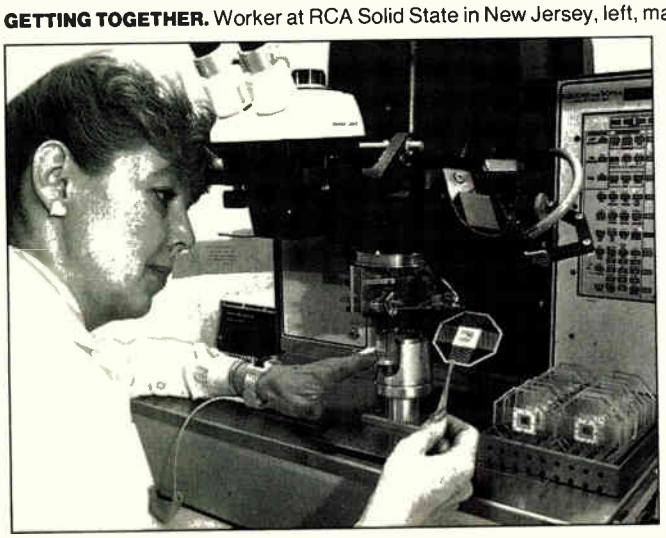
BIG ASIC PUSH. "We're putting the majority of our emphasis and spending the majority of our research and development dollars as well as our capital dollars on ASIC and application-based power products," he says. "We see that market growing on a 23% to 24% annual basis, and we feel the general-purpose semiconductor market is only growing at about 13% a year." Pletcher concludes that GE will be the standard-cell market leader by 1990—"at least that's what the great master plan says."

In March, GE took steps toward realizing that goal when it signed a joint marketing and development deal with Laserpath Corp., Sunnyvale, Calif., to manufacture and sell Laserpath's laser-programmable gate arrays. The devices should enable GE to perform quick-turnaround prototyping and shorten fabrication cycles by about 80% from as much as two to four weeks to as little as 24 to 48 hours. In addition, GE boasts a 1.25-μm CMOS technology it says is outpacing commercialization of the technology emerging from the Pentagon's Very High Speed Integrated Circuits program and will go into full-scale manufacturing early next year.

Meanwhile, RCA is cranking out new products and product enhancements at a rate of almost 40 a month as the division polishes its image to make a good showing for the new ownership [*Electronics*, April 28, 1986, p. 21]. Like the surgeon who goes to heroic measures to save a stricken patient, RCA's Turner is pressing the division to give its all, even as the takeover looms on the horizon. "We are keeping on with our present plan," Turner says, adding that he is operating independently of GE. Another insider says candidly, however, that "GE's here every day—they could probably implement a consolidation plan by July if Justice Department approval comes soon."

That approval came last week from the Justice Department's antitrust division. However, the merger still must be approved by the Federal Communications Commission because RCA owns the National Broadcasting Co. Still, RCA Solid State's time in limbo is nearing an end. □

GETTING TOGETHER. Worker at RCA Solid State in New Jersey, left, may have to find a new job or move to GE's plant in North Carolina, right.



FINALLY, A SCSI STANDARD; BUT THERE ARE STILL LOOSE ENDS

STILL NEEDED: COMMON COMMANDS, MULTITASKING, IBM ACCEPTANCE

by Denise Caruso

SUNNYVALE, CALIF.

When the Small Computer Systems Interface receives final approval from the American National Standards Institute in the next few weeks, the industry will get what it has been thirsting for: a standard to ease the product-development pains of peripherals and systems manufacturers. Until SCSI, they had to design an interface for each peripheral and each computer on the market. But for the standard to win complete acceptance, three loose ends must be tied up.

The first and most crucial is in forging a group of common commands, which are the vertebrae of SCSI. The goal is a set of common commands that are acceptable to manufacturers of the various peripherals and to incorporate it into the first SCSI upgrade, expected next year. Additional stumbling blocks are the need for a multitasking personal computer operating system and the stance of IBM Corp., which so far has been noncommittal about SCSI and could eventually move into the market with its own standard.

SCSI has made tremendous inroads since it was proposed in 1979 by Larry Boucher, then at Shugart Associates, Sunnyvale. "I thought [acceptance] would take much less time than this," says Boucher, who is now chairman of SCSI controller-maker Adaptec Inc., Milpitas, Calif., which he cofounded. "But now it's really on a roll."

Indeed, the recent SCSI Technology Forum in Sunnyvale attracted more than 100 representatives from top companies in peripherals and SCSI controllers, computers, and integrated circuits. Enthusiasts ranged from Apple Computer Inc., which put an SCSI plug in its latest Macintosh computer, to NCR Corp., which designs programmable SCSI chip sets and uses SCSI in its systems. AT&T Information Systems, Digital Equipment, Sun Microsystems, and Wang Laboratories are also SCSI supporters.

Already, some 80 SCSI products are on sale

Some 80 SCSI products are on the market, and about 40 more are ready for shipment. Dataquest Inc., the San Jose, Calif., market researcher, estimates that more than 1 million SCSI devices are in use.

By 1990, projects Don Collier, the president of Applied Magnetics Corp., SCSI will be the interface of choice for 29.5% of all original-equipment-manufacturer systems costing more than $1,000 and having drive capacities of less than 30 megabytes to more than 300 megabytes. Collier, who presented the results of a market survey at the forum, says the $200 million SCSI worldwide disk-drive market will skyrocket to nearly $3 billion by 1990.

Helping make that possible will be the most vital component of SCSI's evolution, the common command set (CCS), an extensive subset of the SCSI command set. CCS Version 4A, which is expected to be included in SCSI II, the upgrade that should be completed and approved by early 1987, sets forth an extended mandatory set of SCSI commands for the operation of hard-disk drives. It also restricts the ways in which those commands can be implemented.

The goal of the CCS push, which began last year, was to limit the number of unique commands each vendor could implement, so controllers and drives could be designed faster and more easily. It got its start when Daniel Loski, marketing manager for the Omti Products Division of Scientific Micro Systems Inc., Mountain View, Calif., asked his largest customers in July 1985 to simplify their design specifications. Eventually, a group of manufacturers came together to form an ANSI Approved Standards Committee, which formulated the CCS draft standard.

All SCSI standard-bearers agree CCS is a boon. But some believe it shouldn't be incorporated into products until all the kinks are worked out. For now, they say, the present SCSI protocol is sufficient. They point out that in various revisions of CCS, the content of some commands was changed—the meaning of a bit or a byte, for example—or a location was used that had been reserved for further standardization. The result is that some already existing SCSI devices fail to conform to portions of CCS. That means many peripheral manufacturers with designs already in compliance must make revisions to be current when the products hit market.

STANDARD BEARERS. Working on SCSI standards are, from left, Fred Berkowitz, Sun; Steve Brightman, TI; Bryan Fifield, Emulex; and Daniel Loski, Scientific Micro Systems.

Another camp argues that CCS is ready to go. "In eight months, many companies had significant input to CCS," says Richard Barrett, president of the Adven Group, Arcadia, Calif., which publishes technical reports and develops software for SCSI-related projects. "And it accomplished the purpose—it provided a set of specifications so suppliers could build something right away."

SUPPORTING NUMBERS. He points to the numbers to support his contention. Without SCSI, designing the host-to-disk connection takes about 1,000 man hours, says Barrett. With SCSI, it takes about 100, or two weeks. And with CCS, he says, it takes a mere 10 hours.

A third camp at the Sunnyvale forum holds that even an imperfect CCS is too valuable to leave in limbo. "We know well enough what we want to do [with SCSI] to make CCS a stake in the road," says Hank Meyer, national sales manager for Hitachi Corp.'s Nissei Sangyo America Ltd. in New York. "If you're hurt by it, so be it—that's the cost of doing business." He adds that people are already designing to CCS and that refinements will continue. "No specification or design is frozen in time. But at some point you have to semifreeze it and go for it."

At least one personal computer manufacturer agrees. William Watson, principal engineer for Apple, says CCS is "a win-win situation for us. It's going to be a while before standards solidify. We want compatibility with the SCSI world that exists now, and we'll be ready for the SCSI II world that's emerging." So despite industry grumblings, CCS 4A will be integrated into SCSI II.

In the meantime, optical-disk-drive and tape-drive manufacturers are hoping to beat nonstandard products to the market. They have started meeting with Loski to develop SCSI command sets specific to their fledgling products.

Tape-drive protocols are expected to be much the same as hard-disk protocols, with exceptions made for the fact that tape drives are seldom used for boot drives in the same way hard disks are. But optical-drive protocols are expected to be somewhat more rigorous, since the medium requires very different handling from magnetic drives. For one thing, defective areas on the disk must be mapped out permanently.

Another critical issue is file format, says William Casey, president of Advanced Storage Concepts Inc., a Houston maker of disk controllers. Special care must be taken to decide on this standard immediately, he says, since compact-disk ROMs "may become the largest SCSI device resident on personal computers in the U.S."

As SCSI is refined for different peripherals through extended common command sets, the need for a multitasking personal computer operating system becomes more vital. SCSI came into existence partly to create a high-performance bus that allows the arbitrated use of a number of intelligent peripherals connected to a single central processing unit.

But tasks can't be arbitrated when that single CPU can do only one thing at a time. So right now, SCSI can't help but create a massive input/output bottleneck in personal computers. "You don't gain much, except cost, by adding one SCSI peripheral to one [personal computer] with a SCSI port," says G. Venkatesh, manager of strategic planning for Adaptec Inc., Milpitas, Calif. A true SCSI implementation with multitasking software could simultaneously use up to seven different peripherals by means of task arbitration and SCSI's disconnect/reconnect commands.

PROGRESS. John J. Hoy, left, of Optotech and Daniel Loski, chairman of CCS working group, discuss SCSI standards for optical disks.

Digital Research Inc., the inventor of CP/M, was the first to attempt a multitasking operating system with its Concurrent PC-DOS. Despite the appearance of multitasking, however, the Pacific Grove, Calif., company's program is single-threaded with a complex switchback mechanism that allows it to process different applications simultaneously.

The last big question: will IBM snub SCSI for its own standard?

Phil Devin, senior industry analyst for Dataquest, says that Microsoft Corp.'s Xenix operating system, a version of AT&T's Unix for IBM PCs, could provide multitasking for SCSI, though he hasn't yet heard of such an implementation. However, there are rumors in the industry that Microsoft's MS-DOS Version 5.0, expected from the Redmond, Wash., company in early 1987 or before, will support true multitasking because IBM has used the SCSI interface on the CD-ROM drive expected later this year. (The company has an ongoing agreement with IBM to codevelop operating systems for its personal computers.)

A multitasking operating system is especially important with slow optical peripherals such as CD ROMs and page scanners, notorious for crippling single-threaded bus connections. This will become even more apparent as new SCSI devices such as local area networks, printer servers, and instrumentation controllers are implemented.

IBM'S SHADOW. The final hurdle for SCSI is endorsement by IBM, which has held back from the standardization talks. "What's the biggest issue in the SCSI world? IBM," says Barrett of Adven. "As far as SCSI goes, it's well established. Some big computer companies are supporting SCSI, like Apple and NCR. But if IBM came out with IBM-SCI—well, they have up to 60% of the market. Vendors would have to develop IBM-SCI."

IBM's blind spot about SCSI is seen by Hank Meyer of Hitachi as an obstacle in SCSI's evolution. He notes that in 1982, instead of choosing the more highly evolved SCSI, IBM chose SASI, the original Shugart Associates Systems Interface, for the PC/XT. In 1985, it chose a proprietary bus for its PC AT.

But despite the obvious snub, Barrett says, "The longer IBM waits, the stronger SCSI gets." The one thing IBM can do that SCSI can't is create generic awareness of a standard. "I don't think SCSI will ever achieve name recognition on that level without IBM's support," says Barrett. "It has one shot—Apple's SCSI plug on the back of the Macintosh Plus. Apple's trying to give it end-user awareness, and all the SCSI controller companies in the world couldn't do that."

But with companies such as Apple, AT&T, DEC, and NCR supporting SCSI, all eyes are now on IBM. "All the noise about SCSI is very important," Barrett says. He figures there will be four to five years of "ferocious development" before SCSI reaches the magic $1 billion line and is noticed by IBM. That was the point at which Big Blue decided that maybe personal computers weren't such a bad business idea.

"It's like an impending earthquake," says Barrett. "If you live near a fault, you tend to forget about it. But if IBM announces [a new peripherals interface], there will be such a shuffle you won't believe it." □

SYMBOLICS: FIGHTING OFF THE AI INVADERS

USE OF COMPANY'S PRODUCTS SHIFTS FROM DEVELOPMENT WORK IN ARTIFICIAL INTELLIGENCE TO APPLICATIONS

CONCORD, MASS.

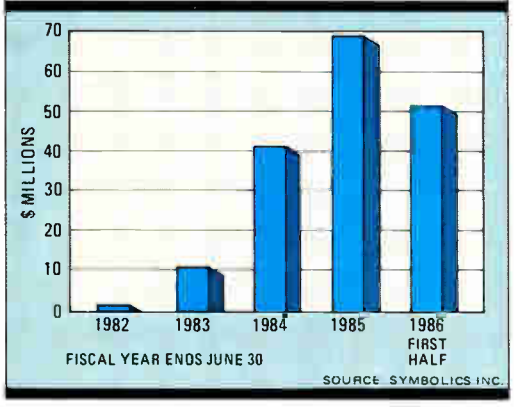
After five years of peace and prosperity, Symbolics Inc. finds itself at war. The enemies: other Lisp processor companies and vendors of standard computing systems architectures that are making a move into artificial-intelligence applications.

Almost imperceptibly, yet decisively, the symbolic-processing market is shifting from development work in AI to applications, and a host of general-purpose computer companies and other vendors of symbolic-processing gear are scrambling for a piece of the action. This shifting market demands major-league marketing, which has been a weak area for Symbolics to this point.

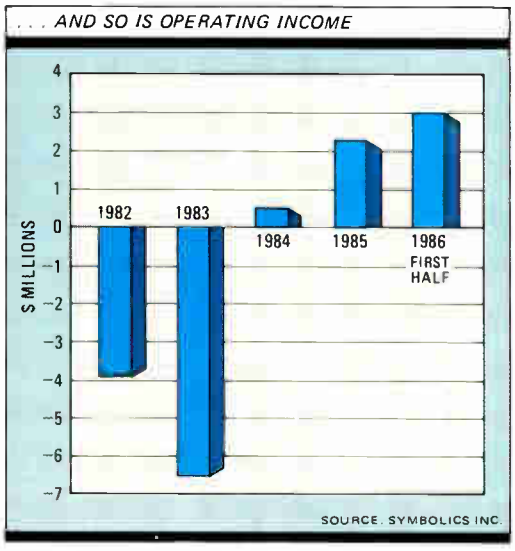
Since it was founded as a builder of Lisp processing systems, the Concord company has grown to a point where it is now generating revenue at a rate in excess of $100 million per year—and is profitable—and has staked out a position as the vendor with the best product for symbolic processing. Much of this rapid growth has been fueled by customers seeking out the company's high-powered tagged-architecture computers for use in AI development work. (In tagged-architecture computers, each piece of data carries a "tag" that identifies what the data contains and enables more efficient processing.) Symbolics' hardware architecture pioneered this market, and by consensus it remains the best available for serious development work.

NOFTSKER: Symbolics' head isn't worried by competition.

FOR SYMBOLICS, REVENUE IS UP . . .



. . . AND SO IS OPERATING INCOME



Now the company, which has an installed base of over 2,000 machines, finds itself threatened at the lower end of the market, primarily by Texas Instruments Inc., which already markets a Lisp processor, the Explorer. By year end, TI will also develop an Explorer Lisp chip.

Symbolics has responded with a recently unveiled application engine, the 3610 AE [*Electronics*, April 21, 1986, p. 55]. Refusing to concede the competitive advantages of a Lisp chip, the company has embarked on a project with Merrill Lynch Technology Ventures Ltd. to develop its own system based on a very large-scale-integration chip implementation of its architecture and operating system. Merrill Lynch, through a research and development partnership, will contribute $7 million toward the estimated $16 million project.

Despite claims by TI that its chip's performance will nearly match that of Symbolics' higher-end machines, there is little outward concern at Symbolics. For one thing, Symbolics president Russell Noftsker says his company will continue to push its gate-array technology for higher performance. So if and when TI reaches its target levels, he says, Symbolics should be farther up the performance curve.

Yet Symbolics recognizes the problem it faces in the product marketplace. "The hard part to judge is whether the market will ramp up at the low end or the high end," Noftsker says. At the less complex end of applications, he concedes, Symbolics will be hard-pressed to compete with general-purpose work stations from the likes of Apollo, Digital Equipment, and Sun, which will likely continue to offer improved Lisp processing ability.

Those vendors will not challenge Symbolics for the applications at the extremely complex end of the spectrum, Noftsker says, but others might. Possible competitors include technology giants such as Hewlett-Packard Co. and Xerox Corp., which markets a low-end line of symbolic processors, says John Kulp, vice president of R&D.

The stiffest competition is likely to come in gray areas, where applications could run either on specialized hardware or, with minor performance concessions, on general-purpose computers. Here, Noftsker says, Symbolics has not ruled out offering a dual processor—both numeric and symbolic computing—to compete with work stations that may incorporate Lisp chips.

HIGH MARKS. Industry observers generally give the highest marks to Symbolics' technology. "There are maybe six important operating systems in the world, and Symbolics has one of them," says Curt Monash, vice president at Paine Webber Inc., New York. He thinks Symbolics has "a sustainable technological lead" over the competition for a couple of reasons. Notably, he says, it has the best technical staff in the world by a significant margin. And he adds that advances in operating systems are hard to come by. But Monash criticizes the company for a lack of marketing. "There has been weakness in getting the message out."

The success that Symbolics has had may be making it hard for the company to move forward, says Harvey Newquist, who tracks the market for DM Data Inc., Scottsdale, Ariz. "Everybody who really needed a machine has one. Now people will have to be convinced."

To shore up its marketing, Symbolics named Bruce Rusch as vice president of marketing and sales late last year. Rusch, who in the past served as president of Gould Inc.'s programmable controller division and as president of Adept Technology Inc., characterizes Symbolics as a big startup that

has passed its order-taking stage but is only now in the process of building a strong organizational marketing structure. Along with others at Symbolics, he believes the company has yet to play one of its strongest cards: the ability of tagged-architecture products to enhance the productivity of conventional software development.

Another selling point, say Rusch and Noftsker, is that Symbolics' machines can go beyond AI work, such as expert systems, into such symbolic processing as highly automated software development for a wide range of applications. "Customers will buy one system for AI," says Noftsker, "and come back to buy 10 to 15 for software productivity."

Interestingly, Symbolics also doesn't view itself primarily as a hardware company. "We're a software company that makes hardware because there is no hardware company making hardware to run our software," says marketing director Howard Cannon.

In a similar vein, Kulp says, "The real issue is the competition of good software environments." And though Symbolics believes—and most outsiders agree—it holds a significant lead in that area, it still faces the challenge of improving the system's appeal to the soon-to-be users of AI applications.

KULP: His challenge is to appeal to future AI users.

RUSCH: Brought on board to shore up marketing efforts.

Kulp lists two priorities in that regard. First is that Symbolics' Lisp must become even easier to use. "The basis of making a machine easier to use is that you've got to have something to talk to in the machine, some data structure," he says. "We want to make it easier for applications developers to develop these interfaces." Also a technical priority, says Kulp, is to move the software environment from a virtual-memory foundation to a data-base foundation, which would make programming simpler.

COST. Besides these two actions, Symbolics recognizes that it must bring down the cost of its systems, so that it is not stereotyped as a vendor of expensive hardware. Kulp and others emphasize that prices have come down, and the company announced a series of price cuts—ranging from 4% to 25%—in April. Though a typically configured system still runs about $80,000 and Symbolics' low-end machine is tagged at just under $40,000, Kulp thinks the perception of symbolic processing as expensive will disappear in the future.

The desire to appear affordable coincides with the movement toward applications. Until now, says Noftsker, about 95% of Symbolics hardware has been used for software development. "The limiter there is not lack of products from Symbolics, it's lack of demand," he says. "There are not enough applications programs to constitute significant demand."

Overall, Noftsker believes a relatively small percentage of AI applications will demand symbolic processing—perhaps 15% to 20%. "Another 15% to 20% would clearly benefit from Symbolics' technology, although it won't be the only alternative."

Noftsker expects a significant increase in system sales for AI applications versus development work by late in the fall or early 1987. For 1986, he predicts 10% to 15% of Symbolics' sales will be for applications. That would be about 100 systems for all of 1986, which means a big ramp-up: Noftsker says only four or five will be sold by the close of the fiscal year on June 30. Over the next three years, he expects 25% to 30% of sales to come from applications.

The utility of symbolic processing has not escaped the eye of the government, which is turning into a big user of Symbolics systems. About 15% of Symbolics' sales are directly to the government, with another 35% going indirectly through defense, aerospace, and intelligence applications.

The fastest-growing sales area, according to Thomas Farb, director of corporate development, has been to other vendors of AI products, such as Intellicorp and Palladian Software Inc.

Many of the applications developed by customers on Symbolics systems are kept behind closed doors, says Farb. "Most of what we're seeing is internal deployment. Companies see their development [of applications] as a competitive advantage, and they're not likely to sell them." But they are apparently willing to pay for them. Farb says 40% of the company's recent revenues—which totaled $69 million in fiscal 1985 and is on the way to surpassing that in fiscal 1986—have come from its two higher-end systems. – *Craig D. Rose*

BOTTOM LINES

50% GROWTH SEEN FOR PUBLISHING SYSTEMS

Despite past promises by vendors of office-automation equipment that U. S. industry could one day be the realm of the paperless office, a new report shows increased momentum for computer publishing systems in commercial and corporate market segments. According to C. A. Pesko Associates Inc., Marshfield, Mass., the market for computer publishing systems will see dramatic growth from 1986 through 1990, with system placements up 71% and revenues growing 50% on a compound annual basis. Placements of computer publishing systems will grow from 32,760 in 1985 to 561,390 in 1996. This will result in market revenue of $4.03 billion in 1990, up from 1985's $503 million, it says. While low-priced desktop publishing systems and software are expected to account for 97% of all computing publishing placements in 1990, revenue from this segment will reach $929 million, or just 23% of the total for that year.

MICRONIX FUNDING YIELDS $6.4 MILLION

Micronix Corp., a manufacturer of X-ray lithography systems, masks, and imaging sources used to produce semiconductors, has raised $6.4 million in a third round of venture financing. The Los Gatos, Calif., company said the funds came from a consortium of U. S., European, and Japanese investors. The privately held company was founded in 1981.

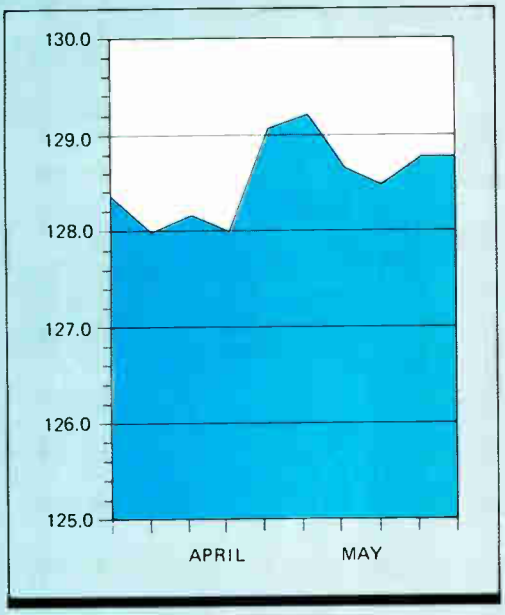
ITT-QUME PRINTER LINE GOING TO ZENTEC

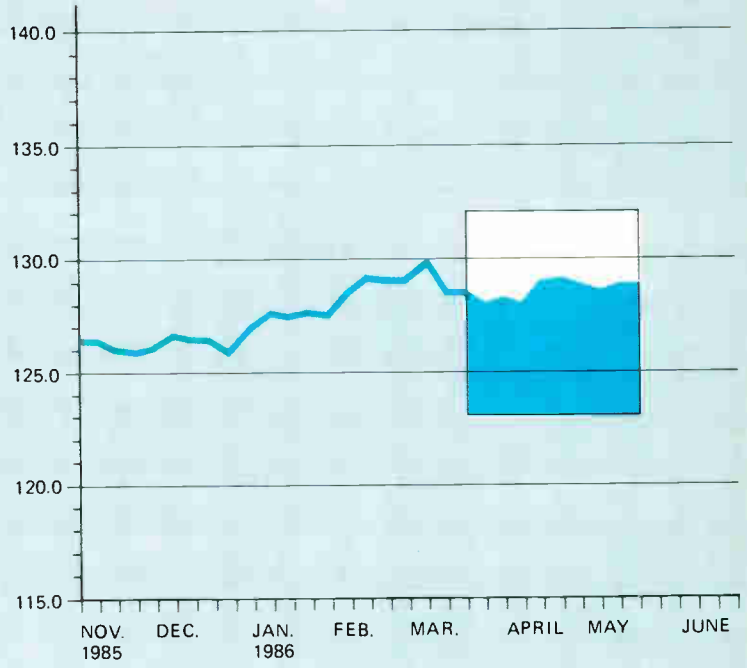
Zentec Corp., a Santa Clara, Calif., manufacturer of customized intelligent terminals, has agreed in principle to buy the color and graphics terminals operations of ITT Qume Corp., San Jose, Calif. Zentec said that under terms of the offer, it will pay an undisclosed amount—part in cash and part in shares of its common stock—for certain assets of Qume's color and graphics terminal business, together with related equipment, tooling, and inventory.

ROUND 2 NETS AXIOM $17 MILLION IN FUNDS

A second round of venture financing has netted Axiom Computers Inc. a total of $17 million. The Milpitas, Calif., company said it is developing high-performance computers aimed at bridging the performance gap between superminis and supercomputers.

ELECTRONICS INDEX





THIS WEEK	= 128.8
LAST WEEK	= 128.8
YEAR AGO	= 127.7
1982	= 100.0

The *Electronics* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

U. S. ELECTRONICS INDUSTRY EMPLOYMENT

Production workers (thousands)	March 1986	February 1986	March 1985
Office and computing machines	165.9	167.0	193.9
Communications equipment	278.7	279.4	297.0
Radio and TV receiving equipment	55.5	56.6	58.3
Components	347.6	345.3	392.9

For the first time in almost a year and a half, the declining labor situation in the U. S. electronics industry appears to be leveling off. Total industry employment slipped 0.1% in March, but this was the smallest decline in the past 17 months. The slippage was so small, in fact, that it had no impact on the *Electronics* Index, which is holding steady from the preceding week.

There was some decidedly good news in employment. Helped by rising sales, as evidenced by increasing book-to-bill ratios, U. S. component manufacturers actually increased their work force by 0.7%, the largest increase in 20 months. Despite this gain, however, employment in this sector remains down 11.5% from the March 1985 level.

The rest of the electronics industry did show declines in employment levels as manufacturers continued to pare work rolls in the face of ongoing sluggishness in demand. The most severe cutback was in employment at television and radio equipment manufacturers, which fell 1.9% in the month. In the past 12 months, employment in this sector has fallen 4.8%.

Less hard hit were worker levels at manufacturers of office and computing machines. There, payrolls dipped 0.7% in March. As a result, worker levels are off 14.4% from the same month a year ago. And even better off, relatively speaking, were production workers at communications equipment companies. Their ranks were trimmed just 0.3% in March. This brought payrolls down 6.2% from a year ago.

With the Japanese yen maintaining its strength against the dollar, it seems probable that employment levels in the U. S. electronics industry will begin to head up over the next few months as domestically produced goods eat into imports' share of the market.

Even if this does happen, however, the U. S. industry has a lot of catching up to do to overcome past worker cutbacks. From October 1984—the last month in which employment rose throughout the U. S. industry—through March 1986, total industry employment has fallen more than 13%. Employment in each industry sector has fared differently. For example, office and computing machinery makers started letting workers go much earlier than other sectors. From August 1984 through March 1986, after 20 months of layoffs, production jobs in the computer industry were down about 35%. Communications equipment makers were able to maintain strong payrolls until April 1985. But from that month through March 1986, employment slipped 7%.

TI'S AUTOMATION PUSH PUTS RAY IN THE HOT SEAT

PLANO, TEXAS

Jodie N. Ray faces a Texas-size task. The senior vice president at Texas Instruments Inc. is coordinating a major companywide effort to hone automation technologies for building a wide range of TI products, from clad metals for chrome car bumpers to 1-Mb memories to missiles. At the same time, he is in charge of the company's biggest move yet into factory-automation markets—including a milestone contract with General Motors Corp.

Ray, 40, heads TI's new Industrial Automation Intracompany Objective from this north Dallas suburb. "The intracompany objective focuses on work that is going on across all of TI and brings it together to create more synergy in the automation area," says Ray, a native of the West Texas city of Idalou. He joined TI as a military systems design engineer in 1967 after receiving a BSEE from Massachusetts Institute of Technology and working in the Air Force's Cambridge (Mass.) Research Laboratories. In 1972, he earned an MSEE from Southern Methodist University.

NEW BUSINESS. The industrial-automation effort aims at opening new business opportunities. Included in a wide range of possible products are token-passing computer nets, machine-vision systems, expert systems software and hardware, and intelligent mobile robots. No products are planned yet, but there is interest in the potential, says Ray.

A cornerstone in both the internal and the new-product efforts is a recently won factory-automation contract from GM. TI is the general contractor for the complete automation of a future GM factory in the Detroit area that will build prototypes of automotive components. "The GM prototyping factory will be automated from back-dock delivery of materials to the shipping dock of final-tested assembled materials. It will include automation of machines, the automation of material handling, assembly, test and inspection," Ray says.

RAY: Serving as TI's point man for internal automation and outside sales.

"Artificial intelligence will be a part of the GM project in terms of scheduling the beginning of a complex project up to automatic reconfiguration of robotic systems for design changes, without interrupting the flow in the factory," he notes.

START AT HOME. While TI continues to bid on selected factory-automation contracts similar to the GM project, Ray's efforts focus mainly on the company's internal needs. "Our current objective first and foremost is to strengthen the automation focus within TI," says Ray, who first became involved in automation during the 1970s at TI's weapons department in Sherman, Texas. In the early 1980s, he was promoted to manager of the TI Defense Group's Electro-Optics Division, which makes infrared night-sight military equipment. Production was greatly automated while he was manager.

Ray also heads TI's manufacturing equipment and technology center and the Industrial Systems Division in Johnson City, Tenn., which markets factory controllers and networks. The manufacturing center produces the robots and machine-vision technologies TI itself uses. It is also applying Lisp-based AI to TI manufacturing systems. Expert systems for process control have already been constructed for a number of outside customers as well.

Automation could turn into a big business for TI, Ray believes. "The loss of

PEOPLE ON THE MOVE

DAVID CAPLAN

☐ For 16 months, David Caplan served as president of Tolerant Systems Inc. as a representative of principal investor Adler and Co. Now the San Jose, Calif., startup has named him permanent chief executive officer. He has fashioned a new management team, including Victor Maxted as vice president of hardware development and Jeffrey A. Oromaner as vice president of sales. Tolerant founder Dale Shipley remains as vice president of software development.

JOHN O'BRIEN

☐ Aerospace giant Grumman Corp. has picked John O'Brien—a 30-year corporate veteran—as its next president, following the retirement of George M. Skurla. O'Brien, now president of the Data Systems Division, is not scheduled to take over the corporate post until Aug. 1. Until then, he will continue at his present position as executive vice president. O'Brien, 55, joined the Bethpage, N. Y., company in 1954. Grumman is expected to aggressively continue its marketing base to new areas, such as data systems, under O'Brien.

LEONARD JAFFE

☐ The embattled National Aeronautics and Space Administration has named Leonard Jaffe as the new chairman of its Space Applications Advisory Committee. The committee advises NASA on applications such as satellite communications, microgravity science, remote sensing, and information systems. Jaffe, currently vice president of program management and product assurance for Computer Sciences Corp., Falls Church, Va., replaces Arthur Mager, chairman of the committee since it was formed in 1983.

MICHELE GIAMMARINO

☐ Micro Power Systems Inc., Santa Clara, Calif., has named Michele Giammarino president and chief operating officer. He will be responsible for day-to-day operations, sales, and marketing for custom, standard, and telecommunications semiconductor products. Before joining Micro Power in 1982, Giammarino, 44, was vice president and division manager of the Linear Division of Texas Instruments Inc. and also served TI as an executive, manager, and design engineer after joining the company in 1971. Before that, he worked for General Instrument Corp. Giammarino earned the equivalent of an MSEE from the University of Naples, Italy, in 1966.

ROBERT C. CORRAO

☐ In an effort to improve its market share, Wavetek Corp. has consolidated its microwave instrument businesses in San Diego and Sunnyvale, Calif., and its research group in Seattle into one entity, Wavetek Microwave Inc. Robert C. Corrao has been named by the company as vice president and general manager of the unit, which will be based in San Diego. Corrao comes to the new division from Avantek Inc., where he was general manager of a business unit.

manufacturing excellence in the U. S. is a real problem. And there is no doubt that the potential exists for a big business in automation as it becomes a major investment for U. S. companies over the next decade," says Ray. "We are assessing and methodically exploring whether we can use the experience we've already accumulated within our company and offer some additional products outside—either at the system-integration level or enhanced versions of what we are already doing in our Johnson City division." *–J. Robert Lineback*

FOR MOTOROLA'S NORLING, ON TIME IS JUST FINE

PHOENIX, ARIZ.

When James A. Norling is asked to name the top priority at Motorola Inc.'s Semiconductor Products Sector, where he is responsible for most day-to-day operations, his response is eye-opening: "on-time delivery."

The reason is that customers are working on tighter timetables as the move to just-in-time deliveries accelerates, and device makers now must meet schedules precisely or lose business, says Norling, 43, who was appointed to the assistant general manager's post last September. Sometimes, deliveries must be made every day—a demand nearly unheard of in the U. S., where deliveries might lag by many weeks, particularly during booms. A customer's protection against shortfalls used to be a healthy stock of components, but this is no longer the case. "Customers can't afford fat inventories now," Norling explains.

NORLING: Keeping the customers happy with just-in-time deliveries is the chief priority.

A 21-year Motorola veteran, he has settled smoothly into the two-man general manager's office with long-time friend Gary L. Tooker, executive vice president and general manager. Duties are divided at the $2 billion operation: Norling has the "Mr. Inside" role, which calls for an executive with a strong technology background. He holds BSEE and MSEE degrees from the University of Illinois. Tooker, generally "Mr. Outside," deals with industry groups and corporate and government officials.

But the arrangement is not carved in stone: the two also pursue interests that might technically fall in the other's bailiwick. Tooker, for example, still largely oversees the $400 million Discrete Components Group, and Norling is getting involved in local Arizona public issues.

Such an arrangement may sound fraught with hazards but, Norling says, "We find it easy to agree."

Revamping internal standards to consistently "hit a 0-to-7-day delivery window can be tough to do," as Motorola found out during a four-month phase-in period last year. "It was shocking to the system," quips Norling, who notes that most of the wrinkles have been ironed out since then. He assumes that competitors are going through a similar wrenching transition, but he is not certain; industry-wide, the subject somehow has not grabbed much attention, considering its importance.

One factor that makes life easier for Norling is that Motorola's product lines are in good shape, especially given its 1985 triumph of being the first volume producer of a 32-bit microprocessor—the MC68020—and necessary support circuits in volume. The firm therefore is focusing most strongly on production-line technology "to bridge the gap between the laboratory and advanced manufacturing areas."

Norling believes that Motorola's newest fabrication facility, in Austin, Texas, breaks some new ground on this score "by pairing research and development people literally with manufacturing counterparts in the same physical area." The objective is for key device-design decisions that affect manufacturing to be made jointly in advance rather than further down the line, as it had been done in the past.

In semiconductor manufacturing technology, the leading edge has moved below 1-μm geometries—especially in the popular CMOS process. But Norling says that big random-access memories are the prime tuning vehicle and that Motorola is still developing advanced versions. He will not comment on plans to re-enter this business, but, he notes, "It would be wrong to assume we've washed our hands of any important subject." *–Larry Waller*

NEW PRODUCTS

VMEBUS DEVELOPMENT SYSTEM GOES AFTER REAL-TIME USERS

FORCE's STATIC-RAM CACHE MEMORY ELIMINATES WAIT STATES

If designers are to make best use of the VMEbus, they need a fast and powerful development system. Force Computers is providing just that with its miniForce 2P21.

Force bills its new product as the first real-time 32-bit multiuser hardware- and software-development system. It contains a 68881 floating-point processor as well as a 68020. And it is supplied with Eyring Research's PDOS multiuser, multitasking operating system, which is becoming a favorite for real-time work on VMEbus.

The PDOS kernel, floating-point module, file manager, debugger, and BIOS fit into 16-K bytes of ROM, making the system practical for the kind of diskless environment needed by real-time users. A non-real-time Unix version will be along in six to nine months, the company says. Force sees applications in signal and image processing, robotics, simulation, artificial intelligence, and process analysis.

Rather than bypass slow main memory by using a cache-memory scheme, Force has equipped its development system with fast—55-ns access time—static RAM. In effect, says marketing director Wayne Fischer, "the whole memory—half a megabyte, expandable to a full megabyte—is cache."

NO WAIT STATES. The result, Fischer adds, is that the system can operate its 68020 central processor without wait states. "We can actually run the 68020 at 20 MHz," Fischer says. "No one else can do that." System performance is rated at 3.5 million instructions/s.

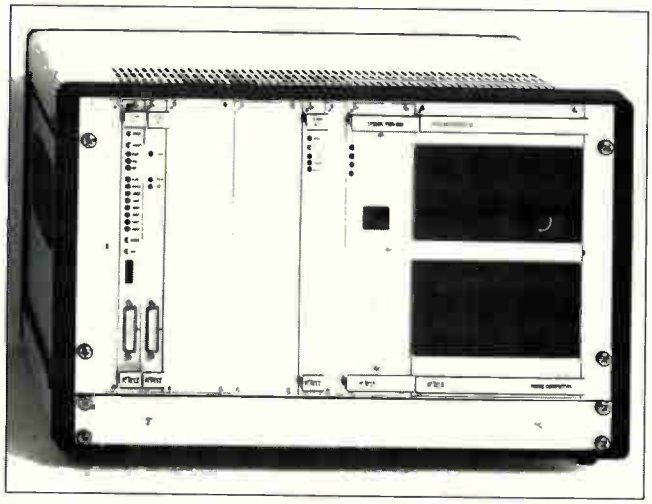
Microprocessors such as the 68020 are too fast for dynamic RAMs, Fischer says. The CPU frequently has to wait while reading and writing to memory. Fast cache can alleviate this problem but not completely solve it, because queries to 4-K bytes or 8-K bytes of cache will occasionally come up empty. SRAMs are an expensive alternative—the extra 500-K bytes costs $2,000, four times the cost of the same amount of DRAM—but Fischer says customers are willing to pay for the extra performance.

The SRAM is built from 64-K chips from Toshiba and NEC. Force will eventually replace the 64-K parts with 256-K SRAMs, expanding main memory to 4 megabytes.

There are over 200 companies making VMEbus-based products. Now IBM Corp. Personal Computers are being used heavily for some low-end development applications, but they can't handle graphics and image-recognition applications, Fischer says. These require special boards that plug into the bus.

The 2P21 is designed to act as a development system for high-end VMEbus products. Ideally, Fischer says, users would like to perform product development on a machine that is at least as fast as the machine for which they are developing the product.

Although the VMEbus was developed for the Motorola 68000 series, it is processor independent, Fischer notes. And the miniForce can be used to develop VME systems that use other processors. Some developers have put Intel 80286-based systems on the VMEbus; AT&T Technologies has developed a system with its 32100 processor; and the military 1750 32-bit CPU, the new Mips Computer Systems reduced-instruction-set computer chip, and National Semiconductor's 32032 systems have also been built on the VMEbus. In addition, some Small Computer System Interface boards have been built with VMEbus interfaces, so that control of peripherals can be offloaded.



DESIGN AID. The miniForce is fast enough to aid designers working in artificial intelligence and signal processing.

The 2P21 has six VMEbus expansion slots and two RS-232-C interfaces and comes with a 51-megabyte Winchester drive, a 1-megabyte floppy-disk drive, a screen editor, and a macro assembler. C, Fortran 77, and Pascal language compilers are also available. The system is priced starting at $15,990 and is available now.

Force Computers Inc., 2041 Mission College Blvd., Santa Clara, Calif. 95054. Phone (408) 988-8686 [Circle reader service number 338]

BAR-CODE MULTIPLEXER AIMS AT REAL-TIME NETS

In today's factories, products typically go through the manufacturing cycle bearing small bar-coded tags or labels for tracking by hand-held scanners. With its new Universal Identification Interface, Allen-Bradley Co. is out to cut factory costs by further automating that process.

The UII is a high-speed, intelligent multiplexer that supports a real-time interface between a host controller and up to eight tag sensors, such as bar-code scanners and radio-frequency devices. "Other companies in the bar-code industry have multiplexers, but none with the speed and functionality necessary for real-time networking," says Kenneth C.

Thompson, commercial marketing manager for identification products at Allen-Bradley's Sensing Products Business Unit in Milwaukee.

Bar-code multiplexers, such as those supplied by Intermec Corp. of Lynnwood, Wash., are designed for use with hand-held scanners, says David D. Perrine, commercial manager at the Allen-Bradley unit. But the UII is the only multiplexing product to date directed at the market for automatic sensor control where humans are taken out of the loop, Perrine says.

RF TAGS, TOO. Multiplexers for hand-held scanners typically communicate with sensors at 19.2 kb/s and work with bar codes only, Perrine notes. "I'm not aware of any other multiplexers for use with rf devices." By contrast, the UII will be able to mix both bar-code scanners and rf tag sensors on the same eight-node network.

That will include rf antenna-based devices which not only gather information from a product tag, but also write in information such as measurement or routing data. Because some rf tags can accommodate up to 2,000 ASCII characters, Allen-Bradley designed its UII net to run at 375 kb/s to ensure real-time control of multiple data-intensive read/write rf devices on the net.

The UII will save users money and I/O ports compared with current methods that require rf sensors to be point-to-point wired to the host, Perrine says. That's because only one host port is necessary to hook up to the UII, and wiring costs are lower than those for a multiple point-to-point implementation. In addition, the user will not be required to write software drivers for each individual point-to-point connection. With the UII, "by writing one driver for the host, the user can make it talk to eight different devices," Perrine explains.

In the UII, an Intel Corp. 80286 processor handles sensor read/write chores and an Intel 8344 performs protocol conversion between the various sensor types and host. Sensing devices will also require a built-in 8344 to run on the UII net, so Allen-Bradley is bringing out new versions of its rf-antenna and bar-code scanners.

The UII will sell for between $2,500 and $3,000, depending on volume, and will be offered in three versions. One is a card that plugs into an Allen-Bradley 6121 host, a ruggedized IBM Corp. Personal Computer AT. Another is a stand-alone version with host communication over RS-232-C or RS-449 connections. The third is a remote I/O version that links to an Allen-Bradley programmable controller serving as the host.

Maximum cable length for a UII network is 2,000 feet, with up to 100 foot-long sensor cables that will link to the net over a standard T-drop connector. UII network configuration programming is done from the host. A hand-hand monitor is included with the UII that can be used during network installation and debugging, for checking the status and configuration of sensors on the net.

For UII communication with the host, users initially will have the choice of either DF1 or RJD6, both proprietary Allen-Bradley protocols. The company plans later to also add capability for whatever protocol is specified for product tag identification tasks as part of the Manufacturing Automation Protocol specification. MAP standards organizations are currently contemplating RS-511 for that task, and a final vote is scheduled for this summer, Thompson says. "If they make a decision by August, we'll have it on the UII by about the January timeframe," he adds.

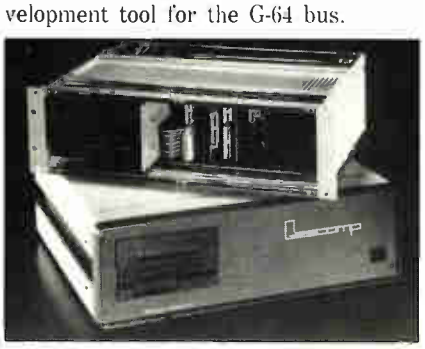
Like the UII, the 2750-AU rf sensor will be ready for delivery by July and will cost between $1,700 and $2,000. It will also carry an 8031 processor for handling data acquisition.

Set for November delivery, a comparably equipped bar-code scanner will let users mix both scanner types on the network and will sell for about $3,875 or $5,375 each, depending on scan-rate capabilities and other factors. Allen-Bradley says it will add other UII-compatible tag-sensor types, such as optical-character or magnetic-stripe readers, if demand develops. *–Wesley R. Iversen*

Allen-Bradley Co., 1201 S. Second St., Milwaukee, Wis. 53204.
Phone (414) 671-2000 [Circle 340]

GESPAC SYSTEM WORKS LIKE A PC AT

The Gescomp 8420 microcomputer runs on the company's proprietary G-64 bus but runs software for IBM Corp.'s Personal Computer AT. Its applications include machine and process control and automatic test equipment in harsh environments. The Gescomp 8420 also serves as a hardware and software development tool for the G-64 bus.



The system, which is built around an Intel Corp. 80286 16-bit microprocessor running at 6 MHz, comes with 1 megabyte of RAM, expandable to 16 megabytes. Units come with an 800-K byte floppy-disk drive and a 20-megabyte Winchester disk drive.

The price of a 1-megabyte, 80286 system is $7,950; a 512-K-byte system with a 68000 microprocessor sells for $6,750. The Gescomp 8420 is available now.

Gespac Inc., 100 W. Hoover Ave., Mesa, Ariz. 85202.
Phone (602) 962-5559 [Circle 352]

INDUSTRIAL COMPUTER WITHSTANDS RF NOISE

The CS200 industrial-grade computer is ruggedized for operation at 0°C to +55°C. Its rf noise levels are below FCC-A requirements by 20 to 30 dB. It has demand-paged memory management and scatter loading to optimize processing

speed and memory utilization. Memory can be expanded to 16 megabytes, and internal hard-disk storage is available in either 50- or 140-megabyte capacities. The operating system is AT&T Co.'s Unix V.

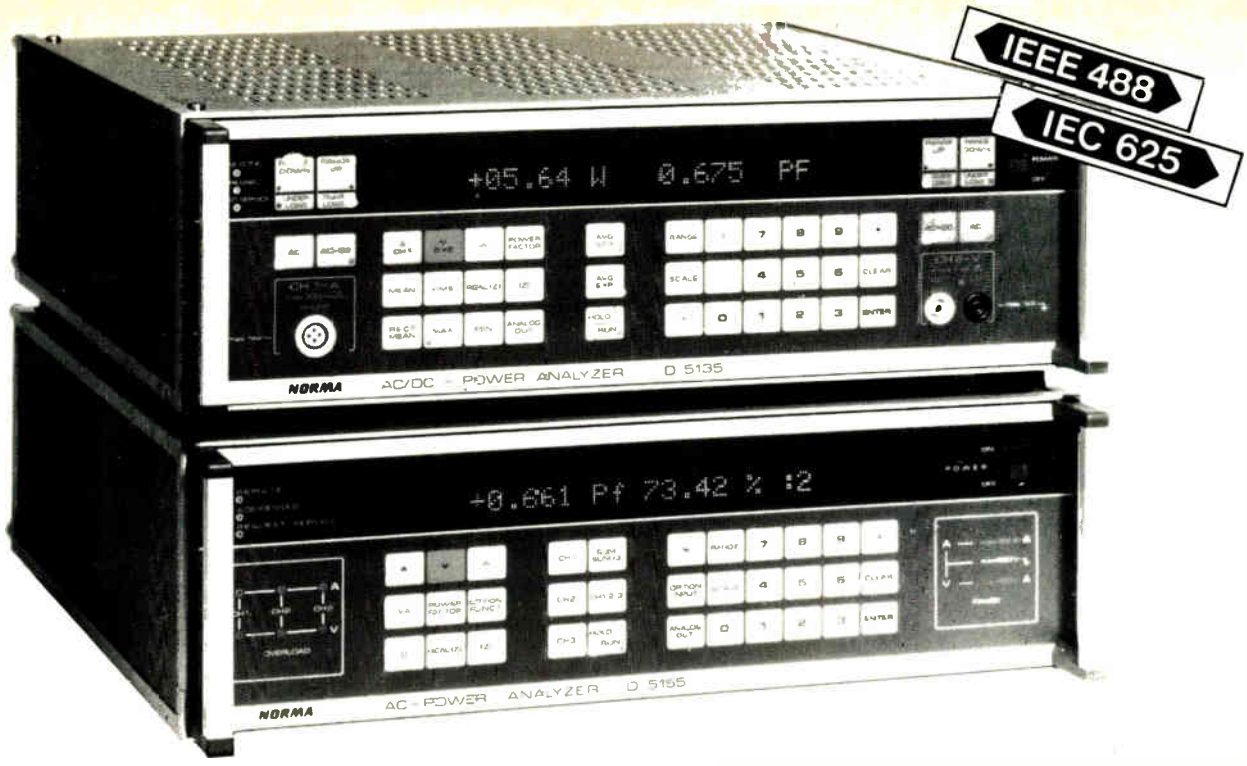
An optional communications board supports mainframe-to-mainframe communication and the X.25 and Ethernet network protocols. Other boards are available to support graphics and peripherals. Systems are available now from $12,995 to $18,000, depending on memory and storage configuration.

Cromemco Inc., P. O. Box 7400, Mountain View, Calif. 94039.
Phone (415) 964-7400 [Circle 351]

ECLIPSE COMES IN HIGH-SECURITY VERSION

The Tempest version of the Eclipse MV/4000 supports up to 64 users and stores up to 8 megabytes of main memory plus 500 megabytes of disk storage. The MV/4000T can process up to 700,000 instructions/s. Typical applications include software development, particularly of Ada programs, and command, control, communications, and intelligence.

An Eclipse MV/4000T with 4 megabytes of memory, 146 megabytes of disk storage, and a tape drive is priced at



Unmatched in Technology: AC POWER ANALYZER D 5155 AC/DC POWER ANALYZER D 5135 of NORMA

Two well-know meters of the D 4000 series (Multi-Functionmeter and Precision Wattmeter) have been enhanced to create the new AC and AC/DC POWER ANALYZERS.

AC POWER ANALYZER D 5155
The new AC POWER ANALYZER D 5155 takes three-phase measurements of active power, apparent power, power factor, energy, active resistance, impedance current and voltage.
Up to 32 values are obtained from a single measuring cycle (e. g. summation values). The wide scope of ranges 65 V–650 V and 0.1 A–50 A as well as the high accuracy of **0.1%** assure a wide range of applications in singlephase or polyphase systems.

Transformertesting-Version **NEW**
The special version for transformertesting will in addition measure the average value of all voltages, compute their form factor and correct the measured unload power losses in compliance with testing regulations. In case of lower power factors (short-circuit losses) measurements are effected at enhanced accuracy. This compact measuring system is particularly suitable for testing large transformers.

Motortesting-Version **NEW**
The special version for motor-testing features three additional DC voltage inputs for connection of transducers for mains frequency, rpm and torque. This compact measuring system acquires and computes all major characteristic quantities required in testing AC machines.

AC/DC POWER ANALYZER D 5135
The new AC/DC POWER ANALYZER D 5135 measures DC, AC and mixed quantities. For current and voltage, arithmetic mean, rectified mean and TRUE RMS values are obtained, supplemented by active power, power factor, active resistance and impedance.
The instrument measures DC components, AC components with their harmonics up to 100 kHz and the summation values.

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Microprocessors compute the measured values, check input and control the measuring cycles. Remote control is effected by IEEE 488 or IEC 625 Interface. An analog output permits graphic recordings of measured values.

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$123,886. Also available is the 6333T Tempest color dot-matrix printer, which runs at 200 characters/s for draft quality and 50 c/s for near-letter quality. Its price is $4,995. First shipments of both the computer and the printer are being made now.

Data General Corp., Federal Systems Division, 4400 Computer Dr., Westboro, Mass. 01580. Phone (617) 366-8911 [Circle 350]

8-BIT DAC HITS 300-MHz CLOCK RATE

The Bt108 8-bit digital-to-analog converter for color-graphics applications operates at clock rates as high as 300 MHz. The high-speed converter for terminals with screen resolutions over 2,048 by 1,536 pixels contains bias circuitry that allows it to run with either 10K or 100K ECL. It can drive a 50- or 75-Ω coaxial cable without need for external buffering.

The 300-MHz Bt108 comes in a 32-pin flatpack and sells for $87 in lots of 100. A 200-MHz version in a 24-pin Cerdip sells for $47. Production quantities are available now.

Brooktree Corp., 9950 Barnes Canyon Rd., San Diego, Calif. 92121.
Phone (619) 452-7580 [Circle 353]

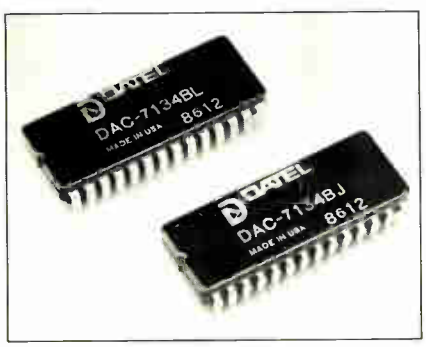
CONVERTER BOASTS 14-BIT LINEARITY

The DAC-7134 offers 14-bit linearity, combining a four-quadrant, multiplying digital-to-analog converter with on-chip correction circuitry. The PROM-controlled correction circuit eliminates errors introduced by the thermal stresses of packaging, the maker says.

For microprocessor-bus interfacing, the DAC-7134 converter uses standard memory write-cycle timing and control signals. Maximum differential linearity is specified at 0.003% full scale; the maximum gain temperature coefficient is ±8 ppm/°C.

The price in hundreds, in either the unipolar or the bipolar model, is $32.95. Delivery is from stock.

Datel, 11 Cabot Blvd., Mansfield, Mass. 02048. Phone (617) 339-9341 [Circle 354]



FLASH DACs USE JUST 35 mW

A family of 4-bit flash analog-to-digital converters with applications in television video digitizing and robot vision operates at up to 25 MHz while consuming just 35 mW. The conversion time for the CMOS CA3304/3304A family is 40 ns.

The converters come in two linearity-and-speed versions. The CA3304A is rated for ±⅛ least-significant-bit integral and differential linearity errors maximum at a top conversion speed of 25 MHz; the CA3304 provides ±¼ LSB linearity errors at a maximum conversion speed of 20 MHz.

The CA3304/3304A family are immune to latchup; an overflow bit means they can be connected in series to increase the converter circuit's resolution. In quantities of 1,000, prices for the flash converters, which are housed in plastic packages are $4.25 (model CA3304) and $6.50 (model CA3304A) each. They are available now.

RCA Corp., Solid State Division, Route 202, Somerville, N. J. 08876

BRIGHT LEDs CAN BACK LIGHT PANELS

The Multi-chip line of LEDs offers intensities of up to 60 millicandelas over a wide dispersion angle. The manufacturer says that's more than four times the light output of the best LEDs previously available, and makes the line bright enough to use as illuminators rather than just indicators. Types include two miniatures that the customer can order with plug-in diffusing lenses for uniform illumination over the viewing angle.

Applications include back lighting for panel legends and illuminated push-button switches. The LEDs come in red, amber, and green with color-coded cases. The Multi-chip line can be operated at up to 24 V, both ac and dc.

Depending on whether the illuminators contain four, six, or eight diodes, pricing in thousands ranges from $1.76 to $3.52 and will also depend on configuration. Delivery is from stock.

Data Display Products, 301 Coral Circle, El Segundo, Calif. 90245.
Phone (213) 640-0442 [Circle 361]

PAPERLESS PLOTTER CUTS MATERIAL USE

A 5-ft-high display, Softplot 2122 can display a full-color, size D engineering drawing—22 by 34 in.—before a hard-copy is made. The screens used by most computer-aided design systems are not large enough to show the full drawing.

Displaying the full drawing before it

is plotted saves money and time. Each plot would cost about $1 in paper, pens, and toner, the company says. Images are created in less than 1 minute compared with 6 to 8 min for plots created on an electrostatic device, or up to 1 hour on a pen plotter.

When it is integrated into the host system, Softplot 2122 plots in real time. Screen resolution is 400 dots/in.

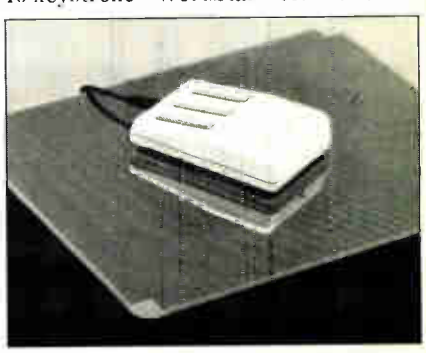
Softplot 2122 offers a 16-level gray scale and a palette of 4,096 colors, and lines can be drawn at widths from 10 to 50 mils in a single pass. Vectors can begin and end at any of 120 million addressable points with no distortion at the edge of the flat screen, at a write-erase speed of 2,000 in/s. In raster drawing mode, the user can view text and photo images as well.

Softplot 2122 emulates several common software plotting standards and also emulates Tektronix 4107 and IBM Corp. 3279 graphics terminals. Shipments will begin in the fourth quarter and delivery will be in 60 days. The quantity-one price is $46,176.

Greyhawk Systems Inc., 1557 Centre Point Dr., Milpitas, Calif. 95035.
Phone (408) 945-1776 [Circle 370]

MOUSE CONTROLS WORD PROCESSING

The SummaMouse interfaces with popular business and graphics software, including Lotus 1-2-3 and WordStar, on the IBM Corp. Personal Computer. The maker says that, with SummaMouse, a 16-keystroke WordStar command to



move copy requires only two keystrokes and a move of the mouse.

Because SummaMouse is electronic rather than mechanical, it reads by means of light reflected off a pad, for high accuracy and reliability. The peripheral also includes an on-board microprocessor, continual self-checking, a built-in RS-232-C port, and solid-state optical technology.

The suggested retail price of $119 includes the mouse, a 9-by-11-in. operating pad, a power supply, and software.

Summagraphics Corp., 777 State St. Extension, Fairfield, Conn. 06430.
Phone (203) 304-1344 [Circle 363]

OPERATING SYSTEM COMES IN 3 FLAVORS

Three new versions of the UniFlex/VM operating system each suit a different application. UniFlex/DA is a ROM-based system intended for process control; UniFlex/RT is a real-time system with full intertask communications; and UniFlex/MX is an enhanced version of the original virtual-memory operating system. All are for use with the 68020 microprocessor.

UniFlex/DA can be configured with or without a file system. UniFlex/RT includes a high-speed communications driver for transferring data and enqueue-dequeue, a mechanism that allows semaphore and resource-control operations. UniFlex/MX is designed for a multiuser, multitasking environment. Under it, the user can create multiple RAM disks for rapid access to frequently used files.

Available now, the UniFlex/VM sells for about $600 and the UniFlex/RT for about $1,000. Uniflex/DA is a customer-configured package, and the company will quote a price for it.

Technical Systems Consultants Inc., 111 Providence Rd., Chapel Hill, N. C. 27514.
Phone (919) 493-1451 [Circle 362]

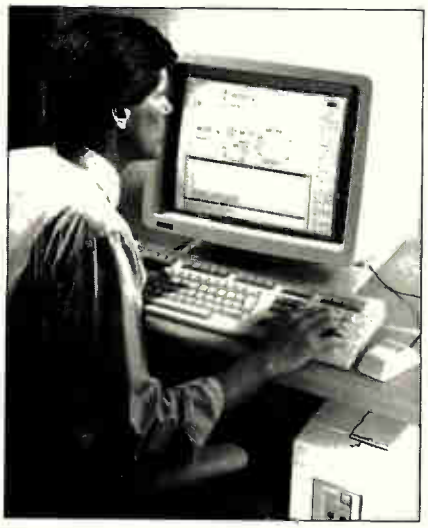
DEC'S ENTRY-LEVEL STATION IS $15,000

Digital Equipment Corp. has added an entry-level model to its VAXstation family of engineering work stations. The system, which is called the VAXstation II/RC, is built around the MicroVAX II processor.

Priced at less than $15,000, the work station is targeted at primary applications in electronics and mechanical computer-aided design, software development, computer-aided software engineering, and technical publishing.

The VAXstation II/RC is available in fixed-package systems of 3- and 5-megabyte configurations. Both include a 19-in. monochrome monitor, 71-megabyte disk drive, disk controller, Ethernet interface, 95-megabyte streaming tape drive, video subsystem, standard keyboard, and three-button mouse. Both the MicroVMS and Ultrix-32M operating systems can be used on the work stations. The systems are available now.

Digital Equipment Corp., 129 Parker St., Maynard, Mass. 01754. [Circle 369]



FRAME GRABBER READY FOR MICROVAX II

The DT2651 high-resolution frame grabber is a single-board image processor for Digital Equipment Corp.'s MicroVAX II computer. The single card does the work of comparable systems that have three to six boards.

The frame grabber performs real-time math and logic operations on single or multiple 512-by-512-by-8-bit images. The board works with most video sources, including slow-scan devices, to produce 256 gray levels. Thanks to an on-board multiplexer, the DT2651 can capture images from up to four cameras.

Typical image-processing functions include frame merging, subtracting, and offsetting. Priced at $2,995, the frame grabber can be connected to the DT2658 frame processor ($1,595) over external I/O ports for speeding lengthy image-processing calculations. The DT2658 processor greatly accelerates arithmetic-intensive image-processing operations. Units are available now.

Data Translation Inc., 100 Locke Dr., Marlboro, Mass. 01752.
Phone (617) 481-3700 [Circle 367]

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MEETINGS

VISION MEETING TO FOCUS ON EMERGING AREAS

The Computer Vision and Pattern Recognition conference, to be held June 22-26 in Miami Beach, will highlight several emerging technical areas of interest in the vision field. General chair Linda Shapiro notes that the new topics getting a lot more attention include parallel vision processing algorithms, machine vision, and motion analysis.

The parallel visual algorithms session will be one of the most important of the 20 technical categories at the conference, according to Shapiro, director of intelligent systems at Machine Vision International, Ann Arbor, Mich. "To be able to satisfy customer [real-]time requirements, you need parallel work."

Pipelined processing of data from individual pixels on parallel computing hardware as well as the implementation of convolution algorithms are key topics. Parallelism is also a key element at a session on industrial vision systems. In addition, W. Daniel Hillis, founding scientist at Thinking Machines Corp. in Cambridge, Mass., will give a special presentation on the company's Connection Machine and its parallel method of image processing.

Two motion-analysis sessions will feature several papers on how a vision system can determine an object's structure from its motion. Shapiro says that much of this work stems from government-sponsored research on developing a completely automated land vehicle. Other sessions will cover such topics as multiple scales, edge detection, two- and three-dimensional shape representation, character and word recognition, and stereo vision.

Computer Vision and Pattern Recognition, IEEE Computer Society (1730 Massachusetts Ave. N. W., Washington, D. C. 20036-1903), Fontainebleau Hilton Hotel, Miami Beach, Fla., June 22-26.

94th American Society for Engineering Education Conference, ASEE (11 Dupont Circle, Suite 200, Washington, D. C. 20036), Clarion Hotel, Cincinnati, June 22-26.

ATE East '86: Automatic Test Equipment Conference, Morgan-Grampian Expositions Group (1050 Commonwealth Ave., Boston, Mass. 02215), World Trade Center, Boston, June 23-26.

CPEM '86: Conference on Precision Electromagnetic Measurements, National Bureau of Standards, IEEE, and Union Radio Scientifique Internationale (Norman B. Belecki, National Bureau of Standards, NBS Facility, Gaithersburg, Md. 20899), NBS Facility, Gaithersburg, June 23-27.

EFOC/LAN 86: European Fiber Optics Communications & Local Area Networks Exhibition and Conference, Information Gatekeepers Inc. (Joan Barry, Information Gatekeepers, 214 Harvard Ave., Boston, Mass. 02134), International Congrescentrum Rai, Amsterdam, June 23-27.

Intellibuild Conference and Exhibition, International Intelligent Buildings Association Inc. (Department M-186, 1815 H St. N. W., Washington, D. C. 20006), McCormick Place, Chicago, June 23-27.

1986 Power Electronics Specialists Conference, IEEE (William Dunford, Department of Electrical Engineering, University of British Columbia, Vancouver, B. C., Canada V6T 1W5), University of British Columbia, Vancouver, June 23-27.

Advanced Manufacturing Systems Conference, Cahners Exposition Group (1350 E. Touhy Ave., Des Plaines, Ill. 60017-5060), McCormick Place, Chicago, June 24-26.

Symposium on Electromagnetic Compatibility, Minister of Posts and Telecommunications of the Polish People's Republic (EMC Symposium, 51-645 Warsaw 12, Box 2141, Poland), Technical University of Warsaw, Warsaw, June 24-26.

28th Electronic Materials Conference, Metallurgical Society (B. W. Wessels, Technological Institute, Northwestern University, Evanston, Ill. 60201), University of Massachusetts, Amherst, Mass., June 25-27.

Design Automation Conference, IEEE (J. D. Nash, Raytheon Co., Bedford, Mass. 01730), Las Vegas Hilton, Las Vegas, June 29-July 2.

FTCS-16: The 16th International Symposium on Fault Tolerant Computing, IEEE Computer Society (H. Kopetz, Interconvention Hofburg, P. O. Box 80, A-1107, Vienna, Austria), University of Vienna, Vienna, July 1-3.

International Conference on Radio Receivers, Institution of Electronic and Radio Engineers (99 Gower St., London, WC1E 6AZ, England), University College of North Wales, Bangor, England, July 1-4.

14th International Optical Computing Conference, IEEE Computer Society (Joseph Shamir, Department of Electrical Engineering, Technion, Haifa 32000, Israel), Hebrew University, Jerusalem, July 7-11.

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ELECTRONICS WEEK

ELECTRONICS IS BIGGEST BOSS...

The electronics segment of the U.S. economy again employed more people in 1985 than any other manufacturing industry. According to the American Electronics Association, the electronics industry—with more than 2.5 million employees—placed ahead of transportation products (2.03 million), food and kindred products (1.64 million), and nonelectrical machinery (1.61 million). Electronics has been the leader in employment since 1980, when it was responsible for just under 2 million jobs.

...AND CALIFORNIA BOOSTS LEAD

California continued to add jobs in electronics during the last year, strengthening its already overwhelming dominance in the industry. According to estimates by the American Electronics Association, California electronics companies employed 598,000 workers as of June 1985, an increase of 6,000 over the previous year and far ahead of second-place New York. The Empire State employed 226,000 in June 1985, a loss of 4,000 jobs over the 12 months. Third was Massachusetts, which held steady at 214,000. Texas, a distant fourth at 157,000, showed the biggest increase in electronics employment as it gained 11,000 jobs.

HOME VIDEO SALES STILL INCREASING

Home video products are enjoying solid sales, extending even to the poor man of the industry, monochrome TVs. Sales of video cassette recorders to U.S. dealers for the first four months of 1986 totaled 3.7 million units, some 15% ahead of last year's trend-setting pace, according to the Electronic Industries Association's Consumer Electronics Group. Color-TV sales likewise rose, with dealer shipments though April totaling 5.3 million units, some 5% ahead of 1985, which was a record year. Even monochrome TVs are showing strength after several years of declining sales. Shipments totaled 1.1 million units for the year—some 3.7% ahead of last year's first-quarter pace.

GERMANY FUNDS 4-Mb RAM PROJECT

West Germany's Ministry for Research and Technology has decided to support the joint Siemens-Philips development of 4-Mb random-access memories to the tune of $145 million. The ministry was skeptical that the two companies could attain a leading position in the high-density-RAM market, but an international group of experts appointed by the Dutch and German governments found the project worth supporting, given the market potential of the 4-Mb parts.

DIP IN PROFITS KEEPS HP LID ON

Hewlett-Packard Co. will keep the lid on expenses and hiring following the announcement of a bare 6% increase in earnings and a 2% decrease in profits for the second quarter of fiscal 1986. HP credited international sales, up 10% to $855 million, for pushing net revenue to $11.778 billion, but laid much of the gain to a weakening of the dollar. HP's U.S. business has been "essentially flat" for the past two years, said HP president John A. Young.

GENRAD, DAISY TO SELL INTERFACE

Genrad Inc., Milpitas, Calif., and Daisy Systems Corp., San Jose, Calif., have inked a joint marketing deal for a software interface that goes a step beyond test-vector simulation. With the interface, users of Daisy's Logician and MegaLogician can debug chips through access to the control program for two Genrad testers, including the new 120-MHz GR 180. A single license for the software will cost $10,000.

MENTOR BUYS JAPANESE PARTNER

Mentor Graphics Corp. has bought out Marubenl Hytech, its partner in a Japanese co-venture, as part of a series of moves expanding its Asian and European operations. Mentor, of Beaverton, Ore., has also added a seventh Asian sales office, in Osaka, Japan, and another European office, this one in Zurich, Switzerland. Foreign sales accounted for 37% of Mentor's 1985 revenues of $137 million. It claims 65% of an estimated $38 million market in engineering work stations in Japan.

CONCORD DATA IN JOINT MAP DEAL

Omron Tateishi Electronics Co., Kyoto, Japan, and Concord Data Systems Inc., Marlboro, Mass., have agreed to jointly develop equipment such as local-area networks and communications-control systems that will conform to the Manufacturing Automation Protocol. Concord Data will transfer production technology for its C2000/C500 personal computer, while the Japanese maker will customize it for marketing to Japanese customers. Omron Tateishi also is studying the possibility of manufacturing automated teller equipment in the U.S. to overcome the negative effects of the stronger yen on its export sales.

SME FINANCES PRODUCTION STUDIES

The Society of Manufacturing Engineers has awarded $398,406 in cash grants to 63 universities and technical institutions for work in manufacturing technology and productivity, and to further manufacturing engineering as an academic discipline. Also, in-kind equipment grants amounting to $222,748 were awarded to 29 schools. These are gifts from companies and include software for computer-aided design and manufacturing, milling machines, lathes, and robots.

ARCO SOLAR SIGNS FOREIGN PARTNER

Arco Solar Inc. has formed its second joint venture in two months, joining forces with a West German company in the still-infant photovoltaic markets. The Los Angeles subsidiary of Atlantic Richfield Co. and Siemens Interatom GmbH have agreed to manufacture and market thin-film photovoltaics for emerging solar-energy markets in Europe. The two companies will set up a manufacturing plant in Europe based on Arco Solar's thin-film technology as well as perform joint research on high-performance products. In March, Arco Solar signed a similar joint manufacturing pact with Showa Shell Sekiyu KK of Japan.

NSF FUNDS LINK TO SUPERCOMPUTERS

The National Science Foundation's Office of Advanced Scientific Computing will finance the creation of a new communications network linking universities in 12 southeastern states and the District of Columbia to NSF's five supercomputer centers. More than $1.4 million will be awarded to Southeastern Universities Research Association (SURA), a 35-member university consortium based in Arlington, Va., to construct and operate SURAnet, the NSF's first regional data-communications network. The network will initially include 56-kb/s transmission links, eventually to be upgraded to 1-Mb/s speeds.

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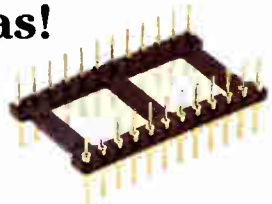

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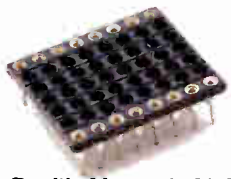

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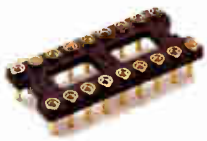

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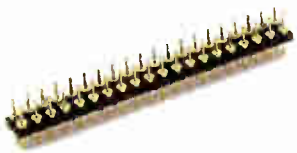

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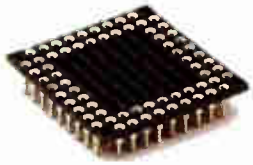

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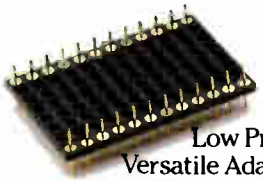

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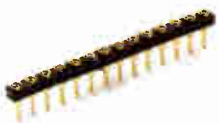

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