A McGRAW-HILL PUBLICATION

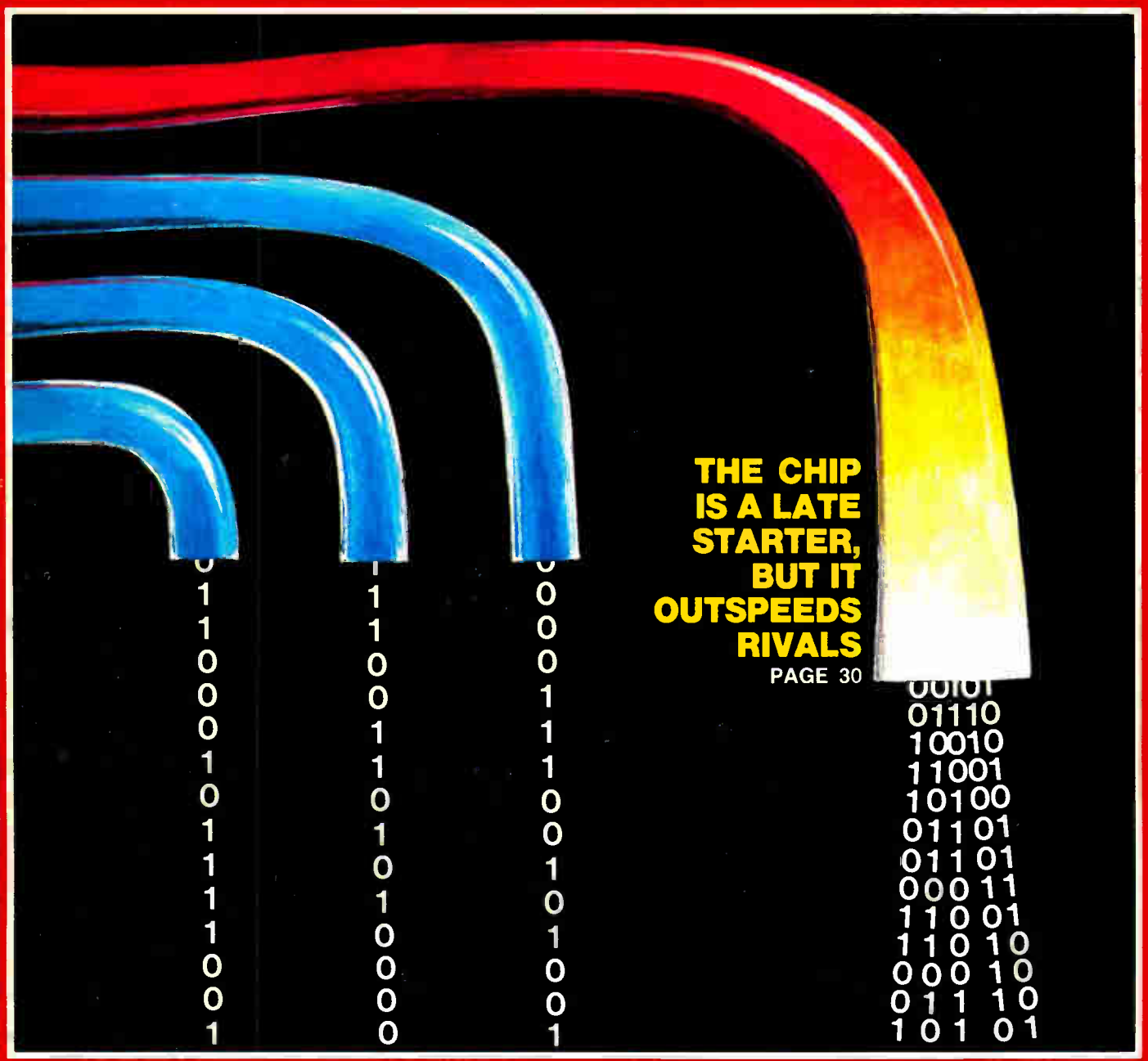
THREE DOLLARS

Electronics

THE WORLDWIDE TECHNOLOGY WEEKLY

MARCH 10, 1986

MOTOROLA'S SIZZLING NEW SIGNAL PROCESSOR

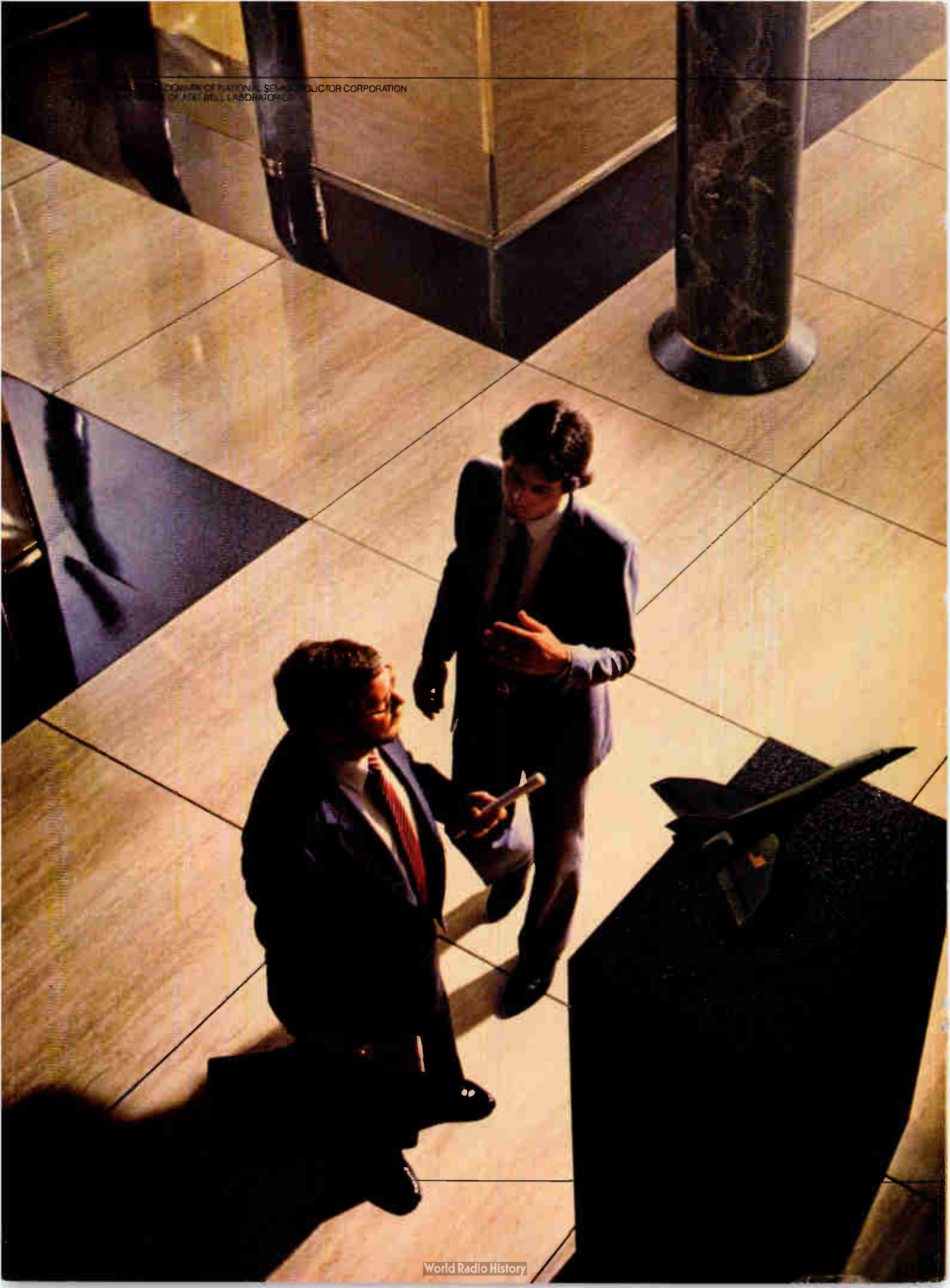


THE CHIP IS A LATE STARTER, BUT IT OUTSPEEDS RIVALS

PAGE 30

SUPERCOMPUTING HITS ITS STRIDE/44

CAN IBM MAKE THE LAPTOP MARKET HAPPEN?/59



"We did it!"

"It's our competitors' faces I want to see. We've really cracked this market now."

"Like National's 32-bit microprocessor family?"

"I knew we'd close that sale. Did you see their faces?"

"Looks like we made all the right decisions at the right times."

"You can't build a system out of data sheets and promises. National had it, they delivered it, and they got us here first."

While you're still dreaming about success, Sequent is delivering it. With National's Series 32000 family.

On January 17, 1983, eighteen people started a new company called Sequent Computer Systems. They had no product, no plan, no backing. Only a dream.

Two years later, that dream came true. They delivered their first system—a sophisticated parallel processing computer. A full year ahead of their competitors.

How'd they do it? Hard work. Calculated risks. Belief. And a critical decision. They chose the Series 32000™ microprocessor family.

It offered them a *complete* 32-bit microprocessor family, including demand paged virtual Memory Management, Floating Point, and other peripherals with full UNIX™ support.

But the Series 32000 wasn't just the right engineering decision, it was the right *business* decision. It helped Sequent get their system to market fast. First.

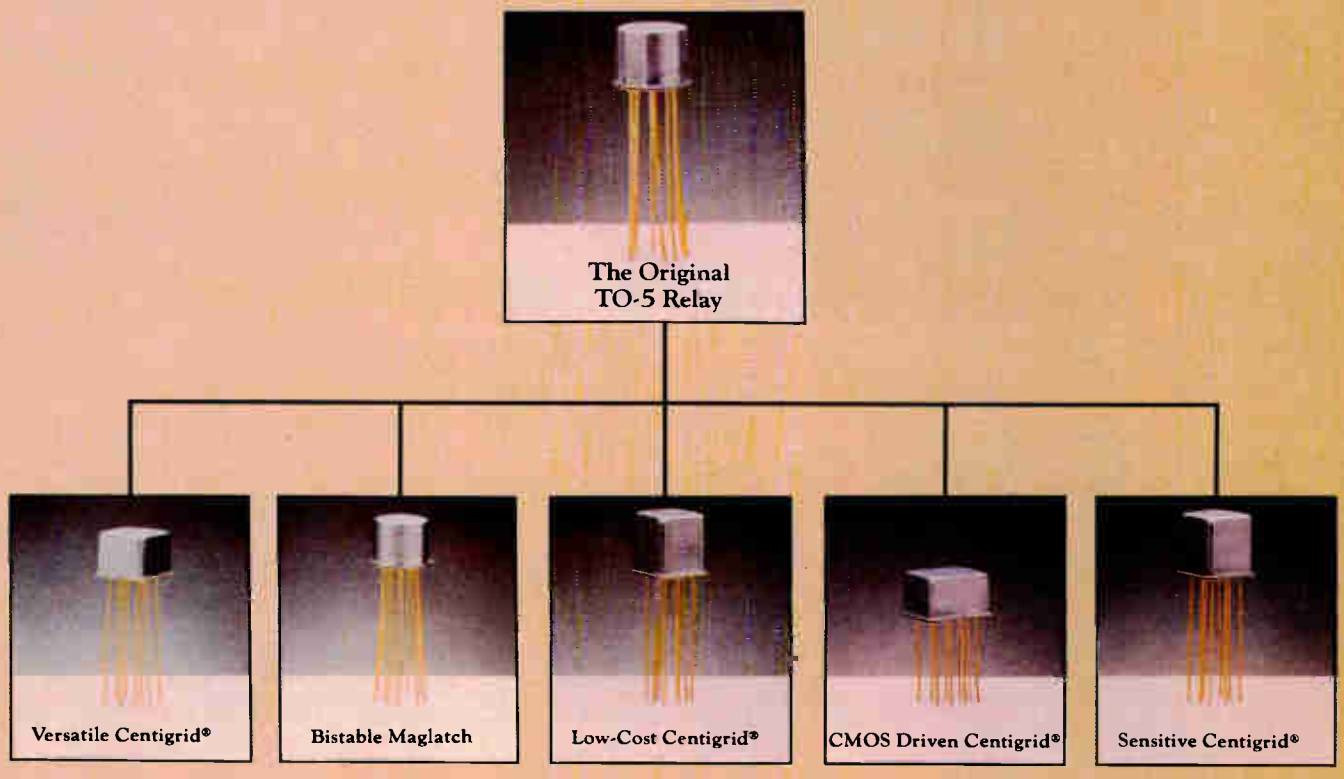
Sequent hit their window of opportunity. And that window is still open—for now. So find out how the Series 32000 can help you build your own success story. Contact National Semiconductor today.

National's Series 32000. MS 23-200
P.O. Box 58090
Santa Clara, CA 95052-8090

National Semiconductor
We're doing it.

Circle 1 on reader service card

From the industry's first choice come the industry's first choices.



We designed the original TO-5 relay over 20 years ago. But that was just the beginning. Since those first days, we nudged it into fathering a family of adaptations and extensions along the way.

In the process we also pioneered many innovative techniques for production, for manufacturing, and for quality control to ensure a reliability level so consistently high it would be taken for granted.

Of course, for us it never was.

Soon, TO-5 relays were available in latching versions, in single, double and 4-pole styles, and in hybrid versions with internal diode and transistor drive. All with excellent RF switching characteristics.

Today, there's a version for just about any application—general purpose and sensitive, commercial, and military (qualified to "L," "M" and "P" levels of MIL-R-39016).

Our family boasts the Centigrid,® possibly the most advanced hermetically sealed armature relay available today. The Maglatch, a relay with memory and low power requirements. And lots of brothers and sisters to handle applications like high temperature, high shock, and high vibration designs for critical, hi-rel applications. We even have versions that can be driven directly from CMOS and TTL (qualified to "L" and "M" levels of MIL-R-28776).

If you'd like complete technical information on our TO-5 relay and all its offspring, or some applications help, or just a little history, drop a note or give us a call.

Like proud parents, we love to talk about the family.

TELEDYNE RELAYS
Innovations In Switching Technology

12525 Daphne Ave., Hawthorne, California 90250 • (213) 777-0077
European Hqtrs: Abraham Lincoln Strasse 38-42 • 62 Wiesbaden, W. Germany 06121-7680
Belgium Sales Office: 181 Chaussee de la Hulpe • 1170 Brussels (2) 673-99-88
U.K. Sales Office: Heathrow House, Bath Rd., Cranford, Hounslow, Middlesex, TW 5 9QQ • 01-897-2501
Japan Sales Office: Nihon, Seimei Akasaka Building • 8-1-19 Akasaka, Minato-Ku Tokyo, 107 Japan (03) 403-8141

Circle 2 on reader service card

MARCH 10, 1986 VOLUME 59, NO. 10

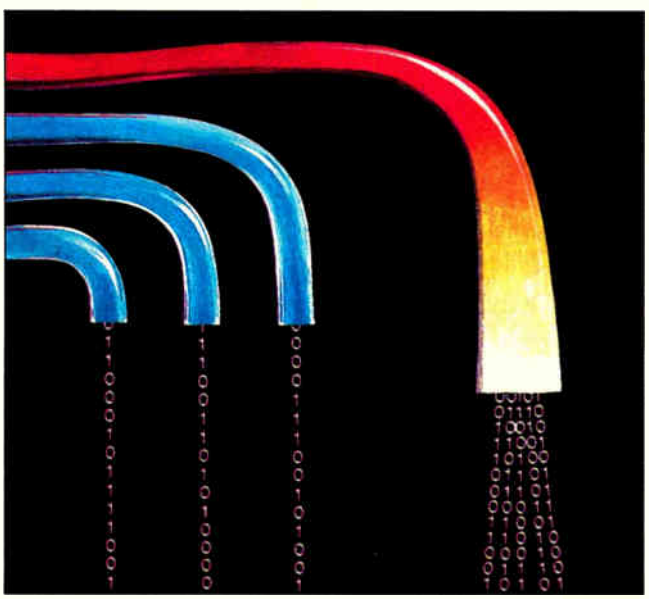
Electronics

NEWS

INSIDE TECHNOLOGY

PROBING THE NEWS

COVER



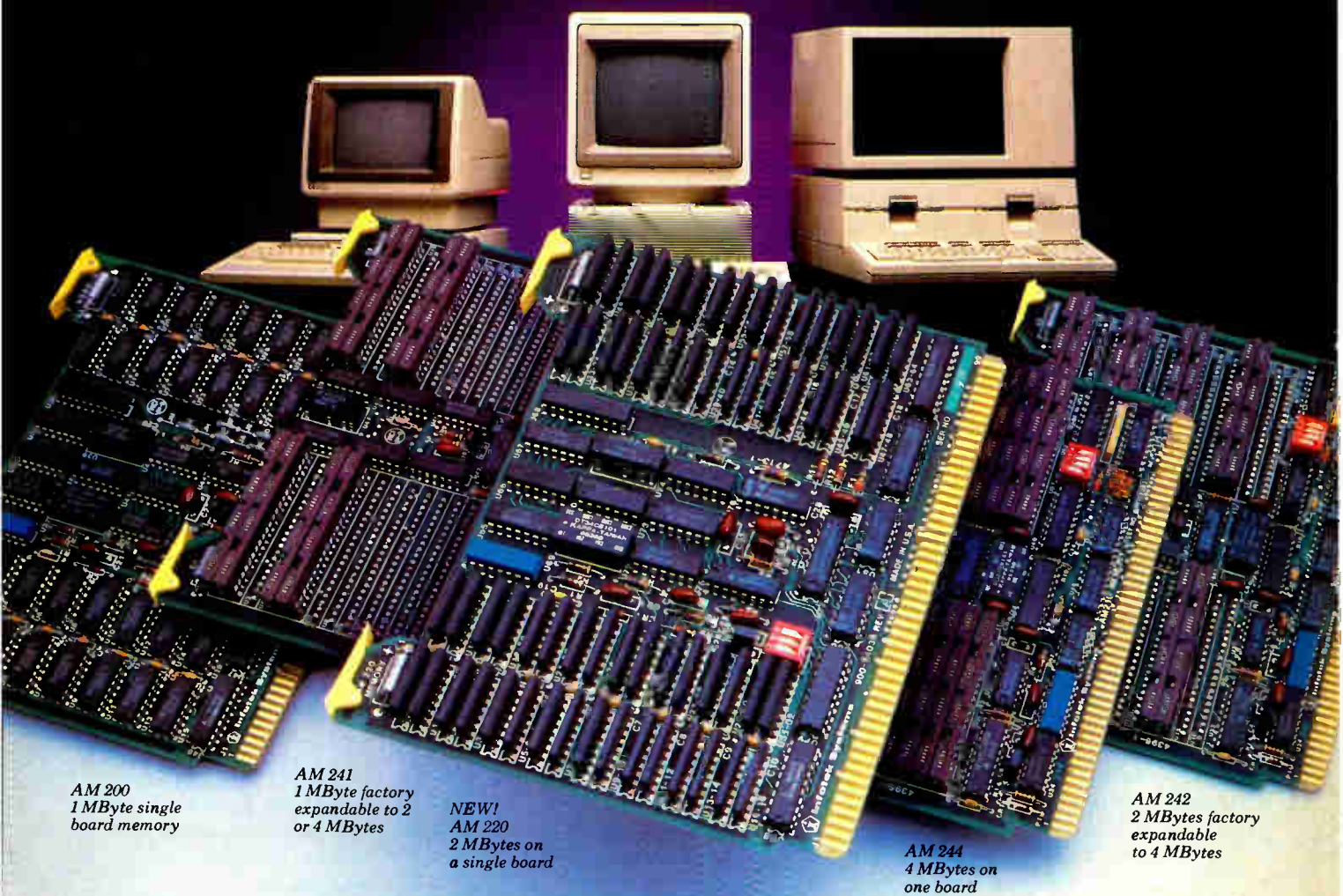
Cover illustration by art director Fred Sklenar

NEW PRODUCTS

DEPARTMENTS

MEGABYTES NOT MEGABUCKS

That's what you get from Infotek's new cost and space saving 2 MByte HP 9000-compatible memory.



AM 200
1 MByte single board memory

AM 241
1 MByte factory expandable to 2 or 4 MBytes

NEW!
AM 220
2 MBytes on a single board

AM 244
4 MBytes on one board

AM 242
2 MBytes factory expandable to 4 MBytes

Now, you can have a full two megabytes of instantly accessible memory for your HP Series 300 and Series 200 computers for a price you'd expect to pay for 1 MByte. That's like getting half your memory free! And even better, you get those 2 MBytes on a single board, so all that extra capability occupies only one I/O slot. You just plug in the new board in seconds with no special tools required.

The new Infotek AM 220 2 MByte memory board is ideal for all scientific and engineering applications where large memory requirements remain constant. A 1 MByte product is also available at a very reasonable cost; and, for maximum capacity, Infotek offers a 4 MByte single board memory.

If your data storage needs are growing, you can have Infotek's unbeatable price/performance/size benefits in an expandable single board memory—1 MByte of memory upgradeable to 2 or 4 MBytes, or a 2 MByte board which expands to four when memory requirements increase. You can even get a floating point processor and 1 MByte of memory on a single board.

Of course, all Infotek memory boards have the high quality you demand for your HP system. Their exceptional reliability is backed by a two-year warranty. So increase productivity, save time, and enhance the capability of your HP 9000 computer. Call Infotek toll free today. The only way to get MegaBytes without spending MegaBucks.

Infotek Systems, 1400 North Baxter Street, Anaheim, California 92806-1201, (714) 956-9300, (800) 227-0218, in California, (800) 523-1682, TELEX 182283.

INFOTEK SYSTEMS
A DIVISION OF ALS CORPORATION

Your Second Right Decision.

Circle 4 on reader service card

English majors can have a tough time after graduation because the world isn't loaded with career opportunities for them. But reading and writing are good training for the journalist's life. And given an ample supply of curiosity, a nose for news, and doggedness in the search for facts, the person with a degree in English can find a career in journalism. Eve Bennett of our Palo Alto bureau is one of those.

EVE BENNETT: From digging for oil to digging for news.

Actually, Eve has some science in her educational background. A native of Covington, Ky., Eve, 26, traveled to Southern California after high school armed with scholarship aid from the Society of Exploration Geophysicists—the people who prospect for oil—to attend the California Institute of Technology in Pasadena. "I studied geophysics and literature for two years there. Then it dawned on me that I was more comfortable with the literature than the geophysics, so I transferred to the University of North Carolina at Chapel Hill, where I graduated with a BA in English lit," she says.

Eve started work for *Electronics* as a secretary a year later, and has successfully made the transition to reporting and writing. She does a little bit of everything. For example, in this issue, Eve contributed reporting to the story on Sierra Semiconductor Corp.'s integration of analog and digital logic with single-bit electrically erasable programmable read-only memory on a standard cell (p. 14) and wrote a People profile of Teledyne Semiconductor's young president, Mitchell Goozé, on p. 65. She also frequently writes stories for Companies and New Products, in addition to making frequent contributions to the newsletters.

For her part, Eve says, "I've been fortunate to be based in Silicon Valley, where so much of the exciting electronics technology is being developed." For our part, we are glad that Eve decided that it is more exciting to pursue the news of the electronics industry than to look for oil.

We have a surprise for you. Our cover story, on p. 30, reveals that Motorola Inc. has a state-of-the-art digital signal processor, a fact that up to now has not been known to the electronics industry. The article came from our Dallas bureau manager, J. Robert Lineback. "I wish I could say I got the story because I'm a great reporter, but the fact is we got it because [Motorola program manager] Bryant Wilder is a dedicated reader and a fan of *Electronics* and thought the magazine was the place for the story," Rob says.

He recalls that after Wilder telephoned, "it was just a matter of going out to Motorola with a tape recorder. I wish they were all that easy."

Laurence Altman

March 10, 1986 Volume 59, Number 10
94,587 copies of this issue printed

Electronics (ISSN 0883-4989) Published weekly by McGraw-Hill Inc. Founder: James H. McGraw 1860-1948. Publication office: 1221 Avenue of the Americas, N.Y., N.Y. 10020; second class postage paid at New York, New York and additional mailing offices. Postage paid at Montreal, P.Q. Registration Number 9034.

Executive, editorial, circulation, and advertising addresses: Electronics, McGraw-Hill Building, 1221 Avenue of the Americas, New York, N.Y. 10020. Telephone (212) 512-2000. Teletype 12-7960 TWX 710-581-4879. Cable address: M C G R A W H I L L N E W Y O R K.

Subscriptions limited to professional persons with active responsibility in electronics technology. No subscriptions accepted without complete identification of subscriber name, title or job function, company or organization, and product manufactured or services performed. Based on information supplied, the publisher reserves the right to reject nonqualified requests. Subscription rates: the United States and possessions $32 one year, $55 two years, $76 three years; company addresses and company libraries $40 one year, $67 two years, $93 three years; Canada and Mexico $34 one year, $57 two years, $78 three years; Europe $50 one year, $85 two years, $125 three years; Japan, Israel, and Brazil $85 one year, $140 two years, $200 three years; Australia and New Zealand $95 one year, $170 two years, $240 three years, including air freight; all other countries $50 one year, $85 two years, $125 three years. Limited quota of subscriptions available at higher-than-basic rate for persons allied to field served. Check with publisher for these rates. Single copies $3.00. Please allow four to eight weeks for shipment.

Officers of McGraw-Hill Information Systems Company: President Richard B. Miller, Executive Vice Presidents: Frederick P. Jannot, Construction Information Group; Russell C. White, Computers and Communications Information Group; J. Thomas Ryan, Marketing and International, Senior Vice Presidents: Francis A. Shinal, Controller; Robert C. Violette, Manufacturing and Technology. Senior Vice Presidents and Publishers: Laurence Altman, Computers and Communications; Harry L. Brown, Computers and Communications; David J. McGrath, Construction Group Vice President; Peter B. McCuen, Communications. Vice Presidents: Fred O. Jensen, Planning and Development; Margaret L. Dagner, Human Resources.

Officers of McGraw-Hill Inc.: Harold W. McGraw Jr., Chairman; Joseph L. Dionne, President and Chief Executive Officer; Robert N. Landes, Executive Vice President and Secretary; Walter D. Serwatka, Executive Vice President and Chief Financial Officer; Shel F. Asen, Senior Vice President, Manufacturing; Robert J. Bahash, Senior Vice President, Finance and Manufacturing; Ralph R. Schulz, Senior Vice President, Editorial; George R. Elsinger, Vice President, Circulation; Ralph J. Webb, Vice President and Treasurer.

Subscribers: The publisher, upon written request to our New York office from any subscriber, agrees to refund that part of the subscription price applying to copies not yet mailed. Please send change-of-address notices or complaints to Fulfillment Manager, subscription orders to Circulation Manager, Electronics, at address below. Change-of-address notices should provide old as well as new address, including zip codes. Attach address label from recent issue. Allow one month for change to become effective. Subscriber Service: call (201) 356-7980, 9 a.m. to 4 p.m. EST. Postmaster: Please send address changes to Electronics, att: Fulfillment Manager, CN 808, Martinsville, N.J. 08836.

Editorial department phones: Administration (212) 512-2645, News and New Products (212) 512-2685, Technology (212) 512-2666. Bureaus: Boston (617) 262-1160, Chicago (312) 751-3811, Dallas (214) 458-2400, Los Angeles (213) 480-5234, New York (212) 512-3322, San Francisco/Palo Alto (415) 968-2712, Washington (202) 463-1650, Frankfurt 72-5566, London 493-1451, Paris 42-89-03-80, Tokyo 581-9816. **Business departments:** (212) 512-3469 (Business departments follow the Advertisers' Index).

WEEK 20

If you're serious about competing in the high-end 32-bit systems game, it's time to sign up for the first register file, and the first microprocessor family, designed for high-performance. We're talking about the Am29334: Our new 64-word, Four-Port, Dual Access register file. It's the first chip in a set that will soon be found at the heart of tomorrow's hot, new 32-bit systems, our Am29300 family.

Like the other Am29300 family members, the Am29334 boasts speed a plenty. In this case, 80ns cycle and 24ns access times. So it won't slow down your 32-bit hardware.

Am29334

Register for the 32-bit performance race.

In the long run, though, the Am29334's high-performance architecture is just as important.

Four data ports (two input and two output) allow simultaneous read or write access to two 16-bit data words in the same cycle. So you can fetch a full 32 bits with no performance penalty.

Or you can easily cascade Am29334s to handle 32-bit words. Or 64-bit words. Or larger words if you like. And at the same time, you can increase the depth to 128 words, 256 words and beyond.

What's more, each Am29334 word contains two parity bits to support fault detection/correction schemes (like the one in our Am29300 family) to keep your system going at full speed.

And, like the rest of the family, the Am29334, will be available in CMOS and ECL, in addition to the current TTL version.

The Am29334 guarantees winning performance no matter how you plan to run the race.

Design and application seminars are available for this product. Write or call for information.

Circle 151 on reader service card

WEEK 21

Our new 256K CMOS DRAMs give you more than just the bits you need to build large, high-speed memory systems. So much more, in fact, you might want to grab a pencil and paper.

For openers, put down "power." Not just "stand-by power," although ours is as low as 100μA, but "data retention power," as well. By pushing the refresh cycle out to 32ms, we've pushed the retention current down to 230μA. So you can finally combine the density of DRAMs with the reliability and portability of battery back-up.

Am90C255/256/257

More than enough to remember.

Then write down "speed." With their 100ns access times, these DRAMs will keep pace with your systems.

Don't put the pencil down yet. There's more:

There's a choice of 3 addressing modes. Nibble mode (Am90C255), enhanced page mode (Am90C256), or static column mode (Am90C257). The last two with continuous data rates of over 18MHz.

If all that seems like a lot, then just write down "CMOS DRAMs—AMD."

That's really all you need to plug into your memory.

Circle 152 on reader service card

WEEK 22

The improved features of our new AmPAL18P8 IMOX™ PAL* device are the result of some very careful reasoning.

Why not, for example, allow designers to plug increased logic power into their designs, without the extra cost of a 24-pin package? So the 20-pin AmPAL18P8 comes loaded with 8 bidirectional I/O pins (not 6), 18 inputs (not 16), and an additional product term per output (a total of 8 plus OE). The perfect foundation for more complex logic functions.

And why not mix outputs—both active high and active low—on the same chip? So the AmPAL18P8's output polarities are user programmable. Eliminating outboard inverters and extra circuitry.

AmPAL18P8

There's a lot of logic in this.

Finally, why not give this advanced logic the speed, power and reliability benefits of our most advanced technology? So the AmPAL18P8 is implemented using platinum-silicide fuses and our exclusive IMOX process.

The AmPAL18P8. Choose it because of all the logic that went into it.

*PAL is a registered trademark of, and is used under license from, Monolithic Memories, Inc.

Circle 153 on reader service card

WEEK 23

Just a quick reminder. Now that our Am2970 Dynamic Memory Timing Controller is in volume production, you've got everything it takes to refresh dynamic memories without robbing the CPU of valuable processing time.

That's because the Am2970 can be programmed to initiate refresh cycles independently, while the CPU is busy with other tasks. This "hidden refresh" technique will give your system higher throughput without extra cost or design penalties.

But even if you can't always use hidden refresh, the Am2970 is something to remember.

Am2970

We'll refresh your memory in no time.

After all, unlike other controllers, the architecture of the Am2970 allows you to schedule timing signals when they're really needed, instead of when the system clock thinks they're needed. And that, in turn, means you have the unique ability to balance refresh, CPU and DMA requests for maximum memory performance.

Keep in mind, too, that the Am2970 is the perfect companion for our popular Am2968A Dynamic Memory Controller. And with the upcoming Am2969 Controller (which supports error detection and correction), the Am2970 is part of the most flexible 256K dynamic memory controller family on the market.

The Am2970. Use it once and it will stay in your memory forever.

Circle 154 on reader service card

On October 1, 1985, Advanced Micro Devices committed to deliver fifty-two new products in one year. One a week. Every week. On the shelf. In volume.

After 13 weeks, our customers could reduce networking costs, modernize old state machines, revive fading memories and see graphics in a whole new light.

If you haven't seen the solution to your problem yet, the game has just begun.

Watch this space for thirty-nine more new products. One a week. In volume. On the shelf.

That's not a promise. There are too many promises in this business. That's a commitment.

Advanced Micro Devices

901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088
Call toll free (800) 538-8450, ext. 5000, inside California, call (408) 749-5000.

BOOKS

OP AMP NETWORK DESIGN
John R. Hufault
Wiley/Interscience
$34.95/440pp
The applications-oriented *Op Amp Network Design* is for circuit designers on tight schedules. After discussing network parameters, the author presents over 300 networks, all of which can be modified, with component values included. The emphasis here is on tradeoffs—such as between physical space and accuracy when it comes to the dielectric absorption parameter in a holding network, or between frequency stability and amplitude stability in a sine-wave oscillator. The author, a private consultant, was a Hughes Aircraft Co. instrumentation designer for the space shuttle research program.

MICROPROCESSOR SOFTWARE PROJECT MANAGEMENT
Eli T. Fathi and
Cedric V. W. Armstrong
Marcel Dekker Inc.
$57.50/368pp
Microprocessor Software Project Management breaks down the process of microprocessor software development into subsystems, making a project easy to track. Under "documentation classification," for example, the authors list each category—preliminary, system, program, data, operations, user, and control. They then go on to list documentation problems, causes, and solutions, ending with a policy checklist.

The book's core is the chapter on "Principles of Project Management," based on D. J. Reifer's 1981 tutorial for the Computer Society of the Institute of Electrical and Electronics Engineers. No project is likely to fit all the authors' paradigms exactly, but the authors have foreseen many problems; both Parkinson's Law and the Peter Principle receive mention.

Eli T. Fathi is vice president of engineering at Pertronics Technology Inc. Cedric V. W. Armstrong is president of Tridex Systems Inc. The book is based on a course for software engineers at the Ontario Centre for Microelectronics, Ottawa, Canada.

KOREAN SEMICONDUCTOR INDUSTRY ANALYSIS
Dataquest Inc.
$2,500/150pp
Dataquest's Japanese Semiconductor Industry Service has compiled and analyzed data on Korean companies and their manufacturing capabilities, support services, and technology. Information presented here includes data on the proliferation of foreign companies in Korea and investment there by low-cost contract manufacturers. Companies that already are clients of any of Dataquest's Semiconductor Industry Services can purchase this report for $1,900.

ANALOG-DIGITAL CONVERSION HANDBOOK
Third Edition
Engineering Staff of
Analog Devices Inc.
Daniel H. Sheingold, Editor
Prentice-Hall Inc.
$32.95/733pp
For the 1986 edition of the *Analog-Digital Conversion Handbook*, the authors have restored the "Guide for the Troubled," the bibliography, and the index, which were dropped from the 1977 (second) edition. Other new or rewritten chapters include those on testing, specifying, and applying converters. Entire design areas—video conversion, synchro and resolver converters, analog-to-frequency converters, and intentionally nonlinear converters—have been added.

STATUS 1986
Integrated Circuit
Engineering Corp.
$245/200pp
The 20th annual issue of this report on the integrated-circuit industry says that to survive 1986, companies must increase cooperative efforts in research and development as well as production. The report also says that high-density memories are the product to watch this year. *Status 1986* covers the worldwide semiconductor market, open-market IC suppliers, U. S. captive suppliers, technology trends, and more.

THE CREATIVE ENGINEER: THE ART OF INVENTING
Winston E. Kock
Plenum Press
$25/385pp
Is a creative engineer an oxymoron? Not according to Winston E. Kock, who argues in *The Creative Engineer* that creativity is more than just a sudden intuition or feeling—it is a synthesis of imaginative and technical skills effectively transformed into useful products.

Kock, an inventor and pioneer in acoustics, electronics, and optics, examines the adventure of inventing, drawing upon his own background. In addition, he suggests methods of nurturing creativity in engineering. For example, he strongly suggests pursuing an interdisciplinary curriculum. The combination of his own interests in music and electronics led him to invent the reedless, pipeless organ in 1932.

TECHNOLOGY NEWSLETTER

TI RESURRECTS ITS SOLAR-CELL RESEARCH

A closed-loop solar energy system that Texas Instruments Inc. once was developing for homes could emerge as supplementary generating equipment for electric utilities. TI researchers in Dallas have quietly reconfigured the system so that it might be a suitable alternative to high-cost conventional generators used mainly for peak-load periods. TI researchers have seen conversion efficiencies of 12% and expect to reach 15% with improvements to the highly manufacturable, single-crystal silicon spheres making up the solar-array collector. TI's solar cell, originally conceived by integrated-circuit pioneer Jack Kilby, combines silicon photovoltaics and hydrogen bromide fuel cells. In its new design, TI has unbundled the original system, separating the hydrobromic-acid electrolyte from the tiny silicon spheres. Separation of the collectors from the corrosive hydrogen bromide makes for a more manageable system. The spheres generate a trickle current that splits the electrolyte into hydrogen and liquid bromide, which are later recombined in a fuel cell. □

PUMP IMPROVES EFFICIENCIES OF VISIBLE-LIGHT LASERS

Significantly improved visible-light lasers now are in sight. Researchers at the University of Illinois at Urbana have come up with a way to pump a mercury bromide laser that should dramatically improve output efficiencies, says lead researcher J. Gary Eden. The technique could improve efficiencies 5 to 10 times over today's state of the art, he says. In essence, the method strips off one of the bromine atoms from mercury bromide gas molecules by means of a low-power continuous electrical discharge before optical pumping starts. The resulting diatomic vapor can then be made to lase with about 3.5 eV of energy, compared with about 6.4 eV for a conventionally pumped triatomic vapor. The Illinois researchers have already measured output conversion efficiencies of 22% in ultraviolet-to-green lasers. That compares with typical 1% to 2% efficiencies with the conventional approach. □

LARGEST BUSINESS COMPUTER GOES INTO OPERATION THIS FALL

Sometime this fall, the largest computer system ever built for a business application will be up and running at Citibank Corp.'s North East Banking Division headquarters in New York or at its office in Secaucus, N. J. Teradata Corp. built the 168-processor relational-data-base DBC/1012 model 2, which will be used for transaction processing and query applications. The Los Angeles company says its earlier installations average 15 parallel processors. The peak processing speed of the DBC/1012 model 2 will be 170 million instructions per second. The system will include 32 interface processors, to connect it to host computers, and 136 access-module processors, which will manage data on 136 disk drives holding 515 megabytes each. Teradata uses Intel's 80286 microprocessor and the 80287 math coprocessor. □

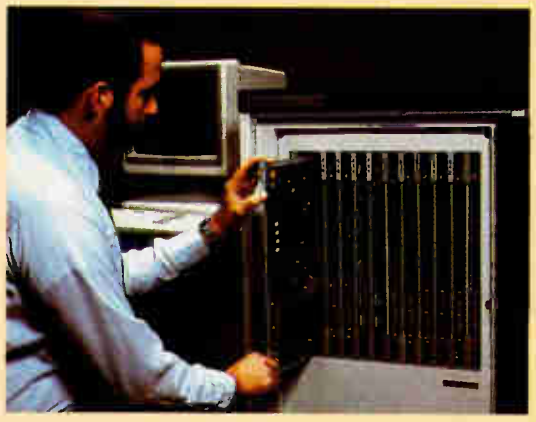
WAFERSCALE STRIKES DEAL WITH RCA/SHARP ON ASICs

Waferscale Integration Inc. is forming an alliance with RCA Corp. and Sharp Corp. to multisource standard-cell libraries. The agreement covers manufacture by RCA of Waferscale's high-speed erasable-programmable read-only memories, 32-bit-slice processors, and peripherals using its 2-μm CMOS process. (Sharp acquired a Waferscale license under an earlier deal.) Waferscale customers will have access to RCA's standard-cell library. The agreement also extends to joint-venture RCA/Sharp Microelectronics Inc., Camas, Wash., which will acquire 7% of Waferscale's outstanding stock. Waferscale, a privately held Fremont, Calif., company, expects the deal will extend to its next-generation 1-μm cell libraries as well. □

Just what the DoD ordered! An embedded, parallel multicomputer with run-time Ada for less than $50,000.

The new Series 600 and 1200 Flex/32 MultiComputers offer system integrators and OEMs the best price/performance available in fifth generation, parallel systems. The Flex/32's concurrent software provides an Ada real-time, run-time environment as well as an Ada development environment. The Series 600 and 1200 come in 21-inch high, standard rack mountable chassis ready for embedding, or in desk-high cabinetry.

And all of this for less than $50,000 in OEM quantities.



The Series 1200 configured with 8 super minicomputers and 33 mb of memory.

APPLICATIONS
Command/Control and Communications
Multi-target Radar/Sonar
Flight/Combat/Weapon Simulation
Test Systems
Signal/Image Processing
Artificial Intelligence/Expert Systems

PARALLEL HARDWARE
Multiple Super Minicomputers
Multiple Memories
Multiple Data Paths
Multiple Instruction Paths
Multiple VMEbus I/O Paths
Multiple Built-In-Test

CONCURRENT SOFTWARE
Ada
ConCurrent C
ConCurrent FORTRAN
UNIX System V
Real-time Operating System
Concurrency Simulator

Flexible Computer Corporation

1801 Royal Lane, Bldg. 8; Dallas, Texas USA 75229; (214) 869-1234; TX: 5106001569

Sales Offices: Philadelphia (215) 648-3916; New York (203) 325-9440; Chicago: (312) 654-1125; Los Angeles (213) 640-3322; San Francisco (415) 593-7044; Washington D.C. (703) 356-8882; Denver (303) 741-3539; Florida (305) 344-0808.

Circle 10 on reader service card

ELECTRONICS NEWSLETTER

PLAYERS IN CDROM MARKET START TEAMING UP

The prospect of a market that could reach $864 million by 1990 has touched off a small flurry of alliances in compact-disk read-only memories. KnowledgeSet Corp. (formerly Activenture Corp.), Monterey, Calif., and Digital Audio Disk Corp., Terre Haute, Ind., a wholly owned subsidiary of Sony Corp. of America, said they will form a joint venture to manufacture finished CDROM disks from customer-supplied raw data. They made their announcement at last week's First International Conference on CDROM, sponsored by Microsoft Corp. In Tokyo, Victor Corp. of Japan announced a similar service that will let software houses use a premastering system it developed with Optical Media International, Aptos, Calif. The software houses will produce formatted videotapes, which JVC then converts to CDROMs. In another joint venture announced at the Seattle conference the giant Italian national telecommunications holding company STET has created a new company with Ing. C. Olivetti & C. to develop telecommunications-related CDROM applications and to distribute them worldwide. □

U.S. AND JAPAN MOVE CLOSER TO AN ANTI-DUMPING PACT

Japanese and U. S. government negotiators need at least one more round of talks—scheduled for Washington late this month—to figure out how to monitor production costs and thus keep track of pricing structures for companies charged with dumping chips on the U. S. market. Negotiators have agreed that action must be taken to stop semiconductor dumping, and after two days of talks in Tokyo last week, a U. S. official said, "We've narrowed our differences." One is how to ensure that the Japanese government will provide production information promptly enough to protect U. S. companies from being "dumped to death," says the official. □

NTT TO BUY IBM AND SPERRY EQUIPMENT

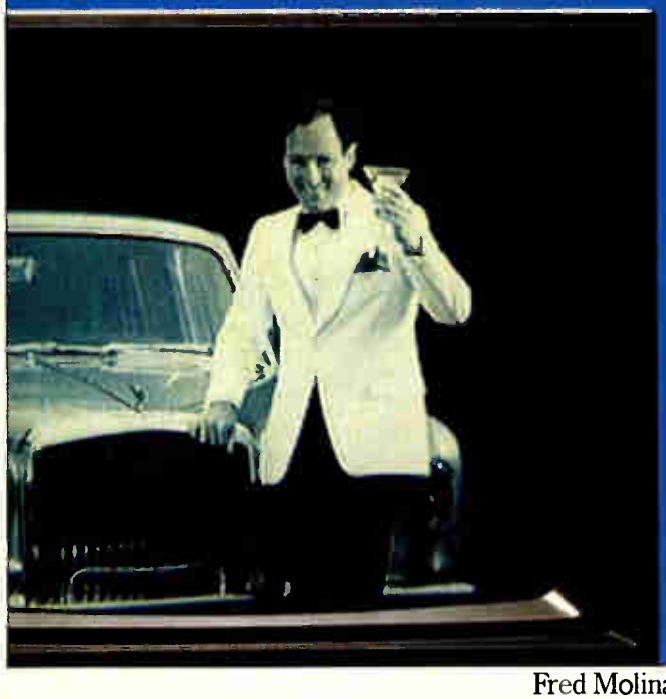
Nippon Telegraph & Telephone Corp., Tokyo, starts its new telegraph system this week with equipment supplied by U. S. companies. NTT had sought vendors with the technical know-how to jointly develop new hardware when it decided to replace its obsolete 25-year-old system. IBM Japan Ltd. provided the Telegram Exchange Automated System and the Display Controller. Nippon Univac Kaisha Ltd., a subsidiary of Sperry Corp., provided the Telegram Entry Equipment. NTT says the new system can stem the telegraph operation's tide of red ink, because the company will abandon its dedicated telegraph-transmission network and use the packet-switching network it has set up for data transmission. □

THE SEMICONDUCTOR OUTLOOK GETS EVEN BRIGHTER

Signs of an upturn for U. S.-based semiconductor houses continue to pop up. Last week, Intel Corp. announced it had raised prices of its erasable programmable read-only memory chips by 25% over November 1985 levels. The Santa Clara, Calif., company's price hike, combined with similar EPROM price increases last fall by Advanced Micro Devices Inc., Sunnyvale, Calif., indicates that demand is picking up. Further evidence that the gloom of several months ago in the chip industry is being swept away comes from previously skeptical James Barlage, financial analyst for Smith Barney Harris & Upham, New York. The veteran analyst, who has covered the semiconductor beat for more than a decade, now sees 1986 moving into plus territory, and says it "marks the beginning of a three-year cycle." Barlage believes that U. S. companies have 10% gains in store for them this year, with 25% increases in the picture for 1987 and 1988. □

Are you spending too much on your image?

Data Translation's IBM PC Image Processing Board, $1495.



The Competition's IBM PC Image Processing Boards, $2500-4500.

Fred Molinari, President

The popular "standard" for video imaging is 512 x 512 x 8 bits.

But ask yourself: do you really need that much resolution? Chances are, you can get excellent results from one of our 256 x 256 x 6 bit real-time processing boards. Which cost considerably less.

These image processors feature high bandwidth, which provides a very sharp image. And our boards give you faster processing too, because the data requirements are reduced.

We could get into short strokes like VCR compatibility, full-functionality-on-one-board, and extensive software support, but we won't waste your time. The issue here is value. We'll deliver excellent results for about half the price.

And if you feel you need 512 x 512 x 8, well, we have that too.

Call (617) 481-3700

IMAGE PROCESSING CHART

256 x 256 x 6 Imaging Boards	Bus	Frame Grab Speed	Software	High Speed Coprocessor Support	Price
DT2803 Image Processor	IBM PC	Real-time	Videolab	Yes	$1,495
DT2603 Image Processor	MicroVAX II	Real-time	Coming soon	Yes	$1,895

FIVE DAY 5 DELIVERY

See our new 646 pg. catalog/handbook or see us in Gold Book 1986. Or call for your personal copy today.

DATA TRANSLATION

World Headquarters: Data Translation, Inc., 100 Locke Dr., Marlboro, MA 01752 (617) 481-3700 Tlx 951 646
European Headquarters: Data Translation, Ltd., 13 The Business Centre, Molly Millars Lane, Wokingham Berks, RG112QZ, England Tlx 851849862 (#D)
International Sales Offices: Australia (61) 2-6635289; Belgium (32) 2-7352135; Canada (416) 625-1907; Chile (2) 2-253689; China (408) 727-8222, (86) 87214017; Denmark (02) 187188; England (44) 0734-793838; Finland (358) 0-372-144; France (33) 146306839; Greece (30) 031-527039, (30) 13-614300. Hong Kong (852) 3-324563; India (91) 2-231040, Israel (972) 3-324298; Italy (39) 2349751; Japan (81) 3-502-5550, (81) 3-348-8301, (81) 3-355-1111; Korea (82) 753-3101; Malaysia (60) 3-36299; Morocco (21) 9-30-6949; Netherlands (31) 70996360; New Zealand (61) 2-663-5289; Norway (47)(02) 559050; Peru (51)(14) 31-8060; Philippines 818-0103, 818-3073, 818-4230; Portugal (351) 1545313; Singapore (65) 271-3163; South Africa (27) 12469221; Spain (34) 14558112; Sweden (46) 87617820; Switzerland (41) 17231410 (41) 22360830; Taiwan (86) 2-721-7864, (86) 2-531-2434; West Germany (49) 89809020.

PRODUCTS NEWSLETTER

HITACHI DRAM CAN CHANGE MEMORY DATA TO VIDEO SIGNALS

Hitachi Ltd.'s multiport 64-K-by-4-bit dynamic RAM for video applications features on-chip serial-access memory and a built-in shift register to provide the conversion to change memory data to video signals. The HM53461's multiport configuration makes it possible for a CPU to rewrite data and simultaneously transfer it to the CRT. The DRAM comes in versions with access times of 100, 120, and 150 ns; the three versions of the on-chip serial-access memory, configured as 256 words by 4 bits, have minimum cycle times of 40, 40, and 60 ns. The HM53461 and the HM53462, which adds graphics processing, will be available in April. In Japan, the HM53461 will cost $4.72 in lots of 1,000 and the HM53462 will cost $5.00. □

SIMULATOR-ANALYZER WILL CHECK MAP NETWORKS

Look for Tekelec Inc. to unveil in May a simulator-analyzer for pinpointing software problems in Manufacturing Automation Protocol networks. The portable instrument initially will perform automatic simulation and conformance tests on the internet and transport protocols of MAP networks. Future developments from the Calabasas, Calif., company will include simulator support for the session and case kernels of the software. The basic unit will sell for $25,000, including software. □

A SAFE WAY TO PROTECT LOW-VOLTAGE DATA LINES

EEV Inc. is bringing the tube surge-arrester technology common in telecommunications to the data lines. Called Alpha, the 90-V gas-discharge tube protects low-voltage data lines from transients caused by lightning, power lines, and static discharge. The hybrid circuits currently used to protect the lines have been known to cause fires, destroying the equipment they are supposed to protect. At about $1 each in large quantities, the Alpha costs less than hybrids. The Elmsford, N.Y., company's three-electrode tube, which works with secondary protection devices, will be available next month. □

APPLIED MATERIALS' AUTOMATED REACTOR CUTS PROCESSING TIME

Applied Materials Inc. is ready to ship an epitaxial reactor that integrates easily into automated wafer-fabrication production lines. The Precision Epi 7010 processes 27 five-in. or 21 six-in. wafers per batch, using only two thirds the cycle time required by previous systems from the company. The key to the system's speed is a dual-susceptor single-chamber design that permits off-line wafer loading and unloading and cassette-to-cassette automation. The Santa Clara, Calif., company's reactor was introduced last week at Semicon Europa in Zurich and costs $1.2 million to $1.5 million. □

BIT-SLICE PROCESSORS GET A HIGH-LEVEL LANGUAGE

Step Engineering, a Sunnyvale, Calif., maker of development systems and software tools, is providing users of bit-slice microprocessors with a high-level language system. Up to now, bit-slice processors have been programmed in assembly language. The MetaStep Language System consists of a definition-processor module to define macroinstructions, constants, and variables; an assembler to build the microprogram from source code and instructions; and a linker/debugger. It accepts Advanced Micro Devices Inc.'s Amdasm source code, a popular microprogramming syntax, as well as its own C-like language. MetaStep is available in versions for two operating systems—AT&T Co.'s Unix and IBM Corp.'s PC-DOS—and for Step's own Step-27 system-development tools. The price for each is $3,000. □

Electronics

NOW A SINGLE CHIP CAN HOLD A REPROGRAMMABLE SYSTEM

ON-CHIP EEPROM CELLS LET AN IC TEST AND REPROGRAM ITSELF

SAN JOSE, CALIF.

The fully self-contained reprogrammable single-chip system is in sight, now that Sierra Semiconductor Corp. has come up with a cell family based on electrically erasable programmable read-only memory. The cells are used, not for bulk memory, but for adjustment and control of on-chip linear and digital cells, and they can be integrated on a chip with Sierra's analog and digital cells.

Distributed across an application-specific integrated circuit, they make possible a whole new class of reprogrammable ASICs—even self-testing and self-adapting chips. Also, such electromechanical parts as switches and potentiometers can be integrated on-chip. Sierra, a three-year-old CMOS specialist, is apparently the first to perfect the tricky process of integrating linear, digital logic, and EEPROM technologies in a single standard-cell chip.

Other companies such as Intel, National Semiconductor, NCR, VLSI Technology, and Xicor are working on EEPROM cell technology, but only NCR is expected to hit the market soon.

The Sierra cells are flip-flops and latches that look to the designer like any other logic cell. They have the same inputs and outputs except for a single lead that distributes the high-voltage programming pulse. The cells mesh with Sierra's standard library, which also includes 33 analog and 237 digital cells. The EEPROM cells allow the others to be programmed by the user.

"As few as 16 bits of E^2 can allow the customer to do a tremendous amount of reconfiguring a digital function," says marketing vice president Tom Reynolds. "These features can be added at final test, or the final user can be allowed to reconfigure a system."

The Sierra cells include a D-type flip-flop, a data latch, a set-reset latch, a high-voltage generator cell (for obtaining an 18-V programming voltage on-chip), and two cells to interface with on- and off-chip programming voltages. When functioning as pots and switches on a board, these cells can trim an on-board operational amplifier's gain, for example, or control an input/output format electronically, just as is done manually with a dual in-line package switch.

Other companies have duplicated discrete components with EEPROMs. One example is Xicor Inc., Milpitas, Calif., with its E^2POT, an IC version of a potentiometer. But the Sierra cells are distributed on the chip itself, physically near the element they control, and so do not require addition of I/O pins for accessing. Xicor has an EEPROM technology agreement with Intel Corp., Santa Clara, Calif., which is also believed to be working on EEPROM cells, though Intel will not comment on them.

NCR Corp.'s Microelectronics Division, Miamisburg, Ohio, is expected to enter its EEPROM cell candidates next month: 256-bit arrays that can be used to design personalized systems. NCR sees applications in encryption as well as controls.

MANY USES. National Semiconductor Corp., Santa Clara, has rights to the Sierra integrated EEPROM technology, and is looking at adding EEPROM modules to many devices, according to Jim Owens, vice president of technology at National. The company's work in this area entails possible use of the technology as well as developments from National's memory group. Owens says EEPROM devices will probably first be added to microprocessors for programmable microcontrollers, and he cites possible use in programmable logic arrays, telecommunications circuits, smart cards, analog-to-digital converters, and voltage regulators.

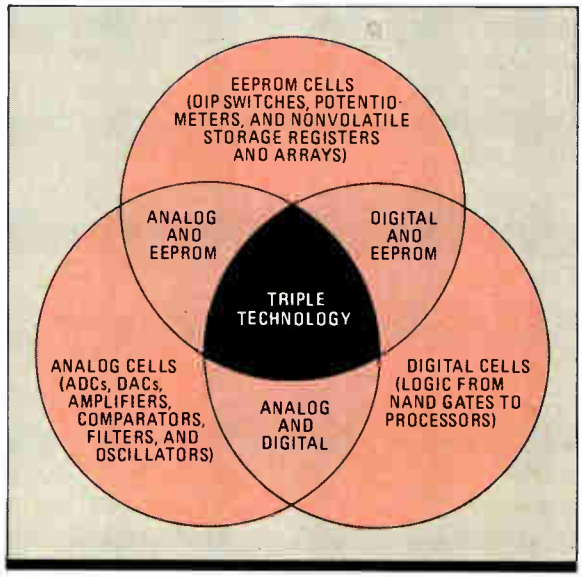
VLSI Technology Inc., San Jose, has a technology agreement with Sierra (swapping VTI's digital technology for Sierra's linear), and it plans to make EEPROM cells. VTI acquired Sierra's design tools, which run on the Digital Equipment Corp. VAX, the Elxsi 6400, and Apollo Computer Inc. work stations. But the agreement with Sierra does not cover EEPROM, and VTI will not announce its own products this year.

Sierra's CMOS process was designed from the ground up to be compatible with linear, digital logic, and memory circuits. Usually, the three different circuit types use different processes.

Sierra's basic process is 2-μm n-well CMOS, with a single layer of polysilicon and up to two layers of metal. A second layer of poly is used in analog cells. The EEPROM technology is an additional module, and the EEPROM cells are ruggedized by a patented Sierra design so that they can be placed anywhere on the chip and be immune to the various types of signals coming from their neighbors.

The 1-bit EEPROM is the most flexible of the new Sierra cells, but the least efficient in terms of space; cells are 500 μm wide by 72 μm high. Sierra is also designing byte-wide on-chip EEPROMs and small one- and two-dimensional arrays that double and quadruple the efficiency, says design vice president Andrew G. Varadi.

Uses for the new cells, Reynolds says, include ASIC DACs, smart telecommunications chips, power-failure detectors, oscillators, and applications that let users program supervisory functions. *–Clifford Barney and Eve Bennett*



TRIPLE. Sierra cell library integrates three key technologies.

IS E-BEAM LITHOGRAPHY FINALLY READY?

HAYWARD, CALIF.

Electron-beam technology appears ready to move into the commercial marketplace, thanks to a boost from the Very High-Speed Integrated Circuits program. Perkin-Elmer Corp. is promising to ship a working production unit this month, with a second to follow in two weeks. It says it has overcome the defects and delays that have plagued the prototype system, which can directly write circuit features as small as 0.5 μm.

The Aeble 150 may have a bright commercial future because of its high wafer throughput. Perkin-Elmer specifies the machine at up to 12 six-in. wafers or up to 20 four-in. wafers per hour. High throughput is critical for e-beam processing, says consultant Dan Hutcheson of VLSI Research Inc., San Jose, Calif., because 20 wafers/h is the point at which e-beam technology becomes cost-competitive with optical steppers.

"If Perkin-Elmer can build [the Aeble 150], they have a ready-made market for it," Hutcheson says. "E-beam could be a major revolution in lithography for the application-specific market. For the first time, users will be able to do on-the-fly customization of wafers at reasonable cost without having to go to a reticle."

The first two Aeble 150s will be used to build chips in the Defense Department's VHSIC program. TRW Inc. has ordered one. The prototype will remain at Perkin-Elmer's Electron Beam Technology Division in Hayward, but will eventually be delivered to Hughes Research Laboratory, Malibu, Calif., also for VHSIC applications.

Building the Aeble 150 has been no cinch. Direct-write e-beam technology has a reputation as one of the toughest and costliest to implement in electronics. It combines five exotic technologies—laser optics, high-precision measurement, vacuum technology, electron optics, and sophisticated computer control.

Although the Perkin-Elmer prototype has been in use for over a year, the production version has been delayed by software problems and the reported inability of the prototype to meet specifications at the high throughput rate. The software problems have been "substantially resolved," according to Harold Borkan, deputy director of the Electronic Technology and Devices Laboratory, the lead Army lab for VHSIC.

At 20 wafers an hour, e-beam systems can compete with steppers

But Perkin-Elmer's real difficulty, outside sources say, was in obtaining the proper acuity of lines and registration of patterns on the wafer. This problem affects the ability of digital-to-analog converters to steer the beam properly and get it to settle on one spot.

VULNERABLE. The Aeble 150 is particularly sensitive to such problems because it uses a shaped beam, so it can write triangles and squares directly, and uses a write-on-the-fly technique in which the beam's motion is correlated with the continuous motion of the stage carrying the wafers.

Performance problems with Hughes Aircraft's prototype could be traced to contamination in both building and using the equipment, says Charles Biechler, general manager of Perkin-Elmer's Electron Beam Division. "It has not been in a clean environment," he says. "In fact, even to give it a class 10,000 label is probably a euphemism. There have been Hughes and Perkin-Elmer engineers crawling all over it."

Contamination causes a charging of the electron beam so that it tends to wander. The production machine, adds Biechler, was built and maintained in a clean room rated better than class 100.

Perkin-Elmer's delivery promises are raising skepticism in some quarters—TRW does not expect to receive its Aeble 150 until April 28. However, Biechler maintains that Perkin-Elmer has overcome its production difficulties, and that not only can it meet specifications at a high throughput, it can beat them. "This is going to be a super machine—performing consistently at 0.5-μm and even 0.25-μm geometries."

The equipment isn't cheap—a production model costs about $3 million, more than three times as much as optical steppers. Still, Perkin-Elmer expects to sell a number of Aeble 150s in the commercial market. European Silicon Structures, a consortium of six European companies with some outside venture capital, has announced its intention of buying 10 e-beam machines, some of them Aeble 150s. Another machine is reportedly slated for a Japanese customer. "We continue to book orders at a satisfactory rate," Perkin-Elmer told its stockholders on Jan. 31.

By awarding a VHSIC contract for a 0.5-μm optical stepper to GCA Corp. of Burlington, Mass., last fall, the DOD en-

READY TO ROLL. Perkin-Elmer plans to ship this month the first high-throughput Aeble 150 electron-beam system for 0.5-μm work.

couraged speculation that it was straying from its five-year dedication to e-beam technology for VHSIC. The optical stepper could be used for high-volume production of chips developed on e-beam systems.

But the ETD Lab's Borkan denies that there was any conflict within the DOD with respect to e-beam technology. "The VHSIC program is supporting three types of lithography equipment—electron-beam, optical, and X-ray," he says. "Electron beam has the highest resolution but is slowest in terms of wafers-per-hour throughput." As for the GCA contract, he adds, "one cannot predict whether the optical approach can do the entire lithography required for 0.5-μm devices, or if it will be used in a mix-and-match mode." *–Clifford Barney*

MILITARY

MISSILE TEARDOWN AT TI STIRS SERVICE SQUABBLE

CRACKS. Soldering "nonconformances" temporarily halted HARM acceptance.

LEWISVILLE, TEXAS

The HARM missile is caught in a Washington dispute over the Navy's mild reaction to a report detailing defects in a missile built by a Texas Instruments Inc. plant in Lewisville. Miffed HARM backers complain politics and program sniping within the armed services are behind the dispute.

The squabble stems from a February teardown of a HARM (high-speed antiradiation missile) by inspectors working for the Navy. The inspectors reported 881 minor defects and 28 more serious flaws in the guidance and control sections of a missile Most of the flaws were in solder joints.

TI, sole supplier of the $300,000 radar-seeking missile, insists the anomalies and defects pose no long-term danger to HARM's reliability. In Washington, Navy officials defended HARM's brief track record and the decision to keep missiles in production last month despite the long list of deficiencies. They say that the teardown uncovered no critical mission-threatening defects.

OFF GUARD. The unexpected disclosure of the audit during a late-February House defense-appropriations subcommittee hearing angered TI officials in Dallas and caught some Navy program managers off guard. Most believe the report was blown out of proportion. Just how the subcommittee got a copy of the report has not been made public.

Some officials in the Pentagon and in the defense industry suggest that 909 reported deficiencies merit stronger action by the government, which has shut down contractor factories for far fewer infractions. The incident has rekindled debate on inconsistencies in weapons inspections and crackdowns on defense contractors.

In 1984, Hughes Aircraft Co.'s Phoenix missile facility in Tucson, Ariz., was shut down after defects were found during an inspection. "When the Air Force inspected the Phoenix we found 68 defects, and that closed Hughes down. We should be more consistent, at least," says Thomas S. Amlie, assistant for technical systems in the Air Force office of financial management in Washington.

Willis Willoughby, the Navy's executive director of reliability, maintainability, and quality assurance, says he has reviewed the findings of the teardown and believes "they weren't problems of any magnitude. It is overreaction." Willoughby has supervised previous audits of missile systems.

Plants have been shut down for far fewer infractions

For the record, Navy officials decline to comment on alleged infighting. They have issued a statement acknowledging that the inspectors did record a large number of apparent "nonconformances" to MIL STD WS6536. Cited discrepancies included more than two dozen termed major, meaning those that may have "some potential to affect long-term reliability of the missile."

Much of the problem with inspecting solder defects is determining whether anomalies are meaningful, says William B. Mitchell, president of TI's Defense Systems & Electronics Group, which builds HARM. "If anyone tears something down and you have 15 or 20 people looking at stuff under 10-power microscopes, you are going to see something that you judgmentally think should look different. The color might be different than you are used to seeing or the lead is crimped differently."

In the teardown, defects were listed as surface cracks on solder joints and nicks or scrapes on components, say Navy officials, who received the audit report from certified inspectors at TI's plant. HARM is TI's biggest weapon contract, accounting for roughly 10% of its total defense equipment sales, and Pentagon officials say the missile could have a lifetime value of more than $5 billion.

ON TARGET. The Navy emphasizes the TI-built missile has had higher-than-specified reliability in captive flight (under the wing of an aircraft). Since last May, all 12 test firings of the HARM have been successful. To reach this level of reliability, software deficiencies were corrected, the missile's radar-tracking abilities were expanded, and its trajectories reshaped. HARM operates by locking onto enemy radar emissions and is aimed primarily at attacking surface-to-air weapon systems.

HARM's guidance-and-control system contains some 42,000 solder joints and connections. The 881 minor discrepancies fell into 17 categories of nonconformances and anomalies considered unlikely to impair long-term reliability. The minor flaws were "indications of the need for process improvement," says the Navy Air Systems Command (Navair), which oversees the HARM program.

While assembly continued last month, the Navy halted acceptance of HARM systems for about three weeks in order to reach an agreement with TI to add new quality-control steps. The Navy also plans to perform more environmental tests before deploying the weapons.

TI quickly agreed to extend its three-year warranty to cover missiles built with 1984 appropriations but not previously included under a two-year-old extensive weapons guarantee. (TI has pushed down the price of the missile from $589,000 in 1982; fiscal 1986 purchases will be for $266,000.) The Navy's request for an extended warranty is "a very measured response to our contractor that it has to do better," says Capt. Larry E. Kaufman, Navy HARM program manager.

The Navy emphasizes the February audit is still in progress and a final re-

port won't be ready until the end of March. The number of discrepancies could drop. Meanwhile, the Navy is withholding payments of $50,000 per missile until environmental tests are complete.

At least one action planned by TI to ensure greater soldering reliability is certification and increased use of a new infrared-laser inspection system, which quickly detects faulty connections by tracking thermal signatures of cooling joints. The system is made by Vanzetti Systems Inc., Stoughton, Mass.

One move the Navy might make would end TI's monopoly on HARM's guidance-and-control system, which represents about 48% of the missile's cost. The Navy is thinking of replacing the HARM's system in 1990 with one that will have multiple sources—the low-cost Seeker guidance-and-control system. Ford Aerospace & Communications Corp. and Raytheon Co. hold development contracts for the new Seeker system. *–J. Robert Lineback and George Leopold*

RESEARCH

BUDGET FIGHT THREATENS R&D FUNDING

WASHINGTON

Government and university officials see bleak prospects for research and development, despite the Reagan administration's proposed 17% increase for R&D to $61 billion in fiscal 1987. More than half of that total would go to electronics R&D. The officials fear that the pressure of possible mandatory cuts under the Gramm-Rudman deficit-reduction act could force the R&D proposal into a game of "budget chicken" between the administration and Congress. The result could be a substantial cutback in funds, many observers feel.

President Reagan considers the R&D budget a high priority and will support new starts across the board, says John P. McTague, acting White House science adviser, who appeared at an R&D budget briefing sponsored by the Institute of Electrical and Electronics Engineers in late February. This year's R&D request includes increases for the Department of Defense, the National Aeronautics and Space Administration, and the National Science Foundation. The Pentagon will start a program to develop gallium arsenide integrated circuits, and the NSF plans to establish a new computer directorate within a few months.

DOD's shielding of SDI hurt other research

R&D RISE. Most researchers, however, discount the chance of a budget hike. In fact, they think when the ax starts chopping, basic research will be the first to go. Yet McTague maintains that research is second only to general defense funding as the fastest growing budget component, and says that funding has swung more heavily toward basic research in recent years. He acknowledges that basic-research funds to universities, which were cut for fiscal 1986 under Gramm-Rudman, would not have been cut by the administration and were victims of a "mindless process."

Other government officials at the briefing were less optimistic. Joel Snow, director of the Energy Department's Office of Energy Research, says the likelihood that the budget will emerge from Congress looking anything like the administration's original proposal is the lowest in his 20 years in Washington.

In figures supplied by the Office of Management and Budget, $42 billion of the proposed $61 billion for R&D comes from a Pentagon request for research, development, testing, and evaluation funding. That figure includes funds for the Strategic Defense Initiative, and only the research segment of SDI has dropped in fiscal 1987—from just over $1 billion to $986 million. Congress has criticized the Pentagon budget proposal for failing to recognize the limitations imposed by the specter of Gramm-Rudman cuts [*Electronics*, Feb. 10, 1986, p. 42].

Gramm-Rudman cuts lopped $3 million from Pentagon R&D in fiscal 1986, says Donald I. Carter, deputy under secretary of defense for research and advanced technology. Because the Pentagon chose to shield SDI from budget cuts, other research suffered. Most notable is the Defense Advanced Research Projects Agency, which took about a 10% reduction, rather than the Gramm-Rudman basic across-the-board cut of 4.9%. Carter acknowledged under questioning that Darpa sustained a double whammy, but says the DOD will try to recover that loss this time around.

A large increase in confidential, or "black budget," items during the Reagan years has made it more difficult to discern trends in Pentagon R&D. A recent *National Journal* magazine study estimates that 11.5% of the current Pentagon R&D budget is classified.

The Very High Speed Integrated Circuits program will take a 34.2% cut, to $132 million, in budget authority next year as the Pentagon seeks "about $150 million and probably more" for the GaAs analog ICs through its Microwave/Millimeter-Wave Monolithic Integrated Circuits [Mimic] effort. Deputy under secretary Carter calls the Mimic program "the eyes and ears" of next-generation weapon systems, with specifications comparable to submicron VHSIC chips.

NSF INCREASE. Elsewhere, the NSF will devote more funding to computing programs if it gets the $1.5 billion requested for 1987. Its fiscal 1986 funds were $1.3 billion before the 4.9% Gramm-Rudman cut. The funding request for the NSF's Advanced Scientific Computing program jumped from $45 million last year to just under $54 million, says Carl W. Hall, deputy assistant director for engineering. The computer directorate, which will be separate from the advanced computing group and absorb NSF's computer engineering group, will cost about $100 million, says Hall.

NASA, which will probably submit supplemental 1986 and 1987 requests to account for the loss of the space shuttle Challenger, still looks to spend $410 million on the second phase of space station development. Moreover, the embattled agency is now seeking space station contributions from the European Communities, the European Space Agency, and the Japanese and Canadian governments, adds Dudley G. McConnell, deputy associate administrator

FEDERAL R&D SPENDING TO GROW IN THE MILITARY SECTOR

Department	Fiscal 1986	Fiscal 1987
Defense-military functions	33,485*	41,823*
Department of Energy	4,785	4,886
NASA	3,594	4,051
National Science Foundation	1,334	1,508
Transportation	364	277
Commerce	380	297
Other	8,084	7,961
Total	52,026	60,803

*Obligation estimates in $ millions

SOURCE: U.S. OFFICE OF MANAGEMENT AND BUDGET

WE COULD HAVE CALLED IT A **32-BIT MICROPROCESSOR.**

WE COULD HAVE CALLED IT A **10-MIP COMPUTING ELEMENT.**

WE COULD HAVE CALLED IT THE FIRST **CONCURRENT SOLUTION.**

INSTEAD WE CALL IT THE **TRANSPUTER.**

INMOS introduces the transputer family. A range of evaluation boards for the first transputers is available now.

The transputer is a fast, easy to use VLSI component designed for applications ranging from single microprocessor systems to supercomputers.

The IMS T414 is the first transputer, integrating a 32 bit microprocessor, four inter-transputer communication links, 2 Kbytes of RAM, a 32 bit memory interface and a memory controller onto a CMOS chip.

The microprocessor runs at 10 MIPS and is designed specifically for the execution of high level languages. It combines direct support for multi-tasking, floating point, block transfer and record handling with sub-microsecond procedure call and task switching.

Each transputer link provides a full duplex, 10 Mbits/sec, point to point connection with an on chip DMA controller. Links are used for inter-transputer communication or, via an INMOS Link Adaptor, interfacing to industry standard byte wide peripherals.

The memory interface provides access to a linear 4 Gbyte address space at a data transfer rate of up to 25 Mbytes/sec.

Transputers are designed for ease of engineering. All transputer family devices operate from a single 5 MHz clock input, which is used to derive high speed internal clocks for all on chip systems.

When transputers are directly connected via links, additional components are not necessary. Independent or common clocking can be used, regardless of timing skew.

The configurable memory controller also requires no external components. It provides all the necessary timing and refresh signals for memory systems, comprising any mix of ROM, SRAM, DRAM and memory mapped peripherals.

Transputers are designed for ease of programming. INMOS offers development systems which provide integrated editing, compiling and source level debugging for both single and multiple transputer applications, using C, Pascal, Fortran and occam.

In applications requiring only a single computing element, the transputer's speed, minimal support component requirements and programming efficiency provide significant cost/performance advantages over conventional microprocessors.

Systems of any size can be built from interconnected transputers, using the links. The same program can be configured to run on one, tens or thousands of transputers allowing a simple trade off between performance and cost.

The transputer family already includes 32 bit and 16 bit transputers, peripheral controllers, evaluation boards and development tools. Start assessing its capability for yourself now with an IMS T414 evaluation board.

TRANSPUTER PRODUCTS	
IMS T414	**32 Bit, 2 Kbyte RAM, 4 Transputer links**
IMS T212	**16 Bit, 2 Kbyte RAM, 4 Transputer links**
IMS C001	Transputer Link Adaptor, Separate 8-Bit input and output
IMS C002	Transputer Link Adaptor, Multiplexed 8-Bit input/output

DEVELOPMENT TOOLS	
IMS D100	INMOS Transputer Development System
IMS D600	Transputer Development Software, VAX-VMS
IMS D700	Transputer Development Software, IBM-PC

EVALUATION BOARDS	
IMS B001	Double Eurocard, IMS T414, 64 Kbyte RAM, 2 x RS232C ports
IMS B002	Double Eurocard, IMS T414, 2 Mbyte RAM, 2 x RS232C ports
IMS B004	IBM-PC add on card, IMS T414, 1 Mbyte RAM

INMOS Corporation, P.O. Box 16000, Colorado Springs, Colorado 80935, USA. Tel: (303) 630-4000 Tx: (910) 920-4904
INMOS Limited, Whitefriars, Lewins Mead, Bristol. U.K. BS1 2NP
Tel: 0272 290861 Tx: 444723.
INMOS GmbH, Danziger Strasse 2, 8057 Eching, West Germany.
Tel: 089 319 10 28 Tx: 522645.
INMOS Sarl, Immeuble Monaco, 7 Rue Le Corbusier, Silic 219, 94518 Rungis Cedex, France. Tel: (1) 687.22.01. Tx: 201 222.

For a complete data pack on the Transputer and its support products, fill in the response coupon, and post to INMOS Corporation P.O. Box 16000 Colorado Springs, Colorado 80935, USA.
For faster response, call (303) 630-4000

Name _____

Title _____

Company _____

Street/PO address _____

_____

City/State/Zip _____

Country _____

Telephone _____

☐ Please send Transputer data pack
☐ Please have a salesman call
☐ I am interested in ordering an Evaluation Board

inmos®

TRANSPUTER FAMILY

for space and science applications.

Fiscal 1986 R&D for NASA calls for $3.6 billion, and the 1987 proposal earmarks just over $4 billion. McConnell says NASA will give priority to presidential initiatives, such as the space station, over more commercial uses, such as satellite launchings.

Research officials, meanwhile, wonder how to generate congressional support for the proposed R&D increases. Administration science adviser McTague urges them to promote basic research as a "generic activity, not just single projects," while emphasizing the short-term payoffs of research. *–George Leopold*

PACKAGING

A LASER PACKAGE BREAKS AWAY FROM THE CROWD

MURRAY HILL, N. J.

Packaging is usually one of the more mundane features of high-speed laser devices, but as the song from *Porgy and Bess* goes, "it ain't necessarily so." AT&T Co.'s new Astrotec line of lasers comes in a 12-pin multilayer ceramic package that helps the laser run faster than it can in the usual metal packages.

Multiple layers of patterned metal sandwiched between ceramic layers form the connections inside the package. These patterned-metal connections can be made with very low impedance to bring microwave-frequency signals to the indium gallium arsenide lasers, which run at up to 1.7 Gb/s.

"We had to make an optical coupling and a microwave coupling to the laser at the same time," says Alfred Zacharias, supervisor of device packaging at the Lightwave Devices Laboratory at AT&T's Bell Laboratories. That, he maintains, had never been done before.

Lasers are typically housed in metal packages, in part because the metal acts as a heat sink, helping to diffuse the heat generated by the laser. But to achieve data rates up to 1.7 Gb/s, researchers at Bell Labs had to change their thinking. "We tried," says Zacharias, recalling attempts to use the older packages. "But we don't think it's possible to build a standard package [of this type] for a communication system."

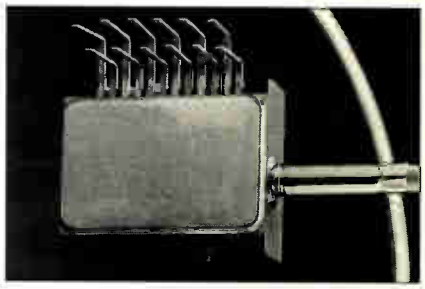
PATTERNED LAYERS. Instead, Zacharias and others looked to the ceramic packages used in high-speed microwave devices. "The multilayer ceramic package allows you to intersperse layers of metal with ceramic using high-temperature bonding techniques," says Richard Dickson, director of the Lightwave Device Laboratory. "The metal layers can be patterned." Within the package, the laser is wire-bonded to the metal layers within the ceramic shell.

A shielded strip transmission line, or strip line, is built into the package. The line, says Zacharias, "allows us to control the impedance in the leads," which makes for better transmission at high rates. The package's terminated lines establish an impedance match between the laser and the high-speed data terminal to which it is connected. "The biggest advantage is at high frequencies, where the impedance of the leads is most important," Dickson says.

By using multilayer ceramics, AT&T was able to eliminate the glass-to-metal seals around the leads used to hermetically seal standard metal packages. In the Astrotec packages, Zacharias says, "the leads that come through the package walls are part of the ceramic itself," so there is no need for an extra seal.

He denies that a ceramic substrate is hard to cool; he says that the alumina ceramic material in the package is no worse a conductor of heat than the alloy Kovar, the most common laser packaging material. To cool the Astrotec devices, AT&T built a thermoelectric cooler into the package to keep the laser from overheating, which is standard procedure. A copper-tungsten plate with an expansion coefficient identical to that of the ceramic shell was also added to the back of the package to radiate heat.

Dickson does not know why multilayer ceramic technology has not been used before; it has been available for some time. "The reasons may be relatively mundane," he says. "Metal packages are easier to machine. But once the technology is stabilized, the cost advantage of the ceramic package will become more evident. Ceramic is typically less expensive than the analogous metal package." *–Tobias Naegele*



MATCHED. Laser package brings the signal in on a low-impedance transmission line.

COMPANIES

NOW BELGIUM HAS ITS OWN PLAYER IN THE IC GAME

OUDENAARDE, BELGIUM

Belgium at last has a native integrated-circuit maker. The startup, called Mietec, owes its existence in part to the government's desire to end total dependence on imports to satisfy the semiconductor needs of its electronic equipment manufacturers. Mietec is no mere token entry in the European IC market. Just now ramping up to full production in Oudenaarde, it churns out chips in five different technologies at a collective rate of 1,000 wafers per week. The startup already has the equipment to more than double that figure and could triple it to some 150,000 wafers per year by adding more gear in its spacious factory.

WHISTLE CLEAN. Critical fab operations, such as photolithography, are carried out in Mietec's class 10 clean room.

Mietec was cofounded by the GIMV, a venture- and development-capital company owned by the state of Flanders, and ITT Corp.'s Belgian subsidiary, Bell Telephone Manufacturing Co. (BTM). The two own, respectively, 49% and 49.5% of the company's equity. The remaining 1.5% is held by bank-

"In ASIC, the customer has to be more than a job number."

"What do application specific IC (ASIC) users need? We've been answering that question for 20 years and three basic beliefs hold fast.

One, no single ASIC option is optimal for every circuit. So we developed them all—gate arrays, standard cells, and cell-based custom.

Two, we can't expect customers to adapt to us. So we assembled the most flexible design interfaces in ASIC. Including gate array and cell libraries for workstations, PC-based systems and most others.

Finally, to keep customers ahead, we must be a leader in design technology. Our cell-compilation work is the natural next step.

Keeping pace with change is one of the hardest skills to learn. Gould AMI is leading the pack. Our customers have the advantage."

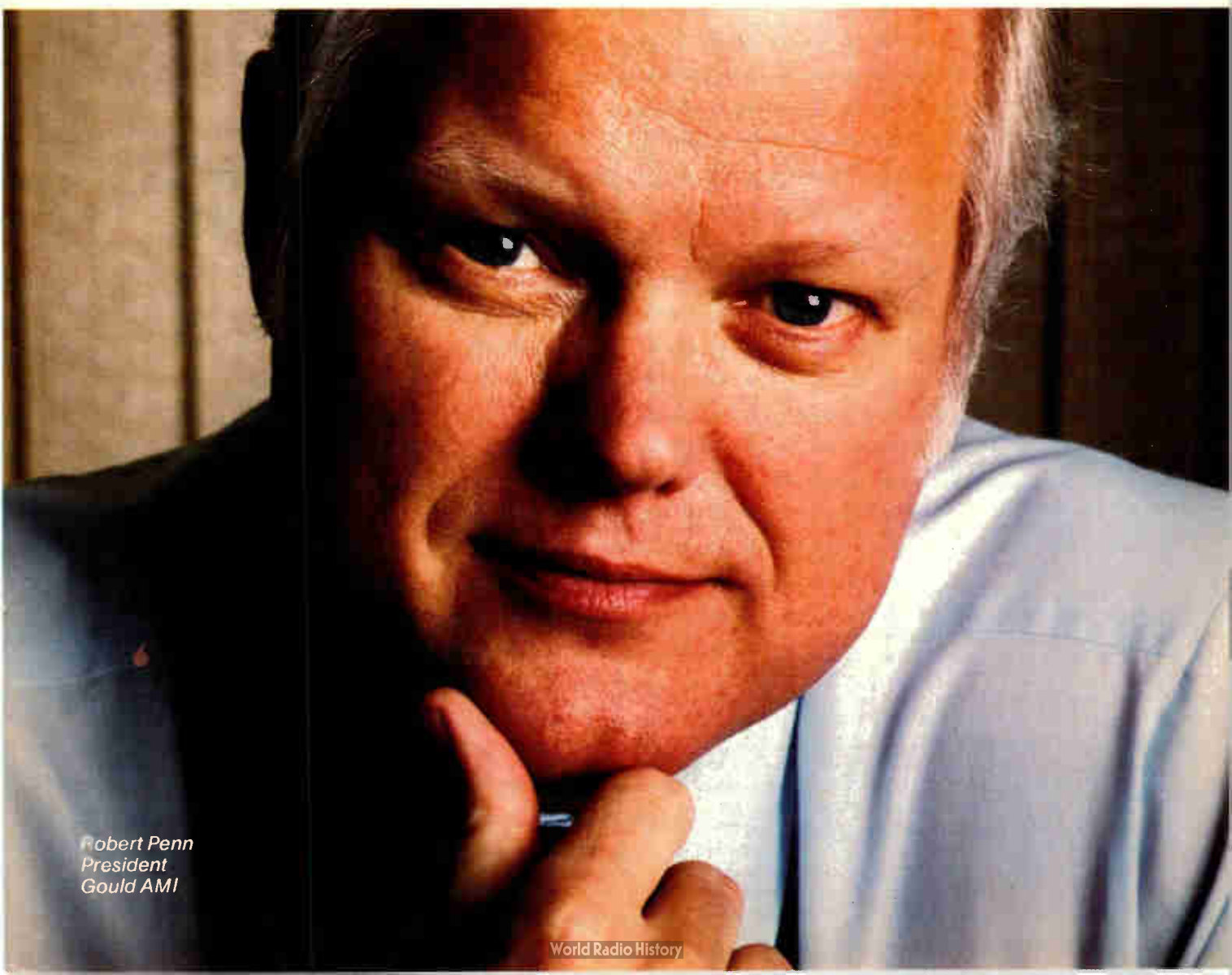
To optimize your ASICs, call us at 408-554-2311. Gould Inc., Semiconductor Division, manufacturer of Gould AMI semiconductors.

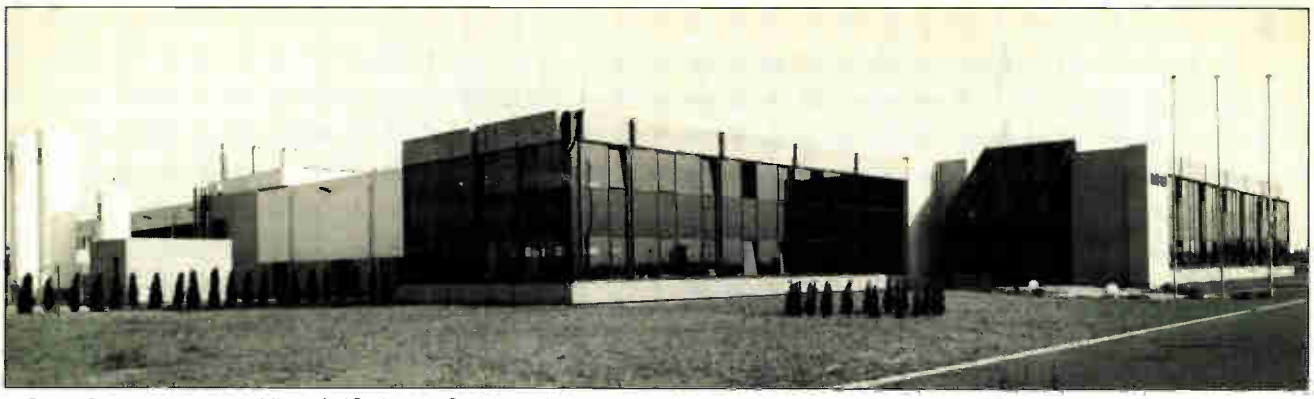
Gould AMI ASIC: Depend on it.

High Performance Solutions in Factory Automation, Computers, Instrumentation, Defense and Semiconductors.

Circle 21 on reader service card

GOULD
Electronics





HIGH TECH IN FLANDERS. Mietec's IC plant at Oudenaarde currently turns out 1,000 wafers a week in a mix of five different technologies.

ing interests. The company is part of a broader microelectronics initiative fostered by the Flanders government. That plan already has produced a world-class research laboratory in Leuven called IMEC, for Interuniversity Microelectronic Center, a spin-off of the Katholieke Universiteit Leuven's electrical engineering department [*Electronics Week*, Oct. 1, 1984, p. 18].

The government chose not to fund Mietec, as it did IMEC. Given the realities of the merchant semiconductor business, it believed, the IC startup would need the firm support of an equipment manufacturer that would also be a major customer, principally at the outset. That necessity meshed perfectly with BTM's need for a reliable source of the proprietary ICs used in its telecommunications systems.

Most of Mietec's production, therefore, is for BTM, but managing director Jean-Pierre Liebaut makes no apologies for that situation. He reasons that BTM and its orders not only give his company the initial volume needed to get production off the starting block, but also offers Mietec a strategic opportunity unusual for any startup.

"From BTM, we've inherited a remarkable library of analog cells, and that will be one of the key points of Mietec's success," he says. "Our strategy is to serve the market for application-specific ICs, but particularly for those applications, like telecommunications, where analog processing or an analog interface is necessary. There aren't enough IC manufacturers who are aware that the world is not digital."

To serve the analog market, Mietec has an impressive array of tools. Its current production, for example, is distributed across five different IC technologies: 5- and 3-μm n-MOS; 3-μm CMOS with three interconnection layers, one metal and two polysilicon; dielectric-isolation high-voltage MOS that can withstand up to 400 V; and 8-μm BiMOS integrating both bipolar and MOS transistors on the same substrate.

BTM developed the first four processes at its pilot line in Antwerp, which was shut down in favor of Mietec's production. The last comes from a technology-exchange accord with Sprague Electric Co., Lexington, Mass. In return, Sprague probably will get access to Mietec's high-voltage MOS technology. The two companies' versions of bipolar-MOS processes are compatible, giving each a valuable second source in the ASIC market.

Mietec's state-of-the-art fabrication lines—including a class 10 clean room—spread over an 80,000-meter^2 area. Production is oriented toward 4-in. wafers, but all equipment is compatible with 5-in. wafers. The company has more than 300 employees.

One of the company's first strategies will be to loosen its dependence on BTM. Liebaut figures that by 1988, the parent company's share of Mietec's production will be down to no more than 25%. That is also the year in which Mietec will move into the black, he projects.

Meanwhile, Mietec is working at full speed on developing proprietary computer-aided design tools based on BTM's analog cells as well as cells developed in-house. It will then distribute the CAD tools to its design centers as well as put them directly into the hands of its best customers. *–Robert T. Gallagher*

MATERIALS

U.S. SEEKS OWN SOURCE OF ULTRAPURE SILICON

PITTSBURGH

Westinghouse Electric Corp. is moving to fill what many believe to be a serious gap in U.S. silicon technology. It is developing production capability for ultrapure, 5-in.-diameter crystals grown by the floating-zone technique that significantly reduces the number of contaminating oxygen atoms.

The Westinghouse effort could be strategically critical to the U.S., and it's being encouraged by the Department of Defense. The company says it has already spent $2 million of its own money and now hopes to attract nearly $5 million from the DOD and others.

The technology is not new, but it is expensive, and so the only U.S. maker of the ultrapure silicon got out of the business in mid-1984. Only three companies—two in Japan and one in West Germany—now produce the material.

The DOD relies on floating-zone silicon for use in not only infrared detectors but also power devices for electromagnetic weapons launchers and other gear. What's more, the high-voltage blocking and current-switching capabilities of devices built on large-diameter floating-zone wafers may be necessary in directed-energy weapons planned for the Strategic Defense Initiative, says Noel Thomas, manager of materials growth and device technology at the Westinghouse Research & Development Center. With power devices, larger-diameter floating-zone wafers translate directly to an ability to build higher-current devices, he notes. "We're looking for high purity and high uniformity."

Unlike conventional Czochralski silicon-growth methods, in which the crystal is pulled from a silicon melt contained in a quartz crucible, floating-zone technology relies on a containerless approach. A polysilicon rod is fused with a single crystalline seed and is then moved progressively through a heated coil, which creates a molten zone that is held in place by surface tension and converted into single-crystal material.

PURER. Though more difficult and costly than the Czochralski technique, the floating-zone method eliminates the crucible that adds to oxygen contamination in Czochralski-grown silicon, says Thomas. The oxygen-atom count typically is 10^{18}/cm^3 in conventional Czochralski-grown

"Why compromise in ASIC, when you don't have to?"

"Don't let anyone tell you an ASIC is an ASIC is an ASIC.

If that were true, you'd only need one choice of application specific ICs. But an ASIC solution is more than a gate array. Or a standard cell. Or a cell-based custom circuit. These are simply different approaches to your system solution.

Time-to-market, development cost and performance needs make every application unique. So no single ASIC option can work best every time.

There's no problem, though, unless your vendor offers just one basic ASIC option. You'll get an ASIC design all right, but odds are it won't be the optimal one.

At Gould AMI, you don't have to compromise. We offer the complete continuum of ASIC options. I know some vendors make you do ASIC their way. It's just not our way."

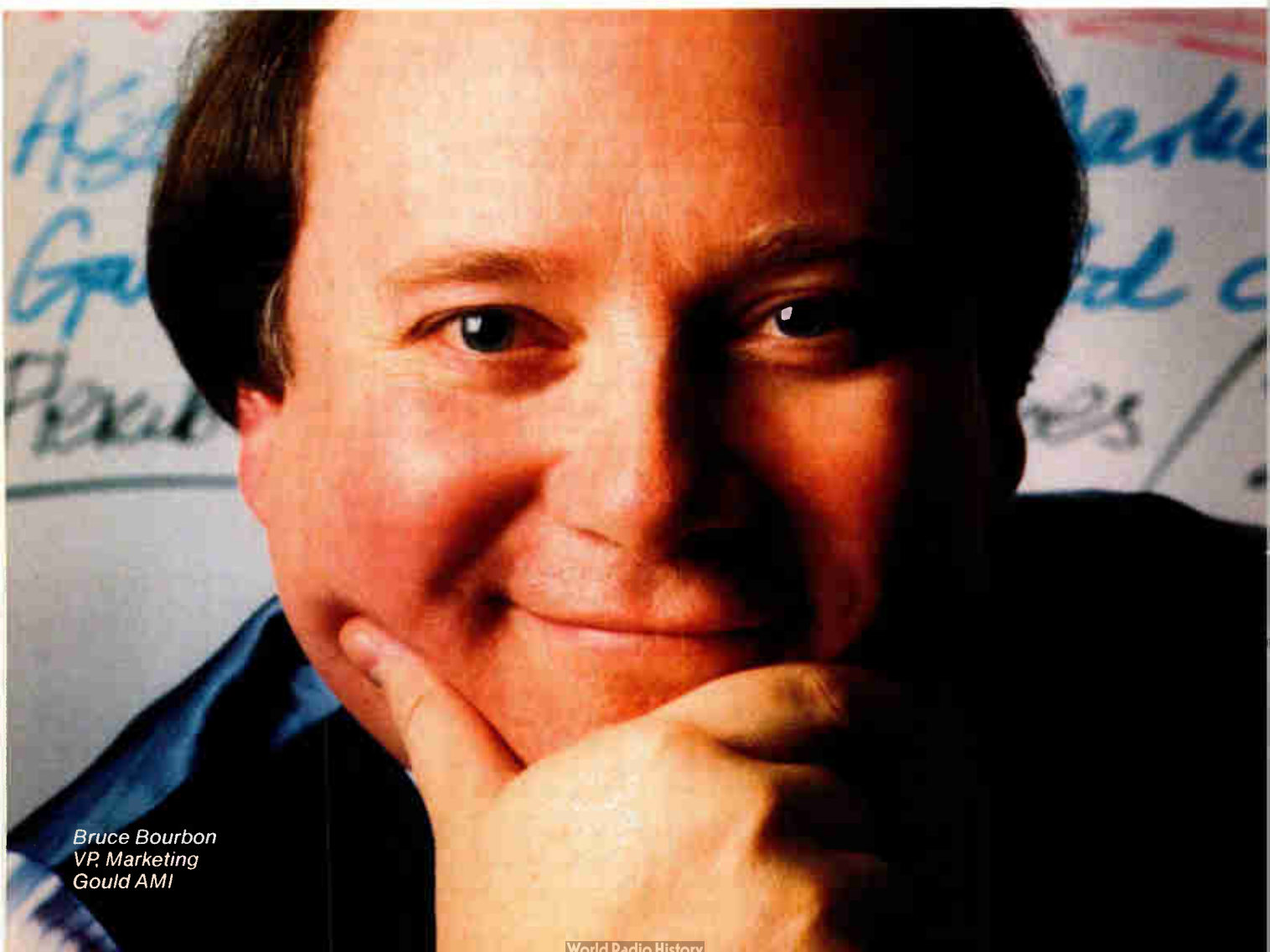
To optimize your ASICs, call us at 408-554-2311. Gould Inc., Semiconductor Division, manufacturer of Gould AMI semiconductors.

Gould AMI ASIC: Depend on it.

High Performance Solutions in Factory Automation, Computers, Instrumentation, Defense and Semiconductors.

GOULD
Electronics

Circle 23 on reader service card



silicon, and 10^{17} for advanced magnetic Czochralski-produced material. This is fine for low-current devices, but the higher resistivity needed for high-current power semiconductors and IR detectors calls for fewer oxygen defects. The floating-zone growth technique keeps contamination to the 10^{15} range.

The relatively small market for floating-zone materials, coupled with fierce pricing competition from Japanese and West German companies, prompted Monsanto Co. to get out of the floating-zone business. The move may have made sense for Monsanto, which decided to focus on its high-volume, higher-growth Czochralski business. But some DOD officials and other users of high-current power semiconductor devices are worried about depending on foreign sources for the material.

Thomas says Westinghouse plans to fire up its floating-zone furnace in about three months for the first time. Currently, the only companies producing leading-edge 4- and 5-in. floating-zone ingots are Shin-Etsu Chemical Co. and Komatsu Electronic Metals Co. in Japan and West Germany's Wacker-Chemie GmbH, say industry sources. "As soon as they [Monsanto] got out of the business, we [U.S. device makers] couldn't get the material. There were 12- to 15-month delays and it was a seller's market," complains Narain Hingorani, director of the transmission department for the Electric Power Research Institute (EPRI), an R&D funding organization sponsored by the power-utility industry.

The supply situation now seems to be easing, says Thomas Nowalk, an advisory engineer at Powerex Inc., a Youngwood, Pa., joint venture of Westinghouse, GE, and Mitsubishi. "We've gotten some engineering quantities of 5-in. floating-zone wafers, and 4-in. wafers are now commercially available."

Westinghouse plans to fire up its floating-zone furnace in three months

Nevertheless, the Defense Advanced Research Projects Agency plans to provide funding for the Westinghouse effort, probably by late in the current fiscal year ending Sept. 30, says Richard A. Reynolds, director of Darpa's defense sciences office. The ultimate amount could be affected by Gramm-Rudman budget cuts, Reynolds says. But he adds that Darpa hopes to work toward the $1 million annual level proposed by Westinghouse for the course of its planned three-year effort.

Westinghouse also expects to get funding from the Army and an Air Force program that is working on how to increase the purity of polysilicon, says Thomas. Also, EPRI may provide about $750,000 over three years, contingent on adequate funding from Darpa or others to ensure a reasonable chance of the project's success, Hingorani says. "If they [Westinghouse] don't commercialize the process, then our interest isn't there."

Today's high-current devices based on 4-in. floating-zone silicon wafers can block about 5,000 V and switch about 100 MW, says Thomas. But after three years, Westinghouse aims to produce high-quality 5-in. floating-zone wafers to support devices capable of 20,000-V blocking and switching up to 500 MW, he says. Westinghouse will start by growing 4-in. crystals but expects to begin producing 5-in. ingots about 18 months into the project. *–Wesley R. Iversen*

A WAY TO MAKE OXYGEN-RICH WAFERS

TOKYO

Sometimes oxygen-rich wafers can be a boon to chip makers, and so Sony Corp. has moved in the opposite direction and modified its magnetic-field crystal-pulling technology to produce wafers with an extra dose of oxygen in the single-crystal lattice. The oxygen-rich wafers should be good for fabricating memory and bipolar analog chips because they provide intrinsic gettering, capturing the metallic contaminants in the melt.

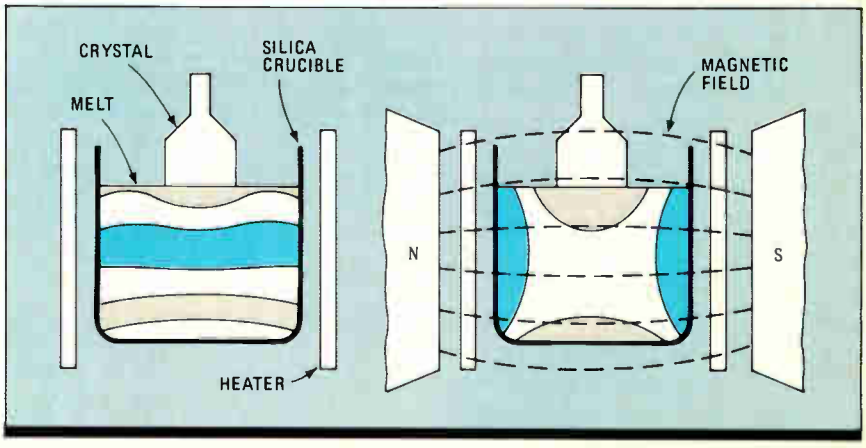
The technique produces lower defect densities at the wafer surface than is possible with a conventional Czochralski process, so the high-oxygen wafers promise higher device yields. Sony expects to use these wafers in memory production soon.

The new process is based on one Sony developed about six years ago. Called magnetic-field Czochralski, or MCZ, the process uses a vertical or horizontal magnetic field to suppress motion in the melt [*Electronics*, July 3, 1980, p. 83]. The company's patent claims also apply to other semiconductor materials—the process is being used by Nippon Telegraph & Telephone Corp. to grow gallium arsenide, for example. Sony has already licensed MCZ to Monsanto Co. in the U.S. and several Japanese wafer manufacturers.

The controlled MCZ environment means process parameters can be varied to tailor characteristics for different devices. It can reduce oxygen atoms in the crystal lattice to about 10% of the number found in conventional wafers—or it can increase them. Such parts as power thyristors and charge-coupled-device sensors benefit from low oxygen content, but others accrue more benefits from added oxygen.

New MCZ process conditions enable ingots to be grown with an oxygen content of about 2.8×10^{18} atoms/cm^3; 2.0×10^{18} is difficult to obtain using conventional methods. Also, the crystal-growth rate is increased to 1.6 to 2.0 mm/min, about twice the normal speed, while keeping ingot surface striation and internal defect-density low. The higher oxygen content of the new process comes from rotating the crucible to increase the rate at which the fused quartz—silicon dioxide—dissolves in the melt.

Because motion in the melt is controlled, it is possible to use carbon heaters that are designed with profiled heating characteristics to give a designed temperature profile in the melt. The proper temperature profile is a key factor in reducing the surface defect density. In the standard Czochralski process, the temperature in the melt changes in horizontal strata but is almost constant



MELT. Temperature varies rapidly along the central axis of a standard crystal-pulling melt (left). Sony uses magnets to control both heat distribution and oxygen content in the crystal (right).

"My philosophy on ASIC design? Whatever works for you."

"Some application specific IC (ASIC) houses are very rigid. You follow their rules—no questions asked. At Gould AMI, you make the rules.

For example, we know learning an unfamiliar CAD system takes time. So we support the workstations and PC systems most designers use: Mentor Graphics, Daisy Systems, P-CAD, Viewlogic and FutureNet, to name a few. Plus our own terrific, low-cost software for PCs—Sceptre II. You can even get translator programs for proprietary systems. And as much design help as you want.

Why reinvent the wheel? Use our proven gate array and standard cell macros, and you can quickly design an application specific IC to meet your exact performance, time to market and cost needs.

Call me. I'm committed to making your design efforts easy and successful."

To optimize your ASICs, call us at 408-554-2311. Gould Inc., Semiconductor Division, manufacturer of Gould AMI semiconductors.

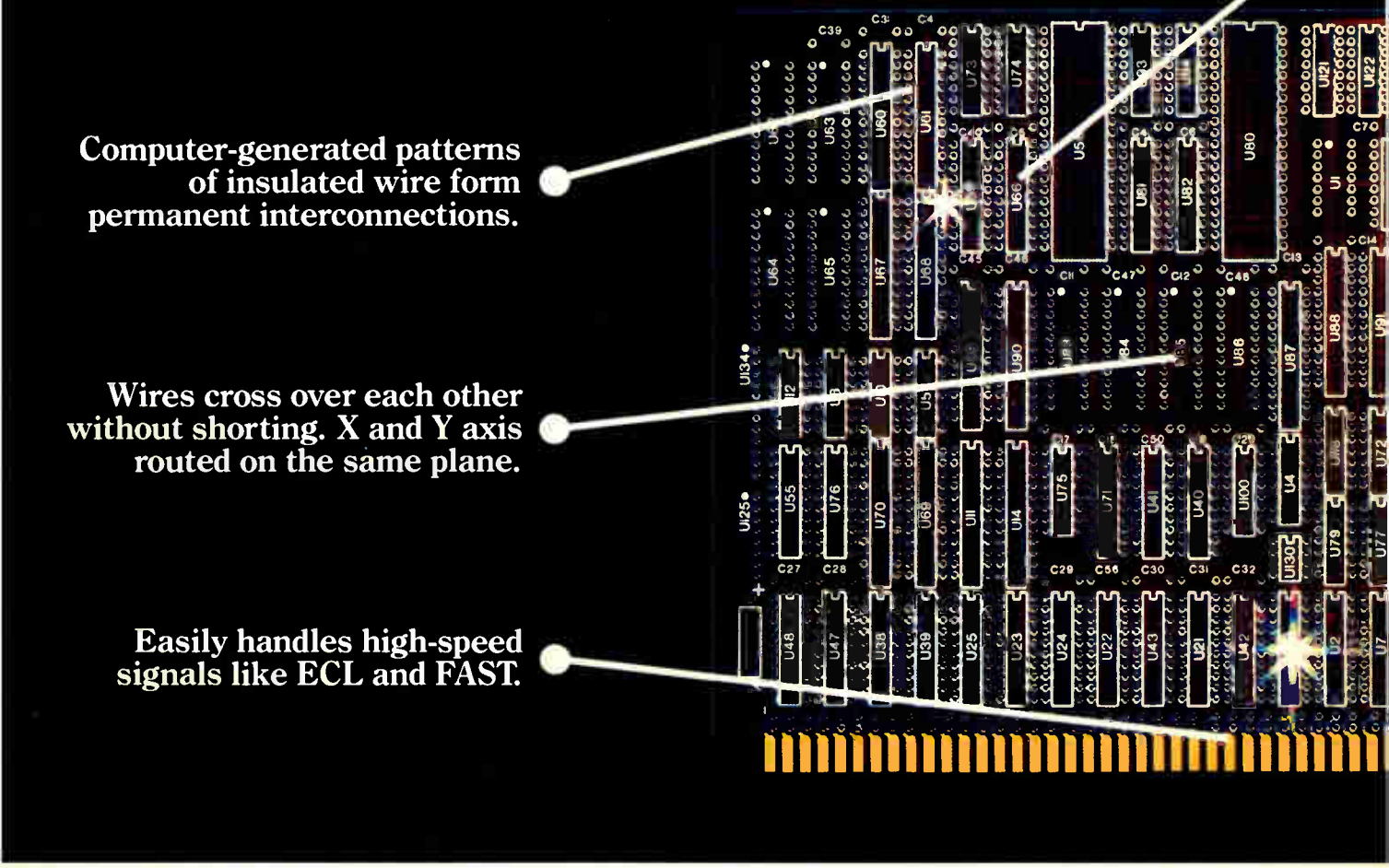
Gould AMI ASIC: Depend on it.

High Performance Solutions in Factory Automation, Computers, Instrumentation, Defense and Semiconductors.

GOULD
Electronics

Circle 25 on reader service card

WHY MULTIWIRE DIVISION BOARDS ARE BETTER THAN MULTILAYER. POINT BY POINT.



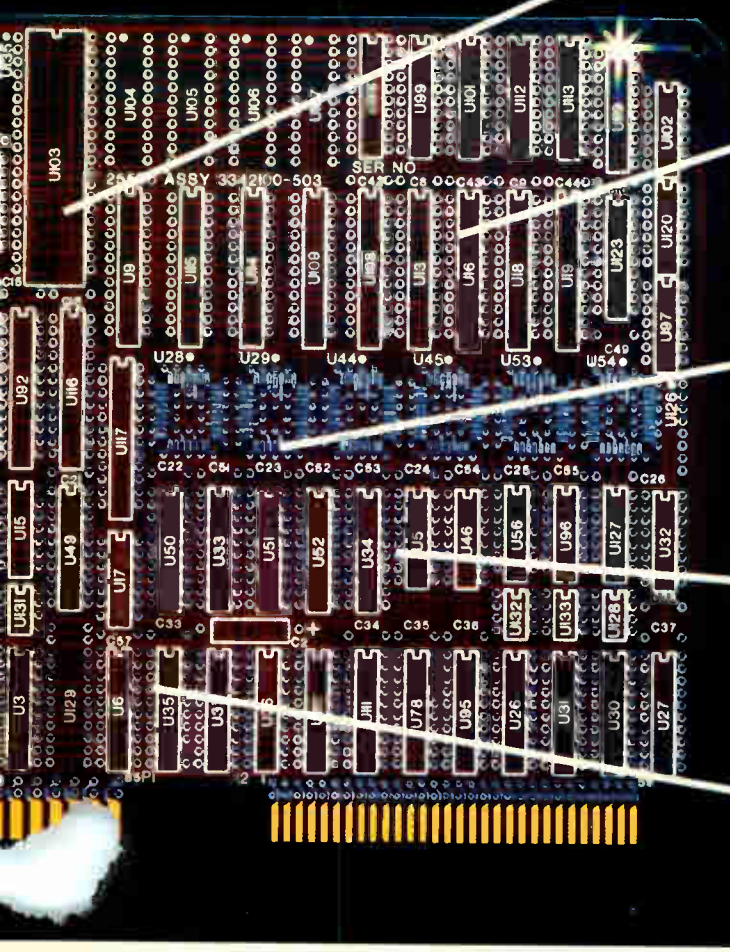
Multiwire Division's electroplated circuit board construction provides surface features for surface-mount components as well as traditional through-hole-mount components. Our experience in new package types encompasses both leaded and leadless devices with pin pitches of 18 mils or more, pin grid arrays and discrete surface-mount components.

We have successfully designed and manufactured boards to accommodate pin grid arrays and chip carriers with 130 pins and greater. Because our insulated wires can be crossed without shorting, board real estate can be used for components instead of via holes. This allows increased packaging densities and decreases the need to interconnect between cards, which can result in greater system reliability and lower costs.

Over the last 16 years, Multiwire Division has designed and manufactured thousands of Multiwire boards. We have produced boards for through-hole and surface-mount components, military and VHSIC/VLSI applications and used our expertise and experience to solve system and circuit design problems for high-speed logic and thermal management applications. Our sales, design and manufacturing centers located across the country are ready to prove to you the advantages of Multiwire boards from Multiwire Division. For a free copy of our brochure, just fill out and return the coupon.

Meets or exceeds ANSI/IPC-DW-425 (DOD) and the performance requirements of MIL-P-55110.

Accommodates component densities of 0.4 square inch per IC and greater.



Fast and economical design and design revisions.

Electroplated surface features mechanically and electrically accommodate surface-mount components.

Superior electrical characteristics. Crosstalk and impedance levels tightly controlled.

Designed from as little input as a schematic or netlist.

MAKE IT A POINT TO BUY MULTIWIRE® BOARDS FROM MULTIWIRE DIVISION.

MULTIWIRE
250 Miller Place, Hicksville, NY 11801

☐ Please send me a free copy of your brochure.
☐ Please have a salesman call.

Name
Title
Company
Address
City State Zip
Telephone

MULTIWIRE® DIVISION
KOLLMORGEN CORPORATION

MULTIWIRE/EAST, 250 Miller Place, Hicksville, NY 11801 (516) 933-8300
MULTIWIRE/NEW ENGLAND, 41 Simon Street, Nashua, NH 03060 (603) 889-0083
MULTIWIRE/WEST, 3901 East La Palma Avenue, Anaheim, CA 92807 (714) 632-7770
Multiwire® is a U.S. registered trademark of the Kollmorgen Corporation.

STYLE.

STYLE AND SUBSTANCE.

The differences between the Citibank Preferred℠ Visa® card and the other card that happens to be pictured here are, in a word, substantial.

To start, we offer a credit line of $5,000 to $50,000. And our card is accepted in 4 times as many places as theirs. From restaurants to resorts, on business trips or pleasure trips, it's always the right card in the right place.

What's more, the Citibank Preferred Visa card gives you immediate access to the nation's largest network of cash machines. At bank branches, shopping centers and major airports.

You can also take advantage of substantial financial opportunities unique to Citibank. Everything from investing in CD's and high interest savings plans* to buying gold bullion.

And every time you use our card, you'll earn CitiDollar$® Bonuses good for valuable discounts on brand-name merchandise, from the truly extravagant to the downright practical.

No other card gives you as much. Not some other bank's premium card. Not American Express® Gold, despite their fancy annual fee.

If your household income is at least $25,000, fill in the application and mail it. If it's already taken, call us toll-free at 1-800-952-2152 and we'll rush one to you.

Everyone can use a touch of style. But there's no substitute for substance.

CITIBANK®
A CITICORP COMPANY

THE CARD TO END ALL CARDS.

*Federal regulations require substantial penalties for early withdrawal from time accounts.

Circle 28 on reader service card

from center to edges (see figure). The temperature is at its minimum at the top and increases markedly to a certain depth, after which it again decreases.

In the new process, there is a hot zone around the periphery of the melt, and temperature change from top to bottom along the central axis is reduced. The ingot is cooled rapidly as it is pulled from the melt.

Interstitial oxygen at the wafers' surface is driven off during initial stages of processing, forming a low-oxygen region for device fabrication. Oxygen in the bulk interior has less propensity to precipitate out than in conventional wafers because the wafer has a far lower density of defects to act as precipitation centers. Defect density at the surface is reduced from 10 to 1,000 per cm^2 to close to zero. Mechanical properties such as high-temperature strength are also superior.

Although the MCZ process requires a hefty investment in magnets and the power to operate them, Sony says the increased crystal-pulling rate attained in the new process more than balances out the increased cost. *–Charles L. Cohen*

DATA COMMUNICATIONS

THIS SINGLE-CHIP MODEM COULD GET ISDN GOING

AGRATE, ITALY

A big roadblock in the push for a European integrated-services-digital-network standard is a means of achieving acceptable data rates in cases of relatively low phone-line quality. What's needed is an inexpensive, high-speed, one-chip modem to realize the U interface, the connection between the digital exchange and the subscriber line.

Neither of the conventional modem designs for coping with variable-quality phone lines fill the bill. Echo-cancellation techniques are too complex for an inexpensive one-chip implementation. "Ping-pong" burst-communication techniques, in which transmission bursts bounce back and forth between the modems on either end of the line, can't span long distances.

The chip uses a new method for signal processing

A compromise may be at hand, however. Engineers at Italy's SGS Microelettronica SpA have developed a signal-processing scheme called echo-pong, which combines both techniques.

Echo canceling is generally preferred for phone-line modems because it imposes fewer limitations in distance and transmission rate. Unfortunately, implementing echo canceling would require a chip of well over 100,000 transistors, a correspondingly expensive item. This is the route that ITT Corp. and Siemens AG are following for West Germany's ISDN trials scheduled for 1988.

Ping-pong systems cost as little as one tenth as much to implement, but are restricted to far shorter transmission distances. For this reason, ping-pong techniques can be more profitably used for private ISDN applications—within a single building, for example—than for public networks.

SGS's answer to this dilemma is to combine the most attractive elements of both systems. In the echo-pong scheme, a patented echo-canceling burst-mode modem provides a full-duplex data-communications link over a standard two-wire telephone link at 144 kb/s, which will be the norm for first-generation ISDN applications. It does this at a cost near that of conventional ping-pong modems.

In essence, the SGS U-interface system codes the standard ISDN signal into frames with a length of 4 ms. These frames are further broken down into three periods—one each with only useful data, only echo, and a combination of the two.

Because the system knows which part of the frame is carrying which kind of data, it simply extracts the part containing useful data and uses the section with only echo to determine the echo's parameters. Data is easily extracted from the portion containing both signals by using the known parameters to cancel the echo. As in ping-pong systems, a period with no data between frames is used for synchronization of the signal.

Designated the SMT 1C10, SGS's chip will carry a line interface, alternate-mark-inversion coder and decoders, a line equalizer, a digital-feedback-equalizer and echo-canceler module, and a 12-bit digital-to-analog converter, all synchronized by a digital phase-locked loop. Because the system uses complex and cumbersome echo canceling for only one portion of each frame, it can process the signal as a whole at a rate of 160 kb/s to reach the net 144 kb/s rate.

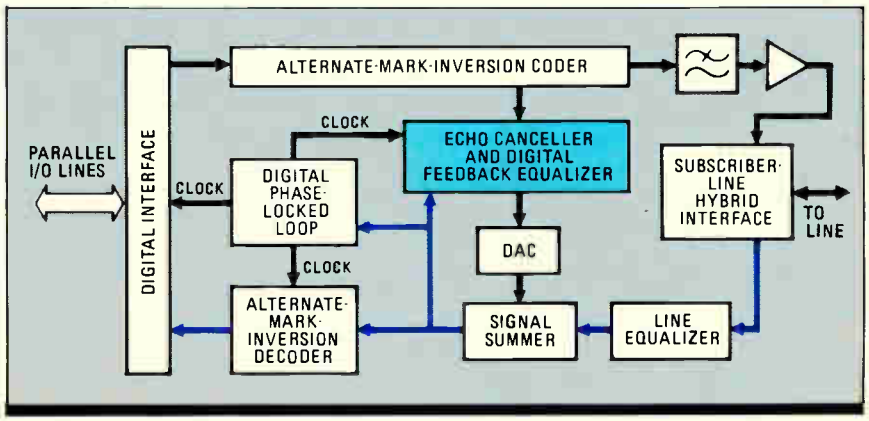
Such a scheme requires only 35,000 transistors on chip, says Gianguido Rizzotto, SGS's manager for corporate strategic marketing in information technology. What's more, it can transmit as far as 7 km, so it can be used for the vast majority of ISDN connections.

"We began studying the Italian market and found that our echo-pong system could be used to realize some 95% of the envisaged connections," Rizzotto points out. "Looking further, we found that it was sufficient to satisfy a similar number of connections in Germany, France, and the UK."

CONFORMS. The chip will conform to the International Telegraph and Telephone Consultative Committee 1430 standard bearing on ISDN interfaces, and it has already been chosen by Italy's national phone company for its ISDN trials. Rizzotto says SGS is in "an advanced stage of negotiations" with the French and Swiss telecommunications authorities for its use in those countries.

Equipment manufacturers wishing to design it into their equipment can purchase the system in the form of a board based on two 5,000-gate arrays. The cost, a seemingly steep $40,000 for four boards, is explained by Rizzotto as the price for participating in the development of the circuit rather than the outright purchase of the boards. He says the sales to customers already contacted are higher than SGS expected.

SGS is holding back on completion of the single-chip version until reaction is in from equipment manufacturers. First samples of the 2-μm CMOS chip are scheduled for delivery in the second quarter of 1987. *–Robert T. Gallagher*



ON LINE. SGS's U-interface chip for integrated services digital networks teams echo-canceling and ping-pong techniques to achieve 144-kb/s rates on existing subscriber lines.

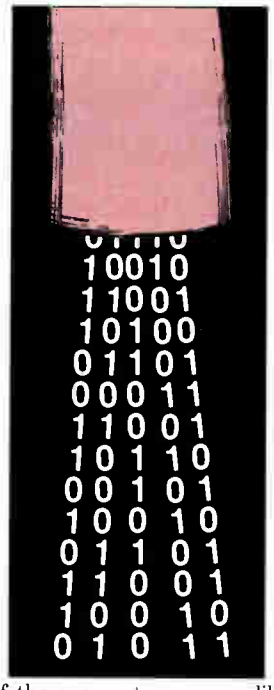
INSIDE TECHNOLOGY

MOTOROLA'S SIZZLING NEW SIGNAL PROCESSOR

THE CHIP IS A LATE STARTER, BUT OUTSPEEDS RIVALS

Motorola Inc.'s first digital signal-processing circuit finally is out in the open. The highly parallel, 24-bit CMOS chip, designated the DSP56000, can execute 10.25 million instructions per second at maximum clock rates of 20.5 MHz. Though Motorola is entering the DSP market later than its major competitors, product managers at the company's new Digital Signal Processor Operation in Austin, Texas, believe the wait will pay off. With the extra time, the company was able to apply a number of new architectural and programming concepts to its DSP development efforts.

Motorola claims that its technology eclipses the power of other recently introduced DSPs. Most important is the unmatched ability to perform 24-by-24-bit multiplications and a 56-bit accumulation in a single 97.5-ns machine cycle. Multiplication-accumulations are one of the most heavily used sequences in DSP algorithms, and the faster throughput gives the chip the ability to serve emerging real-time applications.



The 88-pin 56000 contains four 24-bit parallel data buses and three concurrently operating execution units—the address arithmetic logic unit, the data ALU, and the program controller. Each of the execution units has its own independent memory space. The chip also contains three independent memory blocks and programmable multiple input/output ports that reduce the overhead of using external memories or peripheral devices. The general-purpose 56000, Motorola says, will also top the latest introductions with a rich set of microcomputer-like I/O peripherals and a broad-ranging microprocessor-like programming model.

"This is the biggest announcement that we have made in the last five years," says Murray A. Goldman, vice president and general manager of the Microprocessor Products Group in Austin, which is the parent unit of the new DSP Operation. And Motorola is betting big that DSPs will be where the action is.

"We are going after this emerging market to be No. 1—we are not treating it as a niche," says Goldman. Some of the markets Motorola sees for the DSP are in telecommunications, numerical processing, spectral analysis, two- and three-dimensional imaging, and speech recognition and synthesis. Sample quantities of the 56000 will be available in the second half of the year, and software that simulates the processor on personal computers is now ready for prospective 56000 users.

To get the 56000 to the top of the DSP heap, Motorola is relying on a highly optimized hardware architecture, which is largely responsible for its speed. Goldman says the 56000 is a reduced-instruction-set-computer (RISC) chip. Thus the design boasts a nonpipelined multiplier-accumulator and some 62 software-language instructions tailored to DSP applications.

The company is hailing the 56000 as a fourth-generation DSP. As Motorola tells it, the first generation began with NEC Corp.'s 7720, which incorporates a 16-by-16-bit multiplier on a programmable processor. In the early 1980s, Texas Instruments Inc. began what Motorola says is the second generation of DSP circuits with the introduction of the TMS32010. The design brought the Harvard architecture—which includes separate program and data storage—to the DSP world, and featured a pipelined accumulator to the multiplier and the ability to expand memory off the chip.

Motorola believes the recent round of DSP announcements constitutes a third generation, adding dual data memories, larger data sizes, and address-generation techniques. What makes the 56000 a fourth-generation DSP, Motorola believes, is single-cycle multiplication-accumulation combined with increased parallelism, plus its microprocessor-like features and programming techniques.

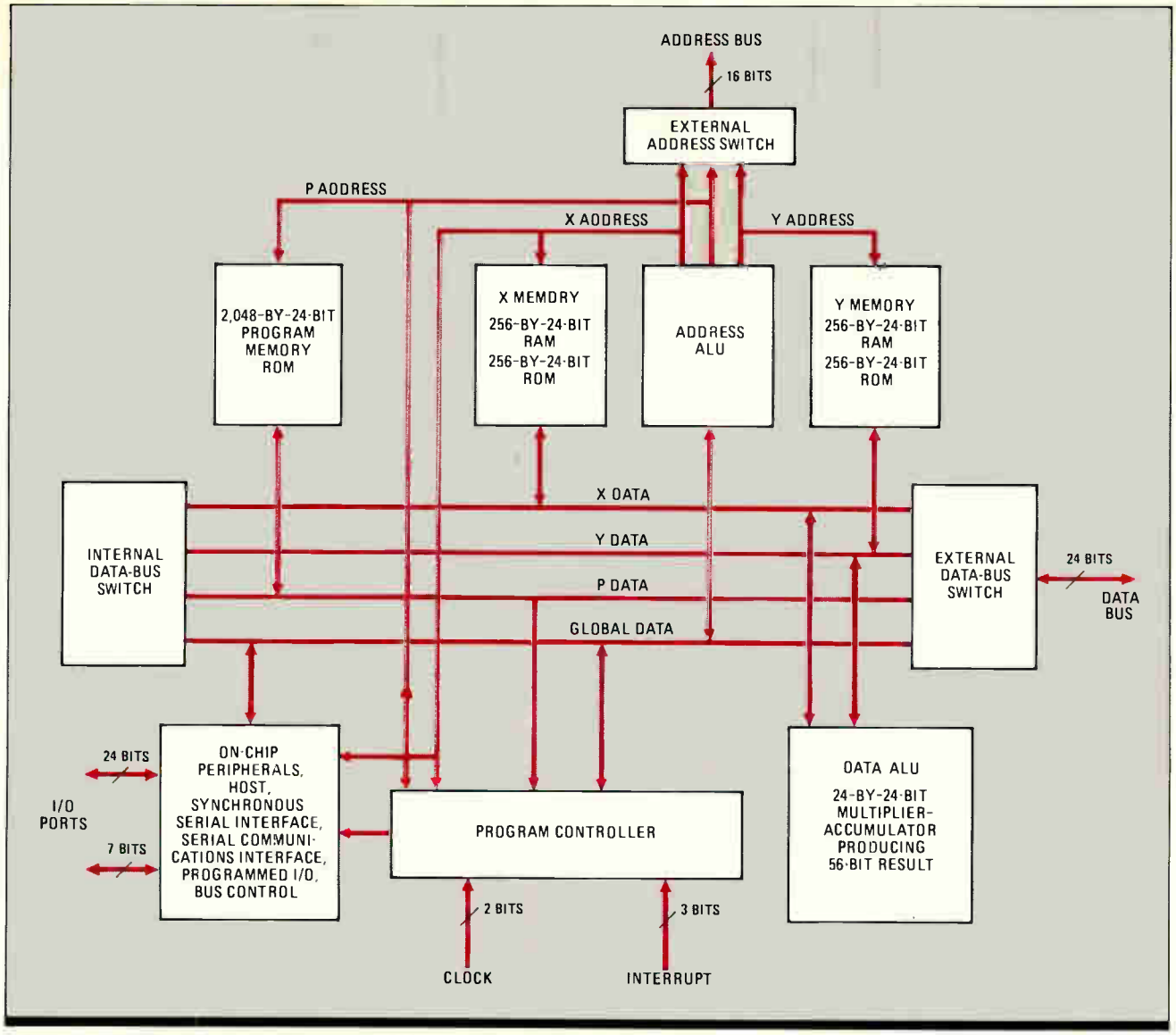
Driving the high-speed 56000 is a patented array multiplier. Internally, its results are handled by two 56-bit accumulators, which can be used interchangeably as source and designation registers. The accumulators provide some 336 dB of dynamic range—as much as three times the amount of some current DSP products, says Jim Thomas, systems manager for the 56000 project. Although the ALU uses 56 bits internally, data is sent out of the 56000 through a 24-bit word, which can handle a 144-dB dynamic range.

PRESERVING PRECISION

The accumulators' wide dynamic range guarantees that no precision is lost in calculations. Moreover, the multiplier-accumulator can round off the results with another addition function in the same clock cycle. Results are immediately available on the next machine cycle.

Unlike multiplier-accumulators in the data ALUs aboard other DSP products, the one-cycle engine is a single circuit block, rather than two math units pipelined together, explains Kevin L. Kloker, principal staff engineer at Motorola's Systems Research Laboratory in Schaumburg, Ill. He says that many DSP chips appear to perform single-cycle multiplication-accumulations because one instruction triggers the math sequence. The multipliers are often pipelined to accumulators, and because data streams must run from one arithmetic block to the other, pipelined results generally are not available on the next clock cycle. In the 56000 chip, however, the data ALU also contains 10 registers and uses separate X and Y data

TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*



1. HIGH-POWERED. Motorola's 24-bit digital signal processor, the 56000, performs 10.25 mips at a 20-MHz clock rate.

buses to load and store two operands simultaneously.

The nonpipelined multiplier-accumulator makes programming easier, according to Goldman. With a pipelined architecture, the programmer faces the complex task of reestablishing data flow whenever an operation is interrupted. The 56000 is not pipelined, so once the cycle is over, the data is instantly available.

THREE EXECUTION UNITS

The 56000 spreads processing among the three concurrently operating execution units. Each of the units has its own set of registers to eliminate processing overhead while concurrently performing its job, says Kloker.

"What we like to do is keep all three sections busy all of the time, then we can achieve our maximum throughput," he says. The chip contains three 24-bit-wide memory blocks—two (X and Y) for data and one for program storage. The parallel X and Y data buses can be used in tandem to produce an internal 48-bit data word—what is known as double-precision mode. This preserves the 48-bit accuracy of the multiplier-accumulator (the extra 8 bits of the 56-bit total are for overflow protection), and doubles the internal dynamic range to 288 dB—useful for systems requiring a high degree of accuracy, such as global navigation positioning. The memories can deliver independent simultaneous fetches in single 97.5-ns cycles over the processor's four parallel 24-bit buses (Fig. 1).

Two of the buses are routed logically between the data ALU and the separate X and Y data memories. The program data bus links the program controller to its memory. A 24-bit global data bus provides a pathway between the three parallel execution units and supports programmable communications to a broad range of onboard and off-chip peripherals.

Internally, the separate X and Y storage spaces are made up each of 256 by 24 bits of random-access memory and the same configuration of read-only memory. The program memory contains 2,048 by 24 bits of ROM. The RAM provides the main storage for data on chip, while the data ROM is used for coefficients, such as for filters and lookup tables. The address ALU has some 24 registers and two modulo-arithmetic units, which calculate a wide range of address modifications. The address ALU can also use the program memory through the parallel bus structure for additional storage of coefficients and lookup tables.

All three memory spaces can be expanded with an external address switch and an external data bus switch. The 56000 chip can use up to 128-K by 24 bits of external data storage and 64-K of off-chip program memory. The DSP has been designed to incur no overhead penalties whenever an

```
                do      #passes,_end_pass
                move                    n0,a1
                lsr     a               #data,r0
                move                    a1,n0
                move                    r0,r4
                lua     (r0)+n0,r1
                lua     (r1)-,r5
                move                    #twiddle,r6
                move                    n0,n1
                move                    n0,n4
                move                    n0,n5
                do      n2,_end_grp
                move                    x:(r1),x1       y:(r6),y0
                move                    x:(r5),a        y:(r0),b
                move                    x:(r6)+n6,x0
                do      n0,_end_bfy
                mac     x1,y0,b                         y:(r1)+,y1
                macr    x0,y1,b         a,x:(r5)+       y:(r0),a
                subl    b,a             x:(r0),b        b,y:(r4)
                mac     x1,x0,b         x:(r0)+,a       a,y:(r5)
                macr    -y1,y0,b        x:(r1),x1
                subl    b,a             b,x:(r4)+       y:(r0),b
_end_bfy
                move                    a,x:(r5)+n5     y:(r1)+n1,y1
                move                    x:(r0)+n0,x1    y:(r4)+n4,y1
_end_grp
                move                    n2,a1
                lsl     a
                move                    a1,n2
_end_pass
```

2. ROUTINE WORK. Thanks to the Do-Loop instruction, the 56000 can perform a radix 2 fast Fourier transform routine with as little as 42 words of code.

instruction must access one external device.

Motorola is also attacking signal-processing bottlenecks with a bundle of new programming modes as well as reconfigurable I/O ports. Programming modes and fast-interrupt structures have been styled like those found on many popular microprocessors—including Motorola's own 68000 family.

The 56000 has a total of 62 basic operation codes. A Do-Loop instruction cuts down the amount of assembly code necessary to perform complex DSP algorithms by instructing the processor to repeat a block of macrocode a certain number of times. In addition, Motorola is making available in its DSP development software package a wide variety of macrocode for signal filtering and other popular applications.

The Do-Loops are executed in the hardware registers of the 56000's program controller, eliminating software overhead. The potential code saving from Do-Loop instructions grows as DSP applications become more complex, says Bryant Wilder, operations manager at the Digital Signal Processor Operation. The program controller contains a system stack of registers 15 words deep, which will support 15 interrupt levels or seven nested Do-Loop commands. The system stack can be extended into the allocated memory space using software stack-pointer operations.

The Do-Loop instruction makes it possible to perform a radix 2 fast Fourier transform with as little as 42 words of code. The number of words remains the same, whether the DSP application is a 64-point FFT filter or a more-complex 1,024-point filter. Only the repeat values for the Do-Loop increase (Fig. 2).

As a result of the loops, Motorola claims the 56000 will outperform competing DSP parts with shorter code when executing a 1,024-point complex FFT filter program. Wilder says the FFT code for competing parts will be as much as 15 times longer than similar 1,024-point filter applications using Motorola's hardware-nested Do-Loops. The efficient code, plus the fast parallel hardware, enables the 56000 to complete 1,024-point FFT filtering algorithms in 5 ms (table). The new Analog Devices Inc. ADSP-2100, which contains a 16-by-16-bit multiplier but is highly parallel, executes the 1,024-point FFT in 7.2 ms, and National Semiconductor Corp.'s LM32900 takes 13.24 ms. And NEC says its new 77320 executes the 1,024-point FFT in 10.75 ms. Running against the same 1,024-point filtering application, TI's 320C25 has been benchmarked by its maker at 7.1 ms.

Motorola sees another ease to programming in its flexible address calculations, or address modifiers. This concept employs modulo arithmetic and a dedicated set of hardware registers in the address arithmetic logic unit.

In essence, the modifiers set up circular buffers, which automatically move the address pointers from one point in memory to any other location and returns them without incurring the overhead of shifting data. Some chip designs have implemented circular buffering techniques, but none allows the flexibility of arbitrary modulo calculations and offset values, adds Kloker, who originated Motorola's concept. Motorola believes the modulo-addressing scheme is useful in a number of applications, such as in speech recognition, that require DSP chips to work their way through table structures.

"This directly implements structures, such as those known as delay lines. For microprocessors, they are known as a queue or a first in first out. We directly implement those data structures in memory," says Kloker. The address modifiers set up the structures through hardware registers, speeding up processor operations and eliminating the overhead associated with similar functions implemented in software.

In the future, Motorola plans to introduce high-level language tools for programming 56000 applications. "We fully expect that a high-level language will be used most of the time, with some assembly language mixed in the places where speed has to be optimized," says Goldman, adding that Motorola intends to support a high-level language for DSP.

BENCHMARK COMPARISONS OF DIGITAL SIGNAL PROCESSORS

Benchmark	NEC 7720	TI 32010	TI 32020	Motorola 56000
Finite-impulse-response filter with data shift	0.75 μs per tap[1]	0.4 μs per tap[2]	0.2 μs per tap[5]	0.1 μs per tap
Infinite-impulse-response biquadratic filter	2.25 μs[1]	2.0 μs[3]	2.0 μs[5]	0.4 μs
64-point complex fast Fourier transform	1.6 ms[1]	0.555 ms[2]	0.434 ms[6]	0.147 ms
256-point complex FFT	—	20 ms[4]	2.44 ms[6]	0.713 ms
1.024-point complex FFT	77 ms[1]	42 ms[4]	14.18 ms[6]	5 ms

[1] NEC μPD7720 Signal Processing Interface user's manual
[2] TMS32010 Workshop, TI Regional Technology Center
[3] TMS320(10) Product Description, TI SPRV001
[4] Details on Signal Processing, Issue 5, June 1985, TI SPRN005
[5] TMS32020 Product Description, TI SPRV002
[6] Details on Signal Processing, Issue 6, November 1985, TI SPRN006

SOURCE: VARIOUS PUBLISHED SOURCES AND MOTOROLA INC.

The 56000 has been loaded with a number of microcomputer and microprocessor features. For example, the DSP chip has serial interfaces, similar to those employed on Motorola's single-chip 8-bit microcontrollers to provide a low-cost, dedicated path to outside expansion peripherals and memories. A synchronous serial interface can be used as a 5-Mb/s network linking up to 32 other DSP chips without tying up the main outside data bus.

A host interface on the 56000 provides an 8-bit-wide parallel interface to microprocessors, which may be using the DSP as a real-time peripheral. The host interface has direct-memory-access capabilities. To host microprocessors, the parallel interface is treated as the I/O of fast static memory. A serial communications interface lets the DSP connect to an RS-232-C device. A programmed I/O feature can turn unused host, synchronous serial, or serial communications interfaces—accounting for 24 pins—into general-purpose input/output pins.

The 56000 is designed to be programmed like a microprocessor

The 56000 can also be programmed to have different wait states for four areas of external memories or off-chip peripherals. The programmable wait states are intended to let system designers closely match the access speeds of the DSP chip to a wide variety of fast and slow devices. The wait states, which can be changed on the fly by system software, are intended to reduce the need for extra glue-logic chips that are ordinarily required to match speeds of different parts.

For portable, battery-backed applications, the 56000 contains a number of instructions to place the CMOS chip in a low-power mode. Wait and Stop instructions place the 56000 into a low-power standby mode, similar to that used on Motorola's 6805 and HC11 microcontrollers. The Wait instruction halts the internal clock, taking the power dissipation down to the level of the still-running crystal oscillator. The Stop instruction kills even the oscillator, cutting the power dissipation down to the leakage current of the chip. This mode keeps only data alive in the 56000's registers and memory.

Motorola has focused much effort on making the programming models for 56000 assembly code widely recognizable to microprocessor programmers. "Because of the regularity and rich set of registers, this chip should be quite suitable for high-level languages," Kloker says. "It will allow people to make a tradeoff in the use of assembly languages and high-level languages. That is especially important when you've got 90% of the [chip's operation] time in 10% of the code. A lot of the program could be in higher languages, and then the tight codes could be done in macros, which are in our library."

Along with the chip, Motorola is introducing its DSP development software to potential 56000 customers. The $295 package turns an IBM Corp. Personal Computer or compatible into a full-function simulator and software-code assembler. The development software runs under Microsoft Corp.'s MS-DOS operating system. Motorola chip engineers used the package in the final stages of the design to debug the 56000's complex layout, which has nearly 200,000 transistors. Software development packages are planned for Digital Equipment Corp. VAX minicomputers and Sun Microsystems Inc. engineering work stations.

The 56000 will be fabricated in a new Motorola double-level-metal n-well CMOS process, says Wilder. The initial minimum features are expected to be between 1.25 and 1.5 μm. The process will yield smaller gate lengths than are currently on the 68020, Motorola's most powerful 32-bit microprocessor.

The new CMOS process is now being fine-tuned by another chip design. "We will have nine months of processing information before the 56000 comes out. So we will be able to hit the ground running," says Wilder. □

THERE'S SOME SERENDIPITY IN MOTOROLA'S DSP

To launch its venture into digital signal processors, Motorola Inc. drew on disciplines ranging from technology to marketing. Key members of the project were Kevin L. Kloker, principal staff engineer in the Systems Research Laboratory; Garth Hillman, strategic applications manager; systems manager Jim Thomas; and Bryant Wilder, program leader and operations manager in the Digital Signal Processor Operation.

Kloker pioneered many of the processor's features. At 31, Kloker is already a 10-year veteran of Motorola. He received his BSEE from Bradley University and an MSEE from the Illinois Institute of Technology.

The basic architecture for the single-cycle multiplier-accumulator surfaced during 1981 and 1982, and much of the chip's architecture was set by 1984. A little serendipity came into play during the development: the concept of modulo-arithmetic address modifiers, for instance, came to Kloker while he was taking a shower.

Hillman, a six-year Motorola veteran, campaigned about the virtues of getting into the DSP business. "One thing we recognized early on is that DSP would not be a fad. It will be something that will take us well into the 1990s. We wanted a good foundation to enter that market. So what we came up with may be a little more sophisticated" than what the company started out to do. The 40-year-old Hillman holds a doctorate in electrical engineering from the University of Alberta in Edmonton.

Because speed is what really matters in DSP applications, DSP chips must have enough throughput for real-time signal-processing equipment, notes Thomas, who designed the chip's microprocessor-like features, such as the serial I/O ports. Thomas, 36, was lured back to Motorola by Wilder after he had left to work on ion-implanter control systems. He holds a BSEE from the University of Texas at Austin.

Wilder, 37, heads the new business venture and kept such tight wraps on the 56000 project that many Motorola insiders were unaware of its existence. He collected his BSEE and MSEE from the Georgia Institute of Technology before joining Motorola 11 years ago.

To Wilder, one of the most exciting aspects of the Motorola DSP is that not even the company conceived of all the product's future applications. "The architecture keeps finding new uses," he says. "We keep finding it can solve problems we did not anticipate."

FATHERS OF INVENTION. Hillman, Thomas, Wilder (behind, from left), and Kloker (front), brought Motorola into the DSP market.

A SYSTEM BUILDING BLOCK THAT GIVES OEMs A FREE HAND

ITS LOW-COST PLATFORM ARCHITECTURE IS EASY TO EXPAND AND UPDATE

The rising star in system architecture is the platform: a base from which many different systems can be built using the latest in cost-effective high-performance hardware. Just such expandability and easy updating are features of the Advanced System Platform from Counterpoint Computers.

The ASP is above all a very flexible system that can be expanded seamlessly and inexpensively, thanks to its open architecture. Processors and peripherals with different functions play in harmony and can be mixed to build systems for many different applications. New hardware, such as faster processors and denser memories, can be applied without disturbing the architecture, thereby preserving a user's software investment. Another example of a platform is Hewlett-Packard Co.'s Spectrum [*Electronics*, March 3, 1986, p. 39].

In developing the ASP and the just-introduced System 19, which is based on it, Counterpoint's design team lowered the price for multiprocessor systems while maintaining high performance. They achieved the lower price primarily with three innovations: the elimination of an expensive bus backplane, a combination of local and global memory that also pared down bus requirements, and an efficient interprocessor procedure call that eliminated the need for expensive hardware to manage multiprocessing. The performance in the San Jose, Calif., startup's System 19 comes primarily from the fast MC68020 microprocessor, the distributed dual-ported memory, and the new interprocessor procedure call. The layered software architecture includes a shared general-purpose window manager for building easy-to-use applications and support for virtual terminals so that existing applications can be run unchanged.

The many different kinds of product strategies that the ASP facilitates mirrors Counterpoint's organizational strategy—begin with a large company and a global outlook through harmonious interplay of diverse organizations [*Electronics*, Jan. 27, 1986, p. 60]. In keeping with that strategy, the company's first product announcement is the System 19 family, a complete customizable computer line built upon the platform provided by the ASP architecture (Fig. 1).

System 19 dramatically lowers the price range of multiple-processor systems—the entry-level price for a two-processor model is $21,500, compared with $60,000 from other makers. Prices of single-processor systems start at $13,000, so the move up to a multiprocessor system is not a big jump. Counterpoint claims that a single-processor system will run 1.5 to 2 times faster than a Digital Equipment Corp. VAX-11/780 in most applications. It says it is the only one offering such inexpensive multiuser multiprocessor systems, multiprocessor graphics systems, multiuser graphics systems, and multiuser multiprocessor graphics systems—all built on the same platform and running the same software.

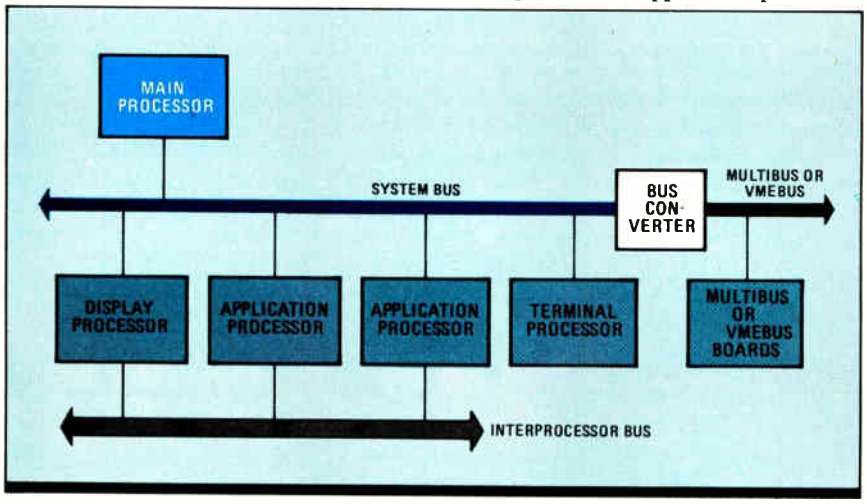
Big multinational businesses, such as Counterpoint's own strategic partners, AT&T and Kyocera, require very broad product lines to compete in multiple vertical markets. To meet these needs, Counterpoint has designed and developed a platform that can take on many different market personalities—a chameleon-like system. Another important need of big companies that System 19 provides is the ability to move quickly with new technologies into emerging markets.

ONE FROM COLUMN A

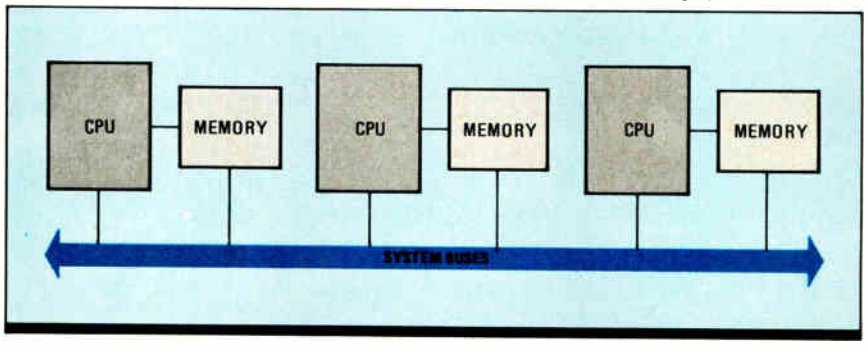
The System 19 family consists of multiple-personality work stations and computer systems offering choices like those from a Chinese restaurant menu. From the graphics offering, a user can chose monochrome or color. In multiuser systems, the choices are bit-mapped work stations, ASCII terminals, or a mixture of both. And for network servers, the list includes computational servers and gateways to two IBM Corp. networking schemes—Systems Network Architecture and 3270.

The key features of the System 19 are:

- A main processor and up to seven application processors



1. MULTIFACETED. System 19 can take on muliple personalities with its different types of processors, peripherals, and standard-bus boards. Dual buses deliver high performance.



2. MINE AND YOURS. Memory is connected to individual processors through one port and to the system bus through another, providing the advantages of both local and shared memories.

(graphics units, input/output processors, and the like).

- AT&T Co.'s Unix System V operating system, version 2.2 with virtual memory and the Berkeley 4.2bsd networking extensions.
- An icon-based user interface.
- Ethernet with the Transmission Control Protocol/Internet Protocol.
- Gateways to VME and Multibus buses.

Counterpoint's offerings are open systems so that its customers can develop multiple product lines with software compatibility. Also, each product line can grow incrementally over a wide performance range. In other words, Counterpoint has achieved a pathway to seamless systems of unified products. The openess that contributes to the seamless expandability consists of a standard operating system, a proprietary system bus that original-equipment manufacturers can license, and many other functions, such as bus expansion and networking, that are based on industry standards.

3. SMARTLY DRESSED. The flexible, expandable System 19 product family comes in a 5-in.-high plastic-sheathed case. As systems expand, modules neatly snap together.

Also contributing to the seamless expandability is the ability to add application processors for many different types of jobs. As long as they adhere to the system bus specification, these processors can be of any circuit technology and architecture. Equally important for seamless expandability is the fact that a basic low-cost, one-processor system, small to medium multiprocessor systems, and the biggest multiprocessor configuration all look alike to the software. Another seamless aspect is the ability to mix different types of applications on one system, such as adding support for business data processing to a basic graphics work station. Such flexibility is a boon to small companies or small departments in larger companies.

The processor building block in the System 19 is a powerful single-board computer consisting of a Motorola 68020 central processing unit, a memory-management unit, an MC68881 floating-point processor, 1 to 5 megabytes of memory, two RS-232-C input/output ports, an Ethernet interface, and a disk controller. A user can mount one of these boards in a Counterpoint System 19 cabinet with a power supply and a disk drive and connect two terminals to create a low-cost two-user system.

One money-saver is a a system bus based on the processor bus

The Counterpoint engineers decided it would be too expensive to have two buses plus a card cage. So they extended the 68020's 16-MHz, 12-megabyte/s, asynchronous 32-bit bus beyond the chip to use it as the ASP system bus. They also eliminated an expensive card-cage backplane in favor of a flexible printed-circuit board that serves as the system bus. As system elements are added, the system bus is extended by lengths of the flexible bus and connectors. To expand the system further with standard bus cards, the engineers added modules that convert bus signals for a VMEbus or Multibus II.

The ASP design also includes a synchronous interprocessor bus to provide an efficient 33-megabyte/s pipeline for transfers of data among processors in high-end configurations. Single processor configurations do not need the interprocessor bus and do not have to bear that cost.

One way the designers of ASP maintained high performance and reduced cost was to come up with a memory design that has the advantages of both shared memory and private memory systems while eliminating as many of the disadvantages as possible. The major advantage of a shared memory system is that workloads can be distributed dynamically. A major disadvantage is that the bus bandwidth will at some point limit the maximum number of processors that can be connected to the main memory. Another disadvantage, for low-end low-cost systems, is that high-bandwidth buses are expensive. Such expense has to be born at the outset even if the first system contains only one or two processors.

In a distributed multicomputer architecture where each processor has its own private memory, load distribution is inefficent because of the message- and data-passing overhead required between private memories. But this setup does use less bus traffic, which means the system can have more processors at a lower bus cost.

LOCAL MEMORY, GLOBAL OUTLOOK

The Counterpoint distributed dual-port architecture retains the advantages of both local and shared memory. The physical memory is tied locally to each processor, but it can perform logically as global shared memory (Fig. 2). It can support a larger number of processors with a low-cost bus and yet retain high processor efficiency because workloads can be dynamically distributed among processors.

For global memory sharing, each processor's memory-management unit maps the total memory of the system—all the local memories—into one contiguous virtual-memory-address space. Each processor then can transparently execute programs either from its own local tightly coupled memory or from a companion processor's memory. The system supports a total physical memory space of 2 gigabytes, allocating 64 megabytes for each processor. Programs or processes can address up to 1 gigabyte of virtual memory out of the total 4-gigabyte virtual memory space.

In any multiple-processor system design, one area that requires very careful planning is the interprocessor communication. A critical function of interprocessor communication is letting one processor call on another to run a process. Inefficient interprocessor communication during such tasks can bog down a system too quickly as traffic volume grows. The Counterpoint team came up with a simple yet efficient interprocessor procedure call.

The engineers used standard Unix mechanisms already in the system for load distribution, so the interprocessor procedure call looks like a context switch. That is, a process can be swapped to another processor in much the same way that it is

swapped out to a disk. For example, the ASP application processors do not have direct access to disk drives. If one of them needs access to data on a disk file, it stops running its current process and puts it on the run queue of the main processor, which controls the disk drives. The data is transferred directly to or from the local memory of the application processor using the direct-memory-access feature.

ADDING FEATURES

One example of an application processor is the ASP display processor, built around a 68020 to provide fast, high-resolution monochrome graphics. Also included is a frame buffer for storage of a screen image and a 32-bit barrel shifter that speeds up graphics functions. The frame buffer can be operated upon by the display processor, the main processor, and any accelerators connected to the interprocessor bus. Counterpoint's engineers coded all the lower-level drawing functions to run out of the 256-byte instruction cache of the 68020. This architecture is fast enough that a more expensive bit-slice processor is required only for color displays.

In System 19, most other application processors are based on the same basic processor as the main processor. Any system configuration can have multiple display and application processors. The system packaging is modular too. For example, there are separate power supplies for each module.

The System 19's main-processor module can contain up to four processors, the mass-storage controller, and the basic disk drives. The basic 5-in.-high chassis module can be used horizontially for a desktop system (Fig. 3) or vertically with feet on it for a desk-side unit. A system can be extended by stacking other 5-in.-high modules and extending the flexible printed-circuit system bus to them.

A processor-expansion module containing up to four processors is one option. Another four-board option is a Multibus or VMEbus module. Also available is an expansion peripheral module containing one or two add-on 5¼-in. disk drives.

At the bottom level of the ASP's layered software is the Unix kernel containing basic system functions such as memory management, paging, and process control. On top of the kernel sit the software drivers for such functions as the disk drives and Ethernet communications. Above the drivers is the window manager, which constructs and handles the multiple windows on the display for all the application software, which is at the top (fourth) layer.

In a multiple processor configuration there remains one copy of the operating system on the main processor. For efficiency, local copies of the kernel code are distributed to each processor. The drivers and the window manager are shared among processors and processes.

For applications written with a particular I/O model in mind, the ASP architecture provides what is known as a virtual terminal facility. The virtual terminal is software that sits between the application and the display. It makes the ASP window display look like the terminal model for which the application was written. The programming code for virtual terminal support communicates with the window manager to learn where on the screen its current window is open then all output traffic is communicated directly between the virtual terminal and the display, freeing the window manager for use by other applications. This scheme eliminates any possible bottleneck caused by the window manager. It also allows existing application programs to run without change since the virtual terminal isolates the application's I/O view from the details of the system architecture.

Many applications with their associated virtual-terminal code can be in use at one time, distributed over all processors. A single window manager can support them all. In this system, windowing is a very efficient operation. □

IT TOOK 13 MONTHS TO DEVELOP THE ADVANCED SYSTEM PLATFORM

It took a talented team to put together all the ideas for Counterpoint Computers' Advanced System Platform. The project attracted computer-system project veterans with a broad range of experience in software and hardware design, which is one reason the team was able to deliver the beta-test units in only 13 months. The team's cohesiveness came from their solid agreement on the main reason they were there—a chance to work on a project they believed in and wanted to do.

"The sense of urgency along with everyone's commitment to the plan and schedule pulled the team together," says Richard Goss, engineering project manager and the first hardware engineer on the team. "Of course, the fact that we made a major sale [to AT&T] early on helped a lot, too." He came to Counterpoint from Qualogy Inc., where he was a hardware manager and did a multiprocessor Unix system. He also spent four years working on bus designs at Motorola Inc.

In directing the development efforts, engineering vice president Fred Kiremidjian kept the focus constant. He and Pauline Alker, company president, brought technical and business acumen to the party. Cofounders of Counterpoint, the two had earlier founded Convergent Technologies Inc. The other principal players also have business as well as technical expertise, most of them having been involved in other startups.

Among the key people, Raymond Hou, director of engineering, is an old Unix hand with a PhD from the California Institute of Technology and Unix experience from AT&T Bell Laboratories and then Convergent Technologies. Providing the design and direction for such packaging issues as the power-supply and printed-circuit board layouts was product design manager Dennis Silva. He spent 11 years at Hewlett-Packard Co., then moved on to two other startups before joining Counterpoint.

Monte Pickard, the program manager for the operating system and networking software, did a distributed file system under Unix at Plexus Inc. Kent Peacock, with a PhD from the University of Waterloo, Ontario, Canada, and experience at Dialogic implementing a multiprocessing kernel for a system, stepped in to manage the multiprocessing software development.

Robert Nystrom, who is carrying the ball beyond the research and development enclave by managing the technical support to customers, worked closely with the development group while directing work on support materials, such as documentation and training aids.

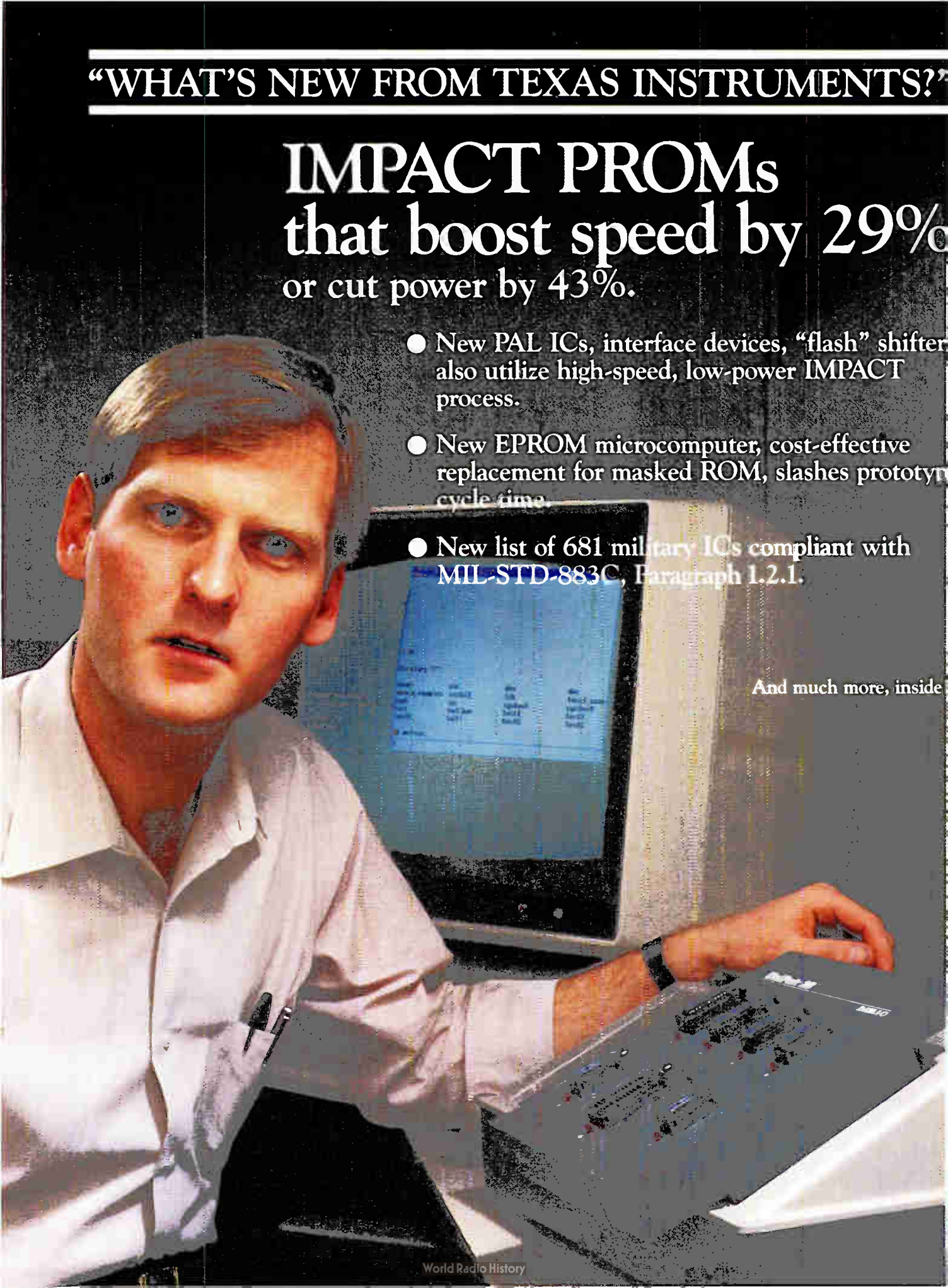
MAKING IT HAPPEN. Sitting left to right are Counterpoint Computers' Monte Pickard, Dennis Silva, Raymond Hou, Robert Nystrom, Kent Peacock, Richard Goss, and Fred Kiremidjian—key figures in the ASP project.

"WHAT'S NEW FROM TEXAS INSTRUMENTS?"

IMPACT PROMs that boost speed by 29%

or cut power by 43%.

- New PAL ICs, interface devices, "flash" shifter also utilize high-speed, low-power IMPACT process.
- New EPROM microcomputer, cost-effective replacement for masked ROM, slashes prototyp cycle time.
- New list of 681 military ICs compliant with MIL-STD-883C, Paragraph 1.2.1.



And much more, inside

IMPACT PROMs deliver 25-ns speed at industry-standard power.

New Series 3 IMPACT™ PROMs from Texas Instruments make 16K-memory performance upgrades quick and easy. If speed is your most critical parameter in a high-complexity PROM, you can achieve it now without paying a power penalty. Just design in TI's new 25-ns, 175-mA IMPACT PROMs: The TBP38S165-25 (2K × 8) or the TBP34S162-25 (4K × 4).

Or use the world's fastest 16K registered PROMs. TI's TBP34R165-18 (2K × 8), with a minimum address-to-clock setup time (t_{su}) of only 18 ns, is nearly *2¼ times* faster than the closest competitor. And the TBP34R162-30 (t_{su} = 30 ns) is the only 4K × 4 registered PROM on the market.

Standard speed at 43% less power

You can also cut power without sacrificing speed, using TI's new TBP38L165-35 IMPACT PROM. It is pin-for-pin compatible with existing 2K × 8 PROMs and operates at the same 35-ns speed, but instead of 175 mA, it draws *only 100 mA*. TI's broad family of Series 3 IMPACT PROMs also includes 256-bit, 1K and 2K devices.

Reliability built in

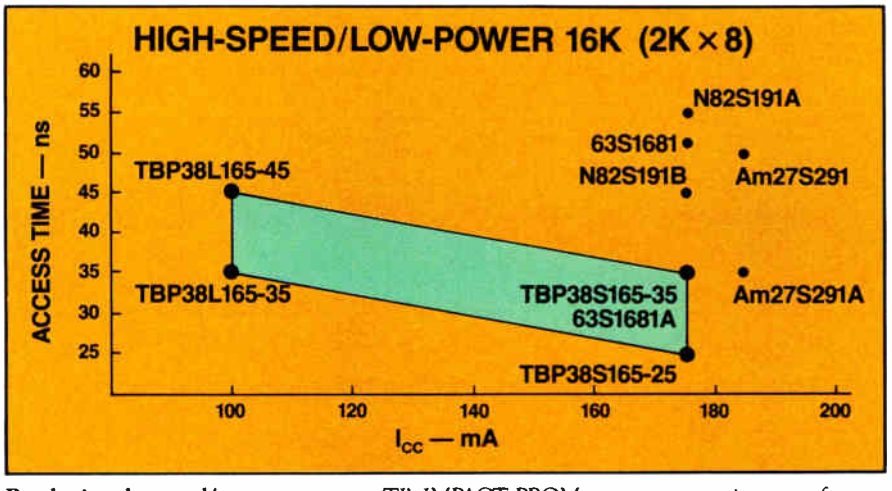
IMPACT PROMs are designed by TI for exceptional reliability. Current densities, metal spacing, and contact sizes are all conservatively designed. Electrostatic-discharge tolerance up to 4,000 V is designed in. During programming, TI-developed titanium-tungsten fuse links insulate themselves with titanium-oxide caps. Electromigration is eliminated by copper-doped aluminum in the first-level interconnection. And you can program any of TI's new Series 3 PROMs on widely available commercial equipment, using TI's standard Series 3 programming algorithm.

Shift 32 positions in less than 29 nanoseconds.

Now TI's 2-μm IMPACT technology also brings you high-speed "flash-shift" operations — with the new 74AS8838 32-bit barrel shifter. Shifting as many as 32 positions in a single 29-ns instruction cycle, it can dramatically increase throughput in such applications as graphics systems, wide-word CPUs, and array processors. At an energy cost of less than 1.5 W, you get higher speed with lower power, in a single 84-pin ceramic pin-grid-array package.

You can program the 74AS8838 for logical, circular, or arithmetic shifts. Its two 3-state, 16-bit outputs give it the versatility to be configured as a 32-bit-in, 32-bit-out barrel shifter, as a 16-bit funnel shifter, or as a 16-bit shifting transceiver. And it can drive buses directly with 24-mA low-level output — with no additional circuitry.

The 74AS8838 barrel shifter, first device in TI's 74AS88XX 32-bit processor chip set, is available today through your local authorized Texas Instruments distributor.



Bracketing the speed/power spectrum, TI's IMPACT PROMs cut power requirements from 180 to 100 mA for "standard" 35- to 45-ns access time. Or at 180 mA, they can give you 25-ns speed.

IMPACT technology doubles speed of new PAL ICs.

Four new exclusive-OR programmable-array logic (PAL®) ICs from TI feature the highest speed available today. Their 20-ns propagation delay at 180 mA makes them twice as fast as any comparable devices.

These devices — TIBPAL20L10-20, TIBPAL20X4-20, TIBPAL20X8-20, and TIBPAL20X10-20 — are designed primarily for counter-intensive applications. The exclusive-OR feature suits them ideally to digital voice applications and video-screen information correction. They can also be useful in memory addressing and mapping.

Programmable logic sequencer is 250% faster because of IMPACT processing.

Still another new product in TI's growing line of high-speed programmable logic devices is the TIB82S105B. At 50 MHz, it is 2½ times as fast as functionally equivalent 16 × 48 × 4 field-programmable logic sequencers — at the same 180-mA power. Unlike them, however, it maintains that speed even when using many product terms.

Because of its improved clocking scheme, the IMPACT TIB82S105B is not a direct replacement for the TI or Signetics N82S105A. But it is ideal for those new high-speed state machines designed to control peripheral I/O, dynamic memory systems, and video blanking systems.

For more detailed information about any of TI's growing line of high-speed, low-power IMPACT products, just check the appropriate box on the attached reply card and return it to TI.

your competitive edge.

6

Keeping you competitive: ASICs and TI.

If you're looking for increased system-level integration and performance, shorter design-cycle time, and reduced VLSI development costs, take a hard look at application-specific integrated circuits (ASICs). And a long look at TI.

Broad choice lets you pick the right implementation

Texas Instruments supports an extensive library of 3-μm CMOS standard cells — more than 200 of the standard SN54/74 TTL functions you have designed with for years — including MSI, analog, and procedural LSI functions like RAM, ROM, PLA, and ALU. In addition, high-drive cells (up to 48 mA) are true TTL replacements.

From TI's new family of advanced standard cells you'll be able to choose among more than 280 functions and achieve increased system integration and performance.

Or for the performance you need, and quick turnaround to get your product to market fast, there's TI's DLM TAC-H and TAC-VH silicon-gate CMOS gate-array family. These devices, fully alternate-sourced, offer complexities from 440 to 8,000 gates.

Extensive design support

Whatever level of help you need, you get it from TI. In your design cycle as well as in meeting your prototype and production requirements *on time*. TI's proven expertise and worldwide manufacturing facilities are your assurance of dedicated support and products in the volume you require. And you have a wide range of package options: DIPs, SOs, PLCCs, pin-grid arrays — from 8 to 179 pins.

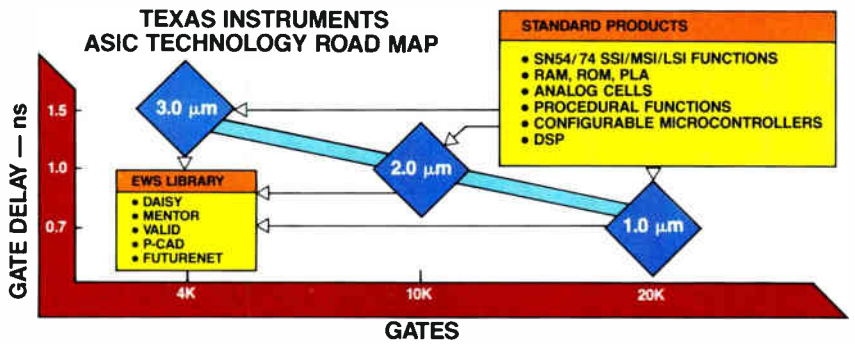
Design your own way

You can reduce your costs and speed your ASIC design with TI because you don't need special proprietary software or design tools. And you can do it at a TI regional design center or at your own work station. Because TI's cell libraries are supported by most work stations, including Daisy LOGICIAN®, MEGALOGICIAN®, and GATEMASTER®; Mentor IDEA 1000®; Valid SCALDsystem®; and P-CAD® and FutureNet® in IBM PC® environments.

TI's worldwide network of 13 training and design centers, staffed with experienced ASIC design engineers, can provide access to work stations, as well as mainframe capability. And you can learn ASIC design in one of TI's unique hands-on workshops. Using TI's semicustom libraries with a real-world standard-cell example, you'll learn every phase of design from schematic capture through test-pattern generation and simulation.

Select TI distributors can also give you local access to TI's leading-edge ASIC options, with dedicated facilities, tools, and trained engineers.

To find out more about what TI ASICs can mean to you, check the appropriate box on the return card.



Advancing technology in ASICs need not demand new rules and tools. Your investment in hardware and training is protected when you move up with Texas Instruments to faster, more complex ASIC functions.

7

New series of input-latched and registered PAL ICs lowers parts counts.

Eight new 30 MHz PAL devices from TI are the first input-latched (TIBPALT19XX) and input-registered (TIBPALR19XX) PAL ICs in the marketplace. Functionally similar to TI's TIBPAL20XX series, they include either 11 D-type transparent latches or 11 D-type input registers on chip. This added circuitry allows you to synchronize inputs without external registers or latches. These devices can reduce your parts counts and simplify your design task in a wide range of applications such as random logic, bus-interface logic, and input synchronization to custom controllers.

8

And now, a new, easy-to-use EPROM microcomputer.

TI's new TMS7742 EPROM microcomputer can cut to zero your lead time for development, prototyping, field tests, and product qualification. And it bridges the gap to ROM-based volume production. For low-volume applications, it can be a cost-effective alternative to mask-programmed ROM. Its 4K bytes of on-chip EPROM are identical to TI's TMS2732A — transferred into the chip area vacated by masked ROM. So if you can program the TMS2732A you can program the TMS7742. This new microcomputer provides EPROM capability for the TMS7020, the TMS7040, and the new TMS7042 ROM microcomputer.

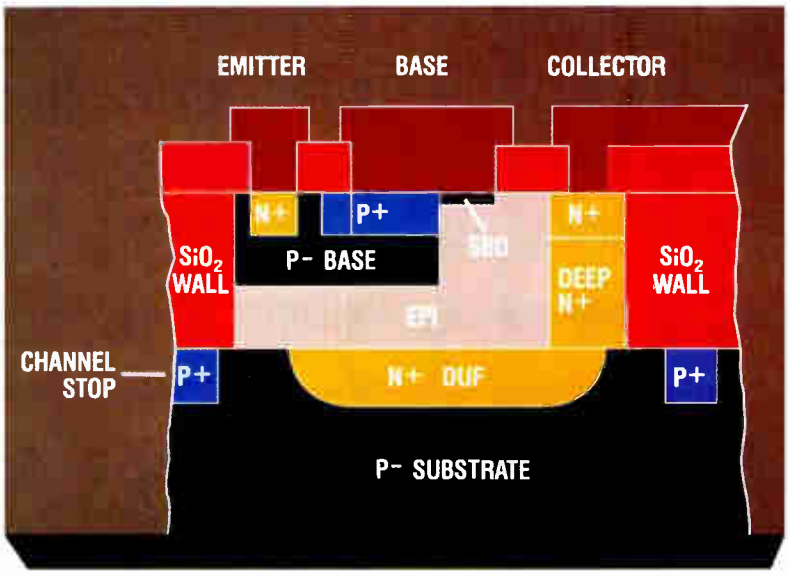
Also new to TI's TMS7000 family is the ROM-less TMS7002 microprocessor. Both the TMS7002 and the TMS7042 feature 256 bytes of RAM, a serial port for USART and serial I/O functions, 32 I/O lines, and three timers. And with their 60% performance increase over earlier TMS7000 ICs, they can improve system performance in such applications as disk and tape drives, printers, and industrial and motor controls.

High-density IMPACT circuits speed logic, memory access.

TI's unique *Imp*lanted *A*dvanced *C*omposed *T*echnology (IMPACT) capitalizes on the advantages of ion implantation, oxide isolation, and composed-masking techniques to increase the speed and density of bipolar ICs.

This innovative technology dramatically reduces the size and the sidewall capacitance of circuit elements (*see diagram*). As a result, speed/power ratios are significantly improved: In PROMs that cut power consumption by 43%, or more than double the speed (*see story opposite*). In PAL ICs that reduce propagation delay by as much as 40% — to only 15 ns at 180 mA.

With the high speed and low power that TI's IMPACT process makes feasible, its potential for large-scale integration will reduce package counts in many high-complexity circuits.



A major reduction in capacitance results from the 2-μm feature size which TI's IMPACT processing makes possible. Silicon dioxide is the isolation material. Switching speed is further enhanced by utilizing this silicon dioxide for emitter and base sidewalls.

Composed masking yields high density

In composed masking, critical components are defined on the chip with a minimum number of masks. Thus they can be more tightly defined and more densely spaced than by conventional masking.

The IMPACT process also makes it possible to insulate critical base and emitter components with oxide walls. This insulation reduces sidewall capacitance, which, at the 2-μm dimensions of IMPACT features, can represent as much as half the overall capacitance. Small size and oxide walling together contribute significantly to the increase in switching speed.

DRAM technology spurs IMPACT growth

The IMPACT process is not a direct descendant of DRAM technology. Nevertheless, TI's commitment to DRAM production has provided IMPACT technology with vital processes.

It was the DRAM effort, for example, that drove photolithography to its present advanced state and contributed key dry-etching processes. Ion implanters designed to produce CMOS DRAM ICs enhance the quality — and the economy — of TI's bipolar IMPACT ICs. And this vital "cross-fertilization" from VLSI memory is one reason Texas Instruments — almost alone among U.S. semiconductor manufacturers — is committed to the development and manufacture of DRAM devices.

◀ **More chips per slice** help cut costs. The 150-mm wafers now used on TI's advanced MOS 256K DRAM wafer-fabrication line have 125% more area than the 100-mm slices formerly used.

8 new ways TI can help sharpen

1

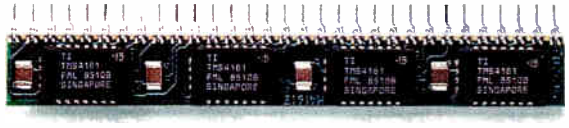
A new alternative for memory-systems design: TI SIP DRAM modules.

Memory-intensive packaging for the future is available today — in TI's highly reliable modules in single-in-line packages (SIPs). With them you can have the many advantages of surface-mount technology (SMT) — while using through-hole-mounted or socketable packages. Thus without changing your manufacturing technology, you can increase memory density by a factor of up to 3.5 over dual-in-line packages (DIPs). And you can simplify board layout while facilitating replacement and future upgrades.

Each SIP module uses DRAM chips in plastic leaded chip carriers (PLCCs), surface-mounted along with decoupling capacitors on an epoxy substrate. Since all connection points are on one edge of the substrate, the module "stands on end" to make the most of your board area.

TI's full line of SIP memory modules — from 64K × 4 to 256K × 9 and 1M × 1 — includes standard DRAMs and Multiport Video RAMs in various organizations. And all are available through your authorized TI distributor.

For more information, just check the appropriate box on the reply card.



Memory can be 3.5 times denser using fully-qualified, production-proven RAMs configured in SIP modules. TI SIPs combine the density of surface-mount technology with economies of through-hole insertion.

2

Interface performance enhanced by TI.

Also new from Texas Instruments is an improved direct replacement for the UCN5812 vacuum fluorescent display driver. TI's TL5812 is 11% faster and draws 60% less current. With an output voltage swing of 70 V and an output source-current capability of 40 mA.

Only TI's patented BIDFET technology — combining bipolar, double-diffused MOS (DMOS) and N-channel and P-channel CMOS transistors on the same chip — makes these improvements possible. And at a competitive price.

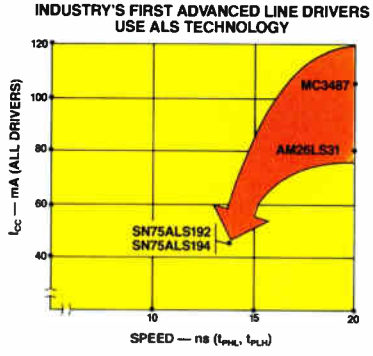
3

Fast line drivers and bus transceivers from TI.

In the new SN75ALS192/194 quadruple EIA Standard RS-422-A differential line drivers, TI's exclusive ALS 1.5 process technology (oxide-isolated Advanced Low-power Schottky) yields the best speed/power ratio in the industry: At approximately half the power consumption, these devices are 30% faster than the competition.

A new family of differential bus transceivers, SN75176B, 177B, 178B, and 179B, are faster than earlier versions. Designed for bidirectional communication on multipoint transmission lines in noisy environments, they meet EIA Standards RS-422-A and RS-485. Typical propagation time is only 22 ns.

Want to know more about these new interface products from TI? Just check the appropriate box on the reply card.



Advanced TI line drivers are 30% faster, typically draw only half the power of the devices they are designed to replace.

4

Fast, economical new 8-bit SAR A/D converters.

Now Texas Instruments offers 8-bit SAR (serial-approximation resolution) A/D converters that are as economical as any you can use. And because they use LinCMOS™ polysilicon-gate-process technology, they are unsurpassed in speed. TI's TLC549 analog-to-digital converter performs 40,000 conversion cycles per second (cps), while the new TLC548 pushes speed to an unprecedented 45,500 cps. At any supply voltage between 3 and 6 V. And typical power consumption is only 6 mW.

Performance of the serial-approximation algorithm is not only fast. It's accurate: Conversions are performed with the guaranteed low error rate of ±0.5 LSB (least significant bit) across the temperature range from −55° to 125°C.

5

681 military TI devices comply with 1.2.1.

Now designers of military electronics have the broadest choice ever of devices that comply with the requirements of MIL-STD-883C, Paragraph 1.2.1. The vast majority of TI's military ICs — 681 different devices — now qualify:

Product Type	Number
ALS/AS	83
TTL	131
LS/S	238
HCMOS	80
PAL ICs	16
Linear	113
Memory/LSI	19
MOS DSP	1
TOTAL:	681

For more detailed information on specific TI military devices, just check the appropriate box on the reply card.

Texas Instruments quality recognized in Tokyo and Detroit.

Outstanding Texas Instruments quality-assurance programs were lauded during 1985 both at home and abroad. In June, Ford Motor Company granted TI linear products the coveted Q1 Award. And in November, TI's wholly owned Japanese semiconductor operation received the prestigious Deming Prize. Both awards recognize exceptional levels of quality and reliability, achieved through aggressive defect-prevention programs.

First Ford Q1 Award to a semiconductor supplier

Ford Motor Company's Q1 Award to Texas Instruments Linear is the first ever to a major U.S. semiconductor manufacturer.

Qualification is based on a demonstrated defect-prevention program, along with Ford's review of warranty returns, specifically keying part numbers to failures. Thus it recognizes both initial product quality and continuing reliability.

Both quality and reliability are attributes that TI Linear has pursued aggressively through its "monitor program," begun in 1979. The goal of the program has been to achieve levels of quality and reliability equal to or better than the best worldwide competition. And the Ford Q1 Award is one visible token of its success.

First U.S. winner of Japan's Deming Prize

At ceremonies on November 11 in Tokyo, the Japanese Union of Scientists and Engineers awarded the prestigious Deming Prize for total quality control to TI's bipolar semiconductor operation in Japan.

The prize, never before won by a wholly U.S.-owned company, recognizes outstanding quality-control achievement in all aspects of business — including marketing, engineering, manufacturing, and support. It is named for W. Edwards Deming, the American statistician whose work in defining and measuring quality control in Japan after World War II became the basis for the legendary Japanese commitment to quality. In 35 years, the Deming Prize has been awarded to only 48 individuals and 111 institutions. Texas Instruments Japan, Ltd. was one of only eight companies so honored in 1985.

As is the case with the Ford Q1 Award, sensitivity to customers' requirements is a key factor in selecting winners of the Deming Prize. TI's successful commitment to quality and reliability in support of all our customers' needs has been demonstrated twice again. And TI is justifiably proud of this achievement.

More news upcoming from TI in the next issue:

- A new CMOS version of TI's trend-setting TMS320 Digital Signal Processor.
- More new additions to TI's growing family of IMPACT PAL ICs.
- New CMOS standard cells and gate arrays that augment TI's leadership in Application-specific Integrated Circuits (ASICs).
- And more ...

For more information...

Check the appropriate square on the reply card, or write **Texas Instruments Incorporated, Department SY093, P.O. Box 809066, Dallas, Texas 75380-9066.**

TEXAS INSTRUMENTS

Creating useful products and services for you.

27-5296

For more information, complete coupon and mail today.

SSY093EC600R

YES. I want more information from Texas Instruments:

DM02	☐ Series 3 IMPACT PROMs	LN05	☐ Low-cost 8-bit SAR A/D converter
DB01	☐ 74AS8838 barrel shifter	GY01	☐ MIL-STD-883-C-compliant ICs
DP02	☐ IMPACT PAL ICs	RL02	☐ Application-specific ICs (ASICs)
MM09	☐ SIP memory modules	PN01	☐ TMS7742 EPROM microcomputer
LL01	☐ Quad RS-422-A differential line drivers and bus transceivers	LD01	☐ BIDFET 20-bit vacuum fluorescent display driver

NAME _____

TITLE _____

COMPANY _____

ADDRESS & M/S _____

_____

CITY _____ STATE ____ ZIP _____

PHONE ____ ____ — _____ EXTENSION ____

Expires August 31, 1986.

For more information, complete coupon and mail today.

SSY093EC600R

YES. I want more information from Texas Instruments:

DM02	☐ Series 3 IMPACT PROMs	LN05	☐ Low-cost 8-bit SAR A/D converter
DB01	☐ 74AS8838 barrel shifter	GY01	☐ MIL-STD-883-C-compliant ICs
DP02	☐ IMPACT PAL ICs	RL02	☐ Application-specific ICs (ASICs)
MM09	☐ SIP memory modules	PN01	☐ TMS7742 EPROM microcomputer
LL01	☐ Quad RS-422-A differential line drivers and bus transceivers	LD01	☐ BIDFET 20-bit vacuum fluorescent display driver

NAME _____

TITLE _____

COMPANY _____

ADDRESS & M/S _____

_____

CITY _____ STATE ____ ZIP _____

PHONE ____ ____ — _____ EXTENSION ____

Expires August 31, 1986.

For more information, complete coupon and mail today.

SSY093EC600R

YES. I want more information from Texas Instruments:

DM02	☐ Series 3 IMPACT PROMs	LN05	☐ Low-cost 8-bit SAR A/D converter
DB01	☐ 74AS8838 barrel shifter	GY01	☐ MIL-STD-883-C-compliant ICs
DP02	☐ IMPACT PAL ICs	RL02	☐ Application-specific ICs (ASICs)
MM09	☐ SIP memory modules	PN01	☐ TMS7742 EPROM microcomputer
LL01	☐ Quad RS-422-A differential line drivers and bus transceivers	LD01	☐ BIDFET 20-bit vacuum fluorescent display driver

NAME _____

TITLE _____

COMPANY _____

ADDRESS & M/S _____

_____

CITY _____ STATE ____ ZIP _____

PHONE ____ ____ — _____ EXTENSION ____

Expires August 31, 1986.

PLACE
STAMP
HERE

Texas Instruments Incorporated
P.O. Box 809066
Dallas, Texas 75380-9066

PLACE
STAMP
HERE

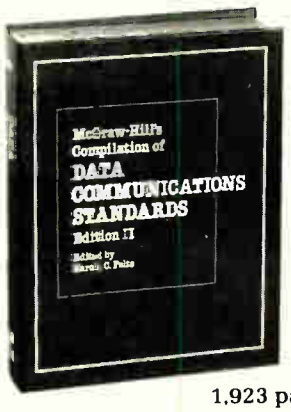
Texas Instruments Incorporated
P.O. Box 809066
Dallas, Texas 75380-9066

PLACE
STAMP
HERE

Texas Instruments Incorporated
P.O. Box 809066
Dallas, Texas 75380-9066

NEW EDITION

All standards are new, revised, or reaffirmed since the previous edition



1,923 pages
illustrated
Edited by Harold C. Folts

DATA COMMUNICATIONS STANDARDS

All 123 interface protocol standards set by:
- CCITT • ISO • ECMA
- ANSI • EIA
- U.S. Government

Special feature for instant access to the applicable standards:
Cross-reference tables of the similar and interfacing standards of each standards organization.

Electronics Magazine Books
P.O. Box 541
Hightstown, NJ 08520
609/426-5070

Please send _____ copies of R100-*McGraw-Hill's Compilation of Data Communications Standards Edition II* at $295 each.

Name

Title

Company

Address

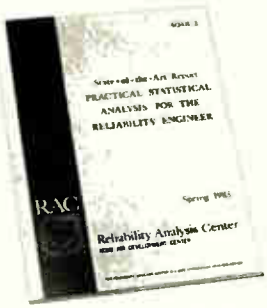
City/state/zip

U.S. customers please add local sales tax. McGraw-Hill pays regular shipping and handling on prepaid orders.

DCT

When talk turns to STATISTICS, are you STUMPED ?

"Practical Statistical Analysis for the Reliability Engineer."



- **A complete state-of-the-art report to meet the statistical needs for the engineer dealing with reliability problems. Easy to understand and interesting to read.**

"COVERS"

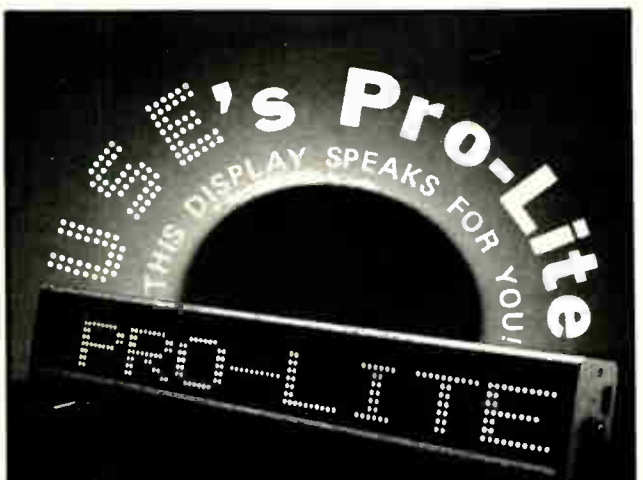
- **Hypothesis Testing**
- **Correlation Coefficients**
- **Confidence Intervals**
- **Weibull Plotting**
- **Analysis of Variance**
- **Goodness of Fit Tests**
- **Sampling Inspection**
- **Bayesian Statistics**
- **Regression Analysis**
- **PLUS MUCH MORE.**

- **Order No. SOAR-2 $36. per copy ($46. Non-US) Prepaid**

RAC
Reliability Analysis Center
RADC/RAC • Griffiss AFB, NY 13441 • Tel. (315) 330-4151; Autovon: 587-4151

RAC is a DoD Information Analysis Center Operated by IIT Research Institute

Circle 43 on reader service card



- Good quality and low expense
- Get more customers, more customer satisfaction and loyalty.
- Brings you more sales, more profits, reduced costs overall.
- Lets your customers bear in their minds what your display in your store.
- Easy to program the message your want.

U-SUN ELECTRIC CO., LTD.
P.O. Box 4–12, Pan Chiao, Taiwan, R.O.C. Tel: (02) 952-3333 (6 Lines)
Telex: 33247 USUNE Cable: "USUNE" Taipei

Circle 81 on reader service card

SUPERCOMPUTERS HIT THEIR STRIDE

It was 10 years ago this month that Seymour Cray ushered in the era of the vector supercomputer. His company, Cray Research Inc., delivered the first of the giant superfast machines, the Cray-1, to Los Alamos National Laboratories in March 1976. He spawned an industry that is growing explosively and that continues to break ground in the critical technologies of architecture and circuits, packaging and cooling, and software.

Ten years ago, it was generally thought that the total market for such big, expensive machines would be just a handful of systems. Now it looks like a boom market.

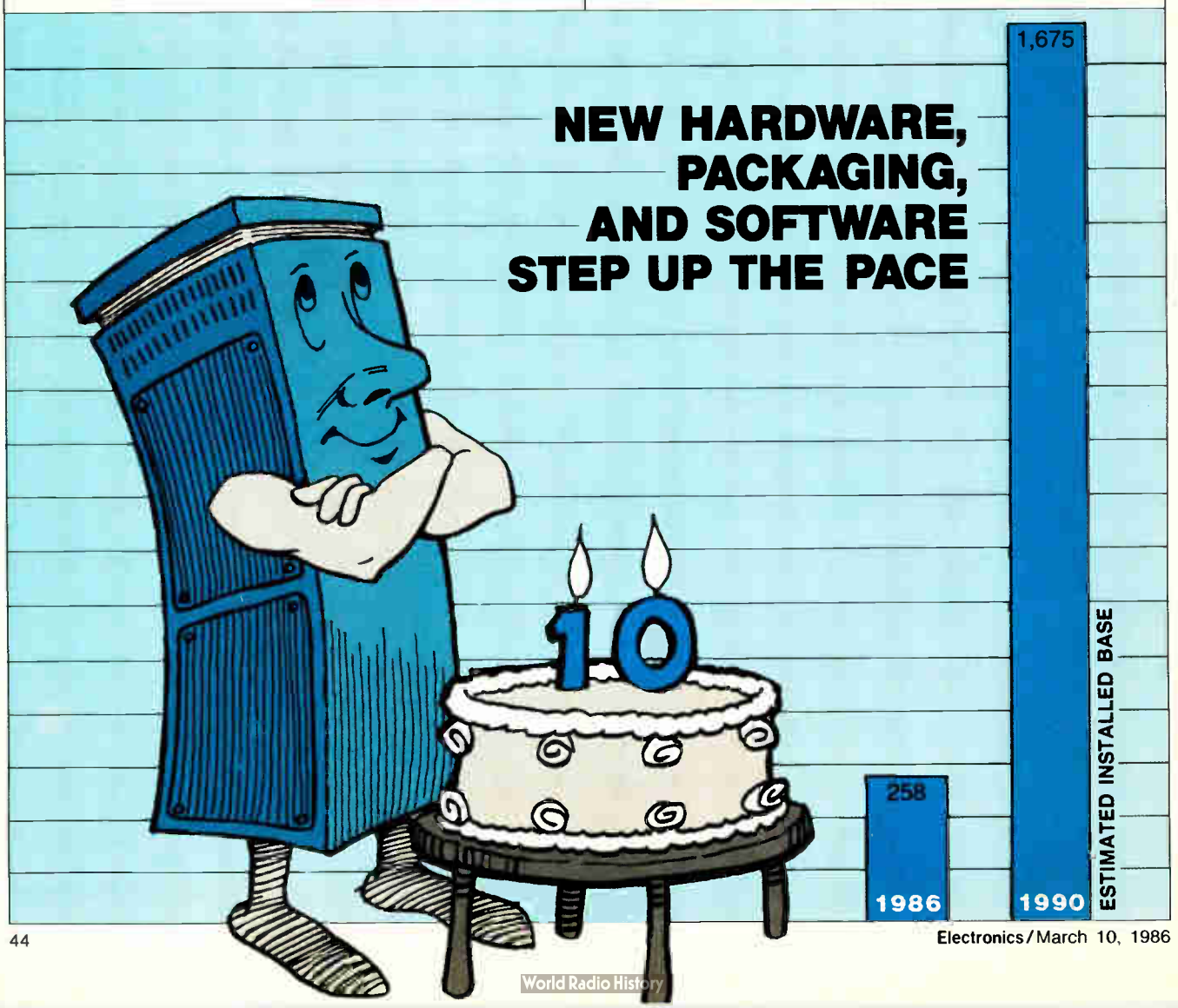
The impetus for the boom is the need for lots of fast computation. The price/performance ratio of supercomputing has been rising, making it more attractive. Another spur is the new class of minisupercomputers, which has reduced the entry-level cost of supercomputing.

A recent report from the research department of Sanford C. Bernstein & Co. forecasts annual growth of 60% in system installations and 45% in system value through 1990. The New York broker figures that the worldwide supercomputer installed base at the end of 1985 was 165 machines. It is projecting growth to 258 in 1986 and to 1,675 by 1990 (chart). Not only is supercomputing becoming big business, but the number of new companies offering more machines in the supercomputer range is increasing considerably.

The supercomputer market is showing signs of greater complexity, as many new companies enter with new supercomputers, minisupercomputers, or parallel computers. The world's supercomputer makers are Cray, ETA, CDC, Fujitsu, Hitachi, and NEC.

The industry leader, Cray Research, Minneapolis, has an estimated 70% of the market, with about 116 systems installed. Second place belongs to the other U. S. maker, ETA Systems Inc., St. Paul, Minn. ETA, a Control Data Corp. spinoff, now sells CDC's Cyber 205 (about 40 installed) and will introduce its own machine, the ETA[10], later this year. CDC is still a player, and IBM Corp. has recently joined the ranks with add-on vector processors for its 3090 mainframe computers [Electronics, *Feb. 3, 1986, p. 35*].

In Japan, the three major computer companies, Fujitsu, Hitachi, and NEC, all of Tokyo, now make supercomputers. NEC Corp. has orders for five systems—four in

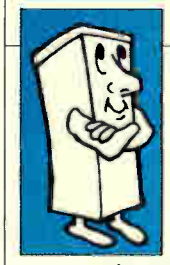


Japan and one in the U.S., and Hitachi Ltd. has received nine orders. France will be getting into the act, too; Bull SA is preparing to enter the commercial market this year.

The rising price/performance ratio in supercomputers stems from the ever-greater performance levels of these machines. So several new vendors are rushing to improve the other side of the equation, with minisupercomputers that deliver less performance but also cost far less. Convex Computer Corp., Richardson, Texas, has been shipping its minisuper since September 1984 and has installed more than 80 systems worldwide. Floating Point Systems Inc., Beaverton, Ore., was second into the market, and Alliant Computer Systems Corp., Acton, Mass., markets a multiprocessor vector machine. Culler Scientific Systems Corp., Santa Barbara, Calif., recently introduced its first model [Electronics, *Nov. 25, 1985, p. 43]. *Scientific Computer Systems Corp. of Wilsonville, Ore., has just introduced a Cray-compatible minisuper, and Vitesse Electronics Corp., Camarillo, Calif., is developing a family of high-speed numerical computers targeted for 1987.*

PARALLEL DESIGNS ARE MAKING INROADS

by Tom Manuel



There's a revolution brewing in supercomputers, pitting the classical von Neumann architecture against parallel configurations. Parallelism is making inroads in all sizes of computers, but the greater throughput it promises is especially critical in supercomputing.

The main thrust in supercomputer architecture to date has been to build the fastest possible vector processor for single- or dual-processor supercomputers. The dual-processor models often team a superfast vector processor with a general-purpose scalar processor. Although many configurations may have only one vector processor, that processor is often highly pipelined for concurrent vector processing. But now there is a clear trend toward multiple-pipeline vector processors and even multiple vector processors in order to boost throughput even higher. For example, Cray is delivering four-processor machines—both X-MP/48 and Cray-2 models—and Alliant is delivering its FX/8 supercomputer with up to eight vector processors [*Electronics*, July 29, 1985, p. 56].

1. PARALLEL POWERHOUSE. CDC's Cyber Plus is a powerful parallel computer.

Machines with more parallelism are on the drawing boards. The upcoming Cray-3 will have up to 16 processors, and the ETA^{10} computer will have up to eight processors. New, highly parallel architectures, such as the one developed by Flexible Computer Corp., Dallas, will be getting add-on vector processors in the near future.

The Japanese supercomputer companies, though relatively new to the supercomputer scene, are talking about parallel architectures, too. A representative of Hitachi agrees that parallel processing in supercomputers is definitely a trend. "Parallel processing becomes more necessary with the passage of time because the speed increase provided by improved hardware technology is only about a factor of two every four years," he says. A representative of NEC says that his company intends to incorporate parallel processing in its future supercomputers and to develop higher-speed single-processor hardware.

France will be the first Western European country with a supercomputer company. Bull is starting with a simple architecture that combines a scalar processor with a vector processor. It is to be a top-level machine with some parallel processing included.

Cray, the world leader in supercomputers, is pursuing five development efforts, according to president John Rollwagen. Two of them are the enhancements to the X-MP and Cray-2 systems. In addition, three new machines are being designed. One may be introduced this year: the Y-MP, whose architecture is similar to that of the X-MP. The Y will be able to run with up to eight processors—the X has a maximum of four.

The second new machine will be the Cray-3, which is to be largely compatible with the Cray-2 but with about 10 times the performance. The Cray-3 will have up to 16 processors, with the processor logic and some of the critical memory parts made from the gallium arsenide integrated circuits the company is developing. The third project, just started, is an unnamed and as yet undefined system that probably will have more parallel processors than any of the others and is likely to deliver around twice the performance of the Cray-3.

BEST CHOICE IS BOTH

There is a controversy between those companies that push very fast single processors and those that champion a multitude of multiprocessor approaches, according to Stephen Nelson, Cray's director of research. "The best is to have both," he says. Cray started by pushing the limits of single-processor speed. It still does that, but lately it has been pushing multiprocessing as well. "We are rapidly coming up against a brick wall" in the ability to increase the speed of single processors, says Nelson. "It is inevitable that supercomputers go to multiprocessing."

Another architectural trend is very large main memories directly addressable by the CPU. One example is the Cray-2, with its 2,048 megabytes (256 megawords) of real memory. In fact, a single Cray-2 has more memory than there was in all previously sold Cray machines put together.

The ETA^{10} will be structured with up to four pairs of very fast processors. Each processor, which will be immersed in

liquid nitrogen to speed up its CMOS circuits, will be complete on a single board and will deliver performance two to three times that of a Control Data Cyber 205. The ETA[10] will be architecturally compatible with the Cyber 205 and will eventually replace it in the marketplace.

Control Data has been in the large-computer business from the beginning. Its backing of ETA Systems is a commitment to making the biggest supercomputers, while its separate development of the Cyber Plus parallel computer is a similar commitment to top-end parallel processing.

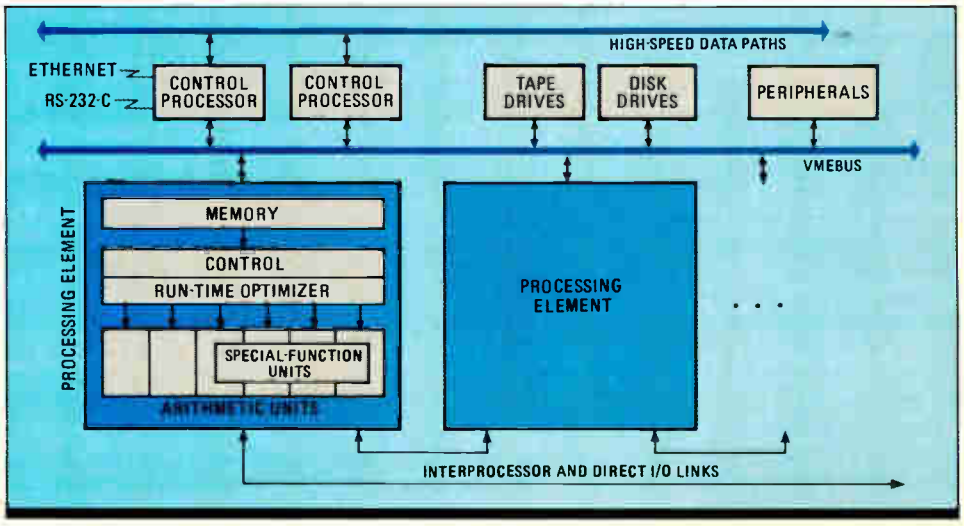
The Cyber Plus is a ring structure of 21-ns processors that connects to a Cyber 180 mainframe as a front end and through networks to other computers (Fig. 1). With the ring architecture (in contrast to a bus structure), every time the number of processors is increased, the total data bandwidth is increased: more processors mean more pathways for data, which increases the system bandwidth. The system has three levels of parallelism—within the processors themselves, multiple Cyber Plus processors on the ring, and parallel operation between the Cyber 180 and the Cyber Plus processors.

All of the action in supercomputing is no longer limited to the biggest, fastest, and most costly machines. A new class of minisupercomputers has emerged in the last couple of years that offers lower levels of performance at very much lower prices. For example, Scientific Computer Systems has just announced the newest minisupercomputer entry (p. 69). Its 64-bit scientific computer offers entry-level supercomputer performance at a moderate price—25% the performance of a Cray X-MP/1 at 10% of the cost. The SCS-40, a minisupercomputer, uses the Cray X-MP instruction set plus the Cray time-sharing operating system and vectorizing Fortran compiler to run over 200 applications developed for Cray X-MP machines.

One trend: huge main memories that the CPU can address

Another company developing a new minisupercomputer is Vitesse. Its Vitesse Numerical Processor, or VNP, is designed for multiprocessor operation. The architecture will also include many gigabytes of memory; each processor will have attached memory. There will be no global, shared memory per se, nor a shared bus. However, selective memory sharing will be available to all processors through a system of buses for which the company has applied for patents (Fig. 2). The architecture is not limited to a specific number of processors. "Processor types other than vector number crunchers, such as data-base or Lisp processors, can be integrated on the VNP non-bus," says Allan Eddwin, president of Vitesse's Digital Products Division.

The massively parallel architecture of the Flex/32 computer from Flexible Computer Corp., Dallas, is designed to add large numbers of different processors for different functions [*ElectronicsWeek*, May 13, 1985, p. 49]. The company recently won a research grant from the National Aeronautics and Space Administration to develop a 32-bit vector processor for the Flex/32 architecture. Because many supercomputing tasks do not require the precision of 64 bits, and because high throughput can be achieved with the Flex/32 parallel architecture, a lower-cost 32-bit supercomputing processor will fill the bill for many applications. The first supercomputing processor for the Flex/32 will be on one board, perform both 32- and 64-bit arithmetic, have more than 1 megabyte of static random-access memory, run at 12 million to 15 million floating-point operations per second (delivering a net performance of about 10 megaflops in parallel operation). It will be formally announced by about midyear. Users will be able to gang as many as they need to get the performance they want.



2. FAST ONE. The Vitesse Numerical Processor under development will be fast, especially when it gets a boost from GaAs chips.

ADDING NETWORKS

To get the most performance out of a supercomputer, users are discovering the value of installing them in a hierarchical network containing minisupercomputers and engineering work stations. Steve Wallach, vice president of technology at Convex, the first company to introduce a minisupercomputer, speaks of a three-tiered hierarchy of machines, with the big supercomputers, mainframes, and application-specific black boxes at the top. These are connected to the next layer of minisupercomputers through a fast local-area network such as a Hyperchannel from Network Systems Corp., Minneapolis. On the lower level are work stations connected to the middle level by an Ethernet.

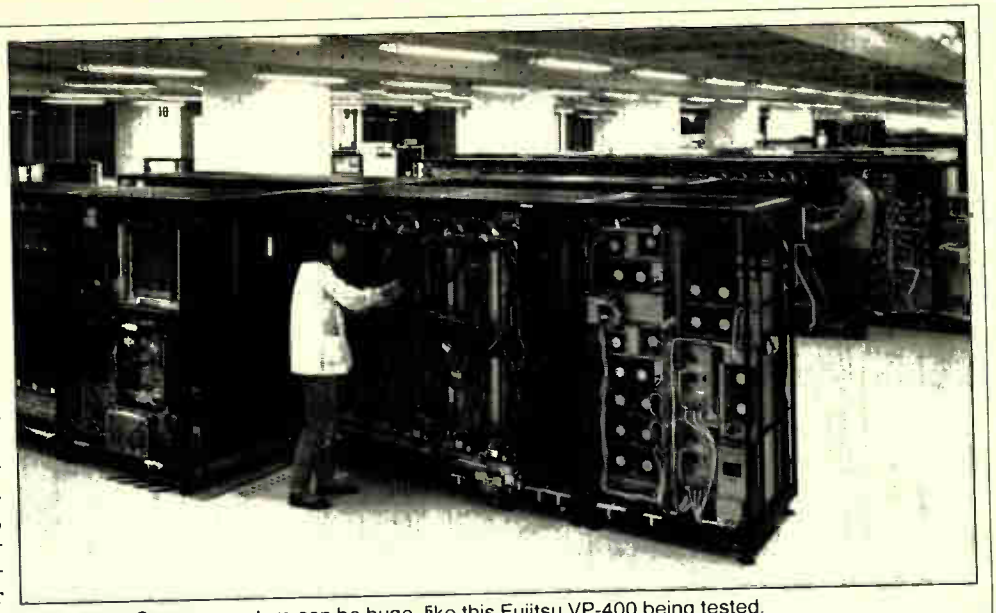
This machine hierarchy "comes from the hierarchy of needs in most organizations," says Wallach. Powerful work stations are replacing terminals for many users. Minisupercomputers such as Convex's C-1 Cray-like minisupercomputer will be installed as department computers, both for new departmental installations and for replacing existing departmental minicomputers that have run out of gas. Many medium-size and most large organizations need one or more large computers available to the whole organization for big applications.

Frank S. Greene Jr., president of ZeroOne Systems Inc., Santa Clara, Calif., agrees that the new minisupercomputers are important in the supercomputing hierarchy. His company is packaging the Convex C-1 with very high-performance disk drives from Ibis Systems Inc., Westlake Village, Calif., more Cray compatibility (through a Cray Fortran preprocessor and Cray object-code generation by the Fortran compiler), and a high-speed Hyperchannel link between the C-1 and the Cray to offer front-end systems to large Cray computers. Work stations tied to the C-1 can be used to offload short jobs and software development from the Cray to the minisupercomputer, freeing the big machine for the big jobs. For many short jobs, the C-1 will provide a much faster turnaround, even though it takes longer to run the job; on a heavily loaded Cray, the short job could wait a long time to run.

The Japanese lineup of supercomputers begins with Hitachi, which now has three separate supercomputers: the S-810/20,

rated at 630 megaflops; the S-810/10, at 315 megaflops; and the S-810/5, at 160 megaflops. The computers consist of scalar processors with pipelined vector processors, and the number of vector processors can be expanded. The scalar processor has an architecture similar to the IBM Corp. 370. Hitachi will continue with this type of architecture for at least three to five years.

NEC offers two supercomputers, the SX-1 and SX-2, that also incorporate a scalar control processor and a vector processor. The scalar processor has a small number of instructions, making it a type of reduced-instruction-set computer. The instructions are hardwired rather than in microcode.



3. BIG ONE. Supercomputers can be huge, like this Fujitsu VP-400 being tested.

"The RISC concept is important because it is needed for scalar speed. Thus it should not be considered a fad but an important design trend," says the NEC representative.

Because it is difficult to adapt software to a parallel architecture, NEC engineers are going all out for the highest possible scalar speed in a single processor. The speed of the SX-2 on the loop benchmark for measuring floating-point computational performance, developed by the Lawrence Livermore Laboratory in California, is 286 megaflops. The Hitachi 810/20 has been benchmarked on the Livermore loop at 100 megaflops, while Fujitsu Ltd.'s VP-400 turned in 161 megaflops on the same test.

Fujitsu's supercomputer offering goes from the VP-50 to the VP-400 (Fig. 3). Fujitsu's supercomputers have a complex-instruction-set-computer architecture consisting of a general-purpose scalar processor plus multiple pipelined vector processors to counter the limited capability of this vector processor design. From the user's viewpoint, the collection of vector processors appears to be a single processor. The VP-200 has two vector processors, and the VP-400 has four.

Meanwhile, the only Western European commercial supercomputer is being developed in France. Bull began its Isis supercomputer program in 1984 as a noncommercial venture aimed at gaining French national independence in the strategically essential area of supercomputers. But because of the program's progress, Bull will turn the project into a commercial product when the first prototype of the Isis machine is completed by the end of this year.

Isis will be a 1-gigaflops computer, essentially for military applications. Bull plans to continue research on a second generation of the machine with significantly improved performance.

Bull is relying on an architecture that, despite its relative simplicity, takes advantage of vector, parallel, and scalar processing. All the machine's components can be found on the commercial market. Isis consists of a two-part central processing unit—a scalar part and a vector part. The machine also has three memory modules, a main memory controller, and two dedicated-connection interface devices to connect main memory to the CPU and the secondary memory unit (Fig. 4).

The CPU is composed of four identical and independent scalar data paths. Under program control, the data paths either execute scalar instructions or assign vector processing to the vector unit. Therefore, the CPU can execute four scalar tasks and one vector task in parallel. Each of the scalar data paths has its own integer and floating-point calculation units, 256 general registers with three simultaneous accesses, and an instruction cache for 256 instructions, which permits automatic anticipation of changes in instructions and advance preparation of linkages between instructions. The large number of general registers associated with a reduced instruction set optimizes performance of the machine by reducing the number of necessary memory-access operations.

GaAs circuits are being developed for the Cray-3

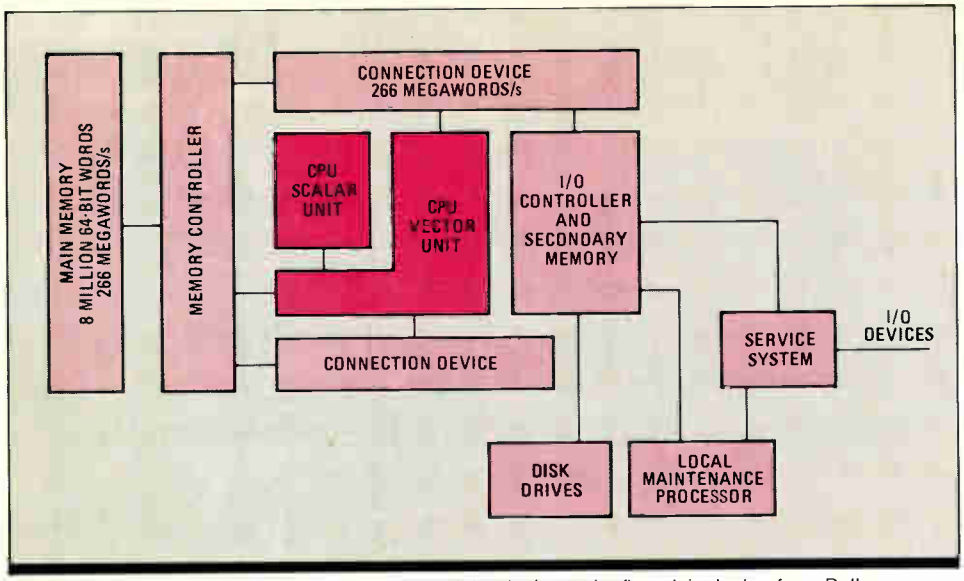
The need for the fastest processors possible in supercomputer design is one of the main drivers of the most advanced circuit-technology research and development [*Electronics*, Sept. 9, 1985, p. 92]. The U.S. supercomputer makers are working closely with IC companies to develop faster and denser bipolar ICs, very highly integrated CMOS gate arrays that can be further speeded up by supercooling, and fast GaAs circuits. The Japanese supercomputer companies have their own very advanced circuit-development operations and are looking at similar technologies for the future.

Cray has established IC development and fabrication facilities and is developing GaAs circuits for the Cray-3. In its prototype GaAs line, it has produced logic chips of several hundred gates, as well as special memory chips containing 512 and 1,024 bytes on 3-in. wafers. Cray is working with GaAs IC vendors such as GigaBit Logic Inc., Newbury Park, Calif., to fabricate the same designs. "The Cray-3 will require a large number of logic designs—over 100, maybe 150," says Nelson.

Cray is using first-generation GaAs—depletion-mode metal semiconductor FETs. The Japanese companies, as well as Vitesse and Ford Microelectronics in the U.S., are working on enhancement/depletion-mode devices. The Colorado Springs microelectronics division of Ford Motor Co., now selling 500-gate depletion-mode logic arrays and 1-K SRAMs, is developing 500-gate enhancement/depletion-mode arrays for supercomputers.

Cray's 300- to 500-gate logic chips will be made in a variety of speeds because it is possible to trade speed for lower power. The fastest chips will be developed for the most critical parts of the machine. The target speed of the processor is a 2-ns clock speed versus the 4-ns Cray-2 speed. The Cray-2 and X-MP computers are made from 21 to 22 types of 16-gate emitter-coupled logic devices.

Cray has built and tested a number of fully functional 1-K GaAs memory chips (that is, all bits work). These chips will be used in local processor memory where speed is essential, such



4. FROM FRANCE. The French supercomputer debut is the 1-gigaflops Isis design from Bull.

as in vector registers and caches. The very large main memory for the Cray-3 will still be made of silicon.

Although Nelson foresees a big future for GaAs, the company is not abandoning silicon-based logic circuits; it has installed facilities for developing those, too. For example, ECL gate arrays with about 2,000 gates (better than two orders of magnitude denser than the 16-gate parts now used) are being developed for the Y-MP computer.

Silicon remains the semiconductor of choice at neighbor ETA Systems. But ETA is shifting from bipolar to CMOS. In conjunction with Honeywell Inc.'s Digital Product Center in Colorado Springs, ETA has developed a 20,000-gate CMOS gate array that it will operate at 77 K. All 92 gate-array design options required have been designed and are in the production pipeline, and most of them have been returned and fully tested [*Electronics*, Feb. 10, 1986, p. 9].

"These arrays will be the sole logic component on the processor board," says Dave Resnick, senior technologist. The chips will also be used in other parts of the machine, where they are applicable—for example, in memory control, I/O, and the clock distribution network. But because the chips also operate well at room temperature, only the CPU boards will be immersed in liquid nitrogen.

One other U.S. supercomputer company, Vitesse, is working on GaAs circuits for its machine. The VNP computer will first be implemented in silicon, but as the GaAs circuits are developed, they will be built into the processor to improve performance. In this architecture, each functional unit runs at its own speed, so it does not have to be redesigned to use faster GaAs in some units. The system is synchronized by one master clock.

For the present, Japanese companies are sticking with silicon technologies. Today's Hitachi supercomputers use ECL gate arrays with up to 1,500 gates, the same devices used in the company's M-280H mainframe computers. Hitachi's later M-680H mainframes use ECL arrays with 5,000 gates [*Electronics Week*, March 18, 1985, p. 16], and the use of these circuits is a distinct possibility in Hitachi's next supercomputer, expected soon. Both gate arrays and custom circuits are now being used, but the trend is toward more gate arrays. Logic-in-memory chips are used for the scalar cache. For the future, GaAs and high-electron-mobility transistors appear attractive, but silicon keeps improving and will remain a contender.

NEC now uses low-power current-mode-logic 1,000-gate arrays that dissipate 5.5 W. Custom chips are also used. Dissipation of the 36-chip modules is slightly more than 200 W.

Fujitsu's supercomputers are built around 1,300-gate custom circuits and 400-gate ECL gate arrays with a propagation-delay time of 350 ps. ECL RAM is used for cache; main memory is 64-K n-MOS SRAM with an access time of 55 ns. Systems to be sold five years from now probably will use ECL in the form of higher-density gate arrays.

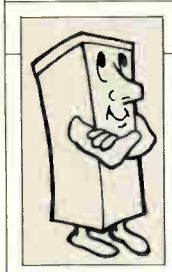
Fujitsu undoubtedly will continue to use the same type of highly integrated devices, where the trend is to 3,000- and 10,000-gate devices, that it developed for its general-purpose mainframes and will be using in its supercomputers.

Circuit hardware for Bull's Isis CPU consists of ECL gate arrays with densities of 2,000 gates, which could be increased to 8,000 or 10,000 gates within the next couple of years. There are no full-custom ICs in Isis, nor are any planned. ICs in the primary system memory are SRAMs with a cycle time of 35 ns; in the secondary system memory are dynamic RAMs. □

Additional reporting was provided by Charles L. Cohen in Tokyo and Robert T. Gallagher in Paris.

SUPERCOOLING COMES TO THE FOREFRONT

by Jerry Lyman



More than ever, the design of supercomputers turns on devising a way to cool the superfast machines. It's still important to select a high-density high-speed IC package, design a controlled-impedance, state-of-the-art, multilayer printed-circuit board, and figure out how to interconnect all circuitry with a minimum of propagation delay, reflections, and crosscoupling. But tomorrow's systems could dissipate as much as 100 kW, and so cooling is even more critical than in today's supercomputer designs.

Not surprisingly, the leading supercomputer maker, Cray, is also a leading innovator in supercomputer packaging. The company's first units, the Cray-1 and X-MP, are based on relatively simple ECL small-scale-integration chips in ceramic flatpacks mounted on 6-by-8-in., five-layer pc boards. Vertical Freon-cooled aluminum columns carry away the heat generated by horizontal stacks of pc boards.

For Cray's next system, the Cray-2, the company went to a completely new design for packaging and cooling. Instead of a horizontal stack of boards, Cray used an even denser three-dimensional cube of slightly smaller circuit boards, which raised the power-dissipation level above that of the Cray-1.

To take care of this power increase, Cray decided to immerse all boards in Fluorinert, an inert cooling fluid from 3M Co. This fluid is kept circulating across the boards, keeping critical components at a uniform and safe temperature.

High heat-transfer rates enable the cooling fluid to remove

heat rapidly, which allows components to be spaced very close together without a sacrifice in reliability. This close spacing allows for very short signal paths, which increase operating speeds.

Cray is in the midst of developing its fastest and most advanced systems yet—the Cray-3, based on GaAs ICs, and the Cray Y-MP, based on ECL ICs. "For the Cray-3, we are still in the experimental stage and final details have not been determined," says Cray's Stephen Nelson. "We are still working on assembly techniques. Packaging will involve a surface-mount kind of technology. We are heading in the direction of 3-d packaging and immersion cooling somewhat like the Cray-2."

He says the company wants to improve the circuit density, however, and intends to shrink everything it possibly can—the line widths on pc boards and so on. The power density on the Cray-3 will be higher than on the Cray-2 because of the circuit density, and he predicts that the big challenge will be cooling.

"The Cray X-MP is not immersion-cooled," Nelson points out. Like the Cray-1, the X-MP uses aluminum column bars with Freon. "The cooling for the follow-on to the X-MP, the Cray Y-MP, has been defined, but we are not ready to disclose details yet. However, it won't be an immersion-type cooling.

"The Y is much further along in development than the 3. This system is targeted to be an eight-processor system. It will have a flatpack type of packaging. It will be similar to the X, yet it still will be different. The power density on the Y is not as great as the Cray-2 because we are using much larger circuits and therefore there is less I/O on and off the chips. Therefore it is unnecessary to immerse the Y," says Nelson.

SUPERCOOLING WITH LIQUID NITROGEN

ETA Systems, Cray's main U. S. competitor, is building its ETA[10] supercomputer based on 20,000-gate CMOS gate arrays cooled by liquid nitrogen. The CPU boards will be sealed in cryogenic containers through which liquid nitrogen will be pumped. This cryogenic environment serves both to carry away heat and to supercool the chips for higher operating performance.

The main building block of the ETA[10] processor is a board of about 40 layers containing nothing but the 20,000-gate CMOS gate array that was designed by ETA and fabricated by Honeywell. At 16 by 20 in., the state-of-the-art board provides plenty of room for 250 chips. The CPU will require about 240 chips, the company says.

The board's controlled 50-Ω impedance, which allows the board to act as a transmission line, is achieved by keeping board edges as clean as possible. This may be one of the first uses of a 50-Ω system with CMOS.

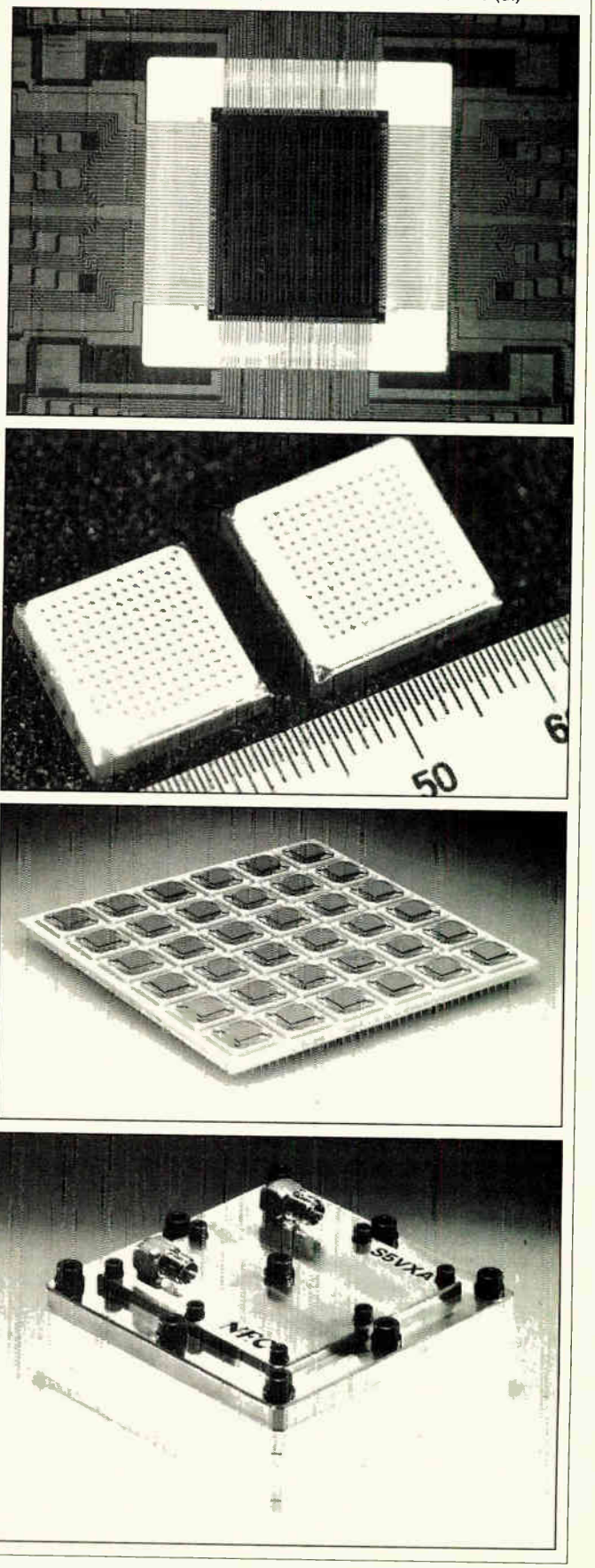
"The next step in circuit density for ETA will require a careful decision on just how far to go," says Tony Vacca, the company's director of technology concepts. "Packaging constraints will be the biggest issue. The first-level packaging will be the biggest concern. Memories present no problem. Microprocessors' pins can be multiplexed. But in supercomputers, you can't multiplex—too slow. So you have a problem with requiring lots of pins for the very dense circuits. We will look for a proper balance between not enough gates versus not enough pins—at least until we have 3 million gates and 1,000 pins in one chip."

In Japan, the other main participants in the supercomputer competition—Hitachi, NEC, and Fujitsu—all take different approaches in packaging their supercomputers.

Hitachi's supercomputer packaging is similar to that used in its M-280H mainframe computer, but vector registers are added to the second side of the circuit boards of the vector processors to minimize propagation delays.

The basic package used in the scalar processor is a ceramic flatpack with leads on four sides. Hybrid modules with ceram-

5. SUPERCOMPUTER PACKAGING. In NEC's latest supercomputer, TAB gate arrays (a) are placed on special bumped chip carriers (b), which in turn go on a large multilayer ceramic substrate (c). This package is then housed in a special water-cooled module (d.)



ic chip carriers on both sides of a ceramic substrate are used for the main memory. Pinout of this module resembles a modified pin grid array because there are four rows of pins—along two opposite outside edges—and two more rows of pins parallel to those along the outside edges but running between the columns of chip carriers. (A full pin grid array is not possible with chip carriers on both sides of the substrate.)

The vector register hybrid modules consist of ceramic chip carriers with radiator fins on one side of the ceramic substrate. The substrate has flatpack-type gullwing leads on all four sides.

NEC's SX-1, SX-2, and SX-1E have the most advanced supercomputer packaging in Japan. They combine tape-automated-bonded low-power CML gate arrays, composite multilayer polyimide/alumina substrates, and water cooling [*Electronics*, Nov. 11, 1985, p. 26]. Low-power CML gate arrays with 1,000 gates are bonded into special bumped leadless carriers (Fig. 5). These, in turn, are mounted on special 10-cm^2 ceramic/polyimide multilayer substrates, with a pin-grid-array format, that hold 36 of the bumped chip carriers. These assemblies are then mounted in special water-cooled modules. This arrangement cools the 200-W modules and minimizes wiring lengths and propagation delays.

In Fujitsu's Facom VP series of supercomputers, logic chips are housed in leaded chip carriers with cylindrical heat sinks. For memory, special leaded chip carriers hold four high-speed RAM chips, each with its own cylindrical heat sink. The logic and RAM modules are mounted on a large (30-by-30-cm) multilayer pc board called a multichip carrier.

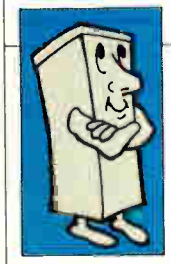
A maximum of 13 multichip carriers can be installed in one carrier stack, forming a cube of about 50 cm. All these features help the vector unit operate at a machine cycle of 7.5 ns.

The Facom VP series is now air cooled. Fujitsu's next-generation supercomputer may go to a one-board system, as did its recently announced M-780 mainframe. This will increase the thermal density and will force Fujitsu to convert to liquid cooling of the single large board, as it did on the M-780. □

Additional reporting was provided by Charles L. Cohen in Tokyo.

FULL SPEED AHEAD FOR SOFTWARE

by Alexander Wolfe



Supercomputing software is moving into high gear, spurred by the rapid spread of supercomputers into new applications. The critical challenge is how to develop tools that will make it easier for programmers to write applications that take advantage of vectorizing in the classical supercomputer and the parallelism that is emerging in supercomputers and minisupercomputers. Writing parallel software is a challenge that every programmer must face because parallel architectures are springing up across the range of computing.

"In the supercomputer arena, software has not been keeping pace" with the hardware, says David Kuck, director of the University of Illinois Center for Supercomputing Research and Development (Fig. 6). Illinois is one of the hotbeds of supercomputer software research, along with Cray, Cornell University, and IBM. "I think we're just all starting to learn—I guess I would put it in the infancy stage," says Margaret Loftus, vice president of software at Cray. "We have so much horsepower available. The ease with which we can put it at the programmer's fingertips is going to make all the difference."

Cray is developing a host of tools for programmers. Tools to support multitasking (in supercomputer parlance, multitasking means dividing up a single program to run on multiple processors) are high on Cray's agenda. "Our aim is to make things as automatic as possible," explains Loftus.

On tap for multitasking is Premult, dubbed a microtasking tool. As a preprocessor for Cray's CFT77 Fortran compiler, Premult will provide fine-grain multitasking: "Much of the multitasking done today has been done at a very high level—big chunks of code which run on multiple processors. Microtasking will break programs into pieces smaller than a [small] subroutine," says Loftus.

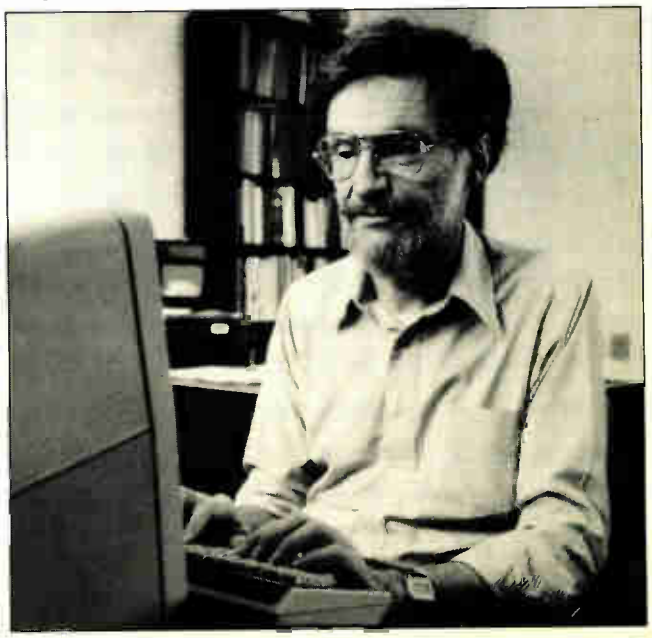
Cray's current lineup of tools includes Flowtrace, an analyzer that logs information on where a program spends its time, an important aid during debugging. Also available is the CFT compiler, a vectorizing compiler for the Cray-1. Vectorization lets the applications software take advantage of the vector hardware in a machine, using it to rapidly execute program loops containing large arrays of data.

Cray is also at work adapting existing operating systems, subroutine libraries, and compilers from the Cray-1 to its other machines. Within the next few months, Cray will release its Unix-like Unicos operating system and the CFT77 Fortran compiler in versions running on Cray X-MP and Cray-2 hardware (Fig. 7).

At Cornell University's Center for Theory and Simulation in Science and Engineering in Ithaca, N. Y., supercomputing research centers on an IBM 3084-QX mainframe with four processors, to which four Model 264 array processors from Floating Point Systems have been attached. Over the next six months, the Theory Center will be adding software for multitasking on the system, according to director Kenneth Wilson.

"Here, the emphasis will be more on taking old, dusty decks [existing programs], and taking advantage of opportunities for small-scale parallelism that don't require wholesale rewriting of these decks—doing the sort of thing where you discover that your whole program has four parts which can run in four processors, or that there's one outer loop which you can divide among four processors," says Wilson.

6. LEADING THE WAY. David Kuck of the University of Illinois is one of the guiding lights in software for parallelization and vectorization.



The objective is to move the technology out of the lab. "We will make a major effort to try to get actual scientists using these systems and starting to change their thinking, not just the people writing systems software. Part of our plan has been to have big iron which we put the scientists on and get them to see that parallelism has a real advantage for them," Wilson explains.

STARTING OUT IS HARD

One big hurdle facing any new venture in supercomputers or minisupers is developing a software base. Some idea of the effort it takes comes from IBM's experience in preparing programming languages and development tools for its recently introduced 3090 Vector Facility. Software engineers at IBM's Kingston (N. Y.) Laboratory prepared a new version of the IBM VS Fortran compiler to add automatic vectorization. Other major efforts at Kingston included a new interactive debugging facility with windowing and animation, and a major rewrite of Fortran's intrinsic functions (sine, cosine, etc.).

Another important tool developed by IBM programming talent around the world is the Engineering Scientific Subroutine Library. ESSL includes many scientific and engineering functions that were recoded to produce routines optimized for the Vector Facility architecture. The company and third-party vendors also adapted several big scientific and engineering applications for the Vector Facility.

Last month IBM released two more pieces of software to aid programmers in developing software for the Vector Facility. One is an execution analyzer for identifying the hot spots in a program—those sections that use many processor cycles. The other is a simulator that runs under the VM operating system and allows programmers to develop and debug programs for the Vector Facility without having one installed.

IBM also is supporting parallel programming on the multiple CPUs and multiple Vector Facility machines that can be installed in 3090s. The VF Fortran library contains a multitasking facility that programmers can use to introduce parallelism. As yet, IBM has no auto-parallelization software to modify programs to run in parallel, but it is working on it.

The University of Illinois' Kuck is also attacking the shortage of supercomputer software tools through his Champaign, Ill., company, Kuck & Associates Inc. K&AI has two auto-vectorizing preprocessor products on tap, one for use with Cyber 205 machines and the other for an array processor from Star Technologies Inc., Irvine, Calif. These preprocessors take existing programs and generate highly vectorized programs that can be compiled by a Cyber or Star compiler.

As Kuck describes it, the idea behind an auto-vectorizing preprocessor is to "take a nest of loops and interchange them, and get all the vector work in the innermost loops and all of the concurrency in the outermost loops. You optimize it so that for a machine which has vector processors, you get lots of vectors in the innermost loops so the instructions that you can compile are vector operations. [In the outer loops] you get what we call Do-Across. And that's where each of these iterations can be done on a separate processor. So now you've got lots of work for individual processors." The technology has been demonstrated on the University of Illinois' Paraphase preprocessor; Kuck says the K&AI products will be ready this summer.

The new parallel machines are beginning to push the price/performance edge and may ultimately challenge their larger cousins. Several different parallel architectures are competing in the supercomputing arena. In a Hypercube architecture, for example, each processor is connected to, and can communicate with, every other processor in the same parallel computer system. But parallel machines are suffering from the same shortage of software tools that plagues bona fide supercomputers.

"It's mainly an individual programmer's job to figure out how to program a parallel machine," according to John Palmer, chairman and chief executive officer of parallel-computer manufacturer Ncube Corp., Beaverton, Ore. "Some companies will say they've got some of this automated stuff. But if you actually try to use it, you'll find out that it's pretty much research stuff."

Palmer believes that the computer world does not yet know how to design effective parallel-programming tools. "If it were a matter of development, we would certainly be doing it; but it's really a matter of invention," he explains. "It's pretty hard to decide to invent something." On the other hand, with so many scientists and engineers at work on the problem, Palmer believes a breakthrough may be forthcoming.

"The problem with software that can take advantage of the parallelism is that it is extremely application-dependent," says Alison Brown, manager of system development at the Cornell Theory Center. Certain applications—signal processing or scientific calculations replete with arrays, for example—naturally lend themselves to being broken down into small, separate pieces that can run on separate, parallel processors. Other applications, including many artificial intelligence problems, are much more difficult to decompose; these applications' computations occur irregularly, and a processor's load cannot be easily anticipated.

"The basic problem is finding out how to keep in balance the computing that each processor does, and that's what all the software is trying to address," explains Brown. Some of this can be done either manually or with automated tools, by looking at a problem and determining the pattern of interaction between the pieces of the computation in order to figure out a way to decompose it. But there are some inherently unpredictable programs, which may not be possible to decompose in advance. Instead, they would require some way to redistribute loads dynamically while running on a machine.

The problem: parallel software is extremely application-dependent

At the University of Illinois, Kuck is developing software to support parallel processing for use on Alliant Computer Systems Corp. machines. "We're buying Alliants and building the Cedar [a University of Illinois hardware project] out of them. We're building our own software, which is able to do quite a bit better with the Alliant than Alliant's own software does."

Programmers have not generally realized that parallelism should be considered at the beginning of designing an application. There are three phases in the development of a software application, according to Dave Rodgers, vice president of engineering at Sequent Computer Systems Inc., Beaverton, Ore., maker of the Balance family of parallel computers: design, implementation, and "tuning."

Areas ripe for parallel decomposition should be uncovered

WHICH SYSTEMS RUN THE SUPERCOMPUTERS

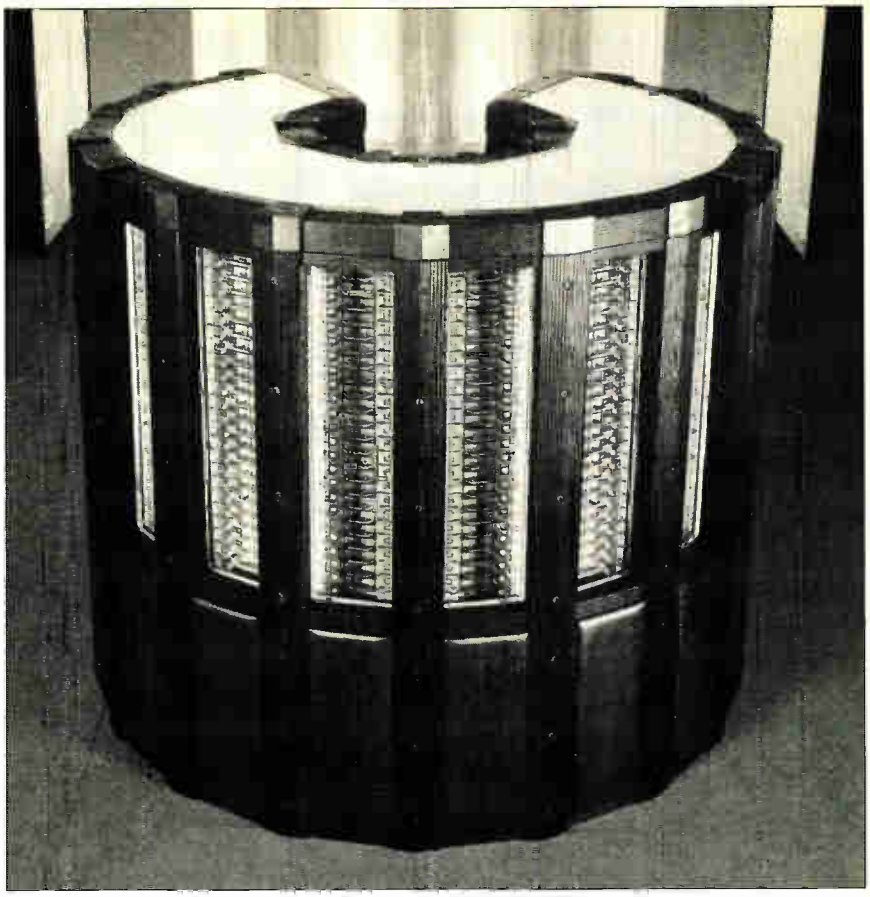
Computer	Operating systems
X-MP (Cray Research)	-COS (proprietary) -AT&T Co. Unix (Unicos)
Cray-2	Unix
Cyber 205 (Control Data)	VSOS (proprietary)
ETA^{10} (ETA Systems)	-Unix -VSOS
VP series (Fujitsu)	VSP (proprietary, IBM-compatible)
S-810 series (Hitachi)	VOS3 (proprietary, IBM-compatible)
SX-1 and SX-2 (NEC)	SXCP (proprietary)

in the design phase. During implementation, he says, "what you're concerned about is technology that allows you to express higher-level ideas, and have the compiler do the hard work of actually scheduling the execution. Then in the tuning phase, you need to be able to look at how the application actually runs, because at the analysis time you can't anticipate some of the asynchronous events. For example, you can't predict the effect on a collection of programs of input and output done by one of them."

A parallel debugger like the one that is in the works for Sequent's Balance machines would allow programmers to dynamically monitor the operation of a program. A major benefit will be the ability to view the effect of individual asynchronous events such as inputs and outputs on the whole program.

"When you're finally done designing an application, you have to be able to observe its actual behavior, and then go back and adjust the parameters of the application so that you're balancing [the program] for the real environment for which the program is designed," Rodgers explains. Sequent's parallel debugger, currently in beta testing, will be available in the late spring.

Software cannot pick up all the parallel-computer slack, says Ray Naeini, Flexible Computer's vice president for software engineering. Some hardware issues remain to be resolved. "A multiple-processor system doesn't mean having several computers on a bus—it goes way beyond that. In a multiprocessor environment, we have had a lot of old problems such as busy/waiting [where processors are sometimes idle because they're waiting for bus access] form of operation and not having a very quick and efficient synchronization tool, and previously we have been trying just to remove those problems in software environments. These famous problems should be resolved first in hardware and in an efficient way, and software should actually utilize those features."



7. BIG UNIX. The Cray-2 is the most powerful machine in the world running Unix.

BOTH SIDES NOW

Common to both the supercomputer and parallel-computer worlds is the issue of operating systems. Today, AT&T's Unix is the leader of the pack. Cray is promoting Unix as the operating system of choice on its equipment, a move that will probably influence other supercomputer makers to adopt it as well. ETA will also offer Unix on the ETA^{10}, but for compatibility, the Cyber 205 operating system (VSOS) will also be offered. Fujitsu, Hitachi, and NEC in Japan currently offer non-Unix operating systems for their supercomputers (table, p. 51).

"Operating systems are kind of a psychological matter: if you've used Unix on the VAX and if you've used it somewhere else, then you might as well have it on your Cray," according to Kuck. "I think that's the whole reason Unix is so popular—Bell Labs basically gave it away to all the universities, but now AT&T is selling it inexpensively, and it's easy to port."

In terms of demand, there appears to be a split between the two important categories of supercomputer and parallel-computer users. On one side are the technically sophisticated users with backgrounds in computer science and engineering. In the other camp are scientists who see the computer mainly as a tool for their research. The computer-wise covet powerful hardware more than they do user-friendly software tools. But the less computer-oriented users need a lot of hand-holding, and tools are just beginning to arrive for them.

"The concept of the parallel environment in software development has been around for quite a while," says Flexible's Naeini. "Now we need to deliver the actual software packages. Then we face the issue of how much of that is required. Obviously, this is the first question in terms of how we can satisfy different users."

"The real bottleneck in programming these things is whether or not you're willing to learn a new set of techniques," says Cornell's Brown. "And there are a lot of people in the world that are not willing to learn anything new, period. Those people sit and say parallel processing is terribly difficult."

Neube's Palmer believes that sophisticated users, even if they are not computer scientists, will be able to handle the machines. "My experience is that physicists who use computers are at least as smart as computer scientists. I've never found a physicist who relied on a computer scientist to give him software—they almost always write their own."

Still, less savvy users might have some difficulty. "It's less likely that we'll come across self-taught star programmers in biology," Palmer says.

"I firmly believe in two things," sums up Illinois' Kuck. "One of them is that you need tools to bootstrap yourself onto new machines. And two, even if we have ideal languages with parallelism in them explicitly and we have vast libraries of parallel algorithms, tools for restructuring programs for the newer architectures are always going to be able to pay for themselves, because [parallel] architectures are such that people can't really comprehend what to do, whereas a piece of software can do a better job." □

When it's time to build your ISDN system...

SIEMENS

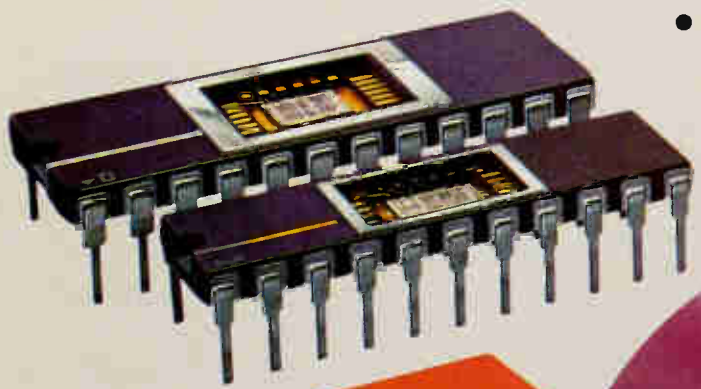
...Siemens new ISDN chips can set it all straight!

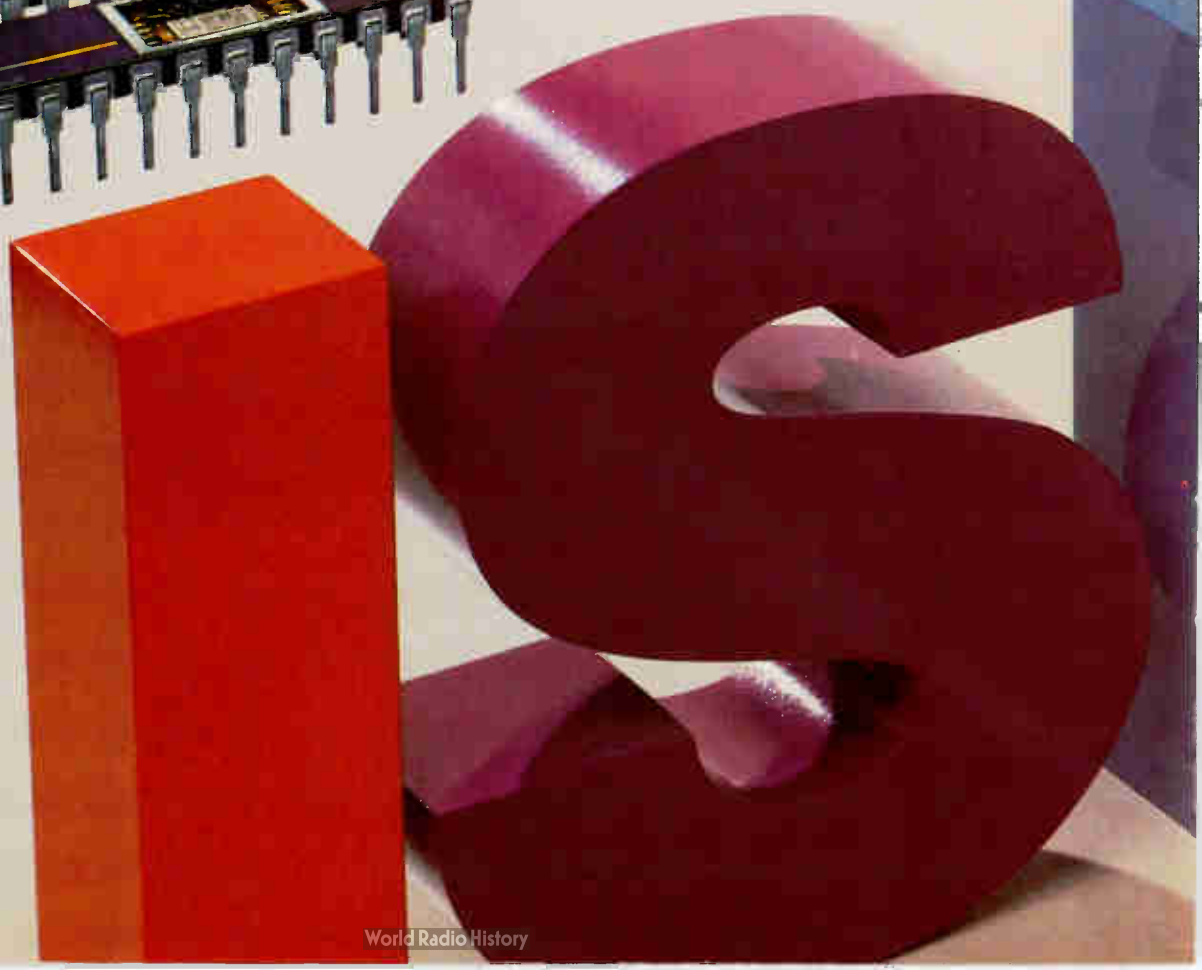
"Getting it straight" in the complex world of ISDN-based telecommunications systems hasn't been easy. Until now. That's because now Siemens offers two important "firsts" – two key ISDN chips specifically designed to meet your most demanding requirements:

- PEB 2070 – ISDN communications controller (ICC)
- PEB 2080 – S-bus interface circuit (SBC)

Designed to meet CCITT specifications, both chips are based on 2µm CMOS technology. In switching, transmissions, terminals, and telephone sets they offer maximum flexibility for the needs of today's telecom system suppliers by providing:

- IOM® interface for flexible allocation of ICs within a system
- Efficient use of the same chip for multiple system applications
- And much more!

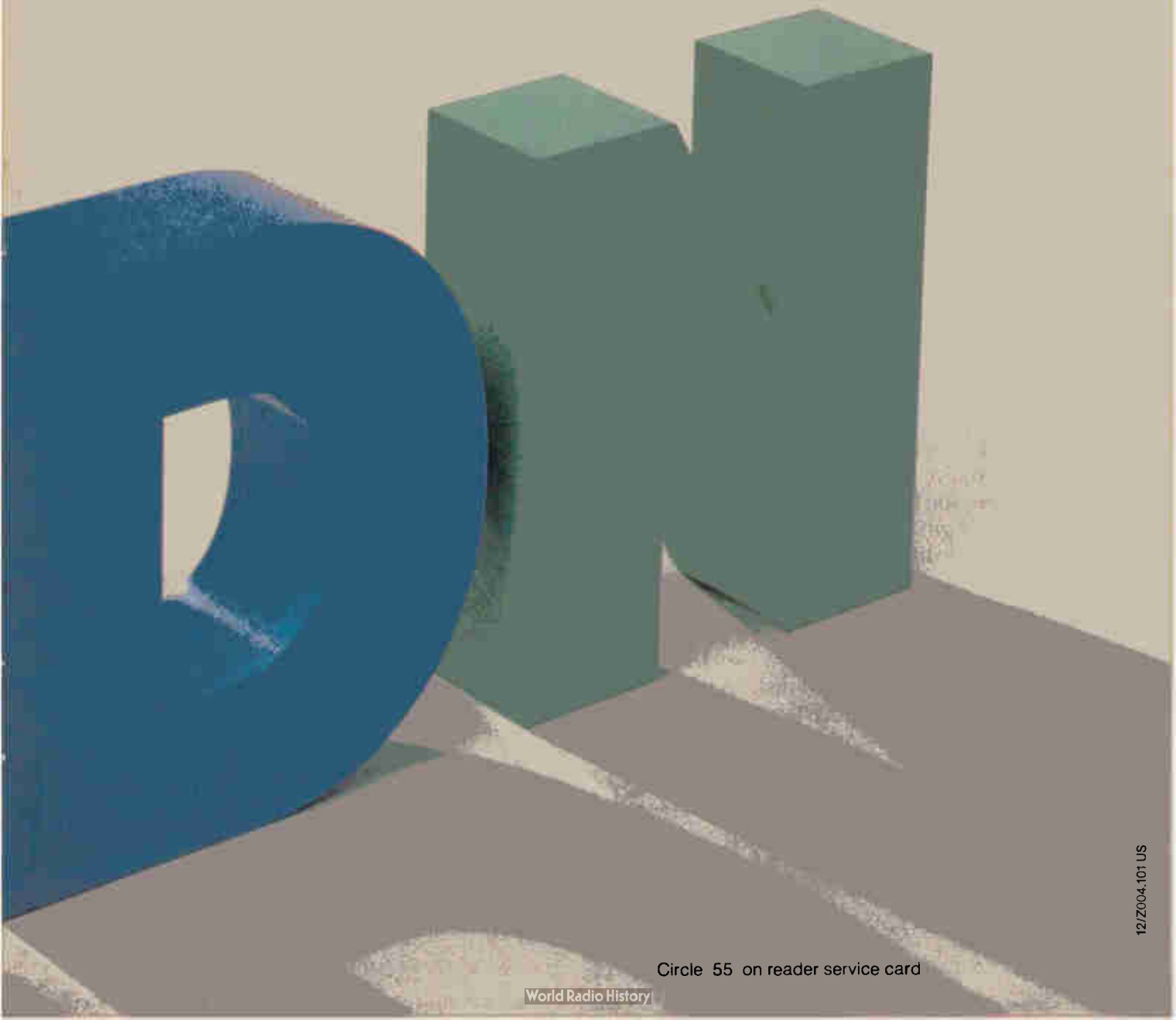




Our new PEB 2070 and PEB 2080 are the nucleus of a family of VLSI chips for ISDN applications designed by Siemens in cooperation with major systems houses.
Now that's a foundation you can build on!
Call Siemens at (800) 222-2203, or circle the bingo number for our literature package.
Siemens Components, Inc., 186 Wood Avenue South. Iselin, NJ 08830.

IOM® – ISDN Oriented Modular Architecture

The key to digital communication systems



12/Z004.101 US

Circle 55 on reader service card

The personal computer that raised high performance to new heights.

If you work with high volumes of information, you need answers fast.

You need a personal computer that's up to the task.

Which is why IBM created the Personal Computer AT® system. It's changed a lot of ideas about business computing.

The idea of "fast" has become much faster. The idea of "data capacity" has become far greater.

There are new definitions of "power" in a stand-alone PC. While phrases like "sharing files" and "multi-user systems" are being heard more often.

And surprisingly, words like "affordable" and "state-of-the-art" are being used *together.*

Clearly, the Personal Computer AT is different from anything that came before. And what sets it apart can be neatly summed up in two words.

Advanced Technology.

If you've ever used a personal computer before, you'll notice the advances right away.

To begin with, the Personal Computer AT is extraordinarily fast. That's something you'll appreciate every time you recalculate a spreadsheet. Or search through a data base.

It can store mountains of information—literally thousands of pages' worth—with a single "hard file" (fixed disk). And now you can customize your system to store up to 30,000 pages with the addition of a *second* hard file.

The Personal Computer AT runs many of the thousands of programs written for the IBM PC family. Like IBM's TopView, the program that lets you run and "window" several other programs at once.

Perhaps best of all, it works well with both the IBM PC and PC/XT. Which is welcome news if you've already made an investment in computers.

You can connect a Personal Computer AT to the IBM PC Network, to share files, printers and other peripherals with other IBM PCs.

You can also use a Personal Computer AT as the centerpiece of a three-user system, with your existing IBM PCs as workstations.

Most important, only the Personal Computer AT offers these capabilities *and* IBM's commitment to quality, service and support. (A combination that can't be cloned.)

If you'd like to learn more about the IBM Personal Computer AT, see your Authorized IBM PC Dealer, IBM Product Center or IBM marketing representative. For a store near you, call 1-800-447-4700 (in Alaska, call 1-800-447-0890).

The IBM Personal Computer AT, for Advanced Technology.

IBM, Personal Computer AT, PC/XT and TopView are trademarks of International Business Machines Corporation.

IBM®

Super Powers

Remote power supplies for microprocessors

Wall Units
+ 5VDC @ 750 ma
± 12VDC @ 80 ma
(W512750/1)

MPI's remote new plug-in units let you take the power supply out of your product and put it practically anywhere. Insert it directly into a wall plug, or rest it on a table top, desk top, bench, or any flat surface.

Designed for use with modems, calculators, appliances, games and a variety of other electronic products, MPI wall and table top power supplies are super-performers; providing outstanding dependability, flexibility and economy. They free up valuable board space, reduce weight and eliminate hazardous voltages, power supply heat and the need for costly cooling devices.

All MPI wall and table top models are UL listed.

Get the MPI super powers working for you. Check these exclusive features and specifications and call us today for details.

- **Multiple & single output**
- **Regulated low ripple**
- **UL and CSA listed**
- **Fully isolated outputs**
- **Comply with FCC EMI regs.**
- **High efficiency**

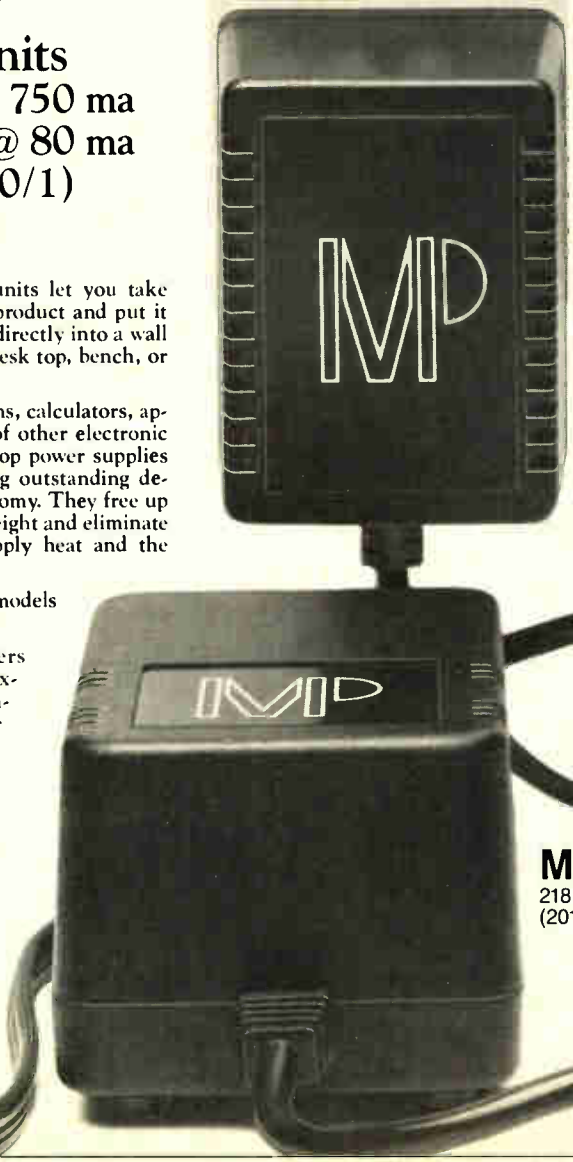


Table Top Units
+ 5VDC @ 1.0 A
± 12VDC @ 310 ma
(T5121000/1)

Specifications:

Input:	120V ± 10% 50/60 Hz
Regulation:	+ 5V 5% overall
Regulation:	+ 15V or + 12V 5% overall
Regulation:	− 15V or − 12V 5% overall
Ripple:	50 MV P-P
Operating Temp:	0°C to + 40°C
Storage Temp:	− 55°C to 105°C
Operating Altitude:	15,000′

Multi Products International
218 Little Falls Rd., P.O. Box 238, Cedar Grove, NJ 07009
(201) 239-8183 • Telex 219289 • Cable: MUPRINUSA-CEDG

Circle 58 on reader service card

PROBING THE NEWS

CAN IBM MAKE THE LAPTOP MARKET HAPPEN?

INDUSTRY FEARS THAT EVEN BIG BLUE CAN'T CREATE BOOM

by Craig D. Rose

BOSTON

Computer marketers learn their first day on the job that IBM Corp.'s move into a market is enough to drive that sector to unprecedented levels. But many of them think that even Big Blue's entry into laptop computers won't spark a boom, as did its entry into the personal computer market. They don't even think that the Internal Revenue Service's decision to buy 15,000 units from Zenith Data Systems (probably for about $1,800 apiece, considerably less than the $3,244 list price) is enough of an endorsement of laptops.

Technology and price are the stumbling blocks

The Zenith Z-171 is an example of the disk-based "laptops" that are too big and heavy to sit comfortably on a lap. Diskless machines fit on a lap, but most have considerably fewer functions than the bigger machines. Both types are battery-powered.

Projections of the market for the disk-based machines have undergone substantial downward revision of late (chart, p. 60) as the sense grows that there is more lacking in this market than just the industry's biggest player. Inadequate technology is one reason; high cost is another.

A new sobriety has arisen from the market's dismal reaction generally to recent products and a consequent reassessment of what customers will accept. Still, many companies already marketing laptops look forward to IBM's entry in the market. "I just wish IBM would hurry up and announce their machine," says Paul Pecka, marketing manager for microcomputing products at Sony Corp. of America, which last November announced an IBM-compatible laptop.

Laptops costing $1,000 to $3,000 will be the fastest-growing segment of the business between now and the end of the decade, believes market researcher InfoCorp, Cupertino, Calif. Sales of these machines will jump from 400,000 units this year to 3.2 million by 1990.

Dataquest Inc., San Jose, Calif., which classifies laptops by features rather than by price, projects that higher-end unit sales will be about 2.75 million in 1989 after experiencing an annual growth rate of about 12%. That's less than half earlier Dataquest estimates, a revision the market researcher attributes to lagging technology, particularly in displays. Other problems cited are battery weight, typically contributing 40% to system weight and 30% to volume. In both areas, relief may be in sight. Vendors report progress on the display front, and Dataquest expects that new battery technology such as rechargeable lithium units will be forthcoming.

Another drag on the market has been cost, specifically for display and CMOS memory. Some reduction is expected in CMOS prices, but they will remain relatively high for a while.

Because of the cost, "it's a second-machine market," says Seymour Merrin, vice president of personal computer services at Gartner Group, the Stamford, Conn., market researcher. "Maybe in an office, they'd have one of these for a guy to take along—there are few large customers. How do you get to all these little people? It's been an active market that had a lot of sex appeal, but it's a market in search of customers."

Merrin and others believe that the market would grow substantially if prices dropped to, say, $1,000 to $1,200 for a machine with a good display and true desktop capability. George Colony, president of Forrester Research Inc. in Cambridge, Mass., adds that some weight reduction for the high-end laptops would also be a plus. Most of them weigh from 10 to 15 lb. "I think it's got to be 4 or 5 lb," Colony says.

OFF THE DIME. Apart from the stamp of legitimacy, many believe, IBM's arrival will knock some customers out of their holding patterns. For example, John Hancock Mutual Life Insurance Co. is shopping for laptops for point-of-sale activities and wants them this year. "We're looking at a number of machines," says John Baker, director of marketing systems. But the Boston company would prefer to see IBM's before making a final decision. "IBM creates standards."

One of the standards IBM could set

LINEUP FOR BATTERY-POWERED COMPUTERS IN U.S.

Company	Number of units (in thousands)	% of market (1985)
Disk-based units		
Grid	15	28.3
Data General	12	22.6
Zenith	8	15.1
Texas Instruments	6	11.3
Kaypro	4	7.5
Morrow	3	5.7
Tandy	1.5	2.8
Other	3.5	6.6
Diskless units		
Tandy	47	30.7
Epson	40	26.4
NEC	25	16.5
Hewlett-Packard	10	6.6
Sharp	10	6.6
Convergent	5	3.3
Sord	2	1.3
Other	13	8.6

SOURCE: FUTURE COMPUTING INC.

WORLDWIDE SALES OUTLOOK DROPS SHARPLY (in thousands of units)				
	1984	1985	1989	Combined annual growth rate 1984–1989
Original count	292.5	838.4	5,254.2	78.2%
Revised count	260.5	481.1	2,770.4	58.1%
Decrease (%)	11	43	47	

SOURCE: DATAQUEST INC.

with a laptop is disk size. Although the IRS opted for a 5¼-in. floppy-disk format when it made its Zenith award, most suspect IBM will opt for a 3½-in. format. It had requested bids on a 3½-in. Winchester disk-drive prototype to be delivered by April or May of this year. Later, the timetable was pushed back to midyear, which one industry insider says puts the laptop introduction at least 18 months away. However, others predict that it will arrive at any time from the end of March through August.

If IBM goes for the smaller format, some supply problems could develop, says Barry K. Berghorn, president of Morrow Designs Inc., San Leandro, Calif., which markets a laptop that uses the larger floppy. Berghorn believes drive production cannot shift quickly because there is not enough 3½-in. capacity.

More important than IBM's disk format will be the machine's functions. "IBM usually has a substantial impact when they introduce anything," says John Frank, vice president of marketing at Zenith Data Systems. But IBM's clout will take longer to be felt if its laptop does not offer functionality and price comparable to a desktop's. That is because the largest potential group of customers for laptops is experienced computer users who see it as a "second car in the garage," says Frank, and they will be seeking compatibility with IBM's Personal Computer.

NO TRICKS. A smaller group of potential buyers consists of first-time users, usually working with computer-savvy Fortune 1,000 companies, with portable-specific applications. According to Frank, "They're not going to be tricked into buying a product that doesn't do everything they need."

With customers identified and products in place, the only thing missing thus far is volume sales orders. "The market is not where industry analysts said it would be 20 months ago," says John Gannon, product marketing manager of the portable computer division at Hewlett-Packard Co., whose offerings are diskless. "But we do feel very bullish about the laptop market and still feel the numbers and the market size are the same."

A product that demonstrated customer resistance to existing technology was the Data General/One, introduced in 1984. The much-ballyhooed 3½-in. floppy-disk-based product packed more functionality into a 10-lb machine than any previous product, but it has sold poorly despite several price cuts. Most, including Data General Corp. president Edson de Castro, blame the machine's liquid-crystal display, which users find hard to read. De Castro remains convinced that there is a significant market for small portables and says the Westboro, Mass., company has made a long-term commitment to developing products for it.

Others blame the Data General machine, at least partly, for slowing the acceptance of laptops. "I think it hurt the market," says Alan Lefkof, vice president of marketing at Grid Systems Corp. of Mountain View, Calif., which was the sales leader in disk-based laptops in 1985. "The screen was so bad it ruined the reputation of LCD technology. We had to work for six months with a very good LCD to regain the reputation."

The biggest challenge: an acceptable low-power display

For the near term, vendors are ruling out alternatives to LCD, such as plasma or electroluminescent displays, because of power requirements. The trend is to continue improving back-lit LCDs. "This technology has now reached an acceptable level and it will continue to get better," says Frank at Zenith. Other technologies will continue to come on, he adds, but he does not expect to see them "this year or next year."

Zenith's approach in winning the IRS contract was to place functionality ahead of portability, with its winning Z-171 weighing in excess of 14 lb [*Electronics*, March 3, 1986, p. 16]. "The competition said, 'Let's build the lightest and smallest possible package and then see what functionality we can build in,'" says Frank. Zenith's priority was matching its laptop's functionality with desktop machines. Similar thinking led Compaq Computer Corp. to shelve its laptop plans entirely and instead trim the size of its portable computer [*Electronics*, Feb. 24, 1986, p. 64].

SOFTWARE KEY. Others in the industry believe the market's key will be application software. "If the right [software] is available at a good price, then the market will grow significantly," says Peter Burgman, a group product manager at Epson Computers Inc., Torrance, Calif. "Just lowering the price alone will not have a major impact." He adds that a significant market would exist for an MS-DOS portable for $1,495 with the right application software.

Lefkof of Grid adds, "The potential for this market is very different from desktops. Companies bought desktops and doled them out one at a time. They were implemented totally as personal machines. Laptops are not personal productivity tools. People will use corporate-prepared software, and there will be more turnkey applications."

Merrin of Gartner Group says that after IBM's rejection by the IRS, customers will look much more critically at IBM's offering than they might have otherwise. So he thinks IBM will want to put some time between the IRS contract announcement and its product introduction.

Among those who have seen IBM laptop prototypes, there is little excitement about its technology. Of course, the same was said about the IBM PC, which nonetheless lit a fire under its market. Either way, IBM's entry is likely to bring others onto the dance floor, including many that have rejected the laptop market as limited.

"There's no vendor who says we're going to make a $4 billion market out of this," says Forrester Research's Colony. "It's a cover-your-butt, 'Let's not let IBM outflank us on this the way they did on personal computers' kind of thing."

Merrin of Gartner Group agrees and expects a crowded field of vendors racing to gain position in what they believe will be a big market. "And they'll all be wondering why it didn't happen." □

U.S. ALSO BUYS ZENITH DESKTOPS

The last week of February was a big one for the people at Zenith Data Systems in Glenview, Ill. Not only were they able to celebrate the company's big victory in the portable arena, but the Zenith Electronics Corp. subsidiary scored another big kill on the desktop front.

On Feb. 28, Zenith received what's said to be the largest microcomputer contract ever awarded by the U.S. government. Under terms of the deal—worth an estimated $242 million—Zenith Data Systems will supply about 90,000 of its Z-200 machines over the next three years. The computers, compatible with the IBM Corp. Personal Computer AT, will be used by the Air Force, Navy, Army, and Marine Corps. *–Wesley I. Iversen*

IT'S SLOW GOING FOR U.S. FIRMS IN JAPAN'S TELECOM MARKET

THE 'OPEN DOOR' COULD LEAD TO SUCCESS ONLY IN NICHE MARKETS

by Michael Berger

TOKYO

The scramble to score in the Japanese telecommunications market is proving even tougher than the most pessimistic U.S. equipment makers thought when the market was opened to foreign suppliers a year ago. Nevertheless, some companies have set up shop in Tokyo, trying to carve out niches in many sectors while remaining realistic about their limited market chances.

One of the busiest markets is value-added networks (see "Japan is hit by epidemic of VAN fever," p. 62), but perhaps the most promising sector is radio communications. Here two markets in particular—cellular mobile telephone and subscriber paging, and portable data transmission—are set for explosive growth over the next 15 years, says Emory Wakat, director of land-mobile products for Nippon Motorola Ltd., Tokyo. Switching equipment and satellite communications are other niches that U.S. companies are targeting.

U.S. companies have managed to score a few market victories. Among them:

- Japanese satellite-communications ventures have bought an estimated $2 billion worth of U.S. equipment.
- Nippon Telegraph & Telephone Corp. has announced a five-year $225 million deal to purchase switches from Northern Telecom Inc., Nashville, Tenn.
- Daini-Denden Inc., Tokyo, has agreed to buy its core switching equipment from Digital Switch Corp., Richardson, Texas.

The two switch deals are seen as clearly linked to pressure to buy American products in light of last year's estimated $49 billion Japanese trade surplus with the U.S. But political pressure can only open the door; it can't guarantee sales. And some foreign players have made more than their share of marketing errors. U.S. companies in particular have found that if they aren't willing to cut profit margins to the bone, they can't compete—even against makers with less-than-leading-edge technology.

There are some 60,000 mobile telephones in Japan—about one fifth the U.S. market total—with an approximate market value of about $62 million, based on Wakat's estimate of average price per unit. But by the year 2000, according to Japanese market forecasts, the number of units will multiply by more than 70 to a total of 4.5 million. Nippon Motorola's chances in pagers, another part of that promising market, depend largely on approval by the Ministry of Posts and Telecommunications of new technologies such as numeric display and message readout devices, in which Wakat says his company has leading products.

Virtually every foreign company regards the time factor as crucial to its long-term plans in Japan. "We have a window of opportunity of perhaps five years to cash in on our investment," says Randall C. Harris, vice president of Uninet Japan Ltd., a joint venture of Kanematsu-Gosho Ltd., Tokyo, and 60% owner U.S. Telecom Data Communications Co., Tokyo.

Harris is confident that his company can provide international packet-switching and data-base access services superior to those of any Japanese operation. Still, that time constraint is worrisome. "We can't get into the business we're aiming at until the Ministry of Posts and Telecommunications implements a new RPOA [Recognized Private Operating Agency] policy," he says.

For now, Tokyo's Kokusai Denshin Denwa Co. is the only recognized international telecommunications carrier in Japan, which means that all operations wishing to crack the expanding business must use the company as their carrier to foreign locations. The MPT has pledged to open the market, but the process is moving slowly.

Harris sits on an advisory committee that will submit its RPOA recommendations to the MPT this month, but that's just one step. "We've got to keep the momentum going," says Harris. If the MPT drags its feet on this and other issues—in effect giving Japanese companies a chance to catch up in technical areas where they trail foreign companies—the millions of dollars that Uninet has invested to build its Japan and Far East markets could go down the drain.

STRONGER POSITION. Nippon Motorola is in a stronger position. The company has been in Japan for more than 20 years and has established a working relationship with NTT and the MPT on the radio market issue.

"We've agreed on a good compromise on allocation of wavelength for our private radio-transmission equipment," Wakat says. "But we still have to work on getting other technical standards set so we can introduce our newer paging products to the market." He adds that he would like to be selling those products by early next year.

There are three key issues in radio communications, says Mark Foster, the Tokyo representative of the U.S. Electronics Industries Association. "The allocation of frequency and easing of licensing procedures for American wireless-service companies is one. Another is de-

FOREIGN COMPANIES PICK THEIR TARGETS

Company	Market interest
AT&T International (Japan)	Value-added networks, central and packet switches, PBXs, telephones
Digital Switch	Packet switches
Ford Aerospace	Communication satellites
General Electric Information Services	VANs
GTE Communication Systems	Electronic mail, voice mail
Hughes Communications	Communication satellites
IBM-Japan	VANs, terminal equipment
ITT	Packet switches
McDonnell Douglas	VANs
Nippon Motorola	Mobile communication systems
Northern Telecom Pacific	Central switches, PBXs, telephones
Rolm	PBXs

SOURCE: EDP JAPAN REPORT

fining customer-premises equipment so that NTT, which used to have a monopoly, no longer has any advantage. And the third is making sure we have access to all the information we need to comply with Japanese market standards and procedures."

The standards and procedures themselves are no longer an issue, Foster says. "We've achieved virtual parity between the Japanese and U.S. markets. Now we've got to see that what's on paper is translated into reality in the marketplace."

In that market, more than 15 foreign manufacturing and service companies have established offices in Tokyo—and 47 companies, double the number a year ago, will have displays at the Communications '86 Tokyo show running April 12-15. But mere presence in Japan does not add up to sales success, as one of the biggest of them all has found.

GOOD GROWTH. AT&T International (Japan) has gone in three years from a one-man operation to a staff of more than 90, engaged in everything from software development to joint ventures with such Japanese companies as Ricoh Co. and Toshiba Corp. But the news has been more bad than good.

In January, when AT&T announced in the U.S. that it was deep-sixing its Network 1000 data-transmission system because of technical problems, there was an earthquake of sorts in Tokyo. Suddenly, 16 Japanese partners in a VAN venture with AT&T had to reassess the entire venture.

A month earlier, three years of AT&T efforts to sell its top-of-the-line ESS5 central digital switches to NTT collapsed when rival Northern Telecom won its $225 million sale. "NTT chose to go with older, less risky technology," says AT&T Japan president William J. Moody (see story, p. 65). "We think our switch would have improved service."

Northern Telecom Pacific (Tokyo) president Hugh Hamilton responds: "We deliberately chose our DMS-10 rather than our larger capacity DMS-100 [which competes directly with AT&T's ESS5] so we could aim for a niche in the Japanese market." AT&T couldn't compete, Moody says, "because we don't have a switch in that [5,000-line] range."

Northern Telecom's strategy of going for a niche makes sense because of the enormous potential in the telecommunications business, making the niches worth going after. One analysis, by the U.S. Embassy in Tokyo, forecasts that Japan's telecommunications equipment and services market will be worth close to $8.5 billion by the end of 1987.

There are a variety of strategies. But for the larger companies, such as AT&T and Northern Telecom, the tendency is to look at Japan not only as a place for sales but often as a production base, with some of the products headed for third-country markets. Northern Telecom has added Oki Electric Industry Co. as the third distributor for its SL-1 private branch exchange system, and indicated that manufacture in Japan is a future possibility. And Digital Switch, which is opening a Tokyo office to serve its first major client, Daini-Denden, plans to market its products, including the digital signal processing equipment of its Granger Associates subsidiary, elsewhere in Asia.

A big lure: Japan's telecom market could near $8.5 billion in 1987

Satellite communications, a growing market in which U.S. technology is clearly superior, has different problems. Japan Communications Satellite Co., a Tokyo venture in which Hughes Communications has a 30% stake with Mitsui (35%) and C. Itoh (35%), has invested more than $300 million in ground support facilities in Japan for an initial launch set for December 1987.

The schedule backup created by the space shuttle disaster places the venture in a tight spot, however, one in which it must compete with other private satellite ventures and the military for space on future launches. Europe's Ariane remains an alternate possibility.

Growth in U.S. company sales, however, is likely to be a gradual process. Rolm Corp., which has spent four solid years mining the Japanese market, still holds only about a 3% share of a PBX market that is valued at about $283 million this year. □

JAPAN IS HIT BY EPIDEMIC OF VAN FEVER

The most active and yet unpredictable Japanese telecommunications market of all is value-added networks. More than 100 new ventures have created a phenomenon that has become known as VAN fever, and companies such as U.S. Telecom Data Communications Co. and General Electric Technical Services Co. Inc. (Getsco) see the market as a base from which to offer services internationally.

John F. Barber, managing director of Getsco's Information Services Division in Tokyo, is cautious about how dramatic such VAN market growth will prove to be. "It may be worth perhaps $200 million this year," he says. "But there's still a lot of floundering around, trying to identify services in demand and then getting systems running."

The most formidable VAN is the extensive tieup announced in December between IBM Japan Ltd. and Nippon Telegraph & Telephone Corp. Called Nippon Information & Communication Corp., it will allow NTT to use IBM's Systems Network Architecture, and, from IBM's view, create expanded markets for its systems products.

GTECommunication Systems-Asia Inc. (Tokyo), which tried and failed to sell its central switches to NTT, now thinks the packet-switched services, in company president Robert H. Farwell's words, "is the best market for synergy with the Japanese." GTE-Asia's Japan VAN is a joint venture with Intec Inc. (Toyama), a government-licensed private telecommunications company. The venture opened electronic-mail services in December and has plans to begin voice-messaging services. *–M. B.*

FARWELL: Synergistic market.

VALUE-ADDED NETWORKS GROW IN JAPAN

Year	Market value ($ millions)	Sectors	% of market
1986	150	On-line data processing	100
1990	495.5	On-line data processing	66
		Basic communication services	27
		Data-base services	7
1995	2,000	On-line data-processing services	50
		Basic communication services	39
		Data-base services	11

SOURCE: EOP JAPAN REPORT

ONCE AGAIN: CAN HICKEY TURN GI AROUND?

THE COMPANY IS PRUNING OPERATIONS AND REFOCUSING ON CORE BUSINESSES IN ATTEMPT TO REGAIN ITS LUSTER

NEW YORK

General Instrument Corp., once a top manufacturer of all manner of electronic products, is no stranger to success and just as familiar with failure. Its fortunes over the last 20 years have ricocheted between profit and loss.

Now the question is whether chairman and president Frank Hickey can work his magic and raise the company out of the ashes once again. Hickey certainly thinks so. By pruning some operations and focusing on the core areas of data systems, broadband communications, semiconductors, and components, he says, he will turn General Instrument around.

FRANK HICKEY: Profits will return this year.

The company was off and running in the 1960s with subscriber equipment for the cable television industry, then suffered a near-disastrous nosedive when the electronics industry tottered in the mid-1970s. Then came 30 straight quarters of growth into the early 1980s. But the 1980-81 recession triggered a swing from which the company is still struggling to recover. In fiscal 1986, it will post a loss of some $76 million, more than five times the 1985 deficit.

TWO VIEWS. Industry watchers are divided about the company, some seeing it as a has-been, others lauding its technology and resources. "They're going to snap back," says Eliot Glazer, senior analyst for aerospace and electronics at Derby Securities, New York. Jay Samstag, senior analyst at Duff & Phelps Inc., Chicago, agrees, noting that the 57-year-old Hickey "has done it before and people believe in him."

Among the naysayers is Joseph Bellace, an analyst at Merrill Lynch in New York. He holds that recent organizational changes, which decentralized the chain of command and relieved Hickey of some responsibilities, won't make much difference. But even he sees possibilities for success.

Hickey acknowledges that General Instrument may have gotten too cocky during its heyday in the late 1970s, when it invested in everything from keyboards to artificial intelligence and direct-broadcast satellite communications. He also admits he was caught flat-footed when business swooned. "The changes took place rapidly. We weren't prepared for the suddenness of this market swing and, hell, I'm the first to admit it. Our resources got stretched too thin."

But today's General Instrument is a mature corporation, he says, focusing on its core businesses and steering clear of the overwhelming urge to diversify. He envisions a forward-looking communications company, concentrating on semiconductors, defense electronics, and cable television yet poised to launch a drive into satellite communications, local-area networking, and other businesses when the opportunity is ripe.

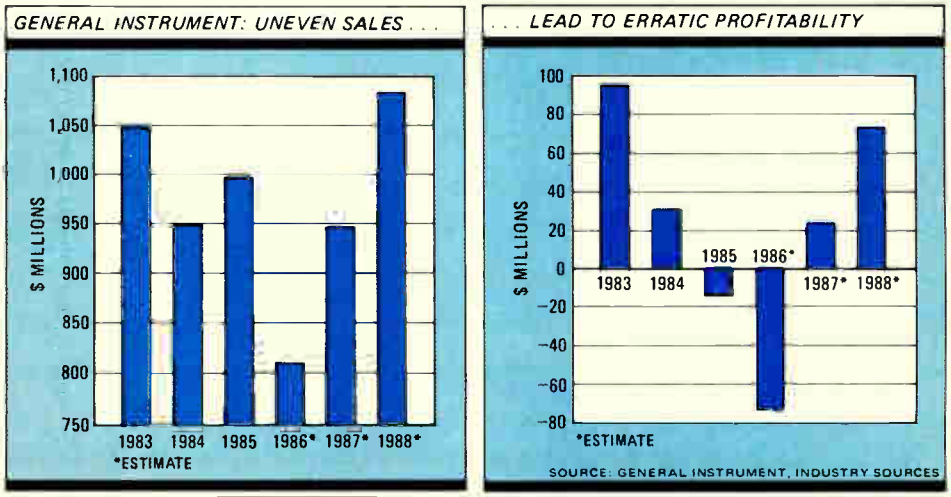
The strategy "is to divest our losing businesses where we do not have market position or where the product life is over," Hickey says. "Mostly, we're cleansing the peripheral distractions from our central businesses." In the last six months, General Instrument has consolidated its Microelectronics Division into one facility in Chandler, Ariz., and closed the Business Systems Division and sold off its assets. It will also stop making keyboards and surge arresters, because, Hickey says, the market opportunity is too small.

Financially, says Hickey, the company has some definite strengths. General Instrument today is cash rich and faces minimal debt. At the end of its third quarter, it had total current assets of $455.9 million against liabilities of only $195.7 million. "We've got more resilience to come back" than in 1976, when net income slipped 37.7%, to $7.2 million, the chairman says. Industry-watcher Glazer agrees: "They've got the best balance sheet of any technology company, including IBM Corp."

Glazer thinks that General Instrument will rebound with a vengeance. He predicts the company will post fiscal 1987 earnings of about $32 million, rising to about $72 million in 1988. Hickey declines to project figures. But he is confident of profits in fiscal 1987 and says that in 1988 "we'll begin to make some decent money."

NEW LINES. Contributing to those profits will be new products. General Instrument's schedule of advanced semiconductor products is "the most impressive I've ever seen," says Glazer. A 1.5-μm 64-K CMOS electrically erasable programmable read-only memory with on-chip error correction is the first of what Glazer says will be seven significant new items scheduled for introduction in coming months.

Those products will lead a resurgence in General Instrument's semiconductor business that will push the division's operating profits over the $50 million mark in fiscal 1988, he predicts. For fiscal 1985, General Instrument lists semicon-



ductor sales of $279.6 million, with an operating profit of $18 million.

Analyst Samstag is more cautious, however. He recalls how three or four years ago, General Instrument, which supplied ROMs for cartridges, was a primary beneficiary of the video game boom. But when that market dried up, he says, "their revenue and earnings died with it. I'd have hoped that new products would have helped them along, but that hasn't happened. The only business that's been consistent for them is defense."

'We weren't prepared for the market swing'

General Instrument's Government Systems Division, which has operations in passive radar warning, surveillance, and targeting systems for military aircraft and vessels, has grown steadily, helping to keep the Data Systems Sector in the black.

Hickey agrees that the steady performance of its defense business is key to the company's future. Also important, he says, will be judicious investment in new ventures. In the past, General Instrument's track record has been spotty. That could be changing, starting with what analyst Bellace calls a major opportunity—the company's 55% interest in Sytek Inc., a leading supplier of broadband LANs. Sytek has a close working relationship with IBM, which has options to buy about 5% of its stock. Hickey praises Sytek for its "brilliant performance" in the LAN market and says General Instrument has "enormous ambition in this sprawling market."

The company's investment in Phasecom (Israel) Ltd., a modem manufacturer, has been less fruitful. "We thought we'd be a hell of a lot further on in point-to-point modems than we are," Hickey says. He also says that General Instrument is now weighing whether Phasecom is "going to be a part of the future of this company.

"We are looking at acquisitions vigorously now, but only where it fits closely with the businesses we have a firm commitment in." Those businesses, rooted in the communication field that General Instrument knows so well, will make or break the company as it clears a new road to redemption. General Instrument has learned its lesson, Hickey admits—the hard way. *–Tobias Naegele*

BOTTOM LINES

VENTURE CAPITALISTS RAISE $2.3 BILLION

There appears to be no shortage of money for investment in new companies. The venture capital industry last year raised $2.3 billion in new capital commitments, reports *Venture Capital Journal*, a Wellesley Hills, Mass., publication that tracks the venture capital industry. The 1985 amount is substantially lower than the $3.4 billion raised in 1983 and the $3.2 billion raised in 1984. However, the journal cautions that "the explosive activity of 1983, which carried over into 1984, was an unusual occurrence and should not be used as the standard against which to measure industry growth." Venture organizations in California raised 32% of the 1985 funding, followed by New York companies with 22% and Massachusetts venture companies with 17%.

TANDON, HYUNDAI FORM DISK VENTURE

Disk-drive maker Tandon Corp., Chatsworth, Calif., and Hyundai Electronics Industries Co., a part of Seoul's Hyundai Group, have formed a joint venture to make and market disk drives in Korea. Hyundai Magnetics Co. will manufacture hard- and floppy-disk drives designed by Tandon. The partners hold equal equity in the new venture, which will have exclusive marketing rights in Korea.

DALLAS SEMI GETS NEW FUNDS

Two-year-old Dallas Semiconductor Corp. last week received $10.8 million in a second round of venture capital, bringing total investments to $32.2 million. President John Smith expects the company to be profitable by the end of this year. The Dallas company, which makes late-definition semicustom CMOS products, had revenue of $3 million in its fiscal year ended Oct. 31, 1985.

FORTUNE SYSTEMS POSTS BIG LOSS

Adjustments and write-offs of nearly $14 million in the final quarter gave ailing Fortune Systems Corp. a loss for 1985 of $23.5 million on sales of just $47.5 million. In 1984 it lost $21.9 million on sales of $70.1 million. The Belmont, Calif., maker of office systems based on AT&T Co.'s Unix operating system said it finished 1985 with $22 million in cash. Last year, Fortune Systems cut its workforce by nearly half, reduced its facilities by a third, and moved some manufacturing offshore. The company says those actions are enabling it to reduce operating expenses and improve margins in 1986.

MOODY GOES AFTER A NEW IMAGE FOR AT&T IN JAPAN

TOKYO

William J. (Mike) Moody, the 46-year-old president of AT&T International (Japan) Ltd., describes himself as a salesman—facing the toughest sell of his life. He's not only trying to promote AT&T products in Japan—he's also trying to re-instill Japanese confidence in the company.

The 21-year AT&T veteran has to do more than overcome the historic Japanese reluctance to deal with foreigners. He also must pick up the pieces after the washout of AT&T's much-heralded Network 1000 data-processing and distribution system, a failure that shook AT&T's Japanese partners in the value-added-network venture.

MIKE MOODY: AT&T is a tough sell in Japan.

The debacle came right on the heels of another AT&T defeat: Nippon Telegraph & Telephone Corp.'s decision, announced last December, to purchase $255 million worth of telephone switches from AT&T rival Northern Telecom Corp. The two setbacks were major blows to the company's sweeping plans for making market inroads in Japan (see story, p. 61).

"We ought to be able to sell here," says Moody, whose aim is to balance AT&T's estimated $300 million worth of annual purchases from Japanese makers by 1989. With that in mind, he's honed his strategy in two ways since arriving in Japan last June after serving as director of business market management for AT&T Communications Corp. "One is the sense of how important communication is in succeeding here. That's both 'big C,' technology, and 'little c,' the ability to communicate your ideas.

"The other important difference is that I am more careful now in exploring alternate ways of doing things," he continues. "You've got to be able to modify your approach, or you'll always be off-target."

Rival companies and industry analysts see in such comments an indication that the U. S. monolith has been humbled. "Not just in Japan, but all over the world, AT&T has a reputation for arrogance," says one rival executive. "Now they're discovering that they've got to change that attitude if they expect to compete successfully." One way is to pay more attention to local market needs for its products.

That could be another reason for Moody's tough work schedule, which routinely includes 13-hour days plus at least half a day on Saturday. But, he says, for the first time he is forcing himself to make sure that work is balanced by other activities. "If you don't do that, you can't be fully effective on the job. The pace of economic life in Japan is incredible. I look up every once in a while and realize that I haven't read a book or seen a show for weeks."

One outlet is exercise; Moody calls himself "the heaviest jogger in Tokyo." And when time permits, he and his wife travel in Japan. You never know where you can make a sale. *–Michael Berger*

GOOZÉ BRINGS HIS ZIP TO TELEDYNE

MOUNTAIN VIEW, CALIF.

Mitchell Goozé has been in a whirlwind since he graduated from the University of California at Los Angeles with a BSEE in 1973. At 34, he is already into his second company presidency, this time with Teledyne Semiconductor, a division of Teledyne Inc. whose principal product is analog linear integrated circuits. His charge there is to revitalize one of the oldest semiconductor companies, founded by Teledyne 25 years ago under the name Amelco Semiconductor. "We're trying to bring back to this company the feeling, the excitement, and the image we had in the 1960s"—when the company was near the top of the supplier heap.

A man blessed with a great deal of energy, Goozé has learned most of the

PEOPLE ON THE MOVE

WALTER TETSCHNER

☐ As the new vice president of engineering at Voicetek Corp., Walter Tetschner will be responsible for development of the Newton, Mass., company's voice-processing products. Tetschner moves from Digital Equipment Corp., where he managed the Voice Products Group and led the development of DECtalk, a text-to-speech product, and also helped develop the interface to DEC machines. Before his stint with DEC, Tetschner was with Delta Data Systems and GTE Information Systems.

ROBERT G. BROWN

☐ Intelligent Systems Corp., Norcross, Ga., has appointed Robert G. Brown president of subsidiary Quadram Corp., also in Norcross. Brown joined Quadram, which specializes in microcomputer enhancements, two years ago as general manager of the Communications Products Division. He was subsequently named national sales manager and most recently vice president of sales and marketing. Brown has been a consultant for several major computer retailers.

RODNEY C. LANCASTER

☐ As part of a program to gear up for an expected growth spurt later this year, Semicon Components Inc. has named Rodney C. Lancaster as president. He will assume the duties performed by Rolland V. Robison of parent holding company Semicon Inc. Lancaster joins the Burlington, Mass., manufacturer of discrete semiconductors from the Semiconductor Equipment Operations, Test Systems Division of Eaton Corp. He was vice president and director of Asia/Pacific Operations after serving as the division's vice president and general manager.

MARLIN L. SHOPBELL

☐ Thesis Group Inc., a Dallas single-source systems integrator for computer-integrated manufacturing, has named Marlin Shopbell to be vice president of semiconductor automation. Shopbell, one of the founders of Mostek Corp., held a number of engineering management positions relating to process development and wafer fabrication with the Carrollton, Texas, chip maker. Most recently he had been the company's manager of manufacturing technology.

CHRISTOPHER L. HAMLIN

☐ Office-automation equipment manufacturer Seicom Business Systems Inc., Carrollton, Texas, has named Christopher L. Hamlin vice president of planning and development. Hamlin returns to the wholly owned subsidiary of Hattori-Seiko Ltd., Tokyo, after spending the last two years heading Xebec Corp.'s Systems Research Division. There he was instrumental in the development of the first compact-disk read-only-memory controller for the IBM Corp. Personal Computer.

POSITIONS VACANT

Design Engineer. As member of a design team in the development of employer's product for the industrial market place, applicant will be responsible for the hardware/software design, debugging and integration of the logic control sub-system for the end product. The product being designed is semi-conductor test equipment. Design includes high speed ECL logic, state machine theory, transmission line analysis, noise and cross talk minimization and microcode design and programming. Debug and integration includes back plane design, power and heat analysis and system software development. Minimum education requirement: Master of Engineering required, major field of study — Electrical Engineering. Other special requirements: Thorough knowledge of high speed logic design techniques (ECL technology), including transmission line and state machine theory, as well as a knowledge of control software architecture required. Education in software operation systems required. Must be able to work in a team environment. Total hours per week: 40; Work Schedule: 8 a.m.-5 p.m. Rate of Pay: $2,600 per month. Apply at Texas Employment Commission, Dallas, Texas or send resume to Texas Employment Commission, TEC Building, Austin, Texas 78778, Job Order #4506900. Ad paid for by Equal Employment Opportunity Employer.

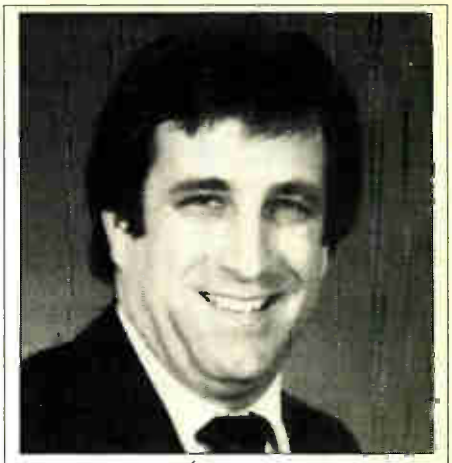
South? Technical/Professional Placement Network-Fee paid. Murkett Associates, Box 527, Montgomery, AL 36101.

POSITIONS WANTED

Electronic Expert For Hire. I do Microprocessor hardware/software, assembly language. Analog, digital design in my N.Y. lab or worldwide. Project rates. Mr. Barry Masel (718) 476-1516.

RESUMES

Resumes — Complete instructions and examples; $4. Consultants, Box 567—J, Bergenfield, N.J. 07621.



MITCHELL GOOZÉ: Pulling Teledyne up in the analog market with sheer energy.

basic job functions in the semiconductor business in a relatively short period of time. He began his career as a product engineer on calculators for now-defunct Lloyd's Electronics, where he worked for two years before signing on with Waugh Controls as a design engineer.

MOVING UP. Two years later, in 1976, he saw an opportunity in the rising wave of microprocessors and moved into marketing with Motorola Inc. in Phoenix, Ariz. He stayed with Motorola till 1978, when he moved on to American Microsystems Inc. (now Gould AMI Semiconductors), Santa Clara, Calif. In three years, he rose to director of the gate-array and microprocessor product groups while completing the course work for his MSEE and almost finishing the requirements for an MBA.

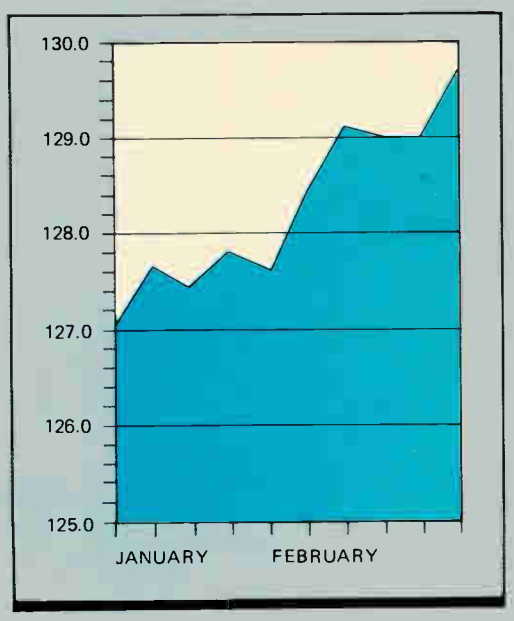
Rather than complete his degree in business, however, Goozé went out and started his own company. Solosystems was the brainchild of Goozé and several AMI colleagues, who quit their jobs to embark on the new endeavor in 1981. Goozé served as president of the San Jose, Calif., concern, which made programming tools. And while Solosystems failed in 1984, Goozé considers his stint there "a very valuable use of my time."

The essential lesson he learned, he says, was "the difference between being a president and being a profit-and-loss manager. When you're president, you don't have anyone else to blame things on. You are ultimately responsible."

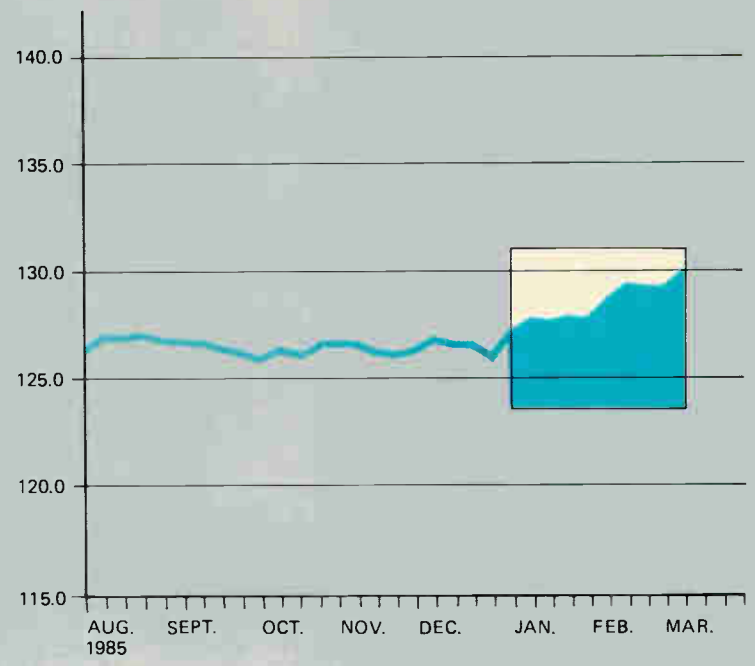
After the company folded, Goozé signed on as general manager of the Custom Power Division of Micro Power Systems, an IC-manufacturing company in Santa Clara.

He had been there for about a year when he heard about the Teledyne position. He applied, and last November became president of one of Teledyne's 137 companies. His aim is far from modest: "We're going to be a major player in the analog market. Not No. 1, but in the top five." *–Eve Bennett*

ELECTRONICS INDEX



THIS WEEK = 129.7
LAST WEEK = 129.0
YEAR AGO = 129.6
1982 = 100.0



The *Electronics* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

U. S. GENERAL ECONOMIC INDICATORS

	December 1985	November 1985	December 1984
Index of leading economic indicators	173.6	172.0	164.1
Budgeted outlays of the federal government ($ billions)	84.079	84.763	77.583
Budgeted outlays of the Department of Defense ($ billions)	23.915	21.971	20.156
Operating rate of all industries (% capacity)	78.5	78.1	78.9
Industrial-production index	126.3	125.4	123.3
Total housing starts (annual rate in thousands)	1,804	1,654	1,607

U. S. ELECTRONICS PRODUCTION INDEX

	December 1985	November 1985	December 1984
Office and data-processing equipment	267.1	262.9	256.4
Communications equipment	223.7	223.9	218.0
Radio and TV equipment	175.3	150.2	150.0
Electronic and electrical instruments	141.0	140.7	138.9
Components	248.2	243.2	298.1

Production of electronics equipment in the U. S. edged up 0.5% in December, even though it fell from levels of a year ago in many sectors. Overall U. S. output of electronics goods slipped almost 1% in 1985, compared with 1984's 21.3% increase.

The December rise translates into a 3% jump in the *Electronics* Index, putting it at its highest level in the past 12 months. Industry sources say this strong showing, which comes on the heels of a 3.7% decline in output in November, could indicate that the U. S. electronics industry is finally starting to recover.

For the full year, the beleaguered U. S. components industry saw production fall 10%, and production of consumer electronics equipment dropped nearly 12% following 1984's 19% increase. On the plus side, computer and office-equipment manufacturers ended 1985 with production up 4.3% from the end of 1984, and manufacturers of communications equipment boosted 1985 output by 9%.

GSI's System: PC-800 Model 4.

The perfect tool for SMD design.

Faced with growing demands for more performance in less real estate, PCB designers are turning to SMD's. And they are discovering that it takes a special kind of CAD system to handle new design techniques like SMD. Fortunately, there's a proven, perfect tool for the new directions in electronic design: the new PC-800 Model 4. The CAD system with the flexibility, precision and interactive nature SMD's mandate. Even the necessary outputs, like solder paste templates and pick and place NC tapes needed for their individual job or panelized manufacture.

Since there are no standard sizes or configurations to SMD's, designers need the PC-800's vast and flexible symbol storage. A library from simple SO-IC's to complete jobs. They need its floating variable grid to accommodate the variety of SMD shapes and footprints. They need continuity checking and design rules checking features that recognize components on both sides of the board. And the ability to create shielding and ground planes accurate to .0001 inch in unusual geometric shapes and voids. With the right tool, SMD's can be the next big mover in your company. And the right tool is the PC-800 Model 4. Call or write for a demonstration today.

GSI™ The Gerber Scientific Instrument Company

83 Gerber Road West, South Windsor, CT 06074 Tel: (203) 644-1551

Circle 68 on reader service card

NEW PRODUCTS

A FAST REACTIVE ION ETCHER THAT DOESN'T DAMAGE WAFERS

MATERIALS RESEARCH'S NEW MACHINE MINIMIZES ION DAMAGE

The newest plasma etcher from Materials Research promises to remove the stumbling block that has kept other reactive ion units from widespread use on production lines. Aries, for Advanced Reactive Ion Etching System, uses magnetron technology to get a throughput comparable to other plasma etchers, but without the wafer damage that earlier machines can cause.

The promise of plasma etchers is their ability to lay down the fine geometries and complex structures required in today's ICs. The critical goal is to achieve good anisotropy—the ability to cut clean vertical features, such as trenched capacitors and isolation trenches, without undercutting the wafer surface and thereby damaging performance.

LOW-PRESSURE ETCHING. A major step toward that end was the development of dry processing systems, such as reactive ion etchers, that use gas plasmas instead of liquids to etch silicon wafers. But these systems were slow. Increasing the pressure of the plasma speeds up the processing rate, but the stronger ion dose can damage wafers.

Aries operates at low pressure but does not sacrifice throughput for definition, or vice versa. The magnetron keeps the plasma's excited ions close to the wafer surface at low pressures, thereby maximizing throughput and minimizing damage from ions. Other companies, such as Applied Materials Inc. and Veeco Instruments Inc., are making reactive ion etchers, but no other etcher maker uses a magnetron.

Materials Research found that by generating a plasma at radio frequencies between two parallel electromagnets on either side of the wafer, it could achieve throughputs between 25 and 70 wafers/h, depending on the process, at a pressure of just 100 mTorr. Though the number of wafers etched in an hour is comparable in other systems, the total yield is increased because there are fewer—if any—damaged wafers.

The company first applied the magnetron principle to plasma etching in its MIE 700 series [*Electronics*, April 21, 1983, p. 184], a pair of high-output research and development machines that failed to muster any market share—only 51 machines have been sold. Two factors account for the disappointing showing, says Walter Vanden Bossche, senior product manager for plasma etching. First, the industry was apprehensive about investing in a new and untried technology; second, Materials Research, misjudging the market, did not provide a production-oriented machine with a host of automatic features.

NO DAMAGE. The Aries etcher uses little pressure and does not undercut wafers.

Fully automated with cassette-to-cassette wafer handling, the serial processing Aries system requires minimal operator know-how. Instead, sophisticated, user-friendly software runs a computer controller that handles the entire process, stopping only to warn the operator if there is trouble on the system—the company guarantees 90% uptime. Aries can handle multiple processes for manufacturers that switch among a variety of production techniques. The system handles wafers of up to 6 in., but can be equipped for 8-in. wafers.

NICHES. In light of its experience with the MIE 700 series, the company realized that it would have to focus on niches to penetrate the market. "This is not the greatest thing since sliced bread for all materials," Vanden Bossche admits. "We're going to concentrate on two families of applications—optical lithography and silicon trench etching. Magnetron ion etching is particularly good for these technologies."

Aries will come in two versions—one for fluorinated gases, one for chlorinated gases. Orders are being accepted for the $395,000 fluorine system, and delivery will take four months. The company is shipping the first such system to Siemens AG in Stuttgart, West Germany, this month. Chlorine systems, which have not yet been priced, will be available by mid-May. *–Tobias Naegele*

Materials Research Corp., Route 303, Orangeburg, N. Y. 10962. Phone (914) 359-4200 [Circle reader service number 338]

MINISUPER'S PRICE TAG IS ONLY 10% THAT OF A CRAY

The new price/performance champ in the 64-bit minisupercomputer field is the SCS-40 from Scientific Computer Systems. It sells for $595,000 for an entry-level system and executes up to 44 million floating-point operations/s. This is about 25% of the performance of the Cray X-MP/1 at only one tenth the cost. For scalar operations, the SCS-40 does 18 mips.

The SCS-40, which is the first model in Scientific Computer Systems' line of minisupercomputers, runs the same software as the Cray Research Inc. X-MP/1 because it uses a compatible instruction set. In addition, it runs soft-

WE HAVE THE BEST LOCATION FOR HI-TECH INVESTMENT IN ASIA

As Taiwan's answer to the Silicon Valley, this ambitious, innovative Science-based Industrial Park has a lot to offer, making it one of Asia's best choice for hi-tech investors worldwide.

- An access to Taiwan's bountiful resource of scientific and technical brainpower.
- Up to 49% government joint venture.
- Attractive tax incentives and low interest loans.
- Favorable government attitudes toward hi-tech industries.
- Well-established infrastructure.
- A modern community boasting housing, clinic, bilingual school, recreational center and other public facilities.

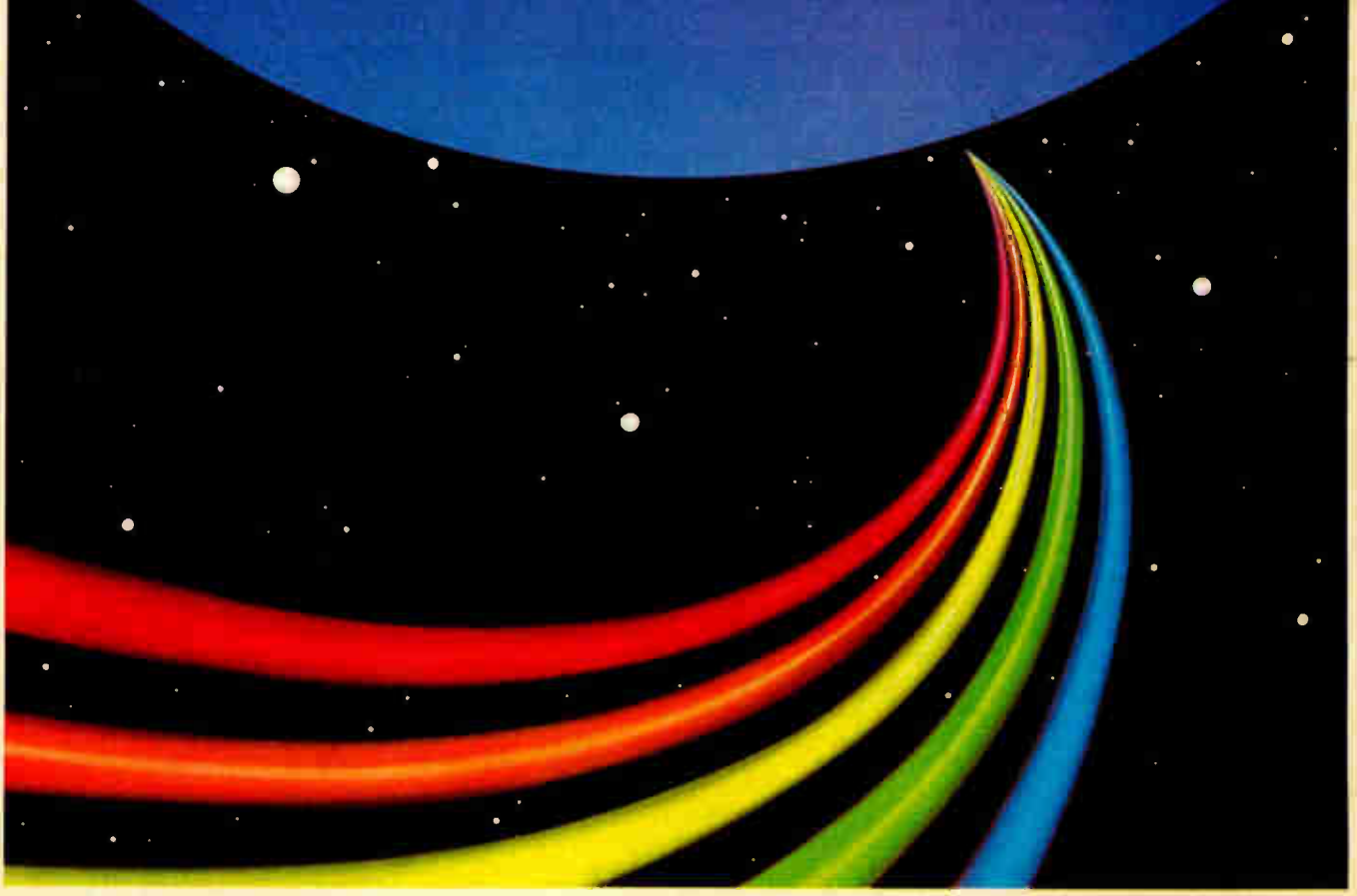
Scores of international companies are already operating successfully in this Science-based Industrial Park. Join them and make it your base in Asia, too.

科學工業園區

SCIENCE-BASED INDUSTRIAL PARK

2 HSIN ANN ROAD, HSINCHU, TAIWAN, REPUBLIC OF CHINA

TEL:(035)773311 TLX:32188 NSCSIPA



ware written for Digital Equipment Corp.'s VAX minicomputers.

"Our price/performance provides an entry into the supercomputing environment for users whose needs have outgrown their current systems. And our Cray compatibility gives them a head start by providing access to a full selection of proven application packages," says Robert Schuhmann, chairman and chief executive officer of Scientific Computer Systems.

HOT MARKET. Minisupercomputers show signs of becoming the fastest-growing segment of the scientific and engineering computer market (see story, p. 44). They are garnering attention by providing a very high price/performance ratio for supercomputing and filling a gap between the giant supercomputers with gigantic price tags such as the Cray X-MPs, and computers with much lower vector processing speed, such as the DEC VAX 8600 and 8800, and IBM Corp. 4381 product lines.

In addition to Cray compatibility, the SCS-40 is compatible with the VMS operating system used on the VAX. The machine fits into existing computer configurations, boosting system throughput without compromising software investments. Cray and VAX users do not have to modify their software environments.

The system comes with vectorizing Fortran 77 compilers, which are in the public domain. The compilers, which adhere to ANSI 77 standards and accept VAX Fortran source code, permit users to convert their existing Fortran programs and keep the user interfaces that they are familiar with. The compilers automatically optimize and vectorize code, and are supported by a number of libraries and development tools.

The computer incorporates an innovative architecture that combines multiple 64-bit data buses and permits up to five vector operations, one scalar operation, and an address operation to execute concurrently in a single clock cycle. The design minimizes signal paths, resulting in high bandwidths. Data is transferred from I/O buffers to central memory at 1 word per 45-ns clock cycle (equal to a rate of 533 Mb/s). The processor busing structure moves 6 words per clock period (1.07 Gb/s) between registers and functional units.

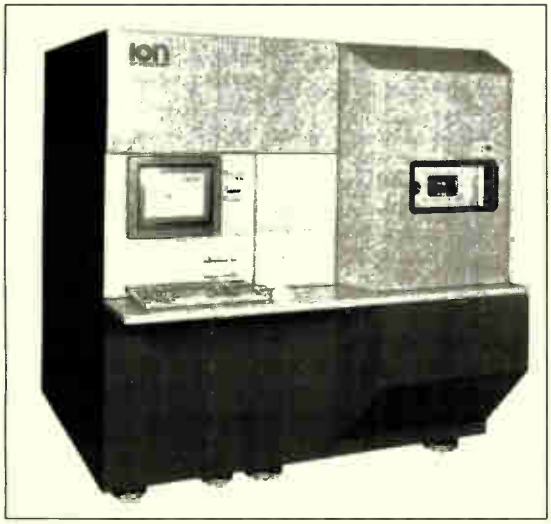
The SCS-40 will be available beginning in the third quarter. *–Tom Manuel*

Scientific Computer Systems Corp., 25195 S. W. Parkway Ave., Wilsonville, Ore. 97070. Phone (503) 682-7223 [Circle 342]

MASK REPAIRER TAKES ON SUBMICRON DEFECTS

Seiko Instruments' SIR-1000 mask-repair system performs fast, precise repair of both clear and opaque defects down to 0.25 μm on glass photomasks and reticles. In addition, the system can make changes in mask design in the laboratory, which Seiko says will shorten the design cycle.

The SIR-1000 uses focused ion beams, which provide the submicron resolution and accuracy needed for the emerging generation of very large-scale integrated circuits based on 1.5- to 1.25-μm geometries. Ordinary laser photomask repair systems can remove only opaque defects larger than 1 μm. The focused-ion-beam principle also applies to X-ray mask repair.



TWO KINDS. Seiko's repair system removes opaque and clear defects as small as 0.25 μm.

Like Micrion's KLA/Micrion 808 [*Electronics*, Jan. 6, 1986, p. 65], the SIR-1000 removes opaque defects—such as dust and poorly etched chromium, which block light through the mask—by scanning the ion beam directly over them. But unlike the 808, Seiko's machine completely mills away defects without damaging the substrate—an end-point monitor automatically stops the sputter etching when the repairs are completed.

The two machines also differ in their procedures for eliminating clear defects, or missing parts of the chromium pattern. Where Micrion's machine etches optical refractors into the glass substrate, the Seiko system selectively deposits an opaque carbon film over the defect. The carbon films can be modified if necessary, allowing greater repair and design flexibility. The operator can review repairs during processing through secondary ion imaging, a feature that uses Seiko's proprietary scan sequences. It allows precise imaging up to 30,000× magnification.

SCRATCH-PROOF. A gas injector continuously deposits the carbon, which is in a hydrocarbon base, onto the mask's adsorbent defect area. The gas molecules are adsorbed in the jetted area. The user then programs the system to scan the ion beams over the defect area, inducing a reaction that provides an opaque film. The carbon films are as resistant to scratching as the mask's chromium films.

The SIR-1000 uses the same hardware for both clear and opaque defects, which Seiko says provides consistency of operation and improved throughput. The company will introduce the system in May at Semicon West in San Mateo, Calif. The first SIR-1000, which is priced at $1 million, will be delivered to a U. S. customer in May 1986. The SIR-1000 is a version of another Seiko machine modified—with mouse-driven software—to serve the U. S. market. *–Jerry Lyman*

Seiko Instruments U. S. A. Inc., 2620 Augustine Dr. Suite 290, Santa Clara, Calif. 95054. Phone (408) 727-0768 [Circle 341]

INTEL'S 1-Mb EPROM: A TRIPLE SOLUTION

Intel is trying to ease the migration to higher EPROM densities by offering three architectures for its 1-Mb part, which it announced at Wescon. The chips are intended for customers who need a clear upgrade to the higher density, for those who do not want to modify their existing designs, or for those working on new designs that can take advantage of advanced 16- and 32-bit processors.

The company is alone among makers of 1-Mb EPROMs to offer three architectures [*Electronics*, Oct. 14, 1985, p. 55]. "What we've found is that the diversity of today's system designs, combined with the sheer density of a 1-Mb device, demand multiple architectural solutions to meet the wide variety of application

WIN $1,000 CASH
ADVERTISER AUDIT

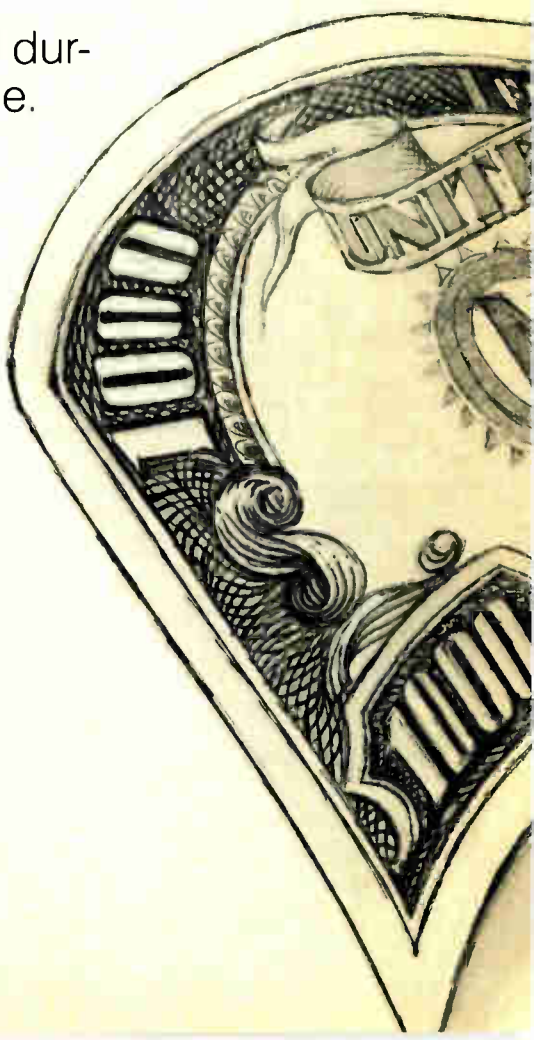
Electronics' unique new contest makes it easy to win big.

The rules are simple. Each issue this month contains a ballot asking you to select your three favorite ads in the issue. All you do is fill in your choices and drop it in the mail. Your returned ballot or reasonable facsimile is automatically entered in the prize drawing at the end of the month. If your name is drawn at random, you win one thousand easy dollars.

Ads receiving the most votes each week and during the course of the contest will be rerun for free.

You can win money *and* let advertisers know what you think of their selling messages. Advertisers can win extra insertions.

So watch for contest ballots and rules in each March issue. And get ready to win big this month.

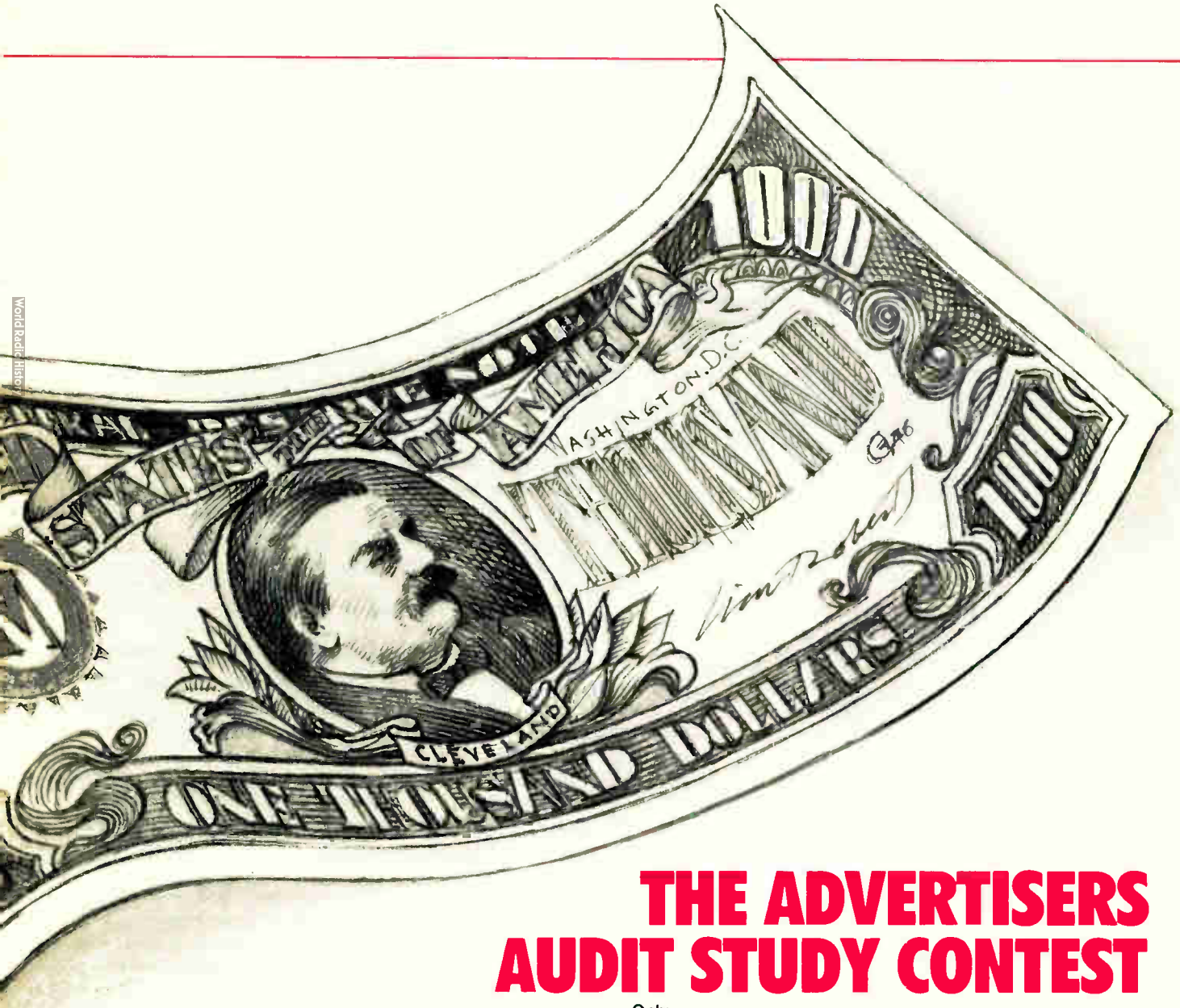


ADVERTISERS: YOU CAN WIN $1,000, TOO!

All advertising and marketing personnel in companies and agencies are invited to participate along with our readers by filling out a special Advertisers Ballot included in each March issue. Whoever comes closest to picking the 15 winning ads for the month (3 from each issue) in this special Advertisers Contest will receive an award for skill in evaluating advertising, plus a free ad insertion for his or her company, and $1,000 cash!

ONLY IN MARCH

IN ELECTRONICS' STUDY CONTEST



THE ADVERTISERS AUDIT STUDY CONTEST

Only this month in

Electronics

Electronics

THE ADVERTISERS AUDIT STUDY CONTEST

Enter a drawing for $1,000 cash by selecting your favorite ads in the March issue of *Electronics.*

Reader Contest Rules

1. After you have examined this issue of *Electronics,* pick your three favorite ads and enter your selections on the entry blank bound in this issue or on a 3" x 5" index card. Your entry should include: 1) the name of the advertiser; 2) the advertiser's Reader Service Number; 3) the page number the advertisement appears on; and, 4) if you would like, your comments explaining what you like most about the ads you selected. Ads placed by McGraw-Hill, Inc. should not be considered in this contest.

2. Check the box on the entry blank marked "Reader Contest." No more than one entry *per issue* may be submitted by any one individual. All entries must be postmarked no later than midnight, April 18, 1986. The winner will be notified in May, 1986.

3. The winner of the $1,000 cash prize will be selected in a random drawing from among all eligible entries. Winner will be notified by mail. Odds of winning depend on the number of entries received.

4. No purchase necessary. Contest void where prohibited or restricted by law. Liability for any taxes on the $1,000 cash prize is the sole responsibility of the winner. Employees of McGraw-Hill, Inc., its advertising agencies, and their families are not eligible to participate.

Advertiser Contest Rules

1. All advertising and marketing personnel in companies and agencies (other than McGraw-Hill, Inc. and its advertising agencies) are invited to participate in a separate contest for advertisers. All rules for the Reader Contest will similarly apply for this contest, with two exceptions: 1) the winner of the Advertiser Contest will *not* be selected in a random drawing from among all eligible entries; and 2) the box on the entry blank marked "Advertiser Contest" must be checked.

2. Examine the March issues of *Electronics* with extra care. Choose the three ads in each issue that you think readers of *Electronics* will pick as their favorites and enter your selections on the entry blanks bound in each issue or on a 3" x 5" index card. No more than one entry *per issue* may be submitted by any one individual.

3. All entries must be postmarked no later than midnight, April 18, 1986. Each individual's qualifying entries will be matched against the winning ads as determined in the Reader Contest. Whichever individual in this Special Advertiser Contest comes closest to picking the 15 winning ads for the month of March, 1986 will receive: 1) $1,000 cash; 2) one free full-page ad in *Electronics* for their company or client; and 3) a plaque acknowledging their skill in evaluating advertising. McGraw-Hill, Inc. reserves the right to schedule the free ad at its discretion.

4. This special Advertisers Contest is open to all advertising and marketing personnel in companies and agencies (other than McGraw-Hill, Inc. and its advertising agencies), whether or not their companies or agencies have an advertisement in the March, 1986 contest issues.

5. No purchase necessary. Contest void where prohibited or restricted by law. Liability for any taxes on the $1,000 cash prize is the sole responsibility of the winner. Employees of McGraw-Hill, Inc., its advertising agencies, and their families are not eligible to participate.

Winning Advertisers Earn Free Ad Reruns

The three advertisers receiving the most votes in each March 1986 issue of *Electronics* will receive a free rerun of their winning ads and a plaque commemorating their achievement. Since there are five issues of *Electronics* in March, there will be a total of 15 winning ads.

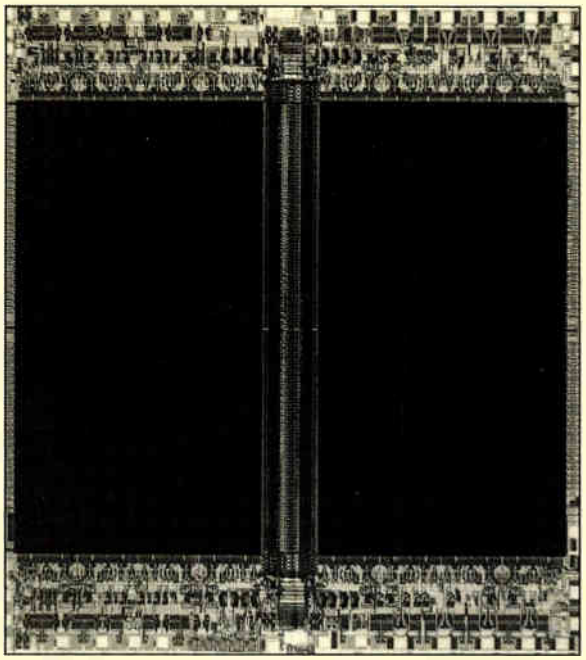
After all the March Reader Contest ballots are received, the three ads that scored the highest over the course of the entire contest will be determined and announced in May, 1986. These three Grand Prize Winners will receive a special plaque, plus a free rerun in *Electronics* of *all* the ads they ran in *Electronics* during the entire month of March.

All reruns will be made from existing plates or negatives. If the advertisement qualifying for a free rerun is an insert, the winner may run up to a four-color, two-page spread on R.O.P. stock from existing plates or negatives. McGraw-Hill, Inc. reserves the right to schedule reruns at its discretion.

needs," says Don Knowlton, product marketing manager for the company's Programmable Memory Operation.

The three EPROMs consist of the 27010, housed in a 32-pin package and organized as 128-K bytes by 8 bits; the 27011, which comes in a 28-pin package and is configured as eight pages of 16-K bytes by 8 bits; and the 27210, housed in a 40-pin package and organized as 64-K words of 16 bits each.

The 32-pin 27010 is suitable for designers who are concerned about an upgrade path from the lower-density EPROMs to ones with high densities. The lower 28 pins are directly compatible with the existing Jedec-approved 28-pin configuration currently occupied by 256- and 512-K EPROMs. To take advantage of the 1-Mb density, system designers need only alter their layouts to accommodate the additional four pins.



FASTER. Intel's three 1-Mb EPROMs have 200-ns access times, but the 40-pin memory also comes in a 150-ns version.

In addition, if designers use the 32-pin configuration today, they can still use 28-pin EPROMs until their applications warrant 1 Mb. A board design that accommodates the 32-pin configuration will assure system designers of an unimpeded path to 8 Mb in the future.

LOCKED IN? For designers who are locked into a 28-pin configuration, the 27011 page-addressed memory is a direct replacement for the byte-wide 27513, a 512-K EPROM. The page-addressing mode feature expands the addressing capabilities of 8-bit microprocessor systems to accommodate higher-density memories while conserving the 28-pin site.

The third EPROM, the 40-pin 27210, represents a new 16-bit word-wide architecture and is designed to optimize the capabilities of advanced 16- and 32-bit microprocessors. In such applications, where the system's EPROM array must be wider, the 27210 can serve as a single- or multiple-chip memory solution.

The 27210's nonmultiplexed organization ensures compatibility with a broad base of CPUs. Its flow-through layout, where addresses are on one side of the chip and data on the other, simplifies board layout. The memory also provides a direct upgrade path to handle 8 Mb. It is also available in a higher-performance 150-ns version.

Programming support for the 1-Mb memories is available now. Customers can use Intel's iUP 200/201 PROM programmers with the addition of a new generic universal programmer-interface-personality module. Using the Quick-Pulse Programming algorithm, the 1-Mb EPROMs can be programmed typically within 15 seconds.

The three parts, which have 200-ns maximum access times, are made in Intel's compacted HMOS II-E process, a process that results in 1.4-μm features.

The 27010 and 27011 are available now for $72 each in lots of 10,000. The 27210 is available in sample quantities, with production quantities to be ready during the second quarter of the year. The memories will first be offered in windowed, ceramic side-brazed packages; Cerdips will be available in the second quarter. *–Steve Zollo*

Intel Corp., Literature Department W-287, 3065 Bowers Ave., Santa Clara, Calif. 95051 [Circle 339]

CAD SIMULATOR CHECKS PLD TIMING

Now that programmable logic devices are becoming denser, more intricate, and more expensive, the PLD engineer's time-honored way of designing them—trial and error—is no longer the work method of choice. Valley Data Sciences has stepped in with a solution: Perfect, a computer-aided-design compilation software with timing simulation capability that allows its use on both synchronous and asynchronous circuits.

The software can be used alone or with the company's Vista PLD schematic-capture software, which runs on the IBM Corp. Personal Computer. It can also be incorporated into AT&T Co.'s Unix operating systems.

"Most engineers who design PLDs don't simulate the part," says Keith Barnes, vice president of marketing and sales for Valley Data Sciences. Typically, most programmable logic devices have been inexpensive to make, allowing engineers the luxury of blowing fuses on a number of devices as they worked out the right program by trial and error. But the devices are changing character, Barnes says, becoming denser and more intricate as they incorporate asynchronous capabilities. This means they're getting more expensive, and therefore less expendable.

Until the introduction of the Perfect software, the few PLD simulators available—such as Cupl and Abel—have had only stimulus-and-response capability. Perfect's timing simulation lets asynchronous circuits be modeled as accurately as synchronous ones.

EASY CONVERSION. Perfect takes Boolean equations, state-machine syntax, truth-table input, or schematic entry from the company's Vista software and compiles it for downloading to a device programmer for use with commercially available PLDs. Converting the software from one manufacturer's PLD to another is easy thanks to Perfect's translator: it transforms standard Jedec PLD files into Boolean equations or net lists, so the designer doesn't have to convert different compilers' syntaxes. At the equation level, the design can be altered and quickly recompiled for different PLDs. The Perfect software also includes algorithms that help optimize a design for a specific programmable device.

Engineers can model and simulate complex logic designs for different PLDs as well as for systems employing PLDs and standard TTL parts (whose parameters are included in Valley Data Sciences' simulation).

Perfect for the IBM PC family sells for $995. A system with a hard disk and 512-K bytes of RAM is recommended, though the software can run on a dual-floppy-disk system with just 256-K bytes of RAM. Bundled with Vista software, graphics card, and mouse, the Perfect package sells for $3,650. A Unix 4.2bsd version is priced at $2,495. Delivery takes 30 days. *–Eve Bennett*

Valley Data Sciences, 2426 Charleston Rd., Mountain View, Calif. 94043. Phone (415) 968-2900. [Circle 340]

MEETINGS

INFOCOM WILL FOCUS ON LOCAL NETWORKS

The increasing importance of local-area networks comes to the fore at this year's Infocom conference, says Harvey Freeman, chairman of this year's standing committee. Freeman founded the computer-communications conference five years ago.

LANs will be a chief topic at this year's conference, and Freeman notes that papers will cover the push for standardization at all levels. Not too long ago, standardization efforts were limited to the lower hardware level, such as wiring. Now "people are starting to choose networks based on what they can do," he says, and that means "they want to be able to get software off the shelf and use it." That's where Infocom comes in, Freeman says. The conference "has been oriented to laying the theoretical groundwork and gauging practical considerations for standardization." One session, on various LAN standards includes a paper on fiber-optic standards.

Another key topic will be the inclusion of networking software in computer operating systems—but by no means will LANs be the sole topic at the conference. Two of the 30 sessions will address issues in network management; in addition, mobile radio systems and satellite networks will receive coverage.

Infocom, which grew to 500 attendees in 1984, dropped off in 1985, reflecting the general industry slowdown. Freeman, vice president at Architecture Technology Corp., Minneapolis, hopes it will "get back on track this year." Its sponsors are the IEEE's two largest groups—the 84,000-member Computer Society and the 24,000-member Communications Society.

29th IPC Semi-Annual Meeting, Institute for Interconnecting and Packaging Electronic Circuits (IPC, 3451 Church St., Evanston, Ill. 60203), Sheraton Hotel, Boston, April 6-10.

Advanced Research in VLSI, National Science Foundation *et al.* (Paul Church, Room 39-321, Massachusetts Institute of Technology, Cambridge, Mass. 02139), MIT, Cambridge, April 7-9.

The Changing Environment for Computer Storage, Gartner Group Inc. (72 Cummings Point Rd., Stamford, Conn. 06902), The Pointe at Squaw Peak, Phoenix, April 7-9.

AIDD Convention and Technology Exposition, American Institute for Design and Drafting (966 Hungerford Dr., Suite 10-B, Rockville, Md. 20850), Diplomat Hotel, Hollywood, Fla., April 7-10.

FOSE, Federal Office Systems Exposition, National Trade Productions Inc. (2111 Eisenhower Ave., Alexandria, Va. 22314), Convention Center, Washington, April 7-10.

Infocom 86, IEEE (Steven H. Richman, IEEE Infocom 86 Publicity, AT&T Bell Labs, Room HO-3L-531, Holmdel, N. J. 07733), Sheraton Bal Harbour Hotel, Miami, Fla., April 7-10.

International Conference on Robotics and Automation, IEEE (Robotics & Automation, c/o Harry Hayman, Exeter C3037, Boca Raton, Fla. 33434), San Francisco Hilton and Tower Hotel, San Francisco, April 7-10.

31st International Sampe Symposium, Society for the Advancement of Material and Process Engineering (843 W. Glentana St., Covina, Calif. 91722), MGM Grand Hotel, Las Vegas, April 7-10.

Communications Week '86, Datapro Research Corp. (Raymond J. DeAngelo and Lynn T. Sadlon, McGraw-Hill Information Systems Co., 1221 Avenue of the Americas, New York, N. Y., 10020), Holiday Inn, San Francisco, April 7-11.

15th International Programmable Controllers Conference and Exposition, Engineering Society of Detroit and Society for Machine Intelligence (ESD, 100 Farnsworth Ave., Detroit, Mich. 48202), Cobo Hall, Detroit, April 8-10.

Nascon: National Security Conference, TCM Expositions Ltd. (Robert Myhelic, Tower Conference Management Co., 331 W. Wesley St., Wheaton, Ill. 60187), Nouveau Palais Des Expositions, Geneva, April 8-10.

1986 Test & Measurement World Expo, *Test & Measurement World* (Meg Bowen, Test & Measurement World Expo, 215 Brighton Ave., Boston, Mass. 02134), San Jose Convention Center, San Jose, Calif., April 8-10.

Icassp '86: International Conference on Acoustics, Speech, & Signal Processing, IEEE *et al.* (Charles F. Teacher, RCA Corp., GSD Engineering, Building 206-1, Cherry Hill, N. J. 08358), Keio Plaza Inter-Continental Hotel, Tokyo, April 7-11.

Robots 10, Robotic Industries Association (Robotics International/Society of Manufacturing Engineers, 1 SME Dr., Dearborn, Mich. 48121), Chicago Hilton & Towers, Chicago, April 21-24.

Comdex/Spring, Interface Group Inc. (300 First Ave., Needham, Mass. 02194), Georgia World Congress Center *et al.*, Atlanta, April 28-May 1.

Advertisers Index

Classified and employment advertising

For more information of complete product line see advertisement in the latest Electronics Buyers Guide
* Advertisers in Electronics International
‡ Advertisers in Electronics domestic edition

ELECTRONICS WEEK

KODAK PLANS CHIP EQUIPMENT . . .

Continuing its recent efforts to expand into more high-technology markets, Eastman Kodak Co. is forming a company to build and market semiconductor-manufacturing equipment. The Rochester, N. Y., photographic giant says the new company—to be called Estek—will draw extensively on technology developed internally to produce custom integrated circuits for use in Kodak products. It will operate as a division of Eastman Technology Inc., a wholly owned Kodak subsidiary, and will incorporate Xertronix Inc., a Rochester maker of rinser-driers for wafer processing, which Kodak bought last summer. Estek will introduce its first products, microcontamination-control equipment, in May.

. . . AND REALIGNS ITS R&D EFFORT

As part of a planned decentralization of its research and development activities to "more directly link specific technology efforts and business strategies," Eastman Kodak Co. has closed its prestigious Kodak Research Laboratories, which were established in 1912. The realignment creates seven independent laboratories, each assigned to a business group.

AT&T ESTABLISHES EUROPE OEM BASE

Strengthening its presence in European markets, AT&T Co.'s Components and Electronic Systems Division has set up headquarters in Munich to sell electronic and optoelectronic devices to original-equipment manufacturers in central Europe. The new operation, AT&T Microelectronics GmbH, also encompasses the U. S. company's first design center for application-specific integrated circuits in Europe. The Munich facility will serve customers in West Germany, Switzerland, Austria, and the Benelux countries.

AMD JOINS MENTOR IN CAE DEAL

Advanced Micro Devices Inc., Sunnyvale, Calif., has chosen Mentor Graphics Corp., Beaverton, Ore., to jointly develop new computer-aided-engineering applications. Looking toward future custom integrated-circuit design, AMD and Mentor say they intend to further integrate the design process, from Mentor's Idea work station series through its Chipgraph physical-layout tools.

APPLIED MATERIALS CUTS BACK

Though the Semiconductor Industry Association says chip makers' book-to-bill ratio is improving, business activity for equipment manufacturers appears slower to rebound. Applied Materials Inc., Santa Clara, Calif., has laid off more than 100 employees and plans five scattered one-day plant shutdowns through April, affecting about 1,000 workers. Although last week the maker of wafer-fabrication systems introduced a fully automated epitaxial reactor system at Semicon Europa, Zurich, Switzerland (p. 13), president James C. Morgan says that there is a "continued softness in bookings for semiconductor production systems on a worldwide basis."

GOULD BUYS CIM COMPANY

Gould Inc. has added machine-vision capabilities to its bag of industrial-automation tricks. The Rolling Meadows, Ill., company announced last week the acquisition of the Vision Systems Division of Automation Intelligence Inc., a private Orlando, Fla., supplier of computer-integrated-manufacturing software and systems. Terms of the deal were not disclosed. Vision Systems will operate as part of Gould's Industrial Automation Systems Group, in Andover, Mass.

ITT SEEKS HIGHER EUROPEAN PROFILE

With the introduction last week at its Brussels headquarters of a line of office-automation and data-processing equipment, ITT Europe is ready for the first time to sell a family of products under its own trademark throughout the Continent. Office 2000 is a line of digital private automatic branch exchanges for voice and data transmission with capacities of 10 to 3,000 lines. With Office 2000, ITT is seeking a high-profile image as an integrator of office systems made up of heterogeneous equipment. The company has sales of some $1 billion per year in Europe in office systems and expects that figure to grow at least 15% per year. Until now, ITT had generally marketed its products under the names of its European subsidiaries.

CIPHER DATA GETS TAPE-DRIVE PATENT

Cipher Data Products Inc. has been granted a U. S. patent on the mechanical configuration fundamental to 5¼-in. tape drives. According to the San Diego company, all streaming-tape drives using standard ¼-in. cartridges in the 5¼-in. format may be covered in this patent, and Cipher is studying its alternatives; presumably the main one is to charge royalties to other manufacturers.

FIELD NARROWS IN PAKISTANI PROJECT

Competition for a coveted Pakistani digital telephone project, which would give the contractor an edge for a billion-dollar modernization of the country's entire Telegraph and Telephone Department, has narrowed to Siemens, Ericsson, and Northern Telecom. ITT West Germany, ITT Italy, Japan's NEC, and France's Alcatel were eliminated after a first round of bidding, despite substantial political pressure from their governments. The current project involves building a factory, setting up 150,000 telephone lines, and manufacturing private area branch exchanges in Pakistan.

FAIRCHILD CLOSES HYBRID OPERATION

In keeping with its plan to concentrate on high-performance integrated circuits, Fairchild Semiconductor Corp. will shut down its hybrid circuit operation at the end of March. It is negotiating with several firms for sale of the manufacturing rights. Fairchild has been making hybrids since 1965, but last year the custom modules accounted for just over 1% of sales, mostly for automobile ignition systems. Fairchild will close its Mountain View, Calif., hybrid facility and try to absorb its 58 employees elsewhere in the company. A Hong Kong assembly plant will also be closed.

IEEE MAP, OFFICE UNITS COMBINED

User groups interested in the IEEE 802.4-based Manufacturing Automation Protocol (MAP) and the IEEE 802.3-based Technical and Office Protocol (TOP) have been combined into a single organization. Both MAP and TOP aim to provide standard methods by which computer-controlled equipment from a variety of vendors can communicate on the same network—MAP on the factory floor linked to TOP in the office. Both approaches are based on the International Organization for Standardization's seven-layer open-systems interconnection model.

A fresh breeze across the Pacific.

The airline that serves more top business centers in the United States now serves more top business centers across the wide Pacific with more nonstops than any other airline.

Convenient service to thirteen cities in all, with all the advantages that come with one airline service.

One airline to handle ticketing, seat assignments, boarding passes, and baggage for your whole trip.

And, of course, United's incomparable Mileage Plus, offering a whole world of exciting travel awards.

You'll enjoy United's famous Royal Pacific Service, the best of the friendly skies in First Class, Business Class, and Economy.

Best of all, you'll be flying with a friend. United Airlines. Now the friendly skies covers the wide Pacific.

Call United or your Travel Agent.

You're not just flying, you're flying the friendly skies.

fly the friendly skies®

United

2,000 sharper-than-ever characters all on a portable LCD display.

Toshiba's newest LCD modules give you 640 × 200 dot displays in a choice of two viewing sizes. One is approximately the size of a magazine, and the other about half that size.

Both sizes put an enormous amount of information on view . . . an array of 80 characters × 25 lines. But still bulk and power consumption are at a minimum. Battery powered, these slim modules interface with various systems through LCD controller without renewing software.

Toshiba's advanced technology has also eliminated surface reflection and developed a sharper contrast which gives a brighter and easier to read viewing screen. And for low light or dark viewing an optional backlightable LCD is available.

These versatile LCDs are ideally suited for applications as displays for personal computers, POS terminals, portable word processors and other display terminals. You can also look to Toshiba with confidence for a wide range of sizes and display capacity to suit your LCD requirements.

TLC-363 *TLC-402*

Specifications

		TLC-402	TLC-363B
Display			
Number of Characters		80×25 (2,000 characters)	80×25 (2,000 characters)
Dot Format		8×8, alpha-numeric	8×8, alpha-numeric
Overall Dimensions (W × H × D)		274.8×240.6×17.0 mm	275.0×126.0×15.0 mm
Maximum Ratings			
Storage Temperature		−20° – 70° C	−20° – 70° C
Operating Temperature		0° – 50° C	0° – 50° C
Supply Voltage	V_{DD}	7 V	7 V
	$V_{DD} - V_{EE}$	20 V	20 V
Input Voltage		$0 \leq V_{IN} \leq V_{DD}$	$V_{SS} \leq V_{IN} \leq V_{DD}$
Recommended Operating Conditions			
Supply Voltage	V_{DD}	5±0.25V	5±0.25V
	V_{EE}	−11±3V Var.	−11±3V Var.
Input Voltage	High	V_{DD} – 0.5V min.	V_{DD} – 0.5V min.
	Low	0.5V max	0.5V max.
Typical Characteristics (25°C)			
Response Time	Turn ON	300 ms	300 ms
	Turn OFF	300 ms	300 ms
Contrast Ratio		3	3
Viewing Angle		15 – 35 degrees	15 – 35 degrees

Design and specifications are subject to change without notice.

TOSHIBA

Toshiba America, Inc.: Electronic Components Business Sector: Head Office: 2692 Dow Avenue, Tustin, CA 92680, U.S.A. Tel. (714) 832-6300
Chicago Office: 1101 A Lake Cook Roac, Deerfield, IL 60015, U.S.A. Tel. (312) 945-1500
Toshiba Europa (I.E.) GmbH: Electronic Components Div.: Hammer Landstrasse 115, 4040 Neuss 1, F.R. Germany Tel. (02101) 1580
Toshiba (UK) Ltd.: Electronic Components Div.: Toshiba House, Frimley Road, Frimley, Camberley, Surrey GU 165JJ, England Tel. 0276 62222
Toshiba Electronics Scandinavia AB: Vasagatan 3, 5 TR S-111 20 Stockholm, Sweden Tel. 08-145600