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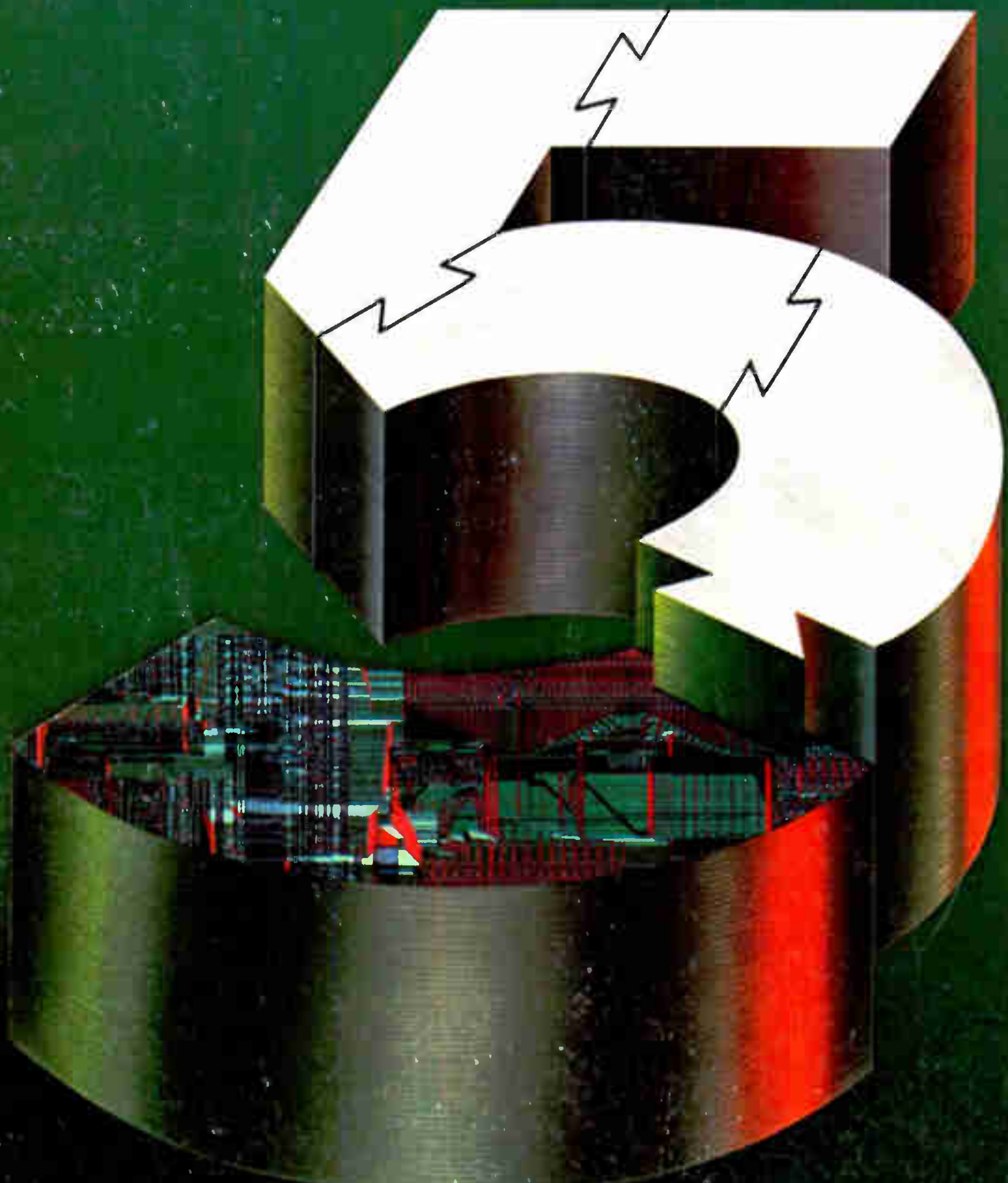
FIVE VLSI CHIPS FORM A SUPERMINICOMPUTER



Electronics

The International Magazine of Electronic Technology and Business

Cover illustrated by David Myers.

The Cover Story

Five chips a supermini make, 121

A proprietary Data General titanium disilicide process makes for a chip set that promises low-cost systems with performance nearly half that of the Eclipse MV 8000.

Major New Developments

Computers that think

The fruits of 30 years' research into artificial intelligence are now starting to show up in practical systems. The hardware is accented in this first part of a two-part special report, 127

Market comeback buoys Wescon

Signs that the electronics industries have come out of the recession abound, so Wescon/83 in San Francisco should be an exuberant ritual, 169

IBM fences in its customer base

A personal computer that in effect puts a System/370 on an executive's desk is part of IBM's strategy to make certain its customers need not go to any other firm for computer gear, 47

Color CRT points the way to office documents

Toshiba ties a color-display interface to a video-disk storage-retrieval system to provide a series of images that guides office workers to the "folder" where a document is filed, 88

NEWSLETTERS

DEPARTMENTS

SERVICES

Electronics Review

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Electronics

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Highlights

Cover: Five ICs realize a superminicomputer, 121

A well-known 32-bit architecture is being reduced to five integrated circuits: a central processing unit, a microsequencer, a floating-point processor, a system input/output unit, and a burst multiplexer channel unit. A titanium disilicide process gives the experimental chip set a big lift in speed.

New technology boosts video conferencing's chances, 103

Full-motion color video conferencing, operating at 56 kilobits a second thanks to data compression, promises to slash the cost of such services. Even as 56-kb/s systems emerge from the labs, however, freeze-frame techniques threaten to steal the nascent market from full-motion systems.

Artificial intelligence enters the commercial world, 127

No longer a laboratory specialty, artificial intelligence is being used in real-world applications, notably in expert and natural-language systems. Part 1 of this special report provides a worldwide overview of the AI industry and of available and projected hardware. An upcoming second part will cover software, natural-language products, and commercial knowledge-based systems.

Byte-wide static RAM speeds up with address-transition detection, 142

By spotting any change in an external address, a technique called address-transition detection cuts the access time of a byte-wide static random-access memory to 45 nanoseconds.

Unix variant serves multiuser transaction processing, 145

An enhancement of AT&T Bell Laboratories' Unix operating system delivers the performance and reliability needed for on-line transaction processing. The additions include a special message-communications system, separate system servers for distributed processing, and a modified file system.

Wescon spotlights computer design aids for VLSI system chips, 169

With application-specific very large-scale integrated circuits growing in importance, Wescon/83 will feature many papers on the computer-aided design, engineering, and program-development systems that make these chips possible. A number of such ICs will be covered in other papers, as are a host of other topics, from packaging to system integration and networking. The show will also feature the unveiling of many new products, and some of the more significant introductions are reviewed on pages 181 through 198.

Coming up . . .

A first look at a radically different microprocessor . . . the state of the art in robotics, a special report . . . what's coming up at the International Electron Devices Meeting.

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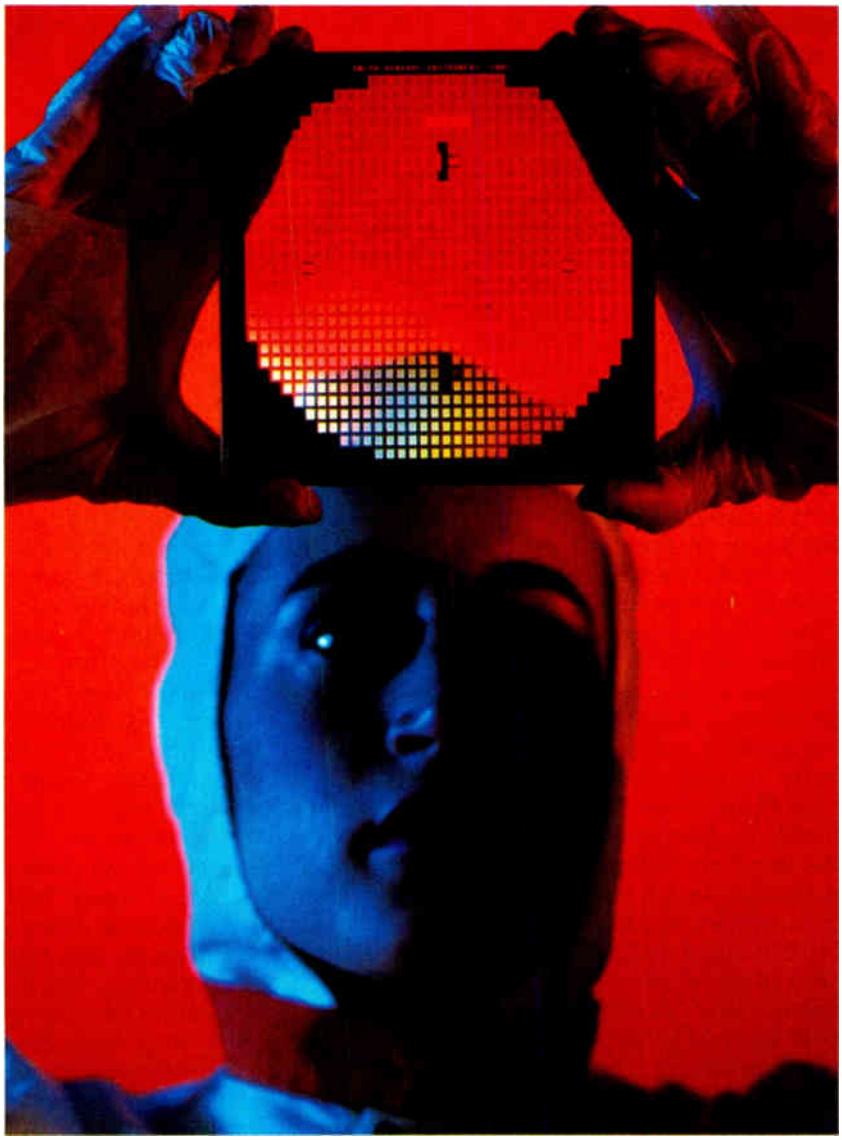

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Circle 5 on reader service card

Publisher's letter

There has been a surge of activity of late in the somewhat esoteric field of computer science known as artificial intelligence, fondly known among its practitioners as AI. After almost three decades of research, AI technology has begun to emerge in a small way into the marketplace.

So it's high time, our editors feel, for an in-depth report on how far AI has come toward actual applications—how viable the technology is today, how much can be transferred to commercial use, what can be expected of it, and, equally important, what are its current limitations.

Soon after Tom Manuel, our senior editor for information systems, and Stephen Evanczuk, our software editor, started their preliminary investigation into AI, they discovered that there was much more going on in the field than they had suspected. Along with the work in the U. S., they found there are substantial programs under way in both Japan and Western Europe. When the reporting started piling up from our international bureaus, they realized that they would have so much material that they would have to break the report into two parts to cover the subject adequately.

Our man in Tokyo, Charles L. Cohen, discovered many Japanese AI hardware projects—some associated with the fifth-generation project, others outside it—that are reported here for the first time. Kevin Smith, our London-based senior editor, found much AI activity in the UK, too.

Says Cohen, "I tackled the Japanese side of the AI feature with great enthusiasm, even though success in AI could lessen the need for my specialty: interviewing Japanese researchers in their own language. One goal of the work is automatic translation." But Charlie figures that overall the AI programs will provide him with many new story opportunities. The scheduling of interviews for the report, he notes, "proceeded like the linked list of a LISP program. One interview would reveal the name of another source who would in turn tell of others in the field."

Cohen believes that the present emphasis on AI hardware development in Japan could provide Japanese computer scientists with a chance to make their mark in new languages—something at which they haven't been too successful so far.

Meanwhile, the quest around the world to get to market with AI systems will accelerate. "One of the key driving forces towards the commercialization of AI is the crying need for easier ways to program and access computer systems," says Tom.

Part 1 of the report that examines the whys and wherefores of AI starts on page 127. It contains an introduction to the commercialization of AI, a short history of the discipline by Clifford Barney of our Palo Alto office, and a close-up of the hardware being offered and developed for AI applications. "In the second part, scheduled to appear in the Dec. 1 issue, we will examine the software side of AI, including programming languages, development tools, and applications," Tom notes.

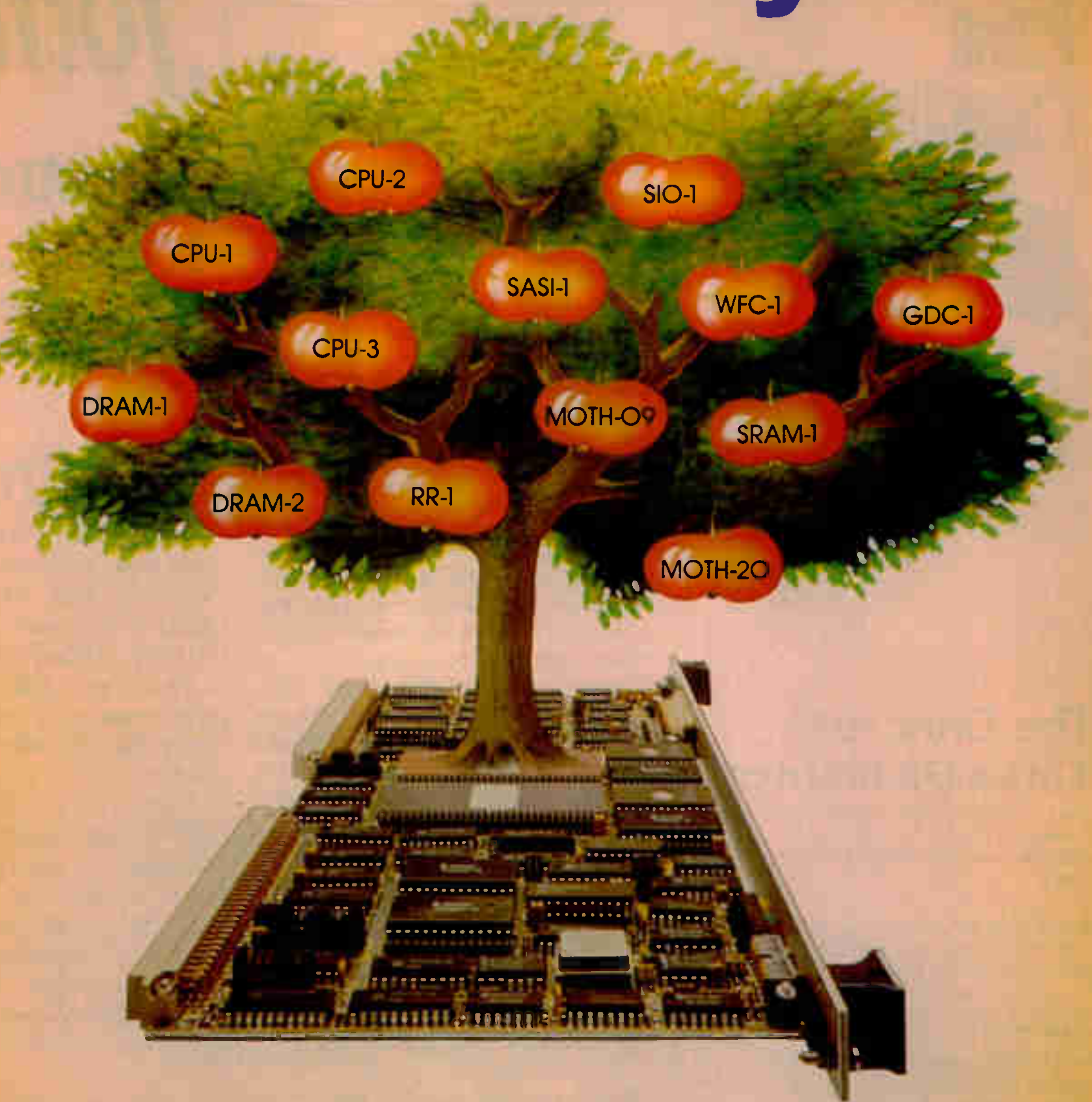
The calendar for November is crowded with meetings and conventions all over the world, and our editors have previewed three of the month's major ones in this issue.

In the U.S., the major event for the electronics industries is Wescon, traditionally a September show but this year a November one. Some 75,000 professionals are expected to turn up in San Francisco for it.

Following our custom, we have done a two-part curtain raiser for Wescon. Associate managing editor Howard Wolff coordinated our report on the technical sessions, which starts on page 169. After our technical specialists had sifted through the papers to single out the significant ones, Howard became convinced that this year's sessions—with 40% of them devoted to CAD/CAM and its accoutrements—mark the beginning of still another new era for electronics technology: that of application-specific integrated circuits.

The other half of our Wescon preview covers some of the show's outstanding hardware (p. 181). "There are some very novel instruments as well as a considerable number of design aids," reports senior editor Jer-

The VME Family Tree



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Publisher's letter

emy Young, who stitched together the new-products reporting from our bureaus around the U. S. Jeremy already has them at work scouting out salient hardware that will appear on the floor at the late-November Comdex show in Las Vegas.

In Europe, show-of-the-month honors go to the Salon des Composants. Traditionally, the Salon was part of the April-in-Paris scene. But it now has been shifted to November and will be held every other year (alternating with Electronica in Munich). The venue has been changed as well, to the new Parc d'Expositions Paris-Nord.

People doing business in European components markets hope these changes will augur a more substantial one—a quickening of sales. But after talking with the major French firms and absorbing the inputs of Kevin Smith in London and John Gosch in Frankfurt, Paris bureau manager Robert Gallagher could find only a few indications that good business news will offset the November chill at Composants (p. 97).

A less subdued optimism can be expected at the Interkama, the dominant European show for control and instrument makers. The people behind the triennial Düsseldorf show, reports John Gosch, see a chance of a return to double-digit growth for their industry next year (p. 106).

This year, our regular, every-two-weeks publishing schedule called for three issues in December. Because the year-end holidays seriously erode everybody's reading time, we have decided to publish only two issues then, on Dec. 1 and Dec. 15. The latter, though, will be a double issue with two special reports, the annual Executive Outlook and a special report on military electronics. After that, we'll start the New Year with the traditional World Markets Forecast in the Jan. 12, 1984, issue.

Paul W. Blin

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Circle #9

In my opinion

Computer-assisted crime: a legislative challenge

by Bill Nelson
U. S. Congressman, 11th District, Florida

Computer-assisted crime poses major difficulties for the future now that computers are becoming increasingly available in our society to assist in whatever work we have to perform. For when many people work daily with a powerful tool like the computer, there will undoubtedly be some who will overstep the boundary between the legitimate and criminal uses of this device.

Familarity with computers is spreading rapidly to tens of millions of working Americans. Newspaper headlines cite rising computer criminal activity. A recent report told of a former employee of the Federal Reserve System who used a stolen password to tap into confidential computer files containing sensitive information on the nation's money supply. The 414s, a group of Milwaukee teenagers, made incursions into more than 50 business and institutional computers, among them the Los Alamos National Laboratory for nuclear weapons. In my own state of Florida, a health-insurance–claims agent generated more than $240,000 by making fraudulent claims on behalf of herself and her family.

Time for a law. Legislation to strengthen the powers of Federal prosecutors to bring to justice those who illegally penetrate computer systems is obviously in order. Accordingly, I—joined by 107 co-sponsors—have introduced "The Federal Computer Systems Protection Act of 1983" to make crimes by computer a specific Federal offense. H. R.1092 makes it illegal to tamper with Federal government computers, the computers of financial institutions guaranteed by the government, and computers operating in interstate commerce or using interstate facilities.

This legislation gives Federal prosecutors a powerful tool to combat the growing threat of computer crime to the national economy and to national security. Prosecutors are unable to make effective cases against computer criminals because the 40 or so Federal laws that could be applied were designed originally to control other kinds of criminal activity. H. R.1092 gives the courts a clear-cut basis for punishing anyone who steals information from a computer or who alters or destroys information in a computer maliciously or for personal gain.

The bill is written to protect a specified computer system from any persons who would "use, or attempt to use, a computer with intent to execute a scheme or artifice to defraud, or to obtain property by false or fraudulent pretenses, representations, or promises, or to embezzle, steal, or knowingly convert to his use or the use of another, the property of another."

A stiff penalty. Anyone convicted of violating this act would be subject to a fine of up to two times the value of the gain from the offense or a minimum of $50,000 and up to five years in prison. Intentional damage of a computer or its data or intentional denial of access to legitimate users could result in a fine of up to $50,000 or five years in prison or both.

We need a national statute to defend our Federal government computers from unauthorized entry, to protect the developing electronic funds-transfer system, to preserve the integrity of the Federal Reserve System, and to safeguard business computers in a world where a computer terminal may be on every desk in every home.

At the same time, we have tried to draft this bill so as not to discourage the legitimate inventiveness of computer programmers. We recognize the need for interaction between people and computers in a familiar pattern.

Limiting access and other necessary security measures cannot be so strict as to prevent computers from being used in their fullest potential in government or the private sector. Employees must have ready access to computers to get their jobs done with a minimum of security hassle, just as they previously needed access to a typewriter, a telephone, or a library.

H. R.1092 is intended to allow that freedom, while providing the protection of legal prosecution of the willful or malicious wrongdoer. I am hopeful that, with the help of my congressional colleagues, the computer industry—its managers, auditors, operators, and security analysts—and law-enforcement agencies, we will be able to enact and enforce this legislation, which will stand the test of time—even in an industry that is advancing and changing every day.

Electronics *will periodically invite the expression of outside views on this page concerning issues of importance to the electronics industries.*

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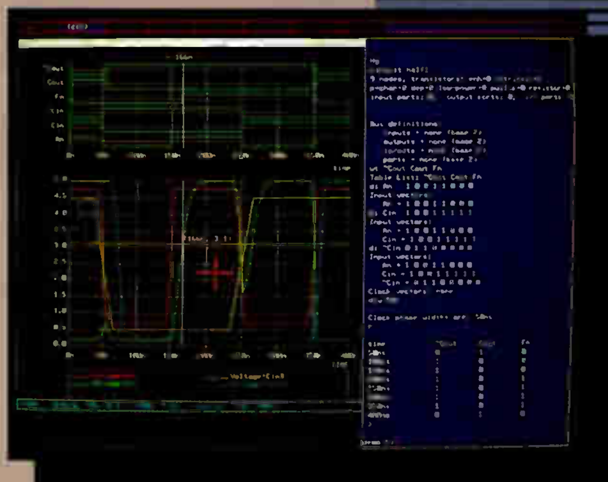

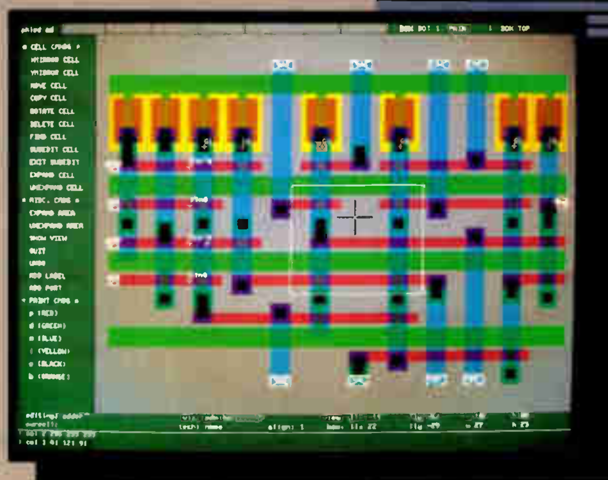

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People

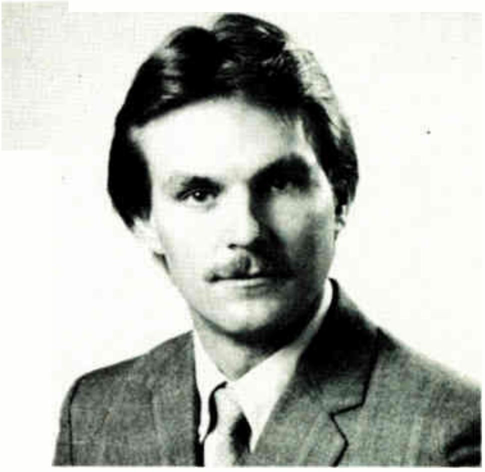
GenRad's Prang aims to merge engineering, marketing talent

For makers of automatic board-test equipment, staying on top of the market no longer means turning out a better test system and doing nothing else. "We're looking at a much bigger picture, now that manufacturers have bought the idea of the integrated factory," observes GenRad Inc.'s Joseph A. Prang.

In August, Prang assumed a new position: strategic marketing and research manager at the Concord, Mass., firm's Production Test division. His mandate, he says, is to integrate the expertise of engineers and marketers, and to that end he is helping to plan products that will connect board testers to other "islands of automation" on the factory floor.

"Today's ATE houses should be thinking about how to interface their products with computer-aided engineering, design, and manufacturing systems and about feedback strategies that will let test data help improve the overall process, instead of just flagging problems," says Prang. The marketer's task—cultivating joint-development agreements with CAD, CAM, and CAE suppliers—must balance the engineer's traditional desire to build ever-better testers.

The balance can be a delicate one, Prang notes, since interfacing testers to other systems may impose performance tradeoffs. The problem is then to stay competitive with "the ATE house that is still holding to a short-term niche orientation and could care less about anything but tweaking its own product." Prang believes that the extra effort will pay off when productivity gains made possible by integrated factory systems persuade customers that team-player test systems are better buys than stand-alone superstars.



Integrator. Gordon Prang believes that ATE makers should be concentrating on integrating their test equipment with CAD and CAE systems.

At 28, Prang seems like a natural to orchestrate engineering and marketing efforts. He holds a BS degree in electrical engineering and a master's in business administration from Purdue University. Co-op jobs in his school years exposed him to engineering, field-service, and programming at such companies as IBM and Standard Oil. In 1979 he joined GenRad as a marketing engineer, and a year later he became marketing manager for the firm's 227X family, which last year earned GenRad the lion's share—a 36% slice—of the in-circuit board-test market.

Bell opens a California window for his Northern Irish firm

A Belfast, Northern Ireland, software house that specializes in languages for Digital Equipment Corp. machines is bound to face limited horizons. To loosen these constraints, Gordon Bell, the managing director of Software Ireland Ltd., took a not-so-obvious step: he decided to expand his market for Unix operating systems by opening an office in Menlo Park, Calif. Bell's product, Sibol, is a computer language and compiler designed to translate Dibol, the best-known application language for DEC computers and for Unix-based personal computers or microprocessors.

Bell is impressed by the huge potential of AT&T Bell Laboratories'

People

Going west. Gordon Bell has opened an office of his Belfast software house in California's balmier business climate.

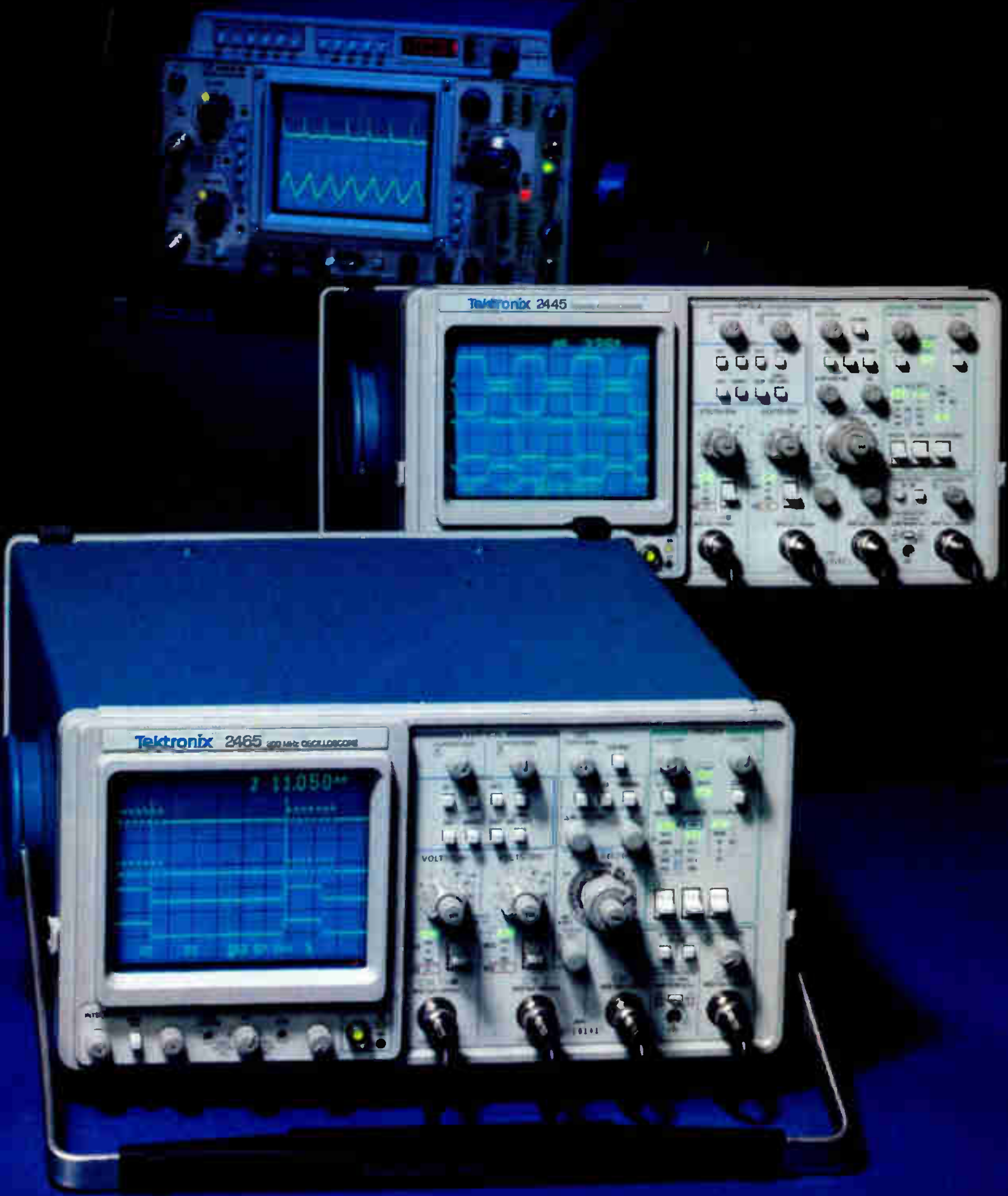
Unix operating system. Some 40 companies already make Unix-based computers, and their numbers are likely to grow, says the softspoken, 38-year-old native of Belfast, who holds a bachelor's degree in mathematics from Queens University, Belfast. He is not related to C. Gordon Bell, the former DEC vice president now with Encore Computer Corp.

Then, too, a large base of DEC installations use Dibol. "We believe there are some 70,000 Dibol installations in the U. S. and well over 1,000 DEC OEMs," Bell continues. All of them could be candidates to use Sibol, which would make it possible for executives to access data bases from small personal computers.

Software Ireland belongs to the ICS Computing Group, whose programming operation has been a part of Bell's life for 14 years. The group also includes ICS Computing Ltd., the largest Irish DEC original-equipment manufacturer, with a network of service bureaus, as well as time-sharing, turnkey, and support centers. Working with ICS, Bell became intimately familiar with Dibol, Basic Plus, and Basic Plus-2, the main application languages for DEC PDP-11 and VAX-class machines.

When Software Ireland was founded, back in October 1979, Bell moved over to it. The organization has already enjoyed some success with Sibol, having signed to the colors more than a dozen computer manufacturers who market their own machines, including Fortune Systems, Plexus Computers, and Codata Systems, as well as Zilog. □

From the folks who gave you the 465B: the new 2445 and 2465.



The new industry standards in 150 and 300 MHz scopes.

Compare Tek's new 2400 Series against its toughest competitor: its predecessor. For years, the Tek 465B has stood as the industry standard for portable scopes. But the new 2445 and 2465 are faster. More accurate. More versatile. And their microprocessor-based architecture makes them even easier to use. In performance, price and reliability they set the new standard in portable scopes.

Both the 300 MHz 2465 and 150 MHz 2445 begin with high performance basics like you've never seen before. Including standard delayed sweep Δ-Time up to 0.5% accuracy. Sweep speeds to 1 ns/div in the 2445 and 500 ps/div in the 2465. Selectable 1 MΩ/50 Ω input for excellent signal fidelity. Triggering to at least 250 MHz in the 2445 and to at least 500 MHz in the 2465, that extends the usefulness of the scopes well beyond their vertical bandwidth.

Just as importantly, the new 2400 Series is proof that more capability needn't be more complicated. From straightforward operation of four channels and sweep slaved calibrator to the backlit front panel indicators and the comfortable feel of the controls, the Tek 2400 Series minimizes errors and maximizes your confidence.

Waveform cursors with CRT readout make possible immediate, effortless measurement of parameters like voltage, time, frequency, ratio and phase. Use the vertical and horizontal cursors to obtain quick readouts—or set up a delayed sweep for even greater accuracy. Delayed B-sweep can display any portion of the A-sweep, including the A-sweep trigger event.

You can select from the most versatile and easy-to-use of all triggers: Trigger from any of the four channels. Select Auto, Norm, Single Sequence or the new Auto Level mode, that provides hands-off triggering on any waveform above 50 Hz. In addition to the usual coupling features, Noise Reject is provided to improve trigger stability in the presence of moderate amplitude noise of any frequency.

At all speeds, trigger holdoff is variable to at least the sweep duration.

Tektronix backs the reliability of the 2400 Series with the longest warranty ever offered: a full three years on all parts and service, including the CRT. Low-cost service plans extend the coverage even further.

This new standard of scope reliability is made possible in part by a higher level of integration and advanced circuit design—including laser-trimmed hybrid attenuators that never need recalibration—plus a new meshless scan expansion CRT.

Laser-trimmed hybrids have also been applied to the new companion P6131 probes, providing full bandwidth at the probe tip.

	2445	2465
Bandwidth	150 MHz	300 MHz
Max. Sweep Speed	1 ns/div	500 ps/div
No. of Channels	4	4
Vertical Sensitivity	2 mV/div	2 mV/div
Δ-Volts Δ-Time Cursors	Yes	Yes
Scale Factor Readout	Yes	Yes
Trigger Level Readout	Yes	Yes
Digital Display	CRT Readout	CRT Readout
Trigger Freq. Range	250 MHz	500 MHz
Trigger Modes	Auto Level, Auto, Norm, Single Sequence	
Weight	9.8 kg/21.3 lb	9.8 kg/21.3 lb
Temp./Shock/Vibration	−15°C to 55°C/50 g's/4 g's	
Δ-Time Accuracy	0.5%	0.5%
Accuracy, Vert/Hor	2%/1%	2%/1%
Warranty	3-year including CRT (plus optional service plans to 5 years in most countries)	

To learn more about these and other portable scopes, contact your local Tek sales representative. Or call the Tek National Marketing Center. You can order, or obtain literature, through the Tektronix National Marketing Center. Technical personnel, expert in oscilloscope applications, will answer your questions and can expedite delivery. Direct orders include probes, operating and service manuals, 15-day return policy, full Tektronix warranty and worldwide service back-up.

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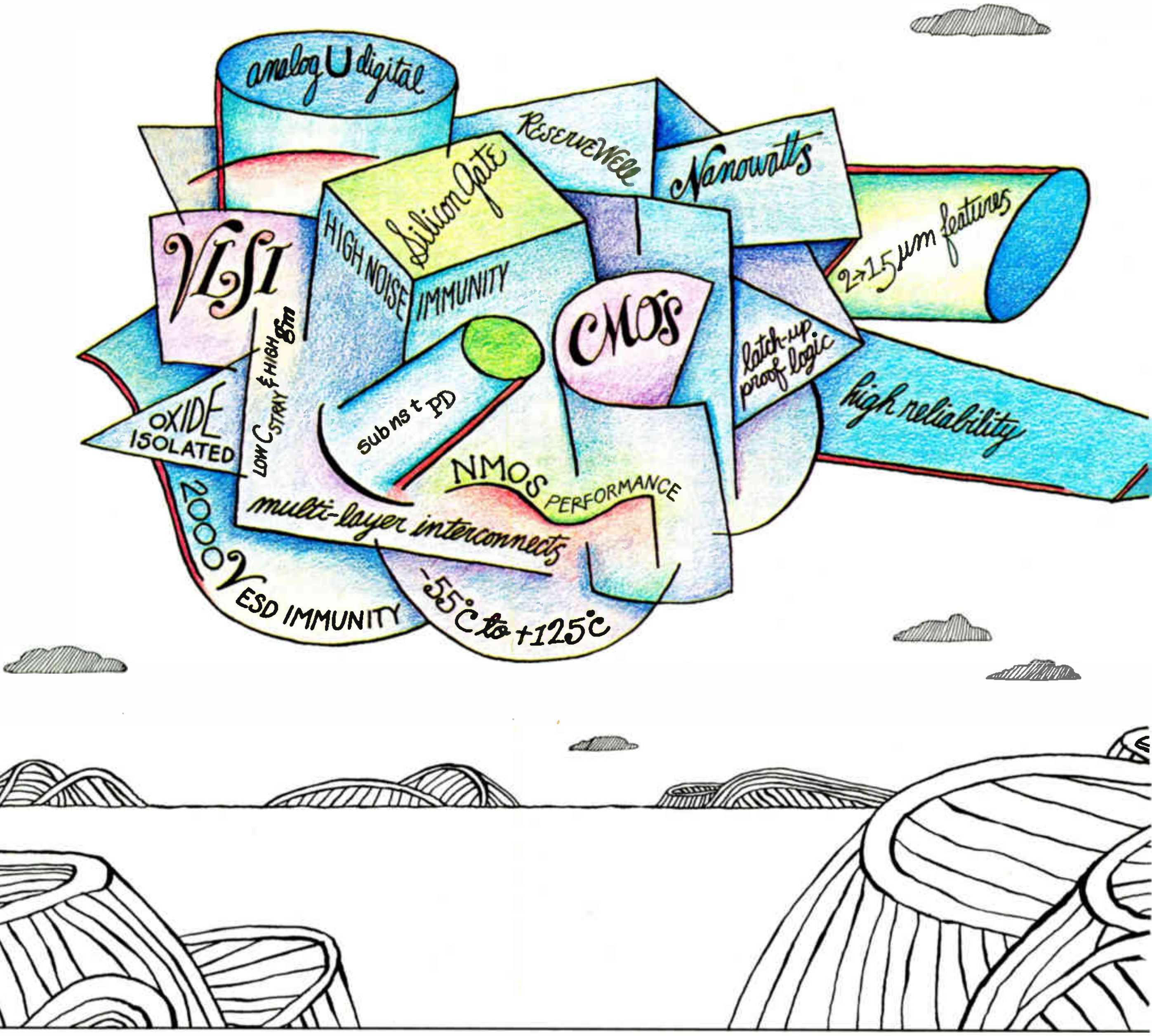
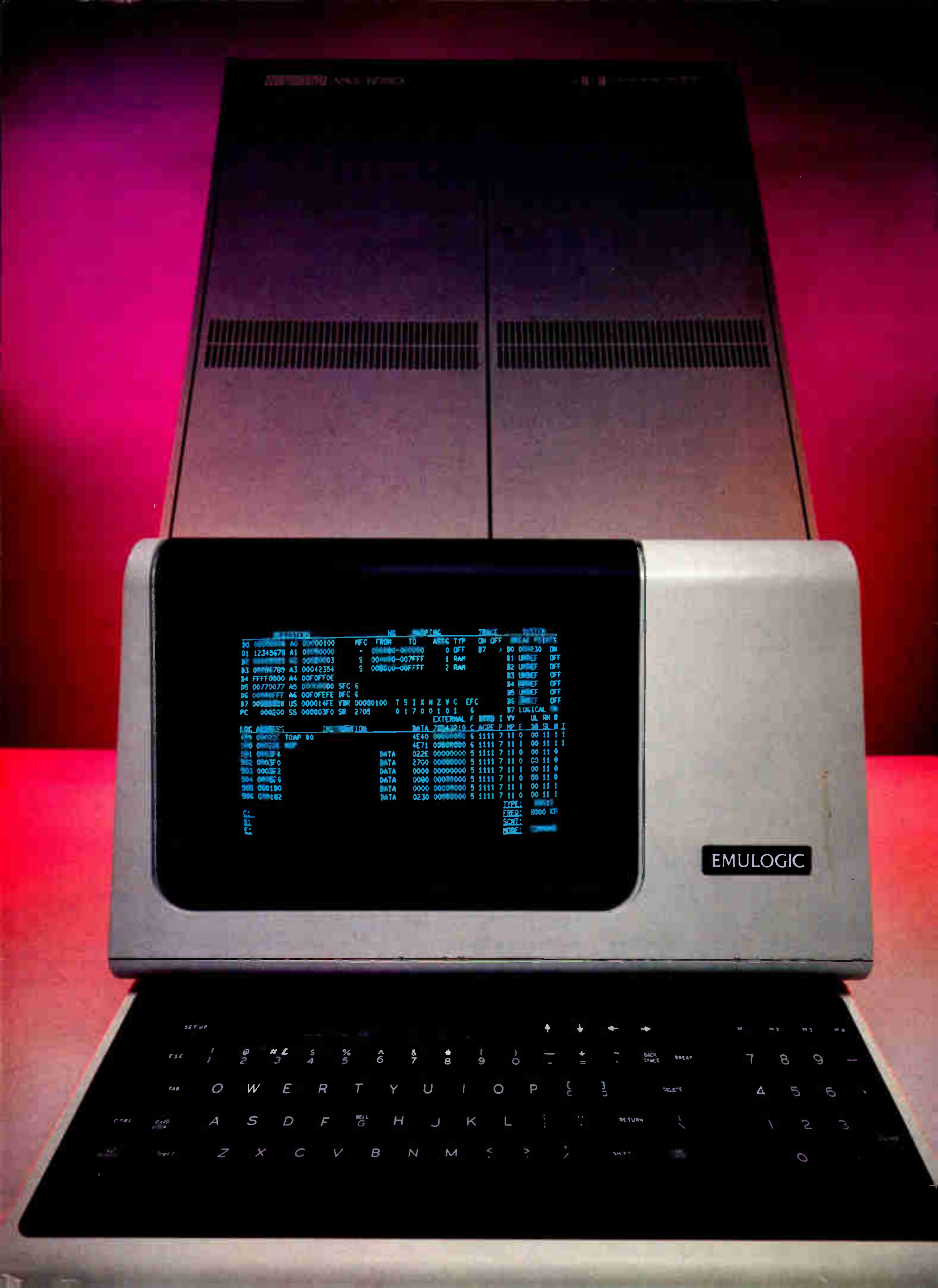
We call our family of processes microCMOS. They use smaller geometries, of course: in the 2-3 μm range. They also use advanced silicon-gate and

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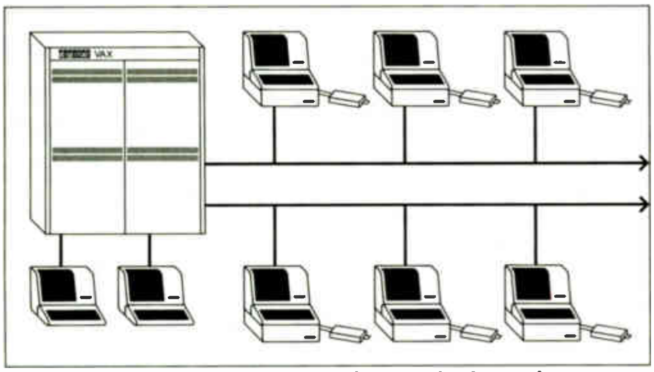
Enter EMUNET-2.

It's the first system to harness *all* of VAX's 32-bit power, *all* of VAX's development tools, *all* of VAX's information management capabilities, and *all* of VAX's mass storage and peripheral facilities, *all* for microprocessor development.

Better still, EMUNET delivers VAX's awesome power right to the workstation of every hardware and software engineer on your development team. Even if that means 60 individual designers.



EMUNET-2 supports as many as 60 hardware and software designers.

It's all made possible by our unique multi-drop, 1-Mbaud coaxial cable that links VAX® to every emulation workstation. At that speed, your designers won't waste time waiting to download their programs.

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Of course, our system is equipped with all the cross assemblers, linkers, symbolic debuggers, and other software tools you need to emulate today's most popular 8- and 16-bit processors. Including the 68010, 68000, 8086, 8088, and more. And you can run the software on your VAX or any local workstation.

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Is Silicon Valley a nest of spies?

Once again, Federal agents have swooped down and charged an American with selling high-tech secrets to an agent of the Soviet Bloc: in this case, details of missiles to a Polish diplomat.

The incident points up the dangers of cramming so much information into so small an area—Silicon Valley, that mother lode of semiconductors on the San Francisco peninsula. It also spotlights the behavior of the daily newspapers, particularly when they report a news story that involves what they even now think of as a black art—an attitude that is at once unfair, inaccurate, and dangerous. At least one major daily has pictured the valley as a hothouse of would-be entrepreneurs made bitter by their failure to achieve overnight riches and willing to sell high-tech secrets to Eastern Bloc nations as just another route to riches.

That is just not so. Despite the many visions of profligate swingers eager to sell out for big bucks, Silicon Valley is a place very much like any other: full of hard-working people neither more nor less patriotic than their fellow-countrymen in other places. The only difference is the concentration there of high-tech innovators, men and women who may work even harder than most Americans do.

Of course, many companies need more security and less trust in human virtue. Individual companies have in fact made admirable efforts to prevent thefts of industrial secrets by competitors, and semiconductor makers have been working hard to stop what occasionally seems to be an epidemic of stolen devices.

All those involved, even peripherally, in this industry must recognize that the United States is caught up in a cold war and that the sophisticated electronic systems that guide and propel U. S. missiles, aircraft, and tanks and that circle our planet in satellites are not only weapons but also prizes in that war. Every infantryman, or former infantryman, knows enough to take the high ground and hold it; nowadays, that high ground is crowded with electronic systems.

Nonetheless, it is wholly irresponsible to represent the Silicon Valley as a standing army of hot-tub freaks, sybarites, and amateur spies looking for a connection with the right payoff. The daily press should do a better job of keeping itself informed about what is happening there—even in the intervals between sensational stories about bumbling silicon spies. And electronics companies, for their part, must redouble their efforts to keep the few rotten apples from tainting the harvest.

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Meetings

29th Conference on Magnetism and Magnetic Materials, American Institute of Physics, IEEE (Fred J. Werner, Westinghouse Research and Development Center, 130 Beulah Rd., Pittsburgh, Pa. 15235), Pittsburgh Hilton Hotel, Pittsburgh, Nov. 6–11.

Asilomar Conference on Circuits, Systems and Computers, IEEE (Herbert E. Rauch, Lockheed 52-56/205, 3251 Hanover St., Palo Alto, Calif. 94304), Asilomar Conference Center, Pacific Grove, Calif., Nov. 7–9.

Wescon/83—Western Electronic Show and Convention, Electronic Conventions Inc. (8100 Airport Blvd., Los Angeles, Calif. 90045), Moscone Center, San Francisco, Calif., Nov. 8–11.

Productronica '83—5th International Trade Fair for Electronics Production, Munich Fairs and Expositions AG (Messegelande, Box 121009, D-8000 Munich, West Germany), Fairgrounds, Munich, Nov. 8–12.

Interkama—9th International Congress for Instrumentation and Automation, Düsseldorfer Messe GmbH (P. O. Box 320203, D-4000 Düsseldorf, West Germany), Fairgrounds, Düsseldorf, Nov. 9–15.

16th Connectors and Interconnection Technology Symposium, Electronic Connector Study Group Inc. (Box 167, Fort Washington, Pa. 19034), Franklin Plaza Hotel, Philadelphia, Pa., Nov. 14–16.

Autofact 5 Conference and Exhibition, Society of Manufacturing Engineers (One SME Drive, P. O. Box Dearborn, Mich. 48128), Cobo Hall, Detroit, Mich., Nov. 14–17.

Paris Electronic Components Exhibition, Société de Diffusion des Sciences et des Arts (20 rue Hamelin, Paris, France 75116), North Paris Exhibition Grounds, Nov. 14–18.

Robotic Intelligence and Productivity Conference, Wayne State University (Department of Electrical and Computer Engineering, WSU, Detroit, Mich. 48202), WSU, Detroit, Nov. 18–19.

Global Telecommunications Conference, IEEE (Estil Hoversten, M/A Com Linkabit, 3033 Science Park Rd., San Diego, Calif. 92121), Town and Country Hotel, San Diego, Calif., Nov. 28–Dec. 1.

Comdex/Fall '83—5th National Fall Conference for Independent Sales Organizations, The Interface Group (300 First Ave., Needham, Mass. 02194), Convention Center, Las Vegas, Nev., Nov. 28–Dec. 2.

Semiconductor Interface Specialists Conference, IEEE (E. H. Nicollian, AT&T Bell Laboratories, 600 Mountain Ave., Murray Hill, N. J. 07974), Bahia Mar Hotel, Fort Lauderdale, Fla., Dec. 1–3.

Semicon/Japan '83, Semiconductor Equipment and Materials Institute (625 Ellis St., Suite 212, Mountain View, Calif. 94043), International Trade Center, Tokyo, Dec. 1–3.

International Electron Devices Meeting, IEEE (Melissa Widerkehr, Courtesy Associates, 1629 K St. N. W., Washington, D. C. 20006), Washington Hilton Hotel, Washington, D. C., Dec. 5–7.

Winter Simulation Conference, IEEE, National Bureau of Standards, *et al.* (P. Saunders, A415 Administration Bldg., NBS, Washington, D. C. 20234), Marriott Crystal Gateway Hotel, Arlington, Va., Dec. 12–14.

Southcon/84—High-Technology Electronics Conference, IEEE (Electronic Conventions Inc., 8110 Airport Blvd., Los Angeles, Calif. 90045), Orange County Convention Center, Orlando, Fla., Jan. 17–19.

Seminar

Power Semiconductor Devices Workshop, National Bureau of Standards, IEEE (Frank Oettinger, NBS Electron Devices Division 721, Washington, D. C. 20234), NBS, Gaithersburg, Md., Dec. 8.

development system for became the most flexible.

Motorola's HDS-400™ Hardware/Software Development Station now allows real-time emulation of three M68000 Family microprocessors, and operates under four host/operating system configurations. Many more users can now apply the demonstrated development efficiencies of the high-performance HDS-400 to a broader range of products.

Four host/operating system configurations.

The HDS-400 Control Station introduced last year operates with Motorola's EXORmacs® host over an RS-422 serial link. It's joined now by the new M68KHDS400A Control Station with an RS-232C serial link for interface to either Motorola's VME/10™ or a DEC VAX™ host. Both the EXORmacs and VME/10 hosts operate under the VERSAdos™ operating system. The VAX host can operate under either VMS™ or UNIX™.

Choose your host: EXORmacs for multi-user support; VME/10 for integrated host/terminal operation; VAX, with either VMS or UNIX to let you utilize your current system. With any of these hosts or operating systems, the HDS-400 provides a complete development system for the M68000 Family of microprocessors.

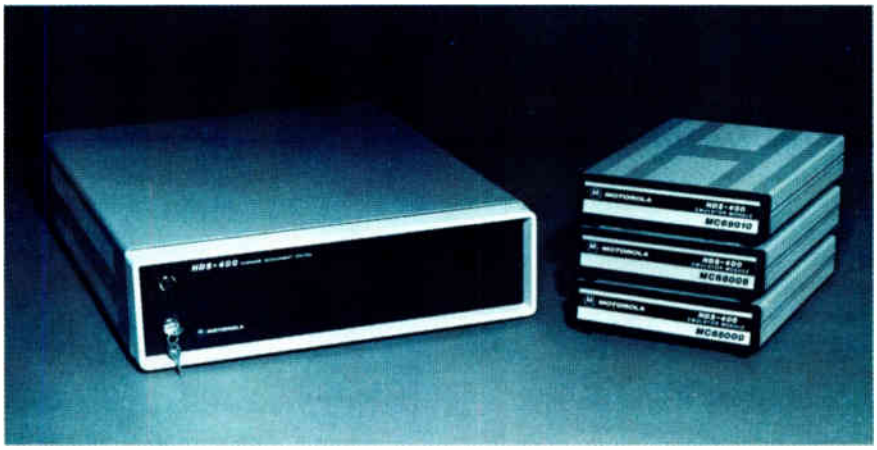
Three emulator modules.

Three interchangeable emulator modules are now available to operate with any of the four HDS-400/host/operating system configurations. In addition to the 16-bit MC68000 Emulator, modules for real-time emulation of the 8-bit MC68008 and the 16-bit Virtual-Memory MC68010 are also available. It's the **only** development system that supports all three — the perfect match of a high-performance development system with the M68000 Family of high-performance microprocessors.

You choose the HDS-400 Development Station with complete confidence that you have full compatibility for your growth path throughout the M68000 Family, including upgrade to the 32-bit MC68020 in 1984. If you're already designing with the M68000 Family, the HDS-400 is the ideal complement: compatibility and growth path are powerful reasons to choose the M68000 Family for future product development.

Optional BSA enhances functionality.

Each HDS-400 emulator supports up to 16 target program breakpoints, within four address ranges, in either RAM or ROM. Optional incorporation of the Real-Time Bus State Analyzer (BSA) significantly enhances system functionality. The BSA provides additional complex event breakpoints which can be specified by up to seven events from 79 qualifier lines. It also adds a sequential trigger mode, a window trigger mode, and performance histograms — powerful debugging and monitoring utilities.



Compatibility plus flexibility.

You can do hardware development and software debugging on the same HDS-400 Development Station. The system helps simplify and shorten your product development cycle, and reduce your development costs. It helps you put a better product on the market faster.

Whether you're designing with the MC68000, the MC68008, the MC68010 or all three, the HDS-400 is the perfect complement. That's compatibility.

Now you can support this powerful development station from either of two Motorola hosts or from your VAX host with either of two operating systems. That's flexibility.

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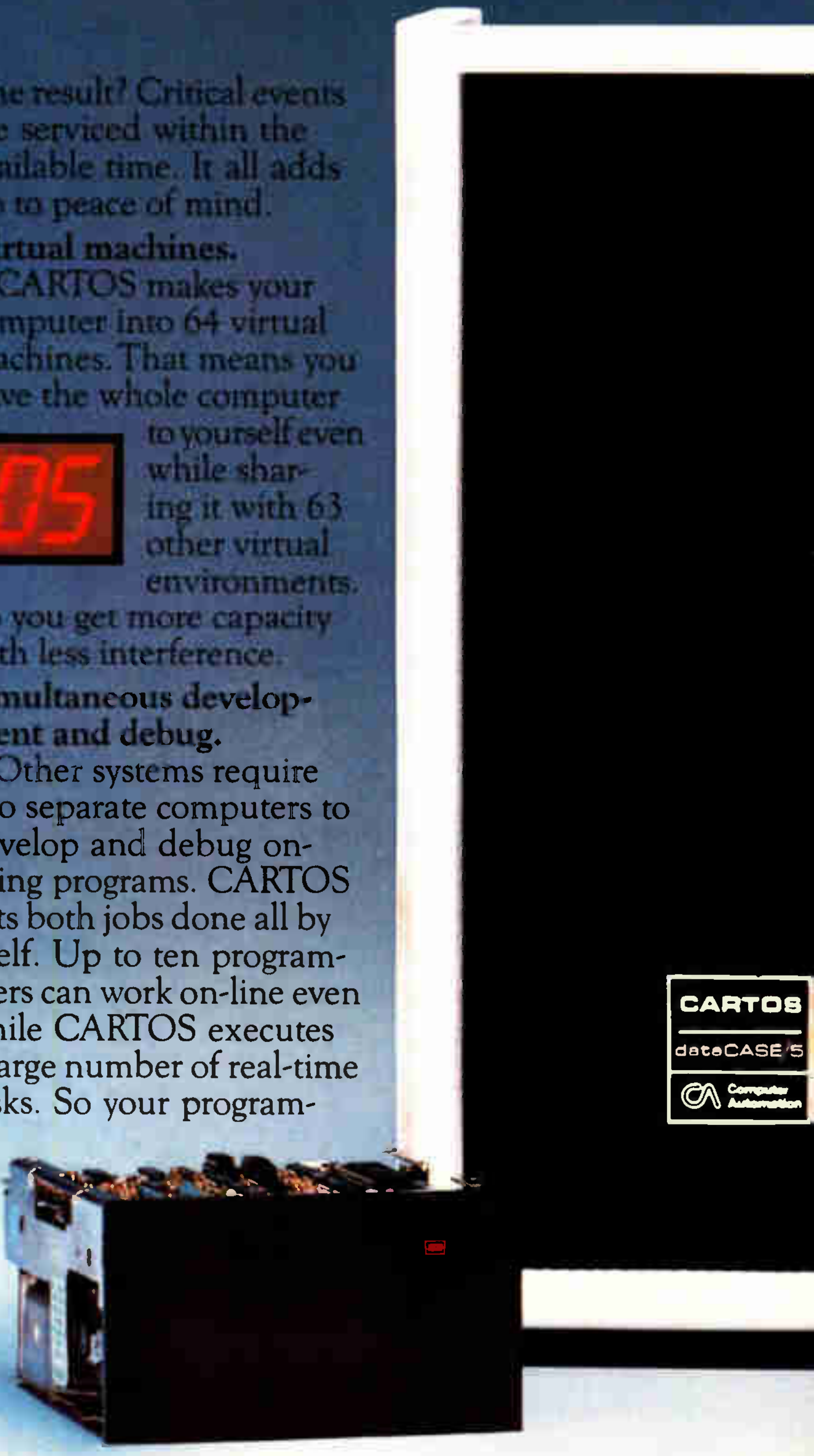

News update

■ It's been a little more than a year since RCA signed an agreement to second-source Motorola's complementary-MOS versions of its 6805 line of microcomputers and peripherals [*Electronics,* Sept. 22, 1982, p. 54]. RCA has yet to deliver the parts it promised. Nonetheless, Motorola must like the progress being made because the two companies are putting the final touches on what RCA's Jim George, director of LSI product operations, calls Phase II of the agreement. These new provisions call for RCA's Solid State division, based in Somerville, N. J., to team up with Motorola's Austin, Texas, microprocessor operation on high-speed (4.2-megahertz) versions of the 6805 line.

In the meantime, RCA continues to work on its six promised parts: three peripherals—a real-time clock, a serial interface, and a read-only memory—as well as a one-chip microcomputer and two microprocessors. The introductions are now set for the first quarter of 1984 rather than the third quarter of 1983, as planned originally.

Implantations. The delay was due in part to RCA's lack of familiarity with the 5-micrometer process, which demands implanted sources and drains rather than diffused ones. "We wanted to make sure that the process was okay," says George, "and we did not want to come up short of parts in stock." He adds that RCA's problems were really no more unusual than those that might be encountered by any normal start-up. Reliability testing has been finished at RCA's plant in West Palm Beach Garden, Fla., where the company is building up stock before the official introductions.

As agreed, Motorola will make the microcomputers, and RCA, the peripherals, in a 3-μm n-well C-MOS process using polysilicon load resistors. An official announcement of the new understanding is imminent. A spokesman in Austin says that Motorola is "as happy as it can be with the agreement." Together, the two companies claim more than 40% of the C-MOS logic and microprocessor market. –**Steve Zollo**

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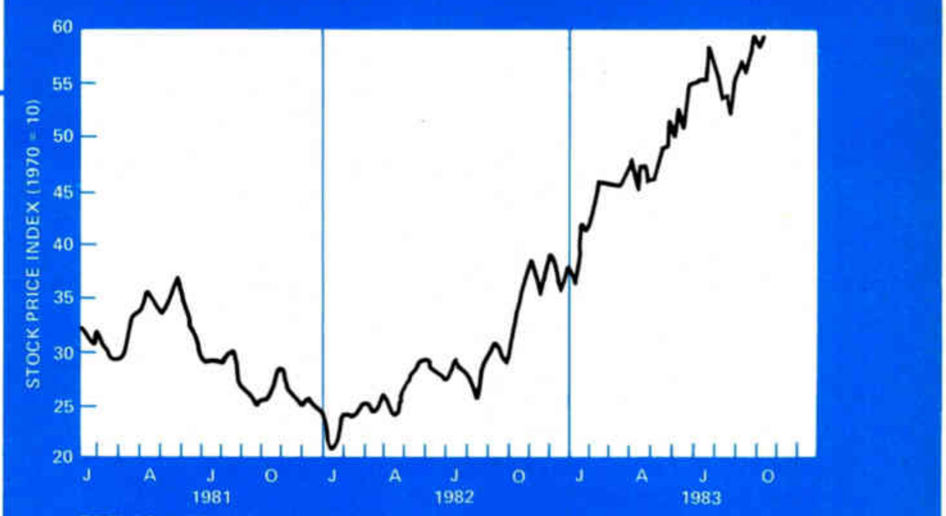
Business activity

"Trends in semiconductor and components stocks" records the stock market activity of a selected group of publicly owned semiconductor and components manufacturers. The index weights the companies by size and therefore reflects their relative performances.



TRENDS IN SEMICONDUCTOR AND COMPONENTS STOCKS

A 1981 tax-law change that provided higher credits for research and development spending has led to a 9% gain in R&D expenditures by electronics firms during 1982. The tax credits are set to expire at the end of 1985, but if they are made permanent and expanded to software R&D, spending by electronics firms could rise by 20% to 25% a year. So claims a survey by Dallas management consultants *Bain & Co.* The survey, conducted through a random sample of the 2,300 members of the *American Electronics Association*, dealt only with percentage increases or decreases in R&D spending by AEA members and not with the dollar amounts actually spent. Bain also found that 80% of the firms responding would be interested in joint R&D efforts. "We recommend strongly that the R&D tax credit be made permanent," says AEA senior vice president Ralph Thomson. The 1981 change granted a 25% tax credit on R&D budgets raised above those of a previous year. The AEA believes also that "some companies refrain from participating in R&D joint ventures due to lack of definition in Federal antitrust regulations."

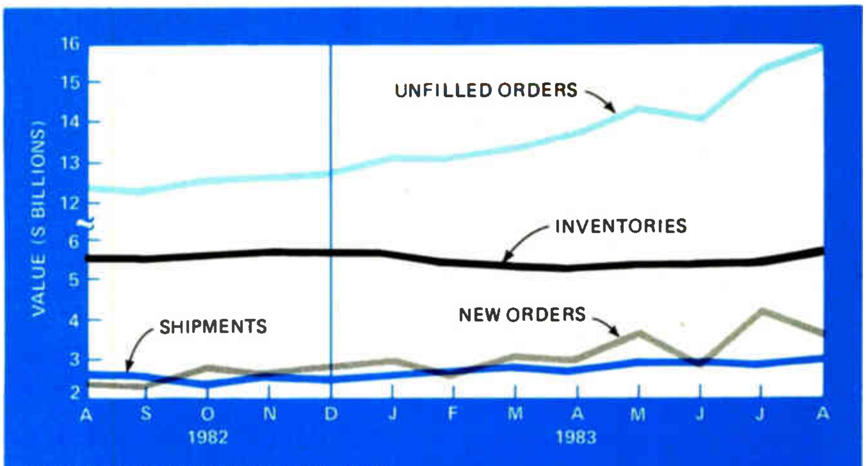
Elsewhere in the R&D world, the *National Science Foundation*, in its latest report on that subject, says that industrial R&D spending rose 17% in 1981. Accounting for about 70% of all U. S. R&D expenditures, industrial firms shelled out $52 billion in 1981, up from $44.6 billion in 1980. The NSF notes that, discounting inflation, the gain was 7%—"well above the 5.4% average annual rate of growth registered between 1975 and 1980." Federal support for R&D spending increased 7% in constant dollars from 1980 to 1981, "more than double the 2.9% average annual rate of growth" from 1975 to 1980. Corporate spending for 1981 rose 6% in constant dollars—the first time since 1963 that company-funded R&D grew at a lower rate than did Federally funded R&D.

Financings . . . Flexible disk-drive maker *Drivetec Inc.*, of San Jose, Calif., raised $5 million in a second round of equity financing. This increases its total financing to $8 million . . . *Inference Corp.*, of Los Angeles, Calif., secured $750,000 in its first round of venture-capital financing. The firm, founded in 1979, plans to market artificial-intelligence software products.

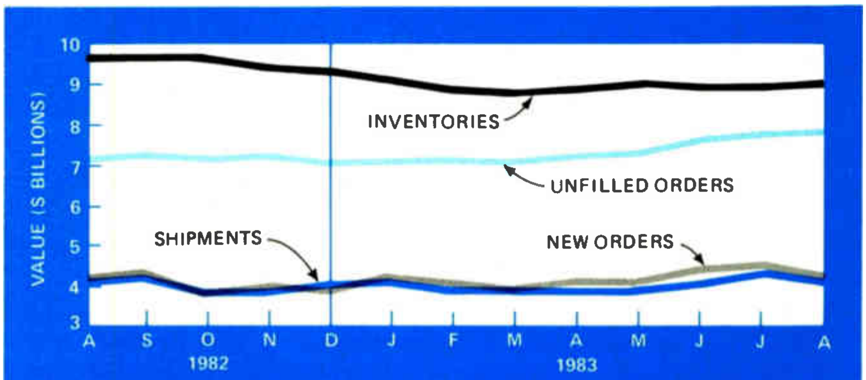
–Robert J. Kozma

Business activity

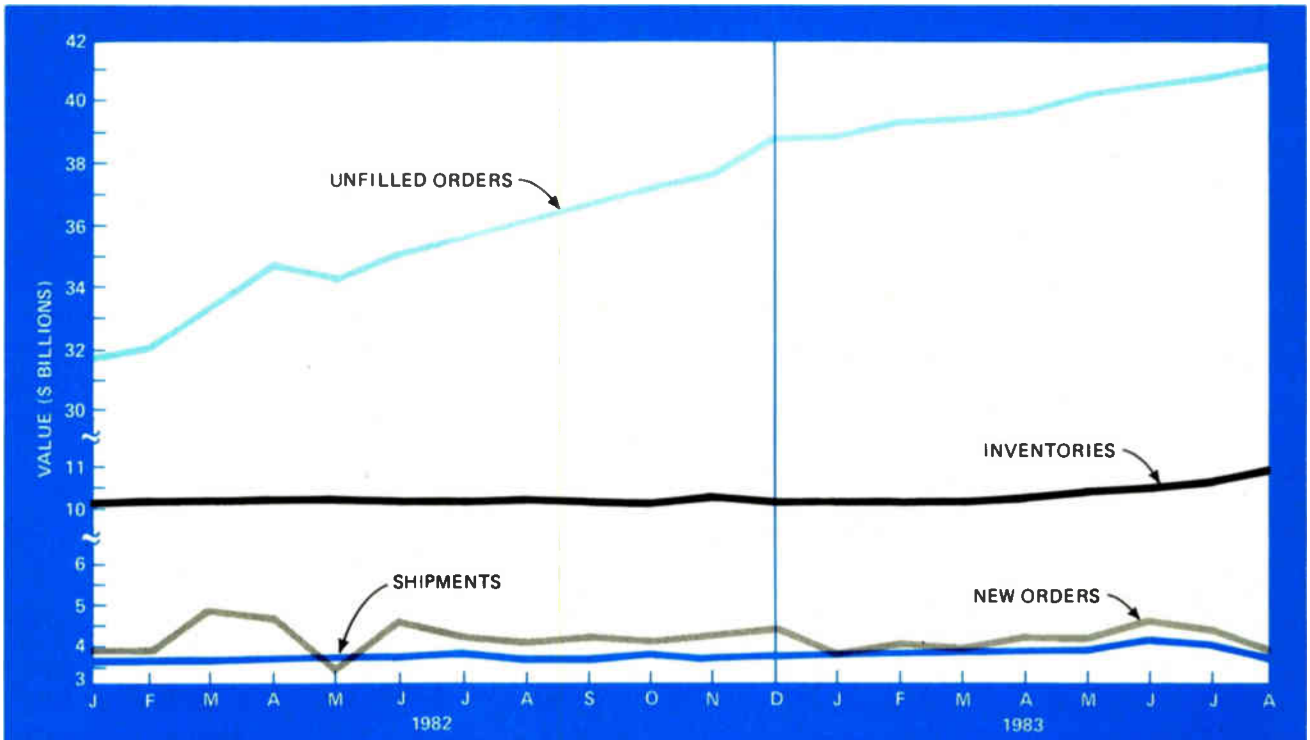
The accompanying charts illustrate the level of business activity in new orders, shipments, inventories, and unfilled orders of U. S. manufacturers of electronic components, communication equipment, and instrumentation from January or August 1982 to August 1983. The monthly indexes for U. S. production of electronic equipment and components, as well as the U. S. economic indicators for the electronics industries and for the economy as a whole, will next appear in the Dec. 1 issue.



ELECTRONIC COMPONENTS ACTIVITY



ELECTRONIC INSTRUMENTATION ACTIVITY



ELECTRONIC COMMUNICATION EQUIPMENT ACTIVITY

SOURCE: U.S. DEPARTMENT OF COMMERCE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Circle 39 for Literature

Circle 123 for Demonstration

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Circle 40 on reader service card

Electronics newsletter

Small EE-PROM chunks slated for Motorola microcomputers

A little electrically erasable programmable read-only memory goes a long way—or so hopes Motorola Inc. This month, Motorola's Microprocessor division, in Austin, Texas, announces a strategy to place small amounts of EE-PROM on its 8-bit MC6805 microcomputers. **Motorola believes that as little as (say) 15 bytes could suffice for a number of device-tailoring functions or as security "combination locks."** This EE-PROM could handle slight changes to on-chip software either to personalize systems for market niches or to update aging equipment in the field. First silicon is due in March 1984 for Motorola's MC6805K2: 128 bytes of EE-PROM will be coupled to 2-K bytes of mask ROM. Later in the year, Motorola will pack some EE-PROM with 3-K bytes of ultraviolet-light–erasable PROM in the MC68705K3, destined for system prototypes. Motorola says as much as 40% of the 8-bit microcomputer market will in the long term eventually use small chunks of EE-PROM.

Storage Technology to market German laser printer

Having dropped its own laser-printer development work late in 1982, Storage Technology Corp. has now elected to market in the U. S. a unit manufactured by Siemens AG, Munich, West Germany. Storage Technology's $195,000 model 6100 laser-printing subsystem—which its Documation Inc. subsidiary, in Palm Bay, Fla., is handling—will bow at this week's Data Processing Managers Association show, in Baltimore. Delivery starts in January. **The IBM-compatible 103-page/min printer uses a cold-fusing agent to fix print to paper.** This cuts cold start-up times to 12 minutes from up to 60 minutes for systems that use hot fusing, Storage Technology says. Meanwhile, NCR Corp., of Dayton, Ohio, has also signed with Siemens to market a similar system with its mainframe equipment.

DEC's personal computer get translater card for instrumentation systems

The Rainbow 100, Digital Equipment Corp.'s only personal computer to gain significant customer acceptance, will soon try to crack the growing market for data-acquisition and instrumentation systems built around personal computers. **The move is tied to a translater card that allows Rainbow to run a family of analog and digital input/output boards** sold by Data Translation Inc., Marlboro, Mass., the translater's developer. Currently, a translater is available only for the IBM Personal Computer [*Electronics,* March 24, p. 93]. The new translater card, slated for December delivery and selling for about $250, connects the Maynard., Mass., company's Rainbow by means of a cable to an external box housing any combination of Data Translation's seven boards.

Plug-in printer being shipped for pagers

Though radio pagers with built-in printers are said to be under development at several firms, Motorola Inc., a major pager maker, does not believe they are what the market wants. Instead, its Paging Products division, Fort Lauderdale, Fla., has begun shipping to selected customers a version of its alphanumeric-display Optrx pager that comes with a detachable thermal printer. The 15-oz, 6⅜-by-5½-by-2¼-in. printer is plugged into the pager's recharging unit only when the pager is left unattended—for example, at an office overnight. **The printer spits out a 2-in.-wide paper record of incoming messages of up to 80 characters each.** Motorola says it built the system at the request of an unnamed large pager customer who wanted printout capability but not a built-in unit's extra size and weight. Motorola is expected to offer the printer, made by IXO Inc., Culver City, Calif., as an Optrx peripheral possibly late in the first quarter of next year.

Compaq Computer unveils hard-disk lookalike of Personal Computer XT

Compaq Computer Corp., of Houston, a maker of lower-cost, software-compatible versions of the IBM Personal Computer, has unwrapped a version of International Business Machines Corp.'s hard-disk machine, the Personal Computer XT. At $4,995, the portable Compaq Plus will sell for about $750 less, says Compaq president Rod Canion. For its 10-megabyte Winchester store, it uses a 3½-in. disk made by Rodime plc, of Glenrothes, Scotland, rather than IBM's 5¼-in. unit. **The 16-bit machine also has a 5¼-in. 360-kilobyte floppy disk, 128-K bytes of random-access-memory, a 9-in. screen, MS-DOS 2.0 operating system, and Basic programming language.** Compaq also announced a $2,500 10-megabyte hard disk for current Compaq owners.

Synchronized cassette and floppy-disk train software users

Users of business application software who find the documentation unclear or downright puzzling can turn to a new simulation package that will train them to use it. Called Fastrain by its developer, Electronic Protection Devices, Waltham, Mass., the system **simulates the operation of any of several popular programs, including WordStar, Multiplan, and dBase II,** as well as the Microsoft Basic programming language. The $498 price buys an audio cassette that plays instructions, a floppy disk with software for one program, and an interface with the IBM, Kaypro, Osborne, Commodore, or Texas Instruments personal computer. Visual cues, including error corrections, are displayed on the computer's screen. A proprietary drive mechanism, as well as a nonstandard tape material, synchronizes the cassette to the floppy disk.

Du Pont to develop packaging technologies at Research Triangle Park

Some 200 scientists and engineers will staff a new semiconductor-packaging research and development facility that Du Pont Co. will open by early 1985. In Research Triangle Park, near Raleigh, N. C., **the 200-acre complex will be used to develop new ceramics and polymers for multilayer IC packages with 400 to 500 leads,** says Charles Arrington, its director designate. In coming years, the facility will include a manufacturing line for IC packages, a market that Arrington predicts will climb to $10 billion a year by 1990. Du Pont now sells more than $750 million a year worth of products to the electronics industries and expects this sum to double in the next five years.

Addenda

Bull Peripherals, a subsidiary of the French computer giant Compagnie des Machines Bull, will be doing advanced product development at the Sunnyvale, Calif., headquarters of its U. S. marketing arm, Cynthia Peripheral Corp. **Starting with half a dozen technical and marketing people,** the office will define drive and printer products for U. S. markets. . . . The National Computer Graphics Association, in Fairfax, Va., has endorsed the Graphical Kernel System (GKS), a proposed software standard for two-dimensional computer graphics. GKS has already been adopted by the International Standards Organization and is close to adoption by the American National Standards Institute.

MICRO POWER SYSTEMS

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The MP574 is a complete 12-bit successive approximation A/D with tri-state output buffers for direct interface to 8, 12, and 16-bit microprocessor buses. The MP574 is implemented with two advanced bipolar and CMOS LSI chips resulting in maximum performance at lowest cost. A proprietary decoded 12 bit DAC provides increased accuracy, lower drift and reduced noise over the converter's operating range. The device is offered in all temperature ranges, including MIL-STD-883. Other features include:

- Fast conversion (25μsec)
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MP7622, μP Compatible, 12-bit DAC

The MP7622 is the first 12-bit ultra stable (non-trimmed) monolithic double buffered multiplying DAC with a flexible interface to microprocessor buses. The MP7622 incorporates ultra stable thin film resistors and unique bit decoding techniques yielding non-trimmed 12-bit accuracy with excellent stability over temperature and time. Other features include:

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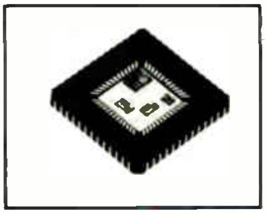
The MP8526 is a complete 13-bit bipolar (both +/- output voltages) DAC with ±5 and ±10 volts full scales. No external elements are required and LCC packaging with MIL-STD-883 is available. The MP8526 is implemented with an advanced decoded CMOS DAC and a bipolar linear chip. The precision, laser trimmed on the chip scaling and offset resistors provide very tight zero and full scales. Twelve, 14, and 16-bit versions are also available with unipolar or bipolar outputs and with any input coding and output full scales. Other features include:



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Circle 43 on reader service card

DATA GENERAL INTRODUCES THE DESKTOP GENERATION.

IBM moves to lock up office market as it puts 370 on the desk

by Marilyn A. Harris, New York bureau

PC link to system's power is made possible by placing whole instruction set on a single card and devising software hookup

Making a strong move to burnish its image among customers as the paternal presence that will lead confused office planners out of a computer wilderness, International Business Machines Corp. has proffered an armful of new products that could make its long-awaited introduction of a home computer seem like peanuts.

IBM, in effect, surrounded the office-automation market late last month when it introduced more than a half dozen systems, including an addition to the 3270 family, the PC 3270, that displays up to seven windows and costs $5,200, some $2,000 less than Apple's Lisa. Also, owners of 3279 color display terminals can now have PCs, too, with an attachment that costs $1,950. And programs that permit documents to be exchanged among several IBM office systems were also introduced.

But perhaps the star of the newcomers is the PC XT/370, a personal computer that in effect reduces a System/370 to desktop size.

The XT/370 is a PC that can transparently access and manipulate programs, services, and data previously available only to one of the 370-class computers running virtual-machine, conversational-monitor-system (VM/CMS) applications. The first of these mainframes, which now include the 4300 series of midrange systems and the 308X giants, was introduced a decade ago. VM/CMS, written for those machines, is often called IBM's best time-sharing operating system.

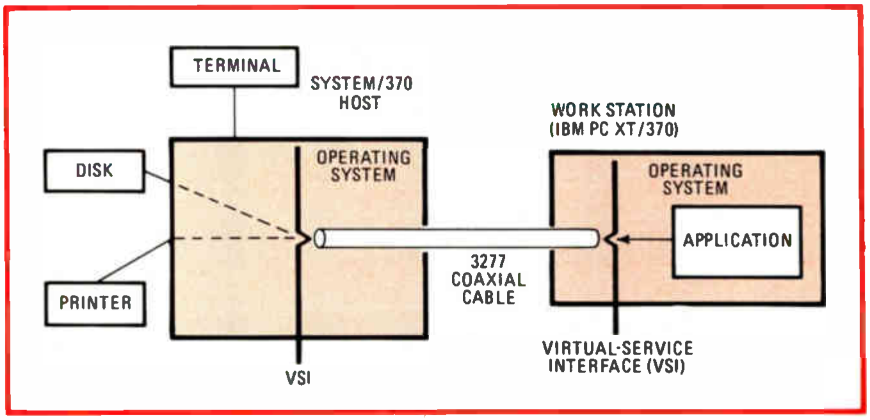
The impetus for the XT/370, according to Frank Moss, manager of communication and distributed systems at IBM's Thomas J. Watson Research Center, was twofold: IBM's Endicott, N. Y., laboratory was able to put the full instruction set for the System 370 onto a card; and a team under Moss in Yorktown Heights, N. Y., led by senior manager and researcher Barry Goldstein, forged a software link between the PC and the 370 at the operating-system level.

Traffic cop. Goldstein expanded the virtual-memory concept to create what he calls a "virtual-service" analog. That is, much as the operating system in a virtual-memory setup orchestrates a call to disk storage when the required data is not in main memory, the operating-system kernel he wrote for the PC's Intel 8088 processor decides whether a request, say, for access to a minifile or a printer can be serviced locally or needs the host. Acting as a filter for the personal computer's resident operating system, it directs the request (see figure).

Along with the 8088 and 256-K bytes of system memory that come with the standard PC XT, the XT/370 includes three new circuit cards. One includes the 370 instruction set and permits the machine to execute 370-compatible programs; it includes a Motorola MC68000 and two custom IBM microprocessors. The second card plugs in an extra 512-K bytes of memory to run VM/CMS applications.

The third card provides the connection for the 3277 coaxial cable that links the machine to the host through a 3274 display control unit. The XT/370 can also communicate with a host over a phone line through an RS-232-C port but in this mode acts only as a dumb terminal. Linked to a 3274 controller that is remotely connected to the host, however, it performs fully.

"We've taken a smart uniprocess-



Quiet filter. A key to IBM's new PC XT/370 is the way the virtual-service interface acts as a filter between the PC's operating system and that of a host System/370.

ing system—the PC—and made it multiprocessing and multitasking, transparent to the user. It meant unlocking the interfaces simply and directly and hooking them into the virtual-service concept," says Moss. In the final product, the resulting special-purpose operating system, the CP88, takes the form of a diskette application program, loaded initially in a simple 20-minute operation.

Once in the system, the virtual-service interface creeps into both the PC and the host and nudges the PC-DOS operating system aside, says Goldstein. "PC-DOS is interrupt-driven," he explains. The new operating system "steals the interrupt and inserts itself between the request and PC-DOS," assuming command of the PC and handling multitasking demands and also sending to the host requests for high-level services like laser printers.

Speed, power. "What you get [with the XT/370] is nowhere near as powerful as a full 370, which supports some 400 users," points out Moss. "But it approximates what each user sharing a 370 would get" in processing speed and power.

The experience has helped direct IBM's systems research, asserts Moss. "We know that an intelligent work station should include coprocessors, interconnect to a host, and give the user a friendly, functional interface—like the 3270's window feature."

The next step, he says, is to connect heterogenous systems without having to replicate the host in the small machine. "But it's going to take time till we know what the end user will ultimately want or need."

Computers

Transputer groomed for fifth generation

The first shot in the global war over the next generation of computer architectures is about to be fired by the Brits. Next month Inmos Ltd., of Bristol, UK, will unveil a product designed for parallel architectures: the transputer, which is a reduced-instruction mainframe on a chip.

Inmos is a latecomer to the microprocessor market. To leapfrog the dominant U. S. companies, it needs something different. And the transputer—the T424—is just that: a fifth-generation building block. Its name, a contraction of transistor computer, reflects the company's belief that it will become as ubiquitous as the transistor.

High levels. Inmos will describe the new unit, a very high-performance 32-bit microprocessor that executes no fewer than 10 million instructions a second, at Wescon (see p. 169). The transputer directly executes the company's Occam high-level language, developed to support concurrent processing [*Electronics,* Nov. 30, 1982, p. 89], and will support other high-level languages as compilers are developed.

> **Occam's razor action**
>
> Occam, aimed specifically at concurrent processing, works by splitting any computational task into self-contained sequential processes and enforcing strict discipline on data interchange among processes. The communications channel, for instance, must always be specified, and all communications among processes are synchronous. The transputer directly executes Occam's limited instruction set; there is no machine code. **–K. S.**

The transputer chip, 45 square millimeters, houses about 250,000 devices. Engineered in the company's complementary-MOS polycide process to 2-micrometer design rules, it consumes a mere 0.9 watt and ticks along at 5 megahertz.

A 10-MIPS central processing unit takes a lot of feeding, so Inmos has provided more than 4-K of static random-access memory on chip, with a bandwidth of 80 megabytes a second. Perhaps even more striking is the CPU's communications capability, both on and off the chip, mounted in an 84-pin leadless chip-carrier. This maximizes data-transfer rates and minimizes board area. A 32-bit multiplexed interface port can address 4 gigabytes of main memory and transfer data at 25 megabytes/s.

An 8-bit multiplexed port, with a block-transfer rate of 4 megabytes/s, can be used to access disk memory and other peripherals. Four dedicated ports handle communication with up to four other transputers—an important feature. Each of these ports has a full duplex data-transfer rate of 1.5 megabytes/s.

The company's choice of packaging and output configurations is the clue to the T424's target market. Used alone or in pairs, the transputer could pack the performance of a large mainframe into a desktop work station. Arrays of transputers used as system building blocks could provide orders-of-magnitude performance improvements over mainframes of the present generation.

Other products, now in the pipeline—a 16-bit version and transputers configured as high-performance graphics or disk controllers—will take Inmos into different markets. These are standard parts, but the company can play many other tunes on its transputer, including custom versions.

Similar parts. Inmos is not the first to disclose plans for 32-bit microprocessors: AT&T Western Electric and Hewlett-Packard have the Bellmac 32 and the MCS III, respectively, while Intel has the 432 and NCR, the NCR-200. Most other big-league chip and computer companies plan similar parts—DEC, for example, has just unveiled its MicroVAX I [*Electronics,* Oct. 20, p. 47]. Inmos is not even alone in optimizing its unit for a high-level language, like Occam: the Bellmac 32 is optimized for C, the 432 for object-oriented programming languages, like Ada.

Inmos believes that two things set the transputer apart: the very high communications bandwidth on and off the chip, with dedicated channels for hooking arrays of transputers together, and the direct execution of Occam. Only Western Digital—whose p machine executes p-code, the intermediate code for UCSD Pascal—is moving in this direction.

The input/output ports for communicating with other transputer-based units permit highly parallel processors to be built from arrays of transputers hooked together and thus provide the architectural underpinnings for Inmos's fifth-generation strategy. These programmable I/O ports are the hardware embodiment of Occam's Channel.

The transputer will also support all high-level languages. Compilers will gradually be made available for the important ones. Inmos says that first silicon is not scheduled until late 1984. —**Kevin Smith**

Medical

Microwaves scan images inside body

Two astrophysicists have developed a medical imaging technique that scans the interior of the human body in much the same way as high-frequency radio waves scan space to pinpoint heavenly bodies. Called Safescan, the technique could replace conventional X rays, computerized-axial-tomography (CAT) scanners, and the newly arrived nuclear-magnetic-resonance (NMR) system for three-dimensional imaging, its inventors believe.

Safescan generates 3-d images by collecting and processing microwaves reradiated from the body of a patient exposed to them at 10 milliwatts per square centimeter for 0.01 second inside a 6-foot-high chamber. "The radio-frequency exposure is totally safe and equal to only one tenth the leakage allowed from microwave ovens by the Food and Drug Administration," says Jeffrey B. Pearce, president and cofounder of Holographics Inc., in Boulder, Colo.

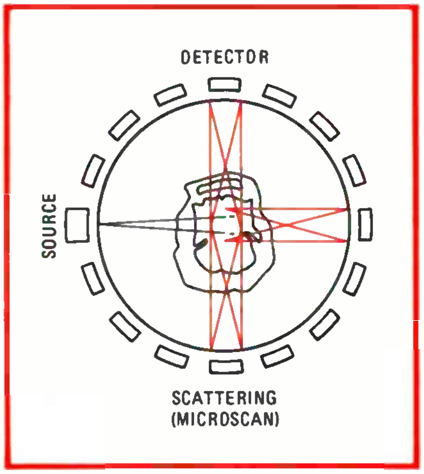
Pearce and his co-inventor, James W. Warwick, are radio astronomers who have experiments on board Voyagers I and II to detect radio emissions from the atmospheres of Jupiter, Saturn, Uranus, and Neptune. Casting about for ways to exploit their expertise in manipulating low-level radio signals, they decided to try them for noninvasive medical examinations.

Having completed the engineering research and much of the body-imaging software development with an engineering model, Holographics is now attempting to raise $1 million, so it can complete its first full-scale prototype within a year. Pearce hopes to raise an extra $3 million to finish five other prototypes, to be tested in hospital research centers.

Once on the market, the system will cost between $500,000 and $750,000, he estimates. At that price, the company believes, Safescan could quickly capture anywhere from 5% to 10% of the total medical-imaging business, which now runs to $4.1 billion a year worldwide.

Intended to yield a hologram of the body's entire interior in one exposure, the system beams radio waves between 700 megahertz and 1.3 gigahertz onto a human body, whose atoms absorb energy and reradiate the same frequency in all directions within picoseconds. Signals are collected by an array of 22,000 tiny dipole antennas, amplified, and digitized for processing by the computer, which deconvolves them in an operation akin to matrix inversion.

To create the hologram, the deconvolved signals are compared in phase and amplitude and then summed to obtain "voxels" (volume picture elements for 3-d images), a process that involves so much data and such an intricate program that a minicomputer working with a slave floating-point processor takes about 30 minutes to complete it.



Body and poles. Safescan system gives holographic view when body's atoms absorb radio waves and reradiate them to 22,000 antennas for collection and processing.

A gigabyte of memory is required to store a full body image so that it can be displayed on a screen with a resolution of 0.1 millimeter. Displayed in color or monochrome, images of any part of the body—such as the heart—can be called up from the memory for viewing on a stereo-optic video display employing two cathode-ray tubes. During this examination, doctors may rotate these 3-d images and from a series of exposures observe the body's organs actually functioning.

Nonionizing. Unlike conventional X rays (two-dimensional imaging) and CAT scanners (3-d imaging), Safescan carries no danger of exposure to the ionizing effects of electromagnetic waves, Pearce maintains. It uses nonionizing frequencies at a very low power level.

NMR—like Safescan—creates 3-d images of patients by reradiation of energy from nonionizing waves. But Pearce believes that NMR's high cost—about $1.5 million to $2 million for equipment alone—and the problem of shielding against the magnetics may take some of the luster off the technique, which is starting to gain popularity.

With Safescan, a copper screen can handle the shielding. Also, Pearce points out, the system operates in a radio frequency containing little natural or manmade interference and thus can run at lower power and "still get high signal-to-noise ratios." —**J. Robert Lineback**

Fiber optics

RCA diode keys lightwave local net

The widespread commercialization of fiber-optic local networks may be several years off, but wealthier customers—like the U. S. Government—are already preparing the roadbed for these high-capacity data highways. The keys to the rarefied nets are their laser-diode transmitters, and RCA Corp. has incorporated one of its star performers, now in production, into a prototype local network that is expected to go to market next year.

The network can deliver data to as many as 100 users at 200 to 500 megabits a second, over links as long as 1 kilometer. What drives the network is an 8-by-8-mil diode, 4 mils thick, that is specified to deliver 40 milliwatts into the net's multimode graded-index fiber.

Called CDH-LOC (for constricted double-heterojunction large optical cavity), it was put into production just two months ago, three years after it was first described. RCA's new new-products division, in Lancaster, Pa., is selling it for $1,500.

The diode's specs beat those of its competitors by a factor of two, crows Michael Ettenberg, the head of optoelectronics research at RCA's David Sarnoff Research Center, in Princeton, N. J. Within a year, an optimized version that more than triples peak output power (see "Laser diode picks up more power") will also be in production, Ettenberg adds.

Biased right. The prototype net that gets a boost from the CDH-LOC is fast and powerful, but so are other fiber-optic nets. What distinguishes RCA's net from the others is the way the laser is biased and stabilized. To avoid having repeatedly to bring the laser to the biased condition—over its lasing threshold—within the desired 2 to 5 nanoseconds, most systems leave it in the biased state. But the continuous background light often obscures actual signals.

To improve on this system, researcher David Patterson developed one that takes the control signal from the local node, biases the laser, transmits the data, and shuts the laser off. Yet the on-off setup affects the stabilization of the laser's operating point; moreover, normal aging takes its toll on its slope and bias point. So Patterson used off-the-shelf complementary-MOS logic chips to devise a compensatory refresh circuit located in the transmitter section at each node.

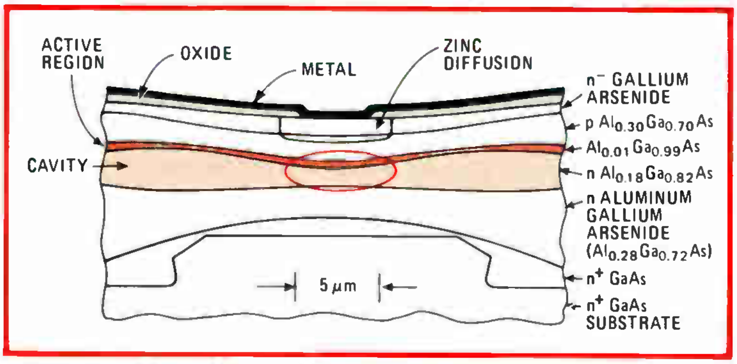
The circuit, activated by a button during routine maintenance, brings the transmitter off line for a few milliseconds and presents the diode with the desired absolute values for the threshold and peak points of light output. A ramping function sets the operating current to these points. The prototype net has run with four terminals, and an optical-disk recorder will be hooked in this quarter, Ettenberg says. Government customers will be getting a demonstration by year-end. –Marilyn A. Harris

Laser diode picks up more power

Even as the original constricted double-heterojunction large optical cavity laser diode moves off RCA's production line and into a prototype local network (see story), inventor Dan Botez and his colleagues at the David Sarnoff Research Center, Princeton, N. J., have more than tripled CDH-LOC's light output.

Like the earlier version, the new diode consists of five layers of gallium aluminum arsenide grown by liquid-phase epitaxy atop a GaAs substrate. Curving the active regions makes for a stable yet large light spot and thus a low lasing threshold and high power. The new diode manages to have even better current confinement than the earlier one because of a p-type zinc channel that has been diffused into the n-type cap (see figure). The channel brings the current closer to the light spot, explains Botez, so that less spills over into the nonlasing area.

Compared with the production version, the new diode's lasing threshold drops from 100 milliamperes to 50, and its electrical-to-optical efficiency is boosted from 10% to 35%. In experiments, the laser stays stable, at up to 100 mW, in a 50% duty cycle in a single spatial mode. –**M. A. H.**

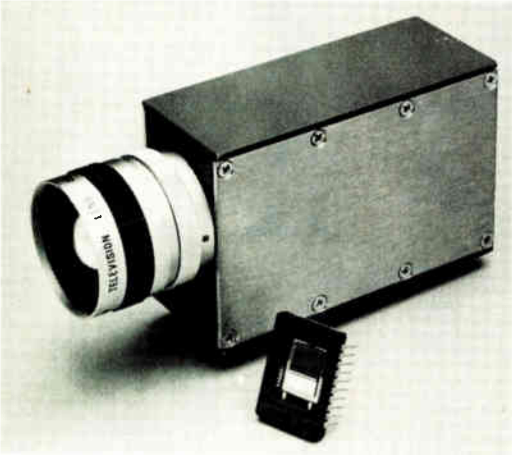


Charge-coupled devices

Electron-holes outdo antiblooming drains

Texas Instruments Inc. believes it has a solution to the blooming problem in charge-coupled devices with a new technique that draws positive "holes" up from the chip's substrate, traps them in a simple polysilicon gate, and then recombines them with unwanted electrons. The act of electron-hole recombination generates a photon, which is dissipated as background charge and heat through the crystal lattice.

In CCDs used as imagers for cameras, the blooming phenomenon—resulting from an overflow of signal charges from one brightly illuminated cell into neighboring cells—can distort pictures of very bright spots. To eliminate the electron overflow, many CCD sensors have drain structures beside each sensing element to siphon off extra charges. The drains, however, consume up to 30% of a



Nipped in the bud. TI saves space in its CCD image sensor by incorporating the antiblooming drain structures in the sensing area of its 250,000-mil^2 chip.

chip's active photomicrograph region, reducing image resolution.

TI incorporates these gate structures in a 200,000-square-mil CCD-array sensor, which is in turn the basis of a solid-state television camera built by the company's Central Research Laboratories, in Dallas. Consisting only of five small circuit boards, the camera was developed so that TI might better understand system demands on solid-state sensors, says Harold H. Hosack, director of the laboratories' CCD imagers and camera project.

No overlap. Unlike multiple-phase CCDs, the virtual-phase devices in the camera have no overlapping electrodes, which ensures higher production yields of large arrays with tightly packed sensors. Teaming the virtual-phase process with the space-saving antiblooming gates, the lab has produced a standard-size TV-camera sensor with twice as many charge-collecting elements per horizontal line as most other CCDs.

The n-channel MOS part contains an array of 488 by 780 picture elements, each measuring 11.5 by 27 micrometers. Half of the pixels (244 by 780) are a standard imaging area measuring 11 millimeters diagonally. The rest are coated with an opaque aluminum shield and function as an analog buffer memory between the imaging area and output registers.

A total of 244 antiblooming gates—formed from a 3-μm-by-8.8-mm strip of polysilicon—are placed only in the imaging area, explains Jaroslav Hynecek, senior staff member in the laboratories and inventor of the technique. The antiblooming gate's entire area is optically active.

Antiblooming drains and associated barriers beside each imaging cell can easily take up 6 μm, "of which half is optically dead," notes Hynecek, also inventor of virtual-phase technology [*Electronics,* Jan. 27, 1982, p. 39]. One alternative is to bury drains under the element, carrying off overflow charges vertically. Hynecek believes, though, that this option could result in signal loss in the longer-wavelength spectrum, mostly generated under the element.

Attracting positive holes from both p-type dopant substrate regions and channel stops along sides of CCD cells, the TI antiblooming gate operates with a clock that sequentially controls positive and negative potentials to the gate. A negative potential attracts positive-charged holes to the oxide-silicon interface.

The holes are then trapped there until a positive potential is applied to the gate, so that electrons from the active area move to the interface and recombine with the holes. The antiblooming thresholds can be set by the clock amplitude and the magnitude of the positive potential applied to the gate. **–J. Robert Lineback**

Software

Local-net package serves all masters

If the brass ring in local networking continues to go to system software that serves more than one kind of microcomputer—as it does today, despite expert predictions that this must change—then SofTech Inc.'s new Liaison package is surely a powerful entry in the game. Developed by the company's Microsystems subsidiary, in San Diego, Liaison is a software family of networking products that cut through the jumble of dissimilar hardware by adapting the company's widely used p-System (see "P as in portable," below).

The p-System's portable object code, which takes a form common to most microprocessors, is Liaison's underpinning, says C. A. (Al) Irvine, vice president for engineering. "The key is media independence," he says. "The normal p-System benefits are magnified by the ease with which information and software can be shipped around a local network." That feature has excited potential users who have seen a preview. "The response," says Irvine, "has been excellent," particularly since many kinds of existing computers can be mixed with new ones in a network.

SofTech's working premise in putting together the new package was that no one family of products, even

P as in portable

SofTech Inc.'s p-System, operating and application software written seven years ago specifically to bridge differences among microcomputers, has a head start as the basis for local networking. Its portability, or universality, stems from its p-code, the company's term for the object code common to all microcomputers. "P" stands for pseudomachine, a hypothetical, idealized computer that executes this machine-independent object code. For example, the p-System compiles, or translates, application programs written in Pascal, Fortran-77, or Basic into the code appropriate for the target machine. The trick is to provide an emulator, a program in the target computer's native code. When an application program runs, the emulator executes the p-code, and the target computer never knows. The firm boasts that the p-System runs not only the 10 top-selling microcomputers but almost 100 others, too. **–Larry Waller**

News briefs

Transaction processor nearly triples throughput

Swelling volumes of transactions processed by the biggest customers of Tandem Corp.'s NonStop System II strained even its highly elastic limits, so Tandem has introduced a transaction processor with throughputs two to almost three times higher. The 32-bit four-board NonStop TXP is modularly expandable and fault-tolerant, just like the NonStop II. It owes its higher throughputs to an architecture that accommodates 64-, 32-, and dual 16-bit operations yet is compatible with its 16-bit predecessor.

Honeywell gets the S1000, NEC gets markets

Users of Honeywell Inc.'s large, top-end DPS 88 computers will have an upward migration path to higher-level machines developed by Japan's NEC Corp. under an agreement the two firms have reached in principle. Instead of developing a higher-performance successor to the DPS 88, Minneapolis-based Honeywell will get distribution and manufacturing rights to NEC's more powerful S1000 system and large follow-on computing systems. The $4.3 million S1000 is now one of the highest-performance large general-purpose computing systems available, with a rating of about 15 million to 54 million instructions per second. NEC will gain access to new markets through Honeywell's distribution channels.

from powerhouse IBM Corp., can meet the disparate needs of the local-network marketplace. "That is very conspicuous to us, so we determined to create a means for sharing hardware resources among a community of users." The result is an open network in which all specifications will be made available, to encourage software and hardware vendors to develop products for it.

Services first. Right away—along with the first application packages, for shared access to disk and printer peripherals—Liaison will provide a set of operating-system services for networking. These services include development tools for users to write programs for locating the nodes in the network and for establishing connections. These tools, says SofTech, support point-to-point communications and verify that messages have been received. The fundamental level of networking is the sockets in each computer node. One Liaison development package lets programmers personalize communications links in minute detail.

Liaison will first be adapted to the Omninet network, and others will follow—to say nothing of many application packages scheduled for release early next year. P-System packages already exist for most personal computers; to hook them up to a specific network, only an input/output adaptation is needed. SofTech itself will be coming out with such products and encourages others to do the same. Prices for the family have not been set. –**Larry Waller**

Prolog compiler due for microcomputers

Growth of the logic-programming language Prolog has been stalled by a scarcity of affordable tools—especially a compiler, needed for writing microcomputer software. This lag could soon end if a start-up Los Angeles company, Silogic Inc., reaches its goal: putting out the first full-fledged Prolog compiler for microcomputers as a standard package by mid-1984.

Few software authorities doubt that interest in the Prolog programming language, invented in Europe in the early 1970s, is now building up to the blast-off point [*Electronics*, Oct. 6, p. 110]. Prolog's power and high-level nature let it manipulate symbolic data bases in a simple way that is ideal for such artificial-intelligence applications as expert systems (see p. 132). Japanese researchers have underscored Prolog's potential usefulness by picking it as the base language for their fifth-generation computer.

Silogic's compiler, now working in prototype, is running on a Motorola 68000-based microcomputer at a speed of about 17 klips. A measurement peculiar to Prolog, each klips, for thousand logical inferences per second, represents procedure calls equivalent to hundreds of the commoner operations per second. The only other compiler written in Prolog runs on the Digital Equipment Corp. 2060 at 43,000 klips and requires 256 kilowords of memory space. Silogic's compiler needs only 100 kilowords.

High hopes. The principals of Silogic, high in the penthouse of a skyscraper in the mid-Wilshire section of Los Angeles, are far from bashful: "We intend to be the dominant factor in Prolog," vows president Kamran Parsaye. The firm is on its way to having what he calls "already, the most complete family of Prolog software anywhere."

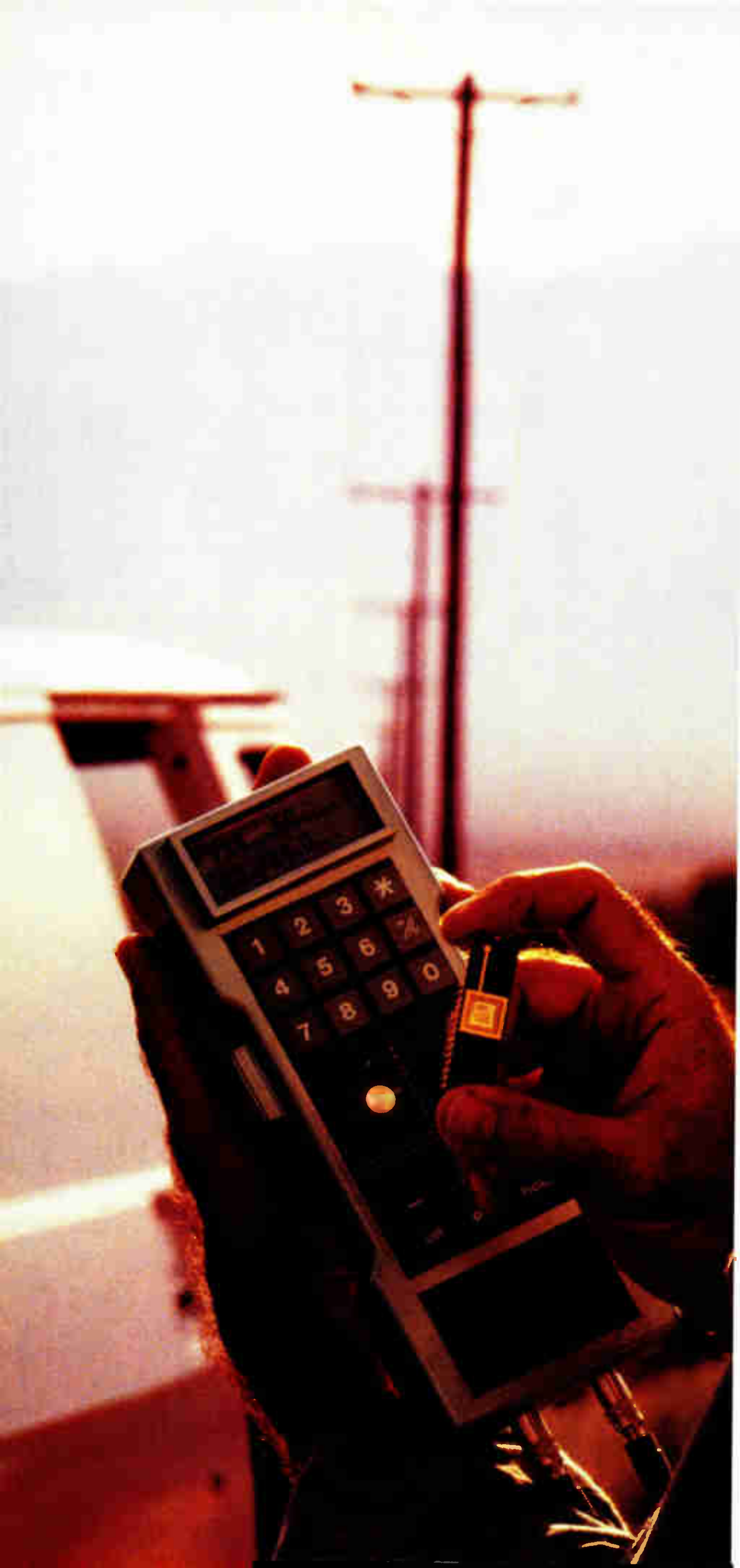
Silogic has also assembled a lineup of computer hardware and software experts closely identified with Prolog. David Warren, a co-developer of the DEC 2060 compiler in the mid-1970s and recently at Stanford Research Institute, is the most notable among them. It has not yet been decided whether or not he will devote full time to Silogic, but he is committed to specific compiler projects.

Also on board is D. Stott Parker, an authority on data bases and a faculty member at the University of California, Los Angeles. Parsaye, too, has taught at various universities in Southern California.

Silogic's compiler emphasizes portability, compactness, high-speed execution, and efficient memory use, the company claims. Its core consists of low-level support for Prolog's instruction set, which executes compiled procedures and provides memory and file management. Written largely in Prolog itself, the core can be tuned to particular target computers. Silogic believes that speeds of 50

Digital Signal Processing: Texas Instruments brings it down to earth by getting it off the ground.

- **Ultrahigh speed, precision, economy** of TI's new TMS320 Processor will spur widespread use of digital signal processing *(Page 2)*.
- **Easy implementation** of high-throughput, realtime applications, such as speech processing, is achieved with TMS320 *(Page 3)*.
- **Application design help** from TI includes a series of intensive seminars on digital signal processing *(Page 4)*. ▶



◀ **Low-cost digital signal processor,** TI's TMS320 is the inexpensive, single-chip alternative to multichip bit-slice systems and custom VLSI devices now used to process signals digitally. TMS320 speed and economy will open unlimited design opportunities for DSP such as the portable telecommunications circuit tester shown here conceptually.

economy. 200-ns cycle. TI's new processor makes DSP practical.

Digital Signal Processing: Coming of Age

Highlights from a discussion with Thomas W. Parks and G. Sidney Burris, Professors, Department of Electrical Engineering, Rice University.

Q. In your opinion, why has digital signal processing rather suddenly become practical and economical?
A. Well, digital signal processing has been possible for some years. We've had computers and bit-slice approaches that could do the job, but these were cumbersome, expensive, and consumed lots of power. One major factor accelerating the implementation of digital signal processing is the onward thrust of the electronic components industry.

The continued development of VLSI devices, by packing more and more circuitry on chip, has shrunk processor size dramatically. Throughput rates and architectures have also been improved enormously so that complex algorithms can be computed with incredible speed and reduced power consumption.

Of course, the development of these extremely efficient algorithms has contributed greatly to wider use.

Q. What do you consider the most outstanding advantages of DSP?
A. Digital signal processing provides the flexibility, precision, and speed required to execute increasingly sophisticated signal processing.

For example, spectrum analysis is frequently integral to signal processing, but for years there were no efficient, high-resolution methods to implement it. Now that VLSI digital signal processors can speed through the fast Fourier transform algorithm, such analyses are greatly simplified at a feasible cost.

Digital processing eliminates most voltage, temperature, drift, and noise problems associated with analog techniques. Digital filters can reliably meet tough specifications on magnitude and phase that would be difficult, or impossible, for analog filters to meet.

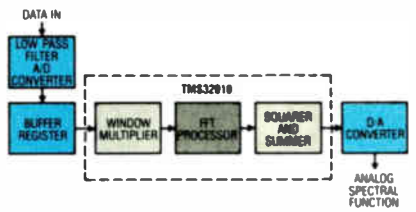
Q. What new applications do you see for DSP in the near future?
A. We are seeing digital technology applied to signal processing in image, seismic, and speech processing as well as in telecommunications, instrumentation, and high-speed control. In the near term—say, five to ten years—it is probable that we'll see digital signal processors becoming ubiquitous in the home, office, and factory. ■

TMS320 processors excel at realtime applications.

Because of their high-speed numeric capability, the new TMS320 processors can be used for realtime computations in many applications: Telecommunications. Instrumentation. Voice recognition and synthesis. Image processing. High-speed process control.

The TMS320 family can handle all the signal processing for spectrum analysis: Autocorrelation, windowing, and FFT—performing a 64-complex point FFT in only 580 µs!

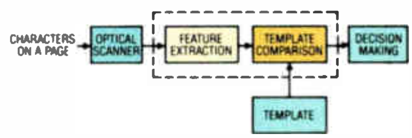
Image enhancement, pattern recognition, and data compression are



New TMS32010 simplifies spectrum analysis

all possible with TMS320 processors. They can extract features, then perform a template comparison to achieve optical character recognition.

The efficient TMS320 devices can also be used to build high-speed modems having rates up to 9600 baud.



New TMS32010 enhances image processing

With full-speed memory expansion capability, the TMS320 DSP family can be used in many other applications. ■

Full development support

In-depth support for the TMS320 consists of a host-independent development system, as well as software that can be run on a variety of host computers. An evaluation module, macro assembler/linker, simulator, and full in-circuit emulation are now available.

Choice of three

The TMS320M10 microcomputer is designed for applications where up to 3K bytes of program memory are mask-programmed into the read-only memory (ROM), expandable with up to eight kilobytes of total program memory (5K bytes off chip at full speed).

The TMS32010, a microprocessor without on-chip ROM, addresses up to 8K bytes of off-chip program memory at full speed.

A military version, SMJ32010JDL, is available processed to the requirements of MIL-STD-883B.

There's much more to learn about the TMS320 family. For our brochure, return the coupon on the following page. ■

See back page for more information.

Electronics review

klips and beyond can be reached.

The firm has Prolog interpreters for sale and reports so much interest that it is hard put to keep up. Now available are interpreters for DEC's minicomputers, for the 68000 with AT&T Bell Laboratories' Unix operating system, and for the Zilog Z80 with CP/M.

A tool in the final stages of development is an English-like language for simple interaction with Prolog data bases. EASE (for essential and simple English), a conversational system that answers questions and gives explanations, will be ready early next year. –Larry Waller

Packaging

National cuts cost of array to 2¢/pin

National Semiconductor Corp. has developed a way to build pin-grid arrays with a projected materials cost of 2¢ a pin, down from the current high of 9¢. Based on chip-on-board technology, the PGA is for multilayered ceramic boards. The method will be described in San Francisco at Wescon/83 (Nov. 8–11) by Matt Penry, section head for advanced packaging in Santa Clara, Calif.

The thermal resistance of the first low-cost PGA types will not be as good as the ceramic version's 35°C per watt. Instead, their figure will be an estimated 50°C/w, acceptable for a low-cost complementary-MOS gate array, which is to be the first product in the new package. A copper backplane can be added to the small pc board to decrease the package's thermal resistance to about 20°C/w. Adding a radiator and some air flow could lower this value to 5° to 10°C/w. Penry says that National expects to come up with a package as reliable as its present plastic DIPs.

To fabricate a low-cost PGA, National's engineers first etch, drill, and plate small printed-circuit boards with a chip's wiring pattern. In the next step, a chip is die- and wire-bonded to the board. Then the die and its wires are covered with a blob of epoxy of the same type as is used in molded dual in-line packages. Finally, pins are inserted and soldered into the board.

Penry adds that an alternative to National's approach could be a molded-plastic PGA, a method at least one connector company is trying and that is expected to yield an estimated cost of 0.3¢/pin if successful. But National, with seven years of experience with chip-on-board consumer modules, decided it was easier

Consumer

Games fan the demand for video-disk players

After years of disappointing sales in consumer and industrial markets, companies that supply laser-based optical video-disk players are suddenly having to cope with a big surge in demand.

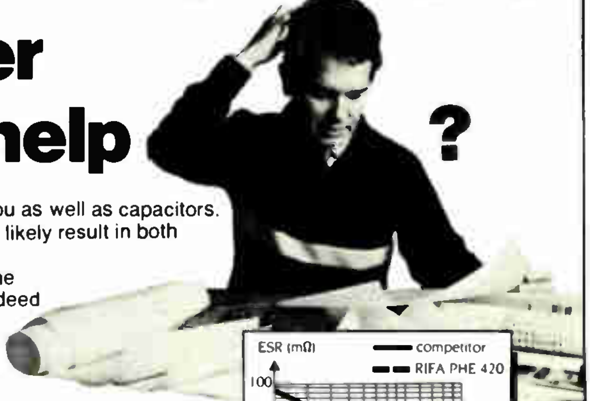
"We're overwhelmed with orders," declares Robert J. Moes, director of marketing for optical video-disk systems at North American Philips Corp., in New York. With order rates in recent months sometimes averaging 5,000 units a week, Moes says that Philips is scurrying to step up production capacity but expects back orders to persist "definitely out through the first quarter of next year." Much the same is happening at other manufacturers.

This sudden flood of orders comes not from consumers or the industrial training market but from the ailing coin-operated video-game industry. The overnight success of Dragon's Lair, the first interactive video-disk arcade game to hit the U. S. market, has game makers hoping it will stimulate sagging sales to game arcades.

The new disk-based games offer movie-like color animation, sometimes with computer-graphic overlays—novelties that game players cannot now get in home systems. Six to a dozen arcade-game makers were expected to show new video-disk–based coin-operated units at New Orleans' International Exposition of

Capacitor Casebook: SMPS

I'm having reliability problems in my SMPS circuits. Would cooler capacitors help?



Staying cool is usually a good idea, for you as well as capacitors. Better performance and longer life are the likely result in both cases.

Let's assume you've correctly identified the problem and that cooler capacitors would indeed upgrade reliability.

So how do you get cooler capacitors?

In theory, you simply choose those with the lowest ESR values.

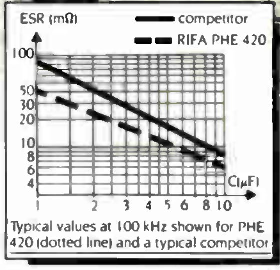
Low ESR means less dissipated power. Less dissipated power means lower operating temperatures. Lower operating temperatures mean higher reliability.

In practice, however, SMPS designers have learned that low ESR claims are not invariably all they seem to be. Claims to provide capacitors with the lowest ESR values are best evaluated in the light of the manufacturer's experience and reputation.

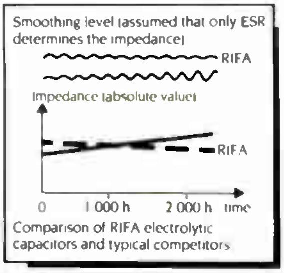
RIFA polypropylene pulse capacitors, for example, offer some of the lowest ESR values on the market. Advanced connection technology, up-to-date manufacturing methods and stringent quality control mean that when RIFA claims a low ESR value, you can be sure that's what you'll get. Any SMPS designers who've ever suffered from bad connections will know this doesn't go for all polypropylenes on the market.

And with electrolytic input and output capacitors, choosing the lowest initial ESR can prove to be a major error if stability is lacking.

So for cooler capacitors, by all means look for the lowest ESR values. But take a good look at the manufacturer's reputation at the same time.



Typical values at 100 kHz shown for PHE 420 (dotted line) and a typical competitor



Comparison of RIFA electrolytic capacitors and typical competitors

Is there really any benefit to SMPS designers in dealing with a full-range capacitor manufacturer?

As one of the world's few genuine full-range capacitor manufacturers, we'd be the first to admit we're biased.

However, we'll try to be objective as well as brief.

In SMPS circuits, the optimum solution often calls for several different types and values of capacitor.

Also in SMPS, perhaps more than in other circuits, designers tend to put large numbers of capacitors in parallel to achieve a certain level of performance.

In both cases, an impartial full-range capacitor manufacturer might be able to suggest a total solution based on a different mix of capacitors or dielectrics — one using fewer capacitors and producing a better overall performance.

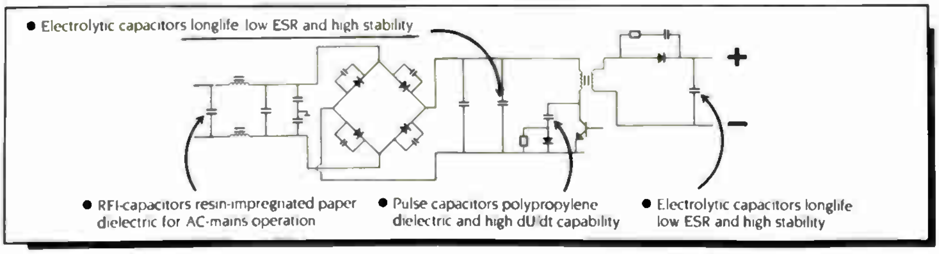
A limited-range manufacturer offers a solution to part of a circuit.

A full-range manufacturer can look for the total optimum solution.

Wescon/83

Electronic Show and Convention
November 8-11/San Francisco, California

If you want to discuss these or other capacitors, see us at Wescon '83, Booth 2407. We will be there with product specialists covering our entire range.



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CK1 (83312) A-E

Games and Music, Oct. 27–30.

As many as two dozen game makers have disk-based machines at some stage of development, and several are moving into production. But the collective rush to market has left manufacturers temporarily unable to meet demand.

At Cinematronics Inc.—the El Cajun, Calif., manufacturer of Dragon's Lair—marketing director Thomas Campbell says that the limited availability of disk players from supplier Pioneer Video Inc. has been delaying production. About 5,300 units of the game were shipped between June and the end of September, filling about half the company's orders.

Severe shortfall. At Chicago's Bally Manufacturing Corp., the largest arcade-game maker, a spokesman describes the disk-player shortage as "very severe." Bally's supplier, Hitachi Ltd., is providing only about a third of the laser-based industrial units Bally would like to have for production runs on Astron Belt, its first disk-based offering, first shipped in October. (Hitachi also manufactures a lower-priced capacitance-electronic-disk, or CED, player for the U. S. consumer market.)

Player manufacturers expect only a temporary crunch as the present market players adjust their production capacity and new suppliers appear. All the action to date has centered on laser-based players that provide the interactivity the arcade-game makers need. RCA Corp. is hoping to penetrate the game business with a new programmable random-access version of its CED player, which hit the market in August.

Even if the disk-based arcade games should prove to be only a short-lived fad, some video-disk suppliers agree that the business could spark the overall market. "A lot of the techniques they [the game makers] are developing can be applied to the consumer and institutional area," notes Robert P. Mueller, vice president of video communications for Sony Communications Products Co., in Park Ridge, N. J. "There's no question that there will be some fallout that could help stimulate sales in other areas." **–Wesley R. Iversen**

Meeting Japan's Challenge

Sixteenth in a Series

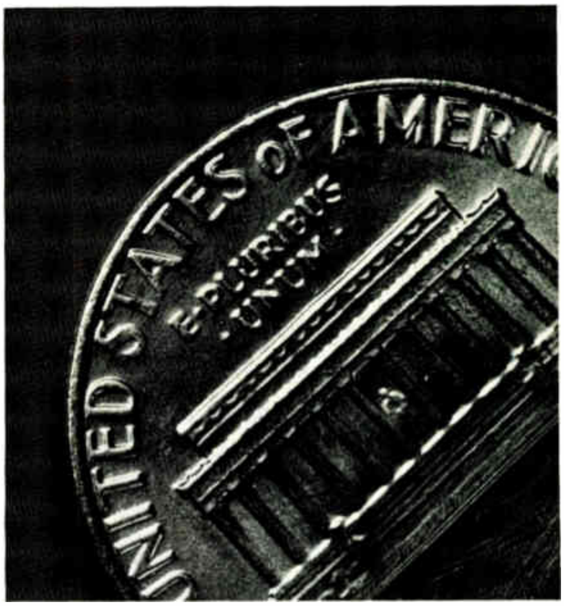
THE SECRET OF INCREASED PRODUCTIVITY IS ON EVERY PENNY YOUR COMPANY EARNS.

The second ad in this series was titled, "Could the Individual Hold the Key to an Entire Company's Productivity?"

In that installment, we described a portion of Motorola's Participative Management Program. This program (PMP I) is now operating successfully for 82% of our manufacturing workforce in the U.S. It has been dramatically successful.

But PMP I is only a part of Motorola's overall system of participative management. Another aspect, PMP II, is dedicated to the needs of our non-manufacturing activity.

While the operating rules for the two plans differ, the basic principles are the same. Teams are formed to set the goals, standards and procedures under which the members do their jobs. Regular meetings of the teams are held. Communication is opened, vertically and horizontally. Performance is rated by standards set by the participants themselves. Excellence is reflected by many forms of compensation, not the least of which is financial.



Targeted goals are charted, posted, and most of all, then surpassed.

PMP II became operational in our Semiconductor Products Sector facility in Phoenix, Arizona in 1980. Almost immediately, the program improved intramural communications, and promoted a consolidation of efforts. Today, more than 50% of our eligible non-manufacturing personnel in the U.S. are enrolled in the program. By 1984, that figure will be 100%.

Of course we know that however good any such program may be, it is not a panacea. We know it is not a substitute for good management fundamentals. It is not a pat formula to be applied mechanically with the expectation of achieving a totally cooperative and productive system over night.

But it is a system that gets the best from people, because it observes some basic truths about human beings. It recognizes that intelligence, perspective and creativity exist in the same proportion among people at all levels of the organization.

And it recognizes that an individual's behavior is primarily the consequence of the treatment that individual has received.

When the "Miracle of America" was taking shape, we lived, worked and governed ourselves by the slogan, "E Pluribus Unum," which declared our dedication to making one mighty entity from the contributions of many. To this day, the U.S. Mint puts that slogan on every penny.

Today, some business writers use the phrase, "The Miracle of Japan," in connection with that country. It is interesting to note that the Japanese make much of the slogan: "None of us is as smart as all of us."

The similarity is pertinent. And it just might make the road to future miracles miraculously clear.

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...An Essential Part Of Our Success Story In Telecommunications

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Working Together To Be The Best

Washington newsletter

Pentagon seeks to tighten controls on technical papers . . .

The Department of Defense is weighing export-control laws already on the books as a new means of restricting the distribution of unclassified papers and other data to the Soviet Union and its allies by contractors in industry and academia. The Pentagon's internal draft proposal was presented at the end of October to the department's Steering Committee on National Security and Technology Transfer. To restrict data flow, unclassified documents would be marked with one of six new categories of what are termed dissemination controls. Contractors could receive copies of documents under most of the controls, but public dissemination would be allowed under only one. **Contract officers would be authorized to halt progress payments to a violator or possibly even cancel a contract.** Exploratory and advanced development efforts—including those of the Department of Energy and the National Aeronautics and Space Administration—would be included in a new category of programs to be monitored under the acronym Metal, for militarily significant emerging technologies awareness list.

. . . and eyes restrictions on meeting attendance

Technical and scientific meetings sponsored by Government and industry organizations may find their attendance controlled by the Department of Defense if a new recommendation is approved. The internal Pentagon proposal to the Steering Committee on National Security and Technology Transfer would allow heads of the military branches and local commanders **to decide whether attendance controls should be invoked if unclassified information is discussed** at a meeting in their area. Two proposed guidelines for limiting attendance deal with presentations that could aid another country militarily and with meetings covering "topics relating to militarily critical technologies, weapons, weapons systems, communications security, signals intelligence, computer security, or electronic warfare."

Senate unit's witnesses clash on issue of Intelsat competition

With two U. S. firms seeking Federal Communications Commission approval to launch transatlantic satellites that would compete with the International Telecommunications Satellite Organization [*Electronics*, Aug. 25, p. 61], the Government and Intelsat appear at odds over the desirability of the competition. Testifying before a Senate Foreign Relations subcommittee on telecommunications policy, National Telecommunications and Information Administrator David Markey said that **the 1962 Satellite Act that set up Intelsat does not preclude the existence of additional satellite systems** as long as they are found to serve the national interest. Striking back was Richard Colino, director-general designate of Intelsat, who charged that competing systems would strip Intelsat of its ability to subsidize costs for poor countries, as well as violate U. S. treaty obligations and public policy. "Should the U. S. wish to export the concepts of competition and private-sector initiative, it can do it through dialogue and bilateral discussion with its Intelsat partners," he asserted. Markey says the Cabinet and perhaps Congress should consider the multifaceted issues raised by the two firms' requests. The Senate has already begun to move on the issue, with S.999, a bill now awaiting markup that would authorize the FCC to license privately run international satellite systems.

Washington newsletter

Satellite-sale plan headed for defeat

A Department of Commerce draft request for proposals on its proposed sale of the Government's remote-sensing and weather-satellite systems could come to naught if Congress has its way. The Administration wants to begin collecting bids in mid-December to complete the deal [*Electronics*, Dec. 29, 1982, p. 37] by the end of February. The Senate, however, has attached an amendment to Commerce's budget denying it the funds to proceed with the sale, which it says would result in a Government-subsidized private monopoly of weather data. **The resolution is designed to discourage the business community from bidding on the satellites** and is headed for a joint conference committee, where it is expected to be widely endorsed, reports a House source.

Supercomputer R&D too costly, says OMB

Despite strong White House support led by George A. Keyworth III, the President's science adviser, the Office of Management and Budget is winning the fight to hold down Federal funding of supercomputer research and development [*Electronics*, Sept. 8, p. 87]. **Funds will be limited to artificial intelligence and to related military R&D efforts.** OMB's opposition, says one agency official, is strictly financial, part of an effort to curb the Federal deficit in the fiscal 1985 budget, which goes to Congress in January. "Too many programs—especially in the military—and too many unexpected outlays for use of [the armed] forces have got us bleeding too much red ink," the source says, noting that projections of the fiscal 1984 deficit, first put at more than $200 billion, have now climbed to about $250 billion.

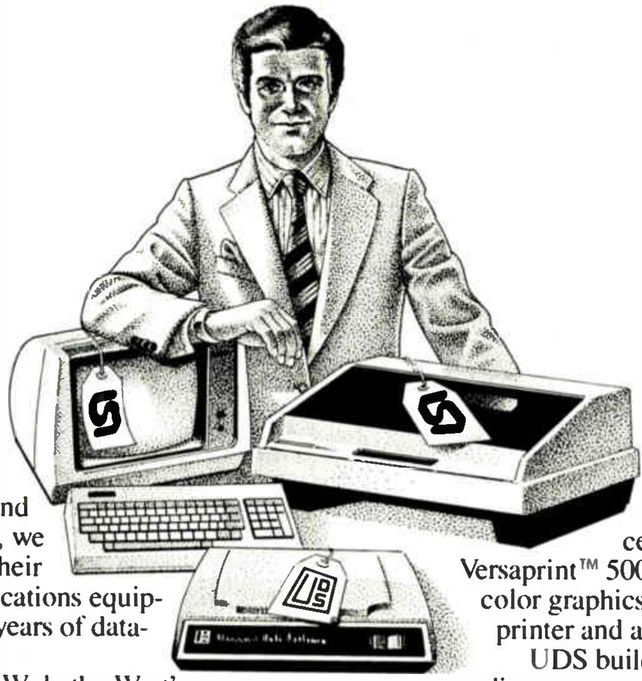
Competition sought for TI's HARM program

In the face of objections by the Pentagon and the Air Force, the House Appropriations Committee has voted for the naming of a second prime contractor for HARM, the High-speed Anti-Radiation Missile that Texas Instruments Inc. has developed for the Air Force and the Navy. In demanding a second contractor—instead of alternate sources for some of the missile's components and the development of a new seeker—**the committee is siding with the Navy.** If the ruling survives the appropriations conference with the Senate, some $142 million will be used to develop a second source.

Tamper-proof computer systems are possible, Congressmen are told

Available technology, such as hardware that intercepts and checks access attempts, is the best defense against computer break-ins—barring an upsurge in public outcry that would deter computer hacks. That advice came from executives of such organizations as AT&T Bell Labs, Honeywell Information Systems, and Wells-Fargo Bank testifying at a House subcommittee hearing on telecommunications security and privacy. **However, major users need a comprehensive how-to manual of preferred practices and procedures for operating tamper-proof computer systems, they say.** The problem is that every Government agency and corporation "is building its own policy structure and implementing details without coordinating efforts or sharing information," said William Ware, a computer security analyst with the Rand Corp., Santa Monica, Calif. He wants the General Services Administration to compile a guide to installing nontechnical computer safeguards.

THE NEWEST COMPANY IN DATA COMMUNICATIONS HAS OVER 15 YEARS EXPERIENCE.



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Expertise that makes Wyle the West's best source for complete datacomm solutions to your specific design requirements.

Because we don't just offer fast delivery on equipment, we give you the technical support you need to make it work. No other distributor has as many technically qualified applications engineers on staff. And no one else is catching up, either. We're determined that the West will continue to belong to Wyle.

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ELECTRONICS MARKETING GROUP

IBM shows prototype token-passing network at Telecom/83

Demonstrating a working version of what it terms a "laboratory prototype," International Business Machines Corp. gave the world yet another peek into its thinking on token-passing ring networks at last week's Telecom/83, the Fourth World Telecommunication Exhibition, in Geneva. The prototype local network—from the firm's lab in Zurich—operates over an IBM-developed cable, which integrates two twisted wire-pairs for 4-Mb/s transmissions with four standard telephone twisted pairs and an optional optical-fiber pair to handle future upgrades for long-distance transmission. **The system is currently capable of handling a maximum of 250 to 300 pieces of equipment in a ring configuration, with a typical distance between nodes of 800 to 900 meters.** IBM, which is jointly developing a chip set for token-passing networks with Texas Instruments Inc. of Dallas, still declines to reveal its product plans.

IBM and Hitachi come to terms in spying case . . .

Sixteen months after IBM Corp. accused Hitachi Ltd. of stealing trade secrets, the Japanese firm has agreed to let the U. S. company inspect its new IBM-compatible products three months before initial shipments to determine if the equipment was produced using any unauthorized technology or information. Announced in late October by Hitachi vice president Hiroshi Asano, **the out-of-court agreement allows IBM to review Hitachi's new mainframe and information-processing equipment** for the next five years. In addition, Hitachi will pay royalties if its system software is found similar to IBM's. Hitachi also will pay court costs in the lawsuit filed by IBM alleging that proprietary information was obtained illegally from its U. S. facilities [*Electronics*, July 14, 1982, p. 111] and has promised to drop its countersuit in Tokyo District Court [*Electronics*, July 14, 1983, p. 76]. With the matter settled, Hitachi will start selling its new mainframe, which is compatible with IBM's 3081-K.

. . . Fujitsu settles on software

Discounting rumors that a U. S. lawsuit from IBM was imminent, Fujitsu Ltd.—Japan's largest computer maker—says it has agreed to pay the American-based firm an undisclosed sum of money for the use of IBM's software copyrights. Fujitsu's executive managing director of computers, Shoichi Ninomiya, promises that the company will continue producing IBM-compatible systems, but admits the payment could be considered the cost for its carelessness in software development. **The Fujitsu and Hitachi pacts are part of IBM's lengthy effort to have its software and hardware rights recognized in Japan.** Meanwhile, Mitsubishi Electric says that it will market its own IBM-compatible software and has no plans to deal with the U. S. company.

Fiber-optic bus links instruments

Siemens AG figures it will be the first to have prototype hardware for a fiber-optic IEC 625 bus for mass data transmission between controllers and instruments in test and measurement systems. The Munich firm's new hardware, to be revealed later this month at the Interkama instrumentation and automation show, in Düsseldorf, West Germany, **can interconnect up to 32 instruments, using fiber-optic cables up to 200 meters long, for bit-serial transmission at data rates up to 100 kb/s.** In contrast, a conventional bit-parallel byte-serial IEC bus operating at the same data rate can handle only up to 15 instruments and allows only 2 meters of cable between them. The greater cable lengths of the new bus, as well as its immunity to electromagnetic noise and the galvanic separation inherent in fiber-optic connections, make it suitable for industrial use, Siemens observes.

Finger traces feed inputs into watch-calculator . . .

Casio Computer Co. has done away with the tiny push-button keyboards found on conventional watch-calculators by turning to a touch-sensitive glass "crystal" to feed in function commands and data. With a finger, users simply trace numerals and math symbols on the crystal, **which is overlaid with a transparent matrix of capacitance-sensitive electrodes that can differentiate 16 inputs**—10 numerals, decimal point, plus, minus, multiply, divide, and equal. The watch-calculators have an analog time display plus an eight-digit display for both time and calculations. They will go on sale in Japan in December, for between $88 and $108.

. . . and enter data in calculator-notepad

Sales will start in early November for a $55 Casio calculator that has **memory space for memos and phone numbers,** entered by being traced on a plastic-film keyboard of the kind found on very thin calculators. The film is a matrix of six by five conductive polymer contacts that serves as a conventional keyboard for arithmetic computations as well as for traced inputs. The unit can store 253 memos or phone numbers.

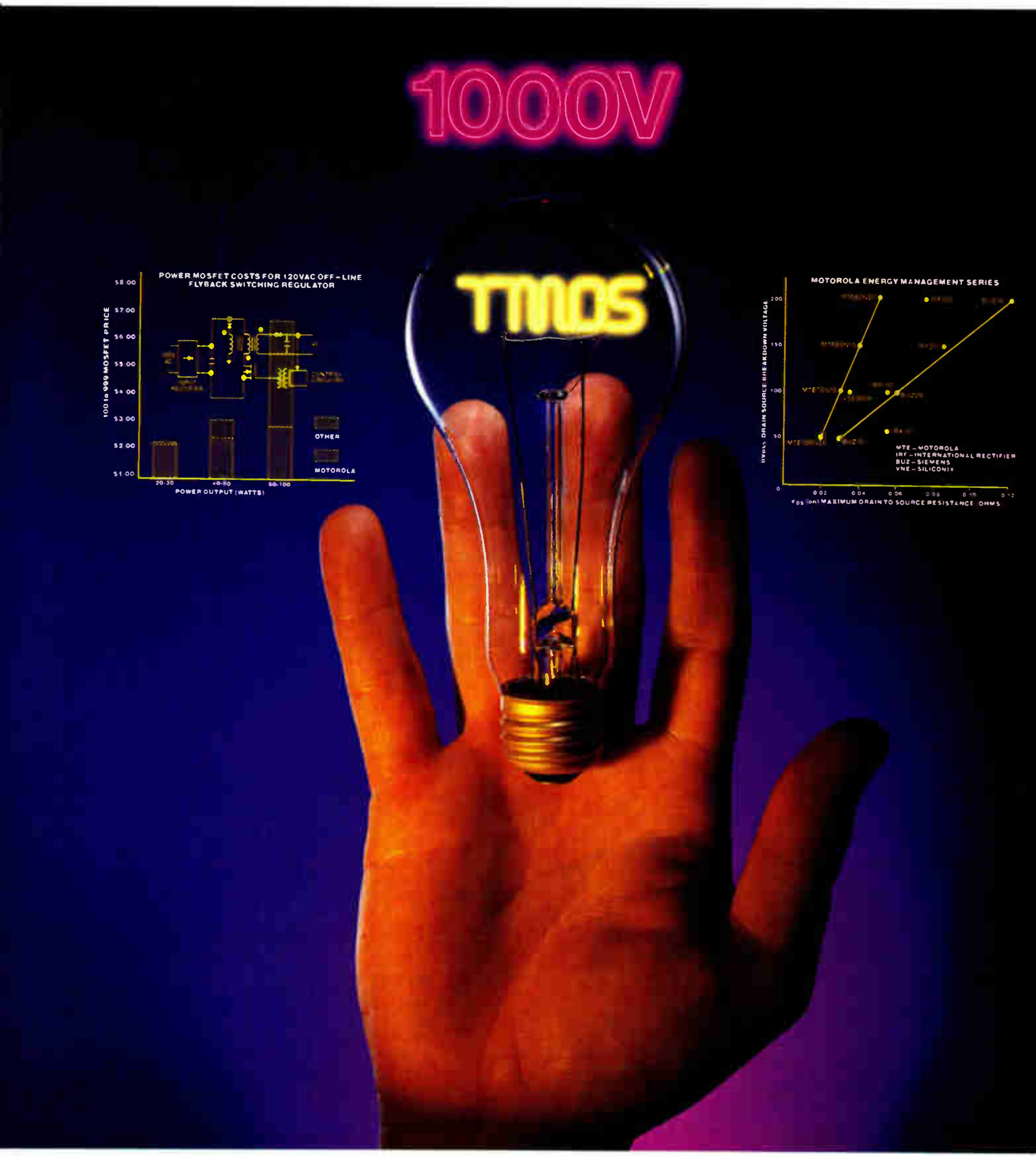
Phone directory will speak German

By the end of the 1980s, West Germany's postal and telecommunications authority, the Bundespost, plans to set up an automated directory-assistance network. In contrast to a French project that relies on a home data terminal to access and display telephone numbers, the German system will use standard phones—with rotary dials or push-button keyboards—to activate the computer-based system. **Synthetic speech conveyed through the receiver's earpiece will then send requested numbers to the caller.** Early next year, as an interim measure, the Bundespost will start using a system based on an IBM 4300/1 and with voice output to assist its directory operators.

8-inch floppy holds eight times the bits

Providing eight times the storage of a conventional 8-in. double-sided floppy-disk drive, a unit from Hitachi Ltd. relies on a new microcomputer-controlled head-positioning system that doubles the number of tracks per inch, a new disk material, and **data compression to offer an unformatted capacity of 9.6 megabytes.** The FDD-441's open-loop–controlled head assembly always approaches its final position from the same direction, virtually eliminating backlash. Therefore, overall head-positioning errors are cut to about half the levels of conventional drives, claims Hitachi. The medium—from Maxell Ltd., a Hitachi subsidiary—features a 1-μm-thick magnetic coating of gamma iron oxide particles with a 10-Å-thick epitaxial layer of cobalt ferrite. With modified frequency-modulation recording techniques, this coating provides a density in excess of 13,000 b/in. Two-to-seven coding compression techniques usually used for hard disks further boost the density to 20,560 b/in., about 1.5 times that of standard 8-in. disks. The unit is scheduled to enter volume production in January.

Half the cost. Half the loss. The switch is on to TMOS™



Twice the flexibility. power MOSFETs.

One power MOSFET family is emerging as design-in winner in the battle for fast, efficient, practical power switching. TMOS.

Not because of structural or topographical variations.

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Price. Performance. Production. Packaging. Quality. Delivery.

From any and all standpoints it has the advantage.

And, once again, Motorola grasps leadership in an MOS technology built on long-established expertise in bipolar.

Price. Down a steep slope.

Individual price leaders (often losers) aren't Motorola's game. Our philosophy of across-the-board price reductions reflects higher yields and product improvements as we accelerate down the learning curve. It's gone fast enough for us to recently announce price cuts up to and over 50%.

While power MOSFET prices aren't yet head-to-head with bipolar, lower voltage (up to 500 V) TMOS is rapidly overtaking them. Motorola's new prices are typical examples of rapidly narrowing parity between TMOS and bipolar: The MTP5N06 5 A/60 V, 0.5Ω TMOS unit has a new 100-up of $1.10.

Comparable bipolar is 69¢.

The MTM5N40 5 A/400 V 1.0Ω TMOS type is now 100-up priced at $3.50.

Bipolar costs nearly as much—$3.00.

Our MTP5N40 5 A/400 V plastic TMOS device has a new 100-up of $2.25.

Bipolar is $1.60.

And comparable *competitive* MOSFETs remain at 100-ups exceeding $8.00.

Motorola's 3.5 A/500 V, 4 A/400 V and 12 A/100 V, low $r_{DS(on)}$ TMOS units are all 250-999 priced at just $3.50. Our nearest competitor sells the identical units at $9.29, $8.30 and $7.60.

We'll furnish you any of these devices for under $2.25 in 25K quantities. And make your system cost-effective right now.

Half the switching loss.

Generally, anything with $r_{DS(on)}$ under 0.1Ω has been considered leading-edge efficient in holding down "on" losses. Taking advantage of the inherent power dissipation capabilities of its "Black Beauty" package, Motorola now offers the MTE- series of industrial-oriented, 250 W, TMOS power FETs with $r_{DS(on)}$ less than half that of others—18 millohms (0.018Ω) at 50 A.

These 100 A units—first of their kind in the industry—offer a simple, unique and inexpensive way to realize optimized high power from power MOSFET technology. The price of one Black Beauty package is actually less than two TO-3s, in parallel, and installation of one single-sided package is *at least* 50% less.

"On" losses can be lower, in many cases, than bipolar units.

Switching losses are minimized, too, for low-voltage automotive, traction motor, solar and wind power converter/inverter applications. And, of course, they're excellent candidates for very efficient, high-speed switching, regulators, controllers and synchronous rectification.

The MTE100N06 is actually usable to beyond 500 KHz.

Twice the voltage.

With high-voltage TMOS, you can raise high-frequency, series-resonant power supply operating efficiencies to higher-than-you-thought-possible levels.

These 500-volt-to-1-kv MTP-MTM2N/3N/6N units can be directly driven from control ICs—typically capable of 100 mA—to control power supplies up to 100 W. A bipolar design requires 10 times more drive.

This TMOS figure of merit sparkles even more brilliantly when you consider TMOS uses its turn-on source only about 10% of the time for input capacitance charging, not continuously like bipolar.

If you're using one of the new, fast control ICs such as the MC34060 or TL494 sourcing 250 mA or designing slower, less speed-critical circuits, buffer stages can usually be eliminated—an additional saving.

Switching losses are lower with less required heat sinking and drive circuits are simpler. Size and weight of componentry shrinks.

And new applications for 2-phase, 220 V international and 230 V domestic use can now be implemented.

Motorola has 18 high-voltage TMOS units ranging from 550 V to 1 KV in plastic TO-218, TO-220 and metal TO-204 (TO-3).

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Floating Point Systems array processor to break

The FPS-5000 Series from Floating Point Systems

Now, a new family of products from Floating Point Systems brings increased computing power and unmatched price/performance to the signal/image processing world.

With 3 to 6 times the speed and 4 times the memory capacity of previous FPS products, the FPS-5000 Series provides computing for applications that exceed their present system's capability.

The FPS-5000 Series offers fast, accurate, flexible computing for the most demanding real-time, user-interactive, and production-oriented applications.

Four basic product groups make up the new FPS-5000 Series: the 5100, 5200, 5300 and 5400. Peak performances range from 26 million floating-point operations per second (MFLOP), to 62 MFLOP. Data memory of 0.5M to 1M words is available along with program memory to 32K words.

By combining a distributed architecture concept with the latest VLSI technology, the FPS-5000 Series sets a new standard for cost-effective computing, breaking the $2,000 per MFLOP* barrier—the first time this has been achieved in any floating-point computing system.

*Based on U.S. Domestic Prices

Typical performance examples of geophysical, medical imaging and signal/image processing applications.

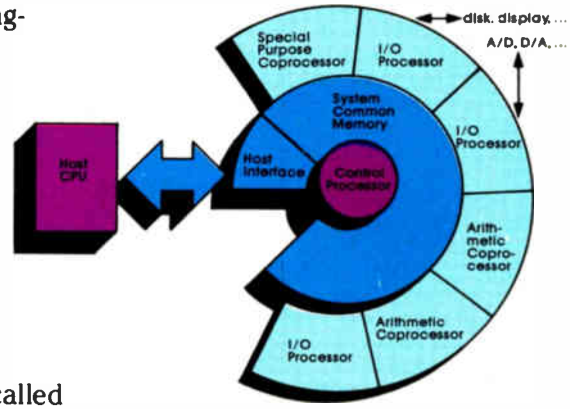
Application Example	AP-120B	FPS-5410	5420	5430
1. Demodulation/Signal Analysis	13.8 msec.	6.5 msec.	N/A	N/A
2. Tomography Preprocessing	60 sec.	25 sec.	16 sec.	12 sec.
3. Multispectral Image Classification (512 x 512 pixels 8 Bands, 4 classes)	49 sec.	25 sec.	13.3 sec.	10.5 sec.
4. 2D FFT (512 x 512 complex)	3.4 sec.	1.4 sec.	.7 sec.	.5 sec.
5. Matrix Multiply (100 x 100)	439 msec.	177 msec.	96 msec.	71 msec.

Based upon specifications subject to change.

Distributed processing architecture

The FPS-5000 Series is a distributed processing system that maximizes throughput by allocating the computational load to a set of high-performance, independent, floating-point processing elements called Arithmetic Coprocessors. Data flow is simultaneously managed

FPS-5000 Series Architecture



introduces the first the $2,000/MFLOP barrier.

by a combination of independent I/O Processors and the central Control Processor.

Each Arithmetic Coprocessor, with synchronous architecture to allow simple application debugging, functions as a self-contained unit.

The new Multiple Array Processor Execution Language (MAXL), based upon FORTRAN 77, allows the user to construct an integrated system environment which can be tuned to application requirements.

Increased performance can be achieved by adding Arithmetic Coprocessors as a field-installable upgrade as the user's requirements evolve.

Compatibility

The FPS-5000 Series maintains software compatibility with previous FPS 38-bit processors and is supported on a range of host computers. Thus, the extensive software support developed for FPS-100 and AP-120B products is maintained and users are able to move existing applications onto the FPS-5000 Series with minimal effort.

Quality and Reliability

The FPS-5000 Series was designed and built with the same quality standards inherent in all of the previous Floating Point Systems products—standards that have earned those products a reputation for unprecedented reliability and one of the best meantime between failure (MTBF) rates in the industry.

The Series is backed by the same outstanding worldwide support services that distinguish Floating Point Systems from other manufacturers.

For more information about how the FPS-5000 can be used in your specific application, call (800) 547-1445 or your local sales office.

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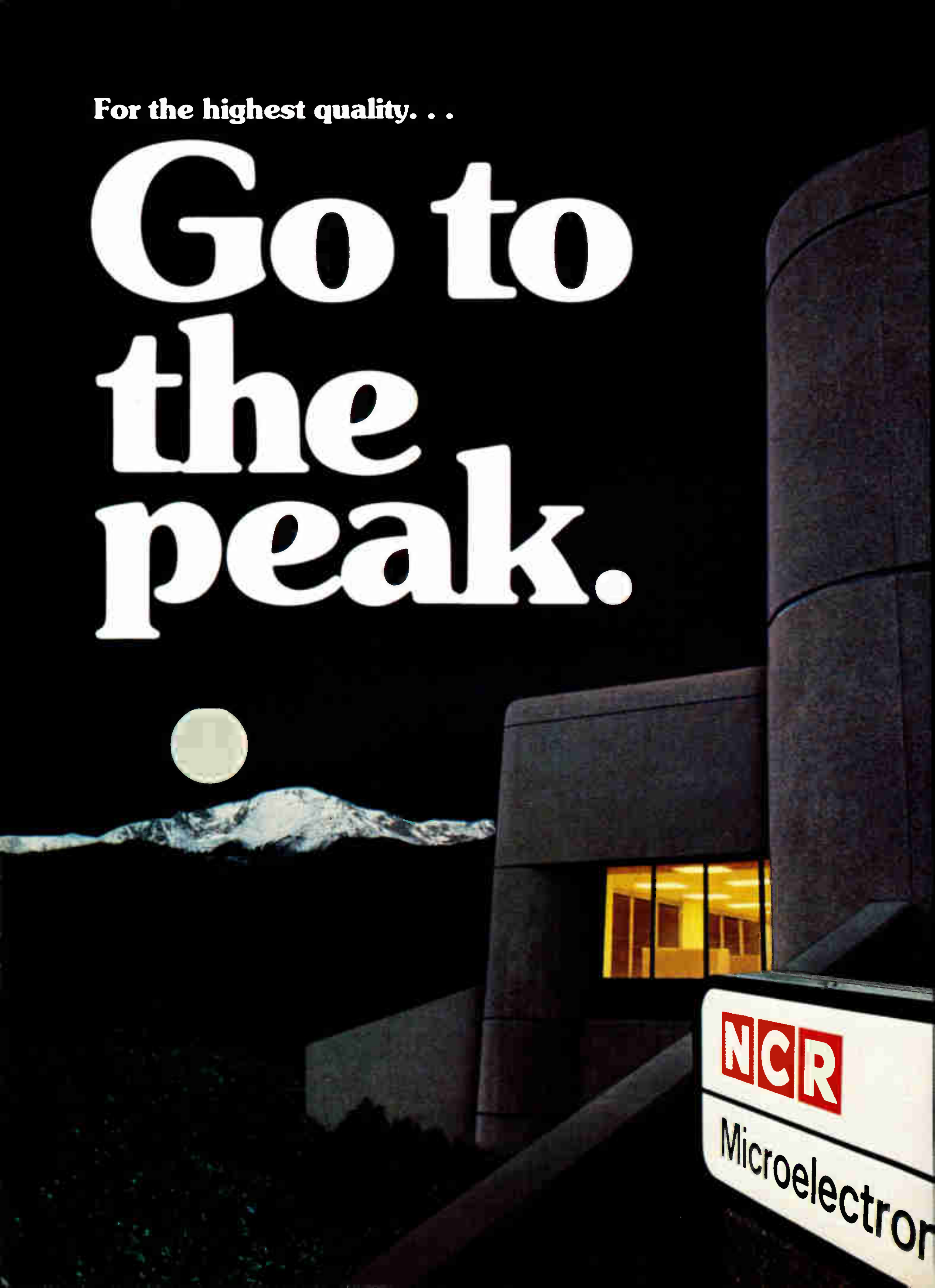
Circle 81 on reader service card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The chip on the extreme left will never leave an NCR Microelectronics plant. That telltale drop of ink indicates it failed one of the most comprehensive testing programs in the semiconductor industry, and it's destined for scrap.

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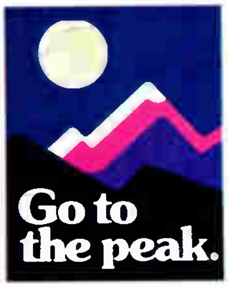

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In an industry where quality control is a science, we're just a bit fussier than the rest. Our toughest customer — NCR — has always demanded it, and we think our new customers deserve it. That means the 64K CMOS ROM you buy from us is just as flawless, just as reliable as one destined for a million-dollar mainframe with NCR's name right on the front.

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Circle 83 on reader service card

Vertical recording stores 10 megabytes on minifloppy disk

by Charles L. Cohen, Tokyo bureau manager

Two-layer sputtered thin-film medium and closed-flux-loop head provide bit densities as high as 70,000 bits/inch

Ten-megabyte Winchester data-storage hard disks, just now catching on, may turn out to be short-lived. Their future is threatened by perpendicularly recorded floppy disks that will be cheaper than Winchesters and more versatile as well, since the floppies can be easily changed and the Winchesters almost always cannot.

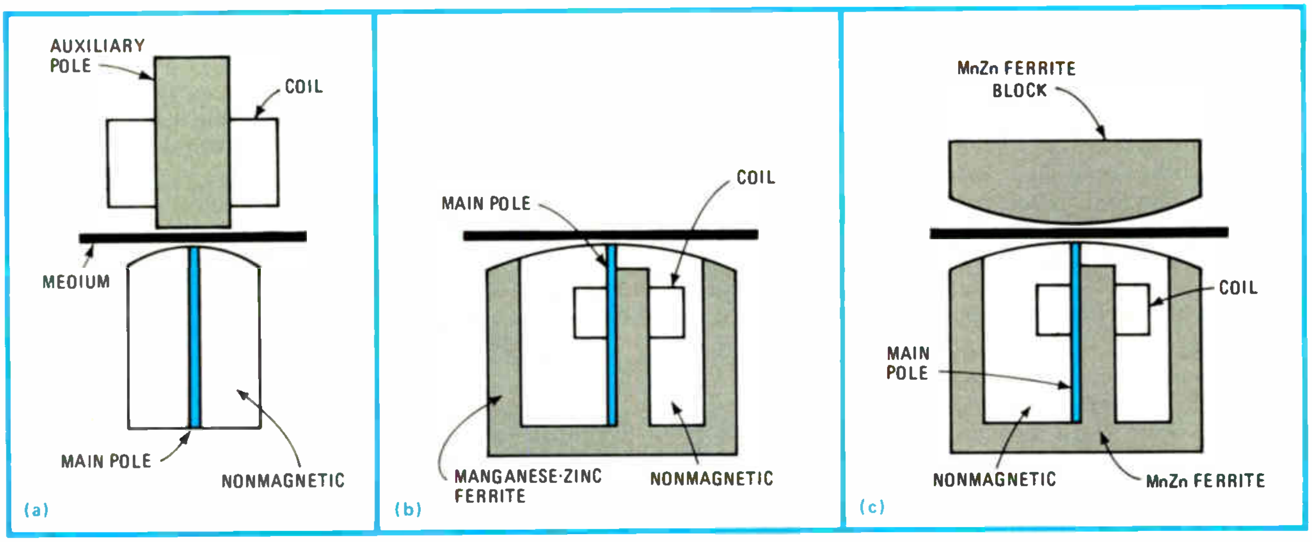
Prototypes of the high-capacity 5¼-inch floppies have been put together at the Matsushita Research Institutes Inc., on the outskirts of Tokyo, at Kawasaki. The disks have an unformatted capacity of 6 megabytes per side—enough for a formatted 5 megabytes per side. This figure matches the storage that Iomega Corp., Ogden, Utah, packs into its single-sided 8-in. state-of-the-art drive, which utilizes a flexible disk in a hard plastic cartridge [*Electronics*, April 21, 1982, p. 117]. As for access time, the prototype averages the usual 200 milliseconds of conventional minifloppies. Also, although all the necessary data is not yet in, Matsushita engineers are confident that the error rate will be a very respectable 1 bit in 10^{12}.

Flux loop. The drives, developed by a group headed by Yasuhiko Nakayama, have a new closed-magnetic-flux head (see figure). Apart from that, they closely resemble current minifloppy designs, using the now-standard 96-track-per-inch density.

The disks, though, are a far cry from the conventional oxide-coated media. Intended for perpendicular recording, they have a two-layer sputtered thin-film medium—iron-nickel 0.5 micrometer thick underlying a 0.2-μm layer of cobalt-chromium alloy, a film pioneered by Shun-Ichi Iwasaki, a professor at Tohoku University in Sendai.

Right price. Marketing strategists at the Research Institutes' parent company, Matsushita Electric Industrial Co., estimate that it will be mid-1985 before the Osaka-based firm can ready a product for the market. But they are convinced that the price will be right, since neither the disks nor the drives should cost much more to produce than their low-capacity predecessors.

Even though a production line with magnetron sputtering equipment will be necessary to produce the medium, the line most likely can be designed to apply thin-film layers on the web from which the disks are



Evolving head. Early head designed at Tohoku University for thin-film medium had an auxiliary pole to obtain an adequate signal despite the very thin main pole necessary for high bit density (a). Sony got better results by suppressing the auxiliary pole and surrounding the main pole with a W-shaped ferrite block (b). Matsushita has managed even higher density by closing the flux path with a second ferrite block, shielding the pole (c).

punched at a rate of about 1 meter per minute. Matsushita has, in fact, built an experimental line for continuous sputtering of magnetic layers on a plastic-base material. Thus, production costs will not force Matsushita to demand too large a premium for the new disks.

Nor should the drives for the new disks be unusually expensive. The magnetic thin films on these disks are stiffer than the magnetic coatings on conventional ones. But Nakayama says that his group compensates for this by reducing the thickness of the polyester substrate to 50 μm from the usual 75 μm so that the overall disk stiffness remains the same. With the mechanical characteristics of the media similar, special features would essentially determine the price differential for the new drives. Adding a second head so that the user would not have to flip the disk for access to the second side, for example, would boost the price.

The prototype Matsushita drive rotates the medium at the standard 300 revolutions per minute. Because of the high linear recording density, the data transfer rate is about 3 megabits a second, which is at the low end of the range common for miniature Winchesters.

Dense. The new head used with this disk can provide a recording density of 70 kilobits an inch. In contrast, conventional 5-in. hard disks, which are designed to match 8-in. floppy disks whose unformatted capacity is 0.8 megabyte per side, offer only 9.6 kb/in. The Matsushita figure also exceeds the 50 kb/in. of Toshiba's ring head and simplified magnetic thin-film medium [*Electronics,* Oct. 6, 1982, p. 68] and even tops the 65.5 kb/in. achieved by Sony Corp. with a similar medium and a W-shaped single-pole head.

All the same, Matsushita's new head reduces bit errors because of its high readout voltage—0.5 volt, about five times what Matsushita was able to achieve using Iwasaki's auxiliary-pole design. Noise caused by stray magnetic fields is about a quarter that of previous heads because the head design shields the fields around the main pole.

The Netherlands

Elcoma pushes IC surface mounting

Believing that by 1990 nearly half of all components sold will be housed in surface-mounted packages, NV Philips Gloeilampenfabrieken's Electronic Components and Materials division has launched a campaign on both the semiconductor and production-equipment fronts to encourage broader use of the space- and cost-saving technology in Europe. In that market, Elcoma believes, surface mounting of chips on printed-circuit boards generally lags behind activity in both the U. S. and Japan.

On one side of the division's thrust is the wide range of active and passive components in a number of standard chip-carriers and small-outline packages; these are being offered in Europe by such Philips subsidiaries as Mullard Ltd. in the UK. On the other side are Philips' production-equipment activities.

Hurdles. Hoping to remove what it sees as a production bottleneck slowing acceptance of surface mounting, the Dutch company is also making available automated board-assembly equipment, including a new low-end model, the MCM I, priced at $150,000 and capable of mounting 17,000 devices an hour. At the high end, Philips is marketing the high-speed MCM III, which sells for up to $2.25 million. In a typical configuration, the MCM III can mount 200,000 components in an hour.

Philips has already installed 22 such systems in the U. S. and Europe, including new surface-mounting equipment in General Motors Corp. plants. The Dutch company now hopes European managers of electronic production lines will take their cue from the No. 1 U. S. auto producer and step up their installation of the equipment, too.

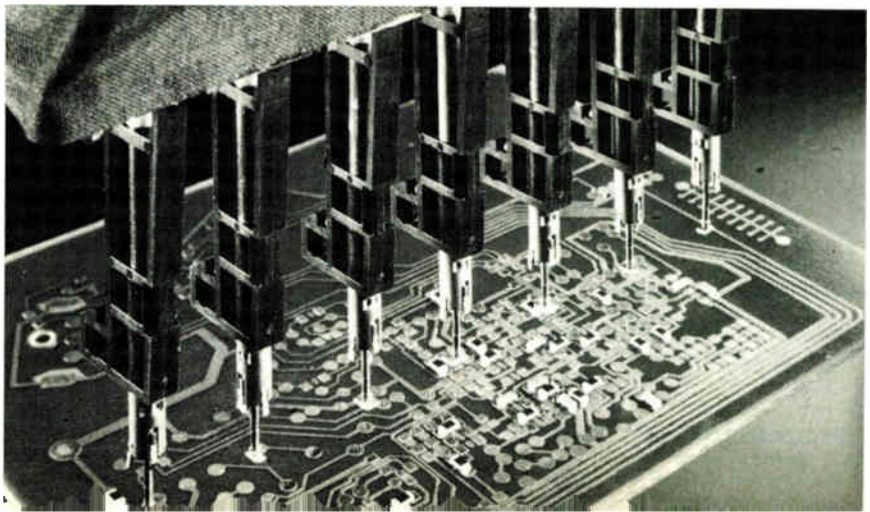
For more than a decade, Philips has pioneered work in the area, but the firm believes it has only been in the last two to three years that all conditions for widespread use have arrived. Duncan Edwards, marketing manager of consumer electronics for Mullard, says Japan's consumer electronics industry began to move in that direction in 1981, and Americans followed in 1982. Meanwhile, Europe, he believes, is "still suffering from jet lag."

From now on, the move on the international level will be ever faster, Edwards warns, adding that by the end of the decade between 40% and 50% of all components sold will be housed in surface-mounting packages. Philips estimates that some 100 billion surface-mounted chips will be sold worldwide by 1990.

Since these packages take up less space than conventional dual in-line packages, they will result in smaller and lighter systems, a critical consideration in both consumer and military markets. Philips estimates flush-mounted technology can halve assembly costs while increasing reliability tenfold.

The initial investment for using

Pick and place. Each pipette of the Philips automatic surface-mounting equipment squeezes the IC package to determine its position before pressing it to the board.



surface-mounting technology can be high, but greater levels of automation can offset that expense. For example, Philips—which first developed gear for its own consumer products operations—is currently offering three models of automated equipment. In addition to the MCM model III and model I—which bows in Munich this month at Productronica—Philips is also offering a model II, which has three software-controlled heads and can place 13,000 to 30,000 devices an hour.

On the larger system, bare pc boards move from a feed magazine to the placement machines. There, the components, in standard-sized blister-pack tapes, speed through the system, which quickly glues them down with an epoxy.

At the heart of the machine are the placement heads, which break each component out of its aluminized blister tape and place it precisely on the substrate. Each component is sandwiched between a lifting pin underneath it and a pipette that drops onto it from above. It is firmly grasped by jaws that squeeze all four sides of the package to ensure that its position is known. The surface-mounted component is then correctly oriented on the pc board, where a drop of glue fixes it ready for soldering.

The entire operation is monitored at each head by tiny microphones, embodied in the vacuum portion of "pick-and-place pipettes." The microphone detects the sound of air slipping through the vacuum chamber if a component is missing. The system is designed to have typically no more than one placement error in 10,000 passes, or 10 parts per million, well within most reliability targets. –Kevin Smith

Japan

On-screen office scene aids document retrieval

Pictures may be worth many words, but they may also save a lot of time when it comes to searching for documents filed away in optical-storage systems capable of holding gigabytes of data per disk. That, at least, is the novel approach being adopted by researchers at Toshiba Corp.

Their experimental, visually assisted man-machine interface package is being aimed at the typical business office environment, where workers often locate documents by remembering the color of a file folder or where it was last placed in a desk or storage cabinet drawer. Usually, digital document-retrieval systems require the entry of file names, which Toshiba believes many office workers will have difficulty remembering or in some cases even knowing.

So instead of using file names, engineers in the Electronics Equipment Laboratory in the Toshiba Research and Development Center, Kawasaki, have devised a graphics-interface system that builds on color images of desks and file cabinets.

Dual screens. To do this, the system uses two cathode-ray tubes: a color graphics display, with touch-sensing capabilities, that presents a graphical representation of office storage locations, and a monochrome CRT for document display. Special hardware converts high-bit-density images on optical disks into lower-density images with gray scale for display. The result seems to the user to be higher screen resolution and less flicker than would occur on equivalent bit-density monochrome screens with only two levels of color.

First, the color screen displays a view of the document-storage locations in an office. A user can then command the system to zoom in on a specific drawer in a desk or in a file cabinet. The drawer may be opened, and a group of color folders shown on the tube. For fine searches, the user may move a file on the display to the top of the desk in the scene and leaf through the pages. The desired document can then be displayed on the monochrome CRT for reading.

Researchers believe this approach is better than calling up files by slug names because its users can comprehend the filing structure at a glance. Also, most offices, they argue, have only a limited number of workers who name their own documents. In addition, active file names may be changed at any time. The system may also allow a search for files based on visual clues. For example, an office worker who cannot remember a person's name but knows his face may access a file by photos.

Toshiba believes this graphics-interface system will be most appropriate for office information that tends to change over a period of time, as

Graphics search. User presses touch-sensitive color CRT to access document from file cabinet displayed on screen. The document can be read on the adjacent monochrome screen.

opposed to data that seldom changes, such as reference material, statistics, journals, or drawings.

For document display, the system retrieves the document data, corresponding to an image with 200 picture elements per inch, from the 30-centimeter optical disk. (There are 1,728 pixels horizontally by 2,304 vertically on each standard A-4 page, for nearly 4 million of them.) However, that resolution is much greater than can be placed on today's affordable office CRTs.

So Toshiba uses a black and white monitor with a 512-by-512-by-4-bit format and signal processing to enhance the resolution based on the stored picture elements. Either full pages or portions of documents may be displayed on the 512-by-512-pixel CRT. When the portion of the document being displayed has more pixels than can be placed on the screen directly, groups of picture elements are processed to convert them into a single display pixel—a dot of black, white, or some level of gray.

The gray scale helps to reduce apparent flicker on the display by acting as a buffer between black and white areas on the monochrome screen. —Charles L. Cohen

France

Dashboard getting SAGEM computer

With a compact, inexpensive dashboard computer, a French company that specializes in telecommunications, aerospace, and military technology hopes to clear the path to a flourishing automotive-electronics market in Western Europe.

To date, the drive by European chip makers and auto-equipment houses to persuade car producers to use digital integrated circuits has not been a smooth one—the auto makers remain reluctant to do away with less expensive road-proven analog and mechanical systems. But Société d'Applications Générales d'Electricité et de Mécanique (SAGEM) hopes its new dashboard computer, based

Driving data. Dashboard computer steps through functions at the push of a button.

on a 4-bit microcomputer chip, will catch the eye and imagination of European automobile makers, who have not taken to computers as rapidly as have their Japanese and U. S. competitors.

Already Régie Renault, the long-nationalized French firm that now ranks as Europe's largest car producer, plans to make the dashboard computer standard equipment in some of its more expensive models next year. SAGEM hopes that others will follow. "Succeeding in the automotive electronics market is simple enough—you just have to offer military-level reliability at consumer prices," quips Georges Benoist, who heads the marketing of the car computer for SAGEM.

Hardy. To circumvent that dilemma, Paris-based SAGEM worked with Renault to ferret out a combination of largely standard hardware—assembled in a way that would withstand the rigors of the road—and its own software. Components on the computer's printed-circuit board are first glued in place and then wave-soldered. Benoist says tests indicate that because of this fabrication technique, SAGEM can count on reliability levels of one failure in a million kilometers (almost 700,000 miles).

Along with the *sine qua non* of reliability, SAGEM believes one of the most decisive factors in favor of the computer—which is no larger than a

standard dashboard clock—is that it offers more than most digital display replacements for analog indicators. Instead of just showing fuel levels or vehicle speed, the unit can process a number of variables based on real-time measurements—such as maximum distance before next fill-up. In addition, the system displays time, temperature, and fuel level.

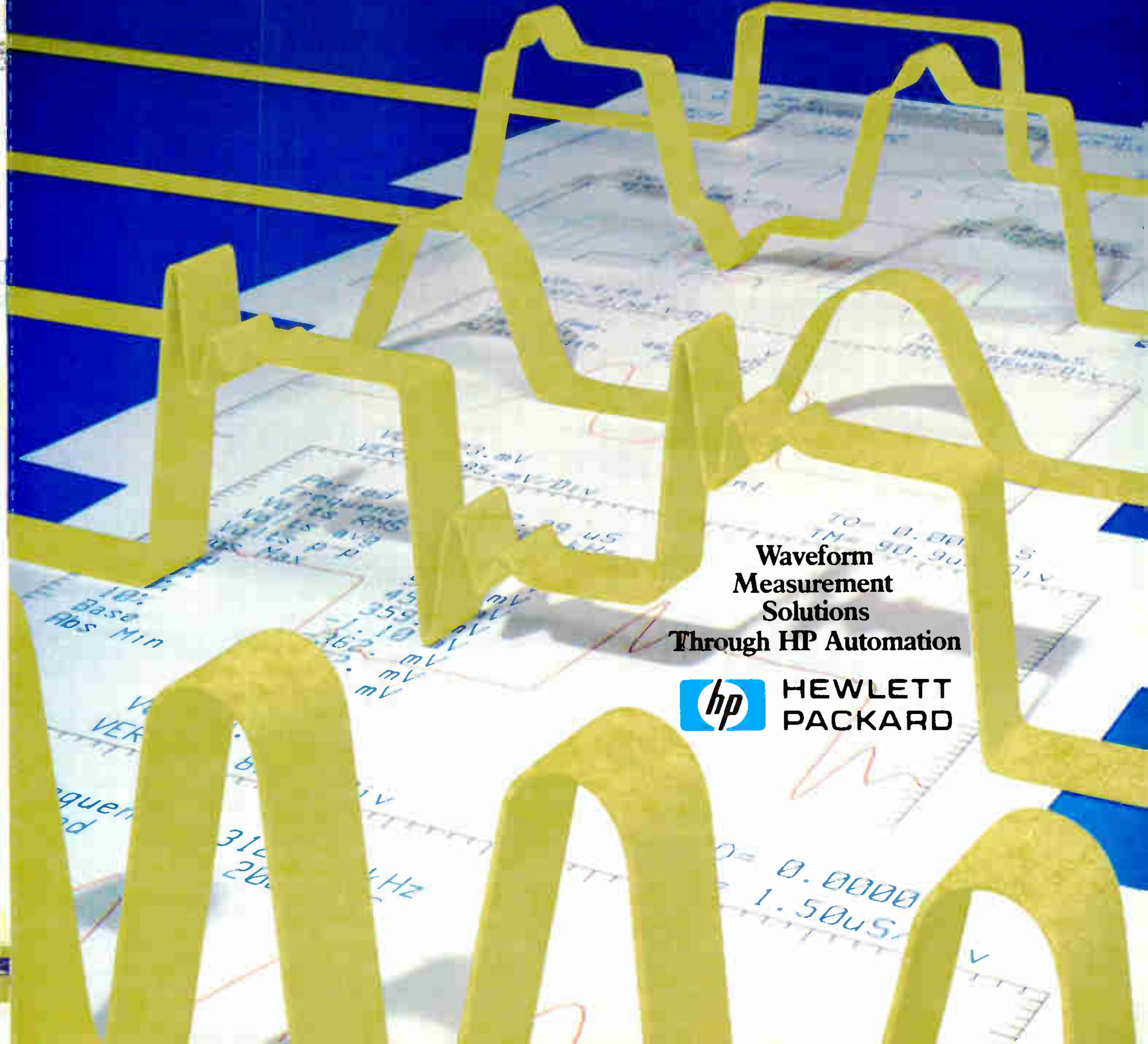
The system consists of a 4-bit processor, a liquid-crystal display, and sensors that pick up information on the exterior temperature, the amount of fuel, the rate gasoline is passing through the carburetor, and speed. At present, SAGEM is using microcomputer chips with mask read-only memory from NEC Corp. (the 7508) and Hitachi Ltd. (the HMCS47C), both of Japan, but the French company hopes to use still other chip-processor suppliers.

The company has also included considerable protection to shield the microcomputer from the vagaries of automotive power supplies. "That means voltages from 5 to 20 volts, gaps, parasitic conditions, and spikes up to 100 V—everything you can imagine that is bad" for computers, says Benoist.

Push button. With the system, a driver can select among readings on eight types of information: time, external temperature, amount of remaining fuel and the distance he can still cover with it, distance covered on the trip, average speed, average fuel consumption, and current fuel consumption. SAGEM indicates that other types of readings would be possible with additional sensors.

The data is accessed by pushing a single button, which steps the computer to a different output each time it is pushed. SAGEM's ergonomic research found that this single-button approach is easier for drivers than manipulating a number of buttons. At the push of a second button, the display returns to the clock mode, displaying the time.

Within the next couple of years, Benoist predicts, nearly all automobile models in the European market—from medium-priced up—will offer this type of dashboard computer system. —**Robert T. Gallagher**



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Reference waveforms can be generated by the HP Waveform Measurement Library software. They can be based on a known good waveform, or drawn from a set of specified data points, which allows any arbitrary shape to be defined as the limit waveform. Comparison measurements with the 1980 are orders of magnitude faster than manual testing. For example, parametric tolerance tests, such as comparing peak amplitude to preset limits, can be performed within several hundred milliseconds.

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HP's 1980 System waveform measurement library minimizes your software development time and costs.

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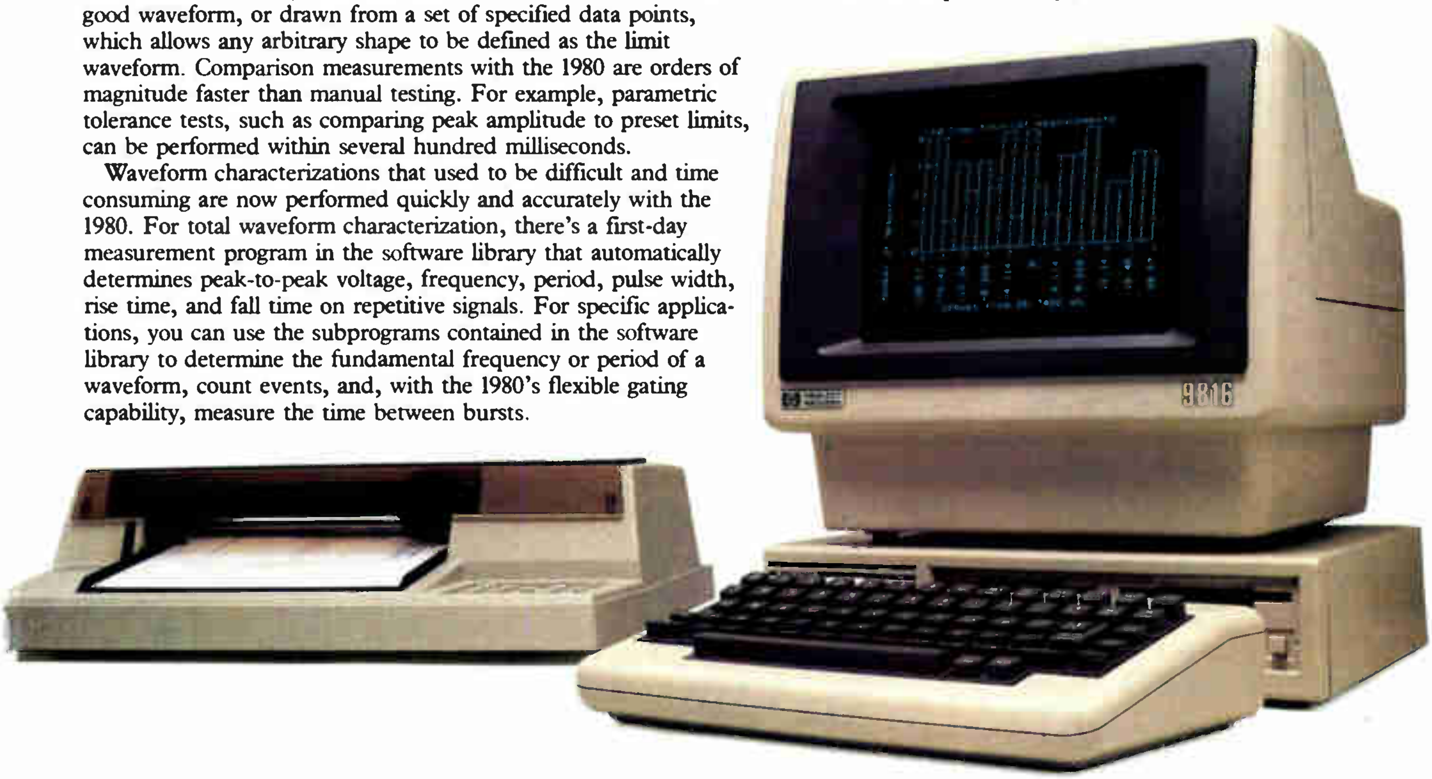

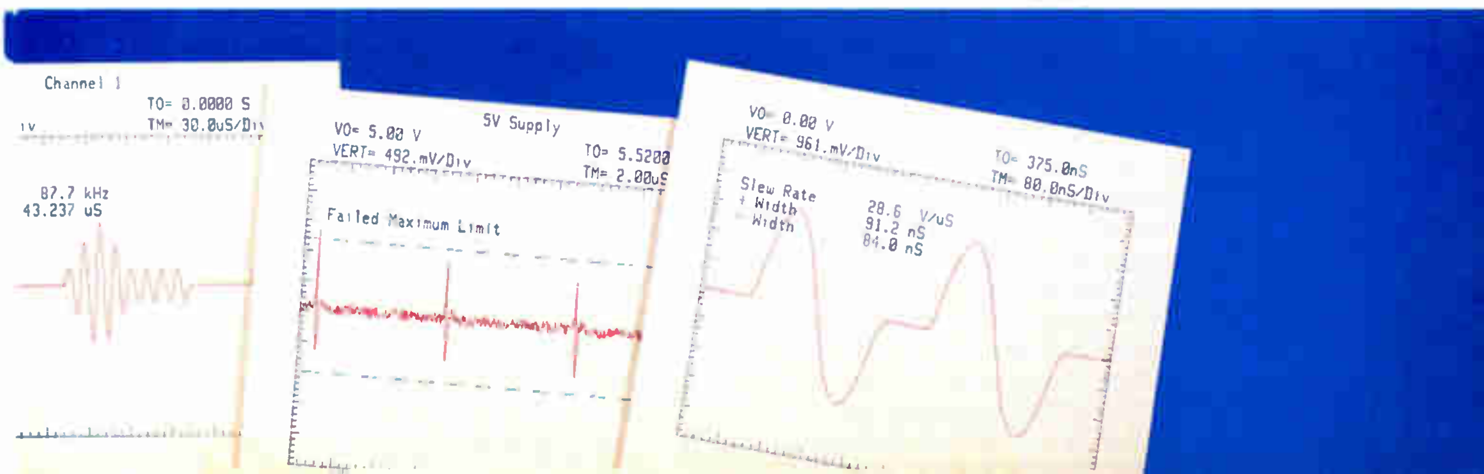

UK paces comeback in components

As the Paris components show opens, European semiconductors are selling well, spurred in the UK by home computers; West German sales are up, too

by Robert T. Gallagher, Paris bureau manager

As European components manufacturers make ready to exhibit their wares at the Salon des Composants in Paris, long-awaited signs of the market's recovery at last seem to be at hand. However, France's biggest professional electronics show has suffered from the worldwide recession. Officials report the number of exhibitors this year, at 1,212, will be down nearly 30% from the 1,705 who displayed their wares when the show was last held, in April 1982.

Though 31 countries—as many as last time—will again send exhibitors, those present may find themselves rattling around the exhibition area. This year, the show has been transferred from the exposition grounds at the Porte de Versailles to more spacious quarters at the Parc d'Expositions Paris-Nord in Villepinte, north of the city and near the Charles de Gaulle International Airport. Here, the show, an April-in-Paris fixture for years, will be taking place Nov. 14–18—and every other November from now on—alternating with the Electronica meeting in Munich, which is the West German equivalent of the French affair.

Looking up. If participants resent having to forgo their springtime in Paris, the first indications that the European components market may be about to follow the lead of its American counterpart and exhibit a sustained upturn should be enough to take the edge off the November chill. To be sure, the European market is as heterogenous as the Continent itself, and everyone has seen enough false alarms to keep any enthusiasm in check. But this time, with electronics markets in the UK showing the most strength, the good news seems to have a solider base.

"In January the book-to-bill ratio for European semiconductor suppliers turned positive for the first time in over a year, and now it's up to about 1.22," reckons Donald Beadle, vice president of European marketing for National Semiconductor Corp., at Fürstenfeldbruck, near Munich. Asserting that the figure for his own company is better than this average, he adds that the industry average indicates slower growth than the 1.55 book-to-bill ratio that is the current average in the U. S. market. "But there's a lot of inventory replenishing going on and a clear upturn in the marketplace," Beadle concludes.

The UK upswing is being termed exceptionally strong, making 1983 the second good year in a row. Solid growth is being found in West Germany and Scandinavia, and slower improvement in Italy and France.

For the UK, the semiconductor growth-rate estimates range from 17% (to quote Malcom G. Penn, director of the European Semiconductor Industry Service for Dataquest UK Ltd., London) at one end of the scale to 40% at the other (to cite Pat Brockett, marketing manager, Northern Europe, of National, in Bedford). So turned on is the semiconductor market, says Brockett, that "any company not growing at 30% is losing market share." That view may, however, reflect National's strong presence in standard Schottky logic, now enjoying a midlife boom.

Home computers. Heading the UK upturn in 1983 is a booming home-computer market led by Sinclair Research Ltd. and Acorn Computers Ltd. In the professional personal computer sector, IBM Corp.'s Greenock plant is cranking out Personal

Probing the news

Computers just as fast as supplies will allow. For as long as Big Blue fails to keep pace with demand, there is also room for a rash of UK start-up manufacturers.

ACT Computers Ltd., in Birmingham, for one, claims it holds the No. 1 spot in the UK for 16-bit machines with the Victor Sirius computer, which it distributes. It has also begun to manufacture a portable machine of its own, the Apricot.

TV sets. Meanwhile, TV manufacturers, buoyed by a peaking replacement cycle, will crank out a record 4 million television sets of all types this year, while the telecommunications sector is using 25% more semiconductors than last year. Telecommunications promises even faster growth as the government monopoly in the field is purposely loosened. The industrial sector, still in recession, is also due for an upturn, while the defense market is "a bit of a sleeper," according to one observer.

Question marks do persist, despite the growth. For example, the home-computer sector could catch cold if the U. S. market slows. Should the Americans then try to sell in the UK, this could raise problems for financially weaker companies.

But, says an executive at a major semiconductor manufacturer, "We look on that business as froth and don't count on it." More outspoken is Dataquest's Penn: "There is gross overcapacity potential in this sector. They [personal-computer suppliers] are all planning to sell their machines to the same customers."

Worries. More worrying is the likelihood of shortages and hefty price hikes. In the last year or two, Europe has benefited from relatively lower prices than the U. S., as Japanese and American semiconductor manufacturers slug it out on neutral territory. Prices in some cases are as much as 20% lower in Europe, points out Penn. With European currencies slipping against the dollar, higher prices may emerge soon, as semiconductor suppliers renegotiate contracts with top customers.

Taken by category, the fastest-growing market in Europe is the gate-array business, expanding at between 70% and 80% annually. The big surprise, though, has been the big demand for Schottky logic, both of the low-power and high-speed varieties. The buoyancy of this sector is probably the best pointer yet to a recovery in the more traditional minicomputer and mainframe market. Low-power complementary-MOS is still lagging, an equally telling pointer to the low state of the industrial sector (see related story, p. 106).

Input. The crowds at the Salon des Composants in Paris in April 1982 may not be matched this year as slower economies, fewer exhibitors, and a bigger exhibit hall leave their marks.

West German semiconductor makers are also pleased. "Since late spring, the semiconductor market has been characterized by orders far exceeding shipments," says Gernot Oswald, sales director for semiconductors at West Germany's Siemens AG, Europe's second-largest native chip producer after Philips.

He describes the upswing as continuous, with no seasonal variations. Market strength is far more pronounced in integrated circuits than in discretes. "Overall, 1983 may finish up 10% better than 1982."

Foot dragging. Elsewhere, "the French market is dragging its feet a bit," reports Jacques Bouyer, president of RTC–La Radiotechnique Compelec, Paris, the principal French subsidiary of the Philips group and a specialist in high-speed emitter-coupled-logic ICs and discrete components. Bouyer nonetheless expects the French components market to grow by about 12% this year. The figure looks far more modest in real terms, since the national inflation rate will almost certainly top the official government projections of 8% by a point or two. He is cautiously optimistic about the prospects for next year, for which the French Socialist government has set an inflation target of only 5%.

A somewhat sunnier perspective comes from Italy. There, Pasquale Pistorio, chief executive of SGS-Ates Componenti Elettronici SpA, Agrate, sees a more pleasant economic climate for both Italy and France making itself felt in the weeks to come.

"We should see all of Europe in a period of economic growth by the end of the year," he predicts. With things already looking up in West Germany, there is reason for optimism in both Italy and France, that country's major trading partners.

Haunting. If there is a specter haunting the optimism, it is that demand is far outstripping supply—a situation that firms prices and also lengthens delivery times and creates shortages. In one case, Jean-Pierre Liebault, marketing director for Matra-Harris Semiconducteurs in Nantes, reports he is accepting no orders for the 8051 single-chip microcomputer for delivery before the second quarter of 1984.

Much shorter delays than that have created an artificial demand in the past, with double ordering and excessive stock-building by equipment manufacturers. For example, SGS-Ates' Pistorio reports that his U. S. and Far East subsidiaries, as well as the European headquarters, were recently contacted by the same customer for the identical order.

Still, the components manufacturers are unanimous in feeling that the basic market strength is enough to ride out quite a bit of double ordering. How long will the boom last? "At least through 1984," confidently predicts Oswald of Siemens. □

Reporting contributed by Kevin Smith, London, and John Gosch, Frankfurt.

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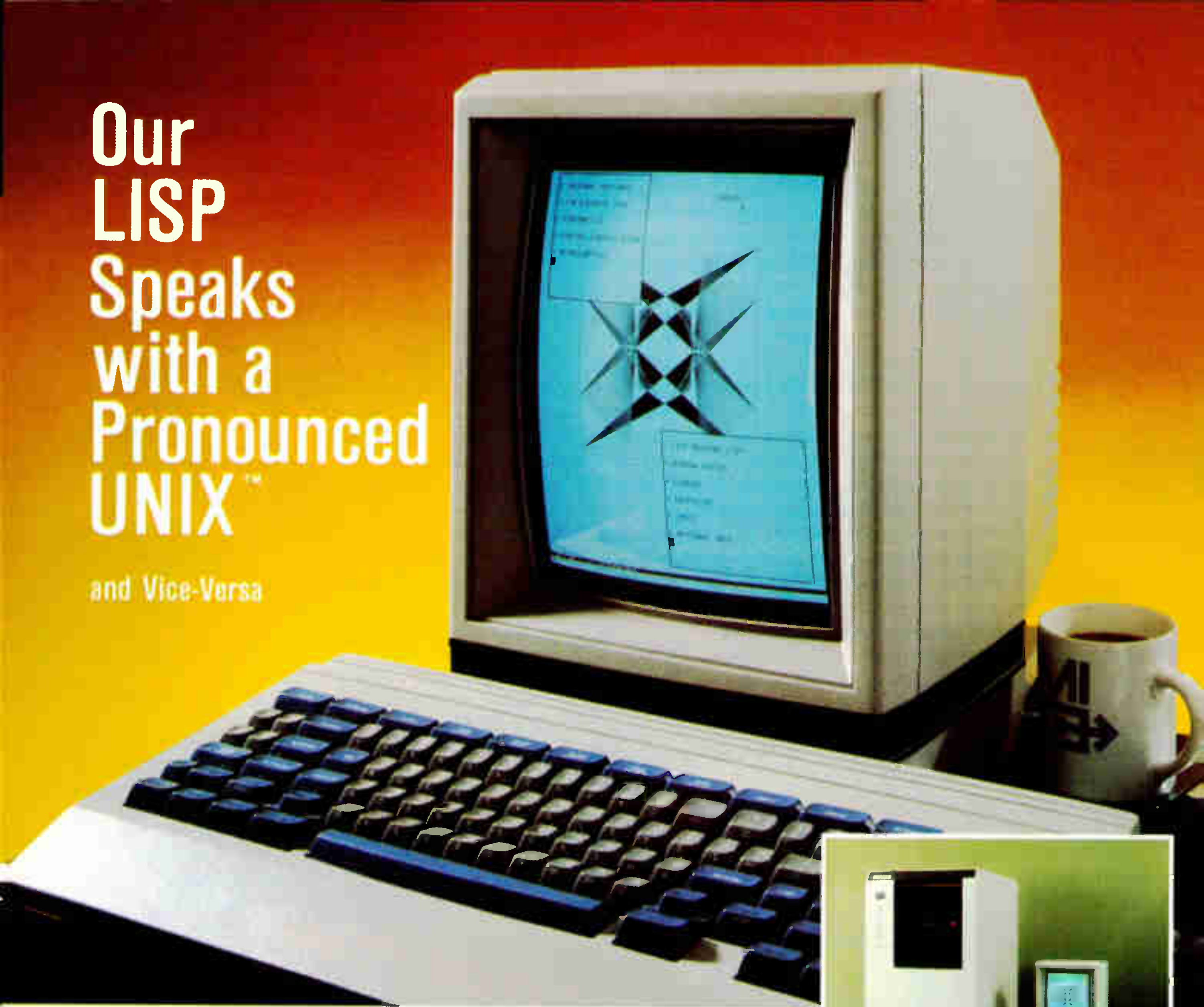

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Telecommunications

Video conferencing sees new window

Opportunity lies in data-compressed 56-kb/s color video codecs that will use AT&T's new packet-switched network

by Clifford Barney, Palo Alto bureau

Video conferencing, which is widely regarded as an idea whose time is always just around the corner, must now pass two more corners. The first of them is the emergence of data-compressed color systems that provide full-motion, albeit somewhat erratically, at 56 kilobits per second. The second is the establishment of AT&T's 56-kb/s digital switched network, which is reported to be on schedule for installation in 50 U. S. cities by the end of 1984 and triple that number in another year.

These converging events—56-kb/s service available for a 56-kb/s system—will make video conferencing cheaper. But not until those corners are turned will it be clear whether or not the new technology is good enough to support practical applications. For as 56-kb/s systems try to undercut their high-bandwidth, full-motion rivals, freeze-frame video—available for several years—is still a cheaper alternative for those users who think they can do without motion.

T1 lines. The most effective full-motion video-conferencing systems that are available today transmit over 1.544-megabit/s T1 telephone lines. The users of these systems say that their picture quality is very high. So too are their costs: $1,500 an hour for a nationwide point-to-point connection. American Telephone & Telegraph Co. will not talk about prices yet, but industry sources say that the likeliest rate for the packet-switched, 56-kb/s service is about $80/h. At this level, says Robert Widergren, the founder of Widergren Communications Inc. (Widcom), of San Jose, Calif., "it will be economically practical for a company to install video conferencing."

Widergren contends that it is already practical, visually—though that is a subjective judgment. In January his company is scheduled to deliver a 56-kb/s color video system it is developing for the Defense Advanced Research Projects Agency.

Breaking up. The system tolerates motion, but an abrupt action—the scratching of an ear, for instance—causes the transmitted picture to break up into blocks of pixels around the moving area, though the picture recovers quickly once motion stops. (In industry parlance, the system is still referred to as providing full motion.) Darpa will reportedly give Widcom's teleconference coder-decoder, the model VTC-56, to the Navy for testing.

At $85,000, this Widcom codec costs little more than half as much as the T1 system introduced in August 1982 by Compression Labs Inc., also of San Jose. The difference in line charges will make the Widcom codec much cheaper to operate, too. In picture quality, the two systems differ sharply. The T1 system's broad bandwidth gives excellent fidelity—"good enough to watch a football

The way of compression

To retain all information, the direct digitization of NTSC broadcast video color signals requires about 80 megabits per second, far beyond the capacity of most transmission lines. To transmit full-motion color at lower bandwidths, the digital signal must be compressed by the removal of redundant information. There are two main approaches. In interframe coding, successive video frames are compared, pixel by pixel, and only changed values are transmitted. In intraframe coding, values for entire blocks of pixels within a frame are transmitted as mathematical transforms. Compression Labs Inc., San Jose, Calif., used both methods to get a 50 : 1 bandwidth reduction that allows video signals to be coded and sent at 1.544 Mb/s over T1 lines.

To get a further reduction to 56 kilobits/s, Widcom Inc., San Jose, squeezes out data on luminance, hue, resolution, and scan rate. The company's cosine transform compresses data efficiently but causes the picture to break into blocks of pixels when the transform needs time for each recalculation and the system has too many bits to send. A different 56-kb/s system being developed by Avalex Inc., of Silver Spring, Md., uses a binary algorithm that degrades by losing resolution when overwhelmed by too much motion. Progress in hardware technology that speeds up these calculations beyond what is possible with the high-speed Schottky logic applied, for example, by Widcom may offer still further improvements.

Slow-scan systems, such as those made by Colorado Video Inc., of Boulder, Colo., do not use video compression but instead store all frame information in a buffer and transmit the bits, saving the information in a receive buffer and displaying a new frame every few seconds. The resolution can be made as fine as the user desires, though data sent must be traded off against time. **–C.B.**

game on," says one user. The Widcom system at times demands considerable forgiveness from the user.

Some analysts believe the T1 system seems more suited to executive meetings that involve large and critical audiences—of stockholders, for example; the 56-kb/s codecs are more suited for transmission of drawings and documents among coworkers. In the latter application, however, the price/bandwidth curve meets that of slow-scan video, which can transmit still pictures over ordinary phone lines on equipment that costs one tenth of the Widcom unit. (A slow-scan codec costs about $6,000; a whole system, less than $10,000.)

"Making a choice in video conferencing requires a systems approach," observes Thomas B. Cross, the video consultant who runs Cross Communications Co., in Boulder, Colo. "You have to decide whether you always need motion. I'm not convinced you do."

Slow-scan. Cross contends that "talking heads" are an expensive extra in video conferencing and that the freeze-frame techniques of slow-scan—now down to about eight pictures a second in the fastest system, from NEC America Inc., Fairfax, Va.—convey enough information for most conferences. He observes, too, that slow-scan systems operate with any phone in the world.

Cross believes that slow-scan has been overlooked by those interested in video conferencing. That, however, will change, he says, if International Business Machines Corp. decides to market a slow-scan system it developed for its own use. He points out that IBM has some 30 slow-scan installations with software that lets a Series 1 computer manage a whole series of transmissions. "If IBM makes that system available, it will pour gasoline on the slow-scan market," he says.

Cross will sponsor a video-conferencing seminar next month in Boulder. The full-motion T1 and slow-scan systems, but not the 56-kb/s systems, will be described, along with various computer-conferencing techniques. The seminar, practicing what it preaches, will be available at other locations through audio and slow-scan conferencing hookups.

Besides Widcom, at least two other companies have developed 56-kb/s motion systems. Avalex Inc., of Silver Spring, Md., however, is not betting on 56-kb/s digital switched service alone. Rather, the Avalex system is configurable from 19.2 kb/s to 1.544 Mb/s, so it can be used with either T1 or switched digital service.

Combining the two. Late in October NEC America introduced a black and white system that combines a slow-scan capability with 56-kb/s transmission. The system transmits with a resolution of only 128 by 128 pixels—a quarter the resolution of the Avalex and Widcom systems. But it is much cheaper, too: $15,000 for the model Netec-XD digital video codec.

NEC is evaluating the best format for the system, says Mike Stevenson, marketing vice president. The alternatives are full motion, occupying a full 21- or 23-inch screen, or motion in just one quadrant of the screen while the rest displays a chart or a schematic that would be transmitted by slow-scan. NEC will supply a freeze-frame codec for $16,500, and a $35,000 color version of the motion codec will be available at the end of the first quarter of 1984.

Meanwhile, AT&T Information Systems has just picked a commercial T1 system for its video-conferencing service, PicturePhone. AT&T, which chose Compression Labs' VTS 1.5E, will make it the backbone of the company's public and private teleconferencing rooms. The contract—for some 300 systems over three years—was reported to run to about $20 million, a shot in the arm for Compression Labs, a privately held company that expects to double its sales this year, to about $12 million. It ousted giant NEC as supplier of motion video equipment to AT&T. (Widergren was among that company's founders, back in 1976. He later left, forming Widcom in 1979.)

The VTS 1.5E sends video at 512 kb/s and can multiplex video with voice and data. Still, it must use a T1 line. Acknowledging that "price sensitivity is way up there," a Compression Labs spokesperson suggests hopefully that AT&T might choose to provide a lower-bandwidth—and cheaper—alternative to T1.

T1 fidelity, however, "may be the quality barrier," says Elliot Gold, of TeleSpan, an Altadena, Calif., research firm. Gold describes Widcom's approach as "doing the best you can to get a recognizable picture," adding that he did not think that the quality, though remarkable at such a low bandwidth, would be good enough for conferencing with motion. More likely, he says, 56-kb/s codec applications will overlap with slow-scan applications, a prediction supported by NEC's new hybrid.

Widergren thinks 56-kb/s video will be valuable in such technical areas as engineering or medical laboratories, where visual information—on charts, graphs, and schematics—must be shared. A version of the Widcom system, for sending X-rays, is now used at San Francisco's University of California Medical Center.

"Business people are intimidated using expensive video facilities that cost thousands of dollars an hour—they feel that they have to make every minute count," remarks Widergren in assessing that market.

Certainly the market has yet even to get moving; equipment suppliers describe business in numbers of customers, not gross volume. Cross, conceding the market "is just not happening," says that about 300 slow-scan systems were installed last year. Full-motion has been even slower to take hold, he says, with fewer than 30 systems installed.

Still to come. A report by Frost & Sullivan Inc., a New York research analyst, puts the whole market for compressed-data video equipment this year at only $8.7 million, rising to $32.6 million by 1987. Only $3.5 million this year—$9.1 million in 1987—will go for codecs.

By contrast, the report pegs the market for video-conferencing services at $370 million this year and $1.218 billion in 1987, figures that reflect the large impact of communications costs, which are more than 10 times higher than the equipment costs. That is why Widergren is so sure that his market is going to take off when 56-kb/s service is available. "Let AT&T install T1 systems," he says. "It will take their minds off what we are doing." □

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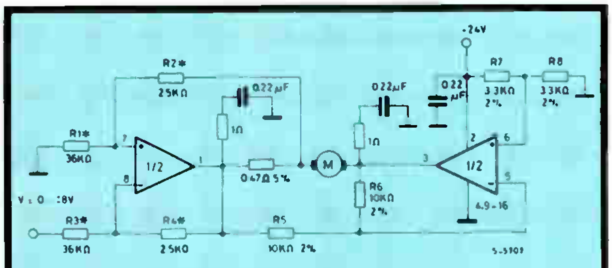

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Industrial

Market up slightly at Interkama

Though growth of instrumentation and automation has slowed, the Düsseldorf meeting sees an upturn on the horizon

by John Gosch, Frankfurt bureau manager

For the world's manufacturers of instrumentation, industrial-control, and automation equipment, business is not what it used to be. No longer are they working at top capacity and wallowing in a backlog of orders. No longer are they enjoying the double-digit growth rates of the 1960s and 1970s. Instead, the real rate of expansion during the early 1980s has slowed to less than 5%.

This will be the message from market experts at the 9th International Congress and Exhibition for Instrumentation and Automation—Interkama, for short—to be held Nov. 9 through 15 in Düsseldorf, West Germany, the capital of the state of Northrhine-Westphalia.

There, at the world's largest gathering of its kind, more than 1,100 exhibitors from 30 countries, including some 60 U. S. firms, will have their frontline wares on hand. Some 100,000 are expected to attend the triennial meeting—the ninth since 1957—during which exhibitors will present both technical papers and hands-on seminars.

The reasons for the industry's slowdown are simple. "Economic changes, more than technological factors, are influencing business in the control and automation sector," declares Hans Habermann, president of this year's Interkama. "The worldwide recession has led to a severe downturn in growth."

In many industrialized and developing countries, balance of payment problems, high interest rates, unemployment, and huge debts abroad have caused cuts in investment in new plant and equipment, says Manfred Thoma, chairman of the Interkama congress. Even some usually cash-rich oil-producing and -exporting countries are currently keeping a tight rein on equipment purchases.

Further, the anti-nuclear movement in some European countries, like West Germany, Austria, and Switzerland, has governments reviewing their spending plans on atomic-power plants, which are usually big customers for instrumentation and automation gear.

Elsewhere, "although the market for robots and material handlers is increasing vigorously, its impact on the sector as a whole is not all that big yet," points out Rolf H. Schuh, an Interkama official.

All told, Interkama estimates put worldwide end-user spending (including that in the East Bloc and in developing countries) for instrumentation and automation equipment at about $48 billion this year, up from about $40 billion in 1980, the last time the show was held. These figures include hardware requirements, as well as engineering, software, installation, startup, and service.

Not gloomy. Despite the bad news, though, the mood among Interkama exhibitors in Düsseldorf this year will not be one of gloom. "After all, unlike other industries, the instru-

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mentation and automation sector is still [growing] on the positive side," observes Schuh.

Also lifting spirits are the prospects for better times ahead. In some parts of the world, the recession is starting to bottom out, with encouraging signs appearing in the U. S. and in some major European economies. Against this backdrop, Schuh expects the worldwide instrumentation and automation market to start growing in the double-digit range as early as next year and to continue growing at least through 1986.

Behind the upswing, says congress chairman Thoma, will be the changing nature of energy generation, as exemplified by coal-liquefaction and -gasification processes, as well as the development of economical ways to recover waste materials. Another factor is the increasing effort in environmental protection. "Above all, however, is the continuing need to make production more efficient through automation," says Schuh.

Leaders. The U. S. produces around 40% of the world's intrumentation and automation equipment. West Germany follows with 10%, and close behind and rapidly moving up is Japan, with 9%. The United Kingdom accounts for 5%, France for 4%.

In instrumentation and automation exports, the U. S. ranks first, followed by West Germany, the UK, France, and Japan. The top six importing countries line up somewhat differently: the UK, West Germany, France, the U. S., Italy, and, in sixth place, Japan.

The largest customers for the gear are utilities, heavy industries, and chemical factories. In power plants, instrumentation's share of a new installation's total cost is 5% to 6%—and the percentage rises to around 8% for a nuclear-power plant, what with its heavy emphasis on safety and monitoring equipment.

Bigger shares. For a pig iron blast furnace, the instrumentation share is only 3% to 4%. But for an integrated steel mill, it can go up to 15%—even to 16% for a highly automated continuous-casting plant. In the chemical industry, the norm now is around 14%, as against 7% in 1960.

Nobody knowledgeable in instrumentation and automation comes to the show expecting to be bewildered by innovation. Instead, visitors will see a steady evolution of technology, not revolutionary advances. They will find that some trends in instrumentation follow those in, say, communications and data processing.

Smart. Most obvious is the ever-increasing use of microprocessors, which allow measuring and control equipment not only to monitor but also to calibrate itself. Microprocessors are also spurring digital design, and that, in turn, is pushing the trend toward decentralized process-control techniques in large plants.

Horst Kaltenecker, scientific consultant in the Control Systems Development Group at Siemens AG in Karlsruhe, also points toward the use of data highways in large industrial organizations to link office and process-automation equipment into one network. This enables managers to monitor virtually all aspects of plant operation.

Also of note is the increasing cost of software, says Adalbert Schmid, sales director for instrumentation and automation equipment at Philips GmbH in Kassel, an affiliate of the Netherlands electronics giant. "In many projects, software cost far outweighs that of hardware, and customers, even with knowledge in electronics, fail to understand the impact and importance of software," he observes.

Visitors expecting to see fiber optics proliferate in industrial control will be disappointed. Compared to coaxial cables, glass-fiber links are generally too expensive, says Siemens' Kaltenecker. "Besides, the optical components required still do not exhibit satisfactory characteristics," he adds.

While speech-output systems are penetrating instrumentation and automation, "the general use of speech input devices is still years away," Kaltenecker says. Big changes are due, though, in displays. In control rooms, huge panels with lights and symbols are giving way to cathode-ray tubes that show flow charts, tables, and text in vivid color and whose information can be scrolled or easily changed. □

Electronics abroad

Korea seeks broader electronics clout

Investments focus on chip R&D and a move from consumer electronics into faster-growing industrial products

by Robert Neff, McGraw-Hill World News*

Visitors to South Korean electronics plants generally express amazement at their scale, modernity, and efficiency. Korean companies, far more than those of Asia's other developing countries, are investing mightily to become worldwide electronics powerhouses [*Electronics*, June 16, p. 98].

"I couldn't believe the front-end capitalization of that plant," exclaims a manufacturing manager of a major U. S. defense electronics firm, who spent a week in Korea last spring. "They've got five $350,000 wire wrappers going when we've just bought our first," he says, speaking of a plant owned by Gold Star Semiconductor Ltd.

Yet little native innovation of note is to be found in the country's development laboratories and factories. Korea's impending invasion of international high-tech electronics markets will come mainly as a result of licensed technology. Most of its research and development efforts aim to catch up to the levels of technology in the West and Japan.

Behind. "Our overall technological level is 5 to 10 years behind the U. S. and Japan," admits Lee Won Ung, coordinator of electrical and electronics engineering at the Ministry of Science and Technology's Office of Science and Technology Policy. "So for the next four to five years, we must learn their technology to narrow the gap."

With just under 1% of the nation's gross national product going

*Robert Neff now works for International Management Magazine, a McGraw-Hill publication.

into R&D, it is easy to understand why Korea has little technology of its own to commercialize. Of course, the route it is taking need not be a drawback: Japan took it to get where it is today. One difference, however, is that this time, the licensors generally insist on a piece of the action.

Honeywell Inc., for example, has a joint venture with Gold Star to make minicomputers. AT&T Western Electric and Gold Star are partners in a semiconductor communications venture, and Corning Glass Works has invested millions in a joint venture with Samsung Semiconductor & Telecommunications Co. to produce television sets. NEC Corp. and Samsung are partners in computer and peripherals manufacturing.

Rights. Still, in 1981 South Korea's electronics industry spent only 2.6% of sales on buying the rights to foreign technology, as against 3.3% for Korean manufacturers as a whole. A 1982–86 five-year plan to push Korea's television- and stereo-oriented electronics companies into higher-growth industrial electronic products will in all probability cause that first figure to start rising.

By 1986 Korean companies should be producing enough large-scale integrated circuits to make the country the world's largest exporter of computer terminals. Local materials will have to form at least 85% of the product, as opposed to 15% at the plan's outset. "These goals may be optimistic," says a U. S. embassy report on the subject, "but it is generally agreed that large Korean firms, such as Samsung and Gold Star, have the wherewithal to greatly increase R&D and to make other changes to stay competitive." "Wherewithal" means motivation and money, part of which will come from new tax incentives for R&D.

Conspicuously unmentioned by the plan is engineering talent, in critically short supply. One estimate suggests that 22,000 Korean-born electrical engineers throughout the world have MAs or Ph.D.s. Many are overseas, and for most of them, returning to Korea would involve sacrifices.

The Ministry of Science and Technology, however, thinks that many of these EEs can be lured back, and there is indeed some reason for hope. In the past year, for example, Hyundai Electronics Industries Co. recruited several top Korean engineers from good jobs in the U. S., dangling before them positions in a bold new start-up, good pay, and a lofty appeal to patriotism.

Education lack. Adding to the talent shortage is the inadequate scientific and engineering education offered in Korea. "They don't seem to grasp the fact that it takes more than just words to create a qualified engineer," says a U. S. computer executive based in Seoul. "There are still no good computer science programs in any university here. Everyone is trained overseas."

He notes that the Ministry of Education is taking steps to encourage the spread of private computer-training institutes, though these tend to turn out computer operators and programmers rather than designers and researchers. So it is not surprising that Korean companies, like some in Taiwan, are establishing R&D laboratories in the U. S. or that the government should be encourag-

Probing the news

ing the setting-up of such labs.

At least one Korean company, Gold Star, has invested in a U. S. firm in exchange for product and marketing rights. Two quasigovernmental organizations have organized a venture-capital firm to invest Korean money in overseas high-tech start-ups and to bring back the technology they develop.

R&D boost. Meanwhile, the government is working to lift R&D spending to at least 2% of the GNP by 1986. It also wants industry's share of R&D spending to rise to 55%, from a current 30%. "The question of how to achieve that is a very tough one," admits Lee, of the Ministry of Science and Technology. "The only way is to give them more incentives and to stimulate competition among them. That's a difficult job."

The government, with its increasingly noninterventionist approach to industry, can do only so much to stimulate private R&D. Already in place are policies sheltering from taxes up to 3% of a company's revenues or 1.5% of pretax profits if they are channeled into R&D. Researchers working for independent labs can avoid the otherwise universal conscription. Nonetheless, most of Korea's skilled scientists work for public institutes, although the government is hoping to shift the balance to industry.

Concurrently, the government has boosted its own R&D spending by 50% annually. This year's expenditures will total about $30 million, and next year's target, Lee says, is $50 million. About half goes to electronics. Both government and industry R&D focus on semiconductors, computer software, and telecommunications. "Our goal by 1986 is to acquire LSI technology from the design stage to total production," Lee says. "We want to develop up to 32-bit microcomputer systems, including software."

KEIT. The hub of publicly supported semiconductor and small-computer research is the government's Korea Institute of Electronics Technology, in the rural industrial complex of Gumi. The institute can already make 3-micrometer–rule chips and is producing 32-K read-only memories with licensed very large-scale integrated-circuit technology. It is trying to produce 64-K ROMs with 4.5-μm design rules.

Like Taiwan's electronics research and service organization, one of the institute's main roles is training engineers through joint R&D projects with industry. In semiconductors, these projects include development work on bipolar video-tape–recorder circuits, 8-bit n-channel MOS microprocessors, and custom VLSI circuits. Next year, the institute plans to start developing gate arrays, an 8-bit complementary-MOS microprocessor, a codec filter, and an erasable programmable ROM.

As for computers, last year the institute helped promote the development of personal computers by managing a project in which five local companies worked out their own systems, buoyed by a guarantee that the government would buy at least 1,000 of any approved model. All five firms had their models approved.

The institute is also standardizing input and communication codes for Korean and Chinese characters and is trying to adapt AT&T Bell Laboratories' Unix operating system to 16- and 32-bit microprocessor systems. The institute's annual budget, about 10 billion won ($12.6 million), comes mainly from a World Bank loan, from the Korean government, and from industry payments for such products and services as circuit masks, high-purity gases, epitaxial materials, and circuit design. The money supports a staff of about 300, including 8 Ph.D.s and about 130 additional university graduates.

Software. The country's computer software effort is spearheaded by the Korea Advanced Institute of Science and Technology, whose software development center and its staff of 350 works on applications that include such things as industrial management, medical information, microprocessor systems, and remote sensing. The center, says its president, Sung Ki Soo, is the largest of its kind in Asia outside Japan.

Will Korea catch up? "We have to," declares Lee, of the Ministry of Science and Technology. "Is there any other way to survive in this competitive world?" □

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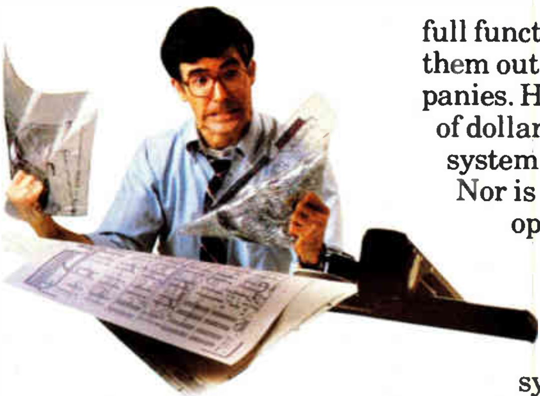

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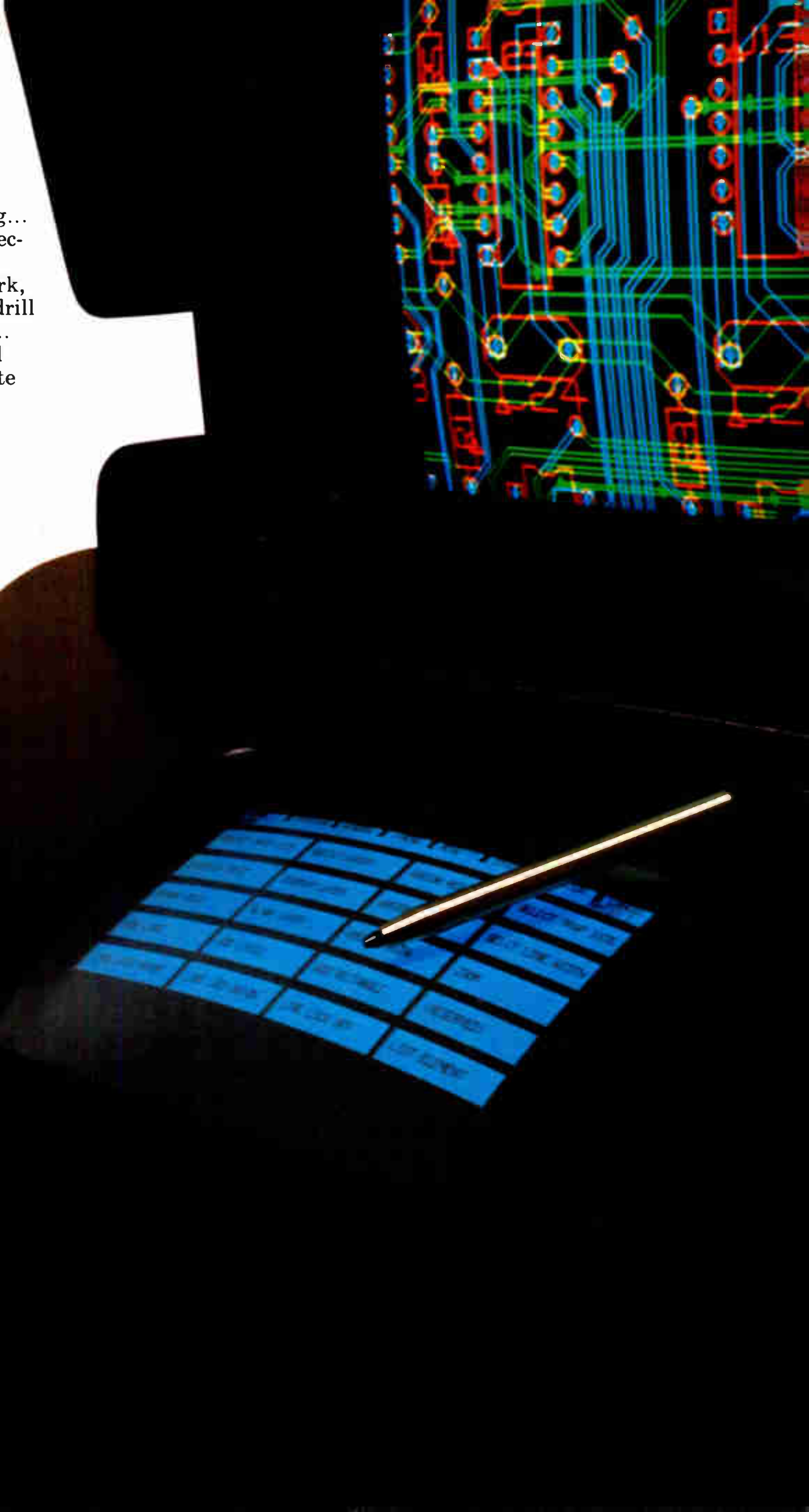

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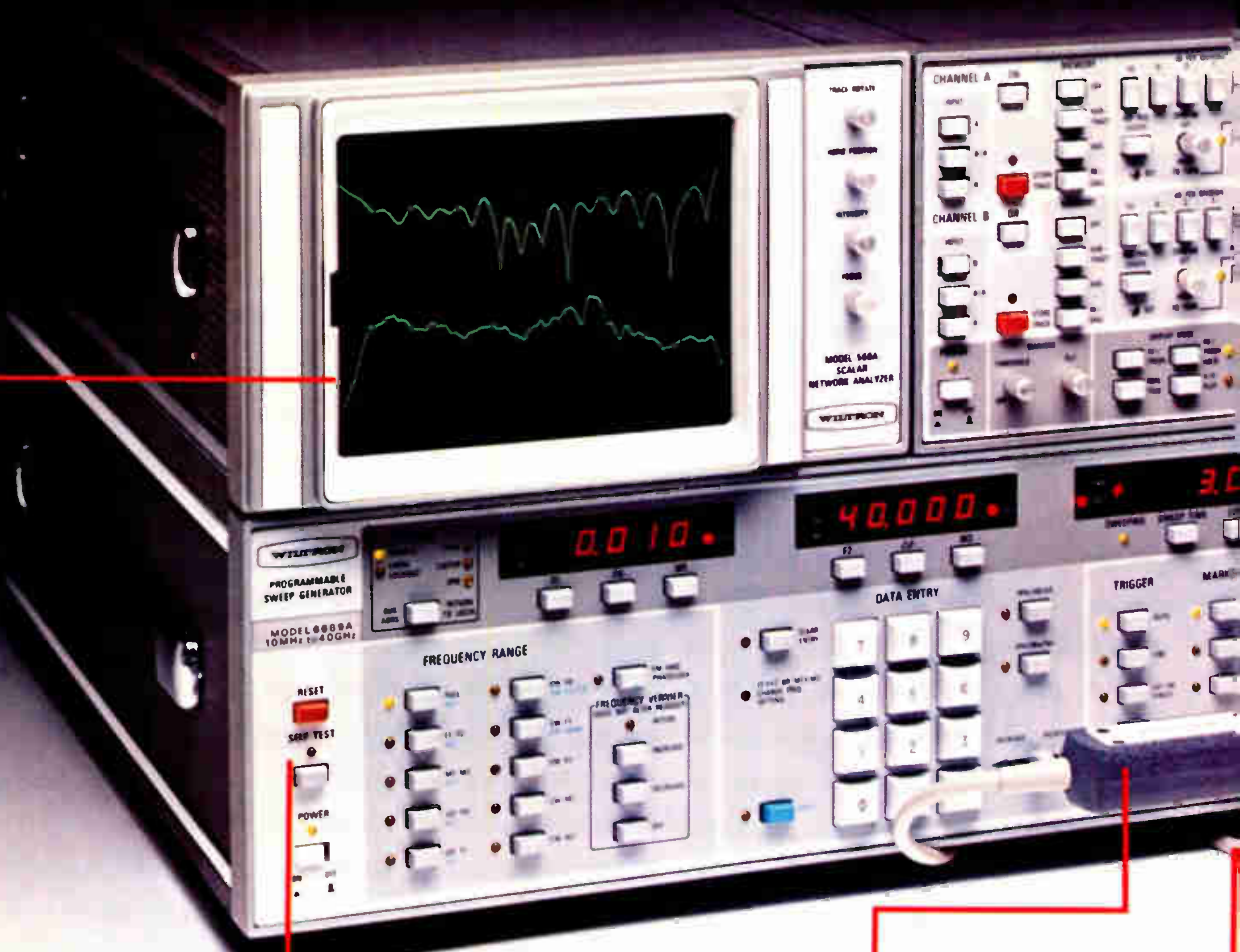

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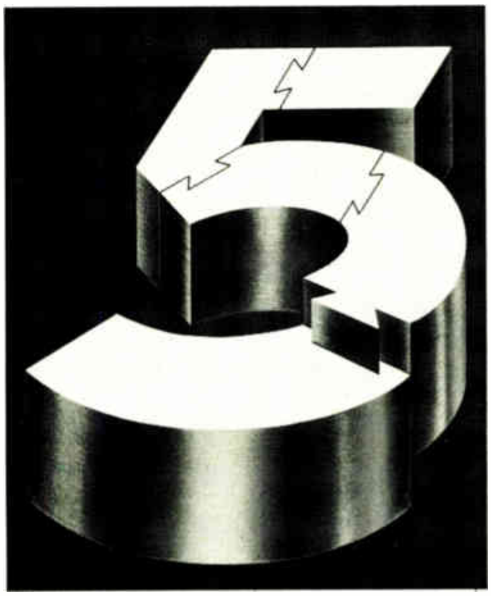
by Chandra R. Vora, Mark Hecker, and Donald Wiser, *Data General Corp., Westboro, Mass.*
and Robert Murdoch, Steve Hamilton, and Nabil Takla, *Data General Corp., Sunnyvale, Calif.*

☐ As system designers take aim at the next generation of computer hardware, new chips that merely widen available word length will not provide enough ammunition. Other considerations besides the central processing unit have to be weighed, too—floating-point processing and input/output handling, for instance.

Data General's new microEAGLE chip set, now in development, will anticipate these needs with a fully integrated combination of five chips. These will form a complete foundation for low-cost, compact systems compatible with the company's Eclipse superminicomputers.



Achieving compatibility with MV series machines was among the design's most important goals; in fact, its performance is about half that of an MV/8000. The design also took up the challenge of minimizing the external logic required to build a system that would implement the architecture of Data General's 32-bit Eclipse MV superminicomputer, which supports 4 gigabytes of virtual memory.

This new and, for now, experimental family of very large-scale-integrated n-channel MOS circuits (Fig. 1) includes a central processing unit, a microsequencer, a floating-point unit, a system I/O unit, and a burst multiplexer channel unit. A proprietary titanium disilicide process and 3.5-volt internal operating voltage help speed operations while holding power dissipation to 3 watts in these complex devices (see "Titanium disilicide boosts performance," p. 123). The CPU executes 32-bit register-to-register operations in a single 400-nanosecond microcycle and performs memory-to-register moves in two cycles with a high degree of parallelism. The floating-point unit, itself no sluggard, handles a double-precision (64-bit-wide) addition in four cycles. The system input/output chip generates Eclipse MV/series I/O bus activity and at the same time provides several internal peripheral functions. Its companion, the burst multiplexer channel unit, handles the burst multiplexer channel I/O of the Eclipse MV/ series.

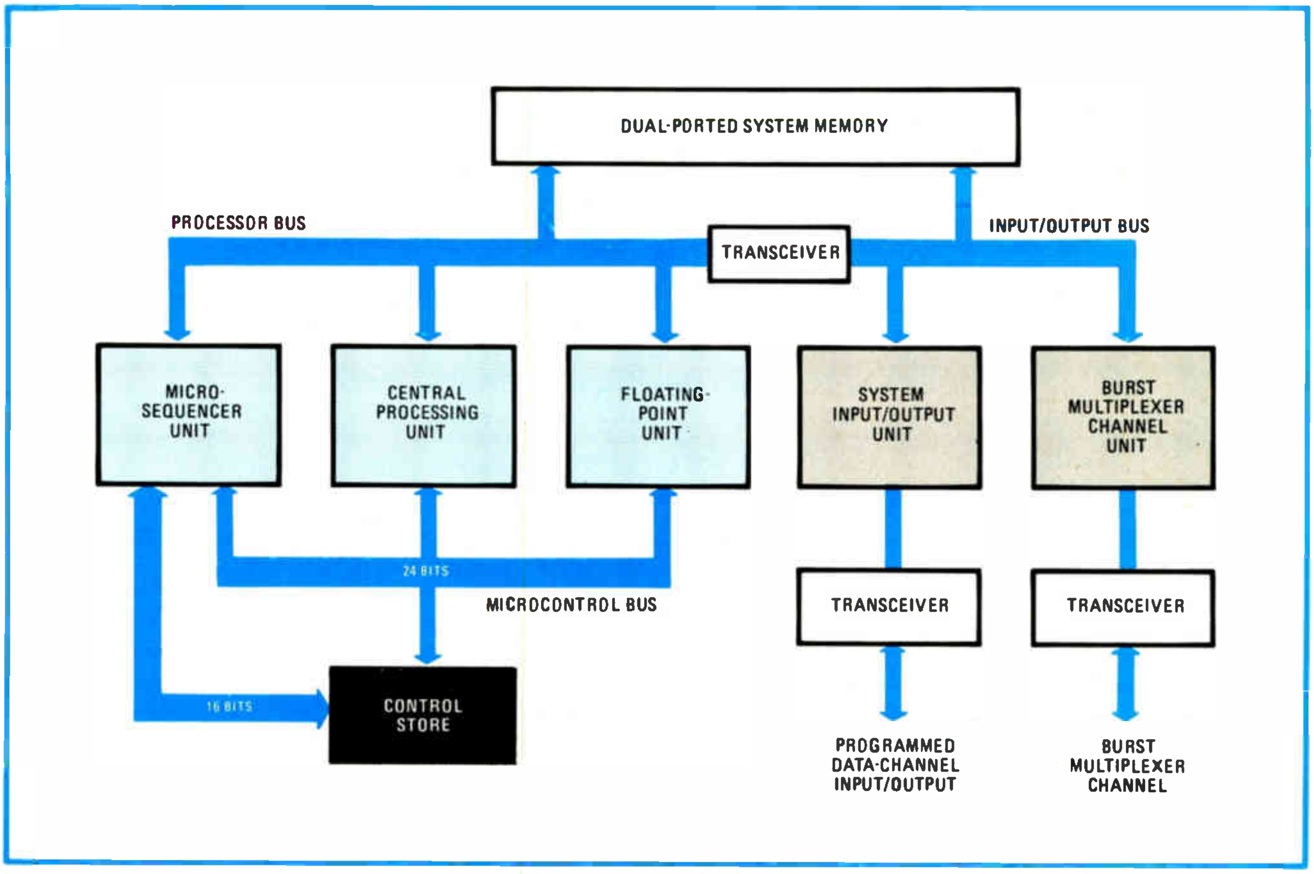
These system elements communicate over a three-state, bidirectional, 32-bit-wide address-data bus (the system bus). One bus transaction occurs during each cycle (T period). For more efficient use of hardware resources, four external clocks divide each T period into eight equal subcycles, S_0–S_7.

Thus, for example, the CPU's register file can be accessed as many as four times in one cycle. An address is driven on the bus during S_1-S_2-S_3, and data is driven during S_5-S_6-S_7. (In order to prevent bus contention, the bus is not driven during subcycles S_0 and S_4.) The system's timing determines what is driven onto the bus. No other signals are needed to indicate that address or data are on it.

A special READY pin signals whether a given bus operation has been completed during the current T period or needs to be extended for another one. No new transaction can be started until the assertion of READY indicates that the current transaction is complete. READY is sampled during the seventh subcycle of every cycle.

A system element must request and be granted the bus before initiating a transaction. Using a minimal amount of external hardware, the system elements are linked in a daisy-chain priority scheme to arbitrate access to the bus. At the lowest end of this chain is the CPU, which has the lowest priority. When no other devices put in a request for the bus, the CPU is responsible for filling it with an invalid transaction. On the other hand, a special VALID bit in the 6-bit control field generates normal valid operations (Fig. 2).

To support multiple-cycle bus operations, a system element can assert the LOCK bit and prevent a higher-priority device from taking over the bus. They must



1. Powerful pentad. Besides a conventional single-bus configuration, this dual-bus approach boosts throughput for a system built out of the five microEAGLE chips. A separate bus handles processor transactions, while another manages the system's input/output activity.

respect the LOCK bit by not requesting the bus if it happens to be locked.

The five chips can be configured in both conventional single-bus and high-performance dual-bus designs. In the dual-bus arrangement, the system input/output unit and the burst multiplexer channel unit contend for one bus while the CPU uses the other. The resulting increased memory bandwidth enhances system performance. Each bus has its own priority chain and is arbitrated independently. Under some conditions, such as a LOCK operation, a requestor must gain control over both buses simultaneously by using a transceiver, which connects the two as one bus.

BIT	0	1	2	3 4 5	6 ...	31
OPERATION	VALID	LOCAL	LOCK	BUS OPERATION		
SYSTEM ADDRESS	X	0	X	X X X	PHYSICAL ADDRESS	
LOCAL ADDRESS	X	1	X	X X X	DEVICE SPECIFIER	OFFSET WITHIN DEVICE

BUS OPERATIONS

```
000 RESERVED
001 WRITE BLOCK
010 READ DOUBLE
011 READ BLOCK
100 WRITE HIGH BYTE
101 WRITE LOW BYTE
110 WRITE SINGLE
111 WRITE DOUBLE
```

DEVICE SPECIFIER

```
001000 0000 SYSTEM INPUT/OUTPUT
000100 0000 BURST MULTIPLEXER CHANNEL
000010 0000 FLOATING-POINT UNIT
000001 0000 CONSOLE
000000 0001 MICROSEQUENCER
```

2. Addressable. A 6-bit control field extends the flexibility of the microEAGLE chip set. When addressing system memory (LOCAL bit = 0), the remaining 26 bits represent the physical address. Alternatively, the remaining bits can address memory local to the other chips.

System elements other than main memory can communicate through the local-communications address space by asserting the LOCAL bit in an address, bit 1 (see Fig. 2). This address space is partitioned among the system I/O unit, burst multiplexer channel unit, floating-point unit, and microsequencer chips, as well as the virtual console read-only memory. The CPU may utilize this local-address mechanism to send commands to the I/O chips, for example.

The central processing unit

A true 32-bit chip, the CPU (Fig. 3) uses five major units—for fixed-point arithmetic, address translation, autonomous fetch, control, and external interface. Through them, it performs all fixed-point operations and addressing in the microEAGLE system. The address-translation unit provides memory management with a 2-K-byte page granularity and supports a physical address space of 128 megabytes. Up to 16 address translations are immediately available in a fully associative cache inside the address-translation unit. The on-chip design permits address calculation and subsequent translation in one cycle.

The address-translation unit also supports a long-address–translation process, performed by microcode, that translates a logical address when the translation is not in the address-translation unit's cache and saves the context block during page faults when necessary. An enhanced first-in, first-out (FIFO) algorithm refills the address-translation unit's cache. If an encached translation is used while the FIFO pointer selects it, the pointer is incremented past that translation, so it will not be replaced until the next time around. This method is particularly effective for preventing the current program-counter translation from being thrown out of the address-translation unit's cache.

Fetching instructions

The CPU's autonomous instruction-fetch unit consists of a five-word instruction-register pipeline and program-counter pipeline. The unit permits simultaneous fetch, decode, and execution and initiates a prefetch operation whenever the address-translation unit has a valid translation for the required memory address and the system bus is not being used for other transactions.

The horizontal programmable logic array (horizontal PLA) is addressed by the sequencing unit. In response to a vertical microinstruction from the microsequencer, it is first addressed from the horizontal address field of the vertical. Subsequent addresses may be generated internally, a procedure that allows a fast and efficient response to internal states.

Exceptional conditions such as long-address translations, coprocessor waits, and memory waits are handled in the horizontal microcode, without interrupting the vertical microinstruction sequence. The key to executing exception-handling routines in horizontal microcode is the microcomplete signal, asserted to indicate to the microsequencer that the execution of a vertical microinstruction has been completed. By holding microcomplete unasserted during exception handling while the appropriate horizontal routine is executing, the microsequencer sees only a somewhat longer but otherwise completely normal execution of a vertical microinstruction.

The microsequencer chip

The microsequencer chip (Fig. 4)—which contains an instruction queue, decode logic, and microaddress-gener-

Titanium disilicide boosts n-MOS performance

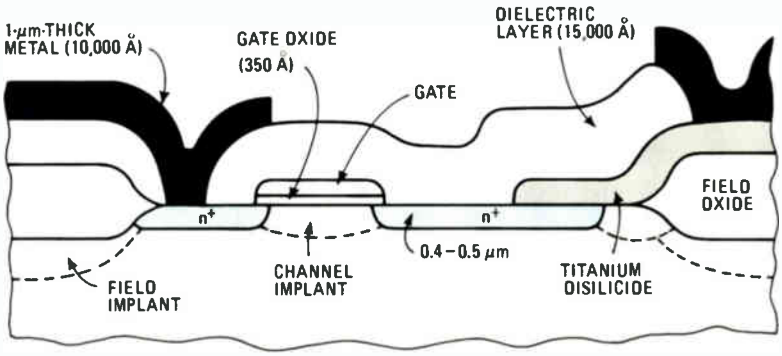
The proprietary advanced titanium disilicide n-MOS process Data General used to fabricate its superminicomputer chip set is based on 2-micrometer channel lengths, 4-μm metal widths, 3-μm metal spacing, and 350-angstrom gate-oxide thicknesses. In this process, titanium disilicide serves as a second layer of low-resistance interconnection (see figure). Produced with no extra photomasking steps, this layer is normally used to fabricate gates for MOS devices. Since titanium disilicide reduces polysilicon resistivity to about 1.5 ohms per square, its major advantage is the speed boost afforded by lower-interconnection RC time constants.

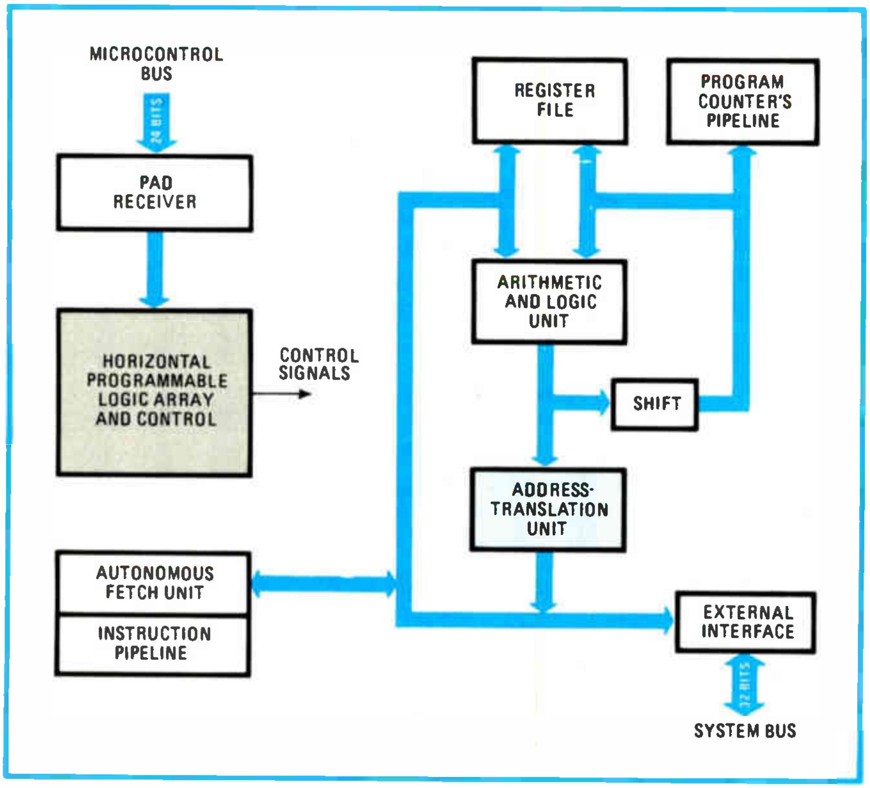
There are three additional benefits, too. First, since the chip's worst-case propagation paths are speeded up, its overall performance can be improved. Second, smaller drive and pull-down devices can be used to achieve the same propagation delay for less performance-critical internal paths. Finally, designers can apply regular structures for those same paths, to generate signals, rather than carefully craft custom structures. Although regular structures often have greater parasitic loads and, consequently, run more slowly, the titanium disilicide process can offset this effect.

Regular structures give designers shorter development cycles. Register-level simulation, logic simulation, circuit simulation, and circuit layout can be completed more quickly, and on-chip testability becomes more feasible. For complex chips like those in the microEAGLE set, speed, power, development time, and testability become increasingly significant.

Several techniques give designers the ability to observe and control the chip set's internal states. For example, in the central processing unit, the output of the arithmetic and logic unit is loaded into flip-flops before being sent to the address-translation unit. Three dedicated pins provide paths through which the contents of these flip-flops can be shifted out and external data can be shifted in. Five scan paths in the CPU reveal its internal state. For run-time checking, the system executes diagnostic microcode on power-up before passing control to the virtual console.

The chips use 3.5 volts for internal functions and a 5-V supply for TTL-compatible levels on all input and output signals. Scaling the internal power supply to 3.5 V increases the chips' speed and reduces their power consumption. Dissipating about 3 watts each, they will be packaged in 84–to–100-pin pin-grid arrays. Although the chips are compatible with an existing product, the very nature of such laboratory projects makes it possible that no finished product will be developed from them. Even a successful implementation would yield such products two years from now—at the earliest.





3. Central processing unit. Besides an on-chip fixed-point arithmetic unit, this member of the microEAGLE family boasts an on-chip address-translation unit with a 16-word associative cache. Addresses not in the cache undergo a microcoded translation process.

ation logic—performs instruction decoding and vertical microcode sequencing (see "Two-level micro-architecture hones performance," p. 126). Each double word of instructions taken from memory by the CPU's autonomous fetch unit is simultaneously loaded into the microsequencer chip. Both chips place the received double word into their respective instruction-register pipelines. As the execution of each macroinstruction is completed, the microsequencer decodes the next instruction in the pipe. The CPU uses two dedicated pins to keep the microsequencer informed of every word loaded into the pipeline, every word extracted from it, and every branch or other event that requires it to be flushed.

When the microsequencer transfers the execution control field to the CPU and the floating-point unit, it begins to execute its vertical sequencing instruction. Those chips do not execute the corresponding horizontal microcode until the next cycle. Any test results generated by the execution chips are not sent back to the sequencer for another cycle after that. Consequently, the microsequencer cannot conditionally branch on an instruction until two cycles after it has been executed.

Best guess

To mitigate the effects of delayed conditional branching, the microsequencer has conditional abort sequencing. It does not delay the branch until the test condition arrives; instead, vertical microcode can tell it to assume that a particular path will be taken and to continue along that path. If the test condition indicates that the wrong path was taken, the system aborts the current one and begins to execute the alternative. When the abort occurs, there is a time penalty of one or two cycles while the microinstruction pipeline is flushed and refilled. Using conditional aborts, the microcode can, for example, be configured to assume that a loop branch has been chosen, and thus optimize the iterative looping case.

To generate the address of the next vertical microinstruction, the microsequencer processes sequencing information from the external control store. Several hardware enhancements implemented in the microsequencer make vertical sequencing more flexible, most important among them a six-deep microaddress stack used in microcode subroutining. For the higher-level macroinstructions included in the MV instruction set, the modularity provided by subroutines is invaluable for developing reliable, maintainable, and space-efficient microcode.

Vertical microcode is stored either in read-only-memory– or in a random-access-memory—based control store. To accommodate engineering changes, the microsequencer chip has an associative memory that can override the selection of up to eight addresses in the ROM control store and divert the control flow to the writable control store. For loading and verification, the CPU can access the associative memory and the control store through the microsequencer's local address space.

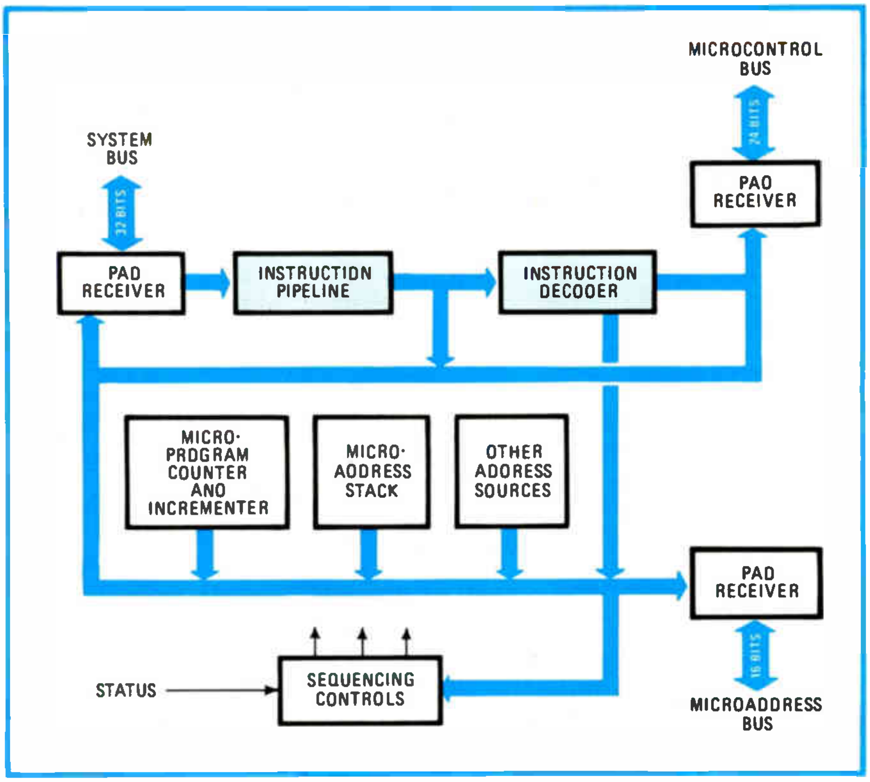
The floating-point-unit chip (Fig. 5) performs the floating-point instruction set of the Eclipse MV architecture, which uses the IBM standard hex-radix, 32-bit single-precision and 64-bit double-precision format. The chip's three major functional blocks—the execution unit, the external interface, and the control unit—all operate in parallel, increasing the speed of floating-point operations, especially for iterative algorithms.

Dual data paths

In the execution unit, two precharged 64-bit buses provide data paths between the mantissa ALU, the exponent ALU, sign logic, and the shifter. The A bus supplies data from the 64-bit register file to the ALUs, and the B bus supplies data to the other port on the ALUs and connects the other functional blocks.

The mantissa ALU is a combination carry-save–carry-propagate adder, combining both functions into one 66-bit-wide unit. The data inputs to the adder contain the latches and data paths needed to support multiply and divide algorithms. It can do two carry-save operations in a single processor cycle, allowing the floating-point unit to perform 4-bit multiplications each cycle using a modified 2-bit Booth algorithm.

The chip's 64-bit shifter can shift left or right from 0



4. Microsequencer. This member of the microEAGLE chip set uses a pipeline for more efficient decoding of instructions. An on-chip cache allows designers to replace microcode sequences in read-only memory with others in writable control store.

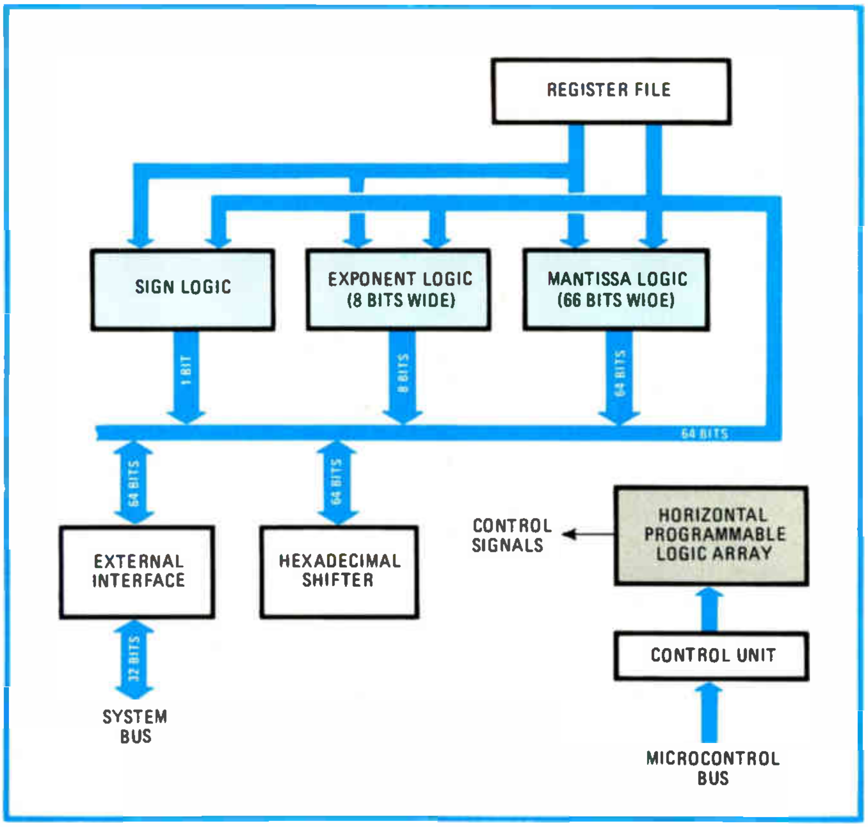
to 16 hexadecimal digits in one cycle. It prescales operands in addition and subtraction, normalizes floating-point results, and acts as a multiplier-quotient register in multiplication and division. For a given cycle, the number of digits to shift can originate from several sources. For prescaling, the output of the exponent ALU determines how much to shift. For normalization, a circuit at the mantissa ALU's output counts the number of leading zero digits and sends it to the shifter. For multiply and divide, the constants are selected from within the shifter control logic itself.

The external interface interacts with the system bus, supplying data to and receiving it from the other system elements. To optimize floating-point data transfers, this interface accesses system memory using an address generated by the CPU. The external interface unit consists of a dual-ported 64-bit bus interface register, the floating-point status register, the state save paths, and the control logic.

The control unit receives microinstructions from the microsequencer chip and generates horizontal addresses from the horizontal PLA. This unit contains a sequencer that allows a sequence of horizontal microinstructions to be executed for a single vertical.

The sequencer gives the horizontal PLA the ability to branch immediately on conditions within the floating-point unit, without the delay inherent in vertical sequencing. It can conditionally skip horizontal instructions or terminate the sequence, and it can branch by substituting condition bits directly into the next microinstruction's address. This last feature is used to detect special cases that are data dependent—for example, when operands are "0" in multiply and divide.

Two chips, the system I/O and the burst multiplexer channel, are compatible with Eclipse I/O buses. The system I/O chip controls programmed I/O, including program interrupts, certain basic I/O devices, support for the soft console interface, and control of the data channel function. Its companion, the burst-multiplexer-channel chip, handles



5. Floating-point unit. Two precharged 64-bit buses supply data to the arithmetic units in this chip, allowing parallel execution of floating-point operations. In addition, the shifter handles normalization functions and acts as an extra register in multiplication and division.

control of the Eclipse burst multiplexer channel.

The CPU chip executes programmed I/O instructions by transmitting a command through the system bus to the system I/O chip, within which programmed I/O control logic responds to the command by generating the I/O bus control signals appropriate for performing the needed transfer over the I/O data bus.

The system I/O chip's devices include the real-time clock, a programmable interval timer, a primary asynchronous line controller, and an Eclipse power-fail monitor. It also provides support for a powerful soft console and for the standard MV/series error-logging device.

Translation cache

A data-channel controller within the system I/O chip handles direct data transfers between the I/O bus and system memory. An associated map residing in physical memory contains their logical-to-physical-address translations. Besides encaching the six most recently used address translations, the system I/O chip boosts performance by prefetching output data from memory 32 bits at a time.

Across the chip's operating range—extending from a 300-ns to a 600-ns T period—internal frequency-synthesis logic ensures constant timing on the external I/O bus and constant real-time measurement from such internal devices as the real-time clock and the interval timer. A 32-bit-wide configuration register further enhances the chip's flexibility by specifying clock frequency, asynchronous line baud rate, data cache enable, and other operating parameters.

For high-speed data I/O, the burst-multiplexer-channel-unit chip manages an Eclipse-compatible burst-multiplexer-channel-unit I/O bus. The Eclipse burst multiplexer channel multiplexes up to eight controllers, transferring bursts of data at 8 megabytes/s between system memory and a burst-multiplexer-channel-unit I/O device controller, without CPU involvement. Bursts may vary in size from 1 to 256 16-bit words of data.

In addition, the burst multiplexer channel unit can transfer blocks of data on the system bus. A block transfer involves two consecutive 32-bit data transfers. In this mode, the chip performs block transfers for all memory reads and writes, whenever possible. □

Two-level micro-architecture hones performance

Because of the complexity of the MV family instruction set, placing all the microcode on the execution chips would have consumed area at the expense of hardware accelerators. Rather than sacrificing the set's performance goals, it was decided to keep microcode in an external control store. The number of control signals required and the limited number of pins on the execution chips made it impractical to transfer a complete control word to the central processing unit and the floating-point unit. A two-level micro-architecture was adopted instead.

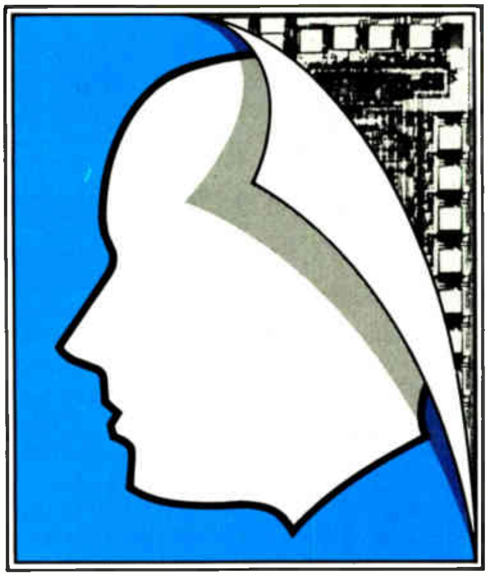
The microsequencer executes the higher-level vertical microinstructions, stored in off-the-shelf random-access or read-only memory. The vertical microinstructions consist of a 16-bit vertical sequencing instruction—interpreted by the microsequencer—and a 24-bit execution control field that is transferred to the execution chips, in which the execution-control field from the vertical addresses the horizontal microcode. The control store is arranged to minimize the need for very high-speed parts. The microsequencer uses 8 bits of the vertical microinstruction to set up data paths within the chip and for other critical controls. Although these 8 bits are stored in 150-nanosecond memories, the remaining 32 bits are not required as early, thus allowing the use of cheaper, 350-ns parts.

The macroinstruction opcode to be decoded is presented as input to a programmable logic array, the starting PLA, in the microsequencer. The starting PLA provides the initial sequencing information and the first 24-bit vertical microinstruction sent to the execution chips. Because the first microinstruction is on chip, there is no need to wait for the microinstruction pipeline to be filled when a new instruction is decoded. The 24-bit vertical field received by the CPU and the floating-point unit is interpreted as an 8-bit horizontal address followed by 16 bits of "arguments" for the selected horizontal. The 256-location horizontal address space is partitioned among the execution units, with the CPU recognizing some addresses and the floating-point unit others. That procedure allows CPU-oriented and floating-point-unit–oriented verticals to be mixed in the microcode stream. Some verticals are recognized by both chips, so concurrent operations can be performed. Some addresses are not recognized by either the CPU or the floating-point unit, allowing future expansion.

Micromodification is a technique for substituting as many as five fields from the 16-bit microcode argument into the selected horizontal. At the simplest level, this substitution allows a single general-purpose memory horizontal to be used to perform any one of the implemented memory operation, for example. A more sophisticated horizontal might allow any ALU operation to be performed on any two registers; the result might be placed in an independently specified third register.

In addition to micromodification, bits from the current macroinstruction op code can also be substituted into the horizontal. Four bits included as part of the starting-PLA sequencing information can independently control the substitution of up to 4 bits from the decoded macroinstruction op code into the vertical address specified by the starting-PLA entry. This feature allows as many as 16 macroinstructions to share a common starting-PLA entry and thus a common initial microinstruction yet also allows them to branch to separate external control-store addresses for the ensuing microinstructions.

The starting PLA contains about 260 entries that cover the more than 400 instructions implemented in the MV family architecture. The substitution technique for the starting PLA permits it to be placed in a substantially smaller area than would have been needed had one starting-PLA entry been used for each macroinstruction—and at virtually no cost to overall system performance.



Commercial products begin to emerge from decades of research

Expert and natural-language systems herald what could be a tidal wave

by Tom Manuel, *Senior Editor, Information Systems*
and Stephen Evanczuk, *Software Editor*

From the early days of computer science, when people like John von Neumann and Alan Turing began contemplating models of computational machines, the dream of building machines that think has fascinated scientists and society alike. From those heights of optimism, however, artificial intelligence plunged into an era of being labeled a useless discipline, from which it emerged as a somewhat arcane branch of computer science. In fact, despite an understandable wariness of popular notions about its capabilities, AI has taken its first careful steps toward becoming an accepted engineering technology in the commercial world.

Noting its capability to offer sophisticated computing power to untrained workers, the information-technology industry has turned its attention to AI in hopes of finding new ways to meet growing demands for better software. In turn, new companies—and new groups in established companies—have responded with the first wave of commercial products based on AI technology.

As a result of this surge of interest in artificial intelligence, U. S. industry will spend an estimated $66 million to $75 million this year to obtain some early benefits. Because AI techniques broaden the computer's capability into the realm of symbolic processing (the processing of concepts rather than just numbers), computers can get down to solving some of life's hard problems.

What are known as expert systems, or, more appropriately, knowledge-based systems, use AI methods to solve problems and to aid decision making by using a knowledge base along with rules of inference that apply to a specific field of knowledge. Some practical examples, now in limited use, include programs that diagnose diseases in several specialties, prospect for mineral deposits, assist in the drilling and analyzing of oil wells, analyze investments, configure computer systems, help repair locomotives, and assist business decision-making in conjunction with a spreadsheet program. These knowledge-based systems not only replicate and multiply the value of human expertise but also capture it and perpetuate it in computerized form.

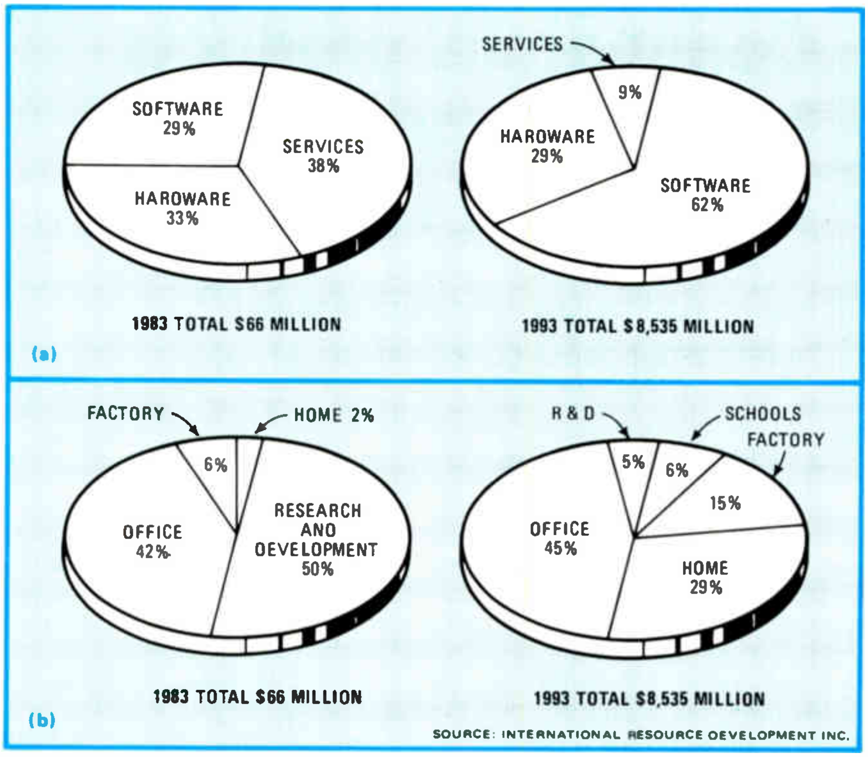
Other working AI systems give computers the ability to understand natural languages, English or others, albeit in restricted subjects or domains. Such natural-language systems make it easier for people without computer experience to use computers effectively for such functions as retrieving information from data bases, preparing the input for and running existing complex computer programs, and developing new computer applications without programming.

Because AI technology has at last demonstrated some practicality, especially in areas of great need and value, the applications summarized above tend to be big payoff stuff. In the next two to five years the worldwide computer industry will produce a wave of AI products that could turn into a tidal wave after that. Two recent U. S. studies of AI technology and markets bear this out. One, from International Resource Development Inc., of Norwalk, Conn., predicts an estimated U. S. market for AI products and services of $66 million in 1983, growing to $8.5 billion by 1993 (see figure on p. 128). The other projects the AI market year by year from 1983 to 1990 (see table on p. 129).

Changing times

AI has a long history of international research and nonexistent or precious little practical application (See "A 'new' technology goes back 27 years," p. 130). However, that state of affairs is changing because two necessary conditions have manifested themselves. First, there are important problems to solve that are too complex for conventional computational technology. Second, the recent availability of abundant cheap computing power and the promise of much more of it open the door for the discipline that has been called a useless science to finally yield some useful technology.

The long-term goals of AI specialists are computer systems that surpass human capabilities in reasoning, problem-solving, sensory analysis, and environmental manipulation. However, AI still has many limitations and a great deal of research still must be done. For the present,



Exploding market. These market projections for artificial intelligence products suggest the emergence of another big growth market in the computer industry at the end of this decade. The future AI market is expected to be big in homes, factories, and offices.

though, the information-technology industry will be satisfied with AI applications as long as they can meet short-term needs.

Even though research continues, it is now possible to accomplish this goal for narrow well-defined application areas, such as those addressed by knowledge-based systems and limited-domain natural-language systems (limited because they can understand only a subset of common words plus the subject's specific terminology).

Knowledge-based systems aim to solve real-world problems. Some examples are: a program called Mycin, which diagnoses blood diseases; XCON and XSEL, which Digital Equipment Corp. uses to provide instructions for computer-system configurations to manufacturing and to help customers configure systems; the Drilling Advisor produced by Teknowledge Inc., Palo Alto, Calif., for Elf-Acquitane, the French national oil company, to advise drilling supervisors on drill-stem sticking problems; and the Dip Meter Advisor, developed by multinational Schlumberger Ltd. for its own use in oil-well logging (dip meter) analysis.

About 50 knowledge-based systems have been built. Some are experimental, others are in use by the companies that built or commissioned them, and a few others are for sale. Many of these will be discussed in detail in Part 2 of this report. A sample of what is available for purchase includes Ada*Tutor (teaching the Ada programming language) from Computer*Thought Corp., Plano, Texas; the Symbolic Manipulation Program (solving mathematical expressions) from Inference Corp., Culver City, Calif.; and a trouble-shooting program for maintenance of diesel-electric locomotives from General Electric Co. Transportation Systems, Erie, Pa.

Natural-language systems provide an interface between a person and a complex computer program that lets the user work with the human language he or she normally writes and speaks. For example, several programs using natural-language techniqes have been developed to give computer users an easy-to-learn interface with data bases. The first real commercial AI application was such a natural-language interface with mainframe data-base–management systems. Called Intellect, it was developed by Artificial Intelligence Corp., Waltham, Mass., to help users specify queries to various DBMSs that run on IBM systems.

There are many definitions of artificial intelligence, though none is universally accepted. Definitions gleaned from several AI practitioners range from the abstract—like "the processing of symbolic information such as concepts, knowledge, and relations"—to the somewhat more deterministic, like "the study of techniques for solving exponentially hard problems in polynomial time." Perhaps the most comprehensive and easiest to understand is: "that part of computer science concerned with designing intelligent computer systems; that is, systems that exhibit the characteristics associated with intelligence in human behavior, such as understanding language, learning, reasoning, and solving problems."

Though the most commercialized AI applications to date are knowledge-based systems and natural-language interfaces, other application specialties to which AI is beginning to be applied include computer-aided design and engineering, intelligent robots, vision for robots, automatic programming, AI system development tools, and military applications crucial to national defense.

Although each specialization has its own practitioners with their own specific interests, research techniques, product development tools, and terminology, some of the more useful systems of the future are likely to combine the capabilities of two or more specialties. Common sense would suggest the combination of natural-language processing with knowledge-based systems, for example.

As is its nature, the science of artificial intelligence pushes the frontiers not only of software technology but also of software development methodologies. Some of the tools developed by researchers for their own work have become very important concepts applied to computing in general—ideas such as time-sharing, list processing, interactive editing and debugging, exploratory programming, graphics-oriented user interfaces, rich program-development environments, and even windows and mouse devices, all stem from AI work.

The popularity of Lisp, the traditional programming language of the U. S. AI community, is based on practical considerations stemming from the highly dynamic nature of AI techniques. Unlike typical number-crunching or text-processing applications, where the structure of the data is known *a priori*, AI programs are forced to deal with data structures—and even executable procedures—whose size and composition are developed as the program executes. Lisp, which stands for LISt Processing language, was designed to manipulate linked lists of objects.

With the acceptance of the programming language, Prolog, by Japan's fifth-generation computer project, however, Lisp may soon not be alone as the *de facto* language for AI development. Prolog—for PROgramming in LOGic—allows programmers to deal directly with logical associations between objects by defining a set of rules that a program can apply to meet its goals.

From the point of view of the program developer, though, language and hardware advances take second place to new program-development environments that ease the creation of software. Some of these systems even go so far as to provide the fundamental mechanisms needed in knowledge-based systems. They may even provide the fundamental hierarchical data structures and search algorithms used in knowledge engineering. Consequently, the creation of programs using AI technology becomes possible for computer scientists who have not been trained in the particulars of AI.

Worldwide strategy

The first AI products are harbingers of an evolution to a new generation of computer hardware and software. Major players in the international computer industry have recognized the strategic importance of AI and are already deeply involved. The Japanese government and the country's major computer companies and universities are about two years into the 10-year fifth-generation computer project.

This massive national project has several objectives and parts, including the development of number-crunching supercomputers, improved conventional business data-processing computers, and advanced process-control and robot systems. But its most ambitious goal is to produce a whole new family of thinking computers with knowledge bases and powerful inference engines (hardware and software that draws conclusions using rules of inference and facts from the knowledge base).

Western Europe has several projects in various stages of implementation and planning. In the UK, a fifth-generation computer project, called Alvey, is under way [*Electronics*, May 31, 1983, p. 101]. In 1984, a research institute devoted to artificial intelligence gets off the ground. Called the Turing Institute, in honor of British mathematician and computer theoretician Alan Turing, it is to be set up in collaboration with the University of Strathclyde, with sponsorship from industry. Industrial sponsors for the first year include, for example, ICL plc, Sinclair Research, Thorn-EMI, two Shell Oil Co. research laboratories, and two government agencies. The institute will concentrate on fundamental research in computer architecture, automatic programming, knowledge-based systems, and advanced robotics.

In France, Paris-based Schlumberger has made the largest commitment to AI of any company in the country. Its several large research labs include the Fairchild Research Laboratory in Palo Alto, Calif., and Schlumberger-Doll Research in Ridgefield, Conn. The company also has a major equity position in Bolt, Beranek, & Newman Inc., a Cambridge, Mass., research firm with a strong AI capability.

The European Commission has its Esprit project [*Electronics*, May 19, 1983, p. 75], while the three largest European computer companies—France's Compagnie Machines Bull, Britain's ICL, and West Germany's Siemens AG—have formed a joint research institute for knowledge processing. AI research is also conducted in the USSR and East European countries—Hungary even exports an AI programming language [*Electronics*, Oct. 6, 1983, p. 110].

In the U. S., major corporations with large commitments to AI research and development include International Business Machines Corp., Armonk, N. Y.; AT&T Bell Laboratories, Murray Hill, N. J.; Xerox Corp., Palo Alto, Calif.; Digital Equipment Corp., Maynard, Mass.; and Hewlett-Packard Co., Palo Alto, Calif. In addition, there are many small and start-up companies whose business is AI. □

THE ARTIFICIAL INTELLIGENCE MARKET

Product category	Market estimate ($ millions)							
	1983	1984	1985	1986	1987	1988	1989	1990
Knowledge systems	10	16	25	40	60	90	145	220
Natural-language software	18	32	60	105	190	335	600	1,090
Computer-aided instruction	7	11	15	20	30	45	70	100
Visual recognition	30	55	100	150	230	360	555	860
Voice recognition	10	14	20	30	50	80	130	230
Total	75	128	220	345	560	910	1,500	2,500

SOURCE: DM DATA INC.

A 'new' technology goes back 27 years

Artificial intelligence was a name chosen for the efforts under way in making machines think and learn at the time the discipline was formally established. The term was invented by John McCarthy, then assistant professor of mathematics at Dartmouth College in Hanover, N. H., for a conference he helped to convene there in 1956. There were few workers in the field, and they were mainly looking for ways in which machines could be induced to mimic brain processes. The name was meant to describe this goal.

The Dartmouth conference represented the beginning of AI as a separate aspect of computer science. McCarthy's purpose in organizing the two-month forum was to bring together all of the then-serious researchers in the field and open channels of communication among them.

One of the surprises at the meeting was the presentation of some work that had been done at Carnegie Institute of Technology in Pittsburgh (now Carnegie-Mellon University) by Allen Newell and Herbert A. Simon. They described their theorem-proving Logic Theorist, the first program to use a computer as a symbolic processor, not a number cruncher, and also the first working AI program. In collaboration with J. C. (Cliff) Shaw of the Rand Corp. of Santa Monica, Calif., Newell and Simon had created a computer language capable of modelling some simple human problem-solving capabilities, and they used it to build the Logic Theorist. This language, called Information Processing Language (IPL), was the first to give a computer the power to process concepts rather than numbers—the first symbolic processing and a major stride toward automating cognitive thought.

Also among the invitees was Marvin Minsky of the Massachusetts Institute of Technology, Cambridge, who had worked with Claude Shannon at Bell Laboratories. The work of these pioneers has stimulated AI development ever since. Minsky directed AI programs under MIT's Project MAC and has written extensively on heuristic programming. McCarthy is the creator of Lisp (until now the favored AI programming language), director of the AI lab at Stanford University, Palo Alto, Calif., and the crusty *éminence grise* of the discipline. Newell and Simon have made Carnegie-Mellon into a leading U. S. center of basic across-the-board AI research, of work on specific knowledge-based applications and tools for building them, and of work on understanding natural-language applications.

AI work during the 1970s included development at Stanford under Edward Feigenbaum of the first expert system, a chemist's assistant called Dendral, to analyze mass spectrography. At Xerox Corp.'s Palo Alto, Calif., Research Center, work was done on enhancing Lisp, developing programming tools and an interactive programming environment around Lisp, and creating Lisp work stations with convenient graphics-based user interfaces. At SRI International, Menlo Park, Calif., still more knowledge-based systems were developed. Another Stanford professor, Terry Winograd, developed a program to manipulate a simulated environment consisting of objects shaped like wooden blocks. His program, Shrdlu, could be told about the blocks and instructed to rearrange them.

The kind of engineering that turns up in commercial products like expert systems derives from a significant change that has taken place in AI since 1956: turning attention to specific problems. Early research looked for general problem-solving solutions but floundered on the problem of combinatorial explosion, the fact that exhaustive searches of a problem domain were quickly mired in possible paths whose branches grew exponentially. People, on the other hand, tend to use their accumulated knowledge of

Allen Newell
Carnegie-Mellon University

John McCarthy
Stanford University

Marvin Minsky
Massachusetts Institute of Technology

the world and their particular experience to solve problems rather than trying all possible alternatives. AI researchers came to feel that perhaps computers could be programmed to do the same. The early work also revealed vast gaps in human understanding of how to conceive of and represent thinking and learning; and AI research eventually turned to simpler functions, such as investigating how to represent knowledge and make inferences from it.

Though the early AI research was distinctly a U. S. endeavor, it started spreading to other countries quite early. Now much of the research is being done in France, Britain, Japan, Hungary, and the USSR. The Japanese, for example, are relying on AI very heavily in their massive 10-year national project to develop fifth-generation computer systems. Also in recent years, AI scientists were hired by commercial companies such as the French-based Schlumberger Ltd., Hewlett-Packard Co., Digital Equipment Corp., Tektronix Inc., Fujitsu Ltd., Hitachi Ltd., NEC Corp., and International Business Machines Corp., to set up industrial AI research labs. This development pleases the AI community because it indicates that its work is recognized as valuable, but also worries it because of the possible effect of a commercial brain drain on research.

Over the years, a consistent source of U. S. AI research funding has been the military, which has supported it ever since the failure of early attempts at machine translation of foreign languages led the Department of Defense to sponsor Noam Chomsky's research into structural linguistics. DOD still has an extensive AI research program administered by the Defense Advanced Research Projects Agency.

Darpa, then called ARPA, was the major source of financial support of U. S. AI research during the 1960s and the early 1970s. It concentrated its resources and thus enriched the four main early AI research centers: Carnegie-Mellon, MIT, Stanford, and SRI International. Now it seems that Darpa is getting ready to put big money into a grab bag of R&D covering supercomputer architecture, AI, and software. There is $50 million in the 1984 budget for this recently set up program, and the agency is asking for $95 million for 1985. It is estimated that the project could ultimately cost $500 million to $750 million.

Douglas B. Lenat, of Stanford's Heuristic Programming Project, suggests that AI is splitting into science and engineering arms, and that the latter feeds on the now considerable base of AI research. But Marvin Minsky feels that research has not yet reached the stage where it can be profitably mined for products, although he, too, is now part of a start-up AI company: International Thinking Machines Inc., in Waltham, Mass. That effort, he says, awaits the development of systems with common sense, as well as the ability to make logical inferences.

As an emerging discipline, artificial intelligence provoked two serious challenges: first that what it purported to do was impossible—that machines could not think in any meaningful definition of the term—and, second, that even if it was possible, it would be dangerous, for teaching a machine to think would somehow diminish the worth of humans.

The first objection weakened when AI researchers stopped trying to make machines think and settled for machines that drew inferences from data. The question is coming back in a new guise, however; Minsky and Douglas Hofstader, author of a Pulitzer-prizewinning AI bestseller, "Gödel, Escher, Bach: An Eternal Golden Braid," insist that AI progress can only continue when researchers seriously consider the implications of machine awareness, however that may be represented. **—Clifford Barney**

Herbert Simon
Carnegie-Mellon University

Edward Feigenbaum
Stanford University

ARTIFICIAL INTELLIGENCE

Lisp and Prolog machines are proliferating

New U. S Lisp machines are announced, as Japan investigates Prolog and Lisp

by Tom Manuel, *Senior Editor, Information Systems*

What follows is part 1 of a two-part series on the commercial status of artificial intelligence. Part 1 delves into AI hardware systems now available, as well as reporting on several product-development projects close to fruition around the world. Prominent among the latter are projects under way in Japan, reported here in detail for the first time. These projects stem both from the fifth-generation computer project and from investigations into artificial intelligence.

Part 2 of the series, which will appear in the Dec. 1 issue, will be a close-up look at the software side of AI. Subjects to be covered will include AI programming languages, application development tools, and existing applications of knowledge-based (expert) systems and of natural-language processing.

The primary hardware tools available now for sculpting artificial-intelligence systems are computers designed to work with fast high-resolution graphics-programming work stations in order to optimize symbolic processing—the processing of the symbols standing for mental concepts, as opposed to numerical processing. The first of these computers were called Lisp machines because they were designed for efficient runnning of Lisp, the first and currently most popular language for AI work. Lisp was designed to easily write programs for the symbolic representation and processing of arbitrary objects and the relationships among them. The hardware tools of the AI trade available today are personal Lisp machines from three U. S. manufacturers, as well as emerging general-purpose work stations and a few mainframe computers, all with AI language support.

Advantages of the Lisp machines are the speed and efficiency gained from the fact that they are designed and tuned for symbolic processing. These work stations typically have large memories and virtual-memory management, plus advanced graphics. General-purpose work stations are not tuned for symbolic languages, but they have all the other advantages of the Lisp machines. Also, they can easily handle non-AI applications, such as the numerical calculations required in computer-aided engineering. Of course, the Lisp machines can be used for non-AI applications, too, and they are excellent programming development tools for all types of software. A couple of advantages of mainframe computers for AI work are, first, a company may already have them, and, second, AI applications developed for them can be integrated with other programs running on them.

Before Lisp machines came along, AI work was done on time-shared mainframe computers, primarily the DECsystem 10s and 20s, made by Digital Equipment Corp., Maynard, Mass. These machines are still in use for AI work, as are time-shared superminicomputers such as DEC's VAX-11 series. However, Digital has discontinued its project to build the successor to the DECsystem 20. Instead, it is concentrating its AI effort on its VAX superminicomputer line and specialized work stations.

From PARC and MIT

The earliest Lisp machines were designed at two research labs: the Laboratory for Computer Science at the Massachusetts Institute of Technology, in Cambridge, and Xerox Corp.'s Palo Alto (Calif.) Research Laboratory. In 1981 Xerox announced an Interlisp work station, the 1100. (Interlisp, one of the several dialects of Lisp, grew out of the original.) The 1100 was the first of a series—two other members are now available, the 1108 and the 1132 (see p. 153) Xerox plans to extend the 1100 series at both ends. At the low end will be a very low-cost work station with enough memory to execute a run-time version of Interlisp-D, which is the company's version of Interlisp. This computer would only run AI applications; it could not be used to develop them.

The entire 1100 series is compatible with Ethernet and the Xerox Network System architecture, and therefore customers can configure these work stations into systems with other XNS products, such as file, print and communications servers. The series is sold in Japan by Fuji Xerox and in Western Europe by Rank Xerox, while a similar machine is sold by Siemens in West Germany.

Another U. S. maker of personal symbolic computers is Symbolics Inc. in Cambridge, Mass. Formed in 1980 to commercialize symbolic-computing technology, the company was founded by members of the team that developed the MIT Lisp Machine and its operating system. Like Xerox, Symbolics introduced its first computer in 1981, the LM-2 being a commercial version of the MIT Lisp Machine [*Electronics*, Aug. 11, 1981, p. 159]. No sooner was this machine in production than Symbolics introduced its successor, the 3600 [*Electronics*, Aug. 25, 1981, p. 40]. This machine (Fig. 1), two to eight times more powerful than the LM-2, went into production in early 1983.

The third U. S. maker of Lisp machines is called, appropriately, Lisp Machine Inc., Culver City, Calif. It also shipped its first machine in 1981, the Series III CADR (CADR is a Lisp function that creates a new list starting at the second member of a previous list, and this was the second Lisp machine to be built). Lisp Machine's next-generation product is the Lambda [*Electronics*, Sept. 8, 1983, p. 196]. Like the Symbolics 3600, the Lambda (Fig. 2) comes with Ethernet capability.

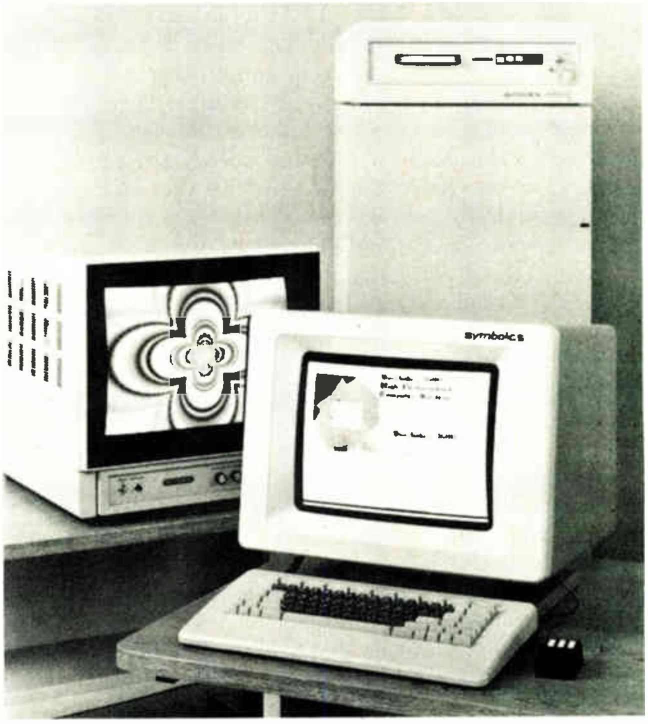
The first practical Lisp machine made in Japan came from Fujitsu Ltd. [*Electronics*, March 24, 1983, p. 71]. The Alpha machine (Fig. 3) is a prototype back-end Lisp processor for a general-purpose computer. The company claims it will be the fastest Lisp machine around at 2.5 million to 3 million instructions a second when running simple programs. Lisp is also available on NEC Corp.'s ACOS series of mainframe computers.

Because AI machines are just starting to appear, no generally accepted set of benchmark programs for measuring and comparing their performance has been developed. Moreover, comparing machine-level rates in millions of instructions per second is misleading when evaluating high-level–language machines.

Performance numbers quoted in MIPS should only be used as broad guidelines, for the prospective buyer and user of these machines must consider many other features, particularly the set of software development tools offered and the particular dialect of Lisp available. Also to be taken into account are the availability of other programming languages, system reliability, and the level of hardware and software maintenance support being offered.

A comparison

To summarize the main features of the machines now available, the Xerox 1100 series has different models with a wide range of performance choices; Interlisp-D; Smalltalk-80, an object-oriented language; Loops, a programming tool that integrates four programming environments [*Electronics*, Sept. 8, 1983, p. 196]; and a well-tested network and server support system. The Symbolics 3600 has high performance; a very rich software development environment; Zetalisp, a derivative of Maclisp, which in turn is another dialect of Lisp; Flavors, an object-oriented language; Fortran-77; and Ethernet.



1. Symbol processor. The model 3600 computer from Symbolics Inc. is one of the class of systems commonly known as Lisp work stations. Designed for fast symbolic processing in Lisp, it is dedicated to a single user and features an interactive-graphics user interface.

The newest work station, Lisp Machine's Lambda also is fast. It has LMLisp, another child of Maclisp, with software development tools; a Lisp microcompiler and virtual control memory for easier tailoring of the machine intruction set; an optional MC68000 processor for running Berkeley Unix, C, Pascal, and Fortran-77; an 8088-based system diagnostic processor; and Ethernet facilities. DEC's VAX systems come in a wide performance range, from the new MicroVAX [*Electronics*, Oct. 20, 1983, p. 42] to clusters of 11/782s [*Electronics*, Oct. 20, 1983, p. 143]. They run much software, including several dialects of Lisp and a new Common Lisp, and offer Ethernet and DECnet. The 68000-based VAXstation 100 work station at $13,000 ($10,000 for the hardware and $3,000 for the software) adds the same kind of graphics-based user interface that the Lisp machines have.

General-purpose high-end work stations—typically based on multiple 68000 processors and offering the Unix operating system, virtual-memory management, large real memory, and advanced graphics-based user interfaces—could join Lisp machines and mainframes as hardware tools for AI development. One dialect of Lisp, Franz Lisp, developed at the University of California at Berkeley, is written in C and runs under Unix and presumably could be made available on the general-purpose work stations.

The AI machines on the market may come from the U. S., but Japan is investing much research and development effort in the field. The work there is both an investigation of artificial intelligence *per se* and also that included in the fifth-generation computer project.

The Japanese government's Electrotechnical Laboratory in Ibaraki has completed fabrication of a personal Lisp machine of roughly the same speed as the Symbolics 3600. If the software were refined by the addition of a full-fledged editor and command system it could be used for practical applications. The system has as its main processor the Pulce silicon-on-sapphire processor completed by Toshiba Corp. in 1978 as part of the government's pattern-information-processing project.

However, the single-processor machine is but the first step in the development of a data-driven Lisp machine named EM-3 for office automation, natural-language processing, knowledge-based systems, and other interactive applications. Yoshinori Yamaguchi, a senior researcher at the Ibaraki ETL, says that work is progressing on a parallel-processor hardware simulator using eight single-board 68000 processors.

In its final form, this system will have 80 to 100 very large-scale integrated processors of a yet-unknown type that the ETL researchers hope to design themselves. It may have to be made with gate arrays because silicon foundries are not readily available in Japan. Present plans call for the hardware simulator to be completed by the end of March 1984.

Key to the new machine, though, is the control mechanism, which will be developed during a one-year feasibility study starting next April. It is expected to be an advanced parallel-control mechanism that will be a natural extension of the data-driven scheme for function evaluation used in data-flow computers.

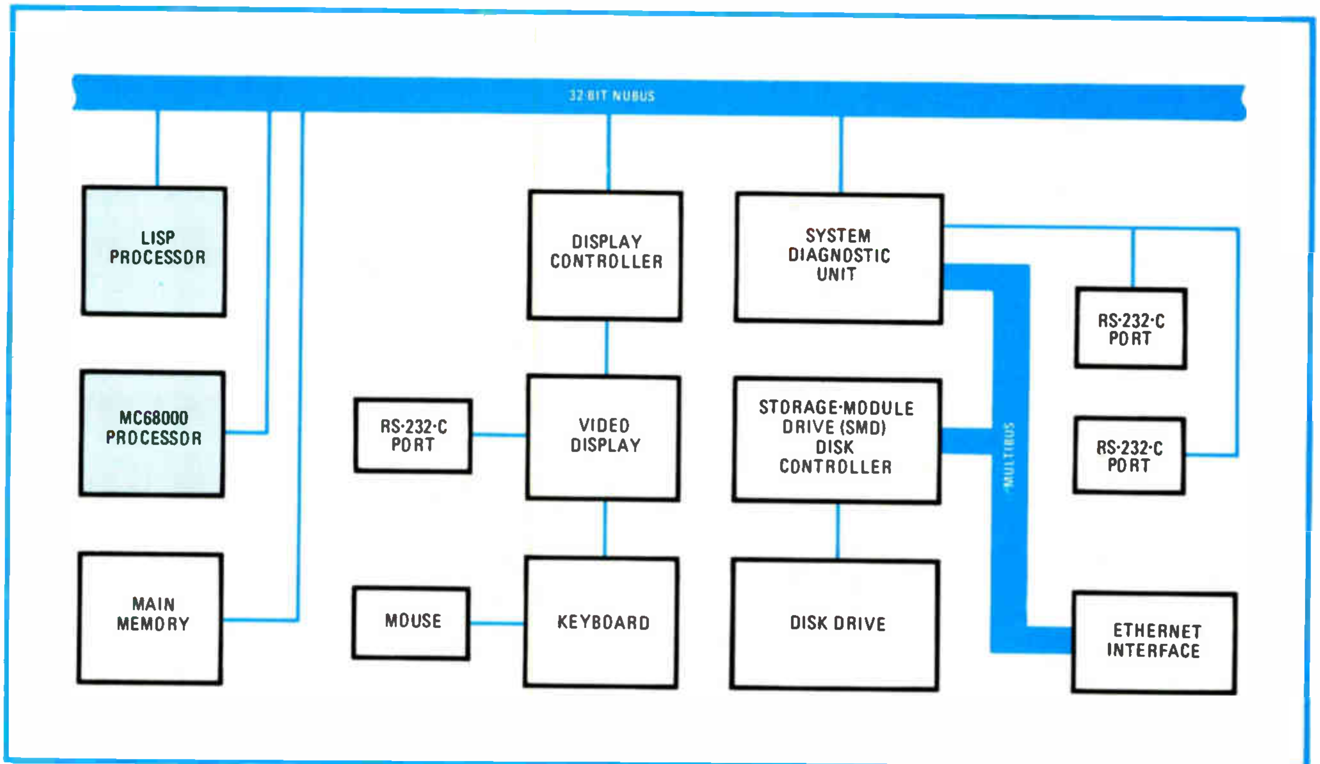
The primary programming language will probably be a Lisp-like language with Prolog features such as pattern invocation and backtracking, although Prolog is also being studied for possible use. Pattern matching also will be required in the language.

Beyond Lisp

Meanwhile, a group headed by Yasushi Hibino at the Nippon Telegraph & Telephone Public Corp.'s Musashino Electrical Communication Laboratory is building a Lisp machine that it expects to complete by the end of March. Multiple copies will be built for AI research.

The machine is being created as part of the so-called NUE project. NUE is the Japanese equivalent of the Chimera of Greek mythology, and the name is intended to indicate that the project is not language-restricted. It started off two years ago as a Lisp project, but it has now become a multilanguage project where procedural, functional, logical, and object-oriented languages will be developed with the syntax of Lisp but the semantics of other languages, including Lisp, Prolog, and Smalltalk.

The reasoning behind the NUE work is that AI problems cannot be solved with one programming style. Ideally, the execution system should work with the same efficiency for any style because the computational volume



2. Lisp and more. The flexible, modular Nu Machine and Nubus architecture of this Lambda computer from Lisp Machine Inc. accommodates different processor types for different applications, such as a Lisp processor and an MC68000 in the same machine.

should be the same, but the programs will be easy or hard to write depending on the problem. With NUE, it should be possible to learn which styles are superior for which problems.

The name of the NUE machine is ELIS, from Electrical Communication Laboratory Lisp processor. Its speed in the interpreter mode is similar to that of Fujitsu's Alpha. Like experimental Lisp machines previously built in Japan, his machine makes use of microprogramming, he notes. ELIS has a 32-bit bus, using 24 bits for address and the remaining 8 bits as a tag. The address space is equivalent to a 27-bit address, because each address accesses an 8-byte cell, so a total of 128 megabytes can be addressed rather than the 16 megabytes that conventional 24-bit addresses can access.

Watch the pointers

Hibino says this configuration was selected because it provides the best performance: in Lisp, following the path of the pointers is more important than computation, so having two large pointer fields to the CAR and CDR instructions speeds up this operation. It could be considered extravagant, but, even when data is missing, memory usage is only double that of systems designed to conserve memory. Hibino also notes that memory conservation is no longer a primary concern, with 256-K chips permitting 4 megabytes of memory on a single board.

The processor has about half of its logic implemented in AMD2903 bit-slice chips and the remainder in Schottky TTL. The 2903 is not ideal for the application because of the vertical connections between the arithmetic and logic unit and the shifter. The vertical connections are superior in arithmetic operations such as add and multiply where shifting is part of the operation because it enables these operations to be performed in one clock cycle instead of two. But they slow down symbolic processing. However, the standard functions of the 2903 arithmetic and logic unit speed up standard data processing more than they degrade symbolic processing.

The ELIS hardware is in operation and the microprogram is working sufficiently well to measure performance. The firmware should be sufficiently refined that the system can be in use at the Musashino lab by April 1984, if the system software has been completed by that time. Hibino is not as yet able to say how many machines will be built or to disclose much else about future plans.

The first project in the Japanese fifth-generation computer effort is a personal sequential-inference (PSI) computer for developing knowledge-processing software [*Electronics*, July 28, 1983, p. 101]. The PSI is intended for developing inferential symbolic processing programs at the Institute for New Generation Computer Technology (ICOT) and will have a sequential von Neumann architecture rather than the advanced parallel architectures planned for the eventual fifth-generation computers.

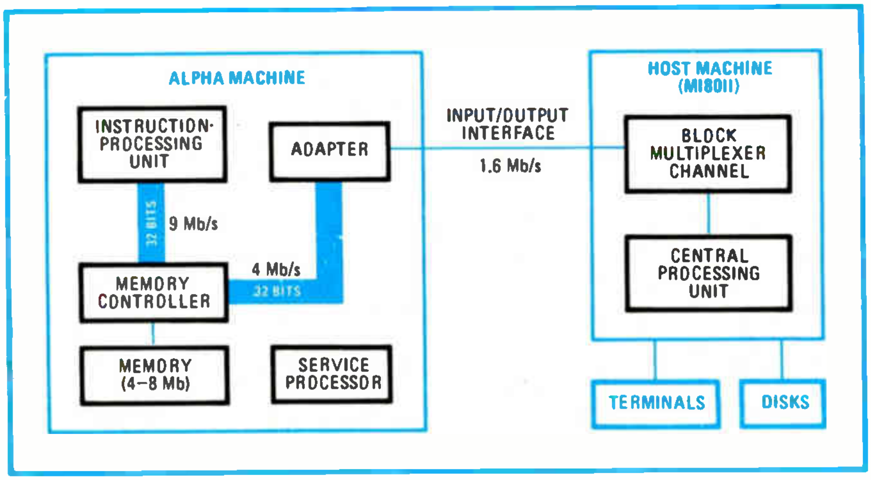
A cooperative effort

ICOT's functions are to design the hardware and software for fifth-generation subsystems and to build the software. The hardware production is being contracted out to computer companies. For example, the pilot model of the PSI (Fig. 4), is being fabricated by Mitsubishi Electric Corp. and Oki Electric Industry Co. Ltd. for evaluation by August 1984 and is to be made from conventional components. A later version will be made with custom VLSI circuitry.

Other ICOT-designed subsystems for the fifth-generation project will be manufactured by various Japanese computer companies. For example, NEC will fabricate a sequential-inference machine faster and larger than the PSI and scheduled for completion within the initial three-year phase of the project.

Also part of Phase One is a general-purpose parallel computer for maintaining and processing knowledge bases and relational data bases. Toshiba will build the basic engine for it, possibly using some very high-speed SOS technology. Hitachi Ltd. will be building a hierarchical memory subsystem—a memory that is organized as a hierarchy and is addressed by subject content at the appropriate level of the hierarchy—and a silicon disk to hold it (Fig. 5). NEC, Hitachi, and Fujitsu are expected to manufacture the parallel inference and knowledge-base machines that will be built during the second, or intermediate, phase of ICOT's fifth-generation project.

One of ICOT's software projects for the PSI is an enhanced version of Prolog. The PSI is being designed to optimize Prolog performance at no less than 20 klips—a fifth-generation performance term meaning a thousand



3. Symbolic helper. Fujitsu's Alpha is a back-end processor that provides users on a time-sharing computer with high-speed symbolic list processing. Connected to a Fujitsu mainframe, its instruction-processing unit executes the Utilisp variant of Lisp.

logical inferences per second. Lips is just a fancy term for the number of Prolog procedure calls per second. Since one procedure call averages from 100 to 300 machine instructions, 1 klips is roughly equivalent to 0.1 to 0.3 MIPS, thus giving the PSI raw instruction performance of 2 to 6 MIPS that is superior to the fastest Lisp machines currently available. This comparison, of course, must be taken with a grain of salt. It can only give a ballpark guess as to how the PSI will perform relative to the Lisp machines, because it is of little value to compare a Lisp procedure to a Prolog inference.

An inference machine

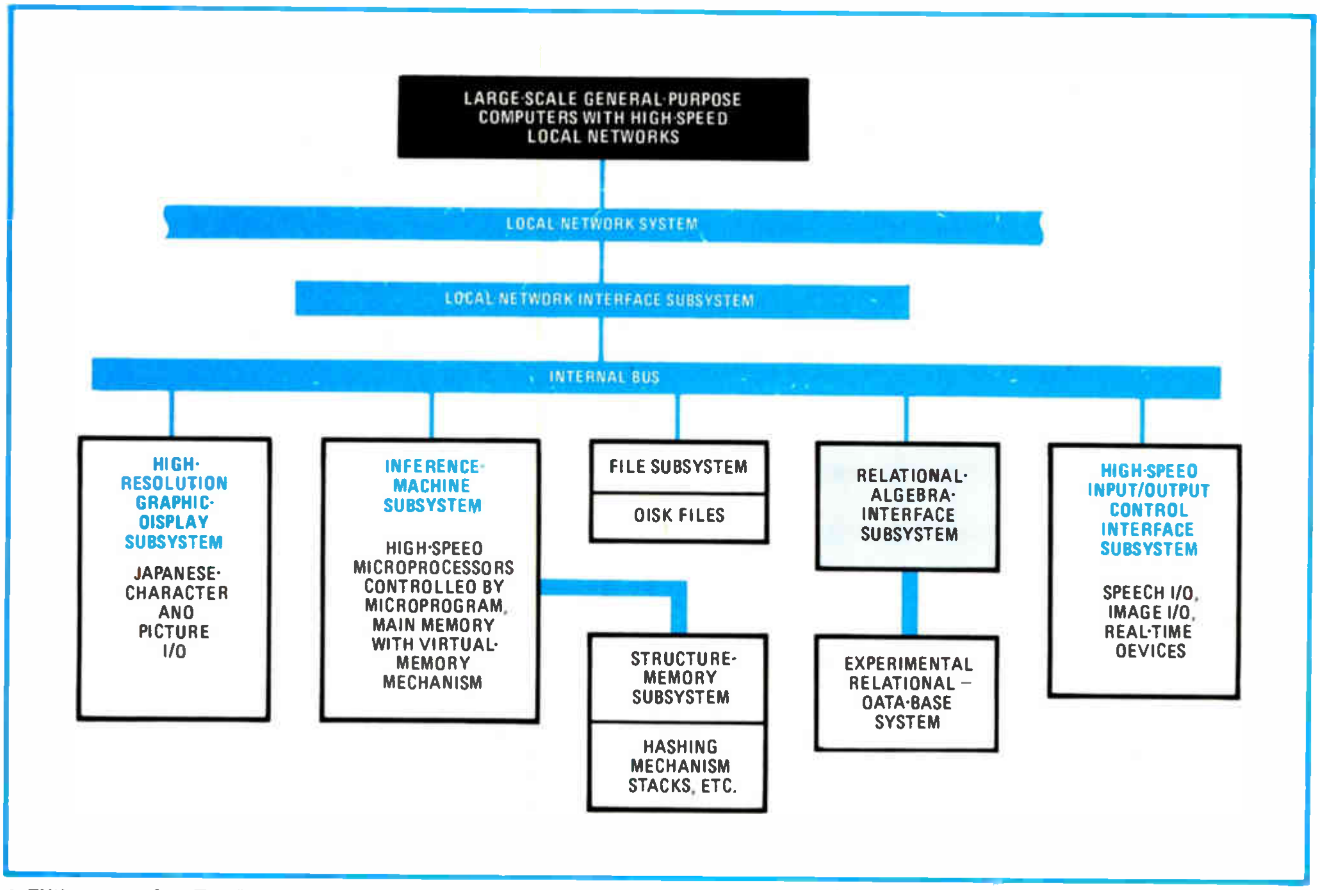
Meanwhile, at the University of Tokyo, Tohru Moto-Oka and a group of his graduate students are developing a parallel inference engine for a Prolog machine. An inference engine is a hardware system for reaching conclusions from facts and rules of inference stored in a knowledge base. This work is in cooperation with ICOT but receives some other funding and represents one of the several approaches—some not yet publicly revealed—toward development of fifth-generation architectures. In some ways, this work is the most advanced sector of ICOT's project because it will immediately jump into parallel processing, while ICOT is starting with a personal sequential-inference machine. The group intends to build a system with 100 parallel high-speed processors, with the first usable system being completed in 10 years.

A simulator written in C has been completed, and the design of the core of the TTL hardware simulator will be completed by the end of this month. The first processor will be finished several months later, and by the end of March 1984, it should be in operation. Within two years after that, the group plan to build a 10-processor system and go on from there.

The Eddy data-flow processor being developed at the Musashino lab [*Electronics*, June 16, 1983, p. 114] will also be a type of Lisp machine. Extensions to Valid, the high-level functional language with recursion and parallel expressions for logic programming developed for this machine, will also make it a type of Prolog machine. The extensions will include pattern matching, making Valid suitable for simple, intuitive programming.

The present basic research phase at the Musashino lab will continue for another two or three years. If the work is continued to completion, a system suitable for user applications should be completed in seven to 10 years. This is roughly the same time scale as the ICOT project, for which this work provides an alternative.

Many observers note that the potential resources of the



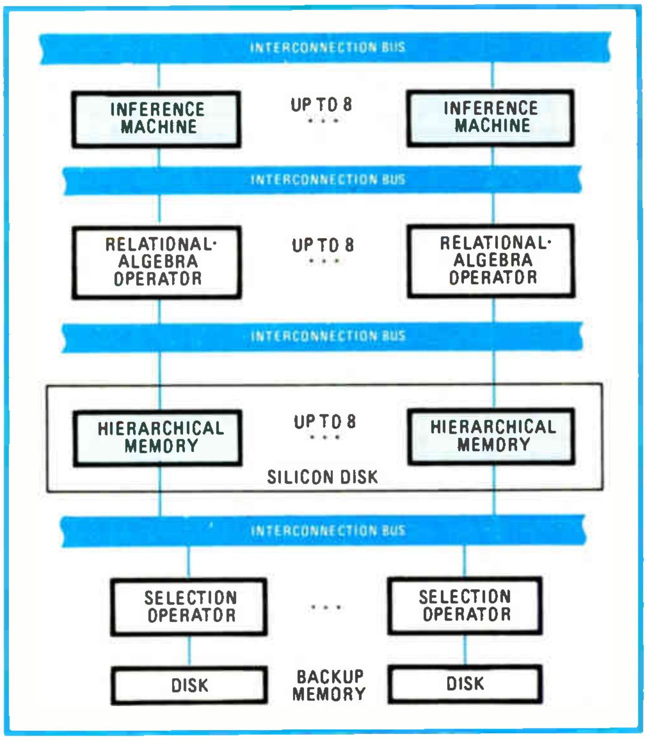
4. Fifth generation. The first Japanese fifth-generation prototype is this personal sequential-inference machine being developed by ICOT. Two major innovations are the inference machine and relational algebra subsystems. Software for the PSI represents the biggest effort.

four NTT Electrical Communication Laboratories—the Musashino ECL, the Ibaraki ECL, the Yokosuka ECL, and the Atsugi ECL—exceed by far those of ICOT. This is true even considering only the personnel and budget available for computer R&D, although the ECLs also have capabilities in semiconductor work and related fields. But the NTT labs each have many projects going, and there is no guarantee that management will continue work on all of them through to fruition at a high level.

Another major center of AI research is the UK, where work is under way on several flavors of Prolog machines. At the low end, there is a version of Prolog for Z80-based CP/M personal computers from Logic Programming Associates of London. It is intended for teaching basic Prolog and not for developing or running logic application programs.

Alice lives here

At the high end, a computer called Alice, for applicative language idealised computing engine, is being developed in a research project at London's Imperial College [*Electronics*, Feb. 24, 1983, p. 67]. It will be a parallel-processing machine designed for Parlog, a parallel version of Prolog, Lisp, and the college's own declarative fifth-generation language, Hope. Parallel architectures for nonprocedural languages like Prolog and Hope make sense because all the premises that might lead to a conclusion in logic could be evaluated at the same time.



5. Hierarchical memory. A parallel relational-data-base machine using specially designed hierarchical memory on a silicon disk (fast semiconductor memory used like a disk drive) with a disk-drive backup is also part of Phase One of Japan's fifth-generation project.

The Alice prototype will have 16 processors and 16 memory modules and a switch to connect any processor with any memory. The basic engine will be the transputer microprocessor chip from Inmos plc [*Electronics*, Sept. 22, 1982, p. 86], with 112 of them being used. Both hardware and software development are on schedule for completion by early 1985.

Hardware development is split into two parts: the communications ring carrying data packets, and the processing agents, each with multiple transputers. The communications ring is scheduled for completion in May 1984. A key element is a high-speed monolithic switch being built for Imperial College by Swindon Silicon Systems. The research group has been promised first samples as a Christmas present. From that point onwards, further progress will hang on the availability of transputer chips, which are just being formally unveiled (see p. 47).

For those seeking to experiment with Prolog programming, there are several options. Prolog versions are available from several sources for machines as diverse as Z80- and 68000-based microcomputers, PDP-11s, DEC20s, and VAX machines. There is even a version for the IBM/370 architecture available from the computer science department of Waterloo University, Waterloo, Ontario, Canada. And a new company, Silogic Inc. in Los Angeles, is now offering Prolog interpreters for a variety of machines, including the Z80 and MC68000 microprocessors, and is currently developing a Prolog compiler.

However, only the Japanese PSI computer is designed to be a Prolog-optimized machine the way the Lisp machines are for Lisp. There is the likelihood that efficient implementations of Prolog will soon become available on the U. S. Lisp machines. They may even outperform the PSI prototype and be available on the open market before it is running.

For instance, a version of Prolog from the University of Uppsala in Sweden is available now for Lisp Machine's Lambda. It is expected to deliver 4.5 klips initially and up to 20 to 25 klips when it is optimized with microcode. As for the 3600, Symbolics says that it is considering two strategies for Prolog: to provide it just as it would provide another language, such as Fortran, or to put the interesting aspects of Prolog into Zetalisp or to develop a Prolog with Lisp syntax.

Advanced, high-performance parallel AI architectures are being researched in the U. S. For example, at MIT, Robert H. Halstead Jr. leads a group that is constructing an experimental multiprocessor called Concert, which will combine 32 68000 processors. As one of its languages, it will run Multilisp, a multiprocessor version of Lisp that is being developed as part of the project. Another MIT project, funded by the Defense Advanced Research Projects Agency, plans to build a 64-processor machine using Symbolics 3600s. □

Additional reporting came from Charles L. Cohen, Tokyo, and Kevin Smith, London.

Designer's casebook

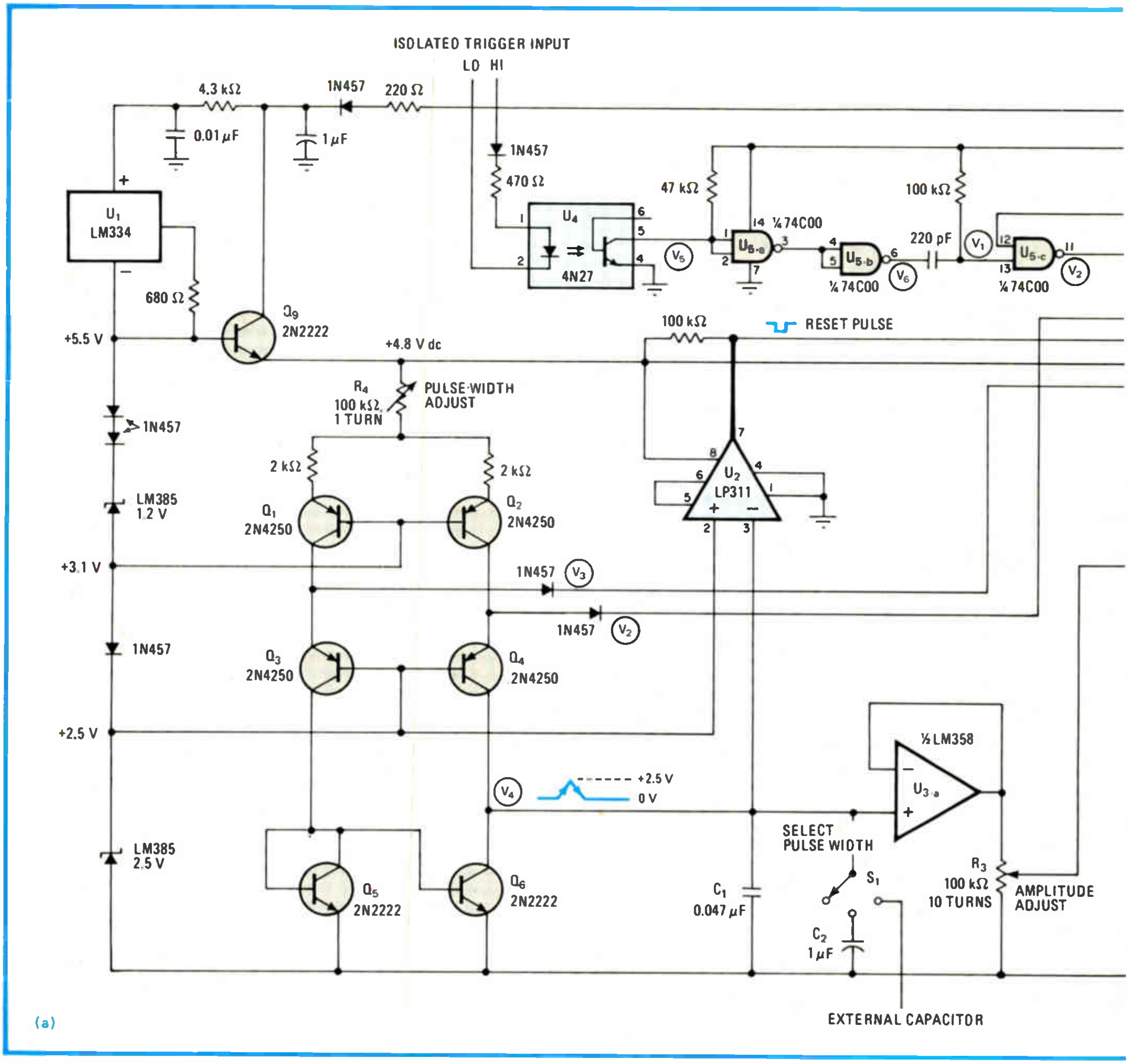
Triangle-wave current pulser is adjustable

by Robert A. Pease
National Semiconductor Corp., Santa Clara, Calif.

Useful for testing nonlinear devices, this versatile triangle-wave pulser provides up to 10 amperes of calibrated output, an adjustable pulse width, and a programmable repetition rate. Its duty cycle can be set as low as desired to prevent overheating at high current levels.

When the R-S flip-flop comprising NAND gates $U_{5\text{-}c}$ and $U_{5\text{-}d}$ is reset (a), V_3 is high, V_2 is low, and transistors Q_3, Q_5, and Q_6 are on. Applying a pulse of about 2 milliamperes to the optical coupler's trigger input causes output V_5 to go lower, which sets the R-S flip-flop. Transistors Q_3, Q_5, and Q_6 now turn off, and transistor Q_4 turns on and ramps up V_4 to the +2.5-volt level. U_2 detects this level and generates a pulse, which resets the flip-flop.

Next, transistor Q_6 turns on and V_4 ramps back lin-



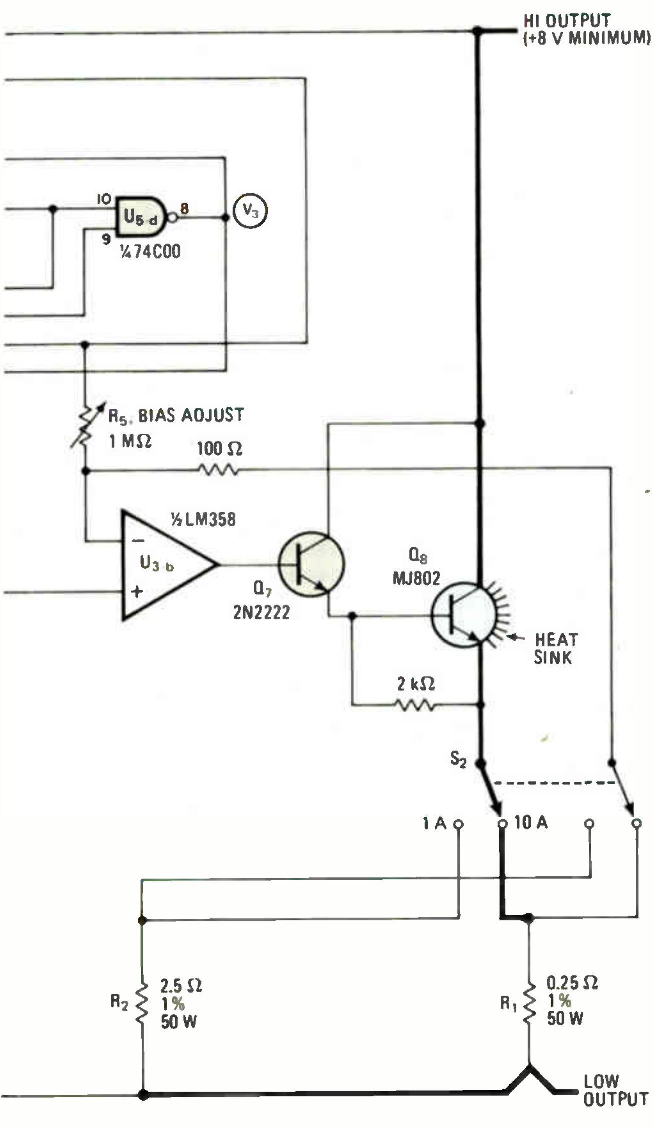
(a)

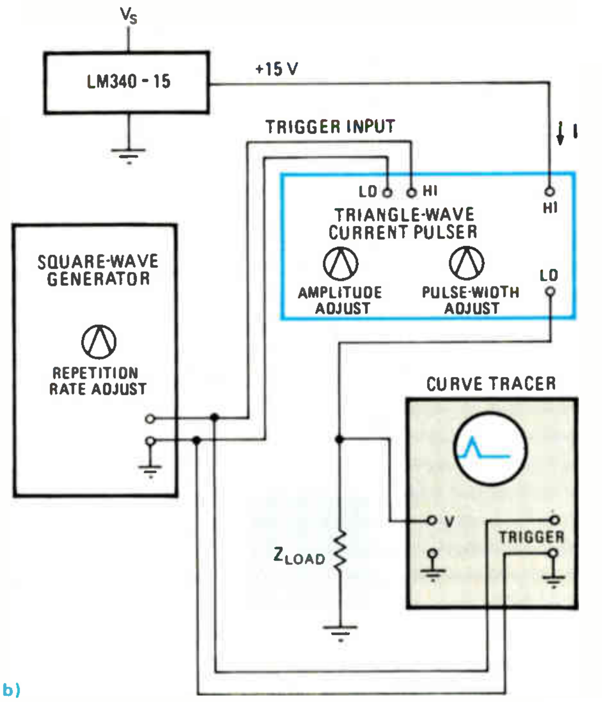
early to ground, generating a triangular waveform that drives transistors Q_7 and Q_8 via buffers U_{3-a} and U_{3-b}. This forces the transistors to put out a current that flows through R_1 as well as through the external load.

Though this circuit uses potentiometer R_4 to control the triangular wave's rise and fall rates, they can also be controlled independently by separate potentiometers. Calibrating the circuit is easy when it is connected to a curve tracer and triggered at about 29.5 hertz, using a pulse width of 2 milliseconds. When connected to the curve tracer, R_5 is trimmed for minimum quiescent current—typically 2 mA—and resistors R_1 and R_2 are trimmed to get the peak current indicated on the curve tracer to agree with the dial readings of the 10-turn potentiometer. Minimum output is about 8 V; however, higher voltages, such as 30 V, require a low duty cycle to prevent excessive heating at higher current levels.

A typical usage circuit (b) shows the pulser loading and testing a regulator's output. The pulser can force a calibrated current in Z_{load}, whether linear or nonlinear, active or passive, ohmic or reactive. □

Pulser. A versatile current pulser (a) provides a triangular waveform that has an adjustable pulse width and a programmable repetition rate. The pulse width is coarsely adjusted by S_1, while potentiometer R_4 provides fine tuning. For the components shown, the pulse width ranges from 0.5 ms to 1 second. S_2 selects the output-current amplitude of 1 ampere or 10 A. A typical test circuit is shown in (b). The load may be linear or nonlinear, active or passive, ohmic or reactive.





(b)

Sample-and-hold yields variable-reference rectifier

by J. Millar and T. G. Barnett, *Department of Physiology, The London Hospital Medical College, London, England*

Unlike conventional half-wave rectifiers, this circuit uses a high–slew-rate operational amplifier and a sample-and-hold integrated circuit to provide a low-noise half-wave rectifier that rectifies about any given reference level. In addition, the circuit can rectify low-amplitude signals and has a wide frequency response.

Input is fed in parallel to comparator U_2 and sample-and-hold amplifier U_3 by buffer U_{1-a}. The reference voltage, derived from the voltage divider and buffer U_{1-b}, is set on the comparator's noninverting input port. When the signal becomes more positive than the reference, the

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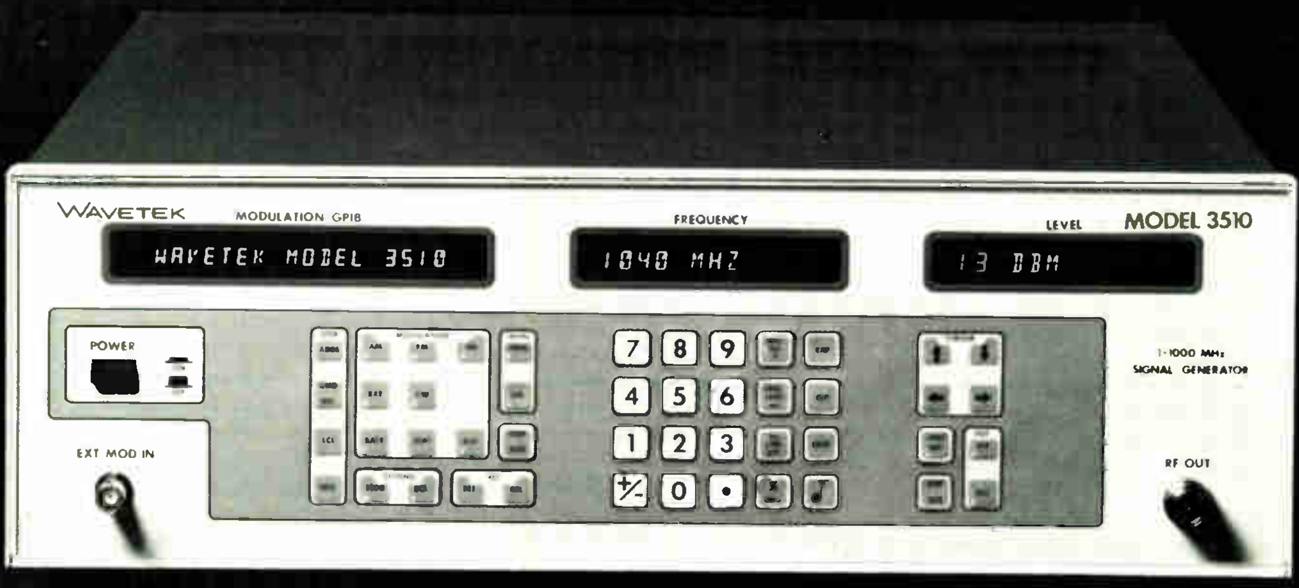

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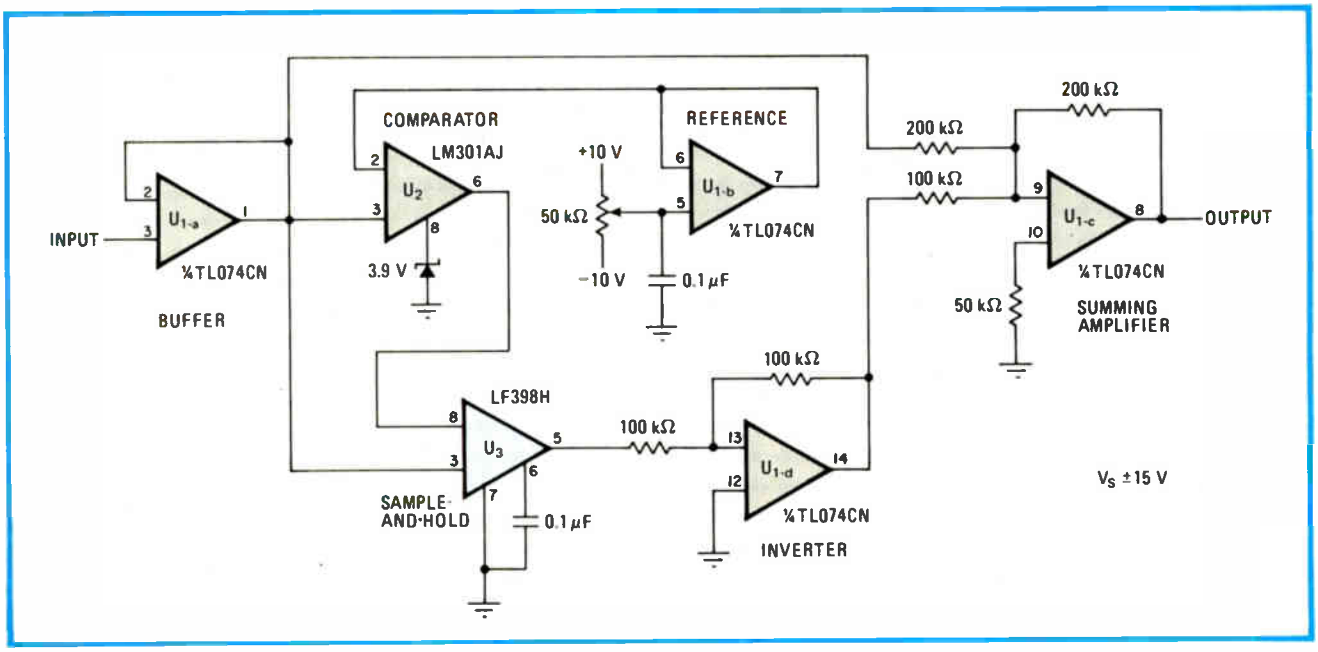


Unconventional rectification. This circuit combines a sample-and-hold IC (U_3) and a high-slew-rate operational amplifier (U_2) in order to provide a low-noise half-wave rectifier that rectifies about any given reference level. Full-wave rectification is then achieved by inverting the sample-and-hold's output and summing it in amplifier $U_{1\text{-}c}$. The hold capacitor determines the input signal's bandwidth.

comparator's output goes high, limited by pin 8's zener diode, and consequently triggers sample-and-hold circuit U_3. This allows the signal to pass through unchanged. When the input signal goes below the reference level, however, U_2's output falls and U_3 holds its output very close to the reference level.

U_3's output is next inverted and fed to summing amplifier $U_{1\text{-}c}$, whose other input is the buffered input signal. The amplifier's resistor network is arranged in such a way that the gain of the original input signal is unity and the gain of the inverted and half-wave rectified signal is double, so that the result is full-wave rectification.

The value of the hold capacitor is selected to match the input signal's bandwidth—a smaller value suits higher frequencies but produces droop at low frequencies. With a ±15-v dc supply and a reference voltage that is variable between ±10 v, a value of 0.1 microfarad for the hold capacitor gives good performance on signals up to 1 kilohertz. □

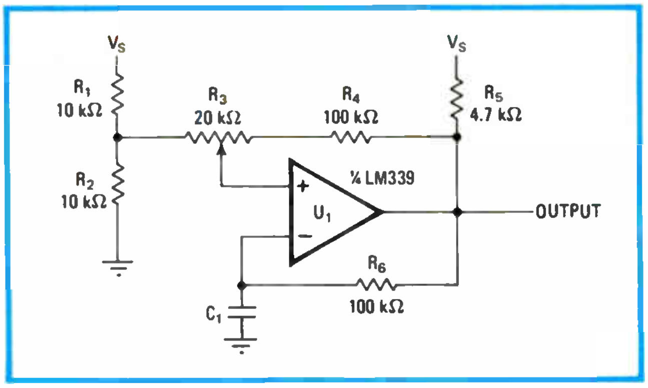
Single comparator forms tunable oscillator

by John Widder
Hewlett-Packard Co., Vancouver Division, Vancouver, Wash.

Using a single off-the-shelf comparator and a few discrete components, this circuit provides a variable-frequency oscillator with a fixed duty cycle of approximately 50%. In addition, the circuit is reliable and its control is smooth. Such circuits often can be used in microprocessor-controlled products.

When power is initially applied, the voltage across capacitor C_1 is zero and output is high. C_1 charges through R_5 and R_6 until it reaches upper threshold V_+. At that point, the output switches to low and C_1 starts to discharge through R_6 until the voltage across it reaches the lower threshold voltage, V_-. Then the output switches to high and the cycle repeats.

Varying the circuit's hysteresis via potentiometer R_3 adjusts the oscillator's frequency. For the components shown, oscillator frequency can vary between 740 hertz and 2.7 kilohertz. □



Tunable. Varying the amount of this comparator circuit's hysteresis makes it possible to vary output frequencies in the 740-Hz-to-2.7-kHz range smoothly. The amount of hysteresis together with time constant R_6C_1 determines how much time it takes for C_1 to charge or discharge to the new threshold after the output voltage switches.

Address-transition detection speeds up byte-wide static RAMs

Predecoding word and bit lines with input state-change detection pushes wide-word RAMs down to single-bit times and cuts power

by John Barnes, Bill Lane, and Vince Soorholtz, *Motorola Semiconductor Products Inc., Austin, Texas*

□ Semiconductor integration has inexorably raised the amount of computing power that can be crammed into single-user systems. As memories mushroom, performance looms larger and larger in the minds of most designers. One key theater of research is the interface between advanced microprocessors and memory. Traditional dynamic random-access memories configured in single-bit output formats—with their address decoding, refresh, and slower speeds—are crimping state-of-the-art microprocessors.

There is a solution: memories with wider output architectures, which let microprocessors receive data in more useful increments—4 or 8 bits per access, for instance. Besides, static RAMs can improve performance by eliminating refresh and other tedious aspects of dynamic RAM overhead. In fact, their performance is so good that byte-wide static RAMs are a perfect match for advanced microprocessors operating at clock rates of 8 megahertz to 16 megahertz.

Wide words at work

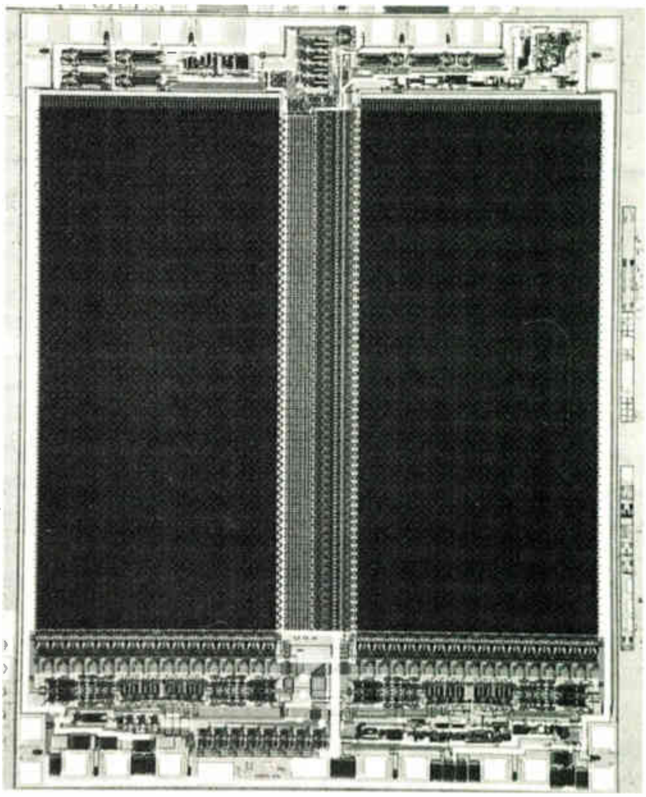
But like many solutions, wider word outputs and static storage cells also create new problems. Static cells typically require six transistors apiece—not just one, like a dynamic-RAM cell—and those five extra transistors are translated directly into a higher cost per bit. And innovative design techniques are needed to prevent the additional output driver circuits needed for wide formats from raising power consumption and slowing down performance.

The speed penalty of 8-bit word outputs has been substantial in the past. Single-bit–output static RAMs, for instance, have reached access speeds of 35 nanoseconds, but 8-bit devices have typically managed only 70 ns. Nonetheless, a design technique called address-transition detection, which detects any change in an external address, helped Motorola engineers to develop a 2,048-by-8-bit static RAM with an access time of 45 ns (Fig. 1).

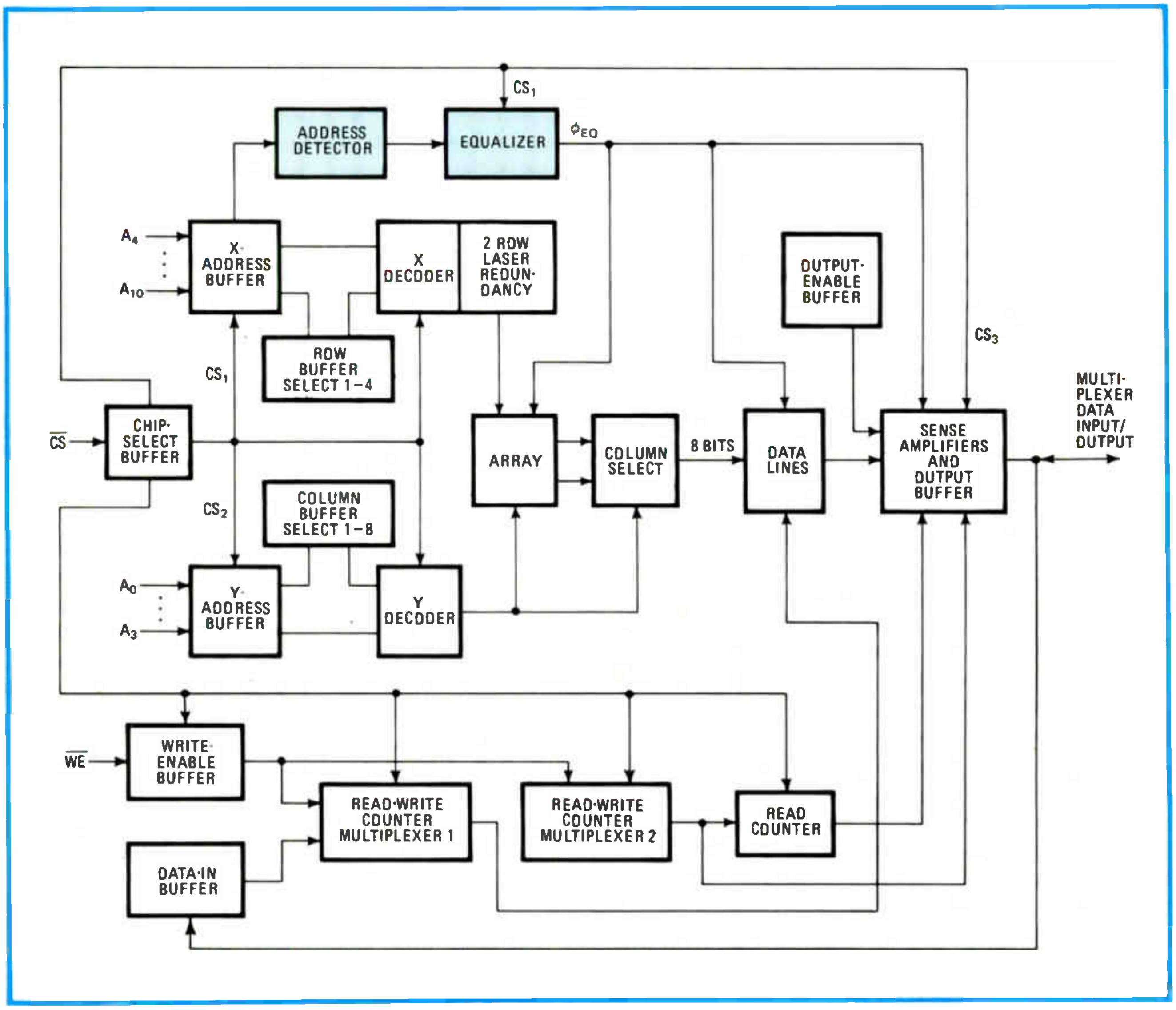
Detecting address changes

Address-transition detection circuitry helps both to raise speed and cut power. By equalizing all differential signal lines just before data pulls them apart, it significantly speeds up access to data but avoids such currently exotic processes as refractory-metal or silicide interconnections. In static RAMS, bit lines, data lines, and sense amplifiers are all paired differential lines. Should these data-path elements remain in their previous data states—as they do in traditional static RAMS—output-state transition times can last up to two times longer than they do with address-transition detection techniques.

The equalization pulse, Φ_{eq}, is created by a comparison circuit that detects an address-level change from a 1 to 0 or *vice versa* (Fig. 2). The pulse provides fast and slow address signals, and a short pulse called Φ_{sat} (phase sense-address-transition) is generated when their logic levels differ. This momentary blip is then latched to start the generation of the one-shot clock, Φ_{eq}. A delay network holds equalization high until the latch is released. Precise layout and circuit timing are needed to minimize the access penalty typical of this method of



1. A sub-100-ns byte-wide static RAM. By combining process advances with address transition detection, Motorola has produced a 2,048-by-8-bit static RAM with a fast, 45-nanosecond access time.



2. Equalization for bit and word lines. Address-transition detection provides an equalization pulse, Φ_{eq}, that restores bit lines and equalizes the sense amps at the start of each new cycle. To improve yields, two rows of redundant storage cells programmed by a laser fuse are added.

clocking the bit-line loads and data-path circuits.

If the nodes are preconditioned with an equalization pulse just before the signal's arrival—instead of continuously, with static pull-up devices—power can be reduced in memories that use address-transition detection. Loading the outputs normally affects access times significantly, however. With address-transition detection the outputs are momentarily three-stated, allowing the loads to move the output voltage toward 1.5 volts. This move to 1.5 V so minimizes the output's voltage change that, even with the slower rise and fall times caused by the larger transistors needed in output drivers, the loaded access time remains equal to or faster than the no-load access time.

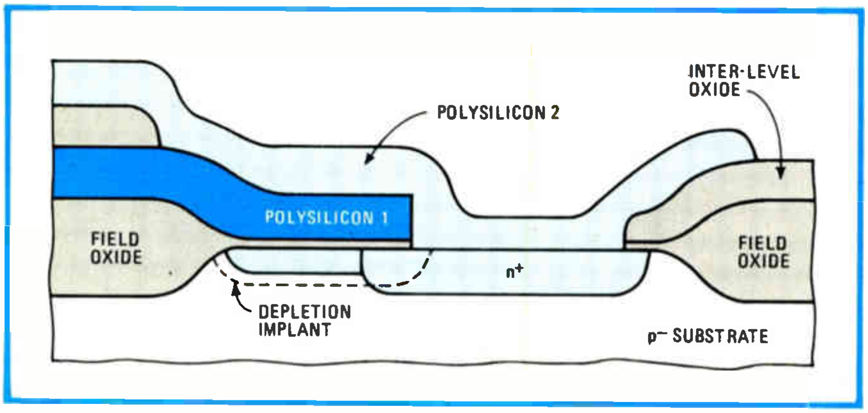
Furthermore, the static bit-line loads, which would consume up to 30 milliamperes in a traditional 16-K static RAM, can be made smaller with parallel-equalization clocked pull-ups. So an added-strength device pulls up the bit line to a 0 logic state before the new word line is chosen.

To cut the power of the unselected row and column NOR decoders, both row and column addresses are predecoded. Two row addresses power-down one of four NOR decoders. Without predecoding, 127 unselected decoders would be consuming dc power. Using part of this saved power to strengthen the row driver can improve word-line speed and subsequent chip access time.

Predecoding for cutting power

Both row and column drivers use dynamic depletion-mode bootstrap circuitry to create supply-voltage–level word-line signals and column-selection signals of higher than supply-plus-threshold-voltage level. These predecoding signals and fast bootstrap circuits guarantee a 45-ns access time with less than 120-mA current.

Besides address-transition detection, 45-ns speeds in a 2-K-by-8-bit static RAM requires 2.5-to-3-micrometer design rules. It is desirable if not necessary that the factory producing such devices benefit from the disciplines of comanufacturing 64-K dynamic RAMS. With commercial



3. Shared versus buried contacts. Overlapping the first and the second polysilicon layers forms a shared contact, eliminating the need for a buried-contact mask step and thus providing better oxide integrity.

process equipment, semiconductor fabrication lines operating on 2.5-μm rules run at 8 to 14 defects per square inch. Further improvements can be obtained through in-house design and fabrication of certain key pieces of automated process equipment.

The cutting down of gate delays depends on a high-speed transistor structure whose key features are the virtual elimination of gate-to-drain physical overload and some variation of the graded drain structure. As effective gate lengths approach 1 to 1.5 μm, however, hot-electron injection caused by charge buildup in the gate-oxide edge can affect long-term reliability—in addition to the usual effects of small gate lengths on yield and speed.

Wide transistors suffer from reduced transconductance because as the charge builds up, the apparent threshold voltage rises locally near the edge of the field oxide. The smallest transistors, and narrow ones, suffer a more generalized threshold increase as the built-up charge extends further into the gate oxide. Eventually, the smallest transistors can fail completely.

Combing process with design

Improving the speed-power product that corresponds to effective gate lengths of 1.5 μm and less requires changing the basic gate structure to minimize or eliminate hot-electron injection. Several techniques come to hand. One requires no additional masking or implant steps: using the first polysilicon masking resist to mask against the reactive-ion etching of the gate oxide. The process rules out an anisotropic polysilicon etch, which would not generate enough polysilicon undercut. The resulting 0.25-μm oxide gate spacer can now be used as an implant mask against a very low-energy arsenic source-drain implant energy because the oxide spacer becomes the doping source in subsequent thermal processing.

Further, the physical gate-to-drain overlap can be virtually eliminated by oxidizing the first layer of polysilicon before the second is deposited. The resulting device structure has low gate delays (thanks to its low effective gate length), low Miller capacitance, and low hot-electron injection.

This structure succeeds in reducing the process to only eight mask steps. The substitution of a shared contact shorting the first and second polysilicon layers for the traditional buried contact (Fig. 3) is especially significant because it improves device yields by avoiding the disruption of cell-oxide integrity and by reducing the "polysilicon haze" effect.

Because the storage array must use transistors with such small effective gates, chip noise has to be controlled. The reliability of a device can be affected by hot-electron injection. In fact, however, high-gain transistors, such as those used in the output drivers, inject carriers in all directions when in saturation. The present generation of 16-K static RAMs store less charge per bit than do 64-K dynamic RAMs, so those electrons that escape the high-gain transistor's depletion region can extinguish data on any positive node. Internal noise injection, alpha-particle sensitivity, and system noise immunity are therefore key issues in the data integrity of static RAMs, not just of dynamic RAMs.

Another approach is to lay out the powerful output transistors as far from the cell array as possible and to increase the effective distance still more by processes, like substrate-oxygen control or surface denuding, that reduce minority-carrier lifetimes. In general, the size of any transistor to be used in saturation—especially the 16-output drive devices—must be held to a minimum. Laying them out is complicated by the need for a substantial grounding structure to hold the substrate voltage at system ground as these eight outputs switch in unison.

If the resistance between device ground and system ground is higher than 0.1 ohm, the noise generated on the device-ground plane can exceed the device's gate threshold and generate incorrect data—especially if the outputs are working into a high impedance. Minimizing the resistance to system ground and loading the outputs cut the noise level on the chip's groundplane. Separating the outputs' groundplane from the ground of the rest of the device seems to work, too.

Because of small geometries, input levels on a 45-ns static RAM are inherently more sensitive to voltage changes. The smallest devices are not used in the first stage of any input. With the rapid propagation of any change, the testing and use of the device becomes more critical. Noise or degraded input levels resulting from slow rise or fall times quickly show up in degraded performance—slower access times and pattern sensitivities, for instance. Proper grounding and clean input signals are needed for optimum performance.

To produce a stable negative voltage of half the supply value, Motorola chose a substrate-bias generator that cut junction capacitances and threshold-voltage body factors, supplied enough substrate current to mitigate hot holes, and could power-down to reduce standby current. An internal chip-disable signal was provided as well, to prevent any circuit action until the substrate-bias voltage reached −2 V during power-supply power-up, thereby ensuring that input transients cannot destroy the circuit during power-up cycles. □

Enhanced version of Bell Labs' Unix serves fault-tolerant multiprocessor system

In this on-line, transaction-processing, multiuser setup, messages keep inactive backup processes up to date, and a faster file system boosts performance

by Sam Glazer, *Auragen Systems Corp., Fort Lee, N. J.*

□ The several commercial variants of AT&T Bell Laboratories' Unix operating system have modifications that make them more suitable than the original for most small-business applications. Yet none delivers the performance and reliability needed for large-scale business applications like on-line transaction processing, expected to be one of most pervasive uses for computers in business during the 1980s. Auragen's system 4000, a new fault-tolerant distributed-multiprocessor system built around an enhanced version of Unix System III called Auros, was developed to meet the needs of those multiuser transaction-processing applications.

Besides adding a special message-communications mechanism, Auros adds Unix enhancements for other aspects of on-line transaction processing, including separate system servers for distributed processing, a modified Unix file system (see "Adding reliability and speed to the Unix file system," below), faster process creation, faster process switching, and more efficient priority dispatching for better performance. Because these modifications affect the Unix kernel internally only and preserve all system calls, existing Unix System III utilities and application programs can run unaltered under Auros.

Commercial on-line–transaction processing requires continuous availability; downtime is disruptive, expensive, and can immediately cut revenue. A system must also expand easily and be flexible enough so that existing hardware and software remain usable as processing re-

Adding reliability and speed to the Unix file system

The standard Unix file system caches data written to disk: if a crash occurs before file-descriptor (i-node) information is actually written to the disk, the new data blocks would be inaccessible. Similarly, if updated i-node information was written to disk and the crash occurred before the new data blocks were written, the old data would be inaccessible.

Auros provides a more reliable file system because the file server maintains "previous" and "current" file systems. The previous system, a consistent read-only structure on disk, is created during the last synchronization. All i-node information that is needed to access files in this system is secure and cannot be lost. The current system, which resides partly on disk and partly in memory buffers, includes all changes made since the last synchronization. When the file server is synchronized, it writes memory-resident data from the current file system into free blocks on the disk, rather than overwriting any data in the previous file system. Once stored, the old current system becomes the new previous one, and the disk blocks occupied by the old previous system become available for use. If a crash occurs, the current file system can be rebuilt from the previous system by performing all write requests received since the last synchronization.

Besides this reliability, the Auros file system adds the high performance needed for transaction processing. For improved record access, Auros reads data in 2-K-byte blocks in order to minimize the number of seek operations needed to read a record. Also, for better performance in write operations, Auros performs all writes at once to contiguous areas on the disk whenever the system is synchronized.

For an extra measure of reliability and performance, all disk operations occur in parallel to two identical, or mirrored, disks. Besides ensuring that data will not be lost even if a disk fails, mirrored disks improve file system performance even during normal processing. Since the data on the two disks is identical, the file manager is free to select the disk that can access the data fastest, that is, the disk with its head closest to the desired data.

quirements change. In operation, the system must ensure data reliability, high performance for fast response in the face of many simultaneous transactions, and ease of use for programmers as well as for application users.

Expandable system

Auragen's distributed-multiprocessor system 4000 meets all these requirements by using clusters of tightly coupled microprocessors. These separate microprocessors serve separate system functions for terminal input/output, disk I/O, application processing, and operating-system activities. Because these functions do not compete for the resources of a single central processing unit, the system's performance remains high, even as the number and type of on-line transactions increase. A typical fault-tolerant system loosely couples two of these clusters, but can expand to 32 clusters without requiring redesign of applications.

In building a version of Unix to run on this distributed multiprocessor and multicluster architecture, Auragen made a basic change in the calls for some operating-system services. In standard Unix, file I/O and terminal I/O services are kernel functions. For example, a user process issuing a READ enters the kernel mode and then directly executes the file-handling and device-driver routines. On completing these operations, the process returns to the user mode and continues execution.

Special servers

In Auros, file-handling routines and terminal-I/O functions are removed and run as special system servers, or privileged-user processes. In addition to the file server and terminal (TTY) server, Auros uses a page server, for demand-paged virtual-memory management, and a process server, to keep track of and balance the load between user processes in different clusters. Kernel functions in Auros include message handling, automatic fault tolerance, and determination of processes able to execute.

For maximum system performance, system 4000's operating-system components are distributed in a way that complements the specialization of the cluster's separate modules (Fig. 1). The page, process, and file servers all run along with user programs in the work processor—a pair of MC68010 microprocessors that share a demand-paged memory-management unit. At any time, each 68010 runs a different user program or system server that resides in the cluster's main memory.

The TTY server runs in the communications processor, which handles communications protocols using its own MC68000 with 256 K-bytes of local memory. Operating-system–kernel functions, including fault-tolerance support, are handled by the executive processor, which has its own MC68000 and 256-K-byte local random-access memory. Finally, a bit-slice processor handles data access to mass storage devices like disk and tape, and manages functions such as optimizing the disk head's movement.

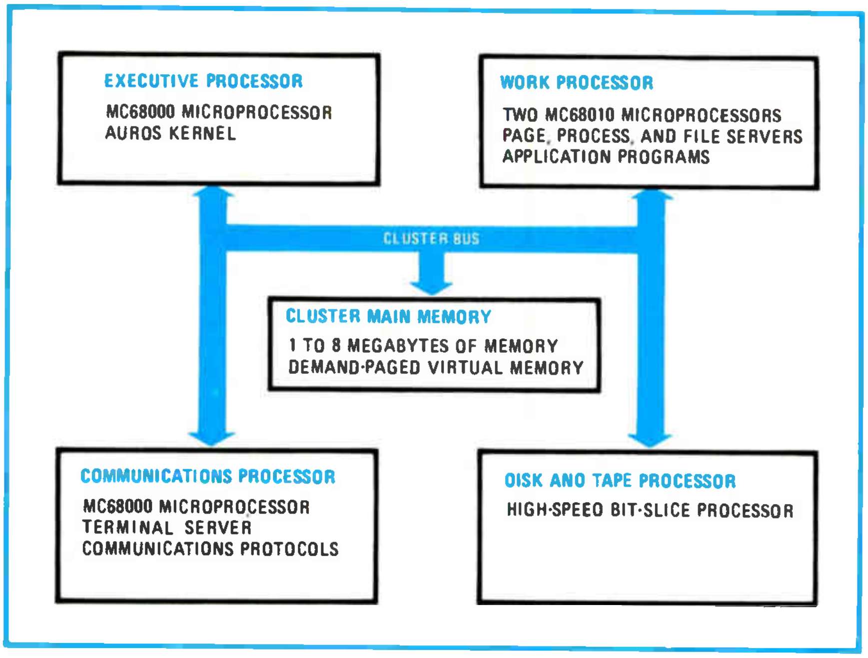
Processor clusters

Every cluster in a system has an executive processor, a work processor, and at least 1 megabyte of shared memory. Individual clusters can be configured with different combinations of communications processors, disk-tape processors, and up to 8 megabytes of main memory to support communications-intensive, data-base–intensive, or computational-intensive transaction applications.

Each cluster uses its own copy of the Auros kernel; however, system servers are available throughout the system. The queue-and-count message system described below makes it possible for a system process running in one cluster to serve another cluster.

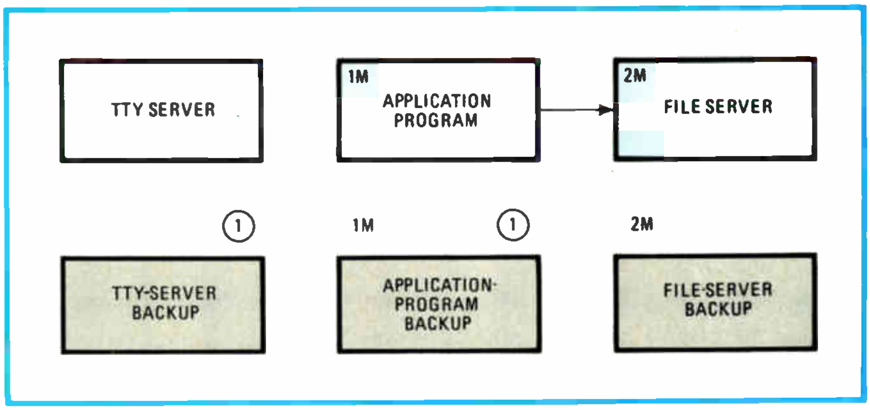
This ability to spread operating-system services across clusters is especially desirable when individual clusters are configured for specialized processing. In addition to distributing servers within a single system, Auros system servers also can be distributed over a local network such as Ethernet or Omninet. The only restriction on distributing servers is that the terminal server and the file server must run in the cluster attached to the devices they access.

Auragen's enhancements to Unix enable programs to access any file, terminal, or communications line without knowing its location. These enhancements further allow any program running under Auros to execute in any cluster or at any local-network node, without the user being



1. Cluster. Within a cluster, separate processors handle system, application, communications, and mass-storage functions. Building a fault-tolerant system then becomes a matter of hooking together two or more individual clusters and letting the queue and count mechanism keep track of messages.

2. So far, so good. After the terminal server and application processor have sent messages 1M and 2M, respectively, the queue and count system sets the count in the corresponding backup processors to one. The appropriate backup processors have queued copies of the original messages, too.



aware of where it's executing. Auros is free to make optimal use of system resources by starting programs in the cluster that has the least load.

Queue and count

Auragen's primary enhancement to Unix was integrating the queue and count message system with the Unix kernel. The queue and count message system controls all interprocess communication and provides the fundamental mechanism for Auragen fault tolerance. All fault-tolerant systems require hardware duplication so that if one part fails another is available to take over and continue its work. Auragen's multiple cluster architecture provides this hardware duplication. Still, programs also require duplication; every program in a fault-tolerant system has two copies—a primary that does the actual processing, and a nonexecuting backup that can continue the work if the primary should fail.

Through its control of all interprocess message communication, the Auros queue and count message system makes Auragen's multiple clusters appear to the user as a single sytem, and ensures that backup programs have all the information needed to take over should a failure occur. In queue and count, whenever a primary process receives a message, the corresponding backup process receives it, too, and saves it in a queue. The backup would process the message only if it had to take over for the primary. In addition to this queue of incoming messages, backups keep a count of all outgoing messages sent by their corresponding primaries. Upon recovery, this count is used to avoid sending redundant messages.

Just how this all works can best be understood through a simple example of a system with three primary processes—a TTY server, an application program, and a file server—and three corresponding backup processes. Here, the primary TTY server has sent a request (message 1M) to the application, which in turn has requested that a record be written (message 2M) by the file server. After the file server has complied and written the record to a file, the queue and counts in the backups would be in the state shown in Fig. 2. At this point, the backup TTY server and the backup application process would each have stored a count of one, although the backup application and backup file server would further have each queued one message (1M and 2M, respectively).

Suppose this sequence of activity is successfully reenacted once. Now, however, as the primary TTY server tries to initiate this series once again, a crash causes the primary-application process to fail (Fig. 3).

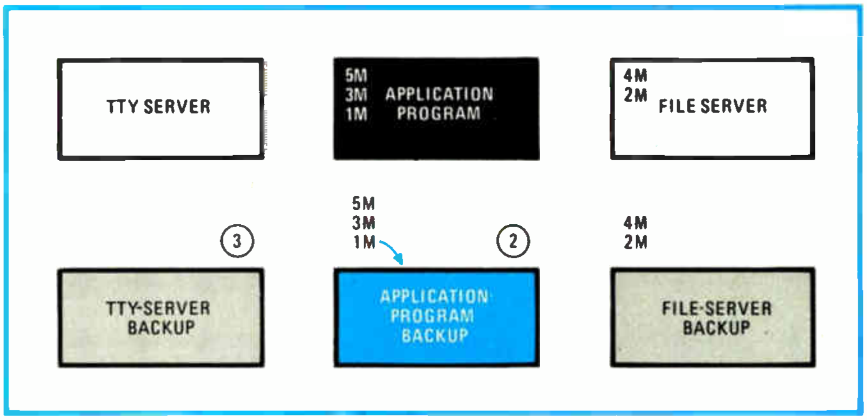
Failure recovery

At this point, the application-program backup will become active and begin to recreate the environment of the primary-application program by processing its stored messages. The queue and count message system ensures that, when a backup process becomes active, it reads the available input messages in exactly the same order as they were received by its corresponding primary machine. The count of messages sent by a primary provides a means to check that a backup does not resend any messages.

Initiating the recovery, the application backup reads the first message on its queue (1M) and, as the primary did some time ago, generates a write request (here called 2M' because it is physically a different message) to the backup file server. Now the count mechanism comes into play. Since the application backup's count is greater than zero, the system recognizes that 2M' is a duplicated write request; rather than write the data twice, the system throws the message away and decrements the count (Fig. 4). Similarly, message 4M' will be thrown away, bringing the application backup's count to zero.

Now, the application backup reads and processes the third input message (5M) and generates a third record,

3. Crash. After the scenario in Fig. 1 has occurred once again, the primary application processor fails after receiving another message from the primary terminal server. The backup processor is now ready to recreate the primary processor's environment by checking its queue of messages.



which it requests be written (message 6M). Since the queue and count message system notes that this message was not previously sent by the primary (since the remaining count of messages sent by the corresponding primary is 0), the message is sent to the (primary) file server, and this third record is written to the disk.

Thus, the system has recovered by using the application backup to reproduce the state of the primary at the point that it failed, and normal operation can continue. Except for a momentary pause during recovery, the user is unaware the system has suffered a failure. Most importantly, no transactions or data have been lost. Because the 4000 keeps running despite hardware breakdown, maintenance engineers can remove, adjust, or replace hardware modules without bringing the computer down.

To avoid any need for complete recomputation by the backup upon failure and to keep its message queue from growing uncontrollably, primaries and backups are periodically synchronized (see "Processor synchronization schemes," p. 149). This synchronization entails the invocation of the normal page-fault mechanism to update those pages changed in real memory but not yet updated in virtual memory. The primary synchronizes its virtual memory with that of its backup when the depth of the message queue reaches a preset value. Only the memory that has changed since the last synchronization and has not yet been updated in the page file is sent. The contents of all message queues and counts are discarded, since recovery can now proceed from the new synchronization point.

Health maintenance

In any fault-tolerant system, if a failure goes undetected, the integrity of the system is corrupted. System 4000's fault-detection mechanisms protect against having an undetected error propagate erroneous information through the system. Auros's "system doctor" is responsible for the health of the system. It communicates continuously with each cluster, checking cluster status and requesting the cluster to run diagnostics periodically. If the cluster reports errors or fails to communicate, the system doctor initiates recovery.

In addition to the system doctor, system 4000 keeps parity on all address, control, and data paths to detect any single-bit error. Besides hardware parity, Auragen's system runs operating-system sanity checks whenever an operating-system subroutine is called. These tests ensure that only legal parameters pass to the operating system.

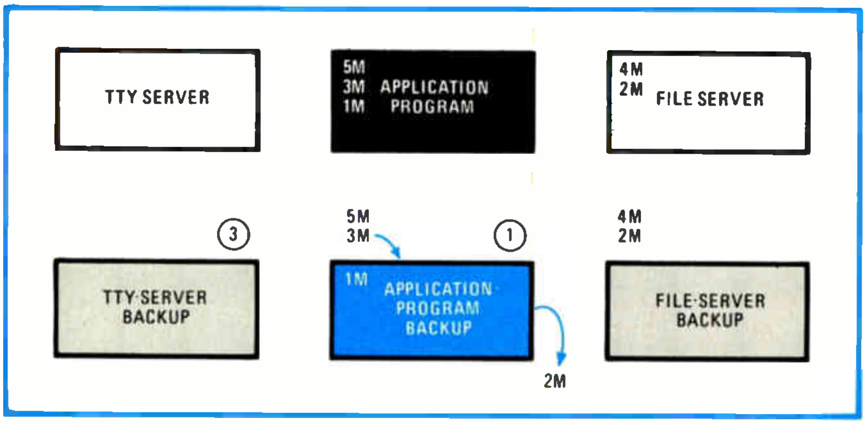
High performance

In keeping with typical transaction-processing environments, a transaction application in the system 4000 consists of many small programs for activities like formatting and displaying a screen, reading input from the terminals, and executing data-base requests. These programs handle one particular type of function for a single user and are characteristically short-lived and I/O-bound. At any moment, each terminal could be executing any one such transaction program out of the hundred or so available in an on-line–transaction system. This environment is very different from the typical Unix time-sharing environment, where users execute single long-running programs that are typically compute-bound (for example, text editors, compilers, and number-crunching applications).

For high performance in on-line transactions, a system must rapidly create and manage large numbers of processes. When a process is created, communication channels need to be established, and a process control block containing the information that the operating system needs to control the task must be set up. In the system 4000, all transaction programs run under a special transaction shell.

When a user logs onto a transaction system, a copy of the transaction shell is created, which in turn opens communication channels to the TTY server and the file server. All transaction programs that the user subsequently runs are forked by the transaction shell and, as in standard Unix, inherit these channels. Transaction processes can be created quickly because the channels do not have to be re-established every time a different transaction program is invoked. Another feature that speeds process creation in the system 4000 is that the process control block for all programs is maintained by the executive processor rather than by the work processor.

Multiple users of on-line–transaction applications share a set of programs. A program cannot be executed unless its instructions and initial data reside in memory. In an on-line–transaction environment, where processes are constantly being created, process creation cannot tolerate the overhead associated with reading in the entire program from disk. Standard Unix keeps the read-only portion of commonly used programs in main memory.



4. Checkout. The failure of the primary application processor has caused its backup to retrieve the queued messages in order, here denoted by the message number's placement inside the box. Since the backup's count is greater than zero, the backup throws away the repeated message at bottom.

Processor synchronization schemes

Schemes for saving—then restoring—the execution state of a computer form the heart of fault-tolerant systems. Hardware redundancy plays a critical role, of course. In addition, though, a careful choice of software techniques can squeeze high performance out of the hardware complement without losing fault tolerance.

Auragen's method of providing fault tolerance has several advantages over other approaches. Some achieve fault tolerance by connecting two systems and having each work simultaneously on the same problem—a solution used extensively in military applications since the 1950s. Such "duplexed" systems provide instantaneous recovery upon failure and do not require special fault-tolerant programming. But the extra hardware needed for fault tolerance yields no extra performance during normal processing.

In the mid 1970s, Tandem introduced the checkpointing approach to fault tolerance. In fault-tolerant systems of this kind, backup hardware can do some productive work during normal operation because the backup programs are nonexecuting. However, the checkpointing method of informing backups about the state of their corresponding primaries is very different from Auragen's queue and count method.

In a Tandem system, primary programs contain special checkpointing instructions. When a primary program checkpoints, it suspends normal execution and sends its backup a copy of its stack and data. The primary program resumes normal execution after the backup's stack and data have been updated. Sending checkpoints slows down the primary program during normal processing. Besides, handling frequent, large checkpoint messages takes up a significant amount of the processing resources both of primary and backup hardware. Finally, special knowledge is required to write fault-tolerant programs.

No special programming is required to develop fault-tolerant applications on the Auragen system because the queue and count message system, which is part of the Auros kernel, automatically initiates and handles the rebuilding of the system. Although the checkpointing technique of Tandem's allow a more rapid recovery (1 s), its overhead slows performance during normal operation.

On the other hand, Auragen's queue and count mechanism trades a slightly longer recovery period (4 to 5 seconds) for better performance during normal operation. Synchronization occurs less frequently than checkpointing. Furthermore, primary processes are not slowed by the synchronization process, because they need not wait for synchronization to complete.

In Auragen's system, all work processors are available for productive work during normal operation. Moreover, few of the resources of Auragen's executive processors are needed to maintain backup message queues. Because Auragen completely integrates fault-tolerant operations into the kernel, source code that runs under standard Unix will run without modification in fault-tolerant mode under Auros.

This copy of a program's instructions can be shared by all the program's users. Each user, however, has a separate copy of a program's modifiable data segment. In standard Unix, this initial variable set must always be read in from disk. In Auros, commonly used transaction programs keep a copy of their original-data space in a cluster's main memory, and the transaction shell can quickly create a transaction process: it simply copies the memory-resident data into another memory location.

Process switching in the system 4000 is fast and uses a minimum of the work processor's resources. Process switching involves copying the current state of a user process into a main-memory location. The state of a process is stored in 16 general-purpose registers and 8 memory-management registers. The work processor can switch quickly between processes by saving and restoring these 24 registers. Auros further reduces process-switching time by having the executive processor maintain a list of runnable processes sorted by priority. When a work processor switches processes, it simply executes the first task on the list.

Application development

System 4000 augments Unix's extensive program-development utilities with additional facilities for user-interface design. The system's screen painter–screen manager allows programmers to create formatted screens by "drawing" the desired form. The screen painter interactively prompts the programmer for field name, editing criteria, and video attributes.

Upon exiting the screen painter, the screen manager generates the program code needed for screen display and control. Any C-, Cobol-, or Pascal-transaction application can use this screen by including simple screen READ and WRITE statements in the program. The screen manager handles the display, editing, and reading of all screens. If the user enters incorrect data, the screen manager will flag the field in error and prompt for re-input. The majority of cases do not need program code for data validation.

Aurelate, Auragen's relational–data-base–management system, simplifies program development by freeing programmers from having to be concerned about physical storage techniques. Aurelate's Host Language Interface allows programmers to use SQL, an English-like query language, as a sublanguage embedded within a host programming language. The Aurelate precompiler preprocesses any C, Fortran, or Cobol programs that use SQL as a data sublanguage interface. SQL automatically selects the best data-access paths.

To make the system easy to learn and use, Auros adds two user interfaces to standard Unix's more complex shell command language. The Auroshell interface provides a subset of commonly used commands that have mnemonic names and follow simple syntactic rules. Auros's visual interface allows users to work with files by pointing to file names with the screen cursor and pressing labeled keys for the desired functions. □

Earlier articles in this Unix series ran in the issues of July 28, 1983, p. 114 and p. 118; Aug. 11, p. 127; Sept. 8, pp. 108–117; and Sept. 22, p. 159.

Delta regulator stabilizes uninterruptible-power systems

Three-phase magnetic regulator prevents phase shifts and keeps power flowing during shorts, overloads, and system failures

by Howard H. Bobry, *LorTec Power Systems Inc., North Ridgeville, Ohio*

□ The uninterruptible-power system that puts out ac power through a delta-regulated inverter is the one most likely to live up to its name today. Because such systems cope very well with sloppy line power, unbalanced loads, sudden changes in load current, shorts, overloads, and subsystem failures, they can supply stable power continuously to computers and other critical loads.

Delta regulation—the key improvement—gets its name from the traditional delta (three-wire) connection for polyphase power transformers. Today's magnetic circuit,

Electronically controlled inverters get complicated

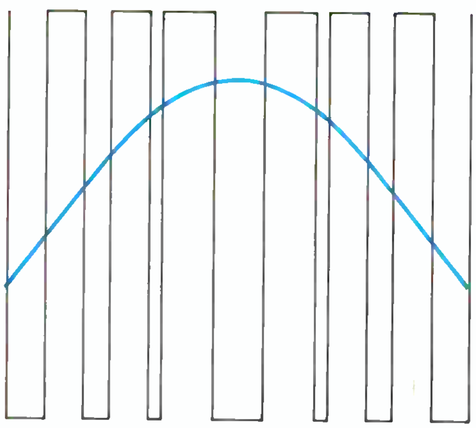
All modern inverters have solid-state electronic circuits to convert a dc input into ac waveforms. But some regulate the ac output with magnetic components designed to saturate at a specific voltage, whereas others control the waveform generator through electronic-feedback and logic circuits.

Most electronically controlled inverters generate the original ac waveform with either pulse-width modulators or step-wave synthesizers. The output sine waves, represented by the colored lines in figures (a) and (b)—are obtained by filtering the original waveforms. In both cases, the original waveform's magnitude is not controlled because it is a function of the inverter's unregulated dc input.

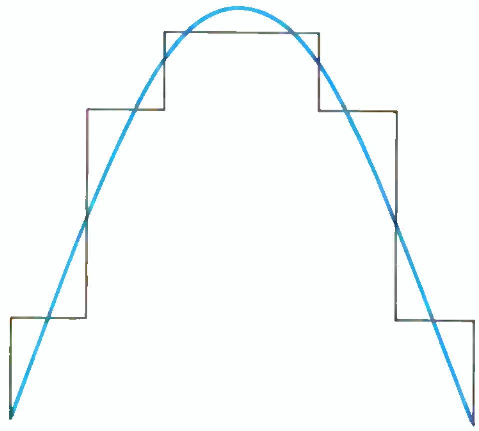
The pulse-width-modulated system corrects output errors by varying the duty cycle, which it must control not only to regulate output but also to produce a low-distortion sine wave without excessive filtering. Step waves require less filtering than pulse-width-modulated waveforms do because they approximate a sine wave, but their other functions are more complex.

Step-wave inverters change transformer taps or add multiple square waves. One version corrects output errors by varying the phase displacement between two inverters. Another varies the inverter's input with a feedback-controlled dc-dc converter. But whether two inverters or a converter and an inverter are used, two power-conversion circuits are needed.

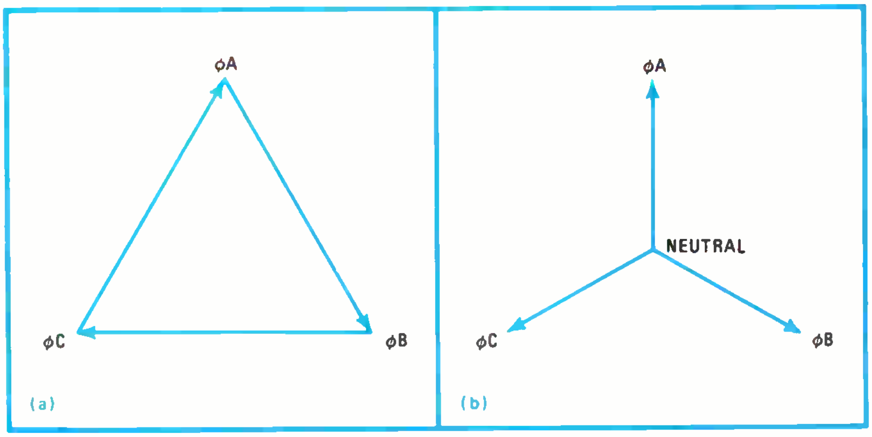
Pulse-width-modulated and step-wave inverters share some problems. Both are complex. Neither has a magnetic circuit's protection against output shorts; they must rely on control circuits to cut currents rapidly back to safe levels. Also, both rely on a control loop remaining stable under conditions that are hard for closed-loop designs to handle.



(a) PULSE-WIDTH MODULATION



(b) STEPWAVE SYNTHESIS



1. Two methods. In basic three-phase regulation methods, a line-line (delta) regulator keeps phase angles at 120° by stabilizing phase-to-phase voltages (a). A line-neutral regulator stabilizes each phase's voltage but may not stabilize phase angles (b).

however, works with three solid-state square-wave generators to convert unregulated dc power into three-phase ac power. It gives a high-power, magnetically regulated inverter better worst-case performance than typical electronically controlled inverters can.

Magnetic regulation is generally preferred in high-power systems because magnetic components are as a rule simpler, more rugged, and much stabler than electronic feedback-control circuits (see "Electronically controlled inverters get complicated," p. 150). Electronic controls do have size and weight advantages, but standby batteries and other backup subsystems make uninterruptible systems bulky, anyhow.

Still, most three-phase inverters, whether magnetic or electronic, have difficulty preventing phase shifts. In Lor-Tec's Delta Magnetic systems, a saturating-reactor network transfers energy from phase to phase. Its energy-balancing action keeps the ac output's three sine-wave components properly phased during load imbalances large enough to deregulate conventional three-phase designs.

The same network also acts as a "flywheel" that keeps power flowing properly during fluctuations in load-current magnitude and direction. Furthermore, it prevents power stoppages. An uninterruptible-power system overcomes overloads and internal failures by transferring loads to alternate ac sources. The network's stored energy gives the uninterruptible-power system enough time to identify and bypass a failure before the failing output disrupts the load's operation.

Three better than one, if . . .

Delta Magnetic systems supply 15 to 125 kilowatts to loads that may contain many computer, communications, instrumentation, or control subsystems. Since the regulators are the output stages, they must tolerate large, dynamic changes in load magnitude or power factor, shifts in per-phase loading, and peaky, discontinuous load currents that may fluctuate between the source and the sink directions.

Delta regulation was chosen because it is inherently a three-phase voltage-regulation technique: three phases are smoother and more efficient than one as long as the three sine-wave components are kept in proper phase relationship. If not, the loads' own power supplies may put out sloppy dc power or, more likely today, interrupt computers and microprocessors by malfunctioning.

Most magnetic regulators are based on a single-phase device—the ferroresonant (or constant-voltage) transformer. In single-phase inverters, the dc input is converted into a square wave, which is regulated and filtered by a transformer and capacitors. The ferroresonant-based regulator produces a phase shift between the square wave and the output sine wave that varies with load magnitude and power factor, but this is no great problem in single-phase designs.

The three-phase adaptation, however, is essentially three single-phase inverters tied together, with the square waves separated 120° in phase. When loads become unbalanced, as they often do in high-power applications, the three sine waves at the regulator output have different phase shifts. These differences can build to the point where they distort the ac sine wave and deregulate the output. Most electronically controlled inverters also find phase shifts difficult.

Ferroresonant designs do not prevent phase shifts because they regulate line-neutral voltages—that is, they regulate the voltage between the sine-wave components at each phase and the common connection of the ac bus. In contrast, a delta regulator controls line-line (phase-to-phase) voltages, thus inherently maintaining the proper relationship between line-line and line-neutral voltages:

$$V_{L-L} = V_{L-N} \times 1.732$$

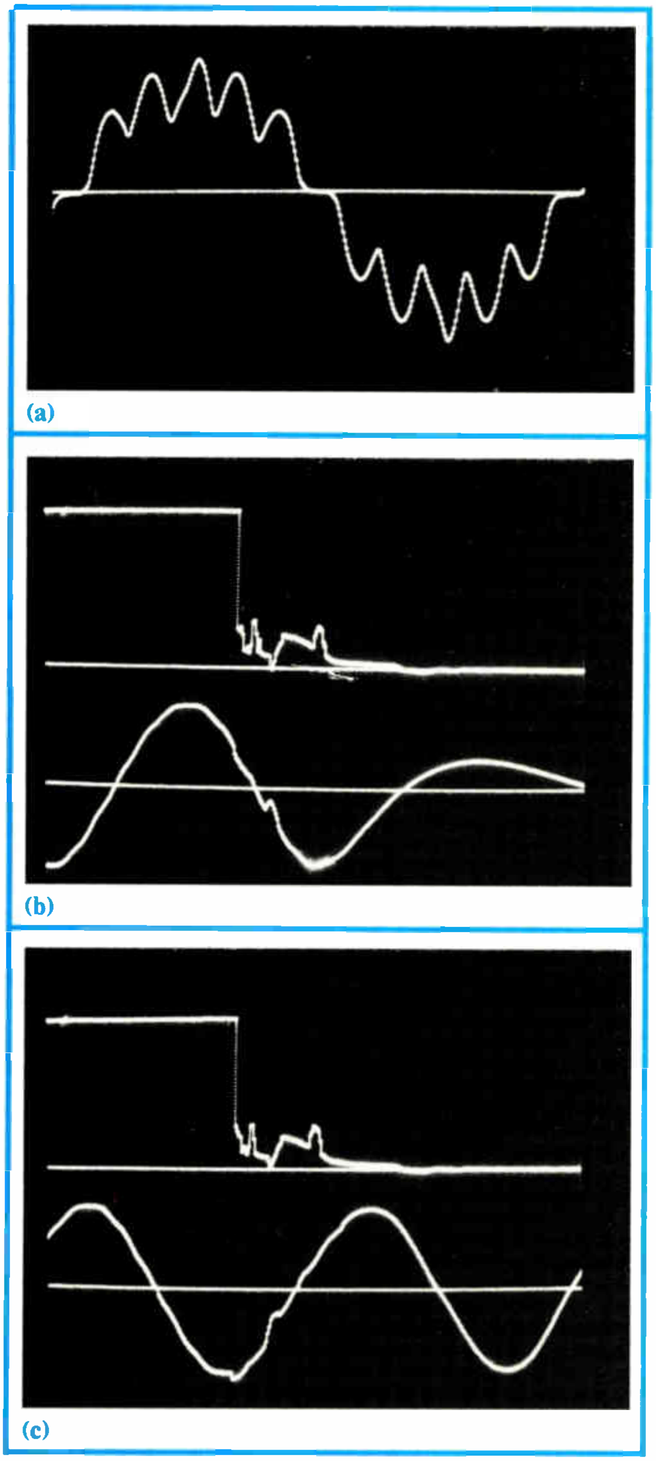
This relationship holds true when—and only when—the phase angles are precisely 120°.

The conceptual difference between line-line and line-neutral regulation is best seen on vector diagrams (Fig. 1). The voltages between phases—ϕ_A, ϕ_B, and ϕ_C— are equalized; in line-line (delta) regulation, the vector diagram is an equilateral triangle; the phase angles must each be 120°; and the line-neutral voltages are also equalized. But line-neutral voltages can be equalized even though phase angles vary, so line-line voltages may not be regulated.

Balancing the output voltages

In the Delta Magnetic inverter, the three square-wave generators are linked by a conventional, three-phase isolation transformer to an inductance-capacitance network designed for line-line regulation and sine-wave filtering. There are delta (three-wire) connections between the solid-state input circuits and the transformer's primary windings, and also between the network and high-voltage taps on the transformer's secondary windings. The three-phase lines and the neutral, or common connection, of the conventional output bus have a Y connection.

The input configuration improves short-circuit protec-



2. Waveforms. The regulator network draws sinusoidal current with nonlinear corrections (a). If the inverter input fails, stored energy prevents a sudden drop in output voltage (b). This "flywheel" effect gives the system time to transfer the load to another power supply (c).

tion and simplifies the filtering of odd harmonics on the waveforms. Linear (nonsaturating) inductors are used to limit inverter current to a safe value, even with a bolted short on the output. The three-wire connection also eliminates triple harmonics (3rd, 9th, 15th, and so on), which must be filtered heavily in a ferroresonant design to prevent sine-wave distortions.

The output inductors are all saturable reactors, and capacitors help them saturate at the desired sine-wave amplitudes. Three inductors and capacitors filter the output, while another three inductors are responsible primarily for the line-line regulation. These are double-wound so that each connects to two transformer windings. The network draws nearly sinusoidal current that varies nonlinearly with voltage (Fig. 2a). If an increasing load tries to pull the output voltage down, for instance, the network will draw much less current, the voltage across the input inductors will drop, and the output voltage will come back to the proper level. The inverter, in essence, acts as a three-phase shunt regulator.

This design works well with unbalanced loads because the network transfers energy from phase to phase, thereby balancing the output voltages and stabilizing line-line voltages. For instance, when a typical 30-kW system was tested with 100% imbalance in loads—a full load at one phase and no load at the other two phases—the output voltage at each phase deviated only a few percent from nominal values. Conventional magnetic and electronic designs tolerate only a limited amount of load imbalance—some as little as 20%.

A 'flywheel' keeps it running

The inductor-capacitor network stores enough energy to act as an "flywheel" in high-power applications—that is, as an electrical counterpart of the heavy flywheels that stabilize engine generators. In normal operation, the stored energy helps the inverter handle large inrush-current loads and loads with pulsating, peaky, or discontinuous current waveforms.

The energy storage also enables the uninterruptible-power system to operate with a "negative" transfer time—that is, the uninterruptible-power system can transfer a load before an overload or failure of a line-power rectifier, battery, or inverter disrupts its ac output. Ordinarily, transfer time is specified as the time that output is disrupted while a load is transferred to an alternate ac source. A typical transfer-time specification is 4 milliseconds. In other words, the "uninterruptible" output would be interrupted for almost ¼ cycle before the bypass restored it.

The delta design keeps the output alive, even with a bolted short across the inverter's dc input bus. Such shorts not only stop the energy flow from the inverter modules to the output but also reverse the current flow. Energy from the rest of the inverter must feed the fault as well as the load. Yet the delta-regulated inverter can still supply the load without significant output-voltage deterioration for about 11 milliseconds, or 2/3 cycle at full load (Fig. 2b). This gives the uninterruptible-power system time to detect the short and transfer the load before the output fails (Fig. 2c).

All this is accomplished with a reliable design. There are no electronic voltage-control circuits to become unstable and fail. The solid-state input circuits are protected by the magnetic components, which are constructed of heavy iron and copper to ensure stability for the life of the system. And the output capacitors are fused, alarmed, and redundant to the extent that about 25% would have to fail to significantly affect the output. □

Family of personal Lisp machines speeds AI program development

Three computers designed to run Interlisp-D implementation provide personal programming work stations for artificial intelligence

by Beau Sheil, *Xerox Special Information Systems, Palo Alto, Calif.*

☐ As programmers explore artificial-intelligence applications, they often find themselves stepping off into the unknown, for the mimicking of human thought processes by computers still has many uncharted areas. The Xerox 1100 family of programming work stations is designed to enhance the productivity of programmers working on these difficult problems. These machines are well-suited to the specialized demands of program writing in application areas such as expert systems, knowledge-based systems, and interactive graphics interfaces between operator and machine.

Such problem areas are fundamentally different from the usual computer applications, for the design specifications are extremely fluid: discoveries made during implementation can dictate changes in the design. Thus, the programmer must use what is known as exploratory development: simultaneous design and implementation accomplished by progressive refinement of both.

This type of programming requires distinctive software tools. In the case of the 1100 family, this software is the Interlisp-D system, a comprehensive, integrated programming environment based on the Lisp programming language. Many of the facilities in Interlisp-D were originally developed on large mainframes. Implementing this software on the much smaller 1100 series hardware constituted a significant design challenge.

The 1100 family is a striking mixture of similarities and contrasts. Since the three machines—the 1108, 1100, and 1132—range in price and performance by almost a factor of 10, the underlying architectures are clearly very different. On the other hand, they all support exactly the same software environment—compatible to the extent that a running program can be stopped in midcomputation, moved between different members of the family, and be started again from where it left off without losing any state.

1. Exploration. The Xerox 1108 exploratory-programming system consists of a bit-mapped, multiwindow graphics terminal and mouse cursor controller. The system processor, 1.5 megabytes of main memory, and disk drives in a separate cabinet.

This level of compatibility means that all three machines must provide effective solutions to the same set of distinctive performance issues of the Interlisp software. These solutions depend on a few key common points in the three architectures, which in turn have decisively shaped the software implementation.

Each machine in the 1100 family is designed to be a personal work station for an individual programmer. The primary tools serving the user may be seen in the photograph of the Xerox 1108, the smallest of the 1100 machines (Fig. 1). The processing unit, memory, and local disk are all contained in the small cabinet next to the desk. The large-format, bit-mapped display offers not only text, in a variety of fonts, but a full range of graphics including line and curve drawing and digitized and half-tone illustrations. The 1100 and 1132 support color and gray-scale bit-mapped displays, which provide an even wider range of options for information display.

The user has a high-bandwidth channel to the machine in the form of a mouse, or pointing device (shown in the user's right hand in the 1108 photo) that, by sensing horizontal motion of the user's hand, allows direct specification of objects displayed on the screen. Not visible is the local-network capability, which permits the 1100 user to access various shared facilities such as large-capacity file systems, electronic printers, and message store-and-forward services.

Using these hardware capabilities, a variety of tools can be provided to enhance a programmer's productivity. These include more effective versions of the traditional programming tools, such as code editors and debuggers, and facilities such as document creation, local and remote file management, and electronic mail. Programmers, like any other professional workers, can reap significant benefits from such nonprogramming professional support tools.

However, these are now standard features in professional work stations or state-of-the-art programming environments for conventional programming languages. The most striking feature of the 1100 family is its ability to provide extensive programmer

Design by successive approximation

Expert systems, interactive interfaces between computer and user, and artificial intelligence applications are all characterized by highly unstable design specifications. Unlike conventional applications, in which the design can be worked out fairly well before implementation begins, designs in these areas must be explored and tried out before the specifications can be nailed down. In short, the designer has to build it before he or she can specify it.

For example, in the case of a knowledge-based system, the designer usually simply does not know what will be required to solve the problem. Not only does the problem look difficult, but human thought processes that seem straightforward often turn out to exhibit subtle interactions and complexities when applied mechanically. Some of these can be detected in paper and pencil exercises. Others, however, simply do not arise until the problem or knowledge base reaches a certain size. Thus, the developer must embark on an implementation facing the almost-certain prospect that he will have to change his mind about it in response to unanticipated difficulties.

The same problem arises in interactive graphics systems. Despite the recently developed understanding of techniques such as menu-directed interactions, multiple windows, and other modern graphics features, the design space is still enormous and relatively unexplored. Most new applications seem to require some extension to the known techniques for displaying information to, and receiving input from, the user. Consequently, each designer is faced with the choice of ignoring these intuitions or striking out into unknown terrain.

Furthermore, even if the designer confines himself to known techniques, anticipating how a particular design will "feel" is still extremely difficult, largely because of the very tight, but ill-understood, tolerances that human perceptual systems impose on things like the latency of feedback. Consequently, the designer of the machine-human interface must expect several iterations of a completely working prototype before the design becomes acceptable.

The need for experimentation reflects a real limit on how prescient the designer can expect to be, rather than a simple unwillingness to work out the consequences of a design in advance. Furthermore, the experiments cannot be limited to making a few quick sorties using toy examples and then reverting to a normal implementation strategy. Many applications require much more thorough exploration. The interesting issues may simply not arise in the small example; the interactive interface may seem fine as long as no one is actually trying to use it to get real work done.

Experimentation may require a full-size model. Nor is the process always quick. It is sobering to remember that even the simple desk telephone is the result of evaluating some 2,500 design prototypes.

support for the radically unconventional software systems required for exploratory development. This support is best appreciated in the context of the application areas in which it arises.

Unconventional programming

Extended experimentation on large systems can be carried out only if the processes of design and implementation are carried out together (see "Design by successive approximation," above). Without such an interleaving, the empirical results of the experimentation are not available in time to influence the design significantly. Unfortunately, virtually all conventional programming methodology is based on the assumption that the process of program development is one of unfolding the consequences of an unchanging design.

Not only are the techniques that are effective for such an unfolding generally ineffective if the design is volatile, but they may positively impede both design and implementation. For example, a standard software engineering technique is the use of multiple, redundant specifications to help detect inconsistencies. While this tactic is effective if the design remains stable, it is counterproductive under conditions of design volatility, because each of the many design changes that must be made requires changing the code in many different places.

For this reason, application domains such as artificial intelligence, where design volatility is the norm, have developed programming environments that facilitate the rapid development of large programs under conditions of design instability. These exploratory development environments provide both a programming language suited for exploratory programming (such as Lisp) and a set of tools for managing the programs being developed.

The most sophisticated programming environments provide integrated programming tools. For example, the Interlisp system notices whenever a procedure is changed through editing or redefinition. The program analyzer then discards any existing analysis, so that incorrect answers are not given on the basis of old information. The same mechanism notifies the program management subsystem—and eventually the user, at session's end—that the corresponding program file needs updating. In addition, the Interlisp system remembers the previous state so that, at any subsequent time, the programmer can undo the change and retreat—undoing all the dependent changes and notifications as well. This level of cooperation among tools provides immense power to the programmer by eliminating enormous amounts of detail that would otherwise have to be managed.

Speaking the language

A key characteristic of any language designed for exploratory development is letting the programmer defer design choices as long as possible. There are four major ways in which Lisp defers commitments that have significant impact on the implementaion of large programs.

First, Lisp supports dynamic storage allocation with automatic reclamation—the programmer can allocate new storage freely, and the system keeps track of usage and reclaims pieces of memory once they are no longer in use. Thus, the programmer need no longer keep track of all the possible access paths to each block of storage; doing so is very difficult if the program structure is liable to unpredictable change.

Second, Lisp supports dynamic typing of variables; that is, the type of data associated with each variable is not fixed when a procedure is written but can vary each time it is called, or even within a single call. This allows the programmer to experiment with the representations to be used. For example, very general but inefficient structures can be used in early versions of a program, and they can be made more efficient after experimentation has firmed up their specifications.

Third, Lisp allows procedures to make free reference to variables. That is, a procedure may use variables that are not bound within any lexically enclosing scope. The binding that is accessed will be found by looking at the calling procedure's variable bindings, then at that procedure's caller, and so on. Dynamic binding allows a procedure to receive and return information from procedures that are arbitrarily far away up the call stack. This feature can, of course, be used to write quite chaotic code. In an exploratory context, however, it allows a programmer to experiment freely with adding new communications paths between different procedures, without having to reconstruct all possible intervening code.

Dynamic procedure calls

Finally, all procedure calls in Lisp are also dynamic, in that procedures are indirectly addressed by name only, so their actual definitions can vary. In its simplest use, the programmer can change the behavior of a piece of code by changing, even at run time, the definition of some procedure that it calls. More sophisticated applications include packaging procedure definitions with the data values upon which they are to operate—often called object-oriented programming—so that each piece of data contains a description of its behavior, as well as its value.

From an exploratory-programming point of view, all four of these language features are well-motivated, but their inclusion comes at some cost. Automatic storage management clearly requires the software to keep track of what is in use. Dynamic typing requires at least one level of indirection for each variable reference because the values assigned to the variable from one moment to the next may occupy different amounts of space. Free variable references might take a lot of processing because the target of the reference could be way up the calling stack. Finally, the dynamic binding of procedures requires not only additional work to retrieve the body of the procedure, but considerably more work to check the arguments given against the specifications found in the procedure that is retrieved.

For this reason, Lisp has always been considered an expensive language in terms of the computational power required to support it. Therefore the implementation of Interlisp for personal machines as small as the 1108 cannot simply be a smaller version of the traditional implementation strategy.

The hardware base of the 1100 machines is varied, both in technology and architecture. The largest machine, the 1132 , is primarily made out of 10,000-series emitter-coupled-logic circuitry, features a heavily pipelined architecture, and has a large main-memory cache. The smaller two, the 1100 and 1108, are both Schottky-TTL machines with little or no pipelining, small hardware stacks, and no cache.

Like the 1132, the 1100 features a very flexible architecture and a relatively high bandwidth from memory, so it can support a variety of demanding input/output devices. The 1108, by contrast, achieves higher performance than the 1100 by providing more specialized hardware support for performance-critical areas (for example, a dual-port memory for the frame buffer) and a more limited general architecture.

Since the family is intended to serve as personal programming machines, a low unit cost is essential, and one design strategy that helps is a single processor serving as both instruction-execution unit and controller of input/output devices. This double duty supports a variety of low-cost controlling subsystems for such peripherals as disk drives and an Ethernet network connection that use the power of the shared processor.

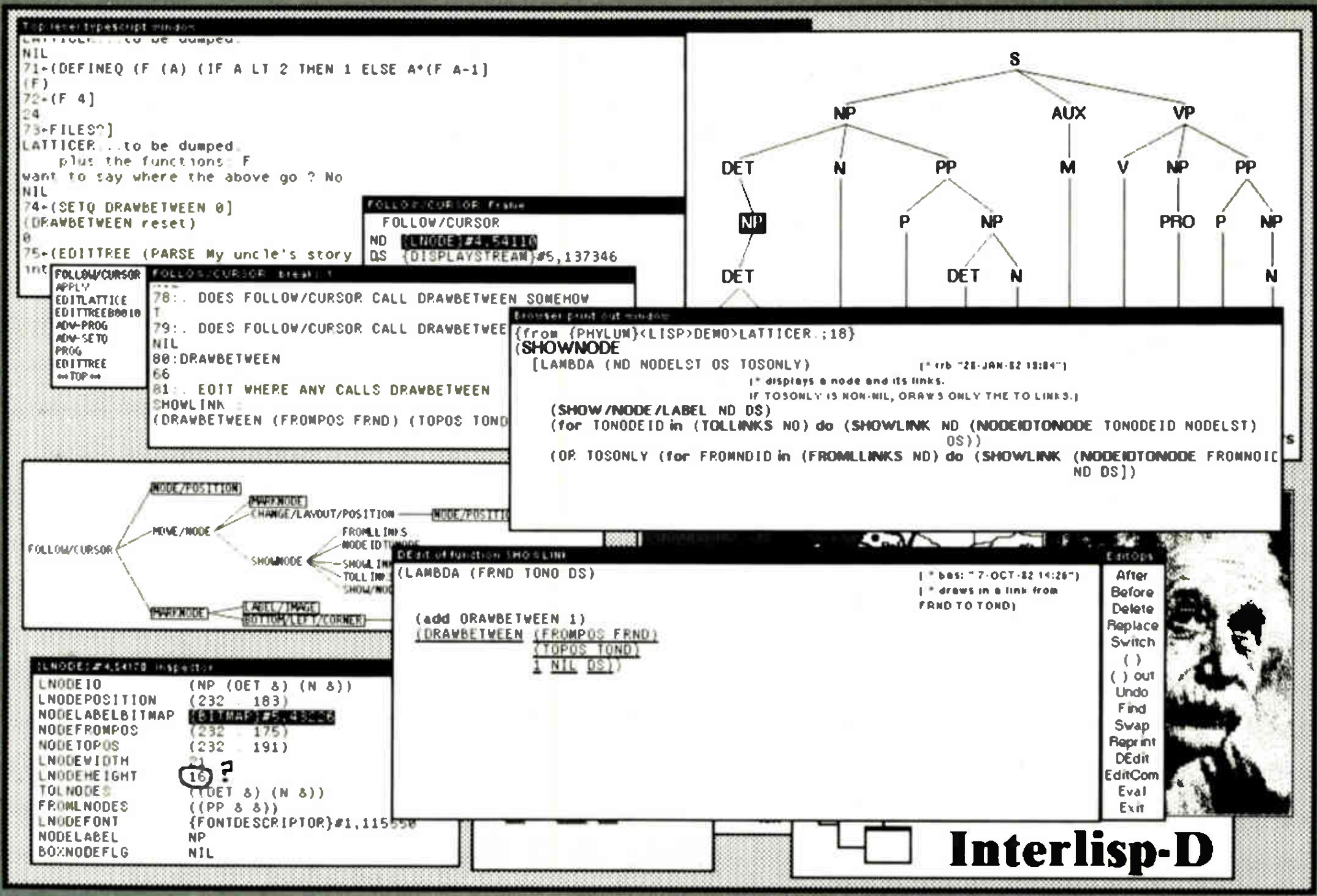
Exploratory-development programming systems like Interlisp-D make strong demands on memory, both virtual memory for the large amounts of code required to provide the rich functionality and real memory for the large working sets typically encountered. All three 1100 machines provide both a large real memory—1 to 4 megabytes—and a large virtual memory—32 megabytes—plus hardware support for the virtual-to-real–address translation.

An interactive graphics interface with the user is a hallmark of Interlisp-D, and all three 1100 machines provide direct support for raster-scanned bit-mapped displays (Fig. 2). Each model allows the programmer to designate a block of directly accessible main memory to be used as the frame buffer for the display. With the frame buffer in main memory, the display may be manipulated directly by the program, albeit at some cost in memory-bus contention. The primary tool by which programs manipulate the bit map is the bitblt operation, which transfers blocks of bit-aligned data and possibly modifies them en route. Although most of these display functions are provided in microcode, a significant amount of shifting and masking hardware helps expedite their operation.

Big software on small machines

The fundamental technique used to implement Interlisp-D on the 1100 family is byte-code emulation. Compiled programs are represented as a stream of byte codes interpreted as instructions to a virtual machine whose semantics correspond fairly directly to those of the higher-level language. In the case of Interlisp-D, these instructions manipulate a stack from which operands are obtained and onto which results are pushed.

This approach has three distinct advantages over a conventional machine-oriented macrocode. It is direct—no machine-oriented macrocode need be implemented and the compiler for the higher-level language can compile into a target language much closer to the source language than a machine-oriented code would be. It is compact—most higher-level operations and statistically frequent code sequences can be assigned single byte-



2. Tools in the window. This screen image shows some of the exploratory programming tools in the Interlisp-D environment. A number of overlapping windows can be displayed, each of which provides a view of some data or one of the concurrent processes.

codes, leading to great economies of space in the compiled code. Finally, it is efficient—the mapping of frequently used code sequences onto single byte-codes provides these with essentially direct microcode support.

The 1100 family's hardware provides two critical features for byte-code emulation. First, a moderately large writable store of 4-K by 36 bits provides enough space so that quite complex instruction sets can be fully implemented in microcode. Writability allows frequent changes to be made in the microcode as understanding of the performance characteristics of the system evolves.

Second, hardware support for the fetching of byte codes, analyzing them, and providing operands to the processor provides an essential boost to performance. As might be expected, the level of hardware support varies across the family—from the high-performance, pipelined instruction-fetch unit of the 1132 to the more modest single-byte IFU of the 1108.

Extensive custom-microcode support, coupled with careful software design, enabled several new techniques for achieving high Lisp performance. These techniques include function calling, automatic storage management, and linked list calls.

Function calling could require a substantial amount of processing because of the memory references required both for dynamic checking and for building the information that must be left on the stack to enable Interlisp features such as unwinding the stack back to a specified point. Interlisp-D organizes both procedure definitions and stack frames so that most of the needed material can be fetched into the cache or hardware stack in a single operation, after which the most common case can be recognized and handled very quickly.

Automatic storage management is handled with a transaction-based reference count system which, once again, optimizes the most common case—a single reference.

The principal data structure, linked list cells, uses a compact encoding that permits two 24-bit data values to be represented in a 32-bit cell. This is accomplished by encoding the common cases of one of the values in very few bits, with a trap value that escapes to a complete representation in the uncommon case. The savings in storage is important because it significantly reduces the amount of main memory required to contain a computation's working set.

The technique is only practical, however, because the encoding and decoding can be carried out by microcode in the shadow of other memory references. A macrocode implementation would incur an intolerable performance penalty. Efficient software architectures like these, coupled with the ability to provide microcode support for the time-critical components, result in high Lisp performance on these relatively small machines. □

Reactive-ion etching eases restrictions on materials and feature sizes

With chemical and ion etching, the technique creates the anisotropic profile needed for VLSI

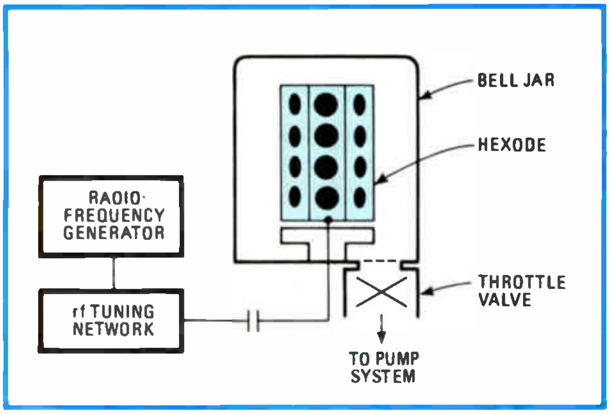
by David N. K. Wang and Dan Maydan, *Applied Materials Inc., Santa Clara, Calif.*

☐ By the late 1980s MOS devices will cram more than 10 million components onto a single chip, MOS-based processors will approach speeds of 100 million instructions a second, and production design rules will demand features of just under 1 micrometer. And when that day comes, it will come largely from new and improved technologies for generating and delineating patterns. Etching is the most important of these steps. The etching processes for the very large-scale integration of the future will have to etch anisotropic features onto highly complex structures, such as refractory metals, silicides, and multilevel aluminum alloys.

To achieve this capability, the semiconductor industry has been passing through a major transition, from wet to dry etching. Fairly soon, dry etching will be used to fabricate all levels of VLSI devices. Moreover, three years ago, only semi-anisotropic etching by high-pressure plasma etchers was available for pattern transfers. Now many systems are capable of doing the job—ion-beam milling, magnetron-ion etching, and reactive ion-beam etching, among others.

Reactive-ion etching seems to be the best technique for high-quality etching of advanced devices. The process consists of a chemical reaction that is enhanced by charged particles, mainly ions, bombarding the wafer. The ions also remove nonvolatile etching inhibitors from its surface and in that way permit etching to continue. Since the ions have an inherent directionality normal to the surface of the wafer, under proper conditions the chemical reaction can proceed in only one direction and thus creates an anisotropic profile. By selecting gases properly, the process engineer can establish the different rates of chemical reactions for different materials and can thereby obtain highly selective etch processes.

Figure 1 shows a batch reactive-ion etcher that can provide both high-quality etching and also high production throughput. Its multifaceted cathode comprises six flat wafer-holders that are located axially in a cylindrical bell jar whose walls constitute the anode. The space between that anode and the cathode is about 6 inches, and the area ratio between the two of them is about 3 : 1. These arrangements cut power density and contamination from the chamber's walls, provide a more uniform etch, and maintain an anisotropic etch. The chamber is connected to a high-vacuum pumping system that can achieve a base pressure of 10^{-5} torr and pump the product gases during etching. Capacitively coupled to the cathode is a 13.56-megahertz radio-frequency generator.

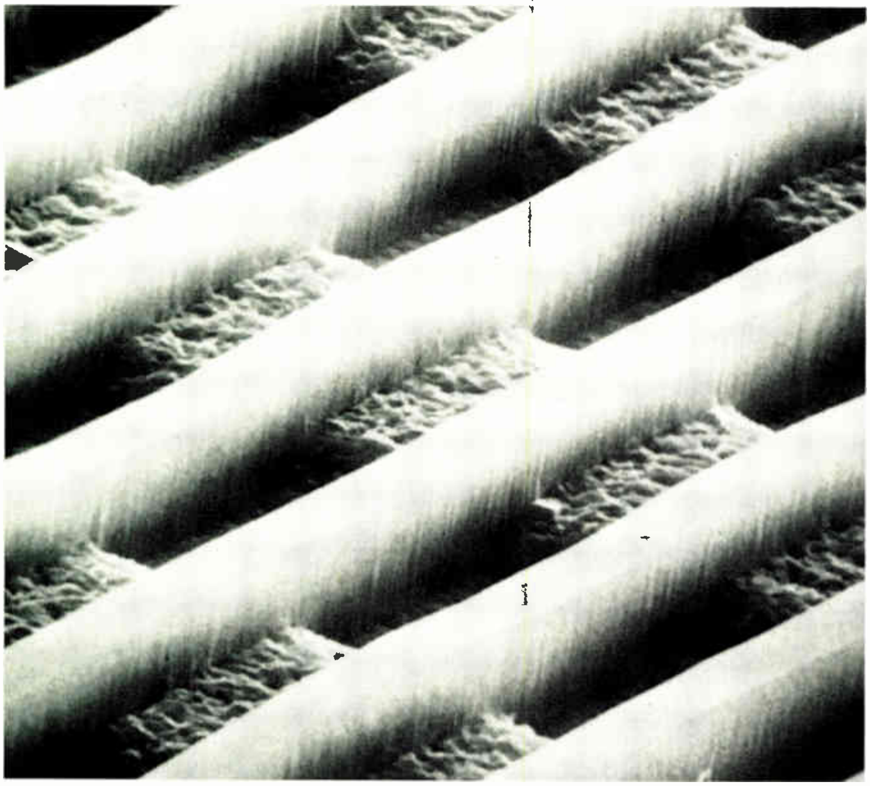


1. Reactive-ion etcher. Combining the advantages of plasma and ion etching, reactive-ion etchers are ideal for fine-line, vertical-sidewall applications in very large-scale integration. Such a system employs a hexode chamber and a radio-frequency generator capacitively coupled to the reactor's cathode.

Multilevel resists

With device design rules below 1 μm it is difficult to get high resolution, good line-width control, and good step coverage simultaneously. Good step coverage can be obtained with a thick resist—at the expense of resolution and line-width control. Higher resolution and good line width can be achieved with a thin resist layer but at the expense of good step coverage.

Some multilevel-resist schemes do demonstrate good resolution, line-width control, and step coverage, all at the same time. For a two-level structure a thick photoresist layer is applied to the substrate and coated with a thin layer of organic or inorganic resist. In the three-level technique an additional sacrificial layer, like silicon dioxide or silicon nitride, is deposited atop the thick organic layer before the working resist is applied. First, the top resist is patterned, and then reactive-ion etching delineates that pattern into subsequent layers. To get a vertical wall profile, to maintain very good line-width control, and to avoid side-wall redeposition from substrate sputtering during overetch, care must be taken to choose the right gases and to optimize etch condi-



2. Three levels. This three-level resist pattern has been reactively ion-etched over aluminum lines, a technique in which a thick layer of photoresist is first applied and then coated with a thin layer of organic or inorganic resist, which in turn is covered by a thin layer of silicon dioxide or nitride.

tions. (See Fig. 2 for an example of etching with a three-level resist pattern over an aluminum surface.) Various laboratories are evaluating these techniques with a view to possible applications in the making of advanced VLSI semiconductor devices.

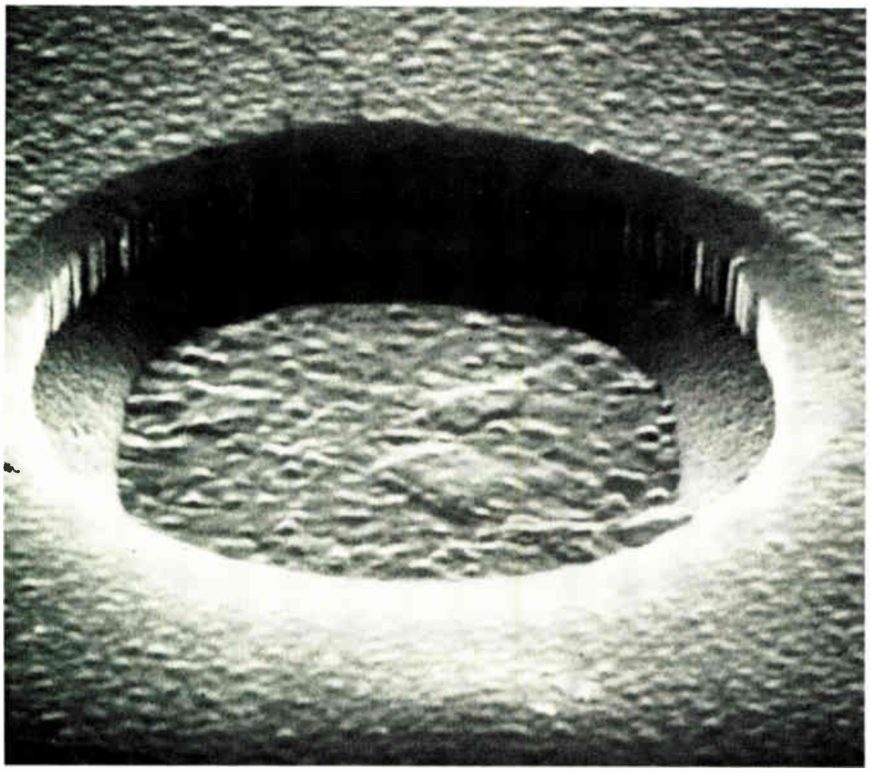
In integrated circuits, metalization failures occur mainly when the metal does not completely cover the dielectric insulating material, a problem that is caused by attempts to replicate topography from one device layer to another and by the very high aspect ratio of contact windows. It is a problem that will no doubt become more pronounced as device dimensions continue to shrink. Complete step coverage of metal over insulating materials will certainly be very difficult to achieve.

To date, device manufacturers have tried to obtain better metal step coverage with high-temperature (1,100°C) phosphor-doped glass reflow, which smoothes the surface topography and contact-window steps. But process temperatures in VLSI chips with shallow junctions or with multilevel metalization structures should be considerably lower. A new planarization technique can, however, replace the standard reflow of phosphor-doped glass.

In this new technique, a thick organic layer is spun atop dielectric materials like nitride or oxide. Since the organic material has rather low viscosity, flow occurs in the course of the application or during a low-temperature bake. The result is a smooth surface either with gentle steps or with a completely flat surface, depending upon the thickness of the organic material that is applied.

Reactive-ion etching techniques then etch the organic and the dielectric layers at about the same rate, so that the profile of the coating organic materials is replicated into the final dielectric layer. The result is a smooth surface. A nitride layer covering an oxide step is made planar by spinning a thick layer of resist.

During planarization, the endpoint between the photoresist and the nitride is readily detected by a laser interferometer. Controlling the relative etch rates of the dielectric materials and the photoresist mask also



3. Tapered. A tapered contact window is shown etched through silicon nitride and polyimide double layers. The silicon nitride is etched to a 45° slope, while the polyimide gets a 90° angle for one third of its thickness and a 45° angle for the remainder.

facilitates anisotropic taper contact-window etching, which is just as important as planarization for good metalization. Etch-rate ratios from 3 : 1 to 2 : 1 produce a tapered etch slope, from 60° to 40°. Oxygen plasma is the main source of the photoresist etch, and mixing and controlling the amount of O_2 in the Freon gases that etch dielectric materials is capable of producing the desired results.

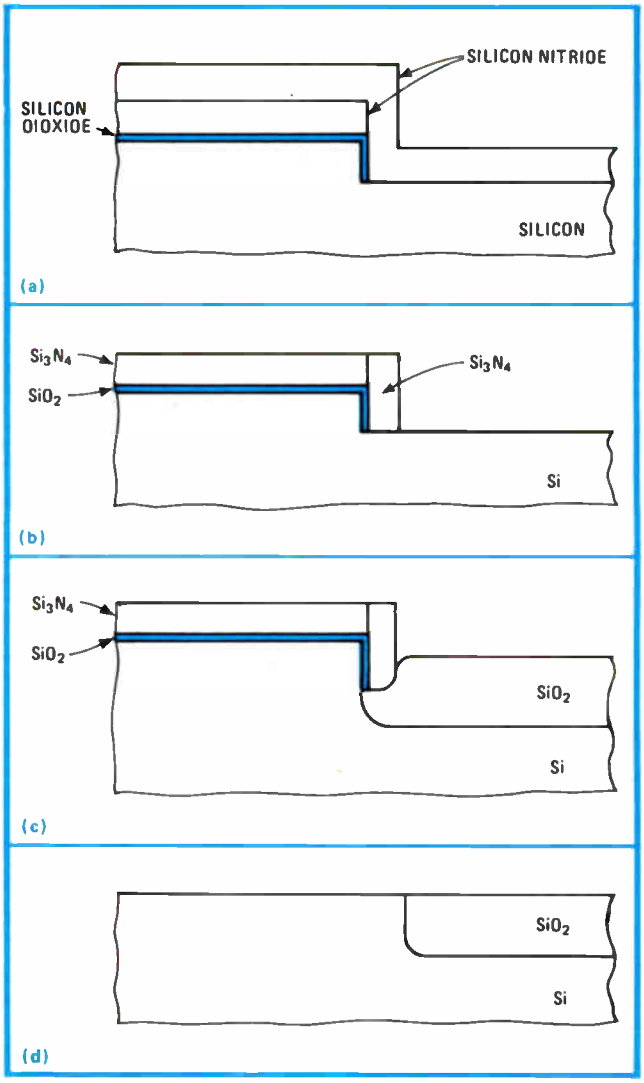
For certain kinds of device structures, the taper window etch actually requires a somewhat more sophisticated process. One such structure is a contact window that is opened through a double layer of plasma chemical-vapor–deposited nitride and a thick polyimide, with a photoresist used as a mask. The etch rate of each layer must be properly adjusted in order to achieve a slope that is smooth overall, without changing the dimensions of the contact. Figure 3 shows the etch profile of such a three-step *in situ* process. The top nitride layer was etched to form a 45° angle, the polyimide was etched vertically to one third of its thickness, and the remainder was etched to form a 45° angle. The result was the fairly smooth profile that is required for the subsequent metalization process.

Isolation technology

Local silicon oxidation—which uses silicon as an oxidation mask, with a thin oxide buffer layer (for stress relief) between the silicon and nitride—has been the dominant isolation technology for LSI circuits. As device dimensions are scaled down without a proportionate decrease in the thickness of the field oxide, this conventional process will face the difficulties inherent in the silicon's different oxidation rates in the masked and the unmasked regions. Uneven rates of local oxidation produce the well-known "bird's beak" structure around the perimeter of the nitride mask. Depending on the thickness of the buffer oxide layer, the encroachments formed can be 60% to 90% of the field oxide thickness. This undesired topography not only deprives the device of space but also creates another problem in the anisotropic etching of the interconnection materials deposited later. Films over steep steps require a significant over-etch to clean the inside corners, which are much thicker than the planar area. As the VLSI of the future continues to reduce the thickness of the gate oxide, any dry-etching process should minimize over-etch of gate oxide, thereby eliminating steep steps.

Recent developments in isolation technology suggest several replacements for the conventional local-oxidation process, most important among them a fully recessed process (Fig. 4) and a refilled-trench isolation process (Fig. 5). Both require a single-crystal–silicon etch. In the fully recessed local-oxidation process, the silicon's etch depth is normally below 1 μm. In the refilled-trench isolation process, however, the depth is 2 to 10 μm, depending on the application. Here, too, the planarization and taper contact-window etch processes can be applied after the trench has been refilled with polysilicon or with oxide.

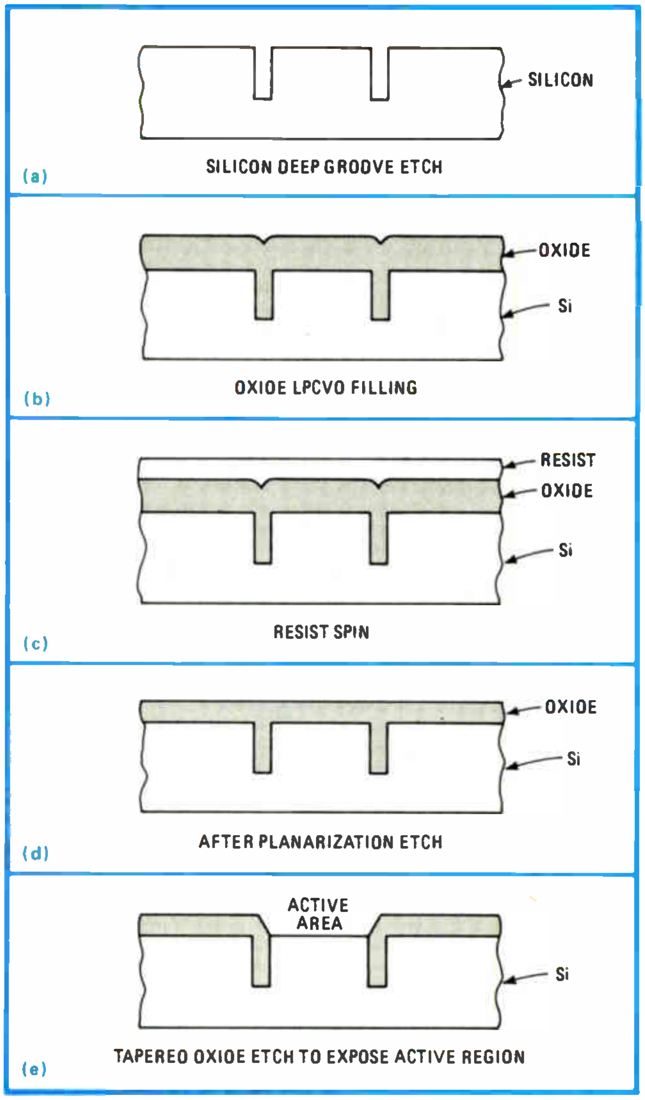
After single-crystal silicon has been etched, subsequent processing and performance will be not be satisfactory if the process has not yielded a vertical wall profile, a rounded bottom profile, and a clean, smooth substrate, free of residue and irregularities. All these requirements have been achieved with reactive-ion etching techniques and fluorinated or chlorinated etch gases.



4. Localized. Differences in oxidation rates of masked and unmasked regions make conventional local oxidation of silicon unsuitable for VLSI. Fully recessed local oxidation through reactive-ion etching, shown in steps (a) through (d), overcomes this problem.

Fluorinated plasma can etch nitride and oxide layers in addition to silicon, thus permitting *in situ*, multistep etching of all three layers in one pump-down operation. This greatly reduces the possibility of defects, since it eliminates additional etching process steps and wafer transfer. The process uses the photoresist as a masking material, for an oxide mask would be etched away. This fact and the selectivity—about 3 : 1—between the silicon and the resist mean that the depth of etching becomes the limitation of the process applications.

For an etch depth of more than 5 μm, photoresist masks are no longer practical. The chlorinated etch-gas process should be used with oxide as a masking material. Figure 6 shows typical results of the *in situ* multistep etching of nitride-oxide-silicon using fluorinated plasma.



5. In the groove. In the oxide-filled groove-isolation method, reactive-ion etching first etches deep grooves in silicon (a), which is then entirely coated with oxide (b). Next a resist is spun on (c), followed by planarization (d) and tapered contact window etching (e).

Polysilicon has been employed successfully in the manufacture of LSI devices, both as a gate electrode and as an interconnection material. Nonetheless, its resistivity makes it incompatible with the more stringent requirements of advanced VLSI devices.

Interconnection resistance

Two ways have been suggested to cut the resistance of the gate-level interconnects and provide reasonable access times. The first, a multilevel metalization scheme, would permit physically wider and shorter interconnects to be used. But this solution would create a topography problem that would make the process more complex. The second uses silicides on gates to cut the resistance of gate-level interconnections by forming a composite layer of polysilicon on the gate oxide and silicide atop the polysilicon. This structure preserves the almost ideal MOS characteristics of the silicon-substrate–gate-oxide–polysilicon structure yet at the same time provides interconnection resistance an order of magnitude lower than that of the polysilicon gate.

Two techniques are now used to fabricate the fine lines of polysilicide interconnections. The first forms a self-aligned metal silicide at the polysilicon-gate, source, and drain-diffusion areas, thus cutting the source and drain contact resistance to acceptable values. This technique increases the complexity of the process. The second technique involves depositing a thin layer of silicide directly atop the polysilicon film and then patterning both layers with a photoresist mask.

In either case, the single-layer polysilicon film or the double-layer structure of silicide and polysilicon film must be etched anisotropically for high resolution and tight line-width control. The high selectivity over SiO_2 is as important, in view of the ever-decreasing gate-oxide thickness of scaled-down VLSI devices.

For subsequent process steps, double-layer structures must meet a particularly stringent requirement for the coincidence of etch side walls. Depending on the process parameters, etching can produce many combinations of profiles for each layer. Besides, residues along the polysilicon edges must be avoided to prevent electrical shorts between conducting lines—a common problem in a double-layer polysilicon structure. In this particular case, a selectivity of more than 30 : 1 over SiO_2 is needed to remove residual polysilicon.

Polysilicon etching with such fluorinated plasmas as NF_3, SF_6, and CF_4 has been studied extensively in the past. Plasma generates active fluorinated species that can react chemically with silicon, silicide, and SiO_2. At high pressures, the intensity of ion bombardment is low. Very high selectivity can be achieved, though etch profiles are more or less isotropic. But in the low-pressure reactive-ion etching mode, anisotropic etching can easily be performed with heavy ion bombardment, which enhances the chemical reactions of the fluorinated species with SiO_2 and thus results in a low selectivity over SiO_2 of less than 10 : 1. In meeting anisotropy and selectivity requirements, it is therefore not appropriate to use fluorinated gases for polysilicon and silicide interconnects.

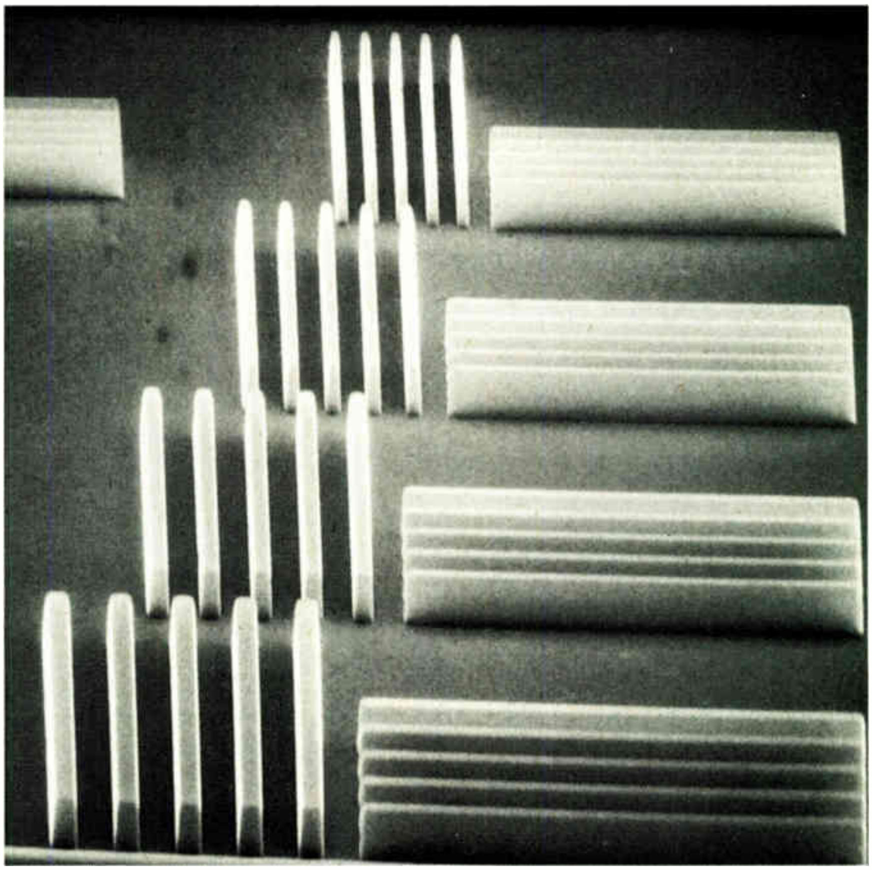
With ion bombardment, low-pressure pure chlorine plasma is ideal for producing both an anisotropic profile and high selectivity over SiO_2. However, the absence of any chemical reaction between the pure chlorine plasma and the native oxide that always exists on the polysilicon surface makes the etching process nonreproducible. In silicide etch, etching cannot proceed in pure chlorine plasma without heavy ion bombardment.

But the addition of a strong reducing, chlorine-containing dopant in the Cl_2 plasma makes it possible to etch the silicide, the polysilicon, and the oxide substrate anisotropically. A two-step process is needed to increase the selectivity over SiO_2.

Metalization matters

Aluminum etching is among the most critical of etching steps, requiring not only an anisotropic etch also a process that can handle very complex structures. In a VLSI chip, a thin layer of titanium-tungsten or sputtered silicon is sometimes deposited on top of the aluminum alloy–barrier structure as an antireflection coating, for

6. Trench isolation. A depth of 2 to 10 μm can be used in the refilled trench isolation. The photo shows how nitride-oxide-silicon is etched *in situ* with a fluorinated plasma. A 2-μm-thick photoresist mask was applied. All three layers were etched in one pumpdown.



better lithographic resolution. In this case, the plasma-etching process must be able to pattern fine lines in place through all three layers.

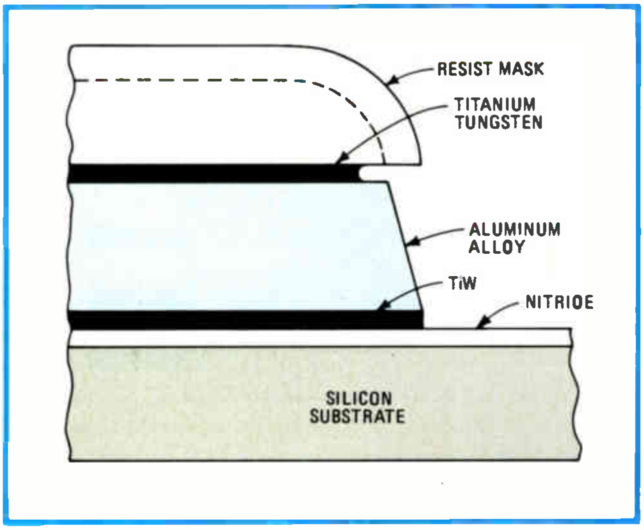
Multilevel metalization structures are becoming more important, too, because they make possible interconnection lengths and relaxed design rules and also make advanced VLSI devices faster and more dense. Tapered anisotropic etching of the first aluminum level is preferred because it promotes a better step coverage for the subsequent layers. In addition to all the other general requirements, the etching process should therefore include a residue-free dry etching of aluminum-silicon, aluminum-copper, and aluminum-silicon-copper, with good selectivities to photoresist, polysilicon, oxide, nitride, and refractory metals. Post-etch corrosion must be eliminated.

Chlorinated gases, like BCl_3, CCl_4, and $CHCl_3$, have been used to etch aluminum in either the conventional plasma or reactive-ion etching modes. Ion bombardment makes BCl_3 or CCl_4 plasma react chemically with aluminum native oxide to form a volatile compound. Chlorine-free radicals generated in the plasma then continuously etch the aluminum.

For a number of reasons, BCl_3 is the most suitable of these gases. First, it is a scavenging agent for moisture absorbed on the wafer and on the chamber walls. Lack of moisture promotes the removal of the native oxide and the reproducible etching of the aluminum. Second, unlike CCl_4, BCl_3 plasma does not form an unsaturated chlorocarbon polymer, which can be deposited on the wafer or on the reactor chamber's walls, and therefore ensures a clean etch and an easily maintainable system. Its etch rate is comparatively low, however—a result of its insufficient supply of reactive chlorine-free radicals. Cl_2 or some other dopant, such as O_2 or CF_4, is needed to get an adequate aluminum etch rate. Note that the proportion of Cl_2 in the gas mixture determines not only the etch rate but also the etch profile.

To etch aluminum-copper alloys, the etch rate of the aluminum and of the copper must be compatible, so that no copper residues are left on the substrate. Since the copper etch product is less volatile than that of the aluminum, ion bombardment is needed to enhance the desorption rate of the copper etch product. The aluminum etch rate must be suppressed below 1,000 angstroms a minute; a reactive-ion etching low-pressure batch reactor is therefore the preferred choice. Batch reactors also have an *in situ* multistep sequential etch capability, without sacrificing throughput.

Figure 7 shows a sequential multistep etch result of TiW/Al-Cu/TiW. The process has six steps: punchthrough oxidized TiW surface, isotropic TiW etch, tapered etch of aluminum alloy through photoresist erosion, anisotropic etching of the second TiW layer, anticorrosion treatment, and, finally, photoresist stripping. □



7. Profiled. Six steps are needed to implement this multilevel, sequential etch of TiW/Al/TiW: the punchthrough of the oxidized TiW, the isotropic etching of TiW, the tapered etching of the aluminum alloy, the anisotropic etching of the second layer of TiW, anticorrosion treatment, and photoresist stripping.

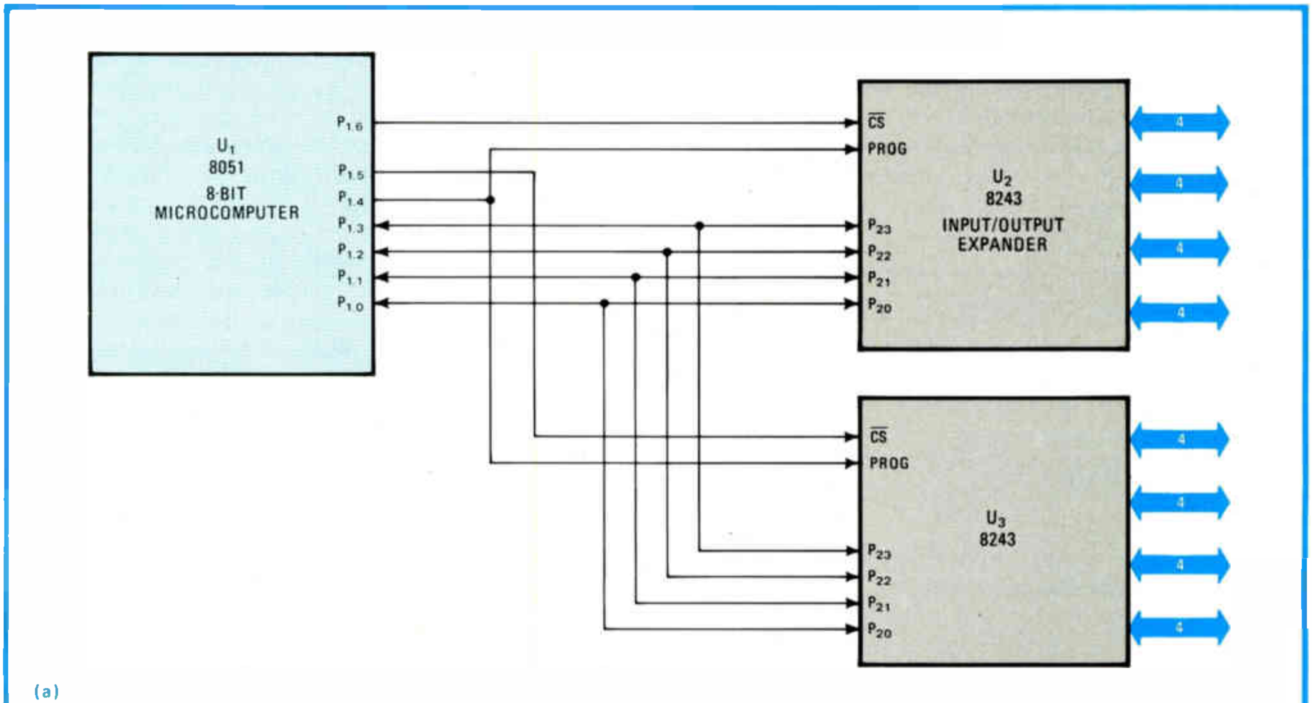
Expanding the I/O facilities of the 8051 microcomputer

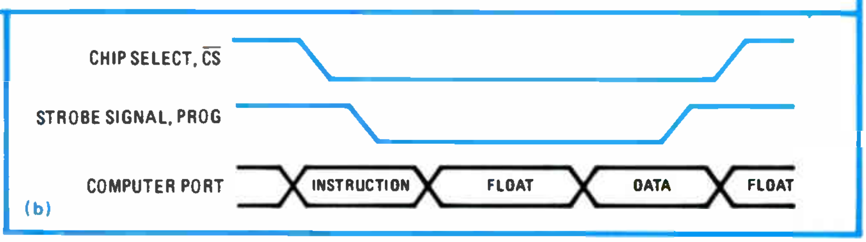
by Robert Brawner
Robert Brawner & Associates, Phoenix, Ariz.
and Alex Toth
Intel Corp., Chandler, Ariz.

In four out of five respects, the 8051 microcomputer chip outdoes the 8048 for many appliance, automotive, computer-terminal, and industrial-control applications: it offers more speed, more input/output pins, and more memory, and adds a full-duplex serial-I/O port. It lacks only the 8048's ability to expand I/O. But in fact, the 8243 I/O expander, which was originally designed for the 8048, can be used to directly extend the 8051's resident I/O facilities if the necessary protocols are emulated by following simple software instructions.

Because the 8051's quasi-bidirectional ports allow each I/O pin either to serve as a test pin or to provide an output strobe, software easily controls data- and control-pin assignments. The interface circuit (a) shows that port pins $P_{1.5}$ and $P_{1.6}$ are used to emulate $\overline{CS}$ functions, while port pin $P_{1.4}$ emulates the PROG-strobe function. Control timing (b) for the 8243 I/O expander is emulated using standard programming procedures (see Table 1).

Because the 8051's Boolean processing instructions provide direct bit handling (that is, single-bit addressing and updating), this I/O expansion program becomes even simpler when these instructions are employed to emulate the I/O expander's $\overline{CS}$ and PROG functions (Table 2). Individual bits can be set, cleared, or complemented with the 2-byte instructions SETB, CLR, or CPL. In addition, bits can be moved to and from the carry flag with the MOV instruction, and logical ANL and ORL functions can be performed between the carry and either the addressed bit or its complement. Also, in the case of the 8243, the 8051's Boolean processing instructions are ideal for updating and testing of individual data or address field bits. □





Expansion. This interface circuit (a) uses I/O expander 8243 to enlarge the 8-bit 8051 chip's I/O facility. The 8243 provides four 4-bit bidirectional static ports as a direct extension of the host computer's resident I/O facility. These I/O ports can be further expanded by daisy-chaining techniques. Control timing for 8243 I/O expander is shown in (b).

TABLE 1: 8051 PROGRAM FOR EMULATING 8243 INPUT/OUTPUT EXPANSION FUNCTIONS

```
; IN8243      INPUT DATA FROM 8243 I/O EXPANDER A
;             CONNECTED TO PORT 1, PINS P1.3-P1.0
;             P1.4 AND P1.6 EMULATE PROG AND CS FUNCTIONS
;             CODE FOR PORT TO BE READ INTO ACCUMULATOR
PROG          BIT     P1.4             ; SYMBOLIC PIN DESCRIPTION
;             ORL     A, #00010000B    ; SET PROG FOR RISING EDGE
;             MOV     P1, A            ; OUTPUT PORT CODE AND OPERATION CODE
;             CLR     PROG             ; LATCH ADDRESS WITH FALLING EDGE OF PROG
;             ORL     P1, #00001111B   ; SET LOW ORDER PINS FOR INPUT
;             MOV     A, P1            ; READ INPUT DATA
;             ORL     P1, #01010000B   ; RETURN PROG AND CS HIGH
```

TABLE 2: PROGRAM EXAMPLE USING BOOLEAN PROCESSING INSTRUCTIONS

```
; IN8243      INPUT DATA FROM 8243 I/O EXPANDER B
;             CONNECTED TO PORT 1, PINS P1.3-P1.0
;             P1.5 AND P1.4 EMULATE CS AND PROG FUNCTIONS
;             CODE FOR PORT TO BE READ INTO ACCUMULATOR
; IN8243      ORL     A, #00010000B    ; SET PROG FOR RISING EDGE
;             MOV     P1, A            ; OUTPUT PORT CODE AND OPERATION CODE
;             CLR     P1.4             ; LATCH ADDRESS WITH FALLING EDGE OF PROG
;             ORL     P1, #00001111B   ; SET LOW ORDER PINS FOR INPUT
;             MOV     A, P1            ; READ INPUT DATA
;             SETB    P1.4             ; RETURN PROG HIGH
;             SETB    P1.5             ; RETURN CS HIGH
```

An 8085 routine divides 32-bit unsigned numbers

by Fred V. James
Sandia National Laboratories, Albuquerque, N. M.

The 8085 assembly-language subroutine on page 165 divides a 32-bit unsigned dividend by a 16-bit unsigned divisor and requires only 21 bytes of memory. The algorithm takes advantage of unspecified operating codes [*Electronics,* Jan. 18, 1979, p. 144] to execute the program in 387 microseconds with a 3-megahertz clock; worst-case execution time is 406 μs. The most significant part of the dividend is placed in register pair HL, its least significant part in DE. The 16-bit divisor occupies register pair BC. Because the two operands are assumed to be nonnegative, each operand's MSB must contain a zero.

Using the restoring method of binary division, the divisor is compared with the higher-order 16 bits of the dividend. When the difference is positive, the partial-quotient digit in the carry, which is 0, is complemented to 1 and the process continued with a left shift. If the difference is negative, however, the partial-quotient digit in the carry is 1. Adding the divisor to the remainder restores the partial remainder, and the partial-quotient digit in the carry is complemented to 0 before the process is continued with a left shift.

8085 PROGRAM FOR 32-BY-16 BIT DIVISION

```
; Input:              32-bit dividend in (HL)(DE), MSB=0
;                     16-bit divisor in (BC), MSB=0
;
; Output:             16-bit quotient in (DE), DIV function
;                     16-bit remainder in (HL), MOD function
;
;         Carry (CY) of 0 indicates overflow error
;         Carry (CY) of 1 indicates successful division
;
; Timing:             Average:    1162 T states
;                     Worst case: 1218 T states

; Algorithm
;
; The subroutine initially compares the divisor with the high order
; of the dividend.  If the divisor is less than or equal to the
; high order of the dividend, the result would be greater than
; 2**16-1 and could not be represented in 16 bits.  In this case,
; an error condition is indicated by zero in the carry and the
; error return is taken.
;
; Otherwise, 16 iterations are performed.  Each iteration
; subtracts the divisor from the most significant 16 bits of the
; dividend.  If the result is negative, the dividend is restored.
; In both cases, the carry is complemented to obtain the partial
; quotient bit, which is shifted in behind the low order of the
; dividend.  Upon completion, the 16-bit quotient is returned in
; (DE) and the 16-bit remainder in (HL).

UDIV    DB      08H     ; DSUB: test for overflow condition by
                        ; subtracting the divisor from high-order
                        ; 16 bits of dividend
        DAD     B       ; restore dividend, leave carry set/reset
        RNC             ; if carry is clear, results cannot be
                        ; represented in 16 bits, take error return

        MVI     A, 16   ; initialize the loop counter
        DB      18H     ; shift low dividend: RDEL

UDIV1   XCHG            ; swap high/low dividend
        DB      18H     ; shift high dividend: RDEL
        XCHG            ; swap high/low dividend
        DB      08H     ; form partial remainder: (HL)-(BC)
        JP      UDIV2   ; if positive
        DAD     B       ; restore dividend
UDIV2   CMC             ; (CY) becomes partial quotient
        DB      18H     ; shift low dividend: RDEL
        DCR     A       ; decrement loop counter
        JNZ     UDIV1   ; until done
        RET             ; return to caller

        END
```

The unspecified operating code 08_{16}, or DSUB, performs double subtraction by subtracting register pair BC from HL, while op code 18_{16}, or RDEL, rotates the contents of register pair DE left.

By saving the sign bits of the dividend and the divisor before calling the subroutine and by using the absolute value of the operand, this algorithm may also be used as a basis for dividing signed 2's complement numbers. Upon return to the main program, the most significant bit of the remainder is given the sign of the dividend. Therefore, if the dividend and divisor are both positive or both negative, the sign of the quotient is positive. □

Engineer's newsletter

Microwave hybrids need polished substrates

Microwave engineers have long understood how important a substrate's surface finish is to the performance of thin-film microwave hybrid circuits, especially at higher frequencies. In the simplest terms, the rougher the surface, the higher the rf loss that can be expected. For example, circuits designed for 5-GHz operation or greater can obtain up to 25% improvements in loss factors by using substrates with a 2-μin. or thinner finish. Indeed, as noted by Robert Fleming, a microwave development engineer at Frequency Sources Inc., Chelmsford, Mass., performance above 40 GHz tends to degrade if surface finish exceeds 500 Å.

Faced with a requirement for substrates with this surface finish, engineers at Frequency Sources turned to Accumet Engineering , a Hudson, Mass., firm specializing in **producing finishes as low as 2 microinches for 99.5% alumina.** For fused silica, which has an ultimate grain size smaller than that of alumina, a 0.5-μin. finish is readily achievable.

Popularity boost seen for energy-efficient metallic glasses

Look for metallic glasses to find widespread use in transformer cores, motor, and electronic uses requiring a low–magnetic-loss material. The reason for this bright outlook is the huge projected savings in total annual power consumption obtainable by switching from cores of grain-oriented silicon steel to cores made of metallic glasses—amorphous metal alloys that are easily magnetized, thus causing very low magnetic losses. Allied's Metglas Products group, Parsippany, N. J., estimates that replacement of all the distribution transformers in the U.S. by amorphous-cored types **would save about $1 billion in electricity costs.** In the industrial motor field, amorphous metal could boost motor efficiency by at least 1%, representing an estimated savings of about $250 per year per motor.

Let the Silicon Valley atlas be your guide

If you are going to Silicon Valley, the 1984 edition of Rich's Business Guide to Silicon Valley will prove extremely valuable. This book pinpoints the locations of more than 1,300 companies with 10 or more employees in a series of street maps. Now in its second year, **the guide has expanded to include more than 900 companies with less than 10 employees.** Restaurant, hotel, and motel locations also are listed. The guide may be ordered for $45 plus $3 for shipping and sales tax for California residents from Business Directories Inc., Suite 215, 1000 Elwell Court, Palo Alto, Calif. 94303, or by telephoning (415) 961-9557.

Primer tells how to test power supplies

A 12-page booklet, "Today's Power Supplies and How to Test Them," from Teradyne Inc., serves as a reference for test engineers responsible for selecting power-supply test equipment and as a backgrounder for those unfamiliar with power-supply test requirements. The booklet highlights recent trends in power-supply design, explains how power supplies work, and describes **the automated production tests verifying that a supply meets its performance specifications.** Both in-circuit and functional tests are covered. Terminology and technical issues pertinent to incoming inspection or manufacturing test of voltage regulators are also defined. For a copy, write to Teradyne Inc., Essex Street, Boston, Mass. 02111.

–Jerry Lyman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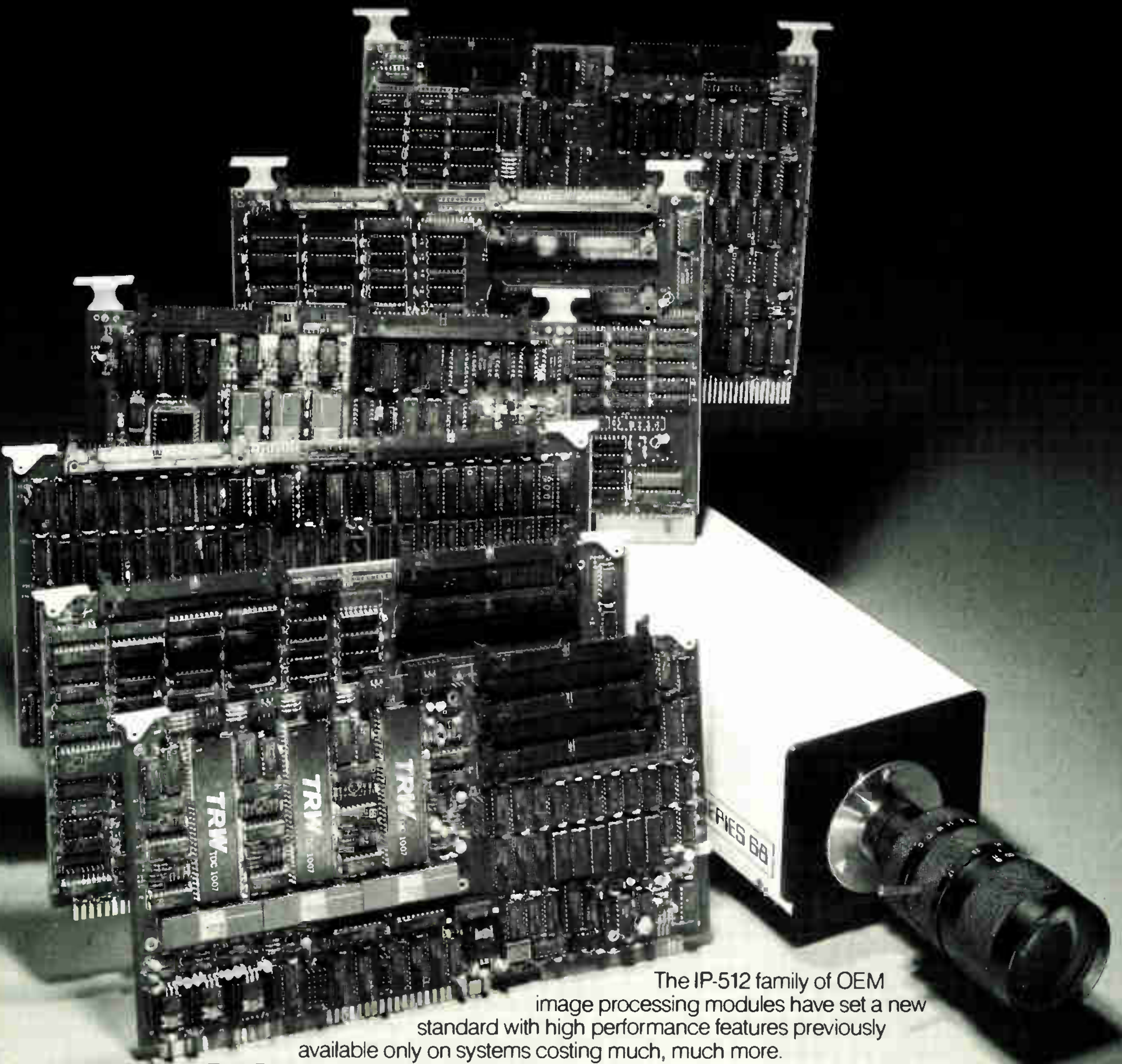

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Wescon Wescon

Electronics industries' comeback means more smiles at Wescon

75,000 expected to attend show in San Francisco as it moves to late fall and expands to four days

☐ With visions of an industry resurgence dancing in their heads, a record number of attendees and exhibitors will return to San Francisco on Nov. 8 for Wescon, the annual ritual of meeting, greeting, looking, and listening. The management of the oldest, and still the biggest, electronics exhibition and convention expects more than 75,000 professionals to wander among the nearly 1,700 booths manned by more than 900 exhibitors at Wescon/83—overflowing the newly completed Moscone Convention Center into the familiar venues of Brooks Hall and the Civic Auditorium.

Wescon veterans will find that this latest conference presents two important departures. First, the date has been changed from the traditional September to early November. Second, a day has been added to make the show a four-day event, the better for exhibitors and prospective customers to sell and buy. For many, however, Wescon/83's focus will remain the professional program. Thirty-five technical sessions will be held in San Francisco, all at the Meridien Hotel.

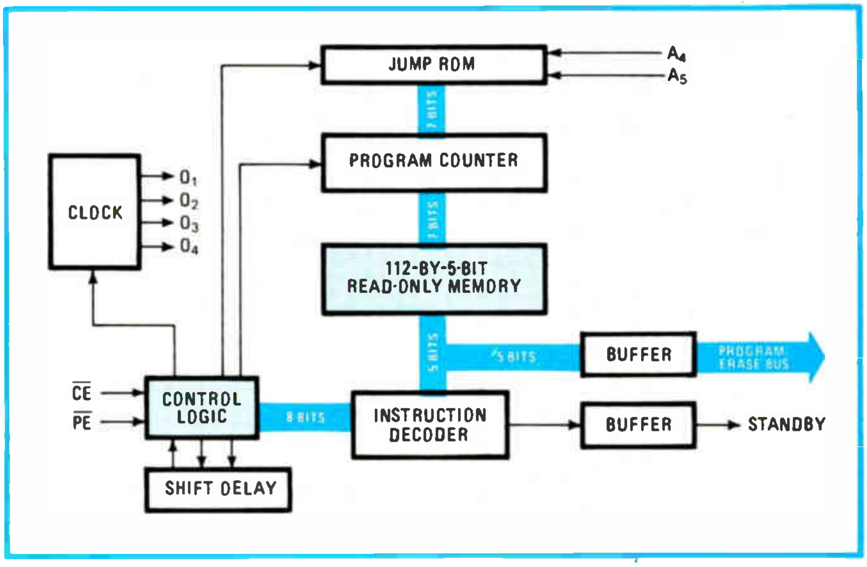
With better than 40% of the sessions dedicated in some way to computer-aided design, engineering, and program development, it becomes clear that the electronics industries are entering a new era: that of system-designed, very large-scale integrated circuits, or, as they are being called by those in the industry, application-specific ICs.

Application-specific ICs include the likes of preprogrammed single-chip microcomputers, gate arrays, and standard-cell devices. As more memory moves onto microcomputer chips, development systems increase in complexity to handle faster devices and larger programs with more input/output points. Gate arrays and standard-cell–design aids extend such complexity even further, to transistor sizes and layout considerations.

Trends and road signs

These design aids and the semiconductors that they make possible will be covered in seven sessions—7, 10, 19, 22, 25, 30, and 33. In all, 36 presentations will discuss developing trends in application-specific ICs and tell what early users of the devices advise others to watch out for in circuit design.

Over the past several years, numerous vendors have taken great pains to educate system designers in the art of using gate arrays; the many papers that will be presented at Wescon on user's experiences testify to the substantial success of such efforts. Primarily, system designers have learned that, in the new application-specific–



Memory smarts. An 8-K-by-8-bit electrically erasable programmable read-only memory from Inmos is one of the standard function chips that will be presented in San Francsico at Wescon/83. It is interesting because its on-chip microprogrammable control sequencer, illustrated here, reduces the control logic complexity that is needed for the in-circuit erase-program cycles.

IC era, price, delivery, and raw performance may not be the principal factors in decisions to use gate arrays. Instead, the most important consideration in many IC decisions is the user-vendor relationship, especially in computer-aided–design and –engineering tools, as emphasized in session 19 by Robert H. Norman, of the Singer Co.'s Kearfott division, Wayne, N. J., and Ralph Schauer, of Ford Microelectronics Inc., Colorado Springs, Colo.

In their efforts to make designers aware of semicustom devices, gate-array makers may have unintentionally attracted new attention also to their most intense competition—standard cells. Such cells offer system designers nearly all the benefits of gate arrays but with the more familiar design interfaces of medium-scale–IC-type logic functions and precharacterized subcircuits. Standard-cell libraries also house migration paths to ever more complex cells, such as microprocessor central processing units and various memory arrays, including nonvolatile random-access types.

Both gate arrays and standard cells, however, suffer from the same drawback—the uneven integration of their various CAD support levels. Although semiconductor firms are making their design tools available and although third parties (the work-station and CAD system makers) are moving to more thoroughly integrated design systems, several bottlenecks still compound problems in the design of semicustom IC devices by system-function designers.

Simulation is the most critical problem. Users stress speed, to give them prototype devices with quick turnaround, while vendors emphasize accuracy, to reach production as soon as possible. Of the two main approaches to simulation, software is more prevalent than hardware. Software simulation, however, can consume hours, sometimes days, of mainframe time and its data output can take a design team even longer to analyze.

Causing the bottleneck are semiconductor makers who guarantee that the chip circuit they deliver will perform exactly as the simulation output their customers described to them—a situation that puts the responsibility for precision back on the project-design team. The true solution is in hardware simulators that can shorten simulation runs to a matter of seconds. Such speeds will allow system designers to work interactively with the simulator, experimenting with and reverifying each of their designs, whether gate array or standard cell, until it is 100% correct.

CAD/CAE companies are moving in the direction of improved simulation, but first they want to equip designers with advanced work stations that provide more flexibility in such semicustom-design tasks as logic entry, verification, automatic placement and routing, and test generation. These systems, by reducing the amount of information that is fed into the simulator, cut simulation time. But the proliferation of different systems from competitive vendors, coupled with the lack of standards in the design-support industry, makes the user's selection of a vendor an even more critical decision.

In addition to semicustom circuits and their design-support requirements, standard-function ICs are amply represented at Wescon. Two sessions on IC controllers for mass memory and floppy- and fixed-disk systems feature eight application-oriented papers from industry leaders, making these sessions a good place to get a brief overview of how different ICs from different makers are approached and partitioned.

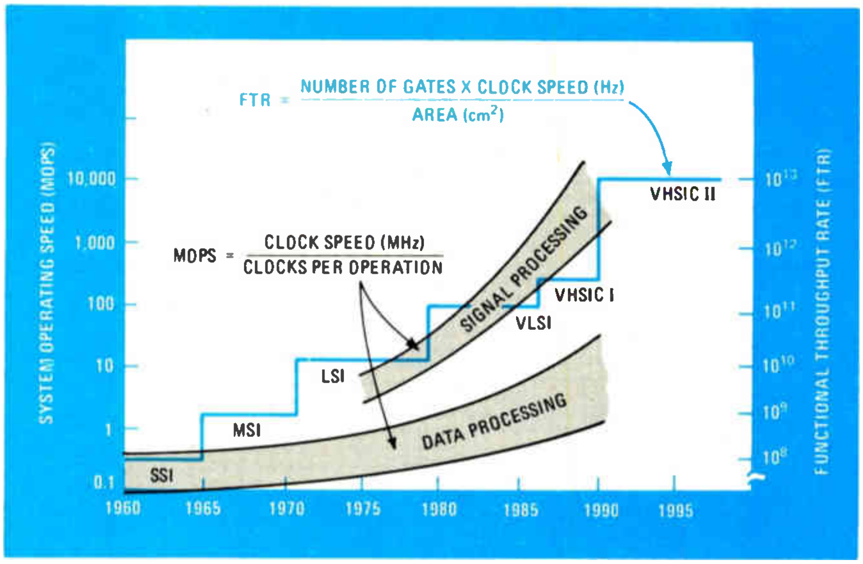
Hardware cornucopia

For the hardware-oriented engineer, Wescon will feature some practical sessions on such diverse topics as IC packaging, surface-mounted thick-film hybrids, and—one of 1983's most discussed subjects—how to comply with new Government regulations on electromagnetic interference.

In packaging, life for the dual in-line package ends, rather than begins, at 40 pins. At that point, the potential IC user or manufacturer has many variations to choose from for high–lead-count devices. Matt Penry, advanced packaging development section head at National Semiconductor Corp., Santa Clara, Calif., will discuss the IC-packaging problem from a manufacturer's viewpoint in session 3.

Penry notes that the rapid increase in lead counts and the introduction of new packages will probably cause standardization of more than one form of packaging. He also will cover tape-automated bonding (TAB) for IC packaging; the chip-on-board (COB) technique for a low-cost pin-grid array (PGA); and the automatic handling properties of various packages.

In the same session, Reed Bowlby,



Ever upward. As the Pentagon sees it, computational throughput has tracked the roughly incremental path of small-, medium-, large-, very large-scale and very high-speed integration. The faster and more complex chips will need more sophisticated design tools.

program manager for strategic marketing at Motorola Inc.'s Semiconductor Group, Phoenix, Ariz., will review current IC-packaging options and offer a peek at the future. For one thing, he sees the PGA's grid spacing tightening from 100 to 50 mils, quadrupling lead density. Bowlby also sees pad-array–carrier packaging, a leadless version of the PGA with an array of contacts on the package substrate's bottom. The pad-array carrier is intended primarily for surface-mounting, direct-solder attachment. Pad-array carriers, he notes, though cheaper, offer packing about as dense as the PGA's and may be surface-mounted. Among their disadvantages are blind joints when assembled and less flexibility in thermal management.

The integration of hardware and software development from the first stage of system design to the last: this is the theme of the Wescon sessions dealing with disparate systems ranging from hardware- and software-development tools to low-cost small-area networks. In fact, from its start as a mere adjunct to hardware design, "the growth of the software component and the need to integrate it with hardware has made software integration the greatest opportunity for most system-development programs," says William A. Swope of Intel Corp.'s Hillsboro, Ore., operation.

In session 29, Swope will offer four points that well represent the views of most Wescon authors addressing hardware–software-system integration:

- Software generation has evolved from a relatively low percentage of the design time for, say, a Z80 or 8080 processor chip to 80% of the time for a 32-bit complex-architecture design.
- To handle the load, the number of software designers has grown rapidly as designs are broken down into modules rather than being handled by one guru.
- Rather than being written by those familiar with hardware and working in assembly language, software is written and debugged in a high-level language by people with no hardware knowledge.
- Overall system performance is governed by the execution flow of the software rather than by the traditional clock speed of the hardware processor.

With these facts as a basic premise, Swope outlines and analyzes the integration of hardware and software for a system design, concentrating on real issues like the hardware-software tradeoffs encountered at each stage.

Swope advocates synergy between hardware and software designs, as does Gail Hamilton of Hewlett-Packard's Logic Systems division, Colorado Springs. But in her paper in session 35, she takes the argument a step further and makes a plea for extensive software-performance analysis. Pulling no punches, Hamilton chastises software designers who work with a high-level language but "have no desire to have any knowledge of the machine that is executing the code."

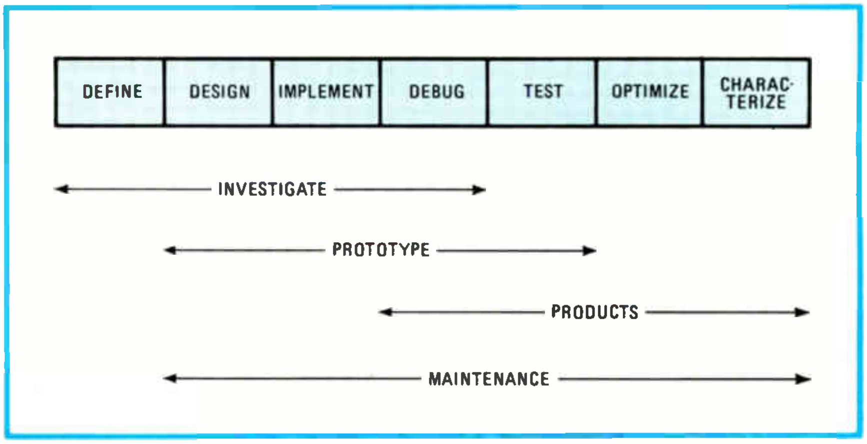
Such a lack of knowledge, she maintains, makes software monitoring necessary to handle what amounts to a software-productivity problem; the software engineer should have the facilities to debug, test, optimize, and characterize software through tracing and performance analysis. More trained software engineers, structured programming, object-oriented languages, silicon software, canned and third-party software, and the like will be a help, she says, but all those are only part of the solution that is to be pursued

Although dandy tools for system development are almost ubiquitous (sessions 29, 32, and 35), to be of use the system integrator must hook them together through, for example, links with various local networks. These networks include the well-known collision-detection and token-passing designs, which, as expected, are well covered (sessions 8, 20, 23, and 26).

Session 8 is a state-of-the-art review of a controversy between competing distributed- and centralized-network designs for microcontroller-based real-time systems. For its major contribution, session 20 features a paper by David W. Sear of Perex Inc., San Jose, Calif. Sear describes a state-machine implementation of Ethernet for the S100 bus—an approach not often seen.

Small-area networks are typical of local networks and are well-discussed in Signetics-Philips–dominated session 26. According to Charles Seaborg of Signetics Corp., such networks connect up to 50 master and slave processors over a maximum distance of 150 meters with a network whose characteristics are between those of a simple serial-data link, such as the RS-232-C protocol, and the full-blown 10-megabit/second Ethernet. The Sunnyvale firm's D2B digital-data bus for small-area networks is designed onboard an 80C51 complementary-MOS microcomputer and is typical of the small-area–network genre. Among other applications, it replaces the wiring harness in an automobile.

Though industry planners have most of the hardware they need for modernizing factories, they come up short



Don't forget. The same development cycle applies to all systems with a major software component. Software maintenance starts almost at the cycle's beginning and goes on past the end, to total 40% to 70% of the project cost. Software performance can minimize this total, though maintenance costs more each time a software bug persists through new development.

on software or the required integration components. With the recent proliferation of computer-assisted–engineering work stations, the problem becomes more difficult—especially for the electronics firms that will be using these devices. With all the elements for computer-aided design and manufacturing in place, it is now possible to integrate them into CAE, says Gerard H. Langeler, vice president of marketing for Mentor Graphics Corp., Portland, Ore., in session 1.

System software falls into three categories: operating system, data-base management, and user interface. "The most critical element of the operating system will be its ability to deal with a proliferation of work stations and data-acquisition equipment that is tied together," says Langeler.

In data bases, the Codasyl approach is giving way to the relational data base—especially now that the latter has received IBM Corp.'s blessing. Perhaps the hardest element to integrate, though, will be the user interface, since everybody has favorites and is reluctant to change. A good interface must be highly flexible and also must be able to handle user-definable function keys, menus, windows, and macro commands, along with various graphics inputs.

Precision is the watchword for session 27, which concerns itself with advances in data conversion. But precision is a moving target. In 20 short years, as session organizer James M. Bryant points out, converters have evolved from boxed laboratory instruments of just 8- or 10-bit accuracy built with a large number of discrete components to today's monolithic devices of 10, 12, and 16 bits of accuracy. Bryant is the European applications manager for Analog Devices Marketing Ltd., Newbury, Berks., England.

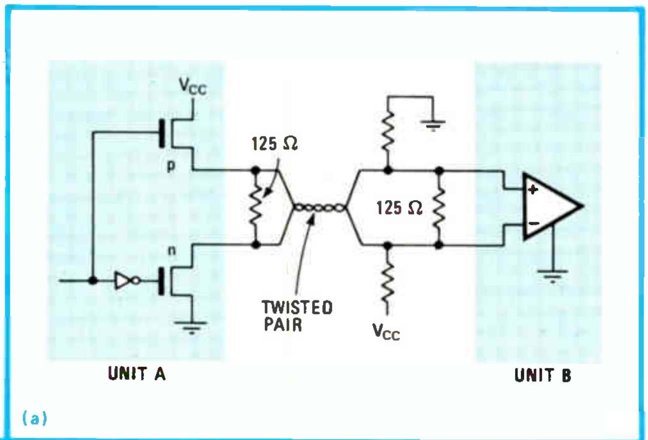
Although advances in precision are being made, participants in the session lament the fact that methods of testing and specifying characteristics are not keeping pace. In his paper, Edwin A. Sloane, manager of advanced development at Fairchild Analog Test Systems division, San Jose, Calif., puts it succinctly when he reports, "Most analog-to-digital and digital-to-analog converters are tested and specified using a limited set of static criteria that provides inadequate performance data for the system designer."

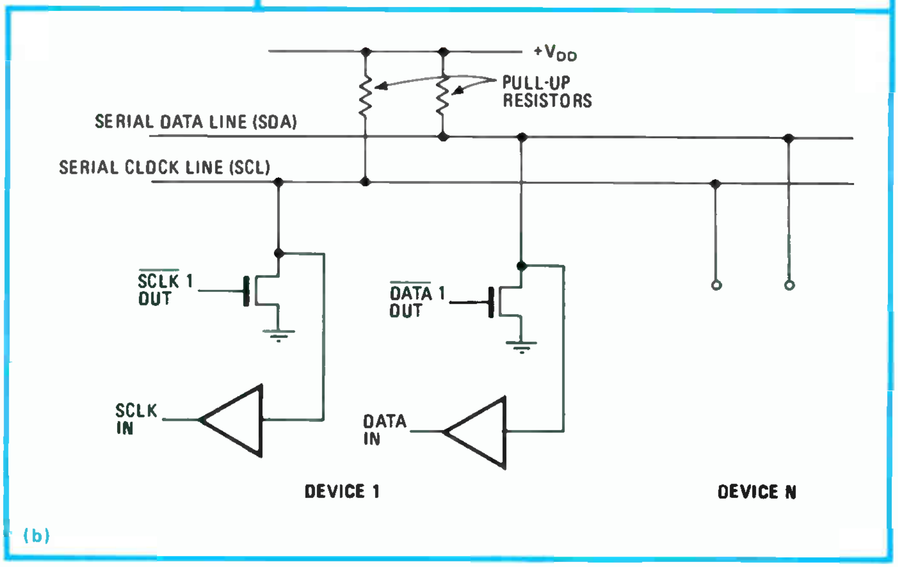
For example, Sloane points out, such characteristics as maximum sampling rate, number of bits, and linearity error may be adequate for quasi-static data-handling applications like weighing or low-bandwidth process control. But the characteristics fall short of the precision that is needed as conversion rates and the implied bandwidth of converters are increased.

Sloane's recommendation is testing that simulates the environment in which the device will be used. He proposes testing all states of the converter and extracting the necessary Walsh coefficients to describe the transfer characteristics and using fast-Fourier-transform algorithms for statistical frequency analysis.

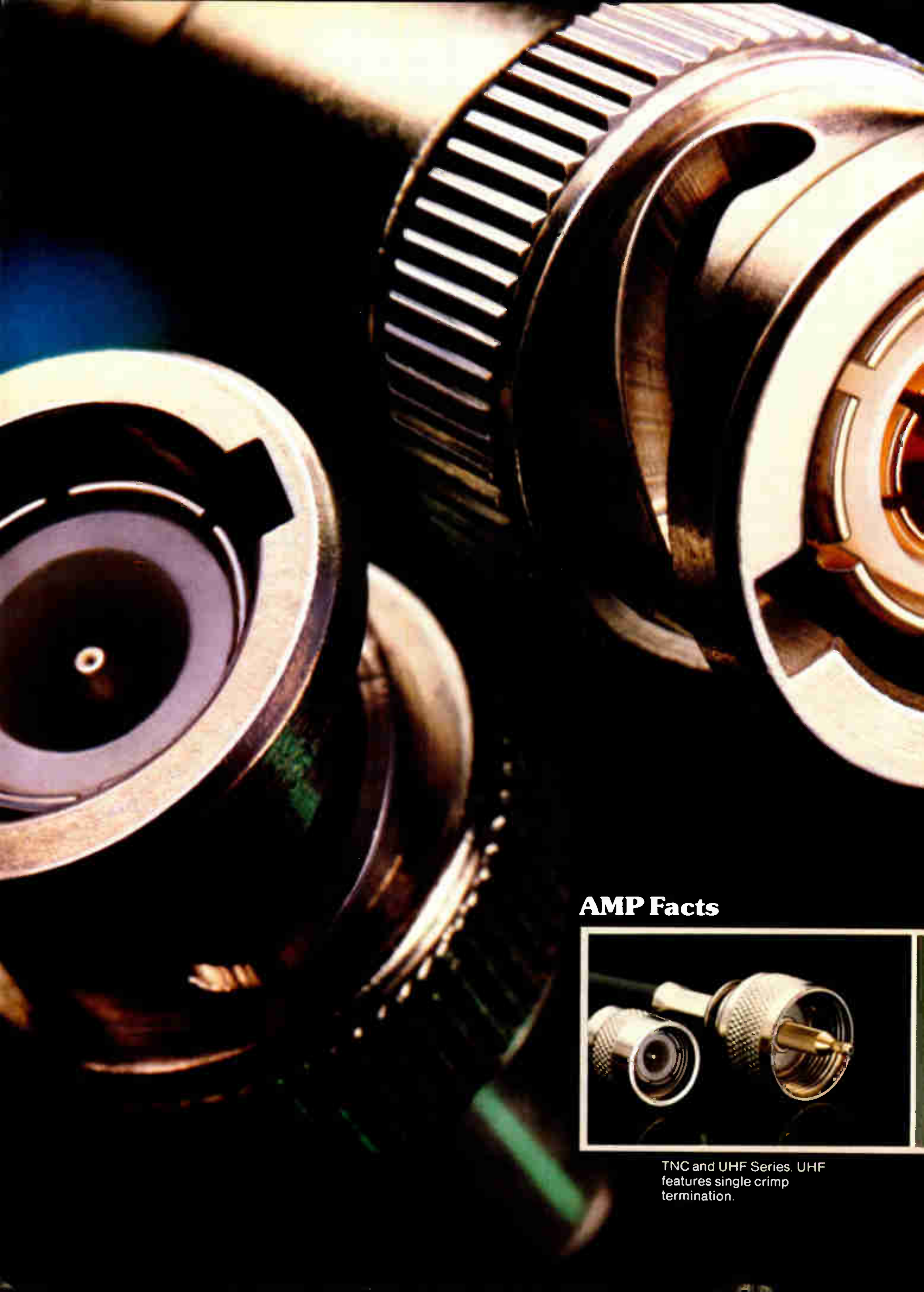
Such characterization methods will prove worthwhile if the advances like the one to be reported by Jimmy R. Naylor, senior design engineer of Burr-Brown Research Corp., Tucson, Ariz., continue. In his paper, Naylor will describe a line of 16-bit d-a converters that are built from a single-chip monolithic DAC. He will also go on to discuss five problems and how he overcame them as well as outlining potential applications for the converters.

Doug Grant, a marketing manager for converter products at Analog Devices Semiconductor, Wilmington, Mass., will report on his company's new designs and processes for high-resolution d-a converters; Baker Scott, manager of data converter design, and his associates, Steve Bolger and Poching Liu, will tell how Siliconix Inc., Santa Clara, Calif., built a monolithic 4½-digit integrating a-d converter. □





ICs connect, too. While Signetics' D2B bus driver and receiver, diagrammed in (a), connects small-area networks, Philips' I2C bus hooks up integrated circuits or modules, as shown in (b). The 100-kilobyte two-wire multimaster-bus design allows more than one bus participant to initiate a data transfer under bus arbitration control.



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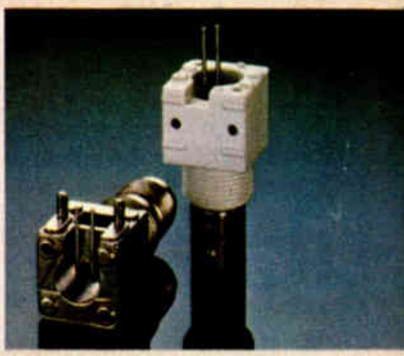

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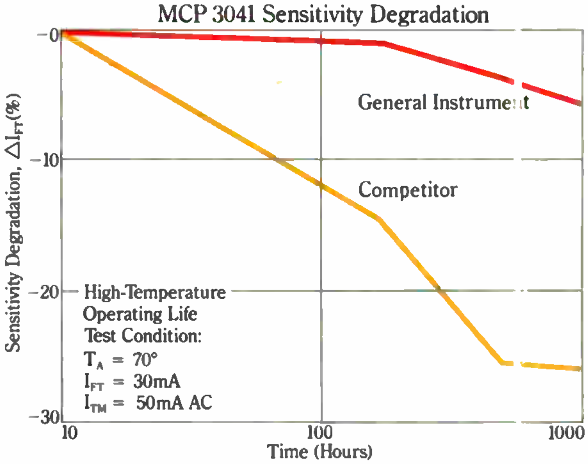

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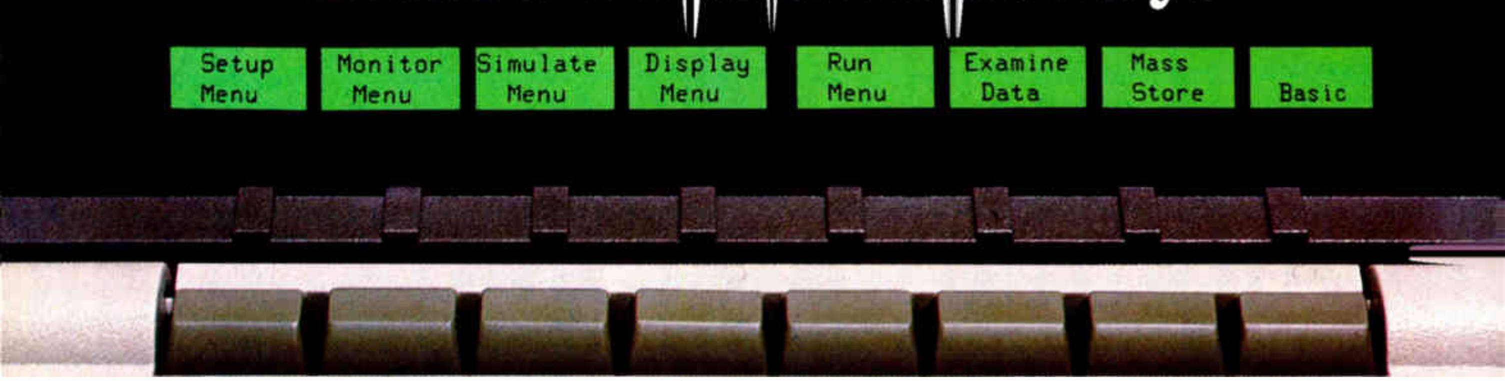

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New products

Novel instruments and design aids shine brightly in the galaxy of products introduced at Wescon, Nov. 8–10 in San Francisco

Digital scope processes inputs before displaying waveforms in seven colors

Several microprocessors, as well as a seven-color display that uses a 9-in. raster-scanning cathode-ray tube and soft-touch keyboard controls, make the multichannel Digiscope 8612 unlike all other digital oscilloscopes. Marketed in the U. S. by Test & Measurement Systems Inc., the instrument is designed and manufactured by Trace Elektronische Geräte GmbH, a company formed in 1981 by several engineers from the University of Austria who had specialized in microprocessor systems and analog-to-digital converters.

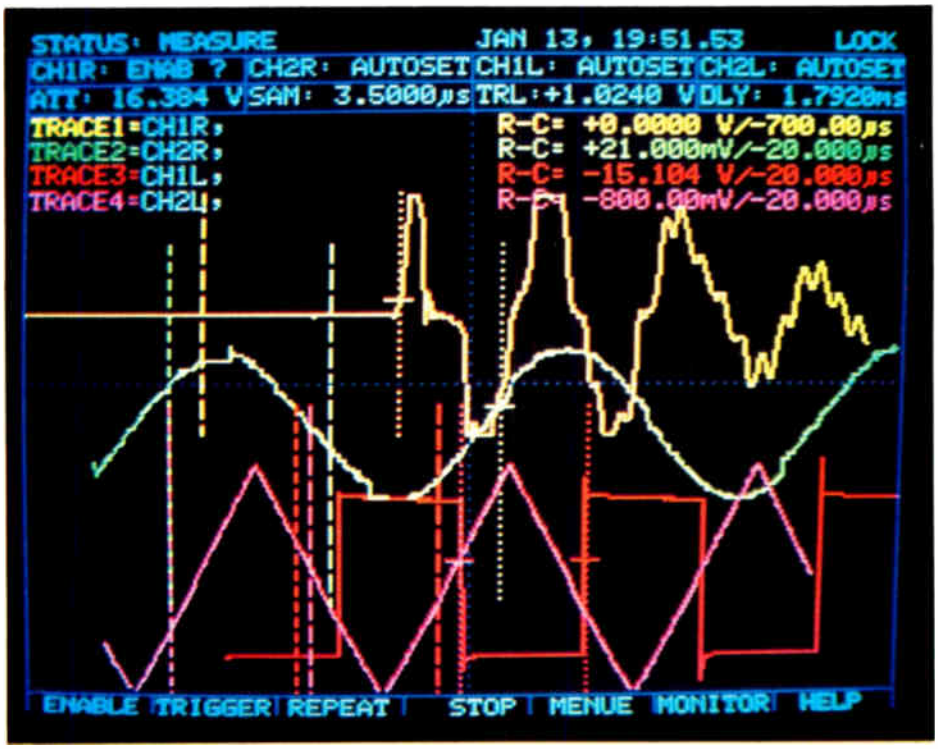
The mainframe accepts up to two input modules from a selection of three: one with two differential-input channels sampling to 12-bit resolution at a 1-MHz rate; a two-channel, 10-MHz, 8-bit unit; and a single-channel, 50-MHz, 8-bit module. Each channel has its own independent a-d converter, time base, trigger, trigger delay, offset, automatic zero calibration, cursor, and reference-pointer generation. The 10-MHz front end can be used to capture a 5-MHz analog signal with 0.2% accuracy, says the firm.

Up to four channels, with their individual trigger circuits, can be set up to trigger on logical combinations of the input conditions, much like a logic analyzer. When a signal is applied to one of the 8612's inputs, the instrument automatically selects voltage and time ranges for viewing the signal. The setting can then be changed with the keyboard, to zoom in on or expand any interval of a trace.

Screen data. Besides as many traces as are practicable for viewing at once, several data lines are displayed. The first, a status line, indicates the time, date, and mode of the instrument (the measure or help mode, for example). The second line tells whether each channel is enabled or manually or automatically set. The third line shows the parameters (attenuation, sample rate, trigger level, and delay) for a selected channel.

A line is also written on the screen for each trace—in the color of the corresponding trace—with data including a label entered from the keyboard, as well as the individual amplitude and time differences between the points marked by the reference and the cursor. The last line appears at the bottom of the screen and indicates the current function of each of the seven soft keys, whose labels change for the input, trigger, and general menus, as well as for the measure and help modes. The help mode explains key functions for the menus and modes.

Controlling the 8612 are an Intel



8086 main processor, an 8089 input/output processor, and a bit-slice processor, based on the Advanced Micro Devices 2903, that controls the display. An optional 8087 arithmetic coprocessor is available for signal-analysis functions.

Storage. Each trace is stored in a 4-K-word memory in the input modules. The mainframe contains 32-K 16-bit words of memory, expandable to 160-K words. An optional floppy-disk drive permits traces to be stored for analysis and comparison.

With so much processing power and available memory, the 8612 is a very flexible scope. The waveforms displayed on the 320-by-256–picture-element CRT are not simply a representation of the data captured in the input modules' memories; the displayed traces are fully computed waveforms. For example, four different views of one trace can be stored and displayed on screen as four separate traces, each with different scales specified, or they can be patched together into one long trace. Two sets of captured data can be combined with Boolean functions and displayed as one waveform. Traces can be swapped in and out of the screen memory with a few keystrokes.

The scope also executes 20 programmable functions such as might be found on a digital multimeter. In an automated test setup, therefore, the scope can take such measurements as true root-mean-square or peak-to-peak voltage, maxima and minima, and signal frequency, performing the required processing locally before sending the results out on the optional IEEE-488 bus.

Test setups can be stored on floppy disks or in an internal electrically erasable programmable read-only memory. Other available options are an RS-232-C interface, an 8-bit Centronics-compatible parallel port, and a red-green-blue video output.

Available in January 1984, the Digiscope 8612 mainframe sells for $14,000. Like the floppy-disk drive, each plug-in costs $3,000.

Test & Measurement Systems Inc., 1094 Robbia Dr., Sunnyvale, Calif. 94087. Phone (408) 773-1208 [Circle reader service number 401]

Modules adapt field-service computer to wide range of digital test situations

The ever-increasing complexity of microprocessor-based products and the rising density of logic circuits call for more and more sophisticated digital test and measurement systems. But such units have turned into unwieldy stationary setups, becoming prohibitively expensive and harder for the technician to use. Seeking a way out of this dilemma, Dolch Logic Instruments Inc. has developed the Colt (for compact logic tester) 300, a low-cost portable instrument designed mainly for use in production, quality control, and, above all, in the field.

"With our Colt, we are aiming at mobile service applications where there is a growing need for intelligent and easy-to-use logic testers," says Volker Dolch, chairman of the firm. "But that does not rule out its use in other areas." Provision has been made to adapt it to research and development work.

Colt is based on the same plug-in module technology that Dolch uses in its Atlas (for adaptive test and logic analysis system) engineering work station introduced last year [*Electronics,* Oct. 20, 1982, p. 235]. In fact, Atlas modules may also be used in the Colt.

A number of plug-in modules make the new tester act as either a logic analyzer, word generator, or in-circuit emulator for general-purpose software and hardware testing or for 8- and 16-bit dedicated microprocessor work. The logic-analyzer modules come with 48 input channels, each sampling at 10 or 20 MHz, with thirty-two 100-MHz channels, or with sixteen 300-MHz channels.

Other modules turn the Colt into a signature analyzer, in-circuit tester, or microprocessor development tool. There are more than 20 modules available, with additional ones in design, covering the whole range of applications from production and service to research and development.

Uncommitted. Also inherited from Atlas is the Dolch architecture for logic-testing systems, in which the modules are front ends for a computer-based mainframe. "By keeping the mainframe uncommitted and separate from the front ends, the mainframe retains all the computing power and the modules can be kept simple," says Dolch. "Small hardware changes suffice to adapt the modules to a new test environment."

For the sake of compactness and portability, Colt has only one slot for the plug-in modules (compared to two for the Atlas). Also, the keyboard is integrated into the front panel instead of being external. However, if the instrument is to be used for stationary work or for more elaborate tasks, an optional external alphanumeric keyboard or an extension chassis, which accommodates

The heavy-duty connection.

From earthmovers to transports to tanks, heavy-duty-transportation applications are difficult and dirty. Shock, vibration, salt spray, mud, brake fluids, coolants and temperature extremes all take their toll. And call for more than standard electronic interconnects can deliver.

To cope with environmental extremes, ITT Cannon works with leading heavy-vehicle manufacturers, using our experience and resources to help define their needs and develop solutions. Cannon is looking to apply this expertise and resourcefulness to meet the rapidly changing requirements of the future and find solutions to new problems.

Cannon's VE, CA and CA Bayonet Series, Sure-Seal,® Standard K, Standard Circular and Microminiature connectors were the result. And are now setting the standards for performance in heavy-duty transportation. All cost less to buy and less to use. And are proving themselves in thousands of heavy-duty vehicles every day.

Electronic solutions are being called upon more and more to keep wheels rolling efficiently and economically.

And Cannon is there with circular connectors providing high performance. While our fiber-optic and filtered-pin connectors are providing economy and reliability by preventing system malfunction due to EMI/RFI.

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We also have custom capabilities for all your non-standard heavy-vehicle requirements.

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Please send for our free Heavy Vehicle Connector Selector Guide. And find out more about Cannon® Connectors complete product line for the heavy-duty connection. Contact ITT Cannon, a Division of International Telephone and Telegraph Corporation, 10550 Talbert Avenue, Fountain Valley, CA 92708. Telephone: (714) 964-7400. In Europe, contact ITT Cannon, Avenue Louise 250, B-1050 Brussels, Belgium. Telephone: 02/640.36.00.

CANNON ITT
The Global Connection

Circle 183 on reader service card

two plug-in modules, can be added.

The mainframe uses a Z80 central processing unit running under MP/M, a multiuser multitasking operating system. "We chose that system because it has become a quasi-industry standard for personal computers," Dolch says. The instrument comes with 64-K bytes of random-access memory, two double-sided, double-density 5¼-in. floppy-disk drives, and a 5-by-9-in. cathode-ray tube.

Drawing on the know-how it has acquired as a builder of programming systems for erasable programmable read-only memories and programmable logic arrays, Dolch has designed two modules that turn the Colt into a development tool for R&D. One module programs any E-PROM, and the other covers almost the entire range of PLAs.

Burn and test. Apart from the plug-in modules, the Colt has special test probes that make it an efficient in-circuit tester for field service. As such, it should come in handy when circuit boards or systems with PLAs are tested. If the PLA elements were previously programmed with Colt, the system can store all relevant data and use it for verification.

There are several advantages to Colt in-circuit tests. For one thing, the PLAs are checked in their natural environment, so errors caused not only by the chip itself but also by the pc board or soldering joints can easily be localized. For another, read-protected PLAs can be tested without the user knowing their logic content. Also, the in-circuit tests call for no expertise, so the tests may be run by untrained personnel in production and service applications.

The Colt can be used either as a stand-alone unit or as part of a test-equipment setup. Its software compatibility with Atlas and other Dolch logic analyzers allows the user to set up powerful system hierarchies. Access to the Colt via phone line makes flexible service strategies possible.

The price for the Colt mainframe and a relatively simple plug-in unit is less than $10,000. The plug-in modules sell for between $2,000 and 5,000 each, depending on function.

The instrument, to be introduced at the November 9–15 Interkama exhibition in Düsseldorf, West Germany, in addition to Wescon, will be available immediately following these events. Delivery time is 60 days.

Dolch Logic Instruments Inc., 230 Devcon Dr., San Jose, Calif. 95112. Phone (800) 538-7506 [Circle 339]

Dolch Logic Instruments GmbH, Justus-von-Liebig-Str. 19, D-6057 Dietzenbach, West Germany [Circle 402]

Two-channel logic scope and analyzer weighs ½ lb, fits in user's pocket

The use of the cathode-ray tube makes conventional oscilloscopes, even so-called portables, into large, line-powered instruments. But a logic scope that uses linear arrays of light-emitting diodes can fit in a jacket pocket and run for about an hour on a 9-V battery.

The 8.25-by-4-by-1.5-in. model 136 Logicscope is actually a combination scope and logic analyzer that weighs about ½ lb, including rechargeable battery. Vic Ivashin, vice president for engineering at Pocket Technology Inc., says: "It has the pulse performance of a 10-MHz scope—it can measure pulse widths down to 100-ns duration and detect glitches between 50 and 100 ns."

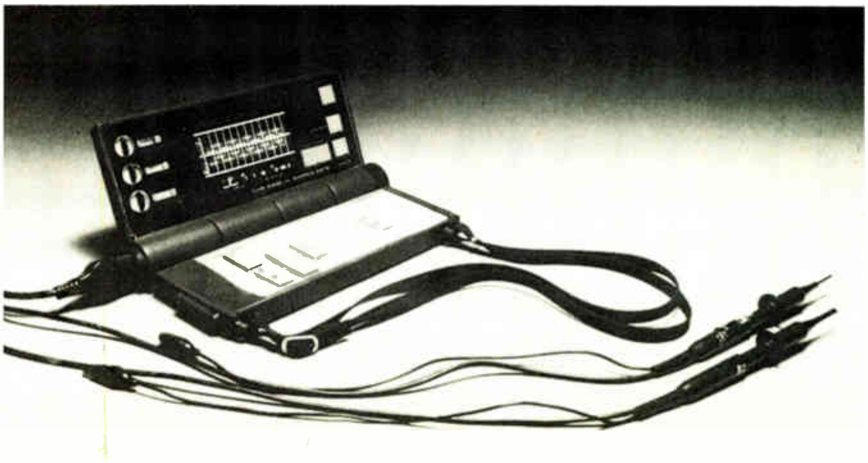
The unit displays pulse waveforms on two rows of 100 LEDs each. It is a dual-channel scope, so it has four parallel rows of LEDs. Sixteen additional status LEDs indicate functions and setups. Because the display consists only of high and low levels for each trace, Ivashin points out, the 136 is designed to look at logic signals, not complex analog waveforms. "But how many times have you wished that you had a scope in your pocket when you were crawling in the back corner of a computer, especially one with a bright LED display that could easily be seen in that dark corner?" he asks.

Like conventional scopes and logic analyzers, the 136 has such features as trigger, single-sweep, logic-compare, free-run, memory, reset, recall, and write facilities. The logic-compare function makes it possible to compare two traces with a logical AND, OR, or exclusive-OR function.

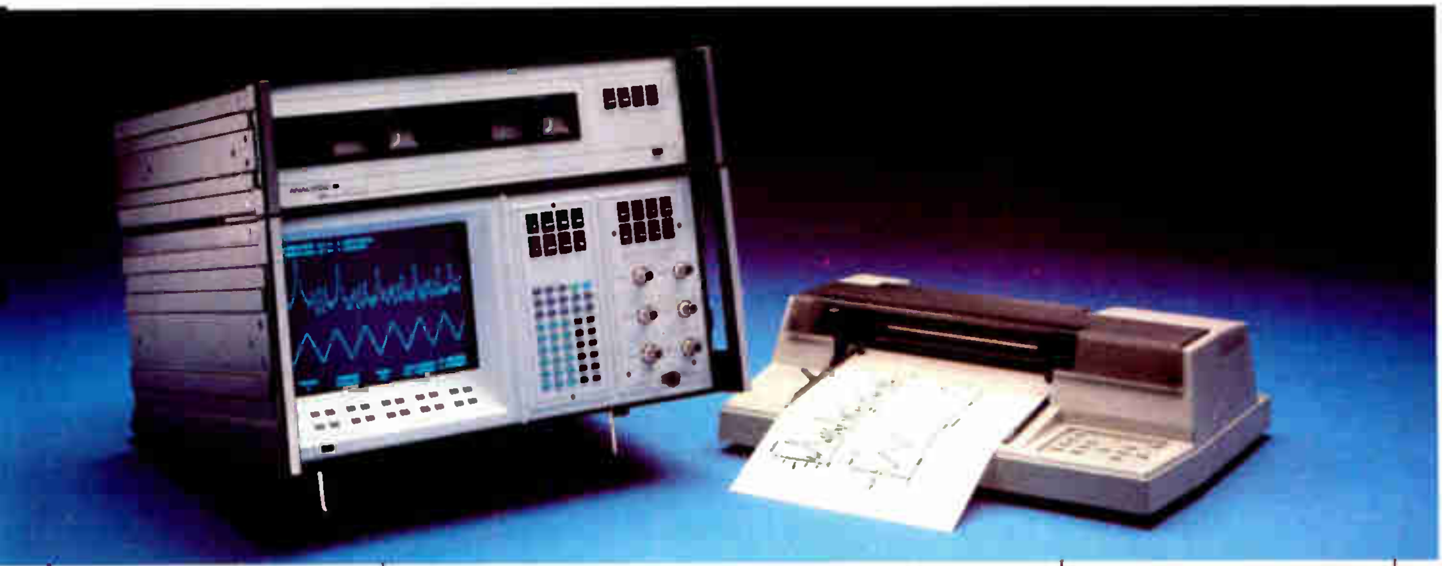
To pack all this into a small package, Ivashin turned to custom complementary-MOS chips, four in all, plus C-MOS memories. The display's LEDs consume most of the power, but, says Ivashin, "most things the scope would be used on are line-powered, so we provide a transformer adapter-charger for the unit and believe that it will be plugged in most of the time it's used."

The four custom integrated circuits are a display controller, a master timing processor, a synchronization and trigger circuit, and a keyboard and memory controller. C-MOS gates act as probe buffers. "We put these buffers in sockets, so just in case the user decides to put the probe in the high-voltage cage, they are easily replaceable," says Ivashin.

Automatic time base. Three probes are provided, one for each trace and one for an external trigger. Sixteen internal registers store and recall waveforms from either trace. "With the input/output controller and a



Data 6000 Universal Waveform Analysis System.



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Data Precision announces an important advance for everyone who wants to know anything about a waveform: the Data 6000 Universal Waveform Analyzer is now a complete system. Major enhancements to the Data 6000's storage, analysis, and display capabilities have extended its usefulness far beyond anything previously available for the price — or for any price. And the entire system is now deliverable in just 30 days.

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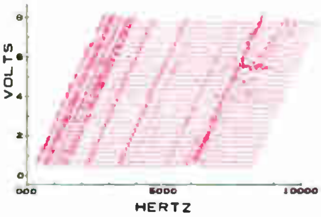

Time series history of rotating machinery run-up

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See us at WESCON, Booth numbers 726-734

Circle #184 for demonstration
Circle #185 for additional information

port we provide, waveforms can be sent to an external system for analysis and display," he adds. The 136 has a few more unique features: for instance, an automatic seek function, which automatically adjusts the timing to fill the display with one complete waveform cycle. "This eliminates having to 'guesstimate' the correct time-base setting for an unknown signal," says Ivashin.

The 136 also has an audio signal that can help in trouble-shooting logic. The scope may be set to capture a single event and to emit a tone when it occurs, eliminating the need to keep an eye on the display. It may also be used to differentiate among three different logic states. A low tone indicates a logic low; a high tone a logic high; and no tone an open circuit.

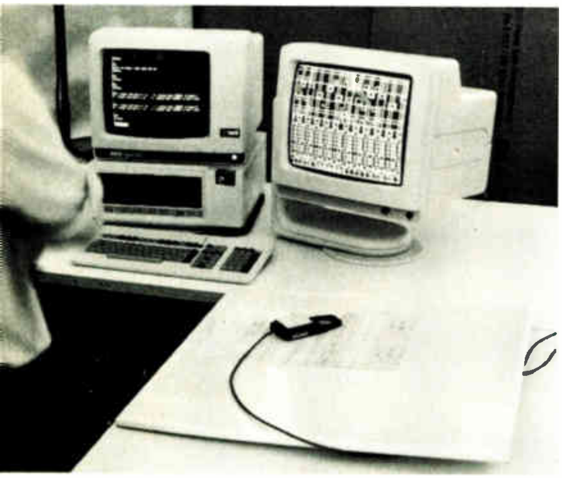
The Logicscope comes complete with probes, adapter, and carrying case. It sells for $495. Shipments will begin in January 1984, and a series of options, including a signal-analysis module and a timing readout module, are to be introduced in 1984.

Pocket Technology Inc., 1095 Shary Circle, Concord, Calif. 94518. Phone (415) 676-5757 [Circle 403]

Development-system work station grows into computer-aided design system

It is unnecessary to start big when getting into computer-aided engineering for electronic system design. Kontron Electronics Inc. is introducing a modular CAE system that offers a low-cost entry into the world of individual design work stations with the opportunity to grow in features and functions as needed.

The user of the Micad hardware and software system can start with a computer-aided design system for printed-circuit boards and for gate arrays in the form of inexpensive work stations that tie into larger computers. Then, later on, he or she can add more hardware and software to create work stations with more design and analysis capability and less reliance on a large central host.



Underlying the system is a Z80-based microcomputer with 256-K bytes of memory running version 2.2 of the CP/M operating system. Kontron's current KDS980 development-system work station has either two 5¼-in. floppy-disk drives or one floppy- and a 10-megabyte hard disk, plus a 15-in. monochrome monitor. A complete Micad 980 system is the same microcomputer with two monitors—a 17-in. graphics monitor with a resolution of 1,024 by 768 picture elements, and a 15-in., 25-line-by-80-character data monitor. The graphics subsystem is supported by a 7220-based graphics processor and 128-K-byte display memory. There is also a 280-by-280-mm digitizing tablet with 0.025-mm resolution.

Besides system software, the Micad 980 comes with digitizing software, an interactive cell-layout program for pc boards, whether two-sided or multilayer types, and a symbol library of most 74XX-type devices. Also, the Micad 980 system has interface software for a plotter and communication to a more powerful central computer, such as a VAX-11/780, for memory- and computation-intensive functions like simulation and design-rule checking.

For gate-array design, the Micad 980 has programs and libraries to support complementary-MOS and emitter-coupled-logic gate-array families from several of the popular international gate-array suppliers.

The complete Micad work station with the hard disk, both graphics and data monitors, plus digitizer and software for circuit-board and gate-array design, is priced at $25,000. The $15,500 hard-disk version of the KDS980 work station can be upgraded to the complete Micad 980 configuration for $10,500. All models are available for delivery 60 days after receipt of order.

Next step. Kontron will be offering a more advanced Micad model with a Motorola 68000 processor board, memory-expansion boards, and a Unix operating system. The Micad 968 upgrade will be introduced at the 1984 Electro show.

The 68000-based Unix upgrade will allow the offloading of some of the processing- and memory-intensive work from a central computer to the work station. Packages under Unix will be available for worst-case logic and timing simulation for circuit boards or gate arrays, automatic placement and routing analysis for both circuit types, automatic routing for C-MOS gate arrays, design-rule checking and pattern generation for gate arrays, automatic test generation, and fault simulation.

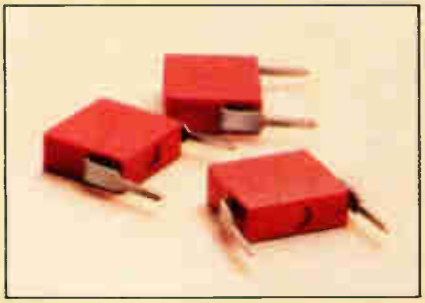
Kontron Electronics Inc., 630 Price Ave., Redwood City, Calif. 94063. Phone (415) 361-1012 [Circle 477]

Software creates relational data base of hierarchical design drawings

In the field of computer-aided design, the high-powered equipment dedicated to very large-scale integrated circuits tends to garner the lion's share of attention. But the time and cost savings offered by CAD can also

New laser technology shrinks TRW 80 Series film capacitors to ceramic size.

Small Wonder.



Now laser-generated metallized winding produces a high-capacitance metallized film capacitor in an ultra-small package.

Introducing TRW's new Micro Thin Gauge Series 80 capacitor. A cost-effective way to improve products and flatten the failure curve.

Utilizing microprocessor controlled lasers, TRW bonds and prints the new MTG Series 80 capacitor to extremely close tolerances. The metallized winding process using lasers is licensed from AT&T. The Series 80 is also more stable with time and voltage, and has a dissipation factor 2.5 times better than ceramics, with dielectric absorption 5 times better. And if it fails, it fails open; not short. Plus, the capacitance change with temperatures is 480% better than X7R and 900% better than Z5U.

This new MTG capacitor actually has the same footprint as a DIP ceramic and serves as a direct replacement. The metallized film is self-healing for overall reliability.

With improved electrical characteristics, reliability, and quality when compared to multilayered ceramic capacitors, our Micro Thin Gauge capacitor is a *small wonder.*

Contact us to learn more. TRW, Capacitor Division, 301 W. O St., Ogallala, NE 69153. (308) 284-3611.

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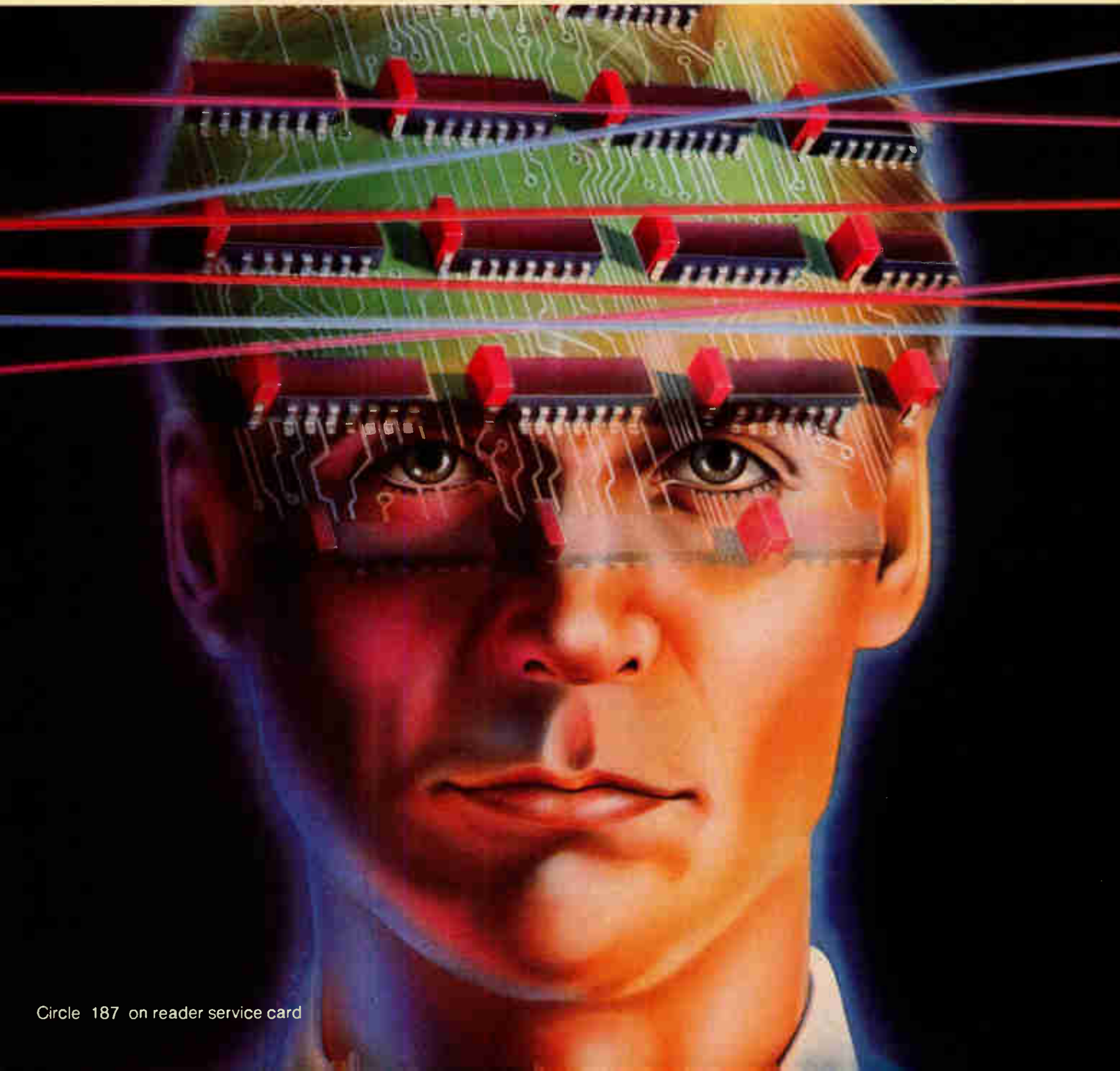

Circle 187 on reader service card

accrue in significant amounts when applied to less glamorous engineering tasks, an example being the ubiquitous and tedious chore of creating and updating the voluminous documentation in any complex program.

FutureNet Corp. is targeting this common task with software that works with its established Dash-1 schematic-design work station. Called Strides (for structured interactive design system), the package simplifies management of up to 99 hierarchical levels of documentation, according to Terry A. Zimmerman, vice president of marketing. It lets a user create a relational data base of schematics and the assorted lists generated during design work.

Changes to any document in the data base's tree are carried automatically throughout the design, affecting all relevant drawings. The FutureNet system thus can manage a large body of documentation from the top block diagram all the way down to individual components, including VLSI equivalents at the gate-array or chip level, points out Zimmerman.

Deeper into detail. The user first defines block-to-block relationships between system elements. At the highest level, for example, a single block displays itself on the screen; on the next level, interconnections appear; and at successively lower levels, finer details emerge as they are selected with single key strokes.

Moving from level to level within the hierarchy of drawings requires only positioning a cursor on the desired part and pressing a function key for upward or downward movement. Changes made at each level are temporarily saved for final checking until the final system-change execution is ordered. Within a drawing level, details may be selected for viewing or editing until one command captures all edited changes and clears all temporary files.

The FutureNet work station, introduced last year [*Electronics*, Dec. 29, 1982 p. 89] consists of an IBM Personal Computer (or the XT version) with a Dash-1 package, which includes design software, a graphics controller board, and additional memory and communications hardware. The price is $5,980 and $6,280 for the FutureNet products alone, or $12,960 and $14,955 for turnkey systems that include printer and mouse. The Strides package costs $1,900 and comes with a part that effects a minor hardware change to programmable array logic in the graphics controller.

Strides is offered separately from the Dash-1 work station because not every user needs it. It is especially cost-effective, says Zimmerman, in large projects. It should appeal to any manager who has ever "suffered through the delays of manual documentation systems," he claims. "A change on an 8-bit latch chip typically ripples through enough drawings alone to pay for Strides."

FutureNet Corp., 21018 Osborne St., Canoga Park, Calif. 91304. Phone (213) 700-0691 [Circle 406]

Stand-alone in-circuit emulators debug 68008- and 68010-based systems

Stand-alone in-circuit emulators for Motorola's 68008 and 68010 augment Applied Microsystem Corp.'s

ES-series emulators for 16-bit microprocessors. The 68010's virtual-memory–management features make emulation particularly difficult, and the firm's unit is one of the first to arrive.

The ES-series emulators are used to debug and test software and hardware during their design, integration, and manufacturing phases. Emulators are also available for the 68000 and Zilog's Z8001 and Z8002.

Real time. To give the user an accurate picture of how the software interacts with the system under development, these emulation systems are designed to change the tested system's operating parameters as little as possible. The two new emulators run at 10 MHz, fast enough to emulate available versions of their respective microprocessors at full speed. This real-time capability makes it easier to isolate timing errors.

All ES-series emulators can accommodate up to 512-K bytes of overlay memory, mappable in blocks of 2-K bytes over the entire address space of the processor under test. Each emulator's trace-memory buffer measures 2,046 by 72 bits.

An in-line assembler and a memory disassembler are standard. Options include a symbolic debugging capability, a logic-state-analyzer probe, and the desired amount of overlay memory.

A basic emulator for the 68008 or 68010 including the pod assembly is $9,950. Deliveries will begin in January.

Applied Microsystems Corp., 5020 148th Ave. N. E., P. O. Box C-1002, Redmond, Wash. 98052. Phone (206) 882-2000 [Circle 480]

PROM burner works with microcomputer

With new programmable memory and logic devices appearing almost weekly, designers have a hard time keeping track of which adapter or personality module to use with what algorithm on which programmer. A universal programmer controlled by CP/M-based software running on a personal computer ends the confusion. The model 160 programs all types of memories and logic integrated circuits of up to 40 pins at present

The data acquisition system instrument users have been waiting for.

Gould's new IBM PC* based DASA 9000.
DASA 9000 starts with a flexible front-end signal conditioner that offers superb high speed multi-channel capability. Each channel has ⅓ MHz/s sample rate, 50 kHz bandwidth, and IEEE 488 compatibility. With DASA 9000 you can acquire up to 112 channels of high frequency data with signal acquisition independent of the computer. This frees the computer to do what it does best—to process and display data.

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It features high speed graphics processing, IEEE 488 interface, 16 bit architecture and an optional 8087 co-processor. And our menus make test set-up simple and fast.

Simplicity of an instrument.
DASA 9000's software package lets it work like an instrument. The keyboard, display and user are integrated into an interactive system. DASA 9000 employs the MS-DOS* operating system and BASICA* for applications programs.

More software to come.
To make your job easier, we're developing a broad selection of calculation and analysis software packages, such as FFT routines for multi-channel spectral analysis, signal processing packages and others.

For more information on DASA 9000, contact, Gould Inc., Recording Systems Division, 3631 Perkins Avenue, Cleveland, Ohio 44114. Telephone (216) 361-3315.

Nobody else comes close.

GOULD
Electronics

Circle 189 on reader service card

and up to 96 pins in the future.

Developed by Valley Data Sciences Inc., the 160 universal programmer employs software instead of hardware to control the algorithms for writing data into programmable read-only memories, erasable PROMs, electrically erasable PROMs, programmable array logic, and Signetics' integrated fuse logic. The complete system includes a programming station with two zero-insertion-force sockets (one for devices of up to 28 pins and one for 40-pin ICs), an interface card that plugs into the personal computer (whether an IBM Personal Computer, an Apple IIe, or a Zenith Z-89), and the software on floppy disk, called LogiSoft for logic devices and MemSoft for memories.

According to executive vice president Martin Cohen, "there are two major trends taking shape in digital systems relating to programmable logic and memory. First, more and more products are coming to market with PROMs and E-PROMs instead of ROMs—they give the designer more flexibility and eliminate outdated ROM inventory. Second, the use of PLAs [programmable logic arrays] is growing rapidly, with new high-speed and low-power devices being introduced at a steady rate. When you combine these with the fact that PLA-design software is now available for personal computers, it makes sense to have a PC-based memory and logic programmer." And the 160 can also be used to program microcomputer chips that contain on-chip PROMs or E-PROMs.

Besides making more sense for the designer, since both design and programming can be controlled by the one system, the 160 streamlines the user interface. A "menu-driven programmer with simple single-stroke keyboard commands is much easier to use than a dedicated programmer with cryptic commands and a small light-emitting-diode display, to say nothing about the problem of trying to find the right personality module when you need it," adds Cohen.

Both the software and hardware of the 160 contribute toward its ease of use. The software contains all of the necessary programming algorithms and device data bases on floppy disks. According to Cohen, "with a unique code-packing scheme, we can store the information for almost 2,000 device types on a single floppy disk." The company also has a software subscription service through which customers receive updated disks when new programmable devices become available.

Aided by the menu-driven software, the user first selects the device to be programmed and then enters some device parameters. Selectable programming options include program, read, verify, check, and quick erase for EE-PROMs. Nonprogramming options include display or edit, move, fill, save, and load. "Most operations require only a single keystroke and the user is guided through the programming process by self-prompting messages in plain English," Cohen points out.

And because of the computer's full-sized cathode-ray-tube display, the editing function is particularly troublefree. "The logic screen editor displays the complete matrix of input lines and product terms, and our proprietary Rosetta screen editor displays the complete contents of a memory device," says Cohen, "allowing quick changes to the fuse map."

Smart socket. The 160's hardware consists of an interface card that plugs into the computer and the 160 programming station with the power supplies and digital-to-analog converters that supply the signals to the programming socket. "This configuration gives us two advantages," says Cohen. "One is that we have a 'smart socket' and don't need different personality modules to adapt to different devices, and the other is that we automatically calibrate the d-a converters each time a device is selected for programming."

The 160 is available with or without the computer. Without the computer, it sells for $4,995 with MemSoft; with LogiSoft it is $4,495, and with both, $5,495. The software updating service adds $400. A typical turnkey system, including a Zenith Z89 computer, the 160, and both software packages, sells for $7,195. New orders will be delivered during the first quarter of 1984.

Valley Data Sciences Inc., 2426 Charleston Rd., Mountain View, Calif. 94043. Phone (415) 968-2900 [Circle 404]

Software-configurable programmer uses development system's terminal

Making use of programmable pin drivers and a plug-in firmware data base of up to 1,000 parts, the Omni 64 programmer for programmable read-only memory handles virtually every programmable bipolar and complementary-MOS device currently in production, including gate arrays, programmable logic arrays, and electrically erasable PROMs. There are no personality modules or socket adapters to change when switching from one family of devices to another.

Unlike most programmers that use a hexadecimal keypad and a cryptic one-line display, the Omni 64 employs a development system's cathode-ray tube for the user interface. This makes possible full-screen cursor-controlled editing (in multiple formats) and an on-line help menu to eliminate the reference books needed

to operate most programmers.

The Omni 64 is placed between the development system and its terminal. When the programmer's on-line key is selected, the main menu appears on the CRT. The user is presented first with an alphabetical list of all semiconductor manufacturers and then, for the one selected, with a complete catalog of parts, complete with part number, manufacturing process, and configuration. All read-compatible parts are listed on the CRT, so that a user who has just decided that the part chosen, say, consumes too much power can at once pick another.

Select and go. When the part to be programmed is selected, the programmer automatically configures all 64 programmable pin drivers to test, read, and program the part. Concerns about programming voltage, intelligent algorithms, rise and fall times, or any other programming parameter are eliminated. The Omni 64 selects the correct fast algorithm even when the part numbers are the same but the manufacturers are different. The Omni 64 comes with a 48-pin and a 64-pin socket.

Four library cards that plug into the programmer suit it to individual needs. A user who programs only MOS E-PROMs and EE-PROMs will need the Omni-Pack I library card; to this, the Omni-Pack IV adds bipolar memories and logic arrays.

The Omni 64 with one high-voltage programmable–pin-driver module (each pin driver is capable of sending power to eight pins simultaneously) and the Omni-Pack I sells for $2,850. With four high-voltage programmable–pin-driver modules and the Omni-Pack IV, it goes for $6,425. An optional subnanosecond timing generator and a precision reference module equip the Omni 64 with both ac and dc parametric testing capabilities.

Delivery of the programmer with the Omni-Pack I will begin next month, with Omni-Pack II to follow shortly. The company is currently adding about six parts a week to its library and expects to be able to deliver the programmer with the Omni-Pack IV sometime in February.

Oliver Advanced Engineering Inc., 676 West Wilson Ave., Glendale, Calif. 91203. Phone (213) 240-0080 [Circle 410]

10-bit analog-to-digital converter is fast, interfaces with processor

Unaided by external components, the monolithic AD573 analog-to-digital converter interfaces directly with 8- or 16-bit microprocessors in high-speed data-acquisition, process-control, and instrumentation gear. The unit, which takes a maximum of 30 μs for a 10-bit successive-approximation conversion, easily outruns any similar part on the market, yet sells at prices comparable with current commercial offerings, says Analog Devices Inc., its developer.

On-chip three-state output buffers, controllable by means of high- or low-byte–enable inputs, let host microprocessors read the AD573's 10-bit output as either a full 10-bit word or as two words of 8 and 2 bits each. The converter also incorporates a temperature-compensated buried-zener reference, successive-approximation register, comparator, and clock. Available in two commercial grades and a military version, the AD573 accepts unipolar inputs of 0 to +10 V or bipolar inputs of –5 to +5 V.

No missing codes. The higher-performance commercial version of the AD573, operating at from 0° to 70°C, and the –55°-to-+125°C military model both have relative accuracies guaranteed at ±½ least-significant bit over their respective temperature ranges. Both models also guarantee performance with no missing codes in 10-bit operations over their temperature ranges. The lower-performance AD573 commercial model guarantees accuracy to ±1 LSB, and no missing codes at the 9-bit level.

Maximum initial gain error in all versions of the AD573 is ±2 LSB; unipolar and bipolar offsets are a maximum of ±½ or ±1 LSB in the commercial grades and ±1 LSB in the military model. Over their operating temperature, the commercial models hold gain error to ±2 or ±4 LSB; their maximum offset error is guaranteed at ±1 or ±2 LSB. In the military version, the AD573's maximum gain and offset error specifications are ±5 and ±2 LSB, respectively.

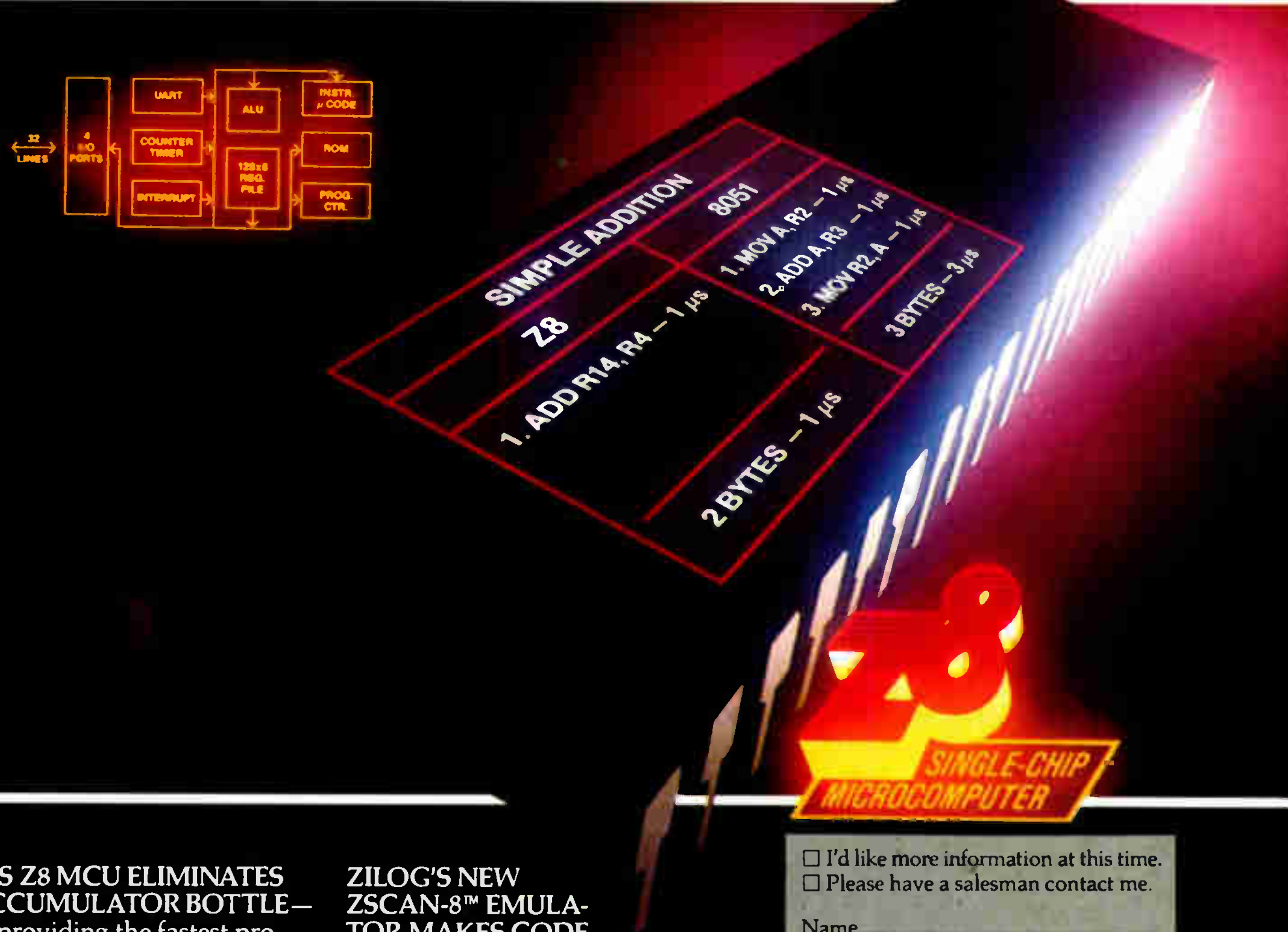
Operable with either +5- and –15-V or with –12-V power supplies, the AD573 comes in a 20-pin dual in-line package. Commercial models, available in plastic or hermetically-sealed ceramic dual in-line packages, cost between $13.90 and $26.00 in lots of 100. The military-grade AD573 comes only in the sealed ceramic package, and costs $67.80 in hundreds; processing to MIL-STD-883B brings the part's price to $77.00. Delivery of all AD573 models is from stock.

Analog Devices Inc., Route 1 Industrial Park, P. O. Box 280, Norwood, Mass. 02062. Phone (617) 329-4700 [Circle 405]

Modem chip digs data out of noisy signal

Motorola Inc. hopes to ring up sales in business-application markets for 300-baud modems with a silicon-gate complementary-MOS modem chip that achieves a high data-recovery rate (only 1 error in 10^5 bits, typical-

Zilog's Z8® single-chip microcomputer gives you 30% more performance with 30% less code than the 8051.



ZILOG'S Z8 MCU ELIMINATES THE ACCUMULATOR BOTTLE-NECK, providing the fastest processing capability available in a single-chip microcomputer. The Z8 MCU's general-purpose register architecture operates on data directly in registers or ports, eliminating the need to first move data to the accumulator. As shown, a simple addition in the Z8 MCU requires only one instruction and executes much faster than Intel's accumulator-oriented 8051. In most applications, the Z8 MCU operates at least 30% faster, with 30% less code!

This device has other advanced features, including 128 bytes of RAM and 4K bytes of ROM, hardware port handshake, a UART and two counter/timers.

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ly) despite noisy signals (an incoming signal-to-noise ratio of 0.5 to 1 dB).

To do this, the MC145445 employs a technique known as differential-delayed detection that uses what the firm calls a semi-phase-locked loop for demodulation. In addition, the 22-pin modem chip—which is compatible with Bell 103 and 113 and the Consultative Committee on International Telegraphy and Telephony V.21 standards—has eight selectable clear-to-send delay settings, providing a range of delays from 0 to 426.6 ms.

"If the modem is working over long-distance lines, you don't want the system to drop off when it encounters a signal delay. So, you may select the longer delay times, which will allow it to recover without losing clear-to-send," says Al Mouton, product planning manager for telecommunications. The clear-to-send delay may be selected by a 3-bit code on three pins, allowing eight different settings.

The 145445 is targeted at a range of business applications, including automatic-teller machines and 300-baud office communications, states Mouton, adding that these markets require much lower error rates than the typical consumer system. Motorola is serving the consumer market with the MC14412 modem chip introduced earlier; it has fewer on-chip features and carries a lower price tag, $3.46 each in 1,000-unit lots.

In 1,000-piece quantities, the 145445 modem sells for $8.47 each in a plastic dual in-line package. Production lots are available for immediate delivery.

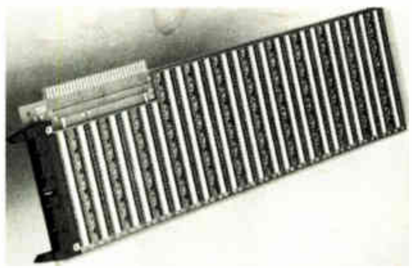
Companion filters. The modem is intended to be teamed up with Motorola's recently announced C-MOS bandpass switched-capacitor filter chips: the MC145440 for U. S. Bell standards, and the MC145441 for European CCITT V.21 formats. The 18-pin filters are slated to enter volume deliveries in December. In 1,000-piece orders, the 145440 costs $8.46 each, and the 145441 is $9.36.

With these filters, the modem chip set is capable of driving +9 dBm into a 600-Ω load; it operates from a single ±10% power supply of 5 V. On-board voltage-reference circuitry also allows the devices to use a split supply. The 145445 uses a 3.6864-MHz clock crystal and has a power dissipation of 25 mW typical, 125 mW maximum and has an operating temperature range of 0° to 70°C. The 145445 also has a carrier-detect input and answer-back tone generator.

Motorola Inc., 3501 Ed Bluestein Blvd., Austin, Texas 78721. Phone (512) 928-6892 [Circle 408]

Prototyping board fits slot in IBM PC

A wrapped-wire socket board that fits in one of the expansion slots of an IBM Personal Computer accommodates up to 86 16-pin chips and



offers the plug-in component replacement, simple rewiring, and rapid design turnaround that can make such socket panels an attractive alternative to printed-circuit boards. Augat Inc., a pioneer and market leader for this type of product, adds the board to a wide product line whose best-sellers to date have been for the Intel Multibus and for Digital Equipment Corp. PDP-8 and PDP-11 systems.

A standard pc board for the IBM PC would hold up to 75 16-pin devices, according to George G. Bauserman, national sales manager for the company's Interconnection Systems group. And although socket panels are priced considerably higher than pc boards, Bauserman argues that they are actually more economical for short and medium-length production runs. They offer substantial time savings in production, he explains, do not require the generation of artwork, and can be modified far more simply and inexpensively.

Designed for input/output and memory expansion, the 13.2-by-4.2-in. IBM panel is fashioned of standard copper-clad glass-epoxy. Tapered gold sockets accept integrated circuits of 0.3-, 0.4-, 0.6- and 0.9-in. widths. The board's 0.025-in.-square tin- or gold-plated pins can be wired manually or automatically.

Machined. Augat emphasizes that its socket, which contacts the IC lead at four points, is machined, not simply stamped. Machined contacts, the company contends, are more reliable than the stamped inner sockets and soldered connections of conventional boards. Manufacturing specifications are to MIL-P-5510C, notes Bauserman. Moreover, IC reliability is said to be improved at higher temperatures because of the heat-dissipating qualities of the pins.

The four-cornered wrapped-wire posts are said to provide a tight wire grip. Point-to-point, as opposed to L-shaped, wiring results in shorter signal paths. The wrapped-wire pins may be wired at two levels, with three-level wiring panels available as an option at a 10% increase in price.

A 64-contact card-edge connector plugs the board into the PC's expansion socket. An SGH 50-pin header interfaces with a peripheral, with a second connector optional.

The 8136-HPG28-2 (with gold-plated wrapped-wire pins) sells for $367.25 in quantities of 1 to 4, $322 apiece for 5 to 9, or $292.50 for 10 to 24. In the same quantities, the 8136-HPG628-2TG (with tin pins) sells for $296, $259.50, or $237.75. Delivery takes three weeks.

Augat Inc., 33 Perry Ave., Attleboro, Mass. 02703. Phone (617) 222-2202 [Circle 476]

SMD controller has megabyte disk cache

Designing a large cache memory into a disk controller can substantially reduce the 30-ms average access time of Winchester Storage Module Drives. Advanced Storage Concepts has taken this tack with a controller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Circle 195 on reader service card

for 8- and 14-in. SMDs that communicates with the host via the Small Computer Systems Interface.

The ACS 800 controller board carries 1-megabyte of random-access memory for cache storage, cutting average access time to about 8 ms, assuming a 75% hit ratio.

A microprocessor (an 8088 to be upgraded to an 80188) controls the host and disk interfaces and oversees use of the cache by analyzing the host's requests. The RAM copies data from the disk and makes it available immediately on request.

The user can lock in the cache files that would normally be overwritten because of their inactivity. Writing, the less frequent operation, is done directly into the cache (a flag is set for written blocks); recording onto the disk is done either when the controller is idle or when new data is about to overwrite the block not used for the longest time.

A full implementation of the SCSI specification allows multiple requests to be queued. If a disk operation presents a long delay, the controller can disconnect itself from the bus, and accept another request—thus allowing concurrent or parallel servicing.

The disk-cache approach is particularly useful in Unix-based systems, which fragment file requests into multiple physical disk seeks. Other uses include computer-aided design systems, data-base–management installations, networked computers, and multiple-user systems.

Currently under development, the ACS 800 will be available early next year for under $4,000. A similar controller for 5¼-in. ST-506–type Winchesters carries 320-K bytes of cache and is priced at $1,995.

Advanced Storage Concepts, 8720 South Gessner, Houston, Texas 77074. Phone (713) 271-5140 [Circle 478]

Board adds I/O ports to S-100 system

The 8800GF2 board for the S-100 bus is aimed at highly input/output-oriented systems, such as those used

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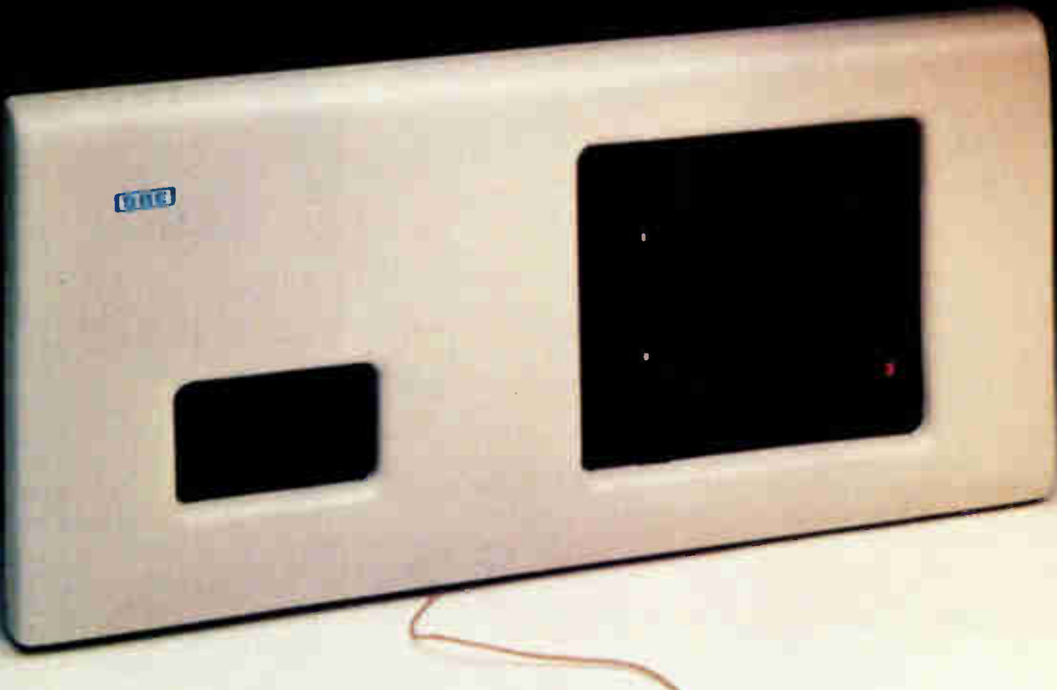

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Circle 197 on reader service card

New products

for data acquisition, machine-tool interfaces, and process control, as well as at ordinary small computers that must drive a number of printers. This board, which conforms to the IEEE-696 standard, provides three full-duplex parallel I/O channels, an RS-232-C serial port, and a selectable-rate interrupt timer.

Each of the three parallel ports incorporates eight latched TTL input lines and eight three-state output lines with 24-mA drivers. Additional lines offer strobe, enable, or attention signals with selectable polarity. The board supports data-transfer rates of up to 10 MHz, according to Floyd Hill, sales vice president of Vector Electronic Co.

A switch-selectable interrupt timer gives the board fixed rates from 50 to 19,200 interrupts/s. The basic rates may be reduced further by factors of 2, 4, or 8 via jumpers. Each parallel connector carries power for peripheral devices. The power available for all three connectors is 5 V at 200 mA and ±12 V at 50 mA.

Isolated. The serial port offers RS-232-C ±12-V signals or optically isolated 20-mA current-loop signals with an internal or external current source. In the RS-232-C mode, the board functions either as data-terminal or as data-communication equipment. Data-transmission rates may be selected from 50 to 19,200 baud, including a 134.5-baud rate for driving Selectric typewriters. Characters may be 7 or 8 bits, with odd, even, or no parity and 1 or 2 stop bits.

The 10-by-5.3-in. epoxy-glass circuit board is solder-masked on both sides and has gold-plated card-edge connectors. Power needs are 800 mA maximum at +8 V and 200 mA maximum each at +16 and −16 V.

The premium version of the Vector board is given a 200-h burn-in. It has a two-year warranty; direct exchange in case of failure is promised. The other assembled and tested version is burned in for 20 h and is offered with a one-year limited warranty for $325. The premium board is $399. Delivery is in two weeks.

Vector Electronic Co., 12460 Gladstone Ave., Sylmar, Calif. 91342. Phone (213) 365-9661 [Circle 407]

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Circle 199 on reader service card


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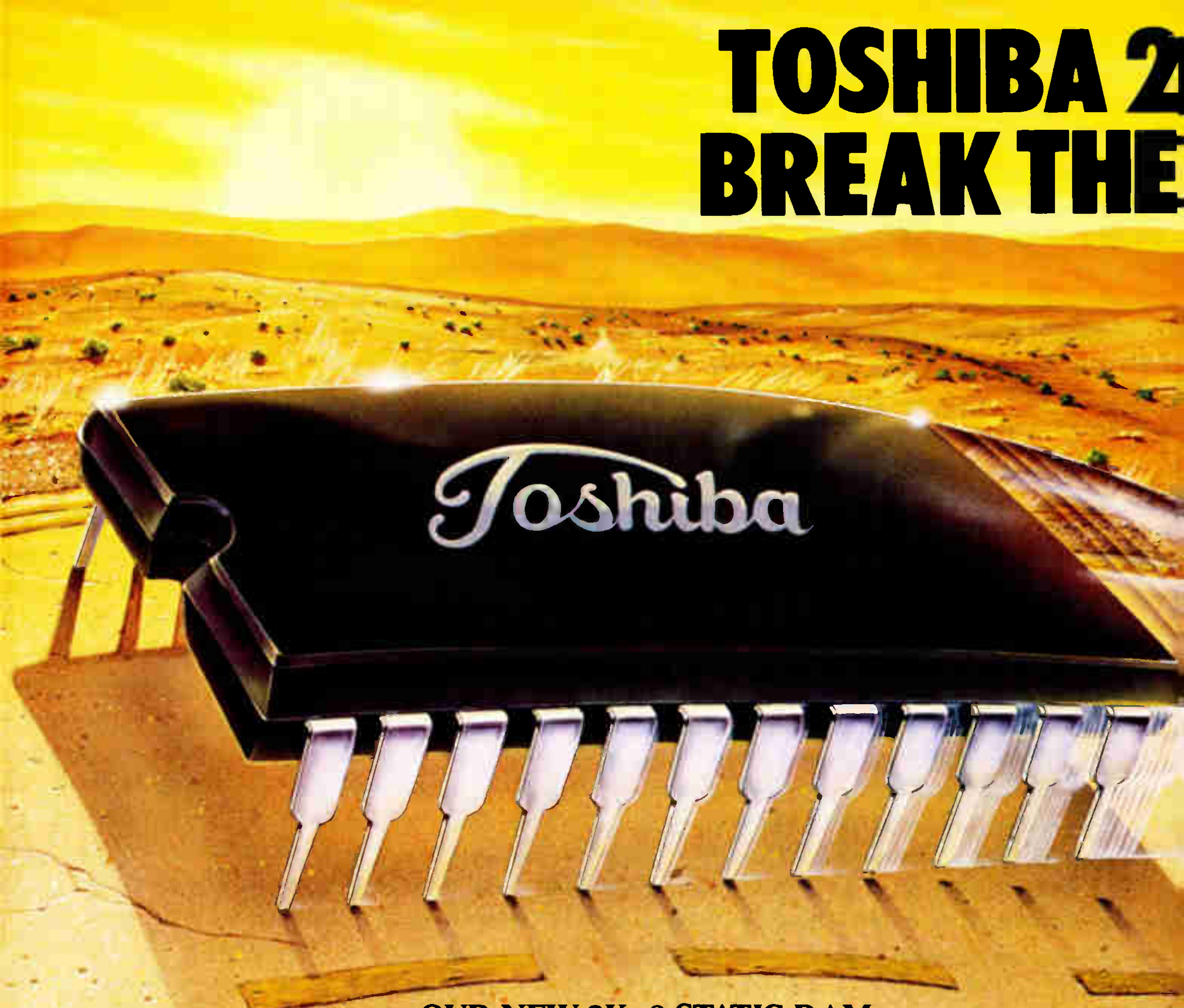

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*2016AP-9	NMOS	90ns	80mA	7mA
*2016AP-10	NMOS	100ns	65mA	7mA
*2016AP-12	NMOS	120ns	65mA	7mA
*2016AP-15	NMOS	150ns	65mA	7mA
**2018D-45	NMOS	45ns	120mA	20mA
**2018D-55	NMOS	55ns	120mA	20mA
5516P	CMOS	250ns	55mA	30μA
5516P-2	CMOS	200ns	55mA	30μA
5516PL	CMOS	250ns	55mA	1μA
5516PL-2	CMOS	200ns	55mA	1μA
5517BP	CMOS	200ns	25mA	30μA
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Circle 206 on reader service card

Station gets extensive graphics facilities

Microsystem line offers color and high-resolution monochrome graphics, versatile display software, upgraded Ethernet interface, file-server version

by Clifford Barney, Palo Alto bureau

Ever since Sun Microsystems Inc. introduced its very first 68000-and-Unix–based work station [*Electronics*, June 30, 1982, p. 139], it has been tweaking the design. The firm has already replaced the original microprocessor with the 68010—which supports a demand-paged virtual memory—enhanced the AT&T Bell Laboratories' operating system, added a mouse and windowing software, and upgraded to a high-speed Ethernet network interface.

Now Sun has pulled together all these improvements and bundled them with a high-resolution bit-mapped display or a color-graphics unit, improved network and input/output interfaces, and additional hardware and software. The new system is called the Sun 2.

The Sun 2/120 is a high-performance work station with a noninterlaced 19-in. display of 1,152 by 900 picture elements and up to 4 megabytes of high-speed random-access memory. The Sun 2/170 is a rack-mountable file server for large networks. The 2/120 comes with a deskside pedestal unit containing the power supply, a 5¼-in. Winchester disk with ¼-in.–tape backup, and a nine-slot Multibus card cage. The 2/170 has no display but does have a bigger power supply and a 15-slot Multibus cage.

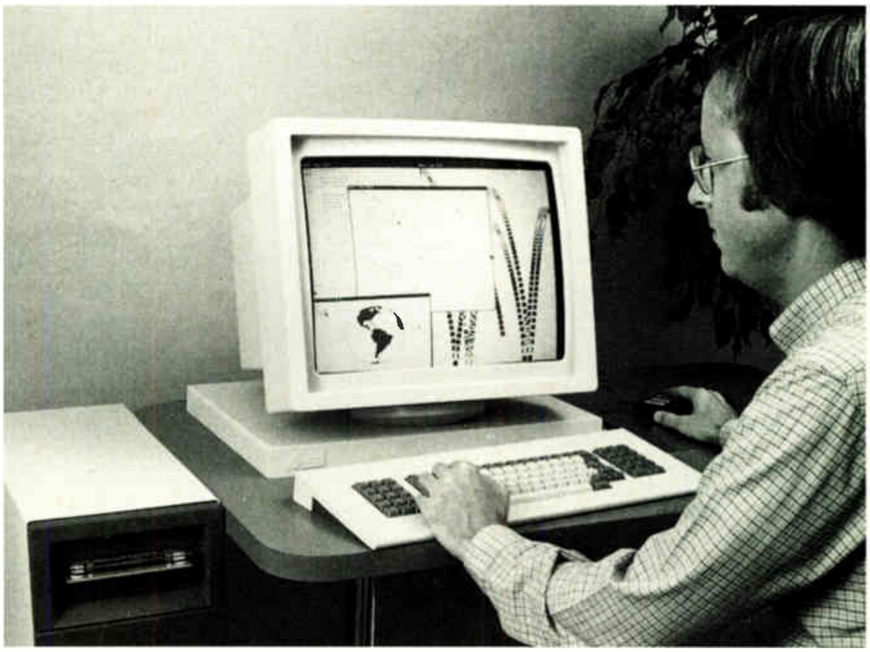
Sun's high-performance microsystem, apparently on the wish lists of many technical professionals, has attracted dense crowds at a number of trade shows. What is now called the updated Sun 1 system, organized around a 10-MHz 68010, provides 16 megabytes of virtual address space and 2 megabytes of physical 150-ns RAM. It runs Berkeley's 4.2 Unix networking software, written by Bill Joy, who is now Sun's software director. The system interfaces with a 10-Mb/s Ethernet.

Floating point. The Sun 2 keeps these features but adds another 2 megabytes of RAM and an intelligent peripheral interface and upgrades the display. It also offers a buffered Ethernet interface, a floating-point processor based on very large-scale integrated circuits, and a color-display controller in charge of a 640-by-480-by-8-bit display memory.

The color-display controller, floating-point processor, and interfaces to Ethernet and various mass storage options plug into the system's Multibus. But the unit's virtual memory manager communicates with another bus as well, a private fast memory bus for the 4 megabytes (maximum) of high-speed RAM. The controller for the high-resolution monochrome display also connects to this bus.

Besides the newly released Berkeley 4.2 version of Unix, the software includes a Core-based graphics package and a versatile display manager that entertains users with overlapped windows, pop-up menus, and icons. The display control is supported by a VLSI "raster op" processor that lets a single instruction operate on a whole block of pixels.

Open interfaces like Ethernet, Multibus, and Unix provide flexibility for original-equipment manufacturers, large end-users, and scientific researchers—Sun's main customers. The system also implements the Arpanet TCP/IP and file-transfer protocols. Sun systems are often used in sophisticated program development; others adapt Sun's software to such applications as computer-aided de-



sign and manufacturing, text processing and makeup, and bioengineering.

Reflecting a recent influx of executives from Digital Equipment Corp., Sun has upgraded the Ethernet interface to DEC's Revision 2, which provides system diagnostics and enhances reliability. The controller incorporates 256-K bytes of buffer memory, so stations can accept back-to-back data packets. The interface maintains its own memory map and can thus start a data transfer to the exit buffer while it builds the Ethernet header—an 80% saving on packet-building time, the firm claims.

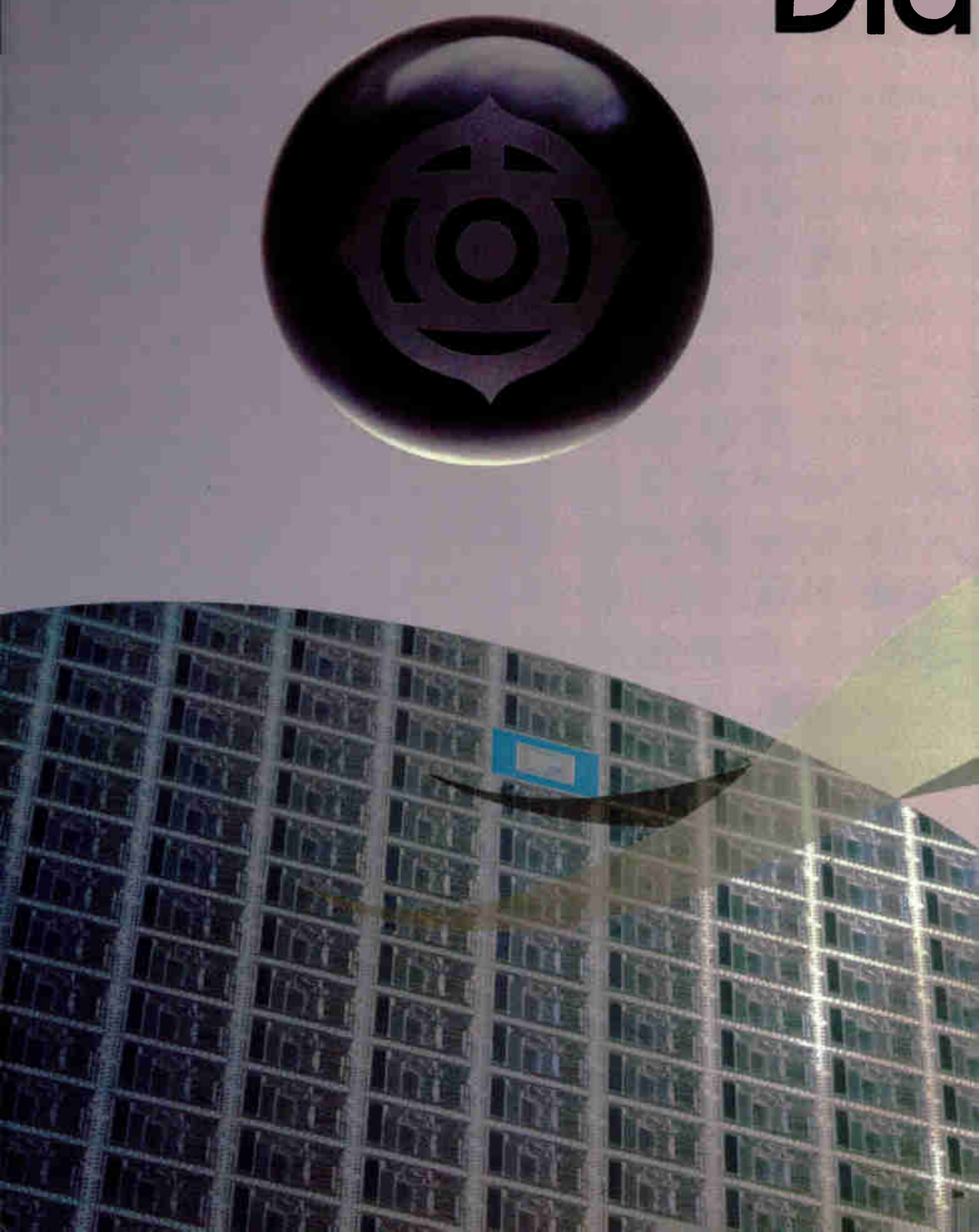
Storage options. Sun has included the Small Computer System Interface, which permits a variety of add-ons. With SCSI come the 42-megabyte (formatted) Maxtor Winchester disk and ¼-in.–tape back-up unit. Any Sun in a network can act as file server for the others, though the 2/170 is specifically designed to do so, taking the place of a minicomputer or a mainframe as the workhorse for a large network and accommodating a 474-megabyte Fujitsu disk.

Sun has emphasized high performance throughout. Main memory is accessible without wait states over its own high-speed bus. The fast hardware and the windowing software have been the big attractions for Sun at demonstration sessions. Sun now provides window "panes," small subwindows within a process. The display operates at a video rate of 100 MHz, repainting the screen in 55 ms.

Both versions of the Sun architecture will operate together on a network. Users who have upgraded their Sun 1 systems will receive the latest software enhancements without extra charge. The Sun 2 will be delivered 90 to 120 days after receipt of order at a unit price of $16,900 for the 2/120 with 1 megabyte of memory or $20,900 for a rack-mounted 2/170 with 2 megabytes of RAM. Both prices include the Ethernet controller; without it, they are $2,500 less. Extra memory costs $3,300 per megabyte. OEM discounts are also available.

Sun Microsystems Inc., 2550 Garcia Ave., Mountain View, Calif. 94043. Phone (415) 960-1300 [Circle reader service number 338]

Did



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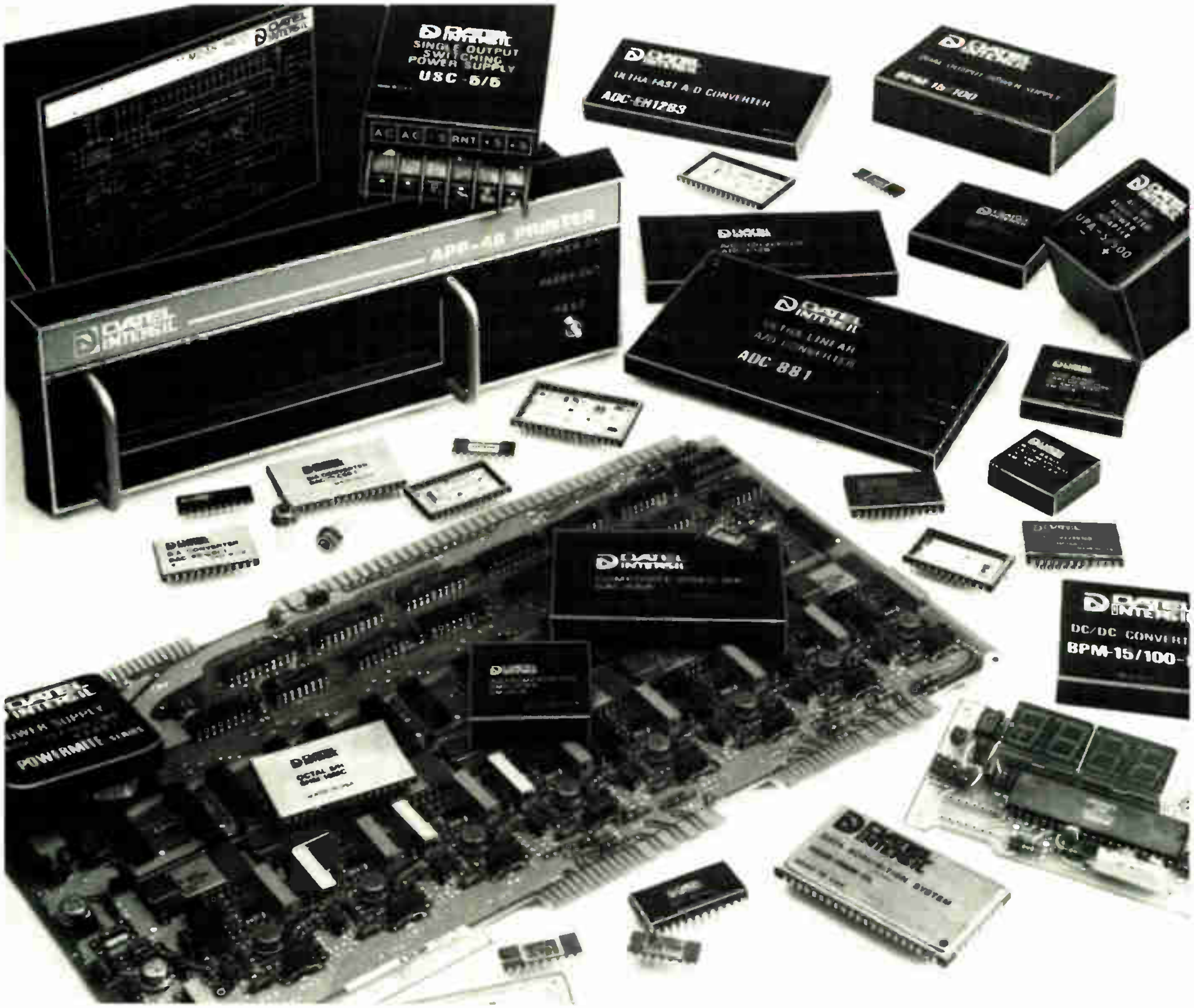

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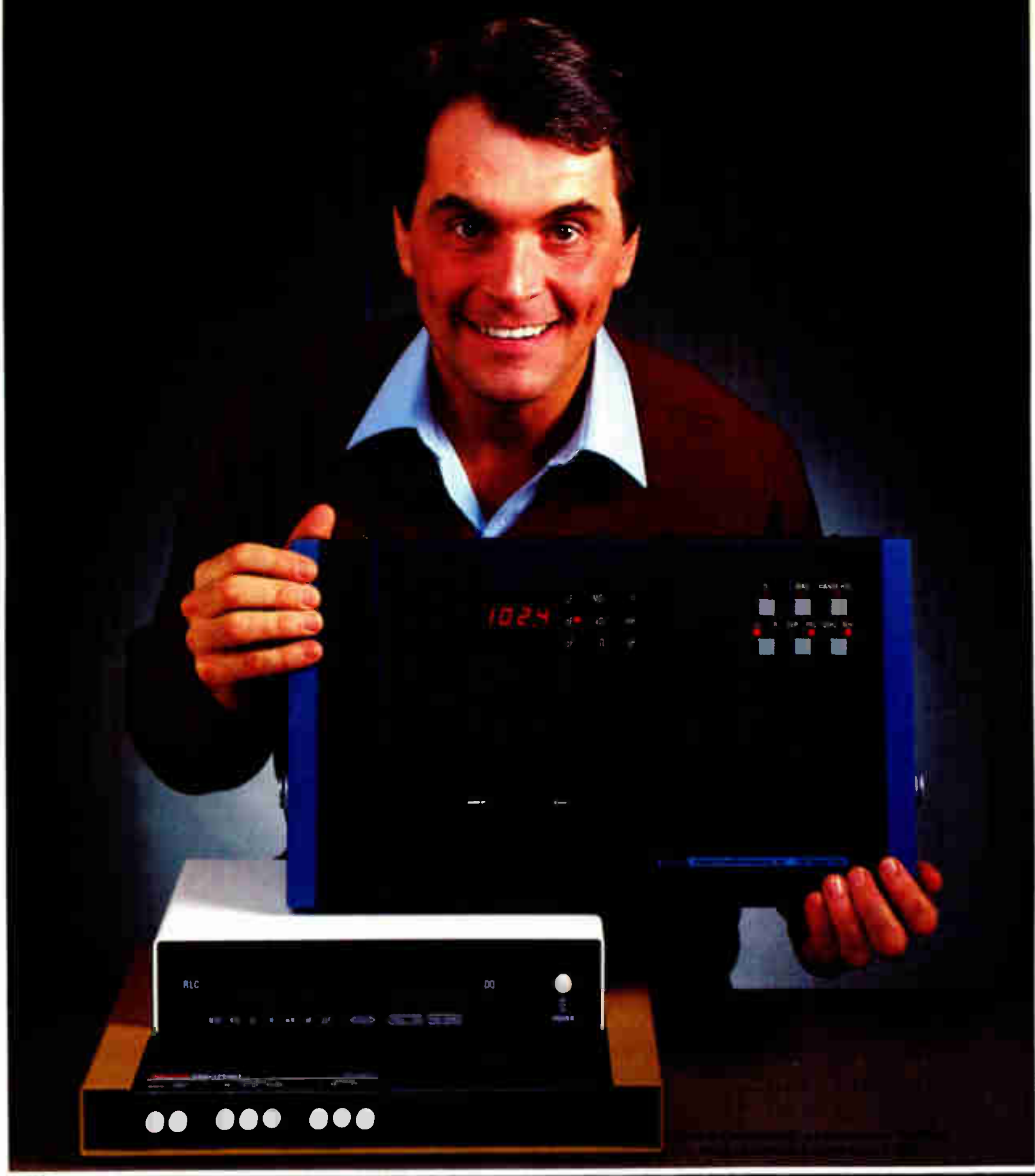

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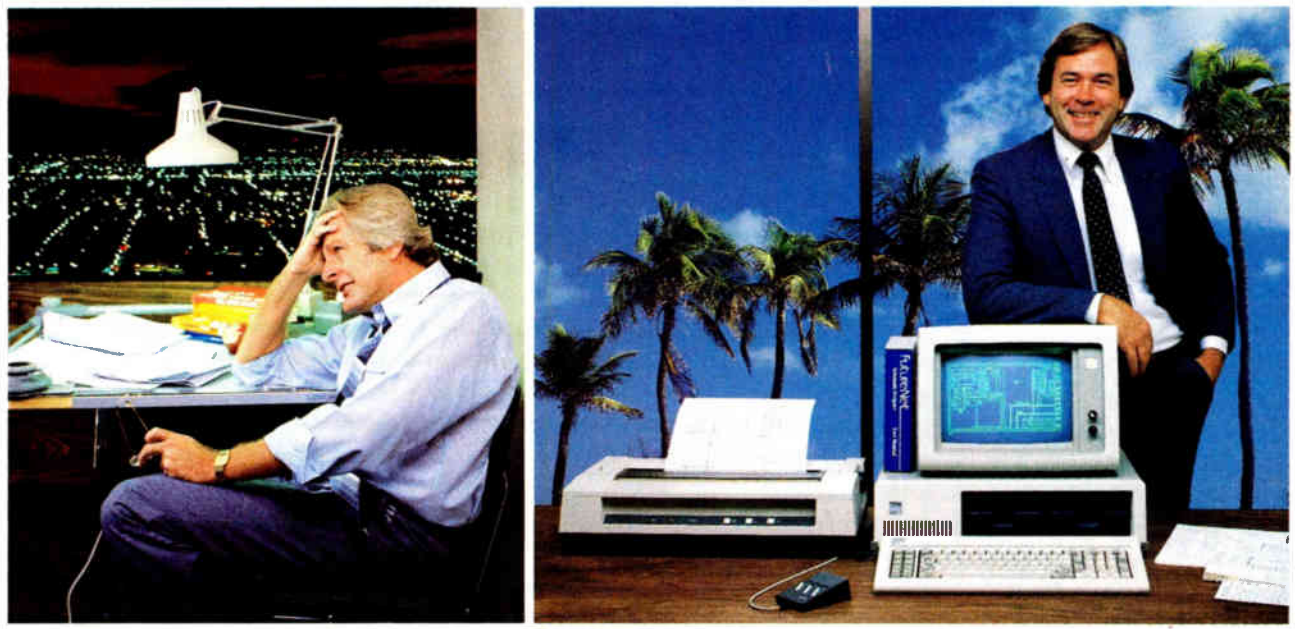

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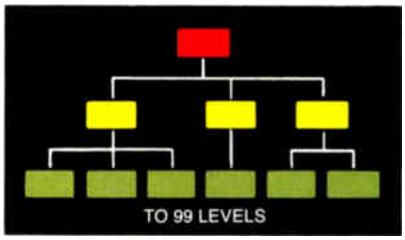

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Computers & peripherals

8-in. drive has low head wear

166-megabyte drive catapults heads onto spinning disks, accesses in 22 ms average

A dynamic head-loading technique inside a fixed 8-in. hard-disk drive subjects heads and media to less wear and tear than do conventional Winchester units that start and stop with heads resting directly on disk surfaces. In fact, tests of Amcodyne's Comanche 8160 turned up no measurable wear to heads or media in 70,000 start-stop cycles.

The drive's patented ramp-loading technique, which catapults the Whitney head and suspension systems over the rotating disk, cuts the time needed to stabilize the heads over the media. In most Winchester drives, heads rest on the disk and are launched as the disk turns. As the medium accelerates to 200 rpm, the heads tend to bounce and drag along the surface for about 3 seconds, says R. David Cordano, Amcodyne's executive vice president.

With dynamic loading, the Whitney suspension is not launched over the medium until the disk is spinning at full speed, a technique that cuts to 3 ms the time needed to stabilize the heads. The Comanche has the same Whitney suspension design, miniature composite-ferrite head technology, and dynamic-loading method used in Amcodyne's first product, the Arapahoe 7110, a 50-megabyte half-removable hard disk drive [*Electronics,* Sept. 22, 1982, p. 183]. In fact, the two products have about 70% of their parts in common, and both are controlled by the same 6803 microprocessor.

Six platters. One difference between the two is the Comanche's 165.9 megabytes of storage from six fixed disks. Ten surfaces are used to store data and one for servo data. The top disk surface is blank and

acts as a cover. The Arapahoe drive uses an embedded-servo technique.

The 4.63-by-8.55-by-14-in. Comanche, housed in the envelope size of a standard 8-in. floppy-disk drive, weighs 19 lb. It has a Storage Module Drive interface. Its average access time is 22 ms, its maximum access time 46 ms, and its data-transfer rate 1.229 Mb/s. Track-to-track seeks take 6 ms.

The Comanche's radial density is 9,600 tracks/in. and its linear recording density, 9,750 b/in., for a density of 9.4 Mb/in.^{2}. The drive also features a 2 of 7 run-length–limited code. Like codes developed for mainframe storage, this one allows 50% more bits per inch than there are flux changes per inch.

The drive operates from a dc power supply of ±24 and ±5 V. Power dissipation in read and write cycles is 90 W; during seeks it consumes 110 W.

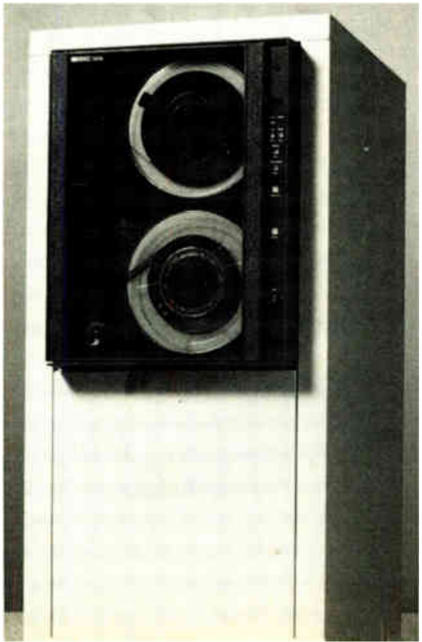
Amcodyne plans to make evaluation units available in the first quarter, with volume shipments beginning in the second. The Comanche's single-unit price is $3,800.

Amcodyne Inc., 1301 South Sunset St., Longmont, Colo. 80501. Phone (303) 772-2601 [Circle reader service number 361]

Start-stop drive streams as well

½-in. tape drive switches from streaming to start-stop mode automatically, optimizing speed

A 68000 microprocessor in Hewlett-Packard Co.'s latest ½-in. magnetic tape drive executes an algorithm that



calculates optimum recording speeds for data-block transfers from a host computer. The subsystem can buffer data from the host in 32-K bytes of high-speed random-access memory.

The 7974A dual-density drive, intended for backup storage for a range of HP computers, automatically sets itself in either a start-stop recording mode or a faster streaming mode, depending upon the lengths of the eight previously recorded blocks of data. In the start-stop mode, the tape runs at 50 in./s; the streaming speed is 100 in./s.

While operating in the faster streaming mode, the drive must back up and reposition itself before recording the next data block, which takes 363 ms. If data blocks are short, the drive runs more efficiently in the stop-start mode, using tension arms to buffer the tape and eliminate the need for repositioning, says James Jones, product manager at the Greeley division.

At power-up, the unit sets itself in the streaming mode. After it receives the first eight transfers, the drive will then average the data block lengths and determine the best speed setting. As the drive operates, it will continue to average the last eight transfers.

To keep the tape drive in the optimum tape speed, HP has included firmwire that will, when enabled, buffer data transfers from the host in the 32-K bytes of RAM. The drive will signal the host that it has received the data as soon as it is placed in RAM, freeing the computer to quickly proceed to the next task. Meanwhile, the drive subsystem performs error detection and correction in the buffer and then writes to the tape. The 32-K bytes can buffer up to 20 commands and blocks.

To take advantage of these features, HP has changed the low-level driver in the operating system for its 3000 series 39, 40/42, 44/48, and 64/68 computers. Next spring, it will be supported on HP's 1000 A and L series and 9000 computers.

Drives formatted with 1,600 characters/in.—phase-encoded format—are priced at $12,500 each. An optional 800-c/in. inverted nonreturn-to-zero format may be added for dual-density needs, adding $2,500 to the price. Deliveries are now under-way. The cabinet, measuring 63 by 23.6 by 30.5 in., can house two tape drives. A 2-m cable, which attaches to the HP interface bus, is included. Drives without the cabinet are priced at $12,000 each.

Missing track found. The nine-track drive can store about 40 megabytes of data on a 2,400-ft reel of tape in the 1,600-c/in. PE format and about 20 megabytes in the 800-c/in. NRZI format. Rewind speed is 200 in./s. In burst transfer (at 1,600 c/in.), the drive can store 160-K bytes/s in the streaming mode and 80-K bytes/s in start-stop. The subsystem's error-correction facility can reconstruct data with an entire track missing in the PE format.

The drive operates with a line frequency of 48 to 66 Hz and uses a standard 120-V power supply. An optional 220-to-240-V supply is available. The operating temperature range is 15° to 32°C, and maximum power consumption is 520 W.

Hewlett-Packard Co., Greeley Division, 700 71st Ave., Greeley, Colo. 80634. Phone (303) 356-9103 or (408) 973-7646 [Circle 362]

Dot printer has high resolution

Matrix impact printer puts out 250 characters/s or slows down for letter-quality 45-c/s work

A multiple-color dot-matrix impact printer, the Office Printer, offers what its manufacturer calls "true" letter-quality printing at 45 c/s. For data processing, it will operate at 250 c/s, and it can also create dot-addressable graphics with a resolution of 240 vertical by 720 horizontal dots/in., so it can perform all the printing tasks of an automated office.

The unit replaces "daisy-wheel printers for quality printing and either dot-matrix or expensive line printers for for general data and accounting work," says Bryan Doherty, marketing vice president of Advanced Matrix Technology Inc., a start-up company founded by industry veterans.

The key to the letter-quality feature is a proprietary device, which the firm calls a microshift mechanism, for the 18-wire ballistic printhead, whose 0.012-in.-diameter wires are arranged in two staggered columns of nine each. In the two-pass design, the print head makes its second pass in the same direction as the first, and the mechanism on the printhead platform shifts the printhead for a ¼-dot offset in the vertical axis. This produces a vertical

density of 240 dots/in., with drive electronics and firmware providing 1/720-in. position accuracy in the horizontal dimension.

A plug-in logic board carries a Zilog Z80B microprocessor, which runs the driver program, monitors sensors, controls the print head, times all operations, allocates memory, and interfaces with the host computer and control panel. An analog driver board, a front-panel board, the power supply, the motor, and sensors are also included.

Three fonts. The Office Printer accepts a wide selection of individual-sheet and continuous types of paper, including forms, with the standard friction mechanism complemented by optional bidirectional tractors and a dual-bin sheet feeder. Each printer comes with three fonts, which can be changed from the front panel or through software.

Firmware is compatible with Qume, Diablo, and NEC printers. Evaluation units are available now for $3,000, and production quantities are scheduled for delivery early in 1984 at less then $2,000.

Advanced Matrix Technology Inc., 1157 Tourmaline Dr., Newbury Park, Calif. 91320. Phone (805) 499-8741 [Circle 479]

32-bit multiprocessor system targets interactive tasks

Using a multiprocessing architecture, the MAI 8000 series of 32-bit computers are designed for interactive multitasking. The series has three models—the 8030 with three central-processing units, the 8020 with two, and the 8010 with one. Users can expand their systems without having to change hardware or software.

The top-of-the-line 8030 comes with 1.5 megabytes of main memory, expandable to 8 megabytes. It supports up to 96 terminals and printers, which are directly attached; some terminals support up to 68 slave printers.

The 8010, which supports up to 16 terminals or printers and an extra 16 slave printers, comes with 512-K bytes of memory, expandable to 2

megabytes. The 8020 has 1 to 4 megabytes of memory and supports 48 terminals or printers and another 48 slave printers.

Up to four parallel printers plus eight disk drives can attach directly on all the systems, which use a 32-bit data bus. Each system has a 160-ns access time and automatic error-detection and -correction circuitry. Each CPU works independently; when each finishes a task, it automatically starts the next.

The MAI 8000 series, priced from $50,000 to $500,000, operates under the BOSS/VS operating system and supports program development in Basic and the Origin data-base software. A typical 8030 system, available now, sells for $210,000.

MAI Basic Four Information Systems, 14101 Myford Rd., Tustin, Calif. 92680. Phone (714) 731-5100 [Circle 363]

16032-based Multibus CPU has on-board cache memory

The UB3050, a central processing unit built on a Multibus card and using the 16032 processor boasts full 32-bit internal arithmetic as well as a complete and symmetrical instruction set. To take full advantage of the 10-MHz processor, the board has an 8-K-byte cache memory that can be accessed in 45 ns.

The Multibus interface provides support for up to 16 megabytes of memory using 24-bit addressing. To accommodate smaller systems, it supports 16- and 20-bit addressing. Bus arbitration may be either serial or parallel and the UB3050 also supports Common Bus Request. Special logic is provided in cases where parallel-bus arbitration is not used.

Other features of the board, which sells for $3,995, include two asynchronous-synchronous serial ports with RS-232-C interfaces, battery-backed time-of-day clock, programmable real-time clock, memory-management unit, floating-point processor, and up to 32-K bytes of programmable read-only memory. Standard software will be Genix, National Semiconductor Corp.'s adaptation of Unix.

Unidot Inc., 602 Park Point Dr., Suite 231, Golden, Colo. 80401. Phone (303) 526-9263 [Circle 364]

68010-based unit can be host to CAD unit, network server

A 68010-based microcomputer system called Unistar 300 features 32-bit architecture and supports virtual memory and the Unix operating system. Targeted at original-equipment manufacturers, the Unistar 300 can be used as a single work station for computer-aided design and other computation-intensive applications or in a multiuser office-automation system. It can also function as a network server.

The Unistar 300 offers up to 2 megabytes of memory with parity checking and no wait states. Its 5¼-in. Winchester mass-storage system can accommodate from one to four drives with one or more controllers using direct memory access. Disk capacity can range from 40 to 160 megabytes, and 5¼-in. floppy-disk drives can also be used.

The 12 slots in the system's Multibus backplane allow users to incorporate such peripherals as graphics-display controllers and a floating-point processor. Input/output processors for multiprotocol-serial and Ethernet links are optional. The Unistar 300 supports Ada, Basic Plus, Cobol, Fortran, and Pascal, as well as assembler languages. Priced from $20,000, the system will be available next month.

Callan Data Systems, 2645 Townsgate Rd., Westlake Village, Calif. 91361. Phone (213) 991-9156 [Circle 365]

CAD system uses HP-9000, Tektronix color display

A computer-aided engineering work station incorporating the HP-9000 32-bit processor can be used in custom and semicustom hybrid- or integrated-circuit design and layout of printed-circuit boards. The EDS-2100 combines the firm's software for development of schematics, layout design, and complementary analysis with the HP-9000 and the Tektronix 4115B 19-in. color-display terminal, which has a resolution of 1,024 by 1,280 picture elements. The HP-9000 processor provides true 32-bit processing at a rate as high as 2¼ million instructions/s.

The EDS-2100 comes with software for project planning and mangement, documentation, logical design, simulation, fault analysis, test generation, physical design, verification, and artwork preparation. The system, which can serve as a general-purpose personal computer as well as be linked with the company's 1000-series terminals, will sell for about

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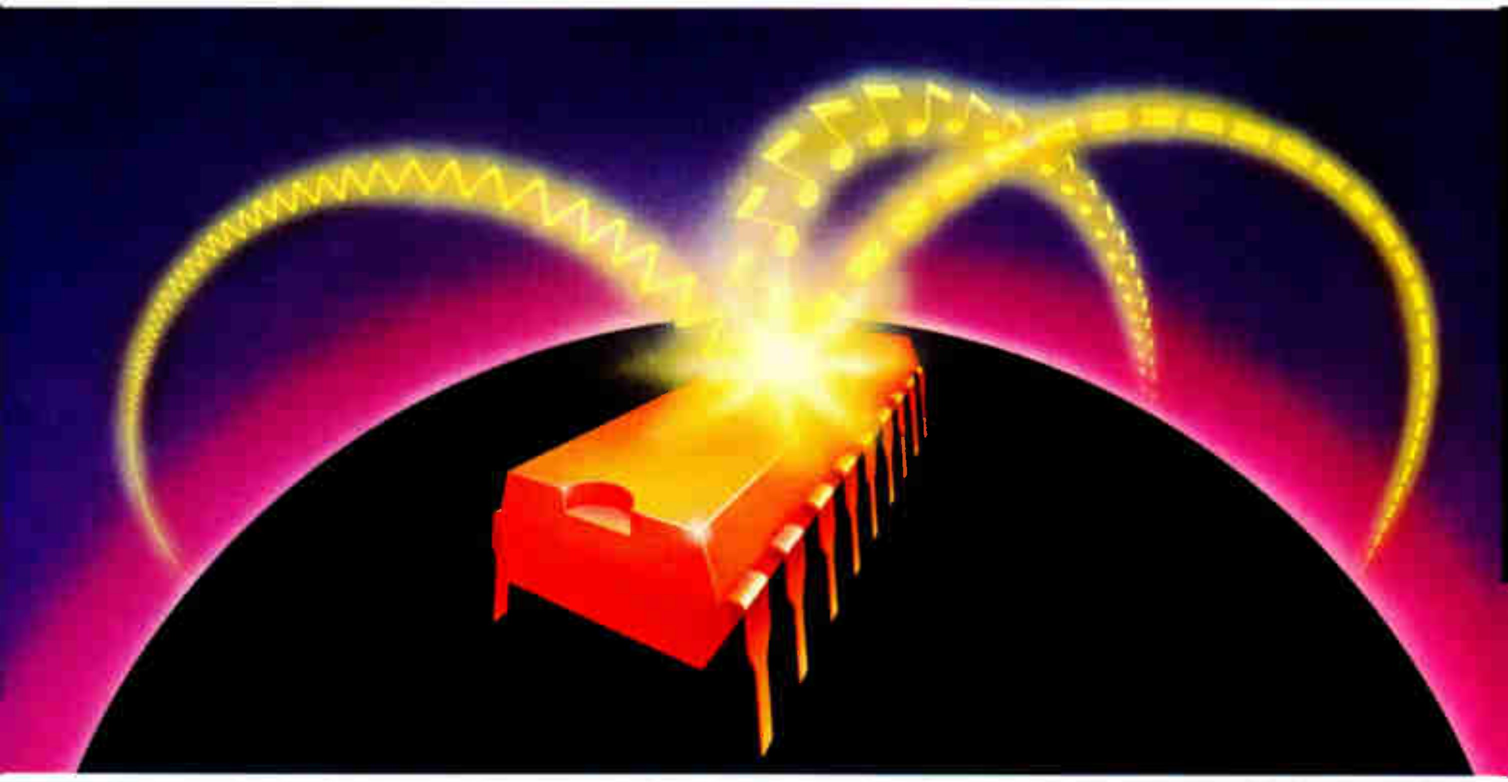

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*Touch Tone is a registered trademark of AT&T

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Circle 88 on reader service card

$100,000. First deliveries are scheduled for January 1984.

Avera Corp., 200 Technology Circle, Scotts Valley, Calif. 95066. Phone (408) 438-1401 [Circle 366]

Work station automates complete IC design process

Based on the Domain line of work stations from Apollo Computer, the SL 2300, SL 2400, and SL 2600 support all phases of semicustom–integrated-circuit design, ranging from architectural definition through cell layout. Six application-specific bundled-software packages are available.

The 32-bit microcomputer-based work stations support architectural and logic-system–level design and simulation and automatic layout for gate-array and standard-cell semicustom technology. Interfaces to other design environments, such as those for printed-circuit–board layout, are also provided.

Software packages consist of the SL 2005 for schematic capture, SL 2010 for basic logic-level design, the SL 2020 for architectural-system–level design, the SL 2030 for switch-capacitor–filter design, the recently introduced SL 2040 for standard-cell design, and the SL 2050 for gate-array design.

The work stations, which run under the Aegis operating system, include from 1.5 to 2.0 megabytes of main memory, a 34- or 158-megabyte disk, and 1.2-megabyte floppy-disk drive. The SL 2300 has a 17-in. monochrome display; the 2400 a 19-in. display; and the 2600 a 19-in. color monitor. Available now, systems range in price from $29,000 to $170,000.

Silvar-Lisco, 3172 Porter Dr., Palo Alto, Calif. 94303. Phone (415) 856-2525 [Circle 367]

Color monitor's resolution is 1,000 lines by 1,200 pixels

The model 7300 color monitor, displaying over 1,000 lines vertically and over 1,200 picture elements horizontally, uses a noninterlaced line-scanning technique. It produces stable images, without line-to-line flicker, by combining a 65-kHz horizontal-scanning frequency and a vertical-refresh rate of 60 Hz. The monitor is targeted at the very high-performance graphics systems with large bit-map memories and fast operating speeds.

The monitor uses a 19-in. fine-pitch (0.31 mm) precision in-line cathode-ray tube with maximum convergence error of 0.4 mm in the screen's main area and 0.6 mm at its edges. Direct etching or by externally mounted filters provide optional antiglare treatment for the CRT.

Other options include digital brightness, degaussing, and on-off control, hard-copy output, and controls located remotely from the monitor chassis. In single units, the 7300 sells for $4,495, with discounts on large orders. It is available now.

Conrac Corp., 600 North Rimsdale Ave., Covina, Calif. 91722. Phone (213) 966-3511 [Circle 369]

5-lb personal computer uses cartridges for data storage

With solid-state cartridges instead of disk drives and a liquid-crystal display instead of a cathode-ray tube, the MicroOffice 100 personal computer weighs just 5 lb and measures 7¾ by 11½ by 3 in. The self-powered unit, which fits easily in a

briefcase, can work as a stand-alone portable computer, a remote workstation terminal, and a communications link.

The MicroOffice 100 has an 8-line-by-80-character LCD screen built into the inside of its cover. Its full-size 73-key keyboard includes 18 function keys, 8 of which allow one-button selection of such resident software as editing, scheduling, phone directory, and terminal emulation. The operating system is compatible with CP/M.

The computer holds up to four 2-by-2-in. removable memory cartridges at a time, each providing up to 32-K bytes of storage. In addition, the MicroOffice 100 holds an 8-K-byte cartridge for data storage and a 16-K-byte one for program storage. The unit also has a parallel interface for an external disk drive or printer and an RS-232-C interface. A 300-baud auto-dial–auto-answer modem is built in. The nickel-cadmium battery pack is said to last eight hours before recharging. The MicroOffice 100, including 64-K bytes of read-only and random-access memory, is priced at under $1,500 in lots of 1,000. Samples are available now.

MicroOffice Systems Technology Inc., 35 Kings Highway East, Fairfield, Conn. 06430. Phone (203) 367-2525 [Circle 368]

Facsimile machine integrates into office-automation nets

A desktop facsimile terminal integrates into office-automation networks to receive computer information for printing or for redistribution to other facsimile units located anywhere. The Telecopier 295 is designed for businesses that transact many local and long-distance messages a month. Each transaction can contain several pages; the 295's log stores up to 25 messages. A page can go from one unit to another in less than 30 s.

The facsimile machine adjusts automatically to the speed of the sending or receiving unit and provides the recipient with a printed message heading showing the time, date, and terminal identification number. For sending multiple pages, the 295 has a 30-page document feeder; messages are received on roll-fed paper and cut automatically.

The Telecopier is compatible with those Group 3 facsimile devices that conform to the recommendations of the International Consultative Committee for Telegraphy and Telephony. One option permits the machine to be compatible with CCITT Group 1 and 2 devices, and another adds an RS-232-C port to link the 295 to computer networks.

The base price of the Telecopier 295 is $4,600; the Group 1 and 2 option goes for $600, and the RS-232-C port adds $700. Deliveries are scheduled to begin in January 1984.

Xerox Corp., Office Products Division, 1341 West Mockingbird Lane, Dallas, Texas 75247 [Circle 474]

Half-height 5¼-in. Winchester stores 40 megabytes

One-, two-, and three-platter 5¼-in. half-height Winchester-disk drives offer unformatted capacities of 13.34, 26.7, and 40 megabytes, respectively. Formatted capacities are 10.48 megabytes for the TL213, 21 megabytes for the two-platter TL226, and 31.46 megabytes for the three-platter TL240. Access times, including settling, are 95 ms average, 20 ms track to track, and 230 ms maximum.

Three platters can be used because the spindle motor is designed inside the platters' hub. The read-write head preamplifier is inside the head assembly for better signal-to-noise ratio and better protection from radio-frequency interference. Improvements in arm-offset and overhang geometery minimize head azimuth and produce a more consistent flying height.

All drives use the ST506/412 interface, but the company can provide higher data rates. Pricing in lots of 500 range from $650 to $1,055. Samples are available now, with production quantities scheduled for delivery starting in January 1984.

Tulin Corp., 2393 Qume Dr., San Jose, Calif. 95131. Phone (408) 942-9025 [Circle 472]

The Total MOS/VLSI Company:
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Selecting a custom or semi-custom circuit supplier isn't easy. Consider the trade-offs. If you choose a large producer of commodity circuits, you may not get the service and attention you need. Go with a smaller IC house and you won't get total capability. You also run an additional risk. As your volume requirements grow, a small producer may not be able to deliver—especially if it's dependent on others for fabrication.

AMI, on the other hand, gives you the best of both alternatives. We are the *only* fully-integrated custom circuit producer. We have complete in-house capability: design, layout, tooling, wafer fabrication, assembly, packaging, testing and quality assurance.

We give you choices. We can handle everything from design to delivery—or provide any service "a la carte." With separate business units in place to handle each circuit design approach, plus over 17 years custom circuit production experience, you can always expect fast, reliable service.

Respond to future challenges, quickly and easily.
At AMI, adapting to changing market conditions is second nature. We maintain a common data base for all design approaches, making it easy to go from gate arrays to standard cells to full-custom circuits. Full pin-for-pin replacements. Another way that AMI always gives you the most cost-effective answer.

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We can offer you a complete selection: from 300 to 5000 gate designs in 5-micron single metal or 3-micron single and double metal CMOS technologies. Currently in development: our new 2-micron CMOS arrays.

A custom solution in less than custom time: standard cells.
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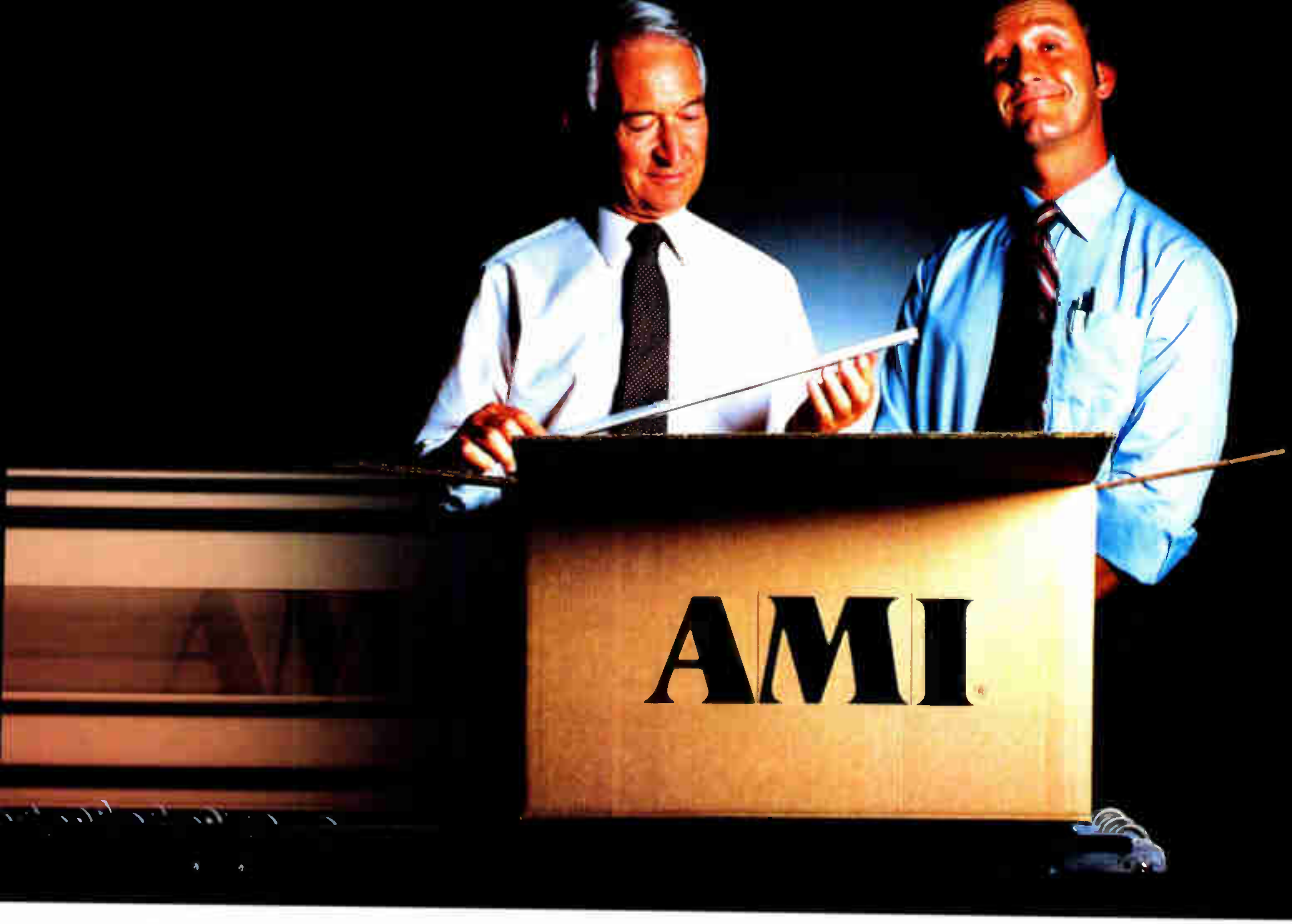

and CMOS cells. Any of these cells can be customized to your needs by adding special features such as input/output structures or by fine tuning them to your speed, power and density requirements. That's another AMI advantage: freedom of choice.

For both gate arrays and standard cells, we can provide low-cost logic entry and verification software on a Prime or DEC VAX™ computer, or on industry standard work stations. After prototype approval, we can begin delivery in as little as 4 to 5 weeks.

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If you already have a design ready for manufacture, call AMI. Our expertise in design rule verification, process engineering and test engineering assures that you always get exactly the circuits you need. With over 27 variations of our CMOS, NMOS and PMOS processes available, we have the technology to match your designs with our processes.

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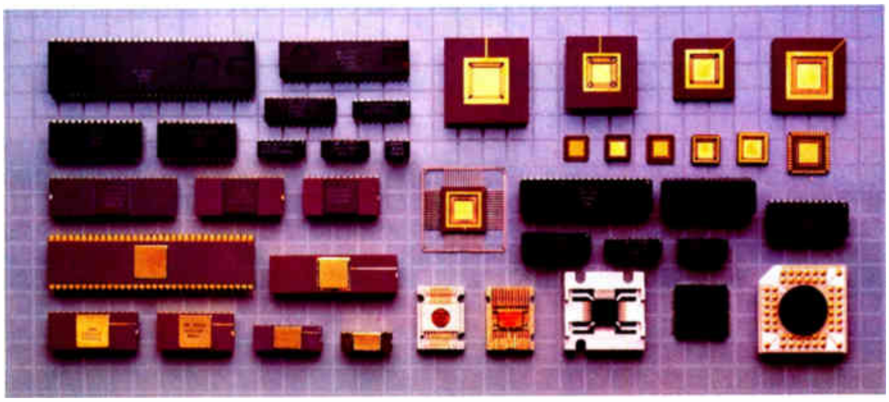
Should you want to develop your own in-house design capability, we're also the people to call on. Establish a Joint Development Venture with AMI, and we'll teach your people how to design the MOS/VLSI circuits you need at either your facility or our training center. When your designs are complete, we'll provide the manufacturing, packaging and testing.



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If you've been watching the trade press, you know that demand for circuits is increasing. Some predict future shortages.

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With AMI, you have your choice of all the latest multi-pin packages. That includes mini-flat packs, chip carriers, and pin grid arrays, with up to 144 leads. Giving you the maximum number of options is our standard way of doing business.

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The bottom line: we work the way you work.
By offering a continuum of capabilities, AMI gives you unlimited flexibility and total freedom of choice. If you want us to handle the entire process, we'll do it. If you only need manufacturing, we'll provide it.

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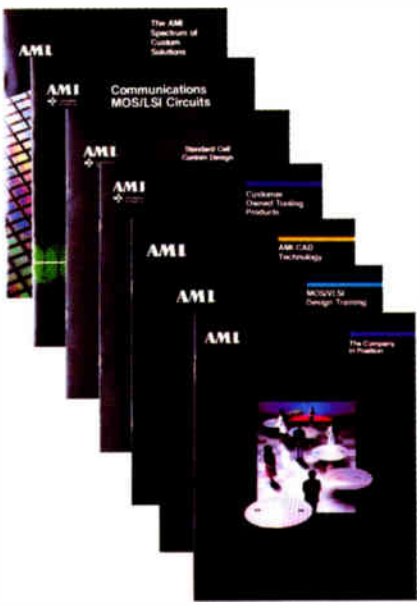

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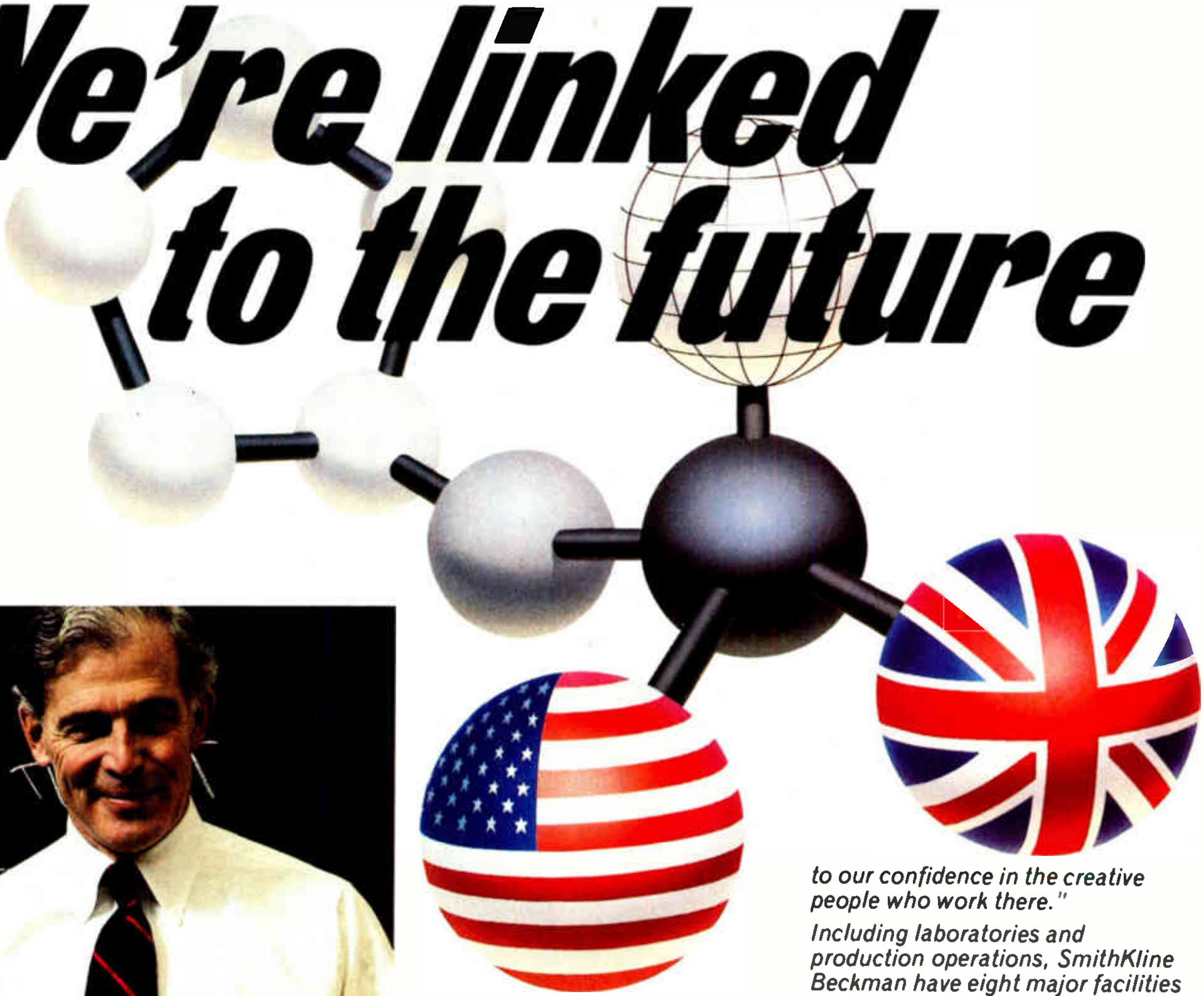

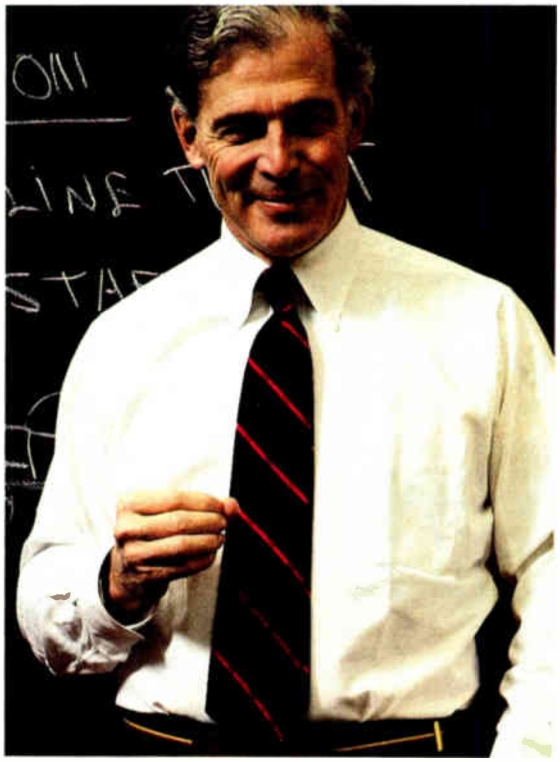

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← Circle 229 on reader service card

Value

It's the one excess we add to our in-circuit test systems.

Value in ATE systems is many things. It's a wide choice of compatible systems. It's innovative engineering enhanced by more years of building ICT systems than any other manufacturer – 16 to be precise. It's Marconi's exclusive ability to provide both local and global area networking. It's CAR,* Marconi's unique computer aided repair system. It's system reliability gained by making ATE systems for installations in every imaginable climate and working environment worldwide...backed by the longest warranty offered in the board test business.

Value. It's the basis of our growth. Last year alone, our world-wide in-circuit test system sales grew by 70 percent, much greater than our nearest competitors.

Four Basic Board Test Systems.

System 80X as shown in the background offers over 2,000 hybrid test points and dual-fixture flexibility. System 80S, shown on the right, and a dual fixture System 80D (not shown) offer up to 640 in-circuit hybrid test points. System 80R (not shown) was specifically designed for automatic board handlers in fully automated factory-of-the-future environments.

Independent dual fixtures increase throughput up to 70 percent. Powerful software retains user friendliness. For high speed digital testing, we provide up to a 16 MHz data rate for VLSI requirements.

Local and Global Area Networking. Marconi Really Has It.

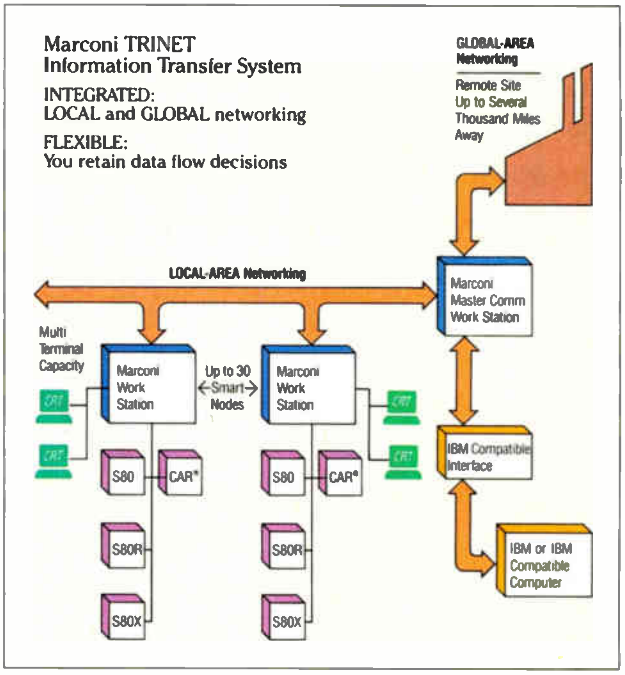
Now you can branch out with Marconi TRINET,™ the integrated and flexible information networking system. It's integrated to give you both local and global networking with IBM compatible mainframe interfacing. It's flexible. You retain data flow decisions.

Within the plant, Marconi work stations can be located as far as 19,500 ft. apart (6,000 meters). Correlate and manage information on a dynamic and continuous basis.

Even over a distance of several thousand miles, Marconi's TRINET gives you the power to exchange information via the international standard X.25 Protocol (packet switching). Information can be gathered on either a real time or batch basis. The accompanying chart shows you how it all goes together.

The CAR* Paperless Option. It Multiplies Productivity.

Before Marconi put automation into board rework with CAR,* (shown on left), the full value of test and repair network economics were out of reach. Now one repair and rework operator can process many more boards with a lower error rate. CAR* instantly identifies trace shorts and component faults in color and physically locates them. Because CAR* is data linked to the test system, information on faulty boards is forwarded to CAR's computer automatically which eliminates manual fault-ticketing.



Value. It's More Productivity For the Money.

The innovative technology of our test systems together with CAR,* our friendly software and networking capability give you the highest productivity for the money.

You shouldn't be surprised that Marconi was first to bring you the advantages of both computer aided repair and networking. We pioneered in-circuit testing in 1967. Now with more than sixteen years experience, hundreds of installations throughout the world and approaching the end of our first century in the electronics industry with over eight billion dollars annual sales, we've added more proof of value.

For more information, address Marconi Instruments, A.T.E. Division, 292 Gibraltar Drive, Sunnyvale, CA 94089. Phone (408) 745-7561.

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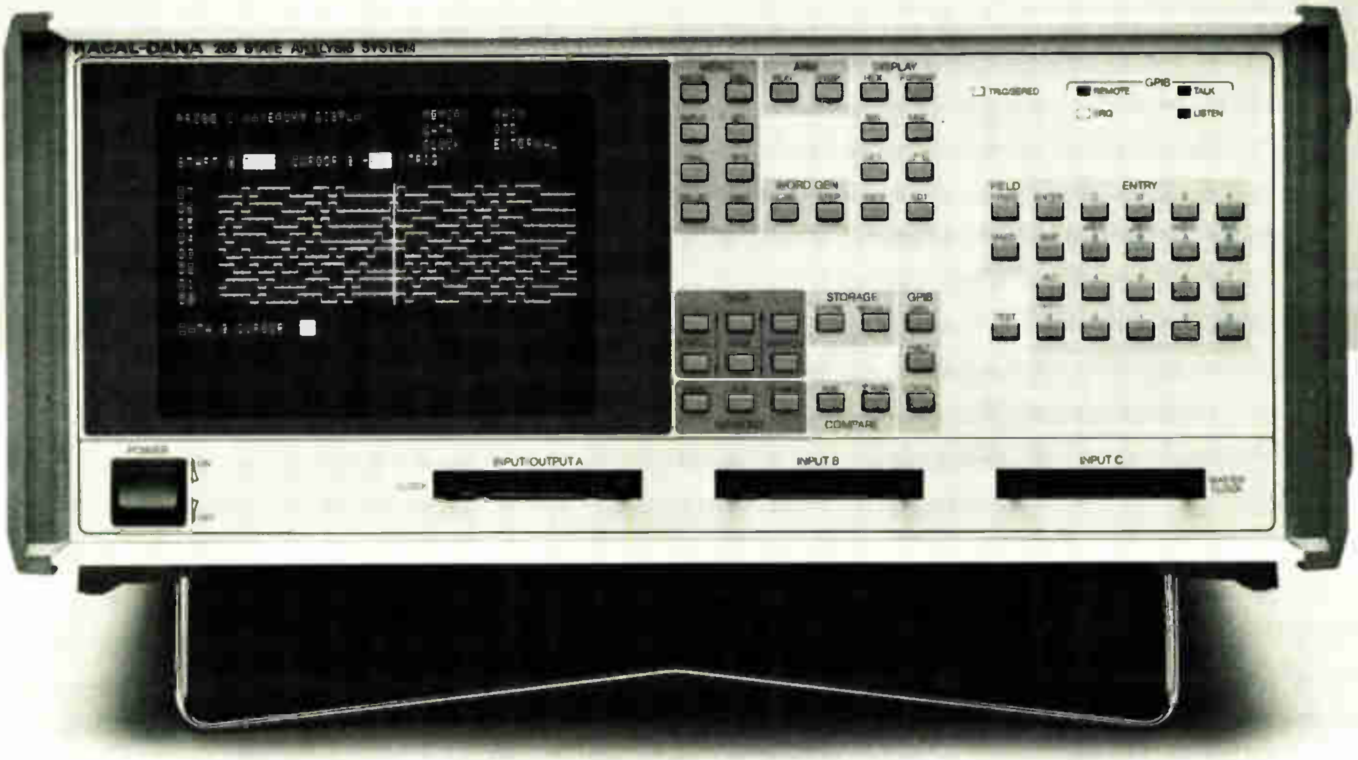
Circle 231 on reader service card

RACAL-DANA SERIES 200 μP ANALYZERS



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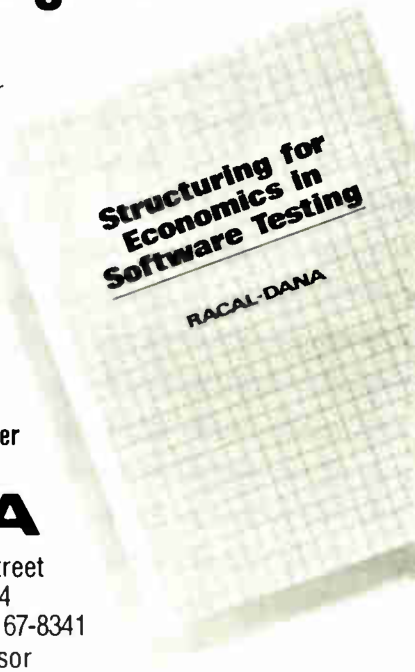

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System integration

Sync equipment gets X.25 link

Packet assembler-disassembler connects synchronous computers to packet-switching network

Computer system integrators who want to connect asynchronous computers and peripheral equipment to X.25-protocol packet-switching networks have no problem in obtaining packet assembler-disassembler (PAD) hardware to do the job. These devices receive messages in the format of the host computer and, in accordance with the recommendations of a 1980 document from the International Consultative Committee for Telegraphy and Telephony (CCITT), send the data in packets through a network, making sure transmission is error-free. They also convert incoming packets back into the computer-native protocol.

PAD users who need to accommodate synchronous protocols have not been able to do so with off-the-shelf equipment and have had to resort to custom software and hardware to perform the PAD functions—until now. Protocom Devices has come up with the P2500 PAD product line, members of which support different synchronous computer protocols.

According to Protocom Devices president Raphael Collado, the P2500 series can accommodate seven common synchronous protocols: the Uniscope (Sperry Univac), BSC (IBM 3270), Honeywell VIP7700, Hewlett-Packard BSC, IPARS/PARS, Burroughs TD-830, and DEC's DDCMP. Thus, such substantial benefits of packet switching as cost sharing among users, payment by the packet instead of the line, and alternate routing in case of node or line failure may be enjoyed by synchronous computer users.

Protocom's P2500 design is based on the seven-layer model for computer communications developed by the International Standards Organization. The key layer in this model for PADs is layer five, which is known as the session layer. In fact, Protocom claims that its session layer is the industry's first fully featured session layer. It involves hardware and software that takes care of: two levels of network security; simultaneously switchable dual-host sessions for certain connected terminals; a data-streaming technique, known as turbo-mode, that reduces queuing delays; error handling that is even more reliable than standard X.25 approaches; and automatic connection. The battery-backed P2500 PADs also feature a menu-driven supervisory control port that provides system diagnostics, statistics, and other network-management functions.

Channels. The P2500 PADs, with 40 logical channels and four physical channels, can handle user-defined packet sizes of either 128 or 256 bytes in any combination of switched or permanent circuits. Data rates of up to 9,600 b/s can be supported with either an external or internal clock. According to Collado, the P2500 complies with CCITT X.25 1980 approved documents, levels 2 and 3, for the packet connections and with the full CCITT X.3 recommendations for the supervisory port.

The four-channel device in a stand-alone configuration measures 32.4 by 7.6 by 28.6 cm. The P2500, which is connected between a synchronous-protocol computer, printer, or terminal and an X.25-based packet-switching network, weighs 8 lb and requires 40 W of input power.

The P2500's single-unit price is $9,500. Deliveries are in 45 days for a Uniscope-protocol PAD, 60 days for others.

Protocom Devices, 207 Atlantic St., Stamford, Conn. 06901; phone (203) 327-6893
[Circle reader service number 343]

Low-cost intelligent terminal replaces IBM PCs on PCnet

Users of Santa Clara Systems Inc.'s PCnet can save money by expanding their networks with PCterminal intel-

The Alps Advantage in variable and fixed resistors:

Alps is the world's largest manufacturer of resistance devices! Just how large is that? We presently produce more than 70-million units per month. To achieve this high level of production, we have created the industry's most complete in-house facilities including our own tooling, punching, stamping and molding. We start with basic raw materials and actually blend our own carbon pastes and silver compounds, and do precision screen printing of resistance patterns. Virtually every step of fabrication and assembly is done on high speed automated machines of our own design — even the test equipment is automated!

Variable resistor controls. Rotary types from single shaft-single unit to triple shaft-8 unit; sizes from 9 mm to 40 mm; resistance from 500 ohms to 1 megohm.

Slide types with travel from 10 mm to 100 mm; single, dual or 4-ganged units; resistance from 500 ohms to 1 megohm; available with LED illuminated levers.

Stick controls, with combinations of pots and switches, including custom designed complete units; operating life up to 1-million cycles.

Trimmer potentiometers with metal glaze, carbon film or solid carbon element; sizes from 4 mm to 10 mm; top, side or bottom adjust; resistance from 100 ohms to 2.2 megohms.

Fixed resistor components. Miniature thick-film resistor networks; low-profile SIP configuration, from 4 to 17 pins; resistance values from 10 ohms to 1 megohm; choice of 9 standard circuits; also available with RC networks. Plus chip resistors in standard size 1.6x3.2 mm or new micro-size 1.25x2.0 mm.

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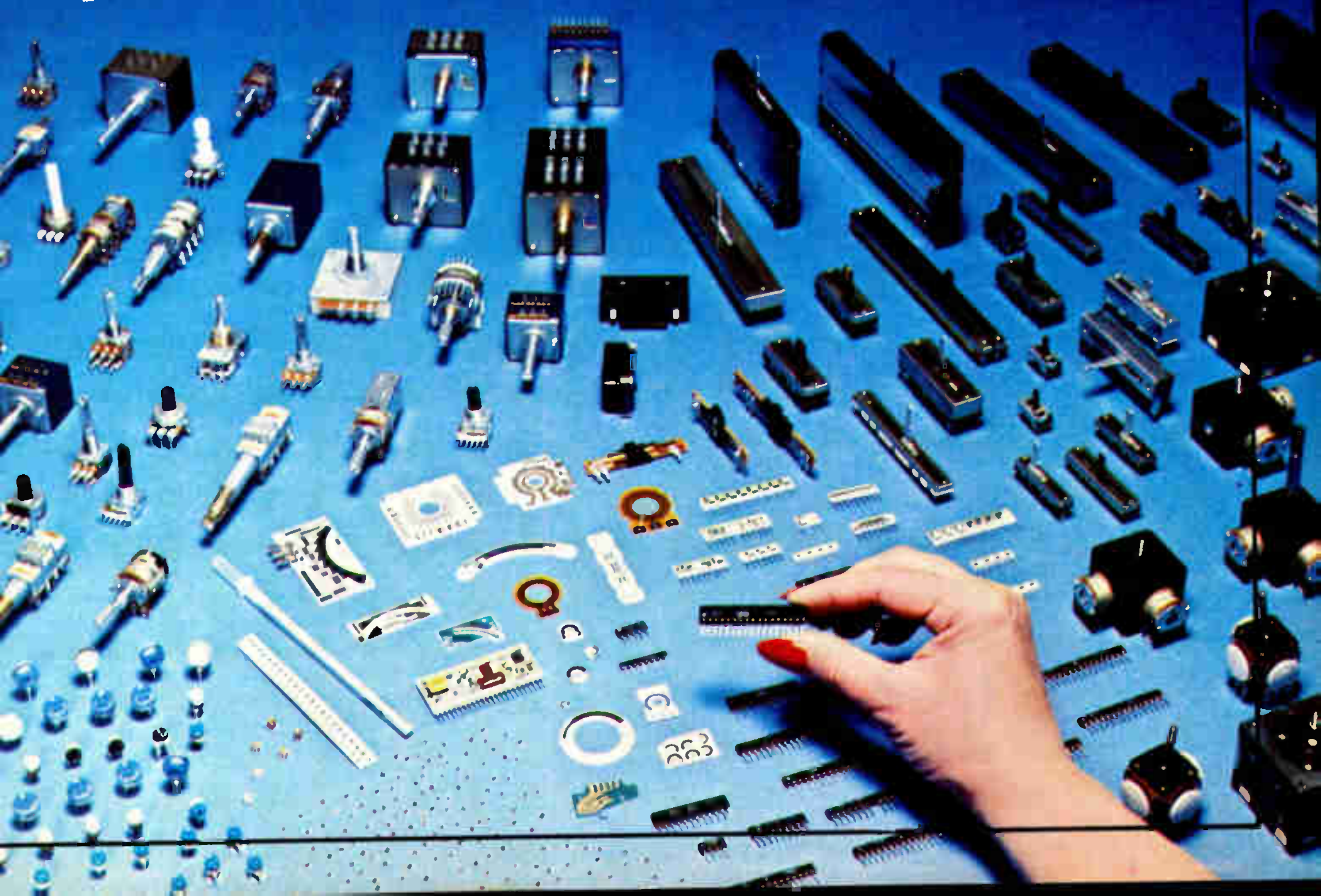


New products

ligent terminals instead of the more costly IBM Personal Computers. Priced at just $1,295, the IBM PC-compatible terminal comes with a built-in local network.

A proprietary-network protocol allows the terminal to initialize its operating system (either PC-DOS or the company's version of MS-DOS, called SCS-DOS) from a hard disk or from an IBM PC's remote floppy disk. The protocol also lets the terminal communicate in the network without its own floppy-disk drive—instead, the terminal picks one PC in the network and shares its peripherals. Up to 16 PCterminals can be connected to one PC or XT. What's more, with an optional floppy-disk drive, users can run programs locally, as well.

The PCterminal, which will be unveiled at Comdex, has a monitor, keyboard, an 8088 microprocessor, both serial and parallel interfaces, four expansion slots for peripheral cards, and 256-K bytes of random-access memory. It will be available in the second quarter of 1984.

Santa Clara Systems Inc., 1860 Hartog Dr., San Jose, Calif. 95131. Phone (408) 287-4640 [Circle 343]

Plug-in board lets LSI-11 computers run CP/M software

With the Logicraft QCP-11 plug-in interface board, DEC LSI-11 minicomputers can run CP/M programs without modification to either their hardware or software. In addition, because the board operates independently of the host system, it can run CP/M programs while other programs are running on the DEC LSI-11. The

board, which has a serial port to connect a modem, terminal, or printer, contains 64-K bytes of random-access memory, 2-K bytes of programmable read-only memory, and a Zilog Z80 microprocessor running at 6 MHz with no wait states.

The QCP-11 is compatible with the RT-11, RSX11M/M-Plus, TSX-Plus, and RSTS/E operating systems and sells for $1,495.

Logicraft Inc., 3 Graham Dr., Nashua, N. H. 03061. Phone (603) 888-4448 [Circle 344]

Controller lets single terminal gain access to two mainframes

Dual–remote-communication interfaces that operate concurrently double the range of host applications that a single-terminal operator can access. The model 311 dual-host controller lets display stations switch freely between two selected IBM or IBM-compatible mainframes through simple keyboard commands.

In addition, the 311 can be configured for application redundancy or host backup to allow uninterrupted processing should the host fail or communications be interrupted. The 311 operates in any Honeywell bisynchronous or Systems Network Architecture/Synchronous Data-Link Control combination and supports 32 display stations or printers.

The 311 can be purchased for $14,215 or leased for three years for $591 per month including maintenance. The company is developing a model 411 controller that will offer the same dual–remote-host access as the 311 but provide asynchronous support as well.

Lee Data Corp., 7075 Flying Cloud Dr., Minneapolis, Minn. 55344. Phone (612) 828-0300 [Circle 345]

VisiCalc IV, VisiWord bow for use on EtherSeries net

Networked versions of VisiCorp spreadsheet and word-processing software for the IBM Personal Computer are now available to 3Com

Corp.'s EtherSeries users. With the software, these users can gain network access to VisiCalc IV and VisiWord, each of which is delivered on a copy-protected IBM PC–compatible disk and installed in encrypted form to prevent unlicensed access and use. When invoked by a user through a network PC, the program is distributed quickly through the network, decrypted, and run.

Prices for both programs depend on the network server. For example, VisiCalc for an IBM XT server supporting five networked PCs, all with access to the application, sells for $115 per user. A single copy of the stand-alone version sells for $250.

3Com Corp., 1390 Shorebird Way, P. O. Box 7390, Mountain View, Calif. 94039. Phone (346) 961-9602 [Circle 346]

Terminal controller runs under sync and bisync protocols

Up to 32 terminals, both Telex and IBM devices that support A-type coaxial cable, can be attached to the 274C remote controller. An alternative to IBM's 3274 remote controller, the 274C features both bisynchronous and Synchronous Data-Link Control communications protocols.

Under SDLC, the 274C supports all Systems Network Architecture parameters exactly as defined for the IBM 3274 41C.

The 274C equips users with 128-K bytes of memory for controller con-

figurations and setup. An optional 128-K bytes of additional memory enables the controller to operate with extended functions like dual host communications, local print buffering, and format and storage retrieval. Available immediately, the 274C is priced at $10,000.

Telex Corp., 6422 East 41st St., Tulsa, Okla. 74135. Phone (918) 627-1111 [Circle 347]

Analyzer and simulator aids in building Ethernet systems

Called the Nutcracker, a local-network system analyzer and simulator for Ethernet tackles two common problems associated with building networks: how to debug and test very complex, high-speed, multiple-node networks, particularly the protocol software components, and how to characterize the operating limits of a given network. Use of the Nutcracker can shorten the network development cycle by as much as six months, the company claims.

To debug and test thoroughly, a designer must be able to see every packet on the network. The Nutcracker's observation circuitry, operating at 10 Mb/s (about 1,000 times faster than most communication instruments), sees every packet, even in fully saturated networks.

In defining a system's operating limits, designers must vary the load on the network in a controlled fashion while analyzing network response. The Nutcracker can indefinitely simulate a loaded network.

The Nutcracker consists of an 8086-based central processing unit along with 900-K bytes of random-access memory, a 20-megabyte Winchester disk drive, and a 600-K-byte floppy-disk drive. At the heart of the system is a high-speed state machine with powerful pattern-recognition circuitry. The system is packaged as a single work station that includes a 12-in. black and white monitor with a keyboard and a printer. The Nutcracker, priced at $49,000, is available now.

Excelan, 2180 Fortune Dr., San Jose, Calif. 95131. Phone (408) 945-9526 [Circle 348]

The only Power Supplies that carry a Passport to the World

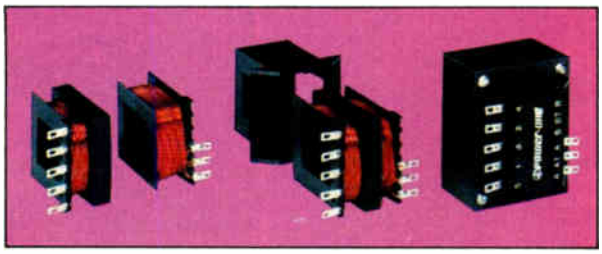
Worldwide Acceptance
POWER-ONE's new International Series is the only high-reliability D.C. power supply series to achieve true acceptance throughout the world.
Designed specifically for products sold throughout the world's major electronics markets, the International Series can be used anywhere, for almost any application...without costly modifications or crippling time delays for safety testing.

Meets International Safety Requirements
Even the most important requirements of the world's leading regulatory agencies are satisfied, including VDE, UL, CSA, BPO, IEC, CEE, and ECMA. Our new patented power transformer winding process features fully separated and enclosed primary and secondary windings. This unique construction complies with the world's toughest safety standards, including:

Leakage Current (Max.)	
Line to Ground:	5.0µa
Spacings (Min.)	
Live Parts to Dead Metal:	9.0mm
Other Than Field Terminals:	5.25mm
Dielectric Withstand Voltage (Min.)	
Input to Ground:	3750 VAC
Input to Outputs:	3750 VAC
Outputs to Ground:	500 VAC

Wide Choice of AC Input Power
More worldwide acceptance. Each unit is rated at 100, 120, 220, 230, and 240 volts, 47 to 63 Hz. This means reduced inventory and service requirements since only one standard off-the-shelf power supply is needed...regardless of your product's final destination. Another International Series exclusive feature.

New Models, More Applications
Demand has been great since the introduction of our International Series, so we have expanded our line with 32 new models..... 76 in all.



Power-One's patented International Series transformers feature separate, fully enclosed, primary and secondary coils. Meets safety requirements of VDE, UL, CSA, BPO, IEC, CEE, and ECMA.

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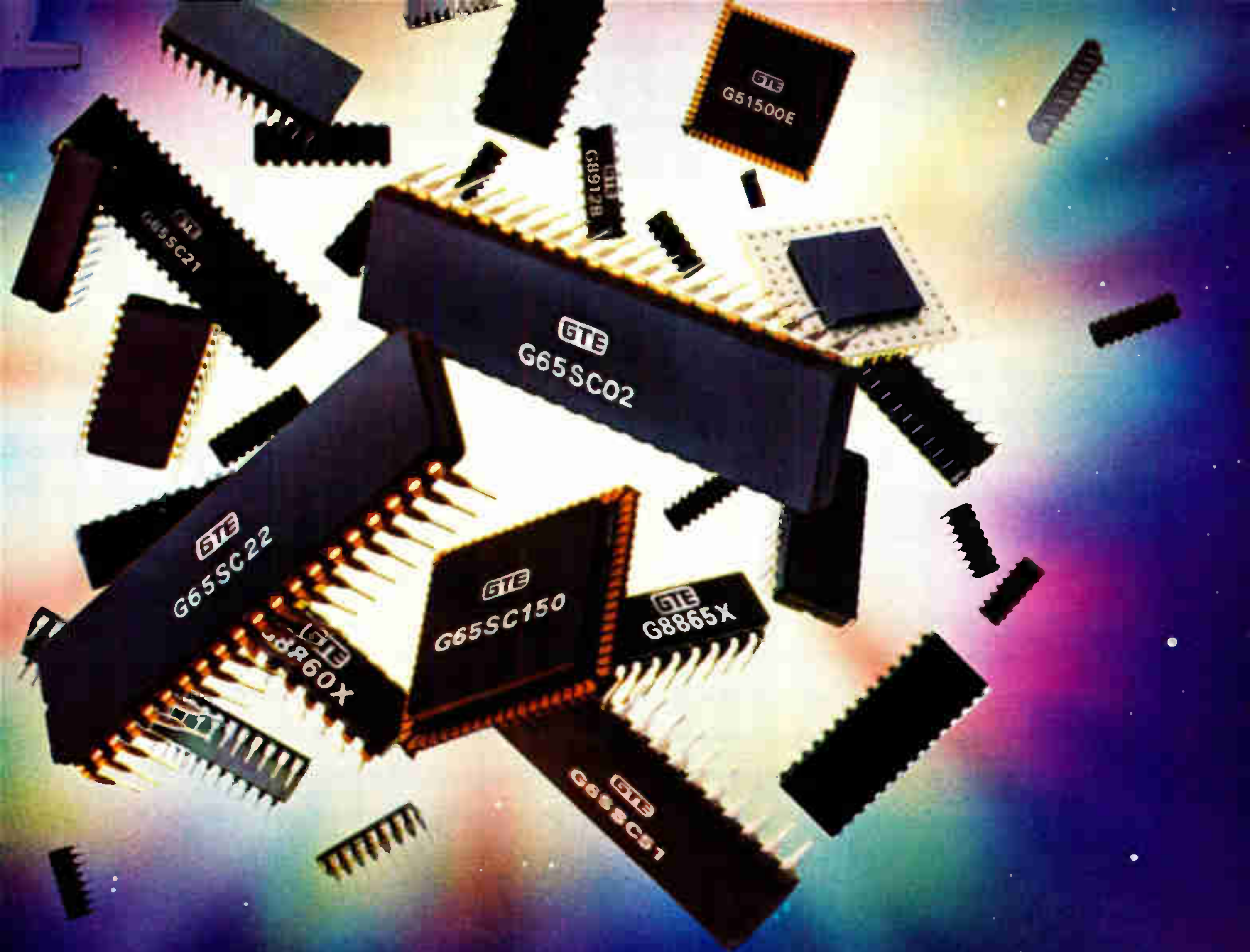

devices. Or our G65SC150 communications terminal unit: an 8-bit CPU, ROM, RAM, timer, I/O and sine wave generator…all on a single chip!

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Want to personalize your design with semi-custom? No problem. Our G50000 series gate arrays let you convert the most complex SSI/MSI logic into a single IC with up to 2,500 gate-equivalent functions. And, thanks to our state-of-the-art Automated Logic Integration System (ALIS), you'll get super fast turnaround on our semi-custom devices. They're all implemented in our leading edge silicon gate CMOS process—a process also available to you through our customer-furnished tooling program.

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GTE Microcircuits

Circle 247 on reader service card

HP's 64000

Logic Development and you won't worry

Timely
Processor Support

Ever have to settle for a second-choice microprocessor because language and emulation support wasn't available for your first choice? Put HP's 64000 Logic Development System in your lab and that frustration is gone.

That's because HP's microprocessor support strategy results in assemblers and emulators for virtually any 8- and 16-bit microprocessor...well ahead of the support available from manufacturers.

How is that possible? With the 64000 system, you can select the tools to build your own assembler and emulator. For assembler support all you need are the instruction set of your processor and HP's user definable assembler. Easy-to-follow instructions will have you assembling code in a matter of hours.

As for emulation, once you have the chip, our Universal Emulator lets you get to work in an execute-only environment in just a few days. And full emulation capability is typically just a matter of weeks. Because we supply hardware and software that's about 80 to 90 percent complete. You do some interface design and complete the software package. Everything you need is supplied, including step-by-step instructions and a design example using a popular microprocessor. Compare this approach to the year or two you'd wait for normal support...if you get it at all. HP also provides full support for a host of 8-and 16-bit processors , with more on the way. So don't let lack of support slow you down or compromise your designs.

Marginal
Signal Conditions

No need to let marginal signal conditions and other timing related gremlins hold you up either. Because the 64000's timing analysis subsystem combines sophisticated triggering, high speed, 8k memory depth, and postprocessing for measurement capability not available in timing analyzers until now.

For example, our dual-threshold mode identifies noise problems and marginal signal levels. And helps you solve bus loading and bus conflict problems.

In the fast mode, 400 MHz speed yields the resolution necessary to resolve critical timing margin problems. New statistical analysis capabilities increase resolution and give useful data for system characterization. And the ability to trigger on transitions, pattern durations and post-processed data conditions give you valuable capabilities in studying control-signal timing relationships such as handshake related problems.

The 64000 Timing Analyzer sets new ease of use standards too. Directed-syntax softkeys simplify measurements. And label assignment lets you analyze results in terms of your system's nomenclature.

With this analyzer, you get to the root of timing problems fast.

Hardware/Software
Fingerpointing

Whose fault? Software or hardware? The 64000, with both timing and state subsystems, and even emulation, can resolve that quarrel in short order. That's because one subsystem can arm or trigger another for real-time interactive measurements.

For example, you can set the timing analyzer to trigger on a middle threshold that lasts too long. Then view state flow to see the affect. Or, you can trigger on state and view timing, which is useful for debugging I/O port malfunctions.

In analysis/emulation interaction, you might monitor software activity with the analyzer, then send a signal to the emulator to halt operation if a specific trace specification occurs. Now, you can study the analyzer trace listing around the suspected problem area. Or, use the emulator to examine register contents and control further operation.

Take this logical path in settling fingerpointing debates and you'll push those designs closer to production.

System...standardize on a system like this about problems like these:

Software Bottlenecks

The 64000, with software performance measurement capability, quickly eliminates these nightmares. Symbolic tracing makes measurements a programmer's dream. And histogram displays give you a graphic picture of bottlenecks and software inefficiencies. This new tool shows system activity as a function of software modules so you can see where the concentrated action is. You can determine how long it takes to execute a given module of code as you vary input parameters. See software traffic patterns. And compare software modules in terms of the percentage of time and occurrence they require in your programs.

These measurements are real-time, not post-processed trace data, which means you can interact with trace displays as well as perform overview measurements on single-shot events.

Software in the Weeds

That's where new software often ends up. But the 64000, with the state analysis subsystem, gets you back on track quickly. First, because this analyzer speaks a programmer's language. Symbolic tracing lets you define parameters in familiar source-code symbols and labels. For example, you can instruct the analyzer to find sequences and trigger points by module names and labels. And with HP's directed-syntax softkeys, defining a measurement is usually just a matter of a few keystrokes.

Inverse assembly means this analyzer speaks your microprocessor's language, too. That makes it easy for you to interpret displayed information, because now you don't have to convert analyzer displays to microprocessor mnemonics and symbols. All this in a real-time analyzer, not a simulator or intrusive run-until-search type of analyzer.

But it's also important to be able to position the measurement window with precision. We do that too.

Extended trace specification features let you navigate through complex code to the portion you want...and display only pertinent information. That's because you can combine trigger, store and count functions in any combination, to a total of eight terms, each as wide as the number of channels installed (to 120). Add to that the ability to define up to 15 sequence terms, or a combination of sequence terms and enable/disable windows, and there aren't many nooks or crannies where software bugs can hide. That means you'll debug software pronto.

One System for Standardization

From start to finish of the development cycle, HP's 64000 Logic Development System can help you speed your designs along. It covers software development, downloading, emulation, hardware and software analysis, and system performance measurements. All with a single keyboard and display that speeds setups and simplifies measurements.

You can choose from two system stations, too. One benchtop station, with 10 card slots, gives you the most expansion capability. The transportable station, with 5 card slots, is a popular development unit for individual bench and field use.

Whichever station you choose, you can configure for dedicated function or combination measurements. You can use each in a standalone situation or as part of a multiuser, distributed processing network. It's a development system that makes sense for labs both large and small.

For details on the 64000 Logic Development System and available subsystems, call your local HP sales office listed in the telephone directory white pages. Ask for your HP field engineer in the Electronic Instruments Department.

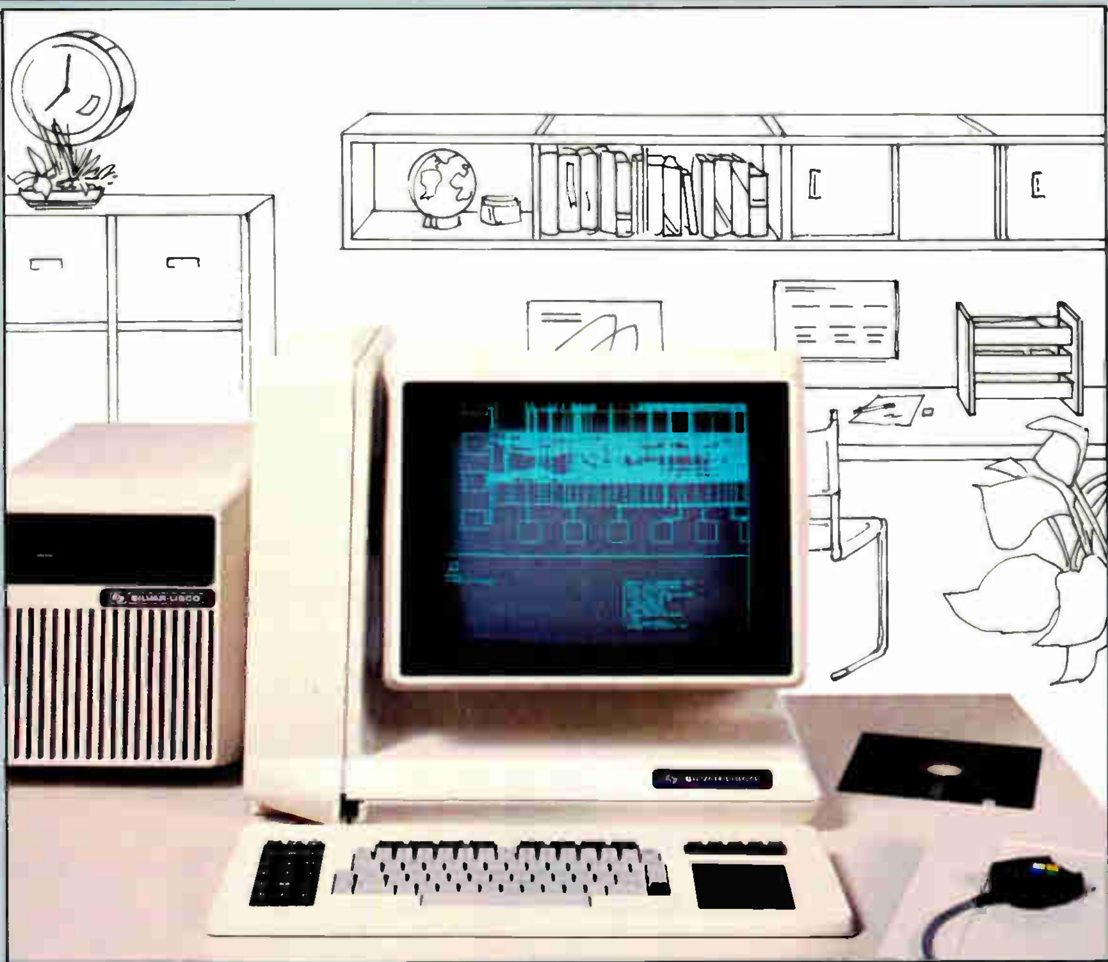
HP-IB SYSTEMS

HP-IB: Not just IEEE 488, but the hardware, documentation and support that delivers the shortest path to a measurement system.

HEWLETT PACKARD

Circle 249 on reader service card

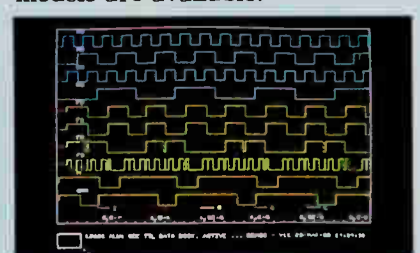
Silvar-Lisco Has Every Standard Cell Devices



Many companies claim to provide input-to-artwork workstations for computer-aided engineering. Silvar-Lisco delivers.

Design Capture
For example, both the StarCell™ standard cell workstation on the left and the StarGate™ gate array workstation on the right let you enter design data interactively, alpha-numerically, or with a digitizer, or with the netlist automatically extracted. But that's only the beginning.

Simulation
On both systems you can perform design simulation all the way from functional system level to the gate and transistor level, independent of the IC technology involved. Libraries of pre-characterized logic models are available.



BIMOS™ Simulation

Standard Cell Layout
With the StarCell system you can turn your system design into a small-size, low-cost die with all the advantages of fast turnaround that semi-custom technology provides. (For starters, you can lay out 5000 gates in less than one hour!) In addition, you can extract electrical circuit characteristics from the layout and feed them back into the design data base for ultra-accurate circuit simulation.

Gate Array Layout
With the StarGate system you can tackle gate arrays of thousands of gates in single- and double-layer metallization. The StarGate system offers fully automatic layout and routing, and optional interactive editing. With our unique router you get maximum gate utilization, along with

thing You Need to Design and Gate Arrays. Fast.

the ability to route through cells as well as channels. Upon request, we'll provide you with the macro cell libraries of your favorite silicon vendor.

Create Your Own Tools

When you work with Silvar-Lisco, you can choose from eighteen software/hardware combinations, or create your own "dream" workstation from our broad range of software tools. Our software products also run on popular large computers such as VAX, IBM and Prime, as well as our microcomputer-based Apollo turnkey workstations. So when your computing needs grow, our products will already be in place to support you. Interfaces to other non-Silvar-Lisco CAE tools are also available.

For more information, call or write Silvar-Lisco, 1080 Marsh Road, Menlo Park, CA 94025, (415) 856-2525. In Europe, contact Silvar-Lisco, Abdijstraat 34, B-3030 Leuven, Belgium, (016) 20 00 16, Telex 22128. In Japan, contact C. Itoh & Co. Ltd., 5-1 2-chome, Kita-Aoyama Minato-ku, Tokyo 107, Japan, 03 497 3203, Telex J22295.

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StarCell, StarGate and SL-2000 Software Family are trademarks of Silvar-Lisco.

The SL-2000 Software Family™

Name	Function
SDS™	design capture
HIDEX™	hierarchical logic design
HIPAR™	hierarchical design partitioning
HELIX™	system level behavioral simulation
BIMOS™	gate and transistor level simulation
GARDS™	automatic gate array placement and routing
CAL-MP™	automatic standard cell placement and routing

Turnkey Workstation Hardware*

	SL-2300	SL-2400	SL-2600
hard disk capacity	34 MB	68–158 MB	68–158 MB
main memory	1.5 MB	2.0 MB	2.0 MB
display	17-inch monochrome	19-inch monochrome	19-inch color

*Apollo-based hardware with AEGIS operating system and DOMAIN network interface. All systems are provided with full keyboard and "mouse" for graphics input. Optional RS-232C communications link to mainframe computers available.

Circle 25 on reader service card

Instruments

Signal analyzer suits many jobs

High-performance portable unit acts as waveform recorder or spectrum or network analyzer

Dynamic signal analyzers for audio and vibration work generally fall into the heavy, expensive, high-performance category or the lightweight, inexpensive, low-performance group. But the 3561A offers, at 33 lb and approximately $10,000, better performance than any current instrument of its kind, states Hewlett-Packard. The single-channel unit can be used as a waveform recorder (for signals with components as high in frequency as 100 kHz), as a spectrum analyzer, or, thanks to its band-limited band-translated noise source, as a network analyzer.

Use of fast-Fourier-transform techniques puts the 3561A head and shoulders above swept-spectrum analyzers, for it can make measurements in a fraction the time the latter require. Its 80-dB dynamic range is unique, says HP, and its amplitude accuracy of ±0.15 dB unequaled. A cross-hair marker with an amplitude resolution of 0.01 dB lets the user make automatically calibrated measurements rapidly.

The instrument's measurement range spans 158 dB. With its flexible zoom capability and spans as narrow as 0.25 Hz anywhere in the 100-kHz range, giving up to 625-μHz resolution, it is useful for measuring distortion, noise floor, and spurious response, for performing modulation analysis, and for many other tasks.

Its noise source, which tracks the frequency and span selected, puts out periodic, random, and impulse signals for amplitude or phase network measurements over the full 100-kHz range. As a network analyzer, it might typically be used for characterizing the frequency response of analog, crystal, or switched-capacitor filters, baseband amplifiers, modems, and weighting filters, among others.

The 3561A, which is fully programmable over the IEEE-488 HP Interface Bus, records waveforms with a 13-bit analog-to-digital converter running at 256,000 samples/s, achieving 80 dB of alias protection. In its time-capture mode, it can store nearly 41,000 samples (equal to 40 time records) to record long and one-time transient events.

A spectral-map mode allows the 3561A to display up to 60 map spectra to identify trends in machines or circuits that contain unwanted harmonics. Run-up or coast-down analysis can be done; the map mode adds a third dimension of time, revolutions per minute, drive load, or other variable to the display.

Calculations. A number of features make the unit attractive for electronic analysis. It offers direct digital plotting and linear and logarithmic scales, performs trace math, and has single, dual, harmonic, and sideband markers. Log-frequency modes include a simple redistribution of linear points and both 1/3- and full-octave proportional resolution. Displays can be calculated in whatever units the user finds convenient.

An A-weight filter is provided to make measurements for acoustic analysis easy, and a constant current source in the unit powers integrated-circuit piezoelectric accelerometers, eliminating the need for separate power supplies. The ability to set the sample rate with an external signal can be used in machinery analysis to normalize the frequency display to the speed of rotation.

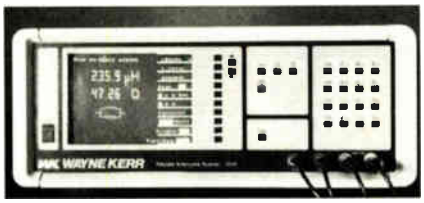
Manual use of the 3561A is simplified by means of menus, soft keys, and versatile software. The unit automatically calibrates itself to maintain its measurement integrity.

An optional 127-record magnetic-bubble memory adds about $1,500 to the 3561A's price. Deliveries are in six weeks.

Hewlett-Packard Co., Inquiries Manager, 1501 Page Mill Rd., Palo Alto, Calif. 94304
[Circle reader service number 351]

Inductance analyzer works over 20-Hz-to-300-kHz range

The 3245 precision inductance analyzer—which sports all the stimulus-reponse, measurement, and computation facilities necessary for analysis of coils, transformers, and other inductors—can drive, bias, and measure inductances at frequencies rang-



ing from 20 Hz to 300 kHz. A basic accuracy of ±0.1% is maintained for any component with impedance from 1.23 Ω to 330 kΩ between 100 Hz and 10 kHz. Resolution is ±1 nH at 199 kHz.

The instrument can be used for precision measurements of components in a laboratory, as well as high-volume testing and sorting of components during incoming inspection. Test setups, stored in nonvolatile memory, appear on the 3245's video display. Once the test setup is chosen, the analyzer guides the operator through a trimming procedure to compensate for stray inductance or capacitance in the test leads.

The analyzer permits major terms (such as L, C, Z, and R_{dc}) to be displayed along with appropriate units. Minor terms (Q, for instance, or dissipation factor), selected by the operator, can be simultaneously computed and displayed. Complex inductances like transformers, inductive components of such devices as wirewound resistors, and printed-circuit board traces can be measured and evaluated, without a dedicated test setup or off-line computations.

Throughout the test, the equivalent circuit being measured is displayed schematically on screen. The unit can sort components into 10 bins by preset categories, such as nominal inductance or insufficient Q, preset by operators. Extensive output and remote control facilities allow the 3245 to be networked within an automatic parts-handling station. The output, the input, and the test setup may be sent to a controller or to a printer through RS-232-C or IEEE-488 ports.

The model 3245 precision inductance analyzer sells for $7,995. Delivery takes 60 days.

Wayne Kerr Inc., 400 West Cummings Park, Woburn, Mass. 01801. Phone (617) 938-8390 [Circle 353]

Development system serves numerous TI processors

Designed to provide users with high-performance, low-cost, and high-productivity tools for hardware and software development, the host-independent XDS (Extended Development Support) allows users to select the Texas Instruments processors best able to solve their problems.

Coupled with a transportable set of development and debugging tools, this configuration emulates in circuit such processors as the TMS320 family of digital signal processors, the TMS7000 family of 8-bit single-chip microcomputers, the TMS9995 microcomputer, and the TMS99000 series. The XDS family supports RS-232-C downlink capabilities and real-time target-system debugging with breakpoint and trace capabilities.

Potential applications for XDS range from timers in clock radios to intelligent speech-recognition peripherals in large mainframes. When extensive code is involved, TI's XDS model 33 provides high-level–language (XMPL) control of the whole debugging process and logic-state tracing. Simpler applications are well suited to the XDS model 22, without the XMPL language.

Versions of the XDS model 22 for the TMS320 signal processor and the TMS7000, 9995, and 99000 microprocessors are now available at a cost ranging from $2,550 to $5,000. Model 33 systems for the four TI processor families, which will be available in the fourth quarter, will cost $7,050 and upwards.

Texas Instruments, Semiconductor Group, Literature Response Center, P. O. Box 401560, Dallas, Texas 75240 [Circle 354]

Analyzer uses bit-slice processor technology

The LeCroy 3500SA/100 high-speed signal analyzer is decked out with high-throughput signal averaging for fast signal-to-noise enhancement, 10-ns time resolution, 8-bit amplitude resolution, and multiwaveform processing capabilities. It can acquire, digitize, process, and archive (on floppy disks) fast analog signals.

Using bit-slice processor technology, the analyzer can average more than 700 waveforms/s for a 1,024-point waveform and can achieve a signal-to-noise ratio improvement (in noisy signals) of more than 100 : 1 in only 14 s. Averaged waveforms may have up to 8,096 points. A 1,024-point fast Fourier transform can be undertaken on recorded waveforms. An RS-232-C serial port is standard.

Fast pulsed measurement applications, such as kinetic chemistry, biochemical reactions, and materials research, can benefit from the system's speed and versatility. A full-feature CP/M-based computer that permits further data manipulation and the use of other CP/M programs, the system comes with Fortran or Basic.

The 3500SA/100 system, including a single-channel waveform digitizer (100 megasamples/s, 10-ns time resolution), a display and processor console, and a dual 8-in. floppy-disk system, costs less than $20,000. Delivery is in 30 days.

LeCroy Research Systems Corp., 700 South Main St., Spring Valley, N. Y. 10977. Phone (914) 425-2000 [Circle 355]

Drive test systems handle Winchesters, floppies, cartridges

The QA3000 family includes the only fully integrated disk-drive test systems that handle not only Winchesters but also floppy-disk and cartridge drives. Its six separate models are designed to test 3½-, 5¼-, or 8-in. drives.

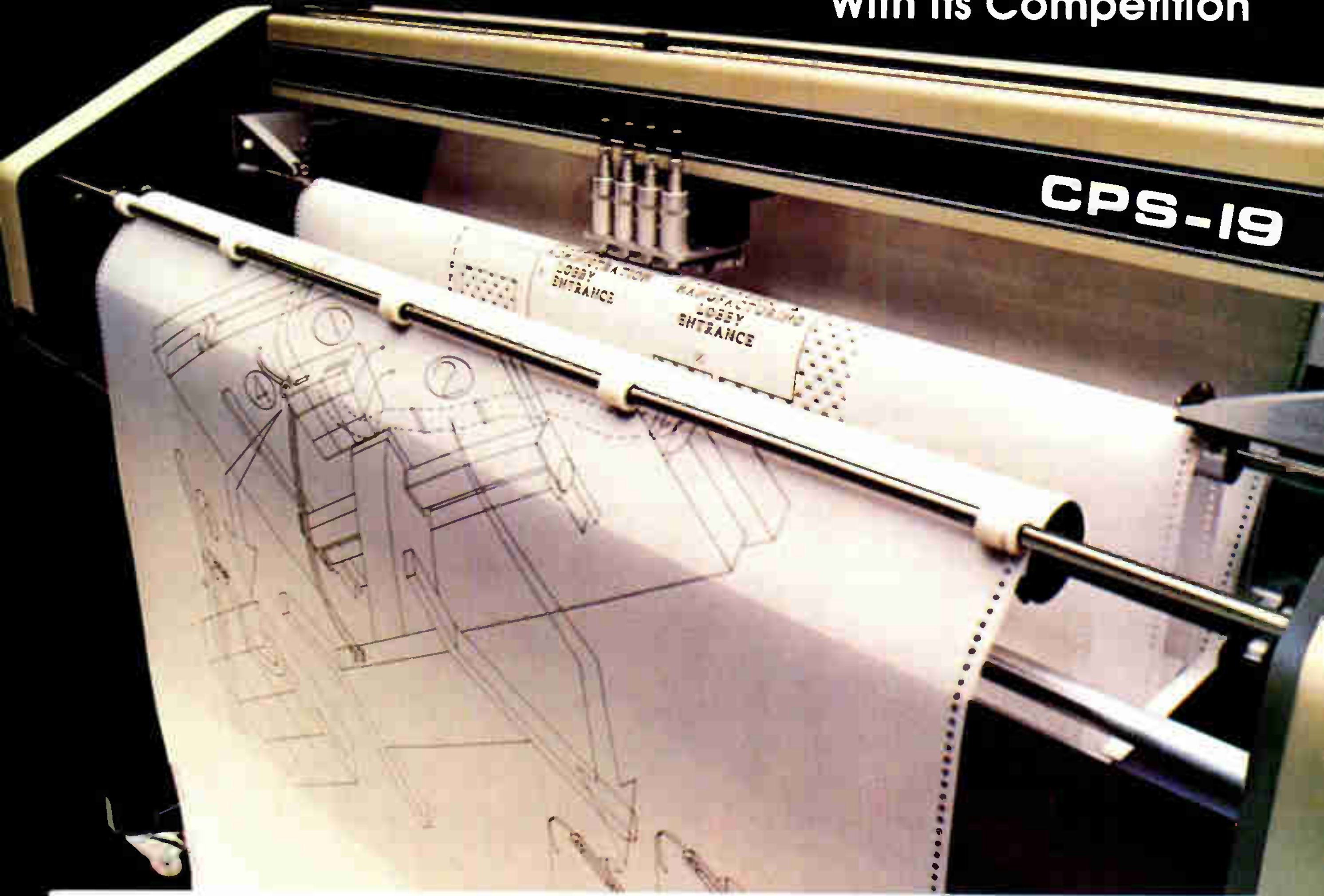
Designed for disk-drive manufacturers, system integrators, and field-service engineers, the QA3000 gives users more than 50 interactive test routines, including phase-margin testing, vital for determining the quality of the drive's head and read-write channel interface, and a surface-scanning test that allows users to detect the location of media flaws. The units can test as many as four drives at once and can be used to write specialized test programs.

The QS3000 family's multilayered circuitry, highly stable components, and phase-locked–loop design permit users to achieve accurate test results, repeatable to within 2 ns. The family's architecture, based on six microprocessors and a high-speed controller, ensure consistent speed and throughput. Also provided is networking through QNET, which can tie one or more QA3000s to a minicomputer host. Pricing ranges from from $13,000 to $16,000.

Qubex Associates Inc., 2090 Concourse Dr., San Jose, Calif. 95131. Phone (408) 945-0551 [Circle 356]

For Value Received

Compare The Houston Instrument CPS-19 With Its Competition



We invite comparison on the basis of quality, reliability and performance... even though the comparison may seem unfair since the Houston Instrument CØMPLØT® costs much less than the competition. The competitive edge of the CPS-19 is based on solid design and meaningful capabilities. The end result is a highly cost effective 34.5" four-pen plotter that performs tirelessly and flawlessly on its owner's behalf. At its highly competitive price*, the Houston Instrument CPS-19 full-size plotter is thousands of dollars more affordable than others of comparable performance.

The CPS-19 will continue its thrifty ways far beyond the time of initial purchase. For instance, the CPS-19 will plot unattended, delivering drawings of up to E size, without interruption, on through the night and into the dawn. Since paper feed is continuous you can generate drawings at a time that's right for you or your system, rather than being restricted by an '8-to-5' plotter.

Finally, compare plot quality. The CPS-19 is an evolutionary stage beyond stepper-motor technology. Rugged servo drives incorporate both position and velocity feedback loops to tightly control pen and paper movement. The result is curves drawn with grace and precision, and straight lines of unerring accuracy.

For the name, address and phone number of your nearest representative, write Houston Instrument, 8500 Cameron Road, Austin, Texas 78753. Phone 512-835-0900, or 1-800-531-5205 if outside Texas. In Europe contact Bausch & Lomb Belgium NV., Rochesterlaan 6, 8240 Gistel, Belgium. Tel 059-27-74-45. Tlx 846-81399.

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Circle 257 on reader service card

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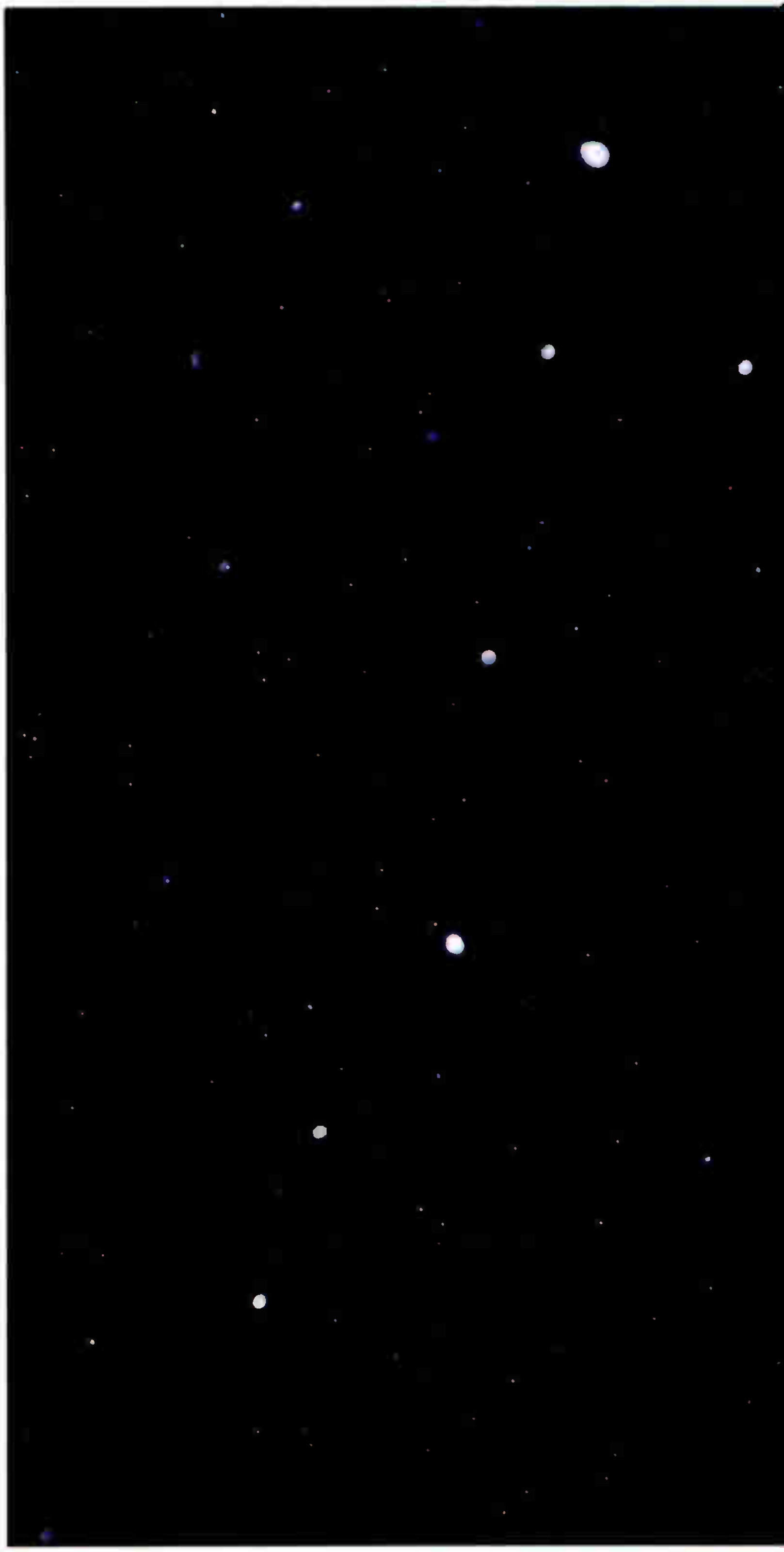

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The UF4002 ultra fast switching rectifier has reverse recovery time less than 50 nanoseconds! Plus other excellent features:

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***Conditions of Sale:**
Minimum order quantity 50,000 units scheduled within 60 days. Minimum shipment 25,000 pcs.
Packaging: 1,000 units per box, or 5,000 units per reel.
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GENERAL INSTRUMENT

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Broad line.

We're more than doubling our product line. By year-end we'll have 98 devices, both n- and p-channel types. These MOSFETs will cover a broad range of voltages (50 to 500V) and current levels (1 to 45A), including a new 45A, 60V device with $R_{DS(ON)}$ specified at only 0.04Ω maximum.

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Our prices are surprisingly low. That's because our cell packing density is the highest in the industry.

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Unequalled quality and reliability. These state-of-the-art processes have also enabled us to achieve an AOQ level of 100 ppm, and an amazingly low 0.0012%/1000 hours FR @ 75° C.

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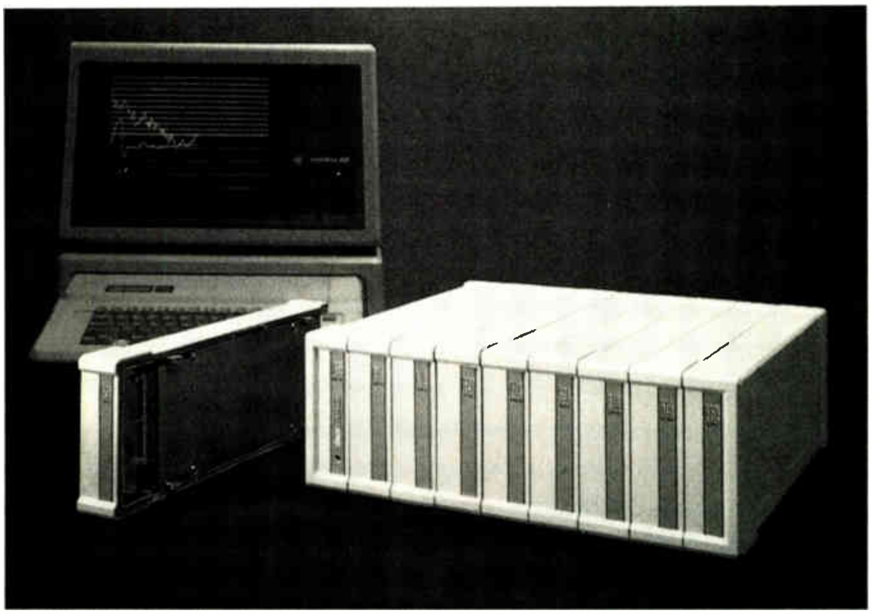
Data acquisition

Modular system links to Apple

Data-acquisition and control unit has local controller, high degree of noise immunity



A modular data-acquisition and control system designed as the front end for an Apple II computer has individually isolated floating inputs and outputs with a high degree of noise immunity. The Acrosystem-800 is controlled by its own 8088-based microcomputer and comes with Apple software that simplifies operation.

The system's modules interlock to form a single unit with a power supply module on one end, a microprocessor control unit on the other, and up to eight input/output modules between them. Any combination of I/O modules, in any order, can be used without change to the software or to the Apple interface. Tools are not needed to set up or to rearrange the configuration of modules.

The proprietary circuit that individually isolates and floats the I/O lines helps give the system its high immunity to noise on low-level input lines, ground loops, and equipment ground lines. The ground lines of personal computers, the manufacturer observes, are notoriously noisy.

To minimize errors resulting from noise still further, integrating dual-slope analog-to-digital converters change inputs slowly. Noise is also cut because the switching power supply's internal frequency is synchronized with the system clock.

First-timers can use Applesoft Basic commands in their simplest form; no additional commands or special languages must be learned. As users gain experience, they can increase the sophistication of system operation by expanding the formats available with Applesoft Basic commands. Throughput can be raised with compiled Basic, Pascal, Fortran, assembly language, and the ProDOS operating system.

At power-on, the processor automatically identifies all modules in the system and displays the information on screen with a menu of choices. At the same time, it initializes the modules to a known state and runs system diagnostics, displaying warnings of possible malfunctions.

Software aids. An on-line help facility will, on demand, display the instruction formats for each module in the system. Other software permits users to measure their programs' execution times and provides several types of displays to monitor the system and analyze the data.

The 810 general-purpose I/O module provides medium-speed analog and digital I/O, four analog-input channels digitized to 12-bit resolution with a 200-μs conversion time, and 16 digital I/O lines with anticoincidence logic. Contact-bounce suppression is available in software.

A thermocouple input module (model 820) has six channels, on-board cold-junction compensation, linearization, and conversion to degrees Celsius. Any type of J, K, T, R, or S thermocouple can be connected to any input. A 16-bit integrating dual-slope a-d converter with a 400-μs conversion time is used.

The 821, another six-channel input module with 16-bit integrating dual-slope conversion, is designed for use with pH meters or pressure transmitters. Its common-mode rejection ratio is 80 dB. The 827, a six-channel unit for resistance temperature detectors, gives them 1-mA excitation; the 828, a four-channel unit for 120- or 350-Ω strain gages, puts out 5- or 10-V bridge excitation and also has on-board linearization and units conversion.

The rejection ratios of the 827 and the 828 are 80 and 110 dB, respectively. An additional analog-output module is under development, as is one for digital I/O that includes counters and pulse-frequency measurement at up to 500 kHz.

The system is designed for use in on-line monitoring of processes, operations, or separately controlled tests; for burst-mode data acquisition during trigger-controlled intervals; and for automated testing and control of processes, operations, and time sequences. Modules range in price from $650 to $1,000; the control unit and power supply together are $1,550. A typical price for a total system, including the Apple computer, might range from $6,000 to $7,000. Deliveries start in January.

Acrotechnology Corp., Acrosystems, 66 Cherry Hill Dr., P. O. Box 487, Beverly, Mass. 01915. Phone (617) 927-8885 [381]

ECL-compatible d-a converter settles in just 35 ns

The HC4000, a high-speed emitter-coupled-logic–compatible 12-bit hybrid digital-to-analog converter, can replace the ADH-030 in both military and in commercial applications. It uses 12 fast, closely matched 4-mA current switches to drive a precision thin-film-resistor R-2R ladder network connected to a time- and temperature-stable internal voltage reference. The d-a converter is housed in a hermetically sealed, 24-pin, dual in-line package.

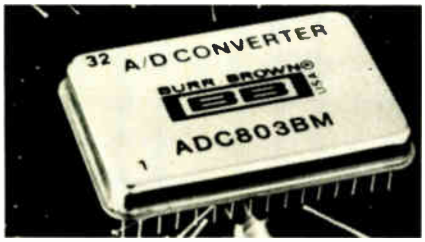
Available in commercial and military versions, the converter is a current-output device with a 35-ns settling time to 0.0125% of full scale (50-ns maximum) and a 50-MHz minimum update rate. For a voltage output, both models can be connected to a high-speed fast-settling operational amplifier. Over their respective operating-temperature ranges—0° to +70°C and -55° to +125°C—the commercial and military versions guarantee integral and differential linearity errors no greater than 5 ppm/°C and typical gain and zero offset errors no greater than 25 and 10 ppm/°C, respectively.

The d-a converter is suitable for such cathode-ray-tube applications as X-Y deflection and discrete data-point plotting, for precision high-speed analog-to-digital conversion, and for such current- and voltage-controlled functions as oscillators, power sources, and active electrical-signal filters. In small quantities, which are available from stock, the commercial version sells for $149, the military one for $344.

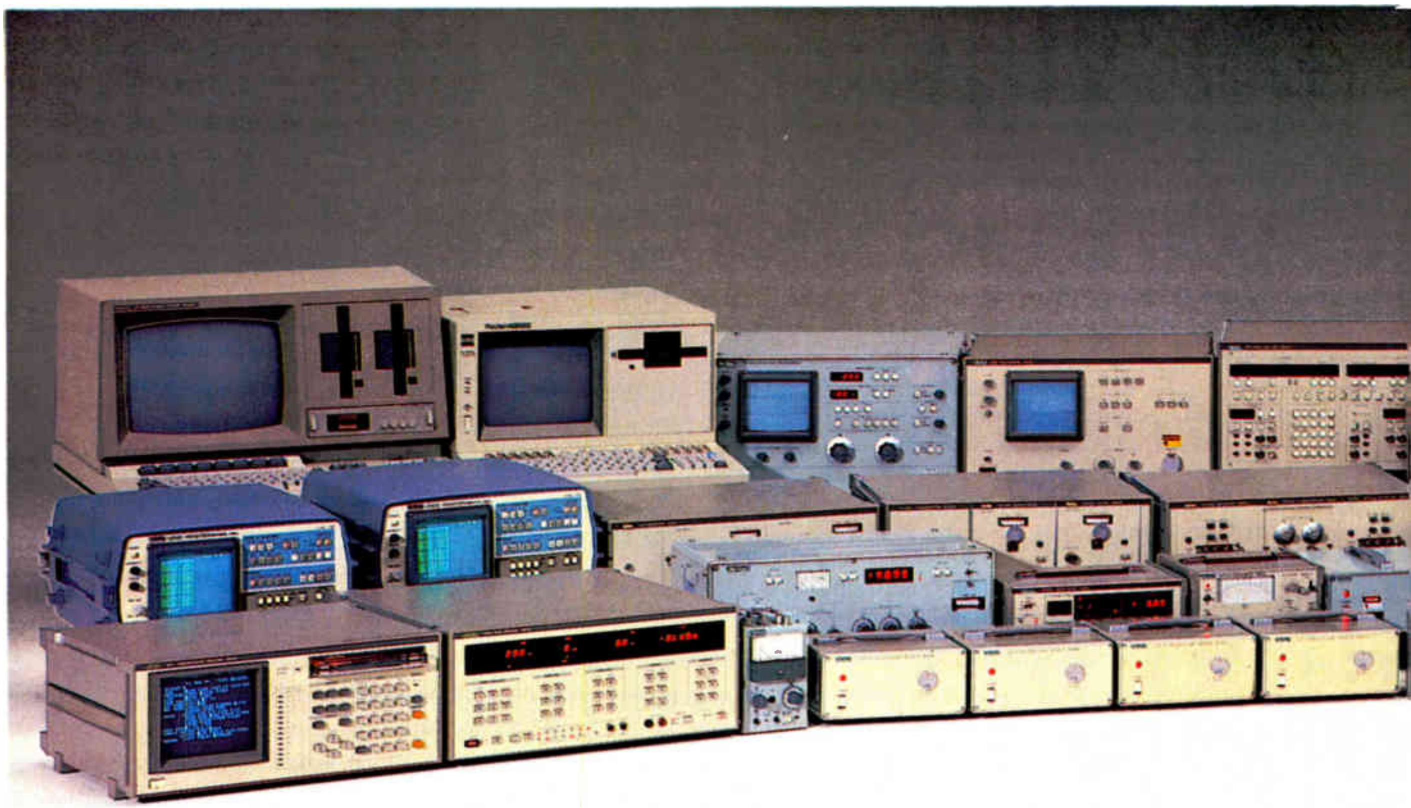
HyComp Inc., 75 Union Ave., Sudbury, Mass. 01776. Phone (617) 443-4631 [Circle 383]

12-bit converter works in 1.5 μs with no missing codes

The ADC803, a 12-bit successive-approximation analog-to-digital converter, accurate to ±0.015% and operating with no missing codes over a -25° to +85°C temperature range, boasts a conversion speed of just 1.5

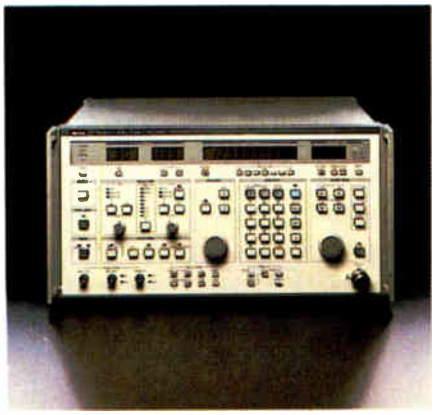


Better Instruments for Better Communications



The MG655A Synthesized Signal Generator

For the testing of AM and FM communications receivers, especially those that absolutely require a highly stable, high-purity signal – anywhere in the range from 100kHz to 1300MHz. Resolution is within 1Hz (or 2Hz above 650MHz), and frequency drift is less than $\pm 5 \times 10^{-8}$ per day. Naturally, GPIB is standard equipment. The MG655A: It's another stellar performer in the Anritsu lineup.



Anritsu means communications.

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optical and digital transmission systems, Anritsu communications products are highly regarded for both unequalled reliability and technical excellence.

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Anritsu builds the electronic instruments that keep electronic and fiber optic communications operating at the knife edge of efficiency. From the simple measurement of voltage and current to complete high-level analysis of both analog and digital circuitry, Anritsu instruments are built by experts in communications. And Anritsu instruments are built to be used.

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Phone (03) 446-1111/Telex: 0-242-2353
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Circle 265 on reader service card

μs. In a 32-pin hermetically sealed dual in-line package, the ADC803 converter uses integrated circuits and laser-trimmed thin-film components to achieve a complete a-d function, including voltage reference, clock, and comparator. Input scaling resistors provide internal selection of analog-input ranges of 0 to −10 V, ±5 V, and ±10 V.

Output data is available both in serial and parallel formats. The converter's output codes are complementary binary for unipolar inputs and bipolar offset binary for bipolar inputs. All digital inputs and outputs are TTL-compatible.

The ADC803's differential-input–comparator design makes inputs easy to drive. The internal d-a converter drives a comparator input separate from the input signal, a technique that eliminates the need for an expensive fast-settling amplifier because the user's driving circuitry does not have to handle the d-a converter's transients. In small quantities, the converter sells for $214.

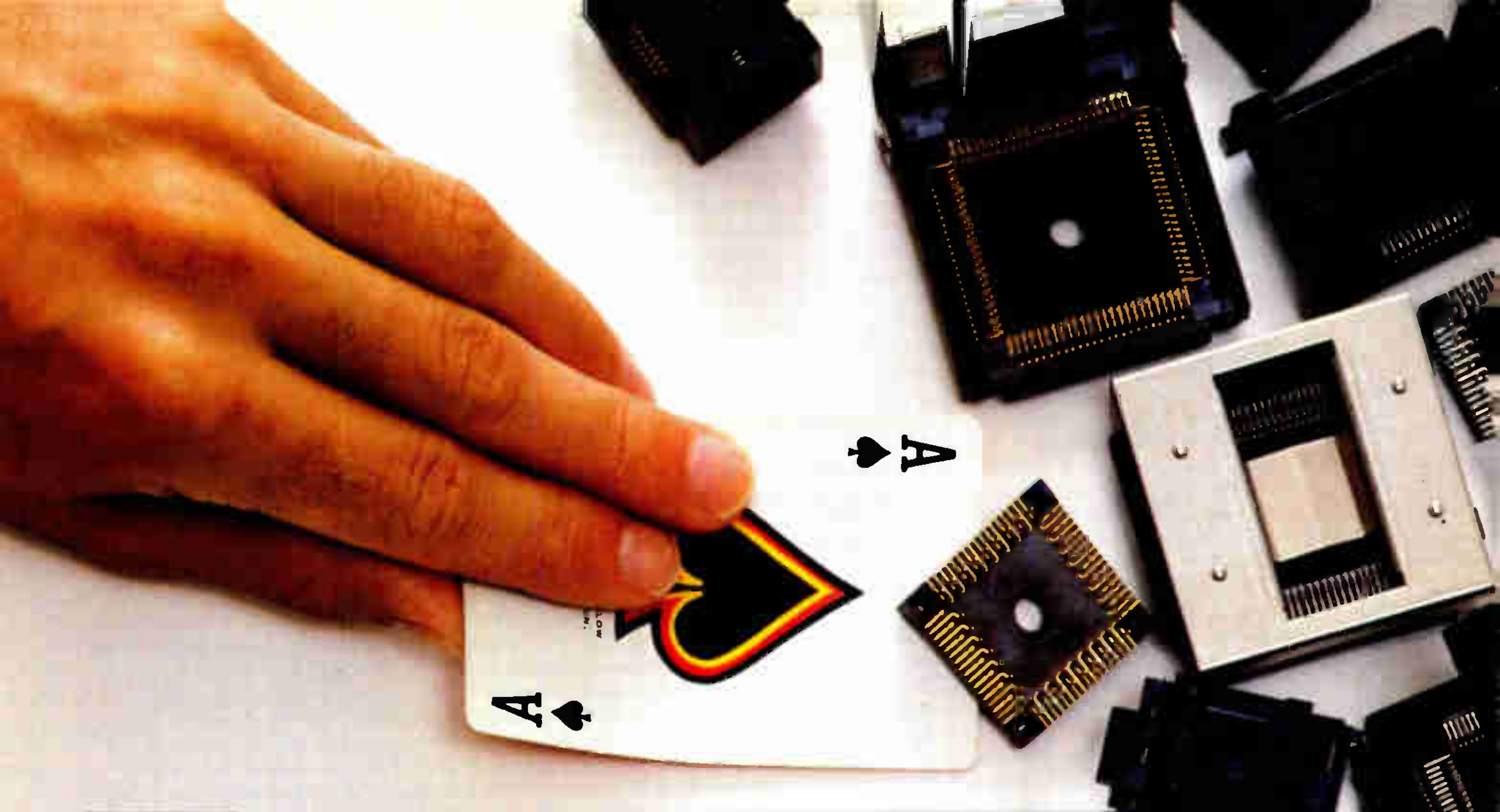
Burr-Brown Corp., International Airport Industrial Park, P. O. Box 11400, Tucson, Ariz. 85734. Phone (602) 746-1111 [Circle 384]

Track-and-hold amplifier claims 5-ps aperture jitter

The HTS-0010 track-and-hold amplifier, which guarantees a maximum aperture jitter (uncertainty) of just 5 ps, has an acquisition time of 14 ns. The hybrid has a small-signal bandwidth of 60 MHz and a droop rate no greater than ±0.1 mV/μs.

The part's typical slew rate is said to be 300 V/μs. Its minimum full-power bandwidth is rated at 40 MHz, and its feedthrough rejection is typically 62 dB when measured with a 10-MHz input signal. Other key features include a maximum gain linearity of ±0.01%, with a 1-V full scale; a maximum gain drift of 40 ppm/°C for the K grade (an operating temperature range of 0° to +70°C); and a maximum gain drift of 50 ppm/°C for the S grade (−55° to +100°C).

The track-and-hold amplifier is suitable for use in front of flash en-



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Circle 267 on reader service card

coders in data-acquisition applications, in deglitching the output of a digital-to-analog converter, and in radar and medical electronic systems. In lots of 100, pricing ranges from $315 to $368; delivery is from stock. Analog Devices Inc., Computer Labs Division, 7810 Success Rd., Greensboro, N. C. 27409. Phone (919) 668-9511 [Circle 385]

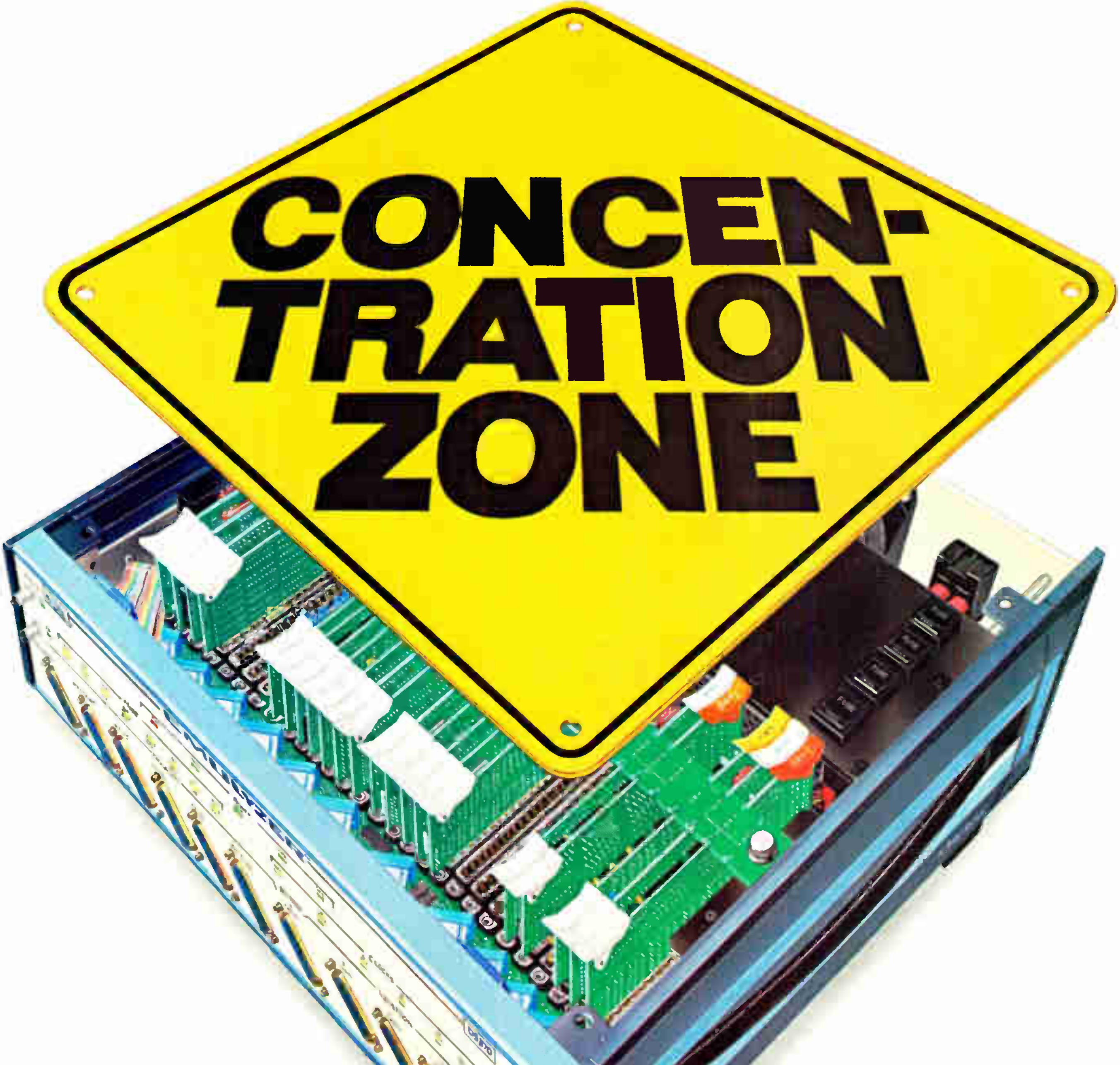
8-bit C-MOS converter carries fast internal clock

An 8-bit complementary-MOS successive-approximation analog-to-digital converter with a total unadjusted error as low as ±½ least-significant bit has an internal clock and a maximum conversion time of 40 μs. The converter's total unadjusted error includes nonlinearity, full-scale, and zero-scale errors.

Designed to operate from the control bus of many microprocessors, the ADC0844 can be used either ratiometrically or with a fixed voltage reference for system applications requiring absolute accuracy. Three-state output latches that directly drive the data bus permit the unit to be configured as either a memory location or an input/output device to a microprocessor—without interface logic. In addition, the converter's reference can be adjusted to permit the conversion of reduced analog ranges with 8-bit resolution.

The device requires no zero- or full-scale adjustments and uses a single 5-V power supply to accommodate an input range from 0 to 5 V. Within the ADC0844 is a four-channel analog multiplexer that can be configured in any of three operational modes: differential, single-ended, or pseudodifferential. Each mode can be selected by loading the multiplexer address latch with the proper address.

Available from stock, the converter, which comes in a 20-pin dual in-line package, sells for $4.60 each in small quantities. In lots of 100 to 999, the price drops to $3.85 each. National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 721-5000 [Circle 386]



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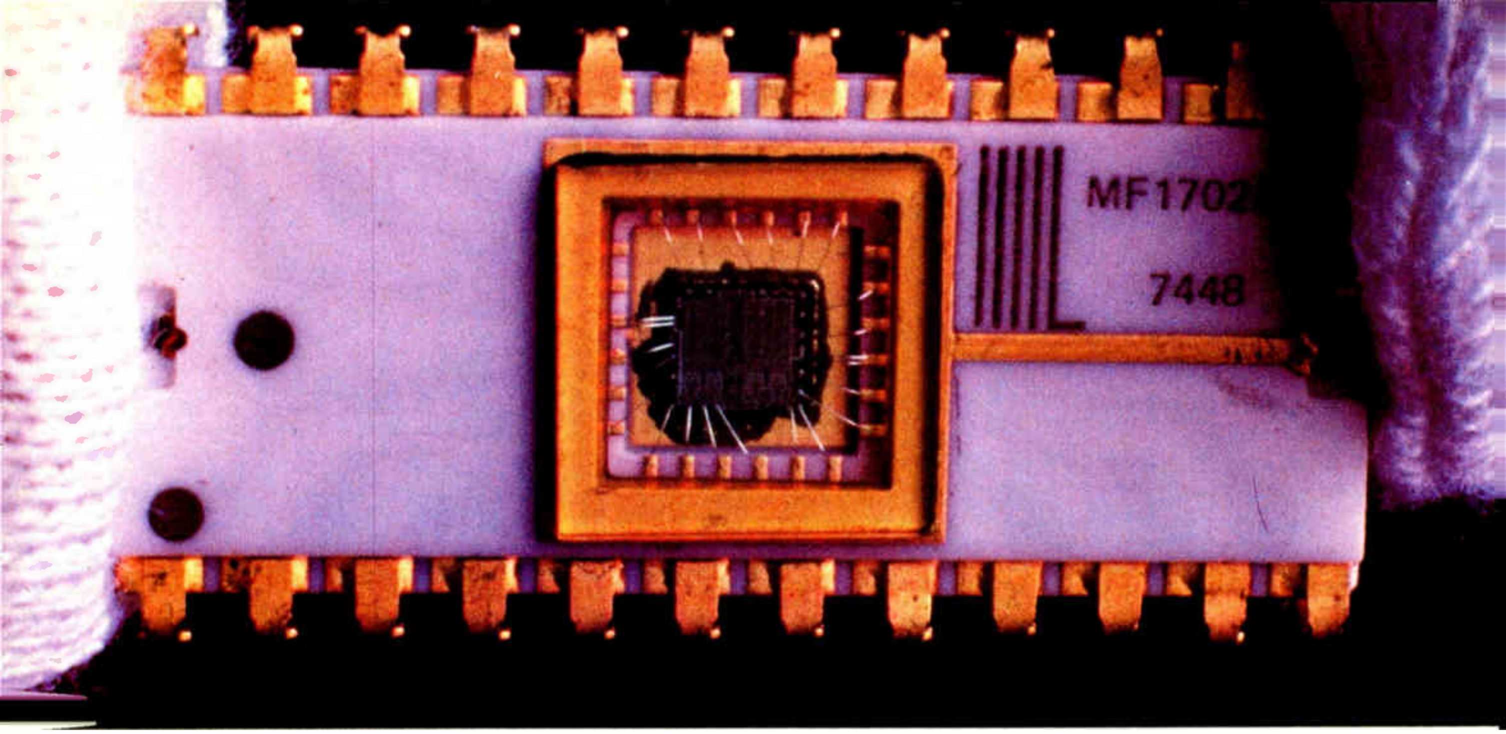

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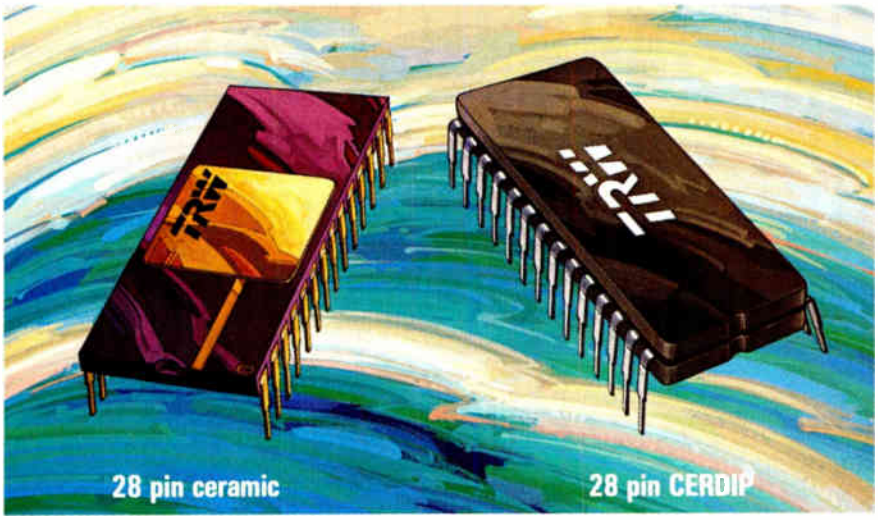

TRW LSI products, the industry leader in high performance A/D converters, announces the TDC1048, our new 8-bit video speed A/D.

The TDC1048 is the optimum solution to your high performance conversion problems. High speed—20 MSPS. Low power consumption—1.4W. Small package—28 pin ceramic or CERDIP. Low cost—$98.* This data conversion breakthrough is made possible by our proven one micron bipolar OMICRON-B™ process.

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Features such as 1/2 LSB linearity, differential phase of 1°, and 2% differential gain make the TDC1048 perfect for video, data acquisition, radar, ultrasound, robotics and image processing applications.

Samples are available now—production quantities available late '83/early '84. For data sheet, call or write our Literature Service Department:

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619.457.1000

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*U.S. price in 1000s.

TRW

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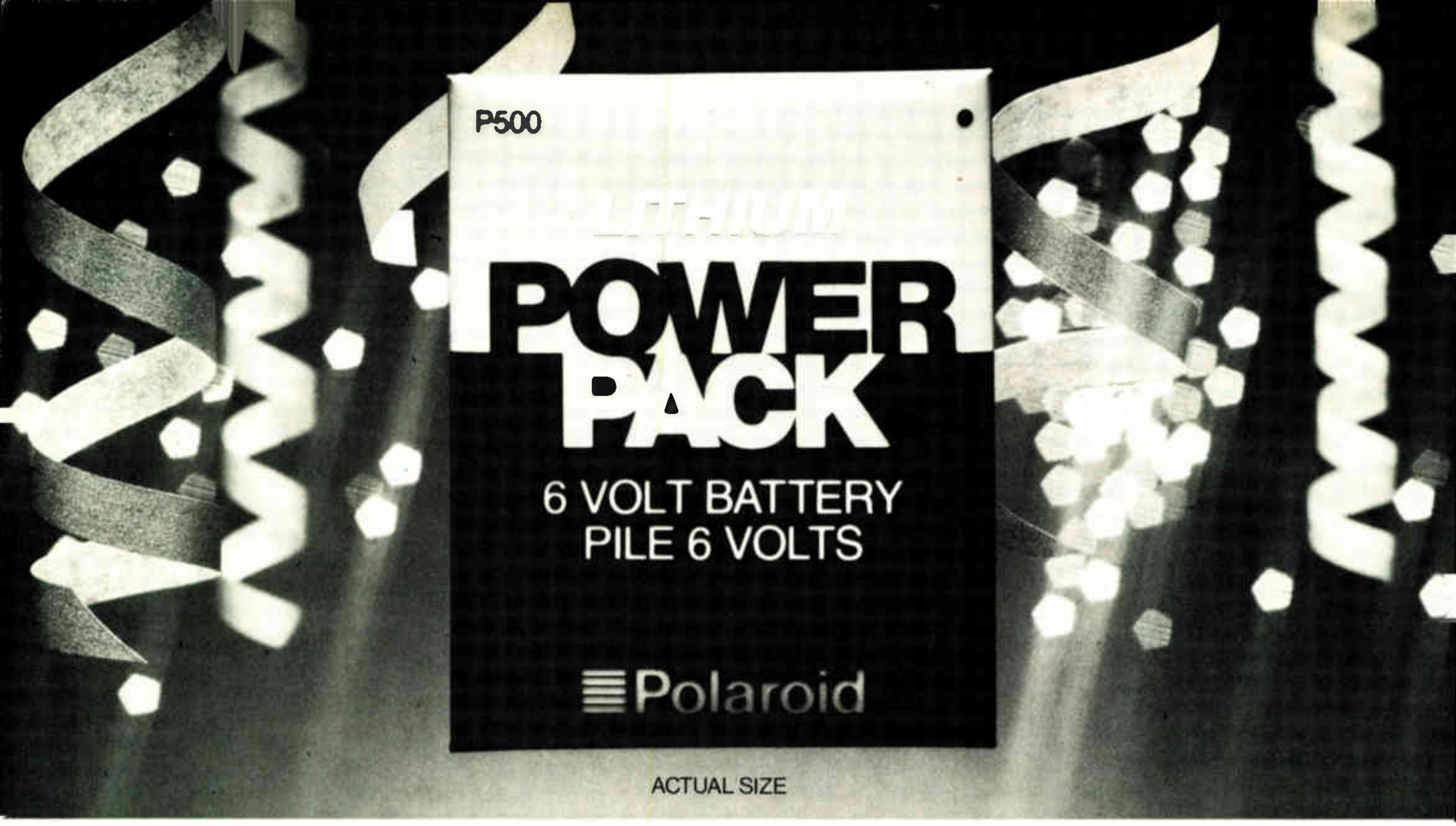

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The P500 is big for its size, though. In fact, it's the highest-energy 6-Volt lithium battery available for consumer replacement use.

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Safe to use; convenient for your customers.
The P500 Lithium Power Pack, like the Polapulse P100, with both contacts on the back of the battery and "card-in-slot" replacement, eliminates the possibility of polarity reversal. The P500 is also hermetically sealed to prevent leakage. And it has an anticipated shelf life of at least 5 years under normal use.

All this and less.
For all their power, compactness, flexibility, and safety, Polaroid's battery products are also affordably priced.

So whatever you produce can be more profitable, more powerful, and more compact when you design in the P500 Lithium Power Pack or Polapulse P100.

With that in mind, what are you waiting for? Call Polaroid at (617) 577-4681 for more information. To receive our Designer's Kit send a check or money order for $22.50, plus applicable sales and local taxes, to the Polaroid Corporation, Commercial Battery Division, Dept. E11, 784 Memorial Drive, Cambridge, MA 02139. Each kit contains 2 Polapulse P100 batteries, 2 P500 Power Packs and 1 molded battery holder.

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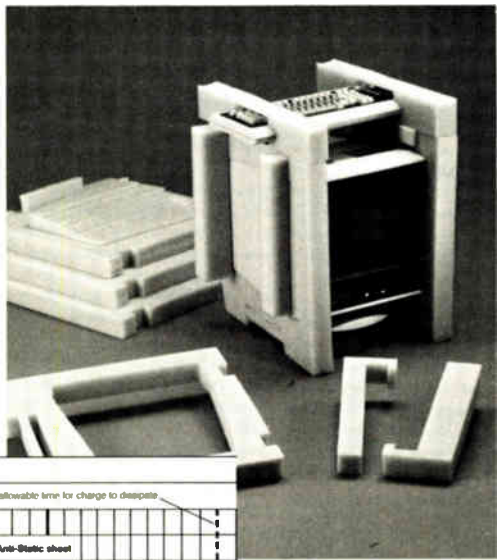
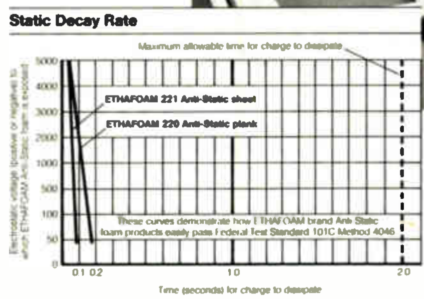
Announcing ETHAFOAM* Brand Anti-Static Polyethylene Foams

for protecting sensitive electronic products from static damage in process, in transit, and in storage.



Now you can help protect your delicate, high-value electronic products from electro-static damage with ETHAFOAM brand Anti-Static foam products.

These polyethylene foams have an internal anti-static agent which reduces static potential within the foams themselves. And they have the ability to dissipate static discharge from other sources which could damage your sensitive products. These properties remain virtually unaffected throughout normal service life of the foams. What's more, the foams meet a government standard set for anti-static materials.



Get anti-static protection along with traditional performance and cost benefits of ETHAFOAM.

ETHAFOAM Anti-Static polyethylene foams provide the same cushioning characteristics, protective capabilities, and cost effectiveness as our other ETHAFOAM products.

For example, the durability and resiliency of ETHAFOAM Anti-Static foams offer "dynamic cushioning" and reusability. They protect from moisture, dust, and are resistant to chemical attack and temperature extremes in many applications.

They're non-corrosive, non-flaking, and attractive. And they're consistent in quality from piece to piece.

They're cost-effective because their use can often reduce packaging material costs, along with labor, shipping, handling, and storage costs. And they often work just as well as other materials, but can cost far less.

A few ways you can take advantage of ETHAFOAM Anti-Static foams.

Cushion packaging applications—ETHAFOAM Anti-Static foams can be used to protect sensitive electronic devices from physical and electro-static damage during shipment. They can be made into corner blocks, braces, saddles, pouches, bags, envelopes, wraps, interleaving and encapsulating products.

Materials handling applications—Here ETHAFOAM Anti-Static foams provide a soft, non-abrasive cushion while protecting parts from static discharge. The foams can be made into trays or tote boxes, or they can be used as a lining inside those products. They can also be made into shunt (stuffing) boards and parts separators.

Work station accessories—In this application, these anti-static foams can be made into table and bench top covers, floor mats, seat cushions, and many other products for clean room environments.

For a free copy of our new, 12-page brochure on ETHAFOAM Anti-Static polyethylene foams, write: ETHAFOAM Anti-Static Foam, DOW CHEMICAL U.S.A., 2020 Dow Center, Midland, MI 48640. Or circle the number shown on your reader service card.

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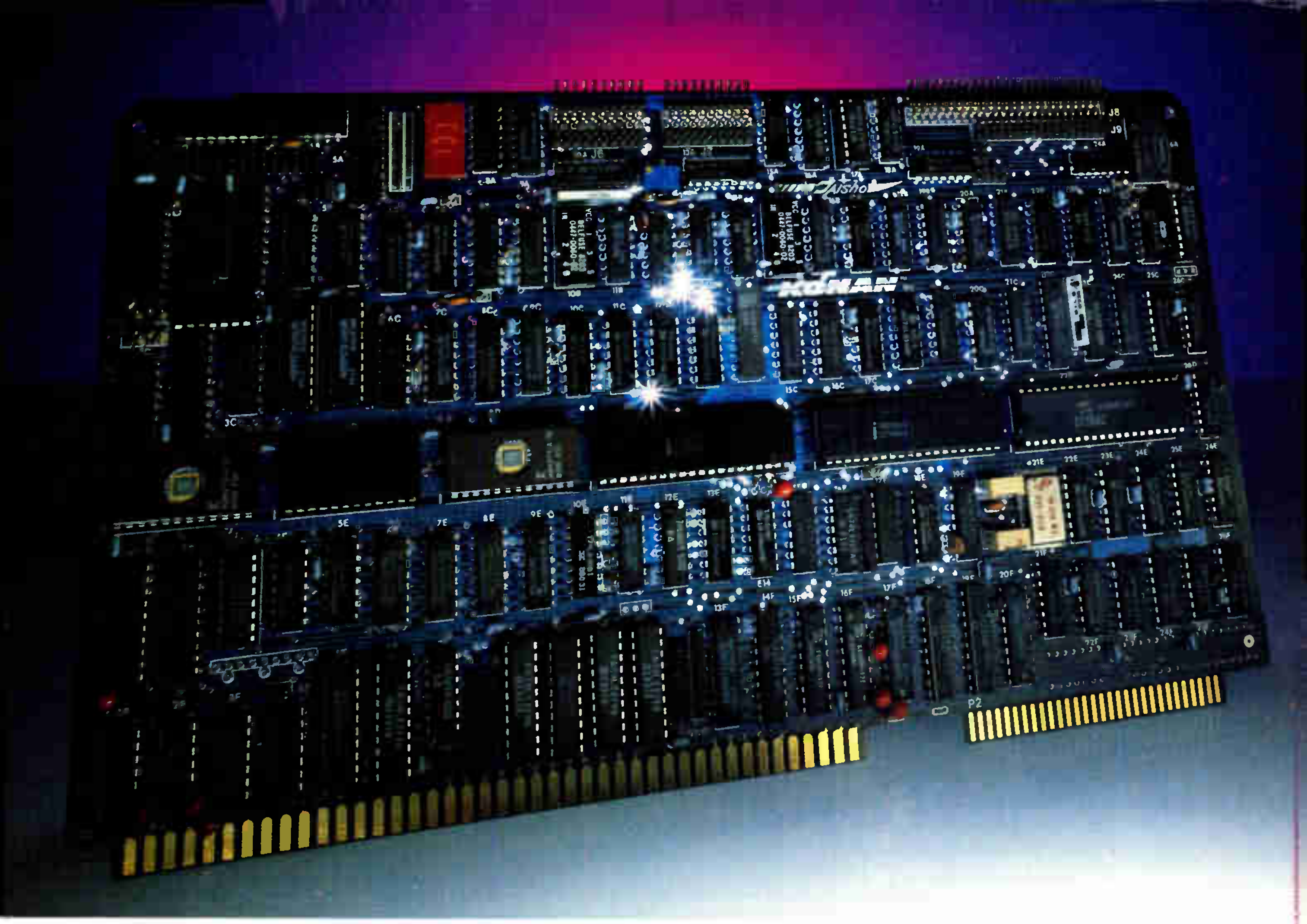

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An elegantly simple interface even allows you to transfer up to 256 sectors with a single command. The command block contains full drive parameters, mode control, host buffer address of the next command, a 16-byte command block which may reside anywhere in host memory and a whole lot more.

Couple design flexibility, quality and an unbeatable price and your choice is simple...TAISHO from Konan.

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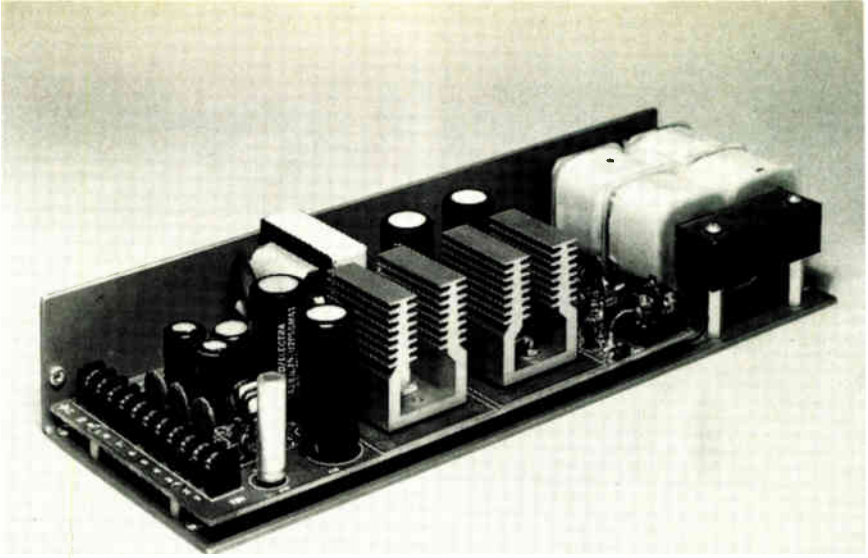
Power supplies

Switcher has reactive input

Unit's high-reactance transformer gives it high power factor, line isolation, and high reliability



A 200-W power supply combines a high-reactance line-frequency isolation transformer similar to those used in ferroresonant supplies with switched-mode technologies. According to OPT Industries Inc., its PX-3551 Reacto-Switcher retains the best features while minimizing the disadvantages of both approaches.

With a high (0.85) power factor, the new supply runs on a significantly lower root-mean-square line current than an equivalent switcher. Inrush current at start-up is limited to 25 A maximum, whether the supply is hot or cold.

The open-frame supply has a lower parts count than conventional switchers, and the company claims that a mean time between failures of better than 150,000 h has been achieved. Efficiency at maximum continuous output power is 75%.

Because the capacitor winding and magnetic shunts are eliminated, the line transformer is smaller and lighter than it would be in a ferroresonant supply of equal capacity. The primary and secondary coils are wound separately and assembled in a side-by-side configuration that achieves high isolation; the Reacto-Switcher easily meets the requirements of Underwriters Laboratories, Verband Deutscher Electrotechniker, and other such bodies.

A single transformer with split primaries set up for connection to 115- or 230-V lines stays within its control range over line variations from 95 V to 130 V and 190 V to 260 V without taps. It also accommodates line frequencies from 42 to 63 Hz.

The transformer's high reactance also reduces electromagnetic-interference problems and the transfer of high-frequency energy between the primary and secondary circuits. The high-frequency switching network is protected from power-line transients.

Ac output. Two features not normally available on switching supplies are the easy availability of isolated ac output for powering such devices as fans and the simple addition of battery backup for configuration as an uninterruptible power supply.

The unit's +5-V dc output, which is rated at 20 A maximum, can be adjusted from 4.8 to 5.5 V and is regulated to ±1% maximum for a change of 40% of rated load. The corresponding regulation figure for the other outputs is 5%; these supply –5 V at 3 A and +12 and –12 V at 4 A each, maximum. Noise and ripple on any output is a maximum of 2% peak to peak or 0.5% rms.

The +5-V line's overvoltage protection activates at 6.25 V ±0.75 V. Hold-up time at maximum output is at least 16 ms.

The 200-W model, the PX3551, measures 2.25 by 4.95 by 14.5 in. and weighs 8.5 lb. Other configurations ranging in capacity from 50 to 500 W are available. Prices are about $1 per watt, and deliveries are in 10 to 12 weeks.

OPT Industries Inc., 300 Red School Lane, Phillipsburg, N. J. 08865. Phone (201) 454-2600 [Circle reader service number 391]

300- and 600-W switchers can be convection-cooled

MOS field-effect-transistor and high-frequency–switching technology keep the SM series of power supplies small enough—just 2¾ by 14½ by 7 in.—to be cooled by convection.

The 300- and 600-W single-output switchers cover the 5- to 15-V range. The 600-W model delivers 2 W/in.³, for very compact packaging. Line regulation is within 5 mV and load regulation is 10 mV for a ±10% change. Output ripple is specified at 100 mV peak to peak. A foldback technique in the units protects against overcurrent, and a resettable crowbar guards against overvoltages. Soft starting limits current inrushes when the supplies are powered up. The SM series is also protected

against excessive temperatures.

The supplies, which are being introduced at Wescon, will be available in January. Prices are still approximate: the 300-W unit will sell for about $425, and the 600-W model for around $675.

Fincor, Incom International Inc., 3750 East Market St., York, Pa. 17402. Phone (717) 757-4641 [Circle 394]

Toroidal transformer fits supply on three Eurocards

Because its transformer's toroidal winding design cuts the DPS 6-L-V power supply's weight and size to roughly half those of equivalent stacked-core supplies, the linear supply resides on only three standard Eurocard-sized boards. Two of the 100-by-160-mm boards, one for rectifiers and the other for regulating circuitry, fit into card-cage slots. The transformer board mounts either inside or outside the card cage.

The DPS 6-V-L accepts 115/230-V, 50-to-60-Hz inputs and provides a regulated output of +5 V at 5 A, ±12 V at 0.3 A, ±15 V or ±18 V at 0.25 A, and ±24 V at 1 A. Thus it can support all the normal peripherals of a microcomputer system. An optional on-board rechargeable nickel-cadmium battery provides complementary-MOS–based systems with up to 60 mA/h of battery backup.

Regulation for the supply is ±0.02% for a ±10% input change. Output ripple reaches a maximum of 2.0 mV peak to peak. In lots of 25, the DPS 6-V-L sells for $209. Delivery takes 30 days.

Dynatem Inc., 22600-D Lambert St., Suite 1007, El Toro, Calif. 92630. Phone (714) 855-3235 [Circle 393]

Battery-backed switcher ensures uninterrupted service

A switching power supply and battery-backup package that slides into a 19-in. rack-mounting cabinet and mates with the backplane connectors produces continuous dc power even if the ac input is degraded or cut off.

The Companion Power System's output ratings are 5 V at 15 A, +15 V at 2.5 A, and −15 V at 2.5 A, for a combined total of 150 W at 50°C. The input requirement is 120 V, 47 to 440 Hz. Other output combinations are available.

Mating the power shelf with additional power systems within the cabinet protects it from power failure. What's more, output isolation diodes mounted on the shelf prevent one system failure from taking down another system. The supply, model 4864-484, is priced at $1,225 in 100-piece quantities. Samples are available from stock.

Lorain Products, 1122 F St., Lorain, Ohio 44052. Phone (216) 288-1122 [Circle 395]

Laboratory power supplies have dual-tracking outputs

A pair of three-output laboratory power sources, the models 4206A and 4218A, are dual-tracking units that combine 0-to-±20-V–tracking outputs, rated at 0.5 A, with single outputs, rated at 0 to +6 V (up to 2.5 A) in the model 4206A and 0 to +18 V (at 1 A) in the model 4218A. Both models offer tracking accuracy to within 1% and a drift no greater than 0.1%.

Fixed current-limiting circuits protect all outputs against overload and short-circuit damage. The ±20-V outputs in both models are limited to 0.55 A and the +18-V output in the 4218A is limited to 1.1 A. Current foldback in the 4206A provides further overload protection for the +6-V output. In addition, it reduces the maximum available current and minimizes semiconductor dissipation during overloads. The power sources are priced at $493 each.

LuTechnology Inc., 3516 Breakwater Ct., Hayward, Calif. 94545. Phone (415) 887-1855 [Circle 396]

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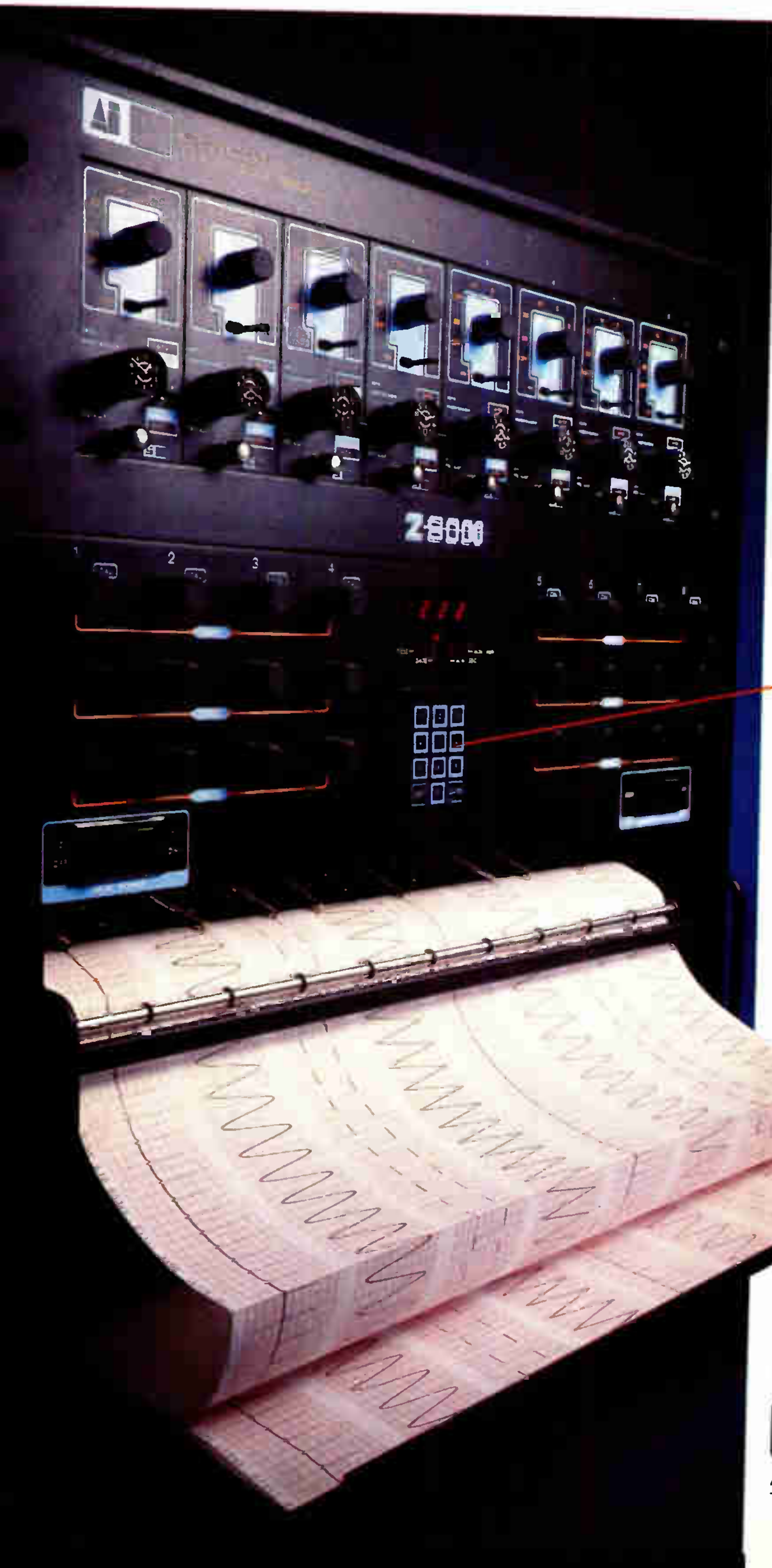

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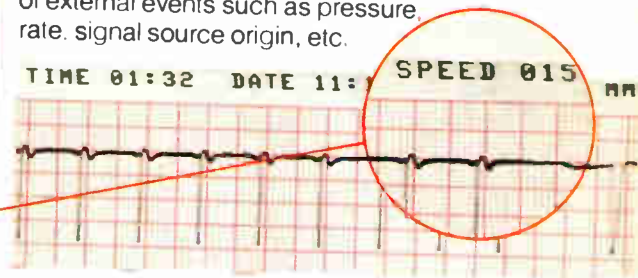

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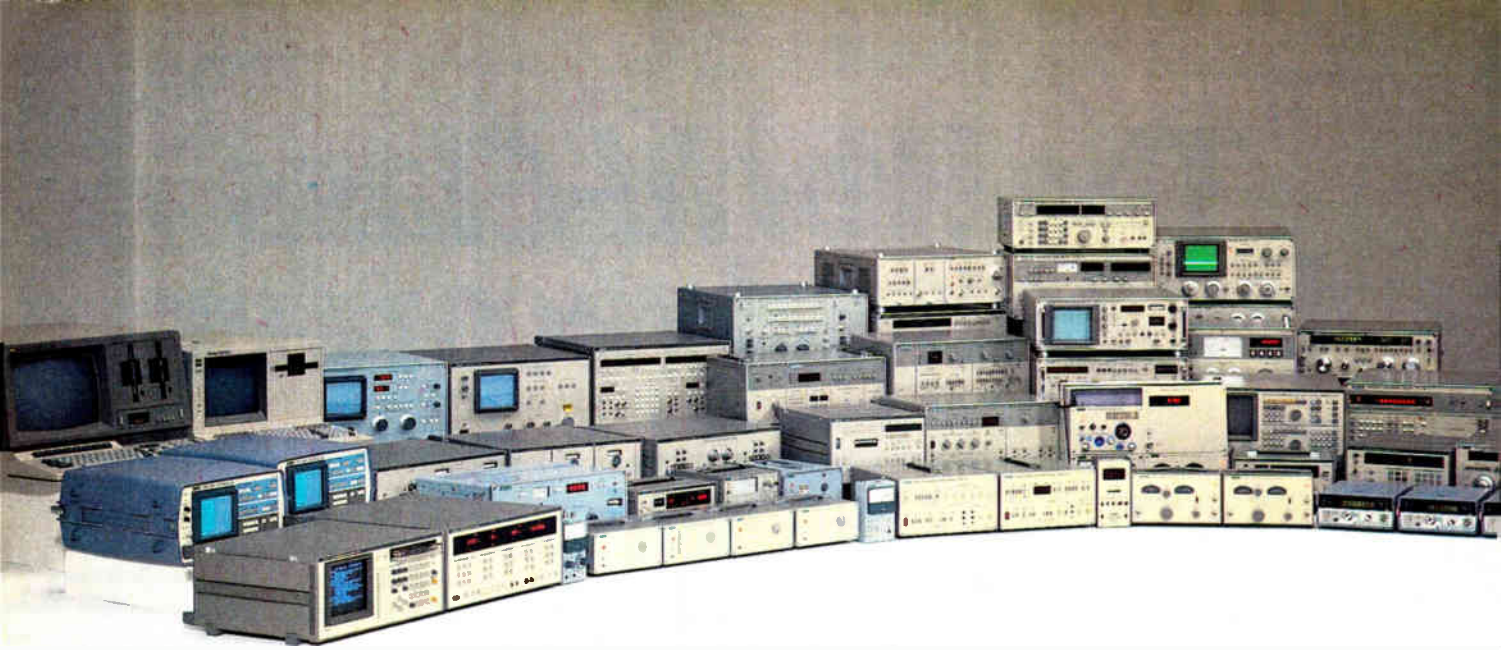

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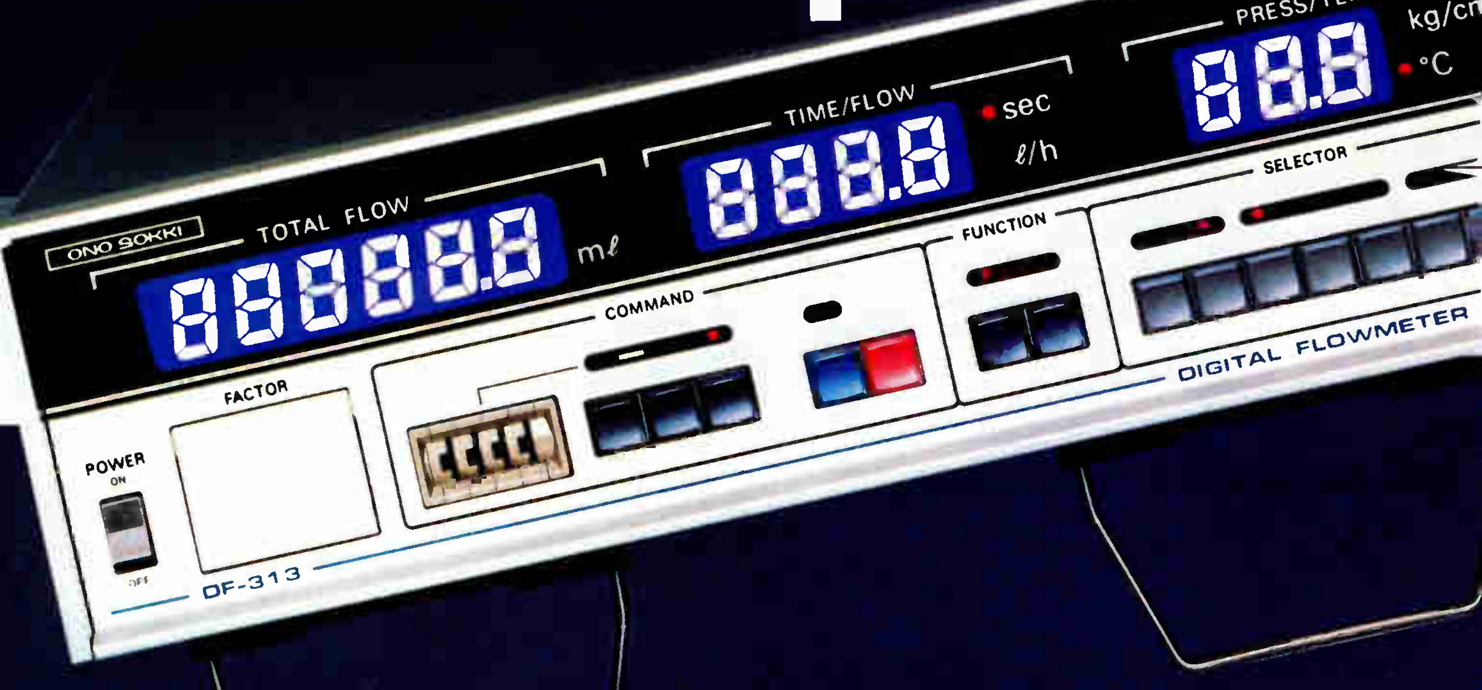
N2305A

Stanley Color LCDs measure up.



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Circle 36 on reader service card

See us at Wescon '83 Booth No. 2525/27.

Products newsletter

E-PROM's chip size and power use drop by 50%

Intel Corp. has introduced a new version of its popular 2764 64-K erasable programmable read-only memory. The 2764A is fabricated on 6-in. wafers with the same process as the Santa Clara, Calif., firm uses for its 256-K E-PROM—the H-MOS II-E process, which reduces the die size from 24,000 mil² to 11,500 mil² and about halves power consumption to a maximum of 60 mA in the standby mode. **Other improvements include a change in the programming voltage to 12.5 V and the use of a fast programming algorithm.** Pricing for the 2764A is the same as for the 2764—$13.40 each for the 180-ns part and $6.70 each for the 450-ns version in lots of 25,000.

Improved algorithms, device ID enhance PROM programmer

Data I/O Corp. has updated its line of programmers of programmable read-only memories with new programming algorithms and electronic device identification, which together quadruple throughput and reduce the chances of misprogrammed or damaged erasable PROMs, the company claims. For a 128-K E-PROM, **the programming algorithm—discounting overhead routines—now takes about 2 minutes compared with the 14 min of a conventional algorithm.** Even with critical overhead routines like blank checks, illegal-bit checks, and exhaustive verification included, throughput still increases fourfold, the company says. Conventional algorithms apply a 50-ms pulse to each memory cell to be programmed; Data I/O's new algorithm typically uses a 1-ms programming pulse followed by a verification pulse. This pattern is repeated only until the bit is programmed.

The electronic device identification equips the memory programmer to read the 16 bytes of information that E-PROM manufacturers store in their parts. With this data, the unit sets up the correct programming algorithm. Pricing depends on the amount of equipment revision needed; customers of Redmond, Wash., firm can have their local service centers make the updates.

Prices for IBM-compatible mainframe computers fall

In keeping with its goal of maintaining at least a 20% edge in price-performance ratio over IBM, National Advanced Systems, of Mountain View, Calif., has reduced prices on certain of its mainframe computers that are compatible with IBM's 4300 line. Prices were cut by about 20% on the AS/6600 series, which competes with IBM's 4341 and 4381—**the AS/6650 drops to $508,000 from $628,000 for an 8-megabyte configuration.** And a 10% to 14% cut was made on the AS/8000 and AS/9000 models—an 8-megabyte AS/8050 drops to $1,650,000 from $1,800,000, a 16-megabyte AS/9060 to $3,150,000 from $3,550,000.

Spreadsheet uses Sequel's data base

Users of Microdata Corp.'s Reality and Sequel business computer systems can add an electronic spreadsheet software system that can access those computers' data bases, as well as permit financial planning. Called Realcalc, the software accommodates basic financial analysis, complex divisional reporting, sales projections, and cash-flow analysis, among others. The Irvine, Calif., company's **software lets the user design his spreadsheet to fit particular numbers.** Individual column widths may be varied at need. Arithmetic, conditional, and relational operators make it possible to form virtually any numerical relationship. Realcalc is available now for $1,595.

Looking for a Distortion Measurement System?

The Amber model 3501 is quite simply the highest performance, most featured, yet lowest cost audio distortion and noise measurement system available.

It offers state-of-the-art performance with THD measurements to below 0.0008% (−102dB), maximum output level to +30dBm and noise measurements to below −120dBm.

It has features like automatic operation, optional balanced input/output and powerful IMD measurement capability. It includes comprehensive noise weighting with four user changeable filters. Unique features like manual spectrum analysis and selectable bandwidth signal-to-noise measurements.

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CF-920 Dual-Channel FFT Analyzer with Floppy Disk and large Internal Memory

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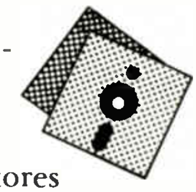

Another memory (semiconductor) continuously stores 32K 12-bit words of real-time data for later spectral analysis. It also stores 30 spectra during real-time analysis or 30 selected spectra from stored time data.

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- Linking (networking) of two CF-920's results in a 4-channel FFT spectrum analyzer.
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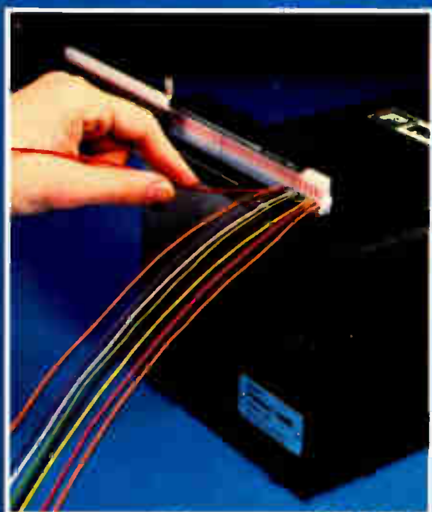

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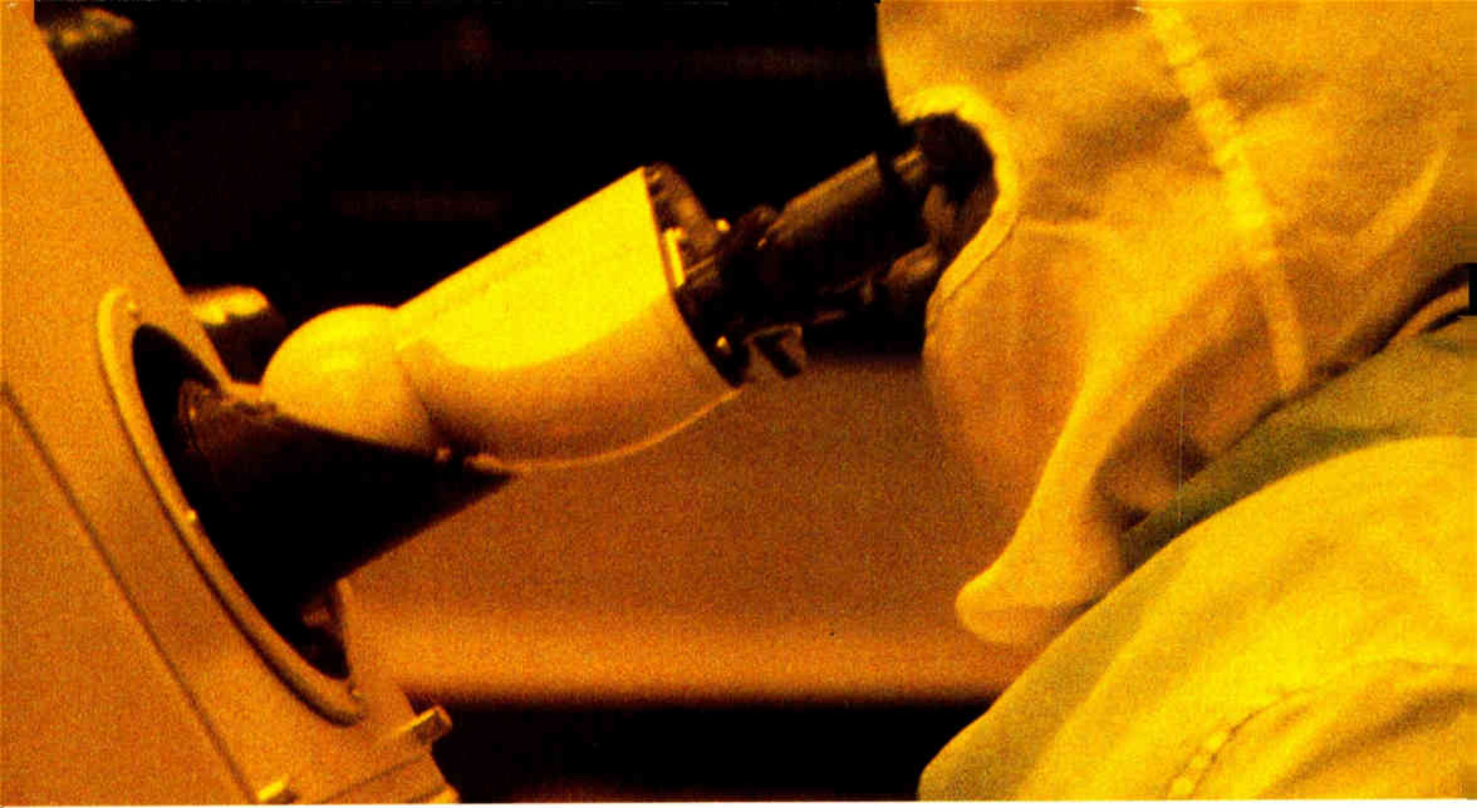

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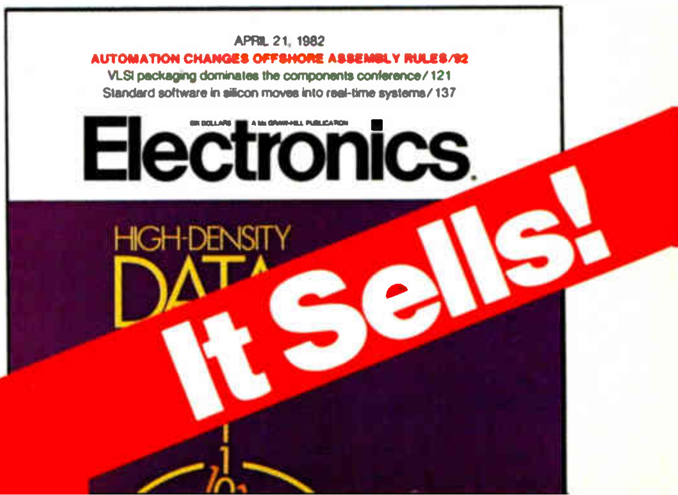

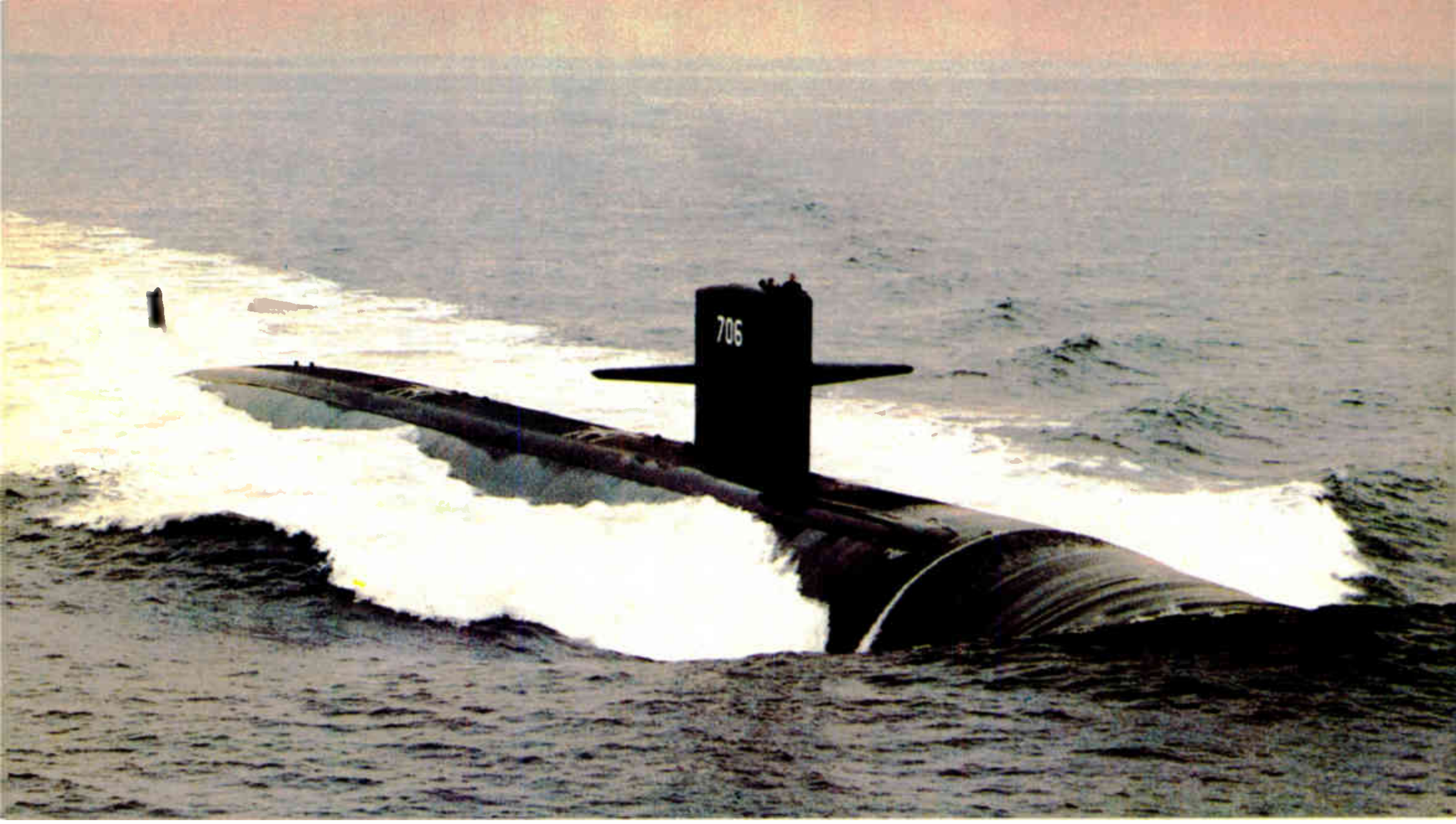

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The Naval Underwater Systems Center is the Navy's principal research, development, test and evaluation center for submarine warfare and submarine weapon systems. We provide high technology vital to the Navy's tactical and strategic edge in combat systems (sonar, combat control, electromagnetics, underwater weapons and targets, weapon launch and handling), surface ship sonar and undersea ranges.

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Career outlook

Recruitment heats up

In yet another sign that business for electronics and other high-technology industries is turning up, a leading indicator of demand for engineering personnel has turned bullish. The High Technology Recruitment Index, which is based on the volume of recruitment advertising for engineers and scientists in newspapers and technical journals, has moved above the norm (1961) for the first time in 14 months. Deutsch, Shea & Evans Inc., which compiles the index, is a New York City recruitment advertising agency.

When the index for July reached 104—its highest one-month level since May 1982 and the third consecutive month in which the index has risen—the agency declared that "the long-awaited turnaround in demand for engineers and scientists appears to be occurring." What's more, says the firm, August's reading was also 104, so further gains may lie ahead. The three-month running average for May through July—101—is also the third such increase in a row and the highest index level since May through July 1982.

Analog shortage. Engineers of all stripes can take cautious comfort from the shape of the future, it seems. Christian & Timbers Inc., the Cleveland high-tech search firm—headhunter, in plain English—has detected a new trend in the demand for semiconductor specialists.

The firm says the communications industry's growth has triggered a "significant increase" in overall demand for analog integrated-circuit engineers. Two things contribute to the shortage, says Christian & Timbers. First, "the great majority of EE graduates of the major universities in the last 10 years have been involved in predominantly digital technology." Second, the communications industry, growing for the last few years at a compounded annual rate of more than 30%, is based on analog disciplines.

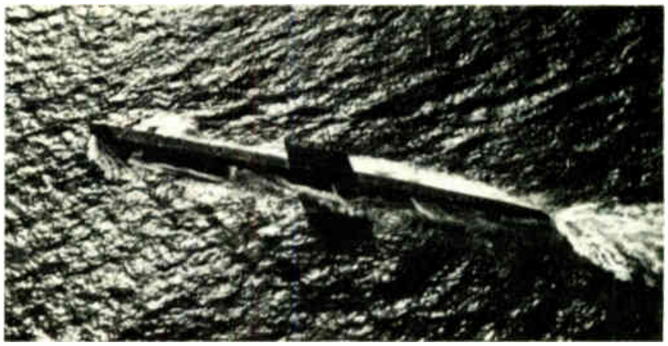
The Cleveland firm points in particular to the short supply of analog engineers with a background in MOS. It claims that throughout North America, fewer than 100 competent IC design engineers are now working in analog MOS. In fact, such a rare bird would command an annual salary of $40,000 to $60,000, plus bonus and stock options. That's 40% higher than the levels prevailing three years ago.

Working EEs. Optimism about demand and shortages seems also to be reflected in the attitudes of working EEs. The New York–based American Association of Engineering Societies is an umbrella organization that includes among its members the Institute of Electrical and Electronics Engineers. It reports that a survey of engineers in all disciplines shows that even though the proportion that expects demand to grow in 1983 has dropped sharply from last year, engineers working in aerospace, electronic equipment, and computers are optimistic about the chances for growth in their industries. Employers, says the AAES, indicate that 1983's net hiring will be slightly above 1982's. Demand is expected to be strongest for EEs.

In yet another survey, the AAES has taken a look at enrollment in U. S. engineering schools. The study, which was undertaken by the society's Engineering Manpower Commission during the 1982–83 academic year, shows that the number of engineering students increased from the previous 12 months.

Involved in the survey were 286 engineering schools, with 403,390 undergraduate students in all engineering disciplines—some 4.1% more than the year before. Although freshman enrollment, at 115,303, hardly changed, the number of graduate students rose by 5.5%. And the number of freshman women was up by 5%, with 9% of them studying civil engineering, 15% chemical engineering, 11% mechanical engineering, and 16% electrical engineering.

The 23,607 foreign students, whose presence has been noted with increasing frequency of late—by members of Congress, among others—made up 5.9% of all engineering students and 35% of graduate engineering students, down somewhat from 37.7% in 1981. □

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Through 1983, Computer Systems and the Defense Systems Division have added substantially to their base of new business. At DSD our products are a sophisticated line of "ruggedized" medium and large scale high reliability computers for use in airborne, land-based and shipboard applications. These high speed computers and related peripheral equipment must perform under extreme environmental conditions and employ the latest in gate array technologies.

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- Logic Design: electrical engineers with 2-8 years experience in microprocessor design, bit-slice design, gate array design and microsequencer design
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- Reliability Engineers: engineers to evaluate the reliability of electronic system designs and develop improved techniques to insure good field performance of equipment/systems
- Maintainability Engineers: electrical engineers to develop features and characteristics for equipment/systems which will contribute to ease-of-maintenance, cost-effectiveness, and efficient man/machine interface

We pride ourselves on the high energy yet informal working environment here. And we invite qualified candidates to join us in some of the most exciting projects our company has ever undertaken. You can take the first step by submitting a resume to Professional Staffing, Sperry Corporation, Computer Systems, Defense Systems Division, ES, U1E20, P.O. Box 43525, St. Paul, MN 55164-0525. An Equal Opportunity Employer. U.S. Citizenship Required.

SPERRY

POSITIONS VACANT

Murkett Associates — Technical Mgmt placement with national affiliates-fee paid. Box 527, Montgomery, AL 36101.

Switched Network Engineer needed for telecommunications common carrier based in Anchorage, Alaska. Must have experience in traffic engineering and switched network management. Responsible for switched database management and overall network design and performance. Send resume in confidence to General Communication Inc., 2550 Denali St. Suite 505 Anchorage, AK 99503. Charlie Carpenter (907) 338-6888 or (206) 621-7655.

Voice/Data Private Line Engineer needed for telecommunications common carrier based in Anchorage, Alaska. Must have experience in private line circuit design with an emphasis on data circuit design. Responsible for all private circuit design and development and distribution of circuit layout record to installation forces. Also responsible for equipment evaluation and ordering as required for various network applications. Send resume in confidence to General Communication, Inc. 2550 Denali St. Suite 505 Anchorage, AK 99503. Attn: Charlie Carpenter (907) 338-6888 or (206) 621-7655.

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Gulf South Opportunities! Numerous openings in the Gulf Coast area for electronic engineers in the medical, computer and defense industries. All fees paid. For consideration send resume or call collect to Ann Jernigan, Snelling and Snelling, 428 Plaza Bldg., Pensacola FL 32505. (904) 434-1311.

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Responsibilities will include the development, design and implementation of firmware for micro-processor-based products, and the optimization of firmware development for real-time run requirements. Assignments will include development of digital signal processing algorithms involving signal filtering, modulation/demodulation and effective implementation of hardware/firmware requirements. BS/MS EE and a minimum of 8 years' experience in real-time software/firmware design and implementation are required. Assembly language programming experience with a variety of microprocessor knowledge is highly desirable.

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Your responsibilities will include providing design support for development of microprocessor-based data communication products. Digital signal processing, analog filters, and standard digital design experience required, in addition to adherence to strict quality, reliability and performance requirements. A BS/MS EE with 5 or more years experience in microprocessor-based design and digital signal processing experience are required. Data communications product design and active filter (Analog) design highly desirable.

Hayes offers experienced professionals a stimulating work environment that encourages personal and professional advancement, and a comprehensive benefits package that includes profit sharing. Qualified candidates should send a confidential resume or apply in person at:

HAYES MICROCOMPUTER PRODUCTS, INC., Department EL-HR14, 5923 Peachtree Industrial Blvd., Peachtree Crossing Office Park, Norcross, Georgia 30092. An Equal Opportunity Employer, M/F. Principals only need apply.

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Applicants with engineering degrees are employed at the GS-5 entry level (GS-7 with superior academic achievement). Experienced engineers, or those with advanced degrees, may qualify for entry at the GS-9 or GS-11 level. The salary for these positions ranges from $20,256 to $31,861 depending on experience.

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Electronic manufacturer in Fairfield County Ct. seeking a good circuit designer with management experience. Candidate should:

- **Be capable of discreet design and knowledgeable of state of the art microprocessor design.**
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- **Have five to ten years experience and process EE, MEB.**
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If you have the desire to become part of a dynamic, fast growing company please send resume along with salary history to:

Personnel Manager
P.O. Box 1439, Bridgeport, CT 06601

Engineers—EE/CS/ME/IE for Aerospace, Defense & Commercial electronics companies on a nationwide basis. All fees are employer paid. For details call or send resume to **Edie Sayer** at **Richard Gast & Associates, 2433 N. Mayfair Rd., Suite 208, Milwaukee, WI 53226 (414) 258-2029.**

FACULTY POSITIONS VACANT

Electrical/Electronics Engineer For Junior College Faculty — The Academy of Aeronautics, a junior technical college in Aeronautical and Electronics Technology at La Guardia Airport, New York is seeking an Engineering teacher for the Electronics faculty. Qualifications: A Masters degree in Electrical or Electronics Engineering with some teaching or industrial experience. Applied engineering or technology experience is preferred to theoretical research. A Bachelors degree may be accepted based upon early matriculation for the Masters, with institutional financial support. Financial support will be provided for graduate study through the doctoral degree. The College is accredited by Middle States Association, and the New York Board of Regents, with major curricula accredited by ABET. The Federal Aviation Administration approves curricula which lead to Federal certification. This is a tenure track position with full paid benefits including hospitalization, retirement, disability and education. The position is available immediately. Forward resumes, including references and salary history to: Dr. George W. Brush, Vice President, Academy of Aeronautics, La Guardia Airport, Flushing, New York 11371.

SPECIAL SERVICES

Microprocessor Consultant, Hardware and Software. Real time control, data acquisition, digital signal processing, automotive, telecommunications, consumer products. Contact Allen Newcomb, Cygnus Microprocessor Technology, 4033 Oak, Kansas City, MO 64111, 816-531-2252.

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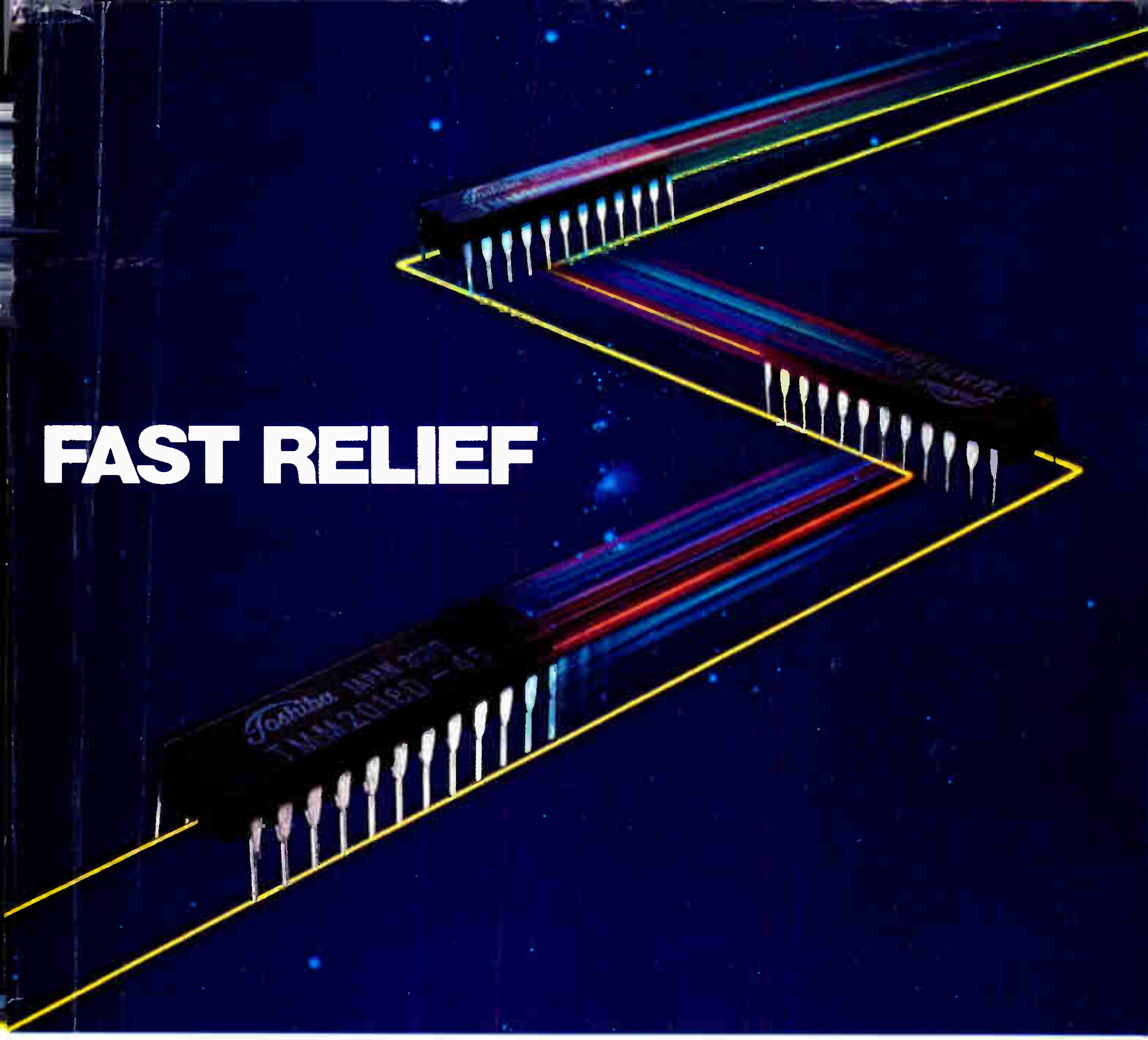

The Toshiba 16K Bit High Speed Static RAM: The Fastest 2K Words X 8 Bit Static RAM in the World

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Toshiba 16K Bit High Speed Static RAM

Model	Access Time (Max.)	Operating Current (Max.)
TMM2018D-45	45ns	150mA
TMM2018D-55	55ns	150mA

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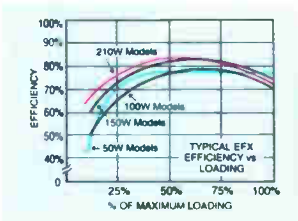
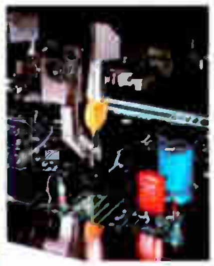
Circle 901 on reader service card

How to tell cheap from low-priced when considering open frame switching power supplies.

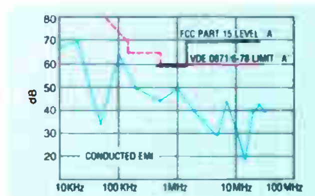
With power on, touch the transformers. If they're hot, they're cheap. *Kepco/TDK transformers are barely warm.* That's because the cores are made of TDK H7C1 ferrite, the finest going, and have been designed for particularly good low-loss characteristics at 40 KHz. Less heat generated by transformers means more compact spacing of components and longer life. (See the efficiency curves.)




Automatic component insertion

Compare the mounting of components on *our* board with any other. The difference tells you a lot. The firm, solid, uniform mounting of our components adds to reliability and long life (our MTBF is over 60,000 hours). And it's a major reason why our open frame switchers are low-priced, not cheap: all components are mounted by a TDK-designed machine, in about five minutes. The money saved in both labor and freedom from rejects is what enables us to use such high-grade components. Machine production also means we're able to supply any number you need.

See whether it has an on-board filter. If it doesn't you'll have to add one that meets FCC and VDE requirements. Our conducted noise is not only well under both (see graph), but the on-board filters use special TDK-made VDE-approved capacitors.



Do you get both 115 *and* 230 V a-c (selectable) inputs at no extra cost? You do with ours. So you can use our switchers for both U.S. & export sales.

Look at the temperature rating of the capacitors: cheap ones are rated at 85°C. Good ones at 95°C. *Ours are 105°C.*

The Kepco/TDK open-frame switchers aren't cheap, they're low-priced.
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