JUNE 30, 1982

ROM MAKERS DOUBLE DENSITY WITH FOUR-STATE CELLS / 81

Microprocessor software opens the X.25 network to OEMs / 109

5-volt-only EE-PROM banishes external components / 127

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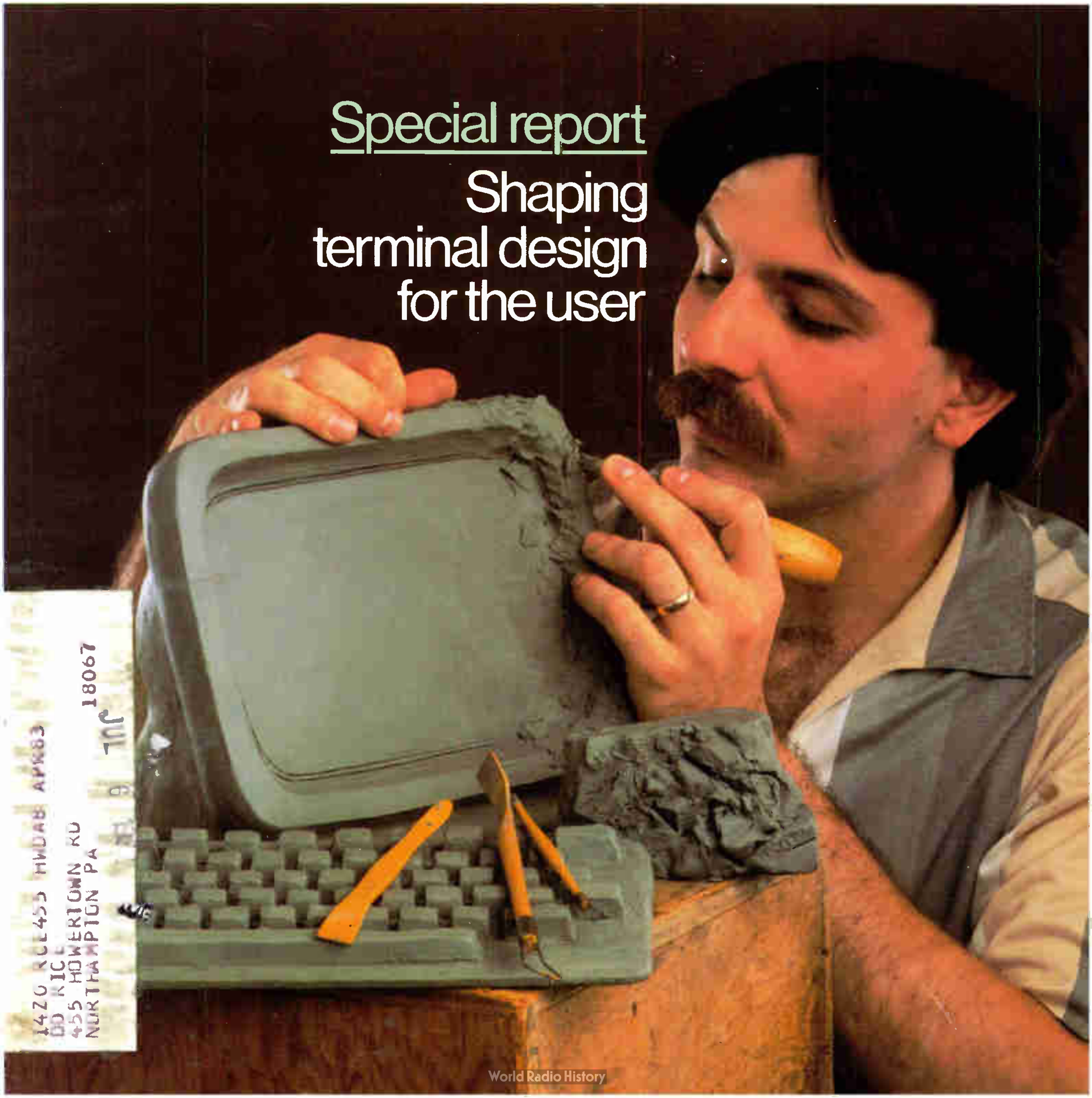
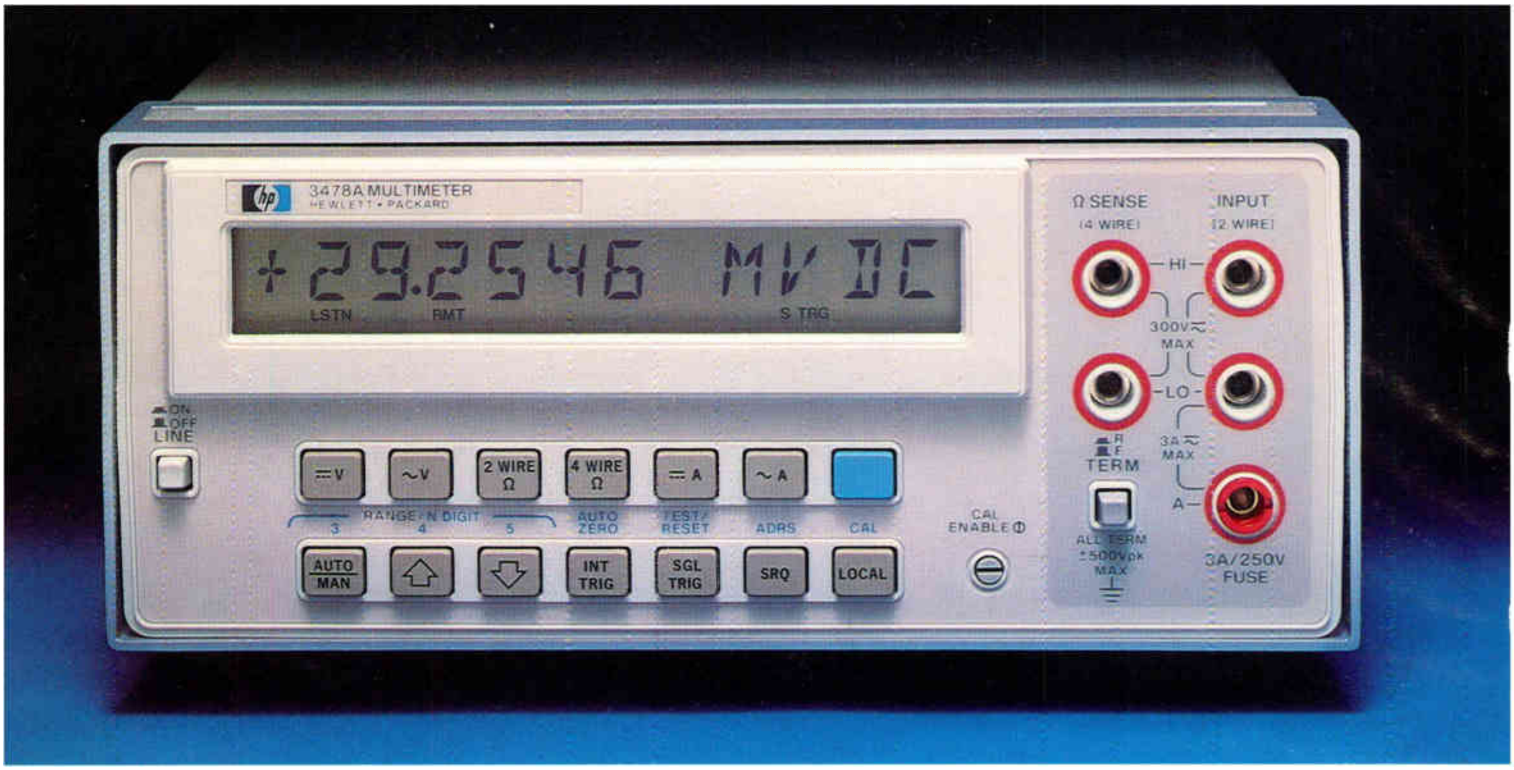
Electronics





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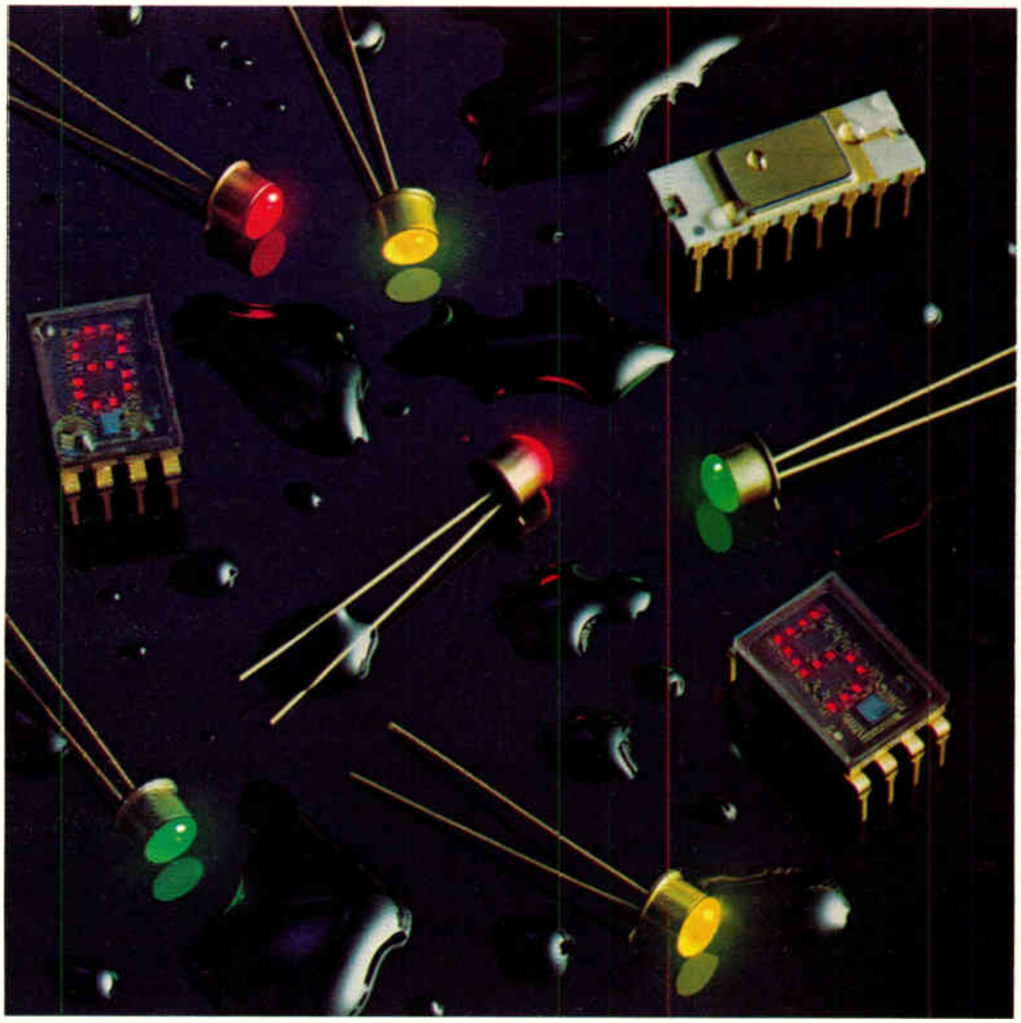

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Electronics

The International Magazine of Electronic Technology and Business

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The Cover Story

Major New Developments

NEWSLETTERS

DEPARTMENTS

SERVICES

Vol. 55, No. 13 • June 30, 1982

Highlights

Cover: Computer terminals adjust to the human interface, 97

Poorly designed computer terminals can cause back- and eye-strain and lower the productivity of their full-time operators—critical matters when many industries are starting to computerize. This special report surveys how this consideration is melding with advances in semiconductor and other technologies to produce a new generation of ergonomically designed terminals in the U. S. and abroad.

Motorola hones four-state memory cell, 81

With an eye on the density bonus, Motorola is developing a 256-K read-only memory that holds 2 bits per cell. This latest version of a four-state cell boast' a novel geometric programming technique.

Z80 parts plus software equals X.25 link, 109

General-purpose Z80 microprocessor hardware can make up the interface between data-processing equipment and an X.25 packet-switching network. The key is the software, and in this case, its modular design partitions the linking functions to speed up execution while assigning host-dependent routines to a single, easily rewritable module to enhance portability.

Data bases enhance multiuser microprocessor systems, 113

Multiuser microprocessor-based systems now can handle mainframe tasks, and a data-base processor will help them to realize this capability. This microprocessor-based peripheral controls a disk resource, which may be shared among a number of different hosts, and provides comprehensive data-base and file management.

Multiuser development system speeds up with coprocessing, 122

With input/output functions relegated to their own processor, a microprocessor development system can tackle the demands of a multiuser environment without bogging down.

5-volt-only EE-PROM subs effortlessly for static RAM, 127

Easy incorporation into microprocessor-based systems is the achievement of a new 5-volt electrically erasable programmable read-only memory. It integrates support hardware and timing circuitry that give it compatibility with standard 24-pin random-access memories.

In the next issue . . .

An elastomeric substrate for denser chip mounting . . . enhanced TTL in the 3081 mainframe . . . a graphics terminal that uses two processors to achieve high performance.

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Publisher's letter

Computer terminals, it seems possible, one day could outnumber pencils and pads of paper in white-collar workplaces around the world. So it's not surprising that computer makers have begun in earnest to study how they can better match their terminals—their human-interface hardware, that is—to the total environment that conditions computer users.

Tom Manuel, our computers and peripherals editor, spotted the emerging trend last year. "In 1981," Tom says, "interest in ergonomics started to perk up at computer and computer-peripheral companies, as they realized that standards for terminals were being forged in Europe while none existed in the U. S." So this spring he made the rounds of the heavy players in the terminal game in the U. S. to see what they were doing about ergonomics, and we sent our overseas correspondents to update what was going on all over West Europe and in Japan.

This extensive reporting was sifted and then put together by Tom for the special report on terminals that starts on page 97. "For starters, we sorted out the current regulations and legislation involving terminals," he says. "Then we took a look at the technology that's enabling computer makers to match their equipment to its human users."

As for standards, the Europeans—particularly the West Germans—have done the most so far, Tom feels. Moreover, terminal makers will benefit from the ongoing effort of the European Economic Community [Common Market] to standardize keyboards so that a single key layout will handle the character sets needed for all the European languages. The Japanese have the problem partly solved, with a standard for the kana phonetic symbols, and they hope to arrive at a common layout for the keystrokes that make up the kanji. However, so far in the U. S., keyboard standards are at best companywide.

Fresh from working on his special report, Tom has a vivid image of what the workhorse office terminal of the late 1990s will look like: "It will surely be a flat screen, probably A-4 size, integral with the desktop. But," he warns, "don't expect to see cathode-ray tubes eclipsed for at least 10 years." Along with the screen, "there'll be an unobtrusive keyboard and a microphone for voice input.'

Though nonvolatile semiconductor memories have been commercially available for a decade or so, the early versions were no joy to work with—multiple power supplies, high voltages, and slow writing discouraged potential users. The push to create a simpler part is yielding noteworthy results, particularly the 16-K electrically erasable programmable read-only memory that Xicor Inc. describes on page 127.

Solid state editor Rod Beresford first heard about the company's new chip back in January. "At the time," he recalls, "we had just published our annual markets forecast, in which we were projecting that consumption of EE-PROMs would nearly quadruple by 1985, to over $330 million. Many of those parts will be going into microprocessor-based systems, where 5-volt power supplies and TTL signal levels are the only way of life."

Xicor's X2816A gets high marks for ease of use. In fact, it's not only microprocessor-compatible, it's a truly self-supporting EE-PROM that's as simple to use as a static random-access memory. Beyond those features, though, our editor was struck by the research at Xicor on the electron tunneling that provides the storage mechanism in EE-PROMs. "I studied tunneling in school," notes Rod, "and can appreciate what the Xicor researchers were up against in trying to get a better fit between theory and experiments. I think they succeed admirably."

Readers' comments

Unix redux

To the Editor: R. Colin Johnson's March 24 special report titled "Operating systems hold a full house of features for 16-bit microprocessors" [p. 113] contains some inaccuracies.

For example, the article states that the Unix fork operation is useful because "if the program goes haywire, a copy of the complete environment has been kept so that no effort will have to be wasted in rewriting destroyed programs." However, the runtime environment of a process is a binary core image, where the programs that one writes and rewrites are files of characters. Having a copy of the runtime environment of a process would hardly help recreate a destroyed source file, even assuming that a program which had gone sufficiently haywire to defeat the protection mechanisms of the file system would be polite enough to destroy its own source file and not somebody else's.

More accurately, the fork is the operation through which a process creates a child process. An editor can use a fork to create a second incarnation of itself, letting the user look at a second file without losing his or her place in the first. The advantage of copying the code, registers, and open files is that the child has access to all the information the parent has accumulated; the disadvantage is that the system insists on copying everything even when the child plans to overlay itself immediately with a different program and so does not need the information.

The article also states that the Unix programmer can use pipes to join program fragments to run sequentially with little performance penalty. In fact, the performance penalty is low precisely because the program fragments run concurrently, not sequentially. The pipe is a real queue, albeit limited in performance because it is implemented on disk rather than in main memory. Yet, so long as it does not fill or empty completely, the process filling the pipe and the one emptying it will run in parallel.

Along the same lines, Table 3 accompanying the article states that pipes are limited to character input/output. This is either too generous or not generous enough. All Unix I/O—to files as well as to pipes—is performed in terms of bytes, and it is up to the programmer to group the bytes into integers, floating-point numbers, or other types of data structures.

Finally, the statement that Unix presents all users with the same command language is misleading. Though the delivered version of the system provides only one kind of user interface, any user can create script files that define new commands out of combinations of the standard ones and it is possible to specify that another command-processing program be invoked in place of the standard command shell for any particular user. In "The Unix Time-Sharing System" (Bell System Technical Journal, July-August 1978), Ritchie and Thompson mention a specialized shell for word processing that automatically invokes the editor when a user logs in and a shell that lets an unsophisticated user play games but prevents him or her from accessing system commands in general.

Steven J. Correll
Livermore, Calif.

■ **The author replies:** *Mr. Correll's comment on the Unix fork operation is somewhat out of context, as the text refers to the automatic invocation of a fork whenever a program is executed. During the program development phase, the advantages and disadvantages enumerated do hold true. As for joining program fragments by means of pipes, the statement is not concerned with whether the fragments are run concurrently or sequentially. Rather, the intent was to illustrate that a program can be coded and debugged as a collection of independent processes and then run with the processes in their original sequence with no penalty in performance. Regarding the reference to pipes in the table, the terms character and byte can be used interchangeably. As for the final comment on the command languages for Unix, though custom shells can indeed be written, they are not part of the standard version of the operating system.*

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COHERENT provides a friendly and flexible environment for program development. To achieve this, the system provides a large number of powerful, general purpose tools for constructing and maintaining programs, as well as for solving application problems. From this substantial base of software, the end-user can easily tailor **COHERENT** to solve particular application problems.

COHERENT and all of its associated software are written in the high-level programming language **C**. This has yielded a high degree of reliability, portability, and ease of modification with no noticeable performance penalty. In fact, use of **C** has allowed more effort to be spent on the choice of proper algorithms, resulting in a system that uses the machine's resources efficiently.

Features

COHERENT is compatible with UNIX both at the **C** source level and at the user command (shell) level. This makes the large base of software written for UNIX available to the **COHERENT** user.

The major features of **COHERENT** include:

- multiuser and multi-tasking facilities,
- running processes in foreground and background,
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- the shell command interpreter—modifiable for particular applications,
- tree-structured, hierarchical file system,
- pipes, asynchronous software interrupts, and memory sharing for interprocess communication,
- generalized internal segmentation model allowing flexibilities such as memory sharing,
- ability to lock processes in memory for real-time applications,
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- minimal interrupt lockout time for real-time applications,
- power failure recovery facilities,
- fast disc accesses through disc buffer cache,
- device drivers, the swapper, and some other system facilities are loadable, considerably simplifying configuration and driver development,
- process timing, profiling and debugging trace features.

*UNIX is a trademark of Bell Labs.

Software Tools

In addition to its facilities for basic file and process manipulation, **COHERENT** provides well over 100 utility programs and an extensive subroutine library The following major software components are included: **SHELL,** the command interpreter; **STDIO,** the standard C I/O library; **MATH,** library of mathematics routines; **AS,** an assembler for the host machine; **CROSS,** a number of cross-assemblers and cross-compilers for other machines are available with compatible object formats; **DB,** powerful symbolic run-time and postmortem debugger for **C** and assembler; **ED,** a context-oriented text editor with regular expression patterns; **NROFF,** text formatting, spelling checking and other utilities related to word processing; **SORT,** sort program with generalized key and record specification; **SED,** a stream editor (used in filters) fashioned after **ED; GREP,** efficient file search for a pattern; **DIFF,** give minimal differences between 2 or 3 textual files; **AWK,** a pattern scanning and processing language; **M4,** macro-processing language; **LEX,** generates lexical analyzer programs; **YACC,** advanced language to generate parsing program from a grammar; **MAKE,** aids in construction and maintenance of a program or software package; **SCCS,** maintain several versions of source code and documentation for a large software project; **LEARN,** computer-aided instruction about **COHERENT; BC,** arbitrary precision desk calculator language; **QUOTA,** various programs to account for system resource usage; **MAIL,** an electronic personal message facility; and **DUMP,** incremental file backup system.

Of course, **COHERENT** will have an ever-expanding number of programming and language tools and basic commands in future releases.

Language Support

The realm of language support is one of the major strengths of **COHERENT.** The following language processors are supported:

- **C** — a portable compiler for the language **C**, including stricter type enforcement in the manner of **LINT.**
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- **XYBASIC™** — a state of the art Basic compiler with the interactive features of an interpreter.

The unified design philosophy underlying the implementation of these languages has contributed significantly to the ease of their portability. In particular, the existence of a generalized code generator is such that with a minimal effort (about one man-month) all of the above language processors can be made to run on a new machine. The net result is that the compilers running under **COHERENT** produce extremely byte-efficient code very closely rivaling that produced by an *experienced* assembler programmer. Finally, the unified coder and conformable calling sequences permit the intermixture of these languages in a single program.

Operating System

Because of the language portability discussed above, and the substantial effort in achieving a greater degree of machine-independence in the design and implementation of the **COHERENT** operating system, only a very small effort is required to transport the whole system to a new machine. This means that an investment in **COHERENT** software is not tied to a single processor. Applications can move with the entire system to a new processor with about two man months of effort.

COHERENT is available for all Digital Equipment Corporation PDP-11 computers with memory management, such as the PDP-11/23, PDP-11/34, PDP-11/44, and PDP-11/70. The system is implemented for the Intel 8086/8087/8088, the Zilog Z8002, and the Motorola 68000 processors. Future plans call for **COHERENT** implementations for many other machines, including the DEC VAX-11 family and IBM 370-compatible computers.

Because **COHERENT** has been developed independently, the pricing and licensing is exceptionally attractive. Of course, **COHERENT** is completely supported by its developer. To get more information about **COHERENT,** contact us today.

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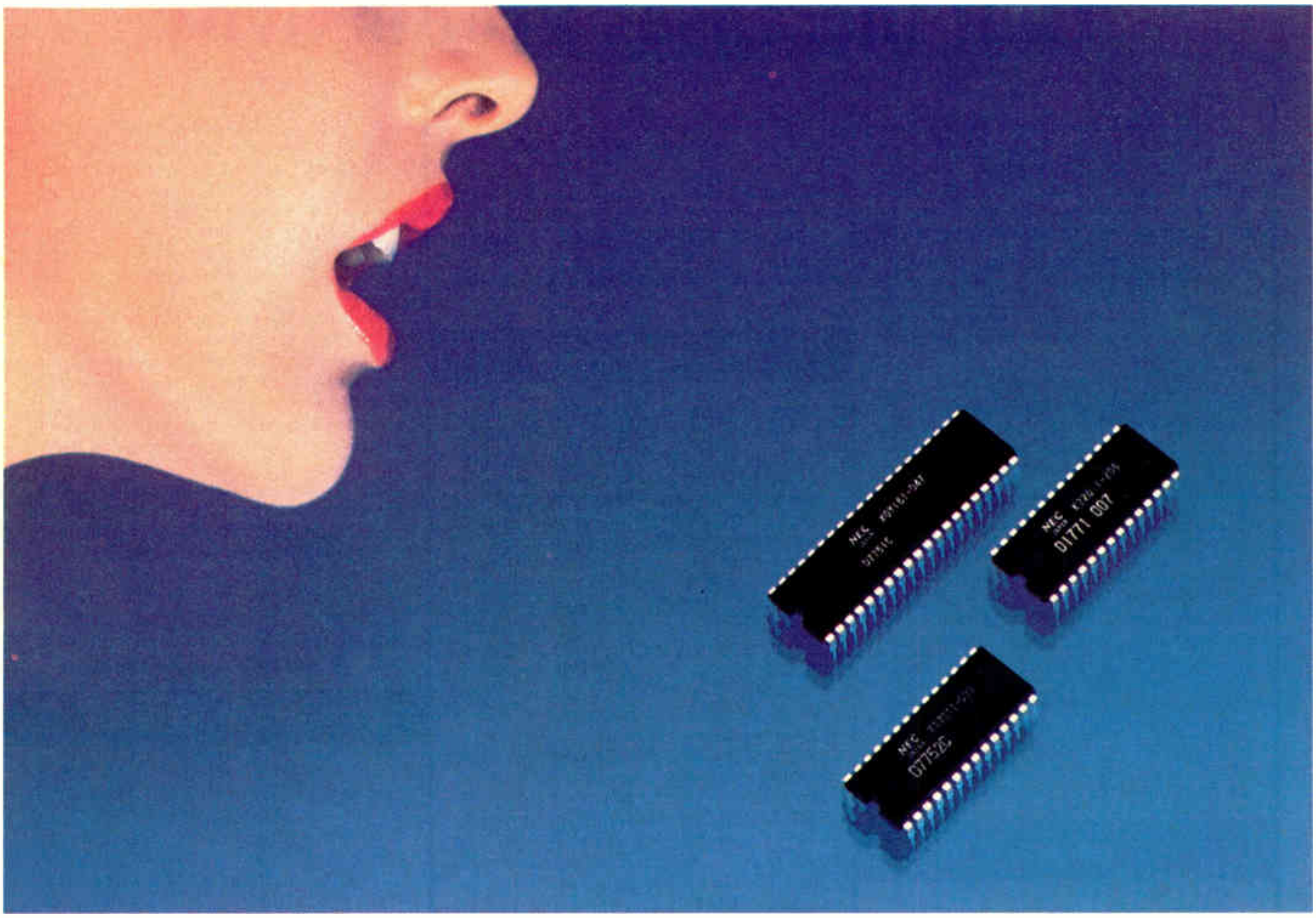


THREE LSIs COVER MOST SPEECH SYNTHESIZING APPLICATIONS

NEC has introduced three new speech synthesizing LSIs: the adaptive differential PCM type μPD7751C, the formant parameter type μPD7752C, and the phoneme type μPD1770 Series.

The μPD7751C encodes speech-waveforms just as they are. So music can be mixed, and the reproduction sounds very natural. The μPD7751C can store eight kinds of messages which can be reproduced selectively by key switches. It is suited for alarms and NC machines.

The μPD7752C uses sympathetic parameters (formants) from the vocal tract, a system that ensures a high compression ratio. It offers three speaking speeds and can be applied to home electronic products, automobiles, language labs, and industrial equipment.

The μPD1770 Series reproduces a wide range of sounds from natural to mechanical by combining segmentations extracted from the original waveform. This low-cost series (including an evaluation chip) incorporates a 9-bit D/A converter for direct drive of a speaker, and is intended for small amusement machines.

Through close interaction with its C&C (computer and communications) technology, NEC offers what may be the most extensive semiconductor lineup in the industry.

NUMBER 124

ANZCAN CABLE NORFOLK ISLAND– NEW ZEALAND LINK

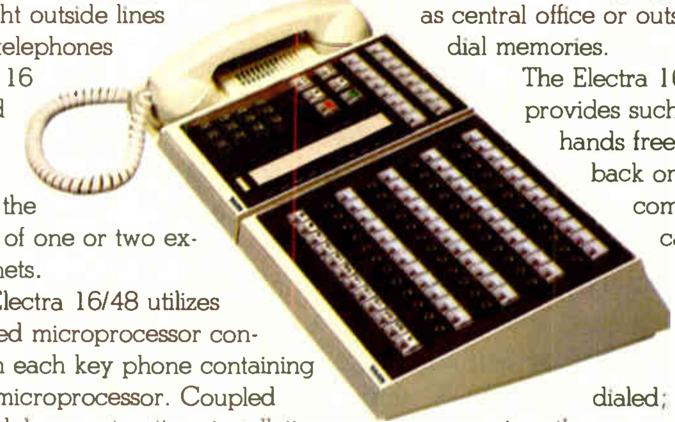
Communications from Australia and New Zealand to countries in Europe and North America are rapidly increasing in volume. Because the existing submarine cable lacks the capacity to handle the increased traffic, Australia, New Zealand, Canada, Fiji, and ten other countries have decided to install a new submarine cable to be called ANZCAN.

NEC, in cooperation with two other Japanese companies, is to design and manufacture all the necessary equipment and cables for installation of the 1,360 kilometer link between Norfolk Island and Auckland. This link will consist of 5MHz equipment using submarine coaxial cables and will accommodate 480 telephone channels. The contract for its construction was awarded by the Overseas Telecommunications Commission (Australia), the New Zealand Post Office, Teleglobe Canada and Fiji International Telecommunications Ltd.

When the ANZCAN system is completed in 1984, it will cover a total distance of 15,000km.

NEW ELECTRA 16/48 ALLOWS SYSTEM GROWTH

Growing companies often outgrow their key telephone systems. To solve this problem, NEC has introduced the Electra 16/48, which allows system growth from eight outside lines and 16 telephones to up to 16 lines and 48 telephones through the addition of one or two extra cabinets.



The Electra 16/48 utilizes distributed microprocessor control, with each key phone containing its own microprocessor. Coupled with modular construction, installation is accomplished with ease, as is the addition and relocation of phones with the use of two-pair cables.

Among the many time-saving features incorporated within the Electra 16/48 system is the two-digit LED display that indicates which station is calling, a message to Call Back, and confirmation of Call Forwarding destination, in addition to its many other capabilities. The Electra 16/48 has 20 function buttons on each key set, some of which are programmable for intercom as station DSS (Direct Station Selection) memories. Function buttons may also be programmed as central office or outside speed-dial memories.

The Electra 16/48 also provides such features as hands free answer-back on the intercom; automatic callback to busy stations; automatic last number dialed; conferencing; three-zone paging; two Direct Station Selection/Busy Lamp Field consoles; and up to four stand-alone Busy Lamp Field consoles.

TWO FIRSTS IN SOLID-STATE RADIO TRANSMITTERS

Completely solid-state transmitters for 10kW AM and 5kW FM broadcasting are now available from NEC.

The MBT-8040A 10kW MW transmitter uses NEC-developed MOS FETs in the final power amplifier stage. It has an overall efficiency as high as 73%, and is extremely compact and quiet in operation.

The FBN-9050S 5kW VHF FM transmitter employs wide-band (87.5—108MHz) 800W PA units with over 60% efficiency, and a high-performance exciter with synthesized PLL circuits.

These transmitters have higher reliability and stability, and lower power consumption, than their tubed counterparts. They are also practically maintenance-free.

The excitement builds in data communications . . .

If this is not the best of times for the data-communications professional, it certainly ranks right up there. Just consider the ferment and turmoil that have been building in the field in the past few years—indeed, in the past fortnight.

The big event, of course, is the anointing of Baby Bell, American Telephone & Telegraph Co.'s unregulated subsidiary, hereafter to be known officially as American Bell Inc. As the story on page 88 points out, the new company, with headquarters in Parsippany, N. J., will provide a service that heretofore could be accomplished only with expensive custom hardware and software interfaces: communication among many types of data terminals and computers. And though the initial offering, as well as capitalization, is not exactly mind-boggling (see below), make no mistake about it: the face of U. S. data communications has been permanently changed.

In the same two-week period, the National Science Foundation released a report that more or less confirms for the general public what the industry has been saying for a long time—that is, that life on this planet in the future will be quite different from what we know now because of the data-communications revolution. The document discusses interactive television services, business conferences via video, and myriad other services that will be available, for better or for worse, during the coming decades.

All this, of course, is just the start. There is virtually no limit to the breadth and width of the technological horizon—the advances up to now have hardly begun to stretch it. Whether the concern is video reception or intercomputer communication, the effect on society and the economy will be profound.

. . . amid some questions about the new baby

When the new unregulated data-communications subsidiary of AT&T, christened American Bell Inc. but fated to be known forever as Baby Bell, takes its first steps next month, not many people will be impressed. That may be precisely the way the parent wants it—to keep anyone from perceiving the offspring as a genie escaped full-grown from a bottle. The initial data-processing services will not match those already available through such competitors as GTE's Telenet and Tymshare, and American Bell's initial bankroll of $56 million is even less impressive. Even with the scheduled increase in capitalization to $511 million by the end of 1985, officials at the Federal Communications Commission point out, liquidation of the new subsidiary would not cost AT&T as much as 50¢ a share.

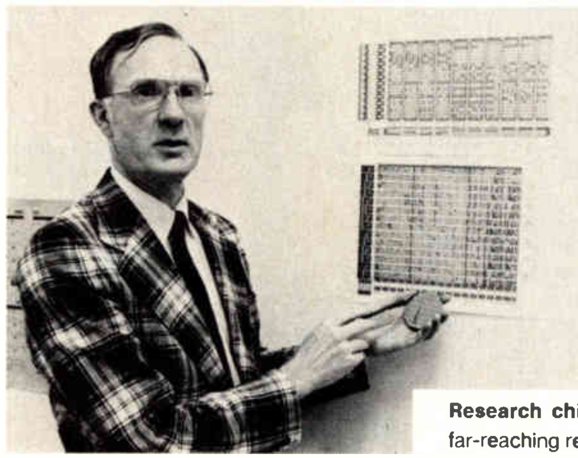
But shed no tears for AT&T. Unable to own or operate transmission equipment, American Bell will have to buy switching services under an FCC tariff—which, conveniently, should add to AT&T revenue when charges for the Bell packet-switching service are approved.

There is, however, a rather serious question facing the FCC, which must monitor the subsidiary to preclude its subsidization by its parent. Skeptics, among them AT&T's competitors, doubt that the FCC is up to the job. The competitors want American Bell to be forced to obtain some outside financing, thereby requiring separate financial reports that would act as a check on it. AT&T, of course, argues that the separation is adequate as is. How this issue is resolved may be academic: now that the baby is up and walking, nothing will alter its power to effect radical changes in data delivery in the U. S.

People

Penfield of MIT aims VLSI work beyond 1985

Paul Penfield Jr. has his gaze trained on distant horizons as he directs the Massachusetts Institute of Technology's ambitious research program in very large-scale integrated circuits. "We want to look beyond the immediate needs of industry, at issues we expect will be important in five years or so," says Penfield, professor of electrical engineering.



Research chief. Paul Penfield heads MIT's far-reaching research program in VLSI.

Penfield, 49, holds a bachelor of arts degree in physics from Amherst College and a doctor of science degree from Cambridge-based MIT. A member of MIT's faculty since 1960, he joined GenRad Inc.'s board of directors last fall. He also serves as a consultant to Digital Equipment Corp. in Maynard, Mass., and MIT's Lincoln Laboratory in nearby Lexington.

His approach to VLSI research aims to break up anticipated logjams in IC design and fabrication. For example, "we will support research focusing on the interface between design and processing; right now, it is a fairly rigid boundary set by the process people." Identifying the ways IC designers can contribute to and vary the fabrication process, he believes, will increase the freedom and flexibility of the design stage, spurring innovation.

Penfield also anticipates what he believes will be the next major hurdle for VLSI evolution. "Currently the dominant limitation to the complexity achievable in VLSI is the design task; we're looking forward to the time when the design crisis is solved and there will be a new limit: the systems limit." VLSI researchers would grapple with "questions that have to do with the architecture of groups of chips rather than the architecture within a single chip."

Another concern of the VLSI program, Penfield says, will be research into novel devices and into systems involving unusual processing steps. He points to a current project that requires an extra processing step still beyond industry's capabilities. "We have a design for a prototype device, an artificial retina, whose signal-processing circuitry must function consistently whether the device is operating in light or dark." The solution is to fabricate an opaque device layer that shields signal-processing elements but contains pinholes that permit enough light to activate the chip's photocells.

Such unusual problems—and solutions—will characterize the chips built at MIT, Penfield says. "We'll be doing some of the things industry can't or won't do today."

CDC's deal with Centronics a 25-year milestone for Kamp

How do you celebrate 25 years in the computer peripherals business? In the case of Thomas G. Kamp, president of Control Data Corp.'s $1.3 billion Peripheral Products Co., the occasion will coincide this summer with CDC's acquisition of a major stake in Centronics Data Computer Corp., the Hudson, N. H., printer manufacturer.

The 57-year-old Kamp was a major architect of the deal (effective June 24), which includes the infu-

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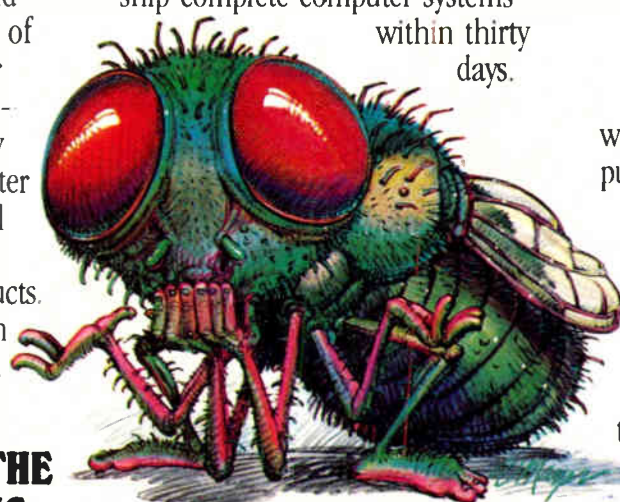

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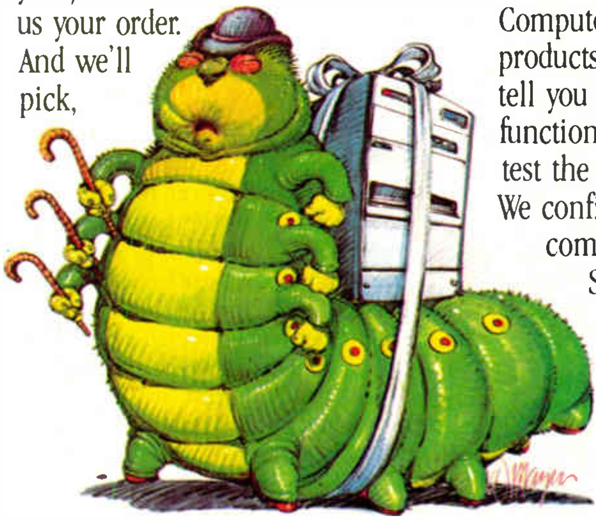

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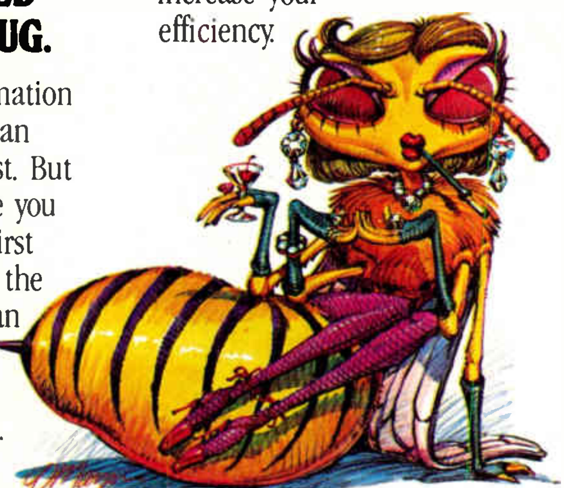

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People

Marriage broker. Thomas Kamp engineered Control Data's takeover of Centronics.

sion of $25 million from Minneapolis-based CDC and the transfer to Centronics of the printer business of Computer Peripherals Inc.—a 50% CDC-owned joint venture with NCR Corp. and International Computers Ltd. The net result will be a 35% CDC ownership in Centronics. And as new Centronics board chairman, Kamp will also control the proxies of NCR and ICL, each of which will hold about 5% of Centronics as a result of the deal.

From CDC's viewpoint, the beautiful part of the deal—which Kamp calls a "reverse merger"—is that it allows effective CDC control of Centronics at a much lower price than it would cost to buy the firm outright. In addition, Kamp points out, CDC funds that would otherwise have been required for its CPI printer business can be channeled elsewhere, since Centronics now has a healthy balance sheet against which it can raise money on its own.

For Kamp, a Detroit native who holds a bachelor's degree in electrical engineering earned in 1949 from the University of Minnesota, the Centronics chairmanship is just one more line item on his résumé. He holds a similar title with CPI as well as Magnetic Peripherals Inc. and Peripheral Components Inc., two other CDC joint ventures. Indeed, his silver anniversary with CDC will occur is August. □

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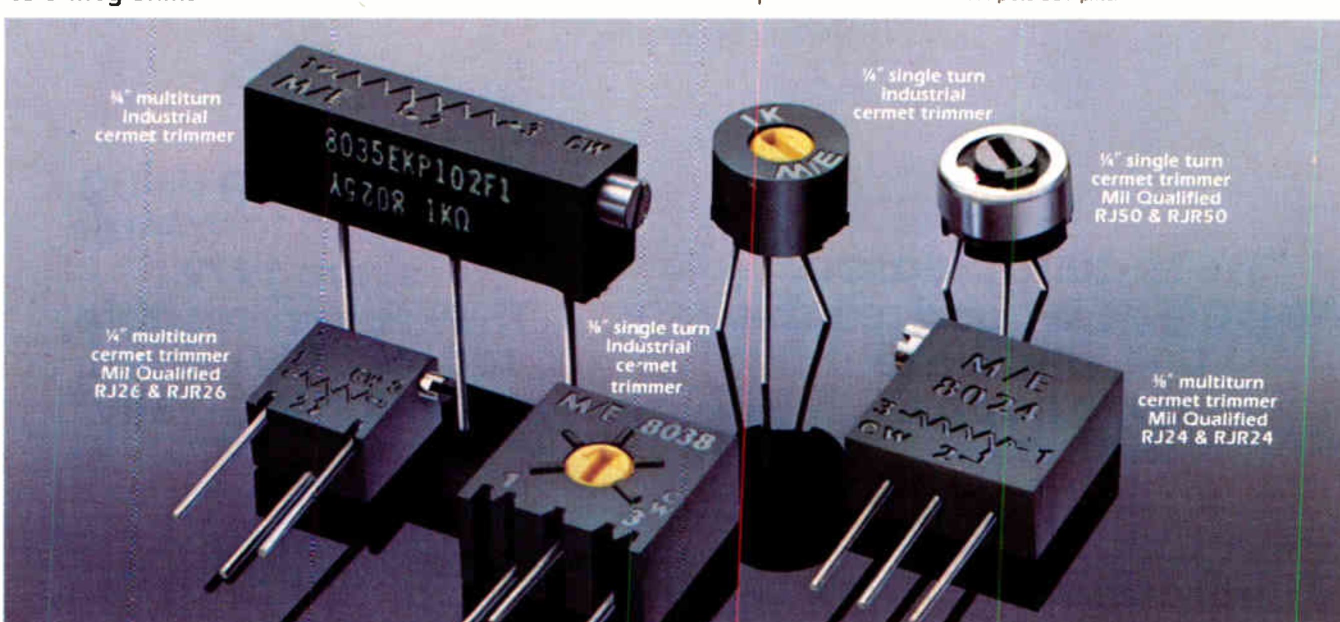

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Circle 17 on reader service card

If you don't feel this good about your terminal supplier, call TeleVideo.

"They set the standard for the industry in service and quality."

"A very honest company to deal with... I can't think of a negative thing to say."

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Millennium Systems Inc.

"We're quite pleased. We wanted a good reliable unit, and we're quite happy."

Tom Peters, Engineer
Gould Inc.

"We've been using TeleVideo terminals since 1979. They're very reliable, reasonably priced, and high in quality."

Hollis Arban, President
Nabra Enterprises

"TeleVideo is very responsive to our customizing needs. They're high quality, reliable units."

John Spaulding, Project Manager
Gould Inc.

We don't satisfy our OEM customers by making the best promises. Instead, we make the best terminals for the money, and deliver them the way they want them—when they want them. A concept so simple, you'd think everyone would have caught on.

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It doesn't amaze us, however. Once we found a way to beat the leaders on price and quality, finding customers was easy.

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Price/Performance: Nothing outperforms our terminals on the job, and no one beats our price for value. Our rigid testing and use of high quality components have made our record of customer service and satisfaction the best in the industry.

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We scooped the industry in 1980 with the first low-cost LSI Winchester disk controller, a five-chip set that provided the basis for our first board-level disk controller, the WD1000. Now, tens of thousands of controllers later, we're introducing the WD1001, the next generation board-level controller. Smaller size. A significant price reduction. New LSI innovations. And the added dependability of ECC.

Right around the bend is the WD1002, which will tap our expertise in floppy disk controllers to provide both floppy and Winchester control on one board. Then look forward to the WD1003 and WD1004 to extend the leading edge in file management, and put more profit in the picture for you.

The story doesn't end there, though. For you do-it-yourselfers, we'll cheerfully sell you all our proprietary LSI, and include microcode, PCB artwork and engineering assistance. Or, if you prefer, we'll gladly customize our board to your bus, with or without DMA, and to your form factor. And deliver working prototypes inside of 60 days.

Heart, courage, brains—and more than a touch of wizardry all play a part in the commitment this announcement represents. Now we'd like to sit down with you to provide the facts, features and technical details you need. Call our controller hotline, (714) 966-7827 and we're on our way. Or write directly to Luke Dru, VP Components Marketing and we'll contact you.

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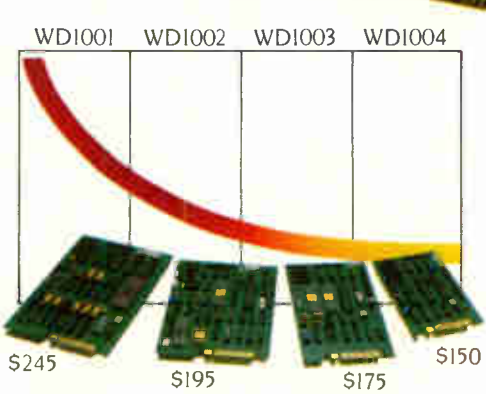

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The data

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Whether it's word processing or business systems or dataset and multiplexer.

Whether it's telephone switching or transmission or microwave.

Cannon® connectors help pass the word and carry the load farther.

Goodbye to EMI. So long to ESD.

ITT Cannon is running interference for you with the only connectors on the market offering proven noise-free performance.

Our D Subminiature filter connectors and RFI/EMI D Sub backshells are built to give you and your customers years of silent service.

And because we hate electrostatic discharge as much as you do, we've developed the shrouded D Subminiature connector. It not only solves your ESD problems, but your EMI problems as well.

20780 easy as 1,2,3.

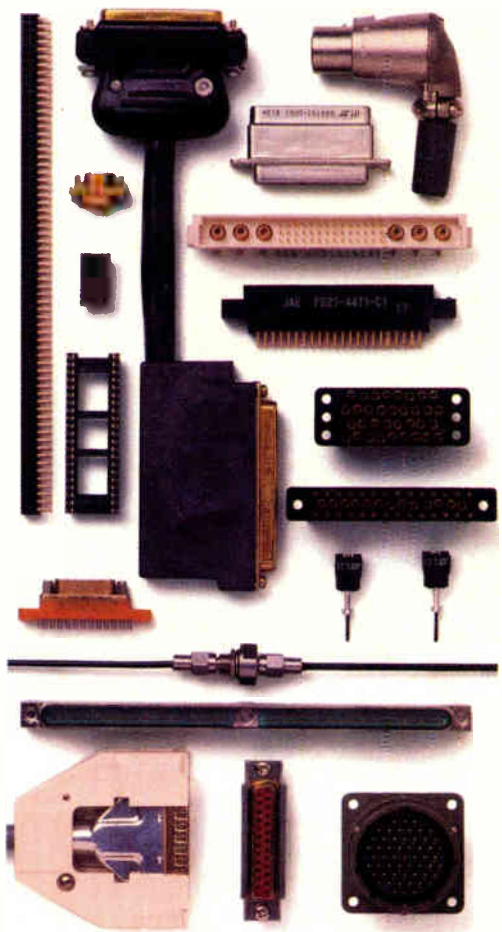
Meeting the strict FCC regulations, like Docket 20780, is simple with Cannon's shielded shrouded backshells. Or our new lower-cost transverse filter designs, available in virtually all types of Cannon connectors. Both designs will keep unwanted transmissions from tampering with your system, at a significantly lower installed cost.

Problems are no problem.

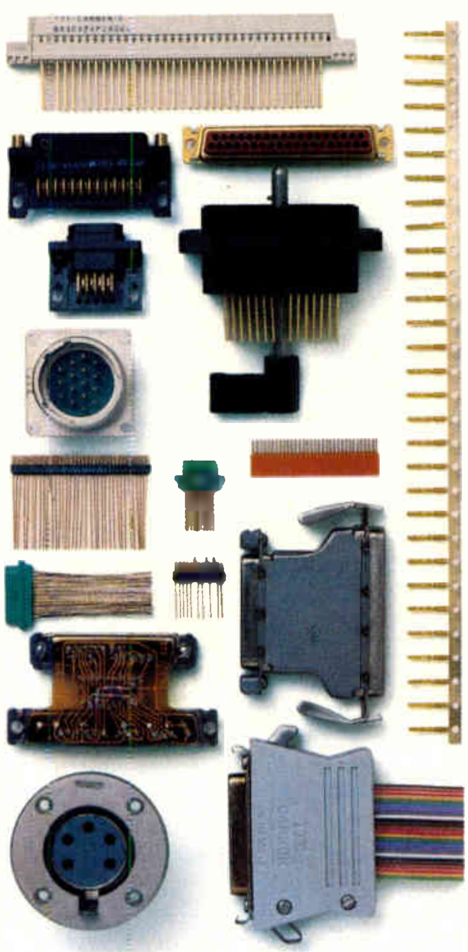
ITT Cannon has already solved many of the connector problems you run up against every day in the development of sophisticated information systems.

Take a look at these:

Our PB18 zero-force edgecard connector not only increases the length of the board, but the life as well.



connection.



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Our P/C connectors are qualified to DIN 41612 (G06) and reverse DIN (G60).

Our microminiature line will let you lower installed costs without giving up a micron of quality.

And our new low-cost, low-profile IC socket (DICF) has two points of contact and no solder wicking. It also offers higher electrical reliability.

But maybe your needs call for fiber optics. Cannon's optical-fiber connectors are lightweight, small in size, provide economy and reliability, and are immune to RFI/EMI interference.

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Free connector guide.

To find out more about our complete line of connectors for information systems, send for our free Information Systems Connector Selector Guide. Contact ITT Cannon, a Division of International Telephone and Telegraph Corporation, 10550 Talbert Avenue, Fountain Valley, CA 92708. Telephone: (714) 964-7400. In Europe, contact ITT Cannon, Avenue Louise 250, B-1050 Brussels, Belgium. Telephone: 02/640.36.00.

CANNON ITT
The Global Connection

New court created to strengthen patents

by **Marc E. Brown,** *patent attorney practicing in Los Angeles*

Where would real-estate development be today if the average cost of ejecting a trespasser were in excess of $20,000? And what if the ejection effort had less than a 50% chance of success after spending all that money? Obviously, things would be a lot different. Yet those are the very statistics that any investor in research and development has had to face if he chose to protect his investment by a U. S. patent.

A major reason patent enforcement has been statistically so expensive is that the success of such actions often cannot be accurately predicted. Without predictability, the incentive to resolve conflicts without litigation is diminished, especially when the purported infringement is on a large enough scale to make the financial gamble of patent litigation worthwhile.

Lack of predictability is caused in part by the frequent assignment of patent trials to judges who are unfamiliar with the intricacies of patent law. In a recent survey, it was estimated that only 1 out of approximately 800 cases heard by a Federal judge is likely to be a patent case. In addition, most of these judges have no understanding of the technology involved and are not provided with ready access to any source of unbiased technical advice.

Although trial court decisions are subject to review by an appellate court, appellate judges also rarely understand patent law or technology. As a result, their decisions often conflict with one another, making it necessary to spend more money doing research to uncover the court in which the case is most likely to be favorably treated. Often, this court will be far from the litigant's home, making the cost of the litigation even higher. And while the U. S. Supreme Court is technically empowered to resolve these uncertainties and inconsistencies, it has historically been too busy to address them adequately. Consequently, patent litigation today is expensive and risky.

New court. Congress has been attempting to solve this problem for the past seven years. On April 2, 1982, President Reagan formally signed into law the result of its efforts—an act creating a new court called the U. S. Court of Appeals for the Federal Circuit.

All appeals in patent cases will be assigned to the new court. Its staff of judges will include many who have substantial experience in patent litigation and are already highly respected in the patent profession. The bill also gives the court the authority to appoint unbiased advisers.

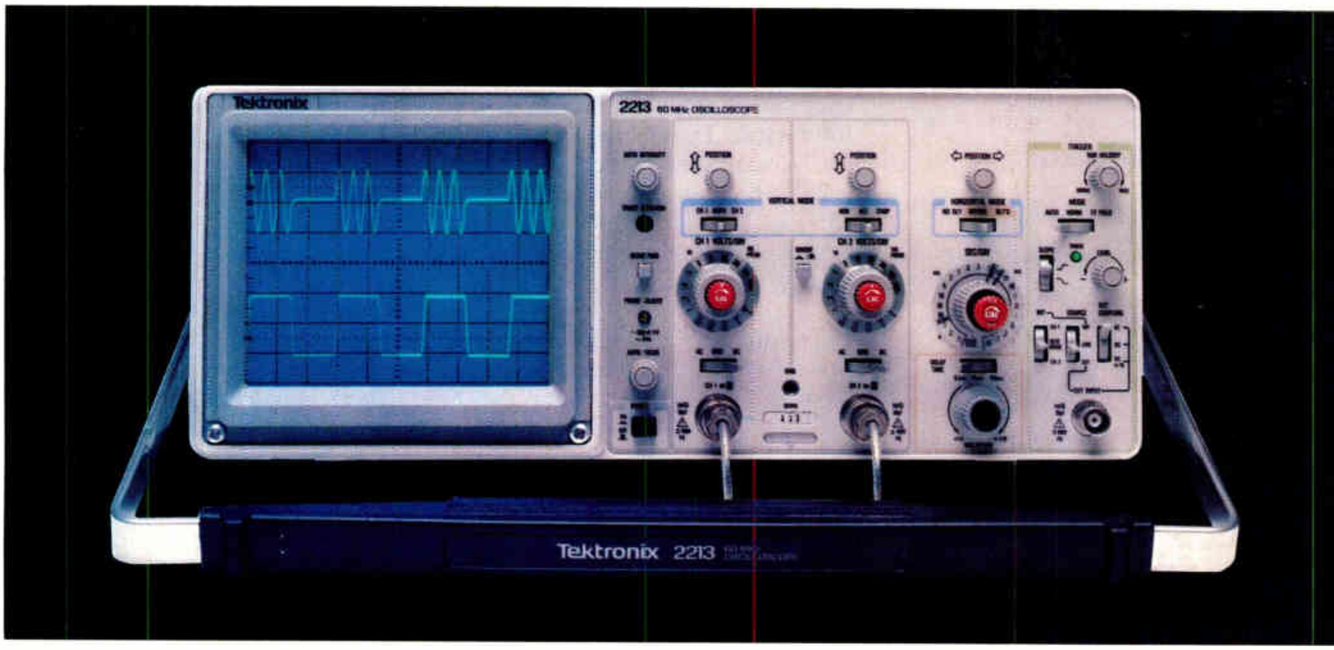
The new court is expected to substantially diminish the uncertainties that exist in patent litigation and the lack of uniformity in judicial application of patent law. It is hoped that this will decrease both the need to engage in forum shopping and the tendency to appeal decisions as a matter of course. With increased predictability, litigation itself is less likely to occur. The ultimate goal is more meaningful protection for inventors.

Opposition. Not everyone, however, is in favor of the new court. The Commission on Revision of the Federal Court Appellate System, for example, strongly recommended against such a unified court. It was feared that judges might develop tunnel vision from hearing large quantities of patent cases. It was also suggested that the incentive to render carefully reasoned decisions might be reduced, since there would no longer be decisions from other appellate courts to consider. Concern was also voiced over the possibility that judicial vacancies in this highly specialized court would be the subject of excessive and unhealthy pressure from special interest groups.

It is clear that the present system is not working. In a 1978 survey of more than 125 major industrial corporations, it was reported that over 84% agreed with the statement that "enforceability of a patent in court is so complex, lengthy, expensive, and uncertain that the full value of the patent incentive is being eroded."

Whether for better or worse, the new court is scheduled to commence operation on Oct. 1, 1982. It remains to be seen whether it will be a blessing for patents or just another burden on the Federal budget.

This column sets forth basic principles of law and is not intended as a substitute for personal legal advice. Questions and comments are invited and should be sent to Mr. Brown in care of Electronics.



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Complete trigger system: Modes include TV field, normal, vertical mode, and automatic; internal, external, and line sources; variable holdoff.

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Siggraph '82—9th Annual Conference on Computer Graphics and Interactive Techniques, Association for Computing Machinery (Siggraph '82, Convention Services Department, 111 East Wacker Dr., Chicago, Ill. 60601), Hynes Auditorium, Boston, July 26–30.

International Conference on Solid State Devices, The Japan Society of Applied Physics (3-4-16 Yayoi, Bunkyo-ku, Tokyo 113), Sunshine City Prince Hotel, Tokyo, Aug. 24–26.

4th Annual Quartz-Crystal Conference and Exhibition (EIA Components Group, 2001 Eye St., N. W., Washington, D. C. 20006), Radisson Muehlebach Hotel, Kansas City, Mo., Aug. 31–Sept. 2.

VLSI Symposium, IEEE (Frank B. Micheletti, Rockwell International D/550, 136-HA27, 3370 Miraloma Ave., P. O. Box 4761, Anaheim, Calif. 92803), Oiso, Kanagawa, Japan, Sept. 1–3.

6th International Conference on Computer Communication, International Council for Computer Communication (P. O. Box 23, Northwood Hills HA6 1TT, Middlesex, UK), Barbican Centre for Arts and Conferences, London, Sept. 7–10.

Symposium on Electromagnetic Compatibility, IEEE (Andrew Nalbandian, P. O. Box 70577, Sunnyvale, Calif. 94088), Marriott Hotel, Santa Clara, Calif., Sept. 8–10.

16th International Conference on the Physics of Semiconductors, International Union for Pure and Applied Physics (Prof. Bernard Pistoulet, Centre d'Electronique des Solides, USTL, Place Eugène Bataillon, 34060 Montepellier, Cedex-France), Université des Sciences et Techniques du Languedoc, Montpellier, France, Sept. 8–10.

6th International Conference on Software Engineering, IEEE (Harry Hayman, P. O. Box 639, Silver Spring, Md. 20901), Tokyo, Japan, Sept. 13–17.

Mini/Micro '82 Computer Conference and Exposition, Electronic Conventions Inc. (999 North Sepulveda Blvd., El Segundo, Calif. 90245), Disneyland Hotel, Anaheim, Calif., Sept. 14–16.

Wescon/82—Western Electronic Show and Convention, Electronic Conventions Inc. (999 North Sepulveda Blvd., El Segundo, Calif. 90245), Anaheim Center and Anaheim Marriott Hotel, Anaheim, Calif., Sept. 14–16.

6th International Fiber Optics and Communications Exposition, Information Gatekeepers Inc. (Ellen M. Bond, Information Gatekeepers Inc., 167 Corey Rd., Suite 111, Brookline, Mass. 02146), Marriott Hotel, Los Angeles, Sept. 15–17.

32nd Annual Broadcast Symposium, IEEE (Robert A. O'Connor, CBS-TV, 51 West 52nd St., New York, N. Y. 10019), Washington Hotel, Washington, D. C., Sept. 15–17.

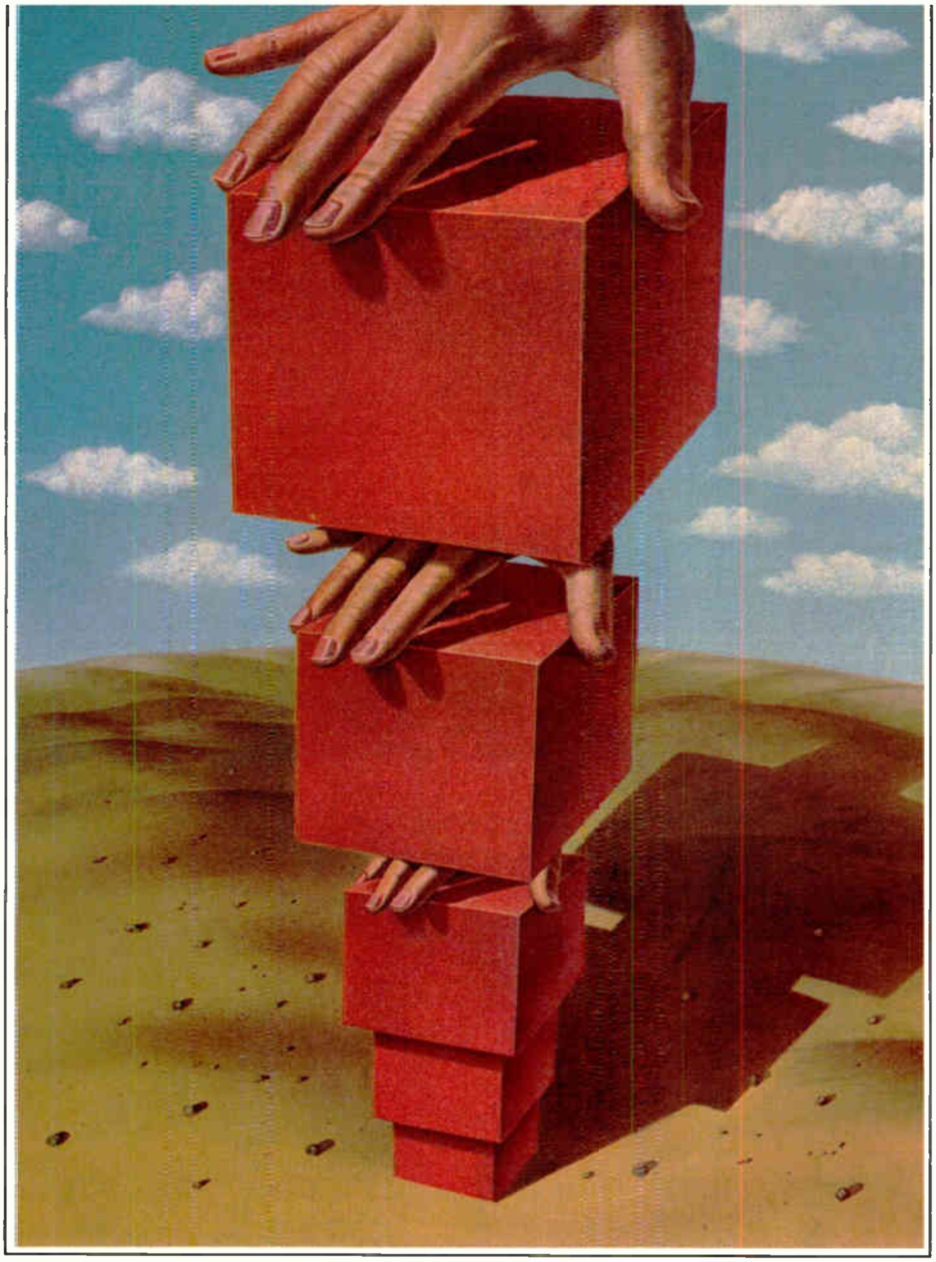
Frontiers of Engineering in Health Care, IEEE (Alfred R. Potvin, University of Texas at Arlington, Biomedical Engineering Program, P. O. Box 19138, Arlington, Texas 76019), Marriott Hotel, Philadelphia, Sept. 20–21.

Electronic and Aerospace Systems Convention (Eascon), IEEE (Lawrence R. Kitty, 4570 East-West Hwy., Bethesda, Md. 20814), Sheraton Washington Hotel, Washington, D. C., Sept. 20–22.

Compcon Fall '82, IEEE (P. O. Box 639, Silver Spring, Md. 20901), Capital Hilton Hotel, Washington, D. C., Sept. 20–24.

Seminars

Software Verification and Validation, Education Foundation of the Data Processing Management Association (P. O. Box 91295, Department SVV, Los Angeles, Calif. 90009), Boston, July 26–27; Washington, D. C., Aug. 2–3; Williamsburg, Va., Aug. 5–6.



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We designed the Series 80 from the inside out to be faster, quieter, more accurate and more efficient than any other analog or mixed-signal tester available.

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Our new Op Amp Application Package allows testing of single, dual, triple or quad op amps. And to greatly reduce your test time, ours is the only application package which enables you to simultaneously test quad op amps in parallel.

To fully characterize and production-test codecs, filters, codec/filters and SLICs with high correlation, our new Telecom Application Package provides all the digital and analog capability you need. And because the Series 80's architecture is fully integrated with digital signal processing, you get much higher accuracy and exceptionally fast test times.

The new Telecom Application Package uses a true programmable digitally synthesized function generator. And an audio digitizer designed for high-speed processing. Each instrument is available separately for other applications.

Since both of our new Application Packages are much more software-intensive than other available packages, they are also much more reliable.

The Series 80 analog test solution will help you push more, better-quality devices out the door than ever before.

For more information, call or write: Fairchild Test Systems Group, 1601 Technology Dr, San Jose, CA 95115, (408) 998-0123, Ext. 2296. Fairchild Camera and Instrument Corporation.

Circle 27 on reader service card

This new programmable sweep generator uses distributed microprocessor architecture.

CW accuracy can be held to ± 10 Hz or better by phase locking to external frequency counter or lock box.

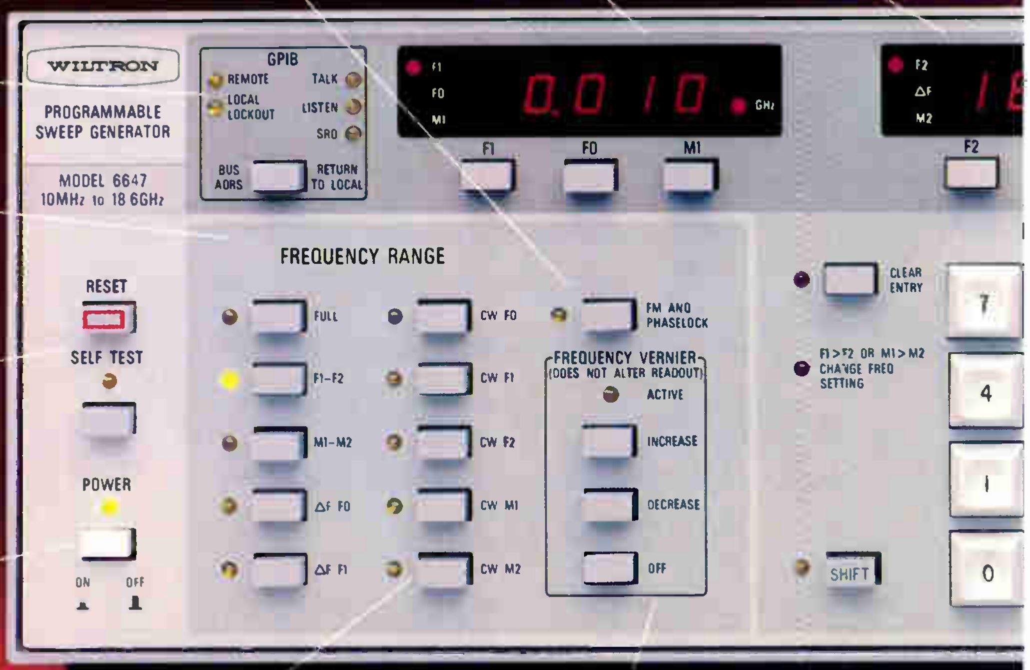
Both F1 (start) and F2 (stop) sweep frequencies, or M1, M2 marker frequencies or any combination can be displayed simultaneously.

GPIB (IEEE-488) bus messages include serial and parallel poll, group execute trigger and SRQ.

Five sweep modes provide broad or narrow band control for unprecedented measurement flexibility.

Self-test and automatic fault diagnosis occur every time the instrument is turned on; a diagnostic code is displayed on the front panel.

SAV and RCL commands can be used to store test setups. Non-volatile memory holds controls and readings at previous setting for 20 days or more.



Remarkably clean and stable CW signals are available with 1 MHz resolution at five pushbutton-selected frequencies or program-selected values.

Frequency Vernier with 100 kHz resolution allows precise adjustment of CW or center of ΔF sweep frequency.

Digital convenience and accuracy are part and parcel of the new Wiltron 6600, an eminently easy-to-use family of instruments which combines new RF technology with microprocessor control. With 10 MHz to 40 GHz coverage, the 6600 group is expressly designed to meet your ATE needs too. There are, quite simply, no more advanced sweeper/signal sources at any price.

A look at the features

Here in one compact 33 pound unit we give you a virtually self-explanatory pushbutton controlled front panel. All pushbutton controls can be programmed via the IEEE-488 interface bus. We give you a sweeper using fundamental oscillators avoiding the substantial errors generated by the harmonic products of multiplier type oscillators. We give you modular construction without the disadvantages of RF plug-ins. We give you a fast unit using distributed microprocessors and a display preprocessor to reduce bus loading and measurement times.

The result, broadband coverage with the lowest harmonic content (>40 dBc, 2-20 GHz), lowest residual FM and greatest stability on the market today. We give you a unit with the best frequency accuracy (±10 MHz up to 20 GHz) because it uses a ROM to correct non-linear residual frequency characteristics of YIG oscillators.

Programmable parameters include stepped sweep with selectable step size, start and stop frequencies, sweep width, marker frequencies, sweep time, output power level and optional attenuation.

Other features of note include high spectral purity, modular construction, self-test, 82 dB power control range with 0.1 dB resolution and power sweep.

So easy to operate

Multiple microprocessor design and human engineered panel controls make it easy for even the least experienced to use—on or off the bus.

It's a Wiltron.

Optional attenuator provides bus or front panel control of power level over 82 db range.

All frequencies, sweep times, power levels and their units are displayed when selected on the corresponding pushbutton or commanded over the bus.

Three markers provide easy identification of swept frequencies, center frequency of ΔF sweep and M1-M2 sweep limits.

Slope control compensates for losses that vary with frequency to provide flat output at test point.

Excellent source match (<1.4 up to 20 GHz) reduces measurement errors.

Wiltron super-flat leveling components hold variations in output power to <±0.6 dB from 10 MHz to 20 GHz.

External directional detector or power meter can be used to level output power at remote test position.

Keypad provides fast, precise data entry.

Convenient electronic control lever obsoletes tedious and inaccurate twiddling of mechanical control knobs.

Eight models cover the frequency range of 10 MHz to 40 GHz.

Model	Range	Power
6609	10 MHz to 2 GHz	>20 mW (+13 dBm)
6617	10 MHz to 8 GHz	>10 mW (+10 dBm)
6637	2 GHz to 18.6 GHz	>10 mW (+10 dBm)
6638	2 GHz to 20 GHz	>10 mW (+10 dBm) at ≤18.5 GHz >5 mW (+7 dBm) at >18.5 GHz
6647	10 MHz to 18.6 GHz	>10 mW (+10 dBm)
6648	10 MHz to 20 GHz	>10 mW (10 dBm) at ≤18.5 GHz >5 mW (+7 dBm) at >18.5 GHz
6636	18 GHz to 26.5 GHz	>3.1 mW (+5 dBm)
6640	26.5 GHz to 40 GHz	> 1 mW (0 dBm)

Compare the Wiltron 6600 with any other sweeper

For a demonstration and/or our new brochure, phone Walt Baxter, (415) 969-6500, or write Wiltron, 805 E. Middlefield Road, Mountain View, CA 94043.

WILTRON

Circle 29 on reader service card

K100-D

GOULD BIOMATION

7 reasons why the K100-D is now the world's best-selling logic analyzer.

How the general-purpose K100-D beat out H-P to become #1.

Not so long ago, Hewlett-Packard logic analyzers were the industry standard. We asked digital designers to compare the K100-D with H-P's popular 1610B and 1615A logic analyzers before making any buying decision.

In head-to-head comparison, the K100-D came out looking so good, it's now the best-selling logic analyzer in the world. Here's why:

1. It's easy to systematize.

For automated troubleshooting and production ATE, the K100-D features a fully-programmable GPIB interface.

To help you support a wide variety of bus-oriented systems, there are standard high-performance probes, specialized probing accessories and detailed application notes available on all the popular microprocessor systems currently in use.

2. It's concise.

The K100-D monitors 16 channels in time domain, 32 in data domain, so you can probe enough points to pin down problems at their source.

3. It's fast.

A 100 MHz clock rate resolves signals to 10 nanoseconds. The front end is also sensitive enough to capture glitches as narrow as 4 ns.

4. It's deep.

1024 words deep in memory—for faster, more accurate debugging. The K100-D extends the length of data you can trap from your system at any one time.

5. It's clear.

The K100-D has a large keyboard and interactive video display, a comprehensive status menu, highly useful time domain display, and data domain readout in user-specifiable hexadecimal, octal, binary or ASCII.

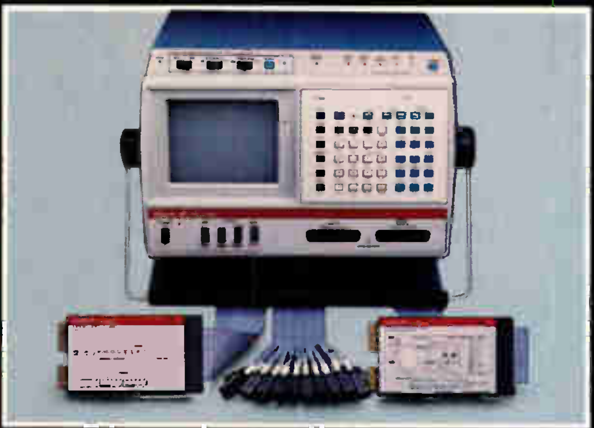
6. It has remote diagnostics.

A new T-12 communications interface option lets your field troubleshooters share their system observations with the best engineers back at headquarters. Remote diagnostics provide faster debugging and save a lot of time and travel for your most valuable people.

7. It's well supported.

You get full applications support from the experts in logic analysis.

For a free copy of our "Logic Analyzer Comparison Guide," request card for microprocessor system application notes, and T-12 Communicator information, just circle the appropriate reader service numbers. Or contact Gould, Inc., Instruments Division, Santa Clara Operation, 4600 Old Ironsides Drive, Santa Clara, CA 95050, phone (408) 988-6800.



The T-12 "top hat" for the K100-D provides logic analyzer remote diagnostic capability. Other options include the GPIB Analyzer and RS232 Serial Data Analyzer.

GOULD
Electronics & Electrical Products

Circle 30 for Comparison Guide
Circle 31 for APP Note request form
Circle 170 for T-12 communicator data

News update

■ Outshone by more versatile silicon, germanium semiconductors not only have refused to fade away fully, but their proponents now are launching new designs after years of coasting with mature products. Dividing about $10 million of yearly business are two U. S. firms, Lansdale Transistor & Electronics Inc. and Germanium Power Devices Corp. [*Electronics*, March 17, 1977, p. 69]. They are the sole survivors of dozens of germanium-based companies that bloomed and faded in the 1960s.

Located in Phoenix, Ariz., Lansdale is bringing out what its president R. Dale Lillard calls "the first new germanium transistor since 1968." It is a 150-ampere power device whose low saturation voltage of 0.5 volt dc represents the one edge germanium has over silicon. Already, customers include General Motors and major telephone and aircraft firms, he asserts.

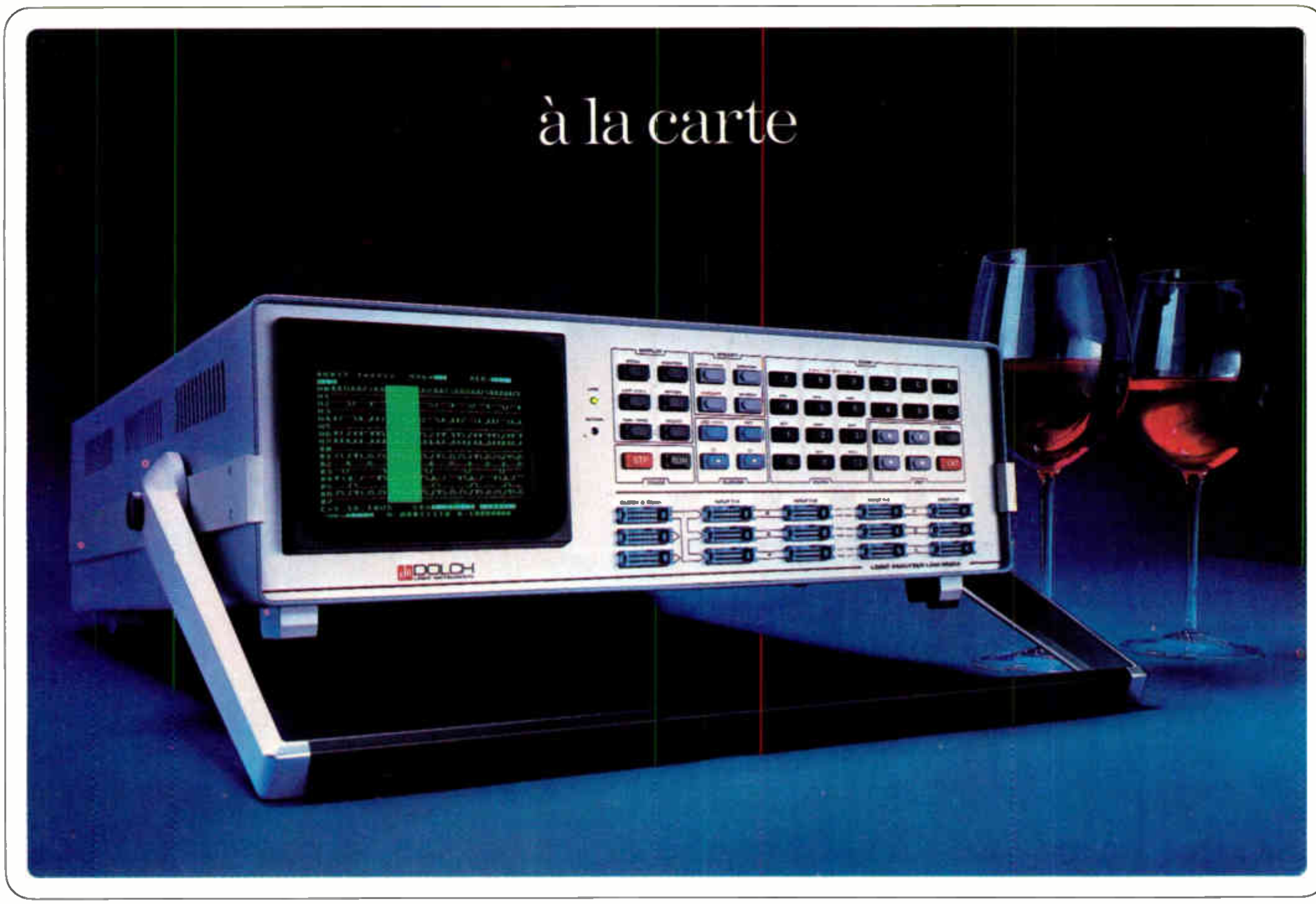
New line. Playing down his competitor's new transistor ("We have that already well covered"), Germanium Power Devices' marketing vice president, John Adams, lauds a new rectifier line. It sports key forward-voltage-drop improvements over silicon Schottky devices, with higher efficiencies and lower power dissipation. A 200-A unit has a forward-voltage drop of 0.42 V at 100 A and reaches only 75°C, against Schottky's 0.5 V and 175°C.

One sign germanium prospects could be brightening is the heightened competition between these two remaining rivals. Germanium Power Devices' Adams thinks the potential for rectifiers tops that for transistors because of the lower-voltage logic going into big computers.

At Lansdale, Lillard sees the military electronics buildup creating demand for his transistors, as it did two decades ago. He is also hedging somewhat by acquiring mature integrated-circuit lines, notably a diode-transistor-logic line from Raytheon Corp. However, both executives do agree on a couple of things: that silicon is inferior to germanium for power and signal uses; and that the other firm is a valuable asset—as a second source. **-Larry Waller**

Dolch.

advanced logic analysis



48 to 96 Channels, 300 MHz, plus Mnemonics

Order up your parameters. Dolch's LAM 4850A logic analyzer makes it easy with a new key — Monitor. Monitor gives you status information and comments on menu setups, and can be called up at any time to interpret each parameter, its range, and its interaction with the current setup. And, you can store your setups for three months without power, eliminating the need to reprogram.

Zero in fast. The LAM 4850A disassembles your code into Mnemonics and gives you the channels you need to trace data, address, port and control lines. And for future needs, you can expand to 64, or even 96, channels.

Circle #172 for demonstration

Hook up fast, too. Dolch personality probes clip right over your CPU chips so you don't waste time connecting dozens of individual hooks. And the probe takes care of clock, timing and signal interfacing — no need to worry about signal conditions.

300 MHz sampling across 16 channels. A revolutionary option gives you the ultimate in sampling resolution — 3.3 ns — to help you solve the toughest timing and phase related problems. A unique memory overlay configuration provides simultaneous dual asynchronous recording across 16 channels without compromising any of the LAM 4850A features.

Don't settle for less than Dolch. The basic LAM 4850A is truly a universal logic analyzer system with 50 MHz sampling rate, 1000 bits per channel source and reference memories, and sophisticated sequential trigger and multilevel clocking.

For details on the Dolch LAM 4850A, or any of our other troubleshooting tools, write: Dolch Logic Instruments, Inc., 230 Devcon Drive, San Jose, CA 95112. Or call toll free: (800) 538-7506; in California call (408) 998-5730.

dli DOLCH
LOGIC INSTRUMENTS

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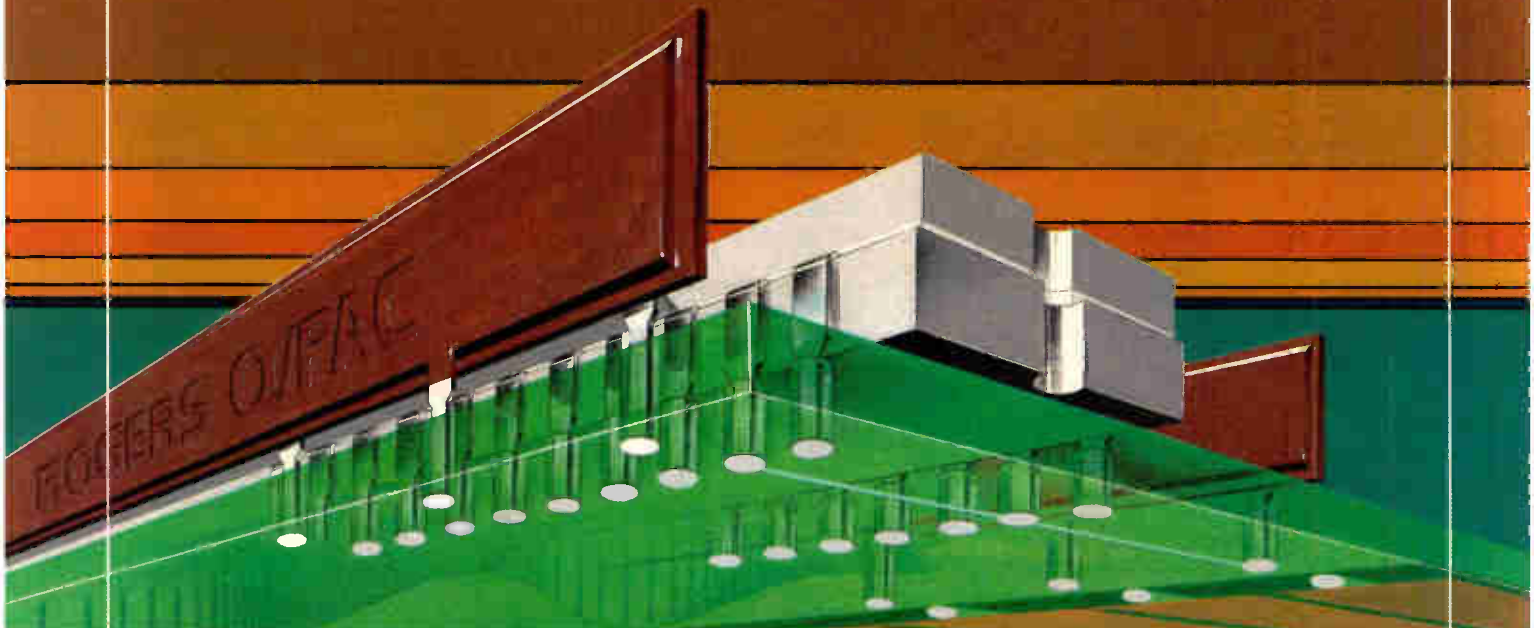
THE Q/PAC® POWER DISTRIBUTION CAPACITOR.

A SMALL REVOLUTION IN PCB PACKAGING TECHNOLOGY.



Now there's a way to achieve ultra-efficient power distribution and high capacitance with the same space-saving component: Q/PAC® from Rogers.

A small revolution in PCB packaging technology, Q/PAC power distribution capacitors improve and simplify all aspects of board design. Rugged and easy to install, they eliminate on-board power traces. And provide noise suppression unmatched by conventional discrete decoupling capacitors.

What's more, since Q/PAC saves valuable real estate by replacing both power traces and discrete decoupling caps, there's more space for signal routing and interconnecting IC's. So you can increase density on dependable two-layer boards—and avoid expensive multilayer.

The simple, cost-effective way to package high-density, low-noise logic, memory and other boards, Q/PAC power distribution capacitors feature low impedance, low dissipation, low inductance and excellent electrical performance. They're available in capacitance values up to 0.04 μf/in. in lengths up to 16". With 2 or 3 conductors in either vertical mounting or horizontal under-the-DIP constructions.

To find out more about how Q/PAC can revolutionize your packaging possibilities, call a Rogers Q/PAC Product Specialist today at (602) 830-3370.

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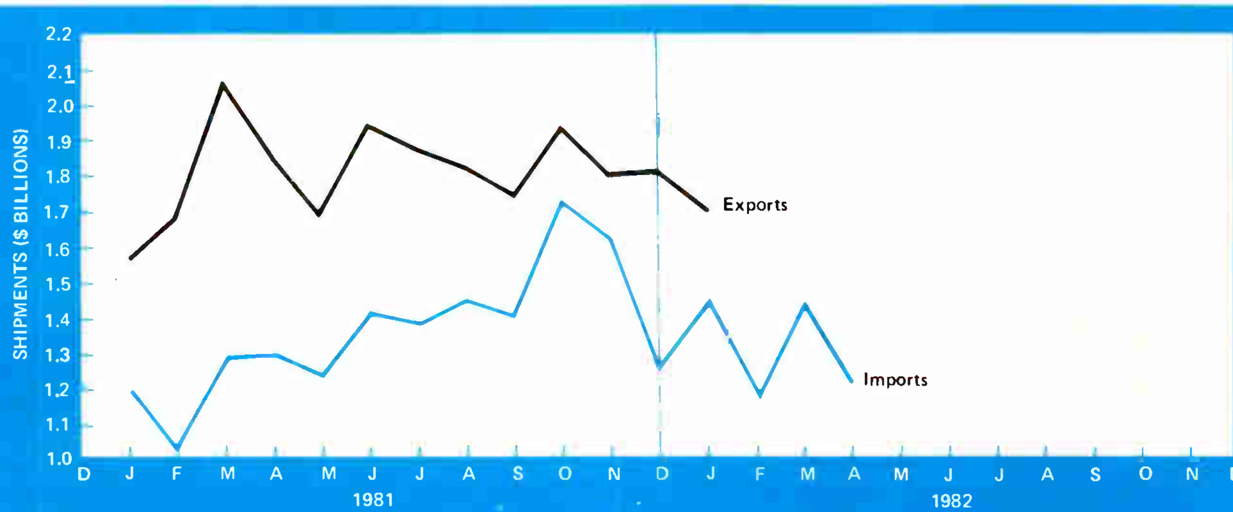
Rogers Corporation Q/PAC Division 5750 East McKellips Road Mesa, AZ 85205

Circle 34 on reader service card

Business activity



U.S. ELECTRONICS IMPORTS AND EXPORTS

SOURCE: BUREAU OF THE CENSUS

U.S. ELECTRONICS IMPORTS AND EXPORTS[1] (MILLIONS OF DOLLARS)

	IMPORTS			EXPORTS		
	April 1982	March 1982	April 1981	April 1982	January 1982	April 1981
Accounting, computing, and data-processing machines	72.595	69.984	51.626	416.749	376.622	382.796
Calculators	29.559	39.443	35.216	8.012	10.110	9.405
Parts for data-processing machines and office calculators	102.089	110.551	81.187	309.157	306.475	296.526
Telecommunications, sound-recording, and sound-reproducing equipment	561.145	755.326	741.184	295.209	279.898	306.143
Electronic or electric instruments	63.648	72.082	69.675	not available	410.725	372.341
Printed-circuit boards	16.102	16.913	11.180	10.907	11.689	8.661
Integrated circuits, diodes and other semiconductors, tubes, piezoelectric crystals, parts	351.909	355.195	299.713	340.734	296.212	304.354
Fixed and variable resistors	14.409	15.130	13.043	11.264	12.210	10.414

U.S. ELECTRONIC-COMPONENTS PRODUCER PRICE INDEX[2] (1967 = 100)

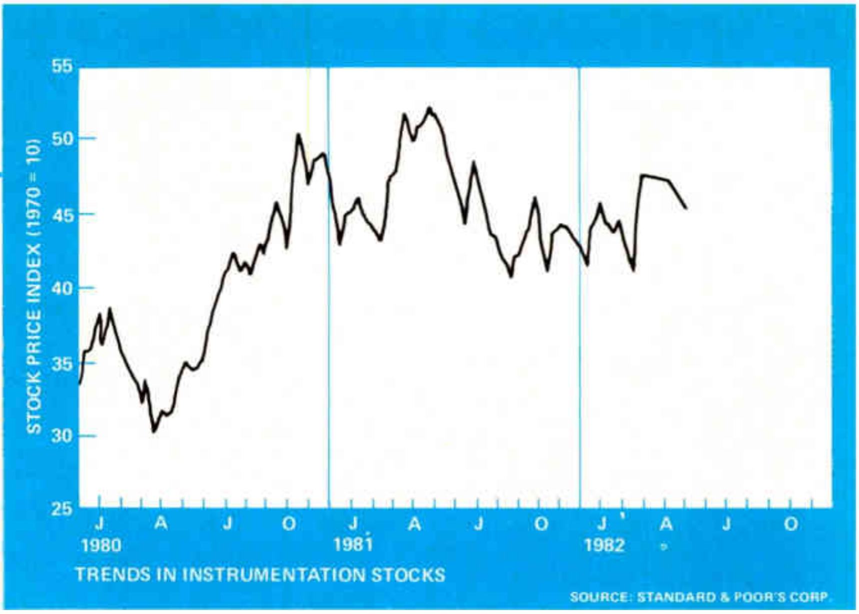
	April 1982	March 1982	April 1981
Digital bipolar integrated circuits	51.2	51.2	53.8
Digital MOS ICs	46.9	47.2	53.2
Linear ICs	55.3	55.8	58.9
Capacitors	198.4	197.5	196.1
Resistors	175.2	174.5	168.9
Relays	235.3	234.4	209.4
Connectors	219.1	218.5	214.1

GENERAL U.S. ECONOMIC INDICATORS

	May 1982	April 1982	May 1981
Average prime rate (%)[3]	16.50	16.50	19.61
Retail sales ($ billions)[4]	89.236	87.899	86.361
Unemployment rate (%)[2]	9.5	9.4	7.5

SOURCES: [1] Bureau of the Census [2] Bureau of Labor Statistics [3] Federal Reserve Board [4] U.S. Department of Commerce

Business activity



The stock market shows no signs of recovery as June heads into July. The Dow Jones industrial average has dropped to its lowest point in two years. Analysts say that if the market does go any lower, it may be a first step towards the selling climax that will probably come before the market can stage a sustainable rally. Much of the weakness is due to investors who were convinced that interest rates had peaked but now fear that the rates may instead rise sharply. Most electronics issues outperformed the market somewhat, with Motorola, NCR, Texas Instruments, and Wang Laboratories among those issues showing better than average gains.

The economy continued to slide further in May as industrial production fell another 0.2%, as did capacity utilization. In addition, unemployment is still rising, with the jobless rate reaching 9.5% and little chance for improvement in June. However, the declines in output and plant use are much smaller than in previous months, and other signs are emerging that the slump may be ending, although at a rather slow pace. The encouraging news has been coming mostly from consumers as retail and auto sales continue to improve. Still, sales of hard goods or big ticket items are weak, and there is worry that car sales may deteriorate as General Motors ends its reduction in financing costs.

With so little in the way of good news and continued worry about high interest rates and budget deficits, it is not surprising that there is a growing perception that there may be no recovery at all. A quick turnaround seems unlikely, but signs of an uptick should become more evident as the July 1 tax cut and the Social Security cost-of-living increase stimulate the economy. Although the Federal Reserve has taken a less restrictive stance in recent weeks, large increases in the money supply during July should result in a renewal of a tight-money situation along with higher interest rates.

Most companies have cut back on their capital spending plans during the recession, but many electronics firms have not. One example of this optimism is General Telephone & Electronics Corp., where president and chief operating officer Thomas A. Vanderslice says that capital expenditure plans remain at about $3 billion. He indicated that a large portion of capital expenditures would go to projects in packet-switching networks and cellular radio. At American Telephone & Telegraph Co., the bulk of the $18.2 billion capital budget will be financed internally because Bell intends to avoid the bond market until divestiture of its local operating companies is completed.

How to turn your modem outside-in.

Turn to Rockwell. We're showing designers how to replace a black-box modem that's outside their computer-based products—with one that's inside. One that's modular, integral, and MOS/LSI-based.

Our integral modems give your products added value, so you get a leg up on your competition.

That's because they provide all the features of black-box modems—but at a fraction of their cost. Plus their compactness gives you new physical design freedom.

And Rockwell modems are available at a level of integration that meets your requirements. Take our R24, for example. A 2400-bps synchronous modem, it comes in three configurations—all exceptionally compact, and compatible with Bell 201 B/C and CCITT V.26 A/B standards.

First there's our fully assembled and tested single-board modem, ready to plug into your system—like the one shown above. Then there's our set of three discrete modules, ready to be designed into your own modem. They allow you to separate transmit and receive functions, if desired. And to speed your modem integration design cycle, there's also an R24 evaluation board available.

Which means that when you're designing computer-based terminals and communications equipment, you can now bring the modem inside your product. How? By integrating the R24's solid-state reliability and economy into your product, for both leased-line and switched-network applications.

That's just the kind of advantage you'd expect from Rockwell, the company that's delivered more integral LSI 4800/9600-bps modems than anyone else in the world. That's right—*anyone*. And Rockwell modems are in stock now—fully assembled, on production or evaluation boards, or as discrete modules.

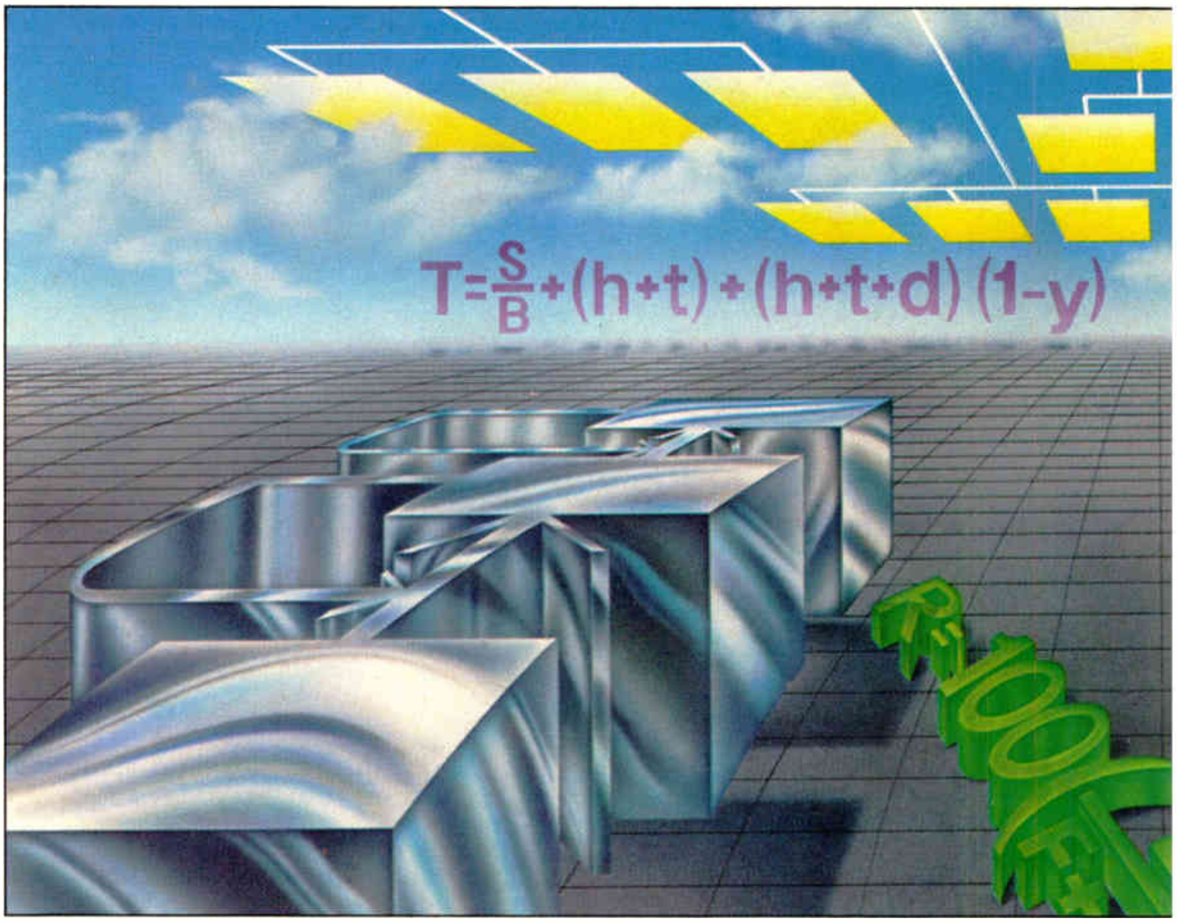
So don't leave your modems on the outside looking in. For information or applications help, call toll free: (800) 854-8099; in California, (800) 422-4230. Or write: Rockwell International, Electronic Devices Division, RC55, P.O. Box 3669, Anaheim, CA 92803.

Rockwell International

...where science gets down to business

Circle 37 on reader service card

For every product line, there's just one correct test strategy. We can help you find it.



Intermittent Problems?

Blowing a Fuse?

Whether they blow fuses or not, transients can cause disruption in all modern electronic equipment. Their sources may be found in power line disturbances or in the internal circuitry itself.

Find Out Why

For many years, power line monitors have given us data on the number and amplitude of line transients, but not on their causes. Today improvements in instrumentation make it possible to capture whole waveshapes, revealing information on the nature of a transient. A recent Navy report has made progress in categorizing types and suggesting typical signals resulting from events such as abruptly energized transformers and switch contact arcing. Figures 1 and 2 show transients from a 60Hz, 120V shipboard power network. They are similar in amplitude and duration, but distinctly different in type. The Nicolet Digital Oscilloscope's pre-trigger viewing and large memory size capture the entire wave signature. Amplitude and duration can be read from the screen's numerics.

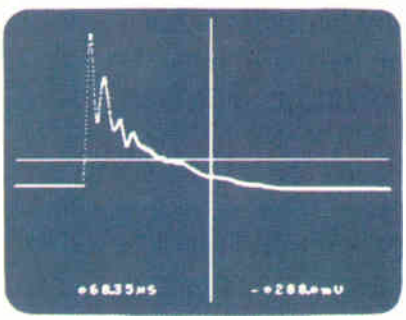


Fig. 1: One type of power line transient

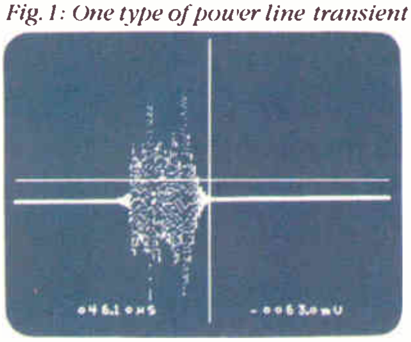
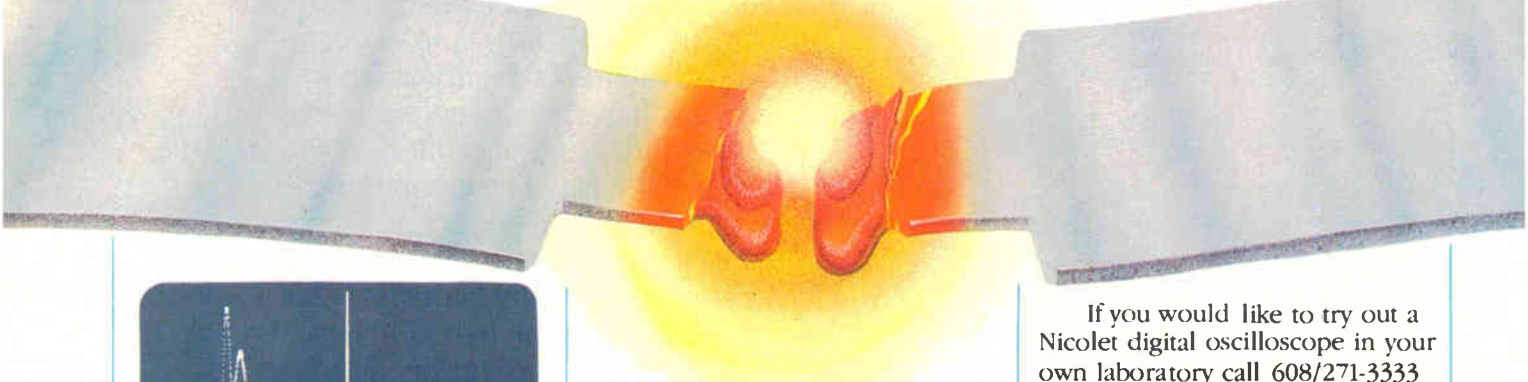


Fig 2: Second type of transient from same network.



Erratic Unexplained Errors?

Intermittent errors located within electronic circuitry are illustrated in Figure 3. This bothersome transient was detected during development of a complex daisy wheel printer. Although a logic analyzer indicated an error condition, the nature of the error remained a mystery. By triggering the Nicolet scope on the error, a fault in the daisy wheel displacement was isolated and corrected.

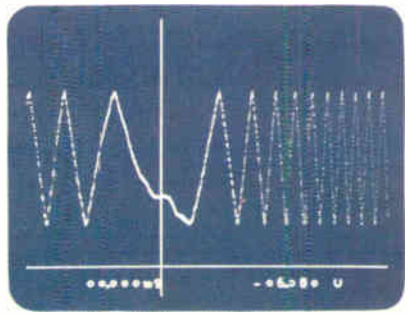


Fig. 3: Print wheel movement. Glitch caused by noise in control circuitry

Let a Nicolet Scope Capture the Cause

In both these examples, transients were captured and recorded on floppy disk automatically, freeing engineers and technicians for more important tasks. Later the signals with all their original data were recalled for detailed examination and comparison.

The data could then be manipulated, plotted or transferred directly to a computer for more complex calculations, for example, of the energy content of the transients.

The Nicolet digital oscilloscope is using new technology to solve long-standing problems. With its help, even hard to find intermittent problems are being isolated and eliminated.

If you would like to try out a Nicolet digital oscilloscope in your own laboratory call 608/271-3333 or write Nicolet Instrument Corporation, Oscilloscope Division, 5225 Verona Road, Madison, WI 53711.

In Canada: call 416/625-8302.

NICOLET INSTRUMENT CORPORATION
OSCILLOSCOPE DIVISION

* Waveforms courtesy of Naval Electronic Systems Engineering Activity and Diablo Systems Inc., Div. of Xerox.

Circle #40 for immediate need

Circle #173 for literature only

Japanese say they made legitimate deals for IBM data

The Japanese firms involved in the U. S. charges that their employees paid a total of $648,000 for IBM computer designs admit paying the money to what they thought were legitimate industry consultants but say they had no way of knowing the data was stolen. Meanwhile, court papers indicate the information they received was not secret. While Hitachi Ltd. and Mitsubishi Electronics Corp. refuse to comment on the Federal Bureau of Investigation's inquiry, **the feeling in Japan is that they were tricked by an Abscam-like operation.** Hitachi says that its senior executives did not know that Kisaburo Nakazawa, general manager of the Kanagawa Works, had approved spending $622,000 for information.

Computer makers in Europe agree on net protocol

Computers of all makes are much closer to talking to each other over local networks. The International Standards Organization (ISO) has adopted a draft proposal governing the fourth (or transport) layer of a seven-layer protocol. Worked out by the European Computer Manufacturers Association (ECMA), which is said to be opting for Ethernet, with Britain's International Computers Ltd. playing a leading role, the standard would be network-independent. Intel Corp. is working with ICL to cast the protocol in silicon, and **industry-standard chips for use in ring or Ethernet systems could be ready next year.** They also may conform to the still-awaited standard of the Institute of Electrical and Electronics Engineers. The new standard is based on the ISO's model for wide-area open systems interconnection, so local and wide-area nets could be integrated easily.

Telidon first to meet AT&T videotex rules

In a move that is significant for the videotex industry, Telidon, the scheme developed in Canada, is the first to conform to American Telephone & Telegraph Co.'s presentation-level protocol for such services. That Telidon beat England's Prestel or France's Antiope systems to the mark is important **because of AT&T's anticipated clout in the videotex business, which insiders say the company will pursue vigorously.** The move follows closely the entry of IBM into the U. S. videotex market.

Sharp, ECD form solar-cell venture

Energy Conversion Devices Inc. of Troy, Mich., has entered a joint venture with Sharp Corp. of Japan to produce commercial amorphous silicon solar cells using the American firm's technology. Sharp will pay $3 million to Energy Conversion in exchange for technical assistance and continuous-web production equipment **that is capable of turning out 1-ft-wide amorphous cells.** Energy Conversion, which says the cells have been 9.2% efficient in the laboratory [*Electronics*, May 5, p. 34], will ship a machine to Japan during the third quarter. The joint venture, 51% owned by Sharp, will be known as Sharp-ECD Solar Inc. Sharp will use the cells in calculators.

Laser writing helps match devices

Laser photodeposition for direct writing and modifying of complex devices on a chip could help in custom fine-tuning of circuits whose devices must be tightly matched, say researchers at the Massachusetts Institute of Technology in Lexington, Mass. The frequency-doubled output of an argon infrared laser breaks up gaseous organometallic molecules and produces free metal atoms that condense onto a chip, thus bypassing multiple-step photolithographic techniques. In this way, **the researchers have written cadmium-gate electrodes onto prefabricated silicon MOS field-effect transistors.** Because each electrode is formed by repeatedly scanning the laser beam to create 2-μm-wide metalized lines, the researchers say that controlling the number and duration of the scans varies electrode dimensions, which determine threshold-voltage and transconductance characteristics of individual MOS FETs.

Device monitors oxygen in brain

A microprocessor-based device developed at Duke University in Durham, N. C., will allow direct, continuous, and near-instantaneous measurements of the brain's oxygen level during surgery. The Niros (for near-infrared oxygen sufficiency) **beams near-infrared light into the brain through fiber-optic bundles encased in headgear, and a microprocessor analyzes the reflected beams.** American Edwards Laboratories, Irvine, Calif., expects to have it on the market by 1984.

Intel stations to join club

Look for Tektronix Inc. to provide users of Intel Corp.'s development systems with the means **to hook those systems to the Beaverton, Ore., firm's multiuser development system, the 8560, and a hardware-software integration unit, the 8540.** An interconnection package, containing ISIS-II software extended for the 8560 and 8540, will cost about $500 and will be ready this fall. Hewlett-Packard's Colorado Springs division is also said to be working on a similar scheme that would allow Intellec systems onto the HP 64000 development network.

Intel-Motorola bubble deal has tight schedule

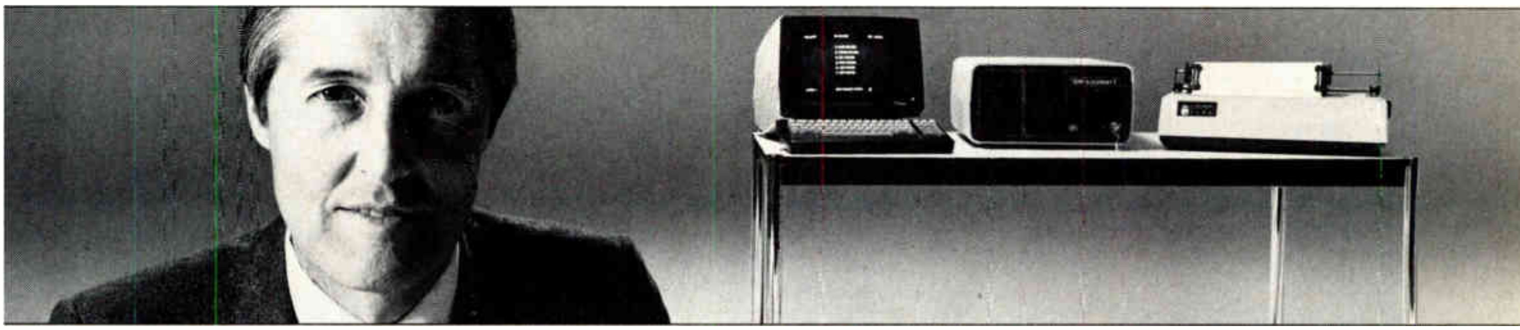
One aftermath of the exchange agreement on magnetic-bubble memories between Motorola Inc., Schaumburg, Ill., and Intel Corp., Santa Clara, Calif., is a tight schedule of design tasks. By late summer the pair has to come up with detailed specifications **for two new 1-megabit memories due to customers beginning in the second quarter of 1983.** For these, cell size must drop to 8 μm from the 10.5 μm for Intel's existing 7110 memory. The second new device must also halve access time—currently about 40 ns—and double data rate to 200 kb/s. Under the late-June agreement, the first ever between the two firms, Intel supplies existing device designs, while Motorola provides its process technology.

Addenda

The latest wearer of the crown as most powerful superminicomputer is the dual-processor Concept 32/8780 announced by Gould SEL in Fort Lauderdale, Fla. The firm says its **computer was clocked at a blazing 17,477 Whetstones/s**—about 24 times the speed of a VAX-11/780. . . . In keeping with its policy of expanding outside Silicon Valley, National Semiconductor Corp., **which just reported a loss of $10.7 million for its fiscal year ending May 31,** opened a systems development center in Mesa, Ariz. . . . Xerox Corp.'s newly introduced 820-II personal computer uses a Z80A 8-bit microprocessor and a microcoded random-access memory that speeds the CP/M operating system. **The machine is sold for from $3,295 to $4,895 as an entry-level professional work station** that can interface with the firm's Ethernet communications network.

"Workstation 1 is the first microcomputer system designed to break down."

Gordon Watson,
Vice President/General Manager,
Naked Mini Division,
ComputerAutomation



"I'll admit, it takes guts to sell OEMs a system like this. A lot of guts.

And that's exactly what we've got in our new Workstation 1™ microcomputer system.

You see, we've designed Workstation 1 to be completely modular, with 62 unbundled product options. You can buy it as a package. Or we'll break it down and sell it as parts.

Starting with the basics: a four or nine-slot chassis with cable and harness. From there, you can add just as much, or just as little, as you want.

CPU. Memories. I/O. Controllers. Power supplies. Any combination of 5¼" floppies and Winchesters. A range of CRT's and printers. Our software. Your software. Even third party software.

And it's all available in any quantity, at any integration level. So instead of getting the system we think you need, you can get the system you think you need.

You know, maybe we shouldn't say Workstation 1 is designed to break down.

It might be more accurate to say it's designed to break through."

ComputerAutomation NAKED MINI® Division
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Circle 43 on reader service card

Plug-in boards add vision, functions to range of robots

by Terry Costlow, Costa Mesa bureau

CCD array provides picture, TTL provides the speed; designers aim at setup blue-collar workers can handle

Even newer than robotics itself is the expertise for endowing them with vision. Whereas most electronics houses having a go at it end up with microprocessor-based systems that must be custom-designed for individual robots, a new California company is developing a set of circuit boards that can be plugged together to perform a variety of functions for a range of robots.

Striking off alone on this path, Electro Optical Integrated Controls Inc. of Solana Beach does not believe in the customizing approach, which might require the user to have special hardware design or programming expertise, according to its president, William J. Heinicke. "If a blue-collar worker went to high school and can read an instruction manual, he'll be able to hook up our vision system," he says, trying to dispel visions of white-coated experts taking over on the factory floor.

Another thing the company set out to avoid was having the vision system under microprocessor control. "Such a system would operate too slowly," says executive vice president Lawrence A. Murray. Instead, some 15 boards are designed with hardwired TTL.

Dedicated boards. A unit combining the firm's dedicated boards to fit the needs of most users would sell for under $15,000, according to Murray. Most currently available vision systems cost anywhere from $20,000 to $40,000, he points out. The boards typically measure 4.5 by 6.5 inches and plug into an STD-bus chassis, which, in turn, is connected to the programmable controller that drives the robot.

According to Murray, the logic circuits, by comparing the shape of a real part with the shape of a standard part stored in random-access memory, can decide if they match "in 33 milliseconds easily and we are pushing down to 5 ms, or 200 decisions per second." The speed makes it possible to display pictures on standard TV monitors whose frame rate is 30 ms, he adds.

For an original-equipment maker, the advantage of the modular approach would be responsiveness: "The OEM could really put it together quickly," says Perry C. West of Automated Vision Systems Inc., a consulting firm in Campbell, Calif.

Functions include part identification, defect detection, and a part-location process that places the part in an X-Y reference frame and then electronically rotates the image until it corresponds to the image stored in memory. One board might suffice, for example, for a simple chore like controlling an air gun by means of a solenoid to blast a screw found faulty into a defect bin, Murray says. But boards can be combined to make the system complex enough to identify a randomly positioned part, locate it, and direct the robot arm to grasp and assemble it, he continues.

Currently, Murray is relying on a 488-by-380-element charge-coupled device from Fairchild Camera & Instrument Corp. The $4,500 price tag is high for Murray's taste, and he is considering switching to a less expensive, yet adequate unit with 288 by 208 elements from France's Thomson-CSF.

By October, he also hopes to have a board that would convert the output of a standard (and inexpensive) 1-in. vidicon tube into a CCD picture-element format that his other boards could then process. "The vidicon would cost us only $200," he says. "However, it is fragile, much larger than the CCD sensor, and won't work in low light levels, so we would have

Robotic. William J. Heinecke, left, and Lawrence A. Murray of Electro Optical Integrated Controls eye the prototype of their Vuebot 301 robot controller. Shapes on the wheel indicate parts' shapes that can be identified using the CCD camera.

to really choose where it can be applied."

The firm's initial product, the Vuebot 301, shown on page 47, was introduced last week. It has only a limited number of boards and is geared to familiarizing potential users with its operation. Production prototypes with more functions are set for introduction late this year. At the front end are cards to handle such functions as memory, timing, and detect and store. Output is handled by what are called personality boards, which convert data to the format required by the more popular robot controllers, says Murray.

"This is one of the few [vision systems] that convert information to the format you need. Most just say 'here's our output,'" says Ron Fukui, control engineer at Prab Robots Inc., a Kalamazoo, Mich., robot maker. He notes too this makes it easy to integrate the system. "We can't afford to develop vision software for each job."

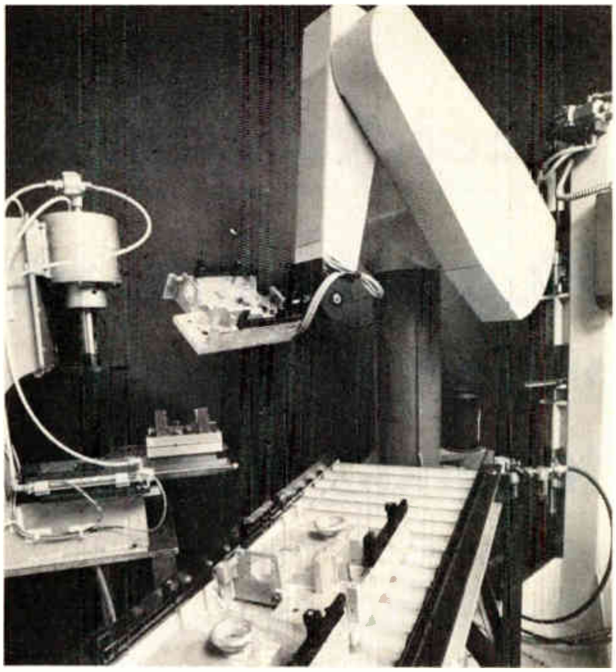
Detractors call the approach too simplistic for the real world. "The key is to get as close as possible to human-like vision. A memory comparison routine is just too far behind the times," says Gary Johnson, marketing and sales vice president at Perceptron Inc., a Farmington Hills, Mich., maker of microprocessor-based vision gear.

Production

Robot helps in disk-drive assembly

Squeezing the costs out of manufacturing is going to play an increasingly important role in helping electronics companies stay ahead of their competition. That is why Shugart Associates Inc., the inventor and No. 1 supplier of 5¼-inch floppy-disk drives, has turned to the strong arm of a robot to hold down its costs.

The Shugart robot arm performs the first eight steps in assembling the mechanical core of the firm's model SA 410 and 450 5¼-in. drives. The arm picks up the main casting and inserts a bearing, inserts the spindle, installs a spring, inserts another bearing, mounts a pully on the spindle, and installs two disk guides along the casting sides.



Helper. This Puma robot at Shugart Associates is lifting the main casting for one of the firm's 5¼-in. disk drives as it takes the casting to a press (left) where the spindle drive is inserted.

According to Ron Albo, manager of advanced-production technology at Shugart in Sunnyvale, Calif., "The robot builds one assembly in 78 seconds. With some minor adjustments, we believe we can cut this to about 53 seconds." In contrast, it takes three persons about 2 minutes to complete the tasks manually.

The robot is a model 550 Unimate Puma (see figure), a medium-sized manipulator made by Unimation Inc., Danbury, Conn. It can swing its arm in a 34-in. arc and lifts up to 5 pounds. The central control for the Puma is Digital Equipment Corp.'s LSI-11, which, in turn, reaches the outside world through a bank of 16 relays—eight input and eight output. This relay interface connects with Texas Instruments Inc.'s model 5TI programmable controller that monitors and controls the work stations around the Puma, including the parts feeders and presses.

"We monitor everything from checking to see that a part is ready to be picked up to the position of each moving section of the hardware," says Albo. But the arm is not just a "pick and place" unit, although it can pick up a part from a pallet. But the next time it goes for that part, it proceeds to the next position on the pallet. When the pallet is empty, it signals for another.

Sharpener. Getting the Unimate to do what Shugart wanted was fairly simple, says Albo. "To become familiar with the system, the first thing I did with the robot was teach it to sharpen pencils," Albo says. "The Puma comes with a 'teach box' that lets you move the arm where you want, and you can store the program for use later. In fact, the program is stored on a 410, the same drive the machine is building." The company received two models in late 1980 and plans to pick up a few more next year, Albo says.

The system can also be programmed through a cathode-ray-tube terminal. "Unimation is one of the few robot makers to have a high-level language, which makes it very easy to control the arm and modify the program if you want to fine-tune it or if you change one of the parts being installed," says Albo.

Ironed out. After getting the feel of the system, Albo and his group began designing the manufacturing station last July and had it running by November. "We had some initial problems with the robot's electronics, but we had it all ironed out by this February."

As for the reliability of the system, Albo says that "we've produced from 3,000 to 5,000 units since then with the robot and have seen about a 70% up time." He adds, "We expect this to be higher once the equipment is installed in its permanent location." The robot is now in a laboratory at the company's Sunnyvale facility and will be installed at the firm's Roseville, Calif., assembly plant later this year.

When the installation is complete, the firm will have spent about $140,000 on hardware and software, Albo estimates. (The Puma itself is $41,500.) "But we expect the unit to pay for itself within 18 months through higher production output, labor savings, and improved quality," he asserts. **-Stephen W. Fields**

Memories

Dynamic RAMs come out at 4 bits wide

The mushrooming market for small microprocessor-based systems is now claiming a significant portion of worldwide dynamic random-access-memory consumption. Already, most memory suppliers agree the balance of dynamic-RAM usage is swinging from large mainframes and minicomputers in favor of these small systems—which are often personal computers.

For that reason, Texas Instruments Inc. is now unveiling its long-planned 16-K-by-4-bit dynamic RAM. With the new device, designated TMS4416, TI is addressing a worldwide 16-K-by-4-bit market that it expects to surpass $400 million in 1985. Although final pinout approval is pending, the Joint Electron Devices Engineering Council has okayed TI's 18-pin format, which uses bidirectional input/output pins.

Though other chip makers agree that wider-bit formats will be popular, most think it premature to bring such products to market. With 64-K-by-1-bit volumes just beginning to take off, many are reluctant to divert resources from the mainstream chip.

However, TI's leap into the by-4-bit dynamic-RAM era is based on its by-1-bit success, says Richard Gossen, manager of advanced MOS memory development in Houston. To make the new n-channel MOS chip, TI is using the same basic design as in its 64-K-by-1-bit RAM. In 1978, when the part was designed, "hooks" were placed in the layout for easy implementation of the 16-K-by-4-bit organization.

"The point is that we intended all along to use the same architecture, the same circuits, the same sense amps . . . all we had to do is come back in, rip off one end of the bar, add four buffers, and fix it up to where it comes out in ByFour [by 4 bits]," Gossen says. "And regarding the front end, that thing should run very close to the same yields we were getting with the 4164 [64-K-by-1-bit] part."

The extra ByFour circuitry—address lines, buffers, and so on—is costing only 3% more die area when compared with the 35,000-square-mil 64-K-by-1-bit chip. Thus TI can introduce a 150-nanosecond version of the RAM for $20 each in 100-piece lots.

Until now, small-computer designers wishing to use dynamic-RAMs had only by-1-bit formats. An 8-bit microprocessor system would require no less than eight such memory chips. Now that dynamic-RAM densities have reached the 64-K level, personal-computer firms are faced with a minimum dynamic-RAM space of 64-K bytes for 8-bit equipment—more than many applications can initially use. Futhermore, memory sizes would leap by another 64-K bytes.

However, with TI's ByFour organization, memory increments for 8-bit systems would begin at 16-K bytes with two chips, followed by 32-K bytes with four chips, 48-K bytes with six, and so on. This enhancement becomes even more apparent at the 16-bit level.

In addition, TI reports that it is receiving attention from makers of high-resolution, bit-mapped graphics terminals, which need high bandwidths to show detailed images. Because the new chip delivers 4 bits at a time, terminal manufacturers are able to increase the bandwidth of equipment without paying a premium for high-performance 64-K-by-1-bit RAMs.

Elsewhere. To address the changing market, Intel Corp., Santa Clara, Calif., plans to introduce in two months an 8-K-by-8-bit integrated RAM, which includes refresh among its on-chip features. Mostek Corp., Carrollton, Texas, believes the by-8-bit format will make more sense at the 256-K level. Motorola Inc., which led U. S. firms in 64-K RAM volumes last year, is putting more emphasis on its 256-K design, which will address some new market needs with a nibble mode [*Electronics*, March 10, p. 37]. Nibble mode speeds access by spewing out data serially, 4 bits at a time.

In Japan, Hitachi Ltd. indicates it

Price of 64-K RAMs firms up

Prices for 64-K dynamic random-access memories are finally firming up, and persistent 16-K demand is at last showing signs of fading, according to memory-chip manufacturers on both sides of the Pacific. In volume quantities, a 150-nanosecond 64-K part is now running between $6.50 and $8.00 in the U. S. and slightly less in Japan. Last year, they sold for about $10. Also, most RAM manufacturers report 16-K shipments are tailing off, having peaked anywhere between the end of March and June. One Japanese firm, Nippon Electric Co., says 16-K prices have recently even shown slight increases. Although demand is pacing production, most manufacturers do not expect a price rise for the 64-K chip this year.

To meet the surging demand—which is attributed to a combination of strong small-systems sales and the number of large-computer firms ramping up 64-K designs—RAM suppliers are taking on aggressive production schedules. Hitachi Ltd., the current world shipment leader, is planning to boost its 64-K-RAM production rate to 2.2 million a month by December. In contrast, it shipped about 4 million units last year. NEC says it will make over 2.5 million devices per month at year's end. Motorola Inc., the U. S. volume leader in 1981, is expected to fabricate over 2 million units in December while Texas Instruments Inc. intends to hit a monthly rate of 2.2 million in the fourth quarter. Even Mostek Corp., which entered into volume production tion of the 64-K devices only late last year, plans to make over 1 million devices per month in December. **-J. Robert Lineback** will decide in two months whether to offer either a 16-K-by-4-bit or a 64-K device with nibble mode, or both. Fujitsu Ltd.—planning to announce a 64-K part with a nibble mode—is also considering by-4-bit parts. Nippon Electric Co. says it will offer an even wider format 8-K-by-8-bit device in 1983. **-J. Robert Lineback**

Consumer

Home earth stations start to catch on

Despite legal clouds hanging over the home satellite earth-station industry, suppliers of the $2,000 to $12,000 television receive-only (TVRO) systems are projecting a sunny 1982 sales picture. Estimates vary widely, but the 13 suppliers who exhibited the backyard dish systems and components at this month's Consumer Electronics Show in Chicago expect sales of between 30,000 and 60,000 units this year, up from 10,000 to 20,000 in 1981.

Biggest demand for the private satellite terminals comes from rural areas where cable television service is not available or where TV reception is poor. Using a parabolic dish 9 to 12 feet across with a low-noise amplifier, microwave receiver, and TV channel modulator, a TVRO system can tune in on some 60 channels taken from TV signals beamed to earth within the 3.7-to-4.2-gigahertz band by relay satellites. The launch of additional birds over the next 12 months will boost total available channels to over 100, suppliers say.

The low-noise amplifiers used in the stations generally employ gallium arsenide field-effect transistors with typical gains of 50 to 53 decibels over the bandwidth. Noise ratios range between 1.05 and 1.5 dB.

Classier. The higher-priced station typically includes a superior amplifier or a bigger or better dish, or all three. A dish of spun aluminum, instead of fiber glass, for example, affords higher gain and, according to General Instrument Corp.'s RF Systems division, in Sherburne, N. Y., could receive the 12-GHz signals from satellites in the offing (see "Direct-broadcast satellites due by mid-1980s," below). Aluminum dishes, the firm claims, also offer higher directivity that could still separate signals even if the Federal Communications Commission decides to place satellites with 2° orbital spacing, instead of the present 4°. (Some makers of fiber-glass dishes also claim this capability.)

The higher-priced systems also include more bells and whistles, of course, such as an automatic motor drive for tracking a satellite (comparable with a hand crank), preprogrammed channel selection, and a handheld infrared remote controller. GI even has what it calls a parental lock-out control, which Mom and Dad can use to stop kids watching a particular channel.

Since 1979, when the FCC deregulated private reception of satellite TV broadcasts [*Electronics*, Dec. 20, 1979, p. 12], about 45,000 private earth stations have been sold in the U. S., says Richard Brown, vice president and general counsel for Space (for Society for Private and Commercial Earth Stations), a Washington, D. C.-based trade group. The growing number of dishes have elicited protests from pay TV services, which charge that unauthorized reception of their signals, especially by entrepreneurs who then sell the programs, is piracy.

Though no major litigation has been filed, says Brown, wrangling over the legality of backyard dishes continues. Three bills affecting the issue are pending in Congress. In addition, the Home Box Office unit of Time Inc., the biggest user of satellites for sending TV programs around the U. S., plans to spend more than $6 million to scramble its signal by late this year or early next to deter private reception.

Earth-station suppliers concede that unanswered questions of the legality of the private dishes may be slowing system sales. There is also some concern that scrambling by HBO could lead other pay services to do likewise. But exhibitors at the electronics show were quick to point to strong and growing sales levels. Indeed, says Guy C. Davis, sales vice president for Intersat Corp., St. Peters, Mo., the industry could be capacity-limited this year by the number of low-noise amplifiers available.

New products were abundant at booths of the 13 companies at the CES show. The Channel Master division of Avnet Inc., Ellenville, N. Y., for example, exhibited new models priced from $4,500 to $6,000. As

Direct-broadcast satellites due by mid-1980s

Sales of home satellite earth stations are spurting now, but the market for the current crop of television receive-only systems will be short-lived due to the advent by mid-decade of lower-cost direct broadcast satellite (DBS) technology. That is the view of Kenneth G. Bosomworth, president of International Resource Development Inc., a Norwalk, Conn., market-research firm (see "DBS people are talking money," p. 92).

DBS programming will be beamed on the 12-gigahertz band, allowing reception by systems employing only a 2.5- to 3-foot-diameter dish and selling for only $300 to $500. Bosomworth believes the market for current home TV receive-only systems will peak at about $150 million annually in 1983 before tailing off as DBS systems become available. "For small companies, [the current market] is a great market to be in for a few years, but there's not much there for the large companies," he contends.

Differing, however, are officials at large firms such as Avnet Inc. and General Instrument Corp. Both have recently introduced private earth stations. "TVRO will not be a mass market like DBS, but we think it will be a continuing market," says Douglas A. Skinner, marketing director for GI's RF Systems division in Sherburne, N. Y. He notes that current GHz downlink satellites have a life expectancy of 10 years, adding that, by 1986, TVRO viewers will have available some 400 channels. **—W. R. I.**

Backyard display. Some 13 exhibitors showed off their home-satellite earth station equipment at the Consumer Electronics Show earlier this month. Seen here are the 9- to 12-ft parabolic dishes that receive TV signals being relayed to earth by broadcast satellites.

others are doing, Channel Master in August will add the ability to receive stereo sound, thanks to a new $349 adapter from another show exhibitor, R. L. Drake Co., Miamisburg, Ohio. **-Wesley R. Iversen**

Software

Single format adapts disks for p-code

Variations in disk formats have long vexed software distributors, who have to carry a different version of an application package for each computer system. To overcome this problem, SofTech Microsystems is developing a utility package now working with a prototype format that lets customers for SofTech's UCSD p-code operating system (especially designed to be processor-independent) use the same 5¼-inch diskette on divers machines.

The concept, called the Universal Medium by the San Diego, Calif., subsidiary of SofTech Inc., Waltham, Mass., combines the utility package with the portability of p-code to create programs that can run on nearly any machine without rewriting or reformatting. (In particular, SoftTech uses the object code of p-code, version 4.)

"The Universal Medium brings home what portability means. Our p-code makes this an engineering task instead of a massive programming effort," says Mark Overgaard, manager of advanced development. Distributors see it as a marketing boon that should popularize the p-system. "The effect could be as great as having p-code to sell in the first place. Distributors can stock less, and dealers won't worry about different versions and can carry more programs, benefiting end users," says Robert Leff, president of Softsell Computer Products Inc., an Inglewood, Calif., distributor.

Greatest number. The Universal Medium requires that software be encoded onto double-density disks in SofTech's format, which is still being finalized. The eventual format will be that which can be read by the greatest number of machines, Overgaard says. Aspects being considered include the number of tracks and sectors and bytes per track.

The utility package, or adapter, takes advantage of the configurability of most disk controllers, reprogramming them to read in the SofTech format instead of the natural format of the computer system to which they attach. As the application package is copied into main memory, alterations are made to convert it into the machine's format.

Because every computer-based system has a unique format, SofTech must write versions of the adapter, which runs only to a few hundred lines, for each. Prototypes shown this month in Atlantic City, N. J., at the Comdex spring conference for computer and peripheral makers run on the IBM Personal Computer, the Apple II, and computer systems based on the Z80 and 68000 microprocessors. SofTech expects to finalize the format and develop versions for more systems by the end of the year, Overgaard says.

Even competitors applaud this move toward greater portability. "It can only be positive for the industry," says Nigel Smith, manager of product marketing at Microsoft, the Bellevue, Wash., developer of the MS-DOS operating system used in the Personal Computer.

Debate. However, the probable effect on the market is arguable. "Software needs to be packaged so it's user-friendly, with documentation, instructions, and the rest. Once you go to that effort, making the disks in various formats is trivial," says Gordon Eubanks, vice president of language development at Digital Research Inc., Pacific Grove, Calif. Digital Research developed CP/M, the popular operating system for 8-bit machines.

Overgaard counters that any trimming in alterations is positive. Price is not yet set, but he feels this will be no obstacle. "We hope it will be available from manufacturers at a nominal charge. We'll do our best with the licensing policy to make it possible," he says. **-Terry Costlow**

Components

Conference spans supply design issues

Riding the crest of faster and more efficient components, power-supply design is turning to compact systems that provide clean characteristics at ever higher efficiencies. Powercon 9, the Ninth International Solid-State Power Electronics Conference and Exhibit, will be highlighting the state of the art in power-supply configurations and products at its meeting in Crystal City, Va., beginning on July 12.

The five-day series of sessions, hands-on product demonstrations, and all-day seminars has a number of papers dealing with the most pressing problems in systems design today, says Ronald I. Birdsall, president of Power Concepts Inc. The Ventura, Calif., consulting firm is sponsoring the event.

"The main attractions are not only designs to solve old problems like efficiency, but also new configurations that deal with the problem of making the supply clean enough to work in a systems environment," says Birdsall. One of the worst problems encountered in systems design—and one that can seriously degrade digital systems—is the switching noise that is introduced on the input line by switching power supplies.

As switching power supplies regulate their output, they continually interrupt the current at the input. "This switching generates an input-current ripple that is one of the major causes of most electromagnetic interference problems," notes Birdsall.

Clean supplies. A session on new converter configurations includes papers on just this problem. Brian Attwood, a consultant in England on pulse-width-modulation applications, will describe a technique that optimally couples waveforms with a supply's power components. Varying the amplitude and shape of the fundamental waveform plays a central role in Attwood's design. The resulting system reaches an efficiency of above 90% for switching power supplies of up to 400 volts at 500 kilohertz with power loads to 1 kilowatt.

An alternate approach to the problem of clean switching power supplies will be presented by M. J. Kocher and R. L. Steigerwald of General Electric Co. in Schenectady, N. Y. Though conventional switching power supplies use pulse-width modulation to regulate against the output, this design regulates with respect to the power waveform on the input.

The converter is modulated so that the input current varies sinusoidally rather than in the usual pulsing pattern, resulting in less ripple on the input line. In fact, the sinusoidal input current is sufficiently pure that its highest harmonic—the third—is 35 decibels down from the fundamental waveform. Though this input current control results in a slight efficiency penalty, the advantage of the design, besides the clean input, is its relative simplicity, according to Birdsall. -Stephen Evanczuk

Solid state

Restructurable IC turns tricks for VLSI

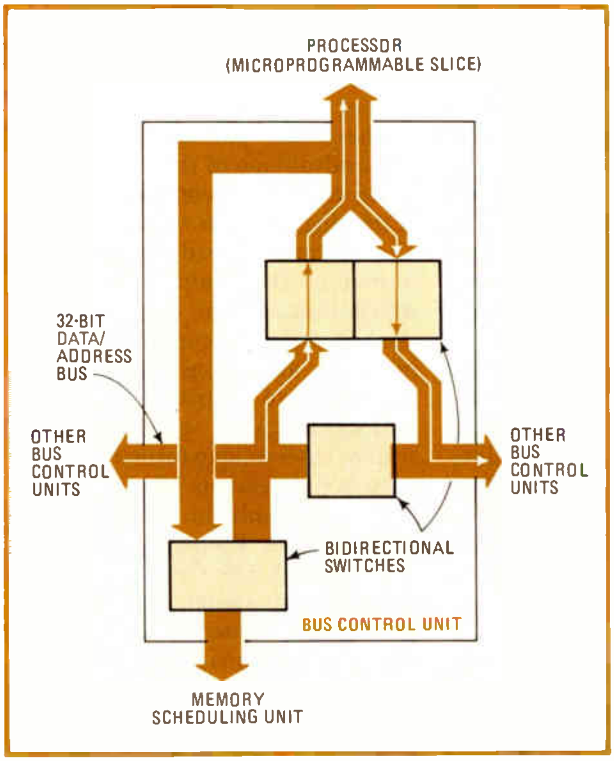
The wisdom of the marketplace has it that the more complex a chip is, the fewer will be sold. Consequently, both yield and reliability stay low because production volumes stay low.

Thus for very large-scale integrated circuits, the most economical answer may be a single complex circuit that could be reconfigured, or restructured, to suit a variety of tasks. Such an idea for a high-volume VLSI product has been kicked around on paper for several years at Texas Instruments Inc.'s Central Research Laboratory in Dallas. Now, key hardware experiments for what TI calls its restructurable integrated circuit, or RIC, are under way.

The ultimate goal is a single chip of some 80,000 square mils, comprising four 16-bit microprocessors, says TI researcher Rob Budzinski. Also on board, he adds, will be four modules of 64-K dynamic random-access memory and a read-only memory. The ROM will hold microprograms for managing the on-chip RAM and setting up connections among the processors.

A bus-control unit, having pass transistors in bidirectional switches, would channel the flow of data and instructions among the processors in the RIC. A program stored in ROM or external RAM could specify how the processors, called microprogrammable slices, would be connected, either in parallel, in a pipeline, as independent units, or in some combination.

The figure illustrates the data path through a bus control unit for data transfer in a pipelined mode. Each processor has access to the 32-bit combination data-address bus through its control unit. The bus controllers are at the center of the chip's restructurability. They allow, for example, one processor to hand data to the next, to request data from its own or another processor's memory-scheduling unit, or to gain access to external memory.



Director. The bus-control unit in TI's restructurable IC routes data and address signals among processors and memory modules through bidirectional switches. Arrows show the path for a data transfer between pipelined processors.

One possibility is to configure the four processors as two pipelined 32-bit units—one would fetch instructions from the ROM, and the other would execute them. TI studied this configuration as a way to implement the instruction set of Digital Equipment Corp.'s VAX 11/780 minicomputer. According to Budzinski, "using the 20-nanosecond clock cycle measured on our prototype chips, our simulations show that one RIC can achieve about half to three quarters the performance of a VAX."

The flexibility of a RIC chip and its ability to satisfy a range of system requirements is key to this single-chip VAX. Half the time, the 32-bit processor that fetches instructions from ROM is split up into two independent 16-bit units to perform other tasks, Budzinski points out.

Assignment. A typical RIC application might exploit this flexibility by assigning one processor to act as the host processor and connecting others for different tasks, such as input/output processing or high-precision arithmetic.

Budzinski expects to see silicon in the next six months on a memory-test chip. "Based on our results with prototype chips in a 1-micrometer n-channel MOS process, we have gone ahead and finished the mask designs for a chip that will test the RIC's memory subsystem," says Budzinski. The design includes a 40-bit processor, a 10-K ROM, and a programmable logic array that implements a test routine for a 2-K static RAM. "The next step will be to integrate two of RIC's four processors," he says. **-Roderic Beresford**

Communications

Western Union delivers more . . .

The same day—June 15—that American Telephone & Telegraph Co. introduced its new added-value services for computer intercommunications through its American Bell Inc. subsidiary (see p. 88), Western Union Corp. was making its own announcements down at the electronic-mail end of the spectrum. By redesigning its computer programs and interfaces, the communications common carrier from Upper Saddle River, N. J., introduced the Access system, a network "that interconnects virtually all hard-copy business-communications systems."

So far, the system accepts both asynchronous and bisynchronous input from 56 types of terminals from 40 makers. Messages can take the form of any of Western Union's services: Telex, TWX, telegram, Mailgram, Cablegram, computer-generated letters, or the U. S. Postal Service's new E-COM messages.

Processing is handled by the company's computer centers in Middletown, Va., and Bridgeton, Mo., and by its subsidiary, Western Union Electronic Mail Inc. of McLean, Va. In January, WUEMI began handling the electronic computer-originated mail (E-COM) service. Distribution is via Western Union's network of Westar satellites, earth stations, and 10,000 miles of 9,600-bit-per-second microwave links. Speeds at which Access accepts ASCII-coded data are 110, 300, and 1,200 b/s. Messages can be stored for delivery as long as three days later.

Word processing. A few days earlier, Western Union also announced an agreement with West Germany's Ministry of Posts and Telecommunications to offer Teletex, an international standard for communicating word processors. Siemens AG of Munich, West Germany, is producing the digital switching equipment, which is being installed in New York. Siemens and at least a half-dozen other European companies make terminals compatible with Teletex, and Tom Mattai, ITT's vice president of office message services, expects "quite a few American manufacturers to join the fray." Transmission is at 2,400 b/s, almost 50 times standard Telex speed. Output is in a letter format, generally on a high-quality printer.

Western Union plans to offer Teletex, a circuit-switching system, in the U. S. this fall, following links between the U. S. and West Germany. However, ITT World Communications Inc., New York, for one, also plans to interface with the West German system, as well as with others like the packet-switching one planned for the UK, according to marketing vice president Bob Olson. Like other international carriers, ITT also is beginning to offer its data and message services domestically. **-Marilyn A. Harris**

. . . as public radio readies data service

National Public Radio plans to tap the burgeoning data communications business in its drive to become independent of Federal financing. This month, NPR formed a joint venture with National Information Utilities Corp. to utilize subcarrier channels in NPR's frequency-modulated broadcast network for "last mile" distribution of data to business and home subscribers throughout the U. S. Ordinarily, such final links are carried over telephone lines; the fm subcarriers can do the job at savings up to 50%, NIU maintains.

The new company, called INC Telecommunications (for Information Network Corp.), is based on a concept of NIU and its principal owner, Jack Taub, who founded The Source, a data bank serving personal-computer users. The Washington, D. C., venture expects to offer subscribers everything from business newsletters and data to video games. Assuming Federal Communications Commission approval this summer, INC Telecommunications plans to begin operations by mid-1983 after six months of tests in the Washington-Baltimore area.

Transmission will be via digital signals broadcast at a rate of 9,600 bits per second to a user's black-box decoder from local NPR stations or other fm stations where NPR does not operate. NPR feeds its 267 local member stations via the 17 uplinks and over 200 downlinks it has available on 12 leased satellite communications channels.

Approvals. Before operations can begin, however, the FCC must approve NPR's petition to allow commercial use of subcarriers by the nonprofit network. Additionally, the commission must reduce the 50-kilohertz separation between each fm signal allocation. To prevent interference, broadcasters now use only 150 kHz of the 200 kHz allocated to each station. Finally, the FCC must also permit digital transmission on the subcarrier bands that will become available by reducing the signal separation. -Ray Connolly

Microprocessors

Rockwell breaks into C-MOS

An all-out plunge announced by Rockwell International Corp. into complementary-MOS technology is shaping up to be a more ambitious undertaking than merely copying its existing 6500 family of 8-bit n-channel MOS microprocessors. "We are working on brand-new designs that fully use the other C-MOS advantages besides low power—largely those that permit laying out more functions in an equivalent area than n-MOS," says an official of the company's Electronic Devices division.

Rockwell has successfully pushed the 6500 family, under license from MOS Technology Inc., Valley Forge, Pa., to a top design-in spot among 8-bit processors. But this n-MOS sector has proven a dog-eat-dog niche where profits are hard to come by. C-MOS offers an enticing prospect, since there is a dearth of products to meet what has become a zooming demand for low-power processing.

Starters. At present, however, the Anaheim, Calif., division's priority is to get C-MOS products out the door quickly [*Electronics*, June 16, p. 42]. So the first one—the 65C02 four-chip set—stays fairly close to its n-MOS counterpart, although its specifications highlight the advantages of C-MOS. Die size of the microprocessor itself, for example, drops to 19,000 square mils from 21,000 $mils^2$ in n-MOS. Also, some 27 new instructions are squeezed in, and there is room for an internal crystal and a quadrature clock, among other options not possible in n-MOS.

Low power dissipation further underscores C-MOS's potential. The processor uses just 20 milliwatts per megahertz (with top speed now set at 4 to 5 megahertz), as against 700 mW for the 1-to-2-MHz and 800 mW for 3-MHz n-MOS versions. Random-access memory speed stays the same 170 nanoseconds. The 65C02 is in fabrication, with samples due in September.

But "the really spiffy stuff on the drawing board," as one Rockwell engineer refers to it, will include one-chip microcomputers planned for next year. This 65C20 family will bear little resemblance to the n-MOS line. Rockwell says a pipelined architecture "lays out nicely," making possible dual on-chip processors that share register space.

The C-MOS effort has taken under than one year, since division president A. G. Lapierre came to Rockwell from National Semiconductor Corp. Rockwell's Microelectronics Research and Development Center, Anaheim, Calif., with long experience in military C-MOS is handling the first phase of fabrication for the commercial line. Production will be carried out in a new $25 million facility in Newport Beach, Calif., that will handle 3-micrometer-wide line widths.

As to a technology exchange with NCR announced in March, Lapierre terms it more "a product partnership than an exchange." No process data or masks are changing hands; instead, Rockwell is trading its proven read-only memory designs in n-MOS for C-MOS random-access memory, a 16-K static version first. NCR also is producing an advanced C-MOS one-chip microcomputer that Rockwell will build. Each will act as the other's second source.

But the challenge facing Rockwell, say industry veterans, is not only holding to a tight schedule with a new process, but convincing prospective customers it intends this time to stay the course. Skeptics note that the division often in the past decade launched bold initiatives, as in magnetic-bubble memories and n-MOS, only to give up on them.

New regime. Something new this time for Rockwell is that the top management of its semiconductor enterprise does not appear to have been raised by Rockwell in house on military programs. Many have been recruited from Silicon Valley. Howard W. Cotterman, vice president for microcomputer products, for example, is from Intel Corp.

That the C-MOS market is hot is confirmed by actions at both Motorola Inc.'s Semiconductor Sector and Intel. Motorola's 14680E2 line, its C-MOS offering of the one-chip 6805, even at a healthy premium price is selling so briskly that "shelves presently are clean," says a spokesman. The Austin, Texas, division is working to expand the line, available since late 1980.

At Intel's microcomputer operation in Chandler, Ariz., which will be taking the firm's C-MOS initiative, first product samples are due in July of the 80C8049 controller, a single-chip microcomputer. Both firms are watching Rockwell's efforts closely, they say. -Larry Waller

News brief

Bell builds Josephson parallel multiplier

Using a basic switching circuit consisting of two Josephson tunnel junctions and a small resistor in a loop, Bell Laboratories in Murray Hill, N. J., has successfully fabricated an 8-by-12-bit multiplier—the largest Josephson-junction circuit to date. The circuit uses 548 junctions in the two-junction Josephson Atto-Weber Switch (Jaws) configuration, which was developed at Bell Labs [*Electronics*, July 19, 1979, p. 42].

Built on a silicon substrate, the seven-layer circuit uses line widths of 10-micrometers for the wiring and junctions, with 2.5-μm line widths for some resistors. Though the 30-nanosecond delay between input and delivery of the most significant 13 bits of the output is fast enough for the intended application of the device, Bell researchers say that they could realize a factor-of-10 improvement in speed by accepting the cost of about three times as many gates per adder. The circuit is to be used for a video-data-compression experiment being carried out at the labs.

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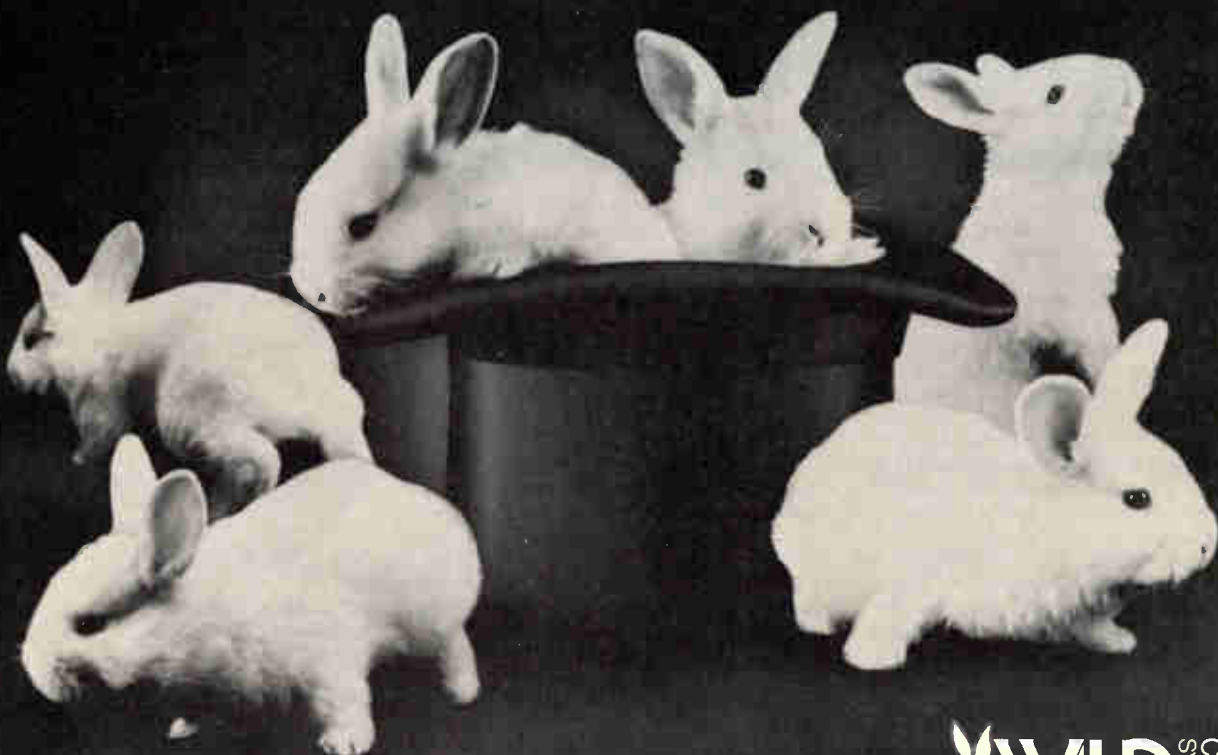

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FBI briefing firms on protection against industrial espionage

Increased efforts by U. S. electronics companies to protect their designs from growing industrial espionage are being carried out in cooperation with the Federal Bureau of Investigation, says Peter McCloskey, president of the Electronic Industries Association. EIA members have taken up the FBI's offer to provide them with special agents to brief them on how to protect themslves against having their technology stolen by competitors, McCloskey says, **"and the companies have been chilled by what they have heard."** Carefully distinguishing between the outright theft of designs and the overseas sale of products that may then be reverse-engineered (a lengthy process), McCloskey hopes that the alleged purchase of IBM computer designs by Japanese firms may "prove psychologically reassuring to some of those people [in the U. S.] who think that the Japanese are 10 feet tall" when it comes to technological competition.

NEC to be assessed charges for dumping

Nippon Electric Co. has lost its defense against charges by Aydin Corp. of Fort Washington, Pa., that the Japanese company has been **selling high-power amplifiers at less than fair value to Communications Satellite Corp.** [*Electronics*, Sept. 8, 1981, p. 57]. The 4-to-1 ruling by the International Trade Commission means that NEC will have to pay penalities of 25% to 40% on the estimated $3.5 million in amplifiers sold in the U. S. and used to send signals to communications satellites.

Space Command to become a triservice unit

The Air Force Space Command, set to begin operations on Sept. 1 at Colorado Springs, Colo., is expected to become a triservice effort under Air Force direction. The new command will take over operations of the Aerospace Defense Center at the Colorado site, which works in conjunction with the North American Aerospace Defense Command. Norad's present commander, Gen. James Harringer, will head the new command, beginning with a planning staff of 200 to be transferred from the Strategic Air Command, Offutt Air Force Base, Neb. Candidate contractors for the new command, however, **are focusing their attention on the new Space Technology Center being set up at Kirtland Air Force Base, N. M.,** which will be responsible for developing military weapons systems and space payloads, including satellites for military communications, surveillance, warning, and weather. The new STC, which will direct efforts at Air Force laboratories in California, Massachusetts, and New Mexico, will work closely with the Space Command. Both will be part of the Air Force Systems Command.

Addenda

The Semiconductor Industry Association is expected by North Carolina officials **to locate its recently formed Semiconductor Research Cooperative in the state's Research Triangle Park** and thus increase the place's appeal to electronics companies. SRC executive director Larry W. Sumney made no comment on the North Carolina report. Other sites being considered include Colorado Springs, Minneapolis, and Phoenix. . . .The International Trade Commission has voted unanimously to recommend that the U. S. bar imports of electronic games that infringe on the copyrights and trademarks of Pac-Man. The action was taken on the petition of Midway Manufacturing Co., Franklin Park, Ill., which charged that **Japanese suppliers have copied and sold the game in the U. S.**

Washington commentary

Small-business R&D: the costs to come

Companies with fewer than 500 employees are about to be guaranteed by law a share of Federal research and development funds. All that remains to be done is for a House and Senate conference committee to compromise on the small differences between the bills passed in each chamber and for President Reagan to sign the final version into law. As indicated nearly a year ago, it will be premised on a desirable concept that is likely to be poorly implemented [*Electronics*, July 28, 1981, p. 58].

Under the mandate, all Federal agencies with annual R&D budgets of more than $100 million except the Department of Defense will be required to set aside 0.2% of their funds for small-business awards in the next fiscal year. The small-business guarantee will gradually rise over four years to 1.25% and stabilize at that level. For the Pentagon's much larger R&D budget, the small-business share will begin at 0.1% in the first year, rising to 1.25% in the fifth and future years. That was one concession won by the bill's opponents who fought against larger percentages. But the percentages do not make the principle any more palatable.

Problems of enforcement

President Reagan is expected to sign the law despite the fact that it will further enlarge the Federal bureaucracy that he has promised to reduce in order to limit the Government's role in the lives of its citizens. Why? "You can't vote against small business—that's like voting against God and Mother," says one Administration aide. "Congress didn't put the bill down; neither will the President." He goes on to note that the legislation got its start in the Senate on the initiative of two Republican members.

The prospect that the new law will be poorly enforced seems likely because just about every agency with significant R&D funds opposed its passage. Among them are DOD, the National Aeronautics and Space Administration, and the Department of Health and Human Services. Also opposed to the bill were Congress's own auditor, the General Accounting Office, as well as the Small Business Administration, which indicated it has neither the staff nor the expertise to monitor compliance by individual agencies. The nation's universities and colleges opposed passage also, but for different reasons: academia sees the law as eating into its share of diminished Federal R&D funds.

Nevertheless, like it or not, the nation must now live with the law. Besides, there is some truth to the complaints of small companies that they have been left on the outside looking in when contracts for Federal R&D are passed out. Now such firms have the law on their side. What many of them have yet to realize is that they must make it work.

That work will entail lawyers and lobbyists charging fees that seem certain to surprise the small innovator. The small company will be obliged to keep track of available contract set-asides and then go after them by completing and filing the many complex documents that are required of Federal contractors. On winning an award, the contractor will then be required to report periodically on the program's progress. The true innovator may then find the product of his labors made license-free for use by the Government, which may decide to share production of the product with a competitor to hold costs and profits down.

The price of waste

In short, as in almost every other set-aside program, there will be waste. Funds as well as labor will be wasted by both industry and Government as they try to conform to the new law. Surely there will be court challenges by companies small and large as the legal community looks for loopholes to fit its own interpretations. Lawyers will profit, but innovative engineers and scientists obliged to pay the legal fees could easily not do so.

Advocates of the new law are delighted that they will now get their "fair share" of Government R&D monies. They have yet to learn that they will also get perhaps more than their fair share of grief. And it seems that a majority of both the House and Senate remains ignorant of the rule that a guarantee of money cannot guarantee good R&D by contractors, whatever their size may be.

Without enough applications by enough small companies, money is sure to be wasted by agencies determined to spend their annual appropriations. The fact that these funding guarantees will be phased in gradually is perhaps the best thing that can be said about the new law to promote innovation by small business. Whether the law helps the nation in its global competition or becomes just one more special interest boondoggle remains to be seen. **-Ray Connolly**

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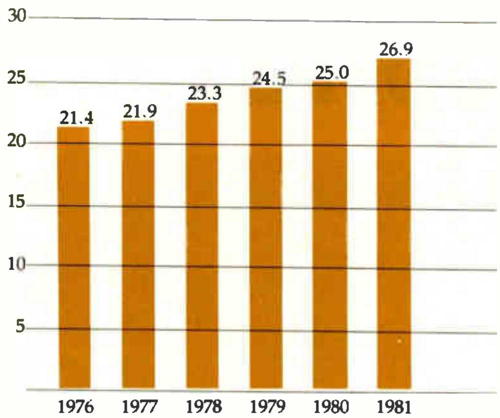

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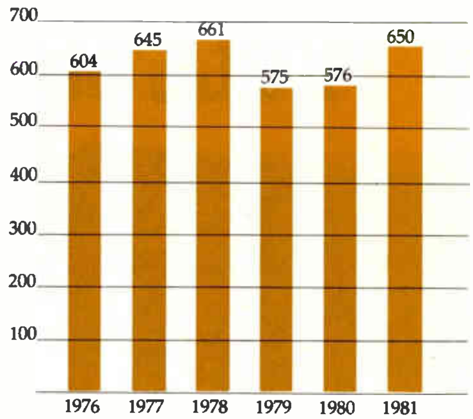

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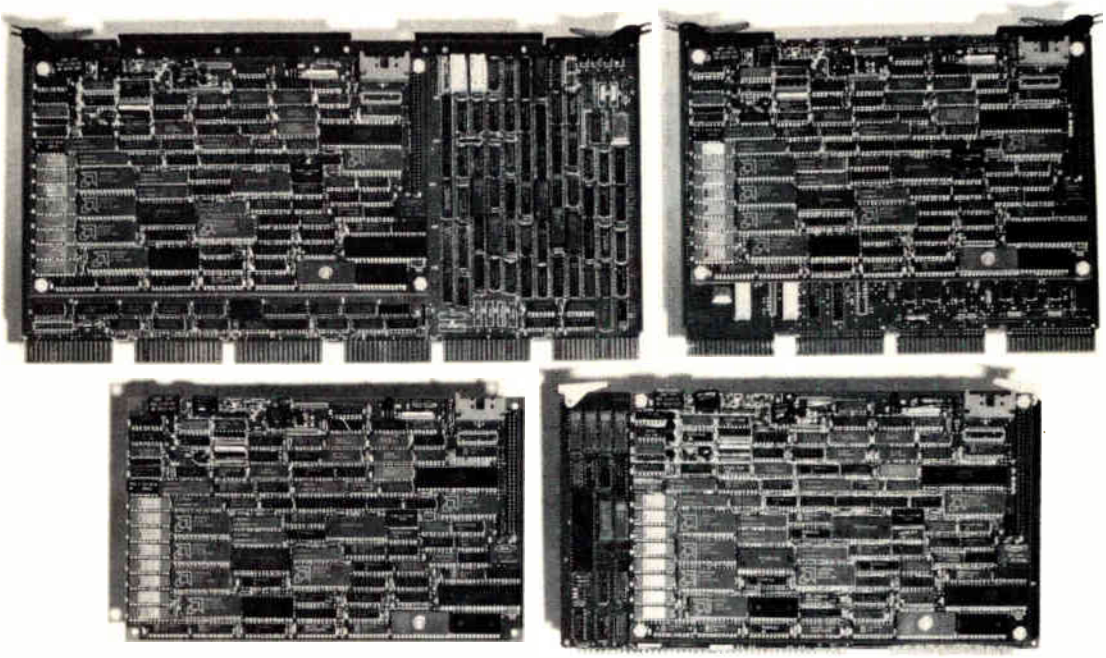

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NTT begins converting phone system into information network

The first part of a $19.6 billion plan that will convert Japan's telephone system into a digital "information network system" by 1995 has been released by Nippon Telegraph & Telephone Public Corp. A fiber-optic digital communication link will be installed between Sapporo on the northern island of Hokkaido and Fukuoka on the southern island of Kyushu—a distance of about 1,200 miles. The NTT project will **implement a rapid change from analog to digital technology that will combine voice transmission and information processing.** Also in the plan is the switch from analog to digital exchanges and more use of communications satellites, the first in a series of which was launched this year.

Static RAM from NEC has 25-ns access time

Japan's Nippon Electric Co. has given its 2147 4-K-by-1-bit static n-channel random-access memory low-resistance interconnections and also shrunk it, so as to decrease its access time to 25 ns. Texas Instruments, Intel, and Hitachi currently have 35-ns parts. In the revised 2147, two levels of aluminum interconnections lower the resistance of both bit and word lines. Also, a transistor design with an effective channel length of only 1.6 μm makes for faster switching and helps keep chip size to 3.2 by 4.21 mm. **The higher speed is achieved without increasing power consumption—at most 880 mW** during operation and 110 mW during standby. The device will sell in Japan for $12 each in lots of 5,000.

Direct-coupled FET logic makes GaAs VSLI possible

By switching to direct-coupled field-effect-transistor logic (DCFL) for their gallium arsenide circuits, engineers at the Thomson-CSF Central Research Laboratory in the Paris suburb of Corbeville seem to have bridged the gap between GaAs and very large-scale integration. Thomson used the same technology, but with low-pinchoff-voltage FET logic, to produce the world's fastest circuit at room temperature [*Electronics*, Dec. 15, 1981, p. 81]. The engineers find that DCFL **far exceeds their requirements for GaAs VLSI of a maximum propagation delay and power dissipation of 100 ps and 100 μW per gate, respectively.** With a gate length of 0.7 μm, the company achieved a propagation delay of 32.5 ps at 62 μW.

Enhanced software offered by Fujitsu for its M-380 computers

To enhance its competitive position against IBM's growing 3081 series, Fujitsu Ltd. has announced a new operating system and step-down versions of its M-380 series computers. **The OSIV/F4 MSP features the same 2-gigabyte virtual-memory address space available from IBM,** but not from other firms offering IBM-compatible software. Other software enhancements include a 2-gigabyte version of Fortran 77 and the AIM/RDB (advanced information manager-relational data base) having the same large addressing capability. The hardware has been enhanced by adding disk cache memory. Thus, Fujitsu has evidently achieved some of what Hitachi is accused of trying to illegally purchase (see p. 41).

Government approval expected for UK VHPIC program . . .

Britain's Royal Signals and Radar Establishment wants top priority for a project **to develop integrated circuits with data throughputs two orders of magnitude higher than in present-day components.** The five-year very high-performance integrated-circuit project, or VHPIC—reportedly costing $90 million—is expected to receive government approval within two months. RSRE says the circuits are essential to tomorrow's intelligent homing missile systems, adaptive radars, and so on, and it therefore mapped out a program that, like the corresponding U. S. very high-speed IC (VHSIC) program, is tied to so-called systems demonstrators, or military systems incorporating the new chips. The industry-funded program will span very large-scale IC lithography and complementary processing techniques, design methodologies, and advanced chip architectures.

. . . and RSRE stresses new architectures

Aside from submicrometer lithography and fine-line processes, new processor architectures will also be developed by the RSRE. For hardwired systems, **one candidate is the systolic array because it permits a generalized design approach to signal-processing tasks.** Such an array comprises a parallel array of identical processors that can be readily interconnected and replicated to match the task in hand. Early systems were word-oriented, but to permit integration at the chip level, the RSRE has in the works a demonstration convolver based on its patented 1-bit–level architecture. For high-performance airborne computing in radar and sonar image-processing applications, London-based International Computer Ltd.'s distributed-array processor—already used by the RSRE to model systolic arrays—is being considered. A miniaturized VHPIC version may be funded. Some of this work would likely mesh with the British fifth-generation computer program [*Electronics*, Feb. 10, p. 71].

Motorola to challenge 4-bit market with an 8-bit chip

Motorola Inc. will bid to take over a significant portion of the 4-bit microprocessor market next year, but with an 8-bit circuit. Designed at the company's European headquarters in Geneva, **the high-performance complementary-MOS variation of the 6805 will be integrated on a chip the size of a 4-bit microprocessor** and is to sell in the 4-bit price range, though it will feature 70% to 80% of the throughput of the parent circuit. Motorola hopes to have the circuit available early next year.

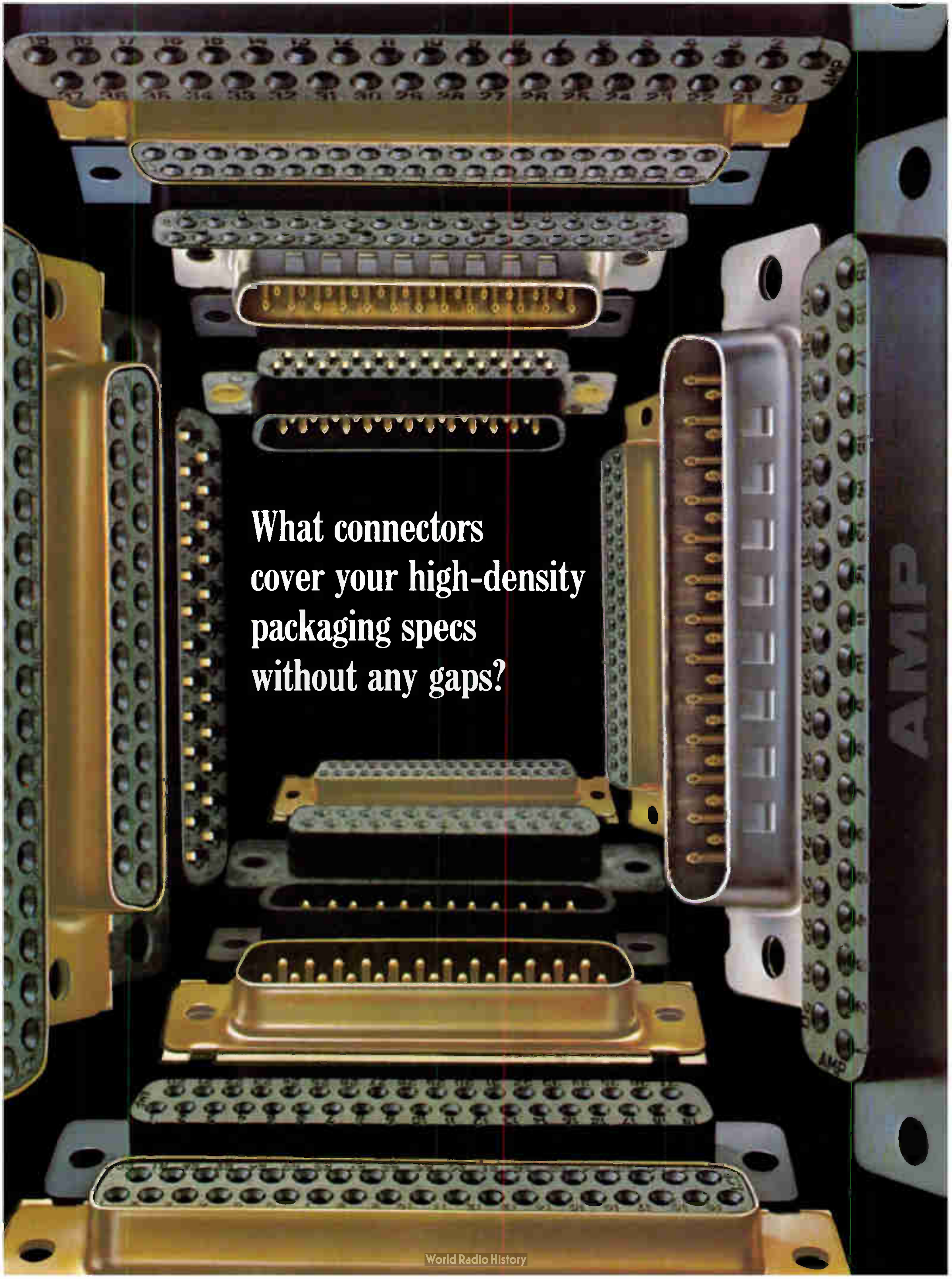
Computerland lands in Japan, Apple to follow with subsidiary

Kanematsu-Gosho Ltd., a large Japanese trading company, will establish in July a joint venture with the U. S. firm, Computerland, to sell Japanese personal computers franchised stores throughout Japan. **The company's plan calls for 30 outlets by next March and 250 within five years.**

Japanese personal computers will surely face increased competition from Apple Computer Inc. William J. Schonfeld, manager of Japanese operations of Apple Computer, says that the firm will open a wholly owned subsidiary completely staffed by Japanese within three months. Initally, it will import computers from the parent company and distribute them through its present sales channels.

Addenda

Ing. C. Olivetti & Co., Ivrea, Italy, has sold 2,000 of its new Z8000-based M20 personal computers after in the first three weeks of marketing in the U. S., **half their goal for the entire year.** . . . The same company says that its evaluation program shows that **the clear edge held by Japanese suppliers of integrated circuits in 1980, when the program began, no longer exists** and that the quality and reliability of U. S.-produced ICs are now at an equal level.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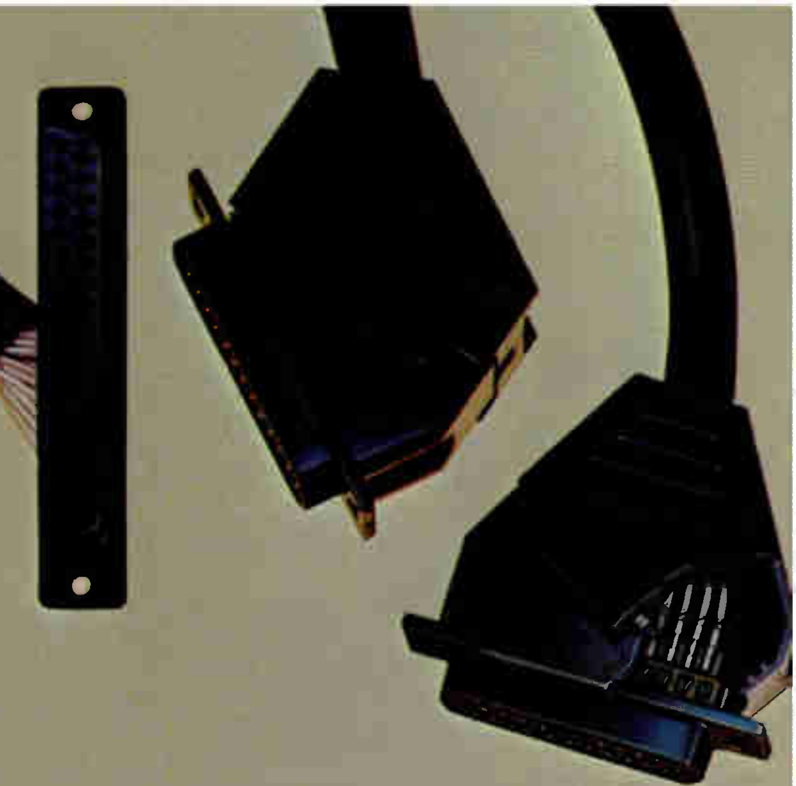

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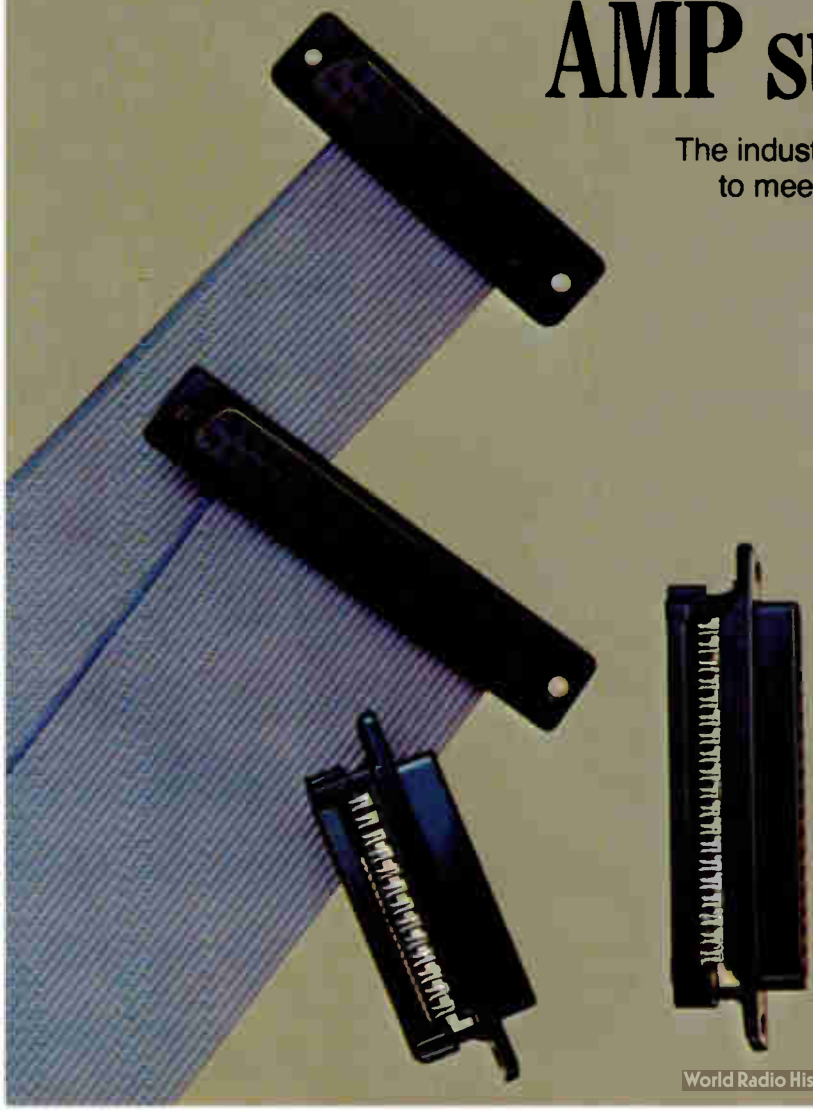

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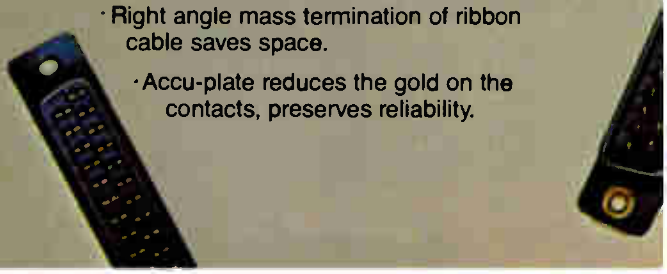

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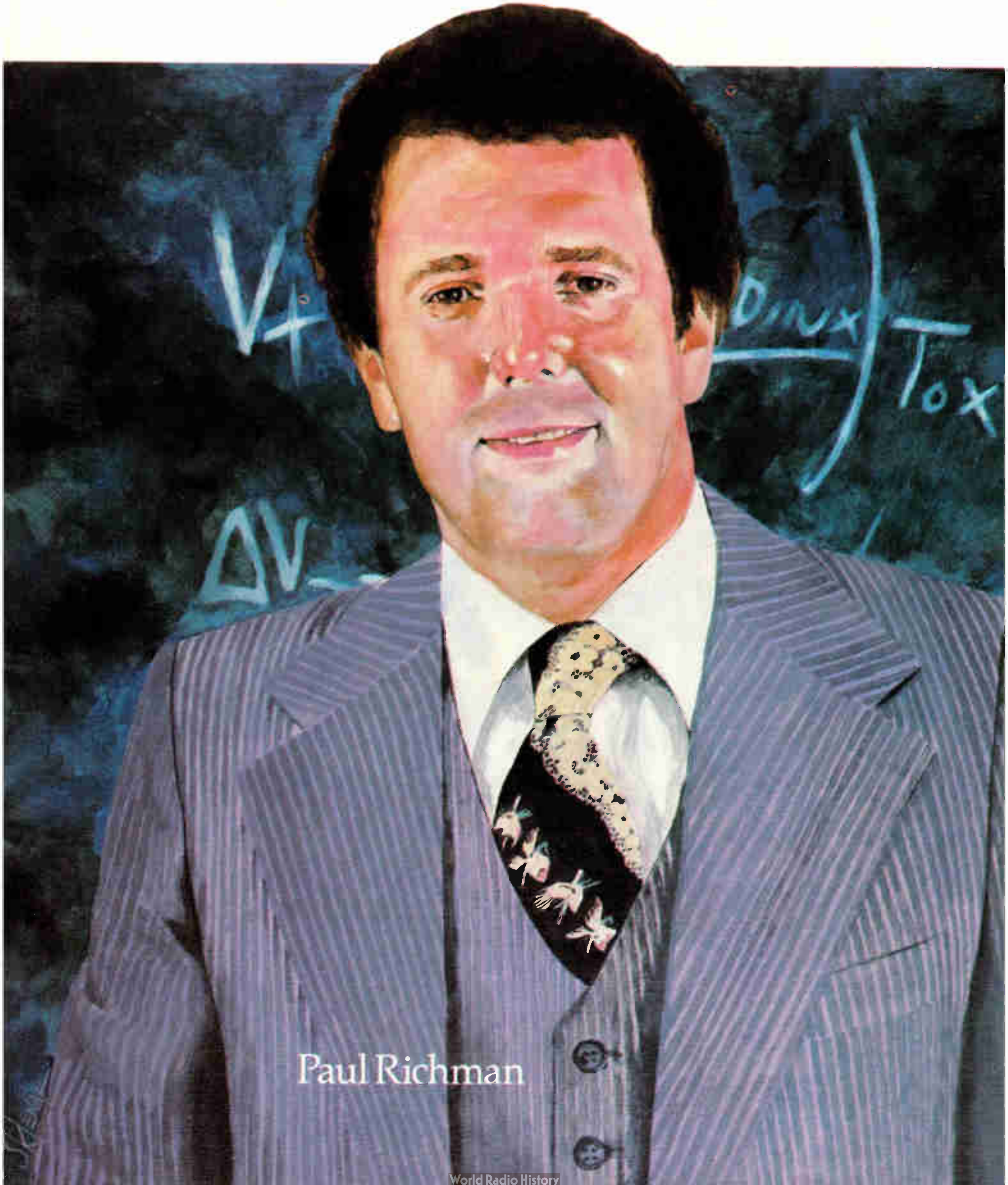

Paul Richman

read important editorial

Paul Richman, creator of Coplamos technology and recipient of Electronics' 1978 Achievement Award, is president of Standard Microsystems Corp. in Hauppauge, New York.

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digital

Circle 71 on reader service card

System edits handwritten copy, finishes sketches

by Charles Cohen, Tokyo bureau manager

Prototypes can run with any language and redraw freehand lines as symbols or straight, smooth curves

Computer processing power could soon be available to read edited handwritten manuscripts and produce clean copy or to turn out finished drawings from sketches. The Yokosuka Electrical Communication Laboratory of the Nippon Telegraph & Telephone Public Corp. has teamed a facsimile terminal with a 16-bit minicomputer to demonstrate prototypes of both types of systems.

Because both systems treat input documents as graphics, spelling checks and other features of editing systems using keyboard input are not available. Still, the editing achievable by processing entire written words or single Chinese characters as units is impressive.

Moreover, the system for processing drawings converts hand-drawn lines into finished renderings. Tags added to rudimentary drawings by means of rubber stamps enable the system to process them into drawings with, for example, the accepted symbols for railways, highways, and local streets.

By way of explanation, Susumu Yonezawa, chief of the Visual Communications Applications section at the lab, says that the new systems incorporate a type of optical character recognition. However, the OCR software recognizes the input as graphical symbols, rather than as alphanumeric or Chinese characters. Thus, completely different recognition algorithms have been developed.

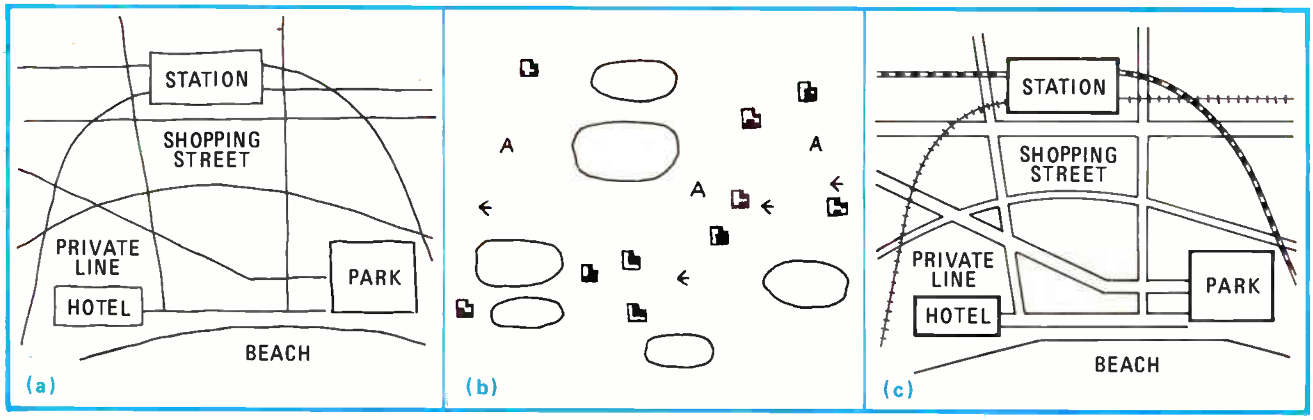
This graphics recognition capability permits editing information to be entered on paper rather than by a keyboard or light pen—and with no dialog between the operator and the system.

Since recognition and processing are based on graphics, the system can replace a freehand line or curve with smoothly drawn ones or can substitute the symbol for a railway or highway for a single line. For writing, the system simply follows instructions to move whatever occupies a given area on the paper from one place to another—it has no knowledge of the actual characters. Therefore, any language—English, Japanese, Arabic—can be used.

Moving ideographs. The Chinese characters and Japanese syllabary characters used in writing Japanese can be moved individually because manuscripts are usually written on paper ruled with rows and columns. The system moves the contents of one or more contiguous boxes as instructed.

Despite the lack of ruled lines, printed Japanese is similar—proportional spacing is not used. Typed English would typically be divided into areas separated by the spaces between words, and handwritten English written on ruled paper can be handled in the same way.

The facsimile terminal provides both input and output with a resolution of 8 dots per millimeter across the width of the page. All processing



Automatic draftsman. NTT prototype system for processing drawings converts hand-drawn pictures (a) into finished drawings (c). An overlay with editing marks (b) determines how lines are controlled. The small black squares are rubber-stamped; the circles hold lettering.

is provided by a commercial minicomputer—several different ones have been used at different points in the project—with a main memory of 128-K bytes, a semiconductor editing memory of 1 megabyte, and a large disk file memory.

Both input and output have only two levels—black and white—as in standard facsimile systems. Any standard facsimile equipment with the required resolution, analog or digital, can be used.

If the facsimile is analog, it can be digitized for computer input. Digital facsimile with redundancy reduction processing can also be used, even though the editing memory stores a bit map of the document including redundant bits, because the signal can be restored by the type of processing used during reception in facsimile systems with redundancy reduction during transmission.

Overlay used. The graphics system employs more complex processing and requires the operator to make editing marks on an overlay, rather than directly on the drawing being edited (see figure). The overlay and drawing are fed into the graphic memory separately.

Putting the editing marks on an overlay permits them to be superimposed on the lines they control—increasing positioning clarity—and read separately for legibility. An innovative digital scheme using small rubber stamps allows graphics input of an almost unlimited number of instructions for processing. For example, stamps only 4 millimeters square can represent 8 bits, for a total of 256 different instructions.

Japan

Look, Dick Tracy, it's a wristwatch TV (and fm stereo, and digital watch)

Dick Tracy's prophecy has come true, albeit 7,000 miles east of 42nd Street: by the end of this year, consumers in Japan will be sporting $400 wristwatch televisions. The product from Suwa Seikosha Co., one of the firms in the Seiko Group, will provide a liquid-crystal-display 1.2-inch screen and driver circuits in the same case as a watch featuring time, calendar, alarm, and stop-watch functions.

A company source says resolution of the wrist watch TV is sufficient to see a baseball and to read titles during news and sports broadcasts. TV circuits and a stereo fm radio, including two alkaline penlight cells that supply five hours of viewing time, are in a 190-gram pocket unit.

Tiny TV. Seiko's TV watch, which sports a 1.2-inch-diagonal screen, depends on a pocket unit containing TV circuits, a stereo fm radio, two batteries, and earphones.

Also part of the set are earphones, whose cord functions as the antenna, as it does in the popular walk-around stereos. A single silver oxide energy cell powers the watch, which is functionally separate from the display that shares its case.

LCD screen. The heart of the display, which Seiko calls an LVD, for liquid-crystal video display, is a 30-by-22-millimeter large-scale integrated circuit that has a switching transistor for each picture element. Also on the IC are shift registers for scanning the display, with redundant registers provided in both vertical and horizontal directions to increase yield. Liquid-crystal material sealed into the space between the chip and a cover glass with transparent electrodes completes the nematic guest-host display.

The 17-by-25-mm display has 210 dots vertically by 152 horizontally, for a total of 31,920 picture elements. Operating power is 100 milliwatts for the display, which Suwa Seikosha claims has a life of seven years. The rest of the all-channel—vhf and uhf—TV circuitry requires only another 400 mW of power for operation. -Charles Cohen

Canada

Codecs shrink, add control or software

Not content with their past world-class performance, the telecommunications system manufacturers in Ottawa are about to come out with yet another bewildering array of codecs. Whether the codecs are software-programmable to replace other chips, have multiple control lines to provide extra features, or boast a unique architecture to reduce chip size, these products from the "silicon valley of the north," as Ottawa is known locally, will be both used inhouse and sent out for export.

Codecs perform a multiplicity of functions in local and central switching offices and private branch exchanges. They will also be found in the all-digital phone when that

piece of gear becomes cost-effective enough for widespread use.

The first codecs developed by Northern Telecom, Mitel, and Bell-Northern Research, all in Ottawa, were little more than analog-to-digital and digital-to-analog converters with filters. The latest models do these chores plus others that used to require subscriber-line-interface circuits (in the form of many ICs) and dozens of auxiliary devices.

Wave of the future. Northern Telecom Canada Ltd.'s E-99 programmable codec can handle both voice and data, so it has many office-of-the-future applications. Until now, the E-99 has been a hush-hush project at Northern Telecom, but some details about it have become available.

According to the firm's assistant vice president, A. G. (Tony) Stansby, the chip transfers practically all the line circuit functions of the company's DMS-100 line of digital switches from printed-circuit boards to a single IC. The 12-volt double-polysilicon n-channel MOS chip is approximately 40,000 square mils in area and comprises over 400 cells with the equivalent of 10,000 transistors. Functions performed include a-d and d-a conversion, filtering, two-to-four-wire conversion, programmable line balance, gain control, dc line supervision, ring signal encoding, relay driving, automatic power-down, selectable μ- and A-law companding, and self-testing—amazingly all in one 22-pin dual in-line package.

Key to the success of the chip is its cellular design. This allows its designers to use a highly structured computer-aided design methodology. The obvious advantage of the use of standard cells—repetition of cell structure—is not as significant in the E-99 (which is a mixed analog-digital IC) as it would be in a highly replicated structure such as 64-K memory. In fact, over 250 of the 400 cells in the E-99 are unique, so it would seem that standard cells are of little help.

Team design. What made Northern opt for the cellular approach was the fact that it let design be a team effort. Nevertheless, there was still a great degree of uniformity in the presentation of the data for manipulation by the firm's CAD system. Stansby says that the chip's production yield and cost effectiveness owe the most to this approach.

Line cards incorporating the new E-99 device are currently undergoing tests and will be in service in DMS-100 gear before 1983. In contrast, Mitel Corp.'s just introduced SX-2000, a 10,000-line private branch exchange [*Electronics*, June 2, p. 56], has a new codec already shipping out with the unit.

In fact, Mitel's codec-filter, designed with Swindon Silicon Systems of Swindon, England, is geared to per-channel PBXs. The feature "that makes the chip somewhat unique," as its inventors put it, is its control data path.

Under control of the PBX, two 8-bit words can be loaded into the control section of the codec-filter. Two bits provide testing capability, 2 provide power-down and loop-around modes, 6 handle totem-pole or open-collector outputs, and 6 provide gain control by 1-, 2-, or 4-decibel pads in the chip's fifth-order transmit and receive filters. With this kind of control over its own operation, the chip contributes mightily to the many features that are packed into the

Terminal that accepts handwriting lets the uninitiated use computer

A Japanese terminal that can read handwriting opens the door to the use of word-processing systems by persons unacquainted with keyboards. Developed by Nippon Electric Co. of Tokyo, the prototype terminal—which is as yet unnamed—can recognize 1,100 kanji and hiragana syllabary characters and symbols that are written in its input tablet, which digitizes the position of the pen. The tablet is basically quite similar to that used in NTT's Sketchphone [*Electronics*, Feb. 10, p. 82]. Additional characters, including the Roman alphabet, are available on a character shift analogous to the shift key on a typewriter.

In the unshifted mode, the terminal tries to decode writing as hiragana or kanji or associated symbols. In the shifted mode, the terminal tries to decode writing as the Roman alphabet or katakana syllabary or associated symbols.

Using a 16-bit processor that NEC will not identify and 64-K of program memory, the system samples the position of the pen at regular time intervals and converts them into a sequential list of pen directions at successive time intervals. Comparison is then made for the best match with standard patterns that are in the same form—sequential lists of directions at successive time intervals. To increase the recognition rate, there are also standard patterns for common variations of some characters. Also, dynamic programming matching varies the length of letter segments and the entire written pattern in its attempt to find the best match. This method has been used with great success in speech recognition systems by NEC. Numbers are keyed in from 10 windows.

NEC will start marketing the terminal this fall for less than $700. Although the unit is compatible with any system having an RS-232-C serial interface, it is a bare-bones, low-cost peripheral intended for use with personal computers, such as the company's PC-8801. NEC plans to market a step-up model for professional applications.

-Kiyo Inoue and Charles Cohen

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Mitel's 2.048-megahertz synchronous codec-filter is designed with a 5-micrometer silicon-gate double-polysilicon Isoplanar complementary-MOS process that produces a 175-by-132-mil die. It operates from a ±5-V supply and draws 30 milliwatts of active power and 5 mW power down, while meeting all North American and European PBX recommendations.

Refinement. Although new codec architectures are fine for the needs of new product designs, product refinement simply for increased cost-effectiveness is not to be ignored. For example, Bell-Northern Research has been producing codec-filters for several years, but its latest device is a fine example of how architecture refinement improves a chip.

The firm has come up with a 24,000-mil² codec-filter that is half the size of its predecessor and consumes half the power—120-mW active power and 15-mW power down from a 15-V supply. It is implemented in a 6.5-μm gate-enhancement n-channel MOS process and is designed for central-office synchronous operations only.

Since asynchronous operation is ignored, the Bell Northern design team was able to eliminate clock recovery circuitry, independent clocks for transmitting and receiving functions, and a d-a converter. A single converter is multiplexed between the coding and decoding circuitry. Thus chip size reduction in this case was simply—though not easily—a function of design techniques.

Similar approaches to reducing chip size and thus raising yield are under study by codec makers outside Canada. **-Harvey J. Hindin**

Great Britain

GaAs epitaxy yields microwave devices

For a potential sixfold improvement in circuit performance over bulk silicon, researchers the world over have been turning to gallium arsenide, but the technology has proved difficult to tame. In the world of high-performance linear circuits operating up to 20 gigahertz, however, researchers at the Plessey Co. PLC's Allen Clark Research Centre, Caswell, Northants., have been making progress on a broad front.

They have cracked the problem of growing epitaxial layers on large-diameter wafers, the starting point for linear integrated circuits of the very highest performance. According to Michael J. Cardwell, who heads up the Microwave Materials group, Plessey is now producing epitaxial layers on 3-inch wafers with high throughput and uniformity.

Cheaper substitute. There is an alternative to epitaxial GaAs—ion-implanted GaAs wafers. Such wafers are cheaper almost by a factor of 10 since the process can be more highly automated and GaAs ICs are predominantly manufactured by this route. However, says Cardwell, "many circuit designers would gladly sell their grandmothers for the extra performance and lower noise that comes with epitaxial devices."

Plessey is good at the epitaxial process, because it has been at it longer than anyone else. It developed this now-standard method back in the 1960s.

The process forms a thin conducting n-type GaAs epitaxial layer atop the pure substrate, which is inherently semiinsulating. The technique involves the vapor-phase transport of GaAs by hydrogen chloride.

The layers are doped by the addition of hydrogen sulphide to the gas stream to produce n-type layers. Plessey has mastered the process with a lot of fundamental physics research and the use of microprocessor control. What's more, the process is now repeatable—the group has three reactor lines running to produce in excess of 2,000 wafers a year, sufficient to meet its research demands and production requirements for its sister group, Plessey Optoelectronics & Microwave.

Meanwhile, further downstream, the company's circuit designers are well-advanced with proving in isolation all the functions needed for a complete range of GaAs IC communication systems. Says George Gibbons, who heads up the Solid State Research division, "We have demonstrated in isolation all the functions required in a monolithic receiver: the amplifier, mixer, and local oscillator."

The group is comparably well along in developing the transmitter functions, too: power amplifiers, phase shifters, transmit-receive switches, and power switches. Now the company is busy designing these functions into systems.

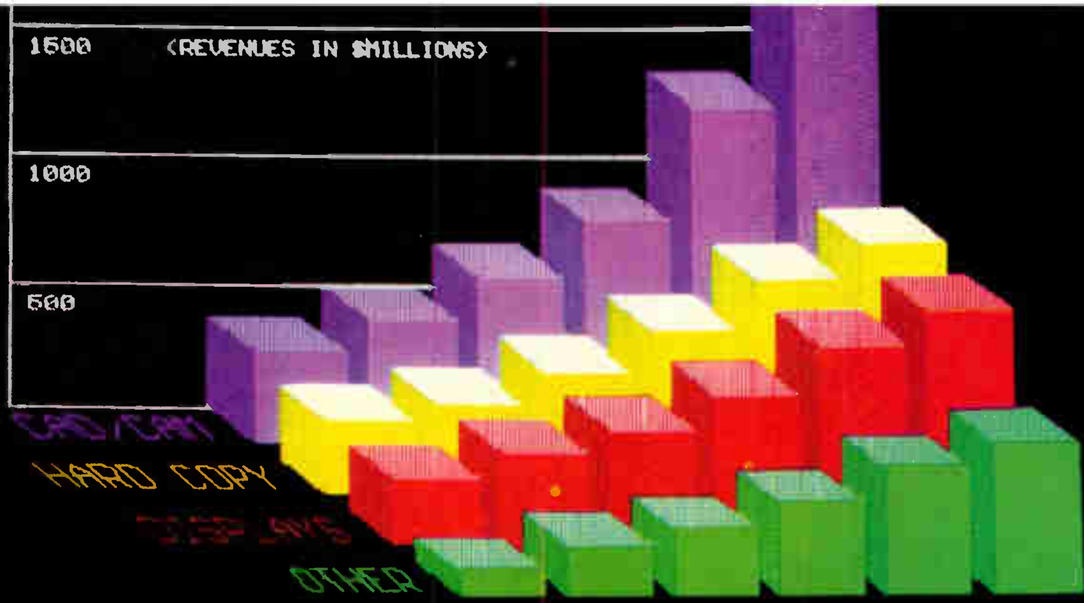
Circuit described. Most recently, at the International Solid State Circuits Conference, Plessey described a fully working phase-shift circuit designed for an active phased-array radar. The circuit incorporates an active splitter and an attenuator in field-effect transistors, as well as a lumped-element combiner. It is now in the process of being integrated into a single chip.

In the consumer sector, the company has long been marketing a GaAs hybrid front end for the reception of direct broadcast by satellite television. The next stage, says Gibbons, is to produce a more highly integrated version in which the entire front end would shrink to just four chips in a 1-square-centimeter package.

Exotic optics. More exotic is an optoelectronic test chip that could eventually become a complete optical repeater on a single chip. The initial research is concentrated on gallium-aluminum-arsenide grown on GaAs. Multiple layer structures have been grown by metallo-organic chemical vapor deposition and are exposed and delineated by selective etching techniques.

The group has already fabricated simple test chips including light-emitting diodes, p-i-n photodiodes, FETs, and resistors. It is now busy integrating them into one structure.

Epitaxial wafers are currently selling at around $110 per square centimeter, but this figure is highly volume-related and prices could be halved with first commercial applications. **-Kevin Smith**



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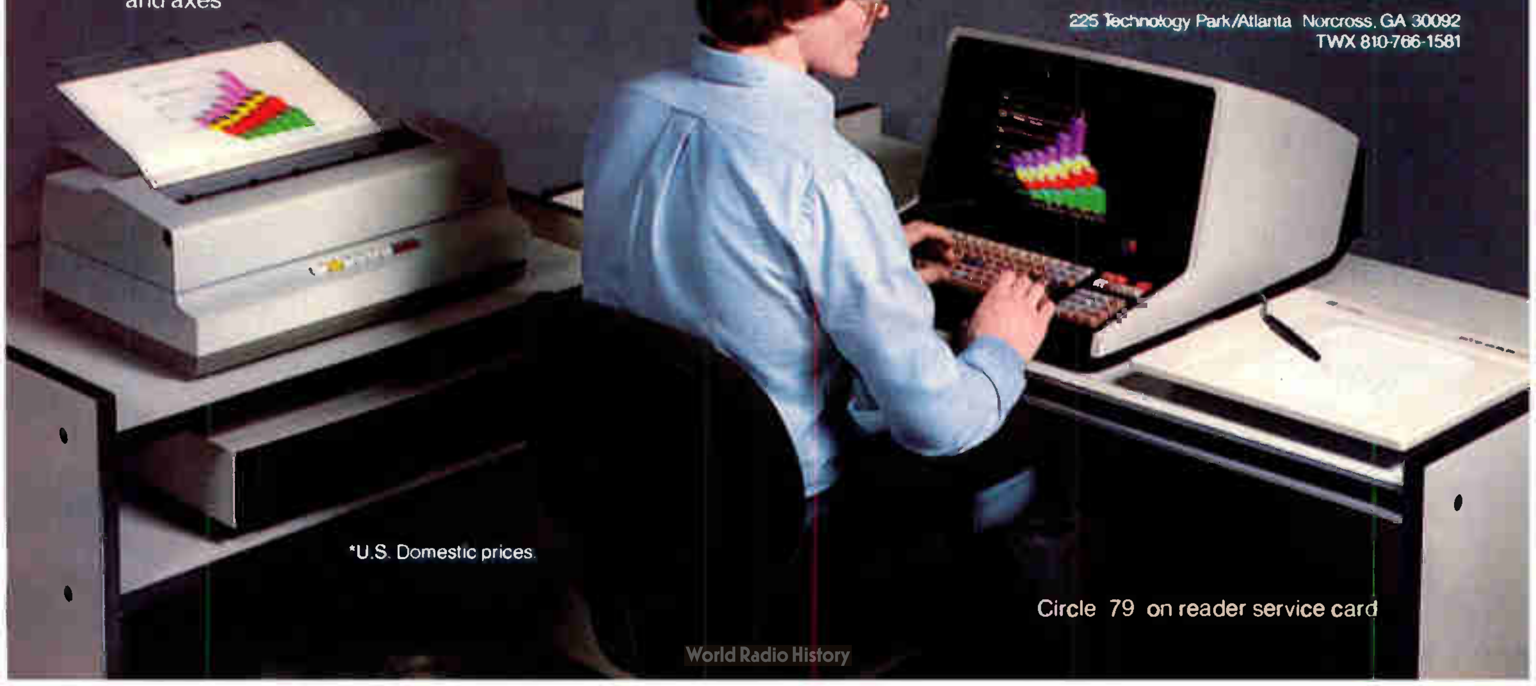

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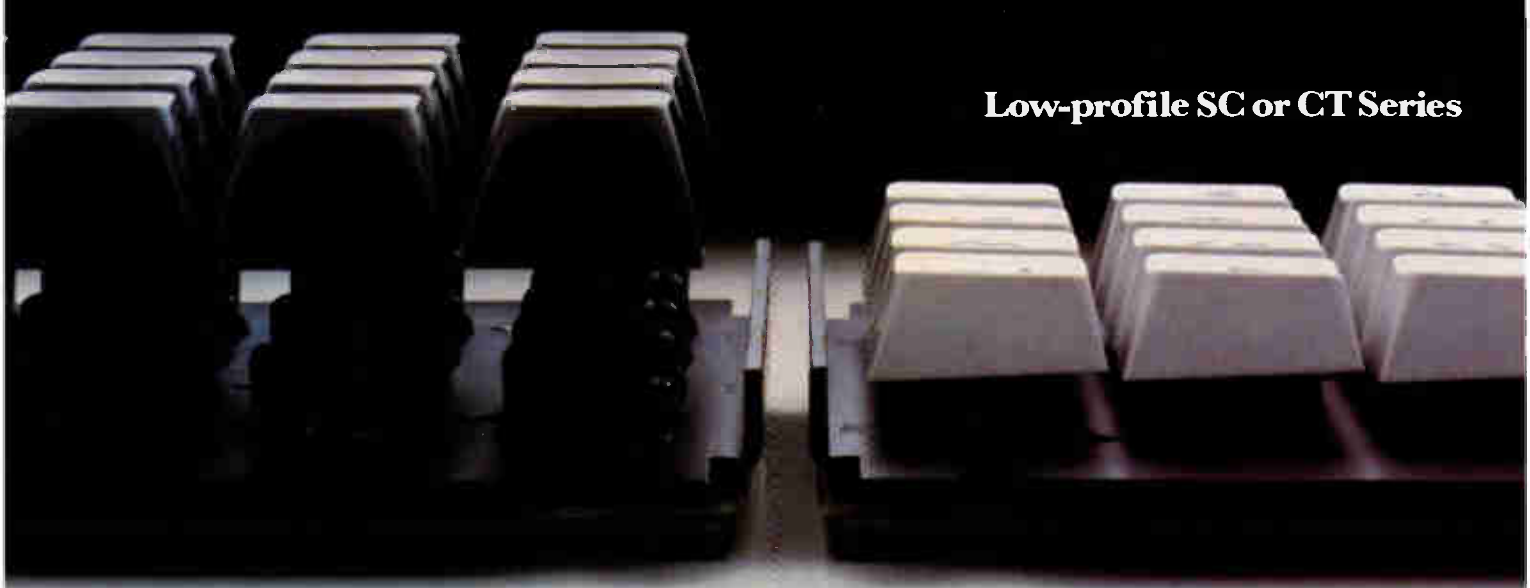

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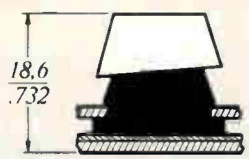

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Circle 80 on reader service card

Four-state cell called density key

Technique that varies sizes of gates will permit Motorola to save 40% of space in new 256-K ROM

by J. Robert Lineback, Dallas bureau

Pressed by the need for greater densities on smaller semiconductor chips, read-only-memory manufacturers have contemplated from time to time multistate cell structures that can store more than 1 bit of data in a single cell. But ironically, that same race for higher integration has set back the use of multibit-per-cell schemes.

With each new advance in microelectronics processing, chip designers find they can comfortably reach the next generation of density simply by shrinking geometries and packing more 1-bit cells in the memory array of ROMs. And because unconventional device structures often burden processing and design efforts, ROM chip makers have thus far tended to shun multistate ROM cells. However, that could change rapidly if Motorola Inc. demonstrates the cost benefits it believes it will get with a new four-state memory cell scheduled for use in a commercial 256-K ROM late next year.

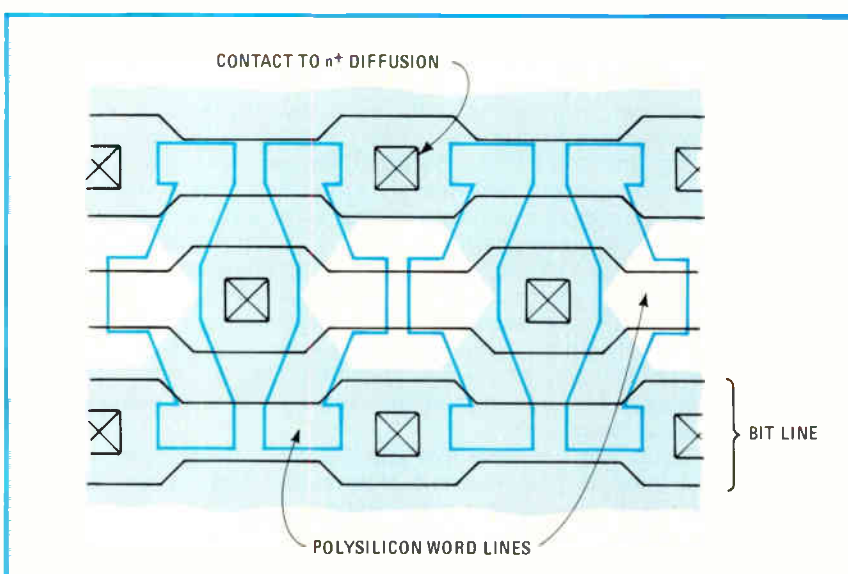
To make the part—designated MCM65256—Motorola has developed a unique geometric programming technique that varies both the effective width and length of polysilicon gates in memory cells (see figure). This layout creates transistors with different channel lengths and widths, and hence resistances. The four states are four current levels from the cell when it is selected. Two comparators in the sense amplifier check the cell current against a fixed reference to generate two bits of data from a single cell.

The result is that Motorola will be able to lay out a 256-K complementary-MOS ROM with about 40% less space in its memory-array region and an overall silicon savings of 25%, says Bill Donohue, ROM design manager at the firm's MOS operation in Austin, Texas. "We are more or less setting up to do this for even larger ROMs, but I think at the 256-K level it's already going to make a substantial savings," he states.

Width only. However, Motorola's chip will not be the first device on the market to use four-state ROM cells. Intel Corp. of Santa Clara, Calif., has been employing 2-bit-per-cell technology on its 8087 numeric processor for about three years [*Electronics*, Oct. 9, 1980, p. 39] and on the more recently introduced execution unit of its iAPX 432 32-bit microprocessor.

With Motorola's four-state approach, differentials in the currents are created by a combination of various channel widths and lengths, a process on which the company filed for a patent this month. With narrower gates, the channel resistance is increased and the current is lower. If the channel length is shortened, the resistance decreases and the current goes up. "By using this technique, we can keep the cell size reasonable and still have more current differential," Donohue explains. "You have kind of a multiplying effect and the current differential is much better than just varying the width. The differential that we get between the reference and the cell is about a fourth of a volt, which is pretty substantial."

In addition to the unique ROM, Motorola is designing a more conventional two-state 256-K channel device (the MCM63256), which will actually be introduced to the market ahead of the C-MOS part in the first



Four states. Motorola programs its ROM cells by tailoring the width of the polysilicon word lines. The resulting four transistor sizes have four different current levels when selected.

half of 1983. The high-performance n-channel MOS device is being optimized for speeds, while the C-MOS ROM is designed for low power.

More potential. As well as higher bit densities, Motorola's four-state process lends itself to greater flexibility compared with other multibit-per-cell methods, Donohue says. "One advantage with our approach is that it's polysilicon programmable. Instead of dealing just with the first layer of silicon nitride, which is the thin-oxide definition and is normally done early in the process," he states, "we are talking about poly variations and programming in poly, which is later in the process cycle."

Because the four-state approach reduces the size of the memory array, access times promise to improve, Donohue suggests. "In the conventional n-MOS two-state ROM, the array is 512 high by 512 wide. But in our four-state device, it's 512 high and 256 wide. So the poly word line is half, and we expect to see that make a difference in performance to a certain degree," he states. "On the megabit version, you may pick up even greater benefits by cutting the word line in half."

A number of ROM designers believe programming four-state cells by device geometries is currently a more feasible approach than double-layer implant programming, in which multiple thresholds are established in each cell by varying the dosage of ions in the channel region. With implant programming, four-state cells may be smaller than those yielded by the geometric approach.

However, today's processing technology and sense-amplifier designs have, for the most part, some limitations in the threshold scheme. Sensing amps may not be able to distinguish the thresholds under worst-case variations in the implant dosage. For this reason, Donohue says, Motorola for the time being has elected to go with the geometric programming method, which it believes will more consistently yield greater signal margins.

Work to be done. Eventually, implanting multistate cells may become more attractive since it affords the greatest potential of silicon savings. To do that, however, developments must continue in sense-amplifier designs and implant processing, says Douglas Sheppard, designer with Mostek Corp., which has also been studying four-state technology. "We have looked at both approaches, and if I were to go off and design a 2-bit-per-cell ROM, I would not throw either one out yet," he states.

In fact, Mostek is making available a 256-K ROM, the MK38000, which is based on a conventional two-state X-shaped cell [*Electronics*, June 2, p. 141]. The Carrollton, Texas, MOS firm packs the ROM onto an n-MOS chip measuring 52,000 mil^2. (Motorola's four-state C-MOS design will have a die size of about 50,000 mil^2.)

But Sheppard maintains that the time has still not arrived for cost-efficient four-state ROM cells. In fact, Mostek's megabit design team is now in the conceptual stages of layout, and Sheppard is confident that the megabit ROM can more easily be achieved with two-state cells. He also points to such concerns as being able to program four-state ROMs late in the processing cycle as well as possible speed penalties, because signals must be sensed at lower margins.

Lower limit. "Eventually, when we cannot push geometries down small enough to cram more and more single-bit cells into an area, then you are forced to get more creative. It [multibits per cell] can be done—no doubt about it—and it can merit a very good design. But the question now is cost savings," Sheppard says. And other manufacturers seem to agree (see "Multistate ROM cells have few friends," left).

Motorola's Donohue is also aware of certain tradeoffs between the use of conventional cells and the multi-bit-per-cell structures. "It makes forms of redundancy on ROMs even more out of the question," he notes. "There is another possible question about four-states. It is that you may not be able to do mixed masks—it's difficult to use a program layer that is loosely aligned." The alignment issue will make the use of steppers difficult in processing. However, implant programming has an advantage here, in that it has less critical alignment requirements compared with those for geometrical programming, he explains. □

Multistate ROM cells have few friends

Other manufacturers of read-only memories are not rushing to implement multistate cells. National Semiconductor Corp. in Santa Clara, Calif., and Texas Instruments Inc. in Dallas both say they are studying multivalue logic read-only memory structures, but they have no immediate plans for them. American Microsystems Inc. of Santa Clara, a custom chip maker that is also a leading ROM supplier, also says it is not planning to use four-state cells in its coming generation of memories. Although it says the decision was not based on ease of processing or costs, Intel Corp. has opted to forgo the 2-bit-per-cell approach on its new 80286 16-bit microprocessor with on-board memory management and memory protection. Instead, the Santa Clara firm says the use of more conventional ROM cells was left to the discretion of project-design engineers.

In Japan—where ROM capacity is of pressing importance because of the space required to store and display Kanji characters—the story is the same. Nippon Electric Co. is not considering a four-state cell because signal-margin problems would likely cut into yields, says Shigeki Matsue, manager of the company's semiconductor department. Mitsubishi Electric Corp., Toshiba Corp., and Hitachi Ltd. all state that they are not currently working on four-state ROM cell designs.

But Motorola remains confident that 256-K space savings of four-state ROM cells will translate next year into lower costs. And it believes that savings promise to grow as ROMs increase in bit density. "If the area-saving advantages are really what we are seeing, then it's possible that one day there will be no more need for single-bit-cell ROMs," Donohue suggests. In addition, other memories—such as electrically erasable programmable ROMs—could eventually employ multistate cells **-J. Robert Lineback**

Consumer

Video disks look to industrial market

Consumers are slow to buy playback systems, while some experts believe that their real role is as a computer peripheral

by William E. Suydam, Industrial/Consumer Editor

Having fared poorly in their initial attempts to market video disks as a consumer item—sales of players have been far below expectations—vendors of the technology seem to be betting on such commercial and industrial applications as software to spur the market demand that could lead to lower prices.

The Electronic Industries Association fixes total video-disk-player sales at 157,000 for 1981, well over the 40,000 figure for 1980. While refusing to discuss actual figures, John Messerschmitt, vice president of North American Philips Corp. in New York, confesses, "We are very disappointed with sales. The only excuse we have left is the economy." RCA Corp. had previously predicted sales of 200,000 players for their first year, which began March 1981. On the other hand, total industry sales of disks jumped tenfold during the same period, from 300,000 in 1980 to 3 million in 1981.

However, Judith Paris, a consultant and president of Advanced Information Management Technology Inc., points out that harsh judgments of market performance may be unjust, reflecting as they do overenthusiastic early predictions. All in all, the oldest video-disk technology still in use dates only to about 1976—the original laser-based DiscoVision system, resurrected under the name LaserVision by Sony, Philips, Sylvania, and Pioneer. RCA calls its system CED, for capacitive electronic disk.

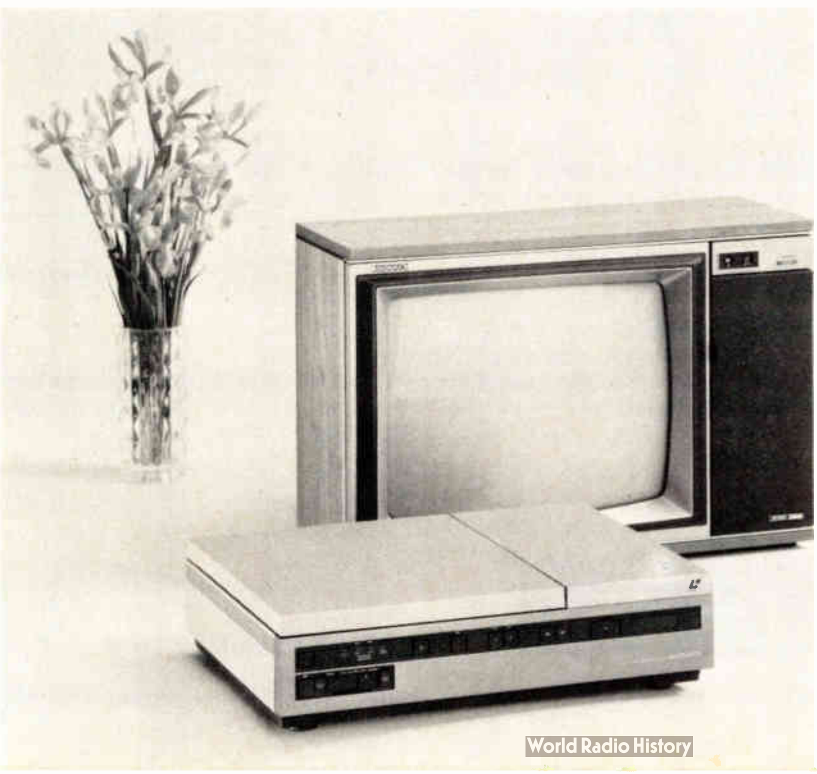
"If you look at video-cassette-recorder sales during the first few years on the market, video disks are doing very well by comparison," Paris maintains from her McLean, Va., office. "The whole technology is a lot like personal computers. Originally there were high expectations, then the high-volume sales failed to materialize. But look what has happened to sales of personal computers and peripherals since IBM introduced its Personal Computer."

Training aid. International Business Machines Corp., ironically, quit the disk business when it sold its interest in DiscoVision Associates, vendors of the original laser disk. But IBM, along with many large firms, has not forgotten about the technology. While weighing video-disk players for possible uses as the mass-storage computer peripherals some say they really are, IBM is already using them for in-house training.

IBM uses interactive video disks as both a sales tool and a training aid. A two-sided disk supports IBM's Patient Care System computer. One side contains a sales presentation, and the other provides an orientation or training session on the system's use. That disk is run on an industrial-grade player, the Pioneer 7820 model 1.

IBM should soon introduce a video disk called Product Selector. Running on a Pioneer 7820 model 3, this disk will question the customer about his or her needs, then display the IBM product most closely meeting those requirements.

Good for GM. General Motors, the largest user of interactive video-disk systems, is turning to them for point-of-sale demonstrations of cars and trucks, complete with options. At the



Luxury features. Opting for such capabilities as infrared remote control and random-access keypad, Magnavox suggests a $750 price for its LaserVision format item.

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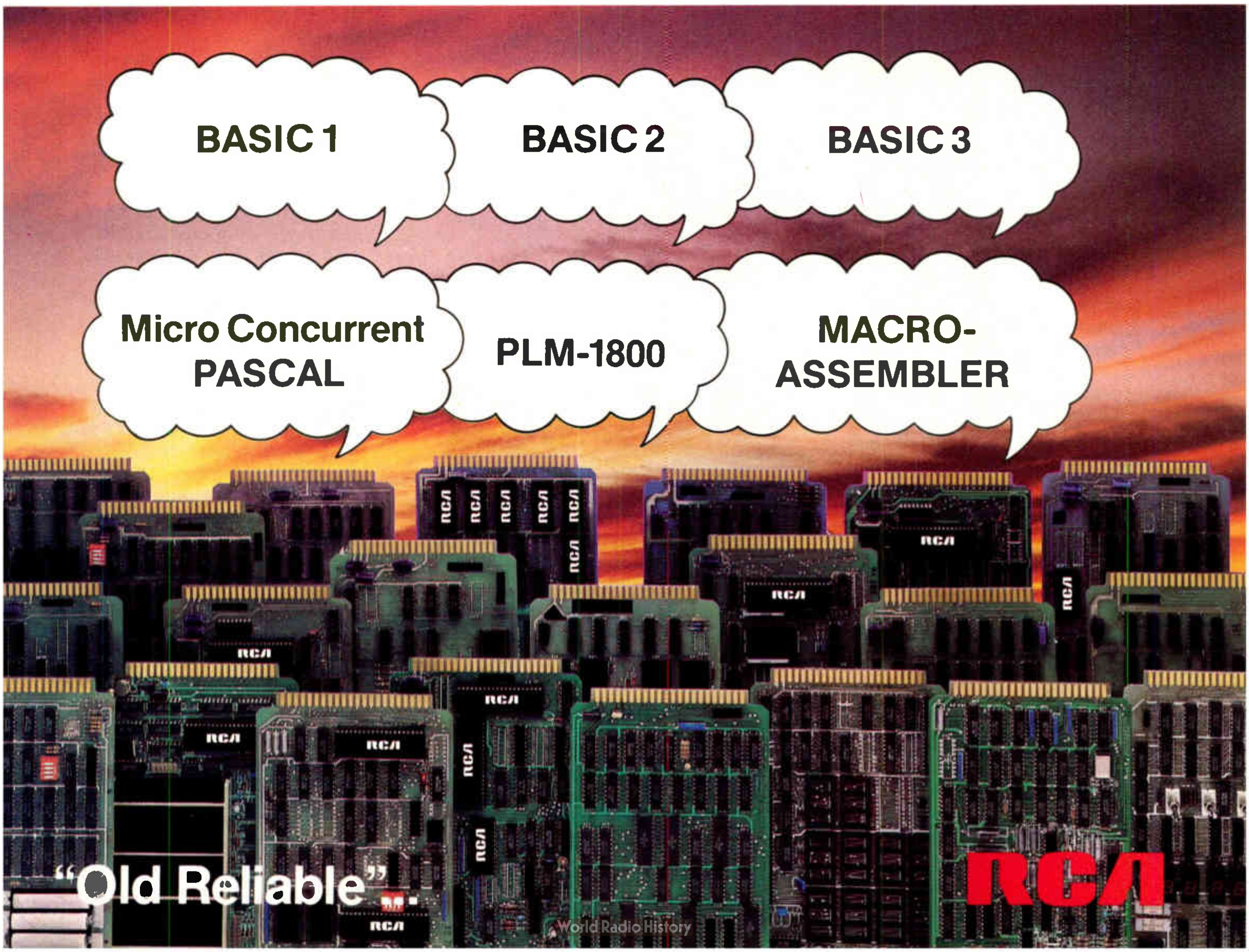

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Consumer Electronics Show in Chicago early in June, game-merchandising giant Atari Inc. of Sunnyvale, Calif., demonstrated the Atari computer that sells itself—with the aid of an interactive video-disk system.

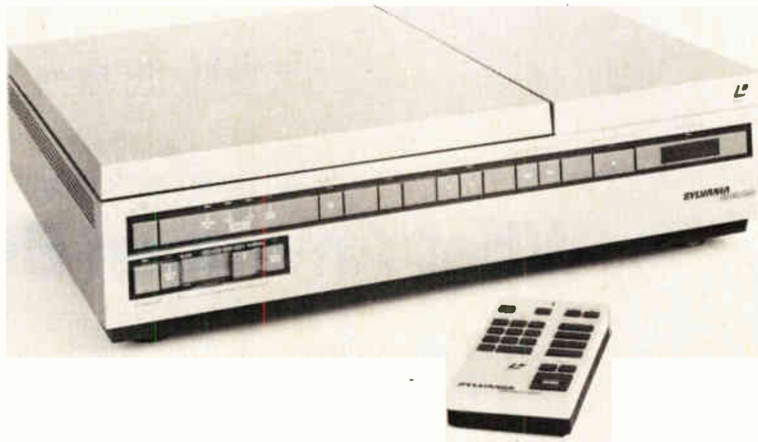
However, Atari was not alone. Magnavox, a division of North American Philips, displayed a system using an Apple II Plus in combination with one of the commercial interface cards available for remotely controlled LaserVision models. Also, Philips demonstrated other experimental video-disk systems.

Peter Crowell, president of the Advanced Learning Systems organization of Black Hawk, Colo., which produced the Product Selector and Patient Care disks for IBM, emphasizes the importance of distinguishing between industrial and consumer video-disk players.

Keypad control. Sony, Pioneer, and Thomson-Brandt market players that incorporate a microprocessor and random-access memory. As a result, they can load program instructions from the laser disk into the processor memory. This loading allows interactive keypad control and eliminates the need for microcomputer access to the player through a remote-control port, the only form of interactive system available with consumer-grade players. Though consumer LaserVision players start at $700 retail for the Pioneer VP-1000, industrial-grade players typically cost around $2,800 in single quantities.

The IBM Product Selector is similar in purpose to Atari's Electronic Retail Information Center—ERIC—that will demonstrate Atari 400 and 800 home computers to consumers. As a person approaches ERIC, its proximity sensor switches on a TV screen showing a salesperson who invites the consumer to participate in a demonstration. When the demonstration is over, the unit directs the customer to a human salesperson for additional information.

As attention turns to the commercial market, insiders are debating the reasons for the unfulfilled consumer hopes. In an attempt to explain why RCA's initial expectations were so off-base, Paris terms the video disk "a computer peripheral. Until there's recognition that it's a software-driven industry, we're not going to see it take off as predicted."



Looking upscale. As RCA aims its VideoDisc at the consumer market, Sylvania, like Magnavox, appeals to the buyer seeking extras with this $750 player. RCA's price is $299.

Disks in lead. She points to the RCA marketing figures as proof. "They spent $200 million. They have sold 100,000 players. But they've sold millions of disks. What that means is that it's a software-driven industry."

Venture Development Corp.'s Ray Boggs agrees. The Boston consultant refers to an R-rated video disk from Japan that Pioneer displayed on a large bank of screens at Chicago till show management insisted it be discontinued because of the crowds it drew. "X- and R-rated programming may well be the Visicalc of the video-disk market," he concludes.

Another significant driving force in the market is price. RCA announced at CES that within seven weeks after it reduced the price of its original SFT-100 video-disk player to $299 last February, more players were sold than in the seven weeks before Christmas.

Nevertheless, Paris might be correct in pointing out that the market is also software-driven. Though RCA's overall player sales may seem disappointing, disk sales have far exceeded the most optimistic forecasts. RCA marketing studies indicate that consumers who owned a player for a year buy an average of 32 disks. The results of the survey of 1,200 owners, released at CES by Thomas Kuhn, vice president of RCA's SelectaVision video-disk division, showed that owners who had owned their players only four months or less already had about 15 disks each.

RCA already has 200 titles on the market and expects to double that—including those from other vendors—by the end of this year. The company is no doubt counting on that software store, combined with the lower price of the players, to keep afloat in choppy market waters.

Will one of the two currently popular video-disk formats emerge victorious in a market battle, or will they peacefully coexist by identifying distinct market niches? Sony, Philips, Pioneer, and Sylvania are supporting a format that is readily compatible with such luxury features as infrared remote control, random-access keypads, and freeze frame—plus ready computer interfacing.

On the other hand, though RCA demonstrated a prototype CED player capable of random access and a limited form of freeze frame, the company originally intended to supply cheap, serial-access video disks and players to the consumer market.

Buyers vote. To the extent that a large base of players encourages vendors to supply software in a particular format, majority rule could determine which video-disk technology stands to benefit most from outside support. Whichever way, Advanced Learning's Peter Crowell is optimistic. "For any kind of programming where interactivity is a benefit, video disk is the only way to go. In the next two to five years, you are going to see tremendous growth in this field, even if consumer video disks go deep six." □

Data communications

What American Bell offers

AT&T's new unregulated subsidiary is to sell information teleprocessing, time-sharing, and ancillary services

by Harvey J. Hindin, Communications & Microwave Editor, and Tom Manuel, Computers & Peripherals Editor

Everybody is oohing and aahing about the potential muscle that American Bell Inc., the new unregulated subsidiary of American Telephone & Telegraph Co., will flex in the data-communications business. But just what will the fully separated offspring, which goes into business with headquarters in Parsippany, N. J., on July 1, really have to offer?

One thing is certain. The communications-processing services it will sell are a lot more than mere public packet-switching. Although the exact form of the new services is still unknown, industry consultants agree that the Advanced Information System Net 1 (formerly Advanced Communications Service) will be broad. In addition to offering intelligent packet-switched network communications, American Bell will go after the data-communications front-end processing market enjoyed by IBM Corp. and other traditional suppliers, plus the value-added services offered by the time-sharing industry, as well as some as-yet undefined new services.

What all this amounts to is a gaggle of service bureaus with communications capability. Each is a profit center, according to the capitalization plan for American Bell approved by the Federal Communications Commission, and they do not care how they talk to one another. American Bell says Net 1 could use Bell's packet-switching service or even the public packet-switched nets.

Why AT&T would strike out in such a manner is explained this way by Kenneth G. Bosomworth, president of International Resource Development Inc., a Norwalk, Conn., consulting firm: "If you were a planner at AT&T and came up with a value-added service, you wouldn't want another Telenet or Tymnet. Their sales pitch is that they offer packet switching cheaper than with AT&T's leased lines. There's no point in AT&T coming up with a packet service that just takes money from one of its pockets and puts it into another one."

Based on what Bell says, IBM does not say, and consultants believe, the service lineup should include:

- Information teleprocessing, because, simply put, Fortune 1,000 companies that operate large distributed networks nationally would rather not do so. They have been forced into handling their own communications processing because there has been no one to do it for them and they are dependent on IBM and what a West Coast consultant labels its "notoriously inefficient communications software." American Bell figures that these companies are itching to offload as much of their communications burden as possible.
- What amounts to time-sharing services. For example, when farflung company branches have their cash pooled at day's end for overnight investment, Bell would handle the transactions.
- Various new services, including, among others, a buying service for electronic parts.

The boss. Sal Barbera, chief executive officer of American Bell, started his AT&T career as a switchman at New York Bell.

Get 'em young. In the area of information teleprocessing, Bell expects to offer enough services to prevent many growing firms from migrating to a full-fledged network such as IBM's Systems Network Architecture. For example, American Bell would handle order entries: raw requests from a branch that must be fully processed, the information distributed to multiple sites, and the fully processed order routed to its final destination.

The new company expects to excel in such processing by allowing its customers to have Cobol software in the nationwide network of nodes that it will provide, for they can hook into Net 1 any way they desire. This is a radical approach—node software in the data-communications field has traditionally been sacrosanct. For example, although some limited processing services are provided, Tymnet and Telenet are basically in the transmission business.

Yet even this is changing. Warren Prince, president of the Cupertino, Calif.-based Tymnet Inc., states that the company is now doing application programming (not user-generated) in its nodes.

Tymnet's competition, Telenet, which is based in Vienna, Va., thinks Net 1's services will be similar to what it offers—at least in the beginning. Telenet does have some enhanced transmission offerings such as Telemail, but more importantly, it and Tymshare offer the X.25 packet-switching protocol for data-generating and -receiving gear that uses packet switching directly—something Bell is only planning.

In any case, if Tymshare and Telenet are to protect their market shares—$60 million for Tymshare and $50 million for Telenet in 1981—as Bell looks for $500 million by 1985, it is clear that both will have to grow faster and offer more applications, especially those that are user-generated.

Another natural function for Bell is the financial time-sharing one. Available now from several competitors, the service would mean connecting all the offices of a firm nationwide with most banks and brokers. To put it conservatively, AT&T has had a great deal of experience in that game.

And the rest. Finally, there is the potential for a host of ancillary services, such as the scenario popular with the industry watchers for a Net 1 parts-purchasing service. Small firms without purchasing departments could use the network to get the best price and delivery of, say, 64-K random-access memories.

AT&T maintains steadfastly that 84% of the terminals in use in the U.S. can be accommodated by the software in each of the 17 nodes that will be in place by the end of 1983. But whether terminal owners will flock to Net 1 is another question. One view is that the new company has already erred. For example, it is servicing terminals that, by and large, use the older IBM Telecommunications Access Method (TCAM) software while not servicing those using IBM's newer Virtual Telecommunications Access Method (VTAM). The reason, says consultant Harry Newton of the Telecom Library in New York, is that AT&T started designing the new service as the predecessor ACS some six years ago. But others say that no VTAM is part of a strategy enabling American Bell to tell customers that so much service will be provided that they will not have to upgrade.

But good or bad, right or wrong, AT&T is laying its cards on the table in what Newton calls "the biggest industrial gamble in U.S. history." ☐

Probing the news

wave applications in the 4-GHz range. At the 270-to-770-MHz band, signals may be transferred to a customer's indoor unit through low-loss, low-cost cabling. This indoor unit performs any additional frequency conversions, signal demodulation, video and audio processing, remodulation before sending the final signal to the TV set.

Potentially blocking immediate realization of the advances are the usual legal obstacles to new communications services. One reason is that the eight applicants to the FCC have, in the words of Richard G. Gould of Telecommunications Systems Inc. in Washington, D. C., "proposed systems with widely different technical characteristics and transmission standards."

Different reasons. Each applicant company is pursuing its own particular interest. Satellite Television Corp., for example, a subsidiary of Comsat Corp., wants to supply three original-broadcast service channels. Another applicant, the United States Satellite Broadcasting Co., a subsidiary of the Hubbard Broadcasting Co., wants to have its satellite distribute locally originated TV shows. For its part in the scramble, CBS Inc. is after DBS in order to broadcast high-resolution TV. Such a system would afford U. S. viewers the superior quality of reception enjoyed in Europe.

Other companies, such as Direct Broadcasting Satellite Corp., RCA Corp., and Western Union Corp., are proposing to lease their channels to various programmers. The first named is the only applicant seeking common-carrier status—that is, to lease its channels without prejudice. In contrast, RCA and Western Union prefer to choose their lessees.

One of the lease contenders, for example, Focus Broadcast Satellite Inc., says it could go on the air by 1984, planning to arrange for channels from the existing 12-GHz Western Union Westar satellite. The legal snarls if any of these companies are stymied could prove a nightmare.

Rules due. The FCC was due last week to adopt rules allowing tests of candidate DBS systems. Authorization of such experiments under interim policies, the commission says, would "serve the public interest" because it would avoid unnecessary delays. Unfortunately, such a shortcut—perhaps generated by the criticism of the decade the FCC took to devise a plan for a nationwide cellular-radio service—is not sufficient to get DBS up and going.

It turns out that nothing final can be done until after the June 1983 Regional Administrative Radio Conference in Geneva. According to plans laid out at the last World Administrative Radio Conference, the regional conference will look to determine just which frequencies and orbital slots will be alloted to DBS in the Western Hemisphere. An advisory committee to the U. S. delegation, chaired by John F. Clark, director of space technology for RCA, has already started formulating the U. S. approach to the questions to be raised at this meeting.

Meanwhile, the FCC has received objections to DBS from TV broadcasting companies. Mindful of potential competition, the broadcasters say that the commission needs congressional approval to authorize satellite-to-home broadcasting. The FCC counters by claiming it can establish a nonlocal system and that competition from such a system would do little or no harm to local programming. The effect on the present 1,800 terrestrial users of 12-GHz microwaves is another question that must be addressed.

Industry experts doubt that they could exist with DBS without major interference problems. So, if they are not to be put out of business, a place will have to be found for them.

What rural residents, hotels, and businesses—expected to make up the bulk of DBS users—will pay has been fairly well estimated. Says Yves Blanchard, director of marketing at Mackintosh Consultants Inc. in San Jose, Calif.: "With the addition of the marketing cost, taxes, and installation fees, the factory cost of 1,000 complete systems in 1985 will be $355 each." Blanchard also says that the cost to a DBS supplier to study and develop a new system will be $120 million, with another $60 million to $80 million for construction, testing, and delivery. ☐

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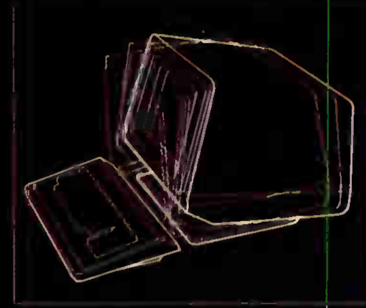

Tilt: 10° forward, 15° backward

Swivel: 270°

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FEATURE COMPARISON CHART					
FEATURE	VISUAL 50	Hazeltine Esprit	ADDS Viewpoint	Lear Siegler ADM-5	Televideo 910
Tilt and Swivel	YES	NO	NO	NO	NO
Detached Keyboard	YES	NO	YES	NO	NO
N-Key Rollover	YES	NO	YES	NO	NO
Audible Key Click	YES	YES	NO	NO	NO
Menu Set-Up Mode	YES	NO	NO	NO	NO
Status Line	YES	NO	NO	NO	NO
Full 5 Attribute Selection	YES	NO	NO	NO	YES
Smooth Scroll	YES	NO	NO	NO	NO
Line Drawing Character Set	YES	NO	NO	NO	NO
Block Mode	YES	YES	NO	NO	YES
Insert/Delete Line	YES	YES	NO	NO	YES
Bi-Directional Aux Port	YES	YES	NO	YES	NO
Columnar Tabbing	YES	YES	NO	NO	YES
Independent RCV/TX Rates	YES	NO	NO	NO	NO
Answerback User Programmable	YES	NO	NO	OPT.	NO

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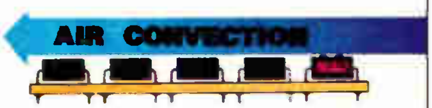

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Molding computer terminals to human needs

West Germany leads the way in setting standards; makers everywhere scramble to build more comfortable gear

by Tom Manuel, *Computers & Peripherals Editor*

☐ The astonishing progress of the microelectronic and data-processing technologies guarantees that most jobs will soon at least in part be computerized. The aim is to maximize productivity. But that goal will not be met if the worker is intimidated, endangered, fatigued, scared, or alienated by his or her dealings with the machine.

After all, the terminal is a person's means of interacting with a computer—it can be thought of as the computer's eyes and ears. At the least, it must be harmless and businesslike. But it should also be as receptive and communicative as possible to enhance the worker's output. Clearly, then, it should be quiet, cool, easy on the eye (in several senses), and compact enough not to dominate the workspace and isolate its operator from other workers.

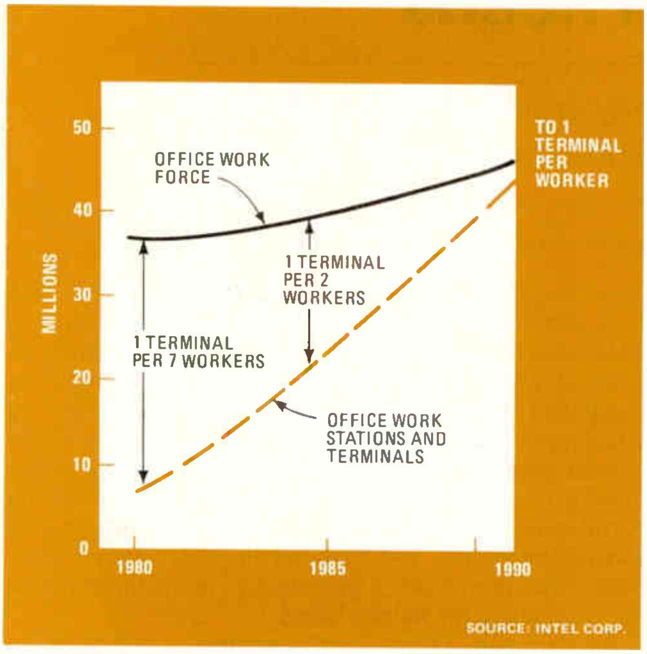
To translate those subjective criteria into physical facts, researchers have studied the hardware and software design of the terminal-to-user interface with a view to improving its physiological and psychological aspects. This body of knowledge is usually called ergonomics when it refers to the physical aspects of a piece of equipment and human factors when it describes the interface of application software with a user. Part of the current surge of interest in ergonomic terminals stems directly from the sophistication of both areas—the rising performance-cost ratios of semiconductor microprocessors and memories and advances in programming practices—that now make it economic to tailor the machine more closely to the human being.

As Norman Olson, staff engineering scientist in charge of human factors at Sperry-Univac, Blue Bell, Pa., says, "We can now afford to worry about how comfortable it is to use computer systems. No longer need we be limited by technology—by the performance

and cost of hardware resources—central-processing-unit power, memory, communications speeds, and display resolution and speeds have high enough performance-cost ratios to be used lavishly to this end."

A sample of the newest ergonomically designed terminals appears in Fig. 1. The major visible ergonomic features of these attractive products are low-profile, lightweight, detachable keyboards; bright, clear, flickerless displays with large, well-formed, highly resolved characters; great ease of use: and minimal obstructiveness, the whole terminal taking up as little space on the desk as possible and not totally blocking a user's view.

As for invisible ergonomic manifestations, the trend is to greater use of microelectronic intelligence in terminals to improve the way information is displayed—for example, by employing display processors and screen-refresh logic and buffering to improve scrolling. Often, too, switches and controls are replaced by programmable keys, and separate microcontrollers located in the keyboard itself limit the risk of breakdown by reducing the number of mechanical parts, improve performance, and allow the detaching of keyboards with only a simple, lightweight three- or four-wire cable.



2. Terminal, terminal everywhere. The number of computer terminals in use is growing much faster than the workforces of the U. S. and West Europe. In these estimates of the U. S. growth, the population of terminals will equal the workforce by the early 1990s.

German ergonomics standards set the pace worldwide

☐ Already a great many people in the U. S. and West Europe use computer terminals for much of the working day, and their numbers are growing rapidly (Fig. 2). In West Germany, for instance, 300,000 workers already operate the machines, and 1 million will probably be doing so in 1990. Similarly, in France, there are 260,000 terminals today and 600,000 are expected to be installed by 1985, not counting the 800,000 planned by the telephone company.

Much data has therefore already accumulated on the problems of the worker-terminal interface, and some of it has already culminated in recommendations, standards, regulations, and even laws on how computer terminals should be designed ergonomically.

Ergonomics, of course, antedates the computer termi-

1. Fancy features. The most common ergonomic features of the new computer terminals are tiltable, swivelable screens in small housings and detached, low-profile, and, perhaps, sculptured keyboards. But though carrying the same intent, they vary in execution from designer to designer.

nal by a good many years. It first became a serious endeavor during World War II, when teams of physiologists, psychologists, and specialists in clinical medicine studied the performance of military personnel handling the highly technological equipment then being introduced. One such piece of research focused on airmen making all-night bombing runs and how to modify controls, instruments, seats, and lighting to reduce the stress and fatigue and hence errors attributable to inept design. Much of this early work was done in Britain, where the term "ergonomics" originated, and the U. S. space program carried it further.

However, the application of ergonomics to computer systems got off to a slow start. As early as 1952, International Business Machines Corp., Armonk, N. Y., established an ergonomics department in one laboratory, and by 1960 most IBM research laboratories had one. Then in the mid-1970s, users in West Germany began to push for better-designed terminals.

Today, the guidelines used by most developers of new terminals stem from that country's Trade Cooperative Association, a rough translation of Hauptverband der gewerblichen Berufsgenossenschaften ev. Issued in October 1980 by the TCA's Central Office for Accident Prevention and Industrial Medicine, they are safety regulations for display workplaces in the office sector. There is an authorized English translation of them, plus a 38-page summary, which are available from the association in West Germany at 2000 Hamburg 60, Uberseering 8, Postfach 60 28 60.

The major terminal design requirements of the TCA regulations, which are subject to change as technology changes, are for: flicker-free displays; positive images (dark characters on a light background); nonreflecting screens; legible characters and phosphors; and low-profile, detachable keyboards (see table).

On Jan. 1, 1982, most of the TCA regulations became parts of the West German government's equipment safety laws. The rest will become legally binding only as soon as they become technically—and presumably economically—feasible, but no later than Jan. 1, 1985. To date, these laws, along with several DIN (Deutsches Institut für Normung), VDE (Verein Deutscher Elektroniker), and VDI (Verein Deutscher Ingenieure), standards are the only binding ones to exist anywhere in the world, says Klaus Buhmann, chairman of the TCA committee for establishing the video-workplace regulations.

The laws affect producers and importers of display terminals for use in West German offices (and office-like workplaces) by workers who spend their entire day operating them. "It is the intention of government authorities to see that they are adhered to," Buhmann avows.

Violators, he adds, are sure to be prevented from selling their equipment on the West German market at sometime in the near future. But this has not yet occurred. According to Jerry Ervin, systems manager at TRW-Datacom in Los Angeles, "European, including German, customers, will ask constantly for the ergonomic features that Germany and Sweden have come up with, but they are always willing to accept alternatives—nonergonomic terminals, small business computers, and personal computers."

Elsewhere in Europe

In other countries, of course, different philosophies and regulations obtain. Norway, for example, has more or less binding recommendations, whereas in Sweden, union officials keep an eye on safety. Sweden was also rather early in recognizing apparent occupational health problems with video-display terminals. In 1979 its Occupational Health and Safety Board established guidelines on lighting, rest periods, and the use of eyeglasses, focus on the legibility of single characters. But text readability is very different from and far more important than letter legibility. People read by fixating on groups of characters and words, and here smaller characters can help because they allow the reading and comprehension of more words per fixation, provided the display is viewed from near at hand. So maximum letter legibility—large characters, large screens, and long distances—may harm text readability.

Although almost all legislation, regulations, and recommendations for ergonomic terminals have to do with eye strain, to Charles Irby it seems as if they the regulators have not really identified the problem. "They are overlooking the fact that if you stare continuously at a book without resting, the same thing happens as when you stare at a video display," says Irby, who has degrees in computer science and psychology and is one of the user-interface specialists on the Star design team at Xerox Corp.'s Office Products division in Palo Alto, Calif. "It is not the display technology *per se* that is causing the problem. People get glued to the screen—that is the problem."

Another problem, according to Irby, is that the normal reading distance of books and papers is 18 inches (45 cm), whereas the normal viewing distance of a screen is 30 in. (75 cm) but the characters are often not much bigger. It seems that there are assorted solutions to some of the problems with video display terminals: make characters bigger or make the displays look like printed paper and bring them in closer, and, in any case, encourage people to take frequent, short rest breaks.

Matt Sanders, product design manager at Convergent Technologies, Santa Clara, Calif., probably typifies the U. S. attitude to ergonomics standards. Though he fears that very rigid standards could inhibit innovations, he concedes they remind manufacturers of operators' needs. Nevertheless, he says, "I am not thrilled about regulation on human factors—it should be part of a manufacturer's attitude."

Makers focus on human factors for present and future terminals

☐ Most of the newest computer terminals have good to very good physical user interfaces, but they are only just becoming available, particularly in the U. S. There are still opportunities for improved user-interface design. Also, there are many bad user interfaces. Good ergonomics in terminal and work-station design has become a competitive necessity.

Actually, good ergonomics is never such a positive attribute—it is more that bad ergonomics is so negative. As Sperry-Univac's Olson puts it, "you get no extra credits for manufacturing hygienic hardware." Yet it is extremely important to not do the opposite.

Ergonomics failures are like the dissatisfiers of classical management theory—something to focus on, complain about, and transfer other dissatisfactions to. If something is good, it is unnoticed: free coffee is unlikely to make workers decide to work at a company or to keep them there. But take it away, and everybody complains about what a lousy place it is to work.

Dissatisfiers really do affect performance and productivity. In the case of computer terminals, the worst offender is the CRT with its flicker, unwanted reflections, and inconvenient bulk. The keyboard, having been around longer, is less of a problem, except in Japan with its multiplicity of characters and ideograms. Future terminals, however, may eventually do without both tube and keyboard if flat-panel displays become economic and the computer can be taught to understand the spoken word.

Meanwhile, a number of companies have produced terminals that take the human condition seriously into account. The CRT in particular has received a substantial amount of study.

Ergonomic displays

The designers of Xerox's Star work station put a great deal of effort into making its CRT display look like a desk. Microcode is used to put a gray background on the Star display to simulate a desktop surface, eliminating the harsh, high-contrast black edges around displayed documents and icons (the small pictures of familiar office objects such as documents, folders, file drawers, in-baskets, and out-baskets that the Star employs). This makes the icons and display windows easy to read, and the display is restful, minimizing eyestrain.

The user can open an icon to deal with the object it represents. When opened, an icon expands into a larger form called a window, in which that icon's contents are displayed. Windows are the principal mechanism for displaying and manipulating information. Thus when the viewer "picks up a document"—in other words, opens up a display window and displays a page of the document—it looks like a piece of paper with printing on it. Also, he or she can inspect the contents of folders and file drawers and see what mail has been received, for example.

The surface of the Star desktop is organized as an array of 1-inch squares, 14 wide by 11 high. An icon may be placed in any square, so altogether 154 icons may be displayed at one time if the viewer likes a messy desk. The intelligent processor in the work station centers an icon in its square, making it easy to line up

4. Getting personal. Personal computers, like terminals, should be designed with the individual user in mind. This new line from Digital Equipment Corp. provides all the best-known ergonomic features in packages that keep the desk surface as uncluttered as possible.

5. Nordic designs. The Tandberg model 2200 from Norway (a) has been available in Europe since 1978 and is one of the most popular designs there. A terminal for the future (b) is in final stages of design at Nokia Computer in Finland.

icons neatly. The desktop itself always occupies the entire display screen; even when windows appear on the screen the desktop continues to exist beneath them.

The technology that contributes most to the Star user interface is the bit-mapped display screen. Bit-mapped displays require a lot of memory and fast display processing as every dot can be individually turned on or off by setting or resetting the corresponding bit in memory. Each dot may have several display attributes and several levels of depth associated with it. Therefore, for each dot on the screen, several memory cells are needed.

Bit-mapped displays offer the kind of dynamic and flexible graphics that help create a good user interface. Fortunately, memory costs are dropping fast enough to make high-resolution, multiple-attribute, bit-mapped color displays feasible for all terminals some day. But more than memory is needed. There must be a way to change the dots on the screen quickly. This requires a large memory bandwidth between the memory and the display and a fast processor to change the display memory. Dedicated microprocessors and microde can be employed to do this. The cost of these is coming down, too, as performance goes up.

At Convergent Technologies Inc., Santa Clara, Calif., a lot of attention was devoted to the display during the design of its work station product line. The company sells to original-equipment manufacturers, two of whom are (so to speak) officehold words in computers, Burroughs and NCR. Both introduced lines of small business computers based on the Convergent system—the Burroughs B20 line and the NCR WorkSaver systems.

Before designing the work-station product line, Convergent did a study to determine the most common desk environment. The designers built a simulation and brought in many people to test it. Convergent's team, headed by Sanders, also learned as much as they could about the state of the art of research on CRT human factors and found the German TCA regulations in use as a *de facto* standard throughout the industry.

The basics of user interaction with a CRT terminal drove the Convergent design. For example, the mainframe electronics had to be three boards—two Multibus boards and one optional memory board. A question was where to put them. If they were put under the monitor, it made the screen too high for comfortable viewing—studies have determined that as the eye, neck and shoulder muscles relax, the most comfortable line of sight is 30° to 40° below horizontal. If the electronics were mounted behind the screen, it made the display too deep, reducing drastically the flexibility of placement. If put in the keyboard unit, they made it too bulky—and also too much heat might rise into the face of the user, causing discomfort. If the main electronics were put off the desk entirely in a free-standing floor cabinet or rack, it would be too costly for some applications.

Convergent chose a 15-in.-diagonal screen and a large 10-by-15-dot character cell for legibility. A custom-designed character-oriented video subsystem was built [*Electronics*, Dec. 15, 1981, p. 151]. The P31 green phosphor display is refreshed at 60 hertz to eliminate flicker. The screen has an integrated, antiglare, optically coated glass filter that does not diffract emitted light and therefore does not distort the characters so carefully formed by the display subsystem.

"I believe in common-sense ergonomics," says Sanders. "I am not a crusader for ergonomics independent of cost and manufacturing considerations. If the cost of the product is too high—no matter how good the human factors are—too few operators will get the benefits."

In the Convergent work station, the extra cost of all the ergonomic features, such as the antiglare filter, the ball and socket assembly for the display, the detachable keyboard, and many more, is estimated to be $50 to $100 in additional material. According to Sanders, it probably does not take much to justify an additional end-user cost of up to $400 per operator so as to obtain increased satisfaction and productivity.

The new personal computers from Digital Equipment

Corp., Maynard, Mass., have a number of ergonomic features, for example, a small, tiltable monitor, detached keyboard, choice of phosphor colors, and a reflection-reducing filter. Ergonomics again was the driving force of the design. In the display area, Digital opted for a 12-in. screen in as small and light an enclosure as possible—it is barely bigger than the CRT itself. The goal was a display with built-in tilting, which was easy to move around the desk, would occupy little space, and would not block the user's view across the desk. The ergonomics designers claim that it was almost an edict from company president Ken Olson to "keep the work surface clear!" The only things on the desk with any of the four models of the Digital personal computers are the keyboard and the display (Fig. 4). The system box can stand beside the desk or be attached to the side of it. All models use the same display and keyboard.

The light small screen has a quarter-wavelength polarized filter bonded to the surface—the best available glare reducer, according to the Digital designers. Every aspect of the monitor was looked into: the shape and color of the surfaces, a copy holder attachable to either side, brightness and contrast controls, and optional phosphor colors (green, amber, or something else if the buyer wants it).

A concept of total ergonomics was applied to the personal computer design. Everything the user touches is designed to be easy to deal with—unpacking, setting up, daily use, and dependability (one of the biggest frustrations reported by workers using computer equipment and terminals is breakdowns). Moreover, its built-in diagnostics are readily understood, and any user, with no tools other than a pen or pencil to unlock the pressure-release mountings, can easily remove and replace the basic units. For example, at a Digital open house for employees, a nine-year-old correctly replaced a Winchester disk drive with the simple instructions provided.

There is color-coded identification of boxes, cables, and software for easy setup. Within Digital, the personal-computer family of products is, to date, the one that has had the most concentrated ergonomics effort.

Ergonomics has trickled down to the lowest-cost, high-volume video-display terminals. A couple of examples are the Viewpoint terminal from Applied Digital Data Systems, Hauppauge, N.Y., and the new Freedom 100 terminal from Liberty Electronics USA, San Francisco. The under-$600 Freedom 100, introduced earlier this month at the National Computer Conference in Houston, has all the physical ergonomic features that are becoming standard plus the smart attributes of more expensive terminals. The two-piece terminal consists of a 12-in.-diagonal, etched, green phosphor display and a 93-key, sculptured, low-profile keyboard. The 7-by-9-dot characters in a 9-by-12-element field are easy on the eyes.

6. Little one. Here is a small terminal with an integrated keyboard and display that has been designed expressly for casual users of information from computer systems. The Scanset personal information terminal, manufactured by Tymshare Inc., is as convenient and as manageable on a desk as is a telephone.

European bestseller

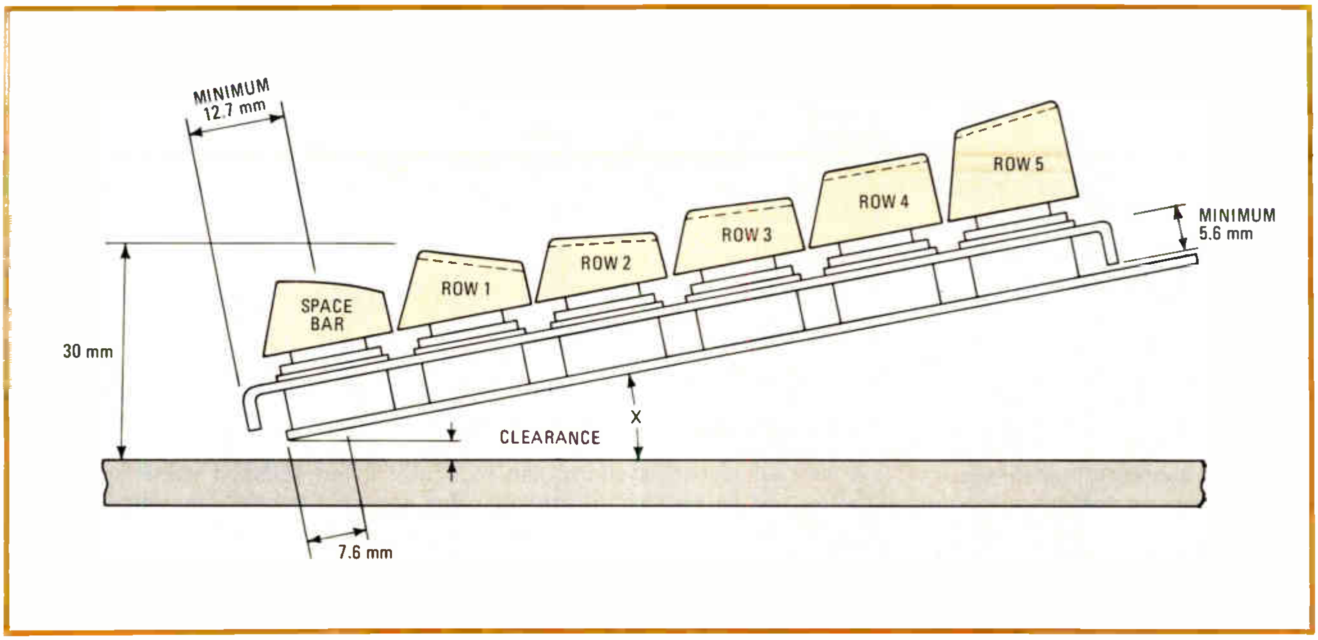
Another example of ergonomic design is one of Europe's most highly rated terminals, the Tandberg Data TDV 2200 family. The Oslo, Norway, company developed the terminal with professional users in mind—those who sit in front of terminals 8 or 9 hours a day. The designers worked with ergonomics researchers at the Technical University of Berlin in order to define the critical attributes.

Besides the requisite tilting and swiveling display and the detached, low-profile keyboard, the Tandberg terminal has been designed to work comfortably on a desk. The display has its intelligent electronics fitted around the tube to reduce the cabinet size. A patented feature of the display scanning electronics is its ability to blow up the dots on the vertical lines of characters to equalize the brightness over a character, making them easier to read.

It is a very soft terminal, with all the switches and display and character attributes controlled by an 8085 microprocessor, 64-K bytes of memory and 8-K bytes of firmware. Attributes can be set and changed either by the operator at the keyboard using a menu on the screen or by downloading from the host computer under program control. It is a single hardware product with many options and variations that can be added with firmware. This is one example of the big trend to very soft terminals combining these soft features with the physical ergonomics.

All the design considerations were driven by ergonomics. The Tandberg terminal and a similar one from Datasaab in Sweden, now Ericsson Information Systems AB [*Electronics*, Feb. 24, 1982, p. 101], are among the most popular terminals in Europe and have been available there since the late 1970s. Now, both designs are being sold in the U.S. because of the suddenly increased interest in ergonomics here. Figure 5 shows the Tandberg terminal and an experimental design from Nokia Computer Co. of Helsinki, Finland.

At Hewlett-Packard Co., Palo Alto, Calif., the German ergonomics regulations got the company motivated and focused. Its emphasis on ergonomics at all levels and groups has been growing the past two years. Originally, the company's European divisions started raising the ergonomics issue flag, because many ques-



7. The key. In order to move information efficiently from eyes to brain to fingers to computers, keyboards must be designed with a careful attention to details. Here is a profile design drawing of the latest ergonomic keyboard to be developed by Key Tronic Corp.

tions about ease of use started coming in from the customers and sales force. From HP's point of view there is no right solution for all users on some of the ergonomic issues, and it plans to offer a variety of solutions. It will give customers choices on screen coatings, various filters, and different colored phosphors while supplying the almost universally desired tilting and swiveling screen.

A very recent development in modifying display terminal screens to improve images and reduce user fatigue has been made by 3M Corp., St. Paul, Minn., and Datapoint Corp., San Antonio, Texas. It is a new lamination method for the video-display tubes designed for Datapoint's 8600 processors. This method basically involves laminating an orange filter to the screen of a yellow-phosphor CRT.

Yellow is used instead of orange or amber because it achieves a higher intensity with less power than other phosphors, Datapoint says. The reduction in power increases the life of the tube. The filter and special adhesives were developed by 3M. They are applied to the tubes by Zenith Radio Corp. for use in Datapoint's display terminals.

Key throughput

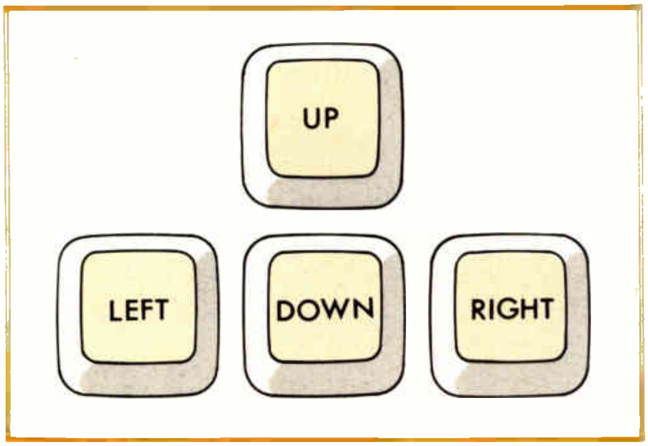
A keyboard is the fastest way now to deliver words to a computer, though other input devices are better for graphics input or pointing and moving. Consequently, keyboard design is very important for operator comfort and throughput. Keytop appearance, shape, legend readability, finishes, color coding, switchfeel, and pre-travel tolerances are critical. There is some controversy over the best height for keyboards and whether they should have a sculptured profile, and the question of standard keyboard layouts and characters is still wide open. But achieving consistent and acceptable ergonomics on keyboards is as important to keyboard and terminal makers as reliability, price, and delivery.

Detached keyboards are considered essential for operator comfort in high-use applications. However, attached keyboards may be better for compact desktop terminals for occasional use—too many pieces of equipment on the desk can be a nuisance if the terminal is only used, say, 10 minutes every other day, says Richard G. Thau, equipment product marketing manager of Tymshare Inc., Cupertino, Calif. His firm has recently introduced a small, integrated terminal with a lot of one-button functions for casual users of information from computer systems (Fig. 6).

With respect to keytop shapes, Key Tronic Corp., Spokane, Wash., evaluated many possible shapes for its new low-profile keyboard. The designers talked to customers and prospects and showed them models of six different shapes over the past year. They decided on a scaled-down version of the IBM Selectric III keytops. This is a sculptured keyboard shape (Fig. 7), which was a clear preference of the users questioned and apparently also of many major terminal and computer makers. It is seen not only on IBM's new typewriters but on the IBM Personal Computer and on Apple's new computers.

HP has initiated a keyboard standardization program within the company. The goal is to try to establish consistent keyboards over the entire product line—common layouts, mnemonics, symbols, and terminology for common functions. This is also a goal at Burroughs Corp. of Detroit. Its newly established Human Factors Laboratory in Plymouth, Mich., will work on ensuring that the same key will be used for the same function across the entire Burroughs product line. This has not been true in the past, with individual designers each doing his or her own product design. Most of the major computer companies now have ergonomics groups staffed with psychologists and human-factors specialists.

The keyboard of Digital Equipment's new Personal Computers is painted a light color to match the general



8. Best position. Moving a cursor or pointer around the display can be done with a variety of input devices. If it is to be done with special keys on a keyboard, then the arrangement of the four keys for the four directions of motion is important. This inverted-T arrangement developed by Digital Equipment is efficient for finger positions.

brightness of paper. It is a low-profile, detachable unit with cable plugs on both sides to make it convenient for both right- and left-handed people. On the basis of tests of keystroke frequencies of four-key cursor controls, the designers chose an inverted-T design (Fig. 8) located just to the right of the main keyboard as the best design for keyboard control of a cursor—it is easy to manipulate with just three fingers, the first on the left key, the second on both the down and the up keys, and the third on the right key.

Of mice and men

There are other ways besides keys of pointing and drawing on displays. One of the areas studied in depth on the Star work-station design project at Xerox was pointing devices. Systematic testing of performance, error rates, and learning problems was done with a variety of subjects using about eight different pointing devices. Cursor step keys were found to be too slow and really unsuitable for graphics input. Finally the Star mouse with two buttons was chosen. It is a Fitts's law device, for it matches the fundamental bandwidth of the human psychomotor nervous system—in other words, it feels as natural and works as well as a pencil in the hand, with just a little practice.

Other positioning, pointing and drawing devices such as tablets, styluses, light pens, touch-sensitive screens, and joy sticks are often used with terminals to complement keyboard input. They are most often used as graphics input devices or for computer games. They will often reduce the flexibility of the work space because they require either additional desk room, or, like light pens and touch screens, a fixed physical relationship between the user and the screen. Some alternative input devices used now tend to violate one of the main ergonomics principles: that is, the need to maintain flexibility in the physical relationship between user and terminal because of the impossibility of designing a fixed, optimal relationship for all people.

As computer applications are developed for tasks at all levels of an organization, the standard keyboard becomes less viable as the all-purpose input device. Other input and control means will have to be perfected or developed since all the answers are not yet in. A tablet and character-recognition logic for the input and recognition of the strokes in Chinese-character writing is still a big problem, for instance. Other important ergonomics considerations have to be addressed for handicapped people and those who wear bifocals.

Speak up

The ease with which computers can be used will take a big leap forward when they can understand human speech. Voice recognition by computers is around today on a small scale. Some systems can understand words spoken by individual voices when they have been trained to recognize them. Others, called speaker-independent systems, can recognize a few selected words spoken by almost anyone. But none are generalized voice-recognition systems, and most cost too much except for some special applications.

Development of voice-recognition systems is moving towards what is really needed—a voice-independent input device capable of 100% recognition of all words spoken in any language. Generalized voice recognition is one of the key technologies being studied and developed for Japan's fifth-generation computer project [*Electronics*, Nov. 17, 1981, p. 83].

Early applications of voice recognition will be in hands-off situations for capture of small amounts of data or the issuing of a few commands. Ron Stephens, president of Votan Inc., Hayward, Calif., calls them "busy eyes, busy hands applications". In September, Votan will be introducing a low cost speaker-independent voice-recognition system with very close to 100% recognition of the digits 0 through 9 and eight command words, including yes and no. The Votan system uses digital signal processing and dynamic programming. It achieves speaker and language independence by collecting several thousand utterances of a particular word by a variety of people. This sample is then statistically analyzed to form a template for the word that best represents a composite of all the voices in the sample.

Speaker-independent voice-recognition systems like this new one from Votan will, when linked with voice-verification systems, be useful in computer-based transaction-processing systems using that familiar terminal, the telephone. An untrained public will be able to access data bases, control equipment, send voice mail, and conduct banking, shopping, or reservation transactions over the telephone, says Stephens. The Votan speaker-independent voice product will be available as a board-level product for under $2,000 or as part of Votan's voice development systems that contain other options, such as speech synthesis for voice output and voice store and forward for voice mail.

Some implications

Voice recognition is not at the stage where it can begin to replace keyboard entry for high volumes of data and text. It could be used now in special applications to command and set up machines or select from a menu; it could be very useful in partly automated industrial con-

9. Color, too. Ergonomics principles are being applied to color graphics computer systems, too, as this Florida Computer Graphics system shows. In addition, bringing color graphics to computer systems is another ergonomic feature in itself, since people enjoy color.

trol situations, in cockpits of aircraft, in trucks, buses and automobiles, and in computer-aided design and automated drafting systems—in short, any place where an operator's hands are busy doing other things.

It is generally agreed that voice input to computers will be a big ergonomic asset to computing—once it becomes extremely reliable and cost-effective. As IBM's Rupp puts it, "Voice recognition has been just around the corner for 20 years. However, it would be a boon to computing." It probably will not be just around the corner for another 20 years, because the ever-rising performance-cost curve of microelectronics and the application of sophisticated mathematics to the problem will make it cost-effective for many more applications within the next three to five years.

In the U. S., several small companies are basing their business on voice systems and the large computer companies either have voice research and development projects or are closely watching developments. In Japan, voice has a very high priority. An official of the Electronic Industries Association there thinks voice recognition is at most three years from the market. In Europe, voice input is a greatly desired alternative to keyboards, especially among executives who have a cultural aversion to keyboards. A French commission has just recommended a 14-project national plan for the nation's electronics industry that includes a project for speech recognition and synthesis and one for data-processing ergonomics [*Electronics*, June 2, 1982, p. 105].

Another use of computerized voice technology for easing the human interface with computers are systems that can digitize and store messages spoken by the operator. An example is the ergonomically designed processor from Office Technology Ltd. of Winchester, England. This word processor and office terminal accepts oral annotation of text documents, stores and forwards voice messages, and takes dictation.

There are several display technologies that promise some day to provide a bright and clear alternative to bulky CRT displays. Technologies such as liquid-crystal, plasma, electroluminescent, neon gas, and electrophoretic displays can be made in thin, flat panels, giving terminal designers new freedom for ergonomic designs. (Electrophoretic display technology involves a black colloidal solution with white particles suspended in it, encased in small cells; an electrical charge can cause a cell to go all white or all black.) However, these display technologies still cost much more than CRTs, which are manufactured economically in very high volumes. Also, some of them need further technical development to increase brightness and resolution in larger sizes.

Future faces

It will still be many years before any of these flat-panel displays will cost-effectively replace CRTs in most high-volume terminal applications. The big advantage in thin displays is the reduced volume over the CRT—though thin CRTs are being developed also. Where bulk is an important factor, the flat displays are beginning to be used. Some examples are portable terminals, hand-held computers, retail point-of-sale terminals, and terminals for use where space is a premium, such as pharma-

Packet switching can save money

Like all data-communications networks, a packet-switched net may be characterized as a collection of nodes and interconnecting communications lines. Its connectivity is not restricted, except for hardware limitations in the number of lines that may be physically connected to a given node. The nodes themselves are usually composed of minicomputers or a collection of microcomputers, with software sophisticated enough to be able to route packets of information across the trunk lines connected to the node.

The protocol imposed on the access line between data-generating and -receiving equipment is the X.25 protocol defined by the International Consultative Committee on Telegraphy and Telephony. The economic advantage from this arrangement is simple. The cost of sending a given amount of data for example over a 56-kilobit-per-second line is much lower than the cost of sending the same amount of data over a 9.6-kb/s line—providing that the 56-kb/s line is fully utilized, as it can be with packet switching.

The idea is that many users can aggregate their data transmissions onto a few high-speed trunk lines. That is, each node will be connected to enough data generators and receivers so that the aggregate data rate will use the trunk lines enough to realize the cost savings.

Packet-switched networks also can automatically route around line and node failures. From the user standpoint, only the node itself and the line to his equipment remain vulnerable to outage. Because the line to the network is usually short, it becomes economically feasible to use redundant lines from the equipment to two different network nodes, thereby providing a high degree of reliability.

new original-equipment-manufacturer application.

The software for this Z80-based interface is carefully fashioned to help achieve a throughput capacity of 100 data packets a second—enough for most practical applications. Moreover, the network link can run as fast as 19.2 kb/s without DMA chips and up to 56 kb/s with them. In either case, a data packet passing through the interface system is delayed less than 5 milliseconds, also a figure adequate for most applications.

The hardware configuration takes full advantage of the Z80's capabilities. This 8-bit central processing unit has a 16-bit-wide addressing capability and an I/O architecture with bit, byte, word, and byte-string operands (158 instructions in all). The CPU consists of 12 general-purpose registers (two banks of six) with dual accumulators, flag and index registers, a stack pointer, a program counter, a RAM refresh register, and a table-pointer register handling interrupts. It is made with a mature, hence inexpensive, n-channel MOS technology.

Especially useful for the X.25 interface is the ability of the Z80 and its family of peripherals to support up to 128 true vectored interrupts. Each peripheral may thus supply a unique identifying vector for interrupt acknowledgment, thereby allowing the use of state-transition tables for the software design. As well as simplifying and speeding up ISRs, such tables facilitate development of error-checking software in the form of exception-driven input processes. This type of error checking frees the system of time-consuming and redundant polled error-condition processing.

The dual-channel SIO is likewise suitable for interrupt-driven error checking, as it can generate up to four different process interrupts per channel. These interrupts are: transmit buffer empty; receive character available (in three modes); external status change (five sources); and special receive conditions, including parity, overrun, framing errors, and end-of-frame signals. The SIO can handle asynchronous protocols, as well as HDLC and Bisync. With internal hardware support, it can generate cyclic redundancy checks and zero insertion/deletion in either channel at data rates of up to 880 kb/s.

The second generation of the SIO, the serial communications controller (SCC), with built-in bit-rate generators, synchronous encoders-decoders, and phase-locked loops, has just gone into production. All the other ICs in the system have been available for some time.

Like the SIO, the SCC may be used in a wait-ready handshake mode with a DMA chip. The DMA IC may be used to support high-speed data transfers, up to 1 megabit a second thereby reducing bus overhead for data transfers to less than a fifth of that in systems relying on the Z80 CPU alone for such transfers.

Like the DMA, SIO, or SCC, the four-channel CTC can generate vectored inputs for communication-line timeouts or system clock pulses. Another useful feature, exploited in the interface system built for the IBM Series 1 computers, is the CTC's ability to serve as a middle man for interrupt signals. Three of its four channels accept triggers and can interrupt on either a rising or falling edge of those signals. Therefore, the chip can be incorporated as the interrupt logic in special-purpose interfaces with the Z80.

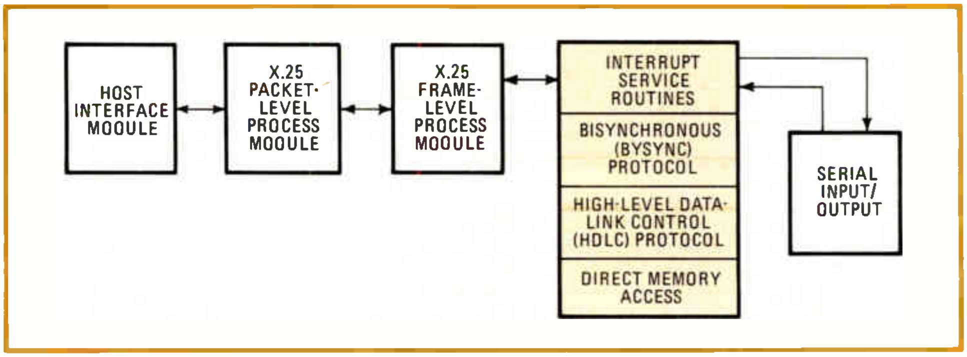
Dealing with complexities

The software of the Z80-based X.25 interface takes into account the many subtleties of a packet-switching net. For example, the restart, clear, and reset packets must be circulated in a timely manner between the net and the host. The need for this synchronization arises for operations in which the Z80 itself issues one of these packets to both the net and the host. Then the CPU must wait for confirmation from both before proceeding.

Another example is the negotiations necessary to fit the message coming from the data generator to the size of the data packet specified by the X.25 network. Not all OEM equipment can perform these negotiations, and so a data generator may try to send a message too large for a packet. In addition, different nets tend to have different defaults for packet and window sizes. The software for the Z80-based interface resolves all these differences with initialization parameters.

Diagnostics is another example of an X.25 subtlety that must be acknowledged in the software. For example, restart, clear, and reset packets may carry a diagnos-

2. Program modules. There are four major software modules in the Zilog X.25 interface. The interrupt-service-routine (ISR) module has software subsets that handle the Bisync or HDLC protocol, as well as direct memory access.



tic code in octet 5 of the packet. Not all networks support these diagnostic fields, however, and others will support diagnostics in one type of packet only.

Hardware-related complexities also must be solved by the software. For example, register saving and restoring on the Z80 is inconvenient, because there is no single instruction that will save and restore all the registers at once. The software must therefore include one save and restore instruction per register.

As for system memory, the Z80 offers users a choice: entirely dynamic RAM or read-only memory in addition to contain the operating-system code. Therefore the X.25 interface's software must separate code and data in the event the OEM opts for the RAM-ROM configuration.

The use of dynamic RAM also has implications for applications incorporating DMA. The burst and continous modes of these ICs can control the Z80 bus for long enough so that the RAM refresh cycle generated by the CPU is lost. In practice, the data rates of communications applications are low enough so that this mishap is unlikely. In fact, they are low enough so that these high-speed modes of DMA operation usually are not needed.

Performance goals

The system was designed to support a 56-kb/s access line using DMA or a 19.2-kb/s line using byte-at-a-time programmable I/O. In either case, the throughput should be in the neighborhood of 100 data packets a second.

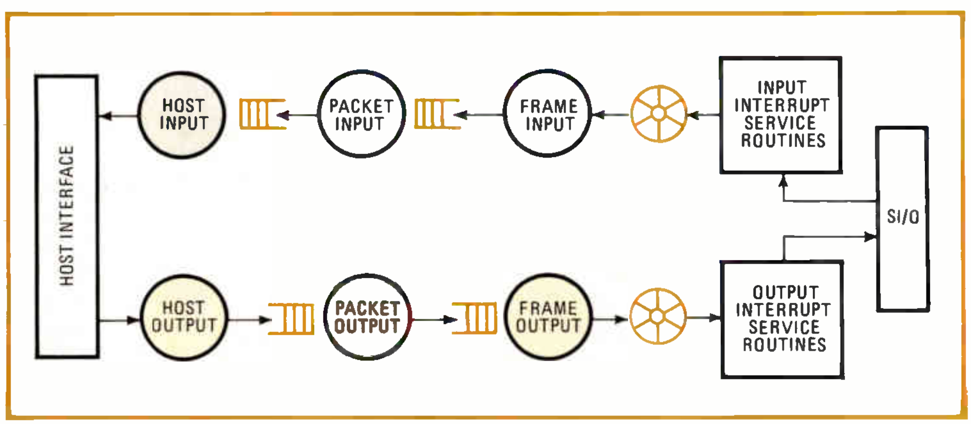
To meet these goals, the first design decision was to organize the software along the lines suggested by the data-flow diagram of Fig. 3. This diagram suggests that the system naturally breaks down into a series of modules, each performing one stage of the processing of data as it flows from the host to the net, or vice versa.

The framing (Fig. 4) of the data bits is done by the ISRs in conjunction with the SIOs using either HDLC or transparent Bisync framing conventions. A background process (one that does not run at interrupt time) processes the frame's content. With this separation of functions, the background process is not sensitive to the framing conventions used on the link to the network. Thus, for example, the differences between the HDLC and Bisnyc protocols are isolated in the interrupt routines of the X.25 interface.

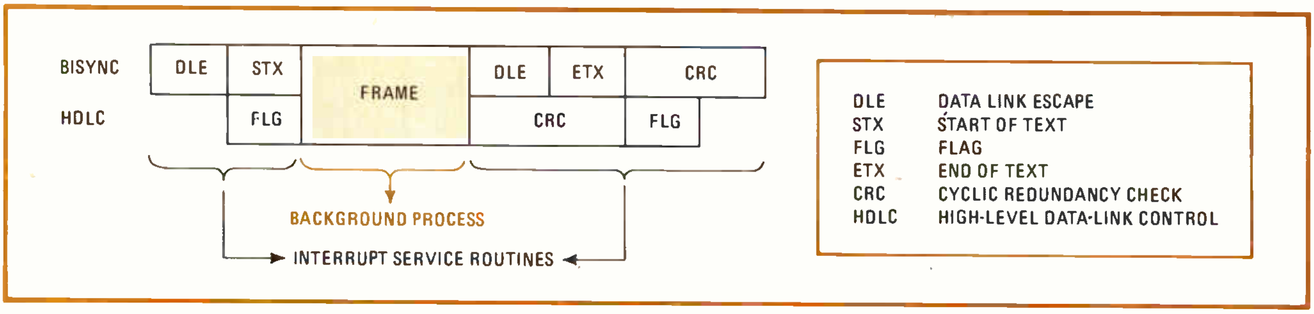
The background process realizes a finite-state machine that models the frame-level procedures. The representation of the state machine is a two-dimensional table of routine addresses. In this table, the first index is by state and yields a pointer to a row of routine addresses for that state. This row is, in turn, indexed by an encoding of the triggering event. The events are encoded by assigning a small integer to each possible frame type. From the packet-level side of the frame-level process only information frames are sent. Therefore, the state machine for this direction of flow has only one event, "send I-frame," implemented without using the formal mechanism of the state machine.

At the packet level, each logical data-communications channel is assigned a table entry containing its state information. This information is frequently referred to by the packet-level software in the processing of a packet for a given channel.

The table is organized using a single-entry cache at a known location in memory. First the old cache contents are written into the table to preserve modifications of the previous contents and the cache is then loaded from the entry corresponding to the requested logical channel. This setup allows the packet-level software to access



3. Data flow. The modules of the Z80-based X.25 implementation regulate the flow of data from one process to the next. By convention, a circle is a process, a washboard is a linked-list queue, and a donut is a circular queue.



4. Frame processing. Depending on whether data in the Bisync or HDLC protocol is being converted to a packet format, the software in the Z80 interface must perform different chores, either by background processes or ISRs.

elements of the channel's table entry without pointer-based constructs. Such a simple access, in turn, reduces the amount of the code in the packet level—the largest module of the system—as well as its execution time.

An important design goal for the software is to reduce the processing time for each packet. Saving milliseconds at design time means that it is not necessary to refine the code to save microseconds in each procedure. In fact, most of the system is written in a high-level language, PLZ (with C-language translation in progress), for easing of software generation and modification. Time-critical routines are written in assembly language, but they are kept to a minimum.

Saving time

There are three areas in which the software design saves packet processing time. They are processor scheduling, process synchronization, and buffer allocation. Together they save about 10 ms per packet.

The processor scheduler is a nonpreemptive, run-to-completion algorithm. No process can be preempted by another, and it will control the CPU until it has finished. Each process is responsible for saving its state when it does return control to the scheduler.

The process synchronization is kept as simple as possible. No synchronizing primitives are necessary because processes are not run in interlaced fashion in this system. Moreover, no locking mechanism is needed on resources such as table entries, because only one process at a time can access them.

The refinements in these two areas save considerable overhead time. Counting acknowledgment at both frame and packet levels, there are eight steps in the processing of a data packet, and an implementation with preemptive scheduling and synchronization primitives could take about 1 ms to "wake up" a process. In the Z80-based interface, the overhead is under 100 microseconds.

To further minimize processing overhead, the software uses a simple buffer-allocation scheme. Based on an initialization parameter that determines the maximum packet size, this scheme claims all available memory for fixed-length buffers at the point when the interface system is initialized.

The software chains the available buffers together in a linked list, so that obtaining one is simply a matter of removing it from the list. This linking scheme contrasts to general-purpose allocators that parcel out memory space in various sizes and then recombine spaces that are released. Such a memory allocator can easily become a multimillisecond procedure, slowing down the system.

With a 4-MHz Z80, the capacity of the system is about 100 data packets a second. There are, of course, a number of system variables that can speed up or slow down this throughput.

To begin with, about 10 ms of overhead is involved in the processing of each data packet under the least favorable conditions, in which the software must process the maximum number of possible acknowledgments. However, the inherent delay due to the processing that must be done on a data packet from the time it first arrives at the SIO until it is sent to the host is 5 ms. In this ideal setup, with no separate acknowledgment packets or frames generated, the throughput could be 200 data packets/s—but because there is likely to be acknowledgment overhead, the 100-data packet/s figure is more realistic.

Another important influence on throughput is the use of DMA. Without this feature, the system at best can operate at 19.2 kb/s. The programmable I/O necessary in this setup requires one interrupt per byte, so the interrupt load at 100% full-duplex usage consumes 24% of the available CPU cycles. Thus, only 76% of the CPU's cycles are available for background processing, reducing throughput to roughly 76 data packets/s.

Using DMA, the interrupt load is negligible, and the system will exhibit a capacity of 100 data packets/s. A 56-kb/s line, driven at 100% capacity in both directions, cannot achieve this throughput unless each packet contains 113 or fewer bytes of data (or 56 bytes at 50% capacity). Alternatively, a fully utilized channel of 256-byte data packets would require a throughput of only 50 data packets/s.

Memory allocation is also subject to system variables. For example, a system with 32 logical channels occupies 26-K bytes of memory space, with each additional 32 channels requiring 1-K byte for table space. The frame-level software for this system occupies about 7-K of the 26-K bytes; the packet-level software about 8-K bytes; and the host module for an IBM Series 1 requires about 5-K bytes (including interrupt routines). Static variables, including the logical-channel table account for another 2-K bytes, leaving the remaining 4-K bytes to go to stack, interrupt-vector, and miscellaneous routines.

The balance of the memory can then be used for buffers. In a system with 32-K bytes of space, there could be about 50 buffers with a maximum of 128 bytes per packet, and in a 48-K-byte system, there could be about 85 buffers with a maximum of 256 bytes per packet. □

Multiuser microprocessor systems get a data-base manager

Sophisticated hardware and software control disk resource while managing data base and files

by Eugene Lowenthal, *Intel Corp., Austin, Texas*

☐ Yet another mainframe support tool is migrating to the microprocessor environment: the data-base processor. It is being introduced at a time when the industry is recognizing that microprocessor-based multiuser systems now have the power and capacity to support the complex, large problems that have been the exclusive domain of mainframe computers. However, these small microprocessor-based systems have outstripped the capabilities of available support software.

In particular, there is a vacuum to be filled with respect to sophisticated data-base management systems capable of supporting shared access to data by multiple terminals, programs, and applications. The iDBP 86/440 data-base processor [*Electronics*, March 24, 1982, p. 44] is the first of a family of such systems that will be designed to fill that vacuum.

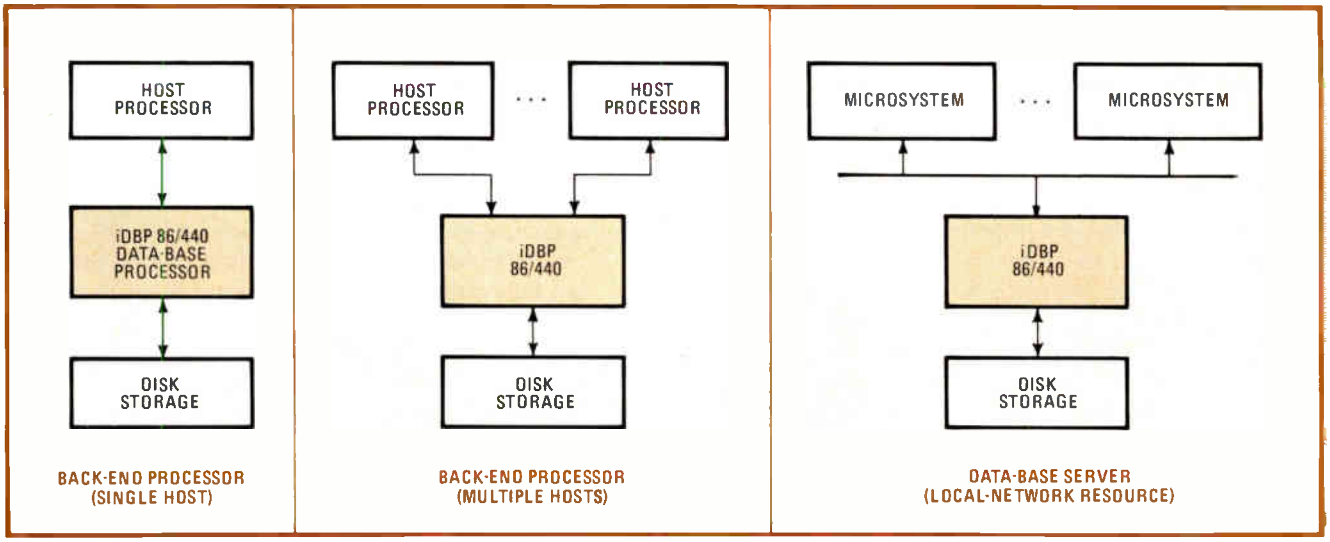
In addition to controlling a shared disk resource for the host computer or computers, this microprocessor-based peripheral system offers comprehensive data-base and file management. Consequently, the designer who integrates the iDBP into an end product can focus on the application—without concern for the mechanics of data-storage techniques.

The iDBP is a building block for the product designer, rather than an end-user system. Intel's objective for data-base machines (and the systems business in general) is to provide high-level building blocks for system integrators and value-added resellers. Thus the iDBP will not appear as an end product, but as a subsystem incorporated within a total system offering developed by Intel's customer. Consequently, the design of the 86/440 accommodates interfaces with a wide spectrum of hosts.

A building block for OEMs

The iDBP will be designed into minicomputers, small-business computers, networks of small computers and work stations, and integrated office systems. Only in rare instances will it be appropriate to connect it to a large mainframe or an isolated single-user system (work station, personal computer, and so on.)

The 86/440 is particularly well suited for integrated office systems. It fills the large gap between software developed for managing text in word-processing systems and that developed for managing records in data-processing systems. Storage-management facilities for office networks must marry both disciplines. In fact, no meaningful integration of word and data processing can be undertaken until there is a common mechanism for managing and relating both record-oriented data (for data processing) and stream-oriented data (such as text,



1. Building block. The iDBP can be connected to a host processor as a back-end processor (left), as a data-base server for a network of microsystems (right), or as an embedded system transparent to users. This versatility makes it a high-level building block.

digitized voice, digitized images, graphics representations, and the like). The iDBP provides this common mechanism for a system to which it is attached.

An important design consideration was to provide a general-purpose building block that could be incorporated into a variety of original-equipment-manufacturer systems (Fig. 1). The iDBP can serve as a back-end processor dedicated to a single host, possibly integrated within the host enclosure—a superintelligent controller.

Adaptable to many different hosts

It can also serve as a back end that is connected to multiple hosts, possibly of different brands—a multiport back end. This configuration is the only efficient way that applications running on different computers can share data, particularly in a heterogeneous configuration of machines.

Finally, it can be a special node in a network. There it is a data-base server, which is a shared network resource that allows all users access to a common pool of information on disks.

The 86/440 is designed to handle large data bases, having files that are individually hundreds of millions of bytes long—but not those that are measured in billions of bytes. It is currently oriented to commercial and office applications, rather than number-intensive scientific uses. Also, the flexibility designed into the host interface is not present in the disk interface. The iDBP supports a broad but specific class of storage devices.

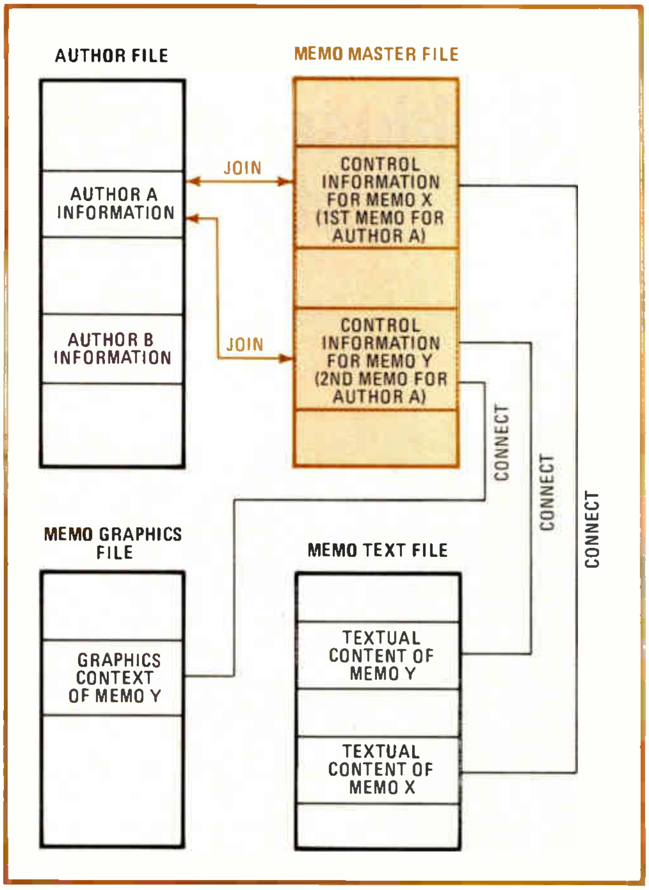
In addition, it does not support transparent distributed data bases. Data transfers from one unit to another, if desired, are initiated not by the 86/440, but by the host to which it is attached. Likewise, the consolidation of data from multiple iDBPs to satisfy a global query is also the responsibility of the host.

In designing the data-management software, the first question was the choice of data-base definitions and manipulation languages. A relational interface was chosen because it accommodates extremely high-level data-manipulation commands, including those that can operate on entire sets of records in a single step. This is in marked contrast to the typical navigational interfaces, which are lower level and require that individual records be addressed only one at a time. The net effect of using the higher-level interface is a dramatic reduction not only in the size and complexity of applications programs, but also in traffic between the host and iDBP.

Division of labor

By its very nature, the iDBP imposes a division of labor whereby the function of data-base management is separated from the user interface. In the distributed environment for which it is intended, other machines—the hosts—contain the software and hardware that provide the bridge between the user and the data-base processor. Since a bridge must be developed in any case, there is no requirement that the relational nature of the 86/440 must be apparent to the end user if there are good reasons for doing otherwise.

If, by virtue of technical preference or past history, the designer is committed to providing a network or a hierarchical style of data-base management in his product, he or she can superimpose it over the relational personality of the iDBP. In fact the iDBP has some special features just to support these nonrelational styles. Chief among these are data-base pointers, which allow records to be addressed by location as well as content, and list-processing primitives, which allow structures of records to be built and accessed by means of such pointers. These mechanisms are completely in violation of the formal rules of the relational model. However, they can simply be ignored if the iDBP is designed into a purely relational end product. The point is that iDBP itself need not be purely relational because the customized host software will act as a filter between it and the user.

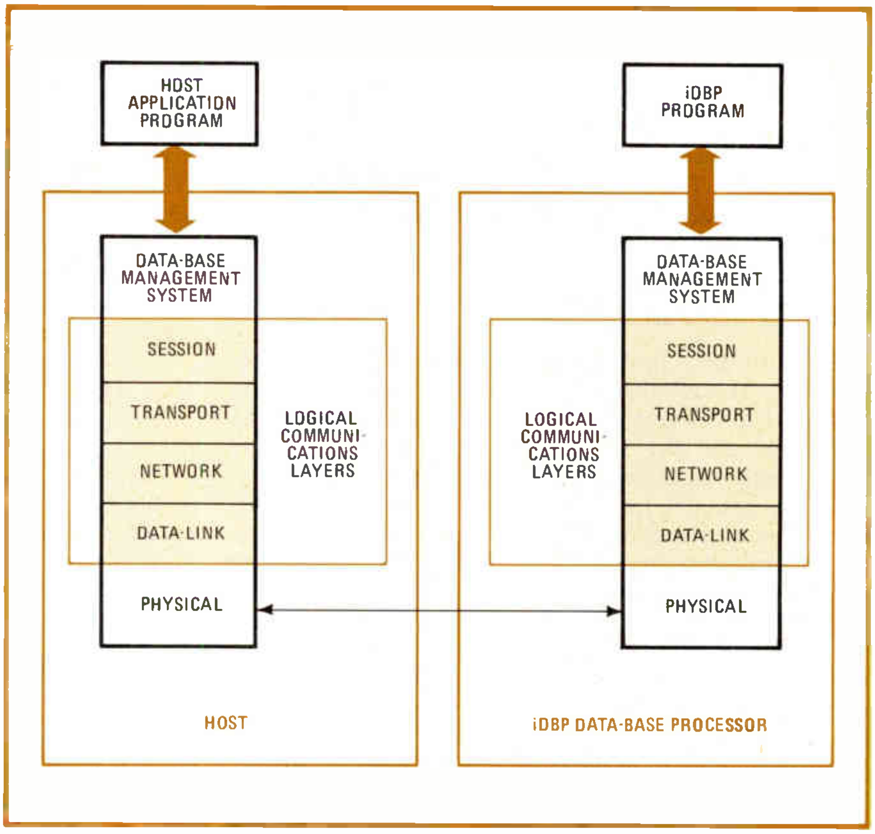


2. Heterogeneous elements. Data-base managers ordinarily focus on either records—data processing—or strings—word processing. The iDBP allows mixing of both using join commands—relating like elements—and connect commands—relating unlike ones.

Another important departure from traditional data-base management (relational or otherwise) is the ability to manipulate individual files. That is, a user creates files and then may aggregate them into data bases to exploit interfile relationships.

However, a given file need not belong to any data base if there are no relationships with other files. Conventional data-base management, in contrast, starts from the notion of an inclusive data base and does not readily accommodate the existence of unincorporated files.

More importantly, these files do not have to consist of records. That is, a file need not be described in relational terms, and its structure, if any, is not known to the iDBP but is interpretable only by software in the host. For



3. High-level communications. The strategy of using a multilayered protocol for the host-to-iDBP interconnection provides great flexibility for the OEM in choosing a specific interface. It also ensures the necessary framework for reliable communication among concurrent tasks executing in the iDBP and its ensemble of hosts.

example, the file might contain a document, a Cobol source library, an array of graphics vectors, or a store-and-forward message queue.

It is important that the iDBP accommodate such arbitrarily structured files because it will be used in small systems where separate subsystems for data bases and files would be too expensive. In local-network environments, data-base servers will also have to manage both data bases and individual files. What's more, the iDBP offers some special extensions to the relational model, which allow these files to be searched, manipulated, and even integrated within a data base.

An unstructured file is treated simply as a string of bytes. Individual substrings can be retrieved and updated, and there is an extremely versatile pattern-search capability for isolating substrings that satisfy the search criteria.

The most radical departure from strict relational principles, however, derives from the unique ability to establish relationships between structured and unstructured files. Fields within records of one file can refer to substrings in other files. Just as the Join—a relational operator command—creates a new file by concatenating records from two source files, the iDBP's Connect operator creates a new file by concatenating records with substrings. For example, a file each of whose records controls a single memorandum in an electronic mail system can connect to one file that contains the textual body of a given memo, connect to another that contains each memo's graphics content in digital representation, and be joined to yet another file of information about the author of the memo (Fig. 2).

The simple ability to interrelate record-oriented information with stream-oriented information under a common data-base discipline will change the way designers perceive the necessary solutions in a number of significant application areas, including office automation and computer-aided design. For the first time, they will be able to think of the organization, access, and control of their information in data-base terms. The cost of developing these applications will diminish dramatically as a consequence of this capability.

Although the iDBP does have a number of unusual features, in most respects it offers the same facilities found in mainframe data-base management systems. Among these are:

- An integrated data dictionary and directory.
- Coordination of concurrent access by multiple users.
- Recovery mechanisms that include save-restore, roll-forward, and automatic roll-backward.
- File-paging algorithms to minimize disk input/output operations.
- Data-base security and integrity mechanisms.
- Performance options like hashing and indexing.
- Data independence, so that the exercise of any performance option will not require changes to the data-base design or application software.
- Integrated sorting and merging.
- Macroinstructions—the ability to define, catalog and invoke frequently used command sequences.

The emphasis on application sophistication clearly differentiates the iDBP from the very simple data-base management systems that are well-suited to personal computers or small-business computers. The 86/440 addresses the more demanding needs of multiuser and network environments. Its capabilities are commensurate with the computational power and storage capacity of such systems.

The challenge in designing the iDBP's interface to the hosts it serves was to select a single strategy that would most easily accommodate a very wide range of system environments. The strategy had to be independent of the host. It also needed to support a spectrum of iDBP roles, from back end for a single host to data-base server for hosts in a heterogeneous network.

The interface's architecture

The answer is a multilayer communications architecture (Fig. 3), such that the full protocol would be used in a network environment and a compatible subset could be configured for the simpler back-end (point-to-point) applications. However, even in the simplest case of a host-iDBP pair, the functionality of the interface must be rich enough to support multiplexing several concurrent dialogues on a single line. This requirement arises from the multiuser nature of the 86/440; that is, several processes in a host can be communicating with corresponding prcocesses in the iDBP on one party line.

The interface also must support reliable delivery of information in both directions, through data-integrity checks and error-recovery mechanisms. This capability is particularly important when the iDBP is used in applications where it is remote from the host.

The communications architecture is typical in that the session, transport, network, and data-link layers are responsible for providing these generic communications services. The layer for data-base management, however, is unique to the iDBP. At this level, the host transmits groups of commands to define access or control files, and the data-base processor returns groups of responses (data and status).

The ability to aggregate commands and responses serves two important purposes. First, communications overhead is minimized because throughput is affected more by the number of transmissions than by the size of each message. Secondly, entire "programs"—sequences of data-base–management commands—can be swallowed up and executed by the iDBP. To complement this capability, branching (if, then, else) and looping instructions have been added to the command set. When decision making and loop control can be offloaded to the 86/440, the traffic on the interface drops dramatically.

Another important benefit of a layered communications framework is the flexibility that derives from the independence of the various layers of the protocol from one another. In particular, new data-link or physical layers can be incorporated as required without modifying the higher layers. So, for example, Ethernet, RS-232-C, IEEE-488, or even a highly customized channel interface can be implemented without reworking the overall communications approach. This partitioning of the protocol is reflected in the modularity of the software and hardware in the iDBP's communications subsystem.

The 86/440 employs a multiprocessor organization (Fig. 4). Several microprocessors execute the complex software and firmware routines that provide the product's functionality. The standard Multibus is the internal high-speed bus used by each processor to communicate with other subsystems and the global memory resource. From a mechanical standpoint, the product is available in several packaging levels, ranging from a board set to a fully enclosed system that is appropriate for applications in the office.

An 8086 configuration

The heart of the system is a processor subsystem constructed around an 8-megahertz 8086, which executes the software of the data-base management system and the operating system. This microprocessor resides on a printed-circuit board that also has the bootstrap read-only memory, diagnostic ROM, RS-232-C diagnostic port (for local or remote service), and 128-K bytes of random access memory. The 8086 can access a 512-K-byte memory board across the Multibus. An additional 384-K-byte memory board can be configured to increase the size of the buffer pool and support more users. All of the RAM modules have error-detection and -correction circuitry to ensure data integrity.

An iDBP can have one to four disk controllers, where each controller is a pc board whose main element is an 8089 I/O processor. Each of these units can handle up to four drives, for a system maximum of 16. For backup and recovery purposes, the system may also be configured with a single 8089-based tape controller for ¼- and ½-in. start-stop drives.

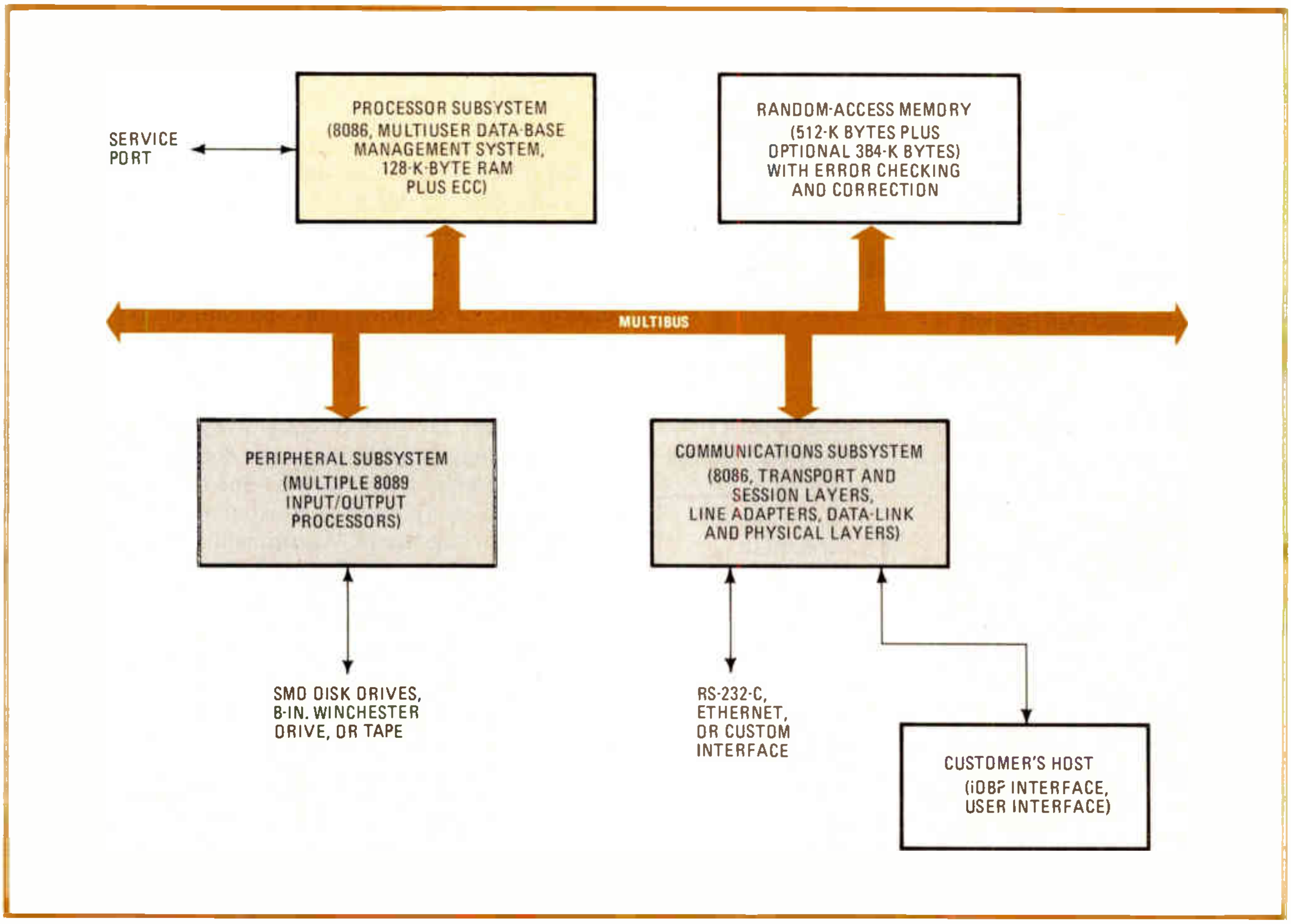
The foundation of the communications subsystem is an 8086-based board that implements the network, transport, and session layers of the host interface proto-

Software-house acquisition buys data-base expertise

The data-base processor for microprocessor systems was an ambitious undertaking, breaking new ground on several fronts. Data-base machines as a class represent new technology, but the iDBP 86/440 was particularly challenging because the paramount design goal was to package mainframe data-base features in a low-cost microprocessor-based vehicle.

Furthermore, it was necessary to extend the notion of data-base management as it applies to conventional data processing, because data processing as such represents only part of the work load for small systems. The iDBP was designed to address the data-manipulation requirements of new applications like those found in office automation.

Although the iDBP development effort did not begin in earnest until late 1979, the product reflects the result of intensive research and development that had been in progress since 1974 at the firm—it was then known as MRI Systems Corp. Over the years, the research emphasis shifted from large back ends (for the system 2000 DBMS) to small systems supporting the relational model of data-base managers. This investment in fundamental groundwork was an important factor in Intel's decision to acquire MRI in 1979 and proceed with the implementation of iDBP. **-R. Colin Johnson**



4. Multiprocessor. Several Intel processors organized around a multibus are used in the iDBP. The 8086 main processor in the system is supplemented by another 8086 for protocol handling with the host and by 8089s for communication with mass storage.

col. This board incorporates a dedicated bus with taps for up to eight line adapters, each of them a small pc board with sufficient logic and firmware to implement the data-link and physical layers of the protocol.

Off-the-shelf line adapters will be available to support the RS-232-C electrical interface with asynchronous, synchronous, SDLC (synchronous data-link control), and HDLC (high-level data-link control) lines. Each line-adapter board can drive two channels at speeds up to 50 kilobits a second. Hence, as many as 16 hosts can be connected to a single iDBP using these common RS-232-C–based protocols.

An Ethernet interface is also provided to support local-network implementations. Special links may also be designed as required to accommodate the idiosyncrasies of various host network and channel architectures.

Future directions

Planned software upgrades are aimed at enhancing the capabilities and performance of the data-base manager. What's more, special attention will be paid to the data-management requirements of the automated office and automated design and engineering workbench applications. Key to success in this effort will be a growing understanding of the kind of data objects that are manipulated in these realms, as distinct from those found in traditional data processing.

The hardware strategy is to move from a single product (like the iDBP 86/440 to a family of application-compatible data-base processors covering a range of prices and performance. The next product in the family will focus on the low end—an entry-level iDBP supporting 5¼-in. hard-disk drives for small hosts or networks. Also, research has begun on techniques for implementing data-base logic at the chip level to reduce the cost of building blocks further.

The needs of the high end are also being addressed. Plans are in place to develop a data-base processor based on the new iAPX-286 microprocessor, with more system memory, and an intelligent disk controller. Ultimately, there will be systems organized around 32-bit microprocessor architectures.

In addition to research and development directly related to the evolution of the iDBP product line itself, there is also the potential to incorporate the technology within other Intel products. For example, work has begun on a data-base work station, which would function as a satellite in a large data-processing installation. The work station would permit its operator to spin off subsets of a central data base for local inquiry and report generation by means of a friendly interface. It would bridge the gap between a mainframe data-base management system such as Intel's system 2000 and its own microcomputer-resident data-base manager. □

Exploiting the full potential of an rf power transistor

by Dan Moline and Dan Bennett
Motorola Semiconductor Products Sector, Phoenix, Ariz.

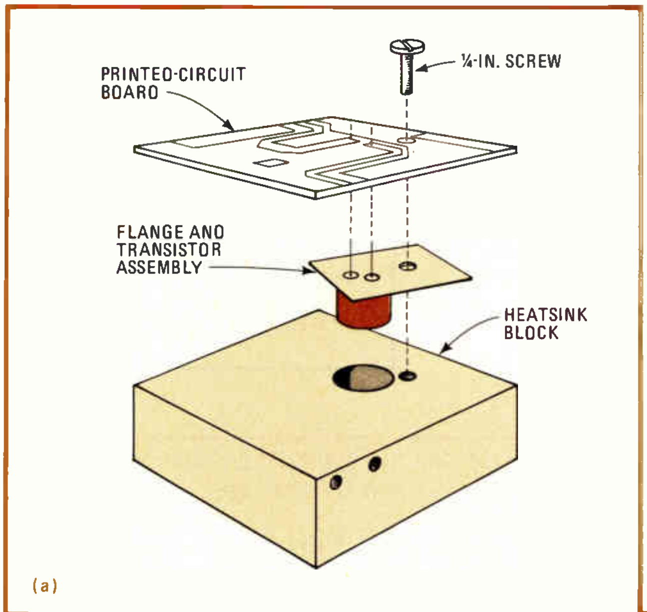
With improved packaging and appropriate circuit design, the new MRF630 radio-frequency power transistor can be used out to its design limits—the generation of 3 watts with 9.5 decibels of gain at ultrahigh frequencies when assembled with an all-gold metal system.

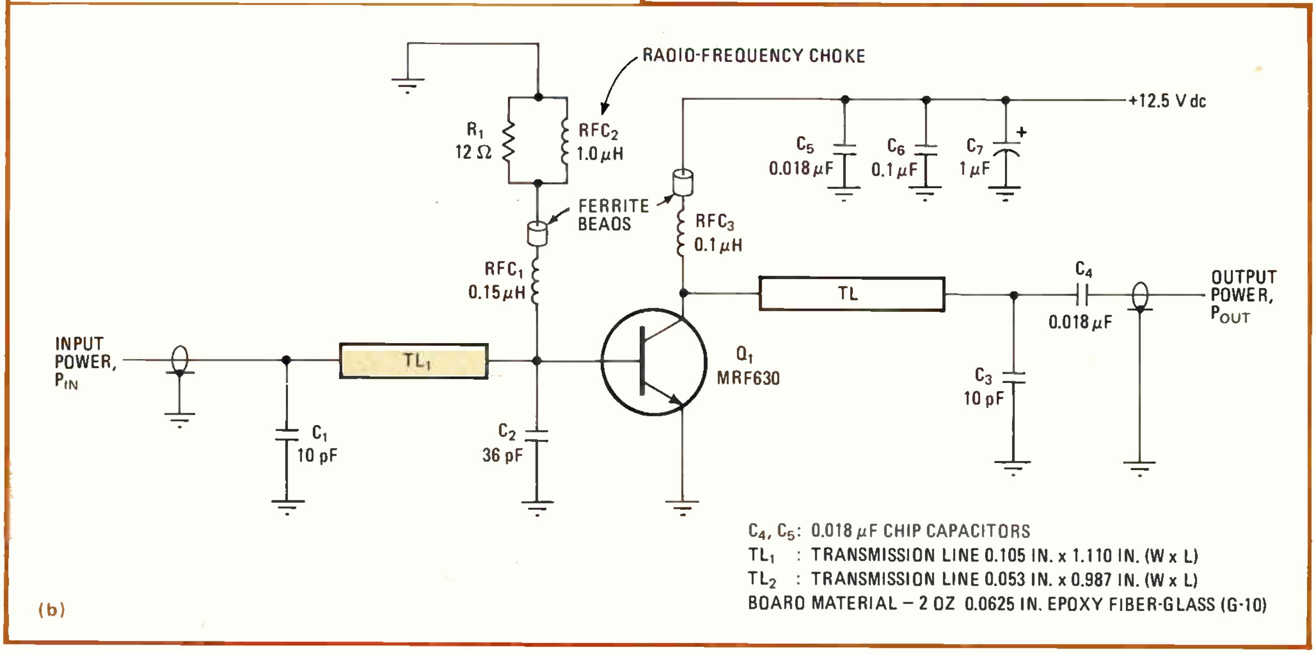
Good heat sinking enables Motorola's low-cost grounded-emitter TO-39 package for rf transistors to perform like a stripline opposed-emitter type. In this package, the MF630, also from Motorola, shows impressive boardband response, excellent heat dissipation, and high reliability.

So that heat can flow directly away from the transistor die, a flange is soldered to the bottom of the TO-39 can and secured to a heat sink by one or two screws (Fig. 1a). This assembly method maximizes heat dissipation while minimizing space requirements. Also, electrical grounding is better as the package is now connected mechanically to the chassis ground.

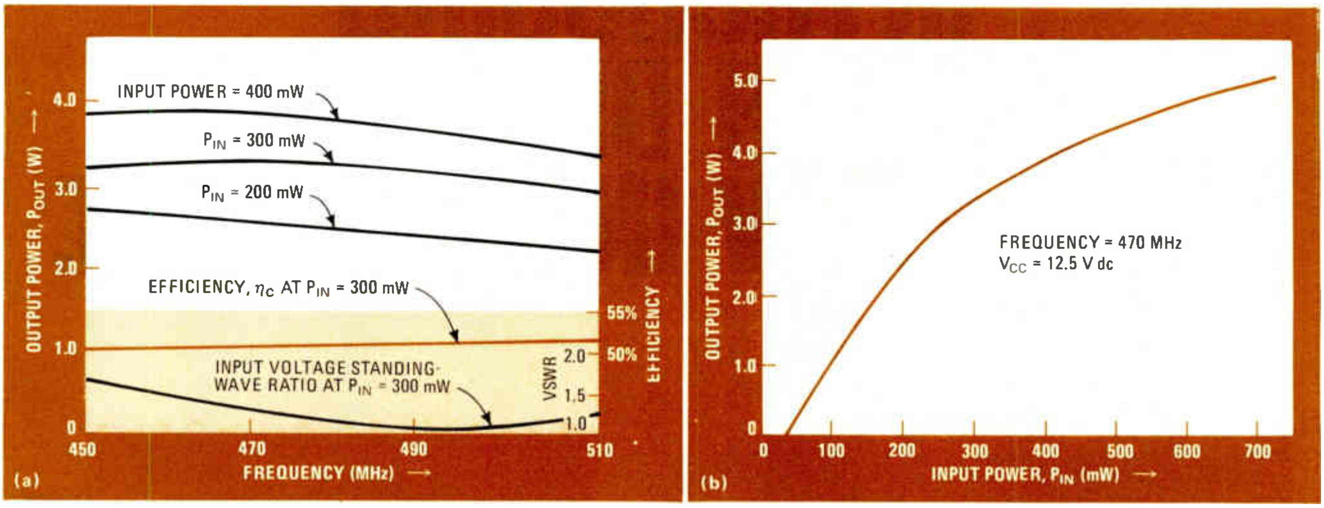
The broadband uhf amplifier circuit in Fig. 1b uses a distributed-element design to optimize the gain and bandwidth of the MRF630. The transmission lines are simulated by epoxy fiberglass G-10 board, whose high dielectric constant and low cost keep the circuit small and inexpensive. (In contrast, the commonly used glass Teflon board offers a low dielectric constant at a relatively high price.) To further cut the cost and exploit readily available components, mica capacitors are chosen for the matching network.

Broadband circuit performance (Fig. 2a) shows that the amplifier can furnish more than 3.0 W at frequencies in the range of 450 to 512 megahertz. The high power output can be extended above 490 MHz by optimizing the input and output–impedance-matching networks. With the addition of the copper flange in the circuit





1. High power. Utilizing the construction technique outlined in (a), common emitter TO-39 package for Motorola's MRF630 provides excellent heat dissipation and reliability at high power levels. The amplifier (b) uses the distributed element design to obtain high power at uhf.



2. Broadband. Its high-frequency performance (a) shows that this amplifier can provide an output of more than 3.0 W above 490 MHz. The gain roll-off above 490 MHz is minimized by optimizing matching networks. The amplifier gain curve at 470 MHz is depicted in (b).

assembly, the thermal resistance of the transistor can be expected to be only 12° to 13°C/W. The gain curve (Fig. 2b) demonstrates typical performance of the transistor at ultrahigh frequencies. □

Active potentiometer tunes common-mode rejection

by Jerald Graeme
Burr-Brown Research Corp., Tucson, Ariz.

A bipolar variable resistance may be simulated by a potentiometer in conjunction with an operational amplifier and four matched resistors. This active potentiometer controls the relative amounts of positive and negative op-amp feedback and eliminates the need for a buffer when employed as a common-mode–rejection trimming circuit. Also, this adjustment circuit makes CMR tuning possible in either direction and is capable of providing output offsetting.

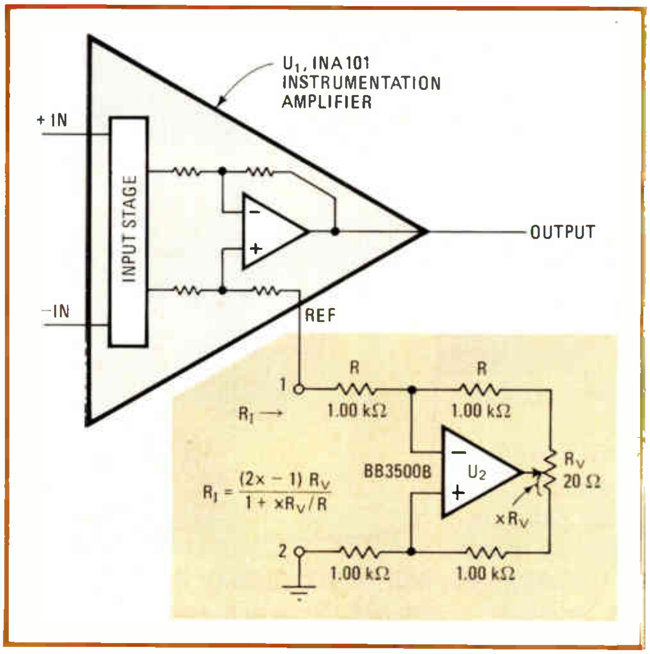
As an example, the circuit may be used with instrumentation amplifier INA101 to fine-tune its CMR. The values attained with this adjustment circuit range from 80 to 110 decibels for a gain of 1 and from 106 to 130 dB for a gain of 100, respectively.

Control over the resistance presented by the adjustment circuit across the terminals 1 and 2 is obtained by potentiometer R_v (see figure) that varies the relative amounts of positive and negative feedback around op amp U_2. The polarity of this resistance and its magnitude is given by $R_I = [(2x-1)R_v]/(1+xR_v/R)$.

The circuit's performance is limited by the op amp used. Any dc errors of the amplifier are reflected at the input terminal of the adjustment circuit as $V_{os}+I_{os}R$, where V_{os} and I_{os} are the input offset voltage and current. Similarly, noise introduced at this terminal is equal to $(e^2_{ni}+2i^2_{ni}R^2)^{1/2}$, where e_{ni} and i_{ni} are the op amp input noise voltage and current, respectively.

As amplifier bandwidth can pose a problem if inadequate, the feedback must be set at levels that optimize this characteristic. If R is small compared with that being trimmed, the feedback factor is ½, giving a circuit bandwidth that is half the unity gain bandwidth of the op amp used. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $75 for each item published.



Bipolar potentiometer. Multiple-feedback op-amp circuit provides a variable resistance that is bipolar. This active bipolar potentiometer allows common-mode–rejection trimming in either direction for instrumentation amplifier INA101. With this adjustment circuit, common-mode rejection can be trimmed over a wide range.

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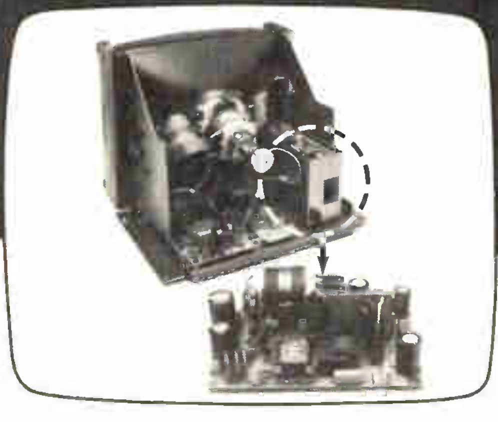

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Circle 120 on reader service card

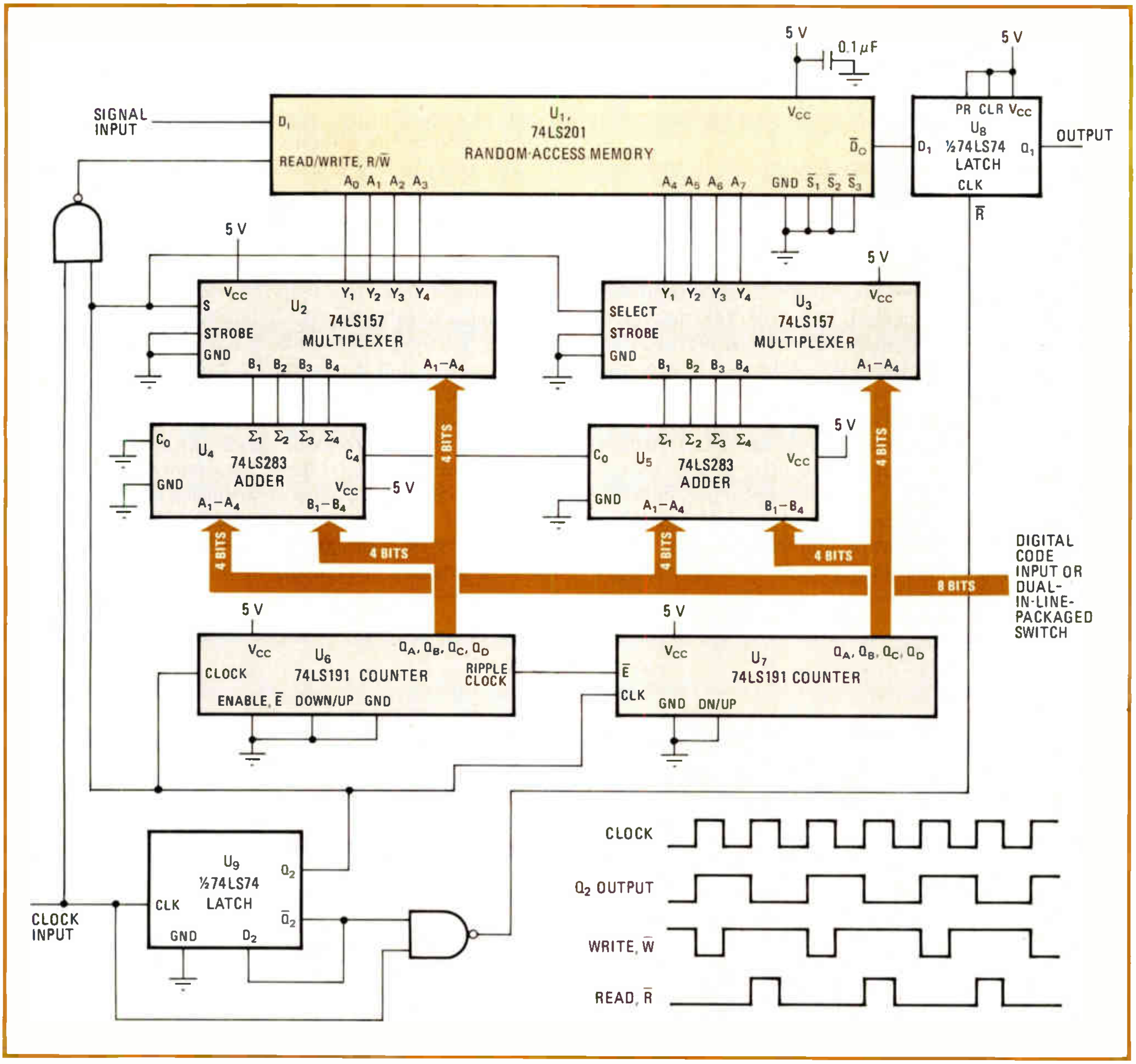
RAM makes programmable digital delay circuit

by Darius Vakili
Bayly Engineering, Ajax, Ont., Canada

For applications lacking in long shift registers and for which bipolar components are too expensive, this simple random-access-memory circuit will program the delay of digital signals precisely and accurately—and without needing varying clock frequencies. The RAM's ready availability and low cost add to the circuit's attractions, especially when high signal speeds are involved.

A digital input code programs the output delay of the signal. The input signal is written into the RAM U_1 at an address generated by synchronous up-down counters U_6 and U_7 and by a fixed input digital code set by the dual-in-line-packaged switch. The stored signal is available at the output when the write-enable input to the RAM is high. This data is read out of the RAM from a location that corresponds to the address generated by the counters only. Therefore, the signal read from the RAM is delayed by a time period equal to the DIP switch's displacement value multiplied by the period of the clock used for generating the address.

The input clock is divided by 2 by latch U_9. The Q_2 output of U_9 clocks address counters U_6 and U_7 and also the select inputs of multiplexers U_2 and U_3. The NAND gates generate the RAM's read and write inputs and also ensure the data is written into the RAM when the control input of U_2 and U_3 is high and read out when it is low. □



Programmed delay. Using random-access memory, this programmable-delay circuit accurately controls signal delay by means of a digital code generated by a DIP switch. Counters U_6 and U_7 generate the address for the RAM. U_9 provides the write and read inputs for the RAM.

Coprocessing expedites software-hardware development

With a communications processor helping the main machine, this microprocessor development system can serve many users efficiently

by Mike Zuhl, *Tektronix Inc., Beaverton, Ore.*

☐ Though it is becoming commonplace to deploy a microprocessor development system in a network, such a setup risks bogging down as the number of design engineers and programmers linking up with it increases. That risk can be minimized for the system's two major development functions—microcomputer software generation and the integration of hardware with software—by the use of coprocessing.

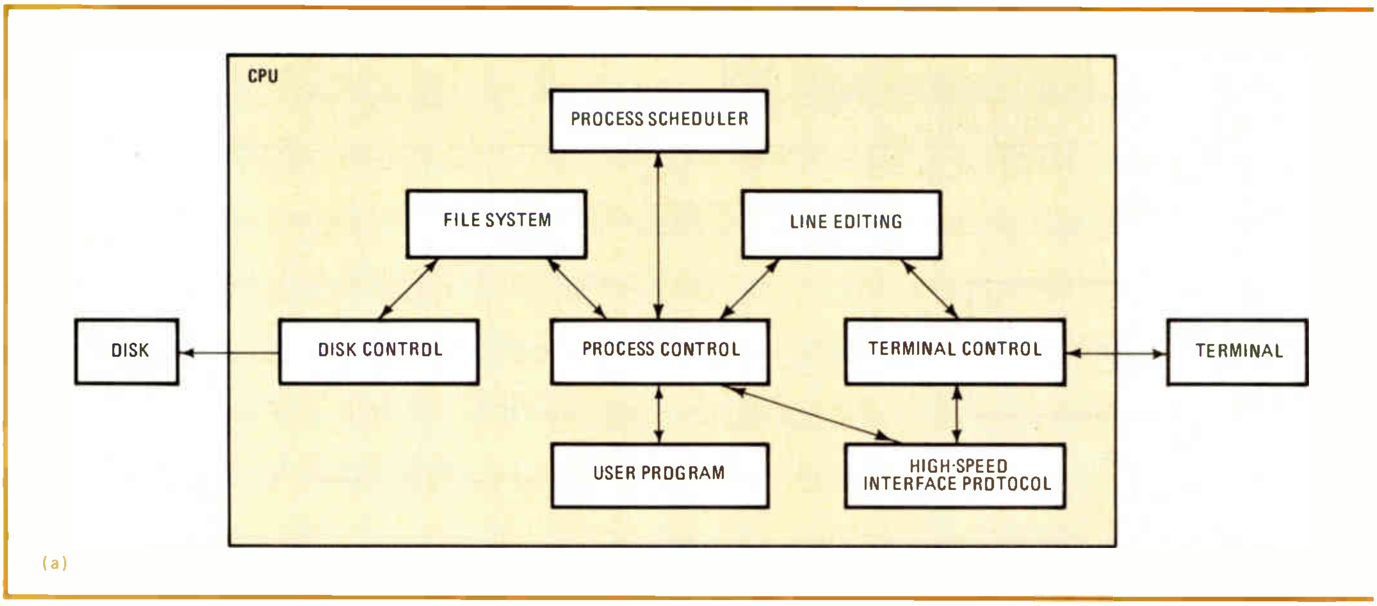
When two or more microsystems tackle a processing task, the overall system's throughput is greatly enhanced. Coprocessing can remove much of the burden normally shouldered by the main processor (hereafter referred to as the central processing unit) and can prevent potential bottlenecks as well. But for coprocessing to be optimally exploited, as in the Tektronix 8560 multiuser development system [*Electronics*, Nov. 3, 1981, p. 220], the nature of the tasks to be performed must first be thoroughly examined.

The development of software, which on the 8560 can be done at standard cathode-ray-tube terminals, includes such jobs as entering source-code files, as well as converting results into object code through operations like compiling and linking. The other major system function, the integration of hardware and software, is accomplished by the 8560 with another unit—the 8540 integration station, an intelligent subsystem that uses a high-speed communication link with the 8560 to transfer object-code files and debugging commands.

In order to support both functions, four main tasks were identified and evaluated: communication with terminals and 8540s, management of the file system maintained in mass storage, application-program processing (such as editing and compiling), and the management of multiple tasks by TNIX, a modification of Bell Laboratories' Unix Version 7 operating system. The two most likely candidates for coprocessing turned out to be file management and work-station communications, as both these tasks consume much processing time yet have well-defined interactions with the rest of the system.

The most sensible approach to reducing the delays due to these potential bottlenecks is horizontally distributed coprocessing—that is, assigning processors to specific functions. Using the opposite approach, a vertical distribution of effort among separate but equal processors, can result in interprocessor communications that contribute more to overhead than they remove.

In the 8560, horizontal distribution optimizes performance of the two tasks since specialized coprocessing systems have been designed with all their hardware and software targeted specifically at the assigned task. The



result is more than double the processing efficiency of a single, unaided CPU, and the major contributor to this increased efficiency is the communication coprocessing system (Fig. 1).

The coprocessing system dedicated to communications with terminals and 8540s is called the input/output processor. It uses an Intel 8088 microprocessor, which employs a 16-bit internal architecture combined with an 8-bit bus and I/O interfaces. This processor is especially suited to the task, which requires high processing speeds but does not call for a wide data bus.

A dedicated assistant

In its role of traffic manager, the I/OP takes a significant load off the CPU. When communicating with terminal work stations, it accumulates entire lines and then transfers them into the program's memory using direct memory access, rather than the normal interrupt-driven input of one character at a time. The I/OP also performs all the intraline editing (for example, erasing the line and backspacing) and retains a copy of the last line input, which may be reedited and sent again as input.

For output to terminals, it allows a programmable end-of-line sequence and optional tab expansion. The I/OP treats all writing operations of less than a certain size as separate complete entities, or "atoms," to prevent them from being mixed in with echoed characters or other writes. This is important when sending control sequences to intelligent terminals.

A packet protocol, referred to as the high-speed interface, permits 153.6-kilobit-per-second transfers through the RS-422 lines that connect 8560s and 8540s. In addition, the HSI protocol supports two logical channels of communication per port: one for controlling the 8540 and the other for the terminal attached to the 8540. With this protocol, the I/OP handles all associated operations, including sequencing, error checking, retry on error, and flow control.

Each task handled by the I/OP relieves the CPU of considerable processing obligations and gives a further boost to system throughput. By handling terminal I/O, the I/OP removes the need for the one-character-at-a-time processing normally done by the CPU. In addition, since this type of single-character processing is interrupt-driven, it would also call for additional handler software and its associated memory space as well as the extra CPU time involved in performing the interrupt service.

Intelligent choice

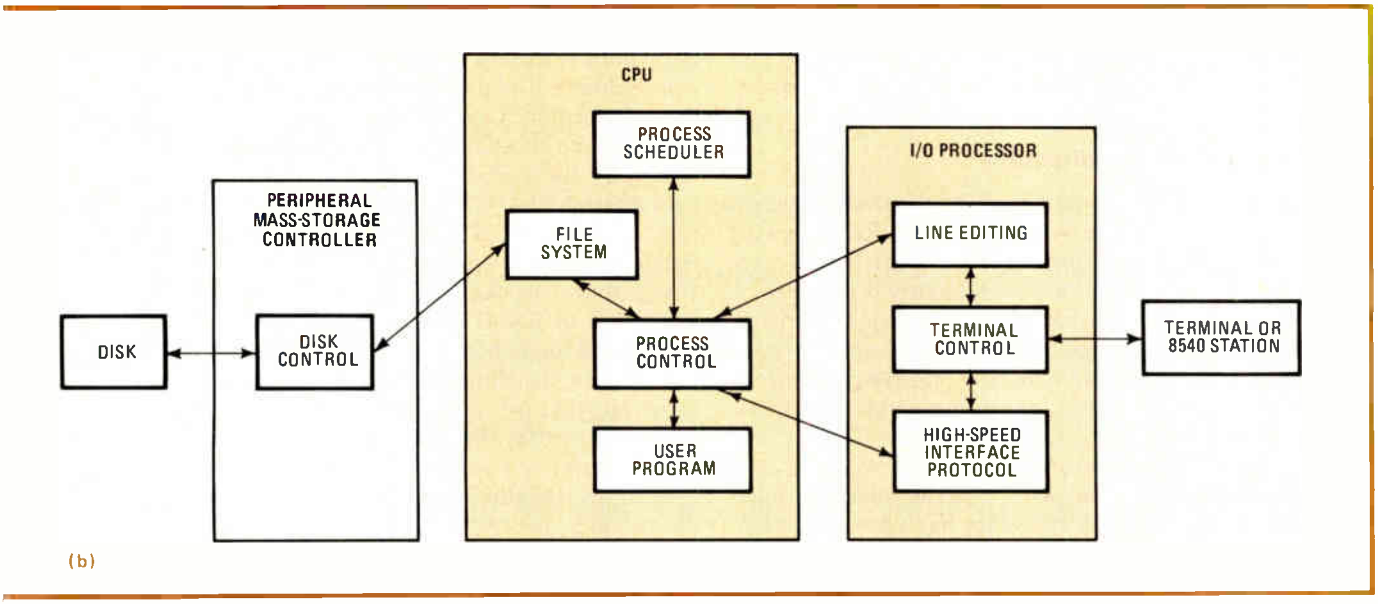
Using controllers for either dumb or low-intelligence terminals could have lessened the CPU's interrupt obligations by permitting the formation of character queues that could be read periodically, but the CPU would still have had to assume all other terminal I/O functions. The I/OP assumes the responsibility for all these additional functions, including, as noted, intraline editing and the ability to edit and reissue the last line entered.

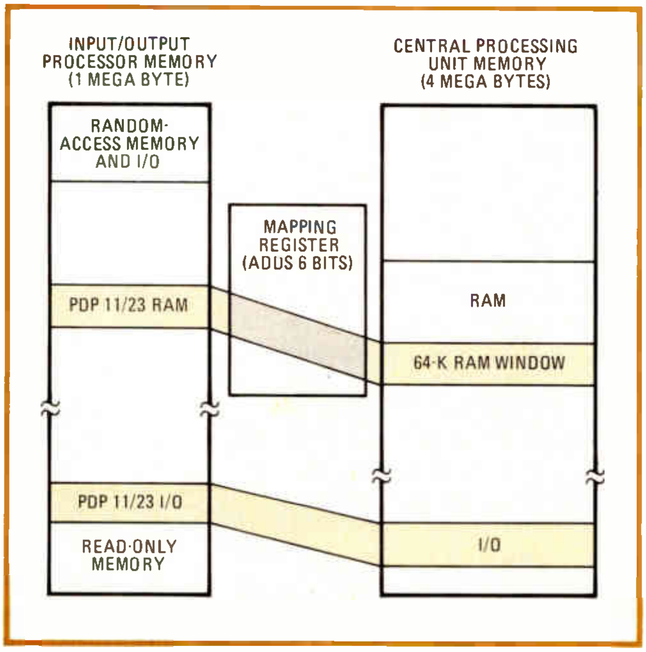
Another major task offloaded onto the I/OP is control of the data flow, a necessity when managing high-speed data transfers with intelligent peripherals, such as the 8540 integration unit. Flow control is a mechanism by which the receiver of data can ask the sender to stop sending data temporarily. Without this mechanism, the potential for data overflow exists during peak loading situations, as when several intelligent peripherals are simultaneously uploading.

The I/OP can accommodate both principal methods of flow control—data-oriented or dedicated line. In data-oriented flow control, the receiver sends a character to the sender, telling it to stop (DC3, also called control-S) or start up again (DC1, or control-Q).

When using dedicated lines for flow control, the receiver asserts data-terminal-ready for as long as it can accept data. The I/OP allows one method to be used in one direction and the other in the opposite. By managing flow control, the I/OP relieves the CPU of the constant,

1. Sharing the load. Without coprocessing (a), a microprocessor development system's CPU needs to handle such tasks as line editing or high-speed interface-protocol formation and terminal control. With it (b), such tasks are offloaded onto an input/output processor specifically designed to handle such tasks.





2. Recalling. To simplify transfer of data between the input/output processor and the central processing unit, a CPU-controlled register adds 6-bits to the I/OP's 16-bit random-access-memory address. Thus, a 64-K-byte window can be moved anywhere in the CPU's memory and transfers accomplished with block-move instructions.

periodic processing required to monitor either the line status or the control data.

The I/OP also assists in managing the suspension and reactivation processes during program execution, an important speed improvement when a program includes extensive interaction with system work stations. For example, when a program indicates a need for input from a work station, the operating system and I/OP acknowledge the need, and the system either leaves the program temporarily in memory or swaps it out onto disk if the CPU's random-access-memory space is needed for other tasks. When the I/OP receives a program input from the appropriate work station, it informs the operating system that the program is now needed in memory. Once the program is again resident in memory, the CPU informs the I/OP that it is ready to accept the input, and the I/OP transfers the data to the program's memory using DMA.

Memory-intensive architecture

Since a coprocessor is not bound by the overall system constraints placed on the system CPU, its design can be tailored for optimum performance of its particular subset of system tasks. The I/OP's architecture is designed to be memory-intensive rather than processing-intensive. Thus, it not only assumes many CPU tasks, but it also executes them at a throughput level not possible with a general-purpose CPU that is executing standard operating-system routines.

For example, Unix character processing with the conventional CPU method involves a series of conditional branches to determine if a character has a special action, such as end-of-line, associated with it. This action uses little memory but requires extensive processing. By contrast, the I/OP's local memory holds a table of appropriate actions for each character. Thus, when a character is received, the I/OP simply refers to the table and begins processing the response immediately—a procedure requiring more memory but substantially decreasing I/O processing time.

With the I/OP's memory-intensive architecture, much less processing time is spent in managing data queues during I/O operations, as well. The conventional Unix-system approach with a single CPU is to pull character-buffer queue elements out of a shared buffer pool as they are needed to service I/O activity. Again, this method conserves memory at the expense of processing time. By contrast, the I/OP system includes individual queue space assigned to every port, so the processor spends no time on this phase of queue management.

Additionally, the queue space for each port is divided into three subqueues: one for the line *en route* to the CPU, another for the last line entered, and a third for the line currently being handled. When an end-of-line is reached, the data in the current line must be added to the data queued to the CPU and must replace the data in the last line queue.

Instead of managing the status of these queues by time-consuming data transfers, the I/OP simply manipulates three sets of queue pointers. In most cases, the queue of data for the CPU and the last-line queue actually overlap in memory (so the data does not have to be transferred), with the queue pointers keeping them logically separate.

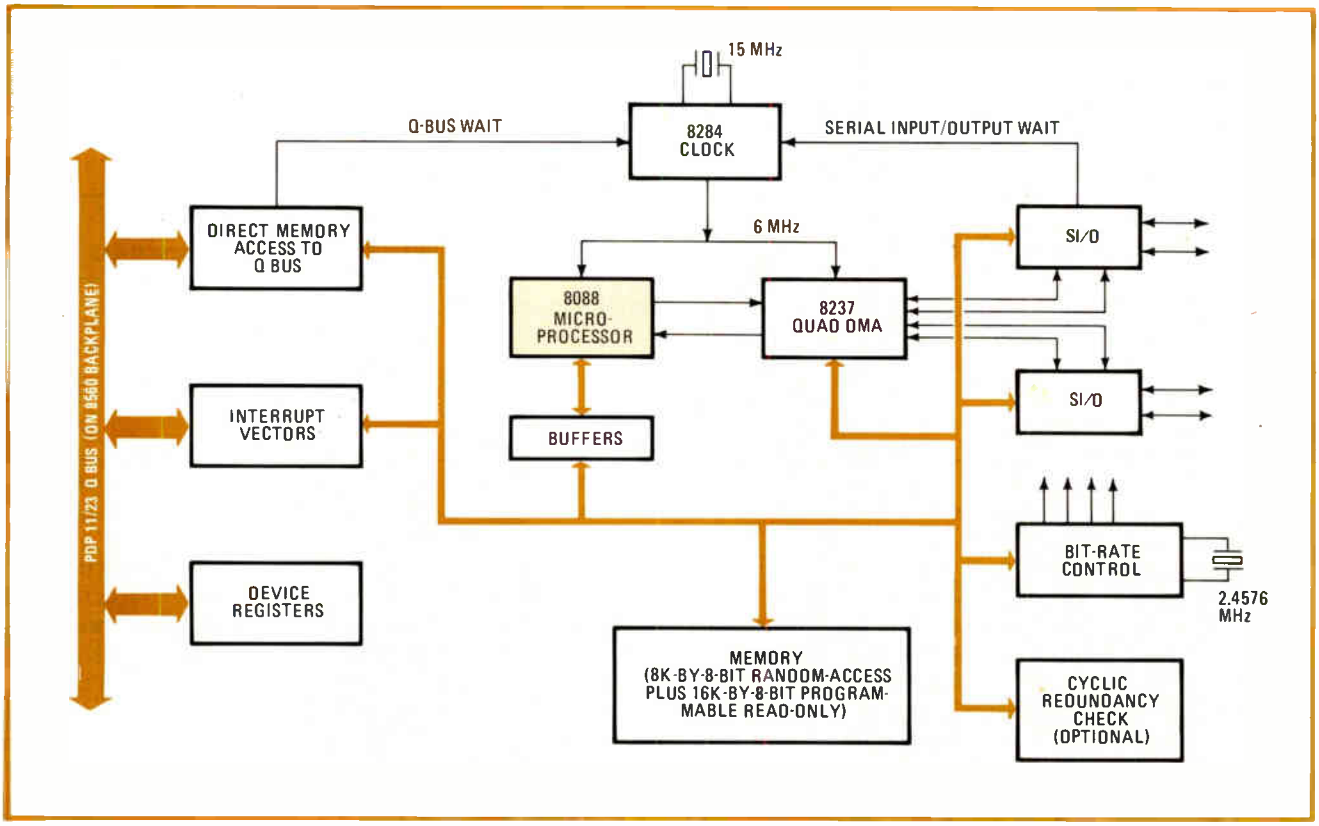
Building a correspondence

Memory mapping is an important aspect of the relationship between the CPU and I/OP (Fig. 2). The CPU supports a 4-megabyte address space (22-bit address), while the I/OP has a 1-megabyte space (20-bit address). A 6-bit register helps map the CPU RAM space into the I/OP address space.

On the I/OP side, the CPU RAM space is handled in 64-K-byte blocks by 16 address bits, with the 6-bit register supplying the high-order address bits. This way, the I/OP retains a 64-K-byte window that can be moved anywhere within the CPU RAM space. Consequently, the DMA data transfers between the I/OP and CPU memory can be done with 8088 block-move instructions.

Both the I/OP's hardware and software are configured to maximize throughput. The I/OP hardware uses DMA internally for certain time-critical tasks (Fig. 3). The work-station side is connected to an I/O adapter board that converts serial I/O for teletypewriter format into either RS-232-C or RS-422 signal levels. Each of the I/OP's four I/O channels can be configured for either RS-232-C or RS-422 through jumper switches mounted on the adapter board. When a channel's jumper is switched to the desired electrical interface, it asserts a logic bit that identifies the default protocol (HSI or terminal) used by the I/OP.

Two serial I/O (SI/O) chips with programmable bit-rate control handle all communications routed through the adapter board. Each handles two channels, for a total of four. (When fully configured, the 8560 contains two complete I/OPs that handle I/O with up to eight work



3. Communicator. The heart of the input/output processor is the 8088, which handles terminal and 8540 work-station communications for the 8560 development system. Four work stations can be managed by one board, and the 8650 will support two I/OP boards.

stations.) Incoming serial data is constantly queued into the I/OP through DMA. This technique expands the normal 4-byte queue internal to the SI/Os to 256 bytes, permitting the queue to fill and empty in long cycles that minimize the amount of processor queue management required during heavy loading.

The CPU side of the I/OP uses a combination of DMA, interrupts, and device registers for communication with the CPU. DMA is used for the transfer of all the data and most of the control information between the CPU and the I/OP. The I/OP can also assert CPU interrupts to signal the completion of commands, keyboard interrupts, or modem hangups. The two device registers belong to the I/OP and are written into by the CPU. Typically, these are used only for establishing command and response queues and for critical system messages.

Command and response

On the software side, the CPU and I/OP interact through a special communications protocol designed to minimize the real-time constraints on both processors. This protocol is built on a command-response structure, with the CPU issuing commands to the I/OP that determine the specific nature of the current I/O operation and the I/OP sending an appropriate response upon completion. The flow of commands and responses is buffered to prevent congestion and to give both processors maximum flexibility in allotting time to I/O tasks. Thus, the I/OP appears to the CPU as two logical devices, one dealing with terminal communications and the other with HSI communications to an 8540 or other computer systems.

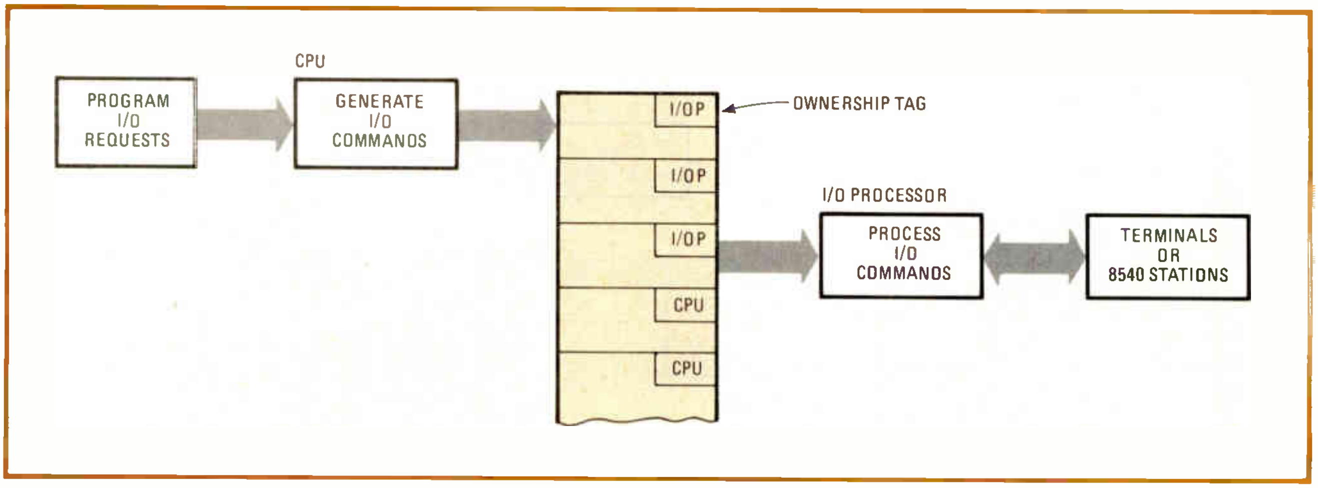
Each logical device has its own command-response set and an associated set of buffers. In the terminal mode, CPU commands allow both reading and writing, plus the ability to characterize the I/OP to specific terminals. This characterization includes echoing, bit rate, and the definition of special control keys.

Other commands permit the output to be flushed and the modem connection to be opened and closed. In the HSI mode, CPU commands allow both reading and writing, plus the ability to set certain protocol parameters, such as time-out values and the number of times to retry after detecting an error. These protocol parameters and error statistics can be read back by the CPU and can help detect failing lines before they become troublesome.

The I/OP's response to the CPU's I/O commands includes the number of bytes transferred and the error status, plus a special software feature called a transaction key. This key is included in the original CPU command and is not changed during the course of I/OP processing. The key is then returned to the CPU, which uses it to keep track of a process requiring an I/O operation for completion.

Key role

The role of the transaction key in I/O management by the CPU can be illustrated by taking a closer look at a data-input operation to a program being executed. First, the program notifies the process-control portion of the operating system that it requires data input through a terminal-read operation. Process control will now form a terminal-read I/O command destined for the I/OP, and



4. Mine. To prevent the input/output processor from accessing a command field before the central processing unit has finished with it, the data fields in the queue are given ownership tags that remain unchanged until the processor is finished. Responses are tagged similarly.

this command will include as its transaction key the process identification of the requesting program.

At the same time as the command goes to the I/OP, the scheduling portion of the operating system puts the program in a suspended state—waiting for terminal input. When the input occurs, the I/OP uses DMA to transfer the terminal data to the suspended program's memory and sends the response data back to the CPU, along with the transaction key. Process control can now inform the scheduler that it should reactivate the program whose process is identified in the transaction key. The program continues execution using the terminal data that is now in its buffer.

One goal of the I/OP-CPU coprocessing scheme was to transfer control information between processors so that they could run asynchronously, maximizing the available processing power. To this end, commands and responses are communicated through first-in, first-out (FIFO) queues of control blocks containing all the associated control information, including the transaction key.

The CPU puts command blocks into a queue from which the I/OP later takes them. When a command is completed, the I/OP places a response block (optionally interrupting the CPU, depending on the priority of the task) into the queue, and the CPU removes this block.

A serious problem can arise, however, when each control-block queue is controlled by a single queue pointer accessible by both processors. One processor could grab a pointer value already being used by the other processor, which may not yet have had time to increment the pointer. If this situation developed, a command or response could be lost and the program waiting for I/O would be suspended forever.

Ownership tags

Keeping shared data consistent is a general problem in multitasking and multiprocessing systems. One task or processor must be allowed to complete its manipulation of shared data before another is allowed to start. With single processors, this completion can be managed simply by disabling interrupts before the manipulation starts and enabling them again upon completion.

The solution chosen for the multiprocessing CPU-I/OP system is for the CPU and I/OP to keep their own set of pointers. A 1-byte ownership tag field is added to each control block, which can be changed in a noninterruptible operation, memory write. Each control block is thus "owned" by either the CPU or the I/OP, and only that processor can legally insert or remove the data contained in the element.

To illustrate how these queues function, consider the handling of the flow of commands from the CPU to the I/OP (Fig. 4). First, the CPU uses its current pointer value to address the queue element and read its tag field. If the tag identifies the CPU as the owner, it will insert command data into the queue element, change the tag field to transfer ownership to the I/OP, and then advance the CPU queue pointer.

If the tag identifies the I/OP as the present owner, this indicates that the CPU has filled all of the command blocks and has wrapped around to the start: the queue is full. When the queue fills up, the CPU will cease queue operations until the I/OP completes a command indicating that the queue is partially empty again. In practice, the queue is seldom filled because enough queue elements are allocated to handle peak request loads.

A similar set of operations occurs on the I/OP side of the command queue. First, the I/OP checks the ownership tag of the queue element currently indicated by its pointer. If the I/OP is the owner, it will remove the command data, transfer ownership of the element to the CPU and then advance the I/OP queue pointer. The I/OP can now store these commands in its own local queue for processing. If the CPU owns the element, the queue is empty, meaning that the I/OP has completed all of the commands. The I/OP will continue to check this ownership tag from time to time to see if a new command has been placed in the queue.

The use of command and response queues is similar to command chaining but adds the important advantage that new commands can be inserted into the queue whenever necessary. For each set of queues, the CPU now requires only two simple drivers. One fills the command queue based on I/O requests from users, and the other empties the response queue to start processes specified by command blocks. □

5-volt-only EE-PROM mimics static-RAM timing

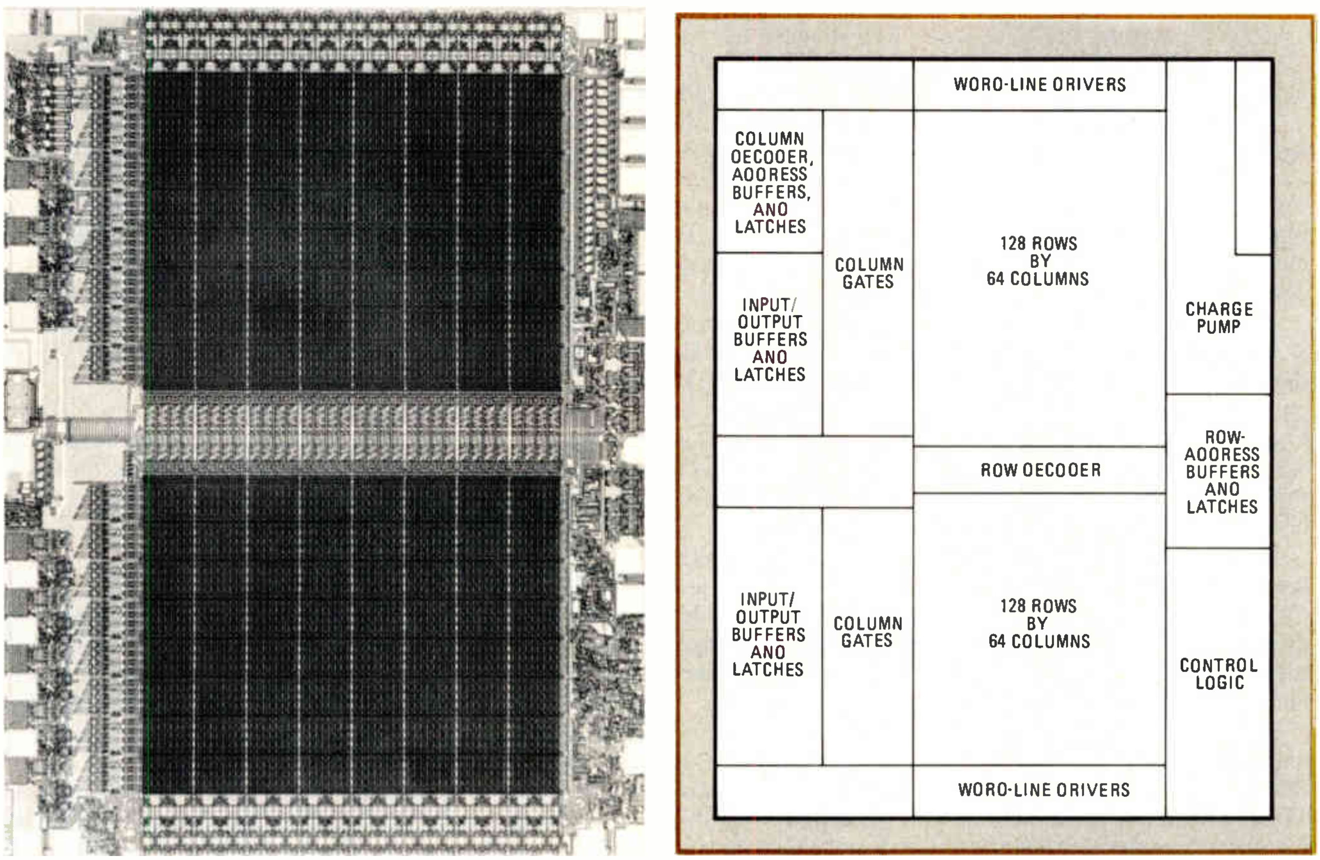
On-chip charge pump, interface latches simplify designs; textured polysilicon enhances tunneling through thick oxides

by George Landers, *Xicor Inc., Milpitas, Calif.*

☐ The approaching mastery in fabricating electrically erasable programmable read-only memory conjures up dramatically different system designs. On the most mundane—but perhaps most immediately valuable—level, alterable nonvolatile semiconductor memory will soon banish routine service calls by allowing remote changing of system software. Not far away, if still somewhat tinged with the aura of science fiction, is the vision of self-programmable systems that adapt themselves to a changing operating environment. The catalyst for these advances is an EE-PROM that is simple to incorporate in microprocessor-based systems.

Now being launched by Xicor is a family of EE-PROMs that is the first to do away completely with external supporting hardware (Fig. 1). The chips contain the charge pump that generates a high programming voltage from a 5-volt supply. Further, latches on chip hold the data, address, and control signals during alteration of the cells, which typically takes 5 milliseconds per byte and is timed internally. The part marks the debut of an EE-PROM that can simply be dropped into a standard 24-pin static random-access-memory socket.

The 5-micrometer n-channel MOS technology applied to produce the X2816A 2-K-by-8-bit EE-PROM and the X2804A, a 512-by-8-bit version, is the same as that being used to build the devices in the Novram line of static RAMs with nonvolatile backup arrays [*Electronics*, Oct. 11, 1979, p. 111]. Recently, however, theoretical



1. All aboard. This 16-K electrically erasable programmable read-only memory integrates all its support circuits. A charge pump generates the programming voltage from a 5-V supply; latches hold addresses and data during the internally timed write cycle.

Shedding light on electron tunneling

The present generation of electrically erasable programmable read-only memories using floating-gate structures draws on a reservoir of process development, circuit design, and basic physics. The floating-gate process has been in production for many years and forms the building block of EE-PROMs. The next step toward a practical 5-volt programmable EE-PROM centers on removing the high currents typically used to alter data by avalanche or hot-electron injection. A high voltage can be generated on chip as long as only minute currents are required, as with the new circuit designs.

As far as the underlying physics, the tunneling processes found in most floating-gate EE-PROM devices are described by a theory introduced in the 1920s by Fowler and Nordheim. As shown in the theory, if the emitting surface is flat, very thin oxides of around 100 angstroms are necessary for significant tunneling currents at reasonable voltages of 15 to 20 volts. To the continued puzzlement of researchers, experimental data has fit the theory roughly, but not especially closely.

Xicor purposely fabricates textured emitting surfaces that are covered with low-lying bumps or hills formed during the oxidation of the polysilicon surface. Recently, tunneling theory has been extended to describe this textured-surface geometry with the result that conventional devices are now better understood as well.

The low-lying hills, which serve as the electron emitters, are less than 150 Å high and more than 500 Å across their base. The figure on the right shows the triple-polysilicon tunneling structure in cross section, a scanning-electron-microscope photograph of a typical textured tunneling surface, and the geometry of a typical bump on the polysilicon surface.

Because the oxidation is a well-controlled step, the properties of the emitters are exceptionally regular. The shape of the emitters tends to increase the electric field at the crest of the hills, enhancing the emission of electrons substantially, which allows the use of thick oxide layers of approximately 800 Å. As indicated in the figure, increasing the voltage not only increases the emission, but enlarges the area from which it occurs. This effect explains the discrepancies between experiments and the earlier tunneling theory. The thick oxides have important practical advantages: they are easier to manufacture and lead to increased retention of data.

Until recently, the theoretical work on Fowler-Nordheim tunneling had solved only the limited case of perfectly flat plates. Roger Ellis and H. A. R. Wegener of Xicor recently presented measurements and calculations that agree over a range of eight orders of magnitude in the current. With the aid of the methods of differential geometry, the tunneling characteristics of a textured surface were calculated for the first time. As the scale of the texturing is reduced, the solution naturally reduces to the familiar flat-plate case. The figure on the far right compares the tunneling currents for flat and textured surfaces.

The two structures were designed for the same operating point—a current density of 10^{-4} amperes per square centimeter at 17 V. At low fields, such as are applied to read data, the thick oxide used with the textured surface has only about a thousandth the current of a flat surface. As a result, data retention would be expected to be far longer.

The current from a flat emitter in fact can be modeled much more closely by considering some texturing of its surface. Even single-crystal polished silicon wafers have surface features on the order of 5 Å, and normally processed polysilicon has even larger variations. Thus, Xicor's tunneling structures accentuate features that are always present in floating-gate devices.

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work has significantly added to the understanding of the tunneling of electrons from textured polysilicon, the mechanism exploited in all these products (see "Shedding light on electron tunneling," above).

This work explains how a textured surface emits more electrons than a smooth one for a given voltage and oxide thickness. (Scanning-electron-microscope studies of the polysilicon surface show that the texturing consists of low-lying bumps about 150 angstroms high and 500 Å across.) This enhanced emission allows the use of typically 800-Å-thick oxides, instead of very thin, 100-Å layers that are much harder to produce reliably.

Besides being easier to manufacture, thicker oxides lead to increased retention of data. What's more, a 16-K EE-PROM with 5-μm linewidths and 800-Å-thick oxides promises to be more readily scaled down for denser memory arrays than one with, for example, 3-μm lines and 100-Å-thick oxides.

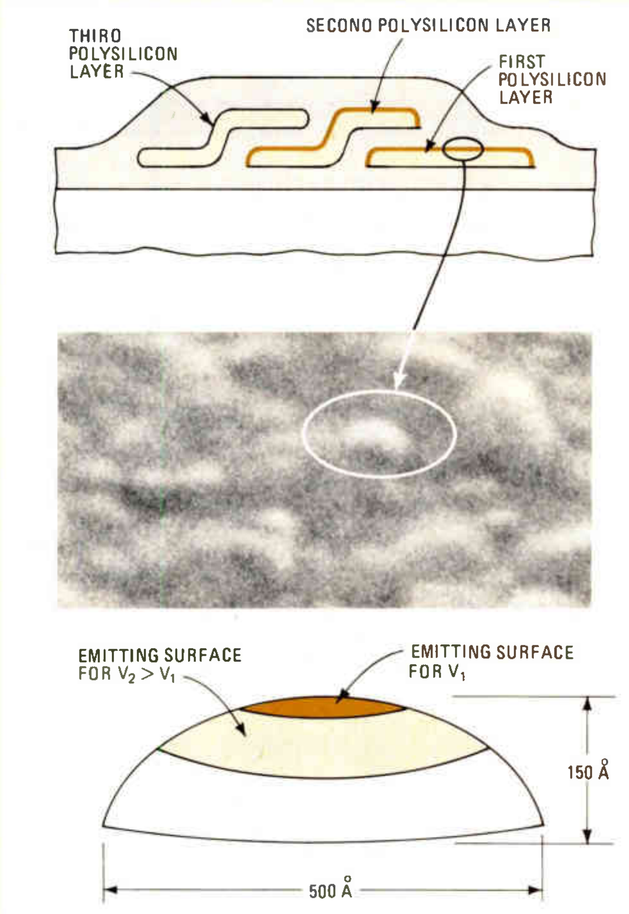
Floating-gate technology along with the architectural features making the parts simple to use present the state of the art in EE-PROMs after a decade of development. Metal-nitride-oxide-semiconductor structures yielded the first nonvolatile memories that were electronically alterable. These devices store data by trapping electrons within the nitride and oxide dielectrics. Besides the problems these devices encounter—data disturbance during the read operation and the loss of data over time—they require multiple power supplies, one of which is often negative, and signal swings beyond TTL levels. All this complicates their incorporation within microprocessor-based systems that work with a single 5-V power supply and TTL levels.

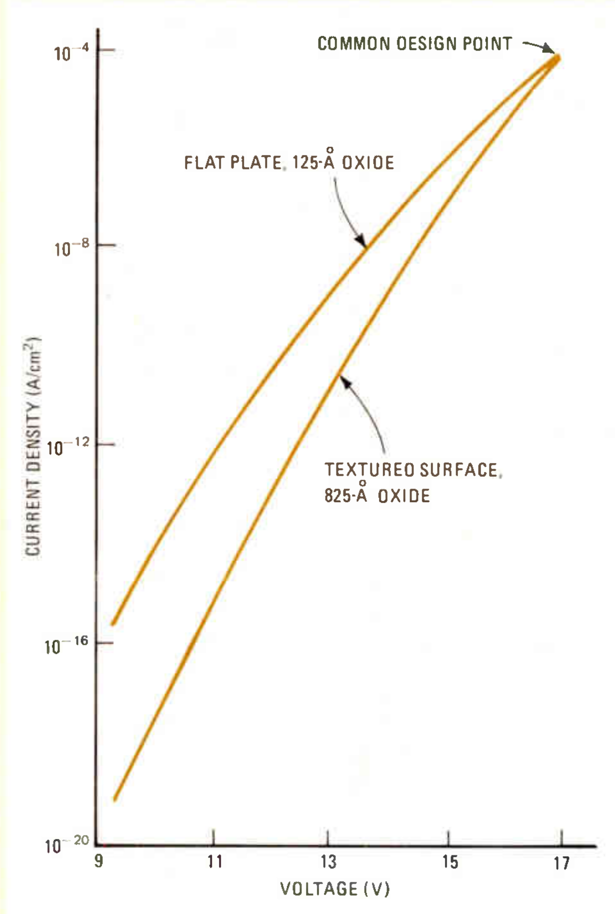
Further complicating their use is the fact that the addresses and data must be stable for the entire write cycle, lasting up to 40 ms. It takes extra hardware to capture these signals and to time the write interval in order to free the processor for other tasks.

Comparing EE-PROMs

The second generation in EE-PROMs was ushered in by the 2816 from Intel Corp. of Santa Clara, Calif. This part stores data by trapping charge on floating polysilicon gates, as is done in ultraviolet-light-erasable PROMs, or E-PROMs, and improves the data integrity compared with MNOS parts. Although the 2816 has a standard pin configuration and uses TTL signal levels, it still requires an externally generated high-voltage pulse for altering data, not to mention latches for holding the address and data signals.

Measured against the 2816, recently introduced third-





generation parts incorporate some or all of the required supporting hardware on chip (see table). The 2817 from Intel moves the external high-voltage pulse generator onto the chip, so that a fixed 21-V supply is all the user must provide. Though it does include the necessary interface latches, it still requires an external capacitor to

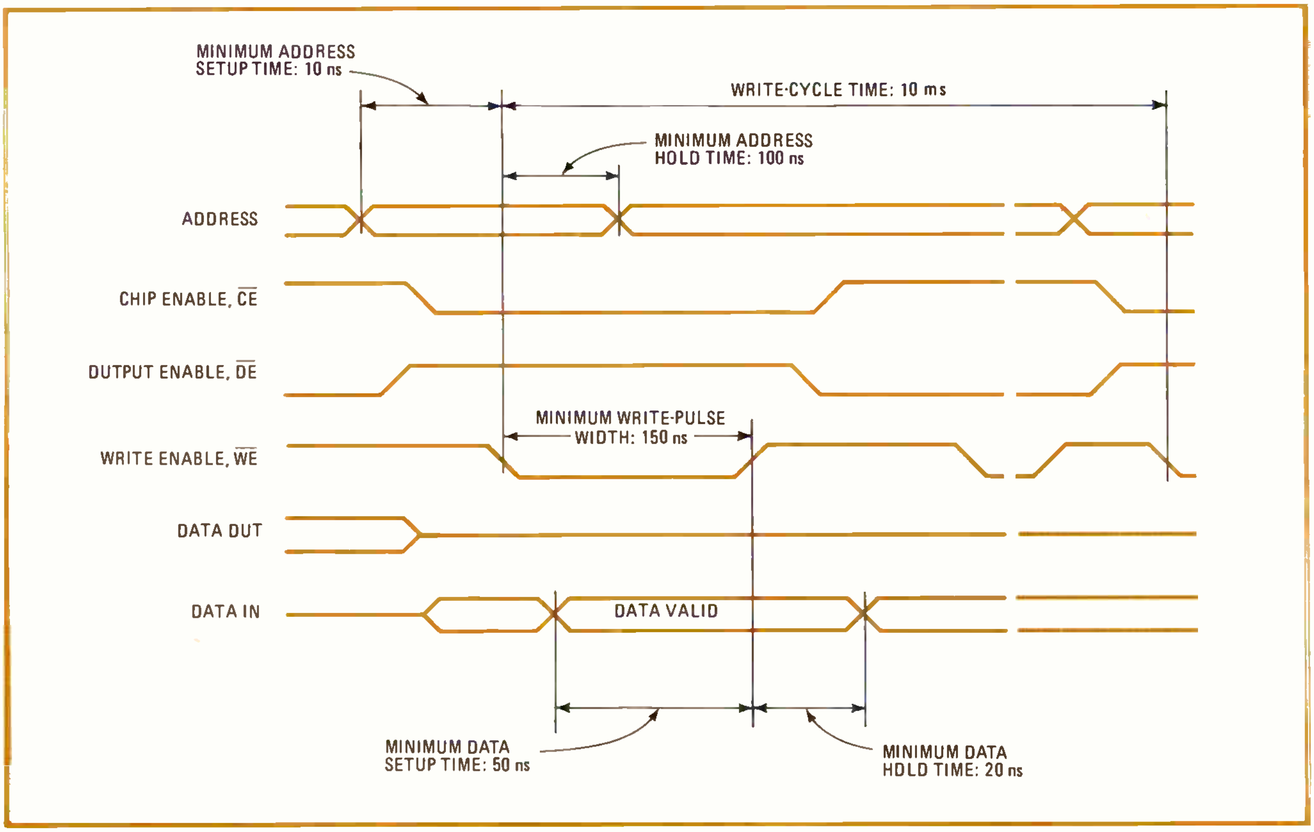
COMPARISON OF RECENT ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

Part	Intel 2816	Intel 2817	Seeq 5213	Xicor X2816A
On-chip charge pump				
Address and data latches				
Automatic erase				
Internal timing of write cycle				
Internal control of write-pulse shape		needs external capacitor		
Maximum erase-write cycle time (ms)	20	75	20	10

time the write cycle. More recently, the 5213 from Seeq Technology Inc., San Jose, Calif., operates from a single 5-V power supply, but still needs latches and external timing. Only the X2816A completely eliminates the external components.

All the X2816A's input and output signals are TTL-compatible and the addresses and data are latched so that they need be stable for only 200 nanoseconds to initiate the 10-ms write cycle. Once the write cycle starts, the part self-times the remainder of the operation, freeing the microprocessor and the data bus for other tasks. Freedom from an external timing capacitor or other hardware leads to considerable savings in component and assembly expense as well as in board space. In addition, the cost of design is lower because the part is far simpler to operate.

As can be seen in Fig. 2, the timing of a write cycle for the X2816A is as simple as that for a static RAM. The latches are active only during a write cycle, when they hold the addresses and data to allow the microprocessor to use the bus for other tasks. A write cycle is activated by both chip-enable and write-enable lines going low while output-enable is high. The addresses are latched on the last low-going edge of either the chip-enable or write-enable signal. The data inputs are latched by the



2. Like a static RAM. The write-cycle timing for the X2816A EE-PROM looks much like that for a static random-access memory. Although the write cycle takes a maximum of 10 ms, latches hold the address and data signals, freeing the processor for other tasks.

first of those two signals to return to the high level.

Unlike with most EE-PROMs, there is no need to precondition the data at the desired address before the write cycle, for the X2816A automatically performs an erase function immediately after the cycle starts. Both the erase and write of the data occur during the 10-ms write cycle. The condition requiring the output-enable signal to be high to initiate the write cycle ensures that the part will not be mistakenly programmed when the power is switched on or off.

A compatible part

Conveniently, a socket designed for one of the earlier EE-PROMS can accept an X2816A as well. An internal detector on the write-enable pin senses a signal above 12 V and initiates the internal write cycle (and thus the part may second-source the 2816). This high-voltage signal is used only to detect the system's request to write data—otherwise, the part draws virtually no current from the high-voltage supply.

Further, because of their internal control over the write cycle, the Xicor EE-PROMs can plug into the standard sockets of 2-K-by-8-bit static RAMs. They will operate with the signals normally applied to a RAM, with the only restriction being the delay of 10 ms after starting a write cycle before accessing data. As mentioned already, the X2816A is not on the bus and requires no servicing or supervision during this 10-ms wait. Since the parts time their own write cycle, other EE-PROMs may be updated while a write cycle is continuing on the first unit.

The 10 ms quoted is the maximum delay for writing—the typical delay is only half that. By polling the part during its write cycle, a user can usually reduce the waiting time. One method is to place a particular byte of data at some address and then ask for data from that address during the write cycle. If the data that is retrieved checks against the data written, the part has finished its cycle.

With the cost of a single service call to modify a system in the field mounting toward $200, no doubt the system that can be serviced from afar will be an early development goal. With an EE-PROM plus a modem or other communication method, a telephone call suffices to download the program and configuration data pertaining to all or some of the systems tied together in a network.

A prime application for this technique would be a system of point-of-sale terminals for a market chain. Pricing for items could be dumped to all terminals in the system by calling each store and modifying the price look-up table in each terminal. Similarly, gasoline prices at computer-controlled service-station pumps may be remotely updated.

Indeed, from here it is only a simple step to imagine writing programs that learn as they go. A terminal might analyze the way it was being used and adjust itself for optimum performance in a particular application. By the same token, the next wave of automated manufacturing systems may calibrate themselves, hold information about the steps that have been completed, then interrogate themselves to determine their point in the manufacturing process. □

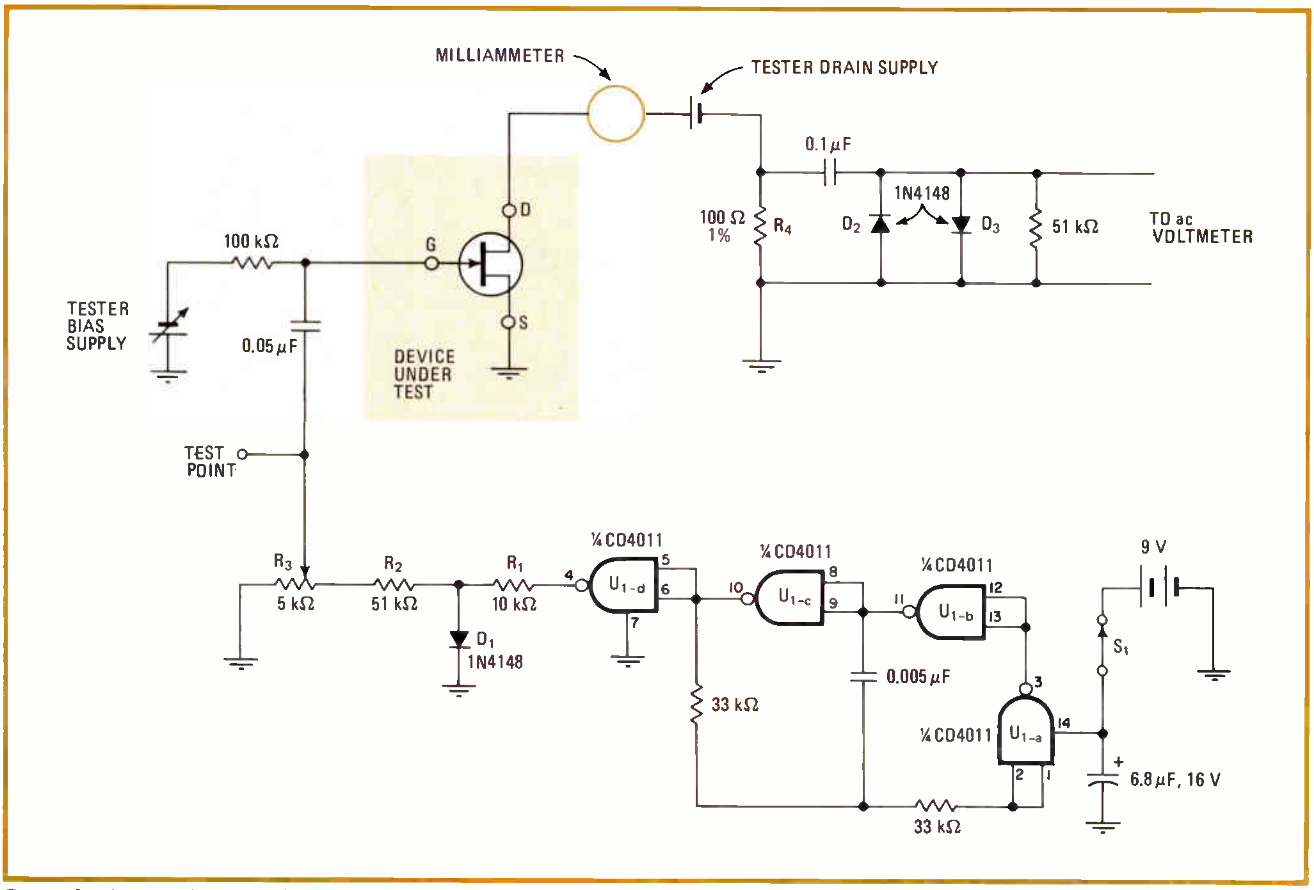
Ac voltmeter measures FET dynamic transconductance

by M. J. Salvati
Flushing Communications, Flushing, N. Y.

Instruments used to test field-effect transistors and MOS FETs make either static transconductance measurements or no transconductance measurements at all. However, when this simple test circuit is combined with a standard ac voltmeter, the modified tester can directly read the small-signal dynamic transconductance of a FET. To accommodate low-transconductance FETs, the circuit requires that the voltmeter's most sensitive range be no higher than 3 millivolts full scale.

NAND gates $U_{1\text{-a}}$ through $U_{1\text{-d}}$ form the oscillator section of the test circuit that generates the test signal. This test signal is a square wave with a frequency of 2,500 hertz, whose amplitude is substantially reduced by the voltage divider consisting of resistors R_1 through R_3 and diode D_1. The diode also stabilizes this voltage by reducing any changes that are due to variations in the power supply.

The 5-kilohm potentiometer R_3 is adjusted until the test point shows an output of 10 mV. As a result, the FET under test produces an output voltage across the sampling resistor R_4, which is placed in the drain path of the FET. This output voltage varies at the rate of 1 mV per millimho of the FET transconductance. The same voltmeter as is used to set the test point at 10 mV must also be used to calibrate the transconductance of the FET. The n-channel FET shown in the circuit is only an example, for p-channel FETs can also be easily calibrated by changing the polarities of the gate and the drain supplies. A typical characteristic curve for the FET under test may be plotted that demonstrates the transconductance versus the gate bias. A similar curve for varying drain current can also be plotted. Gate and drain voltages are adjusted by separate power supplies. □



Dynamic. An ac voltmeter, when linked with this simple test circuit, can be calibrated to read directly the dynamic transconductance of an FET. The test signal, generated by NAND gates $U_{1\text{-a}}$ through $U_{1\text{-d}}$, is fed into the gate of the FET under test whose output across R_4 is measured by the voltmeter. This output voltage varies at the rate of 1 mV per millimho of FET transconductance.

Address checker troubleshoots memory drive, logic circuitry

by F. Chitayat
Canadian Marconi Co., Montreal, Quebec

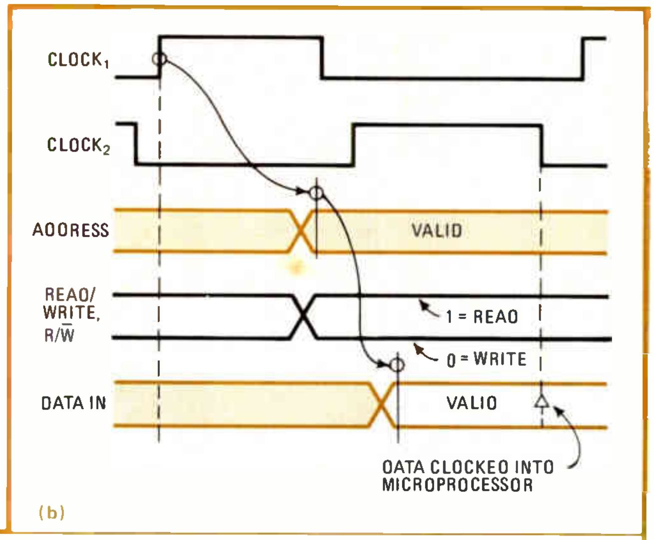
Although error-detecting and -correcting schemes have tremendously enhanced the reliability of microprocessor-based systems, there is still a significant memory failure mode that these schemes cannot detect. If a memory address bit fails due to some problem in the driver or any memory input gate connected to it, the address will be inaccurately written or read. This address checker thoroughly checks for such failures and so complements existing error-correcting schemes. The circuit thus improves the system's troubleshooting capability.

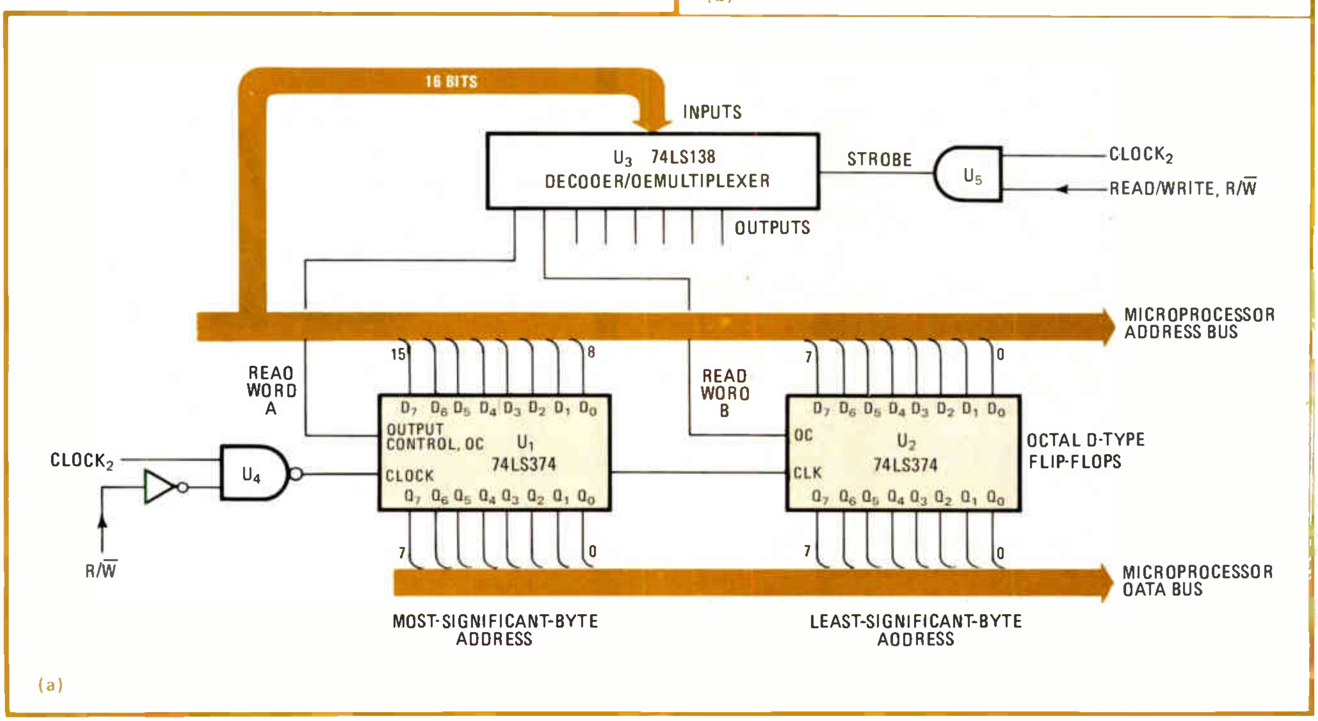
A watchdog monitoring scheme, with the microprocessor programmed to make a certain periodic output that would then be monitored by specialized circuitry, would be only a partial answer, for it would not guard against the failure of more than a few address bits. Instead, the bits checked would generally be only those exercised by the watchdog program. Even if the program ran to 64 locations, at most 6 bits could be checked.

Using this simple circuit, however, the microprocessor clocks the address output onto a register and then reads it back through the data bus. Also, the microprocessor can be programmed to send several test patterns to the circuit by sliding a 1 or a 0 to ensure that every address bit is sent correctly.

The write operation causes the address being written to be stored in registers U_1 and U_2, with the most significant byte stored in U_1 and the least significant byte in U_2. This will not affect the actual writing of the data into the intended address. These registers are read by accessing predetermined memory locations preassigned as input/output locations. In the figure, the specific address locations are referred to as words A and B and are decoded in U_3. When each of these locations is read, the contents of the corresponding register are shifted onto the microprocessor data bus and subsequently read and checked by the microprocessor.

Since a write operation changes the contents of U_1 and U_2, these must be read immediately after a write operation has occurred at the memory-address test location—that is, before another write operation is begun. □





Foolproof. This address checker detects faults in memory addresses due to failures in the driver or receiver associated with each address bit. The memory address being written to is stored in registers U_1 and U_2. Since the registers are automatically clocked by a write operation, the error in the memory address is easily detected by the microprocessor when it reads those registers.

Recovering the clock pulse from NRZ-inverted data

by Doug Manchester
Halcyon, San Jose, Calif.

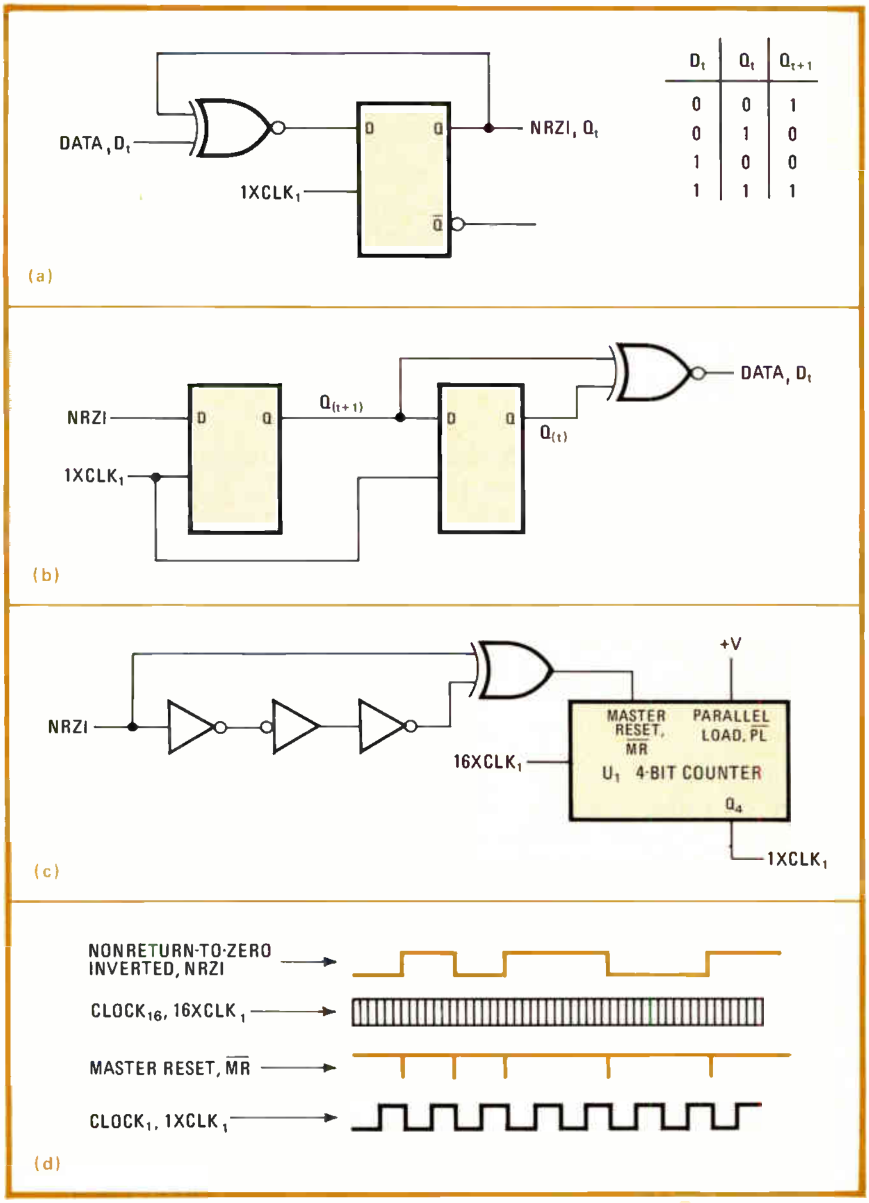
Although most data networks use nonreturn-to-zero–inverted encoding for the incoming data stream, few interface devices can recover a data-rate clock pulse from an NRZI source. However, this NRZI encoding and decoding circuit is capable of recovering not only that kind of clock pulse but also a data-rate clock pulse for synchronous data from an asynchronous modem.

An exclusive-NOR gate and a D-type flip-flop help turn serial binary data into NRZI data. The encoder truth table (Fig. 1a) shows that D_t is the binary data that is encoded at time t, Q_t is the state of the encoder output at time t, and Q_{t+1} is the state of the encoder output at the next bit time.

The NRZI data can be decoded by the circuit in Fig. 1b. This circuit performs the inverse of the encoding function and extracts the relevant information from the received encoded data. The clock frequency is synchronized with the clock pulse used for encoding the data.

The clock-pulse recovery circuit (c) uses a 4-bit counter u_1 to generate the bit-rate clock from the received data and the circuit clock that is 16 times $clock_1$. The counter is reset on every edge transition of data. The received data is sampled in the bit center for maximum distortion tolerance. Distortion as high as 2% per bit for 25 bits is tolerated without resynchronization. The master reset (MR) does not occur on a rising clock-pulse edge (d), for if it rose just prior to that rising edge, $clock_1$ would occur 1/16 of a bit before the bit center. □

Engineer's notebook is a regular feature in Electronics. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $75 for each item published.



Recovery. Using the logic in (a), the binary data is encoded into NRZI data. This NRZI data can be decoded by performing the inverse of encoding function (b). The clock is recovered from the received data by the 4-bit counter U_1 that is clocked at 16 times the fundamental $clock_1$ (c). A typical timing diagram is depicted in (d).

Power-loss detector calls in back-up supply

Many microprocessors need a standby power unit to save the contents of their central-processing-unit registers and memory in the event of a power glitch. An on-board power-loss detector developed by Frank Engelman, a project engineer at General Electric Medical Systems in Rancho Cordova, Calif., generates a signal that first indicates power loss or failure and then triggers a standby power system. **The detector uses just an operational amplifier, a diode, two resistors, and a nonpolarized capacitor.** The diode is connected across the inverting and noninverting ports of the op amp (which functions as a comparator) with its anode and a +5-V dc supply connected to the noninverting port. A parallel RC network is soldered to the inverting port and the diode's cathode. The other end of the network is grounded and, in conjunction with the diode, sets the detector level. Also, a pull-up resistor connects the output to the supply. Under steady-state conditions, the comparator's output is high. When the supply decays, the voltage at the inverting port becomes greater than the voltage at the noninverting port because of the stored charge on the capacitor, resulting in a low signal at the comparator output.

Wire frame coddles floppy-disk drives

Recently a manufacturer of floppy-disk drives was plagued with chassis troubles. The tolerances for these sheet-metal units were too critical, and the drives were causing them to vibrate excessively. On top of this, manufacturing and materials costs were too high. **The solution to these problems was a redesigned steel-wire chassis.** It eliminated the tolerance problem and vibration-damped the frame. The weight of the chassis was reduced by 72% from 18 to 5.1 lb at a cost savings of 32% a unit. For more information, contact E. H. Titchener & Co., 9 Titchener Place, P. O. Box 1706, Binghamton, N. Y. 13902, or call (607) 772-1161.

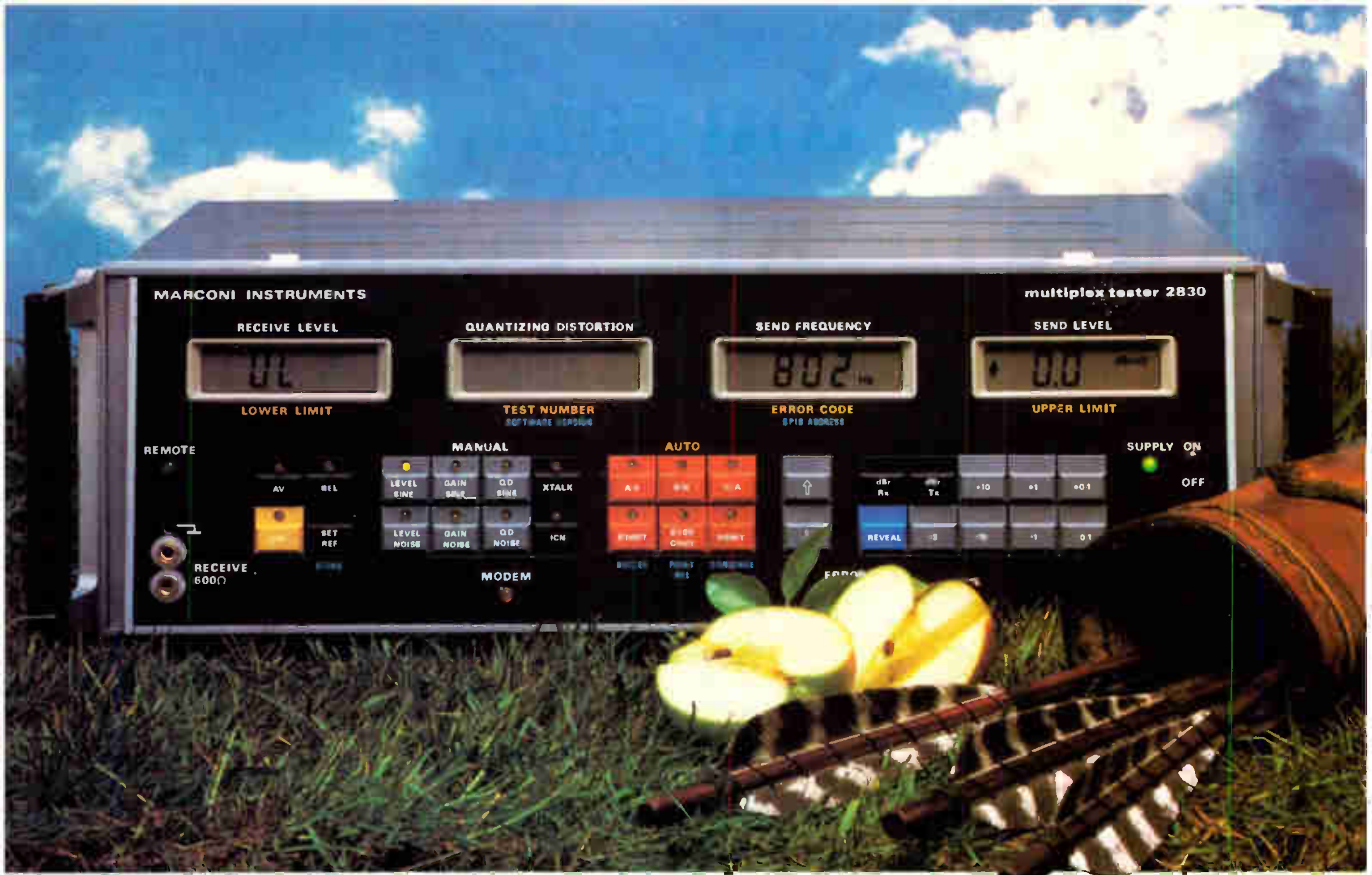
Just how much is a liter?

Is it 3.8 liters to the gallon or 3.8 gallons to the liter? Attempting to ease the inevitable metric changeover in the U. S. is "The Metric System: A Review of Industrial Applications." The applications-oriented book **discusses plans for the metric system, metric programs in private companies, metrification in design,** and metrification in defense groups and in the International Standards Organization. Copies of the $13.50 book can be obtained from the Society of Manufacturing Engineers, 1 SME Dr., P. O. Box 930, Dearborn, Mich. 48128.

Interfacing the 6502 8-bit processor with the outside world

Putting 6502-based control systems in touch with the analog and digital world is the aim of "Advanced 6502 Interfacing," which offers advanced solutions to interfacing the 6502 8-bit microprocessor made by Rockwell International Corp. For those interested in robotics and computer controls, this 190-page book **contains design techniques and circuits that can be used or adapted to virtually any situation where complex computer control is needed.** For example, as a design technique, the author suggests that because the architecture of the 6500 family is very similar to that of the 6800, both may be considered as a resource pool in designing interfaces for either family. Each is designed around a memory as opposed to the register-oriented concept of the 8080 and Z80 microprocessors. "Advanced 6502 Interfacing," book No. 21836, by John M. Holland, is available for $12.95 plus $1 shipping charges from Group Technology Ltd., P. O. Box 87, Check, Va. 24072.

-Steve Zollo



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Circle 137 on reader service card

You said, "Give me a keyboard that laughs at disaster."

Keytek said, "OK."

Introducing the Keytek INDUCTRIC™ keyboard that's impervious to shock, vibration, liquid contamination, electrical interference, temperature extremes, dust...

Keyboards take a lot of abuse. That's why they sometimes act funny, and why sometimes they don't act at all.

But Keytek's INDUCTRIC keyboards are different. They eliminate expensive down-time and repairs because they act right all the time.

Incredibly reliable, thanks to only two moving parts.

The only moving parts in a Keytek INDUCTRIC keyboard are a spring and a plunger with a ferrite core located beneath each key. There are no mechanical contacts or complex components to break. This makes the INDUCTRIC keyboard simple...and incredibly reliable.

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The estimated single component life of a Keytek INDUCTRIC keyboard is 100 million cycles.

Immune to input errors.

Keytek keyboards rely on the principle of inductance. When a key is depressed, the core is moved through a pair of coils etched on the PC board. This generates an output signal through the board's differential transformer circuits.

Because these circuits have such low electrical impedance, INDUCTRIC keyboards are virtually immune to input errors caused by electrical interference from surrounding equipment. They are so rugged, contaminates can literally be washed away with detergent and water.

Intelligent and off-board-scanned models are available, both of which feature true N-Key rollover and operator adjustable touch control for lighter or heavier typing touch.

Hall Effect board features at capacitive board prices.

Keytek INDUCTRIC keyboards cost less than Hall Effect and other inductive keyboards, and they're highly competitive with capacitive and intelligent full-travel membrane types. The reasons are simplicity of design and simplicity of manufacture.

Other keyboard manufacturers still go through the time-consuming process of soldering switching modules to the circuit board. Keytek eliminates this step by etching coils directly onto the board.

The result is a more reliable keyboard for less money.

Learn more about turning disaster into laughter.

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Get all the facts. Call or write Guy P. Russell, Program Manager, Keytek Division, Elco Corporation, 766 N.W. 57th Court, Ft. Lauderdale, FL 33309 · (305) 776-0031.

Keytek Division
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Circle 138 on reader service card

$10,000 buys graphics station

68000-based Multibus system for engineering or CAD runs under Unix, uses monitor with 1,000 by 800 picture elements

by Stephen W. Fields, San Francisco regional bureau manager

Once a designer has had a taste of what he can do with a graphics-based computer system, he doesn't just want access to it, he wants it on his desk. With most systems costing from $60,000 to $80,000 a station, this seldom happens—but a new graphics work station from SUN Microsystems Inc. selling for under $10,000 could make it happen more often.

Called the SUN Workstation, the system is a high-performance graphics computer and terminal aimed primarily at engineering, scientific, and computer-aided design and manufacturing applications. It consists of a high-resolution bit-mapped display, a detachable keyboard, an Ethernet interface, and a 68000-based processor running Unix version 7.

"The idea is to achieve economies of scale," says Andreas Bechtolsheim, director of hardware development at SUN. "The expensive elements such as the disk and the printer are shared, while each user gets a powerful computer, a graphics terminal, and enough memory for most applications. And there is an additional benefit: the work station is quiet—the noisy peripherals can be put in a remote location."

Each work station contains a 1,000-by-800-picture-element 17-in. monitor, with each point on the monitor individually mapped to a bit in the display memory. In the display's base are the power supply and a six-slot Multibus card cage.

Three-slot stations. The basic work station uses three slots for a central processing unit, a frame buffer, and an Ethernet interface. The CPU card contains the 68000, memory management hardware, 256-K bytes of parity-checking memory, five timers for use by the operating system, and two universal asynchronous receiver-transmitters capable of running RS-232-C or High-speed-Data-Link Control-type interfaces. Memory can be added in ¼-megabyte segments.

The 68000 runs at 10 MHz, which, says Bill Joy, who is coming on board as director of software development at SUN, "is roughly comparable to Digital Equipment Corp.'s VAX 11/780 running nonfloating-point applications." Each processor board can support up to 2 megabytes of memory. The CPU board was designed to use the 68010 virtual-memory processor without modification when it becomes available.

All of the hardware required to support demand paging is on the board. Up to 8 megabytes of virtual memory can be addressed by the 68010. "This is especially important," says Joy, "because essentially all current VAX Unix applications will run in an 8-megabyte address space. The software group at SUN is porting the new enhanced Berkeley Unix kernel—4.2 bsd [Berkeley software distribution]—from the VAX to the 68000 to get a paged system on the work station. We expect to introduce this new system in the first quarter of 1983."

The frame-buffer board contains 1-K-by-1-K memory and supports

Commercial outgrowth from Stanford

The original SUN work station was developed at Stanford University by Andreas Bechtolsheim and Forest Basket [*Electronics*, Oct. 20, 1981, p. 46]. Bechtolsheim formed a company, called VLSI Systems Inc., to make the boards and license others to build systems based on the SUN boards.

SUN Microsystems Inc., which supersedes VLSI Systems, was founded this February by Bechtolsheim together with Vinod Khosla (a founder of graphics work-station maker Daisy Systems Corp.) and Scott McNealy, who was director of operations at Onyx Systems Inc., a manufacturer of Unix-based computers. Bill Joy will join SUN next month from the University of California at Berkeley, where he was the main developer of the Berkeley Unix for use with VAX computers.

Two of the companies licensed to build the main SUN boards—the processor and the graphics board—are Forward Technology Inc. of Santa Clara, Calif. [*Electronics*, May 19, p. 14], and Cadlink Inc. of Chicago, which will be marketing a computer-aided design system for metal working. A number of other companies are using the SUN processor board, including Codata Systems Corp., Sunnyvale, Calif. [*Electronics*, April 21, 1981, p. 215], which produces a multiuser Unix system. **-S. W. F.**

New products

"RasterOp". RasterOp is a graphics function with which rectangular areas of display data are modified or combined according to a preselected operation. RasterOp allows complete freedom in painting characters, manipulating windows, scrolling the screen, and drawing vectors. It also lets one page of information be brought in on top of another on the screen. Both text and graphics may be easily moved from place to place on the display. The entire screen can be repainted in about 64 ms.

Unix version 7 distributed by Unisoft is available now to run on the work station. Joy says a disk drive is needed to run it on the station, but he adds that "it is also possible to use SUNs without disks either as programmable graphics terminals or as multiwindow VT100-type terminals or to download programs from other machines.

Initial applications for the SUN work station are for software development and for the original-equipment-manufacturer CAD and CAM market, according to SUN president Vinod Khosla, but there are many applications packages and language products that run on Unix and these are expected to be available for the SUN work station soon.

The basic SUN work station with the 17-in. CRT, keyboard, processor board with 256-K bytes of memory, and the graphics board sells for $8,900. With the Ethernet board, it sells for $9,900. The Ethernet board alone is $1,500. Each 0.75-megabyte memory board sells for $2,500, and the Unisoft Unix is $1,500. Delivery is in 90 days.

Two disk drives are also being offered. Control Data Corp.'s Lark with 8 megabytes each of fixed and removable capacity sells for $8,500. A Fujitsu 85-megabyte Winchester drive sells for $13,900. Both drives come complete with cables. Future additions to the work station include a color-graphics board and monitor and a mouse for screen manipulation. Most of these will be available by the end of 1982.

SUN Microsystems Inc., 2310 Walsh Ave., Santa Clara, Calif. 95051. Phone (408) 748-9900 [338]

Computers & peripherals

5¼-in. drive has 30-ms access time

30-megabyte Winchester uses ST-506 interface, voice-coil head positioning

By applying the electromechanical head-positioning techniques employed in 8-in. Winchesters to its new line of 5¼-in. drives, Atasi Corp. has produced a high-performance 30-megabyte drive that has an average access time of only 30 ms. The system uses the ST-506 standard interface.

According to Don Pate, vice president of marketing at Atasi, the new disk-drive manufacturer is "after the high-performance segment of the 5¼-in. Winchester market, which is primarily the 16-bit Unix computer system. And we define high performance as high capacity—20 megabytes and up—and low access time—under 40 ms average." To achieve this and still remain compatible with the ST-506 standard, Pate says, "means that you can't use a stepper drive for the heads, you have to go to a voice-coil drive. Steppers take too long to find the track and settle on its center. We've developed a way to fold the voice coil into a package that's the standard size for a 5¼-in. drive."

The ST-506 standard calls for modified frequency-modulation coding and a density of 10,416 bytes per track. "From what we've seen," says Pate, "the open-loop servo or stepper drive is limited to about 400 tracks/in. And with 10,416 bytes per track, you get about 4 megabytes per surface." With the Atasi closed-loop servo voice-coil drive, control information is written on one surface after the drive has been assembled. This data controls the voice-coil drive and enables Atasi to achieve a density of 725 tracks/in. Thus three platters have five usable surfaces of about 6 megabytes each.

The company is offering two drives: the 3018 has two platters and an unformatted capacity of 13 megabytes, and the 3030 has three platters and a 30-megabyte capacity. In quantities of 1,000, they sell for $1,470 and $1,800 each, respectively, including the controller. Delivery will begin in August.

No special media. Frank Gibeau, president of Atasi, has spent 17 years building rotating memory at companies including IBM, Sperry ISS, and Memorex. "With our approach to building a high-performance 5¼ Winchester, we don't need plated media or thin-film heads to get a 30-megabyte drive. We are using standard heads and media and a closed-loop servo drive scheme that's 10 years old. The thing we did was to package it in a standard 5¼ drive box."

He notes that other companies offering 30- or 40-megabyte 5¼-in. Winchesters "had to go to nonstandard media or employ different encoding methods such as [more complex] RLL [run-length–limited] codes to get the density. They are still at 150- or 75-ms average access time, and they are not ST-506–compatible." According to Gibeau, "if we went to plated media and run-length–limited codes, we could get to 18,019 bytes per track, which could get us to a 100-megabyte 5¼ three years from now."

Atasi Corp., 235 Charcot Ave., San Jose, Calif. 95131. Phone (408) 942-0770 [369]

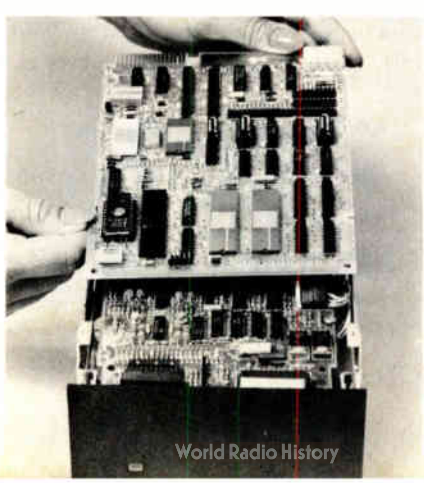
LSI cuts cost of disk controllers

Smart Winchester controllers allow drive changes without modifying system software

Though intelligent controllers for Winchester-disk drives usually have a bit-slice microprocessor and many other bipolar circuits, Shugart Associates' SA1600 series uses just a Z8 one-chip microcomputer and four other large-scale integrated circuits.

The Z8 and a custom LSI device, called the sequencer because it sequences drive operations, together handle formatting, error management, serializing, and deserializing. A second custom chip controls buffer addressing and bus lines, and a two-chip data-recovery system does analog and digital signal processing.

The changeover to LSI promises reductions in microcomputer system software costs, as well as large price reductions for the low end of the market. The Xerox Corp. subsidiary will sell some 1600 models for under $300, or around $200 less than comparable controllers in the company's 1400 series.



There are also 1600 types that are not quite as inexpensive but have software-saving "bells and whistles" that could not be crammed into older designs. Because LSI brings the total number of ICs down to 30, all models fit neatly into floppy-disk–sized 5¼- or 8-in. Winchester drives. Future models will control both floppy- and Winchester-disk drives.

Among the improvements are device independence, distributed arbitration of contention for the Shugart Associates System Interface bus, overlapped seeks, buffering of four data sectors instead of one or two, and a bus rate of 1 Mb/s—up to three times as fast as before.

Plug compatibility. Device independence is tantamount to plug compatibility. In this case, it means that once commands for Shugart's interface bus are programmed into host software, equipment manufacturers can migrate to other storage systems without changing system software. "The same software can be used with 5¼- or 8-in. drives with different capacities, formats, and codes, and with new techniques like vertical recording and optical recording," according to Henry Meyer, product manager. Drives may be changed at any time.

To access new drives, host computers will interrogate the bus during startup to determine what drive types and capacities are available, then use logical-block addressing to read and write data. Users will not be locked into Shugart controllers and drives—other vendors are starting up SASI-compatible product lines. The bus has been proposed as an American National Standards Institute standard for small-computer peripheral interfacing.

Because bus-priority arbitration is now built into each controller, multiple processors can share the drives through Shugart's interface bus. The processors can vary, too. Each processor's input/output bus can be interfaced with the SASI bus with an adapter card.

The old 1400 adapters could be employed, but Shugart plans to produce a new series of microcomputer bus adapters, starting with Multibus and S-100 versions. The new ones will make conventional direct-memory-access controllers unnecessary in most microcomputers. LSI interfaces are also being developed, Meyer adds.

Logical addressing. Addressing is now fully logical because the controller's LSI chip set is programmed to handle physical addressing, error management, and other functions usually performed by host software in low-cost systems. For error checking and correcting, a 32-bit polynomial handles 8-bit error bursts—twice as large as before.

Also, sector addressing is automatically reallocated with a listing of media bad spots stored on disk. That eliminates both the need for spare tracks and the programming of bad-spot information in host software for each drive. The controllers encode data using standard modified frequency modulation.

The first four controllers in the series are: the SA1601-1, priced at $320 in quantities of 100; the -2, at $360; the SA1610-1, at $290; and the -2, which is $330. A 1601 controls up to four 1000, 1100, or equivalent 8-in. drives, and a 1610 controls two 600 or equivalent 5¼-in. drives. The -1 models are similar to the 1400 series, and the -2 models provide the major upgrades. Deliveries are slated for the fourth quarter.

Shugart Associates, 475 Oakmead Pkwy., Sunnyvale, Calif. 94086. Phone (408) 733-0100 [361]

Dense memory checks parity

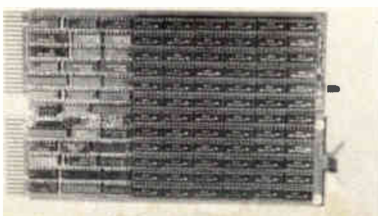
512-K-byte dual-width card for any LSI-11 has register for parity control and status

A 512-K-byte memory card for Digital Equipment Corp.'s LSI-11 microcomputer systems is the first that size to have full on-board support for all Digital's parity-checking functions, says the startup firm offering it. Clear Point Inc.'s dual-width Q-RAM 11 board contains a parity-control and -status register that latches parity-error flags and the associated addresses.

The register makes the board's parity checks available to an LSI-11's system software, which can generate interrupts, address polling, and diagnostics. This feature is not uncommon on ¼-megabyte memory cards but entails external controllers in the case of available boards of higher density, says Vincent P. Bono, the firm's president.

The Q-RAM 11, available in 128-, 256-, 384-, and 512-K-byte versions, is hardware- and software-compatible with all LSI-11-family systems. Employing 64-K random-access-memory chips socket-mounted for easy replacement if faulty, the board has jumper-selectable 18- or 22-bit addressing. It is organized as 256-K words by 18 bits, with each word having 16 data and 2 parity bits. Addressing can begin on any 16-K-word boundary and the parity-control and -status register is programmable to any of eight input/output page addresses standard on Digital hardware. A light-emitting diode on the board flags parity errors.

220-ns access. The board's maximum memory-cycle time is 580 ns. Maximum access time is 220 ns for data read from the Q-RAM 11 and 130 ns for data written into it.



Refresh circuitry is on the board; its maximum refresh-cycle time is 600 ns. Power consumption is low at 13.8 W maximum from a single 5-V supply. The board supports battery-backup systems.

The price of the 512-K-byte Q-RAM 11 ranges from $1,625 for single units to $1,150 for lots of 100 or more. Delivery takes 30 days for orders of up to 10 boards and 60 days for larger orders. Clear Point backs the card with a one-year warranty and a 24-hour replacement service.

Clear Point Inc., 49 Eaton Rd., Framingham, Mass. 01701. Phone (617) 877-9475 [362]

Graphics system also adds word and data processing

Using an advanced distributed multiprocessor architecture, the Beacon color-graphics computer has a graphics performance beyond any existing product priced under $20,000, claims its maker.

The basic system includes control electronics, a detachable keyboard, and a 13-in. color raster-scan display. In addition, standard features include: a 16-bit bit-slice graphics processor having 48-bit microcode and a 200-ns cycle time; a graphics memory of 160-K bytes expandable to 640-K bytes; vector, arc, circle, and rectangle generation by hardware; as well as floating-point arithmetic and mathematics functions. Other processors give the computer word- and data-processing capabilities; standard memory is 128-K bytes, expandable to 256-K bytes.

Disk modules contain up to four 5¼-in. floppy- or Winchester-disk drives in any combination. Desktop modules have up to two intermixable drives. Also available are a 19-in. color or 15- or 19-in. monochrome displays.

Beacon offers 16 graphics and 16 alphanumeric color choices out of 256 colors and has a resolution of 640 by 480 picture elements. Its operating system has enhanced interrupt processing and memory mapping and gives access to thousands of CP/M application programs. Languages include Fortran, Basic, and assembly. Ergonomically designed, the Beacon can be used as a stand-alone processor or under control of a host computer and is priced starting at $12,950 in single units. Delivery takes 60 days.

Florida Computer Graphics, 1000 Sand Pond Rd., Lake Mary, Fla. 32746. Phone (305) 321-3000 [363]

Computer terminals geared toward operator

The Executive 10 and Esprit II computer terminals are designed with the operator in mind. The Executive 10, an addition to the Executive 80 series of smart terminals, offers a wide variety of configurations and options for data entry and inquiry, system control, and software development. It has eight programmable-function keys, a programmable 25th status line, a full set of editing features, a 7-by-10-dot-matrix, a split-screen display, and a business-graphics character set. The Executive 10 is ergonomically designed with a low-profile detachable keyboard. Its display has a nonglare surface to minimize eye strain and will tilt and swivel.

The Esprit II is a buffered terminal capable of displaying the complete ASCII character set. It provides many editing functions that aid the user in data-entry applications like insert and delete line and character, erase field, erase to end of line, and erase foreground, among others. Compatible with the Hazeltine 1500 and Applied Digital Data Systems' Regent 25 and Lear Siegler's ADM-3A, Esprit II has a detachable keyboard with a two-key rollover and a 14-key numeric pad and a nonglare screen for a crisp and clear display.

The Executive 10 is priced at $1,195 in single quantities, and the Esprit II costs $645 in single amounts. Volume discounts are available for both terminals.

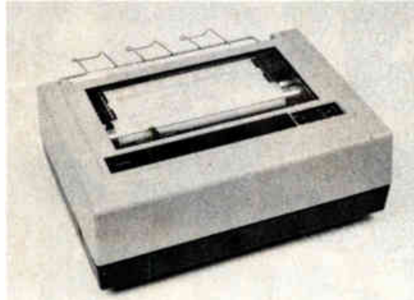
Hazeltine Corp., Commack, N.Y. 11725. Phone (516) 462-5100 [364]

Printer produces full spectrum of colors

With a Flexhammer printhead, the Facit 4544 printer can produce a full spectrum of colors on printouts by using two different color printing methods. One method allows separate use of black, blue, green, or red; the other provides black, cyan, magenta, and yellow that can be used alone or combined to produce any desired color in the spectrum.

The Flexhammer printhead consists of nine flexible hammers that deliver optimum printing with a 100% duty cycle. It requires no adjustments or lubrication and has a working life of 1 billion characters, unmatched by any other print head, claims its maker. Coupled with the 4544's four-color printing capability is a grey-scale mode. Ten different shades can be printed to distinguish different fields of interest.

The 4544 can print curves, diagrams, logotype, and maps, as well as drawings or pictures within an 8-by-14-dot matrix in either normal (10 characters/in.) or proportional



spacings. It has a printing speed of 250 characters/s and up to 535 characters/s with proportional characters. The Facit 4544 will be available in the fourth quarter of this year and is priced at about $5,000.

Facit Inc., 66 Field Point Rd., Greenwich, Conn. 06830 [365]

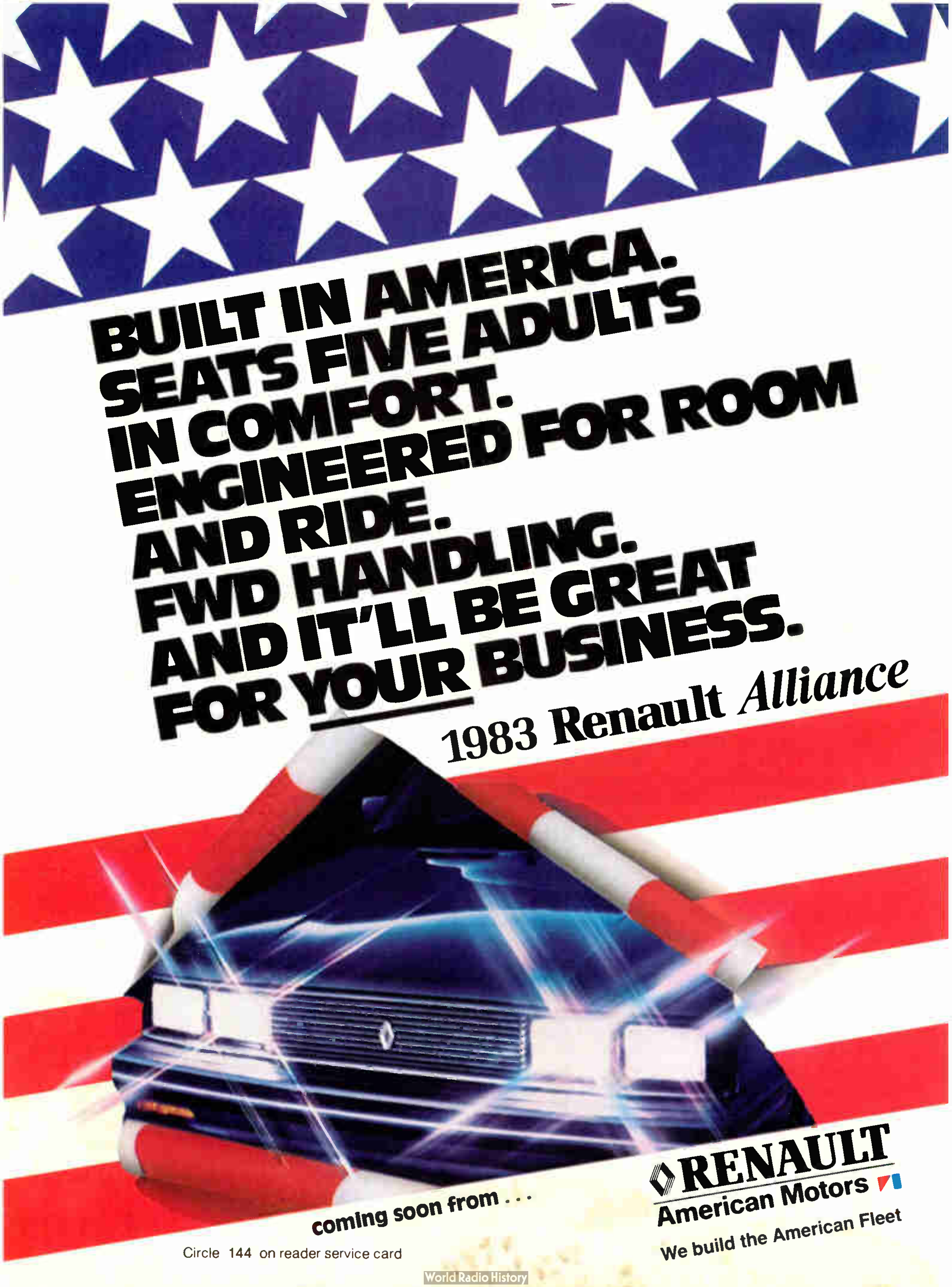
Economically priced plotter offers a speed of 20 in./s

The Zeta 3610 intelligent plotter offers a speed of 20 in./s (on axis), a 0.025-mm resolution, and 2-g acceleration. It costs $25,900 with an integral C53 controller or $23,900 without.

The 3610 has a 36-in.-diameter drum and linear-actuator pen system that accommodates various pen types so that an operator can adjust individual pen pressures. The plotter is available with an option for accepting narrow paper without changing the size of the drum. Standard features include windowing, programmable pause, electronic margin limits, next plot, and grid scaling. With grid scaling, the operator can automatically scale incoming data that will exactly match preprinted forms.

Like all plotters in the Zeta line, the 3610 operates with most computers and protocols. The plotter responds only to upper case ASCII characters, so control characters are not required, and is field-upgradable to the 3620 for applications requiring speeds of 35 in./s on axis and a 4-g acceleration.

Nicolet Zeta Corp., 2300 Stanwell Dr., P. O. Box 4003, Concord, Calif. 94524. Phone (415) 671-0600 [368]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Microcomputers & systems

Unit develops 16032 systems

Terminal built round VME bus gets up quickly thanks to portable high-level software

The Consultant is the first development system available for work with the 16032 microprocessor from National Semiconductor Corp. Its manufacturer, Elite Corp., was able to get it up and running so rapidly because it is based on existing hardware and software designed to develop 68000-based systems. Priced at under $13,000, a complete cartridge-disk–based Consultant can be delivered in 90 days.

The hardware is a desktop terminal-type unit built around the VME bus. Included are high-resolution graphics on a 12-in.-diagonal cathode-ray tube, a detachable keyboard with 83 keys, and a cartridge hard-disk drive with 5 megabytes each of fixed and removable capacity. Made by DMA Systems Corp. of Santa Barbara, Calif., the drive has a 40-ms average access time.

The 16032 microprocessor is supported by memory-management circuitry, provision for serial communications and floating-point hardware, and 256-K bytes of random-access memory, which may be expanded in 256-K-byte increments. The system will support versions of the 16032 running at up to 12 MHz.

Software available for the system includes SSDOS, a multitasking operating system; an interactive text editor; diagnostic, development, and maintenance utilities; and Pascal, Lisp, PL/Basic, and SMPL languages. Cross-development support for the 68000 can be had for all these packages. An interpreter and debugger permits the 16032 to execute code written for the 8080. Support for National's In-System Emulator is also provided.

SSDOS is a portable operating system designed to take advantage of 32-bit architectures. It has been written, says Elite, with few of the artificial constraints that are common in operating systems. Its user interface is an easy-to-understand command language; it provides an environment for real-time process control and related applications, the firm adds. All system software is written in SMPL, a high-level system language that allows the development of efficient portable system software. A globally optimizing SMPL compiler and 16032 code generator are standard packages for the Consultant, but 68000 and 6809 code generators are available.

Languages. PL/Basic is a language readily understandable by application programmers who have used Basic. It also has the high-level structure of PL/1, plus many advanced features—strings and arrays that can be 16 megabytes in size, data formatting and formatted type conversion, high-resolution graphics, multiple-precision floating-point routines (as high as 128 bits), and fill-in-the-blank form-type CRT input/output. The PL/Basic compiler produces fast and efficient code, according to Elite.

A Lisp interpreter and Pascal compiler from Iowa Mountain Software Inc. of Cedar Rapids, Iowa, are also sold for the Consultant. IMS Lisp takes advantage of the pointer and bit-field manipulation provided by the 16032 to achieve execution rates close to those obtained by specialized Lisp hardware.

IMS Pascal meets the extended standards for the language proposed by both the International Standards Organization and the American National Standards Institute. It includes 32-bit integer and decimal data types as well as the standard intrinsic types. A 16032 code generator comes with the language, and machine-code generators targeting the 68000 and 6809 are available.

A display editor and document processor called Poet has editing facilities much like those of Emacs, which is widely used on minicomputers and mainframes. Word wrapping and other text-oriented commands take Poet near the realm of word-processing software.

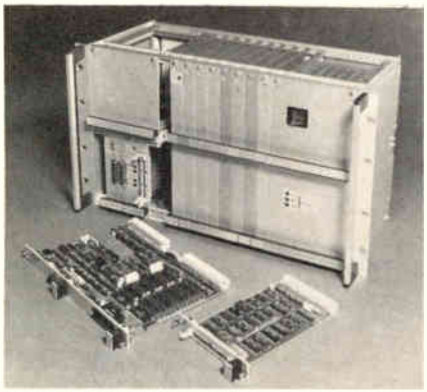
Sam Knecht, marketing vice president, believes the Consultant's processing power will make it popular for both scientific and business uses, in addition to its obvious application in developing 16032-based products. He also sees it as appropriate for original-equipment manufacturers needing a machine with the power for graphics, robotics, and computer-aided design and manufacturing.

With 256-K bytes of RAM, the 10-megabyte half-removable disk drive, SSDOS, PL/Basic, Lisp, Pascal, SMPL, Poet, the 8080-code interpreter, utilities, and diagnostics, the Consultant is priced at $12,400. Additional RAM can be had for $995 for each chunk of 256-K bytes. Other disk drives, printers, and color graphics are available optionally.

Elite Corp., 906 North Main, Wichita, Kan. 67203. Phone (316) 265-0959 [371]

20 products bow for VME bus standard

The VMEmodule family supports the VME bus, a recently announced structure for linking microcomputer



systems that is backed by multiple vendors. The series of 20 modular products will become available in July through the first quarter of the coming year.

Based on the multiprocessing VME-bus system-interconnect standard and Motorola's input/output-channel system architecture, the family includes a single-board microcomputer built around the Motorola 68000, random-access-memory cards, serial and parallel ports, peripheral adapters, analog and digital inputs, a power supply, backplanes, and debugging and monitoring software.

Motorola supports the VMEmodule with real-time system software. The RMS68K real-time multitasking executive package, which can be housed in read-only memory, provides the multiple-task control algorithms needed for real-time applications. For applications requiring mass storage and file management, the VERSAdos disk operating system is available. As examples of prices, the single-board 68000 microcomputer sells for $1,440 and the 256-K-byte RAM card goes for $1,780, both in lots of 25.

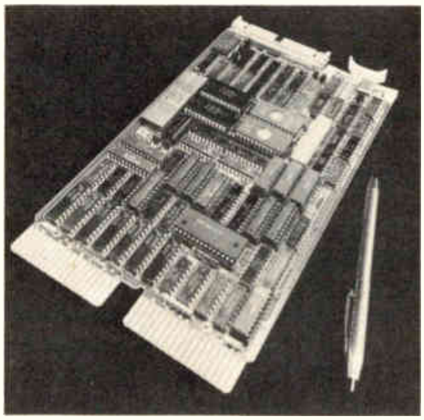
Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 244-5714 [373]

Single-card controller replaces three for disk-drive control

A single-card controller, the WINC-05, can replace three DEC rigid- and floppy-disk drive controllers, the RL01, RL02, and RX02, performing the functions of all three with faster system throughput and greater configuration flexibility.

The system transfers bursts of data at 625 kilobytes/s. Support is provided for either 5-megabyte or 10-megabyte 5¼-in. Winchester drives and 5¼-in. double-density floppy-disk drives. Up to four drives in any combination may be controlled by a single WINC-05.

The WINC-05 is a dual-width embedded controller that can be plugged directly into the central-processing-unit card cage. It may be ordered as a stand-alone unit or as part of a system, including disk drives. It is available now as a dual-width version for Q-bus interfacing and will be available in the third



quarter as a quad-width version for the Unibus. The Q-bus type sells for under $2,000 in single units.

Advanced Electronics Design Inc., 440 Potrero Ave., Sunnyvale, Calif. 94086. Phone (408) 733-3555 [374]

1-megabyte add-on card supports 22-bit addressing

Users of LSI-11/23 and PDP-11/23 Plus computers can add 1 megabyte of memory to their systems with the CDM-82/23R. The memory, packaged on a single quad-sized card, uses 64-K dynamic random-access-memory chips.

The card contains full byte parity as well as on-board software-compatible parity control and status. The CDM-82/23R has on-board refreshing and full 22-bit addressing capability through 4 megabytes. Not only does the memory take up half the slot space of equivalent 256-K-byte module implementations, but it presents only a single bus load for each megabyte of memory.

The single-unit price for the memory is $4,995, which, however, includes either an 11/23 processor card, a VT100 display, or the Fast-disk software. Delivery is from stock.

Cyberchron Corp., P. O. Box 164, Garrison, N. Y. 10524. Phone (914) 424-3755 [375]

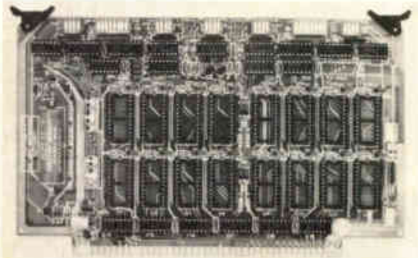
32-K memory module accepts C-MOS or n-MOS memories

Because it allows a mix of devices, the GMS6524 memory module can replace up to three different modules in a system's card cage. The module, which matches the Motorola EXORciser/Micromodule and Rockwell System 65/AIM 65 bus structures, accepts up to 32-K of high-speed random-access memory plus either erasable programmable read-only memory or ROM plus nonvolatile RAM.

The unit can handle up to 32-K by 8 bits of complementary-MOS or n-channel MOS RAM or E-PROM or ROM devices, configured in four independent 8-K banks. Each of the board's sixteen 2-K-by-8-bit sockets may accommodate any of the three types of devices, interchangeably.

The single 5-V module provides 4-MHz operation. With C-MOS devices, power consumption is under 2 μA in the standby mode. In 100-piece quantities, the GMS6524 sells for $233 and is available now.

General Micro Systems Inc., 1320 Chaffey Ct., Ontario, Calif. 91762. Phone (714) 621-7532 [376]



Instruments

DPM links to IEEE-488 bus

\$595 4½-digit panel meter measures dc voltage, has power supply built into case

The model 87 digital panel meter contains within a standard-sized panel-meter case both a power supply and an interface for connection to the IEEE-488 instrumentation bus. At \$595, it represents a new low for the price of adding simple dc voltage-measuring capability to IEEE-488 systems. Until now, instruments built to interface with the bus all have multiple capabilities, many of which are wasted when just a voltage measurement is needed.

A standard two-chip dual-slope analog-to-digital converter with a 400-ms conversion time is used; its accuracy is put at within 0.01% of reading ±1 count after calibration (which can be done from the front panel) or 0.02%±1 count after one year. Maximum linearity error is 0.005%, and the temperature coefficient of full scale is 25 ppm/°C over the range of 0° to 50°C. The normal-mode rejection ratio at the single-ended analog input is 80 dB at 50 or 60 Hz; the common-mode rejection ratio with a 1-kΩ source imbalance is 160 dB at 50 to 60 Hz.

Models are available with one of three voltage ranges: ±1.9999 V, with an input impedance of 1 GΩ; ±19.999 V, with 10-MΩ input; and ±199.99 V, also with 10-MΩ input. Bias current for all three is 10 pA.

Overvoltage protection for the 2-V version is 100 V dc and 75 V root mean square, and for the other two it is 360 V dc and 260 V rms. The decimal point on the 0.56-in.-high seven-segment light-emitting-diode display can be set at any of five positions with jumpers to pins on the rear-edge connector. Polarity indication is automatic.

The 87 uses a low-power version of the 8039 microproccessor, a 2716 erasable programmable read-only memory, and low-power Schottky logic for the bus interface. The current design is a talker only on the bus, but the 8039 and provision for an expansion chip make it possible that future versions could be listeners as well, controlling several output lines to the bus. When used with the Commodore Pet, the model 87 will not hang the interface bus as most other system meters do under certain conditions, the manufacturer says.

The 8039 accepts serial binary-coded decimal data from the converter and formats it for the bus. Software in the E-PROM tells the microprocessor how to recognize commands on the bus and operate as a function of the settings of the 87's switches. The switches, in a dual in-line package, select one of three modes of operation and the meter's address on the bus.

Free running. In the free-running mode, the meter runs continuously: it acquires a voltage reading, converts it, and generates a service request (SRQ) on the bus. It then goes on to acquire another reading. The other two modes are triggered: the trigger in one case is a get command from the bus and in the other case comes from some source external to the meter and the bus.

When triggered, the 87 does one conversion and generates an SRQ to indicate that it is ready, but then waits for another trigger before converting again. In the free-running mode, the last conversion is held and displayed when the external-hold connection is strapped to a logic 0 level.

The 87, which dissipates 3 W, is available with three different power-supply configurations. Two of them let the meter run from 47-to-63-Hz line power at either 190 to 264 V or 90 to 127 V. The third accepts dc power at 5, 12, or 15 V.

Ratio measurements can be made between two analog signals by removing two interval components. Both signals may be brought to the rear-edge connector; the ratio signal may be in the range of 0.8 to 1.2 V, and this input's impedance is 20 kΩ in parallel with 0.68 μF. The meter's 6.4-V internal reference may also be brought out to the edge connector. A shroud is available to protect the connector or a screw-terminal strip assembly may be plugged into it.

In addition to the standard dc-voltage models, meters can be supplied to measure ac voltage or current (with or without true root-mean-square output), other dc voltage and current ranges, or scaled in engineering units. A peak detector or sample-and-hold input can be added, and the plastic bezel can be custom-engraved. Case dimensions are 9.1 by 4.2 by 9.4 cm.

Delivery is from stock; the single-unit price of \$595 drops to \$485 each in lots of 50.

ICS Electronics Corp., 1620 Zanker Rd., San Jose, Calif. 95112. Phone (408) 298-4844 [351]

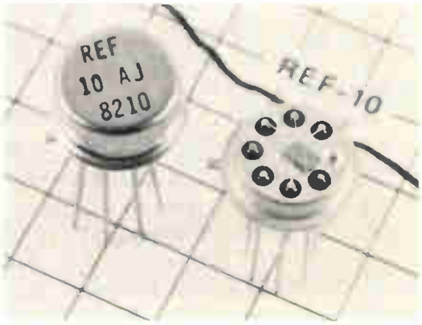
Low-cost pulse generator operates at up to 50-MHz

The Clocksource I pulse generator has a frequency range of 0.5 Hz to 50 MHz and sells for only \$349. Stripped of all features intended for after which samples are drift-tested for 1,000 h.

The output voltage temperature coefficient is typically 3 ppm/°C and 8.5 ppm/°C maximum. The REF-10's input voltage range is from 12 to 40 V. The reference is suited for use in military satellites and industrial applications as well as in portable instrumentation and data conversion systems that require guaranteed stability, low noise, and low power consumption.

The reference is available from stock for $50 each in quantities over 100.

Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, Calif. 95050. Phone (408) 727-9222 [345]



Low-cost Darlingtons are targeted for use in printers

Helping keep the cost of high-speed printers low, a series of inexpensive npn monolithic Darlington transistor pairs suit power-pulsed applications like carriage-motor drives, stepper-motor control, dot-matrix–print-head drives, and other uses that demand high pulse currents.

The Darlington pairs include an integral bias resistance and a clamp diode. The U2TA506, -8, and -10 come in plastic TO-92 packages and are rated at 3 A peak with breakdown voltages from 60 to 100 V. The devices lend themselves to tape and reel automatic insertion.

In lots of 5,000, the U2TA506 sells for 25¢ each, the U2TA508 for 29¢, and the U2TA510 for 33¢. All are available from stock.

Unitrode Corp., 5 Forbes Rd., Lexington, Mass. 02173. Phone (617) 861-6540 [347]

Products Newsletter

Modem can be programmed in many languages

An automatic-dialing communications modem connecting RS-232-C–compatible computers and terminals over phone lines is programmable in any language capable of generating ASCII-character-string commands. The Smartmodem 1200 from Hayes Microcomputer Products Inc. **is built around the Z8 8-bit one-chip microcomputer and incorporates control functions that eliminate the need for telephones or external RS-232-C interfaces,** says the Norcross, Ga., firm. The Bell 212A modem handles both touch-tone and pulse dialing and operates in a full- or half-duplex mode at data rates ranging from 50 to 300 b/s or at 1,200 b/s. Users can also set and modify operational parameters like dialing speed and escape sequences. An audio monitor on the modem lets users check the progress of a call, and the Smartmodem 1200 automatically redials busy numbers. The modem is to be introduced at this week's Comdex show in Atlantic City, N. J.

Graphics added to HP 3000 computers

A new business-graphics package for Hewlett-Packard Co.'s HP 3000 computer line consists of Easychart, Draw, and a capability that allows the HP 2680 laser printer to mix graphics with text. Easychart is a chartmaker that employs a follow-the-example data-entry method. All the user need do is to select the type of chart from those displayed on the screen and then enter data by simply typing over the example. Draw works with a pen plotter to produce multicolor diagrams and text. Text, data, and graphics created by any or all of these software products can be merged into a single document using the Santa Clara, Calif., firm's text and document processor software. **The resulting document can be printed at a rate of 45 pages/min** with the HP 2680, graphics software, and additional memory. Available in 14 weeks, Easychart sells for $3,000 and Draw goes for $4,000. The printer enhancement requires a $6,000 software package, a $2,700 firmware upgrade, and trading in the 256-K-byte memory board and $3,000 for a 1-megabyte memory.

Controller boards with new chips are cheaper

Western Digital Corp. is planning to expand its large share of the floppy– and Winchester–disk-drive controller market with a line of Winchester controller boards. The Irvine, Calif., company will use its new components to trim chip count as well as reduce the price of the boards, which are becoming more popular than unassembled chip sets. **The WD1002 board will use the firm's new 1010 chip, which replaces 35 components,** and will be priced at $195, compared with $245 for the currently available 1001. In early 1983, the price of the 1003 will be lowered to $175, dropping to $150 with the introduction of the 1004 in August of 1983.

Disk-drive maker slashes prices

On the grounds that its manufacturing costs have dropped due to steadily increasing volume, new technology, vertical integration and production, and low-cost off-shore subassembly of components, Tandon Corp., the Chatsworth, Calif., disk-drive manufacturer is slashing prices. Five drives announced at the National Computer Conference in Houston earlier this month carry tabs that Tandon claims are 20% to 35% lower than comparable units. **The firm's top-of-the-line 32-megabyte 5¼-in. Winchester drive, for example, comes in just under $1,000** each for large volumes. Smaller drives in the 20-megabyte range currently sell well above this figure, according to competing manufacturers.

Career outlook

Getting mileage from retreads

The noise about the dire shortage of software programmers and engineers in the computer and allied fields is drowning out an apparently comparable scarcity in another area that employs electronics engineers: process control.

At Monsanto Co., the chemicals, textiles, and materials giant with headquarters in St. Louis, that scarcity has been turned into an asset. The means is a program called the Monsanto–Washington University Program for Retraining and Professional Development, which aims to recycle Monsanto engineers who had been squeezed out of jobs by plant closings and the termination of certain product lines. Other candidates include engineers who had been promoted into managerial and administrative slots but want to return to engineering. Also, the company had found that hiring engineers from other companies was mostly a dissatisfying experience.

The basic program started in 1977. The process-control curriculum was added later on as a one-year pilot project, but because Monsanto needed process-control people so badly and few colleges turn out enough, it has become the major thrust.

The program is thorough and rigorous—no way to spend a relaxed, easy year. Monsanto brings the engineers to St. Louis for 12 months of full-time study. Their salaries continue, and the company also pays tuition and relocation costs. The curriculum at nearby Washington University includes refresher courses, advanced mathematics, and computer skills, as well as other pertinent topics plus a good deal of homework.

All the learning is aimed at application, so in addition to their 42 hours of lectures in the classroom, students do some 40 hours of supervised problem-solving per course. (Training for specific jobs, however, is handled later by Monsanto.) So far, 76 of the 81 engineers who have signed up have completed it, and most were 40 to 50 years old and had more than 20 years apiece with the company. Says a company spokesman, "Considering that they have been out of school a while, their motivation was tremendous."

Success. Although not all the engineers in the program are EEs, the experience of one is typical. Leonard Laskowski was among the first group of Monsanto people to opt for the course. Within two months of his graduation in 1979, he helped update a complex heat-transfer process.

In the view of David Bowen, technical support director in the manufacturing division of Monsanto's textile operation, the program is a smash. "These people are producing results within six months of their return to the field," he says. "One success can pay for a whole year's work for 10 people."

Adds Gerald Kennedy, the manager of technical development for Monsanto's Facilities and Materiel Staff group, "These are very high-powered engineers. They make one improvement, and the money keeps dribbling in forever."

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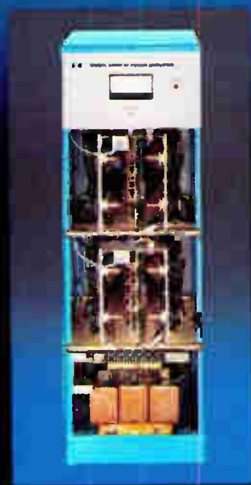

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