OCTOBER 20, 1981

ANNUAL TECHNOLOGY UPDATE ISSUE

Programmable VLSI forces software to the forefront, altering strategies in production, test, and equipment design/114

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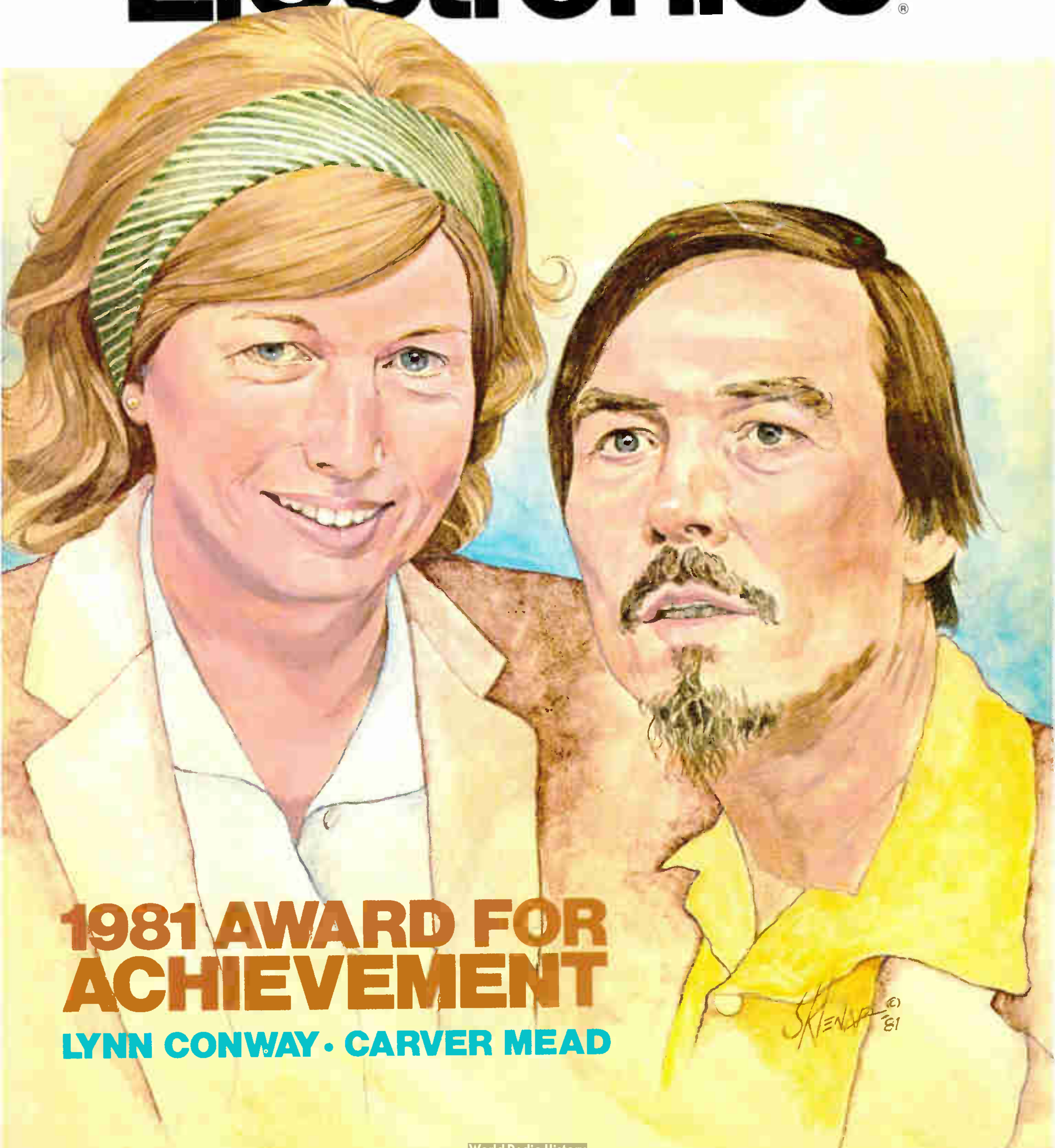


1981 AWARD FOR ACHIEVEMENT

LYNN CONWAY • CARVER MEAD

10. Circuit Testing Update/No. 10 in a series from Hewlett-Packard.

CIRCUIT BOARD TESTING: SHOULD IT BEGIN IN PRODUCTION OR IN THE LAB?

Some successful companies charge production with the responsibility for developing test procedures. Others give the job to the design lab. And with many it's a shared responsibility.

However, if these methods were decided by the standards of yesterday's technology, you may increase today's productivity with a different approach. Consider these points:

Testing options begin in the lab. With today's product designs using microprocessors, memory and other LSI circuits, the question "How to test?" will arise long before a design is released to production. When asked in the hardware/software definition phase, electronic manufacturers can opt for one of three approaches: 1) Not to design for testability, thus leaving test development responsibility to production. 2) Design for go/no-go self test, covering a "critical" subset of board functions, and leaving fault isolation to skilled technicians in production as well as the field. 3) Design for thorough self test, including diagnostics, which facilitate fault isolation, thus providing a total test solution for R&D, production and field service.

Can you afford to design for testability? Let's take a look at the trade-offs. Option 1 appears to offer the shortest design cycle. However, the designer will probably take longer than planned in design turn-on. And design follow-up with production often takes more effort than expected. Longer production test development time is also likely to delay shipments.

Designing in a go/no-go self test (option 2) solves some of the problems associated with option 1. However, a limited self test may still lead to failures at system turn-on. And without fault isolation, expensive technician time will be needed in production and field service.

At first glance, option 3 may seem to require too much of the designer's time. However, the payback can be significant in reduced debugging time and enhanced test effectiveness. After all, the designer best understands the product structure and critical aspects of its operation. And the designer has the tools and the opportunity to implement design features often required for high fault-coverage testing of complex LSI circuitry.

A decision that impacts production most. Whatever the decision, production will feel its effect most. A balance must be found between design time and a viable board test solution. HP provides that balance with the 3060A Board Test System. Equipped with the High Speed Digital Functional Test Option (HSDFT), it delivers the flexibility to solve your μP and LSI board testing problems whether you design for testability or not.

For example, the 3060A can activate μP-based, designed-in stimulus firmware and measure the dynamic board response using Signature Analysis. If self-stimulus isn't available you can use the HSDFT programmable stimulus capability (Figure 1).

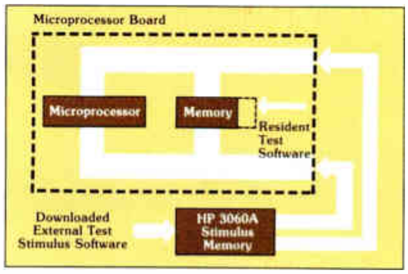


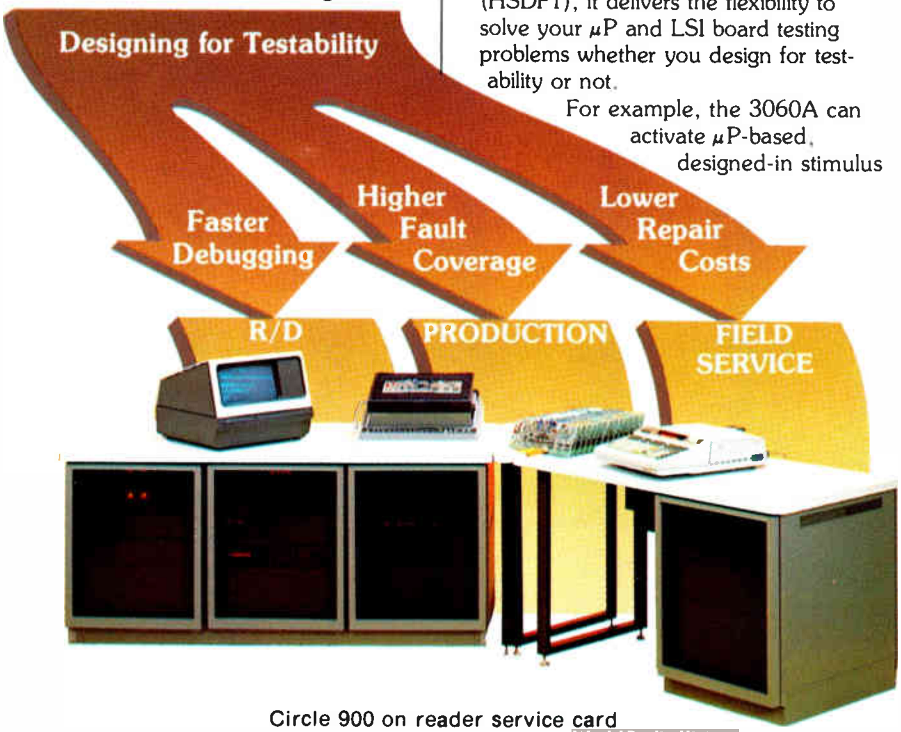
Figure 1 — The 3060A can activate resident test stimulus software or provide that stimulus from its own RAM.

Test stimulus software developed for design turn-on can even be leveraged for production test by downloading from your design system (such as the HP 64000) into 3060A stimulus RAM. Or, alternatively, HP's 3060A Digital Functional Test software provides easy-to-use stimulus and measurement programming procedures.

For fault isolation, the 3060A HSDFT software provides automatic backtracking via in-circuit visibility on the basis of a topological description of the board. And, these procedures can be used as the basis for effective field service repair using HP Signature Analysis instrumentation (HP's 5005A).

The bottom line? Rapid software development, thorough testing, high throughput and efficient field trouble-shooting — the complete solution. That's worth investigating.

For more information. Let HP help you optimize your investment in design, test and service. Write Hewlett-Packard, 1820 Embarcadero Road, Palo Alto, CA 94303. Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.



HP Circuit Testers—The Right Decision

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For bench or system, the new HP 8116A is a prime choice at just $3,440.* But if manual operation meets your needs, we have another outstanding new instrument. . .

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Electronics
The International Magazine of Electronic Technology
Vol. 54, No. 21 • October 20, 1981

114 TECHNOLOGY UPDATE

Electronics

Highlights

Cover: The 1981 Achievement Award, 102

For their efforts to create a common design culture for the very large-scale integrated era, *Electronics* honors Carver Mead of the California Institute of Technology and Lynn Conway of Xerox Corp. Authors of a seminal textbook on structured VLSI design methodology, they have articulated the concept of viewing integrated-circuit design as an extension of integrated system architecture.

The cover is by Art Director Fred Sklenar.

Technology Update, 114

With very large-scale integrated circuits in production, the other electronics industries are keeping pace. As VLSI applications begin to appear, attention turns to software for these programmable ICs.

Semiconductors, 116. Complementary-MOS takes the spotlight, but other digital technologies are advancing as well, including gallium arsenide and Josephson junctions. Linear developments emphasize merged technologies.

Memories, 130. Redundancy is a watchword, but is a point of contention in the struggling 64-K random-access-memory world. Nonvolatile memories are active, except for the departure of many bubble makers.

Components, 144. In data acquisition, the name of the game is added intelligence for greater capabilities.

Packaging & Production, 154. Pin-grid arrays are joining chip-carriers as VLSI packaging candidates, while new generations of processing gear appear.

Test & Measurement, 164. Functional integration and automation are the key to more capable instruments for the more complex VLSI circuitry.

Microsystems, 178. With the 32-bit processor off and running, the silicon system (including support chips) is out of the gate.

Software, 192. Modularity in high-level languages and automatic application-program generators point to major hikes in programming productivity.

Computers & Peripherals, 204. A burgeoning market—office automation—is spurring improved capabilities in terminals and smaller machines, notably personal computers, as well as in storage technologies.

Communications, 216. As data handling grows in importance, transmission channels are ramping up to new levels of capability.

Consumer, 230. Behind snazzy new products like walk-around portable sound systems is a solid base of advancing technology.

The year in electronics: a chronology, 240.

In the next issue . . .

A minicomputer on a chip . . . resistors with the lowest temperature coefficient yet . . . two approaches to electron-beam lithography.

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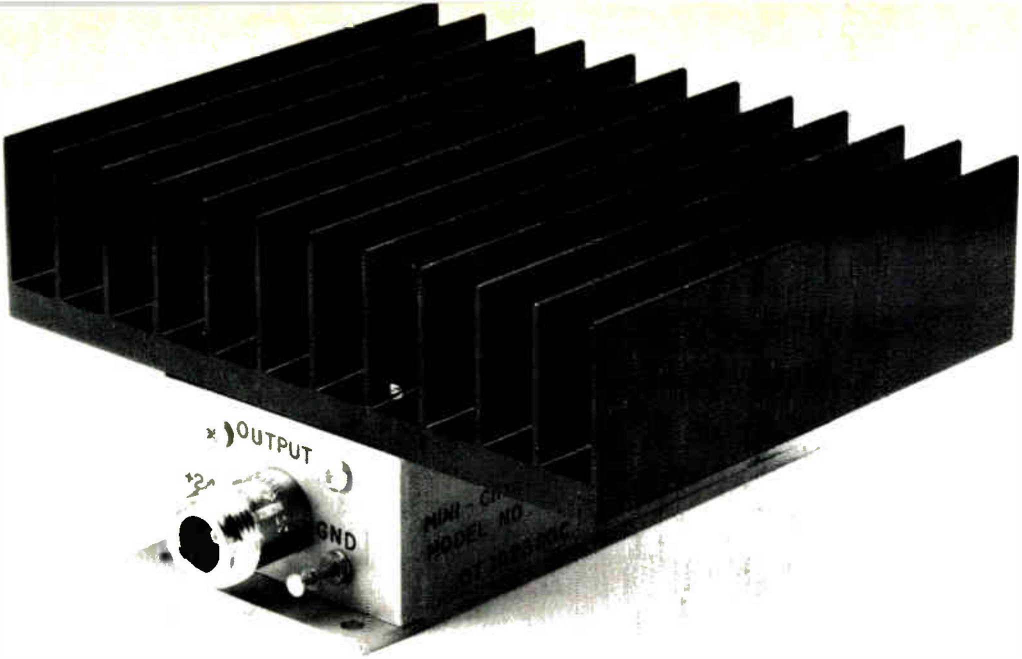

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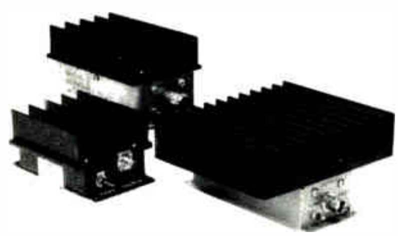

* Model No.	Freq. MHz	Gain dB	Gain Flatness dB	Max. Power Output dBm 1-dB Compression	Noise Figure dB	Intercept Point 3rd Order dBm	DC Power Voltage	DC Power Current	Price $ Ea.	Price Qty.
ZHL-32A	0.05-130	25 Min.	±1.0 Max.	+29 Min.	10 Typ	+38 Typ.	+24V	0.6A	199.00	(1-9)
ZHL-3A	0.4-150	24 Min.	±1.0 Max.	+29.5 Min.	11 Typ.	+38 Typ.	+24V	0.6A	199.00	(1-9)
ZHL-1A	2-500	16 Min.	±1.0 Max.	+28 Min.	11 Typ.	+38 Typ.	+24V	0.6A	199.00	(1-9)
ZHL-2	10-1000	15 Min.	±1.0 Max.	+29 Min	18 Typ.	+38 Typ.	+24V	0.6A	349.00	(1-9)
ZHL-2-8	10-1000	27 Min.	±1.0 Max.	+29 Min.	10 Typ.	+38 Typ.	+24V	0.65A	449.00	(1-9)
ZHL-2-12	10-1200	24 Min.	±1.0 Max.	+29 Min.*	10 Typ.	+38 Typ.	+24V	0.75A	524.00	(1-9)
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Circle 5 on reader service card

Publisher's letter

The **Annual Technology Update** issue has become a ritual at *Electronics*, although the breakneck pace required to produce some 60-odd pages of solid technical editorial (Tech Update is the only issue each year that is entirely staff-written) makes the occasion anything but solemn. In fact, Technology Update is a time for reflection upon what developments took place, what they mean, and what their ramifications will be in the near and far future.

That forward-looking aspect has evolved from the original intention of our first Technology Update seven years ago of assessing a past year's development. It was the astuteness of the technical editors, mainly, that turned what would otherwise be a rehash into a true evaluation of the direction of technology. History assures us that technology doesn't occur in a vacuum: the decline of charge-coupled-device memories, the uncertain future of bubble memories, and other such phenomena should make it clear that technology is but one element in a complex picture involving producibility, cost, marketing, and, of course, timing that all come together to determine whether or not development is truly successful.

That determination is the endeavor of each of our technical department editors in Technology Update. Such information becomes ever harder to find in a set of industries as dynamic as the electronics business. This year, the changing scene is reflected by an expansion of the number of sections to 10 (not counting the Chronology on p. 240): software has earned its place in the ranks of technology, and microsystems and software editor Colin Johnson provides his assessment beginning on page 192.

If there is still any doubt about the importance of the Mead-Conway approach to the design of very large-scale integrated circuits, just try to get an appointment with Carver Mead. With Lynn Conway, he is the winner of *Electronics'* 1981 Award for Achievement for their work in integrating the concepts of device fabrication with those of system architecture.

Mead, in the words of Los Angeles bureau chief Larry Waller, "is the most tightly scheduled person I've ever seen. One of the more academia-industry-integrated people around, his life is a checkerboard of appointments. This past summer included consulting stays at Bell Labs, Boeing, and in Europe, just to give some idea of his travels. Not only couldn't I get more than an hour with him, but students kept coming in to talk to him during that time."

Lynn Conway is an equally hard worker. Martin Marshall of our San Francisco regional bureau in Palo Alto says that the Xerox system designer relaxes by riding her bike and by hiking. And, she keeps cats, whose number keeps varying as they come and go.

Wanted: a consumer/industrial editor

Electronics has open a challenging editorial position for an electronics engineer with a bent for journalism. Right now, we're looking for someone who can write and edit articles on the latest trends in the areas of consumer and industrial electronics, which include video, audio, speech synthesis, and personal computing in the former and robotics and energy management in the latter. A bachelor's degree and experience in design are desirable. We offer excellent salary and benefits. Write a letter telling us about yourself to the Managing Editor (Technical) at *Electronics*, 1221 Avenue of the Americas, New York, N. Y. 10020.

Readers' comments

Overhauling the FAA

To the Editor: Those of us who have read *Electronics* since all airliners had propellers couldn't agree more with your editorial, "The FAA's Sins of Omission" [Aug. 25, p. 24]. For decades you have documented that agency's nonfeasance, indecisiveness, and agonizing foot-dragging. However, "rebuilding the bureaucracy" would be an inadequate corrective measure; "restructuring" is required—both for immediate results and to prevent the otherwise inevitable regression into ineffectiveness. This strategy can be made to work, but its success requires at least two important steps.

The first is that the Institute of Electrical and Electronics Engineers should establish a "shadow" FAA committee to monitor all the Federal Aviation Administration's actions. This would be a highly visible and very vocal group of experts reporting through the business and the consumer press. Full representation should be solicited from airline pilots, the aviation industry, the airlines, the Air Force, and air-traffic controllers—the last of which will eventually begin behaving like a professional association. Specific subcommittees would oversee various existing and proposed air-traffic control systems, such as the instrument landing system (ILS), the ground-controlled approach system (GCA), and the planned automated en-route air-traffic control system (AERA).

The second step would be for Congress to require that one or more seats on each of its committees and subcommittees be held by a public member "designated by the appropriate professional society." These members would not only supply competent technological input to the committee, but also report to their constituency and the public on the performance of committee members.

The key concept here is representativeness. The IEEE members would report on the feasibility, practicality, and state of development of the latest technologies. They could also represent the public. Any IEEE member, and any citizen, could thus contribute ideas through representation in the shadow committee.

Because of the urgency in the specific case of the FAA and its air-traffic control responsibilities, an *ad-hoc* blue ribbon committee, established and funded by the Department of Transportation, should be set up. This would be a short-term proposition and would be discontinued as soon as restructuring was accomplished and properly staffed action groups were in place.

To prevent an inevitable backsliding into bureaucratization, it is imperative to also have in place formal and durable machinery to assist the agency and monitor its performance. Circumstances and expertise have evolved in such a way as to thrust almost the entire responsibility for upgrading air-traffic control upon the IEEE, which many feel has a moral and social obligation to respond with appropriate action. Such a purposeful and worthwhile project cannot fail to add vitality to the institute itself.

In the long run, this immediate restructuring of the FAA will serve as a model for establishing and maintaining high levels of proficiency in all agencies. Those who remember, say, the Common Carrier Bureau's decade of indecision over the status of digital communications might suggest agencies other than the FAA whose bureaucracies are in dire need of restructuring. The operations of the Government that so profoundly affect us all should reflect not only the best that the bureaucracies can offer, but the best that this country can offer.

Henry Stude Jr.
Lutherville, Md.

Corrections

In "Tele-Cause: a match for AT&T?" (Sept. 22, p. 48), IBM Corp. was incorrectly named as a member of the new Washington telecommunications lobby. However, Satellite Business Systems, in which IBM is a dominant shareholder, is a Tele-Cause member. Also in the same issue, the two oscilloscopes from Philips Test & Measuring Inc. described on page 33 have not a 5- but a 50-MHz bandwidth.

Interested in higher performance software?

The Mark Williams Company announces **COHERENT**,™ a state of the art, third generation operating system. **COHERENT** is a totally independent development of The Mark Williams Company. **COHERENT** contains a number of software innovations not available elsewhere, while maintaining compatibility with UNIX*. The primary goal of **COHERENT** is to provide a friendly environment for program development. The intent is to provide the user with a wide range of software building blocks from which he can select programs and utilities to solve his problems in the most straightforward manner.

COHERENT and all of its associated software are written totally in the high-level programming language **C**. Using **C** as the primary implementation language yields a high degree of reliability, portability, and ease of modification with no noticeable performance penalty.

Features

COHERENT provides **C** language source compatibility with programs written to run under Seventh Edition UNIX, enabling the large base of software written to run under UNIX (from numerous sources) to be available to the **COHERENT** user. The system design is based on a number of fundamental concepts. Central to this design is the unified structure of i/o with respect to ordinary files, external devices, and interprocess communication (pipes). At the same time, a great deal of attention has been paid to system performance so that the machine's resources are used in the most efficient way. The major features of **COHERENT** include:

- multiuser and multi-tasking facilities,
- running processes in foreground and background,
- compatible mechanisms for file, device, and interprocess i/o facilities,
- the shell command interpreter—modifiable for particular applications,
- distributed file system with tree-structured, hierarchical design,
- pipes and multiplexed channels for interprocess communication,
- asynchronous software interrupts,
- generalized segmentation (shared data, writeable instruction spaces),
- ability to lock processes in memory for real-time applications,
- fast swapping with swap storage cache,
- minimal interrupt lockout time for real-time applications,
- reliable power failure recovery facilities,
- fast disc accesses through disc buffer cache,
- loadable device drivers,
- process timing, profiling and debugging trace features.

*UNIX is a trademark of Bell Labs

Software Tools

In addition to the standard commands for manipulating processes, files, and the like, in its initial release **COHERENT** will include the following major software components: **SHELL,** the command interpreter; **STDIO,** a portable, standard i/o library plus run-time support routines; **AS**, an assembler for the host machine; **CROSS**, a number of cross-assemblers for other machines with compatible object format with **'AS'** above; **DB**, a symbolic debugger for **C,** Pascal, Fortran, and assembler; **ED**, a context-oriented text editor with regular expression patterns; **SED**, a stream editor (used in filters) fashioned after **'ED'**; **GREP,** a pattern matching filter; **AWK**, a pattern scanning and processing language; **LEX**, a lexical analyzer generator; **YACC**, an advanced parser generator language; **NROFF**, an Nroff-compatible text formatter; **LEARN**, computer-aided instruction about computers; **DC**, a desk calculator; **QUOTA**, a package of accounting programs to control filespace and processor use; and **MAIL,** an electronic personal message system.

Of course, **COHERENT** will have an ever-expanding number of programming and language tools and basic commands in future releases.

Language Support

The realm of language support is one of the major strengths of **COHERENT**. The following language processors will be supported initially:

- **C** — a portable compiler for the language **C,** including stricter type enforcement in the manner of **LINT**.
- **FORTRAN** — portable compiler supporting the full ANS Fortran 77 standard.
- **PASCAL** — portable implementation of the complete ISO standard Pascal.
- **XYBASIC**™ — a state of the art Basic compiler with the interactive features of an interpreter.

The unified design philosophy underlying the implementation of these languages has contributed significantly to the ease of their portability. In particular, the existence of a generalized code generator is such that with a minimal effort (about one man-month) all of the above language processors can be made to run on a new machine. The net result is that the compilers running under **COHERENT** produce extremely tight code very closely rivaling that produced by an *experienced* assembler programmer. Finally, the unified coder and conformable calling sequences permit the intermixture of these languages in a single program.

Operating System

In part because of the language portability discussed above, and in part because of a substantial effort in achieving a greater degree of machine-independence in the design and implementation of the **COHERENT** operating system, only a small effort need be invested to port the whole system to a new machine. Because of this, an investment in **COHERENT** software is not tied to a single processor. Applications can move with the entire system to a new processor with about two man months of effort.

The initial version of **COHERENT** is available for the Digital Equipment Corporation PDP-11 computers with memory-mapping, such as the PDP 11/34. Machines which will be supported in the coming months are the Intel 8086, Zilog Z8000, and Motorola 68000. Machines for which ports are being considered are the DEC VAX 11/780 and the IBM 370, among others.

Because **COHERENT** has been developed independently, the pricing is exceptionally attractive. Of course **COHERENT** is completely supported by its developer. To get more information about **COHERENT** contact us today.

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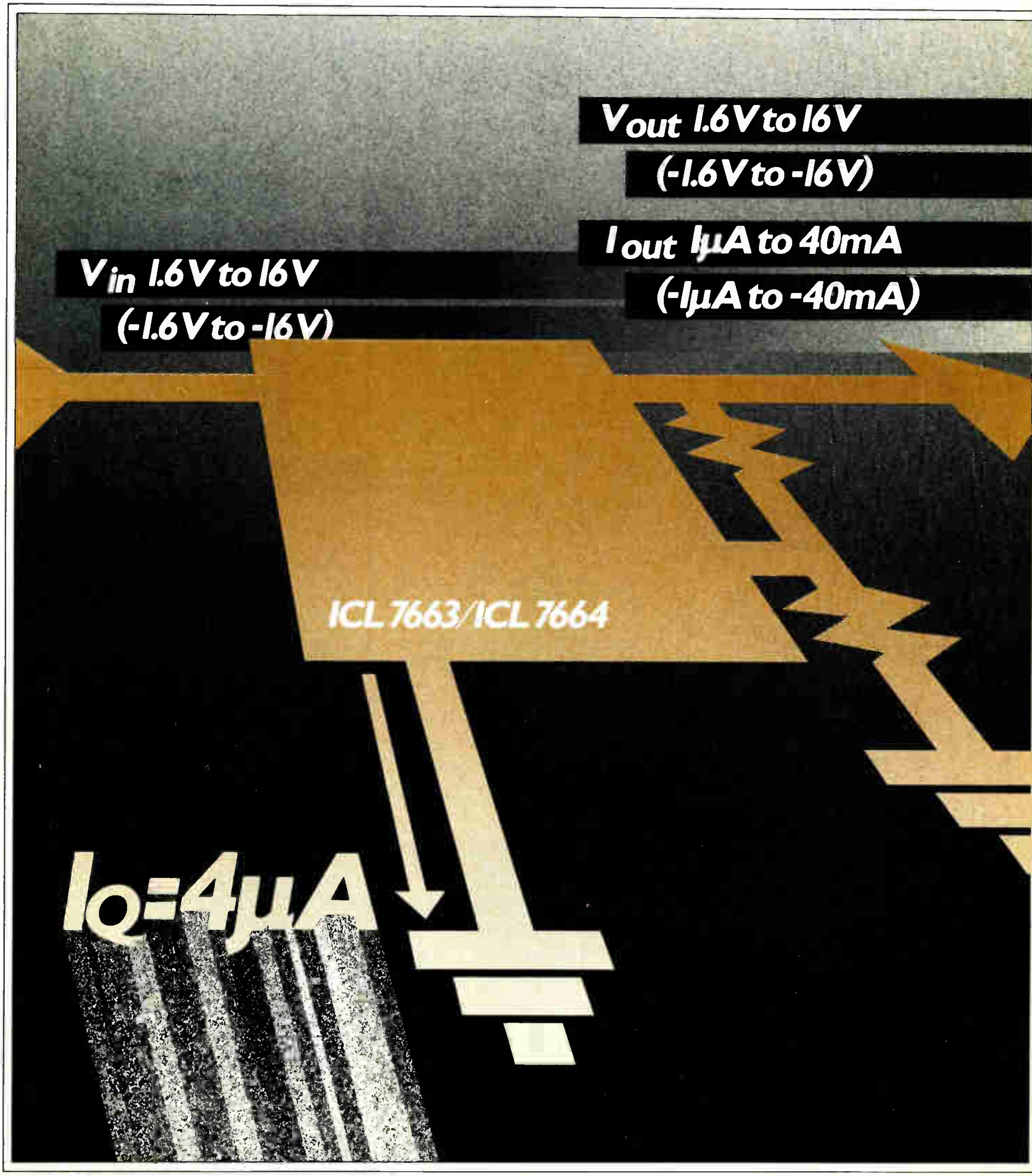

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News update

■ Although designers of custom integrated circuits and their manufacturers have not yet agreed on a standard for test chips, enough progress has been made in the past year to make one a realistic goal.

The desire for a standard, necessary to check performance of short runs of ICs, ballooned last year among a diverse group of university laboratories, Government agencies, and small original-equipment makers who rely on custom designs [*Electronics*, Sept. 11, 1980, p. 44].

Spearheading the development on behalf of the Pentagon's Defense Advanced Research Projects Agency is the University of Southern California's Information Science Institute, Los Angeles. There, Daniel Cohen, now responsible for the program, reports that promising progress has been made.

Measurements. The test structures needed to make parametric measurements have been laid down many times on wafers in production runs. The 40 parameters measured include transistor threshold voltages, inverter-gain and threshold-voltage ratios, diode leakage, and contact resistance. None of these tests are new, but no individual manufacturer has undertaken such a range of them.

In working with manufacturers over the past year, Cohen's group has compiled test data from 10 wafer runs, each holding a total of 800 test strips. Cohen notes that while the test strips are a good start, it will take "two or three years to get enough experience for an industry standard." Another factor to consider is that the ICs themselves are custom devices, not the standard products that dominate the IC field.

Cohen's organization is now pushing ahead to develop drop-in types of on-chip test sites that occupy a full die on a wafer, rather than only a strip on a die. A big part of present work is statistical—correlating data from parametric tests with all-important yield information.

"If you ask me right now if we have an industry standard, I'll have to say no," Cohen says. "But in a few years it could be a different story." **-Larry Waller**

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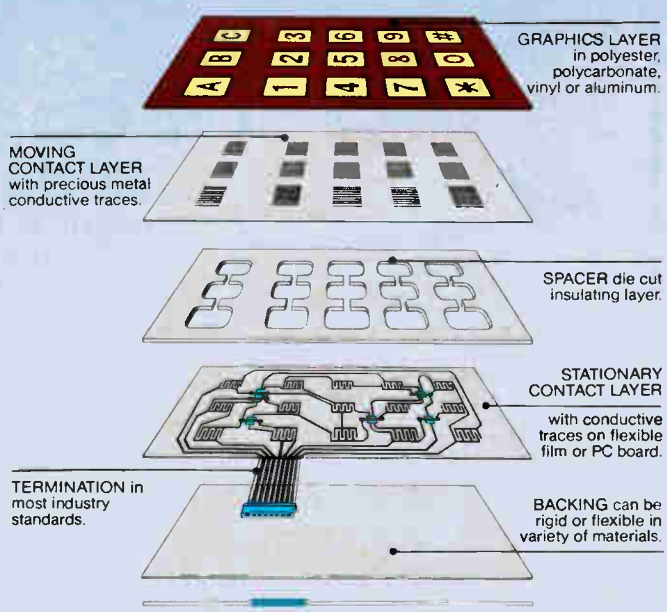

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Circle 13 on reader service card

People

Mostek's Oster foresees device-tailored packages

As semiconductor chip-carriers move into the age of very large-scale integration, designers may soon find themselves tailoring these compact packages with greater frequency to each new device, suggests Carol Oster, the manager of hermetic package development programs at Mostek Corp., Carrollton, Texas.

Keeping an eye on price. Mostek's Carol Oster sees the use of off-the-shelf packages as the key to keeping costs down.

"We are looking at putting more and more things on a single die and asking that one device do many things. And if you are going to do a lot on one die, it's important that the package be much more sophisticated," explains the 37-year-old native of Troy, N. Y. "The trend has been to use standard off-the-shelf packages for as many products as possible, but we are finding we cannot always do that because we see combinations of long narrow chips with pads on the ends and then big fat ones with pads all around."

Despite these pressures, off-the-shelf carriers continue to be a key in keeping the production costs down. "When we were starting up some of our chip-carrier programs, we calculated the cost of bringing them into production as being somewhere between $500,000 and $1 million," says Oster, who joined Mostek in 1978 after working 11 years with Metalized Ceramics Corp.—now Rosenthal Technik North America Inc.—Providence, R. I. "Obviously, we are not in the position to do that 15 times for 15 different devices."

Industrywide standardization of carriers remains one of the most pressing packaging tasks ahead, believes Oster, Mostek's member on the Joint Electron Device Engineering Council package-outline panel. Without industry standards, semiconductor firms will find critical second-sourcing extremely difficult on chip-carriers. And ceramics manufacturers are playing a key role, says Oster, just named a member of the American Ceramics Society's newly formed *ad hoc* committee examining common concerns of the two industries.

Tolerances are one of the biggest concerns, she says. "It's not just being able to make packages the right size and getting closer tolerances, but it's also having to do it at competitive prices," she explains, noting that chip-carrier competition from Japan continues to mount. "What we [the new committee] have begun doing is looking at ways to make the American ceramic-packaging industry more competitive," says Oster, who holds a master of science degree from Clemson University in South Carolina and received her bachelor's degree from Alfred University, Alfred, N. Y., in—what else—ceramic engineering.

Kertzman's Computer Solutions aims high

According to Mitchell E. Kertzman, president of Computer Solutions Inc. in Newton, Mass., high-technology firms inhabit a schizoid world. On the one hand, they must quickly take advantage of brief market opportunities and untapped technologies and do so in the face of increasingly short product lifetimes. On the other, design lead times for their products and vendor delivery times can be painfully long, and unless tightly controlled, the needs of manufacturing and engineering sectors of a

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Kertzman's firm has been dealing with the management problems of high-technology firms for nearly nine years, selling custom software at first, then remote-access to minicomputer-based management information systems (MIS). Now, with its FM/3000 hardware-software package, his firm is entering the MIS merchant market for the first time [*Electronics*, Oct. 6, p. 156].

Kertzman says Computer Solutions was the first firm to offer minicomputer-based, remote-access MIS, and since its founding, it has always targeted the high-technology sector. Clients using its custom software now include GTE Data General Corp., and Foxboro, and Kertzman and his staff have used their experience with these firms to help develop the FM/3000.

Manufacturing management and inventory control can be particularly problematic for high-technology firms, Kertzman insists. "Electronics firms, say, are materials intensive, but their inventory problems often go unnoticed. Also, few industries depend as much on incoming inspection as electronics, and few software packages allow for that. Vendor delivery times, and the tendency of vendors to allocate scarce parts, is another characteristic.

Starting small. "High-tech firms also tend to start small, sometimes as job shops, and then grow rapidly," notes Kertzman. "Managers in such situations need all the help they can get, but it had better be affordable." The Computer Solutions package is inexpensive at $35,000 and includes not just management software but the 3000-40 minicomputer and peripherals, as well.

The FM/3000 addresses these problems, and one other. "Engineers often make poor managers," notes Kertzman. "We would like to think that if an engineer-manager will just keep the data base up to date and scan the monitoring functions of the system once a day, we hope many of his decisions will become obvious." Some engineer-managers probably hope so, as well. □

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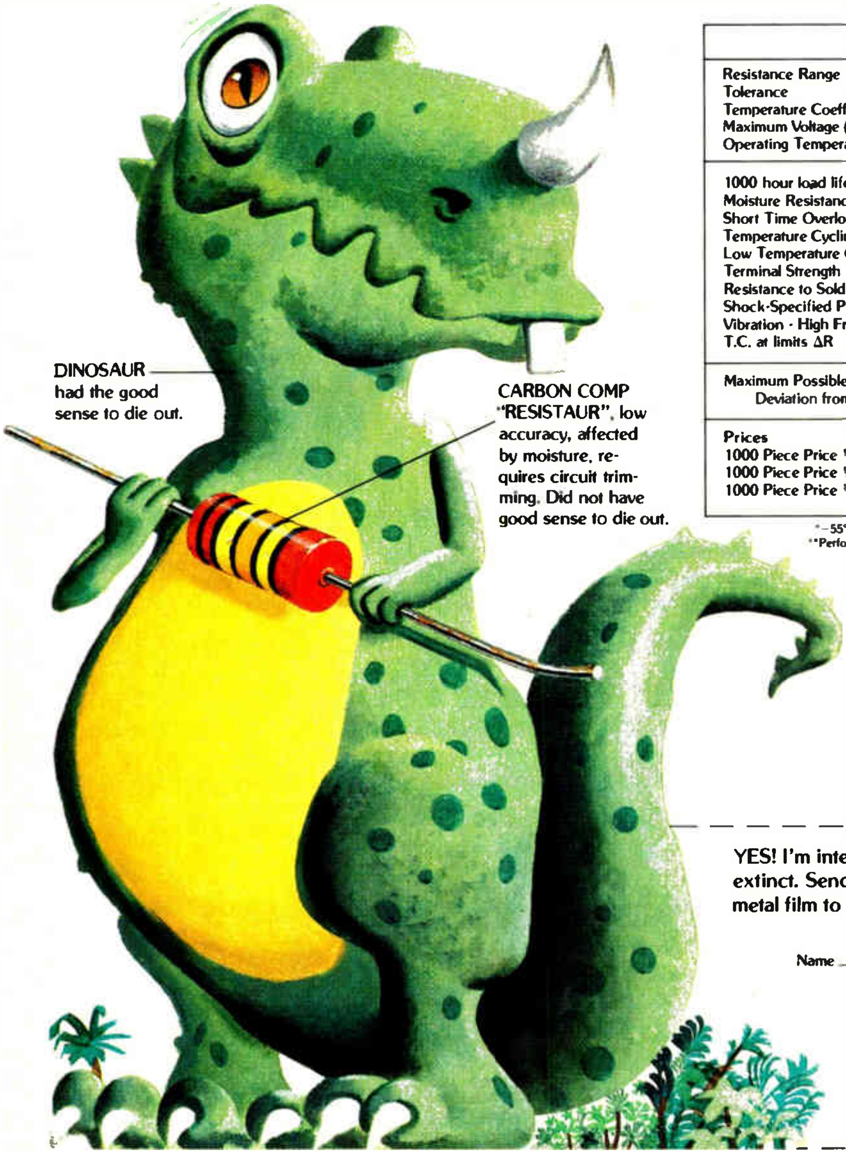

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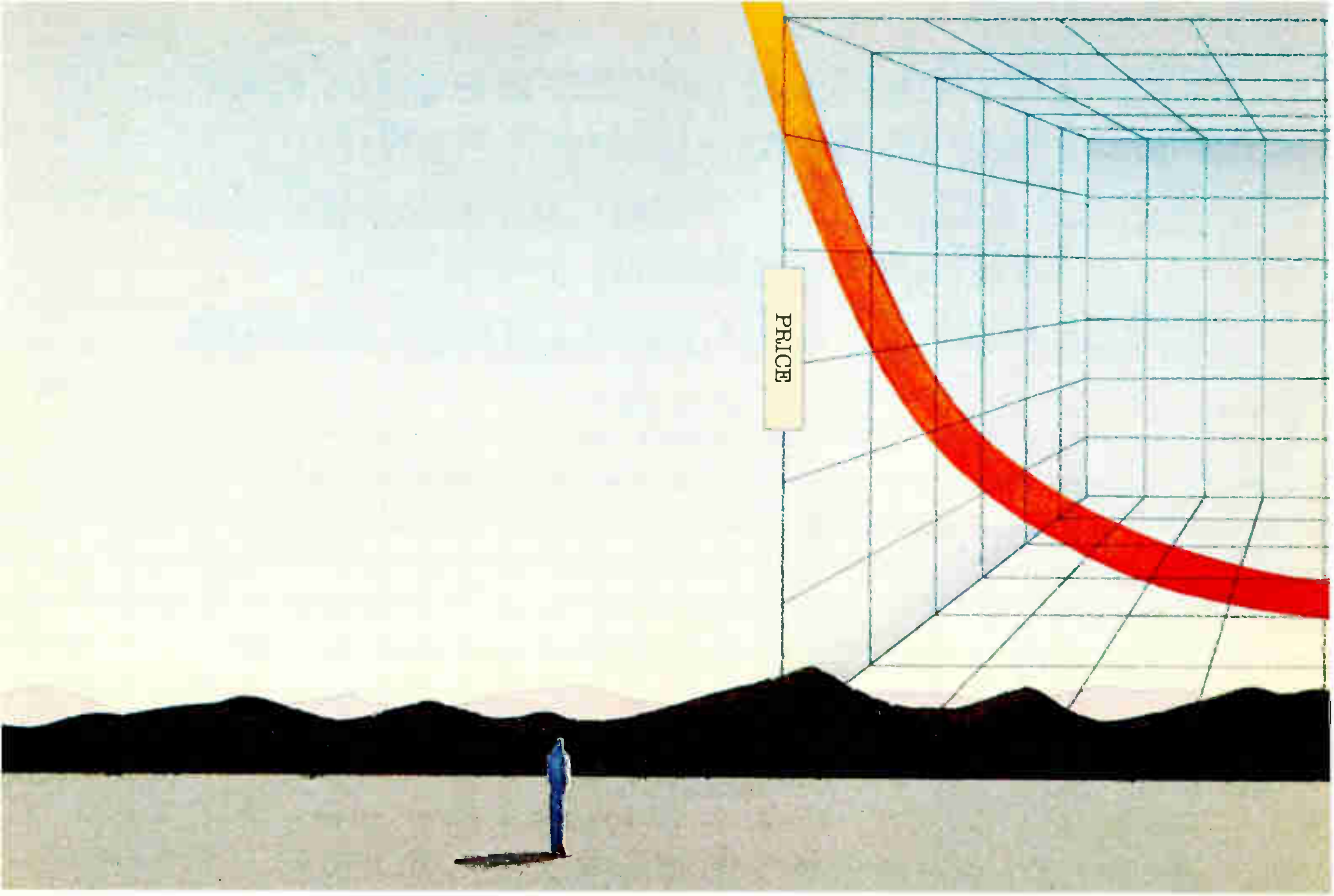

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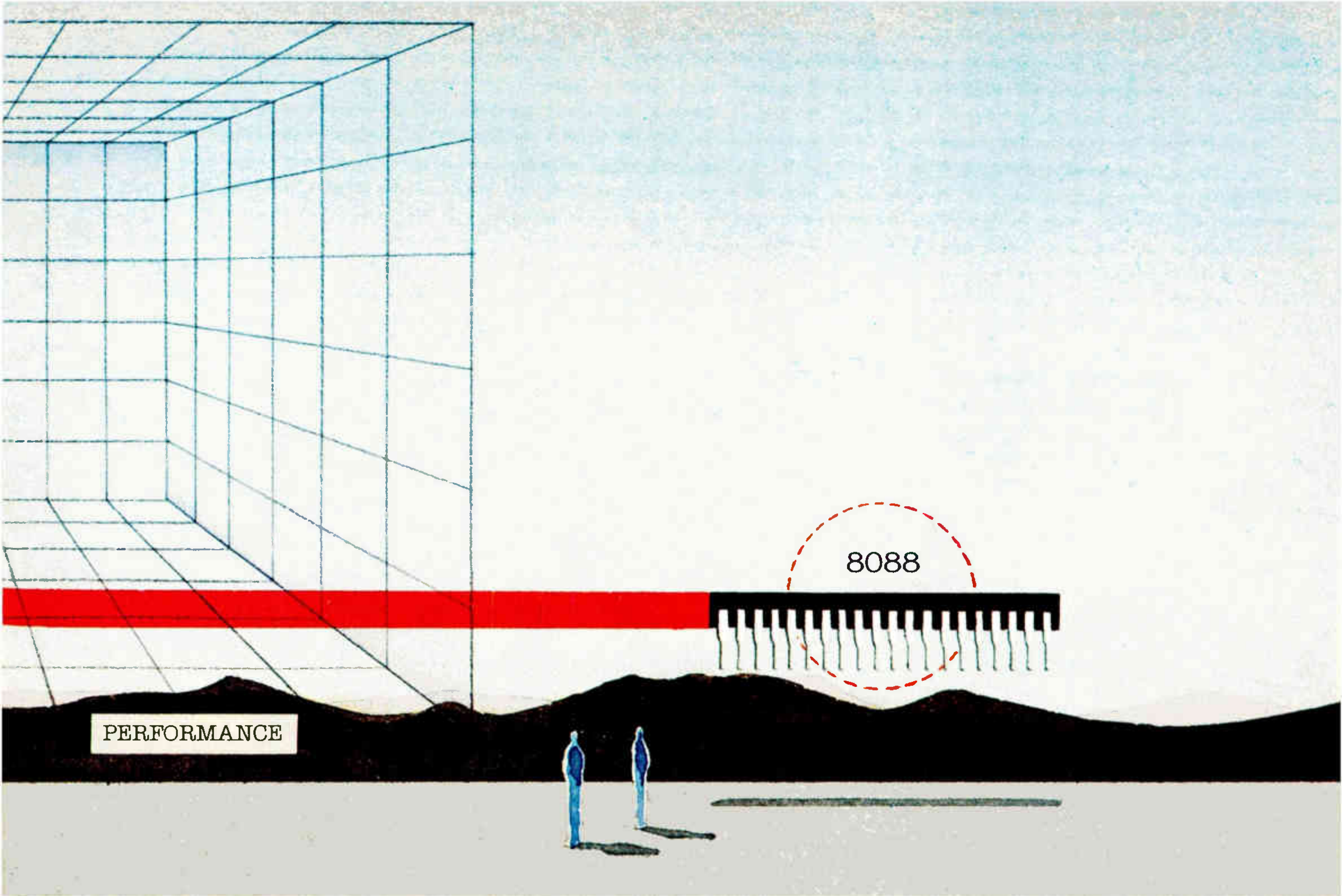
16-bit Multiply	*1.0*	*0.17*	*0.5*
Block Move	*1.0*	*0.75*	*0.49*

Full details of these benchmarks available in the iAPX 88 Book.



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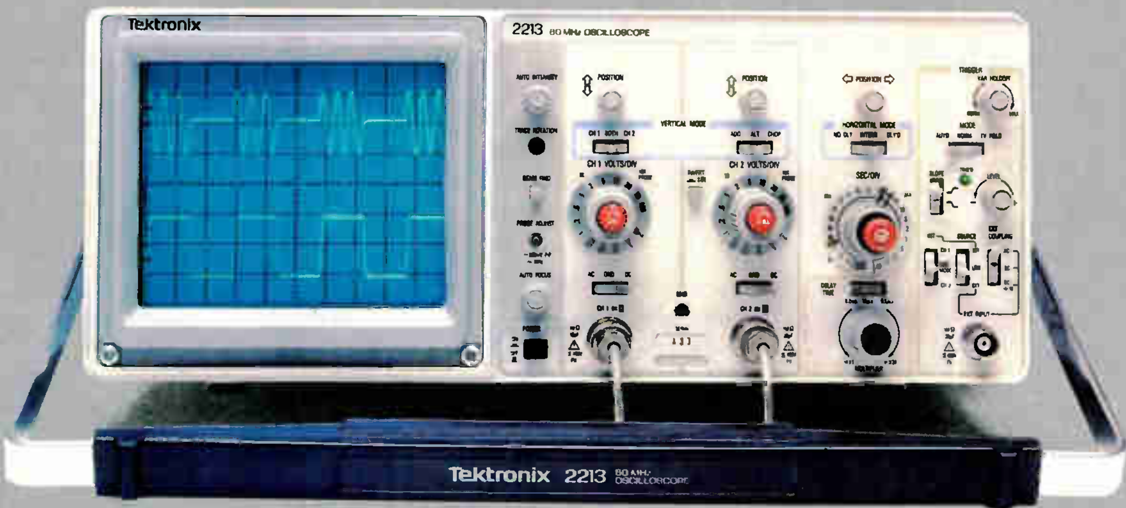

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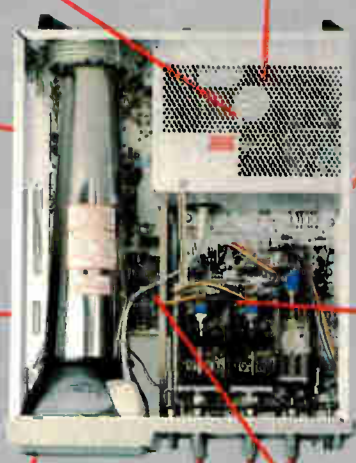

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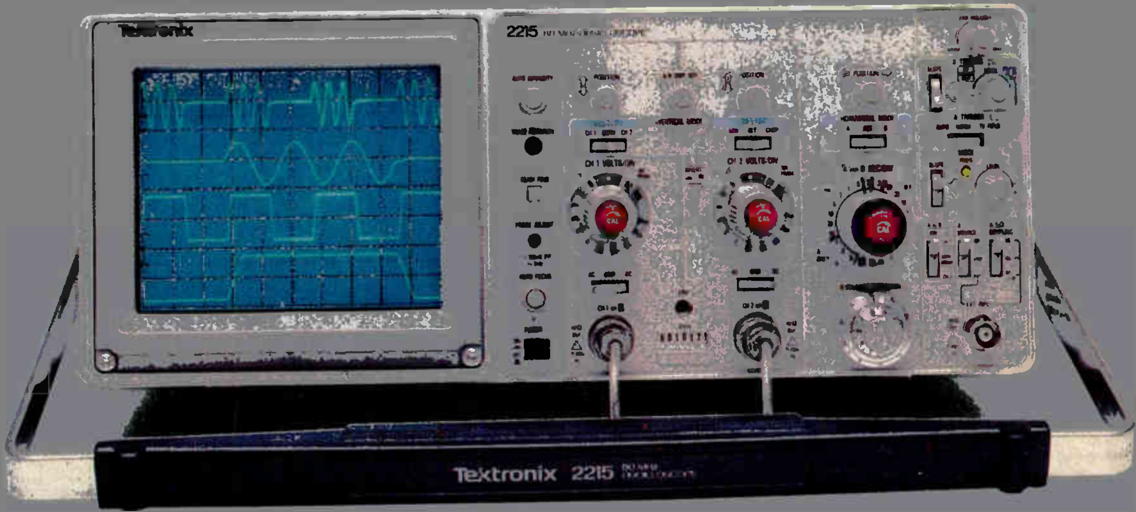

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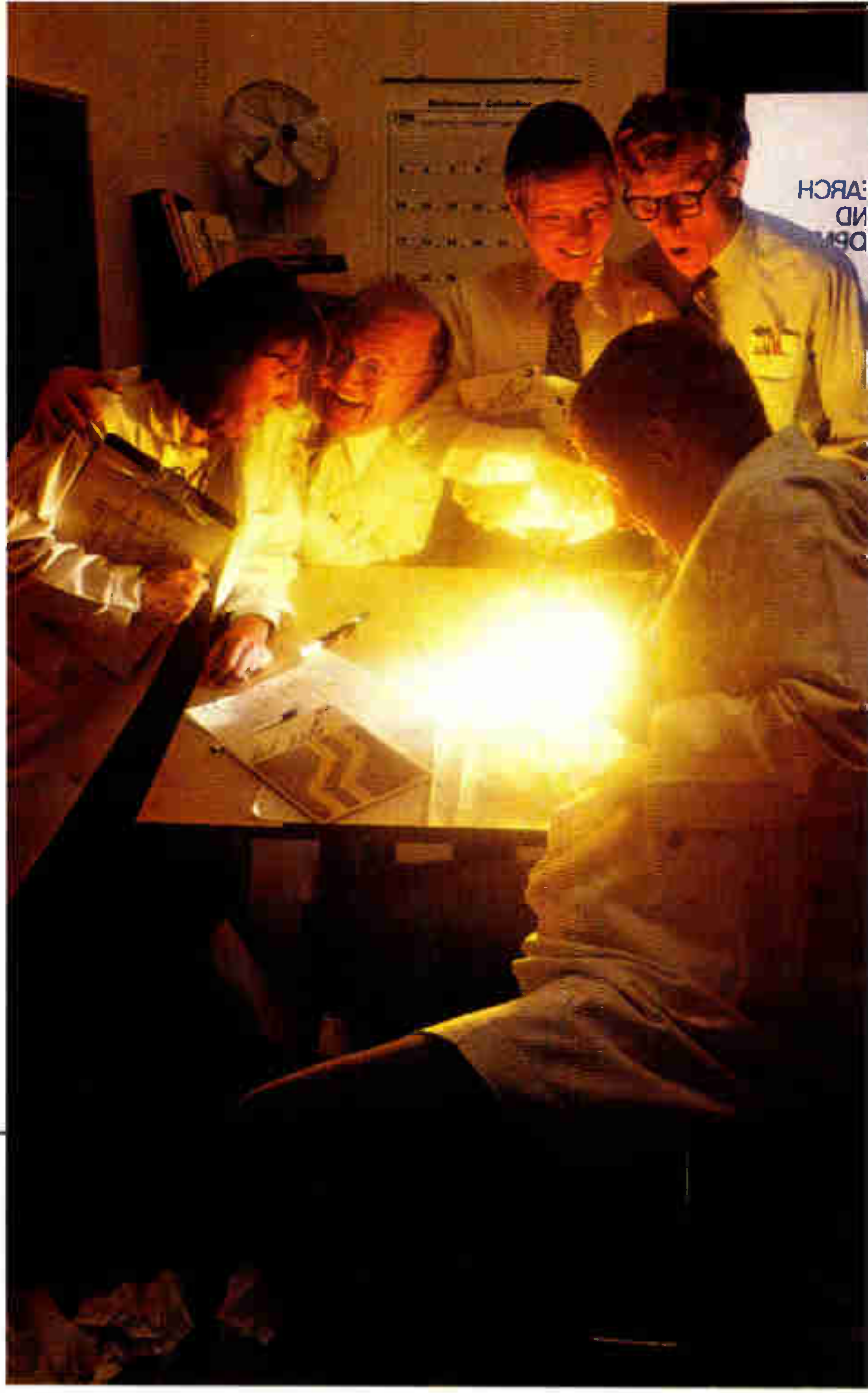

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We've got high performance IMOX LSI families for signal processors, controllers, CPUs, plus all the interface and support you're ever going to need. Not only that, we're using IMOX to make the fastest, most complex proms ever.

And all of them come with a quality guarantee you can't get from anybody else.

If you want the newest, the fastest, the most complete families of high performance LSI, call AMD. We'll show you the light.

The International Standard of Quality guarantees these electrical AQLs on all parameters over the operating temperature range: 0.1% on MOS RAMs & ROMs; 0.2% on Bipolar Logic & Interface; 0.3% on Linear, LSI Logic & other memories.

INT STD 123

Advanced Micro Devices

For more information, call one of our distributors or write the words "IMOX Family" on your letterhead and mail it to Advanced Micro Devices Mail Operation, P.O. Box 4, Westbury-on-Trym, Bristol BS9 3DS, United Kingdom.

Meetings

Midcon/81, IEEE (Electronic Conventions Inc., 999 N. Sepulveda Blvd., El Segundo, Calif. 90245), Hyatt Regency O'Hare Hotel, Chicago, Nov. 10–12.

27th Annual Conference on Magnetism and Magnetic Materials, IEEE *et al.* (H. C. Wolfe, American Institute of Physics, 335 E. 45th St., New York, N. Y. 10017), Sheraton-Atlanta Hotel, Atlanta, Ga., Nov. 10–13.

Productronica 81—4th International Trade Fair for Manufacture in Electronics, Münchener Messe- und Ausstellungsgesellschaft GmbH (Postfach 12 10 09, D-8000 Munich 12, West Germany), Trade Fair Center, Munich, Nov. 10–14.

14th Annual Connectors and Interconnections Symposium, Electronic Connector Study Group Inc. (P. O. Box 167, Fort Washington, Pa. 19034), Franklin Plaza Hotel, Philadelphia, Nov. 11–12.

Eascon—Electronics and Aerospace Systems Conference, IEEE (Robert D. Briskman, Comsat General Corp., 950 L'Enfant Plaza S. W., Washington, D. C. 20024), Washington Hilton Hotel, Washington, D. C., Nov. 16–19.

Integrated Optics and Millimeter and Microwave Integrated-Circuits Conference, International Society for Optical Engineering *et al.* (SPIE, P. O. Box 10, Bellingham, Wash. 98227), Von Braun Civic Center, Huntsville, Ala., Nov. 16–19.

4th Digital Avionics Systems Conference, IEEE (Cary R. Spitzer, Mail Stop 472, National Aeronautics and Space Administration Langley Research Center, Hampton, Va. 23665), Stouffer's Inn, St. Louis, Mo., Nov. 17–19.

Electronic Display Device Exhibition, Electronic Industries Association of Japan (3-2-2 Marunouchi, Chiyoda-ku, Tokyo 100, Japan), Science Museum, Tokyo, Nov. 17–20.

National Telecommunications Conference and Exhibition, IEEE (J. W. Joyner, South Central Bell Telephone Co., 518 Baronne St., Room 1035, New Orleans, La. 70140), Marriott Hotel, New Orleans, Nov. 29–Dec. 3.

International Electron Devices Meeting, IEEE (Melissa Widerkehr, Courtesy Associates, 1629 K St., NW, Washington, D. C. 20006), Washington Hilton Hotel, Washington, D. C., Dec. 7–9.

Infrared and Millimeter Waves Conference and Exhibition, IEEE (K. J. Button, Massachusetts Institute of Technology, National Magnet Laboratory, Cambridge, Mass. 01239), Carillon Hotel, Miami Beach, Fla., Dec. 7–11.

Computer Networking Symposium, National Bureau of Standards and IEEE (Robert Toense, B226 Technology Buildings, NBS, Washington, D. C. 20234), NBS, Gaithersburg, Md., Dec. 8.

Winter Simulation Conference, IEEE (Claude Delfosse, CACI Inc., 1815 North Fort Myer Dr., Arlington, Va. 22209), Peachtree Plaza Hotel, Atlanta, Ga., Dec. 9–11.

First Military Computers & Software Seminar, American Defense Preparedness Association (ADPA, 900 Rosslyn Center, 170 N. Moore St., Arlington, Va. 22209), Sheraton National Hotel, Arlington, Va., Jan. 27–28, 1982.

Seminars

Intel Corp. offers a wide selection of workshops during the fall and winter dealing with its microcomputer components, boards, software, operating systems, and design tools. The workshops are held frequently in cities that include Boston, New York, Chicago, Dallas, and San Francisco. Sessions are offered as well at customers' facilities. For more information, write to Intel Corp., Customer Training, 27 Industrial Way, Chelmsford, Mass. 01824.

Synchronous Communications Interfaces with X.25 capability.

MDB makes the difference!

The industry's only DUP-11* compatible interfaces for Q-bus* (as well as Unibus*) computers are now available with support for X.25, the international data communications protocol. This means that the popular MDB DUPV-11 (Q-bus) and MDB DUP-11 (Unibus) synchronous communications interfaces are ideally suited for use in public common carrier packet-switched networks and multi-computer or terminal communications.

In addition to X.25 capability, the interfaces offer a number of significant performance advantages above and beyond their functional equivalency and software compatibility with DEC. The small size quad boards will accommodate BI-Sync and DDCMP in byte control and SDLC, ADCCP and HDLC bit-oriented protocols with programmable character lengths and complete hardware error control. For Q-bus users, this is big system protocol handling never available before.

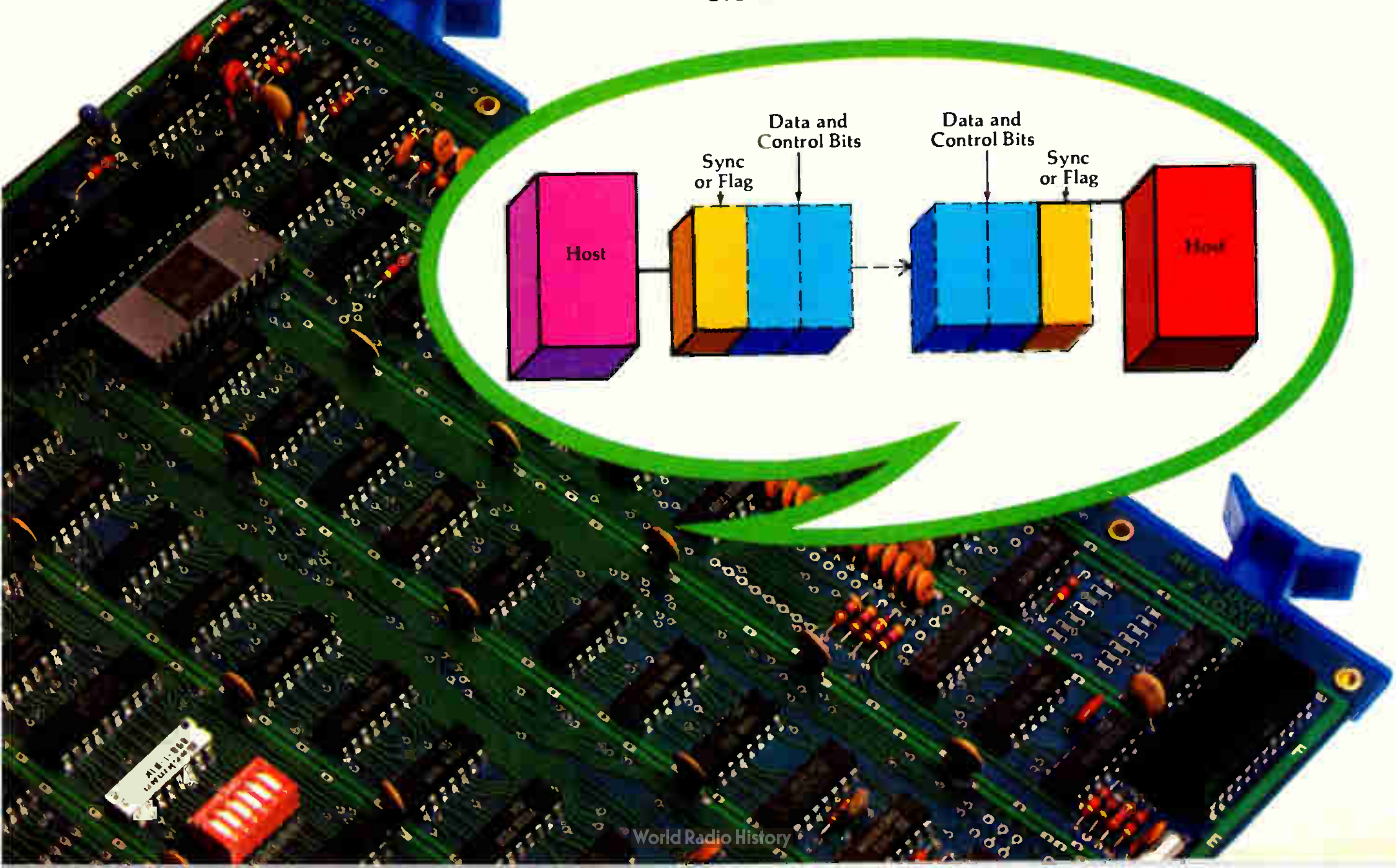
But that's not all the difference MDB interfaces can make to your system. MDB offers line printer controllers for over 100 computer/printer combinations and some of them test themselves. MDB makes the only DZ11 compatible multiplexors for DEC's LSI*11 series — and RS-422 is available. We offer PROM modules with window mapping, asynchronous serial interfaces, LSI-11/23 box systems with 22 bit addressing, and a wide range of products for Data General, Perkin-Elmer and IBM Series/1 computers. Our boards are warranteed for a full year, many are available off-the-shelf and they can be purchased under GSA contract #GS-00C-02851.

Let MDB make a difference in your system.

*Trademark Digital Equipment Corporation

Circle 24 for featured product data.
Circle 25 for general information.

MDB SYSTEMS INC.
1995 N. Batavia Street
Orange, California 92665
714-998-6900
TWX: 910-593-1339



VLSI forces a change in product design strategies

If there is one clear message that is embodied in the pages of our Technology Update issue, it is that the era of very large-scale integration is indeed upon us, bringing with it radical changes in the way electronics companies think about product design and strategic planning. In the wake of VLSI, we foresee even more profound efforts, involving changes in the very structure of the semiconductor industry, shifts in the added value contributed by equipment manufacturers, and dramatic alterations in the traditional roles of component and equipment suppliers.

Already some of these changes have become apparent. Witness the evergrowing list of new ventures offering custom and semicustom VLSI services, for example. Add to this the so-called silicon foundries that are now being established—fulfilling the prophecy made by our Achievement Award winners Carver Mead and Lynn Conway (see p. 102). Finally, mix in the frantic activity in the development of computer-aided design systems, and you have the makings of what can easily be called another revolution.

As we see it, this revolution will tend to move VLSI design away from the exclusive and sacrosanct domains of a few high priests residing in the semiconductor companies and will place more chip design capability directly in the hands of the designers resident at the equipment manufacturer. As this occurs, all participants in semiconductor technology—vendors and buyers alike—must then reassess their roles and their futures.

Obviously, the mass-produced programmable component will be with us for the foreseeable future. But inexorably the cost of CAD and custom fabrication will come within reach of many product planners whose only option right now is to design with commodity components. Once freed from the restraints imposed by the latter, who can predict the course of electronic functions in the years ahead?

Opportunity, not license

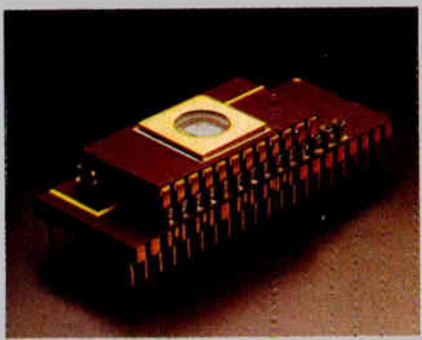
We often disagree with the opinions and the methods of Irwin Feerst, the irascible critic and implacable foe of the Institute of Electronic and Electrical Engineers. But an item in his September newsletter circulated to members of his "Committee of Concerned EEs" caught our eye, and we have to admit the umbrage he expressed was fully justified.

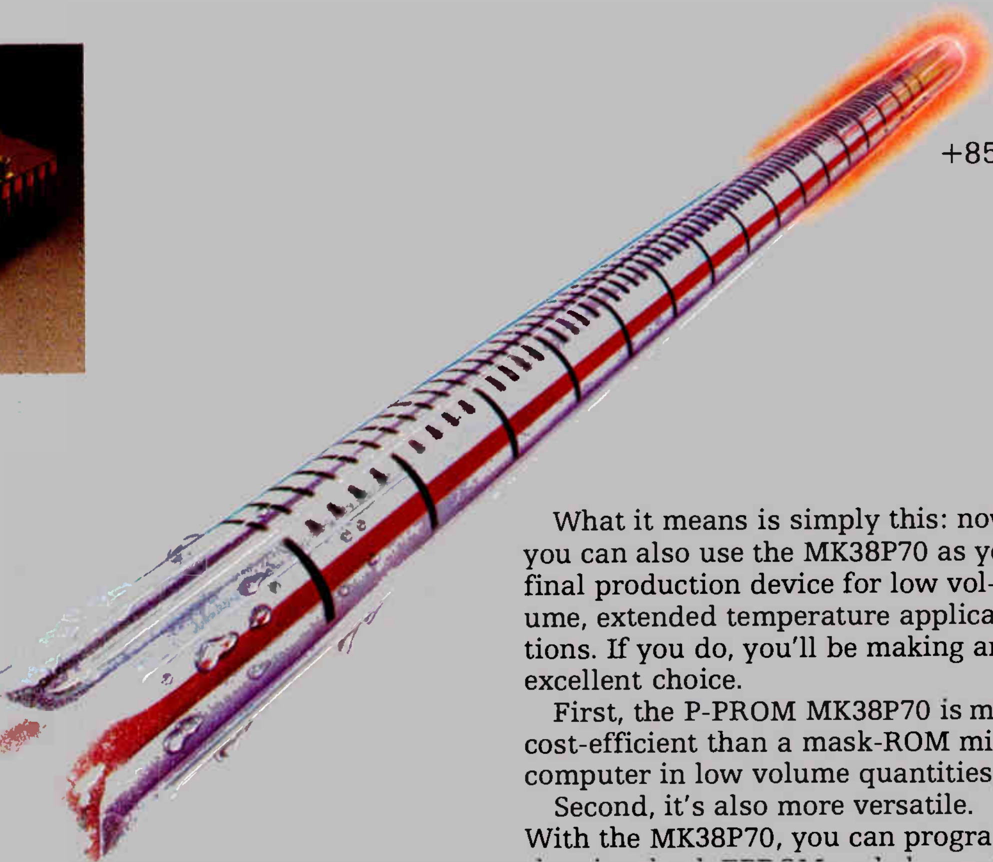
The item was about an advertisement by the University of the District of Columbia that appeared in the Washington Post. In it, UDC's College of Physical Science Engineering and Technology, soliciting enrollments, offered not only high-quality academic programs but "almost guaranteed employment and virtually a license to make money." We have no way of passing judgment on the quality of the curriculum at UDC, but we do note, as did Feerst, that a recent article in Harper's cited the "university" as actually a school for remedial reading, where 90% of its freshmen read below the ninth grade level.

That aside, we do agree that equating an engineering degree with a license to make money is not only demeaning to the profession but will attract to engineering schools students with the wrong motivation, who will inevitably be disappointed. Most of us are looking for an opportunity to do satisfying work for fair remuneration, not licenses to make money.

The first user-programmable, 8-bit micro that runs hot and cold: MK38P70.

UNITED TECHNOLOGIES MOSTEK





What it means is simply this: now you can also use the MK38P70 as your final production device for low volume, extended temperature applications. If you do, you'll be making an excellent choice.

First, the P-PROM MK38P70 is more cost-efficient than a mask-ROM microcomputer in low volume quantities.

Second, it's also more versatile. With the MK38P70, you can program the piggyback EPROM and change it if necessary (as often as you like) on any standard EPROM programmer. Once completed, you're ready for production because the MK38P70 will meet final system specifications.

And, if the application subsequently becomes higher volume, you can still use the MK38P70 to emulate a total of 8 mask-ROM equivalents.

A –40°C to +85°C operating range. Add that to unparalleled emulation capability and it's easy to understand why the MK38P70 continues to be the hottest, user-programmable microcomputer you can get. Call your nearest Mostek distributor to find out more. Or contact Mostek, 1215 West Crosby Road, Carrollton, Texas 75006 (214) 323-1801. In Europe, contact Mostek International at (32)2.762.18.80. In the Far East, Mostek Japan KK (03)-404-7261.

Circle 27 on reader service card

The 10-Bit DAC Race Is Over!

PMI's High-Speed DAC-10 Just Became The Leader in Linear Wonderland

© PMI 1981

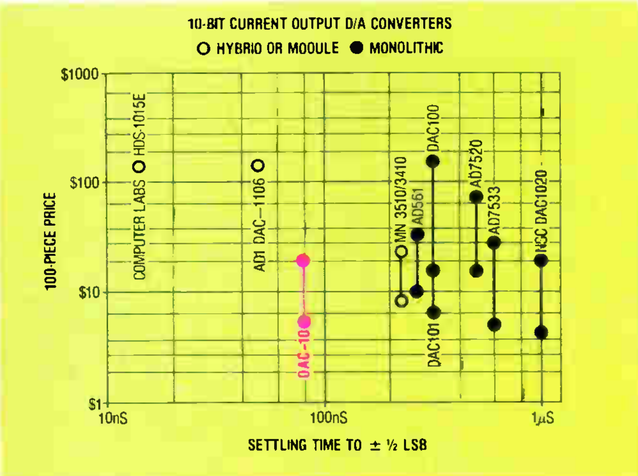
"Oh dear! Oh dear! I shall be too late!," the White Rabbit said as Alice saw him take a watch out of a waistcoat pocket, look at it and then hurry on. In Alice's Wonderland, the White Rabbit was always rushing off in new directions but arriving there too late.

In Linear Wonderland, a lot of circuit designers are like the White Rabbit. They constantly race the clock to complete development of new linear circuits, only to find that PMI's gotten there first.

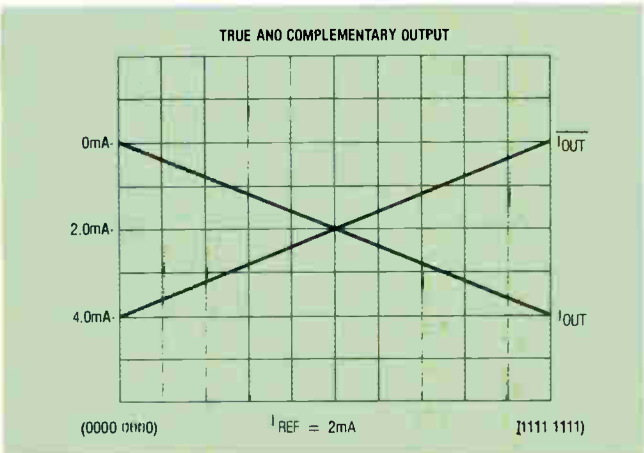
Our new DAC-10 is a case in point. Every linear house has been racing to come up with an affordable high-speed 10-bit D/A converter. Now PMI has one. With a speed of 85ns and a pinout compatible with our industry standard DAC-08, the low-priced DAC-10 will make further development of 10-bit current output DACs unnecessary. PMI is understandably proud of its accomplishment.

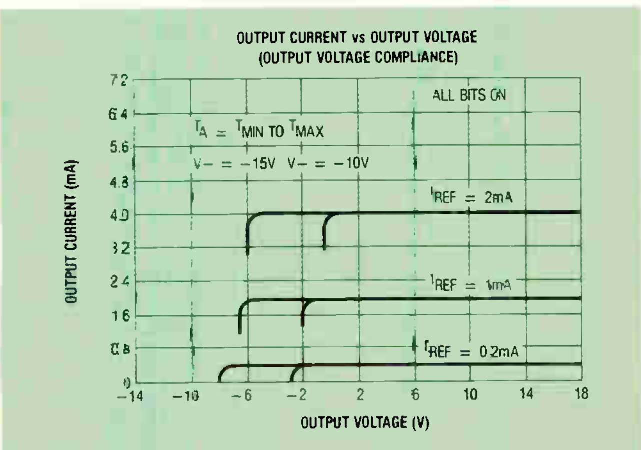
The DAC-10 is not just a modified DAC-08. It's a brand new product, redesigned to achieve the *speed* of the DAC-08 but with 10-bit resolution and ½ LSB full-scale accuracy. Trimming is achieved with zener zapping to avoid the long-term instability problems associated with laser trimming.

All that at attractive domestic prices starting at $5.50 for commercial grades and $14.50 for military grades. A comparison of the speed/resolution/price tradeoffs in existing 10-bit DACs will show you exactly why the PMI DAC-10 is destined to become the 10-bit industry standard, just like the DAC-08 became the 8-bit standard.



The White Rabbit looked at his watch again, then dipped it in his cup of tea to see if he liked what it said any better. If you're still not sure the DAC-10 looks good to you, PMI can give you some other ways of looking at its performance.





While the DAC-10 may have come along too soon for our competitors, we think equipment designers will say it's just in time. Think of the possible applications:

- 10-bit 2μsec A-to-D converter
- Tracking A-to-D converter
- CRT graphic display driver
- High-speed waveform generator
- Programmable current source
- Programmable attenuation/gain
- Voltage output with simple resistor termination

Whatever your application, send for our "Quick As A Rabbit" DAC-10 sample or give us a call.

And tell your engineering friends who design linear circuits they can stop work on their 10-bit DACs and get started on something else. When they get to where they're going, PMI will already be there . . . waiting for them to catch up.

If someone beat you to the coupon, write to us. Or circle #200 for literature.

PMI®
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Santa Clara, California 95050
(408) 246-9222 TWX: 910-338-0528 Cable: MONO

In Europe contact:
Precision Monolithics, Incorporated
c/o BOURNS AG
ZUGERSTRASSE 74, 6340 Baar, Switzerland
Phone: 042/33 33 33 Telex 78722

Check the box for your "Quick As A Rabbit" DAC-10 sample.

☐ DAC-10 ☐ Literature

Mail To: **Precision Monolithics, Inc.**, 1525 Comstock Avenue, Santa Clara, CA 95050
or **Precision Monolithics, Inc.**, c/o BOURNS AG Zugerstrasse 74, 6340 Baar, Switzerland

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10ES217

BIOMATION K101-D

BREAKTHROUGH

The most powerful general purpose logic analyzer you can buy for the years ahead.

It's here. Biomation K101-D. The first logic analyzer to combine high-speed 50 MHz data and 100 MHz time domain capabilities with advanced 48-channel recording. With enough powerful extras to demolish your toughest hardware/software integration problems—even on the most complex multiplexed microprocessor.

Fast, accurate software debugging.
With its 50 MHz clock rate, 48-channel recording and 16 triggering levels, the K101-D isolates software bugs faster and more precisely than ever before. Sophisticated disassembly firmware generates precise mnemonics that cut analyzing time. And 12 external clocks (AND or OR) let you demultiplex 16-bit microprocessors, 16- and 32-bit minicomputers and bit-slice processors.

100 MHz high-speed hardware analysis.
The K101-D's advanced high-performance hybrid probes let you capture glitches as narrow as 5 ns. And, with 48-channel recording, 515-word memory and 16-level triggering, you'll trap the data you need. The convenient display formatting and expansion simplify analysis.

Call now for a free demo.
See for yourself why the K101-D is a breakthrough in logic analyzers for the years ahead. For a demonstration or a copy of our detailed product brochure, write Gould Inc., Biomation Operation, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For fastest response, call 408-988-6800.

For powerful software debugging, K101-D data domain capabilities include disassembly, 50 MHz clocking, 48-channel recording, 12 external clocks, 515-word memory, demultiplexing, 16-level trace control for triggering, 6 display code formats, and reference memory.

For powerful hardware debugging, K101-D time domain capabilities include 100 MHz clocking, 48-channel recording, 515-word memory, 5-ns glitch capture, 16-level triggering, channel labeling, new high-performance probe design, as well as horizontal and vertical display expansion for easy reading.

GOULD
An Electrical/Electronics Company

Circle 31 on reader service card

No other oscilloscope offers this much in one package.

Large 16K Memory

See things you've never seen before with a time resolution of up to 16,000:1 and a dynamic range of up to 32,000:1. Zoom in on the smallest signal detail with expansion up to x256 on both axes. By using subsections of memory, you can display up to 32 stored waveforms simultaneously.

4-Channel Operation

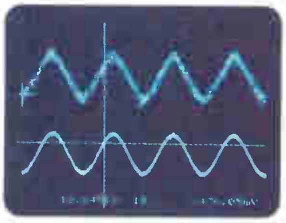
Capture, store and display four signals simultaneously using two plug-ins operating on the same, or totally independent, timebase and trigger. Compare live and stored waveforms in real time. Even compare interactive variables such as voltage/current or stress/strain using X-Y display of either live or stored signals.

Pre- and Post-Trigger Delay

Look into the past or future with a pre-trigger delay from 500 nanoseconds to 37 days or a post-trigger delay up to 106 years. Avoid accidental triggering by checking the threshold and sensitivity using the trigger-view mode.

Signal Averaging

Extract repetitive signals from noise using sweep averaging. Even smooth those slow, noisy, one-shot signals by using the unique point-averaging mode.



Alphanumeric Display

Get absolute or relative measurements from any portion of the waveform using the cursor-interactive time and voltage readout. The numerics include a channel identifier to eliminate errors even on multiple trace displays.

Data Manipulation

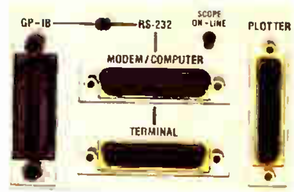
As with all Nicolet scopes, manipulate stored data using the pushbutton functions of add, subtract or invert. With the 4094, continue to expand this capability with disk-extended functions of multiply, integrate, smooth, RMS and much more.

Permanent Data Storage

Store waveforms at the touch of a button on the optional floppy disk or capture and store automatically using the autocycle feature. Get report ready hardcopy records using the standard X-Y or Y-T recorder outputs, or obtain fully annotated plots automatically with the optional digital plotter.

IEEE-488 and RS-232 I/O

Integrate the 4094 into your digital measurement system with the fully bi-directional GP-IB and RS-232 digital I/O option.



One of a Family

Nicolet is the world's leading manufacturer of high resolution digital oscilloscopes. In addition to the 4094, Nicolet offers the 2090 range of 2-channel digital oscilloscopes with many advanced features including high-resolution, disk storage and digital I/O.

Find out how Nicolet can bring digital precision to your analog measurements. For more information, call 608/271-3333. Or write: Nicolet Instrument Corporation, Oscilloscope Division, 5225 Verona Road, Madison, WI 53711.

In Canada: call 416/625-8302.

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OSCILLOSCOPE DIVISION

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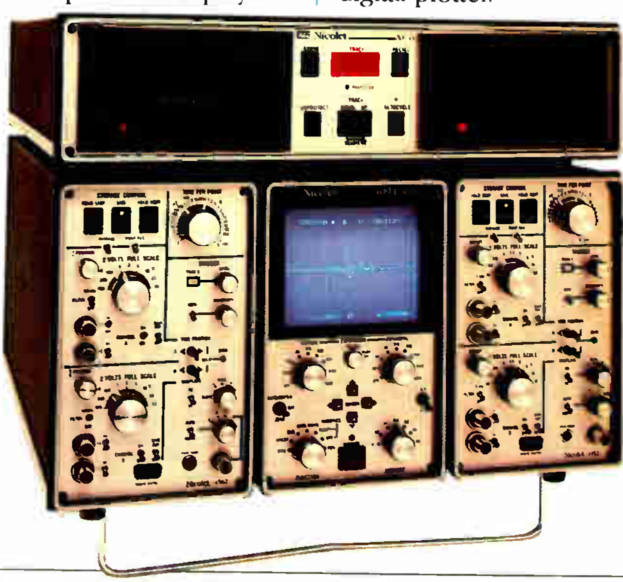


The Nicolet 4094.

DEC module turns VT100 into desktop computer

With an installed base of more than 250,000 VT100 display consoles, the Digital Equipment Corp., Maynard, Mass., is taking a step designed both to protect this base and to enter the personal and small-business computer market. DEC is announcing the VT18X, a printed-circuit module that plugs directly into the VT100, **converting it into a complete, CP/M-compatible microcomputer system.** For $2,400, a VT100 owner gets the computer board consisting of a 4-MHz Z80A microprocessor with 64-K bytes of MOS random-access memory and software-controlled RS-232-C and printer ports. Two 5¼-in. floppy-disk drives also are included, and DEC will sell CP/M licenses for $250. Thus, with the VT100 selling discounted for about $1,450, a VT18X package would cost only about $3,950—competitive with recent entries from IBM and Xerox. Software will be available through Lifeboat Associates, Peachtree Software, and Digital Research.

Motorola, Mostek Signetics agree on 16-bit bus

Motorola Inc., Mostek Corp., and Signetics Corp. have jointly created specifications for a series of **Eurocard bus products that use the 68000 16-bit microprocessor.** To be marketed both in the U. S. and Europe as the VME bus, it will come in two standard sizes: single Eurocards (160 by 100 millimeters) for 16-bit systems, and double cards (160 by 233.4 mm) for 32-bit systems. The single card will have one pin-and-socket connector capable of supporting 16-bit data widths and addressing up to 16 megabytes. In addition to the primary 96-pin connector, the double-size card will have a second 96-pin expansion connector, allowing it to accommodate multiprocessor systems and future 32-bit processors. The new bus, which will be asynchronous, will have nonmultiplexed address and data fields—allowing it to speed up individual bus cycles to handle up to 5 million 32-bit transfers per second.

Silicon foundries pose problems for Japanese

The accelerating move toward silicon foundries in the U. S. has not escaped the attention of Japanese semiconductor officials. One worldwide study on their impact on standard parts already has been completed by management consultants McKinsey & Co. While McKinsey officials stress that any effects hinge on how fast, and indeed whether, custom very large-scale integrated circuits would displace clusters of simpler components, U. S. foundry success will pose strategic problems for Japanese-semiconductor houses. The basic geographic advantage of having foundries near big U. S. customers, **with better service implied along with fast turnaround and good prices,** would be tough for Japanese firms to beat.

Zilog, Seeq to mate microprocessors, on-chip EE-PROMs

An important step toward the day of the self-configuring microprocessor has been taken by Zilog Inc. and Seeq Technology Inc. The two California firms have agreed to exchange expertise as they jointly develop a microprocessor family with on-chip 5-V-only electrically erasable programmable read-only memories. **The devices will be designed by Zilog,** which has headquarters in Campbell. Seeq, a startup by former Intel engineers in San Jose, will share the processing know-how in developing its EE-PROMs, while Zilog will reveal some of the internal hooks of its microprocessor line to allow the two types of devices to be mated. The first products jointly developed will be EE-PROM versions of the Z8 and Z80, but the door is left open for similar efforts with Zilog's 16-bit and upcoming 32-bit lines.

Electronics newsletter

Stata backs maker of low-cost CAT scanners

A Schaumburg, Ill., start-up firm listing Ray Stata as its primary financial backer—he is chairman and president of Analog Devices Inc.—is planning to sell low-cost computerized axial-tomography (CAT) scanners with installation of its first unit early next year. Priced at about $475,000, the full-body X-ray scanner from Interad Systems Inc. will be **30% to 50% cheaper than comparable systems built by major suppliers such as General Electric and Siemens,** says Interad president G. H. Williams. The Interad system will employ an array processor supplied by Computer Design & Applications Inc., Newton, Mass., and will feature an operator's console, based on an LSI-11/2 processor, with 8-in. Winchester disk drives and other peripherals built in. Though a number of companies have failed in the CAT scanner business in recent years, Interad hopes to succeed by marketing its system initially to smaller hospitals with fewer than 250 beds that cannot afford the more expensive units.

Grumman to make broadcast gear

With the National Broadcasting Co. signed up as its first customer, Grumman Aerospace Corp. has gone into a new business: the design and manufacture of television broadcast equipment. The deal with NBC, for about $1 million, is **for design, development, and production of a TV–timing-reference system.** It will be done at Grumman's facility at Great River, N. Y., and will be used at the NBC studios in Burbank, Calif.

Lapierre heads Rockwell division

Bolstering its commercial semiconductor efforts, Rockwell Corp. has named Alfred G. Lapierre president of its Electronic Devices division. Since 1978, **Lapierre has headed the MOS LSI Business of National Semiconductor Corp. Lapierre succeeds Howard Wolrath, who has been appointed a vice president under Kent M. Black,** president of Rockwell's Commercial Electronics Operations, of which Lapierre's division is a part. Previously, Steve Ou was named director of product development and Howard Cotterman became general manager of the division.

Addenda

RCA Corp.'s Solid State division in Somerville, N. J., has signed an alternate-sourcing agreement with Motorola Inc.'s Microprocessor Group in Austin, Texas, for the 146805 complementary-MOS microcomputer family. **RCA will make the 8-bit part in all its versions as well as supply support chips** and will continue to make its own 1800 family as well. . . . Look for General Electric Co. to introduce Gescan 2, a hardware-based text search and retrieval system **capable of multiple, parallel searches of a large data bank at the rate of 2 million characters per second.** . . . Zenith Data Systems in Glenview, Ill., **has added the Z-90 to its line of small business machines.** Like the firm's two-year-old Z-89, the Z-90 is based on an 8-bit Zilog Z80 microprocessor, but has double-density 5.25-inch diskette capability and expands main memory to 64-K-bytes, compared with the 48-K-byte Z-89, which handles single-density 5.25-in. diskettes. . . . Tandy Corp. says **it is negotiating for the purchase of Memorex Corp.'s Consumer Products division.** . . . Asiagraphics, a start-up company in Mt. Sinai, N. Y., is preparing a software package that allows Chinese and Japanese characters to be displayed on standard bit-mapped computer terminals. A unique feature **allows characters not in its 5,000-unit set to be added in real time** by defining which bits in a 16-by-16 grid to turn on.

Meeting Japan's Challenge

Third in a Series

HOW THE SIMPLEST BUSINESS PRINCIPLE OF ALL TURNS COMPETITORS INTO CUSTOMERS.

If you make a better quality product than your competition, customers will buy it.

We at Motorola have seen this simple principle make significant differences in the international electronics industry we are part of.

For example, in recent years quality improvements by many Japanese companies have resulted in major inroads for their products into world markets, especially in consumer electronics.

But the same principle of quality has turned some of those Japanese competitors into important customers of American firms such as Motorola.

A case in point concerns communications equipment Motorola designed and built for NASA. Our equipment has been used on every manned and most unmanned space shots without a single mission-endangering failure. Not one. So impressed was the Japanese Space Agency with the quality of our space communications technology and our reliable performance they have specified Motorola equipment for use on many of their space missions.

Closer to earth, a Japanese national named Junko Tabei, the first woman ever to climb Mt. Everest, used an FM portable two-way radio made by Motorola here in America to help guide her to the top. It withstood nights of 20° below zero and days of blinding blizzards. Small surprise that with plenty of Japanese radios to choose from, Ms. Tabei also specified Motorola for her next climb, this time to the roof of Tibet.

And the examples go on. Even though Motorola has bowed out of the consumer electronics market, Japanese companies that are today's giants in that industry buy millions of quality components from our Motorola Semiconductor Products Sector.

All this isn't happenstance. It is the systematic result of Motorola programs, pioneered and developed over the past decade, to give all Motorola employees a greater sense of involvement in, and responsibility for, the quality of the products they design and manufacture.

So, when we receive quality supplier awards from companies such as General Motors, Control Data and even Hitachi, we know why.

And we're proud of that kind of response. It supports our belief that quality is not only the oldest and simplest principle of business. It also is the most important.

MOTOROLA *A World Leader In Electronics*

Quality and productivity through employee participation in management.

Circle 37 on reader service card

Type MG Precision High Voltage Resistors from CADDOCK deliver 6 big advantages:

1. For maximum design flexibility, there are 19 standard models with 10 voltage ratings in the Type MG 'family'.

The Type MG family of high voltage resistors includes a selection of voltage ratings from 600 volts to 30,000 volts in various resistor lengths to provide maximum flexibility in the design of high voltage assemblies.

In addition to this wide range of voltage ratings, the Type MG family provides a selection of resistor diameters at many of the standard voltage ratings, as illustrated by the three models of 4,000 volt, 1-inch long resistors shown here.

Important performance specifications for all Type MG resistors include:

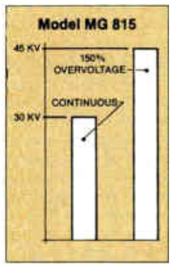
- Full power rating to + 125°C.
- + 225°C maximum operating temperature.
- Resistance values that cover the range from 200 ohms to 2000 Megohms.

2. The standard TC of 80 PPM/°C and resistance tolerances from 1.0% to 0.1% combine to improve circuit accuracy.

Through the full range of resistance values from 200 ohms to 2000 Megohms, the Type MG resistors maintain a temperature coefficient of 80 PPM/°C over the range from − 15°C to + 105°C, referenced to + 25°.

The combination of precision and low TC achieves a significant improvement over other high voltage resistor technologies, particularly in the higher resistance values.

3. Overvoltage rating of 150% is standard for all models.

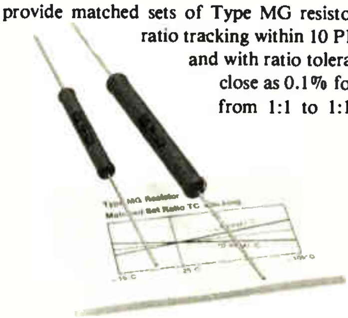


Every model of the Type MG resistors has a *standard* overvoltage/overload rating of 1.5 times the maximum working voltage where this level does not exceed 5 times the rated power. As an example, in the Model MG 815 this capability provides for short-term overloads as high as 45,000 volts.

And for even tougher applications, special factory conditioning can boost the maximum *continuous* operating voltage of many models to 160% above the standard specifications.

4. Matched resistor sets with 0.1% ratio tolerances and TC tracking as close as 10 PPM/°C from -15°C to +105°C.

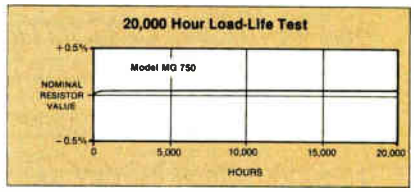
The temperature coefficient of Caddock Micronox® resistance films can be controlled to provide matched sets of Type MG resistors with ratio tracking within 10 PPM/°C and with ratio tolerances as close as 0.1% for ratios from 1:1 to 1:100,000.



For high voltage divider applications, 2% ratio tolerance is standard.

5. Extended-life stability that is typically better than 0.02% per 1000 hours.

20,000 hour *continuous* load-life tests have proven the exceptional stability of Caddock Micronox® resistance films. This graph illustrating the 20,000 hour test results of the 10,000 volt rated Model MG 750 shows extended-life stability well within 0.02% per 1000 hours.



A complete data summary of these test results is available on request.

6. Exclusive Non-Inductive Performance.

Caddock's Exclusive Non-Inductive Design is the answer wherever there are special requirements for excellent high-voltage pulse fidelity and wide bandwidths.

To keep the inductance to an absolute minimum, the special serpentine pattern provides for neighboring lines to carry the current in opposite directions to achieve maximum cancellation of flux fields over the entire length of the resistor.

Caddock's advanced film resistor technologies are the source of these exceptional performance advantages. Produced with a special dedication to quality and unit-to-unit consistancy, these high performance film resistors have achieved an unsurpassed 20-year record of 'in-circuit' reliability.

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Market-share scramble sires faster versions of 64-K dynamic RAMs

by J. Robert Lineback, Dallas Bureau

Memory makers feel that fastest chips will win out and are upgrading their chips for swifter access

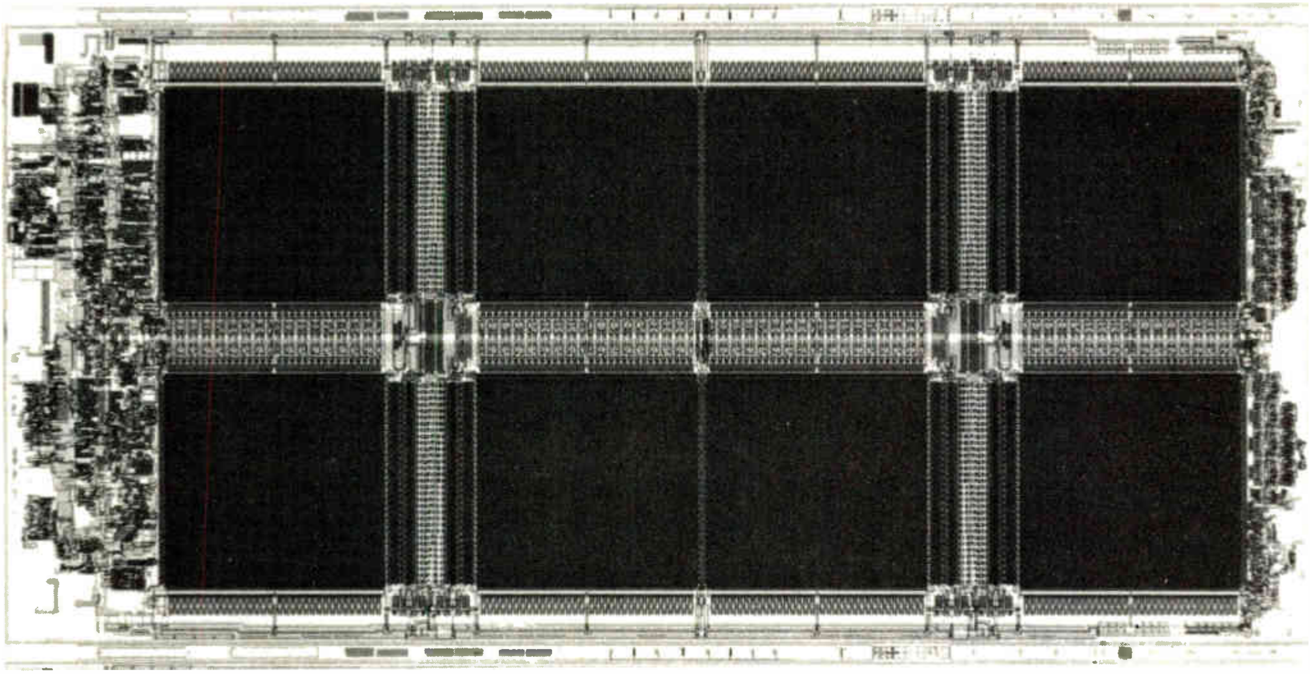
The race for market shares in the 64-K dynamic random-access memory business presumably will go to the manufacturers with the swiftest parts. For although memories with access times of 200 nanoseconds account for most the 64-K RAM business at the moment, increasing numbers of buyers want 150-ns parts.

So to hold their own in the fast-accelerating market, three of the leading U. S. contenders—Motorola Inc., Mostek Corp., and Intel Corp.—will soon hit the market with faster versions of their 64-K chips. As for Texas Instruments Inc., like Motorola a volume producer of the parts, more than half the 64-K RAMs leaving its lines in Lubbock, Texas, and Miho, Japan, meet the 150-ns access standards. Thus TI seemingly can compete with what it has now; the Dallas, Texas, firm will not say whether it has an upgrade in mind.

Higher charges. After nine months of fine tuning, Motorola will begin volume production of its new 64-K chip in November. To boost performance, the Austin, Texas, MOS memory operation improved circuit design and devised a new die layout. The process remains the same as that used for the current 64-K RAM: the company's n-channel silicon-gate H-MOS (high-performance) technology. However, Motorola will move up to 5-inch wafers for the new part, which will be produced initially at Mesa, Ariz.; later the part may be produced in Europe and in Japan.

Chief among the cell design changes is an enlarged storage capacitor. It doubles the amount of stored change to 280 femtocoulombs. As a result, the chip is less susceptible to soft errors, and in fact none occurred during tests totaling more than 2 million device hours.

The new die layout splits the array, adding an extra set of decoders to cut the polysilicon word line in half. "By halving the word line, we



Better halves. To upgrade its 64-K RAM, Motorola added a second line of row decoders (the two vertical bands). They split the cell array into smaller blocks and halve the word line, speeding access to the storage cells. Over half the chips with the new design have 150-ns ratings.

significantly speed up the part," explains David C. Ford, Motorola's Strategic marketing manager of MOS memories. These changes, he insists, are transparent to users of the current 64-K chip.

Because yields have been acceptable, Motorola decided not to put redundant memory cells on its die. "We continue to evaluate it [redundancy], but at the present time we feel pretty comfortable with what we are seeing." Ford says.

Speedsters. He also finds no discomfort in the speeds of the new chips. Over half of the new 64-K RAMs achieve 150-ns row-address-strobe times, he reports. But the RAS speeds must be matched with fast column-address-strobe times before dynamic RAMs will work as high-speed parts in a number of memory applications, Ford cautions.

So Motorola improved the CAS time for its 150-ns part, giving it an address strobe ratio of 2:1. "We will be offering a 75-ns column-access time, which is better than most expectations even for 1982," he says. In addition to the 150-ns parts, there will be 120- and 200-ns ratings in the new 64-K RAM line.

Because Motorola wrought its improvements strictly through circuit-design changes, Ford figures another boost in performance will come from bettered process technology, such as refractory metal silicides. "We are confident that within a year we will have a low sheet ρ polysilicon process that is ready to run in volume," Ford reports. "This will of course result in another increase in speeds."

Motorola, in fact, plans to use this new process for the 256-K RAM it is developing. Meanwhile, the company plans to gradually phase out its first-generation 64-K device, which is now running on a 4-in. wafer line in Mesa.

Fast followup. Mostek plans mass production of its new 64-K RAM in the first quarter of 1982—less than half a year after it began volume deliveries of its current part. Among the changes in the new MS4564 are redundant memory cells and an increase in address speed distributions. But Mostek will not start making use of the redundant cells, which create a fault-tolerance device, until later in the year, says Tim Propeck, memory product marketing manager of the Carrollton, Texas, firm. The 4564 will be available in 250-, 200-, and 150-ns versions.

Despite the new version waiting in the wings, Mostek is ramping up production of its current 64-K device, which is being manufactured in both Carrollton and Colorado Springs, Colo. "We are shipping 1,000 per week now, and it looks like our fourth-quarter volume is going to be in the 250,000 to 300,000 range," Propeck estimates.

Meanwhile, Intel is putting the finishing touches on its new 64-K chip, which it plans to begin shipping in late 1981.

The Santa Clara, Calif., firm pulled its 2164 64-K RAM off the market earlier this year after spotting problems in the zero-level-sensing mechanism. With the new device, Intel will be offering 150-ns RAS speeds for the first time.

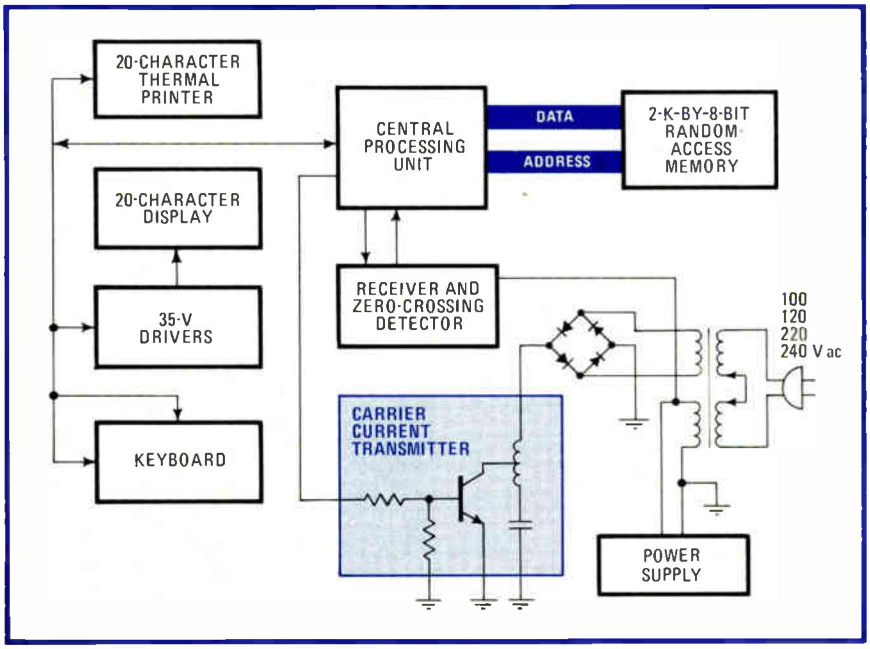
Redundancy is being retained on the second version, but the die size has been reduced from 161 by 317 mils to 137 by 269 mils. Intel tightened the chip's geometry and changed the process to reduce the metalization pitch from 9 to 7.5 micrometers. It kept a polysilicon fuse technique to implement redundancy or the RAM.

Local networks

Data bursts, repeated up to 10 times, conquer spikes on ac supply lines

Alternating-current power lines are a poor medium for local data communications because of the random noise spikes that blast through them—or so says conventional wisdom. However, a new firm in Santa Barbara, Calif., claims otherwise and is readying a small terminal it says has whipped the noise problem in tests.

An ambitious undertaking, the 006 terminal by Evince costs only



Through the spikes. Evince's under-$300 terminals interconnect through a building's regular ac power lines. Data gets through because the processor repeats it up to 10 times.

$250 to $300, yet uses the advanced digital signal-processing technique of time-domain transfer. In penetrating the spikes using this technique instead of the often-used Fourier transform, it will transmit each message in 10-bit parallel data bursts repeated up to 10 times.

The data bursts are structured to remain on line as long as possible. This way, even an overwhelming noise spike can destroy only a part of the signal, says William J. Parrish, vice president for research and development. He is reluctant to discuss specifics of the data-transmission scheme for proprietary reasons.

Typical throughput for the terminal will be 960 bits per second, with higher rates possible. A 512-character message, for example, would be sent in about 40 seconds.

Because transformers are best penetrated by low frequencies, a 10-kilohertz carrier frequency is contemplated. Parrish says the firm does not expect to encounter any problems from power utilities—the owners of the transmission lines.

The most difficult design task was to anticipate noise conditions on 60-hertz power lines, "which can vary by an order of a magnitude in impedance and levels," says Parrish. "Our terminal must be able to penetrate this whole spectrum." Switching industrial lights and turning on motors cause the high-amplitude, short-duration spikes.

The terminal is planned to have an alphanumeric keyboard, a 20-character vacuum fluorescent display, a 20-character-per-line thermal printer, and a central processing unit based on an 8-bit microprocessor. "It is a bottom-up approach for people who don't need expensive Ethernets or Z-nets," says Evince president Jacob Y. Wong.

The 006 will have a range extending up to 200 yards and will handle low-level networking jobs in offices and factories, including teletypewriter communications and the transfer of industrial-process control data, he points out. It will have wall-plug portability.

Started in August 1980, Evince employs some 50 people and does its volume manufacturing out of Hong Kong. Wong says the company has already shipped $500,000 worth of a simple interoffice communications setup whose central display sells for $140, with calculator-sized remote-input units priced at $45. The unit, which like the upcoming 006 relies on ac lines, is programmed with 25 commonly used messages like "hold all calls" or "in a meeting," which are shown by light-emitting diodes.

Development of the 006 is 80% completed, and all of the front-end engineering is finished, says Parrish. Now in the planning stages is an interface gateway computer similar to the 006 that can link computers, either directly or by telephone line. "With our terminal, ac lines will soon be recognized as a viable [data-transmission] medium," Wong predicts. **-Larry Waller**

Business systems

Iowa stores try electronic payment

Iowa's reputation as a pacesetter in electronic funds transfer got another boost this month, thanks to a new point-of-sale system installed for testing in a Des Moines supermarket. The system is touted by its supplier—NCR Corp., Dayton, Ohio—as the first to let shoppers pay for their groceries electronically by using a plastic card instead of money at the checkout counter.

When the checkout clerks ask for payment, a consumer choosing to pay electronically simply pushes a bank-issued debit card through a magnetic strip reader and punches a personal identification number into a small keypad. Through an in-store computer, the checkout terminal is tied into Iowa's statewide EFT banking network. Within 15 seconds, says NCR, the transfer of funds from the customer's checking account to the store's account is complete, and the register prints out a paper receipt.

If the Iowa test is successful, it could touch off a wave of new activity in the EFT field, which in recent years has seen rapid growth in cash-dispensing automated teller machines [*Electronics*, March 27, 1980, p. 96]."I expect we'll see a brief period while people look at what happens in this particular system; and then, I wouldn't be surprised to see a flood of similar systems," says William R. Moroney, head of the Electronic Funds Transfer Association in Washington, D. C.

Not surprisingly, NCR thinks so too. A second Dahl's Food Mart will be equipped next month as part of the Iowa test, and NCR says it has several similar projects under development elsewhere.

The company hopes to begin marketing the card reader and keypad as part of its regular product line during 1982. By 1984, predicts Daniel J. McCarthy, NCR retail systems vice president, such systems could become commonplace.

Not all, however, agree. Consumers and retailers are not yet ready to accept direct EFT payment systems, says Johnny Humphreys, vice president and general manager at National Semiconductor Corp.'s Systems division in Sunnyvale, Calif.

POS scanning equipment "took six years to really catch on from the time that some people thought it might," he points out. National is designing its present product line with an eye toward accommodating EFT eventually, but has no current plans to test the technology, Humphreys says.

In the cards. In the Iowa test, nine NCR 255 POS terminals at a Dahl's Food Mart in Des Moines are tied via phone lines into the Iowa Transfer Systems (ITS)—a shared network that links 110 Iowa banks. The net employs 231 automated teller machines that serve an established cardbase of about 500,000 users, says ITS Inc. president Dale A. Dooley. Brought on line in February, 1977, the system was the first statewide EFT consumer banking network and is considered state-of-the-art today.

When a shopper decides to use the new pilot system to pay electronically, transaction information is transmitted at 4,800 bits a second to a central switch in Des Moines, which logs and verifies the data before sending it on to one of nine data-processing centers that service participating banks. Each transaction message contains between 40 and 60 8-bit characters, including the customer's personal identification number, account information taken from the magnetic strip, terminal information, and transaction codes, Dooley says. When the funds transfer is complete, a message is relayed through the switch back to the terminal. The data centers employ IBM, Burroughs, and NCR mainframes; the switch uses redundant NCR 8455 mainframes. **-Wesley R. Iversen**

Components

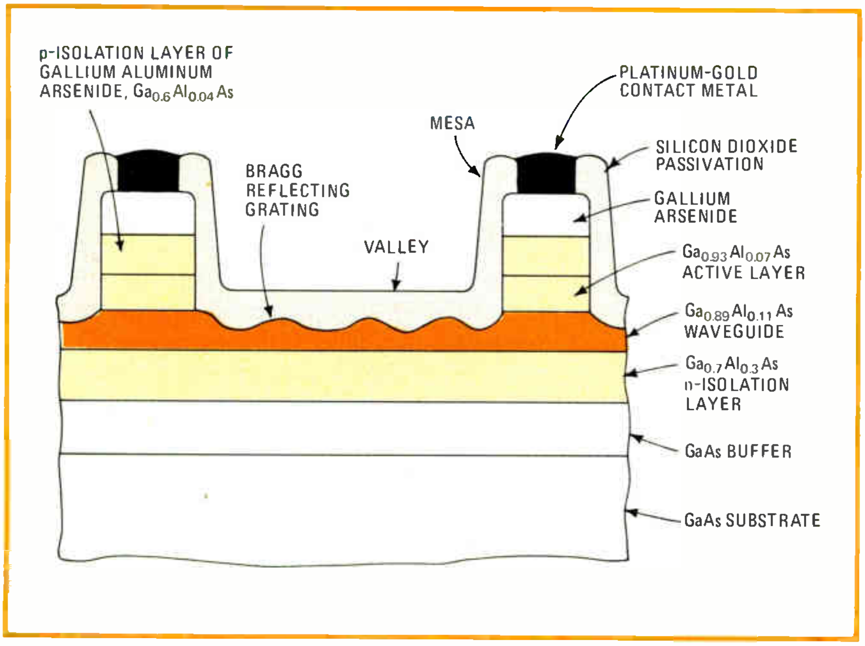
Laser phased arrays shine from a chip

Laser phased arrays have reached the planning stage at several research organizations, but Aerospace Corp. may be the first to get one up and working. The lasers are of the gallium-aluminum-arsenide semiconductor type.

However, it is hard to grow high-quality GaAlAs layers and integrate on one chip all the array's components. These include not only the lasers and a distributed Bragg reflector for stabilizing their output, but also other Bragg devices for expanding the beam vertically and an output coupler for accomplishing the same expansion horizontally among other components.

All together. So far, Aerospace has put lasers and a distributed Bragg reflector on one chip, as shown in the figure, and demonstrated the other elements separately. The chip marries distributed semiconductor lasers to optical feedback based on Bragg scattering. The company is dedicated to putting all components together over the next three to five years, says Gary A. Evans of Aerospace's Electronics Research Laboratory in El Segundo, Calif.

Aerospace plans to put 10 to 20 lasers on a chip 0.5 centimeter square. Output power, with the individual laser outputs adding to each other, would be between 0.1 and 1 watt, far more than the milliwatt output of individual semiconductor lasers.



Reflections. A distributed laser array being developed by Aerospace uses gallium arsenide emitters with varying proportions of aluminum substituted for gallium, as shown. Light reflected from a Bragg grating serves to stabilize output wavelengths.

As for potential users, communications engineers at the Air Force Space Systems division next door to Aerospace say they will be interested in the device—when the arrays are actually built. Such arrays could well substitute, industry sources say, for the large neodymium:yttrium-argon-garnet lasers the Air Force is contemplating for its laser-communication system of the late 1980s. The result may be a more flexible and reliable system.

Optical gratings. Aerospace has integrated its GaAlAs lasers with Bragg-effect gratings having a 0.35-micrometer period. The result is called a distributed laser because of the extended valleys in which Bragg scattering—the optical feedback mechanism—occurs. Laser action occurs in the active regions, with charge injected from n- and p-type regions ("isolation" in the figure).

Altogether six layers—the buffer through the cap—are grown with liquid-phase epitaxy, and the mesas are formed by removing the top three layers. The exposed waveguide layer is then patterned by holographic photolithography to form the corrugated grating structure. Oxide passivation follows and after that metal contacts are deposited and patterned to complete the device.

Light output from each laser travels along the waveguide layer and is scattered by the diffraction grating. Scattered light of a particular wavelength, determined by the grating geometry and refractive index, will constructively interfere with the incident beam, according to Bragg's law, while slightly different wavelengths will interfere destructively and cancel each other out.

As a result, only one wavelength contributes to the output beam. The device in the figure would be cleaved in the middle of the valley.

Stable beam. But the big advantage of combining a Bragg reflector with lasers is the temperature stability of the output beam's wavelength. In a standard semiconductor laser, the change in bandgap energy with temperature results in an output-wavelength shift of approximately 3 angstroms per °C. In a distributed

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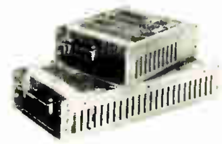

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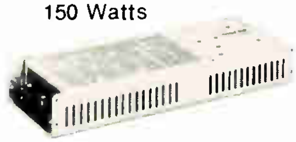

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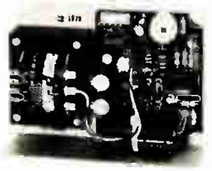

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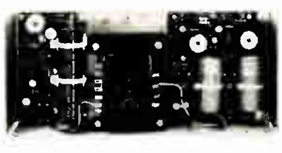

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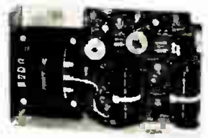

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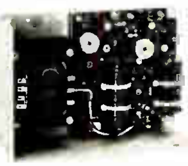

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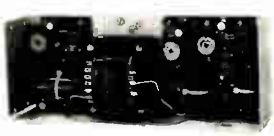

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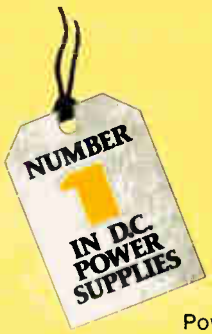

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Bragg-reflector laser, that bandgap shift is present but not important, because the Bragg reflections still occur at the given wavelength. The only temperature dependence of Bragg scattering results from a much weaker temperature dependence of the waveguide's index of refraction. -Larry Waller and Roderic Beresford

Production

Robot loads bases, leadframes in boats

In one hour, six diligent people can load some 6,000 carriers—or seal boats, as integrated-circuit makers call them—with ceramic bases and lead frames that then travel on to an oven to become ceramic dual in-line packages.

Such jobs are threatened by a $39,000 robot in the final stages of development at Conceptek Corp. The CT-10,000 has a top throughput of 10,000 parts an hour, as its catalog number suggests. But Greg De Luca, president of the eight-year-old Tucson, Ariz., firm says the robot usually will handle 6,500 parts an hour.

The robot needs a little help from a human friend to load, start, and stop it; otherwise it is on its own. At the outset, 30 trays are delivered to it, each holding 200 bases, for a total of 6,000 parts. The robot arm sucks up 200 bases at a time and deposits them on an air-flotation loading table. From there, the bases slide down a chute in lots of 10 and are placed one by one in the seal boats, each of which holds 20 bases. Fiber-optic sensors determine the position of the boat.

Glassed in. The boats then travel on a conveyor belt until another fiber-optic sensor determines the bases in them are in position for placement of lead frames. Finally the assemblies enter the oven, which can be interfaced with the robot, where the frame is fixed to the base by being embedded in a glass seal.

Human intervention is required, from time to time, to keep the robot supplied with parts. To achieve 6,500 assemblies per hour, it needs a new supply of bases every 55 minutes, seal boats every 10.5 min, and lead frames every 2 min. An optional $6,500 carrousel loader increases the latter interval to 45 minutes.

Although some semiconductor firms are developing in-house machines to automate this portion of production, "this is the only one with robotics," reports one IC maker who has seen the system. "It's an interesting concept. Mechanically, it's quite impressive."

On the table. Another Tucson firm, Modular System Research Inc., devised the robot's control system. A single Intel 8085 will oversee nearly all the machine's functions, says Claude Ceccos, research director at MSRI. The operating system works off state tables, which it checks in order to determine the status of the machine and hence the next operating step.

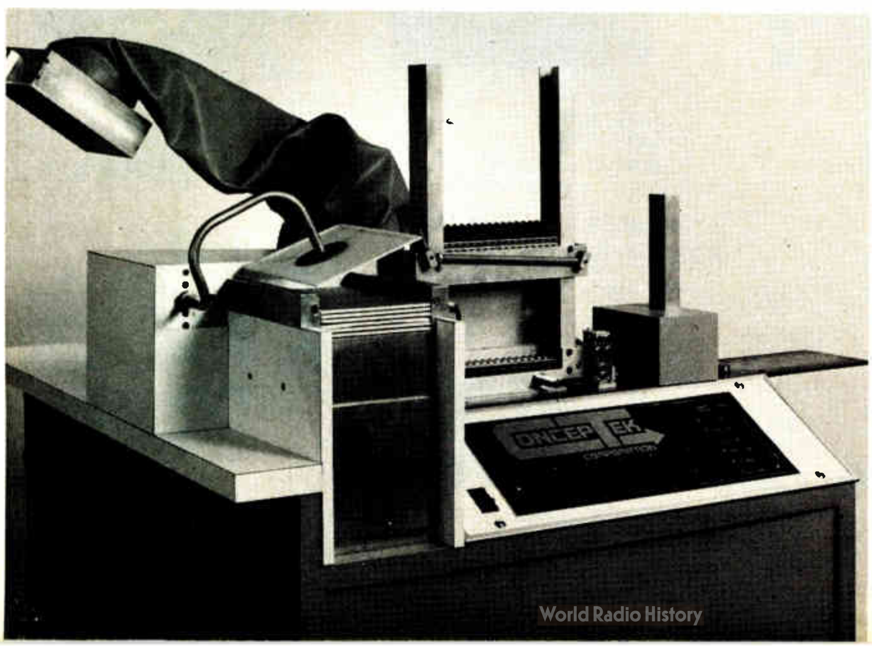
The microprocessor, which will use an estimated 8-K of programmable read-only memory and 1-K of random-access memory, controls between 30 and 40 sensors plus another 25 pneumatic actuators. Mechanically, the work gets done by servo motors and pneumatic power. Servo motors power the robotic arm and elevate the base trays. The remaining operations, like positioning lead frames, use pneumatics. Air-consumption demands are lower than 60 pounds per square inch, a pressure generally available at offshore sites.

A choice. De Luca is still uncertain whether the robots will be offered as standard products or customized. Each unit must now be designed for a given number of leads per chip and the size of the base, as well as the type of seal boat involved. Additionally, interfaces with the ovens will vary, he says.

Whether standard or custom, the list price will be $39,000, with discounts available for quantity orders having the same specifications. The customized units currently take three to four months to design and produce, De Luca estimates.

The first robot will be delivered in November to Motorola Inc.'s Semiconductor Sector in Mesa, Ariz. If all goes well with final development and the trial run at Motorola, De Luca expects to sell about 100 robots during 1982. -Terry Costlow

Fast worker. A robot arm that sucks up 2000 ceramic pieces at a time paces this automatic assembler, which loads bases and lead frames into IC seal boats faster than six humans can.



Photovoltaics

Seven-machine line builds solar panels

If the U. S. photovoltaics industry faces slow growth due to scarce government funding, the rest of the world will forge ahead in solar-energy investments. That is what Spire

Corp. is hoping for as it goes to market this month with what it says is the first commercially available integrated assembly line for solar-panel production.

Called the SPI-Line, the seven-machine system promises to produce up to 1 megawatt's worth of panels a year, based on a single daily 8-hour shift. System prices range from $250,000 for 100-kilowatt capacity to $500,000 for 1-MW capacity.

Three-quarters of the demand for SPI-Line will come initially from start-up photovoltaics enterprises in Europe, Japan, and Third World countries, projects Thomas E. Wilber, marketing vice president of Spire, based in Bedford, Mass. For now, he says, "Europe shows the greatest growth in private entrepreneurial ventures in photovoltaics with countries like France, Spain, and West Germany spending as much as 50% more in this area than the U. S."

Cell mates. SPI-Line's seven-machine system takes finished solar cells and assembles them to form sealed and framed modules. Typically, the modules have 50 cells for a 50-watt output and measure 48 inches long, 16 in. wide, and 2 in. thick. The assembly machines are semiautomatic and may be linked by optional automatic transport belts.

At the head of the line is a cell-tabber that applies metal-plated ribbons, or tabs, to the face of each cell. (The line can accommodate either circular or rectangular solar cells.) The machine reflow-solders one end of each ribbon to the cell, and cuts the other end to a length that will allow later soldering to the back of an adjacent cell in the solar-panel array. The tabbed cells advance to a tester-sorter, which performs go/no-go tests and sorts the cells into one of eight preselected output-level bins.

A cell-interconnect system then aligns the cells into a panel array, and again uses reflow soldering to connect tab ribbons to adjacent cells. A module-layup machine then places the cell array on what will be the panel's base.

This base consists of a sheet of Tedlar polymer, overlayed with a sheet of ethylene vinyl acetate (EVA) and a fiberglass sheet that supports and protects the cell-array interconnections. Once the cell array is in place on this substrate, the layup system covers it with a second layer of EVA and a glass cover that has been specially cleaned and primed by a glass-preparation station on the assembly line.

Making sandwiches. This solar sandwich then goes to a module laminator, which heats it up to 150° C, polymerizing the EVA layers. The clear EVA encapsulates the solar cells, and acts as an adhesive for the module layers. After that, a module-sealing and -framing system applies an edge sealant. Finally, it puts on the frame, completing the panel's construction.

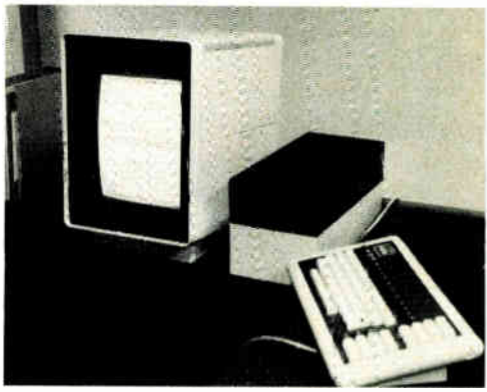
Though the semiautomatic SPI-Line's 1-MW maximum capacity is considerable—it represents last year's production at Arco Solar Inc., Chatsworth, Calif., a ranking U. S. producer—Spire has some upgrading in mind, including the use of robots. The company's long-term goal is a full line of equipment that processes silicon wafers into solar cells and then assembles arrays of cells. **-Linda Lowe**

Computer networks

Stanford work station migrates to industry

An inexpensive yet powerful computer work station from Stanford University is beginning to have a significant impact outside academia. Three Stanford designers have created a company to license the design to industry, where several designers already have found it to be a versatile systems building block.

Born from a Department of Defense research grant and subsequently nurtured by two professors and a graduate student, the Stanford University Network work station has already been licensed by VLSI Systems Inc. of Palo Alto, Calif., to five industrial firms. Fifteen of the units will soon enrich the university's own computer network.



Designers' choice. Stanford University designed this work station for in-house needs, but it offers so much computing power at a low cost that outside firms have licensed it.

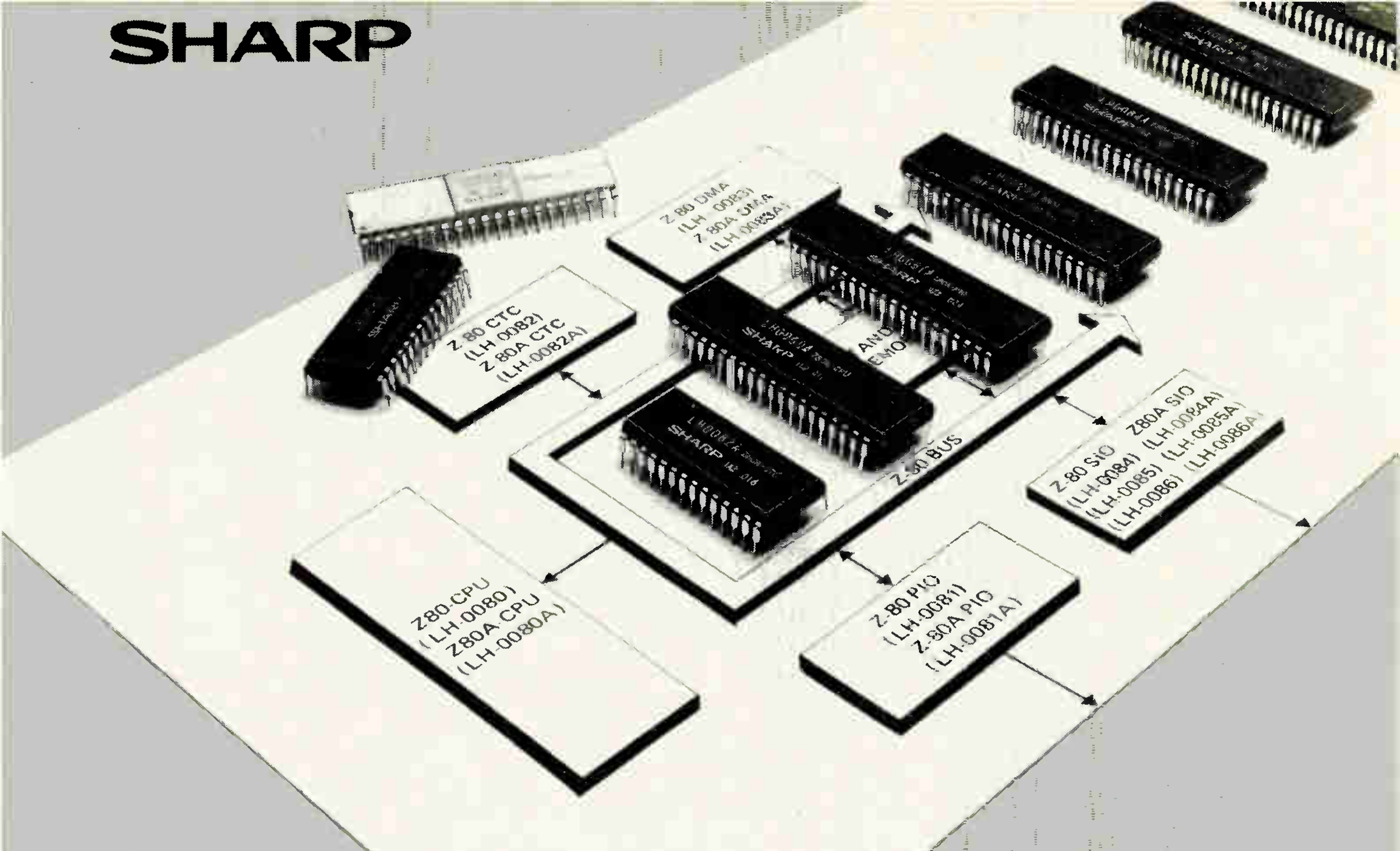
The station combines the power of the Motorola MC68000 microprocessor with the popular Intel Multibus, 250 bytes of random-access memory, an Ethernet link, and a high-resolution graphics package. It includes a keyboard, a mouse-pointing device, a video display similar to that of the Xerox Star, and an electronics module.

Popular board. The work station is built around three boards: the central processing unit, a high-resolution graphics board, and an Ethernet board. The CPU board, which a quarter megabyte of 64-K RAM shares with the 8-megahertz 68000 and a Multibus interface, has garnered immediate popularity. It first appeared as the heart of the CTS-300 computing system from Codata Corp., Sunnyvale, Calif. [*Electronics*, April 21, p. 215].

It is also being sold as a board product by Forward Technology Inc., Santa Clara, Calif., for $3,495 in single-unit quantities and by Pacific Microcomputer Inc. of San Diego, Calif. "By the end of the year we expect to have licensed 15 packaged products," asserts Forest Basket, the Stanford professor who initiated the project for DOD's Advanced Research Projects Agency.

Admirable architecture. Key to the processor-board architecture is a two-level, segment-page, multiprocess memory management scheme, as well as two serial input/output channels (Intel 8274), a timer chip

SHARP



Now may be the best time ever to review suppliers for Z-80/Z-80A !!

- Z-80/Z-80(A) SERIES

ZILOG	SHARP Type No.	Features	Package
Z-80 CPU Z-80A CPU	LH-0080 LH-0080A	• 158 instructions — includes all 78 of the 8080A instructions • Three modes of maskable interrupt plus a non-maskable interrupt • 22 internal resisters • •	40 DIP
Z-80 PIO Z-80A PIO	LH-0081 LH-0081A	• Two independent bidirectional ports • Any one of the following modes of operation may be selected for either port: Byte Input/output, Byte bidirectional bus, Bit Mode • •	40 DIP
Z-80 CTC Z-80 CTC	LH-0082 LH-0082A	• Four independent programmable 8-bit counter/16-bit timer channels • Single phase clock • •	28 DIP
Z-80 OMA Z-80A DMA	LH-0083 LH-0083A	• Single channel 2 port • Three classes of operation • 3 Modes of operation • Up to 1.25MB search rate • •	40 DIP
Z-80 SIO/0 Z-80 SIO/1 Z-80 SIO/2 Z-80A SIO/0 Z-80A SIO/1 Z-80A SIO/2	LH-0084 OH 0085 LH 0086 LH-0084A LH-0085A LH 0086A	• Two full duplex channels • Asynchronous operation • Binary synchronous operation • HDLC IBM SDLC Mode • 0 — 550k bits/Sec • •	40 DIP

Vcc (V): +5 • Z-80: clock frequency 2.5MHz Z-80A: clock frequency 4MHz

SHARP can provide this full line with high quality and excellent reliability.
Ceramic package types also available!

We have a versatile line of 4-bit to 8-bit microcomputers to meet various demands: Our Z-80/Z-80A series (CPU, PIO, CTC, DMA, SIO/0-2) are manufactured for controllers and terminals requiring complex processing while the SM series (4-bit 1-chip) are suitable for consumer product appliance.

- SM SERIES

Features \ Model No	SM 4A	SM 5A	SM 510	SM-520	SM-530	SM 531
Process	CMOS	CMOS	CMOS	CMOS	CMOS	CMOS
Power Supply Voltage	3V Typ	−3V Typ	−3V Typ	−5V Typ	−1.5V Typ	−1.5V Typ
ROM Capacity	2261 × 8 bit	1827 × 8 bit	2772 × 8 bit	3072 × 10 bit	2016 × 8 bit	1260 × 8 bit
RAM Capacity	96 × 4 bit	65 × 4 bit	128 × 4 bit	160 × 4 bit +16 × 2 bit	64 × 4 bit +24 × 4 bit	32 × 4 bit +20 × 4 bit
Instruction Set	54	57	49	93	47	43
Instruction Cycle Time	61μs	61μs	61μs	11μs	91.6μs	91.6μs
Remarks	LCD Direct Drive		LCD Direct Drive	Fluorescent Display Driver Ext	LCD Direct Drive	

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Circle 47 on reader service card

with five 16-bit timers (AMD 9513), up to 32-K-bytes of programmable read-only memory, and a 16-bit input port.

The on-board memory has parity error checking and, according to Stanford graduate student and VLSI Systems president Andreas Bechtolscheim, "the incorporation of RAM eliminates the wait states experienced through the Multibus."

The memory management scheme allows 16 contexts, or active processes, which may each be further divided into as many as 64 segments. The power of the processor is, like many, relative to the type of job processed. "For timed-integer work, it can have 40% to 50% the power of a DEC/VAX 780," says Stanford professor Vaughan Pratt, one of the founding trio and a director of VLSI Systems. "For I/O and floating-point operations, it is considerably slower," he adds.

Cinematic. The graphics board features a 1,024-by-1,024-bit frame buffer, with 800 by 1,024 bits dedicated to the visible display area. "What you see is the left three-quarters of the buffer. The right quarter is used as a cache for font storage and graphics symbols," notes Bechtolsheim.

It only takes 64 milliseconds to write an entire frame buffer, which gives the high-resolution display the 16-frame-a-second cinematic refresh rate that permits nonflickering moving images. The graphics board will first be used by filmmaker George Lucas to create effects for upcoming sequels in the Star Wars saga, according to VLSI Systems.

Networks. The Ethernet board follows Ethernet protocols, but operates at 3 megabits rather than the maximum 10 Mb/s of the standard.

Bechtolsheim acknowledges that a 10-Mb/s board would be useful, but points out that his board is considerably less expensive than Intel's 10-Mb/s board. "It's too expensive to have a network interface in the over $4,000 category," he says.

His next project is to design a color graphics board, and then the company will turn to the design of a 10 Mb/s board. **-Martin Marshall**

News briefs

CBS and AT&T set videotex trial in New Jersey . . .

They form a likely couple. CBS Inc. wants to get a feel for the kinds of services that subscribers to videotex interactive home information systems will buy; AT&T wants to add know-how in videotex terminals and computer systems to its expertise in telecommunications. So the two will join forces for a seven-month videotex trial, starting in the fall of 1982, in 200 households in Ridgewood, N. J. For AT&T, this is its second serious look at videotex—the company currently is evaluating the results of a 15-month trial conducted jointly with Knight-Ridder newspapers in Florida.

. . . and Siemens buys rights to Canadian videotex technology

Telidon, the second-generation videotex technology developed in Canada, may well end up as the *de facto* world standard for interactive home information systems. Already Telidon has strong backing from the U. S., Australia, and Venezuela. This month it gained a foothold in Europe when Siemens AG signed a contract with two Canadian companies—Norpack Ltd. of Ottawa and Infomart Ltd. of Toronto—to acquire Telidon technology, software, and hardware. Siemens will pay at least $10 million for its new videotex capability, which will enable it to add an alpha-geometric option to the European standard (CEPT) systems it now produces.

IBM restructures most its U. S. operations

Starting with the top group level, International Business Machines Corp., Armonk, N. Y., this month restructured its U. S. operations into three new groups. All U. S. marketing will be handled by the new Information Systems Group. Manufacturing and development will be realigned into two new groups, one for large systems and a second for small systems and office products. In early 1982, IBM will further split the Information Systems marketing group into two new divisions, each of which will market the full IBM product line to different sets of customers, a new strategy for the firm.

Production

Easy process makes metal-core pc boards

Metal-core printed-circuit boards have been around for some two decades, but they have not been particularly popular, despite their superior heat dissipation, because they are hard to make and therefore costly.

The boards are likely to become more prevalent, however, because General Dynamics' Pomona, Calif., division—with some help from the U. S. Navy—has come up with a new way of making them. The new process is similar to standard multilayer-board manufacture, with just two extra steps. What's more, because it works on standard circuit-board–lamination equipment, it is widely accessible. The metal-core boards, the company maintains, cost only about 20% more than normal epoxy boards and even less than boards with external heat sinks.

Laminated twice. The company's method is a straightforward double-lamination process, with the aluminum core material treated almost like another layer. The first lamination cycle starts with a 0.050-inch aluminum sheet that is predrilled with oversize component- and through-holes. Then an epoxy bonding-stage is used to fill the holes, coat the upper surface of the board, and attach the upper copper substrate. During this step, the epoxy filling the holes is drawn through a bleeder cloth and the excess absorbed by a blotter cloth, leaving the resin flush with the bottom of the pc board.

In the second lamination cycle, epoxy bonding sheets and a copper substrate are put on the lower side. From this point on, the board is handled conventionally, with excess copper etched off to form circuit pat-

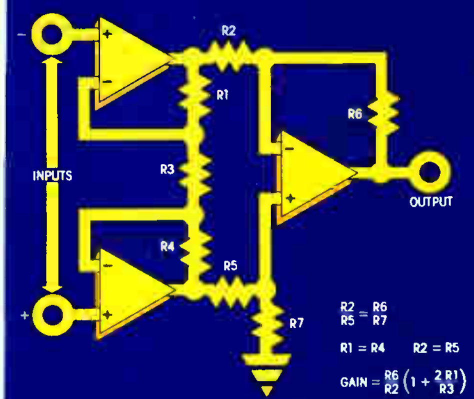
NATIONAL ANTHEM®

SPECIAL ISSUE

SEMICONDUCTOR NEWS FROM THE PRACTICAL WIZARDS OF SILICON VALLEY.

LM363 revolutionizes instrumentation amps.

NATIONAL'S NEW SINGLE-CHIP LM363:
HIGHER PERFORMANCE AND EASE OF DESIGN AT A LOWER COST.



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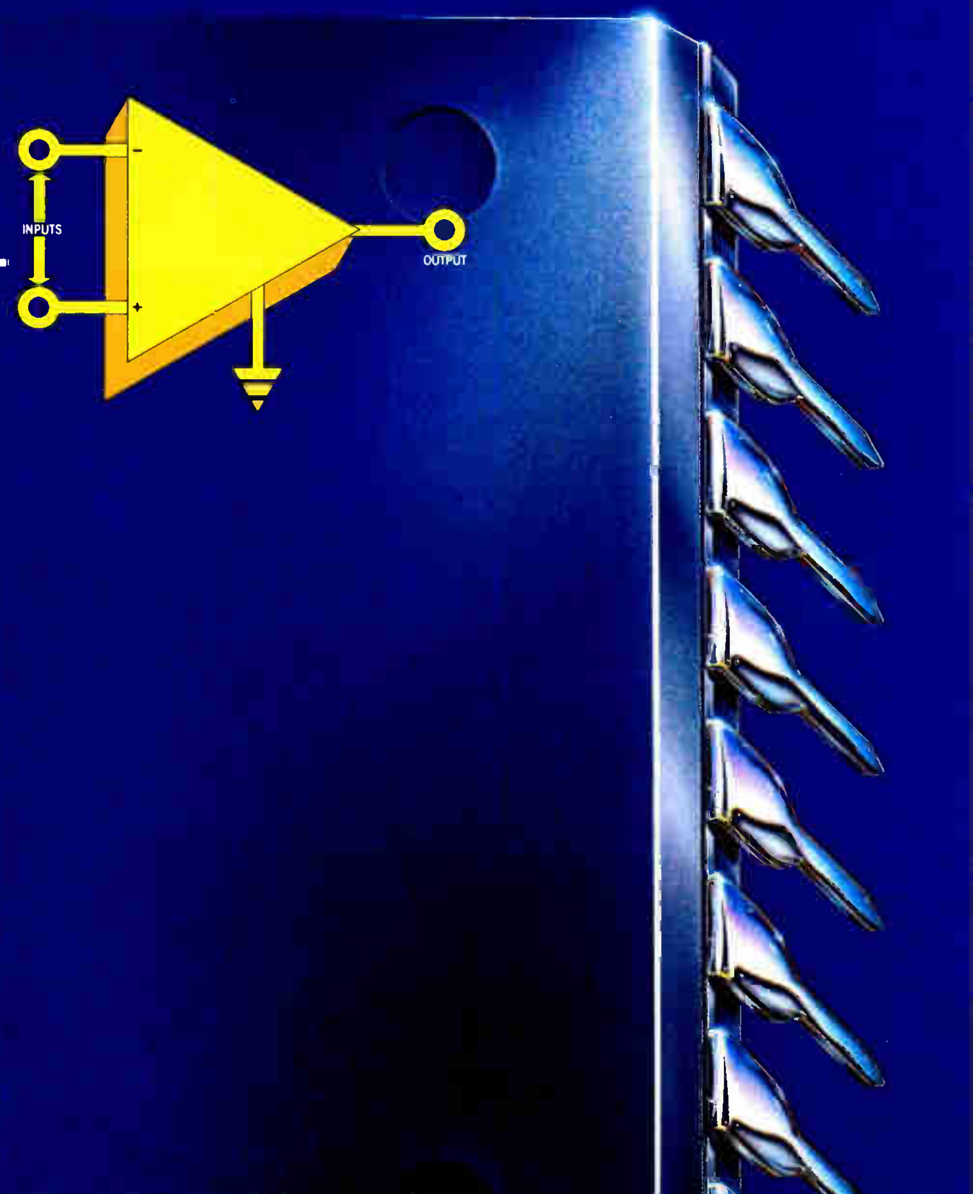


Unequaled performance from an instrumentation amp

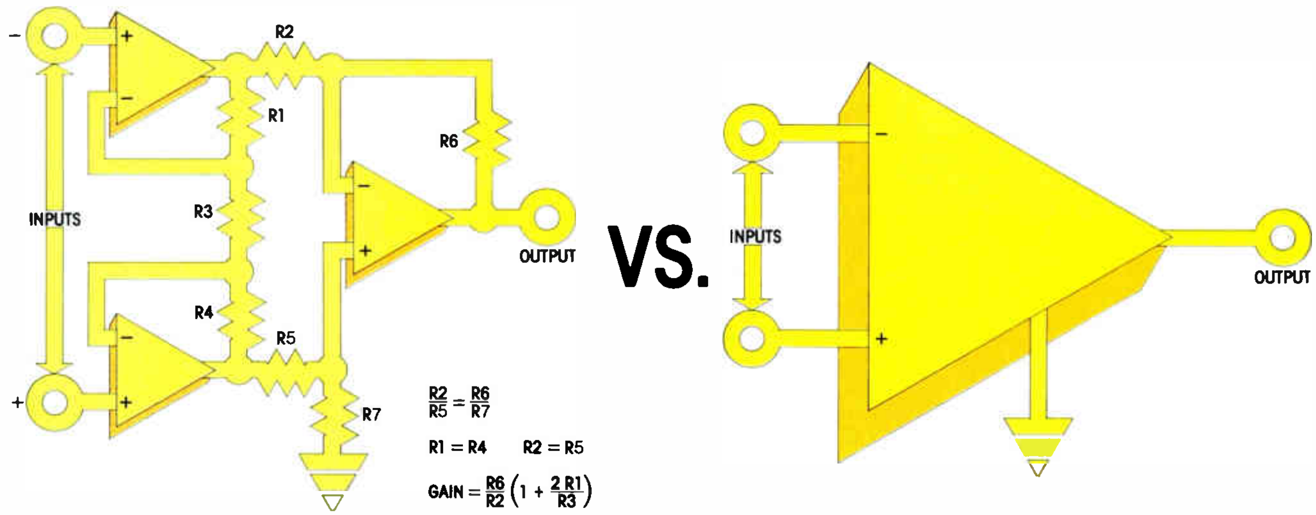
World's best complete 12-bit DAC

High-performance A/Ds, D/As, references and more

Free literature from the National Archives

SPECIAL DATA CONVERSION/ACQUISITION ISSUE

Self-contained LM363 combines higher performance and lower cost.



STANDARD 3 OP AMP INSTRUMENTATION AMPLIFIER.

NEW LM363 MONOLITHIC INSTRUMENTATION AMP.

The Practical Wizards' new monolithic LM363 obsoletes op amps used in instrumentation amplifier designs.

National Semiconductor has made designing with instrumentation amps considerably easier than ever before.

Until now, engineers had two choices when their designs called for a precision instrumentation amp. They could either use three op amps and a handful of expensive resistors (and all the time and board space that involves) or they could buy a costly module.

Well now there's a low cost high-performance alternative: National's new LM363 monolithic true instrumentation amp.

Totally self-contained. The LM363 (and its corresponding military version, the LM163) comes totally self-contained in an 8-pin TO-5 package. It requires no external resistors for accurate fixed gains of 10, 100, or 500 (one gain per package). Very high precision is attained by using trimmed-on-chip thin film resistors.

The Practical Wizards designed the LM363 with a super beta bipolar input stage that yields very low input voltage noise, an extremely low offset drift, and a high common mode rejection ratio.

See the table below for typical values.

Versatility and ease of use. High performance, however, is only part of the story.

National's new LM363 is considerably easier to design into Data Conversion/Acquisition applications than it is to design one's own instrumentation amp. This not only saves time and effort, but board space and money as well.

For added versatility the internally set gains may be increased via external resistors.

The LM363 will soon be available in a 16-pin DIP, with pin-strap gain options of 10, 100, and 1000. The twin differential shield driver pins on this version can be used to eliminate bandwidth loss due to shield capacitance. Also, compensation pins will be available to allow simple low-pass filtering.

LM363 PERFORMANCE SPECS**

	GAIN 100	GAIN 500	UNITS
V_{OS}	50	20	µV
$\Delta V_{OS}/\Delta T$	0.5	0.2	µV/°C
I_B	2	2	nA
CMRR	120	130	dB
NOISE	12	7	$nV/\sqrt{Hz}$
GAIN ERROR	0.1	0.1	%
GAIN NON-LINEARITY	.005	.007	%

The low cost LM363—now available for as little as $9.60* @ 100 pcs.—is a perfect example of how National continues to revolutionize Data Conversion/Acquisition technology.

For all the details on the remarkable new LM363, check box 090 on this issue's National Archives coupon.

*U.S. prices only.
**Data shown represents typical values.

A graphic look into the world's best, complete 12-bit DACs.

The totally self-contained DAC1280A and DAC1285A Series offers lower power and higher speed than the industry standard DAC80s, DAC85s and DAC87s.

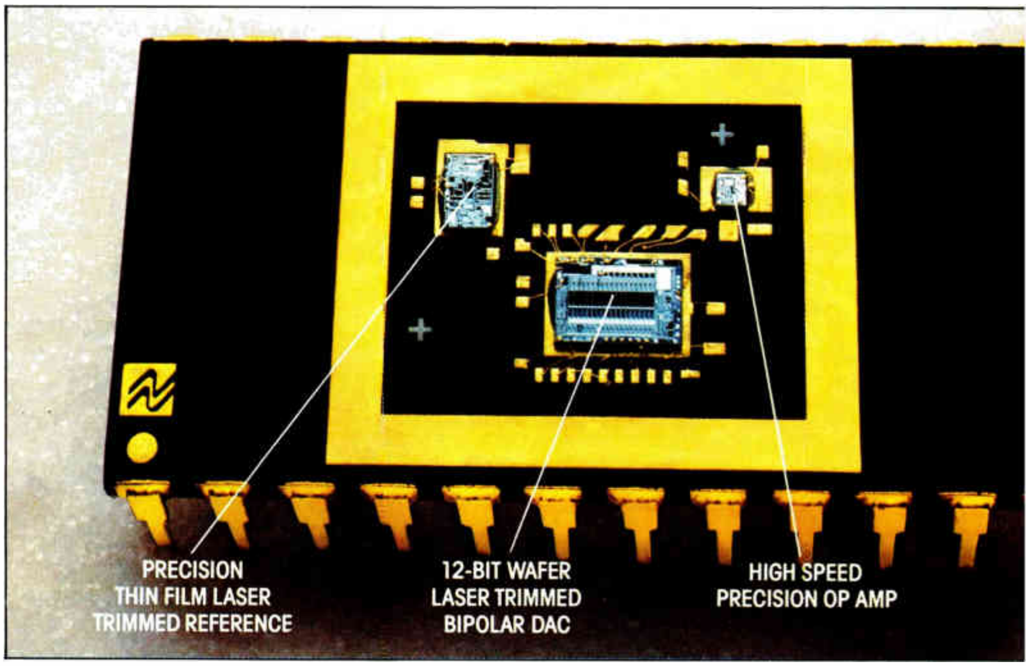
National Semiconductor now offers the highest performance complete 12-bit DACs: their new DAC1280A and DAC1285A Series.

These converters each contain their own DAC, op amp, reference and feedback resistors, all on just three dice. That adds up to low cost and high reliability over the life of the DAC.

In short, they provide higher performance than any DAC80 product now available. (See the DAC cross-reference table below for National's pin-compatible upgrades for standard DAC80s, DAC85s and DAC87s.)

12-BIT DAC CROSS-REFERENCE TABLE

NATIONAL P/N	ALTERNATIVE P/N
DAC1280AC	DAC80-CBI-V; DAC80Z-CBI-V
DAC1285C	DAC85-CBI-V
DAC1285AC	DAC85LD-CBI-V
DAC1285A	DAC87-CBI-V



The new industry standard is here. National's DAC1280As and DAC1285As offer superior performance advantages over today's 12-bit DACs, particularly in terms of speed and power dissipation.

These fast converters settle to full scale accuracy in only 300ns (current mode) and 2.5μs (voltage mode), while dissipating only 500mW.

The DAC1280A, for example, guarantees maximum linearity error of ±½ LSB over the entire 0°C to 70°C temperature range. It also guarantees a ±¾ LSB differential non-linearity and a precise 6.2V reference (±2%) over temperature.

In addition, all specs are guaranteed over a ± 11.4V to ± 15.75V supply voltage range.

The DAC1280A's complementary binary logic inputs—also guaranteed over temperature—are compatible with TTL and CMOS logic levels.

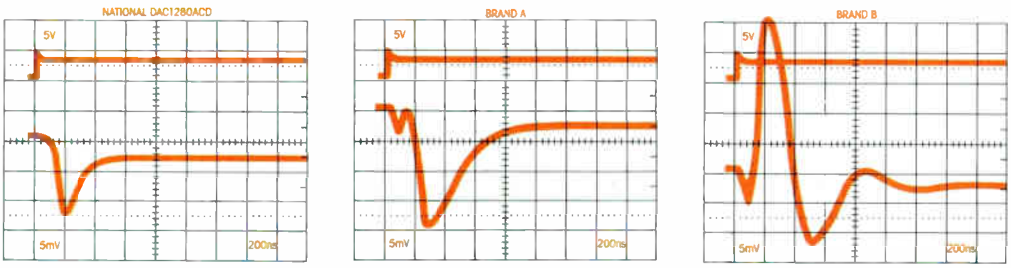
Self-contained reliability and price. National's 3-die design offers a variety of cost advantages as well as reliability advantages.

Initial savings stem directly from a less complicated, and hence less costly, manufacturing process. But more importantly, the standard IC construction technique results in reliability enhancements over the other DAC80s. And that means dependable performance over the long term.

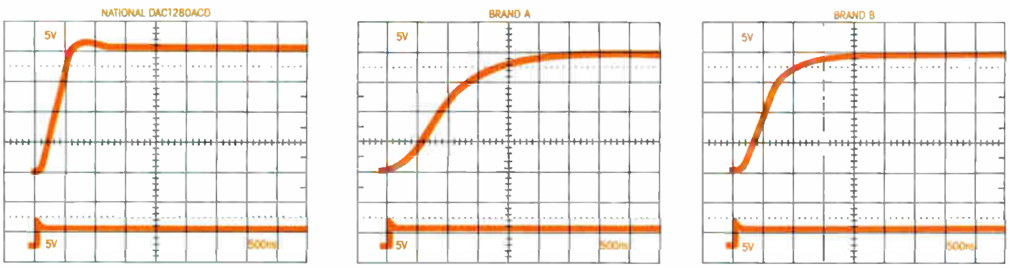
The new low cost, high performance DAC1280A and DAC1285A Series are perfect examples of how the Practical Wizards at National continue to overcome industry limits in Data Conversion/Acquisition technology.

For complete details on the world's most reliable 12-bit DACs, check box number 057 on this issue's National Archives coupon.

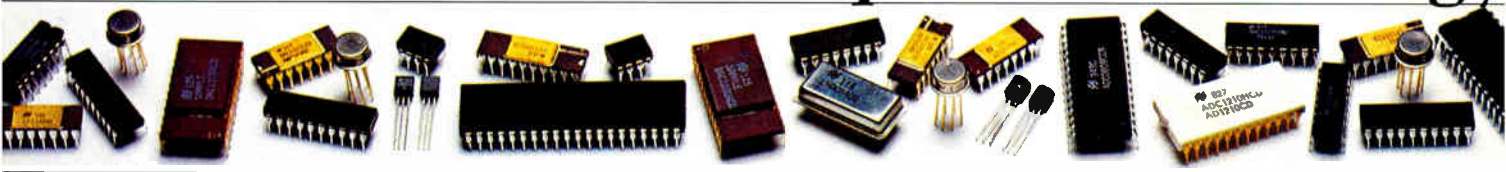
SETTLING TIME FOR 1 LSB CHANGE



FULL SCALE SETTLING TIME −10V TO +10V



Part of the reason why National leads in Data Conversion/Acquisition technology.



The Practical Wizards let their technological leadership speak for itself—in terms of price and performance—for part of their wide range of components.

No single semiconductor manufacturer covers the Data Conversion/Acquisition market as extensively as National. Their DAC1280A, DAC1285A D/A converters and LM363 instrumentation amps are just the latest examples of the kind of technological leadership that's expected of Practical Wizards.

They already offer a broader selection of higher performance components than anyone else. The products featured below offer a taste of where Data Conversion/Acquisition technology is going.

μP-compatible D/A converters. National's line of μP-compatible 8-, 10-, and 12-bit DACs offers:

- guaranteed monotonicity.
- low power dissipation.
- operates in voltage switching mode for single supply fixed reference applications.
- works with up to ±10V reference—full four-quadrant multiplication.
- .3" center 20-pin package.

Their DAC0830 Series of 8-bit D/A converters provides:

- linearity over temperature of 10-, 9-, and 8-bits.
- gain tempco of 0.0006% FS/°C max.

Their DAC1006 Series of 10-bit D/As also feature a linearity over temperature of 10-, 9-, and 8-bits.

In terms of 12-bit DACs, their DAC1230 Series features:

- linearity over temperature of 12-, 11-, and 10-bits.
- gain tempco of 0.0006% FS/°C max.

μP-compatible 8-bit A/D converters. National's family of low-cost 8-bit A/Ds also point up their leadership in Data Conversion/Acquisition. Each of these high-performance parts feature:

- easy interface to all microprocessors.
- 0 to 5V analog input voltage range with a signal 5V supply.
- no zero or full scale adjust required.
- total error (including linearity, full scale, and zero error) is just ±½ LSB or ±1 LSB.
- 100 μsec conversion time.

Their ADC0801/02/03/04 converters, for example, offer all this plus differential analog input all in a .3" 20-pin DIP.

Add to this their ADC0808/09, which feature 8-channel multiplexers with latched control logic.

To round out the family, their ADC0816/17 A/Ds carry a 16-channel multiplexer with attached control logic in addition to direct access to "comparator in" and "multiplexer out" for signal conditioning.

Precision references. National also proves to be the industry's best reference for references. Because in addition to offering the broadest line of IC voltage references, this family of parts includes:

- the lowest power available—12μW (the LM385-1.2V).
- the lowest drift available—.5ppM/°C (the LM199AH).
- the lowest prices available—$.45* @ 100 pcs (the LM329DZ).
- the widest range of voltages—½V to 10.24V.

IC temperature sensors. Many Data Conversion/Acquisition systems rely on temperature sensors for accurate and dependable analog data. National offers an extensive line of devices to fill this need. Some of them, the LM135 and LM335, feature:

- untrimmed accuracies of ±1°C, ±3°C, and ±6°C.
- trimmed accuracy—±0.3°C (±1°C max.).
- temperature ranges available from −55°C to +200°C.
- low prices start at $.95* @ 100 pcs.

For complete information on these and other high performance Data Conversion/Acquisition components, check the appropriate boxes on the coupon below.

*U.S. price only.

What's new from the National Archives?

- 017 ☐ LM385, LM329, LM399 Reference Data Sheets
- 018 ☐ LM335 Temp Sensor Data Sheet
- 023 ☐ ADC0801/02/03/04/, ADC0808/09, ADC0816/17 Data Sheets
- 051 ☐ Data Conversion/Acquisition Data Book ($7.00)
- 057 ☐ DAC1280A and DAC1285A Data Sheets
- 071 ☐ LH0070 Reference Data Sheet
- 072 ☐ CMOS MICRO-DAC Data Sheets
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DAC 2

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terns. The drilling and the second lamination represent the two extra steps compared with standard multilayer-board production processes. But applying the epoxy one side at a time, rather than to both sides at once, has an advantage: it eliminates most of the air bubbles that can cause shorts later, when the holes are redrilled and plated through with copper to interconnect the layers.

High dissipation. In operation, heat is carried from the board through the mounting screws, which also serve as an additional ground. The dissipation is far beyond that of conventional epoxy boards. In a test of boards in actual use, the prototype metal-core board was run at four times the current level of a similar epoxy board—a level that would have burned up the latter. After six minutes, the temperature of the components on the prototype rose from 75° to 136°F, only 12°F higher than the rise for the epoxy board's components.

As a result, General Dynamics is confident enough in the boards and their manufacture to use them in the autopilot regulator board for the Standard Missile 2, which will be shipped to the Navy next year. The development was partially funded by the Naval Ocean Systems Center's manufacturing technology group in San Diego. NOSC is preparing to release process information.

"It's a rather simple way to do the job for those who have lamination presses," says George Messner, senior scientist at PCK Technology, a Melville, N. Y., firm now researching polymeric coating of metal-core boards. That method, currently used in large numbers for telephone circuits by Western Electric Co., requires much more capital equipment than GD's method.

Litton Industries Inc. has for 10 years also been making metal-core boards, forcing powdered epoxy into the through-holes under pressure and temperature. This method yields approximately the same results as General Dynamics' double-lamination process, but requires special handling to avoid contamination from the powder. -Terry Costlow

Microprocessors

AMD changes tune for 16-bit families

Advanced Micro Devices Inc. touched off a ripple of surprise among semiconductor people three years ago when it launched an aggressive advertising campaign proclaiming that the AmZ8000, its second-source version of Zilog Inc.'s 16-bit microprocessor, was better than Intel Corp.'s competing 8086.

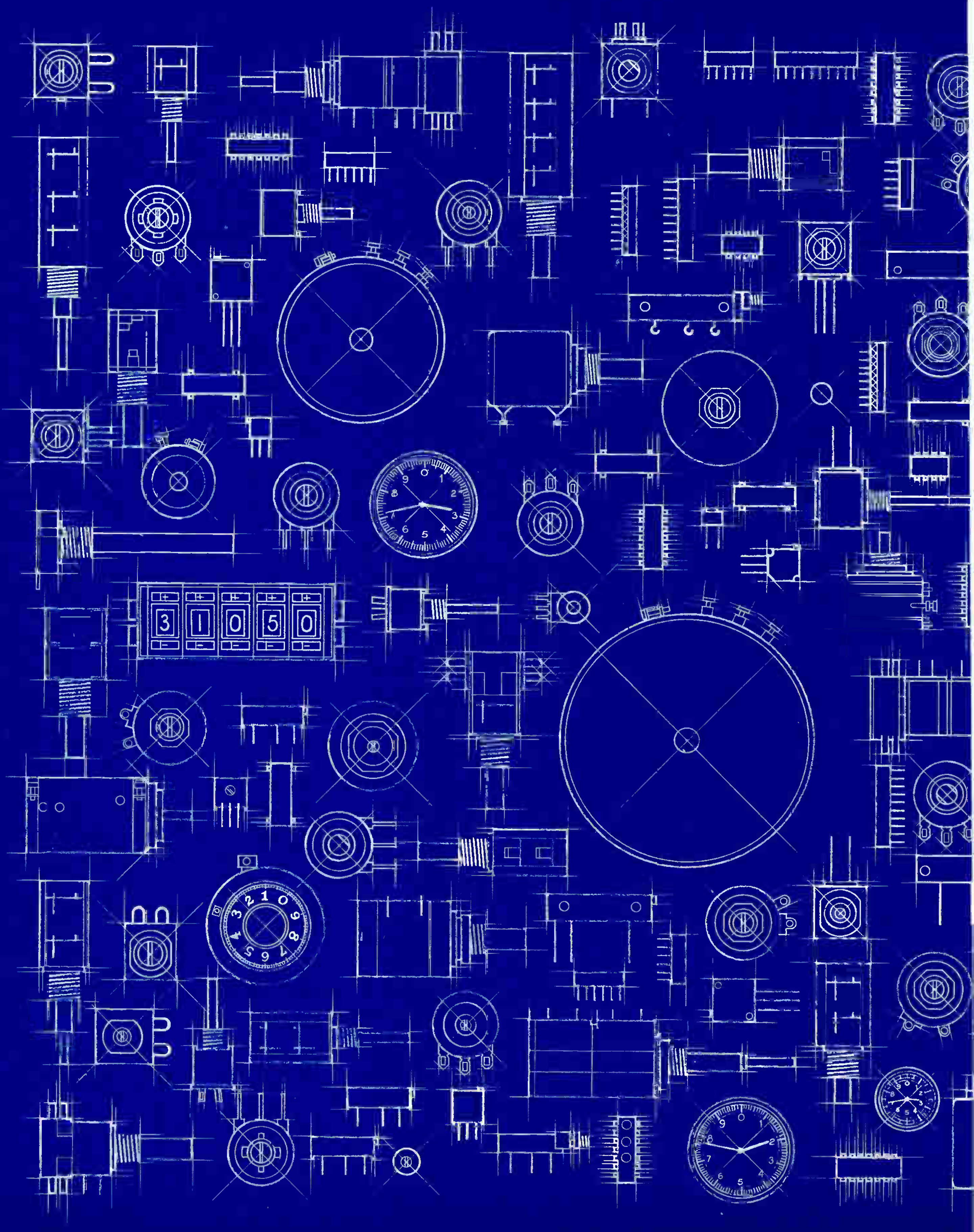
This month, AMD made waves again—so the cartoon character who touted the Z8000 over the 8086 will have to change his line. The Sunnyvale, Calif., company has signed a 10-year contract to back the 8086 with Intel of neighboring Santa Clara. The move, notes AMD chairman Jerry Sanders, "is due mainly to the demand from our customers. They have been designing in the 8086 and we felt a need to swing our mil-spec fabrication facilities to where the market is going."

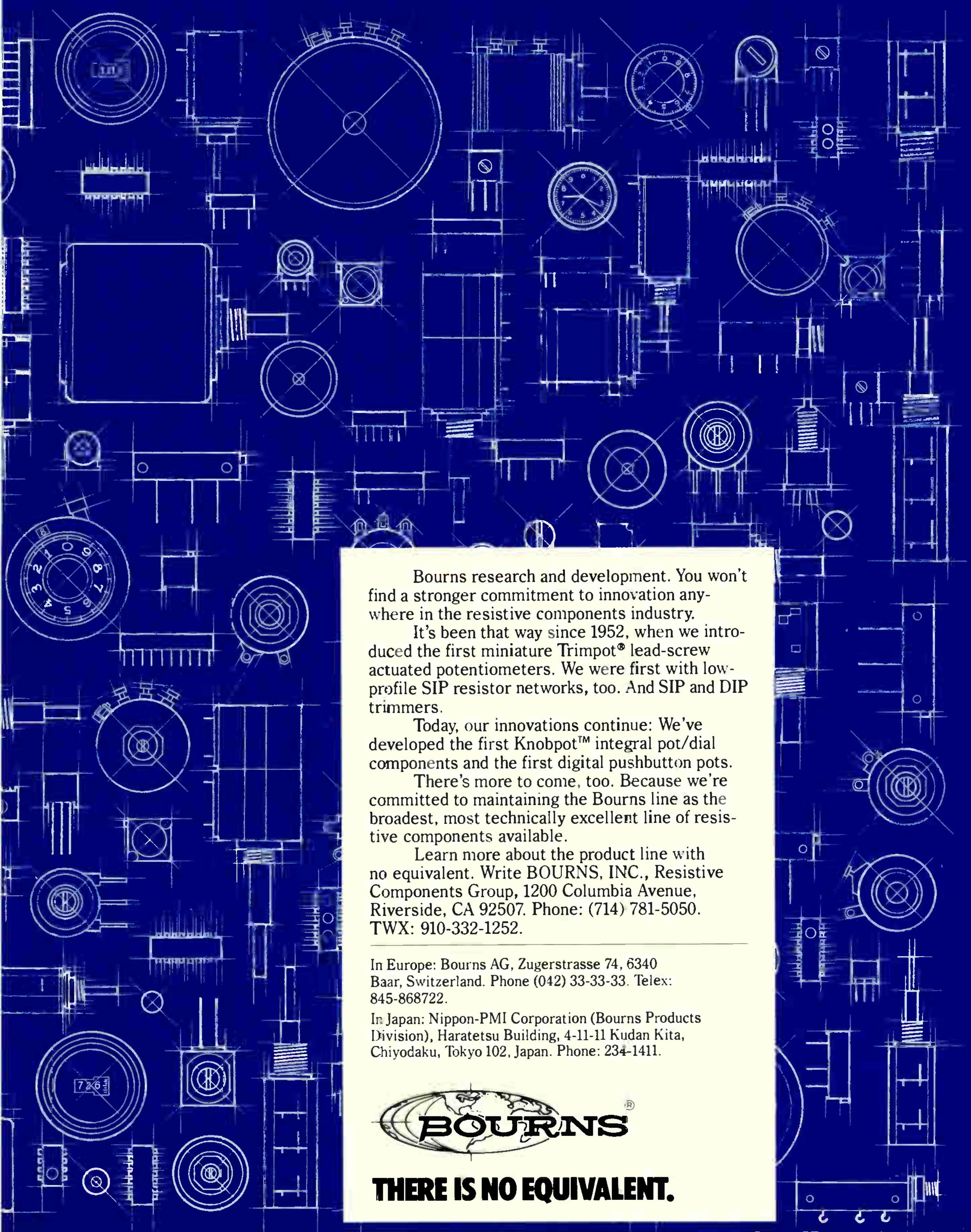
Mask marvels. Under the contract, Intel will supply AMD with masks for the 8086 family and in return receive masks for peripheral chips that AMD developed originally for the Z8000. But there is more involved in the deal than just the 8086 itself.

To start with, there's the 8087 arithmetic processor, the 8088 processor with an 8-bit bus interface, and the 8089 input/output processor. Then there's the 8200 family of support circuits, including the 8251 communications interface chip. The pact also covers the 8-bit 8051 single-chip microcomputer and two unannounced parts (presumably the iAPX-186 single-chip microcomputer and the iAPX-286 microcomputer with on-chip memory management), as well as future n-channel MOS and complementary-MOS upgrades to all the chips involved.

With the headstart of masks and test tapes, AMD figures it will have sample quantities of the 8086 in production during the first quarter of 1982, with 8088s to follow in the

THERE IS NO EQUIVALENT R & D.





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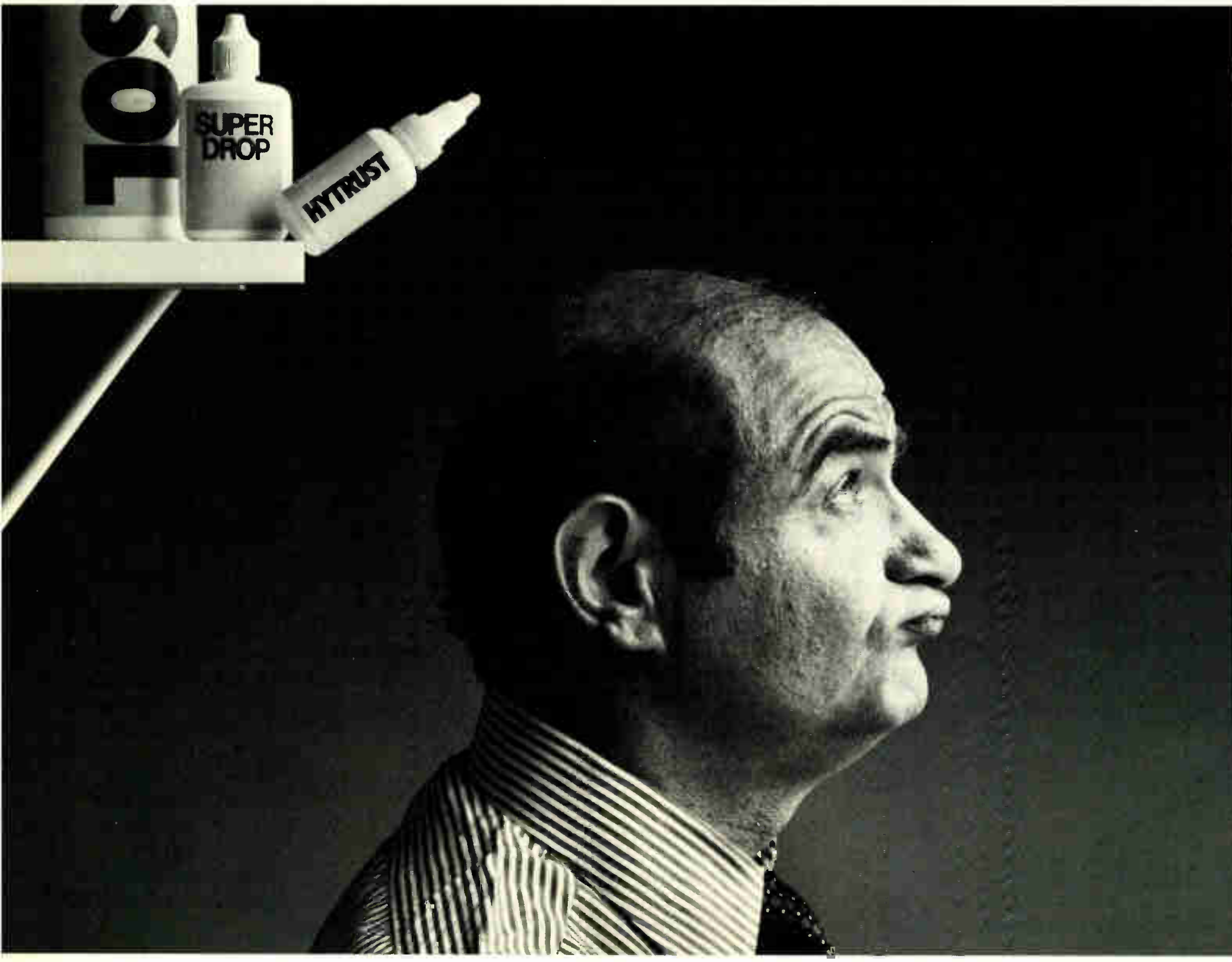

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Washington newsletter

Reagan to upgrade military C^3 systems in extensive overhaul

Dramatic improvements in strategic command, control, and communications (C^3) systems have high priority in the Reagan Administration's many-pronged, $180.8 billion program to upgrade U. S. strategic offensive and defensive weapons over the next several years. **Some $10 billion to $15 billion is earmarked for C^3 from fiscal 1983 through 1988.** Says a Pentagon report: "We will initiate a vigorous and comprehensive research and development program leading to a communications and control system that would endure for an extended period beyond the first nuclear attack." The Pentagon plans to improve the survivability, performance, and coverage of early-warning satellites and radars, including the construction of two additional Raytheon Pave Paws radars in the Southeast and Southwest. It also plans to upgrade the survivability and capability of command centers such as the E-4B and EC-135 airborne command posts and to develop very low-frequency and low-frequency communications receivers for deployment aboard bombers. It also will develop a new satellite communications system with high-frequency channels to ensure two-way communications between commanders and forces.

FCC wants to cut satellite spacing

The Federal Communications Commission will call for industry comments in late October on a proposal to reduce communications satellite spacing in orbit from 4° to 2°. The move would involve only satellites using the 4- and 6-GHz frequencies. **The change is needed because of the number of new satellites being proposed by industry over the next five years.** With 4° spacing, there are approximately 18 slots suitable for domestic satellites without using the marginal areas. By reducing spacing to 2°, the number of usable slots would increase to 36, yet satellites would still be separated by about 200 miles in their 22,300-mile-high orbits.

Senate approves AT&T expansion

A landslide 90-to-4 vote marked the passage by the U. S. Senate of a bill that permits American Telephone & Telegraph Co. to enter such unregulated businesses as data communications through a separate subsidiary. The Senate action comes after six years of debate over how to amend the 47-year-old communications law. While AT&T chairman Charles L. Brown complains that, in mandating competition, the legislation "puts the reins on us but gives spurs to everyone else," he is pleased to see Congress moving on a legislated solution to deregulation in the industry. **The Reagan Administration has promised AT&T that the Justice Department will drop its massive antitrust case** against the telephone company as soon as Congress writes legislation that will protect the Bell System's competitors from encounters in the marketplace with an AT&T subsidiary that is too closely tied to the resources of its monopoly parent.

FCC postpones deregulation date for telecom gear

The Federal Communications Commission has extended from March 1, 1982, to Jan. 1, 1983, the date for deregulating new telephone and terminal equipment installed in homes and businesses. The commission found that the communications carriers and the Government would need this additional time to put into effect its April 1980 decision to stop regulating this equipment and enhanced telecommunications services. **But the commission decided that it will phase in deregulation of the equipment installed before Jan. 1, 1983.** Telephone companies sought to deregulate all equipment—whether new, installed, or for inventory—at one time.

Washington commentary

The Shinto perspective

Nippon Telegraph & Telephone Public Corp.'s president Hisashi Shinto was careful to describe his visit to Washington last month as nothing more than "getting to know America and its people" in Government and the telecommunications industry. Nevertheless, as Shinto got to know Commerce Secretary Malcolm Baldrige and other Government officials, he was discretely advised that they are looking for NTT to open its telecommunications equipment market to U. S. suppliers fairly promptly.

As Baldrige put it in an interview the evening before his meeting with Shinto at the Department of Commerce, "I am going to begin by discussing our trade deficit and go on from there." In 1980 the U. S. trade deficit in telephone and telegraph equipment alone totaled $156.7 million, up 60% from the year before [*Electronics*, Aug. 25, p. 57] and almost all of that increase from Japan.

A broad view

But during a conversation that same evening at a special reception given by the Electronic Industries Association's Communications division, Shinto remained adamantly noncommittal about purchasing imports from America. While speaking broadly about NTT's interest in U. S. mobile-cellular-telecommunications and digital-private-branch-exchange technologies—areas where he concedes this country is leading the world—the executive backed away from questions about how much, if any, of these markets in Japan might be opened to U. S. vendors, and how soon. Yet only a few days later NTT disclosed its planned new agreement with International Business Machines Corp., under which IBM will provide NTT with insight on automated switch and computer production technology in return for being admitted into the NTT market.

NTT is unlike its counterpart, American Telephone & Telegraph Co., in that it has no production capability to match AT&T's Western Electric Co. But NTT is very much like AT&T in other ways—not surprising since the latter helped establish the Japanese company during the U. S. occupation after World War II. Yet NTT does operate with a government-approved budget, unlike AT&T, and it is this issue that Reagan Administration officials are using to persuade the Japanese government to prod the Japanese company to open its markets to American technology. It is a hard, slow process.

Signs that the Japanese government is beginning to respond to these pressures can be seen in the recommendations of its Procedural Commission for Administrative Reform that NTT divest itself of some of its operations, such as data-processing services. But NTT is resisting this and other government proposals, much as AT&T resisted the competition and change proposals of the Federal Communications Commission in the mid-1960s and the 1970s.

Evidence of this intransigence abounds in the comments of American suppliers anxious to compete in the NTT market. "NTT may say it is opening up, and show you the proposal requests to prove it," says one executive of a major U. S. telecommunications producer. "But you can't believe it when you receive a copy of the proposal between 30 and 90 days before its due date, during which time you are expected to analyze it, respond, and have that response translated into Japanese. You know you are not going to win. It is much like doing business with an American agency like the Department of Defense: if you don't learn of the competition until it is formally published, you might as well forget about bidding."

A second U. S. executive cites another problem in NTT's approach. "The quantities of equipment are often small" in NTT's proposal requests, he says. "They are not worth the administrative effort to prepare a bid unless you can offer off-the-shelf hardware. And that's not very often."

A world role for NTT?

About all the above complaints demonstrate is that NTT has learned well from its creators in this country. What is more fascinating to some U. S. telecommunications executives is that NTT may now be in the process of learning even more from AT&T about competing in new domestic and world markets. What intrigues them about the new NTT-IBM relationship, for example, is its suggestion that NTT, because it lacks a manufacturing capability, may be considering similar coalitions with other hardware makers as a means of joining Japan's telecommunications-equipment export brigade.

The Secretary of Commerce and the U. S. Trade Representative would do well to factor that prospect into their planning for the longer term. For, while they concentrate their efforts on breaking down Japanese barriers to a U. S. entry into NTT's domestic markets, they may one day discover that NTT has broken out as a supplier to the rest of the world. **-Ray Connolly**

OCTOPLUS

The Sprague Monolithic Arrays That Provide the Muscle of 8 SCRs in a Single DIP.

Sprague UTN-2886B and UTN-2888A SCR arrays are expressly made for use with microprocessors which are strobing power loads. Compatible with TTL, LSTTL and CMOS, they will interface to high-current loads including lamps, relays, and solenoids.

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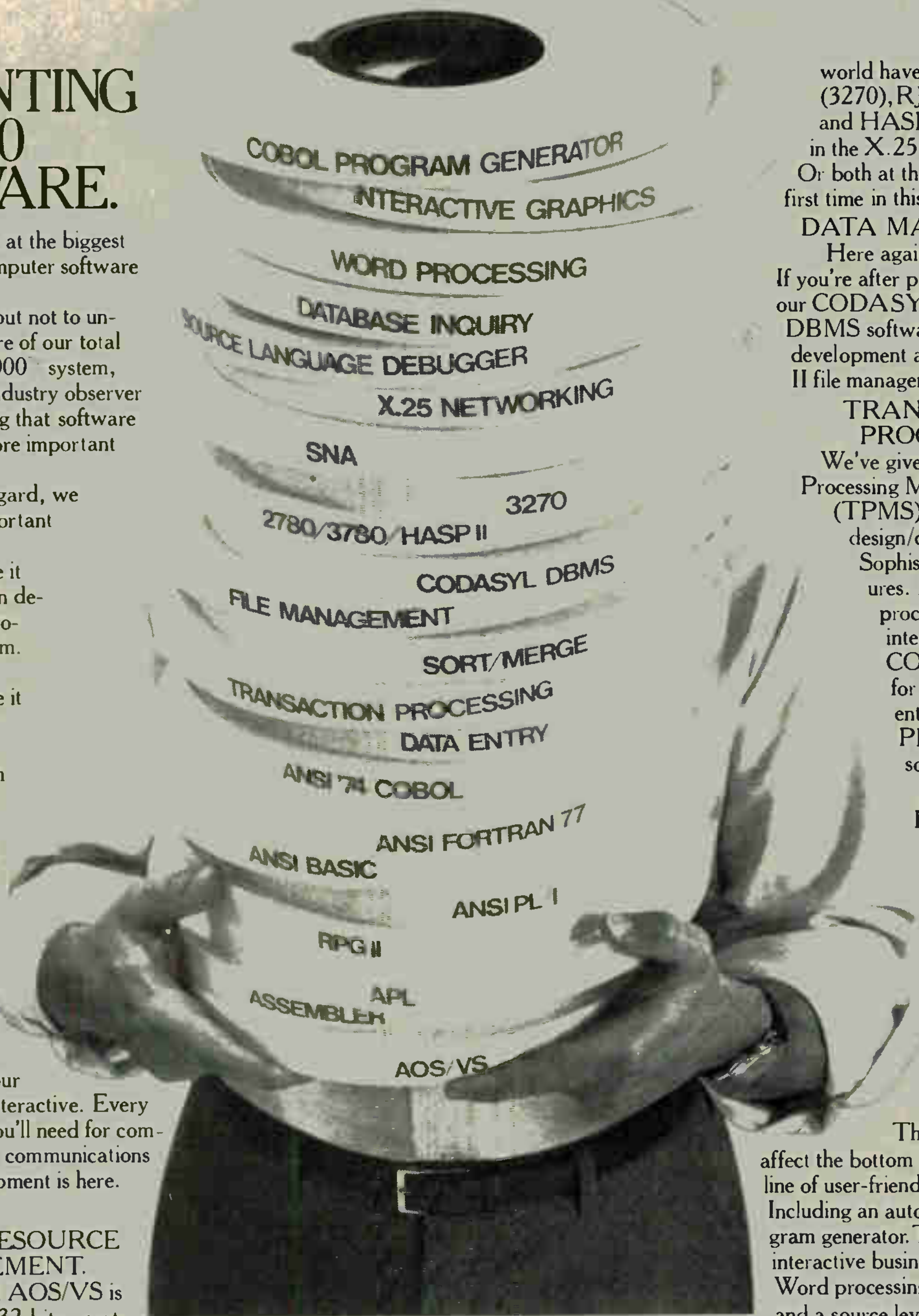

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Data General

Circle 63 on reader service card

Oct. 20, 1981

Electronics International

GaAs oscillator delays only 17.1 ps per stage: page 73

Substrates 2 inches square are basic to a highly automated production line that can process 320 hybrid circuits an hour: page 76

Japanese microcomputer uses silicon software

Japan's first solid-state-software microcomputer is how Nippon Electric Co. bills a low-power complementary-MOS microcomputer that includes a tiny Basic interpreter in 5-K bytes of read-only memory and 128 bytes of random-access memory on chip. Among many other silicon-software products to follow from NEC, says associate vice president Tomihiro Matsumura, will be a real-time operating system for the 8086 similar to Intel's iRMX-86 and a microcomputer with an interpreter for a full Japanese industrial standard version of Basic. He predicts that by 1985 there will be **a crossover between production of microcomputers for machine language and those for high-level languages.**

The new μPD7901G interfaces directly with a keyboard so that the addition of a liquid-crystal-display controller and external memory for the user's programs turns it into a pocket computer. It is also suitable for industrial applications because of the ease of writing software.

Strong dollar dims Western Europe's 1981 electronics growth

At 1980 exchange rates, Western Europe's entire electronics market in 1981 in would reach $103 billion—an 8% increase over the previous year, estimates the 1982 Yearbook from Mackintosh Consultants Ltd. of Luton, Beds. But the strong appreciation of the dollar will turn that growth into a decline of 7% to $97 billion. In terms of local currencies, the largest European market, the Federal German Republic, will expand around 7.5% in 1981; France will spurt 15%; and the UK will be up 9.6%. In particular sectors, data-processing equipment will be up 13.5% at constant 1980 exchange rates but down 4% in U. S. dollars in 1982. **In semiconductors, however, the apparent slump in the market-place produced by exchange rate variations is real,** dipping 7% in 1982—for Europe as a whole, from $4.4 billion in 1980 to $4.1 billion in 1981. Integrated circuits will share this decline but in 1982, says Mackintosh, should bounce back 15% to $3.1 billion.

Telefunken, Bosch to make telecom deal

Watch for an agreement to be hammered out this month between West Germany's AEG-Telefunken and Robert Bosch GmbH, giving the latter a 20% to 25% share in each of three AEG-Telefunken communications activities: Telefonbau und Normalzeit, a producer of telephone exchange systems; Olympia Werke AG, maker of office equipment and electronic mail terminals; and AEG-Telefunken's long-distance communications and cables division. For Stuttgart-based Bosch, best known as an automotive accessory maker but also active in consumer electronics and studio equipment, the deal adds telecommunications to its far-flung operations. For Frankfurt-based financially troubled AEG-Telefunken, the Bosch participation spells **a source of cash it badly needs** to play a greater role in the world's telecommunications markets.

Japan to liberalize carrier services

The value-added network bill that Japan's Ministry of Posts and Telecommunications expects to submit to the Diet at the session starting in December will allow such networks to lease circuits from the country's domestic and overseas carriers, Nippon Telegraph & Telephone Public Corp. and Kokusai Denshin Denwa Co. The new law **will probably restrict foreign firms' participation,** but should go a long way toward satisfying Japanese industrial firms and financial institutions, which have been clamoring for liberalization of communications circuits.

Office work station records speech

Voice, text, and graphics are combined in an advanced work station developed by Britain's Office Technology Ltd., part of the Information Technology Group. The station, which uses two Intel 8086s, allows an executive to annotate displayed documents orally. **His or her comments are digitized and stored centrally on disk for subsequent recall together with the document.** A secretarial version uses one 8086 and lacks the voice facility. A minimum system of two work stations with a controller is priced around $37,000, but extra work stations can be added at $9,300 with voice or $6,700 without. Future plans include the provision of electronic mail and connection to a local network. The station was developed by four ex-IBM engineers from the company's Hursley Park Research Centre.

Japan weighing sensors for missiles

Japan's Defense Agency says it plans **to develop charge-coupled-device infrared–image-sensor area arrays** to provide sight for missiles and other applications. It has an ongoing research program under way at its Technical Research and Development Institute, but a spokesman says that it will rely on manufacturers for experimental devices. As usual, Japanese firms are reluctant to reveal they are participating in a defense agency program. **Meanwhile, Sony Corp. is negotiating with the National Aeronautics and Space Agency** of the U. S. with regard to NASA's purchase of several video cameras using CCD technology. The company says NASA has not said what the cameras would be used for.

Video-cassette plant planned in Germany

Anticipating a continued boom in the demand for video cassettes, West Germany's BASF AG will spend about $46 million for a new video cassette factory near its home base in Ludwigshafen. The plant, whose construction will start next year, will go on stream by 1983. Basically a chemical producer but heavily engaged in magnetic tape and related products, BASF claims to be the world's only company fabricating cassettes for all the video recording systems currently on the market: Japan's VHS and Betamax systems and Europe's VCR and Video 2000 systems. The West German company sees **the worldwide annual demand for video cassettes rising from 88 million units in 1980 to 151 million this year** and to about 360 million in 1983.

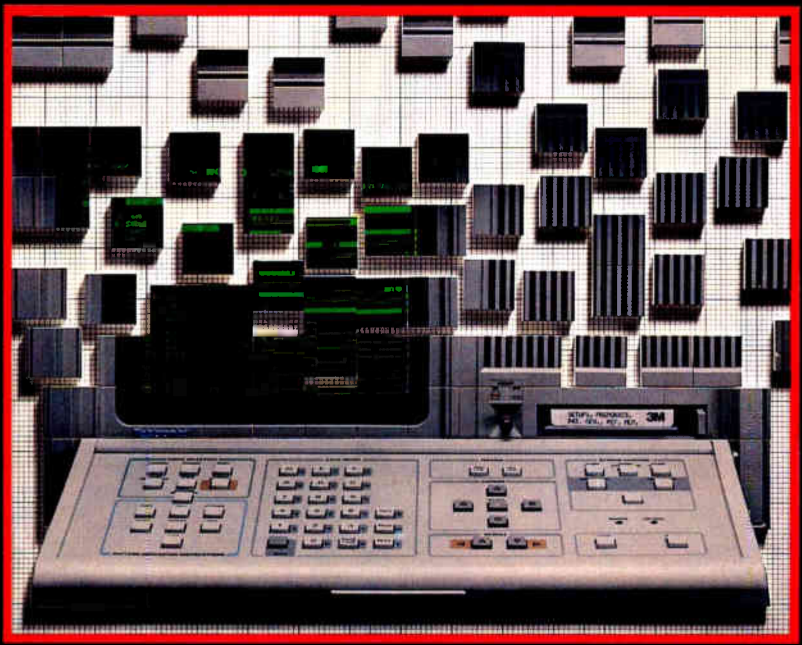
Bipolar gate array uses little power

High speed at low power is attained by a Fujitsu Ltd. low-power Schottky TTL array of 2,000 gates by the use of a 2.3-V as well as a 5-V power supply. Gates operating at the lower voltage have a **power dissipation of only 0.65 mW regardless of fanout.** Average propagation delay for a gate driving a load of 0.7 pF and three to five other gates is 1.5 ns.

CII-HB computers to be sold in U. S.

In what nationalization candidate CII-Honeywell Bull of Paris sees as a hopeful sign that technological and commercial links between it and Honeywell Inc. will continue even if CII-HB is nationalized, Honeywell will **market CII-HB's medium-range DPS7 line in the U. S.** by the end of this year. CII-HB is also expanding the line with two new lower-range models, the DPS7/35 and the DPS7/45, which each offer up to 3 and 4 megabytes of main memory plus 10 megabytes of disk memory. The entire DPS7 line will continue to be made at the company's Angers plant.

Tektronix introduces 132 state of the art logic analyzers,



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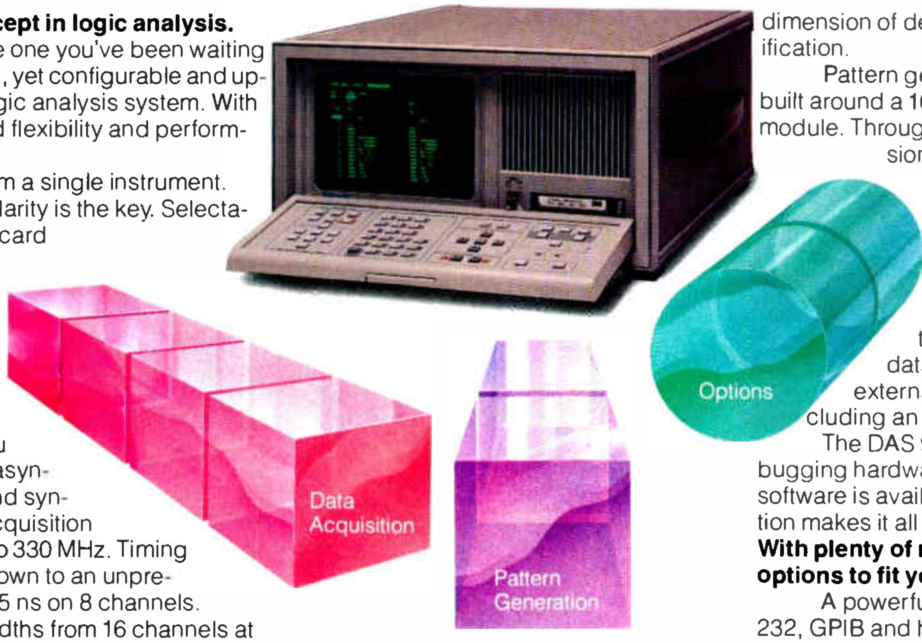

A new concept in logic analysis.

It's the one you've been waiting for. A unified, yet configurable and upgradable logic analysis system. With unparalleled flexibility and performance.

All from a single instrument.

Modularity is the key. Selectable, plug-in card modules and a powerful mainframe let you tailor the exact logic analyzer you need. With asynchronous and synchronous acquisition speeds up to 330 MHz. Timing resolution down to an unprecedented 1.5 ns on 8 channels. And data widths from 16 channels at 330 MHz, to 104 channels at 25 MHz.

But that's not all, because now you can also *link pattern generation with data acquisition.* A powerful combination never before available in a single instrument. One that makes debugging digital systems far simpler than previously possible. Pattern generation provides stimulus data widths up to 80 channels at 25 MHz.

Need I/O capability? There's an option that adds RS-232, GPIB and hard copy interface. And another for a built-in DC-100 magnetic tape drive system.

Select your own width and speed combination, for data acquisition.

DAS 9100 gives you four different data acquisition modules to use as building blocks. Each has its own data width and maximum speed: 32 channels at 25 MHz; 8 channels at 100 MHz with glitch memory; and two modules with 4 channels at 330 MHz. Modules can be combined to give you the performance you need.

Need to go faster? The four channel modules also operate in a two channel mode, with timing resolution to 1.5 ns. All modules can operate either synchronously or asynchronously at full system speed. And the 32 channel module can be used to arm the trigger on those with higher acquisition rates. Plus *modules can be added or changed, as your needs change.*

To back it all up, there's powerful triggering, programmable reference memory and multiple clocks. *Plus glitch triggering,* with a separate glitch memory for unambiguous glitch detection, and our unique, new "arms mode" allows timing correlation between synchronous and asynchronous data.

DAS 9100 integrates the power of pattern generation with data acquisition.

At last, you can have a tool that covers your digital system debugging needs. By combining pattern generation and data acquisition modules, you can stimulate your prototype while simultaneously analyzing its operation. Allowing you to enter a whole new dimension of design analysis and verification.

Pattern generation capability is built around a 16 channel, 25 MHz module. Through additional expansion modules, you can raise the total to 80 channels while maintaining full system speed. The pattern generator allows interaction with the prototype through data strobe outputs and external control inputs, including an interrupt line.

The DAS 9100 lets you start debugging hardware even before your software is available. Pattern generation makes it all possible.

With plenty of room for mainframe options to fit your application.

A powerful I/O option adds RS-232, GPIB and hard copy interface for *full remote programmability.* A built-in magnetic tape drive using DC-100 cartridges is also available, so you can save whole or partial instrument setups for recall.

DAS 9100's easy-to-use keyboard and menus tie it all together.

Operation of your DAS 9100 is simple and straightforward. Selectable menus help you set up trigger conditions, select data formats and define voltage thresholds. You can even define your own mnemonics to fit the data under test.

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SPECIFICATIONS

DAS 9100 Summary

Modules Available

Data Acquisition Modules:
91A32, 91A08, 91A04, 91AE04 Expander
Pattern Generation Modules:
91P16, 91P32 Expander

DAS 9109 Mainframe

Includes 9" CRT, keyboard, controller, one modular power supply, trigger-timebase, space for six add-on card modules

Options Available:

Opt. 1 Tape Drive, for DC100 tape cartridges
Opt. 2 RS232, GPIB and hard copy interface,
Opt. 3 Additional Power Supply
Opt. 4 Two additional Power Supplies
Opt. 5 Rackmount Hardware

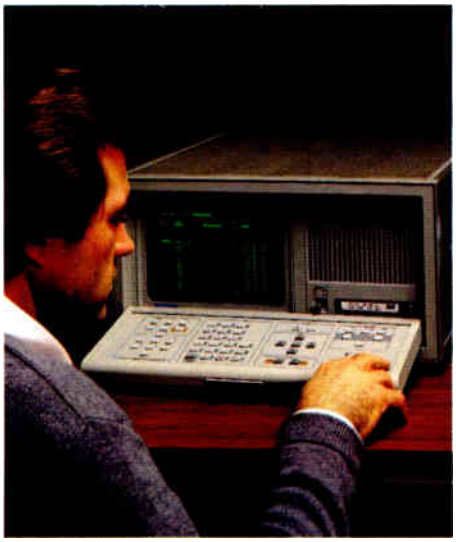
DATA Acquisition Summary

State Table Display

- HEX, Binary, Octal
- User Definable mnemonics
- Search mode
- Multi-speed time aligned data
- Reference memory with editing
- Reference memory compare with data masking and programmable compare window

Timing Diagram Display

- 16 channels simultaneous display
- Programmable selection of channels displayed
- 16 user defineable trace labels
- Horizontal magnification, 1x to 10,000x
- Cursor position & decode
- Multi-speed time aligned data
- Glitch display
- Search mode
- Memory display window



Acquisition Modules

Characteristic	*91A32	91A08	91A04 & 91AE04 Full Channel Mode	91A04 & 91AE04 High Resolution Mode
Number of Channels per Module	32	8	4	2
Resolution/ Clock Freq.	40 ns/25 MHz	10 ns/100 MHz	3 ns/330 MHz	1.5 ns/330 MHz
Modules Per System	3	4	1	3
Channels Per System	96	32	16	8
Memory Depth	512	512	2048	4096
Triggering	**nA→B ≠C	1 level plus arms mode	1 level plus arms mode	
Multiple Clocks	3	With 91A32	With 91A32	
Synchronous	Yes	Yes	Yes	No
Asynchronous	Yes	Yes	Yes	
Glitch Triggering	No	Yes	1.5 nanosecond resolution sampling	
Qualifiers Per Board	2	1	0	
Set-up Times Hold Times	29 ns/0 ns	9 ns/0 ns	2 ns/0 ns	
Number of Probes	4	1	1	

*Data and clock thresholds selected independently
**Any number of occurrences of word A, followed by various logical combinations of word B, reset if word C occurs.
Note: The 91A04 is a master card, channel expansion requires one or more 91AE04s.

DAS 9100 Pattern Generator Major Capabilities

Instruction Steps	254
Instruction Set	Count, Repeat Hold, Go To, Call, Return, Halt
Word Width	16, 48, 80 channels
Max Clock Speed	25 MHz
Programmable Radix	Yes Bin, Oct, Hex
Single Step Mode	Yes
Labels	Yes 32
Subroutine Nesting	Yes 16 Deep
Looping	Yes
Independently Programmable Strobes	Yes 2, 6, or 10
Bus Simulation Capability	Yes
User Definable Output Swings	Yes
Output Types	Patterns, Strobes (1 per probe) Clock
Tri-State Outputs	Yes
Hold Output	Yes
External Interupt	Yes
Internal or External Clock	Yes
Store Program on Mag. Tape	Yes
External Control	Yes

Options Summary

Option 1 DC-100 Tape Drive

- Stores 6 full instrument set-ups or 30 different reference memory patterns
- Directory Space for 32 files

Option 2 RS232, GPIB and Hard Copy Interface

RS232

- Selectable Baud Rates: 300, 600, 1200, 2400, 4800, 9600
- Master/Slave Operation, Full Duplex, Asynchronous

GPIB

- Talker/Listener Only
- Selectable Address
- Selectable Controller Type, EOI or (LF or EOI)

Composite Video Output

- Hardcopy Interface
- Video Monitor Interface

Other Characteristics

- Overall Dimensions — Length-23.5 in./ 59.7 cm, Width-17 in/43.2 cm, Height-9.5 in./24.1 cm.
- Weight — without accessories, 48 pounds/ 105.8 KG
- Voltage Input —
  LO LINE-90 V to 132 V rms
  HI LINE-180 V to 264 V rms
- Line Frequency — 48 to 63 Hz
- Power — 1000 VA, Maximum
- Temperature Range
  Operating 0°C to +50°C (+32° to +122°F)
  Storage −40°C to +65°C (−40° to +149°F)
- Altitude
  Operating — 10,000 ft, maximum
  Storage — 50,000 ft, maximum

DAS 9100 System Configurations

	DAS 9101	DAS 9102	DAS 9103	DAS 9104
Modules Included:				
91A32		1	1	2
91A08	2		1	2
91P16		1	1	1
Options Included			3	1, 4
Total Acquisition Channels:	16	32	40	80
At 100 MHz:	16		8	16
Total Pattern Generation Channels		16	16	16
Available Slots for future expansion	4	4	3	1

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57AX-4832 8/81

Highly mobile electrons make GaAs circuit the fastest chip yet

by Charles Cohen, Tokyo bureau manager

When operated at 77 K, a 27-stage oscillator from Fujitsu is said to near Josephson-junction speeds

The first integrated circuit based on high-electron-mobility transistors has set new records for semiconductor device performance. Researchers at Japan's Fujitsu Laboratories Ltd. say that a 27-stage ring oscillator with enhancement-mode switching transistors and depletion-mode load transistors shows a propagation delay per stage of only 17.1 picoseconds when operated at liquid nitrogen temperature of 77 K. They claim that this exceeds the speed of any other gallium arsenide device and all silicon devices and is close to the 13-ps figure reported for Josephson-junction logic. The company is a subsidiary of Fujitsu Ltd.

The experimental circuit operates from a 1-volt power supply and uses 0.96 milliwatt per stage, thus achieving a delay-power product of only 16.4 femtojoules. But this is only a beginning, because the switching transistor's gate length and source-to-drain spacing are 1.7 and 6 micrometers respectively, about double the dimensions of high-speed gallium arsenide devices built by others.

The present devices have an electron mobility of 20,000 square centimeters per volt-second. But Hajime Ishikawa, manager of the Fujitsu subsidiary's semiconductor device laboratory, says that in HEMT devices built with 1-μm gates and operated at liquid nitrogen temperatures, the electrons should be about three times as mobile because they will collide less often with the crystal lattice or with ions. His prediction assumes both the shorter electron path of short-channel devices and a better quality of crystal in future devices.

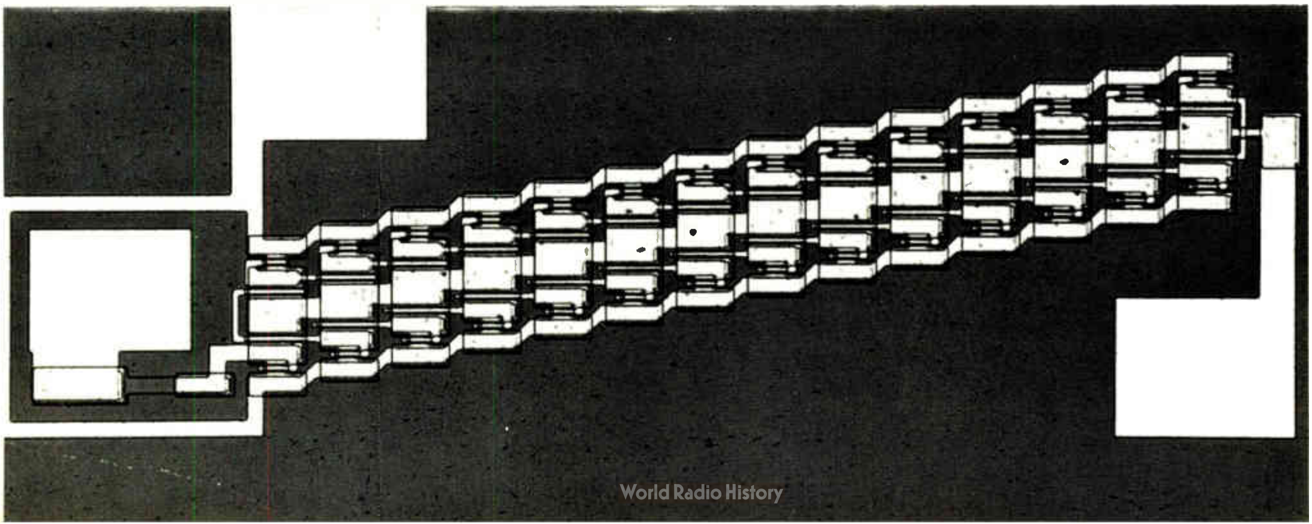
He deduces that such devices will have a switching propagation delay of less than 10 ps when consuming about 100 micro-watts per stage. A power level as low as this would make this ultrafast device suitable for very large-scale integration.

The nearest competition comes from normally-off GaAs field-effect transistors with resistance loads that were built last year by researchers at the Musashino Electrical Communication Laboratory of the Nippon Telegraph & Telephone Public Corp. These achieve a switching speed of 30 ps at room temperature and 17.5 ps at liquid-nitrogen temperature. But the penalty is difficult fabrication and high power consumption—gate length is 0.5 μm, power per stage is 9.2 mw at 77 K.

The HEMT integrated circuit is fabricated on a substrate of semi-insulating GaAs. On this a molecular-beam epitaxial process grows a 0.8-μm-thick layer of extremely pure GaAs, followed by an 0.06-μm-thick layer of silicon-doped n-type gallium aluminum arsenide and a 0.05-μm layer of n-type GaAs. The doping concentration is 2×10^{18} atoms per cubic centimeter.

The n-type GaAs has an insulating film of silicon dioxide deposited on it. Windows in that film make the source and drain regions of the transistors accessible to ohmic contacts made of gold-germanium alloy overlaid with gold metalization. A second SiO_2 insulating layer is deposited and multiple-step lithography per-

Upping the ante. The propagation delay of each of the 27 stages of this oscillator is only 17.1 ps at 77 K, the highest speed yet achieved by any GaAs integrated circuit.



formed to open windows for deposition of a titanium-platinum-gold metalization system for enhancement and depletion FET gates and interconnections.

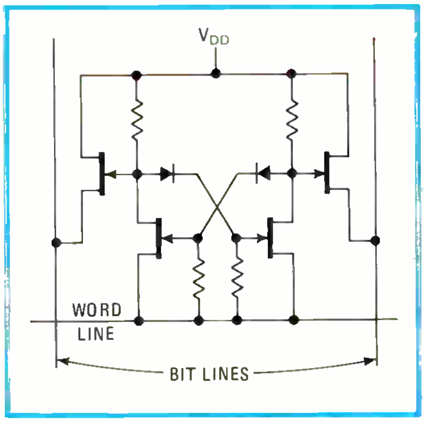
The gates for the depletion transistors are deposited directly through windows onto the n-type GaAs layer. But for the enhancement-type transistors that same layer is etched through and the gates are deposited on the GaAlAs layer. Because Fujitsu's etchant stops at this layer and the thickness of the molecular epitaxy films is precisely controlled, the distance between the enhancement transistor gate and the high-mobility electron layer can also be precisely controlled. The work-function difference between the gate and the GaAs material beneath it creates a depletion layer that extends through to the high-mobility electron layer, which is just below the upper surface of the high-purity GaAs layer, producing as a result an enhancement transistor.

The enhancement-mode transistors in the ring oscillator have the relatively big gate width of 33 μm to minimize the effects of stray capacitance. Load FETs have gates 13 μm wide to give the desired current. Devices with load transistors having 7-μm-wide gates were also fabricated and operated at room temperature. Their switching speed is 56.5 ps and power input 0.46 mW for a supply voltage of 1.1 V.

France

Nanosecond access nears in GaAs RAM

In what is intended as the first step toward the development of a 1,024-bit gallium arsenide random-access memory, Thomson-CSF at its Central Research Laboratory in the Paris suburb of Corbeville has completed work on a fully decoded 8-bit (four 2-bit words) static GaAs RAM with an average access time of 0.6 nanosecond for a total power consumption of 80 milliwatts. An intermediate 256-bit RAM is expected to have a 1.5-ns access time, while the 1-K device could access in less than 2 ns. The circuits are intended to work alongside GaAs arithmetic circuits in future high-speed data processors and will not be silicon-compatible.



Low key. The unusual design of the cell in Thomson-CSF's experimental 8-bit static GaAs RAM will keep charge on the bit lines low and hence access time shorter.

No compromise. "It is not at all in the spirit of our research to worry about compatibility with silicon," explains Gérard Nuzillat, head of the Thomson-CSF group working on GaAs circuit research and design. "Putting a GaAs circuit in a silicon system means that most of the advantage of using GaAs in the first place is lost. Our objective is to create the fastest possible systems, and that means all-GaAs systems."

The RAM was designed using low-pinchoff-voltage field-effect-transistor logic, a Thomson-CSF variation on metal-semiconductor field-effect transistors that optimizes the manufacturing yield of GaAs logic circuits. This approach doubles the tolerance on the threshold voltage compared with the conventional MES FET approach. Even though circuit schematics are slightly more complicated, the flexibility of logic organization is improved.

The circuit consists of 170 components, of which 77 are MES FETs. These transistors are of the quasi-normally-off type with a threshold voltage between −0.2 and +0.2 volts; their gate is 0.8 micrometer long and at least 20 μm wide. The memory cells, which occupy 5,900 square micrometers each, are of an original design unique to Thomson.

Each cell consists of two transistors, four resistors, and two Schottky diodes. A logic swing of 1 V at cell level ensures its immunity to noise. With a transistor width of 20 μm and a power supply of 4.6 V, the normal power consumption of the memory point is a hefty 1.6 milliwatts, though this will be reduced to 0.45 mW for the 1-K RAM because of its 5-μm FET geometry.

Another novelty is the connection of the bit lines, achieved by transfer FETs that share a drain. Moreover, the diode connections enable cell sensing with very little current extraction but with a current gain for cell writing.

Though this type of access makes little difference for a test circuit of only 8 bits, it should present a significant advantage in more complex circuits, where the charge on the bit lines represents an essential portion of the access time.

Methods. The circuit resides on a 0.5-square-millimeter vapor-phase-epitaxy chip and has an active surface of 0.2 mm^2. It is based on recessed-gate technology and the processes used in its fabrication are electron-beam masking, ion milling, and fast chemical etching, the latter to remove no more than 50 angstroms. The gates are made of titanium, platinum, and gold.

"We have just started development of the 256-bit RAM and hope to finish it by mid-1983," says Nuzillat. "Then, if we have no unexpected surprises, the 1-K RAM should not take much more than an additional six months to complete."

The 8-bit test RAM will be presented at the Third Gallium Arsenide Circuit Symposium in San Diego next week. **-Robert T. Gallagher**

Great Britain

Cheap chip-carrier is moisture-proof

A chip-carrier that uses neither ceramic nor premolded plastic spells a major advance in interconnection

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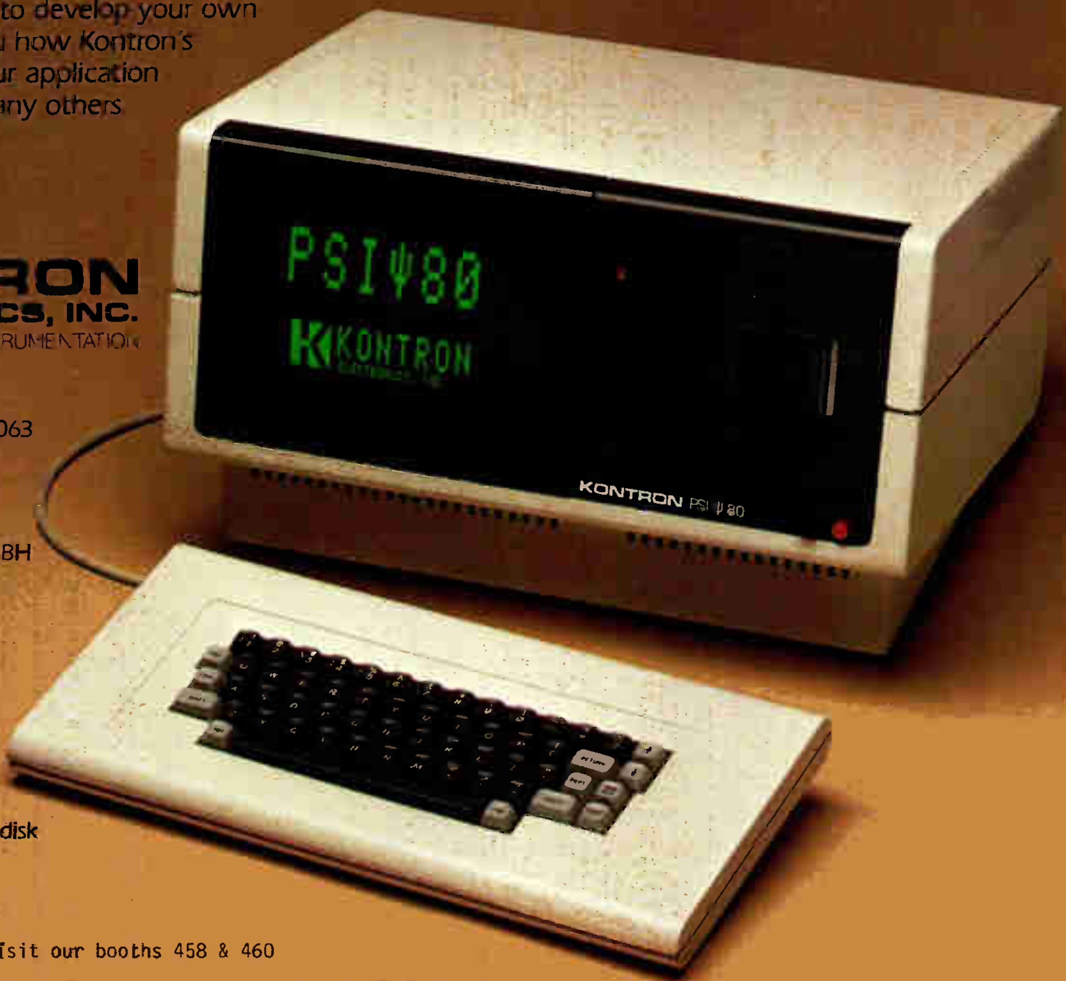

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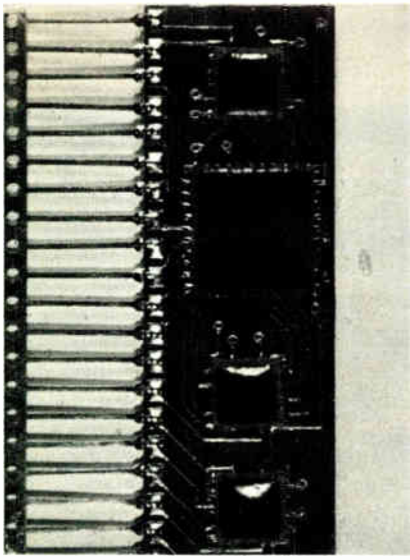


Variety. Chip packages made of pc board and plastic are shown attached to a pc substrate whose edge-mounted fingers may be soldered to a conventional pc board.

technology, one that British manufacturers of telecommunications equipment from System X exchanges to terminal equipment are counting on to reestablish a competitive edge in world markets.

Little larger than the microcircuit chip it contains, the inexpensive package snuggles up closely to its neighbors with hybrid-circuit-like densities and can be precisely placed on cheap printed-circuit boards by fully automatic equipment. Yet it seems likely to meet British Telecom's most stringent reliability standards. The technology was developed by British Telecom's Martlesham Research Centre in collaboration with Tectonic Electronics Ltd., a Swindon-based company with printed-circuit-board, chip-packaging, and hybrid divisions.

The chip-carriers are fabricated in small batches from a 2-inch-square two-layer pc board that can be processed on Tectonic's fully automatic hybrid production line (see "UK firm automates hybrid manufacture," right). The top layer, in which windows have been cut, forms the chip-carrier walls, while the bottom layer carries the pc-board tracks to which the chips are wire-bonded. Plated through-holes transfer tracks from the inner to the outer surface. A diamond saw scribes the double-layer pc board into individual devices. Once mounted and wire-bonded, the chips are then given a proprietary two-layer plastic encapsulation.

Flexible. "We can make flat packs in all Jedec and SOT sizes and even run off a custom special for as little as $600 to $800," says Philip Cook, Tectonic's managing director. "Track patterns down to 0.5 mil can be achieved, and there's no need for solder bumps. Moreover, in large production volumes, 18-way carriers can be produced for as little as 12 or 14 cents apiece."

Unlike bare chips, those in the carrier can be fully tested before being mounted. Moreover, the carriers can be readily positioned and reflow-soldered by fully automatic assembly equipment. As the solder liquefies, its surface tension aligns the through-hole pads with the underlying tracks.

However, the interconnection philosophy does not stop there. The new carrier, explains Cook, can be mounted on a similar pc-board substrate with other surface-mounted components, such as chip resistors and capacitors or miniature SO and flat-pack devices. Because the carrier and substrate are manufactured from the same material, temperature-induced stresses are no longer a problem. Edge-mounted fingers connect the substrate to the conventional mother board.

The pc-board chip-carrier and substrate combination, like many good ideas, seems obvious with hindsight. In the U. S., in fact, General Instrument Corp. did try something similar—its Minipak, in which a blob of epoxy overlaid a chip mounted on a small piece of pc board [*Electronics*, March 17, 1977, p. 86].

The British package, however, is moisture-proof. Test vehicles have been successfully subjected to 110°C and 90% relative humidity over-

UK firm automates hybrid manufacture

A major $6 million investment in highly automated hybrid production lines by Tectonic Electronics Ltd. underpins the interconnection technology it developed jointly with British Telecom. When all eight lines are installed and working some time in 1985, the 5,000-square-foot production unit—reminiscent of a wafer-fabrication facility—will be producing around 45 million hybrid circuits per annum with a minimal staff of around 150 to 180.

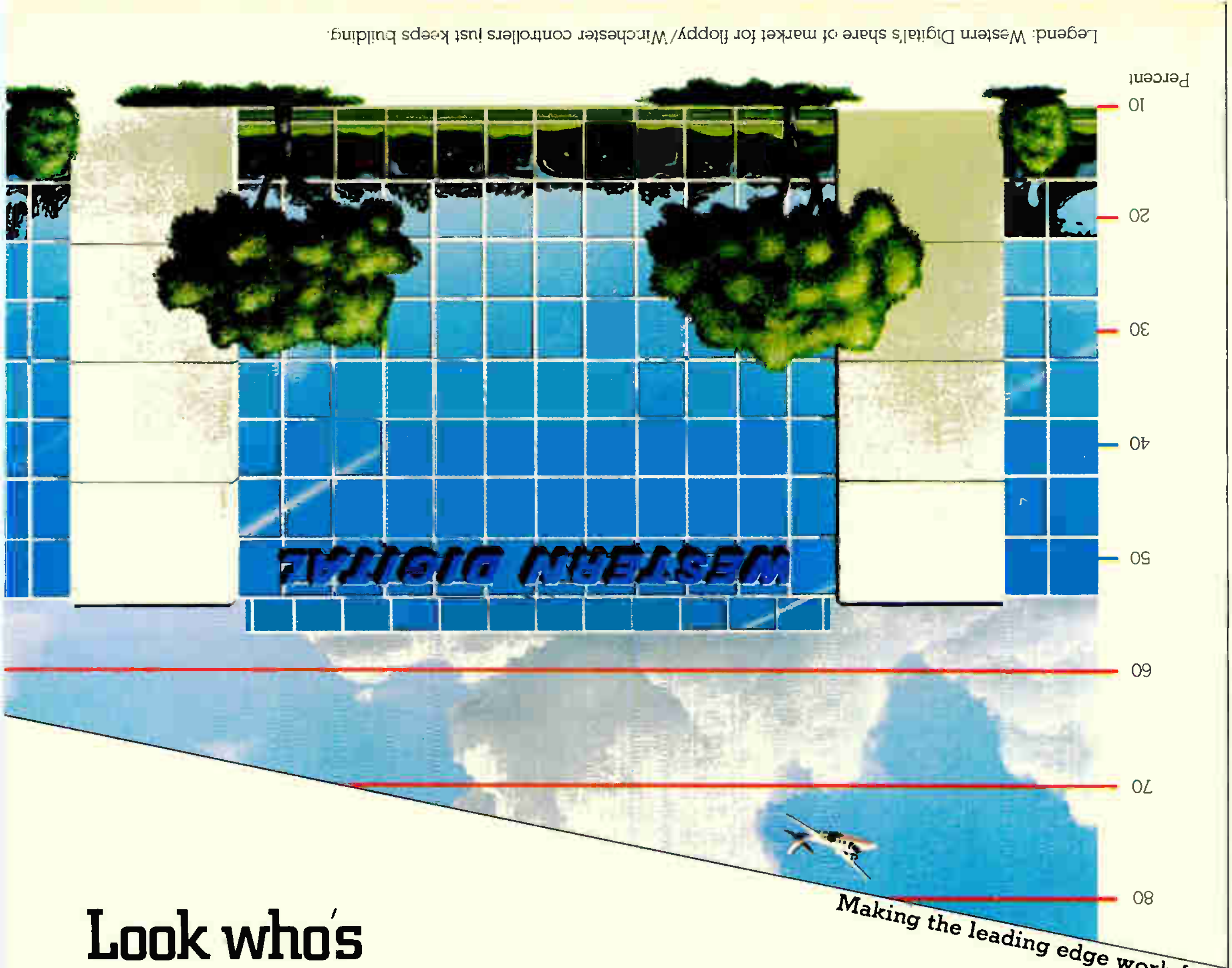
Every stage of manufacture has been automated. The substrate handlers, screen printers, and component placement machinery were developed especially for Tectonic by DEK Printing Machines Ltd. in Weymouth, Dorset, with government backing. A first line is now being commissioned and will serve both as a test bed and shop window for the production equipment.

The entire production line is planned around standard 2-inch-square substrates. Carousel magazines, with 50 substrates in each, feed thick-film printers, dryers, laser resistor trimmers, ovens, and so forth, collecting the processed substrates in a continuous automatic operation. The component placer, the last link in this chain, is now being commissioned and should be able to handle around 320 substrates an hour, each with three circuits and six components per circuit.

Similarly, the laser trimmers used to bring thick-film networks to within tolerance will handle 350 substrates per hour, typically with three circuits per substrate and 14 resistors per circuit.

Carousels are based on the well-proven 35-millimeter film-slide carousel and can handle wet and dry substrates as well as substrates with components attached. Because of these handling methods and the protection they give, yield is exceptionally high. For example, at the print stage it is usually well over 90%, says Richard Hunt, marketing manager for DEK Printing Machines Ltd. Registration accuracy is better than ±25 micrometers at handling speeds of 1,200 substrates per hour. For manufacturers who need to handle larger substrates than 2 in.^{2}, Hunt's firm is developing what are called walking-beam substrate handlers.

-Kevin Smith



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Circle 77 on reader service card

development, an ICL dual has around 1.8 the performance of a single unit. A stopgap machine, to be introduced in November, the 2.2-MIPS 2988 will in dual form have a 3.5-MIPS data rate. In fact, says Dace, ICL plans to take the concept further as it has in the works a 50-megabit-per-second local network that could run up to eight processors in parallel.

Right now, though, ICL is nowhere in the large mainframe 5-to-15-MIPS bracket, a market dominated by IBM. So to penetrate this market and satisfy government requirements for a big mainframe manufacturer, ICL plans to market Fujitsu's Facom 380 in single and dual forms. The strategy, says Wilmot, will plug a huge cash drain, diverting development funds toward the more rapidly growing market in small microprocessor-based systems with a networking capability.

Net plans. Here ICL has recently penned an agreement with Three Rivers Computer Corp. of the U. S. for its PERQ 16-bit graphics-oriented minicomputer work station with an Ethernet network interface. ICL plans to move the product both up and down market, and an LSI version selling for $10,000 (compared with $25,000 at present) is planned. In a further development of its networking strategy, the British company also introduced a multimicroprocessor family developed at its Utica, N. Y., facility, called DRS.

DRS uses a 1-Mb/s local network called Microlan, one of three local networks ICL will use to tie together its products. For 10-Mb/s rates, Ethernet and perhaps the Cambridge ring will be adopted, while for its mainframes, ICL is developing the 50-Mb/s Macrolan. For wide-area networks, ICL is already committed to X.25, and under Wilmot's unfolding strategy, more of its products will also support the Systems Network Architecture protocol, talking to IBM mainframes. Yet further collaborative deals are in the pipeline, taking ICL into personal computers and communications. But one thing is for sure: any new ICL products must feature a networking capability. **-Kevin Smith**

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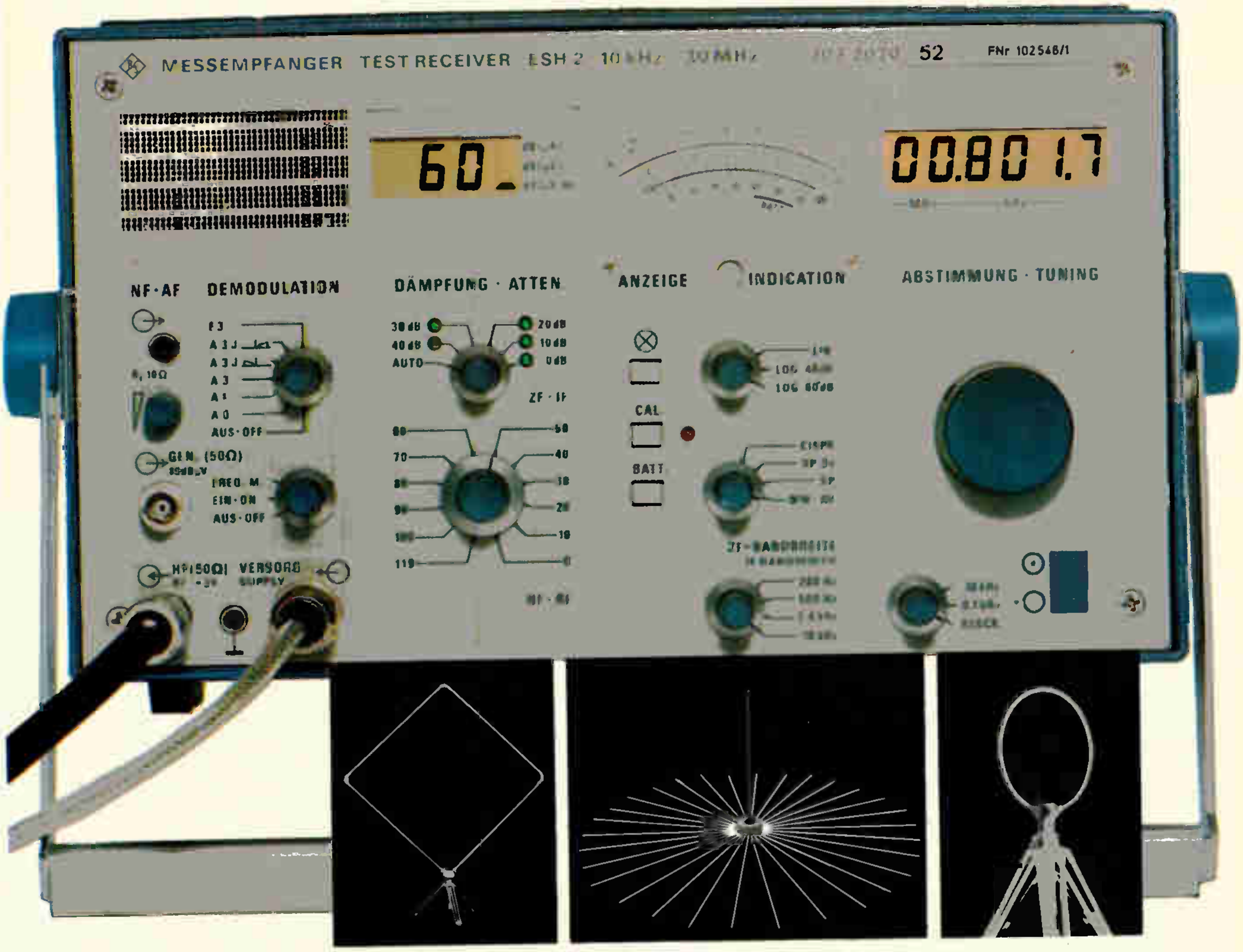

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10 kHz to 150 kHz (left)
10 kHz to 30 MHz (centre, right)

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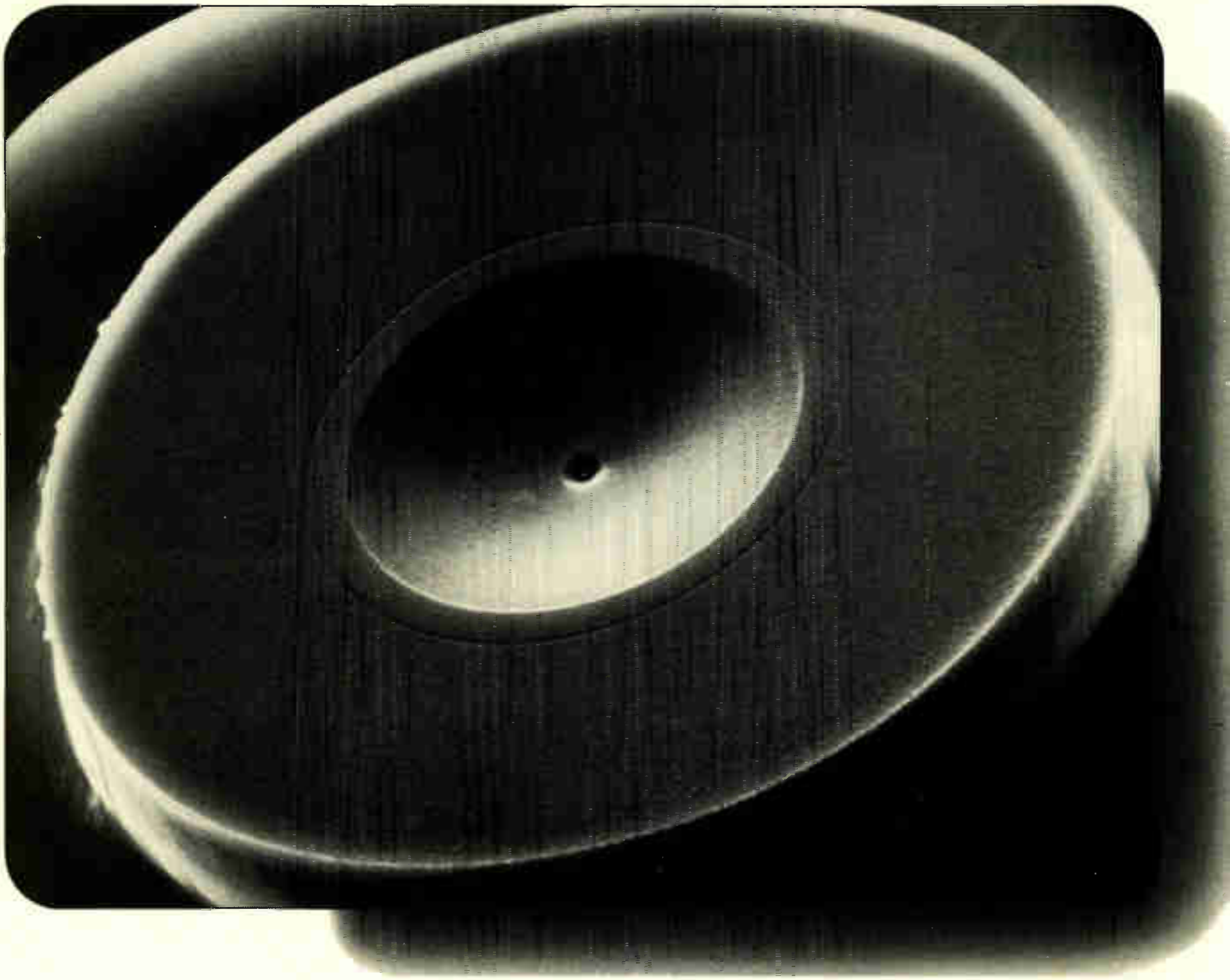
Meeting heavy demands for lightwave transmission

The promise that emerging lightwave communications technology offered just a few short years ago is about to be fulfilled as telecommunications authorities the world over upgrade or expand their networks with optical fibre systems. And Philips technology has contributed much to this state-of-the-art.

For example, Philips originated and developed the plasma-activated chemical vapour deposition (PCVD) method of manufacturing high quality fibre possessing a refractive index profile closely approximating the theoretically desired parabolic form.

Unlike other CVD methods, PCVD employs a non-isothermal microwave plasma to stimulate low-temperature reaction of the gases $SiCl_4$, and $GeCl_4$ and O_2 within a tube of pure silica glass. The plasma reaction zone is produced by a microwave resonator that passes to-and-fro along the entire length of the tube, a very even and thin layer of oxides being deposited at each pass. In this way many hundreds of layers can be deposited to achieve a graded index fibre profile that



An enlargement of the etched surface of an optical graded index fibre 50/125μ for core/cladding diameter.

PHILIPS

ery closely resembles the ideal parabola.

Exceptionally high bandwidth measurements are btained on continuous production runs of these ibres, typically 900MHz per kilometer at 850nm wave-ength, with a lowest value of approximately 600 MHz.Km, and a top value of 1200-1300 MHz.Km.

Philips also achieved a major breakthrough in he complex PCVD manufacturing process by speed-ng up deposition of the layers without any loss in fibre uality. Instead of the standard deposition speed of 0.2 gramme/ minute, new techniques enable speeds up to one gramme/ minute to be reached, thus reducing the time taken to prepare a preform for one kilometer of optical fibre from 25 minutes to only five minutes.

Increasing optical fibre quality at lower production costs is one of the many ways in which Philips technology is helping the communications industry meet the heavy demands for lightwave transmission. Here are some more.

Suspended optical fibre cable now rovides a cost-effective solution to the roblems of television and FM radio eception in mountainous regions. A six-ore optical fibre cable has been suspend-d on a 2.8 kilometer pole-route to connect he villages of Aste and Beon, in the rench Pyrenees, into the local CATV etwork. One of the first suspended ptical fibre routes in the world, it provi-les the population of this remote area vith FM audio reception and a choice of our colour television channels.

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Light wave telephone transmission. In addition to Philips all digital PRX/D exchanges, the Saudi order includes the integration of 140M/bits optical fibre systems into the existing 2M/bits PCM networks in the Jeddah and Riyadh multi-exchange areas. Six-fibre cables, with a capacity of 1920 calls per fibre, will be used in the repeaterless routes, which total some 45 system kilometers. When completed it will be one of the first operational 140M/bits optical fibre transmission systems in the world. Circle 472 on reader service card

Optical fibre detection. The Philips SEM505 scanning electron microscope employs a unique optical fibre detection system within the specimen chamber. In the backscattered-electron mode, the system achieves the highest possible detection efficiency for highlighting topographic and atomic number contrast. When used for cathodoluminescence detection, a light-gathering lens focuses the signal on the fibre bundle. Light impulses from the detector are routed to photomultiplier/-preamplifier combinations via optical switches. The system provides an exceptionally high degree of flexibility as well as a very fast reaction time. This ensures that TV-rate images can be obtained, even at low accelerating voltages, in all detection modes.

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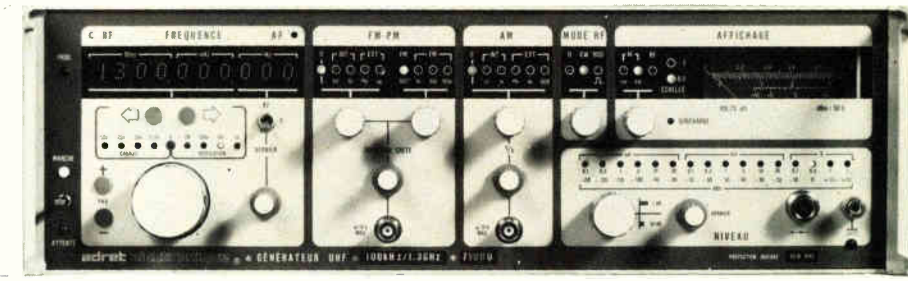

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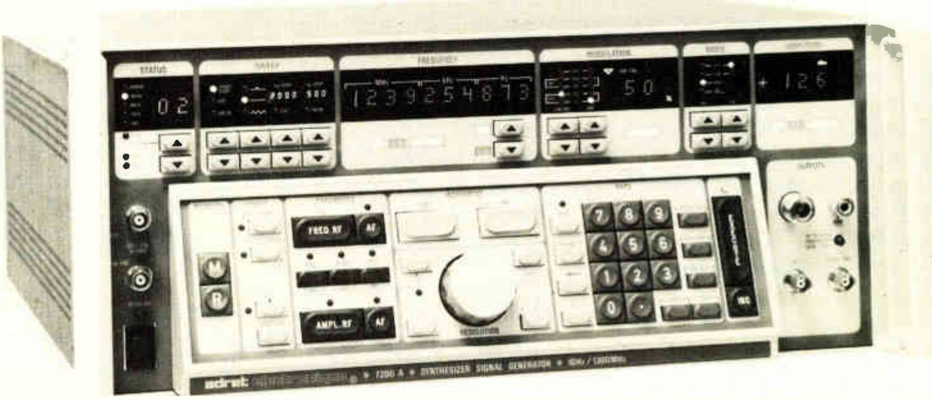

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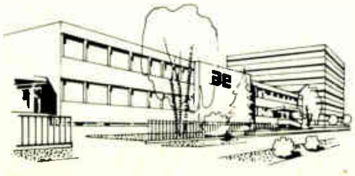

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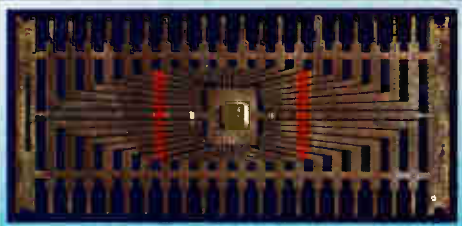
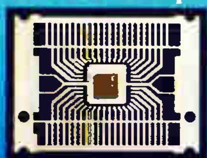
They use the same chips as conventional DILs and power ratings apart, perform in exactly the same way, including reliability. SO packages can therefore go into existing designs easily and quickly. And of course they're ideal for your future designs employing automatic chip mounting techniques.



Conventional 40-pin DIL



40-pin SO package

Both devices are shown actual size. Despite its fine leads, this SO package can be mounted using all soldering methods, including wave and reflow. SO packages reduce PC board real estate, and also give additional design freedom since tracks can be run under the devices.

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Circle 406 on reader service card

Set tests digital phone exchanges despite lost bytes

by John Gosch, Frankfurt bureau manager

PCM generator and receiver check switching equipment under clock-offset conditions that cause omitted bytes

The advent of digital switching techniques, particularly in local and private branch telephone exchanges, has increased the pressure for test equipment that provides information on how such exchanges are operating—for equipment that checks, for example, whether the signals that are applied to the exchange are properly switched or whether the signals suffer in quality on their way through the exchange.

Rising to the occasion is the VM-1 test set from West Germany's Wandel & Goltermann. The compact setup, consisting of a generator and receiver, determines whether the input signal, in the form of a pulse-code–modulation frame containing a channel time slot with a 64-kb/s signal, is switched correctly and whether the signal is impaired by bit or word errors. What's more, the transmission delay between the exchange's input and output can be determined when a reference connection is made between the set's generator and receiver.

The VM-1 provides for separate acquisition of bit or byte errors, byte insertions, and byte omissions or slips encountered by the signals during transmission through the exchange. There is a counter for each error type. Slips are produced by defined shifting of the applied clock. The test set is externally controllable via an interface bus conforming to the International Electrotechnical Commission's 625 standard.

To be sure, digital-exchange test equipment already is available to perform about the same checks as the W&G equipment. But what sets the VM-1 apart from competing instruments is that "measurements are made even under conditions of signal slips," according to Frank Coenning, who heads the firm's PCM and data-measuring equipment division. The VM-1 will be available by December and sell for less than $11,000 on the German market.

The generator produces a complete PCM frame that corresponds to the recommendations of the International Consultative Committee for Telegraphy and Telephony (CCITT). Any of the time slots of a PCM-30 frame can be loaded with a test pattern. The remaining 29 time slots contain a channel-loading pattern. Clock signals can be produced internally, but more usually an external clock from the exchange is used. With external synchronization, a defined positive or negative clock offset can be produced to cause slips.

For testing a digital exchange under real in-service conditions, a regular PCM signal is fed to the generator via an auxiliary unit, the so-called signal-insertion device. This device either switches the PCM frame

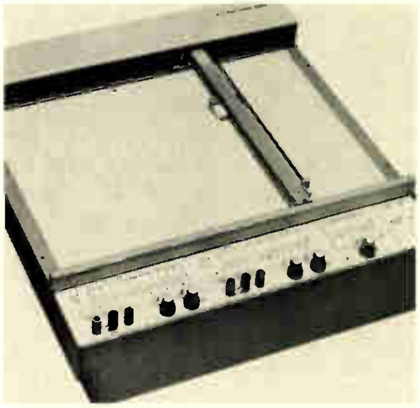
to the input of the exchange or takes the test pattern from the generator and inserts it into an unoccupied time slot. The incoming PCM signal is monitored for correct amplitude and for the alignment status of frames and multiframes.

To identify the origin of a measuring signal appearing at the exchange output, the generator and the channel time slot have a coded number signal that alternates with the test signal. Both signals are transmitted to the receiver for display. To test the frame and multiframe synchronization, identification words can be deliberately distorted.

The receiver synchronizes itself to the PCM frame coming from the unit under test. Monitors display information on the frame or multiframe alignment status and on the received measuring signals. Shown are either the measured results for the selected time slot or the identification signal produced at the generator.

The receiver evaluates the number of erroneously received bits or bytes, either taking into account or disregarding the slips. Also determined are the presence or absence of bytes resulting from the slips. For error counting, the receiver provides for a preselectable time interval within which a single or repetitive count of errors can be implemented.

Wandel & Goltermann, P. O. Box 45, D-7412 Eningen, West Germany [441]



The 3056 X-Y recorder has a slewing speed of more than 100 cm/s, a Y-axis acceleration of 7,700 cm/s², and sensitivities down to 10 μV/cm. It uses a felt pen for skip-free traces at writing speeds over 120 cm/s. Gould Instruments Division, Roebuck Road, Hainault, Essex 1G6 3UE, England [443]

SIEMENS

SMP: bubble memories on Eurocards

Siemens' SMP microcomputer board system, already claiming a top position technologically, is being further expanded by the new SMP-E140, -E141 and -E142 magnetic-bubble memory series and by the SMP-STR140 software driver.

B 8127.101

Supplied on standardized Eurocards with DIN 41612 connectors, this memory system combines the very simple handling of standard boards with the advantages of new bubble memory technology. Per controller board you can expand memory capacity in steps from 128K to 1 Mbyte.

This bubble memory offers decisive advantages compared to conventional storage media such as floppy disks and cassettes:

- no moving parts, and thus no mechanical wear
- no additional mechanical or set-up requirements
- problem-free implementation, just as with every SMP board
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- unlimited data retention, even without supply voltages
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- error correction.

The memory's high reliability, especially in rough environments, solves specific operating problems – such as in factory systems, refineries, steel or rolling mills – problems that traditional moving storage systems media could solve only with great difficulty, if at all.

Siemens provides extensive support to system users in the forms of powerful systems software, experienced applications engineers and not least through training in our microcomputer schools throughout Europe.

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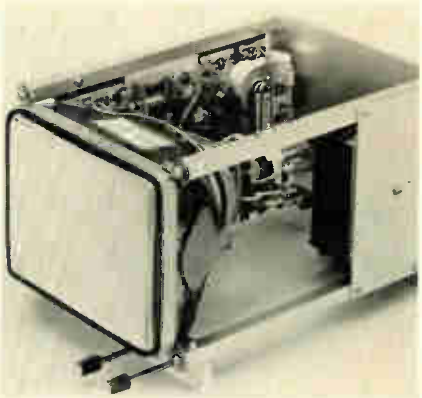
»SMP bubble memory«.

SMP – the microcomputer board system from Siemens

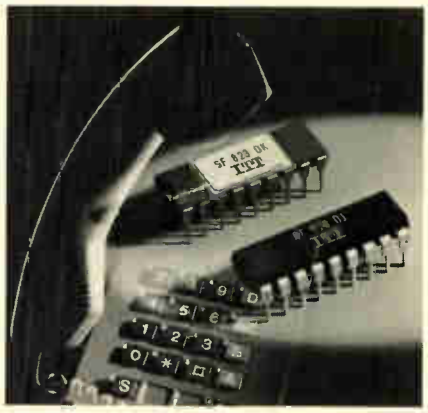
Circle 408 on reader service card

New products international

The PF-2 bit-error-rate measuring set has a clock range from 48 to 8,500 kb/s. Bit rates of 704, 2,048, and 8,448 kb/s are switch-selectable for output from an internal crystal-controlled oscillator. Wandel & Goltermann, P. O. Box 45, D-7412 Eningen, West Germany [442]

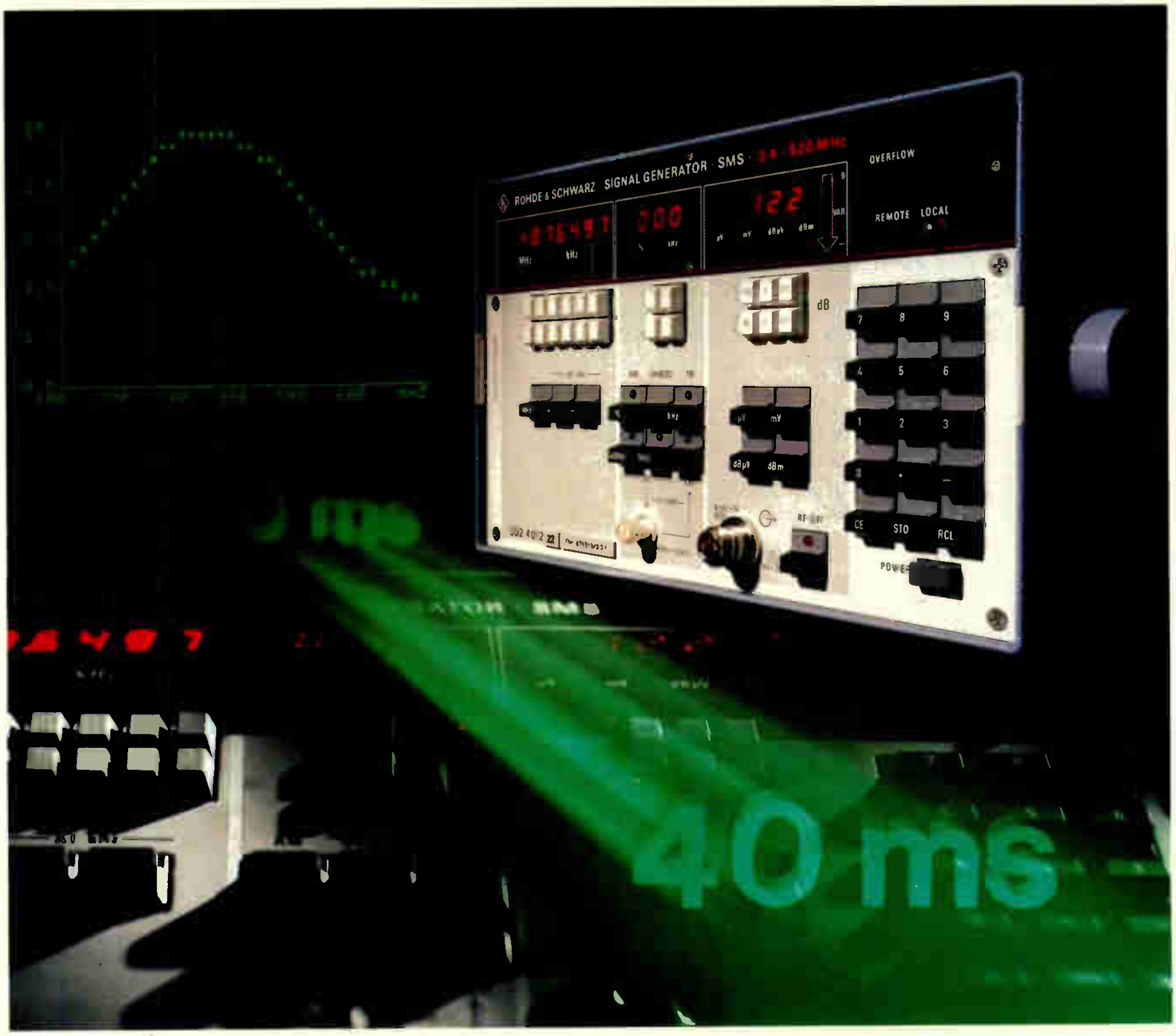


The VM video monitor comes with either a 6- or 7-in. screen. Images can be viewed as light on a dark background or switched to dark on light. It has a 10-MHz bandwidth; deflection is magnetic over a 75° angle. H. Lucius & Baer, Sperlingstr. 1, D-8192 Geretsried 1, West Germany [445]



The DF 820 integrated circuits for repetitive dialing of telephones operate off line power or a 2.5-to-6-V supply. They come in 18-pin plastic or ceramic packages and employ single or double push-button contacts. ITT Intermetall GmbH, P. O. Box 840, D-7800 Freiburg, West Germany [447]

Signal generator SMS
high-speed, IEC-bus-compatible



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The SMS offers you 120 dB/Hz at 20 kHz from the carrier and 145 dB/Hz at 1 MHz, so it's suitable for intermodulation and blocking measurements in line with CEPT.

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The SMS gives you all you want in a general-purpose unit, e.g. high level accuracy, 125 kHz deviation over the **entire** frequency range and only 4 Hz spurious, plus resolution of 100 Hz.

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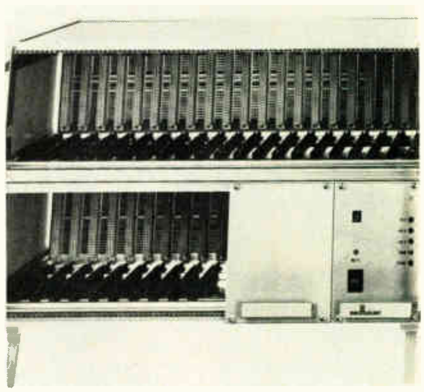
New products international

The MM30 has a 1,024-character memory and a keyboard on its back side. Programmed text can scroll from right to left or top to bottom or flash. Its 16 red light-emitting-diode characters are 3.2 cm high. Text Lite, Zuidermolenweg 27, 1069 CE Amsterdam, The Netherlands [449]



This power supply for microprocessor-based systems is switchable from a 110- to 220-V input at 40 to 60 Hz. It features a power-failure signal, temperature monitoring, protective circuitry, and voltage indication. Sedlbauer GmbH, Quagliostr. 6, D-8000 Munich 90, West Germany [451]

Philips' PM 2521 multimeter takes true root-mean-square measurements to 100 kHz and measures time, frequency (to 10 MHz), and dc voltage, resistance, and temperature relative to a reference. It can read out in decibels. Pye Unicam Ltd., York Street, Cambridge CB1 2PX, England [452]

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Circle 412 on reader service card

New products international

The MX-82 F/T 9-by-9-dot matrix printer has a 96-character ASCII set and eight international character sets for bidirectional printing at 80 characters/s. It offers four printing sizes at a maximum of 159 characters per line. Epson Shinshu Seiki Co., 80 Hiro-oka, Shiojiri, Nagano 380, Japan [453]

The Nanogate electronic high-speed shutter produces exposure times down to 2 ns and has a spectral range of 160 to 900 nm and a dynamic resolution of more than 20 line pairs/mm. The opening point of the shutter is precise to within 1 ns. Proxitronic, D-6108 Weiterstadt, West Germany [455]

The Trackbox-3525 laboratory linear regulated power supply has tracking outputs of 0 to +25 and 0 to −25 V adjustable to within 1% over a 1-A range with a 20-mW resolution and a 4-to-6-V, 3-A output adjustable to a 25-mW resolution. Powerbox AB, Box 159, S-154 00 Gnesta, Sweden [460]

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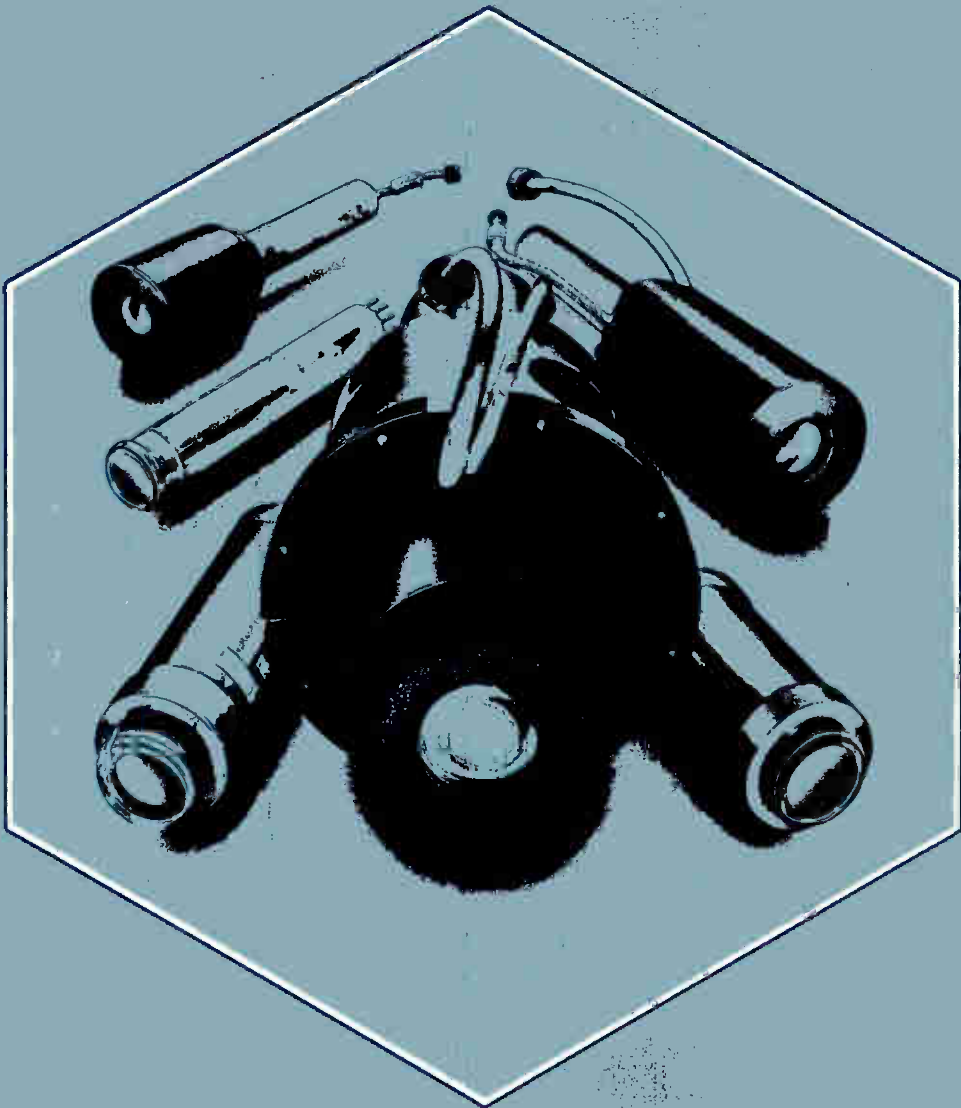

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Tech Tips

FCC Regulates RFI

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On September 18, 1979, the U. S. Federal Communications Commission adopted new regulations to reduce the interference potential of electronic computing equipment (FCC79-555, 14686). These regulations, amending Parts 2 and 15 of the FCC rules, were modified in a Reconsideration Order adopted March 27, 1980 (FCC80-148, 27114). They will be imposed on computing equipment according to the following schedule:

January 1, 1981 —
Class B devices requiring certification (see below) must comply. All other devices must either comply or be labelled with a statement of non-compliance.

October 1, 1981 —
All Class A and Class B devices manufactured for the first time after this date must comply.

October 1, 1983 —
All Class A and Class B devices must comply.

The following definitions and specifications have been excerpted from the FCC publications concerning Docket Number 20780.

DEFINITIONS:

Computing Device. Any electronic device or system that generates and uses timing signals or pulses at a rate in excess of 10 000 pulses (cycles) per second and uses digital techniques; inclusive of telephone equipment that utilizes digital techniques or any device or system that generates and utilizes radio frequency energy for the purpose of performing data processing functions, such as electronic computations, operations, transformations, recording, filing, sorting, storage, retrieval, or transfer. Radio transmitters, receivers, industrial, scientific and medical equipment and any other radio frequency devices which are specifically subject to an emanation requirement elsewhere in this Chapter are excluded from this definition.

Note: *Computer terminals and peripherals (i.e., Input/Output devices for computers) which are intended to be connected to a computer are considered computing devices. All other components or subassemblies (e.g., switching power supplies) of a computing device are not included in this definition.*

Class A Computing Device. A computing device that is marketed for use in a commercial, industrial or business environment; exclusive of a device which is marketed for use by the general public, or which is intended to be used in the home.

Class B Computing Device. A computing device that is marketed for use in a residential environment notwithstanding use in commercial, business and industrial environment. Examples of such devices include, but are not limited to, electronic games, personal computers, calculators, and similar electronic devices that are marketed for use by the general public.

Note: *A manufacturer may also qualify a device intended to be marketed in a commercial, business or industrial environment as a Class B computing device, and in fact is encouraged to do so, provided the device complies with the technical specifications for a Class B computing device. In the event that a particular type of device has been found to repeatedly cause harmful interference to radio communications, the Commission may classify such a computing device as a Class B computing device, regardless of its intended use.*

SPECIFICATIONS:
Conducted RFI will be limited as follows:

Frequency (MHz)	Maximum RF Line Voltage (dB above 1 µV)	
	Class A	Class B
0.45-1.6	60	48
1.6-30	69.5	48

Note: *Conducted limits in the frequency range of 10 to 450 kHz are under consideration.*

METHODS OF MEASUREMENT:
On June 11, 1980, the FCC proposed rules to formalize the methods of measurement and the procedure for verification of computing devices (FCC80-335,27592).

CERTIFICATION and VERIFICATION:
Certification is an equipment authorization issued by the FCC for equipment designed to be operated without individual license under Parts 15 and 18 of its rules, based on representations and test data submitted by the applicant. The following Class B devices require certification:

1. Electronic games, including video coin operated games, but excluding self-contained, hand-held games that do not use a TV receiver for display.
2. Personal computers, excluding desk top and hand-held calculators and digital clocks and watches.
3. Peripherals, terminals, etc. that are capable of being attached to a personal computer.

All other Class B devices and all Class A devices will be subject to verification only. Verification is defined as a procedure where the manufacturer makes measurements or takes the necessary steps to insure that the equipment complies with the appropriate technical standards. Submittal of a sample unit or representative data to the FCC demonstrating compliance is not required unless specifically requested by the FCC.

Class A and Class B devices manufactured after January 1, 1981, but before the date by which they must comply, must either be verified or be labelled as follows:

"This equipment has not been tested to show compliance with new FCC Rules (47 CFR Part 15) designed to limit interference to radio and TV reception. Operation of this equipment in a residential area is likely to cause unacceptable interference to radio communication requiring the operator to take whatever steps are necessary to correct the interference."

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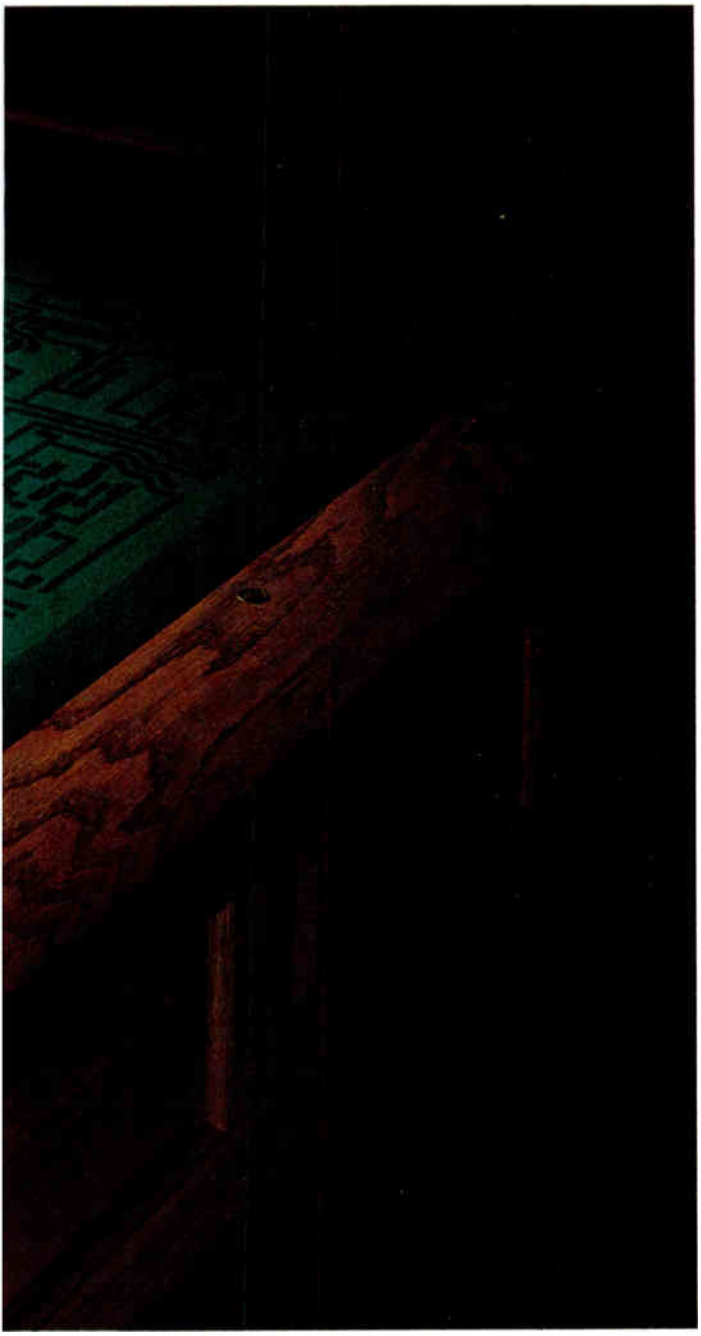

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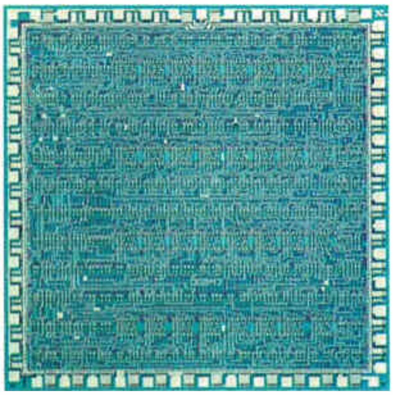

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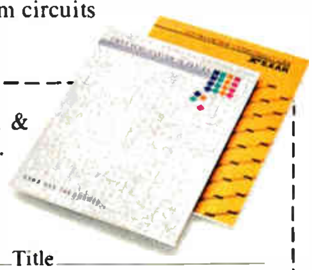

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8021B	•	•	•	•	•	•		•				0.25%
8020B	•	•	•	•	•	•	•	•				0.1%
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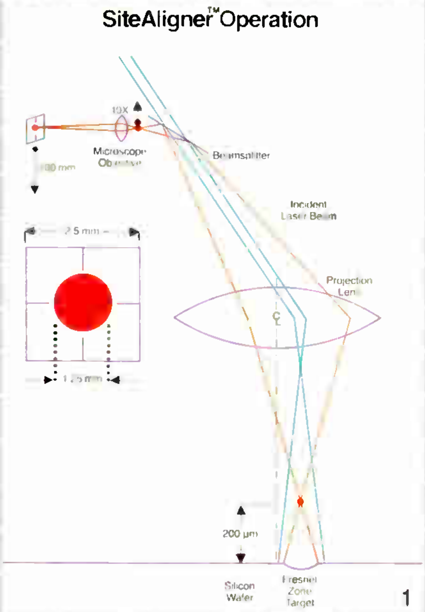

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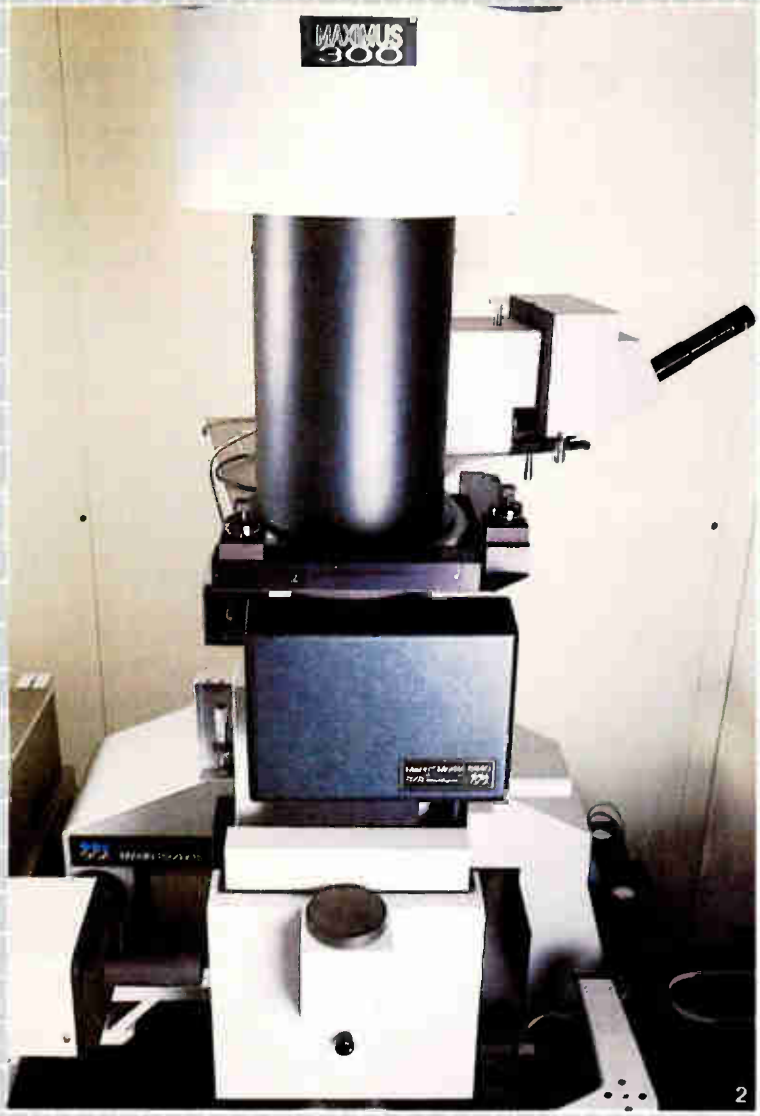

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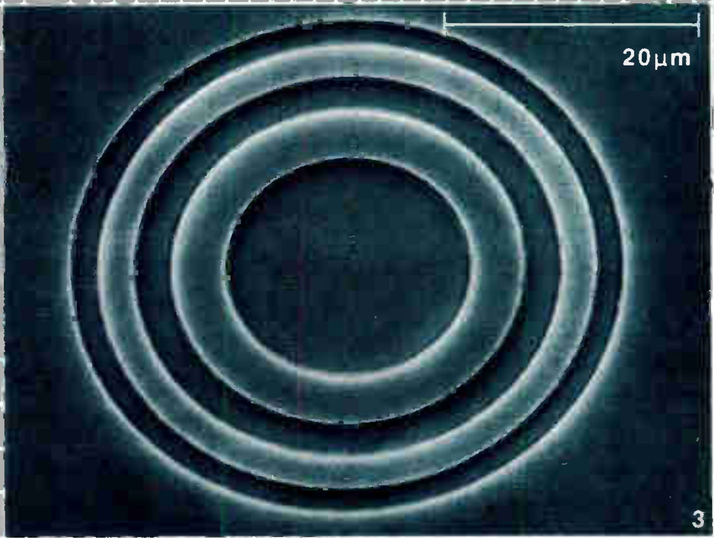

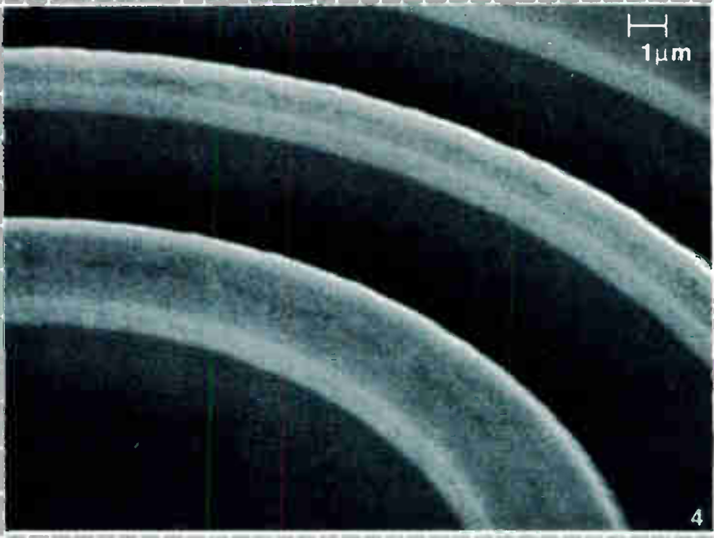

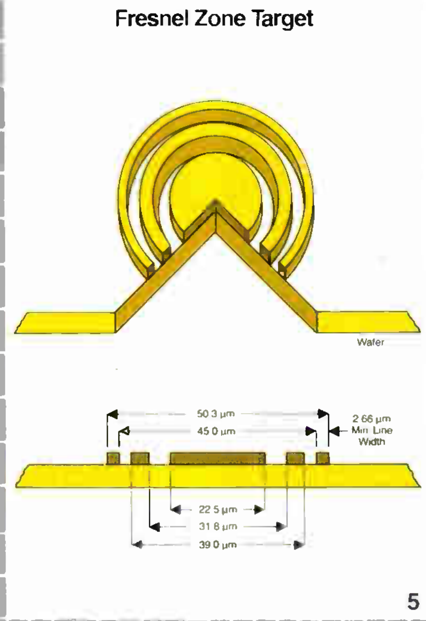

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1. Optical schematic of Mann Model 5840 SXS™ SiteAligner.™

2. SiteAligner mounted on the DSW® Wafer Stepper™ direct step on the wafer system.

3. Scanning Electron Microscope photo of Fresnel Zone Target on wafer (approx. 1600X).

4. Scanning Electron Microscope photo of Fresnel Zone Target on wafer (approx. 3000X).

5. Diagram of the Fresnel Zone Target. The Fresnel Zone Target allows alignment even if a target is damaged.

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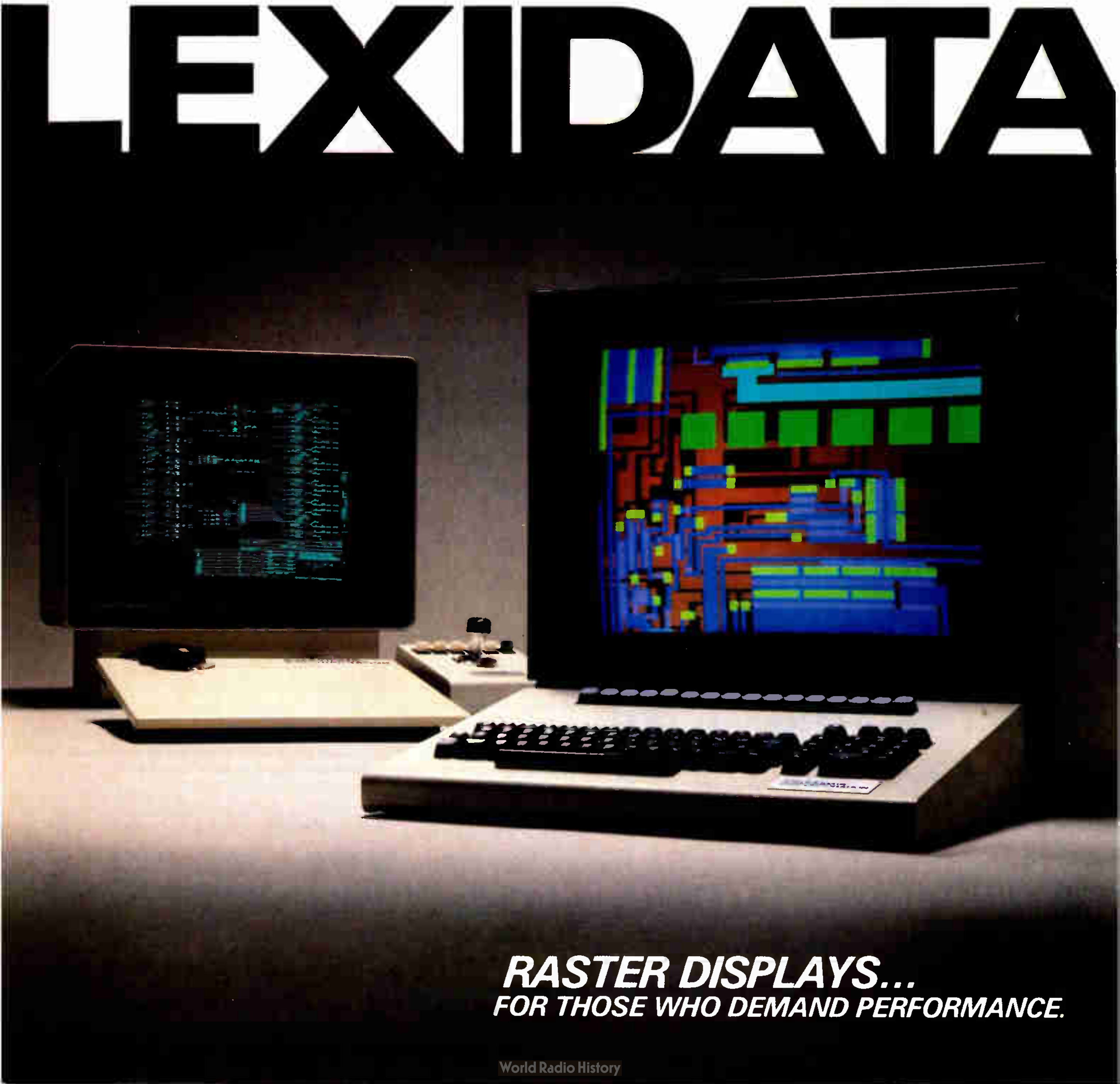


Users want easier tests for VLSI

Problem once again occupies much time at Cherry Hill conference as system test is subject of sessions for first time

by Richard W. Comerford, Test, Measurement & Control Editor, and Jerry Lyman, Packaging & Production Editor

While the blustery winds of late October may chill the air outside Philadelphia's Franklin Plaza next week, the more than 2,000 technologists expected will ensure it will be hot inside the conference sponsored by the Institute of Electrical and Electronics Engineers. The meeting, formally entitled the 1981 International Test Conference/Cherry Hill, is not likely to be any less lively than it has always been during its three days of sessions on Oct. 27, 28, and 29.

What will cause the heat gain is the insistence by users that the next generation of integrated circuits be designed for easy testing, whether alone on boards or in systems. This demand has caused the conference to again devote considerable time to design for testability on chip and on board and to include for the first time sessions on system test.

Two complete sessions with a total of 13 papers represent a significant contribution to the testability effort in very large-scale integration. Looking to be of special interest, the lead paper in session 4, "A Self-Testing Method for Digital Circuits," by M. T. M. Segers of Philips Research Laboratories, Eindhoven, the Netherlands, describes how to adapt the scan-path approach to a self-testing environment. In the scan-path concept, all flip-flops in a circuit are chained together to form a linear shift register.

Today much self-testing is done functionally, as in the case of a microprocessor testing itself. This requires a large design effort for every new construct and has a relatively poor fault coverage. The Philips method makes use of a circuit's structure and is therefore independent of design; it can also reach a wider fault coverage.

Usually, as Segers points out, in straightforward structural self-testing, input testing patterns and corresponding output patterns are stored in two added on-board read-only memories. However, this method requires two specific ROMs for every chip design.

So Segers develops his new concept by replacing the ROM pattern generator with a random-pattern generator whose patterns are fed into the available scan path directly into the combinational circuit. In a second change, the second ROM is replaced by an m-bit feedback register creating a fault signature register. Finally, this circuitry is simplified by using the feedback signal of the shift register as a random input for the scan path of the original circuit as shown in the figure.

In an actual test, the signature of the device under test is compared with a "known good" signature that is obtained either through computer simulation or with a "known good" device's signature. The small amount of control circuitry could be inte-

TEST CONFERENCE SESSIONS

	Tuesday, Oct. 27	Wednesday, Oct. 28	Thursday, Oct. 29
MORNING	SESSION (1) 9:00–11:30 Keynote address and invited panel The challenge of testing VLSI in the 1980's – William Thurston, GenRad, Inc.	SESSION (7) 8:30–12:00 Test equipment and methods (8) 8:30–12:00 Codec testing (9) 8:30–12:00 Design for testability/self-testing (2)	SESSION (13) 8:30–12:00 Test-system architecture (14) 8:30–12:00 System testing in the field (15) 8:30–12:00 Functional testing
AFTERNOON	(2) 1:30–5:15 Microprocessor testing and modeling (3) 1:30–5:15 Memory test (4) 1:30–5:15 Design for testability/self-testing (1)	(10) 1:30–5:15 Board testing (11) 1:30–5:15 Precision measurement, calibration, and testing (12) 1:30–5:15 Test economics	(16) 1:30–5:15 Software (17) 1:30–5:15 System testing in manufacturing (18) 1:30–5:15 Testing, validation, and fault coverage
EVENING	(5) 8:00– Architecture, cost, and performance of next-generation VLSI test systems (6) 8:00– Mostly-good memory devices		

grated with the "original" circuit (IC or printed-circuit board), creating a real self-testing circuit. On the other hand, the control circuitry also could be configured as a simple external tester.

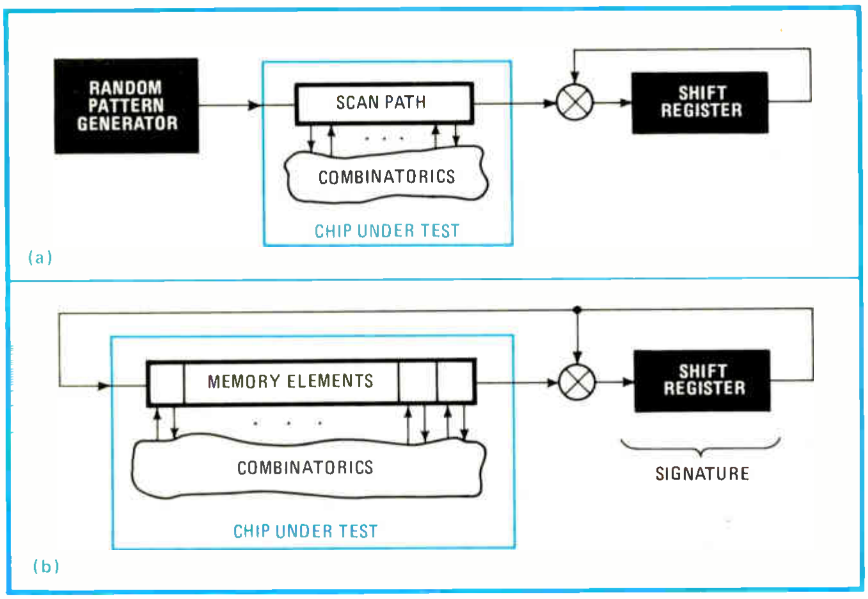
In this method, fault coverage is a function of the number of patterns, the bit length of the feedback register, and the circuit configuration. Segers also reports on test results using this method on an IC with 150 memory elements and 1,000 logic gates. After 250 patterns, fault coverage of this circuit with an 87-bit feedback register produced a result of about 95%. A 4-bit register gave about 85% coverage.

Device Tests. In addition to the two formal sessions on general approaches to design for testability, this topic will be the focus of a panel group in session 3, microprocessor testing and modeling. The session, which will present among other items a unified test plan for LSI or VLSI components using the 8086 processor as a specific example, is chaired by K. Rose of the Rensselaer Polytechnic Institute. Rose points out that "in the past, vendors and users have developed diverging opinions on the need and-or the requirement for a unified test philosophy. This counter-productive trend cannot continue with VLSI designs."

Test strategies for VLSI dynamic RAMs are covered in session 2. One paper in this session deals with the problem of increasing memory-test efficiency, an especially timely topic since test periods have been increasing along with the number of integrated devices.

The authors, D. Pannel and S. Winegarden, discuss their new test pattern, Paragon, which combines with the March test pattern, they say, for "a perfect set of test patterns for assuring logical memory characterization." A new approach to sequence testing, Paragon is a $16N^2$ pattern that not only exercises all possible data and address transitions but also includes all possible pairs of read and write cycles. Another advantage is that it can be easily implemented on most commercial memory test pattern generators.

Differences between pattern generation techniques and the architectures of general purpose VLSI test systems are covered in two sessions, session 5 on Tuesday evening and session 13 on Thursday morning. The evening session should prove essential for anyone considering the purchase of a tester for VLSI, since it pits the representatives of GenRad, Teradyne, Accutest, and others not only against each other but against potential users—the manufacturers will try to defend the new features and software that their systems offer to help speed devices through production test.



Structured. In open-loop structural self-testing (a), a random-pattern generator feeds patterns into the scan path of a combinational circuit. The patterns create a circuit signature in the feedback shift register. In a closed-loop version (b), that register also provides random input to the scan path, eliminating the pattern generator.

Board and system test. Once checked and on boards, VLSI devices will present a new set of problems in test speed and fault isolation for the production department. Those problems and some solutions will be discussed on Wednesday in session 10. Along with papers on the need and techniques for at-speed testing of logic and microprocessor-based boards will be a presentation by S. G. Kochan of Henckels, Haas & Brown Inc. of Saddle River, N. J., about a new algorithm for guided probing on functional testers.

Kochan's paper deals primarily with probe software algorithms but also includes a brief description of the hardware needed for their implementation. In particular, Kochan presents techniques showing how to reduce dramatically the number of points that must be probed to isolate faulty components on bus-structured boards. "These stat-sensitive probing techniques can reduce the number of points to be probed by the operator by a factor of 10 or more," Kochan claims.

Venturing beyond the board for the first time, the conference will consider the needs for system testing, under the direction of Robert E. Anderson, vice president of GenRad Inc. in Phoenix and father of the widely used 2225 functional field tester. Sessions 14 and 17, both scheduled for Thursday, will examine system testing in the field and the factory, respectively.

In session 14, representatives of IBM Corp. and NCR Corp. will unveil portable testers built by their companies for field check of their systems. To introduce the session, J. T. Zender of GenRad will present the driving forces behind the development of what he calls "intelligent, portable System Test and Maintenance (STAM) computers." After the session, chairman Don Cassas of the John Fluke Manufacturing Co., Mountlake Terrace, Wash., and designer of the 9000 series of portable testers, will head a panel on the merits of remote diagnostics, built-in test, and portable systems. □

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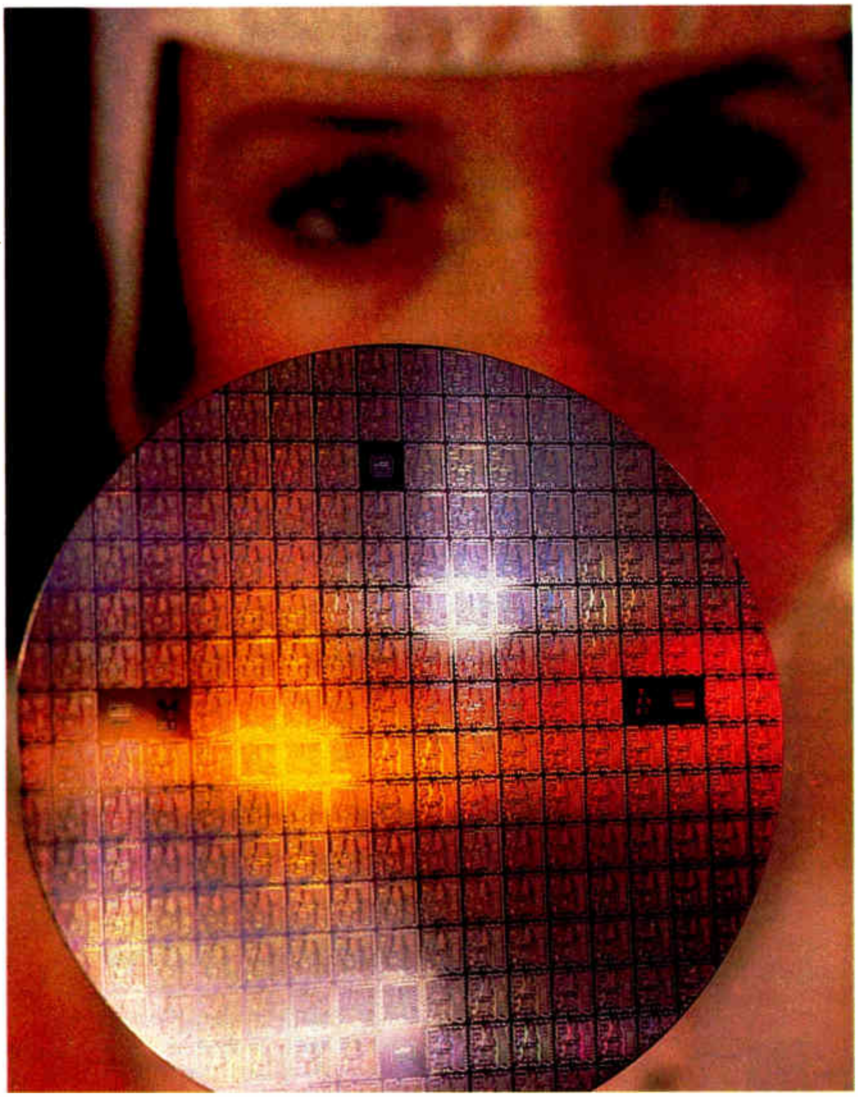

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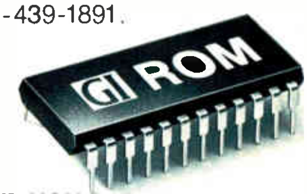

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Components

Gated MOS FETs may boot Schottkys

GE is first with synchronous rectifiers as replacement for Schottky diodes used in low-voltage power supplies

by Roderic Beresford, Components Editor

Switching power supplies—a healthy billion-dollar market that is growing some 20% annually—may soon be using power MOS field-effect transistors for synchronous rectification in their output circuits. Although interest in high-efficiency rectifying circuits is widespread among power supply and device manufacturers, General Electric Co.'s Power Supply operation in Fort Wayne, Ind., appears to have the first entry in this field.

A 300-mil-square power FET developed by Michael S. Adler and coworkers at GE's Corporate Research and Development Center in Schenectady, N. Y., will be discussed at December's International Electron Devices Meeting and in early 1982 will show up in a modular rectifier assembly from the Fort Wayne operation that will replace 50-ampere Schottky-diode devices, offering one third the power dissipation at two to three times the cost.

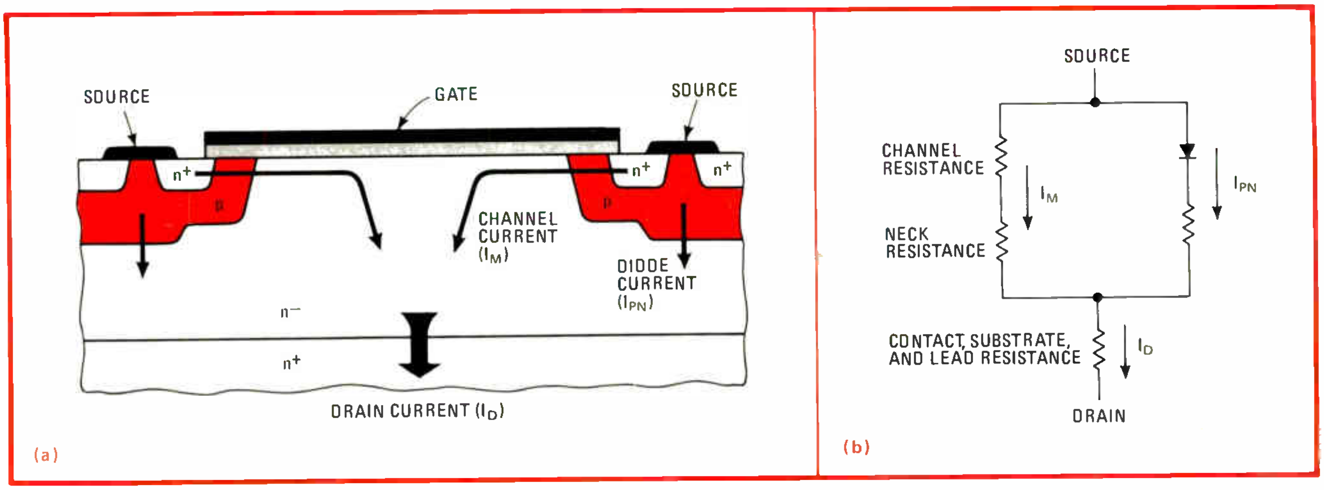
The efficiency of switching power supplies is well established and much touted. At power levels of around 250 watts and higher, switchers have clear advantages over linear supplies in cost and size as well as efficiency. They are even making inroads into the linear realm between 50 W and 250 W. But at output voltages less than 5 volts, where most mainframe logic circuits operate, their efficiency drops drastically, due for the most part to the power dissipation in the output diodes.

This problem has been around as long as switching supplies themselves, and the best solution to date has been the widespread development of Schottky diodes as replacements for pn-junction devices. Since diode dissipation is a considerable fraction of a supply's power consumption only for low-voltage outputs, Schottkys have not had to meet high reverse-breakdown requirements; their key figure of merit is forward voltage drop.

Schottkys presently offer 20% to 30% lower voltage drops—0.6 V to 0.8 V in a 50-A device, depending on the breakdown rating and junction temperature, compared with 1 V or more in a pn diode. Possible further improvements are severely limited by material characteristics: a voltage comparable with the metal-semiconductor barrier height is always required to sustain conduction in a Schottky diode.

This has not stopped Schottkys from growing into a market worth some $25 million worldwide annually, with the bulk of these sales in devices for 20 A and higher that are rated for reverse voltages between 20 V and 50 V. Low-voltage switching power supplies are their single biggest application; the higher the current levels in these supplies go, the more pressing is the need for more efficient rectifiers to hold down the power dissipation that degrades a system's reliability.

Hence interest in synchronous rectifiers has been growing. However,



Fine tuning. Current flow in a power MOS FET (a) is modeled by the circuit in (b) at RCA. This model uses a new method for obtaining the components of on-resistance and shows their relative importance in devices rated for low voltages, such as synchronous rectifiers.

"synchronous rectification was a dream that power-supply engineers had for years," possible only now with the advent of power MOS FETs, according to Joseph Perkinson, a West Boxford, Mass., consultant.

Proper turn-on. A synchronous rectifier now has come to mean a MOS FET whose conducting channel can be turned on at the appropriate times relative to the voltage between its source and drain. Since available vertical power FETs always contain a parasitic diode that is reverse biased when the drain is positive with respect to the source, a FET for rectification must be operated with the source serving as anode, and the drain as cathode.

Then for one polarity of voltage, the gate is held low, giving a pn diode's reverse blocking characteristics between source and drain, which are significantly better than a Schottky's. On the other polarity, the gate is driven high, allowing forward conduction. Since dc conduction is primarily through the resistive channel and not the pn junction, the minimum accompanying voltage drop is not set by a barrier height as in Schottky diodes, but simply by the device's on-resistance and operating current.

Thus one key question for the widespread use of synchronous rectifiers will be the on-resistance attainable in a die size of about 200 mils on a side, roughly the size of the Schottky diodes used in the low-voltage applications for which they will compete. Since a high-voltage blocking capability is not sought, the device's epitaxial layer resistivity can be reduced.

Work on doping. At reverse-voltage ratings below 100 V, the major contribution to the resistance in a vertical MOS FET comes from the channel itself. Because tailoring this region's resistance affects the threshold voltage and transconductance, work will focus on the optimal doping profiles for this application.

At RCA Corp.'s Sarnoff Research Center in Princeton, N. J., synchronous rectifiers are under investigation along with other power MOS FETs—RCA recently announced its entry into the power FET business [*Electronics*, July 28, p. 41]. Ming L. Tarng will be showing an analysis of FET on-resistance contributions at the IEDM, setting down the relative importance on the channel, neck, and contact resistances for varying voltage ratings.

Tarng says that "present capabilities in the laboratory need to be refined for about a twofold improvement in on-resistance to make FETs a fair tradeoff against Schottkys, and that could happen very soon, within a year or so." A factor of four in on-resistance would virtually assure the demise of Schottkys in switching power supplies, but that will take more than just fine tuning.

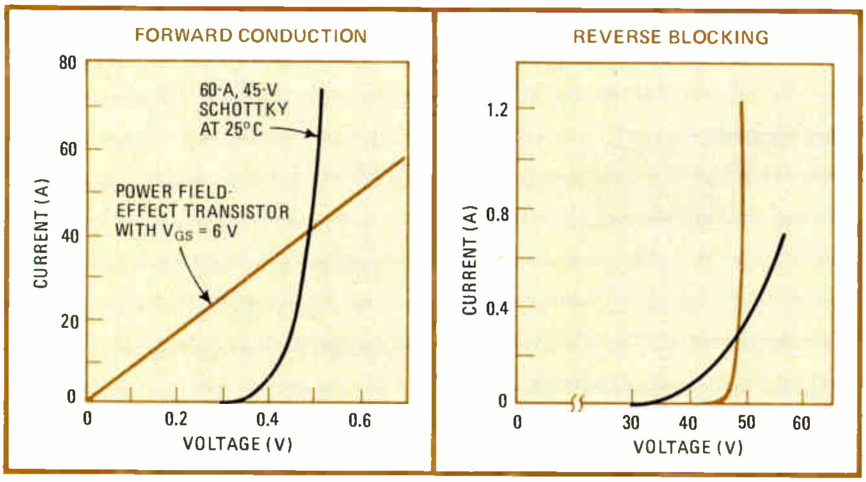
Advanced processing. The researchers at GE are using advanced processing techniques like plasma etching, projection printing, and two-step diffusions to fabricate some 60,000 FET cells in parallel for an on-resistance of 0.014 ohm. As Adler notes, "this is the largest power FET yet reported and is as big a device as one can make with reasonable yields."

Not surprisingly, the pricing of GE's synchronous rectifier module will depend heavily on the device yields. William Archer, manager of development enginering in Fort Wayne, adds that "the components required for the drive circuit are included in the module, amount to less than eight parts for the two rectifiers, and make them two-terminal devices." With proprietary drive circuitry already designed, GE appears to be establishing a foothold from which extended development work can be expected to proceed.

One of the unknowns for many potential users continues to be just how much added cost is incurred by the drive circuits for the FET gates. The simplest possible drive circuit provides additional windings on the transformer that are tapped to drive the gate. Given the low drive requirements of a MOS FET, this scheme could turn on the channel perfectly well. However, turn-off may require not just a voltage to the gate, but current commutation of the parasitic diode. The effective recovery time of a FET in this transformer circuit could be too long for switching power supplies.

Provided that the parasitic diode always conducts much less current than the channel itself, it should be possible to get secondary regulation of power supply outputs by modulating the FET gate drive. In other words, control circuitry could be used not only to sense the primary output and adjust the switching transistor's on-time, but to sense secondary outputs and adjust the voltage dropped across synchronous rectifiers.

While these possibilities are intriguing, Schottky makers are not losing sleep over them now. As William Sebastian, manager of applications engineering at TRW semiconductor in Lawndale, Calif., says, "We don't see synchronous rectifiers crossing over Schottkys in either cost or efficiency in the near future." Good Schottkys now cost only about $3 in quantity. □



FET rectifier. A power transistor from GE promises big gains over Schottky diodes. Forward conduction follows a resistive curve while reverse blocking is by a pn diode.

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Components

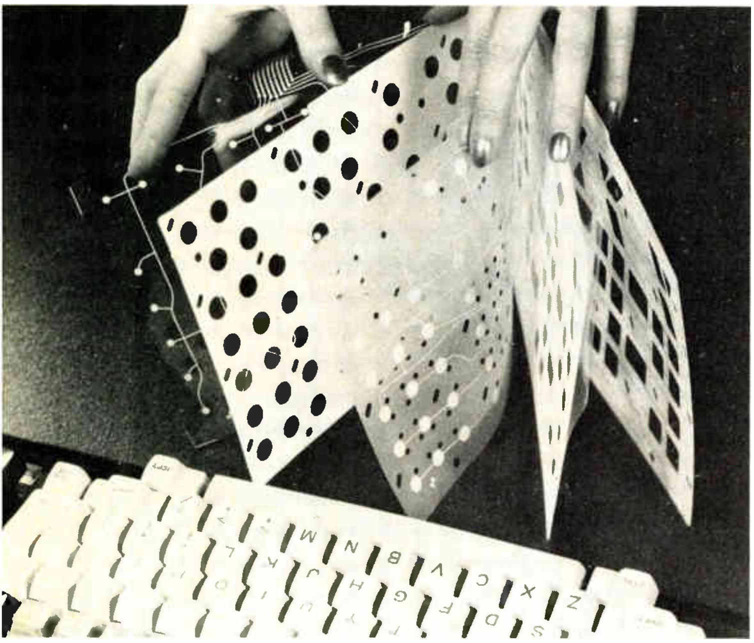
Membrane keyboard boom awaited

New suppliers are attracted to market despite skepticism in some quarters about the technology's reliability

by Wesley R. Iversen, Chicago bureau

The still embryonic market for full-travel alphanumeric keyboards based on low-cost membrane technology may soon be assaulted by a spate of new suppliers. For example, Maxi-Switch Co. of Minneapolis, and Key Tronic Corp. of Spokane, Wash., are planning to bring out new full-travel membrane keyboard units within the next six months. And the W. H. Brady Co. of Milwaukee has developed a new thin-film membrane approach that it plans to put into production during the second quarter next year [*Electronics*, Sept. 18, p. 33].

The flurry of activity is spurred by manufacturers' expectations that the cost advantages claimed for the membrane technology will fuel a fast-growing market among low-end computer and terminal makers. By 1985, membrane units could easily account for 30% of the market for full-travel alphanumeric keyboards of all types, declares William R. Spivey, marketing manager for Honeywell Inc.'s Micro Switch division, Freeport, Ill. "I expect we'll see more people [keyboard manufacturers] jumping on the bandwagon over the next 18 months and after that we'll see a shakeout," says Spivey, whose company this spring became the third to introduce a line of full-travel membrane keyboards [*Electronics*, May 5, p. 34].



Keyboard fan. A six-layer Mylar sandwich makes up Micro Switch's full-travel membrane keyboard. It is 32 mils thick.

Other keyboard manufacturers agree, but not all industry watchers are so optimistic. Despite their heralded potential, they have been slow to catch on among keyboard users. At Gnostic Concepts Inc., senior analyst John Hutchison predicts that sales will continue to be slowed by the technology's lack of a reliability track record. Major keyboard users will shy away from the units, leaving it up to the smaller original-equipment manufacturers initially to prove their worth in the field, Hutchinson says. At least one leading keyboard maker, Cherry Electrical Products Corp. of Waukegan, Ill., says it has no plans to enter the market.

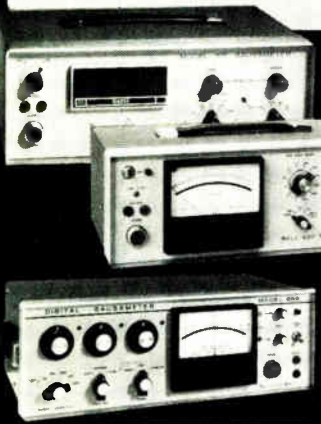
"There are a lot of people who don't trust newfangled technologies," as Steven W. Leininger puts it. And at Radio Shack in Fort Worth, Texas, where Leininger served as director of advanced development, there was also a question over the cost-effectiveness of full-travel membrane units.

Gnostic's Hutchison, who just completed a major keyboard study for the Menlo Park, Calif., market research firm, projects that domestic OEM consumption of full-travel keyboards of all types will soar from last year's $147 million total to about $542 million annually in 1985. But, the membrane versions will account for only $15 million, or less than 3%, of the 1985 total, he says.

Chomeric offspring. Full-travel membrane keyboards were developed originally by Chomerics Inc. The Woburn, Mass., firm's Fastype line introduced in 1979 issued from a marriage of Chomeric's successful flat-panel, touch-sensitive switch technology with conventional vertically moving or full-travel keys.

But the Chomerics product ran into problems in the market. At Genisco Technology Corp.'s Computer division in Costa Mesa, Calif., engineering vice president Rick Harris recalls that his engineers did not like their feel.

At the same time, at Zenith Data Systems' computer business group in Glenview, Ill., computer engineering manager T. Michael Hakeem says his firm rejected the Chomerics line about six months ago because of its key tower design that led to "some problems with sticky keys." Instead,



Probing the news

Zenith chose to run an extensive evaluation of the membrane keyboard brought out by Oak Switch Systems Inc. last year [*Electronics*, Aug. 14, 1980, p. 44].

The Crystal Lake, Ill., company rates its full-travel unit capable of 100 million cycles per key, a mark that some terminal and computer makers specify. By mid-October, Zenith will have completed a 5-million-key-cycle test on the Oak board, says Hakeem. "We're trying to see if there's any breakdown of the contacts and we haven't seen any evidence so far. In future products, I'd say there's a very good chance that we will use them."

As for the Chomerics line, the company's Membrane division was acquired last May by AMP Inc., where the new management is "developing new plans and strategies. We know what the shortcomings are [in the former Chomerics line], and we're going about correcting them," says Jack A. Usner. As director of marketing for AMP Keyboards Technologies Inc., Burlington, Mass., Usner says, "The company that gets there first with the lowest cost and highest performance will drive the full-travel membrane market, and we think we can do that."

Price war. Indeed, full-travel membranes could be in for stiffer than anticipated price competition. At Zenith, Hakeem notes that the threat from full-travel membranes has already prompted aggressive price cutting on the part of some mechanical-keyboard suppliers. Uncoded membrane units from Oak are being offered at $25 to $30 each in volume quantities, and mechanical keyboards from some suppliers are "getting down to within $2 to $5 of that price," Hakeem observes.

Zenith is planning to evaluate prototype full-travel membrane units received from Micro Switch about a month ago. But prices currently being quoted by the Honeywell division—$65 for a fully encoded capacitance unit in quantities of 10,000, $45 for unencoded hard-contact versions in like numbers—seem a bit high, Hakeem says.

For their part, the suppliers say that prices will drop with volume production. While conceding initial OEM skepticism, officials at Oak and Micro Switch contend that now is being overcome and that initial small to moderate production orders are beginning to trickle in. For example, Osborne Computer Corp., a 16-

Conductive elastomer models gain ground

Though full-travel keyboards based on polyester membrane technology are in the spotlight now, there are signs that conductive elastomer-based keyboards may be about to emerge as a new competitor for the low-end computer and terminal market. Low-cost keyboards produced in the Far East that employ synthetic rubber have been used broadly for years in Japan and elsewhere, and more recently in the U. S. Primary application has been in calculators, point-of-sale equipment, and other gear requiring keys with only limited travel.

But now, U. S. keyboard users say they are evaluating Japanese-built conductive elastomer units that offer a full-travel, typewriterlike stroke. Before the end of the year, Maxi-Switch Co., Minneapolis, plans to introduce an elastomer-based keyboard line with about a 0.125-inch key stroke—well within the 0.080-to-0.170-in. travel range defined as "full travel" by industry sources. The elastomer keyboard line will be the first from a U. S. merchant keyboard supplier to offer a full-travel stroke, believes Maxi-Switch president Craig Stout. Maxi-Switch plans to bring out conventional polyester-membrane-based units in addition to the elastomer line.

Elastomer-based keyboard units that offer the longest stroke typically rely upon a molded, nonconductive silicone elastomer membrane or mat that is assembled between a printed-circuit board and an overlay containing plastic keys. The mat contains domed protusions that collapse under pressure. When a key is depressed, a bump or disk or carbon-filled conductive elastomer that has been vulcanized to the underside of the dome is pressed against the printed-circuit board, shorting across two metal contacts to complete the circuit.

-W. R. I.

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Probing the news

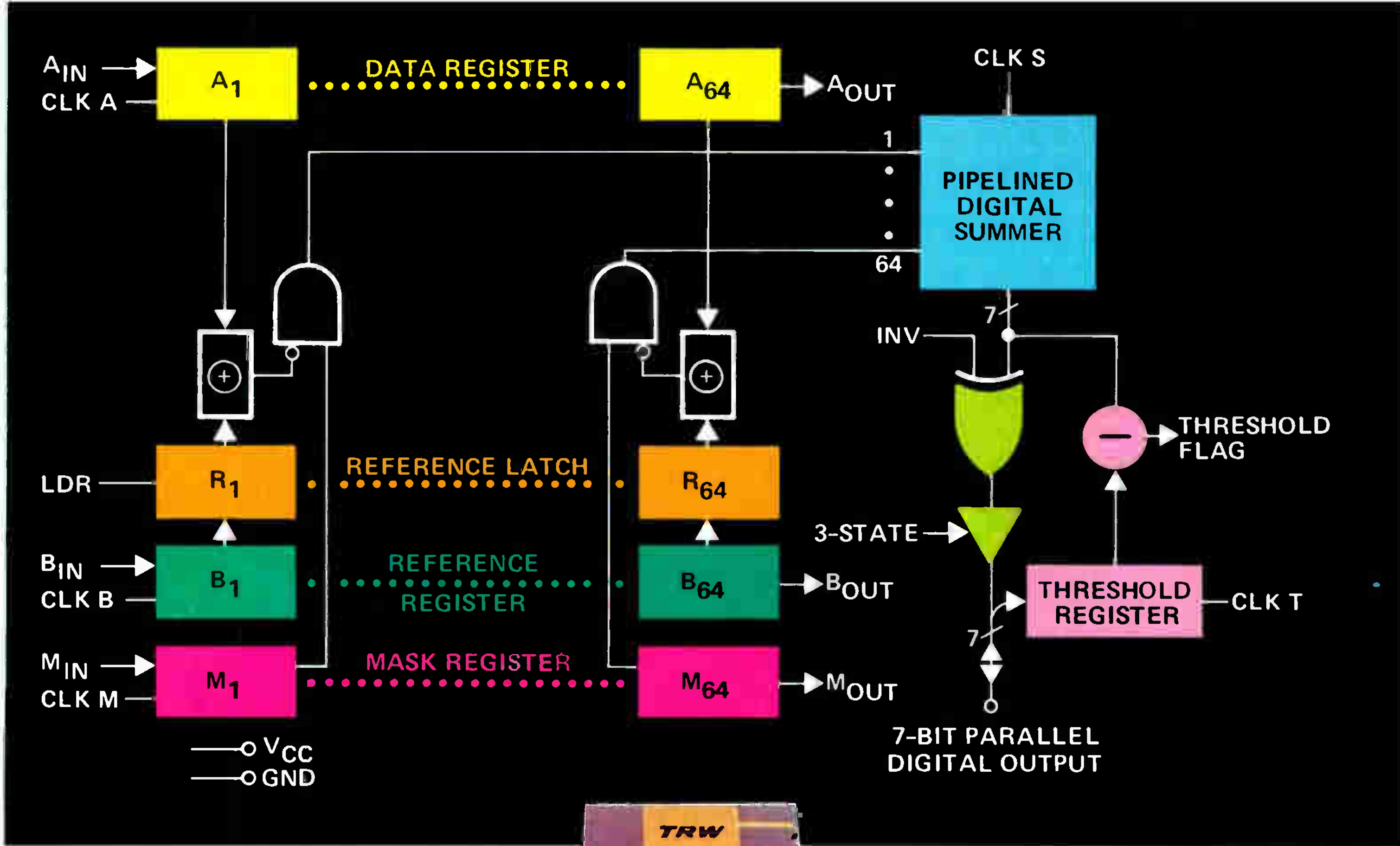
month-old Hayward, Calif., firm, recently decided to take about 65,000 Oak membrane units over an 18-month period as one of two keyboards to be used in the company's Osborne 1 low-cost portable computer, says Thomas E. Davidson, senior vice president and general manager.

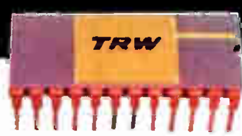
Thin-film approach. One firm that is taking a different approach to the full-travel membrane business is the W. H. Brady Co. Already a supplier of conventional flat-panel membrane switches through its Xymox division, the Milwaukee firm has developed a membrane technique that relies upon the vacuum deposition of a thin film of metal—1,000 angstroms—to form the conductive tracks on the membrane. Compared to conventional membrane methods, which employ conductive inks containing silver laid down by silk screening, the thin-film approach with nonprecious metals will lead to cheaper and more reliable keyboards, contends Sterling F. Strause, vice president for research and development.

Whether full-travel membranes live up to the heady expectations of their manufacturers, of course, remains to be seen. At Hewlett-Packard Co.'s Data Terminal division in Sunnyvale, Calif., engineering manager Lance Mills says that a yearlong evaluation of a variety of keyboard products from some 30 different vendors has led to the selection of a keyboard technology other than full-travel membrane to be used in most of the division's 1983 products.

A primary objection is the "quality of feel," says Mills, who notes that his firm has looked at Chomerics, Oak, and Micro Switch units. "Particularly for the office of the future, the role model we're trying to emulate is the IBM Selectric."

Evaluations are still under way at many OEM houses, however. At one, Datapoint Corp. in San Antonio, Texas, Computer Systems division vice president and general manager James C. Cogan says that use of full-travel membranes in future products would appear to offer a 30% cost advantage over the capacitive keyboards that Datapoint employs in its current product line. □





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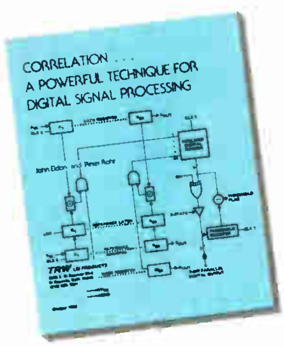

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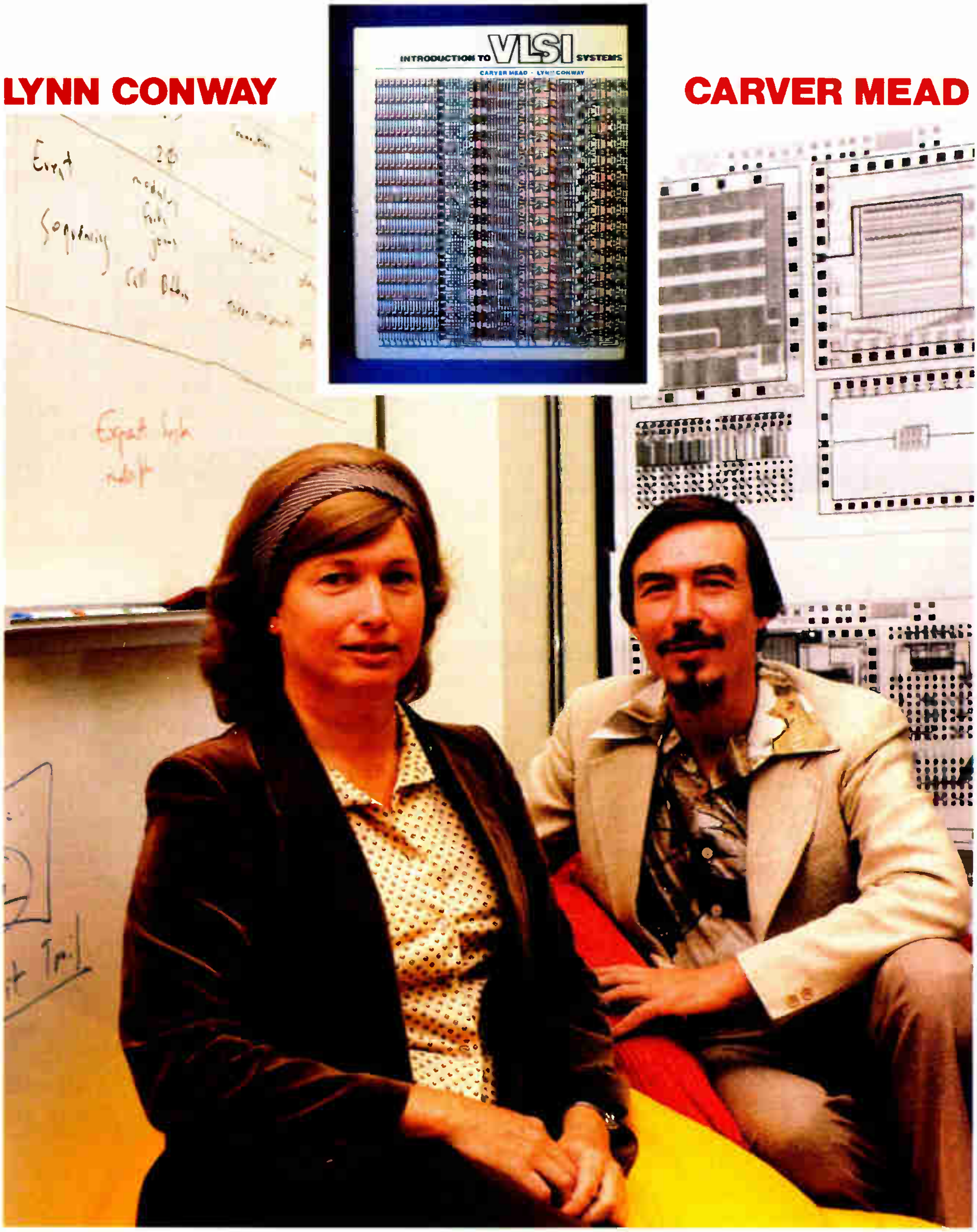


For optimal VLSI design efforts, Mead and Conway have fused device fabrication and system-level architecture

by Martin Marshall, Larry Waller, and Howard Wolff *of the Electronics staff*

☐ The impact of Carver Mead and Lynn Conway on the design of very large-scale integrated circuits is bringing about a fundamental reassessment of how ICs are put together. Mead, the Caltech professor, and Conway, the Xerox system designer, have optimized the VLSI process by melding the concepts of fabrication at the device level and architecture at the system level to produce truly integrated systems.

The work they have done, individually and together, brought to fruition in their seminal textbook, "Introduction to VLSI Systems," is truly monumental. In the area of structured IC-design methodology, they not only have helped spawn a common design culture so necessary in the VLSI era, but they have greatly increased interaction between university and industry so as to stimulate research by both.

Putting their methodology between the covers of a book, one that is now used by more than 100 universities around the world, was only part of their accomplishment—even if it did take the better part of two years. Rather, gaining acceptance for some of the book's underlying assumptions is at the heart of the matter.

Some theorists who create an important body of work stop there, leaving the task of popularizing it to others. Mead and Conway regarded their theories as only the beginning and set out to popularize them. The vehicle was the classroom: Mead through his graduate classes in Pasadena at the California Institute of Technology, and Conway through a landmark course she taught in 1978–79 at the Massachusetts Institute of Technology in Cambridge as visiting professor in electrical engineering and computer science.

Mead, who describes himself as a "lifer" at Caltech, did his undergraduate and graduate work there and then served as assistant professor and associate professor before obtaining the Gordon and Betty E. Moore professorship, a chair endowed by and named after the chairman of Intel Corp. and his wife. Conway is transplanted from New York, with bachelor's and master's degrees from Columbia University's School of Engineering and Applied Science.

For Mead, the seeming rush toward acceptance of his once controversial ideas on simplified custom-circuit design has been anything but sudden. He has promoted his ideas whenever and wherever possible over the past decade, facing dismissal by most of a skeptical semiconductor industry. What support he did gain came mostly from computer and systems firms interested in affordable high-performance devices tailored to their needs. But giant semiconductor houses were implacable in ignoring him and his version of design automation—what used to be called computer-aided design. There was one notable exception: Intel Corp., the Santa Clara, Calif., semiconductor maker, with which Mead has long had close ties.

About two years ago industry opinion began to shift toward Mead's views. The major impetus was provided by the book, which even before its official 1979 publication date had already established itself at such top schools as MIT, the University of California at Berkeley, and Carnegie-Mellon University in Pittsburgh. Mead recalls, "It was Lynn's idea to copy the first chapters to enable the schools to start their VLSI courses. She is particularly good at propagating knowledge."

For all its impact, the basic concept formulated by Mead and Conway is simple. It holds that ICs are so complex and dense that human designers cannot deal with individual devices; instead, they must be handled at a higher level of integrated system architecture. Though today this is a truism because of VLSI's complexity, that view was radical when it was first enunciated some 10 years ago.

Still, the implications of the Mead-Conway concept disturbed semiconductor industry powers. For one thing, it advocates establishing many small groups to design custom proprietary circuits, attacking the concept of the standard IC, which was the bread and butter of the business. For another, in the mid-1970s Mead in particular began calling for what are called silicon foundries that would accept and fabricate independent designs. (The term silicon foundry was coined by Intel's Moore, but Mead disseminated it.)

The unpopularity of such views was almost inevitable. One well-aimed criticism called the approach an oversimplification of the difficulties of device design and held that it overburdened fabrication engineers. Another barb claimed the approach failed to account for basic differences among process technologies.

Another source of friction was Mead's prediction of a widespread restructuring of the semiconductor business to separate design and fabrication functions. It is not surprising that industry officials who struggled to build their companies grumbled about "ivory tower academics" who offered economic advice.

Such criticism is brushed aside by Mead. He simply points to events of the past year, which he believes are proving out his ideas and moving the industry in the directions he charted—for example, Intel's establishment of a silicon foundry in Chandler, Ariz. [*Electronics*, Sept. 8, p. 39]. Smaller firms dedicated as foundries also have been springing up. Mead is quick to predict that the spread of the Mead-Conway design-automation concepts signals nothing less than "an innovative revolution that, once started, nothing will stop."

Mead and Conway's collaboration dates back to 1975, when Conway began to participate on behalf of Xerox in what became the Silicon Structures Project. Her participation was the result of the cooperative effort between Xerox and Caltech put together by the brothers Bert and Ivan Sutherland. Bert was manager of the systems science laboratory at Xerox's Palo Alto (Calif.) Research Center and Ivan was the co-creator of the structures project. "I was working on special-purpose architecture for image processing at the time," recalls Conway. "I had become aware that there was a gap between the sorts of systems we could visualize and what we could actually get into hardware in a timely way."

For that reason, designers of digital systems were almost entirely limited to using off-the-shelf logic. In one design, Conway recalls, her group implemented an image-processing system in medium-scale TTL ICs but couldn't make it sufficiently compact or cost-effective without equivalent VLSI circuits. "At the same time I decided to expand my knowledge from computer architecture to silicon, I met Carver, who was coming upward from a knowledge of ICs into computers," she says. The meeting point was an LSI systems area that Conway and co-workers had formed at the Xerox research center to simplify its design methods.

"We finished the draft of the book just before I had to teach the prototype class at MIT in the fall of 1978," she says. "We printed 300 copies at Xerox. Some were shipped down to Carver, and I loaded the others into my stationwagon and drove off to MIT." The rest, as they say, is history.

The MIT class was a smash hit: the students learned about the methodology in September, created their own designs in October and November, and handed them in by early December. Six weeks later, the masks for the multiproject chip design had been made by electron-beam lithography at Micromask Inc. in Santa Clara, Calif., and the wafers had been processed at Hewlett-Packard Co.'s IC processing lab in Palo Alto. The dice had been cut and packaged with custom wiring running from the 40-pin dual in-line package to the internal pads for each separate circuit project within the chip. Each student received a silicon implementation of his design. "Many of the designs were fully functional," Conway says.

Buoyed by the success of the project, she returned to California in the spring of 1979 with an even more ambitious plan in mind: a network of university projects modeled after hers at MIT. Each would design a multiproject chip, format it, and transmit it to the Xerox research center via Arpanet, the packet-switched communications network of the Department of Defense's Advanced Research Projects Agency.

"It was basically a stunt to show the power of the VLSI design and implementation methods," states Conway. "It involved broadcasting the rules of the game over Arpanet and creating the VLSI implementation system software. We got Stanford, Berkeley, Caltech, the University of Colorado, MIT, the University of Illinois, the University of Washington, the University of Rochester, and Carnegie-Mellon to participate." Again the chips were fabricated at HP, but this time the cycle took only 29 days and the chips were delivered on Jan. 2, 1980.

The MIT class marked a triumphant return there for Conway, who had studied physics at the school before transferring to Columbia. She had joined International Business Machines Corp. at its Yorktown Heights, N. Y., research headquarters in 1964, moving to California the next year when it established its advanced computer research laboratory in Menlo Park. While at IBM, she made major contributions to the architecture of ultrahigh-performance computing systems. In 1969 she joined Memorex Corp., where she was processor architect of a small business computer just before Memorex

The 1981 Achievement Award

For their work in structuring the methodology of the design of very large-scale integrated circuits, summed up in the basic textbook on the subject, "Introduction to VLSI Systems," Carver Mead and Lynn Conway have been designated by the editors of *Electronics* as the recipients of the magazine's eighth Achievement Award. The efforts of Mead, the Gordon and Betty E. Moore professor of computer science and electrical engineering at the California Institute of Technology at Pasadena, and Conway, research fellow and manager of the VLSI system design area at Xerox Corp.'s Palo Alto Research Center in California, have begun to transform the thinking of semiconductor makers around the world.

Previous winners have been: in 1974, Gordon E. Moore, president of Intel Corp. for his overall accomplishments; in 1975, the four developers of integrated injection logic, Horst Berger and Siegfried Wiedmann of International Business Machines Corp. and Arie Slob and Cornelius Hart of Philips of the Netherlands; in 1976, Robert C. Dobkin of National Semiconductor Corp. for linear-circuit development; in 1977, Charles H. House of Hewlett-Packard Co. and B. J. Moore, president of Biomation Corp., for major instrumentation innovations; in 1978, Paul Richman, president of Standard Microsystems Corp., for advanced developments in MOS technology; in 1979, Andrew H. Bobeck of Bell Laboratories for his role in the invention of magnetic-bubble memories; and in 1980, Abe Offner, Jere D. Buckley, and David A. Markle for their development of the projection mask aligner at Perkin-Elmer Corp.

decided to get out of that market. She joined the Xerox research center in its early days in 1973 and began working on a combined optical character recognizer-facsimile system. It was that project that triggered her desire to create systems in VLSI.

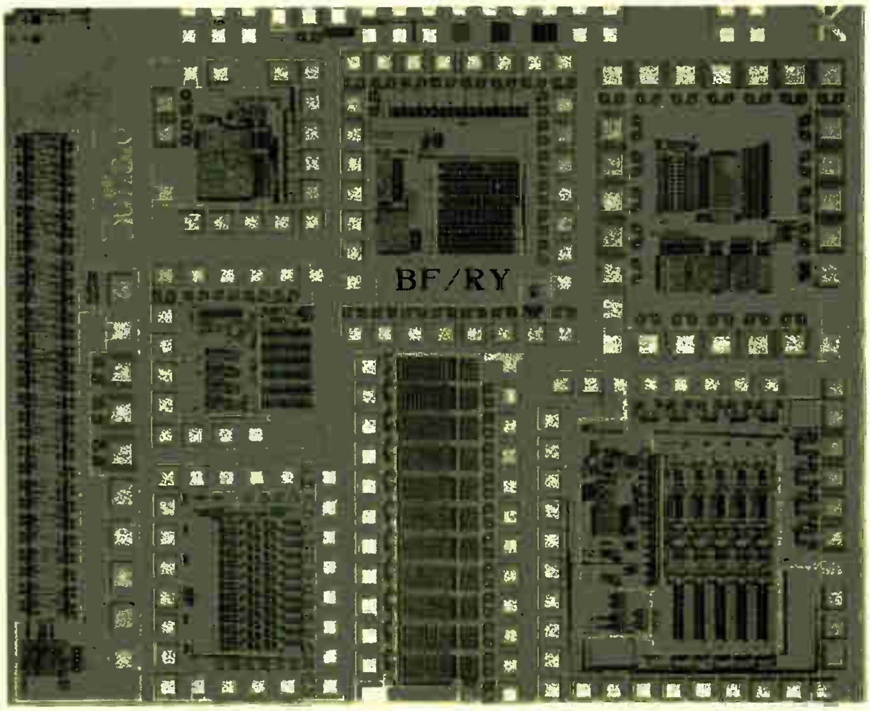
Mead's interest in design automation goes back to the late 1960s, during a project to scale down ICs. "Calculations on how small they could go showed that the answer was lots smaller—down to 0.25 micrometer." Since at that time minimum feature dimensions were down only to 10 μm, Mead's conclusion itself was controversial. "But to this day the 0.25-μm figure has held up, despite many people taking cracks at it," he says.

Nevertheless, posing the possibility that geometries that small were within reach raised the central question of how to design them. "Since then we've been trying to find out," Mead says.

Along the road to that knowledge came Caltech's first algorithmic software package for CAD. It evolved from a program for designing printed-circuit boards that Mead purchased in 1970 for $5,000 out of a special research and development fund. Mead's graduate students designed an experimental clock chip, making their own masks, which were run through Intel's fabrication line. "We bootlegged it through unofficially," says Mead, "although we told Robert Noyce [Intel's vice chairman] and Gordon Moore about it later."

Any discussion about the Mead-Conway methodology comes back to the book. "In electronics, a new wave comes through in bits and pieces," observes Conway. "Usually, after it has all evolved someone writes a book about it. What we decided to do was to write about it while it is still happening.

"Our method was to project ourselves ahead 10 years, and then write the book as though reflecting back upon a decade. Then we would let the people in the community critique it, and let the book itself become the focal point for the creation of methods."



Joint project. This is one of the chips in the 1979 round-robin design project, which Lynn Conway calls a network adventure involving students in a multichip, multiuniversity project.

With such a large body of interdisciplinary knowledge available, Mead and Conway had to struggle with selection. "We had to figure out which knowledge was not needed," she says, "and come up with the simplest subset required to do any digital design." The pair decided that n-channel MOS was the ideal technology for their methodology and also decided to bypass Boolean logic gates as an intermediate step. Replacing them: simple field-effect transistor switches and such devices as stacks, barrel shifters, and functional blocks that are replicated to form larger subsystems. "We also decided that we could normalize the design rule to the resolution of the process," says Conway. "Later on, we could ask about the value of the minimum line width."

By putting together a set of design rules that was independent of line width, Mead and Conway were avoiding some of the difficulties of standard semiconductor design practice. They skirted the issues of fine tuning of the fabrication line by making some fundamental assumptions about such questions as how wide metal should be in proportion to polysilicon. "We wanted to come up with something that students would learn once and retain," says Conway. "We chose the ratios based on Carver's knowledge of where the processes are headed." These ideas anchored the book.

Any lingering doubts about the practicality of Mead and Conway's approach must have been dispelled by the appearance of the Motorola 68000, the 16-bit microprocessor whose design was significantly influenced by the duo's methodology. The 32-bit iAPX-432 from Intel put the icing on the cake.

Besides the commercial components that have benefited from Mead-Conway design rules, a complex experimental floating-point processor was designed by Digital Equipment Corp. using the duo's principles. The job took much less time than with traditional methods. Also notable among VLSI chips designed in academia is MIT's public-key encoding IC with its 40,000 transistors. □

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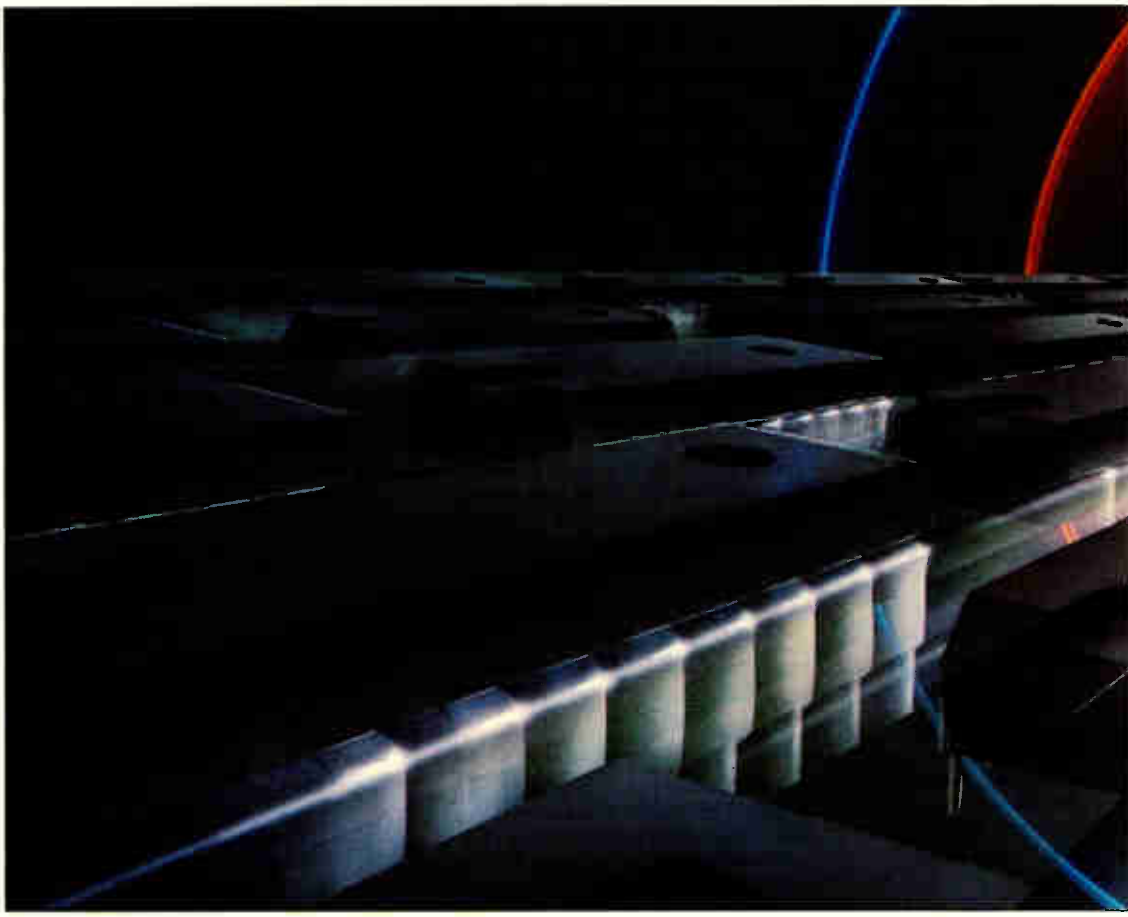

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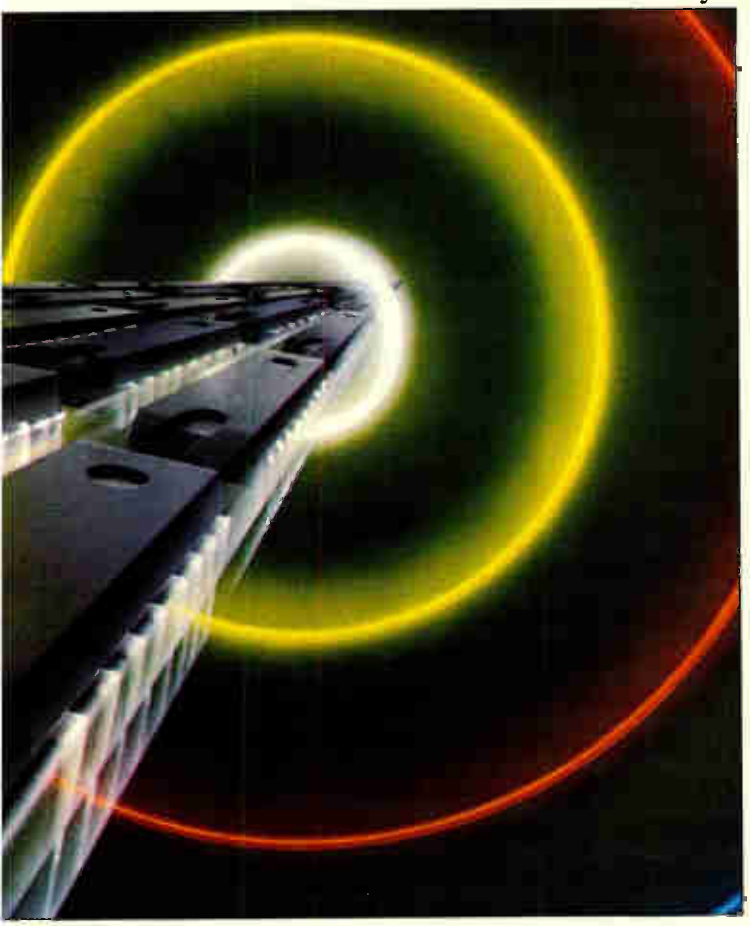

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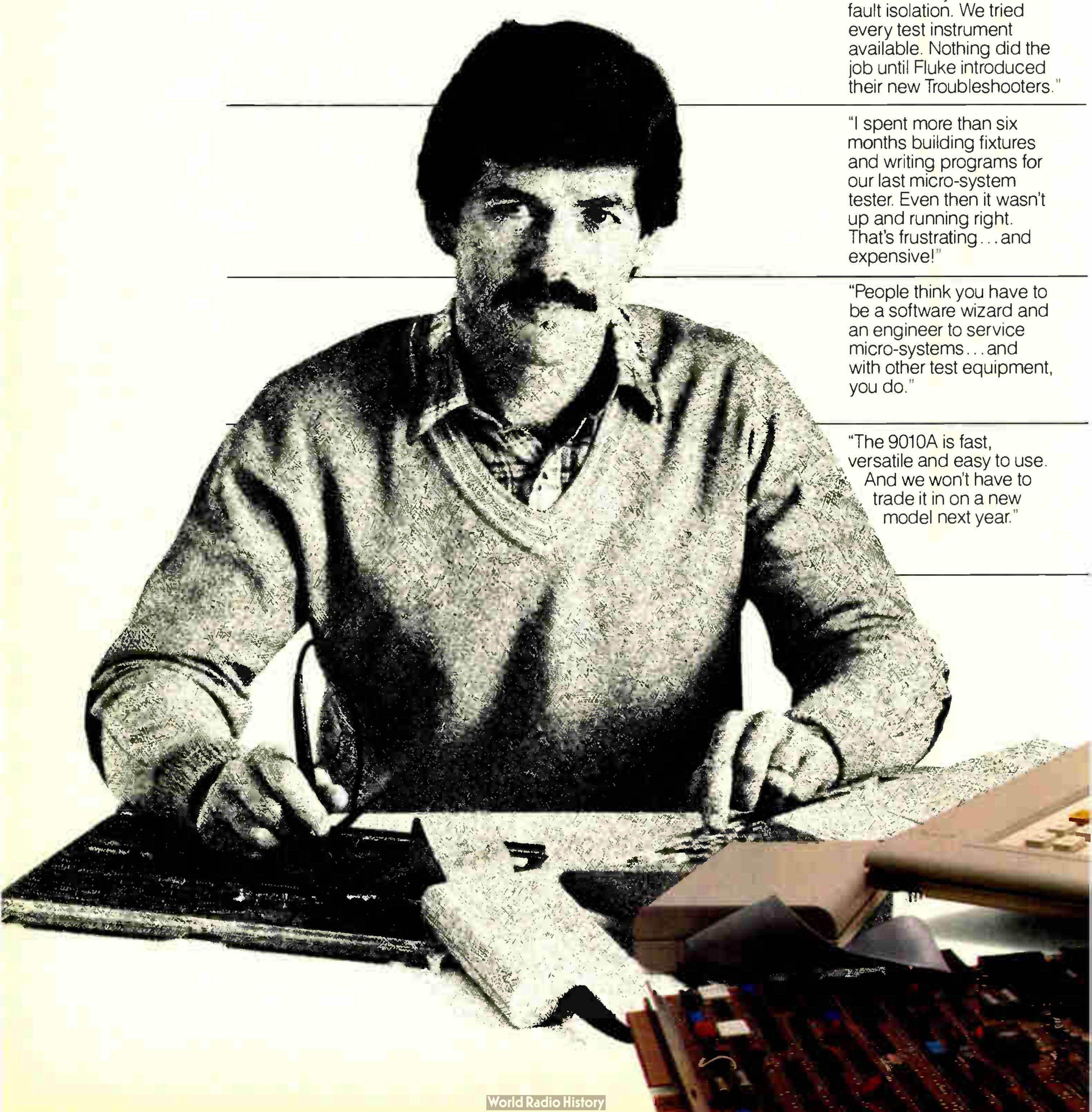

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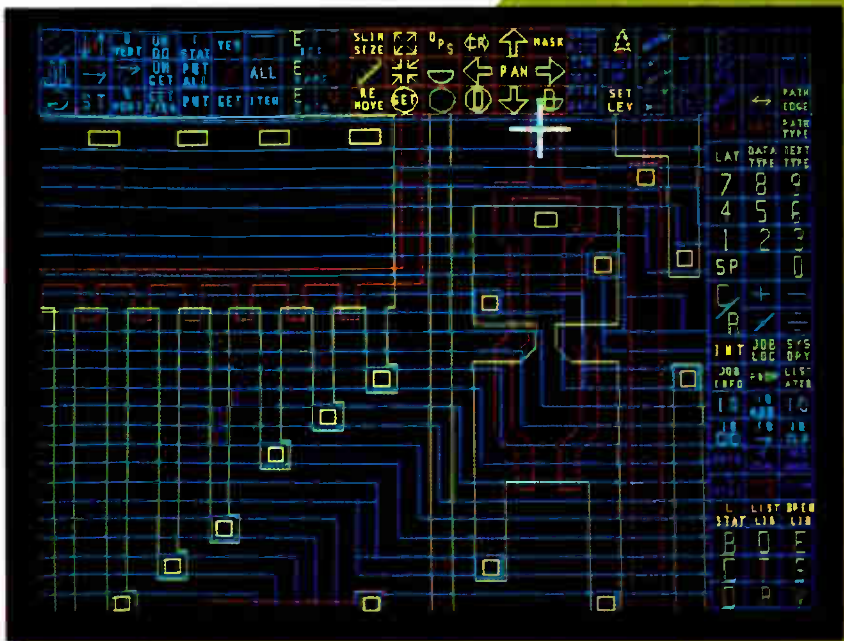
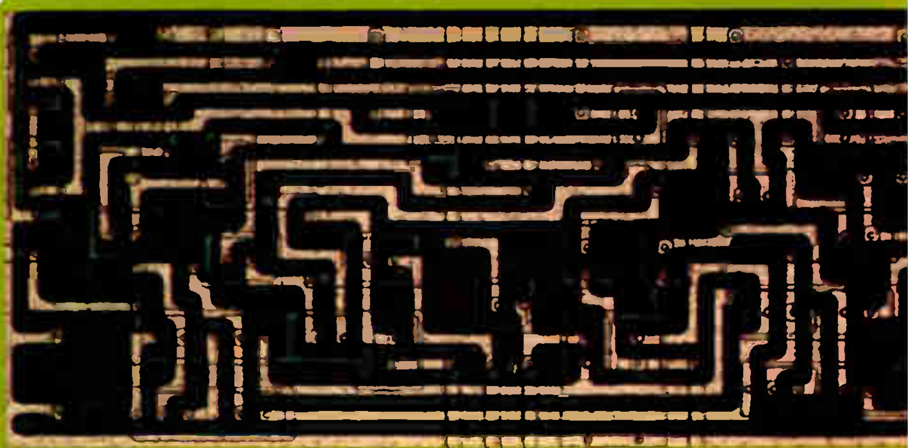
TECHNOLOGY UPDATE

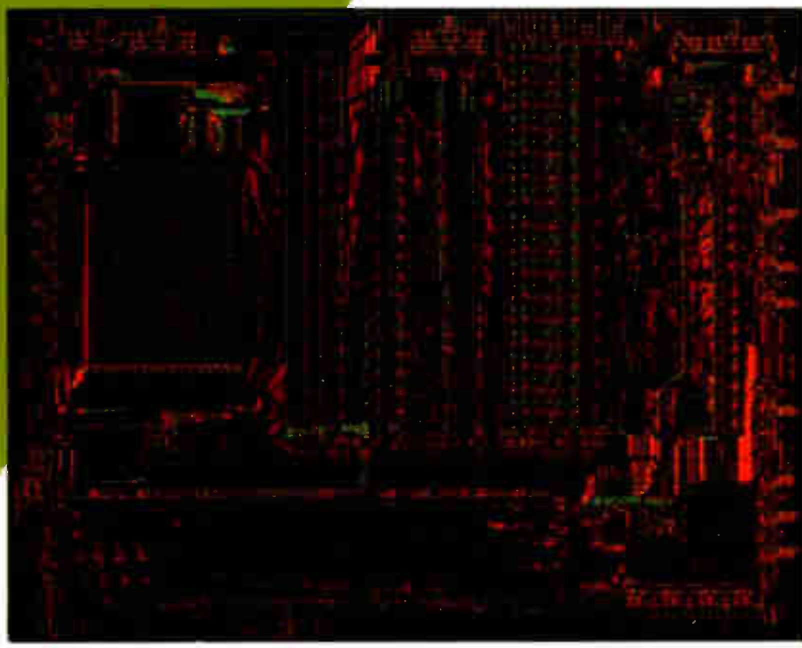


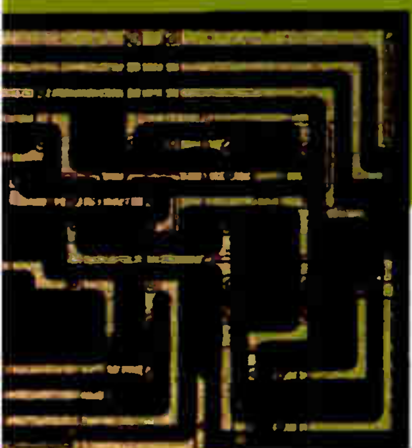


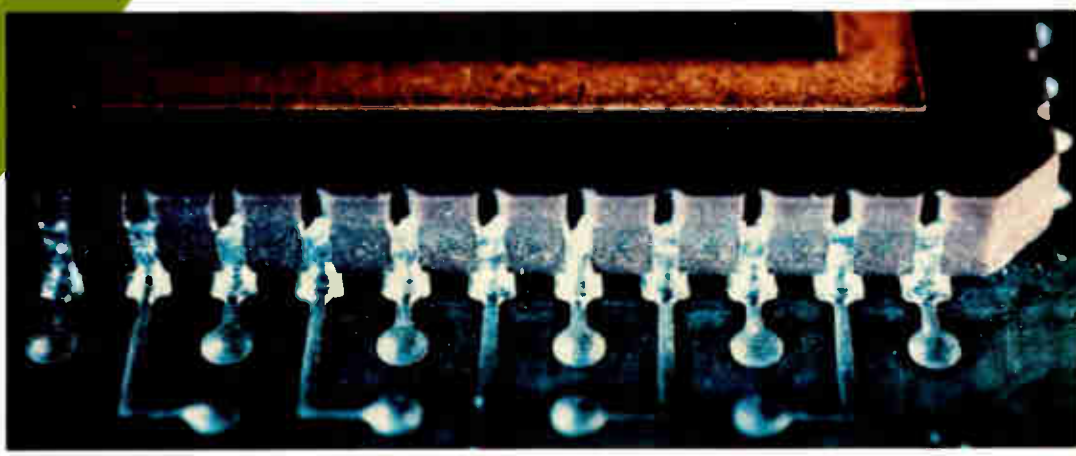
Large-scale integration has changed the face of every area of electronics in so little time that new evidence of its impact can be observed almost daily. Now, as the industry embarks on the era of very large-scale integration, the burden of application labor shifts significantly to software design. Here the possibilities seem endless, as the new degrees of freedom offered by programmable elements are exploited in all sorts of equipment for industry and entertainment alike.

While integrated-circuit technology remains the driving force, it must be supported by concomitant advances in other technologies: the packages that house the dense new VLSI circuits; the automated production equipment that keeps costs low while maintaining quality; and the test equipment needed to see the parts through production, inspection, and field service.

The dominant trends? At the chip level, complementary-MOS is emerging as the superior process; at the board level, chip-carriers are affording a density never possible before with dual in-line packages, and plastic is cutting their cost; in software, Ada is the language to listen for; local networks have become a new communications medium, and in telecommunications, the scenario is all-digital; for the consumer, there's personal video and portable sound. In all, an exciting pace continues.

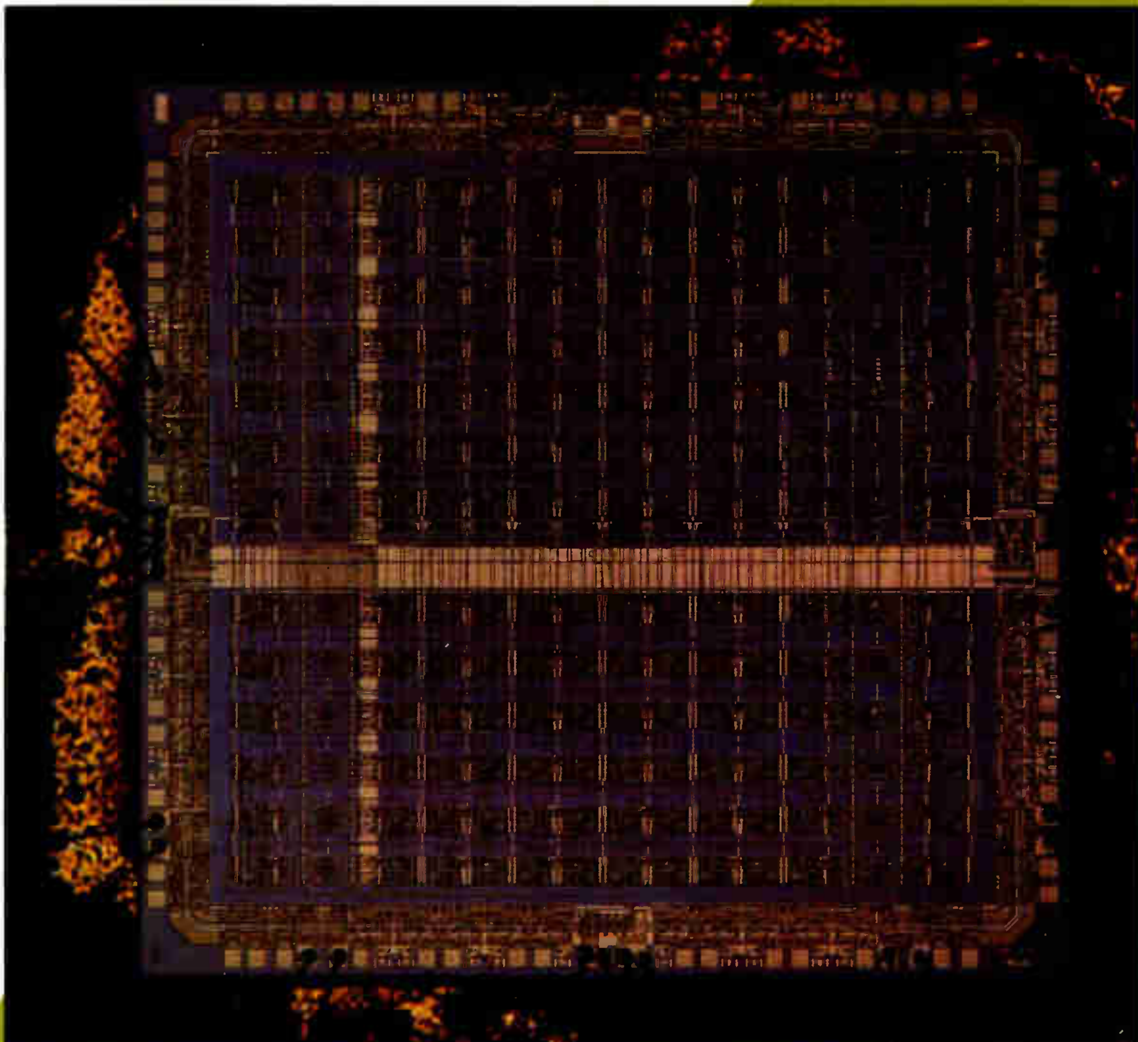






On all fronts. Great strides continue, from the macro to the micro level. Shown clockwise from left, the shuttle *Columbia* will loft new satellites into space; computerized color graphics clarify circuit design and lend startling realism to flight simulation; circuit densities rise to new levels, as in this bipolar microprocessor; such circuits adopt the low-cost packaging of plastic chip-carriers; and commercial products begin using 1-micrometer features.

SEMICONDUCTORS



A maze of arrays. The gate-array business is flourishing, as new and old companies alike sell the slices or the services to interconnect them. This unit from one of the newer companies, Applied Micro Circuits Corp., incorporates high-speed emitter-coupled-logic cells but can interface with either ECL or TTL circuitry.

Logic arrays proliferate; digital MOS and bipolar processes find new ways to speed up and squeeze down; linear circuitry stresses merged technologies

by John G. Posa, *Solid State Editor* and Roderic Beresford, *Components Editor*

☐ In semiconductor technology, no matter where the eye of the observer rests, an unceasing stream of activity immediately claims attention—this was as true in the past year as it ever has been, and it is true across the board in digital bipolar and MOS technologies. Similarly, linear technologies continue their inexorable climb towards ever greater heights of refinement. Activity in the semicustom logic market has been frantic, with established and start-up companies alike unwrapping logic arrays or design-automation services to turn a customer's random logic into silicon.

Standard logic families have not been neglected either, with bipolar gate packages receiving a big push from advanced Schottky TTL and emitter-coupled-logic processes. It is a good thing, because the latest complementary-MOS logic gates are swiftly closing the performance gap on the last generation of low-power Schottky.

MOS technology in general is benefiting from methods that isolate the devices and protect them from the destructive side effects, which would otherwise come from the aggressive down-sizing that is in store. Work continues apace on insulating substrates, but sooner to surface will be metal silicides that will bring dramatic reductions in stage delays.

The speed and density of C-MOS technology is catching up with n-channel MOS so fast that it seems to have time-traveled. In a way it has, because all of the improvements that took so long to develop for n-MOS are being applied to C-MOS overnight. The performance of C-MOS is also being enhanced with twin-well structures that optimize both transistor types.

Bipolar technology is not content to stand still and watch MOS grow fast and dense. If anything, the latest bipolar processes prove the technology has remarkable speed and layout improvements in store. Research and development of gallium arsenide circuitry has never been more heated, with complete memories and processing units being built. Submicrometer lithography is creating the fastest Josephson junctions yet. New materials and constructions underscore the technology's viability for the ultimate in high-speed signal and data processing.

Linear processes are merging technologies to optimize many functions simultaneously. Voltage regulators will be adorned with field-effect-transistor or merged bipolar-FET output stages but use standard bipolar control devices. MOS output devices, integrated with logic circuits, now allow display driving and other high-voltage applications to be performed with integrated circuits.

Continued refinements in junction-FET–bipolar processing is being coupled with laser and zener-diode trimming techniques to improve the input-stage specifications of monolithic amplifiers. Bipolar processes show plenty of life for data-converter applications, with device structures that perform well on either side of the digital-analog interface.

New logic arrays

A myriad of new logic-array products has been introduced. A good number of the recent start-up companies in Silicon Valley intend to sell or wire up gate arrays, and numerous technology-exchange agreements have been set up to speed market development. According to one of the start-ups, LSI Logic Corp. of Santa Clara, Calif., the compound annual growth rate for logic arrays between 1980 and 1985 will be 75%, as the market swells from about $90 million to $1.5 billion.

Part of that market is for very-high-speed ECL chips, consumed primarily by computer manufacturers. Fairchild, Motorola, Hitachi, and Nippon Electric are among the most active ECL-array producers. Fairchild's latest offering—the F300—has perhaps the highest packing density of all with over 5,000 equivalent gates.

The other gate-array market segment is made up of TTL-compatible slices. High-performance C-MOS is very popular here, with large, fast chips available or promised by Toshiba, Mitel, International Microcircuits, and Applied Micro Circuits, among others. The latest C-MOS chips feature at least two levels of interconnection, and up to 10,000 gates in the case of Toshiba.

Analog and digital together

C-MOS arrays also invite analog and digital functions to be integrated on the same die. Carrying this asset a step further, Applied Micro Circuits Corp. of Cupertino, Calif., introduced a C-MOS chip partitioned into four quadrants to accommodate linear and digital subsystems. The digital side allows the equivalent of 1,500 gates, whereas the analog portion contains complete C-MOS operational amplifiers, current mirrors and generators, and so on.

Gate arrays will become increasingly significant as software algorithms that automatically simulate, wire, and test the devices are put into a form that customers can take advantage of easily. Communications between customers and gate-array makers will turn more and more to remote computer links, and this will promote the silicon-foundry concept, allowing semi-custom and then fully custom very large-scale integrated circuits to be designed in one place and fabricated at another.

The third-generation high-performance MOS process, or H-MOS-III, could make a 1982 U. S. debut—Motorola Inc. and Intel Corp. are the most likely sources. According to the former, it will be characterized by gate lengths and delays of about 1.7 micrometers and 1 nanosecond, respectively. Just as H-MOS-II afforded a 2-to-1 density improvement over H-MOS-I, the third generation will be twice as dense as its immediate predecessor and should allow over 600,000 devices per chip. Thus, it will be needed for 256-K dynamic random-access memories and advanced microcomputers.

H-MOS-III will necessarily improve on the basic MOS transistor's structure. Methods will be needed to limit the encroachment of field-oxide and channel-stop implants into active areas. Source-drain regions will not be allowed to overlap with the gate, and they may have to be lightly doped nearest the gate or buried to avoid punch-through and surface effects, respectively. Polysilicon will have to be replaced or augmented with a higher-conductivity silicide or metal, and contact resistance will need to be lowered.

Insulating substrates, too, would be beneficial for device isolation and higher performance. The viability of sapphire as an insulating substrate is being increased through the Department of Defense's very high-speed integrated circuits program (VHSIC) and through Toshiba's efforts to make it commercially affordable. In addition, Texas Instruments Inc. and the Lincoln Laboratory of the Massachusetts Institute of Technology are finding cheaper ways of annealing polysilicon on oxide.

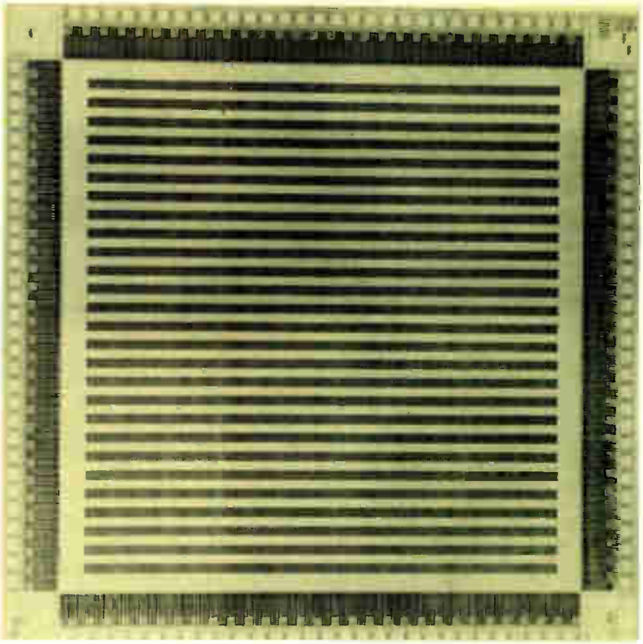
Isolation techniques

The Musashino Electrical Communication Laboratory of the Nippon Telegraph and Telephone Public Corp. has come up with two rather curious ways to isolate MOS devices: Simox, for separation by implanted oxygen, and Fipos, for full isolation by porous oxidized silicon. With Simox, oxygen ions are shot deeply enough into the substrate to form a buried insulator. With Fipos, an electrochemical process converts the p-doped silicon surrounding n-type wells into porous material, which quickly oxidizes in an electrified acid bath, leaving dielectrically isolated islands.

Though not intending to provide dielectric isolation, TI and Bell Laboratories are building VLSI MOS chips on an epitaxial layer. Both do this for their 64-K dynamic RAMs, and Bell Labs in Murray Hill, N. J. has designed a 32-bit C-MOS microcomputer using epitaxy. Mitsubishi has also published on its intentions to build dynamic memories on epi layers.

The lightly-doped epitaxial layer facilitates a highly conductive substrate that limits the lifetime of minority electrons—thereby reducing leakage currents, particularly those associated with critical storage nodes. Moreover, when used for C-MOS, the heavily doped substrate forms the base contact of parasitic bipolar voltage, thereby providing a low-resistance path for carriers that might otherwise cause thyristor-like latchup.

Although high-performance MOS processes use thick, recessed field oxides, techniques are needed to make the oxide walls steeper so that devices can be packed more



10,000 gates due. Toshiba is developing a line of C-MOS gate arrays, the biggest of which will integrate 10,000 gates. This one has 6,000. It has worked out a deal whereby LSI Logic Corp. will provide gate wiring and other services for U. S. customers.

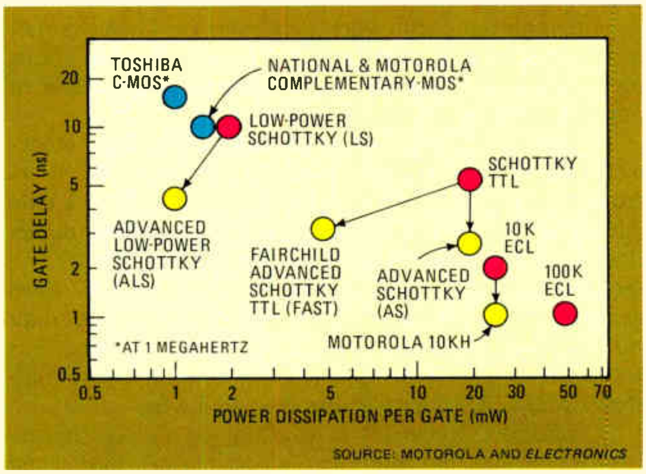
tightly. Toshiba Corp. publishes regularly on such structures, which necessarily lack the bird's beak common to standard selective oxidation processes.

Several new methods have also been proposed to limit the emission of hot carriers from the channel, as scaled-down MOS FETs are subjected to high operating voltages. International Business Machines Corp. has proposed the inclusion of shallow, self-aligned n^- regions between the channel and the n^+ source-drain regions to spread out the high electric field in the drain-pinchoff region. Not only does the technique surpress hot-electron and short-channel effects, but 5-volt parts are able to withstand 8.5 V and are over 50% faster—albeit with a corresponding increase in power consumption.

Bell Labs has made similar improvements to the basic double-diffused MOS structure by burying the drain region under the field oxide. Current flows down and away from areas prone to electron emission, and no short-channel effects have been observed—even when gate lengths are trimmed down to 0.25 μm.

To keep source-drain regions from undercutting the gate electrode, TI is experimenting with a process that leaves a thick sidewall oxide attached to the polysilicon gate to space the source-drain implants a short distance away from the gate electrode. Even if the implants spread out due to subsequent processing, gate undercutting is still avoided.

The Dallas-based company is also one of several manufacturers nearing commercial application of metal silicide to lower the resistance of polysilicon gates and interconnections. The refractory metals will also be used for more substantial ohmic contacts to source and drain regions. TI, Intel, and Bell Labs have recently described methods for applying a silicide directly onto drain and source regions at the same time that it is deposited on



Expanding families. Schottky TTL and its low-power counterpart LS TTL have spawned advanced gates with delays well below 5 ns. At the same time, high-speed C-MOS processes have resulted in new families that will compete with older bipolar parts.

top of the polysilicon gate electrode.

Even if individual devices are optimized in terms of speed and power dissipation, chip density is equally dependent on device layout. Several clever ideas to conserve die area have recently cropped up.

One is the single-device-well MOS FET, developed jointly by researchers from the University of Waterloo in Ontario and Bell-Northern Research in Ottawa. In this SDW structure, a single doped well contains a surface enhancement-mode device and a buried depletion-mode FET that share a common gate. With this merging of devices, only two of the wells are needed to build a static RAM cell. The concept also benefits analog circuits, since an entire MOS differential pair plus current source can fit into one well.

3-D compactness

SDW devices are compact because they are three-dimensional. Similar methods have also been described to shrink C-MOS gates by stacking n- and p-channel devices on top of one another. Both the Lincoln Lab and CNET-CNS of Meylan, France, have recently suggested a double-polysilicon C-MOS structure wherein the upper film is laser-annealed to serve as a second substrate. This allows the heavily-doped first-level-polysilicon gate to control two channels—one above it and one below.

Even without such space-saving measures, the popularity of C-MOS technology will continue booming. By now every major MOS chip maker in the world produces C-MOS components or has a program underway to do so.

VLSI's requirement for lower power dissipation is not the only reason for the widespread support of the technology, either. Now that C-MOS has been scaled down and given polysilicon gates and multiple levels of interconnection, it is as fast and as dense as n-channel MOS. Moreover, the complementary devices allow digital and analog circuits to be mixed on one die.

Early C-MOS structures had the n-channel FETs in p-type wells, primarily because boron—a p-type-dopant—was the only impurity that could form deep, lightly-doped regions. Later silicon-gate C-MOS processes also incorporated p-type wells. But then it dawned on somebody in the industry that an n-well process—one that favors the faster and usually more ubiquitous n-channel devices—makes more sense. So several C-MOS chip makers have since either started off with or are switching to n-doped wells.

Beyond n-type wells, however, are twin-well structures that allow n- and p-channel transistor characteristics to be independently adjusted. Hitachi, Integrated Device Technology, and Bell Labs all use double-well processes. As device features are further refined, it is expected that other companies will do the same.

Bipolar boosts

Apart from the enormous efforts to elevate the efficiency of MOS circuitry, equally impressive work has gone into bipolar technology. Unlike MOS devices, which depend on ever-shorter lateral dimensions for higher speed, the performance of bipolar circuitry largely hinges upon finer vertical dimensions. Other factors aside, MOS FETs benefit from shorter channels and bipolar transistors from thinner base regions.

In addition to geometry reductions, oxide isolation, and self-alignment, bipolar structures need shallower implants and thinner epitaxial regions. NTT's Musashino lab has used all of these techniques in its super-self-aligned bipolar technology and has been rewarded with submicrometer base widths and 63-picosecond gates.

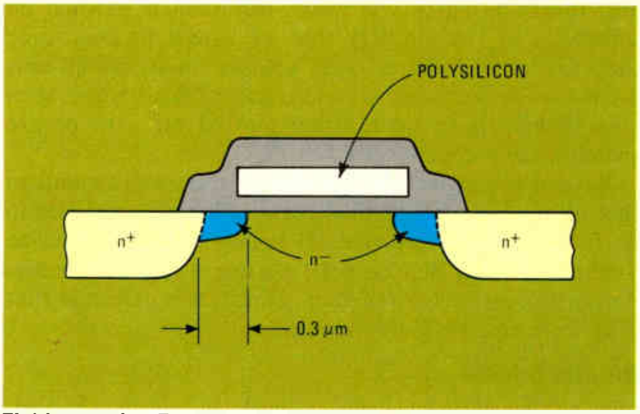
IBM Corp.'s Thomas J. Watson Research Center in Yorktown Heights, N. Y., is also investigating the prospects of bipolar technology for VLSI, and it has built subnanosecond integrated-injection/merged transistor logic (I^2L/MTL) circuits. It sees a need for both high-performance bipolar circuits with high-drive capability, such as ECL circuits, and low-power, high-density circuitry like its I^2L/MTL. It says judicious mixing of both circuit types will enhance the potential of bipolar technology in the VLSI era, and that further research is warranted because bipolar devices can be scaled down without suffering from punch-through and low gain.

Other variants of I^2L—integrated Schottky logic (ISL) and Schottky transistor logic (STL)—are on the drawing board at TI, Philips Research, and Fairchild. TI has stated it will introduce an advanced version of its STL process later this year that will enable subnanosecond gates that dissipate less than 250 microwatts. Research at Fairchild suggests that with 0.5-μm feature sizes, 300-ps injection-logic gates would result.

Since injection-logic gates are based upon output diodes, a method to shrink the diodes would compact the gate. TI is working on lateral diodes that might be suitable for its STL. They are formed with arsenic and boron implants that are adjacent in a strip of polysilicon also used for interconnections.

If these diodes work out, they could be placed over the gate for very high densities. In fact, since logical decisions in injection-logic gates are carried out via the output diodes, logic operations in such a structure would be accomplished entirely in the interconnection pattern.

IBM engineers have developed two circuit techniques to speed up bipolar gates. One, which makes use of saturated transistors instead of bulky capacitors for ac



Field spreader. To combat hot-electron injection and short-channel effects, IBM forms lightly-doped extensions to drain and source regions. The regions spread out the electric field and allow MOS field-effect transistors to operate with higher breakdown voltages.

coupling, has yielded a NOR circuit exhibiting a speed-power product of 0.4 picojoule. The technique is expected to transform, for example, a 20-ns, 2-to-3 watt memory chip into a 12-ns, 1.5-W unit while doubling its density. In logic, the idea may allow up to 10,000 0.15-milliwatt gates to be crammed onto one chip.

IBM's other bipolar circuit innovation is known as low-voltage inverter logic. Not only does it allows speeds twice those of ECL, it uses a fraction of the power. The basic embodiment of LVIL is a two-stage NOR circuit containing five transistors and three resistors; two capacitors could be added for even faster operation. With 2.5-μm layout rules, an LVIL gate approaches 350 ps at power levels under 2 mW; it seems a prime candidate for IBM's extensive gate-array program.

Gallium arsenide advances

Owing to the availability of high-quality starting materials and of maturing processing techniques, gallium-arsenide ICs are proliferating. There are no off-the-shelf LSI GaAs chips, but military and very high-speed proprietary applications are fostering superfast data and signal processors and memories. Although current work centers on depletion-mode or normally-on MES FET circuits, GaAs chips around the corner will employ both depletion- and enhancement-mode devices. Bipolar GaAs chips are also in the offing, thanks to controlled ion implantation, and work continues on GaAs metal-insulator-semiconductor (MIS FET) logic. Beyond these, progress is slow but sure in developing chips made of other III-V compounds, notably indium phosphide.

Two principal contributors to GaAs technology, Rockwell International Corp.'s Thousand Oaks, Calif., Electronics Research Center and Hewlett-Packard Co.'s Palo Alto (Calif.) Laboratories, continue to refine their depletion-mode processes. With its buffered-FET logic, HP will soon report on a medium-scale-integrated GaAs word generator that operates at a 5-gigabit-a-second data rate. Rockwell, with its Schottky-diode FET logic, has succeeded in constructing a 1,008-gate 8-bit GaAs multiplier that delivers a 16-bit product in 5.2 ns.

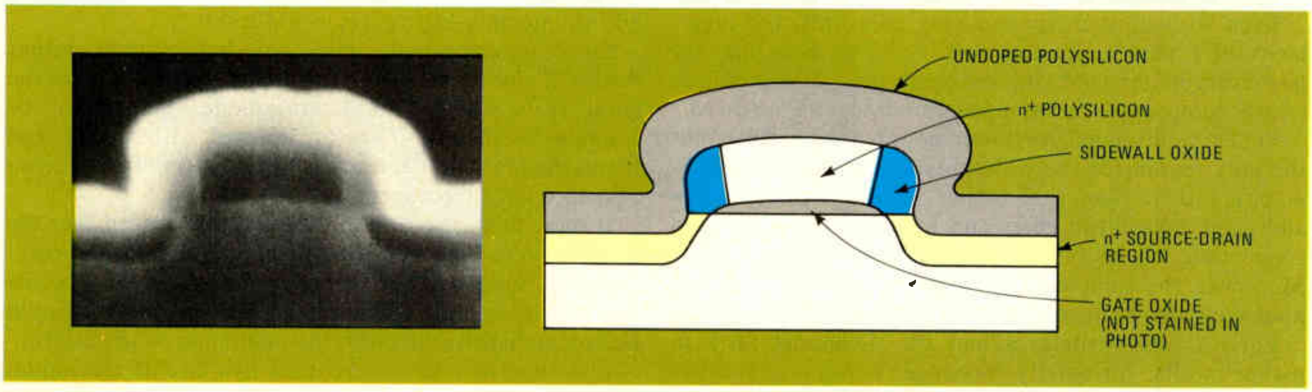
In addition, Rockwell is working on GaAs charge-coupled devices that might make possible subnanosecond information processing based upon 10^9 to 10^{12} equivalent multiplications per second. It has also built a GaAs 32-by-32-bit imaging array and bipolar circuits.

TI, too, has been cultivating a bipolar GaAs structure for over a year. One of the attractions of bipolar GaAs for the company is the ability to fashion I^2L-like gates, which in turn make for compact gate arrays.

Importantly, with GaAs chips that combine enhancement- and depletion-mode devices, many of the same principles used to design silicon chips can be directly applied. Static GaAs RAMs using enhancement- and depletion-mode devices were detailed late last year by the McDonnell Douglas Astronautics Co. and Lockheed Corp.'s Microelectronics Center.

Just as IBM improved silicon bipolar circuits with capacitive coupling, dense capacitively-coupled GaAs gates have been developed independently by British Telecom and the Electrotechnical Laboratory of Japan's Ministry of International Trade and Industry. Both designs require just two transistors and one Schottky diode per stage. The diode is reverse-biased to act as the coupling capacitor. The highly compact circuit requires no negative power supply, but it does need initialization and must be operated above a minimimum frequency.

The Japanese company most serious about GaAs technology seems to be Fujitsu Ltd. Using HP's buffered-FET logic, it has already built a gate array and wired it up into a 4-bit arithmetic and logic unit comprising nearly 1,000 GaAs FETs diodes. The chip consumes about a watt and completes operations in just over 2 ns. More-



Fully enclosed. Texas Instruments has devised this unique structure to make certain that drain-source regions do not undercut the gate electrode. Undercutting is avoided even if the drain-source implants diffuse due to subsequent higher-temperature processing.

over, Fujitsu says that by going from 2- to 1-μm channel lengths, subnanosecond delays will be possible.

Fujitsu does not hide the fact that it intends to use the GaAs technology for super-high-speed computer applications. To that end, it has also developed a GaAs circuit called HEMT, for high–electron-mobility transistor, that is so fast that it competes with Josephson junctions. The complicated structure is made up of alternating layers of intrinsic and doped GaAs so that electrons from the doped layers flow into the nondoped films and become extremely mobile. At room temperature, a HEMT switches in 50 ps, and Fujitsu feels that cooling will bring that down to 10 ps.

Where's Josephson?

Conference papers continue to be delivered on Josephson junctions, but the world still waits for some kind of computer based upon the technology. In the meantime, some useful circuits have been developed with Josephson junctions, like a 6-bit analog-to-digital converter from the National Bureau of Standards, which is capable of taking 2 billion samples a second.

IBM's Zurich Research Laboratory of Rüschlikon, Switzerland, has come up with a circuit called MAIL—for magnetically-coupled asymmetric interferometer logic—that combines galvanic isolation and logic operation in a single device that has triple the density found in earlier Josephson layouts.

Computer simulations of the new circuits, based upon 2.5-μm ground rules, suggests gate delays and power consumption figures of 25 ps and 5 μW, respectively. That works out to a power-delay product of only 125 attojoules—at least three orders of magnitude smaller than for silicon or GaAs devices.

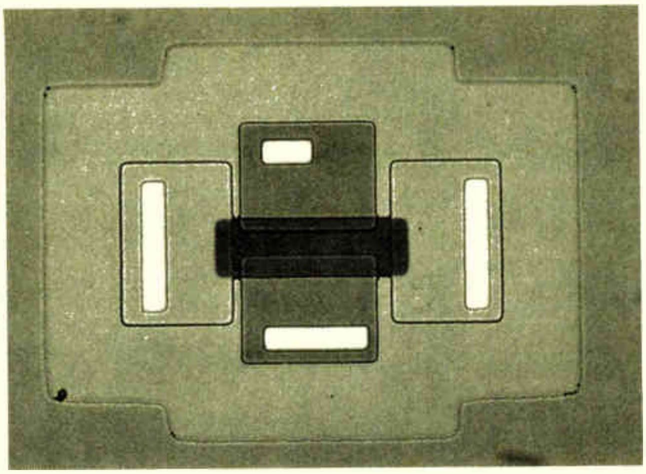
One of the more impressive yet unexpected announcements in the Josephson field came from Bell Labs. Scientists at its Holmdel, N. J., facility have patterned 1,000-Å-square junctions that reached the technology's natural switching speed of about 1 ps. In systems where wiring delays and heating effects come into play, such devices might render delays of less than 10 ps. To resolve such a minute structure, the scientists resorted to oblique-angle evaporation and a two-layer electron-beam resist to minimize overexposure caused by backscattering of the beam's energy.

Linear muscle

Process innovations will continue to push monolithic voltage regulators' capabilities to higher currents and voltages. National Semiconductor Corp. of Santa Clara achieved 10-ampere current levels with a linear process called Moose that borrows from discrete transistor design. The process puts n- and then p-type epitaxial layers on an n^+ substrate.

Contacts to the power transistors' collectors are through the back of the die, instead of from the top through a diffusion to the n-type subcollector. Moving the collector to the bottom of the chip is accomplished with a second collector diffusion step that shorts the standard subcollector to the substrate.

Besides giving a lower-resistance collector, this move frees the top of the chip for larger emitters that can



All merged up. An effort by the University of Waterloo and Bell-Northern Research resulted in the single-device-well MOS FET. Area is conserved by controlling perpendicular enhancement- and depletion-mode transistors with a single gate electrode.

handle increased current levels. Wire-limited current ratings are up to six times higher than previous IC regulators: over 30 A.

While National was pushing regulator current ratings, TI was developing the Bid-FET process to raise operating voltages to 125 V. The process merges precision control circuitry—fabricated from bipolar transistors—with C-MOS logic and high-voltage MOS FET output drivers in a junction-isolated chip. In contrast to commercially produced bipolar devices that can withstand only about 75 V, these devices can take up to 400 V. These FETs are double-diffused n-channel transistors, in which carriers flow laterally from source to drain.

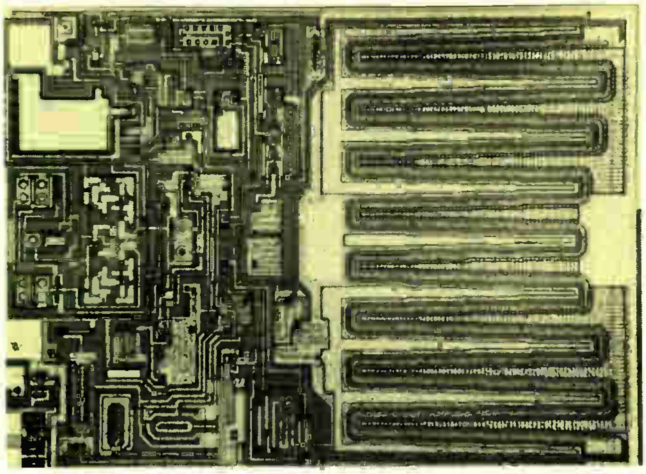
Power switching

Power semiconductor makers are increasingly exploring novel fabrication techniques and sophisticated testing techniques like infrared imaging to manage reliable designs at prodigious power levels. With FET technology having proved its performance advantages, users are watching for prices to come down. Both bipolar and MOS transistors are now handling 1-kilovolt levels, but thyristors are still called on above that point.

Hitachi stands alone with a high-frequency lateral power MOS FET that provides power gains in excess of 14 decibels at frequencies over 100 megahertz, beating both bipolars and vertical MOS FET and presaging the ascension of FETs into frequency-modulated transmission. The lateral design adds reliability by allowing incorporation of gate-protecting diodes and helps switching speed by minimizing the parasitic inductance in the source leads.

Other progress with FETs includes additions to International Rectifier Corp.'s Hexfet line that produces double-diffused vertical-MOS FETs with hexagonal sources and silicon gates. A 250-mil chip from the El Segundo, Calif., company stands off 500 V and conducts 10 A with only 0.4 ohm of on-resistance.

While many makers claim to have reached the 1-kV benchmark for power-FET breakdown voltage, Motorola appears to have been the first to get parts out to users. Initial offerings from the Semiconductor Sector in Phoe-



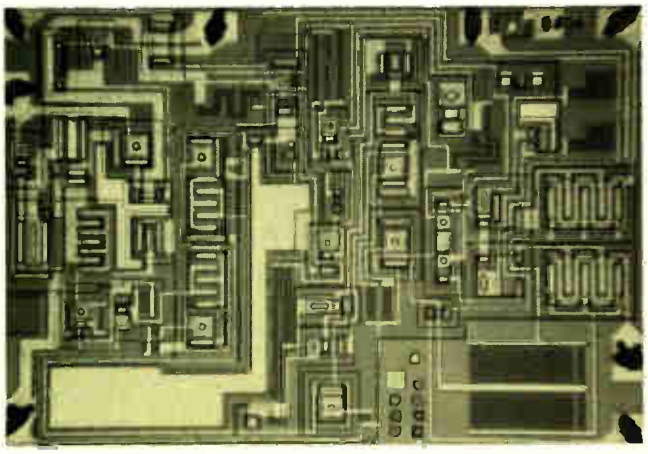
Strength in numbers. Merged processing technologies give Texas Instruments bipolar, C-MOS, and power MOS devices on one chip. The TL783 voltage regulator shown here uses bipolar control circuits and lateral MOS FET output devices for voltage ratings up to 125 V.

nix were rated at 1-A continuous drain current, 75-W dissipation, maximum on-resistance of 10 Ω, and switching times of 300 ns or better.

Besides looking more likely to displace bipolar transistors in switching power supplies and motor controllers, power MOS FETs are showing promise of on-resistance low enough to beat electromechanical relays in low-level switching. Teledyne Relays, the Hawthorne, Calif., subsidiary of Teledyne Inc., for example, used paralleled FET stages in a line of optically-coupled relays to reduce output resistance to 0.3 Ω.

Bipolars lend a hand

Despite the progression of FETs into low- and medium-power applications, bipolar technology is alive and advancing in the high-power arena. Merging bipolar and MOS transistors in a single device for power handling will continue to bring efficiency advantages to discrete semiconductors. Supertex Inc. of Sunnyvale, Calif., is following along the path forged by Siemens AG with Sipmos, by combining the high impedance of a MOS input with the low conduction losses of a bipolar output stage. A 245-mil-square chip with 40% of the area given over to the FET can provide sufficient drive current for a bipolar transistor that handles 20 A or more with only 0.3-Ω on-resistance.



Stable and balanced. Analog Devices' laser trimming of the JFET input stage on the AD547 precision operational amplifier limits the part's offset voltage to 0.25 mV, with 1 μV/°C drift. Automated probing and testing are the keys to drift trimming at the wafer level.

In bipolar devices' realm of unchallenged superiority—thyristor switches—ever higher power levels and improved reliability may finally be joined by the elusive gate-turnoff capability. NV Philips Gloeilampenfabrieken of Eindhoven, the Netherlands, appears to have achieved it in a 5-A, 1.5-kV device, and researchers at Toshiba and elsewhere are uncovering gate-turnoff failure modes by monitoring recombination radiation at infrared wavelengths during device switching.

AEG Telefunken of Berlin exported some improved silicon controlled rectifiers with reduced switching losses and turnoff times claimed in parts rated at up to 930 A of average on-state current and 2-kV blocking voltages. The npnp structures are bonded to a molybdenum disk, and gold contacts define the gate branches and cathode stripes in the top-side interdigitated metalization pattern. The cathode is contacted under pressure through copper and molybdenum plates and a silver template that touches the vacuum-deposited gold.

Analog domain

Despite the proliferation of C-MOS successes in data-conversion components, bipolar technologies will continue to compete because high precision may not be economical in C-MOS for a long time. While advances will be won in extending and improving the linear performance of C-MOS parts, data-conversion applications could well see a resurgence of bipolar technologies in processes that combine fast, accurate analog components with reasonably dense and cool logic.

A high-frequency bipolar process that also yields dense low-power logic circuits helped Advanced Micro Devices Inc. come up with the Am6108—an 8-bit a-d converter. The Sunnyvale, Calif., company's process calls for epitaxial-layer resistivity to be reduced to 1 Ω-centimeter, compared with 5 Ω-cm in a standard linear sequence, and its thickness trimmed down to 4 μm. Combined with a narrow basewidth, the thin epitaxial layer allows npn transistors to reach cutoff frequencies of as much as 1.5 gigahertz.

Polysilicon resistors further enhance linear performance, since they have virtually no voltage coefficient and lower parasitic capacitance and temperature coefficient than do resistors implemented with base diffusions. The same linear process is used in a family of circuits, dubbed linear differential logic, that is similar in operation to ECL but requires one fourth the power and one third the area for comparable or better speed. The advantages are won at the price of a reduction in logic swing from 700 mV to 130 mV that reduces noise margins accordingly.

In the purely analog realm, the continuing trends are toward refinements of the combined JFET-bipolar technologies that improve input stage specifications and toward extensive use of wafer-level trimming techniques. In a forward-looking move that brings the advantages of systems-level integration to analog signal processing, Precision Monolithics Inc. of Santa Clara introduced a chip designed to handle a variety of common tasks, such as full-wave rectification, absolute-value generation, and synchronous demodulation.

Dubbed the GAP-01, this 8,600-mil² chip includes two differential-input transconductance amplifiers, TTL-controlled low-glitch switches, a precision comparator, and an output buffer. These elements get good offset and drift characteristics through the use of the zener-zap technique, in which zener diodes are selectively shorted across resistors during testing.

Zeners and lasers

Zener trimming at Precision Monolithics has progressed to the point where a monolithic buffer like the BUF-03 can be operated open loop to get slew rates up to 300 V/μs. The design uses a JFET input stage with a 2-mV offset and precise level-shifting circuits to eliminate the capacitors usually invoked for stable operation of a feedback-controlled amplifier.

Zener diodes for voltage-reference circuitry are increasingly being fabricated as buried junction devices, in which breakdown occurs well below the wafer surface. The conventional zener, implemented with a transistor's base-emitter junction, is subject to long-term drift due to surface imperfections of the crystal and contamination from mobile charge in the oxide.

The buried junction is isolated from these surface effects, and can be stable to within 50 parts per million per year. Analog Devices Inc., Norwood, Mass., has used the technique extensively in 10- and 12-bit data converters, and Burr-Brown Research Corp., Phoenix, called on buried zeners for its DAC800—the first monolithic version of the hybrid DAC80 12-bit d-a converter.

JFET-input operational amplifers will continue to receive much attention because they can lead to very low requirements for input bias currents, without at the same time increasing the input noise voltage—an inevitable trade-off in bipolar designs. The key to their evolution will be laser trimming techniques that reduce their offset voltage and drift.

Indicative of the present state of the art is the AD547, a JFET-input amplifier from Analog Devices that is specified with a maximum offset voltage of 0.25 mV and offset drift with a temperature of 1 μV/°C. At the same time, the typical voltage and current noise figures at 10 kilohertz are a low 25 nanovolts and 0.003 pA/Hz$^{1/2}$, respectively. Refinements in device geometries and processing that can increase JFET transconductance promise to reduce noise voltages even further.

The static induction transistor originated with Nishizawa

Jun-ichi Nishizawa is famous in Japan for incessantly pushing for more original fundamental research and for development based on that research. Especially now that the semiconductor industry is large and prosperous, he says, it can afford to make some of its own mistakes rather than following the lead of the U. S.

Nishizawa has ample opportunity to put his ideas into practice because he is both a professor at the Research Institute of Electrical Communications at Tohoku University and research manager at the Semiconductor Research Institute—a private laboratory funded by contributions from industry and contract research. Furthermore, he often acts as a consultant to industry, and several firms have made use of loans from the Research Development Corp. of Japan—which is sponsored by the government's Science and Technology agency—to develop products based on Nishizawa's ideas.

Much of his present work is based on one of his earliest ideas, from 1950, for which he was granted a Japanese patent, on electrostatic injection control. Early on, he used it to build p-i-n power rectifiers, photodiodes, and avalanche photodiodes, and p-n-i-p and n-p-i-n transistors—which are the actual configurations of most modern transistors made by diffusion.

Also proposed by Nishizawa as part of the same work—but not producible at that time—was the static induction transistor, a type of field-effect transistor whose drain current does not saturate with increasing drain voltage. He points out that he specified fabrication by ion implantation two years ahead of Shockley and heat treatment (a step that Shockley failed to mention).

Present applications of the SIT principle range from logic to a 500-ampere-peak, 4-kilovolt thyristor with a gate turnoff time of 5 microseconds. Still the search for a wider range of applications goes on, and four new development projects based on the SIT principle will be funded for a five-year period starting about November by the Research Development Corp. Among other projects, Nishizawa's group at SRI will develop low-power static induction tunnel-injection transistors (SITT) in gallium arsenide with a maximum frequency of several terahertz.

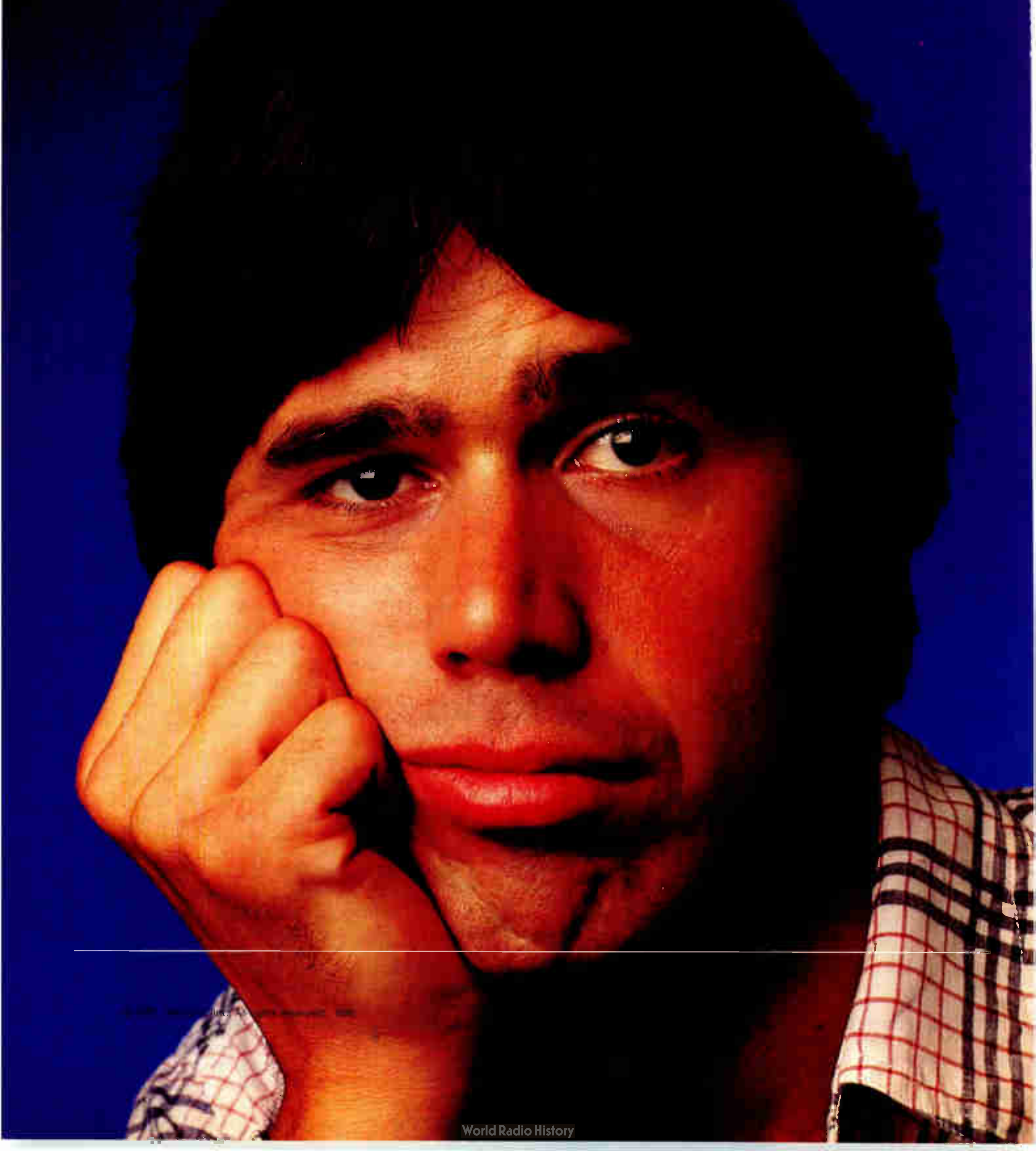
Nishizawa also developed the vapor-pressure control method of epitaxial growth for the fabrication of light-emitting diodes, and it is now used commercially for high efficiency super-high-brightness devices. He also pioneered vapor-phase photoepitaxial growth, which was included in two U. S. papers at the recent Hawaii conference on very large-scale integration.

His 1957 injection-laser-diode patent was one of the earliest in this technology, but Nishizawa did not succeed in securing commercial development. He also did pioneering work in graded-index fibers for optical transmission and in high-efficiency varactor diodes for electronic tuning and modulation. Also to his credit is a positioning system with a precision of better than 0.1 micrometer for an optical pattern generator for mask fabrication.

An outcome of his engineering work is an interest in classical music, which ranges from Gregorian chants to Bach. His amplifier features static induction transistors, and Nishizawa says that there are only two persons in the world who can listen to music on transistors they developed—Shockley and himself. **-Charles Cohen**

TEK 8540 INTEGRATION UNIT

For the designer whose computer can't help him debug his microcomputer software.



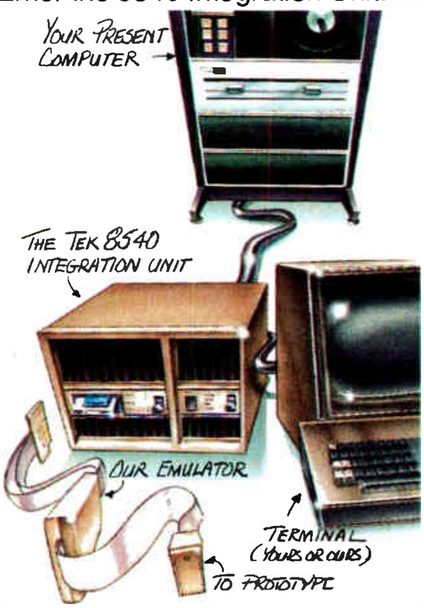
Tek announces the 8540 Integration Unit.

When designing with microcomputers, your resident host computer can be a powerful ally in the fight against impossible design schedules.

But, ultimately, it only gets half the job done.

Even though it gives you everything you need for fast, accurate code development, you still have to install and debug your developed code in the prototype hardware. A process that often consumes half your total design time.

Enter the 8540 Integration Unit.



When it comes to hardware/software integration, Tektronix has the answer. The 8540 Integration Unit. It interfaces easily with almost any host computer using ASCII terminal communications. And, once connected, its high-performance emulators and debug software handle the entire integration process.

All with an unmatched range of chip support.

Your host & the 8540: A synergistic team.

The 8540's sophisticated interface features make the most out of your host's processing power. Like the ability to download symbolic debug tables along with object code to the 8540. Or permanently store your specialized, host-oriented debug commands aboard the 8540 as either key words or command strings.

Breakpoint halts program execution at the address label "LOOP." Also shown is a detailed description of the processor's internal status at the breakpoint.

To retain any terminal-oriented command structures you've developed, the same terminal can be used for direct communication with either the 8540 or the host system. There's even a local printer interface on the 8540 so its printing operations won't burden the host.

A Trigger Trace Analyzer for real-time prototype monitoring.

In many applications, the timing of code execution becomes critical. To fully support real-time debugging, the 8540 includes an optional Trigger Trace Analyzer. It has four trigger channels ready to track down even the remotest sections of code execution.

You can do things like identify all non-ASCII writes to an I/O port. Or count the number of calls to a specific subroutine. Or measure the elapsed time of an interrupt handler routine.

Chips The 8540 I.U. Supports:		
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Let the 8540 finish the job your computer started.

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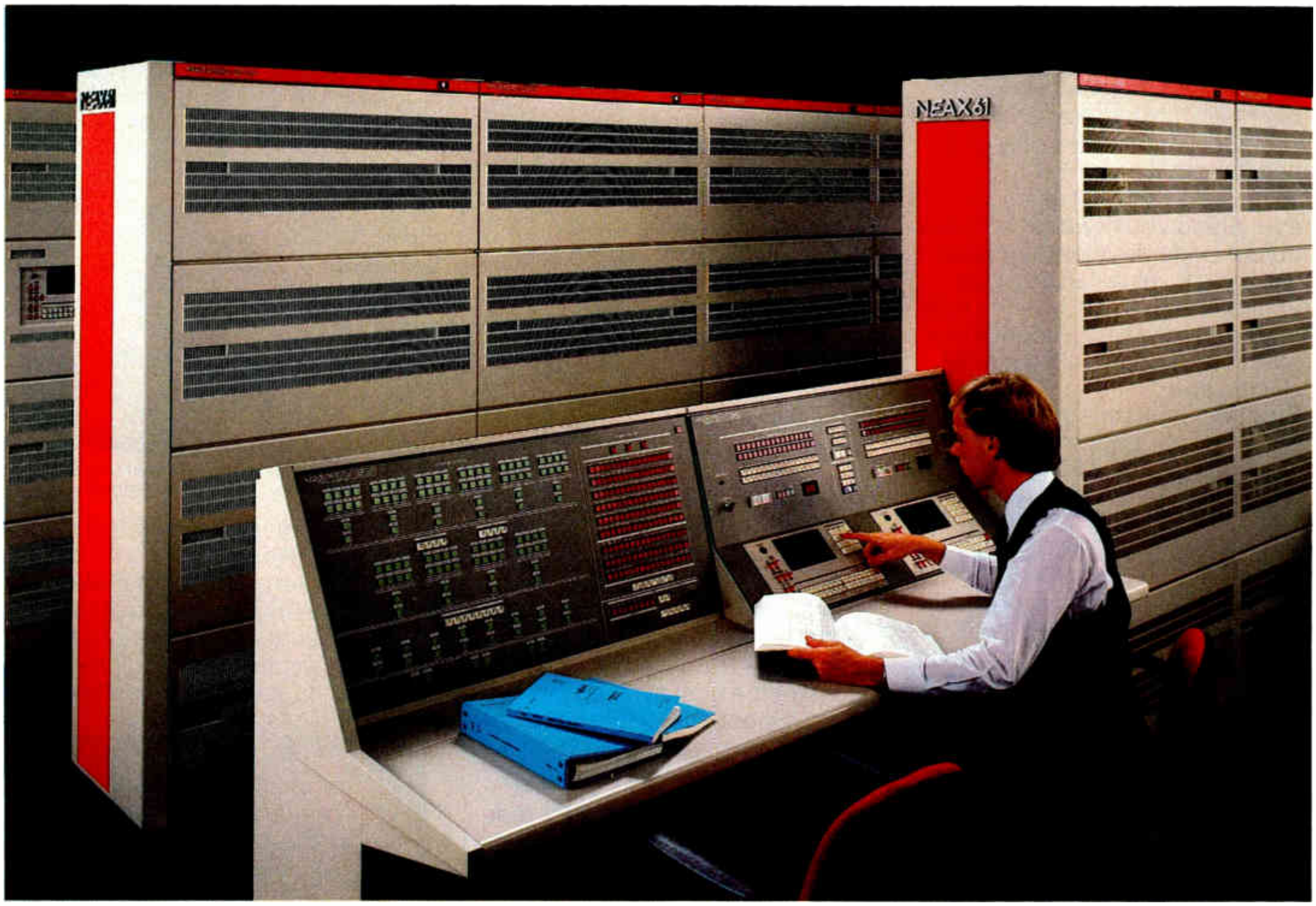


NEAX61 WILL SERVE TWO MILLION SUBSCRIBER LINES IN MALAYSIA

In 10 years, Malaysia expects to have a nationwide digital telephone network with some 3 million subscriber lines.

A contract to supply and install on a turnkey basis NEAX61 digital switching systems for about 2 million subscriber lines has been awarded to PERNAS NEC Telecommunications SDN, BHD (PERNEC) by the Telecommunications Department, Government of Malaysia. PERNEC is a joint venture between the PERNAS Group, a state-owned corporation of Malaysia, and NEC.

The NEAX61 is one of the most advanced stored-program-controlled digital switching systems. The NEAX61 can be used as a local, toll, tandem, remote, mobile, and international gateway switch, and can handle up to 100,000 subscriber lines. It owes its flexibility primarily to its building-block configuration. Intensive use of LSIs and ICs contributes greatly to its reliability and space-saving dimensions.

With the Malaysian contract, NEC has become the world's leading manufacturer/supplier of digital switching systems. NEC has installed, or is set to install, NEAX61 systems in 17 countries for the equivalent of approximately 3,600,000 subscriber lines in all.

NUMBER 120

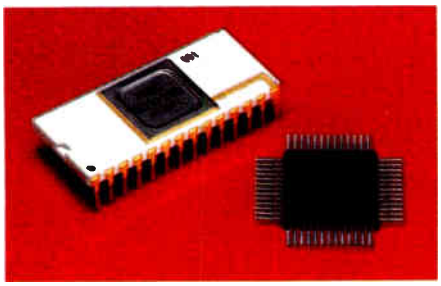
WORLD'S FIRST 128K BIT N-MOS AND C-MOS ROMS

Two new large capacity high-speed mask ROMs from NEC represent the first of their kind in the world.

The n-channel MOS ROM—μPD 23128D—has a memory capacity of 128K bits and features a fast access time of 250 nanoseconds. The μPD23128D, in a standard 28-pin ceramic DIP, operates on a single 5-volt supply with maximum power consumption of 275mW (82.5mW during standby time).

The other product, μPD73128G, is a C-MOS device which also has a memory capacity of 128K bits. It comes in a 52-pin plastic flat package, has an access time of 5 microseconds and operates on a single 5-volt supply with power consumption of 22mW (11 microwatts during standby time).

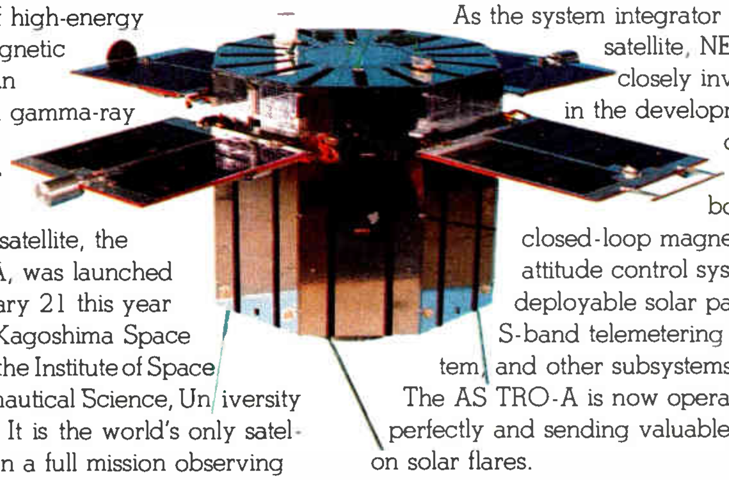
The requirement for large capacity ROMs is constantly increasing in such applications as computer terminals and communications equipment, to



enable such systems to become ever more compact and cost-effective. NEC's two new devices, already in production, completely satisfy these requirements.

NEC-EQUIPPED SATELLITE OBSERVES SOLAR FLARES

Every eleven years, the frequency of explosions on the sun's surface increases. These explosions, or "solar flares", release a great amount of high-energy electromagnetic radiation in X-ray and gamma-ray regions.



A solar flare observation satellite, the ASTRO-A, was launched on February 21 this year from the Kagoshima Space Center of the Institute of Space and Aeronautical Science, University of Tokyo. It is the world's only satellite now on a full mission observing the sun, which is presently in a period of maximum activity.

The ASTRO-A weighs 188kg. It is now in a semicircular orbit with a perigee of 480km, apogee of 640km, and inclination of 31.5 degrees. The spin-axis of the ASTRO-A is controlled to point the sun for observation of its surface with a solar X-ray telescope, solar X-ray crystal telescope, solar gamma-ray instrument, etc.

As the system integrator of the satellite, NEC was closely involved in the development of the on-board closed-loop magnetic attitude control system, deployable solar paddles, S-band telemetering system, and other subsystems.

The ASTRO-A is now operating perfectly and sending valuable data on solar flares.

SARAWAK GAS, OIL FIELD GETS OFFSHORE TELECOMS NETWORK

NEC is to install an integrated offshore telecommunications network in Sarawak, Malaysia.

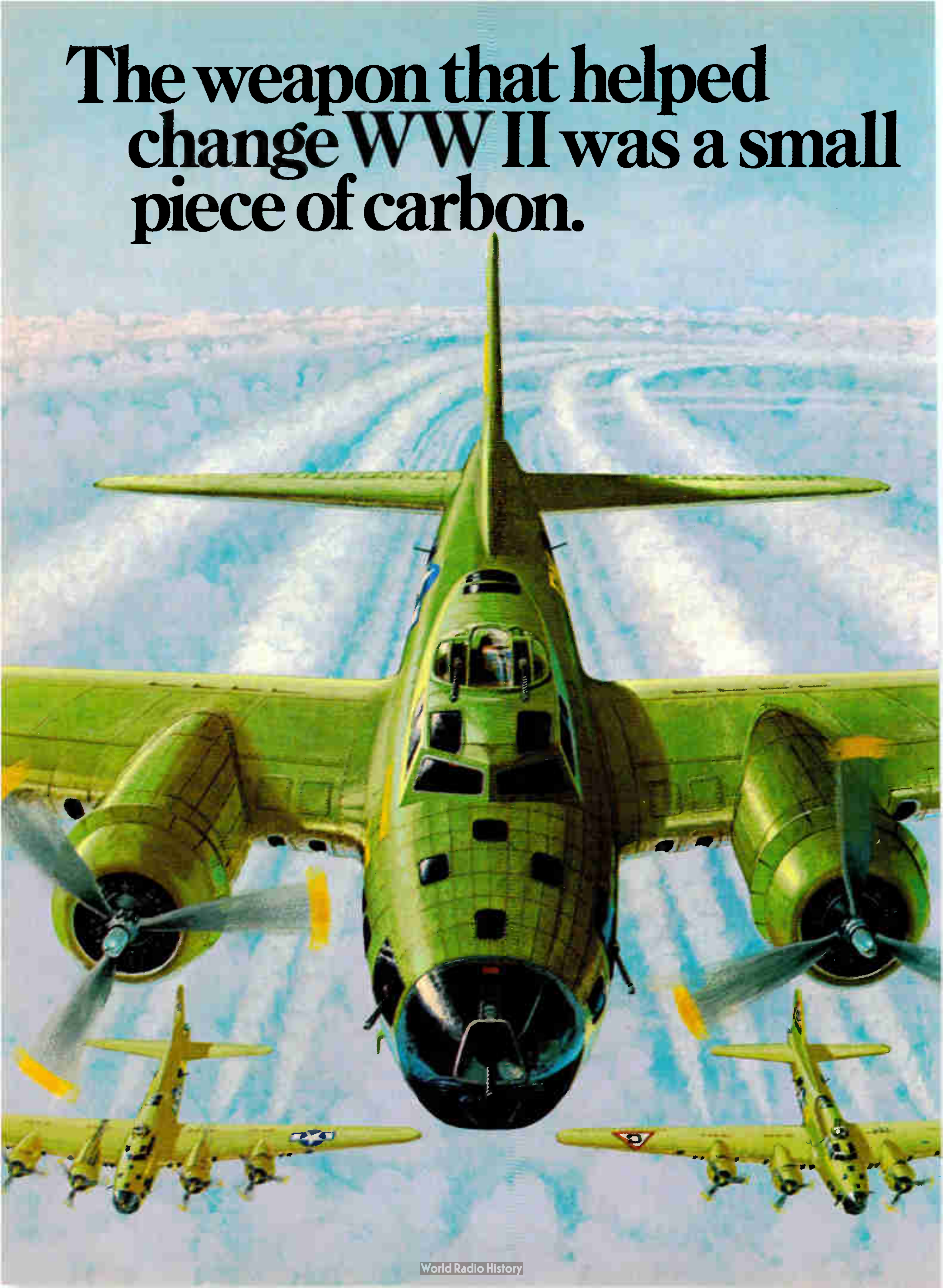
The network, ordered by oil producer Sarawak Shell Berhad, will include almost all types of telecommunications systems. The onshore terminal at Bintulu will be linked with offshore oil and gas platforms some 130km away by means of a 900MHz troposcatter radio communications system. Offshore platforms will be interconnected by a 2GHz line-of-sight microwave communications system.

In addition, the network will have subscriber VHF radio telephone systems between a platform and associated drilling rigs, air-to-ground VHF radio systems, ship-to-ground VHF radio systems, public address systems, hot-line telephones, subscriber telephones (explosion proof type), radio beacons, teleprinters, and private automatic branch exchanges.

Construction is scheduled to be completed in December 1982.

NEC

Nippon Electric Co., Ltd.
P.O. Box 1, Takanawa, Tokyo, Japan


The weapon that helped change WW II was a small piece of carbon.

The strategy was sound. Fly higher. Get above the limits of the fighters. Get beyond the range of the ground batteries.

But the wild blue yonder is a forbidding place. It's colder and drier than you can imagine. So, as our aircraft tried to fly higher and higher, they soon had to come right back down. The generator brushes were rapidly wearing away to dust in the superdry air of the stratosphere.

We went to work on the problem. And, in 1942, Stackpole helped perfect the first high-altitude aircraft brushes. To shorten a war. To pave the way into space.

Application before answer.

We cite this bit of history for two reasons. One: because we're proud of it. And two: because it's a good example of how we work. Every day.

A lot of companies come up with a product, then look for needs or applications where it *may* fit. We work the opposite at Stackpole. Someone has a need or application, then we come up with the product that *will* fit.

What and how are inseparable.

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We know the what: carbon and graphite in powder, bulk and fiber forms; ceramic ferrites; precious metals; and powder metallurgy.

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Put both to work.

We apply this know-how to brushes, billets and mold stock. To carbon fibers, foil and fabric. To machinery and powdered metals. To switches, resistors and ferrites.

Next time you have a specific need, call our application engineers. For the product that fits. In the meantime, get to know our resources better. Call or write: Dauer Stackpole, The Stackpole Corporation, St. Marys, Pa. 15857. (814) 781-1234.

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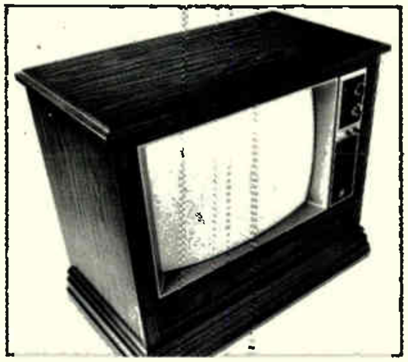
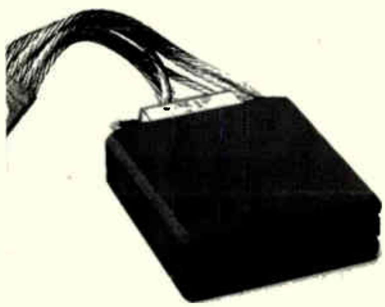
Our workday runs from 1906 through tomorrow.

Once, someone needed a ceramic resistor for spark plugs. To make the car radio a static-free reality. We now make millions of such resistors every week.



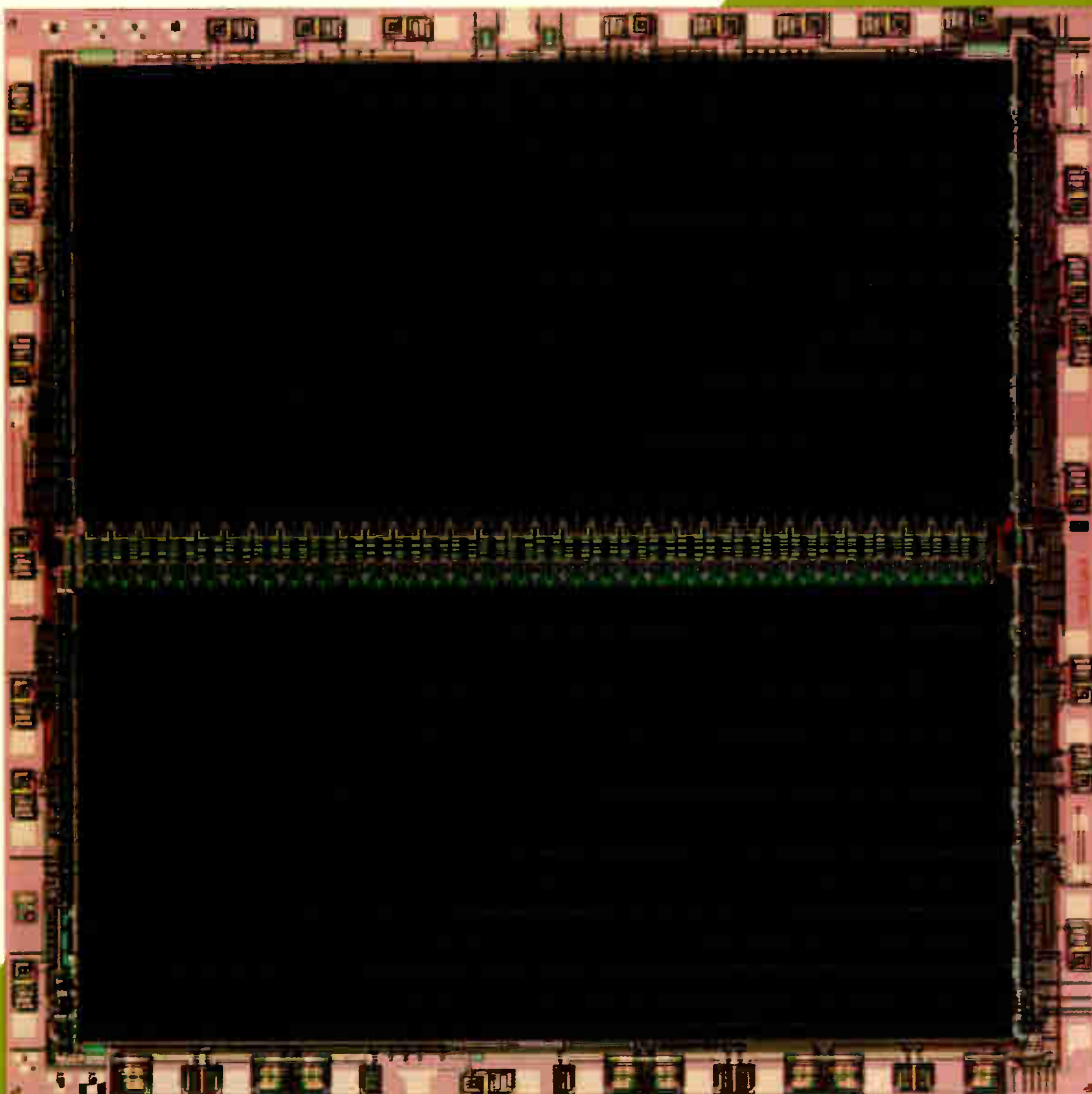
Once, someone wanted to move the television set from the laboratory to the living room. But it had to be safe. We helped develop the ferrite flyback transformer core. Today, our ferrite cores are in millions of TV sets and switch-mode power supplies, worldwide.



Once, someone needed a railroad brush suitable for both heavy freight and high-speed commuter traffic. Today, our wafer brushes are in thousands of diesel locomotives.

Circle 129 on reader service card

MEMORIES



Four for a million. This 256-K read-only memory from Hitachi is one of many developed by Japanese semiconductor manufacturers. Like others from Hitachi, Toshiba, and Sharp, it is built with complementary-MOS technology. Die size is 37 mm^2.

The 64-K RAM is slow to mature, but redundancy may cure some of the yield problems; and while C-MOS improves static RAMs, bubble prospects appear bleak

by John G. Posa, *Solid State Editor*

☐ Redundancy is all the rage for large semiconductor memories, whether they are dynamic and static random-access memories or electrically- and ultraviolet-light-erasable read-only memories. The mechanisms of programming the spare elements and the density level at which the spares become cost-effective are, however, both points at issue. Only a handful of companies are yet able to ship their 64-K RAMs, and firms not even on that list have displayed quarter-megabit devices. The quest for the ideal self-refreshing pseudostatic RAM goes on though recent steps appear headed in the right direction. Complementary-MOS technology is enhancing the specifications of fully static RAMs, and metal silicides promise to do the same for all component types.

In the nonvolatile area, 256-K ROMs abound in Japan; market development in the U. S. is being discouraged by the 64-K ROM price wars. MOS erasable programmable PROMs are selling amidst fierce competition, and bipolar PROMs are gaining in density from vertical structures. EE-PROM shipments have yet to really take off, and most of the U. S. magnetic-bubble memory suppliers have quit the business.

Double is less trouble

For each memory type that now incorporates redundancy, there is a corresponding version of that chip from another vendor who maintains that the feature is unnecessary. Intel, Inmos, Mostek, and Western Electric use redundancy in their 64-K RAM and submit that competing will be difficult at best without it. However, Texas Instruments, Motorola, and Hitachi, to name a few, did not put the extra bits on their 64-K chips—a reminder that, historically, the highest yields come from the smallest dice.

So far, those companies that voted down redundancy are winning the race to volume production. But mature production of the 64-K RAM is years away and a lot can happen before then, as may be learned from the growth of the 16-K market. The memory makers with redundancy counter that when they ramp up, their rise will be swift, and they will surpass the companies who elected to go the conservative route.

For the 256-K RAM, however, there is almost unanimous agreement that redundancy is an absolute must. Unsettled, though, is whether electrical fuses or laser targets will make the best programming elements for removing bad memory cells. Western Electric and Mostek use lasers; Intel and Inmos use fuses.

Electrical fuses have many advantages, but in the long run, their biggest asset may be the possibility of programming after packaging—be it by the manufacturer or user. Lasers offer design flexibility. Because the links need no power or support devices, they take up little area and may be placed anywhere—Mostek Corp., Carrollton, Texas, has located them right in the middle of its 64-K RAM chip.

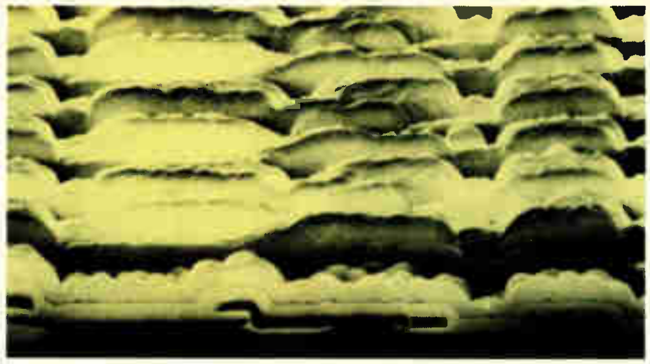
It may turn out that manufacturers will use more than one redundancy programming method at a time, depending upon the type of device. Memories already equipped with floating gates or another kind of nonvolatile element may do well to use these as programming cells by virtue of their availability. Japan's Hitachi Ltd. thought about a fast static RAM with high-resistance polysilicon loads and with redundancy programmed by hitting some of the same load devices—purposely placed in the chip's periphery—with a laser beam. The beam heats up the link and the dopants diffuse in and lower its resistance. This is a clever idea, but only for memories that have high-resistance polysilicon loads available.

Even though Japanese RAM manufacturers say that redundancy will make sense at the 256-K level, the feature either is lacking in all but one of the devices displayed by them or is being kept under wraps. (It is said that Fujitsu Ltd.'s 64-K RAM has redundancy that has yet to be invoked.) Nippon Telegraph & Telephone Public Corp.'s Musashino Laboratory has been involved in the design of at least two 256-K RAMs. The first has redundancy; but the second, a recent cooperative effort with Nippon Electric Co., does not. An earlier design from NEC did not sport spares, nor do the 256-K RAMs on which Toshiba and Mitsubishi have leaked details. Oki Electric did, however, recently pop up with a 256-K dynamic RAM incorporating extra rows and columns.

There will undoubtedly be more than one generation of the 256-K RAM. Manufacturers of the 64-K RAM have taken more passes at its design than they would like generally known—some are still tweaking their layouts. The 256-K RAMs so far discussed will probably be revised—in some cases almost completely—before full-scale production begins. The 0.25-Mb RAMs that have been talked about openly seem to be exercises in scaling down. About the only surprise is their reliance on metal or silicide gates, but performance requirements all but mandate that as well.

However, Texas Instruments Inc. and other companies speak of a second-generation 256-K RAM that will have a genuine one-device cell—not a transistor and a capacitor. The Dallas company, for example, keeps looking at

IBM's biggest. With this experimental 288-K random-access memory, IBM showed that U. S. companies, too, can show off very large memories not necessarily intended for production. The 32-K-by-9-bit unit has only twice the area of IBM's 72-K chip.



Close up on Mostek. This scanning electron micrograph shows top and cross sections of Mostek's 64-K dynamic RAM. Unique to its design is the use of polysilicon bit lines, grounded capacitor plates, mid-level sensing, and redundancy programmed with a laser.

the taper-isolated cell that it pioneered, and it likes what it sees. At the Very Large-Scale Integration Conference held last month in Maui, Hawaii, TI described a fully decoded 5-volt dynamic RAM that managed a tiny 140-square-millimeter storage cell using 4-micrometer design rules. The 512-bit chip sported an access time of 85 nanoseconds.

Similarly, NEC seems satisfied with a double-diffused cell that IBM Corp., Armonk, N. Y., claims to have invented. Interestingly, the structures proposed by both NEC and TI require a lightly doped well. Put another way, both approaches call for a C-MOS process. This means that both designs should also benefit from the more efficient sense amplifiers, decoders, and other peripheral circuits possible when both n- and p-channel devices are available.

Pseudostatics still sought

The perfect self-refreshing dynamic RAM—one with one-transistor cells but that appears completely static to the user—remains an elusive goal. At the 1981 International Solid-State Circuits Conference, Mostek offered a compromise: a fully static 32-K RAM with three transistors per cell. The idea, reminiscent of a similar proposal made some years ago by American Microsystems Inc., Santa Clara, Calif., is to use a charge pump to overcome a transistor's leakage current and thus keep a node storing a logical 1 high. Mostek said it was going to introduce a commercial product based on this principle sometime this year, but has yet to do so.

At least three manufacturers will, however, produce 32-K pseudostatic RAMs. Zilog now offers such a chip, and National has agreed to act as an alternative supplier for it. In addition, Intel Corp., Santa Clara, Calif., mentioned a 32-K pseudostatic RAM at ISSCC '81. All these parts demand some sort of sacrifice from the user to avoid contention between on-chip refreshing and external accesses.

In addition, Mostek, Motorola, Inmos, and—with its latest redesign—Fujitsu have self-refresh modes on their 64-K dynamic RAMs, but demand for this feature has not been hot. Apparently the big accounts that use RAMs in a big system require a more global refreshing scheme.

In a sense, pseudostatic RAMs and the self-refreshing 64-K dynamic RAMs are after the same thing: an easy-to-use memory with a lower cost per bit. Maybe both camps will converge on the same solution. The newer attempts do offer more design flexibility, and the concept in general becomes more practical as densities quadruple. Thus, a healthy market for such parts will develop despite their lukewarm welcoming.

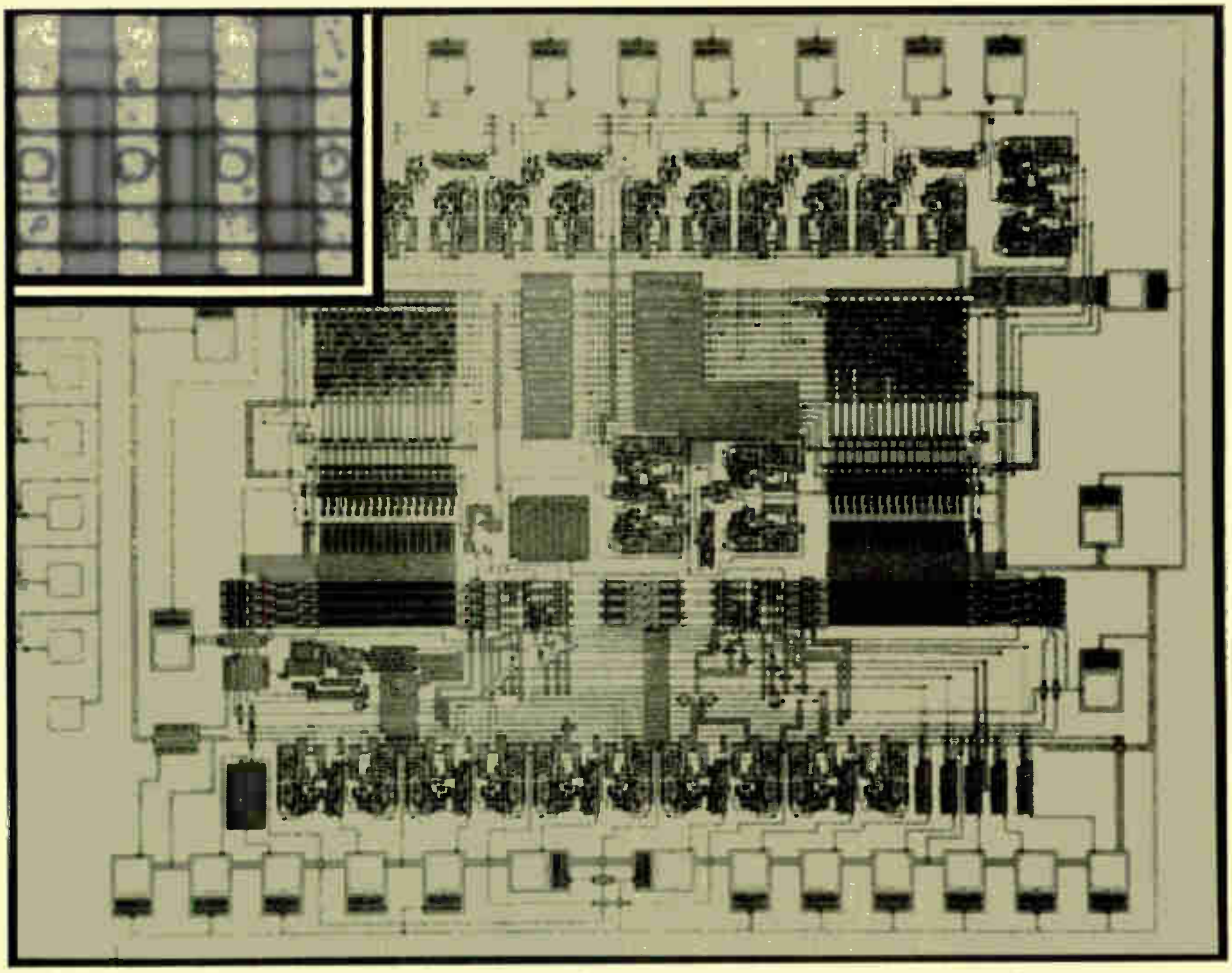
Statics mean action

Perhaps subtracting from the enthusiasm for pseudostatic devices is the incredible performance and density advances and price reductions of fully static RAMs. They have hit the 16-K level. TI, Mostek, Intel, Inmos, Hitachi, NEC, Oki, Mitsubishi, Toshiba, Harris, and even Honeywell's Synertek subsidiary claim to have a 16-K static RAM. Some of these companies will offer more than one chip organization. And some, like Japan's Toshiba Corp., even offer n-channel and C-MOS versions. Toshiba's n-channel version, organized into bytes, already costs $9.95 in volume. At that price, the market may not be large enough for all these firms.

But there are actually two different markets: one for the fast devices, having 1- and 4-bit organizations to replace bipolar units, and another for the slower, byte-wide chip market intended mainly for microprocessor applications. Some of the circuit innovations found on 16-K static RAMs include TI's column sense amplifiers to speed up its 16-K-by-1-bit version and the Datasave mode used by Mostek to lower the power dissipation on its 2-K-byte memory.

Not only does Mostek's 16-K-by-1-bit static RAM feature an efficient sense amplifier that facilitates half-row selection, it also has a novel roll-call function that lets a user find out which columns have been replaced with redundant spares. NEC's 16-K-by-1-bit static RAM will use pure molybdenum to short out long polysilicon word lines to obtain a 25-ns typical access time. NEC also uses boron to form a p-type well under each storage node to sweep away unwanted charge like that generated by alpha particles.

The most spectacular MOS speed advances over the year have come on 4-K static RAMs—C-MOS RAMs, at that. Toshiba, Hitachi, and Intel brought out 18-ns 4-K chips at ISSSC '81. Toshiba attained the speed with a sapphire substrate and molybdenum-silicide gates, Hitachi by scaling down and using feedback sense amplifiers,



A possibility. Texas Instruments seems to be nearing commercial application of its very dense taper-isolated dynamic RAM cell (inset). It recently announced the completion of the fully decoded 512-bit array (depicted above) and measured a 100-ns access time.

and Intel with an n-well process that favors the circuit's high-performance n-channel transistors.

All of these designs may have been test vehicles, though. Hitachi said that its process was really slated for a 64-K static RAM, and Intel is said to be more interested in building a micropower 2-K-by-8-bit unit like Toshiba's TC5516. Intel's C-H-MOS—its high-performance C-MOS process—uses fully static six-transistor cells for a standby power dissipation of 50 microwatts. Toshiba maintains it can sell its silicon-on-sapphire memory at a competitive price. If so, it will be the only semiconductor manufacturer to make a commercial success of SOS.

The blue ribbon for speed, however, goes to NTT's Musashino Laboratory for its 2.7-ns 256-by-4-bit emitter-coupled logic static RAM. As might be expected, NTT used local oxidation and polysilicon for what NTT calls a super-self-aligned technology. Directly responsible for that performance is a submicrometer base width, formed as impurities diffuse down from a 2-by-2-μm doped polysilicon emitter. The design also includes a look-ahead sense amplifier that trims word-line delay by about 15% yet increases the chip's 0.5-watt power usage by only 3%. The concern estimates that with emitters of 1 μm on a side, 1-ns access times can be reached.

Static RAMs are also benefiting from improved current-mode bipolar technologies such as integrated injection logic. Researchers at IBM's Yorktown Heights, N. Y., and Böblingen, West Germany, facilities continue to improve their combined I^2L and merged-transistor-logic memory cell. One of the latest results is a 25-ns 16-K static RAM. IBM split the emitters once common to the two cross-coupled npn storage transistors in the cell and connected them to individual resistors. As a result, the voltage developed across the resistors became a more substantial basis for sensing cell data, and this factor raised performance.

Over 100,000 elements

Several Japanese companies have unveiled 64-K static RAMs. These sneak previews parallel those given of the 256-K dynamic RAMs from Japan. The 64-K static chips completed by NEC, Toshiba, and Matsushita integrate more than 100,000 circuit elements yet in no case has redundancy been mentioned—nor have metal gates or silicides, one of which seems needed here. The points of note in these designs include the use of n-well C-MOS by

Matsushita Electric Industrial Co., Osaka, Japan, and the 64-K-by-1-bit organization of NEC's part and its intended 16-pin package.

NEC does not intend to go after high-speed bipolar memories with this arrangement. Instead, the chip is pinout-compatible with the 64-K dynamic RAM. NEC says that at very high density levels, a static cell will be the only answer to alpha particles and external noise; besides, the 24- and 28-pin packages now proposed for the big byte-wide memories work against the advantages of the high on-chip bit density.

Toshiba seems to be pushing its 64-K static RAMs the hardest—it plans to build three different 8-K-by-8-bit devices to cover all bets. One will be n-MOS for the smallest chip and the lowest cost but not the lowest power dissipation. Another will be all-C-MOS; Toshiba expects that this version will measure about 64,000 mil^2 but consume only 5 μW when idle. The third version, the last to be introduced, will have C-MOS peripheral circuits and an n-channel array that uses polysilicon load resistors. This will afford a die size and power specifications intermediate between the other two designs. As with the 256-K dynamic RAM, no U. S. manufacturer has yet stepped forward with a 64-K static memory.

Another compromise

Just as pseudostatic RAMs attempt to borrow the best features of static and dynamic RAMs, nonvolatile or shadow RAMs try to integrate the best of static RAMs and PROMs. There has been action in nonvolatile RAMs lately, possibly due to the crowded conditions that exist with standard memory types.

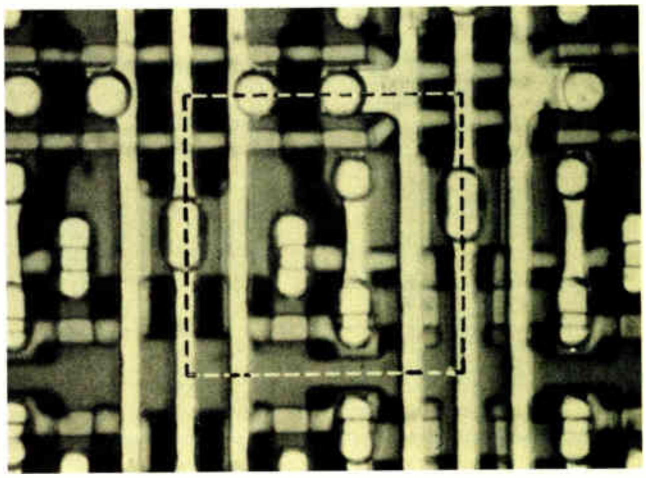
Xicor Inc., Sunnyvale, Calif., brought new life to the nonvolatile field with its 5-V-only 1-K-by-1-bit chip that is two years old. Since then, it has brought out similar chips of different sizes and organizations. Moreover, NCR Corp., Dayton, Ohio, has introduced a 4-K device that uses nitride for storage, while Hughes Aircraft Corp., Newport Beach, Calif., is hinting that it may build Xicor-like parts in C-MOS, and Intel has threatened to break into the nonvolatile RAM business.

All of the known nonvolatile RAMs tack a nonvolatile storage cell onto a fairly conventional cross-coupled flip-flop static RAM cell. Xicor uses a floating gate programmed by means of an extremely thin tunnel oxide. To judge by some of their other chips, it seems likely that if Hughes or Intel enter the business, they will do the same. NCR's decision to go with nitride for its nonvolatile RAM supports the notion that polysilicon floating gates are not necessarily the definitive way to get programmable nonvolatility.

Intel and Hitachi are still the only two chip makers out there with 2-K-by-8-bit EE-PROMs. The one from Intel uses floating gates; Hitachi's stores charge on a nitride-oxide interface; and the overall specifications of the two devices are comparable. Motorola Inc., Phoenix, Ariz., and General Instrument Corp.'s Microelectronics division, Hicksville, N. Y., are also poised to announce byte-wide EE-PROMs, the former using nitride and the latter, floating gates. Hughes has also announced a part that uses floating gates and C-MOS technology.

However, high-capacity EE-PROMs have not yet caught on. One reason may be that in-circuit programming, the feature unique to electrically programmable devices, is either not desirable or too hard to use on current chips. The improved devices due next year will help determine the answer. Xicor, for instance, intends to introduce an EE-PROM needing only 5 V for programming and otherwise. It will also sport address and data latches so bits will get programmed into the right location automatically. Besides Xicor, some of the recent start-up operations in Silicon Valley promise more versatile EE-PROMs. One company to watch in this regard is Seeq Technology Inc., an Intel spinoff.

At the upcoming International Electron Devices Meeting, Toshiba will disclose a 64-K EE-PROM that needs only one transistor per cell. To achieve this, it had to develop a way to monitor how much charge is being yanked from the floating gate, which otherwise would get irreparably programmed into depletion. So it is using three polysilicon layers. The cell is programmed as in an erasable PROM—via channel injection—and erased



Toshiba on sapphire. The dashed box depicts one cell in an 18-ns 4-K static RAM built on sapphire by Toshiba. The cell area is about 1,300 μm^2 using 3.5 μm design rules. Low-power C-MOS technology offsets the high sapphire cost, Toshiba says.

through field emission from the bottom of the second-level polysilicon electrode.

To avoid depletion, a first-level–polysilicon electrode monitors the amount of charge leaving the floating storage. At last year's IEDM, Mostek introduced a very similar triple-polysilicon EE-PROM; it, too, had an adaptive erasure mechanism to circumvent depletion, but it lacked the bit-for-bit and byte-for-byte erasure of Toshiba's design.

The ability to monitor charge flow this way has another, more subtle implication. To make EE-PROMs easier to use, a ready line is needed to tell a microprocessor when previously latched data was programmed. To inform the processor as soon as possible, some form of current monitoring is valuable since different cells may take more or less time to program. Furthermore, Toshiba says it can use the charge-flow monitoring technique to pinpoint bad or weak cells during manufacturing. This, in turn, would help with redundancy programming.

Besides a need for greater applicability, the slowly

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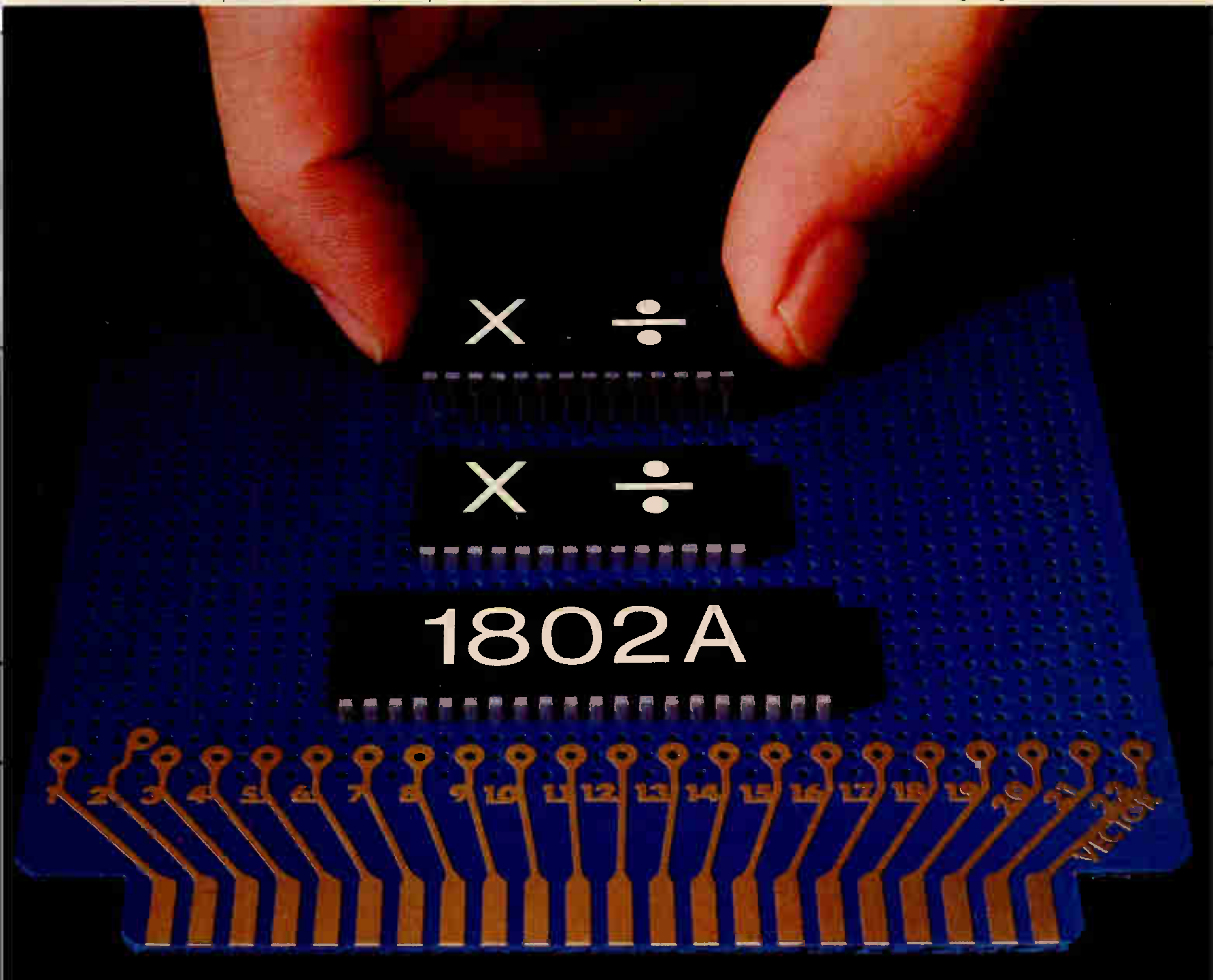

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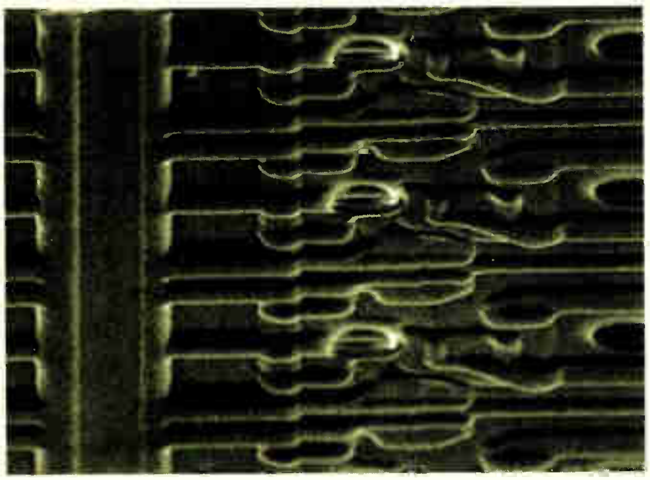
developing market for EE-PROMs is undoubtedly even more related to the glut of ultraviolet-light-erasable-PROMs and their low prices. For instance, Intel is going to guarantee a per-unit price of $16 on its 2764 64-K E-PROM if purchased in quantities of 10,000 or more and delivered during or after the first quarter of next year. That price tag will make the 64-K part cost-competitive with the 2716 16-K E-PROM on a per-bit basis.

The low prices of 64-K E-PROMs are a product of the heavy competition persisting between Mostek, Motorola, and TI. Whereas Intel and Motorola basically use scaled-down 16-K E-PROM cells in their 64-K parts, TI and Mostek use an X-shaped cell. After all of the gate and drain-source sharing, the storage matrix in the latter winds up looking like an array of crosses. Some say that Intel and Motorola will ultimately have to adopt a layout similar to the X-shaped cell for the smallest die size for a given feature size.

Other activity in the E-PROM area includes a slow but sure effort on the part of the Japanese manufacturers to



Memorable. NCR Corp. recently entered the commercial semiconductor business, and this nonvolatile RAM is one of its first offerings. The 512-by-8-bit device features a 250-ns access time. NCR will also bring out an 8-K part based upon the same nitride storage cell.

catch up to the density levels reached by U. S. companies. Right now companies like NEC, Toshiba, and Fujitsu have parts around the 16- and 32-K density levels. Besides these moves to higher densities, lower-density chips are being converted to C-MOS technology and this trend, too, will no doubt continue. At present, Motorola, Intersil, and National offer C-MOS E-PROMs and other will follow suit as they get handier with the technology in the future.

Low-power nonvolatility

C-MOS is also becoming a dominant factor in the design of fuse and mask PROMs. Several semiconductor manufacturers are on the brink of signing off a 256-K ROM to production, some of which, particularly those from Japan, will be made out of C-MOS. An example is the p-well C-MOS 0.25-Mb ROM described by Fujitsu at last month's VLSI conference. Besides operating from a single 5-V supply, it has a typical access time of 150 ns and dissipates about 30 milliwatts of power when active and about 5 millivolts when idle. The ROM's cell and chip area, 64 μm^2 and 31 mm^2 (about 48,000 mil^2) respectively, are typical of the 256-K ROMs due from other suppliers.

Harris Corp., Melbourne, Fla., is making big news in the PROM world by scaling its C-MOS fusible-link family up to the 16-K level and its bipolar units to the 64-K density. The bipolar PROM is basically an extension of Harris's standard PROM line. It uses Nichrome fuses, junction isolation, and—as in its older 16-K part—twin levels of aluminum using 3-μm design rules. However, the 64-K PROM's maximum 85-ns access time seems to render it somewhat fast for MOS microprocessor applications but on the slow side for storing microprograms in bipolar systems. Maximum power dissipation for the chip is just under 1 W.

Harris's 16-K C-MOS PROM, on the other hand, has field programmability, an access time lower than 200 ns, and a 2-K-by-8-bit organization that allows it to interface with the fastest microprocessors. Better still, power dissipation is no more than 500 μW on standby and 50 mW/megahertz in operation. Power usage varies with frequency because, like other Harris C-MOS memories, the PROM is a synchronous design.

As in most C-MOS static RAMs, Harris's PROM takes advantage of the bipolar transistors available with bulk C-MOS processing. Not only do npn transistors drive high-capacitance loads on and off chip, but they also provide the current to blow the fuses, which in Harris's case are made of polysilicon. The company expects to have 32-K and 64-K C-MOS PROMs next year.

The other memory maker hooked on polysilicon fuses is Intel, which at present makes only bipolar PROMs. Using its stacked-fuse bipolar technology, the company recently came up with a 32-K chip that boasts a 40-ns maximum access time and redundancy.

It is interesting to note that Intel, Harris, and others have developed 32-K PROMs with lateral fuses. Above such densities, vertical fuses may be necessary to contain die size. Fujitsu uses a vertical cell, based on what it calls the diffused eutectic aluminum process, for 364-μm^2 PROM cells and 10-mm^2 (15,500-mil^2) 4-K chips. Fujitsu expects that the 16-K part that it now has in development will measure only 30 mm^2 (46,500 mil^2). The diffused-eutectic process is based upon the downward electromigration of aluminum to short out a pn junction directly below it in the cell.

Requiem for the bubble

The future of the bubble memory is a different story. Over the past few months, the prospects for magnetic-bubble memory technology were dimmed with the withdrawal of Rockwell, TI, and then National from the business, leaving Intel's magnetic subsidiary as the lone U. S. supplier. All three exits were attributed to an apparent disparity between profit and the amount of research required to develop the memories and their support electronics.

Rockwell International Corp., Anaheim, Calif., left the business after passing its bubble-memory expertise to Motorola in return for know-how on the latter's MC68000 16-bit microprocessor. Motorola was off building a pilot line for 256-K and 1-Mb chips; Intel, TI, and National were shipping products. Hitachi and Fujitsu were supplying NTT with devices, threatening to enter the U. S. market, and NEC was conducting basic research on bubble technology.

National's departure from bubbles was a surprise, however, and TI's was a real shocker. Outsiders maintain that TI had difficulty in getting high bubble-chip yields using its planar process. In this process, the nickel-iron or Permalloy layers are always deposited directly over aluminum-copper conductor patterns. Both materials are required in conventional bubble chips, but TI's structure was intended to limit step-coverage problems.

National was having bottom-line profitability problems when it lopped off bubble production. Still, National's decision seems the least justified. It had designed some excellent memories and support devices and Motorola, having lost Rockwell as a primary supplier of its device types, fell in with National. National had also designed a very desirable 1-megabyte Multibus-compatible board that beat Intel to the punch. It designed a 4-Mb chip, which promised byte-wide data with a high data rate, and a removable bubble cartridge containing only the memory so as not to replicate the support electronics in each cassette.

The present situation leaves Intel as the only U. S. shipper of bubble memories. Motorola, though, having already spent a lot of money on bubbles, will probably continue its development efforts, for there definitely is a market for these nonvolatile units. The Japanese are surely going to sell their wares in the U. S. Some of those involved with bubble memories at Rockwell, TI and National are going to form their own bubble memory operation and are out hunting down venture capital.

The 4-Mb bubble memory scene looks very like the situation with the 256-K RAM. There will most likely be more than one generation of parts, the first using conventional but scaled-down Permalloy asymmetric chevrons and the second using a new, more advanced technology such as contiguous disks.

The prospects for current-access bubble memory technology, a technique that pledges operation at 5 V and high-speed bubble propagation without perpendicular coils or wire, are less certain. Recently, however, IBM did prove that current-access technology could be used to build bubble memory logic circuits as well as memories, and this discovery may promote research for proprietary applications such as string- and pattern-matching for voice and image recognition, relational data bases, and associative memories.

For redundancy, Smith backs lasers

As a hedge against the low yields that could accompany ever higher levels of integration, redundancy is being incorporated into the latest memory chips at a feverish clip. Of the two competing methods of programming the extra bits—electrical fuses and laser links—Robert T. Smith is sure the laser route will win out.

But then Smith is biased. He has been with Bell's Allentown, Pa., Laboratories since receiving his Ph.D. in physics from the Imperial College of Science and Technology in London, England in 1965. Before becoming supervisor of Bell's 11-member memory test and laser programming group, he worked for three years on new synthetic materials for high-Q crystals in high-bandwidth filter applications. "Then I got promoted and shipped sideways into a field that I knew nothing about: memories."

At first he was in charge of diagnosing and analyzing the failure modes of a 256-bit p-channel static random-access memory. He did the same for later 4- and 16-K dynamic RAMs. In the fall of 1977, the memory designers "were looking at projected yields based on the 4- and 16-K RAMs, and they concluded there wasn't a cat's chance of making the 64-K chip economically without redundancy."

"We got landed with the job of developing the system that would invoke the redundancy," continues the 42-year-old Smith. The designers' self-inflicted constraints—that the redundancy should impose no performance penalties, that spare bits could themselves be replaced with other spares, and so on—made the decision to go with a laser-based approach an easy one for Smith.

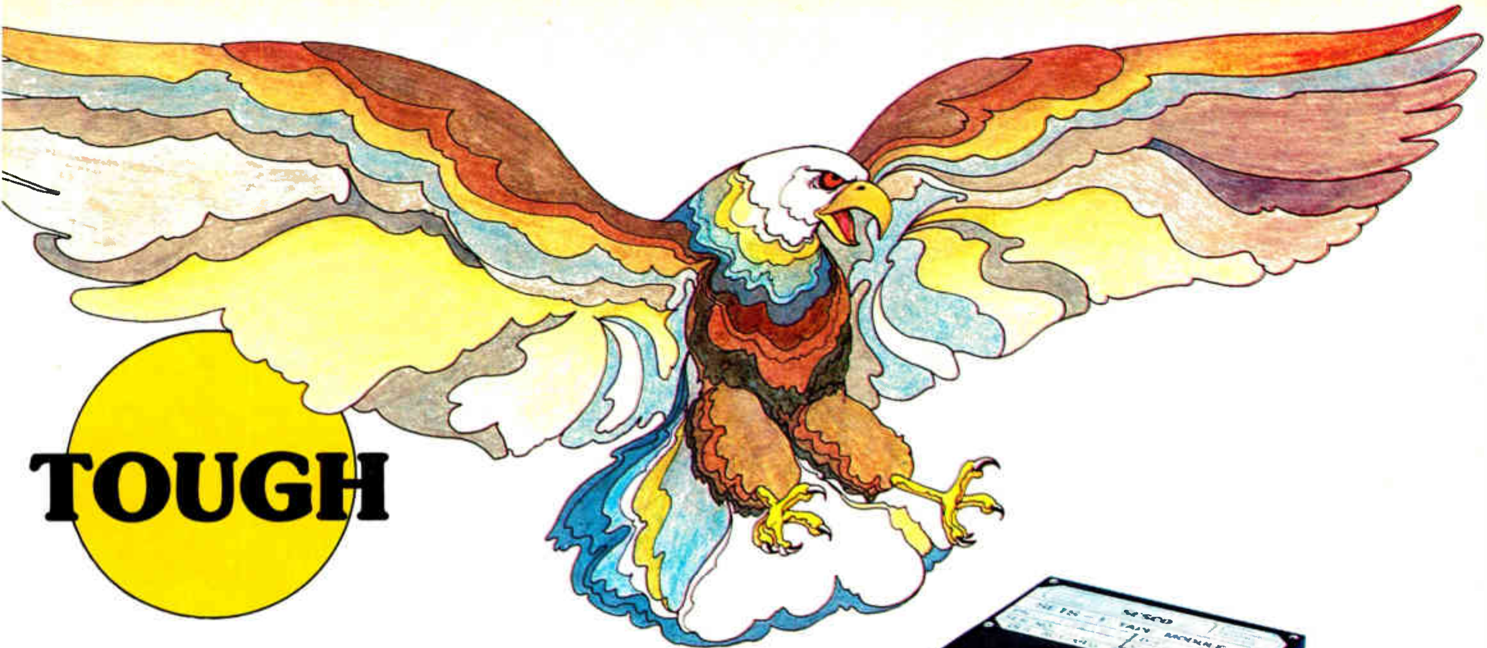
"Electrical fuses were considered but rejected rather quickly. It seemed that a laser, which could completely remove material, was the better way to go."

When Smith was in the testing area, he had to oversee the construction of computer-controlled test sets, and from this he gained quite a reputation for being "handy with computers. In fact, the reason we could bring the redundancy up so quickly and so successfully is that everybody in my group had the same common thread of real-time computer expertise. If the laser guys had been given the project, it might have ended up as a beautiful laser experiment and that's where it would have finished."

Smith is athletic, but his spirit for sports was almost quenched when he took a bad spill on a ski slope the day after he was married. In fact he met his wife while skiing, and now has a two-month-old baby boy who bears his middle name: Taylor. Bob enjoys a hearty soccer or volleyball game now and then and exercises his voice regularly with the two choral groups to which he belongs.

One of his choral groups may even tour Europe in the near future, and this will afford him the opportunity "to show the baby to his other grandparents." Smith was born in northern England—in Durham—and lived there through high school. He now lives with his family in a small hamlet called Coopersburg, which is situated about nine miles south of Allentown.

"We have a nearly-200-year-old converted gristmill on an acre or so with a stream running through it," he says. "It's one of the reasons I like Allentown." **-John G. Posa**



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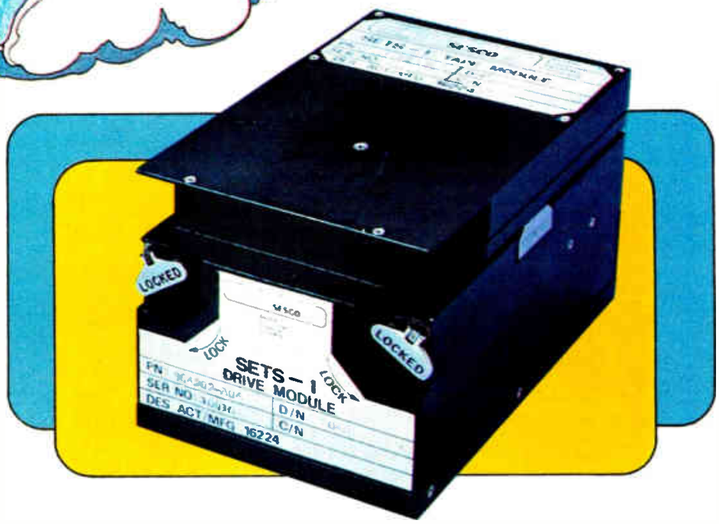

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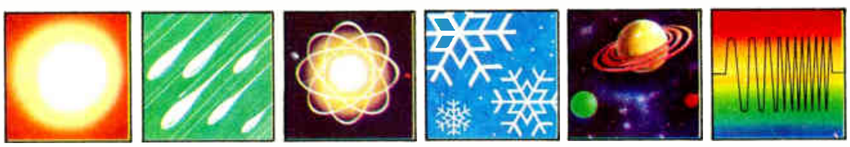

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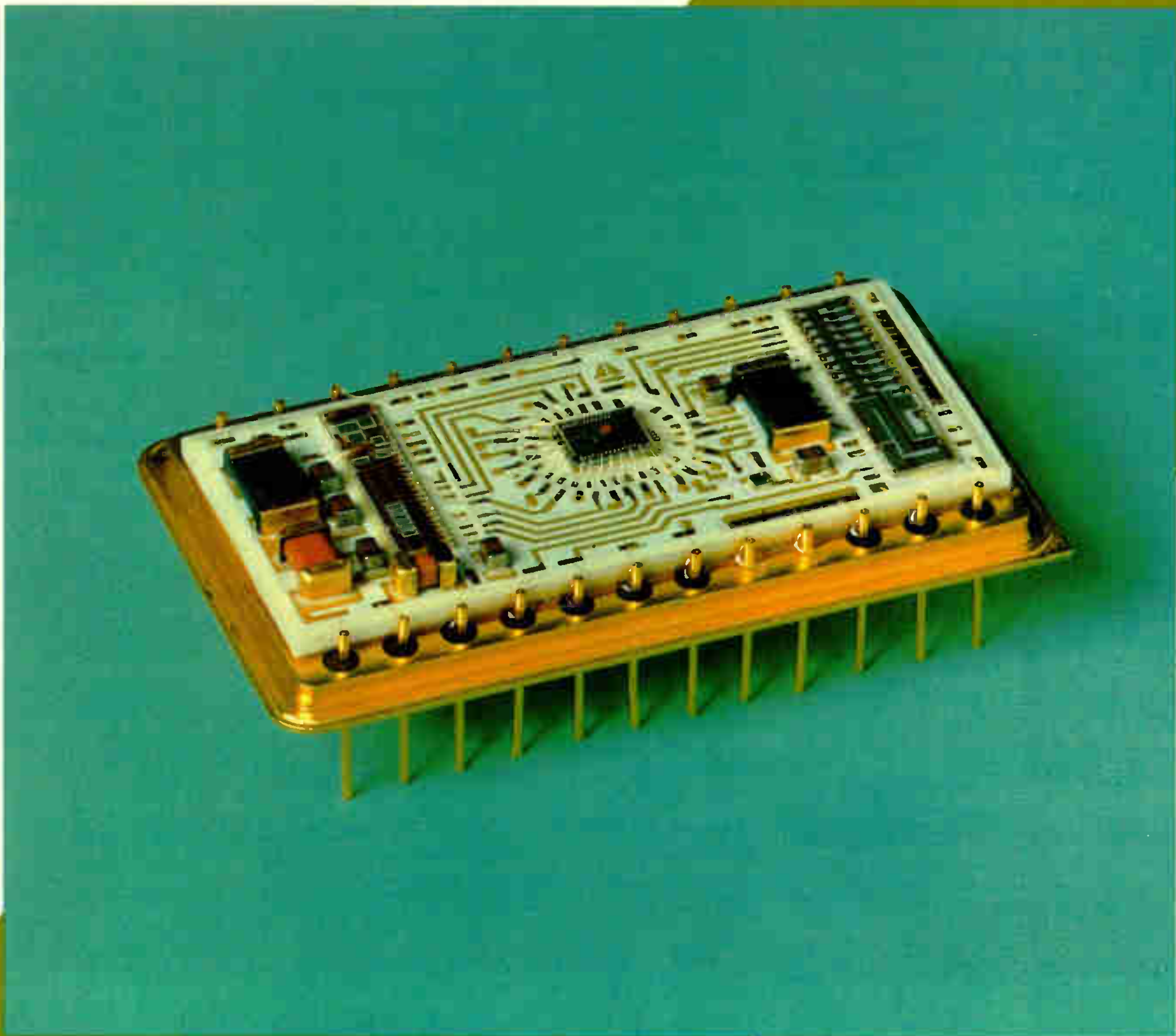


Second generation. ILC Data Device Corp. reduced the active component count from 40 to 1 in the ADH-030 12-bit d-a converter, obtaining one fifth the glitch energy, one third the reference drift, three times the reliability, and an extended operating temperature range for this 35-ns part.

I

ntegration raises the intelligence, resolution, and speed of the links in the data-acquisition chain; materials progress brings more color and variety to displays

by Roderic Beresford, *Components Editor*

☐ The more sophisticated a product is, the better do its particular forms and potential uses harmonize. Refined technologies and changing concepts of component functions were evident this year as data converters and sensors assimilated more capabilities on chip and as new materials brought more and clearer colors to light-emitting diodes and liquid crystals. The next generation may see more intelligence in these parts, as their form and function evolve hand in hand in a stepped-up race to progress.

Data converters, continually progressing to higher resolution and speed, will also eventually acquire direct-memory-access interfaces or even complete microprocessors, natural extensions of the memory and control logic appearing on many present-day devices.

As for evolution within the converter circuits themselves, resistor ladders may yield to all-capacitor charge-summing networks, which not only perform better but need less power and space. Complementary-MOS with its dense logic circuits and plentiful analog switches will anchor these developments, while signals to the smarter converters will emanate from intelligent silicon-based sensors incorporating integrated circuitry for filtering and amplification.

Research is uncovering simpler processes for making imaging arrays for video recording to achieve the density for better resolution and the speed to capture transient phenomena. Display technologies will reveal a broader spectrum of colors, including blue LEDs with reasonable efficiency and dyed liquid crystals in a myriad of hues. Within the next year, flat-panel plasma displays should expand to full-size cathode-ray-tube formats. Also slated for appearance are integrated thin-film and MOS transistor arrays for driving commercial display panels based first on liquid crystals and eventually perhaps on electrochromic materials as well.

A noteworthy trend in passive components is likely to be the rapid spread of chip (thick-film) resistors into general-purpose, printed-circuit–board applications, due to the growth of domestic sources for the necessary automatic insertion equipment. Hybrid-circuit makers will continue to demand precision passive components as their markets slide toward higher performance requirements, impelled by advances in monolithic technologies, especially flash converter chips.

Now that 12-bit monolithic data converters are becoming routine for many makers, their concentration will be focused on creating 14- and 16-bit silicon prototypes and making complete lower-resolution parts totally transparent to the microprocessors directing their functions, C-MOS processing and wafer-level laser trimming of thin-film resistors are emerging as the nearly universal technologies of choice for the coming generation of higher-resolution, low-cost one-chip converters. Designers are looking for temperature-stable voltage references and experimenting with switched-capacitor techniques to manage error budgets within reasonable die sizes.

Hybrid Systems Corp. of Bedford, Mass., was the first to market a d-a converter chip accurate to 14 bits. The HS3140 uses a segmented conversion scheme, with the top 4 bits selecting precisely matched current sources. The lower 10 bits, contributing proportionately smaller errors, are less tightly controlled and made from standard C-MOS switches and a thin-film resistor ladder.

Concurring on the virtues of a segmented approach and foreshadowing a trend in digital audio, Analog Devices Inc. of Norwood, Mass., recently announced the first monolithic 16-bit d-a converter. Although the AD7546's resistor ladder limits accuracy to only 12 bits, its wide dynamic range, guaranteed monotonicity, 10-microsecond settling time, and under-$30 price make it a fair first shot for consumer audio playback. The implementation is C-MOS, with an internal 12-bit d-a converter using an R-2R ladder and operated in the voltage-switching mode. Other companies will likely contribute strong entries in this area also.

Another approach that has potential for audio playback is the companding or logarithmic d-a converter. Precision Monolithics Inc. of Santa Clara, Calif., has led development of this technique for telecommunications, and recent parts like its bipolar DAC78 are aimed at speech synthesis applications. It is priced like other 8-bit parts, but the logarithmic transfer function in effect gives it a 72-decibel dynamic range and 12-bit accuracy.

C-MOS interfaces

However, for cost-effective processing, the leader will continue to be C-MOS. Indicative of the trends are the DAC083 (from $4.50) and DAC1230 (from $15.75), 8- and 12-bit d-a converters from National Semiconductor Corp. of Santa Clara, Calif. Consuming only 20 milliwatts, these parts are designed for simple direct interfacing with microprocessor buses: their latched inputs are TTL-compatible through a biasing scheme that exploits the parasitic bipolar transistors available in C-MOS.

A-d converters are evolving into data-acquisition systems, as multichannel inputs and on-board memory can be economically fabricated in C-MOS. D-a converters can also ease a processor's supervisory tasks by including memory that can be directly addressed. The 12-bit AD7544 from Analog Devices sports a six-word stack, and many other makers are adopting similar strategies.

As well as concentrating more functions on converter chips, C-MOS is at the center of the rapidly emerging switched-capacitor conversion techniques. Completely eliminating resistor ladders from d-a converters cuts power dissipation and size while improving speed and accuracy. Eight-bit successive-approximation a-d converters using weighted capacitor d-a networks surfaced this year, notable among them Texas Instruments' TL520 and Motorola's MC14444. Extension of this technique to 10- and possibly 12-bit a-d parts is likely.

Flash news

The fastest of all a-d conversion schemes—parallel, or flash, encoding—graduated to 8-bit resolution with much fanfare. TRW LSI Products of La Jolla, Calif., presented the video-speed market with the first commercial product made in a 1-micrometer process: the TDC1025 8-bit flash converter. Using a scaled-down triple-diffused bipolar process and optical lithography, TRW managed to get the necessary 255 comparators and encoding logic onto a 200-by-160-mil chip.

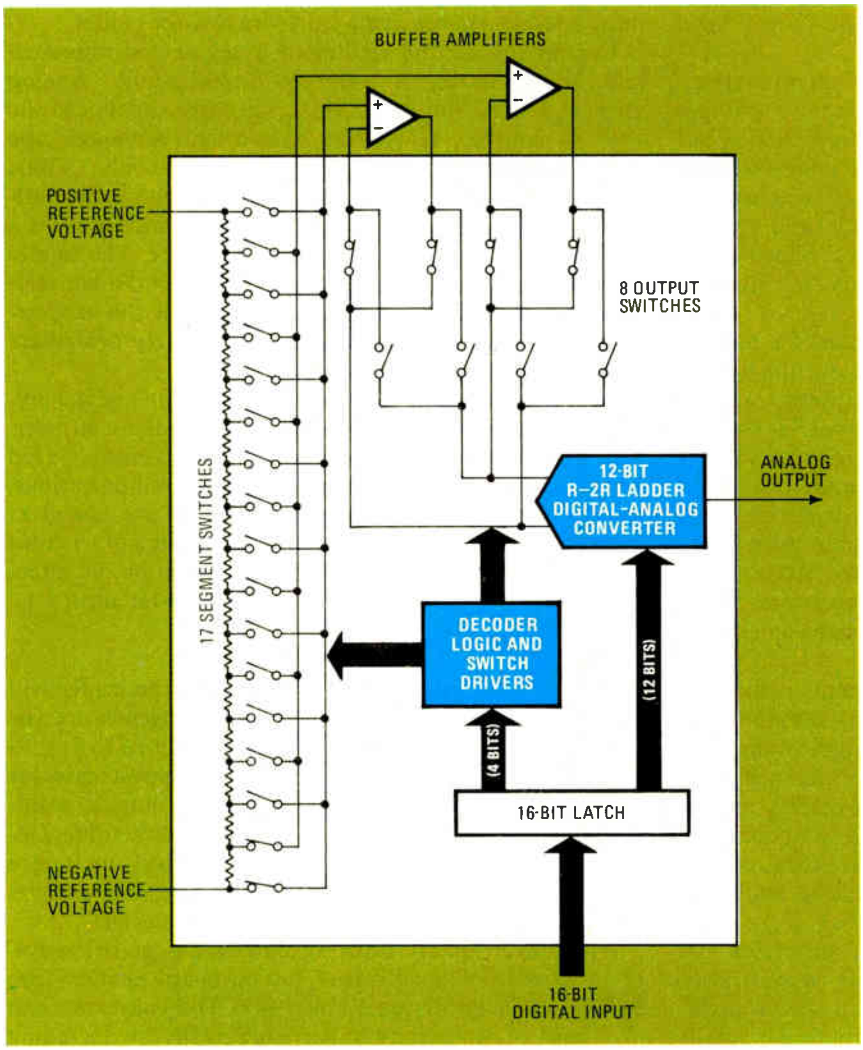
With the tight geometries and well-developed processing, matching of the base-emitter voltages in the comparators' emitter-coupled transistor pairs is close enough to give differential linearity within $\pm 1/2$ of a least significant bit. And although it dissipates 2 watts, the sample rate is up to 75 megahertz—the present record for a monolithic 8-bit conversion.

RCA Corp.'s Solid State division in Somerville, N. J., chose a C-MOS implementation for an 8-bit flash converter that trades speed for lower power operation. Limited to about 15-MHz conversion rates, the CA3380 needs only 200 mW and costs far less than 50-MHz and faster parts. Tradeoffs in flash converter selection will continue to be tricky, since the technique gives parts that can be easily "stacked" for an extra bit or two of resolution or else paralleled for doubled conversion rates. For those still satisfied with a 6-bit component, Analog Devices' AD5010 takes bipolar converter circuits up to 100-MHz sample rates with less than 0.5-W dissipation.

Feeding the hybrids

With monolithics taking over the 12-bit applications, hybrid converter makers are pushing specifications to higher resolution and specialized markets by exploiting the advances in monolithic technology. Micro Networks Co., Worcester, Mass., developed a three-layer metal interconnect technology to produce the MN5700, a 12-bit a-d converter fully qualified to 200°C. Teledyne Philbrick, Dedham, Mass., combined dielectrically isolated switches with a thin-film chromium-cobalt resistor network and a precision discrete operational amplifier to give the 4080 series of voltage-output 12-bit d-a converters that settle in 250 nanoseconds. And Micro Power Systems of Santa Clara, Calif., pushed known techniques like laser trimming to get an 18-bit d-a converter, guaranteed monotonic, with 16-bit relative accuracy. The MP370 is a two-chip hybrid converter with a 2-μs settling time and a low 60-mW power consumption.

Aiming at digital recording studios, Burr-Brown Research Corp. of Tucson, Ariz., has put together a pair of hybrid converters with 16-bit resolution designed with pulse-code-modulated audio signals in mind. The PCM50 d-a converter typically settles in 5 μs and introduces only 0.003% total harmonic distortion. The PCM75 a-d converter performs successive-approxima-



Interpolator. The AD7546 from Analog Devices uses a 12-bit converter in the voltage switching mode to fill in 16 intervals derived from a resistor string. External buffer connections are switched on adjacent segments to compensate for offset voltages.

tion conversions in at most 17 μs with 0.004% distortion. As digital audio opens up, many general-purpose hybrid makers will be able to offer studio-quality devices and will begin quoting distortion figures for this market. But to get into consumer equipment, the rule of thumb calls for a $10 price tag, and that will be a reach for hybrid designs in the foreseeable future.

Top performers

The highest-resolution data-conversion system reported this year was a 20-bit a-d converter from National Semiconductor built around a microprocessor and the old single-slope integrator. Intelligent circuitry offers continuous error correction, apparently a mandatory feature at single-part-per-million error levels.

The prize for highest speed goes to a Josephson-junction–based converter, a 6-bit a-d prototype built by the National Bureau of Standards. Each bit of data is provided by one superconducting quantum interference device. Six of these Squids of binary-weighted sensitivities to magnetic fields are simultaneously exposed to the field generated by the input current, in the superconducting analog of a semiconductor flash converter. Besides reaching a 2-gigahertz conversion rate, the design needs only one device per bit of resolution.

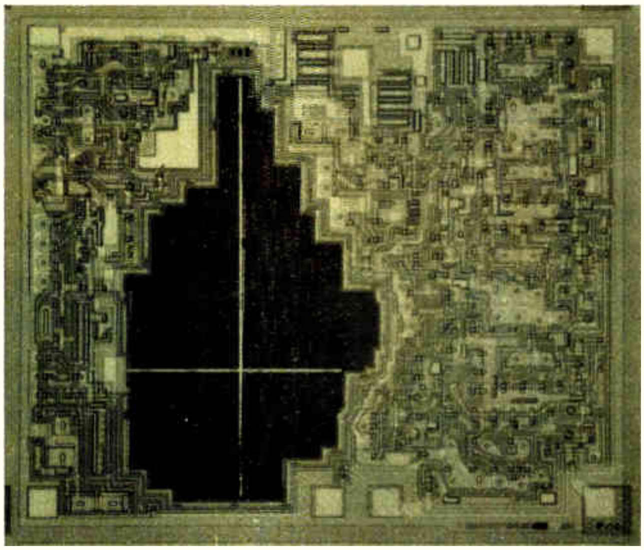
Under pressure

With the chip makers and hybrid houses well in control of data conversion, sensing elements continue to be the weak link in the data-acquisition chain. But expertise with integrated circuits may be producing some solutions. With packaging costs still holding back pressure transducer development, announcement from IBM Corp.'s San Jose, Calif., Research laboratory of a much smaller device sparked interest at the International Electron Devices Meeting last December.

A silicon-based accelerometer measuring only 5 mils on a side incorporated a metal-coated silicon dioxide cantilever beam as the active arm of a capacitive sensing element. Detection circuits were integrated on the chip using MOS devices. Capacitance variations of 40 attofarads per gravity were achieved in an area more than a hundred times smaller than previous sensors.

Bipolar silicon-device technology produced an alternative to Hall-effect sensors. A novel magnetic-field sensor, called a carrier-domain magnetometer, surfaced at Britain's York University. The device uses an annular structure of merged npn and pnp transistors in which the current distribution forms a spoke-like pattern that rotates in the presence of a magnetic field. Junction detectors around the periphery of the ring produce an output signal whose frequency is proportional to the current distribution's angular velocity, with sensitivities typically as high as 10 Hz per gauss.

Silicon temperature sensors are benefiting from increased integration by becoming easier to use. The ICL8073 from Intersil Inc. in Cupertino, Calif., is a laser-trimmed bipolar chip that combines bandgap voltage reference circuitry with thin-film technology to give nonlinearities as low as 0.5°C and that puts out reference signals as well as readings proportional to absolute temperature and degrees Celsius or Fahrenheit.



Smart diode. A photodetector diode from TRW Optron is integrated with logic and control circuits to make an ambient light sensor that will also automatically adjust an LED display's brightness, saving power in dim lighting and improving legibility in bright surroundings.

Although silicon is an excellent performer in some transducers, LEDs are calling on other materials for higher output power and a variety of colors. Matsushita Electric Industrial Co. of Osaka, Japan, increased the brightness of red LEDs by a factor of nearly 10 with the development of a GaAlAs heterojunction diode that puts out 200 millicandelas at a 20-milliampere drive current. The structure, formed by liquid-phase epitaxy, has a zinc-doped p-type layer with a 1.85-electronvolt bandgap and a tellurium-doped n-type layer of 2 eV bandgap. The 10-μm-thick n layer acts as a nearly lossless window to pass the radiation out of the chip.

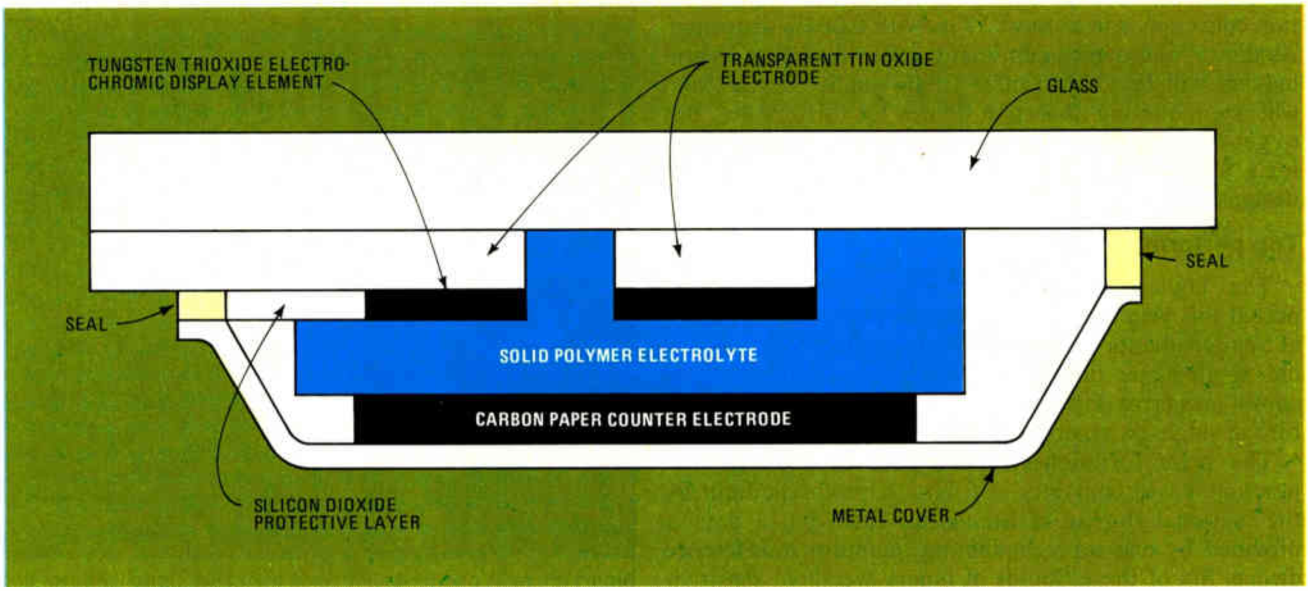
Blue emitters

Blue LEDs are closer to reality with the news, again from Matsushita, that sample quantities of diodes with a 2-mcd brightness for a 10-mA driving current will be available. The devices have gallium nitride and zinc-doped epitaxially grown layers on a sapphire substrate.

Sanyo Electric Co. also came up with a blue emitter, based on silicon carbide, that is grown in a liquid-phase epitaxy process from a silicon melt—the wafer holder contributes the carbon. The n-type layer is doped with nitrogen, while the p-type layer uses aluminum. Brightness of the 480-nanometer light is 2 mcd at a current of 20 mA and driving voltage of 3.5 V. The blue LEDs are offered in a full-color lamp that also includes a red- and green-emitting diode chip based on gallium phosphide.

Discrete photodetectors may be giving way to integrated circuits incorporating photodiodes and providing more functions. An example is the OPL100 from TRW Optron of Carollton, Texas, a silicon IC that includes, in addition to a 2,500-mil^2 photodiode, amplifiers, comparators, random logic, a voltage regulator, and output drivers to automatically control a display's brightness in response to the strength of the ambient light.

Photodetector arrays for solid-state image sensing have begun to hit the marketplace, with Hitachi Ltd. in



Longer life. American Cyanamid has fabricated electrochromic displays using solid proton-conductive polymers that reduce electrode degradation. The entire assembly is simple to mass-produce and stands up to at least 10^7 switching cycles at 0.5-Hz clock rates.

the lead—its VK-C1000 video camera is built around a 485-by-384-element MOS array that provides resolution of 350 by 260 TV lines and signal-to-noise ratios of 46 dB in good lighting conditions. Sharp Corp.'s Central Research Laboratories in Nara, Japan, and Toshiba's Research and Development Center in Kawasaki both showed charge-coupled-device imager arrays at the IEDM that use two layers of polysilicon instead of three, boosting array yields.

Researchers at Hughes Aircraft Co. of Carlsbad, Calif., are on the way to developing an avalanche photodiode imaging array that will be the solid-state equivalent of a photomultiplier tube. The pn diodes of the array are reverse-biased close to the avalanche breakdown point so that light-generated charge from very faint sources of the kind encountered in celestial navigation will trigger breakdown in the depletion region and multiply the current output of the cells.

While night vision and thermal imaging systems based on infrared photodetectors will continue to find military uses, the pyroelectric imager is catching on in commercial and industrial applications, thanks to its lower cost, lighter weight, and ability to work without cooling. Infrared imagers based on pyroelectric materials like triglycine sulfate depend on the heating effects of incident IR photons to modify the electric polarization of the image plane and so to distribute charge over it in accordance with the amount of heat absorbed. A scanning electron beam then neutralizes the imaging charges and gives rise to the output current from the array. Thomson-CSF of Boulogne-Billancourt, France, and Philips Industries Ltd., Eindhoven, the Netherlands, are among the suppliers of the new vidicon tubes.

Flattening displays

Although solid-state TV cameras are here now, the solid-state video display is still in the future. But the quest for the flat-panel display continues, and though there is no clear front-runner, significant advances have been won in several areas, including liquid-crystal, plasma, electroluminescent, and electrochromic displays. Clive Sinclair's flat CRT moved a step closer to market, when Sinclair Research Ltd. of Cambridge, England, contracted with Timex in Dundee, Scotland, for volume production of tubes measuring 6 by 4 by 1 inches.

Burroughs OEM Corp. from Detroit provided a big push to plasma displays with the introduction of a new generation of its Self-Scan technology that incorporates a memory feature by merging ac and dc operation in a single cell. An ac sustaining signal is applied across all the elements of the display panel in parallel, and a level of matrix-addressed dc cells below these ignite or quench the plasma locally when writing or erasing is called for. The scheme leads to simple drive electronics and flicker-free displays that can now extend to the standard 96-character rows of a CRT display.

Electroluminescent panels, which are seen as meeting military needs for rugged, bright, compact displays, are still undergoing much laboratory investigation. The IEDM included a report from Fujitsu Ltd. that a solid solution of zinc sulfide and zinc selenide sandwiched between insulating layers of yttrium oxide can put out light at a 100-footlambert brightness level with only 120 V of drive voltage. And researchers at Rockwell's Electronics Research Center in Thousand Oaks, Calif., were squinting at a 700-ftL green display that uses zinc sulfide doped with a terbium fluoride activator.

Liquid crystals are likely to be the material of choice for the first generation of flat displays made on top of silicon IC driver arrays. They are now routinely made with dichroic guest-host materials, which yield assorted colors and better contrast than the earlier twisted-nematic cells. In a development that improved contrast by a factor of 20, researchers at Brunel University in Middlesex, England, bound these electrofluorescent dye molecules to 1-μm pieces of mineral clay that disperse in water as charged particles. These dipoles can be easily aligned with relatively small electric fields compared to those needed for the dye molecules themselves.

While the fastest LCDs are still the 50-μs surface-mode devices from American Liquid Xtal Chemical Corp., Kent, Ohio, Thomson-CSF showed another possible technique for fast switching at the Paris Components Show: a 10-by-10-centimeter display consisting of a matrix of 240 by 250 pixels was updated at 20 ms per row. The display used a compound based on biphenylnitryl that enters the nematic phase at 40°C, where it orders under an applied field.

Electrochromics at last

In a piece of work that may finally lead to a solution of the lifetime problems of electrochromic displays based on tungsten trioxide electrodes, American Cyanamid Co.'s Chemical Research division in Stamford, Conn., showed attendees at the Society for Information Display conference results of experiments on solid polymer electrolytes. These proton-conductive compounds give display elements that can be switched in less than 1 second with 1-V signals and suffer no degradation in 10^7 cycles. The optimal structure found was based on poly-2-acrylamido-2-methylpropanesulfonic acid, with titanium dioxide dispersed in the polymer to provide a white background for the display.

Another solid-state electrochromic development came from Nippon Kogaku KK of Japan, where 100-ms switching times were achieved in a cell based on metallic hydroxides and tungsten trioxide electrochromic layers, with residual water providing the mobile ions. Reactive-ion plating and indium tin oxide electrodes were used in the fabrication of devices that tested out at over 5 million cycles with no degradation.

Passive activity

The steady world of passive components had a couple of surprises this year, with Vishay Intertechnology Inc., Malvern, Pa., introducing what may be the ultimate in foil resistors. A photo-engraved nickel-chromium alloy is bonded to a layered ceramic substrate with a new composition that better compensates for the resistivity change over temperature in the metal with the strain-induced changes in resistance due to differential thermal expansion of the metal and ceramic. The result is a low temperature coefficient that averages about 0.25 ppm per °C over the range 0° to 125°C.

Analog Devices went into production with one of the first transformers to employ thick-film windings. So far, the tiny component is used in isolation amplifiers. Its coils are built up using hybrid manufacturing techniques: copper paste screened onto ceramic substrates gives the flat spiral windings. The transformer's 12-mil coil pitch leads to a 20-MHz bandwidth, and the thick-film insulation layers isolate up to 8,000 V.

Hexfets derive their high power from Lidow

After lagging behind integrated circuits for years in the use of advanced design and process techniques, the once-staid power components business shows signs of catching up. Nowhere is this more apparent than at International Rectifier Corp., where in a remarkably short three-year development cycle a team of youthful technologists has succeeded in firmly establishing a landmark high-power transistor line based on leading-edge MOS processing.

Spearheading the drive at his family firm ever since he graduated from Stanford University in late 1977 is Alexander Lidow. "We were determined to develop a high-voltage (400-V) process that could apply initially to 100-V parts," he recalls. Lidow already had a head start from graduate studies in the field at Stanford, where he earned a doctor of philosophy degree in applied physics.

The *status quo* in power devices then was bipolar-dominated and limited to about 60 V. "MOS had all the advantages of switching speed and gain over bipolar—everything except for cost," says Lidow. But he and fellow Stanford graduate Thomas Herman in early 1978 quickly turned out, using mask sets built while in school, 100-V and 400-V aluminum-gate MOS field-effect transistors, then the first of their kind. But those did not measure up to desired performance, which forced a redesign to silicon-gate form that within months paid off.

The resulting devices became the Hexfet line that now numbers some 164 different parts of up to 500-V–40-ampere ratings. "The redesign put us over the cost threshold and made the difference between a specialty product and a volume product," says Lidow, who serves as vice president of research and development for the El Segundo, Calif., firm. He credits Herman, manager of new products, with being the "key technologist" behind Hexfet.

The specifications of Hexfet leave no doubt it is squarely in the integrated-circuit business and so poses the same processing challenges facing large-scale integration manufacturers, points out Lidow. The firm's first silicon-gate device two years ago "had 30,000 transistors in parallel, which is high LSI density and amounted to building 30-K RAMs at a time when 16-K was standard," as he puts it.

During the past year, Lidow has labored to transfer Hexfet into volume production in a new next-door manufacturing facility. His interest extends to the smallest details of the MOS process, even to personally training each production worker in the virtually automated plant. "Each is a hand-picked volunteer and so far not a single one has left us," he boasts. The plant went into operation in June 1981 and can produce twenty-five thousand 4-inch wafers a month—"enough by itself to satisfy world demand," Lidow points out.

Pioneering with MOS power devices is just the first step; in the next phase Lidow contemplates adding integrated control functions. "Because most of the world lives out of one socket with one product, it is clear Hexfet is only the start of the transition from power control to energy control," he says.

-Larry Waller

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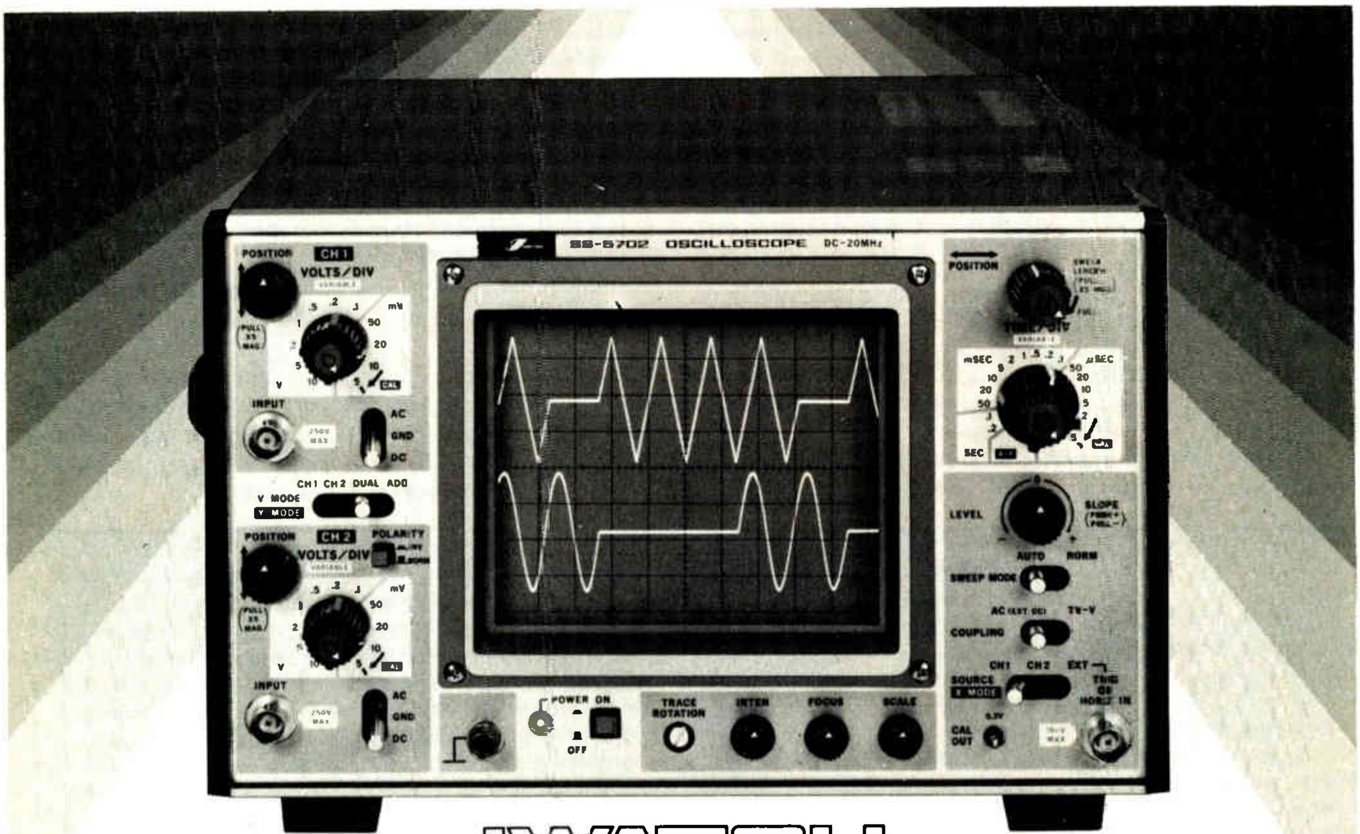

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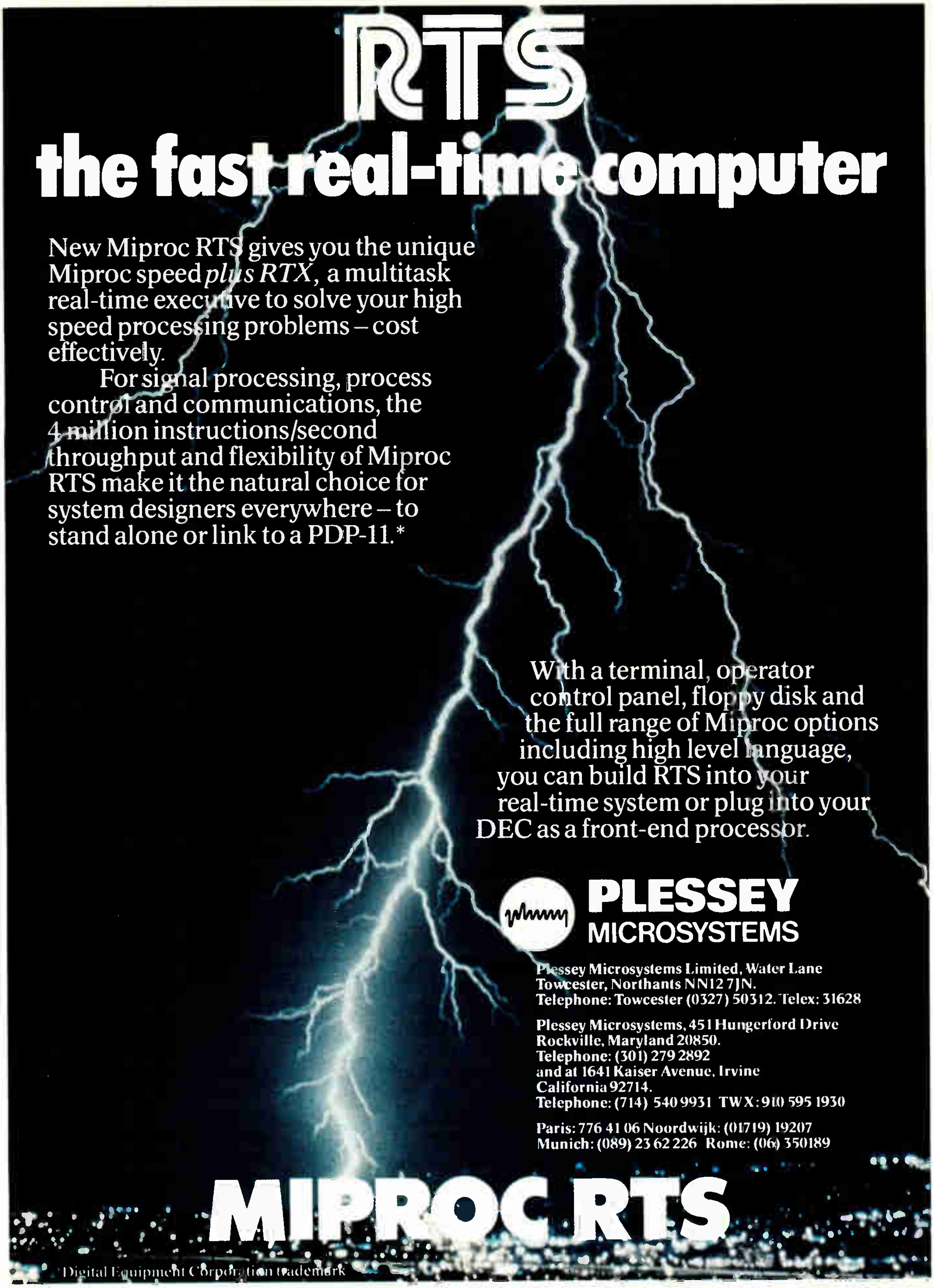
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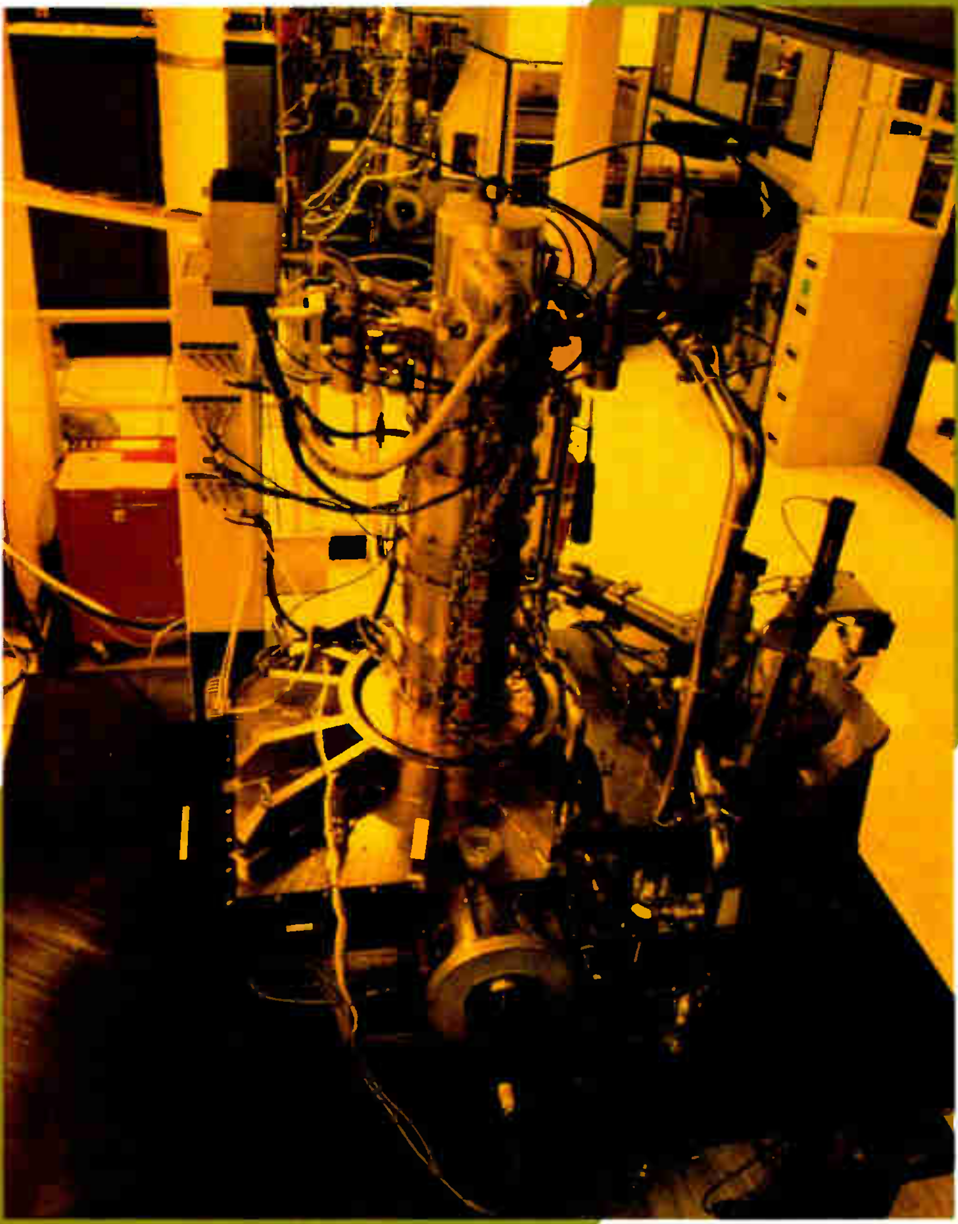


High throughput. IBM's EL-3 high-speed, direct-writing electron-beam lithography system, part of the automated wafer-processing line at East Fishkill, N. Y., is capable of exposing up to thirty 4-inch wafers per hour.

Although the chip-carrier continues to evolve, the pin-grid array is competition; for IC processing, direct-writing electron-beam units enter their second generation

by Jerry Lyman, *Packaging & Production Editor*

☐ Chip-carriers continued gaining in popularity this year. Plastic leaded types not only benefited from improved techniques for pre- and post-molding packages—the appearance of flush-mounting techniques also promises to eliminate their need for plated through-holes. Ceramic leadless types, until now mainly used on hybrid substrates, have found a new home on composite metal-plastic printed-circuit boards. At the same time, vapor-phase soldering of these leadless carriers to polyimide and glass-epoxy boards has at last been successful.

Integrated-circuit firms have also started to accept the ceramic leadless chip-carrier as a viable package for large-scale integrated circuits, with the single-layer ceramic type in particular being favored for most new entries. Meanwhile, in anticipation of the packaging densities and heat dissipation needed for the next generation of very large-scale integrated circuits, many packaging firms are already furnishing carrier prototypes with input/output terminations on 20-to-25-mil centers, compared with today's standard 40-to-50-mil spacing.

As pinout counts approach the 100-to-200 range, the pin-grid array may be a more space-efficient package for the coming generation of VLSI and very high-speed integrated-circuit chips. Moreover, beryllium oxide is being used experimentally as a substrate and packaging material that dissipates heat more efficiently than aluminum.

Finally, in the IC-processing field the first examples of a new generation of equipment are appearing, such as improved electron-beam lithography machines, radically new plasma etchers, and an isothermal annealer based on infrared radiation from a graphite heater.

Skimming the surface

In the past two or three years, a trend has developed toward soldering chip-carriers of all types (leadless and leaded) directly to pc board surfaces. This method eliminates both the expense of socketing and, more importantly, fabricating plated through-holes, which are expensive to make and relatively unreliable and take up valuable board real estate. In fact, with the elimination of through-holes, many two-sided boards could be converted into single-sided types.

Companies like Rockwell International Corp.'s Collins Telecommunications Products division, Cedar Rapids, Iowa, and Martin Marietta's Aerospace division, Orlando, Fla., have successfully soldered and temperature-cycled arrays of leadless ceramic chip-carriers on glass-epoxy and -polyimide boards. However, most electronic packaging experts are still not convinced that the large difference between board and ceramic temperature coefficients of expansion will not result in solder-joint failures over environmental extremes.

This situation has led at least three companies to embark on programs for finding a substrate whose temperature coefficient of expansion comes close to matching that of the chip-carrier's alumina body.

In its approach, Bell Laboratories in Denver, Colo., uses the Lampac method where a thin double-sided epoxy-glass pc board is laminated to a dielectrically coated steel support plane. The composite, which has a coefficient of expansion near that of alumina, separates circuit interconnections from the steel core, which acts as both heat sink and ground plane. Printed wiring interconnections are located on both sides of the thin pc laminate and are connected by vias 11 mils in diameter, rather than by plated through-holes. Bell has tested chip-carriers with as many as 68 I/O pads on its Lampac boards and is evaluating even larger types.

Sandwich board

Researchers at the PCK Technology division of Kollmorgen Corp., Melville, N. Y., have also worked on metal-backed boards to which leadless ceramic chip-carriers can be directly attached. The firm's engineers experimented with many metal-plastic composites, and a 30-mil-thick nickel-iron (Alloy 42) support for an epoxy-glass sandwich yielded some of the best results. Chip-carriers of many sizes were reflow-soldered on top of the sandwich, which has encapsulated wire (as in Multiwire) between its two 5-mil-thick layers.

Continuing this trend, Texas Instruments Inc.'s Metallurgical Materials division, Attleboro, Mass., has developed a substrate material composed of a core of Invar, a low-expansion nickel alloy, clad on both sides with copper. Its thermal coefficient matches that of alumina and, since the material can be supplied in sheets as wide as 24 inches, it could be used for large arrays of leadless ceramic chip-carriers.

A key to the direct attachment of chip-carriers to any type of substrate is the use of vapor-phase reflow soldering. This technique involves heating the entire circuit board, with components in place, in a vented container. The heat-transfer medium is a dense saturated vapor created by a fluorochemical liquid heated to its boiling point. That heats all elements to precisely the same temperature and appears to be the optimum soldering method for directly attaching chip-carriers.

For all its virtues, the leadless ceramic chip-carrier has two serious limitations. It is relatively expensive compared with, say, a plastic dual in-line package, and it is difficult to solder reliably to an epoxy-glass pc board.

Because of these drawbacks, Amp Inc., Harrisburg, Pa., first came out with a premolded leaded plastic chip-carrier in 1976. That carrier was inexpensive and, with its leads, could easily be soldered to any pc board. However, Amp was only interested in selling the package and its automatic assembly equipment, leaving the user to bond his own chips into the package. In addition, at this time, the premolded carrier had to be proven out in a high-humidity environment.

Plastic takes the leads

This year has had two breakthroughs that should finally let the leaded plastic chip-carrier take over many commercial applications from the leadless ceramic chip-carrier. The first breakthrough was the announcement by TI that it would put out a family of digital products in 20-, 28-, 44-, 68-, and 84-pin plastic carriers.

Unlike the Amp premolded carrier, the TI carrier uses the same packaging method as the plastic-DIP–encapsulated chips bonded to a metal lead frame covered by a thermosetting epoxy. The company is currently running environmental tests on IC chips in its postmolded carrier, and says that a test lot of 28-pin packages has been subjected to 85°C at 85% relative humidity (RH) without any chip failures.

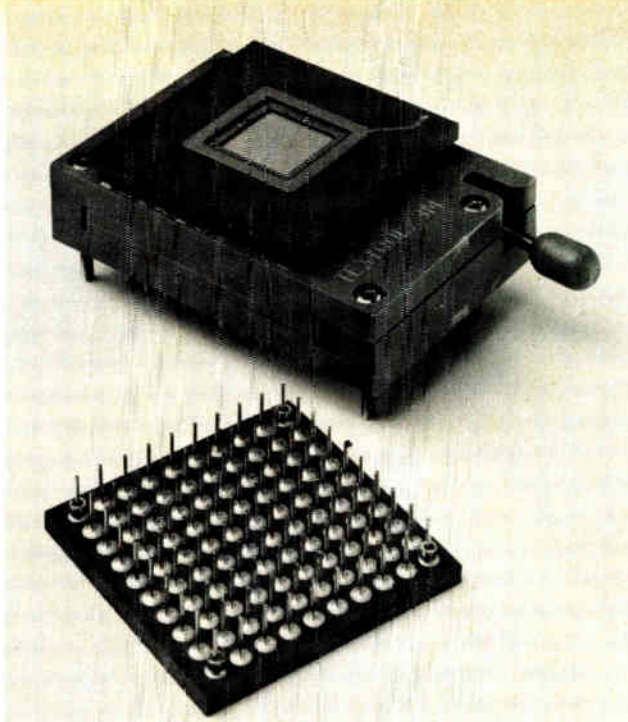
Since IC makers are most familiar with the assembly techniques for packaging chips in plastic DIPs, it is almost certain that other large semiconductor firms will soon follow TI's lead. It is interesting to note that the lead configuration of the TI units is mechanically the same as the earlier Amp carrier. That carrier meets the Joint Electron Devices Engineering Council pc-footprint standard for chip-carriers and it appears that the future plastic leaded carriers from other IC firms will resemble the Amp unit mechanically.

Silicone coating

A second breakthrough took place at Bell Laboratories, Murray Hill, N. J., where some important tests were run on silicon nitride-passivated chips packaged in the Amp carrier and in a molded chip-carrier designed in house. Each carrier's chip was protected either with a Dow Corning RTV silicone or a silicone gel coating. The plastic carriers were then reflow-soldered to a standard pc laminate.

Accelerated environmental checks, which included testing at 85°C, 85% RH, thermal cycling, and flexural tests, were done to gage the reliability of the chip-carriers and their soldered connections to the test boards. None of the RTV-encapsulated chips failed in more than 2,000 hours of 80°C, 85% RH testing, but some gel-encapsulated ICs did. Temperature cycling made a few solder joints fail, mostly because of faulty wire bonds. Overall, the tests showed that both versions of the carriers to be highly reliable. These tests were important to potential users who wish to put custom chips unavailable from the large IC makers in plastic chip-carriers.

With the availability of plastic leaded chip-carriers and other small plastic leaded packages, such as the small-outline and small-outline-transistor SOT types, a new high-density packaging method called flush mounting should start to appear. In this method, all plated through-holes will be eliminated. Components will be attached directly to a pc board by their leads.



The flush mount method should require about 40% to 75% of the board area taken up by the standard combination of DIPs and plated through-holes. However, since the plastic carriers and the other small leaded plastic semiconductor packages have leads on 50-mil centers, finer-line boards will be needed and different attachment processes will have to replace the now universally accepted wave-soldering method.

The technology for attaching leaded plastic components to pc boards already exists in conventional reflow and vapor-reflow soldering. In addition, the plastic leaded carriers will not require boards with matched thermal expansion, as do leadless ceramic chip-carriers. The market for plastic leaded carriers is limited to commercial applications; ceramic chip-carriers will garner all high-reliability military and aerospace sectors. To hasten the application of plastic carriers, TI has already demonstrated an experimental version of a machine that loads, heats, and attaches plastic carriers to a board. Several automatic-assembly machine makers have expressed interest in developing commercial versions of the machine.

Cavity up and cavity down

Continuing last year's trend, more and more IC companies are offering products in ceramic chip-carriers. Also, now microprocessors and microprocessor peripherals are being packed in leadless ceramic chip-carriers. However, IC firms are not in agreement over which type of ceramic chip-carrier to use.

Intel Corp., for example, favors type A carriers—a multilayer unit with its chip cavity facing downward. This type of carrier dissipates power into its pc board efficiently, but the carrier can only be installed in a

Pinned packages. A 100-pin array from 3M's Electronic Products division (left) is shown inverted and in place in a zero-insertion-force socket. Pin-array packages offer a maximal density of input/output pins per square inch with very short signal, power, or ground leads.

socket. Since the Santa Clara, Calif., firm requires that its microprocessors should be field-replaceable, the socket is justified.

Zilog Inc., Cupertino, Calif., and Motorola Inc.'s Semiconductor Sector operations in Austin, Texas, however, are opting for the type B and C ceramic chip-carriers, whose chip cavities face up. Obviously these companies are projecting large-scale direct soldering of their chip-carriers, though the same carriers can be socketed if necessary.

As VLSI chips become larger and more complex, two trends are taking place. One is that with pin counts over 100, chip-carriers with 50-mil I/O spacing are beginning to occupy alarming amounts of board area. The other is that the average power dissipated by the VLSI chip is rising from below 1 watt to at least 5 W.

To solve the I/O problem, many companies are now looking at chip-carriers on 20- and 25-mil centers. But as one chip-carrier manufacturer says, "We can make these carriers, but who will make the boards to put them on?"

Nevertheless, this year should see chip-carriers with tighter spacing available commercially. In addition, a Jedec committee is attempting to develop a standard for carriers with closer spacing.

As far as increasing the heat dissipation of the chip carrier, it appears that beryllium oxide is a good bet. Brush Wellman Inc., Elmore, Ohio, has supplied 68-pin BeO type A chip-carriers to Sperry Univac in Blue Bell, Pa., for evaluation. These carriers were evaluated against aluminum oxide types in special tests in which 3.5 W was dissipated in each package. The beryllia units, with superior thermal conductivity, outperformed the alumina units. The firm is also using the same material in the design of over 100-pin multilayer package in a VHSIC application for General Electric.

Pin-grid arrays are promising

Once the ceramic DIP needed over 40 I/O pins, it was replaced by the ceramic chip-carrier. Now with lead counts in VLSI exceeding 100, it appears that pin-grid arrays will replace the chip-carriers in these applications.

The pin-grid array, which is a square multilayer ceramic package with an array or grid of bottom pins on 100-mil centers, is not new. It was originated by IBM in the late 1960s and is still used there in house. For years, it was regarded as too expensive and complicated, but VLSI has brought it to the fore.

The pin array's big advantage over the chip-carrier is size or interconnection density. As an example, the 160-pin array occupies less than one half the area of a 160-pin Jedec-type chip-carrier on 50-mil centers.

Another major advantage of the pin-array packaging is that its pins are on 100-mil centers. This allows it to be mated with today's pc technology based on designs on a 100-mil grid. In addition, pin arrays can easily be wave-soldered or socketed to a pc board that, unlike the leadless chip-carrier, does not require special handling.

The pin array is available from 3M, Kyocera International Inc., Augat Technical Ceramics, and Japan's NTK Technical Ceramics. Like the chip-carrier, it is available in both cavity-up and cavity-down versions. Cavity-up versions, which can be fully gridded, have a higher density than cavity-down types, where surface area must be dedicated to the cavity. In the same size substrate, for example, a cavity-up type could hold 196 pins while a cavity-down unit could hold 132 pins. Cavity-down types have better heat transfer, though.

Not all pin-grid arrays are fully gridded. Some of the most popular types have a double row of pins around their periphery. In any case, however, they are more space-efficient than a comparable chip-carrier.

Pin-grid arrays still have more room for growth. Most packaging experts are already considering using a 50-mil grid with the technique, particularly for VHSIC parts or multichip applications requiring at least an 18-by-18 matrix (324 pins).

3M is already contemplating pinless designs, which will be known as leadless grid arrays. The socket and contact technology developed by 3M for the 64-pin quad in-line package can be applied to socketing pin-grid array packages. The Jedec JC11 committee is currently in the midst of a program to develop a standard family of pinned and leadless grid arrays that will be on a 100-mil center-line grid.

Lithography advances

In IC processing, a whole new generation of lithography equipment is starting to emerge aimed primarily at VLSI and VHSIC chips. The first two machines to surface are from Hewlett-Packard Co., Palo Alto, Calif., and IBM Corp.'s General Technology division in East Fishkill, N.Y.

Both new electron-beam machines have high throughputs and are basically direct-writing machines of the type needed for VLSI production. The HP machine uses a modified raster-scan imaging technique that has registration accuracies between 0.1 and 0.2 micrometer and can be used for exposing geometries in the 0.5-to-1-μm range. The machine writes at rates of up to 300 megahertz, giving it a throughput of five wafers per hour for chips with as many as 1,350,000 transistors each.

IBM's EL-3 is a third-generation electron-beam lithography tool developed for IC fabrication using direct-writing techniques. The system uses state-of-the-art techniques that will show up in commercial electron-beam systems within the next few years. These include: a learn-calibrated field scan, a high-current variably shaped spot, a subfield vector-writing technique, and the ability to handle workpieces up to 165 mm in diameter.

Upping throughput

The EL-3 can expose thirty 4-inch wafers per hour using 1.5-μm lithography at 10-microcoulomb-per-centimeter current density. Four EL-3s have been completed and installed. One of the units is currently in place on IBM's automated production line in East Fishkill.

Along with the electron-beam systems, other techniques of IC processing have advanced during the past year. In the field of plasma etching, a new entry—

Applied Materials Inc., Santa Clara, Calif.—came out with a machine with guaranteed high performance. In the field of sputtering, Materials Research Corp., Orangeburg, N. Y., began to deliver a radically new high-throughput machine, and in annealing of ion implantation damage, Varian Associates' Extrion division, Gloucester, Mass., demonstrated a new type of isothermal annealing.

Applied Materials' AME 8100 series is an ion-assisted plasma machine that can do anisotropic etching of oxides, polysilicon, and single-crystal silicon, silicon nitride, aluminum, and organic materials. The company guarantees such parameters as edge profile, etching rate, line-width uniformity, etch-rate uniformity, and selectivity. Guaranteed uniformities apply to within a wafer, wafer to wafer, and run to run.

The 8100 processes twenty-four 3-inch or 100-millimeter wafers per hour or eighteen 125-mm wafers/h. An automatic mechanism loads and unloads wafers from standard cassette carriers to special wafer trays. The heart of the system is a novel vertical processing chamber with a hexagonal multifaceted cathode structure.

Materials Research Corp.'s system 80 is an in-line wafer-sputtering system with a throughput of 125 wafers/h regardless of wafer size. The system uses a unique wafer transport mechanism, which maintains a constant wafer flow and imparts a constant rotation to each wafer. The transport holds each wafer on three rollers at a slight angle to the vertical, rather than using a horizontal belt or air track.

Varian has developed a machine that uses a new form of isothermal annealing to repair ion-implantation damage in silicon wafers. Rapid isothermal annealing heats an entire wafer for a short time by radiant thermal energy. The process, which employs a simple graphite heater in a vacuum chamber, is more energy-efficient than other annealing methods.

In experimental tests, complete 3-inch wafers were annealed in a single 10-second exposure with high activation for implants of boron. Leakage currents of implanted pn and np diodes were comparable to furnace annealed wafers. Diode leakage was minimal.

The plastic chip-carrier owes a lot to Grabbe

By the end of 1982 the surface-mounted leaded plastic chip-carrier will start populating boards in many commercial types of electronic equipment. One of those responsible for bringing this package to the fore is Dimitry Grabbe, recently appointed director of technology at Amp Inc., Harrisburg, Pa. The Yugoslavian-born engineer came up with the concept of the premolded package in the mid-1970s and carried the idea through to a whole family of devices and a full line of automatic assembly equipment.

In 1972, Grabbe sold his own company, Maine Research, a firm that did both systems packaging and fabrication of multilayer boards, and began consulting for Amp Inc. A year later he joined Amp as a full-time corporate staff member.

In Grabbe's own words, he was told "to make himself useful." He then proceeded to find areas of technology where he could help other Amp technical people and selected the packaging of monolithic integrated circuits as an area that would grow with time.

In November 1974 Grabbe's group at Amp took the first step in the evolution of the premolded plastic carrier by making experimental quantities of premolded plastic dual in-line packages. The same technique was quickly applied to assembling a newly designed plastic chip-carrier and in 1975, the firm built the prototype of the first premolded chip-carrier. By the next year, a complete assembly line for bonding and sealing chips into the new packages had been designed. Amp was shortly producing units accommodating as many as 68 leads or sockets.

Today Amp is the only firm that can supply a premolded plastic chip-carrier in 20- to 84-lead versions plus all necessary assembly equipment. The Amp units will be used by firms that will bond and seal their own custom chips into the carriers as opposed to buying standard integrated circuits already encased in plastic carriers by their manufacturer.

In the future, Grabbe foresees these carriers being attached to printed-circuit boards partly by surface-mounted sockets and partly by direct soldering to the board surface. In his view, the higher-lead-count carriers with more expensive, complex chips will always be socketed, since desoldering a multileaded package is laborious and possibly damaging to its circuit board.

As for the next primary packaging for very large-scale ICs, Grabbe expects leaded and unleaded chip-carriers with closer input/output spacing—on 20-mil centers and even less eventually. Nor does he anticipate any difficulty in interfacing such dense pinouts with present-day pc boards, based though these are on a 100-mil grid and 10-mil lines and spaces. As he observes, most independent pc makers can now routinely manufacture 8-mil lines and 8-mil spaces—he recalls that his former company could manufacture multilayer boards with 4-mil lines and spaces way back in 1973. Either one of these board types could easily interface with chip-carriers having leads on 50-mil centers and even tighter I/O spacing.

In his new position at Amp, to which he was appointed in September, Grabbe will be responsible for three technical areas—advanced products, plastics molding, and automation and robotics. A senior member of the Institute of Electrical and Electronics Engineers, he is on the steering committee of the Computer Packaging Society. **-Jerry Lyman**

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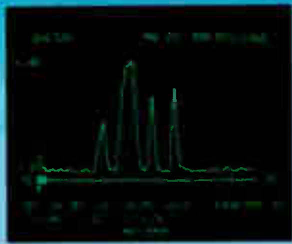

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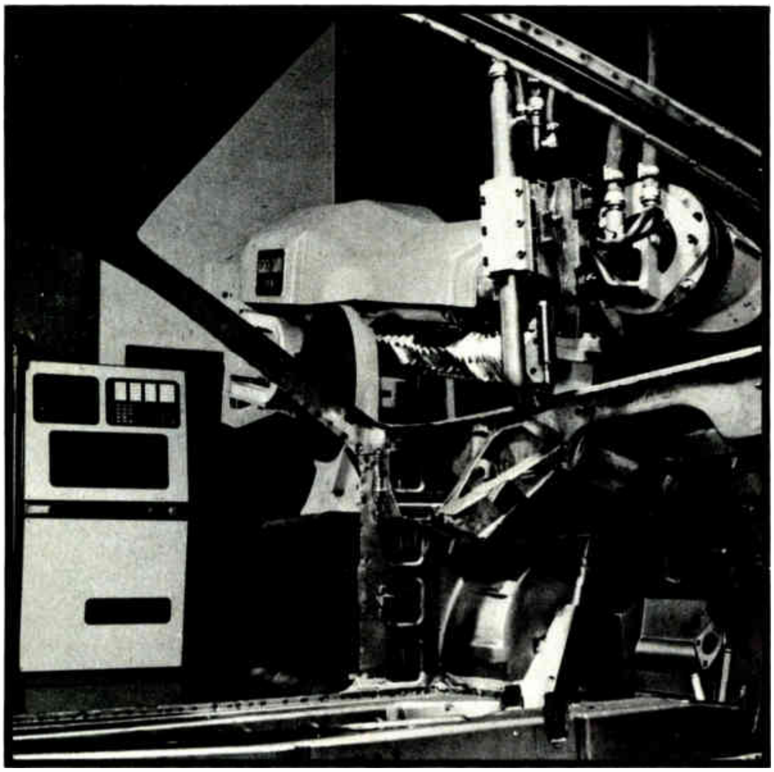

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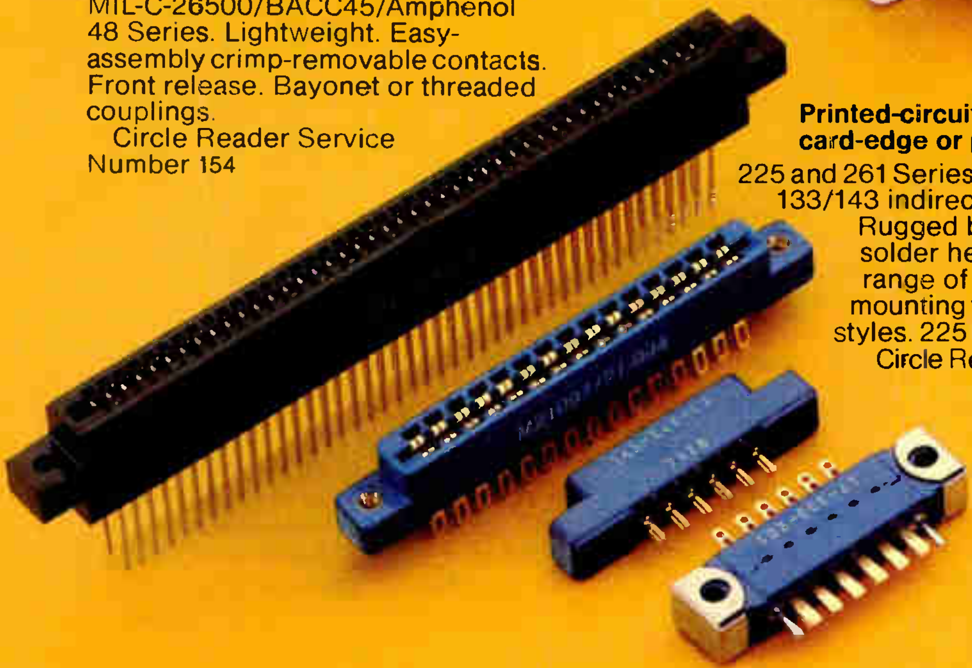

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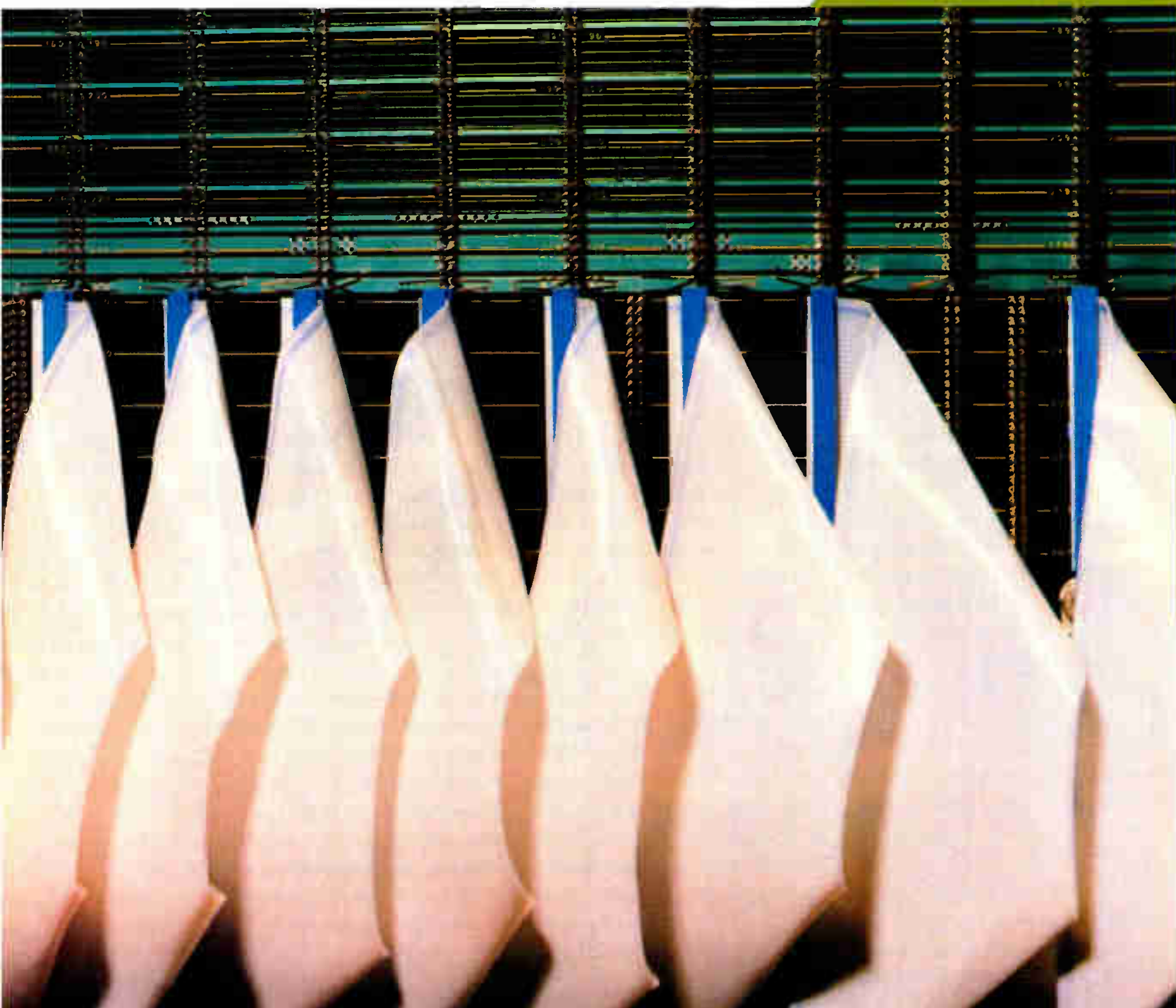


Route to growth. In keeping with the general trend to greater modularity in instrumentation design, the backplane of the GR 16 shown above is only one of three bus structures within the VLSI tester, each tailored to different data rates in accordance with the functions performed in the system.

Tools in general and logic analyzers and field testers in particular gain greater functional integration and automation that will refine their use in design and field service

by Richard W. Comerford, *Test, Measurement & Control Editor*

☐ 1981 might have been predicted to be a rough year for bringing new products to market, but a surprising number of hardy instrumentation companies forged ahead through the economic gloom to develop more sophisticated design tools and instruments that by the decade's end may fully automate the engineering process. Goading the companies forward was, among other factors, the rapid spread of 16-bit microprocessors, which created a demand for testers to test the chips and the temptation to redesign instruments around them. Other driving concerns included how to automatically test very large-scale integrated circuits and how to test boards with VLSI's higher test point counts.

Some of the gains made this year include faster and broader logic analyzers, high-speed digitizing and improvement in digital scopes, more sophisticated automatic testing systems that can be upgraded as VLSI evolves, lower-priced testers for specific applications, increased troubleshooting capabilities, and better field-service testing systems that may eventually become obsolete as the design of self-testing chips matures.

VLSI, with its opportunity for greater numbers of functions on a single chip, is also suggesting new paths for product design. Silicon foundries, perhaps the most prominent example, are changing the way companies approach product design, production, and service. Designers now are asking for tools that interconnect to automatically move information from one stage of the process to another, and the instrument companies are answering with tools that can be linked together to gather and transfer this information. The day is quickly approaching for integrated, computer-aided industry.

Even without VLSI, the number of electronic systems in use is growing at an astounding rate—so quickly it is outstripping the industry's ability to provide qualified people for their maintenance. Faced with this shortage of individuals able to service complex logical systems, industry has once again turned to the instrument companies for an immediate solution, though at the same time hoping ultimately for ways to avoid the task of field service altogether. Within the next few years of the search for more reliable systems, industry must decide to what level and in what manner those systems will be able to check themselves.

The new logic in logic analysis

Logic analyzers moved in four important directions this year—toward higher speeds, greater modularity, greater functionality, and better interfacing. In the coming year, these directions will be further underscored as instrument companies enhance their existing units with more modules or introduce new units that will boast these features.

Early in the year, Gould Inc.'s Biomation division of Santa Clara, Calif., broke through the 100-megahertz barrier to address the increased use of faster logic. Through use of emitter-coupled logic, the $22,625 K500-D, an eight-channel unit, is able to track logic transitions in the 500-MHz range and to capture glitches as brief as 3 nanoseconds.

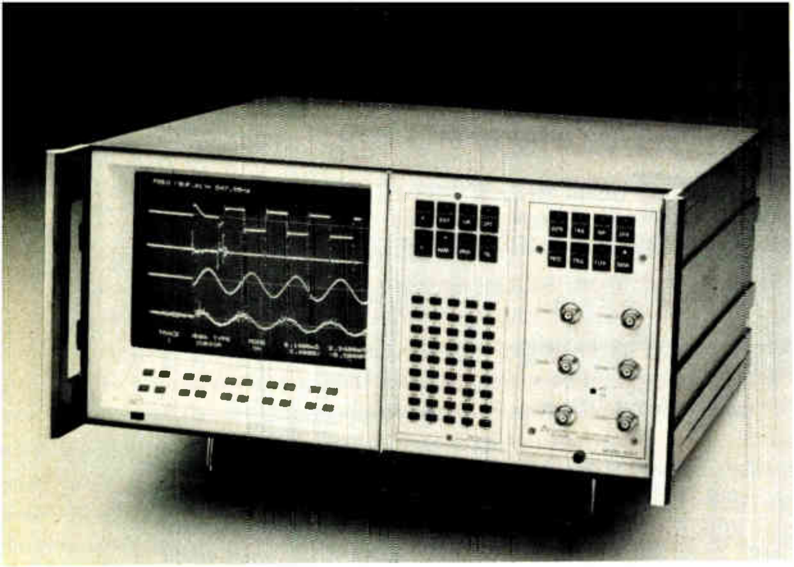
With higher-speed logic a phenomenon throughout the industry, speed is also the byword for engineering in general—that is, letting the engineer work faster. At Xerox Corp. in El Segundo, Calif., engineers built their own sampling logic analyzer and combined it with a microcomputer for a system that both stimulates and measures chip response. The system reduces from months to days the time needed to generate test programs for the company's Sentry system, thus achieving the industry goal of cutting product development time while increasing engineering productivity.

A similar combination of stimulus and response turned up what may be considered the most important logic analysis tools to be seen this year. In March, Dolch Inc. of San Jose, Calif., and Dietzenbach, West Germany, introduced the Emulyzer both in the U.S. and Europe. The $5,000 unit, which connects to the microprocessor socket of a board under test, can be downloaded with software from a development system to stimulate the board while it is examined by a separate logic analyzer which it triggers. The unit can also be used as a stand-alone emulator.

The most dynamic solution to logic checkout, however, came at Wescon this year in the form of the DAS 9100 from Tektronix Inc. in Beaverton, Ore. That system, priced at $16,900 in a typical configuration, can bypass development systems altogether, permitting the hardware designer independently to create test vectors that then trigger the data-capturing side of the box.

The DAS exhibits a major trend in instrument design that will continue through the decade. By the use of printed-circuit cards rather than plug-in modules, it is configurable for a wide variety of test conditions, both in the number of stimulus channels and for state and timing analysis.

Configurability of cards is also the hallmark of the latest logic-analysis product from Nicolet Paratronics Inc. of San Jose, Calif. The NPC-764 mimics the com-



Analog terminal. Designed to tackle a variety of analog waveform measurements, Analogic Corp.'s Data 6000, left, is primarily a digital system. All analog readings are digitized by a plug-in such as the 6002 at right before they are passed along to a 68000 processor.

pany's system 5000 in that it can be configured for various logic-related capabilities using cards. The unit's appearance is more like that of a portable terminal than a traditional instrument, which underscores its computational capability. In fact, the unit can serve not only as a logic analyzer but as a development system and even as a personal computer. Users must simply obtain CP/M-compatible software on floppy disks from independent suppliers for these uses.

Another significant aspect of Tektronix' DAS 9100 is the comprehensive set of menus by which it operates. This relieves the user of the burden of studying the operating manual, letting him or her settle immediately to the task at hand. Extensive menuing is also part of the K101-D from Biomation, whose choose-the-value menus make it simple to set up complex nested triggered schemes. While designers will value the performance of the 100-MHz, 48-channel unit, the unit's $23,500 price tag may present an obstacle. If they can live with a 50-MHz unit, Dolch's LAM 4850A, unveiled at Wescon, can be obtained for half that price. But if they need the speed, Gould's $16,900 K102D will give them 32 channels with which to check out designs.

The number of new logic analyzers introduced this year is just one of the indications of the market's lure for instrument makers. Another is the fact that the Iwatsu Electric Co. of Japan, best known for its high-end scopes, has introduced a $9,800 state-and-timing analyzer with 16 channels having a maximum rate of 20 MHz and 9 channels of 100-MHz capture. Competition from both Europe and Japan will no doubt invigorate analyzer sales in 1982.

Digital refines analog

The strong emphasis on logic analysis underscores digital design as the motivating force behind the entire industry; the digital domain is even encroaching on the measurement of analog waveforms. That this will continue is inevitable: VLSI presents the possibility of designing entire instruments on a single chip, provided that the design is largely digital. VLSI could make possible, for example, a single-chip oscilloscope.

The year's best witness to this phenomenon is the Data 6000, a waveform-measurement computer from Analog Corp.'s Data Precision division in Danvers, Mass. Even though the system is intended to thoroughly dissect analog data, the unit is almost entirely digital. After the signal is fed into the unit's plug-in, sampling at rates up to 100 MHz turns it into digital data that exits through the back of the plug-in and travels through the unit's digital backplane.

With push-button control, the system manipulates the data in ways engineers typically use calculators, thus saving the time of transferring data between machines.

Other examples of such digital manipulation are the 4094 from Nicolet Instrument Corp. of Madison, Wis., and the Triad II system from GHI Systems Inc. of Rancho Palos Verdes, Calif.

The 4094, called a digital scope, uses its 16-bit processor to manipulate digitized signals in accordance with programs from floppy disks. Plug-ins able to digitize 2-MHz signals are available, and the manufacturer will also supply measurement programs on disk for the system, which is priced typically at $13,400.

For lower-frequency signals, to 200 kHz, Triad II combines a specially modified Commodore Pet computer with a separate waveform digitizer, with which users can dissect signals for as little as $4,950.

The connection

Common to all the above systems and to all instruments introduced this year is the IEEE-488 bus, with which many individuals are linking the systems they need. The bus's creator is HP, which early in the year introduced a rack-mounting version of its HP-85 computer—the controller used most—at a price of just $1,675.

In August, Tektronix also introduced its first dedicated IEEE-488 controller, the 4041, as part of a new series of modular instruments called the TM 5000. That controller, priced at $4,995 in its execute-only configuration, addresses the lack of formal standards for bus codes and formats with Tektronix' internal standards. As such, it can control any Tektronix instrument with efficient, easily understood code and will be in agreement with the Institute of Electrical and Electronics Engineers' codes and format standards when they are released.

The TM 5000 series is similar to the earlier TM 500, except that all its modules are programmable via the bus. Especially noteworthy, however, are the series' function generator, with its programmable waveform symmetry, and the 350-MHz counter-timer, able to resolve 1 picosecond for repetitive signals. Tektronix will no doubt add to this system in the future.

Another bus-compatible signal source introduced this year was the HP 8161A. Designed to check out logic as fast as emitter-coupled logic, the 100-MHz unit's pulse output can verify tolerances, while the user adjusts the rise time of the pulse.

Among other notable bus-compatible instruments are the model RF 9303 radio-frequency millivoltmeter from Racal-Dana Instruments Inc. in Irvine, Calif., and the company's model 488 nonintrusive bus tester.

To forecast the future, the design of bus-compatible instrumentation will be influenced strongly by the vast commercial market created by the U. S. Air Force's modular automated test equipment program, or MATE. Sperry Corp.'s Systems Management Group located in Great Neck, N. Y. (in August awarded the title of prime subcontractor for the program after competing with Westinghouse), has already opened a dialog with industry to explain the program's goals.

From design to production

While the modularity of MATE will permit configuration and reconfiguration of systems for military subsystem testing and thus achieve cost reductions, the modular approach has its champion in the commercial ATE world, too. GenRad Semiconductor Test Inc. of Milpitas, Calif., introduced a highly modular general-purpose VLSI test system in January of this year, which despite the capital crunch has already won the acceptance of IBM, Westinghouse, and United Technologies. In its initial form, the GR 16, the 40-MHz unit could take on 144-pin devices. In March the company raised the pin count to 288 with its GR 18.

With its highly modular structure—each functional area of the system can be expanded by adding cards and functions increased by adding cabinets—and its well-organized bus structures, the system is obviously the one to beat. And Accutest Corp. of Chelmsford, Mass. has taken up the gauntlet with its 7900 system. A 50-MHz tester, the 7900 claims an accuracy of 500 ps after autocalibration, but has fewer pins per test head than the GR system.

Yet the GR series, at 40 MHz, still addresses what potential customers at last year's IEEE Test Conference in Philadelphia established as their major need in test speed. Further, the GenRad STI system is designed to permit additional increase in test speed when that stage is reached. While STI awaits that time, it is concentrating on producing focused testers: models for production testing that are geared to special devices such as memories and microprocessors. Those systems, with much lower price tags than the GR 16's $480,000 base price, should appear next year.

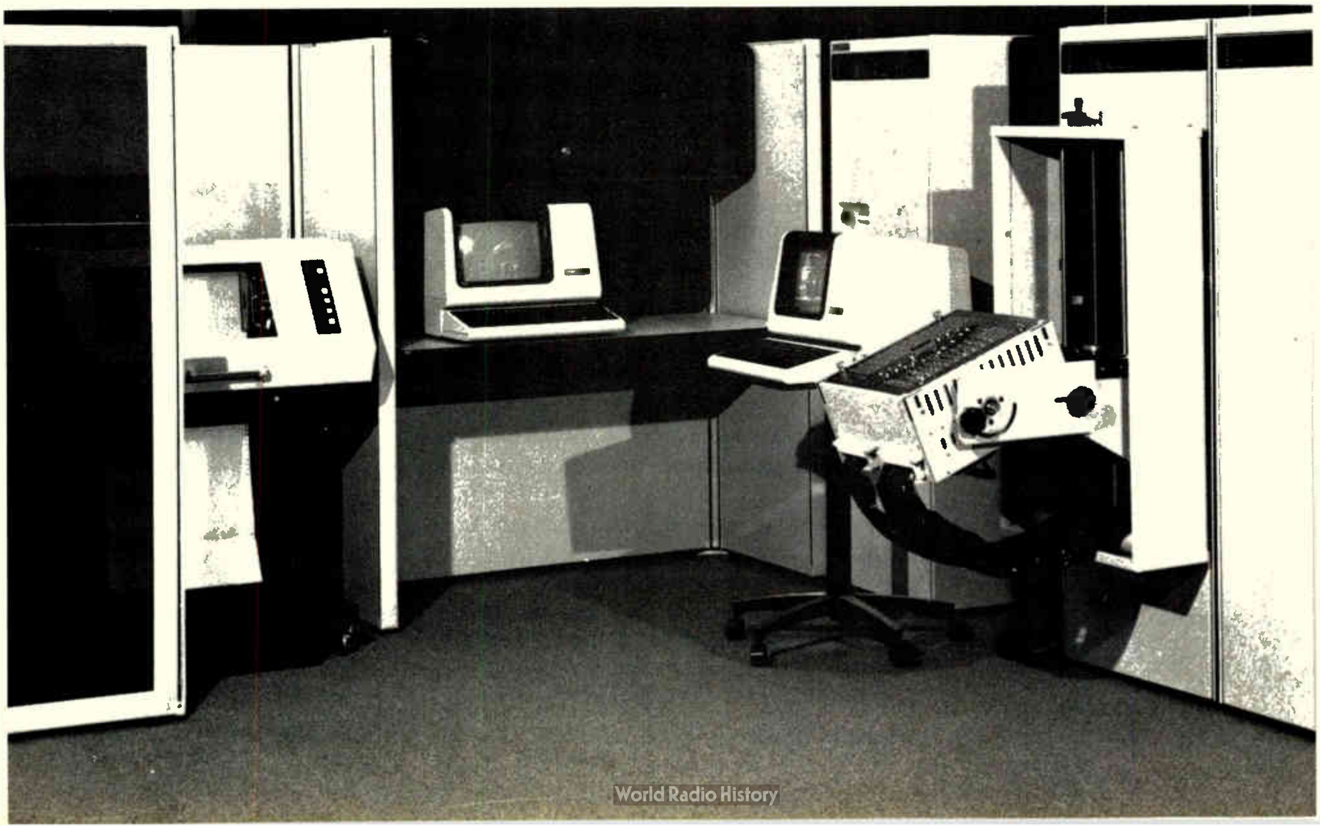
However, another general-purpose VLSI test system is emerging from Teradyne Inc.'s Semiconductor Test division in Woodland Hills, Calif., to provide even more competition for the fledgling company. Called the model 941, the unit will provide long streams of test vectors without stop, and will make possible a tie-in with test-generating CAD systems.

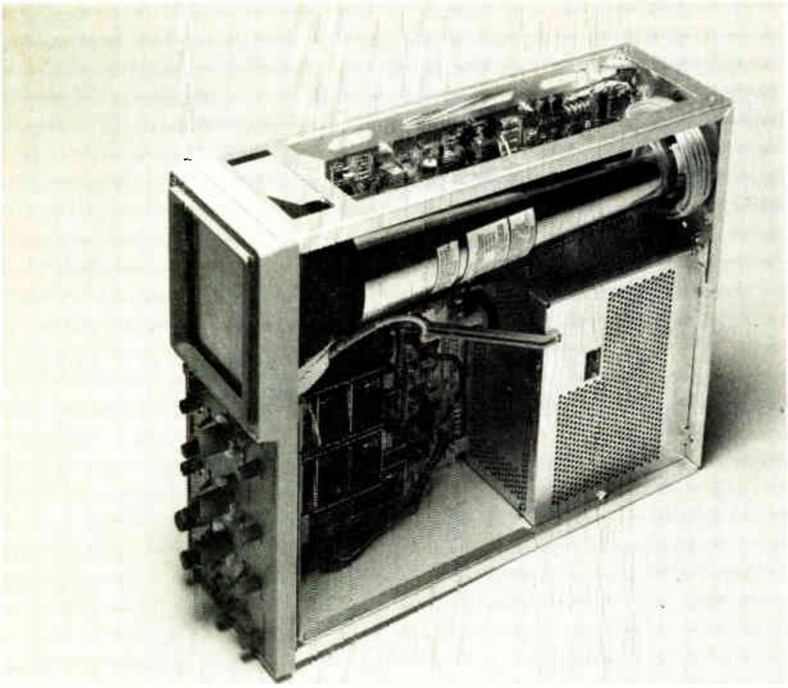
The idea of focused testers was championed by Eaton Corp.'s Semiconductor Test division also of Woodland Hills, Calif., (formerly known as Macrodata) with its Detective series. With the introduction of the 002 system, compatible with the 001 for memory-chip characterization, but without the extra bells and whistles needed for that function, the company offered production testing at $100,000. Further, all the systems in the series are programmable in a high-level, English-like language that reduces programming time. The company's next move will be to refine the interface between device handlers and test systems for truly compatible units.

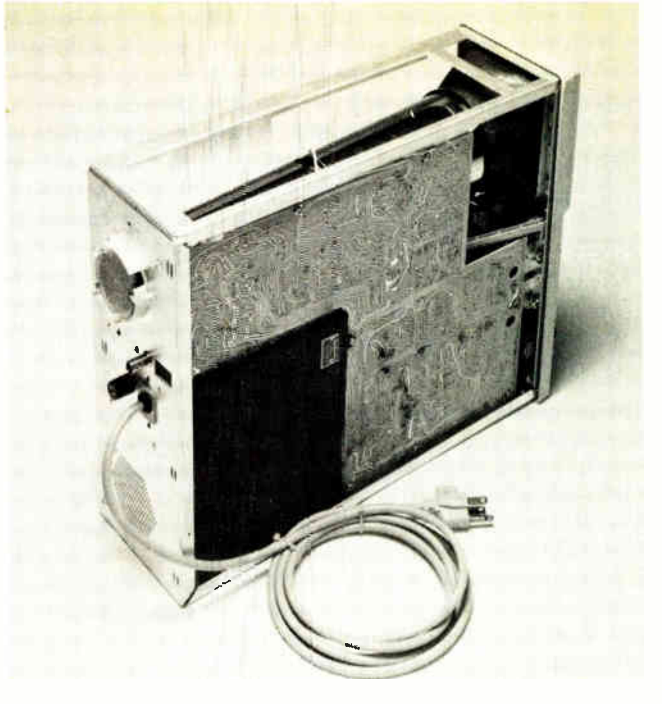
Computer Automation Inc. of Irvine, Calif., also addressed the problem of test program generation in its Sprint system for board test. The software, called MUSE, not only permits programming in English, but can also act as a translator so that other test software can be used.

Based on market competition, industry's vote this year seemed to favor in-circuit over functional testing. HP's

Form follows function fashionably. Housed in each of the cabinets of GenRad's GR 16 are a set of associated functions that each occupy an individual crate, or rack, in the cabinet. Enhancing the VLSI tester's functionality is its pleasant "high-tech" physical design.







Less is more. The lowest-priced ($1,100) and lightest (13.5 pounds) scope in its class, Tektronix' 2213 (left) owes its roomy interior to its having 65% fewer parts than scopes like the 455. As seen above, a single board holds all parts to automate assembly.

Loveland, Colo., division extended troubleshooting to beyond a particular test node so that devices tied to the same node could be examined separately with a guided probe. Further, the company endowed the system with its signature-analysis stimulus source, thus opening a possible path from production to field service via signature analysis. On the other hand, Plantronics Zehntel Inc. of Walnut Creek, Calif., targeted the increasing number of pins on boards with its Troubleshooter 900 system, which has 3,024 universal test pins. The system's ability to test ECL, TTL, and MOS devices confronts the problem of mixed logic, a phenomenon increasingly common in board designs.

Not willing to fall behind in this vital market, GenRad has introduced its 2271 and 2272 in-circuit test systems, which have higher pin counts than the 900 and can also check mixed logic. Further, the systems work at faster throughput rates and thus reduce damage to good components overheated during backdriving.

While the emphasis has been on in-circuit testing, the functional tester is far from dead—at worst it is dormant. That a board's components are in the right slot, or even that each component works correctly, is no guarantee that the output at the card edge will be right. Functional testing needs the stimulus of a goal such as a simpler way of analyzing and programming for functional responses; but this depends on the development of more sophisticated CAD systems.

Bare-board testing, though, is an area that has recently come to life. The market for new testers has jumped because companies have finally started treating multilayer boards as complex interconnection systems and have in turn motivated their multilayer suppliers to check outgoing parts.

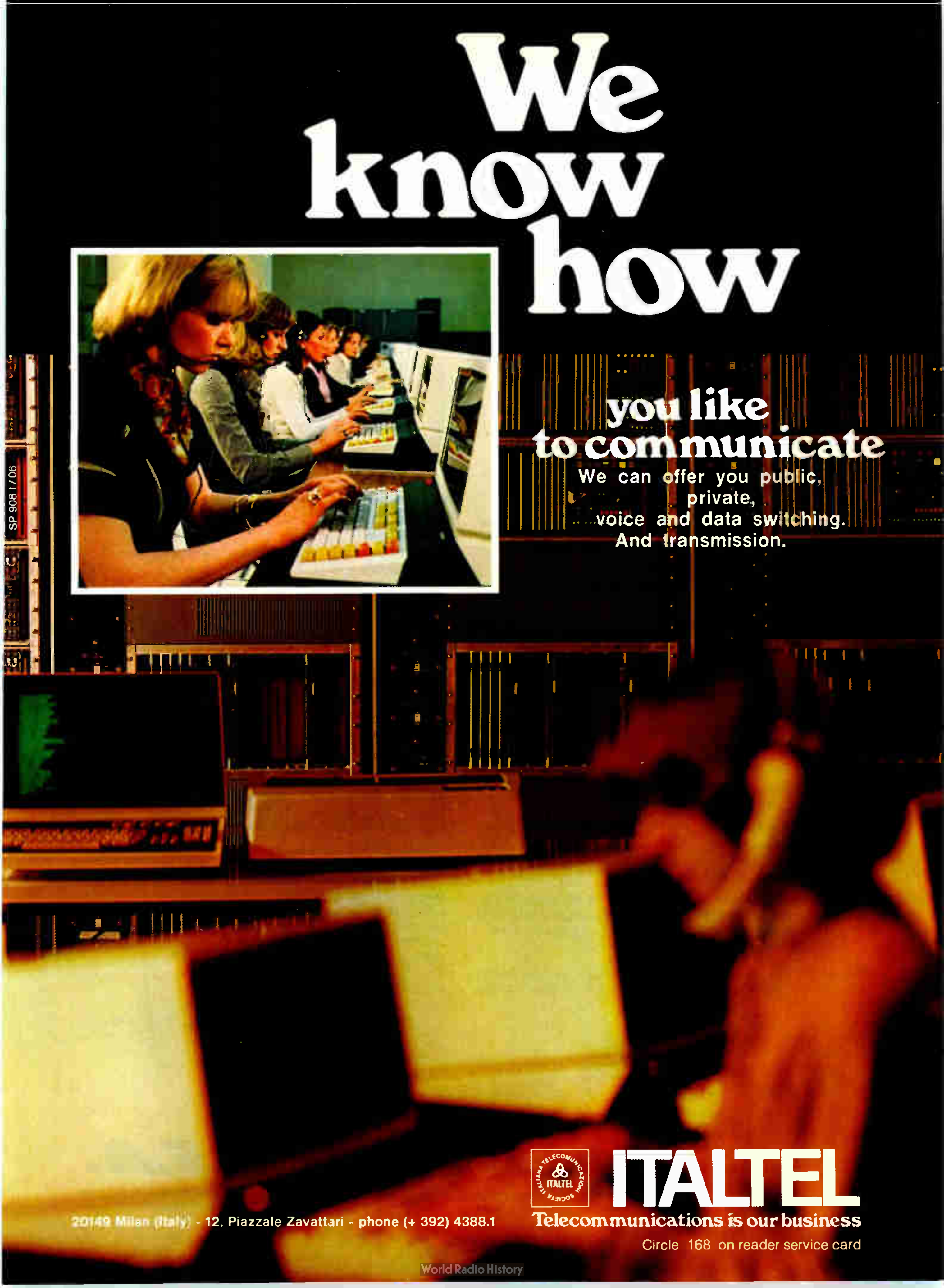
Two eye-catching systems came out of California, from Express Computer Systems of Anaheim and Fluke Automated Systems of Mountain View. Both systems take the tack of offering multiple test stations served from a central computer, thus increasing the number of boards that can be tested in a given time while spreading the cost of the central processing unit among multiple test heads. Fluke's 3200 system can also check the resistance and leakage of the boards, a critical factor when high-speed signals must traverse them.

To the field

The brightest star in Fluke's galaxy of test equipment this year, however, was not its production tester but its field service unit, the 9100. The unit addresses the immediate problems of field service: propelling boards out of the field-to-factory float and back into service with minimum training of technicians. Fluke engineers approached this by devising a special algorithm with which the instrument can learn the address locations of various devices on a known good board and immediately begin to check similar boards. Test programs using the unit can be placed on magnetic tape and distributed to field service personnel. The programs guide the technicians with messages, enabling them to isolate faulty components even without the technician's immediate documentation or knowledge of microprocessor-based designs. Most attractive, however, are the system's under-$4,000 price tag and its adaptability to present and future processors via the change of a pod.

Tektronix also is hoping for sales success with its newest field service scopes. Two new families were introduced this year. First off the line was the 2300, an extremely rugged 100-MHz scope that will succeed the 465 series that for so long has been the industry's bulwark.

But the family that created the biggest stir, with its under—$1,500 price and its low weight and parts count,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High cost wrap/pin boards made OBSOLETE

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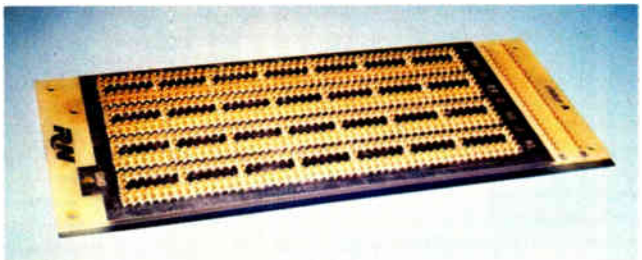
You'll never willingly use wrap/pin for boards again. Consider these advantages:

1. **High speed wiring simplicity**—You connect just **one** wire per connection. There is **no time-consuming insulation stripping** as needed with wrap/pin.
2. **Fast, easy wiring changes**—Repair or modify boards by simply removing the individual wires and quickly re-wiring. Field wiring modifications are simple and fast.
3. **Meets highest reliability standards**—Durable four-finger BeCu contacts and fully heat treated IDC tines insure gas-tight performance.
4. **High density low profile boards**—The "Q/C" board profile is only 0.235″ compared to the 0.703″ wrap/pin board. "Quick/Connect" boards go right into production racks.
5. **Wiring machines available**—The semi-automatic wiring machines now in use can be readily modified for the "Q/C" system. Also, semi-automatic "Q/C" machines are available.

This is not just a "dream" system. A major electronics firm is currently using the "Quick/Connect" system on a regular basis.



Many standard "Quick/Connect" prototype socket boards are available now—with a wide selection of 1/0 configurations and board sizes. COMPUTER INTERFACE BOARDS for DEC* PDP-11 and LSI-11. Apple** interface boards also. MICROCOMPUTER BOARDS in INTEL Multibus*** as well as S-100 configurations now in stock.

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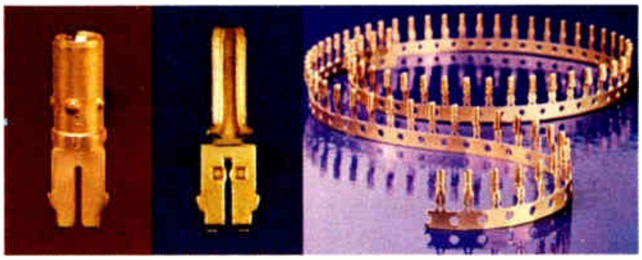

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Write or call today for full details on this new point-to-point wiring system that will obsolete wrap/pin boards. The time and money savings are truly phenomenal!

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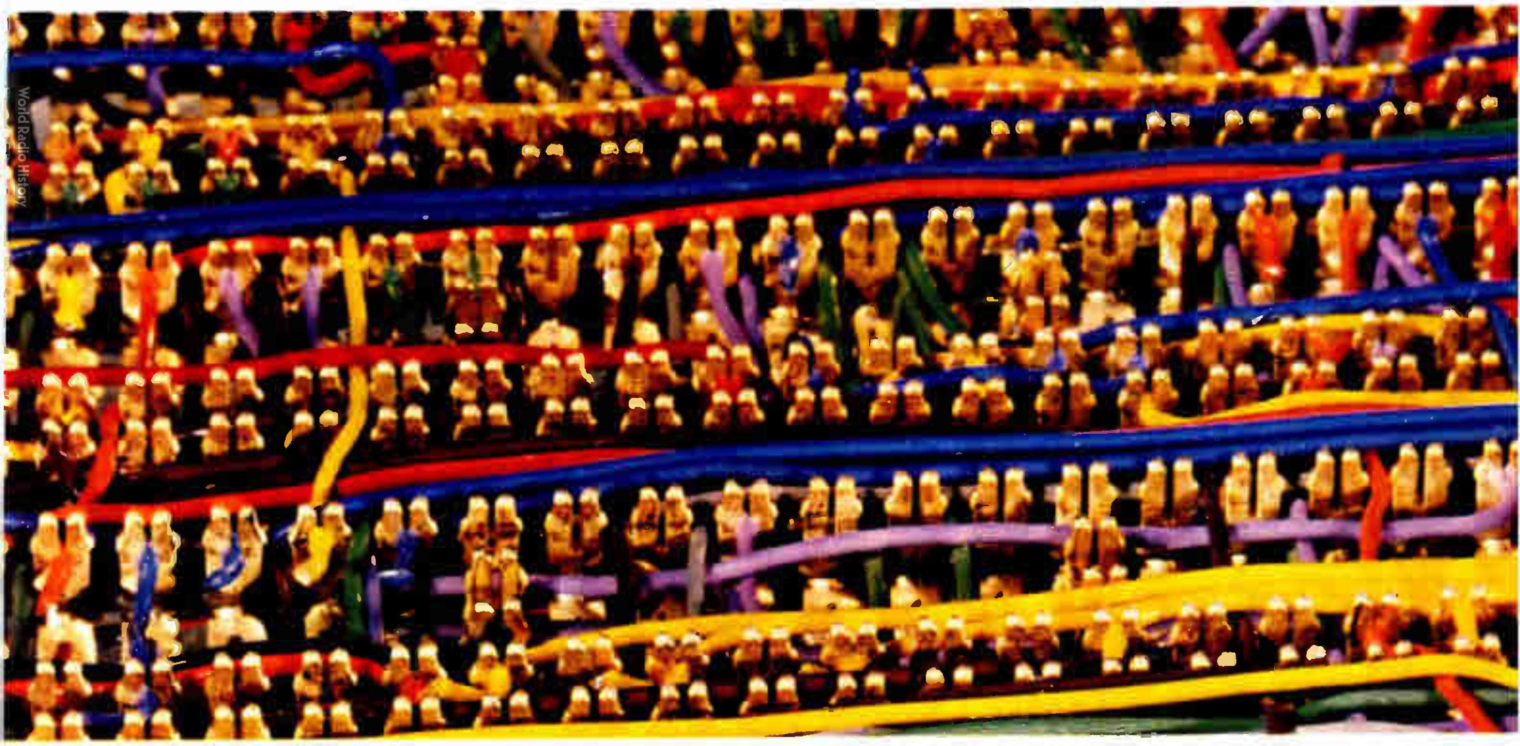
An "eyeball" comparison tells you instantly that "Quick/Connect" has got to be faster to wire, far less costly than wrap/pin boards!



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Circle 172 on reader service card

was the 2200 series. To be fabricated on a highly automated production line in the future, the scopes will be marketed not only to Tektronix' base of industrial customers, but also to smaller customers through a special distribution center. Philips Test and Measurement Instruments countered this move at Wescon with its 50-MHz 3215 and 3217, and foreign manufacturers will join the competition by the end of next year.

The most common field service tool, the multimeter, also underwent significant change in 1981. The resolution of the hand-held digital multimeter increased from 3½ to 4½ digits, permitting field service personnel a better fix on, for example, the voltage output of copier power supplies, a critical factor in some of the new units.

The first to offer a 4½-digit multimeter in the form factor made popular by Fluke was Keithley Instruments Inc. of Cleveland, Ohio, and it did so for $219, the lowest price likely to be seen for a while. At the same time, Data Precision increased the mobility of an earlier series of minimeters in its 255 by using a nickel-cadmium battery, making the unit practical for field use.

Form is often perceived as an important aspect of this market, as borne out by Data Precision's introduction seven months later of the model 945, which follows the standard hand-held design. The unit, which weighs some 8 ounces less than the 255 but 3 oz more than Keithley's 135 (and costs about $45 more), has the added capability of characterizing diodes.

As important as the equipment itself is who will use it. Due to the shortage of skilled technicians and the rapid spread of electronic systems, the third-party service market has grown dramatically in the past few years and shows no signs of slowing in the near future.

Yet the cost of service is such that it has also attracted the attention of engineers who would like to eliminate service calls altogether, by means of built-in testing both at the board and the chip level. These schemes, multiplying with each passing year, have already been incorporated in some systems and can be seen in the most recent chips, such as Intel's iAPX 432.

For VLSI testing, Albrow devised the GR series

Despite his youth, Bob Albrow is an old pro in the automatic test equipment industry. At 38, the native of Slough, England, has had a major hand in many currently used test systems and is the architect for the first wholly new generation of very large-scale integrated-circuit testers—the GR series from GenRad Semiconductor Test Inc. in Milpitas, Calif.

One thing that accounts for Albrow's mastery is that from the start he concentrated on tester design. After receiving his master of science degree in engineering from London University in 1966 and then soloing briefly, Albrow started a careeer that tracked a number of corporate mergers and acquisitions.

First, he teamed up with Tony Davis to become "the fourth or fifth of Membrain's founding fathers." (Membrain Ltd. in Wimborne, Dorset, UK, was acquired by Schlumberger in the late '70s.) He designed Membrain's first product—the MB 1000 functional board tester.

Albrow arrived in America in late 1973 to work for the John Fluke Manufacturing Co. in Mountlake Terrace, Wash., but he felt that his work there was "out of context—not where I could contribute most." In 1974 he moved to Xincom Corp. in Chatsworth, Calif., under Brian Sear, whom he had met while employed at Membrain.

Albrow flourished at Xincom. As product planner and system architect for the company's memory-tester line, he introduced the first host computer for tester satellites, distributed functionality in design, and parallel testing to increase throughput. He also devised an enhanced timing system so that the 5580 memory test system could operate without dead time between cycles, an unpatented technique that Albrow says he will "copy forevermore."

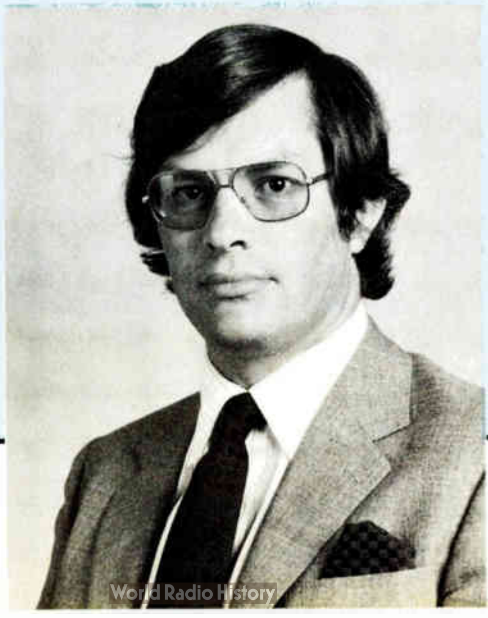
The memory test product line took Xincom from a small, $1 million company to a $10 million market leader, but Albrow says the management atmosphere began to change when Fairchild Camera & Instrument Corp. took over in 1978. "The style became nonconducive to entrepreneurs," he states.

At that time, he also sensed a slowdown in semiconductor tester design. So in July 1979, he and Sear joined GenRad to see what could be done, and the next January the 80%-GenRad-owned STI subsidiary was formed.

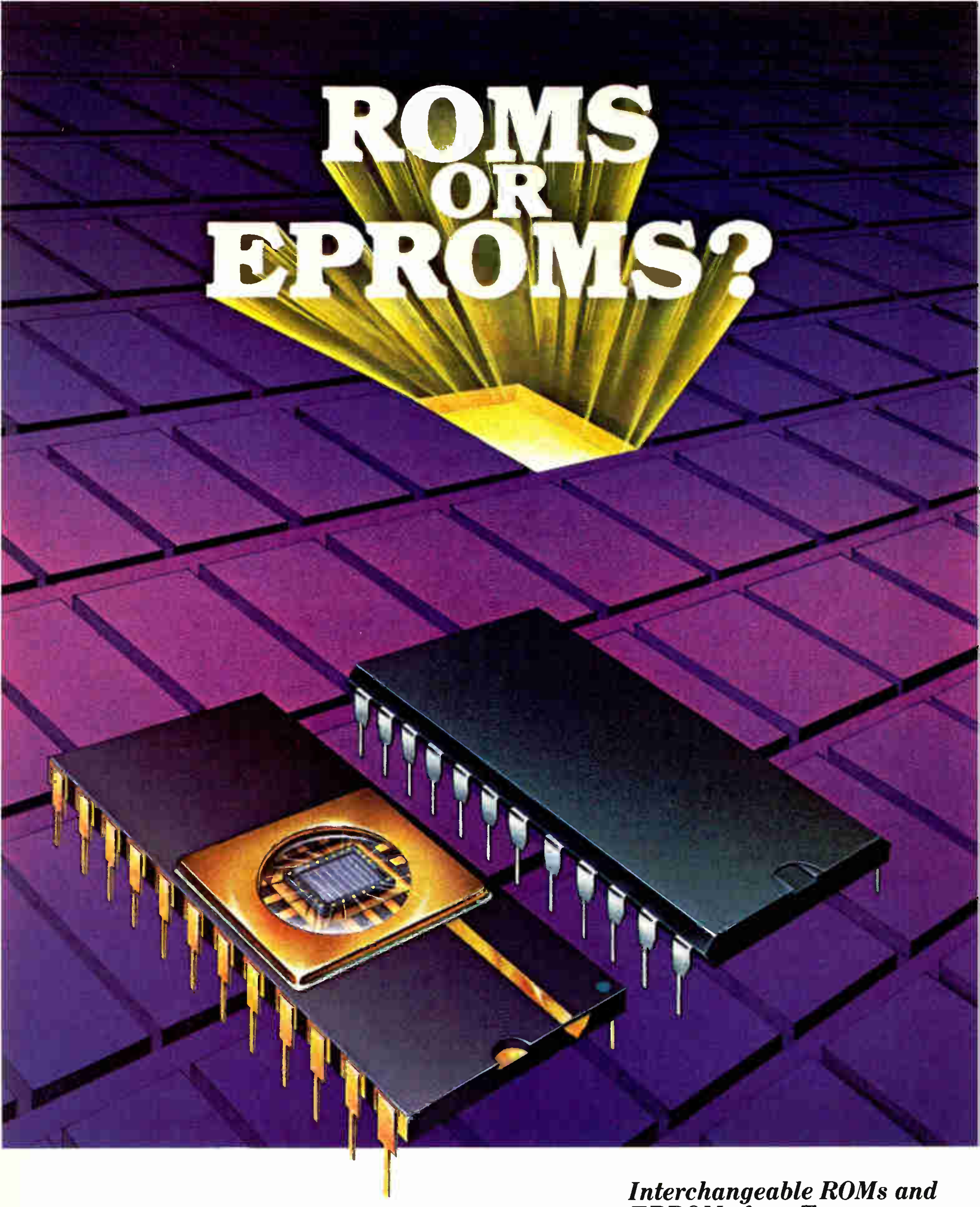
The architecture for the GR series was actually laid out in the first three months of the association. "On the first day, we decided that the line from Digital Equipment Corp. would give us the right price and performance," and so it was chosen for the GR series' central controllers. "It's becoming a DEC world, and if your testers are not running from a DEC machine, you're in trouble," Albrow says.

By the mid-1980s, Albrow believes all test-program generation will be automated. To him, this means every pin on a tester will have to be truly universal since "you can't describe personality cards to a computer in any reasonable fashion." Further, with the number of vectors growing, "1s and 0s won't work" as a means of programming the system, so an algorithmic pattern generator must be an integral part of the vector-generation stream.

Albrow already is developing new product designs for the next generation of semiconductors. General-purpose testers and focused testers for classes of devices like microprocessors or memories will be "fundamental," he predicts; he also sees markets for testers dedicated to just one type of device, such as dynamic random-access memories.



But despite this diversity of technologies and tasks facing the ATE industry, Albrow says "there's only one game in town—to integrate functions so you can give more functions per dollar." Or, the buck stops at the architect's desk. **-R. W. Comerford**



Interchangeable ROMs and EPROMs from Texas Instruments, the total memory supplier.

Here are tips from Texas Instruments on which to use when. Your decision may hinge on economics.

There are times when your system design will clearly dictate either ROMs or EPROMs. At other times, the dividing line between the two is hazy. That's when a careful analysis of the economics involved — particularly the recent substantial pricing changes in the marketplace — may tip you to one or the other with considerable long-term savings as a result.

Texas Instruments, a leader in non-volatile memories and a broad-based supplier, can deliver the byte-wide ROMs or EPROMs you need. And from its years of experience with these memory devices, TI offers suggestions that may help you decide on the least expensive solution for your system.

The case for ROMs

In general, ROMs provide more memory for less cost than any other semiconductor memory. The key to their use is high volume and high memory capacity — on the order of 32K and 64K. Coupled with programming — performed by the supplier — that will not change or need to be updated.

In these circumstances, ROMs are especially cost effective. Total costs are spread so widely that per-bit cost is relatively inexpensive.

Consumer and computer peripheral applications where the volume of end products is large can make very economical use of ROMs.

The case for EPROMs

Prices for 16K and 32K EPROMs have declined significantly, and those for 64K devices will follow suit. Making EPROMs economically attractive, especially for applications where the program is likely to change.

Programming is easily performed by the user, and there is no mask charge. One EPROM type can be used for many different programs. Which means lower inventory costs and no write-off costs when programs vary.

TI's High-Density ROMs

Device	Density	Power Dissipation*	Access Time*
TMS4732-35	32K	440 mW	350ns
TMS4764-35	64K	440 mW	350ns

TI's Leadership EPROM Family

Device	Density	Power Dissipation*	Access Time*
TMS2564-35	64K	840mW	350ns
TMS2564-45	64K	840mW	450ns
TMS2564-50	64K	840mW	500ns
TMS2532-25	32K	840mW	250ns
TMS2532-35	32K	840mW	350ns
TMS2532-45	32K	840mW	450ns
TMS25L32-45	32K	500mW	450ns
TMS2516-35	16K	525mW	350ns
TMS2516-45	16K	525mW	450ns
TMS2508-25	8K	446mW	250ns
TMS2508-30	8K	446mW	300ns

*Worst case over operating temperature range

If you are in a hurry to get to market, EPROMs can be your best bet. They are available from multiple sources on short lead times.

One additional advantage: Because of their programming flexibility, EPROMs are an excellent prototyping tool prior to conversion to ROMs. And, at the end of a product's life when both volume and the number of ROMs being used decline, converting back to EPROMs can cut costs.

The case for Texas Instruments

Whether ROMs or EPROMs or both, Texas Instruments fills your requirements with reliable, proven-in-the-marketplace memories that are fully compatible with each other.

A system designed with appropriate memory addressing can utilize TI's 16K or 32K EPROMs or TI's 32K or 64K ROMs on the same printed circuit board in the same 24-pin socket.

In ROMs, you have a choice of the high densities that spell economy — 32K and 64K (see table). These are fully static memories — no clocks, no refresh — that require only a single 5-V power supply. They are fabricated using N-channel silicon gate technology for utmost dependability. All inputs and outputs are TTL compatible. Maximum access and minimum cycle times are 350 ns.

In EPROMs, you have the broadest choice in the industry — 8K through 64K. All have the same basic pin configuration to ease memory capacity expansion.

Weigh the pros and cons of ROMs vs. EPROMs. Evaluate your system requirements and carefully check out the economics. Then call your nearest TI field sales office for prices and delivery on your choice. Of course, if you still have doubts about which is best for you, we are ready to consult with you at any time.

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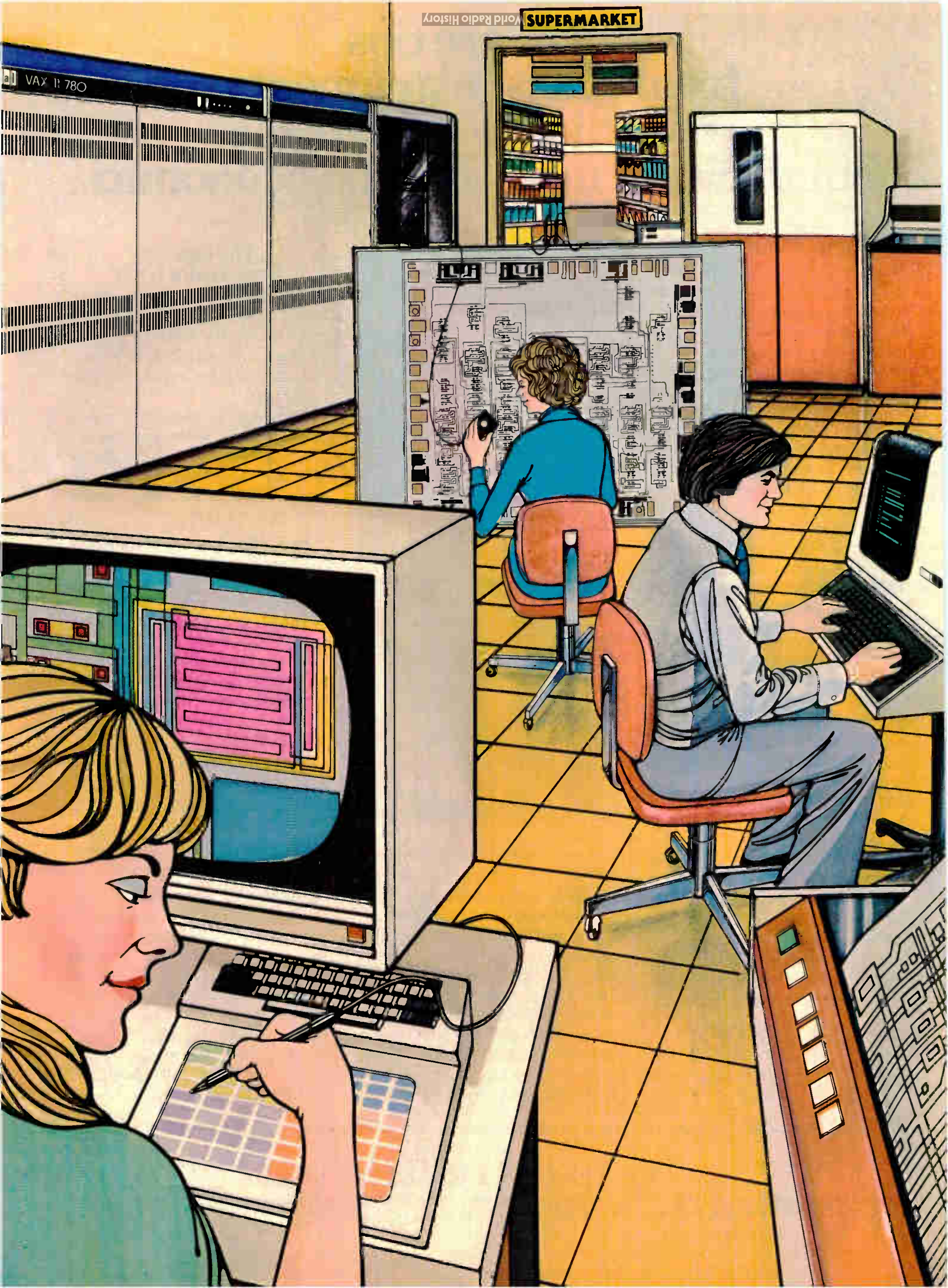
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At the heart of the system is the Applicon graphic system linked with the DEC VAX 11/780 computer. Peripherals include design stations, engineering terminals, high speed printers, a 42″ electrostatic plotter and a pattern generator. The hardware is designed to handle arrays of VLSI complexity.

SOFTWARE

Building on the Applicon 860 Super VSLI foundation, Interdesign has added powerful software developed specifically for gate arrays. For verifying layout versus logic automatically, there's the **InterCheck**™ software. Truth tables are converted to test programs and translated to test equipment format with the **InterTest**™ software. Circuit and test program verification are accomplished through interaction between the **InterSim**™ software and the digitized logic diagram. And, in development, is **InterLink**™, the software tool needed to convert logic diagrams to I.C. layouts automatically.

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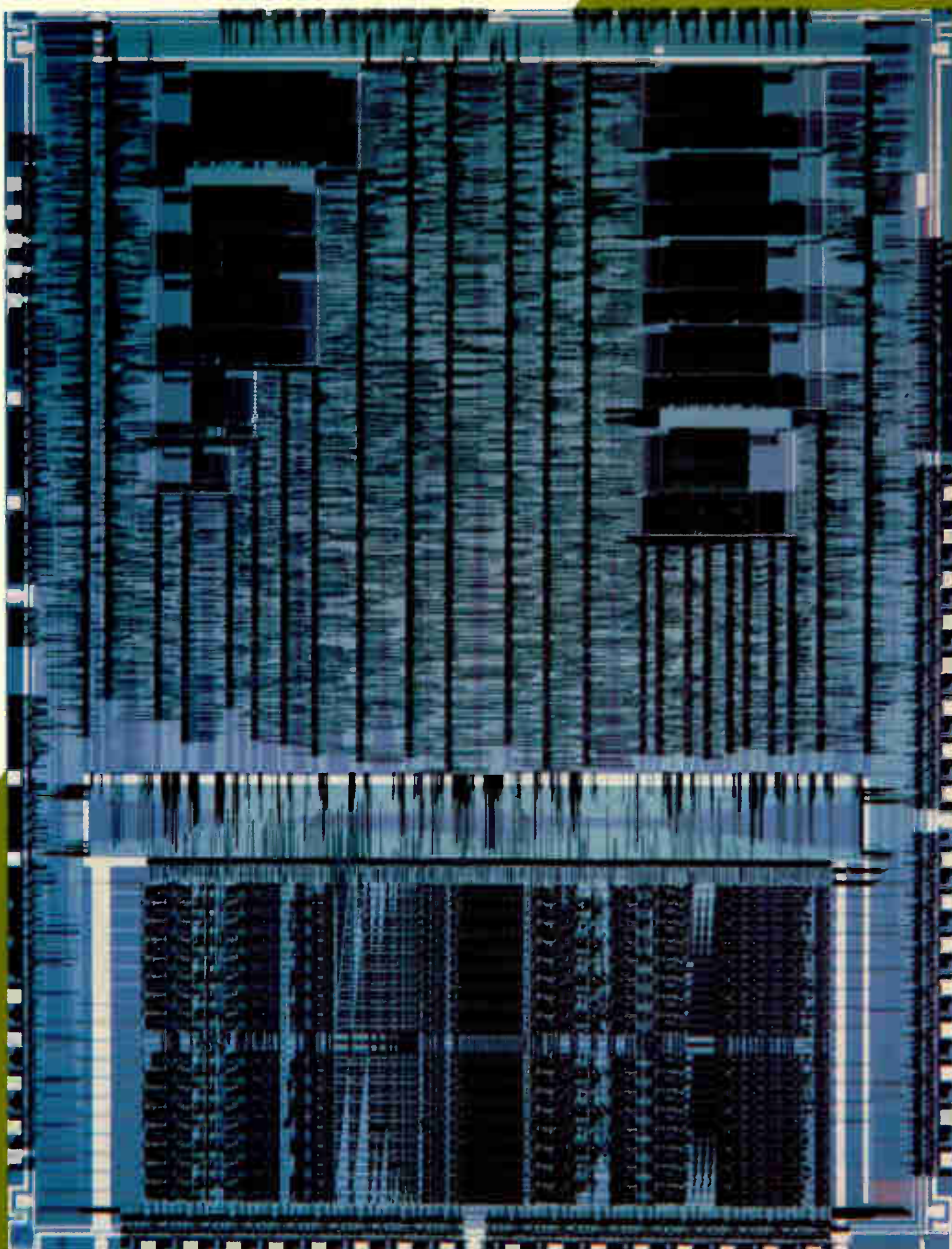
MICROSYSTEMS



Reaching to 32 bits. This microprocessor from Bell Laboratories uses a conventional architecture but with full 32-bit data paths and twin-tub complementary-MOS processing.

A plethora of microprocessors—custom or commercial, special- or general-purpose—is unfolding, along with new support circuits and better development systems

by R. Colin Johnson, *Microsystems & Software Editor*

□ Microsystem technology is growing by leaps and bounds and apparently toward truly integrated silicon solutions. Semiconductor houses have recognized the need for system-level support and are competing not only for that main processor socket, but in peripheral support chips and software. Even as excursions into state-of-the-art 32-bit machines and exotic architectures marked 1981, the battle for dominance in the 16-bit arena is raging wildly. Two major research centers introduced very large-scale 32-bit processors with conventional architectures for internal use, while one very unconventional three-chip microprocessor for the commercial market uses an object-oriented architecture that hides its internal structure from the programmer in order to allow its data and programs to more closely resemble the information they represent. Also, several more well-established minicomputers have been transferred to very large-scale integrated-circuit implementations in order to reap the benefits of a large debugged software base.

While the 16-bit contenders slug it out with multiple alternate sources and increased software support, a new generation of special-purpose processors is emerging, making high-speed controllers a breeze and complex function generation simple. Also, one new 8-bit processor was announced—though it will probably be the last of its kind since the world of electronics has enough good 8-bit machines as it is.

On the support scene, most microprocessor manufacturers pulled through and are now delivering the memory-management units promised last year. They are also bringing out, slowly but surely, the other support circuits needed to build all-VLSI system solutions. With the new multiuser development systems that use sophisticated operating systems and debugging support, it is getting easier and easier for designers to utilize all that silicon.

Bigger microprocessors

The trend to ever-larger-scale IC technology for microprocessors was dramatically demonstrated this year, at the International Solid State Circuits Conference held in New York. Three new microprocessors designed to handle 32-bit data types were discussed: the Bellmac-32 from Bell Laboratories; Hewlett-Packard Co.'s as-yet unnamed 32-bit machine; and Intel Corp.'s iAPX-432.

The complementary-MOS Bellmac-32 from the Murray Hill, N. J., lab and the C-MOS-machine from HP's Desktop Computer division in Fort Collins, Colo., are of conventional, albeit state-of-the-art, architectures, with the Bell machine featuring novel domino-circuit technology and a twin-tub process. Neither part, however, is currently manufacturable for mass-market distribution, with the HP processor sporting over 450,000 transistors, and with the similarly giant-sized die on which the Bellmac-32 is built. However, they do prove the point that 32-bit microprocessors can be built at least for internal use where die price is less sensitive.

Even though 32-bit processors with conventional von Neumann architectures are bound to keep showing up, it is unlikely that they will soon find many design-ins, since the 16-bit machines are only currently coming into their own. This year marks the tenth anniversary of the first microprocessor (Intel's 4004); 8-bit processors have had a market for over six years now; and the 16-bit machines are likely to last even longer.

Intel's 32-bit three-chip n-channel MOS set, however, is not of a conventional architecture. The 432, from the Aloha, Ore., Special Systems Operation, works on memory-resident objects that can range from simple data types like integers to complex data structures like records, all the way to complete processes—subroutines—or even auxiliary processors. It also realizes the long-sought-after dream of a user-transparent multiprocessor configuration—the ability to simply plug in more processors in parallel to increase speed.

When conventional benchmarks like the typical add time are used to compare the 432 with other microprocessors, it does not stand out. However, it was not designed to be a number cruncher, but rather to fit into information-intensive applications like data-base management. More processors that are designed with object-oriented high-level languages like Ada in mind are likely to surface, especially for application areas like office automation.

The tendency to build these next-generation processors using C-MOS technology can be directly related to the increased amount of heat they must dissipate. Thus manufacturers without a good C-MOS process are likely to be left behind in the 32-bit race. The Japanese introduced two manufacturable C-MOS 16-bit processors last year, and more are bound to follow this year. Toshiba Corp.'s 88000 is built on sapphire, runs at 10 megahertz, and uses an external control store.

There will be more VLSI implementations of minicomputers, as well. That move marks an excellent way in which to salvage the extensive software bases that many minicomputer users enjoy. Thus Digital Equipment Corp. realized a single-chip implementation of its very popular PDP-11/34 minicomputer, and NV Philips

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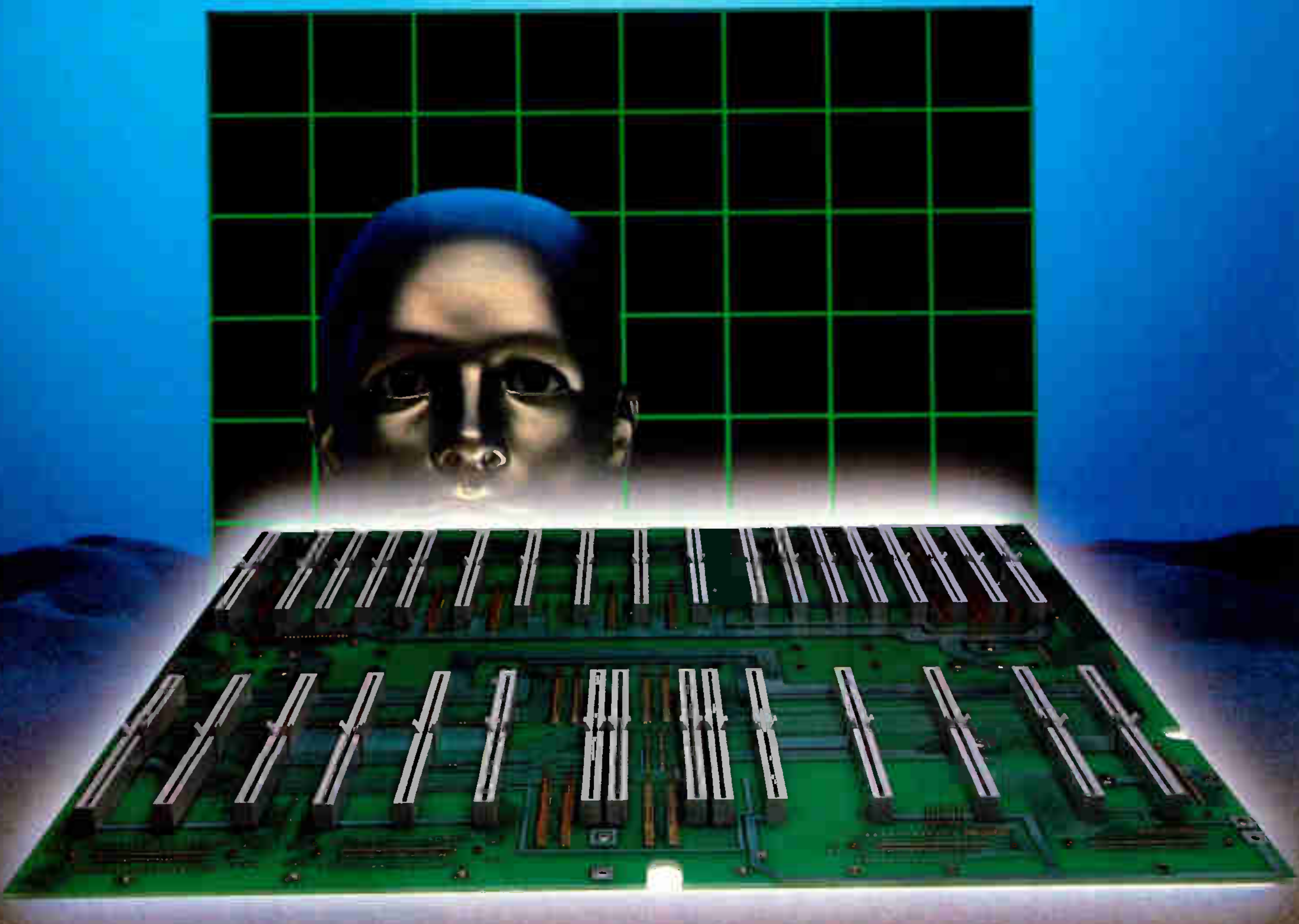

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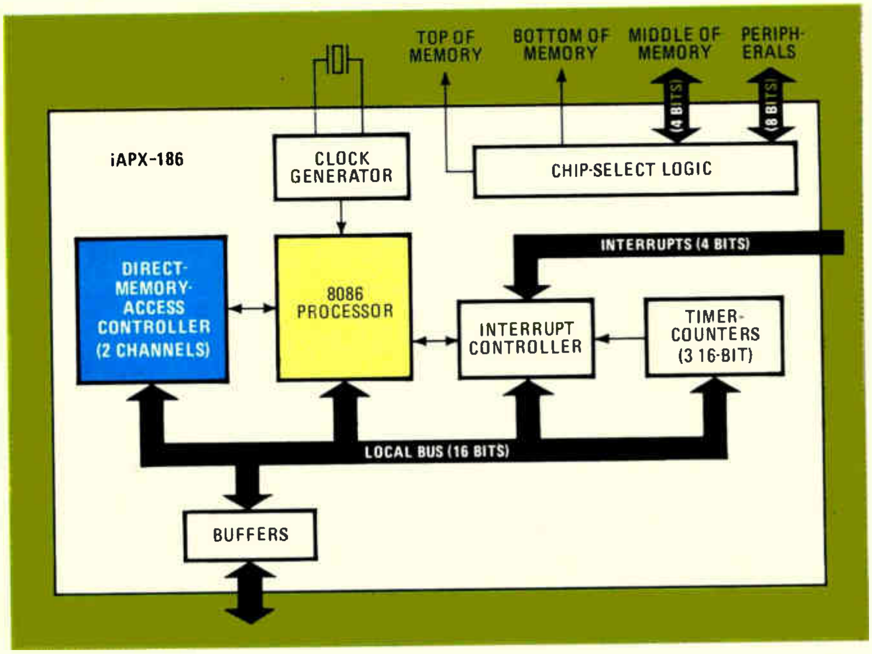

One-chip 8086. Intel's iAPX-186 has an instruction set compatible with the 8086, but is 30% faster and brings on chip all the hardware necessary for many industrial applications. It has two direct-memory-access channels and three 16-bit timers.

er—and partly to try to fill some of the ever-increasing number of 8-bit sockets being designed into new applications by original-equipment manufacturers.

The result is its TMS 7000 series of single-chip microcomputers that has gleaned the best of its competitors' instruction sets and rolled them up into a package that allows the user to add his own custom instructions. However, this move is an exceptional one, and any other new 8-bit microprocessors should be compatible with a present instruction set. Producers are going to stick with their standard lines, while enhancing them with new on-chip special functions, such as memory-management units and serial interfaces as well as implementing them in low-power C-MOS technology.

An innovative example of this phenomenon is Zilog's proposed Z800 processor, which maintains compatibility with the Z80. However, it will also come with a 16-bit bus interface for increased throughput and for compatibility with the new 16-bit bus standards.

Silicon support

One way to increase microprocessor capabilities is to take a leaf from the book of mainframes makers by offloading auxiliary chores as a means of increasing throughput. So chip makers are designing and starting to manufacture many support ICs.

The most widely recognized need is for special-purpose chips devoted to managing large semiconductor memories. In multitasking systems utilizing big stores, software organization of the memory space involves too much overhead to be practical. Some sort of hardware segmentation must be invoked in order to make optimal use of that resource.

Memory-management units can also allow program size to be independent of the size of the memory resident on the target processor. In this way, identical programs can be run on different systems with small and large memories, since the mapping mechanisms can translate addresses and swap in missing segments in a manner transparent to the programmer.

All the major microprocessor manufacturers now offer memory-management companions, and all use some sort of segmentation. Motorola's MC68451 employs an elaborate set of masking mechanisms to identify users, their privilege levels, and the logical addresses from the processor, which are then translated into the physical addresses delivered to the memory system.

To identify those logical addresses on the fly, the 68451 uses a fast content-addressable memory, as does Zilog's forthcoming Z8015 and National's 16082. On the other hand, TI's 74610, Motorola's MC6829, and Zilog's Z8010 merely use the upper address bits to feed a decoder that activates a wider physical address.

The other key issue in memory management is protection. Users should not be able to gain access to each others' programs; data should not be executable; the operating-system code should be inaccessible to users; and so forth. All of the 16-bit memory-management units pay a great deal of attention to protection.

The iAPX-286 includes an on-chip memory manager whose primary function is protection, but that also has the job of translating logical into physical addresses. Rather, Intel chose to widen out the four base address registers already on the 8086 in order to maintain compatability with that part. The program itself must reload these base registers each time a different segment of code, data, or stack is to be accessed.

What these widened base registers do bring to the party is protection against illegal accesses due to an improper privilege level, read-only status, and absence from physical memory, among other dangers. This sort of on-line hardware-protection mechanism can slash processor overhead, especially in multiuser situations where such swapping is done in and out of main memory.

Correcting errors

Another area of activity in peripheral support chips is error detection and correction. Now that semiconductor densities have shrunk to the point that alpha-radiation and other noise sources are significantly affecting memory reliability, error-detection and -correction techniques are becoming mandatory. Disk technology is also calling for error detection and correction, since higher densities are affecting reliability there, too.

For example, AMD's Z8065 burst-error processor uses an advanced Fire code to correct disk error bursts that can be as long as 12 bits. Others are building their own error-correction circuits using regular TTL circuitry, and


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there is even a company now whose sole service is to design custom error-correction circuitry for disk-controller manufacturers: Data Systems Technology in Broomfield, Colo. Many more error-correction large-scale ICs will appear next year, since practically none of the new memory systems larger than 1 megabyte can afford to ignore this problem.

More competition is also likely to appear in graphics controllers, like the low-end TMS9918 from TI and the high-end μPD7220 from Nippon Electric Co. Standard Microsystems Corp. has plans to implement its popular 8002 video terminal attribute controller using its high-speed titanium-disilicide process, resulting in the 25-megahertz 8002H.

Another active area is multiprocessor synchronization and message passing. Two offerings this year, the ZFIO from Zilog and the MC68120 from Motorola, are intelligent buffer memories for message passing. These are well-designed examples, and more versions are sure to follow next year.

Many of the major players in the development-system market concentrated this year on making good their commitments. HP's Colorado Springs (Colo.) division for example, began delivery of 16-bit emulators for its LDS 64000 in September.

Tektronix Inc., which last year announced its plans for growth of its line of development systems, spent this year putting the pieces of that plan in place. For example, in May the Beaverton, Ore., firm introduced the trigger-trace analyzer, able to give a good look at 16-bit processor performance, and last month it began deliveries of its 8540 host computer system. Later this year, the company will start shipping its multiuser system, the 8560 which is built around a Unix-like operating system that the company calls Tnix.

Tektronix's decision to go on its own with development systems left its former supplier, Millennium Systems Inc., free to pursue its own path. The Cupertino, Calif., company quickly brought forth its own stand-alone emulator, the 9508, which could work with other development systems and with its own software-development system, the 9520. At Wescon, Millennium moved into the 16-bit hardware arena with its 9516 stand-alone emulation system. Before too long, the aggressive little company should have its Unix-based multiuser system moving out the door.

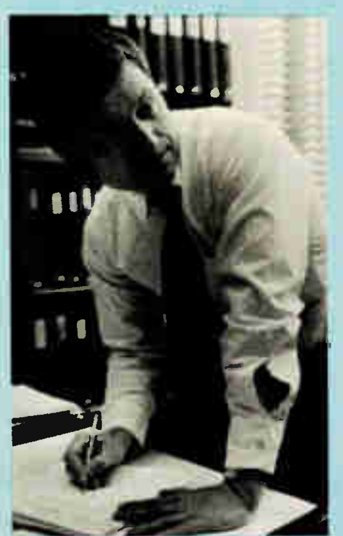
While Intel has been relatively quiet in this game this year, it has pursued a path of steadily expanding software support for its installed base of development systems, which is the largest in the industry. It is doubtful that the company will give it up without a powerful fight, so 1982 should be the year in which it moves to reassert its dominance.

Pushing to gain greater recognition for its development systems while trying to gnaw away at Intel's lead is TI. The company unveiled its Multi-AMPL system in the summer and became the first company to take trade-ins that could be used in discount against the price of a new TI system. These trade-ins may be from any manufacturer, which is also a first.

A monolithic 32-bit microprocessor is 'most satisfying' to Murphy

Long a believer in systems on a chip, Bernard T. Murphy has spent the last 15 years at Bell Laboratories in pursuit of that goal. The latest achievement by the team he leads at the Murray Hill, N. J., facility is a 32-bit processor on a chip: the Bellmac-32.

In the mid 1970s, Murphy came to feel that American Telephone & Telegraph Co. should turn to microprocessor-based systems and further that these processors should execute high-level languages. He decided, too, that machines large enough to execute high-level languages would dissipate too much heat for n-channel MOS, so a complementary-MOS technology would be the way to go for Bell.



Consequently, Bell's first microprocessor, the Bellmac-8, used C-MOS, although not a conventional process. Standard C-MOS employs a p-type load for each n-type device, but the Bellmac-8 shares a single load transistor among many n-type devices.

Murphy's design team then turned out the Bellmac-4, a single-chip version of the 8-bit design, and this year produced the ground-breaking 32-bit Bellmac-32. This new processor "was the most satisfying of all my contributions to silicon technology," he says, because he was responsible for every aspect of the design effort, beginning with the establishment of system requirements.

After taking a Ph.D in medical physics from Leeds University, Great Britain, he came to Bell after brief periods at Westinghouse Electric Corp. and Siliconix Inc. While at the former, Murphy made his first major contribution to silicon technology—the invention of the buried collector, a technique used almost universally today. After his move to Bell Labs, Murphy made another ground-breaking contribution—a method for calculating yields of integrated circuits that is also still widely used and that helped to convince Bell of the practicability of integration.

In addition, his description of collector-diffusion isolation won him his second major patent. His first one, of course, was awarded to his buried-collector invention.

Nowadays, Murphy's team is concentrating on what he calls technology-updatable computer-aided design. In this, the data base used to create masks is independent of the process and thus can quickly revise mask specifications when tighter design rules become practicable.

Unlike some other CAD specialists, he feels that "the silicon compiler is the wrong way to go. Human creativity is not automatable and symbolic representations allow you to retain that most important of all our resources in the loop." **-R. Colin Johnson**

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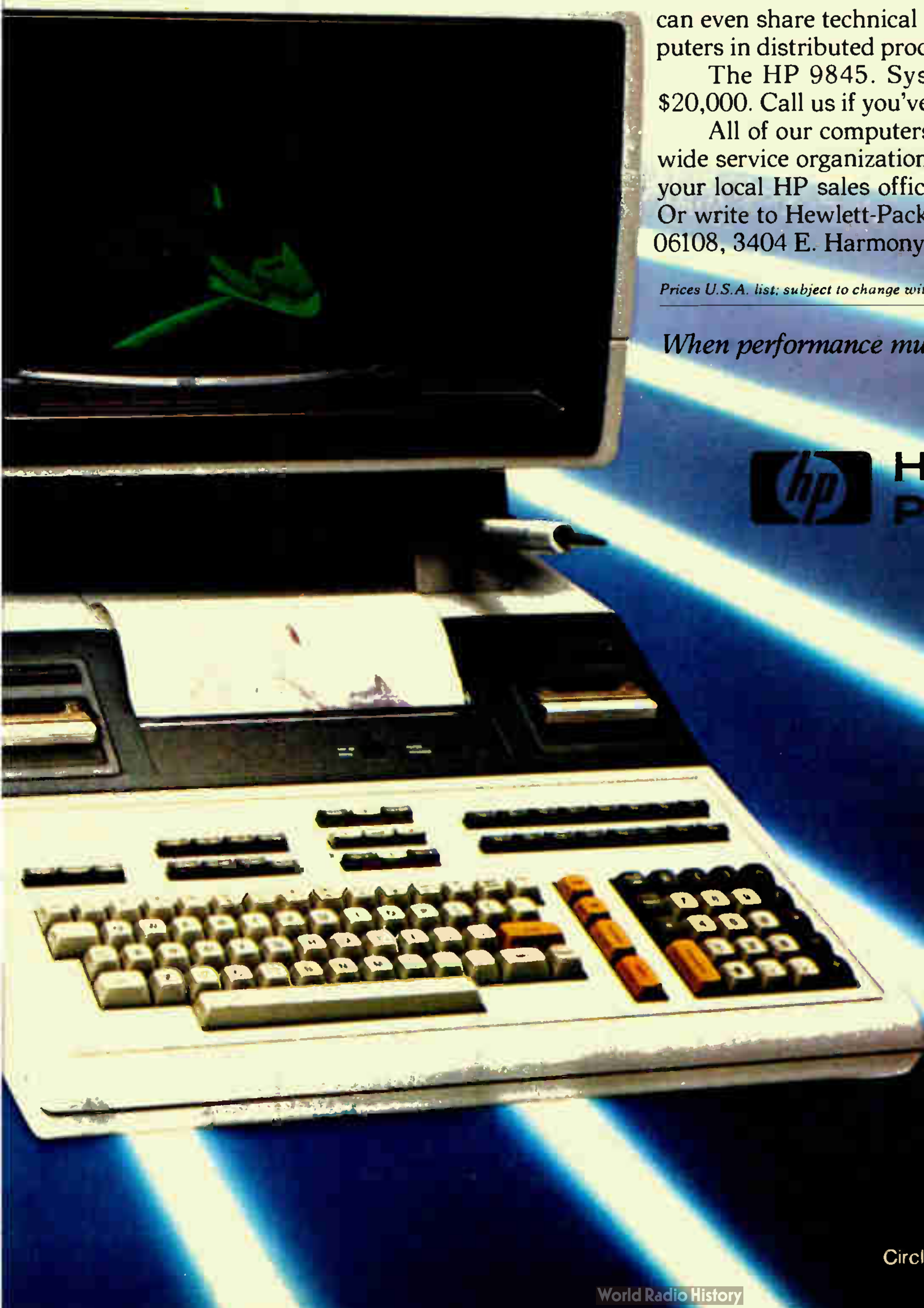

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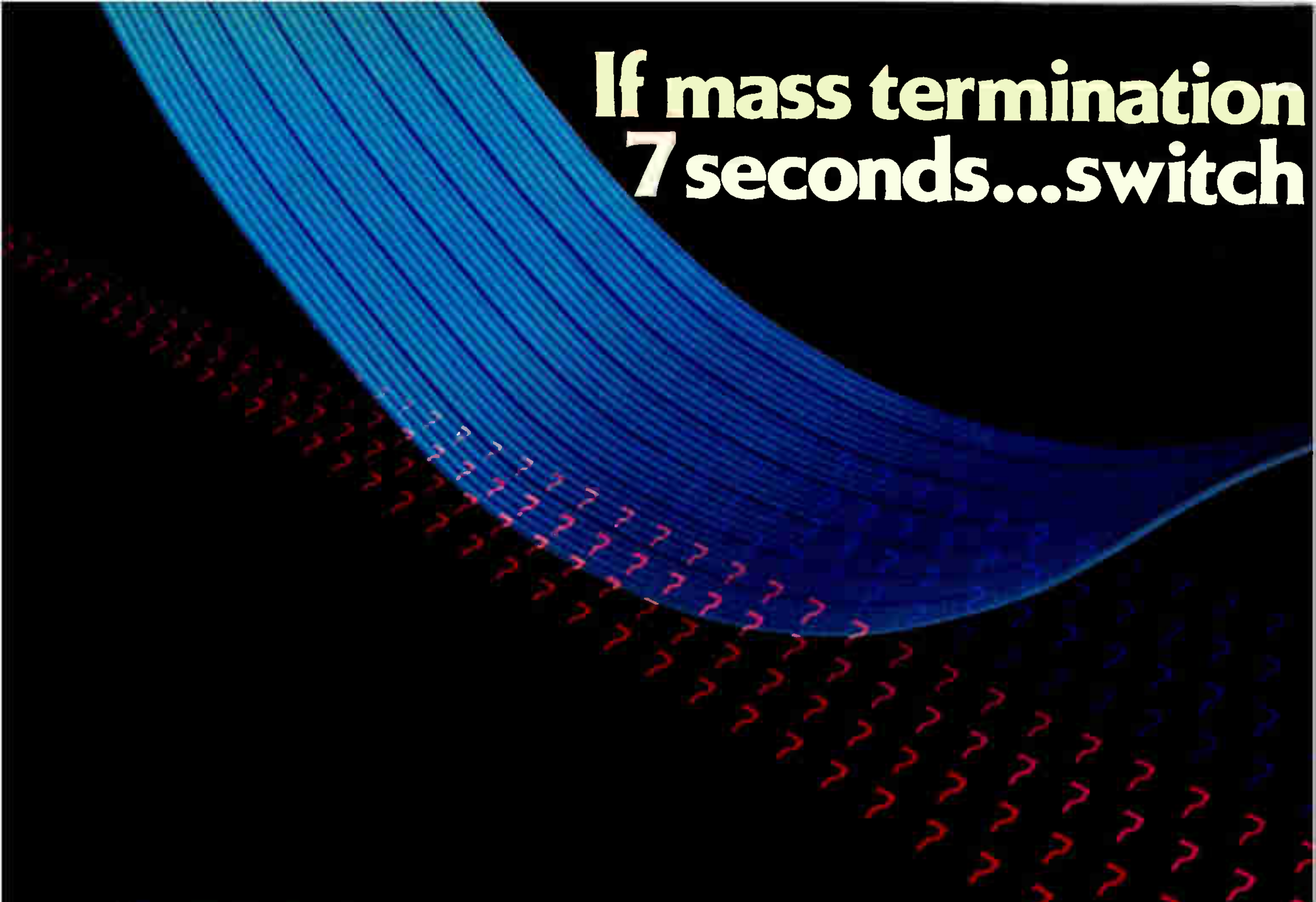

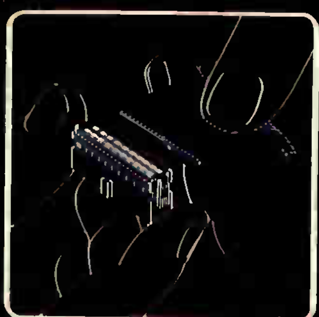

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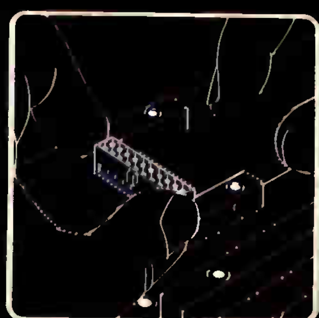

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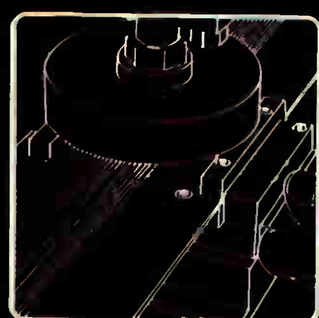

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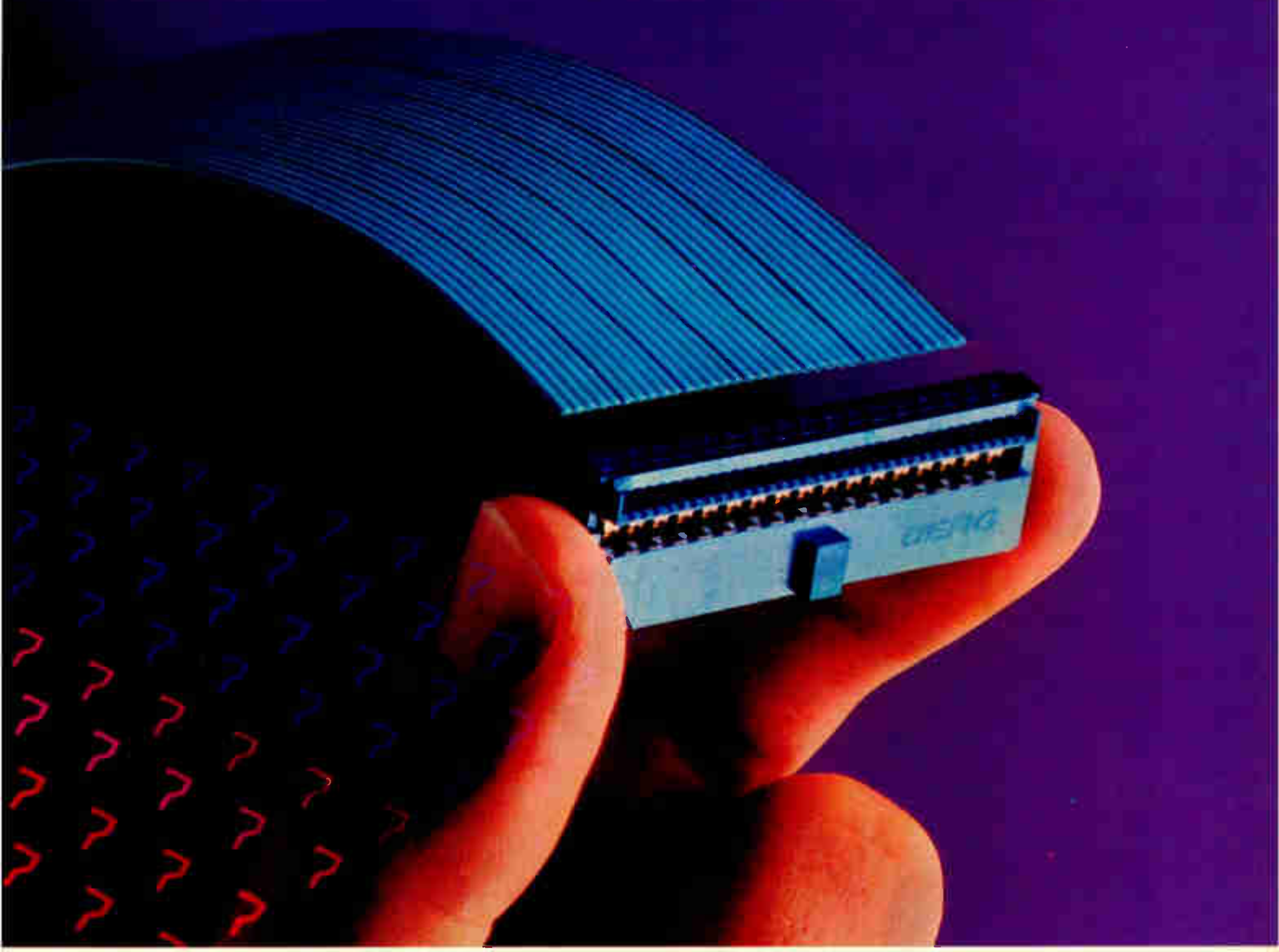

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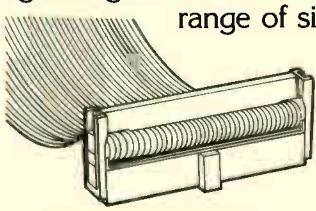

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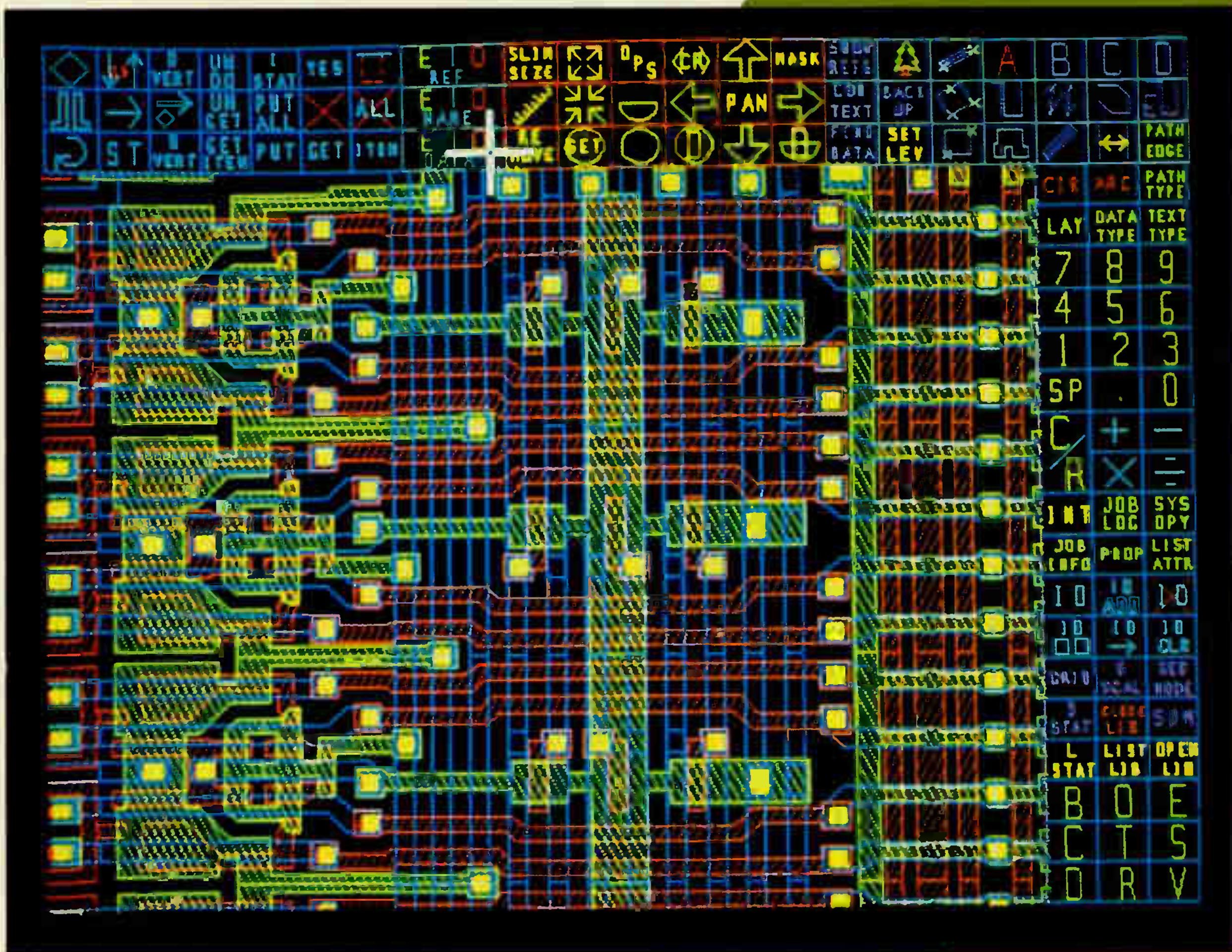

Computer-aided design. The CAD display helps the IC designer lay out a chip by providing a grid to help with spacing, plus various colors to depict different mask levels. Tools like this one from Calma Co. can speed along designs, as well as make the resulting mask more likely to be correct.

Activity principally in three areas holds out hope for a solution to the software crisis: high-level languages, operating systems, application software all advance

by R. Colin Johnson, *Microsystems & Software Editor*

☐ The much-publicized software crisis is far from over, but the past year saw a number of important steps taken towards a resolution: advances abound in high-level languages, operating systems, and applications software. The looming shortage of qualified programmers that has already caused a software-production crunch led to a number of innovative solutions that will help to keep that bubbling crisis from boiling over. One tactic to take is to settle on a single high-level multipurpose language for computer operators to use, and that is the thrust behind Ada, the high-level modular language sponsored by the U. S. Department of Defense. Interest in Ada is growing, but there are some reservations about its usefulness—and some competition, notably from Pascal variants.

Another attack on the software crisis comes from the originators of operating systems. They are pushing development of software interfaces with widely used high-level languages. Also, competition to become a *de facto* standard in the 16-bit arena is strong, with the CP/M family holding onto its 8-bit lead but with a strong competition coming from Unix and its variants for the 16-bit title.

Since the spread of computers is limited by the speed with which application software can be written, much work is going into developing strategies that stretch programmers' skills. A prime example is automatic program generators, not quite as hands-off as the name suggests, but still an important step towards computerized programming. Another tactic is the move by original-equipment manufacturers to encourage—sometimes commission—third-party software houses to write application programs.

High-level languages expand

The biggest software news this year surrounds the DOD's aggressive presentation of Ada—the language it wants to replace all other languages. Ada includes all the features of a modern structured language—like Pascal which is almost a proper subset of Ada—plus facilities for real-time control of multitasking environments, as well as a very high degree of modularity.

DOD is making a play to force those who have Government contracts to bring up an Ada capability. It can do this by requiring all bidders on Government software contracts to have an Ada capability in place.

Western Digital Corp., Newport Beach, Calif., has hired Bob Carlson, the former DOD Ada project leader, to lead its effort to write a proprietary Ada compiler. However, the first commercial compiler for a subset of the language has just been released by TeleSoft Inc. of San Diego, the recent merger between Telesoftware Inc.—brainchild of Kenneth L. Bowles, of UCSD Pascal fame (see "Software standards have Bowles' backing," p. 199)—and Renaissance Systems Corp. The compiler runs on a single-board 68000-based computer built by Renaissance.

Ada, however, has critics. Niklaus Wirth, author of Pascal, says that his new language, Modula-2, is better. It cures the deficiencies of the International Standards Organization's standard Pascal by providing modularity and separate compilation of modules, without introducing the "unnecessary complexities" of Ada, he says.

That seems to be the primary criticism of Ada—it is so complex that it approaches PL/1 in difficulty of implementation. What's more, it is said to require extremely skilled programmers, who are in short supply.

Despite its critics, however, Ada is here to stay, and many more implementations will appear next year. Implementations, albeit subsets, for all the popular 16-bit microprocessors are virtually assured to appear.

One of the more highly integrated competing language systems, the UCSD P-system from SofTech Microsystems of San Diego, Calif., incorporates its operating system. In this way, it is similar to Forth, marketed by Forth Inc. of Hermosa Beach, Calif. However, UCSD Pascal is a general-purpose data-processing language, whereas Forth is optimized for high-speed real-time processing and is ordinarily custom-tailored to each OEM's hardware. It is therefore similar to Microconcurrent Pascal from Enertek Inc. of Lansdale, Pa., which is also designed for real-time multitasking environments and is usually compiled on a mainframe, producing object code for a target microprocessor.

At the other end of the spectrum from complete language systems that include an operating system, program-development tools, a compiler, and so on are specialty languages designed to meet a specific need. One of the newest of these is Mainsail from a start-up company, Xidak Inc. of Palo Alto, Calif. Its primary design objective was easy portability to new computers while maintaining true source-level compatibility—exactly the same programs run on all implementations with exactly the same results.

So far, the biggest user of Mainsail is Intel Corp. for its computer-aided-design effort. The Santa Clara, Calif., firm aims to protect its tremendous CAD software investment over the long haul by using a language that can be transferred to future-generation processors with a

Silicon software soars

Software must be very reliable before it becomes economical to burn it into silicon, especially if less costly but nonerasable read-only memories are used. That is why, up till now, only proven high-level languages (like Basic interpreters) small operating systems (like those on personal computers) and short assembly-language programs (like those used for controllers) have been committed to silicon implementations.

However, an increasing number of problems are becoming well enough understood that standard solutions can be offered in the form of a group of self-contained subroutines enclosed in the same chip. An example is floating-point arithmetic subroutines based on the recently determined Institute of Electrical and Electronics Engineers format. Motorola, for instance, is now offering a ROM that contains the subroutines necessary to do IEEE-compatible floating-point arithmetic with the 68000, merely by calling the subroutines contained on the chip.

There are even more interesting examples of silicon software emerging. They offer functions in subroutines that can be used by the application programmer to speed along program development. The first of these to appear address the problem of real-time control when multiple processes must run concurrently while communicating with each other. Up till now, the application programmer had to write the code that does the interprocess communication, as well as the process control routines themselves.

It is just such functions that are realized by Intel's 80130 companion to the 8086 and by Hunter and Ready's VRTZ for the Z8000. Others are sure to follow next year, and not just for real-time process control either.

Many other functions will appear in silicon, too. In fact, Texas Instruments has big plans to offer a standard line of what it calls software components. They will be 99000 and 7000 microprocessors programmed to perform standard functions for the application programmer, thereby multiplying his or her productivity. Also customers willing to commit themselves to large orders will be able to put custom programs into these parts that TI will be offering as standard units.

minimum of hassle. It now has Mainsail running on its DEC-10s and VAX-11/780s and will soon have IBM 3033 capability as well. By rewriting the portion of its CAD tools that were in Simula, the steps required to produce a working chip dropped from six to two, Intel says. More such languages are sure to appear, now that software science is recognizing the need to free the programmer pool from constant maintenance of existing software as it is transferred to newer architectures.

Several other new languages are designed for the man in the street to use. The most extensive of these is the newest release of Smalltalk from the Xerox Research Center in Palo Alto, Calif. Originally designed for use by children, it allows a programming problem to be specified in everyday terms.

Symbolics Inc. has extended that concept by incorporating its extensive graphics capability into Flavors, a front-end language similar to Smalltalk, that is resident on the Cambridge, Mass., company's all-Lisp minicomputer. Flavors provides a multiple overlapping window system in which objects can be defined and manipulated right on a cathode-ray-tube display.

AUTOMATIC PROGRAM GENERATORS

Name	Company	Output language
Configurable Business System	Lifeboat Associates	none: self-contained
Cobol Program Generator	David R. Black and Associates Inc.	Cobol
Force	Point-4 Corp.	Basic
Genasys	Genasys International	Cobol
Jaspol	Japan System Science Co.	Cobol
No-Code	General Automation Inc.	none: self-contained
Pearl	CPU	Basic
Prism	Micro Applications Group	none: self-contained
The Last One	D.J. Systems Ltd.	Basic
The Master Programmer	The Master Programmer	Cobol

Lisp, traditionally for investigators of artificial intelligence, is showing great promise as an excellent language with which to develop symbolic CAD tools. Its whole structure is designed for symbolic representations that simulate human thought processes making it useful in developing programs designed to interface with the machines' operators easily.

Texas Instruments Inc.'s new language for its home computer, called Logo, is another example of such a language. Originally developed at the Massachusetts Institute of Technology, Logo makes the task of specifying the problem to be solved one that even the novice can perform with little trouble.

Much research into the human interface is being done by the software departments of computer and microprocessor makers, though few are willing to talk freely about it for fear of losing the competitive edge in such an important area. The fruits of that research will be trickling into the open market for years to come.

While the real crisis is with application software, that problem could be significantly reduced if programs were transportable between machines so that they do not have to be rewritten. One way to do that is to write them in a portable language like Mainsail. But programs in standard languages—Fortran, Basic, Cobol, and so on—can be run on different computer systems, too, if the time is taken to properly interface them with a standard operating system like CP/M-80 or Unix.

Microsoft Inc., for example, has successfully rewritten its high-level languages—Basic, Cobol, Fortran, and Pascal—for the IBM Personal Computer's operating system, which it developed under contract to the computer giant. Thus, the wealth of 8-bit 8080 software written in these languages can be run on 8088-based systems (like the Personal Computer) that have been interfaced to Microsoft's MS-DOS.

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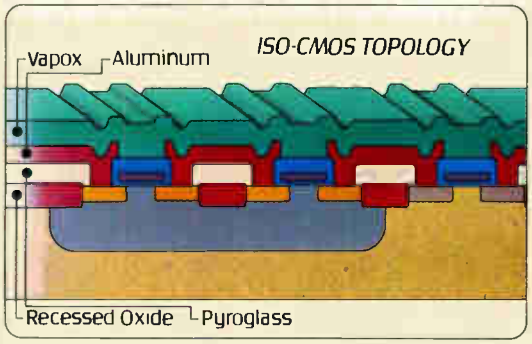

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Shown here is a section of the MT8865 DTMF Filter, magnified 1,300 times.

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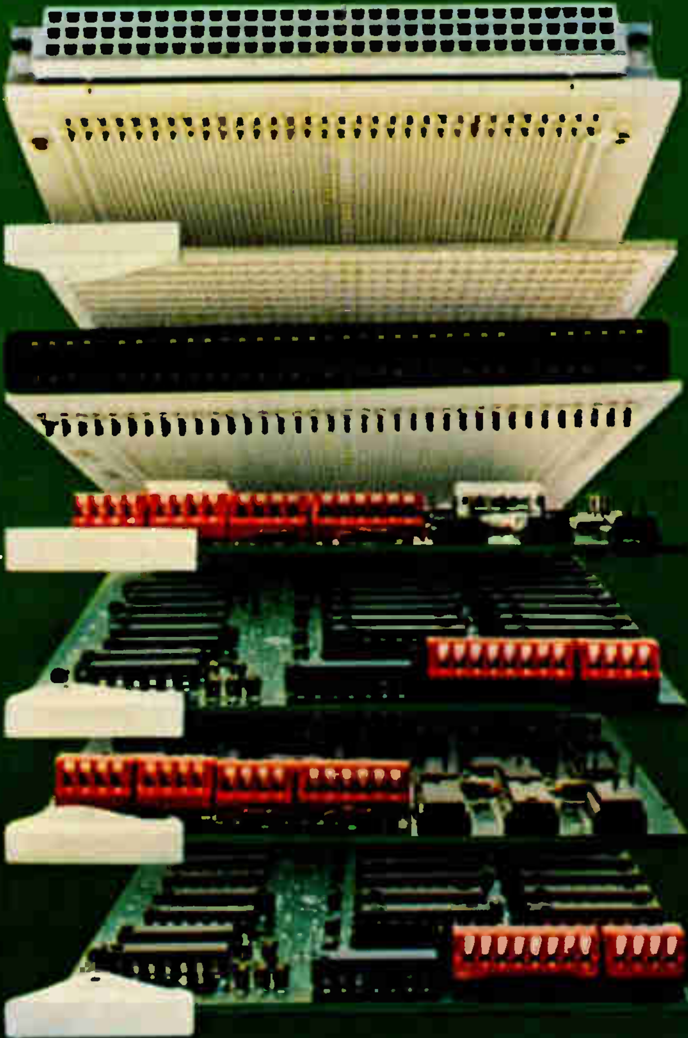

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that will run the same programs. It now plans four such operating systems, with MS-DOS at the bottom and full-blown Xenix—a licensed version of Bell Laboratories' Unix—at the top.

The originator of the CP/M-80 operating system, Digital Research Inc. of Monterey, Calif., now also supports the standard PL/1 subset G language. The company also introduced several new operating systems that will accept code written under CP/M-80. Those are MP/M-80—a multiuser version—and CP/NET-80—for local network environments. It has also developed versions of CP/M and MP/M for the 8086, though of course code written under CP/M-80 cannot be run under CP/M-86.

To meet the need for new high-level languages that run under CP/M-86, Digital Research just purchased Compiler Systems Inc. of Sierra Madre, Calif., the originator of the popular business language C-Basic, and there is talk of further acquisitions now that it has the support of venture capitalists. Other adaptations of high-level languages to CP/M-86 include MT Microsystem's Cobol and Micro Focus's CIS Cobol. Also, Microsoft has adapted its Basic and Pascal to CP/M-86, but it has no plans to support any of its other languages with this operating system now that it has its own MS-DOS.

Next year will be marked by strong competition between systems competing for that coveted position of becoming *de facto* standards for 16-bit microsystems.

An important advantage for Unix is that professional programmers prefer the extensive program development tools it offers. For example, Zilog Inc. has adopted Unix, renaming it Zeus, for its Z8000-based system-level computers, the Z-Lab microprocessor development system, and the System-8000 for business applications. Such adoption comes about because of Western Electric's liberalization of its licensing policies. There is also a clutch of look-alikes that have appeared this year to supplement existing offerings by Whitesmiths Ltd. and Mark Williams Corp.

Also, there is the Oasis operating system from Phase One Systems Inc. of Oakland, Calif., that is not a Unix look-alike but does incorporate many of its convenience features and is being adapted to an increasing number of microsystems. More Oasis implementations will appear next year.

Solving the applications crisis

One of the most revolutionary solutions to the software crisis is what are called automatic program generators. These front-end programs allow the user to specify the kind of program he wants, and the actual code is generated automatically (see table on p. 194).

Another increasingly popular approach to the software crisis is use of third-party software houses to supply programs, rather than for OEMs to develop them in house. This approach can significantly reduce the time to market for a software-based product and offloads the responsibility for future software support as well.

IBM Corp., the king of software for mainframes, recently shocked the marketplace by opting not to develop a single program for its new Personal Computer and also has started its own publishing operation.

Software standards have Bowles' backing

Kenneth L. Bowles feels strongly about standards, a somewhat surprising stance for someone involved in programming languages, which have fewer standards than other electronics industries. That deficiency is the center of his change in interest from the UCSD Pascal language he developed to Ada, the Department of Defense effort promoted as the first standardized language.

What led Bowles to Ada was his popularity as a speaker detailing the pluses of UCSD Pascal, which he and a graduate student at the University of California at San Diego developed in 1974. He was preparing for a talk on Pascal in late 1979 when he first looked seriously at Ada. Although his first thought was that he would have done some things differently, he felt "great admiration for what they had done." When he decided to leave UCSD to form Telesoftware in 1980, he chose Ada as the heart of the new company's efforts.

Pascal was not one of the possibilities, because of problems with its many extensions. "I didn't consider Pascal because it would have meant pouring good effort after bad. Pascal is fatally flawed because of the lack of standards," he says matter-of-factly.

One of the features he likes most about Ada is that standardization provides the ability to create programs for various functions and store them in a library. Thus programmers can use and raise them, instead of rewriting mundane subprograms. TeleSoft, formed earlier this year when Telesoftware merged with hardware maker Renaissance Systems Inc., plans to offer such a library.

Bowles did not start out in software—his Ph.D. from Cornell University is in radio and radar studies, and he spent 10 years with the National Bureau of Standards as an atmospheric physicist. The amount of computing involved prepared him to take over UCSD's computing center in 1968, three years after he began teaching there. That job proved to be the starting point for his Pascal project, which began in 1974.

Bowles sees Ada's popularity growing as programmers gain experience with it. "I think that with serious software engineers, once there are accessible Ada implementations, we'll find an accelerating trend of people who have taken the plunge with Pascal jumping to Ada because they meet so many *culs-de-sac* with Pascal," he predicts.

He does have some fears that the standardization of Ada may not come to pass. "It may have fallen victim to [Reagan's] budget-cutting ax," he says. As it stands, the DOD Ada office is staffed "by two junior people and a part-timer," markedly affecting its effectiveness, he says.

On the positive side, he thinks the industry feels strongly enough about a software standard to carry on if the Government fails. "We'll enthusiastically join with other people to see that it becomes successsful," promises the soft-spoken Bowles. **-Terry Costlow**


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COMPUTERS & PERIPHERALS

Easy landing. A clear daylight approach from 5 miles out on this Rediffusion simulator shows the high degree of realism that today's computer techniques provide for pilot training.

With an eye to office automation, manufacturers improve hardware and software in smaller machines and terminals; mainframes and minicomputers also gain ground

by Tom Manuel, *Computers & Peripherals Editor*

☐ Always a fertile field for new technological developments, computers and their peripherals were especially active this past year. The spur is the impending flowering of a whole new market, as businesses of all sizes turn to office automation to solve problems of information flow and control. Distributed processing, which has been growing by leaps and bounds, got a big boost this year with the introduction of a new systems concept. It took the form of new offerings, which provide powerful computers as individual work stations linked in local networks.

In addition to these desktop minicomputer work stations, other new terminals, intelligent and dumb, have emerged. With so many more people using computer terminals these days and using them for a major part of their working day, the science of ergonomics is being employed heavily in new designs—a trend that will continue to grow.

The proliferation of small computers and work stations has spurred the need for ever-larger quantities of local data storage and has increased demands for ways to back up this data or remove it for storage. The industry has responded with several new technologies applied to products such as high-density floppy disks, floppy and tape cartridges, and even Winchester-technology disk cartridges—and for the future, optical disks.

Aiming at the office

This was a banner year for the personal computer, as well as for office automation. It could be said that the personal computer grew up, or at least became mature enough to be noticed by the big boys. Several of the major U. S. computer companies introduced personal machines, as did several Japanese companies. Personal computers, minicomputer work stations, local networks, and advanced software greatly enhanced the options available for automating many office functions.

Advancing technology has not forgotten the large mainframe computers and minicomputers. Many new large mainframes were announced this year, pushing the top systems to ever higher speeds and power. The 32-bit superminicomputer area also has been humming with activity in the past year.

The operator of a computer terminal is likely to say, "That's my computer," regardless of how much processing power actually resides in it. This is becoming truer than ever as terminals gain more intelligence. In the past year, a handful of companies reinforced the concept of "my computer," by incorporating distributed processing through application of the newest technologies in 16-bit microprocessors, semiconductor memories, local networks, multitasking distributed operating systems, and bit-map displays and other graphics techniques.

Convergent Technologies, Santa Clara, Calif., introduced such a work station based on the Intel 8086, a distributed multitasking operating system, a local net, and an advanced display driver. Apollo Computer Inc., Chelmsford, Mass., and Three Rivers Computer Corp., Pittsburgh, announced similar machines.

The Apollo Domain dual-bus system is based on the Motorola 16-bit MC68000 processor, has a bit-mapped display, and works in a ring network. It also has a processor-independent virtual-memory operating system in which all the memory on the network can be in one global address space.

The 16-bit system from Three Rivers, called PERQ, is similar to the Convergent and Apollo systems and uses Ethernet for its high-speed local network. These systems provide good building blocks for future integrated systems to automate the office.

The office-automation heavyweight, Xerox Corp.'s Office Products division in Dallas, introduced its Star work station with an advanced operating system, sophisticated graphics using a cursor-positioning mouse, and an Ethernet interface that attracted a lot of attention at computer shows this year, such as the National Computer Conference in Chicago and Syntopican in Atlanta. Also, Datapoint Corp. of San Antonio, Texas, developer of a pioneer local net for distributed data processing, moved its four-year-old ARC (for Attached Resource Computing) into office automation by introducing a host of new products. (See "For the office, Schmidt favors simplicity," p. 210).

Other new computers that have many characteristics of these capable work stations include:

- The CTS-300, using the 68000 on a Multibus, from Codata Systems Corp., Sunnyvale, Calif.
- The TS-800 line from TeleVideo Systems Inc., also in Sunnyvale.
- The Advantage computer with bit-mapped graphics from North Star Computers Inc., San Leandro, Calif.
- The TFC 8500 from TRW-Fujitsu Co. of Los Angeles.
- The Mariner computer from Micromation Inc. of San Francisco.
- The DRS 20 with the Microlan local net from Great Britain's ICL Ltd.

Meanwhile, Tandy Corp., the Fort Worth, Texas, leader in personal computers, jumped into this market by offering a local network for its popular TRS-80 Model II computer system. Arcnet uses the Datapoint ARC technology, which makes it possible for Tandy and Datapoint products to share the same net and to work together.

The fast processors driving the graphically oriented multiwindow displays, coupled with the ergonomically designed packaging, are aimed at making it easier for users to do more work with less fatigue. This is but one example of the surging wave of interest in ergonomics in computer systems design. The countries of the European Economic Community have set some stringent standards for ergonomic design—such requirements as low-profile keyboards that can be detached from the displays and easy-to-use brightness controls on tilting and swiveling cathode-ray-tube displays.

Make it easy for me

Software that makes application operations easy to learn and understand and is efficient to operate as well is also receiving much attention. So it can be said that ergonomics is being applied to both the hardware and the programs that run on it.

Besides the new ergonomics, there is a strong trend for all terminals, from the dumb to the superintelligent to increase in quality and reliability, while greatly decreasing in cost. With the prospect of so many terminals to be in use—as ubiquitous as the telephone, at least around offices—this move is sure to strengthen.

One exciting new terminal exemplary of this trend was the Viewpoint from Applied Digital Data Systems Inc. of Hauppauge, N. Y. This little terminal's high reliability (mean time between failures of 23,000 hours), low price ($650), and ergonomic design have made it exceedingly popular. It and others like it from such companies as Lear Seigler, Hazeltine, and TeleVideo Systems gain their quality, reliability, and low cost from simple design, careful and well-planned manufacturing, stringent quality testing, and microprocessor control.

To good terminal designs, processors can be added at little additional cost to produce more capable work stations—the only catch being that software for the extra processor may cost several orders of magnitude more than the added chips. The opposite approach can be taken, too—the processor and memory can be left out of a good work-station design to produce a good terminal (the course Datapoint took recently with the model 8600 processor and the 8220 terminal). However, no matter how an intelligent work station comes into being, there is likely to be a need for mass storage and some way to back it up for greater data security.

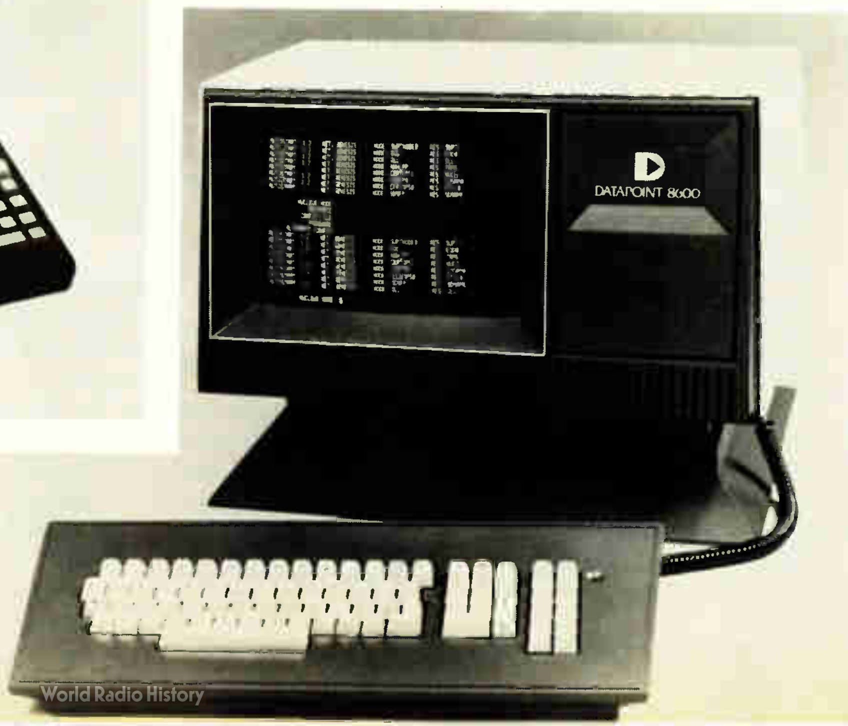
Pack it in

Storing more data on ever smaller media has been a driving force in computer technology since the birth of Eniac. The industry has pushed on from huge magnetic drums rivaling small vans in size and weight to the smallest floppy-disk drive now available, the microfloppy from Sony Corp., which easily fits into one hand, uses a floppy cartridge that slips into a shirt pocket, and holds more data than many early drums.

What was new this past year were several methods of packing more data on removable media of several configurations—floppy cartridges, magnetic-tape cartridges, and even Winchester-technology cartridges. Still in the laboratories at several major companies is data storage on optically encoded disks, similar to video disks.

Among the new floppy-disk cartridges and drives is the 8-inch Alpha 10 from Iomega Corp. in Ogden, Utah. It packs 300 tracks per inch and 24,000 bits/in. to store 10 megabytes per cartridge. Amlyn Corp., San Jose, Calif., offers a five-pack—five 5.25-in. floppy disks in a cartridge that stores 8 megabytes and a drive that picks the floppies one at a time from the cartridge.

In Sunnyvale, Calif., Pragma Data Systems Inc.



Designed for people. These two products, the Datapoint 8600 processor and the ADDS Viewpoint terminal, are designed with ergonomic features like low-profile detachable keyboards and tilting, swiveling screens.

squeezes 80 megabytes on the industry's first ½-in. magnetic-tape cartridge in a product called the model 2000. Using standard 8-in. diskettes, PerSci Inc. of West Los Angeles, offers a new drive employing a track-following embedded head-positioning servomechanism—a hard-disk technology, but new to floppies. It increases track density to 150 tracks/in., raising the capacity of an 8-in. double-sided floppy to 4.2 megabytes, which is better than 2½ times more than the conventional double-sided 8-in. floppy drive offers.

In Winchester technology, New World Computer Co., Costa Mesa, Calif., has developed a removable 5.25-in. cartridge with a low-mass multiple-head assembly (8 or 16 heads; 1 or 2 sides; 2 or 4 megabytes) for fast access. Seagate Technology, Scott's Valley, Calif., is busy developing a 5.25-in. Winchester cartridge drive, and DMA Systems Corp. of Santa Barbara, Calif., introduced the Micro-magnum 5/5 Winchester cartridge drive with 5 megabytes of fixed storage and 5 megabytes of removable. Seagate and DMA Systems along with magnetic-disk maker Dysan Corp. of San Jose, Calif., are joined in an effort they call the 5.25-in. removable cartridge club to promote a physical standard.

More developments in compact, high-density, removable storage media are likely. The demand is rising for ever larger amounts of storage and the means to back it up for small-business systems, work stations, and the cornucopia of new personal computers.

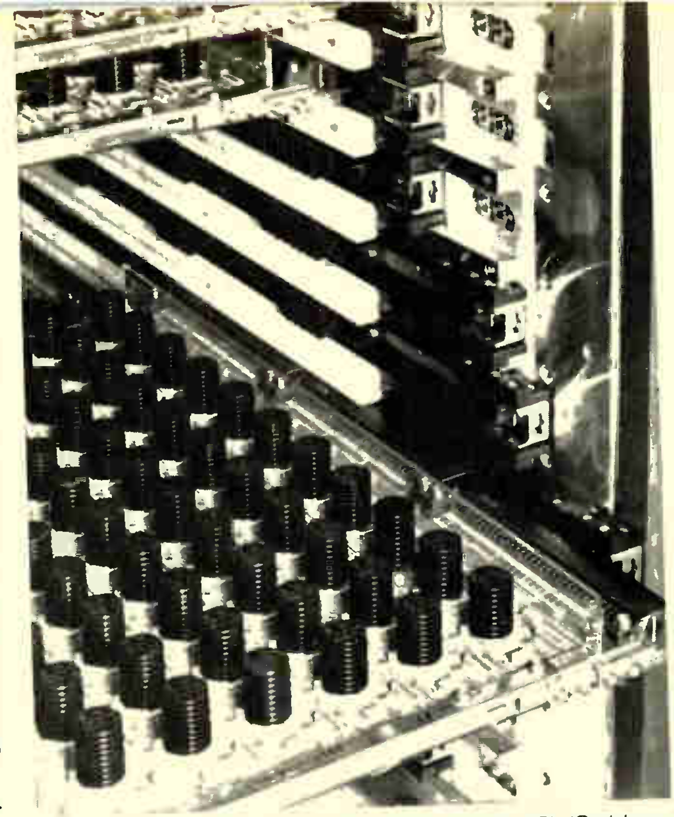
Personal computers

This was the year that personal computers came of age. These handy little machines with a lot of capability, which got their start in life as a hobby, were popularized by companies such as Tandy Corp., Apple Computer, Commodore, and others as useful tools for the home and office. They got a further boost this year as large companies introduced their versions, such as Xerox's 820 and IBM's Personal Computer.

An abundance of similar products flooded the market around the world, some of them updates from the present industry leaders. A partial listing includes: Apple III, Datapoint 1550, Commodore VIC 20 color computer, Data General Enterprise 1000, DECmate Work Processor 278, Fujitsu Micro 8, Hewlett-Packard HP 125 and HP 9826A, Hitachi MB-6890, Nippon Electric Co.'s PC-6000, PC-8000, and PC-8800, Northern Telecom 503, Osborne Computer Co.'s Osborne 1, Philips Austria P200, Sharp Corp. MZ-80B, Tandy Radio Shack TRS-80 Model III and Color Computer, TRW-Fujitsu 3450, and Zenith Data Systems Z-89.

All of them are different—which is the delight of a competitive market—yet all share some common attributes. They are based on 8- or 16-bit microprocessors from relatively few manufacturers; start with 48-, 64-, or 128-K bytes of memory; usually have some form of mass storage, typically floppy disks; and incorporate a CRT display (except for the two color computers, which hook up to a standard TV receiver). They cost $300 to $10,000, with most of them starting at around $3,000.

Both the home and the office are market targets, but the majority of the software offered and being developed is for business use—Space Invaders not withstanding.



Towers of power. The Fujitsu RAM chips and the ECL ICs (shown with the black cooling towers) are used in its top-of-the-line mainframe computers M-380 and M-382 and in Amdahl's 580 series. Multiple chip-carriers are packed into a cube 50 cm on a side.

Some of the computers will be used standing alone, but an increasing number will be interfaced with local nets and public-data networks, where as intelligent work stations they can perform such functions as electronic mail and information retrieval.

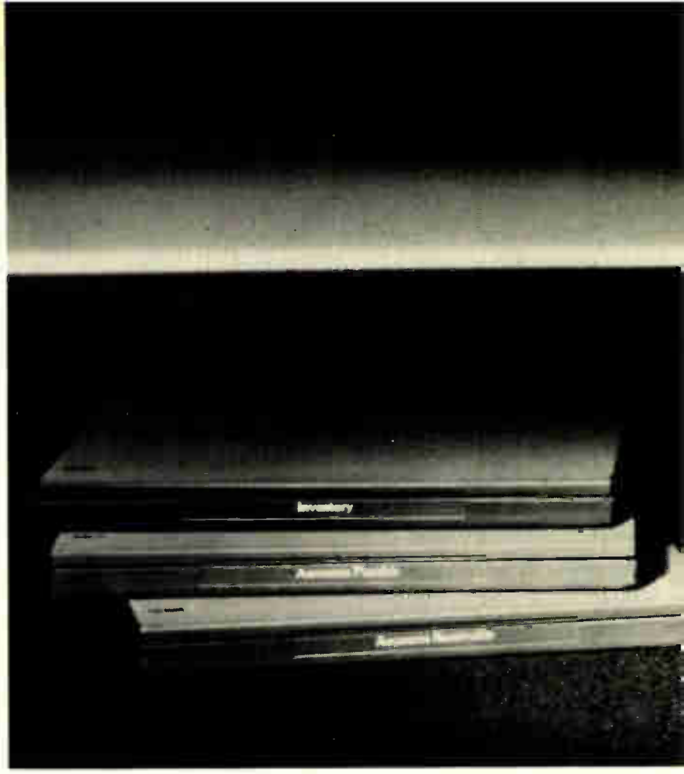
Built-in or plug-in interfaces to local nets—like Tandy's new Arcnet interface—will soon be one of the features of personal computers. As soon as there is an accepted standard local network or a few recognized *de facto* standards, these interfaces will surface.

However, the local-net interface is but one communications option for personal computers. They could use built-in telephone and modems for easy connection to public networks or the new computerized private branch exchanges that carry and switch data as well as voice. Personal computers and terminals that are also telephones or that interface with local nets will play an important role in the future of office automation.

Increase productivity—automate the office

Though the use of computers is expanding in the traditional areas of data and transaction processing, industrial automation, computer-aided design, and the military, the fastest growth in the use of computers is in the office. Computers will be increasingly used for automating much more than typing and secretarial functions. The opportunity to increase productivity by automating the office is great.

Nearly every significant development this year—the high-powered work stations with local nets, the low-cost, ergonomically designed terminals, innovative removable storage devices, and personal computers—are technologies that are being applied to automate more office



Little package, big data. The 8-in. floppy-disk cartridge that slips into this Alpha 10 drive from Iomega holds 10 megabytes of data. New technology where the flying media and aerodynamic read head are closely coupled but not in contact makes this density possible.

functions. What is more, computer graphics being applied to business functions is rapidly becoming another new tool for office automation.

Other new products introduced this year—too many to list individually—were computerized voice-messaging systems, electronic-mail and data-retrieval software, terminals with built-in telephones, and new word-processing systems. There even were a couple of complete product lines for office automation, the OFIS 1 from Burroughs Corp., Detroit, and the DPS-6 from Honeywell Information Systems, Minneapolis.

With all the activity in office automation, personal computers, and the like, bigger and faster mainframes still are needed. The demand must be there, because the companies serving the top end of the IBM-compatible mainframe segment were very active.

IBM Corp., Armonk, N. Y., unveiled the first computer in its H series, the 3081 dual-processor system capable of processing about 10 million instructions per second. For the 3081, IBM uses higher-density logic-array and memory integrated circuits. It packs up to 118 of these chips onto a new 33-layer, 90-millimeter-square chip-carrier sealed in a helium-filled module and cooled by chilled water. Four newly developed multilayer circuit boards containing circuit modules that house about 750,000 ICs make up the 3081's central processing unit.

Higher-density logic arrays and memories in specially developed denser packaging were also used for faster processors by several of IBM's competitors to leapfrog the 3081 in announcements of machines offering performances from 1.15 to 4.5 times greater. Amdahl Corp., Sunnyvale, Calif., unveiled its 580 series immediately following IBM's announcement. The single-processor 5860 will have a performance range 1.2 to 1.6 times the 3081's, and the dual-processor model 5880 should be 2 to almost 3 times faster.

Bigger Japanese mainframes

The Japanese trio in large mainframes—Hitachi, NEC, and Fujitsu—all jumped into the fray with bigger and faster systems than the 3081. Hitachi Ltd.'s M-280H will perform at about 15% better. The NEC Acos 1000 in its two-processor version has throughput performance of about 29 million instructions per second. The Acos line is not IBM-compatible, unlike the offerings from the other two Japanese companies.

Fujitsu Ltd., the No. 1 computer company in Japan—selling more yens' worth of computers there than any other company in each of the past two years—is spanning the globe with its newest computer technology. Its logic and memory ICs are used in its new M-380 and M-382 computers, in Amdahl computers in the U. S., and in the DIPS model 45 computer it makes for the Nippon Telegraph & Telephone Public Corp.

The M-380 and M-382 computers will be sold by Fujitsu in Japan, Australia, Brazil, and Spain, and by Siemens in West Germany. Fujitsu does not now sell its large computers in the U. S. because of an agreement with Amdahl, a major customer for its circuits and also a company in which it has invested heavily.

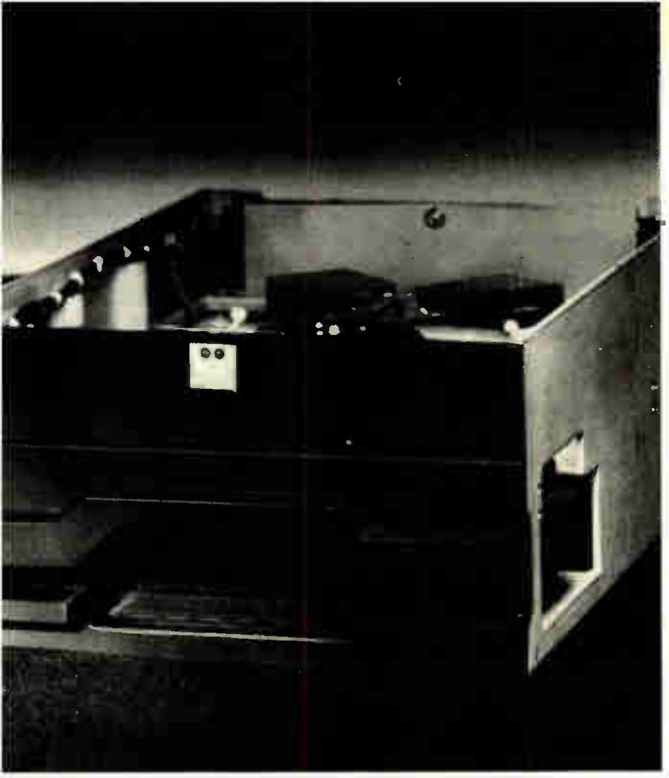
The technology that helps make the M-380 and M-382 so fast is emitter-coupled-logic large-scale integration with a 350-picosecond propagation delay time and 1,300 gates per chip, coupled with 64-K random-access memories. As many as 121 logic and RAM chips, each with its own air-cooling fin, are packaged on 14-layer multiple chip-carriers. These carriers are stacked into a cube 50 centimeters on a side, where connections are contained in two 12-layer printed-circuit boards that make up two side walls of the stack.

This dense packaging reduces the transfer time among logic and memory circuits. Fujitsu is claiming speeds of 15 and 30 million instructions per second for the M-380 and M-382, respectively.

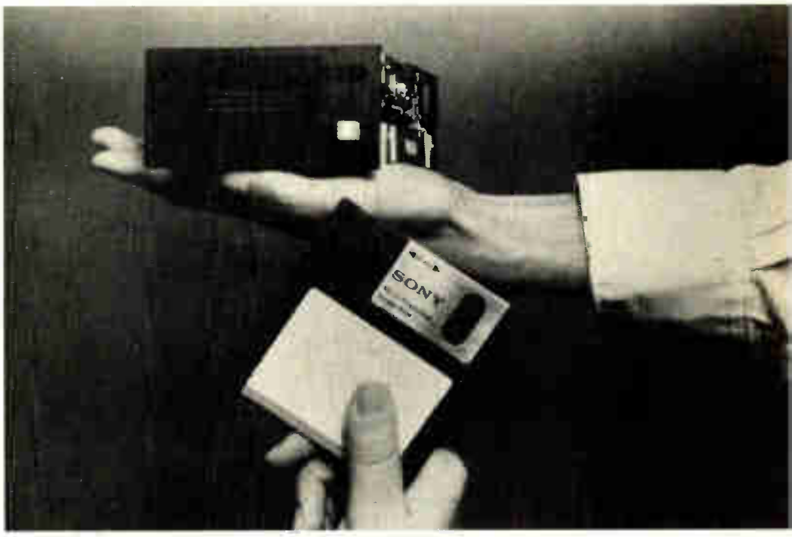
In the mid-range mainframes and the top-end systems that are not IBM-compatible, there was little action this year—there were quite a few new systems in 1980. Magnuson Computer Systems, ICL, Nixdorf AG, and IPL Systems Inc., all announced systems that will compete with IBM's 4300 Series.

Tandem Computers Inc. of Cupertino, Calif., introduced its second generation of fault-tolerant, networked, multiple-processor computer systems for transaction processing. The NonStop II system extends virtual-memory addressing to 1 billion bytes. It also contains a new operations and service processor to help reduce repair times. The NonStop systems can avoid downtime with redundancy, but while one of two parts is being repaired, the risk of downtime is greater; so the shorter repair times add another measure of safety.

There was a flurry of activity in new systems in the 32-bit superminicomputers. Some new systems pushed the performance upward, truly clouding the distinction between minicomputers and mainframes. Other newly announced machines pushed downward in performance,



Handful of kilobytes. The world's smallest disk drive, the 3.5-in. microfloppy drive and cartridge from Sony Corp., is capable of storing up to 437.5 kilobytes of data on one cartridge. The rigid plastic cartridges are small enough to slip into a shirt pocket.



reducing costs and improving the price-performance ratio to a point where they become competitive with the bigger 16-bit minicomputers.

Denser logic-array circuitry and 64-K memories helped improve these new superminis' performance as much as they did in the new top-end mainframes. Also, architectural changes such as more use of cache memory, larger caches, and more functions performed in parallel counted for their share of the improvement.

Among the highlights of the new announcements, Systems Engineering Laboratories of Fort Lauderdale, Fla., introduced its Concept 32/87, the most powerful superminicomputer yet announced. Based on emitter-coupled logic, using multiple buses and several processors for parallel operations, and boasting a 32-K-byte, 75-nanosecond cache memory with a control algorithm that may go as high as a 98% hit rate, the 32/87 can process 4 to 5 million instructions per second. It was not long ago that a machine that could hit a million instructions a second was considered a very fast mainframe.

At the other end of the supermini spectrum, Perkin-Elmer Corp.'s Computer Systems division, Oceanport, N. J., introduced its model 3210, the first superminicomputer to be priced under $50,000 for a complete system. Other companies in the 32-bit minicomputer market introduced new products as well.

Digital Equipment Corp., Maynard, Mass., unveiled the long-awaited VAX-11/750 to slip in under its popular VAX-11/780 and is expected to introduce another little brother, the VAX-11/730 soon. Data General Corp., Westboro, Mass., unveiled its new medium-sized 32-bit mini, the MV/6000, while its neighbor, Prime Computer Inc. of Natick, added a new top-of-the-line model 850. Harris Corp.'s Computer Systems division in Fort Lauderdale introduced its mid-range model 300 with a 24-bit processor and a 48-bit data path.

Two 32-bit machines from Japan joined the superminicomputer family. Toshiba Corp. announced its new enhanced 32-bit supermini line, the Tosbac series 7/70E, and NEC introduced its MS 70.

The new superminis are serving as hosts in computer-graphics systems, and 16-bit microprocessors are providing horsepower for higher-speed, more intelligent graphics terminals with more lines in the displays. The traditional applications in computer-aided design and simulation benefit from the 16-bit processors and the more affordable memory, enhancing machines to deliver more resolution, faster processing, and more dynamic displays containing more information.

This hardware technology, combined with graphics software techniques from computer-science research, is not just for the traditional computer-graphics applications anymore. It is increasingly in use for office-automation applications.

The rapidly growing number of computer users in the office are discovering that graphics, especially color graphics, can be an efficient way of communicating. Also, it turns out that graphics can improve the operator-machine interaction of office automation as well, as Xerox has shown with the control symbols graphically displayed in the Star work station.

Color, color, color

Color adds another dimension to business-graphics and CAD displays and to hard copy, and it is essential for realism in terrain simulation—a major use by airplane, helicopter, and tank pilot-training simulators. When the cost of color drops low enough, it will be preferred for most office and business use, particularly where graphics is involved. Some low-cost color displays are reaching the market now, and even some color printers and plotters are low enough in price to be feasible in some business applications.

A sampling of the new low-cost color graphics terminals with 13-in. screens includes the 3651 from Intelligent Systems Corp. for $3,000, the MVI-7 terminal at

$3,500 from Colorgraphic Communications Corp., the $3,000 model ITI 801 from Integrated Terminals Inc., and the Data General Dasher D280C for $3,750.

One of the most unusual uses of color graphics displays will be the full-color electronics cockpit. Using six screens, it is being built by Thomson-CSF of France for the new A310 Airbus from Airbus Industrie.

More graphics capability

Other interesting developments in computer graphics this year were the unveiling of the first truly three-dimensional display, SpaceGraph by Genisco Computers of Costa Mesa, Calif.—an attention grabber at the annual Siggraph show held in Dallas last August—and several high-powered terminals with enough memory and processing capability (from the built-in 16-bit microprocessors—most frequently the 68000) to take over from the host computers essentially all of the graphics processing. Among the new 16-bit microprocessor-powered terminals introduced in the past year were the CGC 7900 from Chromatics Inc., the model 8000 from the Lexidata Corp., the VC 33000 from Vector General Inc., and the PS 300 from Evans and Sutherland.

Other peripherals also showed solid technological advances. For example, at the small end of the fixed-disk-drive field there were several new 8- and 5.25-in. Winchester drives announced. Seagate Technology, introduced its ST512, the first small Winchester with thin-film heads. At the other end of the scale, Storage Technology Corp., Louisville, Colo., and Control Data Corp., Minneapolis, announced large-capacity 14-in. drives to compete with IBM's 3380.

Printers and optical character readers were not neglected either. Some highlights of the many 1981 developments are a 10,000-line-per-minute Japanese-language laser printer being developed jointly by Fujitsu and Toray of Japan and NTT's Aesop ideogram reader. Delphax Systems, Mississauga, Ont., Canada, introduced the first ion-projection high-speed page-printing engine for future printers and copiers. Also, from Great Britain's Image Data Ltd. came a data tablet capable of reading handwriting.

For the office, Schmidt favors simplicity

An international radio conversation is not the usual starting point for a successful career. But that was how Jonathan E. Schmidt happened to meet his future—when Datapoint Corp.'s executive vice president Victor D. Poor in 1969 persuaded the Michigan native to move to San Antonio, Texas, and develop computer products.

Schmidt describes the serendipitous meeting. In the early 1960s, he was working in South America. "One day I was talking to a guy from Florida on a ham radio who said he received a real nice signal with a beautiful Collins radio he had gotten from his friend Irv, in Ann Arbor, Michigan," recounts the University of Michigan graduate with bachelor and master of science degrees in mathematics. "I came back and said, 'Irv didn't have one of those radios.' (Irv had been my roommate, and I stored my radio in his attic.) 'Irv had no right to give it away.' Well, this guy said, 'You mean to tell me that I stick this pole up in the wilderness and the first guy I talk to lives in Ecuador and claims I'm using his radio?' This was Vic Poor," Schmidt says with a chuckle. The two became fast friends.

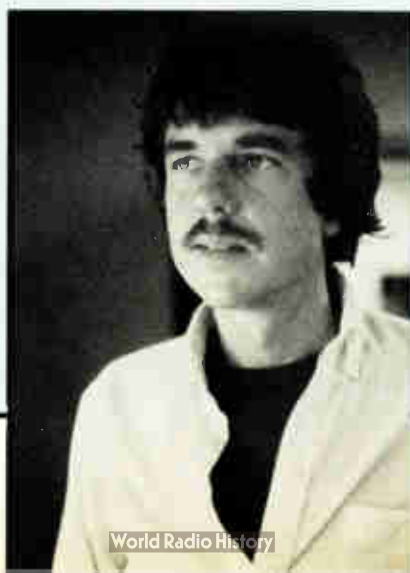
Working for Poor at Frederick Electronics in Frederick, Md., Schmidt designed electronic switching systems and radio gear. Poor soon went to Datapoint and in 1969 persuaded Schmidt he should follow. After the move, Schmidt worked on a number of the major computer projects that helped vault the firm into a leading position in the office systems business. His work includes the development of Datapoint's Attached Resource Computing—a baseband local network—and the Associative Index Method for content-addressable information retrieval.

"Coming through the back door" in computer development, as Schmidt puts it, and "reverence for the frailty of people" during the development of major software and hardware projects were among key factors for early success. "It was terror of the catastrophes that can befall software-development groups that kept us from the pitfalls," says Schmidt, who is now vice president of advanced product development at Datapoint. "It forced us into compatibility between all operating systems and hardware and keeping everything as simple as possible." Simplicity, in his view, is another key to success in introducing high technology to the office. "There is a feeling among people that progress means complexity, that the new things they are going to be forced to use are going to be powerful and therefore complex," he notes.

Schmidt, who turns 40 this month, predicts two major challenges for computer and peripherals designers: better memory management and displays that are easier to read. "There will have to be substantial improvement in the systems to figure out how to use all the memory that's going to become available for very little cost," he says.

Voice capabilities in office products may be one use for that memory: "Store-and-forward audio will be a technology that can eliminate written versions because a stored voice message could simply be waiting over at the other end," he suggests. But at the same time, a user must be able to see the list of calls to enable quick selection of those to be heard first. And to do this, people will most probably be looking at terminals equipped with cathode-ray tubes.

"The CRT's demise was predicted 10 years ago—even several years ago—there were sizable indications that by this year, liquid-crystal-panel displays were to have taken over," he says. "But people who write the demise of a technology seem to forget that the technology whose end they proclaim is also subject to advancement. The fad is to say the future is all new, completely different. But actually, the future is all evolution and in most cases not so different." **-Robert Lineback**



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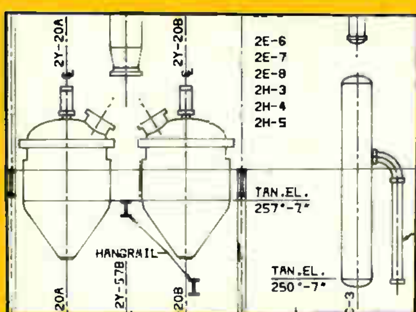

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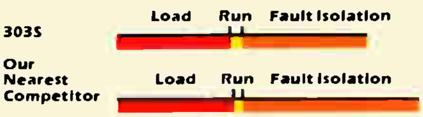
Total Time To Fault Isolation (TTFI)



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From shorts and opens to LSI devices, the new Fairchild 303S will give you test results faster, easier and more accurately than ever before.

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The 303S isn't just built for speed, it's built for versatility. It comes with the largest number of uncompromised hybrid test points (927) in the industry, so it can be used to test either analog or digital points. By simply adding another low-cost terminal, our Foreground/Background programming feature enables programming to be done without tying up the system. And our datalogging feature gives you hard copy documentation of faults—by shift, day, week, or any other time increment—to accurately pinpoint manufacturing problems as they occur.

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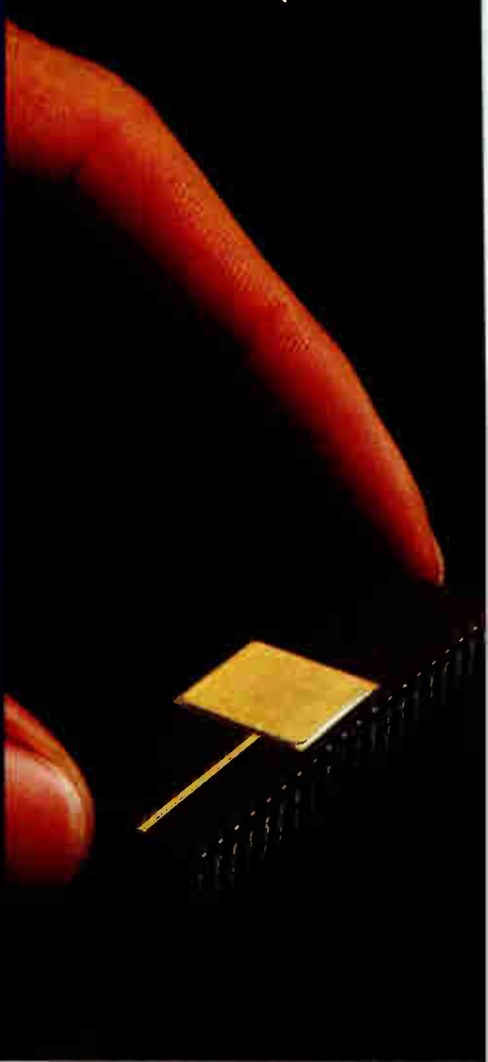
How an innovative electronics company earned a reputation as "Old Reliable."

RCA has more than its share of innovations. But we've always put product reliability first.

1963: RCA begins development of CMOS.

1974: RCA produces world's first 164,000 element chip.

1976: RCA announces first CMOS microprocessor.



As you can see, we've been innovators for years.

But ask people what they think of when they think of RCA, and they'll probably start talking about a company that's been around a long time (we started in 1919). They'll talk about a big, stable company that's been in the electronics industry from the very beginning. And they'll talk about the quality and reliability that they've come to expect from "Old Reliable."

What "Old Reliable" means.

To our customers, "Old Reliable" means quality and reliability in the products they buy from RCA.

Our goal is to produce components that perform to specification in your products. And continue to perform, day after day, month after month, year after year.

To make sure that happens, we spend countless hours on reliability research and testing. In fact, we've written more papers on product reliability than any other electronics company in the United States. We design quality and reliability into every product we make.

Leaders in CMOS.

We invented CMOS. We delivered the world's first CMOS logic parts as early as 1966. And today we offer you a full line of CMOS devices.

Last year, for example, we shipped more than one million CMOS microprocessors. Nobody else even came close. In addition, we shipped more than 175 million CMOS logic ICs.

In addition to commercial devices, we also supply a full line of High-Reliability parts. (In April 1981, RCA became the only supplier to qualify for Class S, Part 1 certification for CMOS radiation-hardened devices.)

Pioneers in BiMOS.

In 1976, we introduced BiMOS technology. Since then its parametric and performance advantages have set new standards in op amp technology.

Preparing for the future.

To make sure that we maintain the highest standards of quality and reliability, RCA Solid State is stepping up its investments in new equipment and personnel. Further, the RCA Princeton Laboratories plus our Solid State Technology Center provide some of the most advanced R&D capabilities in the industry.

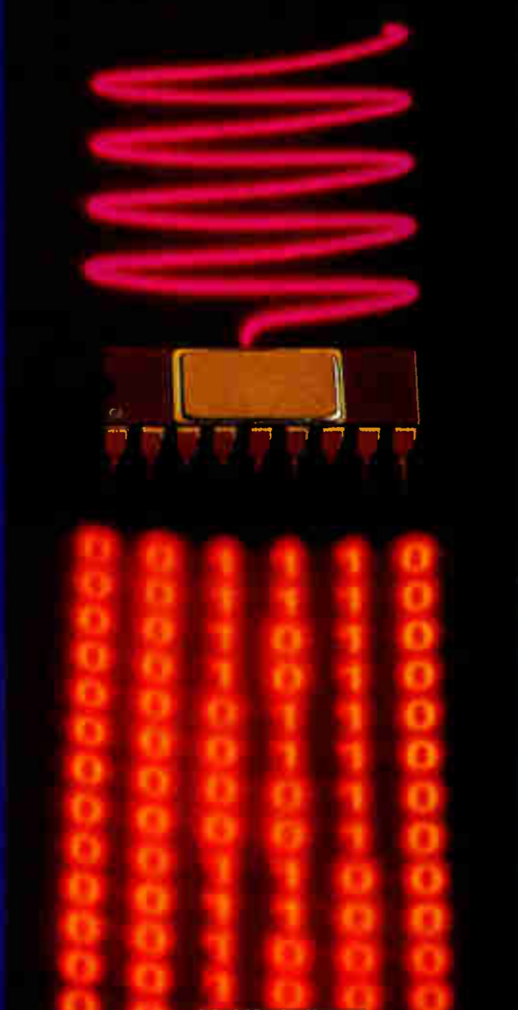
"Old Reliable" is determined to continue providing the components you need, for a long time to come.

And of course, we'll keep those innovations coming, too. What else would you expect from the people who brought you CMOS, BiMOS and television?

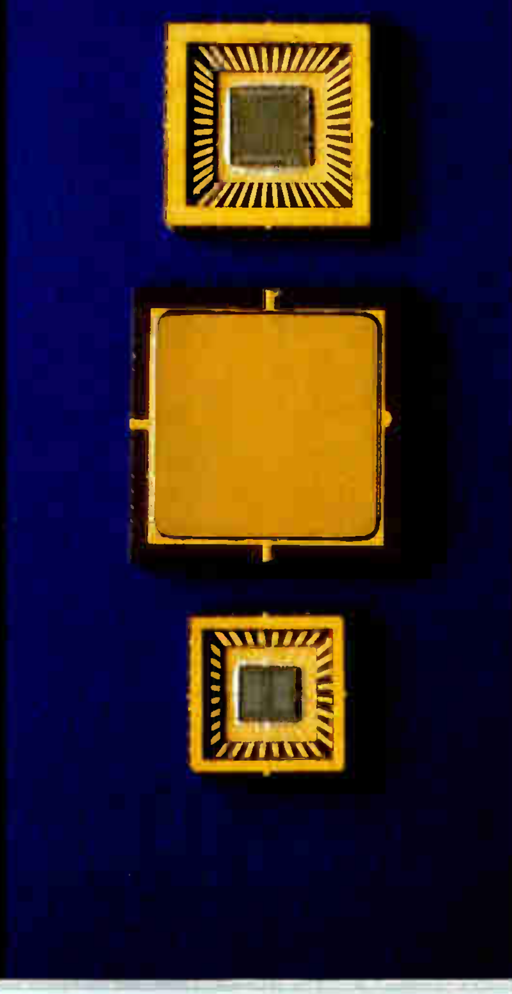
RCA

1976: RCA pioneers the first BiMOS op amp.

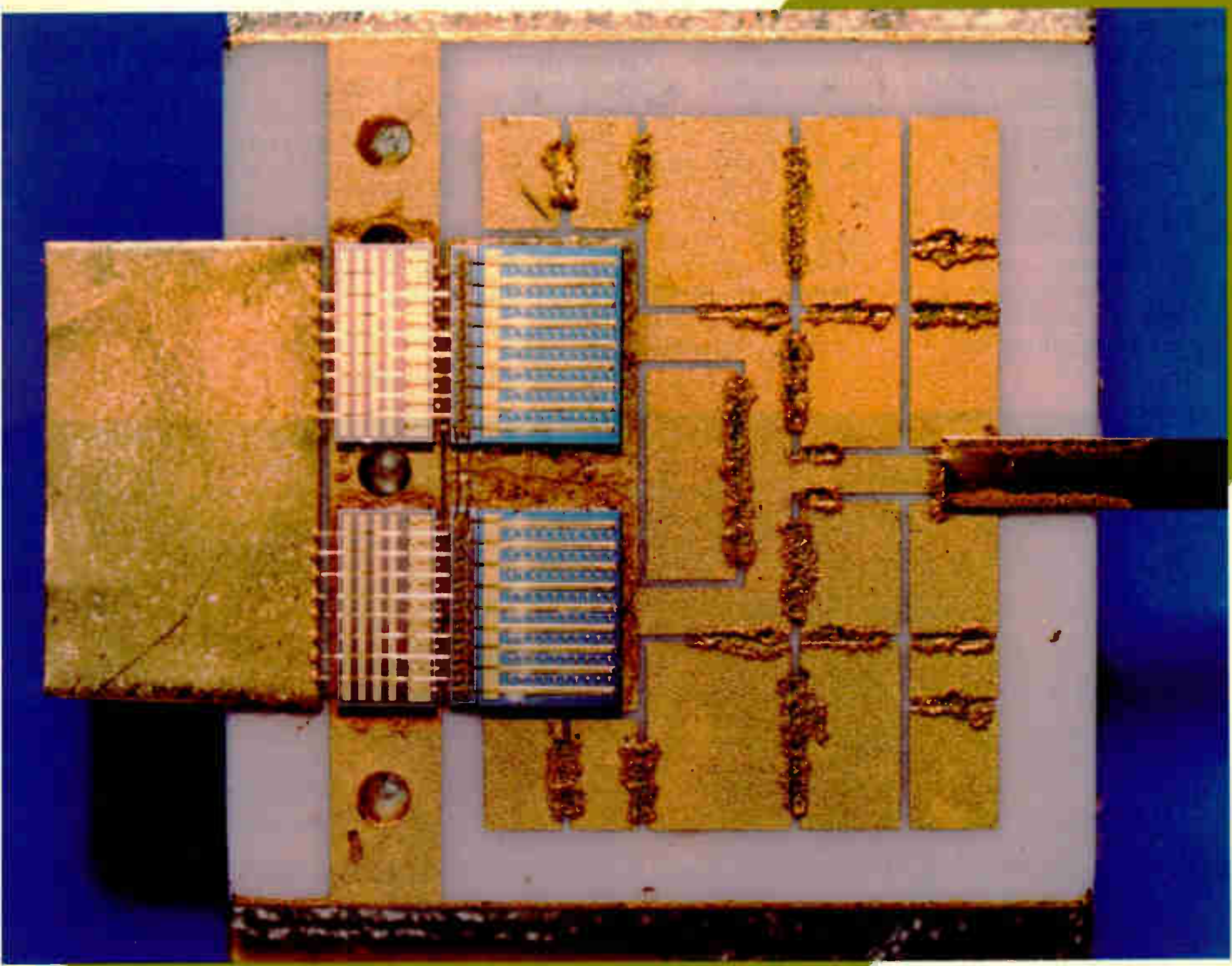
1980: RCA produces first CMOS 6-bit flash A/D converter.



1981: RCA announces expandable CMOS microprocessor chip set.



COMMUNICATIONS



The ultimate in power. Hybrid circuits such as this one from TRW Semiconductors represent the state of the art in microwave devices. The CTX-1182 radio-frequency transistor amplifier is designed for S-band radar and delivers 30 watts of peak power for a 100-microsecond pulse with a 10% duty cycle. Automatic ultrasonic bonding forms the gold wire loops that provide inductors for the circuit.

The search for increased bandwidth spurs moves to local networks, fiber-optic transmission, and digital gear in homes and offices; more satellites fill more slots

by Harvey J. Hindin, *Communications & Microwave Editor*

☐ Communications researchers and manufacturers this year neither enjoyed the leisure nor suffered the economic trials of the stagnation period mature industries often experience, as a seemingly insatiable worldwide demand prodded a constant output of innovations. New products were shaped not only by technology's advance but by Government regulation as well. Though no longer brand new, the key areas of data communications, local networks, earth satellites, fiber optics, and semiconductor chip development were upgraded to prepare for the home, office, and factory of the future. And 1982 looks as if it will continue the groundswell.

All these communications channels, whether they handle telephone conversations, computer information, or television signals, are in reality data-handling channels. Local networks, voice- and data-handling private branch exchanges, statistical multiplexers, and other gear, all based on inexpensive integrated circuits, combined to provide an array of new communications capabilities. Since these were far less expensive and more flexible than those provided by the mainframe computers of past years, it was clear that the growth of decentralized systems would be the dominant technology in the years that lie ahead.

Data encryption is necessary for certain sensitive information, whatever its source, and in 1981 the public-key system of encryption became practical. In fact, the first commercial equipment using this approach was brought to the public by its manufacturer. More such devices can be expected next year since they eliminate the need for decryption key transmittal—a costly chore that can compromise security.

Home, office, and factory communications often depend on earth satellites for inexpensive channel capacity. In a first for this technology, a 14-gigahertz all-digital bird was launched. Geared to business communications only, it is the forerunner of a series that will open up this relatively unused portion of the spectrum. What is learned here will help the 30-GHz satellites now on the drawing boards provide even more channel capacity.

The space shuttle made its first flight this year. This reusable rocket ship will enable the launching of future communications satellites without the need for expensive one-shot rockets. Thus the cost of future communications channels will be reduced and in-space satellite repair will be practicable.

Fiber-optic technology also had its share of breakthroughs. Underwater systems were designed and aircraft manufacturers looked to fiber to cut the size and weight of copper-based communications. Perhaps most important for the growth of high-speed data communications, computer manufacturers determined how to use fiber optics inside their machines. Thus data transmission by means of light, its speed not limited by the capacitance of electrical wiring, drew closer to reality. While light was being put to use inside the computers, quality fiber-optic data links for use in computer-to-computer connections dipped below $60 in price, eliminating the cost barrier to their widespread use.

All these system developments depend on the IC in one form or another. This year's developments in chip technology forecast such devices due next year as a one-chip modem built into data-generating and -receiving equipment. Also to be looked for next year are analog and digital signal processors that are software-programmed to act as filters, codecs, and the like. These will be outgrowths of this year's advances in electrical and optical logic design, optical receivers and transmitters, and microwave receivers and amplifiers—all on a chip. Among other accomplishments, new amplifier gain figures have been set and laser-diode output power records established. Moreover, the first chip-based optical AND gate was constructed, as was the first large-scale integrated cross-point array offering 256 channels.

Data communications on the loose

The major data-communications issue for the 1980s is how to control the data flow of the office, home, and factory. This chore, traditionally done by mainframe computers and proprietary networks, now has competition from voice- and data-handling private branch exchanges and flexible local networks supplied by independent vendors that can handle a diversity of manufacturer's equipment. Both PBXs and local networks showed up in bewildering array in 1981 and are likely to continue to do so in 1982 because the field is new, with an estimated market of billions of dollars. On the negative side, some local networks like the phone-based advanced communication service from the American Telephone & Telegraph Co. continued to falter, while others, like Xerox Corp.'s combined terrestrial microwave link and earth-station–based XTEN network, have been postponed.

The goal of all 1981's PBX work, as shown in products by Datapoint, InteCom, Mitel, Northern Telecom, Rolm, and others, is to route, control, and process voice and data flow. In one approach, firms like Rolm Corp. of Santa Clara, Calif., are updating their voice-only PBXs. This is possible because distributed architecture and

Going public. The Racal-Milgo data-encryption system known as Datacryptor 2 is the first commercial gear to use a public-key encryption-decryption algorithm. Operating at speeds up to 9,600 bits per second, it does not require transmittal of code words.

digital technology make the use of add-on printed-circuit boards economical. Also, layered software facilitates additional programming. This approach will no doubt be imitated in 1982 by other digital PBX manufacturers since it allows existing systems to grow gracefully as needs increase.

On the other hand, newcomers to the PBX industry like InteCom Inc. of Dallas and United Technologies Inc.'s Lexar division in West Los Angeles have of necessity developed totally new PBXs. These are still geared in large part to voice, which is, after all, 80% to 90% of the traffic in typical offices. Unlike its competitors, InteCom's unit uses packet switching for communications among its internal parts. Whether this will be used by other new PBXs is uncertain. But next year several of the totally new PBXs will incorporate fiber-optic links to connect parts of the machines at remote sites.

Perhaps InteCom's approach was the most significant step in 1981 toward solving the problem of accommodating a variety of manufacturers' data-generating and -receiving equipment with a PBX. The manufacturer introduced an add-on to its integrated business exchange that will emulate the popular IBM 3270 terminal's protocol and formats. It is a first step, the company says, to dealing with a variety of data-communications protocols. Other PBX manufacturers will have their own versions to unveil next year.

One way communications devices in an office talk to each other without the use of a PBX is by means of local networks. These were introduced at a rapid rate in 1981 and even more are slated for debut next year. Not bound to any one architecture, they range from low-cost networks for personal computers to high-data-rate links for mainframe computers. Most important, they do not require the user to purchase his data-generating and -receiving equipment from one vendor. As such, their growth next year will be explosive as economy-minded users seek cost-effective techniques to make a panoply of in-house gear.

Importantly, amidst this proliferation in 1981, Intel Corp. of Santa Clara, Calif., proposed a six-layer standard for local network architecture. The first two layers are equivalent to the existing Ethernet local network scheme. If adopted in 1982, this standard would enhance the local network concept. Simply put, the extensive software that such systems need for their operation would be the same regardless of the network manufacturer. Also expected to be approved next year, by an Institute of Electrical and Electronics Engineers committee, is a proposed industry standard called IEEE-802.

While all this activity with local networks was going on, AT&T's local network, known as the advanced communication system (ACS), designed to implement the office of the future through telephone-based packet switching, was quiet in 1981. This was due to software, regulatory, and marketing problems. The only positive note for ACS was AT&T's adopting as a U.S. standard the X.25 packet-switching protocol from the International Consultative Committee for Telegraphy and Telephony. ACS would use X.25 in its operation. Moreover, the communications giant's blessing of the European standard was expected to enhance its acceptability next year for home and office data communications.

Versatile television

Videotex services will be key in home and office communications, and AT&T was active here, too. Entering the arena already occupied by Canada's Telidon organization, England's Prestel, and France's Antiope, the U.S. firm announced its own standard for videotex services. The older players in the game will be seen scrambling in 1982 to see how they can comply.

As important as all these technology considerations are, the influence of Government regulation cannot be ignored. Among data-communications companies, AT&T is the most affected by regulation. For example, in 1981 the company engaged in its usual rounds with U.S. Government agencies. In Congress it failed to win dismissal of an antitrust suit. But, the Senate moved to permit it to enter unregulated markets for information-processing equipment and services. Opinion has it that 1982 will see a lot more debate on these matters, which will affect American communications technology for years to come.

An integral part of many voice- and data-handling PBXs and local networks, statistical multiplexers competed for attention from the data-communications community this year. The designer of data-communications networks has always used multiplexers to combine the data outputs of a number of relatively slow transmission lines onto one high-speed line. These days, he's taking a fresh look at new versions of these machines because, with the incorporation of microprocessors and built-in software, they now offer signal processing instead of the familiar signal combining. Thus, they are more economical than before. In fact, statistical multiplexers introduced this year from a number of vendors can perform data compression, switching, port contention, encryption, dynamic network reconfiguration, down-line loading, and other chores usually associated with mini- or mainframe-computer-controlled network processors or concentrators. Next year promises more of the same with even more capabilities, as machines using 16-bit microprocessors reach the market.

The data-communications community waited throughout 1981 for the popularization of the data encryption standard (DES) that was lately approved by the National Bureau of Standards.

Since no major losses of sensitive data could be documented and there were no laws forcing the use of encryption technology, cost-sensitive equipment manufacturers did little more than offer coding equipment as options. Meanwhile, the rival public-key system, which unlike DES does not require the transmittal of a code key, made two major advances that will make it a formidable competitor to DES next year.

Until this year public-key systems (the knapsack cipher, for one) have required so much number-crunching that they have been restricted to kilobit-per-second decryption rates. This is much less of a data rate than the NBS private-key DES approach will allow. But this disadvantage no longer applies as a result of the work of Paul S. Henry, head of the optic systems research department of Bell Laboratories in Holmdel, N. J. Henry has come up with a fast algorithm for executing the knapsack cipher. It allows megabit encryption rates that will be used in future data-communications applications such as computer data-file transfers.

The other public-key system advance was announced by Racal-Milgo Inc. of Miami, Fla. In an initial step toward freeing the data-communications system designer from having to design key-transmitted systems, it released the first commercial application of public-key cryptography in a data-encryption device. The company's Datacryptor II is designed to prevent unauthorized access to transmitted data by encrypting and deciphering it at rates of up to 9,600 bits per second.

To satisfy the demand for channel capacity, earth satellites, those apparently stationary machines that retransmit voice, data, and video information from ground station to ground station, continued to be launched or contemplated worldwide in 1981.

The best-known event of the year was Satellite Business Systems' launch of a communication satellite that was the culmination of five years of work at an expense of $350 million. The result of the McLean, Va., firm's effort was an all-digital system with a 14-GHz uplink and a 12-GHz downlink that provides a combination of data-communications operating modes and services that the company hopes will be irresistible to cost-conscious customers. SBS's system will shortly be extended to Canada. Moreover, in the next few years it will accommodate the smaller user who cannot support an on-premises earth station, using local networks connected to a central earth station by fiber-optic cable or microwave link.

Meanwhile, encouraged by the success of such U. S. endeavors as the SBS satellite, 17 European nations planned this year to spend $100 million on a 1983 launch of a pair of locally manufactured satellites to handle computer traffic, teleconferencing, electronic mail, and other business services. Thus, the postal and telecommunications authorities that control such activities in Europe are making sure that the office-of-the-future is not just a North American phenomenon in the 1980s.

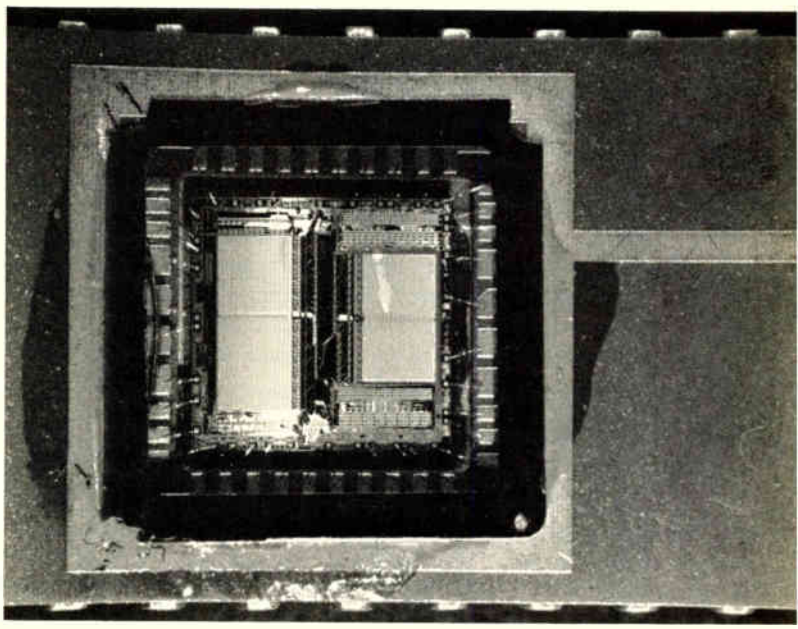
Besides their future office and home applications, satellites will be important throughout the decade for their ability to perform high-technology work impossible to accomplish on the ground. For example, Europe and the U. S. announced cooperation in a project involving satellite-borne lasers. Their goal is to synchronize atomic clocks in Europe, India, and North and South America to within 1 nanosecond. While nanosecond precision is now necessary only for scientific experiments, the European Space Agency, which is running the project, predicts such precision will soon be needed for international high-speed digital communications.

Fiber optics for flexibility

Fiber optics in 1981 made advances in new areas of technology that promised more flexibility in the design of the data-communications system. Most important, computer makers buckled down to serious work on fiber-optic links for their systems. Several mainframe manufacturers, notably Sperry Univac in Blue Bell, Pa., devised means for running light-wave lines between central processing units and peripherals. The goal was to transmit the information reliably at the speed of light and to remove the wiring-capacitance speed limitation of conventional systems.

Since the typical computer interface comprises control, handshaking, and data lines in parallel, the first step was a parallel-to-serial converter that permits use of a serial fiber-optic line. A parallel link is too expensive and wasteful of the fiber's data (bandwidth) capabilities. Just such a 250-Kb/s device was built by R. Kirk Moulton, principal engineer at Sperry Univac. It is fast enough for such peripherals as printers but not for high-speed storage equipment like disks. In 1982 the computer industry will move toward even higher speeds.

After telephony, short-run data communications is the largest application area for fiber optics. The breakthrough in this area was in price-performance ratio, and



Lots of channels. The Mitel cross-point array chip, which is at the heart of the company's 10,000-line voice- and data-handling private branch exchange, is an oxide-isolated C-MOS device that handles 256 channels at one time and switches in both time and space.

Hewlett-Packard, Motorola, and other firms introduced appropriate data links for these applications, which from HP featured a $55 tag.

For HP's price the user bought a link complete with transmitter and receiver suitable for computer-to-peripheral connections up to 20 meters long, with a data-rate capacity of dc to 10 Mb/s. Units priced like this were expected to remove the price barrier that has precluded the fiber-optic data link's widespread use. Just as prices will continue to tumble in 1982 for longer-run links for color television and other high-quality signals, the fiber link will become even more commonly used because of its immunity to radio-frequency interference and its freedom from tapping.

Data links and even raw fiber must be tested in both the field and the laboratory. And, now that optical-fiber communications are competing with copper-wire installations on a cost basis, it is essential that link testing be only a small part of a system's cost. So 1981 saw cost-effective optical time-domain reflectometers standing in for the testing job, and more such equipment is due off the drawing boards next year.

In all these reflectometers, the separation of the transmitted and reflected signals and the processing of the reflected signals were prime. Typical of the new devices available was one from the International Telephone & Telegraph Components Group in Paignton, Devon, England. The microprocessor-controlled ITT-OFR-1 carries out automatic test routines on the extensive fiber-optic communications systems that British Telecom is expected to install this decade. It features both oscilloscope and chart-recorder data readouts. Such instruments are also under study by HP and Tektronix. When they are finally introduced, they will enhance even further the appeal of fiber technology.

There is room in today's fiber-optic technology for classic circuit techniques. In Japan, the 50-year-old concepts underlying the superheterodyne receiver are being applied to that most modern gadget of communications technology, the fiber-optic receiver. The result is what Nippon Telegraph & Telephone Public Corp. claims is the world's first fiber-optic laser-driven superheterodyne receiver. It has been tested both as a 300-megahertz analog device and as a 100-Mb/s digital service.

The superheterodyne approach is noteworthy because, unlike p-i-n diode or avalanche photodiode receivers, optical superheterodyne systems can select carriers spaced only a few megahertz apart. Thus, they can fully exploit the fiber's bandwidth of hundreds, if not thousands, of megahertz. This selectivity will work well with the as-yet incomplete 1.3-micrometer optical-fiber communication system. These have more available bandwidth than present 0.8-μm systems and are starting to appear around the world.

Chips galore

One of the most significant LSI products of 1981 for the communications industry was a cross-point array produced by Mitel Corp. of Kanata, Ont., Canada. The chip replaces 100 parts of medium- and small-scale integration with the reliability of one very large-scale integrated part. The array promises to revolutionize the techniques used for switching in PBXs and telephone switching offices, as it uses so little space and power (see "A big switch was put on a chip by Whitbread's team," p. 225). Designed to switch any of 256 input channels to any of 256 output channels, it is the key element in Mitel's new 10,000-line voice- and data-handling PBX.

The chip is typical of what will be made available to data-communications equipment manufacturers because of the rapid growth in capability of the VLSI industry's data-communications operations. Codecs, time-slot assigners, and subscriber-line interface chips have proliferated. But more importantly, the chip-manufacturing industry has some surprises up its sleeve: it is preparing analog- and digital-signal–processing chips that are software-controlled. These chips, at the system designer's will, are designed to provide the functions of codecs and other such devices. Thus special features peculiar to a particular manufacturer may be had from readily changed software, not a costly custom design.

While the Mitel chip is concerned with electrical logic levels, optical logic design received a boost this year at Bell Laboratories, where researchers came up with a two-input AND gate on a semiconductor chip. The chip reacts to a pair of light signals at different wavelengths. Its output is an electrical signal that can be used to trigger either a light-emitting diode or a laser.

The Bell chip, based on a pair of photoconducting pn junctions in series, provides system designers with the ability to gate light signals. This is crucial to the construction of optical signal-processing systems for intracomputer communications. Bell is working to extend this concept to multiple input gates and other kinds of logic that could be used to make optical computers and switchgear. Such systems, not limited in speed by transmission line capacitance, would rival Josephson-junction machines in capability.

While Mitel looked at electrical logic and Bell looked at optical logic, IBM Corp. looked for a cost-effective chip that would act as an optical receiver and convert light into electrical pulses at megabit rates. Success in this endeavor would lead to, for example, high-speed data-file transfers from the computer to the end user. Today this process is often uncomfortably slow.

Although further work remains for next year to further reduce the chip's cost, IBM researchers did succeed in building an optical-receiver chip that can match the capability of earlier hybrid designs. Key to the new receiver design is the use of current-mode amplification in place of the more usual integrating or transimpedance amplifier. IBM's Thomas J. Watson Research Center in Yorktown Heights, N. Y., claims that the new design can take full advantage of fiber-optic cables' information-carrying capability of 200 Mb/s or more.

Not only were new chips designed in 1981 for rf and optical wavelengths, but microwave chips came in for their share of attention, too. There are only a few monolithic microwave chips on the market and so semiconductor-intensive microwave systems tend to be costly. This year's advances in monolithic microwave technology are expected to cause some system price reductions in the next few years. However, as few microwave systems are produced in large numbers, it is often difficult to

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justify the expense of realizing them in chip form.

An area that needs large quantities of chips is microwave data-communications amplifiers. With this in mind, Cornell University researchers in Ithaca, N. Y., accomplished a monolithic integration of an optical field-effect-transistor transit-time detector and a high-speed, broadband, gallium arsenide metal-semiconductor FET amplifier. The device has a midband voltage gain of 5 V with a 4-GHz bandwidth into a 50-ohm load. Thus it has great promise as a reliable, high-quality data-communications amplifier.

Not yet concerned with monolithic integration but taking a step in that direction, Microwave Semiconductor Corp. in Somerset, N. J., built the most power-efficient solid-state device reported at X band. The GaAs FET amplifiers, in 1-, 2-, and 4-watt versions, are internally matched and use a self-aligning flip-chip mount. As nearly monolithic devices, they will enhance the reliability of future X-band radar systems.

Still another record was set this year for discrete-laser-diode technology. What is claimed to be the highest single-mode power ever recorded for a semiconductor laser was achieved by RCA Laboratories in Princeton, N. J., which produced a diode with 40 milliwatts of output power per facet. Thus, using this powerful transmitter, the fiber-optic systems of the next few years can be expected to operate without the aid of repeaters over larger distances than previously possible.

Local-network devotees were treated to a new chip type in 1981—the first IC for connecting data-processing equipment to a local network. Built as an n-channel MOS device in a 40-pin dual in-line package, it is not general-purpose but is designed only to connect Datapoint Corp.'s proprietary Attached Resources Computer local network (Arcnet) to a Datapoint work station.

The chip, the forerunner of many such chips being designed for Xerox's Ethernet and other local networks, carries data at 2.5 Mb/s by means of a proprietary protocol. It handles the equivalent of the physical- and data-link functions of a layered communications architecture and promises a reliable, low-cost local network interface with data-generating and -receiving equipment.

A big switch was put on a chip by Whitbread's team

"An exercise in human factors"—that was the key to Mitel Corp.'s recent success in a two-year project to design a new switching chip in a parallel effort toward a private branch exchange for voice and data handling. According to J. Ray Whitbread, vice president for research and development for the Canadian company, prepping the team was more than half the battle, once the company fielded its experts in chip logic, system architecture, silicon realization, memory management, process technology, engineering layout, and testing.

Whitbread, with the Kanata, Ont., semiconductor and communications systems manufacturer for six years, for the last two years headed the team charged to design Mitel's new DX chip. The result is a cross-point array that measures 270 by 270 mils, has 256 input and 256 output channels, and uses oxide-isolated complementary-MOS technology. The DX is the cost-effective core of the company's recently introduced 10,000-line SX-2000 PBX.

The human factors for which Whitbread felt his team had to prepare meant encouraging "highly individualistic people" to work together with a constant exchange of ideas and the ability to shift focus between microscopic DX chips and the macroscopic SX-2000 system interface "Many companies have the requisite technology and skills," Whitbread says, "but what counts is how they use these assets to make key choices—for example, how to partition the technology functions: will the cross-point array function be performed in hybrid, discrete, or VLSI technology? This choice is visible early and controls the economics of the final product."

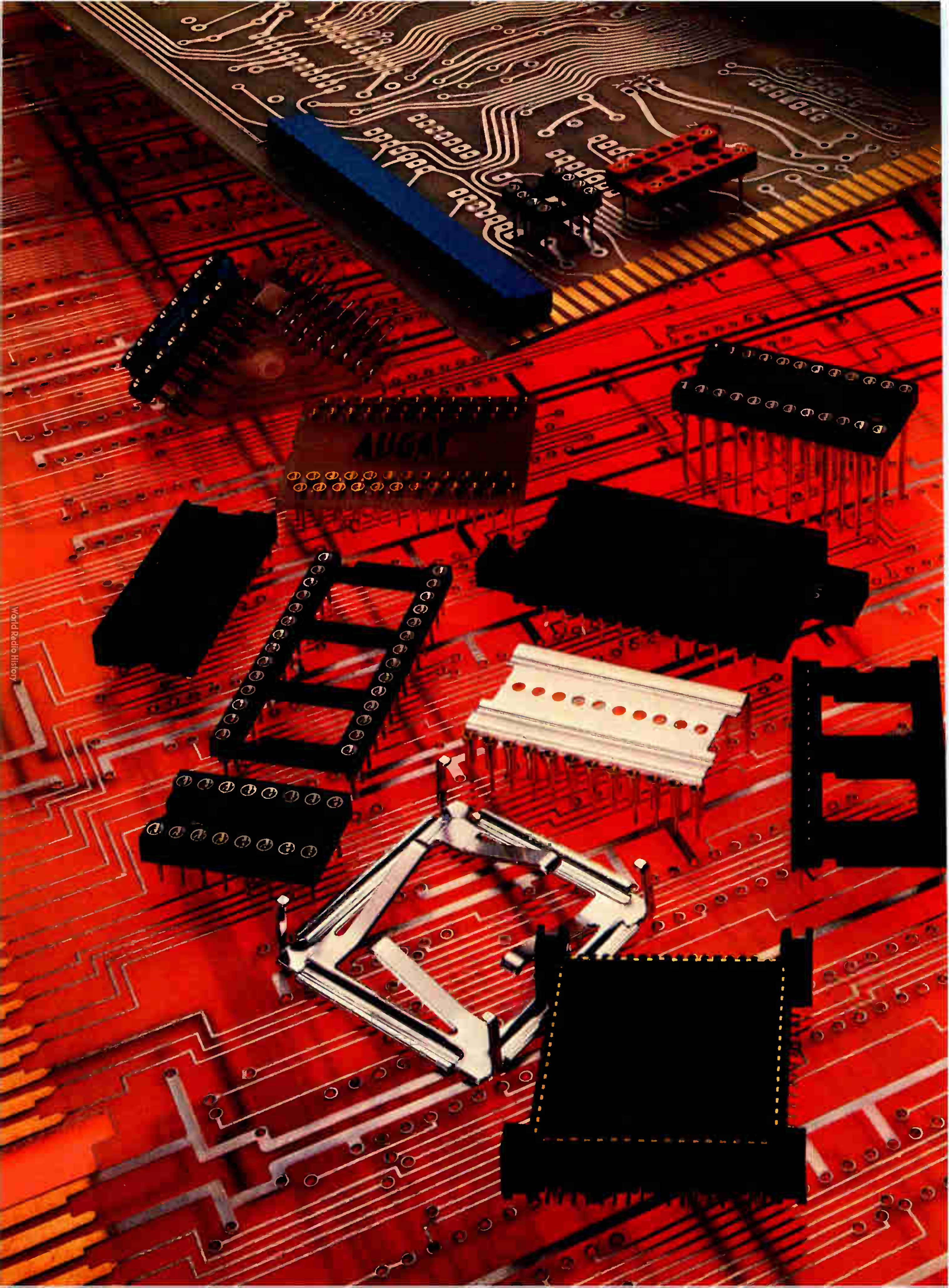
The DX chip switches in a nonblocking mode in either time or space. As such, 2,000 of the chips are incorporated in the SX-2000, which can be used as a data encryptor since it is a bit scrambler under microprocessor control, a concentrator for a standard T-1 carrier from the American Telephone & Telegraph Co., and a general tool for memory-management functions like data-addressing.

The senior engineer realized from the beginning that the chip, essentially a random-access memory, needed a finely tuned control architecture to be successful. When the project started in 1979, there was nothing available in the way of switching control that could force approximately 4.8-K of RAM to behave like a cross-point array. "The challenge was to do this economically for a practical system like the SX-2000," Whitbread says. His background was ideal—experience with linear and hybrid devices at Microsystems International in Canada and Plessey Semiconductor and General Electric Corp.'s Telecom division in England. He is a 1962 electrical engineering graduate of Aston University in Birmingham, England.

The DX's 4.8-K of memory is organized into four blocks each with an access time of 125 nanoseconds. If there was one nightmare that caused Whitbread to think that the project might fail "as all projects can," it was how to organize the memory internally for interconnectability and control so that the SX-2000 would be a flexible, expandable system. "But we did it," he points out. "And it's a practical, cost-effective system."

Whitbread, particularly proud of the "team effort with no lead position" that produced the DX, already has two new projects in view. The first is to maximize the chip's production yield. For the second project, he is looking into ways to reduce the design rules from between 4 and 5 micrometers to 3 μm.

-Harvey J. Hindin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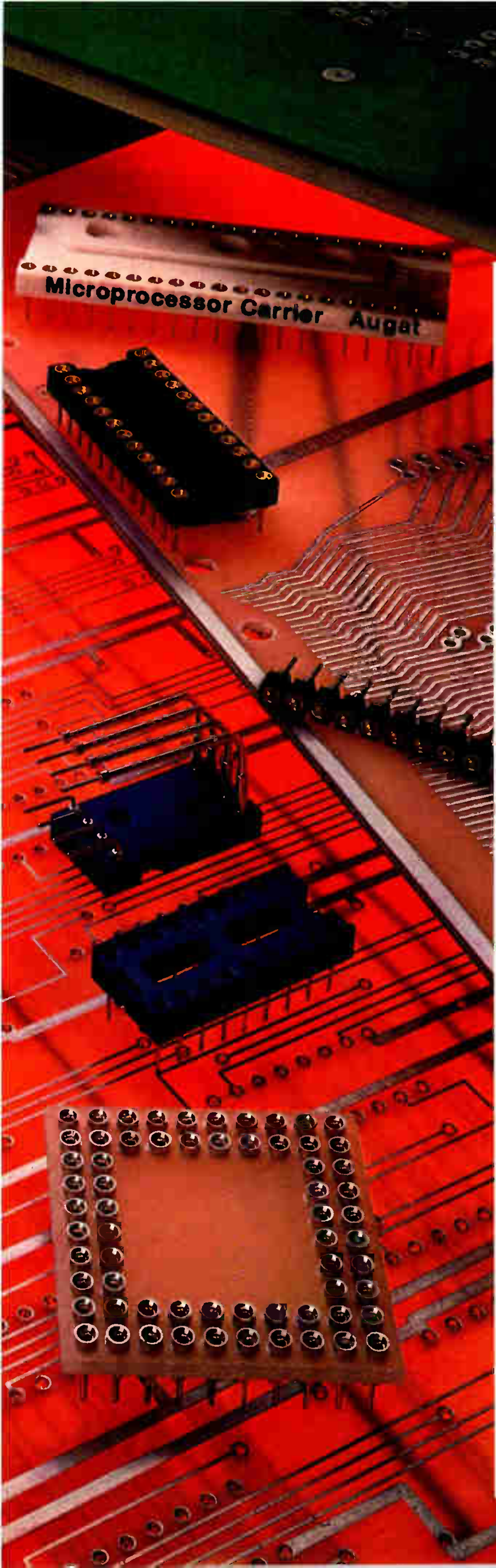
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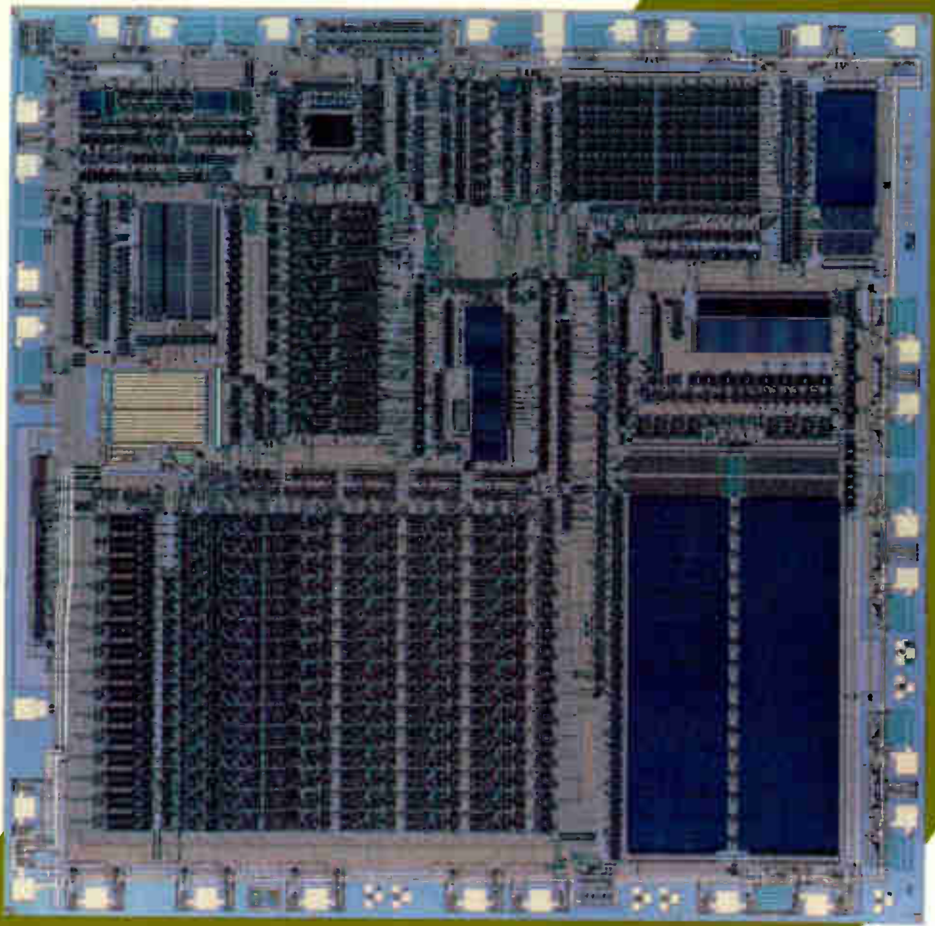

Speech system. Talking appliances are around the corner, now that speech synthesizers fit on a single chip. Hitachi's complementary-MOS 61885 takes commands from a keyboard or bus, requires only a simple filter and gain stage to drive a speaker, and stores about a half minute of speech.

The era of portable audio and personal video begins, with digital signal processing on the horizon; speech synthesis takes hold as the feature of the future

☐ Although cost is so critical a factor in consumer products, premium features continue to ring up sales. In fact, throughout the consumer electronics area, adding a microprocessor to remove drudgery, automate, simplify, or otherwise enhance a product means greater popular appeal. Speech synthesis, not unlike the digital display revolution, becomes a feature hung onto the microprocessor bus like many other outputs. Analog inputs are entirely accepted, and voice recognition borders on becoming just another input.

Circuit integration in general is improving consumer equipment across the board, attacking traditionally nonintegrated apparatus such as video and audio equipment. The outcome can only be better-quality images and sounds, streamlined design, and more sophistication—all at a lower cost than ever before. In both audio and video gear, digital signal processing is inevitable, for though the 14- to 16-bit digitizing resolution is barely affordable now, it will be within the next few years. For televison, the harbinger was a very large-scale integrated-circuit set announced last summer by ITT Intermetall in West Germany. Intermetall's goal? Nothing short of a full digitized single-chip television processor built with a 1-micrometer VLSI process—by 1985.

The VCR revolution

If the video-tape recorder was the salvation of the television studio, then the video-cassette recorder could serve as the vehicle for a resurgence of the home TV segment. The popularity of VCRs—as well as their high price—has led to what could be the next big trend: video components. Using the recorder as the start, set owners of the future would be able to hang on tuners, monitors, cameras, and a host of other shiny features, just as is done with audio component rigs.

For example, at the June Consumer Electronics Show in Chicago, Kloss Video Corp. showed off a $2,495 wide-screen projection-TV monitor minus tuner. By plugging the monitor into a VCR, the owner can save $600 to $1,500, say the Kloss people. From Sony Corp. in Japan comes the Profeel (for "professional feeling") line, with U.S. introduction scheduled for this fall. The line includes two monitors, one 19-inch and the other 25-in. Among the components available for the high-definition monitors are a tuner, a wireless remote-control infrared unit, and the Telecine Adaptor, which permits transfer of a film or slide to video tape. Not to be outdone, another Japanese giant, Nippon Electric Co., has developed a component line as part of its effort to enter the consumer field. It features a 60-in. screen and, like Sony's, stereo sound.

Even as video components are opening up what set makers hope is a huge new market, development of digital color TV continues apace. In early September, the hit of the West Berlin International and Video Fair was not so much what was in the buildings on the fairgrounds, but the showing in a downtown hotel of ITT Intermetall's first digital color TV signal-processing system. Composed now of six VLSI circuits (a figure the company hopes to reduce to three and eventually one), the digital system will be able to handle PAL, Secam, and NTSC, as well as upcoming high-definition sytems and other nonstandard schemes.

CBS Inc. executives are intent on digitizing TV production, with conversion to analog signals coming only at the final transmission stage. Reports from the CBS Technology Center in Stamford, Conn., say that researchers have managed to reduce the number of digital elements in a 525-line picture from 114 to 29 megabits per second with no degradation in quality.

The object of all this work, at least for the consumer, is a better picture. Another development toward that end is high-resolution TV. A joint effort by CBS, Japan's Sony Corp. and NHK (the Japanese Broadcasting Corp., which developed the technique) has produced a prototype system that increases resolution to 1,125 lines from the 525 standard in the U.S. and the 625 in Europe. CBS says that service will be available in the 1980s, but there are technological problems to be solved before then. For one thing, high-resolution TV now eats up about 30 megahertz of bandwidth as opposed to today's 6 MHz. Digital transmission is believed to be the answer, but digital data must be compressed so that it can fit into 6 MHz. Sony reports that it has packed 43 million bits on a square inch of tape, but that is only the start: for high-resolution TV broadcasts via tape, that figure must be quadrupled.

Even as the market for home 8-millimeter movie cameras is being erased by VCRs and their camera accessories, Sony has come along with what amounts to a highly sophisticated snapshot system—the Mavica. This charge-coupled-device zoom camera (which can be used as a video camera when connected to a VCR) in effect imprints a small magnetic disk with 50 still pictures that can be stored, transferred to a video cassette, transmitted over a phone, or mailed.

Another video technology waiting for its time to come is projection TV. Zenith Radio Corp. of Glenview, Ill., may have pushed the clock ahead a bit with its 45-in. unit. The Zenith innovation, in addition to a recessed screen, is managing to eliminate the need for frequent manual adjustments for proper color convergence. According to the company, this is accomplished by tilting the face-plate panel 7° within the two outer tubes in the three-tube in-line projection system.

Another future home companion waiting for its big break, at least in the U. S., is videotex. That break may have been the announcement by American Telephone & Telegraph Co. of a terminal that will be handle both the Canadian Telidon and French Antiope systems.

Sounds good

The Walkman story dominates the audio market. Sony's ubiquitous walk-around cassette player has given its name to the market—to the average consumer, they are all Walkmen—and triggered a revolution in portable sound.

Made possible by the miniaturization afforded by a samarium-cobalt magnet and light Mylar drive element in the headphones, as well as a small, powerful motor, the cassette players were the brainstorm of Sony chairman Akio Morita. Now there are fm-receiver versions, not to mention some that can even record off the air. With all this, prices are coming down, giving many American cities the nether-worldly look of places crowded with zombies wearing headphones.

Interestingly, some of the personal portables even offer the bias and equalization circuits needed for metal-particle tapes—those princely cassettes costing upwards of $10 apiece that promise to deliver unexcelled signal-to-noise ratios and maximum dynamic range. Though tape manufacturers would hesitate to admit it, metal-tape sales have been less than a quarter of initial projections—partly because of price, but also because of the public perception that not only were the advantages not worth the price, but metal seemed a merchandising ploy to sell new equipment.

In fact, metal tape, which actually consists of a powdered alloy of iron, cobalt, and nickel that is polymer-coated to prevent rusting, offers superior coercivity and remanence, since its crystal structure consists entirely of ferromagnetic materials and contains no nonmagnetic elements. A good deal of its technology is quite new, requiring particle refining, magnetic paint mixing, and special coating techniques.

An even more promising technology that is still in the experimental stages is vapor-deposited tape, which relies on sputtering techniques not unlike those used in IC processing. Vapor-deposited, or evaporated, tape promises the highest coercivity and will be essential to forthcoming hi-fi microcassette audio systems and miniature video-camera–cassette units. Some say that the push in both types of metal audio tape was intended to help pay for ongoing research-and-development costs in advance of the market truly opening up.

Evaporated tape, whose 0.4- to 0.6-μm particle size is a tenth that of current coated tapes, will enable microcassettes to double their playing time by cutting tape speeds in half to $^{15}/_{32}$ in./s. At that speed, the tiny tapes can run for three hours. Within the next year or so, therefore, the Walkmen will shrink remarkably as they adapt microcassette formats. Also making possible the transition will be a new type of home tape deck that is already hot in Japan—a combination standard-cassette–microcassette recorder that can transfer tunes between the two mediums.

Portable hi-fi. Sony revolutionized portable sound with its Walkman, the high-quality stereo cassette player for one (or two). Next year, units will shrink further to the smaller microcassette format, made possible by improved metal-particle tape and noise-reduction ICs.

Another technology headed for market is the digital audio disk. The DAD is described as an order of magnitude better in sound fidelity than current digitally recorded disks that must be played back on conventional equipment. Most of the manufacturers of the miniature playback systems are Japanese, and most employ a master recording, made by pulse-code–modulated laser beam, whose modulations are detected and converted into an analog signal for playback.

However, hopes for a single worldwide standard took a hard blow when the 49-company Digital Audio Disc Standardization Conference failed to do just that. Instead, it published a report describing the three formats that were proposed and wound up its three years of efforts with a zero. The majority did, however, favor the Netherlands' NV Philips Gloeilampenfabrieken approach, which uses a 4.7-in. disk.

At the same time, the rearguard action in the war against audio noise continues to produce good results. For example, National Semiconductor Corp. of Santa Clara, Calif., developed an IC-based system that requires no preprocessing and can thus reduce noise in previously recorded material by as much as 10 decibels. Behaving like a dynamically variable low-pass audio filter, it

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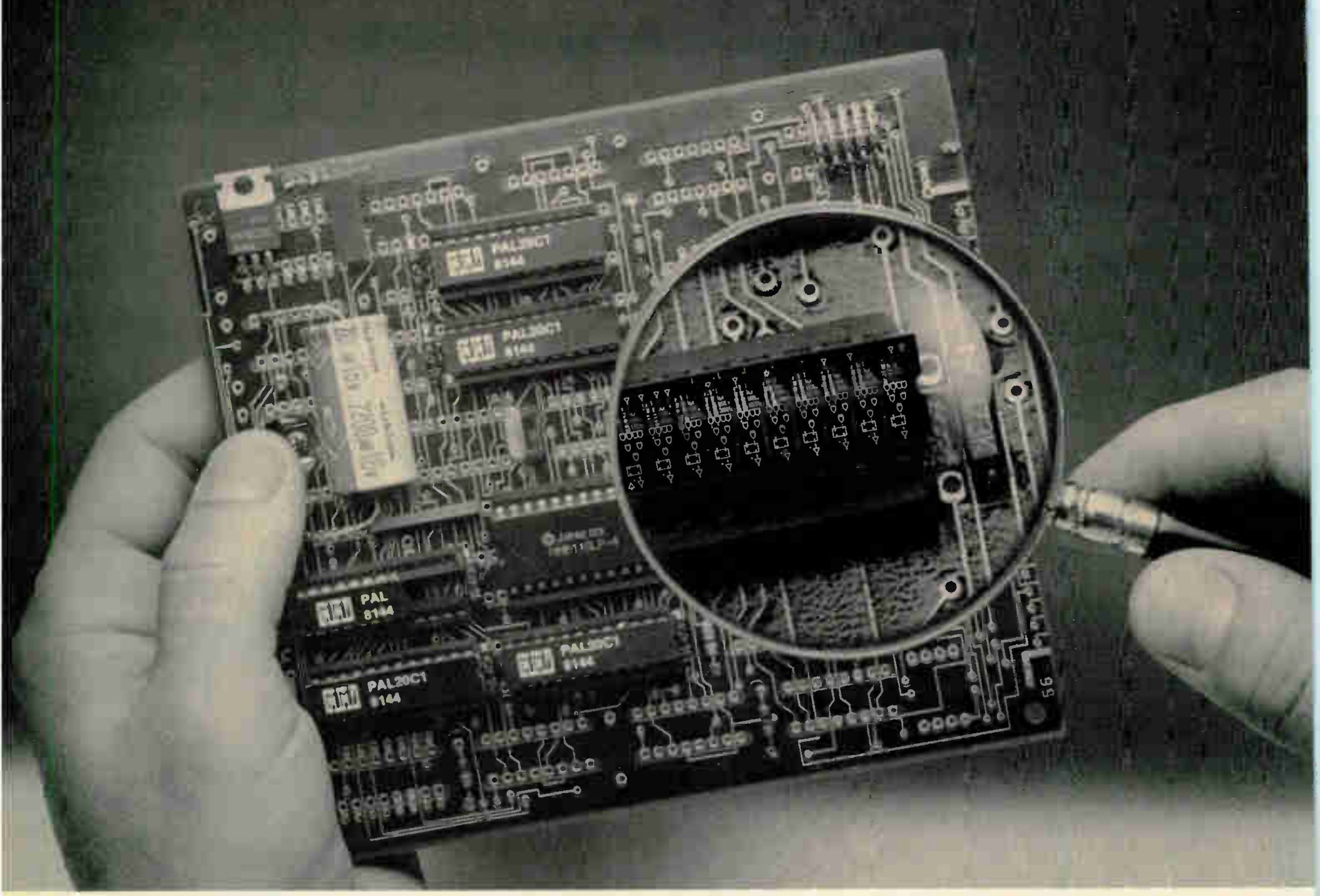

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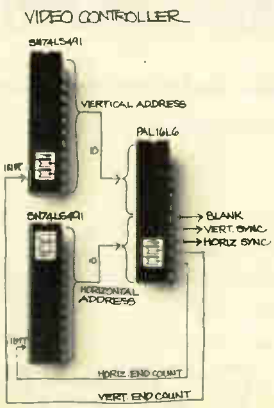

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screens out high-frequency noise (or hiss) when there is little or no signal at the upper end of the audio spectrum. When actual high-frequency signals do appear, the filter opens—up to 30 kilohertz, should that be necessary—to pass the signal.

Another entry is CBS's audio noise-reduction system whose decoders are to sell for $50 to $100. Decoder ICs are coming from Signetics Corp. in Sunnyvale, Calif. And finally, not to be outdated, is Ray Dolby, who introduced his next-generation noise-reduction system, Dolby C. The new approach essentially cascades a pair of Dolby B stages to double noise reduction to 20 dB. Now that noise-reduction systems have been reduced to chips, next-generation tape decks will offer all of Dolby B, Dolby C, and dbx—the companding noise reducer popular among professionals.

Home movies. Portable video-taping systems like this prototype Micro Video Cassette from Sony could appear as early as next year, thanks to strenuous competition in Japan. The units pack leading-edge technology: CCD imagers, LSI, and evaporated-metal tape.

Talk, talk, talk

In speech synthesis, the aim continues to be cheaper systems, of course, as well as ones that sound more like human beings than the mechanical, robotlike utterance with which they have been associated. Single-chip designs were also introduced in the course of the year, geared eventually to bringing costs down as production succeeds in building up.

Early in 1981, General Instrument Corp., for example, began shipping its SP-0256, its single-chip, n-channel MOS speech synthesizer. The 45,000-square-mil chip, from GI's Microelectronics division in Hicksville, N. Y., combines the synthesizer with a 16-K mask-programmable read-only memory that stores data and instructions for producing 256 discrete sound sequences, a 12-pole adaptive digital filter that models the human vocal tract, and a 4-bit microcontroller. GI combines linear predictive and formant coding to produce the sounds and uses an algorithm that removes redundant information from the data to be stored.

Later in the year Japan's Hitachi Ltd. began showing off a single-chip synthesizer made with its advanced, 3-μm silicon-gate complementary-MOS process, called Hi-C-MOS, originally developed for memory products. The low power drain of the C-MOS chip (30 milliwatts when operating at a 800-kHz clock rate at 5 volts, and 25 microwatts on standby) is suited to applications in hand-held battery-driven products like talking calculators and watches that tell time. Hitachi has applied a partial-autocorrelation, or Parcor, method to modeling the vocal tract. This approach is, for all purposes, the same as that used in its pioneering speech chips by Texas Instruments Inc. of Dallas, which describes the method as linear predictive coding.

Hitachi has improved sound quality in the one-chip approach over its 38880 multichip entry by prefiltering the speech to distribute energy over the spectrum. The technique lessens the usual dependence on a small number of filter coefficients, which can now be less exact.

Of note is a technique called contextual recording used in speech-synthesis applications by TI in the interest of conserving vocabulary storage. Many applications require phrases that sound best when synthesized as entities. But in a given application, several phases often contain the same words, which it would be much more economical to store separately and then string together—but stringing sounds unnatural. TI's contextual recording employs a linguistics expert to select words spoken with an intonation so general that they can be strung together into phrases and still sound fairly natural. The linguist actually edits the speech at a terminal, working with the speaker.

In general, techniques will continually be applied to speech synthesis with a goal of improving quality without the penalty of higher bit rates. The next major trend will be in reducing the cost of speech analysis through dedicated hardware. That will surely boost the number of applications, as vocabulary preparation is, as yet, a slow and deliberate process requiring sizable computers.

Going past chips to reach the market for add-on speech aimed at computer systems was Centigram Corp. of Sunnyvale, Calif. It introduced its Lisa terminal, which applied what the company refers to as parametric waveform digitization. The result is perhaps the lowest data rate (4,800 b/s) for forming speech of fairly high quality. Centigram, which is aiming Lisa at makers of low-volume computer-based products, offers to develop vocabulary for $25 per word—well below the several hundred dollars per word that the semiconductor makers charge.

From text to talk

Speech synthesis using a different approach also was shown off during the year. For example, TI developed an adjunct to its 99/4 personal computer that translates words typed into the terminal into speech. Software in this text-to-speech translator analyzes the words into elements called allophones, all 128 of which are stored in a library. These are pronounced by TI's TMS 5200 speech synthesizer controlled by a processor chip. Unlike TI's Speak & Spell learning aid, the translator does not rely on canned words stored in a ROM. Rather, it will read aloud words of a news or a weather report, trying to pronounce them directly from ASCII code. Although the quality of allophone stringing is yet the lowest of all methods, it is the easiest to use and is thus well suited to aids for the blind. Also, the algorithm will continue to improve over the years.

The past year also saw activity in the opposite end of the speech product spectrum: voice recognition. What had heretofore been board-level systems were being shrunk to sets of semiconductor chips. Interstate Electronics Inc., Anaheim, Calif., for example, reduced its 100-word, $2,000 voice-recognition module to a 10-chip system priced at under $500. It also went further and introduced a single chip, the VRC 01, that recognizes up to 8 words—spoken by anyone—with 95% accuracy. Aimed at toys and games, the chip costs $10 in volume.

Trying to make it easy for original-equipment manufacturer to add voice recognition to their systems, Auricle Inc., a Cupertino, Calif., subsidiary of Threshold Technology Inc., introduced a small boxed system for voice input. Dubbed the Auricle I, it permits manufacturers of computer terminals and control systems to familiarize themselves with speech recognition and develop the interface hardware and software for their products. The 7-pound unit sells for less than $2,500 and can recognize a 40-word vocabulary, expandable to 128 words, with greater than 99% accuracy. Its output is a serial ASCII code compatible with RS-232-C terminals. Also being planned is a plug-in speech-recognition module for less than $500 in volume.

In automotive electronics, the year 1981 saw a whole host of new electronic packages hit the road for jobs like controlling emissions and increasing fuel economy, displaying information to the driver, keyless entry, and speed and climate control. Some of the systems could even check themselves out, diagnosing and locating faulty components.

Auto trends

Microprocessor control seemed a byword of sorts, but as cars get smaller in the future and move to four-cylinder engines, their fuel efficiency will be high to begin with. The fine control possible with microprocessors will not be needed. Simpler circuits, or even redesigned mechanical parts, will suffice, some say.

One of the simpler electronic devices, for example, is the read-only-memory–based ignition controller introduced by RCA Corp.'s Solid State division, Somerville, N. J. Called Rombic, the two-chip system, which sets the spark advance as a function of engine speed, consists of a controller chip and a ROM. The pair will cost $7, says RCA, compared with the $20-to-$40 chip cost for microprocessor-based systems being planned. Moreover, built of C-MOS technology, the RCA chips can withstand the heat of the engine compartment. This simplifies installation. Most engine-control circuits are made with n-channel MOS parts which must be protected from engine heat by mounting them on the passenger side of the vehicle. □

For consumers, Teramoto solved materials problems

Iwao Teramoto is a chemical engineer whose interest in chemical physics, especially reaction thermodynamics, has propelled him into the development of new compound semiconductor optoelectronic devices and other devices needed for consumer electronics at Matsushita Electric Industrial Co. in Osaka, Japan. He specializes in solving knotty materials problems that plague advanced diodes, lasers, transistors, and even solid-state sensors.

One of his most recent successes is a gallium-aluminum-arsenide double-heterojunction injection laser diode that will support the entry of Japanese firms into the digital audio-disk business—the latest hot new product, which many firms will start selling next autumn. The diode is used in Matsushita prototype systems and in a pickup that Olympus Optical Co. will be selling as a component to the industry.

Teramoto has been working on light-emitting diodes and injection laser diodes for more than 10 years. About three or four years ago he started in earnest to develop a diode for digital audio-disk players and decided that the ribbed waveguide offered promise. He soon came up with the terraced substrate configuration, in which a rib waveguide can be fabricated with a single epitaxial process.

Prototype devices operate at 8,100 angstroms, but that will soon be changed to 7,800 Å by altering the GaAlAs mixture for the necessary bandgap. Teramoto says that although the diodes will then have a slightly higher threshold current, the change will enable the use of smaller lenses, provide a slightly finer beam, and give a visible beam that is easier to use.

Among the earliest devices that he developed were red and green liquid-epitaxial gallium phosphide LEDs that are used as lamps in a variety of consumer products, including tape recorders. These set the stage that enabled him to solve a major problem.

Ultrasonic remote controls for color TV receivers had been on their way to becoming popular shortly after they were introduced. In 1971, they fell into disrepute when it became apparent that various types of noise had ultrasonic components that could turn on the TV in the absence of viewers. Teramoto pitched for a system using an infrared gallium arsenide LED fabricated by a liquid epitaxial process. This solved the problem.

Recently he has developed a method to make brighter GaAlAs LEDs by a liquid epitaxial method that processes many wafers at the same time, leading to much higher productivity and lower cost. The new method, which does not require the usual slide boat, eliminates scratches often caused by the slide and thus increases yield. Unfortunately, the method cannot be extended to the fabrication of lasers, which require four or five very thin layers.

Teramoto's present position as deputy director of the semiconductor research laboratory at subsidiary Matsushita Electronics Corp.—his employer since graduation from Kyoto University with a master's degree in 1956—allows him to work on a large number of devices at any given time. What's more, his work in the laboratory enabled him to earn a doctorate in 1964. **-Charles Cohen**

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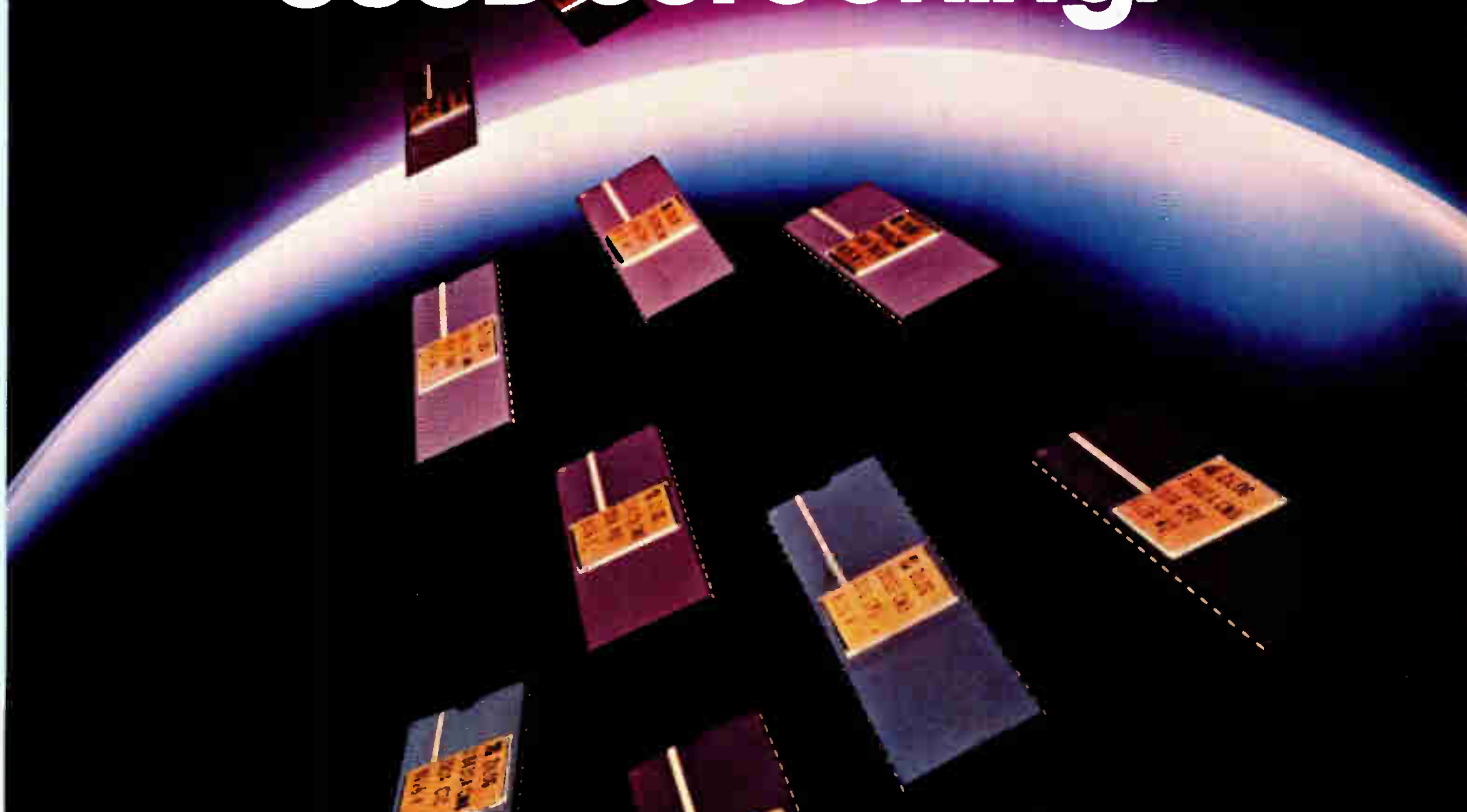

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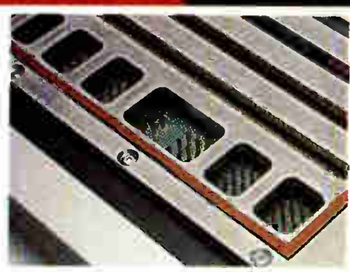

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CHRONOLOGY

October 1980

- Engineers at IBM's Data Systems division successfully put the complex logic of the System/370 processor on a single VLSI gate-array chip. *Oct. 9, p. 139*
- Local network specifications for Xerox's Ethernet are announced, including a 10-Mb/s data rate. *Oct. 23, p. 42*
- TRW brings out the first monolithic digital correlator: the TDC1023J, which processes 64-bit words at a rate of 20 MHz. *Oct. 23, p. 260*

November 1980

- Hybrid Systems announces the first monolithic d-a converter with 14-bit accuracy. *Nov. 6, p. 33*
- National Semiconductor revives single-slope integrating a-d converters with a microprocessor-based 20-bit module. *Nov. 6, p. 151*
- IBM scientists report a new method of beam processing—ion-beam annealing. *Nov. 20, p. 33*
- The long-anticipated H series bows when IBM announces its largest mainframe to date, the 3081. *Nov. 20, p. 41*
- Japanese team makes the world's first superheterodyne laser-driven fiber-optic receiver; it operates at 100 Mb/s. *Nov. 20, p. 73*

December 1980

- Entering the 32-bit superminicomputer and office automation markets, Honeywell introduces 10 machines and office software with its DPS-6 line. *Dec. 4, p. 33*
- Amdahl announces the 580 series of big mainframes that outperform IBM's 3081. *Dec. 4, p. 41*
- Bell Laboratories uses X-ray lithography to produce MOS transistors with 0.3-μm channel lengths and 40-ps gate delays. *Dec. 18, p. 40*
- A team from Bell Laboratories converts digital bits directly into analog voice signals with a simple mechanical transducer suitable for phone earpieces. *Dec. 18, p. 42*
- NEC announces the largest 32-bit superminicomputer from Japan, the MS70, with a 20% higher throughput than a VAX-11/780. *Dec. 18, p. 62*

January 1981

- Sony announces the smallest yet floppy-disk drive, a 3.5-in. microfloppy capable of storing 437.5 kilobytes. *Jan. 13, p. 44*
- Varian Associates produces a traveling-wave tube having 10 times the millimeter-wave power of prior microwave sources. *Jan. 13, p. 46*
- The NBS sets an a-d converter speed record with a 6-bit Squid-based chip that samples at a 2-GHz rate. *Jan. 27, p. 33*
- TI enters the 8-bit single-chip microcomputer market with the 7000 series that employs strip chip architectural topology (SCAT). *Jan. 27, p. 107*

February 1981

- TI discloses that it is building its 64-K MOS dynamic RAM on an epitaxial layer for better-quality components having less noise. *Feb. 10, p. 93*
- Rockwell halts commercial production of bubble memories. *Feb. 24, p. 35*
- IBM develops low-voltage inverter logic: a bipolar circuit that exhibits switching speeds faster than ECL at the power levels and densities of TTL. *Feb. 24, p. 41*
- Genisco Computers, Costa Mesa, Calif., announces development of a true 3-d computer-graphics display terminal called SpaceGraph. *Feb. 24, p. 49*
- 32-bit processor announcements abound: Intel's iAPX-432 three-chip set's object-oriented architecture matches its systems implementation language, Ada; Bell Laboratories' BellMAC uses a twin-tub C-MOS process; and Hewlett-Packard's n-MOS processor has more than 450,000 transistors. *Feb. 24, p. 138*
- The Musashino laboratory of NTT describes a 256-by-4-bit ECL RAM that has a 2.7-ns access time. *Feb. 24, p. 145*
- TI reveals next-generation 16-bit microprocessor, the 99000, which adds macrostore—a high-speed on-chip programmable memory for often-used routines. *Feb. 24, p. 157*

Significant developments in electronic technology reported over the past year in *Electronics*

March 1981	● Thomson-CSF bombards quartz crystals with ions to get 525-MHz fundamental frequency. *March 10, p. 67* ● Harris announces the model 300 superminicomputer, a 24-bit processor with a 48-bit memory word length. *March 10, p. 201*
April 1981	● West Germans test communication service that combines digital transmission and word processors for nationwide electronic mail. *April 7, p. 101* ● PMI introduces general-purpose analog-signal-processing chip. *April 7, p. 121* ● Systems Engineering Labs announces the Concept 32/87, a 4-to-5-million-instruction/s 32-bit superminicomputer that outperforms all others in its class. *April 21, p. 247*
May 1981	● Applied Materials' ion-assisted plasma etcher is first to have guaranteed specs. *May 5, p. 41* ● Bell Laboratories patterns a 0.01-μm^2 Josephson junction that achieves the technology's natural switching speed—about 1 ps. *May 5, p. 48* ● Hitachi develops a vhf lateral power MOS FET that delivers 180 W at 100 MHz. *May 19, p. 81*
June 1981	● Rockwell shows GaAs CCD delay lines operating at 1-GHz clock frequencies. *June 2, p. 33* ● InteCom introduces voice- and data-handling private branch exchange designed to work with multiple protocols simultaneously. *June 2, p. 37* ● Varian shows isothermal annealing system based on a graphite heating element. *June 2, p. 40* ● Xerox enters the personal-computer market with its aggressively priced 820 starting at $2,995. *June 16, p. 33* ● TI follows Rockwell's lead and quits the commercial bubble-memory business. *June 16, p. 93* ● The European Space Agency announces plan to launch satellite that uses a laser to synchronize worldwide atomic clocks. *June 30, p. 74*
July 1981	● Amlyn introduces floppy-disk-cartridge drive for small computer systems that uses 8-megabyte cartridge containing 5 diskettes. *July 14, p. 44* ● Scanning electron beam dynamically probes microprocessor chips for the first time at Siemens. *July 14, p. 105*
August 1981	● The first commercial 1-μm chip—an 8-bit flash a-d converter from TRW—runs at a 75-MHz sample rate. *Aug. 11, p. 37* ● IBM enters the personal-computer market with its 16-bit Intel 8088-based system having a starting price of $1,565. *Aug. 25, p. 50* ● Analog Devices builds transformer with thick-film coils for an isolation amplifier getting up to 8-kV isolation and 20-MHz bandwidth. *Aug. 25, p. 113* ● TeleSoft offers the first commercially available compiler for Ada featuring a single-board computer based on the 68000. *Aug. 25, p. 34*
September 1981	● National becomes the third bubble-memory manufacturer to pull out of the business, leaving Intel as the last U. S. volume supplier. *Sept. 8, p. 41* ● Vishay Intertechnology unveils precision foil resistors with temperature coefficients of 0.25 ppm/°C. *Sept. 8, p. 44* ● EMV Associates uses biotechnology to resolve lines of silver conductor without the need for masking or etching; the research team envisions 10- to 25-nm geometries and bioelectronic supercomputers. *Sept. 8, p. 48* ● Datapoint announces the world's first local-network interface chip, a proprietary device that interfaces only with Arcnet. *Sept. 22, p. 41*

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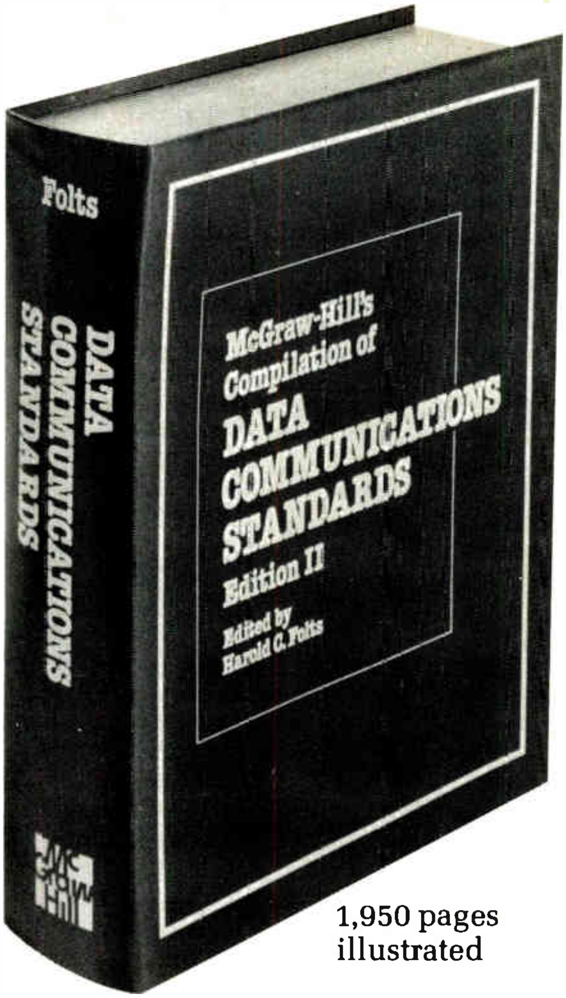

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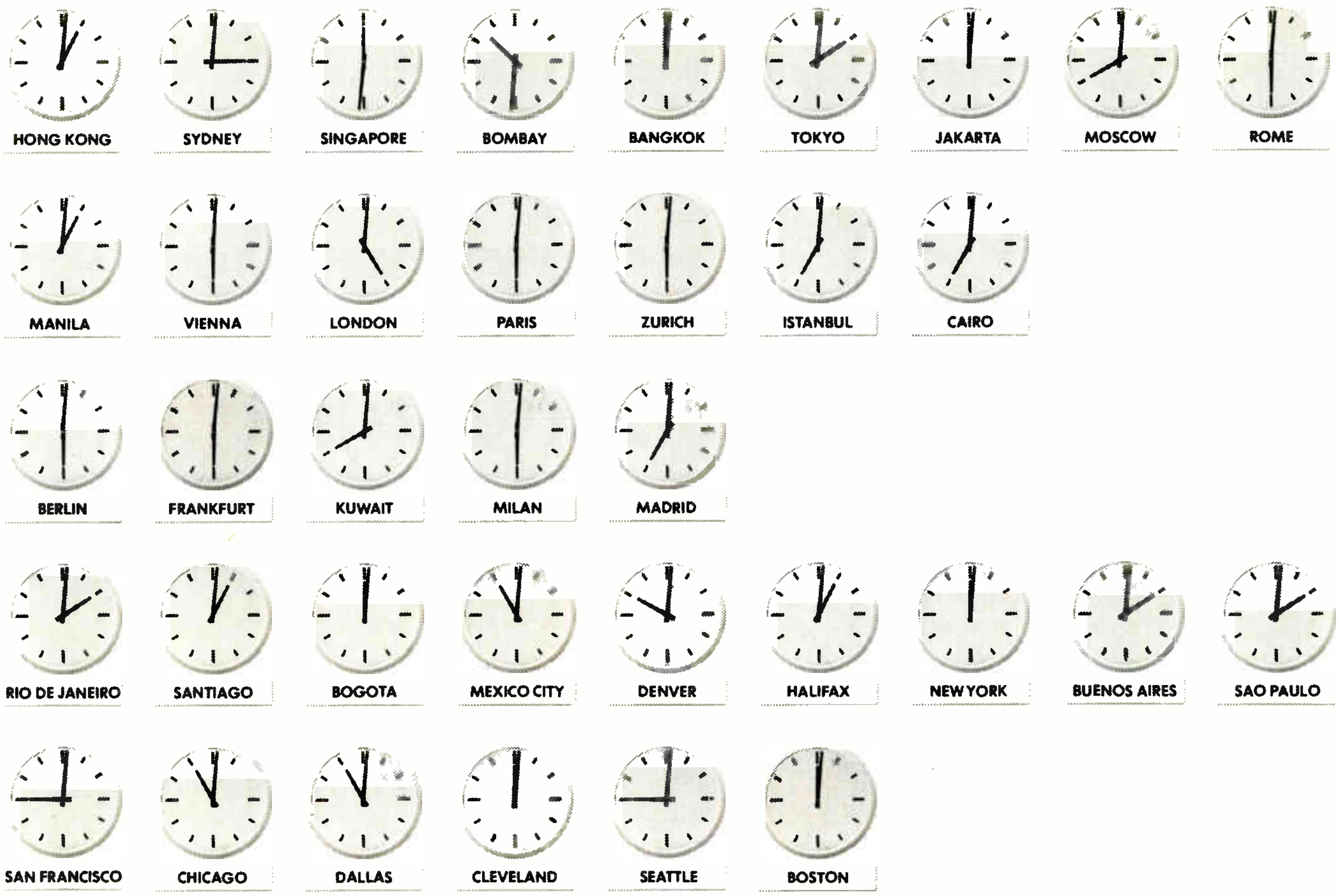

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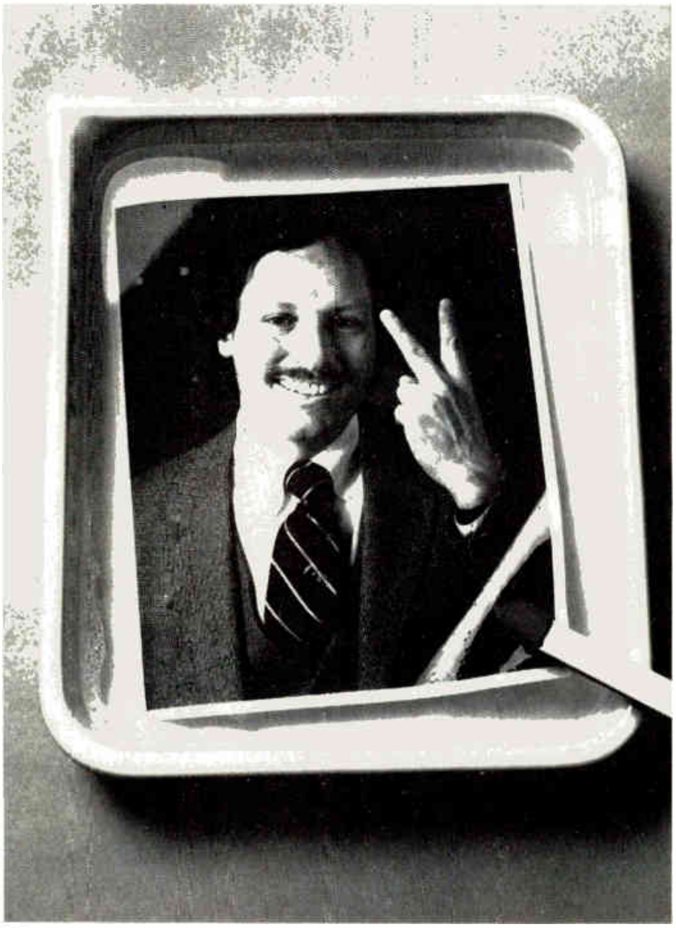

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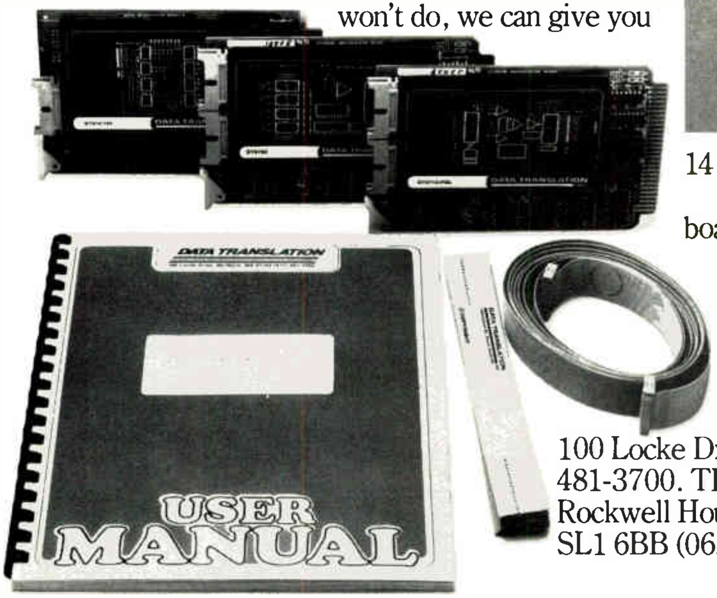

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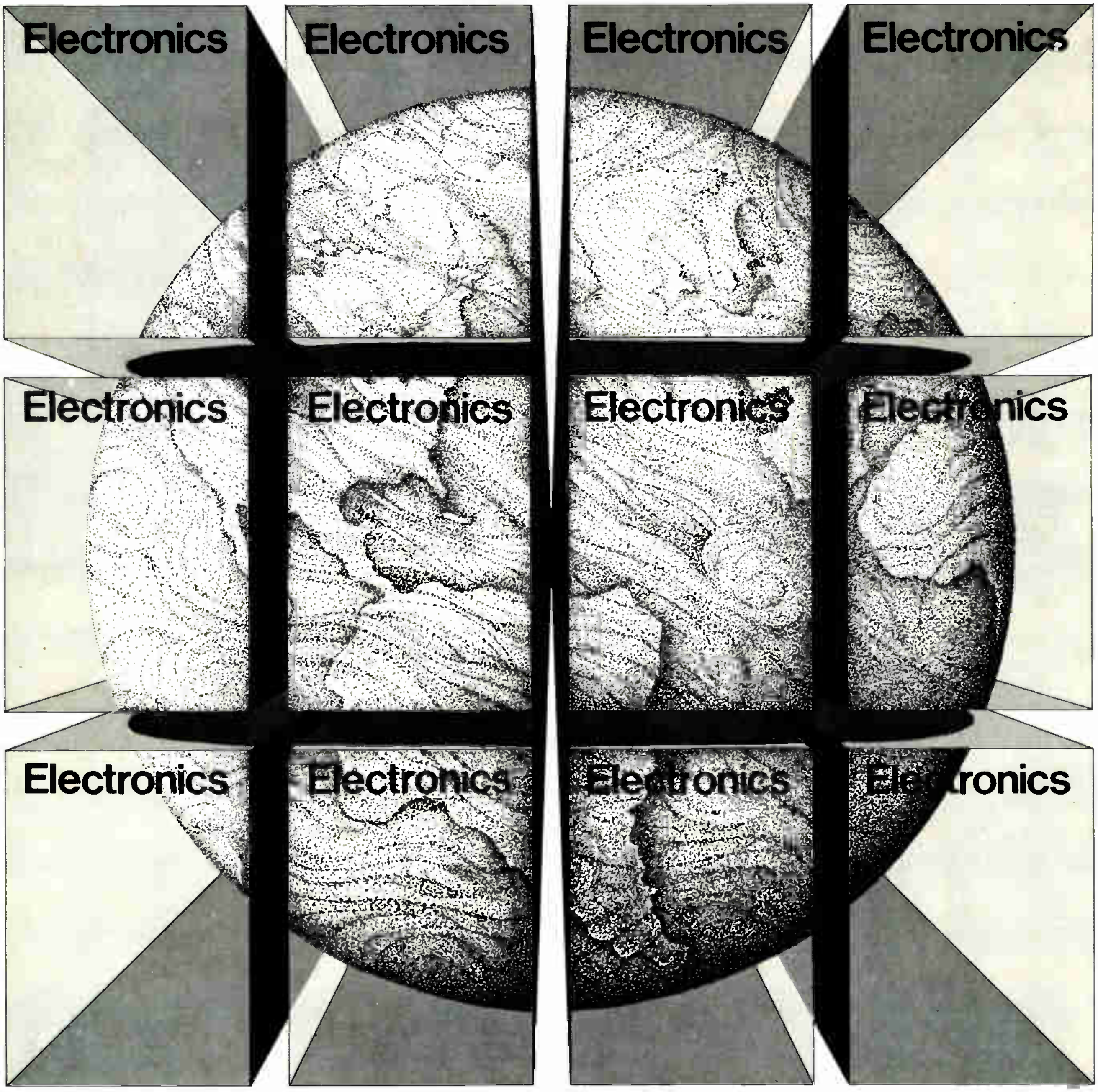

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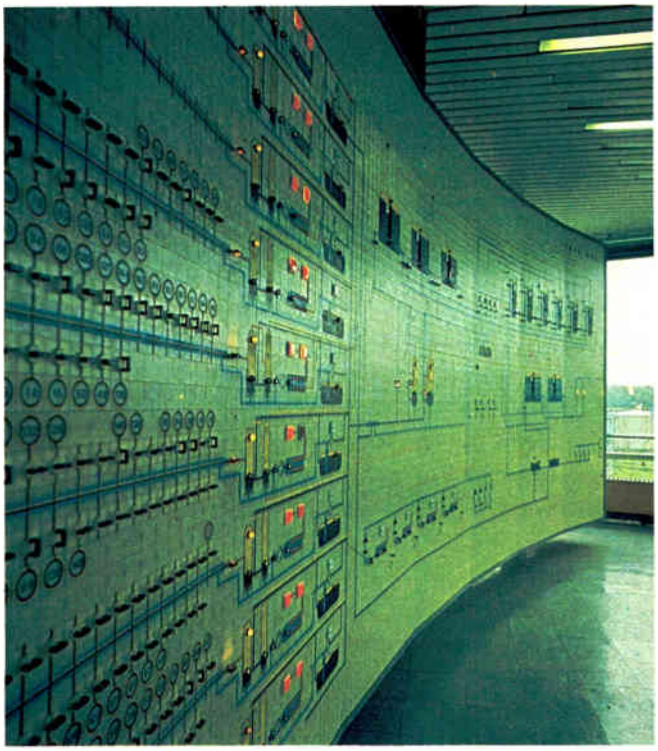

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VLSI test system reduces total test time

264-K bits of RAM back each test-head pin; RAM banks put out 20-MHz patterns through clever use of 5-MHz 64-K RAMs

by Martin Marshall, San Francisco regional bureau

Testers of large-scale integrated circuits waste a lot of time simply shuttling data back and forth—from their computer memory to a high-speed, usually 4-K, local buffer memory, which in turn feeds test patterns into the IC under test. The Teradyne J941 is a new-generation VLSI test system that reduces greatly that source of delay by supporting each pin with 264-K instead of just 4-K of memory.

The trouble with the customary 4-K buffer is that it has to be reloaded 24 times in the course of a test employing over 100,000 vectors. Since each reloading requires over 100 ms of wait states, compared with the 200 μs or so it takes to execute the 4-K pattern, the duty cycle of the machine works out at about 0.2%.

Teradyne's cure—more memory—seems simple but in fact is sophisticated. To keep costs down, the J914's buffer memory mixes a lot of relatively slow and inexpensive 64-K dynamic random-access memory with the very-fast 4-K static RAMs employed in other systems.

"To have used all fast static RAMs would have multiplied the cost of the system by a factor of four or five," asserts Wayne Ponik, product manager for the J941.

Fast static RAMs have a cycle time under 50 ns, which translates into the 20-MHz speed limit of the system. The 64-K dynamic RAMs are much slower, cycling at about 200 ns (5 MHz). The patent-pending trick performed by the J941 is that the data is generated by the pattern generator at the speed of the fast static RAMs, yet is not slowed down by the 64-K dynamic RAMs.

Each test pin receives data alternately from two 4-K RAMs. While the X RAM is delivering data, the Y RAM is being loaded from a bank of dynamic RAMs, the Z RAM. While the Y RAM is delivering data, Z loads X. The Z RAM simultaneously outputs from four 64-K dynamic RAMs, which can be sampled in sequence by the fast static RAMs before a new dynamic RAM cycle is generated.

RAM funnel. Thus the static RAMs act as a funnel to speed up the outputs of the dynamic RAMs. The result, says Ponik, is that the duty cycle is increased by a factor of 10, and test times are reduced by a factor of four or five.

The J941 is capable of handling ICs with up to 48, 72, or 96 pins, depending on the configuration chosen, and can support two fully independent test heads. Each test head in turn may be split into two units with half as many pins each, so long as the twin heads are used to test the same type of part. For certain situations, for instance, the exercising of fast clock pins, two pattern-generating pins can be ORed together to produce a 40-MHz pattern-output rate on a single pin.

The large expansion of the local buffer is accompanied by other advances in the J941. One of these is the M963 computing controller, which is a bit-slice minicomputer with a main memory of 264-K 18-bit words. It has a cathode-ray tube, keyboard, and two 3M DCD 300 tape drives with individual capacities of 4.2 megabytes. A 35-megabyte 8-in. Winchester drive is optional. More than one job can reside simultaneously in the computer, which speeds switching part types.

Voltage swings on the J941 can go from −2 to +9 V, which allows the testing of TTL, some emitter-coupled logic, and some complementary-MOS circuits. Pin-to-pin skewing is targeted to be accurate to within ±1 ns, and the timing resolution of each pin can be set in increments of 100 ps. The system's calibration process adjusts automatically for lead lengths right up to the socket of the device under test.

Instead of trimming a number of potentiometers and creating a data

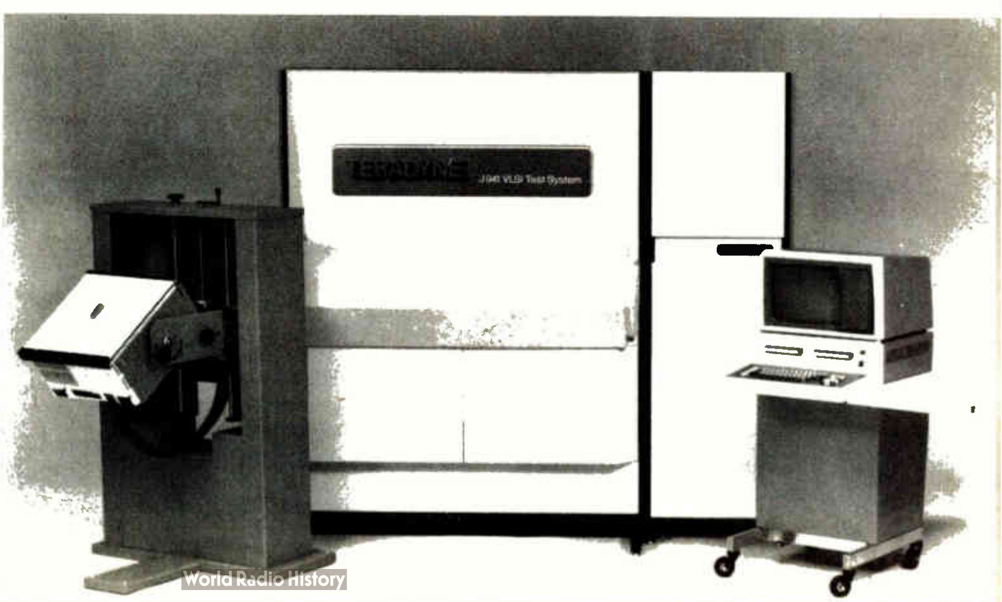

table for post-test numerical corrections, the J941 calibration software actually trims the delays by effecting the automated adjustment of digital-to-analog converters on each pin. "We have over 1,100 converters in there for the tweaking of timing, which we implement through a time-domain reflectometry technique," points out Ponik.

Clocking on the J941 is accomplished through a clock with 16 totally independent phases, plus a period phase, an input/output switching phase, and a pin-multiplexing phase. What distinguishes the 941 test system is that it allows any pin to select any of 256 timing values on the fly. As a result, it is possible also to demultiplex on the fly and to continue on to other tests without waiting, and so forth.

Test-vector sources. In the software arena, Teradyne has recognized with the J941 that a test system is part of a larger process that includes the generation of test vectors by a computer-aided–design or –simulation program. To access these test vectors, the J941 provides a compatibility link to Digital Equipment Corp.'s PDP-11 and VAX computers. The system also provides a link to Teradyne's own Lasar program for the automatic generation of test vectors.

The translation to the J941 of test vectors from programs other than Lasar may be accomplished with the DEC computers and such translation is the responsibility of the user. The program language of the J941 is Pascal T, a subset of Pascal to which Teradyne has added some hardware-related macrocommands.

Pin loading is done dynamically, with a current load supplied at clock rates and switchable on the fly. Each test head can also be interfaced with an automatic handler.

The price of a typical system will be about $1 million, including the controller, two tape drives, a keyboard, and a CRT, but without a printer or Winchester disk drive. Deliveries will begin next June.

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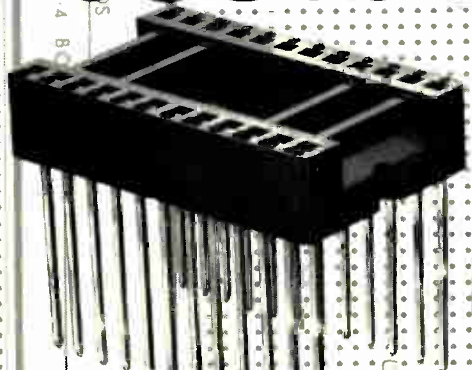

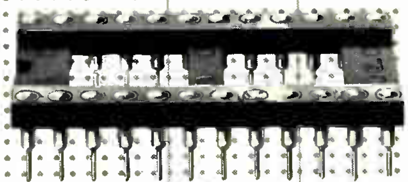

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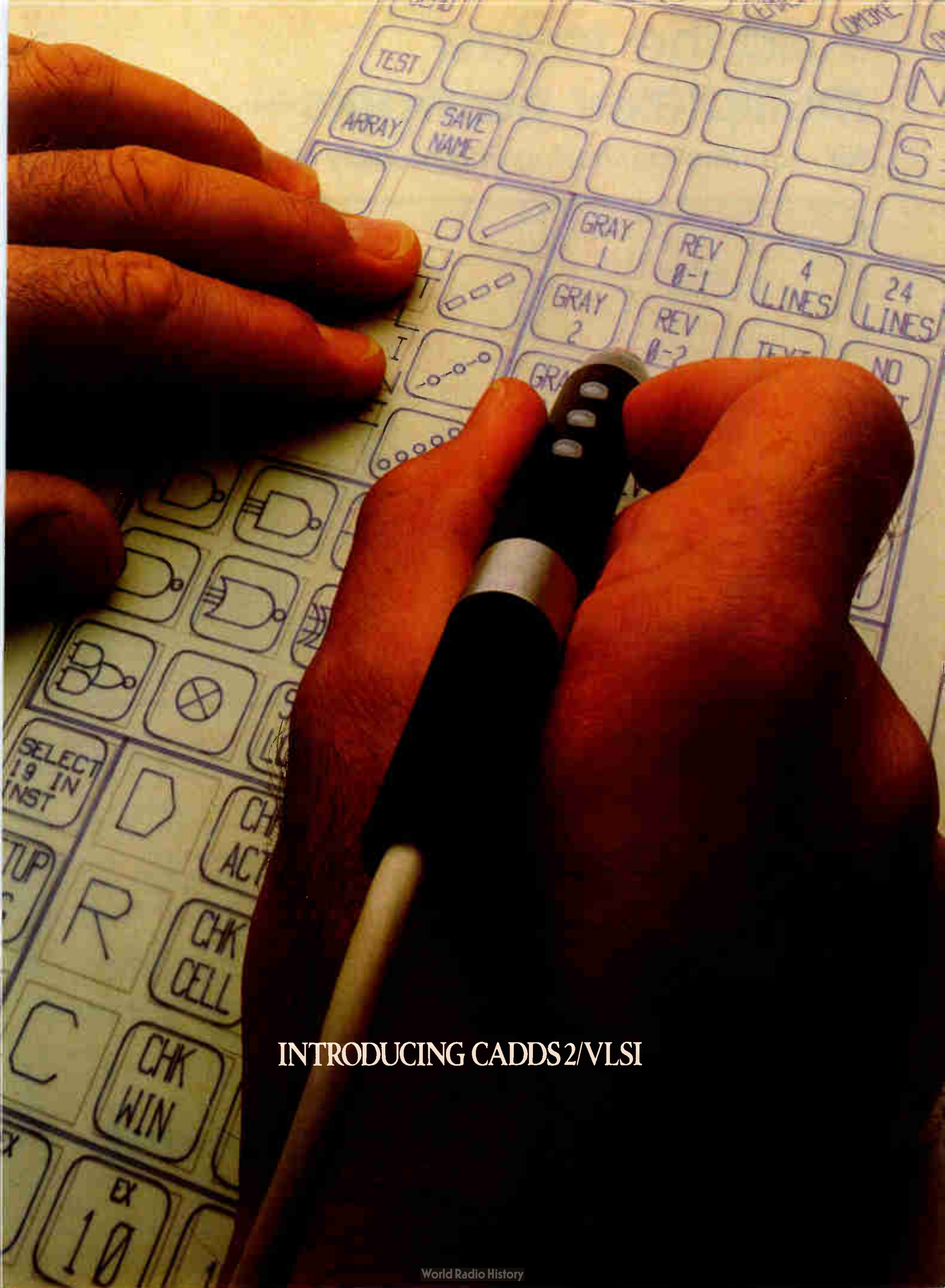
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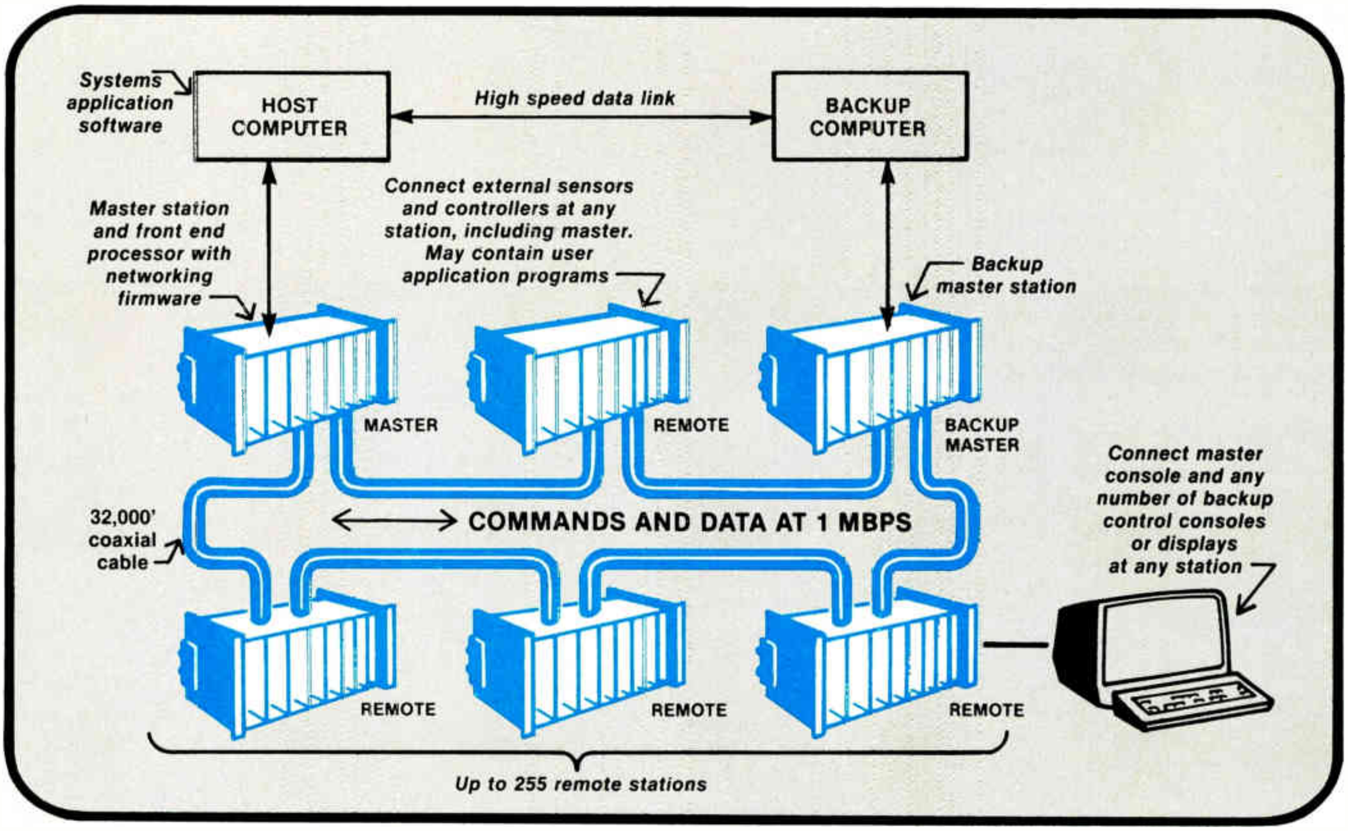

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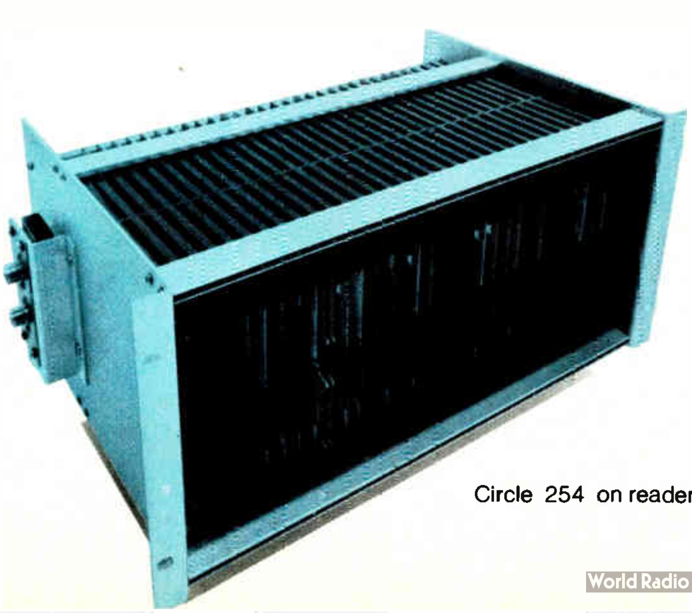

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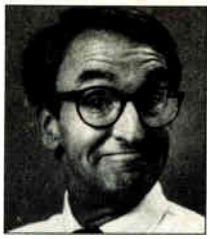

Barney Stevenson just spent two years programming and de-bugging a process control system in assembly code.

Now Barney thinks he deserves some congratulations for his efforts.

Sorry Barney,

NO CIGAR.

Barney Stevenson thought he deserved a pat on the back. As project manager at Smart Widgets, Inc., he had taken on the biggest real-time process control headache of his life. And after 24 months he'd finally succeeded in programming and de-bugging Smart's newest product.

We think Barney missed the boat.

Barney figured the choice was simple. High level languages like Pascal and Fortran could program quickly, but would run too slowly and take up too much memory. Assembly code would take longer to program and de-bug, but was the only answer for real-time applications.

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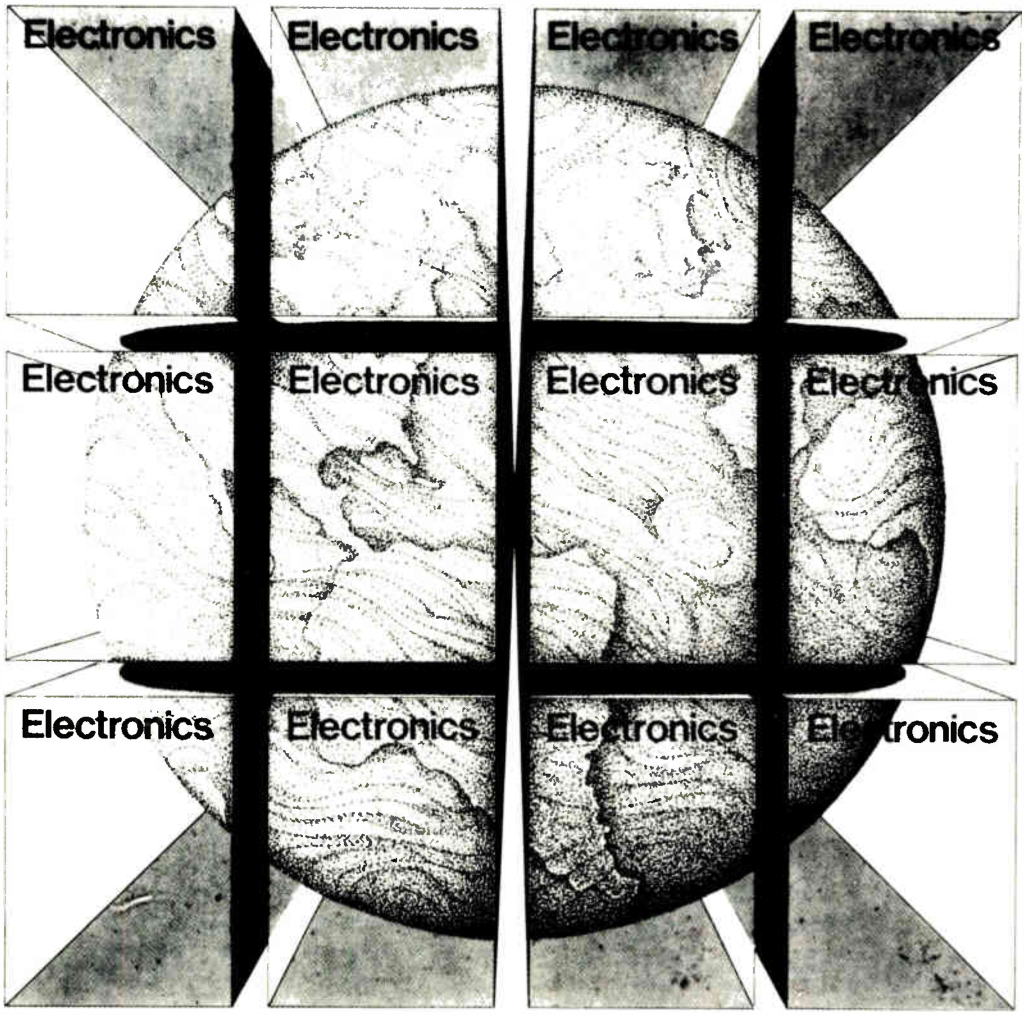

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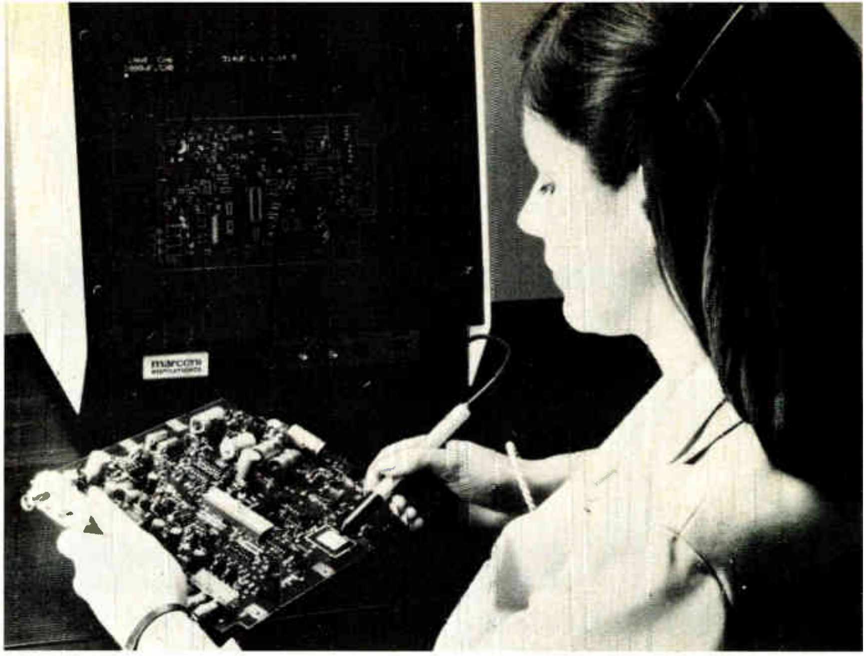
Instruments

Repair station links to tester

Color graphics display guides technician through repairs dictated by test system



Testing printed-circuit boards is now a highly automated operation. But once the computerized test system has worked its wonders identifying component failures or shorts or opens in the printed circuitry, defective boards return to a labor-intensive, error-prone operation—that of board repair. Bringing the computer's advantages to this operation in turn, Britain's Marconi Instruments Ltd. has developed a repair station that guides a technician through a repair sequence. Through the use of color graphics, faults are located and rectified more quickly.

Faulty boards are identified to the repair station through a bar-code reader or a keyed entry. Thus alerted, the LSI-11/34 controller pulls the needed details of the board type together with a failure report from disk. It also calls up a computer-generated image of that board type in which the board edge is depicted in green and components in blue. The first faulty component is highlighted in red, allowing immediate and positive identification. A legend at the top of the screen identifies the component, its correct value and tolerance, and the tested value.

Once the first fault has been rectified, the next is highlighted. Shorted tracks are displayed, one in red, the other in yellow, while other tracks are shown in blue. Recalcitrant boards that are continuously being repaired can easily be eliminated from the loop, as the repair station retains a fault history of every board.

The type 1924 repair station operates in conjunction with Marconi's system 80 in-circuit tester, but Roy Lester, director of systems marketing, anticipates that the station will be linked to competitors' equipment. Ideally, faults located by the test system are sent by data link to the repair station, where board and fault data are stored on disk to await the board's arrival. Other methods of transporting the necessary data can also be used.

The repair station concept represents an elegant means of speeding board repair, but at a ball park figure of around $42,000 for a complete station, it has to earn its keep. Roly Charlton, assistant managing director of Marconi Instruments Ltd. and a dollars-and-cents production man by training, is convinced it will soon pay its way, particularly in a batch-production environment where the test department may be dealing with so many complex board types that repair people may be unfamiliar with many of the boards.

For a system 80 user, that outlay can be reduced to about $20,000 because the 1924 has been designed around Marconi's LSI-11/34-based work station. A computer-graphics package including eight-color monitor and digitizing tablet is added to the station, which can then be used for repair or programming.

The repair station itself involves programming overhead. A computer-graphics image must be generated for every new board entering production. That is a day's work using the menu-driven software, which should be ready in October.

According to Roy Lester, the company has been showing the system to potential customers for 12 months to gauge the response and, as a result of this, color was added to the graphics capability. On a separate display, a fault summary is maintained. Warning that a board has been at the repair station more than three times also appears on this display.

Marconi Instruments, Automatic Test System Division, 292 Gibraltar Dr., Sunnyvale, Calif. 94086 [351]

30-kHz spectrum analyzer computes

Dual-channel unit performs FFTs and other calculations, produces three-axis displays

In instruments, as in cars, one market-winning ploy is to provide as standard facilities that are usually optional. As a newcomer to the spectrum analyzer market, the Solartron Electronic Group Ltd. has adopted just this strategy with its 1200, a dual-channel 30-kHz spectrum analyzer for investigating servo performance, vibration, acoustics, noise and other phenomena.

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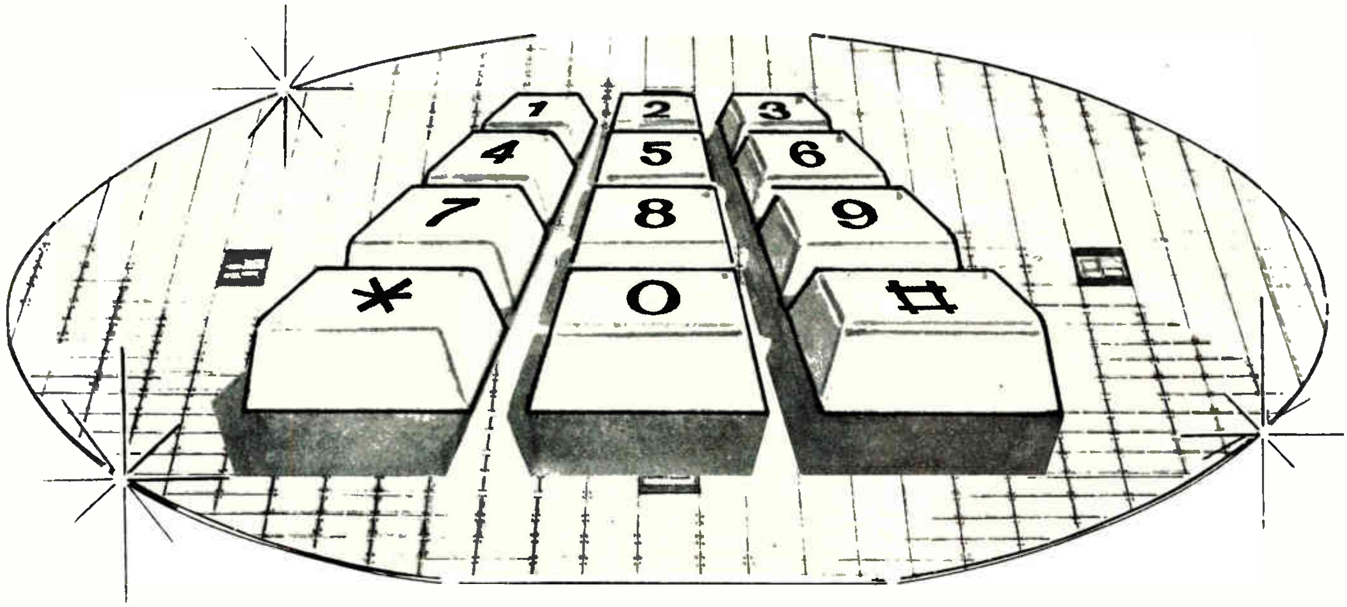

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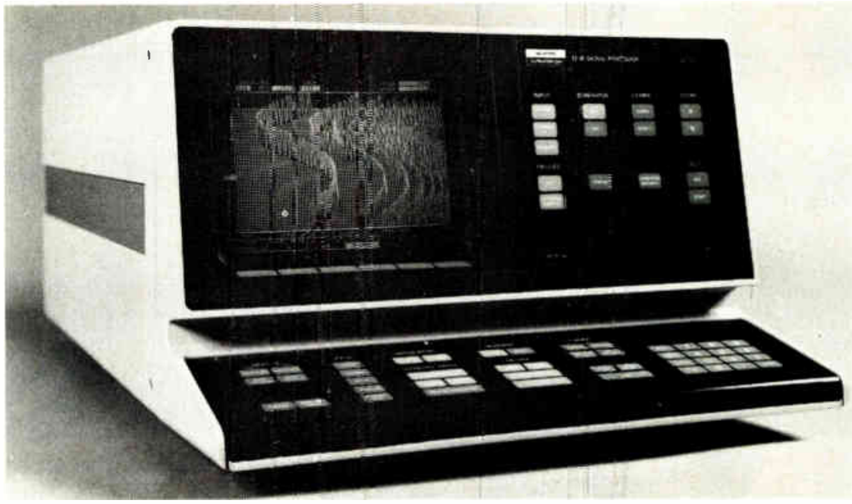


what is called a waterfall display that can show three parameters such as frequency, amplitude, and time in a three-dimensional representation, a zoom facility to improve measurement resolution, a spectrum analysis capability used in the study of echoes, and an IEEE-488 interface.

At the 1200's heart is an array processor, which has two bit-slice arithmetic units coupled to perform a fast Fourier transform using an algorithm developed in the mid-1970s by IBM mathematician Shmuel Winograd. The array processor—which can carry out a complex 16-bit word multiplication in 300 ns—is controlled by a 16-bit microprocessor. A second 16-bit microprocessor drives the display. The total memory capacity of the system is a generous 250-K bytes.

The microprocessors are used to good effect in simplifying the analyzer's operation. Soft keys allow the operator to select what he needs from a menu of options displayed on the 9-in. screen with a minimum of key strokes. Once the measurements and display are set up, the selection can be stored.

The computational package in the 1200 does all the time- and frequency-domain math expected on a high-performance analyzer. Among them in the time domain are impulse response and auto- and cross-correlation, and in the frequency domain, spectrum of a signal synchronized with a trigger, transfer function and coherence, as well as power spectrum and logarithmic, linear, or octave analysis.

Three distinct noise sources are built into the instrument: an impulse function of selectable width, a pseudorandom binary sequence equivalent to stimulation with noise, and a multiple-sine source. The latter puts out 500 sine waves simultaneously. Unlike a pseudorandom signal, this provides a summed noise source that is still periodic and so all the energy can be concentrated in selected frequencies. Also, unwanted frequencies can be pointed to with the cursor and deleted when, for example, that component causes an unduly large resonance.

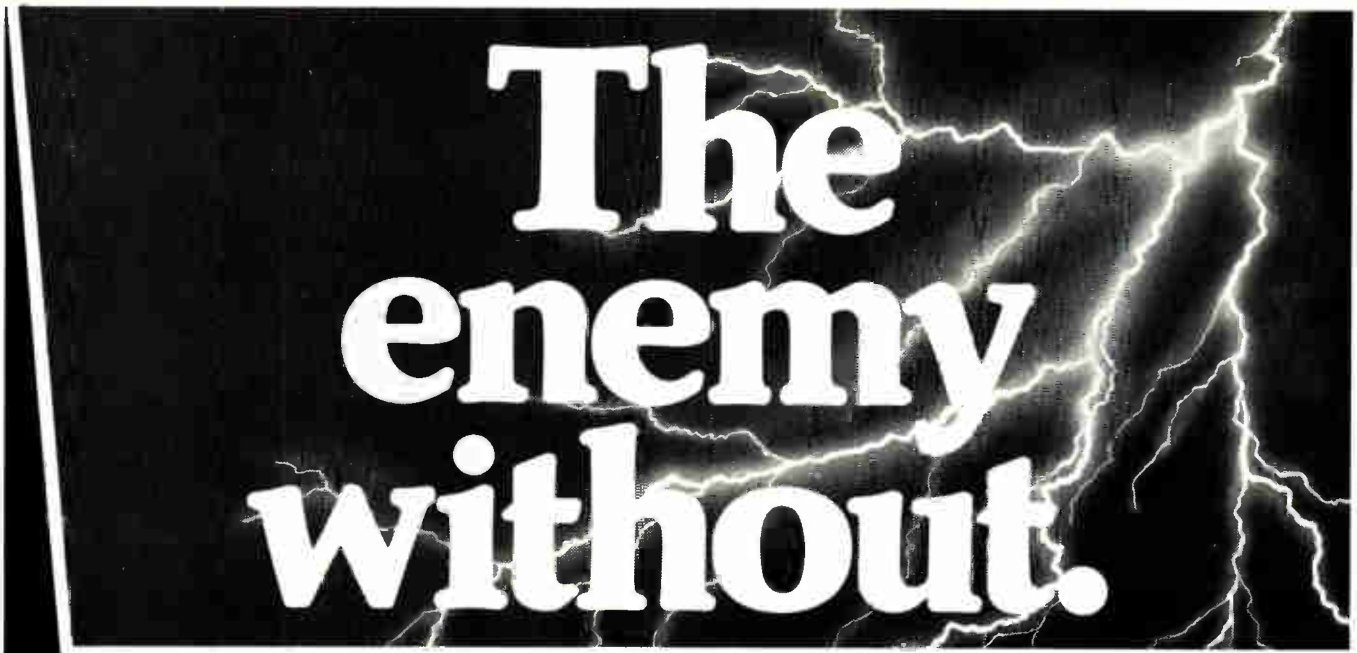
The instrument's display can be operated in split- or single-screen modes. Resolution is 500 lines on each of the two inputs; the display will resolve down to 2-MHz using either of the two zoom facilities.

The 1200's dual differential input channels are autoranging from 10 mV to 300 V with measurement errors as little as 0.04%. The inputs provide a common-mode rejection ratio of over 65 dB.

Sangamo-Weston, 179/172 Sky Park Circle, Suite F, Irvine, Calif. 92714 [352]

50-MHz oscilloscope stores signal for 1 h

Three oscilloscopes feature 50-MHz bandwidth with 2-mV sensitivity on the dual-trace vertical inputs. The



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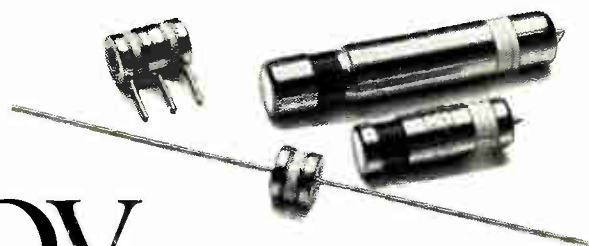

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PM32-15 is a single–time-base instrument, the -17 a dual–time-base unit, and the -19 a dual–time-base scope with storage. All three have automatic trigger-level detection and alternate time-base capabilities, Z modulation, and X-Y displays.

The design of the -19's tube maximizes the light output in either its storage or nonstorage modes—a magnesium oxide storage layer gives it high intensities without burn-in problems. Thanks to an autostore mode and dual-slope triggering, the scope can monitor for transients for over 24 h. A maximum-write mode that increases writing speed from 0.2 divisions/μs to 2 divisions/μs makes it easier to visualize fast–single-shot and low–repetition-rate signals. Storage time is adjustable from 1 min at maximum brightness to 1 h at minimum brightness.

Delivery on any of the scopes takes 10 weeks. The -15 is priced at $1,175 and the -17 sells for $1,495, while the storage model is $4,195.

Philips Test and Measuring Instruments Inc., 85 McKee Dr., Mahwah, N. J. 07430. Phone (201) 529-3800 [353]

Debugger has universal 8-bit emulator adapter card

A new debugger for 16-bit microprocessor systems features real-time in-circuit emulation, software and hardware analysis, and automated allocation of resources.

Model 9516's 24-bit address and 16-bit data-bus structure can be expanded to 32 bits of address and 32 bits of data to support future 32-bit processors. A high-speed static memory operates at 100-ns access time and 150-ns bus cycle time. The 9516 supports multiple in-circuit

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The system also supports 8-bit processors—Zilog's Z80A, Intel's 8080, 8085A, 8041, 8048, 8049, 8050, and Motorola's 6800, 6802, 6801, 6803, and 6809—via a universal adapter card that translates the 9516 bus structure into the bus structure of Millennium's 9508 microsystem emulator. The basic unit is priced at $9,500 with an add-on for cards for the Z8001, Z8002, or 8086 (in minimum and maximum mode). Delivery will begin in January of 1982.

Millennium Systems, 19050 Pruneridge Ave., Cupertino, Calif. 95014. Phone (408) 996-9109 [354]

Modem enables analyzers to talk over phone lines

Biomation's model K102-D logic analyzer, a lower-priced version of the K101-D announced in June [*Electronics*, June 30, 1981, p. 173], has 32 data inputs instead of 48, eight clock inputs instead of 12, and can readily be upgraded to a K101-D model for more power. Available this month, the unit, at $16,900, costs 28% less than the K101-D.

To incorporate the analyzer into a system, the T12 communicator enables two logic analyzers to exchange data over a telephone line and thus service remote digital electronic equipment. The unit combines a 1,200-b/s half-duplex modem, which conditions signals before they enter a telephone line, with a microprocessor-based controller, which manages the interface between an internal modem and the general-purpose interface of the analyzer. The modem is priced at $3,250 and will be available in December.

With the logic analyzer, designers can speed verification, debugging, and integration of Intel 8085-based microprocessor systems using the disassembly module. The unit allows

designers to review software execution in the mnemonics of assembly language instead of translating machine or object code. Available in January, the personality module will be priced at $2,000.

Gould Inc., Biomation Division, 4600 Old Ironsides Dr., Santa Clara, Calif. 95050. Phone (408) 988-6800 [355]

Emulator has 8-MHz speed for Z8000, 68000 processors

The Hewlett-Packard model 64000 logic development system has been extended to include emulation of the 8086/8088, Z8001/Z8002, and 68000 16-bit microprocessors. In addition, Pascal/64000 compilers for the 8086/8088 and Z8001/Z8002 and 8-bit 6809 have been added as options. All can be used with existing logic development systems.

The operating speeds of the emulators, without inserting wait states, are 6 MHz for the Z8000 processors, 8 MHz for the 68000, and 8 MHz and 5 MHz respectively for the 8086 and 8088 processors. Each 16-bit processor emulator has an operating mode that is functionally transparent to the target system. Up to 128-K bytes of emulation memory can be ordered separately. The HP three-pass compilation process runs at speeds of 300

to 700 lines/min. Pascal/64000 modules can be linked with assembler language modules.

Models 64220A 8086/8088, 64230A Z8001/Z8002, and 64240A 68000 emulator systems with memory are priced at $7,900 to $23,500. The price of the models 64814A 8086 and 64816A Z8000 Pascal compilers is $3,000, and of the 64813A 6809 compiler, $2,000. All deliveries take 8 to 12 weeks.

Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, Calif. 94304. Phone (415) 857-1501 [356]

0.2-Hz-to-200-kHz amplifier is computer-controllable

With facilities for full computer control, the model 5205 lock-in amplifier can automatically set its sensitivity range, phase controls, offset voltages, and full-scale normalized voltages. Its full-scale sensitivities range from 100 nV to 5 V root mean square, and its operating frequencies span 0.2 Hz to 200 kHz.

With the optional IEEE-488 interface card, the 5205 can talk or listen to other devices on the bus and be totally programmed by a controller. The processing, display modes, and commands associated with all 13 front-panel push buttons can be controlled remotely.

Both digital and analog readouts augment the 5205 in measuring the intensities and phase shifts of weak signals. A four-digit display presents measurement results in volts, decibels, and degrees. Parameters such as internal oscillator frequency, dc output suppression, and phase-shifter settings can also be displayed.

The 5205 is designed from both heterodyne and Synchro-Het technologies that, among other capabilities, reduce to three the number of band-determining cards needed to cover the 0.2-Hz to 200-kHz range. With one band-determining card, the 5205 is priced at $5,795, with delivery in 30 to 60 days.

EG&G Princeton Applied Research, P. O. Box 2565, Princeton, N. J. 08540. Phone (609) 452-2111 [357]

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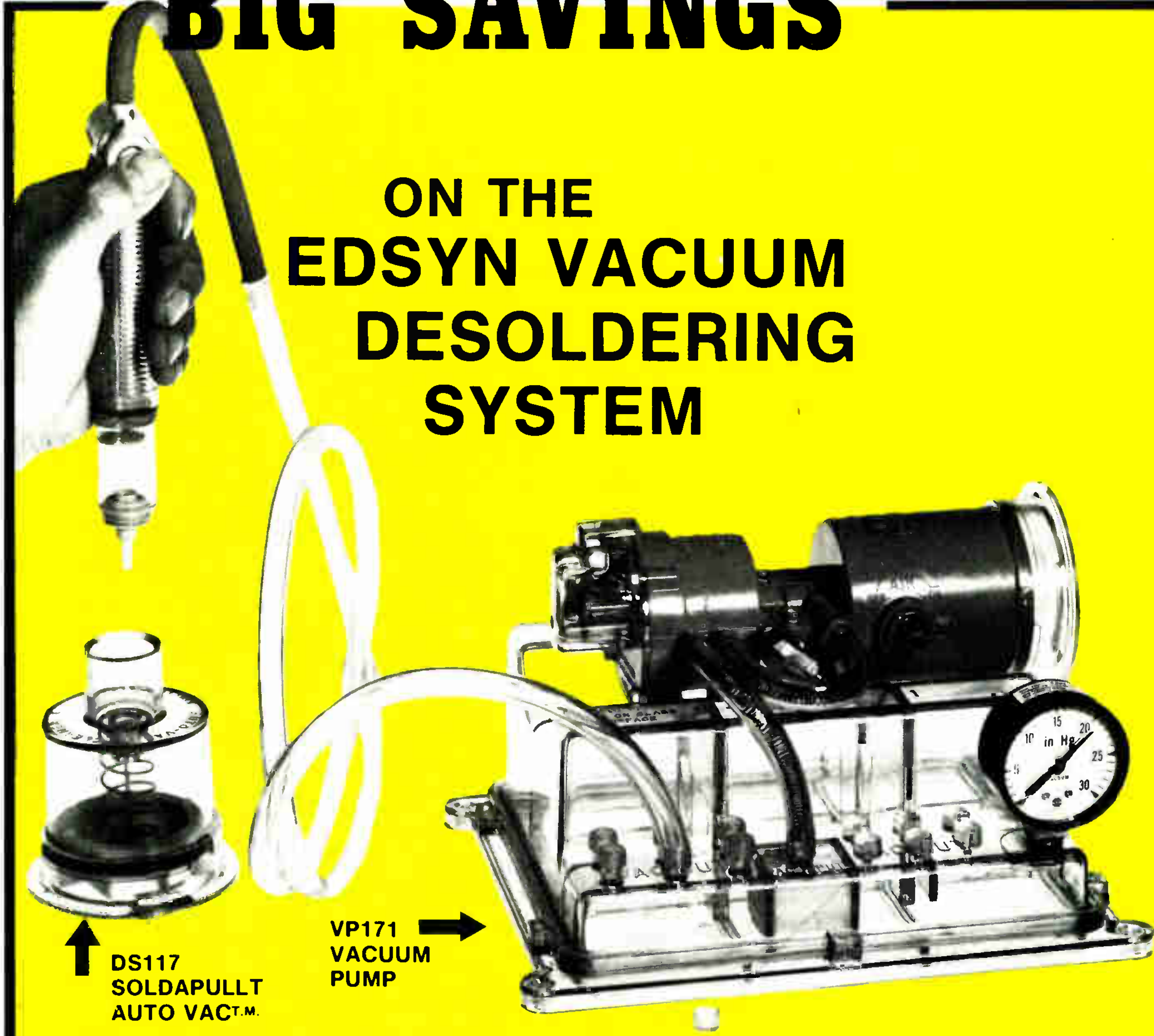

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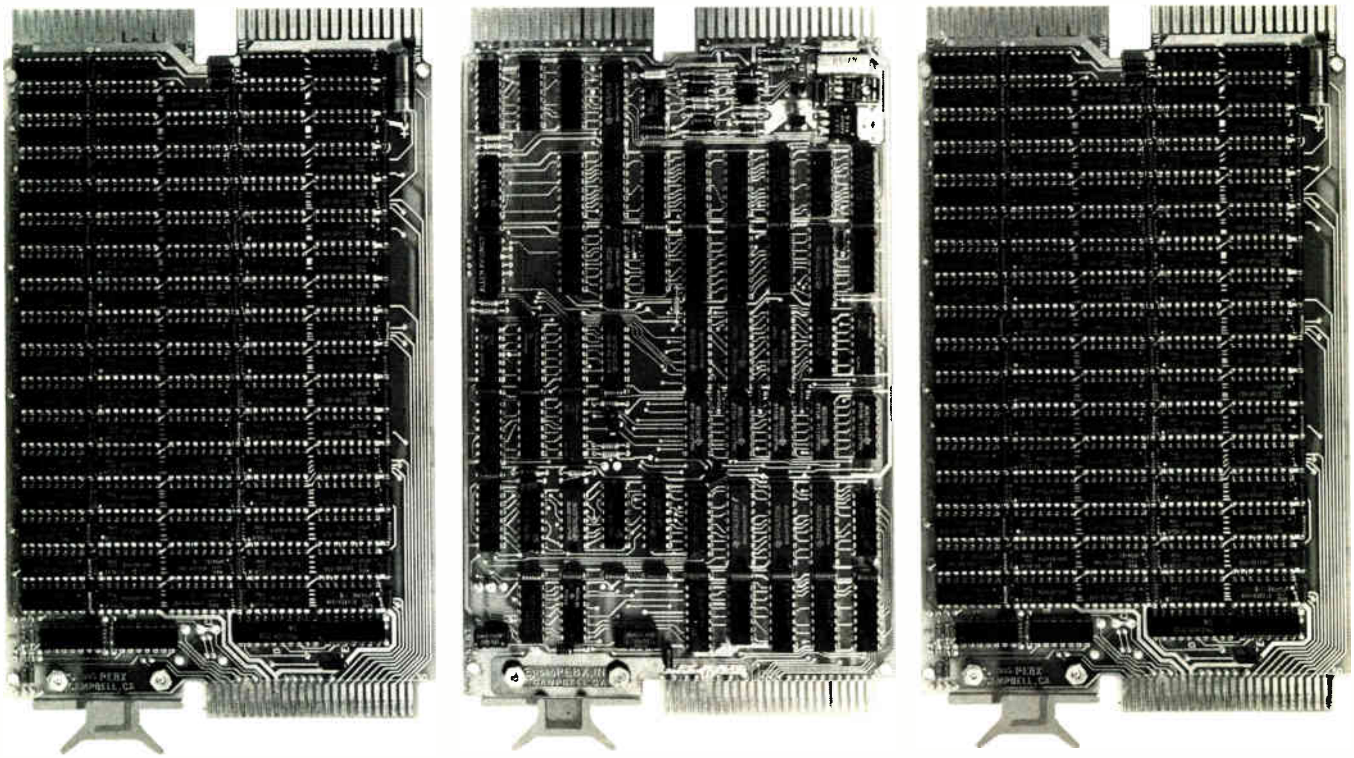

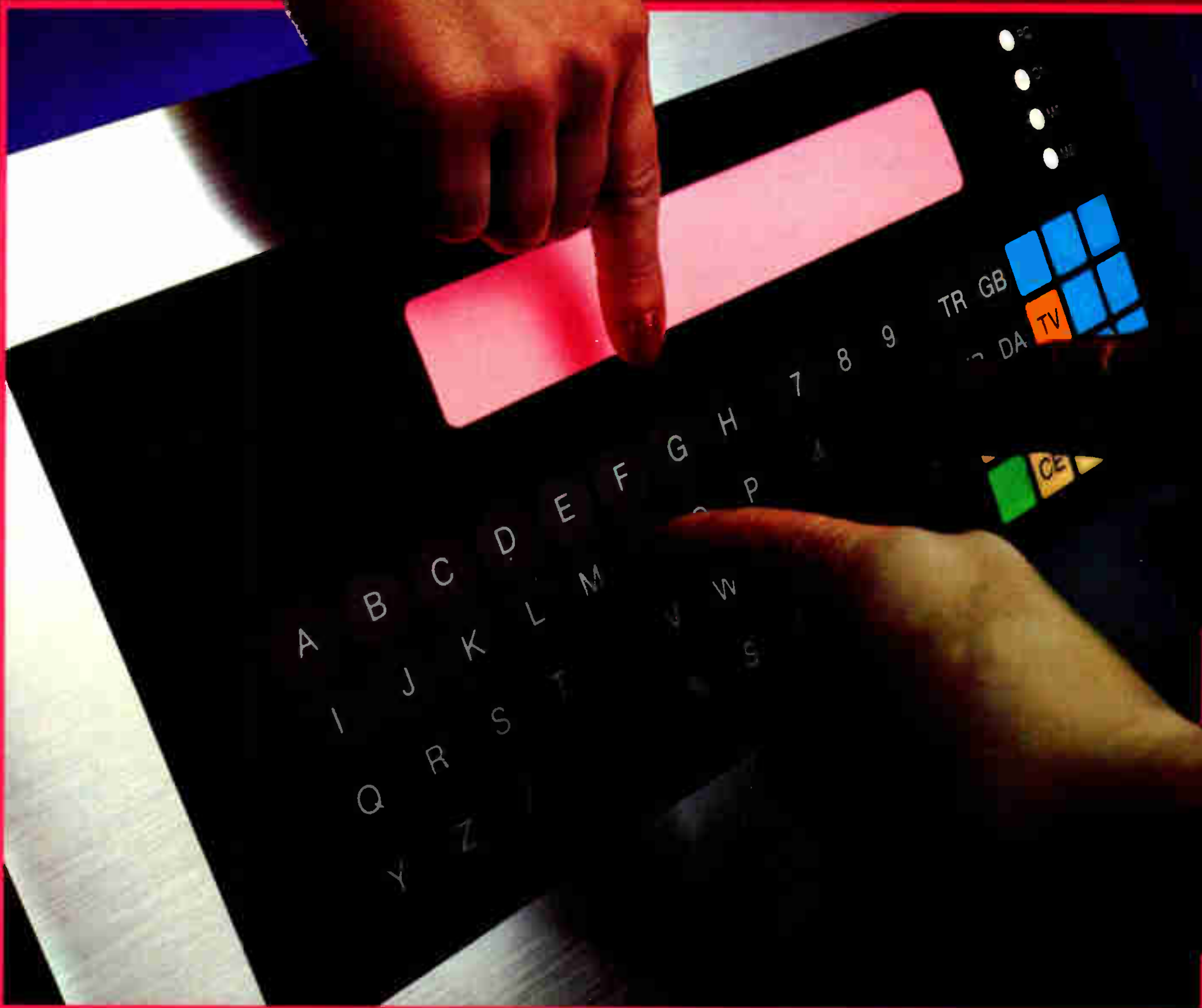

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Circle 23 on reader service card

Computers & peripherals

Graphics front end saves host's time

8086-based front-end processor cuts communication between host and station

Adding graphics work stations to an existing host computer, due to the considerable computing power required to operate the remote sites, cuts rapidly into the host's capacity for other tasks. Megatek Corp.'s Local Intelligent Front-End processor removes much of the processing load from the host, giving the designer quicker response and more flexibility without weighing down the host.

Life is an 8086-based three-board set that can be used in conjunction with the company's Whizzard 7200 series of graphics systems. The set consists of the processor board, an interface card, and a random-access-memory card, with all three fitting into the 7200 backplane.

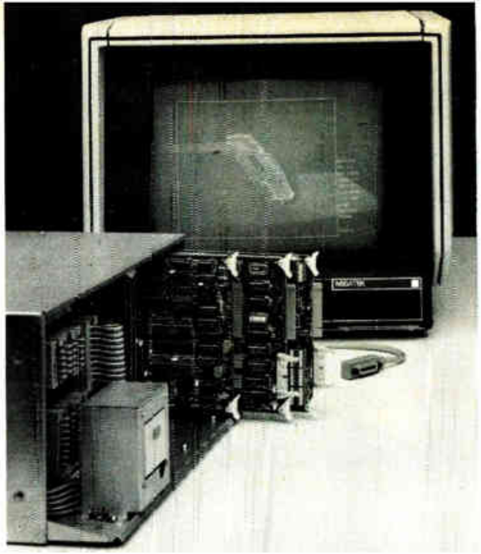
Life lets users develop code at individual work stations and permits the downloading of programs from the host for use at remote sites. "We want to be able to do as much as possible in a remote atmosphere," says Dale Roark, director of product marketing. Towards that end, Megatek decided to offer the front-end processor for general use rather than to offer hardware options dedicated to specific functions. This gives users more flexibility by letting them develop their own programs.

Key functions that can be handled by Life include context switching, peripheral interactions such as attaching a joystick to the station, and nested menu seletion. Using a telescoping menu format, users can look at an overall menu and then examine subsets until the final selection is made without interacting with the host until the program is to be offloaded, cutting communications time dramatically.

Each Life interface supports two RS-232-C ports; parallel ports are available as options. With the parallel port, graphics stations may be located up to 1,000 feet from the host using bus extenders. Using these ports, the user can program directly with the host, using the system like a dumb terminal.

The firm's standard Wand software, used on the 7200, is currently being rewritten to split the tasks between the host and the Life processor. By offloading the software from the host, the company achieved a substantial increase in performance time. When the DSYS diagnostic program was revised to run on the 8086, the firm found various segments of the program ran from 1.5 to 3 times faster than when handled by the host. Roark expects many of the other packages to show similar speed gains when testing is done.

Life groups related data into entities using an associated memory approach, which lets a user call each group by name when starting to work with it. As changes are required, the user simply enters the name of the group and adds or deletes as necessary.



The memory board uses 64-K RAMs, which were selected for their savings in real estate and because pricing has dropped enough to make their use feasible, Roark says. The board comes in 128-, 256-, or 512-K versions. The interface board carries graphics and peripheral buses. The processor board includes the interrupt-controlled 8086, a timer, and universal asynchronous receiver-transmitters. Support from Intel and the number of cross-assemblers and cross-compilers available were key factors in the selection of the 8086.

The basic Life package sells for $6,000 in single quantities. Deliveries will begin in early 1982.

Megatek Corp., 3931 Sorrento Valley Blvd., San Diego, Calif. 92121. Phone (217) 455-5590 [361]

Chip interfaces thin-film heads

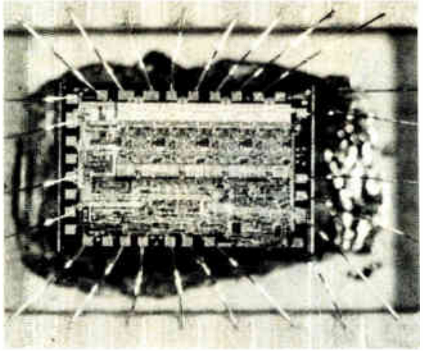
High-speed read-write IC for use in hard-disk drives emulates IBM counterpart

The advent of thin-film head technology popularized by IBM's 3370, -75, and -80 high-capacity disk drives has spawned the need for improved integrated circuits to handle the increased read-write rates as compared with conventional ferrite heads. To meet this need, a group of manufacturers of IBM-compatible drives contracted with Silicon Systems Inc., a custom IC designer, to develop a read-write IC that offered them performance specifications similar to the IBM product.

The resultant device, the SSI 114, is now completed and will be available during the first quarter of 1982. Along with the chip, the company is introducing a companion amplifier, the SSI 116, which boosts the signal coming from the servo head—a weaker one than comparable signals from ferrite heads. Amplifiers on the 114 handle the data-head signals.

In the past, the firm developed read-write chips that emulated those used on IBM's 3340 and -50 drives. Those products, the SSI 104 and 105, currently hold about 80% of the market, according to Roger Budris, marketing manager for computer products.

The 87-by-129-mil chip comes in a 24-pin ceramic flat pack. The unit,



which has TTL-compatible control inputs, performs what is said to be a full emulation of the IBM component, except for a variation in handling the trimming. Silicon Systems uses an external resistor to set the write-current magnitude, with the voltage across that resistor internally trimmed to within 3%. IBM uses a laser trimmer to fix the write-current level, maintains the company.

The IC has bidirectional four-channel multiplexing providing four read and four write channels, one for each of the heads generally mounted on an arm. The write mode is safeguarded by fault-detection circuits that closely monitor the data encoding. Some fault detection is also provided for the read mode.

In the write mode, the 114 will handle up to 110 mA per output. Its head-current switching time is typically 10 ns, much faster than the 45 to 50 ns currently found on the older 3340 drives. The shorted head current transition time is a maximum of 13 ns.

In the read mode, the chip has a voltage gain of about 120. The 3-dB bandwidth is 45 MHz. Input noise is a maximum of 1 nV/Hz$^{1/2}$, fulfilling the low noise level required by the thin-film head.

The 114's sister chip, the 116, is a two-stage differential servo-head amplifier packaged in an 8-pin plastic dual in-line package. This low-noise amplifier has nominal gain of 240 to 250.

Silicon Systems Inc., 14351 Myford Rd., Austin, Calif. 92680. Phone (714) 731-7110 [362]

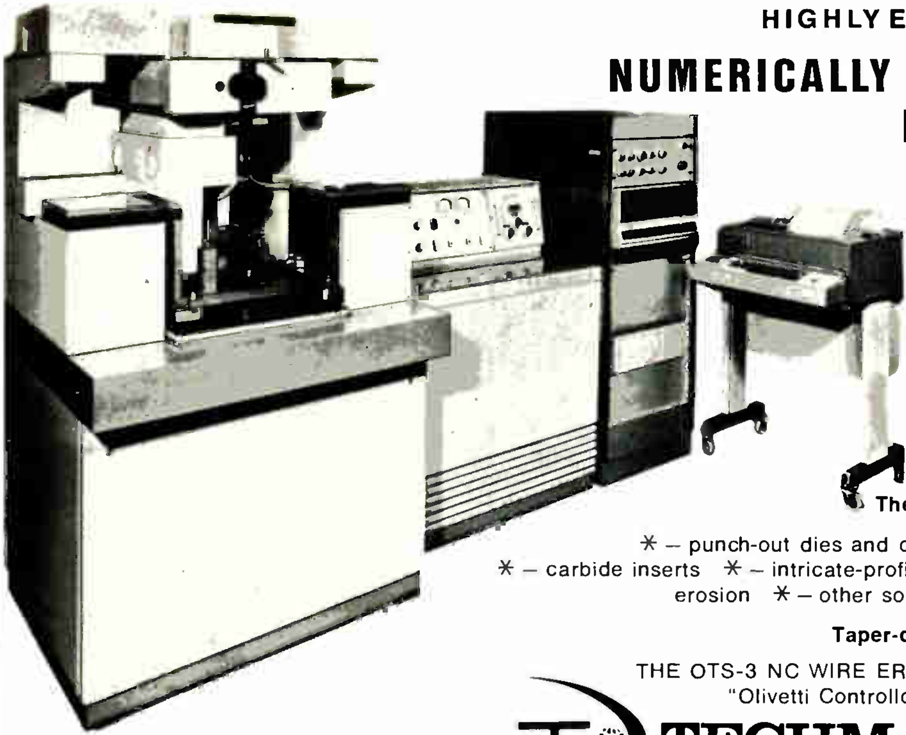
Unit puts CRT on closed-circuit TV

Hood-mounted video camera adapts to numerous screens, sends image via coaxial cable

The GDS-2000 remote terminal display is a video system that transmits images from cathode-ray tube terminals to remotely located video monitors without requiring a direct connection to the terminal's circuitry. Able to transmit images from radar displays and medical instrumentation, as well as from standard CRTs, the system addresses applications in training classrooms, seminars and remote monitoring, maintains its manufacturer, Graphic Display Systems Ltd. of Cambridge, England.

The system focuses a video camera on the image displayed on a CRT. The camera is mounted in an optical hood, which through a variety of bezel adapters can fit terminals from such manufacturers as Tektronix Inc., Digital Equipment Corp., IBM Corp., Hewlett-Packard Co., Imlac Corp., and Vector General Inc. The hood is hinged, permitting a user to swing it aside and view the terminal screen directly. The terminal keyboard remains accessible when the hood is in place; an optional extension keyboard allows remote, on-line access to the terminal.

Images picked up by the GDS-2000's camera undergo conventional video processing and are transmitted over coaxial cable to remote monitors. The basic GDS-2000 shows CRT images with no modification; a second model, the GDS-2000A, uses



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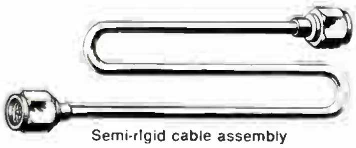

Semi-rigid cable assembly

ASU COMPONENTS Ltd.
A subsidiary of the Swiss ASUAG group

P.O.Box 297, 1860 Aigle, Switzerland
Tel. 025 - 26 55 33, Telex 456 138

Circle 30 on reader service card

a zoom lens on the camera to yield variable image magnification to 2.5 times. A third model, the GSDS-2000PTZ, magnifies images up to 6 times, and adds pan and tilt to the zoom feature. All three functions can be remotely controlled.

The GDS-2000 costs from $2,920 to $3,460 depending on the type of CRT terminal with which it will work. Prices range from $3,250 to $3,625 for the GDS-2000A, and from $8,920 to $9,710 for the GDS-2000PTZ.

Delivery takes 30 days.

Graphic Display Systems Ltd., 76 Hemingford Rd., Cambridge CB1 3BZ, England. Phone Madingley (0954) 210486 [368]

Jodan Technology, P. O. Box 362, Lexington, Mass. 02173. Phone (617) 862-2354 [369]

161-megabyte disk drive has 50-ms average seek time

Century Data Systems' M160 Marksman Winchester disk drive doubles the capacity of previous Winchester offerings by increasing the track density to 712 tracks/in. and the bit density to 10,000 b/in. Its total storage capacity is 161 megabytes. The M160 has a data-transfer rate of 1,280 kb/s and an average seek time of 50 ms.

The M160 features a composite head that is more durable and provides less crosstalk than monolithic type ferrite heads.

Engineering pilot models will be available in the fourth quarter of 1981, with production quantities available in the second quarter of 1982. The M160 is priced at $4,050 each.

Century Data Systems, 1270 North Kraemer Blvd., P. O. Box 3056, Anaheim, Calif. 92803. Phone (714) 999-2660 [363]

CAD-system display has 1,024-by-1,024 resolution

The Design Engineering Workstation for computer-aided design and manufacturing combines three fun-

The only 100 MHz scope that gives you three vertical input channels... Kikusui just had to do it better.

Three vertical input channels, two trigger views and an "add/differential" trace. That's what you get with KIC's new 100 MHz KIK-scope. Use the third channel as an extra data channel, as an additional signal in an x-y display, or for a host of other applications. There's almost no limit to the versatility that this third channel adds to your scope. And, it's included at no extra cost in our new Model 6100.

The Model 6100 is comparable to TEK's Model 465B and HP's 1742 but displays more traces (six compared with three), and offers more screen brightness, more flexibility, greater simplicity of operation and a two-year warranty that substantially reduces the second year cost of ownership. The Model 6100 also features an auto-dynamic focus circuit for clear, sharp pictures and a metal housing that minimizes RFI interference.

Now for the surprising news: Despite all the extra features, the 6100 costs less than either the TEK or HP scopes.

For versatility of operation, an alternate trigger permits viewing a very wide range of non-synchronous signals. For simplicity of operation, a level-lock on the trigger level control for both A and B channels activates a peak-to-peak detector that automatically sets trigger level and triggers without operator intervention.

Rugged and compact, the 6100 is completely modular. Like all KIK-scopes, the construction is on plug-in boards that are supported by a board swap-out program that assures fast maintenance turn-around and minimum down-time.

And, just to give you a little added assurance, your KIK-scope comes with a 30-day "satisfaction-or-your-money-back" guarantee.

This new 100 MHz KIK-scope along with eleven other models for engineering labs, field service and production line applications, is described in our new brochure. Write for it. It's free.

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Carson, California 90746
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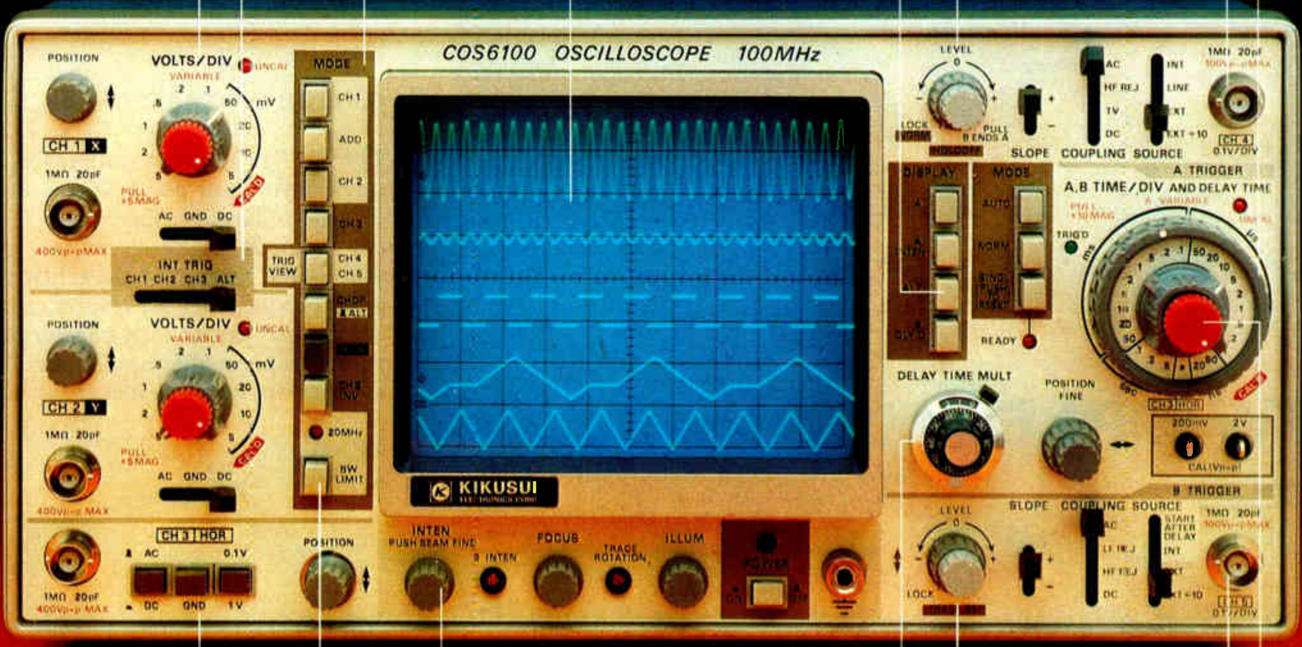


Circle 34 on reader service card

Circle 36 on reader service card

damental building blocks: fast, high-resolution graphics; processing power for the application; and graphics and system software.

The DEW can function in one of three modes: as a stand-alone graphics work station with its own disks, printer, plotter, and other peripherals; as a front-end intelligent graphics terminal linked to a mainframe computer; or as an element of a local loop with other DEWs.

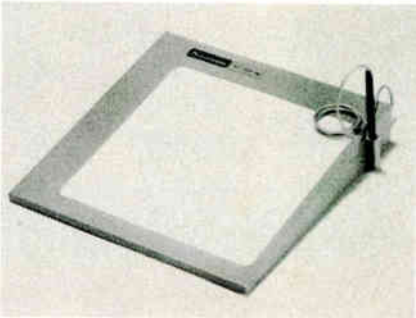
The graphics employs a 16-bit bipolar bit-slice processor to generate the display bit maps for screen memory. It has a 200-ns instruction time and can write picture elements to the terminal at a nominal rate of 40 million pixels/s.

The graphics screen itself has a 1,024-by-1,024-bit resolution, giving 1 million pixels per display. Fully configured, the system can display 256 colors simultaneously from a palette of millions. Depending on configurations and peripheral options, each station will sell at a price ranging from $25,000 to $50,000 in Canadian dollars.

Orcatech Inc., 2680 Queensview Dr., Ottawa, Ont., Canada K2B 8H6. Phone (613) 820-9602 [364]

Desktop digitizer controls computer graphics

The Bit Pat 10 desktop digitizer, for small business or personal computers or where large-surface tablets are not required, can convert the location on the surface of the tablet into digital coordinates for computer processing and can directly control computer graphics displays. It may be used for applications like cursor con-



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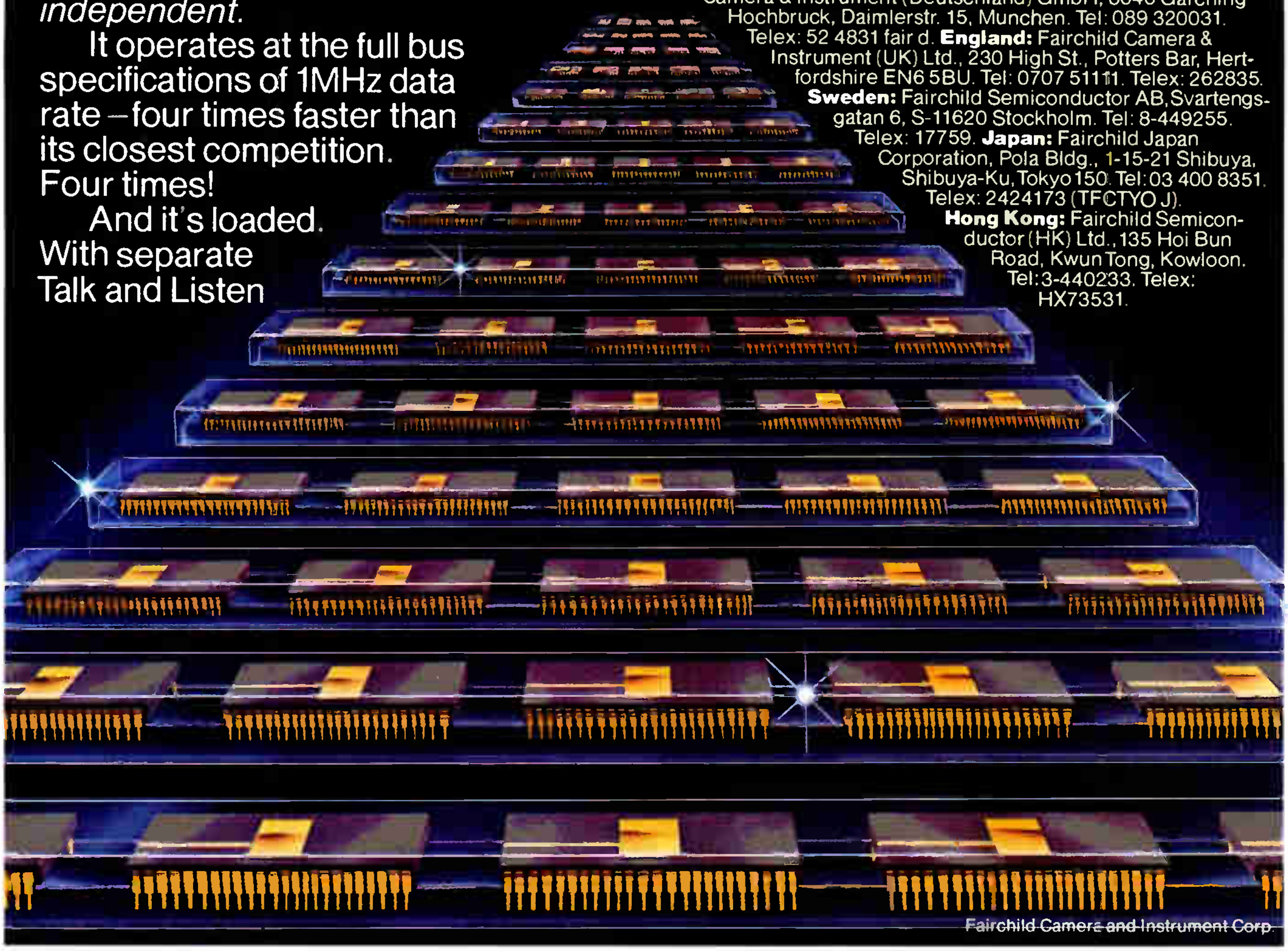
For more information, contact your local Fairchild office.

France: Fairchild Camera & Instrument S.A., 121 Ave d'Italie, 75013 Paris. Tel: 331 584 55 66. Telex: 0042 200614. **Italy:** Fairchild Semiconduttori S.P.A. Viale Corsica 7, 20133 Milano. Tel: 02 296001-5. Telex: 843-330522. **Germany:** Fairchild Camera & Instrument (Deutschland) GmbH, 8046 Garching Hochbruck, Daimlerstr. 15, Munchen. Tel: 089 320031. Telex: 52 4831 fair d. **England:** Fairchild Camera & Instrument (UK) Ltd., 230 High St., Potters Bar, Hertfordshire EN6 5BU. Tel: 0707 51111. Telex: 262835. **Sweden:** Fairchild Semiconductor AB, Svartengsgatan 6, S-11620 Stockholm. Tel: 8-449255. Telex: 17759. **Japan:** Fairchild Japan Corporation, Pola Bldg., 1-15-21 Shibuya, Shibuya-Ku, Tokyo 150. Tel: 03 400 8351. Telex: 2424173 (TFCTYO J). **Hong Kong:** Fairchild Semiconductor (HK) Ltd., 135 Hoi Bun Road, Kwun Tong, Kowloon. Tel: 3-440233. Telex: HX73531.



If you want the fastest bus, we've got it made.

Circle 39 on reader service card

trol, business data entry, and traditional graphic-information entry. The Bit Pat 10 has an 11-in.-square active surface.

The RS-232-C and an 8-bit parallel interface are available. The digitizer sells for $990 plus $95 for a power supply and $130 for the interface cable. Delivery takes six to eight weeks.

Summagraphics Corp., 35 Brentwood Ave., Fairfield, Conn. 06430. Phone (203) 384-1344 [365]

Low-cost printer uses hubless printwheels

The model 620 daisywheel receive-only printer is controlled with a Motorola 6803 and Intel 8041 microprocessor and features plastic drop-in print wheels. The print wheel is electrically aligned with a system that positions the wheel after it has been loosely inserted into an envelope-like opening.

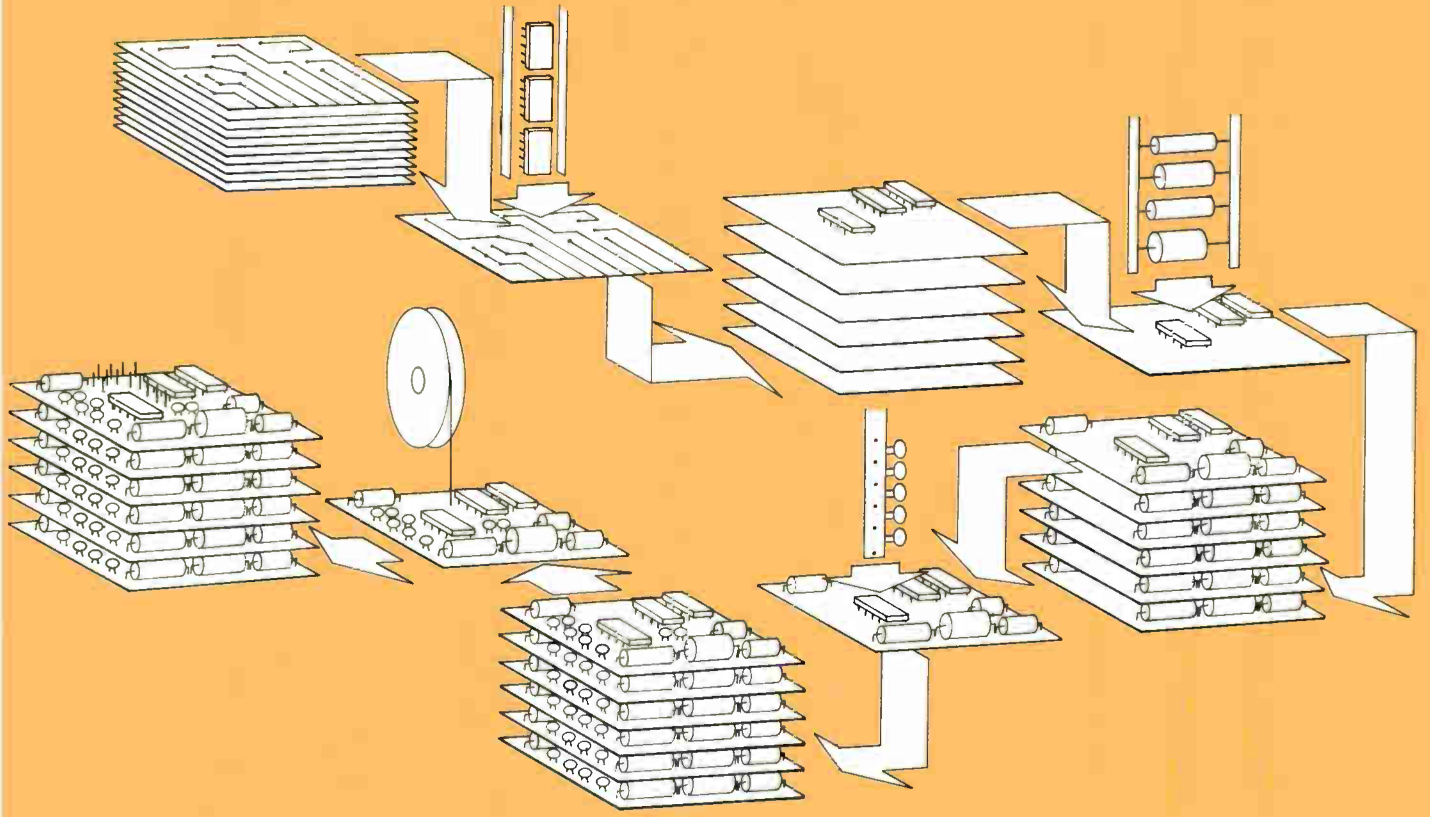
The 620 has no notches, hubs, or alignment requirements associated with its 98-character print wheels. The 620 daisywheels produce more than 10 million characters before requiring a replacement.

With 10-pitch print wheels, the 620 can print 132 characters/line at

a rate of 25 c/s. The printer also features a long-life ribbon cartridge system providing ink for 450,000 characters, which remains in place during print wheel changes. In addition, the unit has a 512-character buffer, correspondence-quality output, and a stepper-motor design that can handle subscripts, superscripts, and bidirectional printing.

The under-$2,000 printer is ex-

PASS-THRU™ unlocks hidden productivity in board assembly systems.



Automatic machines shouldn't be kept waiting when they could be inserting components into circuit boards. This is why Universal Instruments developed its new Pass-Thru board-handling system. Pass-Thru takes only a few seconds to feed a fresh board into an automatic component inserter while it is simultaneously pulling a completed board out of the machine's work area. It does this smoothly and gently, board after board, hour after hour, without fatigue and without error.

Pass-Thru feeds individual boards from a stack of blank or partially assembled boards and deposits finished boards in special compartmental magazines. This way, many boards can be carried in a single, protected load, ready for wave soldering or for automatic feed into another

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Circle 42 on reader service card

pected to have a 2,500-hour power-on mean time between failures in typical office use. Deliveries will begin this January.

Diablo Systems Inc., 24500 Industrial Blvd., Hayward, Calif. 94545. Phone (415) 786-5207 [366]

24-user minicomputer runs under Unix, programmed in C

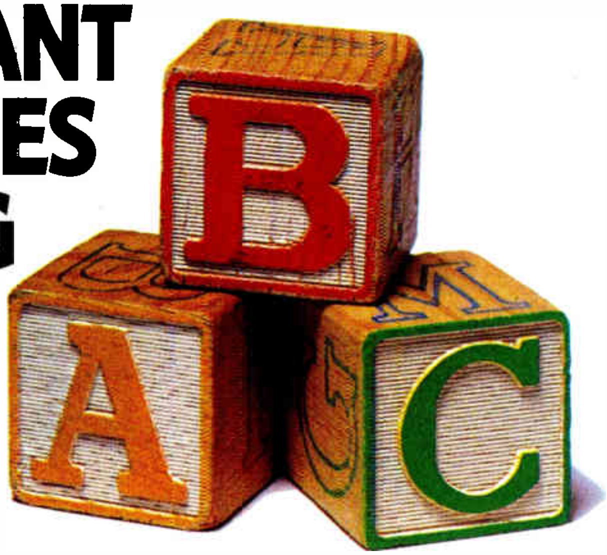
The P/40 16-bit commercial system uses the Unix operating system and the C programming language to support up to 24 stations simultaneously. In its standard configuration, the computer includes the main processor with 512-K bytes to 1 megabyte of main memory, the Multibus interface, intelligent disk and tape controllers for up to four Winchester disk drives and four nine-track tape drives, and from one to three intelligent communication processors with eight serial ports and one parallel port each. The disks can store up to 580 megabytes.

The system is aimed at businesses and computational-intensive applications in which ease of program development and software transportability are important.

A typical eight-user system with 512-K bytes of main memory, 72 megabytes of disk storage, an eight-channel intelligent communications controller, and a nine-track magnetic-tape unit is $49,500 without terminals. A Unix license is an additional $5,000. The system is currently available.

Plexus Computers Inc., 2230 Martin Ave., Santa Clara, Calif. 95050. Phone (408) 988-1755 [367]

RACAL-VADIC'S FULL V.22 COMPLIANT MODEM MAKES COMMUNICATING AS SIMPLE AS...



V.22 Means Four Times the Speed!

Racal-Vadic, world leader in low and medium speed modems, is in full production on Model 1222, a V.22 compliant modem which operates full duplex at 1200 bits/second over 2-wire dial-up or leased lines. Furthermore, it offers all three V.22 alternatives... A, B, and C.

The 1222 makes it possible for terminal users to transmit and receive data four times faster, with no change in protocol, by merely replacing a V.21 300 bps modem with the new Racal-Vadic 1200 bps full duplex unit. No longer will data terminals with 1200 bps capability have to settle for 300 bps operation!

Racal-Vadic, World Leader in 1200 bps Full Duplex Technology

Racal-Vadic is by far the world's leading manufacturer of 1200 bps full duplex modems. No wonder! Racal-Vadic invented 1200 bps 2-wire full duplex transmission in 1973, and has a worldwide installed base of over 125,000 of these modems.

There are a number of reasons why the Racal-Vadic 1222 is the most versatile V.22 compliant modem you can buy. First, if offers all three alternatives... A, B, and C. The inclusion of alternative C means that the 1222 will operate with any terminal at ALL standard asynchronous speeds to 1200 bps, plus split speed (300 bps in one direction, 1200 bps in the other), and overspeed as well.

Also, displays and built-in diagnostics are second to none for pinpointing faults in the entire data network. Packaging is versatile, too. The 1222 is available in a compact desk top cabinet for remote use, or for central computer sites. Up to seven 1222 modems can be housed in a 8 3/4-inch high rack-mounted card nest including power module.

Further, the 1222 is backed by Racal, worldwide leader in data communications.

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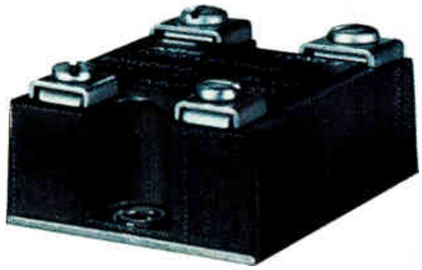

Superior SSR Immunity to EMI. Under $6.40.*

Potter & Brumfield EOM series solid state relays do not false operate (half-cycle) even when subjected to EMI induced by transients greater than 10,000 Vpp (NEMA ICS 2-230 Electrical Noise Immunity Test). And they come in a low profile package at low, low prices.

Transients of less than 1500 Vpp can cause many SSRs to half-cycle, generating even more EMI which can upset sensitive logic circuits. Half-cycling can also lead to early relay failure and shortened load life.

EMI radiated or coupled into these SSRs through the baseplate, input terminals or plastic case can false operate the off-state triac/SCR gate firing circuit. This negates the zero-crossover function, so gating can occur at or near peak AC load voltage. Load current will then flow until the next zero-current point, and the load circuit becomes a potential source of harmful EMI.

The high noise immunity EOM can minimize these circuit problems. For complete specifications and results of our NEMA tests, write for product application note "False Operation of Solid State Relays."

The newest EOM in our SSR family measures only 0.875" high; and 10 amp, 120V AC models are available from leading distributors backed by P&B's sizable factory inventory. Consult our factory for other voltage and current ratings. Potter & Brumfield Division AMF Incorporated, 200 Richland Creek Drive, Princeton, IN 47671. 812/386-1000.

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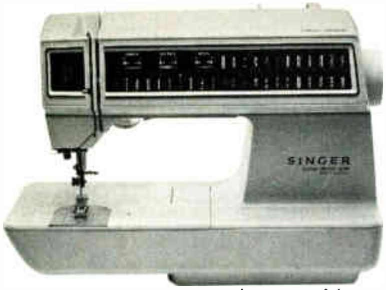

A scratch-resistant *Nesa* glass touch control panel can replace virtually any electro-mechanical device. With no moving parts, there's nothing to break off. And hot or cold environments, indoors or outdoors, won't harm it, either.

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No more pieced-together compromises! Bausch & Lomb innovation has produced a unique long working distance microscope with magnifications to 1000X and working distances from .5" to 1.2". And, MicroZoom Microscopes also include these innovations:

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- Special MicroZoom Prober Models, designed for mounting on your probe station, add greatly to the safety, speed, and accuracy required for critical autopsy probing applications.

When faster assembly and inspection are required, choose Bausch & Lomb StereoZoom® Microscopes. Large working distances to 10.5".

Zoom ranges from 1X to 7X. Magnifications to 280X.

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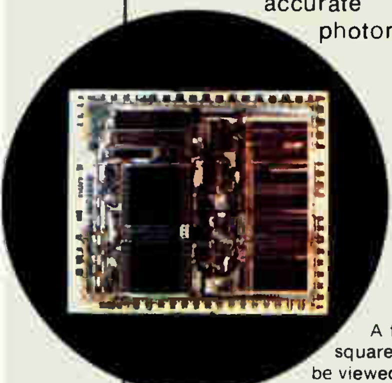

A full ¼" square chip can be viewed at the lowest magnification, 22.5X.

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Circle 56 on reader service card

Microcomputers & systems

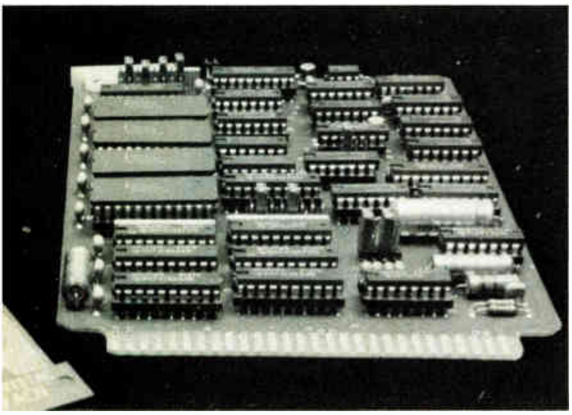
EE-PROM board rides STD bus

Flexible 8-K-byte nonvolatile memory card produces own erase-write control signals

The 3702 STD-bus nonvolatile memory board uses Intel's 2816 or 2815 electrically-erasable programmable read-only memories to store 8-K bytes for 10 years without batteries. All the circuitry necessary to erase and write bytes or blocks is on the board, which is available with a 350- or 250-ns read-access time.

The board may appear to the processor simply as a random-access memory, requiring no special software provisions, or it may operate in eight other modes, some of which involve generating wait signals during the 20 ms required to erase and write a byte. Interrupt modes, for example, allow the board to latch addresses and data, releasing the system for other tasks and to interrupt it when writing is done.

Both vectored and polled-mode interrupts are supported. Modes are selected with the appropriate input codes or with on-board jumpers that prevent potentially disastrous mode changes. A write-protected mode locks the board to ensure data integrity, permitting writing only after a specific byte is sent to one of its ports and relocking the board automatically following the write cycle.



The board may be used to store tables, calibration constants, data, instrument set-ups or for any other job formerly using battery-backed RAMs. It allows programs to be downloaded to a system from a remote location and is handy during program development.

The 8-K-byte 3702 with a 350-ns access is available for $495 in single units and is delivered in six weeks. The 250-ns version and depopulated versions are available on special order.

Solar Wind Systems Inc. 94 Galli Dr., Novato, Calif. 94947. Phone (415) 883-0404 [371]

Two members are added to growing 6805 family

Two versions have been added to Motorola's 6805 family of 8-bit microcomputers. Both feature zero-crossing-detection circuitry on chip. The MC6805T2 also has phased-locked-loop circuitry on the chip, along with a clock, 2,508 bytes of user read-only memory, and 64 bytes of random-access memory. The unit offers time start/stop and source-selection functions and a self-check mode. It also features 19 TTL and complementary-MOS compatible bidirectional input/output lines. Eight lines are compatible with light-emitting diodes.

The device's on-board PLL functions under software control include a three-state phase and frequency comparator, a 14-bit variable divider, and a 10-stage mask-programmable reference divider. The device, made with Motorola's high-performance H-MOS process, is available now in both plastic and ceramic 28-pin dual in-line packages. In quantities of 1,000, the plastic-housed units are $5 each.

The MC68705U3 adds 3,776 bytes of erasable programmable ROM to its 112 bytes of RAM and an internal 8-bit timer with 7-bit prescaler, but has no PLL functions. It emulates the MC6805U2, has an on-chip clock generator, and has 24 TTL- and C-MOS-compatible bidirectional I/O lines, of which eight will drive LEDs. It will be available in December 1981, priced at $38 in 1,000-unit quantities.

Motorola Inc., MOS Integrated Circuits Division, 3501 Ed Bluestein Blvd., Austin, Texas 78721. Phone (512) 928-6863 [372]

CRT terminal board meets OEM display requirements

The Hawk I cathode-ray-tube terminal board is based on an 8085A microprocessor with a dedicated large-scale integrated CRT controller (CRT 5037 VTAC) and an LSI video-display–attributes controller (CRT 8002 VDAC). It allows the user to configure a complete 80-column by 12-row smart display terminal by connecting to it a keyboard, an 18.6-kHz monitor, and a power supply. The display interface provides either separate horizontal, vertical, and video TTL signals or composite video signals for the monitor. It has editing features such as character and line insert and delete and full or partial screen erase; video attributes such as underline, reverse video, character blinking, half intensity, and character blanking; and a 64-character graphics set for the mixing of alphanumeric and graphic displays.

Hawk I can be custom-designed to meet the original-equipment manufacturer's terminal subsystem requirements by offering flexibility in screen display format, character field size, scan rate, character set, and keyboard function definition. It sells for $425 per unit and in quantity discounts. Delivery is immediate.

Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, N. Y. 11788 [373]

Single-chip computer has 12-mW dissipation

A complementary-MOS 8-bit single-chip microcomputer performs logical processing, basic code conversions, and formatting and generates fundamental timing and control signals for

Our filtered connectors keep your system quiet so you won't disturb the FCC.

Get a breather from redesigning today's equipment. Control interference and eliminate electrostatic discharge. Avoid the need for special cable. You can do it all with AMP Quiet Line filtered connectors.

By absorbing noise instead of reflecting it back into the system, our filtered connectors harmlessly dissipate noise as small amounts of heat. And in the process, their performance helps you comply with the new FCC emission regulations.

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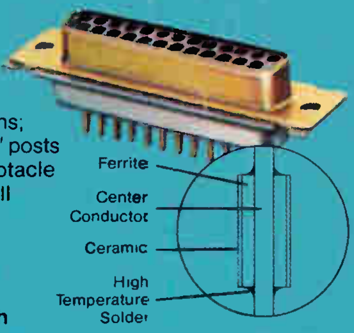
AMP Facts

Subminiature D Type
- RS 232/449 and MIL-C-24308 compatible
- Available in 9, 15, 25 and 37 position sizes.
- Right-angle board-mount, solder-cup and male-female interface versions.

Filtered pin header
- 10 through 50 positions; .100" centerline; .025" posts
- Mates with AMP receptacle connectors and with all similar types.
- Bulkhead mountable.

Circular connector
- 8 positions.
- Bulkhead feedthrough receptacle with pin contacts.

Performance
- Insertion loss—3db at 5MHz to 55db from 1-18 GHz.
- Higher loss elements available



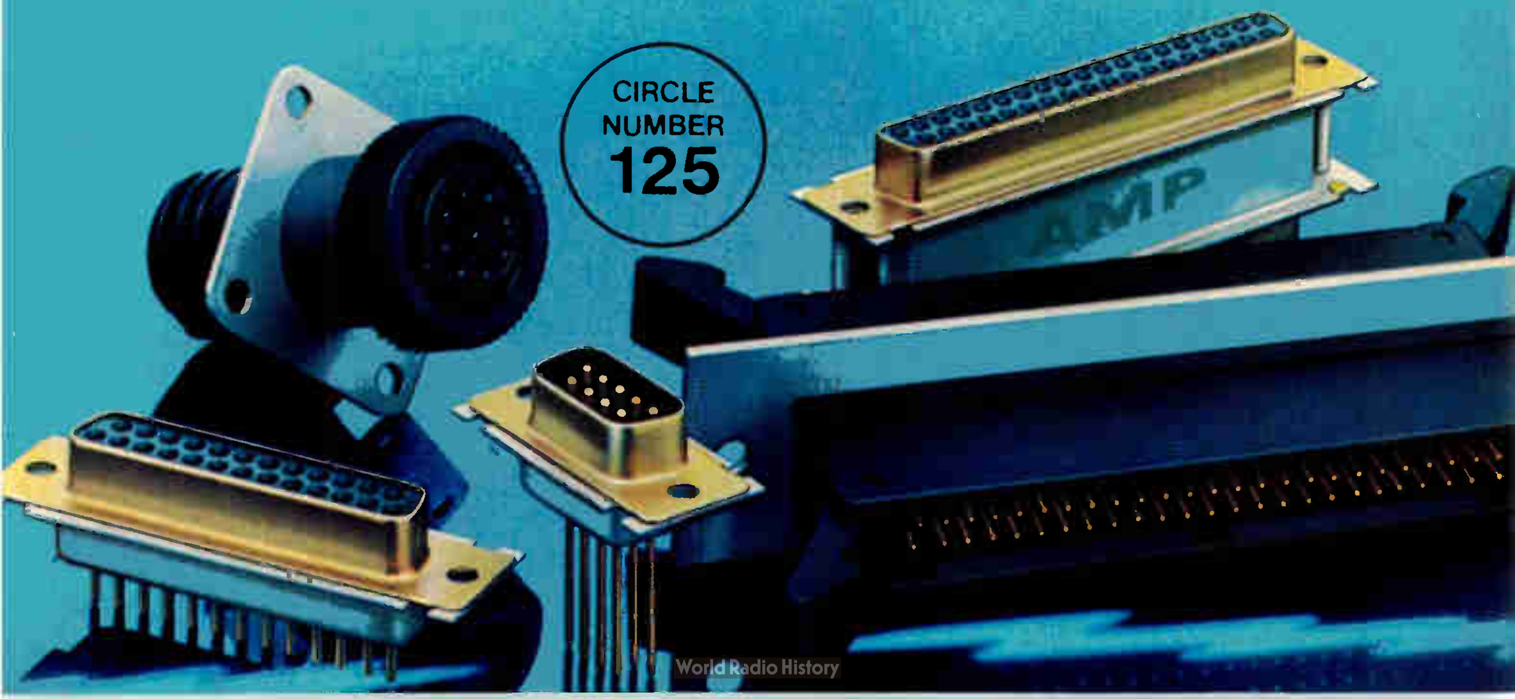
Absorptive Filter Element

For more information, call the AMP Filtered Connector Desk at (717) 780-8400.

AMP Incorporated, Harrisburg, PA 17105.

AMP means productivity.

CIRCLE NUMBER 125



input/output devices. Called the PIC16C55, it consists of a register file of 32 8-bit registers, an arithmetic and logic unit, and a customer-defined read-only memory of 512 program words each 12 bits wide. The register file is divided into operational registers that include real-time clock, counter register, program counter, status register, and I/O registers, as well as the general-purpose registers that are used for data and control information under the command of the instruction set. The ALU contains one temporary working register for accumulator and gating to perform Boolean functions, and the ROM contains the operational program for the rest of the logic within the controller. It also employs an on-chip two-level stack to provide subroutine nesting.

The PIC16C55 is a 28-pin chip that has a low power consumption of a maximum 12 mW, accepts voltages between 2.5 and 6 V, and is hardware- and software-compatible with other members of the PIC family. The C-MOS microcomputer sells for under $3; delivery of the unit takes 16 weeks after receipt of order.

General Instrument Corp., Microelectronics Division, 600 West John St., Hicksville, N. Y. 11802. Phone (516) 733-3120 [374]

Bus joins two Multibus cards, generates its own ± 12 V

The ZX-602 Flatbus allows any two Multibus cards to be connected to form a two-card system that can be panel-mounted in a 2-in.-thick space. It can be attached to a 5-V connector (compatible with Shugart's floppy-disk connector) to generate ±12 V. Two additional mass-terminating connectors are provided on the 602 for use with the company's ZX-85 central-processing-unit card. These two connectors are to be wired to the ZX-903 reset and interrupt panel and the ZX-904 parallel input/output unit. With the 602, the firm's model 235 Integrated work station, containing the ZX-730 dual 8-in. floppy unit, the ZX-85 CPU, and ZX-200A disk controller can be

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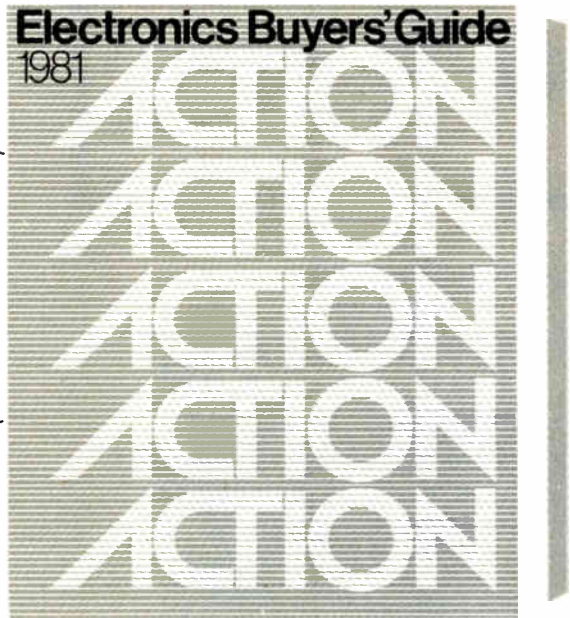

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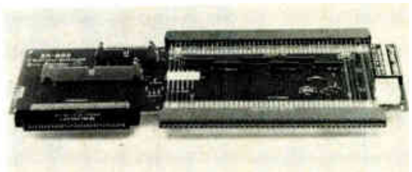

formed—creating a compact unit that can be purchased for slightly over $8,000.

The ZX-602 Flatbus is available from stock at $550.

Zendex Corp., 6680 Sierra Lane, Dublin, Calif. 94566. Phone (415) 829-1284 [375]

C-MOS 8-bit computer executes in 0.5 μs

The HD6301V complementary-MOS 8-bit single-chip microcomputer features a 4-K-byte read-only memory, 88 basic instructions, 128-K-byte random-access memory, error-protection functions, 16-bit timer, serial communication interface circuit, and 29 parallel input/output lines for a performance equal to that of the top C-MOS 8-bit single-chip microcomputer on the market, according to the company.

The HD6301V comes in 2.0- and 1.5-MHz versions with minimum instruction-execution cycle times of 0.5 μs for the 2.0-MHz type and 0.67μs for the 1.5-MHz version. Both have a low power consumption of 35 mW for normal operation, 5 mW in the sleep mode, and 30 μW in standby mode, making each suitable for use in pocket computers, portable data terminals and medical equipment, and telemeter systems.

Motorola's 6801 microcomputer, of which the HD6301V is a copy, runs at only 1.0 MHz and is fabricated in n-channel MOS. Hitachi's faster C-MOS version of the chip measures 6.82 by 7.98 mm, and a smaller version is expected to reach production early next year. Bit-manipulation instructions implemented by the HD6301V can speed execution in certain applications.

The HD6301V microcomputer is compatible with Hitachi's mainstay n-channel MOS 8-bit single-chip microcomputer and sells for $34 for the 1.5-MHz type and $41 for the 2.0-

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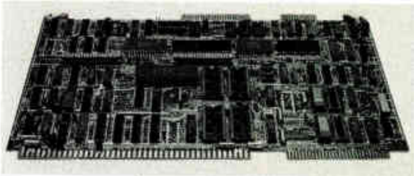
Circle 82 on reader service card

MHz version in the U. S. The shipments of samples are scheduled to begin this month.

Hitachi America Ltd., 1800 Bering Dr., San Jose, Calif. 95112 [376]

8088-based board supports 1-megabyte addressing

The iSBC 88/25 single-board computer is part of Intel's line of original-equipment manufacturer microcomputer systems. Based on the 5-MHz 8-bit 8088 processor, it not only is compatible with the 8-bit line of multimodule expansion boards via two iSBX interfaces, but it also is compatible with Intel's iRMX-88



and -86 16-bit real-time multitasking software offering a 1-megabyte addressing range. In addition, if combined with the iSBC 337 multimodule numeric data processor, which uses the 8087 Numeric processor chip, it yields a performance of 110,000 Whetstones/s.

The board is supplied with 4-K bytes of random-access memory (expandable onboard to 16-K bytes) and four 28-pin sockets for 32-K bytes of erasable programmable read-only memory (expandable onboard to 64-K bytes) and has as standard features two programmable interval timers, 24 parallel input/output lines, a serial I/O port with programmable bit rates, and nine levels of vectored interrupt control.

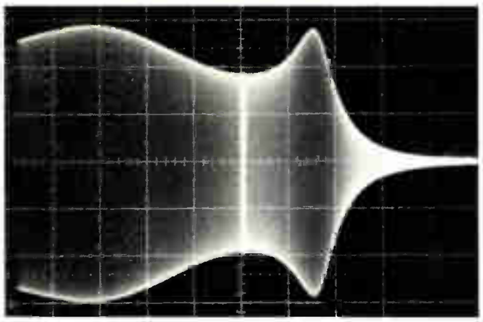
The iSBC 88/25 is suitable for applications such as process and machine control, instrumentation, data communication, and industrial automation. It is priced in single-unit quantities at $1,295. The first customer shipments are slated for November.

Intel Corp., 5200 N. E. Elam Young Parkway, Hillsboro, Ore. 97123. Phone (503) 640-7147 [378]

The combination of digital storage and the analog frequency dial for setting sweep START/STOP and marker frequencies makes the Model 189 a real pleasure to use.

Turn the dial to the desired low frequency (down to 4 mHz) and push START. Then turn the dial to the high frequency (up to 4 MHz within sweep limits) and push STOP. Both frequencies are stored in memory, so the dial is now available for setting the marker frequency.

Other controls set sweep rates from 100 microseconds



rates from 100 microseconds
to 120 seconds, hold or reset sweeps, and set output level (up to 20V). As a function generator, Model 189 gives precision sine, square and triangle waveforms from 4 mHz to 4 MHz in continuous, triggered or gated modes.

So if you're looking for an inexpensive sweep/function generator that handles precision sweeping assignments, you're looking for the Wavetek Model 189.

For more information, contact:
Wavetek San Diego
P.O. Box 651
9045 Balboa Avenue
San Diego, CA 92112
Tel. (714) 279-2200;
TWX 910-335-2007.

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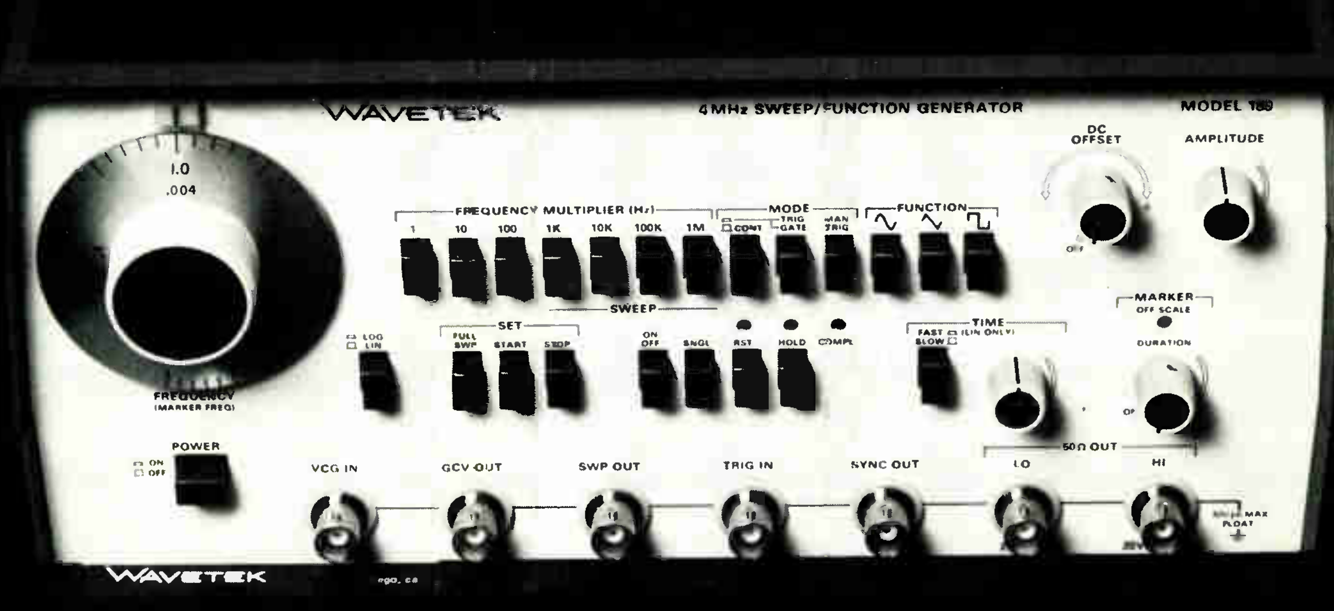
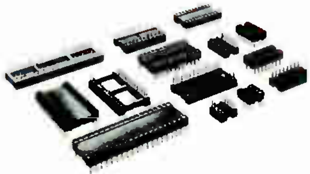


INTERCONNECTION CITY NEWS

NEW card edge connector with insulation displacement contacts for mass termination. Fits .062" PC boards, 4 thru 15 positions.

Circle 104 on reader service card



NEW open & closed low-profile frame IC/DIP sockets R-4000 series with anti-wicking contacts, end and side stackable on .100" grid, meet EIA RS-415 standard.

Circle 381 on reader service card

NEW, in line "JAGUAR" IDC series of mass termination .100" and .156" center connectors for wire-to-board discrete wire or ribbon cable applications.

Circle 382 on reader service card

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Circle 383 on reader service card

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Circle 384 on reader service card

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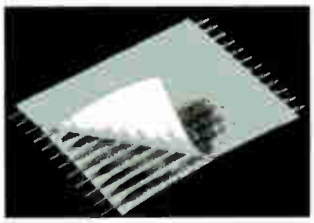
Circle 385 on reader service card

NEW Series 2300, 1-6 circuit power connector insulation displacement termination. Saves crimping & stuffing contacts. Hermaphroditic housing saves handling & inventory. Circle 386 on reader service card

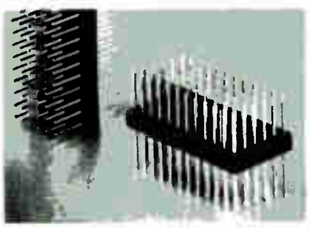


NEW "SUPER-PLY" flat cable jumpers with round wire ends offer reduced circuit board interconnection costs by direct mounting. No special termination required.

Circle 387 on reader service card

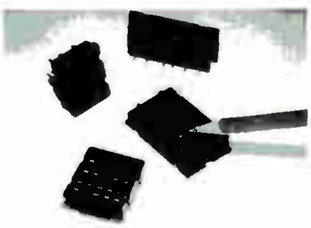
Full mil-spec line of multi-contact sockets for round or square crystal can relays. Insulator bodies are molded green diallyl phthalate.

Circle 388 on reader service card



Wrap type "RELI-ABLOC" terminal blocks for telecommunications with .045" square, .750" long terminals on .240 grid pattern.

Circle 389 on reader service card



NEW miniature 4 and 5 pole standard and programmable turn-around styles of sockets for popular industrial relays. Rugged thermoset molded bodies.

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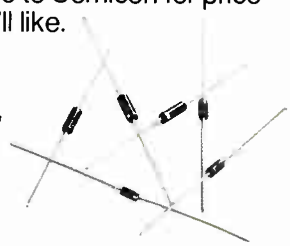

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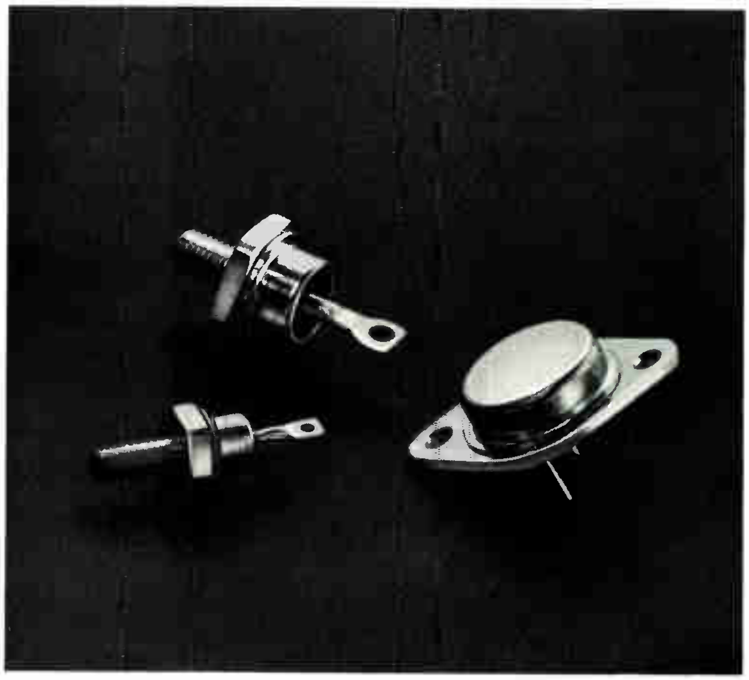

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Twice the channels. Twice the density. Half the cost per channel.

The new Precision System 32 packs 32 programmable channels into the same 7 inches of rack space previously needed for 16.

You get more than 2 digit resolution, with 2047 programmable cut-off frequencies. Time delay filters are superior to Bessel. Elliptics afford 80 dB/octave attenuation. Phase match is within 1°. Interfaces with mini, micro or GPIB.

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Circle 108 on reader service card

Components

E-PROM sets up $100 keyboard

Standard-layout capacitive keyboard is modified using 8748 processor's E-PROM

For its first standard capacitive keyboard, Digitran Co. has given high-volume users the main features of its custom units. But the new KS99, in addition to its general-purpose applications, offers customers a choice of coding schemes through the use of a flexible microcomputer with on-chip erasable programmable read-only memory.

The intelligent keyboard uses an 8748 processor with E-PROM for scanning and encoding so that the standard unit can be programmed to individual needs, according to its maker, a division of Becton, Dickenson and Co. This versatility makes the new keyboard suitable for small-business and home computers and word processors.

Simple and durable. Among the KS99's features is the patented moving-plate capacitor switch action, which is comprised of a hinged moving plate and single fixed plate, both of which are attached directly to the printed-circuit board. The simple design has a mean cycle between failures specifications of 250 million operations, one of the reasons Digitran confidently accompanies the keyboards with a two-year warranty.

The device comes with one or two output configurations: one version has a parallel output with negative strobe and the other a 10-bit, 300-b/s serial output. All outputs are at standard TTL-compatible positive logic levels and can drive at least one TTL load. A single 5-V power supply is required to provide a maximum of 200 mA.

The ASCII-compatible keyboards use keys that require a 1¾-oz depression force and prevent errors by waiting for a key to be held down for 30 ms before transmitting the code. Automatic character repetition is at 15 characters per second.

The KS99 will be an off-the-shelf product; evaluation units are available now. It is priced at $129.95 in lots up to 99, $99.95 in 100s, and less in higher volumes.

The Digitran Co., 855 South Arroyo Parkway, Pasadena, Calif. 91105. Phone (213) 449-3110 [343]

Switched-capacitor filter technique reduces chip size

A series of integrated monolithic filters from Reticon uses the switched-capacitor technique to reduce chip size, permit adjustment of the clock rate, and gain stability over temperature compared with standard discrete or hybrid filters.

The R5609 low-pass filter is a seven-pole, six-zero elliptic device with over 75 dB of stopband rejection and less than 0.2 dB of passband ripple. The R5613 linear-phase low-pass filter has a linear-phase passband and elliptical stopband for sharper roll-off and 60 dB of stopband rejection.

The R5611 high-pass switched-capacitor filter is a five-pole Chebyshev device with 30 dB per octave of roll-off and less than 0.6 dB of passband ripple.

Reticon's R5612 notch SCF is a four-pole filter with over 50 dB of rejection at the notch frequency.

Each device is packaged in an 8-pin dual in-line package and sells for under $7 in 10,000-unit orders.

EG&G Reticon, 345 Potrero Ave., Sunnyvale, Calif. 94086. Phone (408) 738-4266 [343]

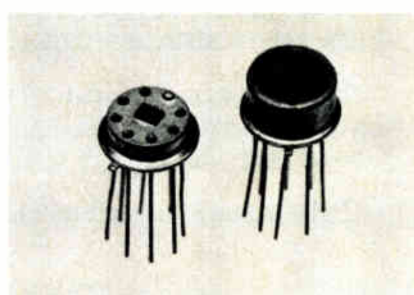
Laser trimming gives op amp 1 μV/°C offset voltage drift

A bipolar–field-effect-transistor operational amplifier called the AD547 achieves 1-μV/°C offset voltage drift by being trimmed with a laser at the wafer level. It has a maximum input offset voltage of 0.25 mV and also comes in J, K, and S grades.

The L-grade device's noise is at a maximum of 4 μV peak to peak, at 0.1 to 10 Hz, and its bias current is guaranteed at 25 pA, maximum. It will operate over a ±5- to ±18-V supply range. Its low offset and bias current make it suitable for many signal-conditioning applications. For handling ac signals, typical small-signal bandwidth (−3 dB) is rated at 1 MHz, full power at 200 kHz, and slew rate at 3 V/μs.

The J, K, and S grades offer maximum offset voltage and offset voltage drift figures of 1.0 mV and 5 μV/°C for the J grade, 0.5 mV and 2 μV/°C for the K grade, and 0.5 mV and 5 μV/°C for the S version.

The AD547 is packaged in a TO-99 metal can and is specified for operation over the 0° to +70°C range for the J, K, and L grades and −55° to +125°C for the S model. In



Thinking about Color for Avionics Displays?
Think Syntronic Deflection Yokes

Cockpit displays in color are the hottest thing in avionics. Why? Because color increases the amount of information a pilot can absorb in a finite time frame. Think of the myriad uses of color. Emergencies or targets highlighted by red. Normal status is white or green. Sky shown in blue with the ground in brown tones. Almost anything displayed mechanically now can be displayed on a color CRT, with no parallax, a condensed format and less clutter on the instrument panel.

But color displays are many times more complex than monochromatic displays because of the critical interface between CRT, yoke and circuitry. And avionic quality displays are too demanding for conventional color TV type yokes.

That's where Syntronic helps the display engineer. For several years, Syntronic Instruments, Inc., the leader in precision yokes for military and industrial displays has been working with major international manufacturers of full-color shadow mask tubes to develop high performance color yokes. High resolution, color purity and convergence, along with faster speed for more display information, all combine to make deflection yoke design a truly challenging task. Syntronic now offers the yoke design capability *and* the technical assistance needed for today's and tomorrow's top quality color avionics displays.

If you're thinking *color*, think Syntronic Instruments. Call Dave Brown at 312—543-6444 for more information.

syntronic Precision yokes for exacting displays

Syntronic Instruments, Inc., 100 Industrial Road, Addison, IL 60101 (312) 543-6444

Circle 112 on reader service card

input to output line of 100 ns at 5 V over the −40°C to +85°C range, reducing the total access-time path in a large decoded memory or I/O system. The unit's output source and sink capability are balanced, and are equivalent to those required for four standard TTL loads. This drive capability allows direct interfacing with large memory sysems without additional buffering.

The CDP1873C can be used in CDP1800 or other general-purpose microprocessor systems as an address decoder or I/O address bus expander. The 16-pin dual in-line device is compatible with the 74LS138 and can be used in similar applications, especially where low power and high noise immunity are desirable. The plastic version sells for $1.68 in quantities of 100 to 999, and the ceramic model costs $1.08 in 1,000-unit lots. Delivery is from stock.

RCA Solid State Division, Box 3200, Somerville, N. J. 08876. Phone (201) 685-6423 [346]

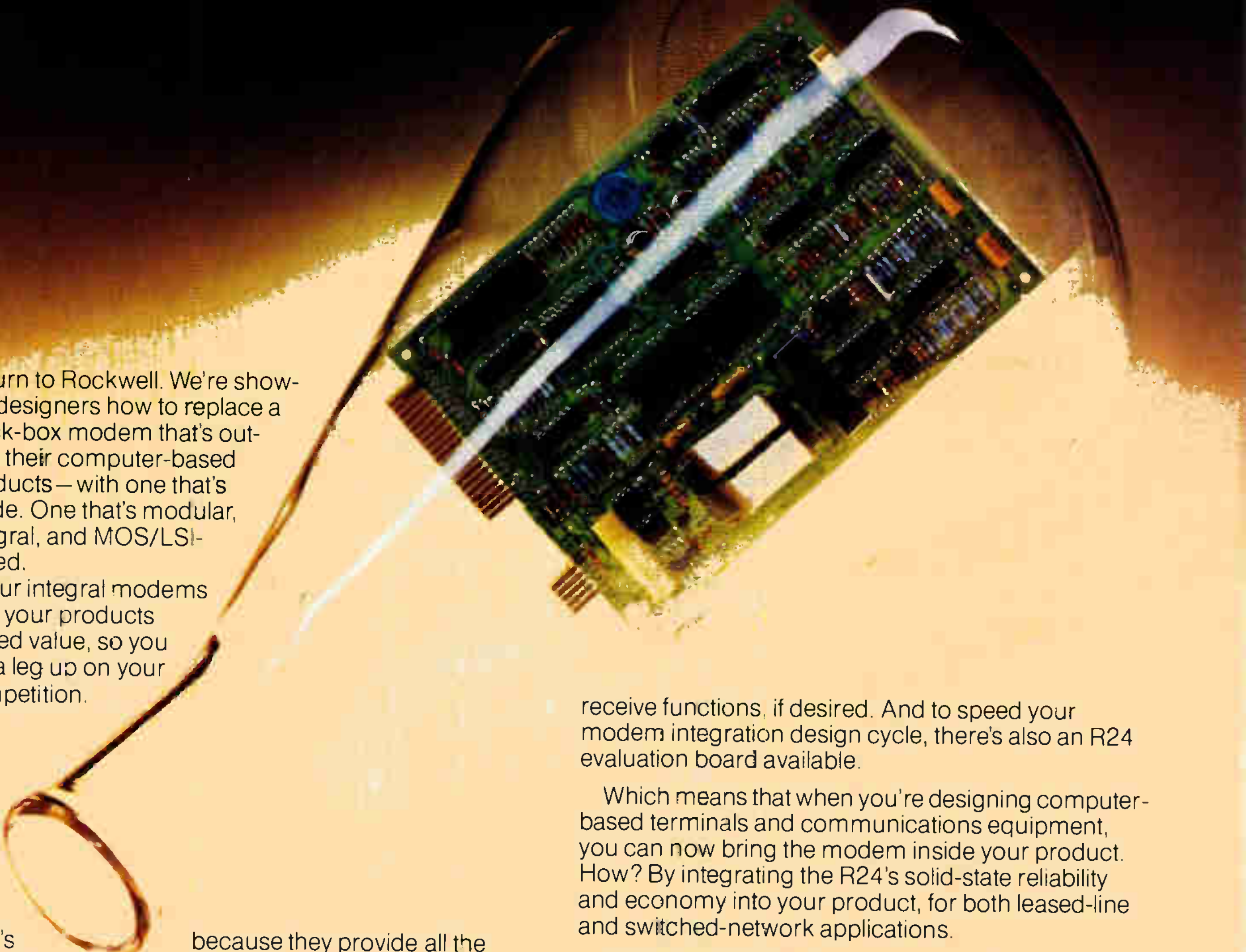
Reflective sensor contains IR emitter, phototransistor

A new reflective sensor sports an infrared emitter side by side with a phototransistor collector housed in a miniature plastic package 0.075 by 0.145 by 0.275 in. A daylight filter screens out extraneous light. The SFH-900's photo current is more than 3 mA at a collector-to-emitter dc voltage of 5 V and a dc forward current of 10 mA, at a distance of 1 mm between the sensor and the reflector. Collector-emitter leakage current is typically 20 nA.

The miniature reflex light barrier is designed for such applications as a position-reporting device, an end position switch, a speed monitor, or as a feeler element in various types of motion transmitters. In 1,000-unit lots, the SFH-900 is $2.24 each with delivery from stock or up to six weeks.

Litronix Inc., 19000 Homestead Rd., Cupertino, Calif. 95014. Phone (408) 257-7910 [348]

How to turn your modem outside-in.



Turn to Rockwell. We're showing designers how to replace a black-box modem that's outside their computer-based products—with one that's inside. One that's modular, integral, and MOS/LSI-based.

Our integral modems give your products added value, so you get a leg up on your competition.

That's because they provide all the features of black-box modems—but at a fraction of their cost. Plus their compactness gives you new physical design freedom.

And Rockwell modems are available at a level of integration that meets your requirements. Take our R24, for example. A 2400-bps synchronous modem, it comes in three configurations—all exceptionally compact, and compatible with Bell 201 B/C and CCITT V.26 A/B standards.

First there's our fully assembled and tested single-board modem, ready to plug into your system—like the one shown above. Then there's our set of three discrete modules, ready to be designed into your own modem. They allow you to separate transmit and receive functions, if desired. And to speed your modem integration design cycle, there's also an R24 evaluation board available.

Which means that when you're designing computer-based terminals and communications equipment, you can now bring the modem inside your product. How? By integrating the R24's solid-state reliability and economy into your product, for both leased-line and switched-network applications.

That's just the kind of advantage you'd expect from Rockwell, the company that's delivered more integral LSI 4800/9600-bps modems than anyone else in the world. That's right—*anyone*. And Rockwell modems are in stock now—fully assembled, on production or evaluation boards, or as discrete modules.

So don't leave your modems on the outside looking in. For information or applications help, call toll free: (800) 854-8099; in California, (800) 422-4230. Or write: Rockwell International, Electronic Devices Division, RC55, P.O. Box 3669, Anaheim, CA 92803.

Rockwell International

...where science gets down to business

Circle 119 on reader service card

Software

Packages support VAX-11 data base

Data-management software lets nontechnical users access data with English commands

More nontechnical business workers will gain access to Digital Equipment Corp.'s VAX-11 series computers, thanks to an information-management software set that accommodates programmer and non-programmer alike. The VAX Information Architecture, as DEC calls it, initially consists of three packages written in Bliss: the VAX-11 Codasyl-compatible Data-Base Management System; the VAX-11 Datatrieve, a high-level data-manipulation facility; and the VAX-11 Common-Data Dictionary.

The VAX-11 DBMS, based on the 1981 ANSI data-base working documents, handles multiple data-base structures totaling up to 5 billion bytes. It supports simultaneous access by many users, locking at the record level rather than at the page or area level to speed response time and prevent data corruption due to simultaneous updates. The VAX-11 DBMS also protects data-base integrity by retracting incomplete updates, or issuing rollback commands whenever a process is aborted.

The VAX Information Architecture also supports VAX RMS, a records-management facility already present in the VAX/VMS operating system. VAX-11 Datatrieve lets nontechnical users access RMS- and DBMS-stored data using simple English commands to define, enter, display, manipulate, or retrieve data; programmers also may elect to use shorter, symbolic commands. Data can be assembled into a variety of user-designed report formats, including VAX-11 FMS forms, tabular presentations, and graphics.

Users can interactively enter, edit, and execute Datatrieve commands, which can be stored and invoked as complete command sequences by the VAX-11 languages. Datatrieve also allows relational access to data, using common fields to retrieve records scattered over several local or (optionally) DECnet-linked remote files.

Datatrieve's file, record, and view definitions, and its stored procedures and validation tables, all reside in the VAX-11 Common-Data Dictionary along with definitions of user authorization for accessing any piece of data. Using these definitions, Datatrieve automatically routes (or denies) interactive or program requests without requiring the user to specify data relationships, format, or location.

The Common-Data Dictionary also contains all data-base definitions for the DBMS, including schema, subschema, and storage schema. An automatic default facility in the DBMS generates subschema and storage schema based on user-specified schema for small applications. This feature eliminates a full-scale design effort initially, yet allows for later, limited restructuring by the user without unloading and reloading the whole data base.

Due for first delivery in December, the VAX-11 DBMS carries a license fee of $30,000. The VAX-11 Datatrieve package, licensing for $15,000, and the $3,000 VAX-11 Common-Data Dictionary will be delivered next month.

Digital Equipment Corp., Continental Boulevard, Merrimack, N. H. 03054. Phone (603) 884-5111 [391]

Kernel for Z8002 offered in ROM

Interrupt-driven multitasking executive coordinates up to 256 tasks with system calls

A startup company called Hunter and Ready is offering VRTX, a real-time multitasking operating-system kernel for the Z8002. The kernel is distributed in read-only memory—a silicon software product following closely the introduction of Intel's 80130 silicon operating system, which performs many of the same functions for the 8086.

VRTX is an interrupt-driven multitasking executive that relieves the application programmer from the burden of coordinating multitasking systems. Instead of writing a monolithic program that performs the tasks at hand and also coordinates and synchronizes them, the programmer merely writes a separate program for each task and uses the system calls in the VRTX to do the rest. This can significantly reduce the development time of complex real-time software systems and at the same time provide a higher degree of reliability and standardization across a product line.

VRTX consists of 22 system calls that perform task management, intertask communication and synchronization, interrupt servicing, and memory allocation. It can also be used with a real-time clock for timing purposes.

The software can manage up to 256 separate tasks, each of which can be assigned a unique priority level so that the most important tasks are executed first. Tasks can be created, deleted, suspended, and resumed under the kernel's control. Intertask communication and synchronization is handled by a nonformatted mechanism that can implement semaphores, mailboxes, or message-passing, as the designer desires. This differs from Intel's approach on the 80130, which uses preformatted task creation and message passing. That buys Intel compatibility with iRMX-86 at the expense of execution speed. Mutual exclusion—for preventing, for example, simultaneous reads and writes to a disk—and resource locking can be supported by the general-purpose communication mechanism.

Interrupts require a user-supplied

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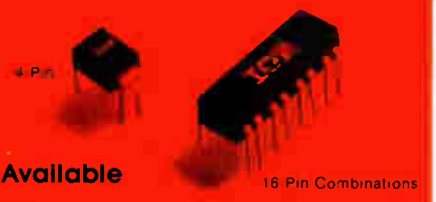

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4-PIN HEXDIPs. Rated 1-Watt

Type	Part Number	V_{DS}	$r_{DS(on)}$	I_D
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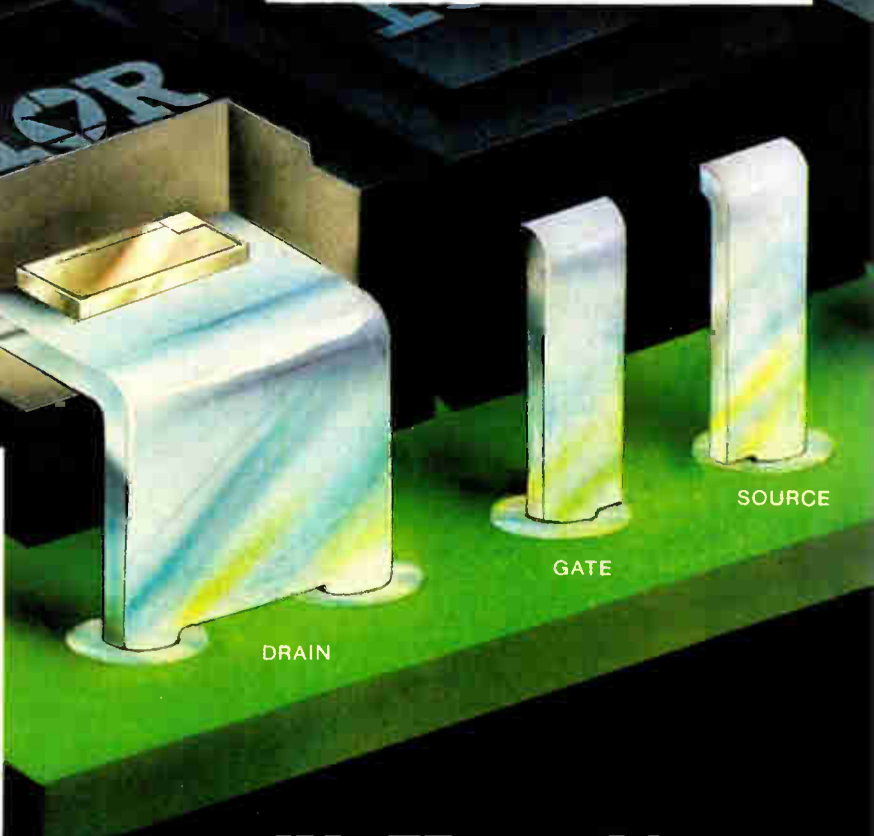
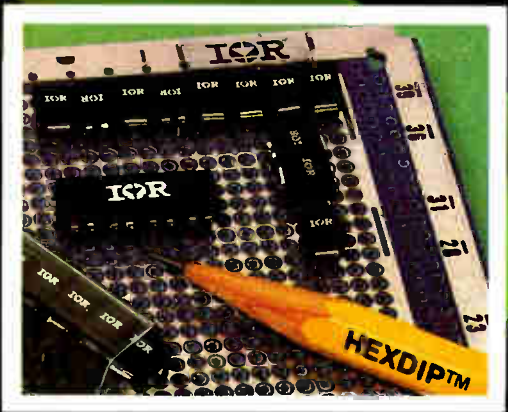
	IRFD111	60V	0.6Ω	1.0A
	IRFD112	100V	0.8Ω	0.8A
	IRFD113	60V	0.8Ω	0.8A
P CHANNEL	IRFD9120	100V	0.6Ω	1.0A
	IRFD9121	60V	[illegible]	1.0A
	IRFD9122	100V	0.8Ω	0.8A
	IRFD9123	60V	0.8Ω	-0.8A

16-PIN HEXDIPs. Rated 4-Watts

Type	Part Number	Combination	
N CHANNEL	IRFE110	FOUR IRFD110 4 PIN HEXDIPs	
	IRFE111	FOUR IRFD111 4 PIN HEXDIPs	
	IRFE112	FOUR IRFD112 4 PIN HEXDIPs	
	IRFE113	FOUR IRFD113 4 PIN HEXDIPs	
P CHANNEL	IRFE9120	FOUR IRFD9120 4 PIN HEXDIPs	
	IRFE9121	FOUR IRFD9121 4-PIN HEXDIPs	
	IRFE9122	FOUR IRFD9122 4 PIN HEXDIPs	
	IRFE9123	FOUR IRFD9123 4 PIN HEXDIPs	
N AND P CHANNEL PAIRS	IRFE5110	TWO IRFD110	TWO IRFD9120
	IRFE5111	TWO IRFD111	TWO IRFD9121
	IRFE5112	TWO IRFD112	TWO IRFD9122
	IRFE5113	TWO IRFD113	TWO IRFD9123





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IOR

Circle 124 on reader service card

new-program-status area to hold the addresses of the user's interrupt-service routines. Messages to a waiting task can also be delivered by the interrupt handler.

Both dynamic and static memory management is supported by VRTX, with separate stack areas provided for each task. All parameters needed to configure the software for a particular memory system and hardware configuration are supplied in the user-written configuration table, which can be as short as 14 words. Also, up to 128 system calls may be defined by the user.

Unlike Intel's 80130, which has other system resources on-chip (timers, interrupt controller, and bit-rate generator), VRTX is a ROM-only kernel, supplied in two 2716 erasable programmable ROMs. It can be linked to assembly language programs or high-level languages, like Whitesmiths' C, for which a CP/M-compatible interface library is available.

Hunter and Ready, 713 Santa Cruz Ave., Menlo Park, Calif. 94025 [392]

Kernel occupies about 100 bytes

Minimal-system multitasking kernel handles switching from one task to the next

The Multitasking Kernel from U. S. Software provides an easy-to-use aid for writing microprocessor software that must handle several tasks concurrently. It handles the switching between tasks by saving the status of the machine and performing the housekeeping duties necessary to start a new one. Since it can be placed in a read-only memory, it is useful in embedded applications that do not require mass storage. The multitasking software has been successfully used at several test sites for purposes including process control on the factory floor and the handling of data acquisition and distribution to and from remote medical instru-

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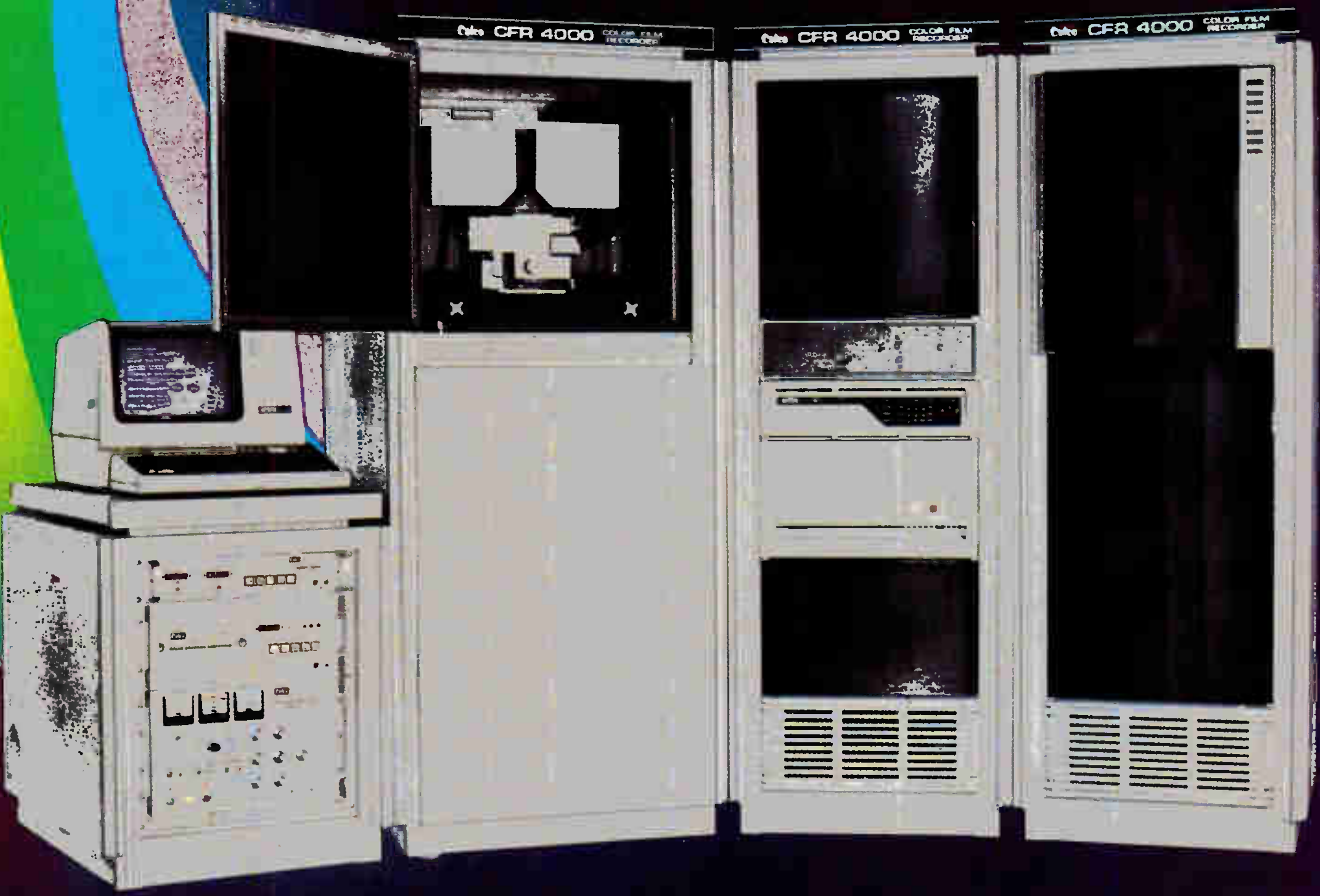

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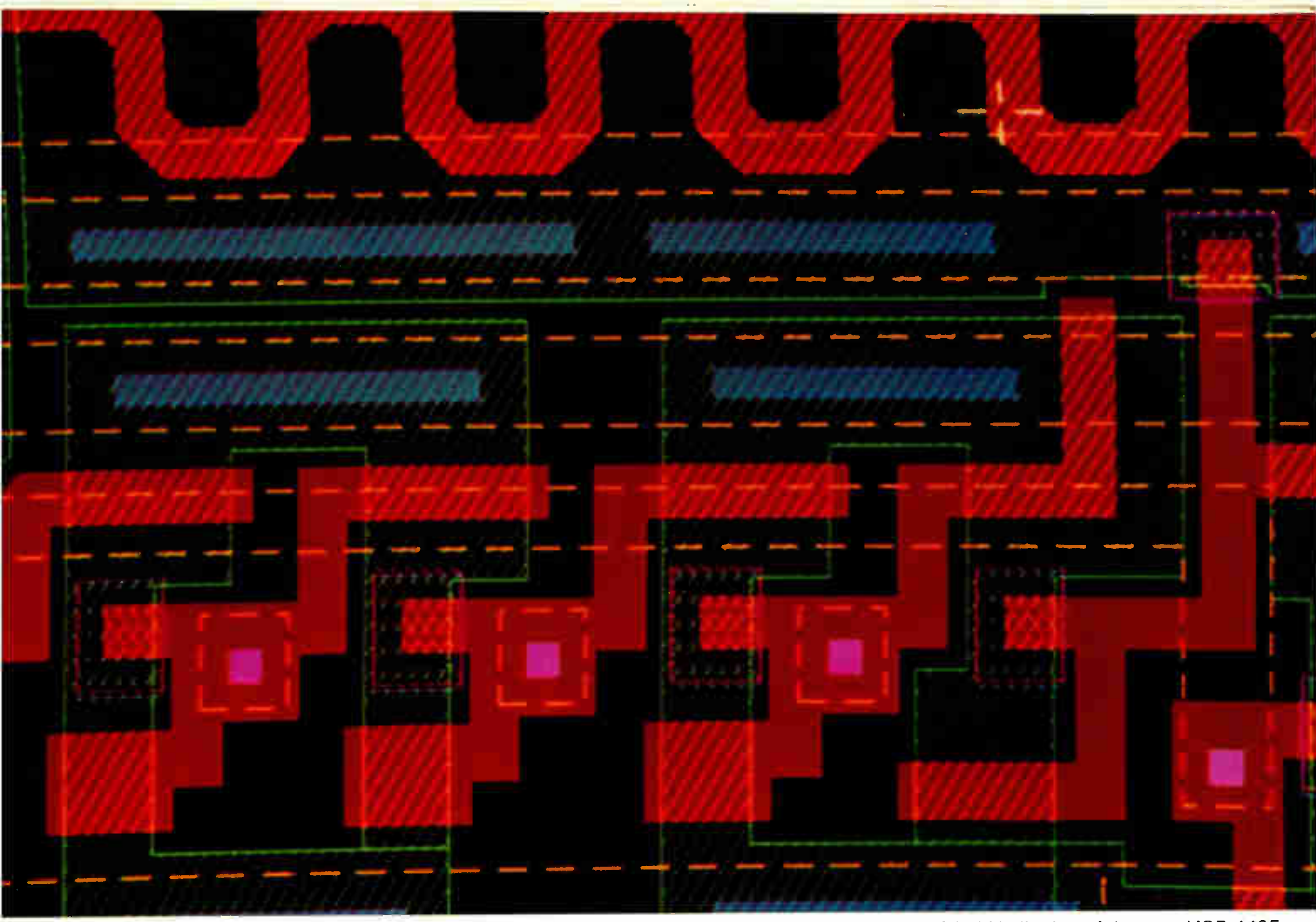

CALMA display of the new NCR 4485

Now you can draw on NCR's experience for the highest density, n-channel NV-RAM available.

NCR's newly patented SNOS (Silicon Nitride Oxide Silicon) process brings you the NCR 4485 — the highest density, microprocessor compatible NV-RAM available. Its 512x8 bit organization gives you 512 bytes of RAM and 512 bytes of EEPROM. All on the same chip.

With the NCR 4485, you get TTL compatibility, JEDEC standard byte-wide pinout, and a 450 ns worse case access time.

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The NCR 4485 is just the first member of a new n-channel family using SNOS. A family whose MNOS heritage ensures high quality and reliability. And because we're in the business to stay, you can look forward to even higher densities from NCR.

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For more information, call Dave Major at (800) 543-5618, in Ohio (513) 866-7217. Or write Dave at NCR Microelectronics Division, Box 606, Dayton, Ohio 45401.

NCR — NV MEMORY GUIDE

Device No.	Organization	Type
2051	32x16	WAROM
2055	64x8	WAROM
1400	100x14	WAROM
3400	1024x4	WAROM
2811	2048x4	EAROM
2168*	2048x8	EAROM
2161*	2048x8	WAROM
4485	512x8	NVRAM

*Pin conservative bus structured devices

MNOS p-channel description:
WAROM — Word alterable ROM
EAROM — Electrically alterable ROM

NCR
Microelectronics Division

gence features like insert line or delete character.

Versions for RDOS, DOS, and MP/OS are priced at $850 per system. The AOS/VS versions for the multi-user environment are priced at $1,000. Both are available immediately. All licenses include software updates at no charge for one year.

Rational Data Systems, 205 East 42nd St., New York, N. Y. 10017. Phone (212) 697-5855 [395]

Applesoft Basic compiler boosts execution speed

Tasc, a compiler for Applesoft Basic programs, converts a standard Applesoft program into machine code, enabling the program to execute much faster than was previously possible. This allows Apple owners to increase the speed of their Applesoft programs without having to learn a new programming language. Speed increases range from 2 to 20 times faster than regular Applesoft programs.

While Basic compilers traditionally impose significant program size restrictions, Tasc's disk-based design and object-code compression schemes can compile and run even large, complex Applesoft programs.

Tasc is easy to use and almost completely compatible with Applesoft, so existing and new programs can be compiled with little or no modification. It requires an Apple II or II Plus, Applesoft Basic, 48-K bytes of random-access memory, and one disk drive. It supports, but does not require the Microsoft RAMCard. It sells for $175, with delivery in 2 weeks.

Microsoft Consumer Products, 400 108th Ave., N. E., Suite 200, Bellevue, Wash. 98004. Phone (206) 454-1315 [396]

Management system builds decision-support systems

An advanced computer language and data-base management system named Express can implement and maintain financial and marketing-decision support systems. Express contains a multidimensional relational data-base system, display capabilities for on-line analysis, formal-report generation and graphics, a wide range of statistical techniques, and advanced modeling capabilities.

Among the applications are financial reporting and analysis, budgeting, long-range planning, cash planning, acquisition analysis, sales forecasting, product positioning, and production planning, as well as competitive analysis, advertising and promotion effectiveness, and strategic-product forecasting.

Express is available through time-sharing or in-house installation. The system was developed for a Prime 550 or 750 and IBM computers that operate under VM/CMS; a large system can simultaneously support 50 to 60 users. The price of an in-house installation starts at about $250,000. The system is available immediately.

Management Decision Systems Inc., 200 Fifth Ave., Waltham, Mass. 02254. Phone (617) 890-1100 [397]

Program merges several spread sheets into one

Supercalc is a spread-sheet software package for a wide variety of CP/M-compatible systems. Both 5- and 8-in. drives are supported with 5-in. formats, including Apple CP/M, Xerox 820, North Star, Superbrain, Micropolis, Zenith, Osborne, and Vector Graphics.

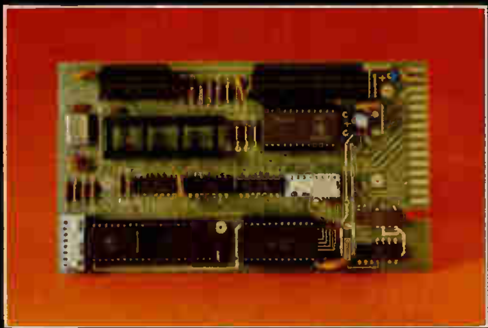
Its features include the ability to merge several sheets into one and a help command that guides the user through all the levels and options in the program. In addition, the program can automatically format printed reports and examine all formulas contained in a work sheet on an interactive basis. The package, which includes a users' guide, reference card, and installation program for use with over 25 terminals, sells for $295 and is available now.

Sorcim Corp., 405 Aldo Ave., Santa Clara, Calif. 95050. Phone (408) 727-7634 [398]

Oak puts E^3 up against the world's fastest typists.

In a keyboard market clogged with claims and confusion about "N-key-rollover," look to Oak's FTM® keyboard for the practical answer. It provides E^3-Entry Error Elimination. And that means precisely what it says. We challenge the fastest typists in the world to make it error. They can't.

Yet E^3 makes its real contribution to Oak's Full Travel Membrane (FTM) keyboard—and to you—in the cost column. You get the Entry Error Elimination and 100-million-cycle-plus performance you've got to have in a keyboard at prices far below those of keyboards with comparable performance. That's practical. Entry Error Elimination is a remarkably sensible microprocessor based N-key-rollover and phantom key lockout system developed by Oak engineers. Without the cost and complexity of Hall Effect and capacitive technologies.



And that's not all. Beneath the FTM keyboard is Oak's proven, industry-leading membrane switch technology. So you get all the good things of membrane switching—reliability, durability, RFI and EMI resistance, design flexibility, and—of course—low cost. All without sacrificing the qualities you demand in a keyboard, right down to human engineered industry standard feel and touch.

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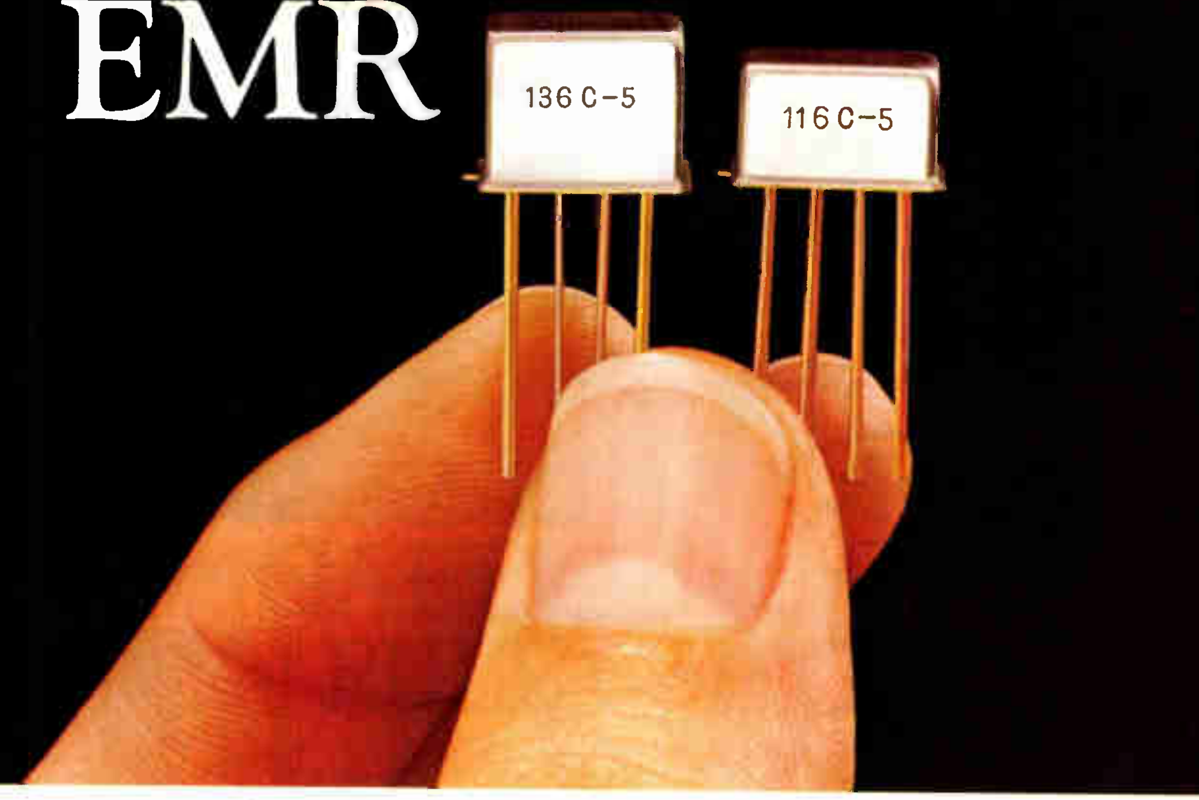

Now for the first time you can drive an electromechanical relay directly with the signals of most logic families—including CMOS. That means simpler board layout problems and reduced components counts for greater reliability.

The new Centigrid relay incorporates a power FET driver in the input to amplify the signal, protects it with a large Zener diode, and packs it all together with a DPDT relay and coil suppression diode in a tiny Centigrid style can. And make no mistakes . . . it is a Centigrid relay designed to meet the requirements of MIL-R-28776. Its ruggedness and proven contact reliability are industry bywords.

Ultraminiature Centigrid relays have proven extremely effective in applications where high board density and close board spacing are critical. Low power requirements make them exceptionally valuable for battery operation, and they have excellent RF characteristics up through UHF.

The new Centigrid is available in both general purpose (116C) and sensitive (136C) versions. Call or write today for complete information or applications ideas.

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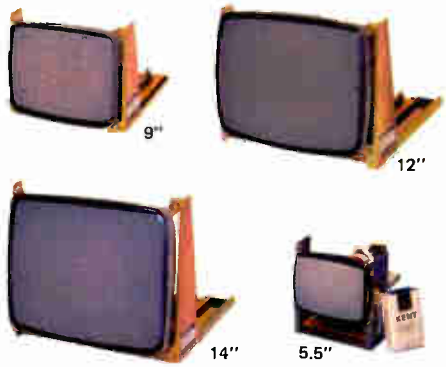

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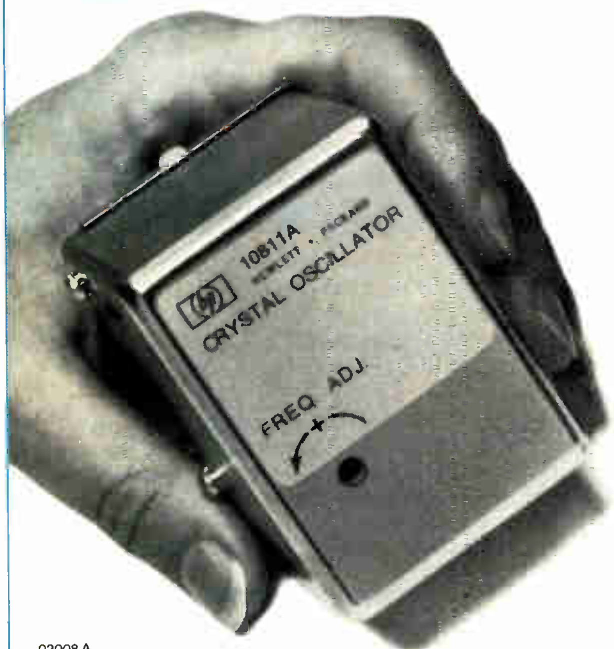
HP's Small Wonders.



Superb performance in new quartz oscillators.

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- ☐ Fast Warmup.
- ☐ Low Power Consumption.

HP's new 10811A/B Oscillators are designed for equipment requiring a compact, rugged, precision frequency source. Ideal for instruments, communication and navigation equipment and precision time keeping.

Look at the superb performance you get:

- Aging rate: <5 parts in 10^{10}/day
- Phase noise: better than 160 dBc at 10 kHz offset
- Warm up: within 5 parts in 10^9 of final frequency in 10 minutes
- Time Domain stability: better than 5 parts in 10^{12} for a 1-second averaging time
- Power consumption: approximately 2 watts, after warmup
- Output frequency: 10 MHz (10.23 MHz on special order).

Both are plug-compatible with HP's 10544 Series oscillators, and offer higher performance. Price is $800* (add $100* for B model with provisions for shock mounting). Call your nearby HP sales office, or write to Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304.

*U.S. domestic prices only.

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sheet and die-cut forms and in custom-designed shapes. Prices, which depend on size and form, are lower than silver-copper elastomers.

Chomerics Inc., 77 Dragon Court, Woburn, Mass. 01888. Phone (617) 935-4850 [477]

A polyurethane coating, HumiSeal 1A62 protects printed-circuit boards from harsh environments. It complies with Rule 66 air-pollution regulations and meets MIL-I-46058 standards. Applied by brushing, dipping, or spraying, the coating will cure in 24 hours at room temperature and can be soldered for repairs. A fluorescent tracer is provided to aid in the inspection of the pc boards under an ultraviolet light.

HumiSeal 1A62, once fully cured, is resistant to solvents and chemicals, is useful over the temperature range of −55° to +125°C, and withstands 3,000 V. It has a pot life of six months and a shelf life also of six months when stored in tightly sealed containers at room temperature away from excessive heat. It is available for immediate delivery in quart, gallon, and 5- and 55-gallon containers at $15 per quart, $39 per gallon, $34.10 per gallon in the 5-gallon containers and $33.40 per gallon in the 55-gallon drum.

Columbia Chase Corp., HumiSeal Division, P. O. Box 445, Woodside, N. Y. 11377. Phone (212) 932-0800 [478]

The Freedom-250 lead wire is insulated with perfluoro alkoxy (PFA) fluoropolymer resins, which are approved for use in food and pharmaceutical processing applications and are useful for portable appliances and electrical and electronic components operating in the 250°C range. Having only half the outer diameter of conventional wire constructions, it is a cost-effective alternative to standard insulations, such as asbestos, TAGT, TGS, and silicone rubber.

Freedom-250 has an excellent abrasion and cut-through resistance without a protective braid, a high dielectric strength, and a low coefficient of friction. These features, together with its compactness, make it superior to conventional wire designs for the 250°C range, according to the company. The wire is available in American Wire Gage sizes No. 26 through 10 with solid or stranded nickel and silver-plated copper or nickel conductor options. Specially designed configurations to meet specific customer requirements are also available.

Radix Wire Co., 26260 Lakeland Blvd., Cleveland, Ohio 44132. Phone (216) 731-9191 [389]

A solventless varnish, Permafil 73537 is a liquid polyester that can cure to an infusible solid. It has an extremely high bonding strength at elevated temperatures, making it suitable for use in small high-speed rotating armatures and to bond all types of coil structures.

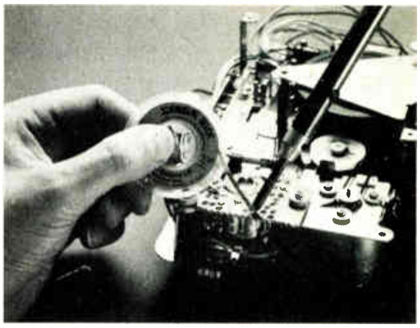
Permafil 73537 varnish is supplied as a two-component package that consists of a resin and catalyst in 5- and 55-gallon kits.

General Electric Co., Insulating Materials Department RV14-118-821, 1 Campbell Rd., Schenectady, N. Y. 12345. Phone (518) 385-3128 [479]

A desoldering wick is based on Xersin, a flux preservative that helps eliminate oxidation, a problem associated with rosin coatings. The wick is not affected by temperature or humidity and never requires any special storage conditions. It will not become brittle or flaky but remains pliable even after years of shelf storage.

The Xersin desoldering wick comes in 0.03-, 0.06-, 0.08-, and 0.10-in. sizes and is color-coded for easy identification. Available for immediate delivery, it is priced at $1.49 apiece.

Multicore Solders, Westbury, N. Y. 11590. Phone (516) 334-7997 [480]



Honeywell's Model 5600: The world's youngest 10-year old tape recorder.

Our Model 5600 tape recorder/reproducer was introduced almost a decade ago. So for the past 10 years, it has proven its reliability and performance where it counts most, not in our labs but in actual use.

At the same time, Honeywell engineers have gradually improved and upgraded the 5600 over the years to produce today's 5600C, an instrumentation recorder that represents the best of both possible worlds: Field proven reliability and state-of-the-art features.

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Find out for yourself what 10 years' worth of proven performance can mean in your application. Call Darrell Petersen at (303) 773-4835 for more details or write for technical information and a free, illustrated brochure: Honeywell Test Instruments Division, Box 5227, Denver, Colorado 80217.

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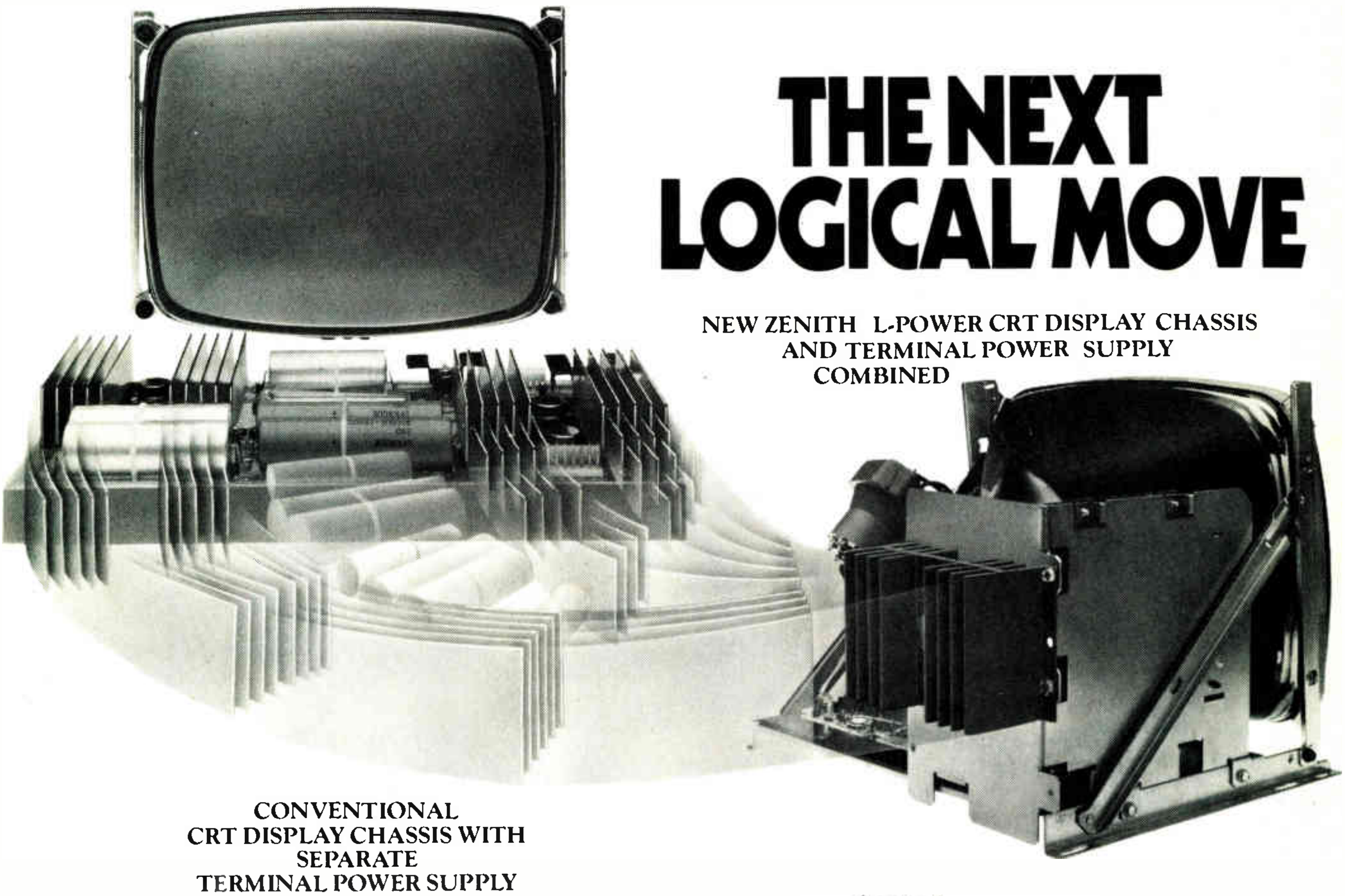
All Zenith CRT Displays: 5", 9", 12", and 15" are available with this innovative new L-Power system. For further information write: CRT Display Engineering Division, Zenith Radio Corporation, 1000 Milwaukee Avenue, Glenview, Illinois 60025, or call (312) 773-0074.



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Products Newsletter

Controller stays with high-density drives

In an attempt to keep up with the new generation of high-density storage-module disk drives, Interphase Corp. of Dallas is offering a new disk controller for $2,250 in single quantities. The SMD 2180-3 is an enhanced version of its 2180 disk controller and **can increase the serial data rate to 15 Mb/s.** The enhanced rate is necessary to remain compatible with higher-density drives like the Fujitsu Eagle, a 472-megabyte drive that spins at 3,900 rpm and has a serial data rate of 15 Mb/s.

Unit captures and displays weather data

Northern Video Graphics Inc. of Minneapolis has begun selling the Video-FX 1, a weather-satellite receiving system with a cathode-ray-tube display that is billed as a low-cost alternative to video systems currently costing about $50,000. **Complete with a 2-meter dish, a Z80-based processor, and a 12-in. black and white video screen** offering a resolution of 512-by-512 picture elements, the system sells for $6,995 and is designed to receive and display weather pictures transmitted directly from satellites operated by the U. S., Europe, and Japan.

Streamer backs up Q-bus disk systems

Joining the move to streaming-tape backup for Winchester disk drives, Plessey Peripheral Systems, Irvine, Calif., is unveiling its PM-CSV11A ¼-in. cartridge subsystem, designed for Q-bus disk systems. **The unit runs at 90 in./s and has a 20-megabyte capacity** with a 450-ft cartridge. Single-unit pricing for the drive, which has an 8-in. floppy-disk form factor, is $3,600.

Controller offers vast range of speeds

Anaheim-based Datum Inc.'s model 1050 tape controller is compatible with all versions of IBM's Series 1 systems, **but offers a wider range of speeds and speed mixtures than IBM systems.** The 1050 can handle speeds ranging from 12.5 to 125 in./s and lets users determine combinations. The pricing is 30% lower than IBM's, at $7,375 for dual-density formats.

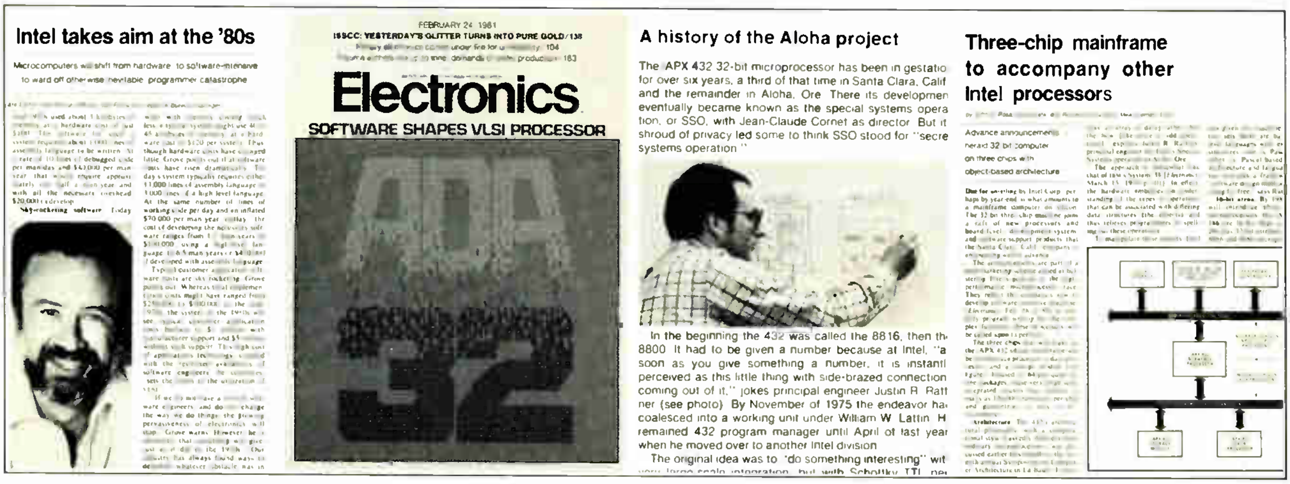
8085A and Z80A get signature analysis

Models 5001C and 5001D microprocessor exercisers that troubleshoot products based on the type 8085A and Z80A microprocessors **are new in the Hewlett-Packard line of signature-analysis troubleshooting equipment** that was introduced by the Palo Alto, Calif., firm over a year ago [*Electronics* June 19, 1980, p. 17]. These instruments can use signature analysis even though the exercise routines and other provisions for signature analysis were not initially designed into the product. The new models are deliverable in 45 days at $900 for the 8085A version, and $1,075 for the Z80A model.

Prices continue to fall . . . and rise

Digital Equipment Corp. of Maynard, Mass., has reduced prices for add-on MOS memory products **by as much as 60% for PDP-11 computers and 33% for VAX computers,** reflecting the reduced cost of semiconductor components and increased manufacturing efficiencies. In the same announcement, however, DEC increased hardware and software prices an average of 2½%, with older products reflecting increases as much as 7%. Piiceon Inc., San Jose, Calif., has also initiated an across-the-board price reduction of up to 30% on all of its board-level products, hoping to further stimulate the market for S-100 bus-compatible products.

Important editorial



Electronics worldwide editorial announces and interprets all the important technological developments.

Take the Aloha Project.

The first hint was given in 1980 when Intel invited Electronics to hear what its top management was planning for the decade. In Electronics' February 28 issue, John Posa, our solid state editor, let the world know of Intel's vow to develop an operating system in silicon which would integrate a high-level language to help compensate for the shortage of software engineers.

In Intel's Aloha, Oregon facility, tight-lipped designers were progressing with this five-year-old project, dubbed the Special Systems Operation or "SSO." The outcome would be the iAPX 432—the first 32-bit microprocessor to integrate a high-level language. The language? ADA—the Department of Defense's new standard programming language.

Even before the iAPX 432 was hinted at, Electronics was covering the competitive 16-bit microprocessor arena with reports on Intel, Motorola, Zilog, TI, Fujitsu and Philips. In May, we got a break on the "SSO" project.

While covering the 7th Annual Symposium on Computer Architecture in La Boule, our Paris News Bureau recognized Intel's principal engineer for the "SSO," Justin Rattner, leading a discussion on the iAPX 432 philosophy. New York was contacted and John Posa investigated. He added this new information to what he had already gathered at an earlier visit to the Aloha Project as the first journalist ever to be admitted to the "SSO." Result: our May 22 issue carried the story quoting Rattner's advance announcement.

In November, Electronics reported Intel's plans to hold three invitation-only sessions to introduce the iAPX 432. And finally, on February 24, 1981, Electronics published the "full disclosure" special report on "SSO," authored by its designers, Justin Rattner and William Lattin.

Important editorial? You bet. The iAPX 432 evolved in the pages of Electronics. The only place important people could have read about it was in Electronics magazine.

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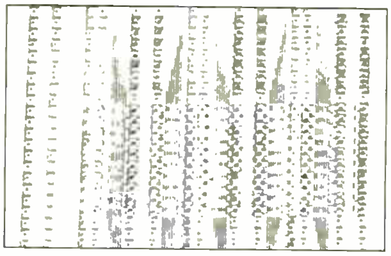
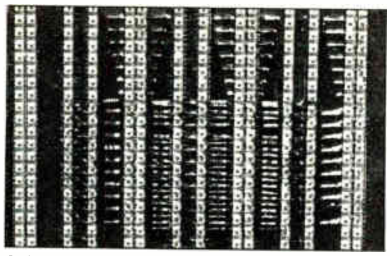
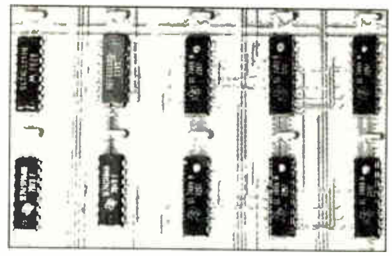


Detail of a K6 wired board



A K6 board wired on both sides, ready for component insertion.



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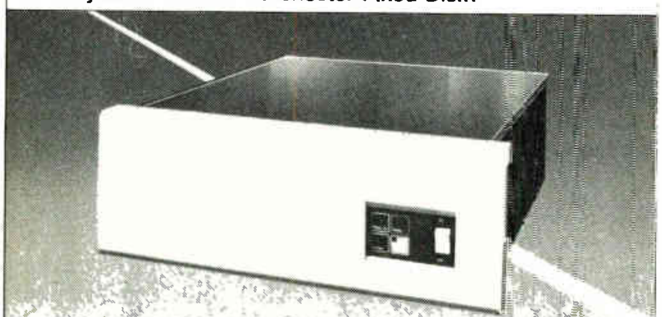

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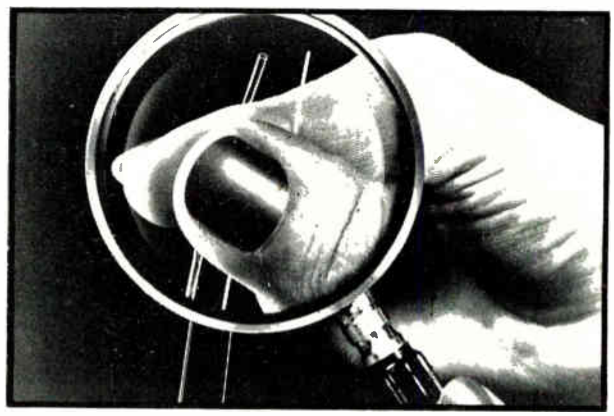

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Teleprinters described. Teleprinters, a Data Decisions report, details the features of communications printing terminals. The report presents specifications on 244 teleprinter models that are produced by 80 vendors. In addition, the products handled by 43 dealers and distributors are identified. Models covered include all keyboard or receive-only printers that can be directly coupled to communications facilities or to cathode-ray-tube terminals via an RS-232-C or current-loop serial interface. A free executive summary is available; the complete report is $25 from Data Decisions, 20 Brace Rd., Cherry Hill, N. J. 08034. Phone (609) 429-7100 [422]

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Pressure transducers. A technical paper, "Basic Advantages of the Anisotrophic-Etched, Transverse Gage Pressure Transducer," explains the uniquely designed diffused silicon diaphragm at the heart of Endevco's miniature pressure transducer product line. The paper, designated TP 277, discusses the advantages of sculpturing the diaphragm (to concentrate stress), anisotrophic etching, the transverse gage approach, and attachment of a heavy silicon ring. For additional information, contact Endevco, Rancho Viejo Road, San Juan Capistrano, Calif. 92675. Phone (714) 493-8181 [424]

Apple resources. The Apple Resource Directory is a complete where-to-find-it book of hardware, boards, accessories, and peripherals for the Apple computer. The second edition of this directory includes product information, photos, pricing information, and complete descriptions of the items featured, as well as manufacturer names and addresses. It also lists reference manuals, publications, newsletters, magazines, user groups and clubs and time-sharing systems for the Apple. The $5.95 directory is available from local Apple dealers or from WIDL Video, 5245 West Diversey, Chicago, Ill. 60639. Phone (312) 622-9606 [425]

International standards. A new comprehensive pocket-sized handbook from ACDC Electronics describes the spectrum of international and domestic regulations concerning design of electronic equipment, safety, and electromagnetic interference. Specifications include those from the Institute of Civil Engineers, International Commission on Rules for the Approval of Electrical Equipment, Verband Deutscher Elektrotechniker, Underwriters Laboratories, Military Standards, and the Federal Communications Commission. For a copy of the handbook, contact ACDC Electronics, 401 Jones Rd., Oceanside, Calif. 92054. Phone (714) 757-1800 [426]

Apple software. Vanloves Apple II/III Software Directory contains over 3,000 software entries in 33 sections divided by subject. The directory, designed to aid the microcomputer user who currently uses CP/M in the selection of software and peripherals, lists a myriad of available programs, their publishers, and prices. A software hotline, (800) 255-5119, is available to directory customers who have software, hardware, or peripheral questions. The directory sells for $19.95 plus $1.50 postage and handling from Vital Information Inc., 7899 Mastin Dr., Overland Park, Kan. 66204. Phone (913) 381-1818 [427]

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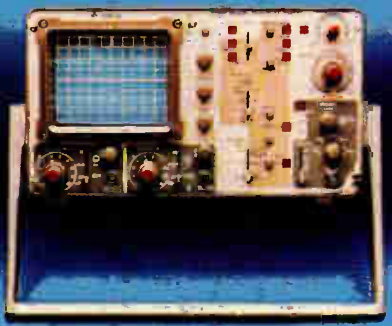

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Career outlook

Passing the hat for schools

Noting that the demand for engineers in the electronics industries is expected to outstrip the supply by 100,000 engineers by 1985, the American Electronics Association has decided to come to the aid of American education. Last month it created an engineering education foundation, tossing in $50,000 of its own operating money, and began to pass the hat among its 1,500 member companies hoping to raise $30 million to $50 million.

The plan is to use the money to help create more qualified engineers. A blue-ribbon panel appointed by the AEA will decide how to allocate the funds, once they are received.

Ideas under consideration include the creation of engineering faculty chairs, the providing of graduate fellowships to engineering students who pursue careers in education, and the funding of engineering faculty fellowships. Other possibilities are the guaranteeing of summer jobs to engineering faculty and offering engineering teachers paid one-year jobs at electronics companies so they can keep pace with the latest changes in technology.

The AEA is asking its member companies to contribute 2% of their annual research and development budgets to the cause. Such budgets are usually 8% to 10% of annual sales.

Programs already in place between individual companies and universities would be credited toward the 2% figure. Equipment could also be donated by companies in lieu of cash contributions.

The AEA also plans to contribute 2% of its annual membership dues. The association's chances of obtaining at least some percentage of its goal seem good, since its board, which consists of 41 top executives of electronics companies, approved the measure unamimously.

Lobbying, too. A significant part of the foundation's efforts would be the lobbying of state legislatures to raise the salaries of engineering faculty in state-run colleges and universities. The AEA itself also plans to lobby at the Federal level. In its attempt to help schools, the foundation would take a regional approach, with the first area task force to be set up around San Francisco to aid colleges and universities there.

The announcement by the association of its proposed foundation follows closely its release of figures supporting its oft-stated view that there is a severe shortage of engineers. The AEA's refrain is the estimate that has gained widest recognition in the non-engineering world.

New data shows that U.S. electronics companies will create 198,191 jobs for electronics and computer-science engineers with bachelor's degrees between now and 1985. However, American colleges will graduate only 69,315 degree holders to fill those slots, according to current projections.

Those numbers do not include attrition, says the AEA, and reflect an annual 14.9% annual compounded growth rate in demand. The calculations are derived from the association's new survey, "Technical Employment Projections: 1981–1983–1985." **-Martin Marshall**

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