JULY 14, 1981

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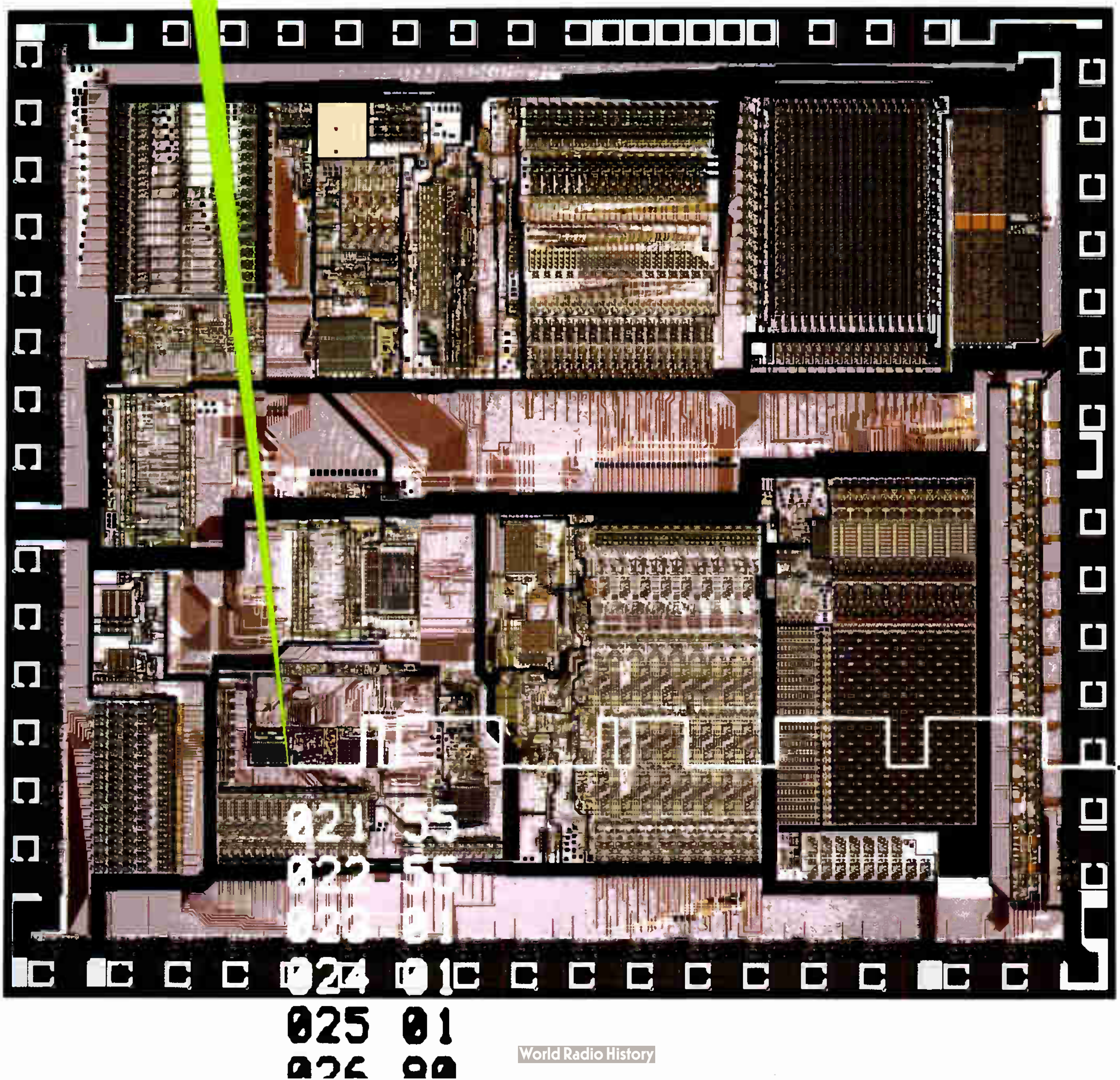

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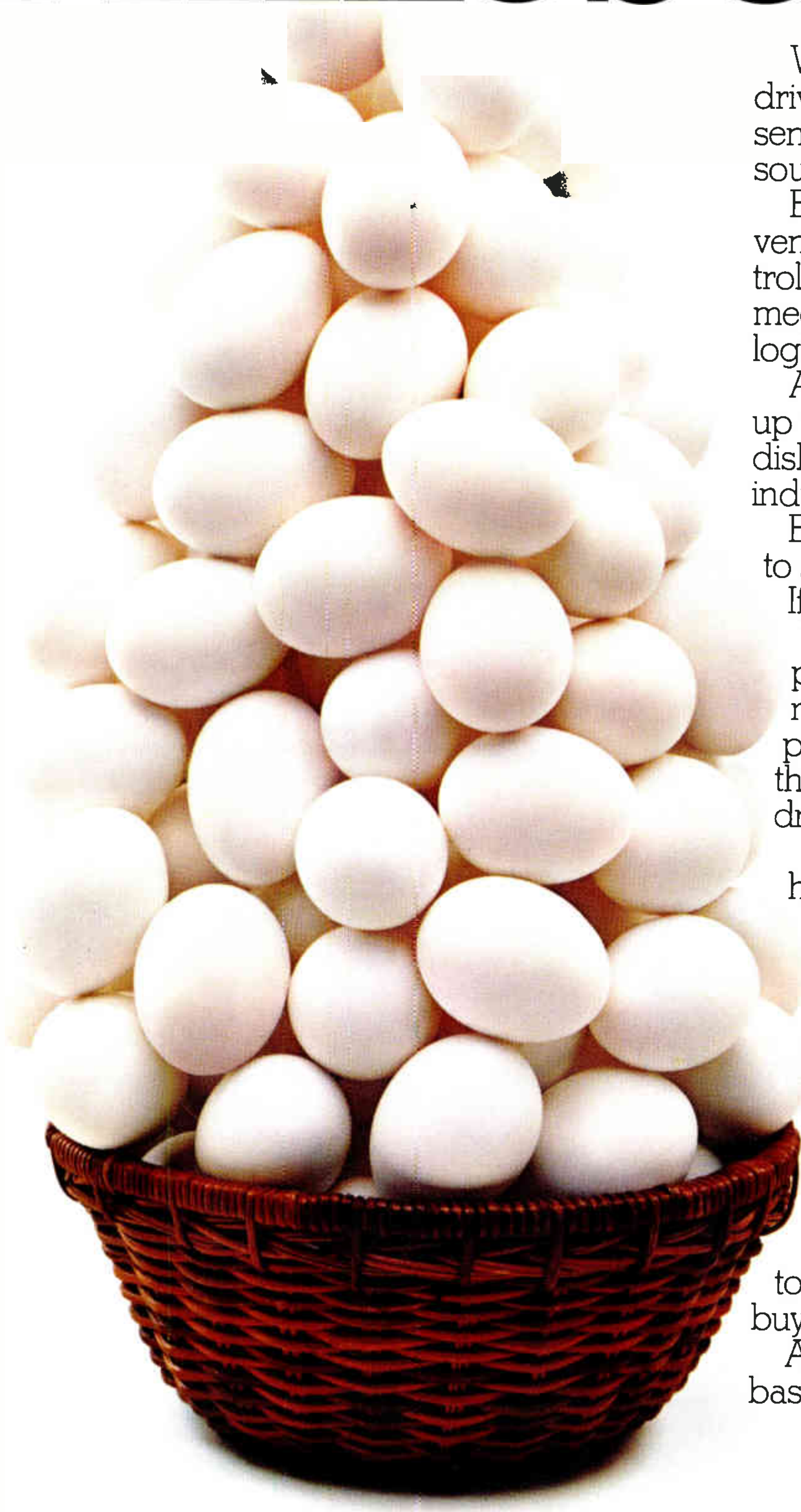

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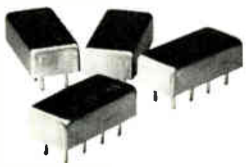
AT-6	6	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1	1W
AT-10	10	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1	1W
AT-20	20	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1	1W



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Electronics

The International Magazine of Electronic Technology **Vol. 54, No. 14 • July 14, 1981**

105 Technical Articles

Electronics

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Highlights

Electron-beam probing tests VLSI chips, 105

A dynamic testing technique that adds a logic analyzer to a sampling electron microscope can plot logic-state maps of complex very large-scale integrated circuits. The scanning electron beam utilizes voltage-contrast representation of the logic states—a technique that it can also apply to the measurement of analog waveforms.

The cover design is by Associate Art Director Charles D. Ciatto; the T88000 microprocessor photograph is courtesy of Toshiba Corp.

U. S. IC equipment makers build in Japan, 89

Since market domination of Japan is being eroded, U. S. makers of integrated-circuit production equipment are setting up joint ventures and *in situ* subsidiaries in order to blunt local competition.

Time-domain reflectometry moves into the digital world, 113

An algorithm for a desktop computer lets a time-domain reflectometer determine the impedance of nonuniform communication paths like those found in high-speed backplanes and printed circuit boards.

Single chip performs 64-bit correlations, 118

Operating at speeds over 15 megahertz, a 64-bit monolithic digital correlator can be used in such cross- and auto-correlation tasks as code correction, data synchronization, and time-delay measurements.

Affordable GTO thyristor tackles high-voltage switching, 129

A gate-turn-off thyristor can perform high-power, high-frequency switching beyond the reach of most power semiconductors. Advanced processing and circuit-design techniques have produced a high-yield, inexpensive device that interfaces readily with logic-level signals.

Automated design tools hook up logic arrays, 132

To set routing patterns for a new family of logic arrays, the designer can rely on the manufacturer's design-automation system, in which manual processes constitute less than 1% of the input.

Holography yields a 3-d bar-code scanner, 139

By wrapping a three-dimensional pattern of laser beams around a retail item, a holographic scanner can read bar codes. The 3-d pattern eliminates the need to line up the bar code precisely with the scanner.

And in the next issue . . .

An in-depth look at memory redundancy . . . a special report on intelligent multiplexers . . . a three-dimensional graphics display.

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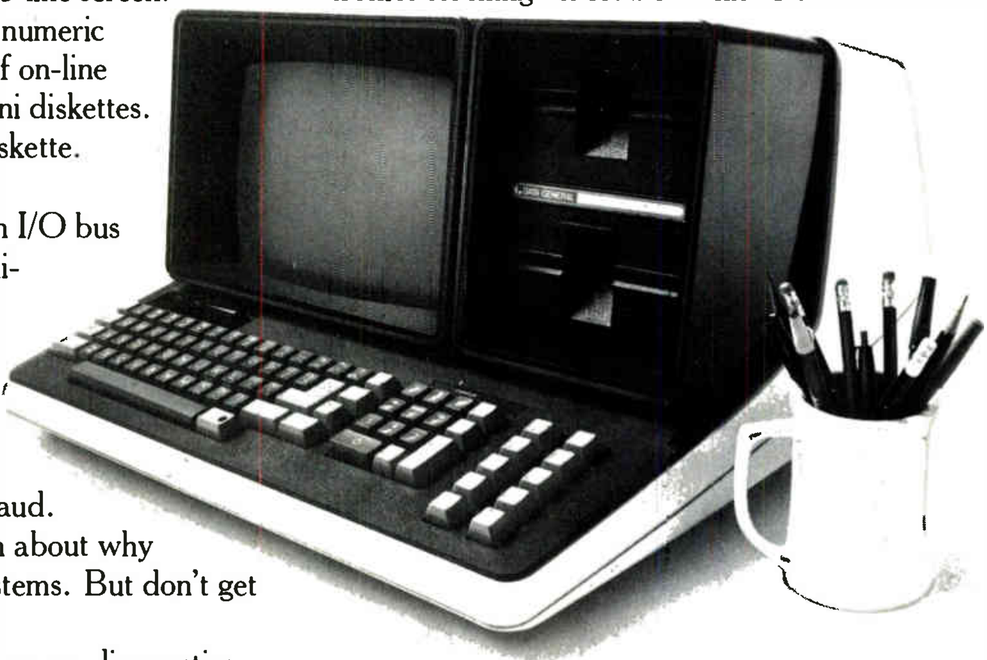

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Publisher's letter

Testing the operation of integrated circuits during the development stage has become an increasingly knotty problem as the level of integration ramps up, and it has long been apparent to most chip makers that the tools and techniques applied to the development of large-scale ICs will be insufficient for very large-scale integration. Still, West Germany's Siemens is one of the few to have invested from the very beginning in a technique suitable for VLSI: loadless, contactless IC testing using electron beams.

"The basic idea for electron-beam dynamic circuit testing by voltage-contrast methods has been around ever since integrated circuits appeared on the scene," says Eckhard Wolfgang, head of the Siemens development effort and one of the authors of the article on it that starts on page 105. In 1956, the University of Cambridge in England proposed and tried out voltage-contrast test techniques on ICs. "But the road from simple testing to complex circuit analysis as performed today was a long and arduous one," notes the 39-year-old, Austrian-born Siemens researcher.

What originally triggered the company's effort was a film shown by a Canadian IC producer that illustrated the functioning and testing of circuits using voltage-contrast principles. "Prodded by our own components people, who wanted a similar but more refined test technique, we embarked on the development project in early 1973," Wolfgang remembers.

Of note is the fact that the Munich-based firm pursued the multimillion dollar project continuously and tenaciously, with the top Siemens management fully behind it. That, Wolfgang adds, contrasts with the attitude of some U. S. firms that were engaged in similar work but discontinued it after a few years, "probably because they did not see an immediate need for nonmechanical test methods. But with the advent of VLSI, that need has become a pressing one."

But the Siemens manager has observed a recent revival in interest in the technique. "During my two visits to the U. S. this year, I have not come across a semiconductor producer who isn't working on or with E-beam test systems—or planning to do so." There is no doubt in his mind that such systems will eventually become standard tools and should prove their worth particularly with 32-bit microprocessors and with circuits featuring structures finer than 2 micrometers.

Packaging and production editor Jerry Lyman, who worked with our Frankfurt bureau chief John Gosch in developing the article, also sees a bright future for dynamic electron-beam testing. He notes that the first commercially available equipment in this area has just come on the market from a small British company, Lintech Instruments Ltd. [*Electronics*, June 30, p. 73]. Also, "many U. S. companies—Intel, TI, IBM, and others—are already using the technique on a static basis," he says, "and it's just a matter of time before they advance to the dynamic testing approach."

At Siemens, electron-beam voltage-contrast testers are already on the way to becoming standard. Four systems are now in use, two at the research labs and one each at the components and communications divisions. They test dynamic random-access memories of up to 64 K, bipolar RAMs, emitter-coupled- and charge-coupled-logic devices, microprocessors, and microcomputers, as well as custom-designed circuits for the company's data-processing and communications divisions.

Manning the four systems are eight test engineers, Wolfgang says. As for the future, testing IC functions is not the only job the electron-beam systems can handle. Another is investigating surface-acoustic-wave devices [*Electronics*, Aug. 28, 1980, p. 73].

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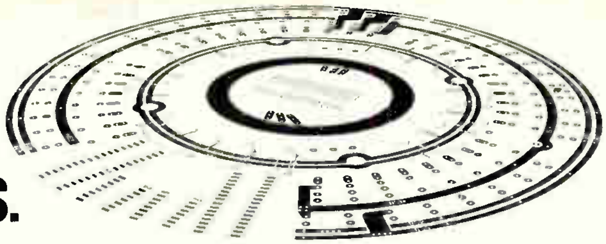

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Readers' comments

Part of the parade

To the Editor: The recent article "Major firms join Unix parade" in your April 7 issue [p. 108] provided very useful information on the Unix operating system developed by Bell Laboratories. The virtues of Unix and its growing popularity deserve such close attention.

However, your list of companies authorized to sell Unix sublicenses omitted Interactive Systems Corp., which was the first commercial sublicenser of Unix systems.

Interactive's IS/1 system is a significant extension of Unix that retains Unix compatibility. It operates not only on Digital Equipment Corp. PDP-11 computers, but as a subsystem under the company's VAX/VMS operating system as well. In addition, Interactive recently concluded an agreement with Onyx Systems Inc. to provide IS/1 as the standard Unix system for the Onyx C8002 system: our IS/1 for the Onyx C8001 is currently available.

Dwayne C. Lowry
Interactive Systems Corp.
Santa Monica, Calif.

Yankee ingenuity

To the Editor: Your special report, "How Japan's chip makers line up to compete" [June 2, p. 117], observed that a double-diffused memory cell innovation came from the Nippon Electric Co. We wish to point out that the memory cell structure described originated in the United States and is covered by U. S. Patent No. 3,919,569 issued to us on Nov. 11, 1975. A corresponding Japanese patent, No. 941480, was issued on Feb. 20, 1979. Both of these patents have been assigned to International Business Machines Corp., Armonk, N. Y.

F. H. Gaensslen and P. J. Krick
IBM Corp.
Yorktown Heights, N. Y.

Correction

In "How Japan's chip makers line up to compete" (June 2, p. 117), a wafer-stepping lithographic process for 256-K RAMs was cited as having a 1:1 projection ratio. The correct ratio is 10:1.

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Editorial

The new science adviser

The designation of George A. Keyworth as science adviser to President Reagan does not serve to encourage those who hold the view that the understanding and encouragement of innovation at the highest Government levels and the fostering of technology on a broad front are essential to the economic health of the nation.

Keyworth is little known outside the important but narrow confines of the military nuclear establishment. He received his Ph.D. from Duke University in 1968, and most of his career has been involved with nuclear physics, including laser confinement fusion development at Los Alamos National Laboratory. When designated, he was head of the laboratory's Physics division.

Although Keyworth may provide some surprises, it is hard to see how his background, conspicuously bereft of industrial experience, can prepare him to steer the Administration towards an intelligent policy on important nonmilitary technological issues. Indeed, he has been quoted as listing first among the major technological issues facing the nation national security, preservation of a credible nuclear deterrence, and energy research and development. At the same time he has expressed admiration for "the Administration's attitude toward technology"—an attitude that is responsible for significant cuts in science and engineering education and does not reflect enlightenment on how to maintain America's technological lead by providing incentives for research and development.

Of course, the goals Keyworth cites are essential. But concentrating our national technological resources on these areas alone would be disastrous. For a science and technology adviser, a more balanced long-term view of the importance of high technology in reaching, say, employment, balance of trade, and productivity goals is also required. Keyworth may ultimately show that he holds such a balanced view, but what is known about him so far is not reassuring.

Where the U. S. holds sway

Amid the dark talk of the narrowing United States technological lead—even the daily newspapers are running Sunday features on the subject—it might be enlightening to read two articles in this issue. They offer a good look at the other side of the coin.

The first, on page 89, details the strategies being followed by U. S. makers of semiconductor manufacturing equipment to consolidate their domination of that market in Japan. While they have seen some erosion, the indication is that they have no peers when it comes to the highest technologies in their business. The other article, on page 101, reports on a survey of world computer markets. That survey concludes that Japanese manufacturers will have only 8.3% of the markets by 1985 and that their growth rates are slower than those of many of their U. S. rivals.

What those two stories make clear is those the U. S. is still the world leader in most areas of electronic technology and will continue to remain so. While that leadership is threatened most seriously in a visible and important marketplace—semiconductors, particularly 64-K random-access memories—in other, equally sophisticated electronics market sectors, American design and software ability are unequaled. Without those strengths there can be no technological dominance.

People

Roach to lead Tandy into speech-learning aids

Maintaining a bridge between state-of-the-art technologies and the home will be the No. 1 challenge of the decade for consumer electronics manufacturers, says Tandy Corp.'s John V. Roach. As technologies continue to grow, so does the demand for up-to-date consumer electronics, observes the company's president and new chief executive officer.

To meet that demand, Tandy—the reigning champion of U. S. home computer markets—will soon be spreading its efforts into speech synthesis, Roach says. "A talking clock will appear in this year's catalog, and it will be only the first of many Tandy synthetic-speech products," says the 42-year-old executive. "This will, of course, lead to other speech technologies in the decade, like speech recognition."

The Fort Worth, Texas, company also plans to take on its neighbor—Texas Instruments Inc. of Dallas—in the hand-held, speech-learning-aid market. Within a year, Roach says, these products will begin showing up at Tandy's Radio Shack stores. TI markets speech technology in products like Speak 'n' Spell and Speak 'n' Math.

Roach, a native of western Texas, was named Tandy president in October 1980 after serving as executive vice president of Radio Shack for two years. He joined the corporation in 1967 and holds both a master's and bachelor's degree in business administration from Texas Christian University in Fort Worth. In becoming Tandy's CEO this month, Roach replaces Phil R. North, who remains chairman of the board.

"We sit in a unique position," says Roach, referring to Tandy's vast experience in consumer electronics. "We've been involved in every aspect of the technology and business, from laboratory to the living room." Tandy will continue to see itself as a vital link between high technology, the home and—in cases like the TRS-80 model II microcomputer—small business.

Speech talk. Tandy's John Roach says firm will take on TI in speech-synthesis market.

"In terms of overall business, Radio Shack sales have boomed in the past nine months," he says. "Not only are the highly visible products doing well, but many of our standard product lines are doing well—like record players and tape recorders." Sales for the fiscal year ended June 30 were up 20%, compared to the previous year. "And that increase is 5% higher than what we experienced in the past three or four years."

Van Tassel to show NCR how to sell semiconductors

Since the day some 16 months ago when James H. Van Tassel took over as vice president of NCR Corp.'s Microelectronics division, a big chunk of his time has been spent grooming the operation for entry into the merchant semiconductor business. "That was part of the deal. NCR wanted to enter the general semiconductor market as a supplier of high-technology devices," the 54-year-old executive recalls.

Last month [*Electronics*, June 30, p. 46], those intentions were made public by NCR with the announcement that it will begin selling nonvolatile memory chips and semicustom logic devices on the open market. The move is a first for the Dayton, Ohio, computer-systems manufacturer, whose chip production to

Circle 15 on reader service card

People

In the market. James H. Van Tassel is leading NCR into the merchant IC business.

date has gone primarily into its own products.

Van Tassel concedes that the conversion from captive into merchant component supplier will not be a simple task. But with 19 years at Texas Instruments Inc., he is well-equipped for the job. After joining TI in 1960 with a master's and Ph. D. degrees in chemistry from Texas Tech University, Van Tassel's tour with the Dallas company included a stint as general manager of MOS for internal consumption. He also got plenty of merchant-market experience later on as general manager of operations for the TMS-1000 4-bit microcomputer.

Learning to sell will be among the toughest challenges faced by the Microelectronics division staff, Van Tassel notes. "We have been dealing at the engineer and application level internally for a long time, but we don't have experience at the salesman–purchasing-agent level." The division will not rely upon the existing NCR sales force, but is setting up a separate network of 150 technical field representatives.

One thing the division will not have to learn is the importance of schedules. "You wouldn't believe how nasty delivery schedules can be when both the sender and receiver report to the same boss," Van Tassel quips. On-time delivery skills and over 10 years of quality and reliability standards as a captive NCR component supplier will serve the division well on the outside, he figures.

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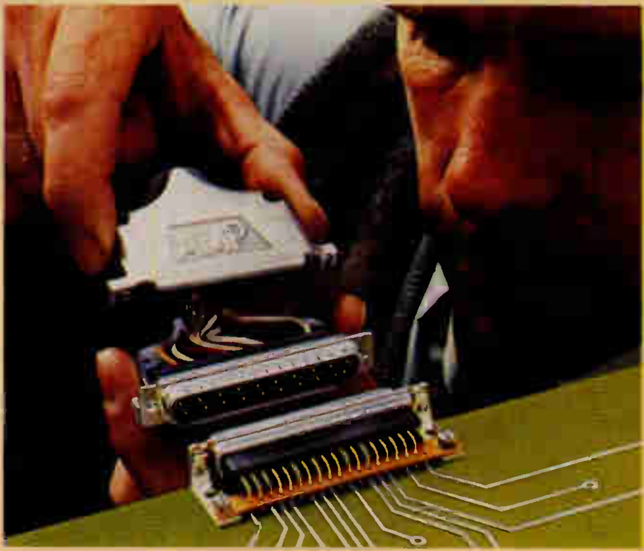

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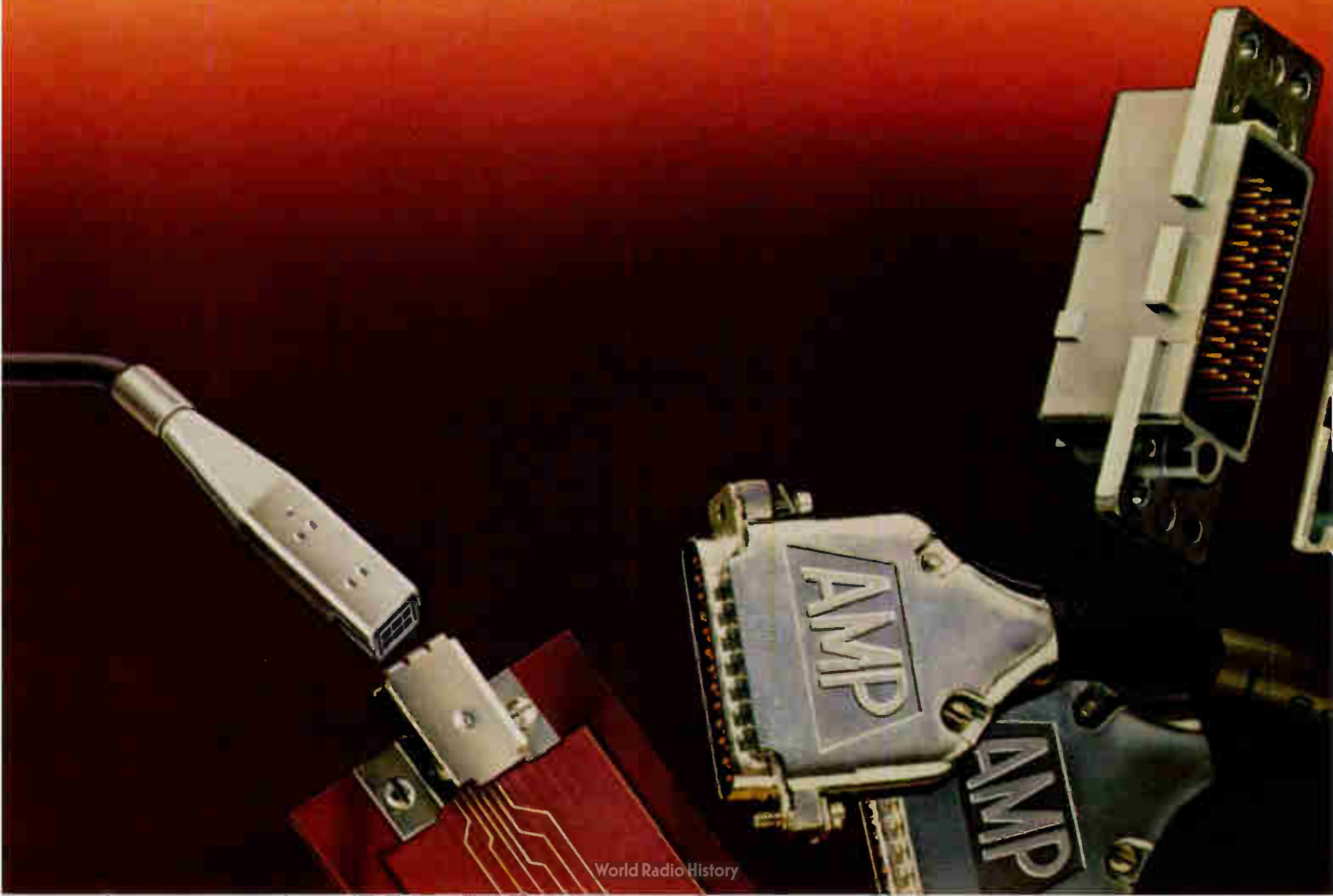

If you're still looking for the best 8" floppy

Go international or go under

by Jerry R. Crowley

president and chief executive officer, Oki Semiconductor Inc., Santa Clara, Calif.

A new spirit is emerging today among semiconductor companies that is multinational in outlook and in operations. Because electronics is now an international technology in which no one country can claim absolute leadership, the companies that form the electronics industry must be prepared to adopt an international viewpoint.

Having been involved in two hemispheres of the semiconductor world—first with Motorola, Signetics, and National Semiconductor and now with Japanese-owned Oki Semiconductor—I view the multinational movement as a good one. Moreover, I think that the trend will work to the advantage of U. S. companies.

Once, it was primarily U. S. companies that were investing and marketing abroad. But times have changed. The world has become an interdependent, multichannel network, with foreign investments in our land becoming more and more evident. We are seeing a realignment of the traditional market structure. Today, the Free World alliance needs to strengthen its bonds with active, progressive trading partnerships and cooperative ventures.

I am not really advocating anything radically new. In fact, these things are already happening, and the direction is not all one-way. Recall these examples: Texas Instruments adds a third wafer fabrication facility in Japan and commits to a manufacturing plant in Singapore; Motorola Semiconductor forms a 50:50 joint venture with Toko for wafer fabrication in Japan; at the same time Mostek heads for Ireland to put down an integrated-circuit production plant; and Siliconix does the same in Wales.

In a sense these internationally oriented companies are reaching outside their traditional territories to find solutions. They are tapping resources—engineering talent, production efficiency, not to mention markets—that are not limited by national boundaries. The steep demand forecast for semiconductors (present slow market conditions notwithstanding), coupled with an anticipated shortage of engineers, has encouraged companies to use international assets. In doing so, managements have had to bridge cultural differences, becoming involved in long learning experiences but finding new sources of ideas and new ways of managing.

These semiconductor firms are filling a void brought about by the decreasing number of purely merchant suppliers and the increasing number of captive or semicaptive producers. Examples of the latter types of relationship would be Philips/Signetics, Honeywell/Synertek, United Technologies/Mostek, Schlumberger/Fairchild, and more recently, General Electric/Intersil.

Bolstering the independents

If we're heading for surging demand from big systems houses and limited supply from the independents—which I'm convinced is the case—how do we close the gap that could develop between semiconductor output and semiconductor consumption? One way is for all of us to take a more liberal view of multinational solutions. There is a need for a group of emerging semiconductor firms, regardless of national origins, to help alleviate the IC capacity crunch in the years ahead. It's the best way I know to avert lost systems markets abroad.

By being an American-run operation in a Japanese-owned company, Oki is a good example of how engineering expertise and management style can be blended successfully. We have the advantages of American know-how in software design, marketing, and technical field support backed by Japanese production capability and long-term planning. Without the intense pressure to deliver immediate results on the profit-and-loss statement that often drives American managers, we can take a more considered view of financial management.

The communication is remarkably good. We have learned that with the international pervasiveness of semiconductor technology, economics is changing the famous NIH (not invented here) attitude.

Electronics *will periodically invite the expression of outside views on this page concerning issues of importance to the electronics industries.*

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Serilization			
Electrical Test +25°C Read & Record	Electrical Test +25°C		Electrical Test +25°C
Burn In Test Method 1015 Cond. B 240 hrs. at +125°C	Burn In Test Method 1015 Cond. B 160 hrs. at +125°C		Burn In Test Method 1015 Cond. B 160 hrs. at +125°C (see note 2)
Post Burn In Electrical Parameters Read & Record at +25°C	Final Electrical Test at 25°C	Final Electrical Test at 25°C	Final Electrical Test at +25°C
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Seal Method 1014 Condition A_1 & C			
Static Test at +25°C and Min/Max Temperatures	Static Test Min/Max Temperatures		Static Test Min/Max Temperatures (see note 1)
Dynamic Tests and Switching Tests at +25°C	Dynamic Tests and Switching Tests at 25°C		
Functional 25°C Test	Functional 25°C Test	Functional 25°C Test	Functional 25°C Test
Radiographic (X-Ray) Method 2012			
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1. Temp Testing Performed As Required To Guarantee Data Sheet Specifications.
2. Burn-In Performed As Required To Stabilize Devices With Internal References.

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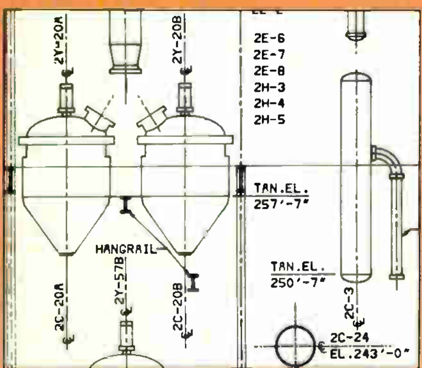

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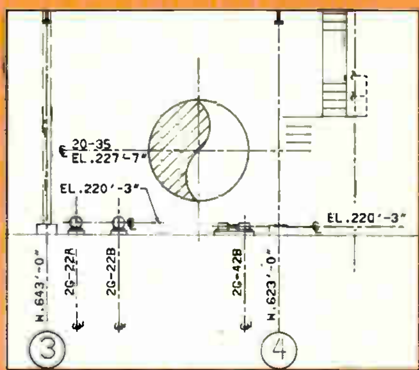

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Electronics newsletter

GenRad plans major new entry in board-test systems

An automated board test system that breaks new price-performance ground is in the works at GenRad Inc., with announcement possible as early as this autumn. The unit will test analog and digital circuitry more effectively than present models, as well as be fast enough to accommodate emitter-coupled logic and pin counts many times more than GenRad's current top of the line 2270 tester, which handles up to 480 pins. The new units will be software-compatible with 2270s. **They will test highly complex boards without the throughput problem or other penalties usually associated with high-speed, high-complexity testing.** With average system prices expected to stay well below $500,000, the new system should "strengthen our position in the minicomputer test market," notes a GenRad spokesman. It reopens a market in which the Concord, Mass., firm appeared to slip earlier this year when it lost a major board-test contract with Digital Equipment Corp.

Harris readies 16-K C-MOS PROM

Watch for early announcement of a 16-K complementary-MOS programmable read-only memory using 2.5-μm geometry from Harris Corp.'s Semiconductor Group in Melbourne, Fla. The firm already makes fuse-link PROMs in 1- and 4-K versions and **plans to have 32- and 64-K units ready within a year, with the latter using 2-μm geometry.** Harris sees its nonbipolar PROM family as competing with the MOS ultraviolet-erasable PROMs—though its C-MOS parts require 20% more real estate, lower in-house testing cost lets the firm price them competitively. What's more, Harris spokesmen say the firm will leapfrog E-PROMs, moving directly to electrically erasable PROMs within two years.

Adapter converts scope or multimeter into fiber-optic tester

The first product from newly formed Fotec Inc., Charlestown, Mass., will be a $250 adapter for standard test instruments, such as oscilloscopes and multimeter, that allows signal tracing through fiber-optic systems. Though the unit makes only pseudo–direct-current measurements, **it will be far easier to use and, according to its developers, far less costly** than the photometers and time-domain reflectometers at present available. The 1.5-by-3-by-5-in. system will have outputs scaled to 1 V per milliwatt or to 1 V per microwatt, thus enabling fairly sensitive attenuation measurements, as well as simple continuity checks.

Commercial deep-water fiber-optic link set in Northwest

In another first for fiber optics, Pacific Northwest Bell will install a commercial deep-water cable link in October. Faced with the option of putting down another copper cable, the telephone company chose to go with fiber optics for long-term cost and capacity reasons. **Two 36-fiber cables made by Siecor Inc. of Hickory, N. C., will be laid 150 ft under Lake Washington near Seattle** as part of what will be a 78-mile link. The underwater run is 11,000 ft.

Superconductivity at room temperature making progress

"It looks like we're on the right track" toward possible room-temperature superconductivity, reports Fred W. Vahldiek, a materials research engineer at Wright-Patterson Air Force Base in Dayton, Ohio. **Preliminary tests conducted during the last several months show that specially grown thin-film titanium boride crystals repel magnetic flux.** This property, known as the Meissner Effect, is a prerequisite for superconductivity, Vahldiek says. He is currently planning additional tests aimed at measuring critical magnetic field strengths. As reported earlier [*Electronics*, Oct. 9, 1980, p. 41], Vahldiek came upon the superconducting material's potential while trying to obtain ductility from titanium boride crystals, which are ordinarily extremely brittle.

Mitel rushes codec filter to market

Convinced that many telephone equipment designers cannot wait for single-chip codec filters to arrive, Mitel Corp., Kanata, Ont., has pushed ahead with the first parts of its MT8912 monolithic filter. Made with the Canadian firm's double-polysilicon ISO^2 complementary-MOS process, **the chip is pin-for-pin-compatible with Intel's 2912 and has a built-in power-line rejection filter as well as an amplitude correction on its receiving filter.** It dissipates 25 mW with power amplifiers on, 20 mW when off. Mitel believes the 16-pin package, which includes both the transmit and receive filters needed by pulse-code modulation codecs, fills a need even though work is continuing apace on a codec with filters on one chip.

Motorola adding wafer plant, opens design center

With an initial investment of $60 million, Motorola Inc.'s Semiconductor Group plans to break ground later this year for a new silicon-wafer manufacturing plant in Chandler, Ariz., south of its Phoenix headquarters. The first production module and a service corridor to which future modules will be attached will be completed in 1982. **Meanwhile, Motorola marks the opening of its first regional design center** in San Jose, Calif., with the extension of its Macrocell emitter-coupled-logic gate arrays into the TTL-compatible arena. Macrocell advanced low-power Schottky TTL will be available through the computer-aided-design center, which opens its doors this week.

Addenda

Real earnings for U. S. members of the Institute of Electrical and Electronics Engineers have fallen behind 1978 levels, according to a survey released last month by the institute. **Salaries have increased from a mean of $31,680 in 1978 to $36,659 in 1980, a 15.7% gain** in the 24 months since the last survey. The Consumer Price Index, however, has jumped 27.3% in that period. On the plus side, involuntary unemployment among members is a tiny 0.5%. . . . With Out-Voice, another product has entered the market for store-and-forward voice messaging systems. A new Chicago-based company, Voice and Data Systems Inc., says **its system can digitize and store 80 hours of voice messages and can be set up to handle from a hundred to several thousand users.** Out-Voice, which interfaces to existing private branch exchange systems, starts at $90,000 for a 100-user system and goes up to about $340,000 for a system for more than 1,000 users. . . . Another energy company, Standard Oil Co. of Ohio, is backing development of amorphous silicon photovoltaic cells by Energy Conversion Devices. **For an initial $3 million, Sohio gains a partnership with the Troy, Mich., firm to manufacture and sell ECD's devices developed by president and founder Stanford R. Ovshinsky.** An additional $12 million will be paid for further development. Atlantic Richfield Co. had previously signed a nonexclusive $25 million agreement with ECD in order to share in amorphous silicon developments.

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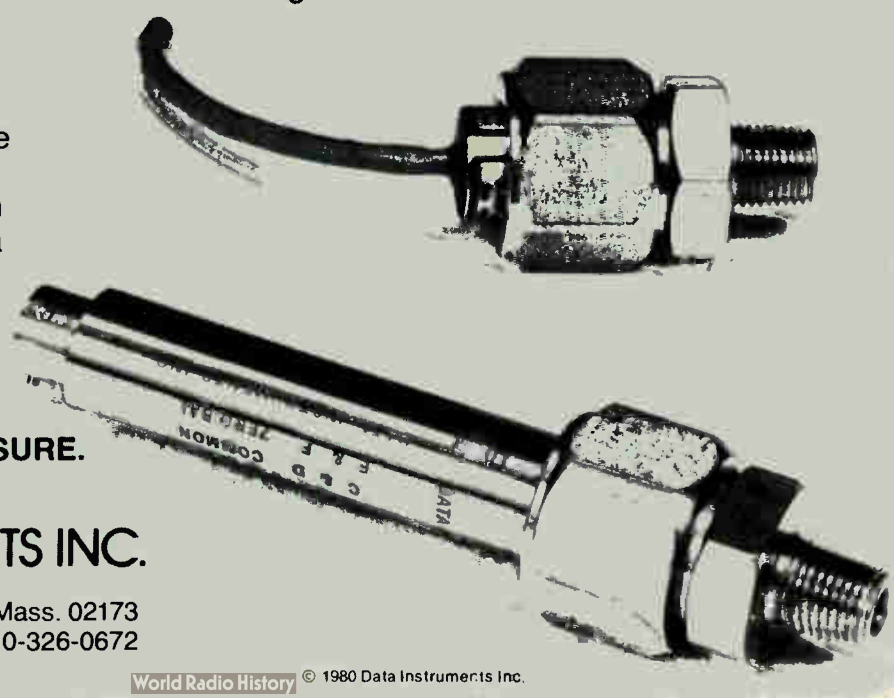

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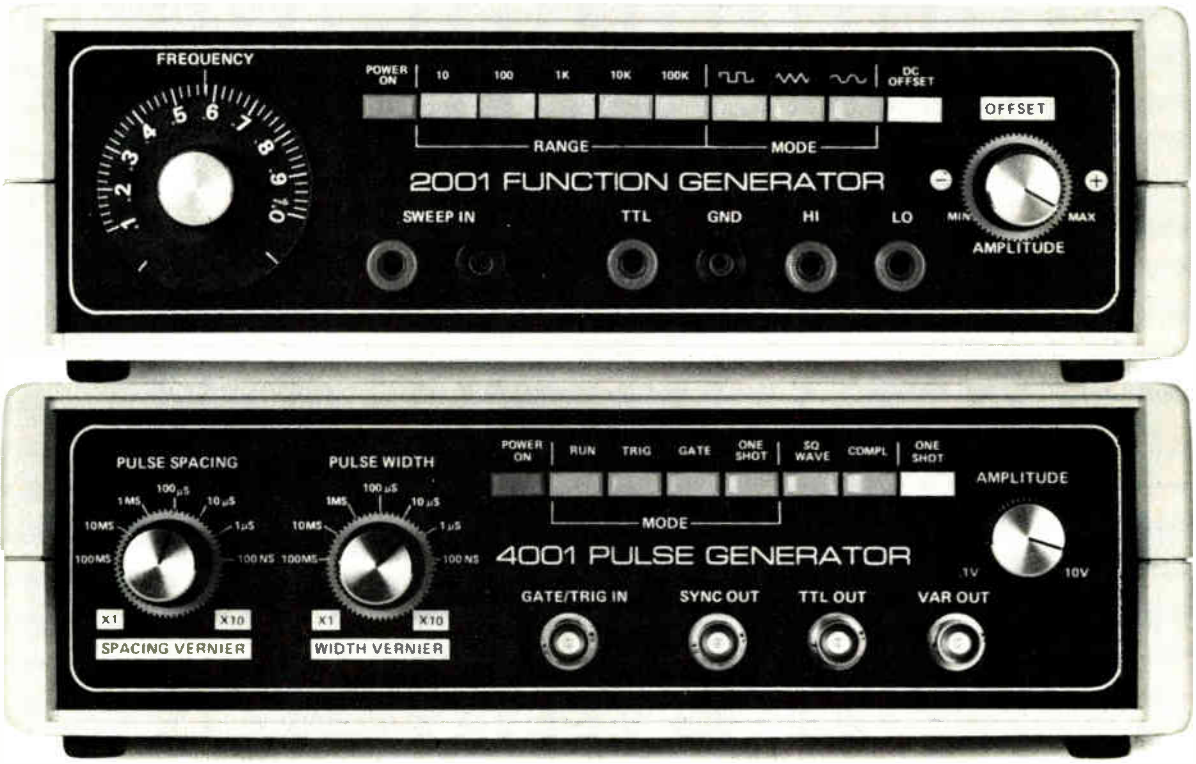

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16-bit n-MOS multiplier rivals bipolar devices with 100-ns speed

by Martin Marshall, San Francisco regional bureau

Small California company designs parallel processor that cuts power consumption without a sacrifice in speed

Multiplying 16 by 16 bits in 100 nanoseconds or less has been a purely bipolar domain. But that territory could soon be contested by low-power n-channel MOS chips if a new Silicon Valley outfit has its way.

Started in January by three chip designers from the advanced integrated-circuit laboratories of Hewlett-Packard Co., Weitek Corp. already has its first design, an n-MOS 16-by-16-bit parallel multiplier, ready to go out the door. But since the Santa Clara, Calif., firm markets very large-scale integration design services and does no fabrication, the WTL 1016 has become a chip in search of a manufacturer.

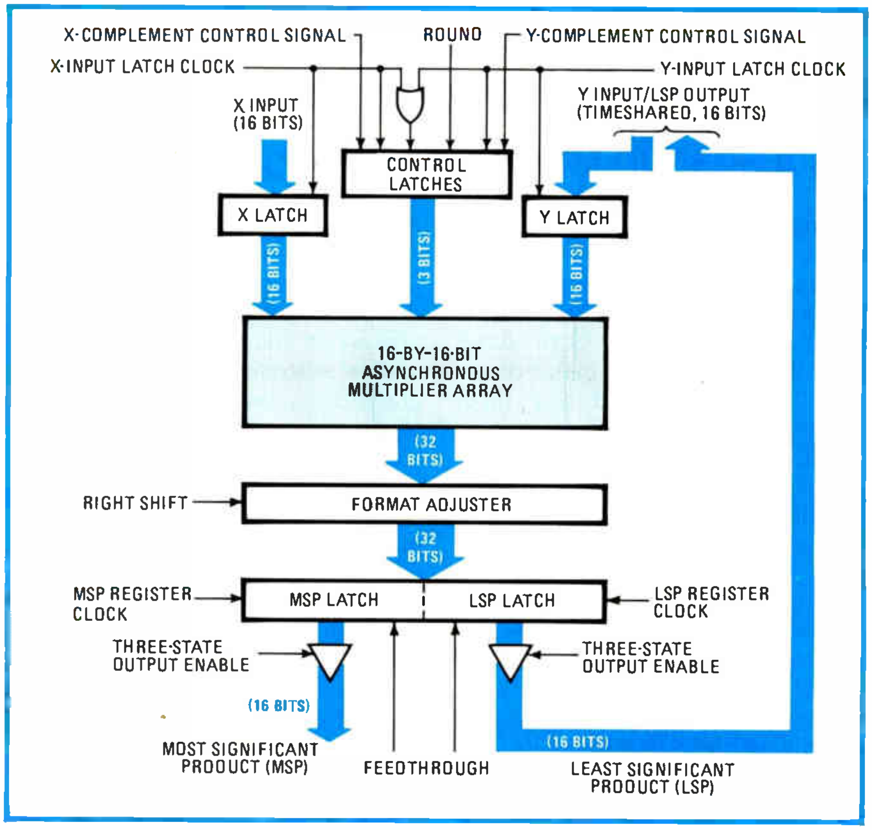
Advantageous. When the design does get into silicon, it will be strong competition for the MPY-16HJ bipolar multiplier of TRW LSI Products Inc., employed widely in digital processing systems like floating-point processors, video processors, speech synthesizers, and complex filters. Using n-MOS technology rather than TTL technology gives the Weitek multiplier some distinct advantages.

For one thing, its power consumption is typically 1 to 2 watts, compared to 3 to 4 W for the TRW part. For another, the gate delay for critical paths within the multiplier has been cut in half because n-MOS is so much denser than TTL.

What's more, the design rules can be less stringent for n-MOS. TRW needed to go to a state-of-the-art 2-micrometer process to make its chip possible; the Weitek design uses a 3-μm geometry. Even so, the bipolar chip is much larger, measuring 200 by 200 mils as against Weitek's 160 by 160 mils. The pinout, power supply, and input/output levels are identical for the two parts.

Weitek founders Chi-Shih Wang, Godfrey Fong, and Edmund Sun participated in the development of HP's advanced n-MOS processes, which resulted in the creation of a 32-bit chip set [*Electronics*, Feb. 10, p. 39], and brought that experience into play when they conceived their multiplier. Besides advanced processing, the Weitek design employs a more sophisticated multiplication algorithm than does the TRW part.

Up a tree. The WTL 1016 relies on a modified Booth's algorithm, whereas the MPY16HJ uses a Wallace tree, a parallel approach to multiplication that reduces the number of gates that partial sums must propagate through by using three input carry-save adders. Booth's algorithm, in contrast, employs a look-



Well-adjusted. Weitek Corp.'s chip design latches 16-bit inputs, which pass to a multiplier array. The right-shift signal selects 2's complement or unsigned magnitude formats.

ahead technique that recognizes strings of binary 1s in the multiplicand and replaces them with a simpler expression—a 1 followed by many 0s less 1—in order to speed up the calculation.

The two 16-bit numbers to be multiplied are fed in through separate data input lines and controlled by a signal that indicates whether the data is an unsigned magnitude or a 2's complement (see diagram). With this setup, the formats of the numbers being multiplied can be mixed. Both multiplier and multiplicand are latched so that they may be entered at different times.

The input numbers then pass through the multiplication array and emerge as a 32-bit product, which is fed into the format adjuster. With the right shift (RS) signal, it reorganizes the number into the desired format. When RS is high, the output is 2's complement, when low, it is an unsigned magnitude.

The 32-bit product passes from the format adjuster into two 16-bit latches. One latch handles the 16 most significant bits, while the other handles the 16 least significant bits. Each of these numbers is clocked out separately through a three-state buffer, under the control of individual output-enable lines. However, the most significant bits have dedicated output pins, whereas the least significant bits share pins with the Y-input bits. For applications where the designer does not wish to have the data latched at both the input and output, there is a feedthrough control that makes the output latching transparent to the data flow, so that once the input data is latched the output becomes automatic.

The n-MOS design will pare costs as well as improve performance, maintains Ed Barnett, Weitek's marketing manager. Although the WTL 1016 has not yet been fabricated, Barnett predicts that "because of the smaller die size, the end-user cost of the part should be 30% to 50% lower than the TRW part." It currently is priced at about $150.

Photovoltaics

Nine-sided tube pulled from silicon melt is cut apart to form solar-cell substrates

Pulling together has brought success in much human endeavor, and by pulling silicon ribbons together in a tube, researchers at Mobil-Tyco Solar Energy Corp. have done away with some of the major drawbacks involved in producing them separately.

With their new technique, Mobil-Tyco has formed large sheets at a rate of 146 square centimeters per minute from a single furnace, about one and a half times the production rate obtained by pulling separate 5-cm ribbons six at a time. Such ribbons have high promise as substrates for low-cost solar cells and they have fabricated with these substrates solar cells with respectable efficiencies of better than 13%.

For Mobil-Tyco, the new process is a natural extension of the edge-defined film-fed growth (EFG) technology it has used to produce silicon ribbons in volume for several years [*Electronics*, July 19, 1979, p. 110], says K. V. Ravi, general manager for production and development. In EFG, molten silicon in a crucible fills a graphite die, which defines the shape of the silicon. A starter seed of silicon is applied to the melt and when withdrawn pulls up with it a thin ribbon of single-crystal silicon that may be several inches wide and freezes when pulled from the melt.

Nonagon. But where the conventional EFG and other ribbon techniques draw up individual ribbons, the new approach uses a nine-sided die and a corresponding configuration of seed crystals to pull a thin-walled, nonagonal tube from the melt. The Mobil-Tyco laboratory system produces 6-foot-long silicon tubes that measure 48.8 cm around the periphery and have typical wall thicknesses of 0.25 millimeter. A laser cuts the tubes into flat rectangles that can then be made into solar cells.

"This is just another form of EFG, only instead of separate ribbons, we've pulled up nine linked together in a tube," says Ravi. The distinction makes for important advantages other than a higher production rate, he adds. Single-ribbon production requires accurate and precise temperature controls, since ribbons are prone to thermally induced discontinuities in width along their edges; the nine-faced tube, however, has no outer edges and thus displays far greater growth stability without having stringent temperature controls. Two other experimental techniques have been proposed to cope with the problem of edge stabilization in silicon ribbons [*Electronics*, Nov. 6, 1980, p. 40]. Both stick with the single-ribbon approach and so far neither has gained the corporate sponsor needed to develop it commercially.

Pulling tubes rather than ribbons also makes it possible to employ furnaces considerably more compact than those producing equivalent areas by drawing several, separate ribbons at the same time. Finally, the Mobil-Tyco team reports that the tubes show less silicon-carbide contamination from the die and pose almost none of the spatial guidance problems encountered in conventional EFG single-ribbon formation.

Stop and go. For all its pluses, however, the new process is not putting separate-ribbon production out of business just yet, Ravi cautions. Its track record so far is confined to the laboratory, he points out and adds, "The production floor has its own demands." Unlike current ribbon processes, the new technique is not yet able to operate continuously, and requires extensive laser cutting to separate the walls of the nonagonal tube into flat rectangles. But the Mobil-Tyco researchers already are considering a continuous tube-pulling and -cutting system. They also see a good chance for growing much larger polygonal tubes at faster pulling speeds.

While Mobil-Tyco remains committed to its present EFG production capability, the Waltham, Mass., firm is working on production of wider individual ribbons under funding from the Jet Propulsion Laboratory, Pasadena, Calif. Also, Mobil-Tyco will add to its production floor this year two new multiple-ribbon producing machines. -Linda Lowe

Computers

Network distributes command and control

Having entered an era where victory on land, on the sea, or in the air will depend on computers as much as on men, the brass of the U.S. armed forces is becoming more and more concerned about the survivability of its command and control systems.

So far, such C&C systems have largely been based on conventional host computers that control a small population of peripherals. A single hit, then, could knock out the host computer, rendering a ship or a field unit practically helpless.

A distributed C&C system, with computer intelligence spread throughout it, would be an obvious solution. Working against any rapid shift to distributed processing, though, is the enormous investment the armed forces have in conventional C&C gear. In addition, military men feel much more comfortable with proven equipment, which, for them, distributed processing is not.

A way out, according to Litton Industries Inc., is to build a distributed processing system (DPS) that nests existing equipment within it. The company's Data Systems division, which specializes in military C&C gear, has done just that.

The Van Nuys, Calif. division of Litton has developed a DPS network made up of interconnected nodes, each with its own central processor and bus controller. The processors emulate standard military computers, so that current C&C equipment can be tied into the network with very little reworking of existing software. The bus controllers distribute supervision of the whole network out among the nodes. "If any node fails, the system will keep operating without missing a beat," says DPS program manager Ralph Hileman.

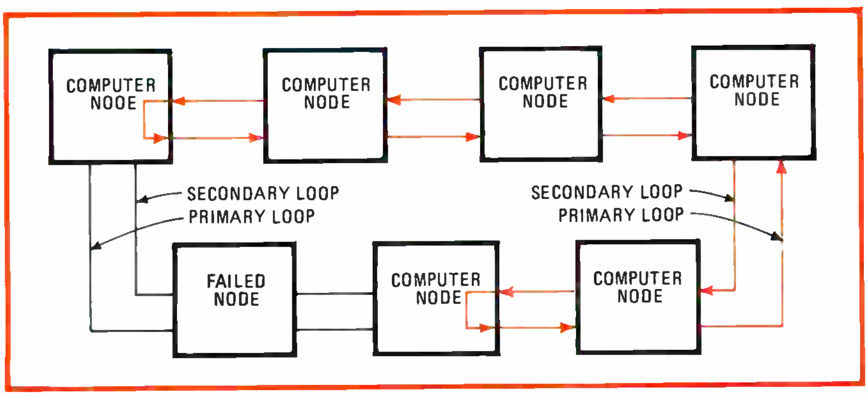
To achieve that performance, Litton's DPS has redundant dual communication loops. The bus controllers monitor the loops and, when a node fails, switch it out automatically (see figure) and reroute the loops accordingly. Data is transferred at 20 megabits per second.

All networking features derive from microprogrammability of the DPS emulators, Hileman points out. The emulation is done with bipolar emitter-coupled logic, "which essentially reproduces in bit-slices the architecture of the military computers," he says. Litton already has emulated such widely used military families as the AN/UYK-20 minicomputer made for the Navy by Sperry Univac and the AN/GYK-12 battlefield minicomputer built for the Army by Litton. An emulator for the Navy's AN/UYK-7 mainframe computer is in the offing.

In test. Litton already has installed a seven-node DPS network on a U.S. Navy Kidd-class (DDG-993) destroyer, where it is used to train crew members to operate weapon fire-control computers. "In general, crew reception has been good," says an official at the Navy's DDG-993 destroyer project office in Washington, D.C. Because this first system was done on a hurried-up schedule, it was not in military-quality packages, so Litton is now proposing to the Navy a version that fully meets military specifications. The system would cost the Navy less than $100,000 per node.

Hileman says the best description of how the Litton DPS functionally relates to existing command and control gear is: "It surrounds it." To get even higher probability of equipment surviving in battle, Hileman contemplates an arrangement of interlocking networks. Upgrading poses no particular problem since the DPS can easily add speed and memory capacity to the nodes.

The 16-bit minicomputer nodes have their control processors on three circuit cards. The nodes themselves weigh about 60 pounds and measure 11 inches high by 12 in. wide by 16 in. deep. Working also in favor of DPS are the characteristics of the ADA high-level computer language the Defense Department plans to make standard for military computing. "It works best with distributed processing," points out Hileman -Larry Waller



New look. Litton's DPS scheme for military command and control systems surrounds existing computers to build a distributed network. There are dual loops for redundancy, monitored by bus controllers in each node. If a node fails, the system reroutes the flow automatically.

Microprocessors

TI takes trade-ins on all development gear

The hoofbeats of Texas Instruments Inc.'s development system center in Houston are ringing louder and louder in the marketplace these days. For example, to promote the sales of its microprocessors, TI this month became the first manufacturer to take trade-ins of other companies' development systems as well as its own. It will also support at least three industry-standard operating-systems, including Unix and CP/M.

"The trade-in credit is being offered to any customer with an old working floppy-based development system," says Thomas Miller, manager for microprocessor development systems. "The discount will be around a third of the original investment in the old system," he adds.

The motivation behind TI's moves is straightforward. The company sees this new development system effort as a way to win a stronger position in both the 8-bit and 16-bit microprocessor markets, especially now that it has a comprehensive line of 8-bit units [*Electronics*, Jan. 27, p. 107]. Microprocessors, in turn, are considered by TI to be crucial to maintaining its market strength in advanced technologies. "The better we penetrate the development-system markets, the better our technologies will be accepted as they come into the market," says Miller.

TI's current flurry caps three months of intense activity in the area. In April, it introduced its Multiple-user Advanced Microprocessor Prototyping Lab (Multi-AMPL). [*Electronics*, April 7, p. 191]. Then just last month, the Dallas firm followed up with a low-end addition to

Exports carry Japanese growth

Though most people in the industry suspected it, now it is official: thanks to a solid gain in exports, the Japanese electronics industry chalked up a production increase of nearly 23% last year, according to figures just released by the Electronic Industries Association of Japan. Total production for 1980 was pegged at $38.4 billion, of which $18.2 billion —nearly one half—went into overseas trade as exports grew some 35%.

In the export sector, to the surprise of no one, there was no semblance of serious two-way trade: imports of electronics amounted to about one seventh that of total exports—$2.7 billion. Industrial equipment accounted for most of the imports, EIA-J notes.

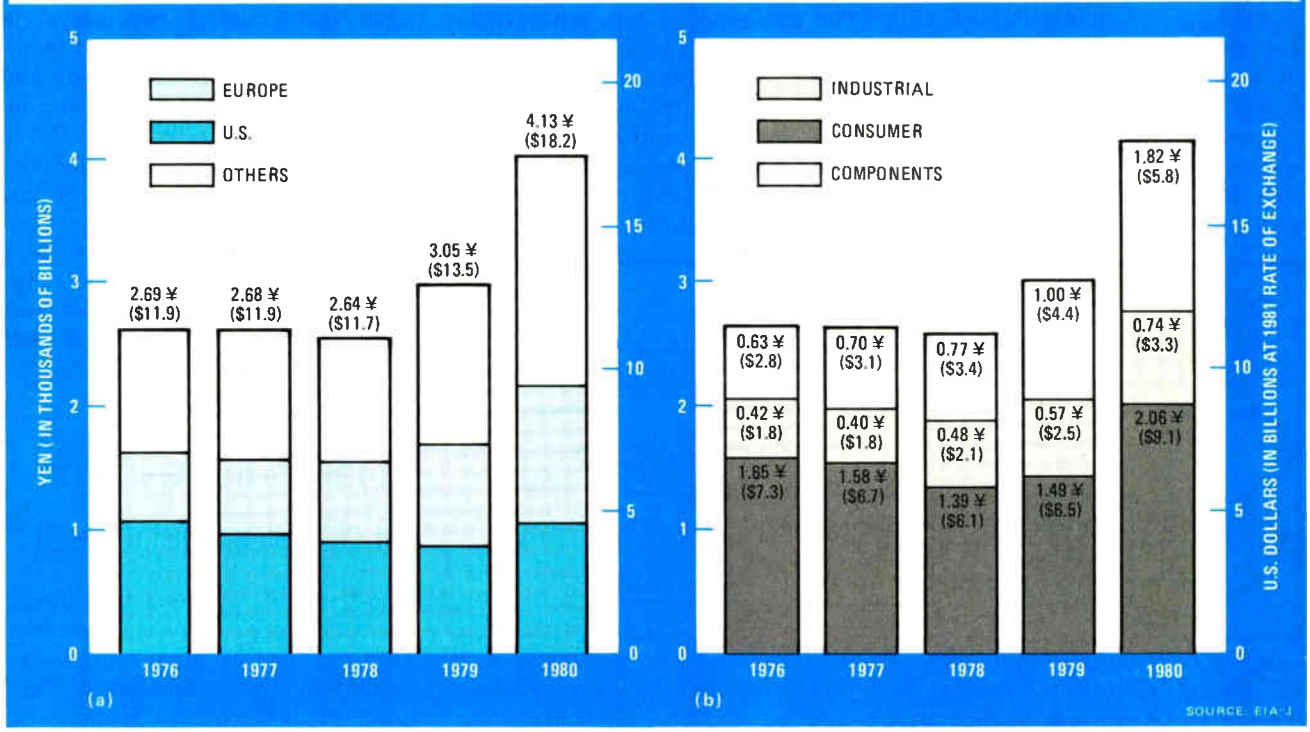
Much of the growth in exports came from sales to countries outside the United States and Europe, which now represent a little over 45% of Japan's export markets. By product type, the consumer segment is by far the leader, representing half of the $18.2 billion total.

Consumer-electronics imports, on the other hand, were a mere $169 million.

Total consumer equipment production in Japan was up over 28% in 1980, with the sharpest gains coming in video-cassette recorders. Some 4.44 million VCRs were manufactured, the EIA-J reports. Of this total, Japanese manufacturers exported 3.44 million units.

Industrial electronic equipment, which includes communications gear and computers, increased to $13.6 billion, with about $3.3 billion in exports. Here the import figures are in better balance than in the consumer sector, but still far from equality: EIA-J figures that Japan took in $1.28 billion in industrial equipment led by computers at $734 million. (For a related story, see p. 101.)

Production of electronic components in 1980 amounted to $11.7 billion with exports accounting for $5.8 billion of the total. All dollar figures were computed at an exchange rate of 226 yen per U. S. dollar **-Gerald M. Walker**



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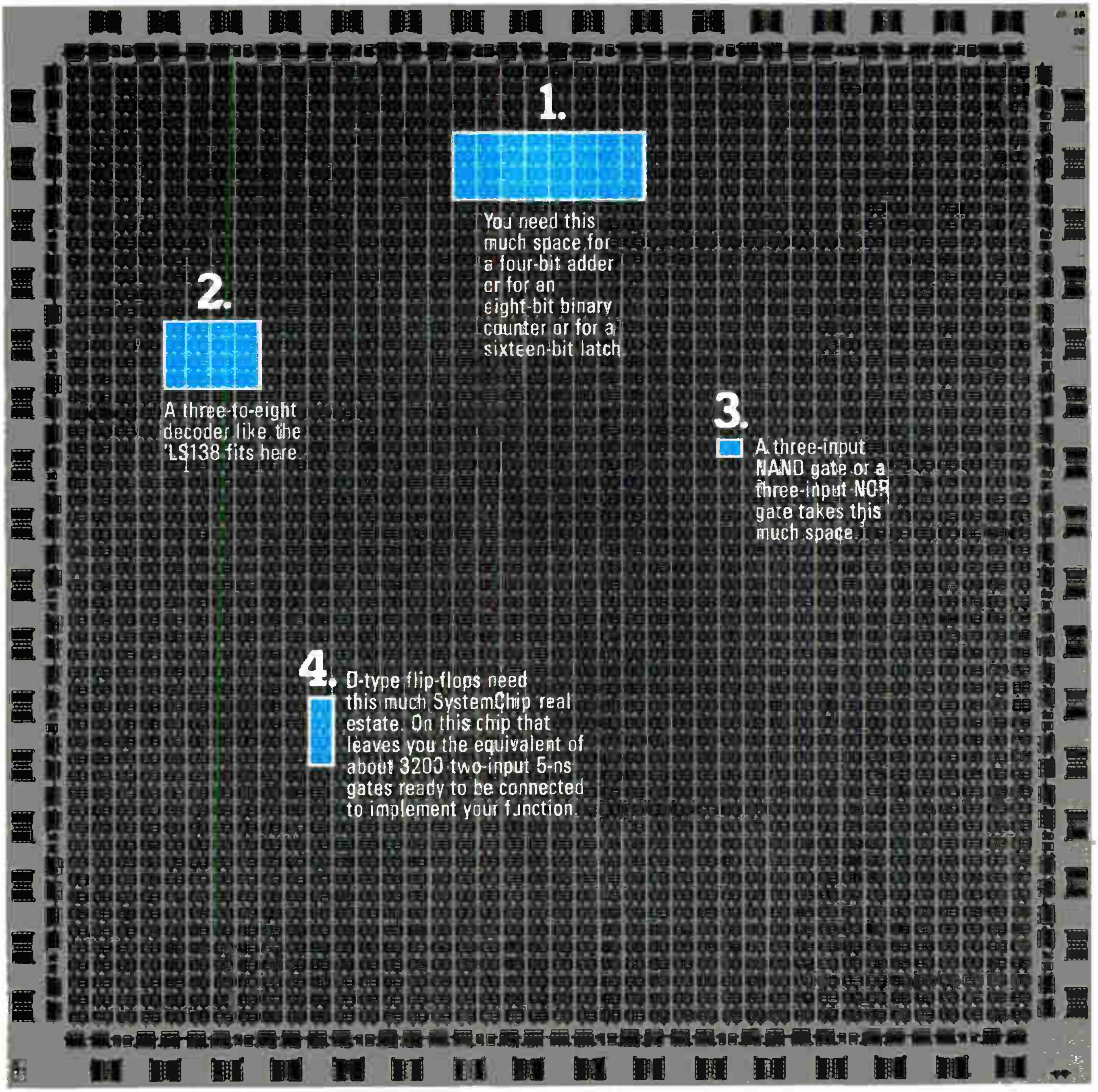

Unretouched photo of the new C82240 gate array before metalization.

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the Multi-AMPL line, the TMAM 9000 single-user, floppy-disk–based system, ticketed at $13,350.

Then this month it will begin supporting the UCSD P-system software for its 16-bit TMS9900 family of microprocessors with a board-level kit. The TM990/601 has three standard TI 990 microcomputer boards—a central processing unit, a 64-K dynamic random-access-memory board, and a floppy-disk controller. With a power supply and card cage, the kit sells for $3,800. A boxed version will go for $4,990.

Software. P-system software is priced at $600 for the first copy and $150 for additional ones. Having previously been adapted for TI's home computer, the P-system brings both Pascal and Fortran plus an operating system to the 9900.

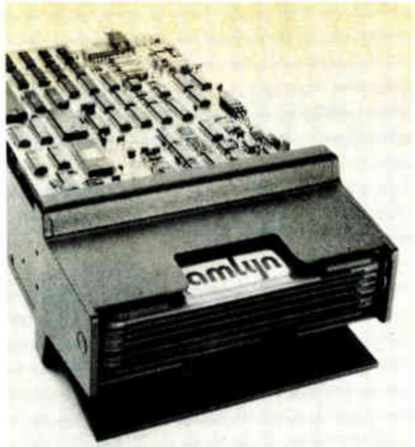
More software is coming. For example, TI will enhance the 990/601 to cover its 16-bit TMS99000 and its 8-bit TMS7000 chips as well as the TMS9900. And within six to nine months, it "intends to expand support for industry-standard operating systems like Unix and CP/M," Miller says. Unix is being adapted to an ever-increasing number of microcomputer systems [*Electronics*, April 7, p. 108]. TI will rework CP/M, originally written by Digital Research Inc. for the Intel 8080, to use the 9900's instruction set. **-J. Robert Lineback**

Peripherals

Floppy-disk drive handles 5 diskettes

For small computer systems, the trend is toward denser storage that can be removed and replaced. Consequently, a newly developed drive from Amlyn Corp., a recently formed maker of floppy-disk drives in San Jose, Calif., is noteworthy. The unit handles five disks simultaneously and can thus replace the pair of separate floppy-disk drives that are often supplied with small computer systems.

Moreover, the memory capacity of



Five-pack design. Inch-high floppy disk cartridge slips into front of drive. Memory of up to 8 megabytes occupies the same space as standard 5.25-in. drive.

one side of each 5.25-inch diskette—only one side is used—is the same as both sides of a double-density 8-in. floppy disk and 60% more than the double-sided, double-density 5.25-in. drives. Therefore the total cartridge capacity is 8 megabytes—much greater than the 2 or 4 megabytes of storage possible with other large-capacity floppy-disk drives [*Electronics*, May 19, p. 106].

Popular models. Amlyn is taking off after some pretty popular hardware in the floppy-disk field. Its model 5850 is electrically compatible with Shugart Associates' SA850 8-in. drive. A firm price is not set yet but, according to Amlyn marketing vice president Jim Snow, it should be around $800 in 500-unit quantities. This should bring the cartridge drive well below the cost of an equivalent 8-in. floppy store, he points out. A second-source agreement with an established disk maker is also being negotiated.

As for the hard-disk market, Amlyn's A506 drive is compatible with the small 5.25-in. Winchester disk drives and is intended as a replacement for their magnetic-tape backups. The drive will be cheaper at $800 or so and be faster than most tape backup systems available today, Snow asserts. For instance, each Amlyn diskette has the same capacity as one surface of Seagate Technology's ST506 disk, Snow continues, and could be used in place of it should the drive go down.

The 5.25-by-5.5-by-1-in. cartridge, which slides easily into the drive, is designed so that either an entire cartridge or a single diskette can be changed at one time. The mechanism calls to mind a juke box. Driven by a stepper motor, a mechanical device positions the cartridge tray to the angle that makes it possible for a mechanical "picker" to remove a diskette and mount it, like a phonograph record, on the drive spindle.

All the A506's mechanical operations are controlled by an Intel 8051 microprocessor. The average time to select and mount a diskette is about 1.5 seconds.

Data is recorded on one side of each diskette at 9,500 bits/in. and a density of 170 tracks/in., which is much greater than the usual 48 or 96 tracks/in. of standard floppy-disk drives. The high track density is made possible by a very accurate read/write head positioner that combines a reference track on the disk and an optical-reticule track-reference scale on the drive itself. The reticule lines are spaced at 0.59-mil increments on Mylar, the same material the disks are made of. Thus the scale expands and contracts at the same rate as the disk.

Movements of the head assembly are made by microstepping the motor in increments of 59 microinches. That works out at one tenth of the spacing between reticle lines and one hundredth the spacing between tracks.

The reference track is written near the outer edge of the disk. To find the reference point on the reticule from which to start counting tracks, the head assembly is moved to the carriage home position outside the reference track. Then the assembly is microstepped until the reference track is detected, whereupon this position is then used by the microprocessor as the reference location for all data tracks. Disk eccentricities are accounted for by looking at the reference track at eight positions around the circumference and by microstepping the head in and out as the disk rotates.

The speed of the two-speed spindle drive is selected under microprocessor control. The normal operating rate is 360 revolutions per minute. The other speed of 600 rpm reads from standard 5.25-in. diskettes re-

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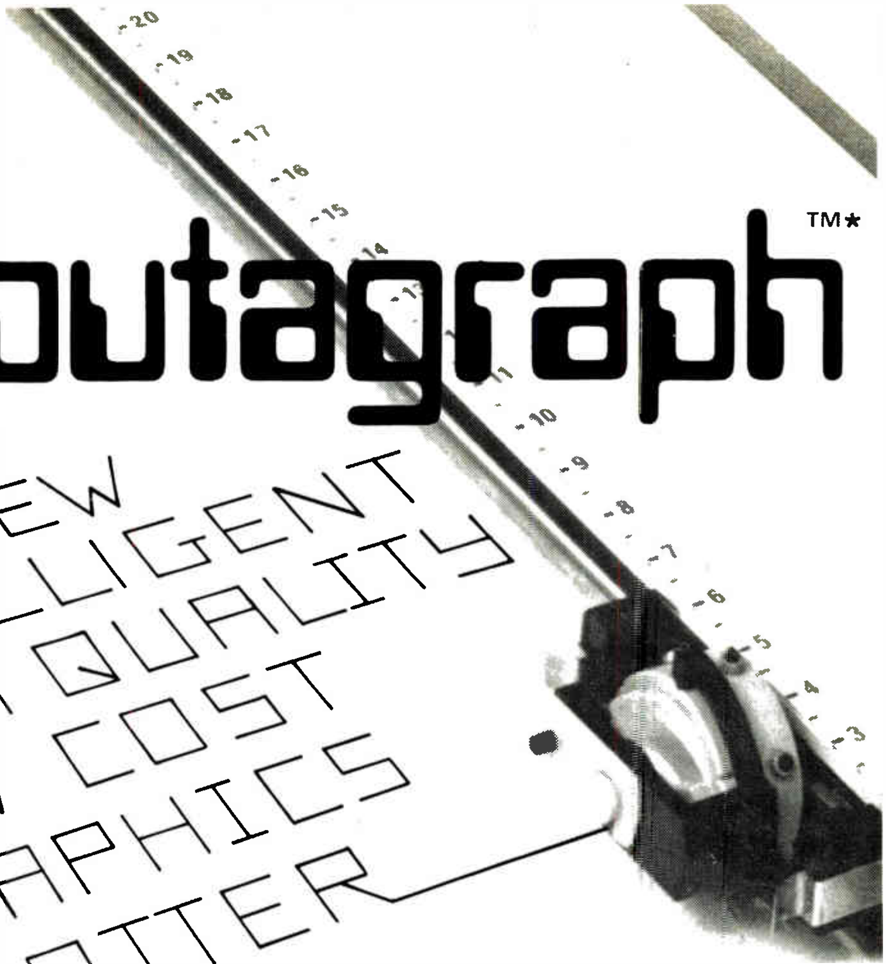

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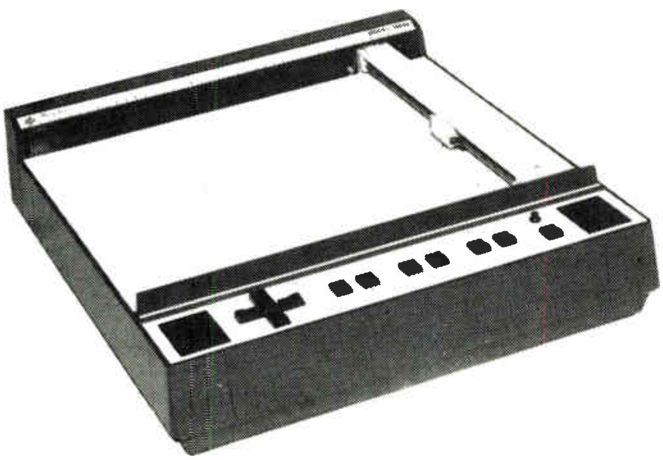

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Circle 221 on reader service card

corded at either 48 or 96 tracks/in. Thus, the new unit will read disks already on the market. A cartridge and five diskettes is expected to sell for about $35. -Tom Manuel

Solid state

Motorola, National to make fast C-MOS

Yet again a MOS technology is meeting bipolar speed. In a challenge to the recent overwhelming popularity of low-power Schottky TTL, Motorola Inc. and National Semiconductor Corp. are joining forces to make samples available this fall of a high-speed complementary-MOS logic family.

The 74HCXX family, the subject of a recently announced second-source agreement between the two firms, will be 20 times faster than conventional C-MOS metal-gate devices at 5 volts. It will also have the speeds and pin-outs of low-power Schottky TTL. Moreover, the new line will offer designers the low-power advantages of C-MOS and improved noise immunity over low-power Schottky TTL.

Because of these benefits, officials at both companies anticipate a strong showing against TTL devices—especially in new designs using C-MOS memories and microprocessors. Motorola estimates the total available market for high-speed C-MOS logic will be over $150 million in two years. However, National places the market in excess of only $100 million by the middle of the decade. Both agree that their estimates are extremely conservative.

"The market could be underestimated by as much as 50%," notes Rick Younts, semiconductor group vice president and operations manager for logic and special functions for Motorola in Austin, Texas.

Under the pact, Motorola and National have agreed to second-source each other on the family's first 25 devices. The 74HCXX line will be made in a C-MOS silicon-gate 3.5-micrometer self-aligning gate process. The devices will be rated at 30 megahertz with a full 4-milliampere low-power Schottky TTL capability. Each has independently developed its own family and C-MOS silicon-gate process and the agreement calls for an exchange of photomasks. The contract also allows the two manufacturers to swap masks on devices beyond the initial 25.

Home-grown process. Motorola's gate process derives from the technology used to make the MC146805E2 8-bit microprocessor [*Electronics*, Sept. 25, 1980, p. 123]. The new process is similar to the one that combines C-MOS and n-MOS on a single chip. However, the new process only uses C-MOS.

National uses a single polysilicon-gate version of its double-level polysilicon P^2 C-MOS process—developed for the NSC 800 microprocessor—to make its version of the 74HCXX family. Both new processes are similar so that only minor alterations are needed before the two can exchange photomasks.

Each firm plans to market at least 100 different devices and two sets of parts with different temperature ranges will be produced. The 74HCXX series will operate between −40°C and +85°C; the 54HCXX series will operate to +125°C. "We expect the family to grow with the advent of additional C-MOS memories and microproces-

News briefs

Former Hughes Aircraft employee faces espionage charges

A former Hughes Aircraft Co. engineer faces espionage charges later this month after admitting he sold photographs of secret radar documents to Polish agents. William H. Bell, 61, was arrested along with Polish businessman Marian W. Zacharski by Federal Bureau of Investigation agents on June 28. Based in Los Angeles, Zacharski is suspected of being a Polish intelligence officer and of passing the data along to the USSR.

FBI agents say Bell has been paid more than $110,000 since late 1979 but cooperated in getting evidence against Zacharski during the week prior to the arrests. The documents cited by the FBI cover a number of programs to which Bell as a radar manager had access. He was fired by Hughes in June.

IEEE gathers facts on low-paid alien engineers

Although no formal action has been taken by the Institute of Electrical and Electronics Engineers on the prickly topic of the alleged hiring by U. S. firms of alien engineers at cut-rate salaries, proponents of curbing the practice feel they are making some headway. At its June meeting, IEEE's U. S. Activities Board considered two resolutions proposed by the Los Angeles Council's Professional Activities Committee (LAC/PAC) and could take up the matter again, possibly as soon as next month's meeting. The resolutions called for advertisements from companies that undercut acceptable salaries to be barred from IEEE publications and for the institute to work closely with the Department of Labor, which certifies alien hiring [*Electronics*, April 21, p. 42]. George A. Morris Jr., LAC/PAC chairman, suggests information about low-paid alien engineers be sent to him or to IEEE's Washington office, which is compiling data for further evaluation.

Westinghouse seeks ties with Mitsubishi

In an effort to increase its semiconductor prowess, Westinghouse Electric Corp. is negotiating with Japan's Mitsubishi Electric Corp. to create a joint U. S.-based venture to manufacture integrated circuits. Westinghouse has also doubled its holdings in Siliconix, Inc., of Santa Clara, Calif., to 42.8%, pending approval by the Securities and Exchange Commission and Westinghouse stockholders.

An agreement between Westinghouse and Mitsubishi would plug Westinghouse into the Japanese company's recent thrust into very large-scale integrated circuits, such as 64-K random-access memories. In turn, Mitsubishi would get greater access to U. S. markets. With Siliconix, Westinghouse would have a source for data-processing and power devices.

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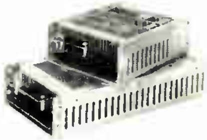

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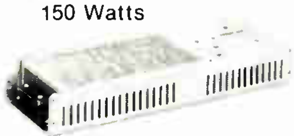

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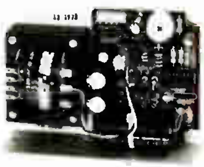

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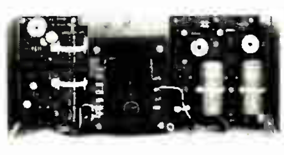
CP323, Up to 4 Drivers : $74.95

8.0" FLOPPY SUPPLIES



CP205, 1 Drive : $69.95
CP206, 2 Drives : $91.95
CP162, Up to 4 Drives : $120.00

WINCHESTER SUPPLIES

2 Models to Power any Manufacturer's Drive

CP379, CP384 : $120.00

Open-Frame Linear

- Industry Standard Packages
- 115/230 VAC Input
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- UL & CSA Recognized
- Industry's Best Power/Cost Ratio

SINGLE OUTPUT

5V @ 3A
12V @ 1.7A
15V @ 1.5A
24V @ 1.2A
28V @ 1.0A
250V @ 0.1A

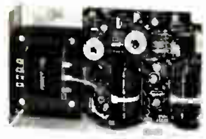
HB Series : $24.95

SINGLE OUTPUT

5V @ 6A
12V @ 3.4A
15V @ 3.0A
24V @ 2.4A
28V @ 2.0A
48V @ 1.0A

HC Series : $44.95 to $49.95

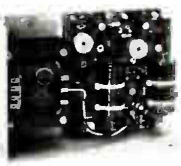
DUAL OUTPUT



± 12V @ 1.0A or
± 15V @ 0.8A

HAA15-0.8 : $39.95

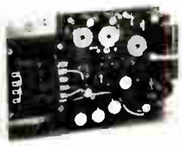
DUAL OUTPUT



± 12V @ 1.7A or
± 15V @ 1.5A

HBB15-1.5 : $49.95

TRIPLE OUTPUT



5V @ 2A
± 9V to ± 15V @ 0.4A

HTAA-16W : $49.95

TRIPLE OUTPUT

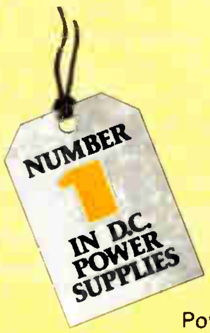
5V @ 3A
± 12V @ 1A or
± 15V @ 0.8A

HBAA-40W : $69.95

POWER FAIL MONITORS

- Indicates pending system power loss.
- Monitors AC line and DC outputs.
- Allows for orderly data-save procedures

PFM-1 : $24.95 PFM-2 : $39.95



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sors—it could be as large as 150 to 200 parts two or three years down the road," says Younts.

Sales will come primarily from new equipment designs, adds Keith Mueller, C-MOS product marketing manager for National in Santa Clara, Calif. "For the most part, it won't be retrofitted," he predicts. But for the new designs, it will definitely be a viable contender against low-power Schottky."

Glue parts. Younts maintains the new logic will make a strong showing as "glue parts" for linking C-MOS memories and microprocessors. However, penetration into the existing product lines that are loaded with bipolar parts will be minimal because the 74HCXX family will not be TTL-compatible.

"That is the main drawback to the family," Younts says. "We decided not to go with TTL-input compatibility because it would drastically take away from the noise immunity and speed, which the market says it needs." However, he points out that pull-up resistors would make the parts totally compatible with TTL. Motorola is already considering an extension to its 74HCXX line that would include TTL compatibility. "We would not duplicate the entire family," he says.

At present, Motorola is developing 46 members of the 74HCXX family: 5 decoders, 4 registers, 1 multivibrator, 1 comparator, 8 counters, 9 gates/buffers, 8 flip-flop/latches, 9 transceivers/receivers/line drivers, and 1 part classified as miscellaneous. National is making some 50 different circuits: 8 gates, 4 counters, 4 flip-flops, 1 multivibrator, 1 comparator, 1 hex-Schmitt trigger, several TTL-to-C-MOS translators, 2 shift registors, 6 multiplexers, 3 area decoders, 7 latches, and 8 drivers. The firm plans to begin mass production of the initial parts in the first quarter of 1982. **-J. Robert Lineback**

NCR serious about merchant market for semicustom logic, nonvolatile memory

NCR Corp.'s plan to begin selling semiconductor devices on the open market has met with some surprise and skepticism. "My jaw is on the floor. I would have assumed that a leopard couldn't change its spots," says one industry official.

"Historically, systems manufacturers have not been able to make the transition into the high-technology components business," adds Larry Jordan, a former marketing manager with the Intel Corp. group responsible for nonvolatile memories. He is now marketing manager for Seeq Technology Inc., San Jose, Calif.

But NCR officials profess a determination to prove the skeptics wrong. "We have to position ourselves so people realize this a major, permanent effort and not just something we're going to dabble in," says James H. Van Tassel, vice president of the Dayton, Ohio, company's Microelectronics division (see p. 14). With seven wafer fabrication lines currently in operation, NCR is spending $155 million on additional component capacity over a four-year period, he notes. Commitments to outside customers will be met, even in times of tight supply when NCR's own component needs are high, Van Tassel adds.

Big payoff looming. In choosing to sell electrically erasable programmable read-only memories and semicustom logic devices, NCR is entering market areas that are expected to grow handsomely. According to projections by Dataquest Inc., a Cupertino, Calif., market research firm, these segments are expected to increase from about $100 million each this year to about $550 million and $600 million, respectively, by 1985. With such growth, even some detractors concede there should be room for NCR to succeed, provided it has a firm commitment to the merchant approach and a sound sales plan. Van Tassel agrees. "We're entering this business to increase revenues and to make money," he declares.

The NCR plan calls for initial sales of semicustom logic devices and nonvolatile memories that are less than state-of-the-art. Higher technology products will come later. NCR's newly announced line of EE-PROMs and nonvolatile RAMs, for instance, is based on the company's 10-year-old p-channel metal-nitride-oxide-semiconductor technology. It is significantly slower than the n-channel MNOS and competing MOS floating-gate tunnel-oxide technologies backed by Hitachi Ltd. and Intel Corp., respectively, as well as others.

The company is supplying samples of seven EE-PROM devices, including two 512-bit parts at the low end, the 2K-by-4-bit NCR2811 and two 2-K-by-8-bit devices—the byte-erasable NCR2161 and the block-erasable NCR2168. Also available is the 256-by-8-bit NCR1734, a nonvolatile static RAM. Access times on these devices are typically between 850 nanoseconds and 1 microsecond, says Dave Major, marketing manager for the line.

Company officials say that faster, n-channel devices will be introduced during the fourth quarter this year. The initial p-channel devices will be fast enough for applications such as data terminals and avionics, Major says. They will compete in such marketing niches primarily against similar parts built by General Instrument Corp. under license, he observes. Pricing on the memory chips will be negotiable, with the 16-K EE-PROM devices expected to be in the $10-to-$20 range, says Andrew F. McKelvey, general manager at NCR's Miamisburg, Ohio, microelectronics plant.

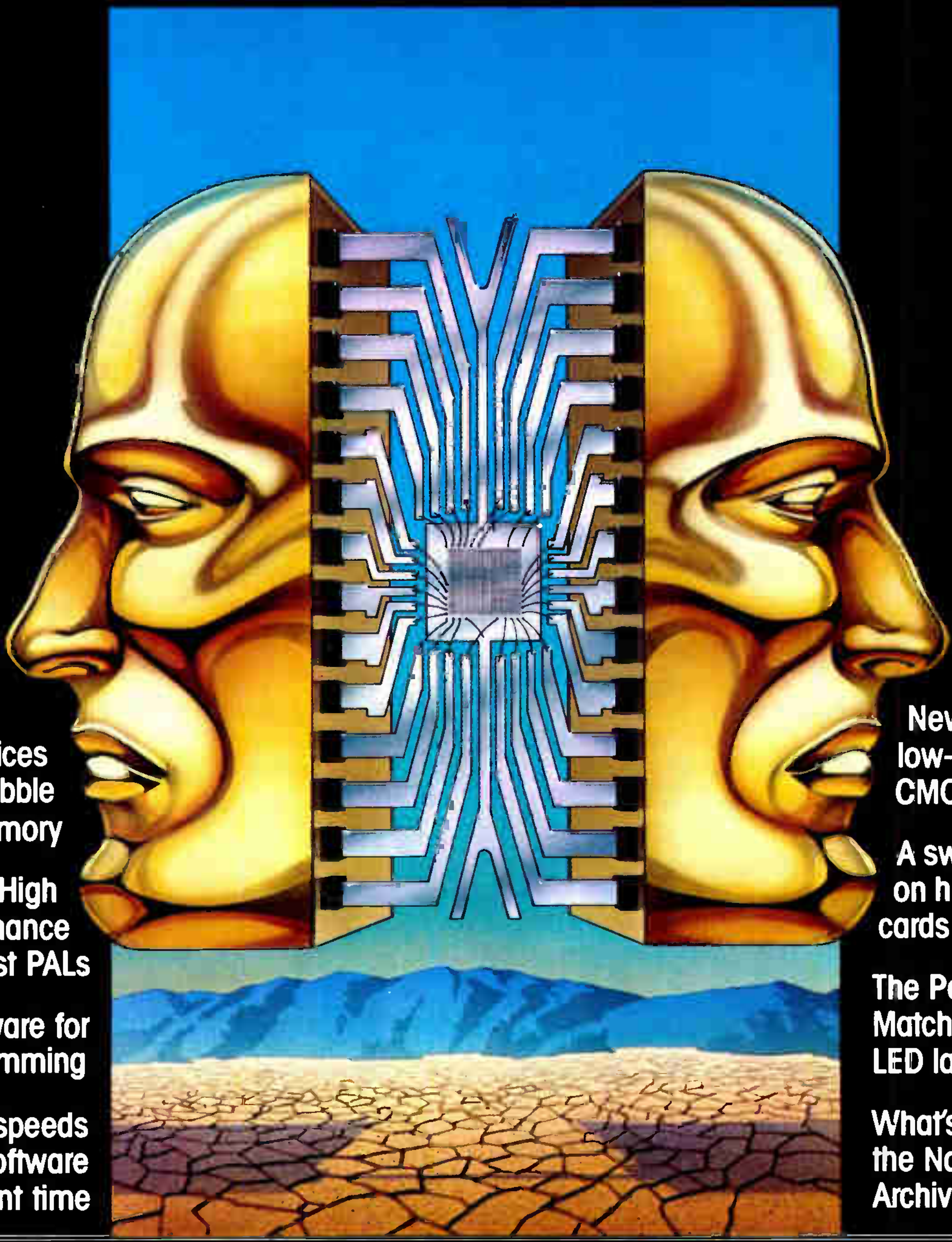
In-house library. The semicustom logic line makes use of an internal library of some 32 standard cell types that began being developed in house late in 1979. NCR will offer two standard die sizes—150 by 170 mils with 28 input/output pads and 225 by 225 mils with 40 I/O pads. By using 5- to 6-micrometer minimum geometries, devices with densities ranging from 200 to 1,000 gates will be possible. **-Wesley R. Iversen**

NATIONAL ANTHEM®

SEMICONDUCTOR NEWS FROM THE PRACTICAL WIZARDS OF SILICON VALLEY.

The first dual CPU microcontroller.

THE COP2440 MAKES DUAL PROCESSING ECONOMICAL.



New choices in bubble memory

High performance Fast PALs

Software for PAL programming

BLMX-80 speeds software development time

New ideas for low-cost CMOS DACs

A sweet deal on high rel cards

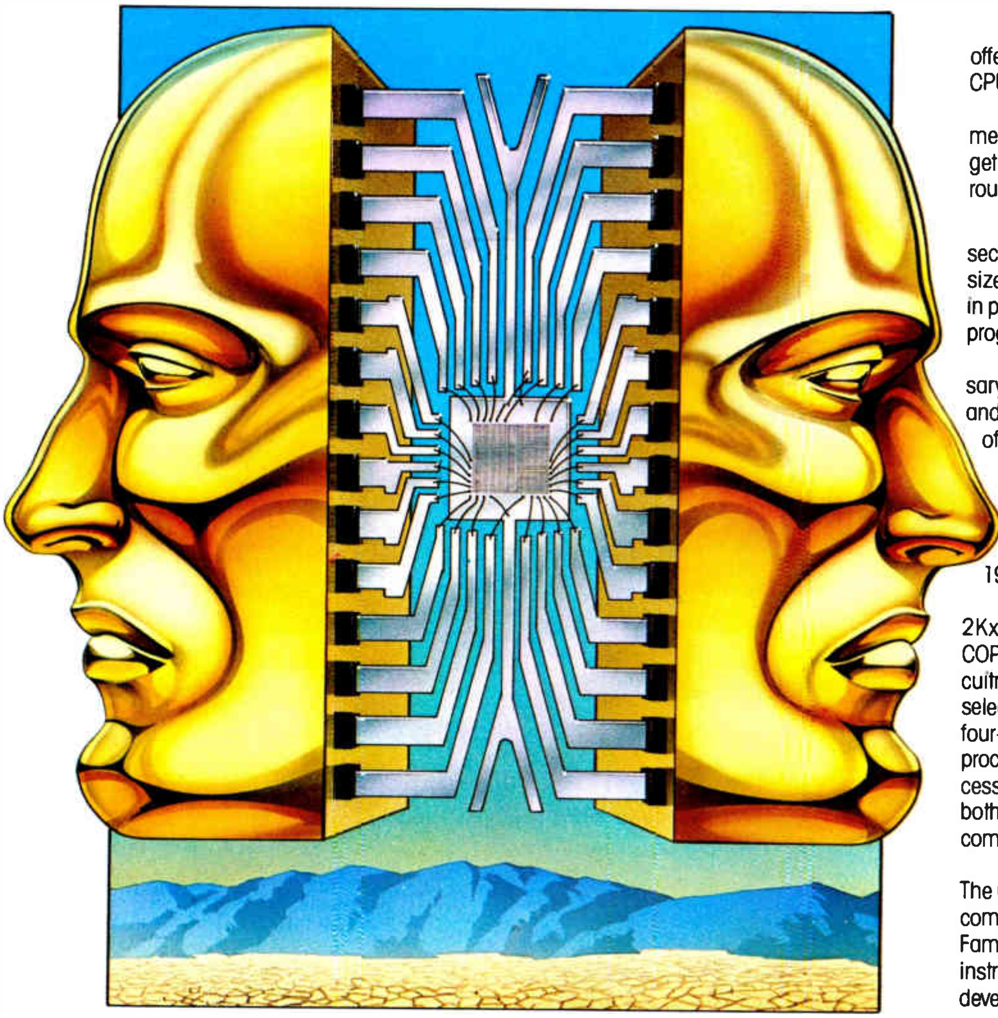
The Perfect Match in LED lamps

What's new from the National Archives?

Digitalker COPS Data Acquisition Logic Transistors Hybrids Linear Interface Bubble Memory RAMS/ROMS/PROMs Transducer Displays Custom Circuits Optoelectronics Memory Boards Microprocessors Development Systems Microcomputers Modules Mil/Aero

NATIONAL ANTHEM

The first single-chip dual CPU micro-controller simplifies programming.



The COP2440 makes dual CPU hardware and software implementation simple and economical.

National's new COP2440 represents the first progressive step away from the traditional "double the memory" approach to micro-controller development.

A new multiprocessor architecture* makes hardware implementation of a dual CPU microcontroller possible at low cost.

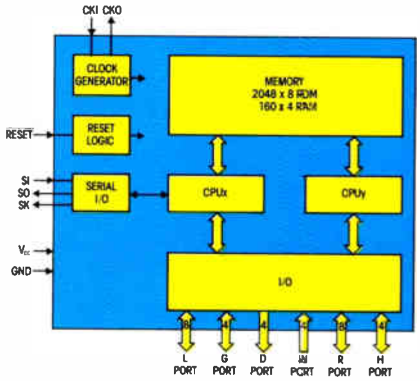
Two identical CPUs allow this latest addition to their COPS™ Family to process two simultaneous asynchronous time-critical events. The COP2440 can, for example, scan its input/output lines while processing data.

CPUs that work together. Dual on-chip CPUs simplify the programming process in several ways.

Now programs can be conveniently partitioned. Regular events can be processed in an orderly manner by one CPU leaving the second free to handle random tasks as they occur.

In time-critical applications, dual CPUs allow a single microcontroller to easily work on two jobs at once. The processor no longer needs to shuffle back and forth between diverse operations to make the results appear simultaneous.

COP2440 ARCHITECTURE



Very low hardware costs. The COP2440 offers significant hardware savings for dual CPU designs.

Since both processors access common memories, program ROM and data RAM, they get double use out of status flags, data, subroutines, and even the main program.

The Practical Wizards have added the second CPU with very little increase in die size. A small price to pay for significant gains in processing throughput, ROM efficiency, and programming ease.

The NMOS COP2440 contains all necessary system timing, internal logic, ROM, RAM, and I/O functions to implement a wide variety of dedicated control functions.

It is available in a 40-pin DIP with 35 I/O lines. Also available are a 28-pin version with 23 I/O lines, (the COP2441) and a 24-pin version with 19 I/O lines (the COP2442).

Additionally, the COP2440 features 2Kx8 ROM and 160x4 RAM, an enhanced COPS instruction set, zero-crossing detect circuitry, true multi-vectored interrupt from four selectable sources, on-chip timer/counter, a four-level subroutine stack (in RAM) for each processor, a 4ms execution time per processor, TTL/CMOS compatible I/O, and it's both MICROBUS™ and MICROWIRE™ compatible.

A multi-dimensional array of products. The COPS Family offers a truly broad range of compatible microcontrollers. Each COPS Family member shares a common set of instructions, MICROWIRE peripherals, and development tools.

So now the engineer can pick and choose from a wide variety of key specs: CPU size, fabrication technology (CMOS, low power NMOS, high speed NMOS), the temperature range, the voltage range, the speed, the I/O options and the package size and type.

Total COPS development support eases design and testing. The COP400-PDS is a low-cost concept-to-product tool designed to expedite every phase of COPS system design.

National's STARPLEX™ development system provides the same capability when equipped with the COPS ISE™.

The COPS QUIKLOOK™ tester is a simple and cost-effective way to perform incoming GO-NO GO inspection of COP Family devices on either the COP400-PDS or STARPLEX systems.

To get more information, check box 096 on this Anthem's coupon.

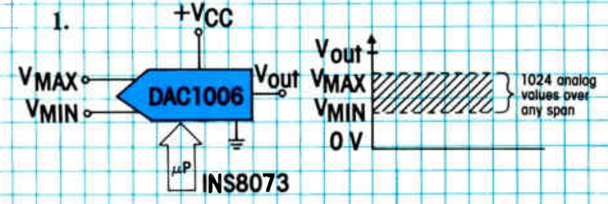
*Patent pending.

Innovative new designs for low cost CMOS DACs.

National's low cost, high performance 8-, 10-, and 12-bit CMOS D/A converters open up new doors to design simplicity. The Practical Wizards offer a complete line of DACs for either µP or non-µP based systems.

The microprocessor compatible MICRODACs™ feature up to 12-bit linearity, monotonicity, and differential non-linearity all guaranteed over temperature making them ideal for closed loop systems. Also, their four quadrant multiplying capability is a natural for digital-to-synchro converters.

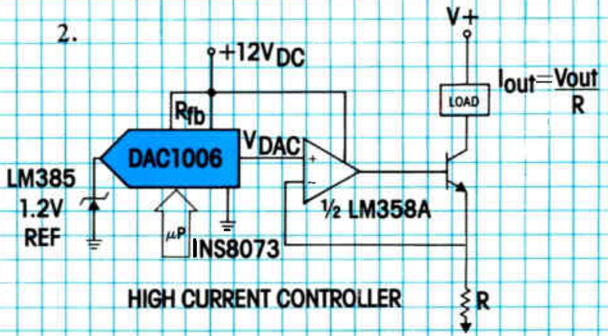
1.



Unique voltage-switching mode provides voltage output in single supply systems.

- 10-bit DACs can now provide high analog resolution over a reduced span.
- ΔV_{OUT} steps $= \frac{V_{MAX} - V_{MIN}}{2^{10}}$
- Non-interacting V_{MAX} and V_{MIN} adjustments.

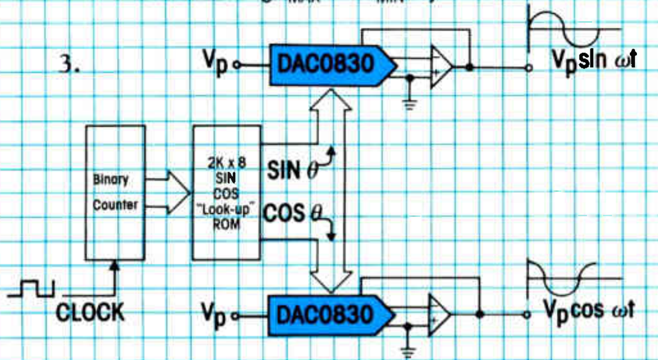
2.



Use µPs to control high power loads.

- Operates on a single supply.
- Operates with a low V_{REF} to increase output voltage compliance and reduce power dissipation in R.

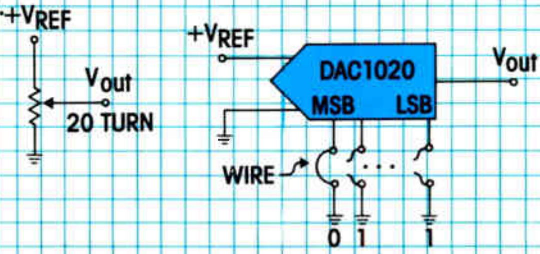
3.



One "look-up" ROM provides both sine and cosine outputs.

- Digital frequency control.
- Fast response to frequency changes.
- Operates down to very low frequencies.
- 90° phase shift between outputs at all frequencies.

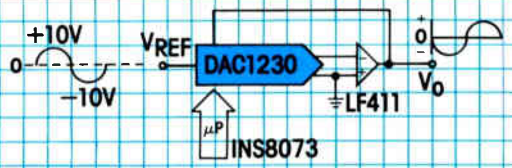
4.



A simple alternative to pots.

- Low cost.
- Vibration and "diddle" proof.
- Precise and stable output voltage.
- Can be automated.

5.



Let µPs control levels of AC signals.

- Accepts bipolar AC signals.
- High resolution—to 1 part in 4096.
- Reduces cost and saves board space.
- Does not distort the signal.

6.

More DAC design ideas.

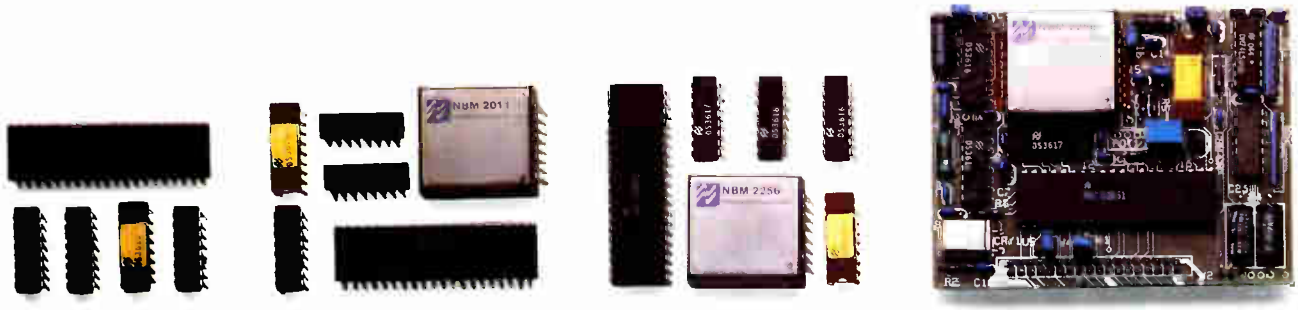
- µP-controlled function generator.
- Two terminal 4 to 20 mA current loop controller.
- Variable f_o, variable Q, constant BW bandpass filter.
- Capacitance multiplier.
- And many others.

For circuit schematics on these and other applications as well as the rest of the facts on National's broad line of easy-to-use DACs, check boxes 051 and 101 on this Anthem's coupon.

It took the Practical Wizards to bring reasonable prices to the best DACs in the industry.

NATIONAL ANTHEM

Freedom of design with the industry's broadest line of bubble memory products.



Only National offers everything for bubble memory applications. Even true second and third sourcing (by SAGEM and Motorola).

In keeping with National's commitment to service the entire bubble memory marketplace, the Practical Wizards are now offering the industry's broadest line of products.

In fact, they're already shipping everything from board level systems and subsystems to advanced bubble devices, controllers and support circuits.

Keeping pace with the design curve. Although the bubble memory concept has been around for a few years, the technology itself has only now been advanced to the point of offering a truly cost-effective alternative to floppy disk and other non-volatile storage media.

At this early stage of the game, incorporating bubble memory into new and existing designs requires that it be available in a wide variety of forms.

It is by no coincidence that National leads the industry in this area by providing the largest selection of sophisticated bubble memory products, including a complete ¼Mbit board level system and a 1Mbit expansion board, low cost ¼Mbit and 1Mbit Board Level Expansion (BLX) subsystems, ¼Mbit and 1Mbit kits, the industry's smallest and most dense bubble memory devices, plus controllers and support circuits. (See the listing at right for a brief description of each product.)

Only National offers such a high level of design flexibility and efficiency. As bubble memory designs move from board level system solutions to tailored configurations, National will be there with the right hardware at the right price.

Design with the highest bubble density available. The Practical Wizards' product line also includes some major technological advantages over the rest of the industry. So application designs can now be much more reliable and cost-effective than ever before.

To begin with, their 16-pin ¼Mbit and 1Mbit bubble memory devices (the NBM2256 and NBM2011, respectively) are the industry's smallest and most dense.

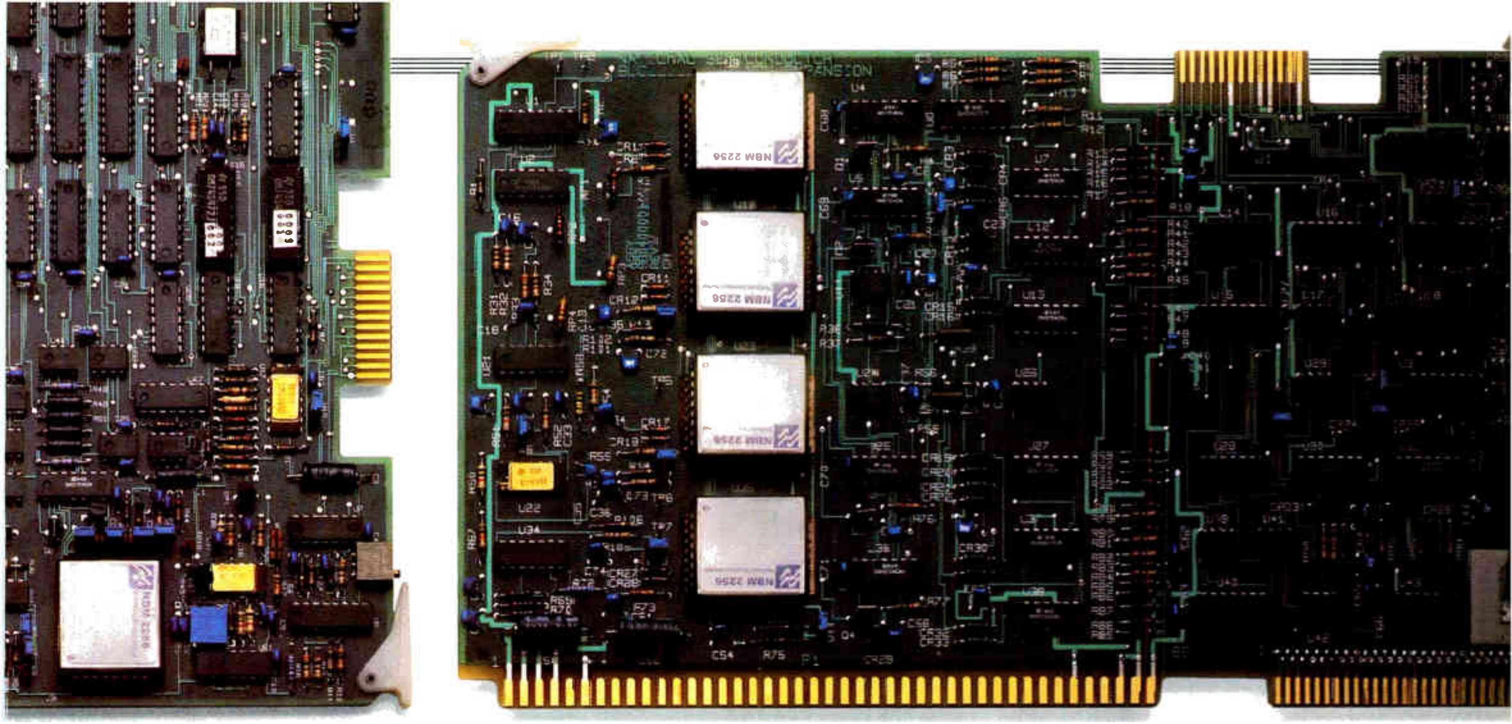
Plus, they've developed a more advanced support architecture that requires only four support circuits (plus controller) as opposed to the competition's five or seven.

By combining this device density with true system density, bubble memory designs will be smaller, simpler and more reliable than they have been before.

Optimize designs with ¼Mbit and 1Mbit functionally compatible kits. To go even further

BUBBLE MEMORY PRODUCT OVERVIEW

PART NUMBER	DESCRIPTION
SYSTEMS	
BLC-9250	Multibus™ and Series/80 compatible ¼Mbit bubble memory board.
BLC-9101	Multibus and Series/80 compatible 1Mbit bubble memory expansion board.
SUBSYSTEMS	
BLX-9252	¼Mbit bubble memory subsystem. This 11 square-inch module adds full bubble capability to National's SuperChip™ host CPU boards.
BLX-9012	1Mbit bubble memory subsystem, also used with National's SuperChip host CPU boards.
DEVICES	
NBM2256	¼Mbit 16-pin bubble memory device.
NBM2011	1Mbit 16-pin bubble memory device (pin-out compatible with the NBM2256.)
KITS	
NBK4251	Compact ¼Mbit bubble memory kit, including an NBM2256 bubble memory device, NBC82851 controller, DS3615 function driver, two DS3616 coil drivers, and a DS3617 sense amp. Expansion kits (minus the controller) are also available.
NBK4011	Compact 1Mbit bubble memory kit, including an NBM2011 bubble memory device, NBC82853 controller, DS3618 function driver, two DS3616 coil drivers and a DS3617 sense amp. Expansion kits are also available.
CONTROLLERS	
NBC82851	¼Mbit bubble memory controller.
NBC82853	1Mbit bubble memory controller (pin-out compatible with the NBC82851).
INTERFACE CIRCUITS	
DS3615	¼Mbit bubble memory function driver.
DS3618	1Mbit bubble memory function driver (pin-out compatible with the DS3615).
DS3616	Bubble memory coil driver.
DS3617	Bubble memory sense amp.



toward easing the design cycle, National also provides both their 256Kbit and 1Mbit minimum subsystems in convenient kit form.

The diagram below shows the ¼Mbit minimum configuration using the devices included with the NBK4251 kit. As the product table at left points out, the NBK4011 kit merely exchanges the 1Mbit versions of the bubble device itself, the controller, and the function driver for the ¼Mbit versions.

The host system's software is identical for both kits except for changing memory size constants.

Expansion kits are also available for applications that use a single controller for 2, 4 or 8 bubble devices.

The NBM2256 and NBM2011 bubble memory devices. The NBM2256 ¼Mbit and the NBM2011 1Mbit bubble devices are much more than just the smallest (16-pin) and most dense. They are also the most reliable, due in part to the use of Cr-Cu-Cr conductors.

They also feature:

- fast access time—typically 7ms (¼Mbit) and 11ms (1Mbit).
- low power dissipation—under 1W typical
- on-chip redundancy map.
- non-volatility.
- pin-compatibility for easy upgrading.

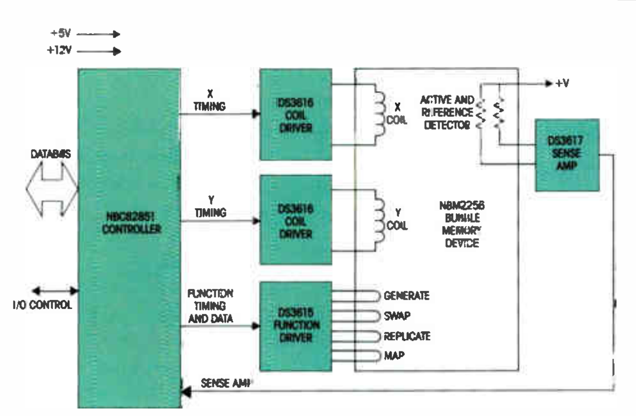
The NBC82851 and NBC82853 controllers. National's NBC82851 ¼Mbit and NBC82853 1Mbit bubble memory controllers are both 40-pin devices fabricated in the exclusive low power XMOS™ technology.

Each controller provides all signal timing necessary to drive 1, 2, 4 or 8 bubble memory devices in parallel. Yet both require fewer interface circuits (4) than any other controller available.

In addition, they feature:

- automatic start-up and power-down sequencing for the utmost in data integrity.
- Error Checking and Correction (ECC).
- they perform all data formatting, including redundant loop insertion and deletion and parallel-to-serial conversion.
- MICROBUS™ compatibility, so they can interface with a wide range of microprocessors.

The most versatile support circuits available. All of National's bubble support circuits were designed by a single design team using reliable bipolar technology. So they were integrated from the ground up to provide the lowest cost solution for complete bubble memory support.



MINIMUM BUBBLE MEMORY SUBSYSTEM (¼MBIT)

The versatility that results from this approach shows up in a number of ways. First, all of them can operate from two standard power supplies— +5V and +12V. Second, most of them could also support bubble memory devices other than the NBM2256 and NBM2011. And third, they all feature power fail protection circuitry for added reliability and simpler design.

The DS3615 and DS3618 function drivers. The DS3615 ¼Mbit and DS3618 1Mbit function drivers actually perform the physical manipulation of the bubbles. This includes bubble generation, replication, transfer and swap.

Both of these pin-compatible devices utilize multiple on-chip current sources to translate the controller's voltage mode commands to current mode events.

The DS3616 coil driver. Two DS3616 coil drivers are used to rotate the magnetic field, and hence the bubble, in each device.

These advanced components feature on-chip output coil clamp diodes and an optional internal voltage booster—both exclusive to National—as well as two high current push-pull outputs.

The DS3617 sense amp. The highly versatile DS3617 bubble memory sense amplifier is packed with features that the competition can't begin to match. For example:

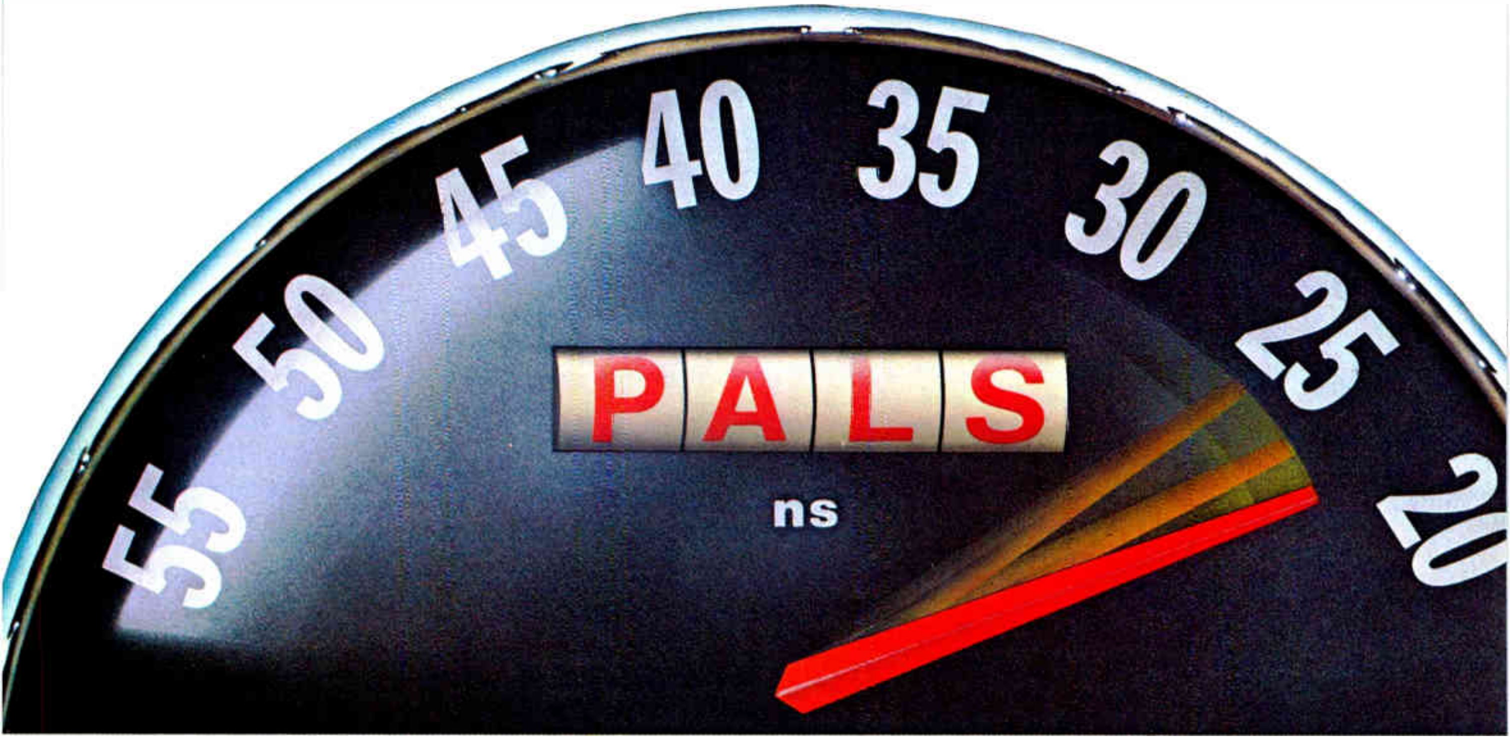
- guaranteed tight threshold limits over the specified temp and supply voltage range.
- the threshold is externally adjustable over the 0mV to 10mV range, so the DS3617 is compatible with a wide variety of bubble devices and non-bubble memory applications.

Rising to the top in bubble memory. It's easy to see that the Practical Wizards from National have answered the needs of the bubble memory market with the full range of high performance, low cost systems, subsystems, kits and components.

They're on a fast rise to the top of bubble memory technology.

For complete details on these advanced products, check box 099 on this Anthem's coupon.

SuperChip, XMOS, MICROBUS are trademarks of National Semiconductor Corporation. Multibus is a trademark of Intel Corporation.



Break the speed limit with 25ns PALs.™

New fast PALs are the quicker version of National's programmable array logic devices for low cost, space saving designs.

Earlier this year National announced that PALs were at the lowest cost ever and still continuing downward in price. Now they've strengthened their PAL line with the introduction of the fastest PALs yet.

These new fast versions are for applications requiring a throughput time of 25ns from input to output, rather than the regular version's 40ns. Other than the speed specs and price, both regular and fast PALs are identical.

PALs were designed to replace standard TTL logic. A single PAL can replace up to 12 SSI/MSI packages.

At easily achievable levels of package replacement, PALs, in volume, are now cost-competitive with the SSI/MSI parts they replace.

And PAL devices are fully field-programmable to provide the utmost in design flexibility and efficiency.

PAL's basic logic implementation is the familiar AND-OR array, where the AND array is programmable and the OR array is fixed. Additional functionality is provided in five of the PAL part types which contain registers.

PAL's standard logic and flexible I/O programming provide design and production efficiency unknown up to now. That's because logic modifications can be made more quickly and easily with PALs than with any other logic.

National is producing TTL-compatible PALs with the same time-tested technology used to manufacture PROMs. Their Titanium-Tungsten fuses have been proven reliable both through internal rel testing and three years of field use.

Program development and debugging of PALs is supported by National's STARPLEX™ development system.

And with 15 different PAL devices to choose from, logic design efficiency and reliability are truly maximized.

To optain a PAL brochure simply check box 025 on this Anthem's coupon.

National — the inexpensive souce for reliable PALs.

PAL is a trademark of and used under license with Monolithic Memories, Inc.
STARPLEX is a trademark of National Semiconductor Corporation.

PALSM. For those who don't have time to waste.

The easy-to-use PAL™ assembler makes PAL programming a snap.

The Practical Wizards have recently extended development support to cover their entire line of standard and Fast PAL (Programmable Array Logic) devices.

It's called PALASM™ — a new software module incorporated into the Universal PROM Programmer, an option of the versatile STARPLEX™ development system. PALASM serves as the software interface between the STARPLEX system and the PROM Programmer.

PALASM converts PAL logic (Boolean equations, etc.) into a form that the Universal PROM Programmer can readily understand and transfer to its associated PAL personality card. The logic is then burned into the PAL array.

Now, with the addition of PALASM, STARPLEX becomes an even more versatile development system.

Check box 085 on the coupon for additional information.

STARPLEX, is a trademark of National Semiconductor Corporation.
PALASM and PAL are trademarks of Monolithic Memories, Incorporated.

Cut real-time software development by up to 80%.

The new BLMX-80 real-time, multi-tasking operating system lets programmers concentrate on dedicated application software.

A software engineer charged with designing a real-time multi-tasking application system can easily spend most of his efforts writing system management functions. In many cases, up to 80% of his time may be spent on what amounts to only 20% of the total software for the system.

National Semiconductor has now turned this situation around with their new BLMX-80 (Board Level Multi-tasking eXecutive) operating system.

BLMX-80 is a sophisticated yet easy-to-use real-time, multi-tasking executive that operates on National's Series/80 Board Level Computer (BLC) products or other Multibus™ boards. It can currently be configured to run on systems built around the 8080, 8085, Z-80® and NSC800 microprocessors.

The easy way to system development. In addition to dramatically cutting software development and costs over the "do-it-yourself" approach, BLMX-80 provides highly structured modular application programming. This not only makes programs easier to test and debug, but also easily expandable and maintainable as well.

Partitioned programming. By starting the development cycle with a fully integrated and easy-to-use operating system already in place (rather than at "ground zero"), the project can be more easily managed. The Project Manager can assign program segments to different team members and be confident that the segments will interface smoothly.

Support software simplifies system configuration. BLMX-80 offers a variety of significant enhancements over competitive operating systems.

In terms of ease-of-use, BLMX-80 includes highly interactive menu-driven system configuration software. By using National's STARPLEX™ development system with ISE™ (In-System Emulation), the system can be generated or reconfigured in as little as 15 minutes. By contrast, other operating systems require the tedious process of setting up data structures manually.

Direct interrupt handling. With the BLMX-80 approach to direct interrupt handling (as opposed to task-based interrupts), response time is not degraded by operating system overhead. This is what real-time systems are all about.

BLMX-80 also provides a complete set of device drivers and interface modules. These include a terminal handler, a printer driver, analog I/O, disk file system, plus drivers for future BLC and BLX products.

For even greater design flexibility, BLMX-80 is fully hardware and location independent and supports a PL/M interface.

A liberal licensing agreement. No competitive operating system even comes close to matching all the capabilities of BLMX-80. But National didn't stop there.

To make their software portable in every sense of the word, they have provided a liberal licensing agreement that makes it much easier for the user to replicate the software with minimal restrictions.

Non-restrictive features of the software license include:

- unlimited copy privileges for the user's internal purposes.
- no serial number or system registration procedures.
- no sublicensing of BLMX-80-based software to customers of National's OEM customers.

BLMX-80 is not only a superior piece of software, it's also available without a lot of strings attached.

The architecture of BLMX-80. BLMX-80 provides a software foundation upon which the engineer can design a wide variety of applications.

The BLMX-80 operating system is based on a kernel concept, where the essential system functions (task scheduling, message control, interrupt channel management, etc.) are contained in the kernel. A variety of system modules may be selectively included to suit the requirements of the particular application.

This can be viewed as a "layered" or concentric software system. The kernel forms the heart or innermost layer, the various system modules which have been selected form the second layer, and the user-written tasks and device drivers (also included) form the outermost layer.

The kernel and selected system modules are designed to form a ROM-resident operating system which is linked as part of the final application program code.

The minimum BLMX-80 configuration would consist of only the kernel plus user tasks. In this configuration, the operating system would occupy only 2K bytes of ROM and require less than 1K bytes of RAM.

The best approach to software development. National's new BLMX-80 real-time, multi-tasking operating system is far and away the fastest and most cost-effective approach to software development and maintenance for real-time applications.

So rather than waste a lot of time and effort writing complex system software, call National. They've already written it.

For complete details on BLMX-80, check box 100 on this issue's National Archives coupon.

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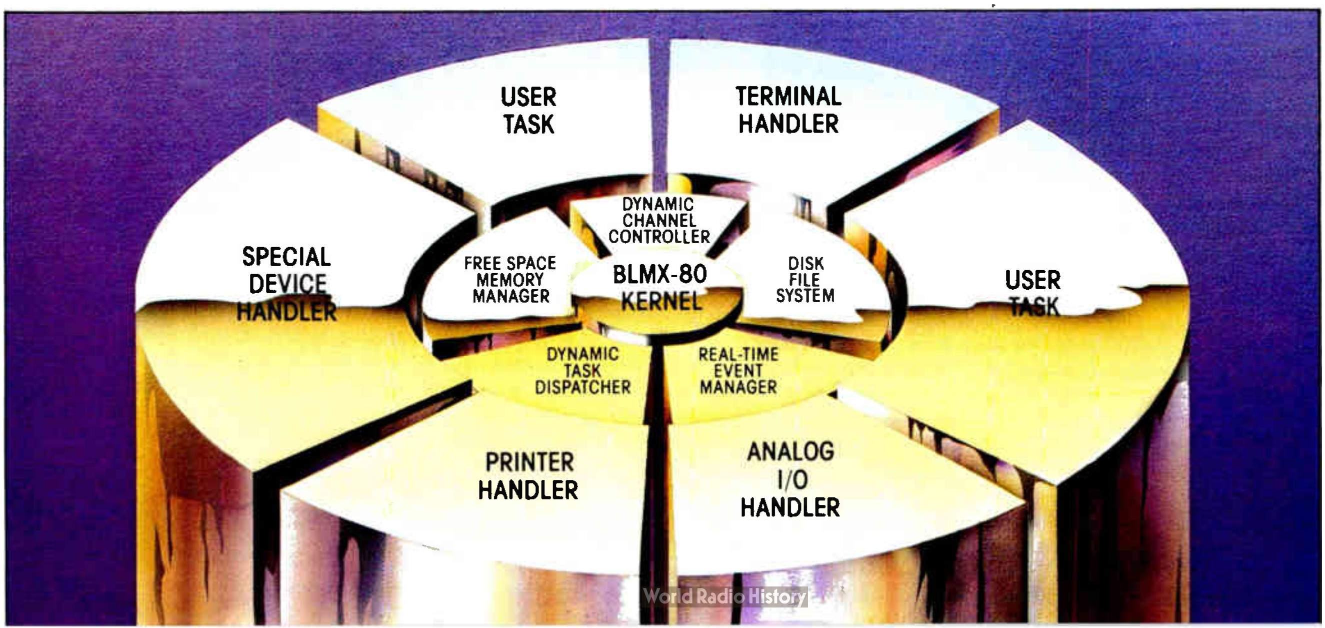
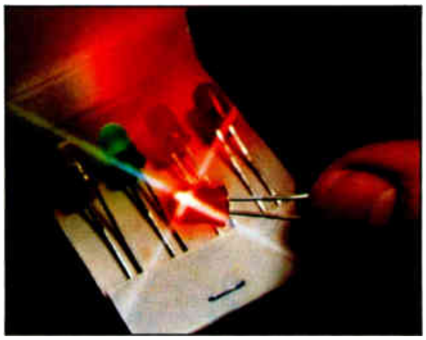


The Perfect Match lights the way to LED uniformity.



New MV5X5X Series cuts LED system costs.

National Semiconductor takes the first big step toward opto standardization with their new MV5X5X Series of T-1¾ LED lamps. These lamps eliminate the need to maintain multiple application design standards to accommodate the various lamps available. As a result, LED system costs are significantly reduced and inventory control is simplified.

Mechanically and optoelectronically identical. The Perfect Match LED's are painstakingly engineered to exactly duplicate the popular industry standard lamps in lead frame size, bulb shape/height/diameter, standoff, color and diffuser level.

And they're now available in all five industry colors: standard red, high-intensity red, green, yellow, and high-intensity orange.

Check box 102 on the National Anthem coupon for complete information on National's MV5X5X Series of T-1¾ LED lamps.

The Perfect Match, another striking example of Practical Wizardry at its finest.

National's AQL cards are a sure bet.

Get Acceptable Quality Level specs for all of the Practical Wizards' devices on a convenient card, free from National.

National knows the reliability business. So they know that the performance of their products is defined by a set of quality parameters.

The Acceptable Quality Level (AQL) is the standard by which quality and reliability test results are compared. It's a standard first established by the military for their own special requirements. But now the AQL is used throughout high tech industries on a daily basis.

So now, as a handy reference for the AQL standards, National has put all of this information on a plastic pocket-sized card, free for the asking.

It's an easy-to-use matrix that shows at a glance the acceptance criteria for each sample size of devices, all under MIL-STD-105.

The AQL card gives, for example, the minimum sample sizes to be tested to assure, with a 90 percent confidence level, that a lot having percent-defective equal to the specified LTPD will not be accepted.

It also contains a grid used in making acceptance decisions based on general inspection levels versus lot or batch size.

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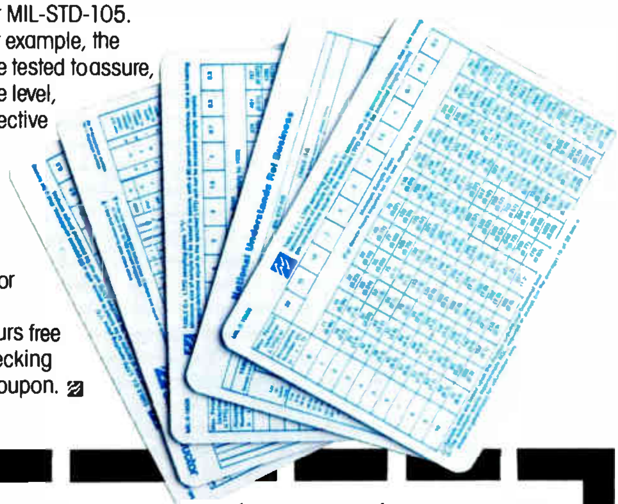

What's new from the National Archives?

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- 051 ☐ Data Conversion/ Acquisition Data Book ($7.00)
- 052 ☐ Data Update— Latest new product information
- 053 ☐ Linear Data Book ($9.00)
- 085 ☐ PALASM and STAR-PLEX Information
- 095 ☐ Acceptable Quality Level Card
- 098 ☐ COP2440 Data Sheet
- 099 ☐ Bubble Memory Data Package
- 100 ☐ BLMX-80 Data Sheet
- 101 ☐ Data Conversion/ Acquisition Brochure and DAC Data Packet
- 102 ☐ Perfect Match LED Information

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NA 31

Washington newsletter

Reagan Administration to push free trade, open world markets

The Reagan Administration is committed to free trade and open world markets in all products not essential to national security and will push for bilateral negotiations preventing foreign governments from subsidizing their exports. These policies were part of a five-point trade policy unveiled July 8 before the Senate by U. S. Trade Representative William W. Brock. He said trade policy will be to push for **eliminating self-imposed export disincentives in Federal laws and regulations; better Federal promotion of exports; tougher enforcement of existing U. S. trade laws and agreements,** as well as renegotiation where necessary; and reduction of U. S. and foreign barriers to the flow of trade and investment among nations.

The Reagan program was criticized by one Republican senator as "an *ad hoc* policy in free-market clothing," while others saw it as noticeably weak on specifics. Initial industry reaction was cautious, characterized by the Electronic Industries Association's observation that it supports the general thrust of the five objectives, while calling for further action by the executive and legislative branches to implement them.

U. S. sales, exports rise in 1980, EIA report says

U. S. factory sales of electronics rose 18.5% in 1980 to about $104 billion compared to the $88 billion level of 1979, and the number of jobs increased an estimated 7% to more than 1.5 million. That's the estimate of the Electronic Industries Association, **which also notes that U. S. electronics exports climbed more than 20% last year to nearly $20.2 billion,** more than offsetting the 13% increase in imports to $13.3 billion. Exports of computers and other industrial electronics rose 20% to nearly $11.7 billion last year, generating a $9.7 billion trade balance by themselves. On the other hand, 1980 saw growing trade deficits in solid-state products, with Japan accounting for $201 million of the $214 million deficit, and in consumer electronics, where the deficit neared $3.7 billion. The totals are in the "1981 EIA Market Data Book" just published by the Washington-based industry association.

Industry posts filled by NASA acting head, defense agency ex-chief

Alan M. Lovelace, acting administrator for the National Aeronautics and Space Administration, left that position last week to join General Dynamics Corp. in the new post of corporate vice president for science and engineering. He **will be responsible for the St. Louis–based company's engineering, research, advanced products, and program development.** Before joining NASA in 1974, he was with the Air Force for 20 years, rising to deputy assistant secretary for research and development.

Lee M. Paschall also has a new job: president and chief executive officer of American Satellite Co., Rockville, Md., a joint venture of Fairchild Industries and Continental Telephone Co. He succeeds William S. Wheatley Jr., who resigned. As an Air Force lieutenant general, Paschall directed the Defense Communications Agency from 1974 until his retirement in 1978, when he became a communications industry consultant.

Solarsat too costly, council concludes

The prospects for Government support of a satellite power system appear to be killed for at least the next decade by a National Research Council study. **The cost of a 60-satellite SPS for the U. S. is beyond the nation's economic capability,** says the council, which found no insurmountable technical problems to the long-term development of geostationary satellites employing massive photovoltaic arrays to convert solar energy into micro-waves for relay to earth [*Electronics*, April 27, 1978, p. 96]. The study concluded that the $1.3 trillion price tag of last year's estimate by the Department of Energy and the National Aeronautics and Space Administration is "two and a half times too low, even in the most optimistic view." It also put the cost per kilowatt at a minimum of $10,000, compared to the estimate of $4,000 from the Energy Department and NASA and the present $1,000 for conventional power systems.

Commerce unit aims frequency monitor at Army use

A computer-controlled receiver system for spectrum management, electromagnetic-hazards measurements, and communications-site surveying has been developed for the Army Communications Command by the Commerce Department's National Telecommunications and Information Administration. Called TAEMS, for transportable automated electromagnetic compatibility measurements system, **the monitor uses commercially available equipment and operates from 1 kHz to 40 GHz,** NTIA's Institute for Telecommunications Sciences, Boulder, Colo., says it has broad potential applications. In addition to the extended frequency coverage, TAEMS has multiple antenna selection, built-in test and noise-measurement capabilities, and a 160-dB measurement range.

Post Office sends mixed message on electronic mail role

The U. S. Postal Service is not planning to go into the telecommunications business to transmit its electronic computer-originated mail (ECOM) even though it could contract with a private carrier to do so. But that assurance by Paul E. Jaquish, senior assistant postmaster general for research and technology, did not convince an industry audience at a USPS meeting this June. Charles S. Shaw, director of USPS electronic-mail systems development seemed to suggest during the session that **the postal service may indeed venture into telecommunications if the ECOM service expands after it begins next year.**

Under the controversial ECOM plan, initially serving 25 post offices in as many cities, the USPS expects a daily minimum of 200 computer-mail messages, each averaging 1,200 characters. Mailers will directly dial the post offices, where ECOM hardware developed by RCA Corp. will print and mail messages for next-day delivery. Users, who will pay a $50 annual ECOM fee and maintain a deposit account, will pay 26¢ for the first page and 5¢ for each thereafter.

SBS sets test of Ku-band receivers

Satellite Business Systems has set **July 22 for the first technical demonstration of its Ku-band (12 to 14 gigahertz) satellite** launched earlier this year. SBS says the demonstration at its McLean, Va., headquarters will give manufacturers of receive-only Ku-band equipment an opportunity to test their hardware in operation with the satellite transponder.

EIA warns House of import assault on U. S. telecommunications

The $20 billion U. S. telecommunications equipment market is "targeted for a concerted attack by foreign competitors" whose home markets remain closed to U. S. exports, says John Sodolski, a vice president of the Electronic Industries Association, in testimony before a House subcommittee. **The technological lead of U. S. producers is thereby threatened** with erosion, he said, unless the U. S. is able to compete "fully and fairly" in Western Europe and Japan.

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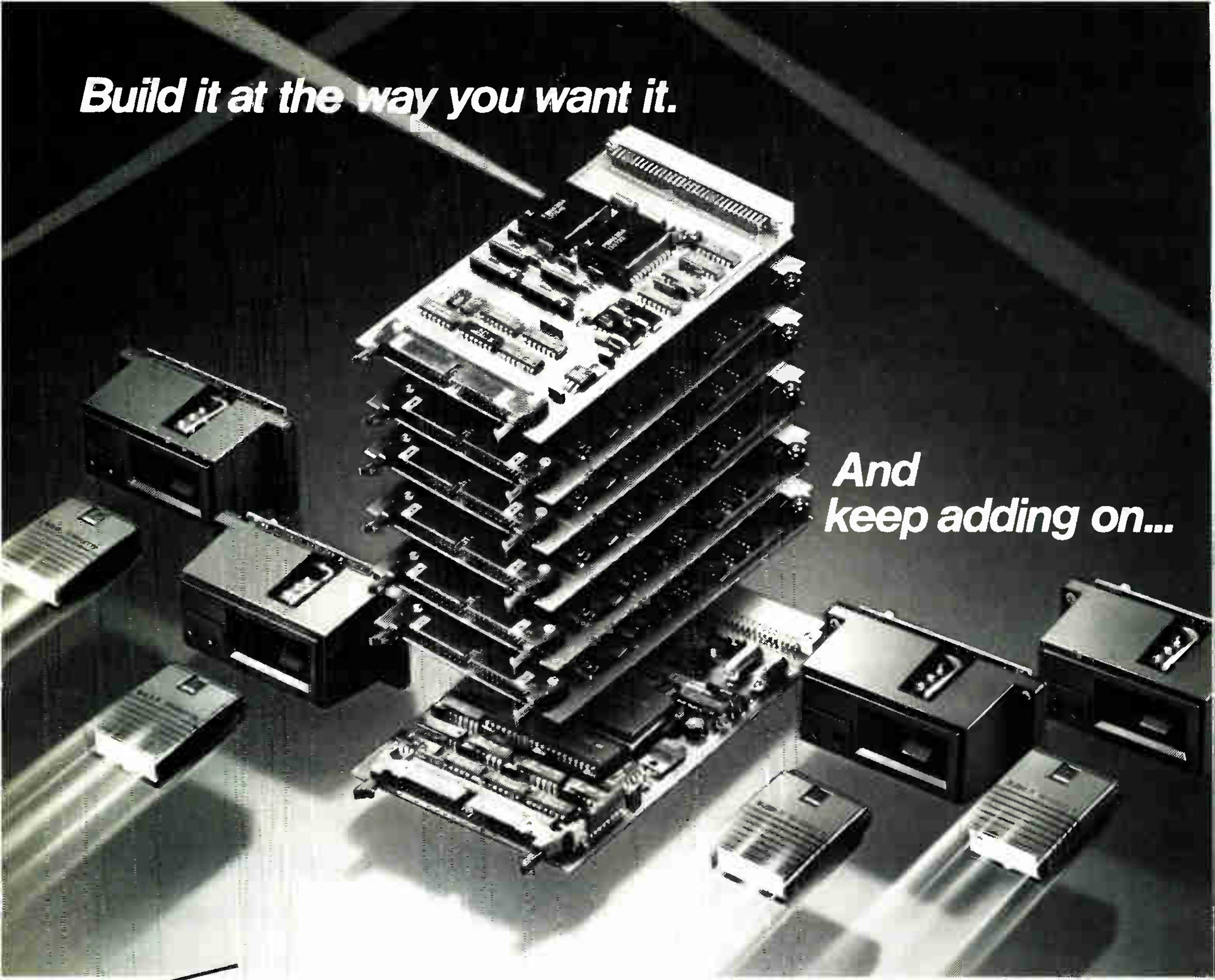

Expandable up to 512Kbytes

Fujitsu's Bubble Memory Euro-Card System

Fujitsu's all-new bubble memory Euro-Cards let you start wherever you want and build up as you go. As you expand, you'll be choosing from up to six bubble memory cards and four exchangeable bubble memory cassettes (or both combined), totalling a whopping 512Kbytes memory power — all in one LSI system. And all at the pace you choose.

Along with this expansion flexibility, the Fujitsu Bubble Memory Euro-Card System offers these valuable features:

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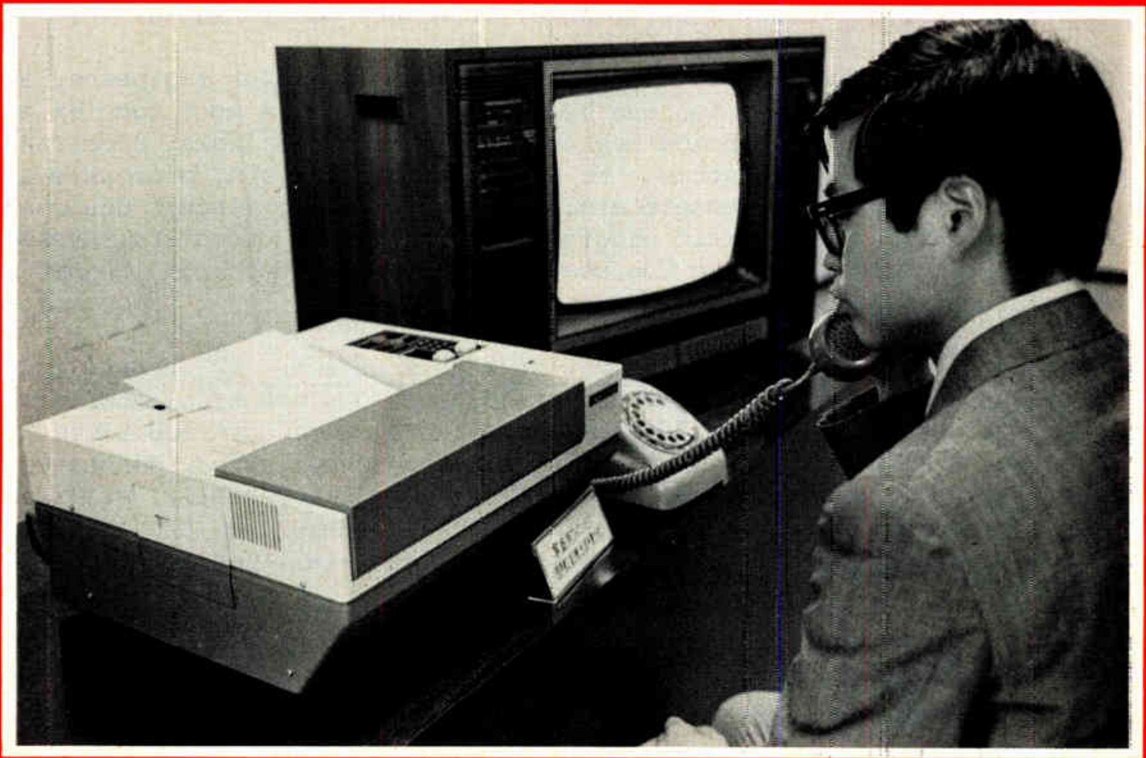
Circle 222 on reader service card

Electronics International

July 14, 1981

One-gun color TV tube has no mask: page 73

This Japanese prototype of a facsimile unit for use in the home can receive both TV broadcast and telephone signals: page 76



SCIENCE/SCOPE

A charge-coupled memory device that can be made with only one additional mask is now under study at Hughes. The chip is a CCD mask-programmable nonvolatile serial read-only memory. It's programmed by a two-step implantation into the region underneath the storage gate electrodes. The first implantation puts buckets of charge under the selected gates using an n-type dopant for n-channel devices and a p-type dopant for p-channel devices. The second implantation uses the same mask and an opposite polarity dopant. Its purpose is to offset surface potential changes that occurred as a result of the first dopant. Implanted regions retain information after start-up by the use of refresher circuits between input and output. The chip also can function as a standard CCD.

A new all-optical logic device could make many electronics systems immune to effects of natural or man-made "noise," including lightning strikes and radio interference. Hughes scientists have fabricated a high-speed optical device that uses no electronic signals. It is made of discrete components, including four reflecting surfaces and a slab of nonlinear material (gallium arsenide). The device has shown optical bistability (flip-flop behavior) with switching times of 3 nanoseconds and switch energies under 100 microjoules. Although propagation delays have kept the device's speed under the theoretical limit up to 10 gigahertz, the speed will be increased by further miniaturizing of the device on an integrated optic chip. The device could be used in fault-tolerance computers, flight control systems, and ultra high-speed signal processors.

A communications system delivered to the U.S. Navy saves weight and space over previous systems. The Hughes tactical information exchange system (TIES) uses a single set of hardware to accommodate many different digital and voice communications processing. This was made possible by a new frequency translator unit and a programmable signal processor. Previous systems used separate pieces of equipment for amplitude modulation or frequency modulation of voice and data.

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A copier that uses a laser scanner to read a page in two seconds can send very high quality copies to widely dispersed locations via satellite. The copier transmits at speeds up to 70 pages per minute, more than 100 times faster than conventional facsimile. Also, using electronic collating, documents of more than one page can be printed at many locations sequentially, eliminating the need for mechanical sorters. AM International developed the copier for Satellite Business Systems. Hughes built the satellites and earth terminals.

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Will fiber optics oust communications satellites?

Fiber-optic data links could be pitched against their satellite counterparts if Britain's Department of Industry liberalizes British Telecom's common-carrier monopoly as recommended in a report the former commissioned from Prof. Michael Beesley of the London Business School. British Aerospace and IBM Corp. are already eyeing a satellite business service [*Electronics*, June 30, p. 64] in anticipation of a favorable decision, and now a consortium including Cable Wireless Ltd., Barclays Merchant Bank Ltd., and British Petroleum Ltd. is **proposing a 512-Mb/s dedicated ring system**—about eight thousand 64-kb/s digitized voice channels carried on four 140-Mb/s fiber pairs—laid between major cities alongside railway tracks. Connections to access nodes would be via 10-GHz cellular radio links, and wide area coverage would be provided on a single frequency by operating the transmitter network in a time-division multiple-access mode, with wideband data links going to customers carrying data at rates of up to 2 Mb/s.

Step-and-repeat X-ray aligner resolves 0.5-μm rules

The Musashino Electrical Communication Laboratory of the Nippon Telegraph & Telephone Public Corp. has developed what it claims is the world's first step-and-repeat X-ray aligner. It is a prototype of the next generation that will be needed when large-scale integrated circuit patterns become too fine for the optical step-and-repeat units now going into operation on production lines. The new aligner **can expose at least five 3-in. wafers each hour** with 0.5-μm rules while maintaining an alignment of better than ±0.1 μm. Yet its estimated cost is only about a third that of an electron-beam aligner because no pattern-generating system is required.

Synchrotron system to aid West German VLSI

West German government and electronics industry officials expect their ability to manufacture very large-scale integrated circuits to receive a big boost from a new synchrotron radiation system nearing completion in West Berlin. The $25 million system, dubbed Bessy (for the German for Berlin electron storage ring for synchrotron radiation), will provide radiation intermediate between ultraviolet light and X rays with which it will be **possible for semiconductor companies to produce line widths of 1 micrometer and below.** Financed mainly by the Bonn government and slated to be operational by mid-1982, the system essentially consists of an evacuated ring-shaped tunnel some 12.5 meters in diameter. Electrons are shot into it at high speed and kept on the ring course by powerful magnets, producing X-ray–like radiation.

Cure for electrolytic migration in vhf circuits found

The Centre Nationale d'Etudes des Télécommunications, Lannion, France has come up with a method of preventing electrolytic migration between layers of circuits that perform at very high frequencies. The circuits were originally composed of gold photoengraved on a chrome layer mounted on either a sapphire or silica substrate.

The problem was that the chrome migrated to the gold causing poor adhesion. The CNET solution is to **separate the gold and chrome with a layer of titanium nitride,** thus stabilizing the chrome layer and giving it a dilation coefficient about equal to that of the substrate. The first samples produced by this method have also responded well to soldering by thermocompression and show normal electrical performance.

International newsletter

Japan looks into teletex service

Japan's Ministry of Posts and Telecommunications will start studies this year that it hopes will enable it to standardize the transmission of Japanese language teletex by the summer of 1983, thus going some way to meet the nation's demand for better communications. At the same time it should greatly **increase the usfulness of the growing number of word processors** now becoming available and accelerate the trend toward office automation. To control transmission, it should be possible to use a protocol similar to that recommended for teletex by the International Consultative Committee for Telegraphy and Telephony last November.

Semiconductor sales off 5% in West Germany

West Germany's semiconductor market, the leading one in Europe, is doing worse than had been anticipated earlier this year. According to marketing officials at both domestic and foreign producers operating in West Germany, sales this year will for the first time in the past half-decade fall below last year's. To break out the overall 5% drop, sales of integrated circuits will be down by more than 1%, while those of discretes will plummet by a whopping 12.5%. In terms of value, the 1981 market, which industry officials had earlier predicted would reach $625 million, will **most likely check in at a disappointing $585 million.**

Japanese to design new defense system

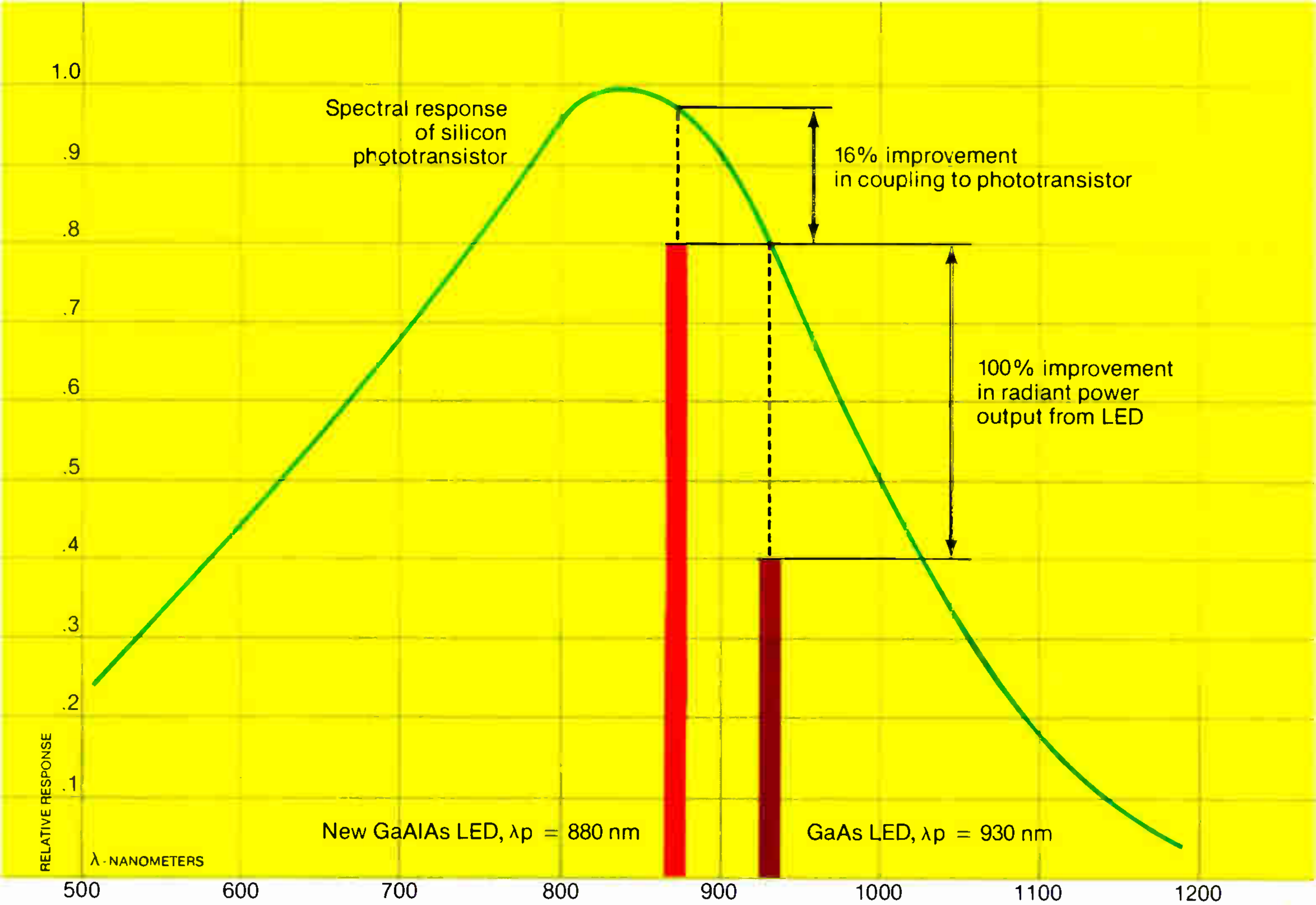
Five Japanese electronics manufacturers are gearing up design groups in anticipation of a request for proposals from the Japan Defense Agency for a new Badge (for base air-defense ground-environment) system that integrates radar sites and air defense center computers for decision making in the deployment of surface-to-air missiles and fighter aircraft. Price of the Badge system, which is expected to be completed in 1987 at the earliest, **is on the order of $900 million to $1,350 million. The selected firm among the five—Nippon Electric, Mitsubishi Electric, Toshiba, Hitachi, and Fujitsu—may have to subcontract part of the job to a U. S. defense contractor** to acquire weapons-related expertise. The present Badge system was delivered in 1968 by a joint venture of Hughes Aircraft and Nippon Electric.

Tablet captures handwriting for computers

As a means of entering computer data, the cathode-ray tube keyboard may have to make room for data tablets that accept stylized handwriting. One of the first companies to develop them is Britain's Bristol-based Image Data Ltd., whose latest model **accepts clearly formed handwriting, as well as sketches.** It also incorporates a touch-sensitive keyboard for function selection that doubles as a calculator. The microprocessor-based unit, which sells for $3,200, uses a drift-free sensing technology with an absolute positional accuracy of 0.5 mm. A food company has already ordered tablets for its telephone sales personnel.

Addenda

On July 20, Japan will start commercial trials of a facsimile mail service between the central post offices of Tokyo, Osaka, and Nagoya. Letters will be sent for $2.18 for the first page and $1.31 each for additional pages. . . . Nippon Kogaku KK has developed **the fastest-yet electrochromic display whose deep colors can be read from any angle.** A porous thin-film insulator separates two color-forming layers, letting the gas evolved in one layer pass through to the other to speed turn-on time.



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All of our products are 100% electrically tested, followed by a quality control inspection to a cumulative .65% AQL. Our Quality Enhancement Goal is 200 PPM.

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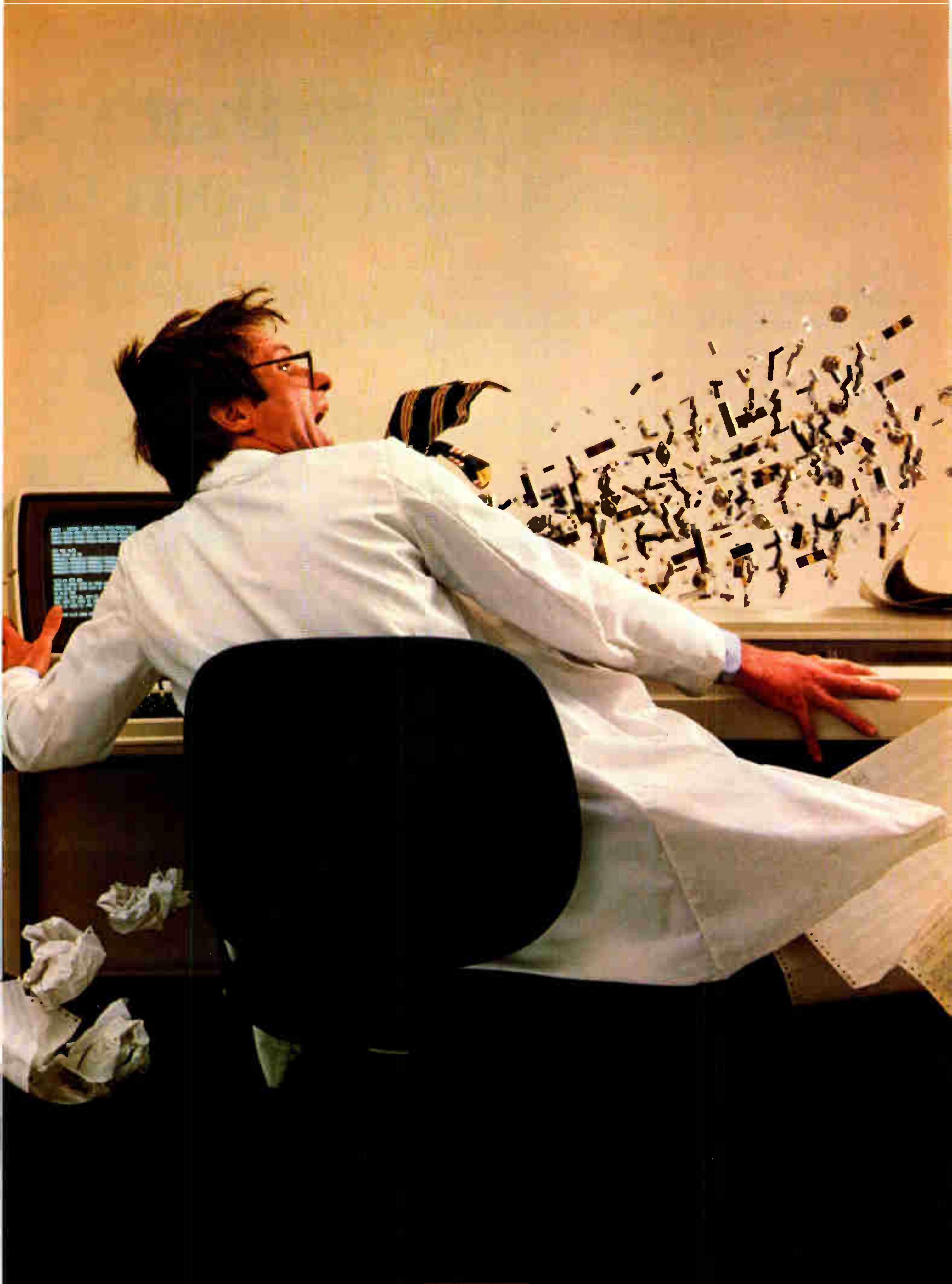

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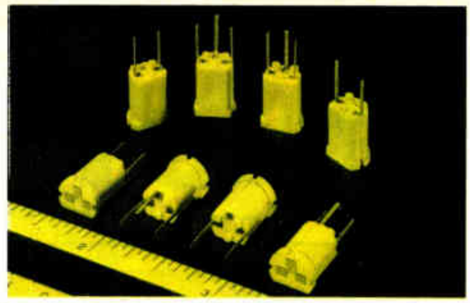

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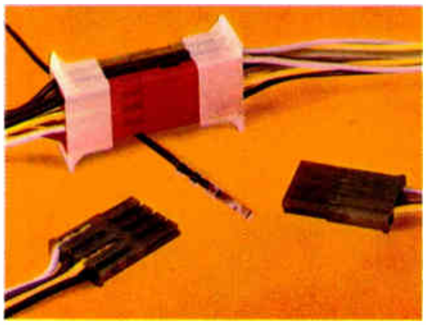

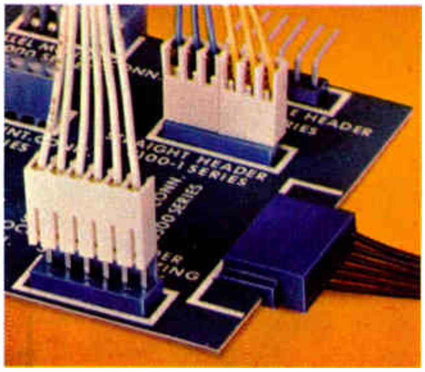

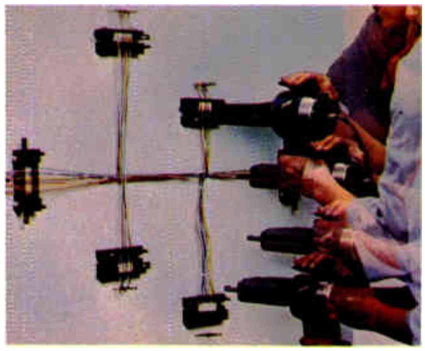

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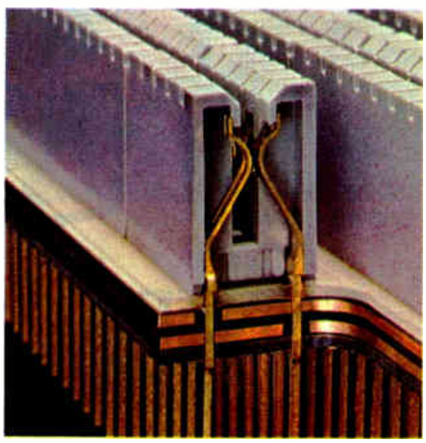

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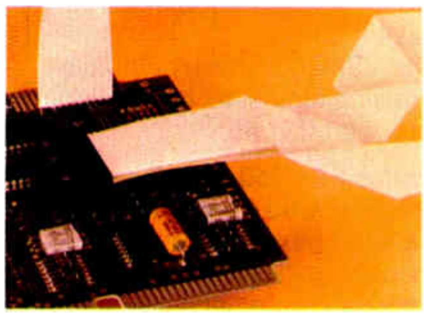

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Color TV tube needs no shadow mask

by Charles Cohen, Tokyo bureau manager

Index signals from faceplate direct single gun to fire three 'colors' of video signal at matching phosphor stripes

An experimental color television tube of the beam-index kind, which uses only a single electron beam and has no need of a color selection mask, requires much less power than the usual shadow-mask type and could also cost less. And the image is improved, being slightly brighter and without any misconvergence, even in the corners.

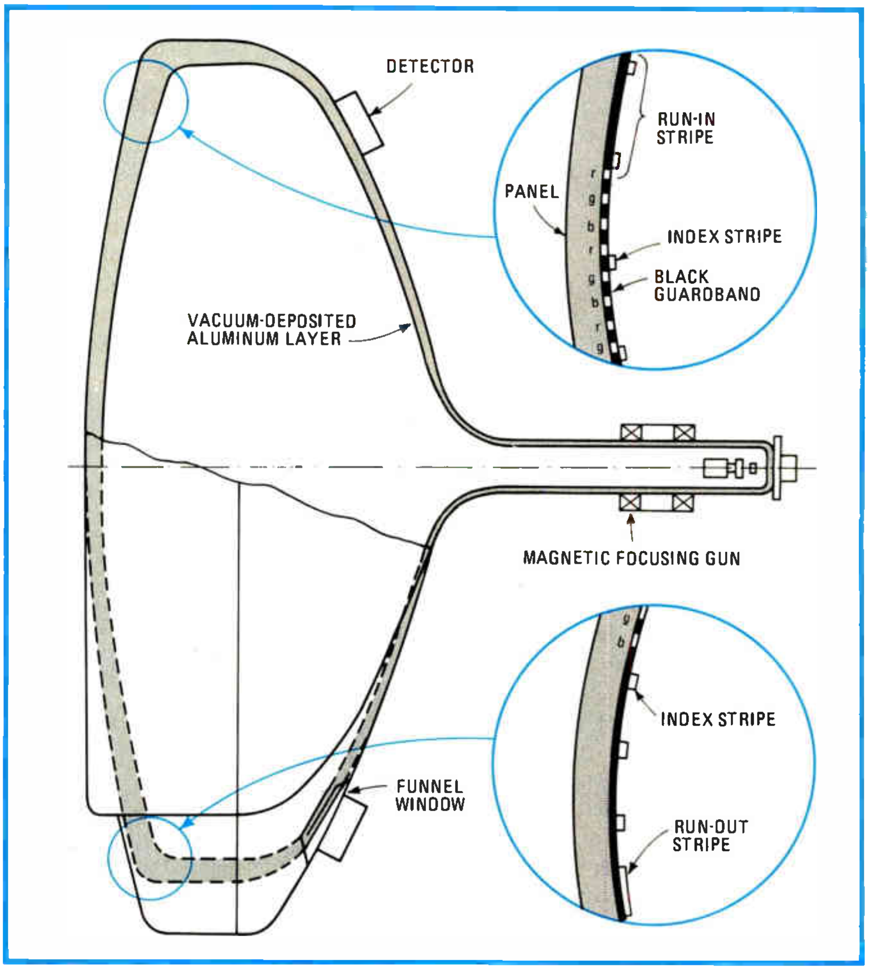
The 30-inch tube is made by Japan's Sony Corp. It employs a bulb with the same 32-in. outer diagonal as the firm's largest shadow-mask–type Trinitron tubes.

Akio Ohkoshi, general manager of the Electronic Devices Development division, says that the firm selected the largest tube size because it promises the greatest cost reduction. The number of circuits and other artifacts a tube requires is independent of its size, whereas the cost of the shadow mask increases with size.

Inside. The tube has a repeating pattern of vertical red, green, and blue phosphor stripes separated by black stripes of the same width. As the electron beam sweeps horizontally across the face of the tube, electronic switching circuits feed the electron gun's grid with a sequence of primary-color video signals matched to the sequence of colored stripes. As in other beam-index tubes proposed from the early 1950s on, periodic index stripes on the inside of the faceplate respond to the electron beam as it passes over them with a signal. This signal is used to synchronize the switching circuits with the motion of the beam.

To generate the index signal, Sony uses a short-persistence green phosphor on top of the aluminum screen backing of every fourth black stripe. To detect the signal, a p-i-n photodiode is used. Photodetectors consisting of a hybrid circuit with the sensitive p-i-n photodiode and a 30-megahertz monolithic preamplifier are attached at four windows on the picture-tube funnel to pick up the index signal from the four quadrants of the faceplate (see figure).

Two factors contribute to the tube's low power. Because its single-beam electron gun is smaller in



View from the top. This TV tube's vertical red, blue, and green phosphor stripes are swept horizontally by matching primary-color video signals from the single electron gun.

diameter, its neck can also shrink to 30.6 millimeters from the 36.5 mm normal for this size of tube—so that the deflection coil is smaller and deflection therefore uses 20% less power. Moreover, beam current is decreased by about two thirds because there is no shadow mask to intercept electrons. The total power consumption of a prototype TV set is 160 watts, 45 W less than that of a comparable commercial 30-in. TV.

Several innovations are used to make a reliable beam-index TV. A constant dark current of less than 1 microampere ensures an index signal even in dark portions of the screen. This current gives a screen brightness of only 0.3 footlambert. Since the maximum screen brightness exceeds 120 ft-L, the contrast ratio is more than 52 decibels. Signals from a run-in region of six index stripes at the left-hand side of the screen serve to ensure synchronization on each scan. Together with signals from a run-out region at the right-hand side (see figure, p. 73), they are also used to stabilize picture width despite changes in brightness. This is extremely important because switching frequency is directly proportional to scan width.

The tube also improves its performance by correcting the linearity of the scan as it travels across the screen. The picture tube screen is sliced horizontally by 34 lines and vertically by 14 lines. The points where these lines cross are used for the acquisition of linearity data, which is stored as 6-bit samples in a 4-K random-access memory. Each time the channel is changed, the screen is driven momentarily to full white brightness for best pickup of index information and then data for linearizing the scan is stored.

Unmuddied hues. For the best color purity, the electron gun shoots a vertically oriented rectangular beam. This rectangle is tilted when the beam is deflected to the corners of the screen, but dynamic correction is provided by a magnetic quadripole on the tube neck. Color purity is thus maintained even at the corners.

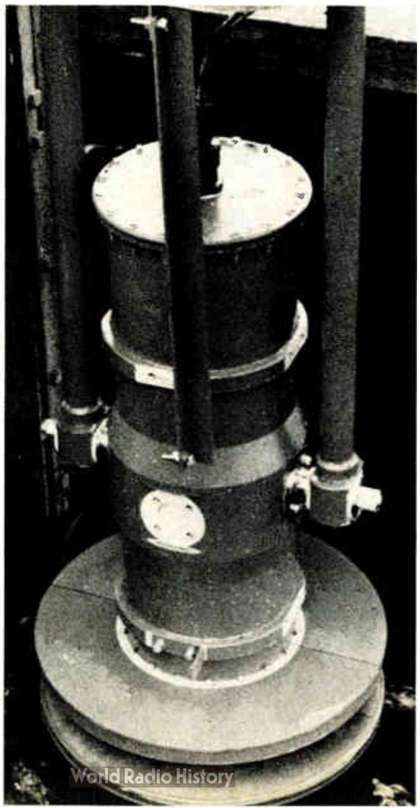
Sony will not say when it will produce the new tube. Some capital investment is required, in particular for the automated line that would fabricate the new single-beam electron gun. On the other hand, set manufacturing costs could probably be cut by about 5%.

Three years ago, Matsushita Electric Industrial Co. built a prototype portable color TV around a 7-in. beam-index tube fabricated by subsidiary Matsushita Electronics Corp. [*Electronics*, Sept. 28, 1978, p. 67]. The aim was not lower cost or a better picture but power consumption low enough for the set to run on dry cells. That project is now in limbo, though, because the demand for and price of this type of set are both low. Sanyo Electric Co. also built a small beam-index tube similar to Matsushita's as a vehicle with which to start a picture tube division, but failed to follow through.

Great Britain

Solid-state sonar builds on new sensor

A plastic with far greater piezoelectric sensitivity than conventional inorganic materials is bringing sonar technology into the solid-state era. Soon electronically scanned sonar arrays with no moving parts will be displacing more conventional mechanically scanned sonar heads in the lethal hide-and-seek game of submarine warfare.



But while research interest in these sonar arrays, printed on thin films of polyvinylidene fluoride (PVDF), a highly piezoelectric organic compound, is strong and though systems using the technology may already be afloat, little of this work has been made public. One exception is Britain's Marconi Space & Defence Systems Ltd., whose Naval and Ocean Engineering division in Camberley, Surrey, recently launched two PVDF-based systems: a fixed installation sonar for protecting harbors, oil rigs, and other strategic installations, plus a towed small-boat sonar system. Both were developed privately.

Electronic scanning with these arrays is more reliable and cheaper and occupies less space than conventional scanned systems, making it practical for the first time to equip boats as short as 12 meters with sonars, according to Clive A. Bridges, manager of the division. But perhaps more importantly, the sensing material, PVDF, is 30 times more sensitive to underwater sound than conventional piezoceramics.

Untrimmed. Moreover, says R. H. Wisbey, who heads the materials applications group at Marconi's research laboratories, where the new 100-element omnidirectional sonar array was developed, "PVDF has a number of other advantages by virtue of its being plastic. Because its acoustic impedance is reasonably close to water's, it naturally has a broadband capability and need not be trimmed to resonance."

Operationally, this last factor is extremely important, explains Bridges, because lower frequencies give long-range penetration through the water and higher frequencies can be used to obtain high resolution close in. For instance, the Marconi

Ultrasensitive. This solid-state sonar head located near a harbor entrance picks up movements of underwater objects as close as 25 meters or as far as 1.2 kilometers

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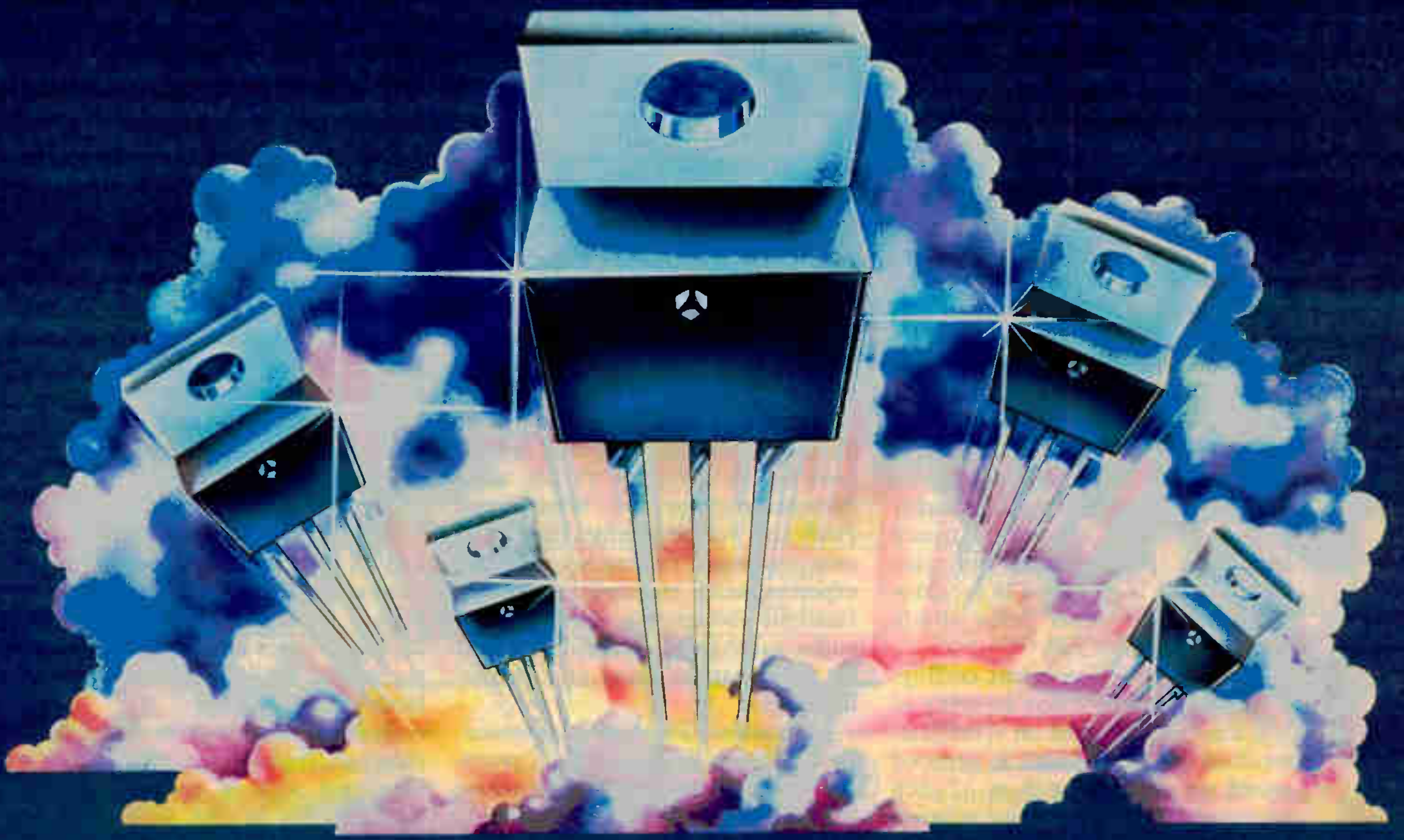

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Circle 75 on reader service card

tor of Matsushita Graphic's facsimile research laboratory, says that the use of an error-correcting code would permit the use of redundancy reduction and greatly speed up transmission.

As for the other system, which receives analog fax signals, it uses a second subcarrier at six times the TV horizontal sweep frequency, approximately 94.500 kilohertz. It is frequency-modulated with a maximum modulation frequency of 15.6 kHz.

Mixed blessing. The two systems represent both good news and bad news for Japanese manufacturers. The good news is that the analog TV mode has been recommended by the Radio Technical Council, a group ranging from professors to journalists that advises the minister of posts and telecommunications on matters related to the administration of the radio spectrum. Thus if the analog mode proves out in tests, it could possibly be in commercial operation in as little as five years and open the way to a large new consumer market. Manufacturers estimate that consumer quantities would bring prices down to the level of large color TV sets, about a tenth the price of the G-3 terminals now sold to offices.

The bad news is that, although the digital TV mode is the more interesting and promising of the two, the council has not yet considered it. Thus it might take as long as 10 years for the digital mode to go into operation—an additional 5-year delay before the start of the new market. **-Charles Cohen**

West Germany

3 digital services fit onto phone wire

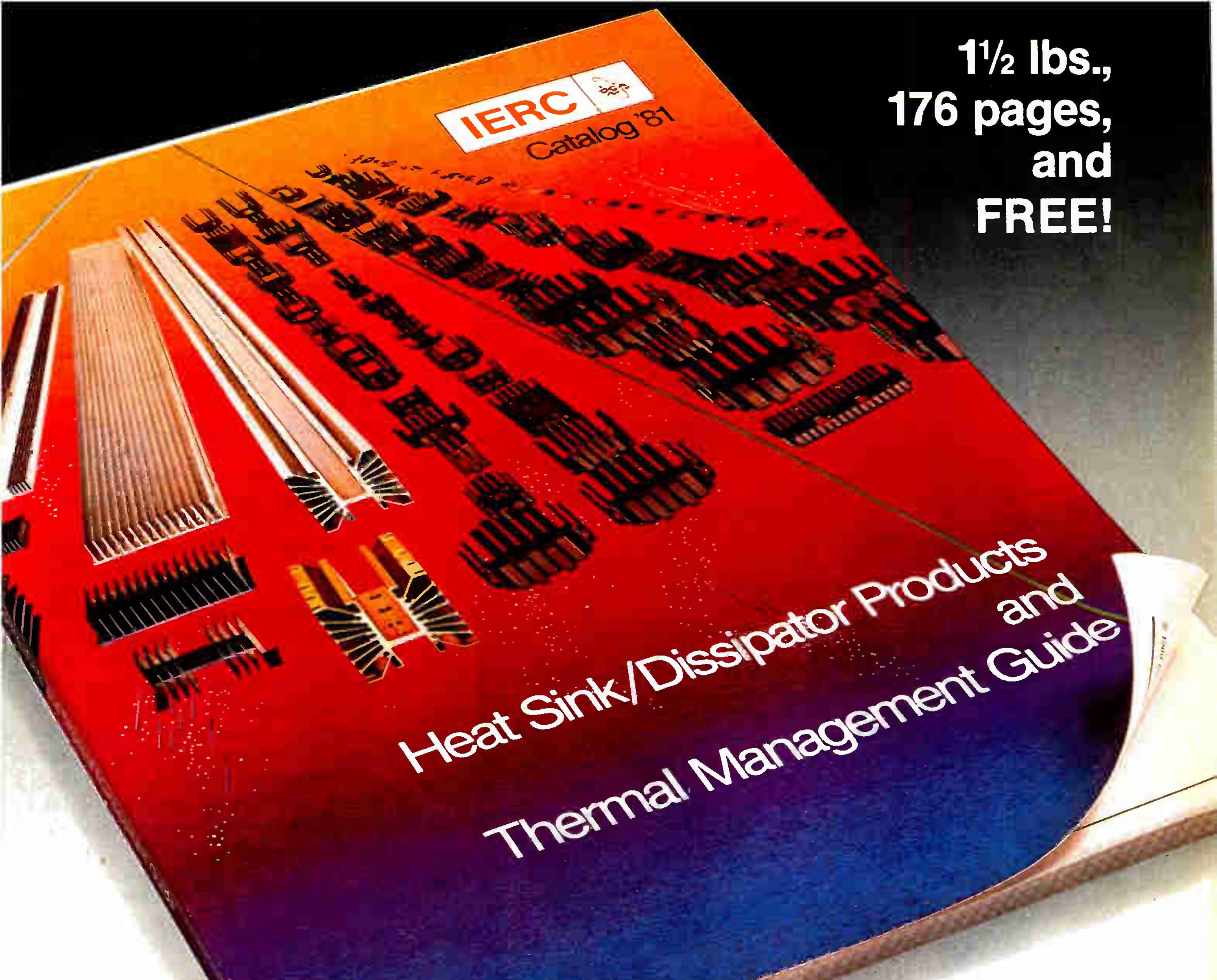
Teletypewriter, teletex, and videotex signals, all in parallel with voice signals, have been sent over a pair of ordinary copper telephone wires in trials that the ITT subsidiary Standard Electric Lorenz AG has just completed in West Berlin. By using very large-scale integration, the digital circuitry required for such communications will eventually become small enough to fit inside the subscriber's telephone.

The SEL trials were part of a project called Digon, the acronym for the German for digital local network, that West Germany's post office is carrying out with the aid of the country's communications industry and a Stuttgart University institute. Stuttgart-based SEL has been assigned the task of proposing and trying techniques for transmitting speech as well as new communication services over two-wire continuous phone lines about 4 kilometers long and having a wire diameter of 0.4 millimeter.

Already in place. On first mention, the use of existing wires instead of more advanced transmission media such as glass fibers may not sound all that progressive. But with more than 20 million phones connected to it, West Germany's subscriber network represents an installation value of more than $7.6 billion and will thus be in place for some time to come.

The SEL system is based on standard pulse-code modulation techniques for transmitting digitized speech. However, instead of the usual 64-kilobit-per-second rate, it employs 80 kb/s. The main, or 64-kb/s, channel is for either speech or fast data transmission. The extra 16 kb/s is occupied by an 8-kb/s channel for one or more services like teletex, teletypewriter and videotex, and another 8-kb/s channel, the so-called delta channel, for exchanging remote signaling and synchronization characters between the subscriber's telephone set and the central switching equipment.

The bit frame used contains 320 bits divided into 32 words, each 10 bits long. Of these, 8 bits are assigned to the main channel and 1 each to the delta and the additional-services channels. The signaling information is coded in data words. On-hook and off-hook conditions are signaled in the delta channel by a digital event signal (rather than a direct-current status signal) since that allows the wires to be replaced



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Circle 79 on reader service card

by glass fiber lines without modifications.

For transmitting a bit stream over a pair of phone wires, explains Lorenz Gasser, head of predevelopment in SEL's Private Communications division, SEL used a modification of the conventional two-wire/four-wire conversion hybrid separation technique, in preference to the time- and frequency-separation approaches. With the classical hybrid method, digital signals cannot overcome the 50-decibel-or-so attenuation encountered in 4 km of wire 0.4 mm in diameter.

The answer. However, digital signals can be made to bridge that attenuation with a controlled digital filter that compensates for unwanted echoes—signals stemming from reflections and not sufficiently suppressed by the loss encountered in the bridge hybrid in the telephone. Since there exists a distinct relationship between the transmitted signal and the unwanted signal at the other end of the hybrid termination, the degree of compensation depends in principle on how many filter control criteria and coefficients are used for the digital filter, Gasser says.

The Stuttgart firm preferred the hybrid technique to the other two approaches because it allows the use of lowest frequencies—down to 30 kilohertz for an 80-kb/s transmission rate—which, in turn, means it can bridge the longest distances. To be sure, the other methods are easier to implement since they do without echo compensation. But with VLSI technology, Gasser points out, it should be possible to integrate echo-compensating devices at low cost.

Chips coming. For the West Berlin trials, SEL implemented the three digital services with commercially available components mounted on some 18 printed-circuit boards, all installed in a 19-inch rack. Work is now under way on integrating it all on just one or two VLSI devices. Such devices, Gasser says should be ready in two years or so—in time for international communication authorities to have reached agreement on standards for digital transmissions over wire-based networks. **-John Gosch**

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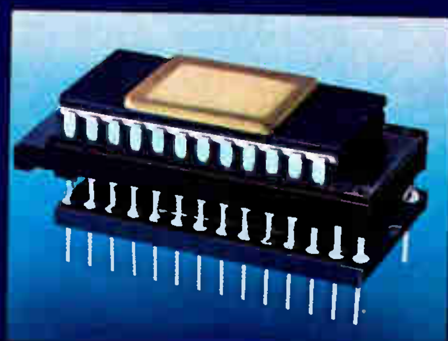

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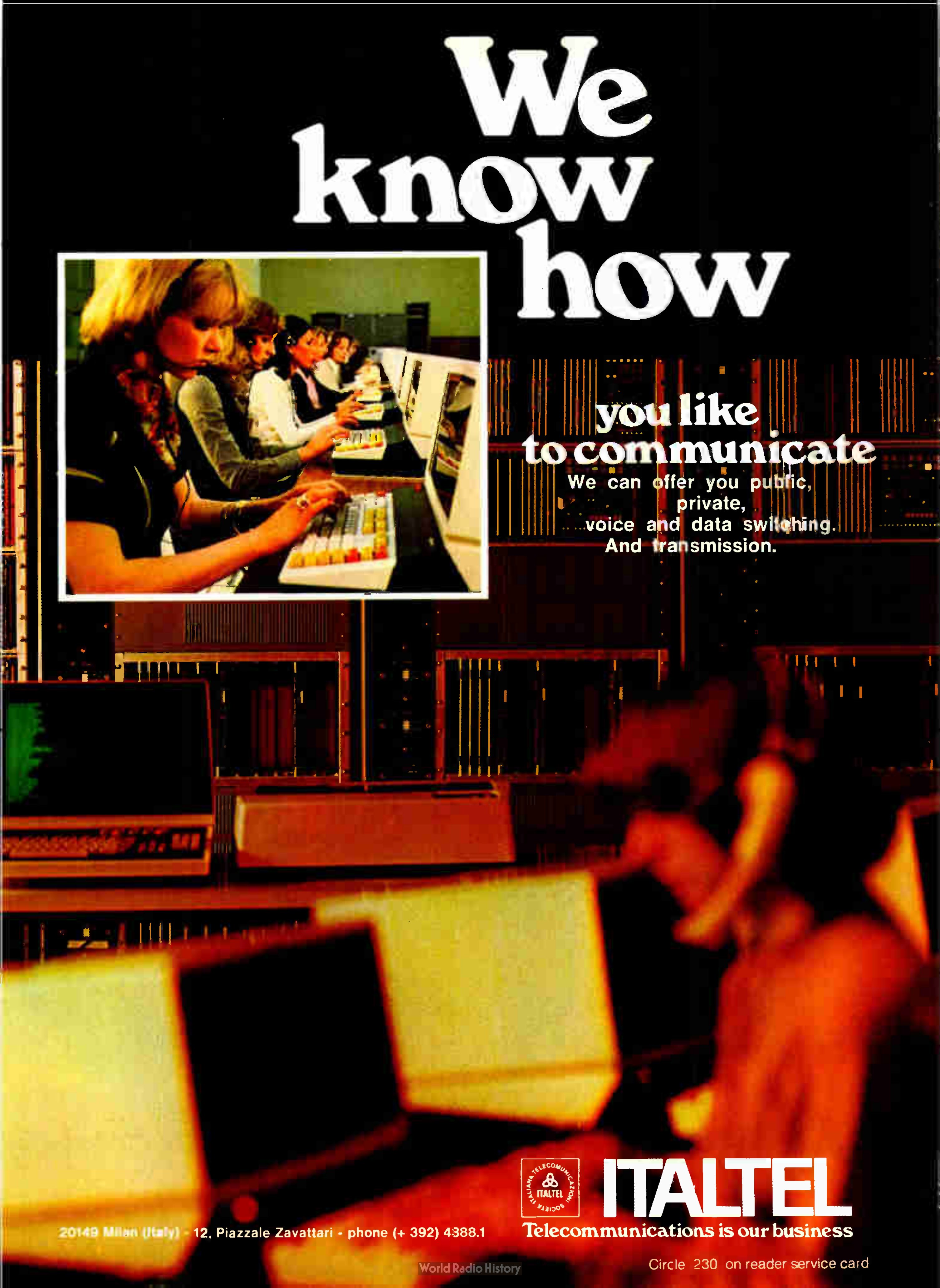
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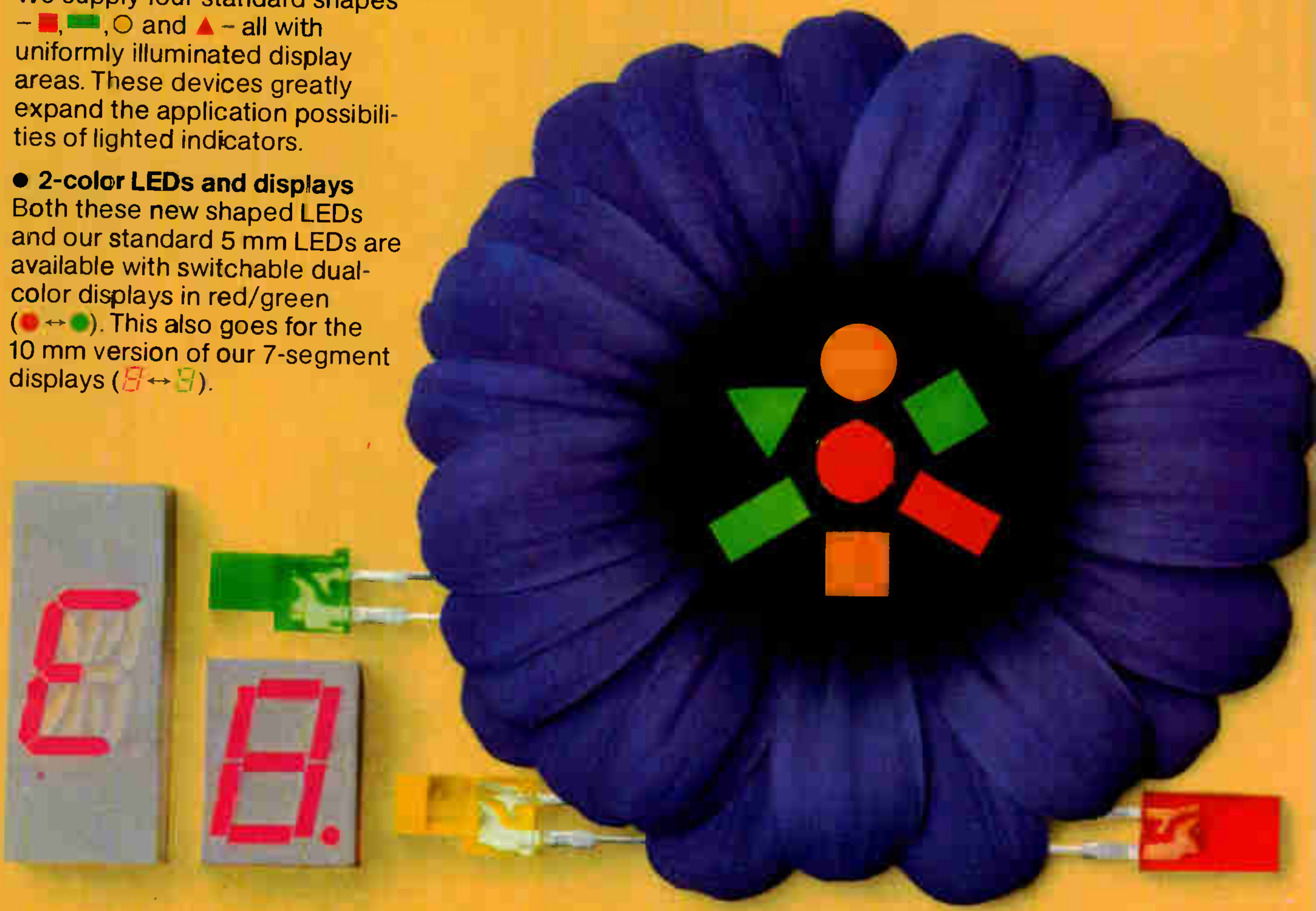

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Direct-frequency crystal oscillator line extends to 1.5 GHz

by Robert Gallagher, Paris bureau

Helium-ion milling technology produces thin, precise quartz resonators that age well and can achieve very high stability

A **helium-ion milling** process brought to bear on quartz-crystal resonators has permitted the Compagnie d'Electronique et de Piézo-Electricité to offer a line of direct-frequency crystal oscillators with outputs of up to 1.5 GHz. "There are very few manufacturers in the world capable of doing work so precise," claims Ranier Unverdross, a CEPE crystal, oscillator, and filter engineer.

The company's oscillators do not employ multiplication, the usual method of obtaining such high frequencies. Though multiplication circuits produce outputs higher in frequency than any useful harmonic present in the input signal from the crystal, CEPE's oscillators obtain their output frequencies directly from a harmonic already present in the crystal's oscillations by filtering out the unwanted harmonics and fundamental.

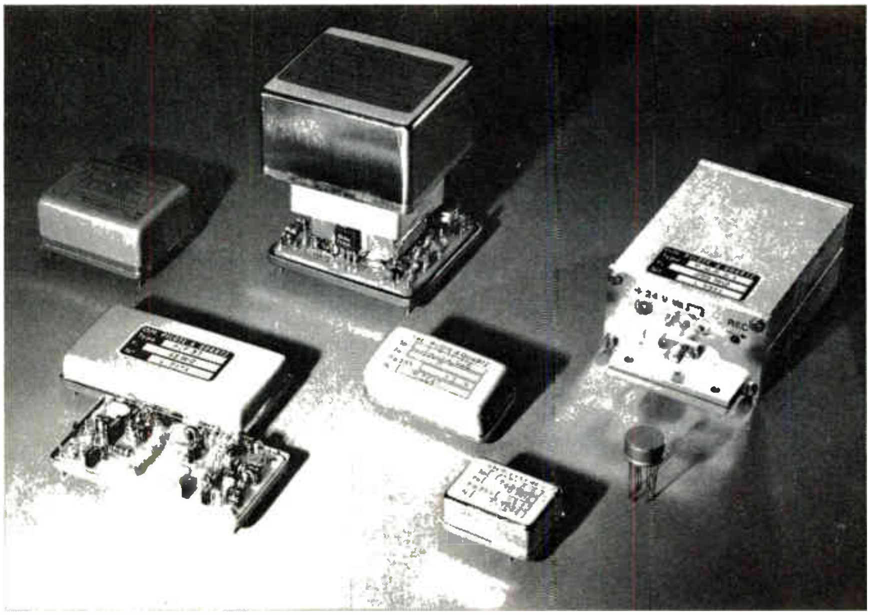
Another advantage of producing quartz crystals with the ion-milling process is stability [*Electronics*, March 10, p. 67]. The company may soon be able to produce crystal oscillators with instabilities as low as 10^{-11} per day, which compares well with rubidium, or even cesium, time bases. Much-improved aging and decreased sensitivity to acceleration are other beneficial effects of ion milling, which gives the crystal a high degree of surface perfection.

To obtain such stable, high-frequency resonators, the crystal blanks are first ground to very fine tolerances. AT-cut quartz crystals are ground to a thickness of 33 μm, where they have a fundamental frequency of approximately 50 MHz; BT-cut quartz goes to 34 μm, or 75 MHz; SC-cut quartz to 37 μm, or 50 MHz; and lithium tantalate resonators are ground to 35 μm, where the fundamental is 60 MHz.

The ion milling process is capable of bringing the fundamental frequencies of the above-mentioned crystal cuts much higher—to 420 MHz for the AT cut, 600 MHz for the BT cut, 450 MHz for the SC cut, and 400 MHz for lithium tantalate. Theory has it that the thirteenth harmonic can be had from an AT-cut crystal, the seventh from BT and SC cuts, and all the way up to the twenty-first harmonic for lithium tantalate. But problems with the parallelism of the crystals' faces at frequencies as high as 4 GHz and the extremely small dimensions of the electrodes set the practical limit well below theory. The third and fifth harmonics are used in CEPE's announced products.

Targeted. The five new oscillators are intended for use in avionics, missile guidance, and telecommunications. Four operate at frequencies up to 500 MHz, using the crystal's third harmonic. The fifth, model BP_5, can be ordered with either a crystal whose third harmonic is used or one whose fifth harmonic is the output frequency. Its output can be as high as 1.5 GHz, though lower-frequency units can be ordered.

The BP_5 is a ground-based version of the BP_3, which is designed for avionics use and carries a BT-cut resonator. Available at frequencies up to 500 MHz, the BP_3 oscillator's

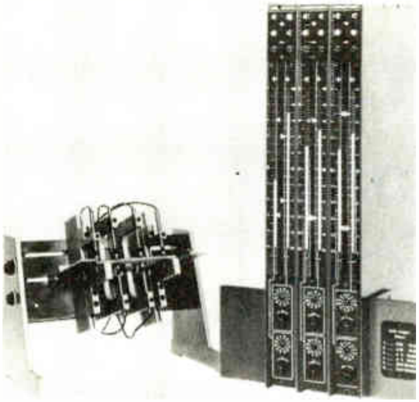


spectral purity and stability are not ideal, but it boasts a particularly short starting time.

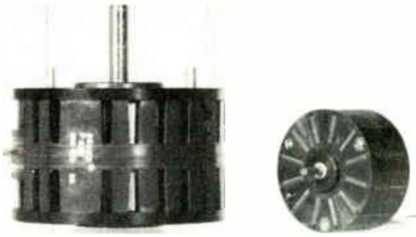
The AP_3 oscillator is for use in radiotelephone and microwave links. With its AT-cut resonator, instantaneous starting, and small package, it is particularly suited to use in portable equipment. The SP_3 also features instantaneous starting and, as it is meant for use in missile guidance, it is conditioned to resist extreme conditions. It uses an SC-cut crystal. The lithium tantalate LP_3 oscillator couples a low noise level with high output power, but its spectral purity is poor. It is set up so that it may be hooked to another oscillator via a phase-locked loop to correct the spectral purity of the signal.

Costly. Prices for the oscillators are not yet available, but they are not low. "To reach these frequencies the amount and quality of work necessary is staggering," says Unverdross. The intended application figures heavily in the price: an oscillator for use in a jet fighter, for example, and the same model for use in a relatively normal ground-based application could differ in price by a factor of three. CEPE expects to deliver the first oscillators from its line later this month.

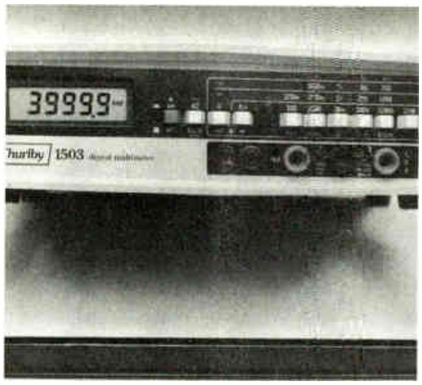
Compagnie d'Electronique et de Piézo-Electricité, 101 rue du PT Roosevelt, B. P. 74, 78500 Sartrouville, France [441]



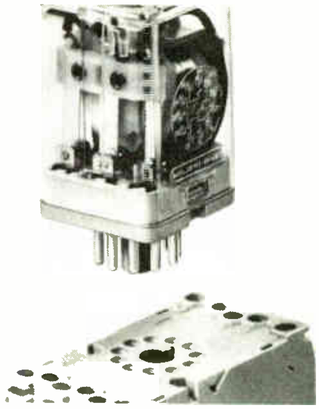
The Sigmacolumn 227-01 is a gaging indicator with a plasma display that has been designed to be operated by the user. It can be upgraded to a fully programmable multichannel system by adding plug-in modules. Sigma Ltd., Spring Road, Letchworth, Herts. SG6 4AJ, England [443]



A family of stepper motors for industrial applications includes the Escap P 312 with 60 steps per revolution and a ½-W continuous output rating and the P 532 with 100 steps/revolution and a peak power output of 30 W. Portescap, 165 rue Numa-Droz, CH-2300 La Chaux-de-Fonds, Switzerland [446]

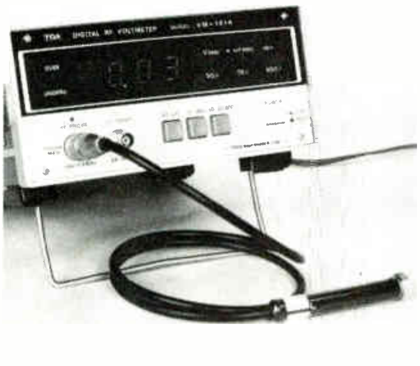


The model 1503 multimeter has a built-in frequency meter. Frequencies of up to 3,999.9 kHz can be measured directly with a resolution of 100 Hz. Thurlby Electronics Ltd., Office Suite 1, Coach Mews, The Broadway, St. Ives, Huntingdon, Cambs. PE17 4BN, England [444]

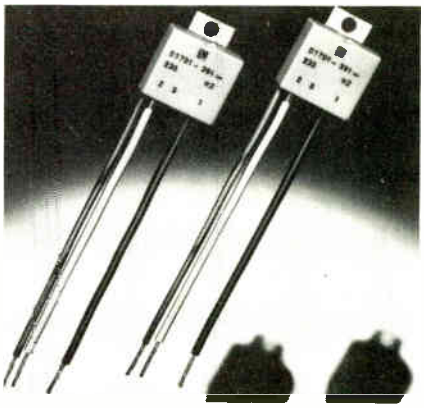


Universal relay UF3-N and corresponding socket Z345 are designed especially for harsh industrial applications. Reliability is enhanced by screw, rather than solder, terminals. The relay is available with contacts of different materials. Kuhnke GmbH, D-2427 Malente, West Germany [447]

The TH 8911 is a 6-in. cathode-ray tube for storage oscilloscopes with a 100-MHz bandwidth. It can write up to 10 m/μs on a dark screen and up to 20 to 30 m/μs on a luminous screen. Thomson-CSF, Division Tubes Electroniques, 38 rue Vauthier, 92100 Boulogne-Billancourt, France [442]



The model VM-161A is a digital radio-frequency voltmeter. A coaxial-cable input terminal for measuring between 20 Hz and 100 kHz and an rf detector probe for 10 kHz to 1,200 MHz are provided. Toa Electronics Ltd., 1-29-10 Takadano Baba, Shinjuku-ku, Tokyo 160, Japan [445]



Rotational-speed regulator B1791-391 uses thick-film technology and can handle a maximum of 8 A. Adjustment range is from 90 to 215 V at a 220-V input. Regulation is with an external potentiometer. Ero GmbH Ludmillastr. 23/25, D-8300 Landshut, West Germany [448]

SIEMENS

Cross over to auto insertion with DIP silicon bridges

Besides achieving good operating specs, component designers must create products with high implementation flexibility – small size, suitable for all layouts, cool operation, not to mention an attractive price. Now another requirement has joined this list: automatic insertion capability. Dual in-line packages have set the standard here, and new devices must follow this lead.

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Supply voltage range: 20–150 V_{RMS}
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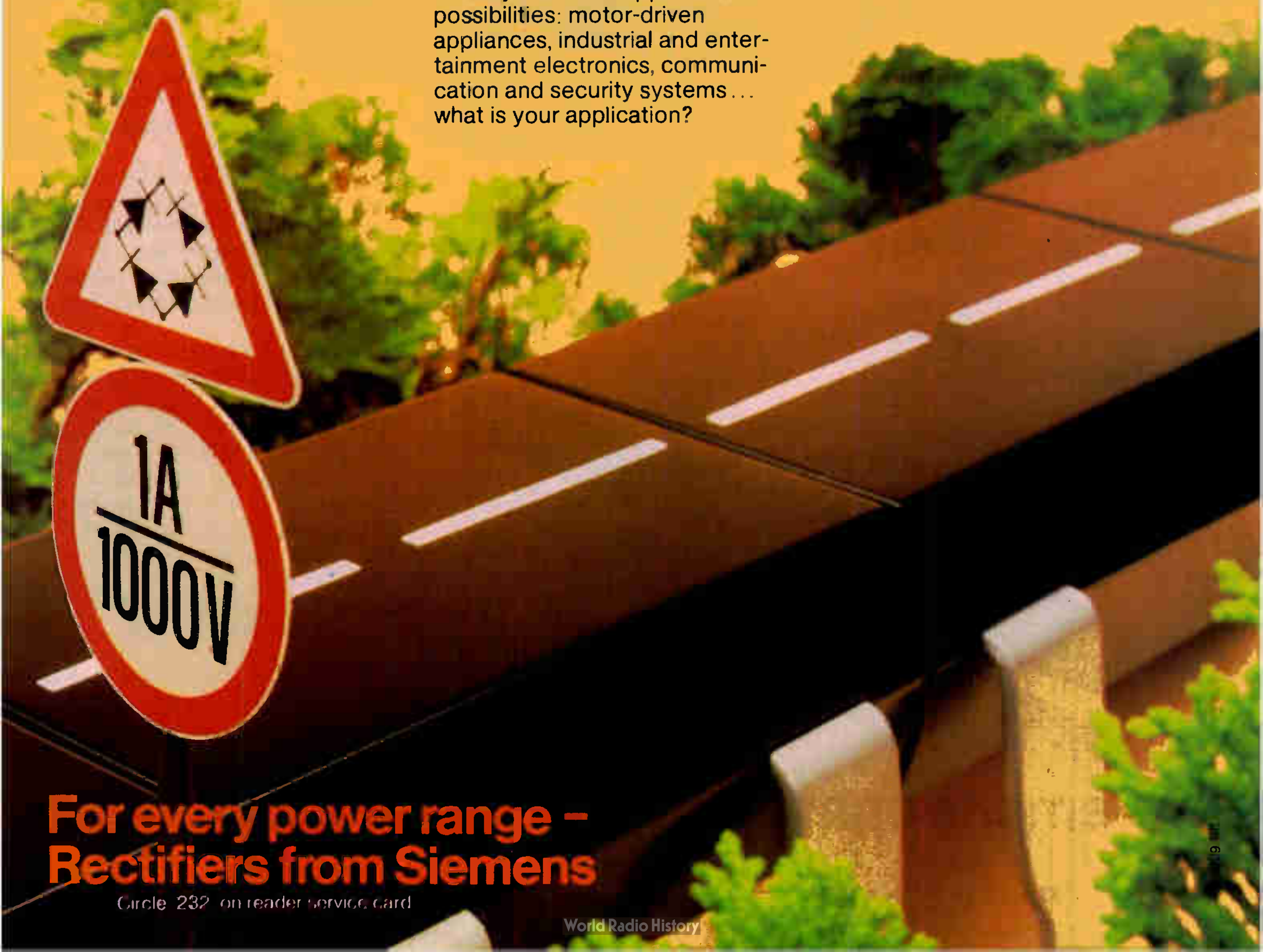

For every power range – Rectifiers from Siemens

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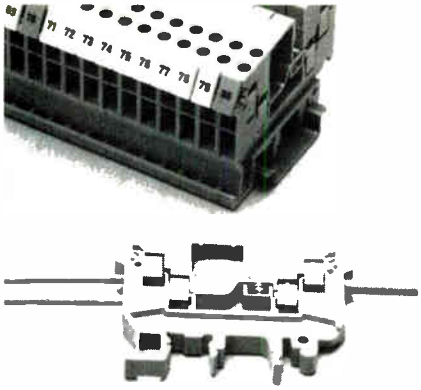
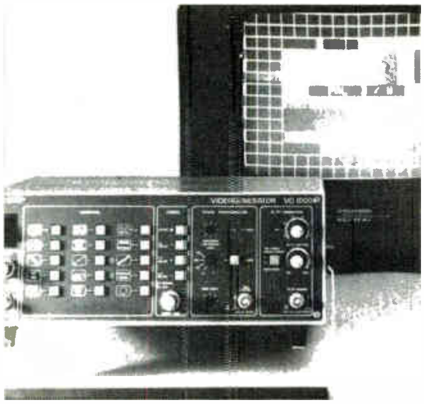
New products international

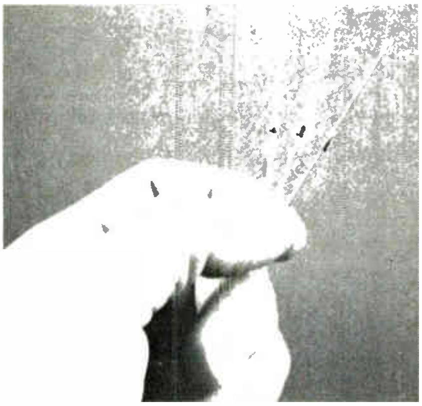


Universal double terminal UDK4, for side-by-side in-line mounting, accommodates two leads at each end instead of one. At each end, there are two independent screw terminals for wire cross sections of up to 4 mm^2. Phoenix GmbH, P. O. Box 149, D-4933 Blomberg, West Germany [449]

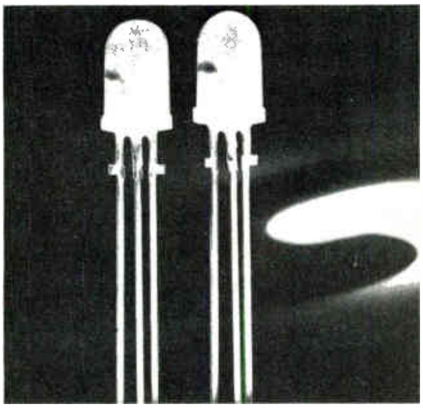


The VG 1000 video generator blends alphanumeric characters—a line of up to 15 characters—into the video test picture of a TV screen for adjusting transmission-link equipment and testing TV networks. Grundig AG, Kurfuerstenstr. 37, D-8510 Fürth, West Germany [452]

The 2017 programmable microprocessor-controlled precision signal generator has a frequency range of 10 kHz to 1,024 MHz. It features a slow-sweep facility for easy detection of spurious responses within the receiver. Marconi Instruments Ltd., Longacres, St. Albans, Herts. AL4 0JN, England [450]



The SD 102A, -B, and -C are silicon Schottky barrier diodes in a miniature glass package with reverse voltages of 50, 40, and 30 V, respectively. They have very short switching times and low forward voltages, typically 0.4 V at 10 mA. ITT Semiconductors, P. O. Box 840, D-7800 Freiburg, West Germany [453]

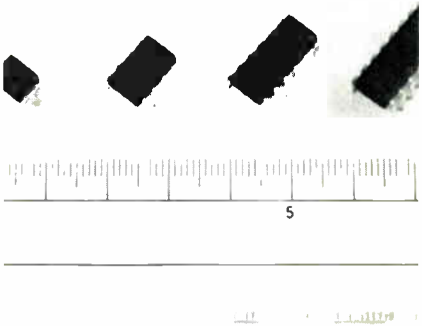


The V628P light-emitting diode produces a blinking orange-red light and a continuous green light. In an indicator system the green light can be used to show operational status and the blinking orange-red as a warning signal. AEG-Telefunken, Theodor-Stern-Kai 1, D-6000 Frankfurt 70, West Germany [451]

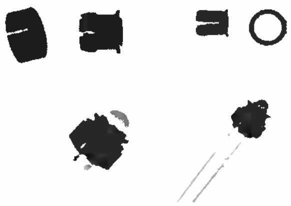
The Thermobox telemetry system comes in a package that protects the system for up to 40 hours against temperatures as high as 300°C, thus allowing it to transmit data from environments with such high temperatures. Johne & Reilhofer, Fraunhoferstr. 14, D-8033 Martinsried, West Germany [454]

New products international

The system 4400 compact controller for automatic control and data acquisition in testing and production applications, has a keyboard, control keys, and a 12-in. screen. NV Philips Gloeilampenfabrieken, Science and Industry Division, P. O. Box 523, 5600 AM Eindhoven, the Netherlands [455]

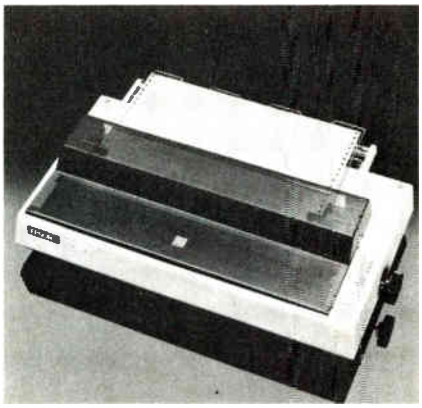


The PC-800 series photocoupler contains a gallium arsenide infrared light-emitting diode and a silicon phototransistor in standard single and double, triple, and fourfold coupled dual in-line packages designed to increase isolation. Sharp Corp., 22-22 Nagaike, Abeno-ku, Osaka 545, Japan [458]

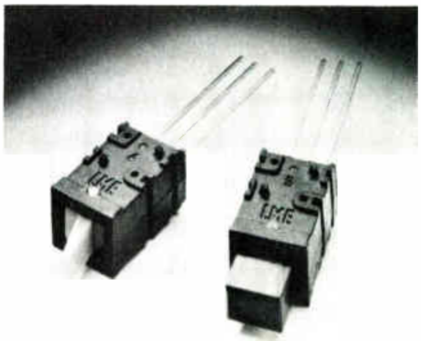


Fixing clips and rings have been designed to support light-emitting-diode lamps and to fit all types of electronic apparatus. They can be mounted easily and quickly and are available in several models. Special types can also be made. Universo SA, CH-2301 La Chaux-de-Fonds, Switzerland [456]

The series 56,000 coded rotary switches are designed for high-performance applications in harsh environments. They are totally sealed, resist contamination like sand and dust, and are built to withstand shock and vibration. Digitran UK, Melbourn, Royston, Herts. SG8 6AQ, England [459]



The MX-100 136 column dot-matrix printer prints bidirectionally at 80 characters/second. It has logical seeking, bit image and emphasized printing, and vertical and horizontal tab functions. Shinshu Seiki Co., Hirooka Division, 80 Hirooka, Shiojiri-shi, Nagano 399-07, Japan [457]



The RMF 351 proximity switch and the RMD 961 contactless pushbutton feature a Hall element for a nominal voltage of 5 to 12 V and a transistor outlet with an open collector. LM Ericsson Telemateriel AB, Components Department, P. O. Box 401, S-135 Tyresö, Sweden [460]

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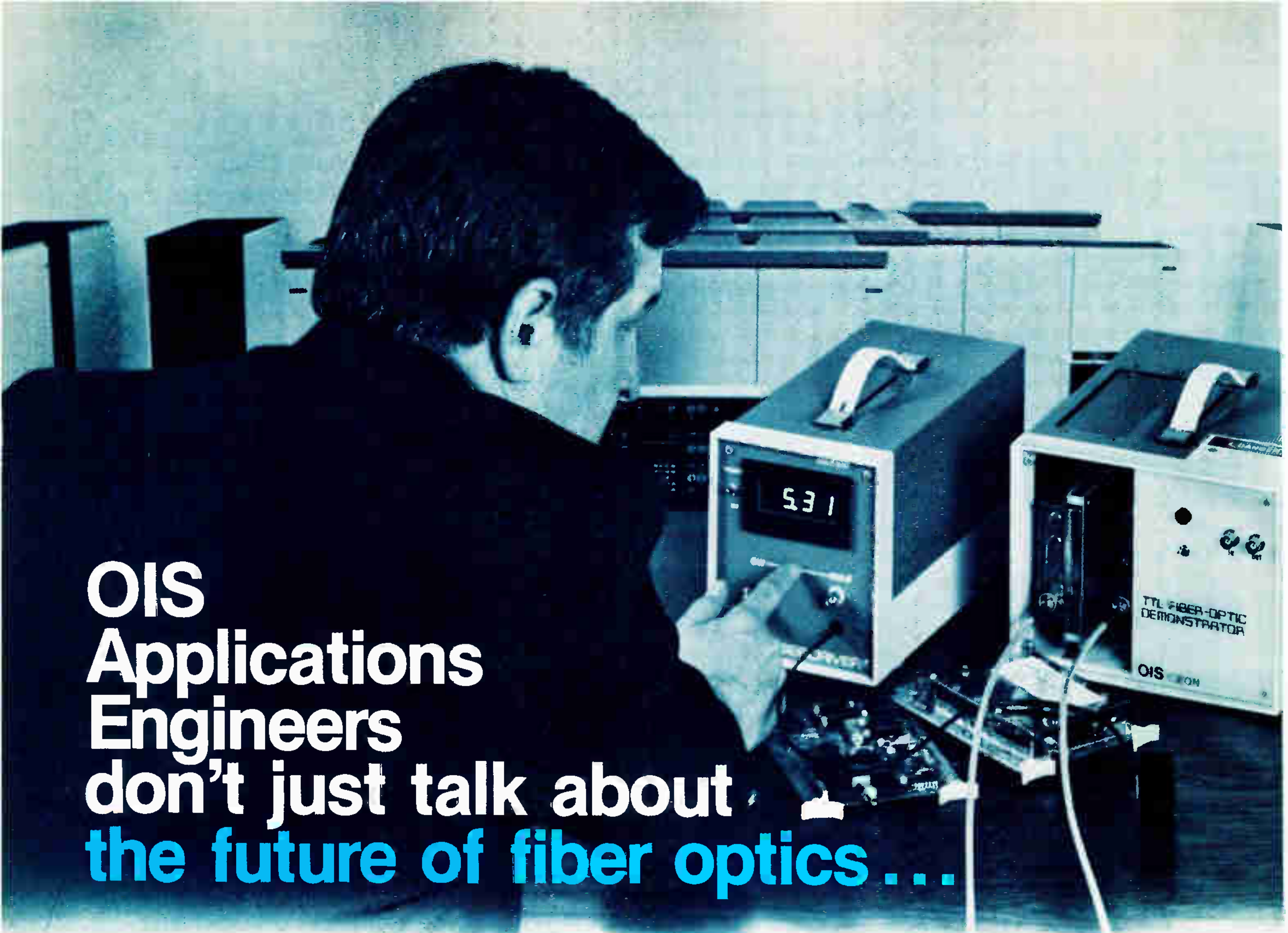

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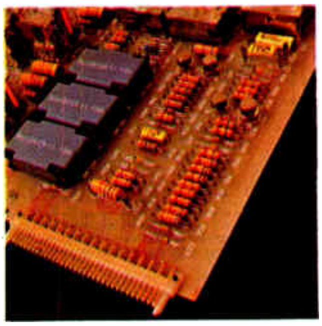

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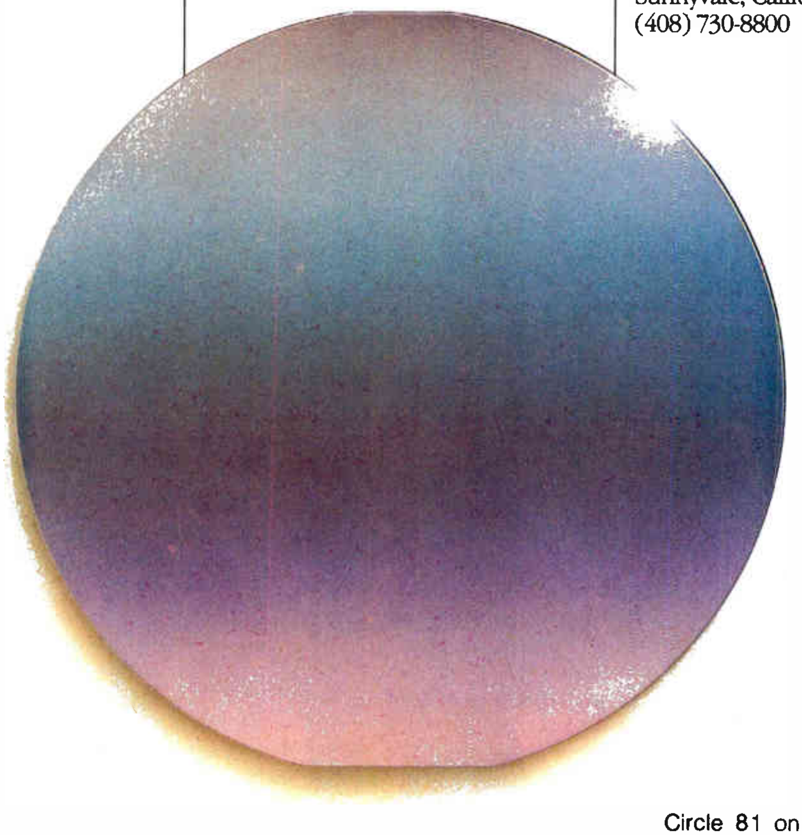

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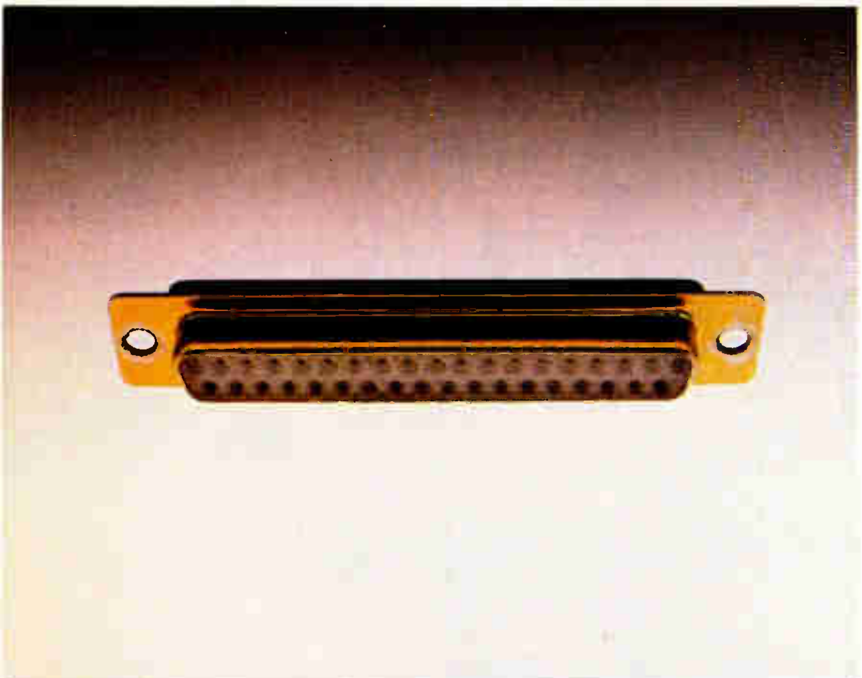

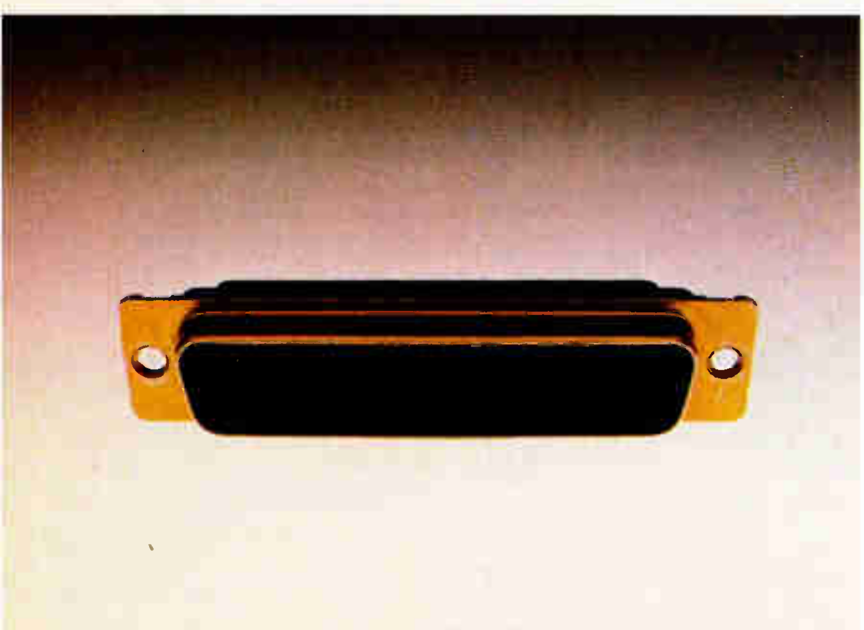

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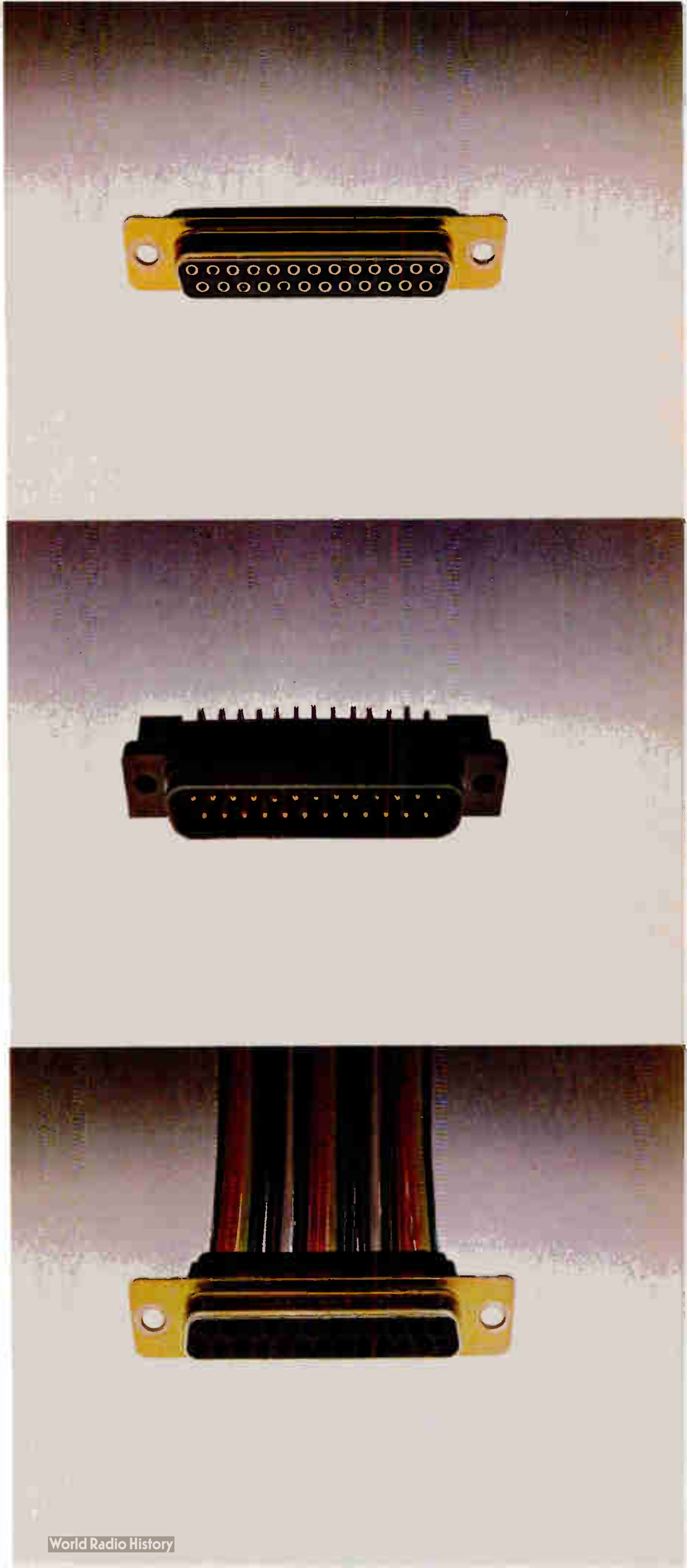

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BUILDING BETTER COMMUNICATIONS

Circle 88 on reader service card

U. S. IC gear makers build in Japan

Leading companies seek to maintain their market shares by establishing joint ventures and subsidiaries

by Robert Neff, Tokyo bureau

Even though they threaten to dominate worldwide semiconductor markets, Japanese manufacturers still count heavily on U. S. machinery for the most sophisticated steps in chipmaking—at least for now.

According to one study, U. S. suppliers will capture at least half the Japanese market this year for mask-making and wafer-masking gear and in such wafer-processing segments as ion implanters and sputtering equipment. However, the same study, by Kanematsu Semiconductor Corp. in Tokyo (see below and next page), shows that the U. S. share is steadily slipping. Other market reports also reflect this trend.

"U. S. semiconductor equipment companies are not doing well in Japan," says Sheldon Weinig, president of Materials Research Corp. of Orangeburg, N. Y., and former president of the Semiconductor Equipment Manufacturers Institute.

To counter this slippage, U. S. companies are aggressively bolstering their presence in Japan. Most companies have in the past relied on local trading firms to market and support their products. But now they are turning to wholly owned subsidiaries or to joint ventures to service, develop, and manufacture equipment in Japan. They see such steps as necessary to retain the confidence of local customers, who value intimate technical contacts with suppliers. Galvanizing this new push is the U. S. manufacturers' knowledge that Japan's semiconductor equipment and materials market is worth $636 million this year and growing annually by 20% to 30%. Examples of this trend include:

- Materials Research Corp.'s creation of a joint venture with its former representative, Midoriya Electric Co. of Tokyo, which holds a 20% share and supplied many of the new MRC Co.'s personnel.
- The establishment in March by Kulicke & Soffa Industries Inc. of Horsham, Pa., of a wholly owned subsidiary in Tokyo to service and sell its wire-bonding equipment. The company is a worldwide leader in that field but has barely penetrated the Japanese market.
- The construction this year by Toyo-Morton KK of a plant near Tokyo that will produce 5 million pounds per year of epoxy molding compound. Toyo Ink Manufacturing Co. of Tokyo and Morton Chemical Co. of Chicago now make adhesives in Japan and have been together for six years in a 50-50 joint venture. The $2 million plant is aimed at preventing Toyo-Morton's share of the Japanese encapsulation market from slipping below the current 7%, says a company spokesman.
- The announcement in June of plans by CTI-Cryogenics of Waltham, Mass., to launch a 50-50 joint venture later this year with Ulvac Corp. of Tokyo to make cryogenic pumps for the Japanese market. CTI also will continue selling its U. S.-made pumps, important components in such machines as sputterers, through trader C. Itoh and Co.
- The formation of a joint venture

TABLE 1: SHARES OF THE JAPANESE EQUIPMENT MARKET FOR THE INITIAL STAGES OF INTEGRATED CIRCUIT MANUFACTURING (%)

	Domestic			Imported		
Wafer making	1977	1979	1981	1977	1979	1981
Crystal pullers	70	80	90	30	20	10
Float zoners	100	100	100	–	–	–
Slicers	95	80	90	5	20	10
Polishers	70	80	90	30	20	10
Surface grinders	20	40	80	80	50	20
Edge grinders	30	70	100	70	30	–
Wafer masking						
Coaters and developers	10	40	50	85	60	50
Aligners	10	30	40	90	70	60
Plasma etchers	40	30	70	60	50	30
Wet chemical etchers	90	100	100	10	–	–
Wafer steppers	–	30	40	–	70	60
Wafer processing						
Epitaxial-growth systems	40	20	70	60	80	30
Diffusers	100	100	100	–	–	–
Ion implanters	–	10	40	100	90	60
Metal depositors	70	60	50	30	40	50
Chemical vapor depositors	60	60	80	40	40	20

SOURCE: KANEMATSU SEMICONDUCTOR CORP.

earlier this year by TRE Semiconductor Equipment Corp. of Beverly Hills, Calif., and Tokyo Electron Ltd., Japan's largest marketer of semiconductor manufacturing equipment. The partners expect to start making TRE's wafer stepper and microlithographic equipment in Japan by late this year.

■ The recent announcement of plans by Thermco Products Corp. of Anaheim, Calif., to build a plant in Japan to make oxidation, chemical-vapor-deposition (CVD), and diffusion reactors. TEL-Thermco Engineering Co., a joint venture with Tokyo Electron launched 11 years ago, is building diffusion furnaces at a plant in Yokohama.

■ The establishment in 1979 of Applied Materials Japan KK, a wholly owned subsidiary of Applied Materials Inc. of Santa Clara, Calif. AMJ is opening regional sales and service centers and is planning a $4 million design center.

Two of the largest U.S. suppliers—GCA Corp. and Perkin-Elmer Corp.—have established their successful businesses in Japan. But Varian Associates gave up on its joint venture with Nippon Electric Co.—Anelva Corp. of Tokyo—and is now selling its various product lines through Tokyo Electron.

Still, the need for proximity to customers has proved compelling for many. "We were frustrated with the trading firm's maintenance ability," says Tetsuo Iwasaki, director of marketing at Applied Materials Japan. He adds that Japanese customers are concerned about poor reliability from U.S. suppliers and want more automation and special options.

Open door. C. Scott Kulicke, president of Kulicke & Soffa, says that "in the past two to three years our machines have gotten so complicated that we felt we needed to control our service resources [in Japan] more closely." Kulicke also expresses the need to compete against its chief international rival—Shinkawa Ltd. of Tokyo—on Shinkawa's home turf. Most of the companies are finding that Japan is not nearly as closed to foreign business as some would have it. "We're moving at the pace we want and there have been no unexpected delays," says L. A. Cambey, senior vice president of Materials Research. "The prefectural governments have welcomed us."

Japanese experts do not necessarily agree, though, that Japan is as open as that to U.S. ventures. "There is no way for Kulicke & Soffa to sell here," says one trader. "We already have two fantastic local manufacturers of wire bonders—Shinkawa and Kaijo." In general, they see a rather bleak future for any foreign supplier not offering the most advanced equipment.

"The U.S. will continue to lose a market share here in test equipment and photolithography," says Minoru Yoshida, executive vice president of Tokyo Electron, which represents more than 10 U.S. suppliers in Japan. He views the Americans as most competitive in electron-beam lithography, 1:1 projection-mask aligners, 10:1 steppers, sputterers, CVD reactors, and ion implanters.

More sanguine about the Americans' chances is Toshiyuki Onoe, general manager of the Semiconductor Equipment division at Kokusai Electric Co., a major supplier. According to his statistics, U.S. producers have 30% of the Japanese market, down from 46% in 1973. But he thinks they can improve their sales here. He says he has felt little impact from AMJ.

Good times seen. The U.S. makers are nothing if not optimistic. AMJ, whose Japanese work force has expanded to 32 from an original 7 less than two years ago, plans to have 45 employees by October and 70 by the following October. Iwasaki is predicting sales from CVD and epitaxial reactors this year of $15 million, up from $7.5 million last year and $3.5 million in 1979. His goal is a 70% share of what is currently a $22 million epitaxial-reactor market, up from today's 40%. "There is a big potential in using single-crystal epitaxy for MOS and our reactor is the only one that can do that," he boasts.

Kulicke & Soffa, whose sales fell short of $1 million in Japan last year, is aiming for an eventual 20% to 25% share of what Kulicke estimates is now a $50 million annual market. That is a bold target indeed, even for a company that claims a 45% worldwide market share.

Weinig and Cambey of Materials Research are no less ambitious. Cambey expects within 18 months to raise MRC's claimed 20% share of the Japanese sputtering market to the same level as its worldwide share, which he says is significantly higher. Weinig ultimately expects 30% to 40% of his entire corporate sales to come from Japan, against 4% to 5% today. ☐

TABLE 2: SHARES OF THE JAPANESE EQUIPMENT MARKET FOR THE LATER STAGES OF MANUFACTURING (%)

	Domestic			Imported		
Mask making	1977	1979	1981	1977	1979	1981
Reduction camera	100	100	–	–	–	–
Step-and-repeat camera	–	–	–	100	100	–
Computer-aided design	–	–	–	100	100	100
Pattern generator	–	–	–	100	100	100
Electron-beam equipment	20	40	40	80	60	60
Contact printer	–	–	–	100	100	100
Assembly						
Dicer	90	95	95	10	5	5
Die attacher	80	90	95	20	10	5
Wire bonder	90	95	95	10	5	5
Molder and sealer	90	90	100	10	10	–
Testing						
Environmental	70	70	90	30	30	10
Probing and sorting	90	90	90	10	10	10
Electrical	30	60	40	70	40	30
Scanning electron microscope	95	95	5	5	5	–

SOURCE: KANEMATSU SEMICONDUCTOR CORP.

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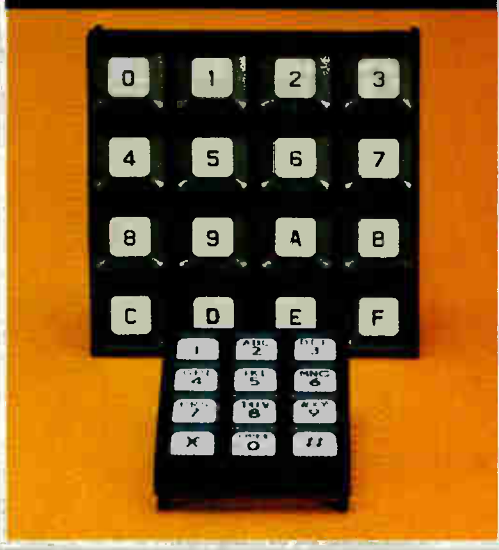

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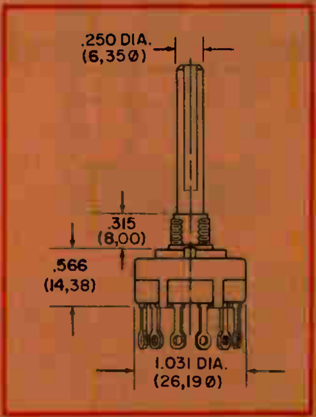

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The role of automation in future industrial scenarios extends well beyond the current use of computers as aids in design, adjuncts to bookkeepers, or process controllers. The integration of all such functions into a data-gathering, process-tracking, design-initiation, and updating system will be commonplace and more than necessary for a well-run and cost-effective manufacturing center.

One such system is already in place and operating at International Business Machines Corp. for the layout, implementation, and production of semiconductor devices, circuit modules, and boards. Encompassing 25 design locations and six manufacturing sites in the U.S., France, Germany, and Japan, the automated capabilities IBM has put in place start with front-end design and extend to subassembly production.

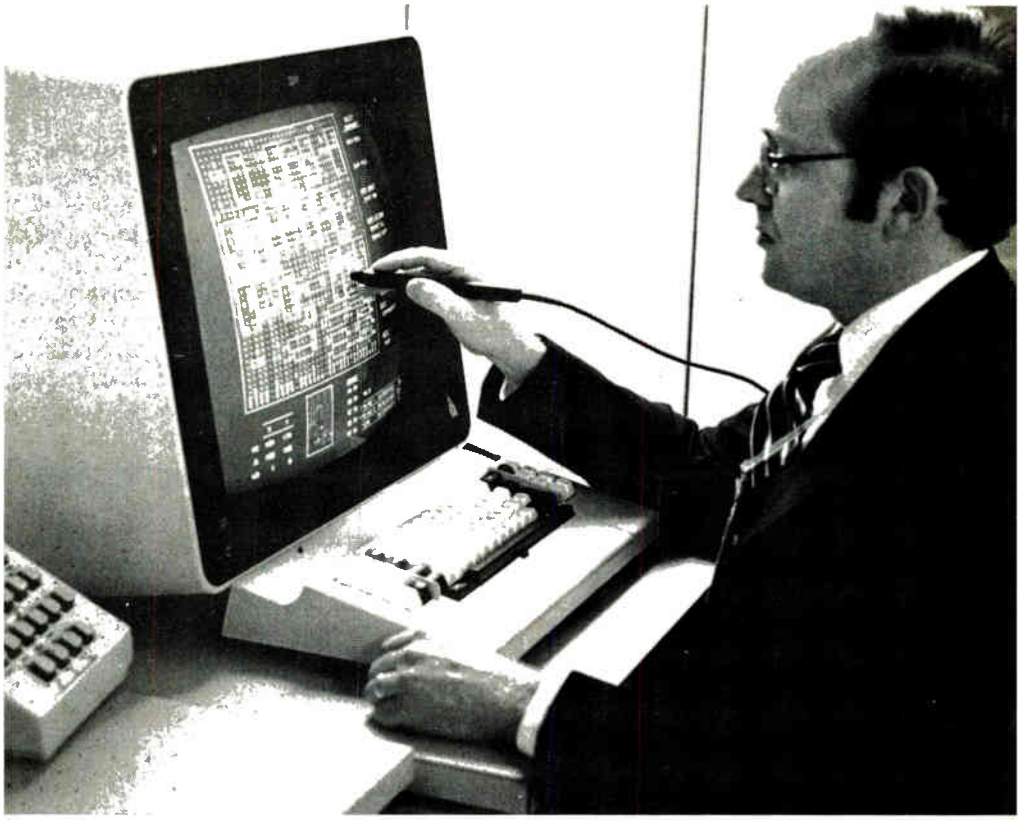
There are three main components in IBM's system—its automated design capabilities, the link between the design engineers and those in manufacturing, and the production line itself.

The engineering design system is situated in East Fishkill, N.Y., and serves as one common system for all the electronic design tools needed throughout the company—be it in Endicott, N.Y., or Böblingen, West Germany. "The system handles all the electronic design, as opposed to mechanical design. We do everything from the silicon to the printed-circuit cards, to modules, boards, and back panels. The system also generates design-verification rules and test patterns," explains Frank J. Worthmann, manager of physical design.

At East Fishkill, there are 25 System 370/168 computers to control the massive system. IBM has been able to automate much of this process because of a decision to incorporate the master-slice approach, which allows manufacturers to maintain a wafer inventory with some design already in place.

Design responsibility. "The designer invents the register-to-register logic, but we establish the methodology," says Worthmann. Included under that responsibility are establishing the parameters for the logic design, plus all the checks and ground rules that are found in the design library. The creation of automated logic diagrams and the verification of logic design through software simulation programs that model all functions are part of the design system as well. From these logic designs a physical design is also generated by the system.

The system works not only for device layout, but also in module and board layout. "So far we've brute-forced our way through with the algorithms in place. We've been able to extend the algorithms up to the



Plugged in. Designer in East Fishkill, N.Y., lays out printed-circuit board with the aid of a terminal in IBM Corp.'s engineering design system that also serves sites in Europe and Japan.

5,000-circuit range," notes Worthmann. The thermal-conduction module sports 120 input/output pins per chip, with each module containing 118 chips, for more than 1,800 connectors. These modules sit on boards with 28 to 32 layers—16 of which are wiring layers and the others for power distribution. All three of these different design levels were generated for the 3081 using the engineering design system, notes Worthmann.

The system generates all the data necessary for manufacturing in what is termed a release interface tape. Although a physical tape is no longer used, the terminology is left over from the first version of the system. Contained in this output data are packaging information, logic diagrams, component mix, placement coordinates, wire sizes and routing, test patterns, and all checking and completion codes.

The "tape" for a 700-circuit chip contains over 2.5 million characters (bytes) of information. One for a 100-chip module contains up to 100 million bytes.

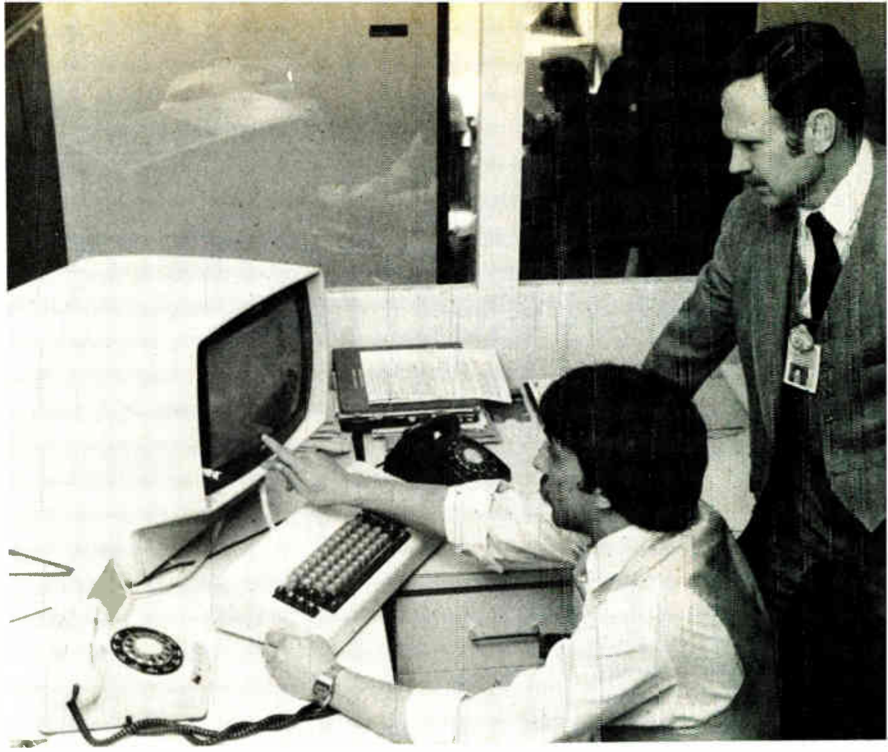
Universal data. It is important to note, says Worthmann, that this design data is not generated for particular production tools, but must be converted into numerical-control data. This allows IBM to use a variety of equipment to produce the devices and does not lock the company into one particular process or manufacturing strategy.

Each manufacturing site has a release facility that acts as an interface between manufacturing and design, checking the design as it comes in and auditing it to ensure that the device or subassembly can be manufactured as designed. This facility does validation checks on the design, technology parameters, and graphics generation. Its final output is numerical control data to run production machines.

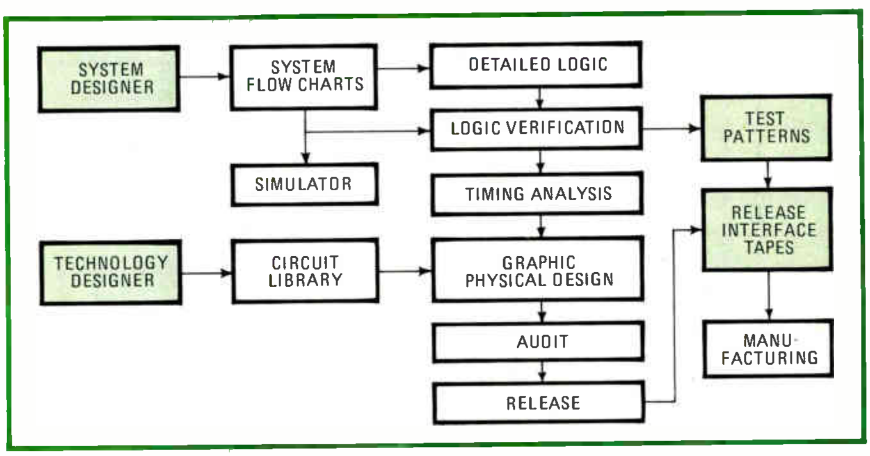
"The engineering design system is releasing personality information only on the devices," notes James L. Gallo, system development engineer at East Fishkill. "What we in the product direct release department provide is a logic- or machine-oriented design. We can respond to a variety of technologies, and thus minimize the time required to introduce a new technology."

Design check. When a release interface tape is received by the product release facility, an immediate audit of the design is done, using the same information from the design library as the designer used. Thus, updated information from Worthmann's group must be available to both designers and manufacturers. If there are any faults uncovered at that time, the design is immediately returned to the design location. The East Fishkill product release facility handles between 1,800 and 2,000 device and subassembly designs each year, says Gallo. A typical design can be audited and preliminary numerical control data issued within five to ten minutes.

At East Fishkill there are two production lines in place. They are known as the QTAT (for quick turnaround time) line and business-as-usual line. The QTAT line [*Electronics*, Jan. 27, p. 121] handles about 10% of East Fishkill's production per year and is primarily aimed at limited production runs, notes Don Mozer, senior engineering manager. Both lines share the same electron-beam facilities—at present three machines and soon to be four—all designed by IBM. □



Looking in. Engineers at IBM's East Fishkill, N. Y., facility observe part numbers for the release interface tapes that have been automatically started through the system.



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Production

Lasers automate pc-board inspection

Systems aim to eliminate field failure of boards that have passed makers' tests and inspections

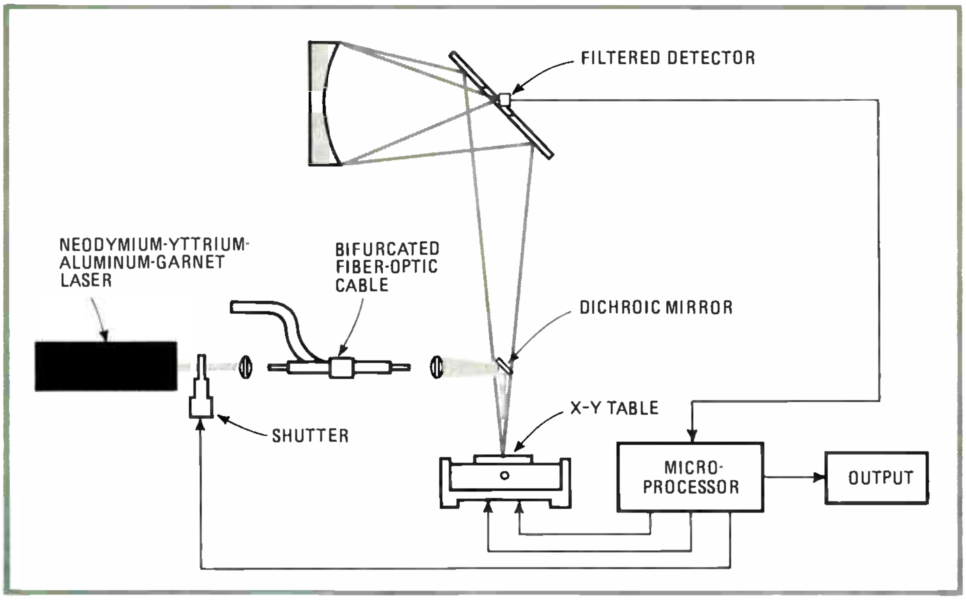
by Linda Lowe, Boston bureau

Perhaps the last holdout against automation in printed-circuit–board manufacturing, the board inspection process is a new target for the laser's beam. One laser-based inspection system that is already commercially available, as well as several others getting ready for market, may soon replace the human eye in detecting flaws on the millions of square feet of pc boards produced each year.

As many as 10% to 15% of these boards will fail in the field, even after going through a manufacturer's test and inspection lines, estimates Philip Geise, an electro-optical engineer at Chrysler Corp.'s Huntsville, Ala., Electronics division. Geise is a codeveloper of Chrysler's laser-scanning inspection system, introduced last fall [*Electronics*, Oct. 9, 1980, p. 44]. Another system developer, Altman Associates Inc. in Stamford, Conn., is readying its own product introduction. Systems at the Advanced Controls Products division of Cooper Industries Inc. in Irvine, Calif., and Vanzetti Infrared & Computer Systems Inc. of Canton, Mass., are still under development.

Very complex boards, in whose manufacture more automated inspection could become a critical need, will also be the fastest-growing segment of the multilayer board market for military and computer applications, notes Philip J. Lapin, an analyst at Gnostic Concepts Inc. The Menlo Park, Calif., research firm projects that this will hold true in sales of multilayer boards overall, where boards having 10 or more layers will demonstrate an average annual growth rate of 25.6%, accounting for over $176 million of total multilayer board sales of $1.976 billion in 1985.

Both Chrysler and Vanzetti Infrared have had military funding in support of their development efforts. Indeed, the very complex, many-layered boards used by the military account for one of the strongest potential markets for laser-based inspection systems, maintains Gunther Rudenberg, microelectronics consultant at Arthur D. Little Inc. in Cambridge, Mass. "At that level of complexity, board faults found late in the production process can be disastrously expensive," he notes, so automated systems capable of finer and more reliable board inspection than people can provide should find an eager customer base. Rudenberg also cites computer manufacturers as a prime market, one that will demand high throughput and maximum reliability.



Heat gage. Developmental laser system from Vanzetti Infrared and Computer Systems Inc. measures thermal responses of solder joints on a pc board to uncover faults invisible to the human eye.

The Chrysler model LIS-510 inspection system, which focuses its low-power scanning laser beams both on bare and stuffed boards, is better than 99% effective at catching board faults on the Chrysler production line, its developers report. The system, which recently became available at a price of $80,000 to $100,000, can inspect a 400-lead board for component presence and proper lead dress in less than 5 seconds, or scan a bare board for improperly sized or placed component holes at a minimum of 50 holes per second, calculates Chrysler's Geise. By contrast, a human inspector takes about 1 second to

ICECAP Report T.M.

By Mel H. Eklund

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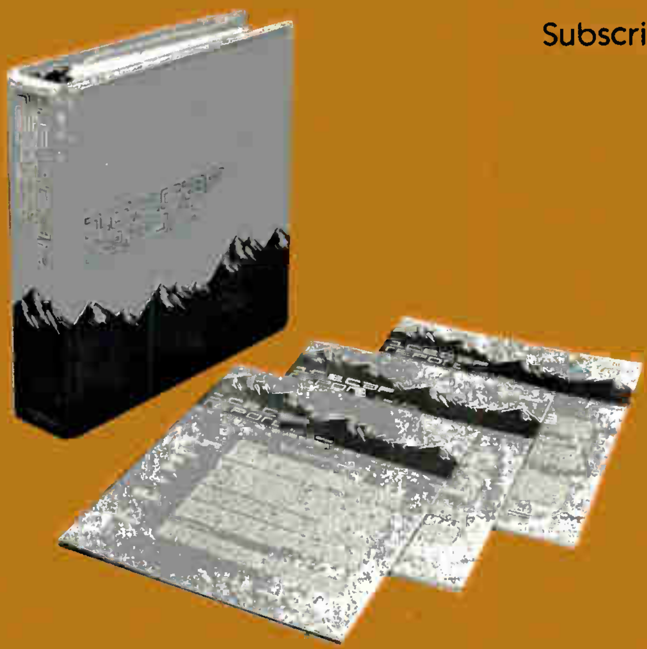

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examine a single lead, he adds. The LIS-510 works by collecting laser beams reflected off a pc board, and comparing them using a minicomputer with stored board patterns.

Comparison beam. Altman Associates, whose board verifier system is slated for commercial delivery by the end of this year, is claiming an inspection rate of up to 50 square feet of bare board per minute and measurement accuracies of within 0.001 inch and better. The system also analyzes reflected laser beams from a board to check hole sizes and positions. Unlike the Chrysler system, however, it dispenses with a master pattern stored in memory. Instead, a second beam from the system's laser scans artwork that describes a board's nominal dimensions, and a minicomputer factors in manufacturing biases and allowed tolerances and decides whether board features come within allowed limits. This allows the inspection of different board types without reprogramming the system, points out company president Norman G. Altman. He estimates the system will range in price from $100,000 to $150,000.

Advanced Controls says its Inspectron system will take about a minute to inspect an 8-by-10-in. bare pc board for line widths and spacing, line breaks, excess copper, and voids. The system also detects incomplete pads, poor pad-lead connections, and shorts in ground planes. Though it, too, uses reflected laser beams in analyzing board features, the Inspectron's only reference is a set of design rules programmed into its minicomputer. The company says violations of these rules account for nearly all rejectable board defects; when the system detects a violation, it will either print out the error's coordinates or stop scanning while an operator examines the flagged error.

By using general design principles rather than specific stored master pattern or artwork references, the Inspectron eliminates the need for tight alignment of board features to match corresponding reference points during a scan, say the sys-

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Contents

1. Lithography and Processing for Integrated Circuits.
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tem's developers. Scanning can begin and end anywhere on the board, and no special placement or alignment equipment is required.

Joint sleuth. Still in the development stage, Vanzetti Infrared's may well be the most sophisticated of the laser systems, although it confines its inspection to solder-joint quality on finished pc boards. Still, points out company president Riccardo Vanzetti, it not only identifies poor solder connections, which can make a board failure and being thrown out unnecessarily.
reduces the possibility of good components getting the blame for a board failure and being thrown out.

Unlike the other laser-based techniques, Vanzetti's incorporates an infrared detector, and finds defects by analyzing variations in thermal characteristics [*Electronics*, May 19, 1981, p. 34]. Thus it can pinpoint faults that are invisible even to the keenest human inspector. The system's laser delivers low-power pulses to each joint, heating it a few degrees above room temperature; a minicomputer compares the joint's thermal response against a stored pattern of normal responses to make a pass-fail decision. Joints with insufficient solder or subsurface air bubbles, for instance, warm up faster and reach higher peak temperatures than do good joints.

Weak points. The system aims at complementing electrical testing of pc boards on their way into the field, says Vanzetti. "Though electrical tests verify a board is intact at the time of the test, it cannot predict a board's fitness for actual use, where the board may be exposed to a lot of handling, thermal cycling, vibration, and the like." His system should prove a means of identifying solder joint weaknesses that make a board prone to failure in systems use where it is expensive to correct, Vanzetti asserts.

The Vanzetti system's developers say it can inspect at a rate of 10 joints per second. Not scheduled for commercial availability until 1982, it will cost an estimated $80,000 to $90,000 without a minicomputer, says Vanzetti. □

Computers

Japanese slow to gain in computers

New study shows U. S. firms dominate worldwide and predicts only an 8.3% share for the Japanese by 1985

by Gerald M. Walker, Business Trends Editor

Though the Japanese are making a dent in the worldwide computer marketplace, a report just published by Martin Simpson & Co. of New York shows that they are far from being a dominating force. By 1985, says the report, Japanese manufacturers will have an estimated 8.3% of the market.

This share gives the six leading Japanese firms approximately a $10.8 billion slice of overall computer revenues totaling $130 billion, the report reveals. In addition, a comparison of revenues of the three top Japanese computer firms—Fujitsu Ltd., Hitachi Ltd., and Nippon Electric Co.—with those of other major vendors also indicates that U. S. firms will continue to be out in front in 1985.

Interestingly, the Simpson study shows that Digital Equipment Corp. of Maynard, Mass., will become the second largest revenue maker behind IBM Corp., passing Control Data Corp. and NCR Corp. Fujitsu, meanwhile, is predicted to show modest growth rates, hitting $2.5 billion compared with DEC's $7.6 billion in 1985. NEC could fare better in the world arena, logging growth rates of almost 20% to reach $2.6 billion in 1985.

"The significance of the study," comments the research company's president, Martin Simpson, "is that it shows the Japanese are not invincible. They have excellent technology, good pricing, and can produce in high volumes, but they are not strong in software or service. The report shows that a company like DEC, which invests heavily in research and development, is able not only to survive against the Japanese but to beat them."

The 142-page report, called "The Japanese Challenge in the Computer, Copier, and Electronics Industries," highlights through 105 tables the niches the Japanese are carving from markets in personal computers to plain paper copiers to intelligent robots. It analyzes both domestic markets—where the products later introduced into outside competition are nurtured in a protective environment—and world markets. Profiles of individual companies such as Fujitsu in computers, Ricoh in office equipment, and Kawasaki Heavy Industries in robots also provide clues to market strategies.

Taking it personally. The domestic personal computer market, for ex-

ESTIMATED WORLDWIDE REVENUES OF MAJOR COMPUTER VENDORS
(in millions of dollars)

	1980	1981	1982	1983	1984	1985	Growth rates (%) 1981/1980	Growth rates (%) 1985/1980
IBM	21,367	24,000	27,600	31,500	35,200	41,000	12.3	13.9
Honeywell	1,634	1,850	2,100	2,400	2,700	3,000	13.2	12.9
CII-Honeywell Bull	1,486	1,800	2,000	2,300	2,600	3,000	21.1	15.0
NCR	2,971	3,300	3,600	3,900	4,300	4,800	11.1	10.0
Control Data	2,791	3,200	3,700	4,300	5,000	5,700	14.7	15.4
Digital Equipment	2,744	3,500	4,300	5,300	6,400	7,600	27.6	23.0
Sperry Univac	2,610	3,000	3,500	3,900	4,400	4,900	14.9	13.4
Burroughs	2,478	2,600	2,900	3,200	3,500	3,900	4.9	9.5
ICL	1,665	1,800	1,900	2,100	2,300	2,600	8.1	9.4
Hewlett-Packard	1,546	2,100	2,800	3,600	4,500	5,500	35.8	29.0
Fujitsu	1,446	1,600	1,800	2,000	2,200	2,500	10.7	11.5
Olivetti	1,380	1,600	1,800	2,100	2,400	2,800	16.4	15.1
Hitachi	1,106	1,200	1,300	1,500	1,700	1,900	8.5	11.4
Nippon Electric	1,084	1,300	1,500	1,800	2,200	2,600	19.9	19.1
Nixdorf	857	1,000	1,200	1,500	1,800	2,100	16.7	19.7
Other	15,600	18,700	22,000	25,600	28,800	36,100	19.9	18.3
Total	**62,765**	**72,550**	**84,000**	**97,000**	**110,000**	**130,000**	**15.6**	**15.7**

SOURCE: MARTIN SIMPSON & CO.

ample, may show portents of things to come. Though U. S. vendors such as Apple, Tandy/Radio Shack, and Commodore had dominated the Japanese market, this situation has been reversed within the past several months as Japanese manufacturers ranging from giants such as NEC to small, privately owned ventures such as Sord Computer Systems, AI Electronics, and Logic Systems International have entered the competition during the last two years.

The Japanese personal computer market is expected to reach $300 million in 1981, up 50% over 1980, Simpson estimates. This market should be worth $675 million in 1983. Although the Japanese hold the edge on hardware production, U. S. companies are still way ahead on software.

The report, the result of two months of research and over 10 years of building contacts in Japan, pinpoints several major targets for research and development identified by the Japanese computer industry. These include work on new devices such as Josephson junctions and chemical-compound semiconductors; concentration on non–Von Neumann architecture, data-flow machines, and data-base processors; effort on special-function distribution systems; and the design of processors with automatic synthesis or module elements including optimized burden sharing for hardware, software, and firmware.

Artificial intelligence. The Japanese are also going after practical applications of artificial intelligence, including pattern and speech recognition. They have mounted a vigorous software-development program to close that gap. And there is a heavy emphasis on intelligent robots.

The Simpson report sees a clear Japanese edge in robots. The worldwide market for industrial robotics reached approximately $325 million in 1980, up nearly 50% from 1979's sales of $220 million. By 1985, this market, which includes fixed-sequence, variable-sequence, numerically controlled, and intelligent robots, is expected to increase by more than 250% to $1.2 billion. □

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Scanning electron beam probes VLSI chips

Noncontacting test method plots logic-state maps of the actual operation of complex parts like microprocessors

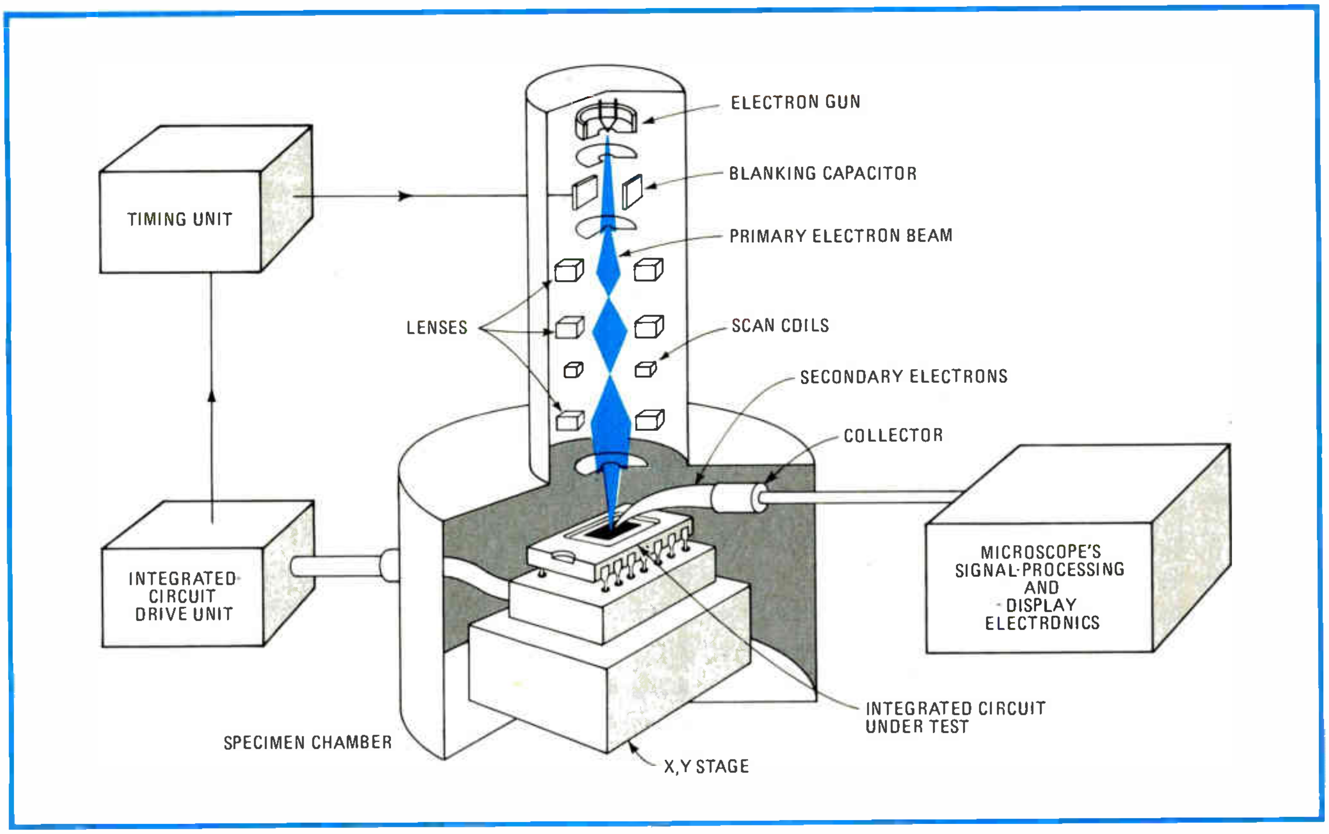
by Peter Fazekas, Hans-Peter Feuerbaum, and Eckhard Wolfgang, *Siemens Research Laboratory, Munich, West Germany*

☐ Functional analysis of very large-scale integrated circuits is beginning to take a new form: a focused electron beam scanning the entire surface of the chip makes noncontacting, nonloading measurements and maps the IC's logic functions. The scanning electron beam implements the established voltage-contrast technique—relying on areas of lightness and darkness in the resulting chip image to represent logic voltage levels—but new test techniques turn the formerly static technique into a dynamic measurement process.

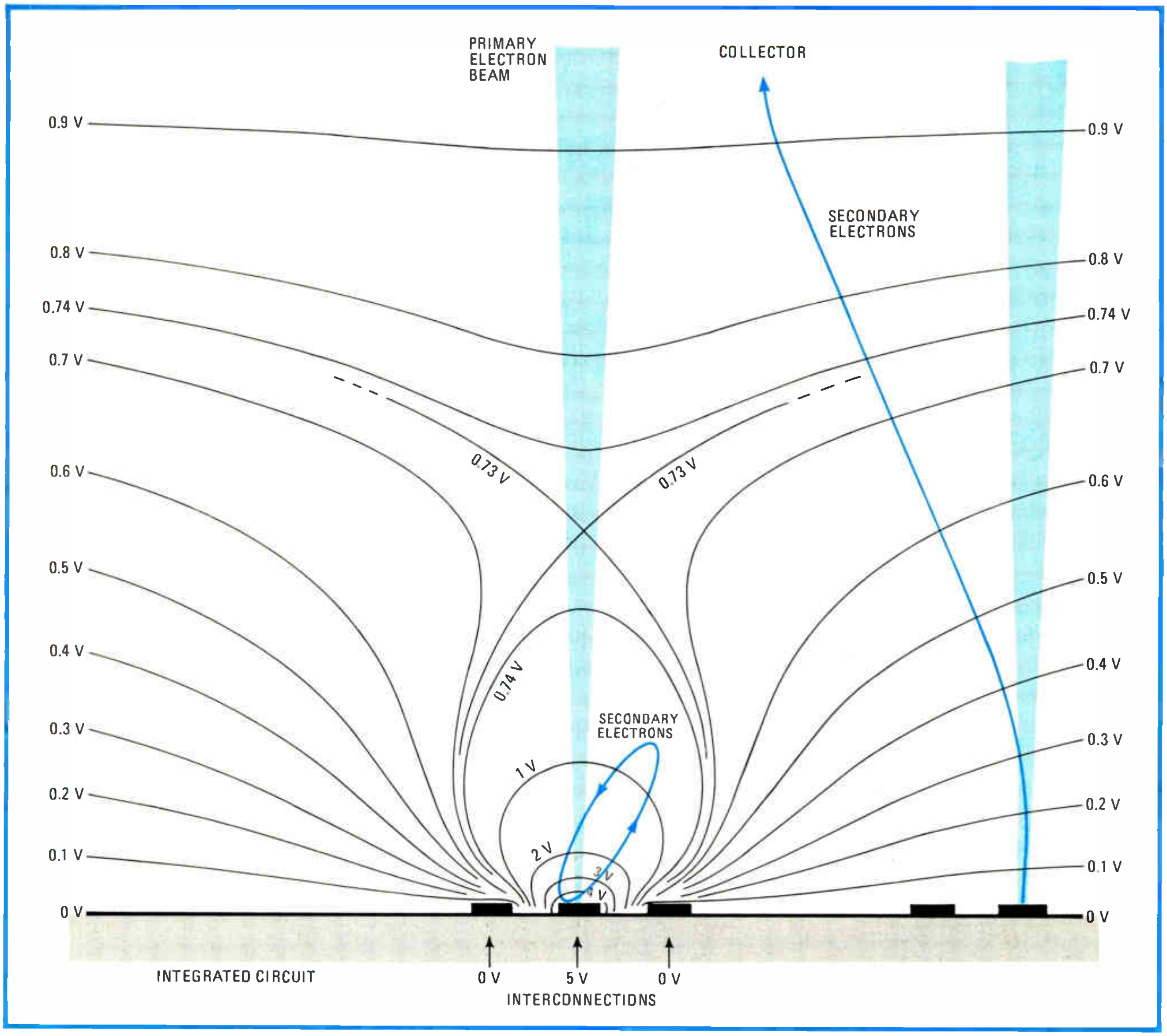
By coordinating the beam's scan rate with the clock signals in an energized device under test, it is possible to display the signals in the form of logic state maps superimposed on the IC image. Thereby a comprehensive analysis of an IC can be made as never before. The test setup adds a logic analyzer to the sampling electron microscope, itself a special version of a scanning electron microscope. Thus digital signals can be measured—but analog waveforms also can be checked, and the test techniques can be applied to all types of ICs.

Why now?

The VLSI era is bringing new importance to electron-beam probing. Some present-day VLSI circuits typically cram half a million transistors—with pattern details of 1.5 to 2 micrometers—into an area of less than 100



1. Electron-beam probing. A packaged IC without a lid is put in a sampling electron microscope's specimen chamber. A pulsed beam of electrons is focused on a point on the IC, and the resulting secondary electrons are collected and displayed on a CRT or logic analyzer.



2. Voltage contrast. Secondary electrons emitted at the 5-V interconnections are repelled by local electric fields, while those from a ground path are accelerated to the collector. Hence, positive interconnections show up as dark in the resulting image, and negative ones as light.

square millimeters. Despite computer-aided-design techniques and the test aids being applied to VLSI, it can happen that prototypes of such circuits do not perform as planned. The built-in test features on many new circuits, increase testability, but to spot design weaknesses, it is still necessary to probe individual IC nodes internally. And only the electron-beam probe can handle the complexity of these VLSI circuits.

As long as the IC has existed, designers have had two alternatives for internal probing: mechanical and electron-beam. Now the advantages of electron probing are becoming an absolute necessity in IC testing. Among these benefits are:

■ Loadless probing—by choosing the appropriate primary electron energy (2 to 3 kiloelectronvolts), it is possible to achieve a charge balance, which means that when one electron strikes the IC, another leaves it again. And thus, no electron current is induced by the electron probe.

■ Nondestructive probing—the low electron energy and the relatively weak currents (10 nanoamperes) do not cause electron radiation damage. Since no probe touches the die, there is no chance of mechanical damage.

■ Easy positioning—the electron beam can be positioned very quickly and very precisely at every point of the IC.

■ Parallel display of electrical signals—by scanning large areas of the circuit rapidly, it is possible to display their electrical functions simultaneously on a logic analyzer or similar piece of equipment.

■ Savings in chip real estate—the electron-beam probe can be positioned on narrow interconnections and is not restricted to special test pads.

■ Obtaining of information from oxide-coated areas—access is possible either through capacitive coupling to the oxide surface or through the formation of a conductive channel between the node and the oxide surface. (For the latter procedure higher-energy electrons are required, which may cause radiation damage.)

There are, however, some disadvantages of the electron-beam probe. They are:

- The need for a repetitive signal—because of the limited bandwidth and the unfavorable signal-to-noise ratio of the secondary electrons, stroboscopic or sampling techniques have to be applied, which make it impossible to measure nonrecurring, quickly executed processes.
- Measurement of ac signals only.
- No commercial availability—the setup for the electron-beam probe is considerably more sophisticated and more expensive than a mechanical probe because it has to be specially developed in the laboratories.
- No possible impressing of voltages or clock signals on the circuit—in contrast to the mechanical probe, the electron probe can be used only for measuring.

Sampling a microscope

In electron-beam probing, an IC is mounted in the evacuated specimen chamber of a scanning electron microscope and excited by a drive unit (Fig. 1). To make a measurement, the primary electron beam generated in the electron gun is focused on the surface of the IC by a lens system.

Scan coils position the electron beam on each measurement point. The low-energy secondary electrons released there hit a collector to which a high positive voltage is applied. The resulting amplified signal is then displayed on a cathode-ray tube. For high-frequency measurements (above 100 kilohertz), the electron optical column is equipped with a blanking capacitor driven by a timing unit synchronized with the IC's clock signal.

Building equipment

Sampling electron microscopes are assembled in laboratories by modifying scanning electron microscopes. The special features, shown in Fig. 1, are: a blanking capacitor, timing unit, IC drive unit, and signal processing and display. Not included is the secondary-electron spectrometer necessary for waveform measurement.

E-beam probing on the rise

Siemens is not alone in its interest in electron-beam probing. Work along these lines is proceeding at many large electronics firms. Additionally, the first piece of commercial equipment for converting a scanning electron microscope into a sampled electron-beam prober has just recently been put on the market by Lintech Instruments Ltd. of Cambridge, England [*Electronics*, June 30, 1981, p. 73]. Perkin-Elmer ETEC Inc., Hayward, Calif., is also developing a complete SEM-based contactless prober for the commercial market.

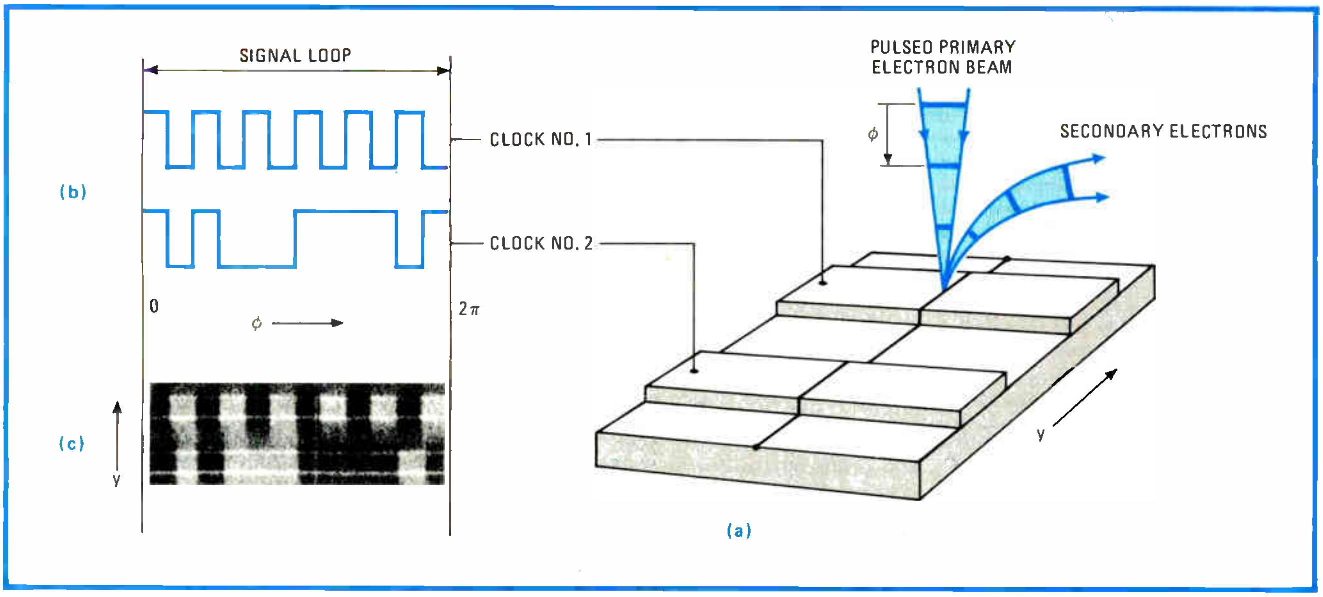
The importance with which the new technique is viewed is evident from the many published technical papers and by a recent VHSIC award to Hughes Research Laboratories in Malibu, Calif. For example, at the 16th Symposium on Electron, Ion and Photon Beam Technology held in May 1981 in Dallas, papers on the subject were given by the Massachusetts Institute of Technology's Lincoln Laboratory, IBM Corp.'s Thomas J. Watson Research Center, and Hitachi Ltd.

Finally, Hughes has been given a Phase III contract under the Department of Defense's Very High-Speed Integrated Circuits program to develop a laboratory scanning-electron-microscope voltage-probing system capable of making measurements on the nodes of VHSIC-type microcircuits. **—Jerry Lyman**

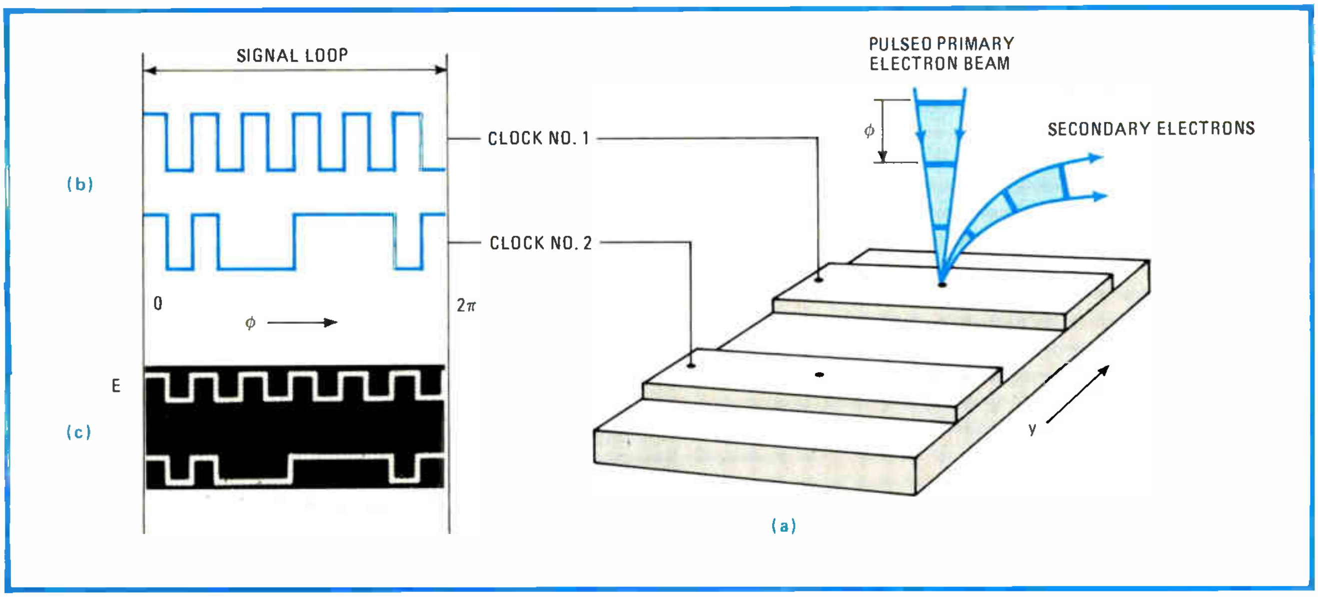
A touchy point in electron-beam probing is the effects such as reflections, cross talk, and stray capacitance caused by long leads. To overcome this, Siemens has implemented two solutions: a specimen chamber with a large area and a minichamber.

The bigger specimen chamber is 33 centimeters in diameter, large enough to accommodate a wafer prober to test either chips on 3-inch wafers or a packaged IC with 64 external pins plus accompanying drivers, which drive the signals on the more-than-1-meter-long leads.

The minichamber reduces the length of the leads into



3. Logically mapped. In logic-state mapping, the primary electron beam scans a line (a). After each scan, the phase is shifted. The clock signals are shown in (b). A logic state mapping of the loop is shown in (c), where dark bars are logic 1s and light bars are logic 0s.



4. Timing diagram. In the course of generating a logic-state timing diagram, the electron beam jumps from interconnection to interconnection (a). Applied clock signals are displayed at left in (b), and (c) represents scanned data as it is displayed on a logic analyzer.

the vacuum to a matter of just a few millimeters: the door of the specimen chamber contains a socket as a vacuum feedthrough. On the vacuum side is the packaged IC; on the air side are the external pins. To make the latter easily accessible, the electron optical column was rotated by 180° so that the beam is made to strike the IC from below.

Because of the demand for nonpassivated chips in open packages or nonpassivated wafers, electron-beam probing is not suitable for mass inspection during production. It is more suitable for failure analysis after stress treatment—burn-in for example—and for investigating field failures, but it is best suited for design verification. It is here that, because of its extraordinary performance characteristics, it will acquire a permanent place in circuit development laboratories.

Voltage contrast

Electron-beam probing depends on the phenomenon known as voltage contrast, which capitalizes on the fact that the maximum of the energy distribution of secondary electrons occurs at a few electronvolts, making the electrons highly sensitive to electrostatic fields.

Because of the high collector voltage (300 volts) in the setup of Fig. 1, almost all secondary electrons released from a grounded test specimen are collected. If, however, the test specimen is a biased IC, its differing voltages build up strong electrostatic fields on its surface. These fields are superimposed on the collector field and may completely nullify its effect.

Figure 2 gives a schematic of the potential distribution above 5-μm-wide interconnections. Secondary electrons from grounded interconnections "see" an extraction field, which speeds them up on their way to the collector. But the secondary electrons from the interconnection with a voltage of +5 V have to pass through a retarding field, which forces most of them back onto the interconnection. The collector thus receives fewer secondary electrons from the interconnection with a 5-V potential, as a result of which this interconnection is displayed as being darker than one at ground potential.

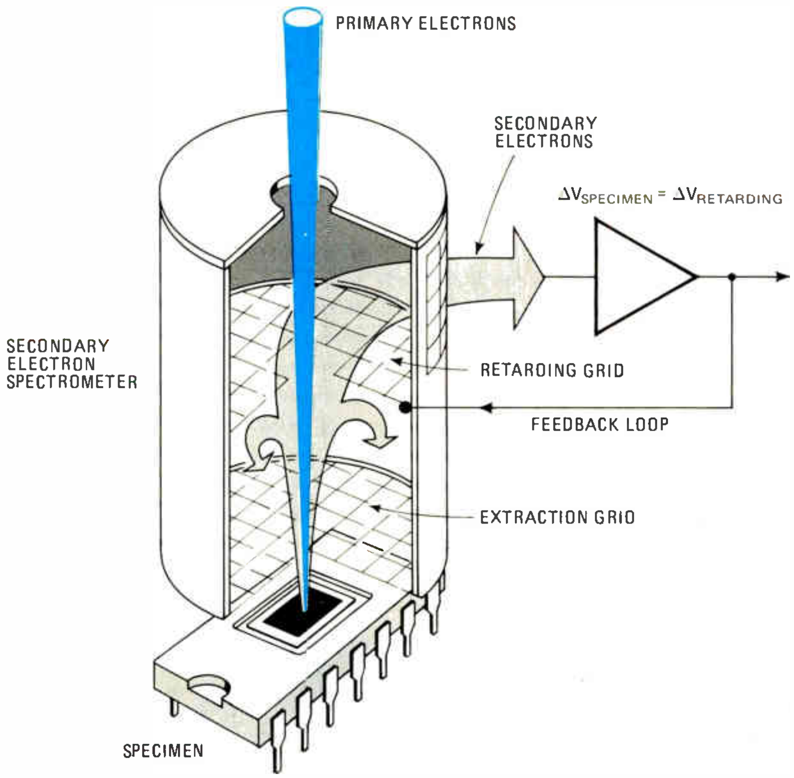
Voltage contrast is nonlinear because of the nonlinear characteristics of electrostatic fields, and it can be affected by voltage changes in adjacent interconnections. It is therefore unsuitable for the quantitative measurement of voltage. However, logic states may be represented with very good contrast, the 0 being light and the 1 being dark.

Display of digital signals

In the analysis of ICs, it is important to know both when and how logic states change, as well as voltage behavior with time. For these measurements, Siemens has applied three techniques: two for representing digital signals—logic-state mapping and the logic-state timing diagram—and one for measuring the waveform mode, which does not use voltage contrast. The first two techniques were specially developed for analyzing microprocessors and microcomputers.

For logic-state mapping, the pulsed electron beam scans in the Y direction across the interconnections (only two of which are shown in Fig. 3a). When the electron beam has reached the end of the line scan, it jumps back to the beginning and the process begins again. While the pulsed electron probe on the IC always scans the same path in the Y direction, the electron beam on the screen of the sampling electron microscope scans the screen line by line so that a two-dimensional micrograph emerges.

Simultaneously with the line feed in the Y direction, the φ phase of the electron pulses is continuously shifted in accordance with the sampling principle. As the phase range along the X direction of the micrograph is freely selectable, it is possible to present either the entire signal loop or selected parts of it in a logic-state mapping. Figure 3b gives a schematic of the clock signals, which are applied to the two interconnections, while Fig. 3c shows the corresponding logic-state mapping, indicating the 1s as dark areas and the 0s as light bars.



5. Voltage measurement. To make an actual voltage measurement, a secondary electron spectrometer is added on to the sampling electron microscope. The spectrometer extracts secondary electrons emitted by the IC, slows them in a retarding field, and then deflects them to the collector.

For a comparison with the logic design, it is useful to be able to present the information contained in the logic-state mapping in the form of a timing diagram. This can be accomplished with an electron probe and a logic analyzer.

The pulsed electron probe jumps from one chosen interconnection to another (Fig. 4a). Its dwell time on the interconnections is chosen in such a way that it is possible to clearly differentiate between 0 and 1 levels. When the electron probe has reached the last interconnection, it jumps to the starting point again, its ϕ phase being shifted by an adjustable discrete value.

The process is repeated until either the entire signal loop or simply certain desired parts of it have been measured and presented in a logic-state diagram. Figure 4b shows the clocks applied to the interconnections, and Fig. 4c shows a logic-state diagram that has been generated with the electron probe and displayed on the screen of a conventional logic analyzer.

Voltage measurement

For waveform measurement of analog signals, the electron probe is directed to a fixed measurement point on an IC. As in the case of the voltage contrast, secondary electrons are used for the voltage measurement. This method takes advantage of the physical effect that a change of voltage at the measurement point, $\Delta V_{specimen}$, shifts the energy distribution of the released secondary electrons by $e\Delta V_{specimen}$. A change in voltage can thus be determined with the aid of an electron spectrometer on the basis of the energy of the secondary electrons.

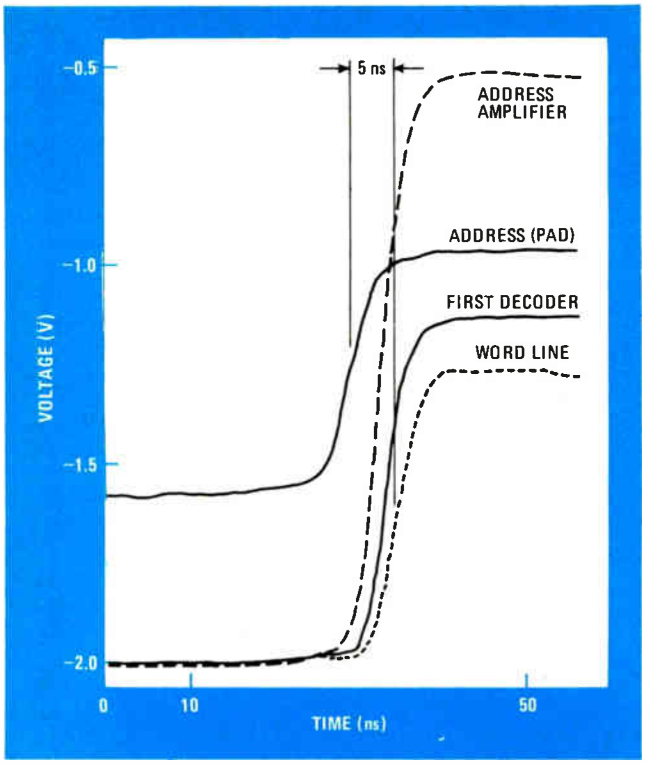
The electron spectrometer (Fig. 5) used for this purpose fits underneath the lenses of Fig. 1. This unit removes the secondary electrons from the surface of the IC with a strong extraction field and slows them down in a retarding field through which only high-energy secondary electrons can pass.

Then these electrons are deflected to the collector where they control the retarding field grid via a feedback loop in such a way that the number of them allowed to pass through that field is always kept constant. A $\Delta V_{specimen}$ change in voltage at the measurement point that would result in a change of the secondary-electron current at the collector is counteracted by the feedback loop by means of a similar $\Delta V_{retarding}$ at the grid: $\Delta V_{specimen} = \Delta V_{retarding}$. Because of the linear relationship between grid voltage and specimen voltage, the grid voltage thus represents the voltage to be measured.

Like a scope

In order to achieve a bandwidth sufficiently high to match those of VLSI circuits, the voltage measurement setup has to function much as a sampling oscilloscope. In such an oscilloscope, a diode circuit controlled by a timing unit sets a time window into a high-frequency signal. Amplification of the signal samples that are then gathered within the window can be performed by an amplifier with limited bandwidth.

In electron-probe sampling, short primary electron pulses take over the function of the electronic time window. The pulses are generated in a blanking capacitor, which, driven by the timing unit, pulses the beam in such a way that it strikes the measurement point only in a defined phase of the applied signal. The secondary electrons released at that phase can then be amplified by a feedback-loop amplifier with limited bandwidth. Shifting the defined phase makes it possible to completely sample a waveform.



6. Time resolution. Measurement of the delay times between the application of the address to the pad and the selection of the word line in the memory area of a 4-K-by-1 ECL memory demonstrates that the electron probe can resolve fine time intervals.

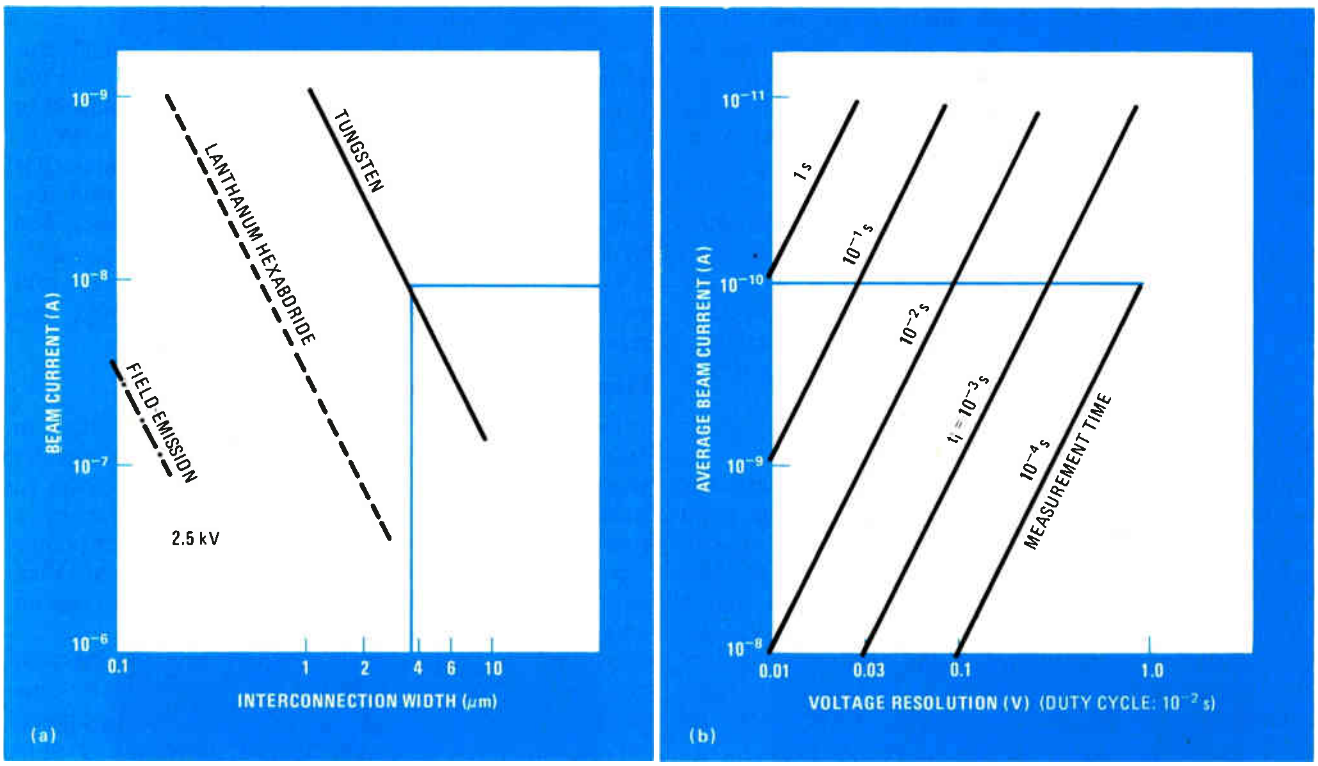
Five applications

The performance of the various features of the three new electron-beam probing techniques are apparent in the following five practical examples, chosen to demonstrate the possibilities of applying them to various circuits and process. The first three applications deal with waveform charting on memories, and the others show the logic checks possible on a microprocessor.

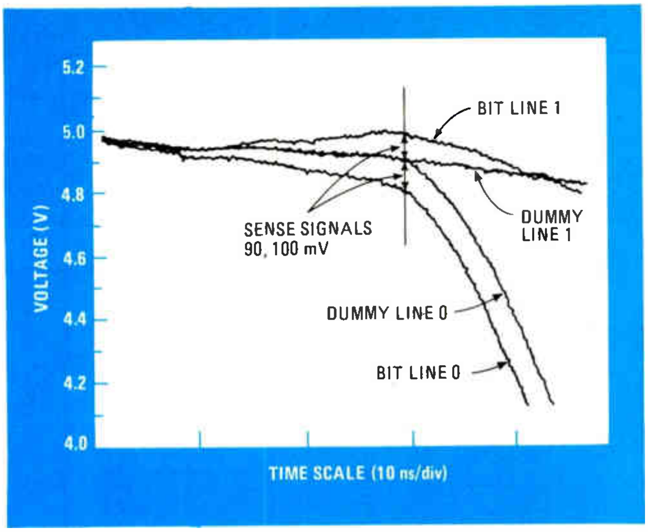
A charge-coupled-device memory circuit, where the shift between 0 and 1 levels is brought about by only 150,000 electrons, demonstrates the nonloading characteristic of the electron-beam probe. The input of the CCD's amplifier is used for sensing the information stored in the memory array. This amplifier has an input capacitance of only 60 femtofarads. The capacitance and current loading at this point are so low that it would be quite impossible to use a mechanical probe with its large stray capacitance.

The sense signal measured by the electron-beam probe between 0 and 1 is 400 millivolts. A prerequisite for this measurement is the precise adjustment of the charge balance between primary and secondary electrons by varying the energy of the primary electrons; in this case the energy is 3.1 kev.

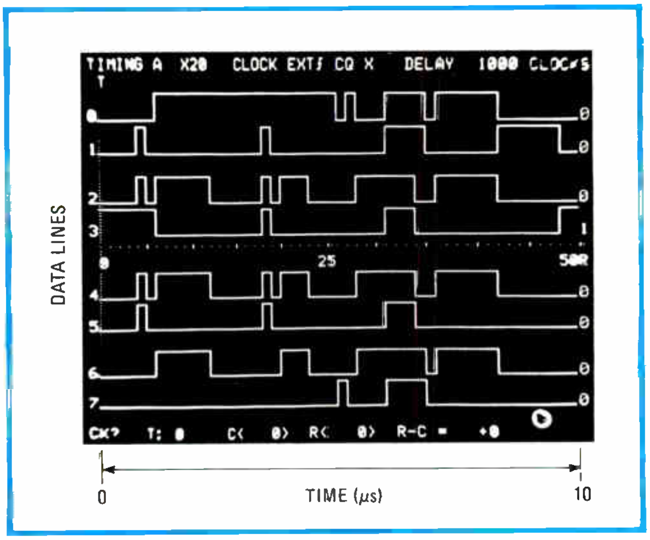
A second example illustrates the ability of the electron-beam probe to resolve small time differences. The wave shape illustrated in Fig. 6 shows that the time differences between the application of an address to the



7. Spatial resolution. Spatial resolution is dependent on a number of parameters such as type of electron-gun filament, beam current, voltage resolution, and measurement time. With nomographs (a) and (b), a graphical solution for the measurement of time is possible.



8. Sense voltage. Measurement of the 90-to-100-mV sense signal of a dynamic 64-K MOS RAM illustrates the voltage resolution of a sampled electron-beam probe. It is possible to read a voltage resolution as low as 10 to 20 mV with this type of equipment.



9. Bus stop. A sampled–electron-beam probing of an 8085's data bus during a short program loop produced this logic state diagram of all signals on the bus during the execution of an add instruction for two operands. Clock signals are shown for reference.

pad and selection of the word line is 5 nanoseconds in a 4-K-by 1-bit emitter-coupled-logic memory. The delays of the switch positions in between can be checked and resolved with an accuracy of ±0.1 ns. Signal waveforms can be sampled with electron pulses at least 0.3 ns wide, so that edges with rise and fall times of 1.5 ns can be precisely displayed.

Spatial resolution

Spatial resolution (the resolution of the window or phase parameter in sampling) and time and voltage resolution are all interrelated. Unfortunately, there is no easy way of indicating the spatial resolution. The parameters that determine this value, namely line width, beam current, voltage resolution, and measurement time are graphically related in the nomograph of Fig. 7.

Proceeding from the width of the interconnections (the abscissa in Fig. 7a), it is possible to determine probe current for three different types of electron-gun filament: tungsten, lanthanum hexaboride, and field-emission. This current value is transferred to Fig. 7b, taking into account the duty cycle of the sampling mode, and it is then possible to read measuring time t_i for a phase point i from this diagram.

The total time for the recording of the waveform is the product of the number of phase points times the measuring time t_i. The overall measuring time for the example shown in Fig. 7 is given by the following: for a line width of 4 μm, using a tungsten filament, with an average probe current of 100 picoamperes at an operating frequency of 2 megahertz and for a 5-ns pulse width, $t_i = 1$ second for V = 10 mV. For sampling at 1-ns intervals, the overall measuring time works out at 40 s for the 40-ns time range.

The voltage resolution capability of the sampling electron-beam probe is illustrated in Fig. 8, which shows a measurement of the sense signal of a dynamic 64-K random-access memory. The two middle curves show the signal of a dummy cell for 1 and 0 levels, which serves as reference signal for sensing. The sense signal is determined by the differences between bit line and dummy line signals and is 90 or 100 mV.

It is possible to read a voltage resolution of 10 to 20 mV from the signal-to-noise ratio. The smallest change of voltage that it is possible to establish with this signal procedure is 1 mV, but that result was obtained with a test device.

A logic-state diagram of the internal data bus of an 8085 microprocessor shows how multiple signals generated by sampled electron-beam scanning can be displayed by a logic analyzer. The bus interconnects the majority of the individual modules of the microprocessor and transmits data between registers.

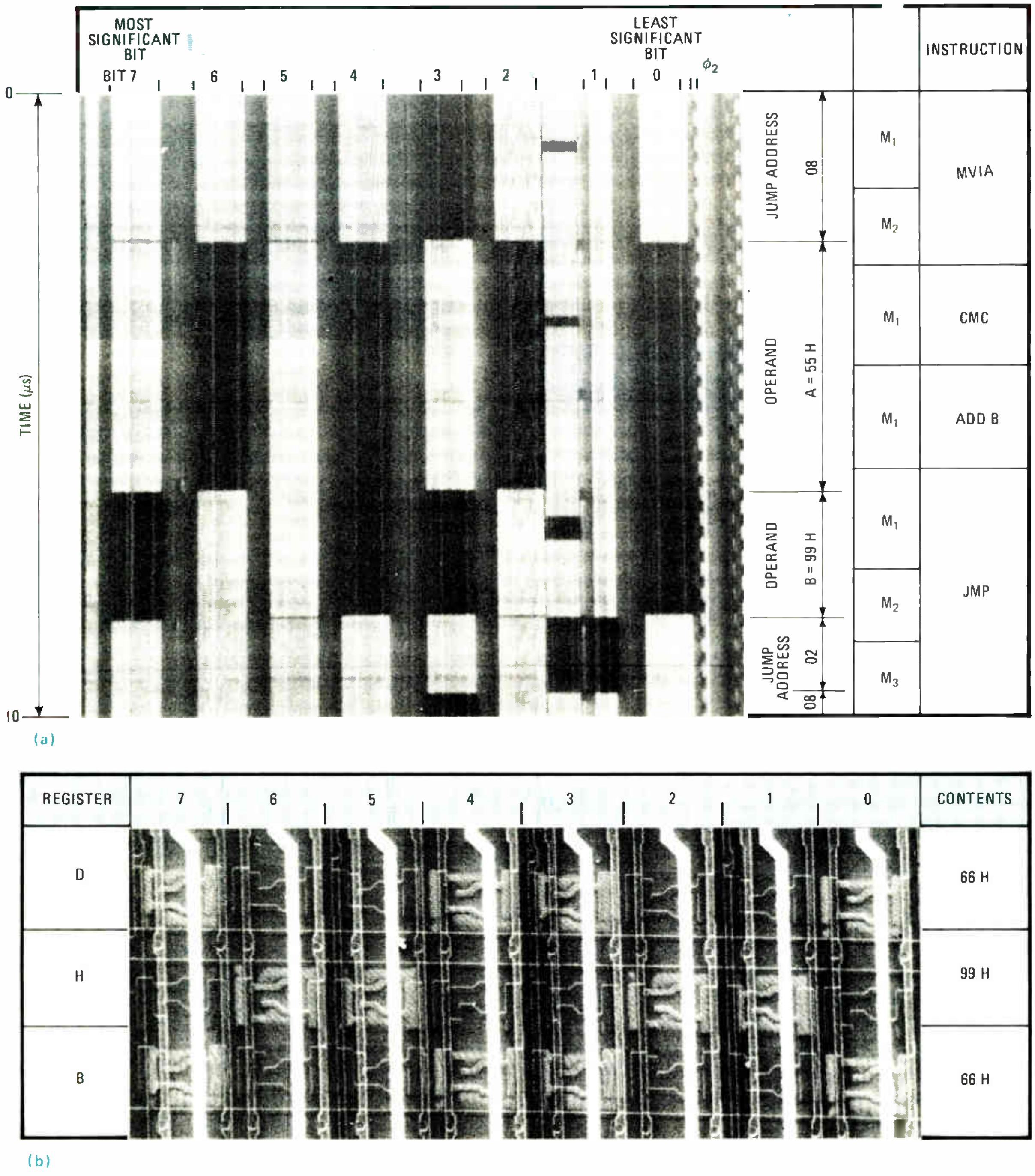
Data busing

The logic state diagram of Fig. 9 shows what is happening on the bus during the execution of a short program loop. The loop consists of the addition of two operands ($01_{16} + FF_{16} = 00_{16}$ + carry). The two internal clock signals are also shown on the diagram for the sake of easy reference.

It should be reemphasized that the electron beam's jumping from line to line at each phase point and repeating this process at the other phase points produces voltage-contrast signals that are weighted, stored, and transferred into the logic analyzer. The dwell time on a line to a phase point is currently at least 2 milliseconds, which means a recording time of 1 s for 50 different phases and 10 lines.

Function modules

The utility of logic-state mapping is exemplified in an application involving the contents of the registers of the 8085 microprocessor. Figure 10a shows the mapping of the temporary register for a short program loop to which the two operands 55_{16} and 99_{16} are added. From this display, it is easy to see when the operands are transferred to the register and when the jump address 08 02



10. Function modules. A logic state mapping (a) shows how register contents change of a 8085 during the same loop as in Fig. 9. A stroboscopic voltage-contrast micrograph (b) of registers A and B shows nodes under a layer of oxide.

for the return to the start of the program appears there.

A second example of logic-state mapping is shown in Fig. 10b. Displayed here are the contents of three registers B, H, and D, whose flip-flops are covered with oxide and are therefore not readily visible in voltage contrast.

Scanning the electron beam with 2.5-kev primary energy charges the oxide positively until impinging and emitted electrons attain equilibrium. If the logic state of the node now changes from 1 to 0 under oxide, then the oxide is recharged at this position and shows up light on the display. Further scanning reestablishes equilibrium, and the voltage contrast disappears.

To map the register contents despite this, the ϕ phase is kept at a constant value while the data is changed. A particular bit pattern and the pattern FF are entered alternately into the registers. The stroboscope voltage contrast of Fig. 10b shows that registers B, H, and D are loaded with constants 66_{16}, 99_{16}, and 66_{16}, respectively. ☐

TDRs profile impedances of backplanes and pc boards

A simple program lets the time-honored technique of time-domain reflectometry be applied to digital design problems

by Norman D. Megill, *Production Services Corp., Waltham, Mass.*

□ Time-domain reflectometry has long been an invaluable method of determining the impedance and integrity of uniform cable lengths. Now with a new algorithm, the method can characterize nonuniform communication paths, such as those found in high-speed backplanes and printed-circuit boards. To apply this algorithm in the form of a subroutine, only a time-domain reflectometer and a desktop computer are needed (Fig. 1).

A time-domain reflectometer (TDR) is a sampling oscilloscope with a built-in or plug-in step generator. The generator injects a step with a very short rise time—on the order of 50 picoseconds—into the cable being tested through an internal resistor. The resistor is usually 50 ohms and is the TDR's characteristic impedance, Z_0.

The waveform at the junction of the resistor and the cable being tested is monitored and displayed by the sampling oscilloscope. This waveform is the initial step plus any reflections that are created by discontinuities in the cable. To make it easier to interpret, the TDR screen is calibrated vertically in a nondimensional unit called a reflection coefficient (ρ) and horizontally in feet or meters.

The vertical scale's reflection coefficient is a variable that relates the reflected voltage sensed at the cable-TDR junction to a scale equaling +1 for an open circuit and −1 for a short circuit. A 50-Ω cable without breaks or shorts produces a ρ of 0. In general, the impedance, Z of a cable is given by the equation:

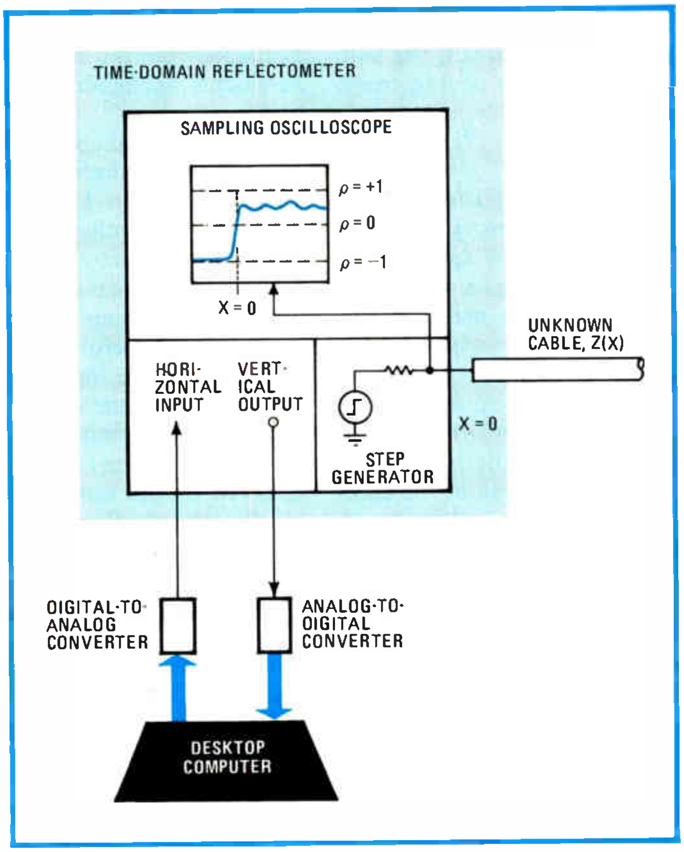
$$Z = Z_0(1+\rho)/(1-\rho)$$

For the horizontal scale, the period of time between the launching of the pulse into the cable and the sensing of a reflection is measured. Since this value when halved is proportional to the distance to the point in the cable from which the reflection originates, the horizontal scale can be calibrated in meters or feet.

The time it takes the waveform to propagate in one direction, referred to as the propagation delay, is typically between 1.5 and 2.0 nanoseconds/ft, depending on the cable's dielectric. Usually, a switch selects the correct delay factor.

Providing computer control for the TDR to examine the waveform is quite easy. Because they use sampling techniques, most TDRs have a port through which the time of the sample, which corresponds to the horizontal (distance) scale, can be triggered. The corresponding vertical displacement is then supplied as a voltage on a TDR auxiliary output. Thus, a computer can control the sample time by driving a digital-to-analog converter and can obtain sample results through an analog-to-digital converter. Samples thus obtained can be used to calculate the path's impedance by using an impedance subroutine (shown on p. 114).

This subroutine, which is written in Basic, may be included in an overall program automating the entire measurement



1. Computerized TDR. Interfacing a desktop computer with a time-domain reflectometer creates a measurement system for profiling nonuniform impedance paths. By controlling the TDR's sampling operation through a d-a converter, the CPU obtains data for the profiling program.

IMPEDANCE-SYNTHESIS SUBROUTINE USED BY TIME-DOMAIN REFLECTOMETER

Line	Statement	Comments
10260	DIM R(200), Z(200)	input array R( ) is destroyed
10270	F=1	initialize comulative forward attenuation
10280	A=1	initialize cumulative round-trip attenuation
10290	Z(1)=R(1)	reflection coefficient at junction of TDR and cable
10300	FOR I=2 TO N	
10310	D=R(I)−R(I−1)	voltage change observed at TDR
10320	R(0)=0	inject forward wave of 0 after TDR step
10330	R(I−1)=0	assume no backward reflection from segment I
10340	FOR J=I−1 TO 1 STEP −1	
10350	B=R(J−1)	temporary variable
10360	C=(B−R(J))*Z(J)	temporary variable
10370	R(J−1)=R(J)+C	compute incomplete backward wave
10380	R(J)=B+C	compute incomplete forward wave
10390	NEXT J	
10400	A=A−A*Z(I−1)^2	update cumulative round-trip attenuation
10410	Z(I)=(D−R(0))/A	compute new reflection coefficient
10420	IF Z(I)^2<1 THEN 10440	
10430	PRINT "WARNING: SYNTHESIZED CABLE IS PHYSICIALLY UNREALIZABLE"	
10440	F=F+F*Z(I−1)	update cumulative forward attenuation
10450	C=Z(I)*F	backward wave on cable segment I−1
10460	FOR J=I−1 TO 1 STEP −1	
10470	B=C*Z(J)	temporary variable
10480	R(J)=R(J)−B	correct incomplete forward wave
10490	C=C−B	attenuate correction term
10500	NEXT J	
10510	NEXT I	
10520	Z(0)=Z0	TDR impedance
10530	FOR I=1 TO N	convert reflection coefficient to ohms
10540	Z(I)=Z(I−1)*(1+Z(I))/(1−Z(I))	
10550	NEXT I	
10560	RETURN	

PROGRAM INPUTS: Z(0) – the impedance of the TDR system in ohms; N – the number of measure points in the TDR waveform; R(1) through R(N) – the value of each point in units of rho

PROGRAM OUTPUT: Z(1) through Z(N) – the impedance of each segment in ohms (distance to each segment is the same as that to each R( ) as shown on TDR)

procedure. It computes the equivalent transmission line needed to generate the displayed waveform on the TDR.

For the subroutine, the TDR waveform should be sampled in uniform horizontal intervals to obtain N discrete values, R_1 through R_N. Sample R_1 is taken just after the initial TDR step. To calculate the impedances, the subroutine also needs the value of the TDR's characteristic impedance.

Some assumptions

The subroutine uses an algorithm (see "The synthesis algorithm," p. 115) that assumes the transmission path may be represented as N small, uniform segments of ideal transmission lines with identical lengths and propagation velocities. Using these samples, it measures the impedances of segments Z_1 through Z_N, with the distance from the TDR to each segment corresponding to the distance shown for the corresponding sample on the screen. While the distance to each segment from the TDR input point is not required to calculate the impedance, these distances can be measured and stored in the computer using a calibration routine, so that impedance-distance plots can be automatically generated.

However, for the plots to have a valid meaning, care must be taken that the data fed to the algorithm is precise. The synthesis of complex cable structures can be very sensitive to small variations in ρ, particularly near the end of the TDR waveform, when most reflections have been greatly attenuated. Therefore, for accurate profile synthesis, the computer-TDR system must be calibrated before being used and the sample-gathering routine must be written so as to ensure the samples it provides to the computer truly reflect the TDR data.

So that system errors in samples can be corrected before they are used in the synthesis subroutine, the computer should acquire three reference waveforms: open-circuit, short-circuit, and 50-Ω terminations. Precision short-circuit and 50-Ω terminations are usually available from the TDR manufacturer; open-circuit measurements are made by not connecting anything to the TDR input.

The open- and short-circuit measurements supply the computer with digital values representing the full-scale values of $\rho = -1, = +1$. When samples are taken, these digitized values are compared to the scale and are then converted into units of ρ. When a 50-Ω termination measurement is taken, the digital values obtained should be subtracted from the corresponding sample values for the tested line before conversion into units of ρ. This will help compensate for drops that may occur in the output of TDR's step generator.

The 50-Ω termination measurement should also be used to determine at precisely what time the first sample is taken by the sample-gathering routine. That routine should take the first sample as soon as possible after the initial rise, but only after the waveform has settled.

Noise filter needed

Whenever measurements are taken, the TDR's noise filter should be used. Results can be further improved if several sets of readings are taken and averaged.

Settling time is slower if the noise filter is engaged, and the sampling subroutine must take this into account. However, the subroutine should be designed so the TDR's vertical output has sufficient settling time after each horizontal sample value is given to the TDR.

The synthesis algorithm

The synthesis-routine algorithm was developed with the aid of a lattice diagram (shown below). The diagram represents the propagation of the time-domain reflectometer's step voltage down the transmission line and the forward and backward reflections generated by it.

The impedance of any line segment and the effects of both backward and forward reflections must be considered in the algorithm. The reflections affect the measured value of ρ and thus must be accounted for before ρ is used to calculate the actual impedance of a segment.

Once the impedances of any two cable segments, Z_i and Z_{i-1}, have been computed, the backward and forward reflections resulting from the junction between them can be calculated. Using the forward wave generated by the preceding junction of Z_{i-2} and Z_{i-1} (f_{i-1}) and the backward wave generated by Z_i and Z_{i+1}(b_i), the following equations yield the new waves:

$$b_{i-1} = (1-\rho_i)b_i + \rho_i f_{i-1} = b_i + \rho_i(f_{i-1} - b_i) \quad (1)$$

$$f_i = (1-\rho_i)f_{i-1} - \rho_i b_i = f_{i-1} + \rho_i(f_{i-1} - b_i) \quad (2)$$

where:

$$\rho_i = (Z_i - Z_{i-1})/(Z_i + Z_{i+1}) \quad (3)$$

At a TDR observation point r_i, the cable structure can be determined only up through segment Z_i, because the initial TDR step must make a trip to segment Z_i and back to convey information about it. The history of the cable waves, not their current state, is known. In the figure, all forward and backward waves are known at and above the lattice diagonal leading from A to B. Waves below the diagonal are unknown.

Consider the observation at point A. A new backward wave of amplitude $r_5 - r_4$ comes from the cable and is superimposed on the TDR waveform. At this point, reflection coefficients ρ_1 through ρ_4 are known; ρ_5 is to be determined. A description of the procedure follows, using iteration i = 5 as an example.

- ☐ Compute $r_5 - r_4$ and save it for later use.
- ☐ Inject a forward wave $f_0 = 0$.
- ☐ Assume that $\rho_5 = 0$ (that is $b_4 = 0$) and compute incomplete backward and forward waves b_3, f_4, b_2, f_3, b_1, f_2, b_0, and f_1 in that order. (The waves are called incomplete because they do not account for any reflection from segment Z_5.) Each wave is calculated from the two waves just above it (just previous to it in time), using equations 1, 2, and 3. By computing b_j and f_j in this zigzag order down the lattice diagram diagonal, the same array can be used to store both of them since only b_0 and f_1 through f_4 will be needed later on; b_j is destroyed when f_j is computed.
- ☐ At this point, the incomplete backward wave b_0 is not equal to the observed TDR voltage increment $r_5 - r_4$, since the contribution of the reflection from cable segment Z_5 has been omitted. The difference between the two is:

$(r_4-r_5)-b_0$ = (forward attenuation) × (reflection at Z_5) × (backward attenuation)

$$= \left[\prod_{j=1}^{4}(1+\rho_j)\right]\rho_5\left[\prod_{j=1}^{4}(1-\rho_j)\right] = \rho_5\prod_{j=1}^{4}(1-\rho_j^2)$$

Solving for ρ_5 yields:

$$\rho_5 = \left[(r_4 - r_5 - b_0)\Big/\prod_{j=1}^{4}(1-\rho_j^2)\right]$$

Now that ρ_5 is known, the true b_4 can be calculated:

$$b_4 = \rho_5\prod_{j=1}^{4}(1+\rho_j)$$

The forward waves f_1 through f_4 are still incomplete (that is, they assume $b_4 = 0$). They must be correct for use in the next main-loop iteration. The correction term to be added to each f_j is the attenuated b_4 after it travels back through four j segments and reflects onto the forward segment j:

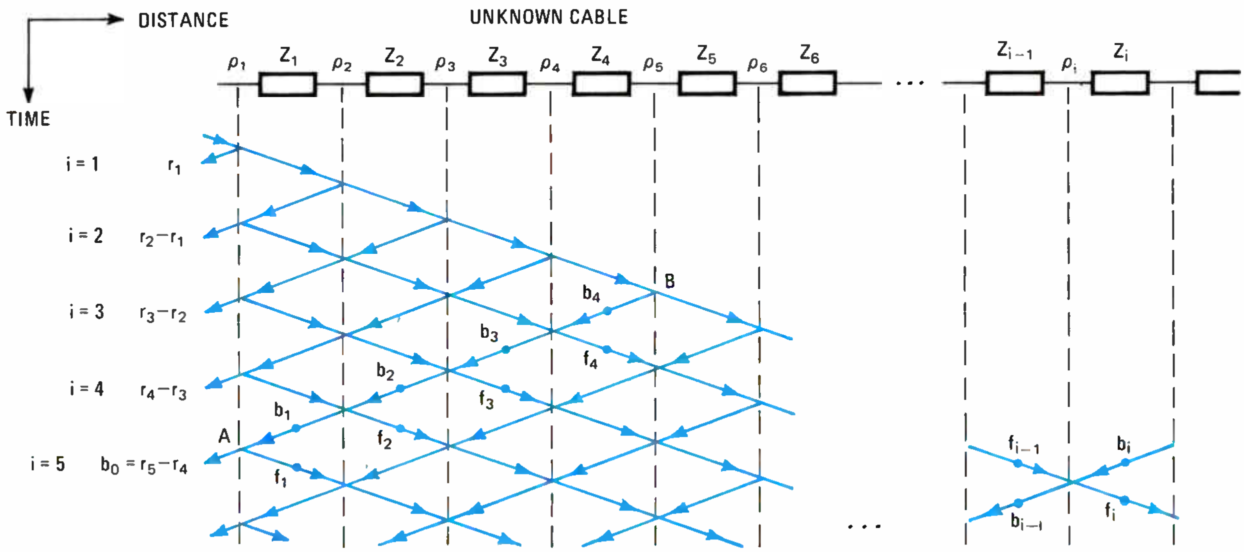
$$f_j(\text{true}) = f_j(\text{incomplete}) + b_4\left[\prod_{k=j+1}^{4}(1-\rho_k)\right](-\rho_j)$$

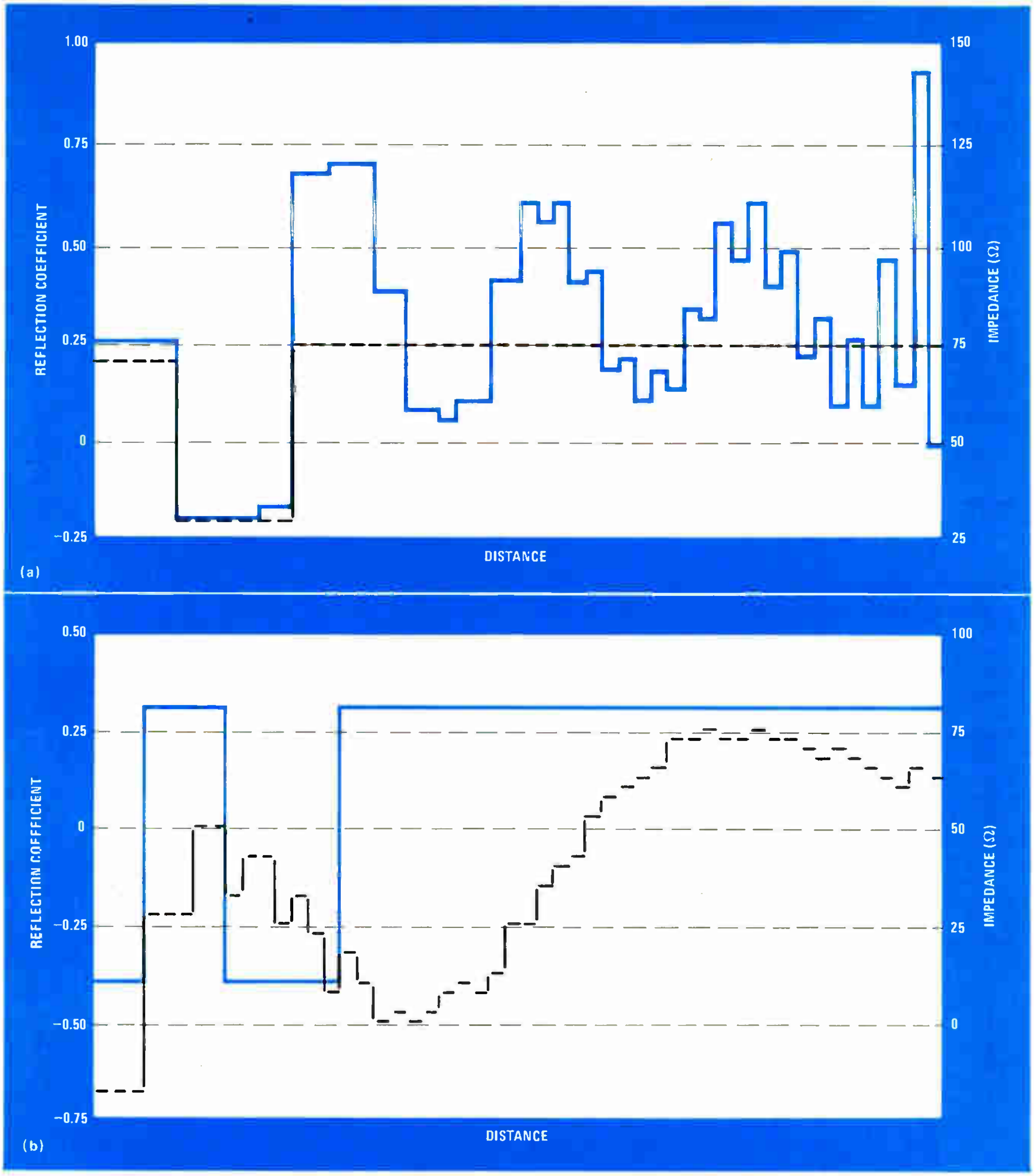
for j = 1, 2, 3, 4; for j = 4, $\Pi(1-\rho_k) = 1$.

After these calculations are done for all segments, the reflection coefficients ρ_i at cable segment junctions are used to compute impedances Z_i of the segments:

$$Z_i = Z_{i-1}(1+\rho_i)/(1-\rho_i),\ i = 1, 2, \ldots N$$

where Z_0 is the TDR's characteristic impedance.



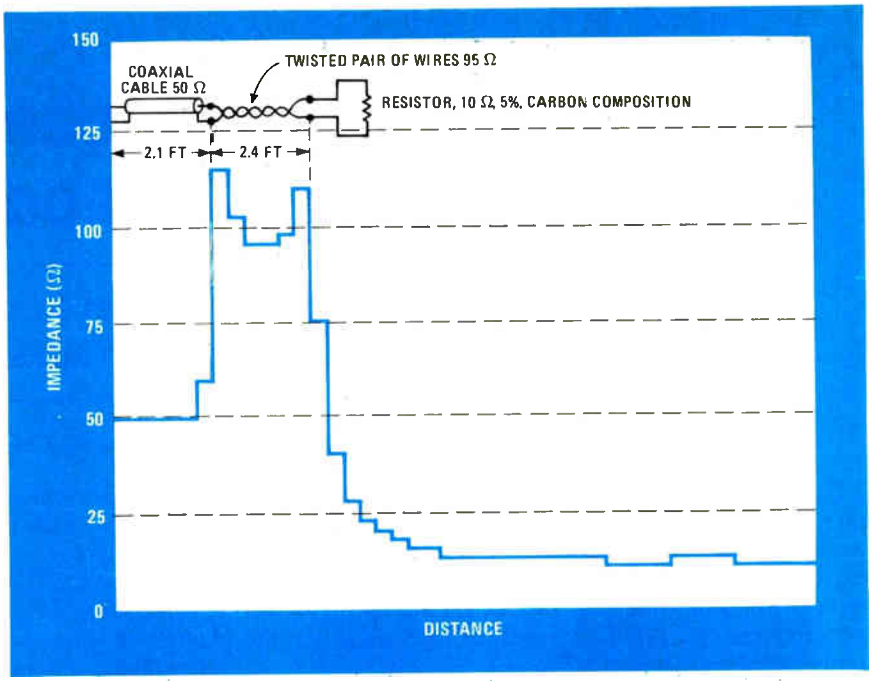


2. Elusive. The correlation between the TDR waveform and the impedance profile is not easy to visualize. In the graphs above, hypothetical TDR waveforms are shown as a dashed line with their scales at left, while corresponding impedance profiles are overlaid in color with their scales at right. In (a), a simple TDR waveform produces a complex transmission path profile, while in (b) just the opposite is true.

Even with highly accurate data, the synthesis subroutine has its limitations. Its algorithm computes the equivalent impedances of small ideal transmission line segments. Various factors—high frequency losses, inductance and capacitance, variations in propagation velocities, step rise time—can distort the correspondence between the real test cable and the synthesized one.

The effects of these factors can best be determined by experimentation. One useful technique is to terminate a cable with a fixed resistor and observe how well that resistor is modeled, particularly at its junction with the cable. The terminating resistor should appear on the TDR as an infinite transmission line with an impedance equal to the value of the resistor. Another technique is to

3. Cause and effect. The transmission line shown at the top was measured with the TDR-computer system, producing the impedance profile seen below it. Note that the terminating 10-Ω resistor appears in the profile as an infinitely long and fairly uniform 10-Ω transmission line, a typical result for such a termination.



WAVEFORM-SYNTHESIS ROUTINE USED BY TIME-DOMAIN REFLECTOMETER

Line	Statement	Comments
12260	DIM R(200), Z(200), W(200)	input array Z( ) is destroyed
12270	Z(0)=Z0	TDR impedance
12280	FOR I=N TO 1 STEP −1	convert ohms to reflection coefficient
12290	Z(I)=(Z(I)−Z(I−1))/(Z(I)+Z(I−1))	
12300	NEXT I	
12310	R(1)=Z(1)	first voltage at junction of TDR and cable
12320	W(1)=1+Z(1)	first forward wave on cable segment 1
12330	FOR I=2 TO N	
12340	W(0)=0	inject forward wave of 0 after TDR step
12350	W(I)=0	initialize backward wave on new segment I
12360	FOR J=I TO 1 STEP −1	
12370	B=W(J−1)	temporary variable
12380	C=(B−W(J))*Z(J)	temporary variable
12390	W(J−1)=W(J)+C	compute backward wave along lattice diagonal
12400	W(J)=B+C	compute forward wave along lattice diagonal
12410	NEXT J	
12420	R(I)=R(I−1)+W(0)	add backward wave to get new TDR voltage
12430	NEXT I	
12440	RETURN	

PROGRAM INPUTS: Z(0) – the impedance of the TDR system in ohms; N – the number of points in the impedance profile; Z(1) through Z(N) – the impedance in ohms at each point in the profile

PROGRAM OUTPUT: R(1) through R(N) – points on the TDR waveform (distance to each point is the same as the distance to each corresponding impedance in the profile)

measure the impedance of the cable from both ends and compare the results.

The algorithm assumes that all cable segments have a finite, positive impedance. However, in some cases where components other than transmission lines are part of the transmission path, it is not possible for the subroutine to synthesize the impedance profile because a negative impedance is required. In this instance, the synthesis subroutine shown previously will print out a warning message.

If the cable has a short or open circuit, a divide-by-zero could occur at line 10410 of the subroutine; in practice, measurement and round-off errors will usually prevent this from occurring. Even if a divide-by-zero does not occur, all synthesized impedances after the short or open will be meaningless. More sophisticated error traps for these conditions can be added to the subroutine.

The relationship between the TDR waveform and the synthesized impedance profile is frequently not obvious and cannot be easily obtained by inspection. A simple TDR waveform may result in a complex profile and vice versa. Figure 2 demonstrates this fact.

Real output

In Fig. 3, the results of TDR measurement and the synthesized impedance profile are compared to the test transmission line. The large inductance at the ends of the 50-Ω cable, combined with the poor high-frequency response of the twisted wire pair, tends to blur the junction at the terminating 10-Ω resistor.

It is also possible to predict the TDR waveform when the impedance profile of a line is already known. Thus, the TDR waveform synthesis routine (shown above) allows experimentation with different impedance profiles. □

Digital signal processing hits stride with 64-bit correlator IC

Chip generates 7-bit output for error-correction, data synchronization, and other auto- and cross-correlation tasks at 15-MHz clip

by John Eldon, *TRW Inc., LSI Products Division, San Diego, Calif.*

☐ Correlation, or the comparison of two signals to determine their similarity, has become yet another signal-processing function whose design has been simplified by very large-scale integration. The TDC1023J monolithic digital correlator compares two 64-bit words bit by bit and produces a 7-bit digital output that indicates the number of bits in agreement.

Design engineers will find that this digital-output, one-chip version of a classic, multicomponent circuit can be used in most cross- and auto-correlation applications (see "The fundamentals of correlation," below). These include error correction for computers and their peripherals and interference reduction in communication systems; pattern recognition for image processing; bit, word, and frame synchronization for telemetry, video, and computer systems; and time-delay measurements for instrumentation, radar, and sonar systems. In other words, code correction, data synchronization, and time-delay measurements are major uses for the 24-pin, bipolar 1023J, which is capable of a correlation rate of over 15 megahertz—a speed that is adequate for many cross- and auto-correlation applications.

The simplest correlation process performed is illustrated in Fig. 1a, where an 8-bit reference word is correlated with an incoming signal. The reference word, stored in a register, is compared with the incoming signal at each clock time. For each clock pulse, the number of agreeing bits is shown in decimal and binary notation (Fig. 1b). Maximum correlation occurs when all 8 reference bits match the respective incoming signal bits. As illustrated, correlation can be performed between two real-time signals, two stored signals, or one real-time and one stored signal, as the application requires.

The simplest implementation of digital correlation employs one serial-in, parallel-out shift register to store the reference signal and a similar shift register to accept

The fundamentals of correlation

Correlation of a stored and an incoming signal involves three basic operations: time shifting (delay), multiplication, and integration (summation). The shifting is performed first, followed by the multiplication and finally by the integration steps.

Multiplying the stored and incoming signals satisfies the logical definition that the correlation value should be +1 whenever the waveforms are identical. A positive correlation results from two signals of like sign, whereas a negative correlation occurs for signals of opposite sign.

Performing an integration after multiplication averages the product and aids in rejecting any noise that enters the correlator on the incoming signal. The closer the integration time is to the total time period of the signal, the greater the accuracy of the final average will be and the better the noise rejection.

Mathematically, correlation between two functions x(t) and y(t) is given by:

$$R_{12}(\tau) = \lim_{T \to \infty} \frac{1}{T} \int_{(-t/2)}^{(+t/2)} V_1(t) \cdot V_2(t+\tau)dt$$

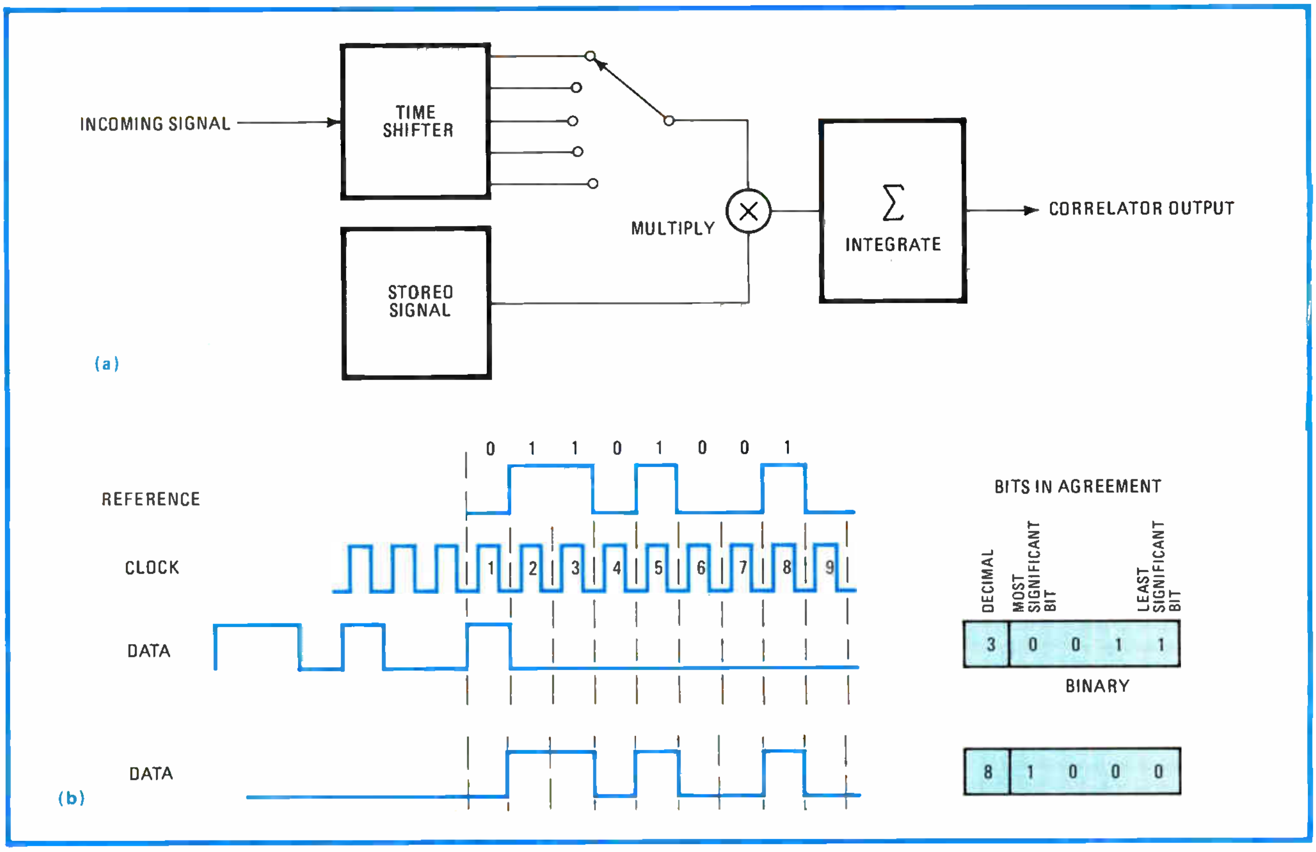
Here, $R_{12}(\tau)$ refers to the correlation between two signals $V_1(t)$ and $V_2(t)$ with relative time offset, τ, which is determined by multiplying $V_1(t)$ by $V_2(t+\tau)$ and then taking the integral of the product. If both $V_1(t)$ and $V_2(t+\tau)$ are periodic with common period T_0, the expression becomes:

$$R_{12}(\tau) = \int_{(-T_0/2)}^{(+T_0/2)} V_1(t) \cdot V_2(t+\tau)dt$$

Correlator applications can employ either cross-correlation or autocorrelation techniques. Cross-correlation is a bit-by-bit comparison between two real-time, delayed, or stored sequences. In contrast, in autocorrelation, one of the sequences is a time-delayed, exact replica of the other sequence.

Cross-correlation applications include the detection of differences (errors) between two data sequences and the determination of the time delay between two similar signals such as radar transmission and its returning reflection. Moreover, they also enable the multiplexing of data among several users, recognition of specified patterns in a data stream, and synchronization of a decoding process with an incoming data stream.

Autocorrelation is most useful in identifying periodicities within a data stream and as a time-domain alternative to spectral analysis and the associated time-domain–frequency-domain transformations. It can also be used to extract a periodic signal from its random noise background, since the signal correlates well with itself, but poorly with the random interference.



1. Bit by bit. In a correlation circuit, corresponding bits of a reference word and an incoming signal are compared to determine which are in agreement (a). The number of bits that are in agreement may be indicated by a decimal or a binary output (b).

the incoming signal (Fig. 2a). The reference word and incoming signal are compared by exclusive-NOR gates whose inputs are obtained from corresponding bit positions of the two registers. A logical 1 output from an exclusive-NOR gate indicates that both inputs are equal. The outputs of all the exclusive-NOR gates are applied to a summing network whose 7-bit output indicates the number of bits in agreement.

Either of two summing networks may be employed. An analog-output type provides a voltage or current that is proportional to the number of bits that correlate. A digital summing network, most useful in the applications discussed later, provides a binary count of the number of bits that correlate.

Bit by bit

Correlation is performed in the 1023J by serially shifting the reference word into an independently clocked 64-bit register (called the B register) and then serially shifting the incoming signal into the independently clocked 64-bit A register (Fig. 2b). By making load R a logical 1, the reference word is copied in parallel into the R latch. The user can then load a new reference word into the B register while correlation takes place between the A register and R latch.

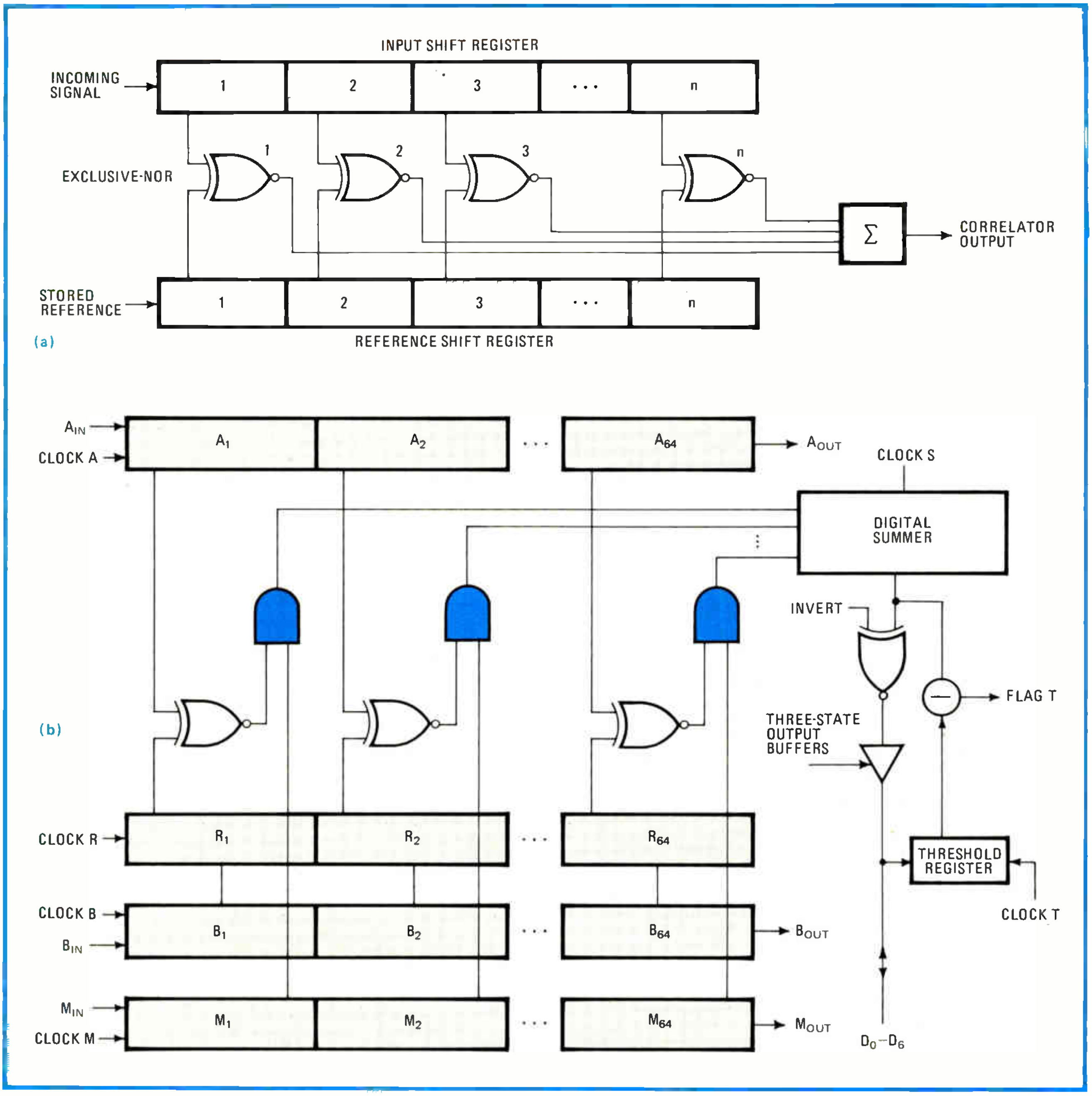
Bit-by-bit comparisons between the A register and the R latch are made by the exclusive-NOR gates, whose outputs are applied to a digital summer through enabling AND gates. The output of the digital summer is a 7-bit binary word representing the number of bit positions in the A register and R latch that are in agreement during the current A-register clock cycle. Since the digital summer is pipelined for the maximum data throughput rate, the updated correlation level appears after a delay of three summer clock cycles and still permits 15-MHz real-time correlation.

The designer may select bit positions where no comparisons are to be made by using the mask register. This is done by inserting a 64-bit serial word into the register with logical 0s in the bit positions indicating no comparison. Since the outputs from the register are applied to the AND gates that also contain the outputs from the exclusive-NOR gates, masked bits are prevented from reaching the digital summer.

Either a true or an inverted binary output can be selected from the 1023J using the invert control line and seven exclusive-OR gates that receive inputs from the digital summer. The gate outputs are then applied to seven three-state output buffers controlled by the time-shifted signal. A logical 1 on the time-shift line disables the buffered outputs by placing them in a high impedance state. When the output buffers are enabled and the invert signal is a logical 1, the outputs are inverted.

Establishing a threshold

If desired, a correlation threshold can be established in the 1023J by using the 7-bit independently clocked threshold register. To accomplish this, the time-shift control line is first used to disable the output buffers. Then, output lines D_0 through D_6 are used to load the



2. Many parts. Shift registers, exclusive-NOR gates, and a summing network make up the basic correlator (a). Three independently clocked 64-bit shift registers and one 64-bit latch store and shift data while comparisons are made by 64 exclusive-NOR gates (b).

desired binary threshold number into the register in parallel. Thereafter, the threshold flag will become a 1 when the binary number from the digital summer equals or exceeds the number in the register.

The output of the 1023J, designated S, is the total number of agreements between the bits in register A and those in latch R, not the number of agreements (positive product elements) minus the total number of disagreements. If desired, the statistically rigorous correlation coefficient, R, can be computed from S, since $R = (2S-M)/M$, where M (often 64 in practice) is the number of bits under comparison, or the number of logical 1s in the masking register. Under this equation, a correlator output of $S = 32$ with $M = 64$ bit positions enabled actually corresponds to zero (random) correlation between two data sequences.

When a correlation code longer than 64 bits is required, chips may be cascaded in series, as when the A_{out}, B_{out}, and M_{out} lines from each device are connected to the corresponding input of the next device. A binary adder is used to sum the outputs of the correlators. If a threshold flag is required, external integrated-circuit equivalents of the threshold register and threshold magnitude comparator must be used. The maximum number of correlators that can be added is limited by the loading and speed of such external circuits.

Error-correction techniques employed in computer and communication systems to ensure the error-free transmission of data are a major application for the 1023J. This procedure requires the use of expanded codes that contain extra bits beyond those absolutely required to convey information.

The improvements possible with expanded codes can be observed by first looking at a maximum-efficiency unexpanded code like ordinary binary numbers. In the binary system, each code is separated by only 1 bit from its neighboring code. Thus, a single 1-bit error transforms one allowable code into another unintended code.

In coding terminology, the binary system is said to exhibit a 1-bit distance between codes and the number of tolerable simultaneous errors is zero. For example, if the code 1110 is transmitted but 0110 is received, there is no way to detect the error.

Expanding for redundancy

Expanding a 4-bit binary code into a 7-bit code produces a redundant system that can correct single errors and detect up to two simultaneous ones. This expansion increases the number of possible code combinations from 16 (2^4) to 128 (2^7), but only 16 are valid codes. In this case, the true codes can be chosen to differ by at least 3 bits from all other correct codes. With this distance, each single-error code can be unambiguously associated with a particular code. The digital correlator is, of course, not limited to this code, and a variety of others can be accommodated.

The 1023J can readily be used in a system that employs a 7-bit expanded code. This arrangement involves a trial-and-error process wherein the incoming signal is compared with the 16 possible correct codes that are stored in memory. First, the incoming 7-bit signal is loaded into the B register and copied into the R latch. Then, the library of correct codes is sequentially applied to the A register, which compares each of the 16 possible correct codes with the incoming signal that is stored in the R latch. In this example, a correlation threshold of 6 is established in the T register to flag only perfect or nearly perfect correlations. The correlation flag threshold is set at the user's discretion.

Going by the clock

The system can operate at a fixed rate, clocking in a new data word after each full cycle through all combinations stored in the memory. Alternatively, the threshold flag can also restart the B register clock. In such a system, a new data word is clocked in as soon as a high correlation is reached, in effect short-cycling the system.

As described, the system is usable for single-error codes. If a relatively high error rate is anticipated, an even longer code expansion must be employed to increase the system's error tolerance. Using a carefully designed enhanced code, double-, triple-, or higher-order errors can be accurately corrected. In fact, the maximum number of simultaneous errors that can be corrected will always be less than half the distance between codes. However, because longer codes necessitate transmitting useful information at a slower rate, there is a tradeoff between a code's efficiency and its error tolerance. Which code is used depends on the application at hand.

If higher data handling speeds are required in such an error-correction scheme, the incoming data stream can be applied to two or more correlators. If two correlators are used, each correlates the incoming data segment with only half of the possible correct codes contained in the memory. When one correlator registers an acceptably high level of correlation between the incoming data stream and one of the stored correct patterns, it feeds the contents of its A register serially to the output.

Explicit instructions

If fewer than 64 bits are required by the error-correction system, the masking register may be used to instruct the correlator to ignore the bits where no comparison is desired. It is done by masking the first $64-N$ bits, where N is the number of bits of code. The last N bits in the register are then compared with the incoming word sample. When a high correlation is obtained, the correct signal occupies the last N positions of the A register and can be shifted out serially.

Although test patterns can be read sequentially into the A register without any spacing between words, synchronization data must inform the correlator when a new word is in position for testing. If this is not done, an unsynchronized comparison between an incoming signal segment and pieces of two sequentially stored patterns could trigger a false agreement.

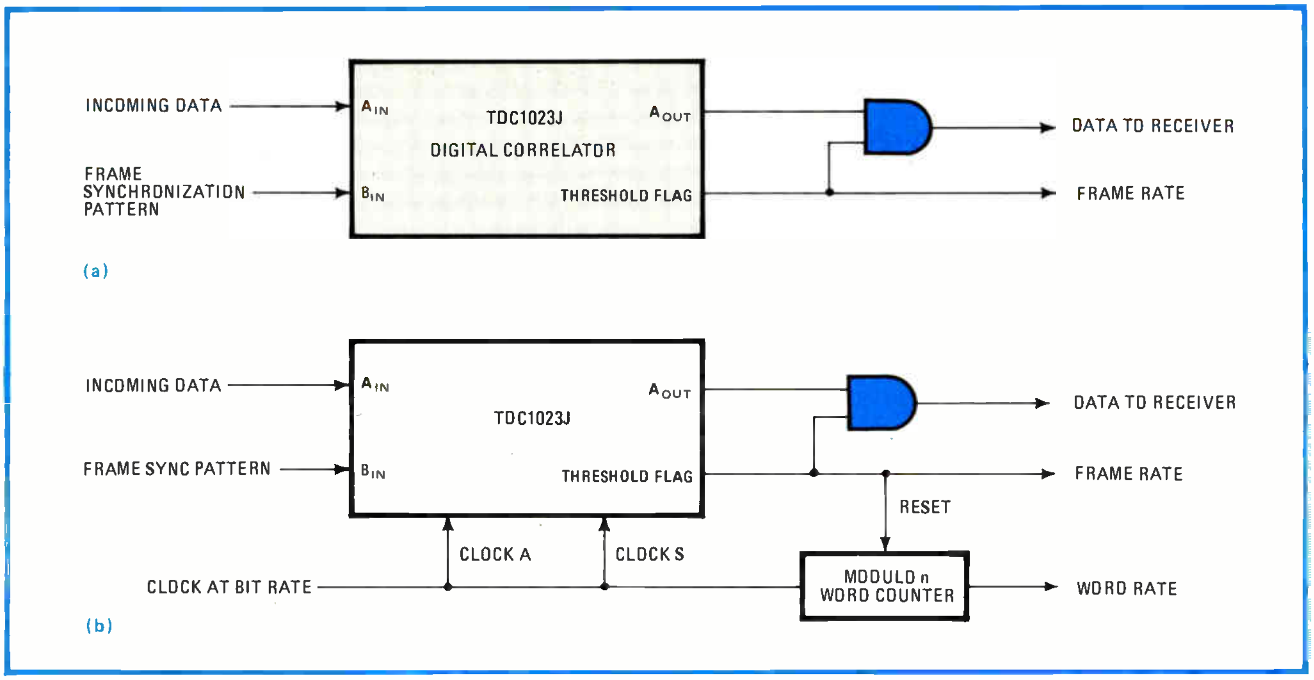
The concept of code expansion can also be used to reduce the number of errors encountered in a high-noise or a high-interference environment. For example, a specific 64-bit code and its complement can be assigned to the binary values 1 and 0, respectively. Then, instead of a simple sequence of 1 and 0, a much longer serial sequence, consisting of the desired combination of expanded codes for 1 and 0, is transmitted. The resulting message contains the intended information, plus redundancy that permits detection of errors in the transmission and reception of the data.

Error detection is readily accomplished at the receiving end of a data transmission using only two receiver correlators—one holding the code for a 1 and the other holding a 0, to reconstruct the intended message. Then, whenever an expanded code version of a 1 or 0 is received, the appropriate correlator sends a 1 or 0 message to the output, where it can be transmitted to the remainder of the system.

Getting into sync

Synchronization of data frames, words, or bits is another common application for correlators. In frame synchronization, a correlator identifies the start of each new frame, or major group, of information. In word synchronization, the beginnings of individual data words are detected. In contrast, bit synchronization involves aligning individual bits of incoming information with the receiver's bit-by-bit clock.

A system can achieve and maintain frame synchronization only if the incoming data stream is interrupted periodically by a specific start-of-frame pattern. This pattern, transmitted at the beginning of each new frame, tells the receiver that a new frame will immediately enter



3. Synchronization. Frame synchronization is accomplished by comparing the pattern embedded in the incoming data stream with the pattern loaded in the B register (a). Word sync may be derived from frame sync with a modulo n counter operating at the system's bit rate (b).

the input register and must be handled accordingly. For example, in a video system, the start-of-frame pattern tells the receiver to return to the start of its vertical and horizontal scan. In a nonvideo application, such as a data filing system, the frame synchronization pattern can denote the beginning of a new group of data. This might be the data file for a particular individual.

Frame of reference

In a frame synchronization system, the B register of the 1023J is preloaded with the standard synchronization pattern, while the incoming data stream is shifted through the A register (Fig. 3a). When a frame sync pattern embedded in the incoming data stream aligns exactly with the stored sync pattern, the correlator's threshold flag goes to a logical 1, instructing the receiver to start handling a new frame of data. The start-of-frame pattern must be long and unusual enough to prevent false synchronization. However, this means that a percentage of the total data stream is unavailable for transmitting useful information.

The receiver-correlator system operates continuously, with the correlator producing a flag value of logical 1 as it receives each successive frame sync pattern in the incoming data stream. The rate at which these high outputs are generated is the frame rate of the incoming data. As long as its scanning system is reset at this rate, the receiver remains synchronized with the incoming data and continues to distinguish one frame or group of data from the next.

When presented with a data stream comprising a series of individual words, a system must decide where one word ends and the next begins. One technique for separating words in a continuous bit stream is to insert a start-of-word marker pattern at the end of each word and before the start of the following word.

The 1023J correlator in the receiver system can be programmed to identify the start-of-word marker. In operation, the correlator puts out a high correlation value whenever it encounters a start-of-word signal, which is analogous to the frame synchronization signal described earlier. If the data vocabulary and start-of-word marker are carefully selected, the correlator's output reaches isolated high values at the word rate with much lower correlation levels. If the signal-processing system is programmed to begin handling a new word at each correlator output, it remains synchronized for words with the incoming data and successfully distinguishes between individual incoming words.

The start-of-word marker code must be carefully selected to minimize the possibility of false triggering by data or noise, rather than the true synchronization pattern. Such low-error synchronization patterns are described in the literature on shift-register sequences, Barker codes, and spread-spectrum signal-theory.

Although the procedure can yield accurate word synchronization, it will be inefficient if the markers occupy a significant percentage of the total data stream. Clearly, if the number or length of the markers can be reduced, then more data can be sent.

Marking off the words

If the data words are organized into fixed-length frames and a frame synchronization marker is included, word synchronization can be derived from frame synchronization (Fig. 3b). If there are always N words per frame, then the word rate is N times the frame rate. The frame-rate output pulses of the frame synchronization correlator can be multiplied upward to produce the needed word synchronization pulses. Given a fixed word length, word synchronization can be established with a recirculating counter, operating at modulo n, where n is the number of bits per word. In this case, the counter is reset at each frame pulse, after which it continues cycling through its states, returning to its word-start position every n cycles. If it abruptly shifts or gradually drifts out of a word synchronization, the counter readjusts automatically at the start of the next frame.

Correlator-based systems can determine the time delay between two similar patterns of bits, such as a transmitted sonar or radar signal and its returned reflection. In these cases, the two signals appear similar in shape and bit pattern, but exhibit a relative time shift of 2D/V, where D is the distance between the antenna and target and V is the velocity of propagation (the speed of light in radar and of sound in sonar). Conceptually, this technique involves the shifting of one signal relative to the other so that the shifting just compensates for the time delay between the two signals.

Measuring time delay

Using the 1023J, the B register can be loaded with the original, or transmitted, signal at the same time as the A register is loaded with the delayed, return signal. The two registers are clocked together so that the time delay between the signals appears as a displacement in their relative register positions. After both registers are loaded, the output of the correlator is monitored while the A register continues to be clocked. This process loads progressively later return signal bits into register A, while shifting the delayed pattern across the underlying signal stored in register B. As a result, the number of bit shifts required for acceptable correlation multiplied by the signal's bit time yields the total time delay between the two signals.

For this system to function properly, the code must be long enough not to trigger on false correlations. For example, a code such as 10101010101 would be unsuitable for time delay measurements because all shifts of 2N bits (where N = 1, 2, 3, . . .) would yield high correlations and produce ambiguous results. In contrast, a code that repeats only once every 500 characters would be much more likely to provide an unambiguous measure for signals with a time delay of less than 500 bit times.

Nonrecurring codes

When a nonrecurring code, such as a single burst of information, is employed in a time delay measurement, the length and pattern of the transmitted code are subject to limitations. Under ideal circumstances, the only objective is to measure distance to a target, and a simple isolated pulse (a single positive bit surrounded by negatives) can be transmitted.

The returning reflection of this signal contains a similar isolated pulse, delayed by the round trip travel time between the antenna and target. However, this alignment test is relatively insensitive, having a total correlation score of 62/64 when the transmitted and received pulses are misaligned, versus 64/64 for perfect alignment. In the presence of noise or interference, the return signal can contain one or more false positives, which can reduce the perfect alignment correlation and generate other relatively high correlations.

Longer codes can be used to improve the accuracy and sensitivity of the time delay measurement. Particularly suitable are the Barker codes, which are characterized by longer correlations with time-shifted versions of themselves. Although a longer pulse code cannot improve the 64/64 correlation score for perfect time-alignment in the presence of noise, it greatly reduces the chance of a burst or random noise causing high correlation. For a given level of interference and bit errors, increasing the length of the Barker code tends to reduce the frequency and magnitude of false correlations and enhances the accuracy of the range measurement system. The Barker codes available offer suitable error rates and sensitivity for these applications.

Spitting image

To recognize periodicities or patterns, the 1023J can be used to compare a single data stream against a time-delayed replica of itself. First, the signal is loaded simultaneously into the A and B registers. Then, when the registers are full, the B register pattern is held, while the incoming signal continues to be clocked in sequentially through the A register. This simulates a steadily increasing time shift.

Periodicities in the data stream will generate high correlations, which appear periodically as the A register contents slide past the B register. These correlations and the number of bits between sequential high correlations correspond to the period of the repeating pattern. For example, the data sequence 100100100100 exhibits a high correlation for every delay of 3N bit times, when N = 1, 2, 3, . . . Although this example is obvious, there are others that are subtle and can cause system problems if they are not spotted.

Random noise can make such periodic signals harder to detect by reducing the contrast between periodic correlation peaks and the low residual correlations between them. However, a digital correlator can still identify signal periodicities in the presence of surprisingly high levels of random noise. If S(m) and S(m+n) are the original and time-shifted versions of the pure signal and N(m) and N(m+n) are the corresponding additive noise values, then the correlator performs the sum:

$$R(n) = \sum_{m=0}^{63} [S(m) + N(m) \times S(m+n) + N(m+n)]$$

where m and n are indexes representing discrete steps in time. In this example, the sum runs arbitrarily over 64 values only because this is the bit length of the 1023J.

The function being summed comprises the four terms $S(m) \times S(m+n)$, $N(m) \times N(m+n)$, $S(m) \times N(m+n)$, and $N(m) \times S(m+n)$. If the noise is truly random, it does not correlate significantly either with S or with its time-shifted self, and only $S(m) \times S(m+n)$ contributes significantly to the overall sum, R(n). However, when a short sample is considered in a noisy environment, the noise can interfere significantly, masking a pattern of periodic high and low correlations. To overcome higher noise levels, longer correlation sequences are used to increase the signal's integration gain. A single 64-bit correlator can provide up to 18 decibels ($10 \log_{10} 64$) of signal enhancement, and two units in the series can supply twice as much, or 21 dB. □

Regulator boosts supply voltage for programming EE-PROMs

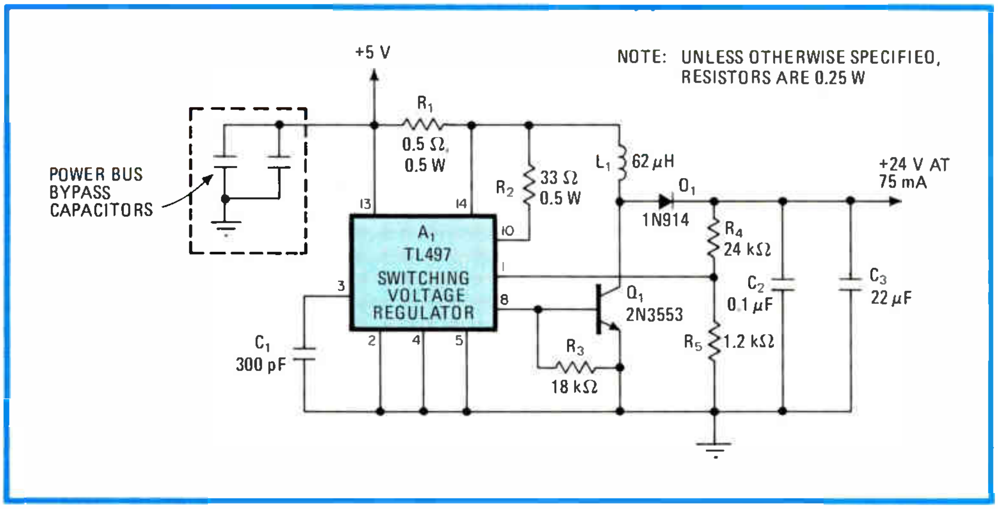
by Henry Fung and John Rizzo
Intel Corp., Special Products Division, Santa Clara, Calif.

The 2816 is a new electrically erasable programmable read-only memory in which writing and erasing can be accomplished on board by feeding a 21-volt dc pulse to the chip's V_{PP} pin. But generating the pulse requires a power supply with an output voltage of +24 V dc, which is then clamped by a zener diode to about +21 V dc. When that is not available, a switching regulator can be used to convert the commonly available +5 V dc into +24 V dc. The advent of large-scale integration technology simplifies the design of such a dc-to-dc converter. Figure 1 shows the circuit diagram for a voltage converter using a TL497 switching voltage regulator that is very inexpensive to build.

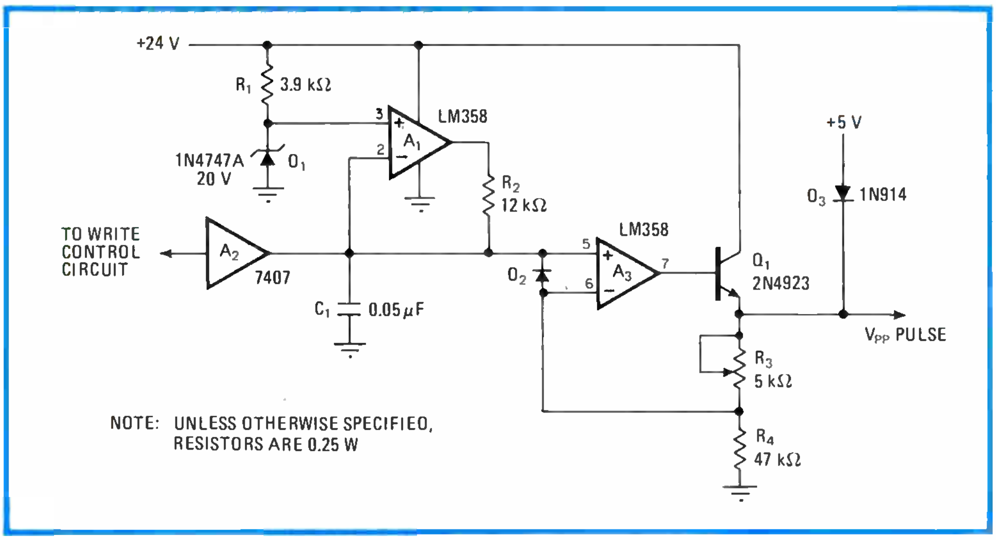
The circuit operates as follows: the frequency at which transistor Q_1 is switching is determined by capacitor C_1. The converter's output voltage is fed back to an internal comparator that controls the on and off time of Q_1. When Q_1 is turned off, the voltage across the inductor inverts, and the blocking diode, D_1, is forward-biased to provide a current path for the discharge of the inductor into the load and filter capacitors (C_2 and C_3). While Q_1 is turned on, the current into the inductor increases linearly. D_1 will then become reverse-biased and the output load current will be provided by the filter capacitors. But current output above 80 milliamperes will cause the output-voltage regulation to degrade.

The switching-regulator efficiency may be calculated as a ratio of output power to input power (including a 50% duty cycle). Therefore:

$$\text{efficiency (\%)} = \frac{\text{output power}}{\text{input power}} \times 100\%$$



1. Big boost. A dc-to-dc converter based on a TL497 switching regulator boosts a 5-V supply voltage to 24 V dc for programming electrically alterable read-only memories. Q_1 is switched at a rate determined by C_1, and the induced voltage in L_1 is the output.



2. Sensing switch. The programming voltage, V_{PP}, is applied when the output of A_2, an open collector gate, is high for 10 ms during a write cycle. C_1 charges up and ultimately turns on Q_1, which provides up to 75 mA of drive to erase or write into a memory.

$$= \frac{24\text{ V} \times 80\text{ mA}}{5\text{ V} \times 1{,}160\text{ mA} \times 0.5} \times 100\%$$
$$= 66\%$$

The output voltage from the switching regulator may now generate the V_{PP} pulse required to program the 2816 EE-PROM. The next requirement is a circuit that switches the 24 V on during write and erase cycles (Fig. 2)

D_1 suppresses any noise on the 24-V line and clamps the line at about 21 V. A_2 is an open-collector gate and when its output is low, C_1 and pin 5 of A_3 will be shorted to ground. Therefore, Q_1 will be turned off and the V_{PP} pulse will stay at a level equal to the 5-V supply voltage less one diode drop. When a write cycle is initiated, the output of gate A_2 will be high for 10 milliseconds, allowing C_1 to charge. The time constant, determined by R_2 and C_1, is 600 microseconds. As soon as the capacitor is charged up to the zener diode voltage, the feedback amplifier will force this voltage to remain constant. The final output voltage is adjusted by R_3. Q_1 provides the additional current-drive capability up to 75 mA. Diode D_2 across pins 5 and 6 of A_3 ensures a V_{PP} pulse that will be glitchless.

The 2816 has an inhibit mode that allows the device to be deselected during programming. Consequently, only one switch is needed for many devices in a system. However, the V_{PP} switch must still supply the I_{PP} standby current for the unselected devices.

The circuit has been tested over the 2816's full operating temperature range. □

Pulse-width monitor flags poor timing

by T. G. Barnett and J. K. Stothers, *Neonatal Research Group, London Hospital Medical College, London, England*

Pulse intervals can be monitored to ensure they fall within a specified range by using two complementary-MOS 4098 dual monostable multivibrators. The original application of this circuit was to monitor biologically produced pulse trains. However, the principle can be applied to any case where it is necessary to know if the limits of a pulse interval have been exceeded.

The 4098 is two independent one-shots in a single package and each one-shot has leading- and trailing-edge triggering, retriggerable and nonretriggerable modes as well as a reset and complementary outputs. These facilities have been incorporated within a monitor that senses whether a pulse train has intervals longer or shorter than those of a chosen range.

The period of each one-shot may be obtained from its data sheet or approximated by:

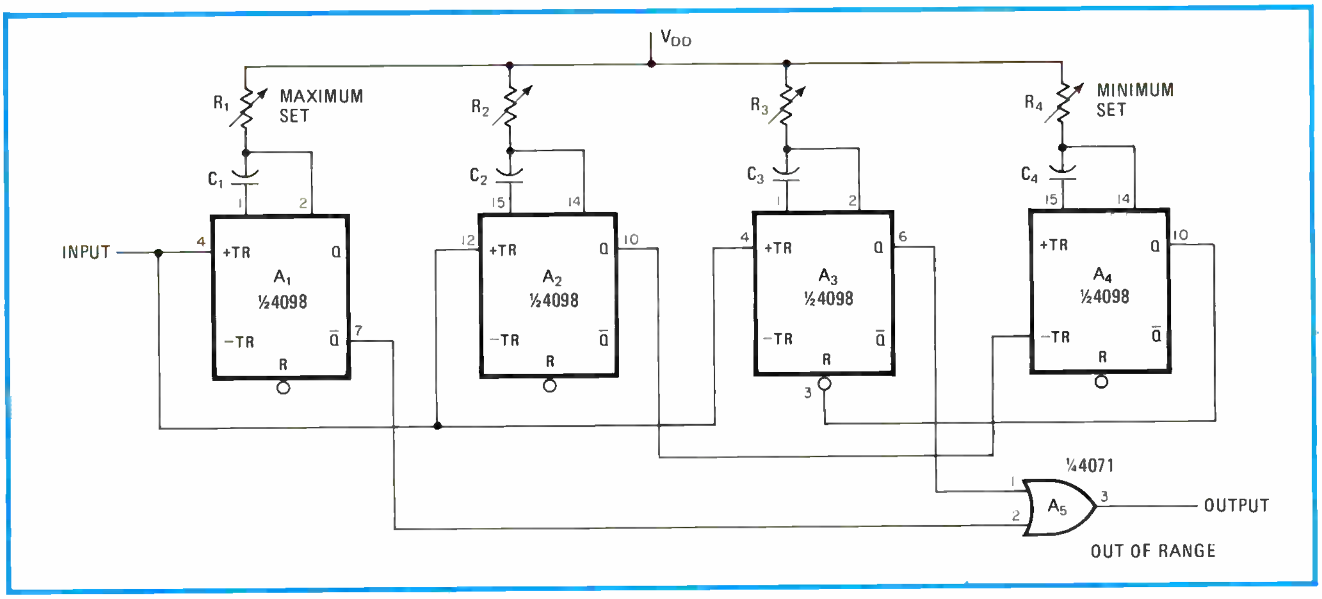
$$T(\text{time}) = 0.5 \times RC$$

for values of $C \geq 0.01$ microfarad.

The value of the capacitor should be as small as possible and the resistor should not be more than 10 megohms. All unused inputs must be connected to either the drain- or source-supply voltage in accordance with the data-sheet instructions.

As the circuit in the figure shows, monostable A_1, operated in the retriggerable mode, is triggered on the leading edge of an input pulse. The $\bar{Q}$ output is normally low unless the input-pulse interval is greater than the duration of the monostable's pulse-width value, set by resistor R_1 and capacitor C_1. If the pulse interval exceeds this value, then $\bar{Q}$ will go high, resulting in the output of the 4071 OR gate going high. Thus the maximum interval time is set by this monostable.

The leading edge of the input pulse also triggers monostables A_2 and A_3, both of which are operated in



1. Watching it. Out-of-bounds time intervals between a train of pulses are detected at OR gate A_5 because one-shot A_1 stays triggered unless the time between pulses is too great. Meanwhile one-shot A_3 triggers if it receives successive pulses too soon. It also drives the OR gate

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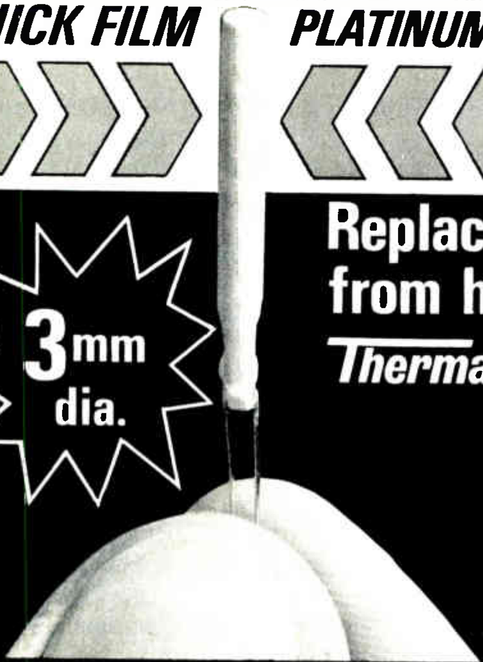

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the retriggerable mode. Output Q of A_2 acts as a delay and is fed into the trailing-edge-trigger input of A_4, whose Q output drives the reset pin of A_3. The delay that is caused by A_2 is a few microseconds and prevents A_3 from being triggered on receipt of the leading edge of the input pulse, as its reset pin is low until A_4 is triggered. A_4 is operated in the nonretriggerable mode and sets the minimum-pulse-interval time.

The Q output of A_3 will go high only if its reset pin is set high by A_4, whose Q output will go high only a short time after A_3 has received a trigger pulse. However, if a further input pulse is received within the time the Q output of monostable A_4 is high, then monostable A_3 will be triggered, its Q output will go high, and the 4071 OR gate will go high. The actual pulse width of A_3, set by R_3 and C_3, can be chosen to suit any application. □

Electronic lock boasts low cost and low power

by B. J. Sokol
London, England

Three integrated circuits, two switches, and a few diodes are all that is really needed to build a very low-power programmable combination lock, the circuit for which is shown in the figure. The combination is entered by pressing two push-button switches or, alternatively, toggling a lever-action telephone-type switch in the correct sequence. If the switches are pressed in the wrong sequence or if the user hesitates for more than 200 milliseconds while entering the combination, the 4017 counter resets and the sequence must be reentered.

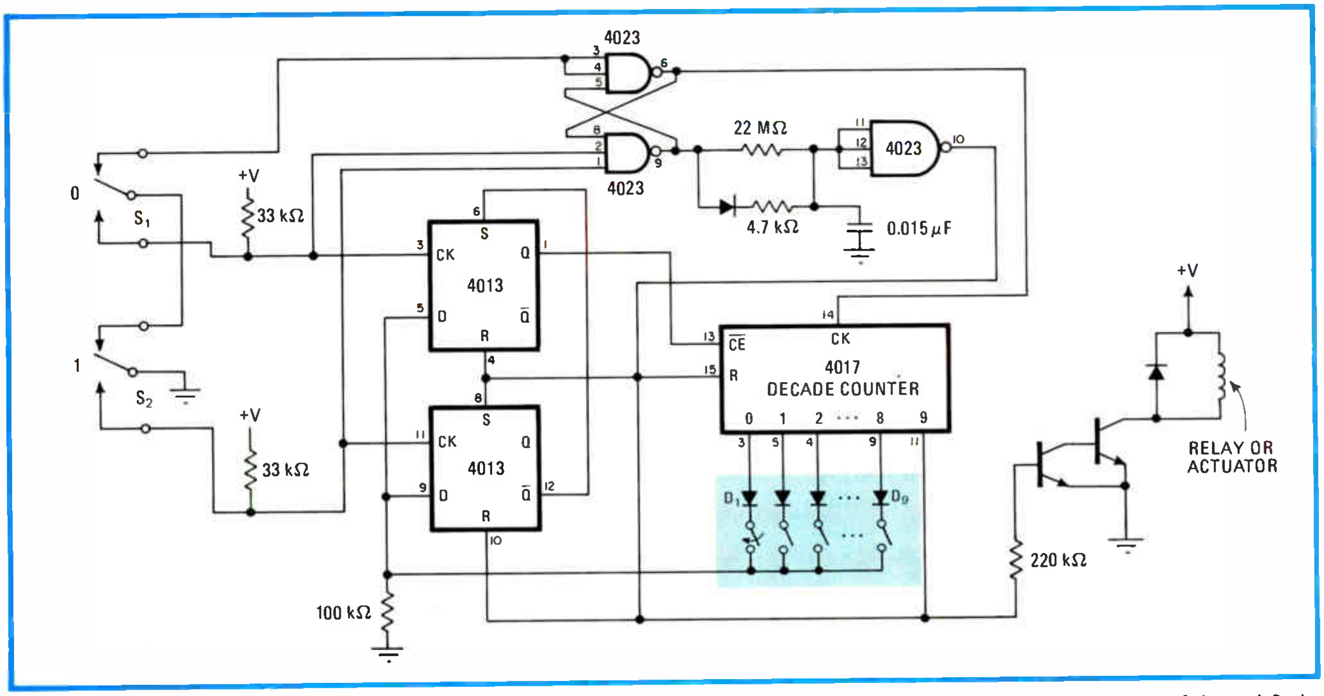
The sequence is programmed by switching a diode in or out between the 4017 count outputs and the 4013 dual flip-flop data inputs. For every diode placed at a counter output, a logic 1 is required at a corresponding point in the switching sequence. For example, if a diode is placed at the counter's 0 output but not at the others, the only combination enabling the relay or actuator to open the lock would be 1-0-0-0-0-0-0-0-0.

After the correct sequence is entered, further switch depressions are ignored because the 4017 $\overline{CE}$ inhibit line is forced high through the action on the reset and set pins of the 4013. However, after about a quarter second, the reset of the 4017 is actuated. This reset is inhibited if either push-button switch is held down—a feature allowing an extended pulse to be applied to an actuator, such as a solenoid-driven door latch.

When the switches are not operated, only a minute amount of power is drawn, most of it by the 100-kilohm pull-down resistor. As this lock will work with very little power, it is ideal for battery-powered applications.

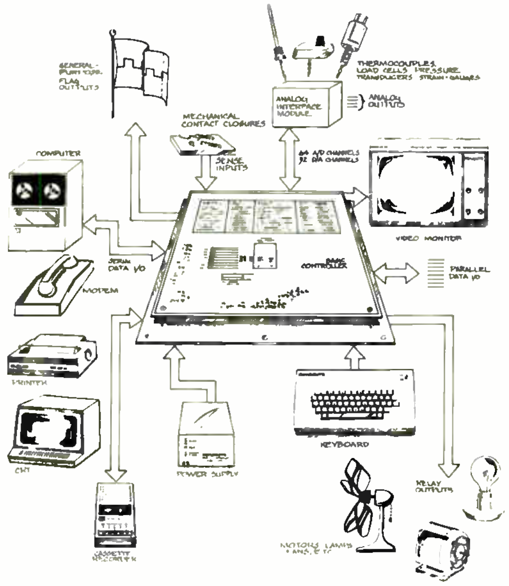
For security, no connection of wires to the switches can trip the lock. Shorter combinations are possible if the connection to the counter's 9 output is moved instead to another output. More than 512 different combinations are possible so anyone attempting to try all combinations would require waiting for a reset in every wrong instance—a process requiring considerable time and trouble. This lock provides reasonable security and an easily remembered code, especially if the user knows octal or hexadecimal notation. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $75 for each item published.



Secret. A few components is all that it takes to put together this low-power combination lock. A nine-number sequence of 1s and 0s is clocked by two switches, S_1 and S_2, and must correspond to the combination programmed by diodes D_1 to D_9, shown in the shaded area.

INSTANT REAL-TIME CONTROL



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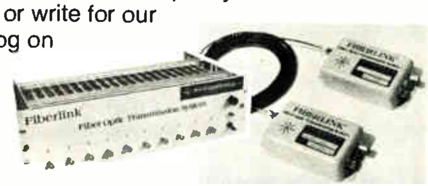

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High-voltage GTO thyristors streamline power-switching circuits

Advanced processing produces gate-turn-off devices with high yields as well as high reliability

by Arthur Woodworth, *NV Philips, Power Semiconductor Division, Stockport, UK*

☐ High-power, high-frequency switching is beyond the reach of most power semiconductors, even vertical-MOS field-effect transistors. Yet the number of applications in which high voltages as well as high currents must be switched is on the rise—for instance, in preventing line pollution due to phase control or in switch-mode systems and in TV horizontal deflection circuits.

A new gate-turn-off thyristor supplies this need. Its use of 5-volt, 200-milliampere drive circuitry makes it especially appealing for use with microprocessors. Moreover, up-to-the-minute processing and circuit-design techniques enable it to be produced in volume with high yields and hence microprocessor-compatible prices—$2 each in quantities of 10,000 or more.

Unlike other thyristors, GTOs not only switch on fast but also switch off fast. Unlike bipolar transistors, they can handle current surges and high voltages without burning out, yet their switching speed is comparable and their drive circuitry about as simple.

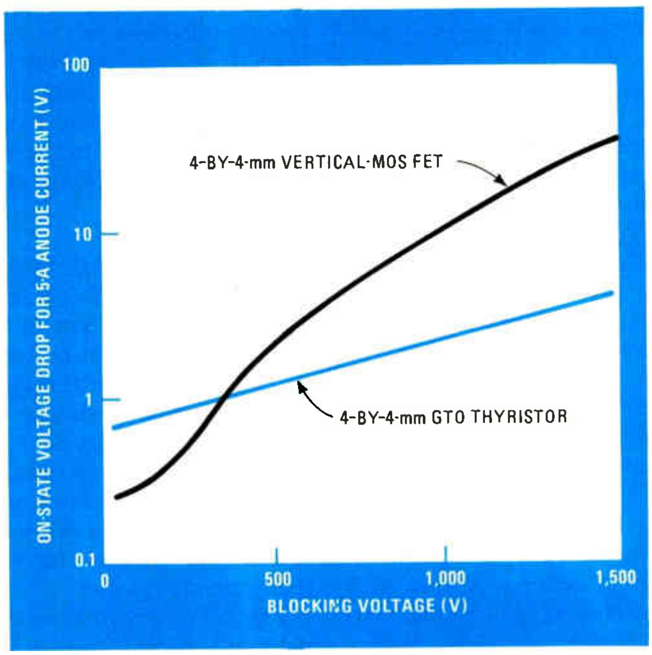
The GTO's nearest competitor is the V-MOS FET, which switches much faster and requires only a low drive current. But unless expensively large, V-MOS FETs have a much higher on-resistance, in the region of several ohms, at voltages above 400 V.

As in other thyristors, the GTO structure is filled with minority carriers of both polarities in the on state. Since both electrons and holes participate in conduction, a thyristor allows a high current density with a relatively low voltage drop, as compared to MOS devices. For example, a 4-millimeter-square, 1,500-V GTO thyristor such as the new BTW58 passes 5 amperes with about a 3-V drop, whereas a V-MOS device of the same size and voltage rating would drop around 30 V (Fig. 1). On-state power dissipation is proportional to the on-resistance, which for the MOS devices follows a power-law dependence on the designed blocking voltage. In this example, the on-state power dissipation is prohibitively high—around 150 watts.

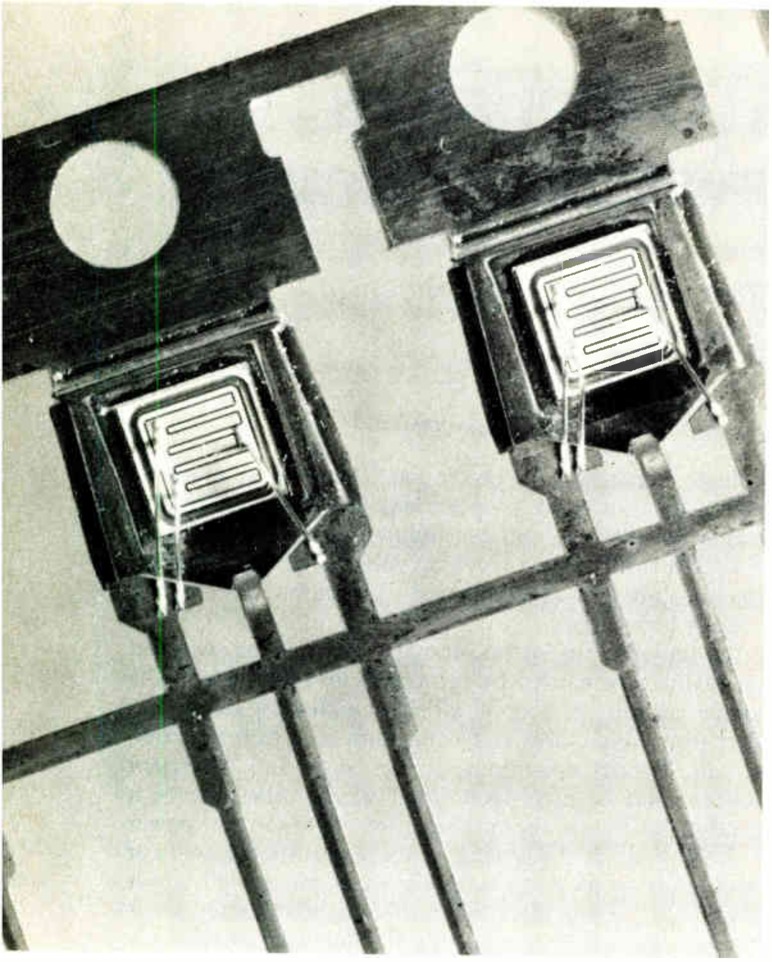
As for other thyristors, though they can be switched on easily, they cannot be turned off using the gate. The anode current is forced off by employing additional thyristors, inductors, and capacitors in a commutation circuit. Forced commutation is a slow and inefficient process that detracts from what would otherwise be a good solution to the problem of high-voltage power switching. Since the GTO thyristor avoids the necessity of commutation circuits without sacrificing high-power capability, it can block high voltages and switch large currents at frequencies up to a few hundred kilohertz—comparable to bipolar transistor speeds.

The GTO thyristor is an npnp structure that can be analyzed in terms of merged npn and pnp transistors with common-base current gains of α_n and α_p. Gate current injected into the center p-type region—or base—drives the npn device; this current multiplied by the gain of the npn device drives the pnp transistor, where it is multiplied by this device's gain and fed back to the npn unit—and so on, in a regenerative loop.

The transistor current gains are small at low currents, so a certain minimum anode current must be established through the device before the positive feedback condition is met. This minimum defines the gate turn-on current. Once the anode current is such that $\alpha_n + \alpha_p > 1$, the device latches and the gate cur-



1. High voltage. On-state voltage drop of V-MOS power transistors forbids high-voltage ratings in a small chip, while GTO thyristors can block 1 kV with tolerable on-state losses. Voltage drop is lower because both electrons and holes carry current.



2. Small and rugged. Philips BTW58—a 5-A GTO thyristor—fits on a 4-by-4-mm chip. The interdigitated gate pattern visible in this cut-away view contributes to the gate–turn-off capability and lowers the gate's resistance. The small TO-220 package keeps costs down.

rent can be removed without losing conduction.

In other thyristors, $\alpha_n + \alpha_p$ is made as large as possible to reduce the on-state voltage drop and the turn-on current. Because of the high gain, it is impossible for the available gate current to halt conduction; switching a larger gate current requires the additional turn-off circuitry that has to employ other thyristors as well as passive components.

With GTO thyristors, current gains are controlled so precisely that their sum only slightly exceeds unity. The gate current required to switch off the device can then be provided by a simple drive circuit. In the case of the BTW device, advanced processing techniques and strict process monitoring achieve the necessary control over these crucial device parameters.

Precision processing

Recent advances in device processing permit such tight control of the thyristor current gains that GTO devices are now being produced with high yields. Before processing begins, computer modeling of the device's switching behavior establishes the optimal current gains for the component transistors, for it is on the careful balancing of the npn and pnp transistors' current gains that GTO thyristor reliability depends.

To achieve this balance in practice, proper doping profiles must be obtained. Neutron doping of the starting ingots adjusts the background resistivity to within a narrow window, so that subsequent ion implantation of the wafers sliced from it will consistently produce the required profiles.

Finally, glass passivation of power-switching chips is essential to their stable, high-voltage performance at high temperatures. By incorporating techniques similar to those used on triacs and thyristors, GTOs are being produced with a mean time before failure of more than 100,000 hours.

Fast switching

Careful processing also minimizes the GTO thyristor's turn-off time within the constraints of the desired blocking voltage, current density, and on-state resistance. The turn-off time has two components: the storage time and the fall time. In the storage phase, the conducting channel is squeezed down to a narrow filament connecting anode and cathode.

Two strategies minimize this delay. First, the cathode is formed as a pattern of long narrow fingers over the gate region, giving a low-resistance path out of the p base (Fig. 2). Fine-line photolithography is required to produce this interdigitated pattern, which allows the gate to exert strong control over the anode current, enhancing the gate–turn-off capability. Second, the cathode-gate junction is made to withstand 10 V or more before breakdown, since a larger applied field during turn-off allows larger anode currents to be turned off. The optimal base doping level is dictated by the tradeoff between low resistance and high breakdown voltage.

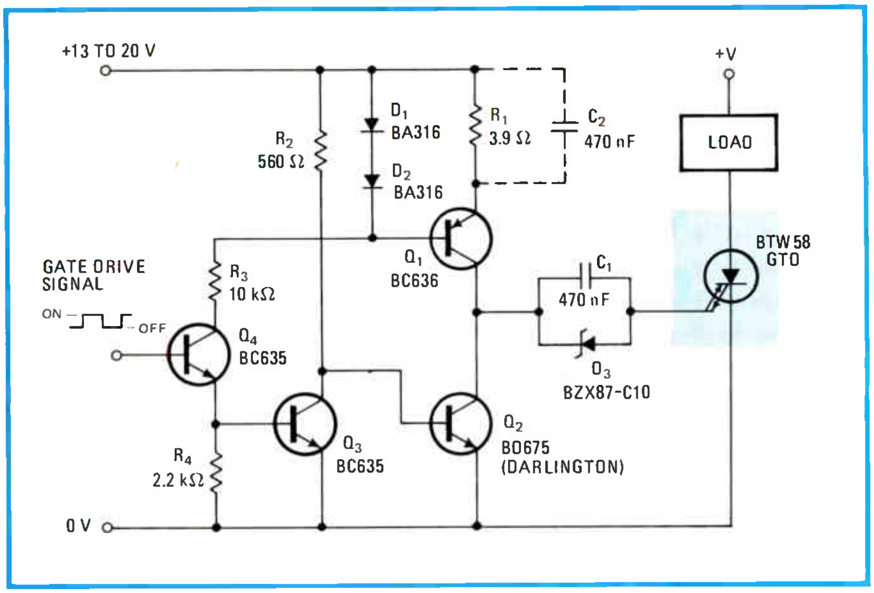
When the filament joining cathode and anode breaks, the device current falls and the anode voltage rises at a rate that depends on the load. This is the start of the fall time. It is minimized by providing shorts between the anode and the pnp transistor's n-type base. This internal base, which otherwise has no direct connection to the outside, is shorted to the anode by masking the boron-diffused region under the cathode fingers.

Drive circuit

The anode current fall time depends heavily on the size of the turn-off current supplied to the gate of the device. A gate current of 1 A on the BTW58 turns off 5 A of anode current in less than 1 μs. If the drive signal pulls the gate down through such a low impedance that the gate current instantly equals the anode current, the fall time is typically 100 ns—comparable to a bipolar transistor's switching time. In this unity-gain mode, the device can tolerate rates of change of the anode voltage of up to 10 kV/μs without spurious turn-on, thereby eliminating the need for snubbing networks along with their attendant losses.

Figure 3 shows a drive circuit for the BTW58. Transistors Q_1 and Q_2 form a high-current push-pull output stage driven by Q_3 and Q_4. A positive gate signal at the base of Q_4 turns on current source Q_1, which turns on the GTO via capacitor C_1. In turning off, Q_2 sinks a large current from the thyristor gate, rapidly halting conduc-

3. GTO driver. Unique gate-turn-off capability allows a single drive circuit to switch a GTO thyristor on and off. The need for extra commutation circuitry is eliminated, boosting speed and lowering parts count.



tion. Capacitor C_2 is included to reduce turn-on losses when the rate of change of the anode current is high.

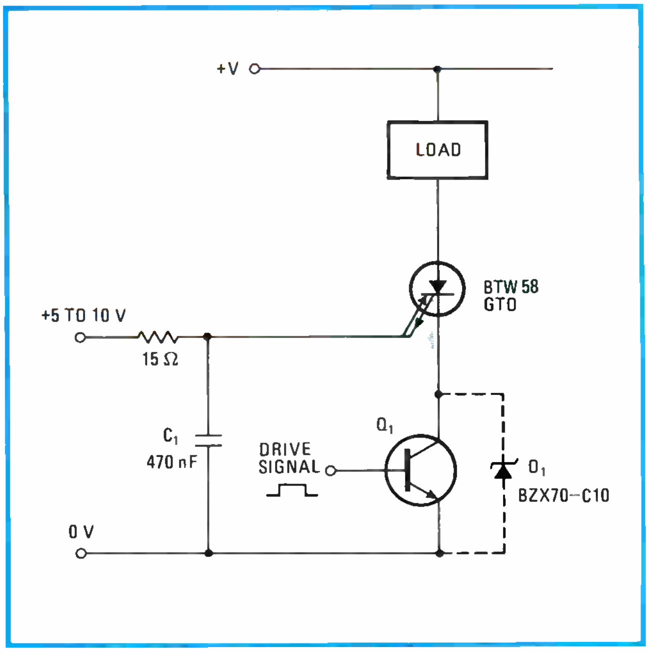
An even simpler unity-gain drive circuit uses a variation of the well-known cascode configuration (Fig. 4). When Q_1 is turned off, the anode current is forced to leave the device through the gate, charging C_1. The GTO blocks the high voltage, but the drive requirements and switching speed are largely determined by Q_1, which may be a low-voltage bipolar or MOS transistor. A zener diode is included to protect Q_1 from high voltages.

Other possible gating circuits include transformer drives and switching to a negative supply line. In all cases, a properly driven GTO thyristor offers the circuit designer the usual advantages of thyristor switches—high voltage blocking and high current in a small and reliable device—plus the added advantages of gate-turn-off capability: low drive power, simple drive circuits, and switching speeds of 100 kHz and more.

Line pollution

The number of applications requiring high-voltage switching of large currents at high frequencies is increasing. A full-wave ac controller using a single GTO thyristor reduces the line pollution for which phase controllers are notorious. Such a chopper controller selects portions of the ac waveform to deliver a higher power factor and lower harmonic content to the load. In addition, it can work as a fast-acting trip to turn off the load at any point in the cycle.

Most switching power systems use diode-capacitor input circuits, which also pollute the ac line. Under threats of legislation, engineers throughout Europe are looking for ways to design converters with low harmonic content and low radio-frequency interference. Resonant systems, such as the series resonant inverter, show the most promise. In such a resonant circuit, the switch must withstand several times the line voltage—something a GTO thyristor is well able to do. Another familiar resonant circuit is found in TV horizontal deflection controllers. The BTW58 can handle 1,500 V of flyback voltage, and its small size and low drive power requirements make it a viable alternative to existing solutions.



4. Cascode drive. A simple GTO drive circuit uses a power transistor in series with the thyristor. Although the GTO blocks the high voltage, switching speed and drive power are set by Q_1. A zener diode protects the low-voltage cascode drive transistor.

The speed of three-phase induction motors can be controlled from a variable-frequency three-phase pulse-width-modulated inverter. The choice of power switches for such an application has, in the past, been between relatively expensive high-voltage bipolar transistors and thyristors. Although themselves inexpensive, thyristors required other components for switching off. But, since the GTO thyristor can be turned off with the same drive circuit that turns it on, these power switches are now more economical than bipolar transistors in many applications. Furthermore, they show excellent promise of scaling up to higher current levels, since the die sizes are relatively small at the present 5-A current level. □

Design automation speeds through customization of logic arrays

With high-level languages describing and testing hardware, manual processes make up less than 1% of the design cycle

by Richard Horton, David Thomas, and Robert Rozeboom, *Texas Instruments Inc., Dallas, Texas*

☐ Between the poles of low-cost standard integrated circuits and expensive custom chips there now stands a brood of logic and gate arrays. But despite the various claims being made about them, these devices all present the same basic question: how to connect the output of each gate in the array to the input of the next? Because the answer is by an extremely complex maze of on-chip wiring chosen from a seemingly endless list of routing patterns, help from a computer in laying out the connections is more than a convenience; it is mandatory. Recently, a pair of logic arrays were introduced that are in marked contrast to other arrays in that they are accompanied by a full supply of automated design tools [*Electronics*, Jan. 13, 1981, p. 41].

Logic equations and test algorithms for the arrays are expressed in their own high-level languages, and together these run an in-place design automation system that delivers a mask set and test tapes. Manual intervention—which dominates some array design schemes—constitutes less than 1% of the input to the system for the parts, dubbed TAT arrays.

A pair of parts

The first two TAT arrays are the TAT008, containing 1,008 internal gates with 104 inputs and up to 52 outputs; and the TAT004, which has 540 internal gates, accepts 76 inputs, and drives 38 outputs. Optional features for either include inverting or noninverting input buffers and three-state totem-pole or open-collector output drivers. Both use eight bonding pads for power. Based on high-performance Schottky-transistor-logic (STL) technology (see "Superintegration yields a small, fast gate," opposite), TAT gates feature a basic delay time of 2.5 nanoseconds for an 80-megahertz toggle rate and dissipate 600 microwatts.

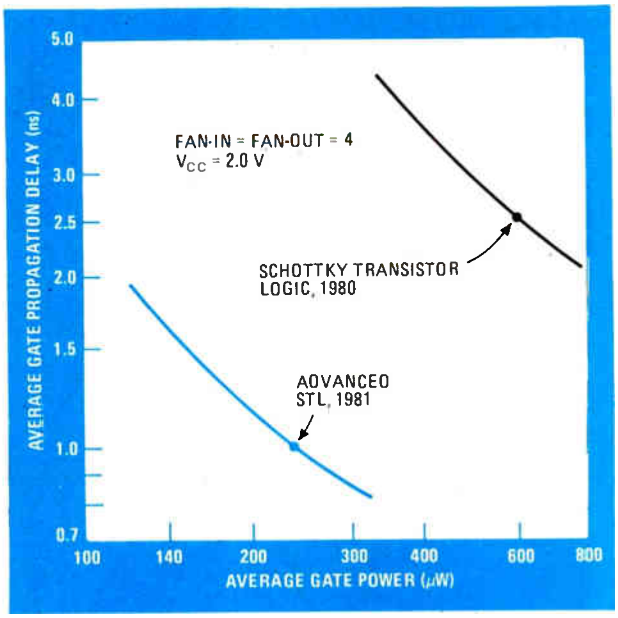
Packaging options include dual in-line plastic and ceramic styles with 24, 28, or 40 pins. In addition, the ceramic housing offers 48 and 64 contacts. Also available are 68- or 84-pin ceramic chip-carriers that conform to the standards of the Joint Electron Device Engineering Council.

An important characteristic of TAT chips is their stability over a wide temperature range. The typical delay of about 2.5 ns changes by just 5% over the operating temperature range of 0° to +70°C. Even over the much wider range of −55° to +125°C, propagation delay shows only a slight variation for a given base drive. There is, however, a minor decrease in both gate speed and power dissipation at high temperatures, because the array's internal resistive elements have a positive temperature coefficient.

On the TAT008, the typical gate utilization rate is 80%. Although it appears inefficient to have 200 gates go unused, they are available should it become necessary to upgrade the chip with additional functions. And since the arrays are mask-programmable, adding new functions usually means only minor modifications to a small number of original masks.

Also influencing propagation delay is the lead length used to connect the gates. Delay gradually increases from just over 2 ns with short interconnections to about 5 ns when on-chip wires exceed 200 mils in length. To

Superintegration yields a small, fast gate



At first glance, the Schottky-transistor-logic (STL) inverter gate that serves as the primitive element in the TAT series of logic arrays resembles conventional, high-speed Schottky logic. But closer inspection reveals a group of blocking or coupling diodes connected to the collector of the switching transistor, and those diodes make the STL gate unique (see figure, lower left). Even so, the diodes, npn switching transistor, and resistors can be integrated into a very compact, single-transistor structure using standard buried-collector junction-isolated bipolar technology.

In a single-transistor STL device, the usual platinum silicide Schottky diode connected between the base and the collector acts as a current shunt. It diverts excess base-drive current away from the transistor's input to prevent forward biasing of the base-collector junction, and that keeps the device out of saturation. That diode and the fact that the logic-signal swing is small—200 millivolts—account for STL's high speed. Helping to conserve power is the low, 2-volt supply voltage used with STL arrays.

As shown in the curve (upper right) of gate power versus propagation delay, a typical delay time for STL logic is 2.5 nanoseconds at a power dissipation of 600 microwatts. A more advanced gate element, scheduled to be introduced late this year, is even faster and less power-hungry, as the curve illustrates.

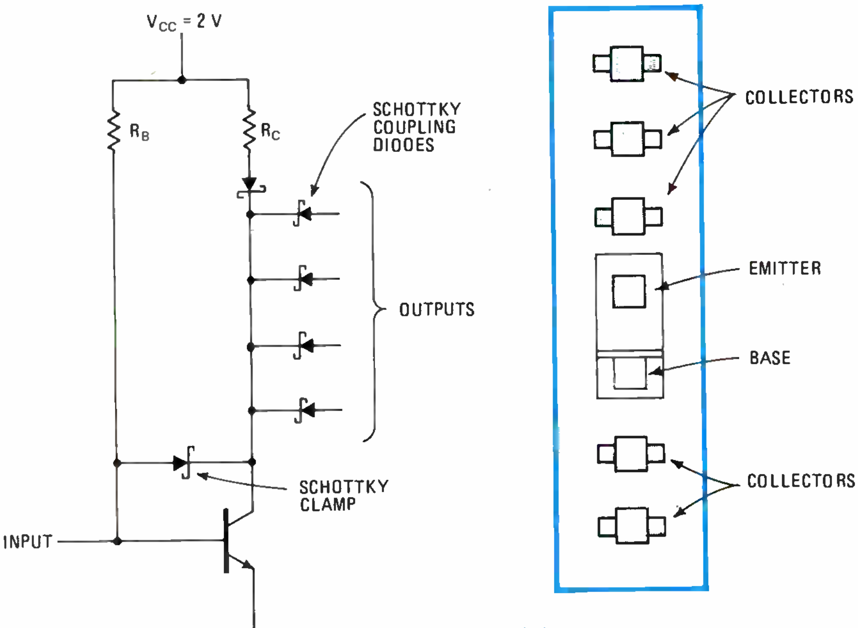
The output diodes, also Schottky types, perform a function similar to that of the input blocking diodes in diode-transistor logic (DTL) or the multiple-emitter input structure in TTL. These diodes make possible the wired-AND logic operation of the inverter, allowing Boolean functions to be implemented by simply connecting one gate's outputs to the following gate's inputs. The small logic swings are conserved because of the low, 0.3-V forward voltage drop of a Schottky diode—a far cry from the 0.7- to 1.2-V diode drops found in older logic families.

The output voltage swing of the STL device depends on the barrier-voltage heights of the two different types of Schottky diodes. The clamp diode is a high-barrier type, whereas the output diodes are low-barrier devices. If the array transistors have equal base-emitter voltage drops, it can be shown that the two Schottky-barrier voltages cannot also be the same. If that were the case, no switching would be possible and the device would not perform as a gate.

However, the diodes must be matched to ensure their tracking with temperature. In addition, for high-temperature operation and to guarantee a high fan-in, both the forward voltages and the reverse leakage characteristics of the Schottky diodes must be precisely controlled.

Besides their inherently high packing density, STL gates are laid out with vertical stick geometry that permits all gate elements to be aligned on a common axis. The benefit is the extremely simple connection of logic elements.

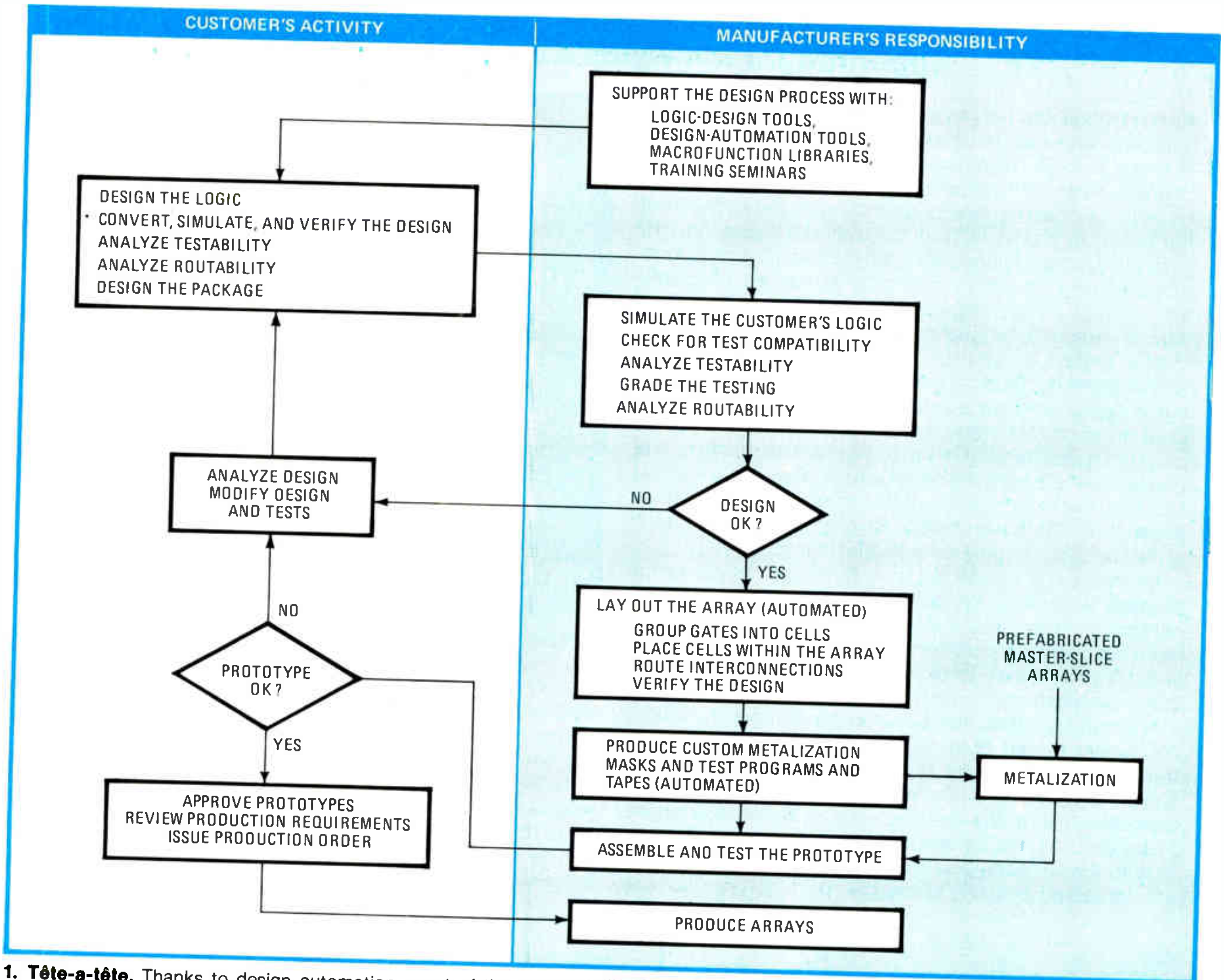
Because of its inverted structure and wired-AND logic configuration, a direct physical correlation exists between the logic diagram of a system and the STL base inputs and collector-diode outputs used to represent it.



(a) (b)

minimize the delays associated with longer wiring runs, computerized automatic layout and routing techniques are used so that critical paths can be predefined to optimize system performance.

In fact, virtually every step of the design process is computerized—manual processes constitute less than 1% of the cycle, as mentioned before. Written in a computer-readable hardware-description language, called HDL,



1. Tête-a-tête. Thanks to design automation, most of the responsibility for gate-array design rests with the manufacturer. The customer converts a system's circuitry into a logical description, but layout, analysis, and tooling are controlled by software.

logic and macrofunction definitions are sent to users, who return final logic descriptions. A second language, called TDL, for test-description language, facilitates the creation of complex text conditions to check out a design before production.

Fully automated

Both HDL and TDL drive an internal design system that automatically produces customized metalization masks and test tapes for the logic arrays. The result is logic devices better able to meet functional and performance requirements than error-prone custom chips, which must be processed from scratch.

The automated design is a two-step process. First, the user describes the structure and behavior of a logic design in high-level HDL, along with its stimulus and response characteristics. Then, the manufacturer verifies that the user's solution is correct, physically maps the data base into coordinates on silicon, and generates an interconnection pattern.

Unlike most logic-array design schemes, this system is said to be design-automated rather than computer-aided. The difference is significant. A computer-aided design system typically assists in routing 90% of an array's interconnections, but that means that if the array contains 2,000 runs, 1,800 are laid out by computer and 200 must still be placed manually. However, a person would experience tremendous difficulty in laying out 200 wires once the computer had generated a complex maze in laying out the first 1,800. Chances are that the designer would have to adjust the computer-generated interconnection in order to complete the task.

But since with design automation, in contrast, the human operator typically completes only 1% of the layout, or 20 wires, that level of complexity can be handled easily. Moreover, the computer will verify the entire layout, including the human input.

Electronic communications

Since the design automation system is oriented entirely toward software, customer-to-manufacturer dealings can be completely electronic: communication is done by means of a dedicated-line network of data handling in the form of remote job entry, a batch-processing technique. The system adheres to the IBM 3780 protocol, so that anyone with access to IBM-compatible equipment can go on line without any problems.

Besides HDL, other programs are available to simulate and verify the design and to analyze its testability and routability. The last program determines how well internal nodes can be controlled and monitored and also verifies that the design rules have not been violated. A completed design file is then submitted for verification. Once the file has been verified, circuit functions are automatically partitioned, placed, and routed on the chip. The company will also fabricate, assemble, and test 20 prototype parts to the user's specifications. Upon acceptance of the prototypes, full-scale production of the logic arrays commences. Figure 1 illustrates the entire customer-manufacturer interface.

Fewer interconnections

The greater the number of functions that can be placed on a single logic chip, the better the system will perform. The reason is that, in most cases, more than 50% of overall system performance is tied up in the interconnections. Logic arrays remove the wiring from printed-circuit boards and backplanes and integrate it into chips, thereby speeding signal propagation.

For example, with MSI logic families—which are still in widespread use—signals must first pass through input buffers that are very slow compared with internal gates. The signal may proceed through three or four levels of gating on the chip before passing through an output buffer. Input and output buffers usually delay a signal three to five times more than an internal gate because they interface with a much higher-capacitance environment. In addition, the signal may run through an IC socket, pc-board cladding, backplane wiring, and an edge connector.

In comparison, each gate of an STL logic array introduces between 2 and 3 ns of delay, and each input/output pair about 10 ns. That makes the logic array approximately two to three times faster than low-power Schottky MSI logic. Moreover, the logic array will consume less power, resulting in a more efficient and more reliable system.

In the initial stage of a logic-array design, the designer must find out if the system can be integrated in a single array or if it will require multiple chips. The packaging constraints of the array must be looked at in terms of the number of I/O pins and buffers.

Taking the first step

The first step is to seek a partitioning of the customer's logic network, particularly when the proposed system appears too large for a single array. This partitioning is used to minimize both the number of gate arrays and the interface between them. There are three different techniques for partitioning digital logic: vertical, horizontal, and functional.

With vertical partitioning, many logic functions are assigned to each signal pin, and the design is characterized by a subdivision into a small number of bits. For example, an 8-bit microprocessor would be partitioned into two 4-bit slices.

Horizontal partitioning is just the opposite of vertical in that a small number of logic functions is assigned to each bit, but the partitioned network handles a large number of bits. Horizontal partitioning would leave the 8-bit microprocessor's data path 8 bits wide through the first half of the device and use the other half to implement an arithmetic and logic unit (ALU), an accumulator register, or an output multiplexer.

Because these functional blocks impose high time-delay penalties, broader word widths produce higher system throughputs. As a result, this form requires a large number of signal pins on the array. In addition, a large number of array patterns is needed to implement the system, since fewer functions are built per pattern.

With functional partitioning, specific tasks are assigned to different parts of the network. For example, a logic network that handles both data and address flow would be divided into two subnetworks, one for each. Any network can be partitioned into manageable subnetworks and further reduced to logic gates, but for large networks, that requires a tremendous amount of time and energy.

MACROFUNCTION DESCRIPTION PROGRAM

```
'BLOCK' BLOCKNAME ((ATTRIBUTE));
   SIGNAL LIST
'STRUCTURE'
   LIST OF COMPONENTS AND INTERCONNECTION
'BEHAVIOR'
   DESCRIPTION OF BEHAVIOR
'TIMING'
   DOCUMENTATION OF DESIGN CONSTRAINTS FOR TIMING
'ENVIRONMENT'
   GENERAL DESIGN DATA AND CONSTRAINTS
'END' ((BLOCKNAME));
```

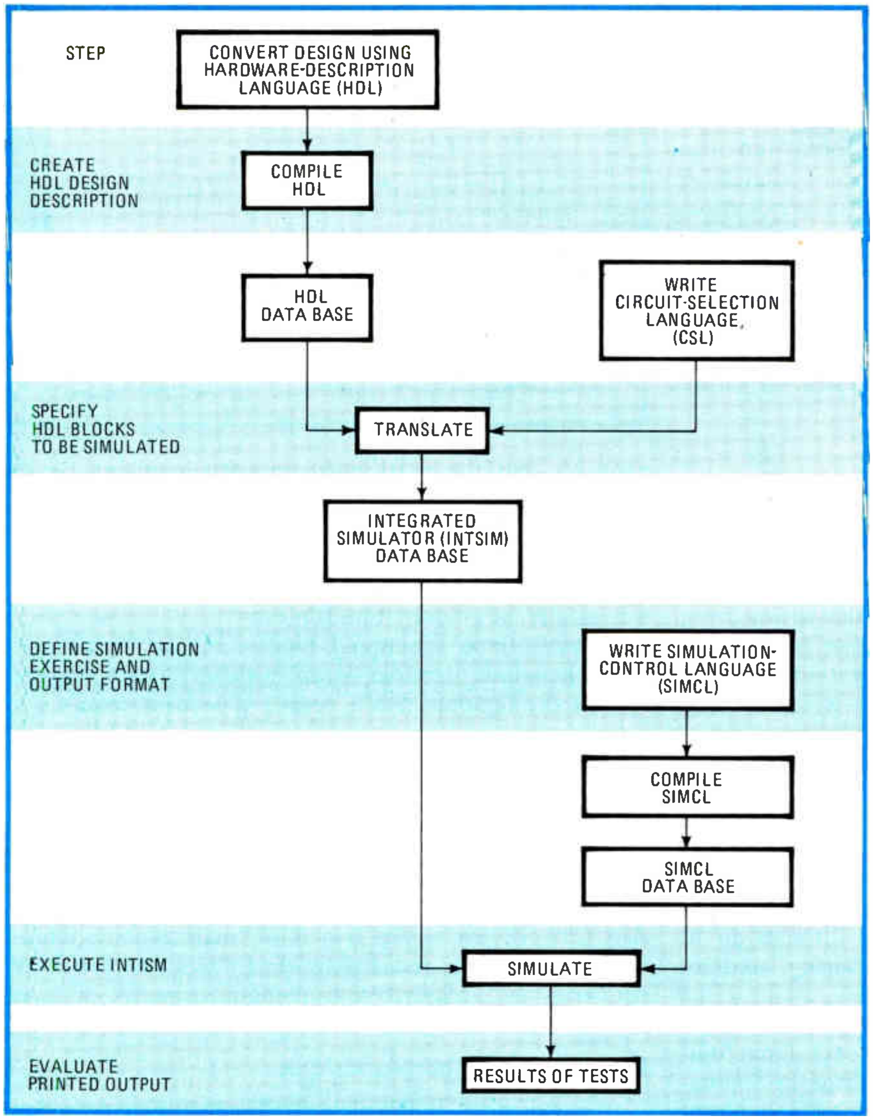
Building with macrofunctions

HDL expedites functional partitioning with precoded software macrofunctions. These digital building blocks can be any circuit element that the designer finds convenient. A macrofunction can be as small as a simple gate; it can be a function such as an adder, counter, or multiplexer; or it can be as large as an entire 4-bit large-scale integrated processing element like the 74LS481. These blocks may be used as if they were actual intergrated circuits, but they are better than real ICs, since they can be modified to conform to specific circuit requirements.

The HDL library contains about 100 macrofunctions in all, 70 of which are equivalent to conventional low-power Schottky functions. The other 30 are unique functions implemented with the STL wired-AND logic used in TAT logic arrays. These include simple gates, data selectors, and encoders, as well as special modules for diagnostics and circuit testing.

Macrofunctions are specified in HDL using a block description (see program, above). As a minimum, the block must include a statement that names the block, a signal list that describes the interface of the block with its environment, and an end statement to terminate the description of the block.

The first block in HDL source code must be a design



2. Flow simulation. After representing an application in the hardware-description language, HDL, a circuit-selection language, CSL, is used to specify which parts of the system will be simulated. The simulator is driven by a control language, SIMCL.

block. It functions as a physical breadboard would by describing the interconnection of the parts that make up the design. So-called generic blocks are the most frequently used components in HDL—they are, in fact, responsible for the language's building-block feature. Generic components are described once; after that, they can be used throughout the design by referring to the generic description. Any component or circuit can be declared generic.

Because macrofunctions are modular, an entire network can be built by expanding a number of modules vertically or horizontally. For example, to design a fast 16-bit look-ahead adder, the 4-bit look-ahead adder macrofunction—ADD4T—is cascaded four times with one look-ahead generator macrofunction called CGEN4T. Exploiting this technique eliminates the need for complex switching expressions or output flow tables.

Given the complexity of logic arrays, the design process is not complete until the network is thoroughly tested. The integrated simulator, or Intsim, performs logical and functional simulation for the TAT gate arrays. This program allows users to evaluate the response of a design to input signal patterns, to make timing analyses, and to verify test patterns.

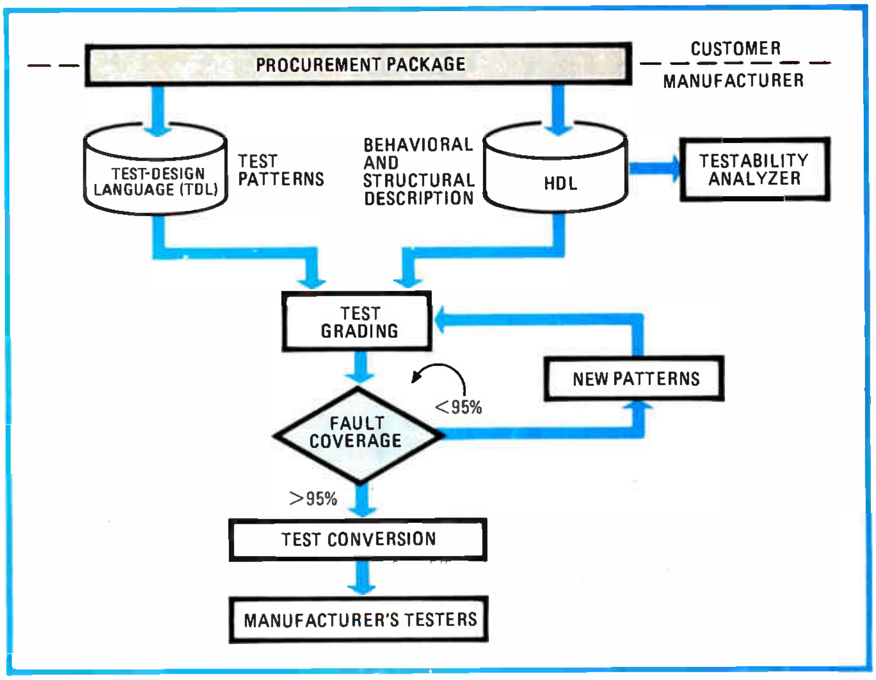
Figure 2 illustrates the process of design simulation in the gate-array system. The designer creates an HDL representation of the application and uses a circuit-selection language, CSL, to specify which parts of the design will be simulated. Execution of Intsim is controlled by a simulation-control language, called SIMCL.

Ensuring that all's well

To check the design, test patterns generated from design-verification and fault-simulation programs are applied to the network's inputs. The network under test is then compared with a known good network, and if the responses are the same, the tested network passes that particular test. Of course, the trick is to design a test pattern that covers virtually every fault condition.

Once the network description has been entered into a computer file, a validation procedure takes place in three stages. In stage 1, known as design verification, the designer simulates the network with test patterns to verify that it performs its logic function according to specifications. This simulation is carried out using a model of a network without faults.

3. Grading tests. Tests patterns can be generated automatically using algorithms, derivatives of logic functions, path sensitization, and random pattern generation. The process generally includes fault simulation to determine the degree of coverage.



Verification cannot distinguish a good network from a faulty one; it merely creates a model of how the actual network should perform. Ideally, the model should be subjected to every possible test pattern that is capable of producing a fault. In practice, it is a matter of engineering judgment to determine the extent of the design verification.

Faults are simulated in stage 2 by applying every possible test pattern to a fault-free network model and to each network version containing at least one fault. Multiple models of the network are thus used in the simulation run for each test pattern. When the output sequence of a good network differs from that of a faulty one, the test pattern can be used to identify the fault while testing or diagnosing the network.

Test-pattern generation is a byproduct of design verification in that test patterns are created by exploiting the intended function of the network. But functional test patterns provide only limited fault coverage, since they simulate a good network. For more thorough fault coverage, test patterns should have the ability to distinguish a good network from all possible faulty networks. Such a pattern guarantees that the network is free of faults regardless of its function.

The designer's task

Test patterns can be generated automatically using structural test methods involving algorithms, derivatives of logic functions, path sensitization, and random pattern generation, but these are the sole responsibility of the designer. Functional tests are a subset of structural tests, since they stimulate only a good network and not a faulty one. In general, test-pattern generation includes fault simulation to verify the test patterns and to determine the fault coverage (Fig. 3).

When a logic array has been designed, automatic layout software takes over to handle the actual interconnections. The structural data base created by the user is mapped into physical coordinates on silicon.

The first step toward interconnection is global partitioning, followed by local placement, wherein individual gates from the data base are positioned on the chip. After input and output contacts are placed, the interconnections are first generated locally over two levels. Actually, there are three levels in all, but only two are used by the automatic routing software; the third is predesigned for power distribution.

Connected up by computer

With local interconnection finished, the array consists of a series of cells or blocks (an MSI function exemplifies a block). To connect the entire array—that is, to effect a global interconnection—a channel router is called on. This powerful software algorithm builds a graphic model of the available routing area and routes all intercellular connections to minimize path length and eliminate channel overflow.

A major portion of the global router processes feedthrough paths (a feedthrough path is one passing through a cell that is not assigned to a signal). A preprocessor finds the feedthrough paths and the global router assigns signals to them. This process alleviates channel congestion by moving as much of the intercellular connections as possible into the cells.

When global interconnections are completed, the user's data base is completely defined in terms of X-Y coordinates and implemented with the design rules and process geometries available. As a final step, the logical data base is reconstructed and resimulated to verify that the circuit implementation is exactly what the user specified.

From a cost perspective, dense logic arrays allow a system to function with fewer parts, thereby reducing circuit-board area and minimizing cabinet dimensions. In addition, less hardware means fewer interconnections and that eases system upgrading. □

308 DATA ANALYZER

Big power in a small package.

The 308 operates in four modes: parallel state, parallel timing, serial state and signature analysis.

The 308 Data Analyzer. From Tektronix

The new 308 Data Analyzer packs an impressive array of logic analysis capabilities inside its trim, 8 pound (3.6 kg) frame. For instance, it operates in the serial and signature modes as well as parallel state and timing. And samples both synchronously and asynchronously up to 20 MHz. With a variable voltage threshold that covers all logic families in addition to TTL.

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Holographic scanner embraces supermarket bar codes

A three-dimensional pattern of laser beams wraps around retail items searching for their product codes

by E. A. Moore, *International Business Machines Corp., System Communications Division, Research Triangle Park, N. C.*

☐ A new checkout scanner is not only one of the first commercial products to employ holography but also exploits it in a novel way. Normally, the laser-based technique is used to create three-dimensional pictures or images. But in the IBM 3687 checkout scanner, a three-dimensional pattern of laser beams wraps around an item to sense its bar code.

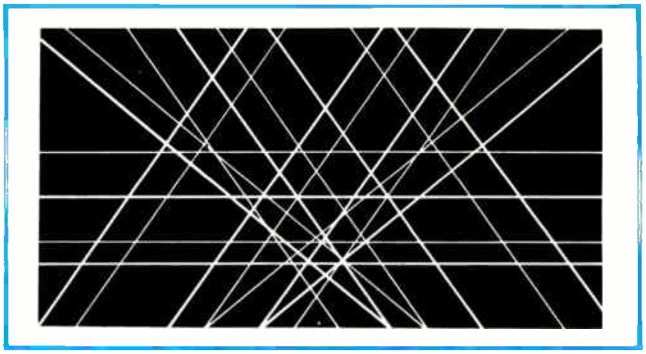
Scanning systems were first introduced into supermarkets in the mid-1970s. They provide easier, faster, and more accurate store checkout. They also make data on the movement of supermarket items readily available for sales analysis and automatic reordering.

The 3687 significantly advances the state of the art by virtue of its smaller size, greater reliability, and lesser need for careful orientation of items to be scanned than previous IBM units—advantages deriving directly from the use of holography for laser light deflection, creation of the scanning beams, and their collection. In addition, it is much less expensive than would be a nonholographic scanner with a similar wraparound pattern.

As an input device for the IBM 3683 point-of-sale terminal, the 3687 scanner (Fig. 1) reads the product-code identification symbols, or bar codes, on items. These symbols are known as the Universal Product Code (UPC), European Article Number (EAN), and Japanese Article Number (JAN) in the U. S., Western Europe, and Japan, respectively.

The unit is easy to integrate into a store's check-stand furniture, since it is less than a third the size of previous IBM checkout scanners and has simpler cabling require-

1. Plug it in. The IBM 3687 checkout scanner is a compact unit that can be easily mounted in supermarket checkout-stand furniture. The simplicity of the product eliminates the need for installation by specially trained service people and for periodic adjustment.

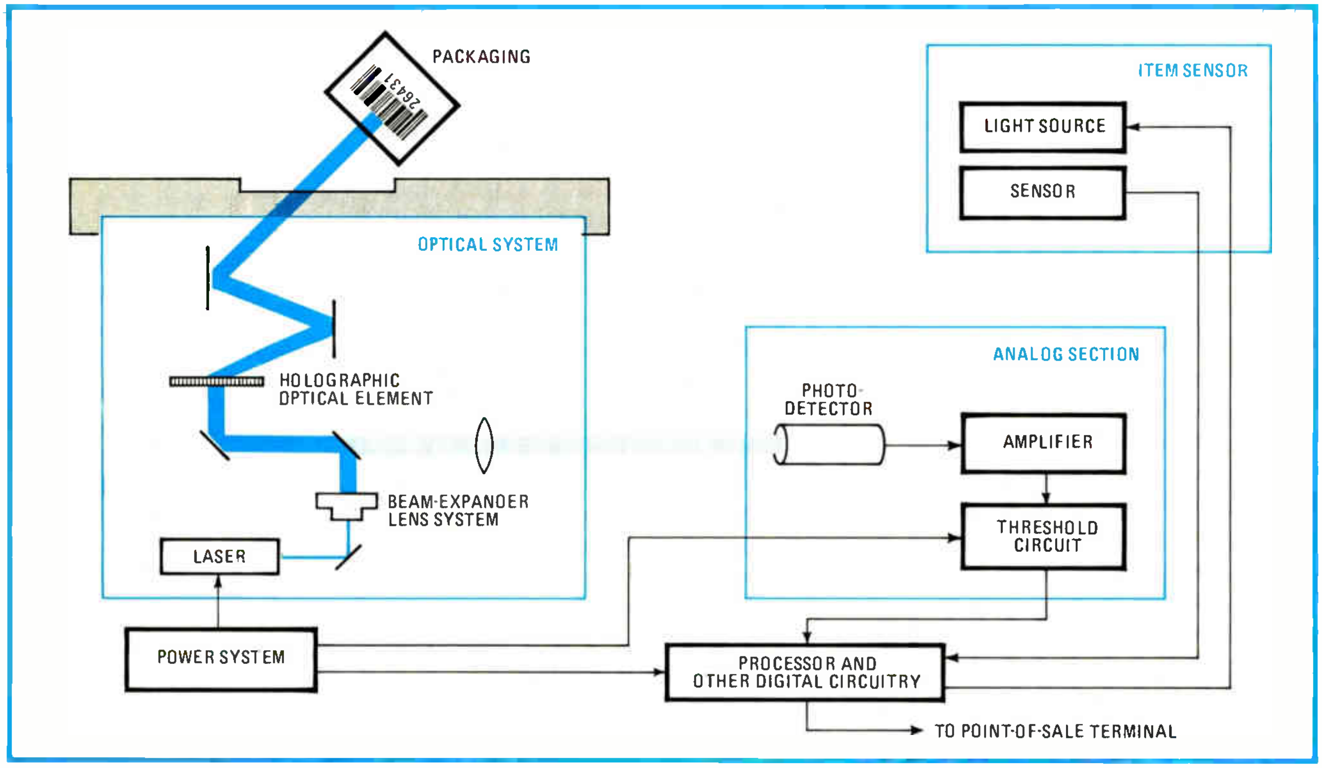


2. Search lights. This pattern, seen looking down at the scanner window, is produced by the laser beams projected from the window during one revolution of the holographic disk. The beams exit in so many directions that one will be sure to scan the product code.

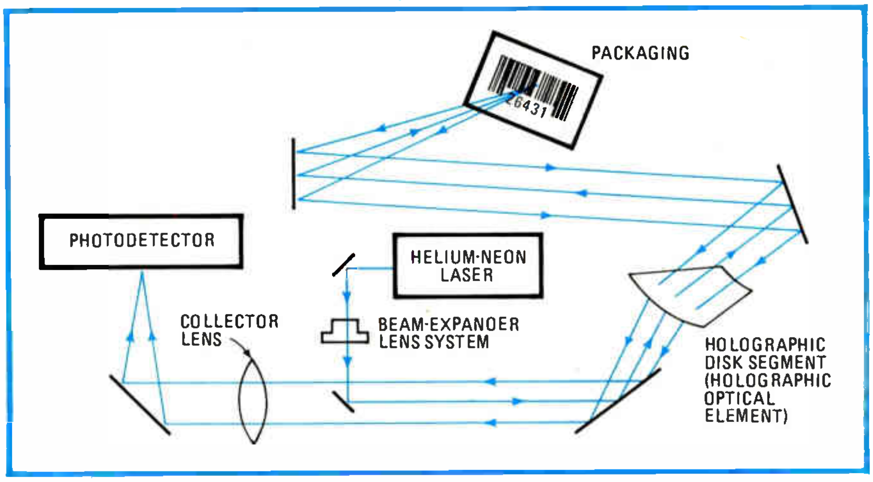
ments. Also, because it requires no tools to install nor any field adjustments, it can be set up or moved by the customer without a service call.

Reliability was a key consideration in designing the 3687. To provide a similar scanning pattern with traditional optical elements (mirrors, lenses, and so on) would have resulted in a much larger, heavier, and more complex scanner that would have needed adjustments from time to time. In contrast, none of the elements in the 3687's optical system require adjustment once the machine has been assembled, and the only moving parts are the holographic deflector disk rotated by a small motor, a cooling fan, and a shutter. These two aspects enhance the scanner's reliability and make it easier to manufacture and service.

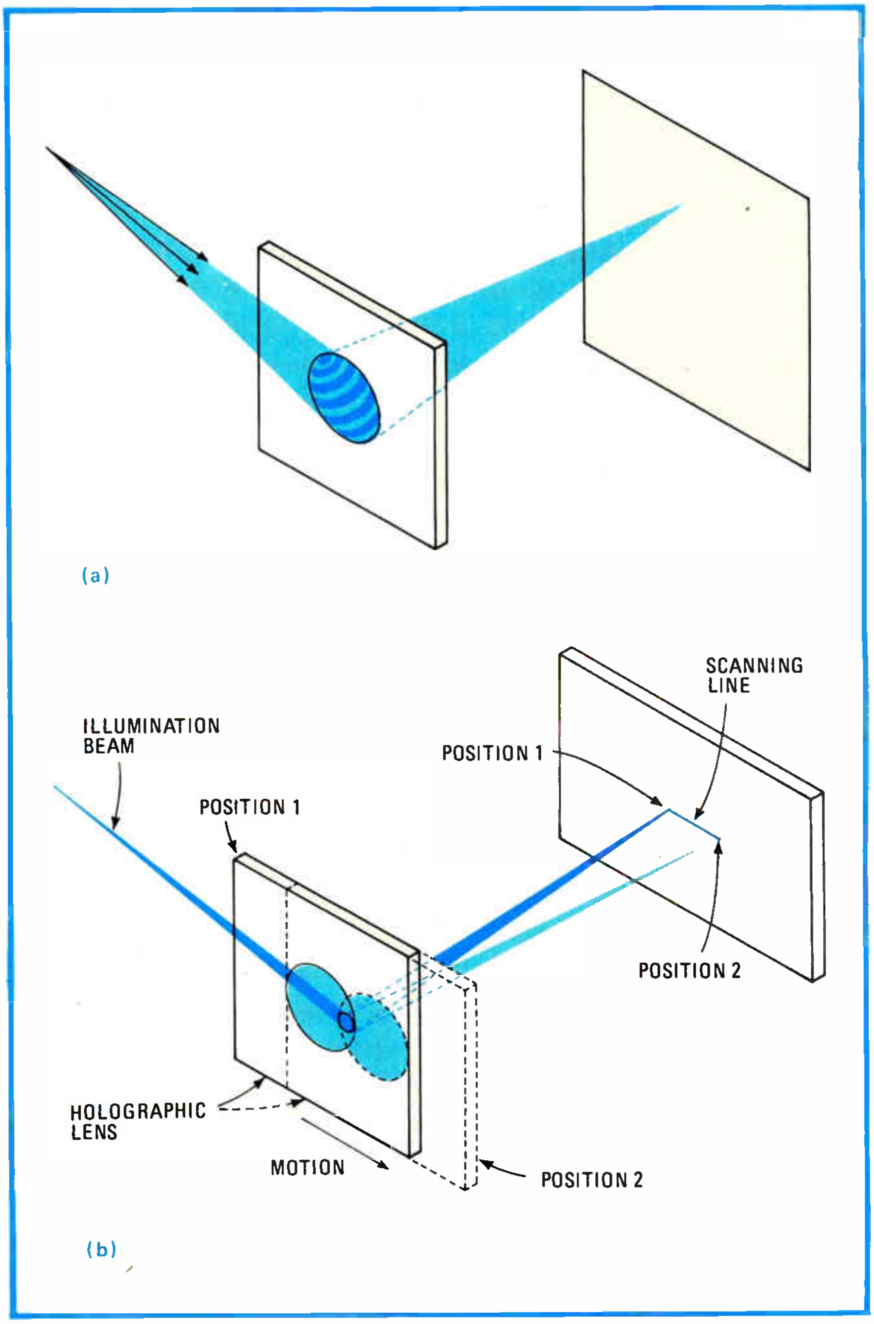
A beam of laser light scans the bar code as an item is passed over the window of the scanner. The light reflected from the symbol is collected by the scanner's optical system. Next, the decoded bar-code information is transferred to the point-of-sale terminal. The terminal forwards the item-code data to an IBM 3651 store



3. Five-part scanner. Inside the holographic checkout scanner are five subsystems—the optical system, the analog section, the microprocessor-based digital circuitry, the item sensor, and the power system. They all fit into a single small cabinet.



4. Light fantastic. The optical system includes the elements to produce the three-dimensional pattern of light beams that sweep around products placed on the scanner. This subsystem also detects the product-code patterns in the reflected beams.



5. Deflect, focus, move. A simple holographic optical element performs like a combination of a prism and a lens; it both deflects and focuses a beam of laser light, producing a small spot (a). The spot of focused laser light becomes a scanning line when the holographic optical element is moved. Each element produces a scanning line having its own focal length and deflection angle (b).

Casting some light on holography

Holography was conceived in 1947 by Prof. Dennis Gabor of the Imperial College of Science and Technology in London, while investigating ways to reduce spherical aberration in electron microscopes. Although he did not achieve his original goal, many people consider his discovery of holography a far greater achievement—in fact, in 1971 he was awarded a Nobel Prize for it. However, applications of Gabor's wavefront-reconstruction principles had to wait for a coherent-light source—that is, one that produces light having parallel rays of an extremely narrow bandwidth, such as a laser. Thus holography, although invented before the laser, could not be used until the laser was developed.

The word "hologram" comes from two Greek words: *holos*, which means "whole" or "complete"; and *gramme*, which means "letter" or "piece of writing." Thus, a hologram is a complete message about or record of something (such as an object or scene).

In conventional photography, light from an object or scene is focused by the camera lens onto a photographic emulsion. The resulting exposed and developed plate or film is a reverse (negative) picture of the original subject. Variations in the amount of light reaching the photographic emulsion appear on the negative as varying shades of silver density.

A hologram, on the other hand, may be produced without a lens, since no image of the subject is formed. Instead the light from a laser is split into two beams by a partially reflecting mirror. Both beams are expanded and filtered by a short-focal-length lens and pinhole assembly (see figure). The light in one of these beams is directed toward the object, which reflects and scatters it to a high-resolution photographic plate.

The photographic emulsion records optically coded phase and amplitude information in the interference pattern formed by the combining of these two light beams (referred to as the object and reference beams). This interference pattern appears on the developed plate as light and dark wavy lines and dots with no hint of the image embodied in it. Yet this pattern, unintelligible to the human eye, contains all the information necessary to re-create the light waves originally emanating from the object. Instead of recording an image, a hologram records the coded information representing light waves themselves. The original light waves can be regenerated from this code.

A hologram is seen by illuminating it with a reference beam identical to the original. The resulting image is indistinguishable in its three-dimensional aspects from the appearance of the original object or scene: perspective changes with viewing position, and there are differences between near and far objects in a scene caused by parallax. As with the original scene, an observer can move his head to look around an object in the foreground to see an object hidden in the background.

A hologram can be thought of as many complex wave patterns frozen on a photographic film. When the coded light waves are reconstructed with a reference beam, the halted waves continue outward from the hologram exactly as the original waves would have done had they not been interrupted by the photographic plate.

As the technology developed, other types of holograms with special and unique features were produced using numerous modifications of the basic technique. A transmission hologram is illuminated from behind the plate, and the light is transmitted through it to the viewer's eyes. A reflection hologram is produced by making the object beam and the reference beam falling on the plate from opposite sides. This type of hologram is illuminated by reflecting the source light from the plate.

The most successful and widely used application of holography today is probably holographic interferometry.

controller, which looks up the code and retrieves the price and item description. This data is then returned to the terminal, where it is displayed and printed on the customer's receipt.

Laser, laser everywhere

The performance of the 3687 has been improved by providing a dense scanning pattern (Fig. 2) with the laser beams exiting the window of the scanner at such angles that a wrapping effect is achieved around items passed over the window. Consequently, items having symbols on their sides can be scanned by being passed upright over the scanner and rotated up to 90° in either horizontal direction.

The scanning pattern has been designed to produce a maximum number of beams traversing the symbol as the item passes over the scanning window and at the same time to distribute the reading capability as evenly as possible throughout the scanning volume. The density and three-dimensional configuration of the scanning pattern eliminate the need for turning products to position the product code directly over the scanner's window.

Ambient light presents no problem because the optical system returns the reflected laser light to the photodetector along the same path as the outgoing beam that scans the symbol. Ambient light entering the scanner from other directions does not reach the photodetector and so cannot interfere with the light containing the product-code signal. The insulation from ambient light and the use of multiple scanning beams greatly reduce problems caused by reflections from shiny packaging.

The optical system has been designed to conform to the Food and Drug Administration regulations for a Class I laser product, which is the safest such classification, and requires no safety labeling. In addition, the laser is automatically turned off when the scanner is unused for a certain period and is automatically turned on when scanning is resumed.

Five parts

The scanner can be divided into five major sections—the optical system, the analog electronics, the microprocessor-based digital circuitry, the item sensor, and the power system (Fig. 3)—all of which is housed in a single cabinet. Data passes to the point-of-sale terminal over a thin, flexible cable.

The purpose of the optical system is both to provide a source of light for scanning symbols on purchased items and to collect and detect the light reflected from the symbols. In order to read product codes from items, two

This is a nondestructive testing technique in which a holographic image of an object is superimposed over the real object, forming interference fringes on the surface of the real object. The spacing and regularity of such fringes can be used, for instance, to evaluate rotating turbine blades, detect cracks in aircraft components, and examine automobile tires. Holography also has potential for large-depth-of-field microscopy, making three-dimensional terrain maps, and visual displays. However, the applications that most excited people's imagination when it was invented—3-d TV and movies—are not expected to become a commercial reality before the year 2000.

Holographic optical elements have been employed in scanning, ranging, and camera systems and in such military applications as missile-seeking systems and aircraft cockpit head-up and simulator displays.

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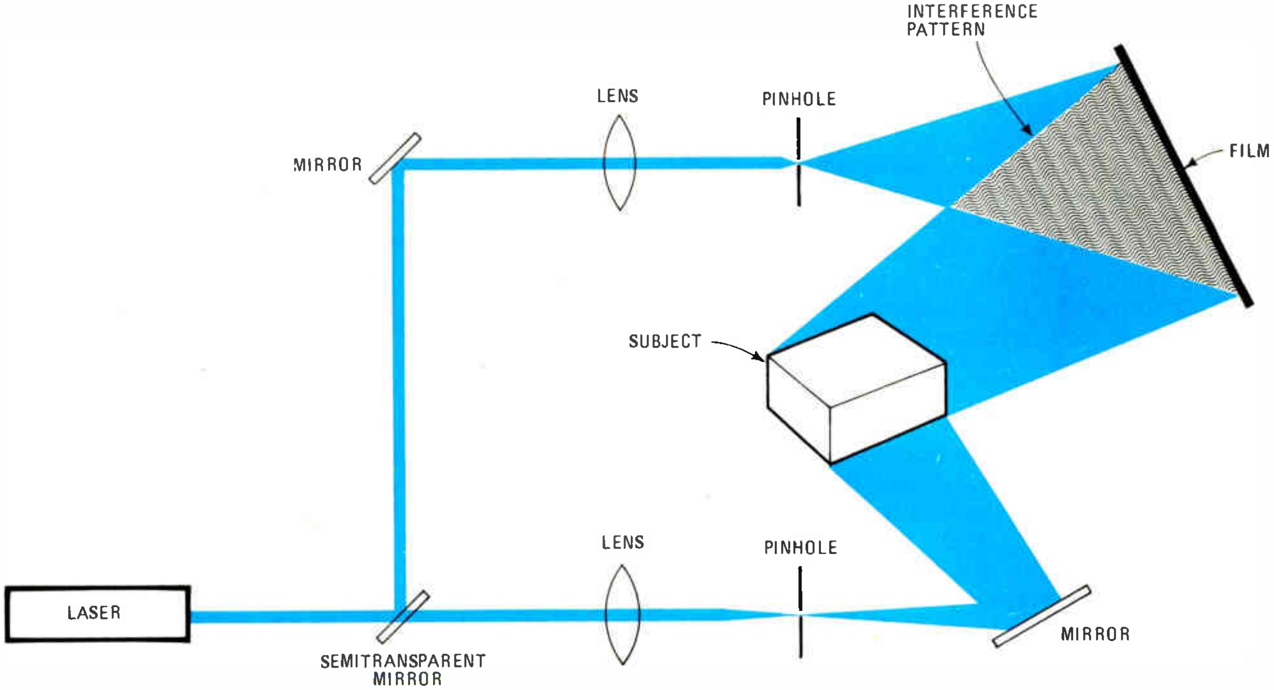


operations must take place: the operator must pass the item over the window of the machine, and the optical system must cause the laser light beam to scan the symbol. A pattern of beams is formed, and as the item passes over the window, the beams will traverse the symbol one or more times.

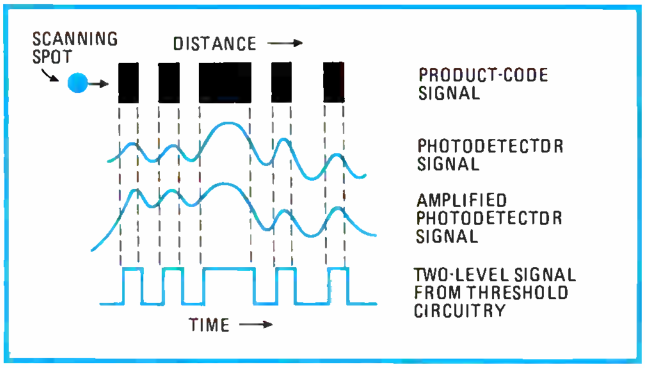
Mirror, mirror

The light source for the optical system (Fig. 4) is a low-power helium-neon gas laser. A beam-expander lens system increases the diameter of the small collimated beam produced by the laser, allowing the optical system to have a larger relative aperture, or lower f number, so that a smaller scanning spot can be used. The beam is then directed by mirrors to the holographic deflector disk. As the disk rotates, the laser beam is deflected onto a system of fixed mirrors, forming the scanning pattern. In addition, the holographic deflector also functions as a lens and focuses the laser beam to a very small spot in the area of the scanner's window.

When the focused beam scans the symbol, light reflects from it in all directions, with the bars and spaces in the symbol returning different amounts of light. Some of the light is reflected back along the path of the outgoing beam (the retro-reflective path), collected by the holographic disk, and focused onto the photodetector. The returning light path has a much larger diameter than the small collimated beam from the beam expander, being limited only by the sizes of the mirrors and the holographic element. Most of the returning light will pass around the small mirror that deflects the output beam and will be focused onto the photodetector by the collector lens.

A unique feature of the 3687's optical system is the use of a holographic deflector to produce the scanning pattern. Holograms are popularly thought of as creating three-dimensional images (see "Casting some light on holography," opposite). The holograms employed in the scanner are created by means of the same light-wave interference technique; however, the object here is to produce, not a three-dimensional image, but a holographic optical element (HOE). In this case, the hologram, or holographic optical element, is the optical equivalent of a prism and lens in combination. It deflects and focuses a collimated laser beam passing through it, acting very much like a zone-plate or diffraction grating (Fig. 5a).

If the holographic optical element is moved relative to the laser beam, the focused spot formed by the element will also move and, in moving, will produce a scanning beam (Fig. 5b). The deflection angle and focal length of



6. Signal shaping. The electrical signal produced by the photodetector is amplified, then shaped by the threshold circuitry into a two-level digital signal for the microprocessor. The latter converts the signals into the appropriate numbers of the product code.

the element can be modified by changing the setup used to make the hologram. Thus different holograms with different focal lengths and deflection angles can be mounted in a rotating disk. As the disk spins, scanning beams of different focal lengths are created. A system of fixed mirrors forms this set of beams into a scanning pattern that appears to wrap around the item.

Making a HOE

A holographic optical element is produced by combining two interfering coherent light beams (an object beam and a reference beam) that originate from the same source and arrive at a light-sensitive recording medium, such as film. The location of the lens determines the focal length of the element, and the spatial relationship between the object and reference beams determines the deflection angle. Exposing high-resolution, fine-grain silver halide film with the interfering object and reference beams yields an interference pattern of many closely spaced lines that remains after the film is developed.

However, holographic deflector disks made of HOEs as described above would be prohibitively expensive for a checkout scanner. Fortunately, a method of making such elements employing a master HOE (analogous to making photographic prints from a negative) is possible. In this process, the master is placed next to the film used to make the copy. The master is illuminated with a laser and the deflected light forms a light wavefront exactly like that of the object beam used to make the master. Some of the light passes straight through the master and acts as the reference beam to produce, in the copy, the same interference pattern that exists in the master. Consequently, the copied element has the same focal length and deflection angle as the master. The copy is then developed, in a process similar to that used for photographic film.

Minimizing losses

Some of the light falling on a holographic optical element passes straight through without being deflected, some is reflected, and some is absorbed. Only the deflected light is useful in scanning. The amount of light returned through the HOE during scanning is limited partially by the diffraction efficiency of the element, or the ratio of light going out of the element at that particular deflection angle to the light coming in. Since only a small portion of the light reflected from a symbol is returned along the retro-reflective path, it is critical that losses of the returning light be minimized.

To maximize the diffraction efficiency for both the outgoing and the returning light, dichromated gelatin was chosen as the photosensitive holographic recording medium for making copies of the holographic optical elements. This material, which is merely ordinary gelatin sensitized with ammonium dichromate, can be used to create holograms in thin films that have a high diffraction efficiency and are relatively insensitive to misalignments of the incident laser beam.

In the deflector disk, the dichromated-gelatin-film elements are sandwiched between two glass plates to give them rigidity, strength, and protection from the environment. A hub is bonded to the disk for connection to the shaft of the motor.

Shaping up the signal

After the optical signal is converted into an electrical signal by the photodetector, it is amplified and shaped to form a two-level signal that has a temporal relationship proportional to the spatial relationship of the bars in the symbol being scanned (Fig. 6).

The dynamic range and bandwidth requirements impose stringent demands on the design of the amplifier. In addition, the distortion introduced into the signal because of the amplifier and the shape of the light spot scanning the symbol require sophisticated edge-finding techniques in the design of the threshold circuitry, which produces a digital signal.

Symbol finding, decoding, and testing are performed by the microprocessor-based digital portion. Symbol data from the photodetector is interspersed with random data generated by scanning printed matter (other than the symbol) on items. The processor filters the data by looking for patterns that fit the geometry of the allowed symbols. Data passing this test is then decoded into numbers by measuring the temporal relationships within the data pattern and processing it using the symbol-decoding algorithm.

Modulo checking

Items passed over the machine are generally scanned by the light source several times, as noted. When the scanning is complete, the data is tested by a modulo-checking algorithm determined by the particular code being scanned. Data that passes the modulo checking is then passed to the point-of-sale terminal for data lookup, display, and printing of customer receipts. A flashing light and a beep tell the cashier the scan was successful.

An optical sensor system made up of a photodiode and a light-emitting diode detects an item as it approaches the scan window and opens a shutter located between the laser and the beam expander. To reduce cost, improve reliability, and achieve a larger field of detection, the sensor's two elements have been packaged on the same circuit board. A mirrored surface on the opposite side of the machine reflects the light from the source back to the detector. □

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Simple patch reconciles parity flags in Z80, 8080

by Zvi Herman
Elbit Computers Ltd., Haifa, Israel

Since the Z80's instruction set is a superset of the 8080's, a program written for the latter can be run on the former. However, there are subtle incompatibilities that may cause unexpected behavior when such a program is run on the Z80—one of them being the definition of the parity flag.

In the 8080, this flag indicates the parity of the result, whether the operation is arithmetic or logical. But the meaning of the flag has been modified in the Z80 so that it indicates the parity of the result after a logical operation only.

When an arithmetic operation is executed, the parity flag (called P/V in the Z80) instead indicates an overflow condition. Hence, when an 8080 program relies on the parity resulting from an arithmetic operation, that piece of code could produce erroneous results when run on the Z80.

For instance, suppose the content of the accumulator is 55_{16} and the following instructions are executed:

ADI 11H (add 11_{16} to the contents of the accumulator)
JPE NEXT (if parity is even, jump to NEXT)

The 8080 adds 11_{16} to 55_{16}, the result is even, and the condition for the jump is true. But when the Z80 adds 11_{16} to 55_{16}, the result causes no overflow and the P/V flag stays off. Now the condition of the jump is false, and the Z80 continues right through the next instruction, rather than jumping to NEXT.

It is obvious that a patch is needed here. This patch (between the ADD and the JUMP) should leave the accumulator and the flags intact. The only change required is modification of the P/V flag to reflect the parity result from the arithmetic operation.

There is no single instruction in the Z80, however, that can do all that. All instructions that modify the P/V flag, in the sense of parity, change either the accumulator or other flags; a series of instructions, however, will produce the desired result.

The following sequence provides the solution:

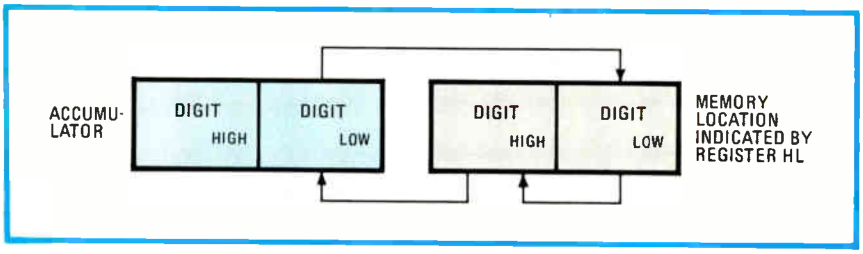
```
ADD  A,11H
RLD         (rotate left one digit [nibble] to the left)
RLD
RLD
JP   PE,NEXT
```

The RLD instruction rotates the least significant (4-bit) digit of the accumulator through the memory location pointed to by register HL (see figure). It modifies the P/V flag to reflect the parity of the accumulator and does not affect the carry (CY) flag.

If the instruction is used three times, the accumulator is returned to its initial value and the CY, sign (S), and zero (Z) flags are restored. Note that RRD may be used to rotate the digit right with the same success.

This patch, however, does contain a few pitfalls. For one, the half-carry flag is zeroed by the RRD/RLD instruction. When the parity of the result of an arithmetic instruction is desired, the chance that the half carry is needed somewhat later is small, but it does exist.

When HL points to locations in read-only memory, this patch is not suitable, since ROM locations cannot be written into and thus cannot be used for temporary storage. Finally, the patch adds execution time to the program, and that factor should be considered when software timing is important. □



Bit brigade. Parity is flagged for arithmetic operations in the Z80 by rotating the least significant nibble in the accumulator through memory and back. Three executions of the RLD or RRD instructions perform this task.

Current loop supports remote distributed processing

by Akavia Kaniel
Measurex Inc., Cupertino, Calif.

Long-distance serial communications between distributed processors, such as Intel's 8051 single-chip microcomputer, is best achieved by using one of the data-transmission standards—a 20-milliampere current loop, for instance. The circuit shown in the figure uses the universal asynchronous receiver/transmitter and the bit-rate generator built into the 8051 to implement a full-duplex, 20-mA current loop that operates at speeds of

COMMUNICATION SUBROUTINES FOR 8051 MICROCOMPUTER

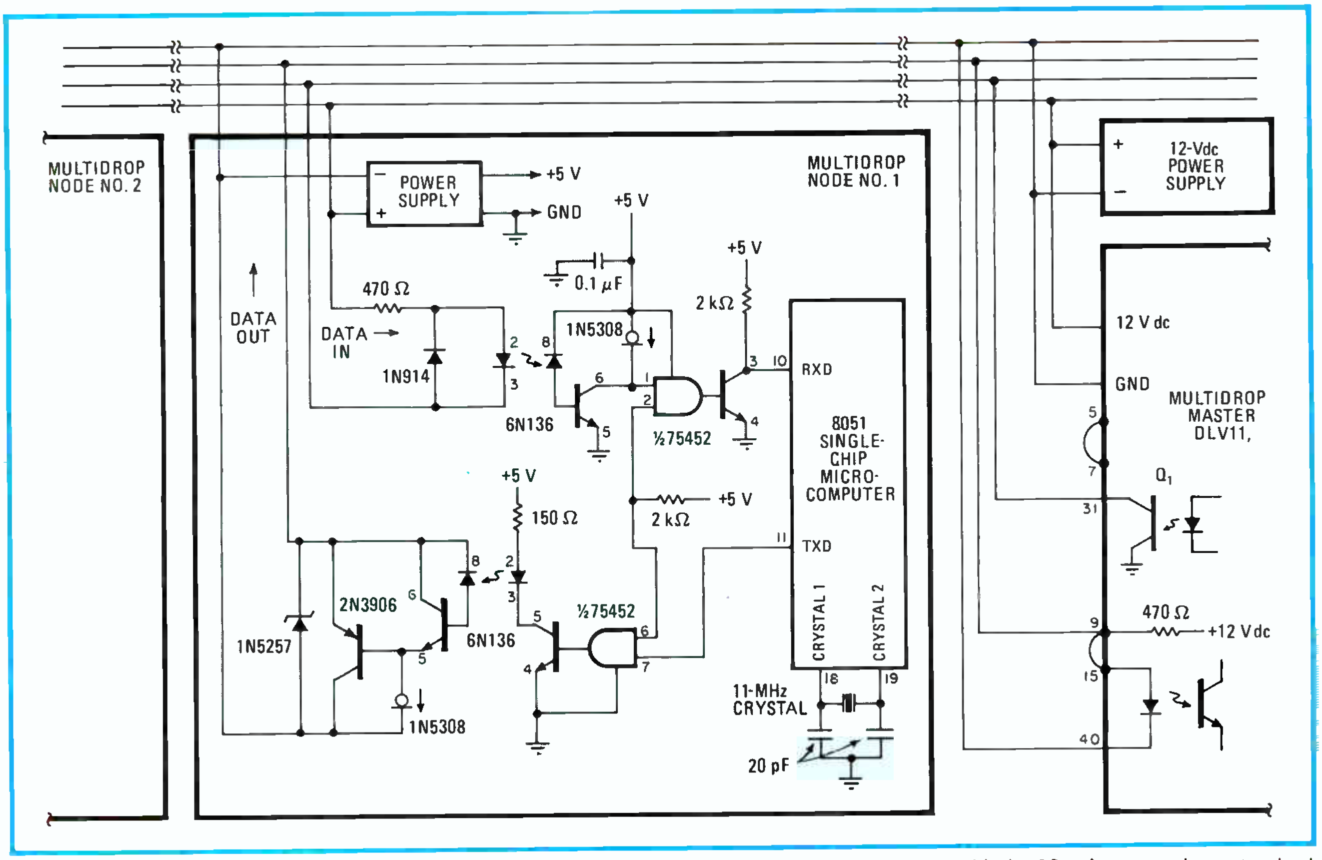
Program	Comments
INIT: MOV TL1,=0FDH	PRESET COUNTER 1 TO 253
MOV TH1,#0FDH	FOR 9,600-b/s RATE.
MOV SCON,=0C0H	UART SET TO ASYNCHRONOUS, 1 STOP, 1 START, 8 DATA BITS, 1 EVEN PARITY BIT; RECEIVER NOT ENABLED YET.
MOV TMOD,=25H	TIMER 1 IS BAUD-RATE GENERATOR, TIMER 0 IS A 16-BIT COUNTER.
SETB TR1	ENABLE BAUD-RATE GENERATOR.
SETB REN	ENABLE RECEIVER.
RET	
SEND: JNB TI,SEND	WAIT HERE TILL THE TRANSMIT BUFFER IS EMPTY.
MOV A,CHAR	STORE CHARACTER TO BE SENT IN THE ACCUMULATOR.
MOV C,P	MOVE THE EVEN-PARITY
MOV TB8,C	BIT FROM THE PROCESSOR STATUS WORD TO TB8 = PARITY BIT IN TRANSMIT BUFFER.
CLR TI	CLEAR THE TRANSMIT-BUFFER-EMPTY FLAG.
MOV SBUF,A	SEND THE DATA TO THE TRANSMIT-BUFFER.
RET	
RCV: JNB RI,RCV	WAIT HERE TILL THE BYTE-RECEIVED-FLAG IS HIGH.
CLR RI	RESET THE FLAG.
MOV A,SBUF	STORE THE RECEIVED BYTE IN THE ACCUMULATOR.
MOV C,RB8	STORE RECEIVED PARITY BIT.
JNB P,N_PAR	CHECK IF THE PARITY
JB CY, PROC	OF THE RECEIVED BYTE
CALL ERROR	EQUALS THE
JMP PROC	PARITY BIT IN THE
N_PAR: JNB CY,PROC	RECEIVED BYTE; IF
CALL ERROR	NOT CALL THE ERROR-
PROC: RET	ROUTINE.

110 to 9,600 bits per second.

In addition, there are three canned software routines that perform initialization, data transmission, and data reception and are meant to be called by the user software when needed. These routines are given in the accompanying table.

The figure also shows how a string of 8051-based nodes situated along a four-wire transmission line is configured. Each node represents a point where some processing is accomplished, as, for example, in an industrial plant. At least 10 nodes can be driven with the system shown, this limit being set by the current-sinking capability of transistor Q_1 in the multidrop master.

Besides data, the transmission line also carries power to each node, 12 volts dc in this case. If necessary, this 12 v dc can be converted to other voltage levels that are needed locally by the electronics at each of the nodes. As illustrated in the figure, each node is also coupled to the transmission line through an optical-coupler circuit using a 1N5308 constant-current diode. □



1. Long distance. Individual nodes are linked along the four-wire transmission system in accordance with the 20-mA–current-loop standard. At least 10 nodes can be driven by this system. In addition, the transmission line supplies 12 volts dc to each node for local electronics.

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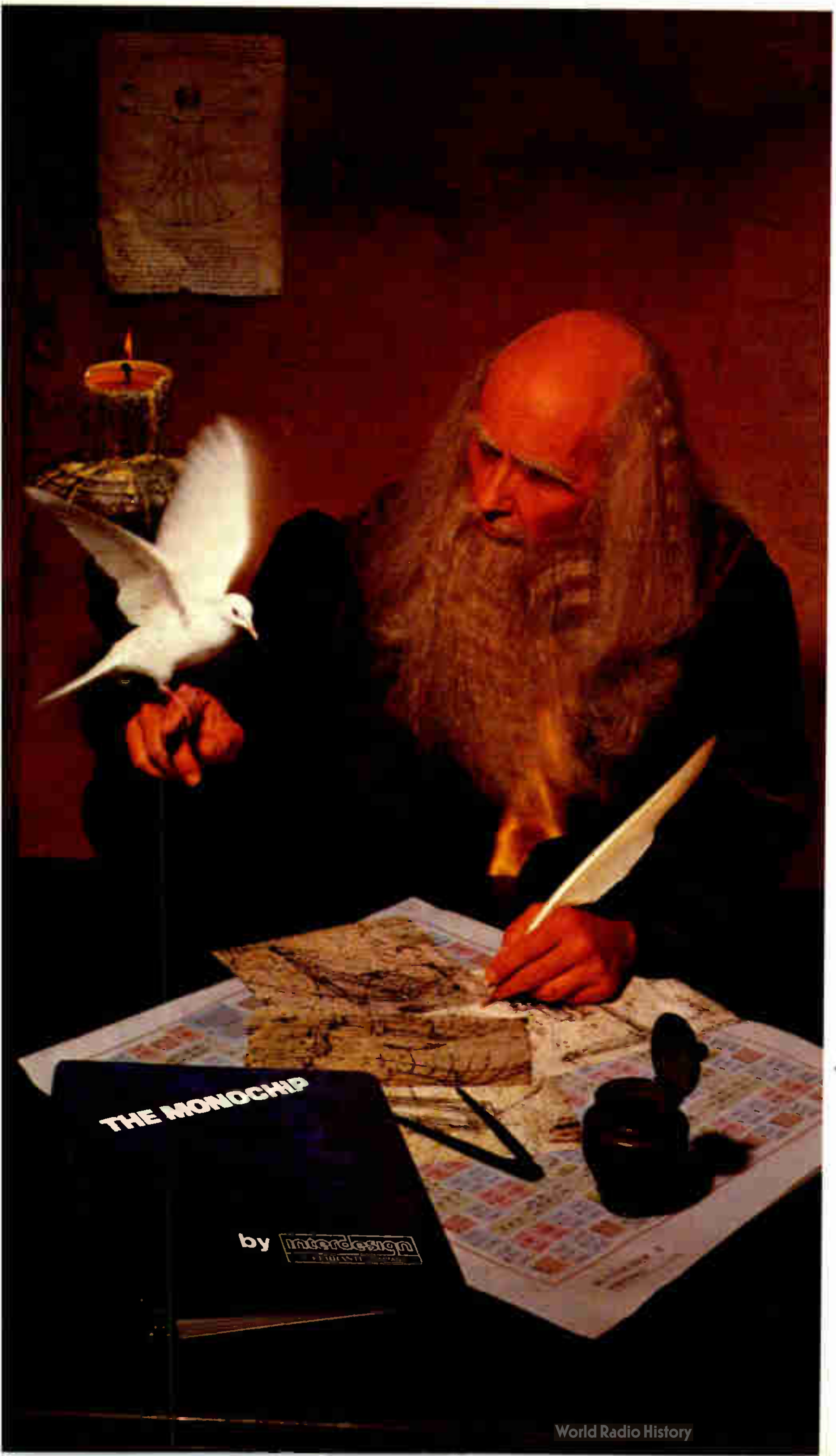

"Can man fly?" That was a question that haunted Leonardo da Vinci for almost twenty-five years. If Monochips™ were around in his lifetime, he might have designed a computer to solve the riddles of aerodynamics — and taken to the sky five centuries before Wilbur and Orville Wright.

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Calculator plots time response of inverse Laplace transform

by Hank Librach
Fairfield, Conn.

Combining the benefits of two previous notes[1,2] in this series, this HP-41C calculator note solves the inverse Laplace transform and then displays the results on the calculator's miniprinter-plotter.

Using the Gaver algorithm[3] to approximate the time-domain representation of a Laplace transfer function, the Hewlett-Packard calculator and program form a portable tool for visualizing the time-domain response of a system given the Laplace transform. The user is prompted by the program to choose the bounds of the time axis as well as the time increments. Then by redefining the start and end points of the axes, the user can zoom in on smaller time increments.

Step 59 (LBL A) in the program shown is where the transfer function is entered—in this case, it is $F(s) = 1/(s+2)$. Then the corresponding time-varying function—namely, $f(t) = e^{-2t}$—is plotted along the axes specified by the user.

The prompts that specify the plot coordinates are shown in the table. The resulting printout, for a range of 0 to 2 seconds in 0.1-s increments, is shown in the figure. The Gaver Approximation makes conventional assumptions regarding the time functions—namely that f(t) is bounded and well-behaved. Finally, an extra memory module is needed to run the printer-plotter. □

References
1. Kin-chu Woo, "TI-59 inverts Laplace transforms for time-domain analysis," *Electronics*, Oct. 9, 1980, p. 178.
2. Michael A. Wyatt, "Home computer displays inverse Laplace transforms," *Electronics*, March 24, 1981, p. 163.
3. D. P. Gaver, "Observing Stochastic Processes and Approximate Transform Inversion," Operational Research, Vol. 14, No. 3, 1966. pp. 444–459.

PROMPTS FOR SETTING X AND Y AXES

NAME ?			AXIS ?		
ILT		RUN		0.00	RUN
Y MIN ?			X MIN ?		
	0.00	RUN		0.001	RUN
Y MAX ?			X MAX ?		
	1.00	RUN		2.00	RUN
			X INC ?		
				.10	RUN

Miniplotting. The plotted curve of the inverse Laplace transform is generated from the computed results by an HP-41C calculator. Axes are set up according to the user's response to series prompts that are part of the overall program for calculating the inverse transform. The X and Y coordinates are rotated 90° clockwise from the standard Cartesian representation in the arrangement, right, which depicts the actual plot as it emerges from the calculator's miniprinter.

```
        PLOT OF ILT
     X (UNITS = 1.) ↓
     Y (UNITS = 1.) →
        0.00                1.00
        0.00
      ├- - - - - - - - - - - - -┤
0.00:                           x
0.10:                       x
0.20:                    x
0.30:                 x
0.40:               x
0.50:             x
0.60:           x
0.70:          x
0.80:         x
0.90:        x
1.00:       x
1.10:      x
1.20:     x
1.30:     x
1.40:    x
1.50:   x
1.60:   x
1.70:  x
1.80:  x
1.90: x
```

HP-41C PROGRAM LISTING FOR INVERSE LAPLACE TRANSFORM

```
PRP "ILT"

01  ♦LBL "ILT"
02  STO 26
03  .083333333
04  STO 13
05  -32.0833333
06  STO 14
07  1279.000076
08  STO 15
09  -15623.66689
10  STO 16
11  84244.16946
12  STO 17
13  -236957.5129
14  STO 18
15  375911.6923
16  STO 19
17  -340071.6923
18  STO 20
19  164062.5128
20  STO 21
21  -32812.50256
22  STO 22

23  ♦LBL B
24  12
25  STO 25
26  RCL 26
27  2
28  LN
29  X<>Y
30  /
31  STO 23
32  0
33  STO 12
34  STO 24

35  ♦LBL 02
36  1
37  ST+ 12
38  ST+ 25
39  RCL 23
40  RCL 12
41  *
42  XEQ A
43  RCL IND 25
44  *
45  ST+ 24
46  RCL 12
47  10
48  X=Y?
49  GTO C
50  GTO 02

51  ♦LBL C
52  RCL 24
53  RCL 23
54  *
55  RTN
56  GTO B
57  "ENTER FUNCTION"
58  PROMPT

59  ♦LBL A
60  2
61  +
62  1/X
63  RTN
64  END
```

Learn all about speech processing

It's a major commitment in time and money, but for five days starting on Nov. 9, at a cost of $925, the tutorial seminar "Making Silicon Talk . . . and Listen" is a good way to learn about speech processing, algorithms, and architectures. Conducted by Signal Technology, the meeting will present the principles, techniques, and implementations of analysis and synthesis systems ranging from channel, formant, and linear predictive vocoders to the newest vector quantization approach. The audience also will learn about phonetics, text-to-speech systems, waveform coding, and speech recognition and will hear **a comparative evaluation of architectures and technologies for implementing speech-processing algorithms.** The seminar is not for the faint-hearted or the technically uninitiated and requires advance background reading. For more information, contact Alan Gersho, Signal Technology Inc., 15 West De La Guerra, Santa Barbara, Calif. 93101; (805) 963-1552.

Book deciphers communications security issues

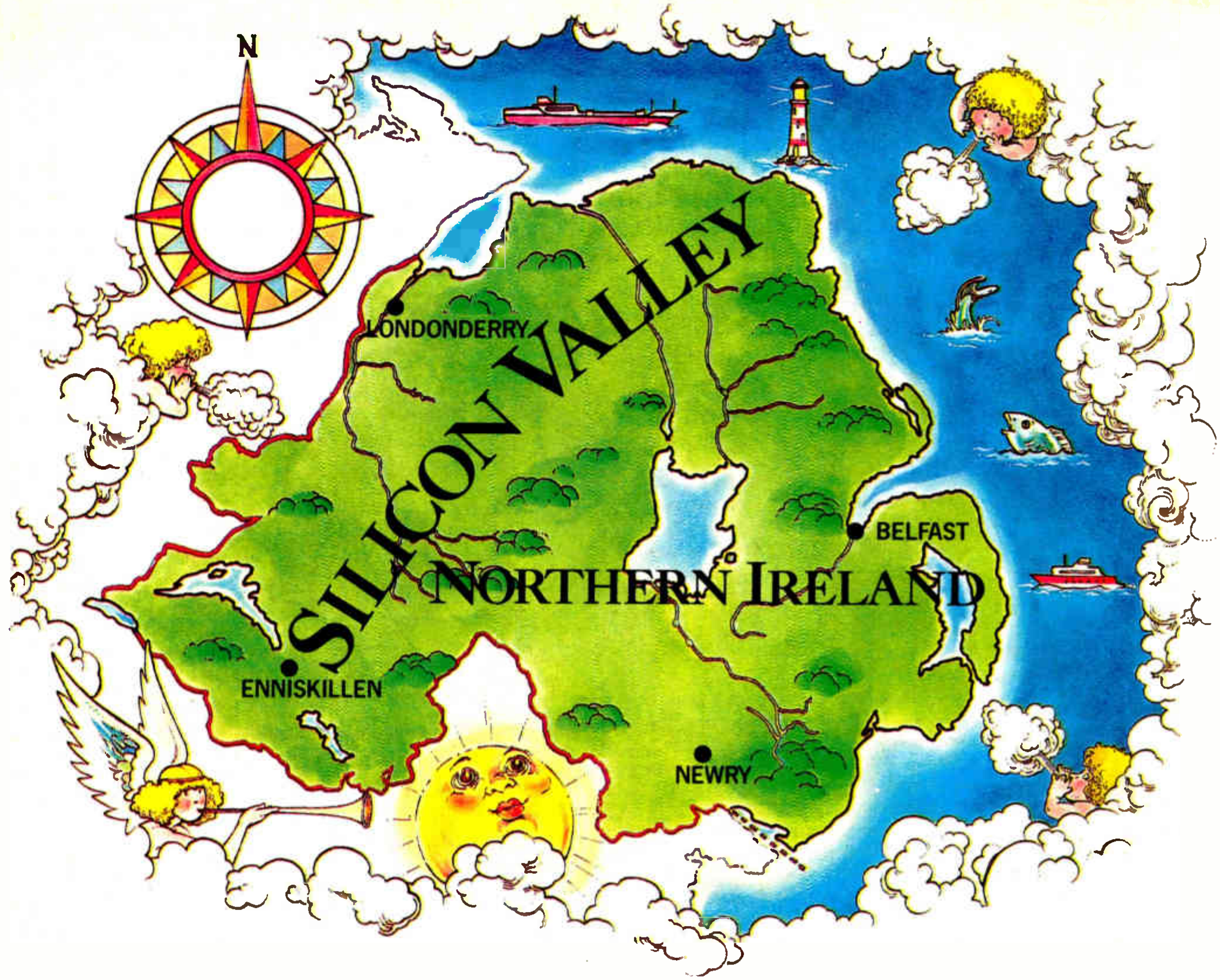
One of the problems of communications security is that few people understand what the real issues are, and one reason for this lack of understanding is that little information is available in jargon-free English, says consultant J. Michael Nye. "Who, What, and Where in Communications Security" is Nye's well-written, exceptionally informative solution to the problem. The 124-page report, **compiled with the assistance of industry vendors, the intelligence community (not all of it), the National Bureau of Standards, and the Department of Commerce,** discusses electronic interception in general and even goes into the hush-hush Tempest concept—classified Government specifications for the electromagnetic emissions allowable for data-communications equipment. It analyzes various specialized voice- and data-encryption schemes, as well as the NBS's data-encryption standard. Call Nye at (301) 791-0290 for further information, or write to him at Marketing Consultants International Inc., 100 West Washington St., Hagerstown, Md. 21740.

Video cassettes guide engineers in learning Jovial language

Jovial, the Air Force's high-level programming language for real-time military command, control, and communications, may ultimately be replaced by Ada, but for now it's still the Air Force standard. So engineers who need greater familiarity with it **should welcome a video-cassette self-study course on Jovial.** The program, for individuals or small groups is offered by SofTech Inc., 460 Totten Pond Rd., Waltham, Mass. 02154.

Teach connection and packaging with video tapes

If you're an engineering manager responsible for employee training and continuing education in production techniques, you'll likely want to look at three video tapes just released by the Institute for Interconnecting and Packaging Electronic Circuits. "Techniques of Soldering" shows the mechanics of hand soldering. "Rigid Flex Multilayer PWB Production Process" is **a study of manufacturing technology documenting the process parameters for printed-circuit (or printed-writing) boards that combine rigid and flexible layers.** "Interconnection Technology Trends in the 1980s" discusses new designs, substrates, fine lines, plated through-holes, packaging density, and more. Write to the Institute at 3451 Church St., Evanston, Ill. 60203, or call (312) 677-2850. **-Harvey J. Hindin**



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Reflectometers sight fiber-optic work

Optical time-domain reflectometers bring detailed link analysis, including fault location, out of the laboratory and down in price

by Harvey J. Hindin, Communications & Microwave Editor

Now that optical-fiber communications are competing with copper-wire installations on an economic basis, it is essential that link testing be only a small part of a system's cost. Therefore, testing must be cost-effective from the fiber manufacturing stage through the installed system checkout. But since conventional laboratory equipment is both expensive and difficult to use, the electro-optics industry is introducing cost-effective optical time-domain reflectometers for the job.

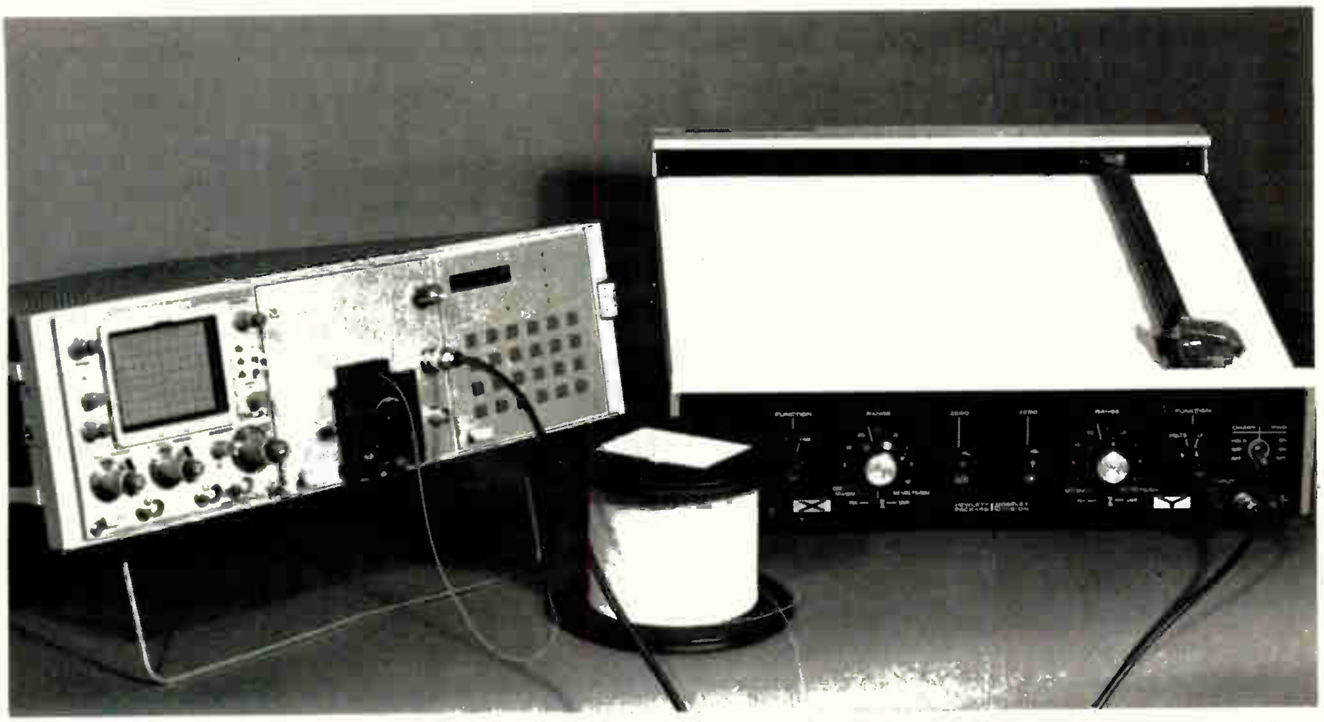
A multitude of these devices has already appeared. In all such reflectometers, the separation of the transmitted and reflected signals and the processing of the backscatter data are of prime importance.

Reflectometer processing techniques strive to maximize the backscatter signal-to-noise ratio. Both autocorrelation (see p. 118) and simple photon-counting techniques improve weak signals that are returned by small imperfections in long fibers. Processing circuit-design is made all the more difficult by theoretical problems in analyzing the backscatter waveshape in all but the simplest of cases. Phenomena such as step- or graded-index fiber type, the nature of the reflection, and the effect of bends in the fiber combine to make analysis difficult.

The ITT Components Group (Europe) Ltd. in England emphasizes automation: its ultimate goal is to produce a microprocessor-controlled reflectometer that can carry out automatic test routines on the extensive fiber-optic communications systems that British Telecom is expected to install in this decade.

The ITT OFR-1 is priced at $20,855 and can be delivered in six weeks. It can instantly display a fiber's backscatter-versus-distance curve on an oscilloscope (see "An optical radar," p. 154) and a more accurate hard-copy readout may be produced on a chart recorder. In either case, the fiber being tested may be optically scanned in equal steps over its entire length.

To observe weak backscatter sig-

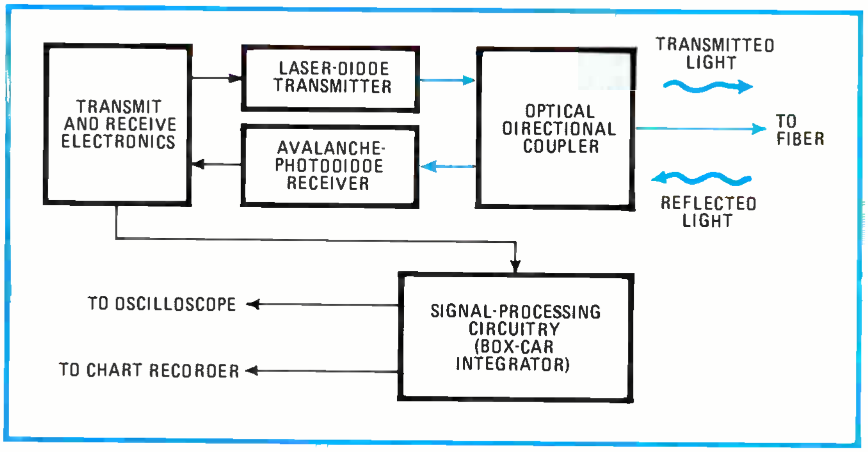


Reflections. The TD-9901 optical time-domain reflectometer from Laser Precision Corp. has a digitally swept box-car integrator with linear and logarithmic outputs. A chart recorder or plotter documents the characteristics of, in this case, a length of fiber still on the spool.

nals, the ITT reflectometer uses a signal-processing method known as box-car integration. A box-car integration circuit, through a sophisticated averaging technique, allows a reflectometer to detect nonreflecting fiber breaks at distances equivalent to more than a 30-dB round-trip loss. This is not possible with oscilloscope receivers lacking the signal-processing capability.

However, the oscilloscope receiver approach is adequate for many tests. It is so useful, in fact, that it was adopted by Times Fiber Communications Inc. in its Fiberscan series 50 reflectometer. The company claims a ±1-meter resolution in some cases for this $6,850 plug-in reflectometer, which is compatible with series 500 oscilloscope mainframes from Tektronix. The same reflectometer design may be had as a $7,250 model 51 stand-alone unit for use with any wideband scope, as a $9,250 model 53 laboratory unit with scope, or as a $9,650 model 55 field unit with scope. Delivery of any of these models takes four weeks.

Like the ITT unit, the Fiberscan reflectometer uses an avalanche photodiode detector as a receiver since maximum sensitivity in an optical



Critical component. A directional coupler with low attenuation and high directivity is needed to separate the transmitted and reflected light at the reflectometer-fiber interface.

receiver is necessary [*Electronics*, Oct. 9, 1980, p. 155]. Since a laser transmitter was used by both manufacturers, great attention was paid to eye-safety devices. In addition, either of two pulse widths (10 or 100 ns) can be chosen to optimize the backscatter signals for a particular application.

Digital readout. The key to reflectometer success for Laser Precision Corp. is microprocessor control. Not content with the raw video signals that a scope can generate, LPC has added to its $13,750, 37-lb TD-9901 reflectometer a digitally swept box-car integrator with both linear and logarithmic outputs, a microprocessor-controlled signal processor, and a direct digital readout of cable length or fault location. A hard copy of the backscatter may also be obtained by feeding the output of the boxcar integrator to a chart recorder.

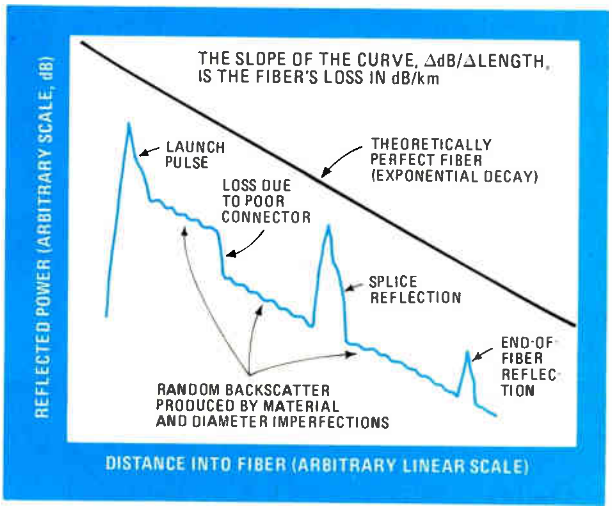
The microprocessor is especially useful for providing precise fault locations in an optical cable. The processor controls a cursor, which provides a digital display of the elapsed reflection time with a 10-ns

An optical radar

The optical time-domain reflectometer is useful for characterizing all but the shortest of fiber-optic communications links. It is designed primarily to detect such faults as poor splices, mechanical ruptures and other discontinuities and as a bonus can pinpoint their location. The reflectometer also provides information about the fiber's attenuation, its physical uniformity, and the characteristics of its connectors as well.

A time-domain reflectometer functions much like a one dimensional, closed-circuit optical radar, and like a radar, it can perform with great accuracy. Its laser transmitter injects short pulses of light into one fiber end. Depending on material inhomogeneities and any other physical variations in the fiber, such as those at splices, the transmitted pulses are partially reflected back to the test instrument, where an optical receiver captures their reflected energy. Through signal processing, the amplitude, shape, and time delay of these returning pulses yield information that lets the designer see how well his system is performing.

In high-grade communication fibers, the dominant physical mechanism causing light to be reflected is known as Rayleigh scattering, and the total reflected signal caused by it is called backscatter. By considering an oscilloscope display of backscatter as a function of the distance along a cable, a trained observer can tell a great deal about various aspects of the link's behavior. **-H. H.**



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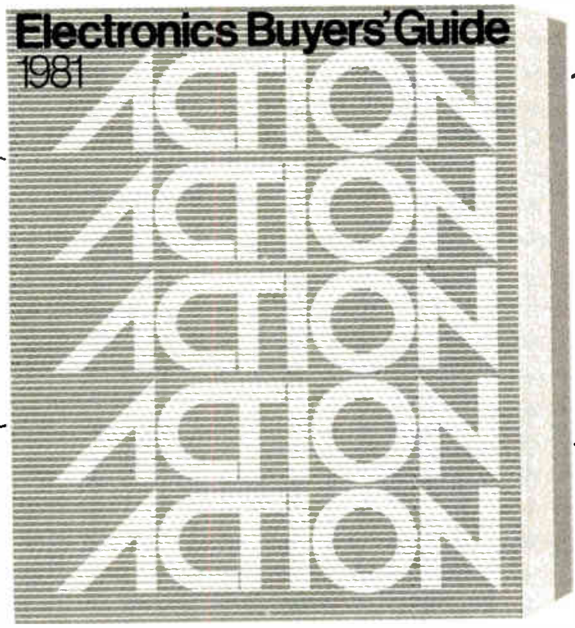

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precision and accuracy that is within ±0.01%. Distances can be extrapolated from the display once the fiber core's index of refraction has been entered into the microprocessor. (Unfortunately, this information is not always offered by fiber manufacturers.) Like the other reflectometers on the market, the TD-9901 has selectable laser pulse widths; unlike some of the others, it has self-diagnostic capabilities. Deliveries are in 60 to 90 days.

No scope. To Orionics Inc., it is clear that a hard copy of the output from a boxcar integrator reflectometer is what fiber-optic–system designers want. To fill this need, its $14,000 OTBR-106 reflectometer has a built-in chart recorder and a digital light-emitting-diode display, but no oscilloscope.

The Orionics instrument is coupled to the tested fiber by first squaring off the fiber by cleaving it and then placing it in a precision front-panel X-Y-adjustable V-block fixture. Fibers from 100 to 200 μm in diameter may be accommodated in this fixture, which requires optical-coupling compound for the best results. A single defect in a fiber can be located to within ±2 m and two adjacent defects may be resolved if they are more than 15 m apart. According to the company, attenuation of splices and connectors can be measured if the one-way fiber attenuation is less than 30 dB.

Orionics also manufactures the OTDR-103A, which is a plug-in unit for the Textronix 7000 series of oscilloscope mainframes. The firm says that fiber breaks more than 1 m from the reflectometer can be detected by the 103A, which, like its more elaborate cousin, has an X-Y positioner. The $7,560 OTDR-103A can be delivered in 10 to 12 weeks; the OTBR-106 takes 14 weeks.

ITT Components Group (Europe) Ltd., Optoelectronics Division, Leeds, Yorkshire, England [401]

Laser Precision Corp., 1231 Hart St., Utica, N. Y. 13502 [402]

Orionics Inc., 34368 E. Frontage Rd., Bozeman, Mont. 59715 [403]

Times Fiber Communications Inc., 358 Hall Ave., Wallingford, Conn. 06492 [404]

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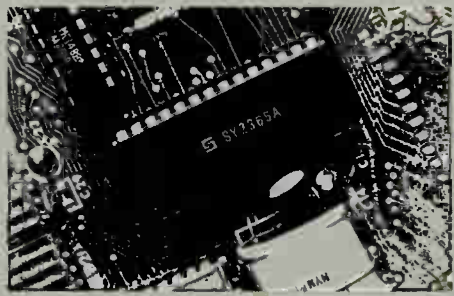

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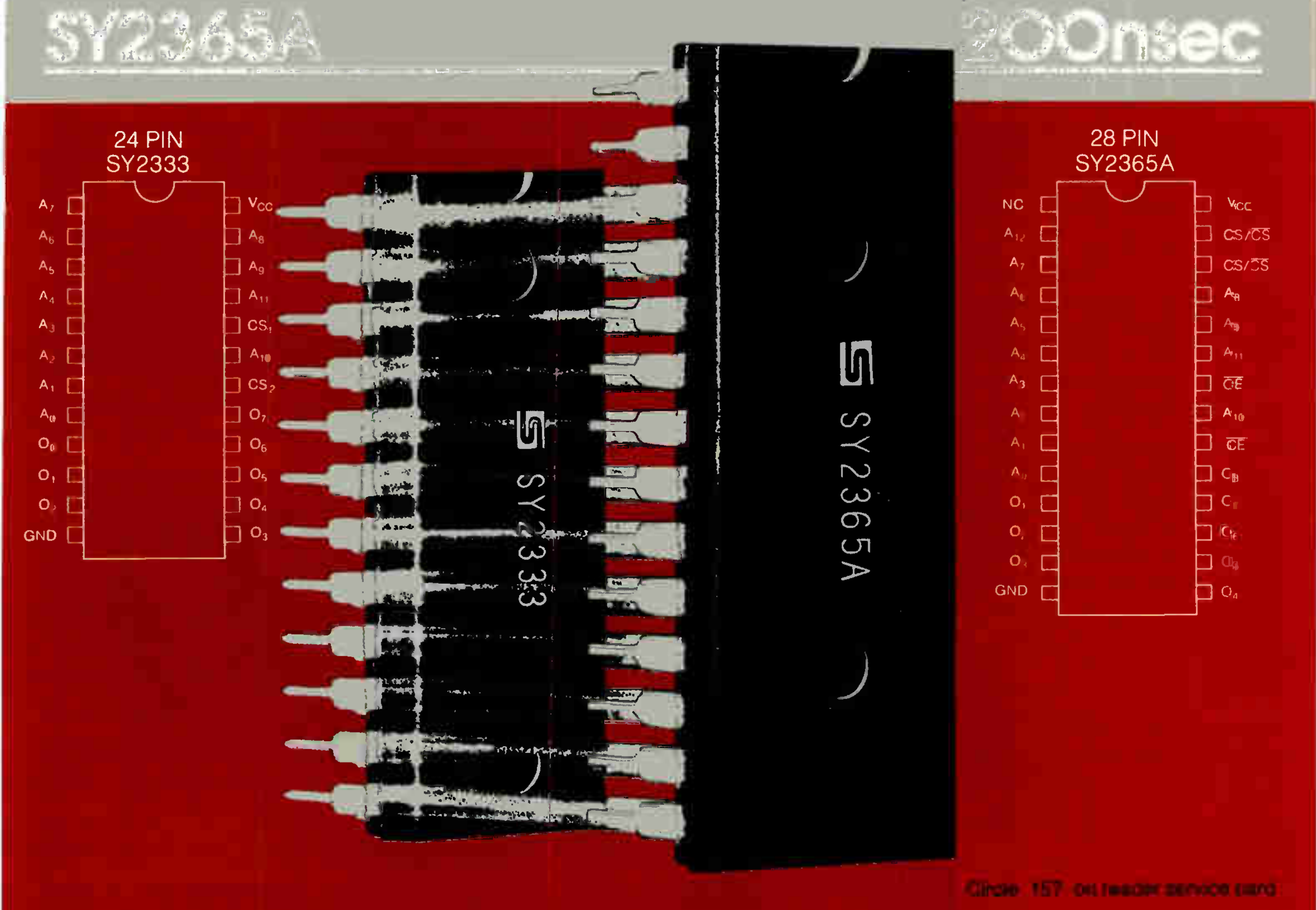


Relays have 0.3-Ω FET outputs

Line of ac and dc optically isolated solid-state relays get low on-state resistance from paralleled FET cells

by Larry Waller, Los Angeles bureau manager

Power field-effect transistor technology is being used in Teledyne Relays' line of optically isolated solid-state relays to lower the on-state resistance of the output to as little as 0.3 Ω. Minimizing the offset voltages at the outputs, the FET-based relays can be used in a number of low-level and power-switching applications now dominated by electromechanical reed-type relays, says Dennis Chabala, director of engineering at the Solid State division. Optically isolated, FET-based solid-state relays from the Opto-MOS line of Theta J Corp., Woburn, Mass., range from 2.5 to 65 Ω in on-resistance.

"Basically, multiple cells in the FET technology parallel resistance in relays and get the on-resistance down," says Chabala. Under development for two years, the Teledyne relays have proprietary hybrid microelectronic construction and may be driven by TTL or complementary-MOS logic inputs. All the relays have a third input terminal that is used in the latter case. The buffered inputs are specified to handle signals of 3.8 to 32 V.

A Schmitt trigger at the input increases the noise margin when C-MOS is used, according to Teledyne, preventing false triggering in noisy environments. The input logic circuits are protected from output voltage transients up to 1,000 V.

Package choice. The Teledyne relays come in two series, the 690 and -91 and the 685 and -86. The former series is housed in the firm's hermetically sealed low-profile Centigrid package. Otherwise electrically equivalent, the latter series comes in a larger hermetically sealed dual in-line package, which doubles power-dissipation capability, allowing 1.0-A loads to be carried in 80°C ambient conditions, according to the Teledyne engineer. For custom jobs, operation can be boosted to 5 or 10 A, he adds.

Both series include ac models rated to switch ±80-V loads and dc models with 80-V output ratings. The 685 is a dc relay rated to carry a 1.0-A load; it has 0.3-Ω typical on-resistance and a 3-ms turn-on time. Its ac counterpart, the 686, carries a ±700 mA load, has 0.6-Ω on-resistance typically, and turns on in 5 ms.

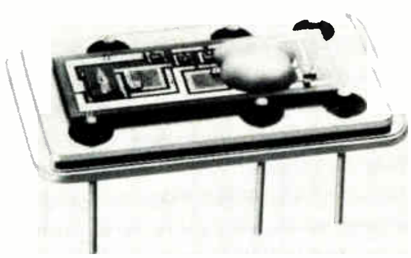
The 69X series has four members—the dc 690-1 and 690-2, and the ac 691-1 and -2. They are rated to carry, respectively, 250, 1,000, ±150, and ±700 mA, and have typical on-resistances of 1.2, 0.4, 2.4, and 0.8 Ω, respectively. Turn-on times range from 1.5 ms for the 690-1 to 5 ms for the 691-2.

The 69X series in the Centigrid package is intended for military uses where small size and reliable operation in high–electromagnetic-interference conditions are critical. But these qualities should provoke interest among the designers responsible for equipment with general-purpose analog and transducer signal switching, the company maintains.

An example of thermocouple or low-level (down to 100 μV) analog switching is a network of the relays that can multiplex signals to an instrumentation amplifier. "They can multiplex directly from microcomputer input/output ports or C-MOS ring counter circuits," points out Chabala. The relays can also set the gain of the instrumentation amplifier under microprocessor control, he adds. Other applications for the FET family include isolated line drivers, current-loop switches, servo- and synchro-resolver control, and data couplers. In power switching, the devices allow less power dissipation than does bipolar technology—for example, 30 mW compared to 2 W for a Darlington type, both carrying 1 A at 2 V.

The 100-unit price of the 690-1 is $41, and at 1,000 units, the unit price is $35.50. The 691-2 sells for $55.50 and $47.50 in like quantities. Samples will be available in September, with full production expected in October.

Teledyne Relays, 12525 Daphne Ave., Hawthorne, Calif. 90250 [338]



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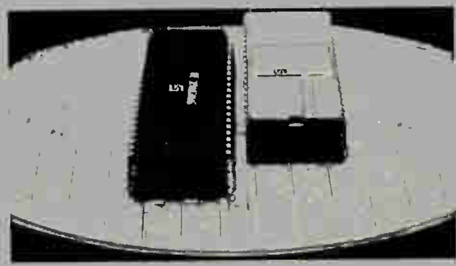

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Microcomputers & systems

256-K-byte board maps dynamically

Multibus-compatible memory uses 64-K dynamic RAMs, has error-correcting option

The BP-0300 memory board from NEC Microcomputers adds 128- or 256-K bytes of dynamic random-access-memory storage to Multibus-compatible 8- and 16-bit computer systems. The board incorporates NEC's μPD4164 n-channel MOS RAMs and includes error-detection and -correction circuitry as an option. The BP-0300 boards, which carry their own refresh circuitry, will range in price from $1,500 to $3,600 when they become available at the end of this month.

Besides accommodating 8- and 16-bit data buses, the BP-0300 can operate on 16-, 20- and 24-bit address buses. It also has an on-board memory mapper that can implement a variety of addressing capabilities, including dynamic memory mapping for multiuser and multitasking applications. In this the board is unique, claims Richard J. Weiner, manager of engineering for the NEC Microcomputer Products group. "No other Multibus-compatible memory board has this feature, as far as I know. The BP-0300 not only has it but also lets users implement memory mapping according to their particular needs."

NEC includes a μPD429 read-only memory in the BP-0300 package for fixed memory mapping; the ROM's eight memory-addressing patterns configure the board's RAM to eight different starting addresses under jumper or software control. Alternatively, the BP-0300 can also accept user's own ROM or erasable programmable ROM for programmed configuration of the board's 64 4-K-byte memory pages beginning at any page boundary.

Finally, an NEC μPD446 static complementary-MOS RAM can mount in the BP-0300 and direct dynamic, on-the-fly memory mapping in multitasking systems where the memory configuration continually changes. The BP-0300's memory-mapping capabilities address both 8- and 16-bit words, and are transparent to host central processing units, according to NEC's Weiner.

The optional error-detection and -correction circuitry corrects any single-bit errors and flags any multiple-bit errors that occur in memory. An on-board status register stores error-condition information, which the host CPU can access under program control. This information, which also is displayed by a bank of light-emitting diodes connected to the status register, includes identification of the error as either single- or multiple-bit, the location of the error in memory, and whether or not more than one error has occurred since the last CPU interrogation and resetting of the status register.

Correction chip. A special-purpose large-scale integrated circuit, along with 6 or 12 added memory chips on the 128- and 256-K-byte boards, implements error correction. The device generates and compares 6-bit check words in both read and write cycles to detect any mismatches between data values and their corresponding check bits. In the case of a single-bit error, the device inverts the polarity of the offending bit before it is transfered to the Multibus. Depending on its configuration, the BP-0300 can either send an interrupt to the CPU or reset the system in response to multiple-bit errors.

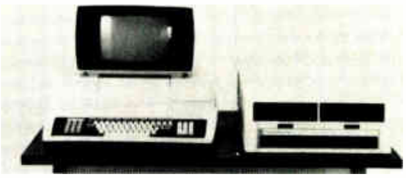
The boards have a 650-ns maximum read or write cycle time and a maximum access time of 450 ns (500 ns with error correction). The BP-0300 can operate on user-supplied battery back-up power; it has an isolated back-up power bus to minimize standby power drain.

Delivery initially will take four to six weeks. The firm plans to begin delivering from stock beginning this September.

NEC Microcomputers Inc., 173 Worcester St., Wellesley, Mass. 02181 [371]

TI development system has 64-K RAM, 4-MHz operation

The TMAM9000 single-user floppy-disk system is a low-end addition to Texas Instruments' recently introduced line of multiple-user Advanced Microprocessor Prototyping Lab (Multi-AMPL) development systems. Like others in the series, the TMAM9000 will support both current and future developments in TI technology. The tabletop system includes a TMS9900-based central processing unit, complete with keyboard and display, plus a separate



enclosure providing 2.2 megabytes of mass storage on two double-sided, double-density floppy-disk drives. The CPU has 64-K bytes of random-access memory and features 4-MHz operation. The disk drive unit offers 4 times the storage capacity and 10 times the data-transfer rate of previous FS990 AMPL systems. The software included is the 9000 Amplus system software, a package including the AMPL high-level debugging language, 9000 family assembler, screen editor, linker, text formatter, disk-conversion utilities, programmable read-only memory and erasable-PROM programmer utilities, and file and directory utilities. Available immediately, the basic system sells for $13,350.

Texas Instruments Inc., P. O. Box 202129, Dallas, Texas 75220 [373]

Board permits evaluation of NSC800 microprocessor

The NSC888 microprocessor board enables the user to evaluate the performance and features of the NSC800 8-bit P²CMOS microproces-

Price breakthrough: $499.

For a CMOS microprocessor development system.

Our new CDP18S693 costs less than any other 1802 microprocessor development system on the market. And the development system can even become your final target system.

The incredibly low $499* price includes:

- CDP18S601 computer Microboard.
- ROM/audio cassette controller Microboard.
- Five-card chassis and case.
- Detachable 5-volt power supply.
- Audio cassette tape I/O drive for mass storage.

You get these capabilities:

- Extended BASIC resident in ROM with full floating-point arithmetic.
- 2K-byte monitor program with extensive memory manipulation.
- RS232C or 20 mA terminal interface, up to 1200 baud.

Or, for $799,* you can get the CDP18S694. It has all the capability of the 693, plus:

- ROM-based 1802 Assembler/Editor.
- PROM Programmer board.
- A second cassette tape I/O drive.

System expansion:

- Expand your Microboard system capability, choosing from over 40 expansion boards and hardware accessories.
- Memory expandable to full 65K bytes.
- Virtually unlimited I/O expansion capability using any combination of analog and digital I/O boards.
- Run-time BASIC 3 firmware for final system configuration.

Develop software for any 1802-based component design, or for any Microboard system in BASIC or assembly language.

At these prices you can't afford not to get into CMOS.

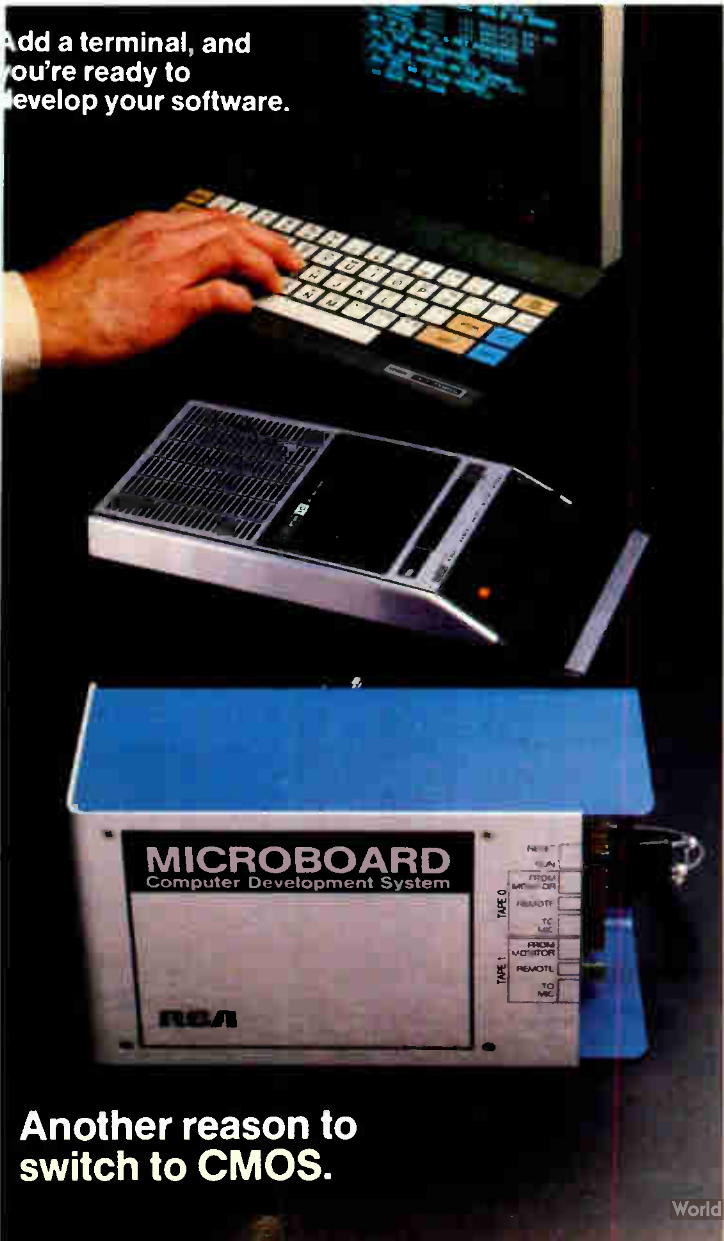
For more information, contact any RCA Solid State sales office, sales representative or distributor.

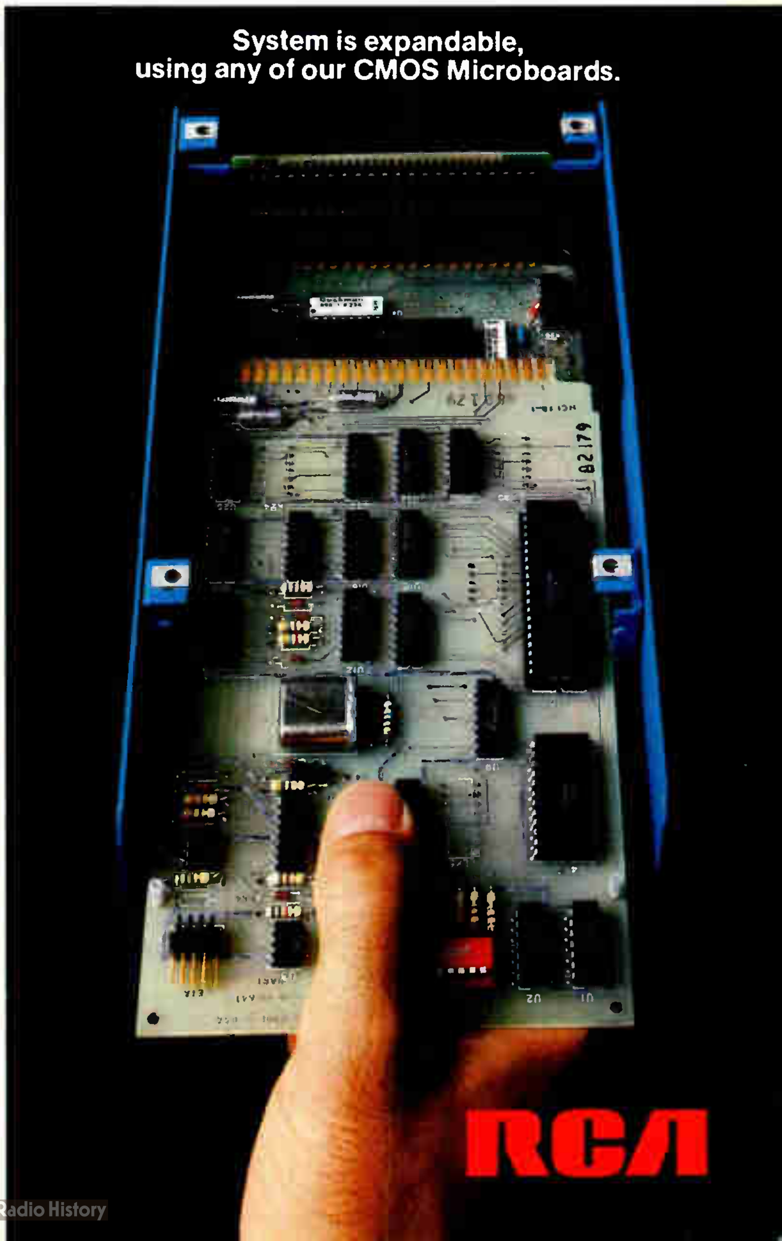
Or contact RCA Solid State headquarters in Somerville, N.J. Brussels, Belgium. Sao Paulo, Brazil. Hong Kong.

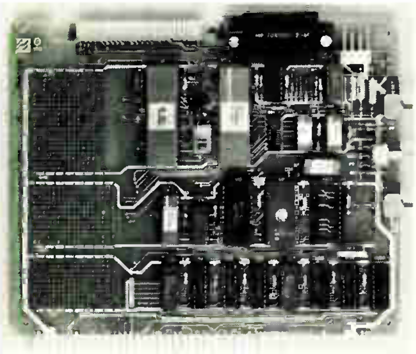
Or call Microsystems Marketing toll-free (800) 526-3862.

Circle 161 on reader service card

* U.S. optional distributor resale, single unit price.





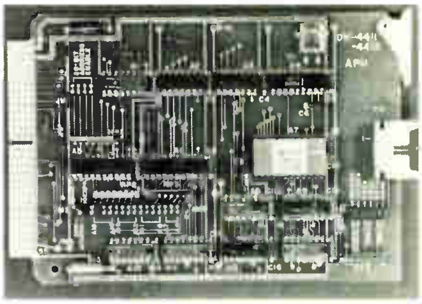


sor family. With the board, the user can write, debug, and execute an NSC800 program under control of a 2-K-byte monitor. Only the addition of a ±5-V power supply and an RS-232-C interface cable to the user's terminal are needed to begin the process. Included on the board are the NSC800 central processing unit plus random-access memory, timers, input/output lines, erasable programmable read-only memory, and interface components. Each board is $995, and delivery is in two weeks.

National Semiconductor, 2900 Semiconductor Drive, Santa Clara, Calif. 95051 [374]

Unit gives 32-, 64-bit floating-point functions

Desert Microsystems' latest STD Bus products are the DM-4411 and -4412 floating-point math boards. The 4411 is based on the AMD 9511 arithmetic processor unit, which features full floating-point math functions including most trigonometric and logarithmic operations. The 4412 is available with the AMD 9512,



which provides single-precision (32-bit) and double-precision (64-bit) floating-point arithmetic functions. Both have memory-mapped interfaces that permit the 9511/9512 stack to be read or written using the block move instructions of the 8088 and Z80 microprocessors. Both boards also connect all interrupt signals to an accepted STD bus interrupt connector. And both versions

are available in two speeds. In quantities of one to four, the price for either the 4411 or 4412 is $415 for the 2-MHz version and $475 for the 3 MHz version. Delivery is from stock.
Desert Microsystems Inc., Star Rte. 1, Box 1174-D, Pasco, Wash. 99301. Phone (509) 547-3397 [375]

Board 'fronts' for DS990s in distributed networks

The Bit Character Asynchronous Interface Module enhances the distributed-network performance of TI's DS990 computer systems by handling many protocols, speeds, and configurations. It contains an on-board TMS9900 microprocessor and semiconductor memory, both of which act to reduce the workload of the DS990 central processing unit. The memory includes 8-K bytes of read-only memory and 2-K bytes of random-access memory. BCAIM buffers multiple bytes of data in on-board memory before interrupting the system CPU. Each standard board is $900, $970 with a data-set cable. October shipping is planned.
Texas Instruments Inc., Digital Systems Group, P. O. Box 202146, Dallas, Texas 75220. Phone (512) 250-7305 [376]

Memory card transfers bytes or 16-bit words

Seattle Computer Products' SCP-110 64-K-byte IEEE S-100 memory card uses the new 100-ns Intel 2167 16-K static random-access memory. The new chip allows memory management functions of offset and protection to be performed with the firm's 8-MHz 8086 central processing unit without wait states. Its access time from address is 190 ns. The card performs both 8-bit and 16-bit transfers, switching automatically. It can ignore the extended address lines in systems that do not use them. Power requirements for an active board are 1.6 A at 8 V while an inactive card uses 0.8 A. The card uses 24-bit addressing, the upper 8 of which can be disabled. The list price is $1,295 with discounts for larger quantities. Delivery takes up to two weeks.
Seattle Computer Products Inc., 1114 Industry Dr., Seattle, Wash. 98188. Phone (206) 575-1830 [379]

Semiconductors

HAL series starts with seven parts

High-volume hard-array logic family adds standard parts to custom use of array logic

Continuing its assault on the ubiquitous Texas Instruments TTL Data Book, Monolithic Memories Inc. has used its hard-array logic technology [*Electronics*, June 2, p. 49] in creating seven new standard-function products. If the analogy holds that HALs are to PALs (programmable-array logic) as read-only memories are to programmable ROMs, then these special-function products represent to the HAL what a character generator represents to a ROM—that is, a high-volume subset of a general part class.

The first set of special-function HALs from MMI includes seven parts, each of which has been packaged in a 24-pin Skinny DIP and assigned a 7400 series part number. There is an octal counter (54/74LS461), a 10-bit counter (54/74LS491), a shift register (54/74LS498), a multimode register the firm calls a super interface (54/74LS380), a 16-to-1 multiplexer (54/74LS450), a dual 8-to-1 multiplexer (54/74LS451), and a quad 4-to-1 multiplexer (54/74 LS453).

With the exception of the 8-bit counter, super interface, and the 10-bit counter, each of the new parts corresponds to a function in the TTL Data Book. These functionally equivalent parts are listed as the LS100 series with the same last two digits as the MMI parts. The difference between these and the TI chips is that the MMI parts have doubled the density of the TI parts: MMI's quad 4-to-1 multiplexer contains twice the circuitry of TI's corresponding dual 4-to-1 multiplexer. The data book does have an analogous 16-to-1 multiplexer chip, but it is in a wider, standard dual in-line package instead of the Skinny DIP.

The synchronous 8-bit counter is similar to TI's 54/74LS161, which is a 4-bit counter, except that the MMI part adds three-state outputs and bus-structured pinouts. All the data-in lines are grouped together on one side of the DIP, and all the data-out lines are at corresponding positions on the opposite side. It has parallel load, clear, and hold capability and can be cascaded for larger counters. It also drives 24 mA, compared to 8 mA for the 54/74LS161.

Video. The 10-bit counter is also referred to as a video chip because it can handle the 9-bit resolution necessary to keep track of either a 512–picture-element horizontal or vertical video display. Production chips will reach 16-MHz speeds, more than fast enough to handle the 10-MHz required for normal graphics applications and the 12-MHz required for high-resolution graphics. Unlike the octal counter, the video chip can count both up and down.

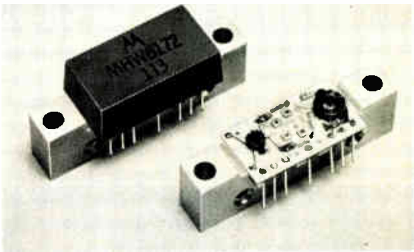
The "super interface," or multimode register, has no direct counterpart in the TTL Data Book. It is closest in function to a combination of 54/74LS registers numbered 374, 377 and 273, but it has additional advantages. Although the 374 is a three-state device, it cannot clear or enable a clock. The two-state 273 and 377 parts contribute the clear and the clock-enable functions, respectively, and all three chips can load true. MMI's 380 super interface may load either true or complement, as well as performing the three-state, clear, and clock-enable functions. It can also perform presets, which none of the three analogous chips can do.

Samples of these parts will be available this month, with volume production beginning in five weeks. They will initially be available in Cerdip J-type packages at commercial-grade 100-unit prices of $5.00 each for the multiplexers and $9.00 each for the registers. MMI plans to follow in October with N-type plastic packages, which will reduce the prices to $4.00 for the multiplexers and $7.00 for the registers.

Monolithic Memories Inc., 1165 E. Arques Ave., Sunnyvale, Calif. 94086 [411]

Wideband CATV modules handle 53 channels

A series of hybrid modules specifically designed for broadband community-antenna TV applications now have bandwidths as high as 500 MHz and are capable of handling 53 ultrahigh-frequency channels. Included in the seven-member series is the MHW6171 with a 500-MHz bandwidth and a minimum power gain of 16.7 dB at 50 MHz. With a 450-MHz bandwidth, the MHW5171 has a minimum power gain of 40 dB, and the MHW5122 has an 11.5-dB power gain. Maximum cross modulation for the series ranges from −54 to



−59 dB, and the minimum noise figure ranges from 6.5 to 9 dB. All modules offer a gain flatness of ±0.1 dB over their respective frequency bands. The modules are currently being released in sample quantities, with full production volume scheduled for the third quarter of 1981. Unit pricing is expected to be below $35 in large production quantities.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 244-6394 [413]

Chips replace wired circuits in dbx noise reduction system

Two chips replace the discrete circuitry for the voltage-controlled amplifier and root-mean-square detector on dbx Inc.'s noise reduction system. Though actual prices have not yet been decided, the chips should lower the per-channel cost of licensing dbx systems from its present

$3.50 to a figure below the going rate for Dolby systems. Using International Radio Consultative Committee weighting, the dynamic range of the dbx system is in excess of 100 dB. A dbx-equipped system provides 50-dB noise reduction compared with 20 dB for Dolby C. The dbx chips' frequency response is 30 Hz to 20 kHz ± 1 dB, and their total harmonic distortion is 0.5% typically, 0.1% from 30 Hz to 15 kHz.

Delivery of the chips is within 30 days of order.

dbx Inc., 71 Chapel St., Newton, Mass. 02195 [414]

8x60 controller converts RAM into first-in, first-out buffer

A single integrated circuit can convert standard random-access memories into large first-in, first-out buffer memories. With the 8x60 FIFO RAM controller, two asynchronous systems may be interconnected for buffered data-transfer rates exceeding 8 MHz. The 8x60 supplies an address up to 12 bits long to a user-selected RAM of the desired data width. FIFO depth is selectable by two control signals to any of four word values: 64, 256, 1,024, and 4,096. A four-signal handshake interface is provided for read and write control from the two communicating systems, as well as status signals to indicate full, half-full, and empty conditions.

The chip's inputs and outputs are standard TTL with the address outputs having a 16-mA drive capability. The 8x60 has no fall-through requirements (a timing period during which a part cannot be accessed). It is manufactured using Signetics' integrated Schottky logic (ISL) process and operates from a single power supply. One additional external dropping resistor provides a current supply to internal ISL. Available in 28-pin plastic dual in-line packages, the 8x60 is $26.25 each in 100s.

Signetics, 811 E. Arques Ave., P. O. Box 409, Sunnyvale, Calif. 94086. Phone (408) 739-7700 [415]

Package for MOS FETs allows greater pc board densities

An end-stackable four-pin dual in-line package for low-power MOS field-effect transistors allows automatic handling and insertion equipment to place switching components closer to logic components on printed-circuit boards for higher packing densities than TO-3 and TO-220 packages can provide. Therefore the Hexdip series eliminates lead forming and hand insertion. The devices respond to TTL– or complementary-MOS–level drive signals. Both n- and p-channel devices have a drain-to-source breakdown voltage of 60 or 100 V, a resistance of 0.6 or 0.8 Ω, power dissipation of 1 W (quad), and a drain current of 0.8 or 1.0 A for a single device. Unit prices for the 4-pin IRFD110 parts range from $2.59 to $6.04 in quantities of 1,000. Prices for the 16-pin IRFE110 devices (all n- or all p-channel, or a combination) range from $10.88 to $25.36 in like quantities.

International Rectifier, 233 Kansas Street, El Segundo, Calif. 90245 [416]

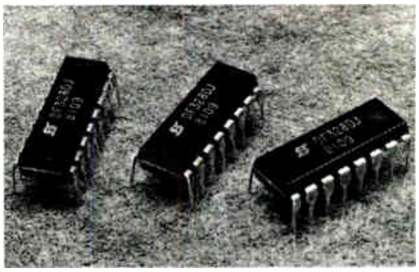
PROM family offers 600-mil, high-density 300-mil versions

Ten new Advanced Micro Devices 2,048-by-8-bit programmable read-only memories use the company's proprietary high-density ion-implanted micro-oxide process, Imox II. Five are offered in standard 600-mil, 24-pin dual in-line packages, and five are available in high-density 300-mil, 24-pin dual in-line packages. Developed as part of AMD's generic PROM series, they all employ AMD's proprietary platinum silicide fuse. All have a maximum access time of 50 ns. The Am27S190 and Am27S290 have open-collector outputs while the Am27S191 and Am27S291 offer three-state outputs. Imox II also is used to produce versions of these parts with guaranteed maximum access times of 35 ns. The Am27PS191 and Am27PS291 are three-state power-switched versions that satisfy more stringent power limitations. Switched via the chip-select line, both devices recover their full operating capabilities in less than 10 ns with an address access time of 50 ns at most. In the power-down mode, current drain is 90 mA. Prices in 100-unit lots start at $38.15 each for the Am27S190/191 family, and $51.65 for the Am27S290/291 family. They are available now from stock.

Advanced Micro Devices Inc., 901 Thompson Place, Sunnyvale, Calif. 94086. Phone (408) 732-2400 [417]

C-MOS loop-disconnect dialer remembers, redials 20 digits

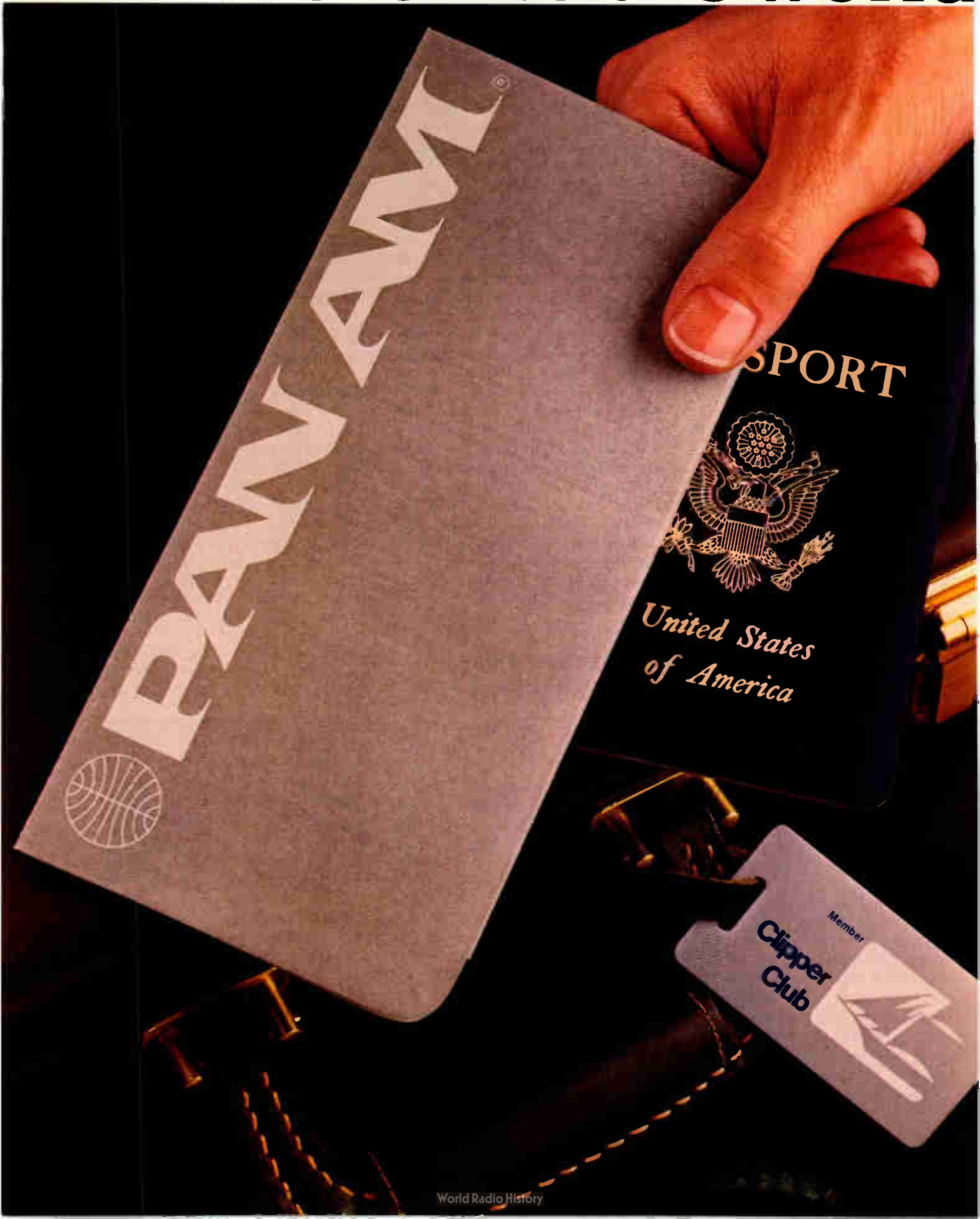
The DF328 low-power, monolithic complementary-MOS loop-disconnect dialer contains all the logic needed to interface the standard double-contact keyboard with a telephone system requiring loop-disconnect signaling. It stores up to 20 digits and offers automatic redialing by pushing the number key. Using negligible standby current and low operating current and requiring an unregulated supply voltage of 2.5 V, the DF328 interfaces with long telephone lines. Component count is minimized in using the DF328 by



the inclusion of an on-chip clock and high-impedance pull-down terminations for programming inputs, as well as pull-up terminations for direct interfacing with the keyboard. The Siliconix DF328 is priced at $3.20 each in lots of 100 and is available from stock.

Siliconix Inc., 2201 Laurelwood Rd., Santa Clara, Calif. 95054. Phone (408) 988-8000 [418]

We're #1 to the world



Instruments

Scope shows line from TV frame

U. S. and European versions of dual-trace, 100-MHz scope trigger on frame-sync signal

Aiming at what it sees as a growing market for specialized test instruments in the professional television service field, Philips Test & Measuring Instruments Inc. is introducing a specially tailored version of its PM3263 100-MHz oscilloscope [*Electronics*, Nov. 9, 1978, p. 143]. With the PM3263X, service technicians can dial up any line of a TV frame for viewing.

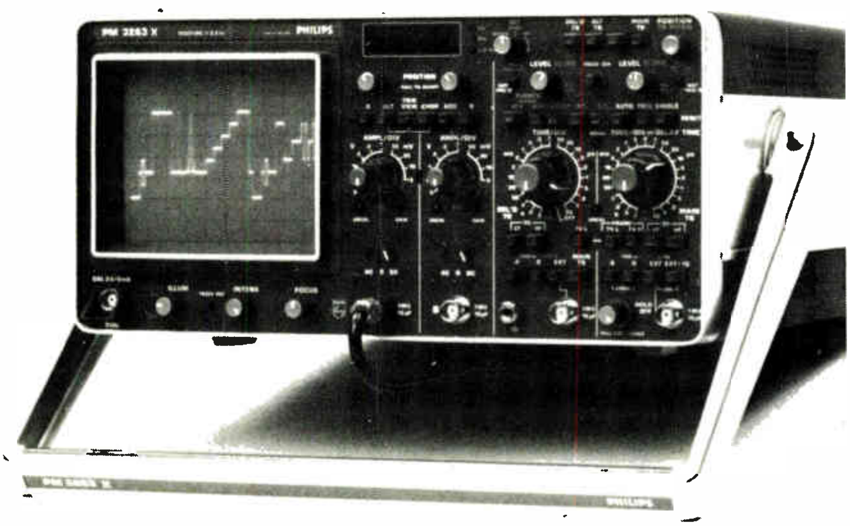
The new dual-trace scope has been designed to trigger automatically on a TV frame's synchronization signal. Setting the scope's event counter to the number of a desired line, which is shown on a light-emitting-diode display, causes the scope's processor to delay the trace until the processor has counted to that line. Two versions of the scope are available: the North American version conforms to the National Association of Broadcasters' standards, while the European version conforms to the line-numbering standards of the European Broadcast Union and of the International Radio Consultative Committee of the International Telecommunications Union.

Coupled with the unit's dual-trace capability and its main and delayed time bases, the line selection capability gives the user an in-depth view of the TV signal. For example, the main time base can be used to present a trace of an entire line while the delayed time base is set so that a particular portion of the line is visible in detail. Similarly, the scope can be set so that the entire frame is viewed at the same time as the individual line, or the frame can be divided into two so that each half is displayed on a separate trace.

According to the company, the scope should be particularly valuable for all types of video signals, including radar, video disk and cassette recorder systems, and teletext. Its full general-purpose 100-MHz performance allows the unit to be used for non-TV measurements.

The PM3263X is priced at $4,595; deliveries are in eight weeks.

Philips Test and Measuring Instruments Inc., 85 McKee Dr., Mahwah, N. J. 07430 [351]



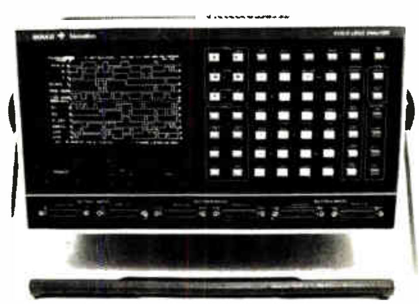
48-channel, 100-MHz analyzer has 16 levels of trace control

According to Ed Jacklitch, marketing manager for Gould Inc.'s Biomation organization, "a logic analyzer is not a field service tool, it is a design tool." The company's latest product, the K101-D, therefore offers the sophisticated triggering and clocking needed by today's designer to capture data from its 48 100-MHz channels.

Jacklitch points out that digital systems will process several megabytes of data per second, "quantities so vast that they have previously defied convenient analysis." So the K101-D provides 16 trace-control levels, with the parameters for each level individually selectable by means of separate menus. For each level, then, the user can define the stop, jump, advance, and trace events and thus take from complex data streams at each level only the information that is germane to his or her task. Data is stored in a 515-by-48-bit memory.

The analyzer can make both time- and data-domain measurements simultaneously using both internal and external clocks. Internal clocking is possible with resolution to 10 ns, with glitch capture better than 5 ns. Twelve separate clock input lines are arranged as six sample clocks (edge active) and six latch enables (level active).

The menus are extremely easy to set up, saving designers considerable time. Moving a cursor to each item in the menu allows the user to scroll through the possible selections for that item at the push of a button.



Captured data can be displayed in binary, octal, hexadecimal, decimal, ASCII, EBCDIC, and sign. Probes to provide device-associated mnemonics will be offered in the future. A graph display permits an overview of program behavior. The K101-D is priced at $23,500 and shipments will begin in September.

Gould Inc., Biomation Division, 4600 Old Ironsides Dr., Santa Clara, Calif. 95050. Phone (408) 988-6800 [352]

Analyzer examines, modifies registers and memory

The CAS-11 analyzer does not require a card slot in the LSI-11–based system it is testing. With the device the user can halt the central processing unit, single-step it, run in real time, and run with system data periodically collected and displayed or modified. It can also examine and modify CPU working registers and any of the memory locations, even if resident in system random-access memory. The CAS-11 provides a 40-bit breakpoint function, a 256-machine-cycle trace memory, and a substitute program memory for the system under test. The breakpoint circuits consist of a breakpoint condition register, a breakpoint mask register, and a pass-count register. The CAS-11 analyzer can identify such malfunctions as a loose cable connection or an inadvertent interface foul-up following routine maintenance. Delivery of the $4,650 analyzer is 30 days after receipt of order.

Electro-Design Inc., 7364 Convoy Court, San Diego, Calif. 92111. Phone (714) 277-2471 [354]

DEC-based Fastprobe network supports three test stations

The Fastprobe network, which supports up to three 4500 test stations, increases test and repair throughput by dedicating one or more test stations to production testing while others are used for fault isolation and repair. Since edge-connector testing approaches do not thoroughly exercise and test microprocessor-based boards and systems, the test station uses three test methods—in-circuit emulation, time-domain analysis, and signature analysis—to provide real-time functional testing and fault isolation. The Fastprobe test network consists of a Digital Equipment Corp. LSI-11/23 computer, dual floppy disks, 20-megabyte hard disk, control terminal, expanded applications software, 180-character-per-second printer, and up to three 4500 test stations and defect printers. Options include a modem and series 200 or 9508 program development system. The network can be operated under constant computer control for production testing and factory repair or in a stand-alone mode for use in depot repair facilities and in the field to diagnose system problems. The Fastprobe network is $90,000 and is available 90 days after receipt of order.

Millennium Systems Inc., 19050 Pruneridge Ave., Cupertino, Calif. 95014. Phone (800) 538-9320 [355]

Sweep generator covers 75 to 110 GHz

The 47726H solid-state millimeter-wave sweep generator covers the entire W band of 75 to 110 GHz. It consists of a full-band sweep source, a leveling loop, and a full-band sweep plug-in. The sweep source includes three Impatt sweep oscillators and an electrically actuated waveguide switch. The leveling loop consists of a ferrite modulator, directional coupler, and a flat broadband detector. The full-band sweep plug-

in contains all the controls needed for the sweep sources and leveling loops.

The unit is designed to plug into the Hewlett-Packard 8620C mainframe or the 8350A mainframe with high-resolution digital displays. Leveled power output is 1 mW minimum across the 75- to 110-GHz bandwidth, and frequency linearity is typically 1%. Compatibility with the IEEE-488 bus is optional. The 47726H is $32,560, with delivery 40 days after receipt of order.

Hughes Aircraft Co., Electron Dynamics Division, 3100 West Lomita Blvd., Torrance, Calif. 90509. Phone (213) 517-6400 [356]

Thor 1 simulates noise for test and evaluation

The Thor 1 high-performance noise generator tests computers and other electronic equipment in the design stage. Thor 1 induces controlled amounts and types of noise into a test environment, and on the basis of this simulation, users may evaluate a product's noise-susceptibility or performance under actual operating conditions. The unit will induce either radiated emission or conducted discharge, and two operating modes provide the user with a choice of single-shot or repetitive burst modes, both of which produce relatively flat noise spectrums well into the megahertz region. It is battery-operated (30 W) to maintain noise isolation from the user's power line; the unit is equipped with a battery charger. Optional trigger and scope modules are available for special applications. Thor 1 is priced at $2,985, and delivery is in 30 days.

International Control Systems Inc., Lakeview Office Park, 2622 West Lake St., Minneapolis, Minn. 55416 [358]

Components

Sensor controls display brightness

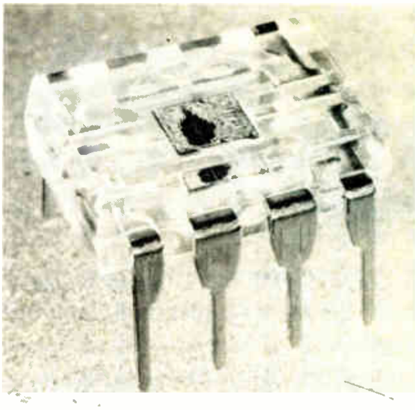
IC with photodiode produces analog or digital output to adjust display to ambient light

TRW Optron has integrated a 2,500-mil² photodiode with 10 other circuits to produce a single-chip light-level control sensor. The integrated circuit, designated the OPL100, will sense ambient light levels and then automatically adjust displays—such as light-emitting diodes and incandescent and vacuum fluorescent devices—for easier viewing. Initially, the bipolar chip is being targeted at automotive markets, but TRW Optron indicates the OPL100 is also well-suited for similar applications in aircraft, military equipment, testers, television sets, home appliances, and other consumer and industrial products.

Housed in an 8-pin plastic dual in-line package, the OPL100 will cost $5.31 each in quantities of 1,000. The automatic light-level controller, which is the densest circuit in TRW's Photologic line, will also be offered in an eight-pin flat-window TO-5 hermetic package at a slightly higher cost, says William Nunley, marketing development manager for TRW Optron. (No price has been set on this version.)

Located on the OPL100 chip are: a photodiode, a high-gain temperature-compensated amplifier, an operational amplifier, four comparators, a latch, random logic, an output driver, and a voltage regulator. An off-chip fixed or variable resistor can also be used to set the control reference points of the integrated circuit with respect to the ambient light levels. Pulse-width modulation is used to adjust displays from 0% to 100% of maximum brightness.

Capable of operating in a supply voltage range of 4.5 to 24 V, the device has a relatively constant supply current of 12 mA. The OPL100 also features a totem-pole output, which will source 50 mA at a minimum supply voltage of 2 V and sink 10 mA at a maximum of 0.3 V.



In the eight-pin DIP versions, the chip—which measures 108 by 92 mils—is encased in a clear molding compound, MG18, made by the Hysol division of Dexter Corp.

In addition to allowing external sensitivity adjustments with an off-chip resistor, the OPL100 has both analog and digital outputs and synchronous or asynchronous modes of operation.

TRW Optron, a division of TRW Inc., 1201 Tappan Circle, Carrollton, Texas 75006. Phone (214) 323-2200 [341]

Analog chip suits many jobs

Multifunction IC has two transconductance amplifiers, voltage follower, comparator

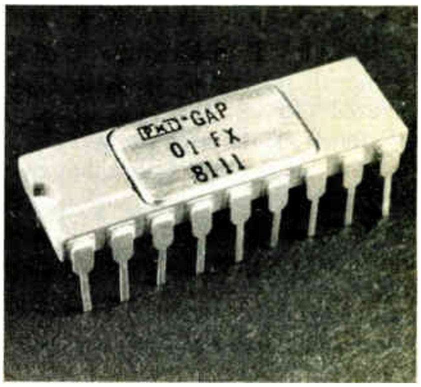
The unique architecture of the GAP-01 signal-processing chip equips it to satisfy a wide spectrum of possible analog functions with its single 18-pin package. The high-level integration of this multipurpose part brings high performance, simpler design, greater reliability, and lower cost to a broad range of analog systems.

Under external control, digital logic steers signals through the device in such a way that it can be configured for different applications [*Electronics*, April 7, 1981, p. 121]. The actual circuitry features two differential-input transconductance amplifiers, two low-glitch current-mode switches, an output-buffer amplifier, and a precision comparator on an 8,600-mm² chip. The control signals switch either amplifier's output into the voltage follower, creating two digitally selectable signal paths through the device. Feedback selects the magnitude and sign of the gain through the two channels.

Double duty. An external capacitor supplies closed-loop frequency compensation and doubles as a holding capacitor in sample-and-hold applications. The on-chip comparator rounds out the analog package for cost-effective applications in data conversion.

The GAP-01 can be wired as a two-channel operational amplifier, multiplexer, or sample-and-hold amplifier; an absolute-value function generator; a precision half-wave rectifier; a synchronous demodulator; and a host of other commonly needed functions.

The amplifiers have a low 3 mV of offset voltage error, achieved by selectively shorting zener diodes across trimming resistors during wafer testing. Their 400-kHz bandwidth gives a settling time to 0.1% accuracy of 41 μs for a 20-V step. The input bias current is 50 nA, and



the common-mode rejection ratio is 86 dB.

Comparator performance is also well above average, with a fast 200-ns response time and a wide differential input voltage range of 24 V. The comparator's output level is set by external resistors, for the greatest possible noise immunity as well as direct interfacing to all standard logic families.

Internal current switching is accomplished in a mere 50 ns; charge transfer onto the external capacitor during switching typically falls below 1 pC and is constant over a 20-V input signal range. These characteristics exceed those of most dedicated sample-and-hold amplifiers. Sample-and-hold applications also benefit from the voltage follower's high-impedance field-effect-transistor inputs, which include a current cancellation circuit that limits input bias current to 10 nA, even at 125°C.

The BQ-grade device operates over the −55° to +125°C range, and the FQ grade handles −25° to 85°C. Devices processed to MIL-STD-883 and an FP grade for the 0° to 70°C range are planned. Sample devices are available now. Pricing for 100 piece lots is $12.50 for the BQ grade, and $7.50 for the FQ device.

Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, Calif. 95050. Phone (408) 727-9222 [342]

Low-power bi-FET op amps have high input impedances

The LF441 single, LF442 dual, and LF444 quad operational amplifiers made with National's Bi-FET II technology have extremely low power consumption, typically 150 μA per amplifier, and junction field-effect transistor inputs with impedances, typically, of 10^{12} Ω. These devices combine bipolar devices and FETs on the same chip, joining the low input bias and offset characteristics of FETs to the high performance of bipolar transistors. According to the company, when compared to industry-standard op amps not made with the combined technologies, the LF441, -442, and -444 have a higher input impedance than parts with comparable specifications—a gain bandwidth of 1 MHz, a slew rate of 1 V/μs, and a gain of 25 V/mV.

The op amps have low input noise voltage and current of 40 nV/Hz$^{1/2}$ and 0.01 pA/Hz$^{1/2}$, respectively. The LF441 and -442 feature input offset voltages of 0.5 mV and 1 mV maximum, respectively, and input offset voltage drift of 10 μV/°C maximum.

Available in 8-pin plastic dual in-line packages and TO-8 metal cans, the LF441 is priced at 50¢ and the LF442 is 95¢ in quantities of 100 or more. The LF444, in a 14-pin package, sells for $1.55 in lots of 100.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 737-5000 [343]

Vacuum fluorescent display has 256-by-64 dot matrix

Consisting of 16,384 0.4-mm^2 dots, the itron DM256X4A vacuum fluorescent dot-matrix display panel is arranged in a 256-by-64 configuration—an active area 166.15 mm long and 41.35 mm wide. Randomly addressable, the unit can display bright, high-resolution, cursive and block alphanumeric messages in a variety of shapes and sizes, graphic-line and filled-in area pictorializations, symbols, and geometric patterns in a number of combinations that can be scrolled from side to side or up and down. These images can be read from a distance and at wide viewing angles, even when subjected to intense ambient light.

The DM256X64A can be used for computer-generated graphing, plotting, and image display; automotive instrument panels; signature verification systems; and word processors. The unit displays bright blue-green images over a temperature range of −10° to +55°C and can be stored from −20° to +70°C without degradation.

In quantities of one to nine, the display panel is priced at $290 each; in quantities of 10 to 99, at $255; and at $225 each for 100 and up. Delivery is within 60 days of receipt of confirming purchase order.

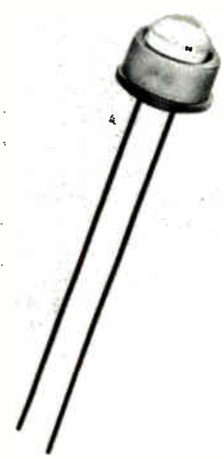
Noritake Electronics Inc., 22410 Hawthorne Blvd., Torrance, Calif. 90505. Phone (213) 373-6704 [344]

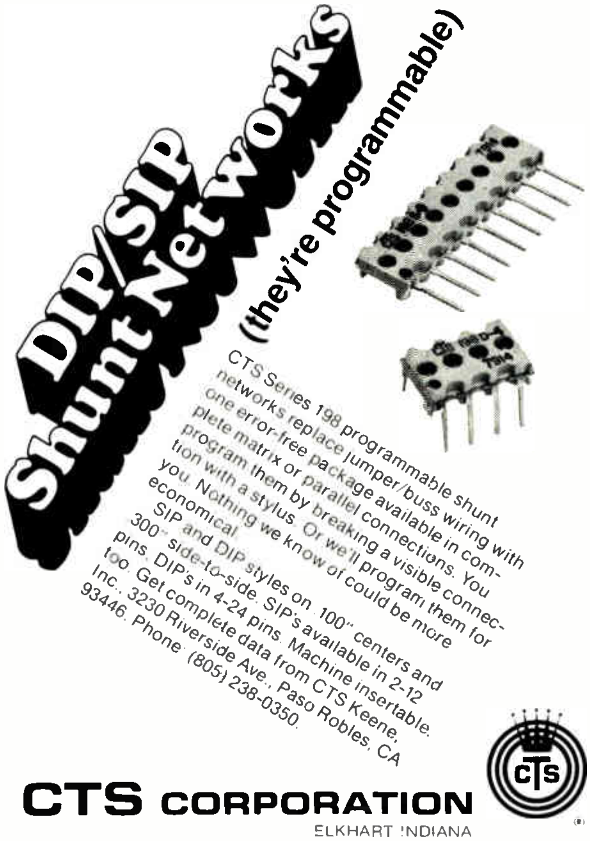
Collimated light source improves encoder's performance

Dynalite, a gallium arsenide light-emitting diode, is used in applications that require a high degree of collimation, such as optical encoders. It reduces the influence of disk-to-reticle distance variations and improves the waveform, ripple, duty cycle, and resolution of the linear or optical encoder assemblies.

The 940-nm infrared light source features a precision lens; it provides a consistent light pattern and high output power. The high-intensity spot it develops is large enough to accommodate a standard six-cell silicon-array sensor. A typical beam angle is 5°, with a spot diameter of 0.180 in. at 0.250 in. from the lens.

Dynalite has an operating temper-





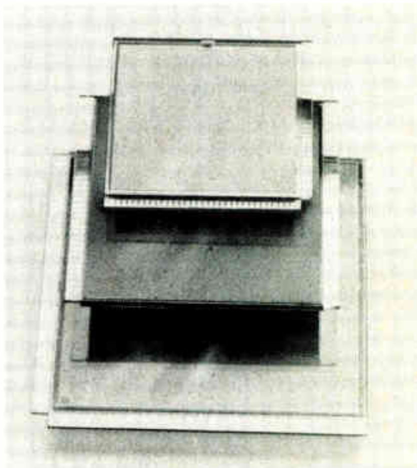
ature of −55° to +90°C. It is designed in a custom package consisting of a TO-46 header and a molded lens cap and is available in five models with typical radiated power levels of 1.5, 2.5, 3.5, 4.5, and 6.0 mW. Prices for Dynalite are $1.49 each in quantity to original-equipment manufacturers. Delivery will be in 30 days.

Sensor Technology Inc., 21012 Lassen St., Chatsworth, Calif. 91311. Phone (213) 882-4100 [345]

Liquid-crystal displays offered in selection of colors

Seiko Instruments' line of multiplexed liquid-crystal displays has been expanded to include models 201 and 203 to be used in products that require a low-power visual display, such as toys, games, calculators, digital instrument displays, computer peripherals, consumer appliances, and medical and telephone add-on equipment. These LCDs have a life expectancy of typically seven years, a standard operating voltage of 3.0 or 5.0 V, and an operating-temperature range of −10° to +60°C, depending upon the model.

The models are available in numeric and alphanumeric formats and can be specially designed to meet specific requirements. They are offered in a variety of shapes and sizes up to a 6-by-8-in. panel and come in a variety of display colors. Colored polarizers, reflectors, and



liquid-crystal materials are optional.

The model 201 is priced at $10 in quantities of 1 to 29 and $8 in lots of 30 to 99. The 203 sells for $11 in quantities of 1 to 29 and $9 in 30 to 99 piece lots. Delivery will be in 70 days.

Seiko Instruments USA Inc., 2990 W. Lomita Blvd., Torrance, Calif. 90505. Phone (213) 539-8777 [346]

Active filter modules used for antialiasing applications

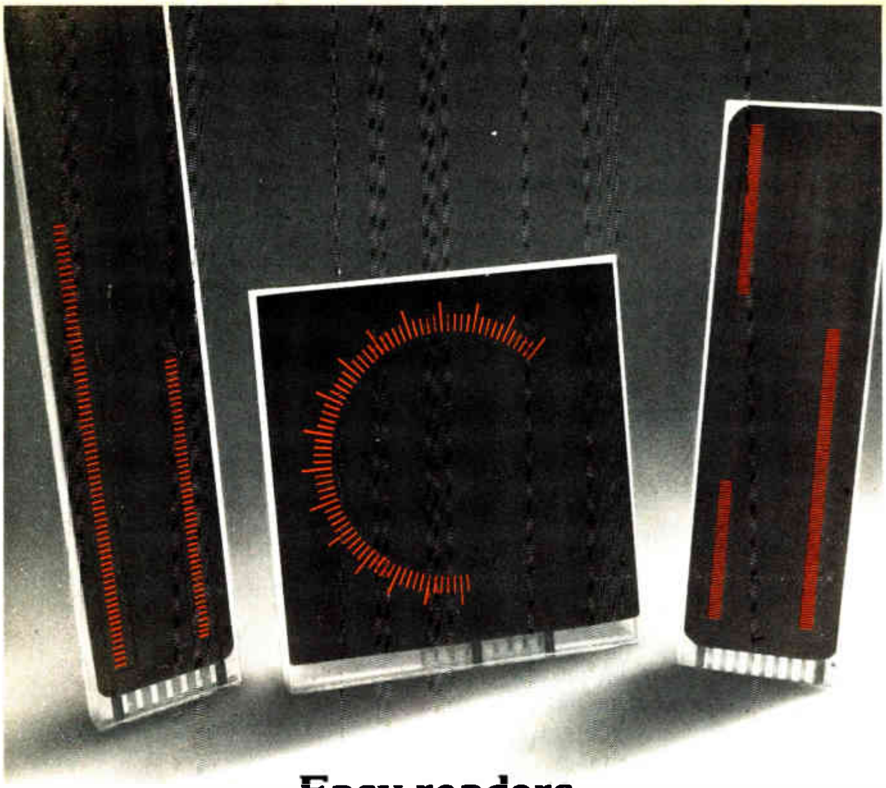
Designed for antialiasing applications, such as data-acquisition systems and applications requiring Elliptic (Cauer), Butterworth (maximum flatness), and Chebyshev and Bessel (linear phase) characteristics, are two active filter modules, the APL-6 and APH-6.

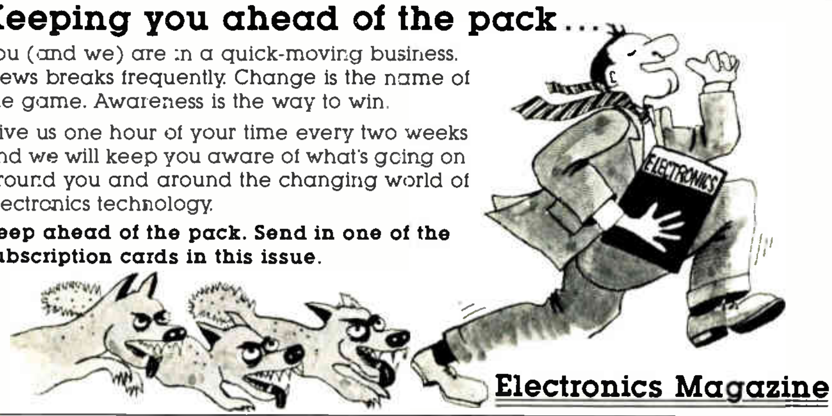
The APL-6 is a six-pole active low-pass filter that passes frequencies up to a specified cut-off frequency and attenuates those above. Its standard cut-off frequency is 10 Hz to 100 kHz. The APH-6 is a six-pole active high-pass filter that passes frequencies above a specified cut-off frequency and attenuates those below. Standard cut-off frequency range is 2 Hz to 50 kHz; the upper 3-dB cut-off point in the pass band is 200 kHz.

The units measure 1.35 by 2.75 by

0.6 in. and are supplied in dual in-line packages. They require a power supply current of ±35 mA and are priced at $150 in quantities of 3 to 10. Delivery takes two to six weeks.

A. P. Circuit Corp., 865 West End Ave., New York, N. Y. 10025. Phone (212) 222-0876 [347]





New products/materials

Easypoxy K-45 is a two-part epoxy adhesive. It has a 5-min pot life and develops high-strength bonds in 2 to 3 hours. Bonded assemblies can generally be handled after only 10 to 15 minutes. In 24 hours at room temperature, it develops a tensile shear strength of greater than 2,500 lb/in.^{2} on aluminum. Easypoxy comes in repair kit, quart, gallon, and 5-gal units. In lots of 1 to 9, 6.8-oz kits are $5.20 each. A 90-lb 5-gal pail is priced at $414. Delivery takes from one to two weeks.

Conap Division of Wheelabrator-Frye Company, 1405 Buffalo St., Olean, N. Y. 14760. Phone (716) 372-9650 [476]

Two new series of Lamiglas thermal- and flame-barrier cable wraps are made without halogenated fire retardants. Employing halogen-free adhesives, the laminated wraps use glass paper bonded to polyester film for the thermal barriers and glass paper bonded to glass scrim for the flame barriers. Halogens are avoided because of their corrosive effects on surrounding metallic components after ignition. The wraps protect conductors in service and equipment cables under heat or fire and thus permit equipment to continue operating with cable-circuit integrity during sudden or sustained external increases in temperature.

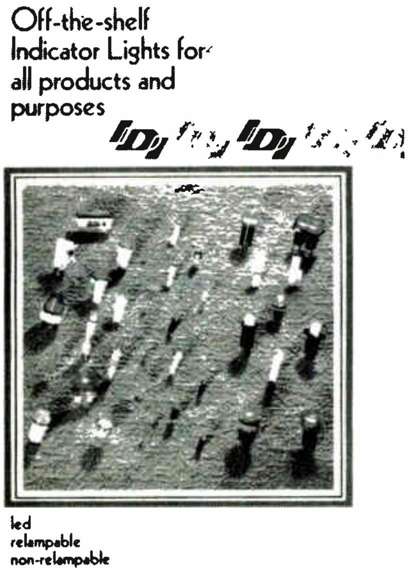
Sun Chemical Corp., Facile Division, 185 Sixth Ave., Paterson, N. J. 97524. Phone (201) 684-1000 [477]

A new thick-film materials system for membrane switches and other flexible circuits is made of screen-printable conductors and compatible organic insulators. Conductors in the system are filled with either silver or carbon powders depending upon application requirements. Fired conductors may be flexed into 180° creases. Conductors are available with conductivity ranges from 20 mΩ/square with processing temperatures from 60° to 150°C depending upon requirements. The insulators are designed for use as dielectrics, and for crossover and cover coating applications.

Cermalloy Inc., 320 Long Island Expressway South, Melville, N. Y. 11747 [478]

New literature

Indicator lights. "Off-the-shelf Indicator Lights for All Products and Purposes" is a 48-page catalog that covers Industrial Device Inc.'s line of indicator lights. It is divided into four sections—light-emitting diodes, indicator lights whose lamps are replaceable, those whose lamps are not, and standard variations for custom-designed applications. Each section contains photographs, dimensional drawings, mounting information, technical specifications, and ratings. It provides information on the company's Safe-T-Klip test lead clips, test accessories, and engineer's kits of indicator light samples. An index helps designers locate the kind of indication light they need. For a free copy of the catalog, request form FDH from Industrial Devices Inc., Edgewater, N. J. 07024 or phone (201) 224-4700. Circle reader service number 421.

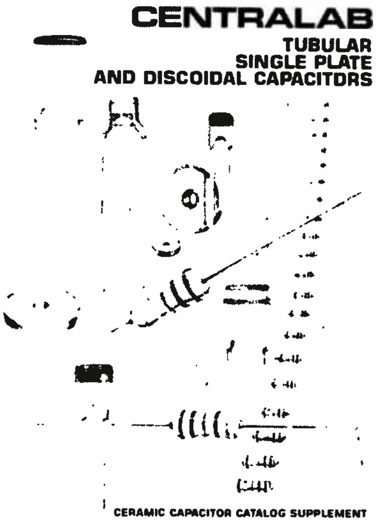


Integrating spheres. A 20-page technical report, "Integrating Sphere Performance," by D. J. Lovell, a Labsphere staff scientist, discusses the three basic parameters—throughput, efficiency, and stability—that are used in describing the performance of an integration sphere, which can be employed to determine the total radiation of a lamp or to attenuate an intense source. The report is priced at $5.00 and can be obtained by contacting Philip B. Lape at Labsphere, P. O. Box 70, North Sutton, N. H. 03250; (603) 927-4255 [422]

Engineering adhesives. Stalok anaerobic adhesive/sealants, the 7400 series cyanoacrylate adhesives and the M890 acrylic adhesives, are the topics of an eight-page catalog entitled "Bostik Engineering Adhesives." It discusses their application techniques, curing and priming times, surface activities, breakaway and prevailing torque, and their uses. Graphs showing their performance and chemical resistance characteristics are provided, as are military specifications. Also included is a discussion on pipe sealant with Teflon and Redi-Form Gasket. For further information or to obtain a copy of the catalog contact Broadview Chemical Corp., 2910 S. 18th Ave., Broadview, Ill. 60153, or phone (312) 626-4416. [423]

Software information. The sixth edition of Digital Equipment Corp.'s "Engineering Systems Software Referral Catalog" provides software analysis and design information for engineering and industrial manufacturing firms. It contains descriptions, licensing, purchasing, and availability data for over 300 software packages developed by independent software vendors to run on Digital Equipment computer systems. Disciplines covered include structural analysis and text processing. For a free copy of the 350-page publication, write to the Engineering Systems Group, MR1-1/M75, Digital Equipment Corp., 200 Forest St., Marlboro, Mass. 01752, for the attention of the SRC manager. [425]

Ceramic capacitors. A 12-page catalog contains electrical, mechanical, and marking specifications, dimensional data, and operating parameters for Centralab's line of ceramic tubular, single-plate, and discoidal capacitors. It features a selector chart to guide in the selection and application of the capacitors, a section on how to order, and the Electronics Industries Association industry classification system and standard designations and codes. Copies of the catalog may be obtained by writing to Centralab Inc., a North American Philips Co., 5855 N. Glen Park Rd., P. O. Box 2032, Milwaukee, Wis. 53201. [424]



Mercury relays. General-purpose relays from 10 to 60 A, general-purpose contactors from 80 to 150 A, high-voltage contactors, and time-delay relays and flashers are discussed in a 16-page catalog, "Durakool Mercury Relays." Typical coil data is provided in a chart form and dimensions are given in U. S. and metric standards. Ordering information and explanations of product codes are also given. For more information, contact Durakool Inc., P. O. Box 280, Elkhart, Ind. 46515, at (219) 264-1116. [426]

Time and frequency. The FTS 4050, 4010, 4000, and 5000 cesium-beam frequency and time standards, the FTS 6016 digital clock, the FTS 1000 series of quartz crystal oscillators, the FTS 1050 and 1150 quartz frequency standards, and the T-200 satellite timing receiver are described in a 19-page catalog. It discusses Frequency & Time System's capabilities in both commercial and high-reliability products. A list of manufacturer's representatives is included. For a copy of the catalog, write to Frequency & Time Systems Inc., 34 Tozer Rd., Beverly, Mass. 01915. [427]

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Products Newsletter

Delayed C-MOS 8048 arrives in volume

Having resolved masking layout problems that delayed commercial availability of its complementary-MOS version of the 8048 n-channel single-chip microcomputer, NEC Microcomputers Inc., of Japan, is going to market with the μPD80C48 and quoting 12- to 14-week deliveries. The Wellesley, Mass. marketing office says NEC is the first out with such a part and reports good volume-production yields. **NEC has dropped its 1,000-piece-lot price to under $10 per unit;** it also carries a $1,000 read-only memory masking fee. The part draws 10 mA maximum at 6 MHz.

TI continues quarterly 7000 series introductions with the TMS 7040

Look for Texas Instruments Inc. to add a new member to its 8-bit, single-chip microcomputer family every three months. This one is the TMS 7040, which **has 4-K bytes of read-only memory and sells for $9.40** each in orders of 1,000. The 7040, the third member of the TMS 7000 line [*Electronics*, Jan. 27, p. 107] is now available in sample quantities. Production lots will be available later in the third quarter. The 7040's size is 35,000 mil^2, compared with 28,000 mil^2 for the 7020.

Perkin-Elmer machines supported by Mostek's 256-, 512-K-byte boards

Mostek Corp. is expanding its line of add-in memory board products to include support **for Perkin-Elmer 3220 and 3240 minicomputers.** The MK8032, which costs $4,200 in single quantities for a 256-K-byte version and $7,995 for the 512-K-byte model, uses Mostek's 16-K and 64-K dynamic random-access memory chips. The memory card, which is the Carrollton, Texas, firm's first add-in board for Perkin-Elmer computers, contains on-line/off-line switching and access light-emitting diodes.

Comparator chip allows 7-μs, 12-bit a-d conversions

The CMP-05 from Precision Monolithics Inc., Santa Clara, Calif., satisfies the need for a monolithic voltage comparator with the speed and accuracy required for under 7-μs, 12-bit analog-to-digital conversions. **The unit has an offset voltage of 100 μV, a drift of 1.5 μV/°C, and a response time of 18 ns with 100-mV overdrive.** Commercial and industrial operating temperature ranges are available in a variety of package styles and pricing begins at $4 in 100-unit lots.

Service to translate IBM disk files

Watch for Altertext Inc.'s August introduction of a disk-file translation service **making stores from IBM's System 6 compatible with IBM's new Displaywriter.** The two IBM office systems presently are incompatible, but not only would the Boston, Mass. firm's service allow them to share files, but it also would enable file sharing with systems from DEC, Wang, and Vydec. Also due soon is a service for converting files into and out of Xerox format. The service would cost a minimum of $100 with price based on the number of disks to be translated.

Socket boards interface popular mini- and microcomputers

Robinson Nugent Inc. will be coming out shortly with a series of socket boards for interfacing with many popular mini- and micro-computers. **The boards will be wired with the Quick Connect technique** wherein insulated wires are routed through special insulation-piercing terminals to make a gas-tight connection. The New Albany, Ind., company will supply boards for Digital Equipment Corp.'s computer interfaces, Intel's Multibus, the S-100 interface, and the Apple II interface.

Career outlook

Help wanted everywhere

The electronics community is being bombarded by gloomy predictions and dire warnings about the current and future shortages of engineers, computer scientists, and technicians. Now, the American Electronics Association has come up with statistical fuel for the argument. Contained in a survey entitled "Technical Employment Projections," the numbers offer few surprises.

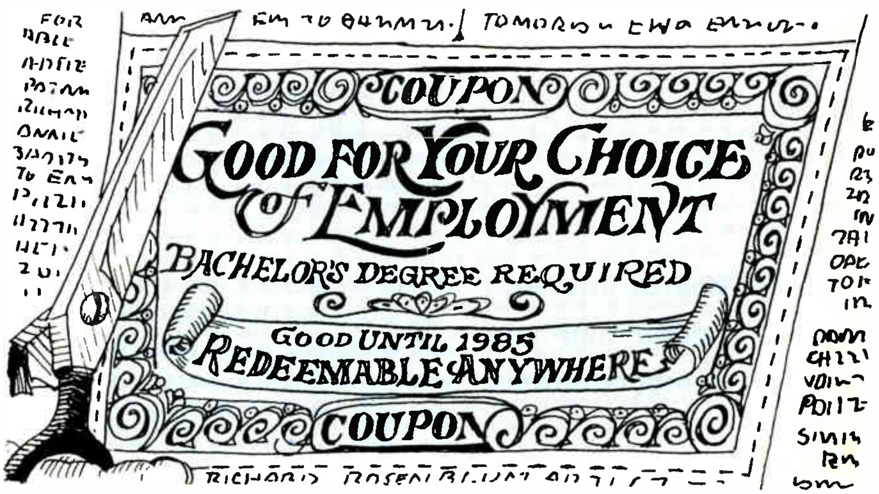
The 198-page report is the result of responses from 671 electronics firms [*Electronics*, June 30, p. 46], or a third of the electronics industry, in AEA's estimate. It is what the AEA calls "a bittersweet concoction," as it projects a robust future tempered by recent real-world layoffs by Texas Instruments Inc., Mostek Corp., and others. Many respondents hedged their 1981 projections, which were for a 22% increase overall, by saying that they were postponing several hirings until 1982.

The projections, which run through 1985, show growth of more than 100% in several job categories. Laser technicians lead the pack with an increase of 228%, a demand that perhaps indicates that the laser industry has finally come of age.

Bridge post. Another relatively new position, the electronics engineer technologist, also shows a dramatic increase. The position is defined as a bridge between technicians and engineers, and the firms surveyed project over 4,200 openings, 113% more than are currently employed. Other rapid growth areas: software-related positions, field-service technicians, and electrical engineers each show job projections of well over 100% and will require a large number of new employees.

Regionally, according to the report, the Sun Belt sections lead the way. Of the 671 respondents, those firms in the Southwest predict the most job openings, with over 28,500 by the end of 1985, and the Southeast is the percentage leader with a 22.6% rise in jobs, or about 13,500 new slots. The West, New England, and the Middle Atlantic region should continue their growth in technical positions. The Middle Atlantic states expect over 20,000 openings. New England projects nearly 17,500 new positions. As for individual states, California leads the nation with over 96,000 new positions by 1985. Texas, Massachusetts, and Colorado follow with about 13,800, 10,900, and 10,800, respectively.

Action slated. "The survey is to verify the manpower shortage and to help us get a handle on how large it is," says Pat Hill Hubbard, manager of technology training and careers. The figures have been given to universities and government agencies and are being used by an 11-member panel created by the AEA to examine engineering education [*Electronics*, April 21, p. 312]. The panel will use the results to help shape a plan of action at a July 15 meeting and recommend a program it judges industry could support. -Terry Costlow



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Director, US Army Signals Warfare Laboratory
ATTN: DELSW-MP
Vint Hill Farms Station
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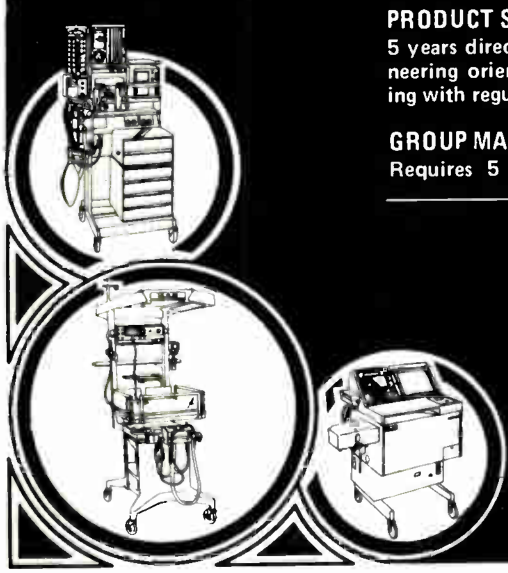

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