JUNE 30, 1981

CAN EPITAXY BUILD A BETTER 64-K RAM?/103

Supercomputer designs its successor/106

Process yields new current highs for IC regulators/111

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Electronics®

The Pentagon Connection
PLUGGING INTO TECHNOLOGY

9. Circuit Testing Update/No. 9 in a series from Hewlett-Packard.

HOW CAN YOUR MICROPROCESSOR BOARD HELP TEST ITSELF?

It's ironic. The very intelligence that makes your products excel can also be the obstacle that makes testing difficult. Why? Because those intelligent microprocessors are difficult to model. And until they're put to work via code, they're no smarter than any other piece of silicon. Can they be awakened and used to test themselves? Let's look at some of today's testing techniques and see.

Alternatives for testing microprocessor boards.
Board testers available today generally use one of four approaches:

1) Simulator board testing. This is an edge-connector and guided probe testing technique that relies on patterns from a simulation model. The processor is usually removed from the board, and input patterns applied. Output patterns are then compared with those predicted by the simulator. If the patterns match, the support logic is judged good. Next the processor is inserted and different patterns are applied. Now the outputs are compared to those predicted based on the original model plus a high-level software model of the processor. If those patterns match, the entire board is said to be good. Excessive time can be consumed generating both high-level models and testing software.

2) In-circuit testing. Using a bed-of-nails fixture, contact is made with each logic circuit on the board, including the μP. Pulses are applied to input pins of each device. Outputs are compared to those predicted from device truth tables supplied by manufacturers. These libraries are programmed for common device configurations and must often be modified for actual configurations.

3) Comparison testing. In this edge-connector and guided probe method, a known good board must be available as a reference. The known and unknown are initialized, synchronized and then are compared by applying preprogrammed instructions or patterns, or by stimulating with pseudorandomly generated pattern sets. If the outputs match, the unknown board passes.

4) Processor-based testing. This technique uses the intelligence of the μP on the board. The board is powered up and operated at speeds up to 10 MHz using preprogrammed test code resident in the test system or on the board itself. The on-board μP executes this code to exercise the address and data buses, and support circuitry. Key nodes are monitored with signature analysis to detect faults.

Why does HP use processor-based testing?
Our experience in testing μP boards has revealed several benefits of processor-based testing. That's why we've incorporated it into our 3060A Board Test System with the High Speed Digital Functional Test option.

First of all, boards are tested at speed, with all components, buses and control lines operating in modes similar to actual use conditions. The result? Ability to test pins which are not exercised unless the processor is executing instructions (Fig. 1), plus detection of faults related to the address and data bus structure and timing faults.

Examples of Processor Pins Testable Only With Software

	8085		6800	Z80
Interrupts	INTR TRAP	RST 7.5 RST 6.5 RST 5.5	$\overline{IRQ}$ $\overline{NMI}$	$\overline{INT}$ $\overline{NMI}$
Control Outputs	S_0 S_1 $IO/\overline{M}$	$\overline{RD}$ $\overline{WR}$	VMA R/W	$\overline{M1}$ $\overline{RD}$ $\overline{WR}$ $\overline{HALT}$
Other	SID SOD			

Fig. 1

In addition, processor-based testing permits fault detection using Signature Analysis (SA), which is complimented by new software in the digital functional testing package. SA allows rapid fault isolation to the component level on active bi-directional buses. That means high throughput in production.

Furthermore, with the programming aids available from HP, functional test program development time is minimized for μP, memory and IO boards. For example, you can either modify existing routines provided by HP, build your own stimulus routines using HP-supplied building blocks, or develop stimulus programs on a development system and download to the 3060A. The bottom line of processor-based testing is fast test program development, high throughput, and high yield at the final product level.

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To find out how processor-based testing can benefit you, write: Hewlett-Packard, 1820 Embarcadero Road, Palo Alto, CA 94303. Or, call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.

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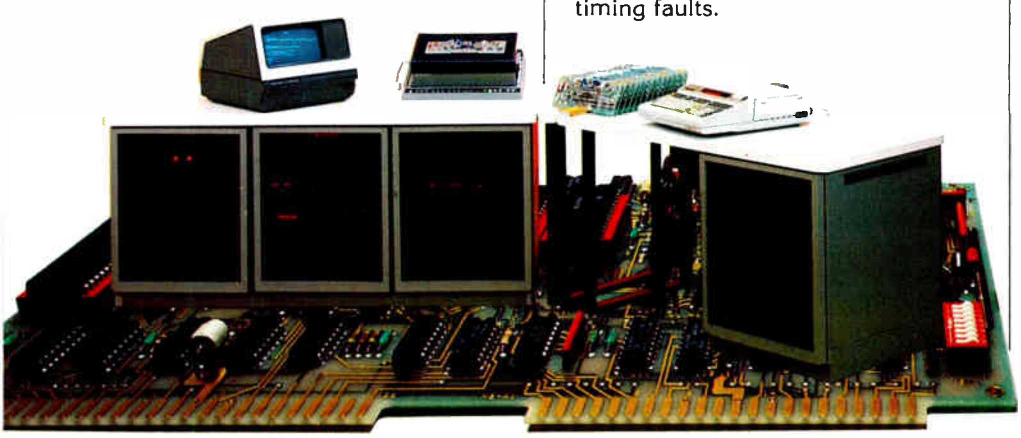

HP Circuit Testers— The Right Decision

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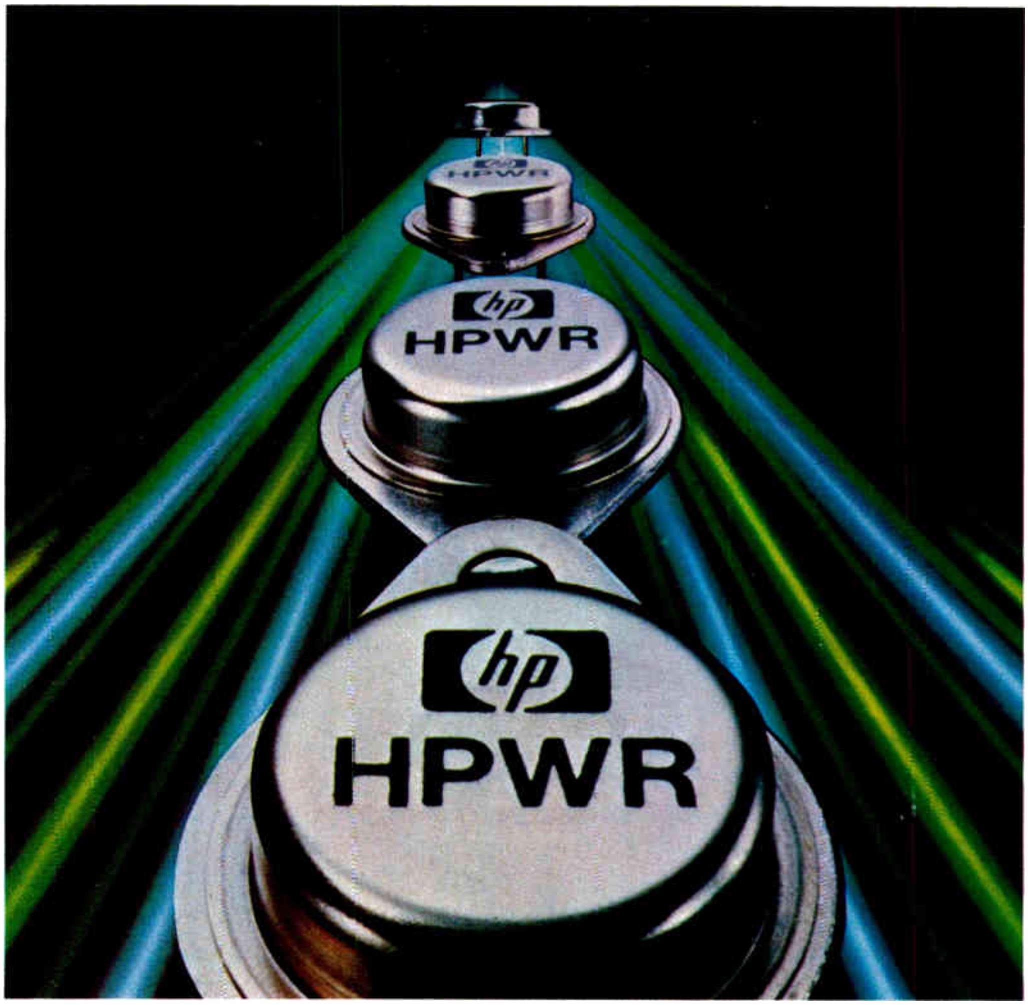

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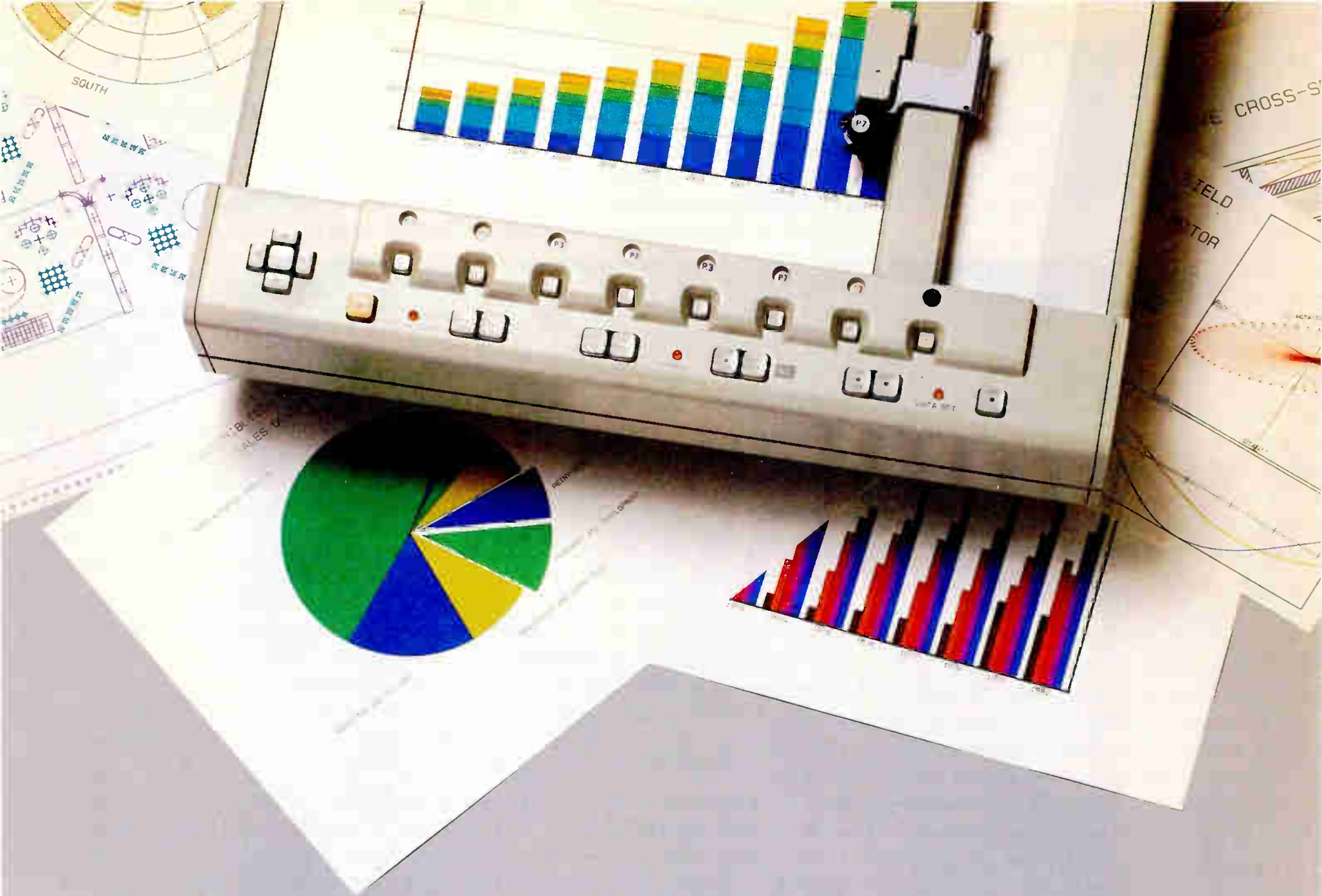

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Electronics
The International Magazine of Electronic Technology
Vol. 54, No. 13 • June 30, 1981

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Electronics

Highlights

Cover: What the U. S. military buildup means for electronics, 88

Claiming a need to answer military developments in the Soviet Union, the Reagan Administration is going full speed ahead with its plan to strengthen the U. S. armed forces. Of course, the bigger defense budget promises both larger and more contracts to be awarded, and this Inside the News report details what is in store for electronics firms.

The cover illustration is by Sean Daly.

Epitaxy controls harmful stray charge in large MOS RAMs, 103

With dynamic MOS random-access memories now up to the 64-K level, minor problems have become major ones. Superfluous charge, which can be caused by the rapid switching of address signals or by alpha particles, is one of these problems. But it can be effectively countered by building a RAM in a lightly doped epitaxial layer, enabling a heavily doped substrate to sweep away the stray charge that can upset valuable data.

CAD system enlists supercomputer in building its better, 106

An advanced, hierarchical computer-aided design and manufacturing system was employed in creating the fastest such machine currently available. The software provides for simulation by a supercomputer to ensure that the new one will perform as planned.

Making virtual memory easy for microsystems, 119

Because it expands a physical main memory into a larger logical address space, virtual memory is a welcome addition to microsystems—and hardware support for such a scheme is one way to eliminate most of its drawbacks of added complexity. Here, a 16-bit microprocessor adds an instruction-abort mechanism and teams up with a memory management chip for relatively fast and simple implementations of either segmented or paged virtual memories.

Large-scale integration moves into hybrid s-d converters, 124

Hybrid synchro-to-digital converters are one of the latest products to gain from large-scale integration. By substantially reducing the chip count and therefore the number of interconnections, custom LSI devices have bestowed on these converters their customary benefits of increased reliability, smaller size, and lower power consumption.

And in the next issue . . .

Electron beam probes very large-scale integrated circuits . . . a holographic checkout scanner . . . a fast gate–turn-off thyristor for high-power switching . . . a one-chip digital correlator . . . time-domain reflectometry for nonuniform cable lengths.

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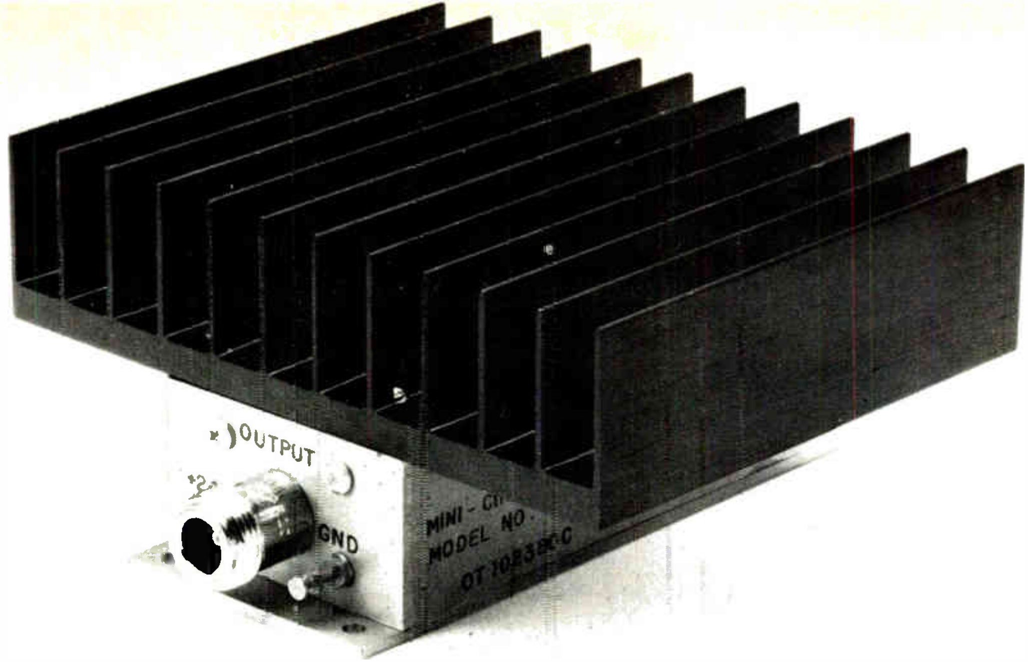

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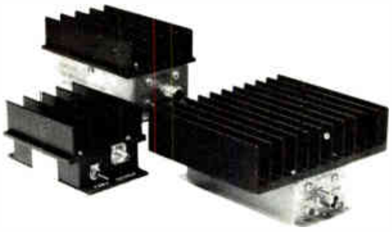

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Publisher's letter

Billions of dollars will soon be anted up as the Reagan Administration begins the mammoth military buildup the President promised during his election campaign. And the U. S. electronics industries stand to garner a significant share of the huge pie being baked by the Secretary of Defense Caspar W. Weinberger and his cost-conscious troubleshooter, Deputy Secretary of Defense Frank Carlucci.

To size up the dimensions of this new military thrust and to gauge its impact on the electronics industries, our veteran Pentagon watcher, senior editor Ray Connolly, with the help of our far-flung bureaus, interviewed scores of Department of Defense officials, military commanders in the field, program managers, policy makers, and manufacturers, not to mention numerous congressional staff members who have a hand in controlling the purse strings. The result is the comprehensive Inside the News report beginning on page 88.

According to Ray, the Pentagon is finding a great deal of interest in military programs in the electronics community, both from experienced contractors and from companies that have traditionally shunned military contract involvement.

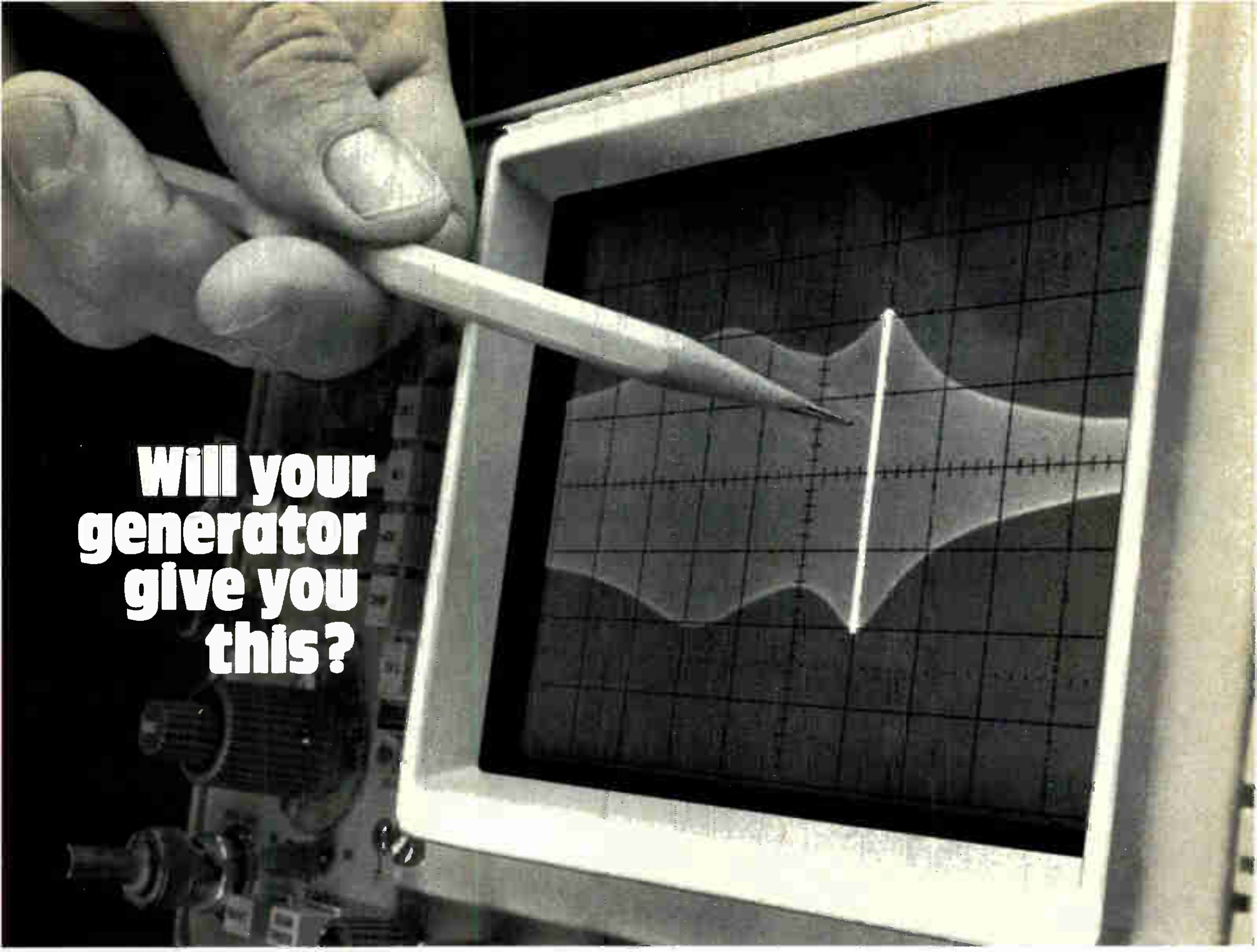
"It's probably because of the current softness in many areas of the commercial electronics market," says Ray, "and the participants in these markets are looking for some kind of hedge. But while the Department of Defense is finding this strong interest encouraging in the short term, they are also a bit leery about the longer-term prospects. They wonder if these newcomers will demonstrate the staying power required in this business by committing the manpower and plant space for the lengthy periods that will be demanded."

Ray, who has been covering the Washington scene for *Electronics* since 1969, doubling as our bureau chief and our military/aerospace editor, tells of worries about other aspects of the military buildup. For example, his report shows widespread concern over the potential impact of the program on engineering manpower, which is already in severely short supply.

But there is admiration for some of the innovations in contract management being sought by Weinberger and Carlucci in the interests of reducing waste and speeding contracts to fulfillment. Many of the proposals adopted by the two officials have been sought by industry for a long time; they include eliminating hundreds of Defense Department regulations and directives and increasing the Pentagon's risk sharing with contractors. Also, the emphasis is shifting toward the acquisition of simpler, more cost-effective weapon systems using less risky technology, in order to get them out into the field faster with less maintenance required.

"Reporters like me who have been around Washington a long time," says Ray, "have a distinct feeling of *déjà vu* these days. In the past, we've seen many other attempts of administrations to get their arms around the defense establishment, all failures. We remember Kennedy's Defense Secretary, Robert McNamara, and his Whiz Kids, and recently Harold Brown under Carter—all coming in with new ideas for getting better defense for fewer dollars.

"There are a lot of skeptics around, but most are willing to give the new guys a chance. They've got to learn to work with the seasoned bureaucracy, which knows how the system works. But they don't have a lot of time." According to Connolly, the new Weinberger-Carlucci rules will have to show results fast to retain the confidence of industry and the Congress. Ironically, the unrealistic inflation factors imposed on the DOD by Director of the Office of Management and Budget David Stockman may be their biggest obstacle to success.



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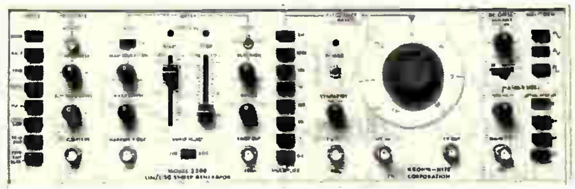

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Readers' comments

Amateurs training amateurs

To the Editor: Your article "Educators flunk on innovation" [May 19, p. 231] points out a great failing of the engineering education system in this country. When Prof. Van Valkenburg complains that we are producing electrical engineers who have not been taught some of the fundamental concepts of our profession, he is agreeing with a claim I have made for many years: all too often, the college professors who teach EEs have had no industrial experience. They know eight different ways to calculate the curl of a vector, but they cannot trigger an oscilloscope. This results in the unhealthy situation of having amateurs training amateurs.

However, it is possible to correct these shortcomings, and Van Valkenburg and his Accreditation Board for Engineering and Technology are the key. What is so terrible about insisting that, as a prerequisite for accreditation, a substantial number of EE faculty have experience working in industry? (I do not mean the one-day-a-week consulting done by the academics.) If this condition is not met, the ABET should refuse to accredit the institution.

I find it ironic that working EEs support the ABET through dues paid to the Institute of Electrical and Electronics Engineers, and yet it still functions as an old buddy network—you accredit my school and I'll accredit yours. Until this changes, we will continue to produce engineers without the breadth of knowledge necessary to survive in a competitive world.

Irwin Feerst
Massapequa Park, N. Y.

The perils of xenophobia

To the Editor: The April 21 Electronics Review discussing the employment of foreign engineers in electronics firms in the U. S. ["IEEE urged to act on alien hiring," p. 42] gives the impression that such hiring is injurious to the electrical engineering profession, as it displaces domestic talent with underpaid foreigners. Anyone who has been on the front line of professional technical recruit-

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ment knows that experienced people are scarce these days.

The Modicon division of Gould Inc. has responded to this situation by supplementing its aggressive domestic hiring with recruiting in the United Kingdom. The results to date have been extremely gratifying, as we have tapped a valuable resource. The engineers from the UK are being paid salaries directly competitive with salaries we pay to U. S. nationals, and the net effect is beneficial to electronics engineers: by applying an underutilized talent pool from abroad to help our firm develop the products it needs in order to grow, we are helping to expand the electronics industries and create additional employment opportunities.

I am aware of several other firms that have experienced similar success in overseas recruiting. It would be self-defeating to cut off this channel so long as our domestic labor pool cannot fill the demand.

Dennis Picker,
Gould/Modicon Division
Andover, Mass.

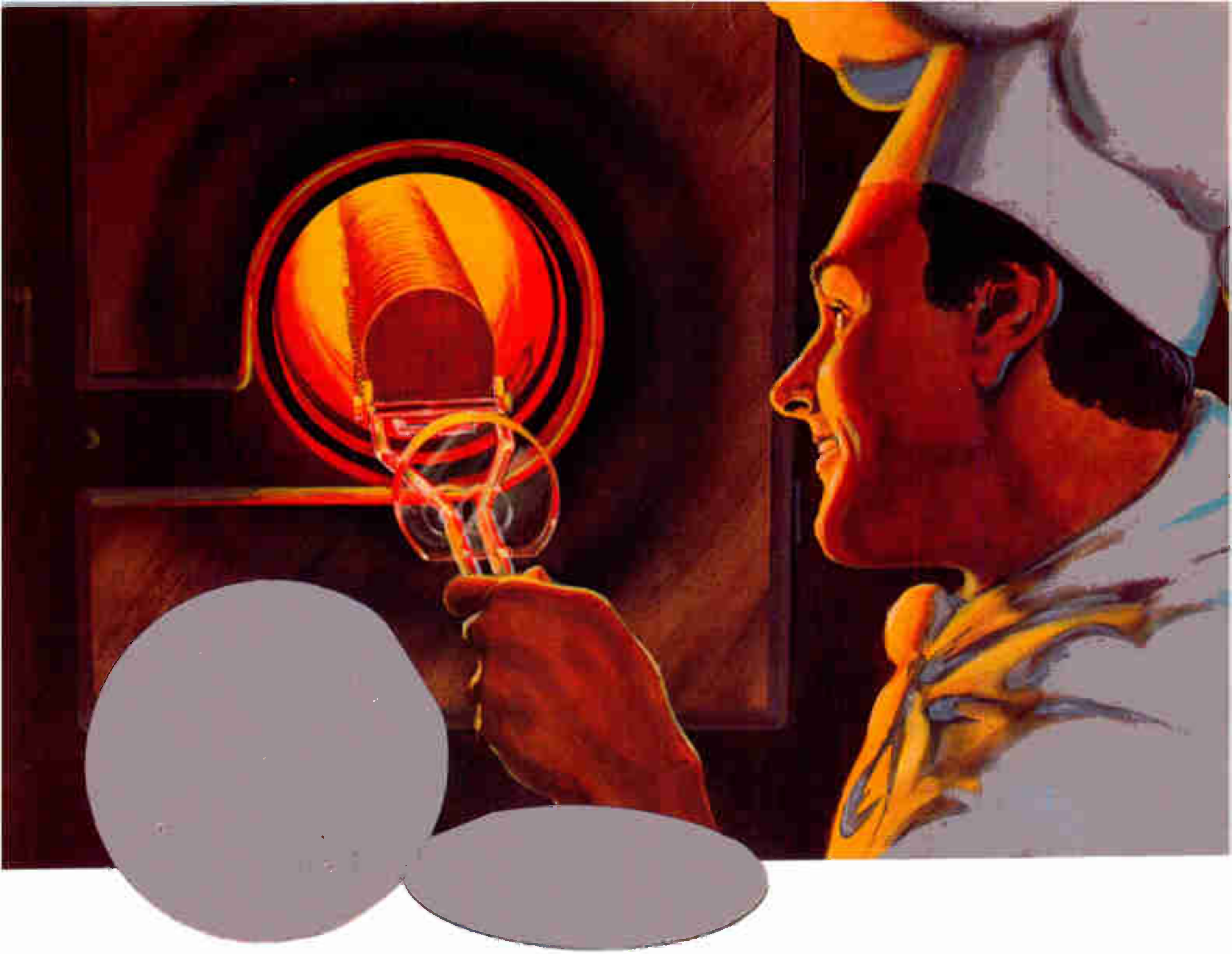
Thank you, Japan

To the Editor: I just read your three-part article on our industry, "The drive for quality and reliability" [May 19, p. 125]. I've worked in quality assurance for 20 years, 18 of which have been spent swimming upstream against a management mentality that says "ship it." If the success of the Japanese has caused U. S. manufacturers to make a conscientious commitment to specification conformance, I'd like to say *arigato* ["thank you"].

T. J. Lally
Spencer, W. Va.

Corrections

In "Power-fail detector uses chip's standby mode" (May 19, p. 153), regulator LM-390 and operational amplifier LM-334 in Fig. 1 should have been labeled LM-340 and LM-339, respectively. Also, the author notes that capacitor C_3 can be omitted in certain applications and that the external-interrupt pulse in Fig. 2 was accidentally inverted in his original drawing.



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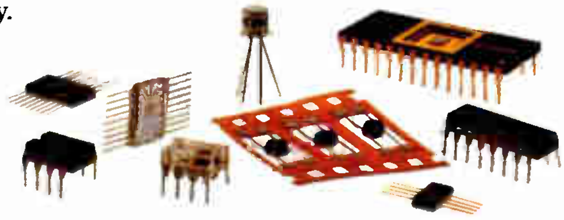

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Circle 13 on reader service card

People

Stansberry watches contracts and the foe for Air Force

The new commander of the Air Force's Electronic Systems division, currently administering some $16 billion in contracts with industry, keeps a portrait of his Soviet counterpart on his office wall at Hanscom Air Force Base, Mass. "He's the man I have to beat," smiles Lt. Gen. James W. Stansberry. "Seeing him every day reminds me to keep my priorities in order."

Stansberry would like to see everyone in the defense contracting community similarly reminded, lest second-order priorities obscure "this country's overall defense goal: survival." What worries him particularly is the "pervading belief that technological development must be a risk-free process." The result of that philosophy, Stansberry says, is a bureaucratic system that "talks every contract proposal to death; overtests every new system; and has become so loaded with checks, balances, and chains of authority that it takes forever to get things done."

With the U. S. running well behind the USSR in its military investments, this overcaution could be suicidal, Stansberry insists. "The perfect, fail-safe weapon that's still in field testing is irrelevant in a military showdown." So he is already campaigning hard for shorter development cycles, decentralization of contracting authority, and stronger funding commitments to important programs that promise fast results (see p. 88).

Stansberry, who began his military career by enlisting as a private in the Army in 1945, is a graduate of the U. S. Military Academy at West Point and earned a master's degree in business administration at the Air Force Institute of Technology. Prior to his appointment at ESD, he served as deputy chief of staff for contracting and manufacturing.

One of his chief interests at ESD is extending the range and quality of training programs for military and civilian personnel alike. "Much of the responsibility I'm delegating will fall on young shoulders, since so many of our senior people are taking earlier retirement. The youngsters are well-educated and energetic, but it's still important to give them the strongest possible grounding in program management and technical and industrial issues."

Rival. Gen. James Stansberry, head of the Air Force's Electronic Systems division, keeps picture of his Soviet counterpart as a reminder of who the opposition is.

Fiebiger bucks the tide and Motorola lands safely

Running against trends seems to be a habit lately for James R. Fiebiger, Motorola Inc.'s corporate vice president and manager of the firm's MOS operation in Austin, Texas. About a

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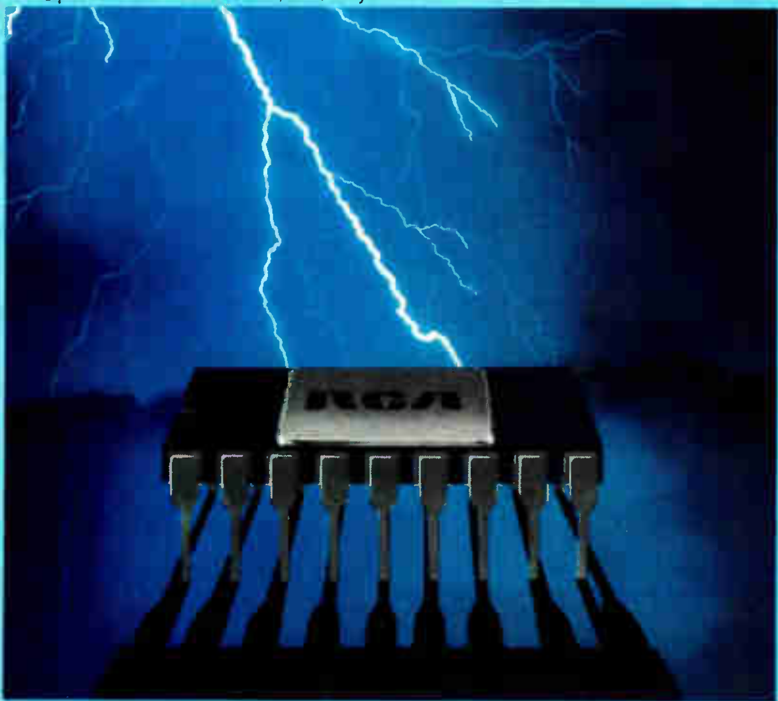

People

year and a half ago the 39-year-old executive surprised his people by telling them he was curbing hiring at the Central Texas plant. "We were reacting in February 1980 to what we saw as a coming recession in the industry," recalls Fiebiger, who joined Motorola as the Austin plant manager in 1977 from Texas Instruments Inc.

While other electronics companies were busy recruiting to keep up with the business in early 1980, Motorola's MOS and other semiconductor operations were asking employees to work some overtime in an attempt to protect them when the recession finally hit later that year. At the same time, Motorola was quietly paring down the size of its workforce through attrition.

Since the slowdown, other Texas semiconductor operations—as well as others across the nation—have been forced to reduce work schedules [*Electronics*, June 16, p. 96]. But that has not been the case in Austin, because of the action in early 1980, says Fiebiger, who earned his doctorate at the University of California at Berkeley. He predicts a stabilization period for MOS markets through the rest of 1981. However, he willingly admits that "we are still watching the economy like a hawk. We were right the last time, so we don't want to be wrong this time."

The Austin MOS operation finished 1980 with a book-to-bill ratio of 1.17, says the Minnesota native. The first quarter of 1981 ran close to last year's total, with the MOS operations entering 1981 with backlogs 26% higher than those at the beginning of 1980. The worst quarter was the third, when the ratio fell to 0.99, but the measurement improved in the final period to 1.21.

In addition to bucking the workforce trends, Fiebiger's operation is planning to double its presence deep in the heart of Texas with the construction of a second plant about 15 miles southwest of the existing Austin facility. When completed, the new complex will employ 4,000 people and have 750,000 square feet of space—about the same size as the present facility. □

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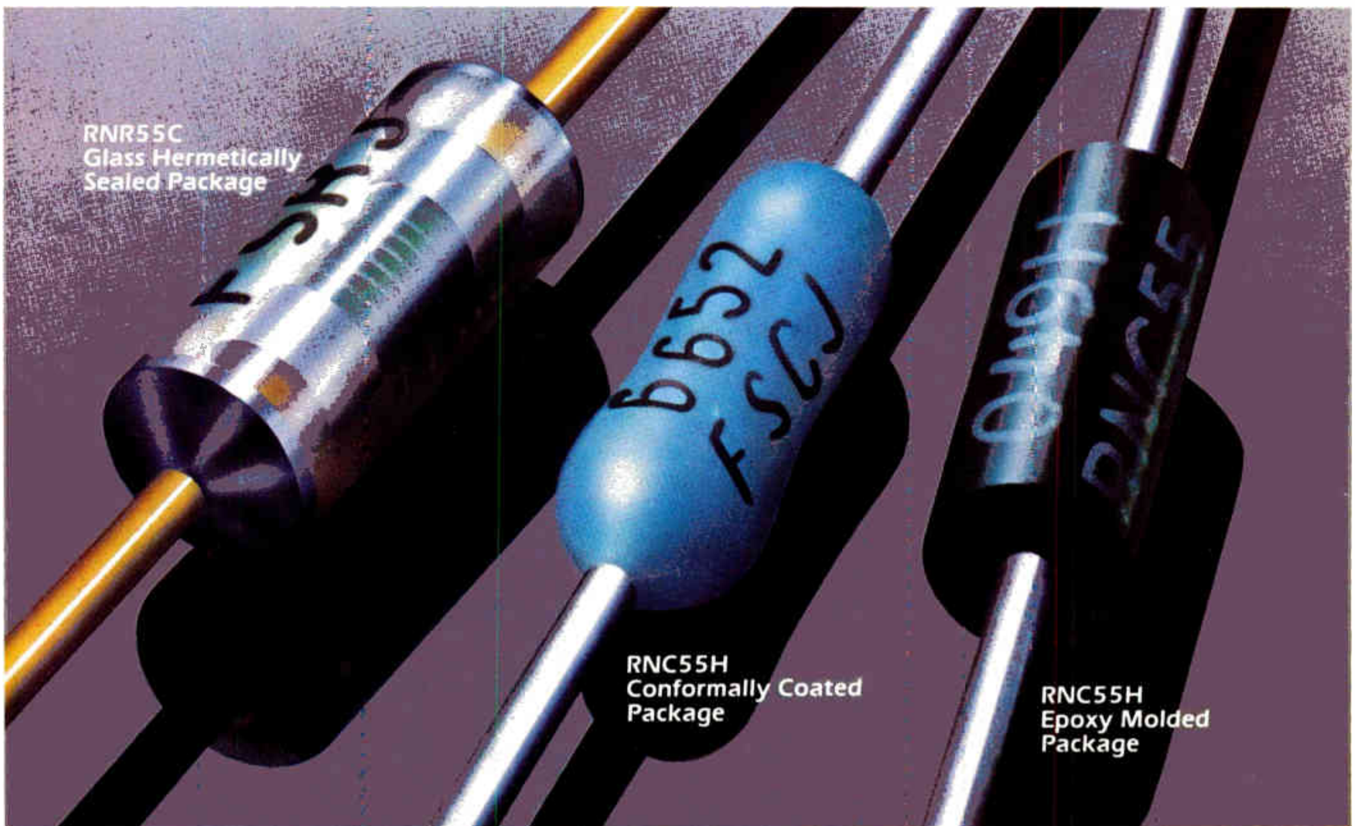
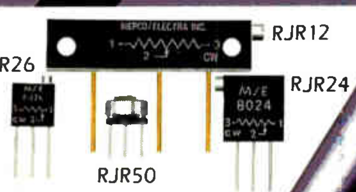




Now you do!

Circle 17 on reader service card

Intel's Series 90/iQX. The memory

Intel's new Series 90/iQX is the first standard Intelligent Memory System to offer continuous operation and high maintainability at low cost.

Now, for the first time, OEMs can design systems with built-in protection against errors, downtime, and excessive maintenance costs. How? With Intel's new Series 90/iQX.

Series 90/iQX Intelligent Memory System

The iQX controller adds the intelligence of an iAPX 86 microcomputer to the standard Series 90 Memory System. Intelligence that monitors memory operation directly, detects and corrects errors, runs local or remote diagnostics, and reallocates memory space as required. All without burdening the host system.

Fault-tolerant operation

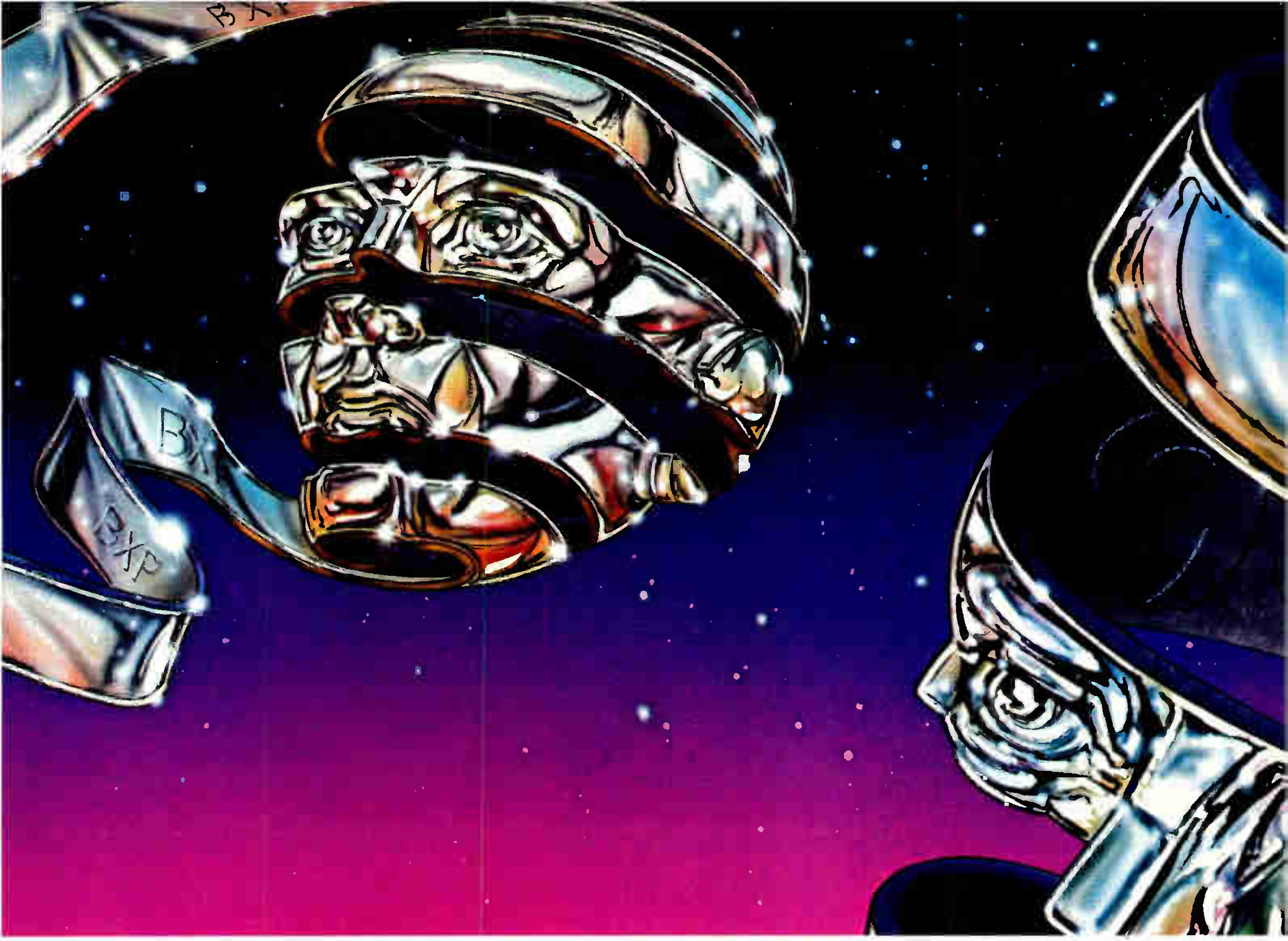
Hard errors or soft, Series 90's iQX controller uncovers them. Soft errors are simply "scrubbed" and corrected. In case of hard errors or device failure, the controller routes data around the problem, allocating spare memory as needed. It then logs the error for future reference.

With protection like this, the Series 90 system will continue operating uninterrupted until all spare memory is filled. And thanks to the iQX's memory status reporting, your customer will know well in advance of memory resource problems. Which not only improves data integrity, but increases reliability and reduces maintenance dramatically.

Instant diagnostics

To keep users continually apprised of conditions within their memory system, the iQX controller provides easy access to its complete diagnostic file. Information can be accessed by the host system either automatically via a simple message-driven software interface, or manually, using the iQX's Service Communicator. This detachable terminal allows technicians to instantly retrieve diagnostic data in plain English through a compact, alphanumeric keyboard/display. With no interruption of the host computer's operation.

For fast, simple maintenance, system diagnostics inform the user of any



machine with non-stop intelligence.

errors it has tracked—soft or hard, correctable or avoidable—and their precise location by row and column.

Many problems can also be solved using the iQX's memory tasking capability to move data blocks as required. Then too, the iQX monitors the system's power supply and signals a warning if voltages drop critically. As a final, double protection, the iQX controller even diagnoses its own operation continuously.

Diagnosing from a distance

To reduce maintenance costs for remote systems and networks, iQX diagnostics can be accessed over phone lines through a single diagnostic station. By being able to analyze problems from afar, you'll eliminate unnecessary service visits and shorten those that are required. And since one diagnostic station can easily serve up to 150 installations, the set-up and ongoing diagnostic costs are contained as well.

Consider the economics

The iQX's protection features offer important economic advantages for systems OEMs. Because of the increased demand for fault tolerance in today's marketplace, systems equipped with iQX capability add significant value to your products. In fact, many applications simply could not be justified economically *without* such self-healing and remote maintenance. Now, through Intel's leadership in 16-bit microprocessing, the Series 90/iQX brings you this capability at an incremental price only nominally above that of ECC alone.

In sum, iQX gives your systems state-of-the art fault protection, reduced maintenance costs, and therefore increased value. Best of all, Intel is delivering Series 90 systems with iQX right now. For detailed information, return the coupon to Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080. For hot line service, call (800) 538-1876.

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Circle 19 on reader service card

The Tektronix 4054 Desktop Computer

(Below) Using the 4054's Dynamic Graphics option, design symbols can be selected from a menu, dragged into position in refresh mode, then transferred to storage mode at the push of a button.

(Above) The 4054 screen's 13 million addressable points let designers work with whole circuit board layouts without sacrificing clarity of detail.

High speed. Dynamic graphics. Precise curve forms.

We're helping designers cut corners with confidence.

Design productivity reaches its peak on the 4054: It gives you straight answers fast, without burdening your host computer. It gives you real graphic curve forms instead of stair-step approximations.

Nothing else even comes close to the combined computing power and exacting, interactive graphics of the Tektronix 4054.

Fast graphic computing frees you from delays and uncertainties and keeps the work flowing productively. Even complex engineering designs can be completed in minutes. Your design tools include 36 distinct dot-dash patterns and four stroke-generated character sizes for labels, text and titles.

Its computational capabilities are some of the fastest and most powerful you'll find on a desktop. Special matrix functions are built-in. Strings and transcendental functions execute with desktop speeds unique to Tektronix.

Dynamic graphics option lets you move symbols and text around the screen under built-in thumbwheel control. Complex graphics objects can be quickly and easily assembled, then stored in place with the push of a button. With easy BASIC, you focus on the project, not protocol.

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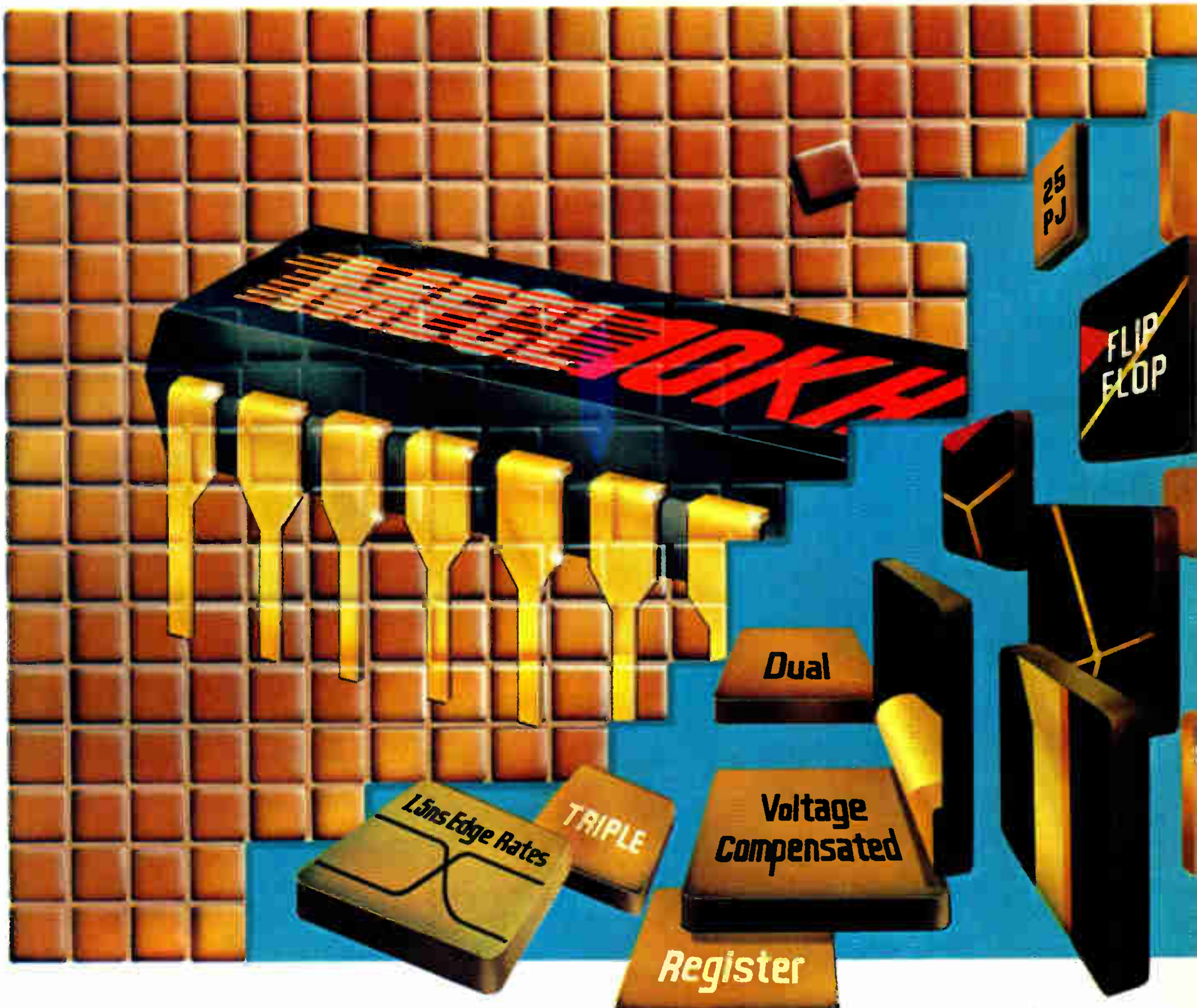

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Speed X 2.

MECL10KH increases the speed of industry-standard MECL10K by a factor of 2. System clock rates increase as much as 40%, parasitic capacitance drops 50% and half the propagation delay, now just 1 ns, occurs at the same, 25 mW power levels as MECL10K.

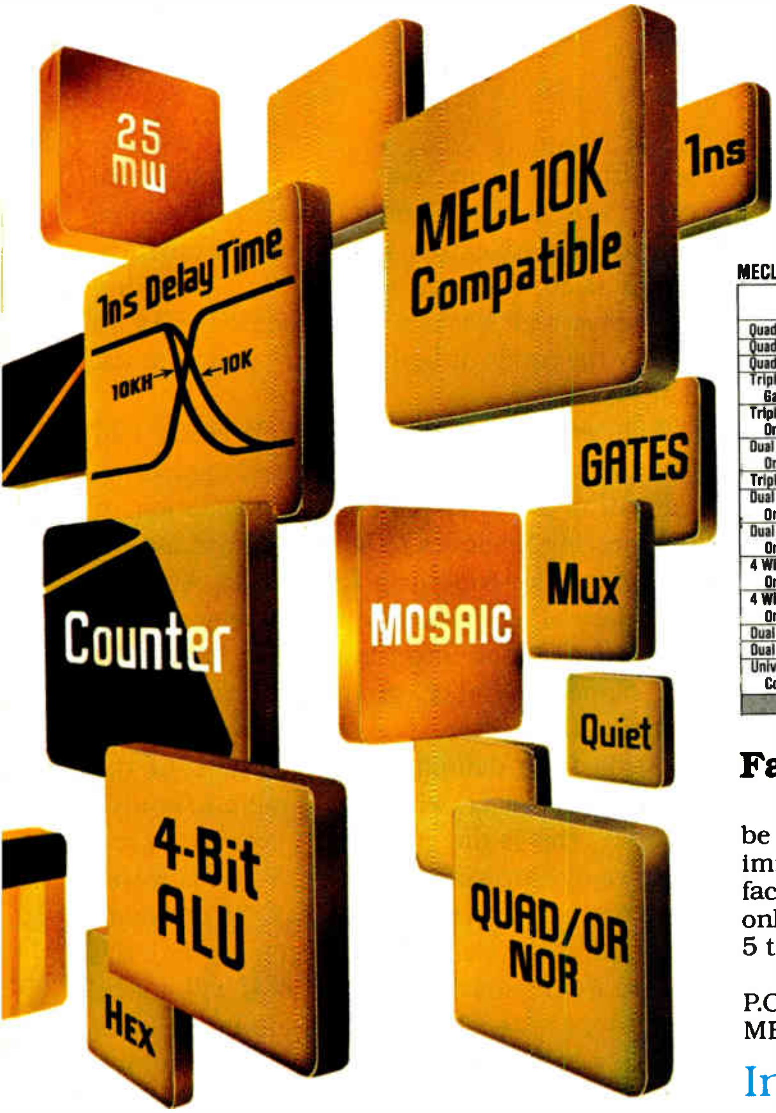
The resulting, 25 picojoule, speed-power product is the best of any ECL logic family today.

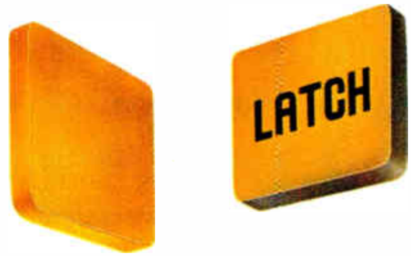
Maximizing with MOSAIC™.

It's all because of MOSAIC...Motorola's proprietary, high-density, oxide-isolated process that not only increases performance dramatically but decreases device area to about 1/7th the size of existing MECL10K products. That boosts f_T as well as all other initial device parameters.

Further, 10KH circuits are voltage-compensated and offer noise margins typically 20% better than

1 ns MECL10KH. that's available fast, first.





MECL 10KH INTRODUCTION LIST

Function	Part Number	Samples Available
Quad Or/Nor Gate	MC10H101	Now
Quad Nor Gate	MC10H102	Now
Quad And Gate	MC10H104	Now
Triple 2-3-2 Or/Nor Gate	MC10H105	Now
Triple Exclusive Or/Nor Gate	MC10H107	Now
Dual 4-5 Input Or/Nor Gate	MC10H109	Now
Triple Line Receiver	MC10H116	Now
Dual 2-Wide Or-And/Or-And Invert Gate	MC10H117	Now
Dual 2-Wide 3 Input Or-And	MC10H118	Now
4 Wide 4-3-3-3 Input Or-And	MC10H119	2nd Half 1981
4 Wide Or-And/Or-And-Invert Gate	MC10H121	2nd Half 1981
Dual D Latch	MC10H130	2nd Half 1981
Dual D Flip-Flop	MC10H131	2nd Half 1981
Universal Binary Counter	MC10H136	2nd Half 1981
4 Bit Universal Shift Register	MC10H141	2nd Half 1981
16 × 4 Bit Register File	MC10H145	2nd Half 1981
12 Bit Parity Generator/Checker	MC10H160	2nd Half 1981
Binary to 1–8 Line Decoder (Low)	MC10H161	2nd Half 1981
Binary to 1–8 Line Decoder (High)	MC10H162	2nd Half 1981
8 Line Multiplexer	MC10H164	2nd Half 1981
Quad 2 Input Mux W/Latch	MC10H173	2nd Half 1981
Dual 4 to 1 Multiplexer	MC10H174	2nd Half 1981
Quint Latch	MC10H175	2nd Half 1981
Hex D Flip Flop	MC10H176	2nd Half 1981
Look Ahead Carry Block	MC10H179	2nd Half 1981
Dual High-Speed Adder/Subtracter	MC10H180	2nd Half 1981
4 Bit ALU	MC10H181	2nd Half 1981
Dual 3-Input Or Gate	MC10H210	2nd Half 1981
Dual 3-Input Nor Gate	MC10H211	2nd Half 1981

10K devices. And, higher density functions that couldn't be manufactured economically in MECL10K technology are planned with MOSAIC... Motorola's own process.

10K-compatible.

The family is specified at the -5.2 V level for compatibility with MECL10K logic and memories and with the MC10800 bit-slice family, the MC10900 LSIs and the MECL MACROCELL™ array. Its 0° to 75° C range also matches constraints established by these products.

All MECL10KH specs have guaranteed minimums and maximums for extremes of both temperature and supply.

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Human capital formation

The alarm over the growing shortage of engineers and other technical personnel has been sounding loud and clear for some time now, and the chorus is beginning to get shrill. There are still those who believe the whole thing is a propaganda campaign by some of the larger corporations to attract more engineers into the field in order to slow or stop the rapid ascent of salary levels. And there are still others who view the news as simply the beginning of another cycle of boom and bust—they remember all the engineers who went into the pizza business in the debacles of 1970 and 1974. Despite these cynics, however, there is plenty of evidence that the shortage is real, that it is growing, and that it represents the seeds of a crisis that will sprout in the near future if nothing is done to alleviate it.

For example, a recent survey of 1,265 firms conducted by the American Electronics Association showed there will be a need by 1986 for an additional 113,000 professionals, including engineers and computer scientists, and more than 140,000 paraprofessionals such as technicians, assemblers, and draftsmen. The U. S. is currently graduating between 17,000 and 20,000 engineers, and that rate will leave a considerable shortfall by 1986. What's more, these numbers do not take into account the additional effect on the available engineering pool of the Reagan Administration's military buildup (see p. 88).

A more insidious problem, and maybe one with even longer-term effects, is the erosion of qualified faculty in the engineering schools. Prevailing high wage scales for engineering talent, particularly for those with advanced degrees, are attracting Ph.D.s into industry and draining them away from the traditional career of teaching. Should this trend continue, engineering educators say, it would create a severe decline in the quality of engineering graduates and weaken the nation's ability to satisfy the needs of both industry and national defense.

The problem has become sufficiently bad for the American Society for Engineering Education and the American Association of Engineering Societies to be casting around for solutions. The American Electronics Association has set up a committee on engineering education to look into the problem, and there are numerous other groups and companies studying the matter.

Aside from defining the dimensions of the shortage, however, what else is there to study? Frankly, this is one problem it seems possible to solve by throwing money at. What is working here is the fundamental rule of the marketplace, with talented people going where the money is. Obviously, many schools will not be able to raise the salaries of their faculties to industry levels without making tuition so high as to be out of reach for many potential students. We suggest that industry will have to get into the act. Two possibilities would be for electronics companies to underwrite faculty positions or to furlough some staff to local universities at full pay on a rotating basis. A third would be to make the shrinking pool of teaching talent more widely available through interactive cable television.

In a period when one of the major problems of U. S. industries is capital formation, it is essential to husband our most precious capital of all—human capital.

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Meetings

16th Intersociety Energy Conversion Engineering Conference, IEEE, American Society of Mechanical Engineers, American Institute of Aeronautics and Astronautics, *et al.*, Hyatt Regency Hotel, Atlanta, Aug. 9–14.

20th General Assembly of the International Union of Radio Science (R. Dow, National Academy of Sciences, 2101 Constitution Ave. N. W., Washington, D. C. 20418), Hyatt Regency Hotel, Washington, D. C., Aug. 10–19.

Optical Information Processing for Aerospace Application, (H. Hendricks, Langley Research Center, Hampton, Va. 23665), Hampton, Va., Aug. 18–19.

VLSI 81—International Conference on Very Large-Scale Integration, (Secretariat, VLSI 81, 26 Albany St., Edinburgh EH1 3QH, UK), University of Edinburgh, Edinburgh, Scotland, Aug. 18–21.

1981 International Conference on Cybernetics and Society, IEEE, Atlanta Hilton Hotel, Atlanta, Aug. 24–27.

SPIE International Symposium and Instrument Display, Society of Photo-Optical Instrumentation Engineers (P. O. Box 10, Bellingham, Wash. 98227), Town and Country Hotel, San Diego, Calif., Aug. 24–28.

Seventh International Joint Conference on Artifical Intelligence, IJCAI *et al.* (Pat Hayes, General Chairman, IJCAI-81, University of Rochester, Department of Computer Science, Rochester, N. Y. 14627), University of British Columbia, Vancouver, B. C., Aug. 24–28.

1981 International Conference on Parallel Processing, IEEE Computer Society, Shanty Creek Lodge, Bellaire, Mich., Aug. 25–28.

FOC '81—Fourth International Fiber Optics and Communications Exposition, Information Gatekeepers Inc. (167 Corey Rd., Brookline, Mass. 02146), Hyatt Regency Embarcadero, San Francisco, Sept. 1–3.

European Conference on Electronic Design Automation, Institution of Electrical Engineers (Savoy Place, London WC2R 0BL), University of Sussex, Brighton, UK, Sept. 1–4.

Electron 1—Home Video and Personal Computers Exposition, Epic Enterprises (6158 Mission Gorge Rd., San Diego, Calif. 92120), Convention Center, Los Angeles, Sept. 4–6.

International Audio and Video Fair Berlin, AMK Berlin (Messedamm 22), West Berlin Fairgrounds, Sept. 4–13.

11th European Microwave Conference, Eurel, IEEE, *et al.* (M. T. Vlaardingerbroek, Philips, Elcoma EH5, 5600 MD Eindhoven, the Netherlands), RAI Congress Center, Amsterdam, the Netherlands, Sept. 7–11.

Seminars

VHSIC Military and Commercial Applications, American Institute of Aeronautics and Astronautics (AIAA Conferences, 5959 W. Century Blvd. Los Angeles, Calif. 90009), Westpark Tysons Motel, Washington, D. C., Aug. 3–4, and Howard Johnson's, Boston, Sept. 3–4.

Impactless Printing, Institute for Graphic Communication Inc. (Richard D. Murray, IGC, 375 Commonwealth Ave., Boston, Mass. 02115), Highlands Inn, Carmel, Calif., Aug. 9–11.

Laser Optics Course, Laser Institute of America (P. O. Box 9000, Waco, Texas 76710), Los Alamos Inn, Los Alamos, N. M., Aug. 17–21.

Office Automation and Integration of Word Processing and Data Processing, Frost & Sullivan Inc. (106 Fulton St., New York, N. Y. 10038), Holiday Inn, Fisherman's Wharf, San Francisco, Aug. 19–21.

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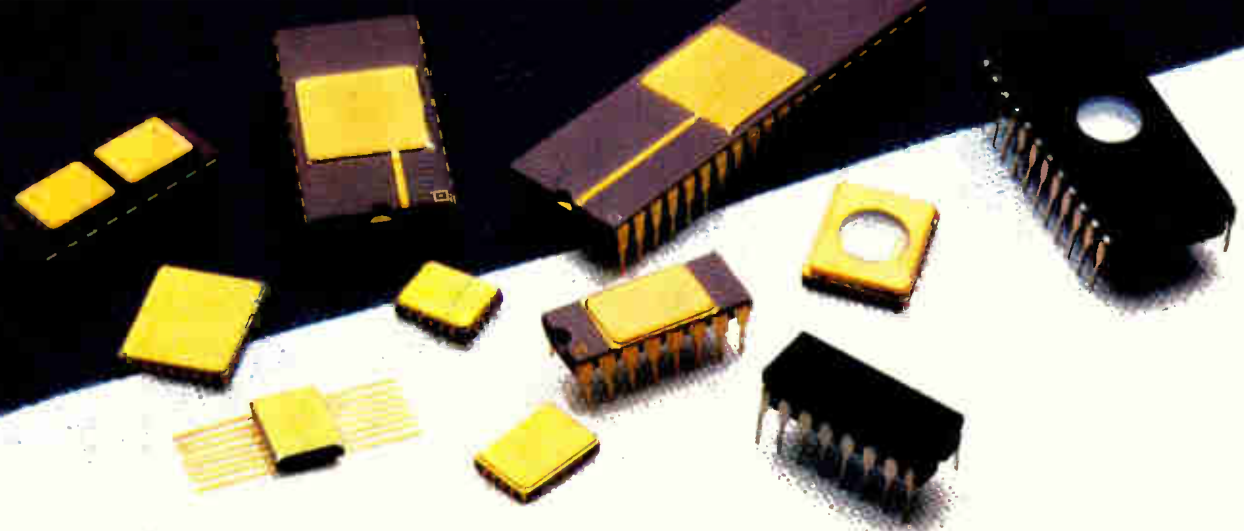

A lot of little things.

And we make a lot of the little things.

We're Mostek Military Products. And we make a full line of memories and microcomponents for military, aerospace, and industrial/scientific applications. Our LSI and VLSI devices add intelligence to everything from avionics to hospital instrumentation. From tactical missiles to telecommunications.

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Circle 27 on reader service card

FJYCX	PPRWX	URMMR	ZVCYC	UEJPD
JUDXJ	WWCVW	CUOXV	WQYCU	DQOCJ
FRPEW	IJPHD	RPHQZ	UQPHJ	WZJMM
HQWDI	RCTGJ	NIPBQ	HJHIP	BCHYA
QHYJV	NJHYP	BIPBC	HYPBQ	PVCFF
YJVNJ	HYCOP	BIJHI	PBQPV	CFFLJ
PBIGJ	OPLQG	QYIHQ	PRNIQ	FVQXO
OCLIO	VCPBP	BIBCL	LIHTF	QVPBI
TCNOP	HCHIP	XKINA	IHPJT	QPQOE
PQEIO	HCHIP	XKINA	IHPJT	PBIPC
GIPBI	FQOPP	IHKIN	AIHPP	QEIOP
BIJPB	INHCH	IPXPB	IPJQO	PQFVQ
XOTQF	FODIF	FCILO	CLILJ	VHWXZ

HU HCPURB

WICACVWJPWCVW

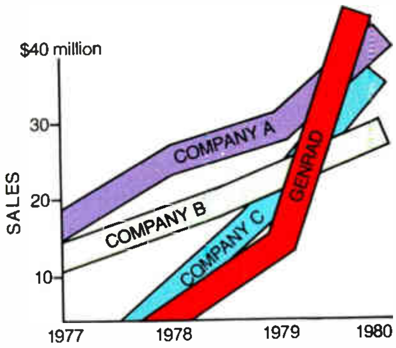
Test #3. This cipher contains a message everyone in in-circuit testing will appreciate. To solve it, you must find the correct substitute for every letter.

HERE'S ANOTHER GREAT GENRAD CIRCUIT TESTER.

This time we've come up with a cryptogram to test your analytical powers—and make it clear why a GenRad in-circuit system gives you higher quality tests.

If you're searching for a way to improve the quality of your boards, take a little time and try to solve our puzzle. There's an important message here about the advantages of owning a GenRad in-circuit test system.

Why a cryptogram? It can be devilishly deceptive. Just like claims for easy solutions to in-circuit testing. We know. Because we've identified the problems. And designed a system that anticipates them. That's why we can state unequivocally that our 2270 delivers the most thorough and comprehensive test of any in-circuit system available.



From market entry to number one in only two years.

Knowing that, it probably won't surprise you if we reveal another fact: GenRad in the short span of two years, has become #1 in in-circuit test systems.*

The Secret Is In The Software.

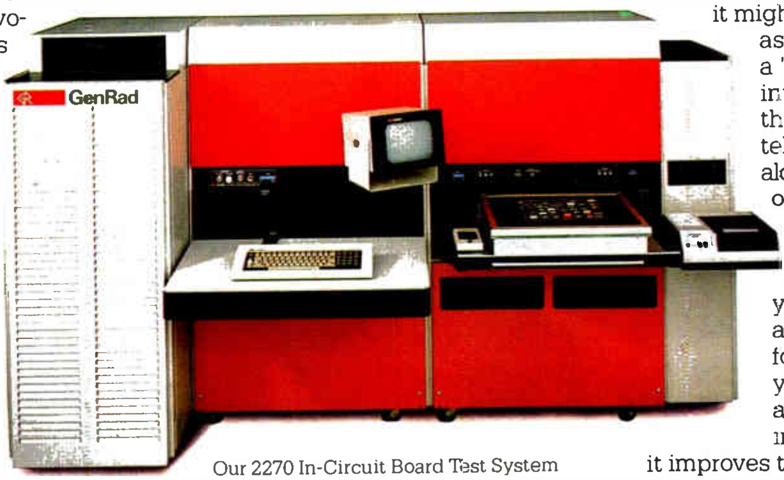
What makes our system so much better than other in-circuit systems? Primarily, our software. It does more for you up front, during your test program generation phase. Which makes your job much easier and faster at the debug end. (Imagine if you could get your hands on the key to the cryptogram in advance. Cracking it would be a piece of cake, right?)

How does our software do it? For one thing it's based on circuit analysis. So it automatically can think in advance of all the "gotchas" that can crop up when you finally try to make your program work with your board. (Wouldn't that be a handy thing to have to solve our cipher?)

We also have a feature called automatic bus disable. This automatically isolates the IC under test from the effects of other IC's. And saves you from writing extra tests manually, which is tedious and error-prone. (Incidentally, isolating individual letters, say all the E's, is one shortcut used in solving ciphers like ours.)

Three other things (out of many) about our software that stand out. Automatic feedback squelch to block troublesome "glitches" and assure you of repeatable tests. Automatic test program modification to optimize the test based on wiring configurations. And the most extensive library of ECL, TTL and MOS devices.

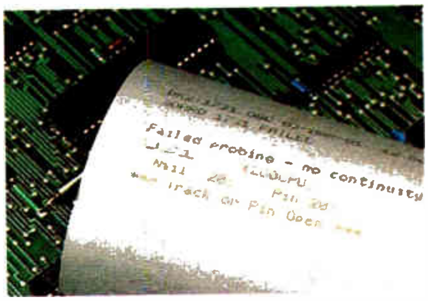
Go out and dig into other systems. No matter what the claims, the truth is you won't find all these important features on any of them.



Our 2270 In-Circuit Board Test System

Thanks For The Memories.

A good memory can be a useful tool for either cryptoanalysis or circuit testing. We put memory behind each pin in the 2270. So each device is tested the way it was meant to be operated, with all pins functioning simultaneously, rather than one pin at a time. This speeds up testing throughput by more than two times the speed for other in-circuit approaches. It also means more comprehensive coverage, especially for LSI and VLSI devices.


There's nothing cryptic about our repair messages.

Finally a word about diagnostics. We designed ours to be clear. The 2270 will never leave you with repair messages that look like the opposite page of this ad.

The Final Analysis. And an open offer.

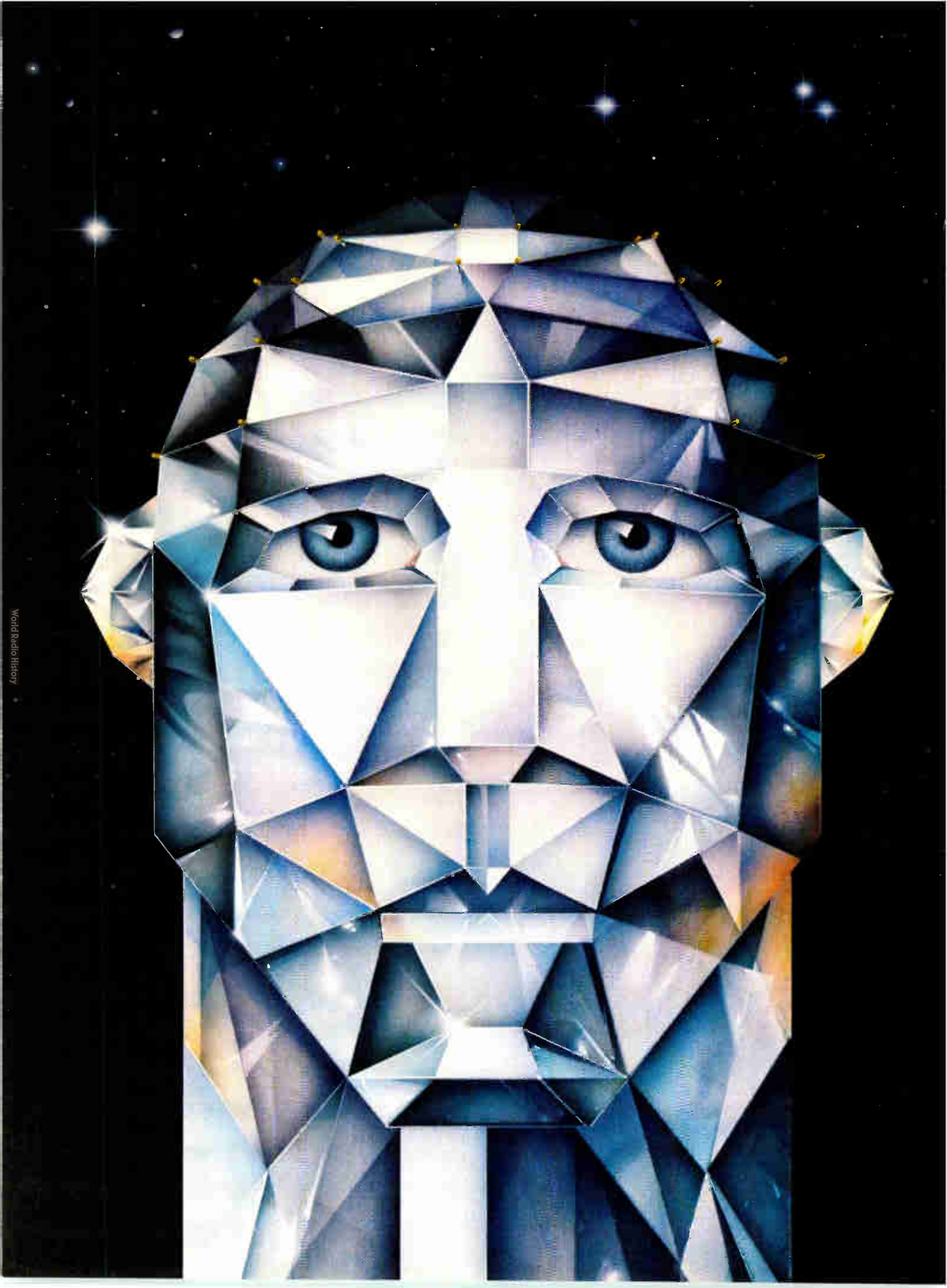
Broken our cipher yet? We said it might not be easy. Just as in the real world, there's a "gotcha" in it. If you run into trouble, keep in mind the key word we've been telling you to look for all along: quality. Whether or not you uncover our message, let us know on your letterhead and we'll send you a poster-size version, along with the solution for you to fill in. And if you'd like to know more about what's in a GenRad in-circuit system and how it improves the yield of good boards, just contact us at 300 Baker Avenue, Concord, Massachusetts 01742. Telephone: (617) 369-4400.

We'll make everything clear.

GenRad
THE BEST IN TEST.

*Source: Dataquest, Inc. 1981

Circle 29 on reader service card



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NEC is making a special offer that will let you test your μPD8048 prototypes within a week, plus get NEC's μPD8748 programmable processor at μPD8048 prices.

Here's how it works. Just place an order for μPD8048s or μPD80C48s, our low power consumption CMOS version. After we receive and accept your order, we'll send you μPD8748s programmed with your code for testing purposes.

And we'll send them at the same price as the product you order, so you'll save big.

If you order μPD8049s, we'll still send you the μPD8748s, but without programming.

When you've completed testing your prototype, you can reprogram and reuse the μPD8748 for any application you'd like.

For orders of 1,000 to 5,000 units, we'll send you 25 μPD8748s. For larger orders, we'll send you 0.5% of the total order, up to 100 μPD8748s.

So order your μPD8048 products today. And we'll put you on the program. Pronto.

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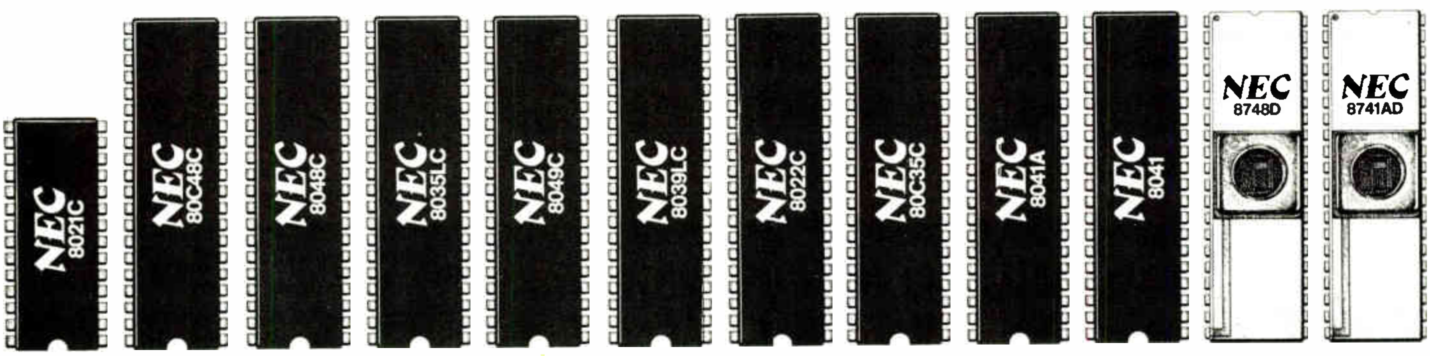

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Racal has a high technology approach. Advanced research, pioneering work in microelectronics and careful market evaluation help to keep us in the forefront across a wide range of electronics markets.

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From radio and data communications to radar and navigational systems, from computer-aided design to instrumentation and encryption devices—Racal is a world leader in these and many other fields.

We're growth

We're a company that's going places. During the past five years our annual sales have grown from about $ 150 million to a current annual rate in excess of $ 1 billion.

We're worldwide

We operate through over 50 principal Racal companies, to markets in 150 countries and backed by more than 1000 distributors, agents and service locations. We are totally committed to customer support wherever it's needed.

We're here

Today there are some 15 Racal companies based in the United States, with a total of around 5,000 employees. These US companies represented 25 percent of our 1980 gross annual sales.

An information package on Racal is available by writing the Racal Electronics Group at P.O. Box 5506, Grand Central Post Office, New York, N.Y. 10163.

Circle 32 on reader service card

RACAL

The Electronics Group

Racal Electronics Limited, Bracknell, Berkshire RG12 1RG England.

Electronics newsletter

Under-$3,000 terminal emulates others . . .

A desktop data terminal with a 13-in.-diagonal color CRT display that can emulate about a dozen of the most commonly used computer terminals will soon be distributed by Intelligent Systems Corp. of Norcross, Ga. Equipped with an 8080 microprocessor, a minimum of 16-K bytes of MOS main memory, a 72-key keyboard, and 92-K bytes of minifloppy-disk storage, the unit can be configured by the user to emulate cathode-ray-tube terminals from Perkin-Elmer, Lear Siegler, Beehive, Hazeltine, Intertec, Digital Equipment, and others. Not only would the model 3651 terminal emulation package help solve the communications compatibility problems common in large computer networks, **but it also would offer off-line processing capability and eliminate the expensive color-processing electronics** now inserted between mainframes and some color consoles. Pricing is not yet firm, but the company says that the terminal should sell for less than $3,000 in single units and 25% to 30% less in quantity to original-equipment manufacturers.

. . . as HP's terminal becomes a computer

Look for an August announcement of an enhanced intelligent terminal from Hewlett Packard Co. in Palo Alto, Calif., that doubles as a personal computer. Dubbed the HP 125, it will be the same size as the HP 2621A intelligent terminal but contain additional functions. Whereas the model 2621A uses one Z80 as a terminal controller, the HP 125 uses an additional Z80 running under Digital Research's CP/M operating system as a general-purpose processor. As a stand-alone computer, **it will be able to run a large body of third-party applications programs available under CP/M**, including word-processing graphics, VisiCalc (a business software package), and high-level languages. The unit also can be used as an intelligent terminal for the HP 3000 series of business computers, thus enabling the user to select data from a large data base.

Microprocessors move in on power-line communications net

Twacs, a microprocessor-based two-way automatic communications system for electric utilities, is being installed by the Missouri Power & Light Co. of Jefferson City, Mo. A product of Emerson Electric Co.'s Load Management Systems division in St. Louis, it uses 13-kV lines between power substations and customers as a communications medium. Its applications include automatic meter reading, peak-load management, power-factor control, and maintenance of meter security. **Twacs employs low-cost microprocessor-equipped transceivers and phase modulation of high-voltage current** from substations to as many as 5,000 customer sites per station and pulse-code modulation from the customers to substation. The system, expected to require relatively low capital expenditures compared with competing systems, was developed for Emerson by Arthur D. Little Inc., Cambridge, Mass.

Nine-sided tube could replace ribbons in solar-cell process

A variation on the edge-defined film-fed growth (EFG) process used by Mobil-Tyco Solar Energy Corp. for producing solar-cell silicon substrates could become the Waltham, Mass., firm's method of choice in the next year. Whereas the original EFG method pulls multiple ribbons of silicon from a crucible [*Electronics*, July 19, 1979, p. 110], the new technique produces a nine-sided silicon tube measuring 48.8 cm around and having a typical wall thickness of 0.25 cm. Laser cutting produces flat, rectangular substrates from each of the tube's nine faces. Batch production of the silicon tubes, **which in the laboratory has reached a formation rate of 146 cm/min, already appears more economical than Mobil-Tyco's current full-scale commercial EFG operations,** the company says.

NEC to build $100 million IC plant in U. S.

Representing one of the largest infusions of Japanese investment into the United States, NEC Electronics USA has begun work on a $100 million wafer fabrication facility in Roseville, Calif. **The plant will have complete facilities to take a product from wafer fabrication to packaged chip.** The devices will be made using n-MOS technology; in addition to the random-access and read-only memories currently produced by NEC's Electronic Arrays subsidiary, it will enable the company to turn out electrically programmable ROMs and microprocessors. The company's rationale for locating the plant in the U. S. is that, since it is to produce products customized for the user at the mask stage, such as ROMs, array logic, and 8048-type microprocessors, it must be close to its customer base.

SLICs from ITT take high voltage in their stride

Two subscriber-line interface circuits—one, the 2002, for the private-branch exchange market and the other, the 2001, geared to central office use—will be made available for evaluation by the North Microsystems division of International Telephone & Telegraph Corp. The 2002 will be ready in July, the 2001 in the last quarter. Based on the 3081 and 3082 SLICs [*Electronics*, June 5, 1980, p. 113], the devices from the Deerfield Beach, Fla., division combine a monolithic circuit and thick-film hybrid to perform test, measurement, and control functions, **among them the handling of such high-voltage chores as lightning protection.** Other semiconductor makers have had difficulties with SLICs as chips have problems in handling the 1,000 V or more that may appear on a phone wire.

Burroughs launches office system

Serving notice on the Wangs, Xeroxes, and IBMs that it intends to be a major factor in the automated office market, the newly formed Office Systems Group of Burroughs Corp., Detroit, has unveiled its OFIS 1 system. Designed to be operated by relatively unskilled managerial and professional people as well as clerical staff, it combines new and existing products and adds some new software. **OFIS 1, which can now be connected to Ethernet through Xerox's network servers,** uses Burroughs or other word-processing systems, facsimile systems, optical-character-recognition page readers, printers, and terminals. It ties them together with a new communications and system manager called the OFISdirector, which is based on Burroughs' CP95000 processor—the engine for the B90 family of computers. The OFIS director also handles electronic mail and manages OFISfile, a new Winchester-based (80- or 160-Mb) file management system, with a generalized and universal content-addressable information search and retrieval feature.

Rockwell officials form GaAs IC house

Fred A. Blum, vice president of Rockwell International Corp.'s Anaheim, Calif., Microelectronics Research and Development Center for 2½ years, **has resigned to form a custom integrated-circuit house, GigaBit Logic,** which will use ion-implanted gallium arsenide technology. The other founder of the Yorba Linda, Calif., firm is Louis R. Tomasetta, director of the optoelectronics research department at the Anaheim facility.

Why it pays to enlist EAROM.

Richard L. Wiker, author of the ERADCOM study on *Electrically Alterable Read Only Memory* reports:

"The use of MNOS EAROMs and WAROMs in military memory systems has now become a low risk, cost effective, alternative to bulky, costly, less reliable magnetic and rotational memories. While MNOS is a relatively mature technology in moderate commercial use, military grade parts have either had their availability restricted by the manufacturer or had to be individually characterized and screened by the potential user. The improved prospect for MNOS use in military memories is derived from the sale of High Reliability versions of the ER2810 and ER3400 by General Instrument. This removes a long standing hurdle in seeking an electrically alterable non-volatile memory technology that can be compatibly packaged with other IC's in a relatively dense, efficient approach. The expanding use of these and similar parts in a variety of military systems is also providing the reliability and life cycle cost information necessary to support the use of MNOS memory devices, in hi-rel systems."

General Instrument Hi-Rel EAROMs meet full military temperature requirements (−55° C to +125° C) and are processed and screened per Mil-M-38510/Mil-STD-883B. With bit densities from 512 to 8192, EAROMs offer clear-cut advantages over rotating memories, core, RAMs and UV PROMs as charted below.

Write Microelectronics Division, General Instrument Corporation, 600 West John Street, Hicksville, N.Y. 11802, or call 516-733-3358 for applications assistance.

Features	EAROM	RAM & Battery	UV PROM	TAPE	CORE	DISC
Word Alterability In-System	Yes	Yes	No	Yes	Yes	Yes
Access Time	1µs	< 0.5µs	< 0.5µs	secs	µs	ms
Re-programming Time	11ms	< 500ns	15 mins	secs	µs	ms
Radiation Hardness	good	poor	poor	good	good	good
Temp Range	−55°C to +125°C	ltd by battery	−55°C to +125°C	limited	limited	limited

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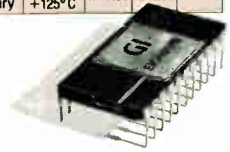

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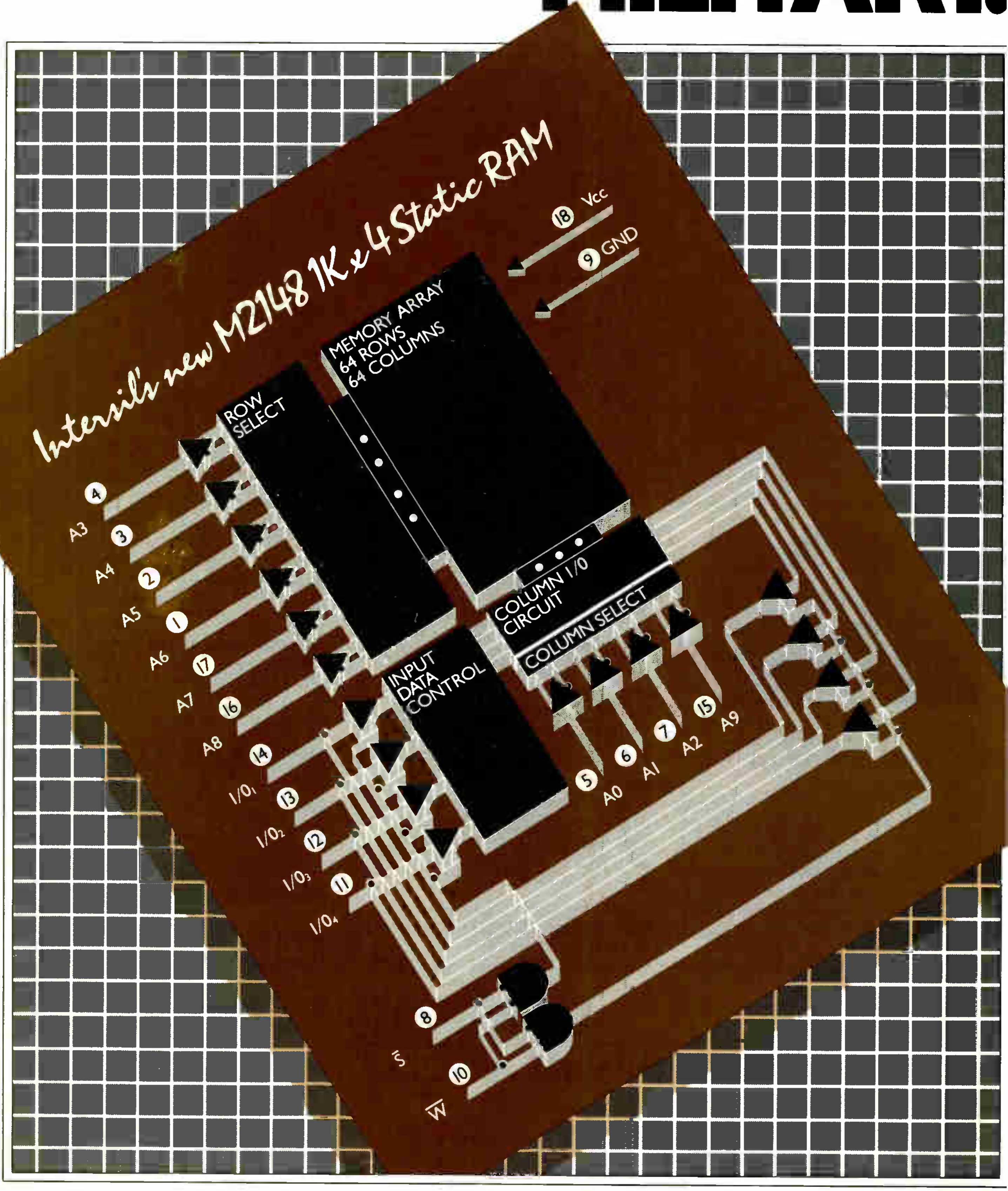

STANDARD 2148 IN FROM INTERSIL.

INTERSIL MILITARY 2148s*			
	t_{aa} (ns)	I_{op} (mA)	I_{sb} (mA)
M2148	85	180	30
M2148-3	70	180	30

INTERSIL MILITARY STATIC RAMS*			
	Organiz.	t_{aa} Range (ns)	I_{op} (mA)
M2148	1K × 4	70 – 85	180
M2147	4K × 1	70 – 85	180
M2114	1K × 4	200 – 450	90
M7141	4K × 1	200 – 450	90

*All chart specifications are worst case, guaranteed over operating voltage and temperature ranges.

HIGH-SPEED 1K × 4 RAM—FOR HI-REL.

Yes, it's the industry standard. Yes, it has multiple-source availability. Yes, it's pin-for-pin compatible with 2114s and the other 2148.

But Intersil offers it in military versions as well as commercial. With temperature operating range from –55° to 125°C. With Hi-Rel processing to 883B class B processing or to your custom Hi-Rel requirements. And in a choice of standard packages—cerdip or flatpack.

FOR HIGH-SPEED APPLICATIONS.

Finally, there's an industry-standard 1K × 4 static RAM for systems that demand both high speed and tolerance of extreme environments. And it comes with a choice of speeds: 85ns for the M2148 and 70ns for the M2148-3. Which makes this RAM well suited to real-time data processing and a host of other applications.

1K × 4 OR 4K × 1—TAKE YOUR CHOICE.

Either way you want it, Intersil has RAMs for you—as the charts show. In addition to the M2148s, we offer military versions of 2147s, 2114s and 7141s.

And since our single-layer poly HMOS is producing speeds competitive with bipolar, we're continuing to expand the family. Right now there are plenty to choose from. In the near future, there'll be even more.

CALL INTERSIL.

If you've been waiting for a fast, Mil-temp 1K × 4—wait no longer. Get a price quote and prove to yourself how cost-effective the M2148 can be in your system. Also, see how competitive our delivery commitments are.

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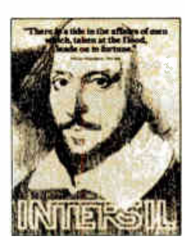

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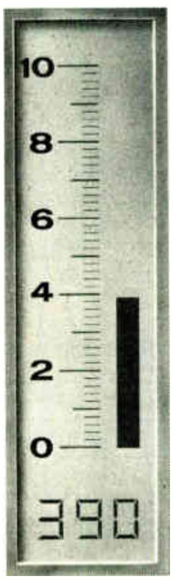

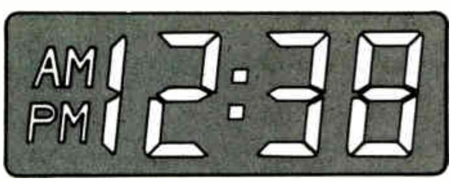

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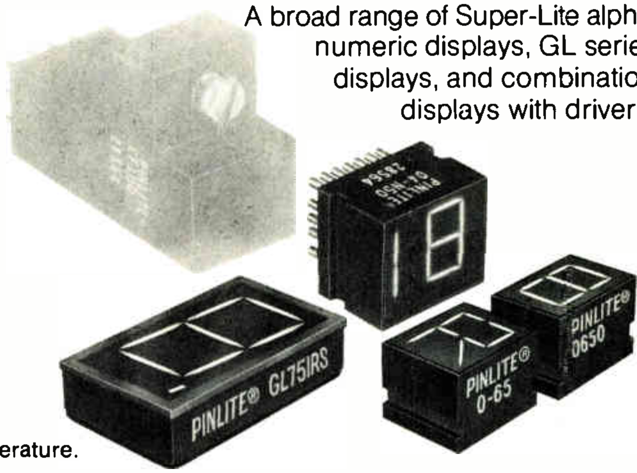

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TI tries out plastic leaded chip-carriers

by J. Robert Lineback, Dallas bureau

First to arrive in new, low-cost packages will be advanced low-power Schottky circuits

History, we are told, repeats itself—particularly when the forces that shape it remain essentially unchanged. What happened with dual in-line packages for integrated circuits thus seems sure to come about with chip-carriers, which are supplanting DIPs as the popular package for large, complex chips. Ceramic chip-carriers will be edged out of the commercial market by low-cost plastic versions.

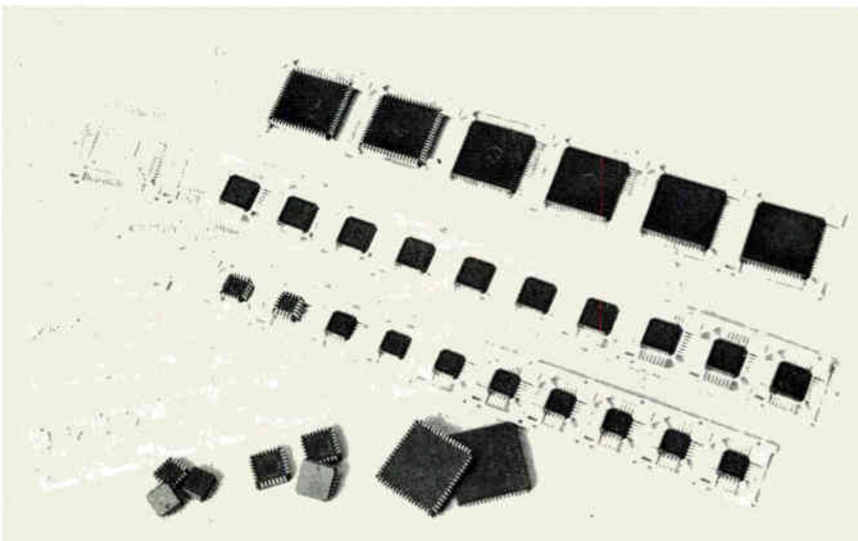
Their advent in mass now looks imminent. Texas Instruments Inc. has started supplying samples ICs in its new plastic leaded chip-carriers (PLCCs), and added impetus is in sight from Bell Laboratories, Murray Hill, N. J. The widely respected research facility has tested commercially available plastic chip-carriers from Amp Inc. of Harrisburg, Pa., and some it had concocted as well. Now it has gone on to an evaluation of their use in telecommunications hardware.

Confident. TI fabricates its PLCCs from the same materials and by the same assembly processes that it uses for its plastic DIPs. Thus TI is confident that its postmolded PLCC will stand up just as well in humidity and reliability tests as do its DIP counterparts, says John W. Orcutt of the company's central packaging operation in Dallas. His group is working on the promising new packages with several of the firm's product-line centers. Compared with DIPs, chip carriers cut package size and weight by some two thirds. Many semiconductor users already use ceramic versions for that reason. Plastic chip-carriers will slash costs—by a factor of two or three if history repeats itself in pricing—and bring a further reduction in weight as well.

So far, only Amp has put plastic chip-carriers on the market. Its carriers are premolded on the lead frame, and after the chips are bonded, they are potted with a silicone-gel compound to protect them from humidity. TI, on the other hand, uses a postmolded approach, encapsulating the bonded chips in thermosetting epoxy.

As for package outlines, TI's chip-carriers have the same footprint as Amp's. The sizes range from 350 mils square for a 20-pin package to 1.15 inches square for the 84-pin version. In fact, TI has been in contact with the firm to make sure its new PLCCs fit snugly in Amp's current plastic chip-carrier sockets. And TI has been discussing carrier characteristics with other major semiconductor makers in the hope that industry standards can be worked out. TI's PLCCs also have the same footprint as its own current ceramic versions, which are currently offered in more than 2,000 products.

Advanced levels. At present, TI has its sights on five pin-out levels for logic applications. Initially, 20- and 28-pin packages will be offered in advanced low-power Schottky products. Some are already being evaluated by customers; production quantities will follow next year. TI also plans to begin supplying sample 44-, 68-, and 84-pin PLCCs by the end of the year. These larger packages will house logic arrays. Orcutt says the



Advantageous. Plastic leaded chip-carriers may wind up as the most popular packages for complex integrated circuits. TI has started running characterization tests on them.

square plastic chip-carrier package should be able to handle up to 124-pin devices without passing the "practical limit."

During the past month, TI had no failures while running a test lot of 28-pin packages through both 85°C, 85% relative-humidity (RH) and "pressure cooker" tests. Complete package characterizations of the PLCCs will be completed by the end of the year.

Plastic leaded chip-carriers also stood up remarkably well in extensive testing at Bell Labs. Here, a quantity of special test chips in 28- and 68-pin PLCCs made by the labs from a silicone-epoxy compound and 24-pin types from Amp showed no failure modes when tested at 85°C and 85% RH, at 125° and 175°C under 40-volt static bias and under thermal cycling with no bias from −40° to +150°C. The results were reported earlier this month at the NEPCON '81 East Conference held at the Coliseum in New York.

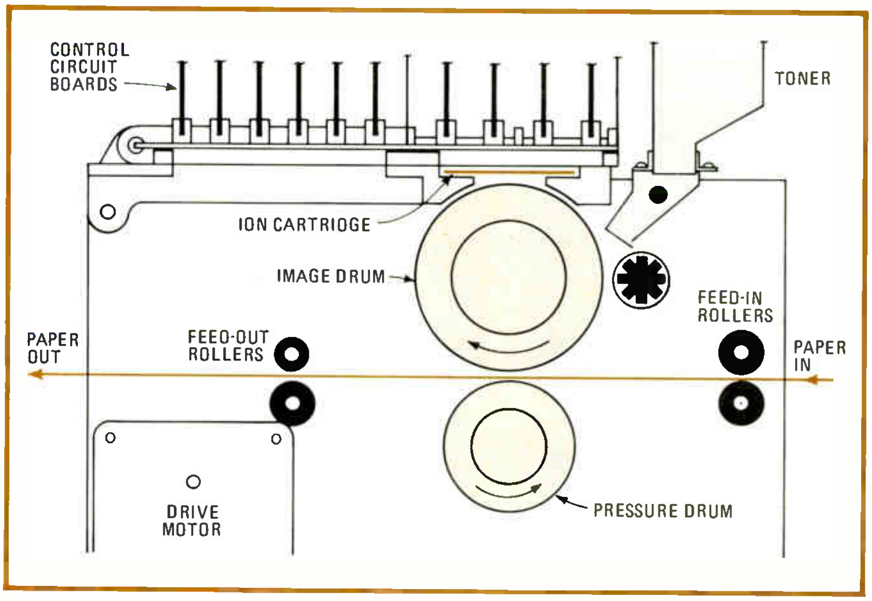
TI believes the PLCCs will be used in three general categories—with plastic sockets, on chip motherboards (which in turn are mounted on a printed-circuit board), and directly attached to pc boards. TI is in "a strong board-attachment development phase," Orcutt states. "We are working with customers and suppliers of pc boards and reflow equipment to develop the direct-board attachment."

Peripherals

Projected ions rival lasers for printing

Laser-beam printers, touted as the technological leader in high-speed, high-quality printers for computer-data output, are facing a challenge from a new imaging technology: ion projection.

The first printing mechanism based on this technology arrived from Canada this month when Delphax Systems of Toronto, Ont., introduced its model 2460 printing mechanism. It can churn out 60 8½-by-11-inch pages of alphanumerics and graphics per minute, a rate that matches that of all laser printers except the big top-of-the-line machines from Xerox Corp. and International Business Machines Corp.



A different drum. This printing mechanism forms charged latent images by projecting ions onto a dielectric drum. The images attract a toner, which is then transferred to plain paper.

With a resolution of 240 image-forming dots per inch, the reproductive quality of an ion-projected page is excellent. However, because it is simpler in construction and therefore more reliable, Delphax maintains that its new hardware will spawn printers selling for about half the price of currently available laser-beam models. These models start at $75,000 and can run as high as $300,000. For end users, Delphax says, ion-projection printers will bring total printing costs to about 1.5 cents a page in high volume.

Projected. With this technology, a dot-matrix pattern of ions—electrically charged atoms or groups of atoms—is projected onto a dielectric image drum (see drawing). The resulting charged image attracts a single-component iron oxide magnetic toner to the drum and then the image is transferred to plain paper by means of a pressure drum in a cold-fusion process.

The key element in the printer is the cartridge that creates the ions and projects them onto the drum. Completely solid-state and built much like a multilayer printed-circuit board, the cartridge has more than 2,000 individually controlled ion generators. Each of them has an insulating layer with an electrode on either side.

Overlapping. When an ac pulse of 1 kilovolt is applied across the electrodes, the surrounding air is ionized. Ions then speed through the matrix pattern of selected holes on the cartridge's lower surface, situated 0.008 inch from the dielectric surface of the image drum. There, the dots overlap each other by 50%; because of the overlap, solid lines can be printed.

The 60-gram cartridge and its electronics control system supplant about 300 pounds of complex electro-optical–mechanical hardware ordinarily found in a laser-beam printer. Instead of being two thirds mechanical and one third electronic as laser-beam printers are, ion-projection printers reverse this ratio. As a result, Delphax says, the mean time before failure of the model 2460 is more than 200,000 pages. An added bonus is that any part can be replaced in less than 30 minutes.

Replaceable. However, nothing is perfect. The holes in the cartridge get clogged with dust after about 100,000 pages have been printed. Thus Delphax considers the cartridge a consumable item and has designed the printing mechanism accordingly. An operator can easily replace the cartridge, which will cost about $200 to the end user.

Delphax plans to have prototypes of the printing mechanism with its control electronics available for evaluation in the third quarter of 1981. Volume production is scheduled to start early in 1982, and the model 2460 should sell for $8,000 to printer producers who buy at least 500 units a year. That means a complete printer may be priced at between $35,000 and $50,000.

The company estimates that the worldwide nonimpact printer market is currently $400 million, or 5% of the electronic printer market. Delphax is projecting the nonimpact sector to grow to $6 billion by 1985—approximately 25% of the total printer market. **-Tom Manuel**

Instruments

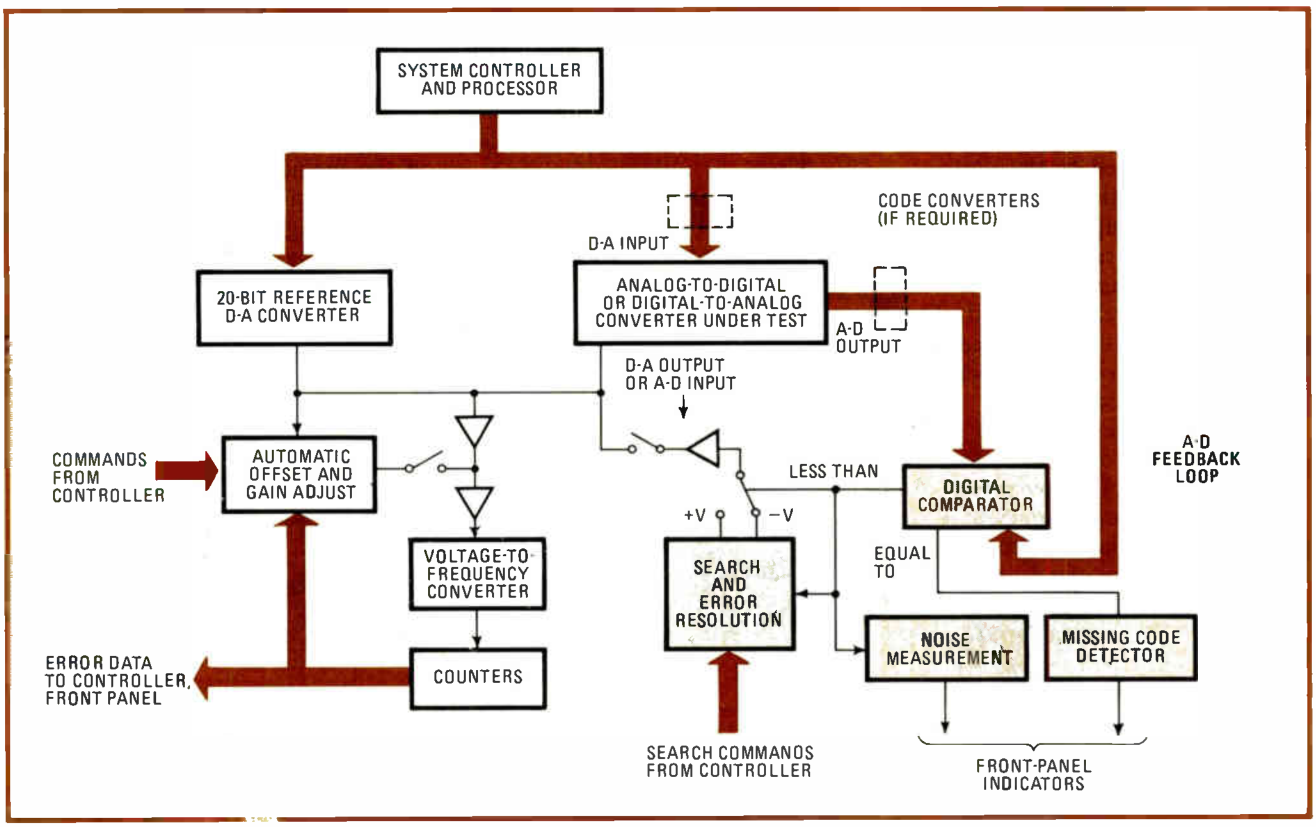
NBS calibrates data converters that resolve up to 18 bits

The recent flurry of analog-to-digital and digital-to-analog converters having resolutions as high as 18 bits is challenging the measurement capabilities of many companies. To help them face the challenge, the National Bureau of Standards stands ready with a new converter calibration service based on a specially built test system.

"There are a lot of converters that people don't have a good way to measure," explains Michael Souders, the physicist in charge of the new service, offered by the NBS's Electrosystems division in Washington, D. C. He says that no standards have been set for high-resolution converters and that "a lot of people have asked that we improve the situation by offering a standard test method."

Presumably, an improvement will be widely welcomed. Referring to his company's 18 bit d-a converter, a spokesman at Analog Devices Inc. in Norwood, Mass., agrees. "People don't know how to test them. We have to do it and it's a long and expensive test procedure," he explains. For its 18-bit part, the company provides buyers with a certificate that guarantees that the measurements performed in house on the part are traceable to NBS primary standards. To make such measurements, Analog Devices built its own costly test system using NBS-calibrated instrumentation.

In agreement. Robert Leong, principal development engineer for GenRad Inc.'s Component Test division in Bolton, Mass., rates the NBS's new service as "very interesting, particu-



High standards. The National Bureau of Standards built this highly accurate test system to calibrate d-a converters having a resolution of 12 bits or more. By using the output of the 20-bit reference d-a unit as an input, the system checks a-d converters as well.

larly for a-to-ds." He believes that NBS-traceable converters will become internal laboratory standards to check production parts. Souders concurs. "We expect that test system manufacturers will use the service to calibrate the converters in their test setup," he says.

To provide a standard test service, Souders' group at the NBS fabricated its own 20-bit d-a converter reference (see diagram). "It doesn't use any fancy technology," Souders says. Instead, it employs mercury-wetted relays to switch weighed bit currents from precision-resistor networks onto a summing point where the analog output appears. The relays have very low, repeatable contact resistance and thus help keep the uncertainty contributed to the measurement by the test system itself down to as little as 3 parts per million. Further, the system can calibrate a-d units with high precision using a unique feedback technique and the 20-bit reference converter.

Comparisons. For d-a units, the system applies up to 1,024 different code words to both the 20-bit standard and the converter under test and compares the two analog outputs. For a-d parts, on the other hand, the output of the reference converter is applied to the unit undergoing calibration. A feedback loop adjusts this input until the digital output of the test part is just at the point of transition to the test value fed to the reference unit. The adjustment needed to make the match is a measure of the accuracy of the converter under test.

At present, the NBS can make static measurements on converters with a minimum of 12-bit resolution and an error of less than 500 ppm. A-d parts must have a conversion rate of 100 microseconds or better for the test system to operate efficiently, precluding calibration of slower converter types such as dual-slope units. Eventually, the bureau expects to upgrade its test system so that it will be able to run dynamic tests as well.

The NBS has not yet set a firm schedule of fees for the service, but Souders expects that a basic linearity calibration will run about $240, with an extra charge for a fix on a converter's differential linearity. In making these measurements, the gain and offset of the converter are trimmed beforehand, if that can be done using the unit's own trimmers. The gain and offset can also be measured on request, as can the root-mean-square input noise of a-d converters. -Richard W. Comerford

Memories

NSC forges ahead with triple-poly RAMs

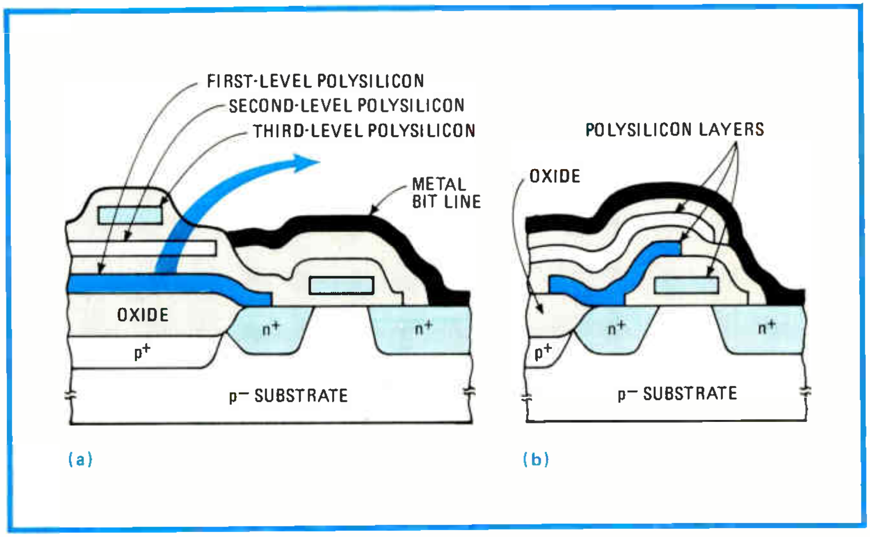
National Semiconductor Corp. is pushing ahead with its pioneering three-polysilicon-layer 64-K dynamic random-access memory. It had been rumored in the industry that inadequate yields were forcing the company to revert to a double-polysilicon part it was designing in parallel. But in fact, the Santa Clara, Calif., chip manufacturer has made ready for volume production later this year, having shifted the triple-polysilicon memory and some of the part's design team to the firm's new manufacturing facility in Salt Lake City, Utah.

Industry insiders generally believe that National's triple-polysilicon process is intended only to reduce die size and raise the quality of on-chip storage capacitors. But the company's idea turns out to be even more forward-looking than that. Andrew G. Varadi, vice president and group director for memory components, says that the three polysilicon layers will also help National prepare for the highly vertical structures necessary for future integrated circuits like a 256-K RAM.

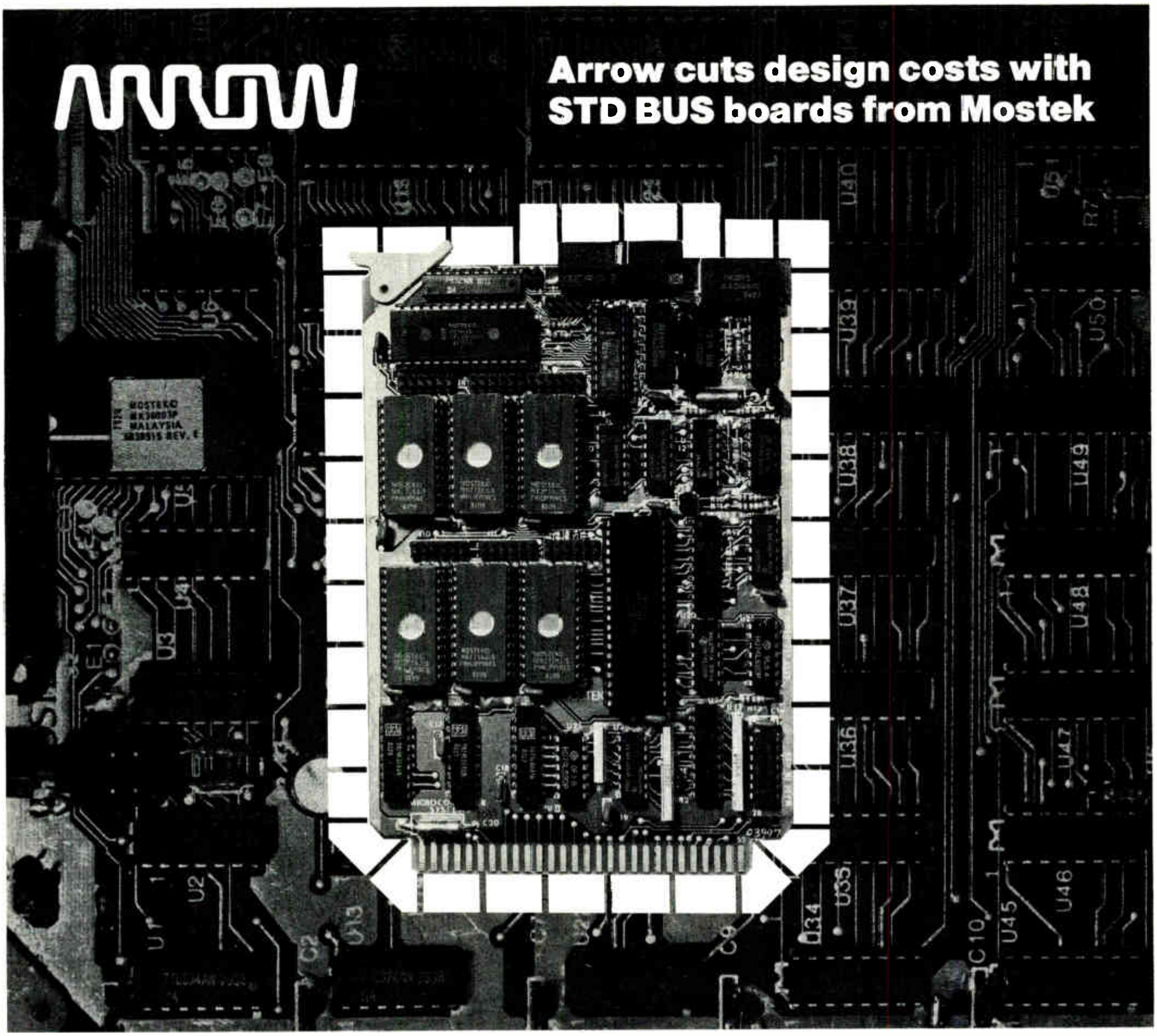
For its 64-K chip, the company uses rather conservative 3-micrometer design rules, compared with the 2.5-μm found in other 64-K RAM designs. But thanks to the three layers of polysilicon, the chip that National is taking to market is, at less than 30,000 square mils (19.4 square millimeters), the smallest of its class in the industry. And, says Varadi, when his company scales down to 2.2-μm geometries, the 64-K memory will approach 20,000 mil^2 (12.9 mm^2).

National's 5-volt-only 16-K RAM, the NMC 5295, is built with the same triple-polysilicon process. Measuring only 13,000 mil^2 (8.4 mm^2), it is the smallest 16-K memory in production.

Stacked. Moreover, for future RAMs, National intends to take the storage capacitor and flop it on top of the memory cell's access transistor, thus drastically reducing the size of the storage array and the memory chip (see figure). Varadi notes that



Packing them in. National intends to shift the storage capacitor from its conventional position (a) to one on top of the access transistors (b) to cut cell area in its RAMs.



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the resulting structure is precisely the one arrived at by Japan's now-defunct government-funded VLSI Cooperative Laboratories. The VLSI co-op labs called its memory cell quadruply self-aligned and with it built a half-megabit stacked-capacitor RAM [*Electronics*, March 13, 1980, p. 42].

In fact, Varadi is surprised at the simularities between the two approaches. Both schemes come extremely close to the ultimate for a tiny RAM cell, he says, one that measures two by three times the minimum lithographic feature length. Also like the Japanese, National intends eventually to replace one or more of the polysilicon layers with metal or a metal silicide to reduce signal attenuation (the co-op lab used molybdenum).

Varadi maintains that the stacked-capacitor idea is "basically a very minor adjustment to our triple-poly process." In addition, National is upgrading older single-layer–polysilicon 4-K static RAMs and developing new 16-K static RAMs with a 2-μm double-polysilicon process that promises to enhance access times and yields.

If National can pull off the triple-polysilicon process, it maintains, there will be a payoff in highly cost-effective dynamic RAMs. But others say it is a mistake to bet on stacked capacitors. As structures become more and more vertical and horizontal features diminish, they say, vertical dimensions, too, will have to be minimized in order to avoid step-coverage problems. For that reason, some companies are trying to go from two levels of polysilicon back to one, as Inmos Corp. did in its 16-K static RAM [*Electronics*, Sept. 11, 1980, p. 117]. **-John G. Posa**

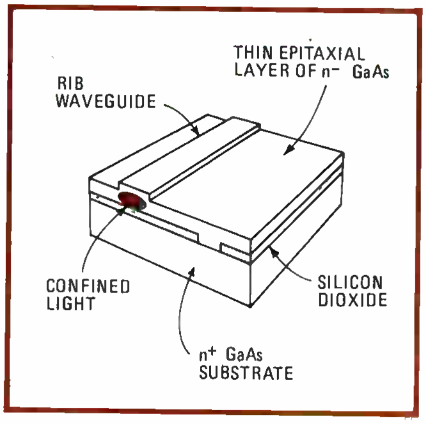
Optoelectronics

Thin oxide layer under GaAs epitaxy confines light in optoelectronic IC

Optoelectronic monolithic integrated circuits promise very high speeds, so it is not surprising that much development work aims to combine optical circuitry with ultrafast gallium arsenide semiconductor technology. But before commercially viable ICs based on the combination can come about, optical attenuation and bend radii problems in GaAs waveguides need to be solved.

A group of scientists at the Lincoln Laboratory of the Massachusetts Institute of Technology has taken a significant step toward a solution with a new method of building optical waveguides on GaAs substrates. Not only does the approach achieve lower attenuation than with earlier GaAs waveguides, it also offers the promise of smaller radii for waveguide bends. That would translate into smaller overall geometries in future devices.

The Lexington, Mass., group has created GaAs optical waveguides with measured attenuations of only



In confinement. Large differences in the indexes of refraction of GaAs, SiO_2, and air help prevent light from escaping from new low-loss monolithic waveguide.

2.3 decibels per centimeter, at a wavelength of 1.06 micrometers. That is far better than the 4 dB or more of attenuation achieved so far for GaAs waveguides formed through doping. Better still, it is within striking distance of the 1 dB/cm attenuation achieved with nonsemiconductor materials. Moreover, according to team members, the new approach, called oxide confinement, could reach that magic 1-dB number perhaps by merely taking added care during etching.

Buried layer. The team experimented with a number of guide geometries, but the most successful to date resembles a rib or ridge when viewed in cross section (see drawing). The rib is etched into the surface of a layer of epitaxial GaAs using standard semiconductor processing techniques. Crucial to the structure is a buried silicon dioxide layer that forms the underside of the guide. This buried layer, plus sharp GaAs-air boundaries on the guide's upper surface and sides, prevents light from seeping laterally into the lossy n^+ GaAs substrate that surrounds most monolithic guide structures.

For the same reasons, tighter bends are possible in the rib waveguide. Light simply has a much tougher time escaping from it because its lateral seepage is as much as one hundred times less than through the walls of a guide formed by doping. Thus the new waveguides can have either the same geometries as doped waveguides but with lesser attenuation or tighter bends with the same attenuation.

Spread out. The construction of an oxide-confined GaAs optical circuit begins with a single crystal of n^+ GaAs on which a film of silicon dioxide, around 3,000 angstroms thick, has been laid down. Next, stripe-like openings to the GaAs are etched in the silicon dioxide, and the wafer is placed in a vapor-phase epitaxy chamber. Growth of new epitaxial GaAs begins in the slots, but quickly spreads laterally over the oxide surface to form a uniform, single-crystal layer. The process is called lateral epitaxial growth and is similar to the laboratory's Cleft GaAs wafer-production system [*Electronics*, May 19, p. 38]. It also retains Cleft's advantages of speedy production and economical use of materials.

Once the upper GaAs layer is formed, any desired waveguide pat-

tern can be etched into the surface of the wafer or a die. Typical guides so far have run about 6 μm wide and about 0.5 μm high.

The team also found it possible to form Schottky barriers both in and on the epitaxial GaAs. The barriers' voltage breakdown was high and the leakage low. This important side benefit should simplify the task of interfacing the optical with the electronic sections of optoelectronics ICs, according to team, perhaps making it easier to place optical emitters and detectors in and around electronic circuitry. **-James B. Brinton**

News briefs

Need for engineers may be surprisingly high
Despite softening markets, the electronics industries may be hard pressed to find the technically trained manpower they will need over the next four years. Responding to a survey made by the American Electronics Association, 671 companies reported that they will need some 55,300 new electronics engineers and computer science engineers, 18,700 technicians, and 66,400 assemblers through 1985. The data suggests that the need for technical workers "may be greater than we had imagined," says Pat Hill Hubbard, manager of technology and careers for the Palo Alto, Calif.–based industry association.

RCA will boost video-disk capacity
A scant three months after the large-scale introduction of its SelectaVision video-disk system, RCA Corp. reports that the demand for disks has been brisk enough for the firm to increase substantially its disk-pressing capacity. The expansion program will boost production capacity to 3 million disks by the end of 1981 and then up to 10 million in 1982. Eventually, the company's Consumer Electronics division in Indianapolis, Ind., estimates, it will need to make 30 million disks a year. RCA initially forecast that player sales would run 200,000 units this year; so far consumers have bought slightly more than 28,000.

NCR to join semiconductor merchants
The prospect of lucrative markets for nonvolatile memories and semicustom logic devices during the 1980s has lured NCR Corp. into the merchant semiconductor business. Within the next 30 days, the Dayton, Ohio, computer systems manufacturer says it will begin supplying samples of a new family of electrically erasable programmable read-only memories ranging in density up to 16-K. Also planned for sale to outsiders is a 2-K static random-access memory fabricated with MOS technology and a line of MOS semicustom logic circuits that will capitalize on NCR's internal standard-cell-library design technique. The EE-PROMs will be built using the company's metal-nitride-oxide-semiconductor technology and will be offered in both block- and word-alterable versions. Customer relations and initial fabrication of the new chips will be handled at the company's Miamisburg, Ohio, plant.

Computers

CDC couples CPUs in fast network

Local networking has been an industry buzzword of late, with most of the buzz emanating from low- to medium-speed equipment for linking together small computers, terminals and peripherals. But now Control Data Corp. is quietly slipping into the high end of the networking business with a product aimed at high-speed mainframe-to-mainframe communications for large computer centers.

That, presumably, is good news for Minneapolis-based CDC, whose sales in 1980 totalled $3.8 billion. But it could be bad news for Network Systems Corp. of Brooklyn Park, Minn., whose sales are a fraction of a percent of those of CDC. That company has so far had the market for high-speed networking virtually to itself. But if CDC is successful with its new product, other mainframe vendors may enter the market as well.

Name your brand. CDC's Loosely Coupled Network (LCN) breaks new ground among mainframe manufacturers because it is designed for use with processors supplied by other vendors as well as CDC's own. To date, says Roger L. Meyer, the firm's director of communications systems for computer products, LCN is capable of interconnecting the 360, 370 and 303X series of International Business Machines Corp. and the PDP-11 machines of Digital Equipment Corp. in addition to CDC's 6000, Cyber 170 and Cyber 200 series. In every case, however, at least one CDC machine must be included in the system.

LCN employs interfaces called network access devices to tie mainframes and peripherals to a coaxial-cable data trunk for bit-serial communication at speeds of up to 50 megabits per second. In contrast, only a 10 megabit-per-second speed is possible, for example, with Ethernet, the networking scheme aimed at linking office automation equipment that is backed jointly by Xerox Corp., Intel Corp., and DEC.

With LCN, each network access device ties into as many as four different trunks simultaneously and each trunk can accommodate 27 different drops, thus bringing total network potential to 108 different units, says Meyer. Processors on the LCN net can be located up to 3,000 feet apart. One access device is needed per mainframe, and CDC charges between $40,000 and $45,000 for it.

Large transfers. CDC officials note that the development of the network was spurred by the needs of its existing customers, many of whom employ four to six mainframes from several vendors for large-scale applications such as scientific and engineering pursuits. Typically, these users must transfer data files from one machine to another for load sharing or to take advantage of the processing attributes of a particular mainframe. Since only one access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device is required per processor to enable communications with any other machine in the net, hardware and software requirements are less than in the channnel-to-channel schemes used in some installations. CDC will provide LCN software designed both for permanent file transfer between processors and for transferring queued job files for processing elsewhere. Software prices will run from $6,000 to $20,000 per mainframe.

Processor access to the LCN trunk is by rotating priority, with user-defined data blocks of 512 to 4,096 bytes transmitted in a synchronous-burst mode. CDC developed its own protocol for its new network. Current standard common-carrier protocols such as X.25 would not be efficient for the high data rates used with LCN, explains Alan E. Potter, program manager for development on the project.

In a niche. Network Systems Corp.—formed in 1974 by several former CDC engineers—had $13.1 million in revenues last year. Vice president for development Gary S. Christensen concedes that his company's Hyperchannel product was designed for 50-Mb/s operation partly because high-speed networking was "a market refuge" where no other companies were competing when the product was brought out in 1977. But Christensen professes not to be alarmed over the upcoming competition from CDC. Nor does he fear that other large mainframe manufacturers might crowd into his niche.

With some 107 Hyperchannel installations already in place and adaptors available for some 25 different CPUs, Network Systems figures it has a healthy lead and that it would be hard for anyone to catch up, much less pull ahead. What's more, Christensen says, the market for high-speed mainframe networking products is too small to entice many large computer manufacturers. Interestingly, however, Network Systems' most recent annual report pegs the potential for high-speed networking products within the world's top 1,500 computer centers at some $1 billion. **-Wesley R. Iversen**

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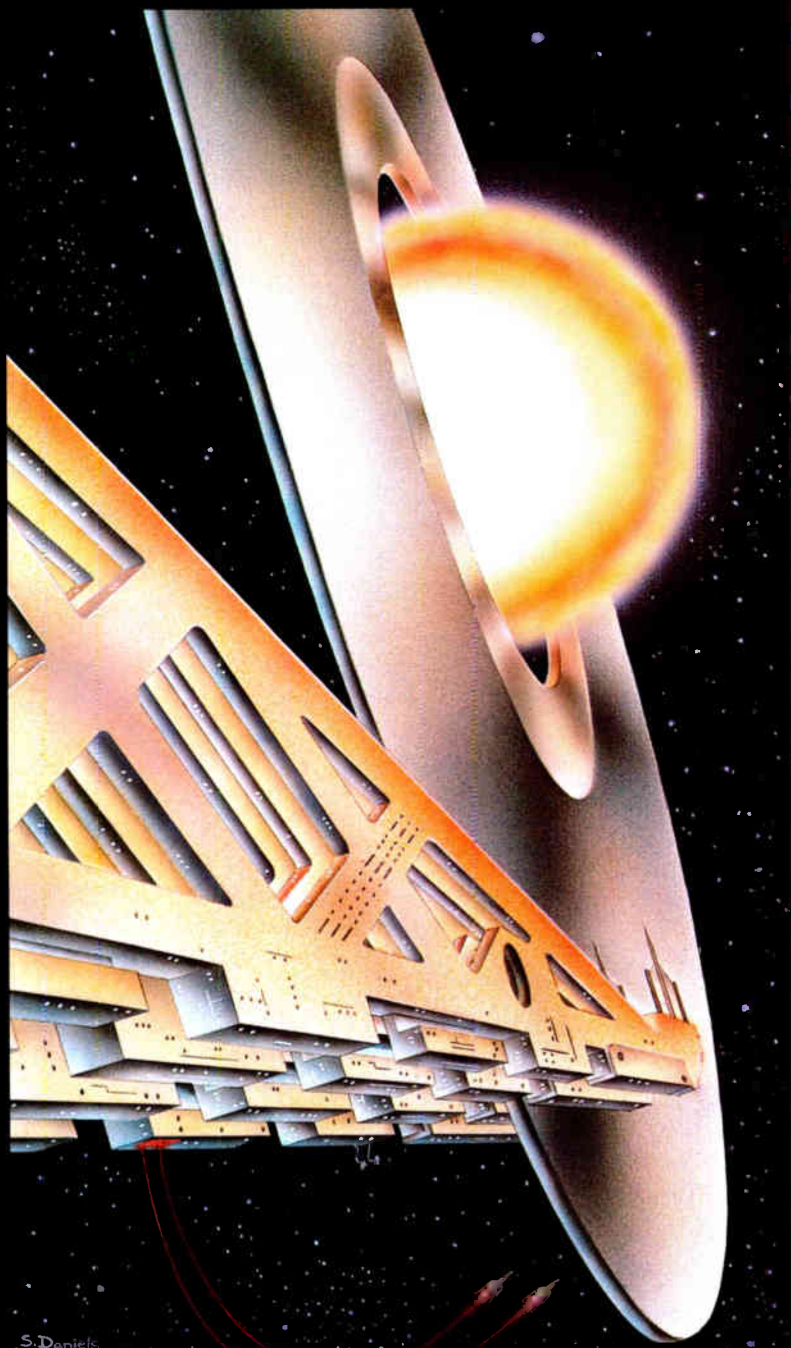

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Plus, by using a BI-FET™ input stage, the LH0101's 300pA input bias current is 100 times less than any other comparable amp on the market. And if this isn't enough, the LH0101 also offers extremely low distortion specs: 0.008% with undetectable cross-over distortion.

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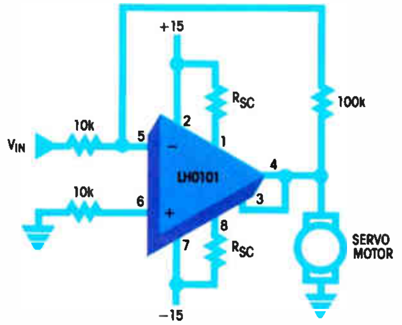

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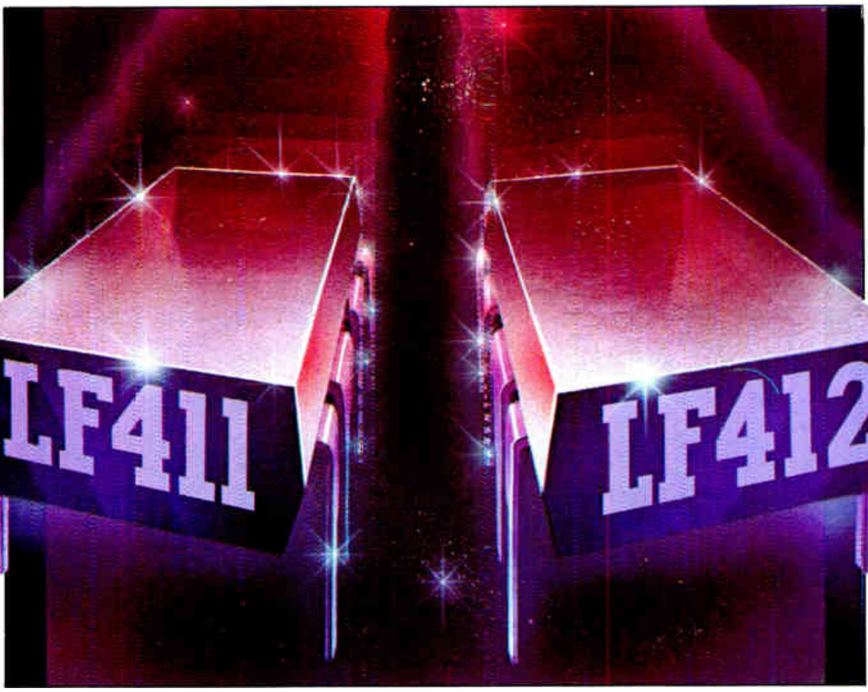
National redefines BI-FET™ op amp standards.

The new LF411 single and LF412 dual op amps—made with National's BI-FET II™ technology— are soon to become industry standards.



Having invented BI-FET technology five years ago, the linear leaders at National continue to lead the industry in BI-FET innovation.

Their new LF411 single and LF412 dual BI-FET op amps feature very low, internally trimmed input offset voltage: 0.5mV (max) for the LF411 and 1mV (max) for the LF412.

And with a guaranteed maximum input offset voltage drift of only 10μV/°C, output errors are reduced and the need for offset adjustments is eliminated. In addition, they maintain a wide 3MHz (min) gain bandwidth and a high 10V/μsec (min) slew rate while requiring a low 1.8mA supply current per amp.

The new standards improve system performance. The LF411/412 op amps are the logical choice for designs such as high-speed integrators, fast D/A converters, S & H circuits and a multitude of other designs requiring superior performance specs.

Conveniently enough, the LF411/412s are pin-compatible with the standard LM741/1558s, respectively. So designers can immediately upgrade the overall performance of their existing designs.

All this performance at spectacularly low prices. These op amps are typical examples of the linear leader's ability to provide high performance parts in high volume at low prices.

Available in both plastic 8-pin DIPs or 8-lead TO-5 cans, the LF411 sells for $.59* and the LF412 for $.99* each in quantities of 100 and up.

For data sheets on these advanced op amps, check box number 078 on the National Anthem coupon.

And start designing in the new industry standard for high performance, low cost BI-FET op amps.

*U.S. prices only.
BI-FET and BI-FET II are trademarks of National Semiconductor Corporation.

National flexes their BI-FETs.

In 1975, the linear leaders at National made significant strides forward when they first introduced BI-FET technology. Because the op amps that resulted were the first monolithic op amps that combined low input bias current and high impedance with high speed.

This winning combination was further reinforced with each new BI-FET product introduction. The LF355, LF356, LF357 and the LF347.

Then, in 1978, these same Practical Wizards pioneered an extension of their field-proven technology: BI-FET II. The enhancements incorporated into BI-FET II include faster FETs and trimming of the input offset voltage of each amp.

The results of these efforts, as epitomized by the LF411 and LF412 op amps, show up in higher performance at a lower cost.

This is exactly the kind of practical innovation that has maintained National's linear leadership for over ten years.

1975 THE BI-FET LINEAGE

BLX modules create expanding board level versatility.

National offers the industry's broadest line of low cost expansion modules for Multibus™ host boards.

It's the BLX solution—National's board level expansion for BLC users that the competition can't even begin to match. And it brings total versatility to SuperChips™ board system designs.

On-board functional expansion is accomplished by plugging any of National's low cost BLX modules directly into sockets on their BLX-compatible host boards. Each of the BLC-80/11A, BLC-86/12B and BLC-80/116 host boards can accept any two expansion modules.

Cost- and space-saving configurations are now just a matter of choosing which modules provide the best approach.

Modules are available to expand board level capabilities with speech synthesis, analog output, fixed or floating point math, parallel I/O, serial I/O, bubble memory and prototyping.

Soon, however, the growing BLC line will expand to cover National's broad line of semiconductors—the industry's broadest.

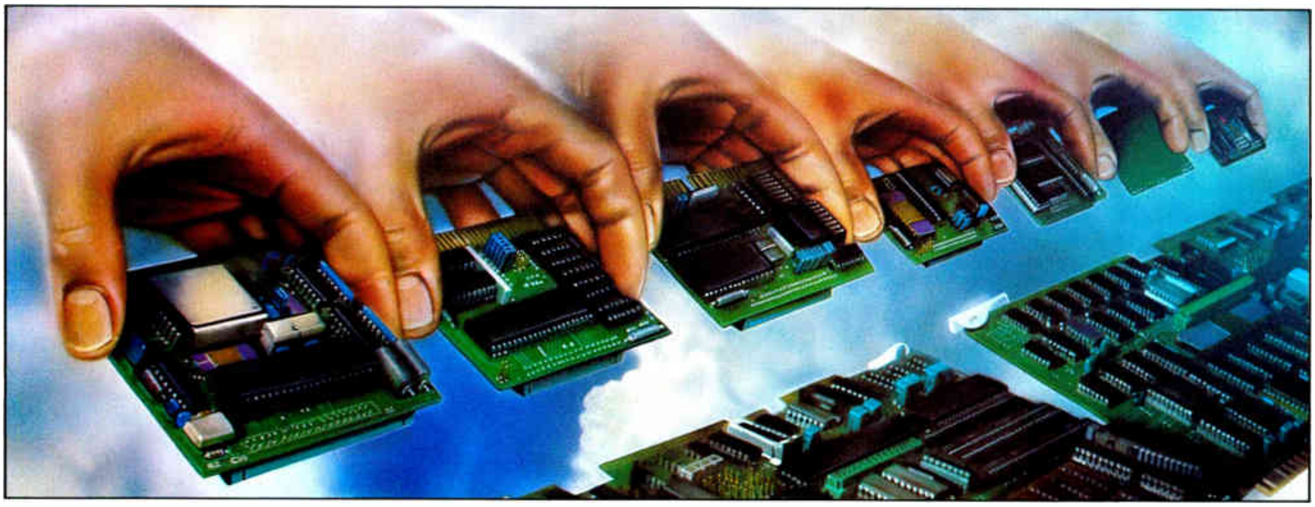
12-month warranty. National's established manufacturing capabilities and technical innovation make them the logical choice for board level leadership from the chip up—with a full 12-month warranty.

For example, everyone has boards that compute and remember. There's no trick to that. But National has boards that translate (BLC-8488 Intelligent GPIB Controller), talk (BLX-281 Speech Synthesis Module) and measure (BLC-8737 & BLC-8715 Analog I/O Boards). The fact is, no one else can touch them in board technology.

Modules and SuperChips. Because man cannot live by chips alone.

For more information, just check box 088 on this Anthem's coupon.

SuperChip is a trademark of National Semiconductor Corporation.
Multibus is a trademark of Intel Corporation.



Titanium-tungsten fuses improve the reliability of 16K PROMs.

National's bipolar PROMs guarantee an extra measure of reliability, thanks to titanium-tungsten fuses and today's high volume Schottky production processes.

National's 87S190 and 87S191 state-of-the-art 16K bipolar PROMs are an example of their bipolar wizardry. They're as fast and as large as any PROMs in the industry. And yet their titanium-tungsten fuses and high volume Schottky production process gives them rock-solid reliability.

These high-speed PROMs are Schottky-clamped for a typical address access of 40 ns and a typical enable access of 20 ns.

As an additional measure of practical reliability, this family of PROMs uses titanium-tungsten as a buffer between the aluminum interconnect and the platinum-silicide "barrier."

They use the same basic production flow as for standard Schottky bipolar RAMs and other logic circuits. It's a proven process that works time-after-time.

For more information check box 096 on the National Anthem coupon.

SCANNING ELECTRON MICROPHOTOGRAPH OF NATIONAL'S TITANIUM-TUNGSTEN FUSE IN THE OPEN STATE.

PROM SUMMARY TABLE

Part Number	T_{AA} (max comm)	Organization
DM74S188/288	35	32 x 8
DM72S287/387	50	256 x 4
DM74S570/571	55	512 x 4
DM74S472/473	60	512 x 8
DM74S474/475	65	512 x 8
DM74S572/573	60	1024 x 4
DM87S180/181	60	1024 x 8
DM87S184/185	55	2048 x 4
DM87S190/191	65	2048 x 8

National is dedicated to rapid deployment of military MOS memories.

Only National has the technical expertise and manufacturing muscle to deliver MOS memory products in volume—with truly competitive pricing.

The MIL-STD-883 screened military MOS memory products from National have hit the market in full volume. They're supplying large scale orders for customers on all of their high rel MOS memory devices, from RAMs to EPROMs—effective immediately.

Their solid advantage in this market is their low prices combined with the best delivery times available.

The Practical Wizards have just stepped up their wafer fabrication capacity at their Salt Lake plant and increased their assembly and test capacity worldwide. They can now ship more parts in one month than most suppliers can ship in six.

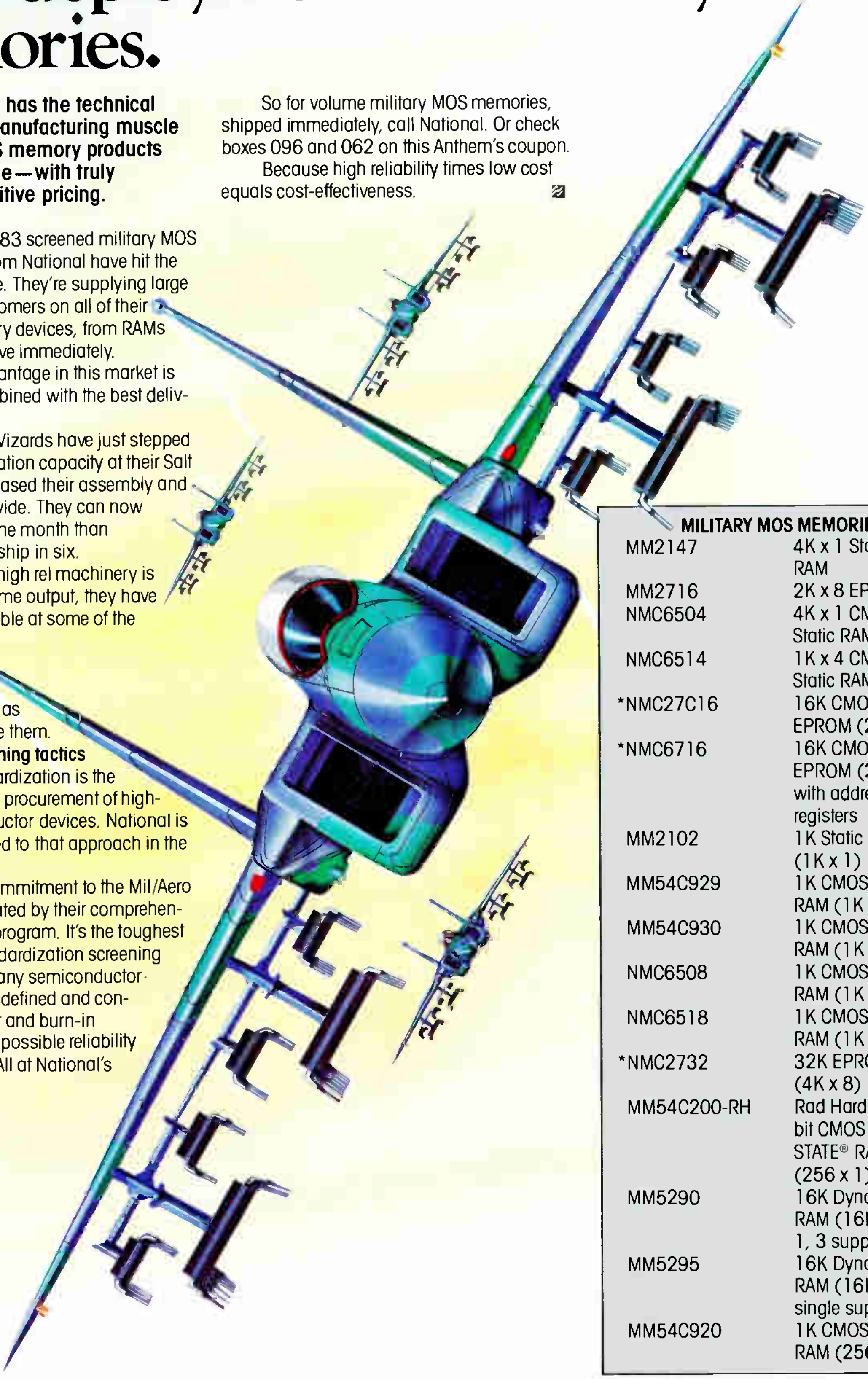
Because their high rel machinery is geared for high volume output, they have these devices available at some of the most aggressive pricing structures yet. So they're filling orders as fast as they can take them.

National's winning tactics on reliability. Standardization is the key to cost-effective procurement of high-reliability semiconductor devices. National is especially committed to that approach in the Rel business.

Their strong commitment to the Mil/Aero market is demonstrated by their comprehensive 883B/RETS™ program. It's the toughest fully compliant standardization screening program offered by any semiconductor manufacturer. Their defined and controlled electrical test and burn-in achieve the highest possible reliability factor per product. All at National's volume prices.

So for volume military MOS memories, shipped immediately, call National. Or check boxes 096 and 062 on this Anthem's coupon.

Because high reliability times low cost equals cost-effectiveness.



MILITARY MOS MEMORIES

MM2147	4K x 1 Static RAM
MM2716	2K x 8 EPROM
NMC6504	4K x 1 CMOS Static RAM
NMC6514	1K x 4 CMOS Static RAM
*NMC27C16	16K CMOS EPROM (2K x 8)
*NMC6716	16K CMOS EPROM (2K x 8) with address registers
MM2102	1K Static RAM (1K x 1)
MM54C929	1K CMOS Static RAM (1K x 1)
MM54C930	1K CMOS Static RAM (1K x 1)
NMC6508	1K CMOS Static RAM (1K x 1)
NMC6518	1K CMOS Static RAM (1K x 1)
*NMC2732	32K EPROM (4K x 8)
MM54C200-RH	Rad Hard 256-bit CMOS TRI-STATE® RAM (256 x 1)
MM5290	16K Dynamic RAM (16K x 1, 3 supply)
MM5295	16K Dynamic RAM (16K x 1, single supply)
MM54C920	1K CMOS Static RAM (256 x 4)

*Available Fourth Quarter

PALs save money and space on tight TTL SSI/MSI designs.

Immediate PAL™ design-in made feasible by steadily declining prices.

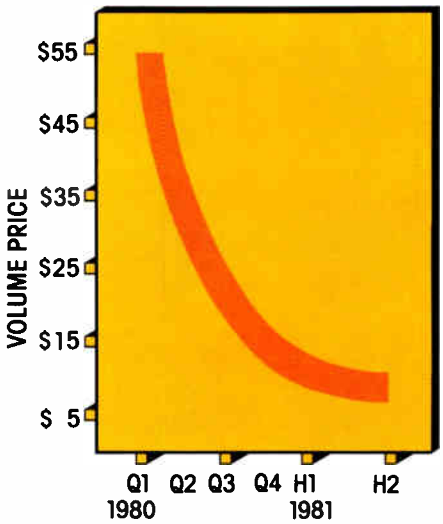
PALs (Programmable Array logic) are designed to replace standard TTL logic. A single PAL can replace from 4 to 12 SSI/MSI packages.

At the higher levels of package replacement, PALs, in volume, are now cost-competitive with the SSI/MSI parts they replace.

So now design engineers can benefit from both PAL price reductions as well as considerable savings in board space. National's technical expertise and volume production capabilities have allowed them to offer PALs at the lowest prices ever.

At the lower replacement levels, PALs can still be cost-justified if an entire PC board can be eliminated. This often happens when a few more logic functions are required than a single board can accommodate.

And PAL devices are fully field-programmable to provide the utmost in design flexibility and efficiency.



PAL PRICES CONTINUE DOWNWARD

PAL's basic logic implementation is the familiar AND-OR array, where the AND array is programmable and the OR array is fixed.

PAL's standard AND-OR logic and flexible I/O programming provides design and production efficiency unknown up to now. That's because logic modifications can be made more quickly and easily with PAL than with discrete random logic.

National is producing TTL-compatible PALs with the same time-tested technology used to manufacture PROMs. Their Titanium-Tungsten fuses have been proven reliable both through internal rel testing and three years of field use.

Program development and debugging on standard PALs is supported by National's STARPLEX™ development system.

And with 15 different PAL devices to choose from, logic design efficiency and reliability is truly maximized.

To obtain a PAL brochure and data sheet simply check box 025 on this Anthem's coupon.

National—the volume source for cost-effective, reliable PALs.

PALASM™. National's new software to develop PALs™.

The easy-to-use PAL assembler supports PAL programming on STARPLEX™, the fully developed development system.

The Practical Wizards have recently introduced complete development support for their entire line of standard PAL (Programmable Array Logic) devices.

It's called PALASM—a new software module executed on their powerful STARPLEX development system. PALASM serves as the software interface between the STARPLEX system bus and the optional Universal PROM Programmer and its associated PAL personality card.

Basically, PALASM converts PAL logic (Boolean equations, etc.) into a form that the Universal PROM Programmer can readily understand. So it can then turn around and burn that logic into the PAL array.

Easy-to-use development interface. PALASM offers the programmer a highly interactive, easy-to-use method to develop and debug PAL logic. It does, for example, allow PAL programs to be debugged in standard PROM debug mode.

This same convenience-oriented approach to PAL programming is, in fact, carried throughout the versatile STARPLEX system.

Because in addition to PALs and PROMs, STARPLEX with ISE™ (In-System Emulation) is used to develop, test, analyze and debug prototype hardware/software for all of National's programmables: INS8080, INS8048, INS8049, INS8050, INS8070, 8085 AND NSC800 microprocessors, COPS™ microcontrollers, and even Z-80® μPs. Plus their line of board level microcomputer products.

And now, with the addition of PALASM, STARPLEX is truly the fully developed development system.

Check box 085 on the coupon for additional information.

Transducers at their best in the worst.

Two new abusable pressure transducers—built to take millions of pressure cycles in stride.

National continues to broaden its line of dependable low cost IC pressure transducers with two new series: the LX04XXA and LX05XXA/0.

Both new products are monolithic absolute transducers that operate at pressure levels up to 3000 psi with an overpressure rating to 5000 psi.

Since they're designed with metal-to-metal seals, these abusable transducers function consistently and reliably over literally millions of pressure cycles.

The LX04XXA, ruggedly packaged in a concentric PX4AS stainless steel housing, is quite at home in a hostile working environment. This compact package design allows easy installation (a crescent wrench will do just fine). Its ten-inch flying leads—epoxy sealed for extra protection—lend themselves perfectly to easy soldering and secure electrical connection.

The LX05XXA/0 transducer features a gold-plated Kovar TO-5 header (PX5A0) with a nickel cap, so they're quite suitable for PC board mounting.

So whether it's in an automobile engine, robotics, hydraulics, pneumatics, or even deep well pumps, the LX04XXA and LX05XXA/0 Series offer high accuracy and stability.

For complete details on these low cost, high performance absolute pressure transducers, be sure to check box 097 on this issue's National Archives coupon.

P²CMOS™: a new generation of low power high performance RAMs.

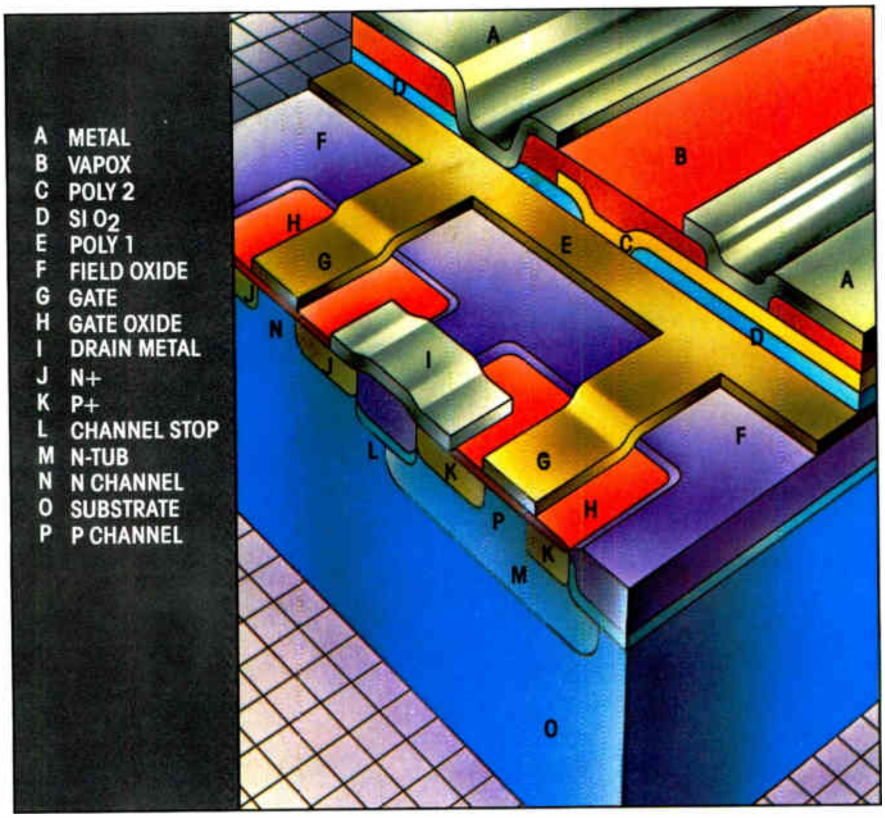
National leads the industry with their new P² CMOS memories.

P²CMOS, National's silicon-gate complimentary-MOS process, has made possible a whole new generation of static RAMs.

These high density RAMs employ two levels of polysilicon interconnect and one level of metal interconnect and the result is NMOS speed at CMOS power.

And these RAMs—available in military, commercial and industrial versions—take full advantage of P²CMOS, higher reliability, low power and heat dissipation, and improved immunity to system noise and alpha particles.

For data sheets and additional information check box 064 on the National Archives coupon.



P²CMOS STATIC RAM FAMILY

Part Number	T_{AA} (ns)	Organization
NMC 6508	180-300	1K x 1
NMC 6518	180-300	1K x 1
NMC 6551	220-350	256 x 4
NMC 6552	220-350	256 x 4
NMC 6503	300-350	2K x 1
NMC 6504	300-350	4K x 1
NMC 6513	300-350	512 x 4
NMC 6514	300-350	1K x 4

The Practical Wizards' new book of Logic.

The Practical Wizards have just published a complete, single volume library of technical information on their extensive line of bipolar logic devices.

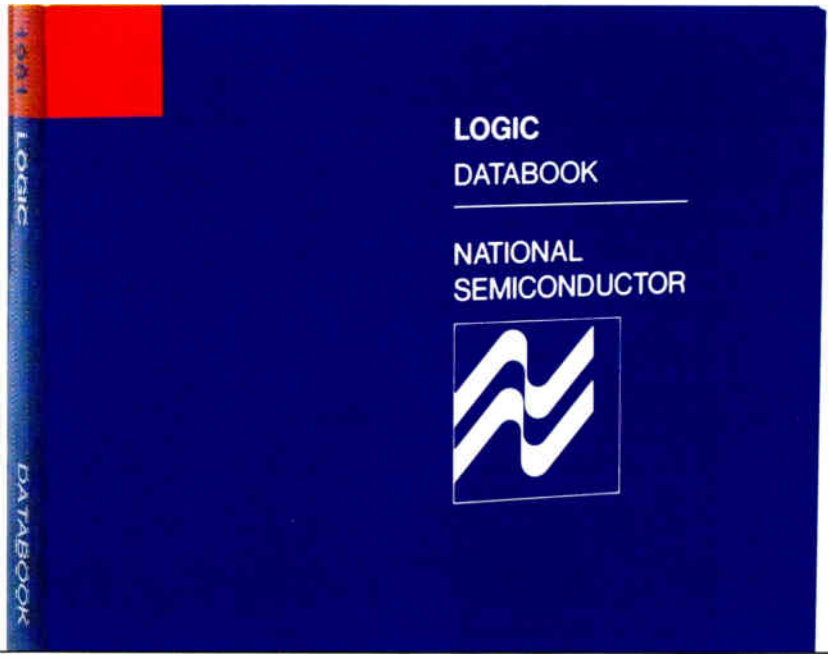
National's new Logic Data Book covers five of their logic families: TTL (54/74), Schottky (54S/74S), low power Schottky (54LS/74LS), high speed (54H/74H), and low power (54L/74L).

The Logic Data Book—specially organized for quick and easy referencing—offers two complete functional indices and selection guides, one for SSI and one for MSI devices. In addition, it includes over 100 connection diagrams and test waveforms to help speed the design-in cycle.

All in all, it's probably the most comprehensive collection of practical information ever assembled on such a broad line of practical components.

And it's available hot off the presses for only $9.00.* Simply check box 092 on the coupon below.

*U.S. price only



How to speak fluent Quality.

Get National's free glossary of quality and reliability terms.

Q & R people have to stay ahead of the game. Their job is to intercept glitches that occur on the world's smallest and most sophisticated maze—the chip. Quality and Reliability has become one of the most complex fields in semiconductor manufacturing.

As a result, Q & R people have evolved a language that mirrors the unique complexities of their technology. It's a high tech hybrid language that doesn't appear everywhere and certainly doesn't appear to be getting simpler.

So National has published a new glossary of quality and reliability terms. It's a handy, quick reference source that covers the latest jargon of the industry's watchdogs. A helpful tool for daily use, the glossary is a valuable addition to any electronics library.

Best yet, it's free from National. Just check box 091 on the coupon below.

What's new from the National Archives?

- 025 ☐ PAL Brochure and Data Sheet
- 051 ☐ Data Conversion/ Acquisition Data Book ($7.00)
- 052 ☐ Data Update— Latest new product information
- 053 ☐ Linear Data Book ($9.00)
- 061 ☐ CMOS Data Book ($6.00)
- 062 ☐ Reliability Handbook ($12.50)
- 064 ☐ P²CMOS Memory Data Sheets
- 078 ☐ LF411/412 Data Sheets
- 080 ☐ LH0101 Op Amp Data Sheets
- 085 ☐ PALASM and STARPLEX Information
- 086 ☐ BLX-9252 Data Sheet
- 088 ☐ BLX Expansion Module Information
- 091 ☐ Glossary of Quality and Reliability Terms
- 092 ☐ Logic Data Book ($9.00)
- 096 ☐ Bipolar Prom Update
- 097 ☐ Pressure Transducer Booklet

For desired information, mail coupon to:

National Semiconductor Corporation
2900 Semiconductor Drive
Mail Stop 16251
Santa Clara, CA 95051

In Europe, mail coupon to:

National Semiconductor GmbH
Industriestrasse 10
D-8080 Fürstenfeldbruck
West Germany

Enclose check or money order based upon appropriate currency. Make checks payable to National Semiconductor. All prices shown are U.S. prices only. Add applicable state and local sales tax to your order. Allow 4-6 weeks for delivery. This coupon expires on September 30, 1981.

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National Semiconductor
The Practical Wizards of Silicon Valley

NA 30

Washington newsletter

Reagan to hear bid to drop AT&T suit

Commerce Secretary Malcolm Baldridge is reportedly ready to pass on to the President a recommendation of a special Cabinet telecommunications task force that the U. S. drop its six-year-old antitrust suit against the American Telephone & Telegraph Co. The task force, formed last month at the suggestion of Edwin Meese III, the President's counselor, and headed by Secretary Baldridge, was unanimous in its recommendation, according to sources, although officials decline public comment. The recommendation—to the dismay of AT&T competitors and the Justice Department's Antitrust division, which must complete its prosecution in Washington by June 30—**is reportedly based on uncertainty being created in the capital market by the possible breakup of AT&T into separate entities** for regulated telephone service and for unregulated information-processing markets. Leaving AT&T whole, operating in new markets through a fully separated subsidiary, as now proposed in Senate bill S.898, is favored by Secretary Baldridge [*Electronics,* June 16, p. 58] and by Defense Secretary Caspar W. Weinberger, who sees a breakup hurting military telecommunications.

MCI wins first contract with an independent

MCI Communications Corp., a Washington, D. C.–based rival of the Bell System, says it has contracted with its first independent telephone company—a small one in Iowa—for long-distance service and expects other independents to follow. In a one-year test beginning Aug. 1 **the Iowa customers will be able to choose the routing of long-distance calls** by dialing 1 plus the number for routing through AT&T Long Lines, or 6 plus the number for MCI routing.

IRS chooses Sperry Univac

The Internal Revenue Service, in one of the largest Federal competitions for commercial computers, has awarded $102.6 million to Sperry Univac, Blue Bell, Pa., for 11 model 1100/82 large mainframes, related hardware, and software to process tax returns. **The losers were Honeywell Inc. and Vion Corp., which bid with computers made by Japan's Hitachi Ltd.** The Sperry Univac systems, using Cobol as the primary language, will replace Control Data Corp. 3500 and Honeywell Information Systems 2050A and 200 computers. The first machine is scheduled for September delivery to the IRS National Computer Center at Martinsburg, W. Va., for use in program development. The other 10 will be installed at IRS regional centers over a 16-month period beginning next March.

Three to share NSF computer grants

Three universities—Wisconsin, Illinois, and Cornell—will share $11.3 million in five-year National Science Foundation grants for experimental computer science research and research facilities. The NSF says the grants **"address concerns about the shortage of computer science Ph.D.s in industry and academia, as well as the deterioration of U. S. facilities"** for data-processing research. The University of Wisconsin's Madison campus will get nearly $4.7 million to develop a 50-node, partitionable multicomputer for matching computer resources with research problems, concentrating on numerical analysis, system architecture, data-base design, and computer languages. The University of Illinois at Urbana will get over $4 million to buy additional equipment to expand research on computer aids. Cornell University, in Ithaca, N. Y., will receive $2.6 million for research on automating programming.

The Pentagon's problems are people

In the never-ending battle to build a better military machine that will work in the chaos of war, the problems facing the U. S.—cost, quality, performance, and a good mix of weapons—are traceable to a single source: the sheer diversity of people.

The hydra-headed multitude confronting the military electronics establishment ranges from the nation's civilian and military leaders, legislators, Government economists, planners, and program managers down to the soldiers, sailors, and airmen who one day, if all else fails, will be required to fight with whatever is at hand. All are individuals with different biases, interests, training, and skills—just like the technologists in the electronics industries.

Breaking old molds

The success or failure of the Reagan Administration's weapons spending buildup depends largely on whether that multitude can cooperate to produce a better fighting force without severely affecting the nation's economic health. It is a sociological problem that will require much change in the attitudes of those involved, says Air Force Maj. Gen. M. Roger Peterson. Nevertheless, Defense Secretary Caspar Weinberger and his deputy, Frank Carlucci, are convinced that it can be done.

Both the House and the Senate are going along with Reagan's program for now, though there are skeptics in Congress. What Capitol Hill staff members find troublesome are the Office of Management and Budget's economic assumptions on declining weapons-system inflation factors. Historically, they have been far higher than inflation in the general economy.

Also among the doubters is Digital Equipment Corp.'s C. Gordon Bell, engineering vice president for the Maynard, Mass., computer maker. Since the Defense Department will aggravate the engineering talent shortage (see p. 24) as the weapons market expands, Bell argues that Japan may overtake the U. S. in the world's nonmilitary markets while the engineering community's attention is on such projects as the Army's Military Computer Family.

Pentagon planners deny that military market expansion will add to the engineering drain by noting that procurement increases are coming largely in systems already designed, requiring increases in production workers rather than engineers. Secondly, they cite a soft market in the electronic components industry. As a result, they believe, that industry will welcome military programs.

The computer family project, Bell contends, "will cost several hundred millions [of dollars] and get us another obsolete, high-cost computer for the military. Tax incentives won't help much except to drive up engineers' salaries and make the commercial economy a higher-cost one than that of the Japanese. Being less competitive will cycle the system down. Who's going to pay for the military equipment we continue to create?"

Calls for change

Even advocates of the Reagan program are calling for changes in the procurement system. Air Force Lt. Gen. James W. Stansberry, new head of the Electronic Systems division at Hanscom Air Force Base, Mass., favors contract awards based on prior performance (see p. 14). George H. Heilmeier, former director of the Defense Advanced Research Projects Agency, concurs, as does Litton Industries Inc.'s Leon Bloom, director of the Van Nuys, Calif., Data Systems division and its Army and Air Force programs.

"In the commercial world you cannot get inside the door if you bomb out and give customers the runaround," says Heilmeier, now vice president of corporate research, development, and engineering at Texas Instruments Inc., Dallas. Yet he notes that in the military business, "the same wonderful people who brought you the first disaster get back in line."

Carlucci is trying to change all that [*Electronics*, May 19, p. 66]. Yet Congress is still waiting for the Pentagon to implement, among other things, its Directive 4155.1. Revised in 1978, it calls for files on contractor-quality history and an automated central data bank for interservice reporting of quality failures by contractors.

A policy, please

With Reagan's new team in office less than six months, getting the contractor-quality reporting system up and running may have to wait awhile. What must precede it is a definitive military policy that says something more than beat the Russians. It must be a policy that defines military missions more clearly than it has in the past so that technological design will be directed by military tactics—reversing the roles that have wrongly prevailed for so long.

Also, it must be a policy that all those involved, advocates and dissenters alike, can comprehend and act on. Without it, much of the enthusiastic support for the Reagan program from the military and much of industry will become just more lip service. **-Ray Connolly**

Sure way to improve power supplies: put in Sprague input filter capacitors.

Get more capacitance per case size, lower ESR, and higher ripple current...566 standard ratings to choose from!

Now you can meet your specific power supply requirements without paying for special input filter capacitors that increase both cost and lead time.

For example, you can get Sprague input capacitors with capacitance values as high as 390,000 µF in a 3″ D. x 8⅝″ L. case. But don't take our word for it. Make a spec check in the table below.

KEY SPECS	TYPE 623D* Extralytic® ALUMINUM ELECTROLYTICS 20 Standard Ratings	TYPE 602DX Extralytic® ALUMINUM ELECTROLYTICS 150 Standard Ratings	TYPE 32DR Compulytic® ALUMINUM ELECTROLYTICS 132 Standard Ratings	TYPE 32DX Compulytic® ALUMINUM ELECTROLYTICS 132 Standard Ratings	TYPE 36DX Powerlytic® ALUMINUM ELECTROLYTICS 132 Standard Ratings
Case Size Range (D. x L.)	1.375″ x 2.125″ to 3.000″ x 5.625″	1.375″ x 2.125″ to 3.000″ x 5.625″	1.375″ x 2.125″ to 3.000″ x 8.625″	1.375″ x 2.125″ to 3.000″ x 8.625″	1.375″ x 2.125″ to 3.000″ x 8.625″
Operating Temperature Range	−55°C to +85°C	−55°C to +85°C	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C
WVDC Range	200 and 250	5 to 250	7.5 to 150	10 to 200	10 to 450
Capacitance Range (µF)	7400 to 260*	270,000 to 150	310,000 to 410	320,000 to 180	390,000 to 80
Max. ESR (ohms) at 120 Hz	7400 µF at 200 WVDC: 0.020	270,000 µF at 5 WVDC: 0.0062	310,000 µF at 7.5 WVDC: 0.010	320,000 µF at 10 WVDC: 0.017	390,000 µF at 10 WVDC: 0.012
Max. RMS Ripple Current (Amperes) at 120 Hz and 85°C	20.0	36.0	23.9	18.3	15.3
Terminal Styles	Low Screw-Insert	Low or High Screw-Insert, or High Current	Low or High Screw-Insert, or Solder Lug	Low or High Screw-Insert, or Solder Lug	Low or High Screw-Insert, or Solder Lug

*Designed specifically for off-line switched-mode power supplies.

4SE-1107

For complete technical data, write for Engineering Bulletins 3461A, 3457B, 3441E and 3431D to Technical Literature Service, Sprague Electric Co., 35 Marshall St., North Adams, Mass. 01247.

THE BROAD-LINE PRODUCER OF ELECTRONIC PARTS

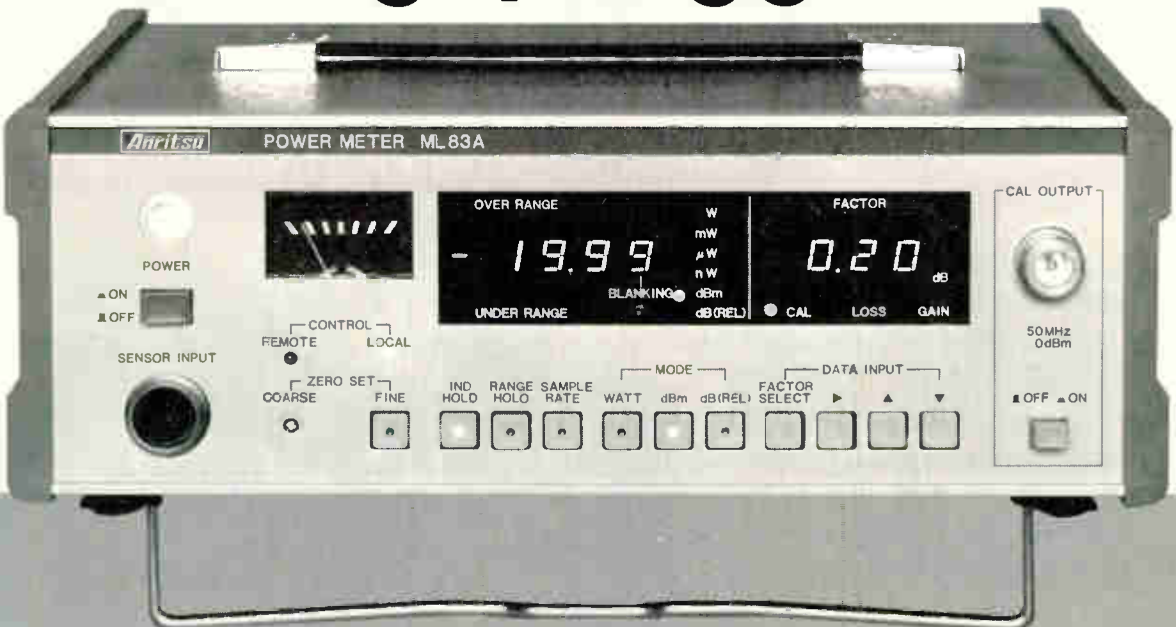
SPRAGUE®
THE MARK OF RELIABILITY

a subsidiary of **GK Technologies** Incorporated

Circle 59 on reader service card

40~140 GHz

That's right, 140 gigahertz!



The ML83A Power Meter from Anritsu

At last there is a meter for making sensitive, precise RF power measurements in the millimeter-wave region with no danger of zero drift or instrument damage. The new ML83A Power Meter from Anritsu offers extremely flat frequency response, accurate digital readout from −20 to +20 dBm, and simple, rugged construction for use in the laboratory or the field.

Such remarkable performance is due in part to the TC-MP series of mounts. These five mounts are quickly interchanged with no special adjustment of the ML83A Power Meter, and together they cover the full 40–140 GHz range flat to within ±6%.

Hermetically sealed within each mount, a unique thin-film thermocouple is used as the power-detecting element. This thermocouple overcomes the problems inherent in bolometer or thermistor elements and invests the ML83A Power Meter with a healthy capacity for RF power (200 mW CW) and almost negligible zero drift.

Other features of the ML83A include a recorder output, a full range of flanges for perfect matching to any waveguide, and, in addition to AC power, an optional battery pack and charger that give the instrument complete portability. The GP-IB (IEEE 488) Interface Bus is also available as an option for remote monitoring or control.

The ML83A Power Meter is another Anritsu instrument that is measuring the limits of technology.

Anritsu

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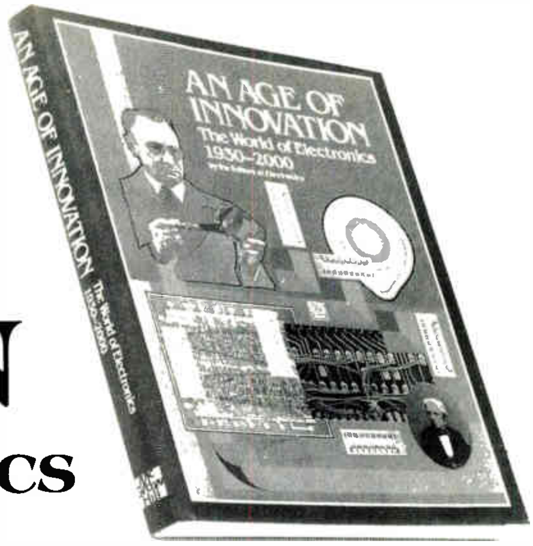

AN AGE OF INNOVATION

The World of Electronics 1930-2000

by the Editors of *Electronics*
274 pages, 300 illustrations including many in full color, hardcover, $18.50

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Painstakingly researched and written, AN AGE OF INNOVATION brings you up close to the discoverers who set the pace for an age . . . the classic circuits that marked turning points in the development of electronic systems . . . and the major breakthroughs that brought us to where we stand today.

Discover our legacy of achievement as you . . .

- witness the 1930s' great advances in fm and television . . . the invention of negative feedback . . . and the patenting of the semiconductor for amplification
- watch the tide of progress as World War II leads to outstanding advances, including radar, loran, computers, and guided missiles. See how at the war's close commercial television, stereo and tape recording mark the beginning of the all-pervasive impact of electronics
- share the 1960s' excitement of men landing on the moon, thanks in part to semiconductors and the expansion of computer power to an unprecedented degree
- acquire new perspective on the 1970s' two major events that will forever change the way we live—the end of cheap energy and the birth of the microcomputer

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EL 1

The Microprocessor's PAL.
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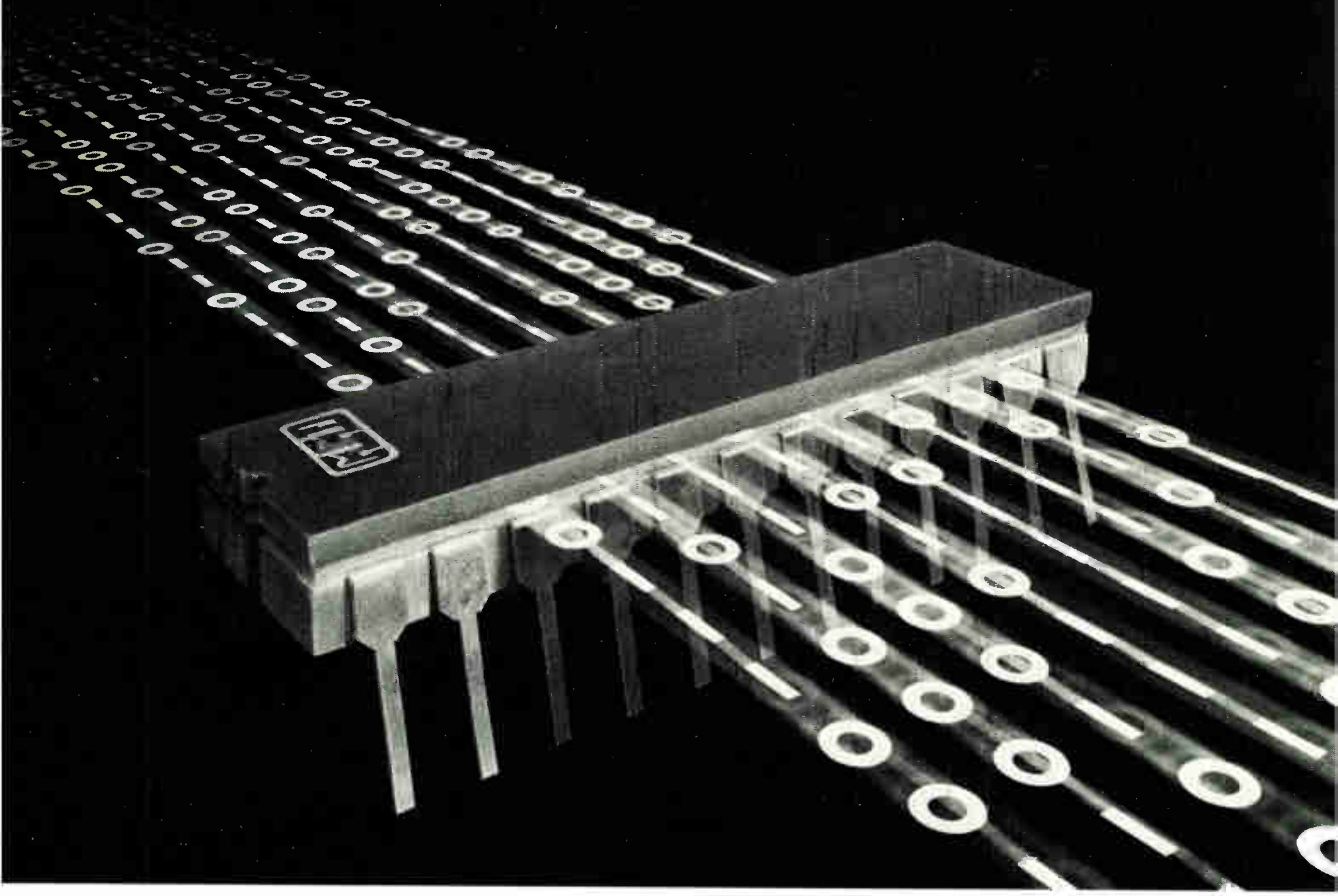

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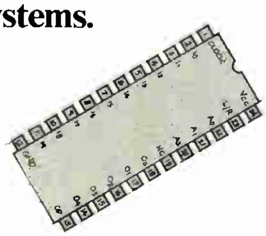

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ELEC 5/30/81 MM15

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Monolithic Memories MMI

Marconi extends sonar range . . .

Sonar technology is about to be transformed by a new piezoelectric transducer comprising **a thin film of polyvinylidene fluorine (PVDF) plastic on which an electrode array can readily be formed.** One of the first companies to capitalize on this highly vibration-sensitive transducer is Marconi Space & Defense Systems Ltd., which has introduced an electronically scanned 360° system with no moving parts for harbor and coastal defense. During trials, divers at distances in excess of 200 meters and more substantial targets out to 1.2 km were detected and displayed on a plan-position indicator similar to that used in a conventional radar. In this system an array of 100 electrodes has its beam electronically shaped and is rotated 8,000 times a second by electronic switching. Marconi has also carried out trials on a shipborne sonar system using the same technology but in addition electronically stabilized.

. . . introduces frequency-hopping radio series

Little more than a month after Racal Electronics Ltd. launched its very high-frequency Jaguar-V frequency-hopping combat radio [*Electronics*, May 19, p. 71], Marconi Space & Defense Systems has come up with its answer to the frequency-agility problem: a range of radios called Scimitar that cover both the hf and vhf bands and include a pocket-sized vhf set of limited range and frequency (68 to 88 MHz) and weighing just 0.5 kg. Apart from spanning both the hf and vhf bands, Marconi's system differs from Racal's in the techniques employed to synchronize transmitter and receiver hops. The Marconi approach allows **a selective call facility that can deny a captured manpack access to the net** and hops over the entire 30-to-88-MHz band that Racal split into nine hop bands. Racal, though, is already delivering products, whereas the first Marconi deliveries will be in the fourth quarter of 1981. In a separate venture, Marconi is a major contractor to the U. S. Sincgars frequency-hopping program.

French defense buying digital gigahertz links

Thomson-CSF of Paris has begun mass production of a new military digital microwave communications link that consumes only 40 to 50 W and thus can run off battery and charger, thermogenerator, photovoltaic generator, or the mains at 48 V dc. Intended for fixed or temporary networks, the line-of-sight TFH 150 operates in the 1.35-to-2.7-GHz band and has **a capacity of 8.5 to 34 Mb/s, enough to carry 120 to 480 channels.** Its frequency agility is set by synthesizer in 1-MHz depth and the receiver's maximum noise factor is 6 dB, though this can be reduced to 3.5 dB by using a low-noise amplifier. The French armed forces expect to have the system in full use by early 1982.

Japanese OCR research benefits U. S. mails

Nippon Electric Co. will supply technology and components for optical-character-recognition sorting machines to be delivered to the U. S. Postal Service by Burroughs Corp. in October 1982. It will be paid about $9 million of the $70.6 million that Burroughs will receive for the initial order for 126 machines. NEC also expects to profit from a follow-on order for 300 machines. **The machines handle 30,000 letters and postcards an hour.** They read the zip code and address, translate them into a bar code that they print with an ink jet, and sort the items by destination into 12 to 60 groups. OCR technology of the type the machines use was developed by both NEC and Toshiba Corp. in research that started in 1968 under contract to Japan's Ministry of Posts and Telecommunications.

International newsletter

UK weighs a UK-only satellite business system

Watch for private industry to set up a national satellite business service serving just the UK. British Aerospace is one of a number of companies to have discussed the possibility of such a joint venture with British Telecom as well as with IBM Corp. and other potential commercial partners. It is **also positioning itself for direct broadcasting by satellite** and has recently formed the Satellite Broadcasting Company Ltd. with banking firm N. M. Rothschild. A Pan-European service, though attractive, would probably be road-blocked by the Continental telecommunications authorities.

Swiss report finds Far East electronics jobs are changing

Despite a slump in the number of jobs for Asian electronics workers, employment in the Japanese electronics industries appears stable, according to a report by the International Metalworkers' Foundation, the Geneva-based coordinating body for trade unions. Citing international trade restrictions, such as quotas on color TV imports, as a principal reason for the slowdown, the foundation points out that most governments in Asia's developing countries are beginning **to change the structure of the industry from labor- to technology-intensive.** Particularly hard-hit is South Korea, where electronics employment fell 13% between 1979 and 1980.

Arab involvement in satellites grows

Kuwait expects to complete the construction of a satellite ground station in 1982, a year before the first Arabsat telecommunications satellite goes into orbit, according to the OPEC news agency. A joint venture by all the Arab countries except Egypt, Arabsat is currently scheduled for launch by the U. S. space shuttle Columbia and **will provide 8,000 telephone lines, 6 television channels, and improved Telex and facsimile services.**

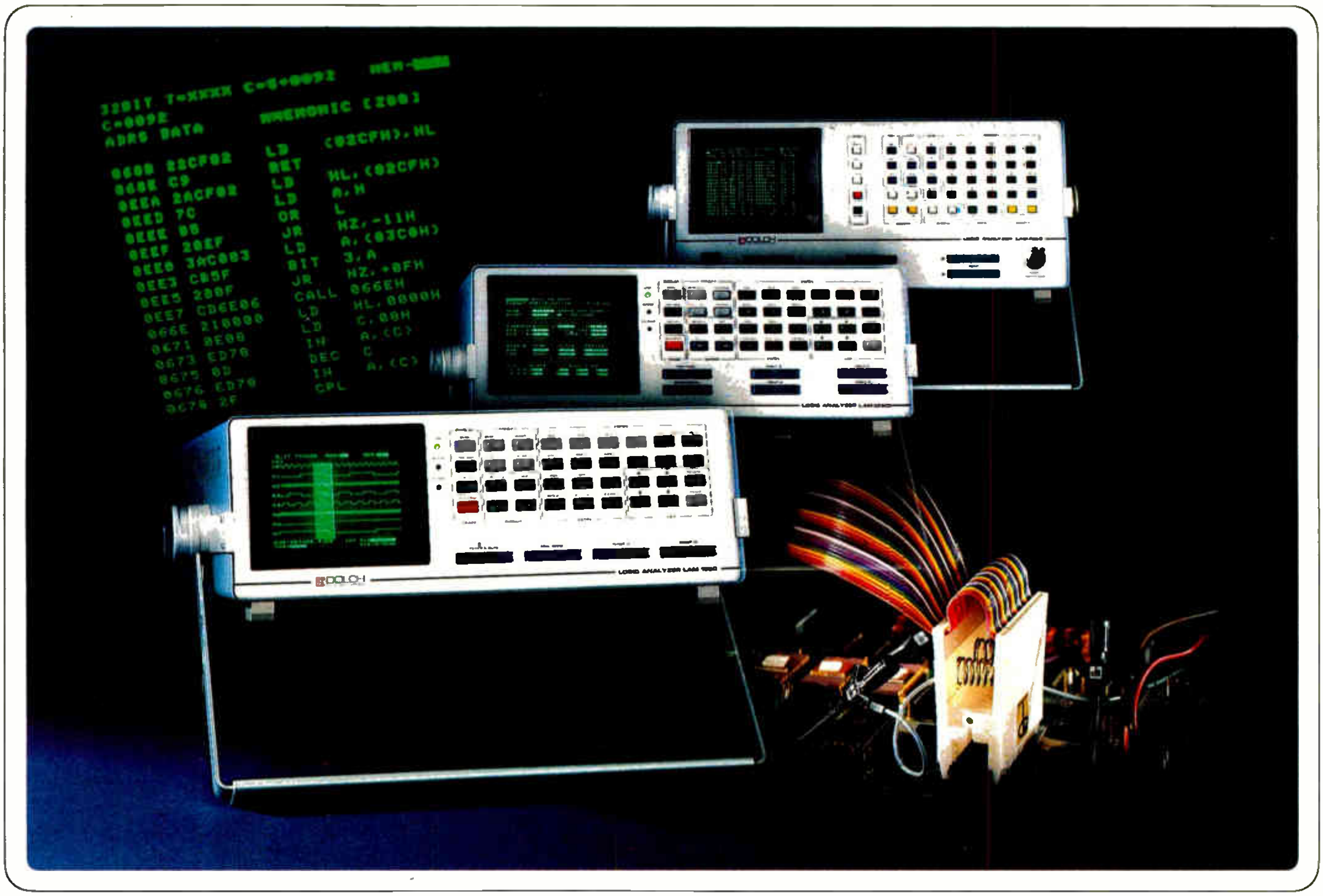
Meanwhile Qatar plans to complete its second ground station by 1983. To be located at Mukeinis, it will enhance the country's telecommunications with Europe and the U. S., for its tower will face satellites orbiting in the Atlantic zone. Qatar's present station links up with the Indian Ocean zone and has 140 of its 960 channels in operation.

ICL aims system at distributed processing market

Britain's troubled computer company, International Computers Ltd., aims to better its prospects by entering the market for small distributed systems, one of the fastest-growing computer sectors, with a high-performance derivative of its popular System Ten. Called System 25, it performs four times better than the present System Ten 220 and **thus at $50,000 and up achieves a 30% price-performance advantage over the competition,** says ICL. More importantly, it adds a powerful communications capability capable of supporting both IBM Corp.'s Systems Network Architecture and the X.25 packet-switching standard.

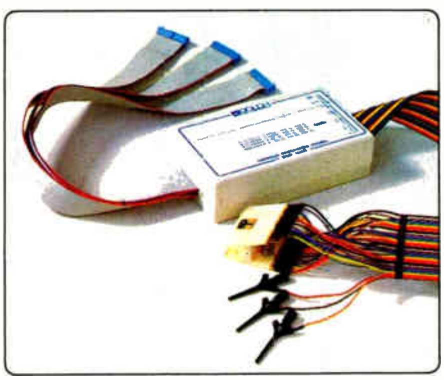
Addenda

Japan's Suwa Seikosha has developed a **low-cost self-contained complementary-MOS speech synthesizer** that provides 6 seconds of speech and 63 words. In lots of 30,000, the SVM9300 will be $4.48 each. . . .Toshiba Corp.'s new Tosbac series 7/70E **enhanced 32-bit megaminicomputer** features three operating systems, plus more storage and higher speed than its predecessor. Intended for control systems, the machines cost from $180,000 up to $4.5 million. . . . Oki Electric Industry Co. says that it is **ready to start selling two kinds of emitter-coupled-logic gate arrays,** two Schottky TTL kinds, and three MOS kinds.



16 TO 96
Channels, the most logical family

Dolch's family of third generation Logic Analyzers lets you meet your trouble-shooting needs now, and expand to meet future needs.



With a new channel expansion probe, Dolch's line of 16, 32 and 48 channel Logic Analyzers can easily be extended by a factor of two.

Disassembling bus activity and displaying the state information in Mnemonic code is the most efficient method of tracing program execution. Dolch proudly provides the industry's widest selection of μP personality probes and disassembly firmware, for both 8 and 16 bit machines, as well as standard bus interfaces (GPIB & RS 232).

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A Battery-Backed Menu Memory is one of Dolch's many unique contributions to the industry. It lets you store up to 6 separate files of display and menu parameters, for up to three months without power. This allows you to recall complete test setups with a single keystroke.

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- 1000 bits of recording and reference memory
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Rockwell. Your

There's more than one way to skin a microprocessor spec. Examples? Rockwell has moved customers targeting at 16s to 8s and others from 8s to 4s to save costs. Just as often customers have been shown how a more powerful device was the better fit for performance reasons.

Fact is, since we make all three families (4s, 8s and 16s) we can truly optimize cost/performance tradeoffs. All because we think systems not devices.

When you need systems solutions, call Rockwell.

The Rockwell 4s

This single-chip microcomputer family is so efficient, it's more akin to 8s than other 4s. Ninety percent of PPS 4/1 instructions are executed in a single byte. That makes PPS 4/1 memory and control operations a quick fit for microcontrollers where there's a man/machine interface: appliances, thermostats, telephones, sequencer timers and more.

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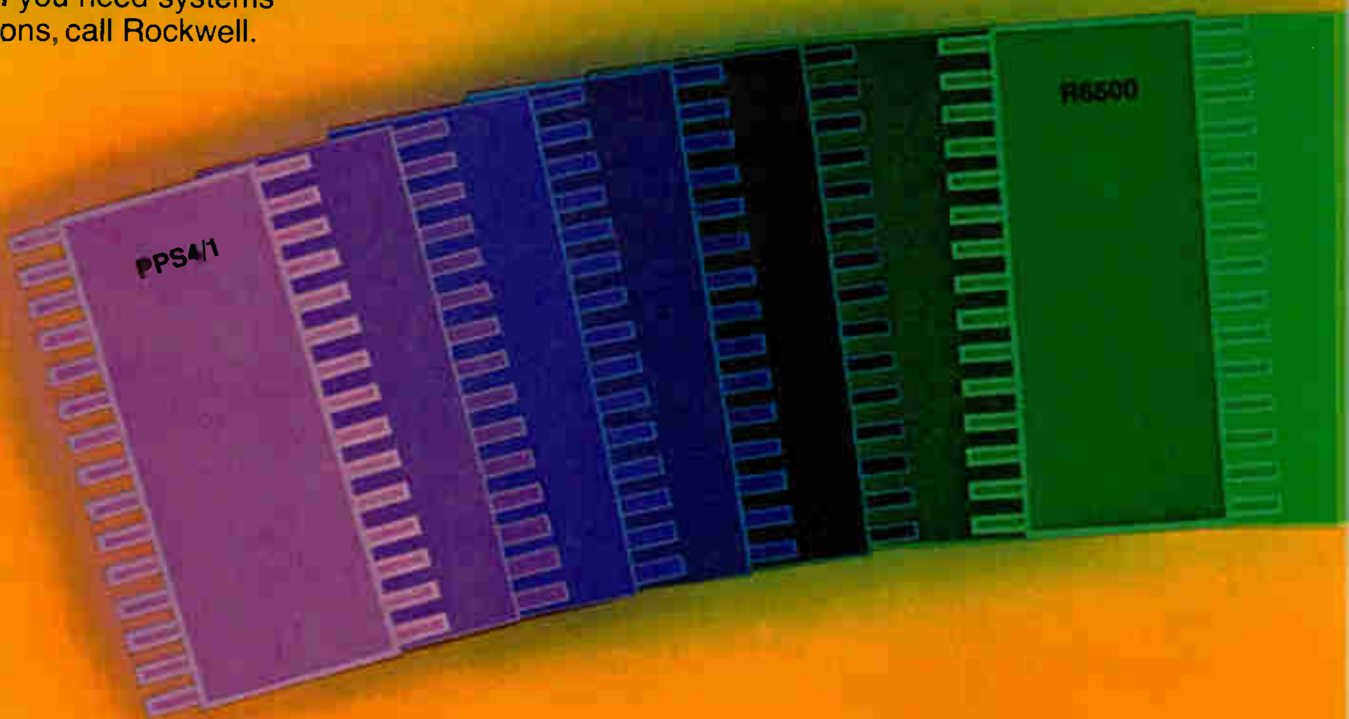
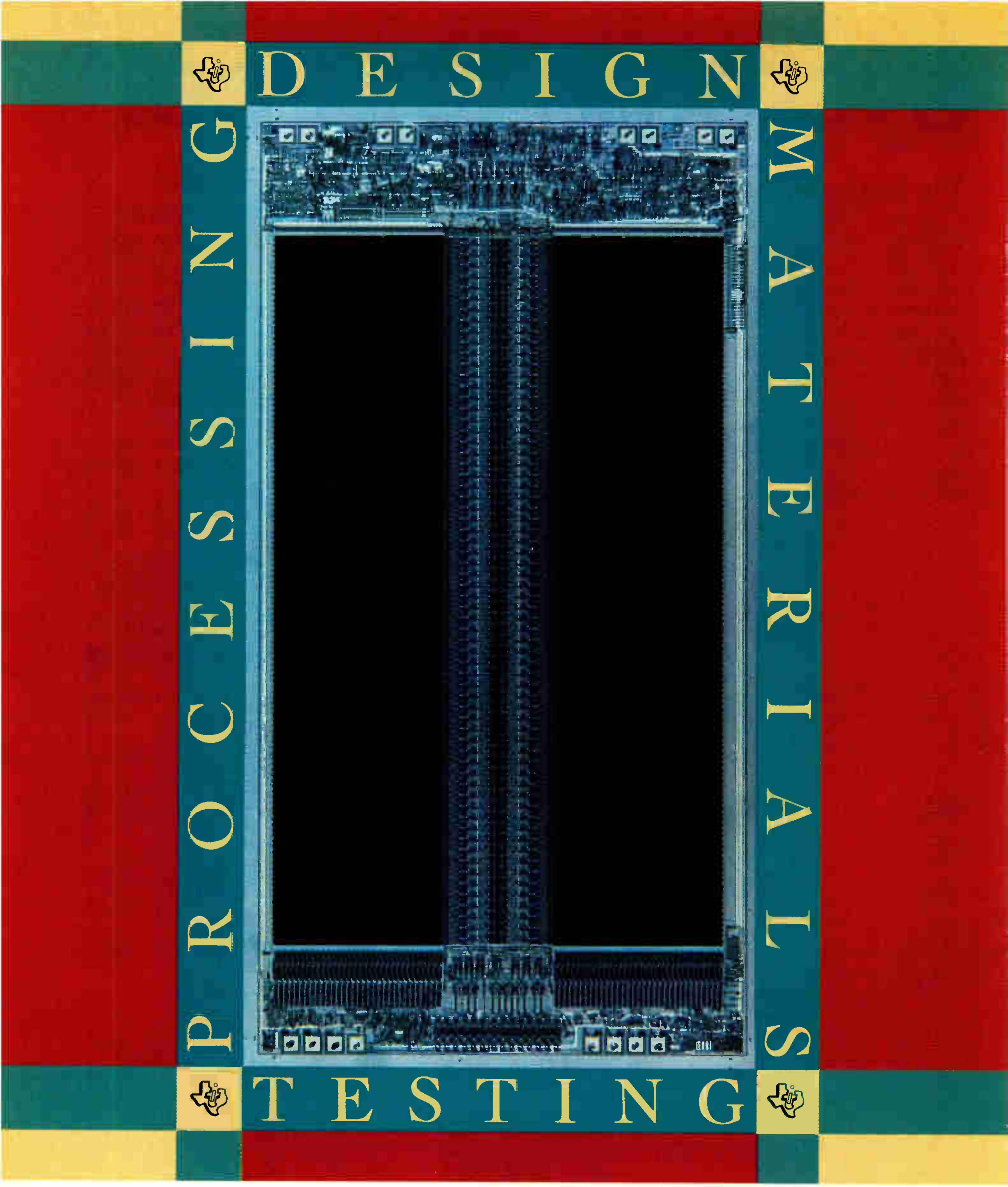
R6500 microprocessors, support devices and R6500/1 single-chip microcomputers are the throughput champions. Most instructions execute in as little as 1 microsecond. Which should you use in your high throughput application? Rockwell will help you optimize a multi-chip R6500 system or put together a single chip R6500/1 design. They use the same software so you can't lose.



PPS 4/1 R6



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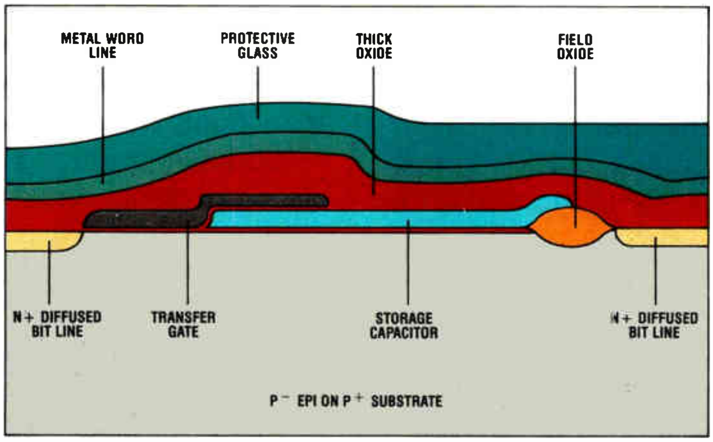
TMS4164 from Texas Instruments. Advancing the systems approach to 64K technology.



Fabricating the TMS4164 cell on epitaxial silicon virtually eliminates substrate noise.

Using diverse resources and production-proven experience, TI developed a 64K dynamic RAM supported by a broad base of technical innovations — at all levels.

There's a systems approach to the advancement of 64K technology that assures our customers that TMS4164 is superior in design — and equally superior in the use of materials, processing and testing techniques.

Because improvements in one technology drive improvements in all the others, it's the shared learning experience between all TI semiconductor technologies that has brought TMS4164 to the leading edge of the state-of-the-art — and beyond.

Design

Our unique grounded substrate design totally eliminates the need for a substrate bias generator — and its less effective method of establishing a negative voltage to control injected electrons. Enhanced noise immunity, greater tolerance to negative undershoot, wider operating margins and firmer transistor parameters are just a few of the breakthroughs TI has achieved with the grounded substrate technology.

Of course, there's much more to the design story, too — like our advanced 256-cycle, 4-ms refresh architecture, low-power dissipation and fast cycle time.

Materials

Innovations are also incorporated into TI's use of materials. By depositing a thin, closely controlled layer of highly resistive P^- silicon onto a low resistivity P^+ substrate, we have virtually eliminated peripheral noise in the TMS4164.

The low resistivity substrate damps out capacitive coupling typically caused by clock bus line activation. Other benefits of this epitaxial (epi) layer are reduced algorithm sensitivity and immunity to address voltage bump. And, epi sets the stage for the future — the not-too-distant future of 256K devices — and the challenge of VLSI.

Processing

Processing advances in TI's TMS4164 mark major technology turns in high-performance DRAM production. TI has unequalled experience in the development of key equipment, like our own dry plasma reactors, and use of advanced low-temperature processing techniques. Our processing capability means device consistency, uniformity and reliability. And satisfied customers.

Testing

For consistently superior system performance, every 64K DRAM is tested well beyond device specification. TI's meticulous attention to equipment accuracy and exhaustive algorithm testing result in high incoming quality. And, our own Test Data Management (TDM) system uses TI's 990 minicomputer to statistically track transistor parameters and other performance characteristics for constant process improvement.

Thanks to this kind of real-time process feedback, TI can assure every TMS4164 user of a more uniform product — and, built-in quality.

For the inside story on TI's TMS4164 64K dynamic RAM, and our leading edge systems approach, call your nearest TI field sales office, or write to Texas Instruments Incorporated, P.O. Box 1443, M/S 6955, Houston, Texas 77001.

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Circle 69 on reader service card

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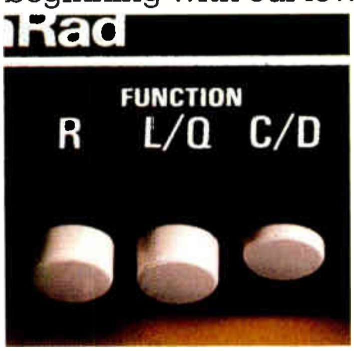

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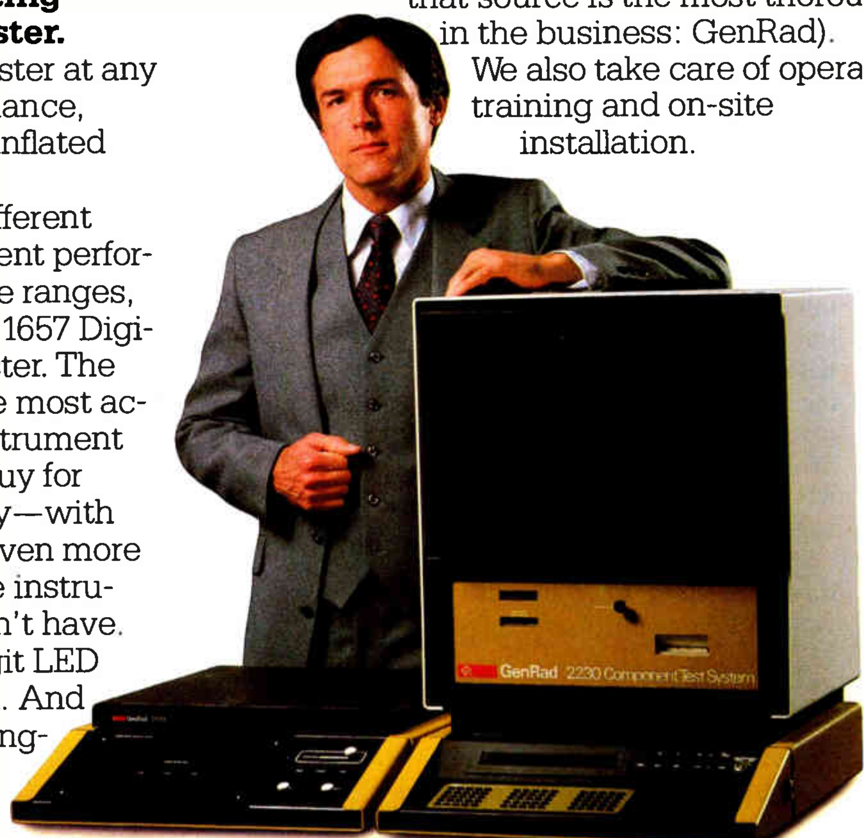
Testing RLC networks and small PC boards: our 2230 will get you on-line weeks sooner.

If you want to test packaged RLC networks, sequenced parts on reels, or even components on small PC boards, you have two choices: You can either do it with our 2230, or you can do it with a rack-and-stac system costing twice as much and lacking the necessary software. Of course, our 2230 will get you up and testing weeks sooner than a setup of unmatched units. And our 2230 is a complete system. Which means needs service from only one source. (And that source is the most thorou in the business: GenRad). We also take care of opera training and on-site installation.

Plain-language keyboard speeds up programming



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We pioneered automatic benchtop testing over a decade ago. And today more people own GenRad benchtop testers than any other brand.

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Our productive 1731 linear IC tester. It offers something nobody else can: immediate productivity. Thanks to a large and proven program library, covering over 1,000 different devices. The 1731 also has a built-in CRT and convenient and quick plug-in family boards for data convertors, voltage regulators and comparators, plus interfaces for all major handlers. Now you can understand why more people own a 1731 than any other low cost linear IC tester.

Displays pass/fail or complete parametric results

Our versatile 1732 digital test system. Not surprisingly, last year more engineers bought our 1732 than any other microprocessor-based digital IC tester. One good reason? Because the 1732 can test SSI, MSI and LSI devices, up to 48 pins. A lot of engineers figure that's an insurance policy for the future. And they're right. In addition no other system is quite so easy to program or to use as the 1732, which lowers your operating costs. But then nobody understands test system software as well as we do.

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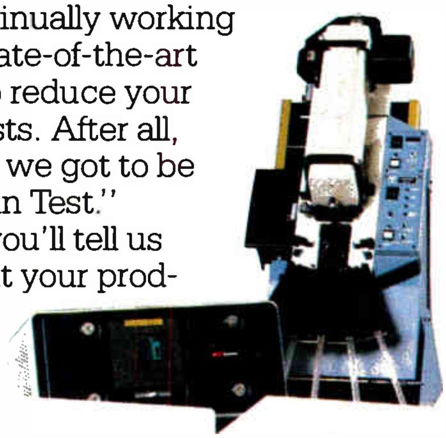


1731 Linear IC System and 1732 Digital IC System

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Circle 71 on reader service card

Modified SEM depicts operation of dense chips

by Kevin Smith, London bureau manager

Fixture turns electron beam of scanning electron microscope into probe that samples VLSI voltage waveforms

Long used to reveal the existence of pin holes, track fractures, and a host of other physical defects in chip surfaces, scanning electron microscopes are now being adapted to studying the operation of very large-scale integrated circuits at speeds of up to 150 megahertz. At the forefront of this embryonic market is a small company in Cambridge, England.

Lintech Instruments Ltd. has developed an attachment that adapts most of the industry's generally used SEMs to this use either during IC development or for field failure analysis. Other research groups, among them Siemens of West Germany, are on the same track. But according to Lintech's managing director, Graham Plows, few of their units are commercially available or can "offer an equivalent combination of usability, flexibility, and performance."

Creditworthy. Plows should know. He wrote what was probably the first paper to appear in the literature on the subject [*Electronics*, July 8, 1968, p. 221]. Moreover, his company has already sold three systems, one each to British Telecom, to the equivalent Italian research organization (CSELT), and to Mostek Corp. in the U. S., and still other companies are interested.

The reason for this interest is obvious. The monolithic circuits with upwards of 100,000 transistors now in view pose a horrendous testing problem, for it is impossible to access their every logic node through their 64 or so output pins. But by powering up a packaged chip with the lid removed in the scanning electron microscope, the half-micrometer-diameter electron beam can be used much like a sampling oscilloscope probe to pick off voltage waveforms from any node on the microcircuit's surface.

The technique is accurate and fast. Unlike metallic probes, an electron beam can be easily and quickly moved, its capacitance is vanishingly small, and it is not destructive of the metallic node. Its only drawback is the risk that some of its high-energy electrons might become trapped in surface-operated devices such as MOS transistors.

However, the Lintech system guards against that by restricting the beam voltage to 2.5 kilovolts. "We can handle repetition rates of 2 kilohertz to 150 megahertz, while the shortest event we can resolve is half a nanosecond," says Plows. The sampling scanner can operate over a voltage range of −11 to +11 volts with a nonlinearity over the entire range of less than 2%—a performance specification that makes the system suitable for probing analog as well as digital circuits.

Series of stills. The sampling fitment operates much like a stroboscopic flash that can freeze the motion of a rotating shaft by triggering at the same point in every revolution. In the same way, a voltage micrograph of the entire chip surface

Turning a scanner into a sampler

The changes that Lintech Instruments makes to a scanning electron microscope to equip it for sampling operation are readily accomplished. There is a rack of external beam-pulsing circuitry and control equipment—a computer-controlled version is under development—and there is a modification to the SEM column and chamber wherein resides much of Lintech's know-how.

In a conventional SEM, fluctuations in the secondary electron emission current—generated by primary beam impact—are amplified and used to modulate the brightness of a raster-scanning CRT display sweeping in synchronism with the SEM's high-energy electron beam, thereby providing the image contrast needed to make the chip or wafer surface visible. Such fluctuations vary with both the surface topography and the material, be it gold, ceramic, silicon dioxide, or aluminum. If any part of the surface is already at a voltage potential, it will also add to the energy of the secondary electron beam. The trick in a sampling SEM system is to filter out these higher-energy electrons.

Lintech's energy filter employs an annular electrode system similar in function to a valve grid, plus a scintillator array and a fiber-optic connector to an external photomultiplier. The grid potential is controlled by the secondary electron current in a closed-loop system and the collector is isotropic in operation. In some microscopes, it can be fitted into the neck of the existing electron-beam column, but for Jeol machines the company provides a new column section. **-K. S.**

can be created by pulsing the scanning electron beam in synchronism with the circuit clock.

When the sample is repeated during each period at the same phase but a different location, successive momentary images are integrated to show the state of the system at the sampling phase.

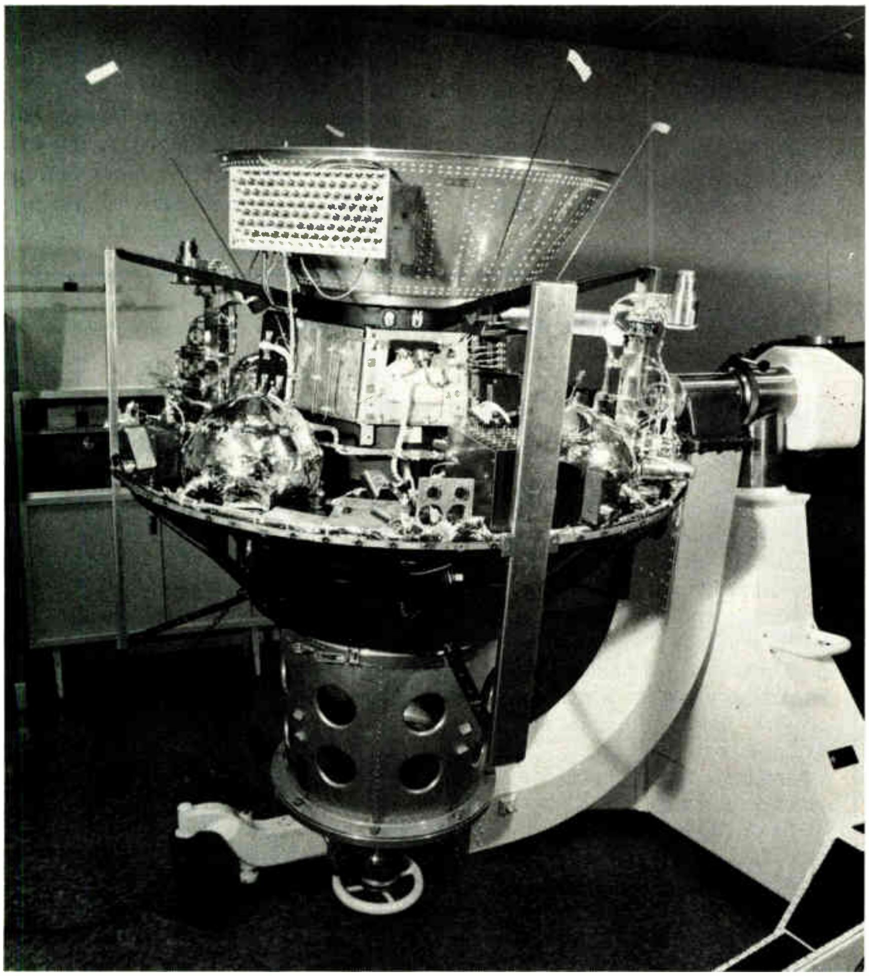
In this imaging mode, the sampling phase is fixed but the electron beam scans the entire chip surface. In the probe mode the electron beam is locked to one spot, and the clock cycle phase used to trigger the electron beam is incremented over a succession of pulses so as to build a picture of a continous voltage waveform over an entire clock period that can be presented on a cathode-ray-tube display.

The next development, says Plows, is to incorporate a full computer control system so that the electron beam can be steered automatically to any desired address.

France

Laser link with Sirio-2 satellite will synchronize atomic clocks worldwide

It would have made Michelson and Morley very envious, this project involving lasers and satellites. To be conducted over a period of two years, the experiment will synchronize atomic clocks in Europe, India, and North and South America to within 1 nanosecond.



Twinkle, twinkle. Using a panel of 98 corner cubes (upper left), the Sirio-2 spacecraft will reflect back laser beams from earth, later transmitting data on their arrival times.

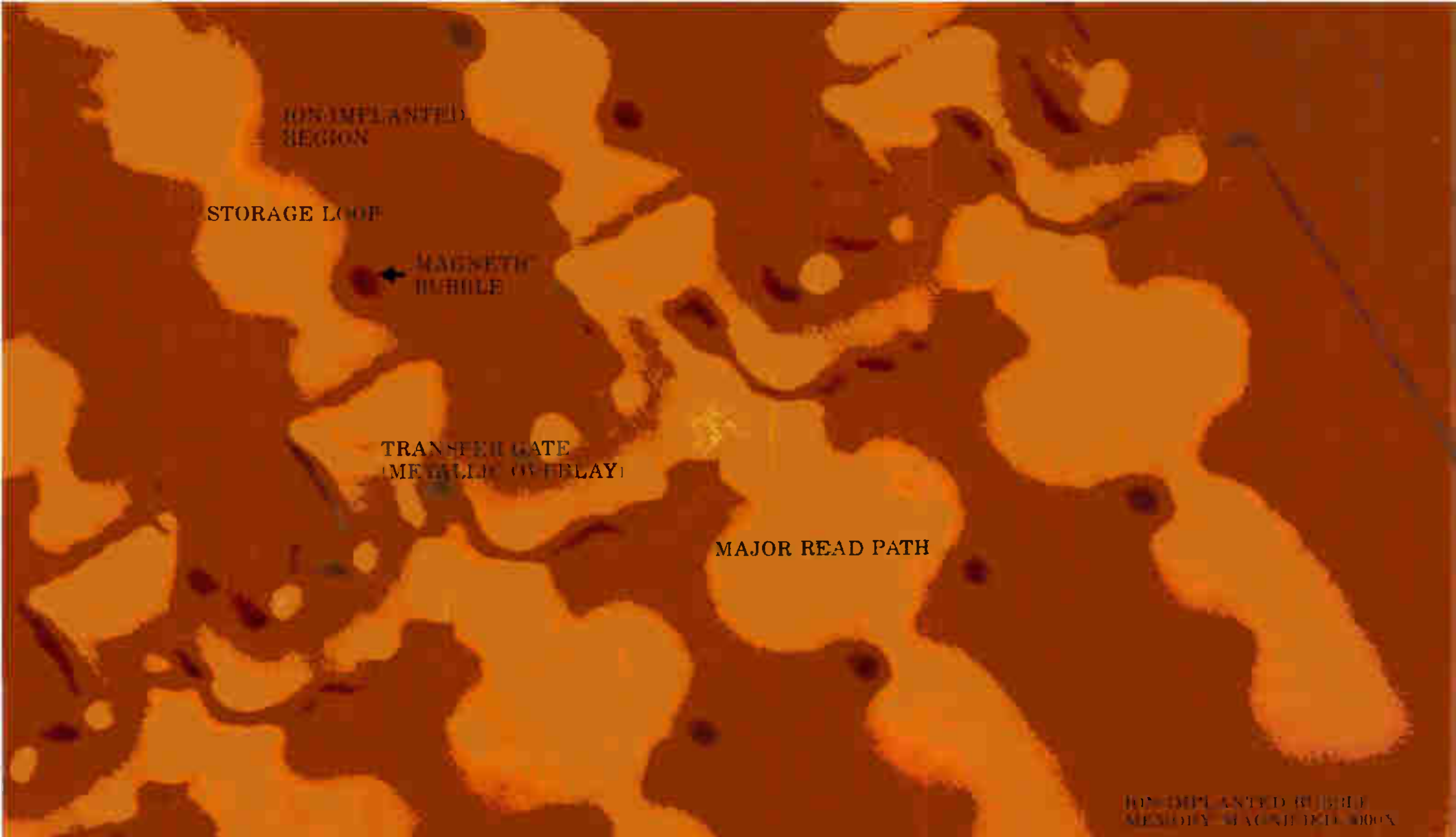
When planning its fifth Ariane launch for February 1982, the European Space Agency offered to include in its program any valid proposals for free. As a result, the Sirio-2 meteorological satellite will carry with it into the sky the hardware for Lasso (for laser synchronization from stationary orbit).

"At the moment, nanosecond timing precision is necessary only for scientific experiments," explains Siegfried Hieber, who is coordinating the project for the ESA. "But it won't be very long before we need such precision for international telephone and digital communications, earth-based navigation, and deep-space navigation. The answer is a repeatable, near–real-time method of long-distance synchronization with subnanosecond accuracy."

The theory behind the Lasso experiment is simple, involving the measurement of the time necessary for laser pulses from two stations on different continents to reach the satellite and be reflected back to their respective stations. It is being tried for the first time now because only recently has the hardware that would make it feasible attained sufficient accuracy.

Up and down. The experiment works thus: lasers of the kind used by astronomers send short pulses from ground stations A and B toward the satellite. Their times of departure, T_A and T_B, are recorded in the respective time scales of the stations' clocks. The pulses are reflected back to the stations by the retroreflectors on the satellite, allowing the measurement of the travel times from the station to the satellite, τ_A and τ_B. Meanwhile, on board the satellite the times of arrival of the pulses are recorded by an event timer and subsequently transmitted to the ground by telemetry to give a time interval, R.

The measurement of these five variables permits the calculation of the shift of time scales between the



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We're also studying how to manipulate bubbles by means of two wafer-thin conducting sheets instead of a pair of external coils.

With this technique, we'll be able to cut the overall size of bubble devices by a third, move the bubbles 10 times faster, and also put far more bubbles on a chip than in today's commercial devices.

A group of Bell Labs scientists and engineers working on magnetic bubble technology holds over 150 patents in the field. About half of them have been awarded to Andrew H. Bobeck, a co-holder of the basic patent for the 1966 invention. Among our inventions:

- Magnetic bubble concepts and devices
- Garnet materials for bubble devices
- Method of growing epitaxial garnet films from a supercooled solution
- Basic technology for device manufacture
- Ion implant method of propagating bubbles
- Dual-conductor sheet method of propagating bubbles

In the Bell System, bubble memories are already at work in equipment that provides recorded voice announcements and in systems that administer and test digital networks. Eventually, the memories could be used in electronic switching systems, and in advanced home and business telephones.

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atomic clocks at stations A and B respectively, using the formula: $C = T_A - T_B + \tau_A - \tau_B + R$, where C = the clock correction.

The Lasso payload on the Sirio-2 consists of a panel of retroreflectors, a photodetection unit, and a timing system. The retroreflectors bounce any light pulses that strike them back along exactly the same path over which they arrived.

The photodiode unit has an interference filter bandwidth of 100 angstroms to prevent it registering any stray incidental light as a pulse. It converts incoming laser pulses for both wavelengths, ruby and neodymium, into electrical signals and transfers them to the timing system.

Refined. The timing system consists of a threshold-detection triggering device, a precise timer, and an ultrastable crystal oscillator that delivers reference pulses about once every 70 nanoseconds. The event timer made by Electronique Marcel Dassault uses the 5-megahertz crystal oscillator with its short-term stability of 2×10^{-11}, plus a clock counter with a resolution smaller than 100 picoseconds. The time tagger encodes the value of the time mark with 42 bits and sends them to a 1-K complementary-MOS memory, whence they are routinely transmitted to the ground via the Sirio-2 housekeeping telemetry system.

The only technical problem is that the satellite is spinning. So each station will have a time gate of about 70 milliseconds in which to hit the satellite and will be told of it by the Sirio-2 command center 15 minutes to an hour before each experiment.

"Initially, we plan to experiment about one hour per day for about two years," Hieber says. "But since the project started it has also expanded. Several people have looked at our plan and said that it is useful for far more than synchronizing atomic clocks. So we expect that the Lasso will also be used for experiments on the theory of relativity and on the effect of gravity on the satellite."

-Robert T. Gallagher

Great Britain

Bubble memory's uniqueness wins continuing commitment from Plessey

The shock waves that accompanied Texas Instruments' departure from the magnetic-bubble memory business may have prompted many to question the long-term prospects of the technology. But the confidence of one European manufacturer of bubble systems, Plessey Microsystems Ltd. in Towcester, Northants., is unshaken. Its biggest concern, says memory and processor product director Ian Chapple, is finding the investment to fund likely production in two years' time.

Still, Texas Instruments and Plessey view the bubble market from different standpoints. As a major component manufacturer, TI invested in a potential jelly-bean market that never quite arrived: failure to standardize and a lack of support circuits, among other factors, held back the bubble market while semiconductor and disk memory technologies encroached heavily on the bubble's potential areas of application.

In contrast, Plessey invested much less than the U. S. giant in component and systems production, though it has a long history of basic bubble research and for a while produced bubble devices of 64-K capacity. Accordingly, its market focus has narrowed to those areas where bubbles have an undisputed advantage—portable systems, rugged industrial and military applications, and high-security systems such as telecommunications exchanges.

Maturing. Projects in each of these sectors are now maturing. For one, a portable billing machine for meter readers at the South of Scotland Electricity Board [*Electronics*, Sept. 13, 1979, p. 76] is now entering production after successful field trials. Again, the company has completed a first production version of a disk-emulation system that at 0.25 cubic foot is half the size of the system it replaces. This is destined for Project Wavell, a computer-based battlefield surveillance system that may survive the Thatcher defense axe. Also, the company has a first working prototype of an 8-megabit backup store for use in a telecommunications application.

Though Plessey was not affected when Texas Instruments threw in the towel, it was hurt by Rockwell International Corp.'s pull-out. The company had earlier decided to standardize on Rockwell parts when it closed its own bubble component operation. So its consequent design switch to parts dual-sourced by Motorola Inc. (originally the Rockwell second source) and National Semiconductor Corp. (Motorola's second source) has caused a production hiccup in several programs.

The availability of dual-sourced magnetic-bubble parts down to the mask level, believes Plessey, will help the market and incidentally prevent a similar hiccup. The group has also developed internally two support circuits for byte-wide memory systems—a four-channel sense amplifier and a four-channel write-driver circuit—and this capability gives it an edge over makers of standard board products, says Alan Hart, commercial memory product marketing manager.

Off the shelf. The company believes it is this kind of capability that guarantees its position as a supplier of custom boards. In its view, bubble memory interfacing is too complex for most engineers, who would far rather buy complete assemblies than tangle with the problems of planning production around the eccentricities of these parts—for example, the need to use test data in the production process because bubble memories have redundant loops.

Plessey is solving this problem by incorporating the bubble testers it has developed in house into a data network to create a data base through which production will be

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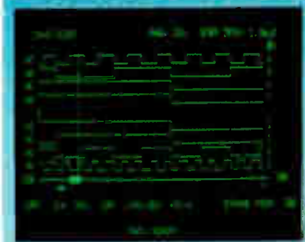

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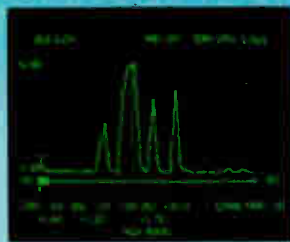

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scheduled. Even so, the firm's price range is not for everyone. To take on a small bubble development for, say, a portable terminal, the company would want to see $0.5 million of business over two years from the original-equipment manufacturer.

Though the bubble memory market may be narrower than once expected, Plessey remains confident of its future. According to military memory product manager Tom Hall, the nearest competitor is the electrically alterable read-only memory, but that is no match for the bubble memory approach, he believes, in price, density, and number of operational cycles. **-Kevin Smith**

France

Computer teaches better with screen

Computer-driven programmed instruction and the classroom have never been particularly compatible. Either each student works at his own terminal, creating more of a laboratory situation, or some students work at terminals while the others wait their turn.

Now the Compagnie de Signaux et d'Entreprises Electriques has combined a new kind of large-format synthetic-image projection screen with some of its already existing computer and audio-visual technology to facilitate teaching technical subjects to classes of 20 or 25.

The SISA, a French acronym for synthetic, adaptable instruction system, is built around the Paris company's CS 2000 computer. The basic hardware also includes a control console for the teacher, up to four student terminals, an industrial video-disk player, and a projection screen 1.3 meters (51 inches) square. The idea is that even students without terminals can easily observe the work being done by watching the video and projection screens.

Even better, the SISA can simultaneously show three aspects of the same problem, points out Jacques Bourron, a CSEE engineer involved in

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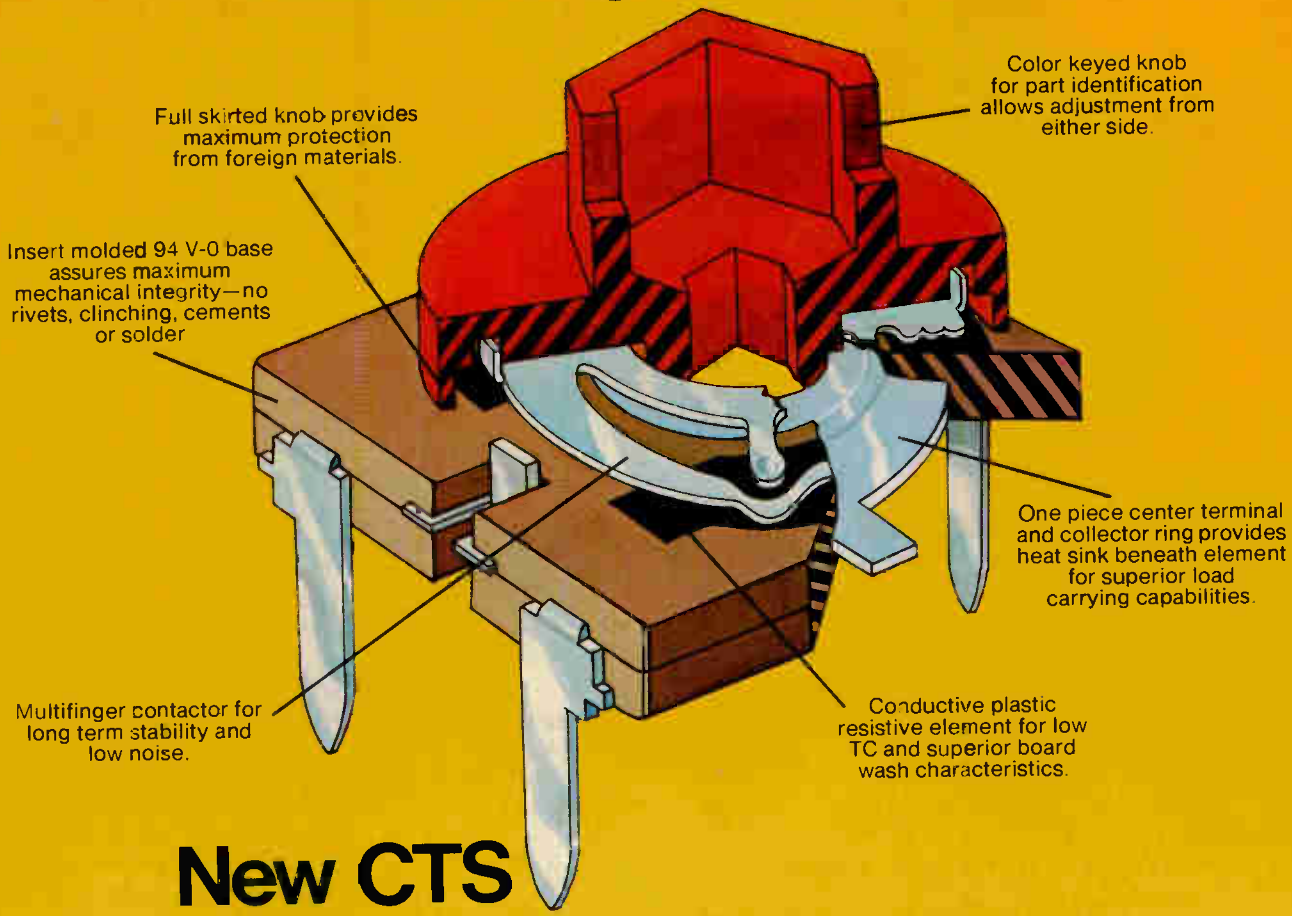

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the project. "A class of mechanics learning about landing gear," he says, "could see a diagram of the system on the projection screen, the control panel of the plane on the student terminal, and actual operational sequences on the video-disk playback monitor."

The innovation that makes SISA possible is the big projection screen. It is based on the system developed by Sony Corp. but, instead of using straightforward video, employs synthetic-image sources that can supply either alphanumeric or dynamic graphic images. For alphanumerics, an allotment of 4-K bytes of read-only memory in the CS 2000 gives a choice of the Roman or Cyrillic alphabets, with the option of 16 Roman character sizes.

Color plus. For graphics, a combination of 32-K bytes of random-access memory and 8-K bytes of ROM is enough for complex moving color images in solid, dotted, or dashed lines. Also possible are rotation and zoom up to 15 magnifications. What's more, the colors can be flashed for emphasis and symbols superimposed. "This computer-controlled screen makes the animated display board obsolete for this kind of application," says Bourron.

The SISA can be used in two operational modes, either completely controlled by the teacher or in a preprogrammed sequence. In the latter case, all equipment is driven by the CS 2000 computer. Based on Zilog Z80 microprocessors, the CS2000 has up to 10-K bytes of memory, can be programmed in Cobol, and accesses any data on its rigid disk in 35 milliseconds.

Originally conceived for military training, the SISA is already being proposed by CSEE as a means of instructing mechanics for the Mirage 2000 fighter, now in the works at Avions Marcel-Dassault-Bréguet. But it should find wide application in the business world as well, despite its hefty $200,000 starting price, Bourron believes. "This is an extremely flexible system," he says. "Once it is in service, it can be adapted to hundreds of uses simply by changing the software." **-Robert T. Gallagher**

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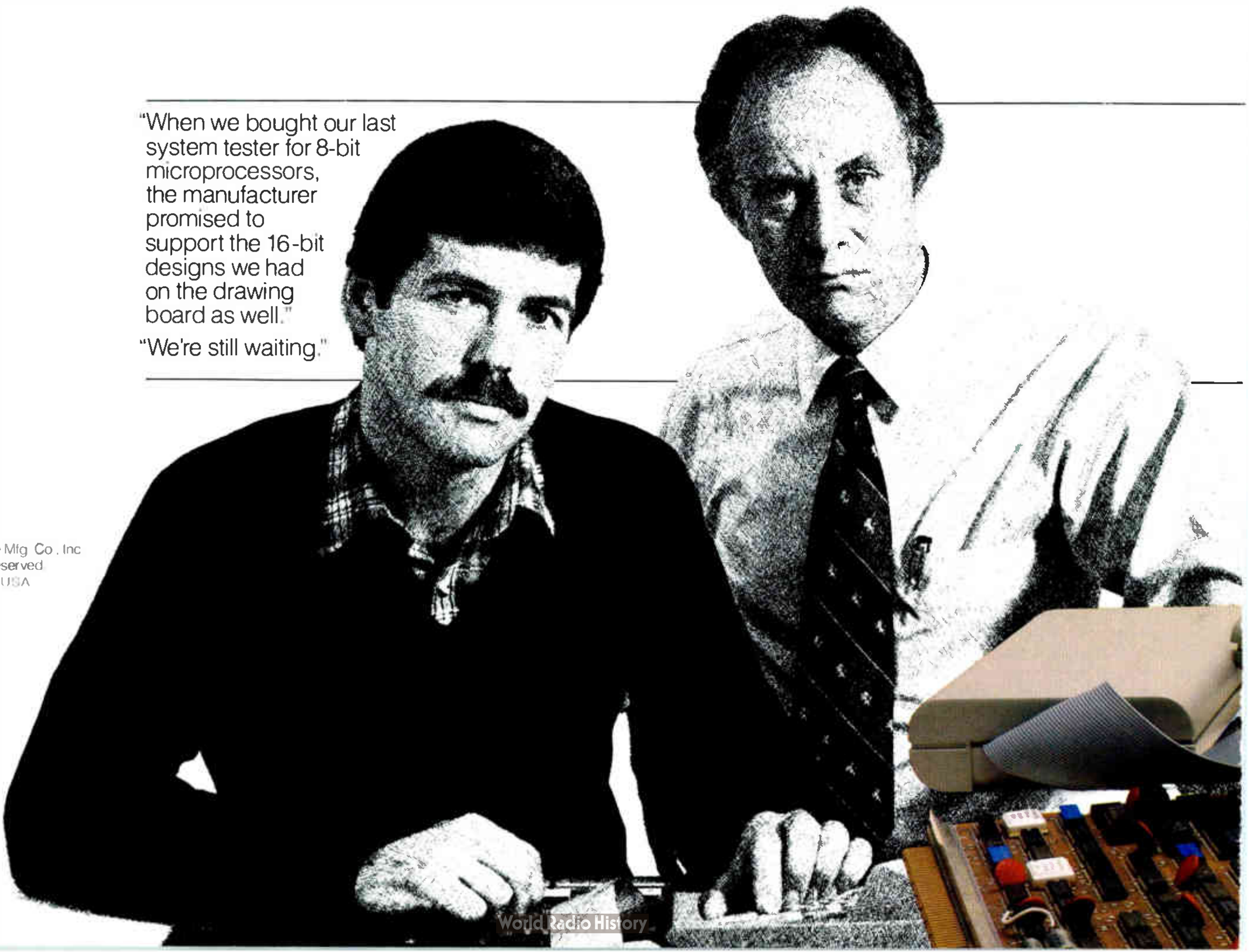

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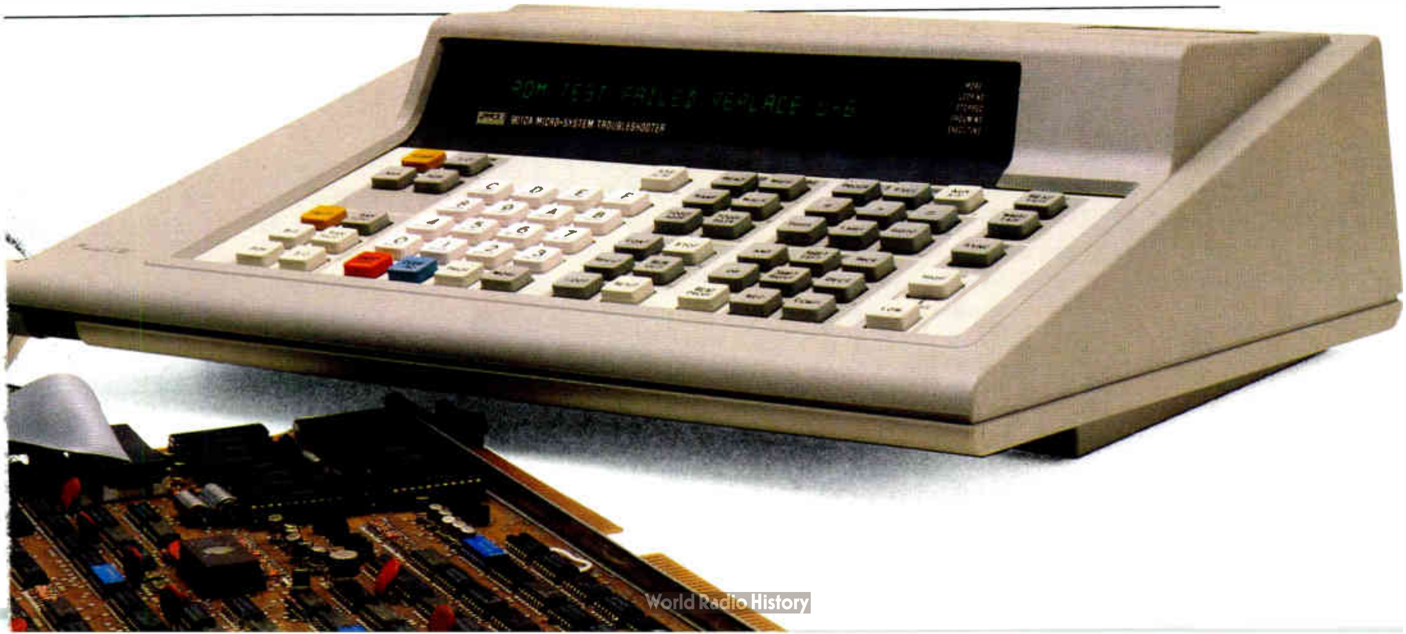


Road to success is labeled 'U. S.'

For West Germany's Dolch Logic Instruments, business plan includes taking on the logic-analyzer heavyweights

by John Gosch, Frankfurt bureau manager

For a small European instrument maker to venture into the tough North American market to battle Hewlett-Packard, Tektronix, and other such giants would seem at first glance to be a trip to frustration. But for West Germany's Dolch Logic Instruments GmbH, a producer of logic analyzers and other microcomputer support equipment, the U. S. move is part of its formula for success.

"If a European company wants to play a role in world markets, it must export to America or build equipment there," says Volker Dolch, head of the five-year-old firm in Dietzenbach, near Frankfurt. About 60% of the worldwide logic analyzer market is in the U. S., he maintains. The country provides the technical stimulus that enables a firm to build high-quality products and compete worldwide. That way, development costs can be recouped, Dolch adds.

His affiliate, Dolch Logic Instruments Inc. in San Jose, Calif., handles the North American market, where it has fared pretty well. U. S. sales jumped from a mere $100,000 in 1978, Dolch's first year of operation in the U. S., to $2.5 million in 1980. The target for this year is more than $6 million, Dolch says.

Currently ranking fifth in U. S. logic-analyzer sales—behind HP, Gould's Biomation division, Tektronix, and Paratronics—Dolch is aiming for more than 10% of the North American market within 18 months. "That will put us in the No. 4 spot ," asserts Curt Burkett, president of the San Jose sales and manufacturing facility. He pegs this year's U. S. market at roughly $70 million.

For the 37-year-old Dolch, the latest *Wunderkind* in West German electronics, success has been a steady companion in his business career. After working with National Semiconductor Corp. in Santa Clara, Calif., in the early 1970s and then as a consulting engineer in Germany for two years, Dolch set up his own company in 1976. Since then, it has grown from a three-person shop to an enterprise employing around 90 people, including 20 engineers and not counting the 40 people in San Jose.

Doubles and triples. Furthermore, DLI's sales in Western Europe have doubled from year to year and even tripled from 1979 to 1980, making it one of the world's fastest-growing manufacturers of test and measurement equipment, according to Dataquest GmbH, the Frankfurt-based affiliate of the Cupertino, Calif., market-research firm. The result is that DLI has 30% of this European market. Non-U. S. sales are predicted to go past the $10 million mark this year.

Dolch puts his company "among the top three in Europe," the other two being HP and Biomation. Other contestants are Philips Gloeilampenfabrieken NV of the Netherlands, Siemens AG of West Germany, and Enertec, a French member of the multinational Schlumberger Group.

High marks for DLI also come from competitors. "It is a dynamic company that knows where it wants to go," says an executive at Philips. Adds an official from a U. S.-based competitor: "Dolch has good ideas. And although some users find the equipment he makes not simple to operate, it is technically sound." It is small wonder that instrument makers in both Europe and the U. S. are casting covetous eyes at DLI in hopes of taking it over. But so far Dolch has turned down all offers.

Key elements. What has helped Dolch on his way up is a keen sense of the market's needs coupled with technical know-how. Starting out as a producer of low-cost logic-analyzer accessories for oscilloscopes, DLI in 1977 came up with its logic monitor, an instrument using a microcomputer for formatting and a special display. "Unlike other companies, we turned from the normal oscilloscope to a display dedicated to logic-analyzer tasks—to a raster-scan display

Ambitious. Volker Dolch wants the West German logic analyzer manufacturer bearing his name to capture more than 10% of the North American market within 18 months.

providing greater brightness and a better price-to-performance ratio," Dolch says.

This was followed in 1979 by the logic analyzer module, a unit combining the analyzer and display in one package. Dolch's key innovation, though, was the creation of the first 48-channel logic analyzer, also born in 1979. "That instrument put us on the map and ahead of others as regards number of channels," he says. "With 16-bit microcomputers appearing on the scene at that time, there was a real need for such high-channel analyzers."

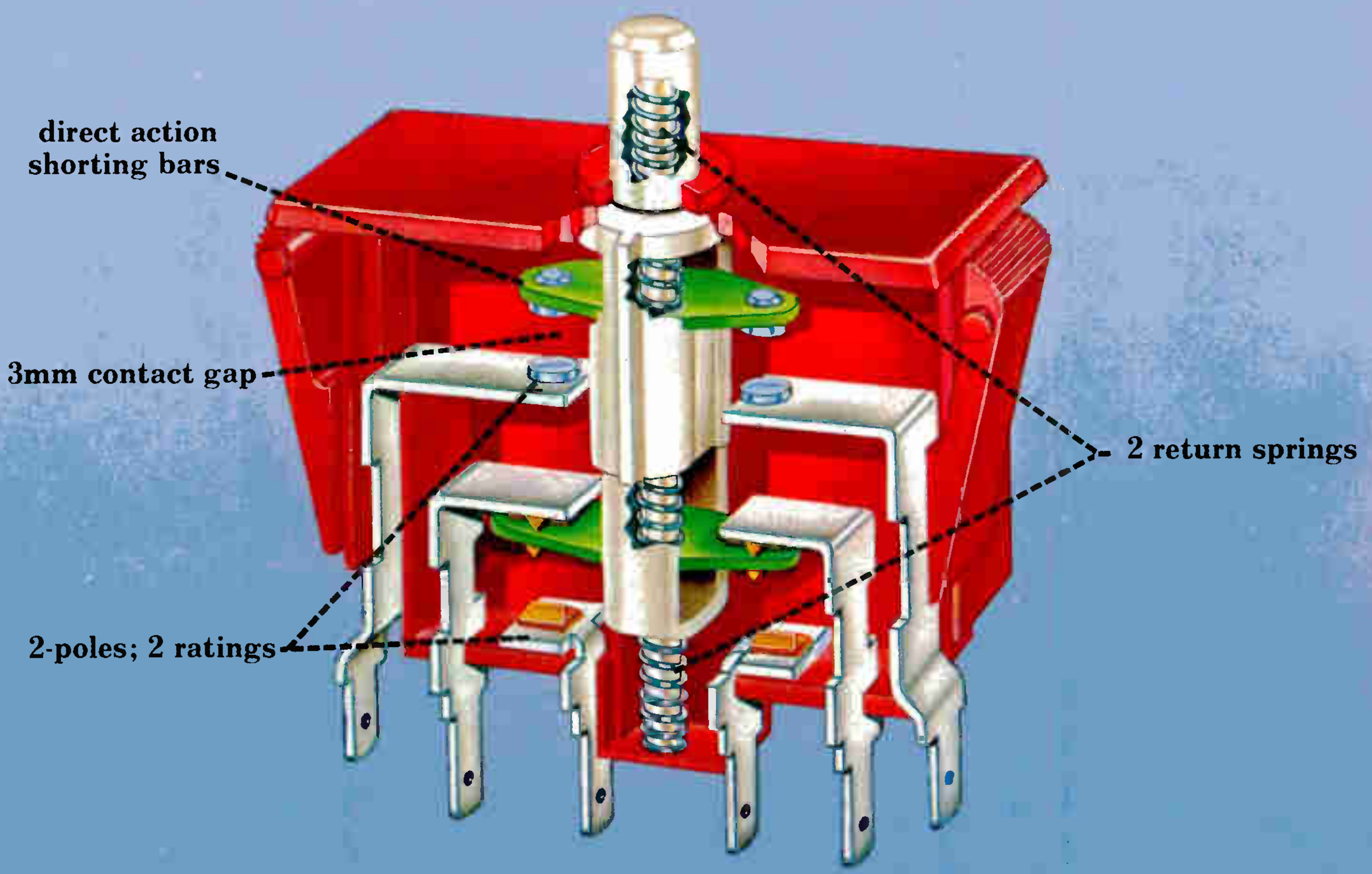
Dolch maintains that the instruments will not go much beyond their present number of channels and speed of 500 megahertz. "Anything higher does not make economic or technical sense," he says. What lies ahead, Dolch points out, are analyzers that can be operated by semiskilled workers, that interface with computers, and that can be used as part of an automatic test system.

No obstacle. With that in mind, can a small company with a single product line continue to be successful? "Yes," Dolch says. "With expenditures for research and development taking more than 15% of our sales revenues, we think we can stay in the forefront of logic analyzer design. What's more, we are in a bustling market." As Burkett of San Jose sees it, worldwide logic analyzer sales will grow by 25% annually—from roughly $115 million this year to $225 million by 1985.

For profitable participation in that market, Dolch considers his company's presence in the U. S. to be a big asset. "Being located in Silicon Valley puts us within easy reach of the high-quality components—custom-designed chips and hybrid devices, for example—that we need."

Yankee touch. Also important is the design expertise DLI is getting from the U. S.-trained engineers at San Jose. "Those people have brought along Silicon Valley know-how and are applying it especially to front-end engineering and to the design of automatic test equipment for in-house use," says the Frankfurt University–trained Dolch. □

LINE-INTERRUPT switch meets latest specs... WORLDWIDE



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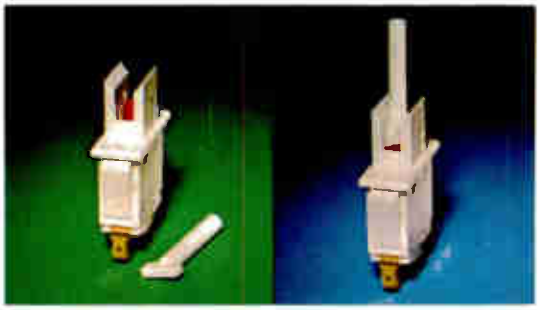

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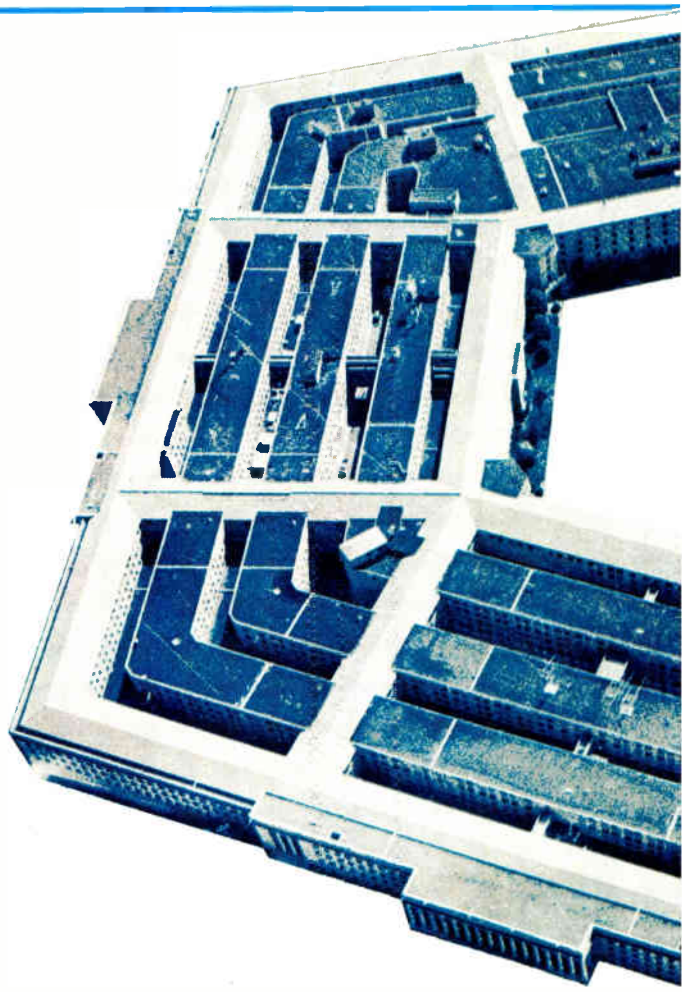


The Pentagon goes shopping for technology

by Ray Connolly, Senior Editor

The biggest U. S. buildup in military electronics capability since the Vietnam War is beginning, just as President Ronald Reagan promised in his 1980 campaign. Designed to counter the Soviet Union's growing military might, the program directed by Secretary of Defense Caspar W. Weinberger calls for accelerated stages during this fiscal year and fiscal 1982, which begins in October. In the four following fiscal years, the projection is that the total Department of Defense budget authority will grow 7% annually after inflation.

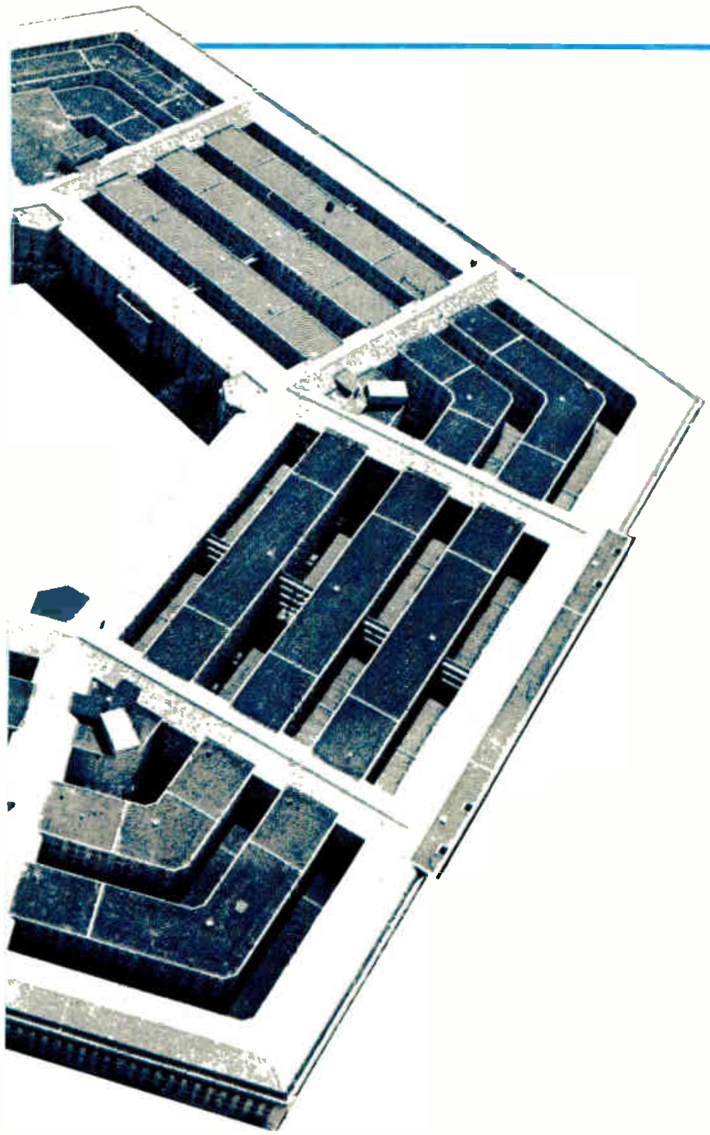
For the five years ending in fiscal 1985, defense spending will total a record $1.27 trillion (see table, p. 90). The U. S. electronics industries' share of that total is expected to be about $190 billion, about 7% more than the $177.5 billion forecast by the Electronic Industries Association last fall [*Electronics*, Oct. 9, 1980, p. 95]. But that excludes a significant area: direct foreign military sales by companies. And they will have greater freedom than in the past, promises James L. Buckley, a former Republican senator from New York who is now under secretary of state for security assistance, science, and technology.

New approaches. The Reagan program will be marked by a number of innovations instituted by Deputy Secretary of Defense Frank C. Carlucci to foster greater Government-industry teamwork, increase production and productivity, and bring the inflation of weapons costs under control. The most significant of these for the electronics industries are:

- The use of "less risky technology" in order to deploy systems sooner in quantity. Carlucci's goal of cutting research, development, and acquisition times in half to less than five years is being heard clearly in military procurement commands. "I suspect it will be much easier to get money for programs that mature in the next few years," says Air Force Lt. Gen. J. W. Stansberry, "than for those with far-term promises." Stansberry recently assumed command of the Electronic Systems division at Hanscom Air Force Base in Massachusetts (see p. 14).
- Upgrading of weapons already in the field with newer high-technology subsystems under an approach called P³I, for preplanned product improvement. Aircraft avionics such as radars and fire-control systems as well as missile guidance and navigation packages are prime applications for the P³I approach.
- Encouraging greater capital investment by contractors by getting congressional approval to extend multiyear contracting to more major systems and by raising the $5 million ceiling on reimbursement to contractors whose program may be canceled.
- Increasing reliability and maintainability by providing contractor profit incentives for meeting objectives that will be set early in a development program.

Management changes. Inside the Pentagon and the services, system program managers are being given a freer hand under Carlucci's new rules. "They will be responsible for anything that goes wrong, too," says one aide. Still under study and thus unresolved is industry's recommendation last year that program management be assigned to civilians who can stay with it from beginning to end [*Electronics*, Feb. 24, p. 104]. However, service officials believe part of that problem may resolve itself if many program development and acquisition cycles can be halved, as Reagan's team proposes.

Among other proposals adopted by the Weinberger-Carlucci team are some long sought by industry. Among them are the reduction of military and contractor administrative costs by eliminating many of the more than 2,000 Pentagon regulations and directives now in



Emphasis shifts to quick results, subsystems to improve existing weapons, eased contractor investment rules, and profit and capital-investment incentives

force and an increase in the degree to which the Pentagon shares in contractors' risks. Another new Carlucci rule is considered idealistic and unworkable, however—it calls for program offices "to budget to most likely expected cost in order to reduce overruns and provide stability" [*Electronics*, May 19, p. 66].

Nevertheless, there is widespread praise within the military, industry, and Congress for the management and procurement initiatives taken thus far. How quickly and how successfully they can be implemented in both the military and industrial sectors is another matter. Carlucci, for example, is known to be concerned about the response of subcontractors, many of whom are electronics suppliers that regularly bemoan their treatment by major prime contractors. He "insists that we must have the full support of industry at every level" if these changes are going to work, says one staff member. "Just as DOD must assure primes that future procurement will be stable, so must primes assure their subs."

Another senior Reagan appointee in the Pentagon believes that positive results of the Carlucci rules changes will have to begin appearing within a year if the confidence of industry and the Congress—which must fund the programs—is to be retained. Considering the magnitude of the changes involved, final success is not foreseen for several years. But, this official fears, "we could lose it all" within a year "unless we can demonstrate that system costs can be controlled, that they will perform as they are supposed to, and convince industry that there is stability in this market. We can do that if industry cooperates."

Showing that the reforms are beginning to take hold within a year is going to be difficult, say most contractors, unless inflation rates decline markedly or the Office of Management and Budget raises the unrealistically low inflation factor set for military procurement [*Electronics*, May 5, p. 64]. Although weapons costs have been escalating at an annual rate of at least 12%—in some cases more than 20%—OMB Director David Stockman has imposed inflation factors on the Defense Department that are even lower than those complained about during the Carter Administration.

The new rates for fiscal 1981 and 1982 have been pegged at 10% and 8.7%, respectively, and then slip steadily downward to 5.5% for 1985 and 1986—years when many programs now in development are scheduled to begin production and increase pressure on the national economy overall. Weinberger and Carlucci, as well as congressional leaders, are pushing the White House hard for more realistic levels.

Progress already seen. At this point, military and industry leaders agree that many problems, like inflation rates, remain, yet they also agree that the team of Weinberger, Carlucci, and Richard D. DeLauer, the new under secretary of defense for research and engineering, are making progress. DeLauer, recruited from the executive ranks of TRW Inc., is charged with implementing 16 of the 23 Carlucci rules for program management. Congress, too, is going along, funding most of the Reagan program requests.

"They are tough and determined people who seem to know where they are going and how to get there," says one senior House Armed Services Committee staff member, who formerly had little praise for military program management. "I don't necessarily buy all the changes they want—it would surrender too many congressional prerogatives—but they do deserve credit so far. They are taking on a system that proved too much for many good men before them over more than a quarter of a century" (see "The Pentagon's three wise men," p. 92).

Meanwhile, profits, personnel, and national policy are the key issues that military electronics system contractors want to hear more about. The first two subjects deal, of course, with the ability of the nation's defense

Inside the news

industrial base to respond to the Reagan program. The policy question being asked is: what are the Reagan program goals?

"Industry needs more guidance on national defense policy than it has got so far in order to make its own long-range plans," explains one military market analyst in Washington. "Beyond the fact that the Administration plans to match the Russians and lean hard on our European allies and Japan to spend more for their own defense, we in the industry still lack a clear definition of U. S. military priorities and their economic impact."

That definition may not come until next fall when the Defense Science Board convenes a meeting of major military prime and subcontractors to assess the Reagan long-term spending projections. By the time that meeting rolls around, the Reagan Pentagon team will be in the final drafting stages of its first original budget—for fiscal 1983, which goes to Congress early next year. Then industry should gain some insight into specific program priorities and their funding in future years. In the meantime, however, there exist what one Senate military budget analyst calls "too many unresolved issues and too many potential conflicts."

For example, decisions are still to be made on what kind and how many new long-range bombers will be bought, as well as on the new MX intercontinental missile and whether it should be based on land or at sea. Also to be determined is the number of divisions the Army will need as well as the number of Trident missile-launching submarines the Navy should have. The Trident decision will also affect Navy spending plans for antisubmarine warfare—a market that depends almost totally on electronic technologies—as well as the proposed doubling of the size of the U. S. fleet.

R&D word. R&D policy decisions to come involve the level of effort on a follow-on bomber using Stealth technologies to overcome enemy countermeasures and on space-based weapons using lasers and charged-particle beam technologies to destroy enemy satellites and ICBMs in flight. Also awaiting a go or no go is a host of tactical weapons replacements and improvements, including infrared imaging and other all-weather and night-fighting systems, where the U. S. believes it is behind the Soviets. "All we can say right now is that it appears the Administration wants to buy nearly everything in sight and in larger numbers," shrugs the Senate analyst. "I confess I'll remain a bit uncertain until there are more firm choices."

Compounding this uncertainty, however temporary, are contractor concerns with low profit rates and the problem of recruiting skilled engineers and technicians in order to match the Reagan buildup. Sperry Univac's Richard L. Seaberg, vice president and general manager of its Defense Systems division in St. Paul, Minn., pinpoints narrowed profitability, rather than a shortage of skilled people, as the primary issue for industry. The reason: continuing high capital costs and interest rates that cannot be charged off under military contracts.

Seaberg complains, for example, that since lead times for delivery of semiconductors have "doubled in the last three years," Sperry has had to carry large inventories at high interest rates for longer periods to meet production schedules on its military computer programs. On four Navy production programs alone—the long-standing AN/UYK-7 and AN/UYK-20 computers, the RD348 magnetic-tape unit, and a data-exchange auxiliary console—Sperry's inventory interest charges last year totaled $7 million, Seaberg says, to carry an inventory averaging $35 million a month. At a minimum, he believes interest expenses should be allowable for capital outlays.

Opportunities abound. Despite the fact that "in today's environment there are more opportunities than you can pursue," Seaberg says that his operation is not planning to increase capital spending because of the high cost of money. The division is running at full tilt with some 8,500 personnel—30% of them engineers and technicians—generating about $400 million in 1980 sales to the U. S. military and its allies in Canada and Germany. That represents a 10% gain on the year before.

The shortage of engineering talent throughout the electronics industries will not hinder the weapons buildup promised by the Reagan White House for the short term, says the Sperry executive, since much of the growth will come in programs already in production that require relatively little engineering effort compared to new products. For the longer term, however, he sees the technical personnel shortages as "a major challenge." Sperry, for one, hopes to meet it with a three-pronged program. First will be the acquisition of existing companies and their work forces, like the recently completed purchase of RCA

FIVE-YEAR PROJECTION OF U.S. MILITARY BUDGETS
(total obligational authority in billions of dollars by fiscal years)

	1981	1982	1983	1984	1985
The Reagan changes . . .					
Current dollars	178.0	222.2	254.8	289.2	326.5
Constant 1982 dollars	193.9	222.2	238.4	255.1	272.9
Annual growth rate (%)	12.4	14.6	7.3	7.0	7.0
Inflation factor (%)	10.0	8.7	7.3	6.2	5.5
. . . from Carter's budget					
Current dollars	171.2	196.4	224.0	253.1	284.3
Constant 1982 dollars	186.5	196.4	206.2	216.5	227.4
Annual growth rate (%)	7.8	5.3	5.0	5.0	5.0
Inflation factor (%)	12.0	10.0	8.5	8.0	7.4

SOURCE: DEPARTMENT OF DEFENSE

Problems for the European allies

While the Reagan Administration, like its predecessors, continues to make headlines by calling for its allies in Western Europe and Japan to pick up a larger share of their own defense burden, there is a more crucial problem facing the North Atlantic Treaty Organization. "It is upgrading and standardizing systems in areas like command and control communications and their computers and software, as well as collaborating in newer areas like electronic warfare," says one senior NATO military man in Washington. "It has been NATO's No. 1 problem since its inception."

U. S. defense officials say that Reagan's Pentagon managers want to change all that by encouraging joint weapons programs by NATO nations' forces, coproduction teaming by American and European companies, and the transfer among them of electronic and other technologies. Yet there is no firm Reagan policy at this point, and U. S. military and corporate officials are reluctant to share their technology leadership for both security and economic reasons. Even though Reagan managers reportedly want to begin rolling back arms export controls and reduce U. S. approval limits on the sale of weapons made in Europe with U. S. technology to the Third World, a real conflict still exists that is expected to involve a Congress concerned with protecting technology transfer and the economic interests of U. S. corporations.

Within NATO's own headquarters in Brussels there is an ongoing concern about upgrading such command and control communications—or C³—projects as the antiquated NATO Integrated Communications System (NICS) and the NATO Air Defense Ground Environment (Nadge) system for strategic communications. There is also the need to set up longer-term efforts, such as the Airborne Command and Control System (ACCS)—which will use the Advanced Warning and Control System (Awacs)—and for advanced electronic warfare.

While electronic warfare efforts are bogged down as the partners try to agree on what the threat will be, the communications programs are strapped for cash. According to NATO observers, members like West Germany, faced with cost overruns on domestic weapons purchases, are unwilling to contribute to the pot of $12.5 billion that NATO says it needs to cover the upgrades through 1984. This funding shortfall will affect not only NICS stage 2 and Nadge upgrades but also plans for new and revamped microwave communications links, ground radars, and the next-generation satellite known as Satcom 4.

Complicating these strategic program difficulties is NATO's failure thus far to get communications interface standards for battlefield tactical communications systems so they can interface with big programs like the NICS 2 upgrade. Again, costs are the stumbling block.

Europeans note that the small size of their domestic military markets precludes the lower prices resulting from such competition as exists in the U. S. Says Gerard Cauvin of France's Thomson-CSF, the country's largest military electronics producer, "There is nearly always a cooperative effort between the government and the supplier," unlike the arm's-length relationships in America. Cauvin, a retired naval officer, is managing director for external relations. What's more, French exports to developing nations require "more and more attention to reliability and operability" of military electronics, Cauvin says. Unsophisticated Third World armed forces have no substantial maintenance capability, he points out, leading to the export of proven, rather than state-of-the-art, systems.

West Germany, on the other hand, has anxiously seized opportunities to gain U. S. technologies, since most of its exports are within NATO and, thus, less subject to U. S. disapproval. The Modular Forward-Looking Infrared System, Modflir, is a case in point. With it, Germany took advantage of the three-to-four-year U. S. lead in night vision to enhance sales of its Leopard tank and tactical missiles like HOT and Milan to smaller NATO countries.

Like the U. S., Britain is weighing the expenditure of its proposed $27 billion defense budget "for more but simpler equipment," says Secretary of State for Defense John Nott. But, like its NATO allies, the UK is encouraging greater specialization among contractors.

WHO SPENT WHAT FOR DEFENSE IN 1980
(in billions of U.S. dollars)

Nation	Total	Percentage of gross national product	Per person
U.S.	142.7	5.5	1,644
West Germany	25.1	3.3	410
UK	24.5	5.2	437
France	20.3	4.0	374
Canada	4.2	1.8	177
Italy	6.6	2.3	115
Denmark	1.4	2.1	274
Luxembourg	0.05	1.1	134
All others in NATO[1]	2.6	3.4	168
Japan	9.0	0.9	75
Soviet Union[2]	165.0	11–13	620

[1] includes Norway, Netherlands, Belgium, Portugal, Greece, and Turkey
[2] Central Intelligence Agency estimate for 1979

SOURCE: NATO AND INTERNATIONAL INSTITUTE FOR STRATEGIC STUDIES

While there are multiple problems, more political than technological, to be resolved within each country of the alliance, more collaborative ventures are deemed necessary by all NATO leaders if the concept of a compatible family of communications and weapons is ever to come about. The Reagan Administration says, as expected, that it supports this approach even though it has yet to spell out the costs to the companies of the alliance: transfer of technology and coproduction (with the U. S.) of electronics advances in terms of discovery by potential enemies as well as copying by allied competitors. In addition, the weapons price tag will unquestionably be higher, as NATO coproduction experience with the General Dynamics F-16 demonstrated. Because of shorter production runs, less plant automation, and lack of competitive pressures, European costs run about 15% to 20% higher than in the U. S., where Congress consistently complains that American military electronics and aerospace products already cost far more than their projections.

These facts of economic life are unlikely to be offset by savings from avoiding duplicate development, even if the UK, France, and West Germany all agree to cooperate fully. Yet this seems to be the tradeoff necessary to achieve NATO standardization. At this point, however, it will be difficult for any of the NATO governments to sell at home, given their internal economic problems. **-R. C.**

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Corp.'s 600-person avionics systems business in Van Nuys, Calif., and then the building up of new operations. Finally, the company will work closely with local universities to build up technology curricula.

Military electronics and aerospace prime contractors in Southern California and other Sun Belt states are in unanimous agreement with Seaberg about lead times on mil-spec semiconductors. They call that the biggest and costliest bottleneck, slowing the accelerated production of existing weapons as envisaged in Washington. Where they disagree with Seaberg is on the engineering shortage in an inflationary environment that discourages both engineers and technicians from changing jobs. Soaring home mortgage rates, for example, "make a lot of people think twice before changing jobs today," says one recruiter in California.

Hughes Aircraft Co.'s Charles W. Wilcox, engineering and program

The Pentagon's three wise men

"It's not always in jest when they are called the three wise men," says one Pentagon manager regarding Secretary of Defense Caspar W. Weinberger (far right), Frank C. Carlucci, his deputy (near right), and Richard D. DeLauer, under secretary for research and engineering (below). "They recognize what the problems are, and they are moving fast to control them." Coming from a bureaucrat who survived the transition to a Republican administration, the words are a high compliment. "They are also rattling a lot of cages around here—especially Carlucci. He is a driven man."

Weinberger and DeLauer, with their milder manner, may appear to be less energetic than Carlucci, but all three are part of a team that is driven to improve the strength and readiness of U. S. forces. At the same time they are determined to price future weapons more realistically and hold down cost overruns by using proven technology wherever possible. Their predecessors failed to overcome those challenges.

What Weinberger and Carlucci have going for them is their knowledge of the Federal bureaucracy and how it works. "They know the pressure points and they have a lot of friends in Congress," says one former aide to Weinberger. A lawyer by training, the 63-year-old Weinberger served the Nixon and Ford Administrations between 1970 and 1975. In that period he moved from chairman of the Federal Trade Commission to deputy director and then to director of the powerful Office of Management and Budget before becoming Secretary of Health, Education, and Welfare. "Cap was not completely happy with the new job," says a friend of Weinberger's. "He believes that Defense, State, or Treasury are the only Cabinet posts worth having" in terms of influence on major policy. Weinberger reportedly wanted the Treasury assignment under Reagan, whom he served in California as director of finance after heading the Little Hoover Commission to reorganize the state government.

Carlucci, 50, first worked under Weinberger at the OMB as his associate and later deputy director and then followed him to HEW as under secretary. In the Carter administration, Carlucci served as deputy director of the Central Intelligence Agency for two years—a period of service that distressed some conservative Reagan advisers when Weinberger sought to have his old associate named as his deputy. "You never heard very much about that flap, and that's to Cap's credit," says a Weinberger friend. "He worked very quietly and he won it. He can maintain a very low profile and still be effective." What most of Carlucci's early critics fail to realize is that nearly all of his career has been with the Federal government, beginning in 1956 in the State Department's Foreign Service and then moving to head the Office of Economic Opportunity in 1971 before joining the OMB.

Under Secretary DeLauer, 62, and like Weinberger a Californian, was not nominated for his post by Reagan until March and finally confirmed by the Senate in May. Yet he, too, knows the system, having served on the Defense Science Board, the military's prestigious technology advisory group, as well as on the Aerospace Industries Association's board of governors. An aeronautical engineer who received his doctorate in 1953 from the California Institute of Technology, he moved steadily upward through the ranks of TRW Inc. to become executive vice president in 1970—the post he gave up to become the Pentagon's technology chief. "He makes a good third man and fits in perfectly with Weinberger and Carlucci," says a senior Pentagon staffer. "He knows management as well as technology and is just as determined to get costs under control as they are. He tends to speak softly, like the secretary, but with just as much candor as the deputy."

How well the contractor and military communities will respond to the separate challenges posed by the Department of Defense's triumvirate has yet to be determined. But no one who has had contact with them and their subordinates is willing to sell them short. **-R. C.**

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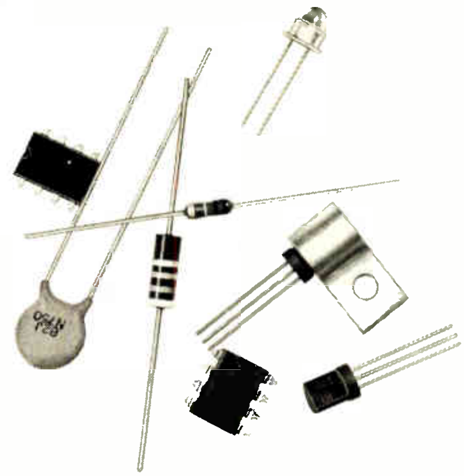

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development director for the company's Aerospace Group in Culver City, Calif., concedes that "we're having substantial difficulty attracting enough qualified people" even though hiring is somewhat easier than during the 1979–80 boom. "The electronics-intensive subsystem side is saturated," Wilcox asserts, creating a problem for Hughes as it tried to gear up for beginning production of new systems as well as increase its output of ongoing programs.

Hiring foreigners. Litton Industries Inc.'s Leon Bloom, director of the Data Systems division's advanced Army and Air Force programs at Van Nuys, Calif., sees one way of getting around the personnel bind: hiring lots of foreign nationals for nonclassified work. His division has pursued this course, since California living costs make it near impossible to recruit in other states. But Bloom notes that design, software, and systems analysis specialists are still in short supply.

Equally desperate short-term solutions are being explored by Hughes's Wilcox. He believes one answer may be to train para-engineers and paraprofessionals, although accelerating production schedules make that difficult, too.

The increasing seriousness of the personnel shortage has other ramifications as well, affecting profits and the possible development of a seller's market. Sperry Univac's Seaberg sees midstream system design changes producing losses for contractors where the resultant costs are not covered by a contract modification. Although the new Reagan management team at the Pentagon is determined to hold engineering changes to a minimum—and to rely on later preplanned product improvement (P³I) to counter obsolescence—this policy may prove difficult to implement, particularly in systems where production begins before the development and operational testing of prototypes is completed.

Until midstream design changes are minimized—and the Sperry executive believes military customers and contractors must share the blame equally since both sides have design engineers who constantly want to make changes—Seaberg suspects that contractors in today's expanding market "probably will tend to stay away from [military] customers that have a reputation for nickel-and-diming you" with costly program alterations.

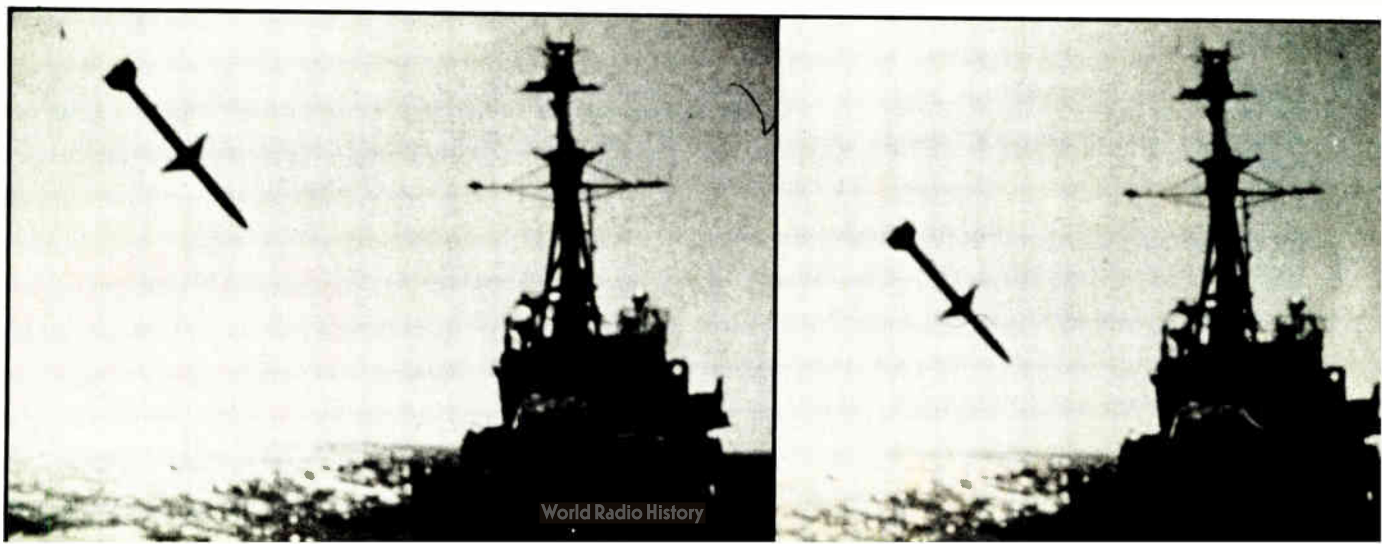
Yet there are virtually no military electronics makers running from the major contract opportunities being offered by the Pentagon's new managers. The range of electronic technologies involved is as varied as the military users they must serve. The needs range from space—with its communications and surveillance satellites, to be followed much later by more exotic antisatellite weapons and lasers to destroy intercontinental ballistic missiles in flight—to the world's ocean bottoms, where the emphasis is on both missile-firing and attack submarines and on the antisubmarine-warfare sensors, mines, and torpedoes needed to destroy them.

The Reagan team wants most to build U. S. strength in these strategic areas as well as those in between—tactical air, land, and sea systems for fighting and winning without resorting to nuclear warfare. For the next three to five years, the biggest share of production funds will be used for increasing quantities of tactical weapons and what the military calls C³I—command, control, communications, and intelligence—systems to coordinate tactical and strategic operations. At the same time, R&D monies will push development of improved subsystems to upgrade systems already in use for research into new technologies.

Priorities listed. Beyond the aircraft and missiles themselves—where the Reagan Administration initially wants to buy larger quantities of production or development systems—the military consensus is that secure C³I systems and associated countermeasures need top priority. Compared to the marginal improvements that can be seen for aircraft and missile airframes and engines, the growth opportunities for electronics are almost open-ended, argues Lt. Gen. Stansberry, the new commander of the Air Force's Electronic Systems division. But Stansberry also echoes Deputy Secretary of Defense Carlucci when he advises contractors to reorient their designers toward systems with less risky technologies that work and can be delivered quickly.

This scares some industrialists. They fear that the near-term emphasis on sharp increases in quantity purchases of existing systems is that this will mean, as one put it, "the

In Harm's way. Harm air-to-ground missile from Texas Instruments scores a direct hit. The Pentagon wants to increase its purchase to 350 missiles costing $434.5 million for the combined fiscal years 1981–82 from the 80 missiles for $174.2 million called for in the Carter Administration's defense budget.



Japan builds on U. S. licenses

Sheltered by the U. S. military umbrella for more than 35 years and operating outside the turbulent North Atlantic Treaty Organization, Japan's small military electronics industry is almost the image of its giant consumer products counterpart in its early years. Many weapons systems made in Japan are produced under licensing agreements from U. S. companies—the McDonnell Douglas F-15 fighters being built by Mitsubishi Heavy Industries Ltd. and the Raytheon Hawk and Sparrow missiles produced by Mitsubishi Electric Co. are cases in point.

Another aspect of the image is that the Japan Defense Agency values product performance over cost in choosing between domestically produced competing systems. It is unlike the U. S. approach, maintains Gitchi Ohyama, general manager of two of Nippon Electric Co.'s divisions selling to the JDA.

In fact, Japan is unlike the U. S. in many military matters, spending only 0.9% of its gross national product on arms for its own defense—some $11.5 billion in the 1981 fiscal year, which ended March 31. And only $134 million of that went to the JDA's Technical Research and Development Institute to conduct and oversee research, development, design, planning, manufacturing, and testing. The result: the 99 members of the Japan Ordnance Association, the industry lobby with 43 electronics suppliers, must use much of their own money for R&D.

Nevertheless, Japanese manufacturers say they stay in the military market in the hope that it will expand, provide technological fallout for their profitable commercial and industrial businesses, and, says NEC's Ohyama, because of a sense of duty. Jinshichi Hirano, the JDA's director, estimates that 80% of Japan's military electronics is produced domestically. He notes that his country not only has a small domestic market—a problem shared by America's NATO partners—but is also constitutionally precluded from building or exporting offensive weapons. In addition, economies of scale are ruled out because there are so many small producers.

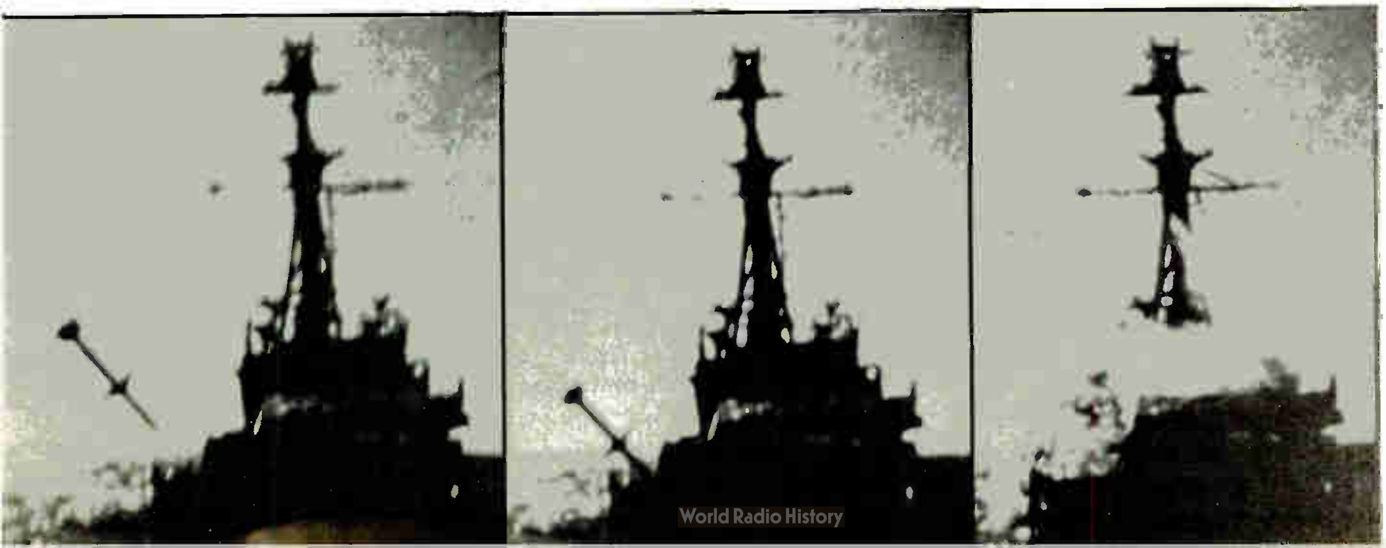
Between fiscal 1974 and 1979, production of weapons in Japan rose by 28% to $2.28 billion. Military electronics production in that same period climbed 53% to $338 million, boosting its share of overall weapons output to 30% from 23%. The JDA's three largest electronics suppliers and their fiscal 1980 backlog are: Mitsubishi Electric with $337 million, Toshiba Corp. with $153 million, and Nippon Electric with $104 million. But NEC is by far the most diversified, with 291 contracts versus Mitsubishi's 188. Mitsubishi Electric specializes in fire-control systems, with about 60% of the missile guidance market and 90% of the electronic warfare market. Takeshi Abe, general manager of the Government Requirements Marketing division, says 50% of the production value of Mitsubishi's work is done under license with foreign companies or by coproduction involving importing key parts for domestic assembly. For example, it is building the F-4EJ Phantom fighter's fire control under coproduction with Westinghouse Electric Co. of Baltimore, Md., and the F-15's with Hughes Aircraft Co. of Culver City, Calif.

NEC, which derives about 3% of its total sales from defense electronics, has licenses with 15 U. S. companies, says Ohyama. About half are for systems in the F-15 fighter and the P-3C antisubmarine patrol plane, the latter being built by Kawasaki Heavy Industries Ltd. Ohyama figures about 20% of the company's military electronics product lines were developed with JDA funds, another 20% made under license, and the rest developed internally. Though its biggest military sales are for sonar and radar, Ohyama regards computers and communications as NEC's forte. Though he concurs with Mitsubishi's Abe that JDA interest now is strong in electronic warfare systems, Ohyama also sees strong interest in missiles.

What Japanese manufacturers lack, says the JDA's Hirano, is sophistication in weapons systems software, which is leading to a proliferation of imports of supersecret black boxes for missiles. He blames this on a lack of technicians and R&D spending at JDA and its lagging interest in software. "Makers can't do it alone," he argues, "because they need the user's input." Hirano also claims that the number of JDA personnel expert in evaluating technology is declining. **-Robert Neff and Ray Connolly**

'ins' are in, while the 'outs' are out." However, for electronics that is not so, says one Defense Department program planner. He explains that increasing quantities principally affect the big aerospace primes in the aircraft and missile business. He goes on to say, "The P³I [preplanned product improvement] upgrade program will be designed to give proven performers a shot at new subsystems for existing platforms."

Typical of near-term upgrading in the command and control area already beginning servicewide is the addition of antijam capabilities to transceivers operating at high, very high, ultrahigh, and L-band frequencies. Even though high-frequency technology is usually decried as "old and tired," says one Defense Com-



munications Agency specialist, "it does work, is relatively cheap, has long range, and is adaptable to antijam." The Navy sees its hf improvement program as one that will complement its 30-to-300-gigahertz extrahigh-frequency satellite system for long-range communications, says Vice Adm. Gordon R. Nagler, command and control director for the chief of naval operations.

For Navy line-of-sight tactical systems, Nagler is overseeing two other efforts to improve connectivity. First is the straightforwardly-named Combination Radio Plus AJ (for antijam) Applique and the seagoing segment of the Joint Tactical Information Distribution System (JTIDS), the complex and thus controversial triservice digital data and voice system. The combination radio, explains Nagler, is a vhf-uhf-a-m/fm system that will replace current Navy airborne uhf radios. The antijam applique, he says, would be compatible with the Army's vhf/AJ version of Sincgars (single-channel ground and airborne radio subsystem), as well as with the Air Force antijam initiative in its uhf Have Quick system.

Millimeter waves. For Army battlefield command and control, the service is exploring millimeter-wave radars and radios for the mid-1980s and later, according to Lt. Gen. Donald R. Keith, deputy chief of staff for research, development, and acquisition. But the chief of staff, Gen. Edward C. Meyer, is apparently more interested in basics; he calls the Army "a hollow shell" requiring its biggest buildup in force structure and training, as well as weapons.

Maj. Gen. Albert N. Stubblebine III, head of the Intelligence Systems Command, concedes that the Army "tends toward conservatism" in uses of highly sophisticated electronics, for two reasons. "We operate in a very dirty environment. The Air Force's 'blue yonder' is cleanest, while the Navy's biggest problem is salt water." And the second reason is: "if there is a way something can be broken, the soldier will find it."

Army high-technology management also tends to turn off the electronics community, say Congress's auditors at the General Accounting Office, a regular critic of overreaching by all three services. A current GAO favorite in its collection of horror stories is Sotas, the Standoff Target Acquisition System that the House Armed Services Committee wants to kill.

Sotas, mounted on a Sikorsky YEH-60B Black Hawk helicopter, employs radar for day and night detection and location of enemy ground and air vehicles beyond the forward battle line. A communications link then relays this information for display to division commanders. "It is not only highly vulnerable, but the detection and data links work poorly," says one GAO official, noting that the program cost estimates "are out of sight."

Too many cooks. Part of the Army problem, says the GAO, is that management of the major Sotas components—the helicopter, radar, and data link—is diffused among three separate and independent project offices. Sharing prime contractor responsibilities with Sikorsky Aircraft of Stratford, Conn., on Sotas electronics is Motorola Inc.'s Government Electronics division, Scottsdale, Ariz. Compounding the contractors' problems, according to the GAO, were unanticipated technical problems caused by use of unproven, advanced technology, plus the fact that the critical data link has to meet the requirements of two other unrelated programs.

"This is a classic worst case," admits one Pentagon aide. Yet, he adds, "the Army does need this kind of capability and quickly. We must rethink Sotas—and a lot of other programs—where overly complex technology was bought because military managers want multimission weapons. That generates too many technical unknowns when too many different electronic subsystems, all state-of-the-art, must interface and work together."

For the Air Force C³I contractor community, Maj. Gen. Jasper A. Welch has a related message. As special assistant to the chief of staff, Welch concedes that "we in the military do not spend enough time thinking about the wartime situation" in which C³I is essential to controlling chaos and preventing a fighting force from becoming "a mob." His prime concern: the lack of spare parts, so desirable in peacetime to keep down costs and "the inventory float," is altogether different from the wartime need to keep planes in the air and C³I operational. While the Reagan Administration is beginning to address this issue by increasing orders for initial spares, Welch's wartime command and control concerns are that C³I systems designed in peacetime for maximum efficiency are most likely to fail under stress or limited damage.

Efficient vs effective. Yet performance efficiency of communications systems—the all-things-to-all-men design syndrome—usually drives design of hardware systems or management information systems in peacetime. But Welch says he ranks efficiency "somewhere between tenth and seventeenth" in a list of C³I goals. At the top are maintenance of force cohesiveness, avoidance of blunders and disasters, and provision of "some nonzero effectiveness to avoid being totally ineffective." The Soviet Union, Welch says, "consistently ridicules the West" for its inattention to this aspect.

Military R&D dollars in the next two fiscal years are expected to keep pace with true inflation but not much more. That is the judgment of congressional and military staffers who have seen the Defense Department's first tentative projections of fiscal 1983 spending plans. For the year beginning in October 1982, total R&D is estimated to exceed $24 billion, or 13% more than the Reagan 1982 request. Despite OMB estimates that military program inflation rates will drop to 7.3% in that year [*Electronics*, May 5, p. 64], military and industry sources say privately that a 13% R&D spending rise will keep the budget essentially flat. Procurement accounts will continue to get the greatest emphasis in fiscal 1983 with requests for aircraft up 13% to $29.25 billion and missile purchases rising 34% to nearly $13.8 billion.

Nevertheless, R&D emphasis will be heaviest on electronic components and related technologies including fiber optics, on infrared and millimeter-wave radars for both target

REAGAN FACES THE REALITIES OF OVERRUN
(in millions of dollars)

	Weapon system	Base year	Base year estimate	Current total
ARMY	Patriot missile*	1972/P	4,009.1	8,465.9
	Pershing II missile	1979/D	1,249.7	1,794.2
	Hellfire missile	1975/D	767.5	1,484.1
	UH-60A helicopter	1971/P	2,462.8	7,293.5
	AH-64 helicopter	1972/D	2,196.6	5,958.2
	SOTAS (division sets)	1979/D	1,329.1	2,239.0
	M-1 tank	1972/P	5,097.4	18,585.9
	Roland missile*	1975/P	1,807.3	3,324.1
	DIVAD gun	1978/D	2,515.0	4,470.6
	MLRS support rocket (*firing segments only)	1978/P	2,211.3	3,954.8
NAVY	E-2C warning aircraft	1968/P	1,830.9	3,696.6
	F-14A fighter	1969/P	8,201.4	12,055.0
	F-18 fighter	1975/P	13,906.8	35,297.0
	P-3C ASW plane	1968/P	3,570.9	8,399.3
	LAMPS Mk III helicopter	1976/D	3,184.4	6,369.2
	Captor ASW mine	1971/P	712.9	1,551.8
	Harm missile	1978/D	1,141.0	2,141.1
	Harpoon ship missile	1970/P	1,041.6	2,149.0
	Phoenix missile (F-14)	1963/P	1,139.2	2,629.5
	Sidewinder AIM-9M missile	1976/P	228.0	439.2
	Sparrow AIM-7M missile	1978/P	628.1	1,039.5
	Tomahawk cruise missile	1977/D	1,999.4	3,044.9
	Trident ICBM sub	1974/P	16,517.1	29,920.5
	Surtass ASW sonar	1975/P	444.4	863.3
	SSN-688 attack sub	1971/P	7,084.2	14,567.2
	CG-47 Aegis cruiser	1978/P	13,026.1	22,149.7
	CVN-71 carrier	1979/P	1,857.9	2,595.3
AIR FORCE	A-10 attack plane	1970/P	2,385.0	5,410.3
	F-15 fighter	1970/P	7,090.4	15,375.7
	F-16 fighter	1975/P	9,920.7	20,278.8
	E-3A AWACS	1970/P	2,558.7	4,455.0
	E-4 command post (AABNCP)	1974/P	692.2	1,053.1
	EF-111A airborne jammer	1973/P	703.2	1,416.5
	Precision Location Strike	1977/D	330.7	475.5
	Harm missile (AGM-88)	1978/D	1,666.4	3,540.0
	Maverick IR missile	1975/D	1,720.2	4,128.7
	Sidewinder AIM-9M missile	1976/P	280.5	510.2
	Sparrow AIM-7M missile	1978/P	941.4	1,578.3
	DSCS III satellite (space segment)	1977/D	714.6	1,168.6
	Navstar/GPS satellite	1979/D	1,571.3	2,197.0
	ALCM cruise missile	1977/P	3,658.1	5,864.0
	GLCM cruise missile	1977/D	1,783.0	3,186.1
	Total		136,976.5	277,116.2

Note: The most recent cost totals for March 31 are expressed in millions of dollars; the letter P or D after the base year indicates whether a program is currently in procurement or development

SOURCE: DEPARTMENT OF DEFENSE

detection and terminally guided munitions, and on manufacturing technology with particular stress on computer-aided design (CAD) and manufacturing.

Certainly the hottest new program is the triservice Very High-Speed Integrated Circuits (VHSIC) effort [*Electronics*, May 19, p. 40]. Directed by the Pentagon's Larry W. Sumney, VHSIC last month selected six contractors to begin the program's first phase. That covers development over the next three years of complete electronic brassboards on pilot production lines that will include chips with 1.25-micrometer feature density operating at a minimum clock of 25 megahertz and a functional throughput rate of 5×10^{11} gate-hertz per centimeter squared (clock rate times equivalent gate density).

After that, Phase I contractors will push to extend IC technology to 0.5-μm features by using high-resolution lithography and replication; improvements in substrates, epitaxial growth, and reliability of the metalization; interconnect analysis; and CAD techniques. "Chips resulting from this effort," Sumney says, will have "a functional throughput rate of 10^{13} gate-Hz/cm^2."

In the follow-on second phase, estimated to cost $72 million over the three years when it begins in fiscal 1984, parallel programs will involve subsystem demonstrations in weapons based on first-phase brassboards, as well as continuing the submicrometer development effort.

Big firms involved. The ongoing $57 million phase III technology support program already has 50 contracts outstanding. Efforts to draw universities into the support program "have been only partially successful to date," Sumney admits. Only seven schools and research institutes are participating, with Cornell University's research group the largest in terms of awards. "Large companies," Sumney says, "dominate the supporting technology effort." Results of the supporting technology work will be made available to all VHSIC primes equally.

Yet VHSIC circuits, assuming their success, will not be militarily operational on a large scale for another decade. With the lead times on conventional ICs with military specifications now stretched to two years in most cases, what can the Pentagon do to prevent second- and third-tier components subcontractors from becoming a bottleneck in the Reagan military buildup? "Buy commercial," respond IC producers nationwide. The Naval Material Com-

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mand in Arlington, Va., has been pushing this concept hard through Willis J. Willoughby, who is responsible for reliability, maintainability, and quality assurance. Though the idea of buying high-reliability, user-tester circuits has support from the Navy plus some segments of the Pentagon, it is strongly opposed by much of the Air Force [*Electronics*, May 19, p. 132].

One industry supporter of using highly reliable commercial components in military programs is Texas Instruments Inc.'s J. R. Junkins, vice president and manager of the Dallas-based equipment group. Commercial parts would, he says, "certainly help in making systems more cost effective for the same reliability or maybe an improvement in reliability." He contends that "all you are buying is test results, paper, and not necessarily that much change in reliability." While the Weinberger-Carlucci team is listening carefully and evaluating such arguments, the issue is far from resolution.

Fiber optics. Still in its infancy, the fiber-optics industry is now at the "same stage as the telephone system was 50 years ago, the integrated-circuit industry 20 years ago, and the microprocessor industry 10 years ago," says Glenn W. Carter of Dale Electronics Inc., Columbus, Neb. Nevertheless, the military is enthusiastic about its potential. So are manufacturers who heard Defense Electronic Supply Center officials tell them in late April that, unlike semiconductor military specifications, the new Pentagon regime has directed "maximum use of non-Government standards" for fiber optics in deference to industry's own recommendations.

When the approach became known at the Electronic Industries Association's first fiber-optics standards conference, the EIA immediately leaped into the breach and established a fiber-optics working group designated EIA P-6. It has six subgroups dealing with systems as well as standards for cable sizes, connectors, sources, detectors, couplers, and modules.

The Government/military market for fiber optics totaled $21.9 million last year, or 37% of the U. S. total, according to a presentation to the EIA session by Gnostic Concepts Inc., a Menlo Park, Calif., research organization. That Government share compares with 21% for commercial telecommunications. By 1985, according to the study, the Government market will grow to $154 million, and then more than double to $332 million in 1990.

Many pluses. Fiber cable, of course, weighs less and occupies less space than copper. A 1,000-foot reel of fiber cable weighs about 10 pounds, compared to the 75 lb of a 250-foot reel of 26-pair copper cable. But military enthusiasm for fiber focuses more on its inherently superior security and its resistance to jamming, electromagnetic interference, and electromagnetic pulses from nuclear bursts.

Who is in the lead? Few dispute that the American Telephone & Telegraph Co. is at or near the front in commercial uses. On the military side, however, several contenders claim leadership. Among them are GTE Sylvania's Communications Systems division in Needham Heights, Mass.; Litton Data Systems in Van Nuys, Calif., which is working with International Telephone & Telegraph Corp.'s Electro-Optical Products division of Roanoke, Va., on a Marine Corps program; and Valtec Corp. in West Boylston, Mass., a joint venture owned by North American Philips and M/A-Com, also of Massachusetts.

Whoever is ahead, both military users and contractors see the market potential expanding in direct proportion to how fast the EIA's working groups can come up with standards. "The most work," says one Pentagon specialist, "needs to be done in connectors, couplers, and modules. Industry has got the ball now. They'd better not fumble it" in what is certain to be a closely watched standards effort. For it represents a landmark opportunity for an industry to do its own thing—regulate itself, as it were—without over-regulation by the Government and the resultant mountains of paper. □

THE MILITARY'S FISCAL 1983 WISH LIST
(in millions of dollars)

	1982	1983	Change (%)
Research and development			
Army	3,905.2	4,709.5	+20.6
Navy and Marine Corps	6,083.3	6,743.1	+10.8
Air Force	9,398.1	10,128.5	+ 7.8
Defense agencies	1,881.4	2,464.0	+31.0
Procurement			
Aircraft			
Army	1,787.4	2,401.4	+33.6
Navy	9,352.5	10,269.1	+ 9.8
Air Force	14,751.9	16,577.0	+12.4
Missiles			
Army	2,482.5	3,496.2	+23*
Navy	2,555.0	2,938.3	+15
Marine Corps	223.0	72.2	−67.6*
Air Force	4,658.2	7,285.3	+56.4
Tracked combat vehicles			
Army	3,487.3	3,993.5	+14.5
Marine Corps	281.7	329.8	+17.1
Torpedoes and support			
Navy	516.6	603.4	+16.8
Ships			
Navy	10,290.1	10,709.7	+ 4.1

*reflects transfer in procurement responsibility from Marines to Army

SOURCE: DEPARTMENT OF DEFENSE

Reporting for this article was provided by Terry Costlow, J. Robert Lineback, Linda Lowe, Larry Waller, and Wesley R. Iversen in the U.S.; Kenneth Dreyfack, James Smith, and Kevin Smith in Europe; and Robert Neff in Japan.

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Epitaxial layer blocks unwanted charge in MOS RAMs

Lightly doped epitaxial layer permits the use of a heavily doped substrate that sweeps away error-causing superfluous minority carriers

by G. R. Mohan Rao, L. S. White Jr., and Richard N. Gossen, *Texas Instruments Inc., Houston, Texas*

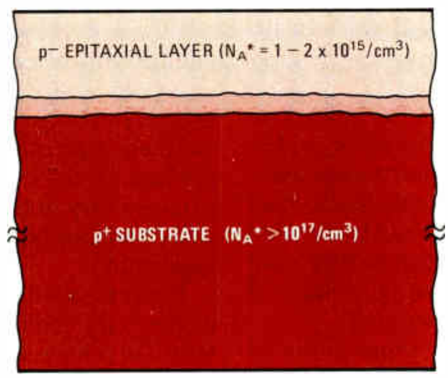
☐ All 64-K dynamic random-access memories borrow circuit and processing innovations from previous chip designs. However, in doing so, they have often carried over some of the operational hazards of 4- and 16-K RAMs and exacerbated them with narrower line widths. Consequently, although it has been widely believed that fundamental changes can wait until the 256-K level, it turns out that the storage and sensing demands of 64-K chips have hastened the need for improved fabrication techniques.

One such technique is the use of epitaxial silicon. A problem that has been growing with increasing chip density is the control of stray charged particles, and an epitaxial layer provides that control.

Storage capacitors now hold so few electrons that the slightest amount of external noise can upset valuable data. Noise can come from the rapid switching of address signals applied to the chip or from a particular input data pattern. In addition, it is now widely recognized that superfluous charge is also generated by alpha particles [*Electronics*, Feb. 10, 1981, p. 93].

Building a RAM in an epitaxial layer combats this noise by separating wanted from unwanted charge. The layer, being lightly doped, increases the lifetime of electrons, thus increasing the holding power of the memory cells. In contrast, the substrate under the layer has a much lower resistivity, and it is grounded. As a result, electrons generated in this bulk material are swept away and not allowed to interfere with critical active areas.

The construction of an epitaxial layer turns traditional chip fabrication upside down. As shown in Fig. 1, the starting material is very low-resistivity p^+ silicon. On top of this substrate a thin layer of high-resistivity p^- silicon is epitaxially deposited. The resistivity of the epitaxial layer approximates that of a conventional single-crystal substrate because of its low concentration of about 1×10^{15} to 2×10^{15} acceptor ions per cubic centimeter—several orders of magnitude less than that of the substrate.



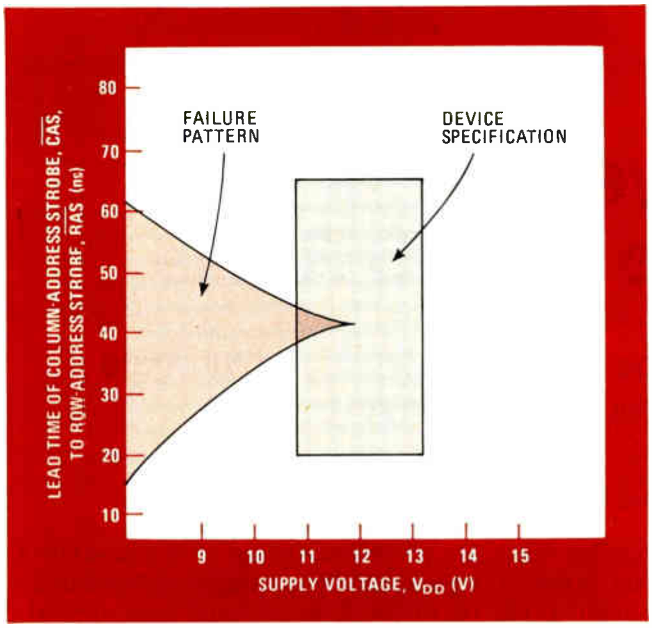
1. On epi. To protect a random-access memory from external noise, a thin, lightly doped layer is epitaxially grown on top of heavily doped starting material before device fabrication. The highly conductive substrate sweeps away excess electrons.

Intimate encounter

Thus, with an epitaxial layer two materials with vastly different properties are brought into intimate contact. The characteristics of each type of silicon are used to maximize memory performance. Minority-carrier (electron) lifetime in the epitaxial layer is very long, just as it is in a single-crystal substrate. On the other hand, lifetime in the substrate is relatively short, making it easy for electrons to recombine. In a memory device, this combination leads to an expanded refresh period for the memory array and a fast discharge path for nodes on the periphery of the chip by providing a ready sink for minority carriers.

The difference in the dopant concentration of the substrate and the epitaxial layer establishes a transition region where the layer meets the substrate. Rather than being a uniform, perfectly defined crystal, the interface is a poorly oriented structure, but that proves to be advantageous because contaminating heavy ions migrate to the interface and become trapped.

In normal silicon processing, no matter how pure the starting material is, impurities always emerge as the substrate is put through high-temperature MOS processing. Some of the heavier metals, oxygen, and carbon



2. Like a dog's tail. When the address signals applied to a dynamic RAM are switched quickly between minimum and maximum levels, the noise generated may cause the multiplexing time to become a function of supply voltage. The part may then fail specification.

drift to the top of the substrate. Indeed, one of the long-standing problems in silicon processing is keeping oxygen from the surface of the chip, for once there it degrades the threshold voltage.

Epitaxial construction is highly insensitive to oxygen content, since the substrate material does not have to be very pure. The impurities are trapped in the interface without causing performance problems. Once caught up in the interface, such particles are never re-released.

Thickness not critical

The thickness of the epitaxial layer is not critical, as it neither defines nor controls the operation of the transistors in the circuit. In V-groove MOS devices, in sharp contrast, the thickness of the epitaxial layer defines the critical channel length.

In conjunction with input clamping and filter circuitry, epitaxial construction yields excellent operating margins. A typical TMS 4164 64-K RAM can tolerate negative dc input levels of up to 2 volts and several volts of ac undershooting having a bandwidth of 20 ns or wider. This tolerance is important because, under typical operating conditions, input address and clock levels may undergo an undershoot of -2 to -3 V for a short period of time—say, 20 to 30 ns. Such undershooting can forward bias on-chip n^+p diodes, generating millions of electrons that can render a device nonfunctional.

All 64-K dynamic RAMs draw on some form of advanced semiconductor processing to achieve a high packing density and single-supply operation. But most manufacturers rely only on circuit design to prevent injected carriers from interfering with the low charge levels in the cells and critical peripheral nodes.

Generally, a charge pump is used to establish a bias voltage in order to control injected carriers within the bulk silicon substrate. This -5-V V_{BB} supply provides the 1.3-to-1.8-V threshold voltage required for proper device operation and also minimizes parasitic junction capacitance. An epitaxial layer, however, far outperforms the bias generator. Furthermore, the epitaxial approach sets the stage for building even larger memory arrays—like those in 256-K chips—that will have a major role in future computer systems.

For a single-crystal substrate to support memory operation with a reasonable access time of less than 200 ns, its resistivity must be about 15 to 20 ohm-centimeters. Such a value yields an effective parasitic junction capacitance low enough for satisfactory memory operation.

In general, devices built in higher-resistivity material exhibit lower junction capacitance. But ironically, this lower capacitance can actually compromise performance. Junction capacitance is inversely proportional to the width of the depletion layer; the wider the depletion layer, the lower the parasitic capacitance. That would seem to be a desirable effect; however, a wider depletion layer uncovers more generation-recombination (G-R) centers, and bulk leakage is linearly proportional to the density of those centers.

Increasing the number of G-R centers reduces the time that charge can be stored on a capacitor, shortening the refresh time of the device. Therefore a basic challenge with single-crystal silicon is holding the resistivity low enough so as not to degrade the power-delay product of a circuit while holding the depletion layer shallow to obtain as long a refresh time as possible.

If single-crystal material with a resistivity of 15 to 20 Ω-cm is used with a single 5-V supply, the depletion layer while storing a logic 1 level will be no more than a few micrometers below the surface. All important device parameters like charge storage and charge transfer are dominated by those few micrometers nearest the surface. In the 1 state, both sides of the storage capacitors are charged to 5 V, creating an absence of electrons. Although a 0 state is not disturbed, even if many more electrons are introduced at the surface of the chip at high temperature, there can be problems in the 1 state.

Pattern sensitivity

In every memory cycle, during row- and column-address switching the charging and discharging of nodes associated with clock and sense amplifiers creates millions of free electrons. In a given memory cycle of 300 to 400 ns, these electrons are free to float about the substrate and occasionally discharge a stored 1 level. The device's susceptibility to this condition shows up as pattern sensitivity and can be measured with a so-called disturbance algorithm.

Pattern sensitivity means that a memory's failure modes vary with the test pattern of input data. Such sensitivity may surface in reading, writing, or simply retaining data. It can be caused by the dynamic nature of the data-storage process itself or by coupling between physically adjacent bits. Subthreshold leakage in transistor gates may also be a contributing factor, and so can the interaction of peripheral circuitry with a stored bit via RC noise or substrate coupling. The offending peripheral circuitry can be data lines, sense amplifiers, on-chip clock generators, and so on.

TABLE 1: 64-K MEMORY REFRESH PERIOD WITH AND WITHOUT EPITAXY (ms)

Five test units with single-crystal substrate		Five test units with epitaxial layer	
Burst algorithm	Disturbance algorithm	Burst algorithm	Disturbance algorithm
313	5	502	92
234	<4	>1,000	132
184	<4	600	57
247	<4	520	111
196	8	430	87
14	<4	241	56

NOTE: Case temperature = 70°C; power supply, V_{DD} = 4.5 V.

Many of the most successful tests for dynamic RAM pattern sensitivity employ a column-disturbance algorithm. With this scheme, the entire RAM is written with 1s or 0s. Next, one row is written to the opposite polarity. This row is then read continuously for a predetermined time, usually one refresh interval, or 4 milliseconds in the case of the 4164. The algorithm is termed a column-disturbance one because noise coupled to adjacent rows will show up as a column-related error. The test is repeated for each row, for both 1 and 0 data states, at both high and low values of the power-supply voltage, V_{DD}, and at the temperature extremes.

The reason that column-disturbance pattern testing places such a high stress on the cells in a dynamic array is that the algorithm causes several hundred picofarads of capacitance to be discharged almost 10,000 times every 350 ns. This high capacitance is primarily associated with the bit lines. The charge pumped back and forth between the storage nodes and the substrate eventually takes its toll on the 1s stored in nodes adjacent to the disturbed rows.

Epitaxy prevents this sort of disturbance. Data stored in 64-K dynamic RAMs with epitaxial construction exhibits a high immunity to pattern sensitivity, even when subjected to the rigors of testing under a column-disturbance or similar algorithm. The high data integrity allows longer periods between required refreshes, as can be seen in Tables 1 and 2.

TABLE 2: DISTURBANCE REFRESH PERIOD FOR FIVE TEST DEVICES WITH EPITAXY AT 90°C (ms)

V_{DD} = 4.5 V	V_{DD} = 5.5 V
31	128
49	43
35	34
43	42
71	74
26	23

Smoothing pad bumps

Single-crystal silicon is responsible for the failure of several 16-K RAMs to operate properly under certain multiplexing conditions. Dynamic RAMs function with the row-address strobe ($\overline{RAS}$) acting as a chip-enable signal and the column-address strobe ($\overline{CAS}$) serving as a chip-select signal, with the addresses performing the switching in a multiplexed mode.

Depending on the timing between $\overline{RAS}$ and $\overline{CAS}$, conditions can arise under which the device will not operate properly, particularly if the input levels are allowed to swing between +7 and −1 V, the maximum permissible excursion according to most user-specifications. Under those conditions, the peculiar problem of address-pad bumping—or dog-tailing—occurs (Fig. 2). The multiplexing time becomes a function of the supply voltage and the device cannot meet specifications.

The address inputs are capacitively coupled to the substrate, and high-resistivity materials inadequately dampen this noise. Hence, the noise couples onto the diffused n^+ bit lines, where the interference prevents proper sensing of data. In particular, if a voltage swing occurs at a time when data is being sensed, the bit lines will swing suddenly in the opposite direction, resulting in incorrectly detected or restored data, or both.

If the memory is allowed to operate between the minimum 1 and maximum 0 TTL levels, there may be fewer problems with address-pad bumping. However, in most systems, that is not always possible. In fact, the condition is magnified when a large number of memory devices are tied to a common bus line. In that case, a slight upward surge in the supply voltage is likely to cause the more sensitive memories in the system to fail.

The high-conductivity substrate beneath the epitaxial layer quickly dampens noise within a short distance. In effect, the substrate acts as a low-impedance ground plane, so that noise generated by address coupling is shorted out in the substrate before it reaches critical sensing nodes. Unlike memory designs based on large storage cells or folded bit lines to enhance common-mode signal levels, the epitaxial solution costs no additional chip area.

Alpha-particle sensitivity continues to hamper dynamic RAM operation, prompting most manufacturers to place some type of protective material on the chips. An epitaxial layer may offer a natural partial solution to soft errors. Depending on the angle at which they struck the chip, alpha particles drifting within 25 to 30 μm of the surface can free electrons that are then able to discharge a stored 1. However, since the layer is much thinner than the substrate, many of the electrons within 25 to 30 μm of the surface recombine in the low-resistivity substrate before they can reach the storage capacitors. □

Supercomputer outdoes itself by designing its successor

Computer-aided design systems and simulation helped the Cyber 205 to hit the ground running

by Anthony A. Vacca and Neil R. Lincoln
Control Data Corp., Minneapolis, Minn.

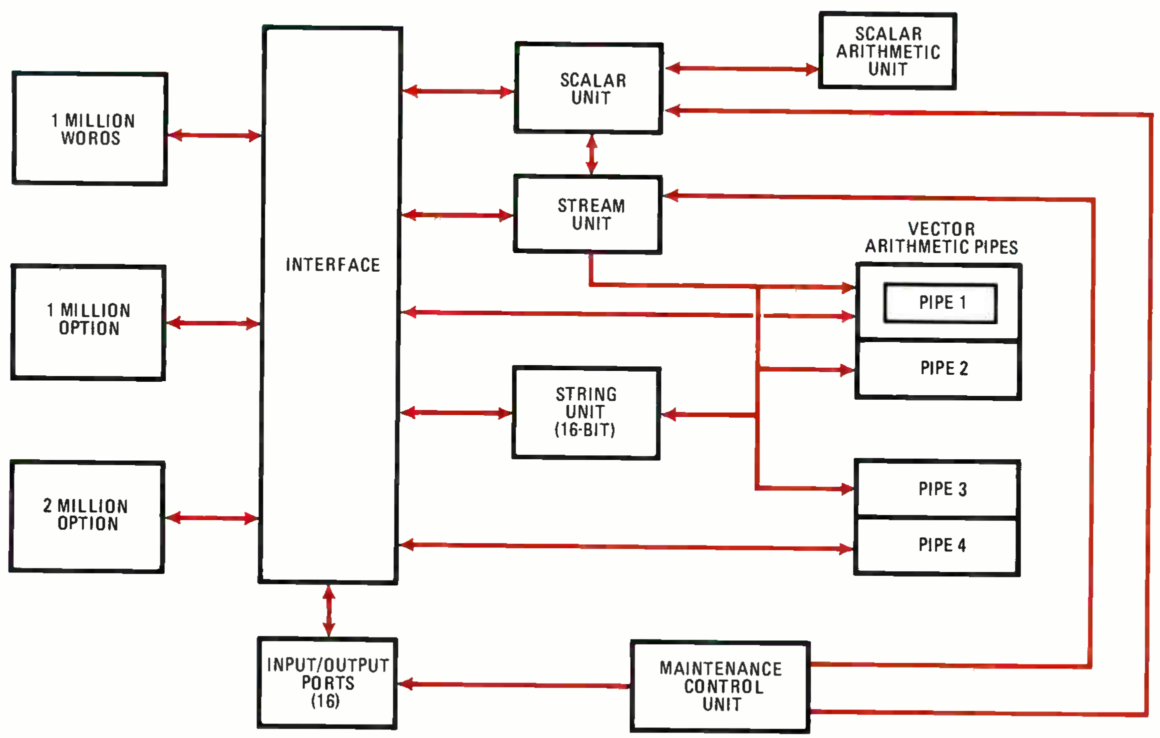
☐ Control Data Corp. treats its breed of supercomputer as a coach treats a world-class runner—both push machine and athlete to nearly the breaking point. Like the athlete, when a glorious career has climaxed, a CDC supercomputer will be working on the design of future front runners so they too can win the big race.

At the moment, the fastest computer in the world is the recently introduced CDC Cyber 205. It is a system that, in its maximum configuration, is up to eight times faster than any previous CDC supercomputer and more than three times faster than any computer that is currently available (Fig. 1).

The Cyber 205 was designed with a strong capability for the accurate simulation of recently developed CDC computer designs. It allows design engineers to verify and modify their design, predict performance, and discover design errors before a computer is built. Several generations of CDC supercomputers have run versions of this system to assist in the design and fabrication of their successors and have been building on an architecture dating back to 1965. The Cyber 205 was designed with the help of the Cyber 203.

Components in such equipment must operate at their predesigned limits. By using an advanced, hierarchical computer-aided design and verification system with computer-aided manufacturing capabilities that supports simulation by supercomputer, a designer can be assured that the system will meet specifications.

With this advanced CAD/CAM system, Cyber 205 reaches new milestones in concurrent computing:



(a)

- Scalar processing of up to 50 million instructions per second.
- Linked-vector-stream processing of up to 800 million floating-point operations per second.
- Vector floating-point arithmetic hardware divided into one, two, or four units or pipelines, with most scalar instructions executing in parallel with vector operations.
- Four million 64-bit words of central memory.
- Two trillion words of virtual memory.

The Cyber 205 is the first supercomputer to use emitter-coupled logic in both scalar and vector units, with 168 ECL switches per chip and subnanosecond speeds. Its input/output system has eight I/O ports that are expandable to 16; each port concurrently handles up to 200 million bits per second, providing a memory bandwidth of up to 3.2 billion bits per second. Cyber 205 users can take full advantage of this kind of data flow through advanced features that include: an instruction repertoire providing computation and storage on 32-bit half words as well as 64-bit words; a unified floating-point arithmetic structure with extended capabilities; and mapping algorithms for operations on arrays of bit strings that can more than double throughput.

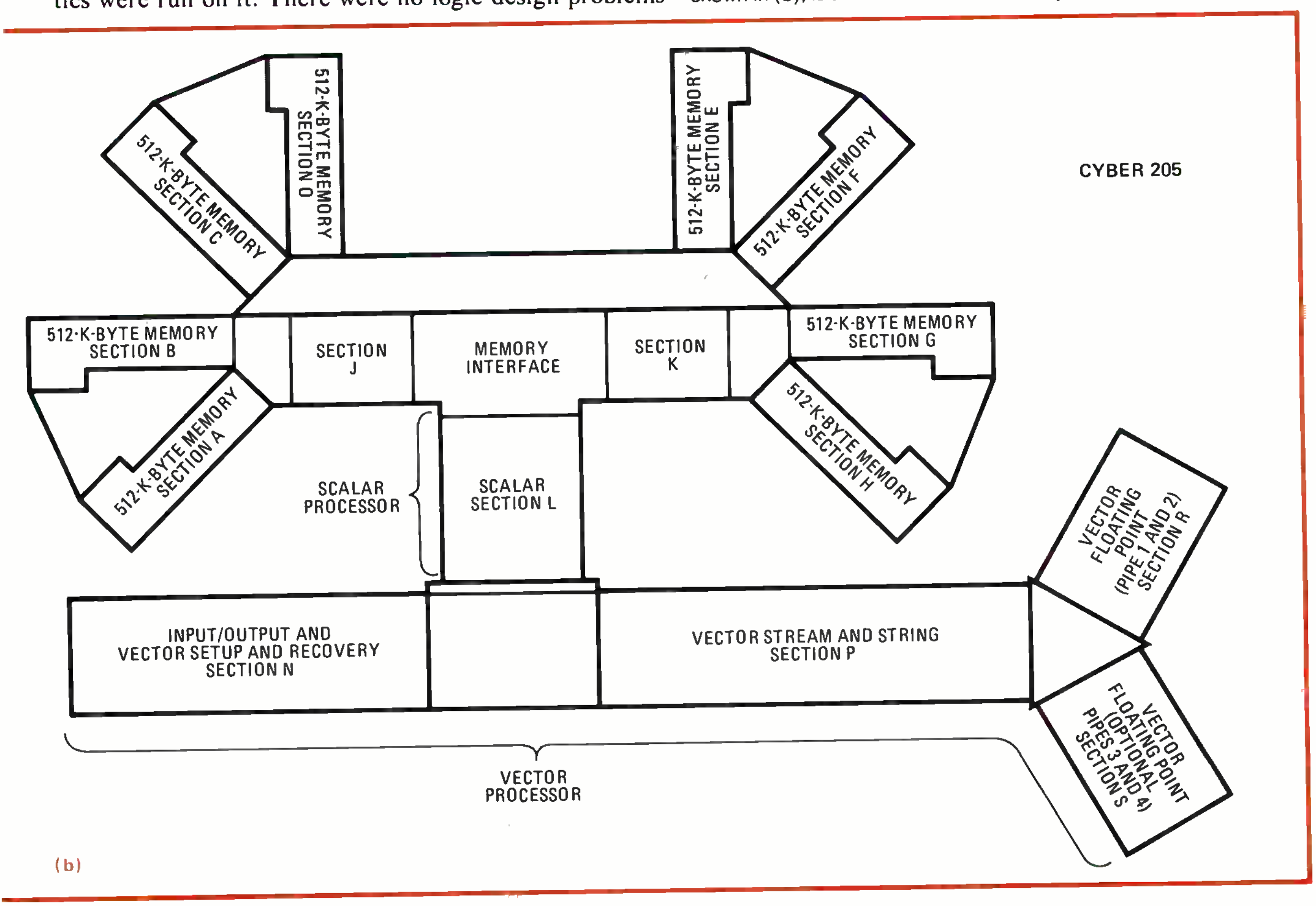
Before any design for the Cyber 205, with its up to 88 boards of large-scale integrated circuits and over 2 million ECL gates, was committed to hardware, instruction diagnostics were run in a simulation of the 205 using nominal circuit delays and worst-case delays of 15%. Then, when the hardware was built, these same diagnostics were run on it. There were no logic-design problems and only two small timing mishaps. Extensive measurements of circuit switching speeds and wire propagation delays proved that the simulation signals were within 10% of hardware signals. General-purpose system-simulator (GPSS) simulations of computing rates of 21 million floating-point operations (megaflops) for implicit code were within 5% of actual execution times. The central-processing-unit time required for each job in a typical mix of jobs in gate and block model verification are shown in the table on page 110.

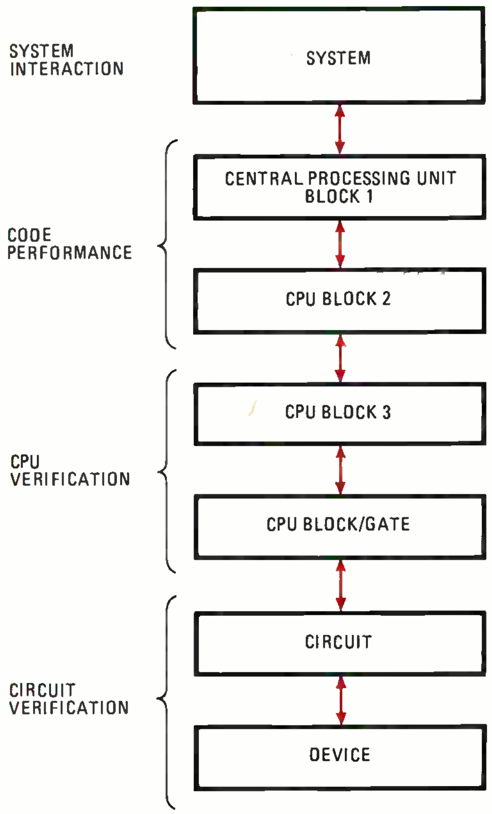
The bottom-up detailed verification process that designed the Cyber 205 yields a fully simulated design of a computing engine of known capability. It complements the GPSS simulation of real kernels of code in addition to ensuring the validity of high-level designs. Together, these tools create a hierarchical simulation-verification-manufacturing support facility that is essential for producing computers that push beyond the current standards and product limits.

Software supports simulation

Software for CAD includes an event-processing simulator permitting simulation speeds greater than 90,000 events per second. This speed was achieved, in part, by stressing no-frills simulation and down-playing functions

1. Fastest. The schematic diagram of the Cyber 205 central processing unit (a) shows both the scalar and vector processing units. The maximum configuration of the Cyber 205, whose physical layout is shown in (b), is three times faster than any other computer.





2. Thorough. The top-down–bottom-up flow of the computer-aided design and simulation used to design CDC supercomputers starts by simulating system interaction and proceeds through several levels to the devices. When the devices are designed, the process is reversed.

like automated placement, interactive display, rise- and fall-time analysis, and circuitry simulation.

The top-down simulator phase begins with two GPSS models (Fig. 2). In the study phase of the Cyber 205 development cycle, high-level plans were drawn up to match the processor's board requirements. The GPSS simulations tested the design balance to help ensure that it would meet Cyber 205 performance expectations.

At the same time, a detailed hardware design was started at the functional block level to shorten design time. When the top-down process reached the circuit verification level with detailed gate simulation, the process was reversed and became bottom-up verification.

Hardware design

Hardware design for the Cyber 205 includes three major categories: circuit design, board design, and logic verification. The first step was the design of a custom high-performance, two-input ECL AND gate. Diffusion masks were designed, geometries determined, and an analog model of the ECL gate was built. A complete ac and dc verification was performed on the AND gate design by using a network analysis program before the first gate-array IC was diffused in silicon.

Next, several hundred ECL cells were placed on 170-mil LSI chips and mounted in 52-pin packages. LSI part types were developed from a diffusion set by altering metalization layers. Metalization routing options for each logic function (AND and OR) built from the basic two-input AND gate were placed in a cell library.

When the Cyber 205 project began in 1978, CDC's CAD/CAM system included the following functions:

- Design verification (CAD)
  - Circuit verification
  - Algorithm verification
  - Board verification
  - Detailed design verification
    - Test Boolean implementation
    - Test for long/short paths, race conditions
    - Remove skew from data trunks
  - Tune clocks
  - Logic design verification
    - Gate-level simulation
    - Block-level simulation
    - Test cases
- Manufacturing process (CAM)
  - Data-base management
  - Manufacturing documentation
  - LSI circuit and board production
  - Engineering change orders
  - Testing and documentation

The CAD system maintains a library of logic macroinstructions, assists in the layout of metal patterns to produce custom arrays, provides output to simulation programs, and builds the tape for producing diffusion and metal masks (Fig. 3). Wire lists for each custom LSI part type, describing logic at the gate level, were directly generated from the metal-routing pattern file and simulated for final verification.

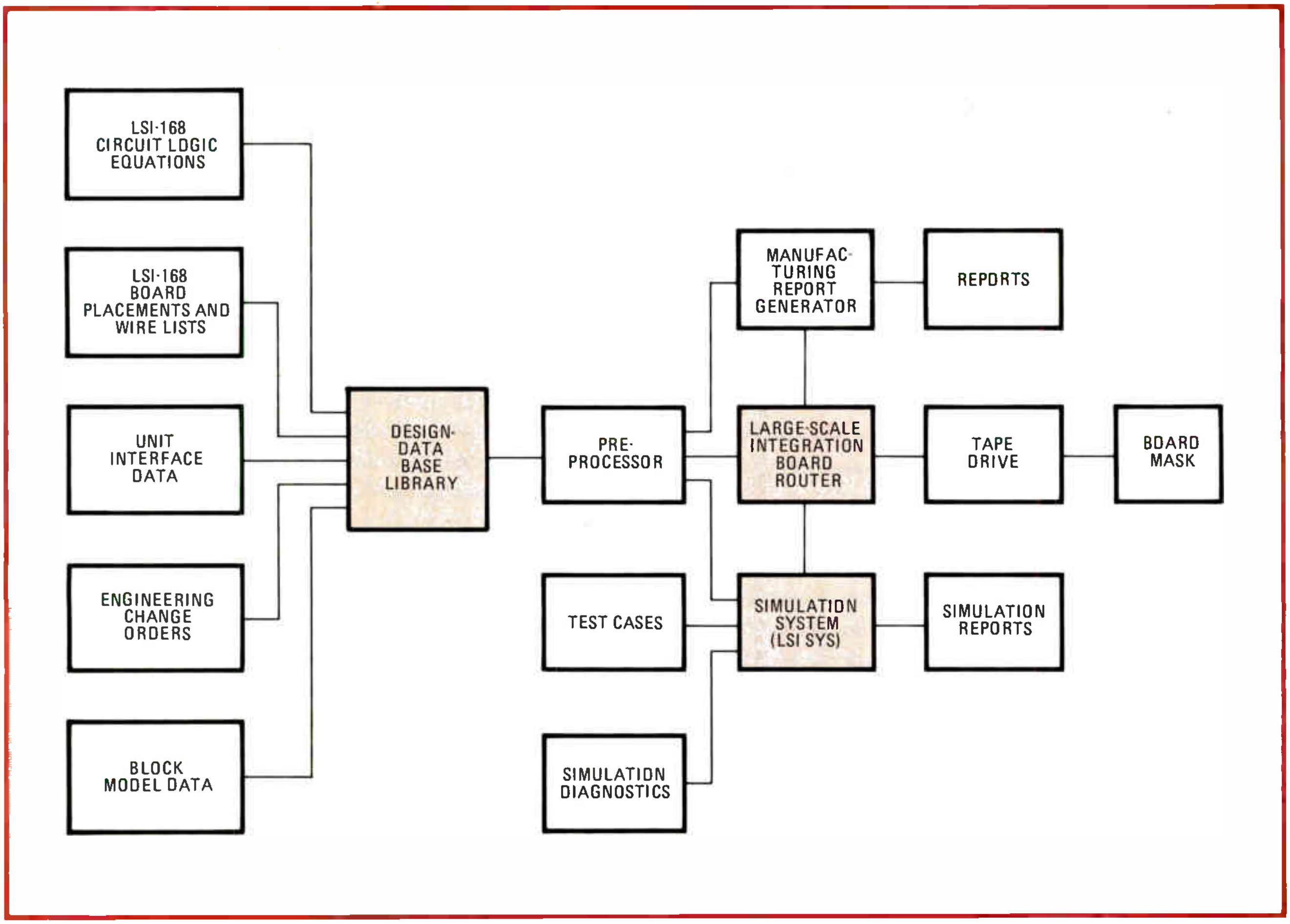
At this point, the top-down design from the GPSS system-level simulation, through functional block design, and down to the custom chip design had been completed. The design process then switched to a bottom-up approach with the layout of the circuit boards.

The boards were routed using board-routing software working from the stored wire lists describing the circuit interconnections. More complex board routing was optimized or completed through a terminal. The output from routing programs consists of wire lists and lengths for simulation and generation of board layout masks on a precision plotter.

The logic level

During the first phase of logic design for the Cyber 205, function diagrams are developed showing data flow throughout the computer at the fundamental clock cycle level, often called the minor cycle level—from registers through adders and shift networks and into registers. Control responsibility is also indicated for the direction of data flow. To make the overall design more manageable, logic is partitioned into functional units having one to eight LSI logic boards.

Minor cycle models developed for each fundamental unit became available for simulation long before detailed gate design was finished. A minor cycle model of the entire computer is simulated first at the individual instruction level and then by running diagnostic routines



3. Simulation power. Many simulations were possible because the simulation was done on a very fast Cyber 203. Several sources of input create the design data-base library feeding the CAD/CAM system that provides board-routing masks and manufacturing reports.

containing up to 1,000 instructions. As the detailed gate-level design became available, part of the computer was modeled at this level and part at the minor cycle level. Instructions were again simulated individually and through diagnostics.

Software represents hardware

A software model of logic design that closely approximates actual hardware is constructed from a set of predefined blocks interconnected with wire lists. A CAD system routine duplicates logic operation of each block at the interface pins.

The logic is simulated by propagating events, or signals, between blocks. An event is received by a block and processed by the routine describing the block type. Events are sometimes created by the model, and wire delays are sometimes not included in the interconnection lists.

Designers can define logic networks, specify starting conditions, and select the signals to be included in simulation reports. The simulator determines state changes and records event propagation throughout the network. As the simulator operates, it generates files, and from these files reports are produced. At the lowest level, gate models simulate ANDs, ORs, and latches built from ECL gates. Next, LSI models represent an entire circuit that is modeled at the package pins. Finally, function models simulate networks like registers, adders, and shifters.

The bottom-up simulation process, then, goes from a gate model of each LSI circuit type, described in wire lists defining the interconnection of gate functions on the circuit, to LSI circuits interconnected on logic boards, and hence to automatic routing of logic boards and determination of wire lengths. A pseudo-board router estimates wire lengths with an 80% accuracy, running in less than 20 seconds, and is used until the logic is completely simulated. Then an actual board router, taking typically 3,000 seconds of computer time to complete a board, provides the routing tapes for board fabrication.

To increase simulation speed and capacity, block models for 52-pin circuits sometimes replace gate models. However, with the circuits modeled at the package pin level, it is not possible to report on individual gates. The advantages of 52-pin circuit block modeling decreases in direct proportion to any increase in circuit complexity.

Simulated logic

Logic was functionally simulated at the minor cycle level before and during gate design, to verify data flow, minor cycle timing, and control equations. A set of predefined functional block models describing registers, adders, and combinational networks was interconnected with the aid of wire lists to represent a logic network. The functional models were placed on 150-location LSI

TABLE 1: CENTRAL-PROCESSING-UNIT TIMES FOR GATE AND BLOCK MODEL VERIFICATION JOBS

Job	Cyber 203 CPU time (s)
Circuit simulation	150
Single large-scale-integration board simulation	150
Data-base update	150
System-block model verification	1,200
Functional-unit gate tests	1,200
LSI board routing	3,000
Nominal-system-level mixed block and gate tests	3,000
Large-system-level block and gate testing	6,000

logic boards and occupied anywhere from one 52-pin location to as many as 99 locations.

The best way to simulate control functions is to use either microcode or programmable logic arrays. Control is typically defined in terms of Boolean equations or microcode. Control equations used during Cyber 205 simulation are loaded into a PLA function model and translated into signals. Microcode is loaded into a memory function and read out as address bits change. LSI logic boards containing functional models are wired by the same board router that interconnected LSI circuits; however, wire delays are set to zero since the timing could be designed using the microcode.

An accommodating design tool

The Cyber 203 system accommodates 15 to 20 designers running simulation jobs during a typical working day. Each designer normally makes a minimum of two runs a day and expects no worse than a 1-hour batch-mode turnaround. To support this activity, typical simulation jobs were limited to 15 minutes of Cyber 203 CPU execution time, and larger simulations were restricted to nonprime time. Computer utilization was approximately 60% to 80% throughout a 24-hour day.

Six programs make up the simulation system (LSISYS):

- BDIN—builds wire lists for board router.
- BDROUTE—routes LSI logic boards.
- BDCON—interconnects logic boards.
- BLDLSI—builds LSI simulation tables from wire lists.
- LSISIM—simulates all the different levels of design.
- DSPLY—displays simulation results.

Wire lists and placement descriptions serve as inputs to BDIN. For a typical simulation run, which includes running all the programs, execution time on the Cyber 203 is about 15 minutes. Such a run involves changing several dozen interconnect wires and printing out a listing of simulation results.

The simulation program, LSISIM, is the event processor handling approximately 90,000 events per second. Simulation of a dozen operations through a four-board floating-point pipeline arithmetic unit, capable of performing 64-bit additions or multiplications every 20 nanoseconds, generated approximately 6 million events. That job ran in 250 seconds, about 100 of which were used for event processing.

LSISYS block model subroutines were specifically designed and coded to conserve memory space, and memory was also conserved by carefully designing the event-processing algorithm. Processing speed is enhanced by restricting the use of branches, by eliminating many Fortran IF and GOTO statements, and by restricting the number of processing steps associated with events. Both these factors—memory conservation and speed—combined for high performance.

Functional simulation is approximately 12 times faster than gate simulation. A 200-instruction diagnostic program for the 88-board Cyber 205 requires approximately 10 minutes of Cyber 203 CPU time, running with a minor cycle functional model. Simulating with a gate model requires one hour. Typically, diagnostics were run with several logic board models at the gate level and the remainder models at the minor cycle functional level.

Events are stored in a 32-K-byte memory, two events per word. The memory was divided into 1,024 sections, or buckets, with each bucket containing 32 words. The buckets were chained together to form an events list. Events occurring at the same sample time were allocated to the same bucket or series of chained buckets. Seventy-five percent of the allocated buckets were completely full during a typical run.

Solves current mysteries

The Cyber 205 does much more than advance the state of the computing art: it helps to solve problems that are currently beyond an effective solution. CDC's analyses show there is a market for at least 100 Cyber 205-type supercomputers.

In petroleum exploration and recovery, the Cyber 205 is expected to allow three-dimensional studies of oil fields where only two-dimensional analyses are currently possible. In doing so, it can help to minimize the false images that fool geologists into believing oil is present where none exists, retrieve remaining oil from an existing reservoir, and find hidden oil pockets.

In studies of nuclear reactors, the Cyber 205 is expected to handle realistic, three-dimensional analyses of a reactor's entire core in eight hours or less—studies that cannot be cost-effectively performed on prior supercomputers. By 1985 it should be able to troubleshoot on line so an operator who spots an unfamiliar problem on a nuclear reactor console can hook into a remote Cyber 205, input the problem's characteristics, and get a swift reply that should provide an answer to the problem.

The extremely big computing system has a key role to play in weather forecasting; in analyses of earth photographs taken from satellites; in large-scale CAD/CAM systems; and in other applications.

Semiconductor technology continues to advance, supporting supercomputer development. However, these technology advances in integrated circuits by themselves are no longer enough. Over the past decade the CAD/CAM system at CDC has evolved until it has become as essential as circuit technology to further progress in developing supercomputers beyond the upper limits of performance. Right now, the CAD/CAM system, up and running on the Cyber 205 computer, is developing the Cyber 205's successor. □

New process boosts current levels of monolithic voltage regulator

Bipolar IC borrows power npn structure from discrete technology to handle currents of 10 A plus

by Carl Nelson, *National Semiconductor Corp., Santa Clara, Calif.*

☐ Long dominant in low-current applications, monolithic linear regulators are ready to take on high-current uses. By combining discrete-device techniques with conventional bipolar integrated-circuit technology, National Semiconductor Corp. has developed a process called Moose that overcomes several limitations of single-chip power-handling circuits, accommodating unprecedented current levels of 10 amperes and up.

Yet the resulting high-current regulators are as easy to use as their lower-current brethren, and their improved performance can be strengthened even more with some simple design twists. They also make possible better paralleling techniques, and a version that offers two more pins than the standard model lends itself to a design scheme that boosts efficiency.

Until recently, no unduly difficult engineering problems cropped up as current levels increased. Die sizes were simply scaled upwards, roughly doubling every four years, as it became clear that there were applications for monolithic regulators as large as the semiconductor manufacturers could make. Now, at the 5-A level, certain limitations come into play, and process innovations are required to further increase power levels.

Bonding limit

One constraint is that the current-handling capability of a monolithic regulator is limited by the number of bonding wires used. For example, a standard 3-mil aluminum bonding wire can carry only 1.5 A, so 14 bonds would be required for a 10-A regulator—seven each for the input and the output. All seven related bonds must be attached to the same pin, making assembly quite difficult. Reliability can suffer as a consequence.

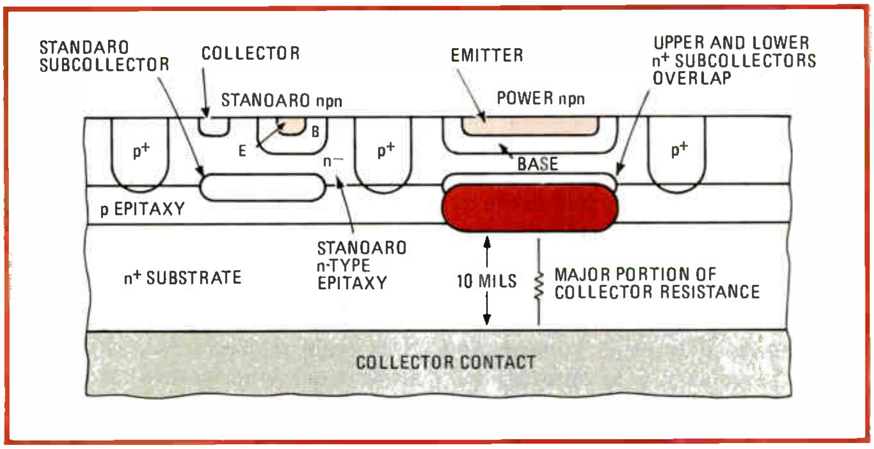
On the other hand, reducing the bond count by increasing the wire size imposes another limitation: each bond is collecting current from a larger interdigitated structure of emitters and collectors. As the area of this interdigitated structure increases, the size of its metal interconnects grows quickly out of hand. A standard 2-micrometer-thick aluminum layer can reliably carry about 0.1 A per mil of width, so a 10-A line would need to be 100 mils wide—a dimension comparable to the total die size.

Ohmic losses

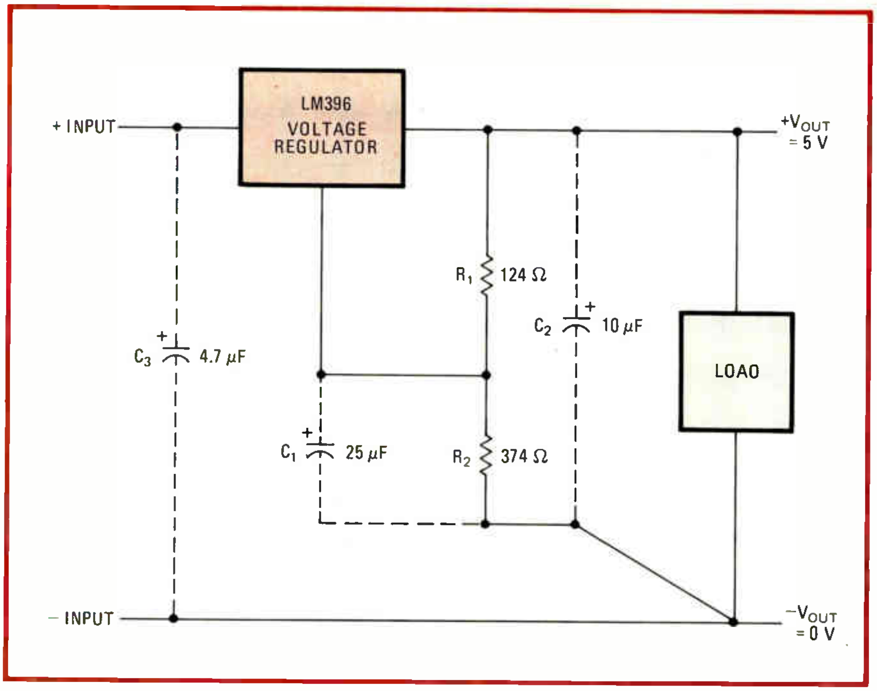
A second limitation at high current levels is voltage drops across these relatively thin 2-μm aluminum interconnections. Unequal losses cause current crowding and generate hot spots. Even the balanced losses get so high at 2.5 A per bonding wire that these losses make a standard IC structure not feasible. A typical loss might be 0.5 volts at 10 A, or 5 watts lost just in the metal. Widening the interconnections enough to solve that problem again wastes silicon because the area under the metal cannot be utilized.

The Moose process [*Electronics*, Nov. 20, 1980, p. 40] solves these problems by using a structure that is similar to that in discrete power transistors yet that can be realized in standard bipolar IC technology. An extra mask level is added to the standard npn process to allow formation of a lower subcollector connecting the power transistor's collector with the heavily doped n^+ substrate (Fig. 1). The standard npn devices are still isolated by the p-type epitaxial layer and the p^+ diffusion pockets.

Connection to the power transistor is made through the bottom of the chip, eliminating the area-consuming metal interconnects. Furthermore, the collector satura-



1. Inside Moose. A voltage regulator made with a new bipolar process has a power npn structure akin to discrete circuitry. The collector has low resistance and is contacted through the substrate, simplifying bonding.



2. Typical application. For this 5-V, 10-A regulator, precison resistors R_1 and R_2 provide a 1.25-V reference from the 5-V output. The optional bypass capacitor C_1 improves rejection of noise and ripple.

SPECIFICATIONS OF THE LM396 REGULATOR	
Output voltage (V)	1.2 – 15
Output current (A)	0.01 – 10
Load regulation (%/A)	0.07
Line regulation (%/V)	0.005
Temperature coefficient of output voltage (%/°C)	0.003
Reference voltage tolerance (±%)	2

tion resistance is much lower than that in any standard power IC structure, since the collector current flows through only heavily doped regions. The process thus improves specifications and reliability, at the expense of slightly more complicated fabrication.

New regulator

The first product using Moose processing is the LM396: a 10-A, 70-W adjustable positive-voltage linear regulator. It incorporates all the protection features of the lower-current LM317 and LM350, including current limiting, power limiting, and thermal shutdown.

The package is a standard three-lead TO-3 case, but with thicker 0.06-inch pins that retain good load regulation. The extra-thick pins are not necessary on parts like the 317 where the case is used as the output. In the 396, the case must be used as the input because the collector contact—the input to the regulator—is the back of the die, which is electrically tied to the case.

The 396 is simple to use and, because it is adjustable, will satisfy a wide range of output voltage requirements: 1.2 to 15 V. Its internal voltage reference has been pretrimmed so that precision external resistors accurately determine the output voltage, and no external trimming is necessary. The internal trim also reduces the typical output voltage temperature drift to 0.003%, or 30 parts per million, per °C.

As Fig. 2 shows, the new regulator is as easy to use in a typical voltage regulation circuit as its lower-current predecessors. R_1 and R_2, which set the output voltage, should be 1% (or better) metal-film or wirewound types that track each other's temperature coefficient to 30 ppm/°C or better to take advantage of the low output tempco of the LM396. If a low temperature coefficient of the output voltage is not critical, the tight tracking is not necessary; however, carbon resistors should never be used because of their poor long-term stability.

C_1 is an optional bypass capacitor that if used will improve noise and ripple rejection. The improvement is the ratio of output voltage to reference voltage—5:1.25 in this 5-V application. Also, C_2 is optional, but it improves high-frequency output impedance and should be located close to the regulator. Additional capacitors may be inserted close to the load as needed for local bypassing. C_3 is necessary only if the main filter capacitor is more than 6 in. away from the regulator.

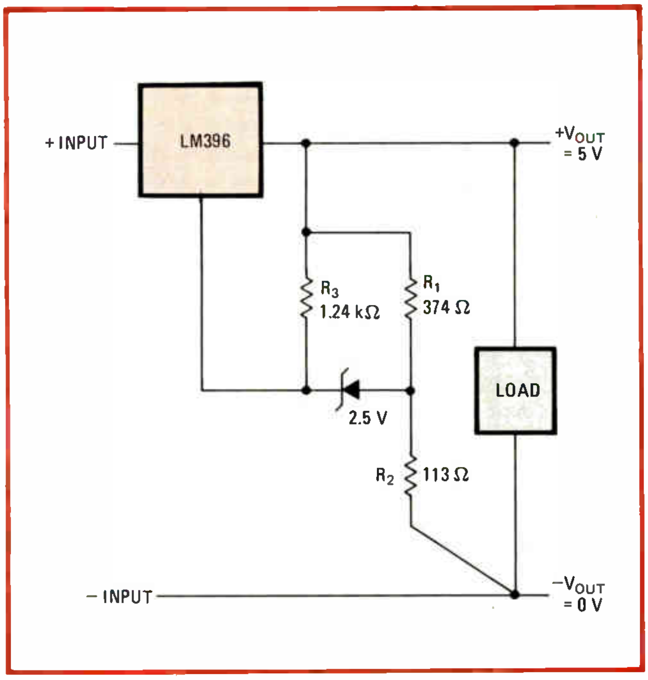
It is not possible to provide full remote sensing in a three-terminal regulator because only one pin is available for sensing. It is used for negative side sensing: one end of R_2 is simply tied to the load separately from the V^- power bus.

The positive output, however, is sensed only at the output pin itself. This is an important consideration for high-current regulators, because the output impedance and load regulation are determined by the resistance of the wire connecting the output to the load.

For best regulation, the top of R_1 should tie directly to the output pin of the regulator. If it were tied to the load, regulation would degrade by the ratio of the output voltage to the reference voltage—4:1 in this example. A fairly heavy wire should connect the regulator to the load; even No. 16 AWG wire has a 40-millivolt drop per foot when carrying 10 A.

Improving performance

The specifications for load regulation, line regulation, and thermal regulation for the 396 are expressed as percentages (see table) because the absolute values of these parameters scale directly with the output voltage. This is a direct result of the resistor divider that sets the output voltage. Significant improvements in these parameters can be made by adding an external reference in series with the adjustment pin of the regulator. This move reduces the resistor ratio required to set the output voltage. For example, a 3:1 improvement is realized by adding a 2.5-V reference diode to this circuit (Fig. 3). R_3



3. Better performance. To enhance line, load, and temperature regulation, an added reference diode reduces the voltage-divider ratio that is required between the output and reference. This improves the specifications by a factor of 3.

establishes a 1-milliampere operating current for the reference diode.

The 396 also lends itself to more efficient implementation of paralleling. Users of three-terminal regulators often try to parallel devices for higher output current, but this practice is generally not recommended by manufacturers because the regulators will not share currents equally. Some will run in a current-limit mode, at two to three times their normal rated current, while others in the parallel group will be idle.

A parallel scheme

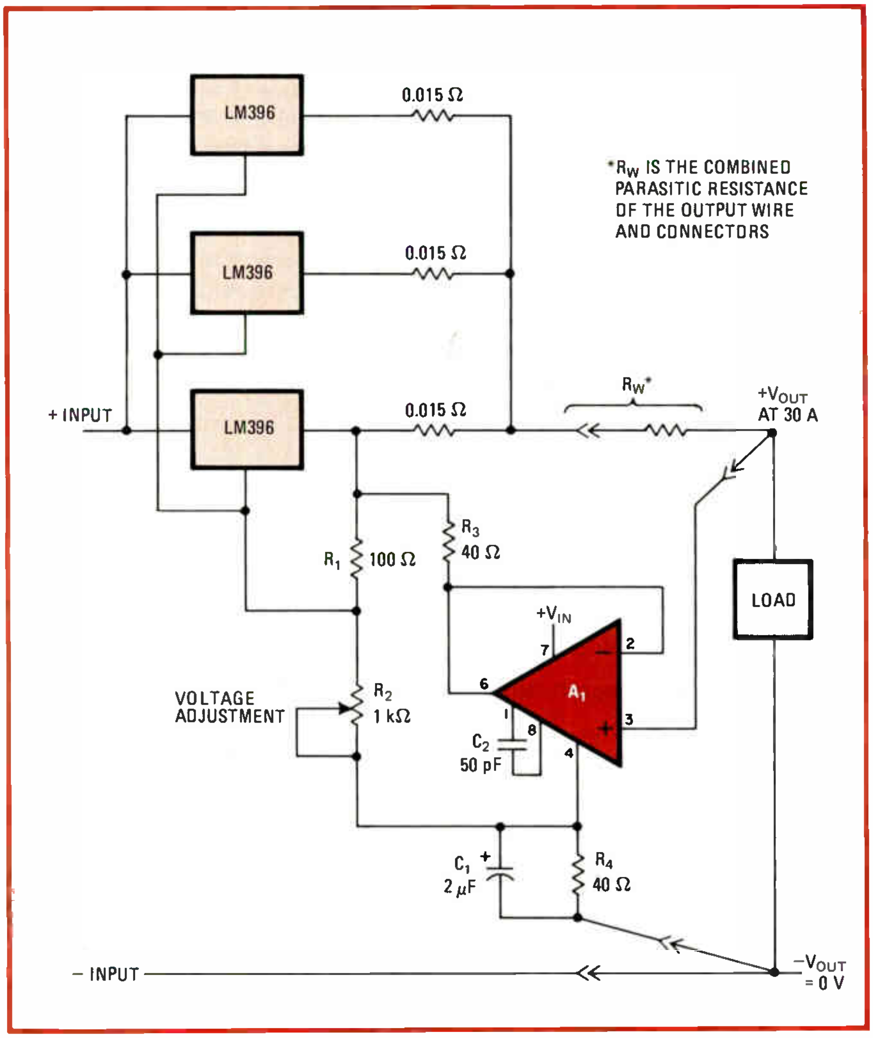
The problem is that each regulator inherently has a slightly different output voltage in independent operation; yet they are being forced to the same level by the parallel connection. Thus the regulator with the highest output voltage supplies all of the load current until it limits current. At this point, the output of the parallel regulators drops from the highest output voltage in the group to the second highest, where it stays until the second regulator limits current.

This setup gives poor overall load regulation and an extremely high output impedance at the transition points where one regulator limits current and the next takes over. Operation at or near these points will cause very high noise, ripple, and load crosstalk.

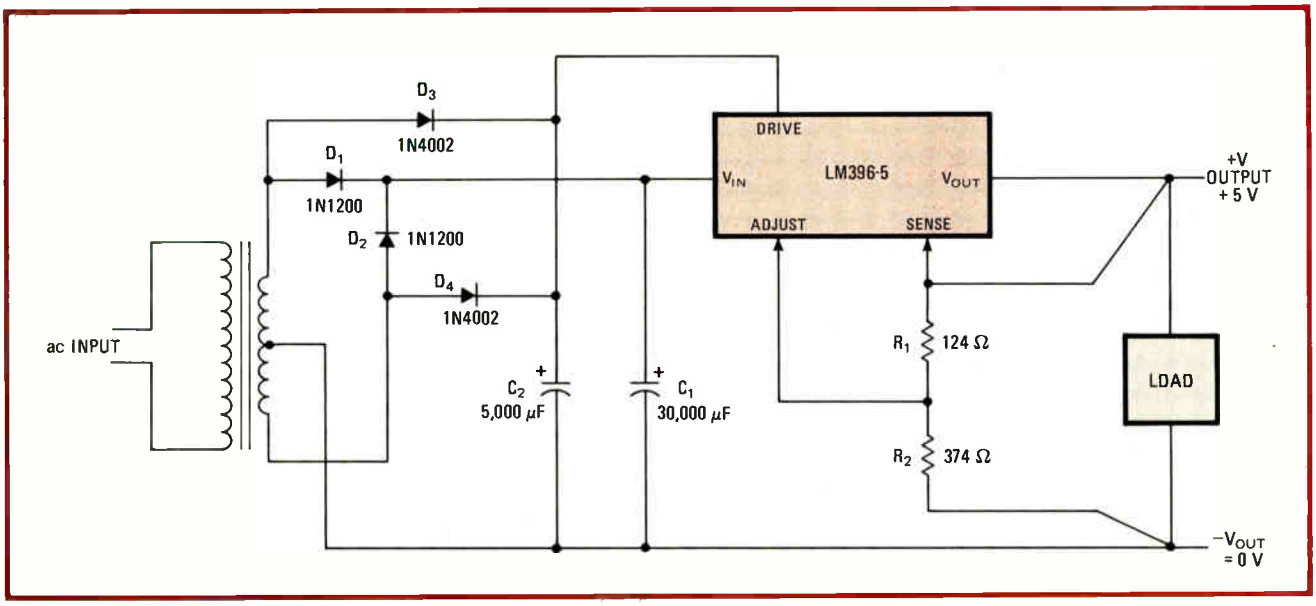
Two methods can solve the current sharing problem, but not without some undesirable side effects. Inserting ballast resistors in series with each output solves the sharing problem, but also further degrades load regulation. Adding current-sensing resistors at each input plus one operational amplifier for each regulator provides equal current sharing with no load-regulation or impedance problems, but at the cost of additional parts and an added negative supply for the op amps.

A new technique for paralleling that combines those two methods has been developed for the 396 and is also applicable to other three-terminal adjustable regulators. It is illustrated in Fig. 4, where a single op amp, A_1, drives three regulators.

A_1 senses the voltage difference between the first regulator output and the load. This voltage is forced across R_3, and the resulting current flows into the output of A_1 and out of its V^- terminal through R_4. The



4. Moose herd. A new scheme for paralleling regulators to multiply current capability uses an op-amp driver. Small sharing resistors prevent saturation of the regulators. This technique combines two earlier schemes, overcoming their assorted drawbacks.



5. Efficient. A five-terminal version of the LM396 can improve efficiency. The drive pin supplies extra voltage to the control circuitry at 1.5 V above the input level. The pass transistor saturates, reducing dropout, so the input voltage can be reduced by a like amount.

resulting voltage drop across R_4 raises the regulator output just the right amount to keep the output voltage at the load constant, independently of the load current.

The ballast resistors can be as low as 0.015 ohm each because of the tight tolerance of the reference voltage on the 396—so they do not degrade efficiency. What's more, they make it possible for a single op amp to serve all the regulators. No additional negative supply is needed because the op amp's output is always at a level well above ground.

Five-pin version

The loop works independently of the actual values of the ballast resistors and of R_w (the combined parasitic resistance of the output wire and connectors), as long as the voltage drop across these resistances does not get so high that A_1 limits current when trying to drive R_3. It also works independently of the value of R_1 and R_2, so that the regulator can still have an adjustable output (down to 3 V).

A second version of the LM396 in a five-pin TO-3 package improves on the three-terminal part. Load regulation is specified five times more tightly than in the three-lead part: typically 0.05% at 10 A. One of the added pins is used for positive-side sensing of the output, and the other provides the control circuitry's supply voltage. It can be used to gain significant improvements in the regulator's efficiency.

The efficiency of linear regulators is receiving more and more attention as energy costs rise. A typical 5-V linear regulator has an efficiency of 50% to 60% as compared with 80% to 90% for switching regulators.

More efficient

The critical specification for linear regulators is the minimum input/output voltage differential, or dropout voltage, which is the lowest voltage between input and output that still maintains regulation. For monolithic regulators, this is typically 2 to 3 V at full load. Allowing for low line voltage and filter-capacitor ripple adds an extra 2 to 3 V, so a 5-V regulator typically needs a 9-to-10-V input voltage, yielding 50% to 55% efficiency.

With the five-lead LM396-5, this efficiency can rise to around 65% by using it in the circuit shown in Fig. 5. The drive pin, which provides power to the control circuitry and driver transistor, is held 1.5 V higher than the power input, so that the pass transistor is operating in saturation. In this case, the dropout voltage is reduced to near zero at low currents and to about 1 V at 10 A.

At first glance, it would seem that the voltage on the drive pin is the same as that on the input, but closer inspection reveals that under heavy load conditions, the voltage on C_2 is indeed 1.5 V higher than on C_1. This occurs because of differences in the peak forward voltage of the diodes (0.8 V as against 1.2 V) and in the ripple voltages on C_2 and C_1 (0.1 V versus 1.2 V).

The 1.5-V higher drive-pin voltage allows a reduction in the raw supply voltage for the regulator by 1.5 V, raising efficiency from 55% to 65%. Equally important, the power loss in the regulator drops from 40 to 25 W—a 40% decrease. This drop allows smaller heat sinks or considerably reduced operating temperatures.

Moose futures

Now that the major monolithic die limitations due to circuit topology and efficiency have been overcome, high-current ICs will be developed for many new areas of application. They might include switching regulators, buffer amplifiers, and solenoid drivers.

How high will current and power levels go? Five amperes per bonding wire is a reasonable limit for Moose geometries, and up to six bonds could be used with special posts; therefore, 30-A devices are feasible. Power limitations, however, are a different matter: the standard steel TO-3 case is good only up to 100 W. A solid copper TO-3 can handle 200 W, but for greater power levels, a new multipin power package must be developed. □

Designer's casebook

FSK transmitter uses two gated oscillators

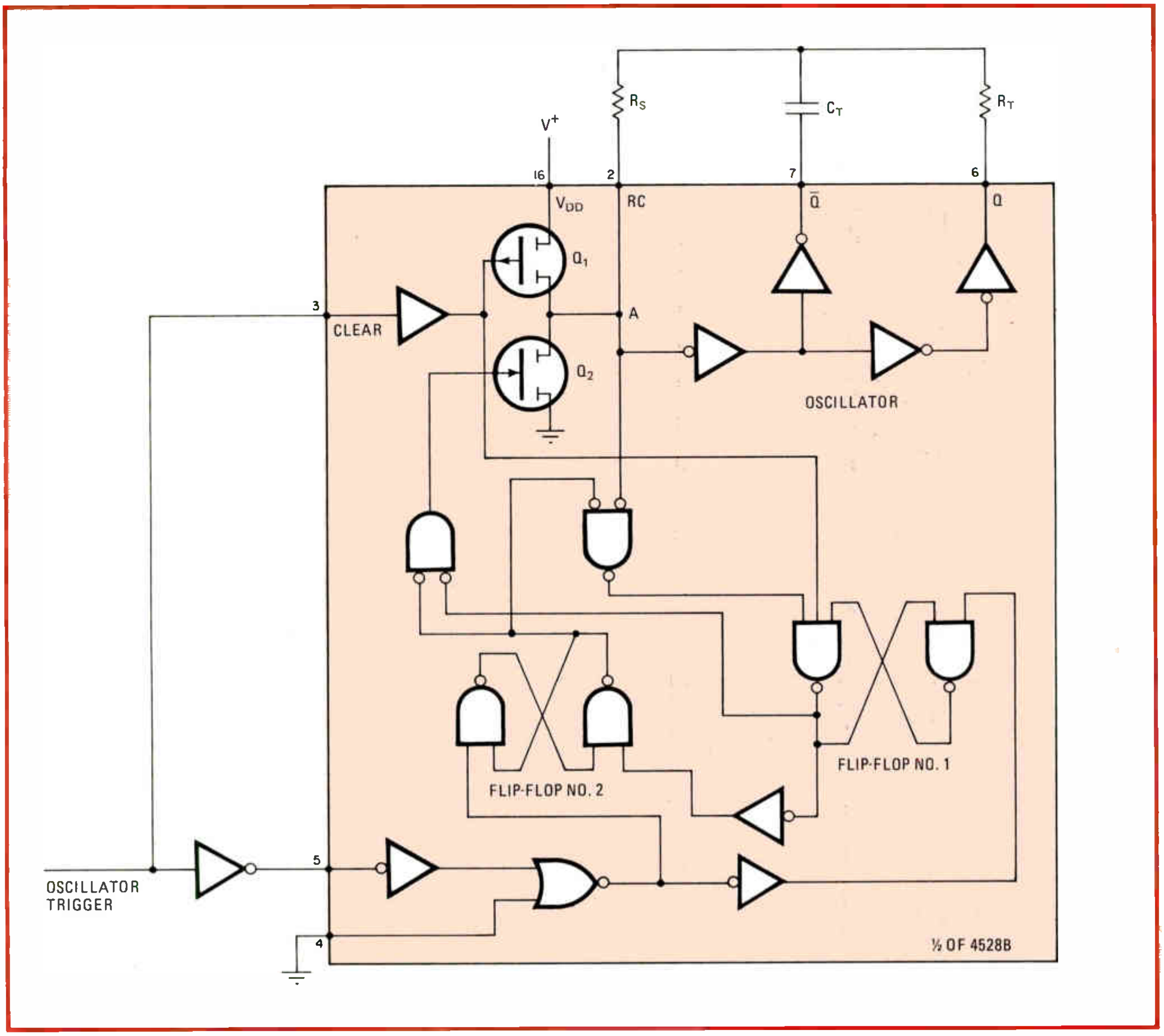
by Akavia Kaniel
Measurex Corp., Cupertino, Calif.

The 4528B complementary-MOS dual monostable multivibrator can operate as a frequency-shift–keyed (FSK) transmitter. Each half of the chip, shown in Fig. 1, is used here as a gated oscillator and is activated either when a mark or a space frequency is to be transmitted.

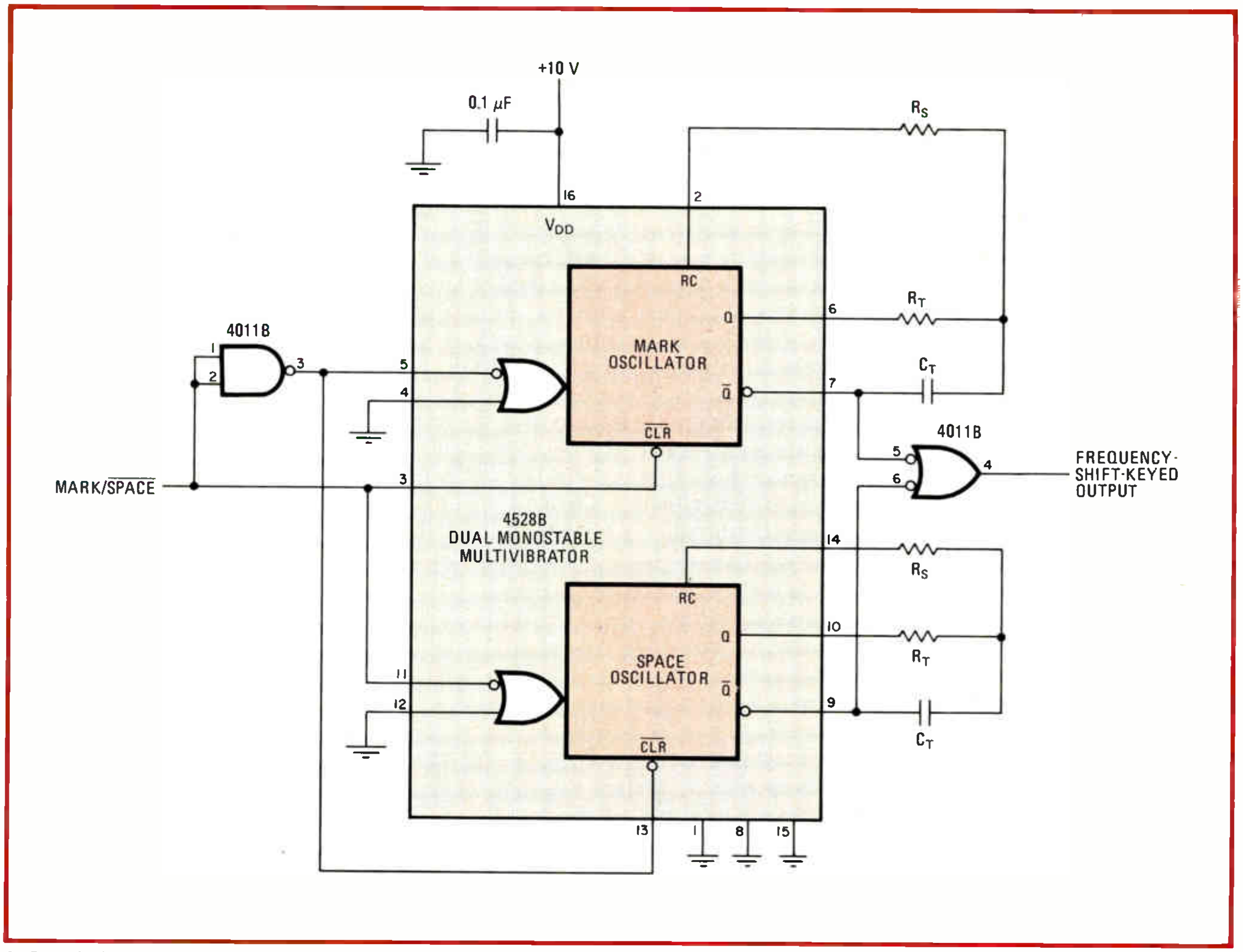
As long as the input signal to the clear input (CLR pin 3) is present, transistor Q_1 is turned on and the oscillator will not oscillate. Once the CLR pin is pulled high, however, Q_1 turns off and the outputs of flip-flops No. 1 and 2 turn low. Transistor Q_2 turns on for an instant, triggering the self-starting oscillator. At the same time flip-flop No. 1 senses that point A, shown in Fig. 1, has gone low and turns Q_2 off.

With Q_1 and Q_2 off, the oscillator runs at a frequency determined by resistor R_T and capacitor C_T and is given by the expression: $F = 1/(2.3 \times R_T \times C_T)$ for 1 kilohertz $\leq F \leq 100$ kHz, where $R_S \approx 2 \times R_T$.

When the CLR input is pulled low, Q_1 turns on and the oscillation stops. The complete FSK transmitter circuit is



1. Shifty. The core of the frequency-shift–keyed transmitter is a gated oscillator, which is controlled by a signal present at the clear (CLR) pin. The full circuit uses two such oscillators—one for a mark and another for a space—contained in a 4528 dual one-shot package.



2. Coupled. A complete frequency-shift-keyed transmitter is formed by coupling the outputs from both monostable multivibrators through a dual-input NAND gate, as shown here. Mark and space frequencies are fixed by R_T and C_T, where $R_S = 2R_T$.

shown in Fig. 2. It is formed by coupling both oscillator outputs. When the mark-to-space control input goes high, the mark oscillator signal appears at the FSK output, and when the same line is low, the space oscillator signal appears at the FSK output. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $75 for each item published.

Simple sound generator takes orders from microcomputer

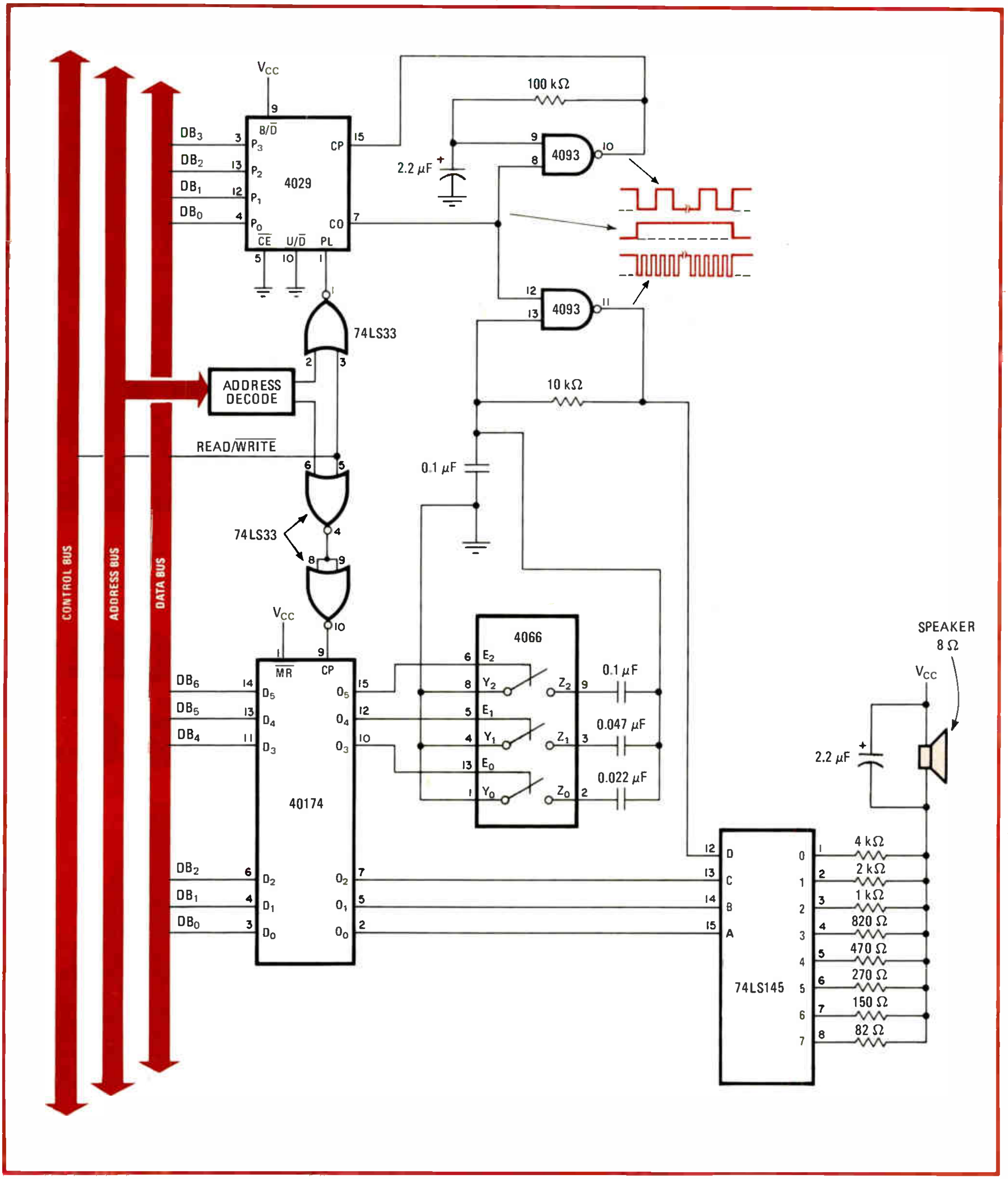
by Joseph Huijts
Waalre, the Netherlands

Only six integrated circuits are required to build this low-cost programmable sound generator. The circuit, as shown in the figure, permits a choice of 8 different levels of loudness, 16 time durations, and 8 frequencies (they are not related to musical intervals).

In operation, 2 bytes of data are sent from a microcomputer to this circuit, which produces a tone. The duration is programmable; thus no action from the microcomputer is required to end the tone.

The first byte is sent to a 40174 hex D-type flip-flop, to control frequency and loudness. The second byte is sent to a 4029 binary/decade counter with the ability to load data in parallel. The least significant nibble is loaded into the counter enabling an oscillator circuit—a NAND Schmitt trigger with RC feedback. This oscillator causes the counter to decrement until it is inhibited by the final count indicated by the CARRY OUT pin going to a logic 0. The time span that is produced depends on both the oscillator frequency (about 10 hertz) and the nibble that is loaded into the counter. In this way 16 different time spans can be selected from 0 to 1.5 seconds in 0.1 second steps.

The final count output also controls a second oscillator, producing the output tone. The frequency is controlled by the R and C values of the feedback circuit. The capacitor can be paralleled by a programmable combination of other capacitors with three bilateral analog switches like those used in a 4066, set by the most significant nibble of the 40174 hex dual flip-flop. The frequency can be adjusted between 700 and 2,300 Hz. The least significant nibble controls the loudness in eight 5-dB steps with a 74LS145 binary-coded-decimal–to–decimal decoder-driver. The sound-producing frequency is connected to the D input of the 74LS145, selecting outputs 0–7 when low or outputs 8 and 9 (not connected) when high. The A, B and C inputs—controlled by the least significant nibble—select a resistor to feed the loudspeaker. A 2-microfarad tantalum capacitor rounds the edges of the generated square wave. □



Sound off. Programmable sound generation under microcomputer control is achieved by decoding information on the address bus. This decoding directs frequency and loudness information bytes to the 40174 hex flip-flop and duration information bytes into the 4029 counter.

Bringing virtual memory to microsystems

Tailored for such schemes, the Z8003 works with a memory-management IC for faster, simpler implementation of segmented or paged virtual memories

by John Callahan, C. N. Patel, and David Stevenson
Zilog Inc., Cupertino, Calif.

☐ The capabilities of the newest microprocessors and their support chips are making virtual memory management possible at the microsystem level. Virtual memory management can be a boon for the applications programmer because it automatically maps a large logical address space onto a smaller main memory and a large secondary memory—but it can be a mixed blessing for the system designer to implement.

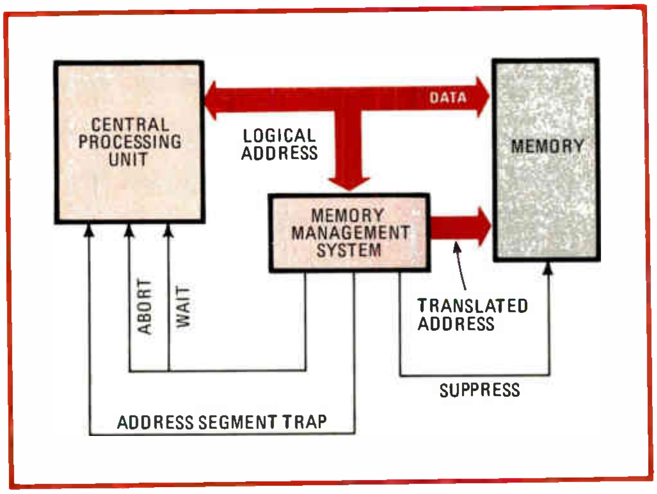
Support of virtual memory management complicates the host computer's operating system, which must swap the program and data fragments into and out of main memory, but the rewards of automatic memory management can be worth the additional complexity for many applications. To support virtual memory design, Zilog is adding hardware support of virtual memory schemes to its line of Z8000 microprocessors.

The Z8003 16-bit processor is pin- and instruction-compatible with the Z8001, but it adds an instruction-abort mechanism that aids in the construction of economical virtual memory schemes. With the associated memory-management chips, it can be used in systems (Fig. 1) that support either of the popular virtual memory schemes: segments of variable sizes or pages of a fixed size. It also facilitates the implementation of multiprocessor systems with a special status signal that aids synchronizing access to common resources.

The instruction-abort feature of the Z8003 is a vital part of solving the major problem in implementing virtual memory management—handling instructions that attempt to access locations resident outside main memory. In this case the processor must be halted, the desired information swapped into main memory from secondary storage, and the instruction retried.

The interrupt pin on standard microprocessors like the Z8001 is unsuitable for halting the processor in this context, since it is checked only after the current instruction has executed. But this check will often occur too late, since during the instructions faulty execution registers may be overwritten with nonsense, resulting in an uncorrectable error.

To fix this, the Z8003—at first called the Z9000



1. Virtual partners. Working with a memory-management chip, the Z8003 processor can implement a virtual memory setup. It includes an instruction-abort pin that facilitates the swapping-in of missing data or instructions to main memory from secondary storage.

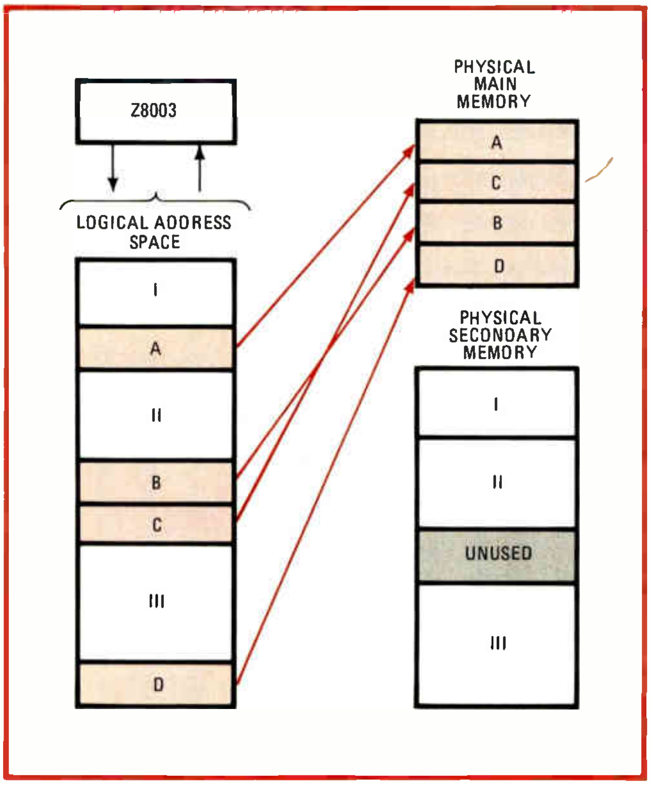
[*Electronics*, Oct. 23, 1980, p. 41]—includes a pin located at the Z8001's reserved pin 33 that lets the processor be interrupted during execution. This new function leaves the processor in a well-defined state that allows software to recover from the aborted instruction. Software can then swap in the missing data or instructions automatically, without operator intervention and without the need for special code in the program.

Managing a hierarchy

Facilitating this swapping action is the key to implementing the storage hierarchy of a virtual memory, in which fast, but expensive, random-access main memory is supplanted by slower, but cheaper, storage like disks or tapes or bubble memories. This hierarchy can reduce hardware costs by accommodating very large programs and data sets in the secondary memory and moving them block by block to the main memory for execution.

However, managing the use of the memory hierarchy can be a considerable problem. It all boils down to determining what information should be in main memory at a given time.

The early solution for system designers was to use the technique of overlays—dividing a program and its data into logically coherent units (such as subroutines or records) and moving them in and out of main memory with software provided by the applications programmer. The major disadvantage of this scheme is the difficulty of tracing all control paths through a program and of laying out memory for efficient use.



2. Logical mix. In a virtual memory system, the processor sees all its memory resources in a single logical address space, but only some portion of those resources physically resides in the main memory. Segments I, II, and III must be swapped in for use.

To complicate matters further, code usually had to reside in the same location whenever it was present in main memory. The result was that overlays could be difficult to construct and prone to subtle runtime errors, as well as being a time-consuming programming task.

A better solution is to automate this memory management task, resulting in a virtual memory system. It presents a programmer with a large, homogeneous logical address space of differing memory types, rather than with a large, heterogeneous physical address space.

In order to use a Z8003-based virtual memory management system, the programmer merely partitions the program and data into segments of whatever size is most convenient. The operating system may then automatically further partition the segments into fixed-size pages—in other words, a paged virtual memory is a variant of the segmented scheme.

As a program executes, unneeded portions of its code and data reside in the secondary memory, while the information most likely to be accessed is maintained automatically in main memory. When the program generates a logical address, the memory management system automatically translates it into a physical main-memory location. If the information is not in main memory, the processor is temporarily halted, the program suspended, and operating system software invoked to swap the desired information from secondary memory into main memory. After an updating of the translation mechanism, the program is restarted by reexecuting the uncompleted instruction.

Invisible mapping

As an example of such a setup, Fig. 2 shows a large logical address space, with only a portion of the locations accessible to the program actually residing in main memory. If the program generates an address in areas A, B, C, or D, the memory management system instantaneously maps the logical address into the appropriate main memory location. If, however, the program generates an address in areas I, II, or III, the instruction must be aborted and software invoked to swap out some data or instructions in main memory and swap in the required data from the secondary memory. With the new data in memory, the original program may reexecute the aborted instruction and proceed as if nothing unusual had happened.

Here the applications programmer is not involved with anticipating the need for new information as the program executes or with handling the transfer. Even more importantly, he or she need not know the memory characteristics of the system on which the programs will run. Freeing applications from limits on memory size greatly enhances the utility and portability of large, complex programs among different system configurations, regardless of their main-memory sizes.

The Z8003 generates segmented logical addresses—23 bits divided into a 7-bit segment number and a 16-bit offset—allowing external circuitry (becoming available as special-purpose integrated circuits) to implement virtual memory with variable-sized segments or with fixed-sized pages. So the choice of which type to implement is up to the system designer.

In order to fetch information at a given logical address in a segmented virtual memory, the entire segment containing that address must be in main memory before the program may continue executing. The Z8003 accommodates 128 segments that can hold between 256 bytes and 64-K bytes each.

In a paged virtual memory, each segment is subdivided into fixed-size pages (2-K bytes is a typical size). When information is fetched at a given logical address, only the page containing that address must be in main memory before a program may continue executing.

There are a number of tradeoffs between a segmented and a paged virtual memory. These will play an important part in the designer's choice.

For the Z8003, the software required to recover from an address translation failure is simpler and more efficient for the segmented virtual memory since fewer instructions require fix-ups before backing up the program counter. Also, the system tables indicating the location of logical segments in main or secondary memory are considerably smaller than those indicating the location of logical pages, since there are typically many more pages than segments.

But since segments are larger than pages, virtual memories in which the segments are divided into pages require less information to be transferred between main memory and secondary storage with each address translation failure. Thus they give better response time and throughput in multiuser systems. On the other hand, pages are usually larger than the minimum increment for segments (2 K versus 256 bytes), so the last page of a segment usually has unused space.

On the plus side, the fixed page size simplifies the allocation of the physical memory. In a segmented memory with its variable sizes, segments may have to be moved around in order to create a contiguous block of main memory large enough to hold an incoming segment. The single size of a page automatically creates contiguous blocks of the proper size in the main memory.

Software support

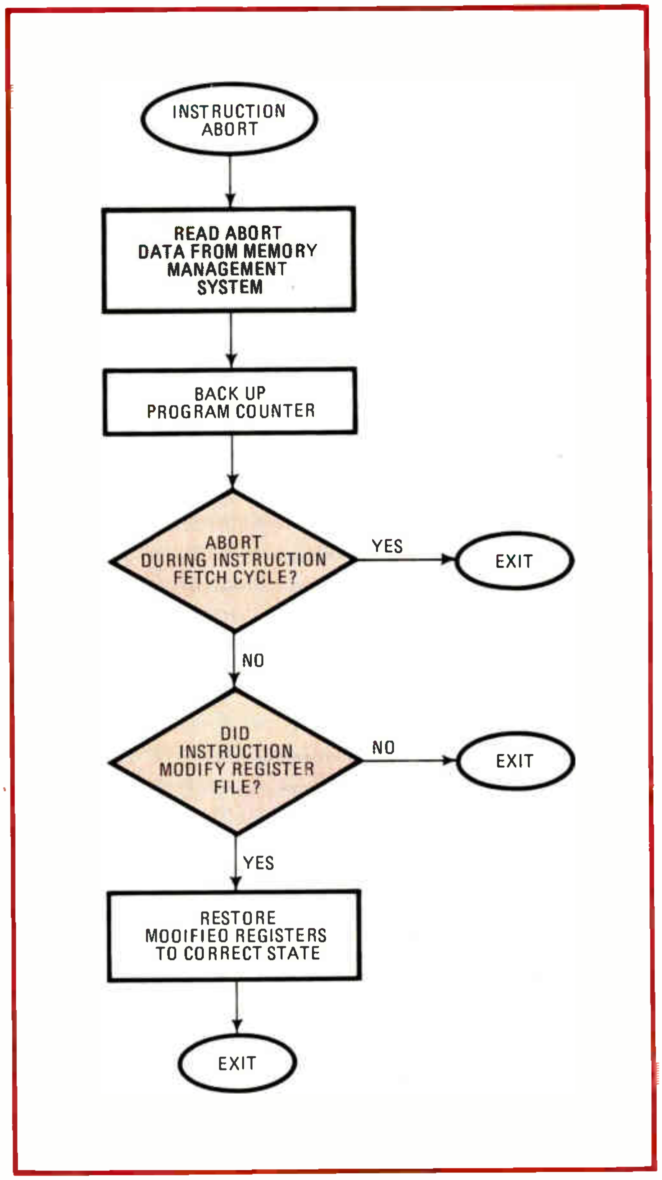
After the Z8003 attempts to reference a logical address not in the main memory and the current instruction is aborted, the addressed data or instruction should be brought into main memory and the aborted instruction should be restarted. To do this, the system designer must provide two pieces of software: a fault handler and an instruction restart routine.

The fault handler is invoked by the address/segment trap request and is responsible for saving information about the aborted instruction and for initiating a request that the data or code be brought into main memory. The designer must also ensure that the state of the aborted program (flag and control word, program counter, and register file) be saved and that another process be executed while the missing data or code is being fetched. Obviously, the fault handler must not generate a fault itself until all data about the aborted instruction and the program state have been saved.

The instruction restart routine must return the program counter to point to the aborted instruction. In addition, it must decode the instruction's operational code to determine if any of the registers had been modified before the cycle when the abort occurred (Fig. 3). For a small number of instructions, some registers will have been modified, so this routine must return these registers to their previous states. Which instructions require fixing of the registers and how to fix the registers depends upon whether segmentation or paging is used.

In either case, the system stack must always be in main memory so that accessing it will never cause a fault. Input/output buffers should always be in main memory so that I/O instructions will never cause a fault. Finally the program status area should always be in main memory, too.

Given these conditions, the following information must be available for restart of an instruction: the program-counter value during the initial instruction fetch cycle (signaled by a special code on the status



3. Reaction. Whenever the instruction-abort mechanism is activated, the system-level software must save the program's status, swap in the missing segment, restore registers that may have been modified, and retry the instruction by backing up the program counter.

output lines), the address that caused the fault, the state of the status lines during the aborted cycle, and (for paged memories) the data in a counter that records the number of successful data accesses made by the instruction before it was aborted.

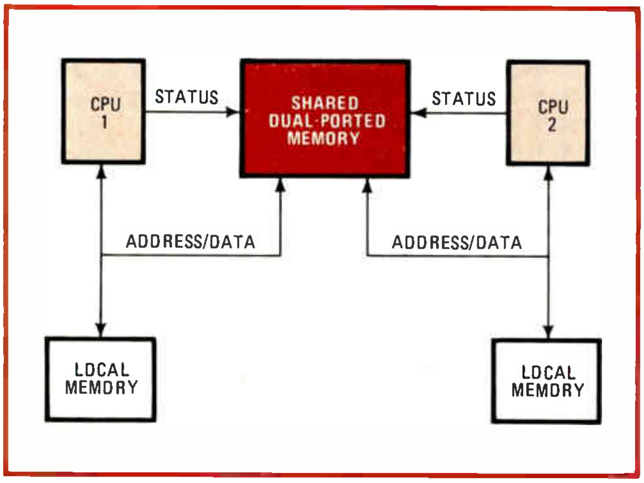
Restarting instructions

To recover from an absent segment, an aborted instruction can simply be restarted after the segment swap by reloading the program counter value saved by the memory management system. There are 24 instructions for which registers may have to be reinstated to their original condition. The software fix required for these functions involves adjusting either a pointer register or a count register. For example, if a write is attempted to an absent segment during a push instruction, the stack pointer must be incremented by two before the instruction is restarted.

To recover from a page fault, an aborted instruction can simply be restarted after the page swap by reloading the program counter. On a paged scheme, there are 29 instructions for which registers may have to be reinstated in their original status. Aside from the updating of pointers (as for the segmented virtual memory), most of the complexity of the instruction restarts arises from accessed data crossing a page boundary while modifying a register used for the address calculation.

An example might be an instruction that loads four words into contiguous registers, using the contents of the first two registers to point to the data. If a page fault occurs after two data reads, the addressing information will be overwritten and must be recovered before restarting the instruction. Given the faulty address and the number of successful read operations carried out before the fault is encountered, it is a simple matter to restore the contents of the pointer register and restart the instruction.

Zilog's memory management unit, the Z8010 MMU, contains most of the circuitry required to implement a segment-swapping memory management system. It contains 64 segment descriptors, so that a pair can translate addresses for all 128 segments a Z8003 can access.



4. Multiprocessors. The Z8003 also implements a special instruction that locks out other processors trying to access a common resource, in effect performing a read-modify-write operation that is ideal for implementing semaphores for interprocessor communication.

The 8010 also automatically records the most significant 15 bits of a violation address, so only an additional 8-bit register is needed to record the low-order byte of the program counter. This register is updated at the beginning of each instruction (indicated by the instruction fetch-status that the Z8003 puts out) and is locked when a suppress signal indicates a missing segment or an access violation.

One bit in each segment descriptor can be used to indicate that a segment is currently outside main memory. Other bits provide additional protection, since segments may be marked as read-only, execute-only, or system-only.

The 8010 also records the accesses and writes to segments. This record can be used to determine which segments have been referenced and which of them have been modified.

Such data is useful in improving the performance of a virtual memory system. Segments that are frequently referenced should remain in main memory. Segments that have not been modified from their original state in secondary memory may simply be written over when swapping in new segments without writing the unmodified segment back into secondary memory. Thus the frequency of address translation faults and the amount of traffic between main memory and secondary memory may be minimized.

In addition to the 8010, Zilog will be offering another MMU that will add the hardware support for a paged virtual memory. In fact, no external circuitry beyond this paged MMU will be required.

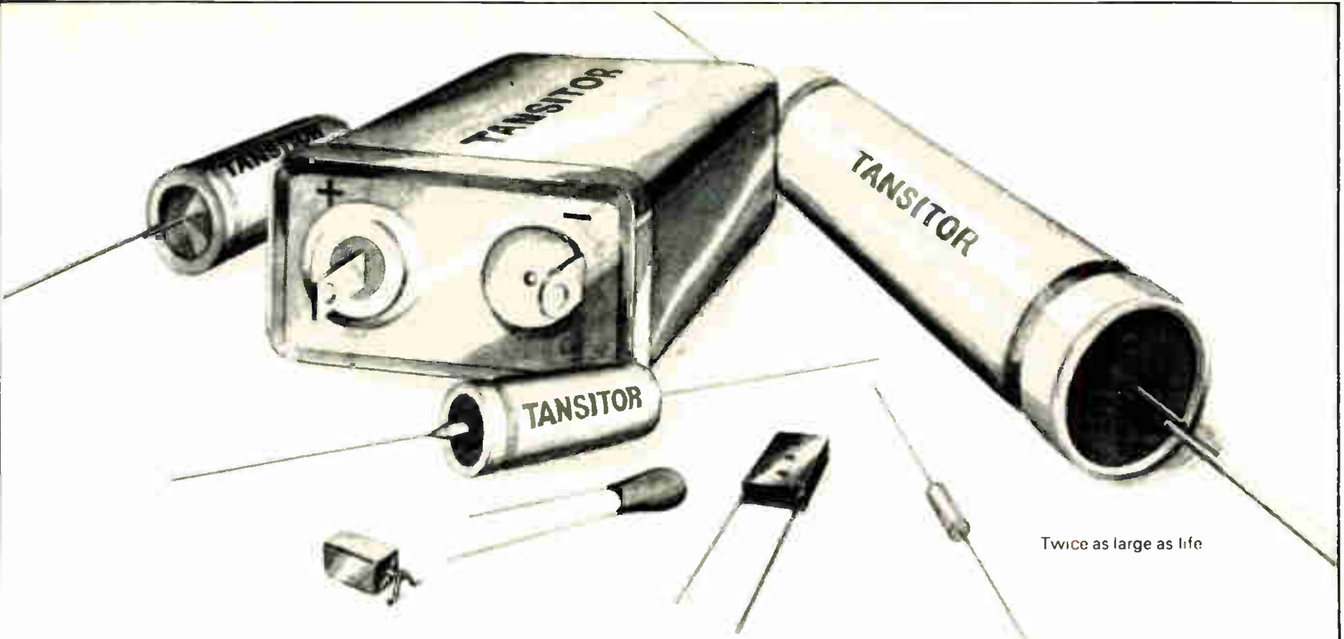
Managing more processors

The Z8003 differs from the Z8001 in one other respect. It includes a feature useful in implementing software semaphores that synchronize access to critical resources in a multiprocessor environment.

During its test-and-set instruction, it puts out a special status code that in effect forms a read-modify-write data access. This signal can be used to lock out other processors from, say, accessing memory between the reading and updating of a variable.

In a two-processor system (Fig. 4) where each processor has access to a dual-ported random-access memory with a list of tasks to be performed, a RAM byte can be used to indicate when one of the processors is updating the list. For access to the list, a processor performs a test-and-set operation on this byte, checking to see if the other processor is accessing the list and setting the byte to indicate that it intends to access the list. It repeatedly executes the test-and-set operation in a loop until the other processor has finished, then updates the list and clears the byte (indicating the list is available to the other processor).

By using the test-and-set signal to lock out simultaneous accesses, the system guarantees proper synchronization of the two processors. It is impossible for both processors to read the semaphore byte simultaneously and to assume that each has exclusive access to the list—which could lead to both removing the same task from the list. □



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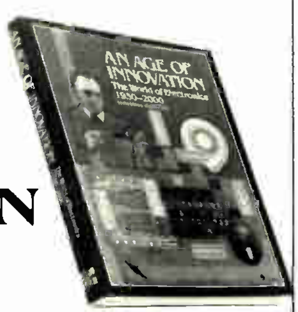

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LSI chips shrink synchro-to-digital converter hybrids

C-MOS LSI design gives s-d hybrids twice the accuracy and smoother output than conventional devices

by Seymour Lanton, *ILC/Data Device Corp., Bohemia, N. Y.*

☐ A combination of custom monolithic and hybrid technologies known as the Monobrid process is helping create a whole new series of improved data-conversion products. Intended for thick-film hybrids and designed specifically for data conversion, each chip replaces the many standard small-scale integrated circuits used in a conventional hybrid design. As a result, many interconnections are eliminated, increasing the converter's reliability and reducing its size and power consumption. In addition, custom features can be designed into the chips at relatively low cost.

The first of these new products is the HSDC-8915, a 14-bit tracking synchro-to-digital (s-d) converter that is intended as a replacement for discrete converters, rather than as a competitor for other hybrids. But compared with its 14-bit hybrid predecessor, which was made with standard ICs, the new unit is a great improvement It consists of two custom ICs (along with six other standard ones) housed in only one 36-pin double dual in-line package instead of 18 standard chips in two DIPs. At 1 ounce, it has half the earlier device's weight, and it is four times as reliable (its computed mean time between failures is 2.66 million hours in a ground-benign environment). One +15-volt power supply replaces +15-V and −15-V supplies, and the 8915 consumes only 30 milliamperes, or about half as much power.

The converter also includes a 2-byte, three-state output for an eight-line data bus and an inhibit-controlled data latch so that inhibit commands do not interfere with continuous tracking. It exhibits an accuracy of within 2.6 minutes and an inherently smoother output, and its combination of high reliability and low cost ($385, compared with $809 for its predecessor) can dramatically decrease life-cycle costs.

Many major IC manufacturers do not offer chips designed specifically for s-d conversion because the market is relatively small. Because of this, ILC chose to do its own custom IC design work in house and then opted for outside wafer processing.

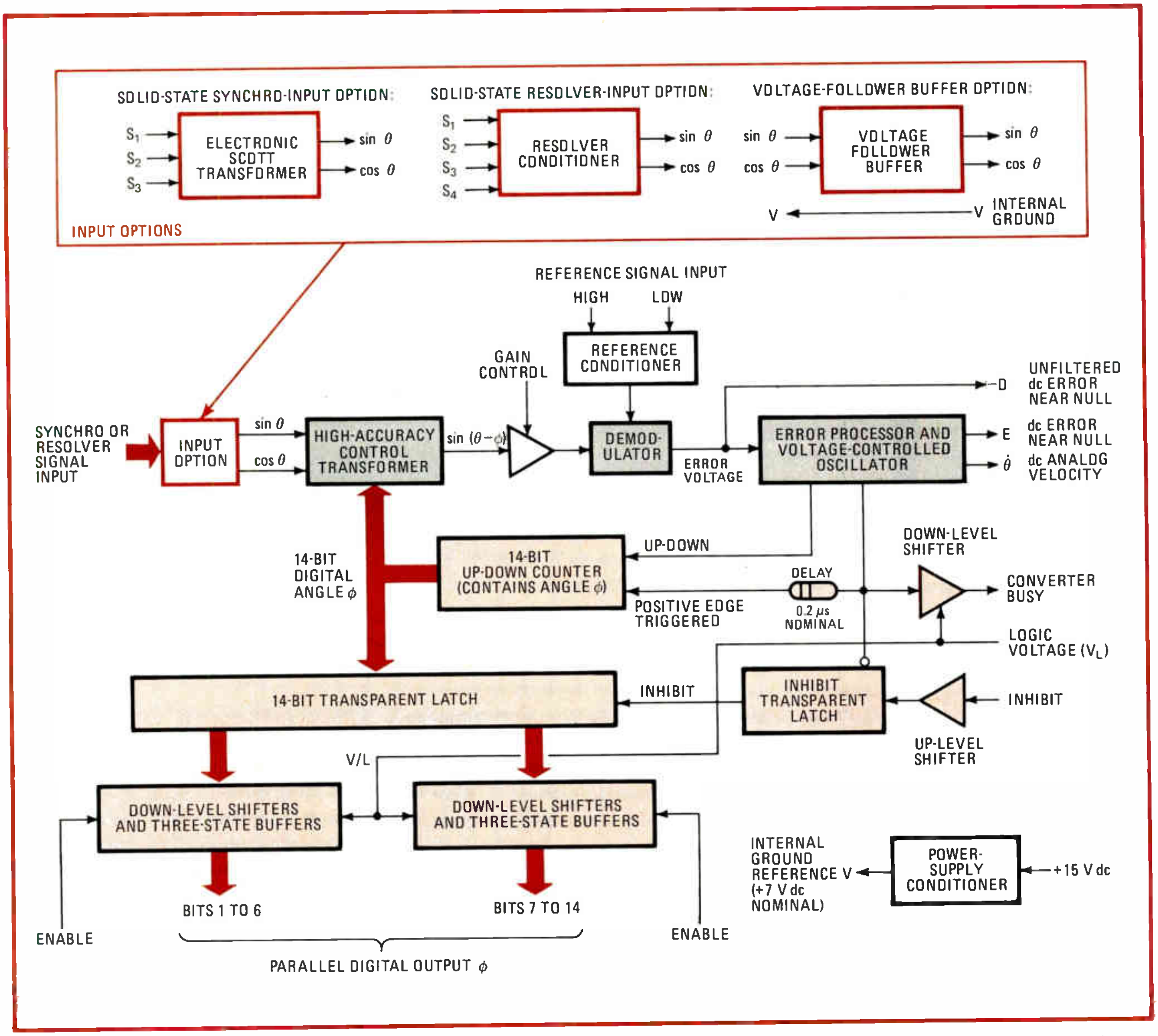
Synchro-to-digital converters require both digital and analog circuit elements. Thus, complementary-MOS processing was chosen for the 8915 because it is well-suited to both analog switching and digital logic. In addition, C-MOS uses little power and its speeds are adequate.

At this time C-MOS processing cannot be used to produce the fast operational amplifiers and comparators with the low offsets currently available with bipolar linear ICs. However, C-MOS methods are easier to apply than their bipolar counterparts and can be used to implement the majority of the functions in an s-d converter.

Moving on chip

For the 8915, the engineers designed two ICs that include the analog switches needed for the control transformer and all the logic- and TTL-compatible interface components, such as drivers and receivers. The block diagram of Fig. 1 shows approximately what is contained on the two custom chips. The colored areas are entirely contained on the two chips, whereas the gray ones are only partially so.

Analog functions such as comparators and op amps are implemented with commercially available IC chips.



1. Customizing. In this block diagram of the HSDC-8915 s-d converter, the colored areas represent circuitry contained completely within two custom chips. Gray areas indicate the circuitry partially contained on them. All other blocks employ standard small-scale ICs.

This is only the first step in applying the Monobrid process, and a new s-d converter chip design in which more functions are implemented with the C-MOS process is already under way.

As the block diagram shows, the 8915 consists of three main parts—an input-signal conditioner, a servo loop whose output is the angle φ, and digital logic that includes both the inhibit circuits and three-state buffers. Input options include solid-state inputs that permit common-mode isolation for direct synchro or resolver signals and a low-level resolver input option for external isolation transformers or low-voltage resolver signals derived from other solid-state circuits.

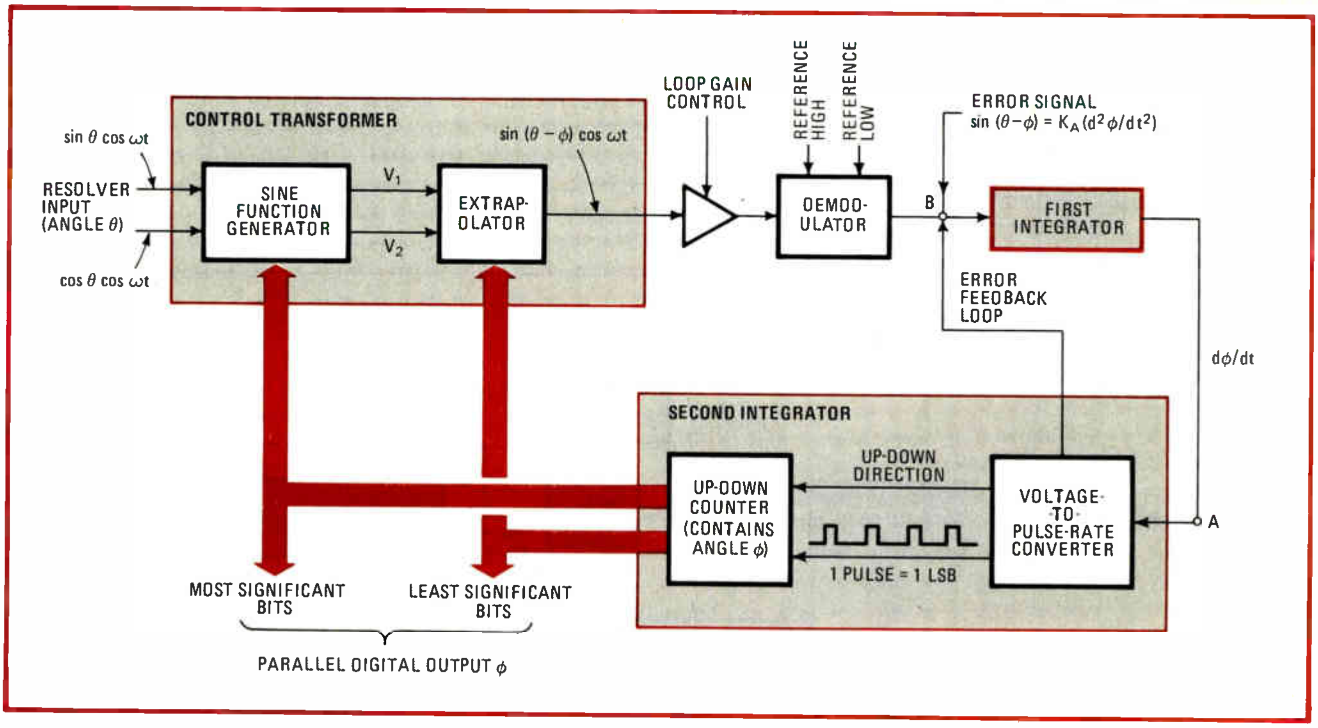
The digital logic section has special features. A transparent output latch and inhibit logic have been added so that the inhibit function can lock the output bits for data transfer while the servo loop continues to track data. An inhibit command can be applied at any time because the inhibit logic prevents interference during the time between the updating and inhibiting of the transparent latch. The three-state buffers provide either normal 14-bit parallel output or enabled 2-byte output for eight-line microprocessor systems. All digital input and output is level-shifted to the user's external logic level, which can include C-MOS as well as TTL levels.

Closing the loop

The servo loop contains the most significant design features of the 8915 converter. A highly accurate control transformer makes it possible to obtain a smoother and more accurate output from the servo loop.

As illustrated in Fig. 2, the servo loop used in the 8915 is similar to that used in other DDC tracking converters. The output from the loop is the digital angle φ, which is contained in the up-down counter. The input angle θ from the synchro or resolver is resolved into two components: sin θ cos ωt and cos θ cos ωt.

The control transformer serves as a summing junction



2. Double integration. The servo loop of this tracking converter has two integrations—a conventional op amp type followed by a digital integration in the counter containing the output angle. This type II servo can follow a velocity signal without exhibiting any lag.

for the main servo loop, producing a signal that can be expressed as $\sin(\theta-\phi)\cos\omega t$. The error term $\sin(\theta-\phi)$, modulated by the reference carrier ($\cos\omega t$), represents the difference between the counter angle ϕ and the measured angle θ. At point B shown, the carrier ($\cos\omega t$) has been removed by the demodulator.

The main servo loop contains two successive stages of integration—an analog integrator followed by a digital integrator. The voltage-to-pulse-rate converter produces pulses at a rate that is proportional to the input voltage at A, and each of these pulses updates the counter by 1 least significant bit. Since the digital angle, ϕ, is equal to the product of the pulse rate and time, it therefore integrates the voltage at A.

The two stages of integration create a type II servo loop, which has the characteristics described in "Tracking characteristics of the type II servo loop" (see opposite page). The output ϕ from a well-designed servo loop should remain accurate, stable, and well-behaved as the input angle θ changes.

A matter of minutes

Most tracking converters have an accuracy of within about 5.3 min. Essentially this figure depends on the accuracy of the control transformer; offsets in the second integrator will not contribute to the inaccuracy. However, quadrature voltages should be adequately filtered. The dead zone (hysteresis) created by the error feedback loop (a minor feedback loop) should be less than 50% of the accuracy so as not to dominate it.

In the 8915, the transformer's accuracy has been doubled to within 2.6 min. The error gradient (error signal per LSB) is so high that offsets of as much as 25 millivolts dc contribute less than 20 arc-seconds to the unit's total inaccuracy.

The quadrature voltages are generally small enough in a 14-bit converter that the reference input to the demodulator does not have to be used to compensate for the usual 5° phase lead of a synchro or resolver signal. The dead zone in the 8915 is ±1.2 min., or ±0.9 LSB.

The output (ϕ) is jitter-free and does not hunt. It will also be stable if the differential linearity and the filtered noise are sufficiently small compared to the hysteresis. The differential linearity in the 8915 series is ±¼ LSB.

Smooth transitions

As the input (θ) changes, a well-behaved output makes smooth transitions at all carry points, does not run through transitions, changes direction smoothly, and does not jitter. The control transformer is again the most important factor because it is where the transitions occur and where glitches are most likely to arise.

The output will not run through transitions if the differential linearity is small and the dead zone is narrow. Smooth changes in direction are a function of smooth transitions between positive and negative voltages throughout the loop, including the control transformer, the first integrator, and the output of the voltage-to-pulse-rate converter.

The quality of the control transformer is the most critical element in the design of the servo loop. Its performance is limited both by the accuracy of the algorithm used and by errors introduced by physical components. A good algorithm not only introduces negligible math errors (which are due to the approximation of a trigometric function) but also is easily implemented. In a well-designed control transformer, component error is usually the main source of inaccuracy.

The 8915's control transformer meets these previous criteria with the following parameters:

Tracking characteristics of a type II servo loop

The tracking characteristics of a type II servo loop can be derived from the basic loop equation. The loop equation can be obtained by considering the voltage at point B in Fig. 2. At B, the demodulation output is:

$$\sin(\theta-\phi) = K_a (d^2\phi/dt^2)$$

where K_a is the constant of proportionality. The dynamic behavior of the loop follows from that equation. Thus, if the output is constant:

$$\phi = \text{constant}, (d^2\phi/dt^2) = 0, \theta=\phi$$

Therefore the output angle is equal to the input angle.

If the output velocity is constant:

$$d\phi/dt = \text{constant}, (d^2\phi/dt^2) = 0,$$
$$\theta=\phi, d\theta/dt = d\phi/dt$$

As a result, the output angle tracks the input angle without lag. The input velocity will equal the input velocity so long as the maximum rate of the voltage-to-pulse-rate converter is not exceeded.

If the output acceleration is constant:

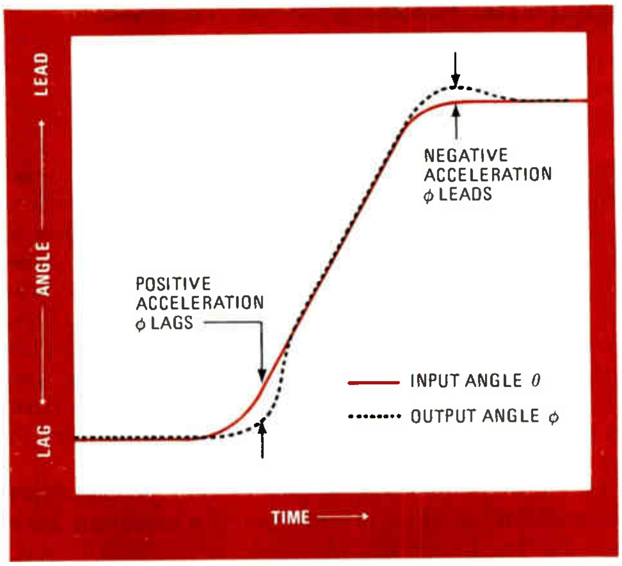
$$K_a(d^2\phi/dt^2) = \text{constant} = \sin(\theta-\phi)$$

Differentiation shows that:

$$d\theta/dt = d\phi/dt \text{ and } d^2\theta/dt^2 = d^2\phi/dt^2$$

Thus, the output velocity and acceleration are equal to the input velocity and acceleration. Furthermore, there will be a finite lag between θ and ϕ. For small accelerations of $\sin(\theta-\phi) = (\theta-\phi)$, the lag is equal to $K_a\, d^2\phi/dt^2$, where K_a is the acceleration constant.

The dynamic behavior of the loop is illustrated in the figure. Except for a temporary lag or lead during periods of acceleration, the output will always be equal to the input.



■ A ratiometric design that limits its errors to the relative ratio errors of the unit's sine and cosine channels.
■ A very low math error that limits accuracy to ratio errors due to precision thin-film resistor errors.
■ A Gray code algorithm for bits 1 to 5 that keeps them totally independent of the transformer's degree of accuracy so that, whenever any of the 5 most significant bits change, the transformer's output, sine $(\theta-\phi)$, will change by 1 LSB to the accuracy of the LSB circuit.
■ A Gray code algorithm designed to limit switching noise and keep the converter inherently jitter-free. Switching noise in an ac carrier system has two sources: the well-known high-frequency spike associated with the switches and the less well-known step change in the dc level that usually occurs at major switching points like quadrant points when sine-cosine signals may be switched from plus to minus gains or when the sine-cosine signals may be interchanged because op amps are switched around. Although normally dc levels are capacitively coupled out and are not a source of error in themselves, a step change in dc level will instantaneously couple through the coupling capacitor and may cause jitter. The Gray-coded control transformer is designed to eliminate step changes in the dc level so that the converter is inherently jitter-free.

Tracking the s-d field

The most important benefit of the new Monobrid units is their reduced cost. In the short run, the lower-cost hybrids can be expected to replace comparably priced discrete converters, as well as other hybrids. And as the new technology matures, further price reductions should expand the s-d converter market. This is because s-d and resolver-to-digital converters are the most significant cost elements in designing instruments for synchro or resolver shaft-angle measurement.

The largest segment of the s-d converter market is shipboard applications, including inertial navigation, steering control, sonar, radar, fire control, and retransmission systems. Most shipboard converters have been discrete modules because hybrids have been more expensive. At the same price, the HSDC-8915 will occupy much less space, require fewer power supplies, consume less power, and have much greater reliability. A system filling an entire rack can be replaced by a few printed-circuit boards, and life-cycle costs will be reduced.

Potential new markets strongly influenced by these costs include industrial applications, such as numerical control of machinery and heavy equipment. A mining machine with multiple drilling arms, for instance, requires simultaneous control of many shaft angles and positions. Another potential market is in solar power stations with a central energy collector. The azimuth and elevation of thousands of reflecting arrays must be continually adjusted to aim the solar radiation onto the central collector. Price decreases brought about by the Monobrid technology may help to make such solar power plants economical.

For some users, however, the most important benefit from the new technology will be the converter's reduced size and weight. These factors are important in commercial and military aircraft, which require a variety of angular-position indicators for navigation functions, flight control, fire control, and general instrumentation. □

Dynamic depletion circuits upgrade MOS performance

by Clay Cranford, *IBM Corp.,*
System Communications Division, Research Triangle Park, N. C.

In the design of MOS integrated circuits, the need frequently arises for an efficient, low-power driver to charge and discharge high-capacitance loads, be they on chip or off. Standard driver circuits include either enhancement-depletion inverters or inverters with push-pull output stages. However, both suffer from high input capacitance, and with a push-pull driver the high-state output voltage is limited to a threshold-voltage drop below the power-supply potential. Clocked driver circuits cut power dissipation, but chip area must be provided for clock-signal generation or routing or both.

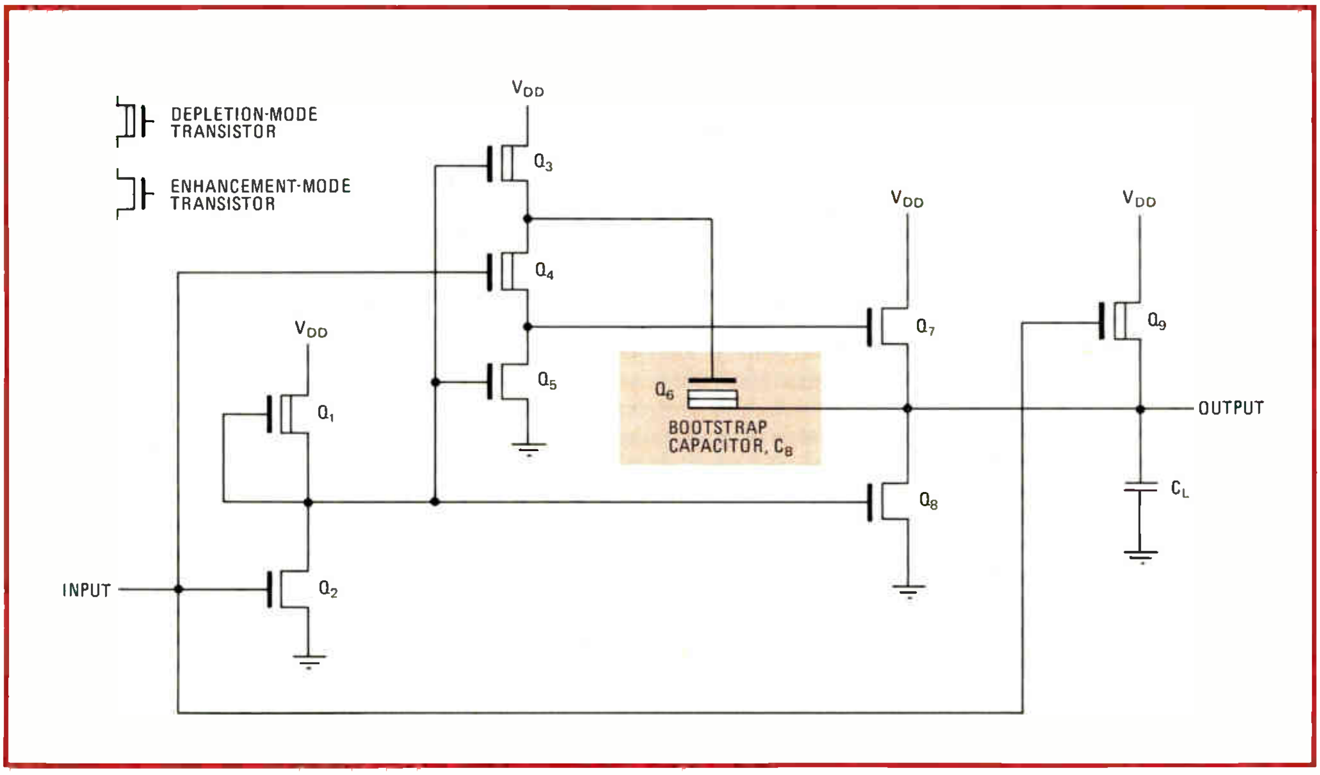
Two new circuit solutions include the dynamic depletion-mode driver (Fig. 1) and the active bootstrap driver (Fig. 2). The first takes advantage of the high conductance of a depletion-mode device under high gate bias. The output can be charged to the full power-supply voltage, V_{DD}, and dc power is reduced by limiting the low output-level current drain. The idea behind the approach is to charge a bootstrap capacitor, C_B, and then redistribute that capacitor's charge when the output is being driven to its high level.

In Fig. 1, transistor Q_6 serving as the bootstrap capacitor is charged to V_{DD} when the input is low. Q_4 is in a low-conductivity state and Q_3 and Q_5 are turned on, causing the gate of Q_7 to be held near ground. As the input rises, the charge on C_B is redistributed between C_B and the gate of Q_7 via Q_4. At this point, Q_3 and Q_5 turn off (Q_3 has functioned as the dynamic depletion-mode device, switching between conductive and nonconductive states). Device Q_7 is switched to its linear region and Q_8 has turned off, charging the output to V_{DD}.

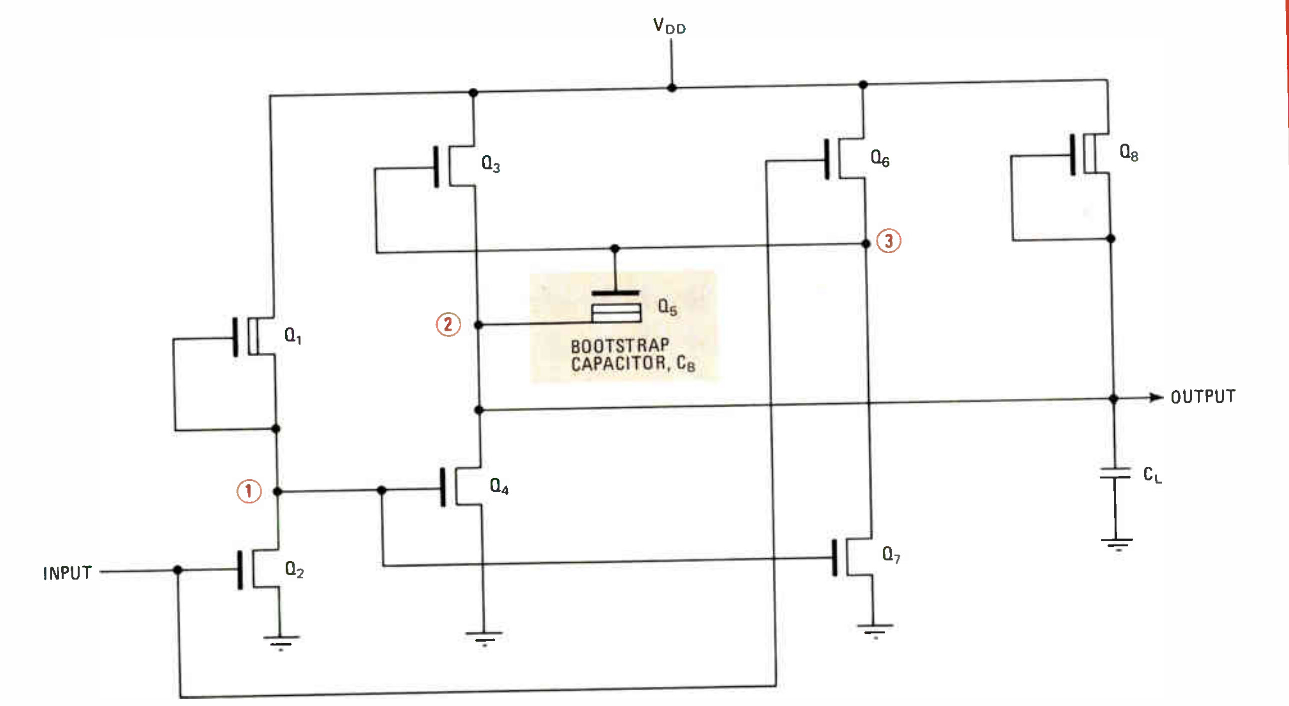
In the active bootstrap technique (Fig. 2), a voltage-bootstrapping circuit and a power-down feature provide a large amount of overdrive and a reduced output-low power dissipation, respectively. The operation of this circuit also has several steps.

With the input low, node 1 is high. Q_6 is turned off and Q_7 turned on; consequently, node 3 is low and driver Q_3 shuts off. Since Q_8 can be made physically long, its current can be limited to a negligible amount. This accounts for the minimal output-low current.

When the input is raised, Q_6 turns on, and after one inverter delay, Q_7 turns off. The bootstrap capacitor — Q_5 in this circuit — is then charged to approximately a threshold voltage below the input, since node 2 is heavily loaded. Node 2 is held near ground by Q_4 during part of the time that Q_6 is turned on because of the inverter



1. Dynamic driver. Bootstrap capacitor C_B is charged to V_{DD} when the input is low, causing the gate of Q_7 to be held near ground. As the input rises, the charge on C_B is redistributed between C_B and the gate of Q_7. The output is charged to V_{DD} as Q_7 is switched to its linear region.



2. Better bootstrap. With the input low, node 1 is high, Q_6 is turned off, and Q_7 is turned on. As a result, node 3 is low and driver Q_3 shuts off. Q_8 can be made physically long, limiting its current and reducing overall power consumption.

delay between the input and the gate of Q_4.

If node 2 begins to move upward during this precharge period because of different loading conditions or because Q_6 is given a smaller width-to-length ratio, Q_6 will dynamically precharge node 3, being bootstrapped by the rising voltage at node 2 and the bootstrap capacitor, and it will turn off when node 3 reaches a threshold voltage below the level of the input signal. Q_4 is not conducting while node 2 is being charged through Q_3.

Since the bootstrap capacitor is precharged, it will boost node 3 to a voltage higher than a threshold drop below the input. This provides increased on-drive for Q_3 and, in turn, a faster rising output transition than might otherwise be possible. The actual voltage to which node 3 is bootstrapped is determined by the ratio of the bootstrap capacitance to that of Q_3 plus the contribution made by parasitic capacitances.

When the input falls, Q_6 turns off, Q_7 turns on, and node 3 is pulled near ground. Q_3 enters a nonconducting state, resulting in a rapidly falling response, since Q_4 need sink current only from the load capacitance. This action helps to reduce the down-level power consumption as well.

Unlike the dynamic depletion-mode driver, this configuration provides for dynamic precharging of the bootstrap capacitor directly from the power supply (through Q_6). A detailed analysis shows that to obtain a given amount of bootstrap voltage, a bootstrap capacitor less than half the size of that necessary for other configurations is required. For the typical layout, it will be considerably less than half.

The active bootstrap technique can be applied wherever high speed and low power are prime considerations—if the extra chip area required is acceptable. The circuit of Fig. 2 has been designed and tested using n-channel silicon-gate technology. □

Computer notes

Writing relocatable code for 8-bit microprocessors

by Richard L. Riggs
Sangamo Weston Inc., Energy Management Division, Atlanta, Ga.

Position-independent code has proven itself in high-level languages as the way to move programs from system to system with little modification to the original software. But writing position-independent assembly code for first-generation 8-bit microprocessors is not always so easy or straightforward. Here is a way of doing it for a common look-up table.

The program at the top of page 131 shows a tradition-

Time for CMOS Microboards.

We've added a timer to our $99 Microboard computer...and it still costs only $99.

Our new timer has a programmable period of 7.6 μsec to 64 seconds.

Operates in 6 modes:

- Square wave output.
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Expanded temperature range. The timer isn't all that's new. The temperature range has been expanded: now it's from **-40°C** to **+85°C.**

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At $99,* the original was a bargain. At $99,* our enhanced CDP18S604A Microboard computer is a steal.

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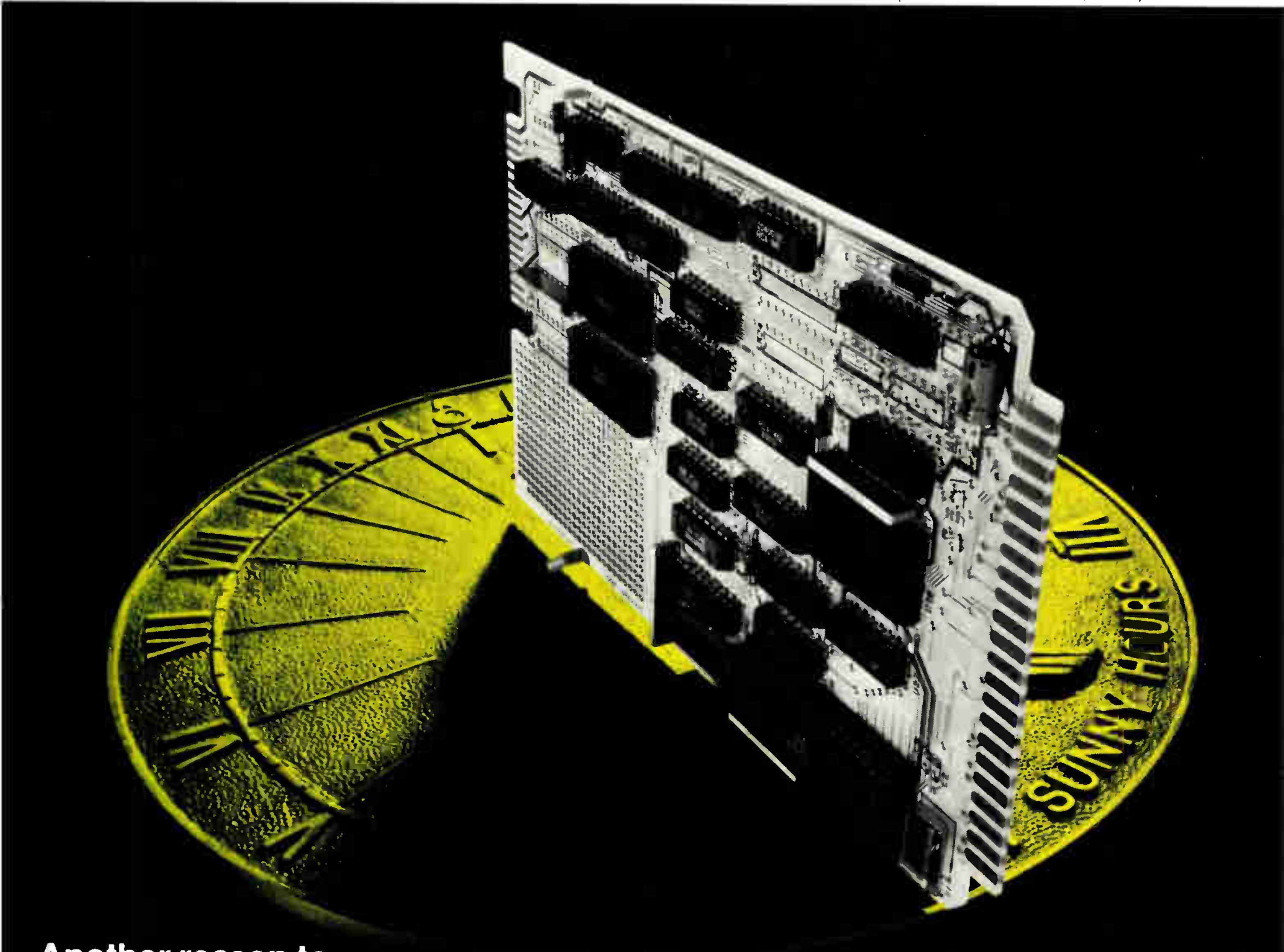
Or contact RCA Solid State headquarters in Somerville, N.J. Brussels, Belgium. Sao Paulo, Brazil. Hong Kong. **Or call Microsystems Marketing toll-free (800) 526-3862.**

*U.S. optional distributor resale, 100+ price.



Another reason to switch to CMOS.

Circle 130 on reader service card

RCA

TYPICAL PROGRAM FOR A POSITION-DEPENDANT LOOKUP TABLE FOR THE 6800

```
200  0000  CE  0019    A  LDDKUP  LDX   #TABLE  }
210  0003  FF  0017    A          STX   TEMP    }
220  0006  FB  0018    A          ADDB  TEMP+1  } calculate the address of the desired data item
230  0009  F7  0018    A          STAB  TEMP+1  }
240  000C  24  03 0011            BCC   EXIT    }
250  000E  7C  0017    A          INC   TEMP    }
260  0011  FE  0017    A  EXIT    LDX   TEMP
270  0014  E6  00      A          LDAB  0,X       data item to B register
280  0016  39                     RTS
290                       ***************
300  0017      0002    A  TEMP    RMB   2
310  0019      04      A  TABLE   FCB   4
320  001A      22      A          FCB   34
330  001B      1D      A          FCB   $1D
340  001C      03      A          FCB   3
350                       *
360                       *       ETC
370                       *
380  001D      0087    A  LAST    FDB   $87
390
```

• Enter with B register containing offset. • Exits with table data in B register. • Uses X register.

TYPICAL PROGRAM FOR A RELOCATABLE LOOKUP TABLE FOR THE 6800

```
420  001F  8D  11  0032  RLDDK   BSR   PSHTAB
430  0021  E6  00     A          LDAB  0,X      data item to B register
440  0023  39                    RTS
450                      ********************
460  0024  36                    REXIT   PSHA     }
470  0025  37                    PSHB            } set up the stack to look as though an
480  0026  07                    TPA             } interrupt occurred
490  0027  36                    PSHA            }
500  0028  30                    TSX             }
510  0029  EB  04     A          ADDB  4,X      } calculate the desired data item
520  002B  E7  04     A          STAB  4,X      }
530  002D  24  02  0031          BCC   REXIT2   } address in the stack X register
540  002F  6C  03     A          INC   3,X      }
550  0031  3B            REXIT2  RTI            return to RLOOK+1
560                      ***********
570  0032  8D  F0  0024  PSHTAB  BSR   REXIT    push RTABLE on stack
580  0034      02     A  RTABLE  FCB   2
590  0035      04     A          FCB   4
600                      *
610                      *       ETC
620                      *
630  0036      87     A  RLAST   FCB   $87
640                              END
```

al look-up table for the 6800 microprocessor. However, the four instructions starting on line 200, as well as those at lines 250 and 260, make this routine position-dependent. Also, 2 bytes of temporary, read/write storage are required, shown here on line 300.

The second program, however, implements a look-up table for the 6800 that is relocatable, uses no read/write memory other than 7 bytes of stack, and works in read-only memory. The trick is on line 570.

For position independence, the branch-to-subroutine instruction on line 570 must be located at the beginning of the table. It pushes the address of the next instruction onto the stack. In this case, the next instruction is not really an instruction but the table base address.

That, along with the push instructions on lines 460 through 490, sets up the stack as though an interrupt had occurred, leaving the address of the table on the stack in the location where the X register would have been pushed had a true interrupt occurred. The balance of the routine adjusts the X register on the stack to point to the desired data item, restores the registers, and obtains the data. This technique works equally well for the 8080 family by using the call instruction. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $75 for each item published.

Engineer's newsletter

Sound-wave velocities help measure high temperatures

A new ultrasonic thermometer accurately measures very high temperatures of up to 2,845°C. Like other such acoustic devices, it converts changes in the velocity of sound waves into temperature readings at points along a sensor wire. Developed at Sandia National Laboratories, Box 4800, Albuquerque, N. M. 87185, it **will work where conditions prevent the use of conventional thermometry equipment,** thermocouples, or optical pyrometers.

Under development for four years, the thermometer consists of a magnetostrictive iron-cobalt head welded to a thoriated tungsten wire whose tip contains small notches (acoustic reflectors) cut at regular intervals. A thin tungsten sheath protects the tip. Microsecond-long pulses, generated 60 times a second by an electromagnetic exciting coil wrapped around the thermometer head, pinch the head, creating acoustic pulses that propagate through the wire. Each notch reflects a small part of each pulse back to the coil, where the reflected energy is amplified and sent to signal-processing circuitry for conversion. Since **the velocity of the reflected pulses depends on the wire's temperature,** the time for reflections to travel from adjacent notches can be translated by means of a calibration curve into the average temperature of the wire between two notches.

The acoustic thermometer is **accurate to ±1° above 1,000°C** and to ±5° below 600°C. In contrast, high-temperature thermocouples typically are accurate to ±5°C in any temperature range.

Motorola offers evaluation kit for its 64-K RAM

Now there is an effective way of evaluating Motorola's 64-K dynamic random-access memory. The firm's Integrated Circuit division, Austin, Texas, has designed a kit specifically for this job and is **selling it for $150. It contains 10 MCM6665L20 64-K dynamic RAMs,** a qualification manual request coupon, two data sheets (MCM6664 and -6665), the company's memory selector guide, and a notebook. Kits are available now, limited to one per customer location. Contact your local Motorola sales office or Motorola distributor.

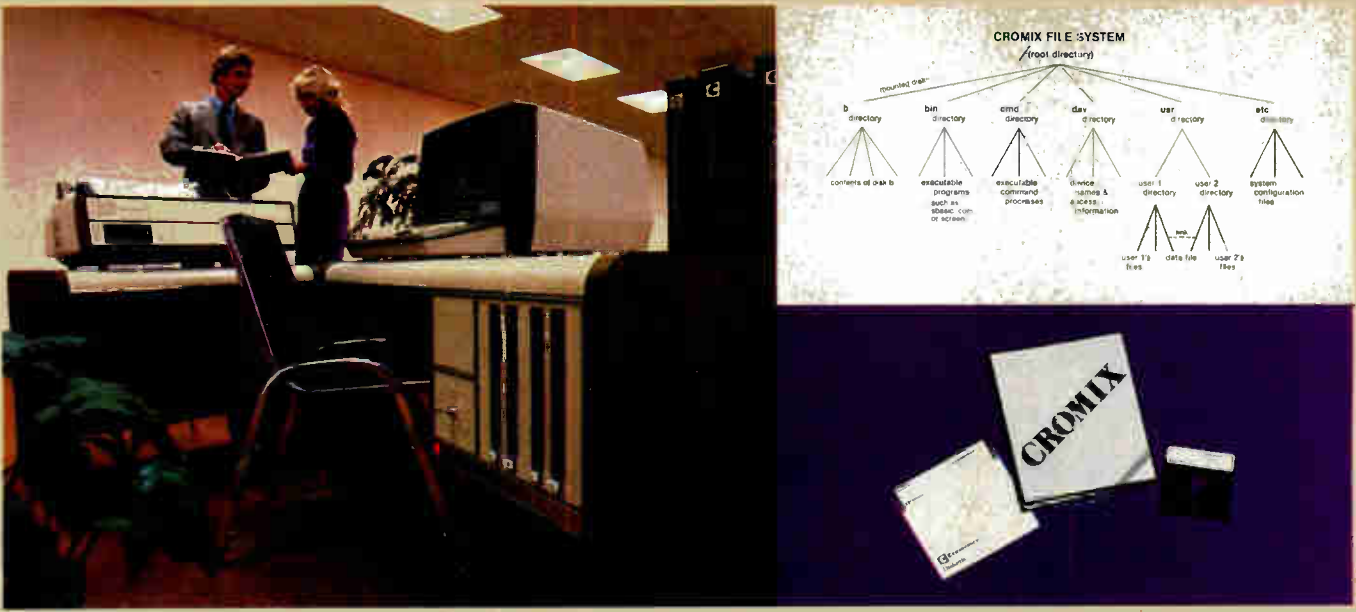
Get the picture(s) on microcontamination

With so many in-house integrated-circuit processing facilities now being installed, knowledge of proper clean-room instrumentation and operational procedures is at a premium. Dryden Engineering has created an audio-visual presentation consisting of 159 slides describing the essentials of microcontamination control. The program, called "Count Down to Zero," answers such questions as: where do microscopic particles come from? how do they travel? and what are laminar airflow system requirement? **Also discussed are detection systems, wet-station electrostatic control, and personnel clean-downs and gowns.** The presentation provides a complete checklist for those who must reduce microcontamination in existing or future process areas. For more information, contact Dryden Engineering Co., 3350 Scott Blvd., Santa Clara, Calif. 95051; (408) 244-7321.

Relay proceedings put between covers

For the specialist in relay design, the 29th Relay Conference Proceedings is now available from the National Association of Relay Manufacturers, P. O. Box 1505, Elkhart, Ind. 46515. The $21 volume contains 16 papers covering various aspects of relay design. Topics included are **uses of surface analysis in diagnosing relay problems** and novel concepts in laser welding of miniature relays.

-Jerry Lyman



CROMIX*— Cromemco's outstanding UNIX†–like operating system

CROMIX is just the kind of major development you've come to expect from Cromemco. After all, we're already well-known for the most respected software in the microcomputer field.

And now we've come up with the industry's first UNIX-lookalike for microcomputers. It's a tried and proven operating system. It's available on both 5″ and 8″ diskettes for Cromemco systems with 128K or more of memory.

Here are just some of the features you get in this powerful Cromemco system:

- Multi-user and multi-tasking capability
- Hierarchical directories
- Completely compatible file, device, and interprocess I/O
- Extensive subsystem support

FILE SYSTEM

One of the important features of our CROMIX is its file system comprised of hierarchical directories. It's a tree structure of three types of files: data files, directories, and device files. File, device, and interprocess I/O are compatible among these file types (input and output may be redirected interchangeably from and to any source or destination).

The tree structure allows different directories to be maintained for different users or functions with no chance of conflict.

PROTECTED FILES

Because of the hierarchical structure of the file system, CROMIX maintains separate ownership of every file and directory. All files can thus be protected from access by other users of the system. In fact, each file is protected by **four separate access privileges** in each of the three user categories.

TREMENDOUS ADDRESS SPACE, FAST ACCESS

The flexible file system and generalized disk structure of CROMIX give a disk address space in excess of one gigabyte per volume — file size is limited only by available disk capacity.

Speed of access to disk files has also been optimized. Average access speeds far surpass any yet implemented on microcomputers.

'C' COMPILER AVAILABLE, TOO

Cromemco offers a wide range of languages that operate under CROMIX. These include a high-level command process language and extensive subsystem support such as COBOL, FORTRAN IV, RATFOR, LISP, and 32K and 16K BASICs.

There is even our highly-acclaimed 'C' compiler which allows a programmer fingertip access to CROMIX system calls.

THE STANDARD O-S FOR THE FUTURE

The power and breadth of its features make CROMIX the standard for the next generation of microcomputer operating systems.

And yet it is available for a surprisingly low $595.

The thing to do is to get all this capability working for you now. Get in touch with your Cromemco rep today.

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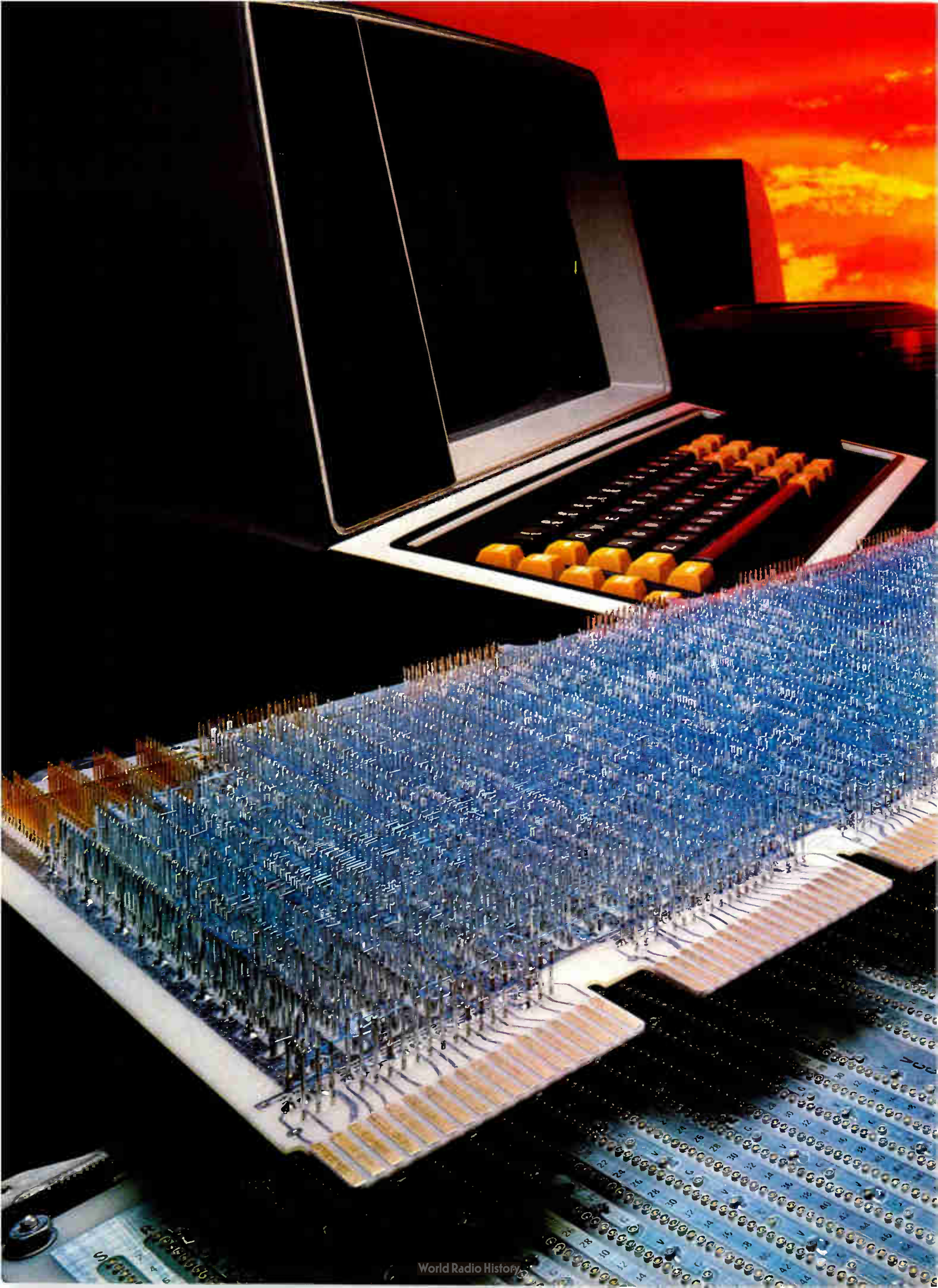

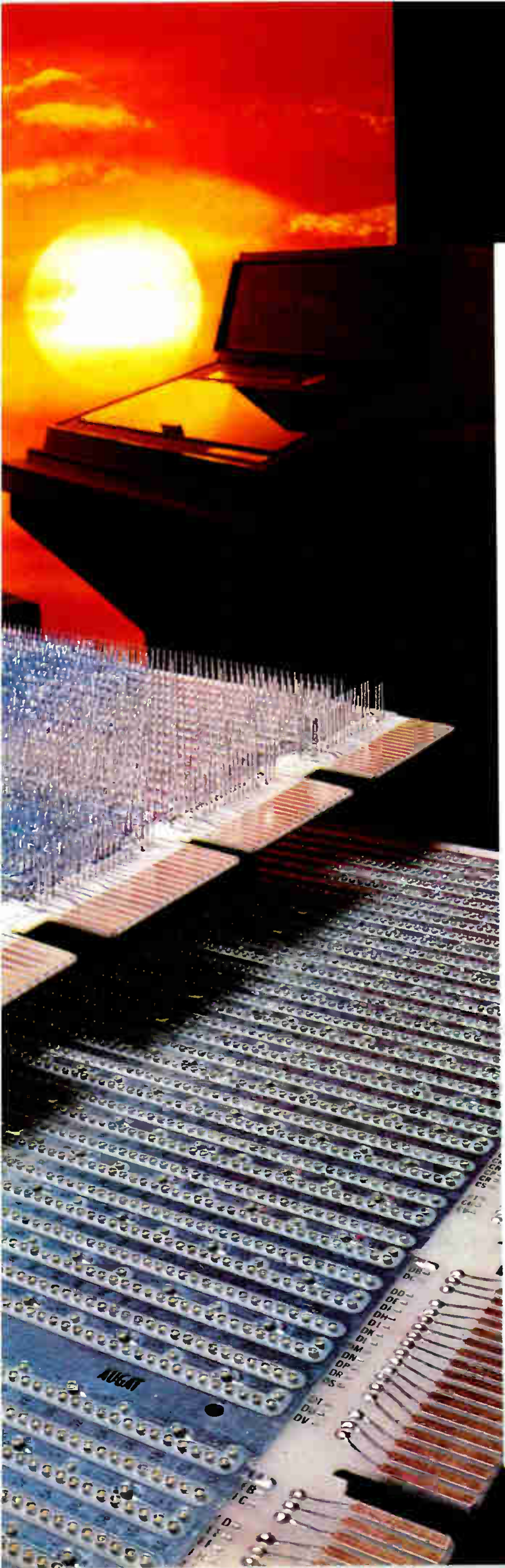

The many interfaces of Augat.

Augat wire wrap* interface panels make it easy to connect with the big names in the minicomputer industry. Digital Equipment Corporation, Data General, Intel, Motorola, Prolog, Zilog, Texas Instruments and all the rest.

First, because our inventory of chassis and bus compatible IC pluggable panels is the most extensive in the business. We have patterned boards and boards with universal columns which accept IC's of all sizes. In fact, there's one to match the specifications of virtually any minicomputer on the market today.

Second, because Augat interface panels give you the time- and money-saving advantages of wire wrap. Their inherent flexibility lets you get your design to the market faster. A strategic advantage and a head start on sales and profits. Logic and wiring changes are quick and inexpensive at any design stage—pre-production, production, even in the field.

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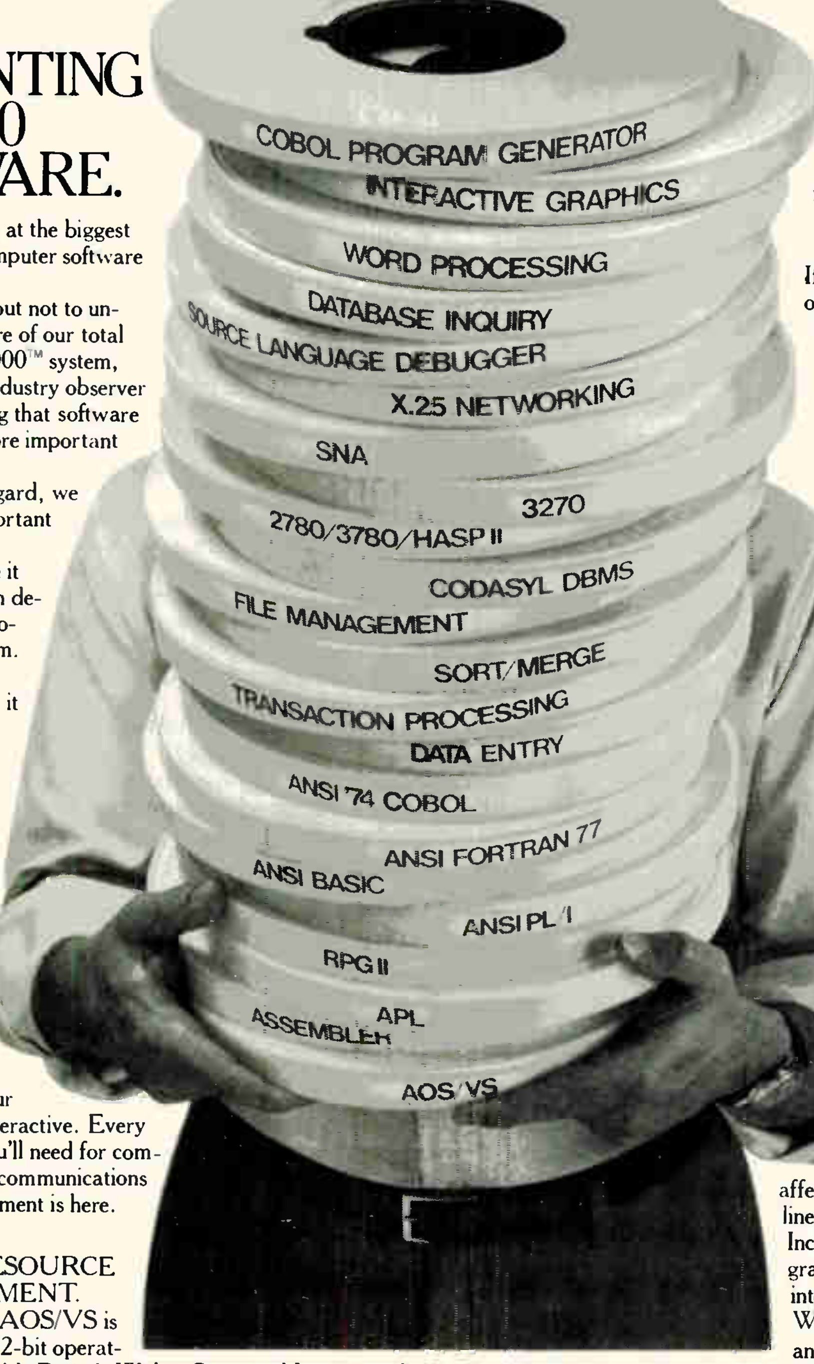

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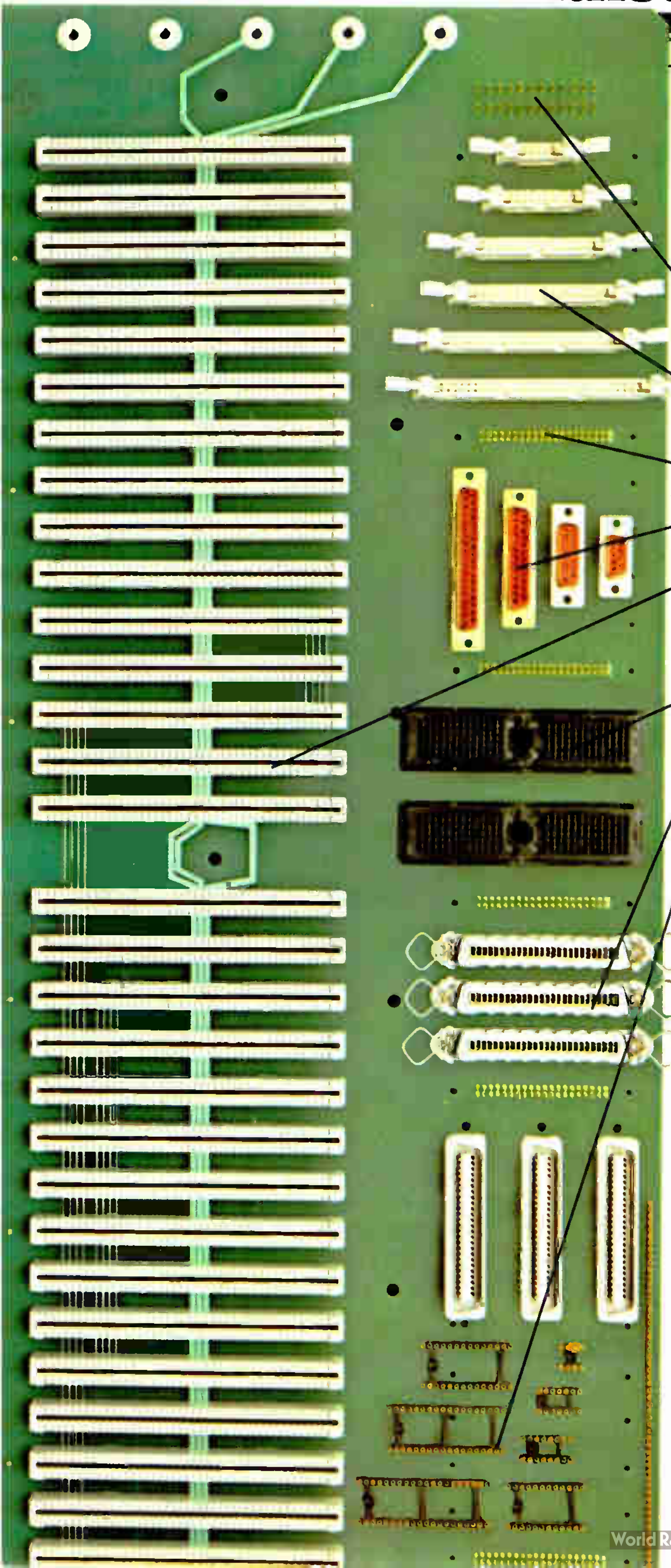

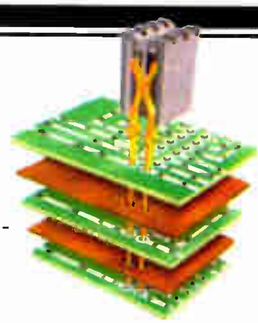

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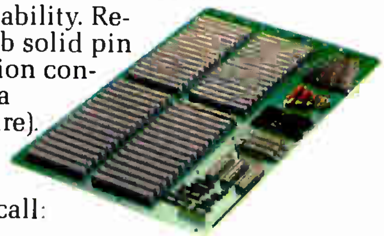

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Local net carries video, data traffic

Coaxial-cable network has 10-to-350-MHz bandwidth to serve video equipment, slow terminals, and fast computers

by Linda Lowe, Boston bureau

The first segments of a local communications network from Wang Laboratories will begin linking users' terminals, video systems, and Wang computer and word-processing systems as phased deliveries take place over the next year and a half. That is just the beginning for WangNet, according to the firm, which plans to add more capabilities such as voice communications later on.

WangNet is a broadband network, having a bandwidth of 10 to 350 MHz. "We chose broadband because it accommodates more data—and more diverse kinds of data—than can baseband or discrete-frequency networks like Ethernet," says William F. Rosenberger, Wang's director of networking. WangNet initially comprises three separate bands.

The network uses off-the-shelf cable-television coaxial cable and associated equipment like taps and splitters. Its main trunk has an open-loop configuration and supports a branching-cable topology that permits its connection to a large number of nodes, says Rosenberger.

Ready for immediate delivery is WangNet's so-called Utility Band, which allocates 174 to 216 MHz for up to seven independent channels available to composite video equipment. This band employs no active components, instead using standard coaxial cables and connectors to link video conferencing and monitoring devices.

WangNet's Interconnect Band, parts of which will be available in early and mid-1982, supports two different kinds of channels, which, through their respective modems, can accommodate any machine having an RS-232-C port. The Interconnect Band is protocol-independent: it has no provisions for protocol translation and so assumes the use of either the same protocol by communicating machines or external translators for individual machines.

Due for first deliveries in January or February 1982 are fixed-frequency modems that interface machines to dedicated channels on 10-to-22-MHz portion of the Interconnect Band. These channels act like leased telephone lines, forming permanent links for point-to-point or multipoint communications between two or more machines. Of these channels, 32 handle data-transmission rates of up to 9.6 kb/s; their associated fixed-frequency modems will cost about $850 each. Another 16 of the permanent channels speed data rates to 64 kb/s; their modems will cost

Message system takes on 'telephone tag'

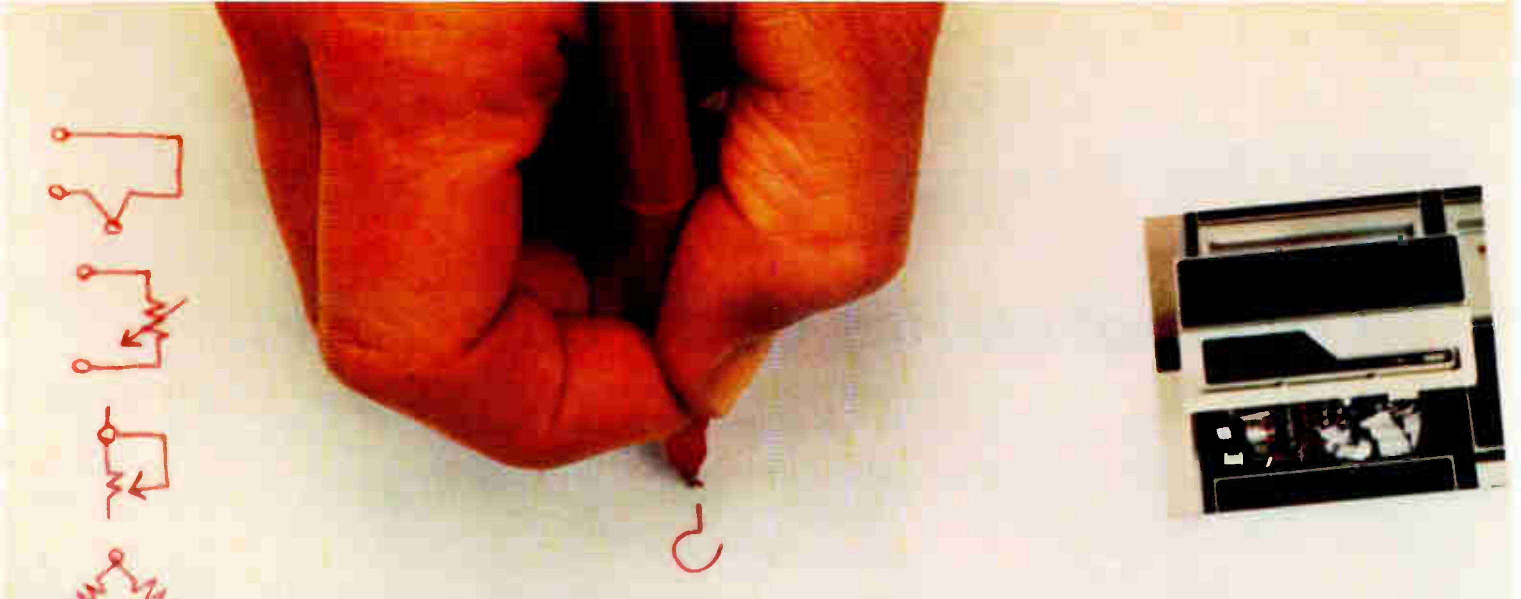
Another push toward the automated office by Wang Laboratories Inc. comes with Wang's introduction of a digital voice exchange (DVX). The system, which can operate over with a company's internal phone lines or private-branch-exchange, Centrex, WATS, and 800-number lines, acts as a telephone secretary, transmitting and storing digitized voice messages (or "voicegrams") for up to 800 users.

Wang has run DVX in its own Lowell, Mass., headquarters for five months, reports director of voice development John W. Sawyer. "DVX has proved a welcome remedy for 'telephone tag'—that frustrating business of trying to catch busy people at their desks and leaving endless call-back messages."

DVX works with any phone equipped with a tone generator. Up to 16 Z80-based input/output message processors (IOMPs) digitize voice messages and transmit them to a central processing unit with 128-K bytes of buffer random-access-memory. The CPU stores the data on disks. When a user calls up messages by punching simple codes on the telephone key pad, the CPU retrieves them and sends them back for reconversion into audio form by the IOMP. It also sends the user recorded prompting instructions for calling up and routing messages and generating new ones.

When generating a message, the user can specify the time and date of receipt by other parties up to 31 days in the future and may simultaneously direct the message to up to 16 phones or up to eight previously established user lists of up to 32 users each. A recipient may send a return message, forward the message to another phone together with a new explanatory voicegram if necessary, or instruct the DVX system to retain the message for later recall. A user planning to be out of the office can generate a message that will play back in response to any incoming call. Software includes a statistical reporting package that monitors system use, traces messages, and keeps track of use of the system for billing purposes.

The DVX system becomes available in January 1982. At the low end, it consists of a CPU, four IOMPs, one 300-megabyte disk drive, a work station, and a printer; this configuration will serve 200 users and cost in the neighborhood of $125,000. A high-end, 800-user system with 16 IOMPs would cost about $320,000—or $400 per user—estimates Wang's Sawyer. -L. L.



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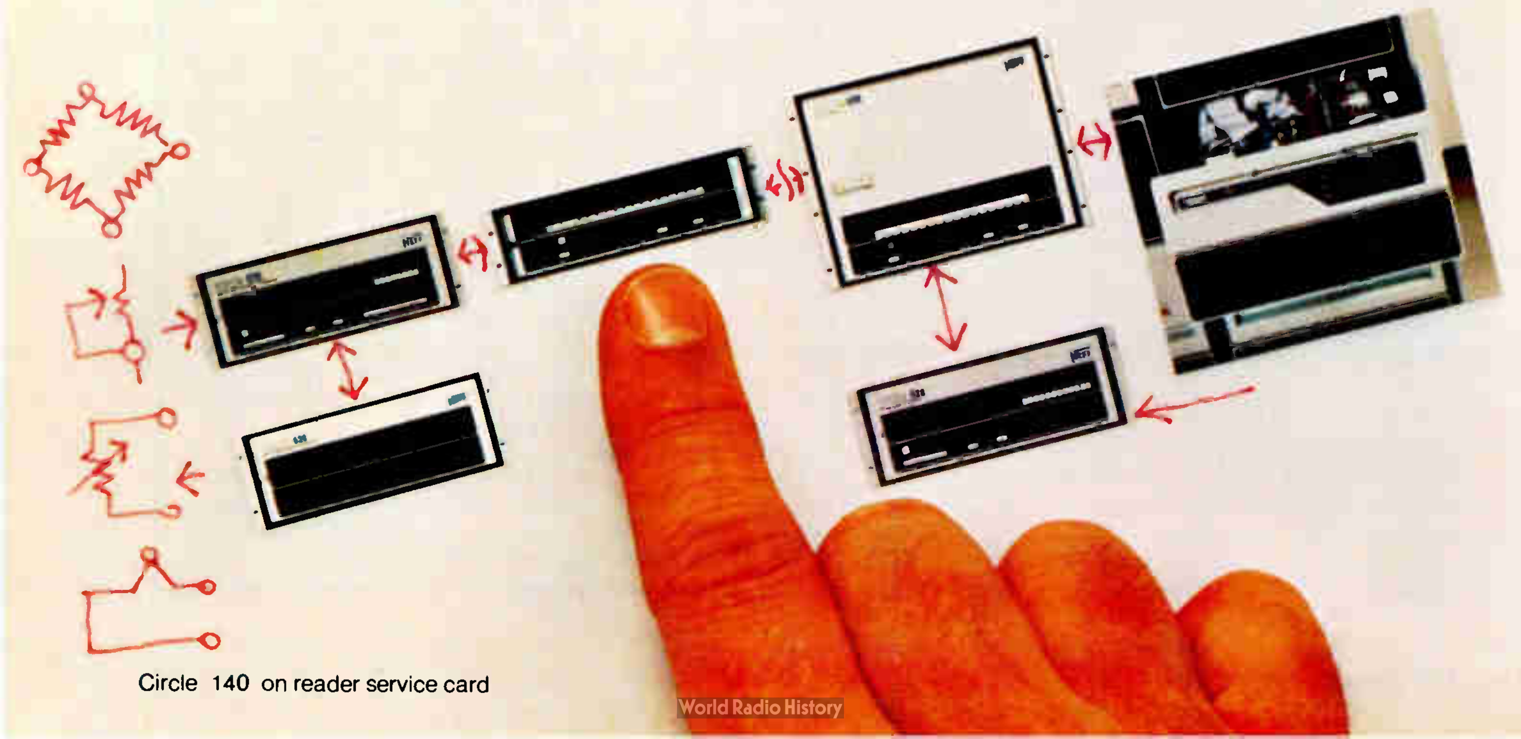

Circle 140 on reader service card

approximately $1,250 each.

The Interconnect Band also supports switched-circuit, point-to-point communications among a maximum of 512 devices connecting on up to 256 channels via frequency-agile modems operating at 48 to 81 MHz. A single unit called a DataSwitch controls the machines' access to one another; when a terminal's operator dials the number of a target machine, the DataSwitch checks the machine, establishing a communications frequency if the machine is free or returning a busy signal if the machine is already engaged. The maximum frequency-agile transmission rate is 9.6 kb/s. Wang plans mid-1982 deliveries of the DataSwitch, priced at about $12,000, and of the frequency-agile modems, which will cost between $1,200 and $1,300 each.

For speed. WangNet's third band (217 to 253 MHz), called the Wang Band, consists of a single channel able to serve an almost unlimited number of Wang computer and word-processing systems at a data-transmission rate of up to 12 Mb/s. Each system links to the WangNet via a cable interface unit, which will cost $3,800 and is scheduled for October 1982 delivery.

The Wang Band is a resource-sharing facility, Rosenberger asserts. "Different Wang systems will be able to share files, documents, and peripheral devices, and all the systems can share products like Wang's Mailway electronic mail software," he points out. Further, a Wang system connected to the Wang Band can become a gateway to outside networks. Wang plans for all its systems, such as 2200 and VS systems, to support the X.25 protocol and IBM's System Network Architecture, as well as other protocols.

Communications between systems on the Wang band take place under distributed control, employing the CSMA/CD arbitration standard proposed by the Institute of Electrical and Electronic Engineers in its standard 802 for local networks.

Wang Laboratories Inc., One Industrial Avenue, Lowell, Mass. 01851. Phone (617) 459-5000 [338].

Computers & peripherals

Big guns fire off small machines

DEC, DG, and Xerox assault small-business market with $7,000 computers

by James B. Brinton, Boston bureau manager

Almost simultaneously, three major electronics firms—Xerox, Data General, and Digital Equipment Corporations—have unveiled contenders for the retail small-business computer market. Though their prices span a narrow range of about $6,000 to about $7,200 in typical configurations, the systems are quite different. All are microprocessor-based and include floppy-disk storage, cathode-ray-tube displays, and keyboards, but that is where the similarities end. In each case, software is more or less unbundled; in some cases there is a broad choice of printers, peripherals, and communications capabilities.

Xerox's 820 is a Z80-based, 8-bit machine with 64-K bytes of MOS main memory, dual 92-K-byte 5¼-in. floppy-disk drives, display, and keyboard [*Electronics*, June 16, p. 33]. Operating system and software are available at extra cost, as is a printer. With a 40-character-per-second Diablo 630 letter-quality printer, CP/M operating system, and a $500 word-processing package, the 820 sells for $6,595 in single units. Discounts on the unit are expected.

Next in line. On June 19, Data General entered the lists with its Enterprise 1000, a unit based on microNova architecture. First of a projected family of small-business machines, the 1000 is a 16-bit unit with 64-K bytes of MOS main memory, 716-K bytes of bulk storage in two 5¼-in., double-sided, double-density floppy-disk drives, keyboard, CRT, and a 150-character/s dot-matrix printer. The price for this configuration, including the system's newly developed operating system, Enterprise OS, is $7,195. Again, company spokesmen are expecting significant discounting from this price.

Yesterday, Digital announced its DECmate line of small-business systems—microprocessor versions of its PDP-8 architecture, but with an enhanced instruction set. The DECmates, or model 278s, are 12-bit machines, have 32-K words of user-accessible main memory (the equivalent of more than 49-K bytes), and use 8-in. floppies, with each dual drive capable of storing more than a megabyte. The system price of $6,795 for the model 278-AC also includes a 30-character/s dot-matrix printer. The 278-AE offers a 180-character/s dot-matrix printer and costs $8,195; the 278-AH comes with a 45-character/s letter-quality printer and sells for $9,195.

The DEC machine also is available in a minimal configuration as the VT278-AH. For $3,900, the unit comes minus mass storage and some of the communications frills of the larger 278s and can act as a down-line-loadable intelligent terminal.

Software variety. In its software aspects, DECmate is more complex than its competitors. Application software packages—and there are many—vary widely in price: some are free, and others cost as much as $4,500. But DEC's software may be one of the 278's strong points. First, there is a lot of it. DEC itself will sell more than 16 applications packages immediately, and there is a vast reservoir of PDP-8 software available from a variety of other sources. This body of software, proven in years of use with PDP-8 class computers, should be almost totally bug-free, according to Gary M. Cole, DECmate product manager.

The software is also transportable. Users of earlier systems like DEC's WS-78 can move their existing packages up to the 278, and in some cases, 278 software is upwardly compatible with systems as large as the

Software ready. The DECmate 278 is a microprocessor-based version of the firm's 12-bit PDP-8 architecture, so it benefits from a large body of bug-free software.

company's 32-bit VAX series.

Unless the user is doing development work, Cole says he need never buy an operating system as such. DEC's application packages subsume any necessary operating-system software. Thus if a user buys the company's $500 word-processing package, he need only bootstrap from disk into main memory and run. Also, much of the software is designed to be capable of instructing the buyer in its use; for especially complex software packages, DEC supplies documentation and audio cassettes as instruction aids.

OS options. For development applications, DEC offers two operating systems and support packages. The OS/78, at $810 to $1,600, supports Basic, Fortran IV, and an assembler; it also allows some limited file transfer to the RT-11 operating system, and thus to DEC's PDP-11 computers. The COS/310 operating system supports the company's tailored version of Cobol, called Dibol, in a new version, Dibol-11, that allows software portability all the way up to computers as large as the VAX line.

The office-support and personnel-oriented applicant-tracking packages are free for the asking to the buyer of a word-processing system. On the other hand, users can spend up to $4,500 for software as complex as DEC's construction-management package; this price includes training and support. Typical accounting software costs about $900 per package, and packages are available for accounts receivable and payable, inventory and invoicing, general ledger, and payroll.

The 278 has been designed to fit communications applications as well, suiting it to remote-node installations in large corporate environments. The unit nominally supports serial byte-asynchronous communications at rates from 50 to 4,800 b/s; higher speeds are possible with special software. The unit also is compatible with RS-232-C and RS-423 communications standards. Finally, it can act as a terminal either directly or via a modem.

Though not directly compatible with the firm's DECnet III [*Electronics*, Feb. 14, 1980, p. 183], the 278 is expected to be used as a terminal with PDP-11 and larger computers. Thus, through these larger nodes, it can sneak aboard a DECnet.

In appearance, the unit is similar to DEC's hot-selling VT100 display terminal and may offer the most flexible display capabilities among its newfound competition. Like the others, it uses a 12-in. CRT, but it displays either 24 lines of 80-column text of 14 lines at 132 columns—a limit imposed by the 24-K display memory. It offers upper and lower case, boldface, blinking, underlining, and reverse video.

New enterprise. Data General's Enterprise 1000, using a 16-bit microNova CPU, could be the most powerful of the three machines. Some users may not notice much difference, but while add time for the DECmate is 2.8 μs, that for the 1000 is 2.4 μs.

The 1000's keyboard is similar to that of the DEC unit, having 83 keys, a 14-key pad for numerical and control functions, and a number of definable keys. DG describes its keys as user-definable; DEC's Cole says that its machine's keys are automatically defined as a new applications program is loaded.

DG's Enterprise OS operating system is not now compatible with its other OS systems, but Patrick Dodds, small-business systems marketing manager, says a version is on the way that will offer compatibility with the firm's larger machines.

The Enterprise 1000 supports synchronous or asynchronous communications at up to 19,200 b/s. The system is programmed both in run-time and in business Basic. Currently available software includes a package for accounts receivable and one for order entry and inventory control. In coming months the firm expects to announce a word-processing package, among others.

Software, excluding the operating system, is unbundled. The two packages at present available each retail for a suggested price of $1,000. Though this is far higher than most of the CP/M-based software for the Xerox 820, and somewhat more expensive than some of DEC's 278 software, DG spokesmen note that the quality of CP/M software and support can vary widely. And training may be non-existent.

Training could be Enterprise's long suit. A video-disk-based in-

Training available. Data General's Enterprise 1000 is based on a 16-bit microNova processor. Video-disk-based instructional systems will be available at retail outlets.

structional system to be installed at each retail site, according to Herbert Richman, DG executive vice president, "is designed to take the user step by step, at his own pace, through each of the system's accounting packages."

In addition to training, the company is emphasizing reliability. "If a small outfit puts its whole company's records on our machine and it crashes, that's the last sale we make to them," says a DG source. The company has included a read-only-memory–based diagnostic system that is triggered at turn-on, before the operating system is booted into random-access memory. Thus it is both insurance, safeguarding against lost data, and, occasionally, a trouble-shooting aid, cutting downtime.

DEC's 278 also includes diagnostics and tests that exercise memory and the central processing unit at power-up. According to DEC's Cole, the routines may also be called up at any time from the 278's keyboard for troubleshooting.

Delivery of the Xerox 820 through retail channels is expected to begin immediately. DEC is targeting August availability for its DECmate 278. DG plans to have the Enterprise 1000 available by September in the U. S., later outside the country.

Fujitsu too. TRW-Fujitsu is another voice in the chorus, introducing a competing desktop computer this month. Altered from the Fujitsu 9450 system for use in the U. S., the TFC-3450 is a 16-bit machine based on Fujitsu's own L16A microprocessor running at 4 MHz. A system with an 80-character-by-25-line CRT, 640-K bytes of floppy-disk capacity, and an 80-character/s 80-column printer will sell very near the price of the DEC, DG, and Xerox entries, though exact figures are not yet available. The TFC-3450 has an automatic dial-up and answer communications ability and is being targeted for distributed data-processing environments. Software is in business and scientific Basic and assembly language.

Data General Corp., 4400 Computer Dr., Westboro, Mass. 01580 [421]

Digital Equipment Corp., Continental Boulevard, Merrimack, N. H. 03054 [422]

The TRW-Fujitsu Co., 9841 Airport Blvd., Suite 620, Los Angeles, Calif. 90045 [423]

Xerox Corp., Office Products Division, 1341 West Mockingbird La., Dallas, Texas 75247 [424]

Video-disk interface gives power, flexibility to player

The DiscMaster 1000 is an RS-232-C interface for the Pioneer VP-1000 and DiscoVision PR-7810 laser video-disk players. This unidirectional, serial interface enables any mainframe, minicomputer, or microcomputer to control the playback of videodisks, making the player a more powerful and flexible device than it is when controlled by its built-in microprocessor. Instead of permanently mastering the disk playback program on the disk platter for downloading into the intelligent player's microcomputer, users can

write, debug, and continually modify their playback program using a high-level language. The DiscMaster 1000 includes all necessary cables, connectors, and a power supply. No modifications to the video-disk player or computer are required. The single-unit price is $395 and deliveries are immediate.

New Media Graphics Corp., 139 Main St., Cambridge, Mass. 02142 [367]

Digitizer's 1-in. border reduces active-area waste

A line of digitizer tablets for entering graphic data surrounds its specified full active areas with a 1-in. border that eliminates the waste of active area for user-definable menu selection, yet may be used for those applications requiring oversized media and no more than ±0.010 in. accuracy at the edge.

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Houston Instrument, One Houston Square, Austin, Tex. 78753. Phone (512) 837-2820 [363]

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Members of the S series are available in one of three standard print formats: bar code with interpretation line plus zero, one, or three lines of free text. The printers are offered for Code 39 (9.4 characters/in.) or Codabar (at 10 characters/in.). Printing from a rotating drum, the S series can mark up adhesive paper labels, tags, or durable plastic label stock. For paper labels, a dispensing option strips a completed label from its backing.

In single quantities, the printers start at $5,945, with a 20% original-equipment manufacturer discount available for quantities of 2 to 9. Delivery is from stock.

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Microcomputers & systems

68000 on Multibus can link to PDP-11

Microcomputer is offered as board, in boxed system, or as development system

The CMS-16 microcomputer series from CM Technologies Inc. is not the first system to put the 16-bit 68000 microprocessor on the Multibus interface [*Electronics*, April 21, p. 215]. However, the company is the first to offer a range of products, from the bare central-processing-unit board to turnkey systems, that link the 68000 through the Multibus. It is also the first to offer a Digital Equipment Corp. PDP-11 link and to use Microsoft's Xenix operating system on such a product.

At the original-equipment-manufacturer systems-design level, there is the CMT-CPU, a CPU board containing the 68000, 64-K bytes of dynamic random-access memory and a Multibus interface. Priced at $2,350 in single-unit quantities, it features a 24-bit address bus, 8- and 16-bit data transfer, memory-mapped input/output, and seven vectored interrupt levels. The CPU board also has two sockets that can accommodate up to 16-K bytes of erasable programmable read-only memory. The board operates at 4, 6, or 8 MHz for compatibility with peripherals and other processors in a multiple-master or master-slave environment.

The CMT-CPU will start being delivered in July; the second product, the CMS-16 will be shipped in August. The CMS-16 incorporates the CPU board in a nine-slot Multibus card cage along with a four-channel synchronous-asynchronous serial I/O module. In this version, the E-PROM sockets are occupied by monitor firmware. Using the open slots in the card cage, the CMS-16 can handle up to six additional modules, including an intelligent controller that can mix up to four Winchester or floppy-disk drives. Single-unit pricing on the CMS-16 is $4,995.

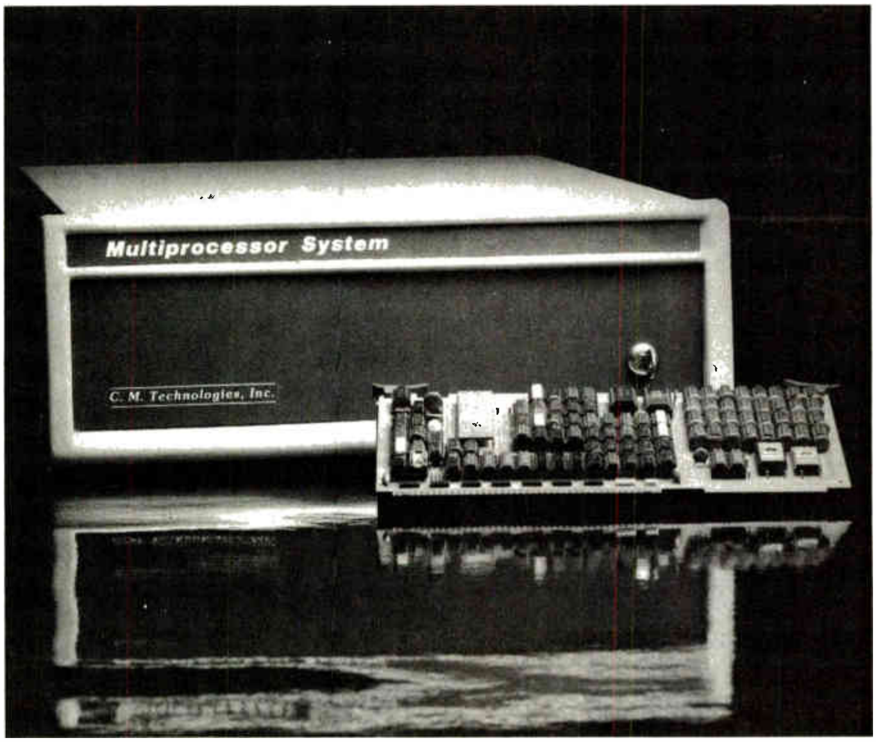
The third product, the CMS-16/DS1, provides the CMS-16 with hardware plus some additional firmware that allows the unit to handle the uploading and downloading of code developed on any PDP-11 minicomputer. It also contains the necessary cabling to have an RS-232-C interface. The DS notation stands for the development system that allows the unit to be used as an in-line processor between the user's terminal and a PDP-11. The PDP-11 can be operated by the terminal with the development system in a pass-through mode, or the development system can be operated by the terminal, or the PDP-11 can communicate directly with the 68000 through the Multibus.

Otherwise. In a second configuration, the 68000 in the development system can act as a back-end processor running concurrently with the PDP-11 host. The development system will be available in September at $6,995 in single-unit quantities. At the end of the year, cross-compilers for C, Pascal, and Fortran should be available as separate products.

Adding a Z80-based card to the cage creates a fourth product, the Multiprocessor System. In this application, the Z80 board is a peripheral controller or a separate processor operating under CP/M. Using a built-in 8-in. Winchester disk drive, the Multiprocessor System has 11 megabytes of unformatted storage as well as a dual-sided double-density floppy-disk drive in a separate storage-subsystem cabinet. The Winchester drive is a Shugart SA 1000 offering 10 megabytes of storage, and the floppy-disk drives are the Shugart SA 850/800 series, which offer 1 additional megabyte of removable storage.

In addition to the two processor boards, the Multiprocessor System includes a 128-K-byte dynamic RAM card and an intelligent disk controller. The controller allows direct memory access, error recovery, and formatting. Including a resident assembler and debugger, the single-unit price for the Multiprocessor System is $19,450. Deliveries are expected to start in September.

The Multiprocessor System is designed to be upgraded to the Microsoft Xenix multiuser operating



system, which should become available by the end of the year. Under Xenix, the CMS series 16 can be configured with eight remote stations.

These four products are the first to be introduced by the two-year-old CMT, which is active in development and technical support of 8-bit microprocessor products in Asian markets.

CM Technologies Inc., 525 University Ave., Palo Alto, Calif. 94301. Phone (415) 326-9150 [371]

Watch chip drives dot-matrix LCDs

C-MOS chip runs off watch cell for a year and a half, drives LCD with 96 elements

The 1270 complementary-MOS 4-bit microcomputer is based on the design of AMCC's 1259 microcomputer [*Electronics*, July 17, 1980, p. 143]. Like the 1259, the 1270 draws only 3 μA from a 1.5-V supply, taking a year and a half to exhaust a standard watch cell. But the 1270 is capable of driving a 96-segment liquid-crystal display using two-level multiplexing and thus is able to drive dot-matrix LCDs. The 1259 does not have this multiplexing capability and can directly drive only 48 LCD segments.

The added circuitry includes an extra bus decoder and latch for each of the chip's 48 LCD-drive outputs. The outputs have also been given dc drive capability—each can be tied to any of three voltage levels. A voltage-halving circuit, which makes the chip able to operate from a 3-V lithium battery, has been added; the chip already had a voltage doubler. The total of 96 bus decoders for the outputs are set up using mask-programmable logic. Finally, an extra line has been added to the strobe decoder, to double the number of possible strobe times.

Communication. The dc drive capability adds a further possibility—that of linking 1270s to drive displays with more than 96 segments. Output lines can be connected to the five inputs normally used for chemical-button inputs.

The entire chip is designed around programmable logic arrays, which can be customized with a single mask for various applications. Its program control, mode control, and arithmetic unit all utilize PLAs. But because of the relatively few program steps available, the approach is not suited to every task. Those it does suit include watches and clocks, hand-held games and toys, remote timers, and sequential controllers.

The 64-pad microcomputer is normally supplied in chip form for mounting on hybrid substrates. It has a 32-by-4-bit random-access memory and requires an external 32.768-kHz crystal. The 1270 will be available within 30 days and will be priced at less than $5.00 each in quantities of 25,000.

Applied Micro Circuits Corp., 10626 Bandley Dr., Cupertino, Calif. 95014. [371]

Single-board computer manages memory

The FT-86M and FT-86M/FP single-board computers are members of Forward Technology's Gateway series of Multibus-compatible 16-bit computers. The FT-86M's design is based on the Intel 8086 16-bit microcomputer. The FT-86M/FP incorporates both the 8086 and Intel's new 8087 numeric data processor, which can perform floating-point calculations. The units support Digital Research's CP/M-86 operating system; in addition, the firm offers a proprietary operating system written in Forth.

Up to seven users are supported by the unit's memory management and protection features. Both computers have 4-K bytes of user-programmable memory, and four sockets are included for up to 32-K bytes of read-only memory. Also, two RS-232-C programmable communications ports are provided, with each capable of handling asychronous formats, synchronous byte-oriented protocols, and bit-oriented protocols. The computers meet all specifications of the IEEE proposed P-796 bus standard. The FT-86M is $1,950, and the -86M/FP runs $2,950, with 25% discounts offered on quantity purchases. Delivery is in 30 days.

Forward Technology Inc., 1440 Koll Circle, Suite 105, San Jose, Calif. 95112. Phone (408) 293-8993 [373]

RAM boards fit LSI-11, Multibus-based computers

Two series of standard random-access memory modules will expand the memory capacity for LSI-11 and Multibus-compatible computer systems. Offering 128-, 192-, and 256-K bytes, the TMM10010 series is a second-generation version of the TMM10000 series. Improved features include the capability to operate at the maximum Q-bus speed, with a typical read access time of 175 ns, write access time of 75 ns, and a read or write cycle of 360 ns. Starting addresses can be selected on 4-K-byte boundaries.

The Multibus-compatible TMM-40010 series is available in 64-, 128-, 256-, and 512-K-byte versions. This series also boasts low access times, with a typical read access time of 325 ns, a write access time of 110 ns, and a read or write cycle of 710 ns. The TMM10010 will be available in September, with prices of from $1,315 for the 128-K-byte version to $3,290 for the 256-K-byte version with parity controller.

Pricing for the TMM40010 series, now available, ranges from $1,845 for the 64-K-byte model to $4,000 for the 256-K-byte card.

Texas Instruments Inc., Integrated Memory Systems Marketing, P.O. Box 1443, M/S 6404, Houston, Tex. 77031. [374]

NEW BIOMATION K500-D

Introducing the world's fastest logic analyzer. Incomparable.

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Now you can dramatically shorten the debug cycle in high-speed random and stored program logic design with our powerful new 500 MHz, 8-channel K500-D. With state-of-the-art 16-bit microprocessor control, 2K static RAM memory and GPIB interface for fully-automated operation, the K500-D is the industry's most advanced integrated test tool for the digital designer.

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Our probes were designed for high performance to cope with the speed and complexity of large systems, as well as complement the super high speed of the K500-D. Now, with 6-foot probes and hybrid buffering circuits in each probe tip, you can conveniently debug even the largest systems with minimum disturbance. With our unique scroll mode, you can probe hard-to-reach test points individually and build your timing diagram one channel at a time.

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Our new K500-D is even easier to use than our best-selling K100-D . . and that's saying something. Its status and data displays permit easy, flexible programming and data analysis. You can expand horizontally X10, X20, or X50, and specify the display format in binary, octal and/or ASCII.

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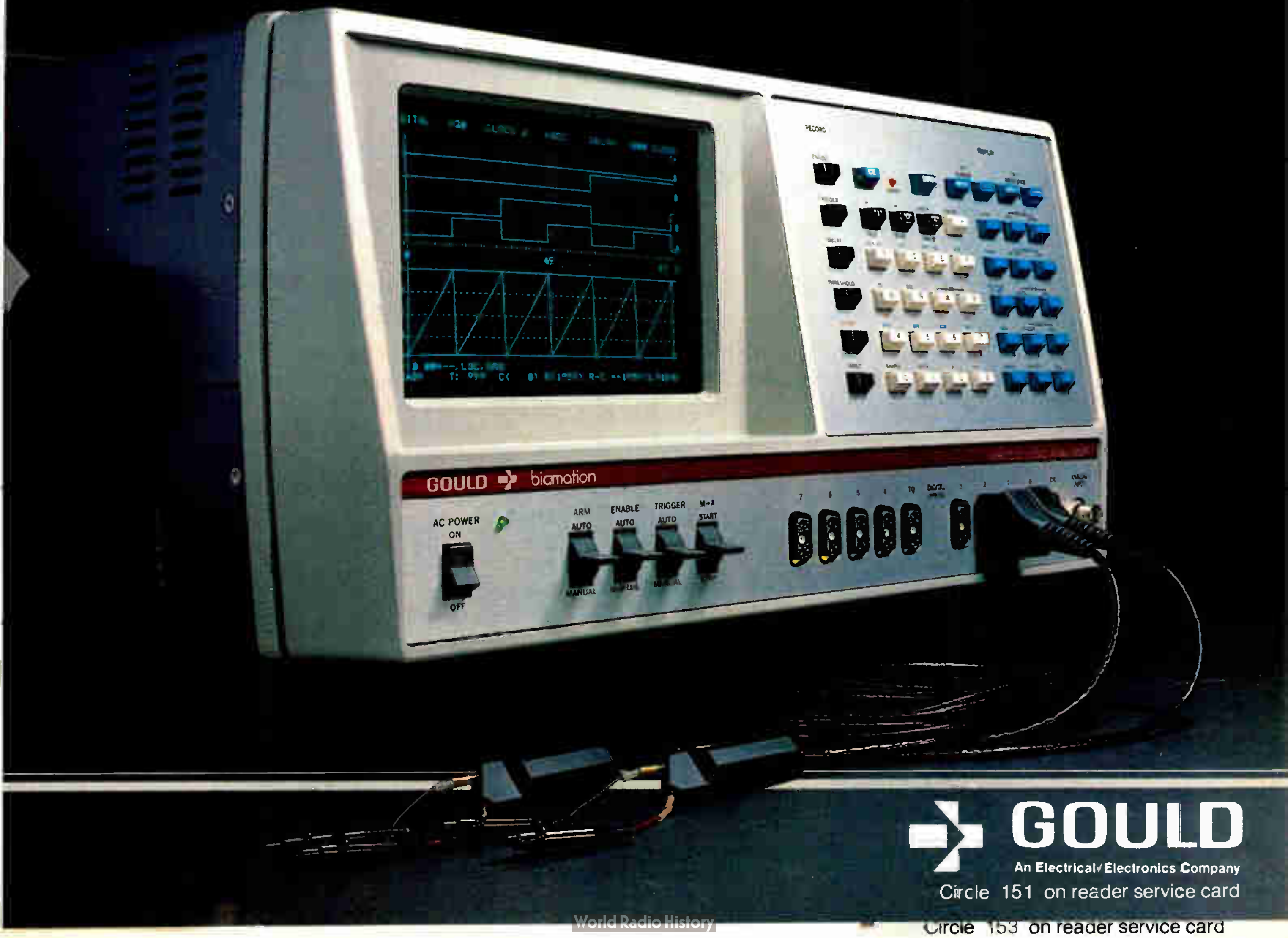
Any designer debugging mainframes or super-minis deserves full details on this revolutionary new logic analyzer. Write Gould, Inc., Biomation Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050. Or call (408) 988-6800.



GOULD
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Circle 151 on reader service card

Circle 153 on reader service card

Packaging & production

Tool keeps track of wrapped turns

Insulation-slitting Wire-Wrap tool stops when it has applied the selected number of turns

The tedium of counting turns in the course of wiring Wire-Wrap contact posts is made unnecessary by a new tool. Internal logic in the P184-7 counts the number of turns wrapped onto a post and stops the wrapping when a preselected count is reached—an ability that is proving useful for moderate-level production and prototype wiring in field trials.

"Many customers have asked us for a more accurate method of placing the required number of turns on a post," says Floyd Hill, marketing vice president of Vector Electronics Co. This need is most critical in the common daisy-chain routing of insulated wire, in which each post has two connections wired to it. Military specifications are particularly demanding, calling for a specific number of wire turns on each post, he points out.

Faster, too. The Vector tool's internal circuitry senses and counts wire turns, limiting them to the number selected—from three to nine—by setting a switch on top of the tool. (The counter may if necessary be bypassed.) The operator simply selects the number of turns, places the tool's bit over the post, and presses the trigger. A magnet affixed to the shaft passes dual sensors that signal each revolution. The average time for each termination is less than 1 second—typically four times as fast as conventional techniques, according to the company.

Vector regards the turns counter as a pronounced improvement on its Slit-n-Wrap tool line. In this series, a patented design slits the insulation automatically only during wrapping, not during routing. A knife-edge on the tool tip makes the slit, exposing the conductor for a gas-tight, metal-to-metal contact with the post. A notch in the two-piece wire-grip housing retains the end of the wire, so that the operator need not hold the wire end while starting to wrap it but can concentrate solely on its placement.

The wire spool on the tool can carry 300 feet of 28-gauge wire, enough for 1,200 daisy-chained or 900 post-to-post terminations with seven-turn wraps and an average lead length of 2 in. An adjustable regulator on the spool keeps tension constant. Tension can be checked with a 3-oz weight supplied with the tool or with a spring scale. Contact resistance is 0.003 to 0.007 Ω and pull strength is 4 lb. The terminations meet performance standards of MIL-STD-1130A, says the firm.

The pistol-grip tool measures 11.25 by 1.8 by 4 in. deep and weighs 13 oz. Power is supplied from a 117-V, 50-to-60-Hz converter. The 28-gauge Tefzel-insulated wire is available from Vector in six colors: blue, black, green, red, white, and yellow. Tefzel has a dielectric constant of 2.6 and a dielectric strength of 450 V/mil.

Vector's P184-7 tool costs $198, with 300-ft wire spools priced at $14.95 each. The set-screw-mounted bits are guaranteed for at least 7,000 seven-turn connections. Replacement bits are $10.60 each. The tools, now in production, are immediately available.

Vector Electronics Co., 12460 Gladstone Ave., Sylmar, Calif. 91342. Phone (213) 365-9661 [391]

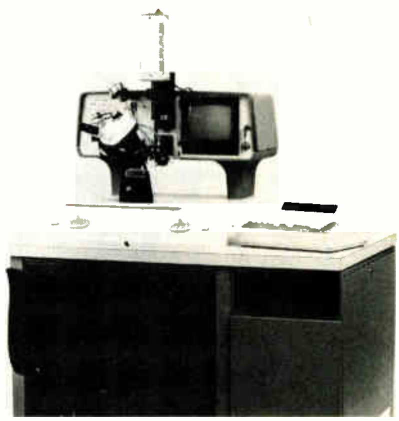
Wire bonder is easy to program

Automatic wire-bonding unit for hybrid-circuit production has time-saving software

An automatic wire bonder for hybrid circuits that provides increased throughput and a lower error rate without needing complicated and time-consuming programming has been developed by Hughes Industrial Products division. The HMC-2460 also offers a pattern-recognition option that further enhances its performance over manual systems.

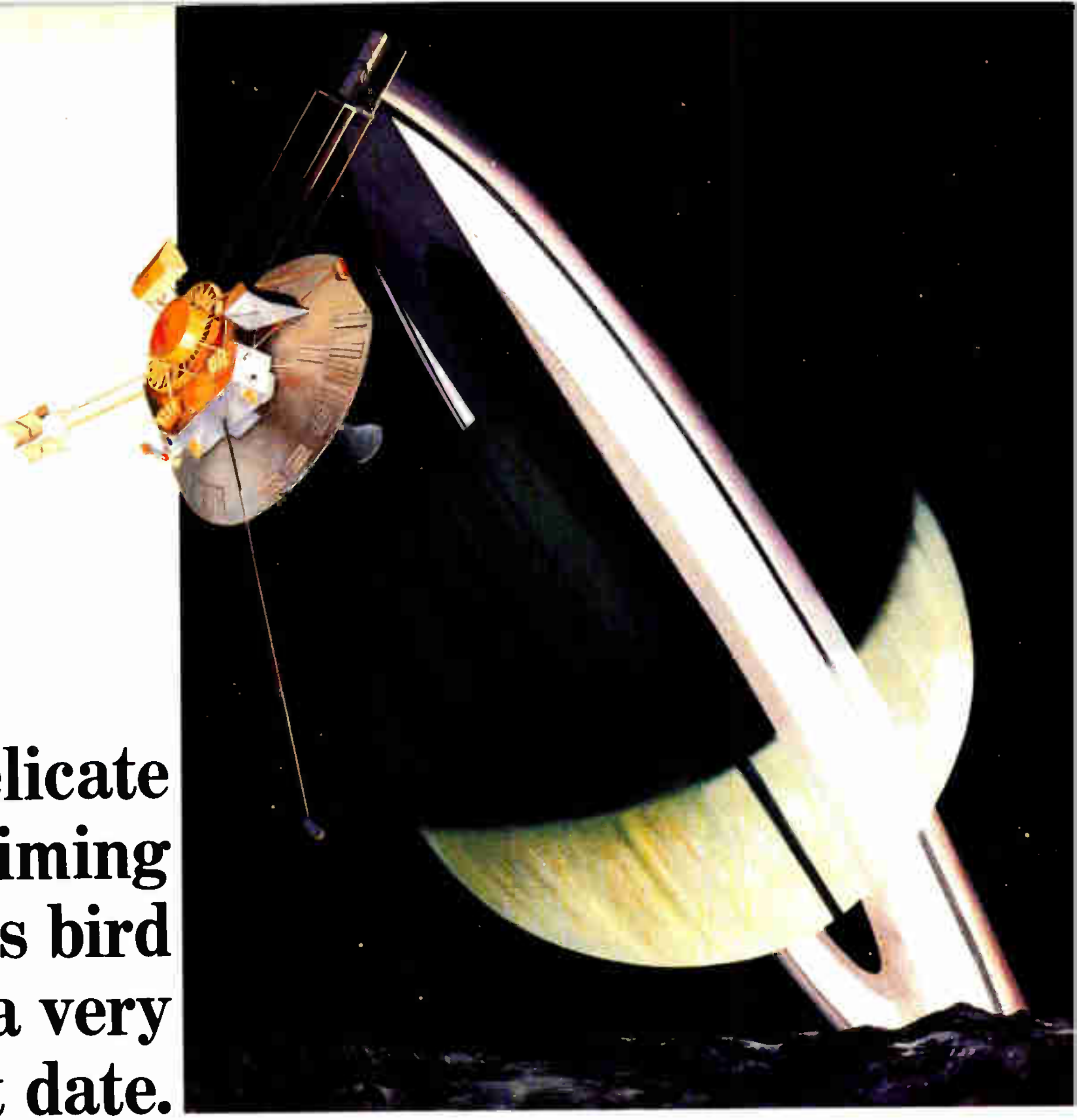
The HMC-2460 will handle a 25-to-30-package hybrid in about 8 minutes, compared to the 40 minutes or so of a manual process, according to Pete Bullock, manager of production equipment products. With pattern recognition, time is cut to about 3 minutes. Cycle time is 350 ms per wire at a wire length of 0.025 in.

The time savings stem mainly from a variety of software operations. Programming the unit is easier because the software is designed for those familiar with wire bonding. Step-and-repeat functions for multiple chips need not be programmed separately, and programming of po-



sitions is done by exception, so that only wires that do not follow set patterns require specific instructions.

The interactive system queries the



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- Military nomenclature: TD-1335/V (Model FE-5450A) and TD-1251/U (Model FE-5440A).

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Circle 155 on reader service card

user, so little programming expertise is required. Operator-programmed functions include bond locations and height, loop shape, electronic-flame-off gap and discharge time, and bond forces and times.

Provident. In operation, the system looks ahead to determine the length of wire needed to form the ball at the next location. Speed of action can be determined by software, so that the system will move more quickly during repetitive actions and slow down for complicated bonding patterns. The wire set of each die is handled as a separate program to simplify software.

The head moves in a purely vertical motion, giving it more accurate height parameters than units that pivot on a hinged arm. Its vertical-motion capability of 0.250 in. is becoming increasingly important as chip-height variation increases as a result of new wafer processing techniques. The three-axis, servo-driven bond head uses thermosonic gold-ball bonding, with bonding wire sizes ranging from 0.0007 to 0.0015 in. The X-Y positioner resolution is 0.0001 in.

Once the wire positions are properly programmed in, the system will not misplace wires, so yield increases dramatically over manual units. Although beta tests have not yet provided solid figures, Bullock feels the increase may be as much as 50%.

Instructions and data for the various operations are stored in random-access memory and on floppy disks. The standard drive is a single-sided, single-density Shugart drive that holds up to 60 patterns or 32 dice. An optional single-sided, double-density Shugart drive increases capacity to 240 patterns or 120 dice. Also stored on disk is a self-diagnostic program. The system will run 15 test programs including routines for floating-point hardware, RAM, and erasable programmable read-only memory, X-Y table tests, and X-Y-Z-axis interface tests.

Perspicacious. The HMC-2460 will recognize the different patterns of chips supplied by more than one vendor and will stop the machine during manual operation if a component from a second source uses different bond pads. The operator can then summon up the program for the component and continue. In the pattern-recognition mode, the system will scan its memory and continue operations on the alternative chip if that pattern is in memory.

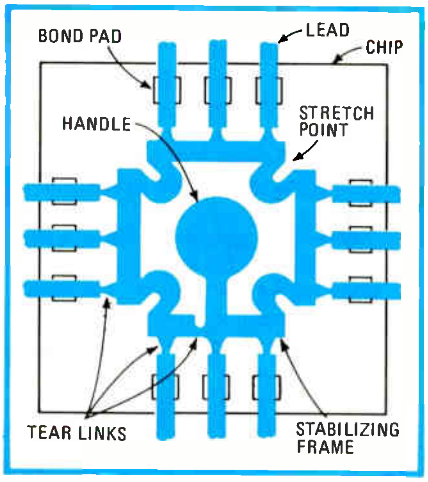
Forgiving. Focusing requirements are very forgiving thanks to a digitized video system that has better depth of field than do most photomultiplier systems, Bullock says. The digitized system is also less sensitive to light changes. The pattern-recognition option requires the installation of a five-board set.

Pricing for a single HMC-2460 ranges from $50,000 to $70,000. Delivery is in 90 days.

Hughes Aircraft Co., Industrial Products Division, 6155 El Camino Real, Carlsbad, Calif. 92008. Phone (714) 438-9191 [392]

TAB scheme improves yields, stabilizing leads with a frame

A technique developed by International Micro Industries substantially increases yield in high-lead-count (40 or more leads) tape automated bonding to integrated circuits. At these high counts, it is difficult to maintain good lead-end stability at the inner ends of the tape's leads. Inner-lead bond yield can be as low as 40%, according to Thomas Angelucci, president of IMI. With the firm's tape technique, called HY-TAB, 90% to 95% inner-lead bonding yields are possible, he says.



Pull here. IMI's HY-TAB tape-automated bonding stabilizes the inner ends of the leads with a copper frame that is removed after bonding by pulling the central handle.

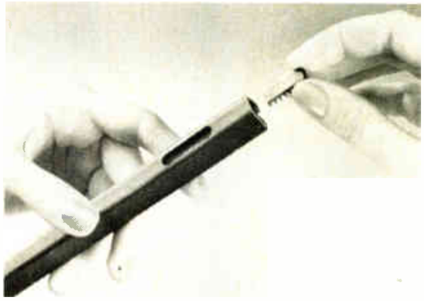
HY-TAB brings to the scene a removable copper frame that connects all the tape's inner leads (see figure), stabilizing them and preventing them from bending out of the plane or from side to side. At the end of each lead is a narrow tear link that locates the separation made when the frame is pulled out. When the handle in the center is pulled after bonding, the links break sequentially and the frame comes away. Each bond gets a pull test when the frame is separated from it, and the frame protects the tape's leads during handling and shields sensitive ICs from electrostatic charges that may be present during bonding.

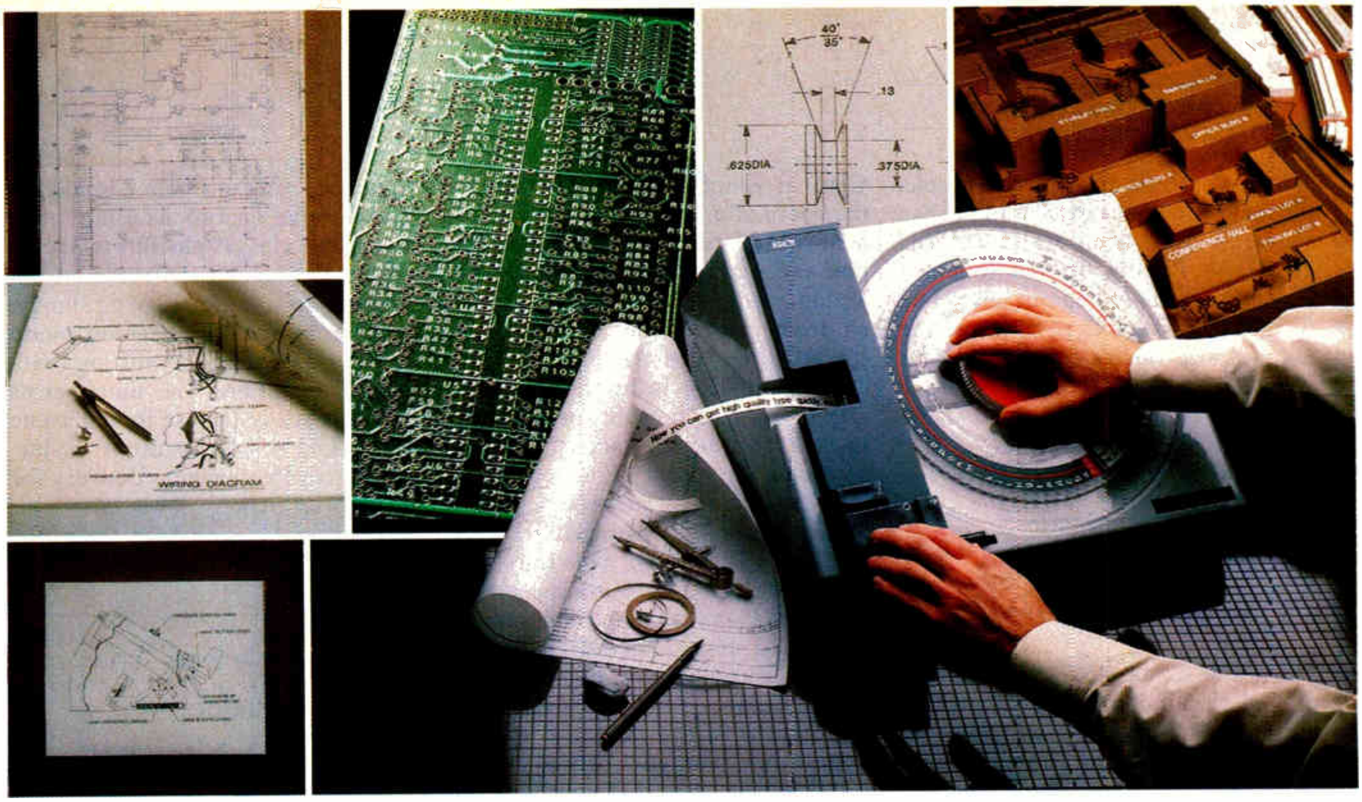
IMI will not manufacture HY-TAB tape itself, but seeks to license the concept to tape manufacturers.

International Micro Industries, P. O. Box 604, Cherry Hill, N. J. 08003. Phone (609) 424-3112 [400]

Shipping tubes shield static in excess of 20,000 V

New static-shielding shipping tubes provide the static and physical protection needed in transporting and handling dual in-line packages. Velostat No. 5550 and 5551 accommodate standard 300-mil and 600-mil packages, respectively, and can be used on most automatic insertion equipment. A molded-in slot in each tube permits inspection of devices. The tubes have volume resistivity of less than 400 Ω-cm, offering protec-





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Kroy lettering comes in twenty different typestyles, (including Microgramma and Helvetica), and a wide range of sizes from 8-point to 192-point (1/16 to 2 inches). Typestyles and sizes depend on which Kroy lettering machine model is used.

There are four types of specialized Kroy lettering supplies. *Diazo* minimizes ghosting, or shadow, during diazo reproduction. *Photo-quality* provides sharp edgeline definition (at up to 200% enlargement) for photo reproduction. *Labeling* and *All-purpose* are suited to a wide variety of lettering projects. Like all Kroy lettering tape, they adhere quickly and easily to virtually any clean, dry surface.

There are five Kroy lettering machine models currently available, including the deluxe Kroy 80™ lettering machine pictured here. Suggested retail prices range from $395 to $695.

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1546

Circle 157 on reader service card

tion from static fields from people, polystyrene packing, and other sources—even when static exceeds 20,000 V. Pricing for the standard 25-in. tube is based on quantity. The 5550 ranges from 49 to 84¢, and the 600-mil size ranges from 55 to 89¢ Delivery is two to three weeks after receipt of order.

3M Company P. O. Box 33600, St. Paul, Minn. 55133. Phone (612) 733-5755 [394]

Printed-circuit connectors are available in 16 sizes

The TRW Cinch 252 series flexible printed-circuit connectors are available in 16 sizes and straight- or angle-contact configurations. Bellows-type contacts permit smooth insertion and withdrawal of flexible printed circuits and maintain reliable continuity between contacts and circuit surface without damage.

The connectors are rated at 500 V ac at 3 A and withstand 1,000 V root mean square for at least one minute. The insulation resistance is 1,000 MΩ or more, and contact resistance is 20 mΩ or less. The specified temperature range is $-40°$ to $+100°C$. The connectors have from 5 to 27 contacts, all on 0.10-in. centers, accommodating flexible and ridged pc boards with thickness ranging from 0.004 to 0.015 in.

In 50,000-unit quantities, pricing is 0.01¢ per position for a 14-position straight-contact connector and 0.0086¢ per position for a 27-position straight-contact connector. Angle connectors are similarly priced. Delivery takes from four to six weeks.

TRW Cinch Connectors, 1501 Morse Ave., Elk Grove Village, Ill. 60007 [395]

Multilayer wiring board survives at over 200°C

A new polyimide planar printed-wiring board that features multilayer density is capable of withstanding operating temperatures in excess of 200°C and vibration of 100 g^2/Hz. Clad in stainless steel and copper, the board offers versatility of component installations and interconnection and makes changes possible. A Teflon-insulated nickel wire is bonded from pad to pad by use of a special stitch-wire machine. Component installation is by direct insertion or by insertion into low-profile sockets for dual in-line packages, nonweldable socket pins, or hole-tight devices. A card can be designed with any or all pad patterns to handle devices with pin rows on 0.3-, 0.4-, 0.6-, or 0.9-in. centers, committed or noncommitted supply or ground lines, expandable edge-finger or airborne type input/output, and ground-strip or flat-ribbon cable. Pricing, which depends on configuration, averages between $50 and $200 per board. Delivery is in six weeks, or sooner if the configuration is off the shelf.

Multi-Link Division of Odetics Inc., 2191 South Dupont Blvd., Anaheim, Calif. 92806 Phone (714) 634-1178 [396]

Pc board repair tool has finger-actuated vacuum pump

The Pace Micro is a self-contained portable system for repairing printed-circuit boards in the field. Compact in design, it weighs only 4½ lb and can be carried in a tool box. A single tool performs both desoldering and soldering operations using interchangeable tips. It has full temperature regulation and can operate from either an ac line or a 12-V dc supply. Its internal, fast-rise vacuum pump is finger-actuated, permitting one-handed operation. The unit warms up and is ready for use in under one minute and is safe for use with static-sensitive components. Delivery for the $395 unit takes six weeks.

Pace Inc., 9893 Brewers Court, Laurel, Md. 20810. Phone (301) 490-9860 [398]

Programmable wafer saw has rotating fixture

A special wafer-cutting saw with a programmable electric feed mechanism and a programmable ingot-rotating fixture works with precision on hard semiconductor materials such as gadolinium-gallium-garnet, sapphire, ruby, quartz, optical glass, and ceramic. The programmable electric feed system optimizes cutting rates on the basis of blade position in the cut. A number of programs for cutting are provided in the saw's software. Feed rates are variable for 0.20 to 3.0 in. per minute with an accuracy of within ±1%. By rotating the ingot-mounting fixture according to a predetermined program, heat build-up at the point of cutting can be minimized, thus reducing wafer surface damage and increasing diamond blade life up to seven times. The rotating mounting fixture accepts crystals up to 5 in. in diameter and 16 in. long and can rotate at speeds of 0.15 to 150 rpm in either direction. Available on new saws, it can also be retrofitted.

Though the saw was developed for processing extrahard materials, it is also useful in processing silicon (with or without the rotating fixture), where it increases cutting rates and wafer quality and maximizes blade life. Modifications will allow diameters of up to 10 in. Delivery is from 12 to 16 weeks.

Silicon Technology Corp., 48 Spruce St., Oakland, N. J. 07436. Phone (800) 526-5218 [397]

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[illegible]

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E6

Circle 159 on reader service card

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- Internal self test program of all characters
- Programmable controls for:
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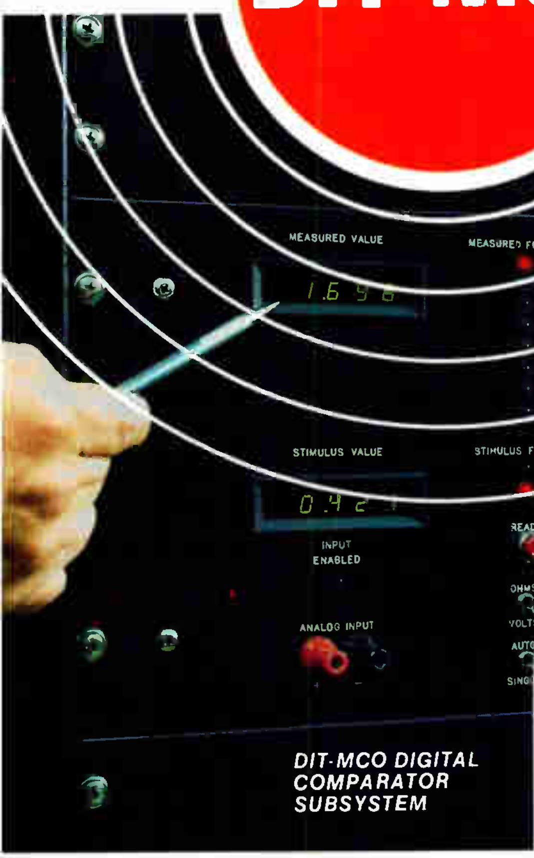

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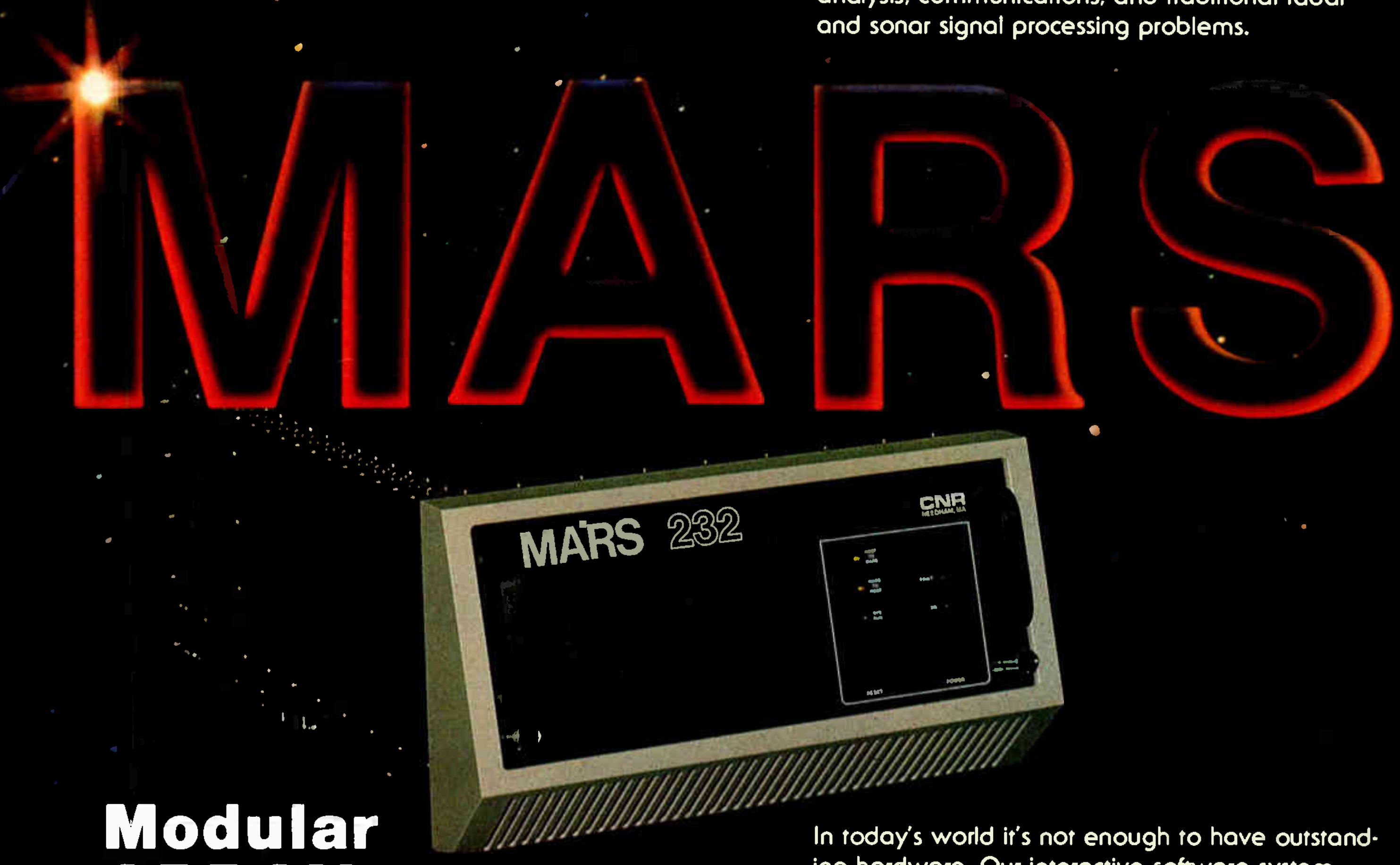

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Industrial

Microcomputer logs data on net

Preprogrammed 3870 is first in family of serially linked parts for distributed control

The first of what is to be a family of devices mask-programmed for distributed industrial control and data-acquisition applications is the SCU20. The part is a 3873 microcomputer set up to give a system event-driven data-logging capability for collecting up to 63 bytes at a time and transmitting them to the host computer over a serial communications line. It can control up to three 8-bit parallel input/output ports and five timer-counters.

The SCU2 line is being developed as a family of intelligent controllers, all of which are to be connected by serial data links. Within a year, Mostek plans to introduce three more SCU2 members. All four will be able to reside on the same serial network using a common serial protocol, says Richard Lee, microcomputer components strategic marketing manager for the firm.

"We had done market research to define the applications that are suitable for distributed control and to define the message protocol that provides effective message transmission while retaining a high resistance to errors that might end up in the stream," Lee explains. He says Mostek's work on the packaged software would represent between 6 and 12 man-months of work by a customer trying to develop his own software.

The software in the 8-bit microcomputer's 2-K-by-8-bit read-only memory, in addition to putting data into serial form, checks for errors and sets timing restrictions. The customer uses the circuit as a distributed-control building block without having to develop the software, Lee says. By using the preprogrammed unit, customers are also not restricted to large-quantity orders, he notes.

The SCU20 is designed to allow the user to network as many as 255 SCU2 devices on one communications channel; its data-transmission rate is selectable. The communications protocol used is secure and error-resistant.

Converter interface. According to Lee, the second member of the packaged-software family will be the SCU24, which will interface with analog-to-digital and digital-to-analog converters. The part is intended to eliminate many of the system noise problems that occur when analog signals are sent over long distances in noisy environments.

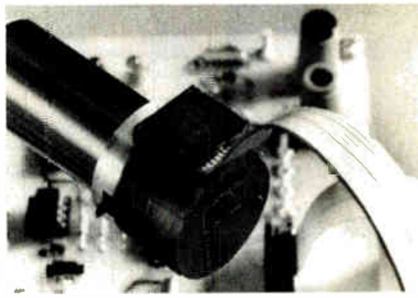
Eventually the SCU2 family of circuits will include controllers for use with both ASCII-encoded keyboards and displays and scanned keyboards and displays; a multiple–stepper-motor controller with programmable acceleration and deceleration; a controller for keyboards with common seven-wire print mechanisms; an IEEE-488 bus controller, a 16-channel analog controller, and user-programmable (through downloading) controller.

The SCU20, like the standard 3873 microcomputer, requires a single 5-V power source and is packaged in a 40-pin dual in-line package. Mostek is now taking orders for the SCU20; single-quantity price will be below $40, although exact prices will be disclosed only by distributors.

Mostek Corp., 1215 W. Crosby Rd., Carrollton, Texas 74006. Phone (214) 323-6000 [341]

500-pulse-per-revolution shaft encoder is compact

Performing at 500 pulses per revolution, the HEDS-5000 two-channel optical shaft encoder is suitable for robot, automatic handler, disk and tape drive, printer, plotter, and positioning table applications. Only 28 mm in diameter, the unit has a low-inertia code wheel and an emitter end plate. Two light-emitting diodes with molded lenses produce colli-



mated light, which passes through holes in the metal code wheel and phase plate to a pair of detectors. The design tolerates 0.25-mm shaft end play and is relatively insensitive to shaft eccentricity, LED degradation, and contamination.

The shaft encoder's digital output is compatible with low-power Schottky TTL. It requires a single 5-V power supply, operates from −20° to +85°C, and can be assembled in five minutes. Six standard hub sizes are available to accommodate most shafts, and a set of tools, designated HEDS-8900, is available for $198 in quantities of 1 to 9 to aid in the encoder's assembly. The HEDS-5000 is priced at $80 each in quantities of 10 to 99; delivery is from stock.

Hewlett-Packard Co., 1508 Page Mill Rd., Palo Alto, Calif. 94304 [343]

Combustion controller suits many other applications

Designed for combustion control applications, the model 1500 general-purpose controller, using four controlled outputs, can control complex processes involving as many as six loops. Typical applications include boilers, soaking pits, reheat furnaces, and pipeline controls. The controller has fully integrated, microprocessor-based technology and can be custom-designed to meet routine and special control needs. Configuration is relatively simple and can be done by most any process-control engineer.

The model 1500 controller has a compact 6-by-8-in. front panel and includes control stations for the four process loops, four special-function push buttons, eight process alarm

New products

annunciators, and a three-part tuning and configuration section, which has a light-emitting-diode display and a lockable access switch. A built-in track-and-hold logic assembly backs up the microprocessor.

The basic programmed model sells for $7,500. Delivery, depending upon quantity, will require approximately 16 weeks.

Westinghouse Electric Corp., Westinghouse Building, Gateway Center, Pittsburgh, Pa. 15222 [344]

Apple peripheral tracks positions of luminous objects

A peripheral device for the Apple II computer, Op-eye is a position-sensing device that sees reflective or luminous objects. It has a special two-axis lateral-effect photodiode that gives it a typical resolution of 1 part in 4,000 across the 1.0-by-1.0-cm detector surface in both X and Y directions. With the appropriate optics, says its maker, displacements of less than 0.0001 in. can be measured.

Op-eye produces position information at over 5 kHz, enabling it to track a moving object's position. Minimum detectable intensity is 0.1 μW in a spectral range of 350 to 1,100 μm.

The Op-eye consists of an Apple II interface board, a 16-channel analog-to-digital converter in separate housing, preamplifiers for two detectors, one detector adapter, and a 28-mm lens. It can be used in production-line and machinery control, angle sensing, small-part detection, shaft encoding, large-area graphics digitizing, bioengineering, profilometry, vibration analysis, stress monitoring, and automatic quality

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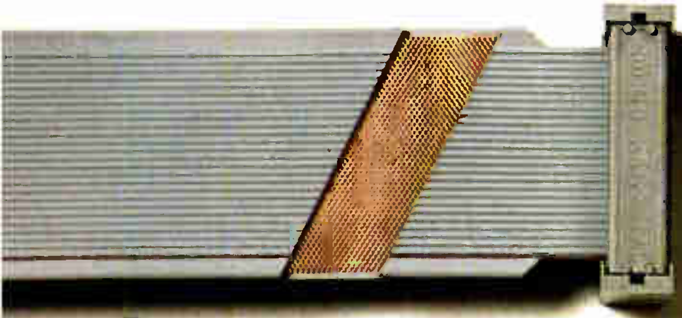

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control. The Op-eye 1 is priced at $1,550. Delivery takes six to eight weeks.

United Detector Technology, 3939 Landmark St., Culver City, Calif. 90230. Phone (213) 204-2250 [345]

Portable controller accepts 420 programming statements

The Eptak 200 programmable controller includes a compact controller with a complementary-MOS random-access memory and central processing unit that is based on an Intel 8049 microprocessor chip, plus a power supply, an input/output track, and a portable programmer. The controller has up to 128 I/O points, a capacity of 420 programming state-

ments, a total of 32 timers or counters in any combination, two 32-stage shift registers, 128 control relay functions, up to 8 data registers, and arithmetic and comparison capabilities. The Eptak 200 provides programmable logic control for smaller industrial applications currently using hard-wired relay control systems or card logic systems. It can economically replace as few as five relays.

The portable unit measures 7¾ by 8 by 2¾ in., is enclosed in a metal case, and weighs 2 lb 6 oz. The basic system has a list price of $2,018 per unit. The price for original-equipment manufacturers is $1,715, and in quantities of 50 or more its unit price is $1,407. It should be available by the end of the summer.

Gulf+Western Company, Eagle Signal Division, 736 Federal St., Davenport, Iowa 52803. Phone (800) 553-1147 [346]

New products/materials

Formon II solder compositions have improved printing properties, flow characteristics, and process flexibility. No separate fluxing is necessary. Solder balling is virtually eliminated, preventing yield losses due to shorting and thermal shock to devices. The new pastes can resolve 20-mil lines or 10- to 15-mil-diameter pads, making them suitable for flip-chip component attachment or semiconductor packaging. The compositions may also be used in assembling hybrid microcircuits and complex printed-circuit boards. Wet prints may be used for up to 48 hours as a temporary adhesive for components. Dried prints may be used in automated processes where parts must be stacked or transferred.

Du Pont Co., Wilmington, Del. 19898. Phone (302) 773-3218 [477]

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Union Carbide Corp., Dept. PJL-1M, Old Ridgebury Road, Danbury, Conn. 06817. Phone (212) 275-2900 [478]

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CVD Inc., 35 Industrial Pky, Woburn, Mass. 01801 [479]

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Products Newsletter

Desktop processor aims at OEMs

Datapoint Corp., of San Antonio, Texas, is targeting its new 2150 desktop processor exclusively at original-equipment manufacturers for a variety of applications, such as data entry, data or word processing, electronic message services, data communications, and personal computing. **The Z80A-based 2150 is the OEM version of Datapoint's 1550 dispersed data processor,** which was unveiled last year [*Electronics*, April 21, p. 163]. It comes with 32-, 64-, or 96-K bytes of main memory and is available with 8-in. diskette or hard-disk drives. Prices range from $7,075 for the 32-K-byte system with a 0.5-megabyte diskette drive to $18,750 for the 64-K-byte unit with a 10-megabyte disk drive.

Winchester drive uses built-in backup floppy

A Motorola EXORbus-compatible Winchester disk drive with a built-in floppy-disk backup is now available from Creative Micro Systems of Los Alamitos, Calif. The unit, which uses an **8-in. Memorex Winchester disk drive with a 10- or 20-megabyte capacity,** can be configured in any combination of up to a total of four drives. The 8-in. floppy disk, from Qume Corp. or Shugart Associates, has a capacity of 0.25, 0.5, and 1 megabyte. A single system with a 10-megabyte Winchester disk drive and 1 megabyte of floppy-disk capacity costs $5,295.

Biomation unveils 100-MHz, 48-channel logic analyzer

Gould Inc.'s Biomation operation in Santa Clara, Calif., has just announced a fast logic analyzer that it claims has the most comprehensive timing and data-flow tracking capability of any such instrument on the market. Called the K101-D, the $23,500 analyzer can **clock data from its 48 input channels into a 48-by-512-bit emitter-coupled-logic memory at rates of up to 100 MHz.** The unit, which will be available in September, also has a built-in digital voltmeter and frequency counter.

Version of 8048 idles on 20 μA

National Semiconductor Corp., Santa Clara, Calif., is gearing up for volume production of its 80CX48, a version of Intel's 8-bit 8048 microcomputer **built with National's 5-V-only, double-polysilicon complementary-MOS (P^2C-MOS) process.** An idle state that brings supply current from 5 mA to 20 μA while saving data in random-access memory and a programmable prescaler for the counter-timer have been added.

Intel and SofTech Microsystems add to 8086 software

The result of over $1 million of hand optimizations is the newest release of Real-Time Multitasking Operating System from Intel Corp., Santa Clara, Calif., for its 8086 16-bit microcomputer. **Version 3 of iRMX-86 is three times faster and 20% smaller.** It includes a user interface with a command-line interpreter, plus device drivers for Intel's magnetic-bubble memory subsystem. Support of the iAPX286's memory management unit is built in, and multiuser access will be added to version 4. The $6,000 price for original-equipment manaufacturers requires as little as $100 in royalties per user.

More software for the 8086 comes from SofTech Microsystems, San Diego, Calif., whose UCSD pseudocode system makes Fortran, Pascal, and Basic, plus all UCSD application programs, available to 8086 users. This implementation also includes the first native-code generator for p-code–to–object-code transformations that allows either interpretive or compiled modes. Program modules can be compiled separately.

Career outlook

Few opto engineers in sight

Like just about every engineering discipline these days, electro-optic specialists are in short supply, a situation that can be traced directly to the educational source. The problem centers on the fact that there are few schools prepared to teach the advanced courses required.

"Only two universities offer the doctorate—the University of Rochester and the University of Arizona. Another, the University of New Mexico, has just been accredited and won't start turning out people for several years," warns Jack D. Gaskill, professor of optical sciences at the University of Arizona in Tucson.

There are other schools such as Carnegie-Mellon in Pittsburgh that offer advanced studies and master's degrees. However, these schools will be hard-pressed to turn out the specialists demanded by rapidly growing solid-state laser, fiber optics, display, and integrated optics technologies.

Two twains. Compounding the problem is the fact that EEs do not get in-depth exposure to electro-optics in their engineering curricula.

"We find it rare for an individual to emerge from the university well-trained in both electronics and optical disciplines," comments R. J. Klaiber of the Western Electric Engineering Research Center in Princeton, N. J.

Gaskill and Klaiber agree that a large part of the problem stems from the failure of industry, government, and academic institutions to work together. They made their remarks at a seminar on electro-optic education at the Conference on Lasers and Electro-Optics held in Washington, D. C., earlier this month.

Oddly enough, the best training seems to come from the two-year technical schools. "Many [community colleges] give excellent training in electro-optics," he noted. Thus, an adequate supply of technicians does not seem to be a problem—at least for Western Electric.

But electro-optics work at the innovative research and development level usually requires a master's degree, if not a Ph.D. And the supply of persons is limited not only by the difficulty of wedding the two disciplines but also by the limited cooperation that exists between the industry, government, and university sectors.

Lack of funds. This lack of cooperation is what is responsible for "a critical shortage of electro-optical engineers in the U. S. today," said CLEO speaker Duncan T. Moore, associate professor of optics at the University of Rochester. "University resources are just too limited to do the job alone," he added.

According to the seminar speakers, those who do go into electro-optics engineering are in for exciting careers involving laser and fiber-optic technologies. **-Harvey J. Hindin**

THE EDUCATIONAL MISMATCH

University-trained electronics engineers	University-trained optical engineers
Familiar with optics through: • wave optics (lasers) • detectors • guiding (modes) • Fourier transforms	Familiar with electrical engineering through: • detection and analysis instrumentation • Fourier analysis • electromagnetic theory
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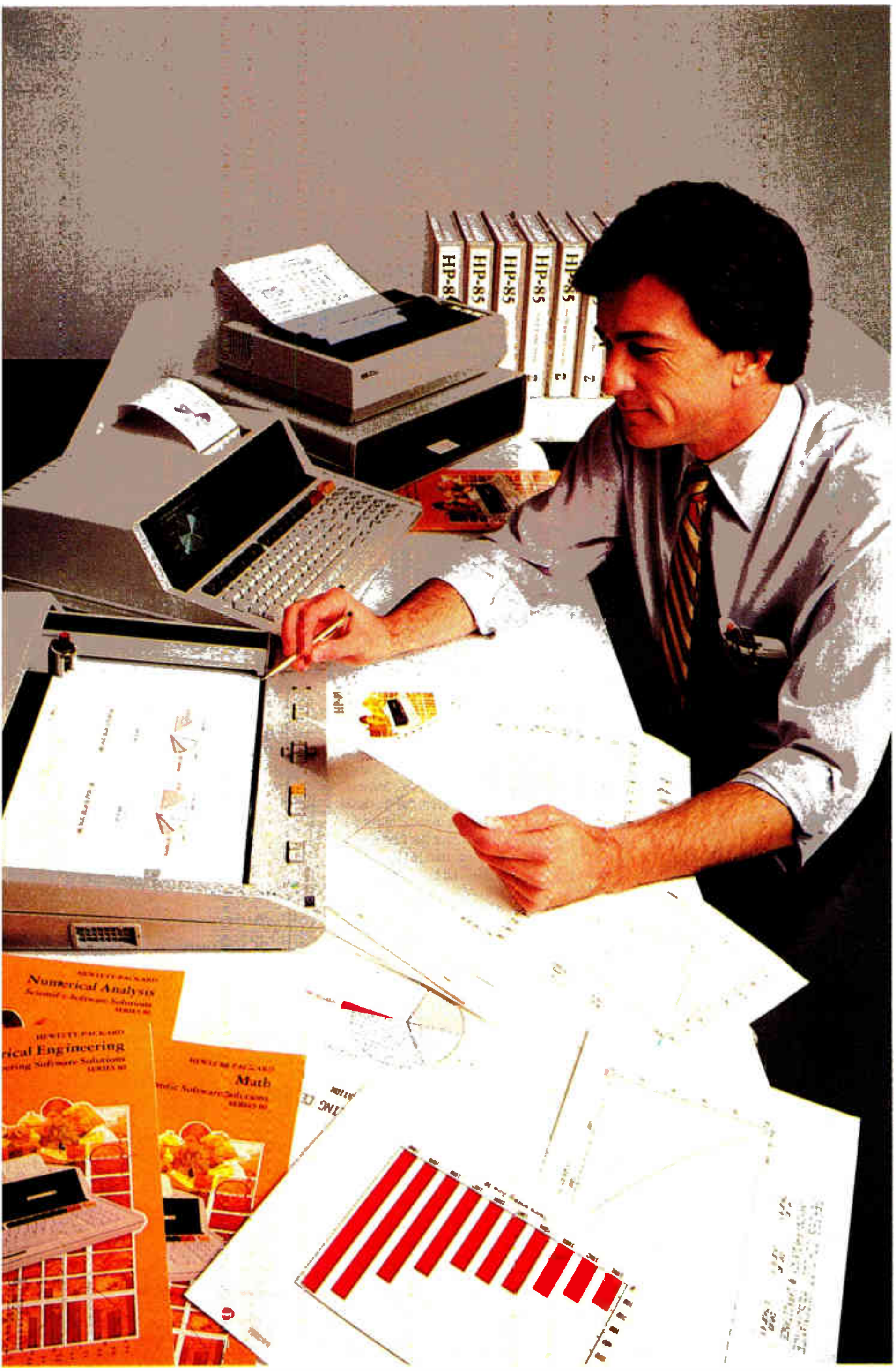

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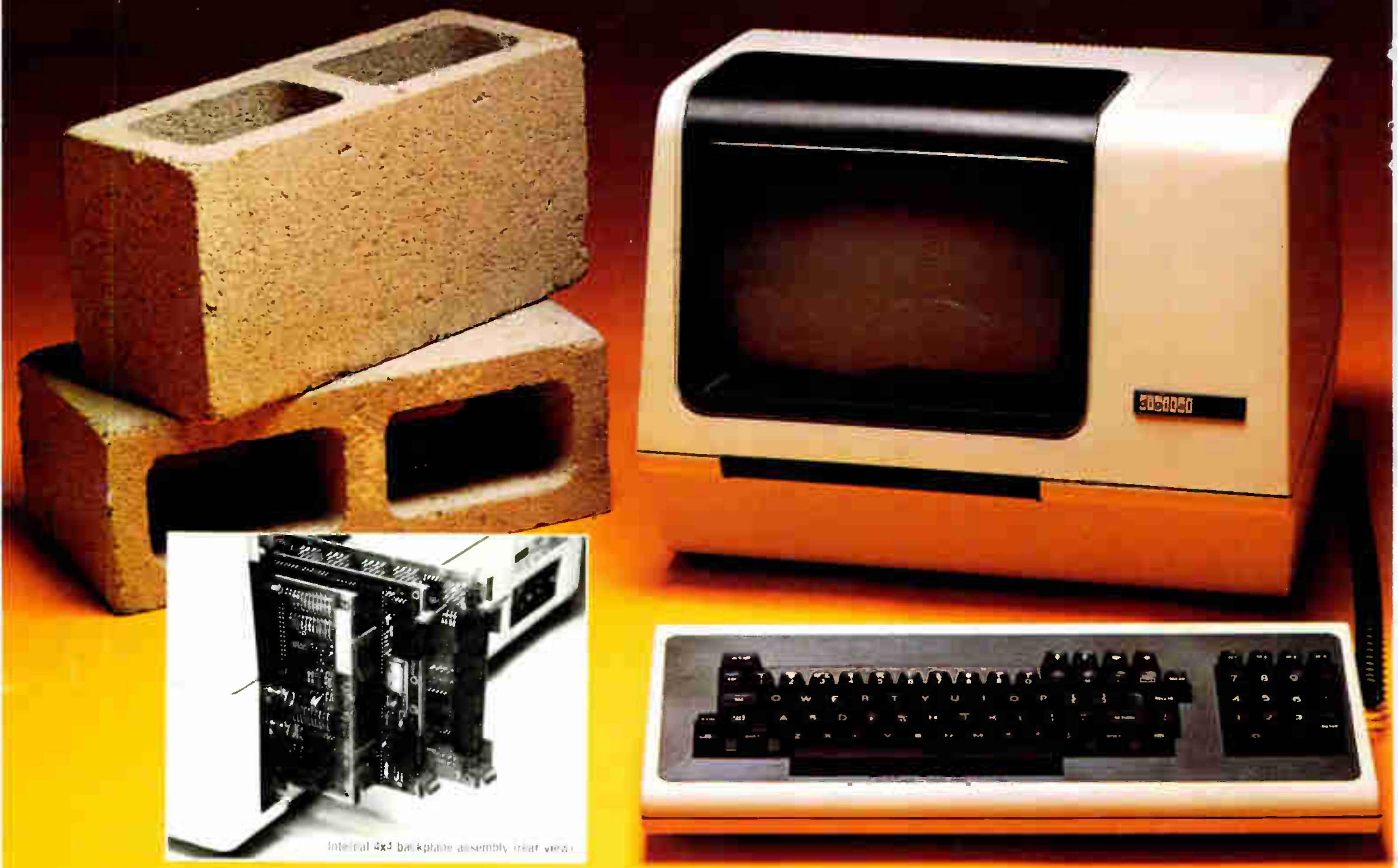

Internal 4x4 backplane assembly (rear view)

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