JUNE 2, 1981

TEST STRATEGIES HELP USERS CHECK BUBBLE MEMORIES/145

Letter from San Diego: the boom is waning/ 100

16-bit processor adds virtual memory to minicomputer line/ 134

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INSIDE JAPANESE SEMICONDUCTOR TECHNOLOGY

9. Circuit Testing Update/No. 9 in a series from Hewlett-Packard.

HOW CAN YOUR MICROPROCESSOR BOARD HELP TEST ITSELF?

It's ironic. The very intelligence that makes your products excel can also be the obstacle that makes testing difficult. Why? Because those intelligent microprocessors are difficult to model. And until they're put to work via code, they're no smarter than any other piece of silicon. Can they be awakened and used to test themselves? Let's look at some of today's testing techniques and see.

Alternatives for testing microprocessor boards.
Board testers available today generally use one of four approaches:

1) Simulator board testing. This is an edge-connector and guided probe testing technique that relies on patterns from a simulation model. The processor is usually removed from the board, and input patterns applied. Output patterns are then compared with those predicted by the simulator. If the patterns match, the support logic is judged good. Next the processor is inserted and different patterns are applied. Now the outputs are compared to those predicted based on the original model plus a high-level software model of the processor. If those patterns match, the entire board is said to be good. Excessive time can be consumed generating both high-level models and testing software.

2) In-circuit testing. Using a bed-of-nails fixture, contact is made with each logic circuit on the board, including the μP. Pulses are applied to input pins of each device. Outputs are compared to those predicted from device truth tables supplied by manufacturers. These libraries are programmed for common device configurations and must often be modified for actual configurations.

3) Comparison testing. In this edge-connector and guided probe method, a known good board must be available as a reference. The known and unknown are initialized, synchronized and then are compared by applying preprogrammed instructions or patterns, or by stimulating with pseudorandomly generated pattern sets. If the outputs match, the unknown board passes.

4) Processor-based testing. This technique uses the intelligence of the μP on the board. The board is powered up and operated at speeds up to 10 MHz using preprogrammed test code resident in the test system or on the board itself. The on-board μP executes this code to exercise the address and data buses, and support circuitry. Key nodes are monitored with signature analysis to detect faults.

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Examples of Processor Pins Testable Only With Software

	8085		6800	Z80
Interrupts	INTR TRAP	RST 7.5 RST 6.5 RST 5.5	$\overline{IRQ}$ $\overline{NMI}$	$\overline{INT}$ $\overline{NMI}$
Control Outputs	S_0 S_1 $IO/\overline{M}$	$\overline{RD}$ $\overline{WR}$	VMA $R/\overline{W}$	$\overline{M1}$ $\overline{RD}$ $\overline{WR}$ $\overline{HALT}$
Other	SID SOD			

Fig. 1

In addition, processor-based testing permits fault detection using Signature Analysis (SA), which is complimented by new software in the digital functional testing package. SA allows rapid fault isolation to the component level on active bi-directional buses. That means high throughput in production.

Furthermore, with the programming aids available from HP, functional test program development time is minimized for μP, memory and IO boards. For example, you can either modify existing routines provided by HP, build your own stimulus routines using HP-supplied building blocks, or develop stimulus programs on a development system and download to the 3060A. The bottom line of processor-based testing is fast test program development, high throughput, and high yield at the final product level.

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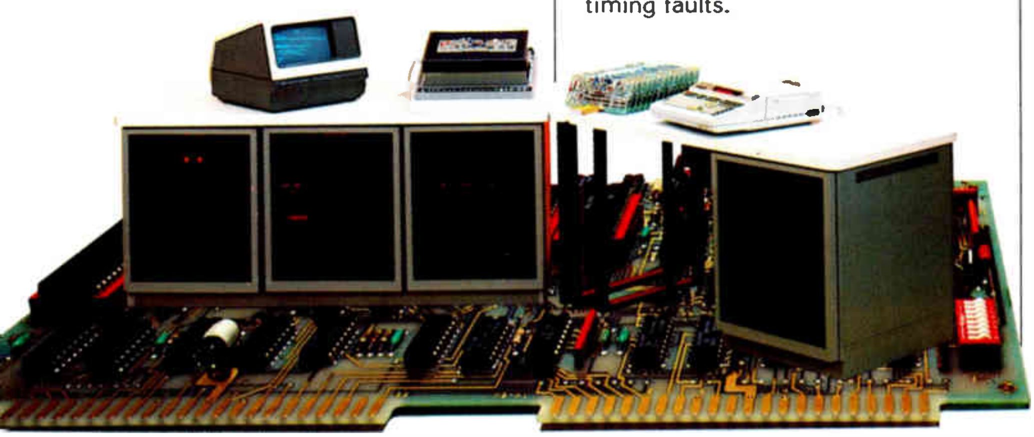

HP Circuit Testers—
The Right Decision

HEWLETT PACKARD

Circle 900 on reader service card

Electronics
The International Magazine of Electronic Technology
Vol. 54, No. 11 • June 2, 1981

Electronics

Highlights

Cover: an inside look at Japan's semiconductor makers, 113

It may seem like a single entity to some, but Japan's semiconductor industry is in reality a group of separate companies that compete with each other, as well as with U.S. and European firms. This special report examines the country's chip makers, their achievements, and their strengths, as well as the factors that helped Japan's rise to solid-state prominence.

The cover is by Art Director Fred Sklenar.

8-mm movie camera makers turn to video gear, 89

With consumers looking for convenience, especially systems that deliver almost immediately viewable images, and sales of 8-millimeter home movie cameras plummeting, manufacturers of this type of film equipment are joining consumer electronics firms in making compact video cassette systems that combine a camera and a recorder. This move is particularly true of Japanese companies, but around the world camera makers are switching over in hopes of winning a share of the growing video market.

Two-chip set brings virtual memory to 16-bit mini line, 134

Large-scale integration has enabled a second-generation set of two chips—a 16-bit processor and a memory management unit—for a minicomputer line to add virtual memory, plus support for other features that are needed for today's applications. Among them are dynamic code changes, multiple processing, and coprocessors for decimal and floating-point operations.

How users can test bubble memories, 145

As manufacturers continue to introduce magnetic-bubble memories and controllers, the use of this storage medium will grow, and as with other memory types, users will want to test the devices before putting them to work. This technical article reviews how bubble memories work, how they can go wrong, and how to test for the various errors or failures possible.

Computer programs aid thermistor linearization, 151

Placing a fixed resistor in series or in parallel with a thermistor can go a long way toward linearizing the latter device, for fast and accurate temperature measurements. Two computer programs, in Basic, take the trial and error out of the linearization procedure by determining the value of the resistor so that the voltage output or the resistance has a zero error at three equidistant points on a linear temperature scale.

And in the next issue . . .

A new troubleshooting tool for microprocessors . . . two articles on local network schemes . . . a 16-bit complementary-MOS processor . . . a fast data-encryption chip.

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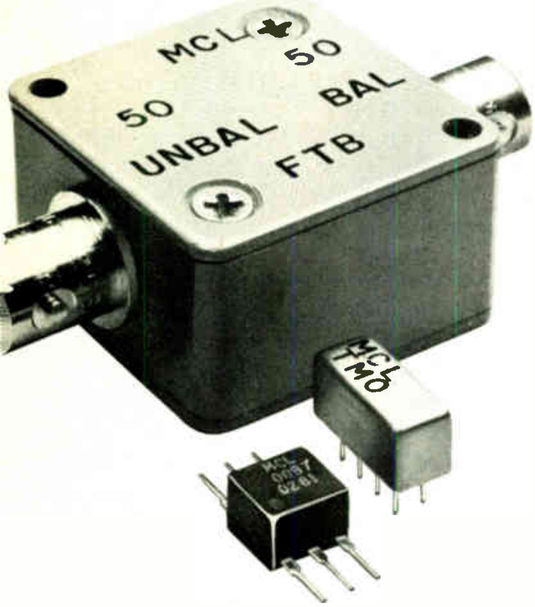

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Publisher's letter

Competition between U. S. and Japanese semiconductor manufacturers has become a preoccupation on both sides of the Pacific, reaching up to the governments of the two countries. Does another article on this competition have anything significant to add?

The report on Japanese semiconductor technology prepared by solid state editor John Posa (p. 113) does indeed have something new to say. Essentially, John has reported on the Japanese chip makers as a part of the U. S. technical marketplace and has considered the competition for what it really is.

"It's a mistake to operate on fear," comments John. "It's about time journalists stopped the fearful reporting, because that view lacks true appreciation for what goes on in Japan."

For one, the Japanese industry is not a monolithic band of firms. The semiconductor companies compete against each other as well as against U. S. producers. Typically, the Japanese makers serve the needs of big parent conglomerates that consume large quantities of components.

"The competition in the long run," John observes, "will be at the system level—the best system will decide the winners. The end product is the key, and I still think that the U. S. is the world leader in defining and supplying what the system market needs."

To get the information for this report, John visited the manufacturing facilities and the research and development labs of the leading Japanese companies. He interviewed the important technical people and the top executives of these companies. The result is an inside view of Japan somewhat different from the usual sound-the-alarm story.

The executives on the interview schedule were open in their discussions. John was therefore able to get an answer to most questions.

But there were other questions. Aspects of Japanese culture left him wondering. For instance, John notes, "I do not know why they need three character sets [kanji, hiragana, and katakana] to make one language." Also curious to John is the Japanese habit of turning off the headlights of their cars at night when stopped by a traffic light. "I was told it is to save on the battery, but it still seems strange," he says.

In other news from Japan, Robert Neff of our Tokyo bureau takes a look in this issue at the impact video cassette recording equipment has had on the traditional 8-millimeter home movie camera makers (p. 89). He reports that, in effect, "if you can't beat 'em, join 'em."

Seeing a large potential market for the new video cameras with built-in recorders that the Japanese consumer electronics companies are bringing to market, the film-based camera companies are also jumping into the field. The reason is simple, Bob says: 8-mm equipment sales are slipping.

But the diversification trend is not limited to Japan. Companies in Europe and the U. S. are also going into VCR cameras to counter erosion of 8-mm sales. Will the strategy work? Bob thinks that major companies such as Canon "can probably carve out a niche in the burgeoning worldwide VCR market."

And from San Diego, we get word from Terry Costlow, our man on the scene, that the electronics community is rapidly turning the area into "Silicon Valley South."

"The jury is still out on whether regional growth has reached its peak," Terry reports (p. 100). Companies new to the area expect continued growth, but firms that have been there for some time worry about rising housing costs and a shortage of managerial talent.

For now, it looks as though the attractions of San Diego, together with the balmy climate, will continue to entice electronics firms.

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Readers' comments

Stop the pendulum

To the Editor: Small business is looking forward to the wide availability of 16-bit microcomputer-based systems. Since peripheral costs are identical to that of 8-bit systems and programming the 16-bit units is simpler, it makes sense that 16-bit microcomputer systems will ultimately be cheaper.

It is disturbing, however, to see manufacturers like Motorola and Zilog rushing to announce new bus configurations and ultimately overshooting the needs of 99% of all small companies, every time they announce a new microprocessor.

I hope there are a few companies in electroland that will take chips like the 68000 and the Z8000 and combine them with the Multibus to make a system that will be good for today and even for the next 10 years.

Henry Keultjes
Microdyne Co.
Mansfield, Ohio

Corrections

A symbol was omitted from the diagram in Fig. 1 of "Dual-function amp chip simplifies many circuits" (May 5, p. 142). The node formed by connecting the 0.01-μF capacitor, Q_3's emitter, and the 3.3-kΩ resistor should be grounded.

In "Counter-timer resolves 1 μs over extremely wide range" (May 19, p. 173), 10-kΩ resistors should be placed between pins 16, 31, and 32 of the TC 5070P counter and ground. Also, a switch that allows measuring the duration of a single pulse can be added between pin 24 of the counter chip and the timer position of the counter-timer switch's lowest gang. Likewise, pin 14 of the 8640B should connect to pin 10 of the 74C74 flip-flop chip.

Finally, in our special report, "The drive for quality and reliability" (May 19, p. 125), Advanced Micro Devices Inc., the well-known semiconductor firm in Sunnyvale, Calif., was sometimes referred to as American Micro Devices. Our apologies to AMD and to our readers. Needless to say, we are now instituting greater quality checks of our own.

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News update

■ Voice communications may be the next facility to be added to the Cambridge Ring, a British candidate for local computer networking. At Cambridge University's Computer Laboratory, researchers have been experimenting with just such a system using a Zilog Z80 microprocessor to interface telephones with the ring.

The Cambridge Computer Laboratory is the originator of the ring [*Electronics*, Aug. 28, 1980, p. 80]. It was developed there from 1976 to 1978 as a means of sharing computer resources, transmitting data at 10 megabits a second over a twisted-pair cable.

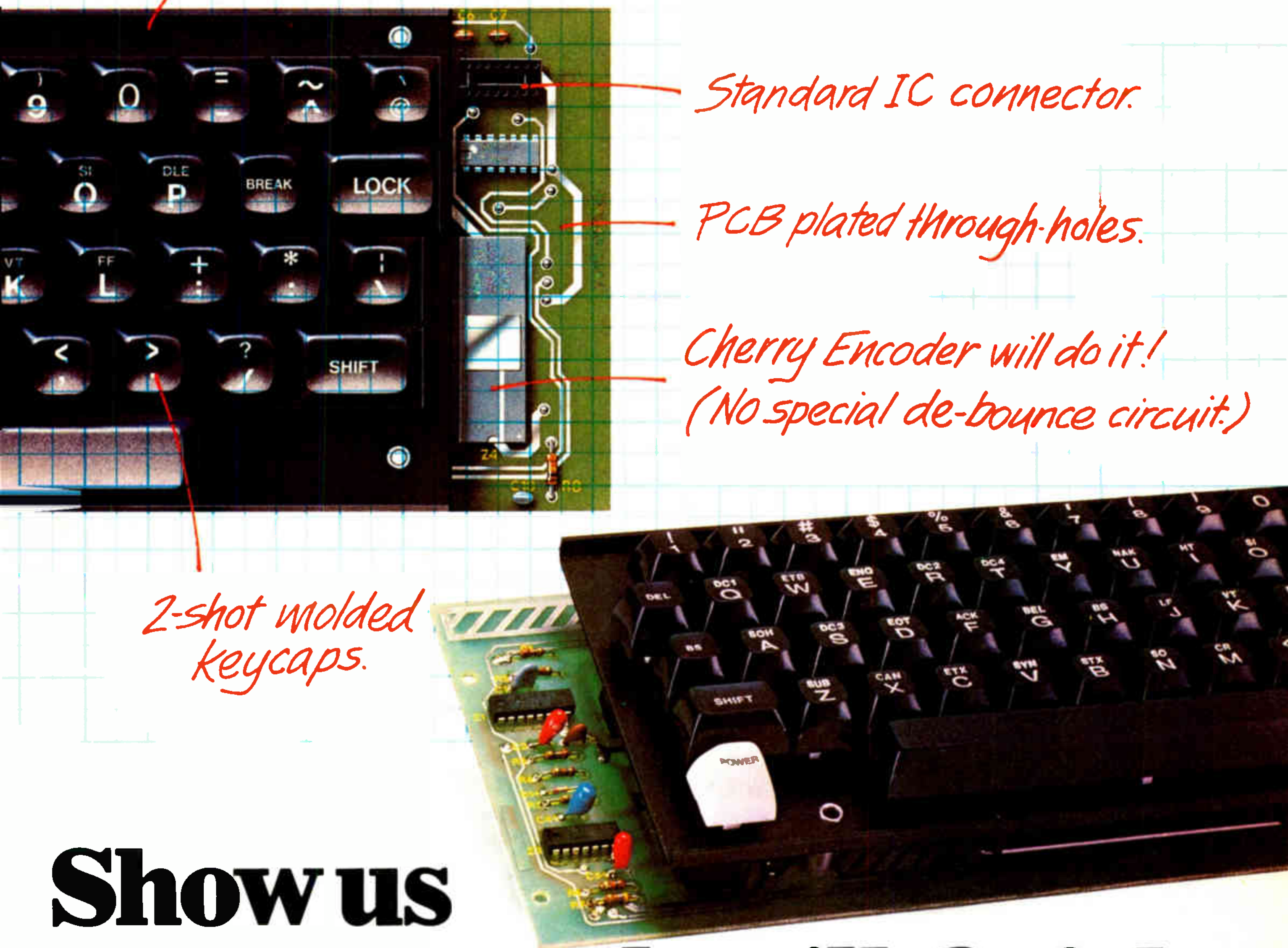
Voice communications via the ring could have an important role in the office equipment environment. It could, for example, be used to append "voicegrams" containing an executive's comments to textual documents stored on disks.

Early on. The Cambridge project is still very much in its early days. For instance, the Z80 is used only for convenience: the control program amounts to no more than 200 bytes of code, a level of complexity that could easily be implemented in an uncommitted logic array.

Cambridge researchers have already used this ULA technique to develop a two-chip interface set for the Cambridge Ring. These chips were due last October, but a second design iteration proved necessary. The first of these samples have now been received and are due for testing, says their developer, Andrew Hopper.

When available, the chips will significantly lower the cost per ring access port but that has not stopped a proliferation of ring hardware suppliers. To date, there are four, among them Logica Ltd., which launched its version last month. Another is Acorn Computers Ltd., which also offers a low-cost local network working at kilobit, rather than megabit, rates. This, it says, could be linked hierarchically to a Cambridge Ring.

There is also a growing body of user experience with the ring—primarily at universities—and it has proved highly reliable. **-Kevin Smith**



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People

Computer Automation needs marketing boost, says Salkeld

Commander. Geoffrey Salkeld aims to give marketing ammunition to sales troops.

One of the foremost things on the mind of Geoffrey Salkeld when he came to America to take the helm of Computer Automation Inc.'s Computer Systems division was to rejuvenate the marketing operation. The Englishman, who had managed Computer Automation's European subsidiary since its inception in 1972, felt that an unpleasant part of his new position at company headquarters in Irvine, Calif., would be a reorganization that would include the ouster of some employees. "I expected to find poor[-quality] people, but I couldn't have been more wrong," the 46-year-old Salkeld says. "What's missing here is the marketing machine."

As division general manager, he plans to build a marketing machine, thereby lifting some of the burden from the sales force. Comparing sales personnel to infantry troops, Salkeld says, "We've got good troops with good weapons, but they've been short of ammunition."

To help supply the sales force, he is establishing two managerial posts—product marketing and product management—and has plans to double the sales support provided by marketing. In the past, salesmen have not received adequate information about the products and their niches in the marketplace, he says. Salkeld also wants to improve customer identification, avoiding what he sees as an American tendency to "play Russian roulette" in making loosely selected sales calls.

Input sought. The self-proclaimed "fanatic on product planning" has established a product-planning review group that will consist of representatives from each product line of the division, so that further products will be planned with input from each sector. Another of his goals is to take some of the decision-making burden from the shoulders of company president David Methvin.

"I want to put well-reasoned options before him," he says, noting that in the past Methvin has sometimes been forced to dictate because of a lack of selections. "He should dictate, but he should dictate from the options, and they must be placed before him," Salkeld emphasizes.

Although he enjoys southern California, the father of two is holding onto his property in England, planning to return after things are back on an even keel in the States.

Solid state is spearhead for RCA, says Pletcher

"There is a corporate commitment at RCA to be No. 1 in electronics and a major player in the semiconductor industry," says Stephen L. Pletcher. The new marketing vice president at RCA Corp.'s Solid State division sees his Somerville, N. J., operation as the spearhead of the company's electronics business. In fact, he notes, "solid state was singled out as a target for heavy emphasis and investment" by the outgoing company chairman, Edgar H. Griffiths, at the recent annual meeting.

As follow-through on Griffiths's charge, Pletcher, the 40-year-old former vice president for sales at Harris Corp.'s Semiconductor Products division in Melbourne, Fla., ticks off these two items:

- The division in 1980 invested more than twice the 1979 figure in capital equipment. "We were behind the big guys, but we'll catch up in two years—and we were able to skip some of the intermediate steps."
- Spending on research and development will be in excess of 10% of

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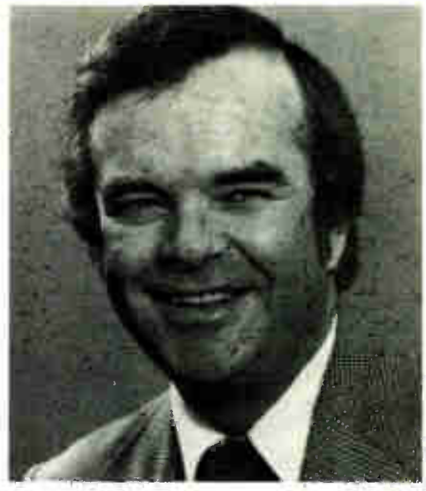

Point man. Stephen Pletcher sees RCA Solid State leading his firm's electronics effort.

sales—which last year represented about 5% of RCA's total of $8 billion. "Here, too, we're behind as a percentage of sales and our plan is to get even."

The master plan calls for the division to grow faster than the markets in which it competes—principally power and discrete devices, complementary-MOS memory and logic, and linear circuits—now that the division has been consolidated, Pletcher says. "We're dedicated to those market niches where we have been successful," he adds, which means a major thrust in C-MOS. However, "silicon on sapphire is still being made for custom applications in high-reliability, radiation-hardened, and certain high-speed areas," he notes.

Pletcher has a bachelor's degree in marketing from California State College in Fullerton and before his tenure at Harris was national sales manager at Mostek Corp. in Carrollton, Texas. He emphasizes that RCA Solid State will no longer adopt the shotgun approach—"almost every process and every market"—but will go after market segments.

"From now on," he says, "we are interested only in the markets where we have strength and where growth is possible." In addition, his plan calls for identifying customers in a "major account focus program" to better fill their needs and for more new products—25 in the chip area so far this year. □

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Standard Resistance Values from 10 ohms through 1 meg ohm. Special values available up to 5 meg ohms

Operating Temperature Range: Industrial Products −25°C to +125°C, Mil Products −55°C to 150°C

Excellent Stability: (Environmental) ΔR <3% (Shock and Vibration) ΔR <1%

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Infinite Resolution

All available in a wide range of mechanical configurations and pin styles!

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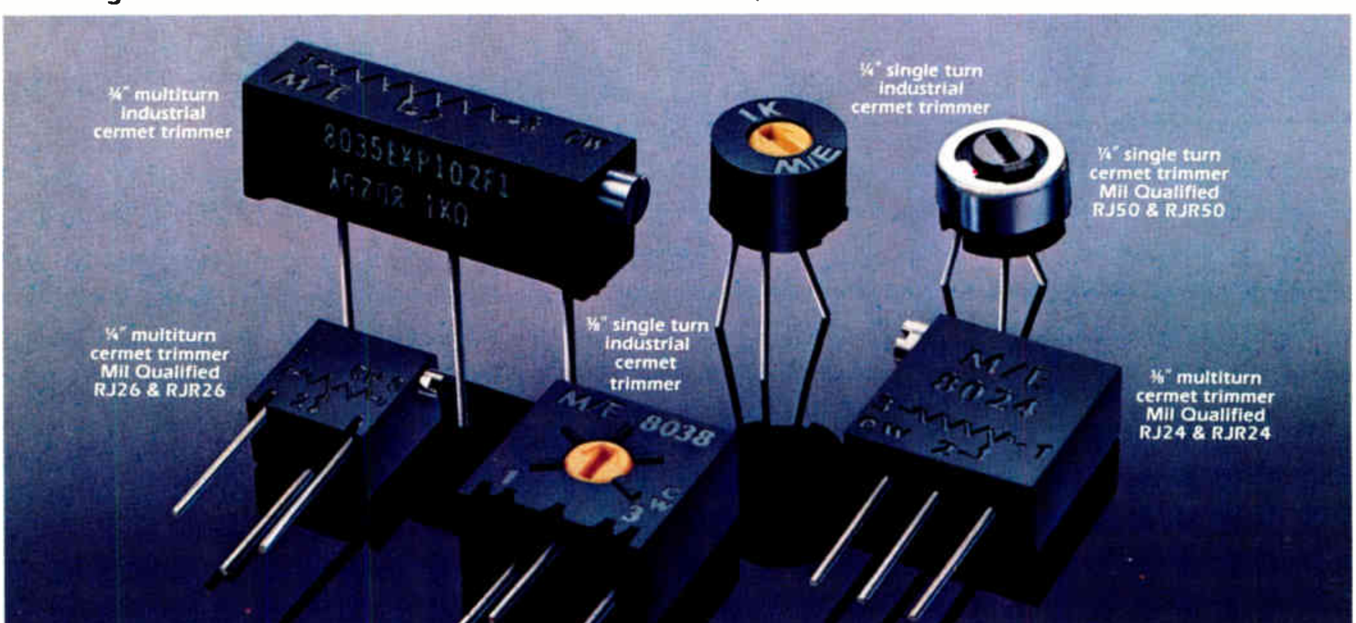

Now you do!

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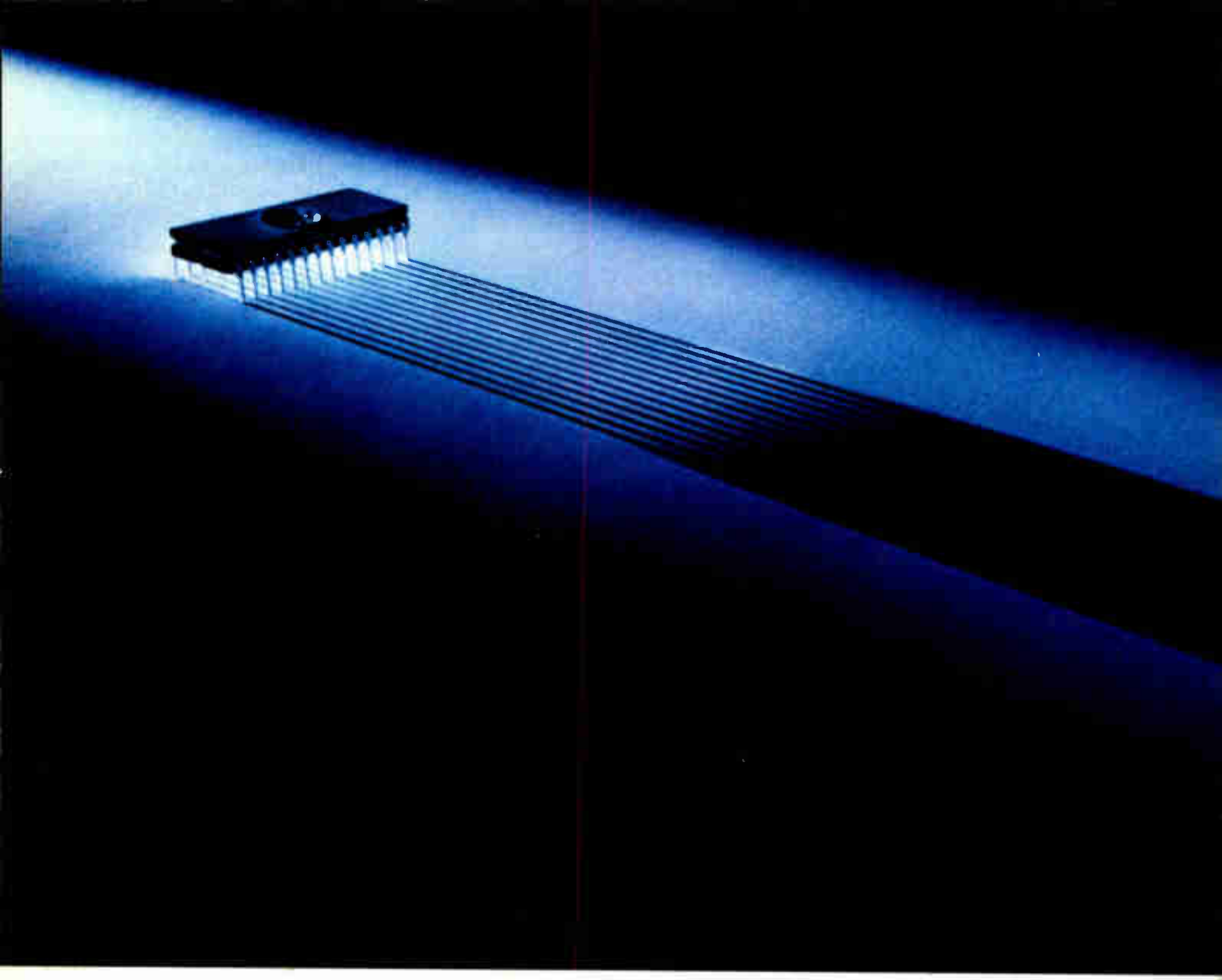

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Now you can get your hands on Intel's 2764 EPROM for just $16.

That's also the price we'll guarantee you for deliveries of 10,000 or more in first quarter, 1982.

And it's good for one today.

Which means you can start to design 64K non-volatile programmable memory into your system right now.

And know by the time your system goes into production, the volume price for 64K will be $16.

We can make that guarantee because Intel's 2764 is already in high volume production. And it has the same size die as our 2716—thanks to our high density HMOS*-E process.

That's why our 2764 is already on its way down a super fast price curve that other 64K EPROMs haven't even started.

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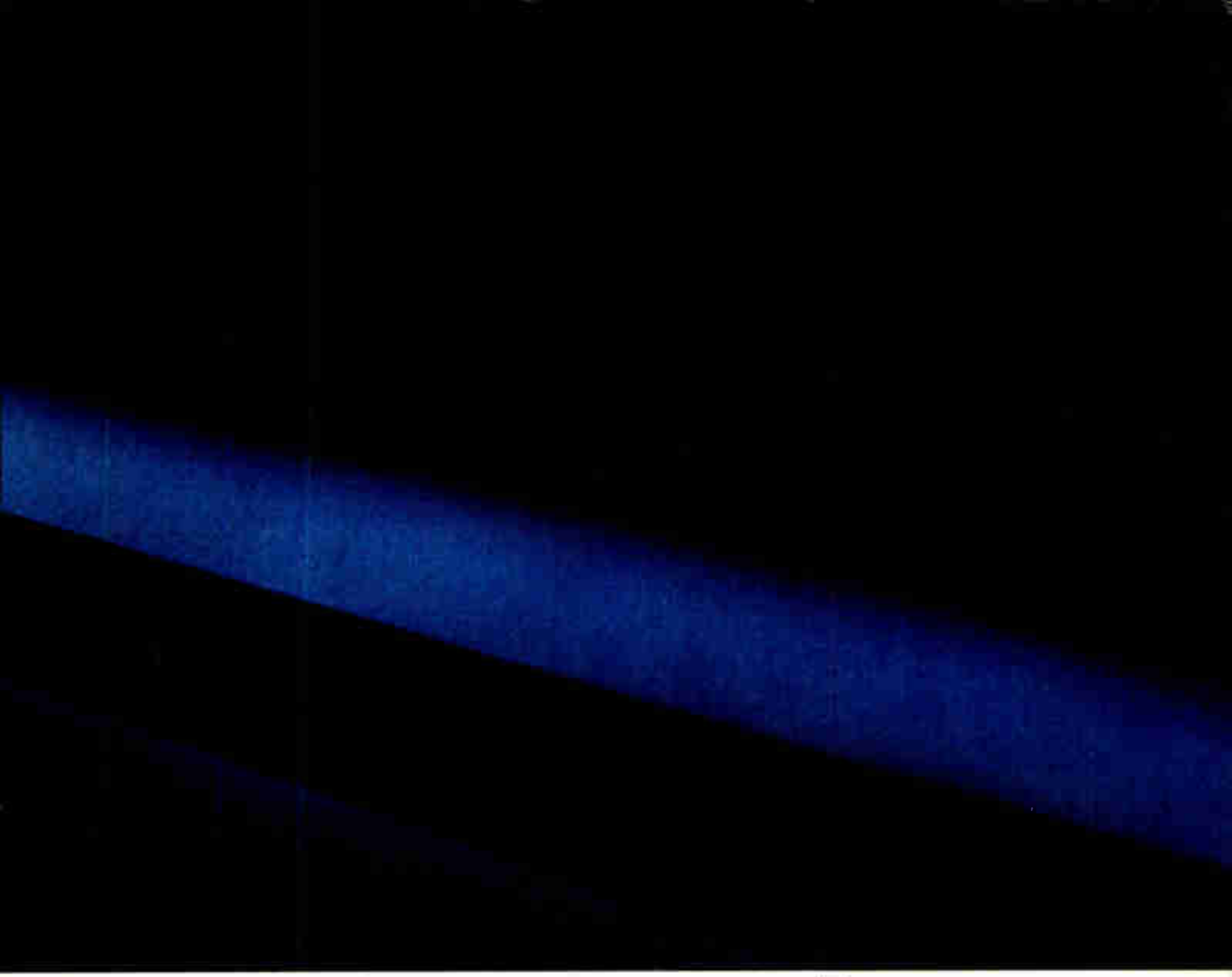
Access times down to 200 nanoseconds to increase your system throughput time.

Two-line control that eliminates bus contention to maximize data reliability.

And along with that, there's our EPROM reliability that comes from 5 million hours of accelerated HMOS-E life tests.

Plus a JEDEC-standard pinout for byte-wide memories.

So you can switch from 16K to 64K in no time—with a minimum of change.



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Estimated 64K usage______________

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The solution to your problems.

Now. A logic analyzer made expressly for microprocessor-based design.

The Tektronix 7D02.

An instrument that provides solutions instead of compounding problems. That cuts design time and improves cost-effectiveness.

Look at just a few examples:

Design Problem: Adapting your logic analyzer to work with a specific processor.

7D02 Solution: Just plug the μP-specific 7D02 probe directly into the prototype microprocessor socket and press START. Acquired data is immediately disassembled and displayed in your processor's own mnemonics.

Design Problem: Sorting error-related data from other program flow.

7D02 Solution: Programmable data and clock qualification filters the data and stores only information pertinent to the problem.

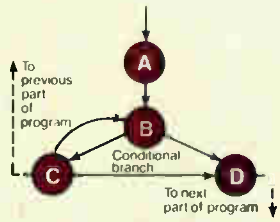
Design Problem: Relating hardware activity to program flow.

7D02 Solution: State and timing sections are included in a single logic analyzer, with each section able to trigger or qualify data acquisition by the other.

Design Problem: Monitoring I/O activity on the system bus.

7D02 Solution: Acquire both synchronous and asynchronous data through interactive triggering to examine both slides of an I/O transaction.

Design Problem: Tracking program flow through non-sequential algorithms with conditional branches to pinpoint an error.



7D02 Solution: The 7D02 can monitor multiple events and conditionally branch as part of its trigger or data qualification sequence. As a result, it can detect an error condition anywhere in your program flow.

microprocessor–based design.

7D02. The solution.
No matter how you look at it, the 7D02 has what you need for faster, more efficient microprocessor-based design.

A series of probe modules adapt the 7D02 to major 8-bit and 16-bit processors, both now and in the future. There's also a general purpose probe for use with microprocessors not specifically supported today. It may also be used like a conventional logic analyzer for troubleshooting the peripheral elements of the system you're designing.

You can have up to 52 channels of synchronous data acquisition, of which 8 channels can be used to acquire asynchronous data at speeds to 50 MHz for timing analysis.

Data acquisition resources include four word recognizers and two interactive counters that can be reset on the fly. Also several modes of both data and clock qualification.

You get two levels of glitch triggering with a resolution of 5 ns, and a separate glitch memory. Plus separate acquisition and reference memories for quick data comparisons.

And all the 7D02's resources are quickly and clearly configurable through a simple user language. One that lets you trigger right on a problem instead of around it. Minimum programming input yields maximum insight into your prototype's software and hardware activity.

For more information on the 7D02, contact your Tek Sales Engineer or call us toll-free. 1-800-547-6711.

You'll wonder how you ever designed without it.

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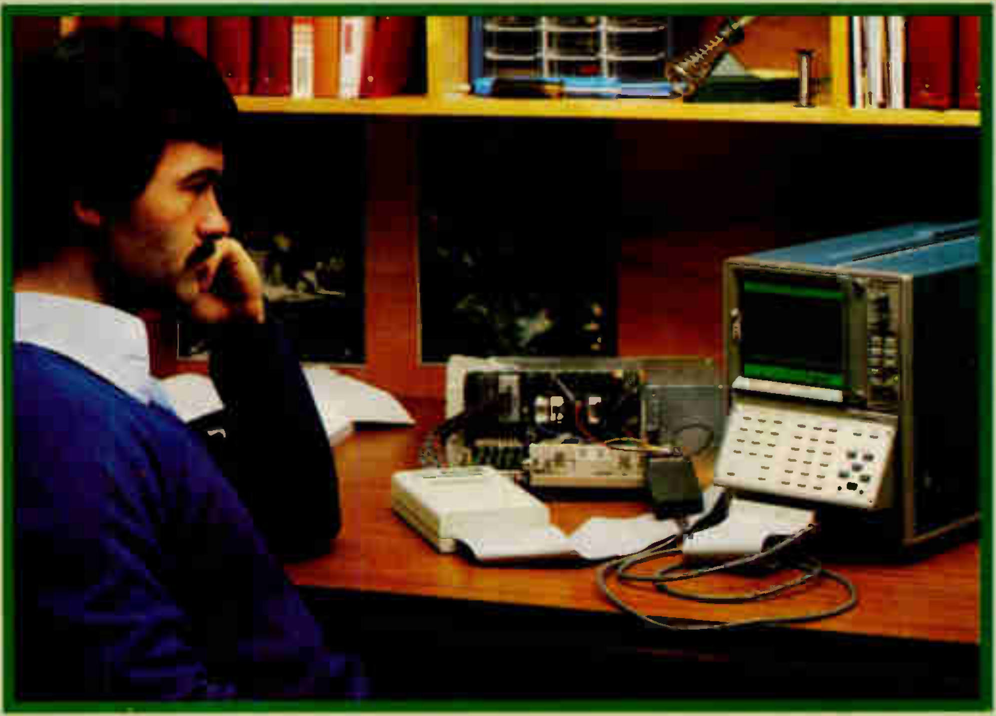

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High Speed

Following the small step

Recent efforts by the Reagan Administration on behalf of the semiconductor industry have paid off moderately in an agreement in principle with the Japanese government to lower tariffs on incoming semiconductors to 4.2%. The significance is not so much in the actual amount of the reduction, but rather as the first signs of willingness of the Japanese to budge on their protectionist stance against U. S. imports. Equally important is the recognition by the Administration that the semiconductor industry warrants vigorous support. So the tariff reduction is a good start, but it is only a small step forward. The industry needs much more substantial help on a number of problems.

For example, there is the difficulty of capital formation in an era of high interest rates while competing with highly leveraged Japanese companies that have an open pipeline to bank loans at low interest. One helpful step would be to allow faster depreciation of the very expensive equipment used by the semiconductor makers—equipment that quickly becomes obsolete as the technology changes. Several bills are now pending in Congress that would help. The best one for the industry appears to be S-317, which permits a 6% investment credit for equipment depreciation over two years.

Support is also sought by the industry in the area of funding for research and development. In the face of organized R&D programs fully backed and funded by foreign governments, U. S. firms find themselves at a distinct disadvantage when they have to do it all on their own. The Government can provide incentives by appropriate legislation. HR-1539, now pending in the House, would permit a 25% incremental tax credit for R&D and is seen by the industry as highly beneficial to fast-growing, high-technology companies. Another bill, HR-1864 (the Senate version is S-692), would grant a 25% tax credit for contributions to universities.

A third important problem for the industry is attracting and holding on to good people. A whole slew of bills are pending—most of them opposed by the Administration—that are designed to help do just that. At least four are in the hopper that eliminate income tax for Americans working abroad, a measure that is long overdue. Insiders give the concept a 50% chance of passing in one of the versions. Other measures being proposed are the reinstatement of qualified stock options and reduction of capital gains tax by raising the exclusion from the present 60% to between 70% and 80%. Industry representatives deem these measures a long shot.

Finally, there is S-970, a trade reorganization bill that proposes a Department of International Trade and Investment that would merge all the various agencies and units now involved in international trade into one cabinet-level department. That would certainly have the advantage of giving the Government one consistent voice in trade policy, an improvement over the current cacaphony of conflicting rules and objectives of the many agencies that get into the act.

If the Administration really believes that semiconductors are a vital component of the economy they are trying so hard to restore, as seems to be demonstrated by the tariff agreement, then they should get behind these bills and get them enacted. No less than the future status of the U. S. semiconductor industry as a world competitor is at stake.

What's so special about Pro-Log's new 4 MHz Z80A card?

You can't tell by specs alone.

It's not just the state-of-the-art 4 MHz clock rate that makes our new 7804 STD BUS card something special.

It's not just the on-board counter/timer with four cascadable channels.

Or the byte-wide memory that allows mapping and strapping in any combination up to 8K bytes of RAM and 32K bytes of ROM and PROM, or up to 65K bytes with the companion 7704 memory card.

Dynamic RAM refresh, power-on reset, bi-directional address and control bus for DMA . . . all are features you can get from other STD BUS card manufacturers.

What's extraordinary is the quality.

Our new Z80A CPU card is built by Pro-Log—the people who designed the STD BUS concept.

Like every one of our STD 7000 series cards, this Z80A CPU card is built with proven, industry-standard parts. All components are 100% tested and burned-in. It's designed to work reliably with all of our STD BUS interface and I/O cards, and to keep on working and working in the field.

We're so proud of our high quality that we back it with a one-year parts and labor warranty.

That's why our customers ask us to build STD BUS cards they could get somewhere else. Because no one builds cards with Pro-Log's attention to quality and reliability.

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Find out what our customers say about using Pro-Log STD 7000 cards. Write or call for our STD BUS applications brochure, plus technical data on our new 7804 CPU card, its companion 7704 memory card, and our full line of STD BUS products.

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STD BUS

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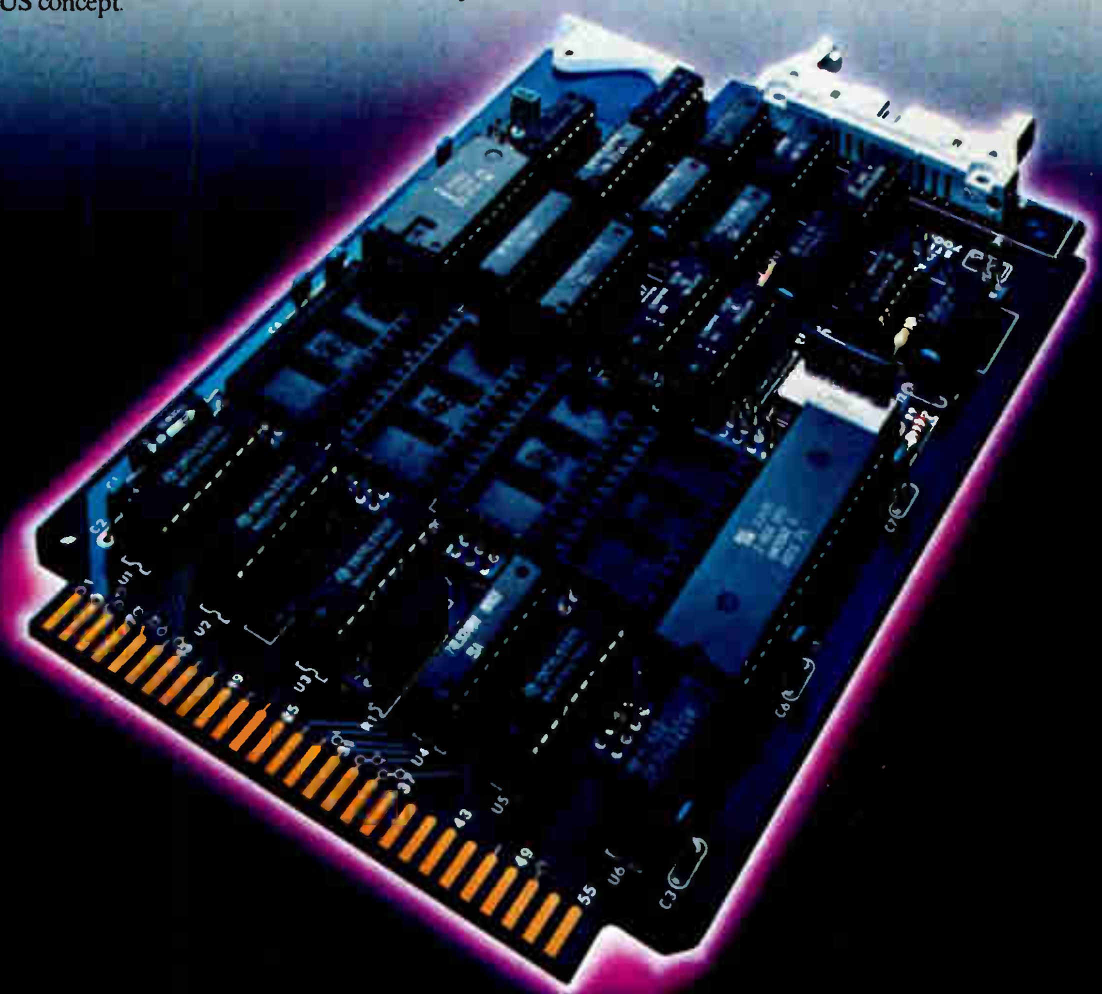

Meetings

39th Annual Device Research Conference, IEEE Electronic Devices Society, University of California at Santa Barbara, June 22–24.

Comdex/Spring, The Interface Group (160 Speen St., Framingham, Mass. 01701), New York Coliseum, New York, June 23–25.

EMC '81—Electronic Materials Conference, Metallurgical Society (P. O. Box 430, Warrendale, Pa. 15086), University of California at Santa Barbara, June 24–26.

FTCS-11—11th Annual International Symposium on Fault-Tolerant Computing, IEEE Computer Society, Holiday Inn Downtown, Portland, Maine, June 24–26.

18th Design Automation Conference, IEEE and Association for Computing Machinery, Opryland Hotel, Nashville, Tenn., June 29–July 1.

Power Electronics Specialist Conference, IEEE Aerospace and Electronic Systems, University of Colorado, Boulder, June 29–July 2.

Third International Conference on Hot Carriers in Semiconductors, Center for the Electronic Study of Solids (Université des Sciences et Techniques du Languedoc, Centre d'Etudes Electroniques des Solides, 34060-Montpellier CEDEX, France), Montpellier, July 7–10.

Concapan 1, First Convention-Exposition of Electrical and Electronic Engineering of Central America and Panama, IEEE, Atalpa Convention Center, Panama City, July 9–12.

ICALP 81–Eighth International Colloquium on Automata, Languages, and Programming, European Association for Theoretical Computer Science (S. Even [ICALP 81], Computer Science Department, The Technion, Haifa, Israel), The Technion, Haifa, July 13–17.

Fifth International Conference on Vapor Growth and Epitaxy and Fifth American Conference on Crystal Growth, American Association for Crystal Growth (Conference Secretariat, Anthony L. Gentile, Hughes Research Laboratories, 3011 Malibu Canyon Rd., Malibu, Calif. 90265), Hotel del Coronado, Coronado, Calif., July 19–24.

WCCE 81—Third World Conference on Computers in Education, International Federation for Information Processing (WCCE 81 Organization Committee, Pierre Immer, 33, av. de Cour, CH 1007 Lausanne, Switzerland), Palais de Beaulieu, Lausanne, July 27–31.

Siggraph '81, Association for Computing Machinery (Siggraph '81 Conference Office, 1 Illinois Center, 111 E. Wacker Dr., Chicago, Ill. 60601), Dallas Convention Center, Dallas, Aug. 3–7.

16th Intersociety Energy Conversion Engineering Conference, IEEE, American Society of Mechanical Engineers, American Institute of Aeronautics and Astronautics, *et al.*, Hyatt Regency Hotel, Atlanta, Aug. 9–14.

Seminars

Visual Psychophysics and Medical Imaging Symposium, IEEE, Vrije University, Brussels, Belgium, July 2–3.

Gordon Research Conferences (Pastore Chemical Laboratory, University of Rhode Island, Kingston, R. I. 02881): "Thin Films and Solid Surfaces," Colby-Sawyer College, New London, N. H., July 13–17; "Point and Line Defects in Semiconductors," Plymouth State College, Plymouth, N. H., July 13–17; "Nonlinear Optics and Lasers," Brewster Academy, Wolfeboro, N. H., Aug. 3–7.

Third Brazilian Workshop on Microelectronics, Laboratório de Eletrônica e Dispositivos (Faculdade de Engenharia de Campinas, Unicamp, Caixa Postal 6061, 13100-Campinas-São Palo, Brazil), University of Campinas, São Palo, July 13–24.

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For emulation or production, put the MK38P70 to work for you.

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For 8-bit microcomputer applications, no other single-chip family gives you more design momentum than the Mostek 3870. Our piggyback EPROM MK38P70 is one reason why.

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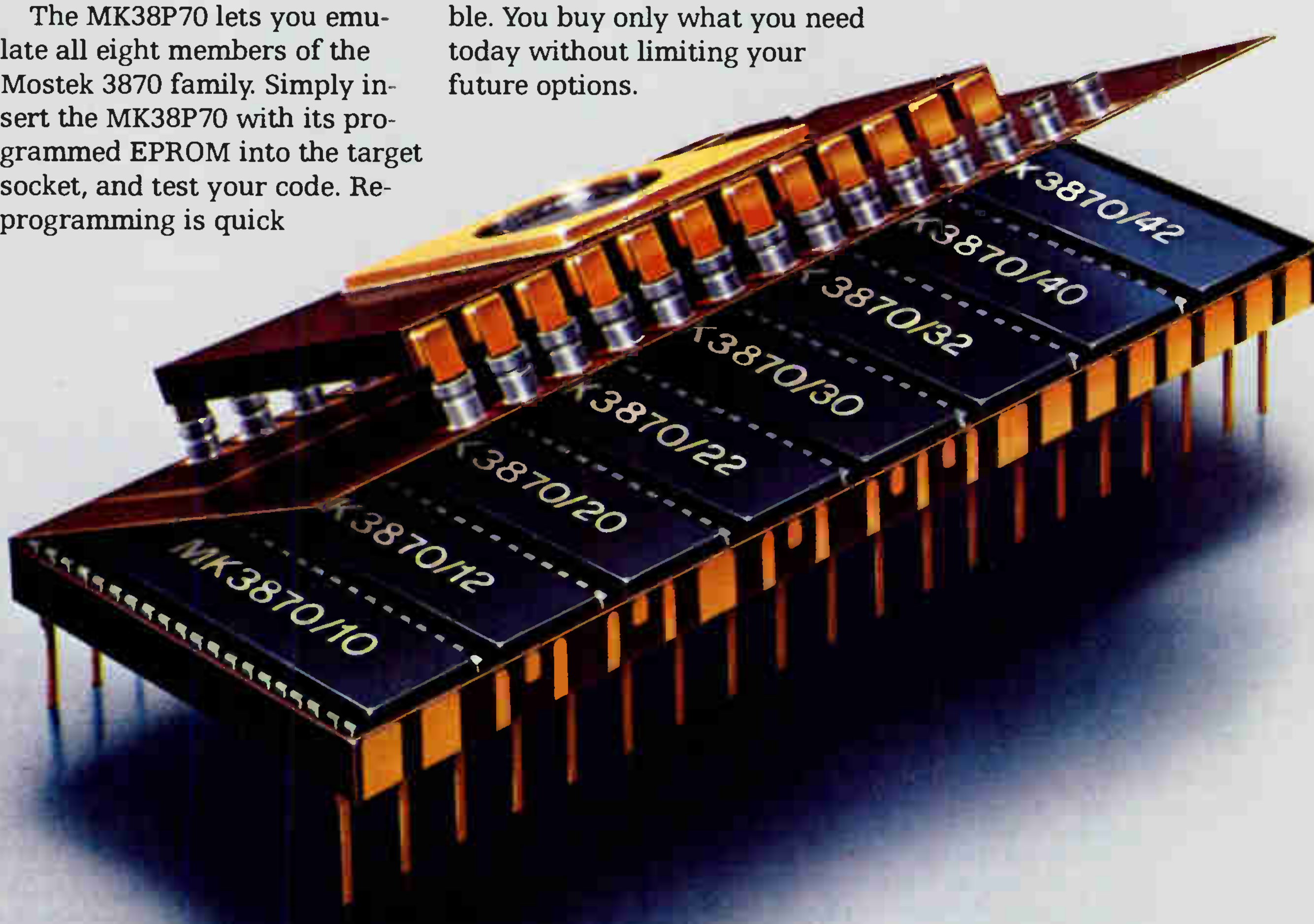
This single-chip family has been proven in hundreds of designs and millions of circuits. And all eight 3870 versions are hardware and software compatible. You buy only what you need today without limiting your future options.

Look at it another way: the MK38P70 gives you eight different custom chips in one standard package available at all Mostek distributors. That's design momentum. Put it to work for you. Call or write Mostek Corporation, 1215 West Crosby Road, Carrollton, Texas 75006; phone (214) 323-1801. In Europe, contact Mostek Brussels; phone 762.18.80.



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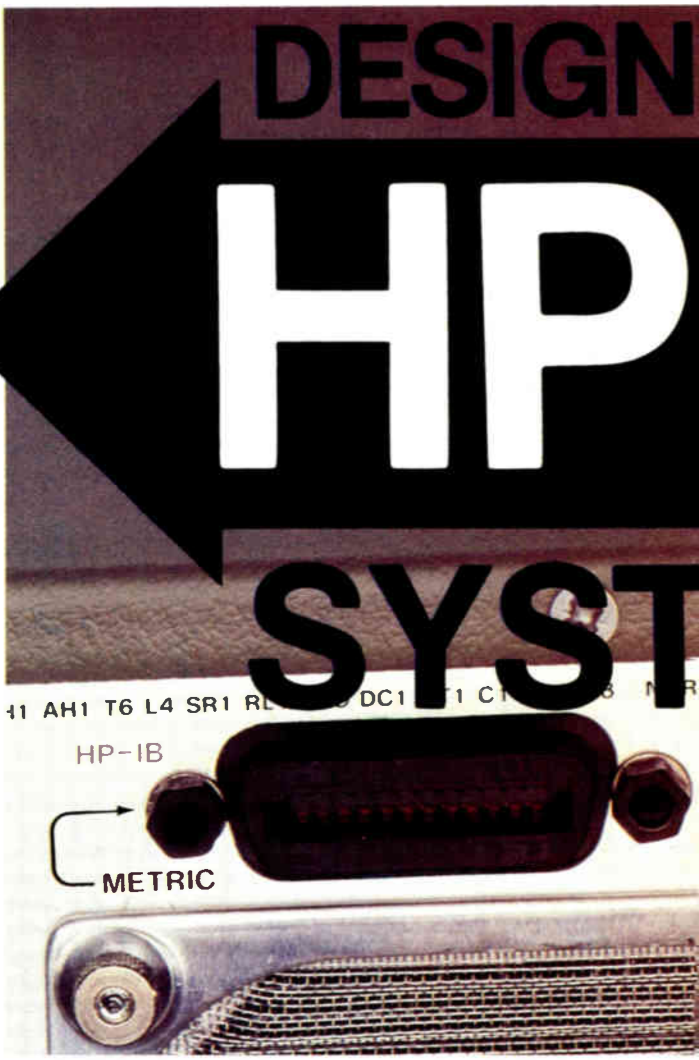
This symbol means faster measurement system development. . .



The familiar HP-IB (Hewlett-Packard Interface Bus) symbol is HP's way of identifying instruments and computers that conform to the IEEE-488 standard. But it means much more than just bus architecture and system compatibility. The HP-IB symbol also stands for the documentation and support that helps you get a measurement system operational in weeks instead of months.

Five reasons why you'll save time and effort.

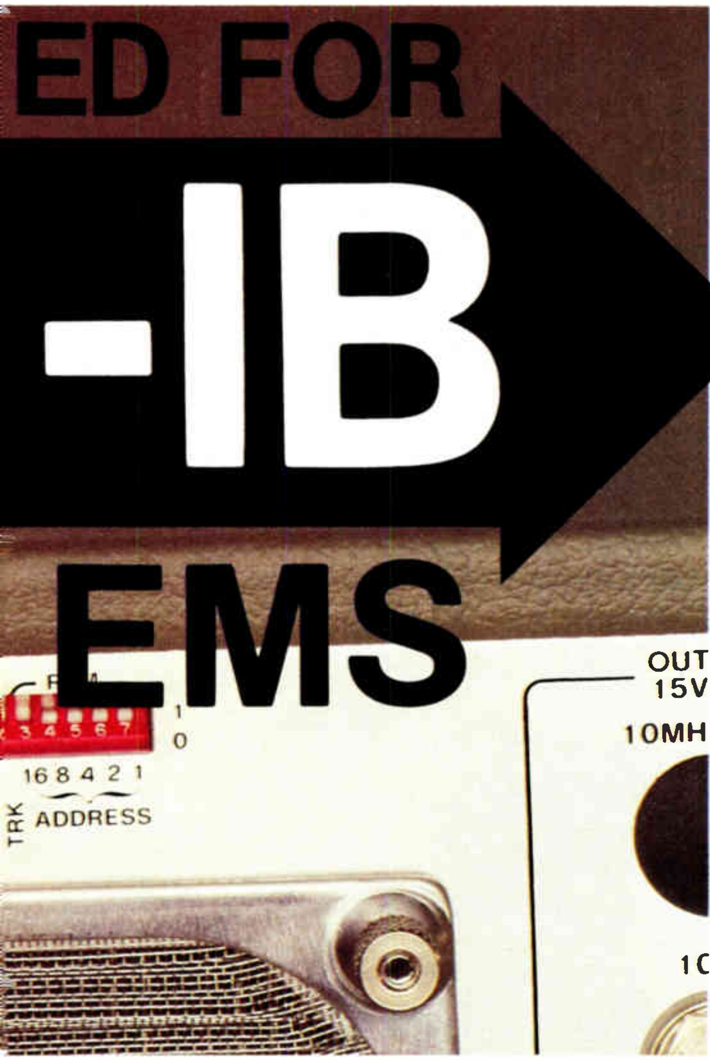
Choose HP when you need a measurement system and you get these advantages: 1) All devices and all documentation come from a single source which means consistency in design and documentation. 2) Every member of the HP-IB family of instruments and computers — over 140 in all — is designed for and tested to rigid HP-IB standards of compatibility. 3) Just as important, every HP-IB device comes with complete and comprehensive documentation that's easy to follow and consistent in its approach to implementation. You'll receive service manuals and operating manuals that typically include a guide to the implementation of computer based systems. 4) You can choose from more than 100 HP application notes. Many of these will teach you how to accomplish specific measurements in conjunction with the controlling computer. Software examples are included in a number of these to help you get to a solution even faster. In fact, one of these examples may be just what you need for your exact application. And many HP application notes list the results of performance tests to help you verify proper system operation. 5) HP also offers training, system engineering support and on-site service . . . assistance from start to finish. But these aren't the only reasons HP is the logical choice for measurement system development.

Over ten years of experience to call on.

When you design and build a measurement system, you can have the confidence of working with the company that was there when the need for a standard was realized. HP invented the 3-wire handshake technique and ever since then we've been designing and building HP-IB compatible components. By choosing an HP instrument or computer, you get the benefit of over 10 years experience in interface bus architecture, and how it can best be implemented.

Choose from a wide variety of computers.

With more than 140 different HP-IB instruments and computers to choose from, you can configure the measurement system that's just right for your application.



because it stands for system documentation and support on more than 140 HP-IB instruments and computers.

For your computing controller, you can choose from among the seven members of HP's powerful, flexible 1000 series family. Or you can select one of five friendly and flexible desktop computers. All HP computers have powerful, high-level languages that make it easy for you to write application programs.

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HP offers all "Designed for Systems" devices with post-warranty support you can count on. You can continue this beyond the normal warranty period with an HP Maintenance Agreement. That means you'll enjoy yearly fixed cost, regularly scheduled preventive maintenance, priority response, and even more.

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To find out how HP-IB compatible instruments and controllers can speed you to a faster system solution, send for our free brochure, "Do your own system design in weeks, instead of months." Just write: Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304. Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.

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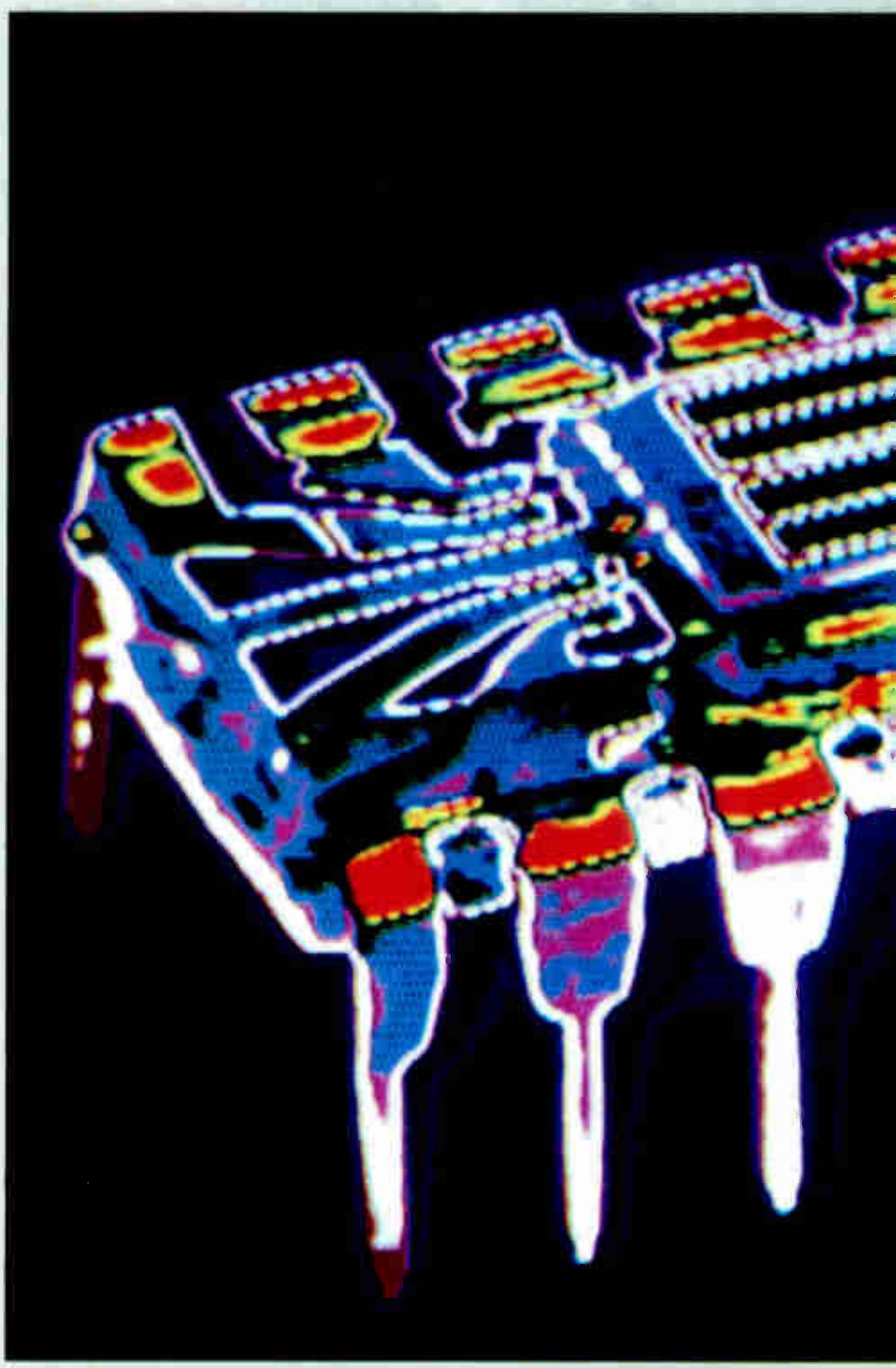
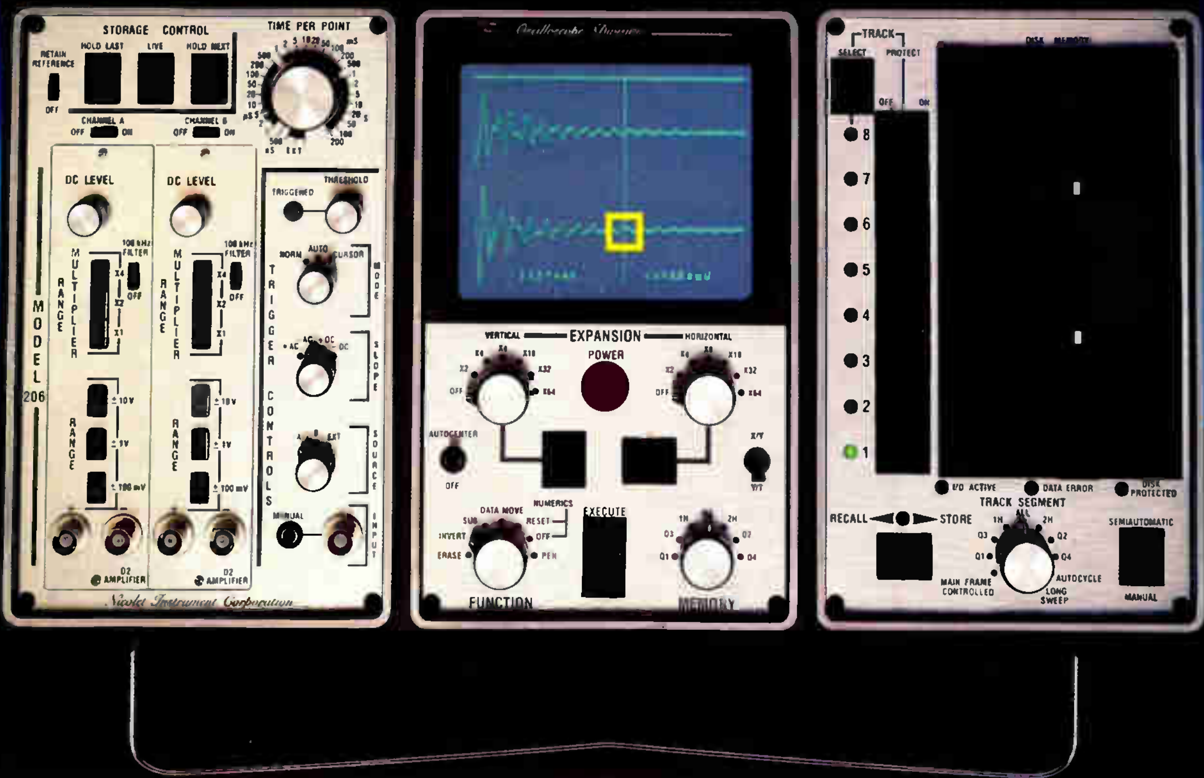
SCIENCE, NOT SCIENCE FICTION

Fact: The Mostek 64K RAM is here. Utilizing our Scaled POLY 5 process technology, this new generation VLSI memory represents the cumulative expertise of the same people who already have three impressive industry standard memories to their credit. Standards that include the MK4096 4K RAM, as well as its second generation counterpart, the MK4027. And more recently, the MK4116 16K dynamic RAM.

Fact: The MK4564 is not, however, a simple scaling of the MK4116. On the contrary, it's an entirely new approach to MOS memory design. One that demanded fresh, innovative ideas to maximize signal strength, yet minimize differential noise, sense amplifier offset and substrate voltage excursions, to name just a few. How we mastered these challenges with new circuitry, new layout techniques and new process technology is why our 64K RAM is so highly



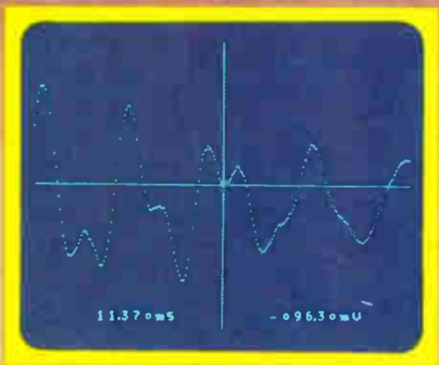
Science showing science: New advances in photographic densitomet



See things you've never seen before.

Nicolet digital oscilloscopes offer you resolution, precision, dynamic range and transient capture capabilities unobtainable on analog oscilloscopes. *They are simple to operate and yet extremely versatile.*

Signals can be viewed live, continuously compared to a reference waveform or stored for detailed examination. Continuous, normal and pre-trigger operation are offered as standard and in all modes cursor-interactive time and voltage coordinates can be displayed concurrently with the signal. Stored waveforms can be displayed or plotted in XY or YT format, transferred to internal disk memory for permanent storage or output to other computing devices via industry standard interfaces.



Expansion of selected area in above photo, for detailed analysis.

In addition to offering you the performance you would expect from the industry leader, Nicolet digital oscilloscopes are extremely well proven with thousands in effective use throughout the world.

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Speedy MOS ICs exploit $TaSi_2$

Standard Microsystems Corp. is fabricating pilot quantities of n-MOS integrated circuits that incorporate tantalum disilicide to lower the sheet resistance of their polysilicon interconnections. According to the Hauppauge, N. Y., chip maker, sheet resistivity has been reduced to less than 1 Ω/sq. using a proprietary technique that is **"completely compatible with conventional IC processing" and requires "no exotic production equipment."** Moreover, the material can be oxidized, unlike pure molybdenum, which is also gaining popularity—particularly in Japan—as an alternative to polysilicon. Already, functional devices have been tested with significant improvements in speed, the firm says. Indeed, MOS memory chips with the silicide alone should show roughly a 40% drop in access time, rendering them suitable for high-resolution video and other applications.

HP mulls entry into E-beam market

While maintaining that it is not yet ready to enter the commercial marketplace, Hewlett-Packard Co. is testing the waters by revealing the details of an electron-beam lithography system capable of handling 1-μm geometries. The Palo Alto, Calif., firm's system features a 0.5-μm beam of 600 nA that is blanked at a 300-MHz rate. At that rate, the beam exposes one picture element (pixel) every 3.3 ns while placed anywhere within an 11.7-by-11.7-cm field accurately to within ±0.125 μm. To speed data handling, it has dynamic software controls to correct aberrations in the beam. Although the company's huge prototype 32-bit microprocessor chip set has not yet been produced on the electron-beam machine, a company spokesman says that it could easily be handled by the system, **whose throughput is five chips per hour for chips containing 450,000 transistors.** Not only is that considered fast for an electron-beam setup, but, HP says, it has the potential to handle chips with three times that many transistors at the same rate. At the same time, the General Technology division of International Business Machines Corp. in East Fishkill, N. Y., has come up with a direct-writing electron-beam system that can produce line widths down to 1 μm on 10 to 20 wafers/h.

Guide promises low losses for optoelectronic ICs

A new type of optical waveguide compatible with integrated circuits and having very low attenuation has been developed at the Massachusetts Institute of Technology's Lincoln Laboratory in Lexington. Heretofore, optical losses through gallium arsenide have been at best 4 dB/cm. **The Lincoln Lab technique already has lowered this to 2.3 dB/cm and is expected to approach 1 dB/cm.** The low-loss guides—which could help development of new classes of optoelectronic ICs—are fabricated with lateral-growth epitaxy [*Electronics*, Dec. 18, 1980, p. 35] in which thin, single-crystal GaAs is grown over silicon dioxide using chemical vapor deposition. Thus, the new structures are called oxide-confined waveguides.

CCD delay lines near SAW performance level

Charge-coupled devices have entered a high-frequency, broadband realm once reserved for surface acoustic-wave devices. The new experimental units, gallium arsenide CCD delay lines, have been clocked at up to 1 GHz. They offer 64 ns of delay and promise analog and digital signal-processing applications **at speeds even beyond the present goals of the Pentagon's Very High Speed Integrated Circuits program.** Future devices may be used in pure delay applications, as fast samplers, or as adaptive filters. With a 1-MHz input frequency, the charge transfer efficiency is 99.99%

and at 1 GHz—where SAW devices can lose 10 dB or more—the CCD delay line transfers out 99.4% of the input signal or more. The units are being developed at Rockwell International Corp.'s Thousand Oaks, Calif., Microelectronics Research and Development Center.

Motorola drives toward '81 date for speech chip

Motorola Inc. is going full speed ahead on efforts to introduce its own speech synthesis chip set by the second half of this year [*Electronics*, March 27, 1980 p. 34]. James R. Fiebiger, MOS IC division manager in Austin, Texas, says, "We have a very intensive effort going on in our logic group **and we do expect to have a product this year.** It is clear that speech will be a big market." (See also p. 42.)

Data units continue to add capabilities

Data-communications machines, designed with digital plug-in modules and plug-in software, are becoming more intelligent and multifunctional. The latest example is Panafax Corp.'s MV-3000, called a Transverter by the Woodbury, N. Y., company. The name is intended to give an idea of what the machine can do. It can transmit a facsimile at a rate of 30 seconds per page conforming to CCITT Group 2 or 3 standards [*Electronics*, Nov. 8, 1979, p. 85]. **It also can serve as a minicomputer and receive and print data** from computers, word processors, or Telex or teletypewriter exchange service (TWX) machines. To be part of a family, it will be ready for delivery by the end of the year. It features bit-slice, all-digital operation with transmission line speeds up to 9,600 b/s. Also, the Transverter sports an RS-232 port and can handle binary synchronous, High-Level Data Link Control (HDLC), and other communications protocols. Later versions will include a cathode-ray-tube terminal and a keyboard.

CP/M-compatible system is 10 to 14 times faster

A new CP/M-compatible operating system will be available shortly from Computer Service Systems Network Inc. of Boston that allows programs to run 10 to 14 times faster than the original **owing mainly to streamlined disk-access methods.** The system, which has not been named yet, uses arbitrary record and file lengths, memory mapping, and a highly efficient directory system to eliminate more than half the disk-head accesses needed by CP/M. The operating system also permits the use of main memory as temporary buffer storage, further enhancing efficiency. It is now offered only with the company's Z80A-based general-purpose business computers, though it may be made available later to a wider market.

Addenda

Polaroid Corp.'s latest photography system, called Instant 600, combines several techniques to deliver what it bills as unsurpassed quality in instant photos. **A microcomputer within the Cambridge, Mass., company's camera makes 42 decisions concerning exposure of the film,** rated at ASA 600, the highest available for a print color film, with the right combination of strobe and natural light. Also, sonar rangefinding and infrared correction in low light help run the less-than-$100 camera. . . . Canon U.S.A. Inc., Lake Success, N. Y., has introduced a desktop copier series, the NP-400, that has features—**reducing, enlarging, feeding, and collating—usually found only in expensive console models.** The NP-400F sports all those capabilities and sells for $7,495.

TECHNOLOGY FOCUS: BIPOLAR ARCHITECTURE.

Sperry Univac's Semiconductor Division houses advanced engineering efforts in custom MOS, bipolar and hybrid development. This report highlights current levels of bipolar system's sophistication.

CAPTIVE AUDIENCE.

The success of Sperry Univac's systems-dedicated approach to semiconductor technology is evidenced by the stature of our installed computer base. Valued at over $11 billion, it is second only to IBM.

While burgeoning non-computer markets continue to spur mass volume upswings for the LSI and VLSI component houses, Sperry Univac's Semiconductor Division has remained intentionally captive, highly R&D oriented, and definitely custom.

BACKSTAGE.

This specialized direction allows us to concentrate substantial semiconductor R&D efforts with a 90% degree of certainty that the results will materialize into marketable products. Firm commitments are nearly always in hand before full scale engineering is engaged.

These factors, combined with the presence of state-of-the-art equipment and facilities, have created an explosive technology environment and an inviting professional atmosphere.

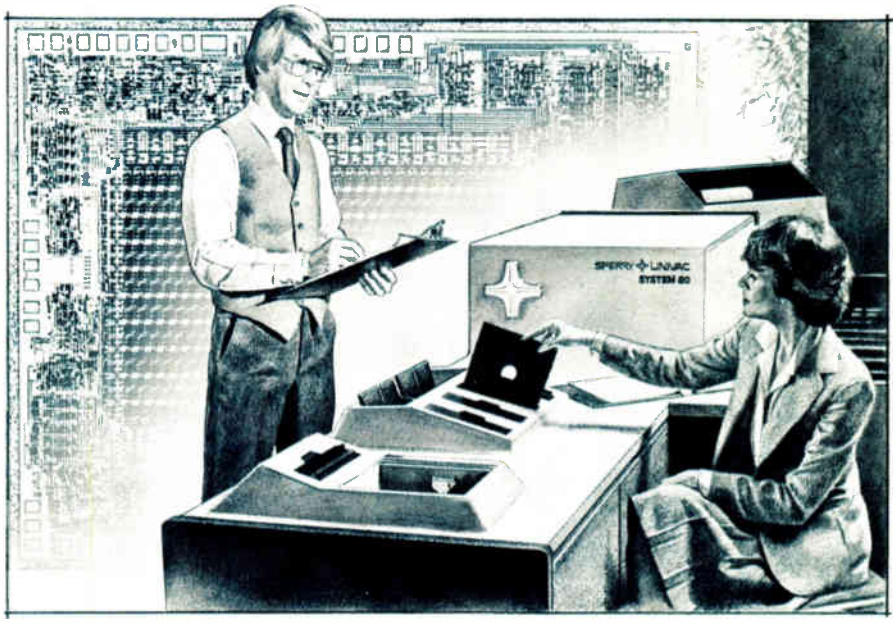
In a brief three-year period, the growing core group of semiconductor engineers here have fully implemented near micron technologies and custom integration of Schottky TTL, CMOS, and high speed ECL circuits employing double and triple level metallization.

Further, current development programs are accelerating in distinct areas of E-beam lithography, laser annealing, submicron device physics, and refractory metal silicide gate structures.

THE SPOTLIGHT.

One of the many focal points for these technologies is the recently introduced Univac System 80 computer. Utilizing high speed VLSI ECL circuitry with gate counts in the thousands, this compact office computer delivers the greatest level of versatile, cost efficient performance of any model in its class —and several beyond.

Revolutionizing the sophistication of computing power continues to be our keynote. Exciting developments of an even more advanced nature are currently underway, assuring a sustained leadership in this field.



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Thick Film Technology/Sr. Process Engineers—Extensive experience in fabrication of thick film circuits. Will be responsible for all aspects of thick film screen printing and firing, including: process specifications, material usages and capital equipment selection, and production aspects. Management potential.

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SEMICONDUCTOR DIVISION

The Computer People Who Listen.

Incompatible gear can talk through data-carrying PBX

by *Tom Manuel, Computers & Peripherals Editor,*
and Harvey J. Hindin, Communications & Microwave Editor

Emulating controller links office automation equipment of varying protocols and formats to IBM computers

InteCom Inc., the Dallas private-branch-exchange manufacturer, is taking a big step toward solving an important office automation problem: how to deal with a variety of data protocols and formats for communication among computer and terminal equipment from multiple vendors. At this week's International Communications Convention in Washington, D. C., the Exxon Enterprises affiliate is introducing a $10,000 add-on to its IBX integrated business exchange series that will emulate the popular IBM 3270 protocols and formats.

With the 3270 IPC (for InteNet packet controller), users with any terminal equipment that communicates in ASCII code can dial a number on their local exchanges and access any IBM machine or IBM-compatible computer that is connected to the IBX switch. The IBX series 40 is a 4,000-port digital office switching system for both voice and data communications.

Possible trend. In what may presage an industry trend for the makers of advanced PBX equipment, the 3270 IPC is the first of a family of controllers for format and protocol conversion that will support a variety of office automation devices and popular local networks such as Ethernet and Z-Net. The IPC will emulate intelligent terminals and controllers by software in the IBX, allowing use of a range of equipment including dumb terminals.

InteCom's idea opens a new category of data-communications applications for private branch exchanges. The typical PBX with data capabilities is designed for communications between compatible equipment [*Electronics*, April 7, p. 139]. Now incompatible keyboards, facsimile machines, optical character readers, communicating word processors, and computers will be able to talk to one another through a private branch exchange. These applications will not long be ignored by other PBX manufacturers.

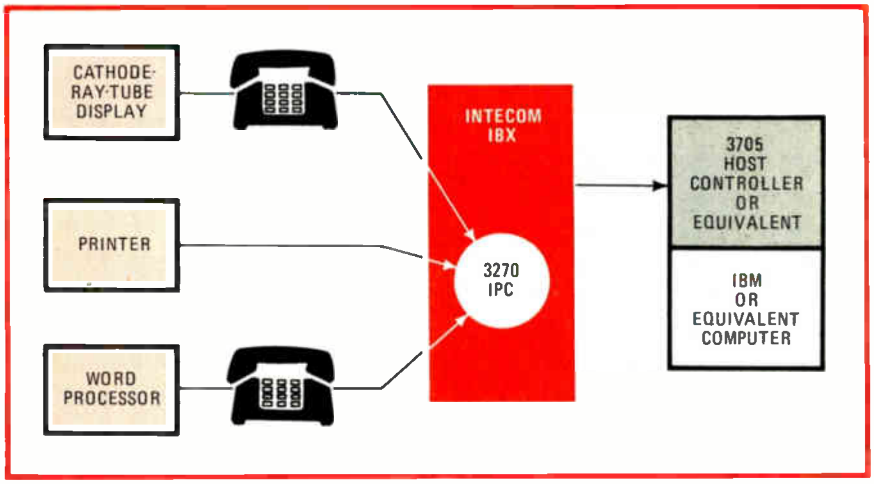
Providing code and protocol conversion is a natural step for the InteCom IBX. Its switching partitions and master control unit communicate by means of a proprietory packet-switching technique.

In the IPC concept, terminals that use different codes or protocols are made to talk to one another by connecting them to programmable packet-switching cards that function as interfaces. Just how these cards function has not been disclosed.

InteCom's 3270 IPC supports emulation of all common functions of an IBM 3271 model 2 control unit, using industry-standard ASCII terminals and emulation of IBM 3284 or 3286 host-initiated printing on standard ASCII printers. The equipment communicates with the host processor in a binary synchronous format at speeds of 4.8 or 9.6 kilobits a second.

All the common features of the IBM 3270 line, such as formatted screens, protected fields, and program function keys are available. Functions added by InteCom include automatic delivery of a user's time-out message to the host computer when a terminal is idle for a long period and an accounting of all time needed for connection.

Terminal locations can be changed without any rewiring, since they simply plug into telephone



Invisible enhancement. InteCom's add-on to its IBX series 40 PBX, the 3270 IPC, will permit compatible communication between electronic office equipment and IBM computers.

jacks. One 3270 IPC emulator will support 8 to 16 terminals or printers, and 512 IPCs can be installed in one IBX series 40 system.

Production

'No hands' assembly packages chips

The state of the art in Japanese automated integrated-circuit packaging is on display in the U. S. Automated packaging is an important factor in the high yield and quality of Japanese ICs, and the machines that do it can be seen at Electronic Arrays Inc., the memory maker acquired by Nippon Electric Co. about 2½ years ago.

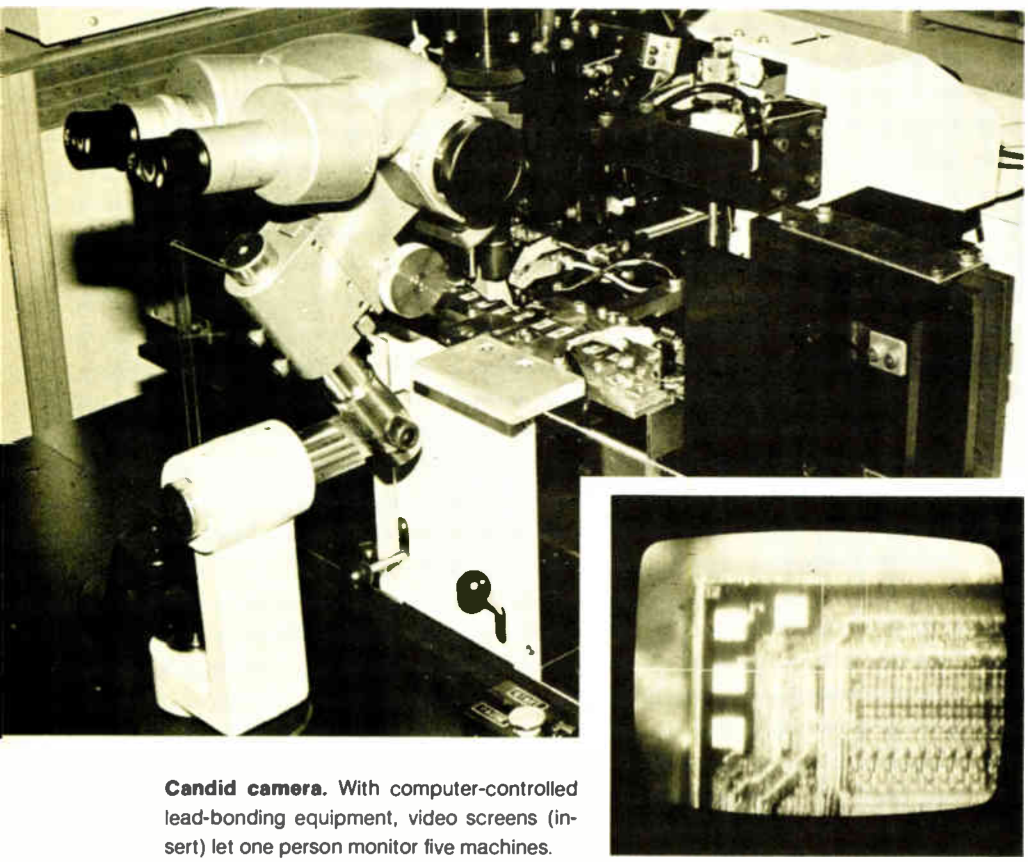
On the company's assembly floor in Mountain View, Calif., sit automatic die-preparation stations, automatic lead-frame insertion equipment, automatic die-attachment stations, and automatic die bonders. All this equipment, used by NEC as well, was built in Japan.

Comparable equipment can now be obtained from U. S. manufacturers, such as Teledyne Inc.'s TAC division in Woburn, Mass., which builds bad-chip recognition and automatic placement and bonding equipment, and Kulicke & Soffa, Horsham, Pa., which makes automatic die bonders.

Motorola Inc.'s Austin, Texas, operation uses some equipment of these types, notably die bonders made by K&S and Foton in Switzerland; it is evaluating other gear.

Says Jack Wright, an engineer in the microprocessor packaging area, "K&S is probably the best in the world, and Foton, which has been around as long as anybody else, is very competitive." He also notes that Japanese manufacturers are way ahead of everybody else in wire-bonding equipment for hermetic lines like ceramic dual in-line packaged units.

Electronic Arrays tested some of this equipment. However, according to Tim Morin, the company's manufacturing manager, NEC maintained that the reliability of Japan-built gear was superior.



Candid camera. With computer-controlled lead-bonding equipment, video screens (insert) let one person monitor five machines.

The automated die-attachment and bond stations incorporate video monitors displaying the minute maneuvers in progress (see photograph). The screens, alive with action, add to the eerie atmosphere, since the few workers on hand are there only to carry loaded cassettes from machine to machine.

Unlike some U. S. assembly operations, the Electronic Arrays line is in a clean room. Besides controlling defects, Morin says, the sterile environment mentally helps instill assembly workers with a sense of care.

Right now the company is manufacturing only read-only memories and assembling both these and 16-K random-access memories fabricated in Japan by NEC. For die preparation, the wafers are scribed, placed on clear adhesive film, and stretched over a circular frame.

During the expansion, the wafer separates along the scribed lines, allowing the bad chips to be picked off and thrown out. Electronic Arrays' die-preparation station does require an operator, aided by a microscope, to activate the plunger that pushes the bad IC into a suction device.

However, more advanced stations, in use in Japan, perform this function automatically. They distinguish good chips from bad through pattern recognition.

Fewer workers. Electronic Arrays currently has 10 die-attachment stations, which together do the work of about 13 operators. One worker can keep watch over five bonding stations, replacing some 30 people.

The bonders take only 200 milliseconds per wire. After bonding, the ICs feed into an automatic trim-and-form machine with which one person does the work of seven.

Another advantage of the automatic equipment is the short time needed to train an operator: just two weeks for either the die-attachment or the bonding machines. It takes about three months for a worker to become competent at manual bonding and two months to master manual die attachment. **-John G. Posa**

Simpler ion implanter to cost less

Working to trim the size and price of ion implanters, Hughes Research Laboratories has condensed the ion path and pared down the number of electromagnetic components. The resultant unit occupies only 30 square feet of floor space, compared with the 100 ft² or more for conventional units, and should sell for about $200,000, less than half the price of current implanters, say engineers at the Malibu, Calif., facility.

To achieve these goals, the Hughes unit is more limited in its power range and the types of ions it implants than are present machines. The flexibility of conventional units is necessary in some applications, but it is often unused in long production runs, says Robert Seliger, manager of the ion physics department at the labs.

A key to the reduced price and cost is the use of a single structure for both source and mass-separation magnets. This approach eliminates costly separate electromagnets and the 90° bend in the ion path found in current implanters.

The two joined permanent magnets also eliminate the need for the distance required to avoid distribution of two charged fields. Also, there is no need for the lenses the conventional units use to focus the ions as they travel from the source to the separation magnet.

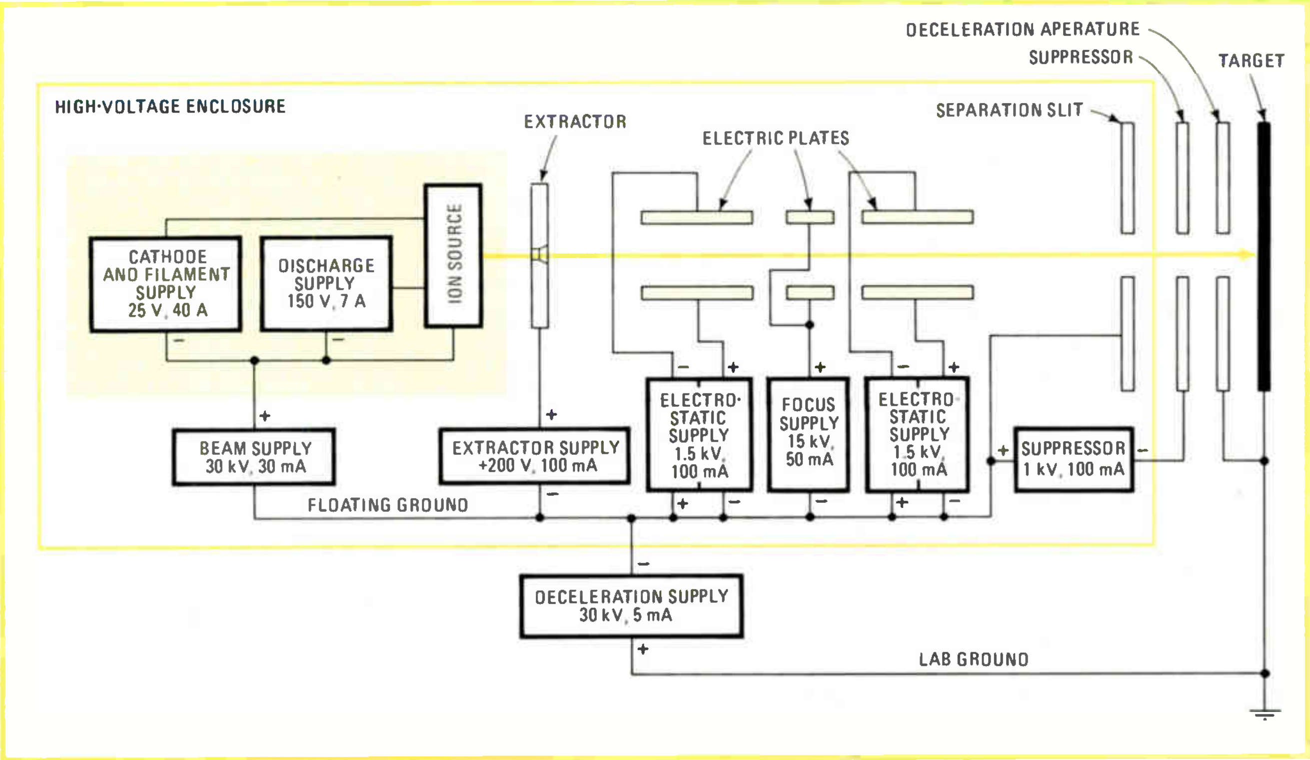
Separating ions. To separate the charged and neutral ions, Hughes engineers have come up with a mass analyzer that measures only 18 inches long. Working with the cross-product of the electric and magnetic vectors (E×B), the analyzer deflects the charged ions toward its electric plates (tinted in the figure). A dog's-leg beam path that does not show up in the figure keeps the neutral ions from the target wafer.

The electric plates of the mass analyzer are split into three sections, each charged with a different voltage to create a focusing device similar to a lens. (Decelerating and accelerating the ion beam keep the initial and final beam energies constant).

The Hughes implanter uses a 2-in ribbon-shaped ion beam, rather than the round beam popular in other units, because it reduces overscan and the space-charge divergence, Seliger says. Beam currents can range from 1 to 2 milliamperes

The power range of the Hughes unit is between 5 and 30 kiloelectron-volts, easily doubled by reversing the polarity of the deceleration power supply, says William P. Robinson, project manager. Although existing implanters go as high as 150 kev, the Hughes power range will fulfill many current needs—and it will easily handle the shallower implanting requirements of future very large-scale integrated circuits, he says.

Some potential users familiar with the unit are taking a wait-and-see attitude, saying the power and throughput capabilities may not fulfill their needs. Hughes gives the average throughput for 3-in. wafers at more than 100 per hour; specifica-



Trimmer and simpler. Hughes Labs' ion implanter takes less than a third the floor space of present units and has a simpler electromagnetic structure, including a single structure for both source and mass-separation magnets that removes a 90° bend in the ion beam's path.

tions for existing high-power units list maximum throughputs for 4-in. wafers of 200 to 290 per hour.

A Z80-based computer controls the system. It determines the voltage of the electric plates when sources are switched—Hughes has set the implanter up for either boron or arsenic implants—and it handles sequencing of the vacuum system, power supplies, and implant cycle.

Upon completion of the prototype trial now in progress, Hughes will ship the implanter to the Naval Ocean Systems Center in San Diego, which supplied some of the funding. Hughes is currently discussing licensing agreements with a number of manufacturers. **-Terry Costlow**

Semicon/West draws new technology

The bustling Semicon/West 81 show, which late last month overflowed its traditional county fairground site in San Mateo, Calif., into the nearby Bay Meadows Racetrack, saw a host of new techniques unveiled in semiconductor-manufacturing equipment. The introductions included a program debugger for integrated-circuit test systems, a technique for annealling ion-implant damage, a method for checking the integration of packaged ICs, and a line of crystal-growing furnaces.

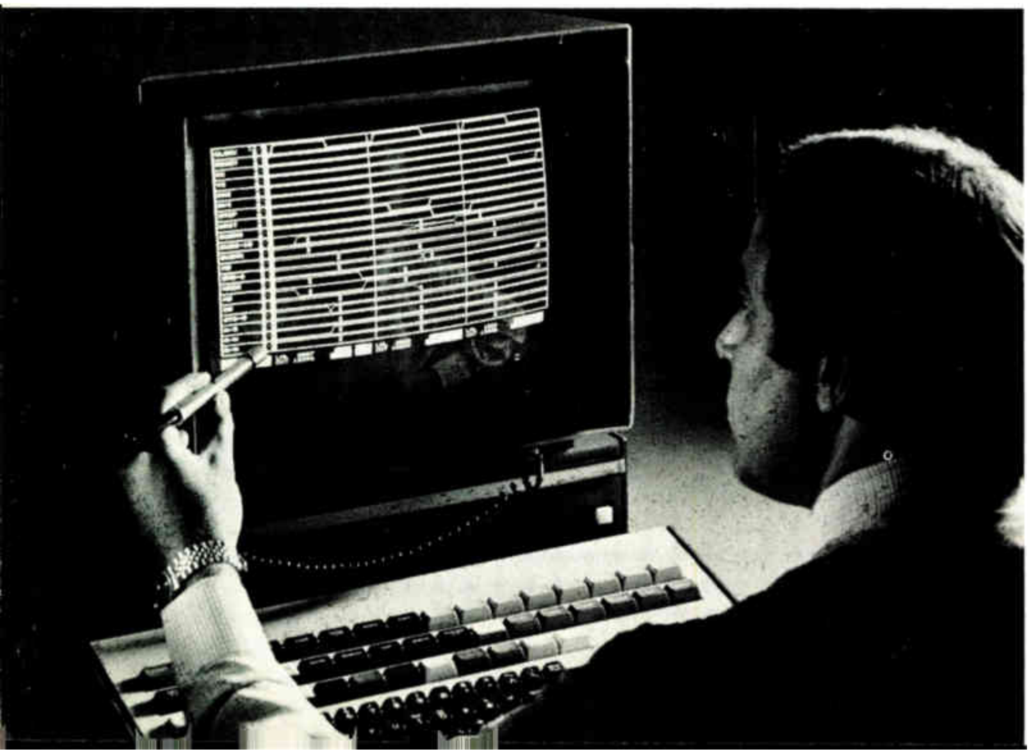
Debugger. Aiming at a productivity boost for program developers, Fairchild Camera & Instrument Corp.'s Test Systems Group reached out to the forefront of computer technology to bring real-time program debugging to test systems. The San Jose, Calif., group's $50,000 System Analytical Graphics Enhancement (Sage) also brings color graphics to Sentry test systems.

It provides the user with a menu of programming options, which can be selected with a light pen (see photograph) or a keyboard. Thus it allows the debugging of Factor language programs in terms of the device rather than the tester.

As the user creates graphic representations of the test program under development. the color monitor differentiates between input waveforms (blue), output waveforms (green), and strobing pulses (red). Errors can be indicated by strobe signals on the appropriate cycles.

In the process control arena, Varian Associates displayed a new form of annealing for ion-implantation damage in silicon wafers. Rapid isothermal annealing uniformly heats an entire wafer for a short time by radiant thermal energy, resulting in good uniformity, reproducibility, and high throughput.

Programmers' friends. For the developers of test software, Fairchild is introducing Sage, a real-time program debugging tool that includes color graphics.



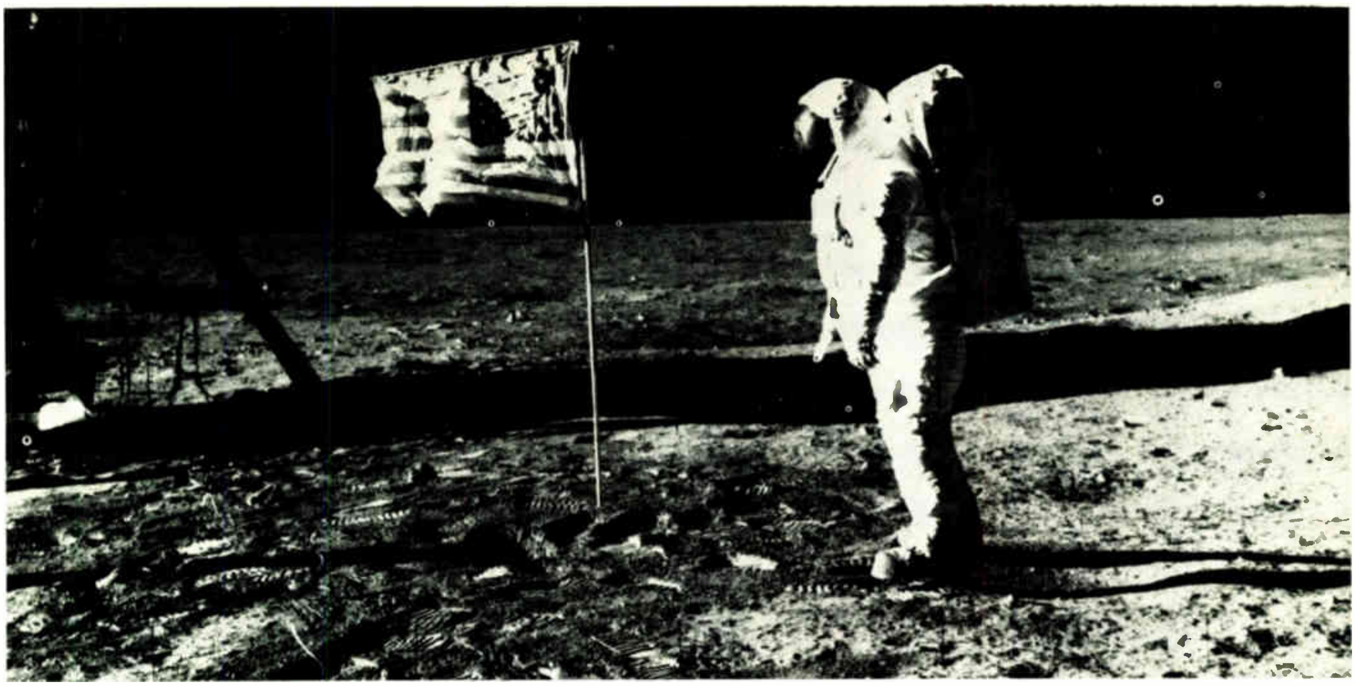
The process from the Lexington, Mass., firm efficiently uses energy, compared with other annealing processes like diffusion furnaces and lasers. The Varian system's heater uses 3 to 4 kilowatts intermittently, compared with the steady 20-kW drain of a diffusion furnace. Lasers, on the other hand, have thermal efficiencies of about 1%, along with a potential to damage oxide films.

Dual resists. Conformal masking, where a positive resist sensitive to near-ultraviolet light is placed over a thick layer of a deep-UV resist that provides a nearly planar surface, is about to take its place on the production floor. This process eliminates the depth-of-focus problems experienced in optically producing near-micrometer geometries in single-layer resists.

Conformal masking lets firms capitalize on the hundreds of millions of dollars of existing optical alignment equipment around. Two such pieces of equipment, from Machine Technology Inc., Whippany, N.J., and OAI Inc., Santa Clara, Calif., were shown for the first time at Semicon/West 81.

In the conformal masking procedure, which originated at IBM Corp., the silicon wafer with dual resists is first exposed to near-UV light in an optical aligner and the top layer is then developed. The wafer next undergoes a deep-UV blanket exposure in which the top layer acts as a mask. The deep-UV resist is then developed, resulting in a fine-line pattern with steep sides.

Stereo check. Nicolet Instrument Corp.'s XRD division in Cupertino, Calif., with its Mikrox inspection system, introduced a new method for checking encapsulated ICs that can detect die-attachment defects and minute broken wires. Like X-ray inspection, stereo radiography requires no disassembly of the package. However, it gives added sharpness through pairs of radiographs in much the same way that a stereoscopic microscope gives added depth



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CC	176,000	±3-±30	3-20
B	626,000	5-500	2-170
BN	112,000	5-48	25-100

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Circle 41 on reader service card

to an image. Yet it is not limited like X-ray test procedures to a 1:1 image.

Ferrofluidics Corp. of Nashua, N. H., announced that it is expanding beyond its traditional vacuum seal and subassembly business into the manufacture of crystal-growing furnaces.

Drawing upon technology from a recently acquired furnace line from Varian, Ferrofluidics intends a radical redesign to achieve a furnace capable of 60-, 40-, or the more traditional 20-kilogram crystal loads.

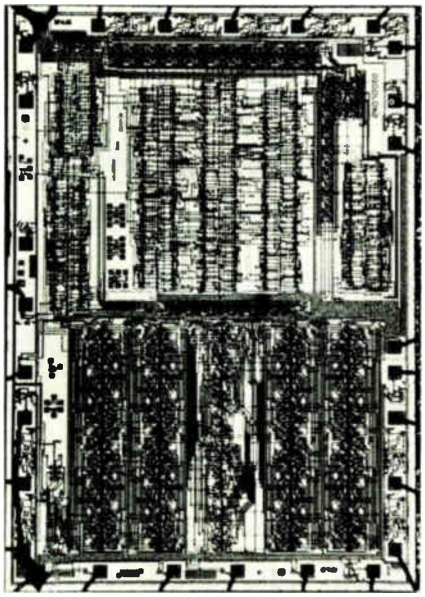
-Martin Marshall and Jerry Lyman

Instruments

Single-chip counter uses two logic types

By combining two Schottky logic forms on a single large-scale integrated circuit, Philips Test & Measurement Inc. has dramatically reduced the component count in its latest series of frequency counters. To make what amounts to a counter on a chip [*Electronics*, May 5, p. 216], designers in Jäfälla, Sweden associated with parent NV Philips Gloeilampenfabriken faced the seemingly contradictory combined design requirements of high speed and a large number of gates.

Multilogic. For its 667X counters, Philips developed this chip combining high-speed integrated Schottky logic (top) and high-density integrated injection logic (bottom).



They needed a one-chip solution for the 667X family of counters and future family members, according to product manager Jan van der Windt. "A split up of the 400 fast gates and the 1,150 low-speed gates on two chips would require too many pins for interconnection, in addition to the large number of input/output pins," he says.

Other requirements. For high-speed synchronization and logic control functions, the Philips designers found they needed jitter-free gate performance with delays of 4 nanoseconds or less to minimize timing errors. They also wanted the chip's back end to interface with a number of different types of microprocessors, so it had to be compatible with complementary-MOS and TTL voltage levels.

At the front end, they wanted the chip to work with emitter-coupled logic so that it could be mated with a front-end down converter to optionally extend the frequency range of the counter. They also wanted the chip's power consumption to be low so that portable units could be made.

Taking those design requirements to various suppliers produced disappointing results. "Especially because of the combined speed and gate requirements," van der Windt recalls, "no one was interested in or capable of fulfilling our needs."

A find. Fortunately, he found inside Philips an applicable type of logic—integrated Schottky logic [*Electronics*, June 8, 1978, p. 41]. At the time, Jan Lohstroh and his colleagues who developed ISL at the digital circuitry and memory group in Eindhoven, the Netherlands, had fabricated only parts like flip-flops and oscillators. Those parts exhibited the kind of speeds needed, with propagation delays of about 3.5 ns.

In theory, ISL could be combined with other types of logic, such as TTL, ECL, and C-MOS, on the same chip. Further, ISL consumed even less power than a fast logic like the low-power Schottky variety.

With a packing density of 150 gates per square millimeter, however, ISL alone would require too much space if all the gates were fabricated with it. So working, with Philips' intercompany custom LSI supplier, the counter group combined ISL with integrated injection logic on the same chip.

Combination. "Benefitting from the speed of ISL, the high density of I^2L, and the economy of a standard Schottky process, the new counter on a chip is now the first multilogic LSI," van der Windt maintains. The resultant chip, which measures 5.8 by 4 millimeters (228 by 157 mils) and has 28 pins, is manufactured by Signetics Corp., a Philips' subsidiary, using its SP4 process. Though the process already yields excellent results, according to van der Windt, further yield improvements are expected from an adapted process that is now being worked on, one that will be optimized for fabricating both ISL and I^2L.

-Richard W. Comerford

Consumer

Talking-game market has sales lockjaw

The boom is over for talking electronic games and toys. The latest word from makers of speech synthesis chips and their associated games is that the higher toy prices caused by adding speech have forced wholesale buyers away, which is contrary to some earlier market predictions.

This rapid cranking down of expectations has largely taken place since the Annual Toy Fair held in February in New York, when it seemed that talking toys could become extremely popular [*Electronics*, Feb. 24, p. 44]. But many participants now admit that they did not have a good inkling of what would sell, a condition that immediate market reaction corrected.

"Buyers say the toys cost too much for what they do," remarks Frederick M. Wickersham, speech marketing manager for National Semiconductor Corp., Santa Clara,

SCIENCE/SCOPE

The first of a new breed of communications satellites is providing secure voice, video, high-speed data, and electronic mail services for U.S. business firms and industries. The powerful SBS satellite is the first domestic communications spacecraft to operate at frequencies of 12 to 14 gigahertz. This means that small antennas with diameters of 5.5 to 7.7 meters can be used in urban areas for business communications without causing interference to terrestrial microwave systems. The satellite has an outer cylindrical panel of solar cells that drops down in orbit to expose an inner panel. The telescoping feature nearly doubles the power. Hughes built SBS for Satellite Business Systems, a company owned jointly by Aetna Life & Casualty, Comsat General Corp., and IBM Corp.

New radar technology may help solve increasingly nagging problems facing military strategists. The Track-While-Scan Quiet Radar, under exploratory development at Hughes for the U.S. Army Missile Command, would stand little chance of being detected, jammed, or destroyed by enemy radiation-seeking missiles. Quiet Radar differs from conventional radars in that it does not emit huge bursts of power in a sweeping pattern. Rather, it emits a low-power continuous-waveform signal while shooting out thousands of tiny narrow beams in a rapid-fire, randomly selected sequence. Extremely low sidelobe emissions and rapid random switching between many frequencies make detection of the radar difficult.

More than 15 years after its launch, NASA's Pioneer 6 spacecraft still transmits data via a Hughes traveling-wave tube. The interplanetary probe measured the sun's corona, studied solar storms, and measured a comet's tail. It also made many discoveries about the sun, solar wind, solar cosmic rays, and solar magnetic field. Pioneer 6's primary TWT operated more than 122,000 hours from launch in December 1965 until February 1980. Then, due to a low voltage condition, the backup TWT was switched on. The Hughes Model 214H TWT, which operates in the S band with 8 watts of power, was developed under contract to TRW.

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Measuring millimeter-wave impedance is easier now by using a new IMPATT-sourced millimeter-wave reflectometer instead of slotted lines and hybrid impedance bridges. Because of its unique design, the Hughes device can sweep the full 75-to-110 GHz bandwidth automatically without time-consuming point-to-point measurements. It uses such advanced technology as broadband isolators and detectors to reduce the effects of unwanted reflections and mismatch error, a 1-KHz square wave modulator that delivers increased sensitivity and dynamic range, and a rotary vane attenuator for constant attenuation with frequency.

Calif., which manufactures speech synthesis chips.

As a result, chip makers have greatly reoriented their projections for the consumer market, dropping it from first to third place behind industrial/telecommunications and computer uses. The outlook for electronic games and toys is so bleak, some say, that it would be no surprise if not one single new talking product shows up for Christmas.

TI's view. "We have not altered our original projections that the speech-synthesis market will reach $3 billion by 1991," says Bernard List, vice president and director of speech technology for Texas Instruments Inc.'s Midland, Texas, operation. "We overestimated the game and toy market when sales were booming between 1975 and 1979. For 1981, this market will be flat at best." Industrial/telecommunications and computer applications are much less price-sensitive.

In order for talking games to take off as steeply as the chip makers initially hoped, drastic cost-cutting moves are required. Instead of chips costing from $100 up per game, as they currently do, the needed cost is $3 to $4, says Wickersham. "And that's a ways down the road."

Besides the price problem, another limitation has been poor use of speech. "They have to be designed around speech, instead of crowbarring talk in as an afterthought or gimmick," points out Alfred Lubienski, general manager of the Votrax division of Federal Screw Works. The Troy, Mich., firm is a pioneer in speech synthesis, with some 10 years' experience. Agrees Wickersham, "They [the toy makers] just haven't come up with enough clever ideas."

Mum's the word. Industry sources agree that what is scaring toy makers away from pushing too hard too soon for flashy talking products is the example of Milton Bradley Co.'s Milton, which was introduced last year. This $80 phrase-matching game turned into a "complete disaster," as one competitor put it.

What's more, industry sources say that a new game, Say It Again, Sam, has been sidetracked as well. Spokesmen for Milton Bradley were not available for comment.

Other toy makers admit shelving 1981 plans, including Mattel Inc., Hawthorne, Calif., and Entex Industries, Compton, Calif. Mattel will go ahead with a speech module for its Intellivision package of electronic video games, but has delayed its introduction until early next year. Entex's Do As I Say, a $60 unit announced early this year, "is on the back burner for an indefinite period," says marketing vice president Nick Underhill.

Education OK. Although electronic games are on hold, a strong market case can be made for educational products that speak, since "educational values will command a higher price," says Wickersham. He is backed up by Tiger Electronic Toys Inc., Mundelein, Ill., where an official says its K-2-8 talking-learning computer "in no way is finding any downswing in interest." The unit has a suggested $99 retail price and has math, spelling, and reading modules at $25 each as learning aids.

Industry chatter also spots Mattel as shifting its sights from table-top toys that speak to the educational side. Reportedly, it is planning to introduce a children's learning center in 1982 or later.

Even TI, while downgrading the consumer market, is charging ahead with a new $60 educational game, Touch & Tell, that was unveiled at the Chicago Consumer Electronics Show. For the preschooler, it combines touch, and sound with a visual panel. **-Larry Waller**

Communications

Modem design uses linear filtering

Bell Laboratories is breathing new life into a moribund filter design for modulator-demodulators. Known as the fractionally spaced equalizer, the filter type has long been recognized as the best compensation for the distortion and noise that can ruin digital transmissions through a modem—but it has been very difficult to build.

Recently, however, researcher Richard D. Gitlin at Bell Labs'

Redundancy, laser rerouting gain

As debated as memory redundancy itself—particularly at today's density levels—the means used to swap in the extra bits and circuit elements is being contested now that laser zapping appears to be gaining on high-current melting of polysilicon fuses. The first round of memories with redundancy, which includes dynamic and static random-access memories from Intel Corp. and Inmos Corp. and even an erasable programmable read-only memory from Mostek Corp., burned the on-chip links with current pulses supplied while the wafers were probed for defects.

Newer RAMs from Mostek and perhaps Motorola will follow a lead established by Bell Laboratories [*Electronics*, May 22, 1980, p. 126] and open the fuses with laser light. Proponents cite easier layout, higher throughput, and reliability as reasons for choosing the latter method.

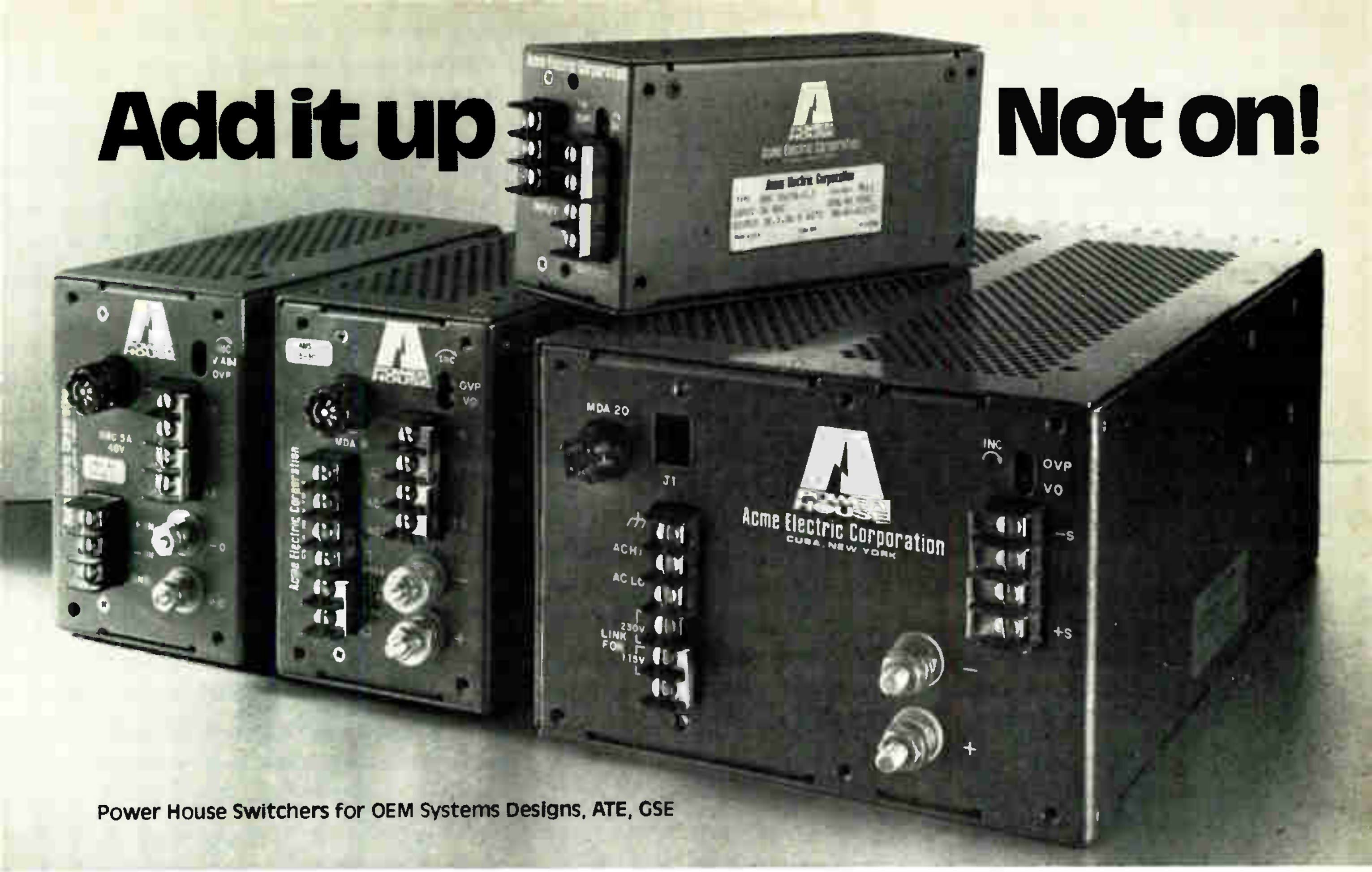
Mostek of Carrollton, Texas, plans to gradually phase in new fault-tolerant versions of its 64-K RAM during the last half of the year. Although it plans to begin shipment of the revised chip next quarter, the redundant circuitry will not actually be implemented until the final quarter. Mostek, which began shipping 64-K RAMs without redundancy in the first quarter of 1981, used its 16-K RAM as a learning vehicle for the laser technology.

Motorola Inc. is contemplating a redesign of its 64-K RAM to add redundancy, but it will not be implemented until next year, says Charles C. Silva, director of MOS memory operations in Austin, Texas. His operation is evaluating several techniques but is leaning toward the laser approach.

Meanwhile, Japanese RAM makers have so far opted not to add extra bits, saying that the area penalties still outweigh the advantages.

-J. Robert Lineback

Add it up ... Not on!



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Circle 45 on reader service card

Holmdel, N. J., facility was able to demonstrate how much the filter type improved on the performance of the standard synchronous equalizers.

At 9.6 kilobits a second—a data rate that is of importance for high-speed voice modems—a fractionally spaced equalizer with feedback "provides a 2-to-3-decibel gain in output signal-to-noise ratio, relative to the synchronous equalizer, over worst-case private-line telephone channels," Gitlin says. This gain translates into an improvement of two orders of magnitude in the bit error rate, he adds.

The fractionally spaced equalizer is a linear filter with taps closer to one another than the reciprocal of twice the highest frequency component in the signal being filtered. Synchronous equalizers are transversal filters with their taps at a distance from one another equal to the reciprocal of the data-signal rate. Until now the closer spacing has been hard to manufacture, but modern printed-circuit technology minimizes any problems.

Rivals react. Word of the Bell development has already made its way around the tightly knit world of modem makers and designers, and rival firms are watching closely. In fact, engineers from at least two U. S. modem makers acknowledge the practicality of fractionally spaced equalizers and say they are debating what to do about designing and testing them.

Although older modem designs can take care of phase distortion on the 9.6-kb/s channels, they are not as effective in reducing timing jitter, a strong point of the fractionally spaced equalizer. In Gitlin's view, the heightened demand for error-free data transmission is another reason to look at this filter design.

"It can deal with a wide range of delay distortions and cope more effectively with amplitude distortion than a synchronous equalizer," Gitlin says. As a bonus, he says, the transmission can be independent of the receiving modem's sampling phase because the equalizer synthesizes the correct delay needed to lock onto the signal. **-Harvey J. Hindin**

Components

Infrared LEDs shine in GaAlAs processes

Gallium aluminum arsenide as the active material in infrared-light-emitting diodes continues to gain momentum. TRW Optron, the Carrollton, Texas, electronic components division of TRW Inc., is introducing its first discrete GaAlAs devices, joining Xciton Corp. and General Electric Co., which have been marketing the GaAlAs infrared LEDs for more than a year.

Although activity is on the upswing, some industry experts say that it may be several years before GaAlAs replaces gallium arsenide. Others say it is still too early to predict a trend.

Others. Motorola Inc., Texas Instruments Inc., and Honeywell's Optoelectronics division (formerly Spectronics Inc.) are all developing GaAlAs in LED processes. So far, none has scheduled products for applications other than fiber optics.

The attractions that brought GaAlAs into prominence in fiber optics will also figure in infrared applications. Compared with GaAs, it can provide double the output for a given level of input. Optron also points out that GaAs diodes operate at a 935-nanometer wavelength, whereas GaAlAs units match silicon detectors, at 880 nm. This efficient coupling can improve detection efficiencies by up to 20%.

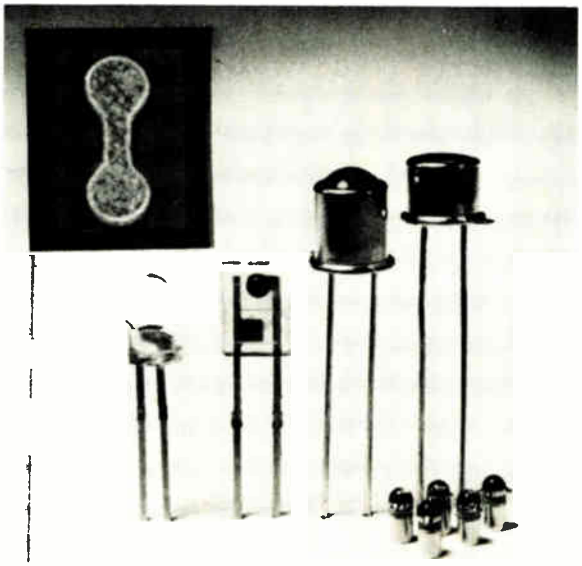
The main barrier is cost, says John Bliss, marketing manager for fiber-optic products at Motorola's High-Frequency Optoelectronics division in Phoenix, Ariz. "Gallium aluminum arsenide technology is new. The trip down the learning curve has not yet occurred," he says.

Questions. Texas Instruments Inc. is also conducting tests on LEDs made of GaAlAs material and designed for non-fiber-optic uses, says Jon Jackson, marketing manager for optoelectronics in the semiconductor group in Dallas. "Our concern is about degradation of power," Jackson says. "There are still some questions that we are asking, and we don't have the answers yet."

At TRW Optron, "gallium aluminum arsenide has No. 1 priority in the company as far as new product developments go," says Raymond A. Vineyard, vice president of engineering. Despite a 10% cost premium placed on the new process, Vineyard believes that many customers will be attracted to the benefits of GaAlAs. The company is introducing versions with a variety of outputs, and more will follow.

Typically, a GaAs LED will emit a total of 6 milliwatts radiant flux at 100 milliamperes. A GaAlAs LED, on the other hand, will emit 12 mW with the same drive current.

TRW Optron says that this feature will allow designers such new options as burning in, which slightly reduces an LED's output but stabilizes the device so that the output remains constant over a long period of time. Also, since GaAlAs requires half the current drive to produce a given light output level, it could be a big plus in



Protean. New gallium aluminum arsenide LEDs from TRW Optron come in a variety of packages and sport double the output power of the equivalent GaAs parts.

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When it comes to performance, both types are low power (30 mW max. standby, 275 mW max. active), single +5 V devices that are upward pin compatible with industry-standard 16K RAMs. All inputs and outputs are TTL compatible.

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battery-powered applications.

Xciton, which introduced its GaAlAs LEDs last year, says business is brisk. Paul Shaver, president of the Latham, N. Y., firm, says it is shipping between 250,000 and 750,000 GaAlAs devices a month.

"There has been a feeling in the industry that this is an experimental product," he says. "That's simply not true." Besides standard GaAs parts, Xciton offers 22 versions of the GaAlAs infrared LEDs and will unveil six new ones in the next three months. **-J. Robert Lineback**

Solid state

Programmed arrays are PAL offshoots

Monolithic Memories Inc., the Sunnyvale, Calif., firm that pioneered the development of programmable array logic chips, is seeking to cut out yet another niche in the fast-growing semicustom logic marketplace. Along with one of its alternative sources, National Semiconductor Corp., it is introducing what amounts to a mask-programmed PAL: hard array logic.

In many ways, the HAL is comparable to a gate array having many functions squeezed onto a silicon substrate, "with everything in place except for the metalization layer," says Shlomo Waser, Monolithic Memories' manager of product planning and applications. The layer differentiates these circuits as specified by the customer.

Unlike the conventional gate array, however, the HAL has a fusable prototype: PAL. The combination of the field-programmable array and a fast turnaround promised for the mask-programmed version will greatly speed system development time, the two companies maintain.

Product plans. Monolithic Memories is already providing HALs to a few large customers, with general availability slated for mid-year. Similarly, National plans to offer HALs, says Dave Uimari, marketing manager for the Santa Clara, Calif., firm's Bipolar Memory division.

National's first HALs are in design and are expected to be available by the end of the year. In quantities of 50,000 to 100,000 per year, Uimari anticipates, a medium HAL will cost between \$4 and \$6, which should be 40% to 60% less than a PAL at similar levels.

Monolithic Memories is fabricating the HAL family with its standard low-power Schottky TTL process. The mode of specifying HALs calls for the user to program and debug a PAL using an assembler that allows him to translate logic equations into a fuse pattern.

He supplies Monolithic Memories with a design specification for HALs

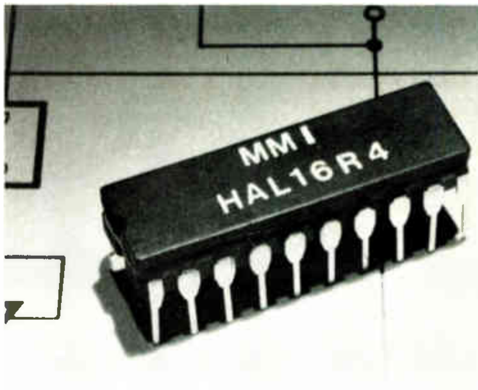
News briefs

Motorola strengthens semicustom bipolar gate-array services

Motorola Inc.'s Semiconductor Group starts an intensified push into semicustom bipolar large-scale gate arrays with the opening of its initial regional-design center, in San Jose, Calif., July 15. Motorola's MECL 10000 macrocell arrays, available for several years, have been aimed mostly at larger computer firms with their own on-site design.

The location of its first center, contiguous with Motorola's sales office in Silicon Valley, was chosen for a sophisticated customer base with potential interest in getting into TTL-compatible gate arrays. Nine more U. S. centers are planned through the end of next year, says Lincoln Young, manager of the centers for Motorola's Bipolar IC division, Mesa, Ariz. "This extends our computer-aided design resources out of Phoenix and makes it easy for them." he says.

Although the service is intended for eventual volume production of chips, having a regional advanced CAD front-end design capability will likely pull in customers whose limited volume needs have in the past ruled them out of the semicustom league.



Mask-programmed. Monolithic Memories is introducing its hard array logic family, essentially mask-programmed alternatives to its programmable array logic parts.

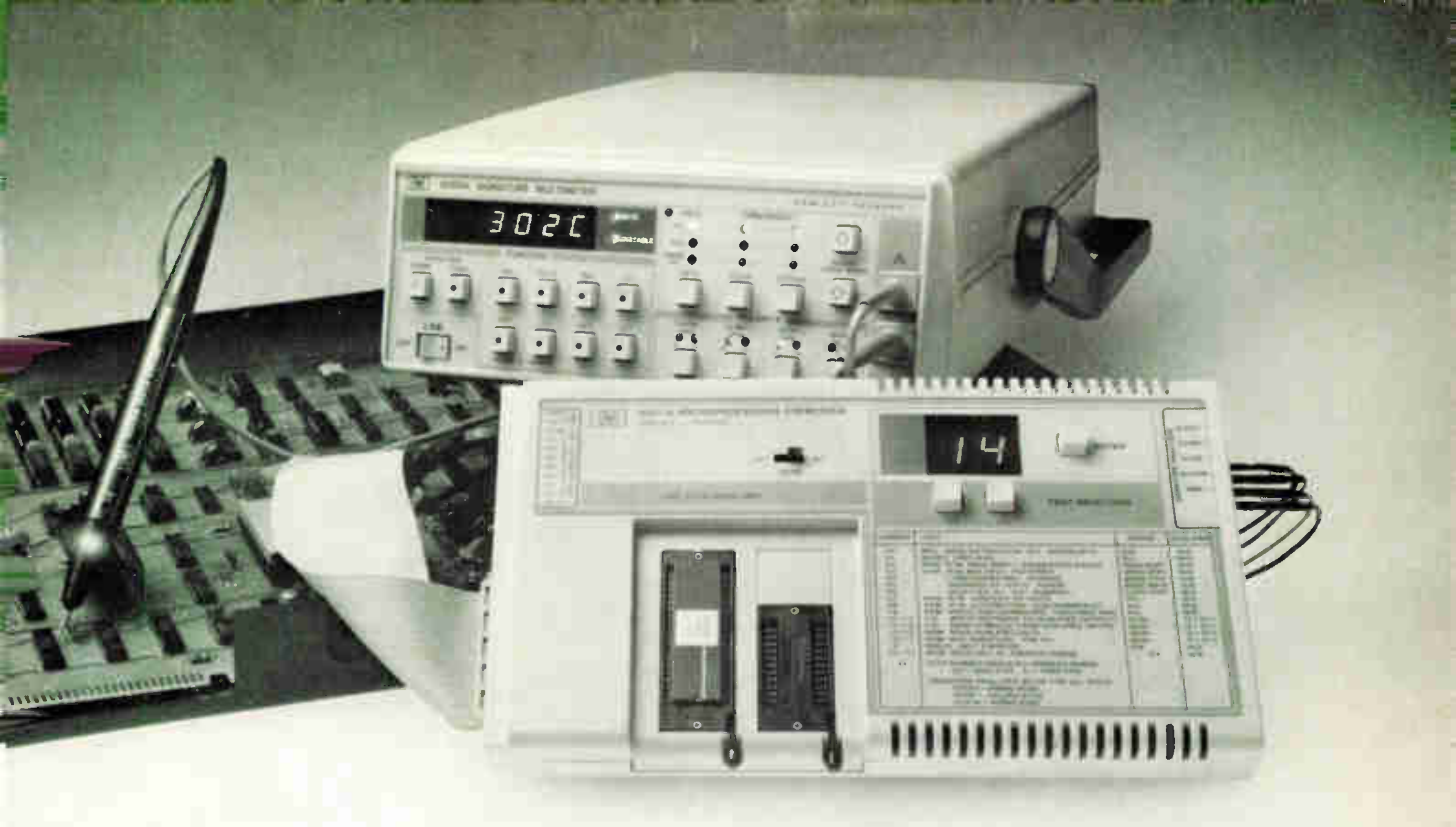
that a VAX-11/780 system uses to generate a mask-pattern tape. The standard format for the design specification contains part numbers, device names, a symbolic pin list, design equations, and a function table.

Monolithic Memories accepts this specification in one of three forms: a computer-generated listing, a typed or handwritten function-table format, or a direct transmission to the company's timesharing computer system. The specification is processed by computer and assigned a bit pattern number. From that point, the firm will provide a PAL sample for customer qualifications.

Predesign checking. Even before any fuses are blown in a PAL prototype, Monolithic Memories performs two major tasks: design verification and the generation of test vectors. According to Waser, a simulator has been added to the PAL assembler, which reads the function table and simulates the device as specified in the state equations detailing the transfer function.

The simulator checks the operation of the logic gates against the equations, thus verifying the designer's intention for the device. The function table that the customer specifies is also translated into seed vectors; that is, a minimum set of test vectors checking each node for stuck-high/-low operation.

Such automatic test-vector generation is a technique that has been employed during the last decade in



Now, HP has two more ways to cut digital troubleshooting costs.

5005A Signature Multimeter.

Before signature analysis (S.A.) troubleshooting microprocessor boards was tedious, time-consuming and costly. S.A. changed this by giving each complex bit stream its own unique hexadecimal signature, enabling technicians with minimum training to identify faulty nodes.

Now, the HP 5005A Signature Multimeter goes the next step by combining a high speed signature analyzer with a DMM, frequency/time interval counter and logic probe in one compact, lightweight package. This versatile combination adds a new level of convenience, making it easier than ever to track down faulty components in both service and production environments.

The 5005A Signature Multimeter offers features new to S.A.: preset logic thresholds for TTL, ECL and CMOS; variable thresholds (±12.5V); a clock-qualified Signature Analysis mode; and a 20 MHz clock rate coupled with a 10ns set-up time for high speed logic. It only weighs 8 lbs. (3.5 kg.), so it travels anywhere. The price is $2500.*

5001A Microprocessor Exerciser.

Here's a simple way to take advantage of S.A., even if it isn't designed into your product. Just insert your board's microprocessor into the new HP 5001A Microprocessor Exerciser, plug the 5001A into the empty board socket, and use its ROM to run test stimulus programs. The 51 self-contained S.A. stimulus programs thoroughly exercise the microprocessor, buses, ROM, RAM and I/O circuitry. Easily monitor the resulting signatures at your product's test points with HP's 5004A or 5005A Signature Analyzers. The 5001A is available for the 6800 microprocessor now—8085 and Z80 soon. 5001A price is $900.*

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03 A

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testing complex printed-circuit boards. However, Waser says, "what people use to do at the board level, they are now doing in silicon. Thus, the problem of testing digital logic is steadily moving from the printed-circuit board to the large-scale integrated chip."

Equally important, perhaps, is the speed with which engineers and manufacturers can begin designing and building systems that will use HALs. For example, the turnaround for just the first iteration of a gate array is typically 12 to 20 weeks, Waser notes, "and the average is at least two iterations. Thus the systems manufacturer is waiting about a half year to nine months before he gets his parts in silicon."

In contrast, PALs can be made available in a matter of hours or days, depending on the supplier. "The user need only wait about 10 weeks for a HAL to be put into silicon," he continues. "He can use PALs, albeit at a premium, if he needs to get into production very early." -Bruce LeBoss

Software

Verifiability sought for space shuttle

An intensive effort is under way to upgrade the space shuttle's software. It is unconnected with any fallout from the software glitch that delayed Columbia's first flight; rather it reflects the fact that the necessary procurement cycles for the shuttle program meant that the software is a far cry from the state of the art.

Thus the National Aeronautics and Space Administration's choice for a high-level language capable of handling the breadth and depth of the tasks that the shuttle software must perform is the almost 10 year-old HAL/S. But many of its features "are not susceptible to existing techniques of program proving and verification," says James C. Browne of the University of Texas's Institute for Computing Science in Austin.

The concept of verifiable software,

in fact, postdates HAL/S's inception. It is so new that even the much touted new high-level language, Ada, "is by no means fully verifiable," says Browne.

Basically, a language must be designed *a priori* to be verifiable, that is, programmers must write software whose algorithms can be proven mathematically to work. Nonverifiable programs must be proved out by use: either by test programs or in actual applications with different operating conditions that involve a wide variety of inputs having a wide lattitude in magnitude.

The glitch that delayed Columbia was a timing-skew problem among a set of four computers [*Electronics*, May 5, p. 48]. Browne emphasizes that at this point it is not clear if programming in a verifiable language would have caught it.

However, NASA does want to update HAL/S, which can perform such diverse functions as scientific computing, concurrent and real-time programming, and error handling. So it commissioned Browne to investigate the language's verifiability.

Already he has identified a verifiable subset, which he has dubbed HAL/S/V. True, it lacks scalar, matrix, and vector data types, among other features. But "there is much that has been retained, such as integer, character, Boolean, and bit-string data types, as well as most control features and input/output facilities," he says.

Ada next. There are many existing significant space shuttle programs that can be expressed in HAL/S/V, he says. Even so, he anticipates a move to Ada for future shuttle software.

"Ada is far more structured and incorporates the software advances of the last decade," he says. "Furthermore, it provides all the capabilities of HAL/S and can be interfaced with it." Thus existing software could be gradually rewritten from HAL/S into Ada.

Browne has already begun a verifiability study of Ada. There are no more verifiability tools for it than for HAL/S/V, he says, but "it is almost certain that some of these will be developed." **-Harvey J. Hindin**

Washington newsletter

U. S. to push sales of weapons overseas . . .

In addition to building up U. S. military forces, the Reagan Administration is readying new guidelines for sales of weapons systems abroad by American producers. The move should accelerate industry expansion **by removing most of the restrictions imposed in 1977 by President Carter.** Under the draft plan, the Carter Administration's ceiling on military hardware sales abroad would be removed, as would the prohibition on U. S. production and export of simplified systems for developing nations.

. . . as State Department takes policy lead

The new policy was outlined near the end of May by James L. Buckley, former Republican senator from New York and now under secretary of state for security assistance, science and technology, and by the State Department's Leslie Brown, deputy director for politico-military affairs, in separate industry appearances. Buckley addressed the Aerospace Industries Association, and Brown spoke before the American Defense Preparedness Committee. The new policy will complement and supplement U. S. defense efforts, Buckley said, and aid foreign policy **by strengthening American influence over the arms policies of other nations.** Carter's constraints under Presidential Directive 13, Buckley told the AIA, "substituted theology for a healthy sense of self-preservation" overseas.

Opposition strong to AT&T request for Custom Calling 2 . . .

The Department of Justice and more than a dozen communications equipment and services companies have come down hard against American Telephone & Telegraph Co.'s request to ease the rules so that Bell System companies can offer Custom Calling 2. AT&T seeks a 15-year waiver of the Second Computer Inquiry ruling in Federal Communications Commission Docket 20828, which calls for AT&T offerings of enhanced services through a separate subsidiary and encourages industry-wide competition. Custom Calling 2 uses voice storage and retrieval to answer, record, and deliver messages to any U. S. telephone on an unregulated basis. The Justice Department and the AT&T competitors urge denial of the waiver request, **maintaining that it would enhance AT&T's monopoly power and short out competition in the new market.** Among AT&T's opposition are such corporate heavyweights as Exxon Enterprises, IBM, Satellite Business Systems (which IBM dominates), and Xerox.

. . . new FCC members to deal with issue

The Custom Calling 2 dispute will be among the first to face Gary M. Epstein, Washington, D. C., attorney and engineer who was just named to head the Federal Communications Commission's Common Carrier Bureau by Mark S. Fowler, new FCC chairman. **Also expected to work on the issue will be Mary Ann (Mimi) Weyforth Dawson,** just confirmed by the Senate as an FCC commissioner for a seven-year term starting July 1. Dawson is a former aide to Sen. Robert Packwood (R., Ore.), chairman of the Commerce, Science & Transportation Committee.

Hughes wins incentive for SBS-1 success

Satellite Business Systems says that its first satellite, SBS-1, is expected to successfully meet its seven-year design-life goal and that the company has made its first performance incentive payment to California's Hughes Aircraft Co., the satellite's builder. The digital satellite, operating on a 14-GHz uplink and a 12-GHz downlink, began regular customer service in mid-March **and is steadily increasing its traffic volume as customer**

networks are cut over to operational service and expanded. The SBS-1 geostationary orbital position is "three times as tight as that of any previous satellite," according to the McLean, Va., company.

U. S. computer exports climb 40%

American exports of computers and related parts rose 40% to a record $7.53 billion in 1980, compared with the year before, while imports increased 20% to $1.15 billion, according to an analysis of Commerce Department data by the Computer and Business Equipment Manufacturers Association. Exports of word processors, calculators, copiers, and automatic typewriters raised the U. S. computer and business equipment total to $8.87 billion, up 35%, compared with a 16% gain for imports worth $2.97 billion. **The resulting positive trade balance of nearly $6 billion ranked third among all U. S. industry manufacturing groups,** exceeded only by such big-ticket industries as civilian aircraft and industrial machinery, with trade surpluses of $11 billion and $10.9 billion, respectively. (For the trade picture with Japan, see p. 102.)

Aerospace job growth to slow

Employment of engineers and scientists, as well as technicians, in the U. S. aerospace industry will continue to expand during 1981 and 1982, but at a slower pace. At the end of 1980, there were 196,000 jobs for engineers and scientists and 78,000 for technicians, respective increases of 10.7% and 13% from 1979. **Increases this year will be held to 2.5% for both categories and then rise by 5% in 1982,** according to a survey of manufacturers by the Aerospace Industries Association. The AIA data attributes the slower growth rates this year and next to a significant drop in the production of commercial jet transports, although the drop will be offset by gains in the fabrication of spacecraft, military aircraft, missiles, and related vehicles. Last year's unexpected surge in total aerospace jobs to 1.2 million represented an 11-year high for the industry.

NASA wants guidance on data processing

The dollar-starved National Aeronautics and Space Administration is soliciting free advice from industry and Government computer scientists this summer to guide future agency research and development in data processing. NASA will run a 10-week workshop beginning June 9 at a University of Maryland center in Port Deposit **to obtain "technical data and policy advice,"** says Paul Schneck of NASA's Goddard Space Flight Center, which will run the program. Workshop participants will be asked to prepare a technology assessment of computer science for NASA, draw up a model technology program identifying critical agency needs, and plan a model development program.

Harris wins Argentine network award

Harris International Telecommunications Inc. **will provide 38 domestic satellite earth stations to Argentina's national telephone company,** Entel, for a unified nationwide communications network, says the U. S. Export-Import Bank. The Melbourne, Fla., company won the $37 million competition when the bank agreed to lend $27.75 million for eight years at 8.75% interest to the Argentine company, which will make a cash payment of $5.55 million and obtain a private loan of $3.7 million. The bank, an independent Federal agency, assists in financing export sales.

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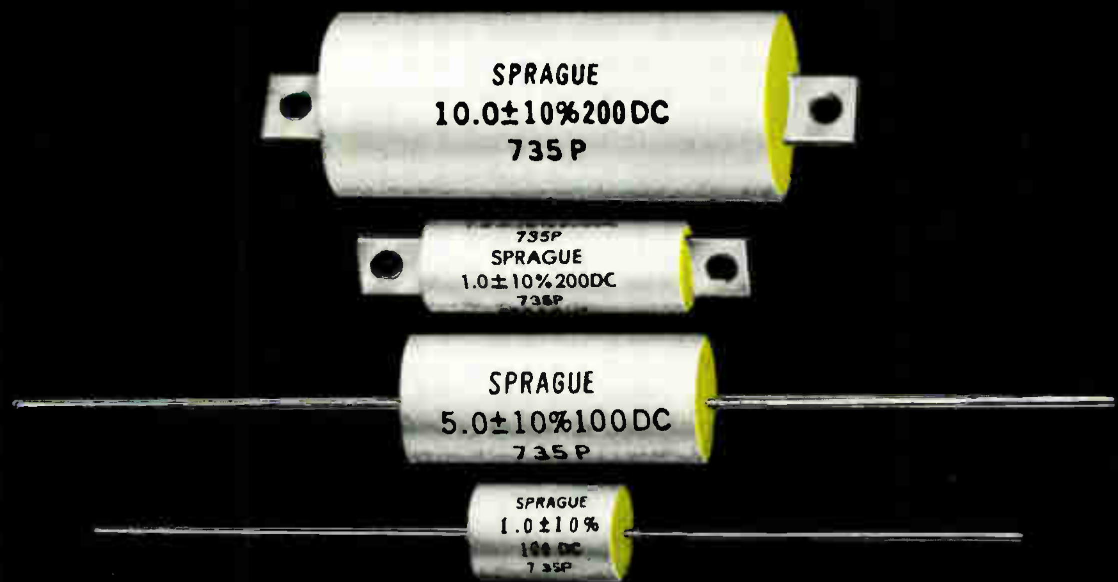

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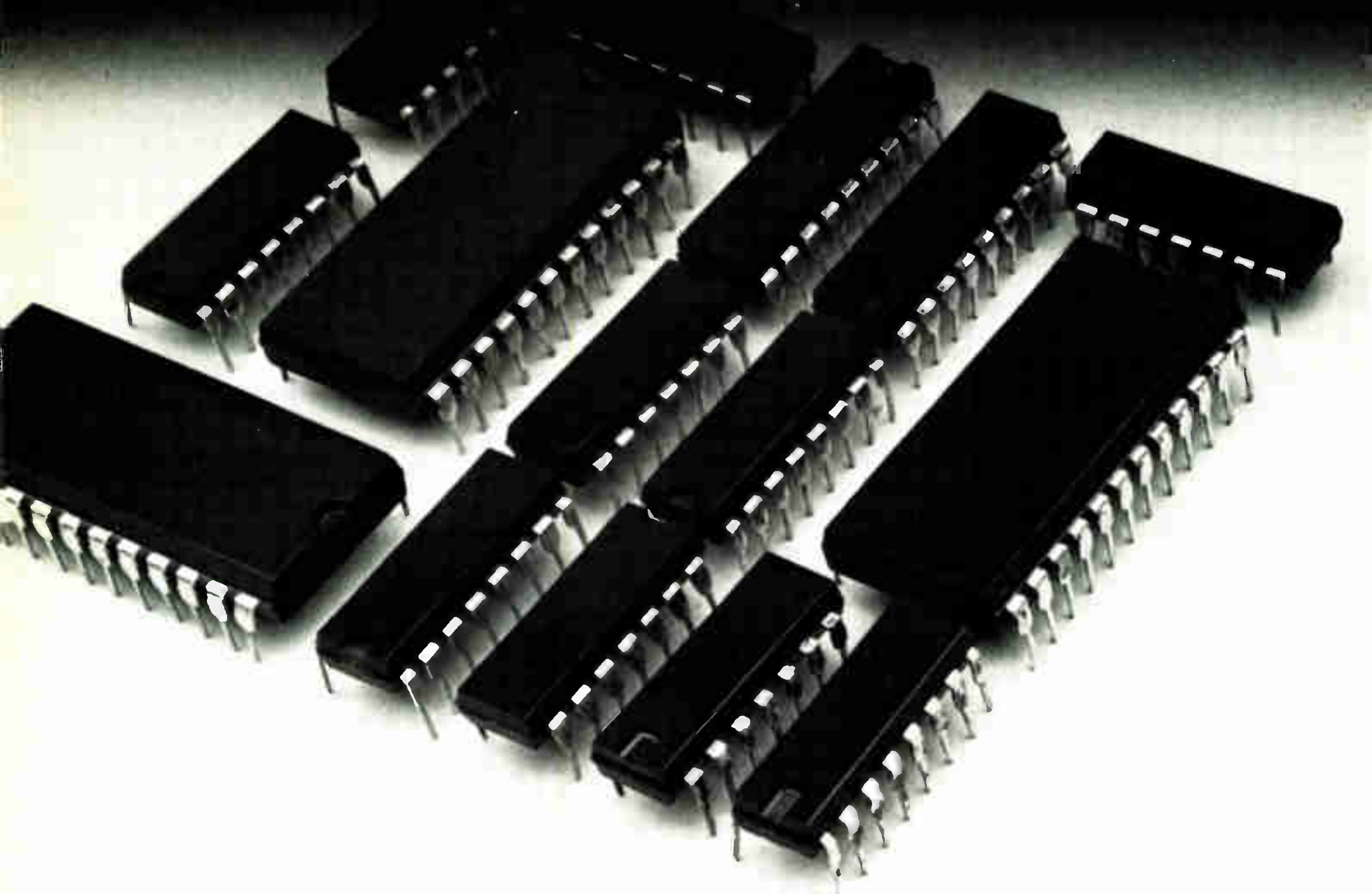

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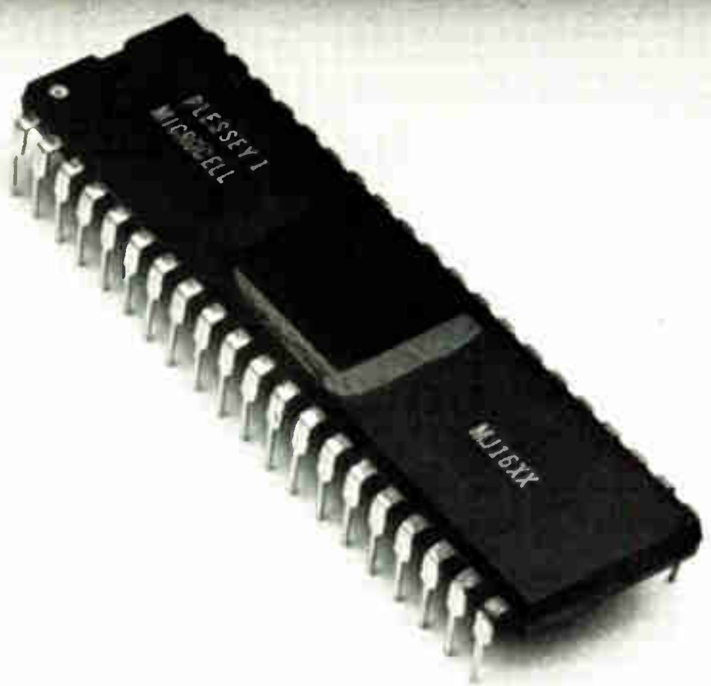

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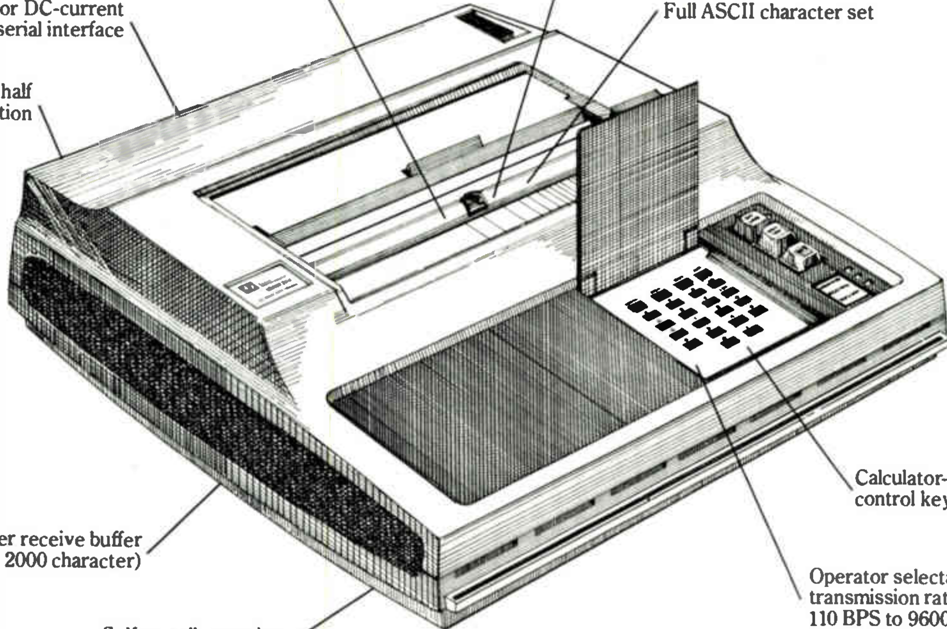

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Circle 62 on reader service card

Fujutsu tops its top-of-the-line mainframes

Announcement of its M-380 single-processor and M-382 two-processor mainframes by Fujitsu Ltd. for delivery by autumn 1982 completes the current round of Japanese machines to compete with IBM's 3081. The firm claims **a performance for the computers of 1.5 and 2.7 times, respectively, when compared with the 3081** and 2.1 to 2.5 and 3.8 to 4.5 times, respectively, when compared with its previous top-of-the-line M-200. The new computers, which follow 3081-competitive machines from Hitachi Ltd. and Nippon Electric Co. [*Electronics,* March 10, p. 71] feature the same technology as the DIPS 45/11 that Fujitsu is building for Nippon Telegraph & Telephone Public Corp. [*Electronics*, May 5, p. 71] and the Amdahl 5860 and 5880 [*Electronics,* Dec. 4, 1980, p. 41].

Fiber-optic cable to link Japan with Hawaii

Kokusai Denshin Denwa Co. (KDD), Japan's overseas telecommunications carrier, expects to use optical fiber for a transpacific cable between Hawaii and Japan by 1990. If the research and development go smoothly, there is a possibility that the third Pacific cable that has been discussed at the Pacific Operators Telecommunications Conference since 1977 will be optical fiber because the plan to lay that cable is two years behind schedule, whereas KDD's optical R&D is proceeding rapidly.

Meanwhile, the Musashino Electrical Communication Laboratory of Nippon Telegraph & Telephone Public Corp. has **successfully carried out tests of a 400-Mb/s repeater for an optical fiber link operating at 1.3 μm in water 700 meters deep.** Systems operating at this wavelength could have a spacing between repeaters of up to 25 km (16 miles). NTT is developing submarine cables to connect islands with Japan and also to take shortcuts across bays. Underwater optical cables are also being tested in the U. S. and the UK [*Electronics*, March 13, 1980, pp. 39 and 72].

Britain develops experimental processors for high-level languages

The research laboratories of Britain's Royal Signals and Radar Establishment, Malvern, is exploring two innovative computer architectures. One special-purpose multiprocessor, called Flex, is for writing operating systems, compilers, and other complex software in a high-level language with an efficiency normally associated with machine-code implementations. The microcoded instruction set is optimized to support high-level languages: the memory is protected by hardware, and **a single universal register can be set from 1 bit to the maximum store size.** Additional processors will be added to the first through a 2.5-Mb/s packet-switched bus. The second machine, engineered by Plessey Electronic Systems Research Ltd., Hampshire, is a fast general-purpose emulator with a 150-ns instruction time that can, for example, emulate a PDP-11/34 in real time. This 32-bit dual-processor system, called Gemini, supports the Flex instruction set.

256-K ROM accesses in 150 ns

Toshiba Corp. will use the same 2-μm design-rule technology that it developed for its 64-K MOS dynamic random-access memory to build a 256-K read-only memory having a maximum access time of only 150 ns. That makes it suitable for use with cathode-ray-tube displays, as well as printers, whereas slower large memories are limited mainly to printers and liquid-crystal displays. The ROM is also suitable for compilers and similar software applications, but in Japan the main use initially will probably be for displays featuring kanji (Chinese) characters. Nine devices can store

4,096 characters as a 24-by-24-dot matrix—a sufficient character set size in a legible format [*Electronics*, May 19, p. 84]. Toshiba's T6746 operates from a single 5-V power supply with a maximum power consumption of 220 mW when operating and 44 mW on standby; its minimum cycle time is 230 ns. The chip measures 179 by 210 mils (4.55 by 5.34 mm) and comes in a 28-pin dual in-line package.

At the same time Sharp Corp. has developed **a low-power 256-K n-well complementary-MOS ROM,** the LH53256, with a typical access time of 500 ns. Use of 2.5-μm rules keeps chip size to a manageable 236 by 235 mils (6.00 by 5.98 mm). It is molded in a 44-pin flat package.

Personal computer from Japan opts for dual processors . . .

Two 6809 microprocessors improve the speed and efficiency of a personal computer with a color graphics capability developed by Fujitsu Ltd. They also provide a total of 128-K bytes of memory space—64-K bytes for a user's programs, including interpreter or compiler, and another 64-K bytes for the display and keyboard. **Eight 64-K dynamic random-access memories form the user's memory,** with an overlay of four 64-K read-only memories containing a 32-K-byte Extended Basic interpreter. An optional software card with a Z80A and about 10 other chips convert the computer into a disk-based CP/M-compatible system that operates at the somewhat lower performance of the Z80A (compared with the 6809).

In addition to Basic and CP/M, UCSD Pascal and Flex operating systems are available, as are a complete line of interfaces and a 32-kilobyte bubble cassette. The minimum configuration of the Micro 8, shipments of which will start at the end of July, consists of the basic computer with built-in keyboard for some $975 and a home TV adapter for $60.

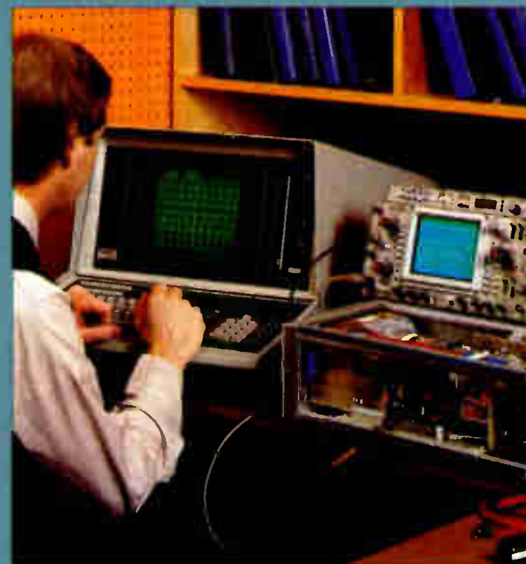
. . . while another adopts bubble cassettes

Removable bubble cassettes and 8-in. floppy disks using IBM- and Facom-compatible formatting are selling points of the Bubcom 80 microcomputer designed by System Formulate Corp. and built for it by Fujitsu Ltd.'s Components Group. The computer is built around a Z80A with 64-K bytes of random-access memory. It runs on the CP/M operating system featuring the latest version of Microsoft Basic. The Bubcom 80 comes with one bubble holder and space for a second to be attached easily. **Bubble cartridges contain 32 kilobytes now, with 128-kilobyte cartridges scheduled for next year.** In Japan, the Bubcom 80 costs some $1,140 with one and $1,325 with two bubble holders. Bubble cartridges cost $133 each.

West German P. O. to automate telegrams

To speed up telegram communications, the West German post office plans to put into operation in 1983 a $10 million computer-controlled system that will automate all routine jobs now handled manually. The agency **has contracted Frankfort-based AEG-Telefunken to supply some 400 intelligent cathode-ray-tube terminals, to be installed throughout the country, as well as a large computer system,** to be located at a center in Frankfurt. Telegrams can be phoned in to personnel at the CRT terminal, which will relay them to the center, or sent straight to the center by Telex. The system will automate such jobs as counting words, determining rates, accounting, transmitting and archiving messages, and keep compiling statistics on telegram traffic. It will handle a single telegram in less than 10 minutes even during heavy traffic hours.

New powers of waveform analysis. From th



(above right) The Tektronix 468 portable digital storage oscilloscope becomes part of a powerful processing system when interfaced to the Tektronix 4052 Computer/Controller for analysis and processing.

(above left) Users can link the Tektronix 492P Spectrum Analyzer with the 4052 to compare accumulated displays over successive sweeps. Right at hand are high-speed analysis, plus permanent records via the Tektronix hard copiers.

(far right) The Tektronix 7854 Oscilloscope interfaces with the 4052 to apply high-speed floating point calculations and simultaneous display of high-resolution graphics and tabular data to the most complex analytical problems.

(below left) To state-of-the-art Tektronix GPIB waveform measurement instruments you can add the analytical capabilities of the 19-inch 4054 computer/controller for problems requiring both speed and large data display, the fast 4052 for computationally intensive applications, or the economical, general-purpose 4051.

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"As a first time ATE user, Milton Bradley's major concerns were ease of use and total system capability. We got both with the 303."
John Scalia
Electronics Manufacturing Engineering Manager

"Before we made a final buying decision on any in-circuit test system, we had to be convinced of two things. One, would the ATE company provide the in-depth pro-

Dave Otto,
Test Engineer,
Sykes Datatronics Inc.

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"Back in 1978, Sykes Datatronics thought the best in-circuit system for isolating manufacturing faults was the 303. Today, we still think it's the best system."
Dave Otto
Test Engineer Sykes Datatronics Inc

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"Based on past performance, we've just placed an order for another 303."

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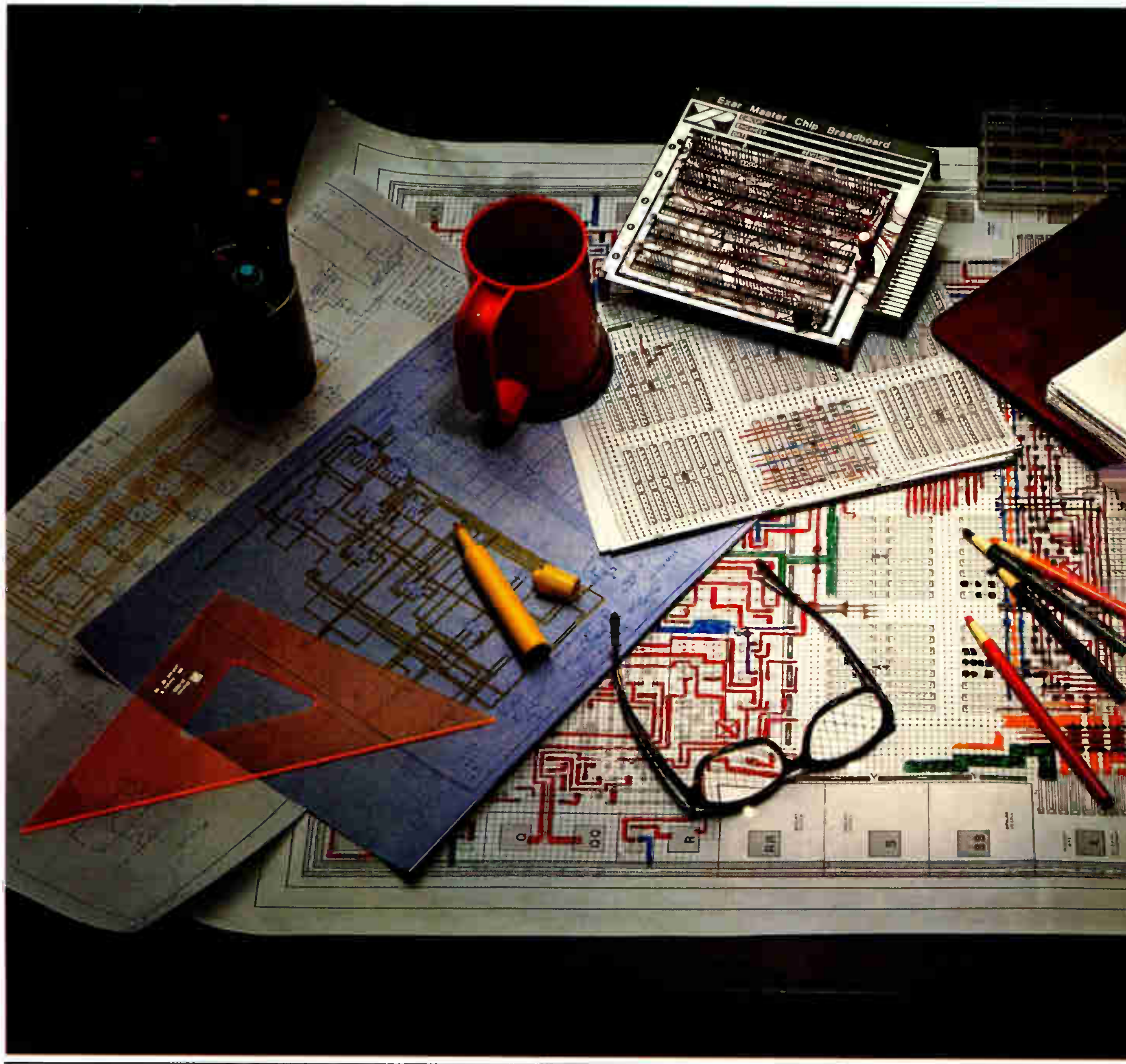

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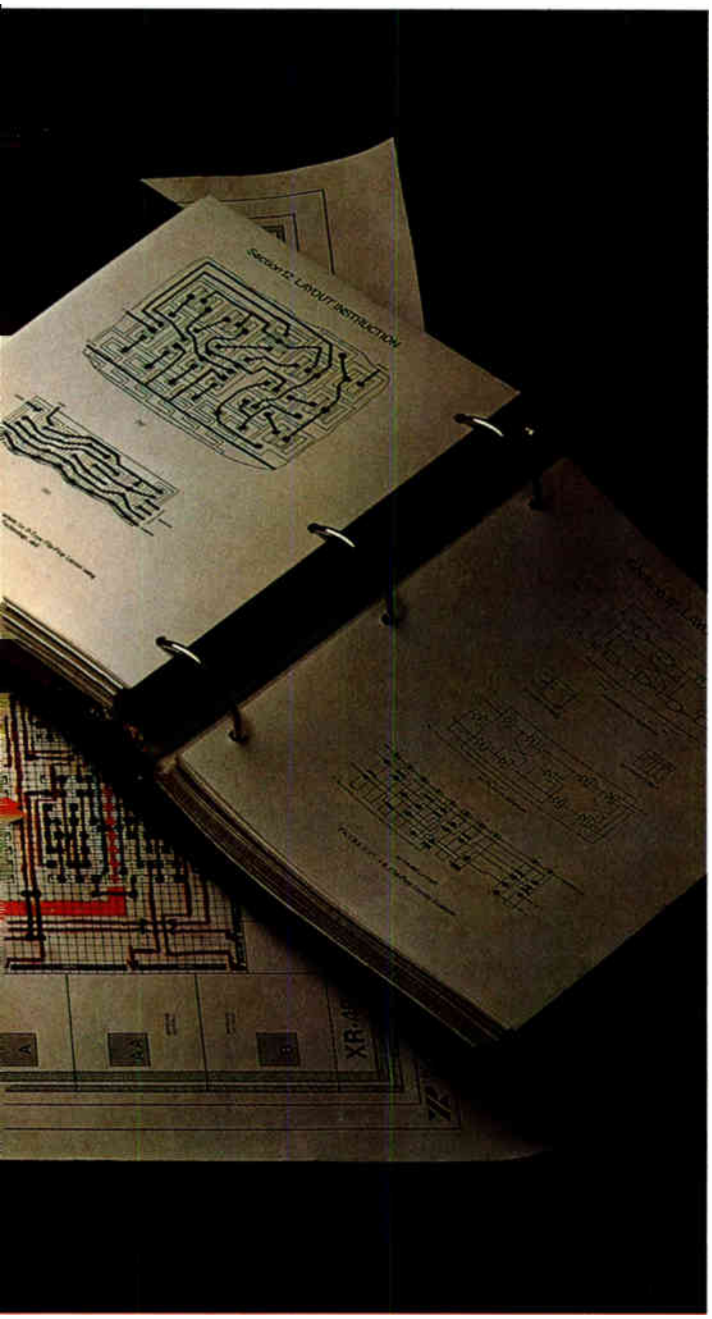

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Fiber optics point the way to solid-state gyro

by John Gosch, Frankfurt bureau manager

Work in Siemens lab using off-the-shelf components and miniaturization aims at resolution of 0.01°/hour

Using standard optoelectronic components such as laser diodes, glass fibers, optical filters, and photodiodes, researchers at West Germany's Siemens AG have developed an experimental rotation sensor that could lead to a compact, lightweight, and inexpensive high-resolution optical gyroscope. Such a device might find wide use as an air-navigation aid—even in small aircraft—and help make flying safer.

The researchers have achieved resolution values of several degrees per hour. That would suffice for torpedoes and other self-propelled missiles traveling over short distances, but for aircraft on long-distance flights, figures of around 0.01°/hour are called for.

That should be achievable with more refined methods for evaluating the results and, particularly, by system miniaturization. Eventually, says Gerhard Schiffner, head of the team that worked at the firm's Munich-based research laboratories, resolution values approaching 0.001°/hour should be obtainable. Work is continuing toward that end, and a commercial "fiber gyroscope," which he expects could be ready "within a few years," could be made to fit inside a cylindrical case 8 to 10 centimeters in diameter and 2 to 3 cm high.

The Siemens scientists worked several years with their fiber gyro to get around the shortcomings of mechanical designs, Schiffner points out. Those long-established mechanical gyros have long been prime targets for replacement. Though high in resolution, they are sensitive to shock and vibration and have a relatively long settling time—in some cases up to half an hour. What's more, they suffer from the drawbacks associated with the bearings of the rotating mass. And despite frequent maintenance, reliability is limited.

The fiber gyro also promises to outperform the ring interferometers or ring lasers of more recent manufacture. Though they too are highly resolving—a value of 0.01°/hour is common—they are elaborate, using special mirrors, a gas laser, a high-voltage power supply, and other space-consuming parts. Ring lasers are also costly to fabricate. In contrast, the solid-state fiber gyro saves space, is highly reliable and simple to implement, and lends itself to mass fabrication, Schiffner notes.

In the Siemens experimental setup the optical fiber is 500 to 1,000 meters long and is wound on a coil about 12 cm in diameter. By means of a beam splitter, the light from a semiconductor laser is coupled into both ends of the fiber. The light waves enamating from the fiber ends superimpose upon each other and impinge upon two photodiodes.

Sanac effect. If this setup is rotated about an axis perpendicular to the surface, the so-called Sanac effect, a relativistic phenomenon, is observed: the time it takes for the light to travel through the fiber is a bit longer in one direction of rotation than it is in the opposite direction. In effect, the light is modulated by the phase difference between the two light waves coming from the fiber ends. That phase difference, in turn, alters the power outputs at the two photodiodes. The power difference, in microwatts, is an indication of the velocity of rotation.

Normally, at very low angular velocities—on the order of several degrees per hour—it is virtually impossible to determine the sign or magnitude of such velocities. Therefore, Schiffner and his colleague have devised a method allowing unambiguous measurements to be made by superimposing an angular velocity of a certain frequency on the

Moving toward the new gyros

The team that has produced an experimental solid-state optical gyroscope at Siemens AG in Munich believes that it has achieved higher resolution, more miniaturization, and better evaluation of results than competitors around the world. Other work on optical gyros is going on at, for example, Rockwell International Corp. in Anaheim, Calif., Honeywell Inc. in Minneapolis, the Naval Ocean Systems Center in San Diego, Calif., and at other firms in the U.S. In France, Thomson-CSF is pursuing an optical gyro. And another West German firm, AEG-Telefunken, has an experimental setup with which it has measured a drift rate of 10°/hour and a noise equivalent rotation of 1.25°/hour. **-J. G.**

unknown angular velocity. The light source, a gallium arsenide injection-laser diode, produces several milliwatts at a wavelength of 850 nanometers. A polarizing filter at each fiber end ensures that the fiber portion wound on the coil acts like a reciprocal two-port device.

Great Britain

Package turns software specs into fully coded bug-free Basic program

It doesn't take the thinking out of writing computer programs, but a soon-to-be launched software package from DJ:AI Systems Ltd. does promise to eliminate the drudgery. It automatically translates a software designer's program specifications—worked out beforehand as a flow chart—into a fully coded bug-free program in Basic.

Last one? Its developers, David James and Scotty R. G. Bambury, call their package "The Last One," implying that it is the last program that need ever be written, and they are promoting it in advance of a July launch with an overstatement that is unusual for the English. The $600 package will run on most popular personal computers configured with 32-K bytes of memory and twin 5¼-inch disk drives.

The Last One is not unique in its objectives: it is one of a raft of automatic program generators now emerging—primarily in the U. S.—allowing unskilled users to generate application software by responding to a menu of questions [*Electronics*, April 7, p. 39]. David James points out that most of these products work by stringing together subroutines. His package works by isolating logically self-contained programming operations.

For example, Pro-4, marketed by General Automation Inc., assembles programs from over 100 subroutines. Nearest in concept to The Last One is Pearl, a Basic language program generator from CPU International Inc. in Salem, Ore., which allows a wide range of business applications to be generated for microprocessor-based computers running the CP/M operating system.

James has analyzed the programming task into a number of logically self-contained programming activities that are held in an index. During program creation, the operator works through a logical tree structure, choosing from a menu of operations at every step. The approach, claims James, is more flexible and produces more compact, faster running code.

The program generater elicits from the user a complete description of the files needed, as well as any procedural requirements describing how people will execute transactions, search for and update information, or perform calculations. The Last One structures the program employing two strategies to separately optimize speed and compactness and then chooses between them.

Then it compiles the program, producing a Basic program listing, which should run the first time. If it does not, the fault will lie in the original program specification.

Since the program is designed from the top down, it is an easy enough matter to modify it, leaving the computer to generate the modified program listing; hence program writing and debugging can be speeded tenfold. The ability to modify programs, says Bambury, is crucial, since modifying a standard business package can be costly.

Just as important, any program so written is readily transportable from machine to machine. That is because any application program is described in its own internal language.

Working with DJ:AI, Crystal Electronics Ltd., Torquay, Devon., is transferring the software package developed on an Ohio Scientific computer to Pet, Apple, Tandy and Sharp microcomputers, as well as to the CP/M operating system, an activity it has built its reputation on. It also plans to make the system easier for users, adding more operator cues.

Basic is of course a simple language. But Crystal Electronics' managing director, T. F. Brownen, sees no problem in applying the techniques employed in The Last One to other languages and hints that such a move is likely. **-Kevin Smith**

France

Six CRTs supply cockpit information in color via central monitoring system

The biennial Paris air show can be classified as a running debate—interspersed with stunning demonstrations of flying—over the relative merits of aerospace hardware of all sorts. However, during the 34th Salon International de l'Aeronautique et de l'Espace, June 4–14, at Le Bourget Airport, the six-cathode-ray-tube layout that Airbus Industrie has designed into the basic version of the A310 Airbus should find no other contenders for the title of the classiest cockpit in the upcoming airliners.

Thomson-CSF, the supplier of the full-color electronic cockpit system is unveiling a working model at the show. It will start delivering production versions this month to the A310's builder, Airbus Industrie—a grouping of the leading airframe makers in France, the UK, and West Germany.

For the 210-passenger wide-body jet, scheduled to fly for the first time early next year, Airbus Industrie's avionics designers decided to go fully digital, tying computers for flight control, navigation, and housekeeping onto a 32-bit Arinc bus. In a sense, the electronic cockpit displays

Chief Engineer

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Full color and computerized. The A-310 Airbus will have an instrument panel with six CRTs: two in front of the pilot, two in front of the copilot (not shown), and two between them.

can be considered as intelligent terminals for the pilot and copilot, says Jean-Paul Langlet, a marketing executive with Thomson's Avionics Equipment division.

Colorful. Because they are tied into what amounts to an extensive computer system and because they can gain attention with color, the displays can provide pilots with a wealth of information that simply cannot be developed by conventional analog instruments.

The photograph shows four of the CRT displays. In front of the pilot are two 5-inch displays, one atop the other, that make up the electronic flight-instrument system—along with two identical units (not shown) in front of the copilot. The two fliers share the two displays that make up the centralized aircraft monitoring system, located above the pilot's right hand in the photograph.

The top CRT in the flight system has an artificial horizon with a blue sky and shows standard information like air speed, plus critical points like the safety zone above stall speed. It also includes the radio altimeter readout, which can change color and boost its readout size as the altitude drops, finally turning red at the decisive height where a pilot has the last chance to pull up before landing.

The lower CRT in the flight system is the navigation display. It shows a video image of a conventional compass rose, but it also can show navigation charts and special displays for takeoff, approach, and landing at specific airports.

The lefthand display in the monitoring pair will warn of faults in such essential systems as the brakes and the hydraulics, giving instructions on corrective actions. The righthand display provides syntopic diagrams of the faulty subsystem, which changes to reflect the results of the pilot's actions. At other times, these displays show cabin-status information and the like.

On their own. The data picked off the bus by the display system originates in outside computers, but both systems have processor circuits of their own to decode signals and generate the display. For the flight system, the more complex of the two, there are three identical processors. one each for the pilot and copilot displays, plus a backup.

Essentially, each signal-generator processor consists of a custom image-processor chip, a custom X-Y converter chip to develop analog drive voltages for the CRT, a control unit based on standard parts of the Advanced Micro Devices 2900 bipolar bit-slice family, and some 64-K of random-access memory.

For the monitoring system there are two similar signal generators with slightly less memory, either of which can drive both displays if the other fails. Despite the redundancy in the electronic displays, the A310 has a full complement of key electromechanical instruments.

Supplied. Although it designed the display system and has overall responsibility to Airbus Industrie for them, Thomson-CSF does not fabricate the signal-generator processors itself. They come from the avionics subsidiary of VDO Adolf Schindling AG of Frankfurt.

Thomson-CSF supplies the display tubes and their drives. Since blue is not possible with penetration tubes, there are high-resolution shadow-mask tubes instead. Half the second frame period is used for a vertical raster scan to paint in the sky and land background. Characters then are written in during the second half by vector scan. **-Arthur Erikson**

Japan

Translators get speaking parts

Recent silence on the introduction of voice synthesis products is about to be broken again as two Japanese companies introduce talking translators. By late June or July, Sharp Corp., Osaka, and Casio Computer Co., Tokyo, both plan to start shipping units that are alike in design and function but different in their speech synthesis techniques.

Casio announced its VT-100 voice translator first, in February [*Electronics*, March 10, p. 68]. Sharp followed just last month with its IQ-5000, a talking version of the IQ-

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Circle 77 on reader service card

3100 electronic translator it has been selling for about a year. The VT-100 measures 7.7 by 3.8 by 1.2 inches and weighs 16.3 ounces, against 7.8 by 3.9 by 1.3 in. and 15.8 oz for the IQ-5000. The VT-100 uses four penlight batteries and the IQ-5000 three. Casio's dot-matrix liquid crystal display contains 22 letters against Sharp's 23.

Both feature a male voice speaking American-accented English. They also have a search function that lets the user insert alternative key words, such as airline names or street numbers, into basic programmed sentences.

Talkative. To operate the translators, the user selects a category such as "airport" or "telephone." A basic sentence appears on the display in Japanese phonetic kana characters, with certain key words in parentheses. If the sentence is not what he or she is looking for, the user pushes a button calling up the next sentence.

After finding the appropriate basic sentence and replacing any necessary key words, like specific names, the user simply pushes a button to vocalize the sentence in English. To learn the English equivalent of a Japanese word, he or she pushes kana character keys to spell out the Japanese word on the display, then hits a button to get the English. The same process can be done in reverse to learn the Japanese meaning of an English word.

Both models have space for a third language module, of which Sharp already sells six. However, neither one can vocalize information from those modules.

Contrasts. Still, there are differences between the two. Casio's model boasts a larger memory—nine 192-K read-only memories versus Sharp's nine 128-K and one 192-K ROMs. That lets the VT-100 display and vocalize (in English only) 264 basic sentences in 12 categories and display 2,508 words in both English and Japanese. It also contains a time clock displaying the time in 24 cities around the world and an alarm func-

CAD system tackles software

Computer-aided design stations are coming to the aid of software engineers these days. British Telecom's Martlesham Research Centre, for example, is developing a fully interactive work station called Cados, for computer-aided design of software.

On its cathode-ray-tube display, a user will be able to represent real-time programs pictorially, using an advanced form of flow diagram developed initially at Essex University. The result will be a high-level source code created from the diagram.

During a nine-month trial period, it prepared five program modules for Britain's System X digital exchange in one quarter to one fifth the time normally taken—and four of the five modules performed the first time. The Cados team's output of 7,000 words per man-year was three to four times the world average, according to the research group. Accurate software documentation such as flow charts and transition diagrams were automatically generated alongside the finished source code.

Because the documentation always matches the code, flow charts—and not the source code—could become the final product of the programmer's work. To use Cados, the programmer first enters his chart in a very free format, defining each flow box type and its functions. The system checks that it is valid then lays it out to System X standards. The computer can automatically produce an equivalent high-level language source code, according to the research center.

The procedure involves the use of interactive graphics techniques so that the software engineer can draw programs on a CRT instead of entering them in a program language. Martlesham researchers have borrowed many techniques already provided in British Telecom's Polygon CAD program for laying out integrated circuits. This program employs two screens—one for high-resolution graphics and the other for procedure prompts. **-K. S.**

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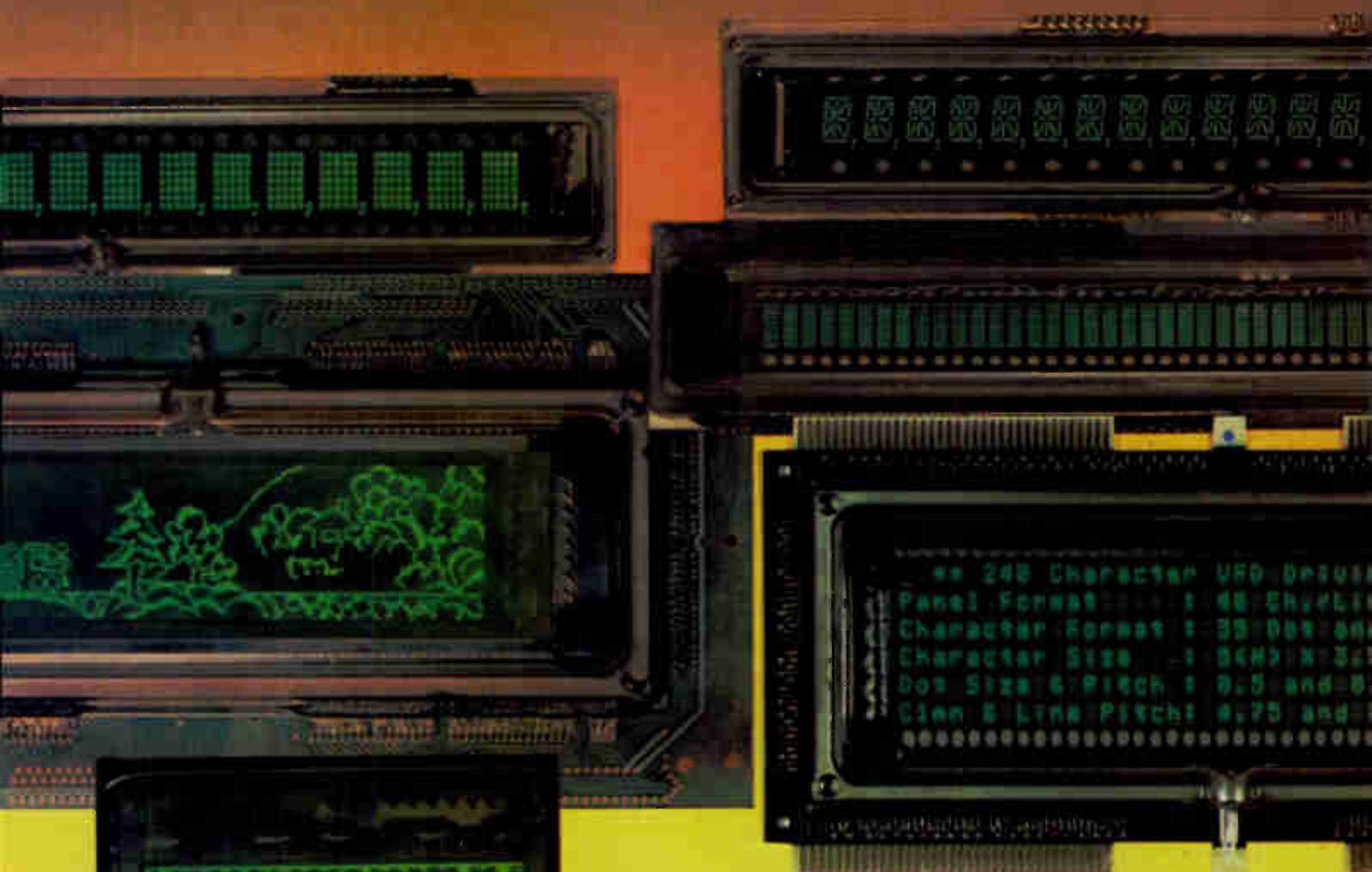

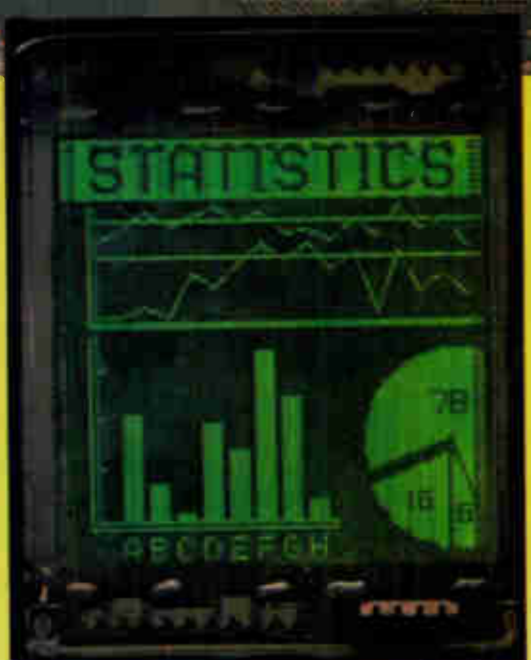

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tion with five spoken Japanese messages such as, "It's time for your meeting."

Sharp's IQ-5000, in comparison, contains 152 sentences in 14 categories and another 2,000 words in both languages, of which 400 can be vocalized in English. It utters the 84 basic Japanese phonemes, which the VT-100 does not, but lacks a time clock and alarm. Sharp claims that its search function offers more alternative words than Casio's, combining into about 3,000 different sentences; Casio, for its part, says it has not counted.

Synthesis types. Sharp calls its self-developed speech synthesis technology "sign-wave superimposition." The bit rate for the IQ-5000 is 1.2 kilobits/second. An 8-bit complementary-MOS central processing unit with a 2-megahertz clock uses one 128-K program ROM, four 128-K voice synthesis ROMs, and one 192-K and five 128-K ROMs for both vocabulary and voice.

Casio is using a Parcor synthesizer from Hitachi Ltd. but will reveal no details. More candid than Casio, Sharp has announced a list price in Japan of about $317 and an initial production volume of 5,000 units per month. The speech function thus adds some $136 to the otherwise similar IQ-3100. Casio will reveal neither price nor volume, but an official there says that "we're about the same as Sharp. Our price won't be much different."

Both companies are aiming their talking translators squarely at Japanese travelers. Sharp says it will eventually export a modified version, but exports of its two nontalking translators are running at under 20% of shipments, mainly to Europe. Casio, on the other hand, sees very little opportunity abroad.

Although Sharp has sold about 100,000 of its basic translators, market experts doubt the companies will find many buyers for their talking machines. "I'm not positive about the short-term market potential," says a Tokyo securities analyst. "It's just like a toy at the moment and will be very troublesome for tourists to use." **-Robert Neff**

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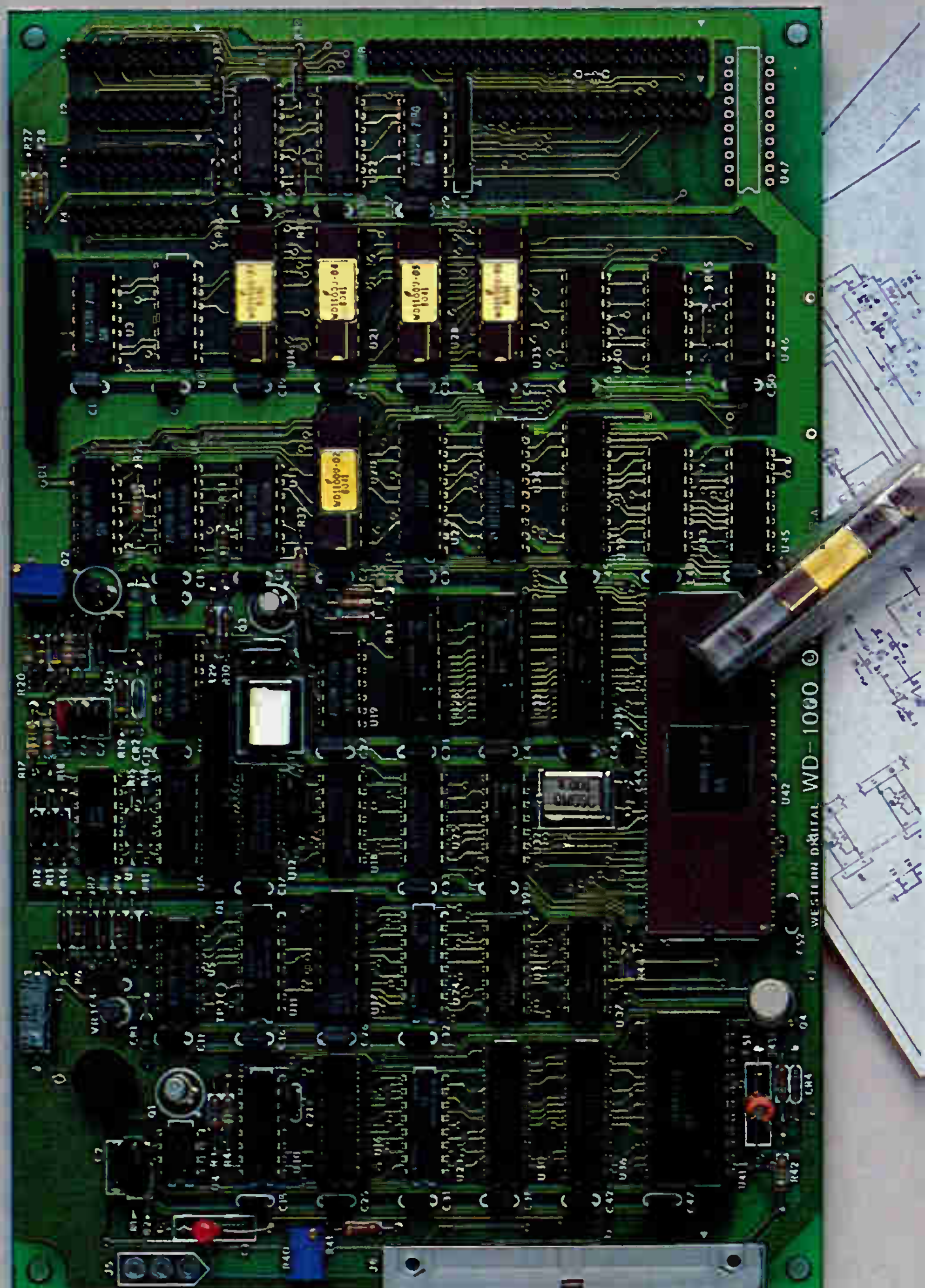

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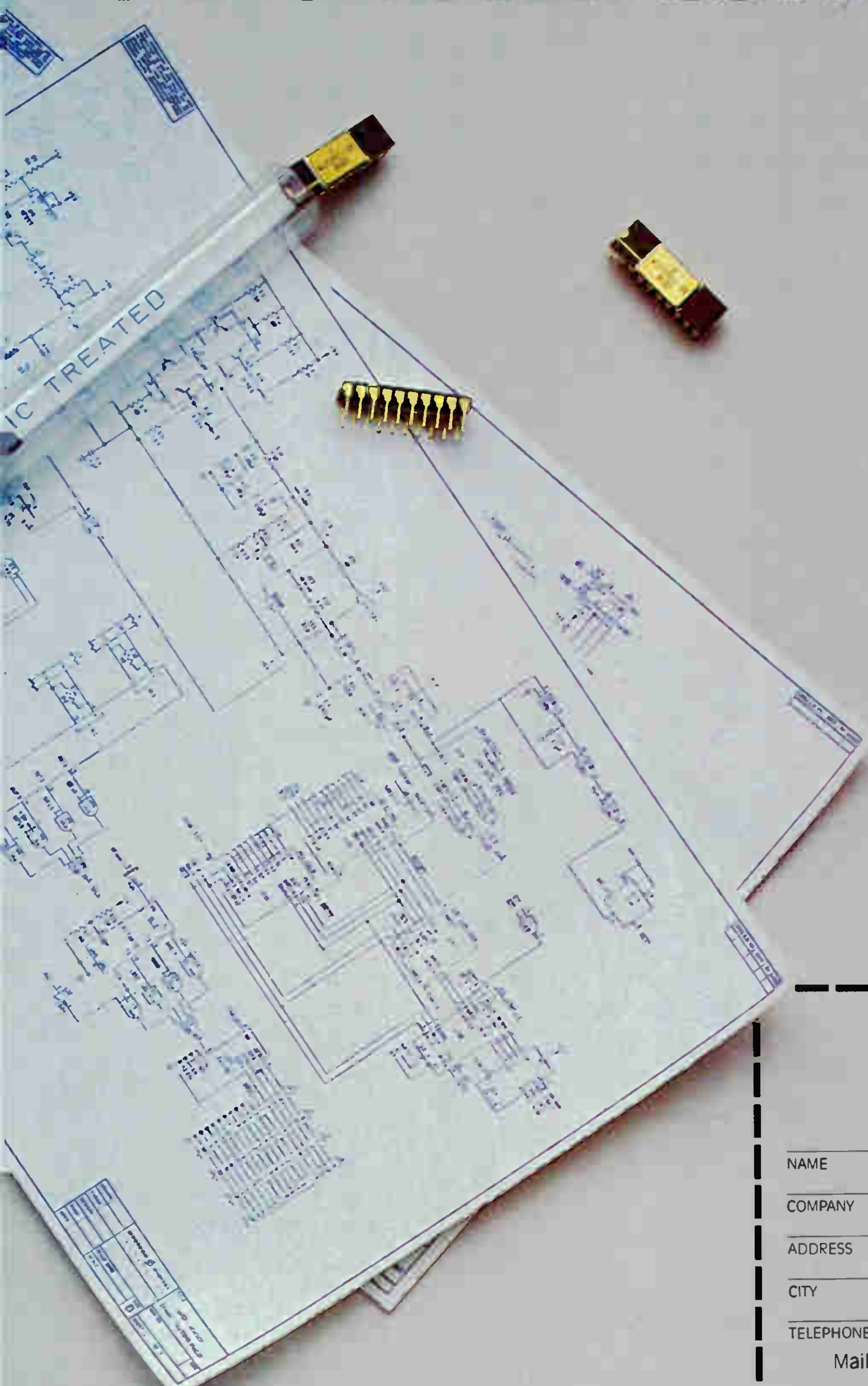

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8-mm market fades to video

Makers of amateur film equipment prepare VCR products as sales of movie cameras and projectors sink

by Robert Neff, Tokyo bureau

As if the market for portable home video cassette recorders were not competitive enough already, a new category of manufacturer is entering the fray. They are camera makers, especially of the 8-millimeter home movie variety, and some of them see video as their only hope for survival.

Beyond that, they want to start positioning themselves now to share in the riches they assume will accrue from the new video cameras with built-in recorders that Japanese consumer electronics companies are developing [*Electronics*, Feb. 24, 1981, p. 80].

Canon Inc. was first out of the starting gate with a quarter-inch, compact video cassette (CVC) system it started marketing April 15 in Japan. Elmo Co. of Nagoya, one of Japan's top 8-mm equipment makers, plans to start making a video camera and the Transvision 600, which shows film on a TV screen, by the end of this year as first steps toward a VCR entry. Fuji Photo Film Co., Eastman Kodak Co., and Chinon Industries Inc. of Nagano, three of Elmo's major 8-mm rivals, are known to be mapping video plans but will reveal no details.

Meanwhile, in Europe, two 8-mm makers, Eumig GmbH of Vienna and the Robert Bosch group of West Germany, this fall will start selling under their own names standard half-inch VCRs and cameras supplied by Victor Co. of Japan. And in July, Asahi Optical Co., maker of Pentax single-lens reflex cameras, will start selling a half-inch portable video system made by Hitachi Ltd. What's more, well-placed industry sources say, is that several major Japanese camera makers are preparing to sell an ultrasmall CVC system supplied from outside.

This new rush into video dramatizes the gradual demise of 8-mm film as a popular visual medium. Sales have been sliding for several years throughout the world, and no one expects a recovery. In Japan, home of major producers, output of 8-mm film cassettes plunged from 1.56 million in 1976 to 898,000 units in 1980. At the same time, camera sales there crashed to 140,000 in 1980, from 300,000 in 1975.

Getting out. Such specialized firms as Elmo have watched their total revenues slip, and the once-powerful Bell & Howell Co. in Chicago bailed out of the 8-mm market entirely in 1979 by selling off its consumer photo products business, which consisted largely of 8-mm cameras and projectors. During the first half of 1979, the firm lost $8 million on sales of $36 million.

Consumers fleeing from 8-mm to video do so mainly for convenience. Video offers instant playback and reusable cassettes, while eliminating the need for a projector, screen, and darkened room. Although the visual clarity is inferior to film's, the sound is far superior. All this has been true for years, but only recently have portable video systems fallen sufficiently in price and size to attract consumers in large numbers.

Speed is paramount. To be sure, video is still more expensive. Canon's video camera alone costs 50% more than a typical 8-mm camera. "But most people want an instant system these days," says Keiji Nagata, a manager at Canon. "If we don't start making video now, the electronics companies will be the ones to monopolize the market."

Not everyone is sanguine about the new entries' chances, however. "I think Kodak could sell a new system, but it won't be easy for others," says a senior video products manager at a major Japanese VCR firm. Nevertheless, firms as strong as Canon can probably carve out a niche in the

New picture. Canon was the first Japanese camera maker to market a video system. Its CVC (compact video cassette) system went on sale on April 15 in Japan for $1,700.

burgeoning worldwide VCR market, which is supplied by 13 makers of half-inch format products—12 Japanese companies plus Philips—and a single quarter-inch maker—Funai Electric Trading Co. of Osaka. Last year, shipments by Japan's VCR makers more than doubled from 1979 figures to 4.4 million recorders and 600,000 cameras, with portable models pacing the growth.

Canon's strategy is to exploit the virtually untapped quarter-inch market with a "shooting only" system supplied at first by outsiders. Funai is supplying Canon's new VR-100 video recorder and 30-minute cassettes; Matsushita Electric Industrial Co. is making the VC-100 color video camera that Canon helped develop and that uses a Canon zoom lens. Nagata says that Canon will start making its own gear "certainly" within two years.

Weighing a combined 4.8 kilograms, Canon's camera and recorder are fully 2 kg lighter than the smallest portable half-inch models. Incompatible with either the Beta or VHS cassette formats, and lacking an optional tuner to allow recording of TV programs, Canon's system is aimed squarely at home movie makers. Its price in Japan of $1,720 compares favorably with $1,845 for Asahi's half-inch Pentax video system, which has just been introduced.

In camera stores. Canon launched its system in 300 domestic outlets, 80% of which are camera shops. By the end of the year it wants to be in 1,000 stores, against 3,000 selling its film cameras. Export plans are not firm yet, but some competitors claim that Canon's entry has been slow to take off. Nagata says reaction has been "pretty good."

With annual sales of only $68 million, Elmo lacks the resources to enter video as aggressively as a Canon, whose sales exceeded $1 billion last year. "It's a very tough field, with so many big companies," says managing director Haruo Teshi at Elmo. "We're too small to succeed unless we have a special technology or equipment." The company hopes to boost production from 1,000 to 3,000 systems this year.

Elmo's initial answer will be a flying-spot scanning system called Transvision that it hopes to start delivering by late this year.

Holding action. Teshi concedes that Transvision is merely a stopgap until Elmo can get a genuine video product off the drawing board. Teshi thinks Elmo can design a lighter, easier-handling video camera with a better viewfinder than is now available, but he acknowledges that the recorders will have to come from outside. Elmo currently is negotiating with potential suppliers. "To sell cameras you need a recorder," Teshi says. "We can only hope for a tiny share of the market, but the total market is huge," he adds.

As yet unanswered is the question of whether camera makers have the marketing resources to sell video. At least one observer is optimistic. "It won't be hard to sell through camera stores," argues a Tokyo securities analyst specializing in video. "The 35-mm camera technology is more sophisticated and electronic now, so sales people should be able to handle video," he says.

Want a vote. The camera makers readily admit that their longer-range target is participation in video industry discussions about the next generation of VCRs. They see single-unit camera-recorders reaching the market in three to five years and want to be identified as video companies in time to help decide what the new generation will be. "Sony Corp., Hitachi, and Matsushita have already proposed different formats and are preparing to start discussions," says Nagata of Canon. At Elmo, Teshi acknowledges that "we are very interested in the single units. If someone invites us, it would be our great pleasure" to enter standardization talks.

Still, the film-camera firms will never likely be in the video driver's seat. For the foreseeable future many will depend on contracts with original-equipment manufacturers or codevelopment deals with electronics companies. And observers believe they will follow the market whenever the new video generation arrives. The well-heeled Canons, Minoltas, and Ricohs can probably make a go of it. Others may not fare so well. □

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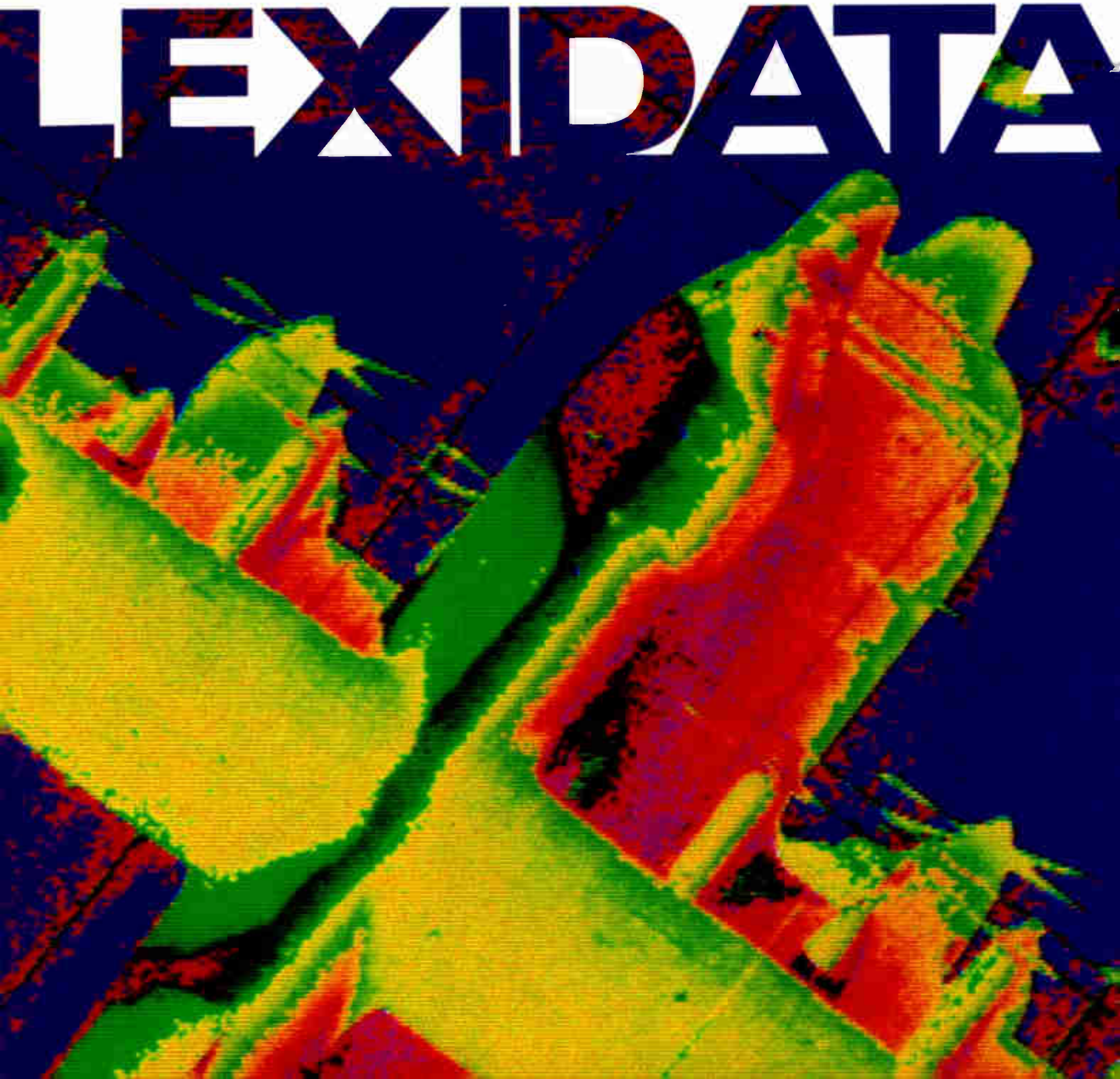


Consumer electronics

Spring conference eyes changing video world

Chicago meeting highlights circuit integration as well as the new role of the TV receiver

by Gil Bassak, Industrial/Consumer Editor

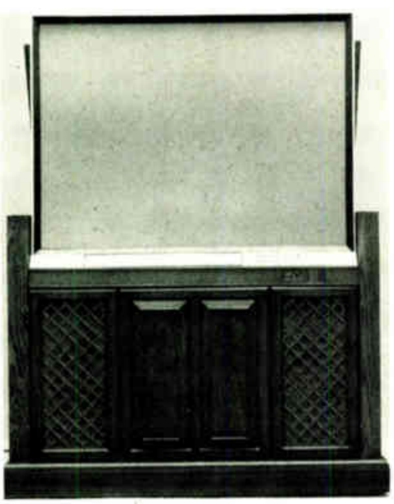
Each year at this time, Chicago is the scene of two concurrent and important electronics events. One, the Electronic Industries Association's Summer Consumer Electronics Show, is a big, sprawling festival that is jammed with marketers celebrating the latest in video, audio, games, and other equipment; it occupies over a half million square feet of exhibit space.

Meanwhile, at a second location, the designers of all that equipment sit down quietly to read and talk

The big picture

Projection color television will take on a new look with the 45-inch-diagonal large-screen unit to be unveiled by Zenith Radio Corp. of Glenview, Ill., at this week's Consumer Electronics Show in Chicago. Known as the SN545P, the $3,750 unit is Zenith's initial projection TV entry. Its innovative feature is a remotely controlled retractable screen (left) that vanishes into a cabinet when not in use (right).

In addition, the system employs a patented projection picture tube technique eliminating the need for frequent manual adjustments necessary on competitive units for proper color convergence. By tilting the face plate panel approximately 7° within the two outer tubes in the three-tube in-line projection system, Zenith engineers say they have developed a self-converging system. This technique eliminates the need for about $50 worth of components typically used by other projection system manufacturers to compensate for image distortion caused by off-axis mounting of color projection tubes. Zenith also maintains that a 25% improvement in picture sharpness is achieved, as well as a peak brightness level that is more than twice that of other single-unit rear-projection systems currently on the market. **Wesley R. Iversen**



about papers that describe the next round of developments in consumer electronics. It is here that one can get a line on what is coming in a market that topped $10 billion last year. This less chaotic show is the Institute of Electrical and Electronics Engineers' Chicago Spring Conference on Consumer Electronics (CSC 81), which is in its 22nd year.

Some of the developments that are disclosed during this meeting reflect overall trends, such as a continuing move toward higher levels of circuit integration. One paper, presented jointly by researchers from Zenith Radio Corp. in Glenview, Ill., and Motorola Inc. in Chicago, describes a virtual television set on a chip as "a new high-performance LSI [large-scale integrated] chip containing all small-signal functions of a monochrome receiver, except sound intermediate frequency."

On a related but smaller and less futuristic scale, state-of-the-art digital phase-locked-loop circuits are the topic of separate papers from Sanyo Electric Co., RCA Corp. in Indianapolis, and Siemens AG in Munich, West Germany. Noteworthy are the tuning techniques Sanyo employs. Its PLL circuit provides discrete tuning control for preset push-button tuning and yields the typical low-tracking error that is associated with such circuits. For auto-search tuning, the same chip uses a voltage synthesizer to perform the tuning function; this gives continuous tuning resolution, covering worldwide frequency allocations.

Look at receiver. The clearest trend in consumer electronics is the heavy emphasis placed on the TV receiver and its elevated stature in the current video revolution. For example, a whole day of CSC 81 is devoted to videotex systems, with no less than 13 papers presented on the subject. This session includes feedback from some of the videotex field trials now under way in the United States, as well as other issues relating to this much discussed field, such as marketing, graphics capability, and parts count reduction. Walter S. Ciciora, director of product and marketing for Zenith's push into cable and satellite TV, as well as videotex, is its chairman.

Ciciora's new post at Zenith was announced in February at the same time that the company revealed plans to establish an organization for the development, manufacture, and marketing of products for cable and subscription television, as well as videotex. Zenith's involvement adds to the growing list of participants in the television industry poised to catch the rising wave of videotex.

Part of the video trend is reflected in changes in display technology. Not surprisingly, a half day will be spent by companies, all of them Japanese, revealing the newest in large-screen and projection TV. However, at the CES, Zenith will unveil its 45-inch TV screen (see "The big picture," p. 93). On the other end of the scale will be Toshiba Ltd.'s description of its pocket-size liquid-crystal-display TV [*Electronics*, May 19, p. 104] and a report on Matsushita Electric Industrial Co.'s work in developing three-dimensional TV.

In the area of nonbroadcast programming material, an ever growing part of the video experience, trends in the video disk player and its older brother, the video cassette recorder, are well represented. One paper, "The Computational Video Disk," presented by Andrew Lippman from the Massachussetts Institute of Technology in Cambridge, describes the potential of the optical video disk player. He cites as an example its use as a self-teaching aid because of its ability "to store digital data along with the pictures on the disk. This transforms the disk into a computation partner permitting simultaneous generation of the controlling program and the visual imagery, where the user may wander freely through densely populated visual surrounds and familiarize himself with an area or procedure."

Here and now. Precursors to this are the currently available disk systems, such as RCA's SelectaVision VideoDisc. Although it is not an interactive system, it does symbolize about 10 years and $150 million of research. Conference goers will have an opportunity to learn about the workings of SelectaVision at one of CSC 81's afternoon sessions, and at a second session they will hear about one of the signal-processing techniques, called buried-subcarrier encoding, that RCA developed in order to bring its player to market.

In this technique, the chrominance subcarrier and its modulation sidebands are placed at a relatively low frequency within the wider-band luminance channel. The approach was developed specifically for RCA's video disk system, but the fundamental principles involved provide unique advantages in other applications with similar requirements, says the company.

What video disks cannot do, however, is record program material. They are play-only machines and that leaves some directions open that are best followed with the VCR. For example, there is mounting competition between VCR companies to produce a portable video replacement for the home movie camera (see p. 89). Technicolor Inc., Los Angeles, has already introduced one that is manufactured by Funai Ltd. in Osaka, Japan.

In the absence of such a standard, other manufacturers have produced compact hand-held VCRs, but only at the prototype level. Two such prototypes will be described at the meeting—the first one, by Hitachi Ltd. in Kyoto, features Hitachi's color solid-state image sensor. The total recording system weighs about 5.7 pounds including zoom lens and battery pack. Recording time is 2 hours. The second unit, developed and described by Sony Corp., weighs 4.4 lb. and uses a special high-energy metal alloy tape for 40 minutes of recording time.

Finally, for those consumers unwilling to spend their time indoors watching television, Motorola Inc.'s Integrated Circuits division in Austin, Texas, has the technological answer. It is a microcomputer that uses a power-saving 8-bit complementary-MOS microprocessor, the MC 146805G2, with 112 bytes of random-access memory and 2-K bytes of read-only memory to form a computer for bicycles. The device provides instantaneous and average speed, odometer reading, and number of revolutions per minute. □

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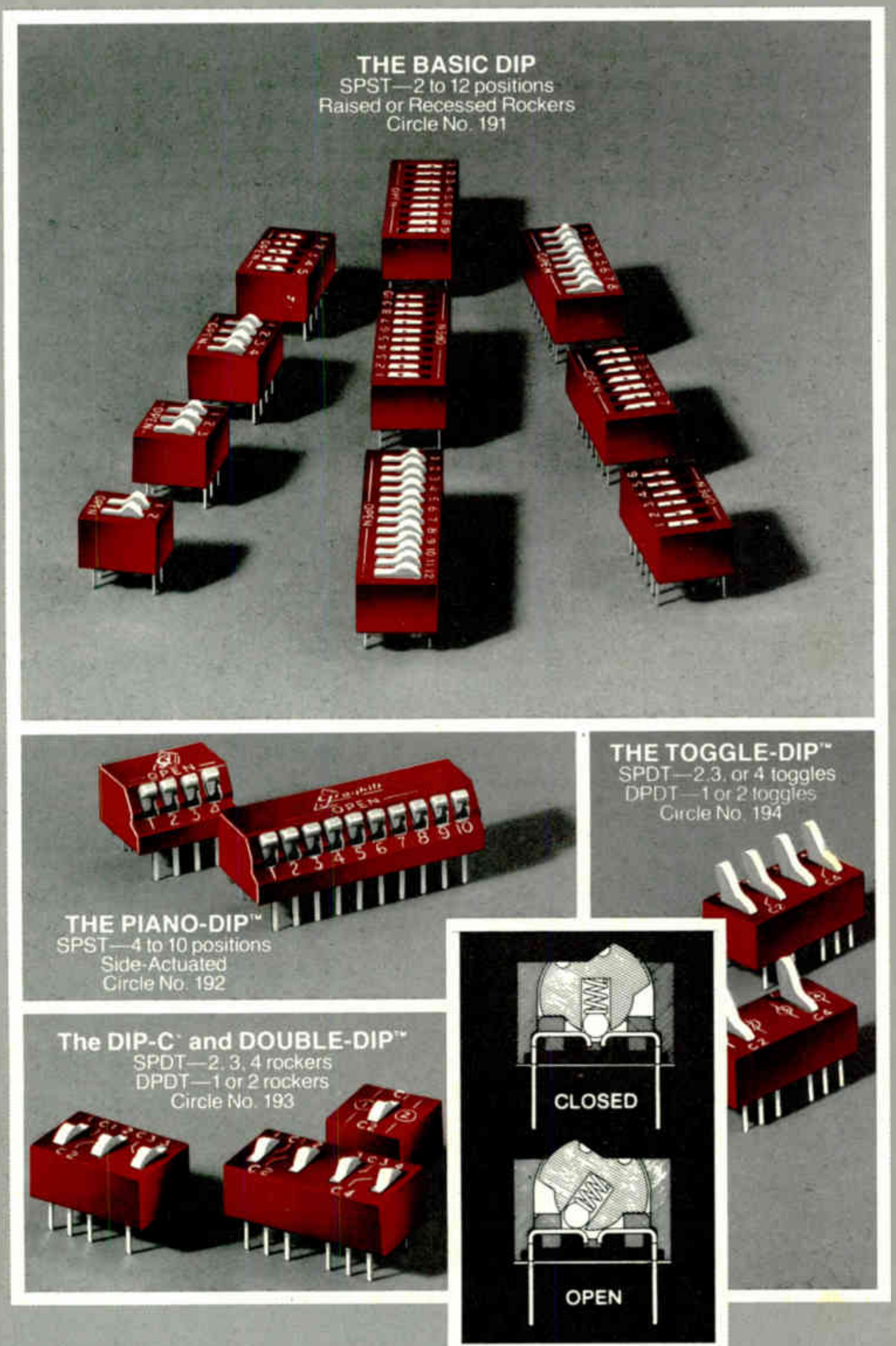

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Computers

McAuto: the good life for computers

Elaborate life-support and backup systems ensure continuous operation of McDonnell Douglas's $133 million in machinery

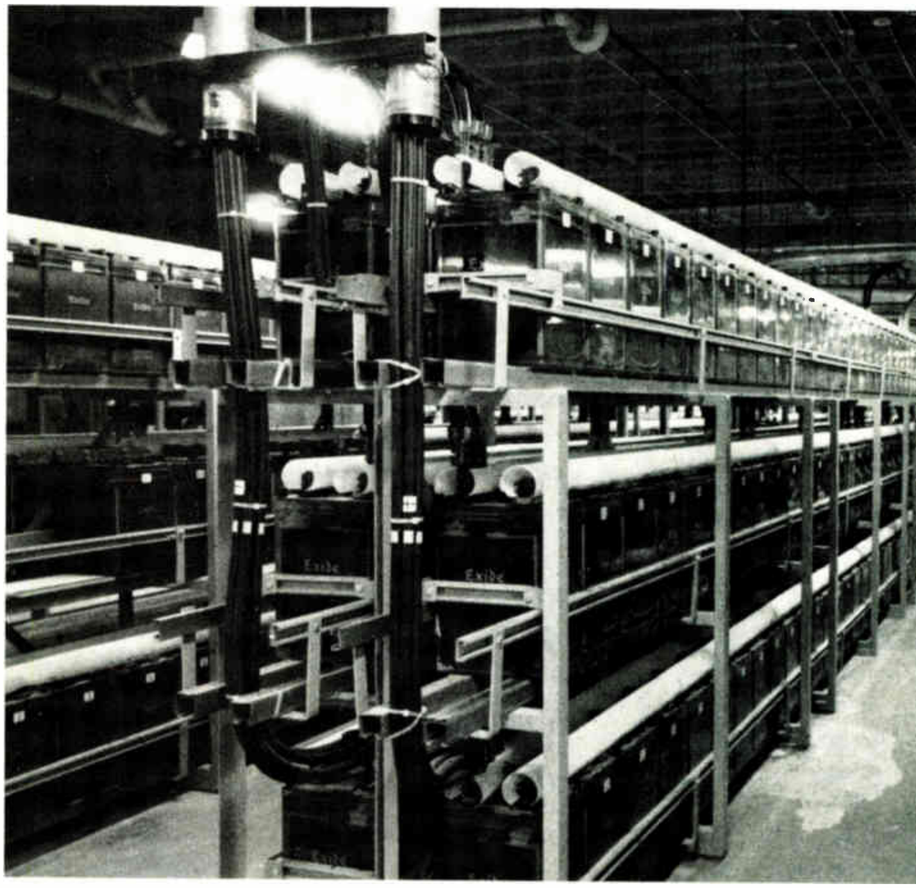
by Tom Manuel, Computers & Peripherals Editor

Large computer systems that must deliver continuous, reliable service need much more care and feeding than desktop or personal models. The big systems require a continuous, voltage-stabilized power supply; heavy-duty cooling; carefully controlled humidity; and, in case of an emergency, a nonconductive fire retardant.

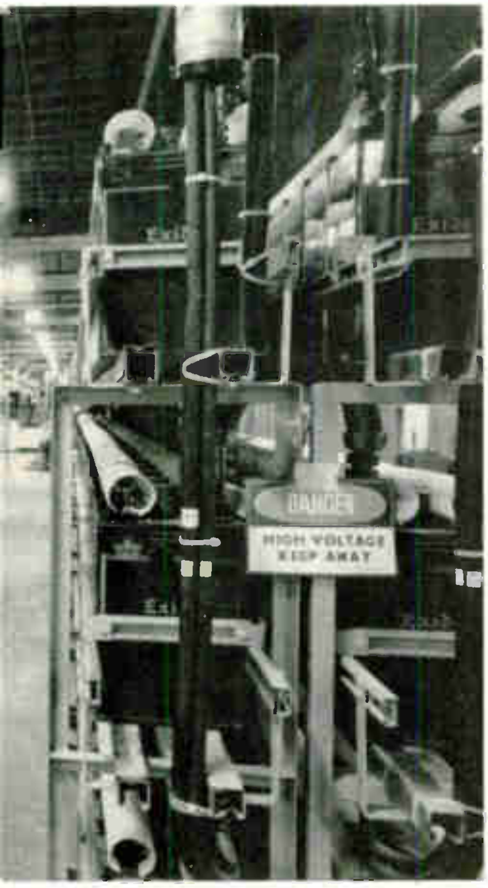
To meet these stringent requirements, McDonnell Douglas Automation Co., which calls itself McAuto, recently moved its computers into a large, futuristic-looking computer center designed from the ground up specifically with the idea of delivering uninterruptible computer service.

A specially designed support facility provides the computers with a continuous supply of the required utilities such as chilled water; cooled, filtered, and humidity-controlled air; voltage-stabilized electrical power; and Halon fire-control gas. And because the support facility is designed as a separate entity, computers can be moved, removed, enlarged, or added without costly and time-consuming changes in the utility service. A vast gallery—a corridor three floors high and extending 450 feet along one side of the computer building—was constructed to deliver these services.

The biggest. The new center at McAuto's headquarters in St. Louis, Mo., houses and supports the world's largest concentration of computer power under one roof, the company says. The close to 4 acres of raised-floor computer space on three levels houses seven IBM 3033 computers, one 3031, four Control Data Corp. Cyber series systems, and a large assortment of peripherals having a



Data shelter. To keep its $133 million worth of computer machinery working, McAuto uses such backup systems as these 2.2-volt batteries (opposite page, top). The computers, which occupy 4 acres of floor space, are centrally monitored (opposite, bottom) and have a tape library containing 130,000 reels (this page, below). But at the heart of the facility in St. Louis are the processors, stretching for seemingly endless rows (above). The company billed $180 million in sales to 3,000 customers last year, plus $240 million to parent McDonnell Douglas.



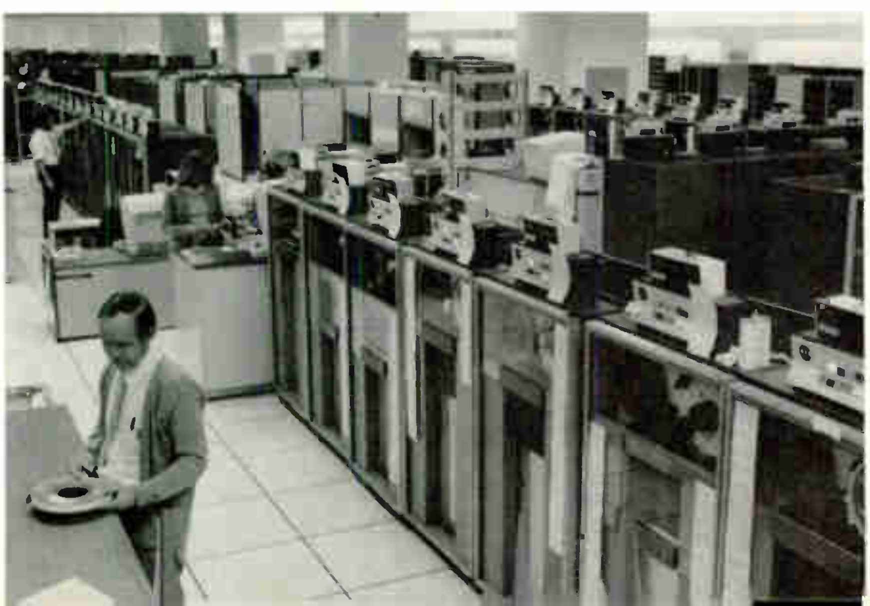
total value of $133 million. The division of McDonnell Douglas Corp. delivers remote computer services to 3,000 commercial customers ($180 million in sales in 1980) and to the parent firm ($240 million.)

In designing the life-support system for the computers, special attention was devoted to ensuring an uninterrupted and stabilized electrical power supply that would eliminate any undesirable effects from brownouts, short service interruptions, or complete outages. The primary power source is a pair of 34,500-volt lines from two different power-generating sources of the local utility.

To clean the power source of voltage and frequency variations, and also to back it up in case of an outage, there is a power-support system that uses 10,020 2.2-v storage battery cells, 30 frequency converters, and 27 solid-state switching units (called reliable power units). This setup converts the incoming ac power into dc and then back into ac, with the storage cells ready to be cut in at the dc stage whenever needed. Switchover is almost instantaneous, and cells can carry all the computers and enough chilled water pumps to keep the center running for about 15 minutes.

Added backup. To back up the main power source for the center's safety equipment and other power needs, there are four generators that automatically start in about 30 seconds. The generators can also handle 25% of the power load for the computers and can be manually switched in when the battery power is about to run out.

An IBM Series/1 computer has been installed as a facilities monitoring system. It watches about 2,000 sensor points in the computer-center support system—six points in each of the reliable power units, all the switches, the motor generators, many temperature points, the ventilation units, and essentially all environmental variables that can affect reliable computer operation. The system's warning and alarm signals are relayed to both computer operations and maintenance personnel. It tells them not only that they have a problem, but also where it is, what is wrong, and in many cases, how to correct it. The system was designed and built by McDonnell Douglas. □



Letter from San Diego

Homes costs curb growth

Many believe the growth rate is being stunted by the refusal of executives to brave the area's high real estate prices

by Terry Costlow, Costa Mesa bureau

The warning signs are there: the four-year upcurve that San Diego's electronics community has been riding may be under attack by the California blight that has bedeviled the electronics industries in the rest of the state. Silicon Valley South, for all its balmy oceanside location, is finding that high housing costs and a shortage of middle management are stymieing expansion.

The jury is still out on whether regional growth has reached its peak. Opinion is divided roughly between newcomers and longtime residents. Those who work for start-ups or divisions of larger companies that have recently moved to the San Diego area maintain that the rapid growth rate will continue. But many of the established firms see housing problems as the stumbling block to continued rapid growth.

"There's not a lot of continued growth in San Diego. We're considering capping our growth in California," says Larry Hemmerich, marketing vice president of Cipher Data Products Corp., a San Diego firm since 1968.

San Diego's problems are not unique or new. Companies in both northern California and Orange County (just north of San Diego) have already begun to expand out of state, where they can afford to import executives. The cost of a house in San Diego has risen to a current average of $126,800, up from $110,000 in 1979 and $85,000 in 1978. Recent Government Consumer Price Index figures, which placed San Diego's 13.5% inflation rate second highest in the country, show that housing took 57% of the average family's income, 11.5% higher than the national average.

A recent survey by the Economic Development Corp., the organization largely responsible for attracting new companies to San Diego County, found 60.9% of the electronics firms saying that the supply of professional and technical or skilled personnel is less than adequate.

"I see the beginning [of a saturation problem] now unless there's a significant break in one of the factors—a drop in interest rates, rising real estate prices elsewhere, or the introduction of significant new housing here," says George Murphy, director of employee relations at Cubic Corp., a firm that has been based in San Diego for 31 years.

Recent employment figures show a flattening is already occurring. According to figures for March 1981 from state's Employment Development Department, the total number of persons employed in the manufacture of office machinery, electrical equipment, and instruments, categories used to make up the electronics industries, has increased by only 3% to 36,900 over March of last year. In contrast, the growth for the 1980 period was up 17% from 1979, and the increase from 1978 to 1979 was 18%.

Growth to go on. Nevertheless, despite these darkening prospects, no one expects growth in the area to halt. San Diego's small town charm and big city attractions are drawing cards that are hard to beat. These features, along with a salubrious climate and the availability of unskilled labor, drew divisions of TRW, Northern Telecom, and TRW-Fujitsu last year alone. Other major companies such as Hewlett-Packard, NCR, Fujitsu Microelectronics, Oak Industries, Burroughs, and National Semiconductor have divisions throughout the area.

The plentiful supply of unskilled personnel is in contrast to the shortage of management. Because of it, San Diego's electronics community has not had to tap the supply of cheap Mexican labor only a few miles away.

Another effect of the sheer quantity of the electronics companies in San Diego is increased confidence of investors, leading to interest by potential entrepreneurs, says Dan Yoder Sr., marketing vice president at Applied Micro Circuits Corp., a young San Diego company. "Venture capitalists now look at San Diego as a good risk. Years ago that was not the case," he says.

The smaller firms that have been in business only a few years generally maintain that they do not have much difficulty in attracting employees for management. Locals at larger firms like the family atmosphere and opportunity, and people from elsewhere often say the potential of joining a firm at the bottom of its growth curve is worth the cost of living in San Diego. □

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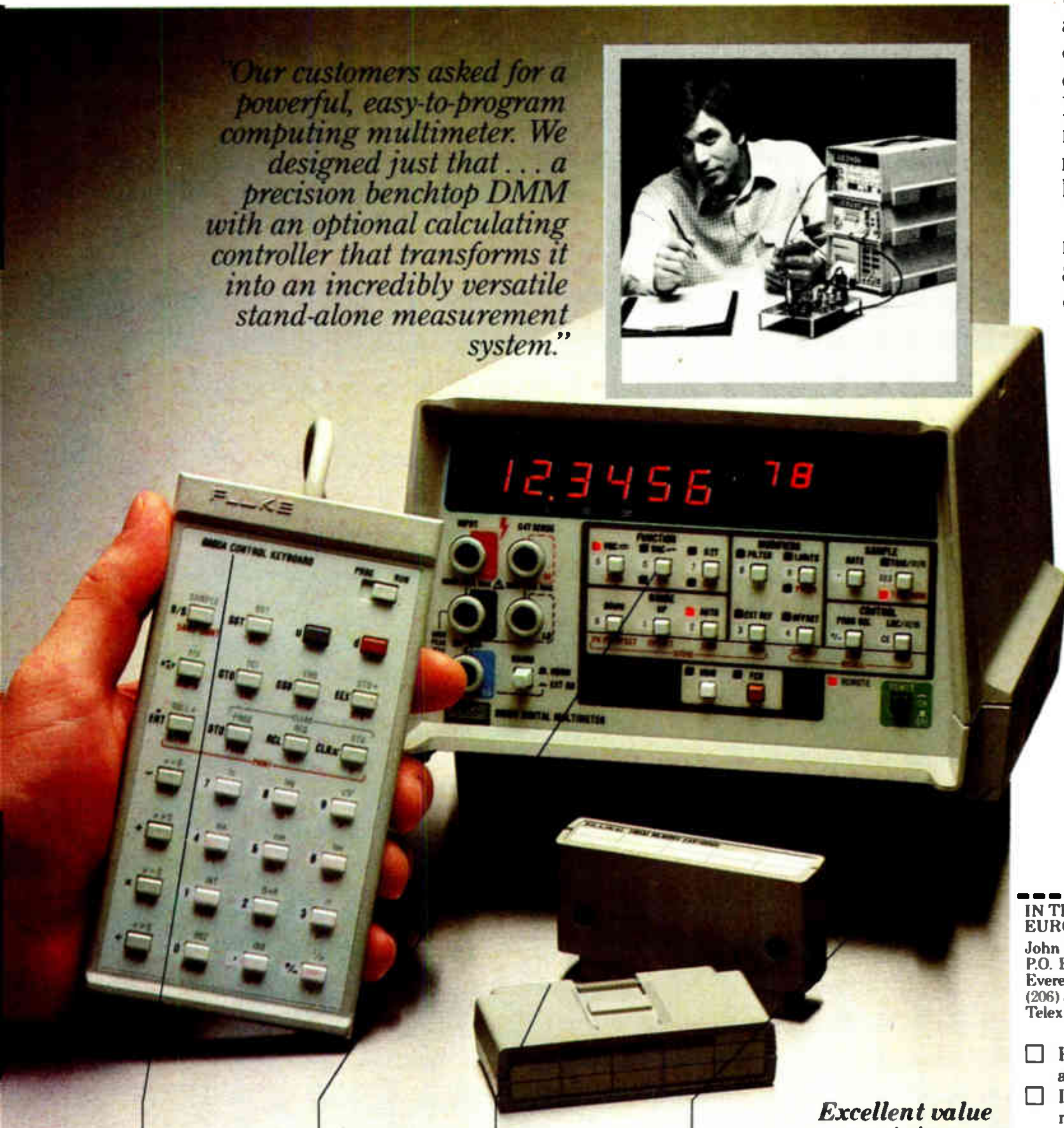

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For technical data circle no. 101

Business

Trade gap with Japan widens

New Commerce Department figures show increased imbalance in six of eight electronics areas as U. S. computer lead shrinks

by Harvey J. Hindin, Communications & Microwave Editor

With the Japanese apparently agreeing to cut tariffs on semiconductor imports, and Nippon Telegraph & Telephone Public Corp. inviting foreign suppliers for the first time to qualify as vendors, it would be easy to believe that Japan is experiencing a second coming of Commodore Perry.

But before U. S. electronics manufacturers permit themselves to jump to that conclusion, a study of the chart on this page should provide a chilling splash of reality. Simply stated, with imports from Japan in electronic goods exceeding exports by almost $4 billion, the U. S. has a long way to go.

The chart, made available to *Electronics* by a U. S. Department of Commerce source, includes final 1980 figures previously unpublished. Those numbers underscore the continuing trend toward greater Japanese electronics exports to the U. S.

True, not only is there movement toward equalizing tariffs [*Electronics*, May 19, p. 42] as well three-day road shows on each coast by NTT [*Electronics*, May 5, p. 110], but now

U.S. TRADE WITH JAPAN IN ELECTRONIC-BASED PRODUCTS, 1975–1980
(millions of current dollars)

	1975	1976	1977	1978	1979	1980
Telephone and telegraph equipment	5.6	5.1	4.4	6.3	8.1	6.6
	25.6	31.1	44.9	92.9	105.6	163.3
Electronic systems and equipment (commercial, military, and industrial)	52.8	51.1	51.6	49.2	66.4	76.9
	111.2	193.7	781.5	391.1	350.4	438.6
Electronic components	109.1	141.9	133.0	172.3	253.4	238.2
	161.2	257.7	371.5	502.0	698.6	830.0
Consumer electronics	22.1	28.4	25.2	37.2	55.4	61.6
	1,251.5	2,578.0	2,047.7	2,757.7	2,350.7	2,337.1
Electronic computing equipment	189.3	239.5	279.5	331.1	441.1	607.3
	32.3	41.7	57.9	187.2	195.7	189.3
Calculating and accounting machines	9.4	7.8	12.3	19.2	18.5	22.2
	180.1	229.4	240.0	333.8	300.3	373.3
Typewriters and office machines	4.4	9.9	12.4	13.6	19.7	25.5
	100.1	162.8	203.0	190.0	226.9	256.6
Photocopying machines	4.6	6.5	14.6	13.9	16.1	17.7
	70.2	105.4	163.9	290.3	307.9	424.0
Totals	397.2	490.2	532.9	642.7	878.7	1,056.0
	1,903.1	3,599.9	3,910.6	4,745.1	4,536.1	5,012.2
Trade balance	−1,505.9	−3,109.7	−3,377.7	−4,102.4	−3,657.4	−3,956.2

Note: The tinted figures are imports; the others are exports.

SOURCE: U.S. DEPARTMENT OF COMMERCE, BUREAU OF INDUSTRIAL ECONOMICS

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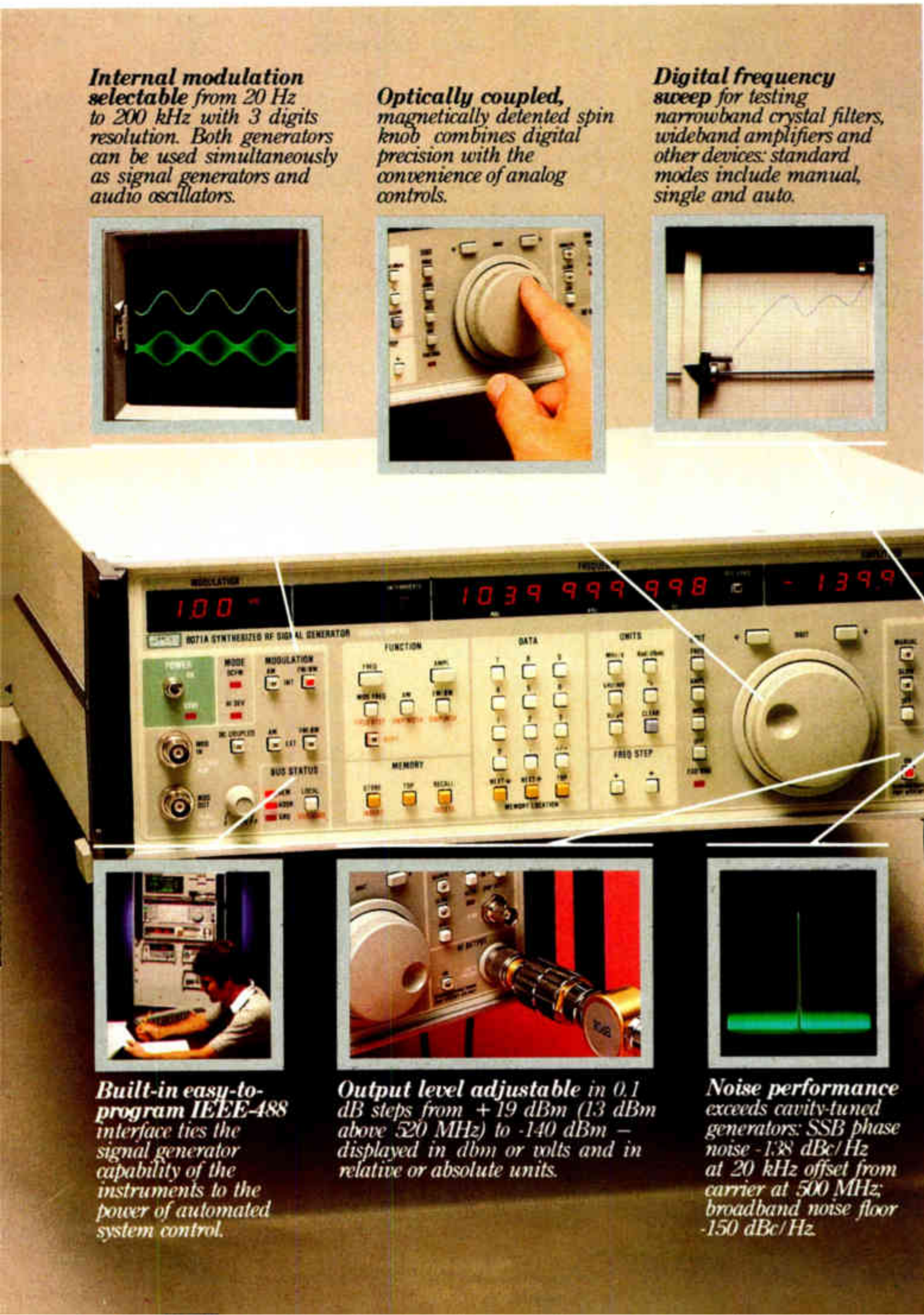

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For technical data circle no. 103

the Department of Commerce is sponsoring a five-day meeting on NTT procurement to be held in Tokyo the week of June 21. Some progress is being made, but with the 1980 balance-of-trade deficit for the U. S. in telephone and telegraph equipment amounting to $157.7 million, it is obvious that it will take many meetings and invitations to reverse the figures.

The picture is even worse in consumer electronics. There, some $2.3 billion flowed toward Japan in 1980. Though the imbalance was the lowest in several years, the small reduction will not materially affect the overall trend.

Computer lead lower. As William J. Sullivan points out, "Only in computers is the U. S. showing a favorable balance. And even this figure has decreased in the last five years from a 6:1 to a 3:1 ratio." Sullivan, a Commerce Department electronics industries analyst, was one of those who helped arrange the NTT mission to the U. S. However, there are plans in Japan to mount an effort designed to capture more of the computer market, notwithstanding predictions that the Japanese will stumble in providing software and service.

Whether the telephone and telegraph situation can be turned around depends on the success of the efforts with NTT. As far as components in general, and semiconductors in paticular, are concerned the pacing factors are quality and reliability [*Electronics*, May 19, p. 125], price and performance. Japanese excellence in those areas permitted its manufacturers to capture 40% of the world market for 16-K random-access memories last year. On the bright side is the recent agreement in principle between Japan and the U. S. to lower semiconductor tariffs: Japan would cut its rate from 10.1% to 4.2%, the U.S. from 5.6% to 4.2%.

All in all, in the eight sectors charted by the Government, the 1980 gap was wider than that of 1979 in six, and narrower in only two. The total 1980 trade imbalance was the second widest in six years, exceeded only by that of 1978. □

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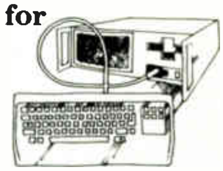

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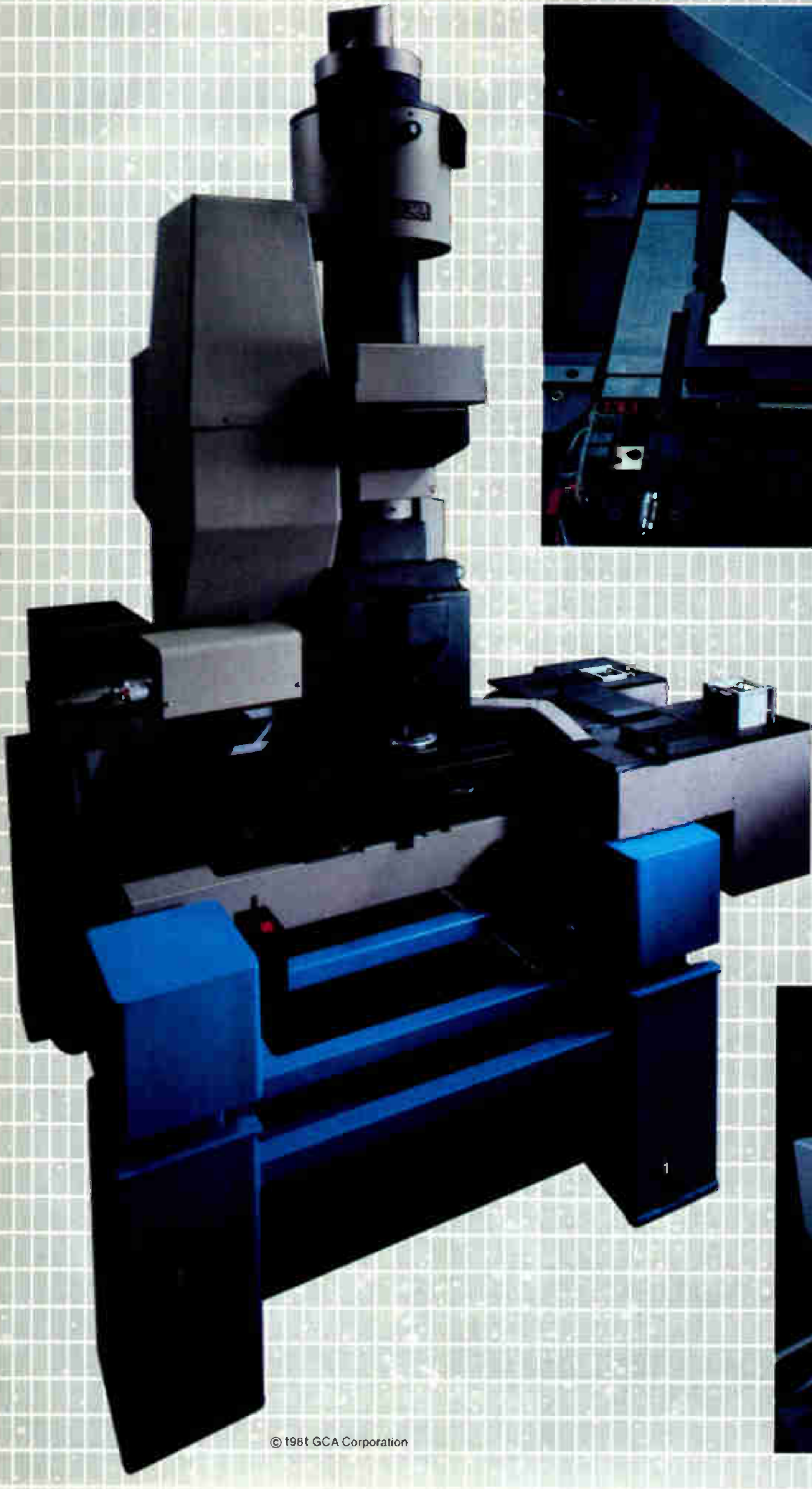

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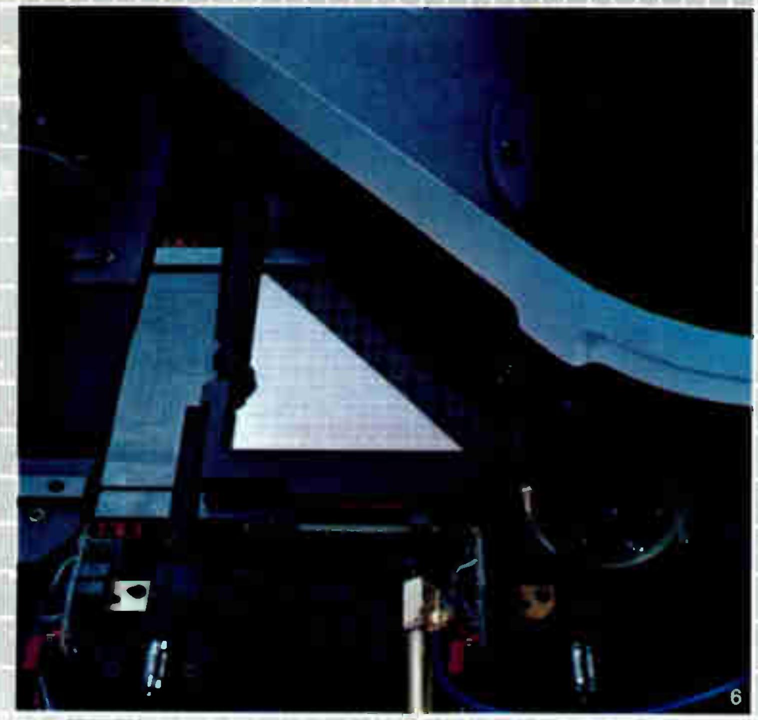

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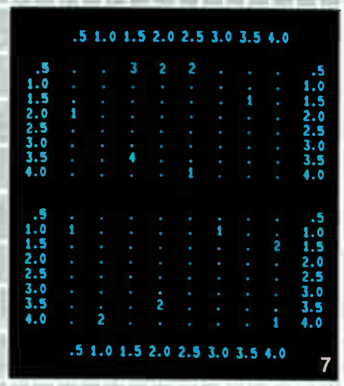
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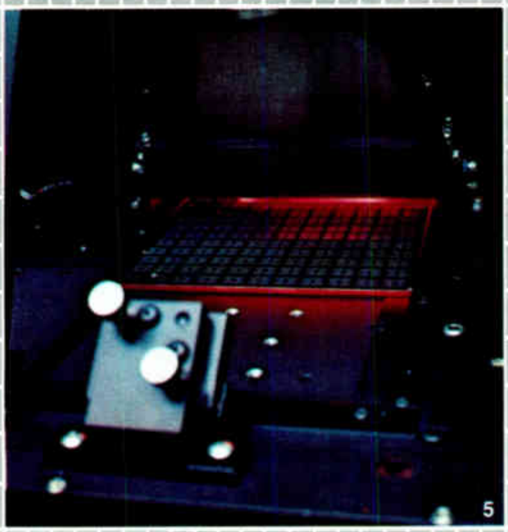

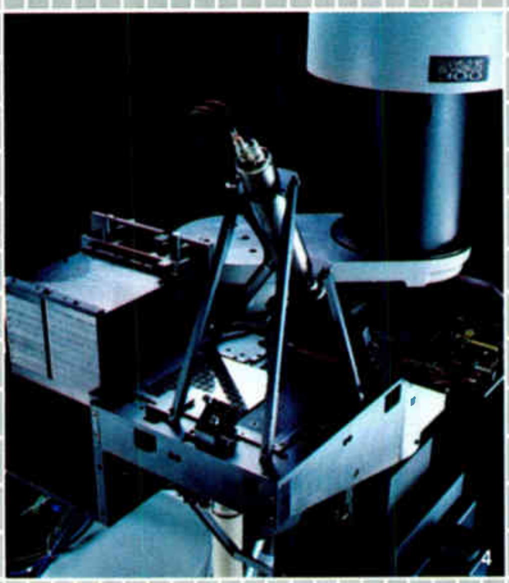

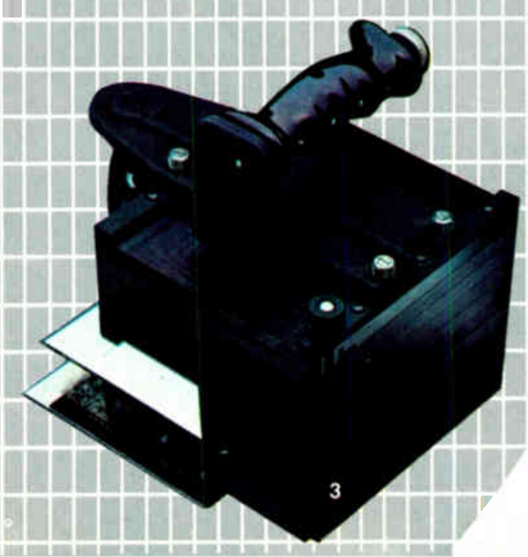

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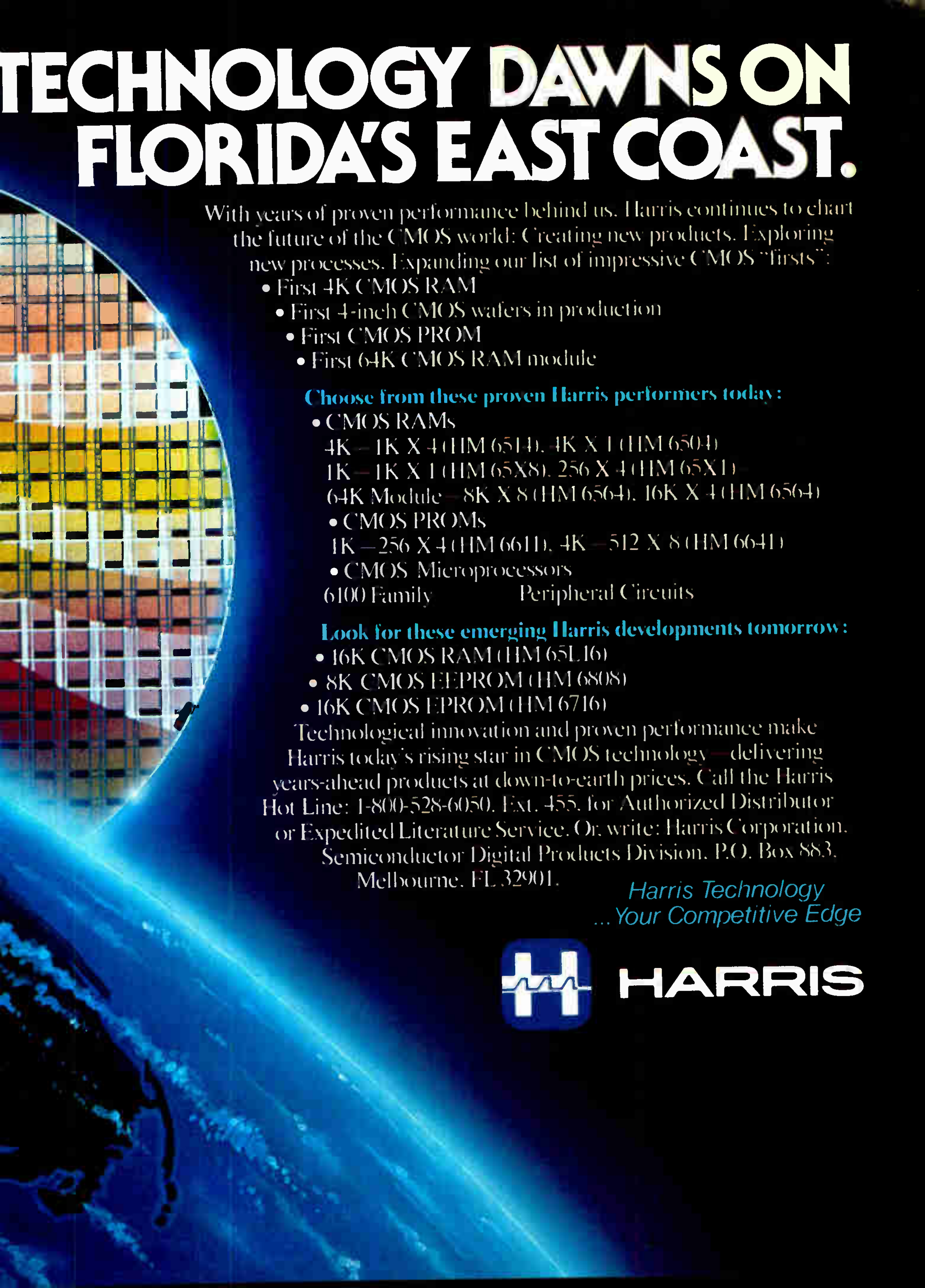
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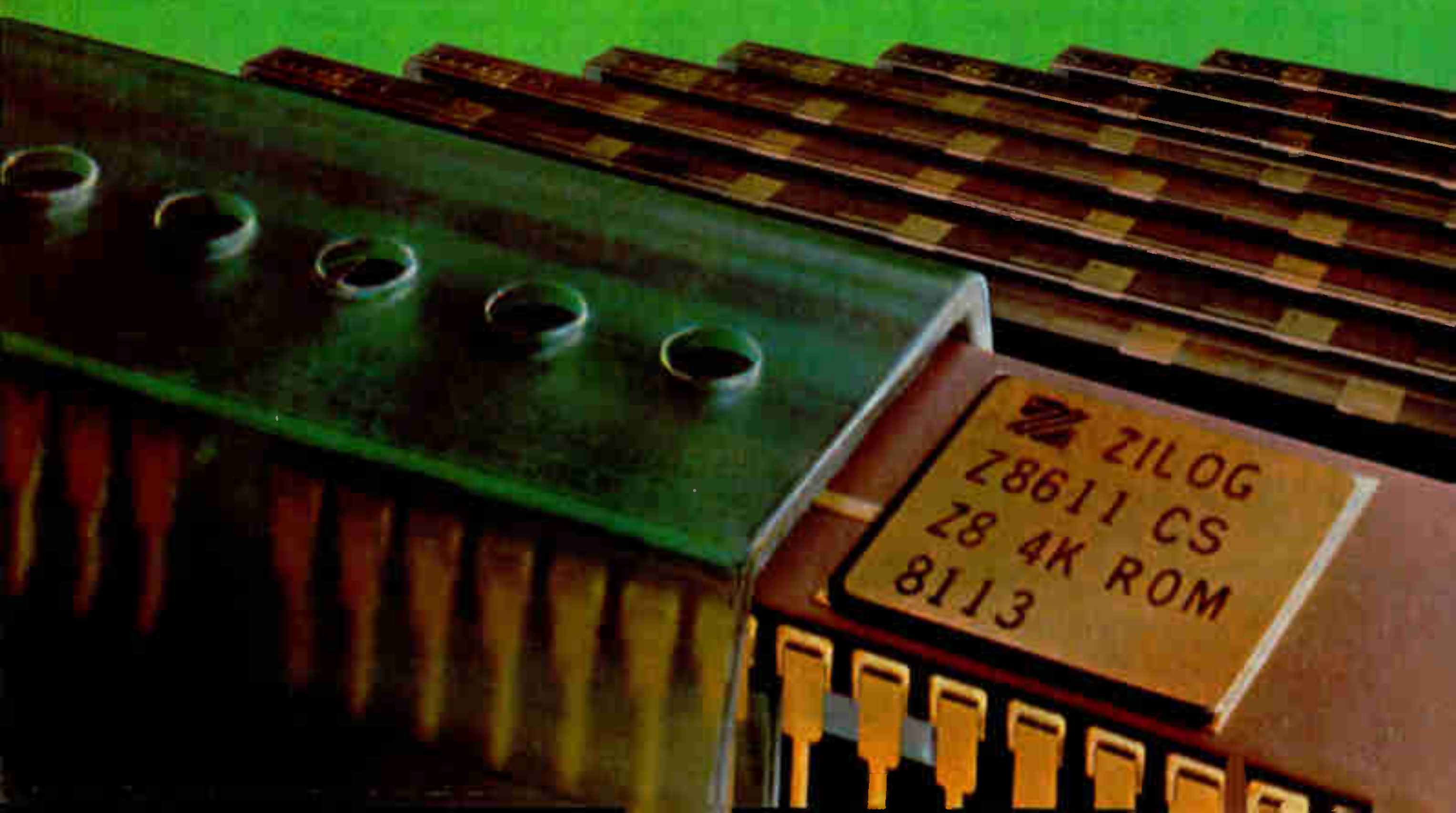
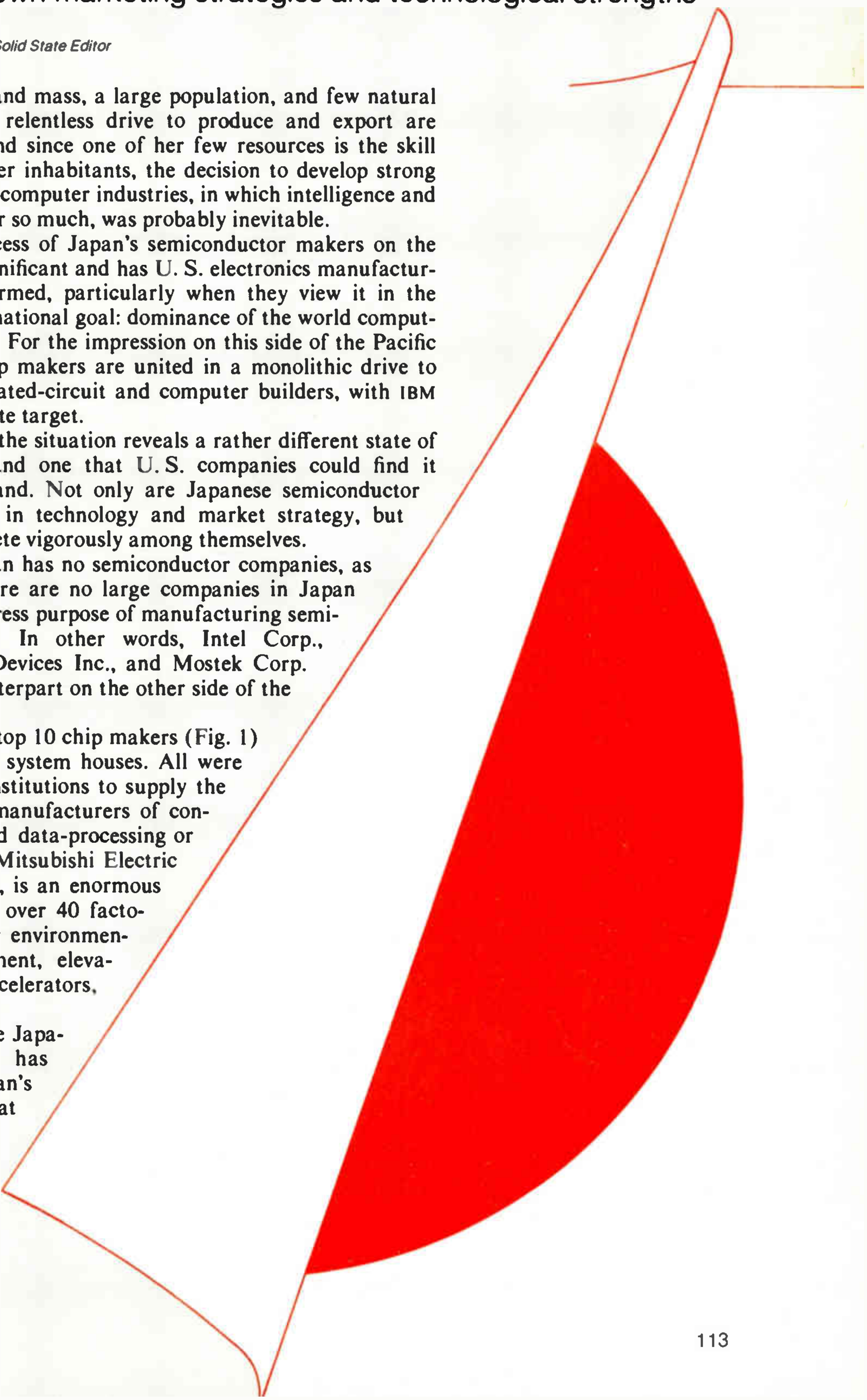


SPECIAL REPORT

HOW JAPAN'S CHIP MAKERS LINE UP TO COMPETE

Beneath the facade of Japan Inc. lie individual companies, each with its own marketing strategies and technological strengths

by John G. Posa, *Solid State Editor*



☐ Given a small land mass, a large population, and few natural resources, Japan's relentless drive to produce and export are understandable. And since one of her few resources is the skill and ingenuity of her inhabitants, the decision to develop strong semiconductor and computer industries, in which intelligence and dedication count for so much, was probably inevitable.

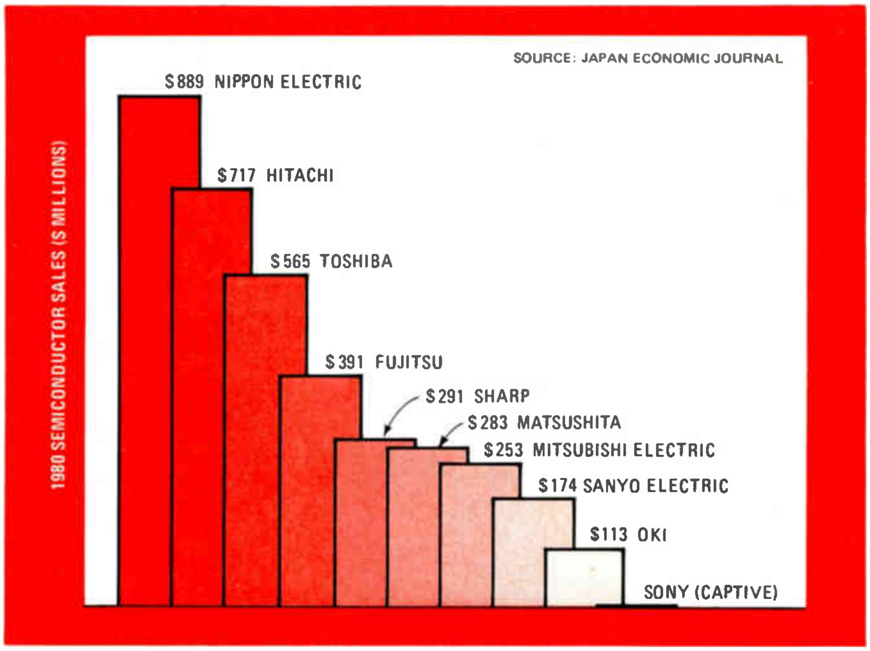
By now the success of Japan's semiconductor makers on the world market is significant and has U. S. electronics manufacturers thoroughly alarmed, particularly when they view it in the light of her stated national goal: dominance of the world computer market by 1985. For the impression on this side of the Pacific is that Japan's chip makers are united in a monolithic drive to topple U. S. integrated-circuit and computer builders, with IBM Corp. as the ultimate target.

A closer view of the situation reveals a rather different state of affairs, however, and one that U. S. companies could find it helpful to understand. Not only are Japanese semiconductor makers distinctive in technology and market strategy, but further, they compete vigorously among themselves.

The fact is, Japan has no semiconductor companies, as such. At least, there are no large companies in Japan formed for the express purpose of manufacturing semiconductor devices. In other words, Intel Corp., Advanced Micro Devices Inc., and Mostek Corp. have no exact counterpart on the other side of the Pacific.

Rather, Japan's top 10 chip makers (Fig. 1) are all divisions of system houses. All were begun as service institutions to supply the internal needs of manufacturers of consumer products and data-processing or heavy equipment. Mitsubishi Electric Corp., for instance, is an enormous conglomerate with over 40 factories responsible for environmental control equipment, elevators, and linear accelerators, in addition to ICs.

It is true that the Japanese government has tried to unify Japan's IC makers, but that effort has not been as successful as generally believed. In the mid-1960s, Japan's Ministry of



1. Individual efforts. This is the way Japan's semiconductor makers line up, but their parent companies cannot be put in the same order. Hitachi is the largest, followed by Matsushita and Toshiba.

International Trade and Industry initiated a multiphase project to win control of the world market for computers. This activity, since dubbed Japan Inc., has, over the years, funded research for development of superhigh-performance computers, systems for processing pattern information, new computer architectures, and very large-scale integration.

Recently, recognizing that its software skills lag behind those of, say, the U. S., it has started a software and peripherals effort. In addition, some observers believe that the Japanese government is preparing to launch a drive to develop the most advanced Josephson junction circuits yet (see "A quick guide to Japan's fastest ICs," p. 118).

MITI has allotted at least $500 million to its nationalized computer effort, but some observers believe that Japan's total investment is much greater—that the individual companies involved have matched the government subsidies many times over, bringing the sum closer to about $4 billion.

During the recently concluded VLSI development phase, these monies were channeled from MITI through Japan's Industrial Science and Technology Agency to the VLSI Technology Research Association and thence to the VLSI Cooperative Laboratory, where the very best engineers from the top chip makers—NEC, Hitachi, Toshiba, and Fujitsu—were to marshal their resources to build a monolithic megabit random-access memory and advanced electron-beam production equipment.

The governmental coordination of the effort was only moderately successful, however, because, just like IC makers in the U. S., Japanese chip houses are competitive. Indeed, the consumer electronics builders vie with one another ferociously because their success hinges on being first to the market, and being first in turn usually hinges on a chip or chip set. For that reason, it is widely believed that the companies involved sent not their top but only their second-best people.

At any rate, the main result of the overall program was a 512-K RAM only partially functional, plus some undoubtedly sophisticated electron-beam lithography equipment. However, the Japanese people in general and IC makers in particular are united in subtler but stronger ways not to be found in other cultures (see "A culture that promotes semiconductor technology," p. 116).

Chips from the computer makers

Fujitsu, Hitachi, and Nippon Electric are the companies principally concerned with computers and communications. Other companies, like Mitsubishi, Toshiba, Matsushita, Sharp, Sanyo, Sony, and Oki are more dedicated to consumer products. According to Kiichiro Yamagishi, a deputy director for MITI, the former group is "strong in memories and microcomputers, and the others are best in linear bipolar technology for calculators and watches."

Yamagishi adds that the big computer companies are also strongest in VLSI. Meanwhile, he says, a good number of the consumer electronics companies are shifting their focus away from bipolar toward n-channel and

NTT has no manufacturing arm, so one aim of its Musashino lab is to conduct basic research to educate potential component suppliers.

complementary-MOS processes and are thus "drifting in the direction of NEC, Hitachi, and Fujitsu." This tendency is strongest at Toshiba, Mitsubishi, Oki, and Matsushita, in that order.

All Japanese electrical equipment suppliers produce ICs for internal consumption, says the MITI official, but some have yet to emerge as component vendors. Such companies include Sieko, Yamaha, and Denso (which supplies Toyota with electrical equipment). Finally, Ricoh, the Victor Co. of Japan (JVC), and Pioneer are just getting started producing ICs of any kind.

In terms of pure technology, a fountain of knowledge is the Musashino Electrical Communication Laboratory of the Nippon Telegraph & Telephone Public Corp. Actually, only 2,000 of the laboratory's 3,000 employees work out of Musashino, a distant suburb of Tokyo. The rest are divided between two other locations. In addition, a fourth branch of the lab, focusing specifically on the latest in semiconductor technology, is being built.

NTT has no manufacturing arm, so part of the lab's charter is to conduct basic research and publish papers on its findings to educate outside vendors. This accounts for the abundance of technical papers delivered by the lab's researchers at device meetings and circuit symposiums held in the U. S. and elsewhere.

The lab's counterpart in the U. S. is Bell Laboratories, only without manufacturer Western Electric Co. Both necessarily conduct research into high-speed communications, digital switching, signal processing, pattern recognition, and speech input and output. Consequently, both have designed MOS RAMs, C-MOS codecs (encoder-decoders), high-voltage cross-point switch arrays, and high-speed microprocessors.

Some specific ICs recently developed by Musashino include a 256-K RAM featuring molybdenum-silicon gates and redundancy [*Electronics*, Feb. 14, 1980, p. 140], a 14-bit digital-to-analog converter trimmed with pulses of current [*Electronics*, July 31, 1980, p. 68], and two speech synthesis chips, one based on partial autocorrelation coefficient (Parcor) theory and the other on line-spectrum pairs (LSP) [*Electronics*, Feb. 10, 1981, p. 78].

Once a circuit has been developed, an outside manufacturer may see the design as fitting well with its own abilities and intentions and if so, may work out a deal with the Musashino lab to produce the part. When it comes to memories, "NEC, Hitachi, and Fujitsu make the practical devices," says Mamoru Kondo, deputy director of the lab's large-scale integrated memory development division.

Indeed, right now it is collaborating with Nippon Electric Co. and Fujitsu Ltd. on a 55-to-70-nanosecond static RAM. Though either manufacturer may spin off a standard component from the effort, NTT's version will incorporate special peripheral circuits that will facilitate its use in electronic switching applications.

Of course, the lab has deals going with companies other than the big computer makers. It developed an optically coupled cross-point array together with Oki, and Matsushita and others have elected to implement a Parcor synthesizer in silicon. So far, Fujitsu says it will construct an LSP synthesizer chip. JEOL Ltd. (formerly known as the Japan Electro-Optical Laboratory) built the electron-beam machine used to expose the Musashino lab's 256-K RAM. The machine, which uses a beam with a variable shape to expose patterns directly on the wafer, may one day come to market.

To keep NTT's communications system up to date, the Musashino lab must constantly push the state of the art in MOS and bipolar processing and develop and test out sophisticated computer-aided design (CAD) tools. To improve the speed of MOS circuits, it has recently developed two methods of dielectrically isolating a chip's active elements and thus removing the retarding effects of unwanted parasitics (Table 1). The schemes are called Simox, for separation by implanted oxygen [*Electronics*, Nov. 20, 1980, p. 136], and Fipos, for full isolation by porous oxidized silicon [*Electronics*, Jan. 27, 1981, p. 77].

With Simox processing, oxygen ions are shot so deeply into the silicon that the oxide layer is formed beneath the channel regions. With Fipos, an electrochemical process converts the p-doped silicon surrounding n-type wells into porous material. The wafer is then placed in an electrified acid bath and the porous silicon swiftly oxidizes from top to bottom, creating dielectrically isolated islands for transistor formation. The lab has used Simox to build 95-picosecond, 1-micrometer–buried-channel field-effect transistors and will use Fipos to construct a 4- or 16-K C-MOS static RAM for test purposes.

Still, Makoto Watanabe, director of Musashino's integrated electronics development division, believes bipolar technology will win out over MOS in the long run so far as speed is concerned. Using identical design rules, "bipolar technology is five times faster," he says, adding that "with it you can achieve 150 to 200 ps at the system level, compared with just under 1 ns with MOS." Also, even though the lab cooled down its own gallium arsenide ring-oscillator circuits and got 17-ps delays, "bipolar [silicon] is still more promising than gallium arsenide for VLSI work," Watanabe submits.

To increase the speed of bipolar devices, the lab uses what it calls super–self-alignment—with impressive results. When used to make an emitter-coupled-logic RAM, it produced a 1-K chip having an access time of less than 3 ns. Most recently, when super–self-alignment was applied to a Schottky TTL chip, the process yielded a

32-bit microprocessor that contains 12,000 three-input gates whose elements can be elongated to accommodate the automatic placement and interconnection of the logic functions [*Electronics*, April 21, 1981, p. 103].

The circuit illustrates the effectiveness of its CAD system. To judge by the photograph (Fig. 4), the device uses polycells: logical functions that are pulled from a library and wired to power and signal buses organized in channels. Some of Bell Labs' CAD-built chips, like its echo canceler [*Electronics*, Feb. 14, 1980, p. 144] and its new C-MOS microcomputer [*Electronics*, March 10, 1981, p. 98], bear a strong physical resemblance to Musashino's VLSI processor unit.

Computer makers

Given the competition for world markets, it is no surprise that the computer makers are at present emphasizing high-density dynamic RAMs, high-speed static RAMs, and gate arrays. In addition, for the next genera-

2. Two camps. According to Kiichiro Yamagishi, a deputy director at Japan's Ministry of International Trade and Industry, computer companies like Fijitsu "are strong in memories and microcomputers, and the others are best in bipolar linear technology."

A culture that promotes semiconductor technology

Japan's small land mass may have something to do with its incessant miniaturization. The Japanese were exposed to overpopulation sooner than much of the world, and it learned to "think small" before the United States did. Its cars sold well basically because they were made smaller sooner; many of its new audio and video products are selling in bigger numbers today because their smaller dimensions are appealing to a wider audience.

Indeed, the skyrocketing electronics content of consumer and industrial equipment may have strengthened the drive to very large-scale integration by Japan's chip makers—each catering to a much larger parent corporation—to keep up the downsizing. In fact, although major U. S. semiconductor firms are experiencing downturns so far this year, Japan's semiconductor sales are up, aiming for an expected 1981 growth of at least 16% [*Electronics*, Jan. 13, 1981, p. 139]. Moreover, this increase comes despite the fact that the nation's executives share a general outlook that stresses longer-term growth over immediate gains.

Also cited as reasons for Japan's successes in automotive, audio, and video markets are a government that is apparently more friendly to big business and a devoted and determined work force. However, with semiconductors, far more fundamental factors may be at work.

Consider that on a television screen or matrix printer, a letter of the Roman alphabet can be displayed with an array of 5 by 7 dots—7 by 9 dots allows upper- and lower-case characters with descenders. Not only does Japan have to contend with three written character sets (four if the widely known Roman alphabet is included), but what's more, the most elaborate form, kanji, which was borrowed from the Chinese, demands at least a 16-by-16-dot matrix, and a 32-by-32-dot matrix would make possible many more of the thousands of kanji characters to be displayed.

Although another one of its character sets, katakana, is used for computing applications, a movement is spreading in Japan to popularize kanji for word processing. It is said that if a company does not offer a kanji option, it will find competing in Japan's ripening small-business computer market difficult. However, not only does kanji processing demand more complex print heads and cathode-ray tubes, but furthermore it requires more memory.

Clearly, character-generating read-only memories have to be more highly integrated for kanji processing. Nippon Telegraph & Telephone Public Corp.'s Musashino Electrical Communication Laboratory has fabricated 1- and 4-megabit full-wafer-scale ROMs for this application, and Nippon Electric Co. has made 512-K ROMs for the same purpose for the joint computer venture NEC-Toshiba Information Systems [*Electronics*, Sept. 25, 1980, p. 78].

In addition, the Japanese are eager to widen the word width of microprocessors and communications integrated circuits so as to better handle kanji. Such a move, of course, would further complicate those circuits—and their packages as well.

Finally, Japan's will to miniaturize may be remotely tied to its cultural heritage. A theme in traditional Japanese art and music is the mastery of nature. Artistic ideals are often very specific, and this characteristic has promoted perfection in some instances. In the case of semiconductors, what could be closer to perfection than an ultralarge-scale integrated circuit like a monolithic megabit memory?

Memory redundancy is a hot topic, particularly since its endorsement by Intel, a U. S. company that has inspired numerous Japanese ICs.

tion of machines, NEC, Fujitsu, and Hitachi have strong programs in ECL, digital gallium arsenide ICs, Josephson junctions, and software.

Besides the Musashino laboratory and the now defunct VLSI Cooperative Laboratory, NEC, Hitachi, and Mitsubishi all have built and tested 256-K dynamic RAMs. Toshiba and Fujitsu are less vocal about their work on this part, but they cannot be far behind. Mitsubishi is the most open about the details of its quarter-megabit memory (Fig. 5), perhaps because of its desire to play in the big-computer league.

Production of these 256-K RAMs is slated for 1983. The manufacturers agree that the transistor gates will need to be made out of refractory silicides or pure metal to circumvent the high resistance of polysilicon at the less-than-2-μm geometries involved. They also agree that 1:1 wafer-stepping lithography is also the right choice because of the stringent level-to-level registration and edge-definition requirements.

In many ways, however, these 256-K RAMs are simply 4116-type 16-K RAMs with Hi-C cells and two levels of metal. The 4116 is the widely emulated 16-K dynamic RAM pioneered by Mostek. The Hi-C cell increases storage capacitance with an added implant and was developed by Texas Instruments Inc. If current design approaches are mantained, Japanese 256-K RAM cells will look about the same, as will the layout and such circuits as the sense amplifiers.

Memory redundancy is a hot topic, particularly now that it has been endorsed by Intel [*Electronics*, Dec. 4, 1980, p. 108], the U. S. company that inspires more Japanese memory and microprocessor products than any other. By and large, Japanese RAM manufacturers did not consider redundancy for their 64-K RAMs, and they are now concerned about deficient yields at the 256-K level. Most claim that they "have not yet decided about redundancy," which can be taken to mean, "we are scrambling to figure it out."

NEC's dynamic RAMs

Innovation at the cell level might come, however, from Nippon Electric Co., the Japanese and indeed the world leader in dynamic RAMs, with close to 50% of the world market, since it has become second only to Mostek in global sales of the 4116 and is destined to become a leading supplier of 64-K chips. The innovation, first described at the 1980 International Electron Devices Meeting, is a double-diffused MOS—or D-MOS—cell structure that merges an n-channel MOS FET for reading with a p-channel MOS FET for writing; thus, this dynamic RAM requires a C-MOS process.

But with two layers of polysilicon and three-way self-alignment and by storing charge between a buried floating p-type well and the substrate, NEC's cell structure saves 50% to 60% of the area of conventional one-transistor cells; therefore the company is tempted to use this idea in its 256-K RAM. Table 2 shows how the D-MOS cell fares against other approaches that also blend storage and charge-transfer functions to save area.

NEC did flaunt a 256-K RAM at the 1980 International Solid State Circuits Conference, but that design exercise was aimed mostly at getting acquainted with wafer-stepping equipment and the 1.5-μm feature sizes involved. A new version uses pure molybdenum gates and redundancy, says Tohru Tsujide, a supervisor in NEC's semiconductor department, adding that the method for implementing the redundancy—electrical current instead of laser pulses—"has not yet been fixed." The latest chip measures 40 square millimeters (62,000 square mils) and fits into a 16-pin package. NEC expects an access time of about 150 ns.

NEC engineers have also looked at the effect that alpha radiation will have on even larger dynamic RAMs like the megabit chip. "We may have to go to static cells because of soft errors," comments Nobuyuki Yasuoka, another supervisor in NEC's semiconductor memory department. That possibility led NEC to display a 64-K static RAM, organized by 1 bit (Fig. 6). Again, however, this IC is more for show than for sale.

NEC does offer static memories as big as 16-K organized by 1 bit for high-speed applications and by 8 bits for microprocessor interfacing—and is just starting to offer fast C-MOS static RAMs and single-chip microcomputers. It was one of the first Japanese companies to offer high-density erasable programmable read-only memories and microcomputers with these ultraviolet-light–eras-

TABLE 1: INSULATED SUBSTRATE TECHNOLOGIES

	Description	Source	Drawbacks
SOS	silicon epitaxial layers grown on sapphire	many companies	many defects, high cost
Simox	separation by implanted micro-oxide	NTT Musashino Electrical Communication Laboratory	high current required to implant deep oxygen ions
Fipos	full oxidation by porous oxidized silicon	NTT Musashino Laboratory	narrow device islands
Grapho-epitaxy	epitaxial layers grown on a grated substrate are almost single-crystal	MIT Lincoln Laboratory	many defects
Lateral seeding	polysilicon on oxide is laser-annealed, using an epitaxial layer as a seed crystal	Texas Instruments, MIT Lincoln Laboratory	many defects

SOURCE: NTT MUSASHINO ELECTRICAL COMMUNICATION LABORATORY able memories on chip.

In fact, with the exception of its proprietary μCOM-4 line of 4-bit controllers and a Z80 look-alike, NEC's microprocessor portfolio is almost identical to Intel's. It is now said to be supplying samples of the 16-bit 8086 microprocessor, and there is a good chance that it will choose to build Intel's latest single-chip processor, the 8051. Indeed, if any Japanese company builds Intel's

A quick guide to Japan's fastest ICs

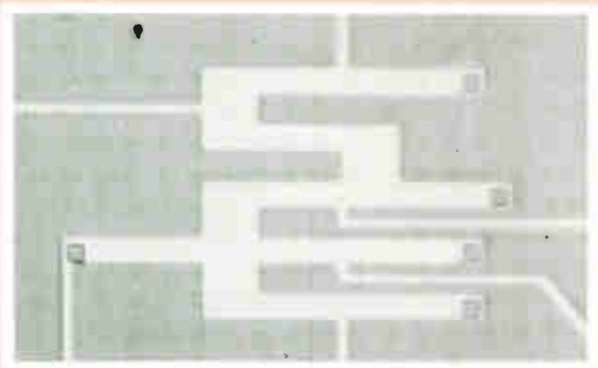
Though Japanese semiconductor makers are very handy with silicon, tomorrow's computers may be based upon gallium arsenide chips or Josephson junctions. Just in case, Japan's top computer makers and major technical universities are studying GaAs technology and Josephson junctions—"JJs," as they are often called in Japan. Some help may even come from the government, as it is rumored that the Ministry of International Trade and Industry is preparing to organize and finance efforts to develop super-high-speed device technology.

NTT's Musashino Electrical Communication Laboratory, Fujitsu, Hitachi, NEC, and Mitsubishi all have ongoing digital GaAs and Josephson projects. The Tokyo Institute of Physical and Chemical Research and Tokyo University also are investigating Josephson technology and have developed interesting fabrication techniques.

The institute, for instance, has taken the basic Josephson tunnel junction and turned it on its side. Ordinarily built vertically, with two overlapping metal films separated by an ultrathin tunnel insulator, this junction instead puts two metal pads side by side and close together under a dielectric layer. This horizontal structure is more durable, according to the institute.

Besides the tunnel junction, so-called Josephson weak links can be used to build logic circuits. A team headed by Yoichi Okabe at the University of Tokyo is using weak links to build what it calls single-flux quantum logic for shorter delays and lower power dissipation. The photograph below shows a two-input AND gate built with SFQL.

One of the goals of the project, says Okabe, is to build a central processing unit out of Josephson technology. The instruction cycle time for such a machine would be truly impressive. "From theory, we estimate that it will be several picoseconds, perhaps 5," he says.



While working on conventional GaAs metal-semiconductor field-effect-transistor logic, researchers at Fujitsu also keep plugging away at their high–electron-mobility transistor (see figure, below right). The HEMT structure consists of alternating layers of intrinsic GaAs and gallium aluminum arsenide layers selectively doped with silicon. Because of the higher electron affinity of GaAs, free electrons from the doped layers flow into the nondoped films and become extremely mobile.

Moreover, if the device is cooled to 77 K, HEMT mobility becomes even greater. Fujitsu workers have already measured mobilities of 37,800 square centimeters per volt-second and say values of 100,000 are theoretically possible. In contrast, theory states that the electron mobility in MOS FETs can only be as high as 2,000 and in GaAs not much more than 8,000. The higher mobility translates directly into greater speed. At room temperature, a HEMT switches in less than 50 ps, and Fujitsu researchers think that cooling will reduce that delay to 10 ps as fast as today's Josephson junctions.

The only problem with HEMT is fabrication. The alternating layers have to be really thin—less than 1 μm thick. So far, Fujitsu has grown them with molecular beam epitaxy on a chromium-doped semi-insulating substrate. However, it is hoping that a vacuum evaporator can instead be used for higher manufacturing throughput and expects to mass-produce HEMTs for computer use before the mid-1980s.

Another GaAs structure that can outperform GaAs FETs is the static induction transistor, or SIT, pioneered and promoted by Jun-ichi Nishizawa of Tohoku University in Sendai. Nishizawa teaches at the university's Research Institute of Electrical Communication, in addition to being director of the Semiconductor Research Institute, also in Sendai. This towering figure in the history of Japanese technology invented the SIT in 1950—not long after U. S. researchers discovered the FET. His countrymen are proud to call the SIT "purely Japanese."

Actually, the SIT can be built from any semiconductor material, but the high mobility of GaAs raises its performance. Significantly, it can also deliver high power at high frequencies, making it suitable for discrete thyristors. Nishizawa has also built or proposed various SIT integrated circuits, including memories, integrated-injection-logic circuits and image sensors. Indeed, says Nishizawa, "we are confident that MOS FETs will sooner or later be replaced by MOS SITs" and that the "development of the SIT should precede that of superconductive devices."

The SIT resembles a FET except that the channel is made much shorter to minimize gate capacitance and

Hitachi carries a broad line of memories and microprocessors. It goes to Motorola for help with microprocessors and receives mask sets.

iAPX 432 32-bit VLSI processor on three chips, NEC is the most likely candidate.

NEC also offers a variety of peripheral chips—most designed by Intel—but recently Intel has opted to build some support products created by NEC. These include the μPD765 double-density floppy-disk controller and the μPD7220 color graphics controller [*Electronics*, April 7, 1981, p. 153]. Although the relationship between Intel and NEC appears to be strengthening, the companies do not, as yet, exchange masks or process know-how—or so they say.

NEC's bipolar process, called APSA, for advanced polysilicon self-alignment, is indeed one of the most advanced in the world. That key determinant of speed, the size of the APSA transistors' emitters, is a mere 1 by 3 μm but is attained, according to NEC, by means of conventional lithography and plasma etching. Elsewhere, however, APSA does make clever use of oxidation and polysilicon deposition to help relax lithography requirements. Although the emitter window is originally opened with a minimum width of 1.5 μm, subsequent oxide growth encroaches on it, narrowing it to 1 μm.

Two levels of polysilicon are used in APSA processing, the first for base and collector electrode formation and the second for the emitter contact. In three separate steps, dopants are diffused through the polysilicon electrodes, forming reliable, self-aligned connections to the underlying silicon transistor areas. To combat the high sheet resistivity of the polysilicon, NEC uses platinum-silicide as a shorting strap, grown atop both polysilicon levels. With APSA, NEC has achieved gate delay times of 300 ps at a power consumption of 1.5 milliwatts.

Interestingly, NEC has chosen current-mode logic, or CML, as the circuit form for its APSA. This nonsaturating ECL-like circuit, once sought for its high density and low power, has fallen into disfavor, probably because of its unusual power-supply requirements. These requirements had limited NEC's APSA CML chips to internal applications: a 1-gigahertz frequency divider and a 1,000-gate array. But now NEC is beginning to produce standard-type ECL devices with APSA; the next destination for the technology may be a high-performance ECL family based on the popular 2900 series of bit-slice processors.

NEC has big programs under way to develop both analog and digital gallium arsenide ICs. In Japan, the company is the largest producer of GaAs monolithic microwave devices. But worldwide, it recognizes Plessey Semiconductors as No. 1 in the development of monolithic microwave ICs, with TI and Hewlett-Packard Co. following. In monolithic microwave, NEC has built amplifiers and front ends.

C-MOS is tops at Hitachi

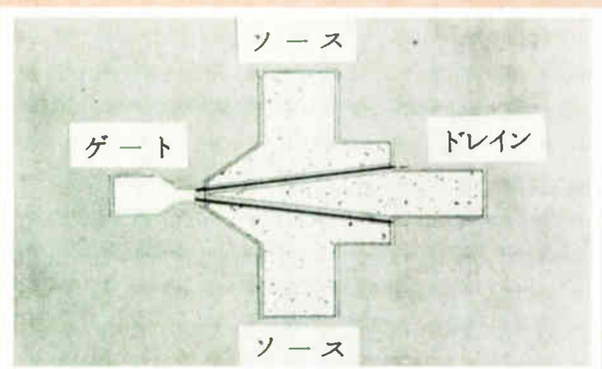
Hitachi Ltd. also has a broad line of memories and microprocessors. However, it goes to Motorola for help with microprocessors and for mask sets and design expertise. In one of its latest deals, Hitachi described its

channel resistance. Nishizawa builds the devices vertically so that lithography is not directly responsible for channel length, which he has reduced to well below 1 μm.

On the other hand, he says, "it may be said that the SIT is a bipolar transistor in which all the impurities in the base region are ionized and that is nearly in a punched-through state." However, when an ordinary bipolar transistor is in this state, its base resistance becomes very high, hindering high-frequency operation. With the SIT, high-frequency gain is maintained through the static induction effect—the drain voltage is simply increased, and this increase lowers the potential barrier of the channel's depletion region, allowing more current to flow.

Nishizawa has employed anisotropic etching, oxide isolation, and annular base contacts to improve the SIT's speed. With these processing enhancements, he estimates operating frequencies of about 800 gigahertz, with 1 terahertz possible with the addition of tunnel junctions. When numerous gate electrodes are actually embedded in the channel region, the structure begins to look like the permeable base transistor spearheaded by the Lincoln Laboratory of the Massachusetts Institute of Technology [*Electronics*, Dec. 6, 1979, p. 130]. Thus, the permeable base transistor and other superhigh-speed structures, such as the ballistic GaAs transistor, "must be included in the SIT family," according to Nishizawa.

Several companies have already begun cashing in on the SIT's potential for high power. Mitsubishi Electric Corp. has come up with a SIT that delivers 100 watts at 1 gigahertz, and Toshiba Corp., a 20-W, 2-GHz device. Hitachi has also picked up on the technique. These specifications are almost good enough for SITs to replace the klystron in microwave ovens. In fact, Mitshubishi is said to be developing a 2.45-GHz SIT for that purpose.



high-performance C-MOS, or Hi-C-MOS, process to Motorola in return for the 68000 mask set.

Samples of the HD 68000 have just begun to appear in Japan. The bugs should soon be shaken out of the companion 68450 direct-memory-access controller, and by the fourth quarter of this year the 68341 floating-point ROM chip for the 68000 will be completed. Hitachi has considered E-PROM versions of the single-chip microcomputers that it makes, but it will instead offer piggyback packages that standard E-PROMs can plug into.

Hitachi is undoubtedly adept at building n-MOS devices; its 64-K dynamic RAM [*Electronics*, July 31, 1980, p. 103] is one of the few solid winners in this market. But its real strength seems to be in C-MOS. Its Hi-C-MOS single-polysilicon process was perhaps the first commercial verification that bulk C-MOS can be low in power and very high in speed at the same time. Indeed, the Hi-C-MOS 6147 4-K fast static RAM may have been a factor in Intel's recent decision to bone up on C-MOS [*Electronics*, Dec. 4, 1980, p. 39].

Having completed 2-K-by-8-bit and 16-K-by-1-bit Hi-C-MOS static RAMs, Hitachi has come up with Hi-C-MOS II, a second-generation process that scales down to 2 μm for a 4-K memory with an 18-ns typical access time [*Electronics*, Feb. 24, 1981, p. 141]. Hi-C-MOS II also adds a second polysilicon layer for an unsurpassed 0.61-mil^2 (392-μm^2) cell area.

Still, this 18-ns 4-K Hi-C-MOS RAM is merely a test vehicle for a 64-K static RAM Hitachi intends to offer around the first half of next year. The chip area for this 8-K-byte memory will be about 35 mm^2 (54,250 mil^2), and access times of 120 to 200 ns are anticipated.

Hitachi's near-term plans for the Hi-C-MOS process will be to build other device types with it. The firm is on the verge of releasing a Hi-C-MOS version of Motorola's 6801 single-chip microcomputer that will have six added instructions and a powered-down consumption of 300 microwatts. Patterned very regularly, the remake contains an internal 32-bit microprogram ROM over 300 words deep. To improve system reliability, it also incorporates traps for improper operation codes and addresses. Because of these alterations to the basic 6801 architecture, Hitachi calls its version "proprietary."

Later this year, the company will begin to market a 1,500-gate Hi-C-MOS gate array based upon three-input NOR basic cells. Using 2-μm minimum features, the device should have gate delays on the order of 2.5 ns, Hitachi says. Since Fujitsu already offers a 3,900-gate C-MOS array, "our goal is to catch up with them," says Tsugio Makimoto, deputy general manager of Hitachi's Musashi works.

Toshiba is pushing SOS

Besides Hitachi, Toshiba and Matsushita are also gearing up for the production of 64-K static RAMs. Meanwhile, U. S. chip manufacturers are barely getting their 16-K static RAMs out the door. In fact, with Kawasaki-based Toshiba Corp.'s recent announcement that it will sell its 2-K-by-8-bit n-MOS static memory for less than $10 apiece in large quantities, U. S. semiconductor firms are starting to think that the 16-K density level is already an economic lost cause.

Perhaps experiencing a little difficulty in defining just what the buying public wants, Toshiba designed three different 64-K static RAMs: two in C-MOS and one in n-channel (Table 3). The manufacturer claims that there are separate markets and separate applications for the products. However, beating the rest of the world to that density of static RAM left the company with no model to emulate, and the extra design effort may simply reflect a fear of announcing a losing component, even if it is a standard memory.

Toshiba has divisions that manufacture industrial machinery, household appliances, small computers and, of course, semiconductors. The overall product line has been compared to that of Westinghouse Electric Corp.,

3. Pure technology. To keep NTT's telecommunications system up to date, its Musashino lab must constantly push the state of the art in semiconductors. Makoto Watanabe, director of the lab's IC development division, says bipolar technology will win out over MOS.

Toshiba is going to take silicon-on-sapphire chips to the merchant market. 'There are no barriers to selling SOS parts on the outside,' it says.

but it is also Japan's third-largest chip vendor.

Last April, Toshiba completed the purchase of Maruman Integrated Circuits Inc. in Sunnyvale, Calif. It kept much of Maruman's old staff, but instead of ROMs and custom semiconductor products, the Japanese company will use the facility first for 4-K static and 16-K dynamic RAMs and then for higher-density static parts and microprocessors. Thus, Toshiba's takeover of Maruman is akin to NEC's recycling of Electronic Arrays Inc. in Mountain View, Calif. So far, it has spent over $10 million on capital equipment to improve Toshiba Semiconductor USA Inc.

Toshiba has long been in the bulk C-MOS business. In the early 1970s, it used clocked C-MOS logic—which it calls C^2MOS—for calculator applications. C^2MOS has been both steadily scaled down and speeded up ever since and is now the basis for the company's high-density static RAMs and C-MOS versions of Intel single-chip processors like the 8-bit 8049. It was the first company in the world to offer an all–C-MOS 16-K static RAM.

Toshiba has also gained quite a reputation for its work with C-MOS on sapphire. In fact, while early promoters are now deemphasizing commercial silicon-on-sapphire products, Toshiba seems to be going the opposite way.

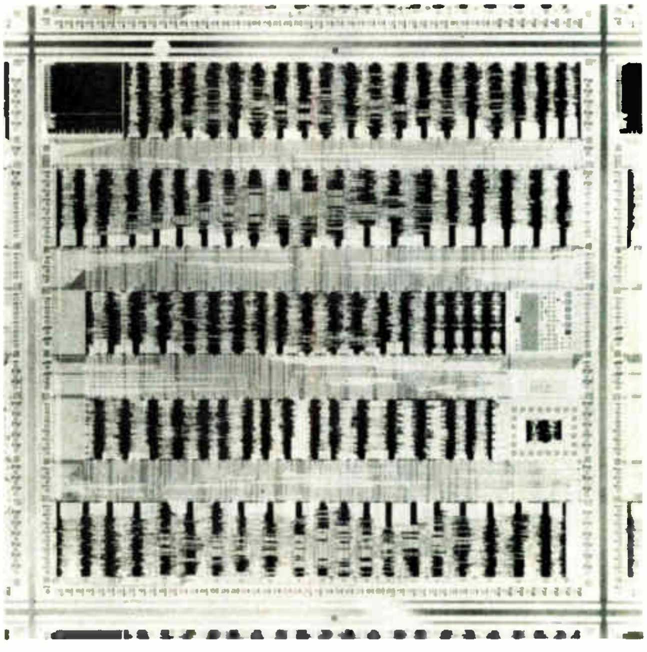
Just as HP did for its HP 300 [*Electronics*, Feb. 1, 1979, p. 108], Toshiba designed a proprietary C-MOS-on-sapphire central processing unit called the T88000 to replace bit-slice components in its own Tosbac series 7 minicomputer. But unlike HP, which decided to drop SOS in favor of scaled-down bulk n-MOS, Toshiba went on to design a superfast 18-ns 4-K-by-1-bit static RAM that it will take to the merchant market [*Electronics*, Sept. 11, 1980, p. 80]. "I don't see any barrier to selling SOS parts on the outside," avers Hiroyuki Tango, manager of Toshiba's SOS technology group. Meanwhile, the general consensus among other Japanese chip makers is that Toshiba will go the way of RCA Corp. and soft-pedal standard SOS parts.

Toshiba at present buys sapphire wafers with epitaxial layers from Kyocera International Inc. and Monsanto Co. It plans to save money by growing its own silicon epitaxial layer, and it is now building a factory to handle 4-inch sapphire wafers when they become available. Future SOS chips may include peripheral circuits for the 88000 like a floating-point math unit or a signal processor. If the 4-K RAM makes it, Toshiba will build high-speed 16-K static RAMs on sapphire, and it may even add an extra power-supply pin for voltage-level shifting to make them compatible with ECL.

As with SOS, Toshiba is also taking integrated injection logic to new heights in the face of many chip makers that have lost interest in that bipolar circuit technology. For the highest performance, however, Toshiba turns to ECL and builds it with advanced NSA, which stands for nitride-self-alignment. Most of Toshiba's bipolar work is for consumer applications such as television prescalers and audio and video analog-to-digital converters. To save die area, most of Toshiba's bipolar chips use double-level aluminum metalization. According to Masakatsu Nakamura, manager of the advanced semiconductor technology department, Toshiba has come up with a secret method that allows phosphosilicate glass (PSG) to adhere to aluminum, enabling it to use that inexpensive material as the intermetal dielectric.

Toshiba's I^2L is fairly straightforward, except that the company is fond of combining ECL or high-voltage analog circuits on the same chip. It improved upon the basic I^2L structure by adding extra base regions to each gate in order to increase fanout and switching speed. When I^2L is combined with ECL, four separate p-type implants are shared between the two circuit types to optimize their characteristics. With its I^2L-ECL technology, Toshiba has produced some highly integrated digital phase-locked–loop tuning systems that interface directly with key pads and displays.

Toshiba calls upon its nitride self-aligned process for the even higher radio and ultrahigh frequencies. Its basic NSA and advanced NSA processes are capable of 4-GHz



4. Design by computer. This 32-bit microprocessor from NTT's Masashino lab is a testament to its computer-aided design savvy. Over 12,000 three-input Schottky TTL logic gates were automatically positioned and interconnected in a matter of one month.

operation. The trick with NSA is to deposit a film of silicon nitride over a very thin thermally grown oxide layer. With the nitride serving as a mask, a 2-μm via is opened in the oxide for emitter formation and contact regions. Since the oxide is so thin, very little undercutting occurs during etching, unlike the case with conventional processes, which etch through thick thermal oxide.

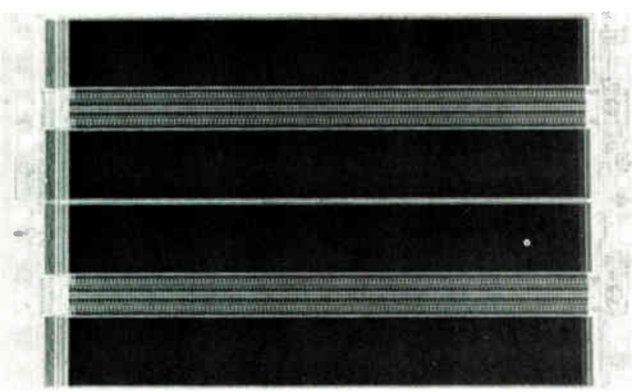
After the 2-μm emitter window has been opened, doped polysilicon is laid down as the emitter electrode. Impurities are allowed to diffuse out of the polysilicon to form a very shallow emitter region. Finally, an aluminum-silicon-copper metalization system is employed for insurance against electromigration and corrosion.

Fujitsu, the computer house

Fujitsu is the "purest supplier of computer and communication equipment in Japan," states Mirek J. Stevenson, chairman of Quantum Science Corp., a New York market research firm. Enlarging on this view, Matami Yasufuku, managing director and general manager of the Kawasaki-based company, says, "Our product families are different from those of, say, Hitachi or NEC. We produce hardly any consumer products."

Fujitsu is Japan's strongest computer builder and it is getting mightier. In 1980, there was a quiet celebration because, for the first time, it surpassed IBM Japan Ltd. in computer sales to its domestic market (¥300 billion versus ¥266 billion). Fujitsu is also infiltrating the U. S. market faster than any other foreign computer maker through agreements with Amdahl Corp., TRW Inc., American Telecommunications Corp., and a growing list of others.

Many industry observers also believe that Fujitsu leads in the research and development of computer-related high-speed technologies. At the component level,



5. Four for a million. NEC, Fujitsu, Hitachi, Toshiba, and the Musashino lab all have designed 256-K random-access memories. So has Mitsubishi; its chip is depicted above. All will use silicide or metal interconnections and higher-capacitance cells.

the company is a leader in MOS and bipolar memories and gate arrays, according to Quantum Science's Stevenson. It is one of the few Japanese companies to push magnetic-bubble memories—it was first in the world to offer a removable bubble cassette, and so far three U. S. companies—National Semiconductor Corp., Intel, and TI—have followed its lead. Fujitsu is also committed to gallium arsenide for its next generation of machines and Josephson junctions for the generation following.

Fujitsu's approach to semiconductor technology is to integrate on a larger and larger scale using more computer-aided design all the time, but not necessarily to innovate at the device level. In silicon-gate C-MOS with two metal levels, it has fashioned a 3,900-gate master slice—the biggest of its kind—and a 16-bit 10,000-gate processor chip for use in its V and system 80 series of Facom computers. Both dice are enormous. The CPU chip measures 172,484 mil² (111 mm²), and the gate array 145,840 mil² (94 mm²).

Fujitsu is "now setting up a design automation center in Santa Clara, Calif., to support our gate array business," remarks Yasufuku. "That is the first step," he continues. "The second step will be metalization in San Diego," where Fujitsu already conducts a minimal amount of IC assembly. The firm's arrays have had three metal levels for over a year and require six masks for customization as a result.

Fujitsu's microprocessor strategy seems to lack direction at present. It makes Motorola's 8-bit 6800 and Intel's 8086 and two other different 16-bit MOS machines for internal consumption.

Its memory product lines are much more in order. It supplied the world's first 64-K RAM (to NTT)—albeit a three-supply part—and it is one of the largest manufacturers of E-PROMs in Japan. It says it will have samples of its 256-K dynamic RAM ready this year. Although it has yet to make electrically erasable PROMs when it does, it will employ a superior proprietary process.

Yasufuku says Fujitsu's relationship with NTT is "nothing special. Like NEC and Hitachi, we supply them with custom parts occasionally." Also, "we have no real dealings with IBM." In sum, Yasufuku points out that although Advanced Micro Devices is smaller than Fujitsu, its bipolar product lines are similar. "In MOS, our products are most like Intel's. So add AMD and Intel and divide by two," he kids.

Chasing bipolar at Mitsubishi

Mitsubishi Electric Corp. it used to be a lot like Westinghouse, but has increased its production of semiconductors to the point where its product lines now more resemble Motorola's. In Japan, it resembles Hitachi;

'It's not impossible for a Japanese manufacturer to break into the 8- or 16-bit field,' says Mitsubishi. These microprocessors will evolve, as did 4-bit units.

their consumer product output is about the same, but in overall sales Hitachi is more than twice as large.

About 30% of Mitsubishi's semiconductors (including hybrids) are discrete devices. Most of the company's production is carried out at its Kumamoto plant, with its IC preproduction and discrete wafer processing done at its Kita-Itami works. The company has n-channel and C-MOS expertise, but its bipolar divisions are most active, developing circuits based upon ECL, I^2L, and TTL.

Its ECL is used in part to make gate arrays, a product area that it is stressing. It has been selling an n-MOS array to its computer division for two years, it has a good start on ECL arrays, and it will one day make them in C-MOS. It has a comprehensive CAD system capable of reverse-engineering a device (deriving its logic diagram from a mask-set data base), and it is going to use a satellite communications system to ship array codes around the globe.

Hisao Oka, general manager of Mitsubishi's LSI research and development lab feels that its ECL gate arrays are among the world's best. Yasutaka Horiba, an engineer in the firm's logic and LSI design group, explains that the finest arrays almost produce a straight line when plotted on a delay-complexity graph like the one in Fig. 8. Besides his company's 2,500-gate ECL array, Horiba believes top arrays include IBM's 7,000-gate low-power Schottky TTL device [*Electronics*, Oct. 9, 1980, p. 139], NEC's 1,200-gate CML array, and a new ECL slice from Hitachi containing 1,500 gates.

So far, Mitsubishi has shown two ECL arrays, one with 900 gates and another, in development, with 2,500. Its computer works began receiving the 900-gate units last fall and shipped the first machine utilizing them in March. This computer uses about 200 of the chips in all.

The average delay of the gates in the 900-gate array is about 1.1 ns, but it will be only 0.8 ns in the 2,500-gate array now in the works. That big IC will have 224 pins and will be housed in a flip-chip–type package. Mitsubishi also has an ECL RAM in development, and neither it nor its arrays use polysilicon as a conductor—though that idea, too, is being considered for future parts.

MOS RAMs from Mitsubishi are also well up to standard. Its 64-K RAM was recently overhauled, and its refresh requirement of 256 cycles every 4 milliseconds was switched to one for 128 cycles in 2 ms. The later revision also incorporates a self-refreshing function and Hi-C cells, both of which can be found in Motorola's part [*Electronics*, Feb. 15, 1979, p. 141], and polysilicon bit lines, which Mostek's 64-K-RAM uses.

Mitsubishi also has done some pioneering work on epitaxial layers for dynamic MOS memories [*Electronics*, Feb. 10, 1981, p. 93]; it may turn to epitaxy for its 256-K RAM, which now measures 8.47 by 5.29 mm (69,550 mil²) and uses a silicide for speed. In fact, Mitsubishi expects access times as low as 60 ns on the device. Fast static RAMs are still in the lab, but a byte-wide 16-K n-MOS static memory has been moved into production. Mitsubishi was an early mover on C-MOS E-PROMs, building an 8-K memory with a process called Fa-C-MOS, for floating-gate avalanche injection [*Electronics*, Feb. 15, 1979, p. 39].

Like NEC, Mitsubishi has a fondness for Intel's microprocessors. It will fabricate the 8048 and 8049 single-chip microcomputers and the 16-bit 8086 microprocessor—it will even build the 8-bit–bus version of the 8086, the 8088. "Mitsubishi's manufacturing division likes Intel parts, so we must prepare for them," states Kazuaki Harada, Mitsubishi's microprocessor and memory manager. But he does not think "it's impossible for a Japanese manufacturer to break into the 8- or 16-bit field." As with 4-bit devices, 8- and 16-bit units will evolve for special applications in Japan, he surmises.

As a matter of fact, the firm is now defining a unique microprocessor for channel frequency synthesis in TV sets. NEC is working on a similar IC. Besides the microprocessor CPU, Mitsubishi's chip will include a phase-locked loop and remote-control logic.

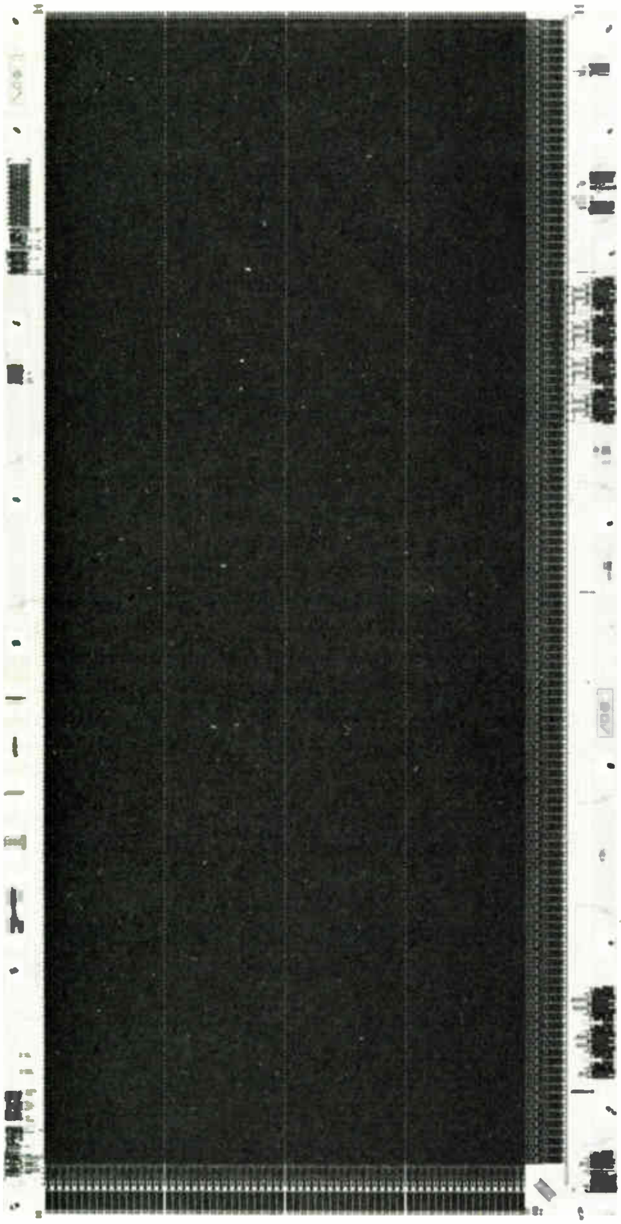
Elsewhere at Mitsubishi, a-d converters, watch and clock chips, and speech synthesizers are designed. Like most speech chips from Japan, Mitsubishi's is based upon the Musashino lab's Parcor method, "because the development software can be purchased from NTT," says Kiyoshi Hosomi, deputy manager of dedicated MOS and ICs. He adds that since "speech quality must go up and memory prices are going down," the firm is investigating techniques that offer higher fidelity but necessitate higher bit rates.

TABLE 2: A RATING OF SINGLE-DEVICE DYNAMIC MEMORY CELLS

Characteristics	Diffused MOS (D-MOS)	Stratified charge	Taper-isolated
Process required	double-polysilicon complementary-MOS	double-polysilicon C-MOS	single-polysilicon C-MOS
Density	2*	1.5	2
Readout signal intensity	5	3	5
Refresh interval	1	10	10
Three-level drive line	address line	address line	bit line
Soft-error rate	1	1	1
Complexity of sensing circuitry	1.5	2	2
Maturity	0.75	0.5	0.25
Overall score	2.5	2	1

*All numbers used in this table are normalized to 1, the value assigned to a conventional double-polysilicon n-MOS cell.
SOURCE: NIPPON ELECTRIC

Of the consumer chip makers in Japan, Matsushita Electric Industrial Co. in Osaka and Sharp are about the same size, with semiconductor sales nearing $300 million annually in each case. Matsushita Electric is perhaps better known under its brand names: National, Panasonic, Technics, and Quasar. These names are stamped on motors, audio and video equipment, kitchen appliances, batteries, office computers, calculators, and communications gear. Electronic components are handled by Matsushita Electronics Corp., sometimes abbreviated MEC. Even though NV Philips Gloeilampenfabrieken of the Netherlands now controls about 35% of Matsushita Electronics, all management decisions are made in Japan.



6. Why 1 bit wide? NEC's 64-K static RAM is organized by 1 bit, unlike the 64-K static RAMs due from Toshiba, Hitachi, Matsushita, and others, which will be arranged into bytes. NEC says that because of alpha-particle problems, dynamic RAMs may have to go static.

About 50% of Matsushita Electronic Corp.'s business consists of semiconductors. Its electronic tube group, which makes cathode-ray tubes, vidicons, and magnetrons, accounts for another 40%, and the rest is taken up by its lighting division. MEC's headquarters are in Nagaoka, as is its biggest LSI fabrication facility. Bipolar chips are also built in Arat.

Matsushita's consumer chips

Matsushita's hottest semiconductor products are those associated with sophisticated consumer products now in development. For instance, the company is perfecting laser diodes for video disk players and image sensors for miniature television cameras. Also, though Matsushita has not yet unveiled its entry, it will join several consumer product makers in Japan beginning in 1982 to market pocket television sets. Figure 9 shows Hitachi's model.

Says Matsushita Electronics Corp.'s executive vice president, K. Fujimoto: "We are a broad-line supplier, broader than TI. We have 60% of the video tape recorder market. We are very strong in 4-bit microprocessors and will ship 30 million units this year. We control 70% of the Japanese market for MNOS [metal nitride oxide semiconductors]. Our latest static RAM has 400,000 elements—and you'll be able to buy it this year.

"We are the biggest clock-chip maker in Japan," he continues. "We are No. 1 in the world with bucket-brigade delay lines for audio applications. We produce 60% of the world's total of bipolar video chips. We use I^2L quite a bit to combine analog and digital functions on one chip. We'll ship 25 million chips this year for camera and tape recorder applications. We have 90% of the Hall-effect IC market. We'll ship over 100,000 gallium arsenide FETs this month for tuning applications—we are leaders here. We'll mass-produce about 380 million solid-state devices—about three times the Japanese population—per month."

Consumer chip companies such as Matsushita have helped Japan establish a commanding lead in solid-state imaging technology. Along with contributions from Hitachi, NEC, Sony, and others, the Japanese have tried about every combination of materials, structure and scanning sequence for their area arrays.

Most companies have experimented with both interline-transfer and frame-transfer image sensor organiza-

'We are a broader supplier than TI,' says Matsushita. '. . . Our latest static RAM has 400,000 elements, and you'll be able to buy it this year.'

tions. In the former scheme, both the sensing electrode and the transfer gate are squeezed into the unit cell of the array. Frame-transfer sensors, on the other hand, are characterized by an independent array of sensing electrodes and an on-chip storage buffer of the same dimensions; in them information is gathered and then dumped into the buffer, frame by frame, before being shifted out in linear fashion.

Problems with blooming—picture saturation caused by local luminance overloads—have been solved with overflow drains, as they are called. When a cell becomes saturated, an overflow control gate is triggered that skims off the excess charge and routes it into the drain.

The arrays have been put into both black and white and color cameras, with filters for the color versions located both on and off chip. Three-, two-, and one-chip color cameras have been designed, the former two using beam splitters and the last type employing on-chip filters that extract a green or a blue-red spectral response from alternate cell rows.

Matsushita has already developed three different solid-state image sensors, two for color cameras and one for black and white. The black and white frame-transfer sensor, which uses a charge-coupled-device imaging area and an on-chip CCD storage buffer, has been in production for over a year. One color imager uses inter-line-transfer CCDs [*Electronics*, Jan. 31, 1980, p. 62]. The other, called a charge-priming device, or CPD, uses a precharging technique to interface an MOS image sensor with a CCD output shift register, thus taking advantage of both the high sensitivity of MOS and the low fixed-pattern noise of CCD transfer gates.

The company must also be given credit for its microprocessor and memory achievements. Its MN1400 line of 4-bit microprocessors is very popular, and now comprises 31 types: 21 in n-channel, 3 in p-channel and 7 in C-MOS. It recently used high-performance n-MOS to upgrade the 1400 series and thus produce the MN1500 series [*Electronics*, July 3, 1980, p. 145]. For customers who need 8 bits, Matsushita is producing Motorola's 6802 and it will manufacture other members of the 6800 family. Its proprietary MN1600 was the first Japanese 16-bit microprocessor. Since its introduction, the company has reduced the number of required power supplies from three to one and added support chips like an input/output interface adapter, real-time system controller, and a DMA controller. Imminent is the MN1613: a fast version that reduces the register-to-register instruction cycle from a high of 1 μs to 300 ns.

Matsushita was the first company in the world to describe a 64-K static memory [*Electronics*, Feb. 14, 1980, p. 138; Nov. 6, 1980, p. 145]. Moreover, this was the first memory device to exploit n-well C-MOS, a process that many—including Intel—deem valuable because it favors the faster n-channel transistors rather than p-channel ones. Takashi Ohzone, the Matsushita manager who led the RAM's design team, holds basic patents on ion-implanted first- and second-level polysilicon resistors and has also published the first papers on memories that use them.

Matsushita's gallium arsenide components can be commended for their low noise figures. It recently completed an amplifier that spans the very-high- and ultra-high-frequency bands with a noise figure of only 2 decibels over the 50-to-2,000-megahertz range [*Electronics*, Feb. 24, 1981, p. 82]. The device, which is going into television tuners at a rate of over 100,000 per month since last year, is called "the first mass-produced GaAs device" by Gota Kano, head of Matsushita's solid-state device development department.

Matsushita also has a novel way of building laser diodes: with an S-shaped step running the length of the

TABLE 3: A LOOK AT TOSHIBA'S 8-K-BY-8-BIT STATIC RANDOM-ACCESS MEMORIES

	T6167	T6228	T6134
Technology	n-channel MOS	complementary-MOS	
Cell size (μm/mil)	15 by 23 / 0.59 by 0.91	15 by 19 / 0.59 by 0.75	19 by 22 / 0.75 by 0.87
Cell pull-up device	second-level polysilicon resistor		p-channel transistor
Chip size (mm/mil)	4.5 by 7 / 177 by 276	4.6 by 6.9 / 181 by 272	5.6 by 7.4 / 220 by 291
Typical access time (ns)	70	100	
Current consumption, active/standby (mA)	70/15	5 per MHz / 3 (0.05*)	5 per MHz / 1 (0.001*)
Operating temperature (°C)	0 to +70		−40 to +85
Possible availability	1982	1981	1982

NOTE: All devices are in 28-pin standard packages. *With CE = V_{DD} −0.2 V. SOURCE: TOSHIBA

7. Look at this. Mitsubishi makes n-channel and complementary-MOS devices, but its bipolar IC lines seem most active, fabricating ECL, I^2L, and TTL circuits. Hisao Oka, manager of research for large-scale integration, is proud of the company's gate arrays.

device. This kink in the substrate helps to define the channel and lengthen the life of the unit.

Other ongoing consumer electronics projects at Matsushita include the development of a 145-MHz phase-locked-loop frequency synthesizer in C-MOS and a two-chip set for pulse-code-modulation digital audio applications. The competition in the PCM digital audio area will include a three-chip set, one each designed by Toshiba, Sony, and Sanyo, and a five-chip set to come out of a collaboration between Hitachi and JVC.

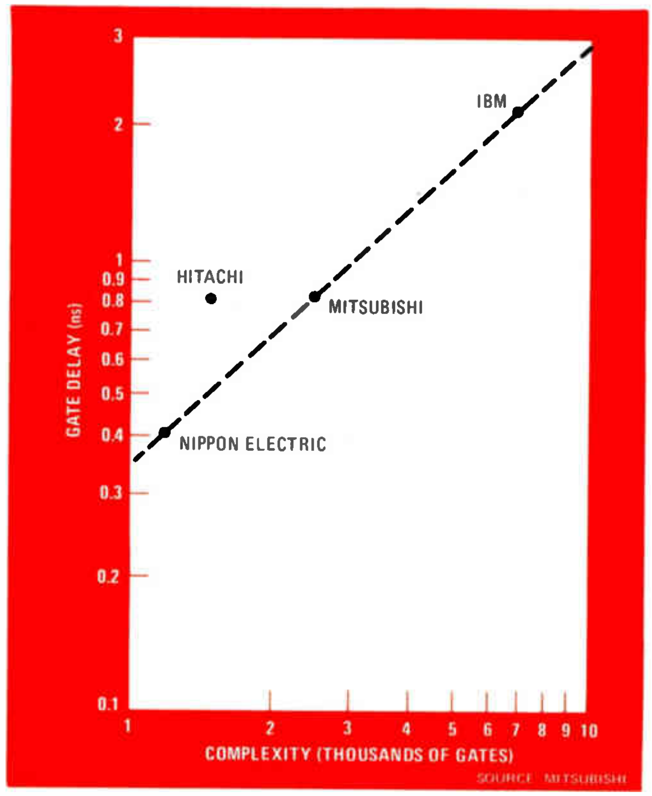
Sharp: from pencils to ICs

Sharp Corp., Osaka, got its name from the Ever-Sharp mechanical pencil invented by its founder back in 1915. It developed a vacuum-tube radio in 1929 and by 1953 was mass-producing television sets. In 1962 it got into the microwave oven business; a year later it began marketing photovoltaic cells. In 1964, it claims to have invented the world's first all-solid-state desktop calculator. In 1976, two of its product lines merged in a solar-powered calculator (the pocket-sized model would wait until 1980), and it claimed the creation of the first film-carrier for IC production, also in 1976.

Sharp is still renowned for its calculator production. Its calculator sales are about the same as Casio Computer Co.'s; the two frequently play catch-up with sales figures. It is also big in appliances and audio and video components. When it comes to semiconductor components, Sharp builds a higher percentage of custom components than Japan's other consumer electronics companies, and given a choice of technologies, it prefers C-MOS to bipolar.

"Our C-MOS process is quite different from that of the other manufacturers," comments Yoshimasa Aoki, general manager of Sharp's IC division. "We use more masks." For example, in the case of its metal-gate C-MOS process, it uses 12 masks to keep source-drain regions from being diffused with more than one dopant. Aoki also thinks that n-well C-MOS is a better way to get higher speed and scaling, and "our advanced technology department will soon announce an n-well process started two years ago."

Like most Japanese chip makers, Sharp carries its own



8. On line. Yasutaka Horiba, an engineer in Mitsubishi's logic and LSI design group, says that the best bipolar gate arrays in the world fall on or near the straight delay-complexity-line plotted on the graph. He also respects Fujitsu's 3,900-gate C-MOS array.

Sharp started out making mechanical pencils. Then it made radios, televisions, and desktop calculators, all with chips inside.

line of 4-bit microcontrollers. Called the SM series, they tend to be more specialized than the general-purpose units from other vendors, however. To cite just one example, the SM-200, used in security applications, has a 3,072-by-9-bit ROM, a 132-by-4-bit RAM, and 14 to 37 I/O lines.

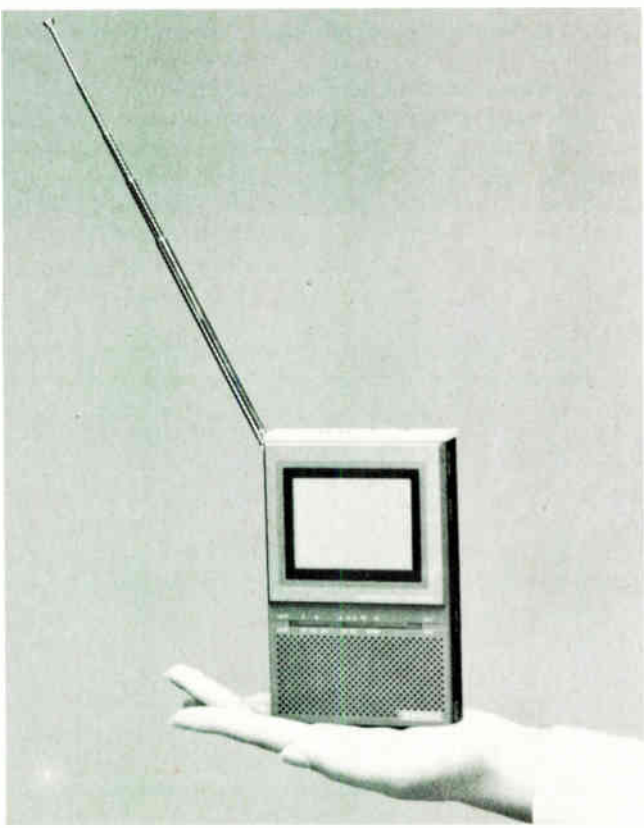
Sharp's latest 4-bit chip is the SM-540, which is capable of driving a 16-by-16-dot liquid-crystal-display matrix directly. Such a device has an enormous variety of applications, one example being is pocket-sized electronic games like the one shown in Fig. 11. Of the C-MOS microcomputer's 60 pins, 40 are used to drive the display.

Eight- and 16-bit microprocessors and microcomputers from Sharp are derived from Zilog Inc.'s products. It has been making the 8-bit Z80, and it is just now delivering samples of the 16-bit Z8000. It also intends to be an alternative supplier of the Z8 single-chip microcomputer. Sharp also makes five peripheral chips for the Z80 as well as Zilog's 4-K-by-8-bit pseudostatic memory. Though it was once rumored that Sharp traded its C-MOS expertise for Zilog's mask sets, it turns out that Sharp simply paid for them.

Although Sharp makes high-density memories, it refuses to waste too much time and energy on highly competitive models. It has just started to mass-produce the 16-K dynamic RAM, but that may also be the last leading-edge C-MOS dynamic RAM it makes. As might be expected, it would rather concentrate on C-MOS static RAMs and ROMs. It has already completed a 132-K C-MOS ROM, but interestingly, it has so far hit only the 4-K level with static RAMs.

For its size and product lines, Sharp has a very sophisticated computer-aided design system. According to Ikuo Nishioka, manager of Sharp's CAD center, the two differences between its system and that of other Japanese chip makers are the capacity to do symbolic layout—which it began doing some 10 years ago—and the

9. In hand. The coming decade will bring pocket-sized television receivers fron Matsushita, Sharp, Toshiba, and the rest of Japan's consumer electronics manufacturers. Most, like the unit from Hitachi below, will rely on solid-state liquid-crystal displays.



10. All smiles. Matsushita Electric Corp.'s executive vice president K. Fujimoto has reason to be happy. His company has assumed a commanding role in many consumer electronics product lines with 4-bit microcomputers, clock chips, and audio and video devices.

ability to derive random layouts from inputs in the form of Boolean expressions.

Sharp is also committed to a flat-panel LCD for video applications. Tadashi Sasaki, senior executive director and general manager of Sharp's engineering center, feels that his company is as far along on a video LCD as the any of the other contenders—Hitachi, Sewa Seiko, Toshiba, and Matsushita.

Sasaki also believes that resolution of the displays will have to be increased to please the public. The problem, he says, is that "when the resolution of an LCD goes up, the quality of the display goes down" without an advanced interlacing scheme. Sharp intends to announce such a method, and Sasaki thinks it may be the first real solution to the problem. Still, it will take four to five years before pocket TV sets will become a commercial reality, at which time the display alone may cost $500, he says.

Sanyo chooses molybdenum

The product line of Sanyo Electric Co. in Moriguchi is similar to Matsushita's, but the firm is only a third Matsushita's size; indeed, Matsushita and Sharp are its biggest competitors. To stay ahead of the game, Sanyo is investing over $50 million over the next four years in a new VLSI research center to serve all of its divisions. The goal is 1-μm pattern definition, and it will use electron-beam lithography to get there. Electron-beam exposure is no new trick for the company, either; in fact, it claims it developed the world's first such exposure system (Fig. 13), which was described at the 1964 International Electron Devices Meeting.

Use of molybdenum is not new to Sanyo, either. A comment from Toshiaki Hayashida, manager of the VLSI project, is that "high-speed MOS should not be C-MOS, it should use moly gates." Hayashida thinks that with minute geometries and molybdenum gates, MOS will break the 1-GHz barrier, allowing it to be used for video processing in future digital televisions. It already has very fast a-d and d-a converters and phase-locked loops in the works toward that end (Fig. 14).

Sanyo also uses molybdenum for a unique nonvolatile memory structure [*Electronics*, Dec. 6, 1979, p. 96] that it has licensed to Fairchild, but which that U. S. company has so far failed to exercise. The nonvolatile memory, which remembers stations in a TV tuning system, is based upon a process that Sanyo calls MNMOOS, which stands for its metal-nitride-molybdenum-oxide-semiconductor structure. The principle is the same as that in an MNOS memory, except that molybdenum is used in lieu of nitride as the floating-gate material. Sanyo's nonvolatile memory chip stores analog voltages used for fine tuning.

The firm used to make Fairchild's F8 microprocessor but de-emphasized it when it did not go over that well in Japan. As might be expected, Sanyo builds a proprietary 4-bit controller and may go on to develop another 8-bit or a 16-bit processor. Actually, it claims to have come up with the world's first multichip 16-bit CPU more than nine years ago.

Sanyo is committed to GaAs and to CCD technology for discrete emitters and image sensors, respectively. It has developed both CCD and MOS interline-transfer image sensors.

Thinking that light-emitting diodes were the way to

11. Fun calculator. Making possible this vest-pocket-sized video game is LCD technology and a 4-bit microprocessor soon to emerge from Sharp. Of the C-MOS chip's 60 pins, 40 drive the display directly. The toy is sitting on part of the IC's die photo.

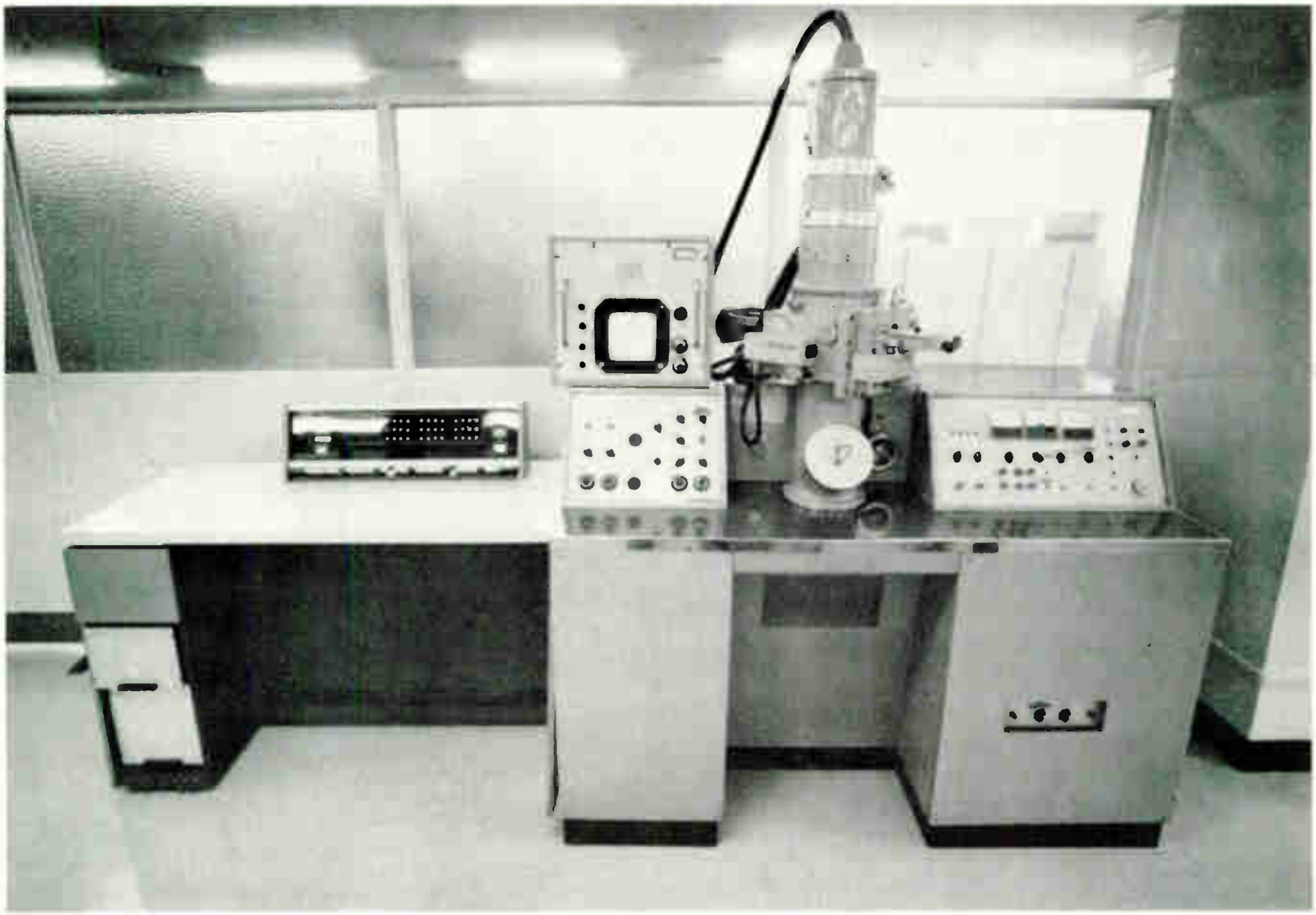
Sanyo will invest more than $40 million over the next four years for VLSI research. It says it built the first electron-beam exposure system.

go, the company has long concentrated on building a flat LED display for TV applications [*Electronics*, May 19, 1981, p. 105]. However, seeing the handwriting on the wall for LCD technology, it may now be shifting its focus in that direction. In any event, Sanyo's contribution to flat display technology has been and likely will be in the area of full-color reproduction. It has already developed a multicolored LED display panel and it has color LCDs going in the lab.

The missing link for its LED display is a blue emitter, but, says Hayashida, "we will have a blue LED by next year." Of three possible materials—silicon carbide, boron nitride, and zinc selenium—the last compound was chosen because "it can be grown on a GaAs substrate using selective epitaxy."

Besides semiconductors, Sanyo builds TV and audio equipment, microwave ovens, washing machines, and office automation products, though its computer business is small. Sanyo fulfills about 40% of its IC needs yet commands over 70% of the market for audio amplifier chips—it is the Japanese company that took control of

12. In the running. Tadashi Sasaki, senior executive director of Sharp's engineering center, says that high-resolution LCDs produce poor-quality pictures without a clever interlacing scheme. Sharp will be first with the right scheme, he says.



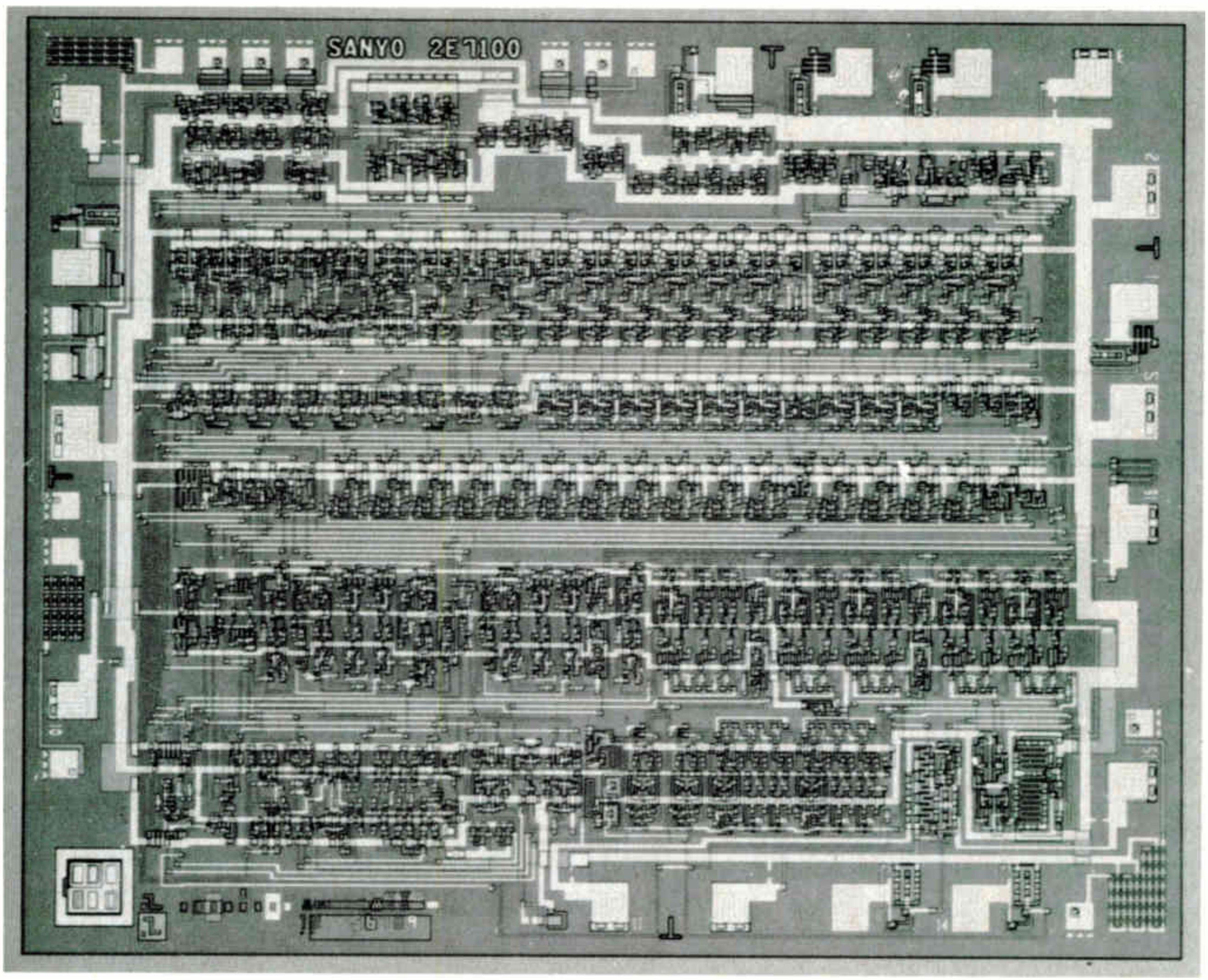
13. Antique. In the world of electronics, old can mean less than 20 years. This electron-beam wafer-exposure system, constructed by Sanyo in 1964, is said to be the first such machine in the world. Sanyo is still sold on electron-beam lithography.

the Fisher stereo company in the U. S.

Oki Electric Industry Co., too, will make the 8048 and 8049, but in C-MOS—like NEC and Toshiba. "We have essentially all processes in development, except for specialized stuff like SOS," says Tadao Higashi, general manager of Oki's Electron Devices Industries Group. "Until three to four years ago, our main purpose was internal supply, but now 80% of our semiconductors go toward outside sales," he adds. Oki's most recent thrusts into the U. S. market explain the sudden abundance of its 16-K n- and C-MOS static and 64-K dynamic RAMs (Fig. 15). It may one day tailor its 64-K RAM for different speed and/or power requirements.

Oki is 100 years old this year. The company lays claim as the first manufacturer of telecommunications equipment in Japan. It has expanded into three major divisions: one for telecommunications, one for computer systems and software, and one for electron devices and semiconductors. With 30,000 employees and worldwide manufacturing facilities, Oki has annual sales, including those of its affiliated companies, now approaching $1 billion.

Oki installed electron-beam lithography equipment in 1977, establishing automatic assembly and testing practices shortly thereafter. It recently committed $40 million to a new VLSI fabrication and assembly facility that



14. Thoroughly modern moly. Sanyo has become very handy in using molybdenum for gate electrodes in high-speed MOS circuits. This phase-locked-loop IC can divide fm local-oscillator frequencies directly and do so over a −40°-to-+85°C temperature range.

'Until about three or four years ago, our main purpose was internal supply,' Oki says. Now more than 80% of its semiconductor sales are external.

it expects will be functional later this year.

Oki started with C-MOS technology "early, in around 1967," recalls Higashi. "There was no specific need—we were just looking for low power." The company's production of C-MOS ICs increased markedly three to four years ago because of the boom in digital watches. "We now have 25% of the world market for C-MOS watch chips," he claims.

For camera and other applications, Oki uses a process that merges bipolar transistors with C-MOS (Bi-C-MOS). Higashi believes Oki was the first in Japan to do this. I^2L is used for circuits such as phase-locked–loop motor controllers, and ECL and low-power Schottky TTL for master slices, but only the chips made with its Bi-C-MOS or I^2L processes are sold externally.

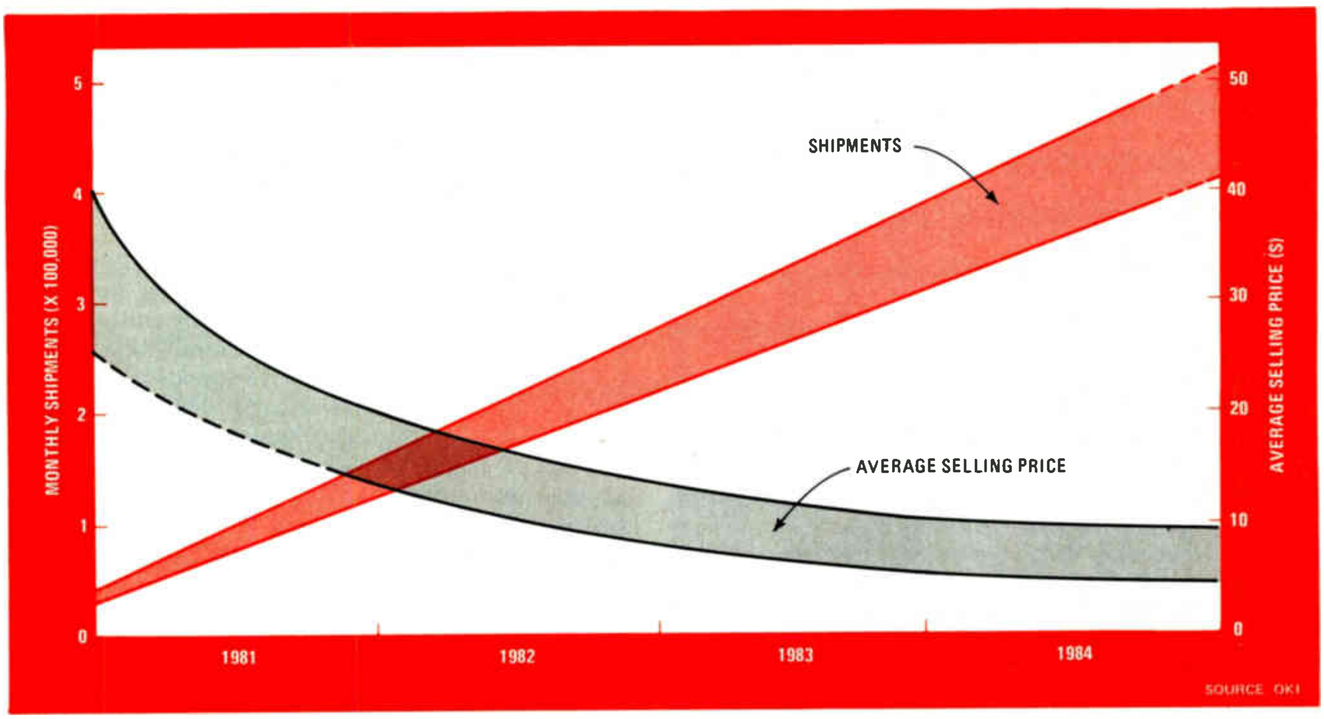
Oki will make fast static RAM and E-PROMs. Redundancy will be used in its 256-K dynamic and 64-K static RAMs, which may be made only in C-MOS. Oki prefers the six-transistor fully C-MOS cell "because the beauty of C-MOS is battery backup," says Higashi, adding that when it comes to C-MOS static RAMs, "I'm more afraid of NEC than Toshiba."

Sony Corp. does not sell its semiconductor components on the outside, but its processing achievements are nonetheless noteworthy. Its Semiconductor division manufactures MOS, bipolar, CCD, and discrete devices in Atsugi, Kanagawa, and Kyushu. The Atsugi plant, just west of Tokyo, employs 1,100 workers and 350 engineers, and the Kyushu plant is about half that size. Sony also builds hybrid circuits at a 220-person plant in Shinoishi, and its research center is located in Yokohama.

According to Teruaki Aoki, general manager of Sony's IC design department, the company uses five major bipolar processes for linear applications. These processes, which exhibit different speed and power characteristics, do not include ECL. Also, "we may be a little behind in MOS LSI," he says, "because 10 years ago we quit the calculator business." However, even though it pulled out of calculators, "we decided three years ago to concentrate on C-MOS," Aoki adds, and platinum silicide gates have since been developed to speed up its C-MOS.

One of Sony's strengths is in its crystallography. It is the company that figured out how to rub out defects in Czochralski-grown crystals by using a strong transverse magnetic field for Skylab-like semiconductors [*Electronics*, July 3, 1980, p. 83]. The field suppresses convection currents in the molten silicon and smoothes its surface, reducing the likelihood that oxygen atoms will enter the crucible and wind up in the ingot. The consequently sharp decrease in crystal defects cuts noise in circuits

15. Emerging. Oki's semiconductor production was once dedicated only to internal consumption. Lately, though, it has been turning its RAMs loose in the U. S. As this diagram illustrates, Oki expects to flood the market with inexpensive 64-K chips.



Japanese color CCD sensors are the world's most advanced. Sony alone has already designed four different versions.

16. Speaking for Sony. Sony does not sell its chips on the outside, but it has contributed much in the fields of crystallography and device passivation. Teruaki Aoki, general manager of its IC design department, says it is concentrating on C-MOS.

with low operating currents such as CCD image sensors, says Sony. Thus, it adds, TV cameras built with these chips produce images with fewer-than-usual white spots.

In fact, Sony is a leader in image sensors, too, having developed at least four MOS and CCD sensors for use in color cameras. Further, in January 1980, the company staked a claim to producing the world's first color CCD video camera. Developed for an entertainment system called Sky Vision and mounted beneath 747 jumbo jets, it affords passengers a bird's eye view of passing scenery [*Electronics*, Feb. 14, 1980, p. 79].

This pioneering camera uses three 111,192-element CCD imagers—fed through beam-splitters—in what Sony calls a spatial offsetting arrangement to double horizontal picture resolution. The interline-transfer CCDs used buried channels to optimize transfer efficiency and tin oxide electrodes to beef up the blue response five times over that possible with polysilicon electrodes.

This imager was preceded by three other color CCD chips. The first model was of the frame-transfer variety, with photosensors exposed to accept more light. It was followed by an improved design, using narrow-channel transfer gates, that enhanced the movement of the charge packets by allowing two-phase clocking. The new frame-transfer chip was employed in a prototype miniature cassette recorder for "video movies."

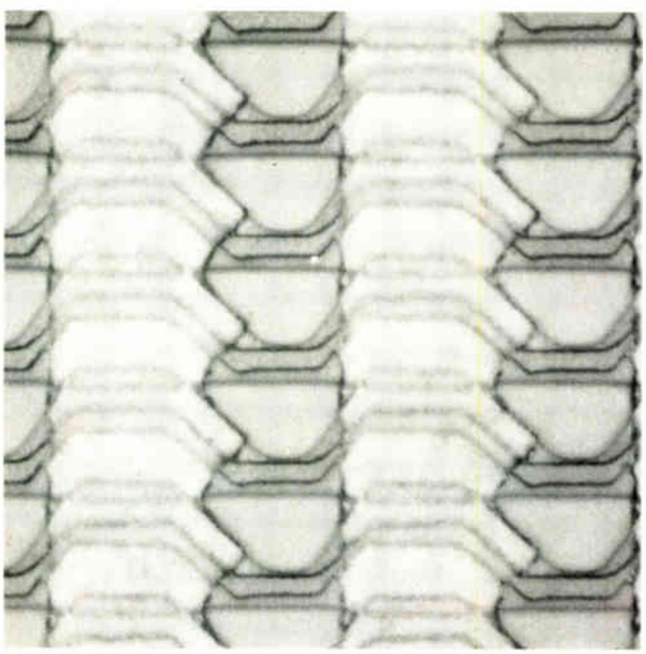
Sony's next color CCD image sensor utilized interline zigzag-transfer imagers featuring sensing sites in a checker pattern. This IC reduces the number of required picture elements by arranging two rows of photosensors along a single vertical sensing column. Signal processing was used to remove crosstalk between neighboring rows.

Sony can also be credited with a different method of passivating discrete and integrated circuits alike. The process, called Sipos, for semi-insulating polycrystalline silicon, is not to be confused with the NTT Musashino lab's Simox or Fipos or with Sipmos, for Siemens power MOS, given that name by the West German electronics giant that thought up the idea [*Electronics*, March 13, 1980, p. 92].

With conventional silicon dioxide passivation, be it thermally grown or poured on, electric charge or high fields on the top surface attract carriers on the bottom surface—at the oxide-substrate interface. These unwanted carriers leave transistors open to conductivity modulation and make it difficult to build high-voltage planar transistors and C-MOS ICs without resorting to so-called channel-stop implants.

When Sony's Sipos is used, however, contaminating ions drift into the passivating layer instead of forming an inversion layer or depletion region in transistor channels. The induced charges also travel up into the passivating layer, forming an electrostatic shield against a further invasion of surface charge. □

17. Here's looking at you. Sony's improved crystal-growing techniques help make its charge-coupled devices the finest for color TV applications. It says it introduced the first color CCD camera last year using three of these interline-transfer sensor chips.



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Circle 133 on reader service card

Chip set bestows virtual memory on 16-bit minis

Second-generation chips add support for coprocessors and multiprocessors as well

by Jan Beekmans,* Gerard Duynisveld,* Claude Fernandes, Leo de Groot,* Louis Quéré,* Frans Schiereck,* and Arjaen Vermeulen
Philips Data Systems, Apeldoorn, the Netherlands, and Fontenay-aux-Roses, France

☐ The application of state-of-the-art MOS and bipolar custom circuitry to computer systems is boosting performance and the number of functions at a phenomenal rate. To protect its edge in system and software know-how over semiconductor houses, Philips Data Systems began a custom large-scale integrated-circuit design effort several years ago. It had the first building blocks by 1979: a 16-bit microprocessor (the SP 16C/10) and two bipolar circuits—one for bus arbitration (the SP16C/12) and one to support the interrupt system (the SP 16C/11).

But though this first generation was powerful, programs have become larger, requiring more addressable memory. Multiprocessing for multiusers demands virtual memory management, as well as strong memory protection. All this has led to a second-generation 16-bit processor—the SP 16C/20 instruction execution unit—and the SP 16C/23 memory management unit. This set supports virtual memory, dynamic code changes, and multiprocessor protocols, plus coprocessors for decimal and floating-point operations.

In addition, the new generation's instruction capabilities allow swapping of virtual memory into available physical space but do not restrict the swapping to fixed-size segments. By allowing segments to be of varying lengths, an entire task can be kept together.

Implementation

The SP 16C/10 was designed to execute a basic, 120-instruction set (called the primary, or P, set) using real, or physical, addressing. It was realized in static, depletion-load enhancement-driver n-channel MOS technology, initially with 6-micrometer minimum features, but now with 4 μm. The design is housed in a 40-pin package; the clock frequency of the 4-μm device is 4 megahertz. In that version, the shortest instructions take less than 2 microseconds. The processor works with both synchronous and asynchronous input/output interfaces, supports direct-memory-access requests, and has a non-maskable interrupt input, along with four maskable ones. Its 16-bit data bus is multiplexed with the address bus. In its present version, the chip measures about 200 mils (5.1 millimeters) a side.

The addition of the virtual addressing scheme called for supporting an additional instruction class and led to a two-chip set for the new members of the computer family. Because the address translation is done in parallel with all instructions, it adds no appreciable delays to instruction execution. The block diagrams of the two new chips are shown in Figs. 1 and 2.

Complete compatibility

To preserve the vast investments of the last decade in system and application software, complete compatibility right down to the machine-code level is dictated. The best way to maintain compatibility and also add functions to an established computer line is to provide new instruction categories while incorporating more sophisticated address schemes, like support of virtual memory, into all instructions. Table 1 shows the four different instruction classes, including the two address schemes, along with the computer designed to execute them. All four classes are based on 16-bit-wide code and data.

Most of the 120 instructions in the P set have five different addressing modes: immediate, register, indirect, indexed, and indexed with indirection. Several data formats, including bits, bytes, words, and double words, are also supported. The set includes instructions like multiply and divide, 16 different shifts, and test and set or reset a bit, as well as 10 string-handling instructions that can move strings up to 64-K bytes long or search for a match with a specified character.

The D set acts on decimals up to 33 digits long and converts between the different formats currently in use for data processing. It comprises 22 instructions.

The F set covers floating-point instructions. Of the two addressing schemes—real and virtual—the real system is most widely used; here addresses directly indicate physical locations in main memory. Because the addresses are 16 bits wide in the real scheme and the smallest addressable unit is a byte, a 64-K-byte main memory can be addressed.

Virtual memory

In the virtual memory scheme, 32-bit addresses are handled in the program, whereas 24-bit physical addresses are computed. In this case, an extra instruction category, the V set, is added to support the wider addresses and the built-in protection mechanisms. Also, there are added instructions to support block-structured languages by implementing both a system stack, used for system parameters, and a user stack, for variables.

When instruction categories F and D are not being executed by hardware coprocessors, traps are generated to allow emulation of such instructions in software. There also are two privilege modes for instructions: system and user. Those instructions available only at the system privilege level control I/O operations, virtual memory management, and the system stack.

The segmented virtual memory management scheme

* Temporarily at Signetics Corp., Sunnyvale, Calif.

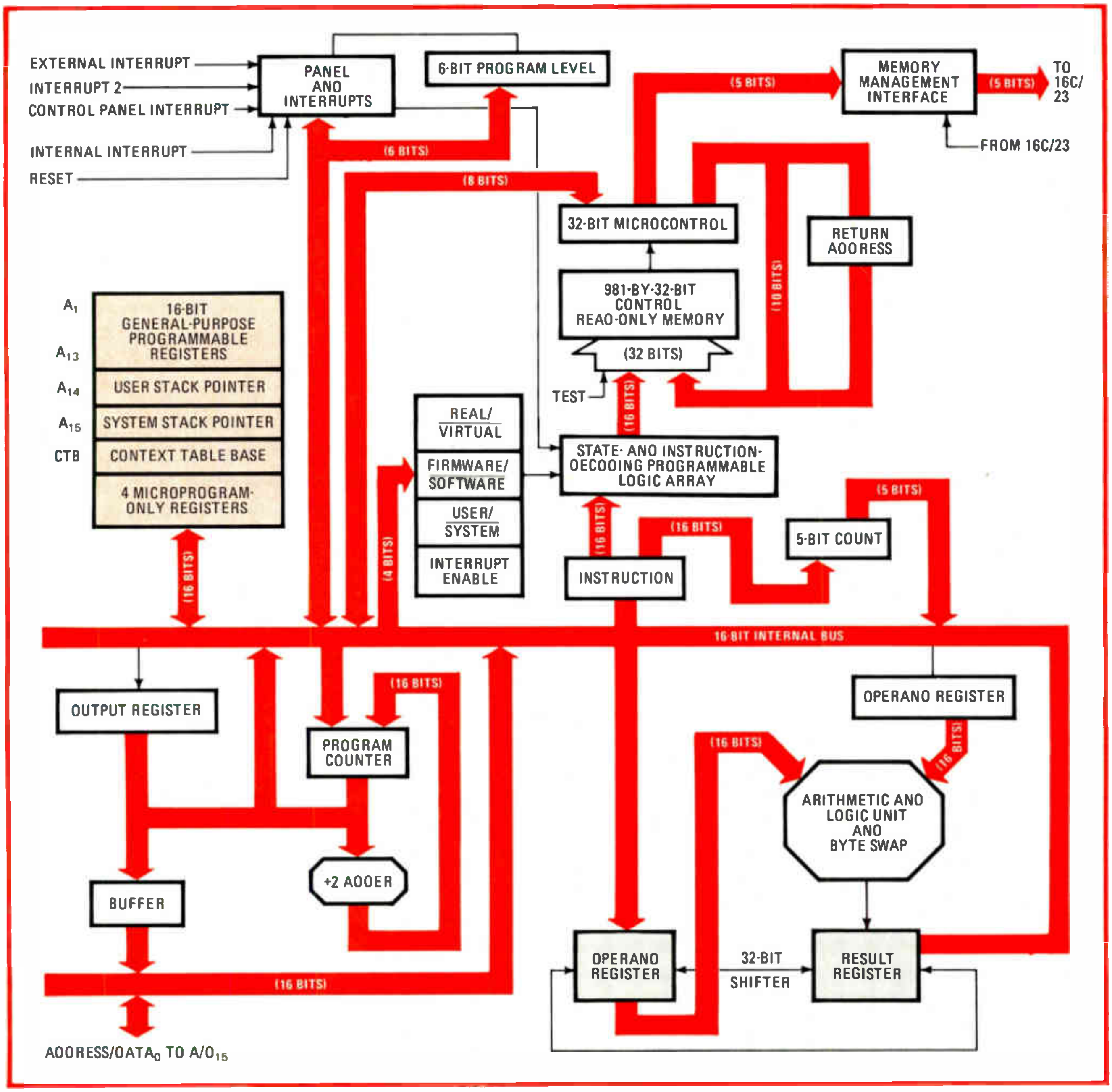
of Fig. 3 meets the requirement of upward compatibility with the existing computer line while serving the need for a well-protected memory space much larger than 64-K bytes. Simply enlarging the address space without any protection—making a linear address space of several megabytes—is inadequate for multiuser applications.

The address space

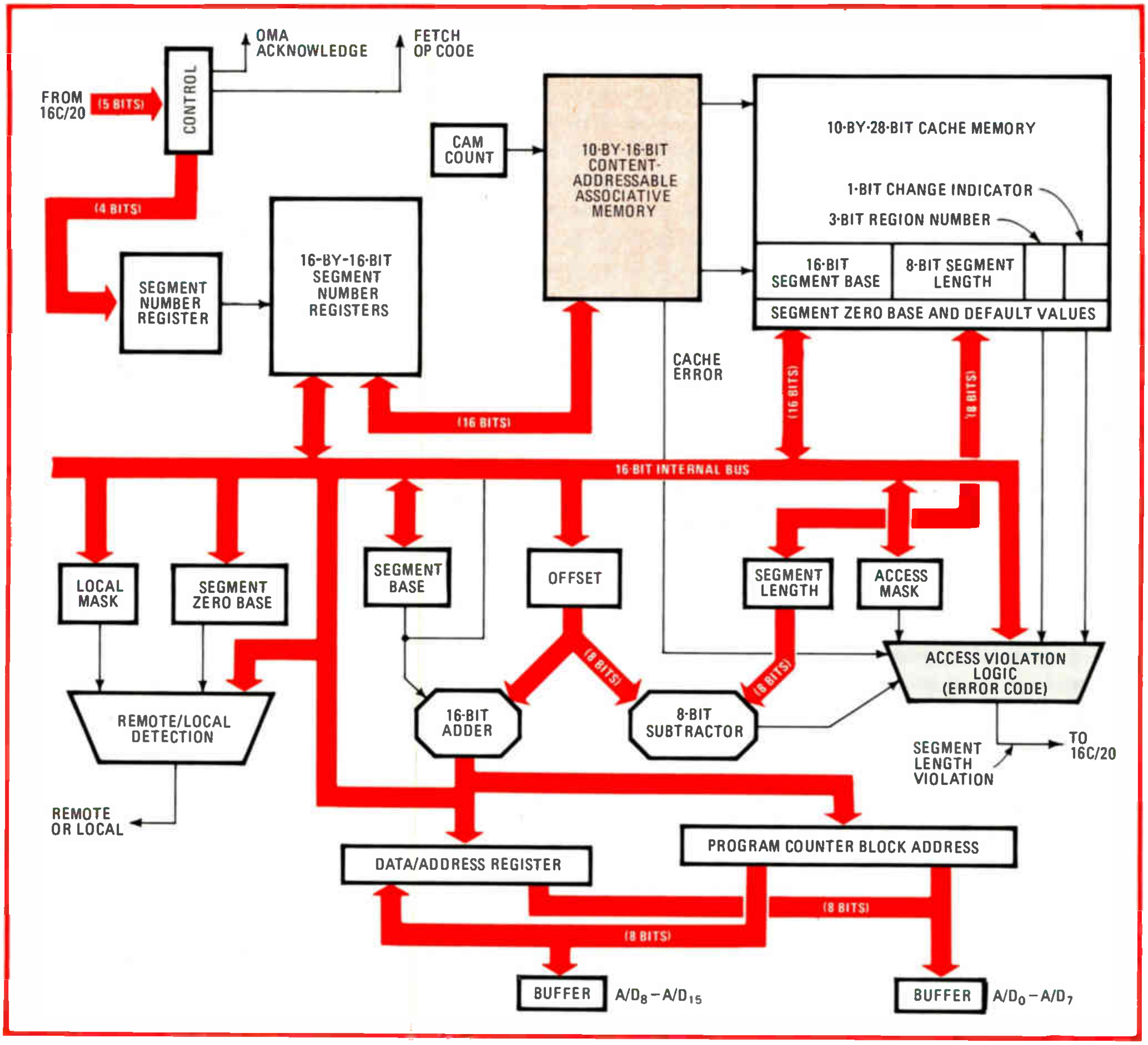
A virtual memory scheme with 32-bit addresses yields an address space of 4 gigabytes. The address space is divided into 65,536 segments, each ranging from a minimal 256 bytes to a maximal of 64-K bytes, allowing for convenient execution of older programs at the machine-code level by placing them in a single segment. Segments with flexible lengths are chosen over the simpler page-based systems—where every page has a fixed length—because variable-length segments can each hold a complete software task.

Upward compatibility with the real addressing mode is preserved by dividing the 32-bit address into two parts—a 16-bit segment number and a 16-bit displacement. These are treated separately so that there is no overflow into an adjacent segment, which could destroy another user's program. When a user reaches beyond the end of his current segment a flag is set that is checked by the microprogram very early in each instruction's execution cycle, preventing illegal accesses.

A segment number signifies an entry in both the system context table and the segment index table. The system context table indicates the locations of the vari-



1. Inside the processor. The SP 16C/20 contains all the standard modules of a central processing unit, plus an interface to the SP 16C/23 memory management unit. It is fully microprogrammed and makes use of a programmable logic array to decode instructions.



2. Virtual memory. A separate chip manages the virtual memory in parallel with the CPU's data calculations. The content-addressable memory and high-speed cache for descriptors keep protected address calculations from slowing down the processor.

ous parts of a user's program context. The segment index table holds the address of the segment descriptor, which in turn holds the address of the user's segment, as well as its length and protection status. These tables let users who by definition have different program contexts share the same segment without the need to copy it into different memory locations. The displacement and the first 16 bits of the segment descriptor (the segment base) form a 24-bit real address for the 16-megabyte on-line memory. The existence of segments is checked during the conversion through the tables, and the displacement is checked against the segment length. An abort trap is activated whenever one of those checks fails.

The protection scheme controls access to users' tasks being executed in the same virtual address space. Each task can be given different access rights to each individual segment (no access or read-only or read/write access). In addition, priority levels for tasks can either utilize 8 hierarchically organized task categories or 256 nonhierarchical ones.

A portion number is added on top of the segmented address scheme so as to group specific task segments. This scheme greatly eases the construction of the operating system's memory management function, which handles swapping between the 16-megabyte real address space (the on-line memory) and the 4-gigabyte virtual memory.

Not at home

Constructing a virtual memory space leads to requests for instructions or data that is not present in the on-line memory, causing a residence error. This type of error will occur frequently; depending on the execution speed of the instructions, the size of the on-line memory, and the regularity and size of the tasks, it will occur several times per second. Hence, a system must be able to

PHILIPS MINICOMPUTERS USING LARGE-SCALE INTEGRATED PROCESSORS								
Instruction classes supported	Using 16C/10 chip (real addressing only)				Using 16C/20 and 23 chips (real and virtual addressing)			
	P-853	P-858	P-400	*	*	*	*	*
Primary	✓	✓	✓	✓	✓	✓	✓	✓
Floating-point		✓		✓		✓		✓
Decimal			✓	✓			✓	✓
Virtual					✓	✓	✓	✓

*Proposed only

recover from it without intervention by the operator. Early in an instruction's microprogram decoding sequence, a check is run for this error to make an elegant restart possible in case it occurs. The procedure slightly complicates the microprogram but is preferable by far to checking at the moment a segment descriptor is loaded, because of the inherent software overhead and the possibility that between the loading of the descriptor and the execution of an instruction in that segment, interrupts might change the residency of segments. The checking also eliminates the need for redundant backup registers to save the previous state of the machine.

Both chips in the second-generation family have 40 pins and are implemented in a dense n-MOS process with 3.5-μm minimum features. Layout and initial fabrication were done at Signetics, and second sourcing is now being set up at Philips in Europe. The processor, like its predecessor, is about 200 mils (5.1 mm) on a side, and the memory management unit (MMU) about 160 mils (4.1 mm). Clock frequency ranges from 6 to 9 MHz for selected parts, giving instruction execution times of less than 700 nanoseconds for the shortest, most frequently used instructions at 6 MHz.

Similar interfaces

The microprogram size for the enhanced instruction set increased from 360 words of 32 bits in the case of the SP 16C/10 to nearly 1,000 words of 32 bits for the SP 16C/20, owing mainly to its virtual memory capability and the requirement that instructions be restartable in case of a residence error. Because processors are members of the same 16-bit computer family, the interfaces with the interrupt system and their buses remain functionally the same.

Translating the logical into the real addresses in the virtual scheme and their inherent checks would normally slow down the processor significantly. Implementing a cache memory on the SP 16C/23 for 11 segment descriptors has fully solved this performance disadvantage. The associate memory checks for valid addresses and loads new descriptors into the cache under microprogram control in order to preserve speed. One of the 11 segment descriptors is always the one used to execute the programs written in the real addressing scheme of the SP 16C/10.

The checks on access rights and segment length are done on the SP 16C/23 in parallel with instruction execution by the SP 16C/20. Thus the virtual memory scheme does not slow down the processor.

The more complex of the two, the SP 16C/20, has about 60,000 transistors, over half of which are used in the read-only memory and the programmable logic array structures. The microprocessor has an instruction prefetcher that also supports dynamic changes in the operation code. Although the capability to change the code slightly decreases the efficiency of the instruction prefetch, it can potentially allow the construction of very dense codes.

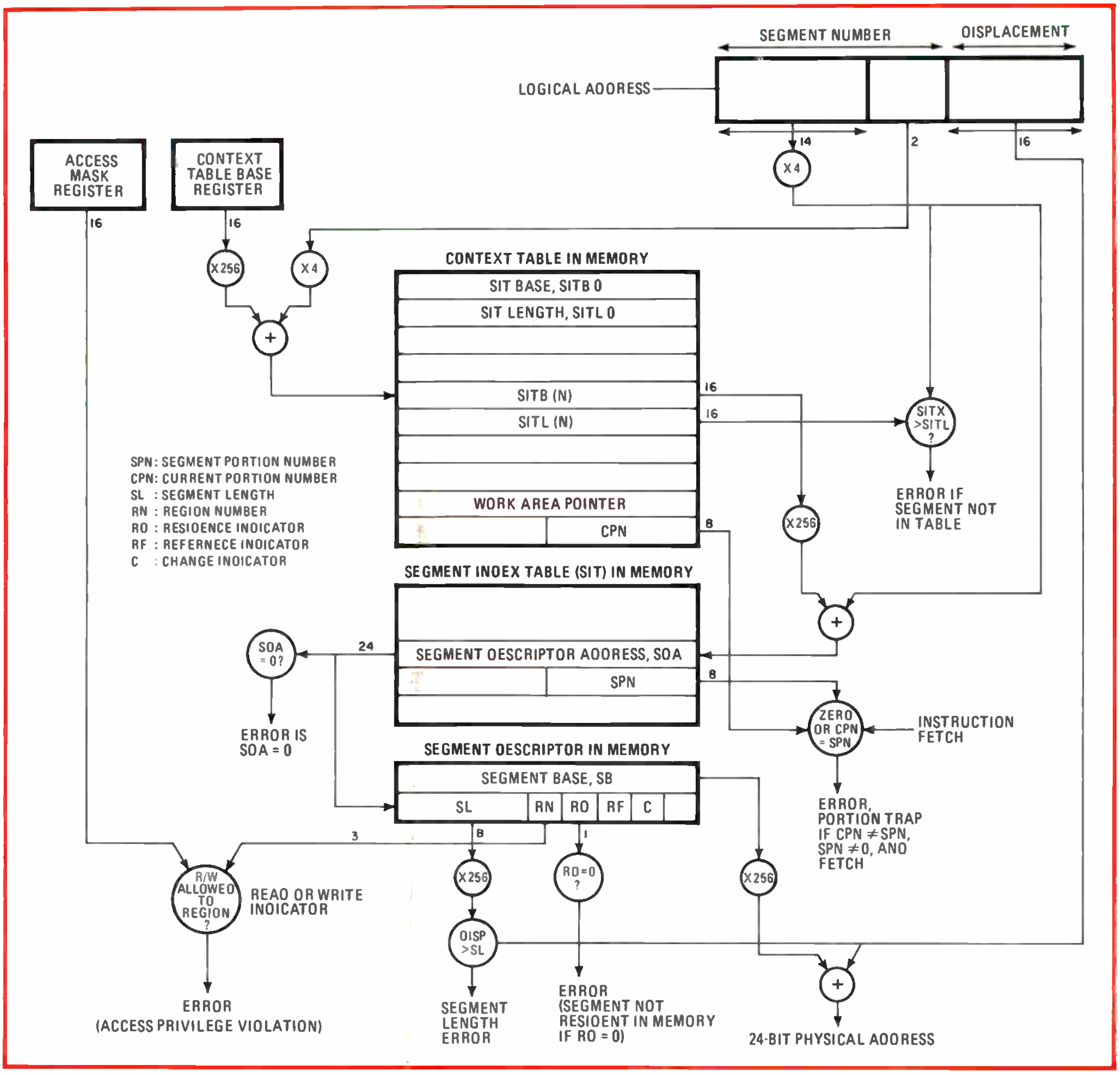
Coprocessors, too

Since the SP 16C/20 and 23 execute only the P and V instruction sets, the D and F sets have to be emulated in software. So that these sets may eventually be executed by separate processors, two interfaces have been microprogrammed into the SP 16C/20—one to pass a program context to a coprocessor, in case a decimal instruction is fetched, and one if a floating-point instruction occurs. The context is passed in less than 20 clock cycles, after which the coprocessor takes over the task, transmitting results and context back to the SP 16C/20 at its completion. The SP 16C/20 detects a coprocessor's presence on the fly, and either a context is passed or, in the absence of the dedicated processor, the emulation routine is started. Because the computer line is mainly for business applications, priority is given to the decimal coprocessor, which is now being microprogrammed.

The P instruction set enables the construction of semaphores for a multiprocessor system. In addition, the basic interrupt protocol of the SP 16C/11 can support such systems.

Multiple processors

With this foundation, a multiprocessor system built of identical processors is envisaged. Each processor is placed on a separate printed-circuit board of the Eurocard size, with a part of the general-purpose memory on board. All these distributed memory chunks make up the total on-line memory. Whereas the local memory is addressed synchronously, the second category employs an asynchronous handshake to allow time for other processors to get off the bus and to support the use of memories having a wide variety of access times. To make this memory organization transparent to the system software, the SP 16C/20 and 23 have extra logic to take the



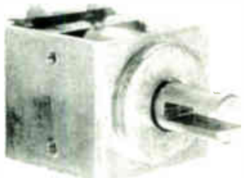
3. Logical to physical. The conversion of 32-bit virtual addresses into 24-bit real addresses is done in two steps. The logical address is used to locate the segment index table entry from the context table, and that entry in turn indicates the location of the segment descriptor.

memory partitioning into account. The idea is to have the processors accessing as much as possible their local (on-board) memory at full speed by a synchronous interface and to minimize the references to remote memory over the slower asynchronous system bus.

At the system level, the processor (or processors, in the case of a multiprocessor system), the on-line memory, and the I/O control units are connected by a system bus, which has as a physical form factor a 96-pin Euroconnector. A 28-pin bipolar device, the SP 16C/12, is designed to permit a bus master device—such as a central processing unit or direct-memory-access control unit—to request and gain control of the common system bus. The SP 16C/12 lets a bus master in a multimaster system communicate with other masters, as well as transfer data to common memory and I/O devices. The chip is about 160 mils (4.1 mm) on a side and allows modular expansion to any number of bus masters. To maximize throughput, the bus allocation runs in parallel with the other functions on the chip.

To support an interrupt system with as many as 63 different interrupt levels, the SP 16C/11 was designed. It is realized in bipolar technology, measures about 170 mils (4.3 mm) on a side, and is housed in a 22-pin package.

The bus interface of the SP 16C/11 comprises only two lines: a clock for the interrupt system and one for the encoded interrupt information. This concept has many features in common with the interrupt structure of the proposed P-896 bus interface standard that the Institute of Electrical and Electronics Engineers is working on for modern 16- and 32-bit multiprocessor systems. □



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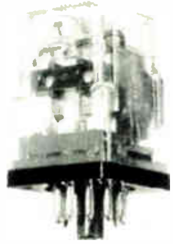

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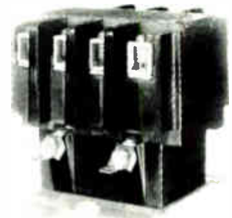

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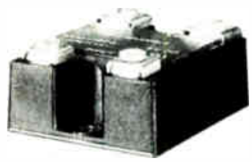

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Fm receiver mixes high gain with low power

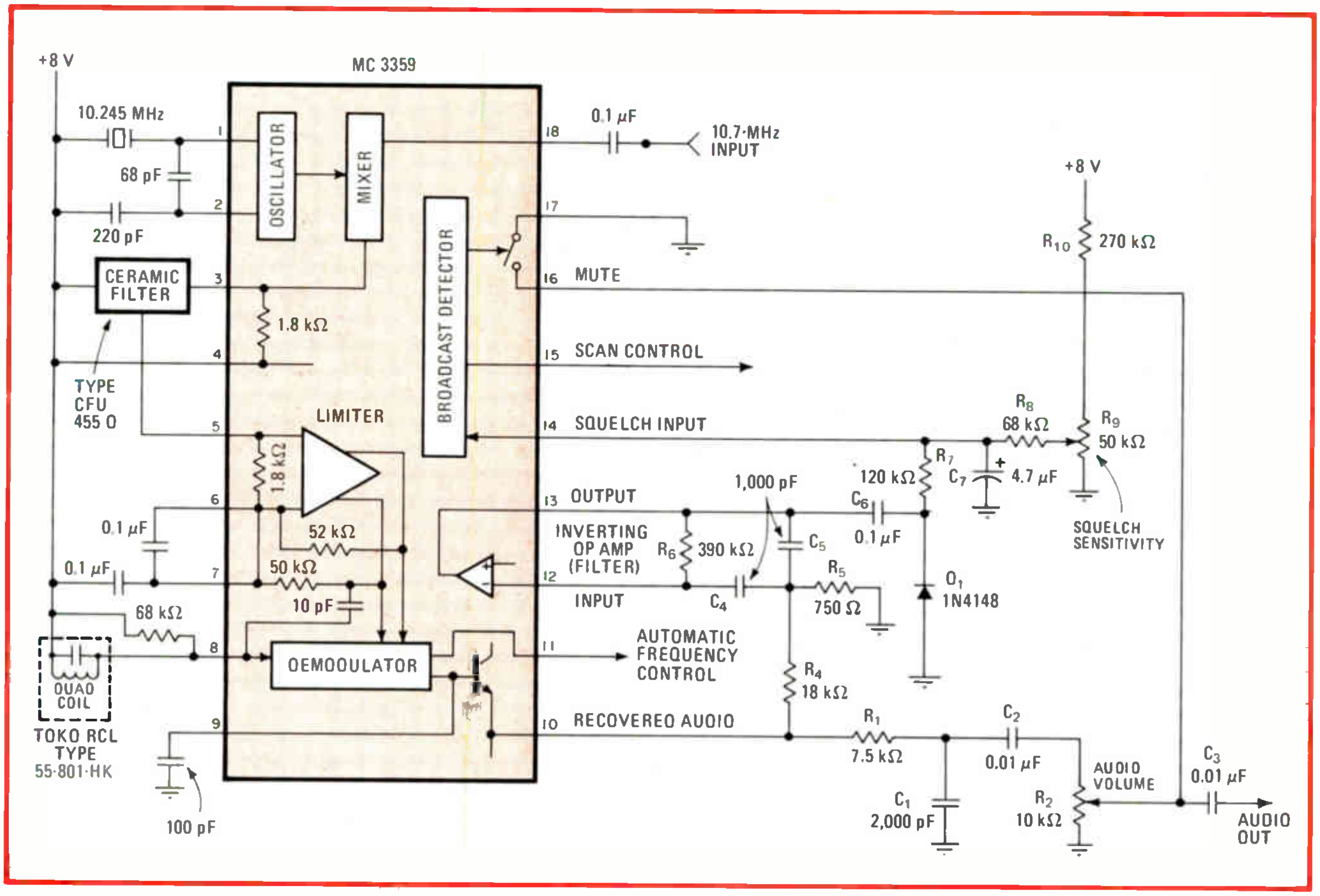
by Peter Whatley
Motorola Inc., Phoenix, Ariz.

Scanning receivers, ham transceivers, and other narrow-band frequency-modulated systems that receive voice or digital information need as much gain as they can get to pick up weak signals. Normally such gain is expensive. But the Motorola MC3359P chip, which has an oscillator-mixer, limiting amplifier, quadrature discriminator, operational amplifier, squelch, scan control, automatic frequency control, and mute switch neatly combines low cost, high gain, and as a bonus, low power consumption. It requires only a front-end tuner and a few other components to form a complete narrow-band scanning receiver (see figure).

A typical application of the MC3359P is as a narrow-band fm scanning receiver for voice communication. As shown, the input to pin 18 (typically 10.7 megahertz) is converted down by a mixer-oscillator combination to 455 kilohertz, and most of the amplification is done by the chip at this frequency. The mixer is doubly balanced to reduce the fm receiver's spurious responses. Its output at pin 3 has a 1.8-kilohm impedance to match an external ceramic filter. For its part, the oscillator is a Colpitts design that can readily be controlled by a crystal.

After limiting, the fm signal is demodulated using a quadrature detector. The recovered audio is filtered through R_1 and C_1 to remove noise and is then coupled via C_2 to a volume control. The recovered audio is 800 millivolts peak to peak at the junction of R_2 and C_2. The unfiltered recovered audio at pin 10 is fed through R_4 to an internal inverting operational amplifier that, with R_5, C_4, C_5, and R_6, forms an active bandpass filter in the 6-kHz range. Therefore any noise or tone frequency, which may be present above the normal audio range, can be selected, amplified, and then detected by the C_6 and D_1 combination. This detected signal is, in turn, sent to the squelch control at pin 14. Squelch sensitivity may be adjusted by R_9, which provides a bias to the squelch input.

If pin 14 is raised to 0.7 volt by the detected noise, tone, or dc bias, the squelch detector will be activated.



Narrow band. In the scanning-receiver circuit shown, the MC3359P provides an audio output voltage of 800 mV peak to peak. Current drain from a 6-V supply is 3 mA, and the sensitivity is 2 µV for −3 dB of input limiting. Only one crystal and some passive components are needed.

This causes pin 15 to act as an open circuit and pin 16 to be shorted to ground via pin 17. Pin 16 is thus connected to the input of the audio amplifier and mutes the audio signal during squelching. Pin 15 can be used for scan control and may be connected to a frequency synthesizer in the receiver's front end. An afc connection is also available at pin 11. In this crystal-controlled application, an afc is not required, so that pin 11 can be grounded or tied to pin 9. With this last connection, the recovered audio is doubled in amplitude. □

Deglitcher–delay circuit serves also as pulse generator

by B. Seastrom and G. Goodwin
Sylvania Systems Group, GTE Products Corp., Needham Heights, Mass.

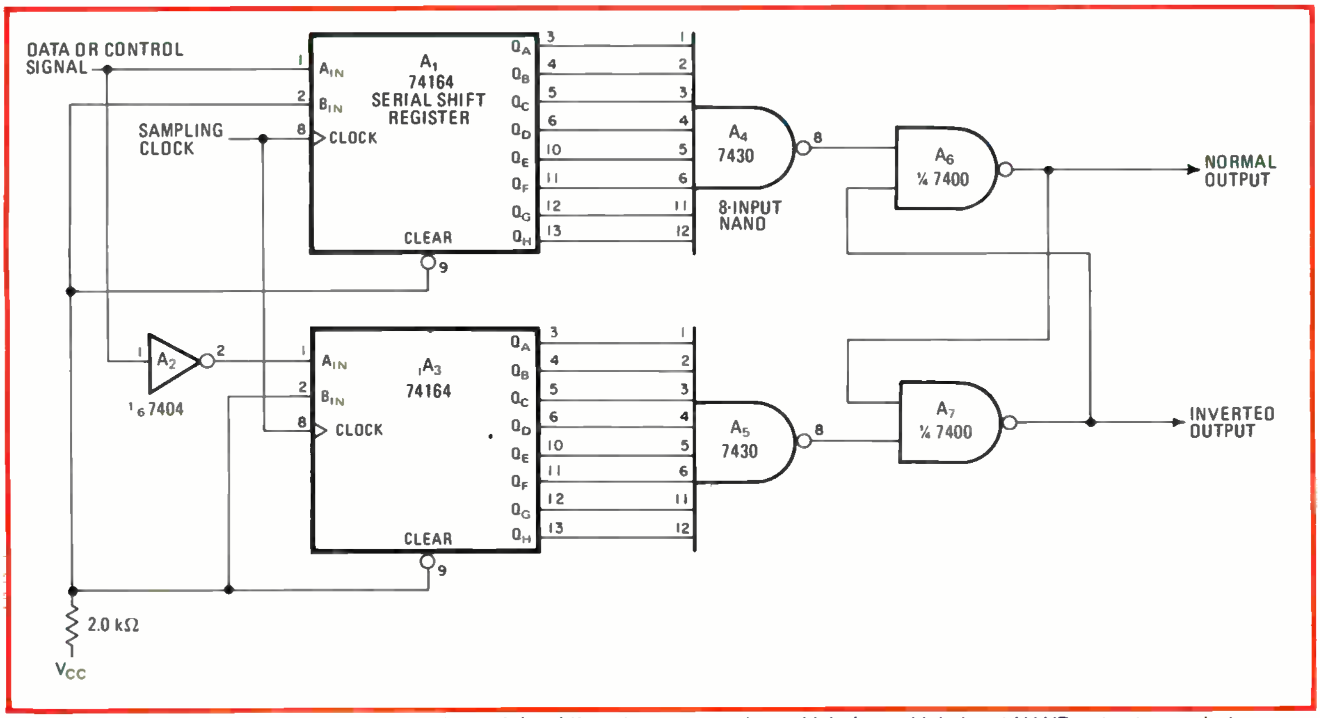
Sustaining its input pulse for a number of clock cycles before translating it into an output pulse, this circuit provides an effective means of discriminating between valid data and spurious pulses or glitches. The designer who uses the circuit has numerous options for adjusting the delay between the input and output transitions, as well as controlling the duration of the output pulse. Furthermore, it triggers on either a rising or a falling edge and generates complementary outputs.

Data entering serial shift register A_1 is sampled at the clock rate and shifted along from output Q_A to Q_H. Meanwhile, for the complement of the input at the output of A_2, the same process occurs at the shift register A_3. Since all 1s are required at gates A_4 or A_5 to toggle cross-coupled NAND gates A_6 and A_7, there is a delay in the leading edge of the output, as well as in the pulse duration. The delay and the pulse duration depend on how many and which taps are connected from the shift registers to the eight-input NAND gates.

It is apparent that noise—in fact, any changes in input level—will be subject to successive samples, whose number is equal to the tap count, before it results in a change in output. By employing different numbers of taps on registers A_1 and A_3, the criterion will be different for different polarity edges—A_1 controls the positive edges and A_3 controls the negative ones—and therefore the circuit is highly noise-resistant. Further, by starting with a tap other than Q_A, initial edge delays can be built in, again selectively for either positive or negative edges.

A version of the circuit allows it to modify the input pulse width. Feeding selected output taps of A_1 into A_5 (eliminating inverter A_2 and serial register A_3) controls the time at which the trailing edge of the output pulse occurs. By judiciously choosing which taps go to A_4 and which go to A_5, the designer can exercise control over the width of the output pulse.

The circuits' applications are enhanced by expanding on the basic concepts. Thus, smaller NAND gates may be used with fewer samples, and expanded gates may be used with more shift registers in tandem. Finally, additional timing signals may be generated by connecting additional sets of gates to the shift registers. □



Tap dance. By changing the quantity and position of the shift register outputs into which the multiple-input NAND gates tap, a designer can mask unwanted spikes, as well as exercise a wide range of control over the output pulse width and rising and falling pulse edges.

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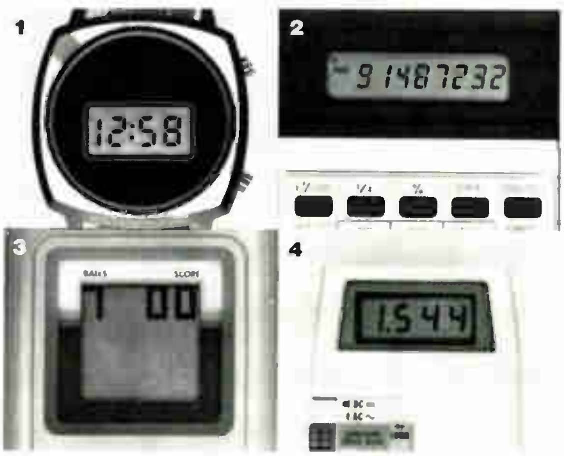

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Agc prevents noise build-up in voice-operated mike

by Russell S. Thynes
Kirkland, Wash.

Hands-free operation of intercoms has several advantages over push-to-talk intercom systems. Constantly keyed "live" microphones, however, have the disadvantage of receiving undesirable environmental noise in the absence of speech. When such mikes are used in conjunction with intercoms having automatic gain control in the microphone mixing stages, this environmental noise will produce a swelling tide of sound each time normal communication is interrupted.

Shown here is an agc-VOX (voice-operated switch) scheme that allows constantly keyed microphones to be used in noisy environments without suffering from the effects of noise build-up.

Although the operation of the circuit is twofold, the function is primarily that of a gain-clamped agc circuit. Part (a) of the figure shows the transfer function of an agc with gain clamping and that of typical configuration. For input levels below those of normal speech, clamping the gain to a fixed value limits the area of the gain curve, reducing noise susceptibility—but without placing restrictions on the dynamic range of the agc itself.

The circuit is shown on the right (b). The agc section consists of operational amplifier A_1 and transistor Q_1, with diode D_1 and capacitor C_1 deriving the feedback control voltage. Q_1 is placed in a T configuration to achieve a wide control range and to ensure low levels of distortion. Distortion is further reduced by the gate-biasing resistors R_6 and R_7. As configured, this agc should provide 30 decibels of gain control with less than 0.5% distortion for most of the audio range.

A_3 is arranged as an adjustable noninverting amplifier, the gain of which can be varied from 20 to 40 dB. R_{12} (also in a T configuration) allows the user to set the VOX sensitivity to offset environmental noise conditions. A_4 simply compares the detected output of A_3 with a reference and switches to either a high or a low output limit depending on the VOX input level.

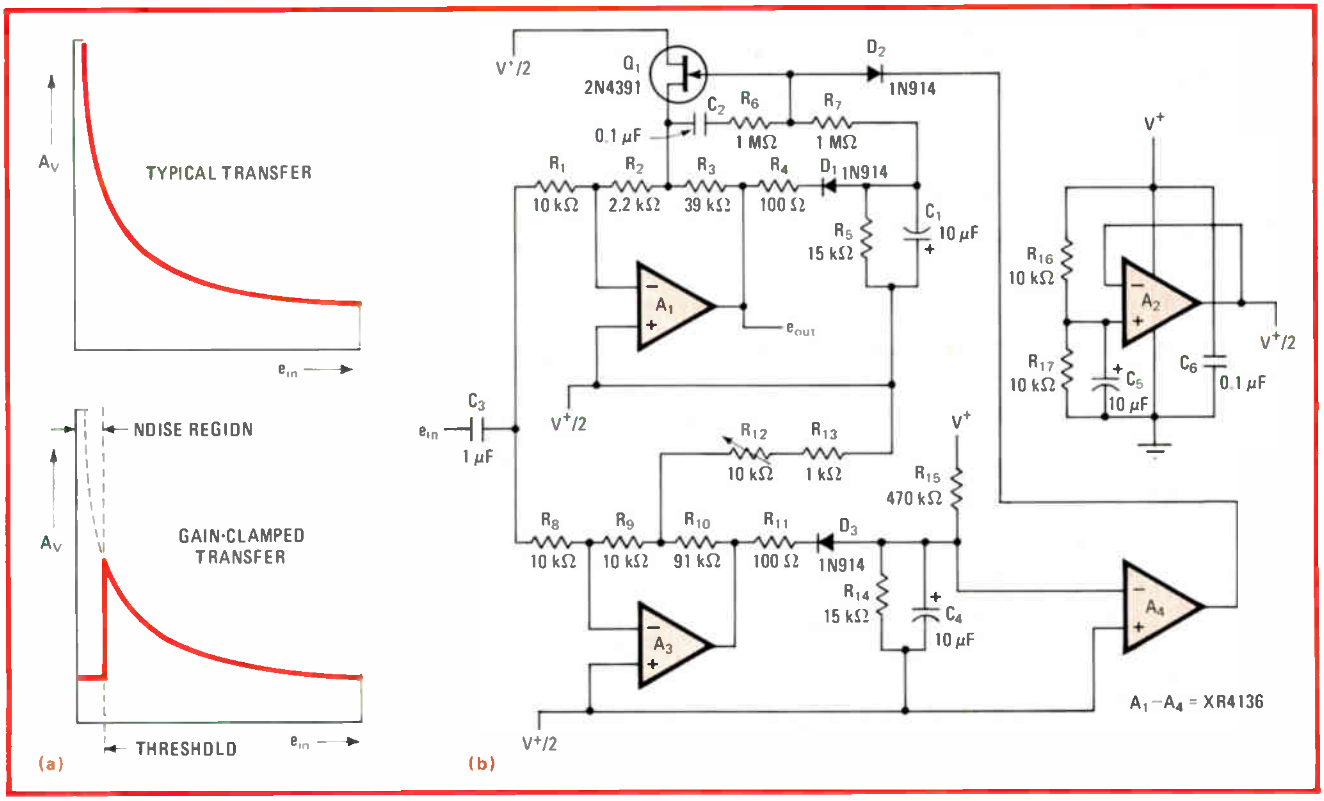
When input levels to the agc are below the VOX sensitivity setting, the output of A_4 will be at its lower limit, biasing Q_1 off and thus clamping the gain of A_1 to $(R_2+R_3)/R_1$.

When the VOX sensitivity level is exceeded, however, the comparator output swings to its upper limit and effectively disconnects the VOX from the agc feedback loop through blocking diode D_2. The gain is then expressed as:

$$-\frac{R_2+R_3}{R_1} \leq A_v \leq -\left(\frac{R_2+R_3}{R_1} - \frac{R_2R_3}{R_{on}R_1}\right)$$

where R_{on} is the practical on-resistance of the transistor.

This entire circuit can be configured using one quad op amp (such as an XR 4136) and requires no special considerations other than attention to the basic rules of grounding and supply bypassing. □



Hands off. If the gain is clamped to a minimum at input signal levels below the noise threshold, the surrounding noise is filtered out of the amplifier network (a), whereas speech kicks in the amplifier's automatic gain control. Both functions are performed by the circuit shown in (b).

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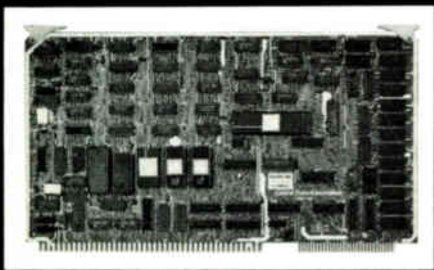

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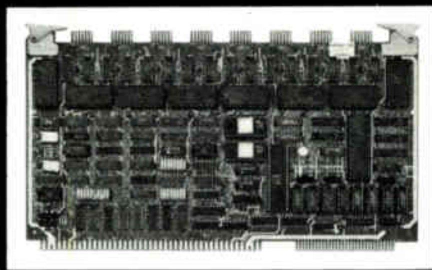

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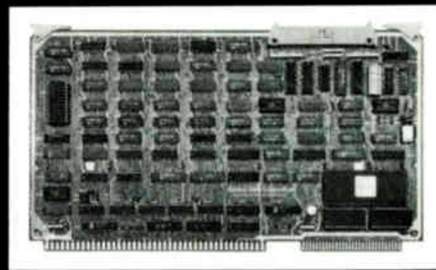

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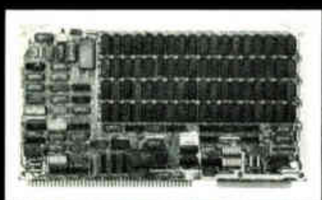

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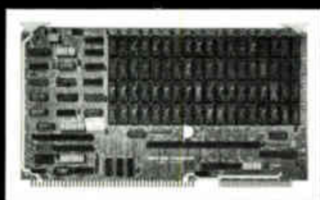

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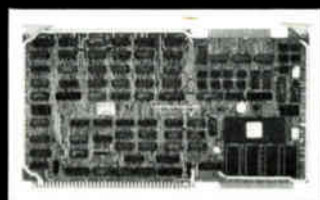

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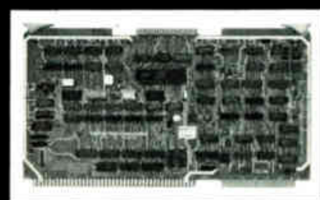

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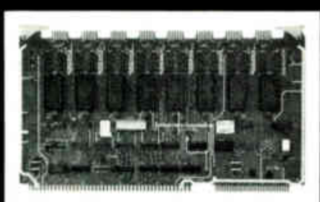

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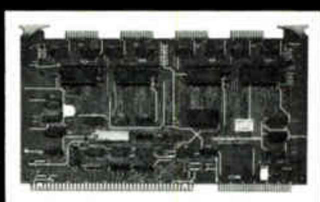

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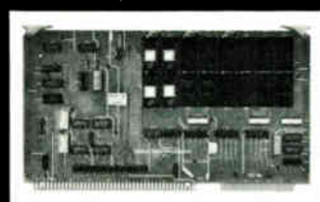

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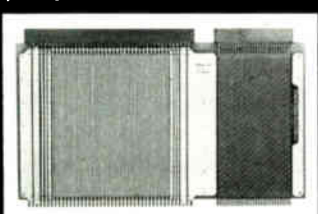

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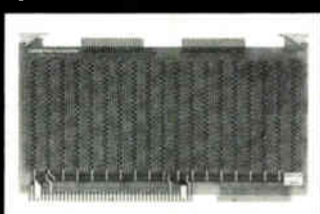

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Circle 144 on reader service card

Test strategies find faults in users' bubble memories

Various levels of incoming testing detect material defects, improper magnetic biasing, or poor timing control

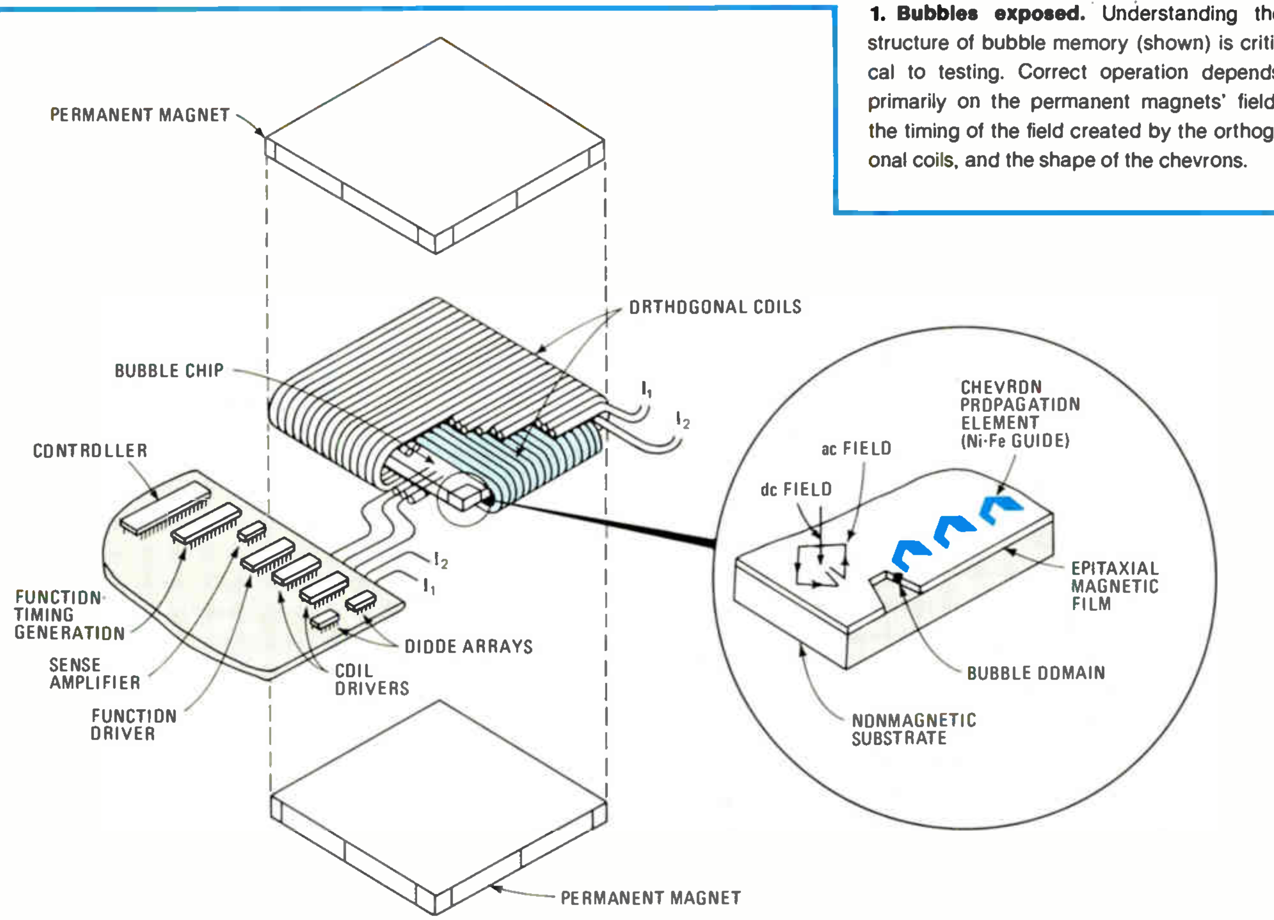
by Don Harmon, *Texas Instruments Inc., Dallas, Texas*

☐ As magnetic-bubble memories and their controlling circuitry become more readily available, many designers are beginning to consider them as a relatively inexpensive form of nonvolatile storage. Even though each device is tested by its manufacturer, the user will probably want to test the device as well before incorporating it into other products.

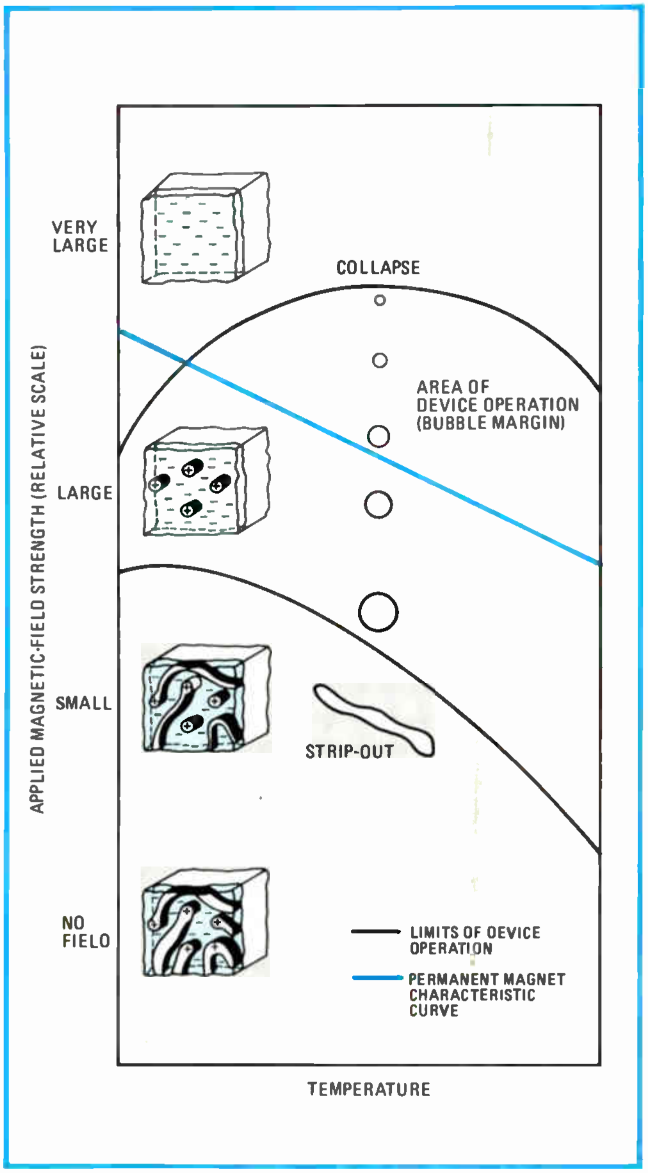
Testing bubble memories can be as simple or as complex a task as the user wishes. But before undertaking any test procedures, users must understand both the way in which the device functions and the ways in which it can fail.

As shown in Fig. 1, a bubble memory device consists of a bubble memory chip, two mutually perpendicular coils, and two permanent magnets. Not shown but enclosing these elements is a shield that protects the chip from interference by external magnetic fields.

The two permanent magnets included in the bubble device supply the biasing field that keeps the magnetic domains, or bubbles (each of which represents 1 bit), on the chip formed even when the device is not powered up, making possible nonvolatile storage. Since the field strength of the magnets depends on temperature, as shown in Fig. 2, they are chosen so that their temperature-field characteristics match those of the epitaxial film in which the bubbles reside. If the field becomes too



1. Bubbles exposed. Understanding the structure of bubble memory (shown) is critical to testing. Correct operation depends primarily on the permanent magnets' field, the timing of the field created by the orthogonal coils, and the shape of the chevrons.



2. Operating margin. The sensitivity of the epitaxial film in which the bubbles reside to field strength and temperature determines the region of proper device operation. The characteristics of the bias magnets (colored line) must be chosen to match this sensitivity.

great, all the domains in the film will line up with the field and the bubbles will collapse. If the field becomes too weak, the domains will take on the serpentine appearance more characteristic of the natural state and the bubbles are said to strip out.

The actual generation, propagation, transfer, and replication of bubbles that are needed for storing and retrieving data in a bubble memory are controlled by two layers deposited above the epitaxial film. One, an aluminum-copper layer, is patterned to form function elements that produce localized magnetic fields when pulsed with a current of the correct duration and amplitude. These fields aid or oppose the external bias created by the magnets and thus generate, swap, or cut the magnetic bubbles in the film.

The other layer consists of Permalloy metal patterns, usually referred to as chevrons, that are deposited on an oxide layer above the aluminum-copper patterns. When the rotating magnetic field created by the two mutually perpendicular coils magnetizes these chevrons, they cause the magnetic bubbles to propagate from one chevron to the next.

Two basic architectures—the major-minor loop and the block-replicate—are most widely employed in bubble devices, and in each type signal timing is critical to proper operation. In the major-minor loop scheme, data to be stored is generated within a single major loop and then transferred to many minor loops for actual storage.

A matter of timing

Transfer of the bubbles from one loop to another is accomplished by specially shaped propagation elements in the Permalloy pattern working in conjunction with the aluminum-copper control element. At the proper time, a current pulse flowing through the control element causes a localized alteration in the magnetic field so that the bubble is attracted from the chevron in the major loop to a chevron in the minor loop. By changing the timing of the current pulse, bubbles can be transferred out of the minor loops into the major loops so that the stored data can be accessed.

In bubble memories using the block-replicate approach, data is generated in an input track, swapped into the minor loops for storage, and then read back by replicating the blocks of data onto a separate output track for detection. The major difference between these architectures lies in the shape of the transfer element that causes the bubble to be split in two or simply replicated to effect the transfer.

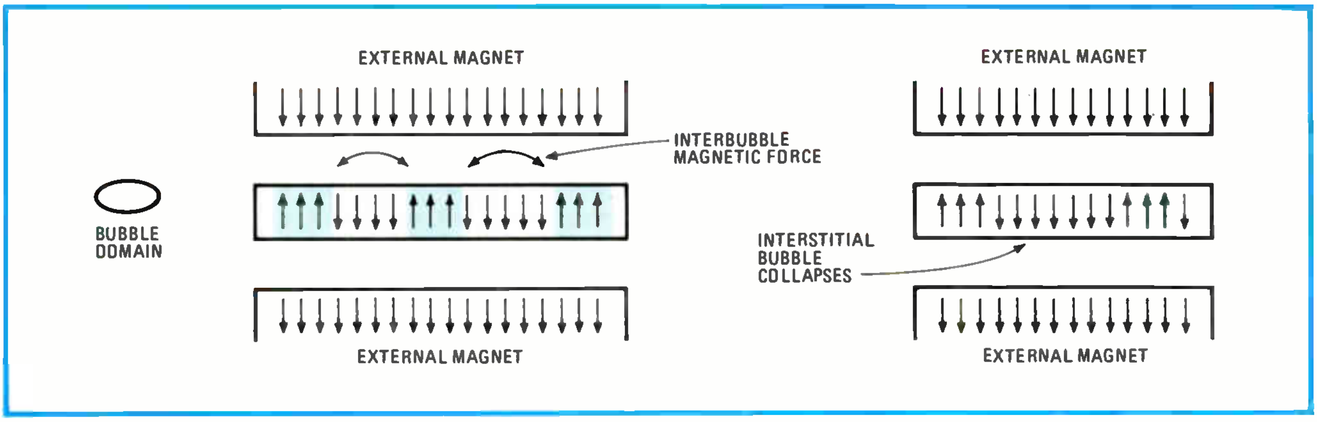
Although bubble generation, transfer, and replication are normal operations in a magnetic-bubble memory, these events can occur in an unwanted fashion because of defects in the device. The anomalies of bubble memory function that cause device failure are of four major types: bubble collapse, strip-out, self-generation, and self-replication.

As already indicated, collapse and strip-out result from the local field strength being too high or too low, respectively. Self-generation and self-replication of bubbles can be caused by a number of factors, including improperly shaped propagation elements, spurious dots of Permalloy material deposited between the minor loops, or incorrect setting of magnetic-field strength.

Magnetic-bubble memories may be tested by accelerating these various types of failure. This is accomplished primarily by filling all the data positions in the major and minor loops with bubbles or by using other data patterns that make failures more apparent.

Fatal attraction

The magnetic nature of the device and the interaction between bubbles during operation make the device more sensitive to the density and distribution of the bubbles than the actual pattern used. Each bubble generated both opposes the external magnetic field and exerts a force on adjacent bubbles. This situation is similar to that of three bar magnets placed parallel to each other. If the field strength is great enough, the magnet in the middle will turn around, reversing its polarity so that the



3. Dueling bubbles. If the magnetic field imposed on the bubble chip is too high, the magnetic interaction between the three bubbles shown can cause the polarity of the middle bubble to reverse. The bubble will then collapse, or cease to exist, destroying the data it represents.

opposite poles of the magnet, which attract one another, will then be adjacent.

The same phenomenon occurs in the epitaxial film of a magnetic-bubble device. If the field strength of the permanent magnets is set too high, the interaction between bubbles on a fully loaded device can cause an interjacent bubble to reverse polarity, or collapse, as shown in Fig. 3.

Bubble collapse can also be caused by an improperly formed propagation element or spurious Permalloy material deposited within or around the propagation loop. The defective element can cause a bubble to hang, or delay movement, long enough to let another bubble come close enough that one of them will collapse. In other cases, the localized magnetic field caused by a defective element could be strong enough to collapse the bubble on its own.

The worst-case test for bubble collapse consists simply of writing logic 1s in all bit positions in the device. This exercise checks whether the permanent magnets have been set too high in the bubble layer's margin of operation, whether the magnets will track the operation over the specified temperature range, and whether any improperly formed elements are causing bubble collapse.

Defective propagation

Bubble strip-out occurs when the field strength of the permanent magnets is too weak to prevent the bubbles from expanding and reverting to serpentine domains. It can also be caused by defective propagating elements that affect the strength of the permanent magnetic field.

The testing procedure for strip-out differs from that used for ascertaining bubble collapse in the nature of the data pattern used. For worst-case analysis of a device in which the magnetic-field strength may be set too low, the pattern has a few widely separated bubbles distributed over all the operating loops. If a bubble strips out under these conditions, then data will appear in bit positions other than those in which data was entered. This test can determine not only if the field strength is set too low, but also if there are any incorrectly formed chevrons causing the bubbles to strip out.

Self-generation is the spontaneous formation of unwanted bubbles within a device—a condition usually aggravated by high drive-field strengths at higher temperatures within the devices's operating range. To determine whether self-generation is occurring in any loops, a pattern of all logic 0s is written into every data position in the device. Then, the bubble memory is read several times to make sure that no bubbles appear. If the output data has any logic 1s in it, self-generation is occurring somewhere in the chip.

Self-replication of bubbles is usually caused by improperly formed elements. As shown in Fig. 4, self-replication can be either vertical (within the same loop) or horizontal (loop to loop).

These failures may be detected by writing several pages of 1s followed by several pages of 0s. Vertical replication will cause bubbles to appear in data pages that should have been empty. This test also determines whether there is a defect in a loop that will cause the last bubble in a string to drop back into the loop because of magnetic interaction between bubbles.

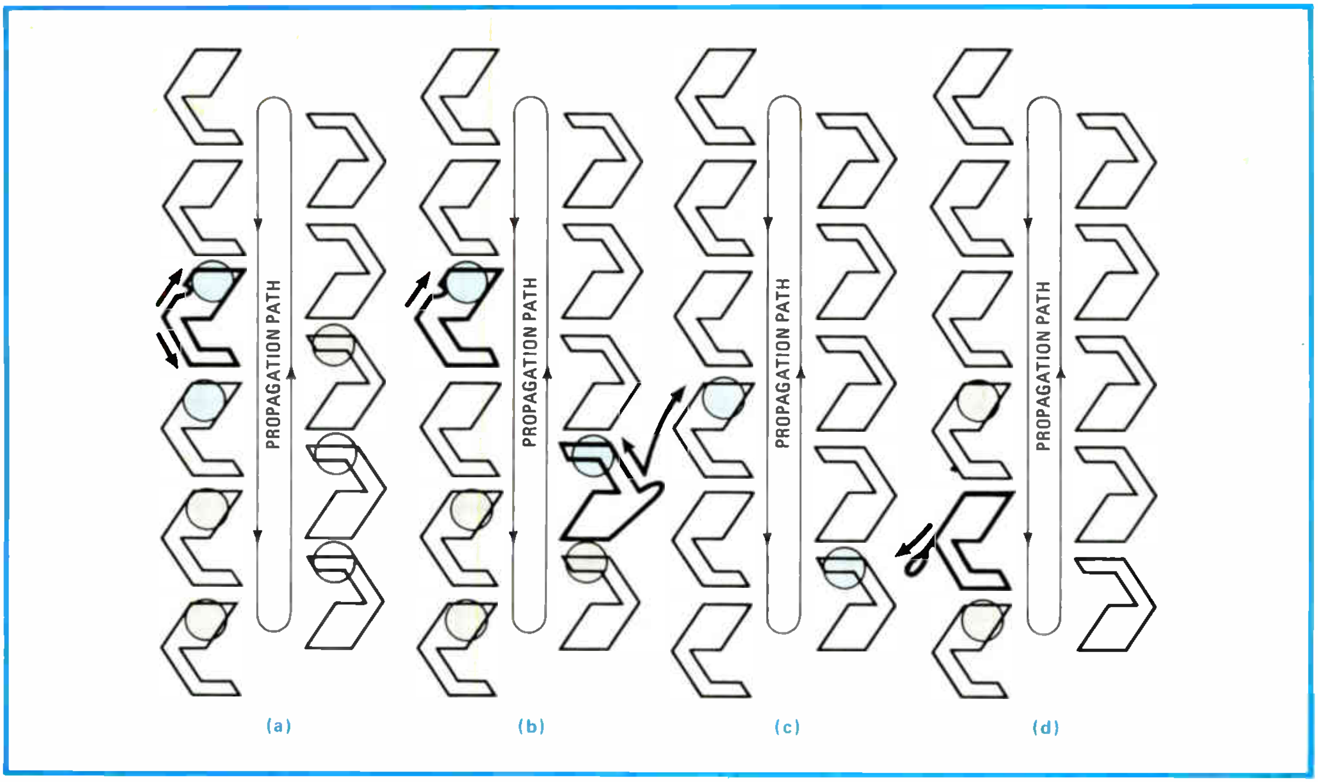
Figure 4a shows a notch in one of the chevrons on the left side of the loop. The magnetic polarities produced in this chevron and the interaction between bubbles may cause the last bubble in the string to replicate and drop back one or more data positions. As a result, when the data is read, pages that should have been all 0s will have some 1s in them. Any tendency to simply drop back, as in Fig. 4b, can be accelerated by initiating a series of stop-start operations, which aid in readily isolating the defective devices.

Horizontal self-replication occurs when data is spuriously duplicated and transferred from one loop to another. Testing for this type of failure entails writing a pattern of several 1s followed by several 0s within one page of data. Repeating this data pattern throughout the bubble memory chip can help determine defects such as those shown in Figs. 4c and 4d, which will cause bubbles to either replicate or simply jump from a populated loop to an empty one.

First-level testing

The testing of magnetic-bubble memories can be done at several different levels of complexity. Because the devices are completely tested during manufacture, however, most users find it economically impractical to test beyond a first complexity level.

The first level encompasses all the aforementioned tests over the range of specified operation temperatures



4. Defect effects. Defects in chevron propagating elements can account for various types of data bit errors. A notch in the nickel-iron chevron can create a magnetic field anomaly that, depending on field strength, can split a bubble and hold half of it back (a) or simply prevent a bubble from propagating (b). Excess Permalloy can cause a bubble to be swapped (c) or replicated (d) into an adjacent loop.

of the bubble memory system (the bubble device and its control circuitry) at the printed-circuit–board level. If an error is detected, the data should be read again to determine if the error is hard or soft. Soft errors result primarily from faulty detection of bubbles during a read operation and can usually be corrected by simply rereading the data.

Careful layout of the system's components on its pc board can hold soft errors to a minimum. For example, it is important to keep the leads going from the detector output to the sense amplifier as short and as far away as possible from noise-generating leads, such as those supplying current to the orthogonal coils.

Hard errors occur because of some problem inside the bubble memory device, and they recur each time the data is read. However, even if the error is proven hard, the test sequence should be repeated to ensure that the problem originates in the device itself and is not caused by some malfunction at the board level. The system can also be operated in a continuous-read/write or continuous-read condition while logging any errors to determine the system's mean time to error (MTTE).

Greater complexity

In a second level of testing, separate digital-to-analog converters and discrete circuitry are hooked up to the device on the board in order to vary the voltages and function-current amplitudes over their specified ranges and over the temperature range of the device. This level of testing can be further extended by building a discrete bubble memory controller to vary the timing of the various control signals over the specified range.

For most users, this method is generally too time-consuming and costly. An alternative approach is to test the support circuitry at the board level before the bubble memory devices are added. Commercially available board testers can measure the duration and amplitude of the output signals from the various function drivers and timing generators. Once the support circuitry on the board passes these tests, the memory devices can be added and the completed board tested as a system. Failure analysis can then be done at the board level.

Figuring the margins

A third testing level attempts to determine where the magnetic-field bias is set by measuring the operating margins of the device. Since each bubble memory is enclosed in a magnetic shield, it is impossible to measure the strength of the permanent magnets' field directly; but normalized operating margins can be determined by using a strong external field to increase or decrease the field bias until bubbles either begin to collapse or strip out, respectively. The normalized operating margin will be the amount the bias can be varied before each type of failure occurs.

This last process is generally very expensive at the user level and can cause several interface, calibration, and correlation problems. Bias testing can contaminate masked-off loops or redundancy-map loops, and it can destroy seed bubbles. The user then has to have the necessary equipment for collapsing all the bubbles in the device and regenerating a seed bubble or any redundancy data for the map loops. For most users it is much easier to leave bias testing to the manufacturer. □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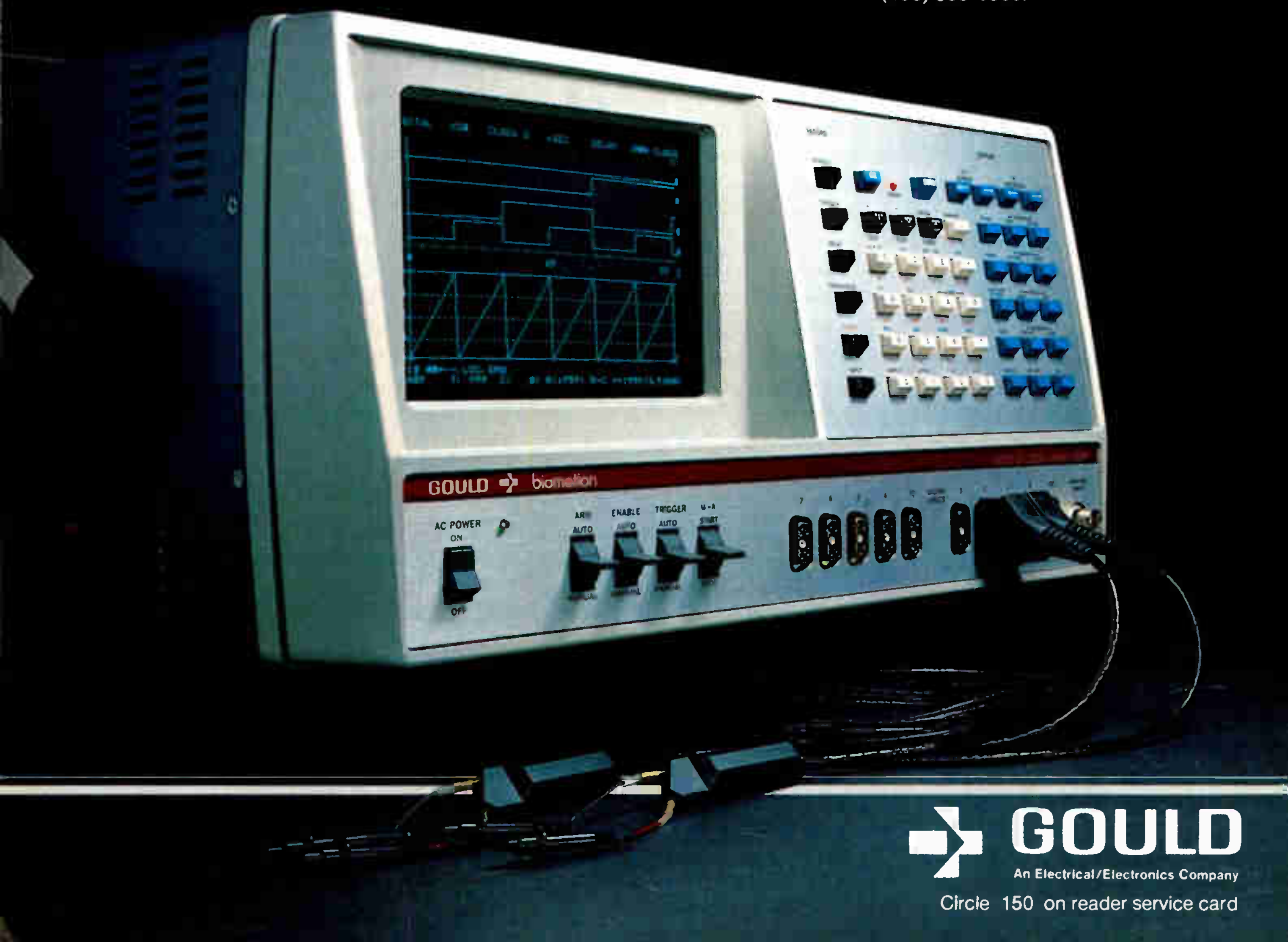

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Linearizing thermistors with a single resistor

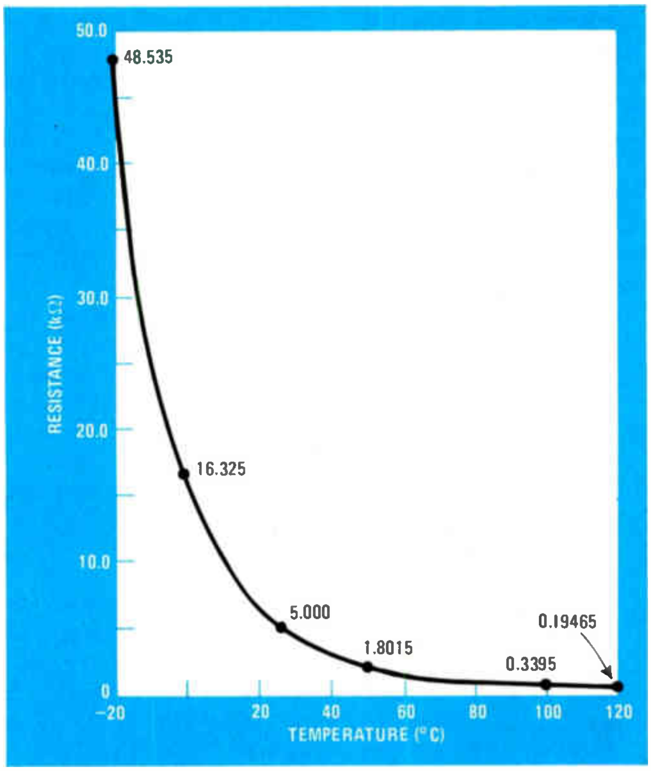
Adding a resistor to a thermistor is a suprisingly easy way to make fast and accurate temperature measurements

by Art Burke, *Burke Electronics, San Diego, Calif.*

☐ Accurate measurements of temperature are needed in a multitude of industrial applications. Thermistors are popular devices for the job, and readings would be simple if the thermistor's resistance varied linearly with its temperature. Thermistors, however, are nonlinear, and so a linearizing procedure is called for.

Manufacturers' design guides often treat linearization of thermistors as a trial-and-error operation or give approximation techniques that yield poor results. A more useful approach forces either the voltage output or the resistance of a simple fixed-resistor–thermistor network to have zero error along a linear temperature scale at three equidistant points, with errors elsewhere distributed in an S-shaped curve. Specifically, the method converts the nonlinear negative temperature characteristics of a thermistor into a linear relationship with peak errors of about ±0.01° over a 10°C range, ±0.05° over 30°C, ±0.6° over 50°C, and ±3° over a 100°C range.

Furthermore, using the resistor-thermistor network in a simple constant-voltage–fed bridge circuit with an adjustable-gain operational-amplifier output produces a voltage output that is directly related to temperature. For example, 0 volts corresponds to 0°C, 0.100 v to 10.0°C, and 0.500 v to 50.0°C.

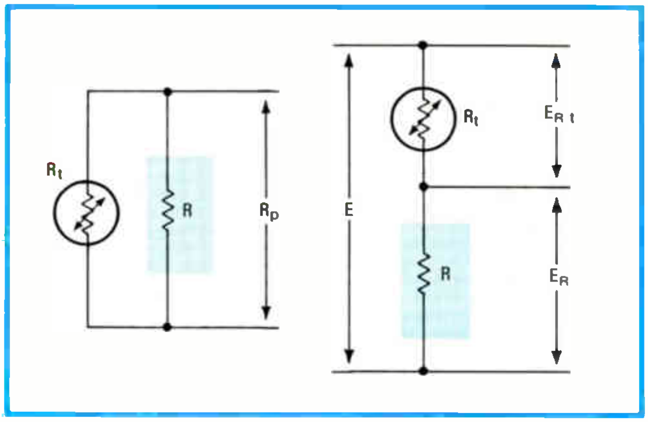


1. Typical. An NTC thermistor decreases in resistance nonlinearly with increasing temperature, as shown. Adding a fixed resistor in series or in parallel goes far toward linearizing the thermistor's response, simplifying conversion from temperature to voltage.

Typical curves

A typical resistance-temperature curve of a negative-temperature-coefficient (NTC) thermistor is shown in Fig. 1 for the range of −20° to 120°C. It is clearly nonlinear, yet a single fixed-value resistor, R, placed in parallel with the thermistor, as shown in Fig. 2, produces a parallel resistance that has a completely linear relationship with temperature at three equidistant points, T_a, T_b, and T_c, and a slightly S-shaped relationship at intermediate temperatures. This relationship is shown in Fig. 3 as the R_p curve. When placed in series with the thermistor, fixed-resistor R of the same value will produce a similar S-shaped curve with the same peak errors if a voltage across R is measured. This curve is labeled E_R (Fig. 3).

If temperatures T_a and T_c are slightly inside the desired range, the peak errors can be reduced somewhat



2. Linearized. A linearizing resistor, R, placed in parallel (left) or in series (right) with a thermistor produces a temperature to resistance or temperature to voltage characteristic, respectively, that is generally linear and at three temperature points is exactly linear.

Deriving the linearization equation

To derive the linearization equation for a fixed-resistor–thermistor network, let T_a, T_b, and T_c represent the temperatures at three equidistant (low, middle, and high) points—a, b, and c. Further, let R_a represent the thermistor resistance at temperature a, R_b the resistance at temperature b, and R_c the resistance at temperature c.

For resistor R in parallel with thermistor resistance R_t, the equivalent parallel resistance is determined by the well-known equation $R_p = R(R_t)/(R+R_t)$. In addition, the condition of equidistance requires that $R_{pa} - R_{pb} = R_{pb} - R_{pc}$. Substituting the equation for parallel resistance into this expression yields:

$$\frac{R(R_a)}{R+R_a} - \frac{R(R_b)}{R+R_b} = \frac{R(R_b)}{R+R_b} - \frac{R(R_c)}{R+R_c}$$

Canceling out the R in all the numerators gives:

$$\frac{R_a}{R+R_a} - \frac{R_b}{R+R_b} = \frac{R_b}{R-R_b} - \frac{R_c}{R+R_c} \quad (1)$$

Similarly, with a constant voltage, E, and the voltage E_{Rt} across R_t being linear, the voltage E_R across R must be linear, since $E = E_{Rt} + E_R$. Consequently, by voltage division, $E_{Rt} = E(R_t)/(R+R_t)$.

From the equidistance criterion, $E_{Ra} - E_{Rb} = E_{Rb} - E_{Rc}$. Therefore:

$$\frac{E(R_a)}{R+R_a} - \frac{E(R_b)}{R+R_b} = \frac{E(R_b)}{R+R_b} - \frac{E(R_c)}{R+R_c}$$

Canceling out E in all the numerators gives the same equation as Eq. 1. Solved for R, it yields:

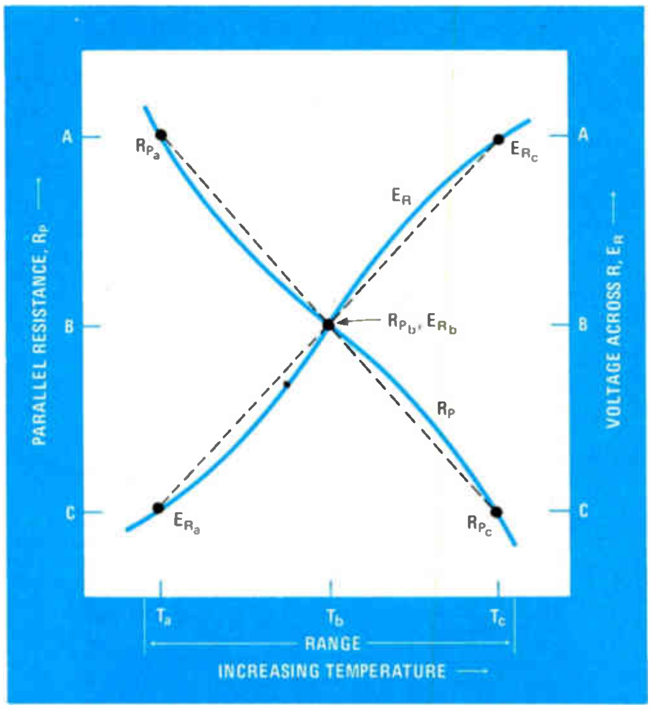
$$R = \frac{R_b(R_a+R_c) - 2R_aR_c}{R_a+R_c-2R_b}$$

because the curve will cross over at a and c. For example, if the desired range is 0° to 50°C, choosing 3°C for T_a and 47°C for T_c gives a slight error at 0°C; no error at 3°C; slight errors up to 25°C, where the error is again zero; slight errors from there up to 47°C, where the error is once again zero; and then slight errors up to 50°C.

The value of linearizing resistor R is found from the expression:

$$R = \frac{R_b(R_a+R_c) - 2R_aR_c}{R_a+R_c-2R_b} \quad (1)$$

where R_a, R_b, and R_c are the respective thermistor resistances at the low (T_a), middle (T_b), and high (T_c)



3. S shaped. The equivalent parallel resistance, R_p, of a thermistor and a linearizing resistor (shown in color) deviates slightly from the linear (black). Similarly, in a powered circuit the series combination produces an almost linear voltage, E_R, across the linearizing resistor.

points of the temperature range and where $T_b - T_a = T_c - T_b$ (see "Deriving the linearization equation.")

As an example, using the values taken from the manufacturers' tables from which the curve in Fig. 1 was plotted and the range 0° to 50°C, let:

T_a = 3°C R_a = 14,025 ohms
T_b = 25°C R_b = 5,000 Ω
T_c = 47°C R_c = 2,020 Ω

From Eq. 1, R is calculated to be 3,898.1 Ω.

The effect of this resistance in parallel with the thermistor is found using $R_p = R(R_t)/(R+R_t)$. A plot of the data between 3°, 25°, and 47°C reveals the shape of the S curve, indicating the small deviation from true linearity. The peak deviation can be estimated to be about 0.6°C, as mentioned earlier. The actual calculated deviations are +0.53° at 0°C, −0.62° at 10°C, +0.58° at 35°C, and −0.48° at 50°C.

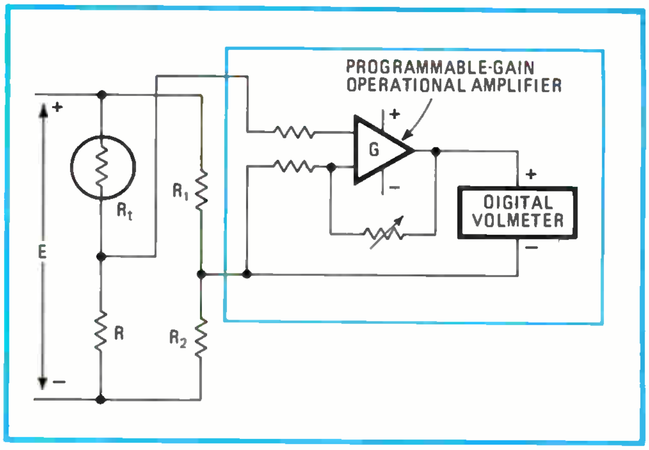
Generally, as noted, a linear voltage-temperature relationship is more useful for measuring temperature than a nonlinear one. It is even more useful if there is a direct reading between temperature and voltage without conversion factors.

If the thermistor, with resistance R_t, and fixed resistor R are put in series across a constant voltage source, the voltage across the thermistor will decrease with a rise in temperature, and the voltage E_R across R will increase as a result. Thus the voltage across R satisfies the requirement of having the output vary directly with temperature. If the voltage, E, is held at exactly 1.0 v dc, the voltage across R is:

$$E_R = E[R/(R+R_t)] = 1.0[R/(R+R_t)]$$

Using the example developed above for the range 0° to 50°C, where R was found to be 3,898.1 Ω (remember that R is the same whether used in series or in parallel with R_t) gives a value of R_t at 3°C of 14,025 Ω. Therefore E_{R3} = 1.0 [3,898.1/(3,898.1 + 14,025)] = 0.217490 v. R_t at 25°C is 5,000 Ω, so that E_{R25} is 0.438082 v. At 47°C, R_t is 2,020 Ω, giving a value of 0.658674 v for E_{R47}.

Since E_{R3}, E_{R25}, and E_{R47} lie on a straight line, E_R and T coincide at those three points. However, the voltages



4. One to one. For convenient temperature measurements, the bridge and op-amp scaling circuit shown gives a one-to-one correspondence between temperature and voltage. The digital voltmeter then displays a voltage that can be directly read as a temperature.

are not directly readable as temperatures. With a 4½-digit voltmeter on the 0-to-1-v range, it would be advantageous to read 0.0300 at 3°C, 0.2500 at 25°C, and 0.4700 at 47°C; moving the decimal point two places to the right, so that the readings are, respectively, 3.00, 24.00 and 47.00, would be even better. But first the maximum allowable voltage for E must be determined.

In most small thermistors, the maximum allowed power dissipation due to self-heating is about 1 milliwatt per °C in still air. To keep the self-heating error to about 0.1°C, the current must be limited to give a dissipation of about 0.1 mw in R_t when it is equal to R, which is the point of maximum power dissipation. In the example above where R is 3,898.1 Ω, the current, I, must be limited to $I = (P/R)^{1/2} = (0.0001/3{,}898.1)^{1/2} =$ 0.00016 ampere. The maximum E is then $I(R_t+R)$, where $R_t = R$, so that $E = I(2R) = 1.249$ v. This value is based on a worst-case condition, where the thermistor is surrounded by still air; if moving air, liquids, or solids are being measured, the self-heating error is much lower.

To get from the accurate but unwieldy voltage versus temperature relationship to a direct-reading digital-voltmeter output requires a bridge and a programmable-gain operational amplifier, as shown in Fig. 4. The first step is to obtain the gain of the op-amp circuit. In the example of a 0°-to-50°C measurement, a temperature change of 44°C produced a voltage change across R of 0.441184 v; the gain, G, must therefore be adjusted so as to be equal to $(D/100)/(E_{Rc}-E_{Ra})$, where D is the difference in °C between temperatures T_c and T_a, E_{Rc} is the voltage across R at temperature T_c, and E_{Ra} is the voltage across R at temperature T_a. Thus:

$$G = \frac{(1/E)(D/100)}{[R/(R+R_c)]-[R/(R+R_a)]} \qquad (2)$$

The next step is to calculate E_R at temperature T_a and subtract $(T_a/100)/G$ from it. That yields the voltage needed across R_2 in the bridge to give a voltage equal to $T_a/100$. For example, if $T_a = 3$°C, the voltage should be 0.030 v, since:

$$E_2 = E\frac{R}{(R+R_a)} - \frac{T_a/100}{G} \qquad (3)$$

and the voltage E_x for any temperature T_x is:

$$E_x = G\left[E\left(\frac{R}{R+R_x} - E_2\right)\right] \qquad (4)$$

where R_x equals the resistance of the thermistor at T_x. Finally, the error, EC, in °C is calculated as:

$$EC = (E_x)(100) - T_x \qquad (5)$$

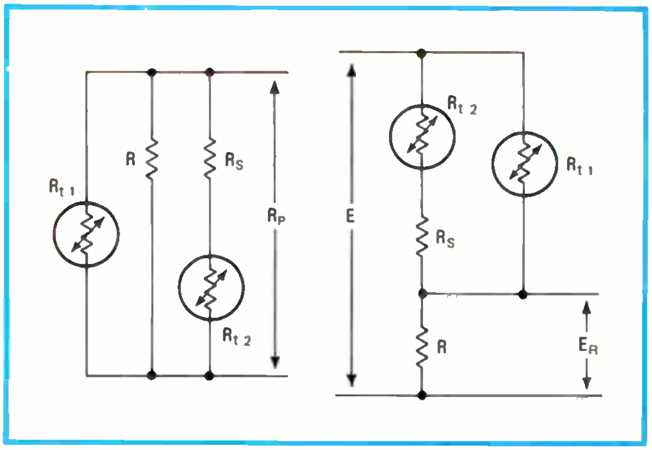
A simple Basic program to solve Eqs. 1 through 5 and calculate a table of temperature, voltage, and error in ±°C is shown at the right above.

The peak errors over large temperature ranges are reduced by an order of magnitude using a computer-aided design technique that combines the three-point

BASIC PROGRAM FOR CALCULATING TEMPERATURE, VOLTAGE, AND ERROR FOR A FIXED-RESISTOR-THERMISTOR NETWORK

```
100 REM 3-POINT THERMISTOR LINEARIZATION
200 DATA 14025, 5000, 2020, 44, 3, 1
300 READ A,B,C,D,L,E
400 LET D=D/100
500 LET L=L/100
600 LET R=(B*(A+C)-2*A*C)/(A+C-2*B)
700 LET G=D/(E*(R/(R+C) -R/(R+A)))
800 LET E2=E*R/(R+A)-L/G
900 PRINT "   R";R;"   G";G;"   E2";E2
1000 INPUT "Tx";T
1100 INPUT "Rx";R3
1200 LET E3=G*(E*R/(R+R3)-E2)
1300 LET E3=(INT(E3*10000+.5))/10000
1400 LET E4=E3*100-T
1500 PRINT" TEMP.";T;"DEG.C,";" DVM";E3;"V.,";" ERROR";E4;"DEG.C"
1600 PRINT
1700 GOTO 1000
```

NOTE: In line 200, type the values of the following variables in order after the word "data": R_a, R_b, R_c, T_c-T_a, T_a, and E for the application. The values for the previous example are used here for illustration.



5. Ultimate. Shown here is an improvement on the three-point linearing procedure of Fig. 2. The circuit on the left is the resistance version; the one on the right is the powered version. For both, peak errors are reduced by an order of magnitude over the original configuration when used over a large temperature range. Here R_{t2} represents N thermistors of the original type connected in parallel. R_{t1} is the original thermistor and R_S is added in series with R_{t2}. The program on page 154 is used to find N and R_S.

BASIC PROGRAM FOR CALCULATING PEAK ERRORS IN A MULTIPLE-THERMISTOR NETWORK

```
LIST
1 REM 3-POINT LINEARIZATION OF THERMISTORS
2 REM
5 REM FORMAT LINE 10: DATA Rt1a,Rt1b,Rt1c,Tc-Ta,Ta,E
6 REM FORMAT LINE 11: DATA Rt1 AT LOWEST TEMP. OF DESIRED
7 REM RANGE, Rt1 AT NEXT HIGHER T STEP, ETC UNTIL Rt1
8 REM FOR ALL STEPS ARE ENTERED. IN THE EXAMPLE BELOW THE
9 REM RANGE IS 0-100 DEG.C., STEP 5 DEG.,5000 OHM THERMISTOR
10 DATA 14025, 1801.5, 370.5, 94, 3, 1
11 DATA 16325, 12695,9950,7855,6245,5000,4028,5
12 DATA 3265,2663.3,2185,1801.5,1493,1244,1041.5
13 DATA 876,739.5,627.5,535,457.65,393.35,339.15
30 READ A1, B1, C1, D, L, E
40 D=D/100:L=L/100
47 REM
48 REM N IS THE NUMBER OF ADDITIONAL PARALLELED THERMISTORS
49 REM N=0 SIGNIFIES A SINGLE-THERMISTOR CIRCUIT
50 INPUT"N";N
55 IF N=0 THEN A=A1: B=B1: C=C1: GOTO 130
60 INPUT "Rs GUESS"; S
80 A2=A1/N: B2=B1/N: C2=C1/N
97 REM
98 REM SERIES-PARALLEL RESISTANCE OF A1,A2,AND Rs IS FOUND,ETC
100 A=(A2+S)*A1/(A1+A2+S)
110 B=(B2+S)*B1/(B1+B2+S)
120 C=(C2+S)*C1/(C1+C2+S)
128 REM
129 REM THE VALUE OF LINEARIZING RESISTOR R IS FOUND
130 R=(B*(A+C)-2*A*C)/(A+C-2*B)
138 REM
139 REM THE GAIN G OF THE OP-AMP CIRCUIT IS FOUND
140 G=D/(R/(R+C)-R/(R+A))/E
148 REM
149 REM THE NECESSARY OFFSET VOLTAGE E2 ACROSS R2 IS FOUND
150 E2=E*R/(R+A)-L/G
160 PRINT "  R";R;"  G";G;" E2";E2
180 PRINT"TEMP","DVM","ERROR"
181 REM
182 REM FORMAT LINE 185: FOR T= LOWEST T IN DESIRED RANGE TO
183 REM HIGHEST T STEP THE DESIRED INCREMENT. NOTE- MUST
184 REM MATCH VALUES IN LINES 11, 12, ETC.
185 FOR T=0 TO 100 STEP 5
187 READ R1
188 GOSUB 210
189 NEXT T
190 INPUT "WANT TO TRY OTHER TEMPERATURES, YES OR NO"; Q$
191 IF Q$="YES" THEN 193
192 GOTO 200
193 INPUT "Tx";T:INPUT "Rx";R1
194 GOSUB 210
195 GOTO 190
200 RESTORE: GOTO 10
205 END
208 REM
209 REM SUBROUTINE FOR FINDING DVM READINGS AND ERRORS
210 IF N=0 THEN R3=R1  :  GOTO 230
215 R2=R1/N
220 R3=(R2+S)*R1/(R1+R2+S)
230 E3=G*(E*R/(R+R3)-E2)
240 E3=(INT(E3*10000+.5))/10000
250 E4=E3*100-T
260 E4=(INT(E4*10000+.5))/10000
270 PRINT T, E3*100, E4
280 RETURN
290 END
READY
```

zero-error method with some cut-and-try efforts to determine the number of additional similar thermistors in parallel (or a single additional thermistor of 1/Nth the value of the original thermistor) and the value of a fixed resistor in series with the additional thermistor(s). The resulting circuit configuration is shown in Fig. 5, where R_t is the combination of the resistance of the original thermistor, R_{t1}; the parallel resistance, R_{t2}, of the N additional thermistors; and the additional fixed resistor, R_S; and where R is the linearizing resistor.

The value of R is found from Eq. 1 using R_t, which is the series-parallel combination of R_S, R_{t1}, and R_{t2} at the three equidistant temperatures. The values of R_S and N are found by the cut-and-try method, to minimize the peak errors. The second Basic program, above, allows for readily changing values of N and R_S and gives the peak errors over the temperature range for each value.

RESULTS OF PROGRAM 2, USING VALUES OF $N = 5$ AND $R_S = 1{,}050\ \Omega$

```
RUN
N? 5
Rs GUESS? 1050
   R 538.924              G 1.85074             E2 .135056
TEMP                    DVM                   ERROR
 0                       .24                   .24
 5                       4.89                  -.11
 10                      9.79                  -.21
 15                      14.83                 -.17
 20                      19.95                 -.05
 25                      25.05                 .05
 30                      30.13                 .13
 35                      35.16                 .16
 40                      40.12                 .12
 45                      45.06                 .06
 50                      50                    0
 55                      54.96                 -.04
 60                      59.94                 -.06
 65                      64.96                 -.04
 70                      70.02                 .02
 75                      75.13                 .13
 80                      80.21                 .21
 85                      85.24                 .24
 90                      90.23                 .23
 95                      95.09                 .09
 100                     99.82                 -.18
WANT TO TRY OTHER TEMPERATURES, YES OR NO? YES
Tx? -5
Rx? 21165
-5                      -4.07                  .93
WANT TO TRY OTHER TEMPERATURES, YES OR NO? YES
Tx? 105
Rx? 293.65
 105                    104.36                 -.64
WANT TO TRY OTHER TEMPERATURES, YES OR NO? NO
N? 4
Rs GUESS? X
?SN ERROR IN 60
READY
```

The thermistor resistances at various temperatures are entered as a data list in the first lines of the program and are used again and again as the cut-and-try attempts proceed. The results are displayed in the form of the table above, showing the errors at each temperature. The crossover points are easily changed in line 10 of the program to equalize the errors over the temperature range, and N and R_S guesses are dynamically changed to minimize the peak errors and consequently arrive at the optimum values. The procedure takes only a few minutes to give the values for minimum errors.

Running the program for a temperature range of 100°C using the data shown and selecting $N = 5$ and $R_S = 1{,}050\ \Omega$ produce the results that are shown above. Note how the errors are balanced over the range and how fast they increase above and below the range (for example, at −5° and 105°C).

In the second program, the "no" answer to the third interrogation jumped the program back to the point where new estimates of N or R_S or both could have been made as part of the cut-and-try procedure. A letter answer to either "N?" or "T_x?" rather than a number terminates the program (as shown) so that other crossover points and other variables can be entered on line 10. This program can be used as a general one, replacing the previous version, because it allows the selection of $N = 0$ for single-thermistor linearization over small temperature ranges, where errors are so small that multiple thermistors are not needed. □

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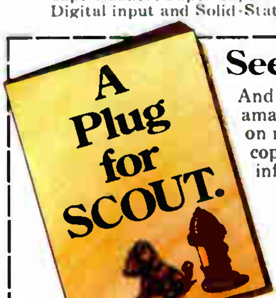

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Stable sinusoidal oscillator has multiple phased outputs

by James J. Rede
Rede Electronics, St. Louis, Mo.

This sine-wave oscillator design is useful as, among other things, a pure signal source for calibration. It provides gain-independent operation, is easy to adjust, and has a wide frequency range and stable amplitude. What's more, the circuit is self-starting and provides multiple-phased outputs of equal amplitude.

As shown in Fig. 1, the feedback loop has two 90° phase shifters and a unity-gain inverter. Thus, the circuit meets the criteria for oscillation—a loop gain of 1 with a phase shift of 180°. Each 90° phase shift is provided by the delay equalizer circuits (A_2, A_3). These two circuits have a unity gain at all frequencies and a phase shift that is adjustable between 0° and −180°. It is these properties that make the oscillator's features notably superior to those of other designs.

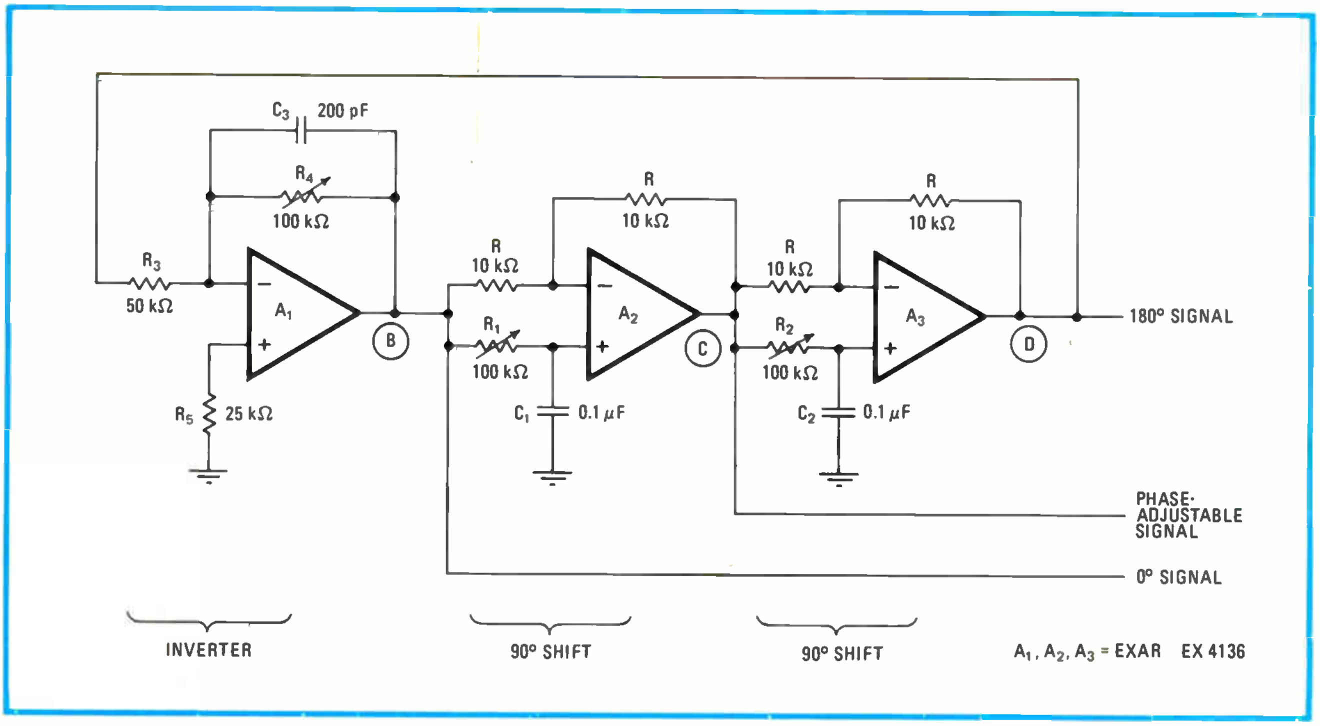
The transfer function of the equalizer circuit is $T(s) = V_{out}/V_{in} = (s-a)/(s+a)$, where $a = 1/R_1C_1$. At any frequency or pole/zero value, the absolute magnitude is always unity: $|T(s)| = |s-a|/|s+a| = (a^2+\omega^2)^{1/2}/(a^2+\omega^2)^{1/2} = 1$. Phase, $B(\omega)$, which is plotted in Fig. 2 is given by $B(\omega) = -2\tan^{-1}(\omega/a)$, where $a = 1/R_1C_1$. At $\omega = a$, the zero contributes −135° of phase shift and the pole contributes 45° of phase shift for a total phase shift of −90°.

The frequency of oscillation is completely determined by the two independent time constants, R_1C_1 and R_2C_2, and can be expressed exactly as $f = 1/[2\pi(R_1C_1R_2C_2)^{1/2}]$. If $R_1 = R_2$ and $C_1 = C_2$, then $f = 1/(2\pi R_1C_1)$.

Since the frequency range of oscillation is totally independent of any gain factor, the amplitude stability and the amplitude of oscillation are completely decoupled from the frequency-determining adjustment of R_4. A wide frequency range is assured for this oscillator. The amplitude of oscillation is determined by the maximum voltage swing of the op amp.

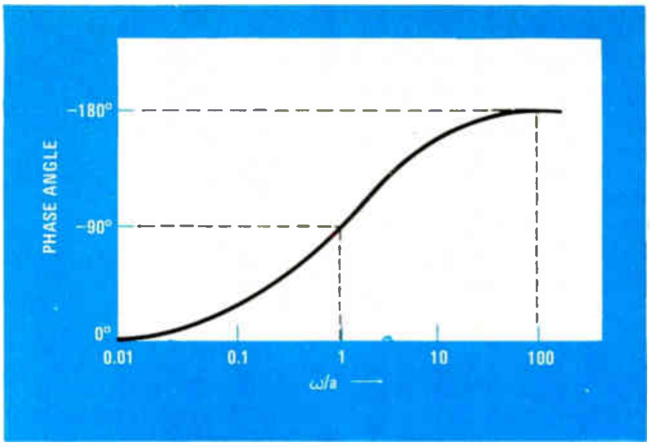
In the circuit of Fig. 1, C_1 and C_2 are equal; R_1 and R_2 are set equal; R_4 is adjusted for a total loop gain of 1. As the loop gain approaches unity, the pure sinusoidal oscillation begins. Further adjustment of R_4 permits the oscillation to be easily stabilized at its maximum amplitude and with no harmonic distortion. Adjustment of R_1 alters the phase relationship between the 0° and −180° signals. It also changes the frequency of the oscillator without disturbing the amplitude, amplitude stability, or oscillation criteria. The placement of C_3 in the circuit prevents high-frequency parasitic oscillations from occurring in the operational amplifiers.

Oscillations over a large frequency range could be obtained by changing the value of C_1 and C_2 and varying R_1 and R_2 with a dual potentiometer. For single-element



1. Phased out. An inverter (A_1) and two identical equalizer circuits (A_2, A_3) form a sinusoidal oscillator. Three equal-amplitude signals are at 0°, 90°, and 180° phase angles, respectively. The oscillator is self-starting and is capable of a wide range of frequencies.

2. Frequency equalizer. The oscillator circuit in Fig. 1 provides unity gain independent of frequency. The phase angle of the output varies from 0° to −180° with frequency, as shown above. At the frequency of oscillation, ω = a, the phase angle is −90°.



control, R_1 and R_2 could be voltage-controlled resistances. Over a narrower range, frequency can be adequately varied by just adjusting R_1.

The circuit is ideal for producing multiple signals with precise phase relationships of equal amplitude. By cascading increasing numbers of delay equalizer stages, signals of any phase can be easily obtained. □

Engineer's notebook is a regular feature in Electronics. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $75 for each item published.

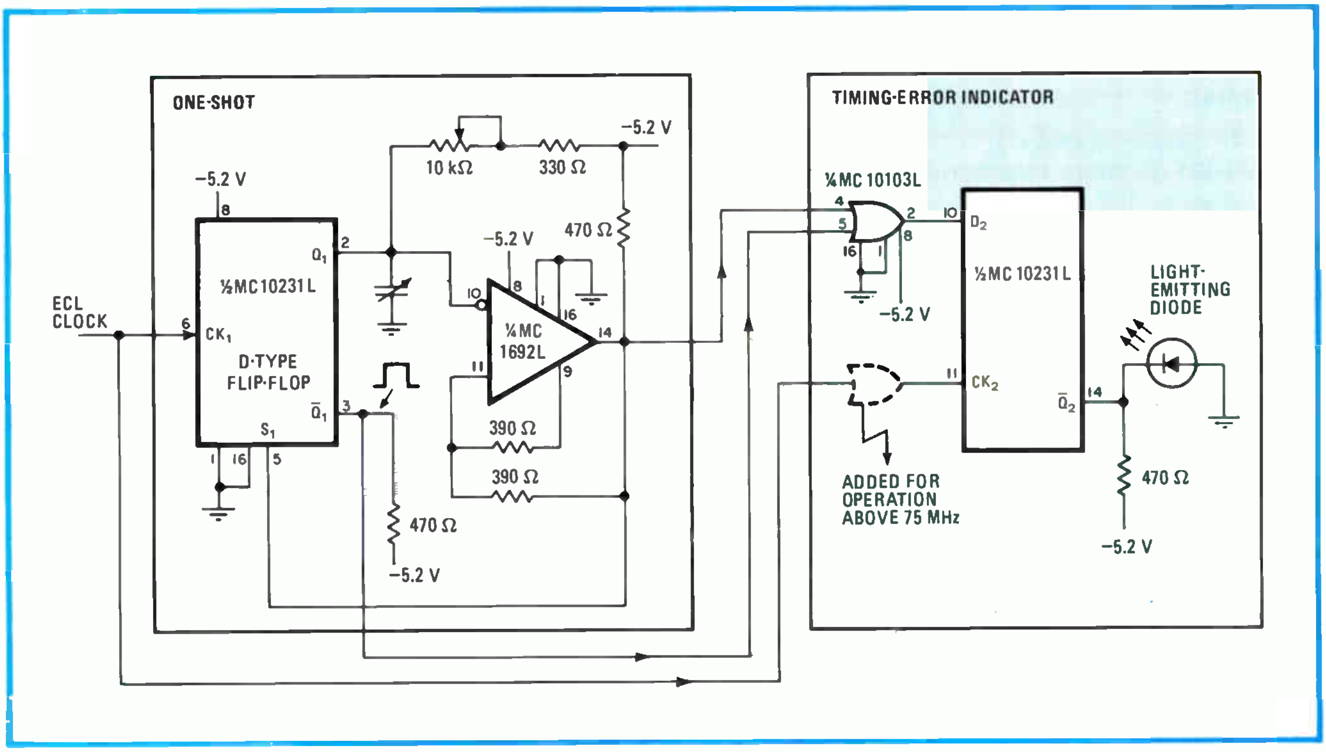
LED indicates timing error in emitter-coupled-logic one-shot

by M. U. Khan
Systronics, Naroda, Ahmedabad, India

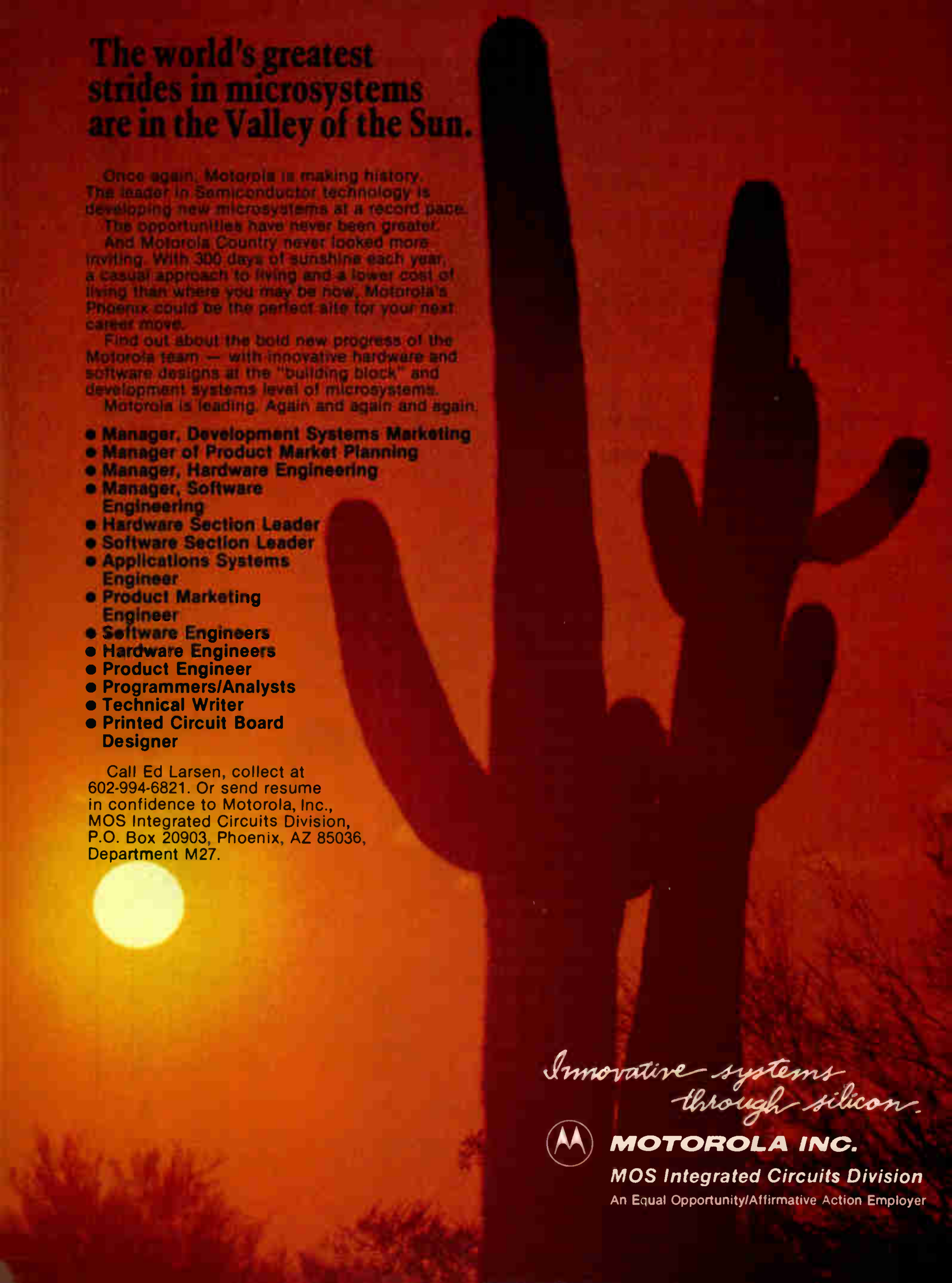
Rather than scrutinize waveforms on an oscilloscope, it is possible to employ a simple circuit to monitor the output of a one-shot to determine if it is being triggered at the right time or if the output pulse width is correct.

If the clock pulse arrives while the normally low output $\bar{Q}_1$ or set line S_1 of the one-shot is at a logic 1 level, the $\bar{Q}_2$ output of the indicator flip-flop goes to a logic 0 level, turning on the light-emitting diode. Q_1 of the one-shot remains at the logic 1 level only in its quasi-stable state, whereas S_1 goes to the logic 1 level only in its recovery state. Thus whenever the one-shot is triggered too early—in other words, before recovering—the LED turns on. When the mistriggering is corrected, by reducing either the clock rate or the width of the one-shot, it automatically turns off.

Besides the LED, the indicator circuit consists of an MC 10103 OR gate and an MC 10231 D-type flip-flop, both emitter-coupled-logic devices. The circuit works satisfactorily up to 75 megahertz. For higher speeds—up to 100 MHz—propagation-delay compensation through an additional OR gate (dotted line) is needed. In the latter case, both the OR gates should be replaced by an MC 1660 dual four-input OR-NOR gate. □



Hot shot. Spotting timing errors in a fast one-shot multivibrator is simplified with the addition of an error indicator circuit such as the one shown in the shaded area. If the clock rate is too high or the output pulse width is too small, the LED will indicate it.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Charge-balancing modulator aids analog-signal isolation

by Tadeusz Goszczynski and Jerzy Harasimowicz
Industrial Institute of Automation and Measurements, Warsaw, Poland

For engineers trying to solve ground loop problems in industrial instrumentation, here is a novel and inexpensive isolation circuit for analog signals. It employs a voltage-to-pulse-width modulator to convert analog signals into digital ones so that the job can be handled easily by low-cost opto-isolators. This is done by using a clock-synchronized charge-balancing scheme to economically achieve an accuracy of within 0.01%.

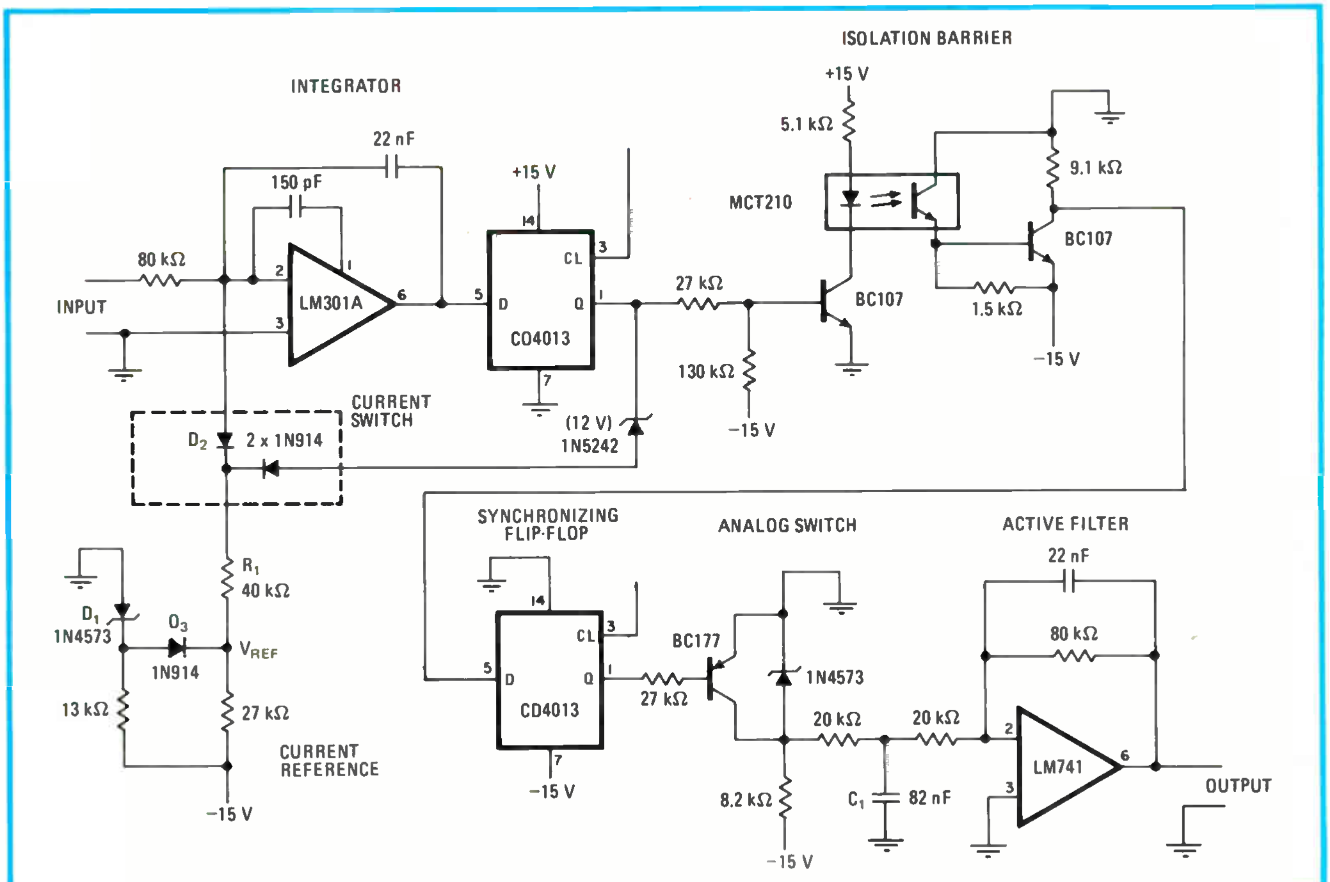
The charge-balancing modulator consists of an operational-amplifier integrator on the input that feeds the D input of a flip-flop. A constant-current sink and switch are driven by the flip-flop to produce a pulse whose width is proportional to the input voltage. This signal feeds the opto-isolator, the output of which is converted back into a voltage by the demodulator consisting of a synchronized flip-flop, a current sink, and an op-amp low-pass filter.

The voltage-to-pulse-width conversion is facilitated by switching the constant-current sink from the output of the flip-flop to the input summing mode of the op amp. Initially, the current switch is open, so that when the input voltage is applied, a negative-going ramp is produced at the integrator's output. When this voltage passes the flip-flop's input threshold voltage, it changes state synchronously with the next clock pulse, thereby closing the current switch. This action causes the reference current (which is always greater than the maximum input current) to be subtracted from the integrator's input current, producing a negative-going ramp at its output that eventually causes the flip-flop to toggle again. The time between toggles is proportional to the input voltage, and a transistor converts that time into a corresponding pulse width that drives the opto-isolator.

The current reference is actually a voltage-reference diode, D_1, and a resistor, R_1, that uses the fact that the integrator summing node is at virtual ground (0 volts) thus making the reference current equal to V_{REF}/R_1. Diode D_3 compensates for temperature-caused variations in diode D_2.

The demodulator relies on a synchronized flip-flop (driven from the same clock source) that can switch another current source on to charge capacitor C_1 to the original input voltage. The active filter smoothes the demodulator's response.

The analog-signal isolator can handle signals between ±10 V accurately to within 0.01% and has a frequency range of 0 (dc) to 100 hertz with a common-mode rejection of 100 decibels and an isolation of over 2,500 V dc between inputs and outputs. □



1. Analog-signal isolator. Input voltages are converted into proportional pulse widths that are fed to an inexpensive opto-isolator. The pulse is then converted back into a voltage that tracks the input voltage accurately to within 0.01%. The circuit uses a minimum of precision parts.

Engineer's newsletter

Hooking up a transistor radio to a home computer

A combination amplifier-speaker is a handy attachment for home computers to generate sound effects for game and utility programs. Though such devices are commercially available, **any transistor radio equipped with an earphone jack can easily be converted into an amplifier-speaker** while retaining its function as a radio. Cass Lewart of System Development Corp., Eatontown, N. J., has done it this way:

Disconnect two of the three leads attached to the earphone jack. Do not disturb the ground lead, but remove the lead going to the speaker and the lead going to the output stage. Solder these two leads together. Then disconnect the lead going to the "hot" side of the volume control and connect that lead to the earphone jack terminal formerly connected to the speaker. Finally, connect the remaining free jack terminal with a short wire to the high side of the volume control. The earphone jack now is the input to the amplifier-speaker. Gain is adjustable with the volume control. When the jack is not in use, the radio operates as before.

Learn to work with CAD

About to make the leap into computer-aided design of ICs? You might want to look into Integrated Circuit Engineering Corp.'s design center, which offers comprehensive hands-on design training programs employing CAD. **A complete program guides engineers through the IC design cycle**—from initial specifications to evaluated prototypes—and shorter programs concentrating on specific portions of the design cycle can be arranged. Basic and advanced application training courses for both CAD and computer-aided manufacturing are also offered. For more information, contact ICE, 15022 N. 75 St., Scottsdale, Ariz. 85260; (602) 998-9780.

Watch water-soluble transformer coatings

Quality-control problems can result from completely unexpected causes, as a recent production problem at Analog Devices Inc., Norwood, Mass., shows. There, a shipment of small power transformers were in the process of being wave-soldered onto printed-circuit boards. The assembled boards were then run on an in-circuit component tester, which detected excessive primary-to-secondary leakage resistance. An investigation revealed that the varnish used to impregnate the windings had washed off during a de-ionized-water wash-and-dry cycle that was a standard part of the company's soldering process; **the loss of the varnish allowed moisture to get into the windings.** A team of engineers worked with the vendor and recommended alternative impregnating materials that ended the problem.

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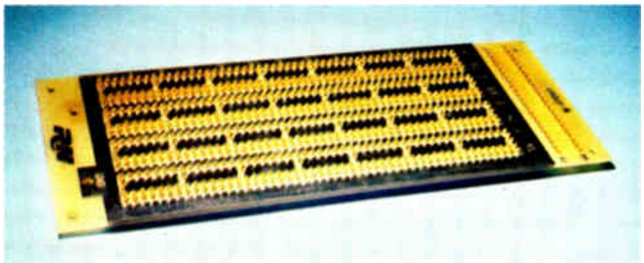

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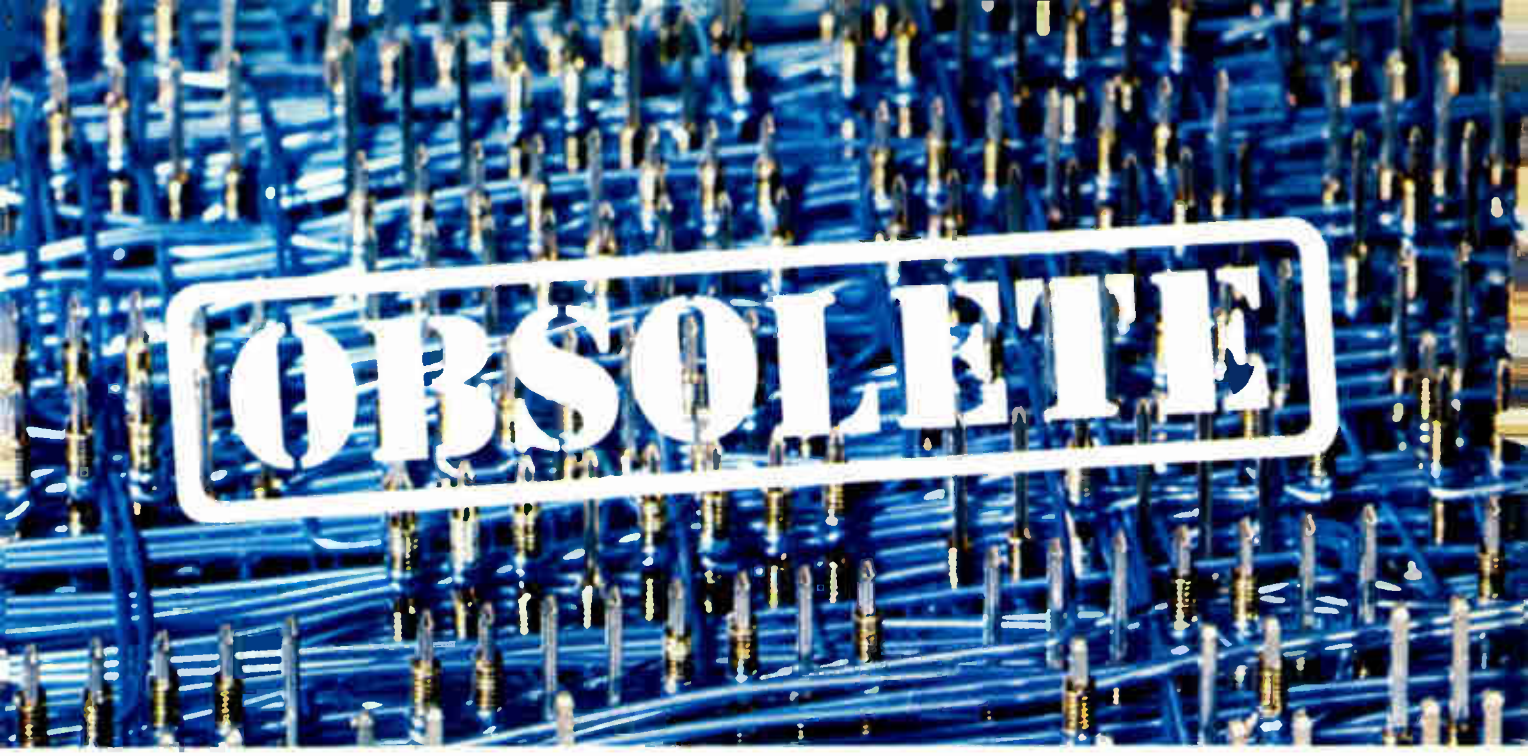

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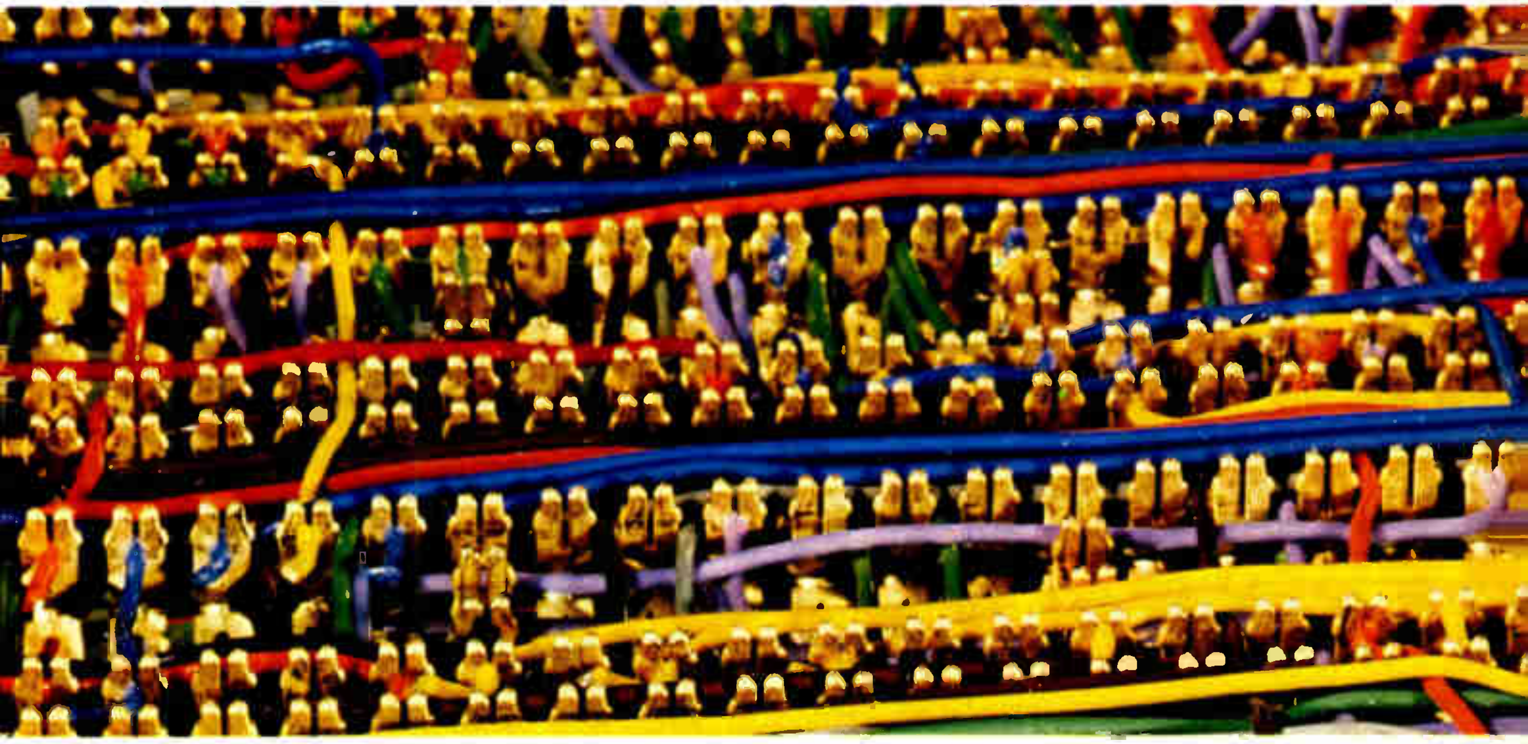

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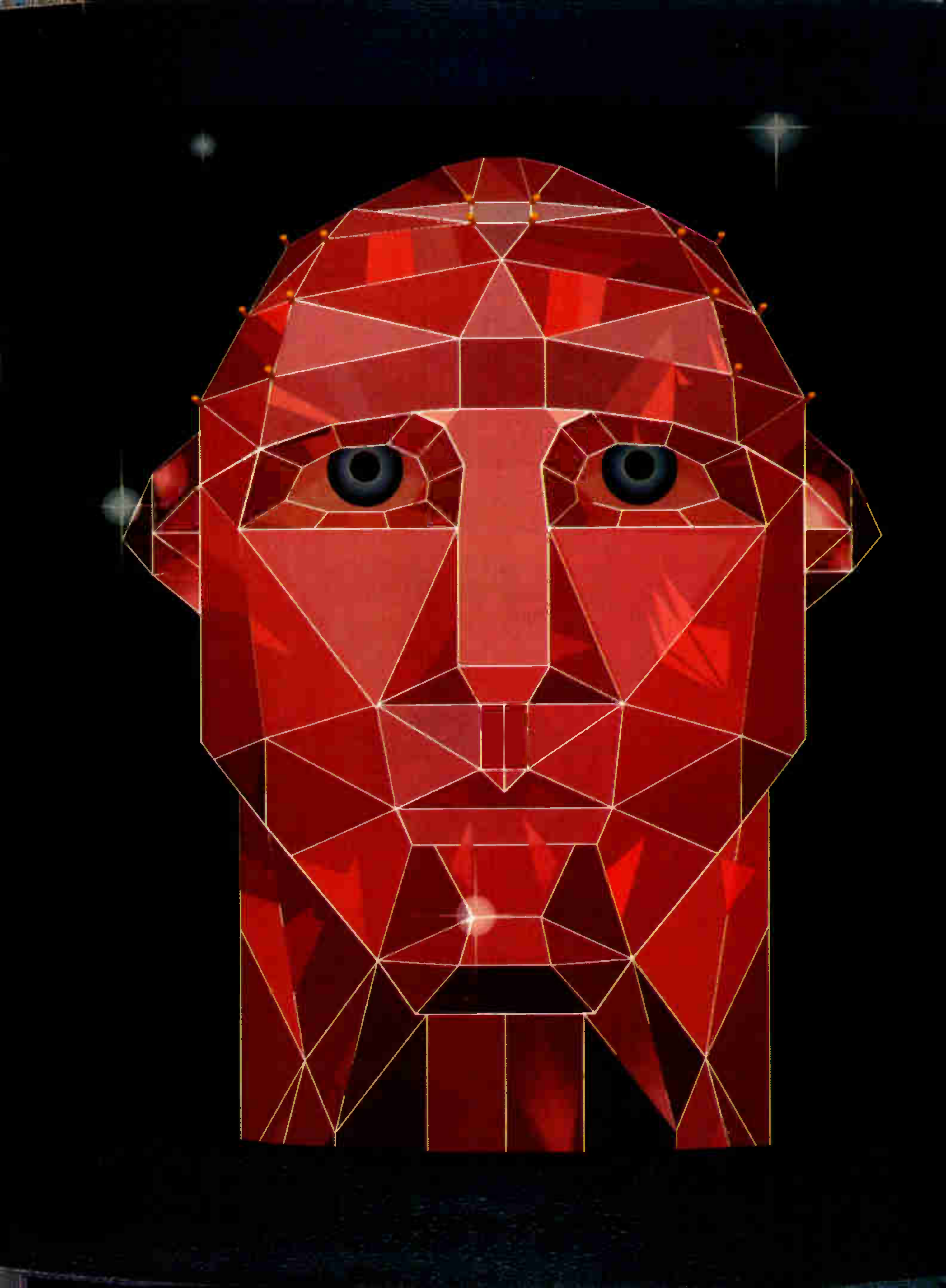

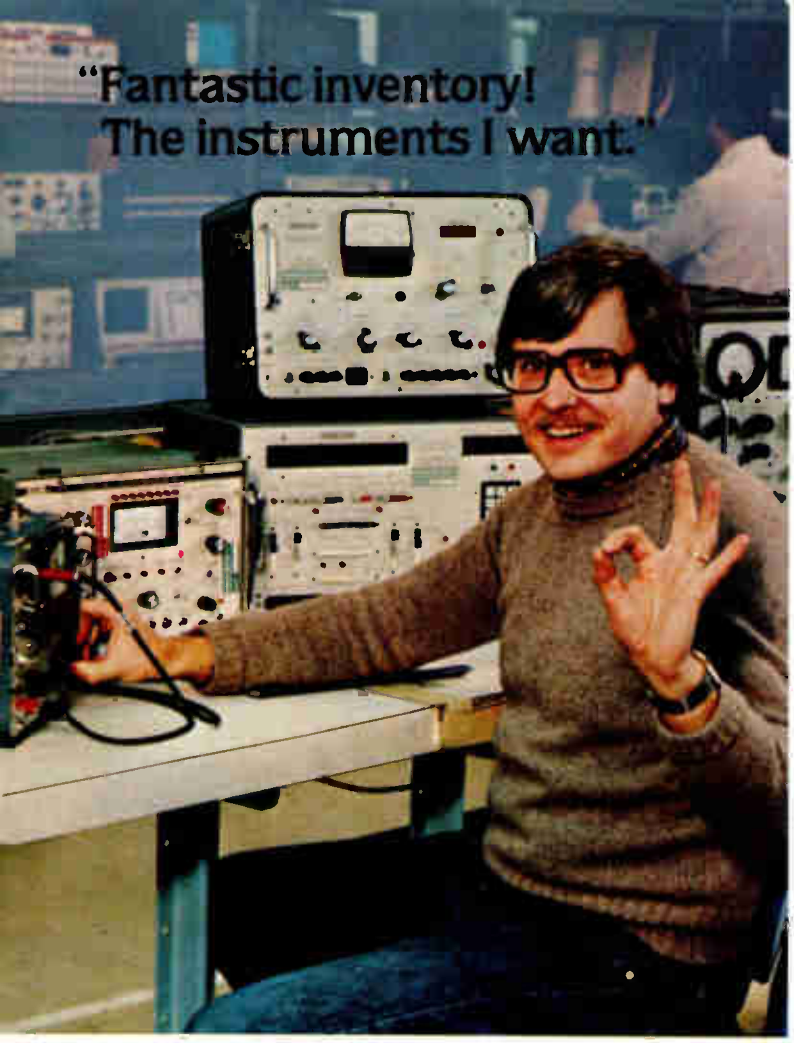
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16-K C-MOS static RAM is fast

Two-level polysilicon process builds a 1.1-mil² cell with 3-μm design rules, achieving a 70-ns maximum access time

by Bruce LeBoss, San Francisco regional bureau manager

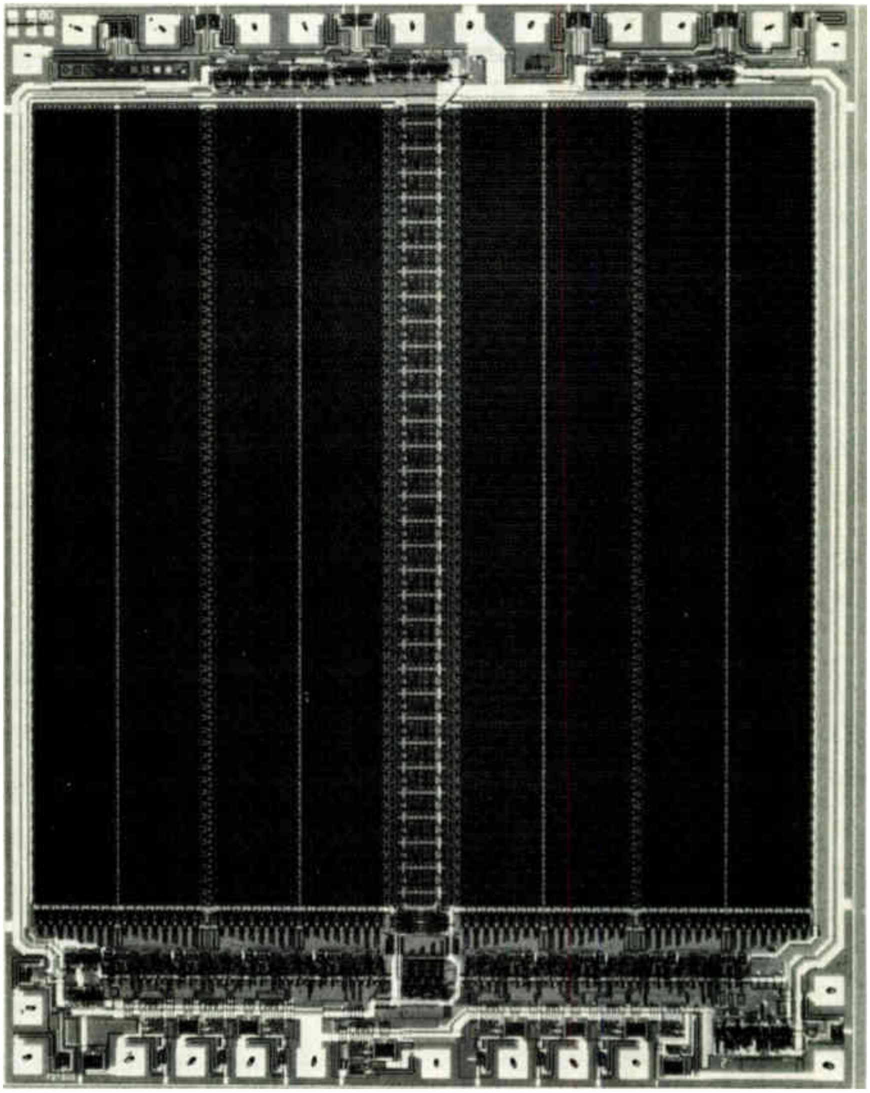
What better way to start out in the semiconductor business than with a sophisticated chip that is the fastest, smallest, and least power-consuming of its kind. That is exactly what Integrated Device Technology is about to do with the introduction of a 16-K static random-access memory made with a proprietary two-level polysilicon complementary-MOS process.

Designated the IDT 6116, the 2-K-by-8-bit part is available with maximum access times of 70, 90, and 120 ns, which makes it as fast, if not faster, than comparable byte-wide n-channel MOS 16-K static RAMs [*Electronics*, May 5, p. 34], as well as the fastest 16-K C-MOS static RAM available: Hitachi Ltd.'s HM6116, with which the IDT 6116 is pin-compatible, has maximum access times of 120, 150, and 200 ns. "We have built a few that run as fast as 55 ns, but we'll not be offering these initially," says George F. Hwang, president. The IDT 6116 consumes 180 mW (39 mA at 5 V) in the operational mode and a mere 100 μW on standby.

According to Hwang, the RAM's two-level polysilicon design facilitates production with conservative, 3-μm design rules. Even without pushing the design rules or shrinking, "which will yield much faster parts," he continues, the IDT 6116 already has the smallest cell area (1.1 mil²) and the smallest chip area (34,200 mil²) by far, in comparison with other byte-wide 16-K C-MOS static RAMs [*Electronics*, Dec. 18, p. 118]. The chip will be available in a 24-pin dual in-line package with pinouts compatible with industry-standard 16-K erasable programmable read-only memories.

In addition to the use of double polysilicon, several process innovations are responsible for the IDT 6116's extremely high packing density, Hwang says. One such is the use of edge-coincident contacts, he continues, "unlike competitive devices that employ traditional dog-bone contacts, which result in a much lower packing density."

Also contributing to the small chip area and high speed of the IDT 6116 is the fact that its three-state output stages are built with bipolar pull-up transistors and n-MOS pull-down



devices. If both the pull-up and pull-down devices were n-channel, Hwang explains, the memory would slow down as the temperature increased. However, the use of the bipolar pull-up transistor, in contrast to the buried junction field-effect transistor that Hitachi's memory uses, causes a faster pull-up phase that offsets the slower pull-down phase as temperature increases.

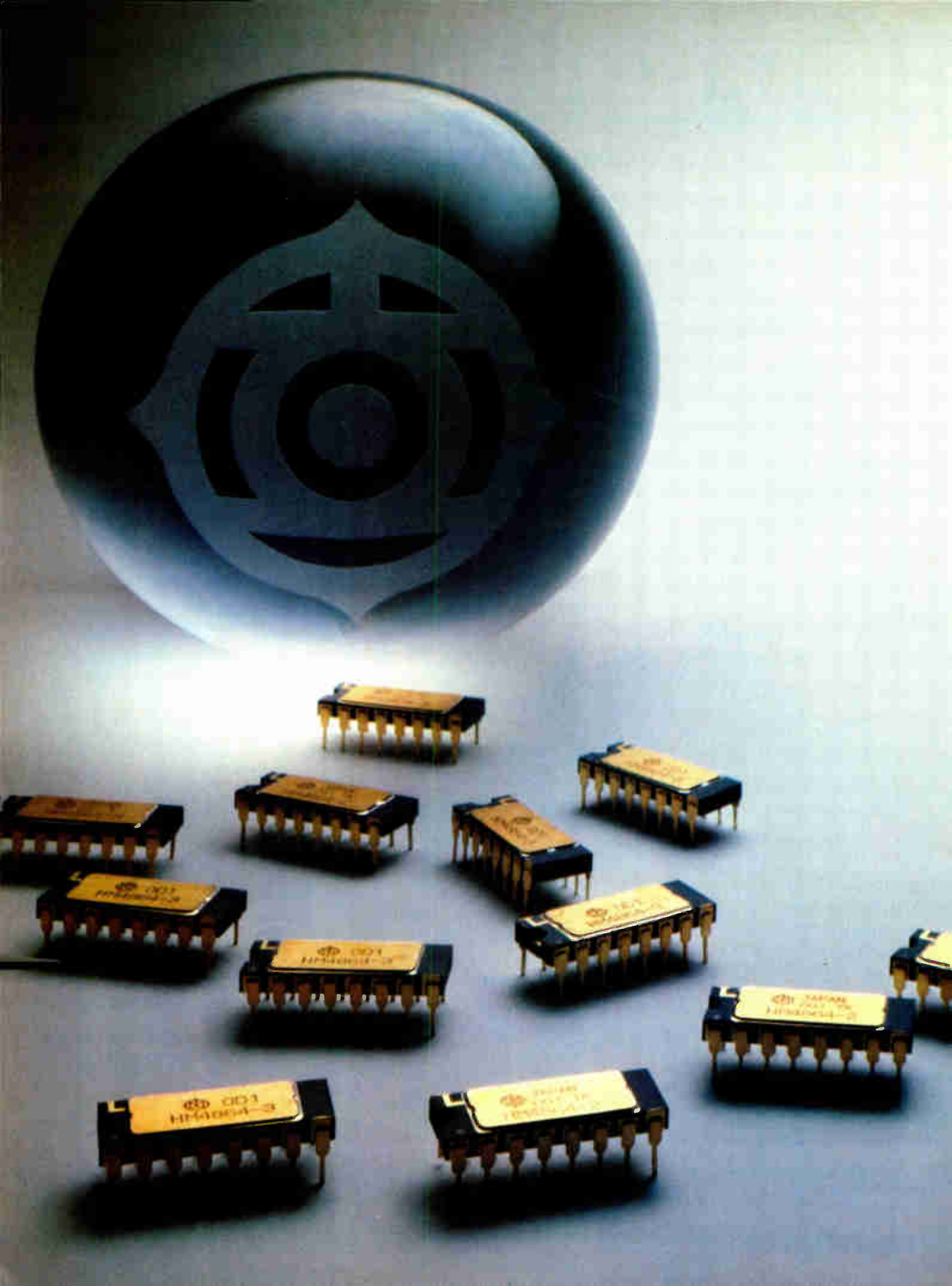
Like the Hitachi memory, the IDT 6116 has C-MOS peripheral circuitry surrounding its n-MOS cell array, or core, which is situated in a large but shallow p well. This dual-well design provides protection from alpha-particle–induced soft errors, Hwang says. "If there are any electron pairs formed, it will be below the p well, where they will be swept away to the n-doped substrate. The IDT 6116 is less susceptible to alpha-particle errors than are most n-MOS and some C-MOS RAMs."

The IDT 6116 incorporates ratioless circuits and differential sense circuits for the output sense amplifiers, causing a broad tolerance for power-supply variations. The memory requires a single +5-V (±10%) power supply, and supply levels can drop as low as 2 V during emergency standby with full data retention. All inputs and outputs of the IDT 6116 are directly TTL-compatible.

In sample lots of 1 to 24, the 120-ns version of the IDT 6116 will be priced at $50 each, "competitive with Hitachi's fastest HM6116," Hwang notes. The 90- and 70-ns parts, for which "no competitive parts exist," he adds, will be priced at $70 and $90, respectively, in like quantities. Delivery is in six weeks.

Quantity production of the fast IDT 6116 will begin by the fourth quarter of this year. At that time, the company is expected to begin supplying samples of a fast 16-K-by-1-bit C-MOS static RAM, the IDT 6167. At a 55-ns maximum access time, the IDT 6167 will be faster than the pin-compatible Hitachi HM6167, samples of which are about to be shipped.

Integrated Device Technology, 21580 Stevens Creek Blvd., Suite 107, Cupertino, Calif. 95014. Phone (408) 257-6493 [338]



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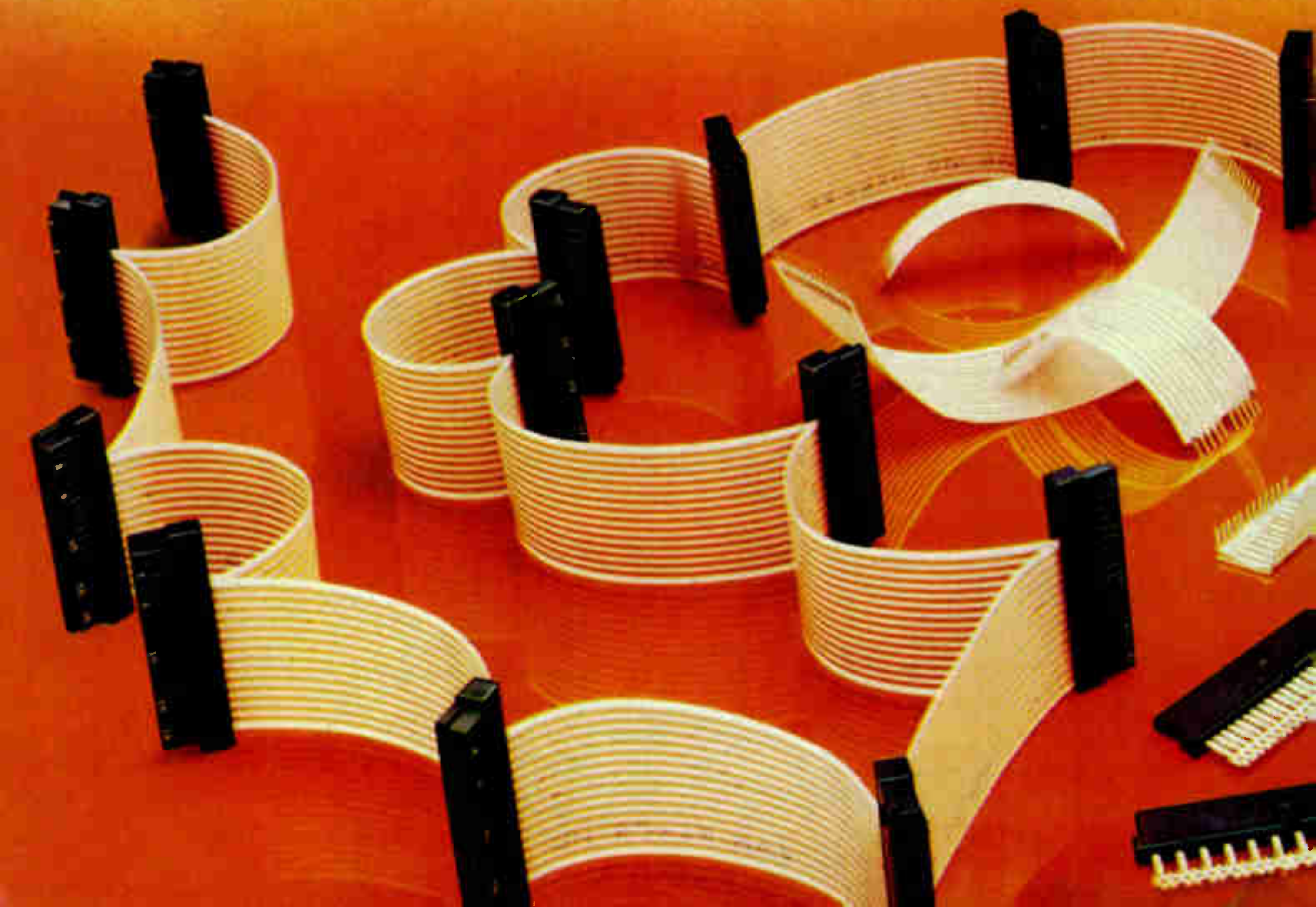


Six-word FIFO joins d-a converter

Monolithic C-MOS digital-to-analog converter accepts bursts of data to ease burden on host microprocessor

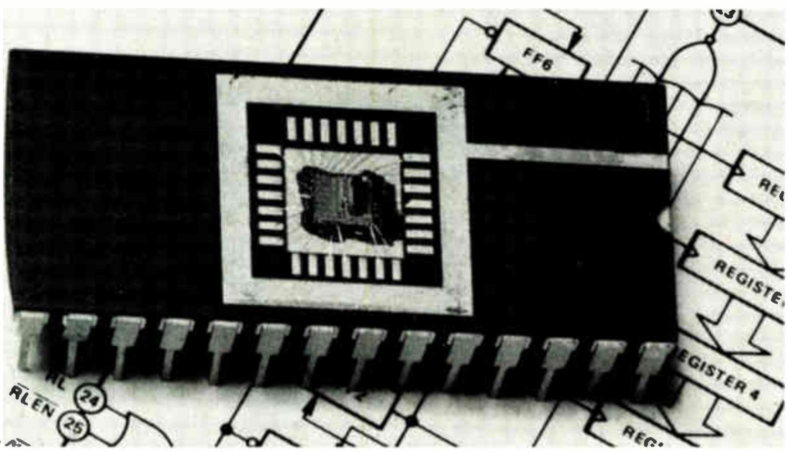
by Linda Lowe, Boston bureau

The AD7544 monolithic 12-bit digital-to-analog converter from Analog Devices employs an on-chip first-in, first-out register stack that accommodates parallel loading of data in bursts of six 12-bit words. This approach eases the amount of software supervision attending the loading of conventional d-a converters, which must receive a continual stream of data and therefore frees the host central processing unit's time for other functions, notes John Wynne, an applications engineer at the firm.

"In automatic test equipment or instrumentation, for instance, you can load a sequence of six values into the AD7544 at processor speed, then clock them through at a slower rate while the CPU is off doing other chores. That's a lot more efficient than making the CPU stand by with a new value for each test," Wynne says. He adds that the AD7544's ability to accept bursts of data also protects it from momentary CPU outages caused by local power failures in process control environments or in cases where the CPU must handle service or interrupt calls from elsewhere in the system [*Electronics*, May 19, p. 229].

A complementary-MOS device that can perform two- and four-quadrant multiplication, the AD7544 interfaces directly with 16-bit microprocessors. Two status flags control the data-feed rate from the CPU into the converter's 12-bit-wide FIFO stack. In addition to ATE and process control applications, the part can work in vector generation for graphics displays by real-time cathode-ray-tube systems or intelligent X-Y plotters and in complex waveform generation, Wynne says.

The AD7544 comes in nine models in either plastic or ceramic 28-pin dual-in-line packages. Three models operate over the commercial temperature range of 0° to +70°C and cost $19.50 to $26 each in 100-unit lots. Three industrial-grade models, operating from −25° to +85°C, range in price from $25 to $31.50 apiece for like orders. Military versions of the AD7544 operate from −55° to +125°C and cost from $62.50 to $78.75 each in 100-unit lots.



Relative accuracy of the lowest-cost models in each temperature-range category is to within ±1 least significant bit maximum, and differential nonlinearity is a maximum of ±2 LSB. Each of the low-end models is monotonic to 11 bits over its full operating temperature range. The other six models have maximum relative error and differential nonlinearity of ±½ LSB and ±1 LSB, respectively, and are monotonic to 12 bits over their full operating temperature ranges.

The highest-end models for each temperature range have a maximum gain error of ±1 LSB at 25°C ambient and ±2 LSB at +125°C ambient. All other models in the series have maximum gain errors of ±12.3 LSB at +25°C to ±14.5 LSB at +125°C. In all cases, gain error is adjustable to zero. The gain-error temperature coefficient typically is 2 ppm/°C for all nine models; the maximum temperature coefficient, 5 ppm/°C.

Propagation. As for other specs, the maximum propagation delay in all models ranges from 185 ns at +25°C to 250 ns at ±125°C, and the maximum propagation delay in the FIFO register stack is from 1.26 µs at +25°C to 1.6 µs at +125°C. Multiplying feedthrough error for all models is a maximum of 2.5 mV peak to peak over the full operating temperature range. Output glitch energy typically is 700 nV-s.

The AD7544 operates at low power, drawing 2 mA maximum from a single +5-V power supply. Delivery is from stock.

Analog Devices Inc., Route 1 Industrial Park, P. O. Box 280, Norwood, Mass. 02062. Phone (617) 329-4700 [341]

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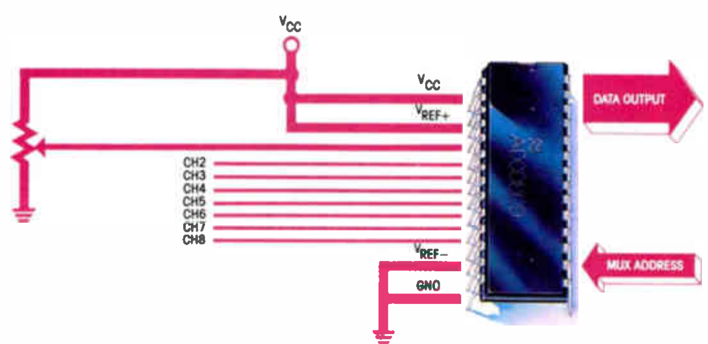

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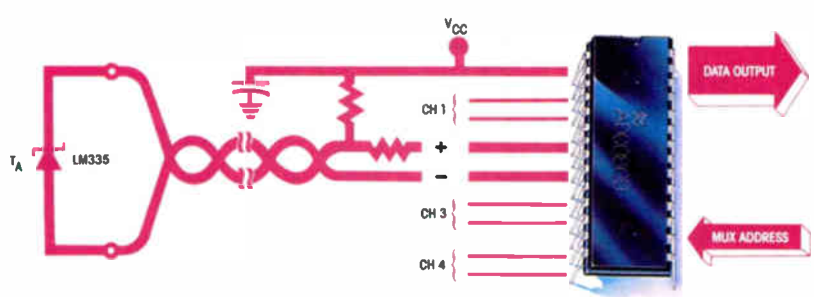

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LH0084-The logical choice in instrumentation amps.

The LH0084 programmable gain instrumentation amps were designed specifically for data acquisition systems where settling time and input impedance are critical to the systems' integrity. As a result, the LH0084s settle to 0.1% in only 4µsec or less and offer 500pA input bias current and a typical input impedance of $10^{11}\Omega$.

Gains for the LH0084 are set internally in two stages. The first stage is software programmable in highly accurate gain steps of 1, 2, 5, or 10. This stage, controlled by a 2-bit TTL-level input word, allows software to set gains dynamically within the system.

For additional flexibility, the second stage can be pin-strapped to gains of 1, 4, or 10. So it's easy to see why the LH0084 is truly the logical choice when it comes to instrumentation amps.

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Board level practicality for process control.

The BLC-8737—the quick and easy link between analog and digital.

National's MULTIBUS™ compatible BLC-8737 I/O board handles the complete analog conversion and scanning control for a data acquisition system. All data is converted with 12-bit resolution and a high ±0.05% accuracy.

Thanks to the BLC-8737's simplicity, the system software need only tell the board what gains it wants for each of the input channels: 16 single-ended (8 differential) that are easily expandable to 32 single-ended (16 differential).

And with two analog output channels available, the BLC-8737 serves as an ideal central supervisor for complex process control systems.

That's impressive capability for such an easy-to-use board.

For more information, check box 001 on this issue's coupon.

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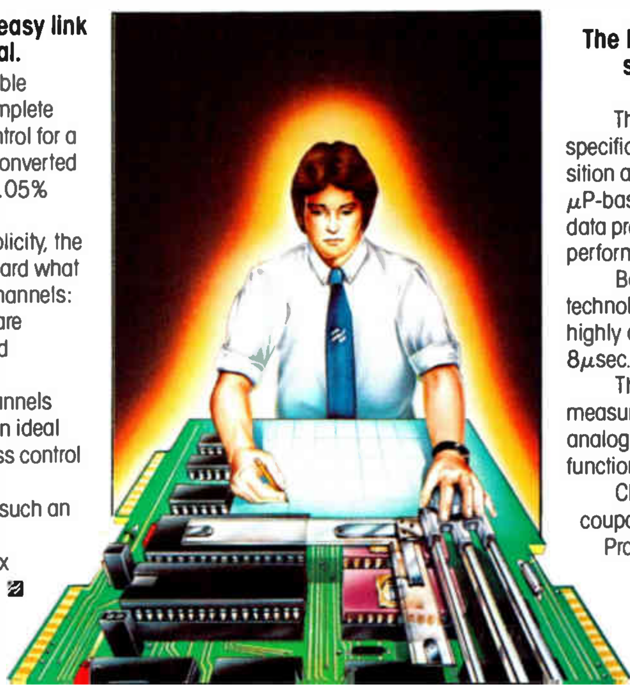

The BLC-8715's onboard intelligence smooths out process control.

The BLC-8715 Analog Input Board was specifically designed for industrial data acquisition and process control systems. This new µP-based interface offloads all of the analog data pre-processing functions normally performed by the host CPU.

Based on National's proven BiFET™ technology, the 8-bit BLC-8715 performs highly accurate A/D conversion in a scant 8µsec.

The BLC-8715 takes care of "front end" measurement and control functions for 16 analog processes plus 22 TTL-compatible functions.

Check box number 039 on this issue's coupon for additional information on the Practical Wizards' intelligent control board.

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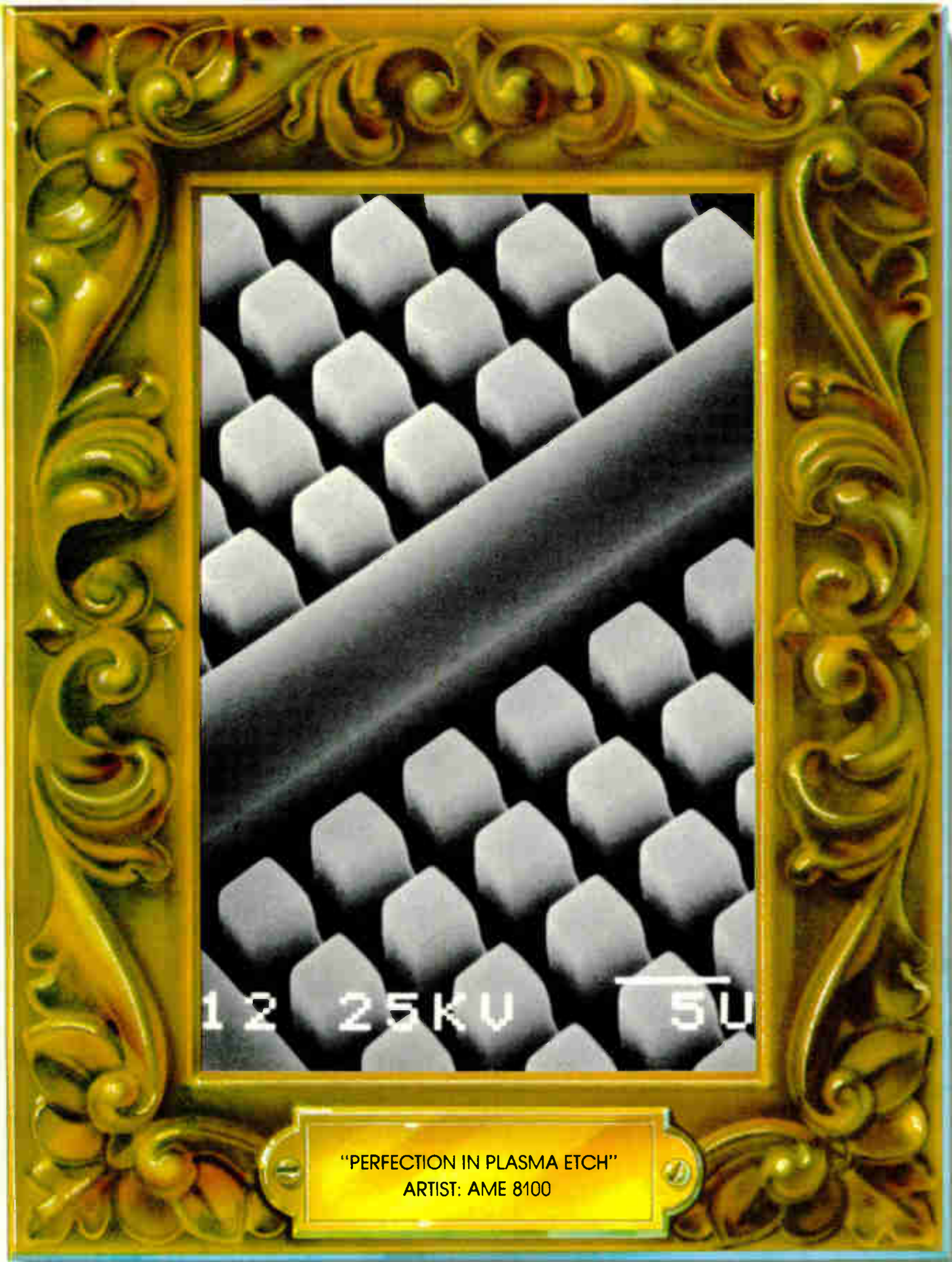

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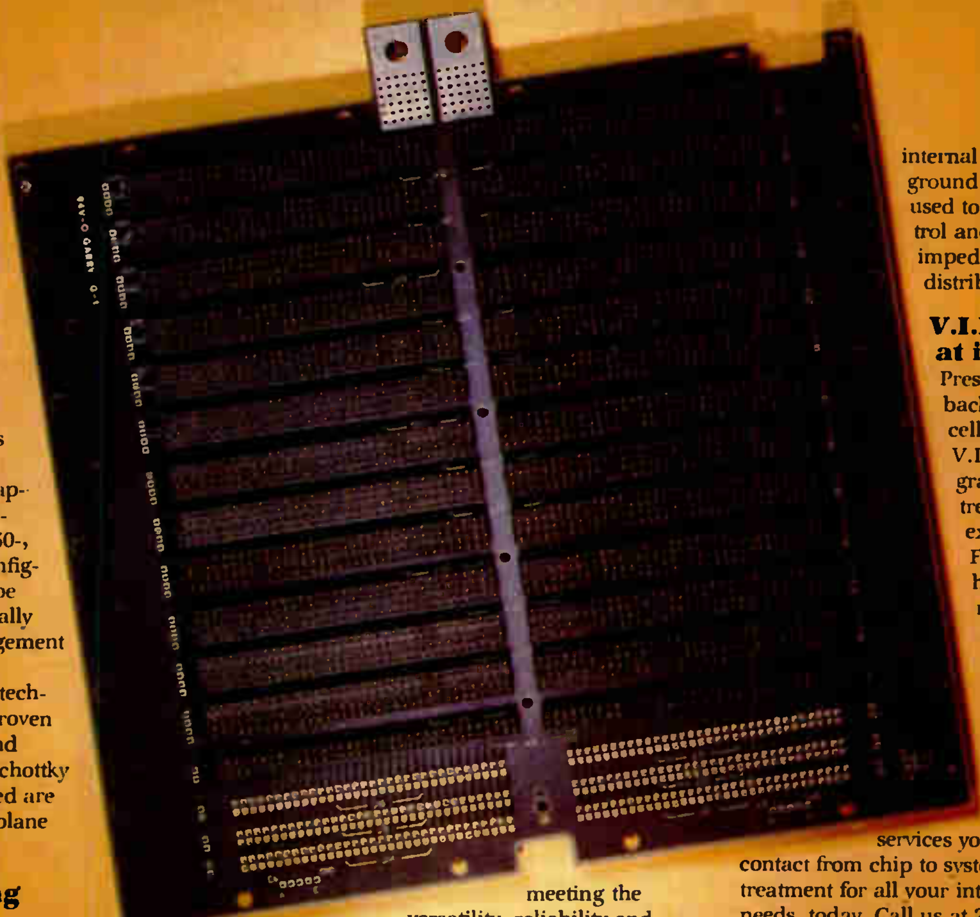

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Technology is the answer

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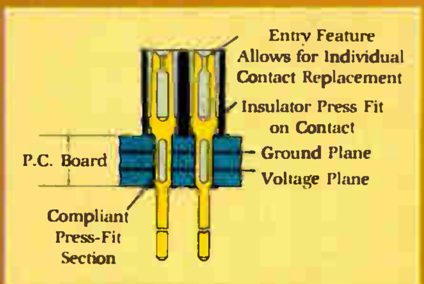

Press-Fit Compliant Contacts—Garry's compliant contact design provides broad contact area and constant contact tension for reliable electrical and mechanical press-fit performance. Beryllium copper (per QQ-C-533) construction, alloy 172 spring temper, gold plated per MIL-G-45204.

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Instruments

Functional tester checks 8080, 8085

Low-cost benchtop tester handles peripheral chips, too, reads out failure code

Considering the cost of sophisticated equipment for testing complex microprocessors and peripheral devices, it is understandable why many low-volume users of these devices do not do their own incoming inspection. Instead, they have had to pay for a costly outside testing service or forget testing altogether in the hope that these complex devices function well in their equipment.

Thanks to engineers at Data I/O Corp., small-quantity users of Intel's 8080 and 8085 families now have another choice. Data I/O has developed a low-cost benchtop unit that tests these 8-bit microprocessors before they are assembled onto boards, where faults are more difficult and costly to locate and repair.

Real environment. Most microprocessor problems are related to a functional failure, notes Ed Dobbyn, product manager. The 1510A benchtop tester detects functional problems by operating the device in a real circuit environment at full rated speed and with the device's outputs resistively loaded. The tester operates the supply voltage at high, low, and normal levels, which may trigger a failure that is inherent in the device.

The 1510A determines the functioning of a device under certain worst-case conditions and tells the operator whether or not it will operate as specified, says Dobbyn. It can be operated in a continuous test mode that repeats the test until a failure occurs. This mode can be used to check out the device for intermittent or temperature-related failures, if such are suspected.

Since most device vendors require some failure analysis or proof that the device failed in use before they will accept returned parts for refund or replacement, the benchtop tester indicates which function failed by displaying a three-digit error code. For example, a displayed number may indicate that the chip's clock is inactive, that an address line is not functioning, or that the internal random-access memory is defective.

Unlike many more expensive and complex testers, the 1510A can be operated by production line personnel, Dobbyn says. The operator need only plug in the correct test adapter for the device to be tested, insert the part, and push a single button.

Traffic light. Testing takes less than a second (typically 200 ms). The front panel will display a green pass light if the device is good or a red fail light, along with a diagnostic message, if it is faulty.

Also unlike many of the more expensive testers, "the model 1510A requires no user programming," Dobbyn maintains. All device-specific instructions for performing a full series of functional tests are contained in the corresponding adapters. Initially, Data I/O will offer with the model 1510A test adapters for Intel's 8080A and 8085A microprocessors, as well as for that firm's 8251A programmable communications interface and 8255A programmable peripheral interface. Plans call for adding test adapters for other 8080 family members, as well as for Zilog Inc.'s Z80.

The 1510A is actually Data I/O's second entry into the low-cost tester marketplace for microprocessors. An earlier model, the 1500A tester, is for Motorola Semiconductor's 6800 family of microprocessors and peripheral devices.

Although the 1510A is intended primarily for incoming inspection, Dobbyn says, "another application of the easy-to-operate unit is in testing devices that have been removed as suspects in troubleshooting." Expected to be available for customer demonstrations in the third quarter of this year, with first shipments slated to occur in the fourth quarter of this year, the model 1510A is priced at $3,695. Each test adapter costs $275.

Data I/O Corp., P. O. Box 308, Issaquah, Wash., 98027. Phone (206) 455-3990 [351]

Tester moves from 2 to 4 MHz

Hardware and software upgrading ups throughput as much as eight times

With the application of faster microprocessors and memories moving the clock rate of boards up to 4 MHz, Computer Automation is introducing an upgraded version of the Capable 4900 board tester that can handle them. Not only can the revised version work at double the clock rate of previous testers, but its new central processing unit and software will move boards through production testing much faster than before.

To double the speed of the upgraded system, which will be unveiled for the first time at the Ninth Semiannual Automatic Test Equipment Seminar and Exhibit in Boston next week, CA replaced the 4-K-by-4-bit, 250-ns random-access memories behind each test pin with RAMs that access in 50 ns.

With these devices able to supply test vectors with a resolution of 25 ns, the company also had to redesign the program stack of the microsequence controller, which schedules and activates each test cycle and the events within it. The replacement,

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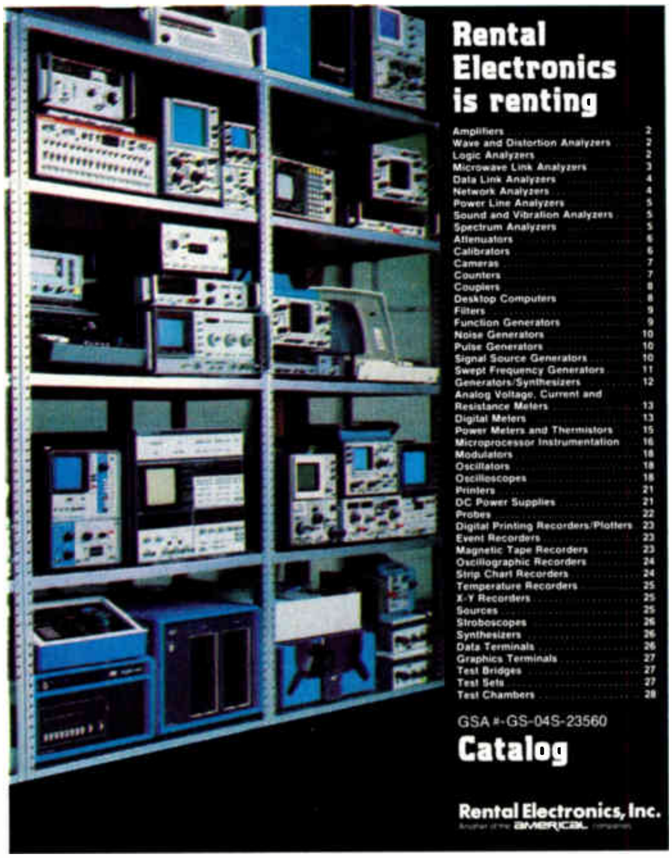

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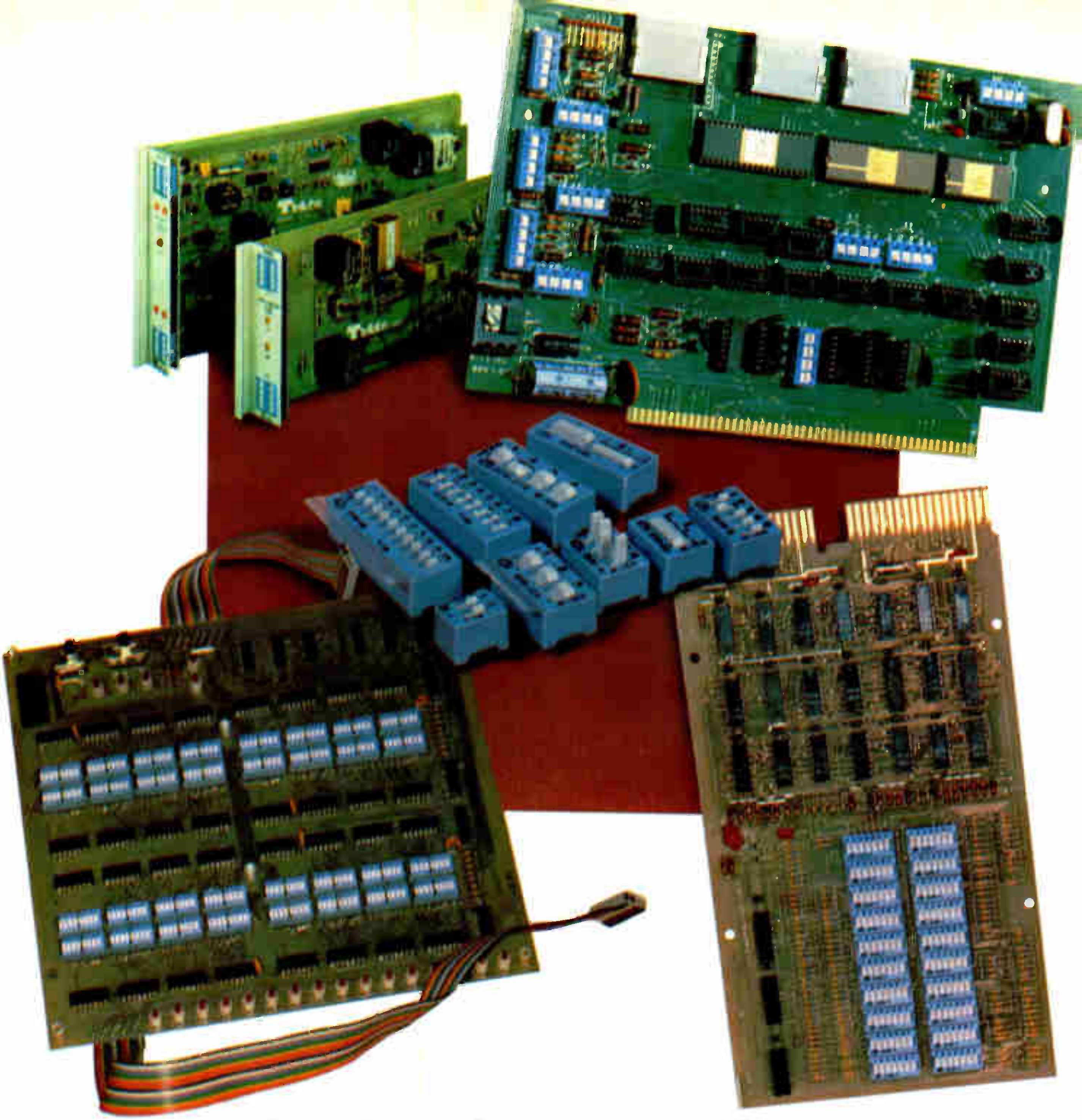


called a program-stack emulator and built on a piggyback card, "lets the test program go at 4 MHz with no difficulty," notes Rick Henninger, products marketing manager for CA's Industrial Products division.

"For boards that rely heavily on bidirectional buses," he says, "the upgraded system can increase throughput as much as eight times." That increase is due to two factors: use of both a new CPU and a new executive program.

CPU power. The CPU is the company's LSI-2/120, introduced by the Naked Mini division last year. It alone increases throughput by 1.8 times, regardless of the need for bidirectional test pins. Called the Super 2, it will become the standard CPU for the entire 4900 family later this year.

The upgraded executive software employs a new file structure that changes the way the system handles bidirectional points. Rather than reviewing the individual status of each pin for every cycle of a test program, the executive looks only for a change in pin status. Based on CA's experience, this overhead reduction is providing throughput increase of six to eight times on boards that require heavy use of bidirectional pins, Henninger notes.

He also points out that the system, like others in the series, offers users another way of increasing throughput. "They can run a functional test using only a few test vectors to check that all the components are working right, or they can run a more complex test that exercises the board as it would operate in the final system." These different approaches, referred to as live testing and system emulation, respectively, let the user choose between getting boards tested quickly with little programming effort or increasing the confidence level of the test by a few percent and further reducing system-level faults.

A fully configured 4900 system with 4-MHz capability costs $550,000. Users of existing systems can purchase upgrades at prices ranging from $20,000 to $100,000, depending on whether they want both hardware and software upgrades and on the present system configuration. Delivery is within 90 days of receipt of order.

Computer Automation Inc., Industrial Products Division, 2181 DuPont Dr., Irvine, Calif. 92713 [352]

Digital multimeters beep to verify continuity

Beckman Instruments' range of digital multimeters now includes models 3020B, 3050, and the RMS 3060. The 3020B is a portable meter that displays continuity by emitting a beeping sound or by illuminating an ohm sign on its liquid-crystal display. It has an easy-to-use single center selector switch, 0.1% basic dc accuracy, a battery life of 2,000 hours from a standard 9-V battery, semiconductor test functions, 10-A ac and dc current ranges, and is protected against overloads. It is available from stock for $189 in the U. S.

The models 3050 and RMS 3060 are bench-top 3½-digit multimeters with visual and audible continuity indication. They feature a single center rotary switch that selects 31 ranges in eight different functions, a battery life of 12,000 hours, 0.1% basic dc accuracy, and built-in resistance range protection. The 3050 sells in the U. S. for $229. The RMS 3060 has true root-mean-square and temperature measuring capabilities and costs $289.

Beckman Instruments Inc., 2500 Harbor Blvd., Box 3100, Fullerton, Calif. 92634. Phone (714) 871-4848 [353]

Low-cost nonintrusive tester monitors IEEE-488 bus

As everyone knows by now, getting a system based on the IEEE-488 interface up and running is not all sweetness and light. Racal-Dana is introducing its first tester for the bus—an inexpensive unit called the model 488 GPIB analyzer.

What separates this $895 unit from other bus testers is the fact that it can be totally nonintrusive, letting the system work as if the tester were invisible. This was accomplished by buffering the analyzer's interface and avoiding any controls that could inadvertantly effect the data flow. Further, the unit is battery powered, so ground loops and power-line noise, which could effect a system's operation, are avoided.

The analyzer has three operating modes: passive, single-step, and trace. In the passive mode, the unit monitors bus activity, displaying the status of data input/output lines in hexadecimal and individually annunciating the housekeeping and handshake lines' status. In the single-step mode, the analyzer can control data transfer byte by byte by taking over the handshake line.

The trace mode activates a 40-word memory for accumulating data during normal bus activity. Trigger-condition controls allow the data to be captured before, after, or on both sides of a trigger event, a particularly useful troubleshooting feature. The trigger feature can also be used to switch from passive to single-step mode. The instrument is available in 30 days.

Racal-Dana Instruments Inc., 18912 Von Karman Ave., Irvine, Calif. 92713. Phone (714) 833-1234 [358]

15-, 20-, 40-, and 45-MHz units join oscilloscope line

Six oscilloscopes featuring state-of-the-art internal circuitry, bright displays, and high efficiency have been introduced by North American Soar Corp.

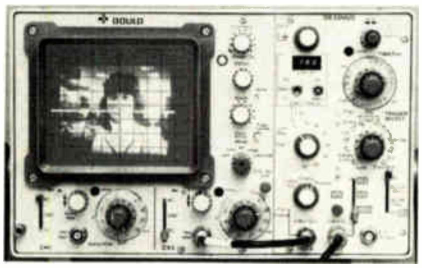
Model 3015 is a 15-MHz dual-trace portable unit with a 3¾-in. cathode-ray tube. It weighs only 10 lb, has 5× magnification, and includes a built-in rechargeable battery pack. The model 6020 is a 20-MHz bench-top unit with a 5½-in. CRT. It has 2-kV beam acceleration for bright waveform displays. Model 6021 is similar to the 6020 but has a delayed trigger sweep of 100 ms to 1 μs in five steps with variable control. The model 6120, also similar to the 6020, has a five-function 3½-digit multimeter. A 40-MHz dual-trace unit with a 6-in. CRT, 5-mV/division sensitivity, and 15-kV acceleration is model 6040. Finally, there is a 45-MHz dual-trace unit, model 6045, similar to the 6040 but with a sweep delay of 100 ms to 1 μs in five steps with variable control.

These oscilloscopes are priced at $849, $699, $749, $799, $1,395, and $1,695, respectively, in quantities of 1 to 9. In quantities of 10 or more, their prices are $720, $595, $636.35, $680, $1,185.75, and $1,441, respectively.

North American Soar Corp., 1126 Cornell Ave., Cherry Hill, N. J. 08002 [354]

40-MHz dual-trace scope monitors television signals

The Gould OS3350/5 TV monitor oscilloscope performs the functions of an NTSC 525-line waveform and picture monitor and a general-purpose 40-MHz dual-trace oscilloscope. It is used for testing and troubleshooting community-antenna television, closed-circuit television, video recording and playback, and other video equipment in mobile-TV, microwave, repeater, broadcast-station, institutional, plant, and production-line applications.



The oscilloscope contains a time-base generator allowing the 525-line waveforms to be examined line by line in addition to displaying complete pictures. A multiturn vernier control provides triggering delays of up to 90 μs, so sections of a line may be examined. It accepts standard-level composite video signals and offers five triggering modes.

The Gould OS3350/5 is priced at $4,395. Delivery is in 30 days after

receipt of a customer's order.

Gould Inc., Instruments Division, 3631 Perkins Ave., Cleveland, Ohio 44114. Phone (216) 361-3315 [355]

Unit converts optical input into calibrated voltage

The model 1500 XP optical waveform analyzer converts optical input signals from light-emitting diodes, lasers, and fiber-optic cables into electrical signals. The unit is calibrated in millivolts out per microwatt in, and has four ranges: 1, 10, 100, and 1,000 mV/μW.

The analyzer is self-contained and has an output BNC connector that plugs directly into an oscilloscope, analyzer, or voltmeter. It has a frequency response of dc to 200 MHz, and a typical rise/fall time of 2 ns.

The 1500XP, which runs on internal batteries to keep noise at a minimum or an external ac supply, is priced in the U. S. at $985 for a single unit. Delivery is from stock and takes two weeks.

Photodyne Inc., 948 Tourmaline Dr., Newbury Park, Calif. 91320 [356]

Phase meter also acts as phase generator

Designed to be used with a voltage and current source to calibrate wattmeters, phase-angle meters, and power-factory meters is the Phase Generator/Meter model 809. It functions as a generator with two output voltages whose relative phase setting is determined by the operator and as a phase meter for measuring the phase angle between a voltage and current applied to a load. Phase measurements are indicated by a 3½ digit display with a 0.1° resolution and an accuracy of ±0.5° from 50 to 450 Hz and ±1.0° from 451 to 1,000 Hz. Generation is at 50, 60, 400, or 1,000 Hz. It is priced at $1,490 and delivery will take three to four weeks after receipt of order.

RFL Industries, Powerville Road, Boonton, N. J. 07005 [357]

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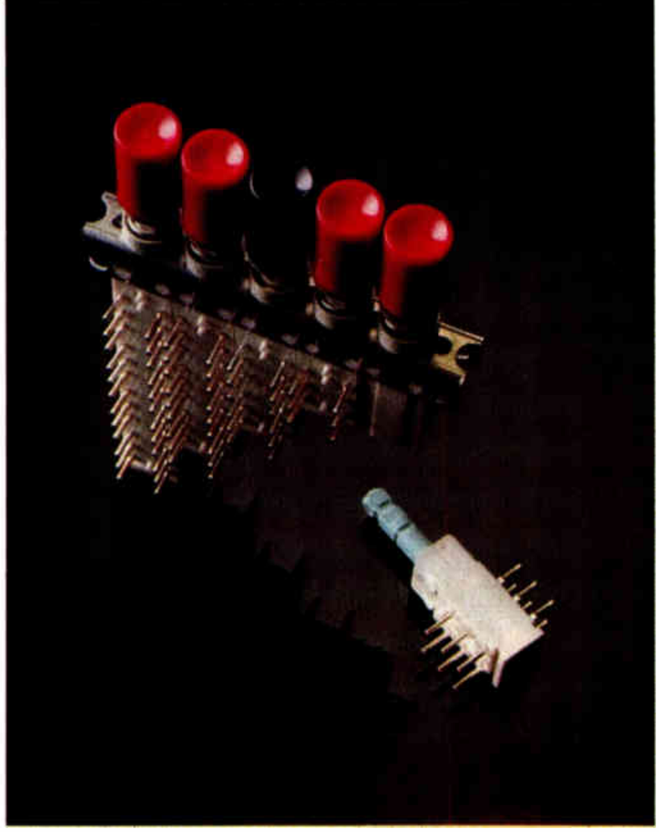

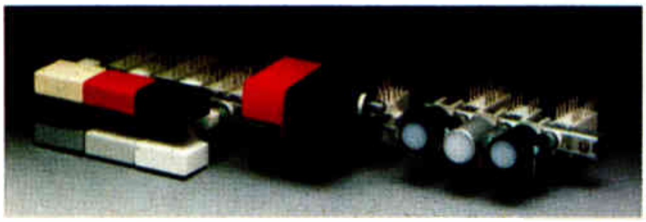

Circle 123 on reader service card

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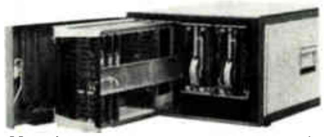

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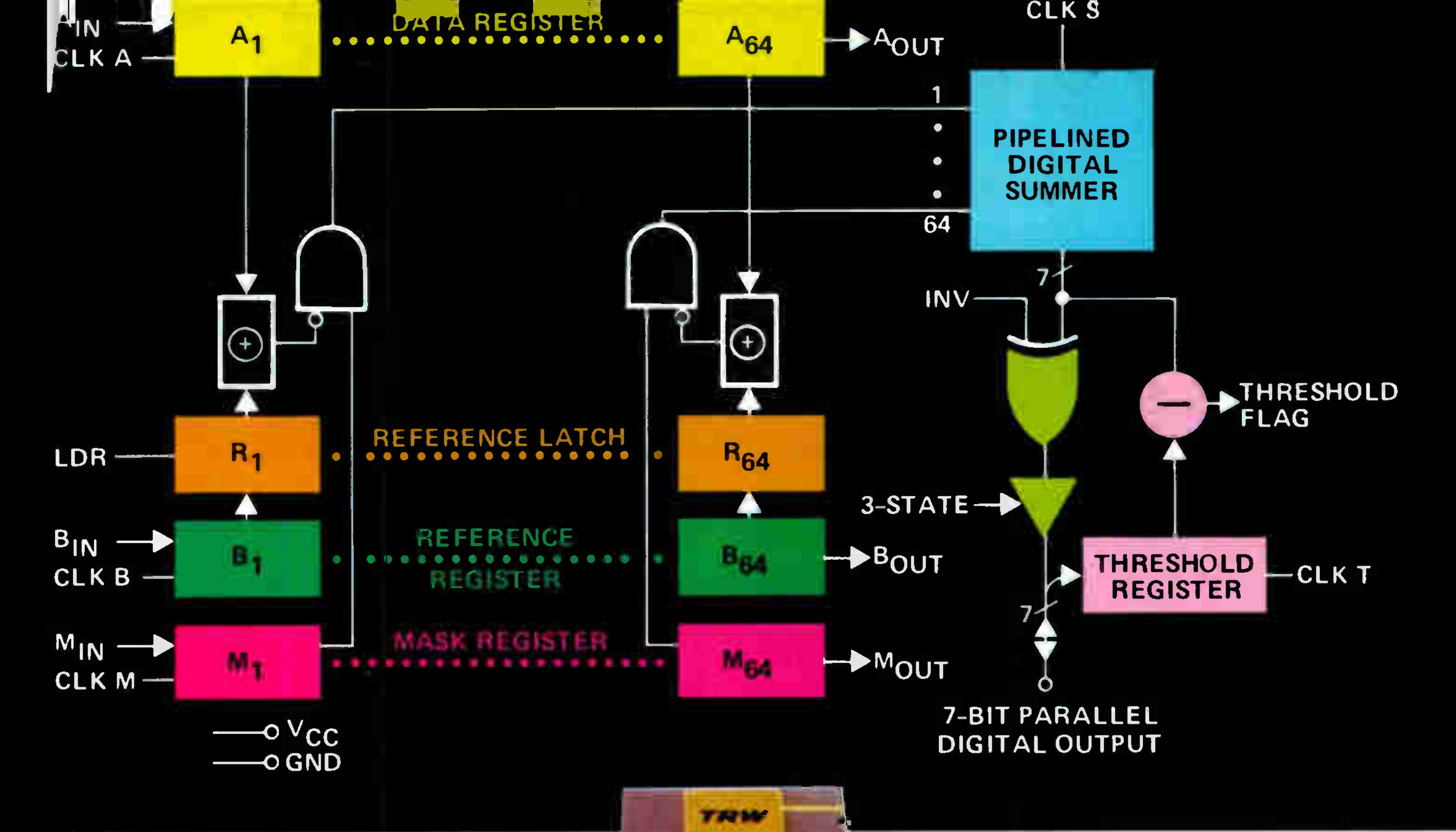

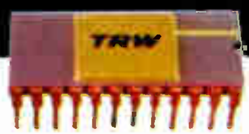

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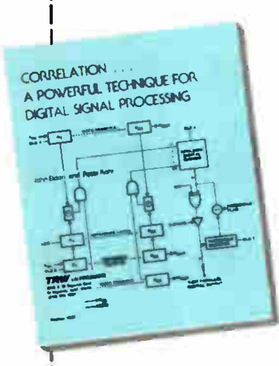

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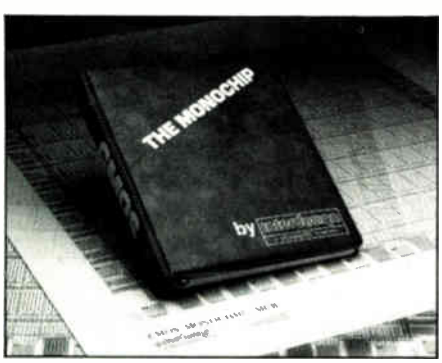

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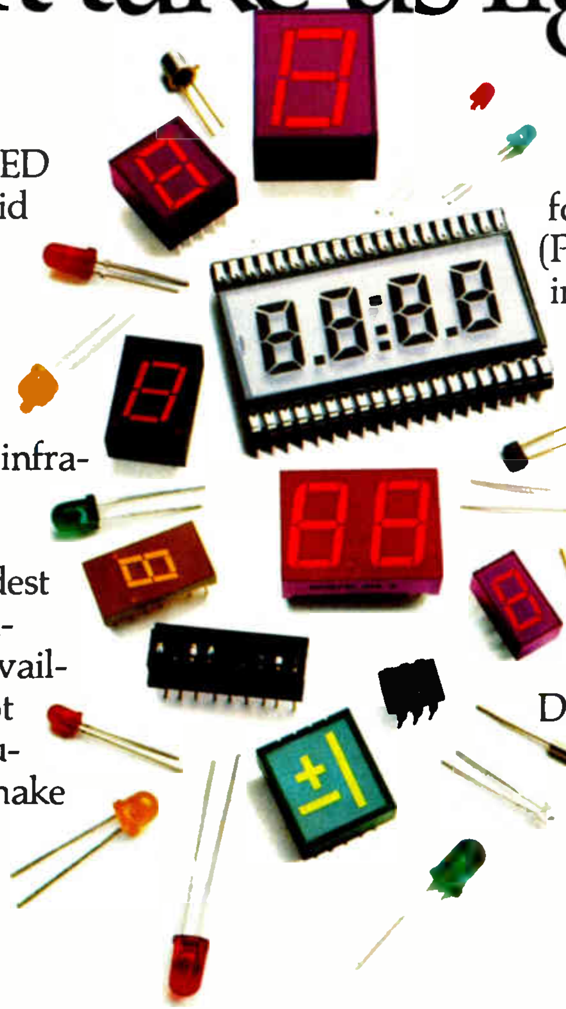

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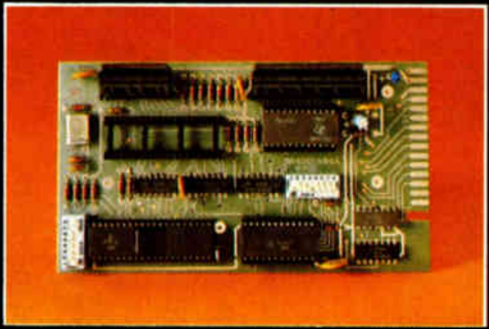

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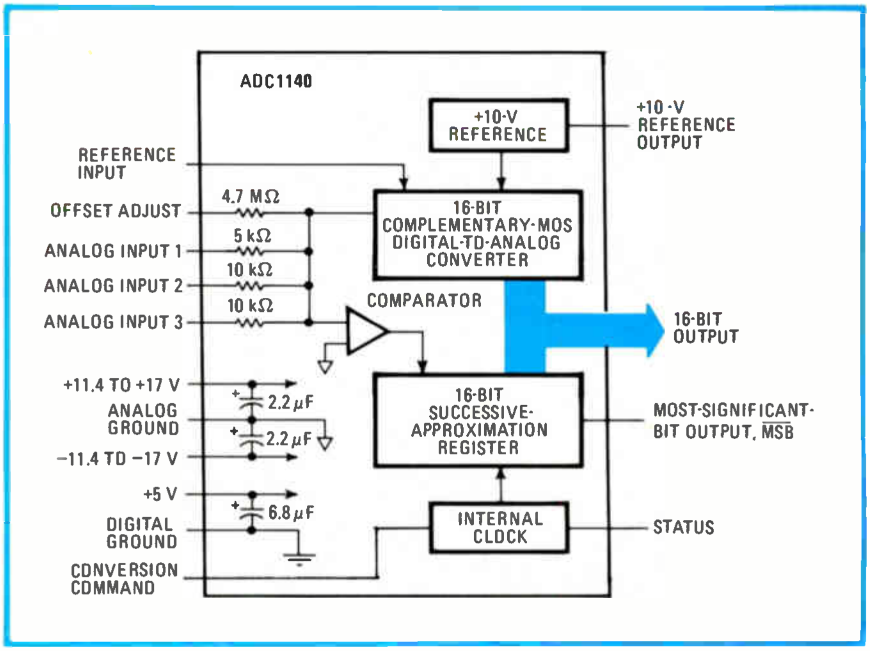
Components

16-bit a-d unit converts in 35 μs

Low-cost analog-to-digital converter made with C-MOS tolerates wide supply range



C-MOS switches. The ADC1140 16-bit analog-to-digital converter makes extensive use of complementary-MOS for low power use and wide supply and temperature tolerances.

Using a modular approach to pull down the cost of converting an analog signal with 16 bits of resolution, Analog Devices has managed to offer short conversion time, low temperature coefficients, and wide supply-voltage range as well. The ADC1140 costs $199 in single units, $149 in hundreds.

The 1140 converts in a maximum of 35 μs, which surpasses all but the top-end 16-bit successive-approximation converters from Zeltex Inc., which cost several times as much. Maximum nonlinearity (and differential nonlinearity as well) in Analog Devices' converter is ±0.003% of full-scale range at 25°C, which, again, is only beaten by the princely converters. Another respectable figure is the temperature coefficient of its linearity: a maximum 2 ppm/°C.

The ADC1140 module is 2 by 2 by 0.4 in. Its design includes proprietary thin-film resistors and complementary-MOS current-steering switches, a low-noise reference, a low-power comparator, and low-power successive-approximation registers.

The extensive use of C-MOS in the 1140 proves to be an asset in several ways. Power dissipation is relatively low—typically 1.25 W—and a low-power version can soon be expected that will drop that to less than 1 W. C-MOS's tolerance to temperature change helps give the 1140 its low temperature coefficients, including a maximum change in gain of only 12 ppm/°C. What's more, the specified temperature range of from 0° to 70°C will soon be extended to from −25° to +85°C, says the firm.

Finally, C-MOS helps make possible a wide power-supply range in the 1140: whereas all other such a-d converters restrict the ±15-V supply to ±3%, the 1140 allows an unprecedented range of ±11.4 to ±17 V. "That will give the 1140 entry into many new areas, especially poorly regulated and battery-powered applications," explains Ted Serafin, marketing engineer of new product development at Analog Devices.

The 1140 offers four pin-selectable input ranges—from 0 to +5 or +10 V and ±5 or ±10 V—the same ranges offered by its primary competition, Burr-Brown's ADC 72. The Burr-Brown part, a hybrid housed in a 32-pin dual in-line package, operates over a wider temperature range but costs slightly more and is edged out in conversion speed by the ADC1140.

Analog Devices Inc., Route 1 Industrial Park, P. O. Box 280, Norwood, Mass. 02062 [339]

D-a converter mimics log curve

8-bit companding IC puts out a straight-line approximation of a logarithmic curve

A monolithic 8-bit companding digital-to-analog converter that is accurate to 12 bits in most applications has been developed by engineers at Precision Monolithics Inc. An outgrowth of the first companding d-a converter, pioneered by PMI four years ago as part of a codec, the DAC-78 is intended for use in industrial applications requiring a wide dynamic range, fast settling time, and low cost.

The bipolar integrated circuit is a sign-magnitude–coded companding converter. Thus, like its predecessor, the DAC-76, it provides a straight-line approximation of a logarithmic curve rather than a linear response, as is the case with conventional d-a units, explains Bill Pascoe, PMI's senior product marketing engineer for data conversion products.

"It dawned on us that the companding transfer function that the original telecommunications device responded to was also useful in other applications," he says. These include digital recording, speech synthesis,

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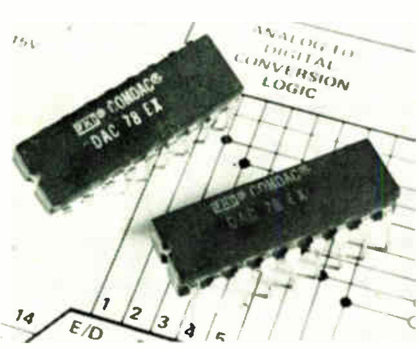
audio attenuation, light-level control, data transmission, and servo positioning systems.

Chords. The DAC-78 has a dynamic range of 72 dB with 12-bit accuracy in chord zero, that is, the first segment or group of linearly related steps (16) in the transfer function that is closest to zero polarity. Such accuracy in the critical low-signal-level areas of the curve makes the DAC-78 especially useful in linearizing outputs from transducers, such as photodiodes, that have logarithmic response characteristics.

Because it has sign-magnitude coding, a multiplying configuration, and a logic threshold that permits interfacing with all logic families—for example, n- and p-channel MOS, complementary-MOS, TTL, and emitter-coupled logic—the DAC-78 is a very flexible d-a converter. It also has the advantage that it does not require the user to perform bipolar offset adjustment or zero scaling.

The DAC-78 offers true output compliance over the range of −5 to +18 V, the same range as that of its predecessor. But whereas the DAC-76 has a settling time of 750 ns to within one step (equivalent to 1 least significant bit in a 12-bit system), the DAC-78 is specified at a 500-ns settling time to within a half step (½ LSB). "Such devices have got to settle in 500 ns or less if they are to keep pace with today's 8-bit microprocessors," Pascoe states. Also, for 12-bit d-a converter applications, he adds, "most designers want accuracy on the order of ½ LSB."

Performance. The DAC-78 has a chord-end-point accuracy of ¼ step in chord zero over the full operating temperature range of −25° to +85°C. Full-scale drift is 1/16 step,



full-scale symmetry error is 1/40 step, and step accuracy is ¼ step. "This performance allows the designer to obtain 12-bit accuracy in most applications," Pascoe says. Thus, rather than buying an expensive ($30 to $40) 12-bit d-a converter, designers now have the alternative of a low-cost 8-bit unit that can do substantially the same job.

The ladder network used in the DAC-78 is designed to produce eight straight-line chords with 16 bits per chord, thereby providing a very close approximation of a logarithimic curve. Tight interval matching between reference input and converter output eliminates the requirement for full-scale adjustment in most cases, he adds.

Paired outputs. Among the more significant features increasing the versatility of the DAC-78 is its two pairs of complementary outputs. One pair is for decoding (d-a applications); the other pair is offset ½ LSB for encoding (analog-to-digital applications). Consequently, a single device can be used in systems requiring both a-d and d-a conversion. For example, with a good comparator, one microprocessor, and one DAC-78, as well as a few resistors and other discrete components, a designer can put together a four-channel data-acquisition system.

When the DAC-78 is used in audio attenuation applications, Pascoe points out, "linearly progressive signals can be put into the device and its output will correspond to a logarithmic curve. Thus, we can convert linear decibels to a log output, instead of taking the conventional approach of going through log amplifiers that typically require several adjustments and are very sensitive to temperature."

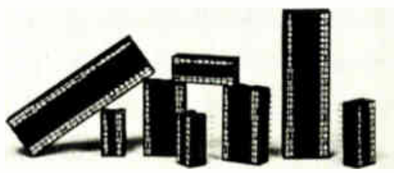
Supplied in an 18-pin hermetic dual in-line package, the DAC-78 dissipates 114 mW with +5- and −15-V power supplies. Available from stock to 30 days after receipt of order, it is priced at $7.50 to $9.00 each in 100-piece quantities, depending on grade.

Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, Calif. 95050. Phone (408) 246-9222 [342]

LED matrix modules aid continuity testing

The Analytyx Light Module features a high density matrix of numbered light-emitting diodes in a hermetically sealed low-profile dual in-line package. In standard form, the LEDs are numbered to correspond with their respective pin numbers; devices with custom nomenclature are also available.

The Analytyx Light Module is



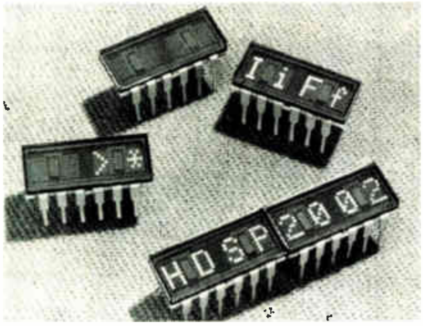
used for fixed-point monitoring on printed-circuit boards and continuity testing of prototype Wire-Wrap boards. They are offered in standard 14- and 48-pin configurations and are typically priced at $29.95 each for a 16-pin configuration in quantities of 25 to 99. Delivery is from stock and specially designed modules are available upon request.

Analytyx Electronics Systems Inc., 1 Executive Dr., Hudson, N. H. 03051. Phone (603) 880-3600 [343]

3.8-mm-high display is useful in bright ambient light

The HDSP-2002 is a low-power, high-efficiency red, four-character solid-state alphanumeric display designed to be used in bright ambient lighting. It features high reliability, a wide viewing angle, uniform display appearance, and on-board serial-in, parallel-out 7-bit shift registers that control constant-current light-emitting-diode row drivers.

The display is TTL-compatible and has a five-by-seven-dot matrix configuration 3.8 mm high. The HDSP-2002 comes in a 12-pin dual in-line ceramic and glass package and sells



for $41 in the U. S. in quantities of 249. Delivery of the alphanumeric display is from stock.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304. Phone (415) 857-1501 [344]

400-Hz toroidal transformers keep a low profile

The Magnetico 13680–13685 line of low-profile toroidal military-grade power transformers are intended to carry loads of 6, 12, or 20 VA. Parts 13680, -82, and -84 are supplied with a 5-V output and 13681, -83, and -85 units have a 15-V outputs.

These 400-Hz transformers range in size from 1 by 1 by 0.62 in. to 2.25 by 2.25 by 0.62 in. Designed for printed-circuit terminal board use, they can also be employed in applications that require transformers which are low in height. Encapsulated and operational at full power rating over a temperature range of −55° to +125°C, the transformers cost from $14 to $16 in quantities of 1,000. Delivery is from stock to two weeks in small quantities.

Magnetico Inc., 182 Morris Ave., Holtsville, N. Y. 11742. Phone (516) 654-1166 [345]

Red and green LED modules come with choice of features

A line of logic display modules has been introduced by Interswitch that includes units with up-down counter inputs, binary-coded decimal inputs, decoders, or built-in memory. These modules have high reliability, a 5-to-24-V range, red or green light-emitting diodes, and can be easily assembled into display blocks.

The logic display modules are compatible with TTL or complementary-MOS and are available in gray or black housings. They can be easily mounted on front panels.

Interswitch, 770 Airport Blvd., Burlingame, Calif. 94010. Phone (415) 347-8217 [346]

Logic-compatible buttons contain ICs, indicating LEDs

The SS01 low profile, printed-circuit mountable single-pole, double-throw switch module provides logic compatibility, bounce-free outputs, and internally connected light-emitting-diode indicators. The custom-designed integrated circuit built into the switch results in high reliability and long life, according to the manufacturer, and allows the switch to be directly interfaced with the user's logic. The SS01's operating mode, alternating or momentary, can be selected by an external jumper.

These push-button switches are available with a variety of replaceable caps in two configurations and eight colors. Round or rectangular factory-assembled LEDs are available in three colors. They have a supply requirement of 3 to 18 V, a temperature range of 0° to 70°C, and an operating force of 100 to 300 g.

C&K Components Inc., 15 Riverdale Ave., Newton, Mass. 02158. Phone (617) 964-6400 [348]

Snap-action switches have turret-type terminals

Now there is a choice of terminals with the series E91, E92, and E93 (which have gold cross-point contacts) line of subminiature switches: sealed or unsealed turret-type terminals and cross-drilled or 0.058-in. Quick Connect pins. The switches are rated at 5 A at 125/250 V ac, 11 A at 125/250 V ac (¼ hp), and 0.1 A at 125 V ac, respectively, and are interchangeable with industry-standard configurations.

The switches are approved by the Underwriters Laboratories and the Canadian Standards Association. They have standard actuators that include external lever, roller, and simulated rollers and are available in two pivot positions for standard- and high-ratio operating forces. Contact arrangements are available in single-pole, double-throw or single-pole, single-throw, either normally opened or closed.

The switches range in price from $2.34 for the basic unsealed button type with a 0.058-in. pin, single or double turret termination ($1.08 each in quantities of 2,000) to $5.50 for the sealed version ($2.53 each in quantities of 2,000).

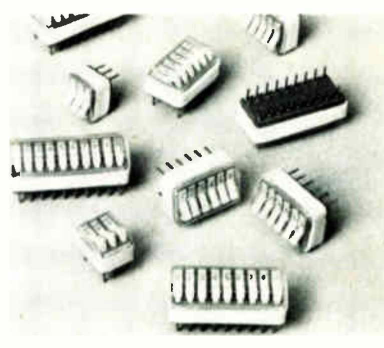
Cherry Electrical Products Corp., 3600 Sunset Ave., Waukegan, Ill. 60085 [347]

DIP switches have flexible cover for complete seal

The 2400 series miniature dual-in-line–packaged switches are to be used with state-of-the-art soldering and cleaning equipment. They can withstand a wide range of temperatures and solvents and are protected against harsh environments: the base is epoxy-sealed and a permanent flexible cover is attached onto the top.

The 2400 series features a gold-on-gold wiping-action contact, 0.020-by-0.014-in. terminals that eliminate insertion and alignment problems, and standard 0.100-by-0.300-in. centers. They are compatible pin for pin with major DIP switches.

EECO Inc., 1601 East Chestnut Ave., Santa Ana, Calif. 92701 [350]



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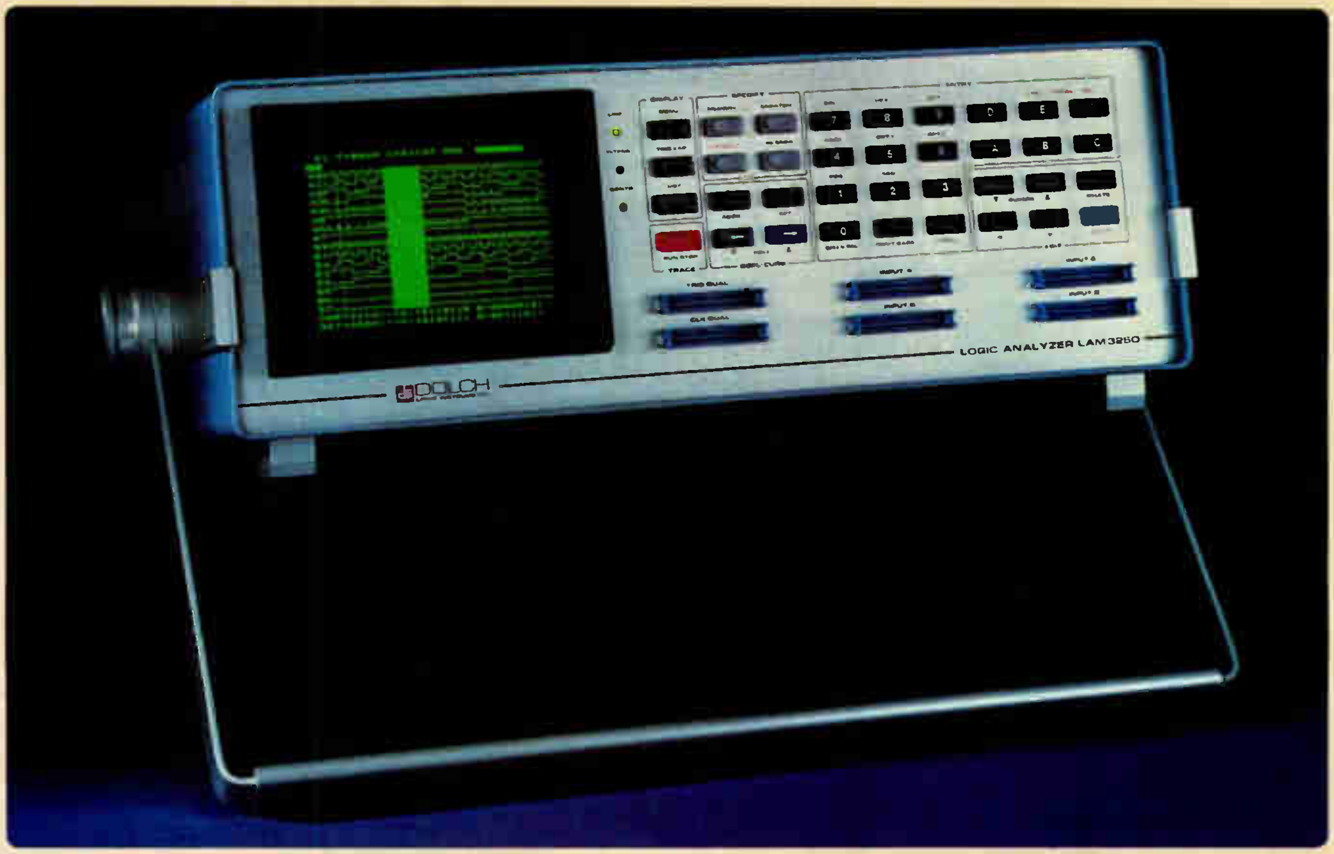
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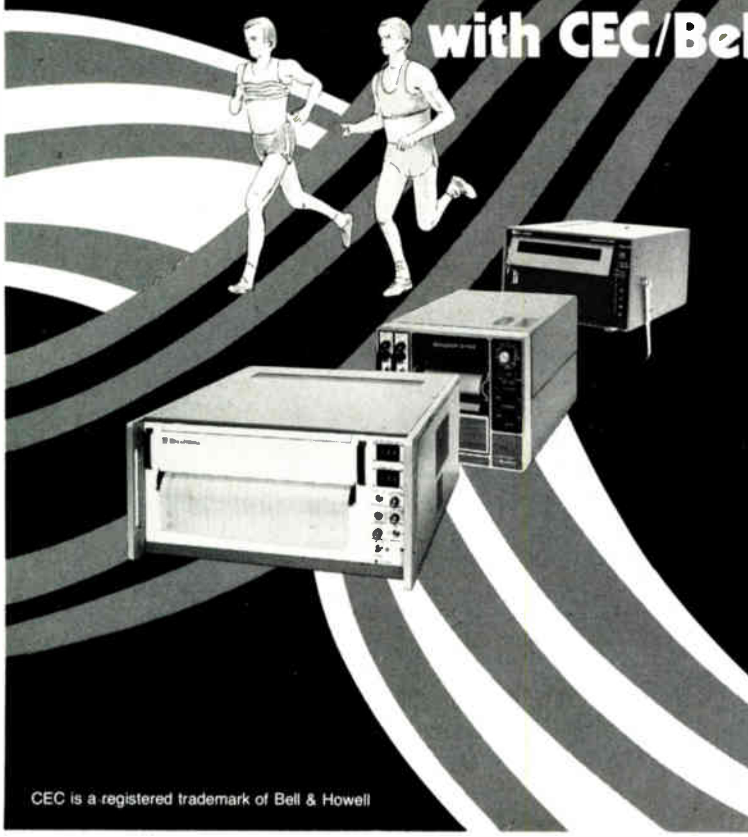

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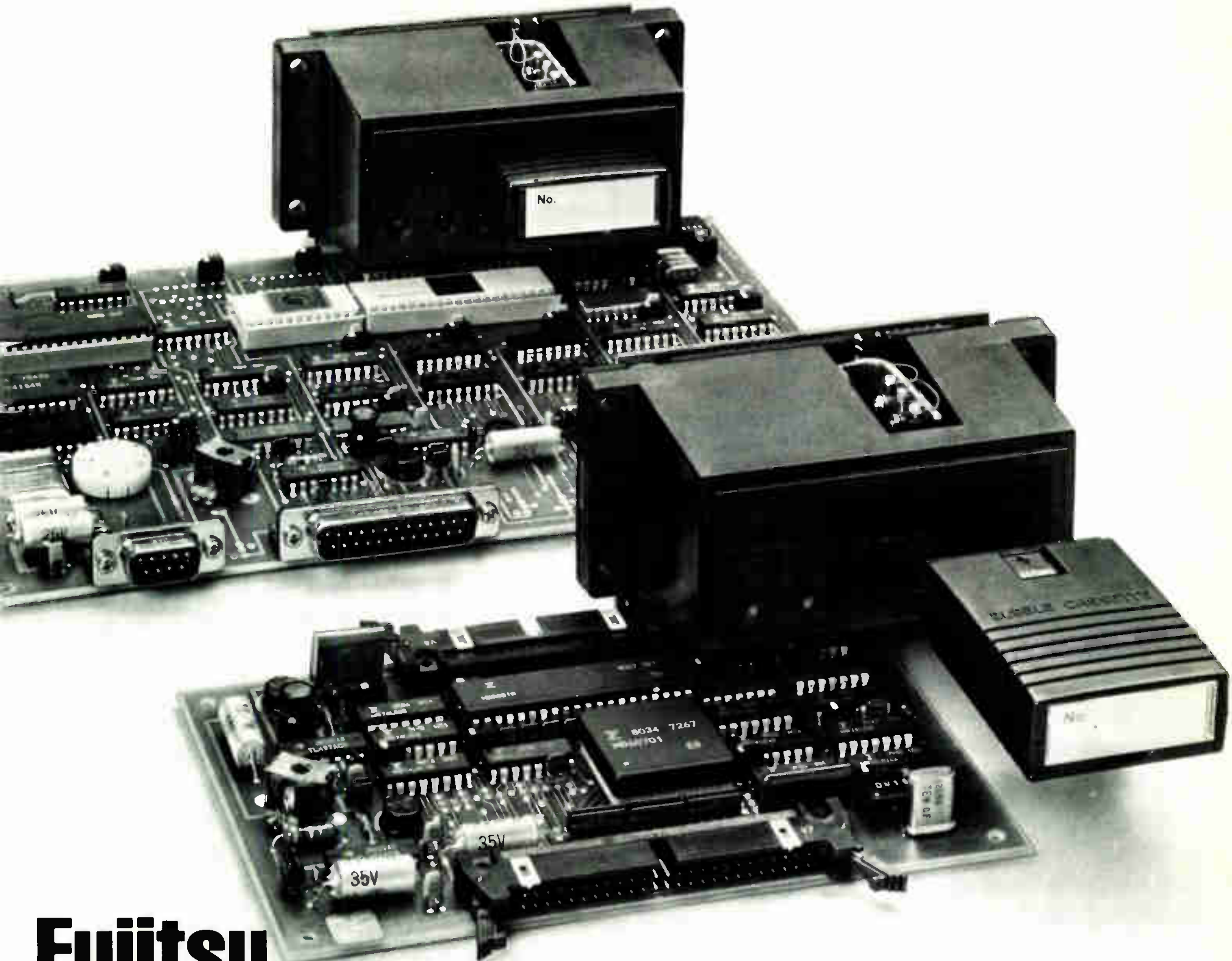

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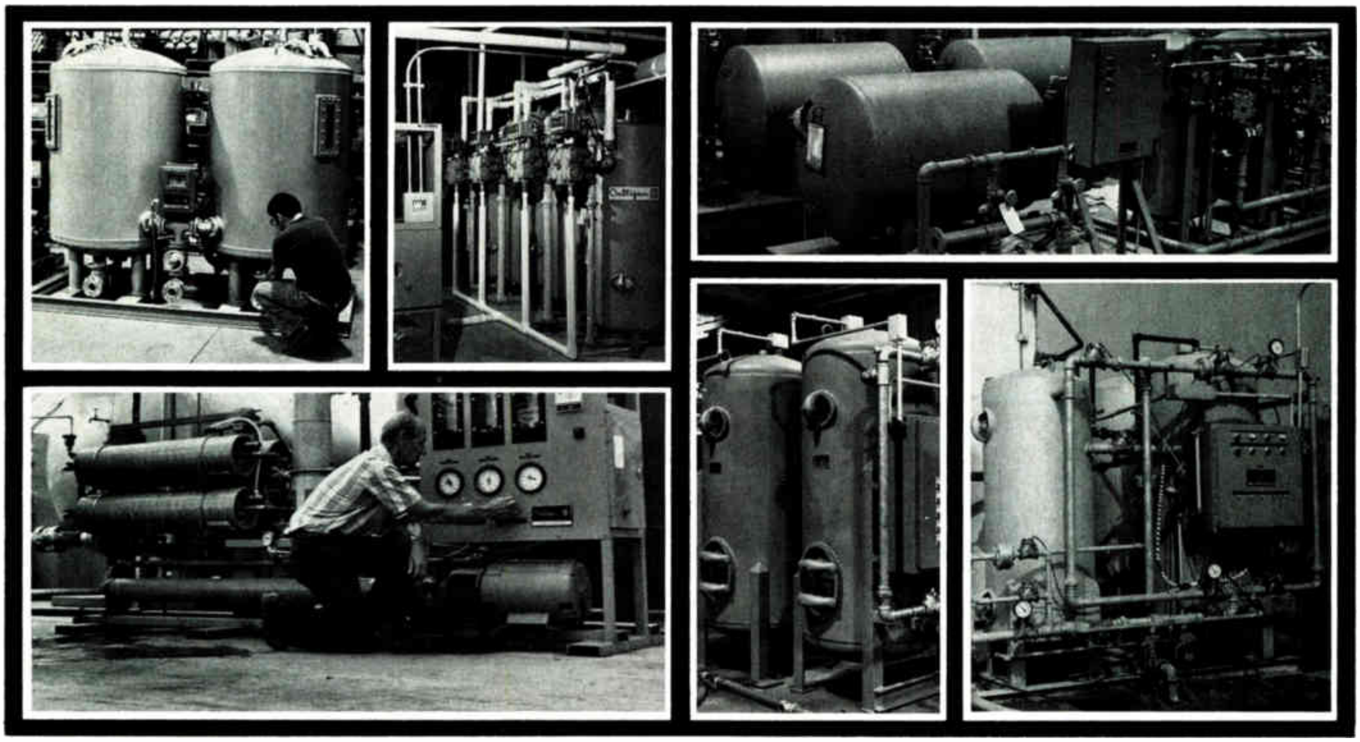

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Packaging & production

Quick Connect is automated

Microprocessor-based system brings semiautomatic wiring to Quick Connect backplanes

The Quick Connect backplane-interconnection system developed in the mid-1970s at Bell Laboratories in Holmdel, N. J., long has been viewed as a successor to Wire-Wrap techniques [*Electronics*, Sept. 13, 1979, p. 98].

The reasons are four: Quick Connect backplanes can be an inch or more thinner than Wire-Wrap planes and use less material; insulation-displacement QC requires no wire stripping before a connection is made; undesired wire runs can simply be pulled out of a backplane (whereas connection removal with Wire-Wrap planes is a real chore); and finally, the Quick Connect system can theoretically connect an infinite string of terminals in series, whereas the Wire-Wrap process can connect only two at a time.

Competition. But the QC system has been prevented from competing with Wire-Wrap because of a lack of automated wiring systems. There are many semiautomatic Wire-Wrap systems available, and a few large, fully automated machines. Now there is a semiautomatic system for the QC process from Computer Numerical Control Corp. The Teach 'n' Run system manages interconnection operations on QC backplanes ranging in size from tiny prototypes to planes 58 by 92 in.

The heart of the system is a microprocessor-based teachable controller. The controller uses a Z80 clocked at 2 MHz and includes a single-sided Shugart 5¼-in. floppy-disk drive and 16-K bytes of MOS static random-access main memory—enough to store the map for 9,600 connections.

A semiautomatic system, Teach 'n' Run first is stepped through its connection and routing pattern by an operator taking advantage of a compact membrane-type keyboard and light-emitting-diode display. The coordinates of each connection are initially stored in memory and relayed to the floppy disk, which can be copied, permitting the operator to program many of Teach 'n' Run systems in a single pass.

Although Robinson Nugent Inc. of New Albany, Ind., the leading vendor of QC terminals and backplanes, is working on a fully automatic wiring head, none is yet available. CNC's semiautomatic system has a positioning jig, which is moved across a backplane to align a hand-held wiring pencil, and an operator makes each individual connection.

But that does not mean that the CNC system is slow. According to George C. Kakridas, president of CNC and a long-time maker of semiautomatic Wire-Wrap systems, QC could be two to three times faster than Wire-Wrap. With a good operator, a semiautomatic Wire-Wrap machine can process 200 to 300 wires per hour; Kakridas calculates that the same operator using a QC rig from CNC could handle 600 to 900 wires per hour. The last figure approaches the 1,000-wire-per-hour nominal rate for fully automated Wire-Wrap machines.

Kakridas says that it now will be possible to distribute output across a number of QC machines rather than having to buy a single, large Wire-Wrap system to achieve a high output level. In addition, if one QC system failed, the others would carry on. He also claims that, for a given output, the capital outlay for the two approaches would be very similar.

Start small. Teach 'n' Run was originally targeted at prototyping applications, and given the normal patterns of market growth, that is where it will sell best at first. The model 100MB, with a maximum panel size of 16 by 23 in. and a maximum wiring area of 12 by 16 in., will be going out the door in greatest numbers at a price of $7,500. Kakridas expects to sell 100MBs for engineering prototype and research and development applications, and because the 100MB's price is low, he expects to penetrate the academic laboratory market.

As the new controller is compatible with CNC's broad line of backplane frames and tool positioners, four other models are available. The 100B handles panels with wiring areas of 24 by 26 in. and costs $10,500. The $12,550 model 1000 can wire a 24-by-39-in. area. The 1000S, at $15,500, has a wiring-area capability of 26 by 45 in. Finally, there is a model that will probably have to be loaded by overhead crane, the 1000SSS, with a wiring area of 52 by 88 in. and priced at $37,500. All prices include the Teach 'n' Run controller.

The company plans to show the system at Nepcon-81 in Chicago on June 16–18.

Computer Numerical Control Corp., 150N New Boston St., Woburn, Mass. 01801. Phone (617) 933-0091 [391]

Connectors stack pc boards for high-density packaging

The Stack-Con connector system makes it possible to stack printed-circuit boards for high-density packaging. Half of a connector pair is soldered to each board; when the two halves are mated, the boards are held rigidly at a 0.510-in. board-to-board spacing. It is available with 18 dual-contact positions on a 0.100-by-0.100-in. contact-spacing grid. The contacts are gold-plated to a thickness of 10, 20, or 30 μm and have a 3-A maximum current rating.

The connectors are made of a flame-retardant nylon. A minimum contact-retention force of 3 lb and a minimum connector-unmating force of 4 lb make it useful in systems liable to severe shock and vibration. In addition, it has an ambient temperature range of −55° to +85°C, a dielectric strength of 1,000 V root mean square, minimum insulation resistance of 1,000 MΩ, and a maximum contact resistance of 0.010 Ω.

Stack-Con is priced at 18¢ per line for a mated pair—plus an additional amount based on the gold-plating

The Texas Instruments News

TI'S POPULAR PROM FAMILY

	NUMBER	ORGANIZATION	TYPICAL ADDRESS ACCESS TIME	TYPICAL POWER DISSIPATION
256 Bits	TBP18S030 TBP18SA030	32 x 8	25 ns	400 mW
1K	TBP24S10 TBP24SA10	256 x 4	35 ns	375 mW
2K	TBP28L22 TBP28LA22	256 x 8	45 ns	375 mW
4K	TBP28S42 TBP28SA42	512 x 8	35 ns	500 mW
	TBP28S46 TBP28SA46	512 x 8	35 ns	500 mW
	TBP24S41 TBP24SA41	1024 x 4	40 ns	475 mW
8K	TBP28S86-60 TBP28SA86-60	1024 x 8	35 ns	550 mW
	TBP28S86 TBP28SA86	1024 x 8	45 ns	625 mW
	TBP28L86	1024 x 8	65 ns	275 mW
	TBP24S81-55 TBP24SA81-55	2048 x 4	35 ns	550 mW
	TBP24S81 TBP24SA81	2048 x 4	45 ns	625 mW

A = Open Collector; L = Low Power

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Three 8K headliners

For outstanding speed, try these TI 8K PROMs: the TBP24S81-55 and TBP28S86-60. Typical address access time: 35 ns; max address access times: 55 ns and 60 ns, respectively.

To conserve space, TBP24S81-55 comes in a 300-mil wide, 18-pin package requiring 60% less board room than the industry-standard 600-mil wide, 24-pin package.

To save power, TI's TBP28L86 8K features typical power dissipation of only 275 mW — about 50% less than TI's standard high-speed PROMs — yet is one-third faster than similar devices currently on the market.

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Redesigned lower-density PROMs now offer up to 20% faster max address access times and reductions of as much as 35% in power consumption. Included are TI's popular 1K; a low power 2K; two 512x8 4Ks; the 1024x8 24-pin 8K.

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On the way from TI: 16K PROM with a typical address access time of 35 ns, as well as Registered Output and Power-Down PROMs. For all the news about TI's big PROM family, call your TI distributor, or write Texas Instruments Incorporated, P. O. Box 225012, M/S 308, Dallas, Texas 75265.

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Circle 212 on reader service card

thickness—in original-equipment manufacturer quantities. Delivery takes six to eight weeks after receipt of order.

Viking Connectors Inc., 21001 Nordhoff St., Chatsworth, Calif. 91311. Phone (213) 341-4330 [394]

Wire-processing unit cuts, strips, and applies wires

The Olympian model 700 is a fully automatic integrated wire-processing system that cuts wires to selected lengths, strips the insulation off both ends, crimps terminals on both ends, automatically stacks the wire leads at a rate of up to 5,000 leads (10,000 terminations) per hour, and needs little attention from the operator.

The model 700 features a precision interchangeable crimper that snaps in and out of the system, allowing the operator to change wire gauges and terminal types in minutes. It has a detector that shuts the machine off immediately in the event of a problem, a knob that controls the cutting depth of the stripper blades to accommodate a variety of wire sizes, automatic batch processing dials that ensure a proper count, and automatic shutdown at the end of a job.

DuPont Co., Berg Electronics Division, New Cumberland, Pa. 17070 [393]

Test system performs data analysis

The T357 discrete semiconductor test system performs wafer probing, final testing, quality assurance, incoming inspection, or device evaluation for a variety of devices—including bipolar transistors, diodes, silicon controlled rectifiers, triacs, field-effect transistors, optical couplers, and transistor and diode arrays.

The system has a 64-K memory for a high throughput and dual 3M Co. tape drives. It also comes with a comprehensive software package that can be used by inexperienced personnel, on-line help lists, im-

proved debugging capability, and data-reduction capabilities that furnish summaries, histograms, and cumulative curves for quality control.

The T357 sells for $80,000.

Teradyne Inc., 183 Essex St., Boston, Mass. 02111. Phone (617) 482-2700 [397]

Dissipater is designed for 40-pin dual in-line packages

The E155-001CB dissipater for 40-pin dual in-line packages occupies a minimal amount of space while transferring heat effectively, thus increasing the device's reliability. A thermally conductive epoxy bonds the 001CB directly to a microprocessor chip, obviating the need for any extra hardware and hence any interference with DIP sockets.

Pinout identification is provided by two ribs on the last radial fin at one end of the dissipater. Once it is bonded to the chip, the ribs help insert the device properly into a circuit-board socket.

International Electronic Research Corp., 135 West Magnolia Blvd., Burbank, Calif. 91502 [395]

Plasma etching system processes 50 wafers per hour

The D&W model 5000 cassette-to-cassette microprocessor-controlled plasma etching system simultaneously etches polysilicon and silicon nitride on multiple wafers at sequential stations. It processes 50 5-in. wafers per hour and automatically detects the end point at the final etching station.

The double-load-lock automatic system requires a minimum of utility hookups and can be operated by using only one button. It occupies less than one half the floor space required by competitive equipment, says the manufacturer.

The model 5000 is priced at $92,000 to $120,000. Delivery takes five months.

Eaton Corp., Semiconductor Equipment Operations, 3500 Garrett, Santa Clara, Calif. 95050 [396]

Gold-finish IC sockets are low in price

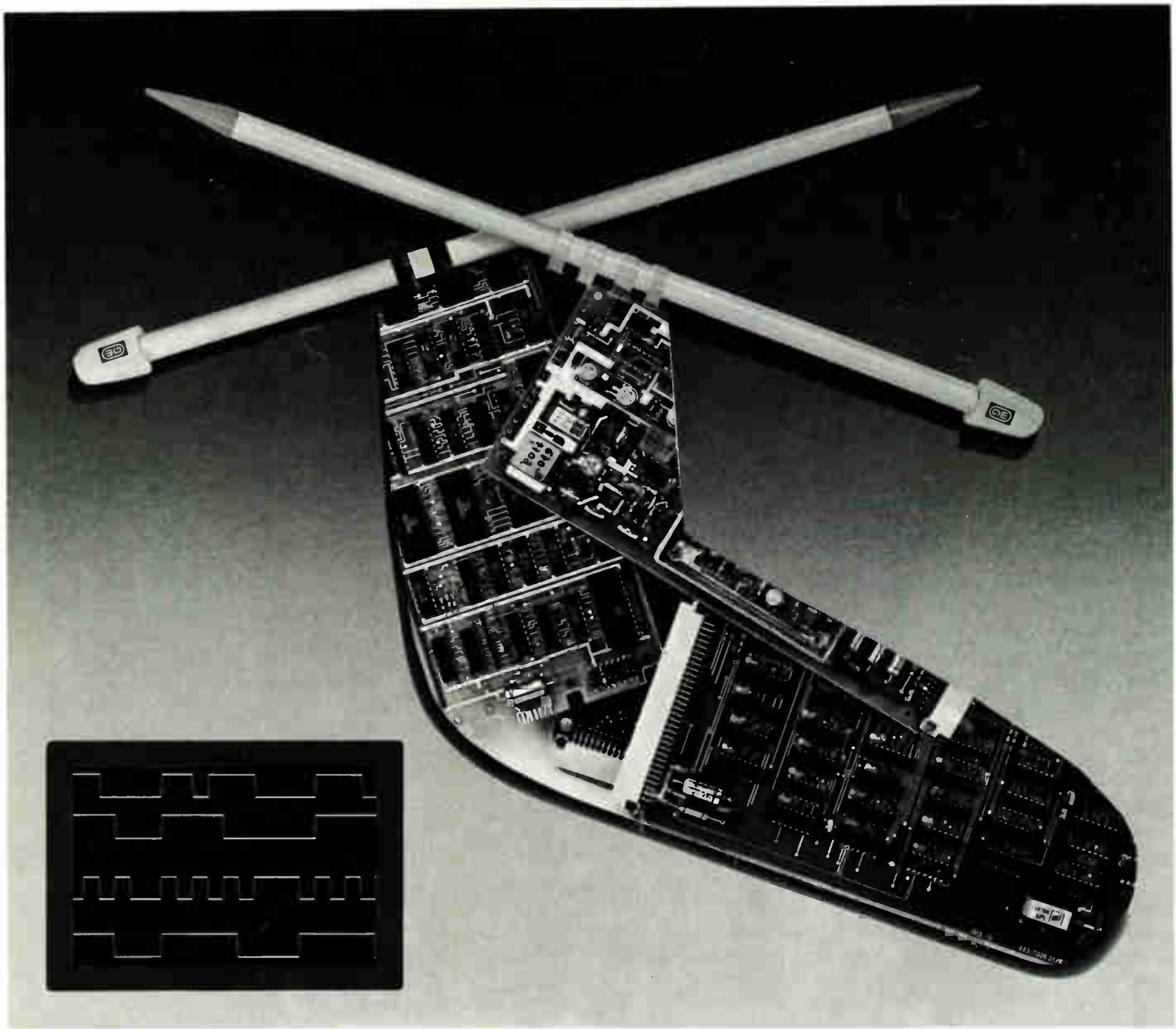
The C72 and C71 series of integrated-circuit sockets, with solder-tail or Wire-Wrap leads, respectively, are 20% lower in price than comparable sockets. When placed end to end, they can accept any pin-socket combination—for example, two 14-pin sockets holding a 28-pin IC.

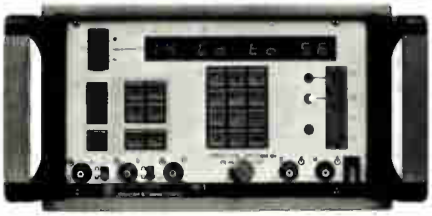
The IC sockets' contacts have a gold-over-nickel finish, making them suitable for use in military equipment, computers, or equipment where corrosion is a problem. The solder tails are optionally available with finishes of gold over nickel or tin and lead over nickel, which are for less demanding applications.

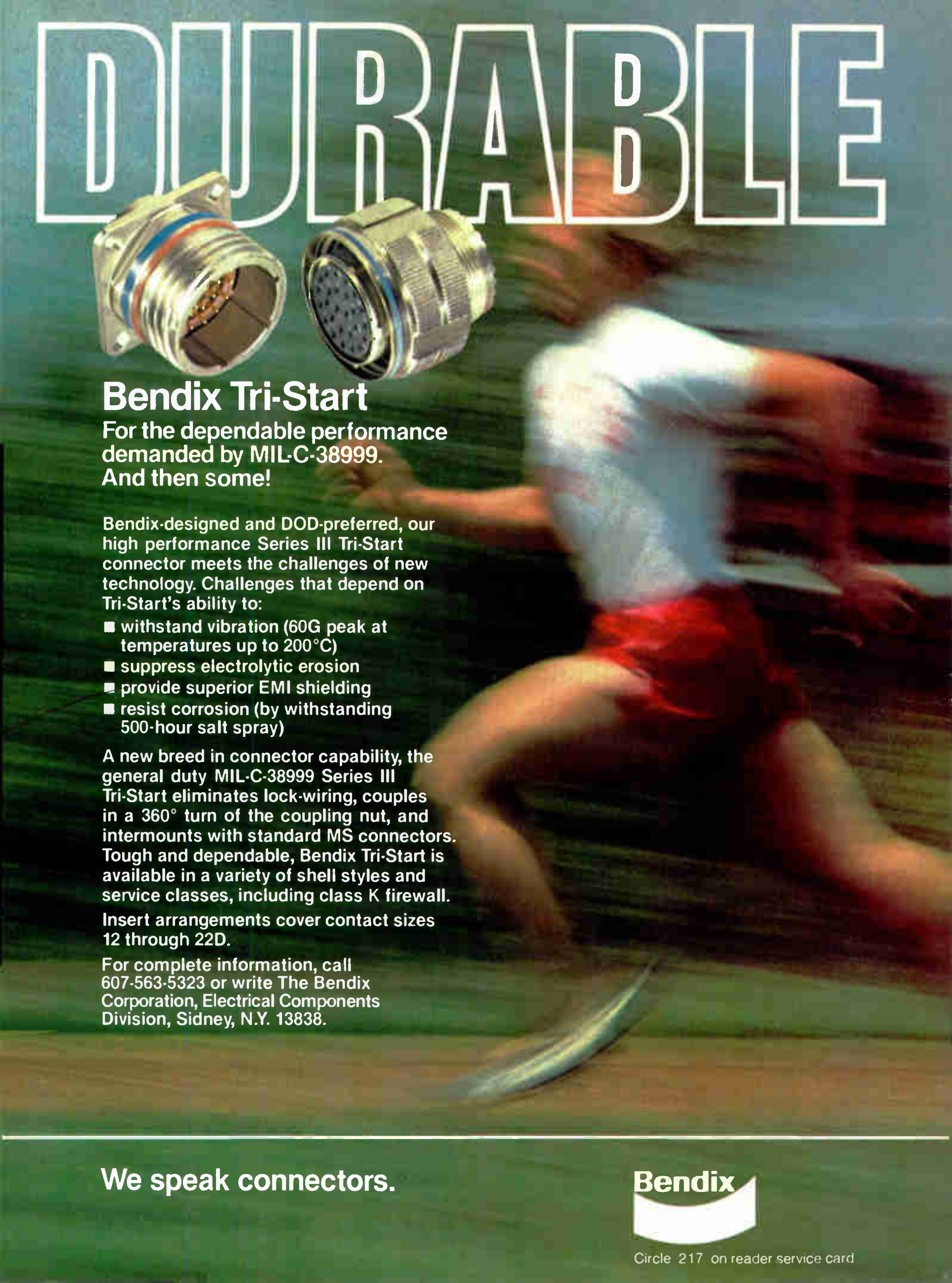
The low-profile open-ladder type socket is available with from 6 to 64 pins in 12 common arrangements. It is made of a tough high-quality glass-filled polyester thermoplastic called Valox, has good heat dissipation, and allows residual flux after soldering to be easily washed away.

In 1,000-piece quantities, the solder-tail 16-pin sockets sell for $1.13 each with gold contact and gold tail and 78.5¢ each with gold contact and tin tail. The Wire-Wrap 16-pin socket is $1.62 with gold contact and gold tail and 97.5¢ with gold contact and tin tail. Delivery is from stock to four weeks.

Texas Instruments Inc., Materials & Electrical Products Group, 34 Forest St., Attleboro, Mass. 02703. Phone (617) 222-2800 [399]



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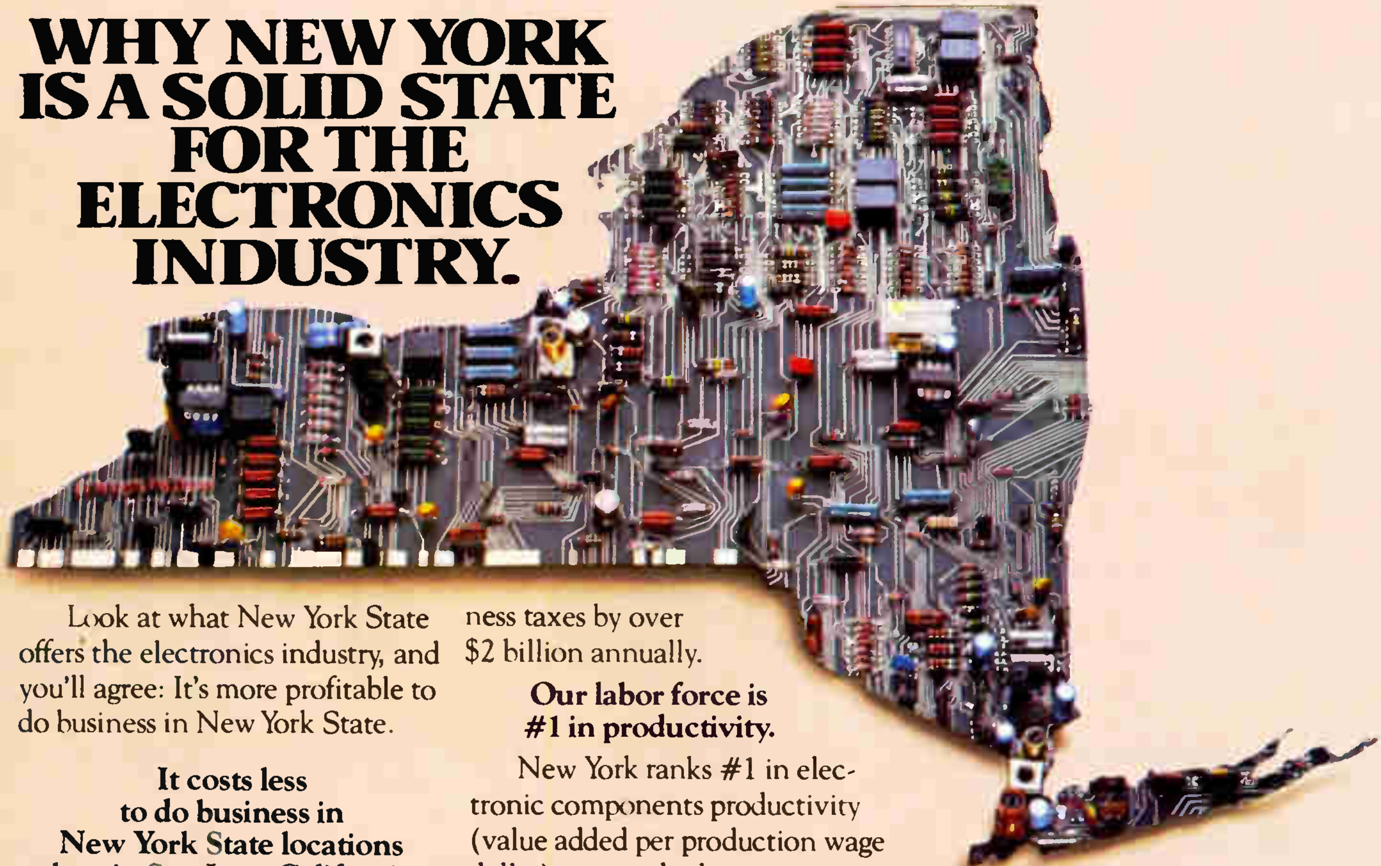
Bendix
Circle 217 on reader service card

WHY NEW YORK IS A SOLID STATE FOR THE ELECTRONICS INDUSTRY.



Look at what New York State offers the electronics industry, and you'll agree: It's more profitable to do business in New York State.

It costs less to do business in New York State locations than in San Jose, California. And we can prove it.

An independent study analyzed the four critical costs of taxes, wages, power and construction for a model new electronics firm. It showed that New York State offers locations where these costs are less than they are for choice electronics industry locations around the country.

For example, these costs would total $7.6 million annually in San Jose, versus only $6.4 million in, say, Brookhaven, New York.

New York has the best business advantages in America.

New York State is committed to a big, broad business-boosting program to create private sector jobs.

Our costs are lower because we have the best tax incentives and credits. We have on-the-job training and job incentive programs. Long-term, low-cost financing. And, we've cut personal and business taxes by over $2 billion annually.

Our labor force is #1 in productivity.

New York ranks #1 in electronic components productivity (value added per production wage dollar) among the locations analyzed. And in the past five years, New York's number of idle man-days due to work stoppages was half that of the national average.

We graduate more electronics engineers than any other state.

Thanks to universities like RPI and Cornell—and dozens of other fine colleges and universities—more electronics engineers are graduated each year in New York State than in any other state including California or Massachusetts. And since many of the largest electronics firms are already doing business here—GE, IBM, to name only a couple—our graduates are quickly turned into seasoned professionals.

When you look into New York, you'll love New York.

We have an abundance of electric power. Lots of affordable housing for your employees. And our 30 million acres include thousands of available plant sites. And some of the most magnificent outdoors and year-round recreation on the American continent.

Tell me more about why New York is a solid state for business. I am particularly interested in information on:

- ☐ Electronic Components
- ☐ Small Computers
- ☐ Semiconductors

Commissioner William D. Hassett, Jr.
New York State Dept. of Commerce
99 Washington Avenue
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Find out for yourself what 10 years' worth of proven performance can mean in your application. Call Darrell Petersen at (303) 773-4835 for more details or write for technical information and a free, illustrated brochure: Honeywell Test Instruments Division, Box 5227, Denver, Colorado 80217.

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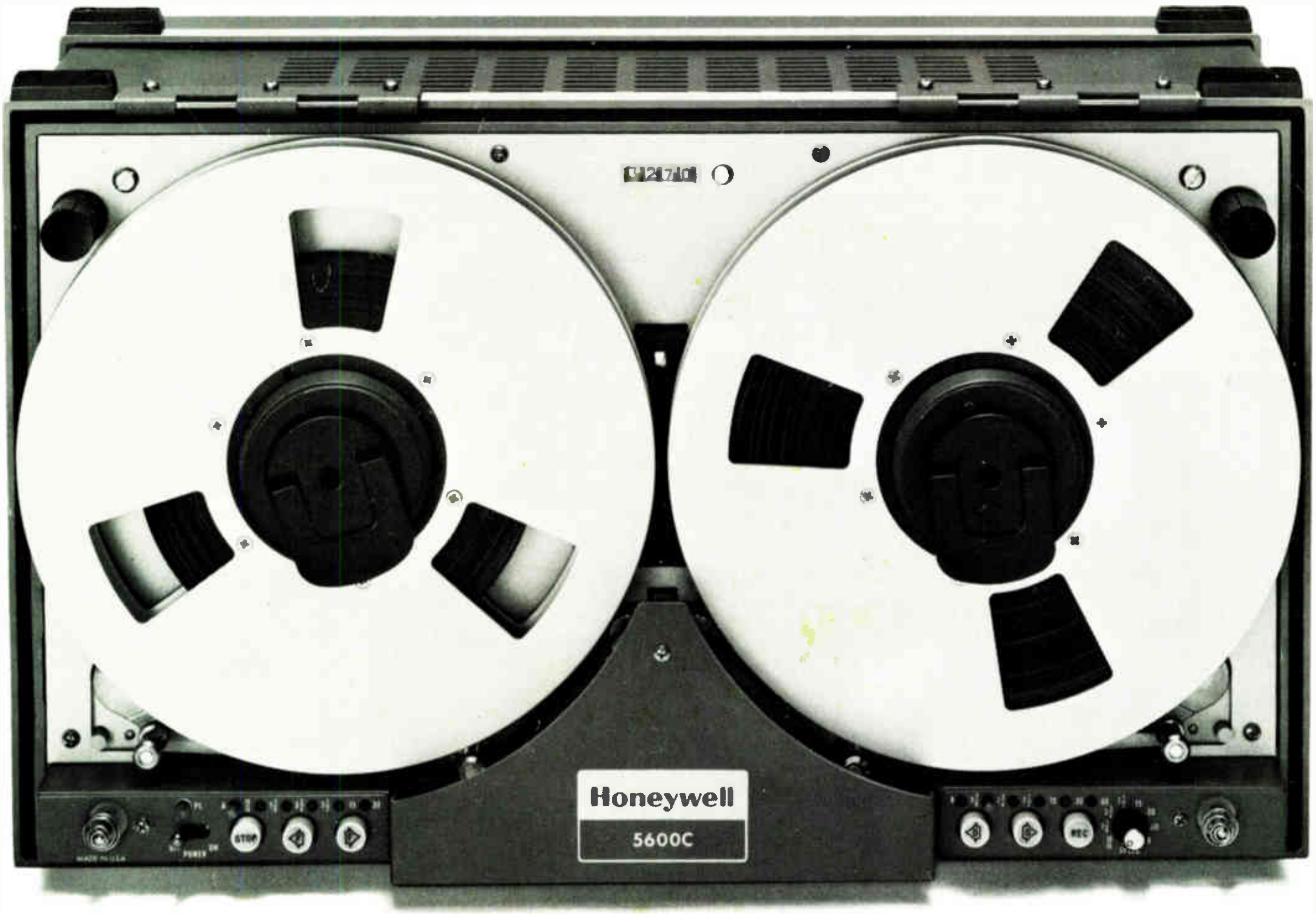


Honeywell

Circle 219 on reader service card

Software

Linker overcomes memory limits

Overlay linking loader divides large programs into segments to run on microcomputers

Lynx is an overlay linking loader that can be used with Microsoft languages—Fortran, Cobol, Basic, and Macro-80. It will also work with other language translators that produce relocatable files that are Microsoft-compatible.

Overlays permit programs that occupy more space than is available in main memory to run on microcomputers. Lynx divides the program into overlay segments that are brought into main memory from the disk as needed. Parameter values can be passed to an overlay as though it were a subroutine or through blocks of common variables.

Westico, the author of the loader, says that many large application programs running on minicomputers or large mainframes can be transported to a microcomputer with relatively minor modifications through the use of Lynx.

Even without using overlays, programs that have reached the maximum size allowed by Microsoft's L80 linker can be expanded by 9-K bytes with Lynx. With overlays, programs can use all available memory, including the space occupied by Lynx itself.

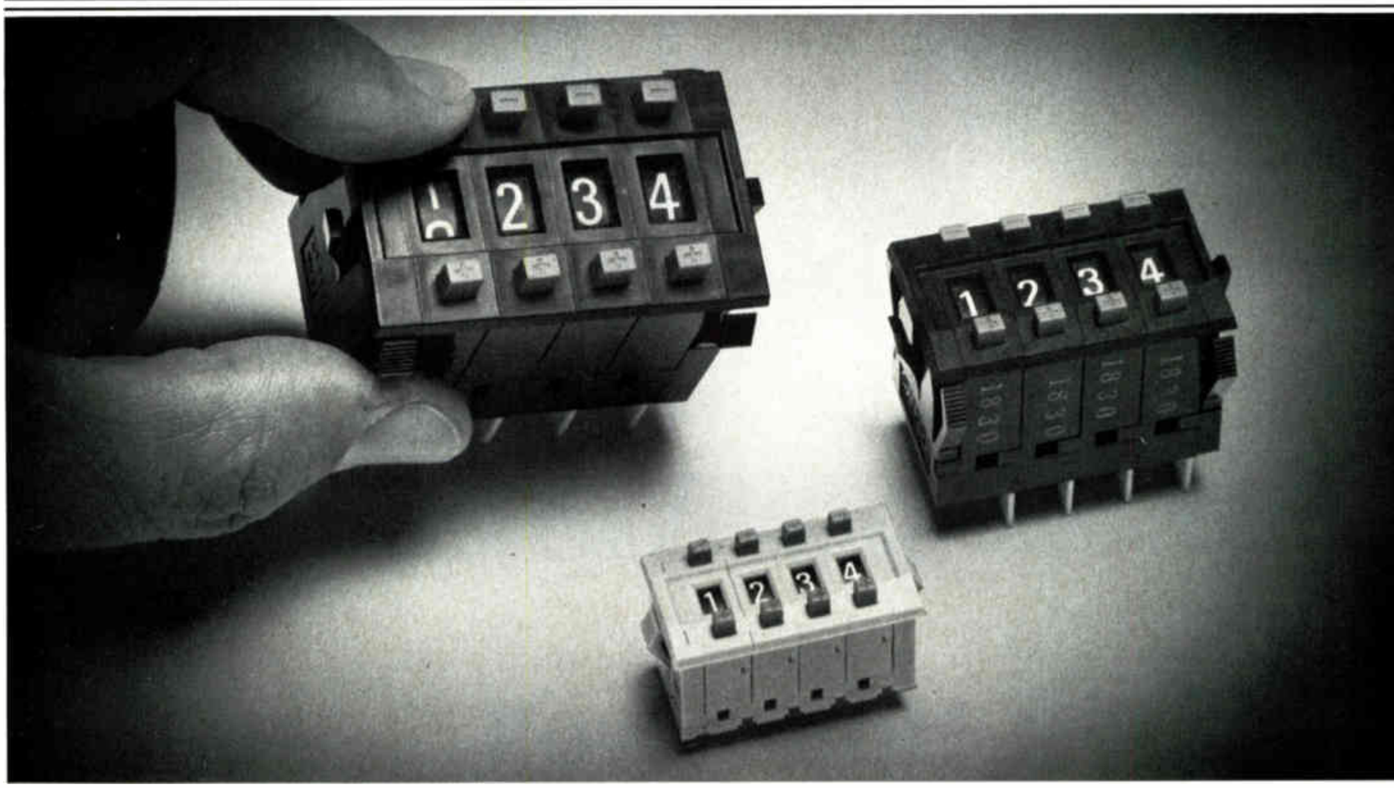
Lynx is easy to use: it employs simple commands, and a complete help function can specify a user's options on request. The loader requires a CP/M-compatible operating system and is priced at $250 with documentation. Documentation for the software costs alone $25.

Westico, 25 Van Zant St., Norwalk, Conn. 06855. Phone (203) 853-6880 [381]

Package passes messages among processors on Multibus

The Multibus message-exchange package, designated iMMX 800, simplifies multiprocessing and message exchange between multiple single-board computers plugged into a common Multibus. The computers can be multiple masters or slaves. Software modules in the set are tied to Intel's real-time executives (iRMX 80, 88, and 86) and support reliable transfer of messages between the application programs running on the various computers.

The modules allow the design of loosely coupled multiprocessor systems and make the coupling of 8- and 16-bit processors a routine job.



Messages of variable length are passed via shared memory; Intel's Multibus Interprocessor Protocol is implemented. Messages may be transferred to intelligent controller boards for data communications using Ethernet, Binary Synchronous, and other protocols.

The iMMX 800 package is priced at $1,000 plus royalties. First delivery is set for July.

Intel Corp., 5200 Elam Young Pkwy., Hillsboro, Ore. 97123 [382]

Multiuser Cobol runs under Oasis, protects data files

A multi-user Ryan-McFarland Cobol package that runs under the Oasis operating system provides up to 16 users with automatic record locking and file-locking security. It is the first microcomputer version of the language with these features, which increase data integrity, says Phase One Systems.

A run-time module is available separately for $250; the complete $750 package includes a one-pass compiler, an interactive debugger, and a file-structuring capability based on the Index Sequential Access Method. Oasis gives the user a high degree of flexibility in maintaining public, private, or shared files; accounting controls; inter-user communications facilities; a text editor; and a print spooler.

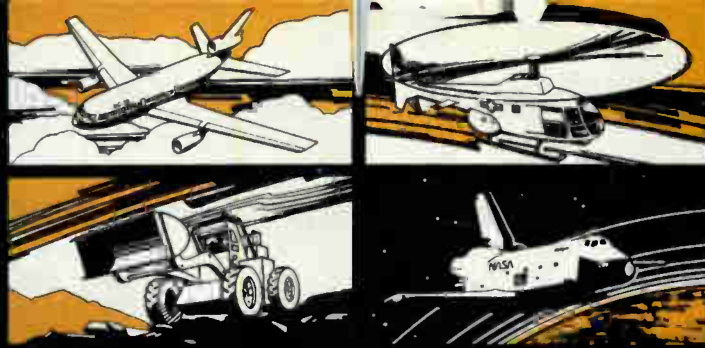
Phase One Systems Inc., 7700 Edgewater Dr., Suite 830, Oakland, Calif. 94621. Phone (415) 562-8085 [385]

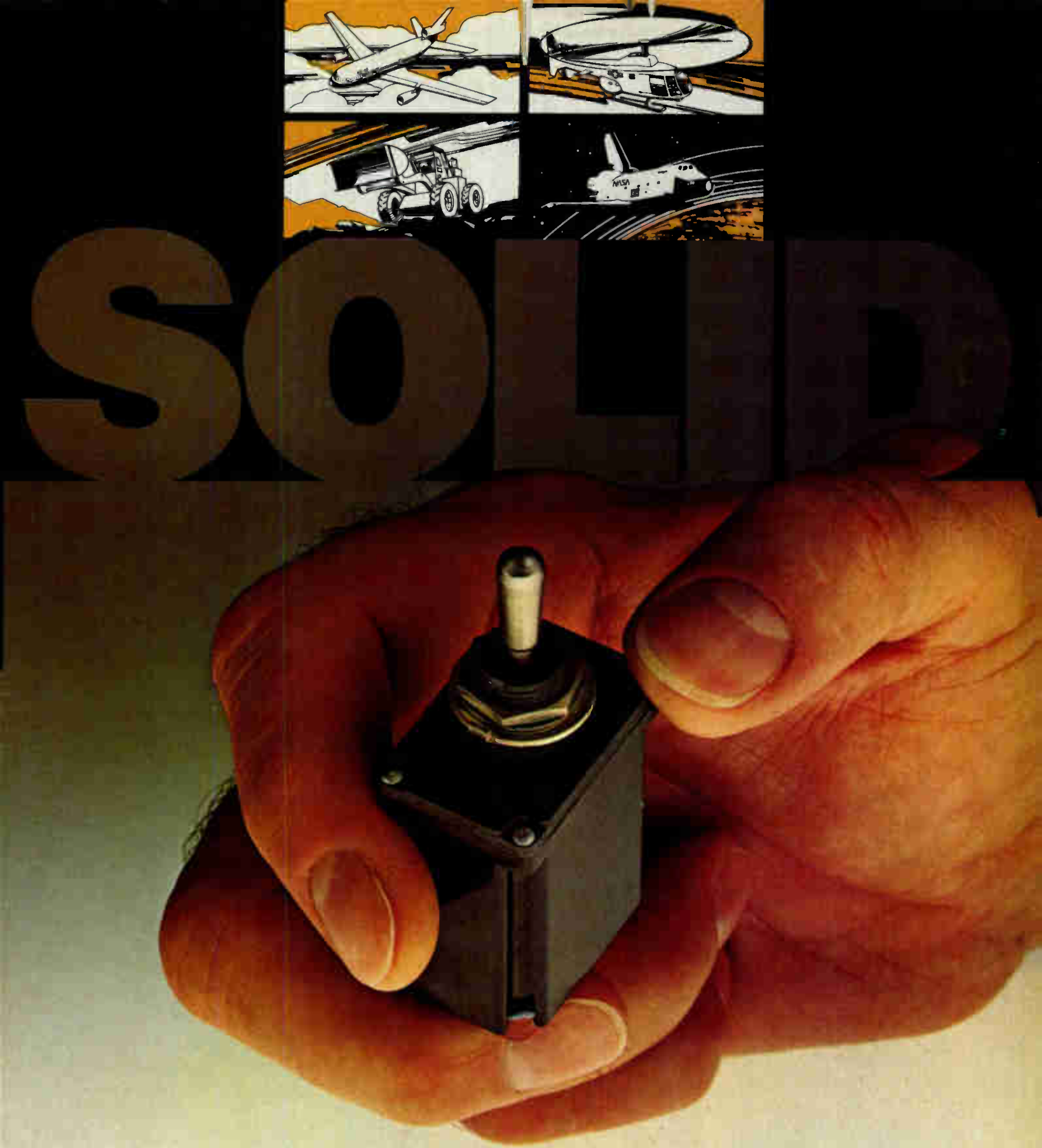
Apple 2 package provides three-dimensional graphics

The AppleGraphics 2 permits the user to view a two- or three-dimensional object from any angle for drafting, architectural, and scientific applications. The low-cost software makes it possible to call to the screen any portion of a drawing for detailed study, without degradation of picture quality. Because it supports a device-independent graphics protocol, AppleGraphics can be used with most advanced plotters to produce high-resolution hard copy.

System requirements are an Apple 2 or Apple 2 Plus with 48-K bytes of memory, Apple Language system, a video display unit, and a disk drive. Programs using the new software can be written in UCSD Pascal or Fortran (provided separately). The AppleGraphics 2 core package is modeled after the core graphics system defined by the Siggraph committee of the Association for Computing Machinery. Priced at $95, it is available this month.

Apple Computer Inc., 10260 Bandley Dr., Cupertino, Calif. 95014. Phone (408) 996-1010 [383]

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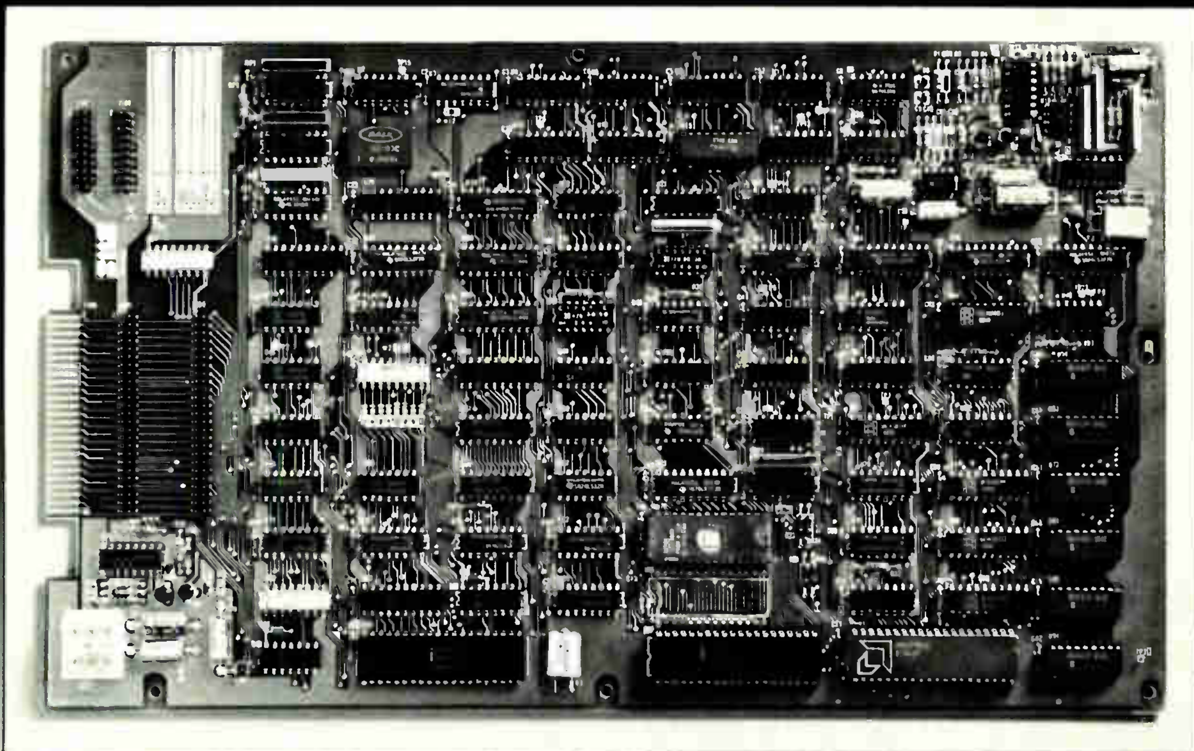
INTRODUCING
THE SMS WINCHESTER PLUS FLOPPY DISK CONTROLLER



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Everett/Charles Test Equipment, Inc. 2887 N. Towne Avenue, Pomona, CA 91767. (714) 621-9511. TWX 910-581-3835

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New products/materials

A new antistatic packaging material suitable for shipping sensitive electronic parts is static-free on both surfaces. Richmond's RCAS-3600 is made with an outer layer of tough antistatic spin-bonded polyolefin for strength, a layer of aluminum foil for shielding and moisture proofing, and an inside sealing surface of Richmond's antistatic pink polyolefin. These elements combine to form a heavy-duty, heat-sealable, flexible wrapping material.

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RCAS-3600 meets all the requirements of MIL-B-81705, type 1 for the prevention of electrostatic discharge.

Richmond, division of Dixico Inc., P. O. Box 1129, Redlands, Calif. 92373. Phone (714) 794-2111 [476]

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Multicore Solders, Cantiague Rock Road, Westbury, N. Y. 11590. Phone (516) 334-7997 [477]

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Aremco-Cast 554 may be used for

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HP-41C, $250; HP-41CV, $325; Optical Wand, $125; Printer/Plotter, $385; Plug-in Card Reader, $215; Quad Memory Module (brings HP-41C to HP-41CV memory capacity), $95; Memory Module, $30; Application Pacs, most are $30; Solution Books, $12.50.

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potting high-temperature transformers, thick-film hybrid circuits, and bonding radomes. It is available from stock at $265.00 a gallon, which is the minimum order. Delivery is in three weeks.

Aremco Products Inc., P. O. Box 429, Ossining, N. Y. 10562. Phone (914) 762-0685 [478]

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Plasticoat EC-121 will adhere to most amorphous plastics, but for crystalline materials, priming is required. The material may serve as a grounded coating in computer terminal enclosures, conductive foam, conductive styrene containers, and as floor paint in munitions areas.

Plastic Systems Inc., 88a Ellsworth St., Worcester, Mass. 01608. Phone (617) 799-2600 [480]

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Formulated Resins Inc., P. O. Box 508, Greenville, R. I. 02828. Phone (401) 949-2060 [422]

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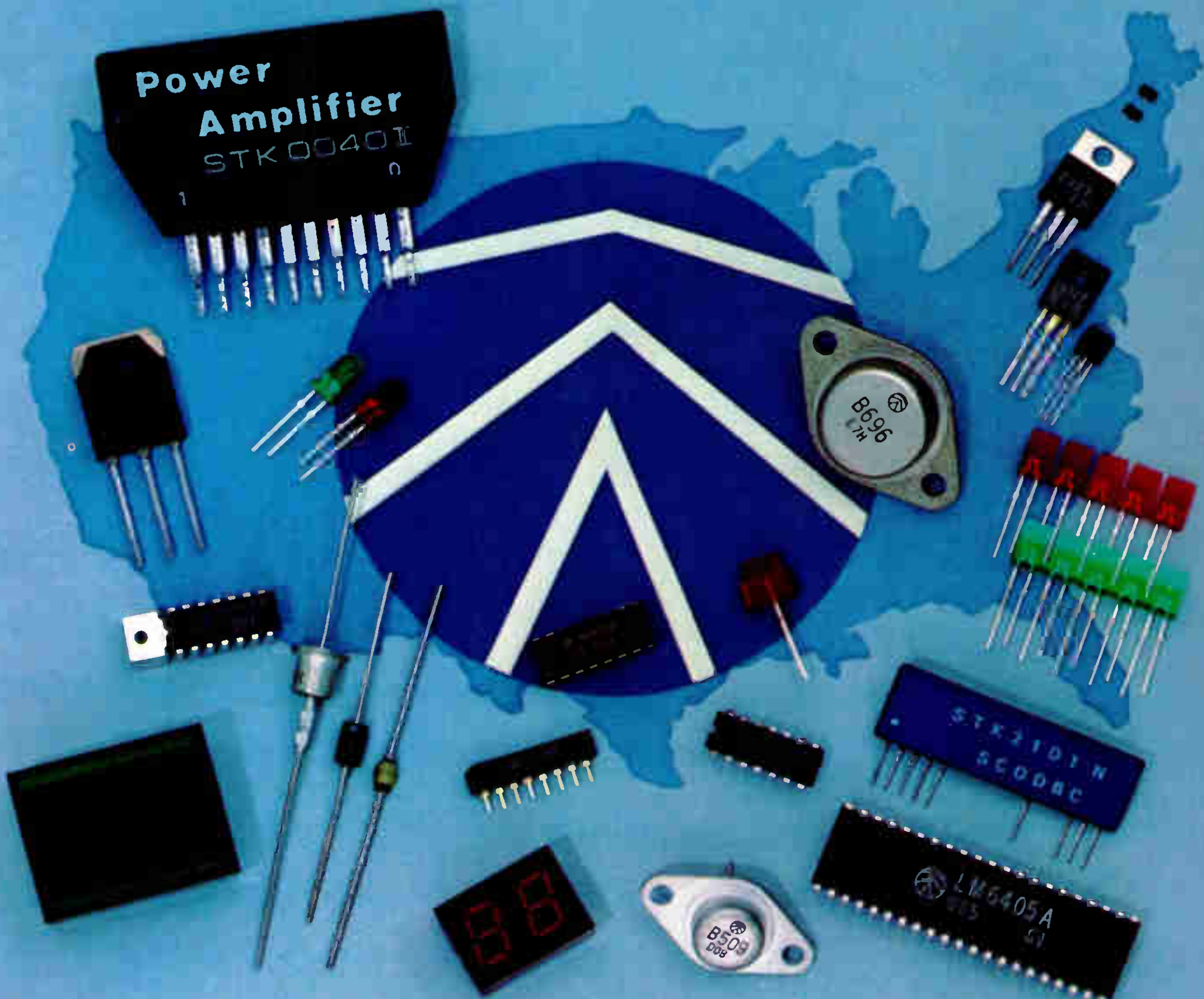

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Circle 235 on reader service card

Products Newsletter

Minicomputer-based development system adds languages

Cambridge, Mass.–based Intermetrics Inc. is expected to follow the recent introduction of its PasPort minicomputer-based microprocessor software-development system with added cross compilers that will support more languages and microprocessors in addition to the 8086 [*Electronics*, May 19, p. 227]. Already tentatively scheduled for release around the end of 1981 is a Pascal-based system for Motorola MC68000 software development; a similar system for the Zilog Z8000 is due in 1982. **The firm will also eventually offer Ada-based cross compilers as well**—it is a bidder in the Ada integrated environment program of the U. S. Air Force's Rome Air Development Center. Finally, within the next two years the company may seek to serve the big aftermarket in 8-bit microprocessors.

Mostek to produce 64-K E-PROMs

Mostek Corp. will join the list of those making 64-K erasable programmable read-only memory chips with the introduction of an 8-K-by-8-bit part. The Carrollton, Texas, MOS company will make the n-MOS device available June 15. In quantities of 100, the MK2764 will cost $52.70 each for 500-ns parts, $44.80 for 550-ns devices, and $32.50 for 650-ns chips. **The MK2764 features include power standby, which cuts consumption to 60% of its active status,** and a maximum power rating of 525 mW. The E-PROM has 28 pins and is compatible with Mostek's byte-wide family of memory components.

Inmos, awaiting 64-K, cuts prices on 16-K RAM

Its sights still set on introducing a 64-K dynamic random-access memory chip by mid-year, Inmos Corp. is cutting the price of its IMS1400 16-K-by-1-bit static RAM. Inmos, which introduced the 16-K part last December, is reducing the price of the IMS1400-55 (with 55-ns access time) from $150 to $77 each in quantities of 100. The price of the IMS1400-45 (45-ns access time) is now $92.40. The Colorado Springs, Colo., firm is planning to introduce its 64-K RAM—called the IMS2600—and a 4-K-by-4-bit version of the 16-K RAM—called the IMS1420—in the middle of the summer. The firm has also given Matsushita Electric Trading Co. the exclusive marketing rights to its products in Japan.

Mil-standard processor a first for Mostek

Mostek Corp. of Carrollton, Texas, also will offer its first military microprocessor this month—the MKB3880P, a MIL-STD-883 class B version of the 8-bit Z80. The microprocessor, **which will be offered in a 40-pin ceramic dual in-line package,** will be available with clock rates of 2.5 or 4 MHz. In quantities of 100, the 2.5-MHz version costs $68.85 each, whereas the 4-MHz part goes for $91.

Second-source DAC80 touts lower cost

A second source for the industry-standard Burr-Brown DAC80 digital-to-analog converter **costs about 60% less than other such units in single quantities and 35% to 38% less in 100-unit lots.** The 12-bit hybrid HS DAC80 from Hybrid Systems Corp. accepts inputs compatible with TTL and complementary-MOS and yields either current or voltage outputs. It also sports specifications almost identical to those of the parent part. Pricing, regardless of order size, is $13.95 for current-output models and $14.95 for voltage-output models, and the Billerica, Mass., firm requires a $50 minimum order. Delivery is from stock.

Career outlook

How to succeed as a technocrat

■ Another technology gap has been filled. While the humorous treatments of how hierarchies actually work contained in Parkinson's Law and the Peter Principle have been adequate, they lack an appreciation for the organizations involved in high technology.

With "Putt's Law and the Successful Technocrat," written by Archibald Putt (Exposition Press, Inc., Smithtown, N.Y., 165 pp., $9.25), high technology is more than represented. The book is a tongue-in-cheek description of technological management that many engineers will recognize as painfully true.

Take Putt's First Law, which states: "Every technical hierarchy, in time, develops a competence inversion." This law is better understood in its corollary form: "Technology is dominated by two types of people—those who understand what they do not manage and those who manage what they do not understand."

Putt explains that the most competent people in a technical organization tend to remain near the bottom, while persons of lesser talent rise to the top. However, he adds, this movement paradoxically is healthy. "Incompetence is flushed out of the lower levels, leaving competent people behind to do the work," Putt maintains.

Scheduled for publication next month, "Putt's Law" contains a range of comic observations on the running of technology-driven enterprises, be they government agencies or companies. Beneath the humor, however, are pungent comments perhaps more telling than the many variations on Murphy's Law.

Computer solutions. In a chapter devoted to data-processing laws, Putt points out that a person or group wishing to promote some action is well advised to get the problem formatted on a computer so that the desired action can be shown as a computer printout. The First Data-Processing User's Law states: "To remove doubt from your actions, invoke a computer solution." Once this step is taken, you can apply the Second Data Processing User's Law: "Attribute successes to people and problems to computers." The author provides a parallel to Murphy's Law—to wit, "Anything that can go wrong will go wrong faster with computers."

Yet academia is not spared Putt's satire either. Suggesting that a university is a marvelous place from which to study the power structure of the technical community, he writes, "Because a university professor has no industrial affiliation, he is a logical choice for membership on government committees that help determine how government research-and-development funds should be spent in industry." After getting on the committees, he notes, the sharp academic will make contacts in industry leading to consulting jobs often "for companies whose businesses were under review by the Washington committees." This set up, Putt calls, "the idyllic life."

There are times, Putt admits, when advancement is not in the cards and ambitious technocrats have to "settle for survival." Therefore, he turns to the First Law of Survival: "Survival is achieved through risk reduction."

The survival method is contained in the Second Law of Survival: "To get along, go along." Putt presents a familiar example.

Engineers preparing a proposal for a government contract are required by management to tighten the schedule and cost estimates in order to win the award. Reluctantly they go along, and as a result, the government soon has one more contract running well over budget.

Who is the author? Actually, Archibald Putt is a pseudonym for a well-known technocrat. According to the publisher, he has served as president of an international technical society, worked on government advisory committees (see above), done basic research, and consulted for large multinational corporations. After reading the barbs and gibes contained in the book, the need for a pseudonym is quite clear. Putt has shown that there is more to a career in technology than can be found in textbooks. **-Gerald M. Walker**

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