MAY 5, 1981

THE RISE OF THE OPTICAL DISK/97

ECC takes on fiber optics, bonding techniques/137

Temperature swings rarely faze reliable bubble cassette/149

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Electronics®

ERROR DETECTION AND CORRECTION

A TRILOGY

HOW CAN YOUR MICROPROCESSOR BOARD HELP TEST ITSELF?

It's ironic. The very intelligence that makes your products excel can also be the obstacle that makes testing difficult. Why? Because those intelligent microprocessors are difficult to model. And until they're put to work via code, they're no smarter than any other piece of silicon. Can they be awakened and used to test themselves? Let's look at some of today's testing techniques and see.

Alternatives for testing microprocessor boards.

Board testers available today generally use one of four approaches:

1) Simulator board testing. This is an edge-connector and guided probe testing technique that relies on patterns from a simulation model. The processor is usually removed from the board, and input patterns applied. Output patterns are then compared with those predicted by the simulator. If the patterns match, the support logic is judged good. Next the processor is inserted and different patterns are applied. Now the outputs are compared to those predicted based on the original model plus a high-level software model of the processor. If those patterns match, the entire board is said to be good. Excessive time can be consumed generating both high-level models and testing software.

2) In-circuit testing. Using a bed-of-nails fixture, contact is made with each logic circuit on the board, including the μP. Pulses are applied to input pins of each device. Outputs are compared to those predicted from device truth tables supplied by manufacturers. These libraries are programmed for common device configurations and must often be modified for actual configurations.

3) Comparison testing. In this edge-connector and guided probe method, a known good board must be available as a reference. The known and unknown are initialized, synchronized and then are compared by applying preprogrammed instructions or patterns, or by stimulating with pseudorandomly generated pattern sets. If the outputs match, the unknown board passes.

4) Processor-based testing. This technique uses the intelligence of the μP on the board. The board is powered up and operated at speeds up to 10 MHz using preprogrammed test code resident in the test system or on the board itself. The on-board μP executes this code to exercise the address and data buses, and support circuitry. Key nodes are monitored with signature analysis to detect faults.

Why does HP use processor-based testing?

Our experience in testing μP boards has revealed several benefits of processor-based testing. That's why we've incorporated it into our 3060A Board Test System with the High Speed Digital Functional Test option.

First of all, boards are tested at speed, with all components, buses and control lines operating in modes similar to actual use conditions. The result? Ability to test pins which are not exercised unless the processor is executing instructions (Fig. 1), plus detection of faults related to the address and data bus structure and timing faults.

Examples of Processor Pins Testable Only With Software

	8085		6800	Z80
Interrupts	INTR TRAP	RST 7.5 RST 6.5 RST 5.5	$\overline{IRQ}$ $\overline{NMI}$	$\overline{INT}$ $\overline{NMI}$
Control Outputs	S_0 S_1 IO/$\overline{M}$	$\overline{RD}$ $\overline{WR}$	VMA R/$\overline{W}$	$\overline{M1}$ $\overline{RD}$ $\overline{WR}$ $\overline{HALT}$
Other	S1D S0D			

Fig. 1

In addition, processor-based testing permits fault detection using Signature Analysis (SA), which is complimented by new software in the digital functional testing package. SA allows rapid fault isolation to the component level on active bi-directional buses. That means high throughput in production.

Furthermore, with the programming aids available from HP, functional test program development time is minimized for μP, memory and IO boards. For example, you can either modify existing routines provided by HP, build your own stimulus routines using HP-supplied building blocks, or develop stimulus programs on a development system and download to the 3060A. The bottom line of processor-based testing is fast test program development, high throughput, and high yield at the final product level.

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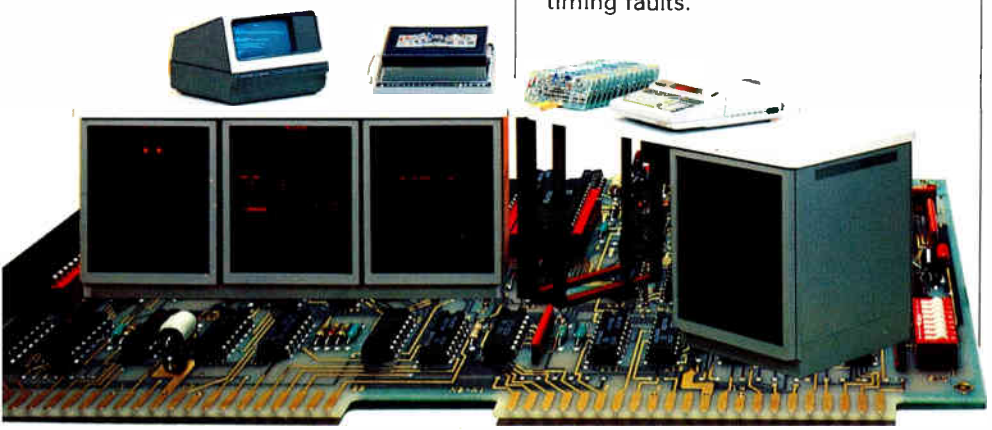

HP Circuit Testers—The Right Decision

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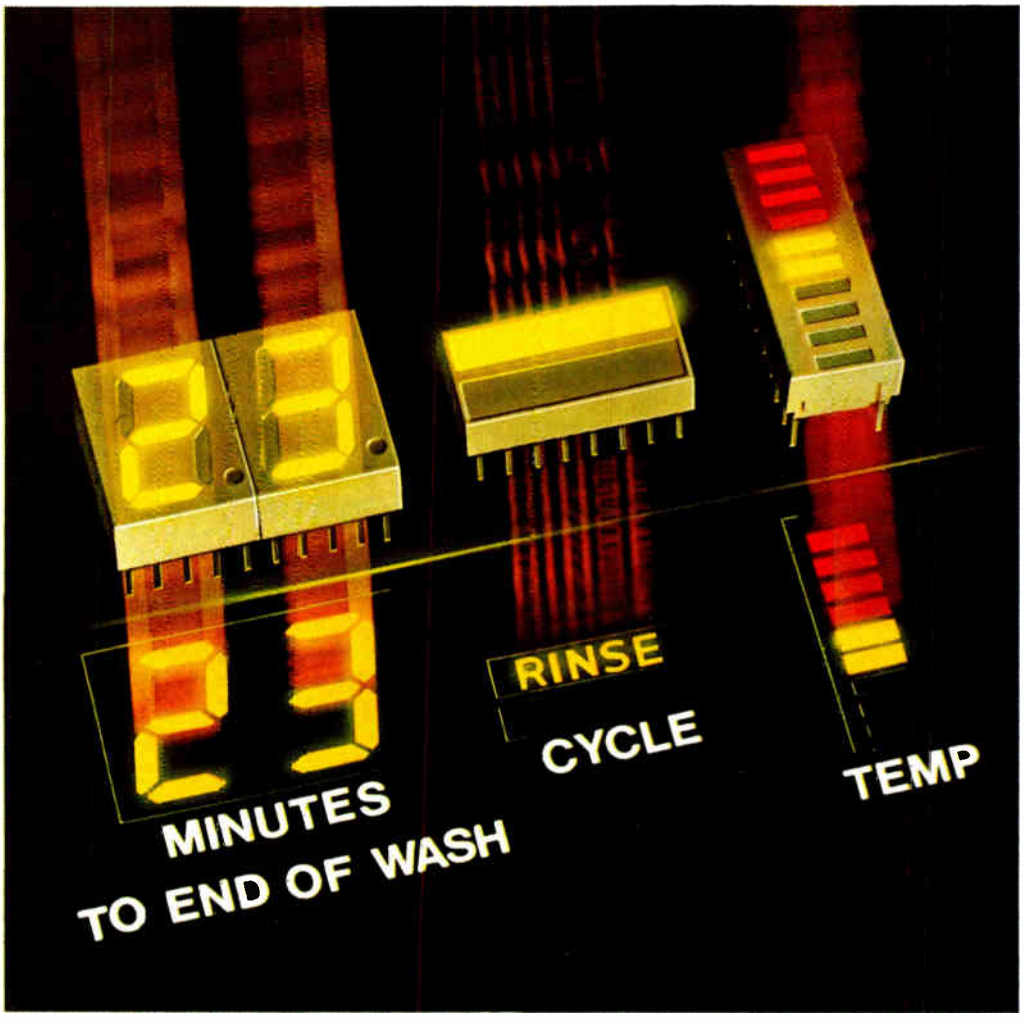

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Electronics
The International Magazine of Electronic Technology
Vol. 54, No. 9 • May 5, 1981

Electronics

Highlights

Cover: Eliminating errors in solid-state and disk memories, 121

The more dense a memory—be it a semiconductor device, which is prone to alpha disturbance and electrical noise, or a magnetic disk, which can suffer surface damage—the greater the risk of error. This three-part series describes some of the latest ways to detect and correct errors. The first two parts discuss hardware implementations: one, for disks, is simply a single large-scale integrated circuit that uses Fire codes (p. 122); the other, for semiconductors, is a board of standard TTL devices that employs a Hamming code (p. 125). The last is a hitherto unpublished scheme called the orchard code that corrects many multibit errors but requires only one check bit per memory location (p. 130).

The cover sculpture was done by Miriam Brofsky.

Optical disks set for a spin as mass storage, 97

Recently launched to compete with video cassettes for home entertainment, the optical disk holds out greater promise as a mass-storage medium. As such, it should move into the automated office in force. Indeed, it will likely make entirely new system applications cost-effective while seriously competing with present storage media, says this Inside the News story.

ECC again presents notable advances, 137

Although low-keyed, the Electronic Components Conference continues to be valuable for both users and circuit designers. Among the highlights of this year's meeting, to be held May 11–13 in Atlanta, are a new semiconductor oxide, an integrated-circuit process that combines silicon and tantalum, and a mechanical fiber-optic switch with the lowest insertion loss reported so far.

Removable bubble cassette is largely indifferent to temperature, 149

Magnetic-bubble memories boast not only compact nonvolatile storage of up to a million bits, but ruggedness as well. Extending the applicability of these devices, a drive system bubble uses a sensor built into the cassette to maintain reliable operation between $-20°$ and $+70°C$.

MNOS EE-PROMs turn to n-channel technology, 152

Nitride-based electrically erasable programmable read-only memories have been confined to consumer and other applications that are not hampered by the low speed and density inherent in their p-channel technology. N-channel technology gives this device the speed and the density necessary for computer and microcomputer systems.

And in the next issue . . .

Quality and reliability: a special report . . . a multicapable disk-drive controller . . . programming microprocessor systems by telephone.

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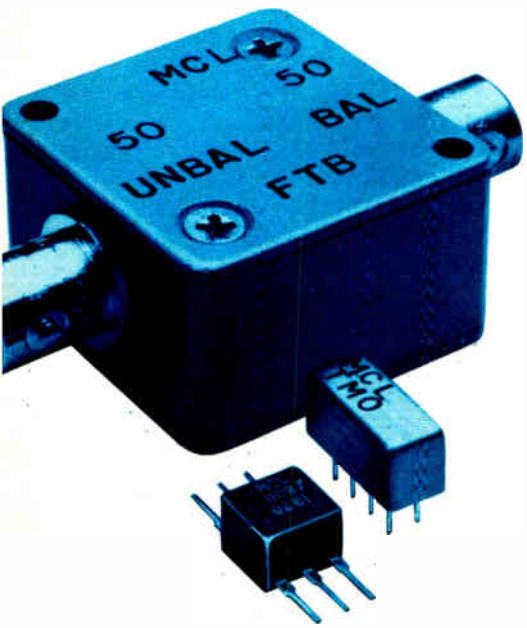

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Imped. Ratio	1	1	1.5	2.5	4	9	9	16	16
Freq. (MHz)	.15-400	8-300	.1-300	.01-100	.02-200	.15-200	2-90	.3-120	7-85
T Model (10-49)	$2.95	$4.95	$3.95	$3.95	$3.95	$3.45	$5.45	$3.95	$5.95
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Imped. Ratio	1	2	2.5	3	4	4	5	13
Freq. (MHz)	.05-200	.07-200	.01-100	.05-250	2-350	8-350	3-300	.3-120
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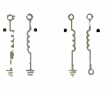

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Publisher's letter

When the chips are down and the bits start to fly, errors start to mount, and that's as true of semiconductor memories as it is of magnetic disks. The prodigious increases in memory densities make the task of error detection and correction even more vital. So it is no surprise that memory makers are incorporating such fail-safe schemes in products.

To give a sense of the directions in which these solutions to bit-error problems are going, we have assembled a package of three articles, beginning on p. 121. These stories cover a chip that implements Fire codes for correcting error bursts on disks, a board of TTL parts that realize Hamming codes for semiconductor memory applications, and a mathematical model, called the orchard scheme by its originators that is so new it hasn't yet reached the hardware stage.

Of course, all of these error-detection and -correction techniques begin as purely mathematical problems. Someone must sit down and do that basic work; for these contributions Richard W. Hamming and Philip Fire earned recognition.

Actually, Hamming is a well-known figure in electrical engineering circles; he is a 1979 winner of the Institute of Electrical and Electronics Engineers' Piore award for achievement in information processing, a founder and past president of the Association for Computing Machinery, and a member of the National Academy of Engineering. After 30 years with Bell Laboratories, he retired in 1976 and joined the computer science department of the U. S. Navy Postgraduate School in Monterey, Calif.

Whereas Hamming is a mathematician, Fire is an engineer. He has been with General Telephone and Electronics' Mountain View, Calif., laboratories since 1955. Like Hamming, he is a fellow of the IEEE, and he also is associated with the Navy; he is on leave of absence from GTE to serve as liaison scientist in communications and information theory with the Office of Naval Research in London.

Hamming worked on his codes during his first years at Bell Labs; Fire developed his as part of a thesis for the first of two advanced degrees he earned at Stanford University after joining GTE Labs.

Memories are always newsworthy, so it's hardly surprising that another major article in this issue is devoted to the optical disk, a rapidly developing alternative to magnetic disks and magnetic tapes. In an Inside the News story beginning on p. 97, our West Coast computers editor Martin Marshall gives the lowdown on this memory technology that until now has been in the news as a consumer product.

"It will be a billion-dollar-a-year industry by 1990," Martin says. A video disk's easy removability, its storage density, and its long data-retention rate are among its leading attractions, he says. With capacities that might hit 50 gigabytes, the optical disk will boast a truly low price per bit.

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Readers' comments

Bus message standards

To the Editor: I was delighted to see the article by Maris Graube in the March 24 issue ["In-house standards fill gaps in instrument-computer interface," p. 131]. But it seems to me that the Tektronix in-house standard for IEEE-488 bus messages could go even further.

For example, it has been suggested that numbers in engineering format (with the exponent a multiple of 3) are more readable than other floating-point numbers, and it also appears desirable to specify the preferred message for certain key operations. Telling an instrument to initiate a reading is one that comes readily to mind. It would be interesting to see a list of the various ASCII characters that have been used for this purpose. In general, IEEE-488 messages should be chosen for mnemonic significance.

Graube has been a member of an IEEE committee that has been working toward a standard in this area. This work has gone on for several years. As a member of the Institute of Electrical and Electronics Engineers, I find it difficult to understand why that committee has failed to submit a proposed standard. Surely there must be something its members can agree on, even if it is only a standard for terminating messages. I have expressed my concern to the IEEE in the past. It would be most interesting to hear what other readers have to say about the Tektronix proposal.

Robert G. Huenemann
San Bruno, Calif.

Correction

In "Fast 16-K RAM idles on 75 mW" (March 10, p. 228), in both the text and the accompanying figure the chip's word-line driver circuit, contained in the X decoder, is incorrectly referred to as a sense amplifier.

1980 index ready

The index of articles published in Electronics *during 1980 is now available. If you are interested in receiving a copy, circle 370 on the reader service card.*

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COHERENT and all of its associated software are written totally in the high-level programming language **C**. Using **C** as the primary implementation language yields a high degree of reliability, portability, and ease of modification with no noticeable performance penalty.

Features

COHERENT provides **C** language source compatibility with programs written to run under Seventh Edition UNIX, enabling the large base of software written to run under UNIX (from numerous sources) to be available to the **COHERENT** user. The system design is based on a number of fundamental concepts. Central to this design is the unified structure of i/o with respect to ordinary files, external devices, and interprocess communication (pipes). At the same time, a great deal of attention has been paid to system performance so that the machine's resources are used in the most efficient way. The major features of **COHERENT** include:

- multiuser and multi-tasking facilities,
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- loadable device drivers,
- process timing, profiling and debugging trace features.

*UNIX is a trademark of Bell Labs

Software Tools

In addition to the standard commands for manipulating processes, files, and the like, in its initial release **COHERENT** will include the following major software components: **SHELL**, the command interpreter; **STDIO**, a portable, standard i/o library plus run-time support routines; **AS**, an assembler for the host machine; **CROSS**, a number of cross-assemblers for other machines with compatible object format with '**AS**' above; **DB**, a symbolic debugger for **C**, Pascal, Fortran, and assembler; **ED**, a context-oriented text editor with regular expression patterns; **SED**, a stream editor (used in filters) fashioned after '**ED**'; **GREP**, a pattern matching filter; **AWK**, a pattern scanning and processing language; **LEX**, a lexical analyzer generator; **YACC**, an advanced parser generator language; **NROFF**, an Nroff-compatible text formatter; **LEARN**, computer-aided instruction about computers; **DC**, a desk calculator; **QUOTA**, a package of accounting programs to control filespace and processor use; and **MAIL**, an electronic personal message system.

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The realm of language support is one of the major strengths of **COHERENT**. The following language processors will be supported initially:

- **C** a portable compiler for the language **C**, including stricter type enforcement in the manner of **LINT**.
- **FORTRAN** portable compiler supporting the full ANS Fortran 77 standard.
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The unified design philosophy underlying the implementation of these languages has contributed significantly to the ease of their portability. In particular, the existence of a generalized code generator is such that with a minimal effort (about one man-month) all of the above language processors can be made to run on a new machine. The net result is that the compilers running under **COHERENT** produce extremely tight code very closely rivaling that produced by an *experienced* assembler programmer. Finally, the unified coder and conformable calling sequences permit the intermixture of these languages in a single program.

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In part because of the language portability discussed above, and in part because of a substantial effort in achieving a greater degree of machine-independence in the design and implementation of the **COHERENT** operating system, only a small effort need be invested to port the whole system to a new machine. Because of this, an investment in **COHERENT** software is not tied to a single processor. Applications can move with the entire system to a new processor with about two man months of effort.

The initial version of **COHERENT** is available for the Digital Equipment Corporation PDP-11 computers with memory-mapping, such as the PDP 11/34. Machines which will be supported in the coming months are the Intel 8086, Zilog Z8000, and Motorola 68000. Machines for which ports are being considered are the DEC VAX 11/780 and the IBM 370, among others.

Because **COHERENT** has been developed independently, the pricing is exceptionally attractive. Of course **COHERENT** is completely supported by its developer. To get more information about **COHERENT** contact us today.

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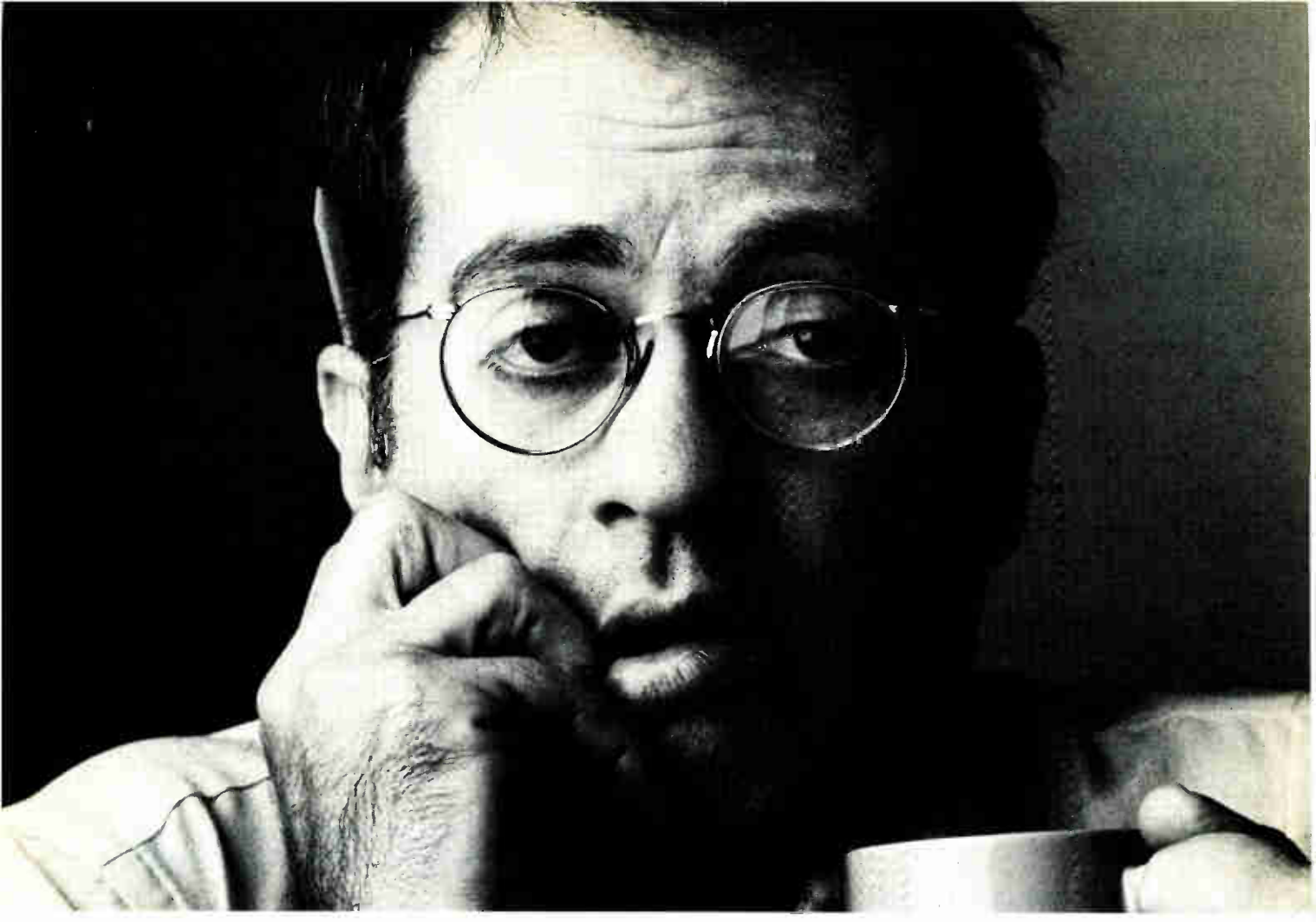

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News update

■ Three years after its founding, Lucitron Inc. plans to deliver its first 34-inch-diagonal flat-panel dc plasma display in June, under contract to the Naval Ocean Systems Center. As the initial commercial fruit of the Lucitron venture, the 6-in.-thick monochrome display will be the first of about a dozen evaluation units to be delivered to customers before next June, says the company.

Funds sought. What's more, the Northbrook, Ill., firm has put together an ambitious business plan and is now looking for a $3 million investment to help it make the transition from research to commercial production. Lucitron was formed by a trio of former Zenith Radio Corp. researchers to continue their flat-panel work when Zenith folded its research facility [*Electronics*, July 6, 1978, p. 50].

Efforts to date have been funded primarily by a three-year development contract from General Telephone & Electronics Corp. That contract runs out soon, and GTE has lost interest in the project since selling its consumer products operation last year, says Lucitron vice president and cofounder Alan Sobel.

The company's dc flat-panel plasma technology depends on a patented multiplexing technique that reduces drive electronics to help hold down costs [*Electronics*, Jan. 31, 1980, p. 69]. It will be important in the face of competing flat-panel technologies expected from Japan and elsewhere. Complex drive electronics have been a stumbling block in the development of practical flat-panel dc displays.

Cost to drop. Initial 34-in. evaluation units will fetch prices well into five figures. But by 1987, Sobel expects, Lucitron will offer 50-in.-diagonal full-color units for an average price of $6,700.

It plans to concentrate on the commercial and industrial market for very large displays and hopes eventually to build color units with up to 60-in.-diagonal panels. Lucitron's business plan calls for profitability within three years and annual sales of $40 million after six years, Sobel says. **-Wesley R. Iversen**

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People

Solomon heads integration of TRW Coast electronics

When TRW Inc. decided to consolidate all its West Coast operations into a single unit in Redondo Beach, Calif., it gave George E. Solomon, its top systems engineer, the job of overseeing the process. Solomon's charter is to spur the interchange of key developments in electronics.

"We will bring together under one roof all the electronic activities of TRW," says Solomon, whose background has been one of steady advancement in TRW's Defense and Space Systems Group ever since he joined the firm in 1954. Most recently he was vice president and general manager for the six-division group.

The impetus for establishing the new operating sector, to be called Electronics and Defense, stems from the mushrooming growth of the separate groups, which despite a common bond of high technology have tended more and more to go their own way. Solomon's new title is executive vice president and general manager, Electronics and Defense.

The soft-spoken Solomon, who first made his mark by solving critical research and development problems involving the reentry vehicle of the first intercontinental ballistic missile, is now immersed in setting up ways to knit together allied parts of the groups more closely. "We're just now coming to grips with technology transfer," he says.

Several examples of the need for closer coordination may be found in bipolar semiconductors and digital telephone switching, where TRW has similar operations in the defense and commercial areas. TRW LSI Products, for instance, which makes high-speed signal-processing devices for commercial customers, spun out of the defense systems business in 1976 and still taps it for basic technology. On the other hand, the systems group is currently building a digital radio and multiplexer acquisition unit for the U. S. Army that employs technology used in digital switching at the electronics group's Vidar division.

The new focus for electronics is slated to emerge with the start of construction this year on a microelectronics center in adjacent Manhattan Beach, Calif. In all, TRW expects to commit about $100 million toward microelectronics advances over the next five years.

Kluchman sees Access's role as key to computer's full use

About eight months ago, Access Technology Inc., a publisher of computer-generated reports in Wellesley, Mass., decided to enter the software-publishing business. Now that

Togetherness. George E. Solomon aims to simplify technology transfer at TRW.

For managers. Allen Kluchman's goal is simpler software for the nontechnical.

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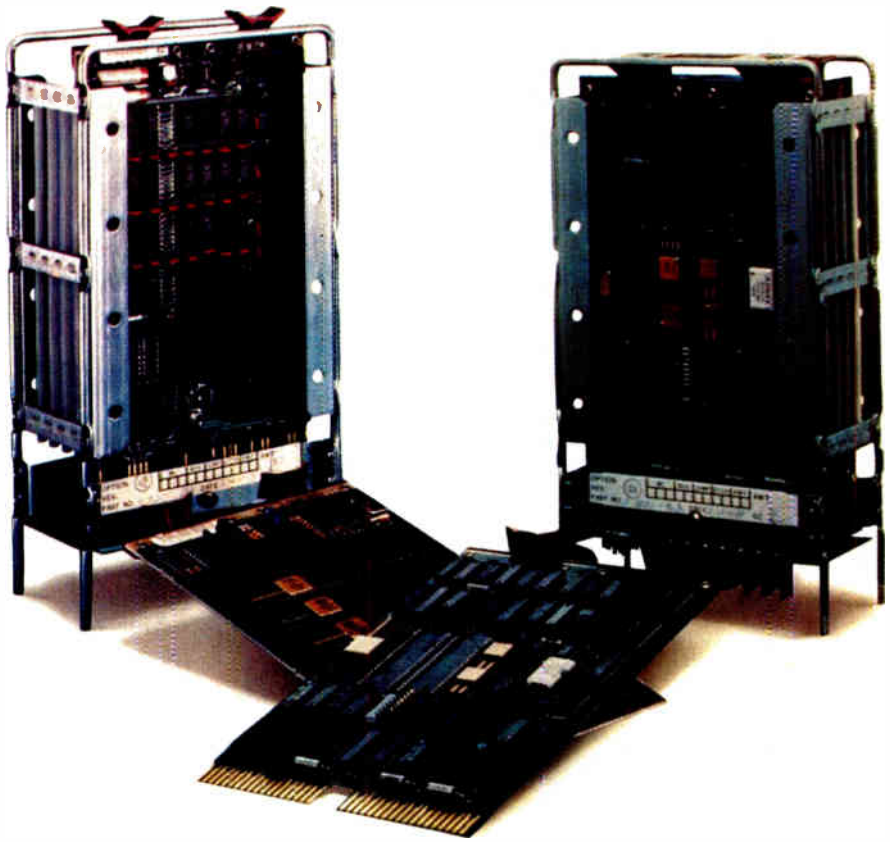

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Circle 15 on reader service card 15

its first product has hit the market, Allen Z. Kluchman, president, believes that "the minicomputer and mainframe businesses could learn a lot from the personal computer sector—there's a lot of creativity there, and the data-processing growth markets of the 1980s already are being foreshadowed by what's happening in personal computers."

And Kluchman knows whereof he speaks. Until recently he was Data General Corp.'s product line manager for small-business systems. In fact, though a consultant for much of the 1970s, the 42-year-old Kluchman was one of the company's first half-dozen employees back in 1968 after spending two years at Digital Equipment Corp. "What I learned about the business since then has encouraged me to enter software publishing," he says.

One of the things he says he has learned is that makers of minicomputers are hardware-driven and think of software as a necessary evil. But, Kluchman believes, with computers slipping out of the hands of data-processing professionals and increasingly into the untrained hands of management types, "what's needed is software that's almost foolproof, more capable than available programs, and supported by the highest-quality documentation."

First product. That is a partial description of Access's first product, a planning and simulation package called Supercomp [*Electronics*, April 7, p. 34]. "We wanted to offer managers and engineers a package superior to Personal Software's VisiCalc," Kluchman says, adding that VisiCalc "may be one of the best reasons to buy an Apple or TRS-80 since it makes them more powerful planning tools than many minicomputers—and some mainframes—with their existing software."

That last clause makes his position clear: "The software offered by hardware vendors will almost never make full use of their machines; the software hackers on the outside will almost always be able to offer a superior product if you can find it. We are doing the finding, the documentation, and the marketing." ☐

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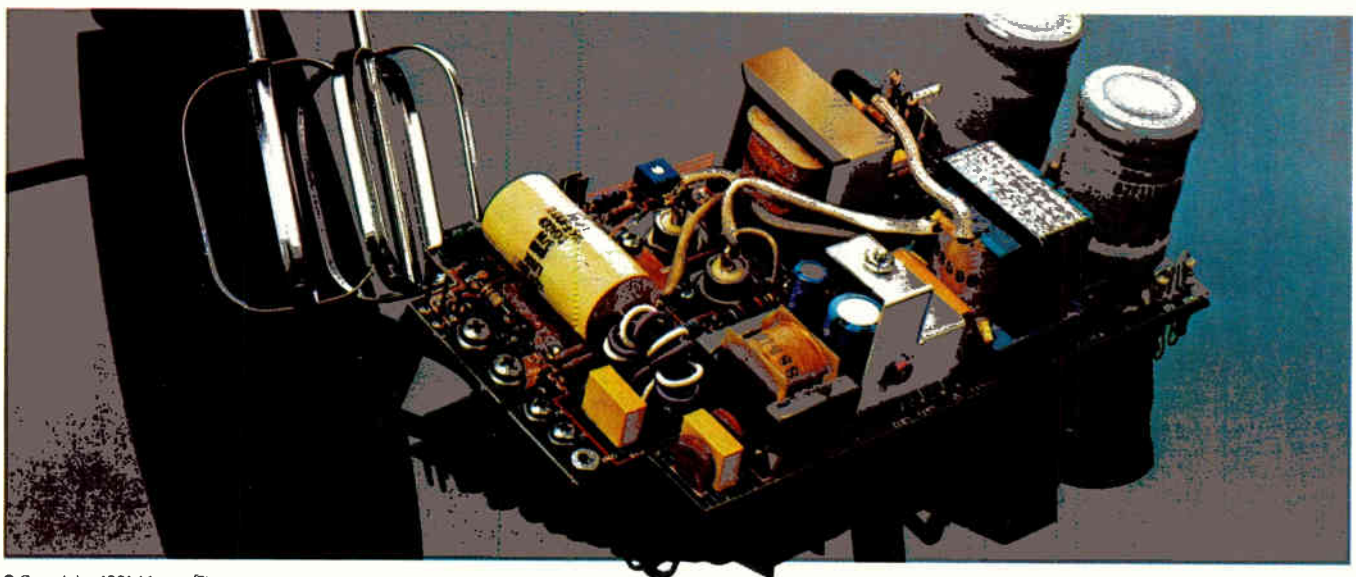

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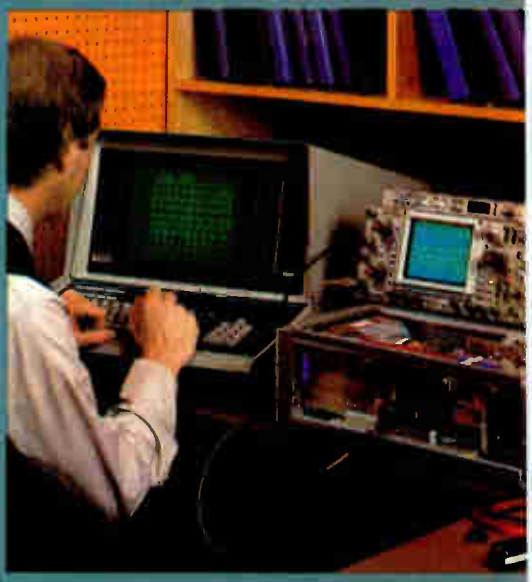

(above right) The Tektronix 468 portable digital storage oscilloscope becomes part of a powerful processing system when interfaced to the Tektronix 4052 Computer/Controller for analysis and processing.

(above left) Users can link the Tektronix 492P Spectrum Analyzer with the 4052 to compare accumulated displays over successive sweeps. Right at hand are high-speed analysis, plus permanent records via the Tektronix hard copiers.

(far right) The Tektronix 7854 Oscilloscope interfaces with the 4052 to apply high-speed floating point calculations and simultaneous display of high-resolution graphics and tabular data to the most complex analytical problems.

(below left) To state-of-the-art Tektronix GPIB waveform measurement instruments, you can add the analytical capabilities of the 19-inch 4054 computer/controller for problems requiring both speed and large data display; the fast 4052 for computationally intensive applications; or the economical, general-purpose 4051.

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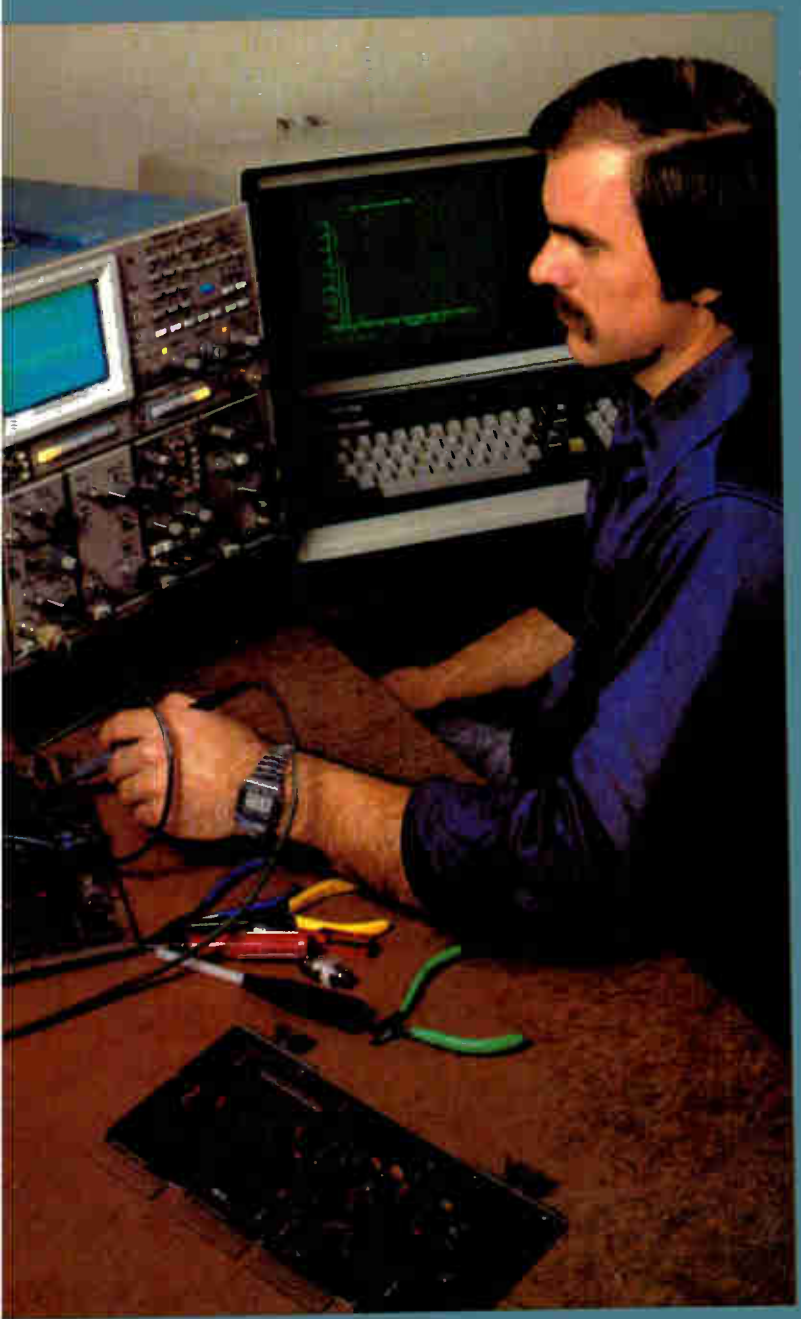

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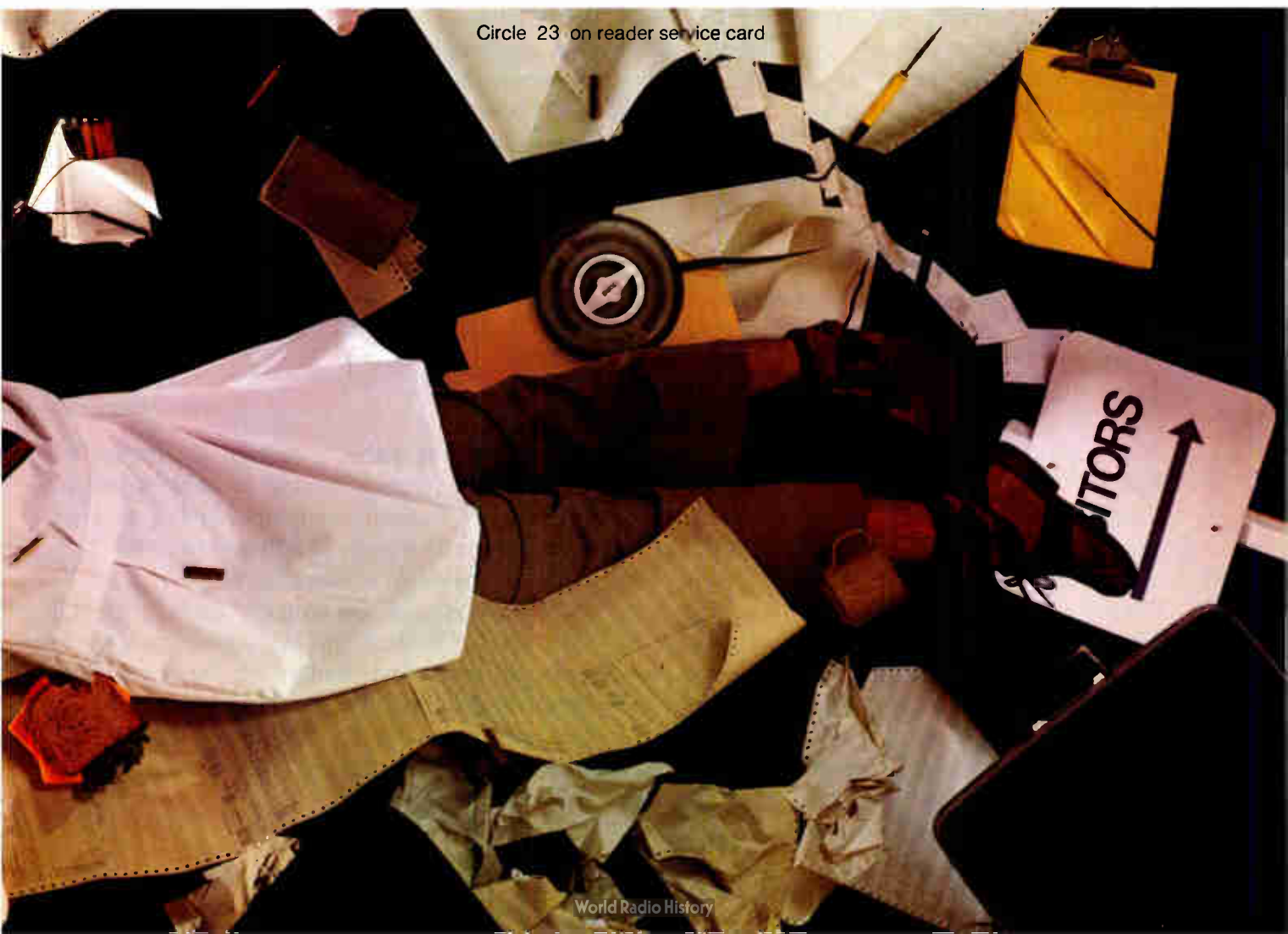

Editorial

What Americans are willing to do to aid the economy . . .

A basic American attitude has quietly undergone a complete turnaround during the last decade—one that bodes well for the economic future of the U. S. The change involves the reaction of labor leaders and workers to suggestions of increases in productivity, suggestions they have traditionally rejected out of hand. Their reasoning, that any such increases would result in a need for fewer workers while merely enriching management, was based on bitter experience from the long organizing struggles of the early part of this century.

Now, however, an ambitious and far-reaching study, "Perspectives on Productivity," sponsored by Sentry Insurance and conducted by Louis Harris & Associates Inc., shows that that is no longer the case. In the words of Harris, "the big news from the study is that America has gotten over the block, so long held, that productivity was either a bad word, a reincarnation of the Charlie Chaplin syndrome [in the movie "Modern Times," Chaplin personifies man against machine, human against the dehumanizing force of the production line] or a predatory device, cleverly designed by management for its own selfish ends." In fact, says Harris, "workers and businessmen seem ready to shift to productivity gains instead of inflation as the base for future wage increases."

Making the finding more significant is the fact that the poll was no ordinary man-in-the-street undertaking. The seventh in a series of such studies sponsored by Sentry, it was organized by the Harris organization and Amitai Etzioni, former senior economic policy adviser to the Carter Administration and one of the country's foremost thinkers on reindustrialization and productivity. Conducted in five nations, it included more than 1,200 executives, workers, labor leaders, consumer activists, and members of Congress, in the U. S.; each was interviewed in person and at length.

Of course, people in the electronics industries know the taste of high productivity—nowhere is the productivity rate increasing faster than among semiconductor makers [*Electronics*, April 7, p. 24]. Now it is up to the rest of the country to follow suit—the situation is, in the words of Harris, at a crossroads: the opportunity exists for doing something dramatic.

. . . and what they are willing to surrender

The Sentry study turned up another interesting and encouraging attitude. The American public, according to the poll's results, believes by a margin of more than 2 to 1 (64% to 30%) that it must make sacrifices in its standard of living and quality of life for the next few years to free more funds for investment and research as a means of enhancing economic growth. Although the principal leadership groups in the nation—business executives, labor leaders, members of Congress, and environmental and consumer activists—are less certain that sacrifice is worthwhile, the strength of the public's feeling on the matter could easily force a change in that direction. Incidentally, Federal regulatory officials are even more certain that some sacrifice is in order: 89% of those polled say it is necessary.

Legislators and government leaders should take careful note of this willingness to give in order to get. And leaders of the electronics industries in particular should be encouraged by this relatively new public awareness of the importance of investment and research to the well-being of the nation.

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TMS9995 — Key features

- 16-bit CPU
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- 256-byte on-chip RAM
- 16-bit on-chip interval timer/event counter
- 7 levels of vectored interrupts
- instruction prefetch
- automatic first wait-state generation
- MID — macro-instruction detect interrupt
- single 5-V power supply
- 40-pin dual-in-line-package.

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Three times faster than the TMS9900, TMS9995 executes a 16x16-bit multiply in just 7.67 µs. A 32-bit number divided by a 16-bit number in just 9.33 µs. TMS9995 can run with currently available fast memories of 120-ns access times, or by using automatically generated wait states, 450-ns access time memories.

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And, TMS9995 uses an intelligent pipelined architecture where the op code of the next instruction to be performed is prefetched. For example, the microcode for Branch and Jump instructions direct TMS9995 processors to prefetch the true next instruction instead of blindly prefetching from the next sequential memory location.

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Execution Time Benchmarks

	Automated Parts Inspection (Seconds)	Computer Graphics XY Transform (Seconds)	Bubble Sort (Millisec)	Block Translation (Millisec)	16 Bit Multiply (Microsec)	Single Vectored Interrupt (Microsec)
9995 (12 MHz) w/120ns PROM	0.666	0.863	1.240	1.767	10.00	8.0
9995 (12 MHz) w/450ns EPROM	0.950	1.081	1.956	2.696	12.67	10.67
8088 (5 MHz) w/450ns EPROM	1.596	2.402	2.254	1.522	40.8	77.6
6809 (2 MHz) w/450ns EPROM	9.67	57.1	2.376	3.01	91.9	27.6

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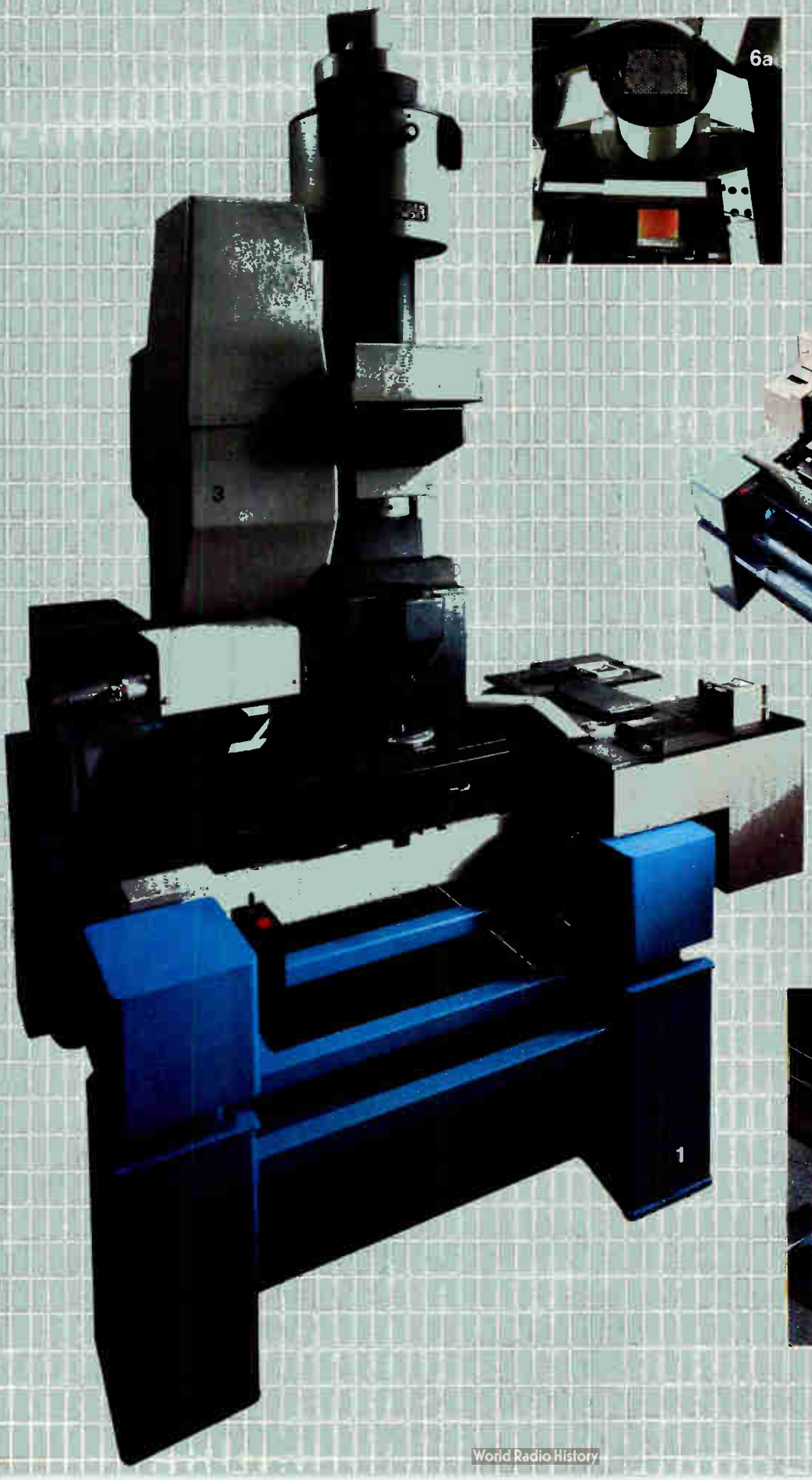

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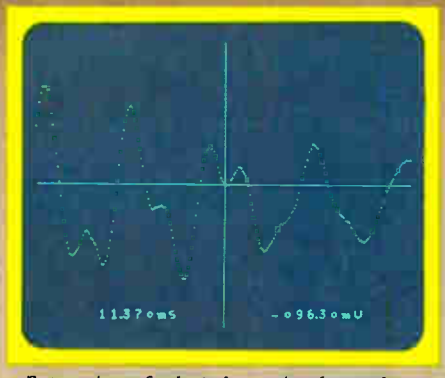

Expansion of selected area in above photo, for detailed analysis.

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Electronics newsletter

National to describe 4-Mb bubble structure

Even though many of the papers at next week's Intermag '81 conference in Grenoble, France, will cover contiguous disks and current-access technology, it grows more likely that the next round of commercial magnetic-bubble memories—the 4-Mb units—will stick with Permalloy chevron propagation patterns. At the conference, National Semiconductor Corp. of Santa Clara, Calif., for example, will disclose **a 4-Mb design that scales down a conventional block-replicate architecture to accept 1.5-μm bubbles.** The submicrometer gaps between chevrons were resolved with a wafer stepper; a thin-film detector, less than 1,000 Å thick, was added to sense the minute bubbles. A new combined swap-replicate gate was developed for the 300,000-mil² chip, organized by 8 bits, for a data rate exceeding 1.5 MHz at a 200-kHz coil frequency. However, the memory has yet to be fully characterized. In fact, a National spokesman says that "we won't even try to bring up yield on the part until next year."

Speed, resolution upped in electrostatic heads

A new approach to the construction of electrostatic print heads, under development at the Metrigraphics division of Dynamics Research Corp. of Wilmington, Mass., could lead to fast, inexpensive, letter-quality printers and graphics-output devices. When ready for the original-equipment manufacturer market, perhaps by year-end, **the devices could easily offer resolution as fine as 1,000 lines/in.** at little more than the cost of today's lower-resolution, 200- to 300-line/in. heads—and throughput could be impressive. Today's fastest line printers use costly electrostatic heads to generate up to 18,000 lines of copy per minute. The new heads are being developed using a technique combining the current-carrying capability of thick films with the fine resolution of thin films. Heads with 400-line/in. resolution have been built and employed already, and 800-line/in. test units have been prototyped.

Ethernet to get universal interface

Network interface units for Xerox Corp.'s Ethernet system (see p. 42) that also can hook up non-Xerox equipment will be supplied by Ungermann-Bass Inc. of Santa Clara, Calif. The units will be sold as the Xerox 872 and 873 communications servers and will be part of the Xerox 8000 systems, a variety of peripheral product designed for use with Ethernet. The 872 and 873 will provide four- and eight-user interface ports or system outlets **and will enable communicating Xerox 860 information-processing systems to exchange information within and between Ethernet networks.** Delivery of the units to Stamford, Conn.–based Xerox are scheduled to start in the fourth quarter.

Ka-band radar could boost mining safety

In a joint effort, scientists at the National Aeronautics and Space Administration and the Georgia Institute of Technology have developed a radar system that could possibly safeguard the health of coal miners. The 35-GHz radar, operating at about a 100-W output, would be mounted on coal-excavation machinery and used **to develop a pseudo–three-dimensional display reaching several feet into the surrounding rock and coal.** The system could track the meandering coal veins and spot voids in the rock. That, in turn, would allow remotely controlled operation of mining equipment, sparing miners the exposure to high concentrations of coal dust at the face, which is a key cause of black-lung disease. It would also remove the risk of cutting into voids that contain methane, reducing the dangers of

asphyxiation, explosion, and cave-in. Four prototypes of the radar were constructed at Georgia Tech's engineering experiment station in Atlanta.

New HP spinoff plans speedy 16-K RAM

Spun out of Hewlett-Packard Co.'s Cupertino, Calif., integrated circuit operation, Integrated Device Technology Inc. will soon make its presence felt on the market with a blazingly fast, low-power 16-K static random-access memory fabricated with its proprietary high-performance complementary-MOS process. Organized as 2-K words by 8 bits, the IDT6116, now being shipped in sample quantities by the new firm, will be available with maximum access times of 70, 90, and 120 ns, **making it the fastest byte-wide C-MOS 16-K static RAM available.** Although designed with 3-μm rules, the IDT6116 is built with a double polysilicon process that yields the smallest cell area (1.1 mil^2) and chip area (34,200 mil^2) in its class.

Sevin, Rosen entering venture capital arena

L. J. Sevin, former chairman of Mostek Corp., and semiconductor industry analyst Benjamin M. Rosen may be tying the knot on a venture capital partnership. According to Rosen, president of Rosen Research Inc. in New York and publisher of the Electronics Letter, **their activity will "generally be in the high-technology area,"** but not in electronics markets. Cash could come from the investment banking and securities firm of L. F. Rothschild, Unterberg, Towbin & Co. of New York, a leading underwriter of high-technology companies, which recently struck up a consulting agreement with Rosen. Sevin stepped down last year from the Carrollton, Texas, semiconductor house that he helped form.

VHSIC awards made to six companies

The Department of Defense has whittled down the number of participants in its Very High Speed Integrated Circuit (VHSIC) development program with the award of the first six contracts under Phase 1, pending contractor acceptance. **Awards range in value from $19 million to $35 million, with the three military services responsible for two each** [*Electronics*, March 27, 1980, p. 41]. Air Force contracts went to Honeywell Inc's. Aerospace and Defense Group in Minneapolis and Westinghouse Electric Corp.'s Defense and Electronic Systems Center in Baltimore. Army awards went to Hughes Aircraft Co.'s Strategic Systems division, El Segundo, Calif., and Texas Instruments Inc., Dallas. Navy winners were IBM Corp.'s Federal Systems division, Bethesda, Md., and TRW Defense and Space Systems, Redondo Beach, Calif. Passed over from the nine-company group that made up Phase 0 were teams headed by Rockwell International, General Electric, and Raytheon.

Addenda

As anticipated, Honeywell Inc.'s Micro Switch division **has jumped into the market for low-cost membrane keyboards.** Fourth-quarter production is slated for the Freeport, Ill., division's three new membrane products unveiled last week: a sealed, full-travel capacitance keyboard; a sealed, full-travel contact version; and a touch-panel keyboard. . . . **A $100 talking wristwatch has been introduced by Personal Electronics Inc. of New York.** Sharp Electronics Corp. of Osaka, Japan, makes the watch's complementary-MOS three-chip set: a 4-bit microcomputer, a speech synthesizer with on-board read-only memory, and a linear amplifier.

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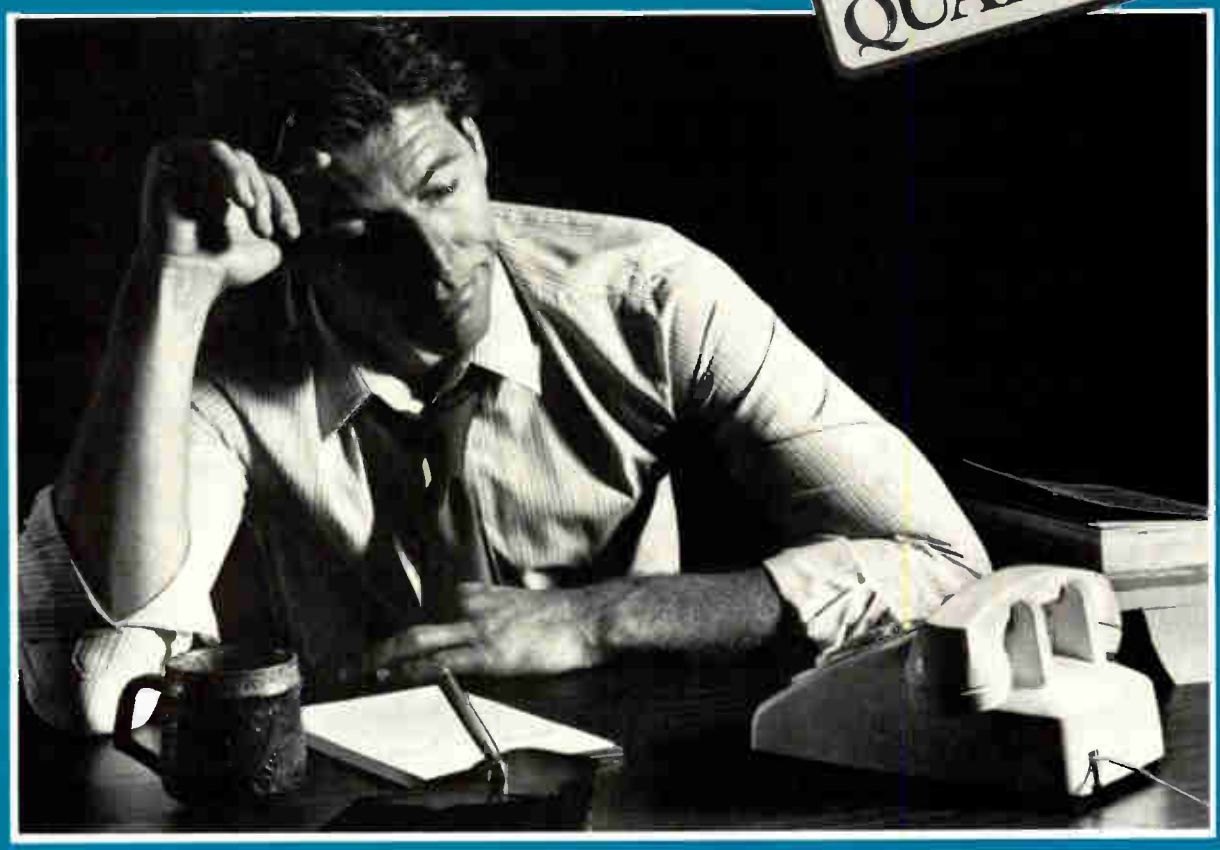

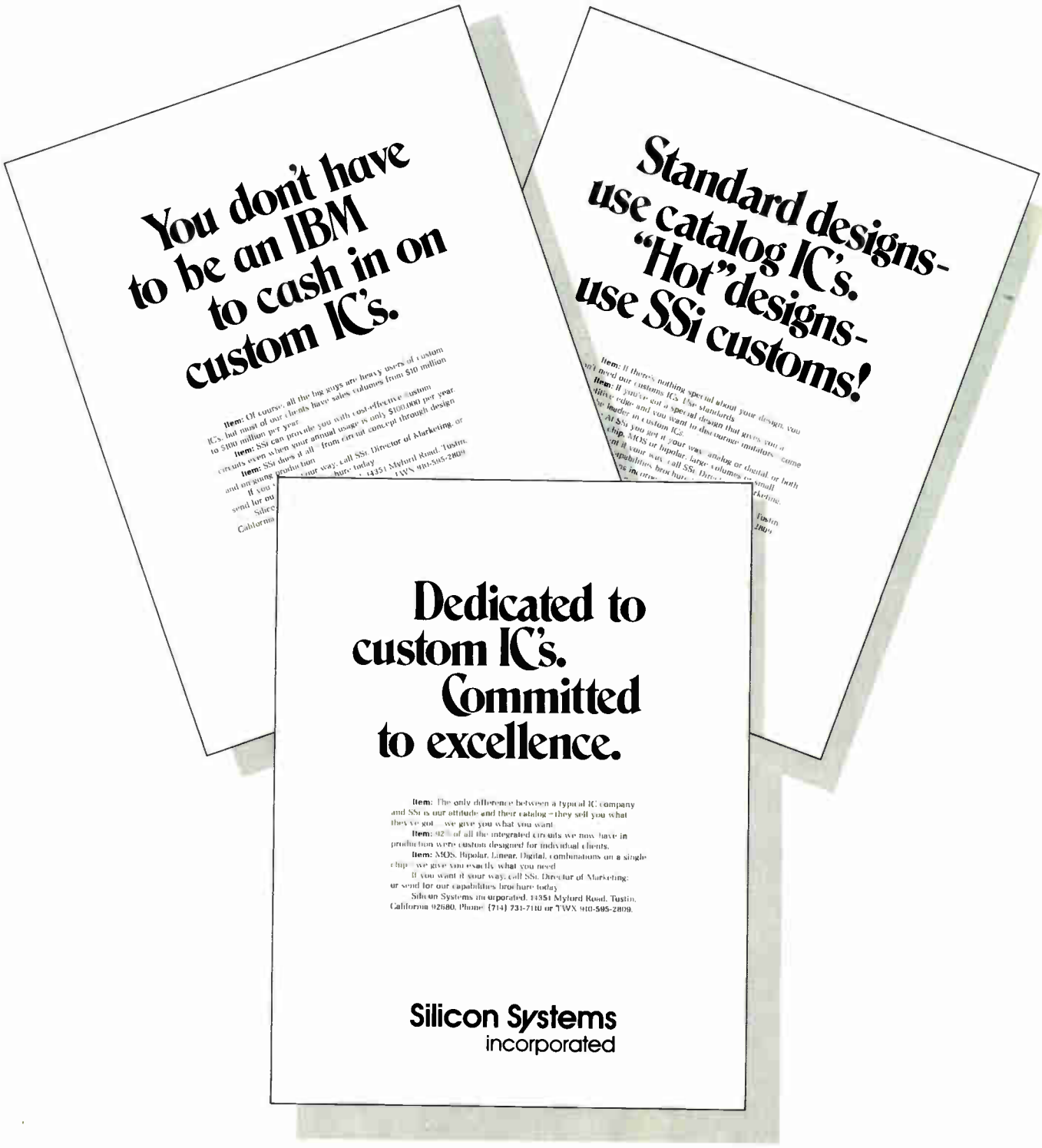

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3-d MOS FETs shrink static RAM cells and analog circuit blocks

by John G. Posa, Solid State Editor

Single device well merges two or more transistors; a differential pair fits in one well, a memory cell in two

A new three-dimensional cell structure that stacks one MOS field-effect transistor atop another may be the vehicle that will let static random-access memories win out over dynamic RAMs at future super density levels. It may also be the ticket to very large-scale analog MOS integrated circuits.

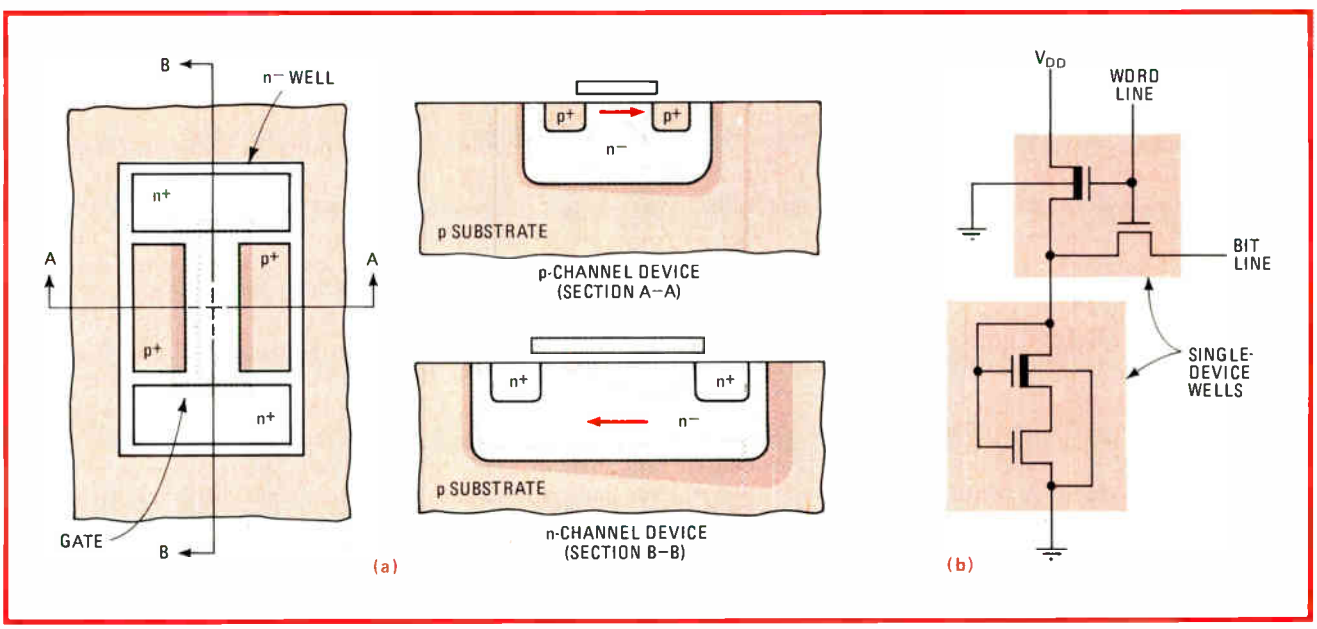
Going by the name SDW, for single device well, the structure has now been used to create a static RAM cell, using bulky depletion-mode load transistors, that measures only 600 square micrometers with 3-μm design rules.

The SDW approach was first described at the 1979 International Electron Devices Meeting by researchers from the University of Waterloo in Ontario and Bell-Northern Research in Ottawa, but two of its principal proponents have since joined Intel Corp.'s Aloha, Ore., memory division. One of the pair, Esmat A. Hamdy, says that Intel thinks the idea has potential, but its commercial application "depends on how much a big company is willing to take on a new device."

Also, Mohamed I. Elmasry, on leave from the University of Waterloo at the Microcomponents Organization of Burroughs Corp. in San Diego, Calif., is quick to add that analog LSI circuits, too, will benefit greatly from the technology. "With SDW, you can fit a differential pair and a current source in a single well," says Elmasry. "In other words, you can fit three devices in the space of one."

Input stage. Together, the differential pair and current source form the basic input stage for many important analog building blocks such as comparators and operational amplifiers. As few as two or three SDW units might make up an entire amplifier—albeit a crude one.

In the basic SDW structure, a single doped well contains a surface enhancement-type device and a buried depletion-mode FET that share a common gate. Part (a) of the figure shows how an n-well in a p-type substrate results in a p-channel surface device and an n-channel buried



A new dimension. A common lightly doped n-well creates two transistors perpendicular to one another (a), and two of the resulting structures can build a compact static RAM cell (b). Using C-MOS processing would add low power to the device's compactness.

device. (With the opposite well doping, the polarities of these devices, too, would be reversed.).

A lightly doped well is essential to SDW construction, since it forms the channel of the buried device, and the junction between the well and the substrate helps confine and control current flow. Only the technologies that offer both lightly doped n- and p-type regions, or wells, will support SDW logic: bulk complementary-MOS processes, C-MOS on sapphire, and structures that incorporate an isolated epitaxial layer to combine bipolar and MOS transistors on the same chip.

As shown in part (b) of the figure, two of the SDW MOS FETs are used to build a static RAM cell, one for the driver and the other for load and cell selection. The SDW driver transistors are interconnected to form a two-terminal device called a lambda diode.

Precedent. Merging transistor structures is a highly desirable approach, and other successes do exist. For example, in bipolar integrated-injection logic and the offshoot circuit forms it inspired, the collector of one transistor is the base of another. Similarly in the multiple-drain MOS process devised by the telecommunications laboratory of the French government [*Electronics*, June 5, 1980 p. 73], a single gate serves as the input for several output drain regions.

These approaches surely save room, but only in two dimensions. With SDW, the stacked devices share a common gate and, for further area compression, the bulk silicon performs an active role.

The approach has important attractions for future megabit semiconductor memories. At these very high density levels, the problems associated with storing, refreshing, and retrieving the diminishing charge packets in dynamic RAMs may dictate a switch to static cells.

The greater area required by static cells, however, will be crucial. The SDW cell is only slightly smaller than a static cell based on polysilicon loads—but in scaled-down geometries, poly loads increase a RAM's susceptibility to soft errors induced by alpha radiation.

For low power in addition to compact layout, standard C-MOS processing with the SDW structure presents "exciting possibilities," Hamdy says. Most C-MOS processes, as they now stand, could accommodate SDW memory cells or logic.

"Latch-up would not be a problem in an individual cell, because there is not a pnpn structure," explains Hamdy. There may be a latch-up path from cell to cell, "but you can probably get around that with oxide isolation."

If oxide isolation is used, a static RAM based on SDW cells could sport an access time as short as 50 nanoseconds—competitive with standard static memories using scaled-down technologies that can be applied to the new structure. The present power consumption of 10 microwatts per cell is high, but oxide isolation could halve that to a level competitive with n-channel cells.

Software

Compiler set unifies high-level languages for easy OEM multilingual capability

Opening the way for new multilingual computer systems, a family of compilers can implement several different high-level programming languages quickly and economically on a single machine. Language Processors Inc., a Belmont, Mass., software firm, says its compilers use a common intermediate language, optimizer, code generator, and run-time library—and adapt with relative ease to most 16- and 32-bit central processing units.

The source languages included are the American National Standards Institute's ANSI-74 Cobol, full ANSI PL/1 and PL/1 subset G, draft-ANSI Pascal, and ANSI-78 Fortran—as well as RPG-11, which is compatible with IBM's System/3. Also in development are compilers for Basic C, says president Michael I. Schwartzman.

The company developed its compilers under private contracts with some of the largest U. S. computer makers. Now it will begin marketing them to smaller systems makers and original-equipment manufacturers whose hardware is based on standard components and commercially available microprocessors.

"These represent a class of computers, priced at $60,000 and below, for which advanced programming languages generally present prohibitive development investments," observes Schwartzman. "We want to change that by simplifying the development of a compiler base and making that base support many different languages."

Shortcut. "A major computer maker can take from two to three years developing a compiler for a new system," points out John C. Ankcorn, vice president and cofounder with Schwartzman of Language Processors. "But we've gotten our compilers up and running on new processors in six to nine months." Thus smaller OEMs will be able to compete with the big systems makers, many of whose machines do offer hardware-specific multilingual capabilities.

The ability to add new languages on the same compiler base could encourage the use of affordable, highly specialized languages tailored to different applications, Ankcorn believes. That is preferable to using one very broad language like Ada, he adds, because it allows the most efficient execution of each function.

What eases the OEM's task is Language Processors' provision of a prototype code generator—a skeleton description that includes all major algorithms to be used. This reduces the individual manufacturer's development task to a few steps in working up the full generator.

Since the compilers are all written in PL/1 subset G, the newly devel-

oped code generator can be bootstrapped up on the target machine from a host computer equipped with a native compiler for that language. Once in place on a target system, the code generator can produce in-line code from all seven of the firm's language front ends, interfacing with them through the common intermediate language and optimizer, according to Ankcorn.

Interplay. The family's front-end compilers use table-driven parsers, which accept the source language with little deviation from its definition. The intermediate language specifies each source language down to the intermediate, or temporary, level. This, notes Ankcorn, isolates the code generator from a language's semantics and so eliminates generation of inappropriate codes for intermediate computation sets.

The common run-time library imposes uniform programming standards and nonconflicting assumptions about the execution environment for its language support routines. Thus, several languages can co-exist as modules of a single user program; each module can call any other module or any procedure in the run-time library.

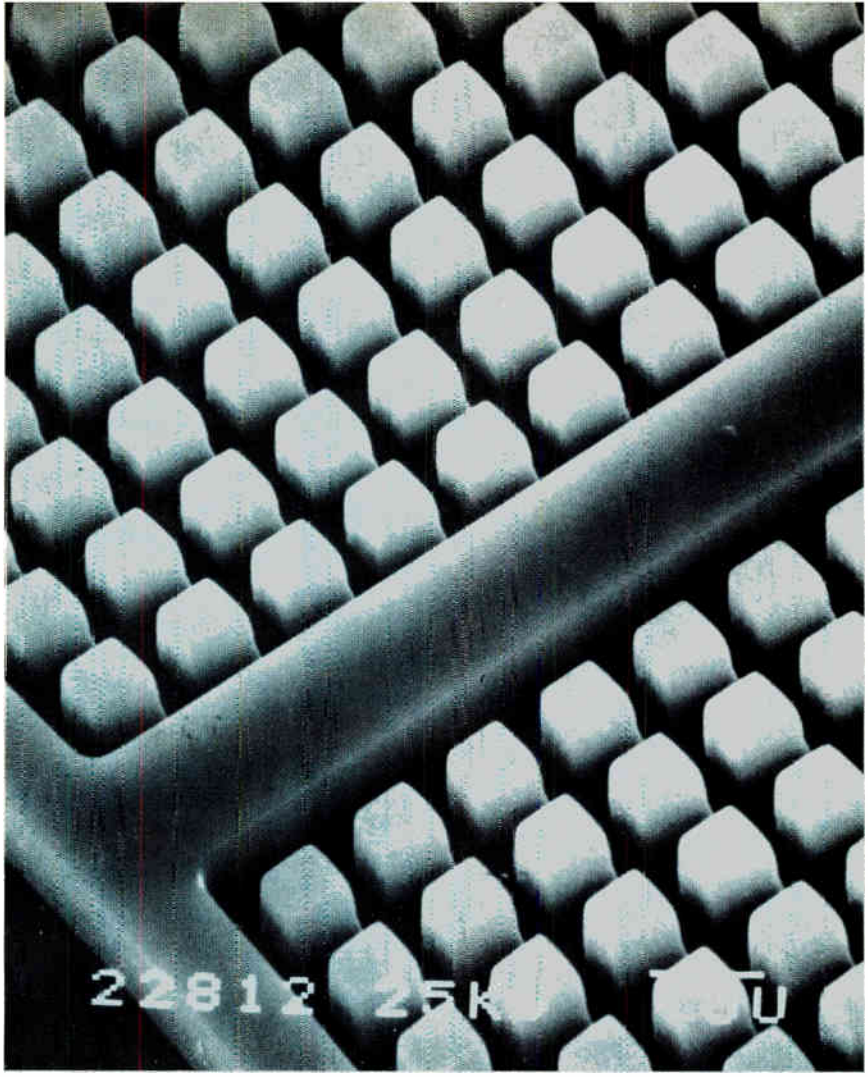
The prototype code generator costs $20,000. Licenses for the front-end compilers range from a low of $50,000 for Pascal to a high of $190,000 for full PL/1. **-Linda Lowe**

Production

Plasma etcher joins VLSI sweepstakes

With an eye to the VLSI era, Applied Materials, Santa Clara, Calif., has joined the lineup of companies with new plasma etching systems [*Electronics*, Feb. 24, p. 183], continuing the trend expected for dry process etching. Like others previously announced, Applied Materials' AME 8100 boasts superior anisotropy plus excellent selectivity and uniformities combined with high throughput.

The AME 8100 can handle the anisotropic etching of oxides, poly- and single-crystal silicon, silicon nitride, aluminum, and organic materials. Isotropic etching processes have also been developed for doped and undoped polysilicon.



Steep and clean. The AME 8120 achieves a steep profile and clean etching 2 micrometers deep with 1-μm spaces in single-crystal silicon (above) and can also handle polysilicon.

Results are impressive. For example, the high-resolution feature of a depth of 2 micrometers, etched in single-crystal silicon using a thermal oxide mask, exhibits very clean sides and a very steep profile without measurable undercutting and with only 1-μm spaces (see photo).

As for the all-important throughput, each production run will process 24 3-inch or 18 5-in. wafers at 65 to 93 wafers per hour, depending on their size, the thickness and type of material to be etched, and the amount of over-etch used. For example, for 5,000 angstroms of thermal oxide over silicon, the etch rate is 450 Å per minute and plasma etch takes 12 min, producing 65 wafers/h.

Selectivity is also good. Doped polysilicon on silicon oxide, for instance, can be etched at a rate of 1,000 Å/min with a selectivity ratio of 30:1.

Guaranteed. Aware of the many variables that can affect throughput, Applied Materials president James C. Morgan has announced a warranty that he says is the first in the industry. "We are guaranteeing such critical factors as etch rate, linewidth uniformity, selectivity, and even up-time of the system," Morgan states. Guaranteed uniformities are ±5% within a wafer, wafer to wafer, and run to run.

Designed by a team headed by Dan Mayden, a plasma etching specialist formerly with Bell Laboratories, the AME 8100 series includes two types of ion-assisted plasma etching systems that involve both chemical and physical reactions: the 8110 for dielectrics such as oxides and organic materials, with an up-time guarantee of 90%, and the 8120

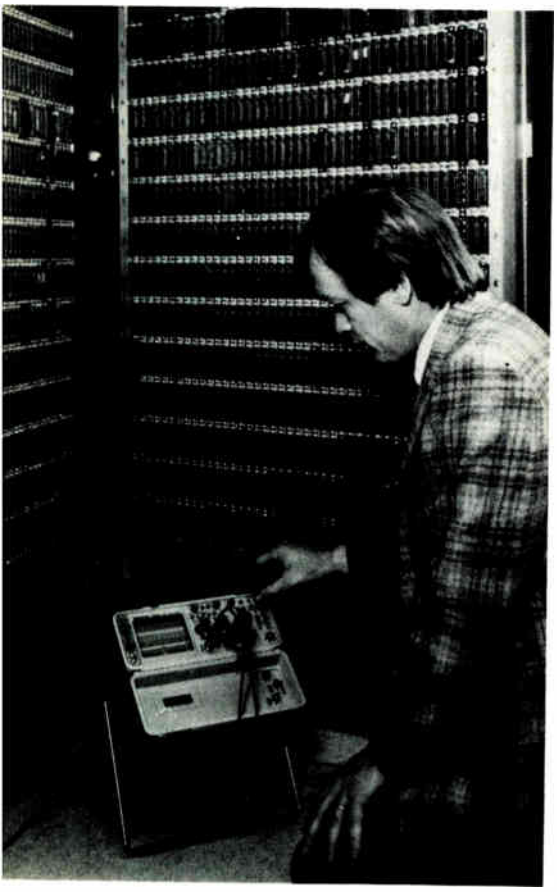
for interconnection materials such as aluminum and polysilicon with an up-time guarantee of 85%. Prices will range from $240,000 to $275,000. **-Jerry Lyman**

Instruments

Tougher scope takes on Japanese

Service scopes travel a lot more than they used to, and of late they seem to be traveling in lots from Japan to the U. S. With the availablility this month of its 2300 family of 100-megahertz oscilloscopes, Tektronix Inc. is beginning to address both these aspects of the service market.

The new instruments are the smallest and lightest 100-MHz service scopes. Their 5-by-12-by-17-inch dimensions give them one half to one quarter less volume than such scopes as Hitachi Denshi America Ltd.'s V-1050 and Kikusui International Corp.'s COS-6100. Also, the 2300 instruments weigh only 17.5 pounds, about 10% less than those units and 30% less than Tektronix's own 465, the industry workhorse whose market share the Japanese have been trying to erode.



Small and rugged. Tektronix designed its 2300 scopes for demanding field service, partly to counter Japanese competition.

The Japanese companies have gone after that market predominantly by adding more channels for logic analysis (the COS-1600 has three, the V-1050 four) while matching or beating the 465's price ($2,695 and $2,390, respectively, versus $2,600). Both Kikusui and Hitachi found that users wanted the extra channels to handle the added inputs and outputs digital equipment is likely to have over analog gear.

Tektronix's 2300 family still offers two channels, but it is considerably more rugged and better shielded against electromagnetic interference than the 465. Also, at a premium over the $2,775 base price, users can get delta-time and digital multimeter features without sacrificing compactness—their electronics fits into the scope lid, a feature one competitor calls "a super idea" that others are likely to adopt.

Changing times. The reason for the design philosophy, according to Michael Turner, a marketing manager for the Beaverton, Ore., firm's portable scope line, is that "the field-service environment has changed drastically over the last few decades." Today scopes must be carried through crowded urban areas and fit into some pretty small places—down manholes, for example.

Then, too, they may work near satellite up- and down-links and on industrial controllers, where high radiated fields can affect their performance if they are not well shielded. To meet all these requirements, Tektronix assembled a design team headed by John Taggart that incorporated mechanical engineers as well as electronics engineers.

Although Taggart had some initial misgivings about how the two sets of specialists would get along, he was glad to find that "the groups worked hand in glove together." For example, the EEs used a computer model to develop a cathode-ray tube about 30% shorter than the 465's, with half the spot size and yet highly readable. Looking out for ruggedness, the mechanical designers added supports for the electron gun to prevent vibrations from jarring it loose and breaking the CRT's glass sides.

Boosting g loads. Mounting the tube was given special attention, too. "Usually, tubes are compliance-mounted—there's a rubber gasket at the front panel and two support towers in front and in back," says mechanical designer Michael Kyle. He points out that this mounting method causes amplification of the g force on the back mounts during shock, which is where the tube is often damaged.

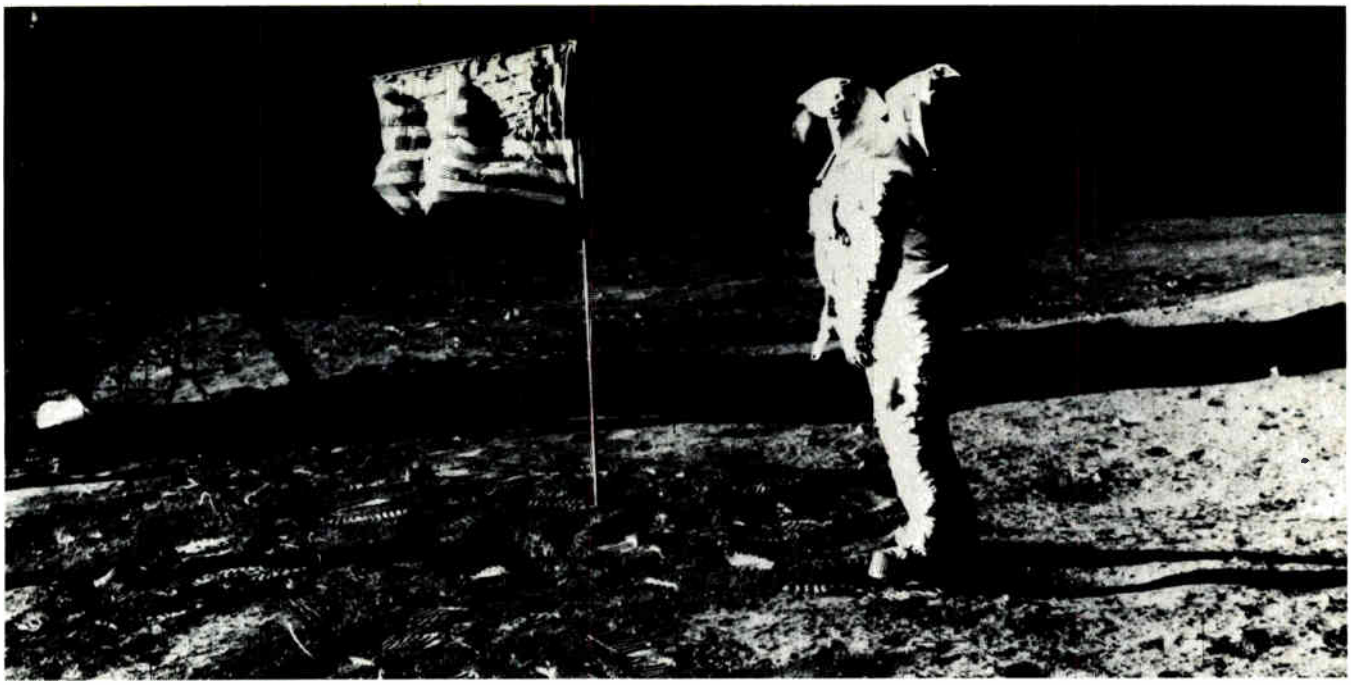
Therefore, in the 2300 series the CRT is cantilevered, with a ceramic funnel holding the tube to the instrument front panel with bolts. The end result, according to Kyle, is that whereas other scopes are rated to withstand 30-g shocks, the 2300 series is rated at 50 g.

The front panel and the cabinet are made of an aircraft-quality aluminum alloy, which provides high strength and shielding. The cabinet's main part is one-piece drawn aluminum, so the combination of material and design more than meets the goal of 10-volt/meter shielding. "Actually, we're seeing 20 to 50 V/m," Taggart says. **-Richard W. Comerford**

Information processing

Ethernet ICs to fit 3 popular processors

Joining the Ethernet sweepstakes, Mostek Corp. and Advanced Micro Devices Inc. will cooperate in developing the three basic chips that will interface systems based on 16-bit microprocessors with the Xerox-proposed local-network standard. Mostek and AMD are planning a general-purpose chip set compatible with the 8086, 68000, and Z8000, in contrast



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to Intel Corp.'s plans for interface chips compatible only with its own processor designs.

In announcing its cross-licensing agreement, Mostek of Carollton, Texas, and AMD of Sunnyvale, Calif., disclosed plans for two integrated circuits: an MOS protocol chip and a bipolar Manchester encoding-decoding serial interface adapter. In June, the companies will announce the third planned very large-scale IC, a bipolar transceiver.

Major functions. Together these chips make up the major functions required to interconnect office information-processing equipment and peripherals. In signaling its plans for similar Multibus-compatible chips, Intel of Santa Clara, Calif., also is announcing board-level versions for prototyping (see p. 224).

Intel, in fact, is collaborating with Xerox and Digital Equipment Corp. in promoting Ethernet [*Electronics*, Oct. 23, 1980, p. 42], so that it will become at the least a *de facto* standard. All these parts that will realize the protocol, however, are some time away: Intel is talking of at least six months for samples of its two-chip set, and Mostek and AMD say their samples will not be available until the second half of 1983.

The two companies' choice of processors to aim at with their chip set gives them an entry into Intel's target market and into their own markets (Mostek will make the Motorola 68000 and AMD is making the Zilog Z8000). "What we will be working on will be a protocol device that can interface very efficiently with at least these microprocessors, which we of course believe to be the leading products on the market," says James F. Vittera, strategic analyst for Mostek's planning organization for microcomputer and telecommunications products and the firm's program manager for Ethernet.

"We are working on a new architecture, which includes an on-board DMA channel" he adds. "I think it will be a unique solution to making peripherals mate with several different processors."

"That's one of our new strategies here at Mostek," he notes, "not to tie them to specific processors." Intel does have a vested interest in making its chip set compatible only with its own popular parts, but the tight coupling that will be possible should increase efficiency and speed.

Under the agreement, Mostek will be the lead designer for the protocol chip and AMD will lead the way on the Manchester encoder-decoder. The protocol integrated circuit may be designed to interface with 8-bit processors as well.

"We think of this chip as being the next generation of UART [universal asynchronous receiver-transmitter] chips," Vittera says. To meet Ethernet's rigorous speed requirement of 10 megabits a second, the company will use its Poly 5 scaled-down n-channel process, with which it fabricates random-access memories. **-J. Robert Lineback**

Ada and 68000 getting together

The new high-level language Ada and the 68000 microprocessor both are getting a boost in the announcement of the merger of a software house and a hardware-oriented company. The software house is Telesoftware Inc., producer of the first compiler for Ada, and the hardware maker is Renaissance Systems Inc., which has designed a 68000-based computer system to run software written in Ada.

Both firms are in San Diego, and the unified company, TeleSoft, will combine offerings. As well as the

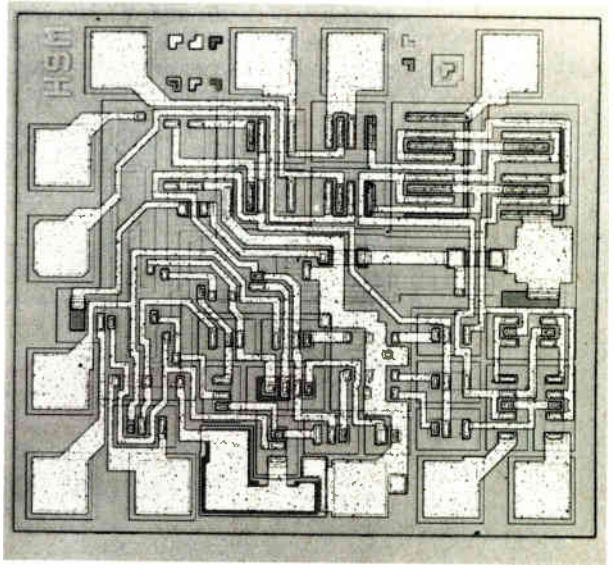
Video front end fits on chip

A juicy target for very large-scale integrated circuits that eliminate a maze of discrete parts are video systems, and Motorola Inc. is unveiling a linear modulator IC that takes a big bite. The bipolar MC1374 has an fm audio modulator, a sound-carrier oscillator, a radio-frequency oscillator, and an rf dual-input modulator in less than 50 mils square.

Such an IC is immediately useful for subscription and cable TV setups, where the coded signal enters the subscriber's home separated into its baseband video and audio portions. The 1374 will replace a package of discrete parts.

However, Motorola does have ambitious plans for its new IC. "In the playback mode, it is ideal anywhere for driving a professional-quality signal into a set," claims Ben Scott, manager of applications for linear operations at Motorola's bipolar IC division in Mesa, Ariz.

The modulator's fm audio distortion is less than 0.5%, making it well suited for reconstructing signals from both video cassette recorders and video disk players. One big attraction should be the chip's pricing—little more than a dollar each in volume quantities. **-Larry Waller**



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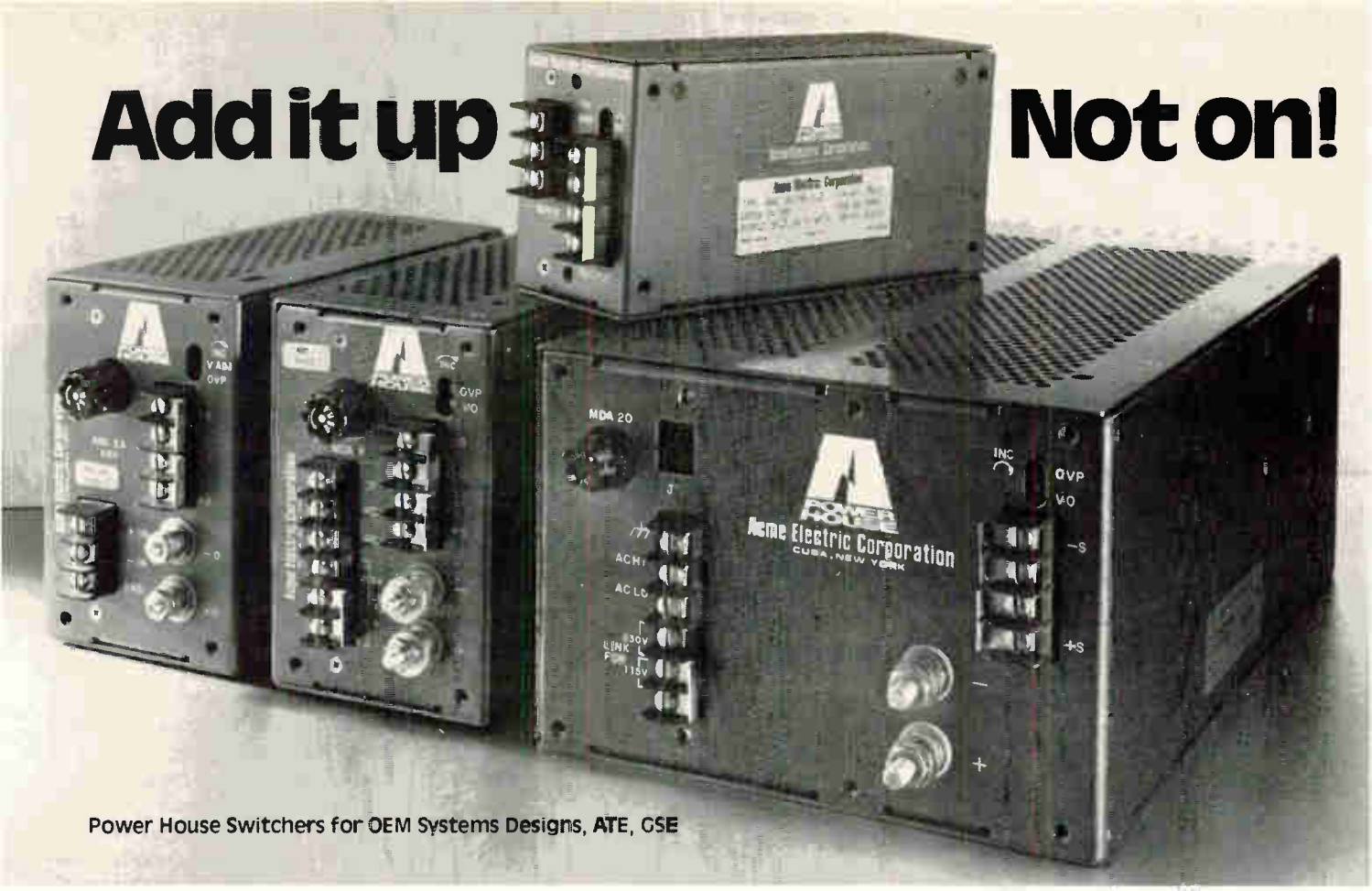

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Circle 45 on reader service card

Ada compiler and the TeleSoft-Workstation computer system, it will sell Ada modules through the GTE Telemail information network.

Telesoftware founder Ken Bowles will be board chairman of the new firm; it will also sell Renaissance Systems' non-Ada products, which generated $1 million in gross sales last year. The merger follows the announcement by Western Digital Corp. that it plans to develop its own Ada compiler [*Electronics*, March 24, p. 34].

Western Digital, in fact, has already announced the Ada Micro-engine, a 16-bit computer that uses Telesoft's present Ada compiler—but that license is likely to lapse now. A 32-bit machine designed for Ada is Intel's iAPX-432, and TeleSoft's interest in the 68000 will put this Motorola microprocessor into the running also.

Subset. The TeleSoft Ada compiler is a proper subset of standard Ada with no extensions, so that all software written for it will also run on any validated compiler. The company also is developing a full-blown standard Ada compiler that should appear sometime next year.

Written in Pascal, the Ada compiler generates an intermediate code that is conveniently translated into the target machine's assembly language. Currently it is supplied only with a 68000 translator, though an 8086 version will follow shortly, along with ones for the other major microprocessors, as well as versions for Digital Equipment Corp.'s VAX series and the IBM 370.

The TeleSoft-Workstation incorporates its 68000 processor in a DEC Q-bus backplane. It has a 4-megabyte (22-bit-wide) address space and comes with 256-K bytes of memory as standard equipment. Also standard are an intelligent terminal and dual floppy disks, with a 10-megabyte hard disk available as an option. The system will be priced around $7,000 ($2,295 for the processor board alone) and will be available at selected test sites in June.

Ada on the phone. TeleSoft's third major product may prove to be the most profitable in the final analysis: its ESP-Net, an abbreviation for electronic software publishing network. This service will permit users to review the catalog of Ada-based software available from TeleSoft, to examine the documentation, and ultimately even to download over the telephone software for which credit has been previously arranged.

Ada is perfect for this type of software publishing, since its strong modularity allows software components—packages in Ada—to be developed independently of any particular program or compiler. TeleSoft will develop its own Ada packages, but will primarily depend on independent programmers for whom it will provide the necessary marketing and pay the authors on a royalty basis. **-R. Colin Johnson**

News briefs

Xerox desktop computer simplifies user interface

Office-bound engineers, finance specialists, personnel staff members, and marketers need a desktop information processor that will operate with a minimum of keyboard entry, reasons Xerox Corp. So its 8010 Star information system uses a screenful of what Xerox calls icons—symbols of common office tools like the out basket and the file drawer—plus a hand-operated cursor positioner to select the operation quickly. For example, a user can call up a document from the file folder (in this system's memory), and if he then selects the printer icon and taps one of the few special-function keys, the document will print. Graphics capabilities and a high-resolution screen that will hold two displays—say, a page of text and an accompanying graph or chart or the page of icons—are also features. The basic Star work station will cost $16,595, and of course it is Ethernet-compatible.

Bar-code reader melds light-pen and laser scanner advantages

The latest in bar-code readers employs a strobe light, image sensor, and microprocessor-based image processor that quickly reads and processes a bar-code image and then decodes it—all in an 8-ounce easy-to-hold unit. The 20-20 instant bar-code reader from Norand Corp. combines the low cost of a light-pen scanner and the flexibility and accuracy of a laser scanner, maintains the Cedar Rapids, Iowa, company. The sophisticated optics let the user simply point the reader like a camera, while holding it as far away as an inch from bar codes of almost any size and legibility. The company expects the reader to appeal to makers of point-of-sale terminals and data-capture terminals intended for small and medium-sized business: the 20-20 unit should add $1,500 to the retail price of such gear.

Times are tough in Texas, too

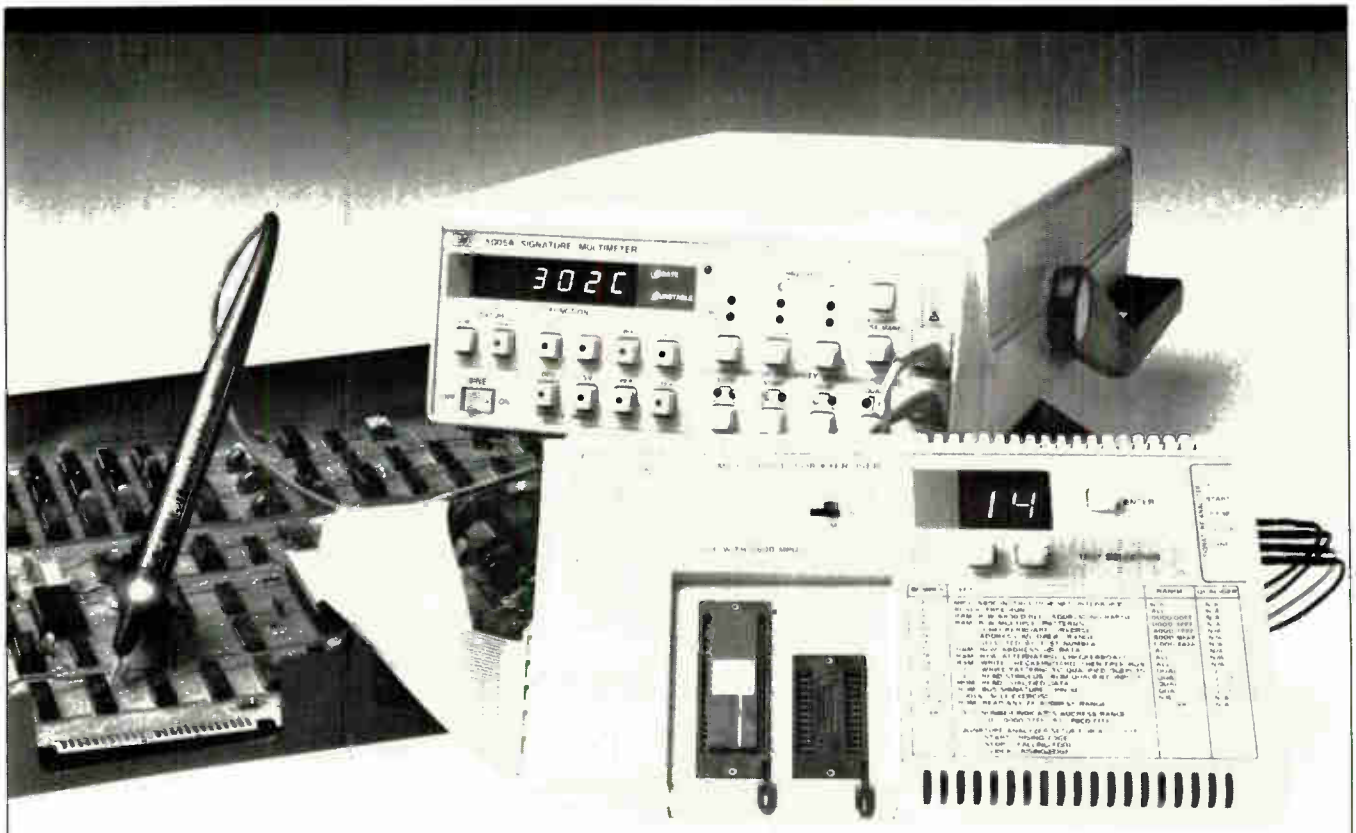
It's not just Silicon Valley that reports a softening semiconductor market; Texas-based industry leaders are reporting slowdowns, too. For example, Texas Instruments Inc. of Dallas saw its first quarter net income slump 32% over last year's—$34.2 million compared with $50.3 million—even though net sales hit $1.06 billion, up 11% from last year. The semiconductor industry worldwide has it equally tough—TI expects annual sales to slip 6% in 1981 from $13 billion to $12.2 billion.

In another sign of market softness there, Mostek Corp. in Carrollton has announced reduced work schedules, including a two-week shutdown of its main facility this summer and an additional 14 days off for its employees that will be scattered throughout the remainder of 1981. TI reports that 10% of its worldwide work force of 90,000 was on reduced work weeks in April, but that is down from 17% in January.

Aerospace

Timing glitch won't hobble space shuttle

When the space shuttle's primary set of guidance, navigation, and control computers is activated for liftoff next fall, there is a 1.5% probability of a timing-skew problem—the same



Now, HP has two more ways to cut digital troubleshooting costs.

5005A Signature Multimeter.

Before signature analysis (S.A.) troubleshooting microprocessor boards was tedious, time-consuming and costly. S.A. changed this by giving each complex bit stream its own unique hexadecimal signature, enabling technicians with minimum training to identify faulty nodes.

Now, the HP 5005A Signature Multimeter goes the next step by combining a high speed signature analyzer with a DMM, frequency/time interval counter and logic probe in one compact, lightweight package. This versatile combination adds a new level of convenience, making it easier than ever to track down faulty components in both service and production environments.

The 5005A Signature Multimeter offers features new to S.A.: preset logic thresholds for TTL, ECL and CMOS; variable thresholds (±12.5V); a clock-qualified Signature Analysis mode; and a 20 MHz clock rate coupled with a 10ns set-up time for high speed logic. It only weighs 8 lbs. (3.5 kg.), so it travels anywhere. The price is $2500*

5001A Microprocessor Exerciser.

Here's a simple way to take advantage of S.A., even if it isn't designed into your product. Just insert your board's microprocessor into the new HP 5001A Microprocessor Exerciser, plug the 5001A into the empty board socket, and use its ROM to run test stimulus programs. The 51 self-contained S.A. stimulus programs thoroughly exercise the microprocessor, buses, ROM, RAM and I/O circuitry. Easily monitor the resulting signatures at your product's test points with HP's 5004A or 5005A Signature Analyzers. The 5001A is available for the 6800 microprocessor now—8085 and Z80 soon. 5001A price is $900*

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software error that delayed the craft's maiden voyage April 10. However, the skew is no major concern, says Richard Parten, deputy director of data systems and analysis at the Johnson Space Center in Houston.

"The problem is random in nature," he explains. "It is the type that will never occur unless it exists at the time the redundant set of four primary computers is initialized." Furthermore, it is easily fixed by reinitializing the computers.

However, officials of the National Aeronautics and Space Administration did not know that on the morning of April 10, when they discovered a 40-millisecond timing error between the four primary computers and a backup unit—all IBM System/4 PI model AP-101 computers. The timing skew surfaced on the system's network signal processor at 20 minutes to liftoff, when the launch team tried to initialize the backup computer and get it into a monitoring mode.

At initialization. "The problem actually began before T−20 minutes," Parten explains. "It was induced 30 hours before liftoff when we initialized the first computer in the primary system." At that point the chain of events that led to a postponed flight began.

In this sequence, the primary system gets a timing reference to which it adds a compensating period for its own initialization. By mistake, the compensating period is 16 ms too short: this causes no problem, unless, as happened on April 10, the timing reference is less than 16 ms from the next time change.

To correct this situation, the primary computers' operating system is programmed to automatically skip a minor cycle, which lasts 40 ms. Because the backup computer was not receiving information in the proper time frame, "it in effect hung up the phone," Parten says.

"This skewing problem is completely transparent to the four primary computers, however." The primary units were programmed by IBM; the backup machine, by Rockwell International Corp., primary contractor on the orbiter.

"There will most likely be no changes in the software before the next flight," Parten says. "Now that we are aware of the potential problem, we will be looking for it after the computers are initialized.

"If the problem exists, we can take corrective action and reinitialize the primary system," he continues. "We then have a 98.5% probability that the problem will not occur. If it does, we will reinitialize it again." **-J. Robert Lineback**

Solid state

Josephson junction switches in 1 ps

Scientists at Bell Laboratories' Holmdel, N. J., electronics research facility have patterned a Josephson junction so small that it reaches its natural switching speed—about 1 picosecond. In a system where wiring delays and junction heating effects come into play, gates based upon the new device might achieve delays of less than 10 ps.

In the Bell junction, parasitic resistance and capacitance are so low as to be negligible. In other larger junctions like the kind fabricated at IBM Corp. and elsewhere, RC time constants produce signal delays and hysteresis that retard the fundamental speed of the Josephson device.

Scintilla. This 1,000-Å-square Josephson junction from Bell Labs subtracts parasitic delays from the device's true speed.

Bell's junction, fabricated by researchers Richard Howard, Evelyn Hu, and Lawrence Jackel, resembles a conventional junction. It consists of a base lead-indium metal and an overlapping lead stripe separated by a superthin insulating layer. The metal layers were thermally evaporated onto a silicon substrate.

But at 0.01 square micrometer, the junction area is less than a fifth the size of any other Josephson device. Indeed, this is the smallest object besides one-dimensional filaments yet patterned by humans.

To scale down that far, the team used an oblique-angle evaporation technique and a two-layer electron-beam resist to minimize overexposure caused by backscattering. The wafer is placed at an oblique angle so that the etched resist can be used as a shadow mask for the stream of evaporated particles, facilitating even finer geometry definition [*Electronics*, Oct. 11, 1979, p. 92].

Single vacuum. Since the superthin tunnel insulator is created by oxidizing the first metal layer, "all three steps—evaporation, oxidation, evaporation—can be done without breaking vacuum," says Hu. This results in a simple, self-aligned structure, she reports.

In addition the junction—the area defined by the overlapping of the second metal layer—was formed by slightly rotating the wafer with respect to the source before the second evaporation. This infinitesimal translation alters the angle of incidence and causes the second layer to be shifted enough with respect to the first layer to form the critical overlap.

Hinting at the intentions on the part of Bell Labs for the Josephson device, the researchers submit that the work is "an important advance in the evolution of superconducting junctions as practical, ultrafast, low-power switches for high-speed, densely packed integrated circuits—particularly for computing applications." The lack of hysteresis means

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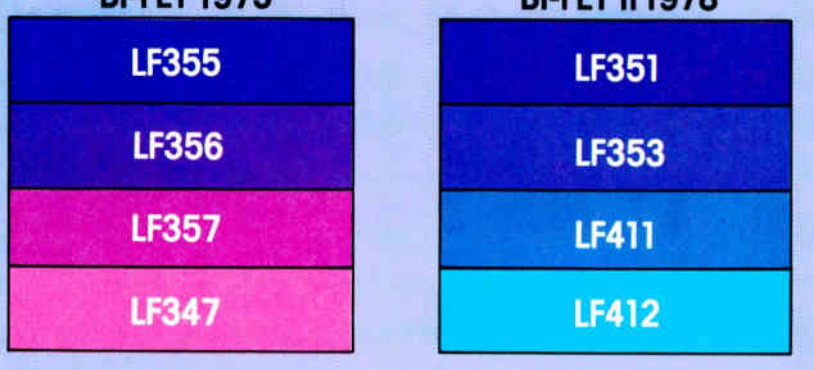

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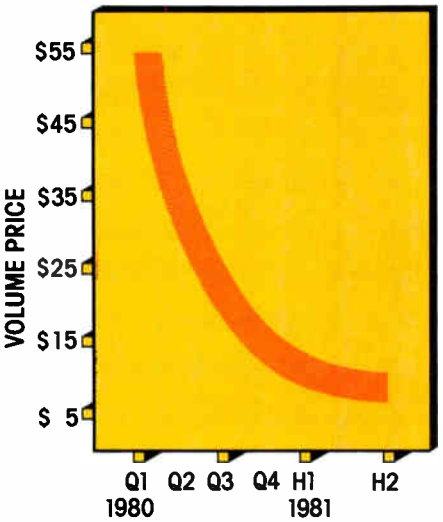

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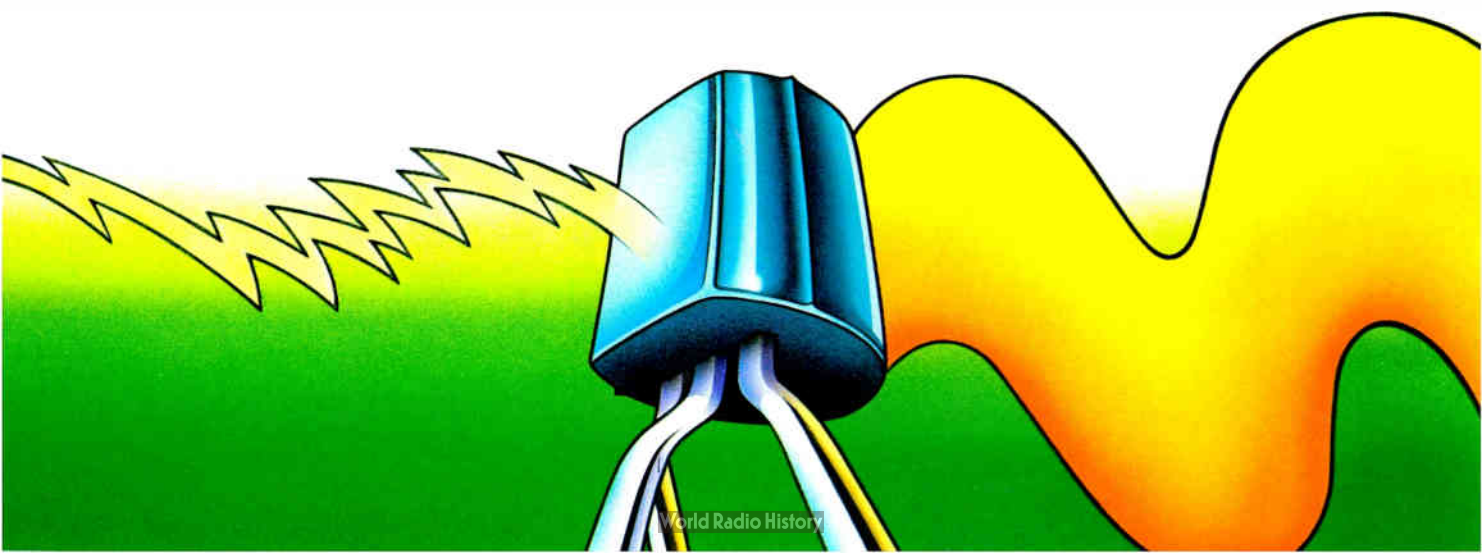

National conquers space with Megarad CMOS logic.

Presenting the industry's broadest line of metal gate CMOS devices capable of withstanding radiation levels in excess of 10^6 rads(Si).

Military and aerospace design engineers have long needed a dependable source of low power radiation-hardened logic devices. Bipolar components were radiation resistant, but required current supplies of several milliamps per gate. And although traditional CMOS operated at microamps per gate, they began to degrade at radiation levels well below 10^4 rads(Si).

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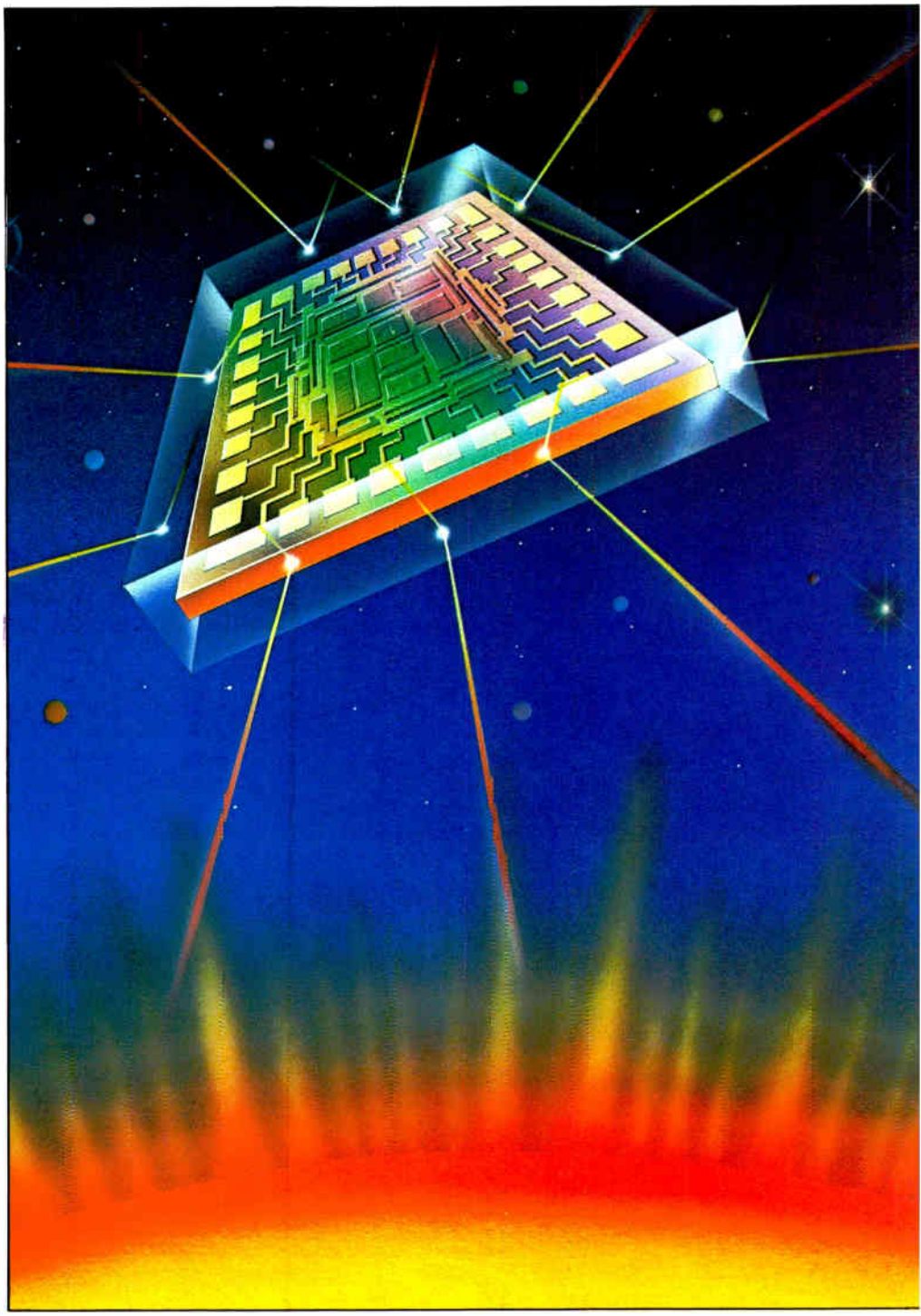
The radiation-induced oxide charge and the formation of Si-SiO_2 interface states were minimized by converting from a wet to a dry oxidation process, with the gate oxide thermally grown in a pure oxygen atmosphere rather than in steam.

This gate oxidation is processed through a nitrogen annealling cycle, thus producing oxides highly resistant to ionizing radiation effects as well as having excellent pre-radiation MOS characteristics.

Since the E-beam aluminum evaporation process normally used on commercial CMOS ICs emits a soft X-radiation—which produces positive charge threshold shifts in the gate oxide and interface states similar to those seen during radiation—National uses induction heated evaporation of the aluminum rather than E-beam aluminum evaporation.

To minimize the effect of threshold voltage shifts, the Practical Wizards significantly raised the negative threshold voltage and brought the positive threshold voltage closer to zero. This was accomplished with absolutely no sacrifice in performance, even on such complex components as the MM54C200 256-bit RAM.



Megarad for maxisystems. The result of all this Practical Wizardry is the industry's broadest line of reliable and readily available CMOS logic and memory devices capable of withstanding the rigors of a radiation-filled environment.

For more on National's rad hardened line of CMOS devices, check boxes 062 and 079 in this Anthem's coupon.

*One rad(Si) is the quantity of any type of ionizing radiation which imparts 100 ergs of energy per gram of silicon.

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The Perfect Match lights the way to LED uniformity.

New MV5X5X Series cuts LED system costs.

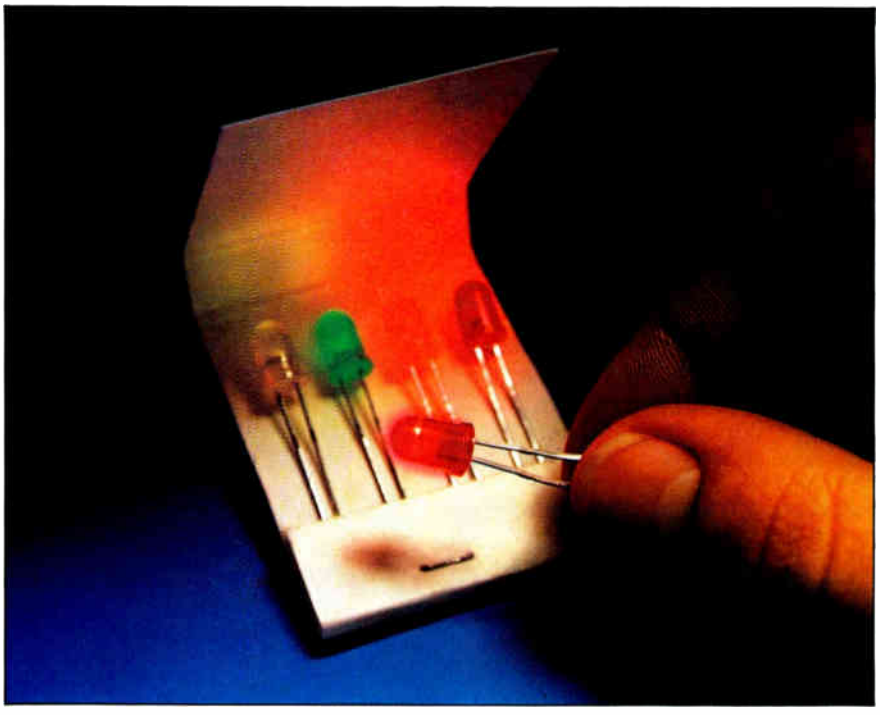
National Semiconductor takes the first big step toward opto standardization with their new MV5X5X Series of T-1 3/4 LED lamps. These lamps eliminate the need to maintain multiple application design standards to accommodate the various lamps available. As a result, LED system costs are significantly reduced and inventory control is simplified.

Mechanically and optoelectronically identical. The Perfect Match LED's are painstakingly engineered to exactly duplicate the popular industry standard lamps in lead frame size, bulb shape/height/diameter, standoff, color and diffuser level.

And they're now available in all five industry colors: standard red, high-intensity red, green, yellow, and high-intensity orange.

Check box 036 on the National Anthem coupon for complete information on National's MV5X5X Series of T-1 3/4 LED lamps.

The Perfect Match, another striking example of Practical Wizardry at its finest.



LED, LCD and VF drivers display family unity.

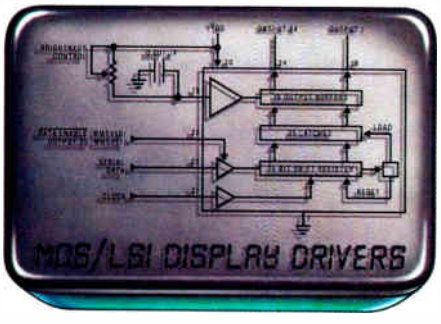
The Practical Wizards offer a complete family of software compatible MOS/LSI display drivers that use a simple serial interface to a μP bus.

National Semiconductor presents the industry's only true family of LED, LCD and VF display drivers.

Their broad line of compatible drivers is designed to meet all typical display driving needs in software controlled applications. So whether the design calls for LED, LCD or VF displays, the microprocessor, COPS™ Family or other microcontroller needs only one software routine to make the interface to any of the 40-pin drivers.

The practical approach. To make these devices even more practical and easy to use, they utilize a simple serial data input channel. In addition, the LED and VF drivers feature a continuous brightness control pin that respectively requires a current or voltage source.

As shown in the product summary table below, the Practical Wizards are offering four PMOS vacuum fluorescent display drivers. These parts, the MM5445/46/47/48, respectively drive 32, 33, 34 and 35 segment displays.



The NMOS MM5450/51 LED drivers can handle 34 and 35 segments, respectively. The CMOS MM5452/53 LCD devices drive 32 and 33 segments, respectively.

The remaining two family members, the MM5480/81, are lower cost LED drivers designed for smaller scale application needs. The 28-pin MM5480 drives 20 segments and the 20-pin MM5481 drives 14 segments. These parts are therefore not software compatible with the rest of the family.

The DATA ENABLE feature on the MM5445/46/52/81 allows these devices to be cascaded.

Once again, National Semiconductor comes through with a broad line of practical and reliable components.

For more detailed information, check boxes 044 and 053 on this issue's National Archives coupon.

COPS is a trademark of National Semiconductor Corporation.

DISPLAY DRIVER SUMMARY TABLE

PART NUMBER	DISPLAY TYPE	SEGMENTS DRIVEN
MM5445	VF	32
MM5446	VF	33
MM5447	VF	34
MM5448	VF	35
MM5450	LED	34
MM5451	LED	35
MM5452	LCD	32
MM5453	LCD	33
MM5480	LED	20
MM5481	LED	14

Titanium-tungsten fuses improve 16K PROMs.

The industry's largest bipolar PROMs from National guarantee an extra measure of reliability, thanks to titanium-tungsten fusing and today's high volume Schottky production processes.

National's technical expertise puts them out in front with significant bipolar advances that make practical sense.

Their 87S190 and 87S191 state-of-the-art 16K bipolar PROMs are an example. They're as fast and as large as any in the industry. And yet their titanium-tungsten fusing and high volume Schottky production process gives them rock-solid reliability.

These high-speed PROMs are Schottky-clamped for a typical address access of 40 ns and a typical enable access of 20 ns. In addition, they use PNP inputs to reduce input loading. And they incorporate TRI-SAFE™ for low voltage programming, with all DC and AC parameters guaranteed over temperature.

Fuses that last. National's titanium-tungsten fuses are made of a very stable and reproducible metal combination which resists oxidation.

National uses an on-chip Darlington programming circuit that "pulse shapes" the programmer's input and sends a very fast, high energy current pulse to the selected fuse.

This minimizes local heating and produces a wide gap in the fuse link. One free of residual conductors and without deteriorating hermeticity. It all results in a very reliable PROM.

Additionally, the titanium-tungsten fusing allows a low 10.5V programming voltage. And that eliminates the need for guard rings and wide spacings.

Reliable PROMs from proven processes. As an additional measure of practical reliability, this family of PROMs uses titanium-tungsten as a buffer between the aluminum interconnect and the platinum-silicide "barrier." They use the same basic production flow as for standard Schottky bipolar RAMs, ROMs and other logic circuits. It's a proven process that works time-after-time.

National's tight quality control and practical innovation pay off in highly reliable, high volume products. In the TRI-STATE™ PROMs, for example, only 11 failures have been observed in 2.7 million hours of testing. And not one of the failures was fuse-related.

So you can't go wrong with National's 16K bipolar PROMs.

The product table in this article gives the part number, organization and T_{AA}. But, for more information on these and other long-lasting memories check box 043 on the National Anthem coupon.

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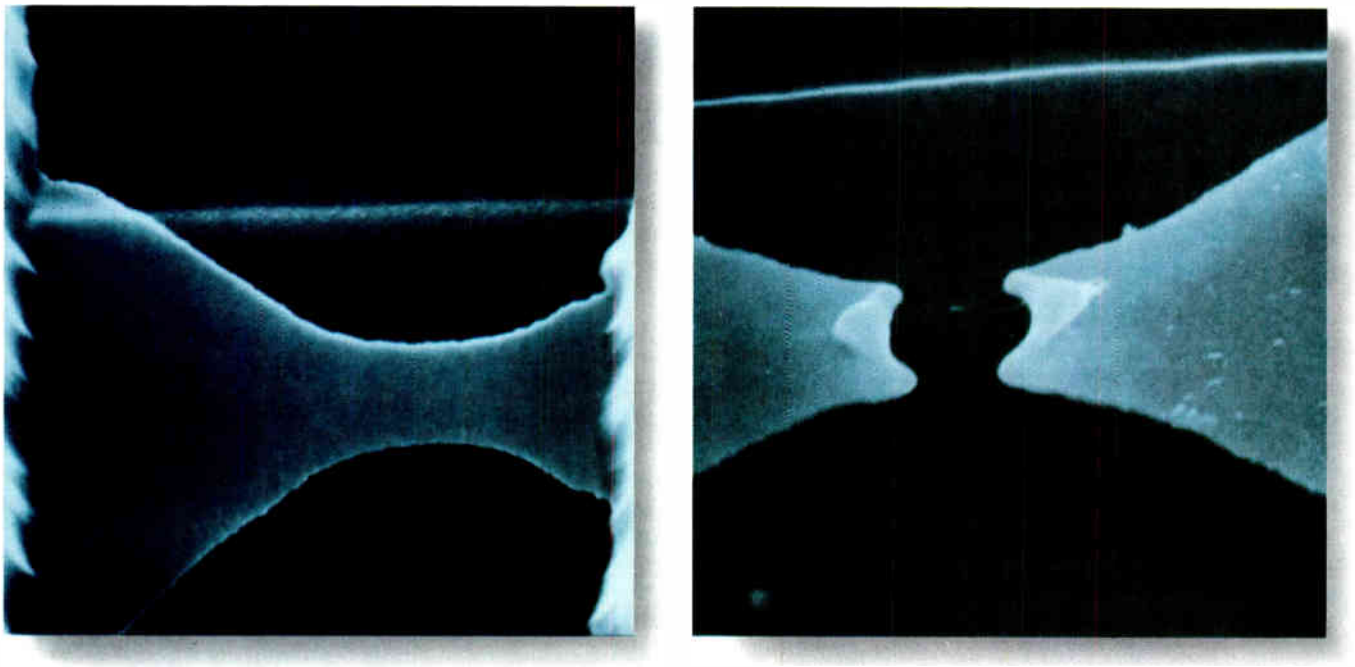
PROM SUMMARY TABLE

PART NUMBER	T_{AA} (MAX COMM)	ORGANIZATION
DM74S188/288	35	32 x 8
DM72S287/387	50	256 x 4
DM74S570/571	55	512 x 4
DM74S472/473	60	512 x 8
DM74S474/475	65	512 x 8
DM74S572/573	60	1024 x 4
DM87S180/181	55	1024 x 8
DM87S184/185	55	2048 x 4
DM87S190/191	65	2048 x 8



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P²CMOS STATIC RAM FAMILY

Part Number	T_{AA} (ns)	Organization
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NMC 6518	180-300	1K x 1
NMC 6551	220-350	256 x 4
NMC 6552	220-350	256 x 4
NMC 6503	300-350	2K x 1
NMC 6504	300-350	4K x 1
NMC 6513	300-350	512 x 4
NMC 6514	300-350	1K x 4

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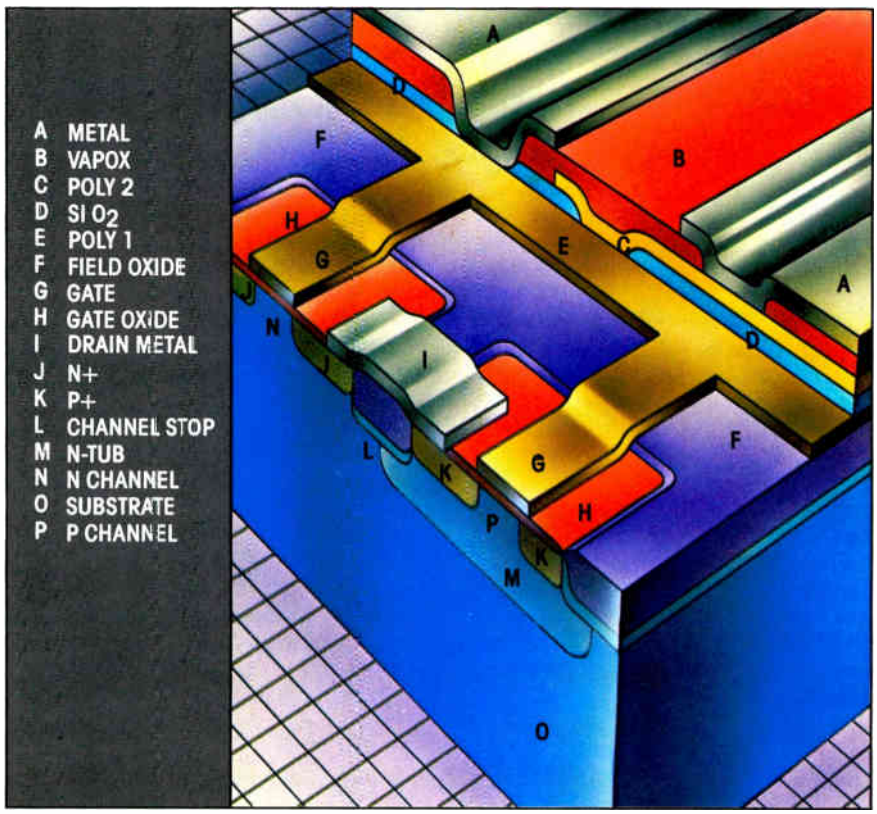

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Electronics review

the junction could be used "as an extremely sensitive magnetometer or as the basis for a nonlatching logic family," remarks Hu.

Even though Josephson integrated circuits have remained in the lab awaiting solutions to problems like economical supercooling and interfacing with room-temperature input and output, "as with semiconductors, you need devices that are 5 to 10 years more advanced so you'll have them ready," the Bell researcher says. **-John G. Posa**

NCC

New matrix printers needling daisywheels

Dual-function dot-matrix printers that can provide either near–letter-quality printing for word-processing applications or lower-quality data processing printouts at high speeds abound at the National Computer Conference this week.

Several of a new breed of printers that use additional wires and dot needles to achieve high-quality output will bow, joining previously announced multiple-pass printers. The goal is to rival the daisywheel printers commonly used in word-processing systems but still offer the high-speed output that matrix printers can achieve. With more printhead needles, the dots fall closer together on the paper—in fact, they overlap—producing the near–letter-quality result.

Prices for the new matrix printers range from about $1,500 up to $2,700 in quantity. Daisywheel printers cost around $3,000.

Among those introducing printers using from 14 to 18 needles instead of the usual 9 are Dataproducts Corp. of Woodland Hills, Calif.; Anadex Inc. of Chatsworth, Calif.; and Amperex Electric Corp., Hicksville, N. Y. Olivetti Peripherals Equipment Corp., Tarrytown, N. Y., is displaying first evaluation units of the DM 80/180 printer it announced late last year. Additional introductions are expected from Japanese

is what is the level of acceptance in the marketplace. The industry has to find a level, and that is still to be set," he observes. **-Terry Costlow**

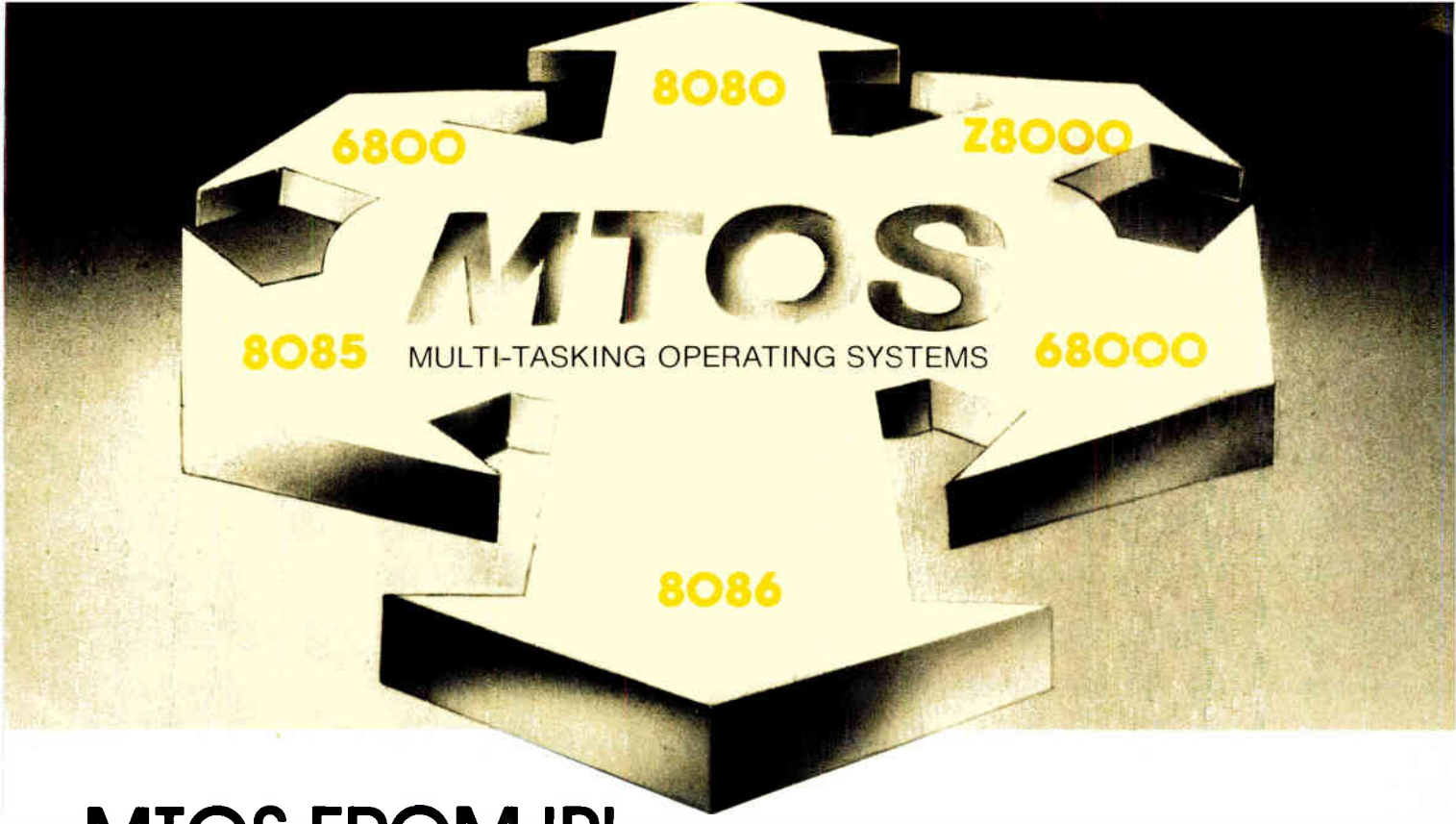
Voice controls image processor

Digital image processors are sometimes operated in a darkened room and require close attention to the display screen, making them difficult to address through a keyboard. A 3M Co. subsidiary, Comtal Corp. of Altadena, Calif., this week is demonstrating at the NCC one solution—voice command.

The goal is to free an operator from the sometimes-tedious keypunching involved in manipulating graphics material on the processor screen, explains Ken Marshall, Comtal regional sales manager. To accomplish this task, Comtal mated a voice recognition module made by Interstate Electronics Corp., Anaheim, Calif., with its own new Vision One/10 image processor.

At the heart of the marriage between these two technologies is operating software that converts digital voice commands into data input compatible with the image processor's format. The program is stored on cassettes contained in a Digital Equipment Corp. VT103 terminal that serves as a controller in the present prototype. If the voice-controlled processor develops into a product, the software will be resident in the processor's cabinet.

The initial research and development on the software took place in St. Paul, Minn., at parent 3M, which then assigned further development to Comtal. At present, voice commands are limited to the 100-word vocabulary of the Interstate module, but these are adequate for executing the basic operations of the image processor. All aspects of manipulating the image are contained in such speaking commands as "zoom" or "smooth image." "Everything that can be done at the keyboard can be done with voice," states Marshall in summary. **-Larry Waller**



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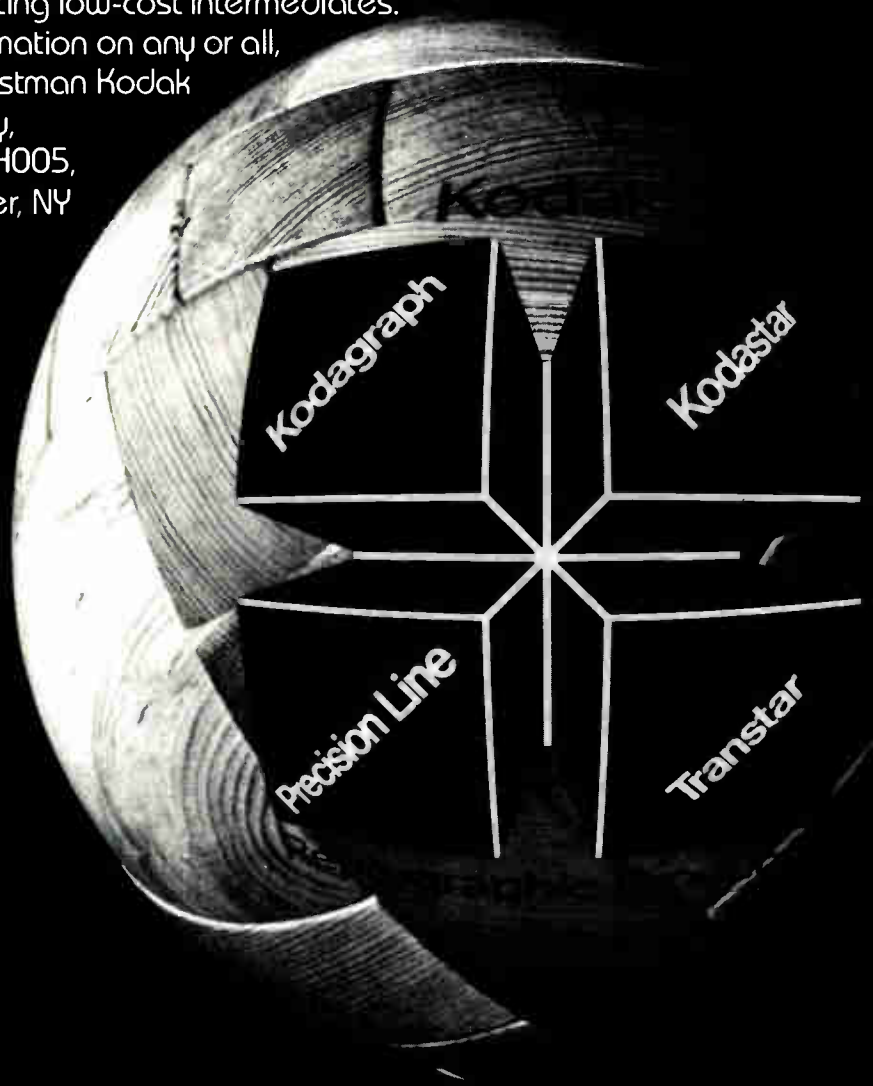

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Washington newsletter

Users of 12.1 to 12.3 GHz see interference threat

A conflict is brewing over the Federal Communications Commission's first approval of direct broadcast satellite service in the 12.1-to-12.3-GHz range. In granting authority to Satellite Television Corp., a subsidiary of Washington, D. C.–based Communications Satellite Corp., to begin building satellites to transmit to small ground-based antennas, the FCC aroused the ire of users who must now share that frequency band. Fixed-satellite services and some local broadcasters see the threat of interference from the new service. **Nevertheless, the FCC called for other applications** under its new interim policy that will be subject to review in 1983 at the Regional Administrative Radio Conference of Western Hemisphere nations. First to respond was the newly formed Direct Broadcast Satellite Corp. of Washington, D. C., headed by former Comsat vice president Wilbur Pritchard. DBS says it will apply within six months.

Reagan criticized for low science priorities

The likely confirmation of two top scientists in the Reagan Administration has some Republican congressional insiders worried. They see a low priority in the White House for nonmilitary science, technology, and space policy issues, despite the President's declaration that the first success of the space shuttle has "started us dreaming again." The two nominees are George Keyworth, physics department chief at Los Alamos (N. M.) Scientific Laboratories, for science adviser to the President and James Beggs, General Dynamics Corp.'s executive vice president for aerospace, to head the National Aeronautics and Space Administration.

Responds one Senate technology specialist, "Keyworth may be quite competent, but he is an unknown in the science and technology community. **That supports speculation that the science adviser will hold little more than a *pro forma* position.** Beggs should be good for NASA, but he will have little to spend." NASA's thin budget is forcing it to merge its Dryden Flight Research Center in Edwards, Calif., into Ames Research Center in Mountain View, Calif. Also, Goddard Space Flight Center in Greenbelt, Md., is taking over Wallops Flight Center, Wallops Island, Va.

Congress, DOD set procurement reviews

A broad study of military procurement practices—with emphasis on "waste and mismanagement," a favorite Reagan campaign theme—is being started by New York Democrat Joseph Addabbo, chairman of the House Appropriations defense subcommittee, according to staff members. At the same time, **the Pentagon has come up with 26 recommendations to implement its revisions** in the planning, programming, and budgeting system designed to give the military services more flexibility and responsibility for systems research, development, and procurement.

Addenda

Federal approval to export microprocessor development systems to China is being sought by Intel Corp. A Commerce Department group is considering industry proposals **to permit the export of microprocessors to countries on the U. S.'s most-favored nations list.** . . . The push to open the Nippon Telegraph & Telephone Public Corp. market to U. S. suppliers (see p. 110) will continue in June with **a visit to NTT officials sponsored by the Commerce Department.** The immediate result is that the Electronic Industries Association has been forced to cancel a similar trip.

Washington commentary

The good news from DOD—and the bad from OMB

Military electronics contractors and their customers are delighted with the dollar increases proposed by the Reagan Administration for fiscal years 1981 and 1982, as well as forecasts for the years beyond. Even though fiscal 1981 is more than half over, the President wants Congress to raise the Defense Department's budget authority by $6.8 billion to a $177.1 billion total. Actual spending would rise by $1 billion from the Carter Administration's level of $158.6 billion. Changes for fiscal 1982, beginning this October, would set a peacetime record of $221.5 billion in budget authority, with spending at $184.8 billion—increases of $25.8 billion and $4.8 billion, respectively, over the present Carter budget [*Electronics*, Feb. 24, p. 63].

Contractors are also pleased with Defense Secretary Caspar W. Weinberger's late-March revision of the Pentagon's system for planning, programming, and budgeting that will decentralize weapons acquisition. The revision gives each service control over its own buys and holds each accountable for program planning that can be integrated into a workable national defense posture by Weinberger and his top aides.

New ground rules

Given this new autonomy—"participative management," as Weinberger's deputy, Frank Carlucci, likes to call it—the Joint Chiefs of Staff and the three service secretaries are expected to cut paperwork in half and get systems into the field faster.

Nevertheless, there is another element in the Weinberger spending program that has contractors nervous. David A. Stockman, director of the Office of Management and Budget, has ordered the DOD inflation factor reduced from the level of the Carter Administration, which many considered unrealistically low.

Recent annual inflation factors for many weapons have been running at 12%, with some aircraft and ship programs topping 20%. Stockman has ordered the fiscal 1981 factor dropped to 10%. For fiscal 1982, the rate is down to 8.7%. For future fiscal years, the OMB has set the Pentagon inflation rate at 7.3% compared with Carter's 8.5% for fiscal 1983; at 6.2% compared with 8% for fiscal 1984; and at 5.5% for both fiscal 1985 and 1986, nearly two points lower than the Carter plan.

Contractors, however eager they may be to hold down costs, do not believe the new numbers, particularly in view of the record military spending proposals forecast by Reagan to build up U. S. forces. "We concur with the spending levels and the need for them," says one military electronics marketing manager in the Capital, "but I don't know anyone who believes inflation will drop to 5.5% in four years just as heavy production orders will have to be placed for weapons now in development. If anything, these outlays may spur inflation, since they may more than offset any cuts in social programs."

Why are opponents smiling?

Indeed, that sentiment is widespread. To calm the anxieties of weapons suppliers, who suspect that inflation-caused overruns may result in fewer system unit buys and cancellation of others, Weinberger says that he will simply go back to Congress for more money to keep his programs on schedule. "That solution," chuckles one House Appropriations Committee staff member, "is not only naive; it simply won't work. Reagan is committed to cutting inflation, so let him cut it."

While many Democrats in both the House and Senate are critical of some of Reagan's goals and Stockman's budget-cutting fervor, none of them will admit to expecting the steady downward revision of the Pentagon's inflation rate to fail. "Reagan's got the mandate," observed one; "let Stockman have his turn at bat." When asked if a strikeout by Stockman will help Democrats in the 1982 congressional elections, he responded with a smile.

Trapped with Stockman

Consequently, some contractors in the military electronics and aerospace industries see themselves walking into a trap created by the OMB mandate. If forecast unit purchases are cut back because of understated inflation rates, notes one industry official, "we'll be back on the old procurement roller coaster again. That is sure to spur inflation, not cut it, because production efficiency will disappear. We can't afford it and neither can the country."

Such views came through clearly in conversations during the Electronic Industries Association's mid-April symposium on military spending. Stockman's plan for quickly bringing weapons system inflation under control sounded a sour note over the prospects of the Reagan military buildup. The fact that Stockman may be trapped by his own economic misjudgment and thereby destroyed offers no satisfaction to electronics suppliers who suspect that they may find themselves caught, too. **-Ray Connolly**

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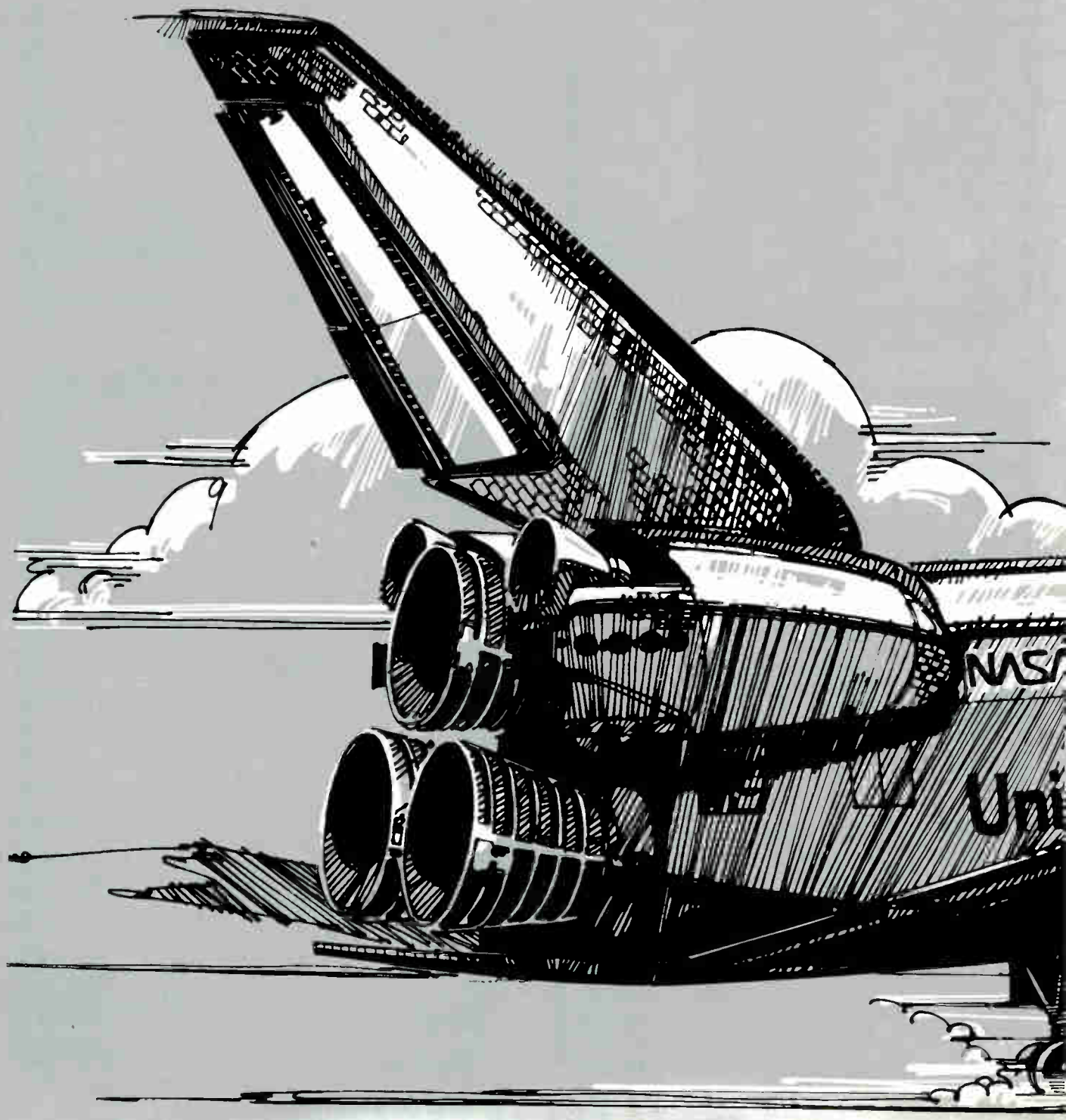

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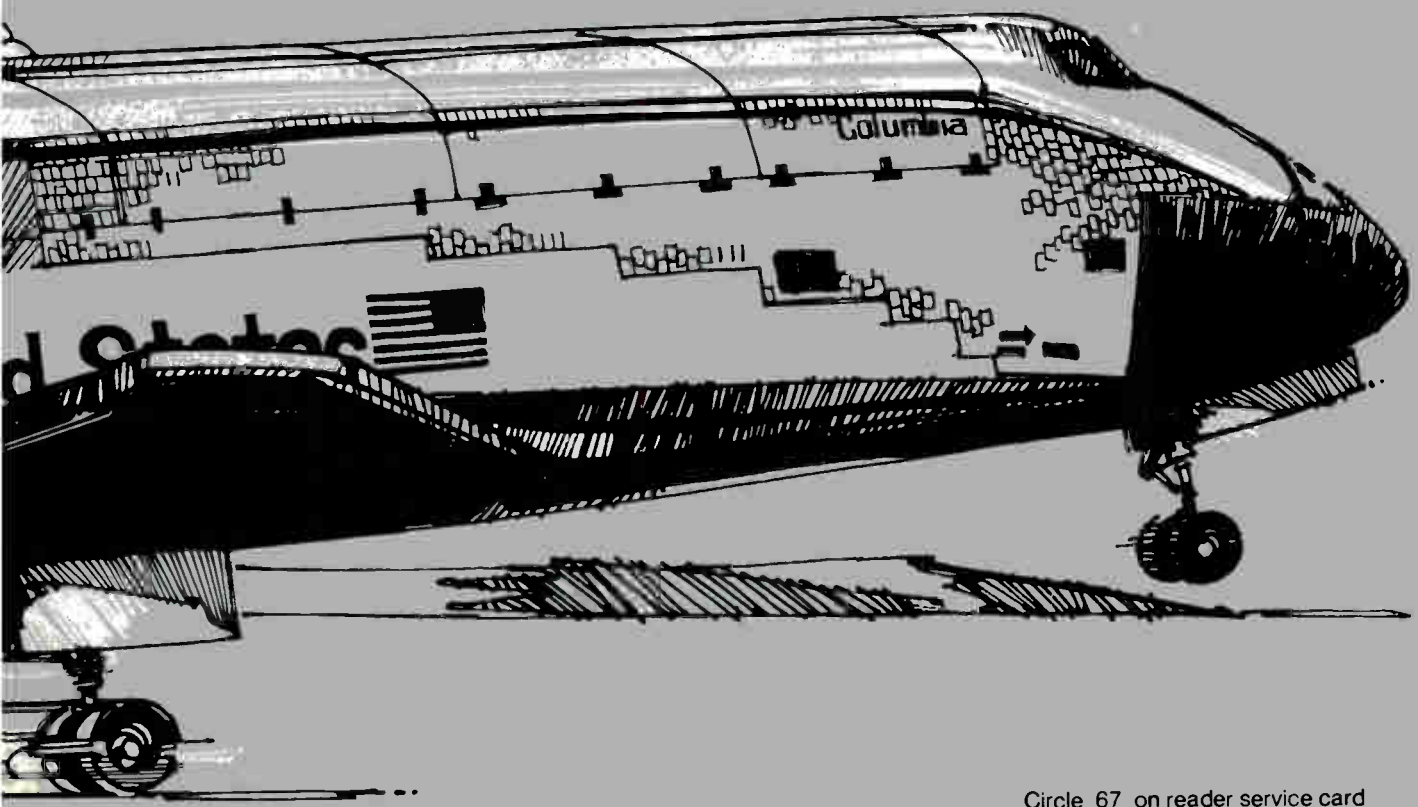


Circle 67 on reader service card

Excellence to Surp

The concepts responsible for the developn
to startle the electron
Two exciting new innovations to boost the

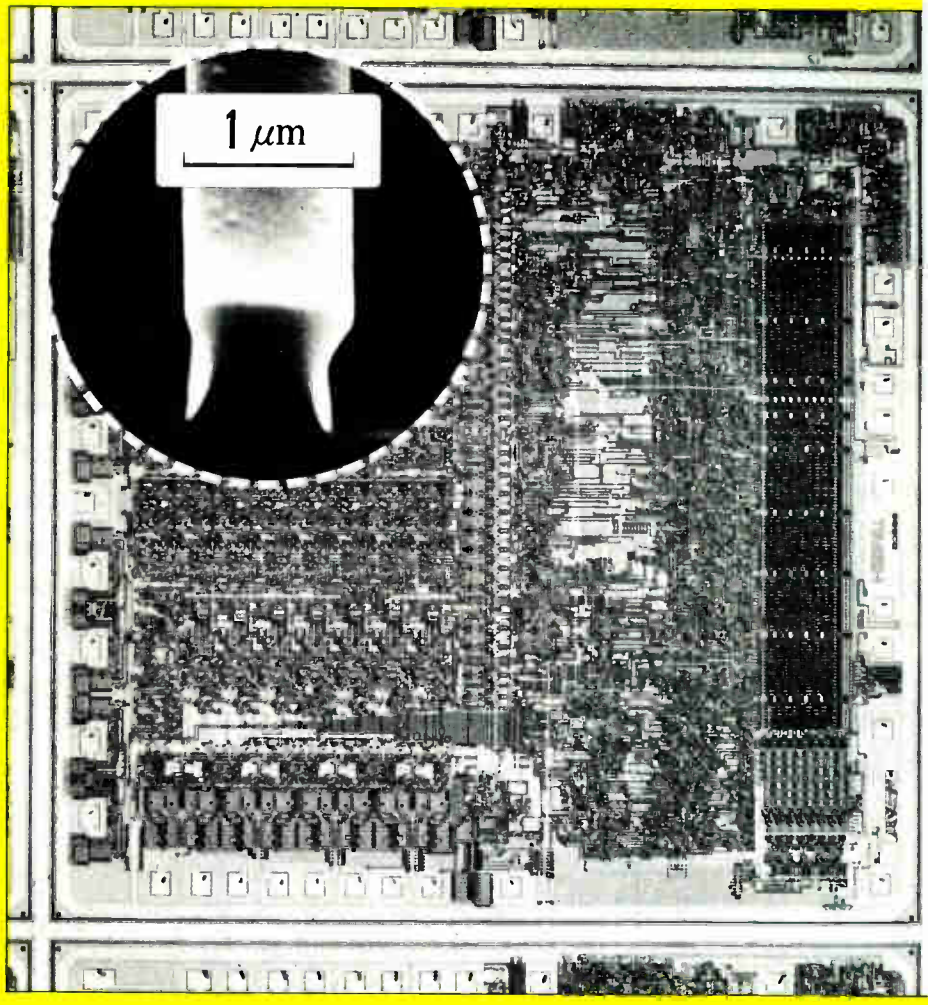
NEW

DEEP-UV RESIST FOR MICRO LITHOGRAPHY

RAYCAST RD-2000N

High resolution of 1μm attained. Our new Deep-UV resist allows mass production of VLSI with the dry etching process.

Photo etching process is the basic technique for IC chip production. As the scale of semiconductor integration expands, photo etching techniques progress, and with it, the precision required on resist materials increases. In this new age of VLSI's, containing brain cells with memory levels in the hundred thousands, conventional UV resist materials are no longer capable of fulfilling the demands. Today's applications require resists with ever increased levels of resolution. Our new negative type RAYCAST RD-2000N is the definitive answer to these needs.



1 **Superior Dry-Etching Resistant Characteristics**
Relative Value of Weight Reduction
RD-2000N/PMMA=28/100

2 **High Resolution, High Sensitivity Resist**
An excellent resolution of 1μm even with a 1:1 projection printer with only a 20 to 40 second exposure time.

3 **High Softening Point**
Durable up to 150°C. Non-deformity of the resist at post-bake.

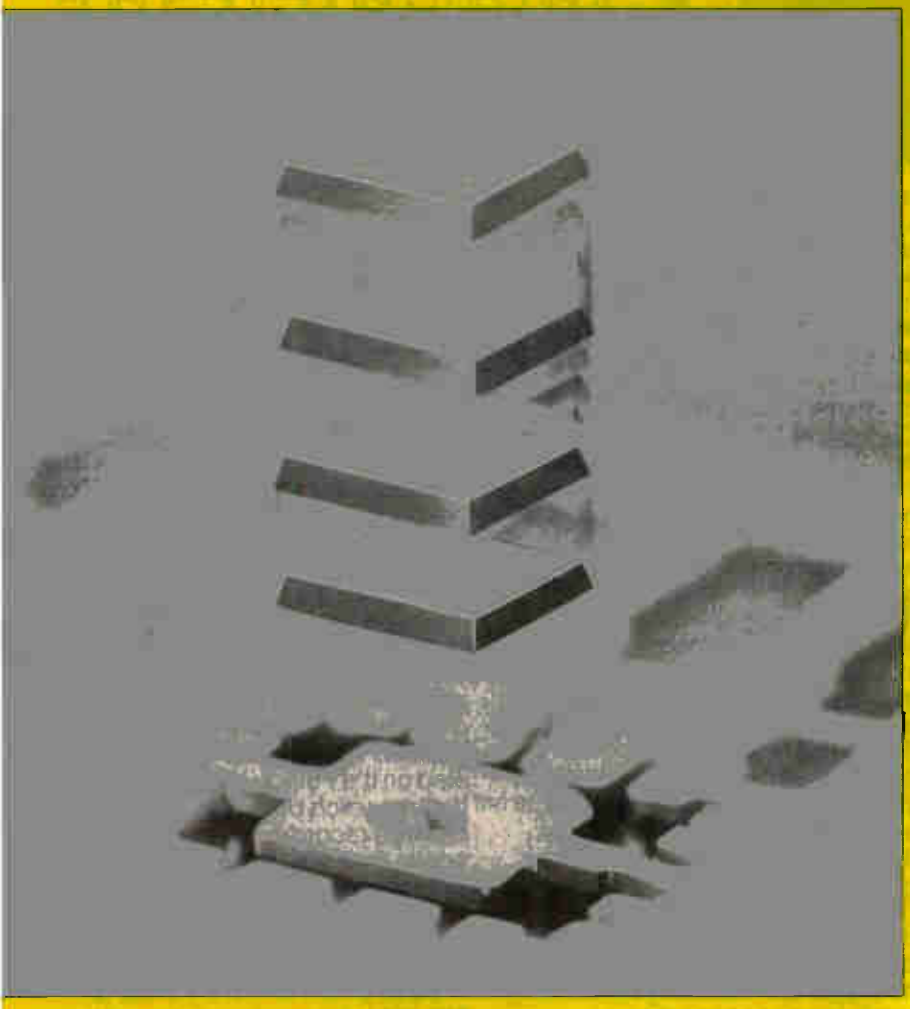
ass Even the PIQ!

nt of the PIQ produce major breakthroughs
cs world once again.
evels of semiconductor technology.

NEW

DIE BONDING PASTE FOR SEMICONDUCTORS

EPINAL 4000

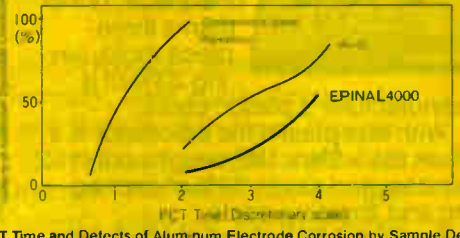


A high purity paste with superb electrode anti-corrosive effect, surpassing even Au-Si eutectic bonding, and at lower costs.

Die bonding paste is used for the assembling of semiconductors. Since semiconductors must be highly reliable, the paste used must a so possess high quality characteristics. In seeking the highest quality possible, Hitachi Chemical, with the backing of the technological experience of the Hitachi Group, has succeeded in introducing another major breakthrough. That newest development is EPINAL 4000, a one-component type silver-filled epoxy resin which not only assures high reliability but considerable cost reduction.

1 **Excellent Resistance Against Humid Conditions**
Superior moisture resistance. Combined use with an epoxy encapsulant offers anti-corrosive effects on electrodes exceeding even an Au-Si eutectic bonding.

2 **High Purity**
The content of impurities and impurity ions is kept at a minimum.



PCT Time and Defects of Alum num Electrode Corrosion by Sample Device

HITACHI
Hitachi Chemical Co.,Ltd.

HEAD OFFICE No 1-1 2-chome, Nish shinjuku Shinjuku-ku, Tokyo 160 Japan. Tel: Tokyo (346) 3111 Telex: J24379 (KASEI HIT) Cable: KASEI HITACHI TOKYO
U.S.A. Hitachi Chemical Company America, Ltd 437 Madison Avenue, New York, N.Y. 10022, U.S.A. Tel: (212) 838-4804 Telex (23) 223128 HCH UR

Circle 69 on reader service card

International newsletter

Blue LEDs on verge of mass production

Blue light-emitting diodes with a 2-mcd brightness when operated at 10 mA will be offered in sample quantities this autumn by Matsushita Electronics Corp. The firm says it has not yet decided when to start mass-producing them or what to charge for them, though the cost of their sapphire substrate will probably make them **initially much more expensive than diodes of other colors.** The new devices, which use gallium nitride and zinc-doped epitaxial layers, have a peak output at 490 nm. For blue LEDs, their power efficiency of 0.03% is quite high and their 7.5-v terminal voltage is quite low.

Bus interface for military avionics to come as chips or hybrid

A two-package, three-chip data transmitter-receiver that interfaces avionics subsystems to the MIL-1553 data bus—the standard for all future U. S. and UK military aircraft—is now being supplied in sample form by Britain's Micro Circuit Engineering Ltd., a newly spun-off subsidiary of Smiths Industries Ltd. The Cheltenham, Glos., company is also negotiating with the Components Group, based in Paignton, England, and Data Devices Corp., New York, **to make the high-density silicon-gate complementary-MOS chips in a redundant hybrid version.**

Sony shows complete 1,125-line TV system

Japan's Sony Corp. has become the first firm to demonstrate a complete 1,125-line high-definition television system, including a 32-in.-diagonal monitor and a 100-in.-diagonal projection display. The image is said to have the same definition as that of a 35-mm movie film, enabling **electronic cinematography to produce the original for movie films as well as for TV and cable TV signals.** Masahiko Morizono, a senior managing director, says that his company will start production as soon as broadcast standards become official. Matsushita, a pioneer in high-definition systems [*Electronics*, Nov. 22, 1973, p. 9E], will show a similar system at its May 31–June 3 technical fair in Chicago.

French data terminal to sell for around $100

Alcatel-Electronique is immediately launching production of half a million small, interactive data terminals. The Paris company, part of the huge Compagnie Générale d'Electricité, has been chosen by the French postal and telecommunications authority to supply **the first 300,000 dumb terminals for the agency's ambitious electronic directory telephone project.** Alcatel chairman and chief executive Georges Pébereau figures the company will be producing 1.5 million terminals a year by the end of 1983. Alcatel is now offering the terminals at about $200 each in bulk, but hopes to nearly halve that price as production steps up.

U. S. firm angling for UK torpedo contract

Like its own Adcap torpedo that stalks its prey and then kicks into top speed for the kill, Gould Inc.'s Gould Ocean Systems division of Cleveland, Ohio, is angling to land the contract for Britain's replacement heavyweight torpedo program, said to be worth $1 billion over 10 years. The bait is offset manufacturing contracts with UK companies said to be equal in cost to the UK program and including some production to meet a U. S. requirement. **Also competing is Marconi Space & Defense Systems Ltd.,** whose Stingray lightweight torpedo is entering production and which now wants to develop a heavyweight and thus challenge the domination of the world market by Gould's Mark 48.

GET FAST RELIEF FOR 12-BIT ADC HEADACHES.

FOR PRICE, SPEED AND PERFORMANCE, OUR AD578 IS THREE WAYS BETTER.

We've just solved your fast 12-bit ADC problem. Until now, you had to trade off price, speed or performance to get a 12-bit analog to digital converter you could use. With our new AD578, you can get all three without sacrificing a thing. Available in three speeds from 3μs to 6μs, our AD578 costs 25-40% less than any 12-bit ADC in the under 10μs range. For performance, you get short cycle capability, positive true parallel and serial data outputs, and a precision +10V reference for external applications.

Our AD578 comes "complete," so you can perform full-accuracy conversions without any external components.

And for your high speed applications requiring 10-bit accuracy, we offer our ultra-fast 1.8μs AD579.

To relieve your 10- and 12-bit ADC headaches fast, contact Doug Grant or Don Travers at (617) 935-5565, or write Analog Devices, Inc., P.O. Box 280, Norwood, MA 02062.

AND IT'S "COMPLETE."

With prices starting as low as $85 (in 100's), you may think we left something out. Think again!

OUR AD578. TAKE TWO AND CALL US IN THE MORNING!

ANALOG DEVICES

WAY OUT IN FRONT.

Analog Devices, Inc., Box 280, Norwood, MA 02062; East Coast: (617) 329-4700; Midwest: (312) 653-5000. West Coast: (714) 842-1717; Texas: (214) 231-5094; Belgium: 031/37 48 03; Denmark: (02) 84 58 00, England: 01/94 10 46 6; France: 687-3411; Germany: 089/53 03 19; Japan: 03/26 36 82 6; Netherlands: 076/879 251, Switzerland: 022/315760; and representatives around the world.

Circle 73 on reader service card

TEK 7D02 LOGIC ANALYZER

The logic analyzer for

The solution to your problems.
Now. A logic analyzer made expressly for microprocessor-based design.

The Tektronix 7D02.
An instrument that provides solutions instead of compounding problems. That cuts design time and improves cost-effectiveness.

Look at just a few examples:

Design Problem: Adapting your logic analyzer to work with a specific processor.

7D02 Solution: Just plug the μP-specific 7D02 probe directly into the prototype microprocessor socket and press START. Acquired data is immediately disassembled and displayed in your processor's own mnemonics.

Design Problem: Sorting error-related data from other program flow.

7D02 Solution: Programmable data and clock qualification filters the data and stores only information pertinent to the problem.

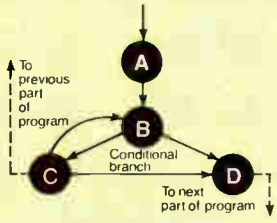
Design Problem: Relating hardware activity to program flow.

7D02 Solution: State and timing sections are included in a single logic analyzer, with each section able to trigger or qualify data acquisition by the other.

Design Problem: Monitoring I/O activity on the system bus.

7D02 Solution: Acquire both synchronous and asynchronous data through interactive triggering to examine both slides of an I/O transaction.

Design Problem: Tracking program flow through non-sequential algorithms with conditional branches to pinpoint an error.



7D02 Solution: The 7D02 can monitor multiple events and conditionally branch as part of its trigger or data qualification sequence. As a result, it can detect an error condition anywhere in your program flow.

 960

microprocessor–based design.

7D02. The solution.
No matter how you look at it, the 7D02 has what you need for faster, more efficient microprocessor-based design.

A series of probe modules adapt the 7D02 to major 8-bit and 16-bit processors, both now and in the future. There's also a general purpose probe for use with microprocessors not specifically supported today. It may also be used like a conventional logic analyzer for troubleshooting the peripheral elements of the system you're designing.

You can have up to 52 channels of synchronous data acquisition, of which 8 channels can be used to acquire asynchronous data at speeds to 50 MHz for timing analysis.

Data acquisition resources include four word recognizers and two interactive counters that can be reset on the fly. Also several modes of both data and clock qualification.

You get two levels of glitch triggering with a resolution of 5 ns, and a separate glitch memory. Plus separate acquisition and reference memories for quick data comparisons.

And all the 7D02's resources are quickly and clearly configurable through a simple user language. One that lets you trigger right on a problem instead of around it. Minimum programming input yields maximum insight into your prototype's software and hardware activity.

For more information on the 7D02, contact your Tek Sales Engineer or call us toll-free. 1-800-547-6711.

You'll wonder how you ever designed without it.

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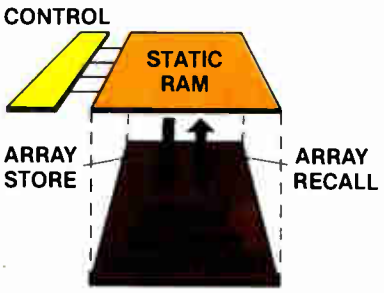
XICOR LAUNCHES

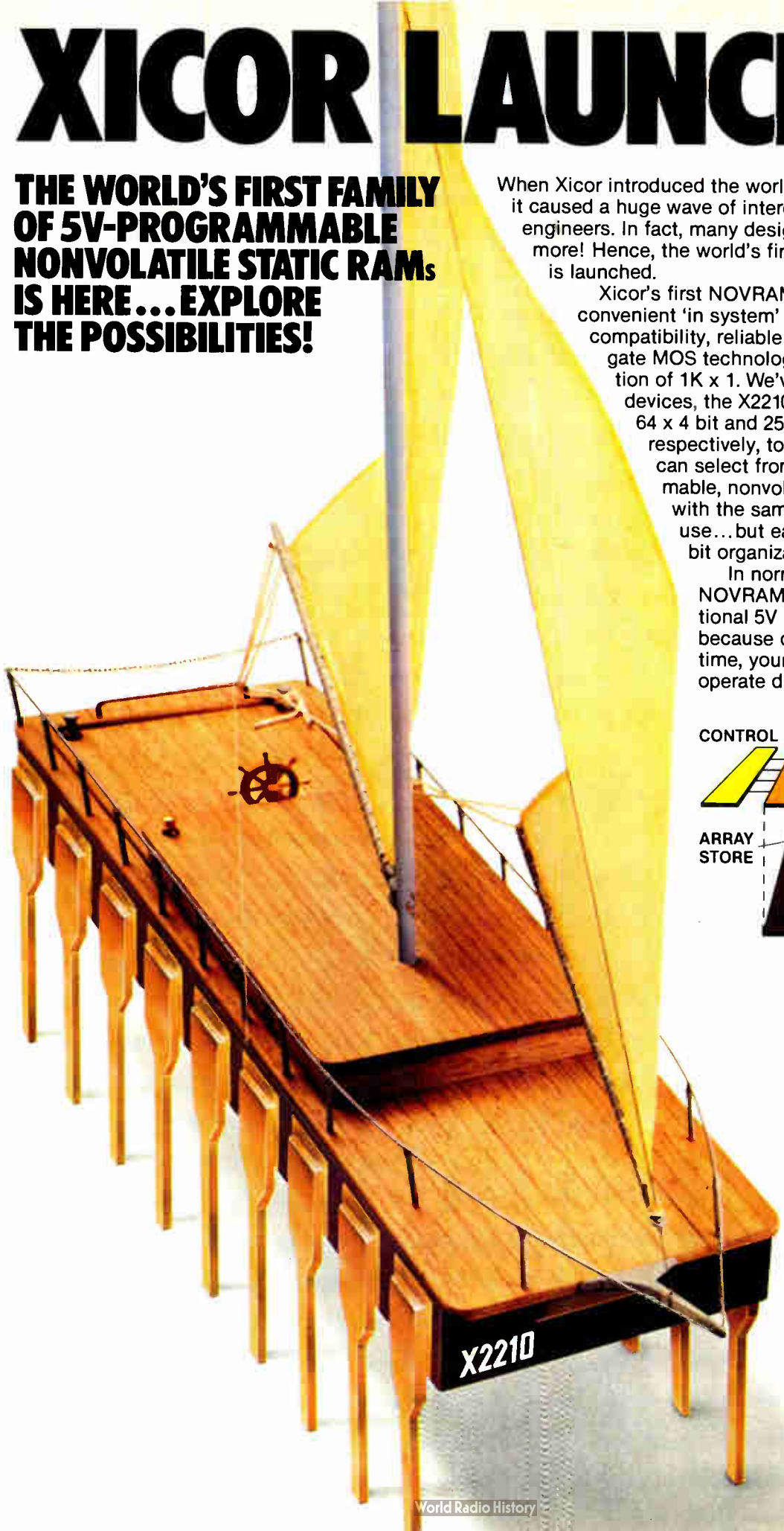
THE WORLD'S FIRST FAMILY OF 5V-PROGRAMMABLE NONVOLATILE STATIC RAMs IS HERE...EXPLORE THE POSSIBILITIES!

When Xicor introduced the world's first NOVRAM it caused a huge wave of interest among design engineers. In fact, many designers asked for more! Hence, the world's first family of NOVRAMs is launched.

Xicor's first NOVRAM, the X2201, offered convenient 'in system' programmability, TTL compatibility, reliable n-channel, floating gate MOS technology and a bit organization of 1K x 1. We've now added two new devices, the X2210 and the X2212, with 64 x 4 bit and 256 x 4 bit organizations respectively, to the series. Now you can select from three 5V-programmable, nonvolatile static RAMs...all with the same features, all easy to use...but each offering a different bit organization.

In normal mode, all three NOVRAMs function as conventional 5V static RAMs. And because of their 300ns cycle time, your microprocessor can operate directly with these

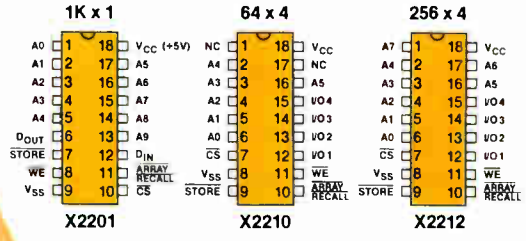




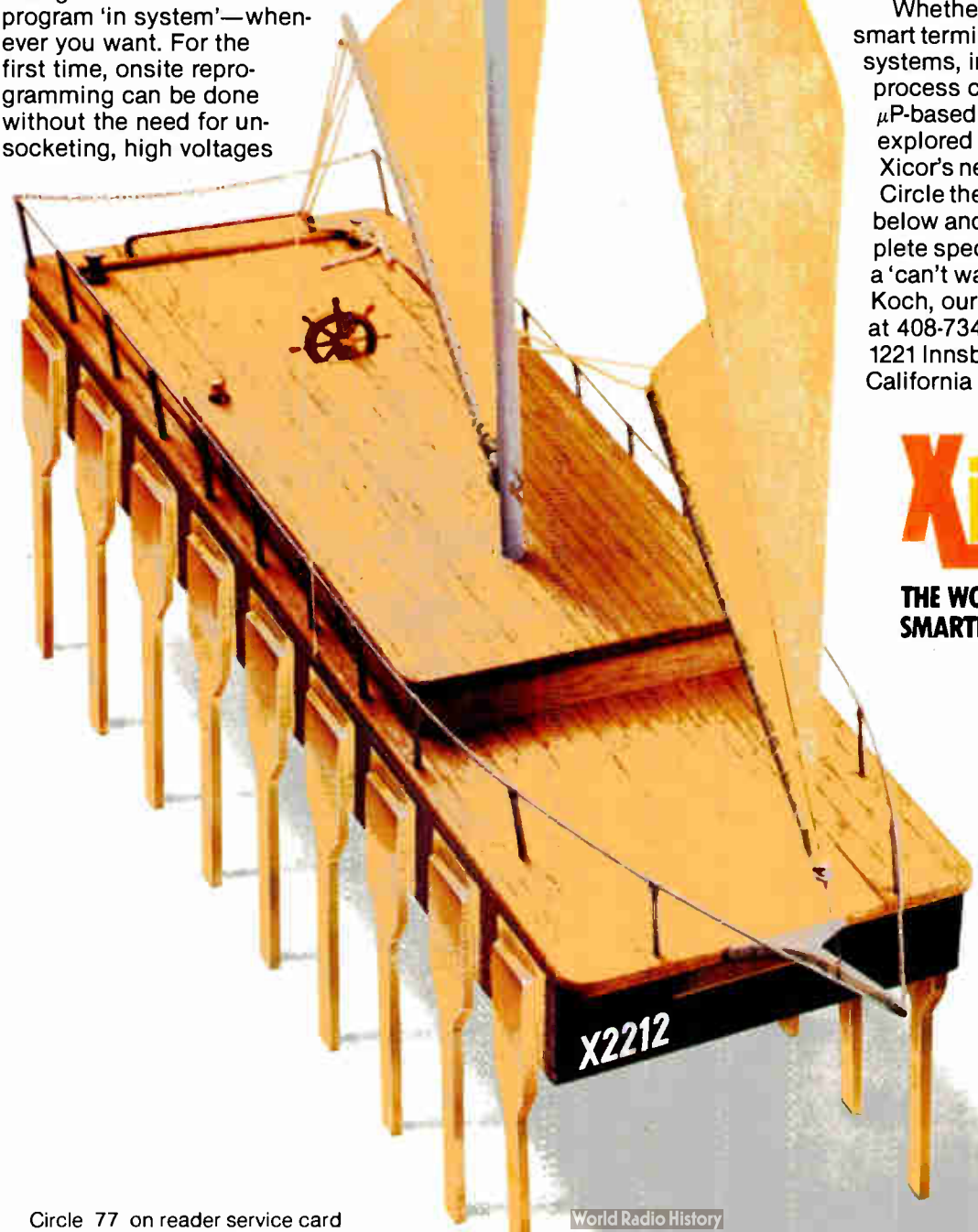
2 NEW NOVRAMs

NOVRAMs at full speed. However, a single TTL signal (STORE) is all it takes to transfer, in parallel, all RAM bits to a unique on-chip shadow memory (E^2PROM). There, the data can be stored indefinitely—*and without power.* So if your power source fails, your data will be kept safe, and you can bring it back into RAM whenever you desire with another TTL signal (RECALL). It's as simple as that.

And there's more! Since it requires no more than 5 volts to perform all functions, a NOVRAM will also allow you to upgrade system firmware—from a single word to an entire program 'in system'—whenever you want. For the first time, onsite reprogramming can be done without the need for unsocketing, high voltages or UV light sources. This means you can reduce your system costs, and at the same time, increase its efficiency by eliminating the use of batteries, extra power supplies, counters or dip switches. And still get full speed operation.



Whether you're designing smart terminals, remote metering systems, instruments, avionics, process controls or any other μP-based system, it's time you explored the possibilities of Xicor's new family of NOVRAMs. Circle the reader service number below and we'll send you complete specifications. If you have a 'can't wait' situation call Bud Koch, our Marketing Manager at 408-734-3041. Xicor, Inc., 1221 Innsbruck Drive, Sunnyvale, California 94086.



Xicor

THE WORLD'S SMARTEST MEMORIES

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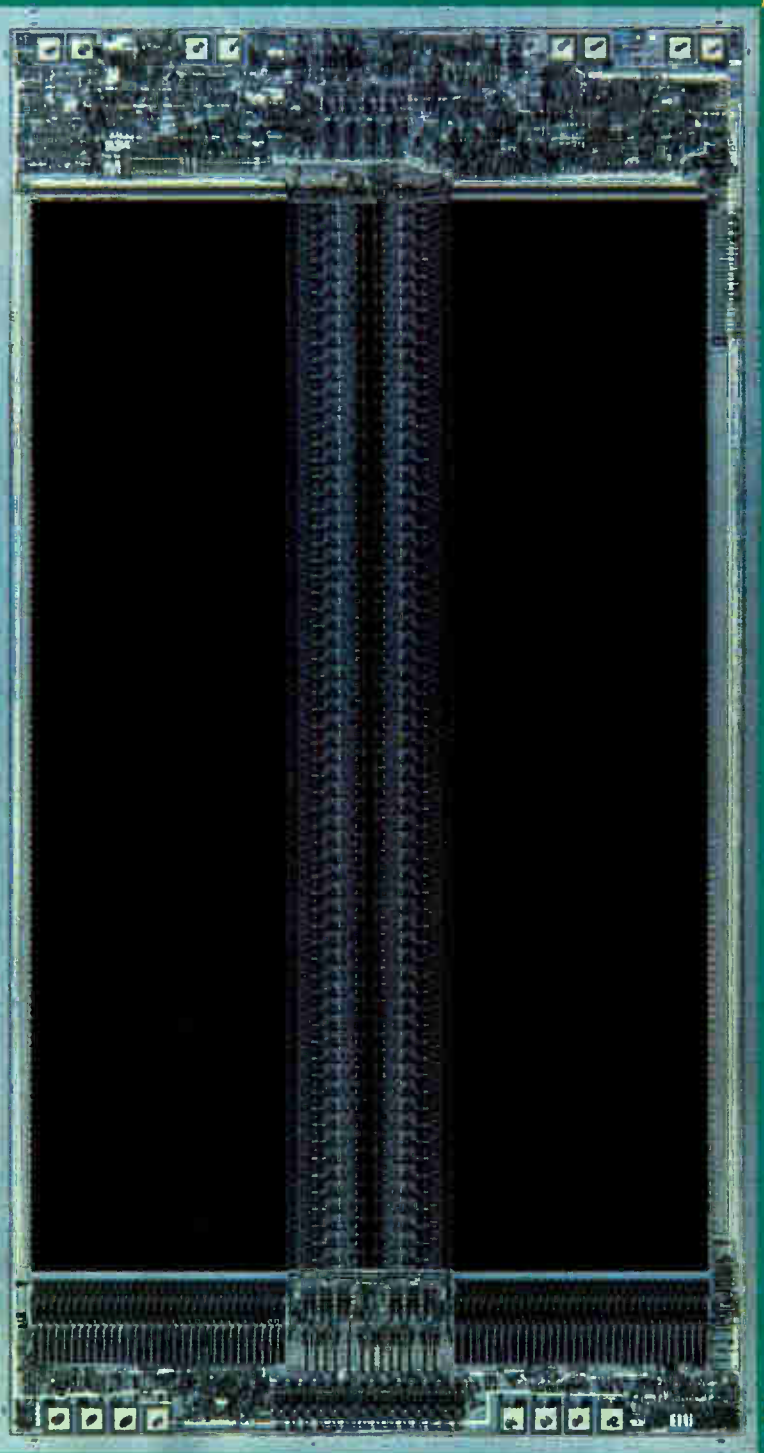
DESIGN

PROCESSING



MATERIALS

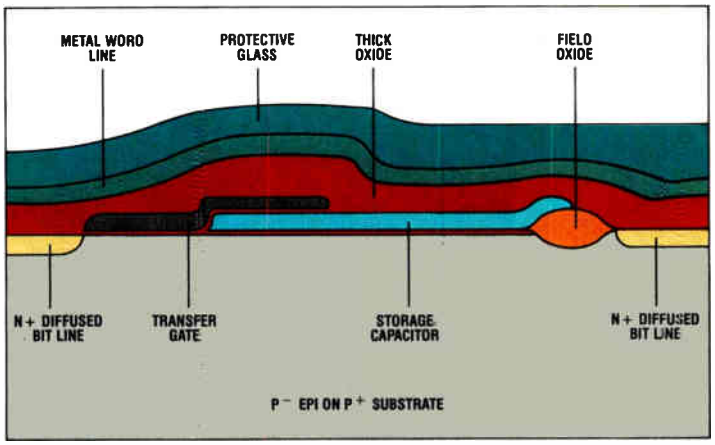
TESTING

from design to test
and everything in between...
a commitment to dynamic RAM
state-of-the-art...

TMS4164 from Texas Instruments. Advancing the systems approach to 64K technology.

Using diverse resources and production-proven experience, TI developed a 64K dynamic RAM supported by a broad base of technical innovations — at all levels.

There's a systems approach to the advancement of 64K technology that assures our customers that TMS4164 is superior in design — and equally superior in the use of materials, processing and testing techniques.



Fabricating the TMS4164 cell on epitaxial silicon virtually eliminates substrate noise.

Because improvements in one technology drive improvements in all the others, it's the shared learning experience between all TI semiconductor technologies that has brought TMS4164 to the leading edge of the state-of-the-art — and beyond.

Design

Our unique grounded substrate design totally eliminates the need for a substrate bias generator — and its less effective method of establishing a negative voltage to control injected electrons. Enhanced noise immunity, greater tolerance to negative undershoot, wider operating margins and firmer transistor parameters are just a few of the breakthroughs TI has achieved with the grounded substrate technology.

Of course, there's much more to the design story, too — like our advanced 256-cycle, 4-ms refresh architecture, low-power dissipation and fast cycle time.

Materials

Innovations are also incorporated into TI's use of materials. By depositing a thin, closely controlled layer of highly resistive P^- silicon onto a low resistivity P^+ substrate, we have virtually eliminated peripheral noise in the TMS4164.

The low resistivity substrate damps out capacitive coupling typically caused by clock bus line activation. Other benefits of this epitaxial (epi) layer are reduced algorithm sensitivity and immunity to address voltage bump. And, epi sets the stage for the future — the not-too-distant future of 256K devices — and the challenge of VLSI.

Processing

Processing advances in TI's TMS4164 mark major technology turns in high-performance DRAM production. TI has unequalled experience in the development of key equipment, like our own dry plasma reactors, and use of advanced low-temperature processing techniques. Our processing capability means device consistency, uniformity and reliability. And satisfied customers.

Testing

For consistently superior system performance, every 64K DRAM is tested well beyond device specification. TI's meticulous attention to equipment accuracy and exhaustive algorithm testing result in high incoming quality. And, our own Test Data Management (TDM) system uses TI's 990 minicomputer to statistically track transistor parameters and other performance characteristics for constant process improvement.

Thanks to this kind of real-time process feedback, TI can assure every TMS4164 user of a more uniform product — and, built-in quality.

For the inside story on TI's TMS4164 64K dynamic RAM, and our leading edge systems approach, call your nearest TI field sales office, or write to Texas Instruments Incorporated, P.O. Box 1443, M/S 6955, Houston, Texas 77001.

TEXAS INSTRUMENTS
INCORPORATED

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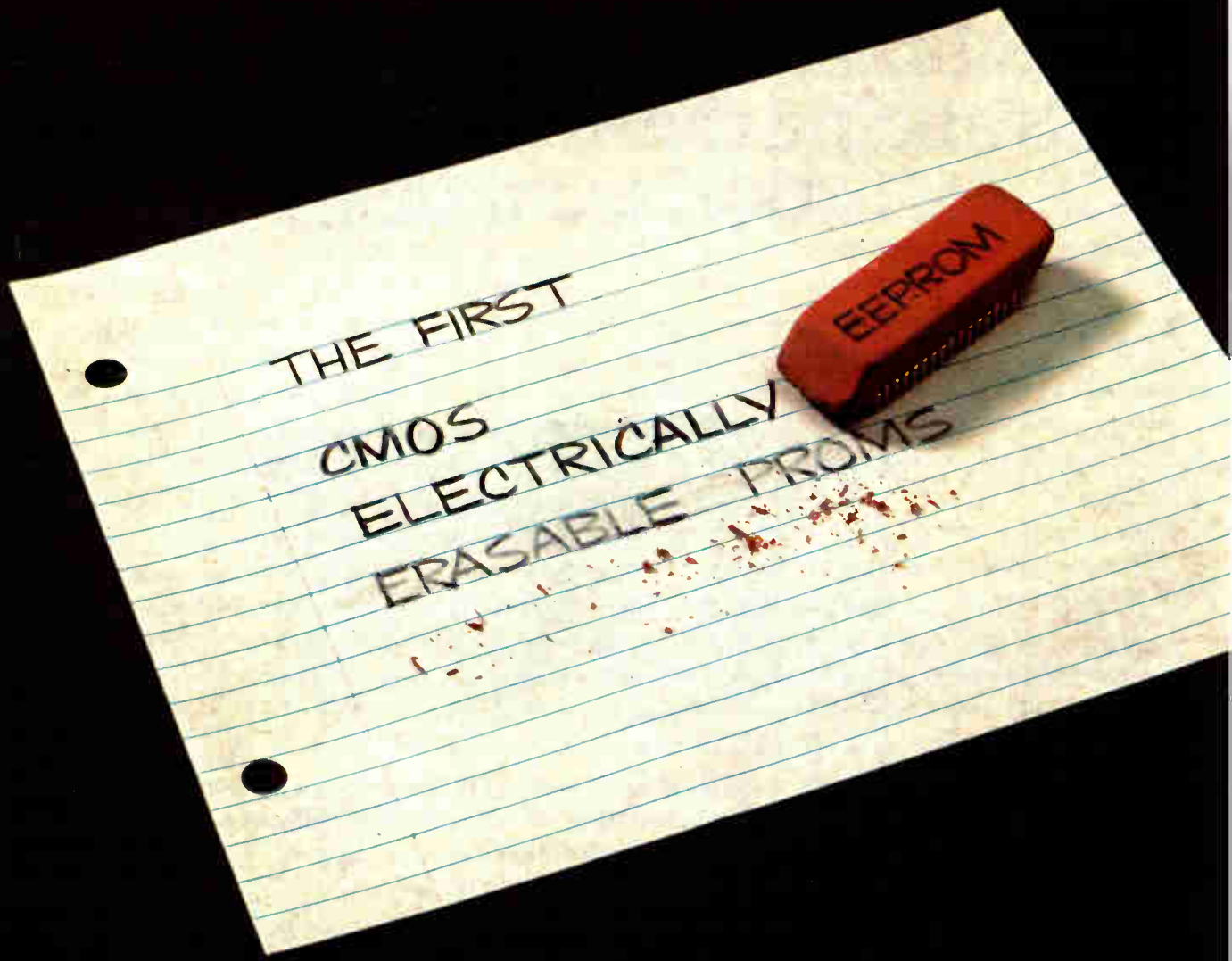

Introducing a Breakthrough in CMOS Technology

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The HNVM 3008 EEPROM Offers the Advantages of:

- Non-Volatile Data Retention (10 years without power)
- High Number of Reprogramming Cycles (100,000 times)
- Fast Electrical Programming
- Low Power CMOS Performance

The HNVM 3008 is an 8,192 bit Electrically Erasable and Electrically Programmable Read Only Memory (EEPROM) organized in a 1024x8 configuration. It has the unique combination of low power. good access time. multiple erase and reprogram cycles and long retention time.

In addition, it operates in a wide temperature range and erases electrically in a very short time (no waiting for factory mask turnaround or ultra-violet light erasure).

The HNVM 3008 operates as a regular ROM with the power supply at 5V. Erasing and programming is accomplished in or out of the circuit when the input supply voltage is 17 volts. This characteristic allows the EEPROM to replace ROM or EPROM and provides non-volatile data updating and retention for a multitude of new applications.

Also available now is the HNVM 3004, a 4,096 bit EEPROM (512x8) for those requiring smaller devices. These exciting new products are part of a planned family of high technology non-volatile devices.

For the HNVM 3008 or HNVM 3004 Data Sheet call or write: Hughes Solid State Products.

Size:	8,192 Bits
Type:	ELECTRICALLY ERASABLE Electrically Programmable
Voltages:	Read... +5V only Erase, Program... +17V only
Power Dissipation:	5mW Operating −0.5μW Standby
Operating Range:	−55°C to +125°C
Access Time:	500 nsec
Endurance (No. of Erase/Reprogram Cycles):	100,000
Data Retention:	10 years at 100°C
Data Erase Time:	100 μsec
Entire ROM Program Time:	0.1 sec

Circle 80 on reader service card

French homes to get their own data bus

by Kenneth Dreyfack, Paris bureau

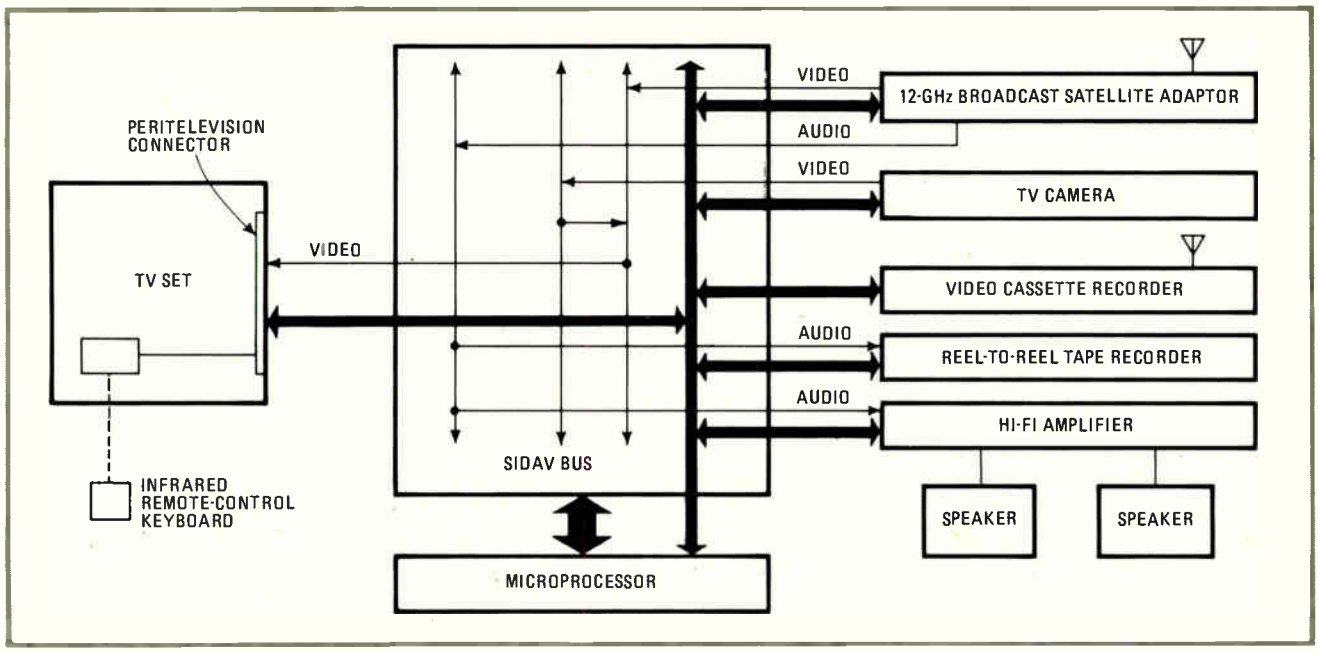
Key pad remotely controls, via a color TV set, a bus linking up to 32 pieces of audio and video gear

Video cassette recorders, teletext decoders, domestic video disks, home computers—what more could French consumers want? A domestic data bus to link them all together, replies French television manufacturer La Radiotechnique. The subsidiary of the Dutch Philips group plans to introduce its first remote-control audiovisual interconnection unit in the fall of next year, and the French Radio and Television Manufacturing Association is expected to adopt it as an industry standard.

"Sidav, a French acronym for dynamic audio video interconnection system, is designed to enable consumers to interconnect as many as 32 pieces of equipment via a single *péritélévision* connector," explains Lucien Bourrasin, chief engineer at La Radiotechnique's television division in the Paris suburb of Suresnes. The connector is a standardized 21-pin device required on every color TV set sold in France and designed to facilitate the addition to it of such devices as video cassette recorders, teletext decoders, or direct-broadcast satellite converters.

Analog and digital. Sidav is basically a switching system, with a data bus to control both analog equipment like high-fidelity audio gear and digital devices like teletext or videotex equipment. For the latter, the bus also handles data transmission—which in the case of the French teletext system, Antiope, can reach a rate of nearly 4 megabits per second [*Electronics*, June 19, 1980, p. 80]. That explains why La Radiotechnique has insisted on a system incorporating three bus operating modes and access priorities in its basic architecture, even though such features will be unnecessary for the relatively simple interconnections the first versions will handle.

The system is controlled through a key pad using infrared remote control. The size of a large pocket calculator, it has four dozen keys divided into six functional sectors. One sector is used to select any piece of



In-house bus. This dynamic audio video interconnection system (Sidav) links audio and digital gear to an infrared remote-control key pad (below left) through a special connector (above left) that is standard in all French color TV sets.

equipment, one controls connection or disconnection, one is reserved for audio or video tape recorder control (fast forward, reverse, and so on), and one controls videotex or teletext instructions (next page, preceding page, and so on). The numeric sector of the device is used to find a particular spot on a magnetic tape or a particular page in a teletext magazine. And the analog control system adjusts volume, contrast, tone, stereo balance, and the like.

While Bourassin expects future TV sets to be capable of receiving the infrared control signals and converting them into the form used on the bus, the first Sidav will be equipped with a separate infrared receiver. In either case, the infrared signal consists of 14 bits—1 each for start and stop, 1 parity bit, 5 bits for the address of any piece of equipment and 6 bits for any command.

Starters. For the simplified first version of the interconnection system, which will control four or five analog devices, this signal is transmitted directly to the 4-bit microprocessor that controls the bus and switching. Since the first version will not handle much data transmission, there is no need for the circuit that on a fully developed system would control modes and priorities.

Information on the bus is organized in segments from 35 to 43 bits long, including 12 bits of address for any device and 8 bits for any instruction. The bus itself consists of a pair of wires—a complementary signal transmitted over the redundant wire cancels out most high-frequency interference.

The actual switching is handled by a simple voltage-switching circuit on the dedicated interconnection board of each device linked into the system. Each circuit board also contains 1 K of read-only memory for storing the user's instructions. When the consumer asks how to operate any particular part of the system, the instructions are transmitted via the bus to a simple character generator circuit—capable of producing eight lines of 20 characters each—and then displayed on the TV screen.

One of the most innovative uses of the Sidav system will be based on the teletext program-flagging scheme now being developed by the French government communications and TV broadcasting laboratory, the Centre Commun d'Etudes de Télévision et de Télécomunications, in Rennes. Known as Epeos, a French acronym for programmable broadcast recording service, the system puts a teletext flag just before the start of each TV program. A viewer equipped with a teletext decoder as well as a video recorder can program his domestic system to automatically record any program.

Automatic alert. By including program-type information in the teletext flag, he or she could even program the system to automatically record, for example, all news programs, without knowing in advance whether any such programs were scheduled. A similar system is being developed in West Germany [*Electronics*, Feb. 10, p. 80].

East Germany

Computer snatches technological lead in Eastern Bloc marketplace

Adding clout to its arsenal of data-processing equipment, East Germany's VEB Kombinat Robotron has come up with a computer system that Western analysts say rates among the most advanced technologically in the Eastern Bloc's lineup of commercial systems. Engineers at Dresden-based Robotron themselves claim their new EC1055M is roughly equivalent to the IBM 370 models 145 to 158. Deliveries will start later this year.

The medium-sized machine—the latest in the Eastern Bloc's ESER series [*Electronics*, Aug. 17, p. 82]—boasts 16-K dynamic random-access memories that help shrink the central processing unit onto only two equipment racks. That is about half the volume of the CPU in the EC1055, the 1055M's predecessor, which has been in production ever since the end of 1979. Moreover, the main memory of the 1055M has twice the capacity of the 1055—4 versus 2 megabytes.

Cooler. Also, the CPU's energy consumption is much reduced—to 4 kilowatts from about 7.4 kW for its predecessor. This reduction, which lowers the need for cooling power, is due to the use of both highly integrated circuits and high-efficiency power supplies operating on line-transformerless principles.

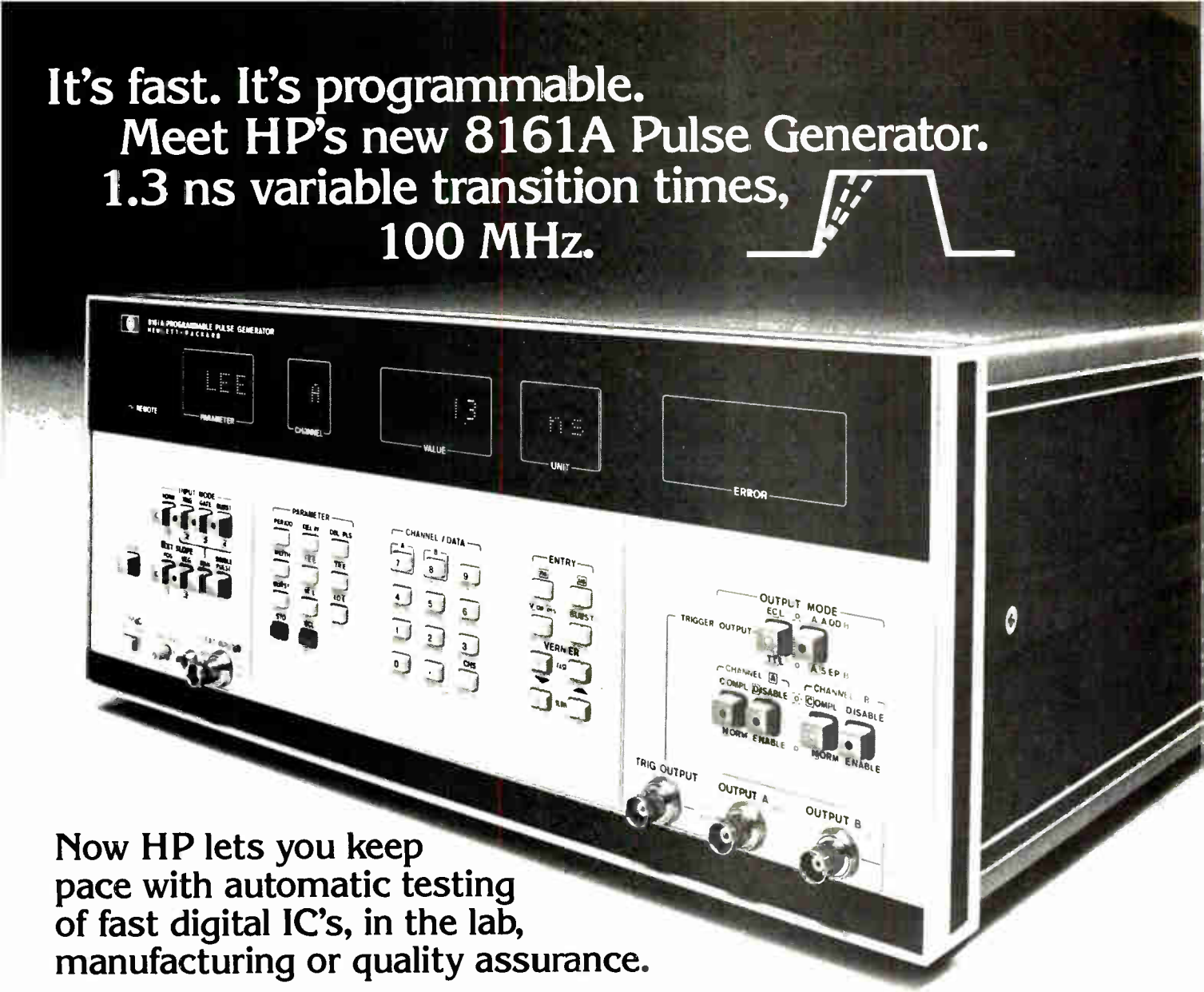
Of note, too, is a new matrix module that carries out floating-decimal-point operations 10 to 50 times faster, plus a new operating system that allows the simulation of several virtual machines and also makes it possible to run dialog and batch-processing modes in parallel.

The CPU, designated EC2655M, has a speed of 450,000 operations per second, and its main memory may hold 1, 2, or 4 megabytes. Although its operating speed is no greater than the predecessor CPU's, the 2655M considerably extends the applications spectrum of the 1055M, which is geared toward industrial and trading organizations, scientific institutions, and administrative centers. Remote data-processing equipment makes the new machine also suitable as a master computer in distributed setups, Robotron says.

64 bits long. The CPU has a microprogram store with a capacity of 8-K microinstructions, each up to 64 bits long, for the hard-coded portion and 1,024 microinstructions, also 64 bits long, for the programmable portion. The cycle time is 380 nanoseconds, and memory loading is via a floppy disk.

An appealing feature for applications involving large amounts of data is the microprogram-controlled matrix module, a high-performance add-on unit for the CPU that can handle such tasks as matrix and vector operations. It comes in especially handy in the fields of statistics, geo-

It's fast. It's programmable. Meet HP's new 8161A Pulse Generator. 1.3 ns variable transition times, 100 MHz.



Now HP lets you keep pace with automatic testing of fast digital IC's, in the lab, manufacturing or quality assurance.

The new Hewlett-Packard 8161A offers a flexible, easy-to-use solution to the problem of testing fast high-technology circuits such as 10K ECL logic and advanced Schottky devices. And, it's the first HP-IB programmable pulse generator with variable transition times down to 1.3 ns, allowing you to evaluate high-speed logic circuits thoroughly.

Features you'll appreciate — now, and in the future. Fast, clean 100 MHz, 5V pulses are just part of the 8161A's story. With 1-2% basic timing accuracy over a wide temperature range plus a one-year recalibration period, the 8161A gives you quality measurements while it saves on maintenance time and expense. Two complementary outputs are standard. And, you can get an optional, fully independent, second output channel that lets you generate complex waveforms in A + B mode. External operating modes and counted burst further enhance the 8161A's flexibility.

A real time saver on the bench. When used as a bench instrument, this new HP Pulse Generator's easy, microprocessor-controlled operation will simplify most test setups. With its high accuracy, no time-consuming 'tweaking-in' is required. Storage of nine complete parameter setups for quick recall simplifies operation. And outstanding repeatability means reliable measurement results.

Ideal for fully automated testing. In an R&D or production system, the versatile new HP 8161A is easily integrated using HP-IB, which allows automated testing of advanced semiconductor devices and system modules. Besides saving time and increasing throughput, the 8161A will eliminate errors associated with manual measurements. You'll get reproducible results over long periods of time without the necessity of constant system monitoring or correction loops.

Fully detailed information — yours for the asking. For comprehensive technical data and application note, write: Hewlett-Packard, 1820 Embarcadero Road, Palo Alto, CA 94303. Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500. Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.

081 7

HP-IB: Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a measurement system.

HEWLETT PACKARD

Circle 83 on reader service card

No antitrust rules in East Germany

Headquartered in Dresden, VEB Kombinat Robotron is an industrial combine that handles virtually all of East Germany's data-processing activities and manufactures everything from electric typewriters and office machines to large computer systems and industrial robots in various production facilities around the country. Of its 70,000 employees, roughly 12% are engaged in research and development and another 16% are involved in worldwide sales and marketing.

What may come as a surprise is Robotron's big export volume. About 70%, or roughly $1 billion, of its total annual production goes abroad. The bulk of those sales is to other Socialist countries, with the Soviet Union ("an insatiable market," as Robotron officials like to point out) taking the lion's share. Capitalist countries account for 10% or so of total exports.

Most of the chips the combine uses are said to be of East German origin, but a substantial share, one official says, comes from the Soviet Union. The biggest single system being exported by Robotron to date is the EC1055, a medium-sized computer of which more than 200 have come off Robotron's production lines during the past year and a half. **-J. G.**

physics, and meteorology. The module boasts a speed of 2.5 million multiplications and 5 million additions simultaneously in 1 second.

The CPU's up-to-4-megabyte main memory has access and cycle times of 740 and 1,140 ns, respectively, and is implemented on just two panels. The 16-K MOS RAMs have one-transistor cells arranged in 128 rows and 128 columns and refresh each cell every 2 milliseconds.

Worth mentioning, too, is the system's operating and service processor, the EC7069M. Also using 16-K RAMs as well as the type U880 8-bit microprocessors [*Electronics*, March 27, 1980, p. 63], the 7069M helps service the system, supervises functions like loading the microprogram store, and diagnoses troubles.

The system's line of peripherals includes removable-disk and magnetic-tape units and cathode-ray-tube monitors. **-John Gosch**

Great Britain

'Watermark' secures magnetic card data

The fear that magnetic-stripe cards may be tampered with may trouble banks, security officers, vending machine operatives and others, but not Emidata, a division of Britain's Thorn-Emi Ltd. The Windsor, Berks., company has a solution to the problem: "watermarked" magnetics, a technique of permanently encoding personalized security data into the magnetic stripe in the course of its manufacture.

Progress. Ever since engineers R. R. Pearce and C. A. Lee came up with the idea at EMI's central research laboratories four years ago, Emidata has been quietly developing the tape manufacturing technology and its associated support systems. Now, it believes its investment is about to pay off. Apart from selling magnetic-stripe cards—its U. S. subsidiary, Malco Plastics Inc., produces 40 million cards a year, or 20% of its output, with watermarked magnetic stripes—the group also plans to sell electronic card-reading modules to manufacturers of vending, identity card, and access control systems.

Last month, for example, at a presentation timed to coincide with the International Fire Security and Safety Exhibition held at Olympia from April 21 to 24, the company launched two new systems for sale to original-equipment manufacturers: one was a high-security identity card system developed initially for a Middle East country, and the other was an access control system, versions of which have just been launched by one German and one British firm.

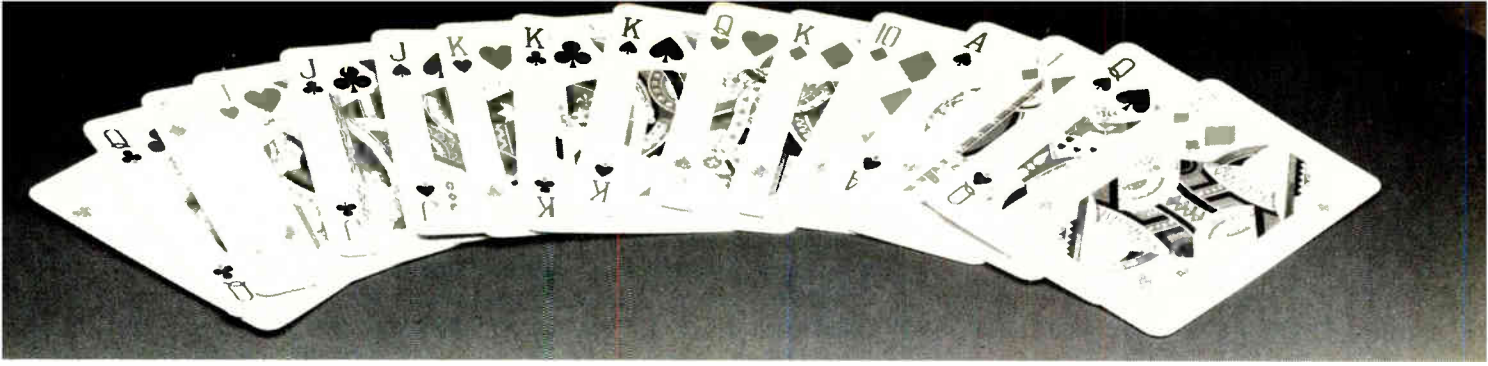
Rival machine-readable data cards are under development: in Mountain View, Calif., for example, the Drexler Technology Corp. start-up is developing an optically read high-density data card, while in France and Italy cards containing semiconductor memory components are also being evaluated. But magnetic-stripe technology is the only approach already in worldwide use.

The manufacture of watermarked tape starts in a similar fashion to conventional tape. A resinous suspension of needle-like gamma ferric oxide particles is coated onto film. Then, when still wet, it is subjected to a constant magnetic field that aligns each miniature magnet to the tape axis. In Emidata's watermarked magnetic process, however, data is frozen into the tape by varying the direction of magnetization: a region oriented at $+45°$ to the tape axis might represent the presence of a digit, while a region oriented at $-45°$ might represent its absence.

Magnetic tapes so manufactured still behave like conventional ones, storing temporary, or soft, data. Permanent, or hard, data can only be read with an additional two-gap read head: the first gap, set at 90° to the tape axis, overwrites any soft data present on that track by applying a steady magnetic field; the second gap, set at 45°, senses a maximum flux change at the boundary of two zones, each magnetized at right angles to each other. Temporary data, too, can be made proof against overwriting by appending check bits to each transaction.

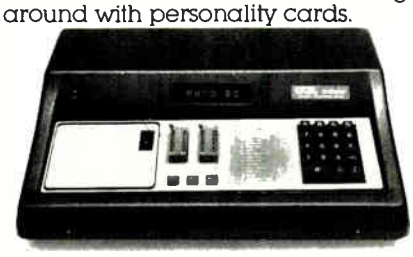
Safe. Watermarked tape, says Emidata, is proof against any of the standard techniques of overwriting or removing magnetic stripes. Conventional tapes have already proved vulnerable, it adds, noting that a workable system for duplicating conventional tapes has been illegally produced in the U. S. for less than $50, and both the Paris Métro and San Francisco's BART have lost out to technology buffs out to crack their systems, neither of which used the watermark approach.

Simon Wyatt, a marketing manager with Emidata, says the company is initally targeting three sectors—identity card, access control,



PERSONALITY CARDS: DEAL YOURSELF OUT.

We wonder if semiconductor programmers wouldn't rather have a 16-position switch right up there on the console for programming any EPROM from 4K to 256K instead of fumbling around with personality cards.



Switch to the switch.

Oh, you can't switch in a new position for every semiconductor that either has been or ever will be made. But, all NMOS EPROMs from 4K to 256K is a BLEEPuva good start, wouldn't you say?

Three peripherals with more thumbwheel switches will handle most of the rest: bipolar PROMs, microprocessors, CMOS EPROMs, EE/EAROMs and logic arrays.

Which not only makes our Citel System 37 easy to use, but cheap in the bargain. Go ahead, ask somebody in Purchasing about the price of personality cards.

And speaking of prices, our Citel System 37 could be the biggest bargain on the semiconductor programming market for one reason.

Because it is a system.

Which brings us to something other equipment makers should warn you about, but don't: Anyone considering semiconductor programming gear should never compare individual components. They should always think system.

Switch to the system.

Thinking systems instead of components is hardly a new concept. Engineers, purchasing people, even company presidents have been doing it in their private lives for years. They probably all own a camera—with a lense system. And a car—with a stereo system. They wouldn't have bought the ones they did if a system wasn't available. Why then, do you suppose, we tend to think component rather than system in the semiconductor business? Because most equipment manufacturers don't want us comparing systems. When we do, they get embarassed.

Ours vs. Theirs

If you want to see just how embarassing things can get for them, take a look at the bottom line of our system versus their systems in our little chart.

Be smart. Start comparing system to system.

Switch to alphanumerics.

All any other semiconductor programming system (See how easy it is to think system once you get started) can give you is numeric code readouts that still have to be decoded for intelligence. You can't even buy an accessory to make them do anything else.

Well friends; you should know; our Citel System 37 comes right out of the box with intelligent communication through alphanumeric display. It also has parallel and RS232C serial interfaces featuring 12 standard and four custom translation formats.

	CITEL	DATA I/O	Prolog
All software device select	YES	NO	NO
Standard 8K x 8 RAM buffer	YES	NO	NO
Alphanumeric display	YES	NO	NO
Self-test	YES	YES	YES
Remote control	YES	YES	YES
Devices programmed:			
EPROM, 4K to 256K	YES	NO	NO
EEROM/EAROM	YES	NO	NO
Bipolar PROMs, 9 families	YES	YES	YES
Logic Arrays, 4 families	YES	YES	NO
16 EPROM Gang	YES	YES	NO
Pricing:			
EPROM Programmer	$2590	$4025*	$5430**
16 EPROM Gang	$1850	$5425+	n/a
Complete system	$7030	$15000+	$15000+

*System '9 with Mospak
**Model 980 with 4 personality modules, socket adaptors and configurators

Okay, then—switched device selectability eliminating the expense and messiness of personality cards; and alphanumeric display at a system cost of less than one-half the competition. Hey, these Citel people may have something here.

No doubt about it. And this is just the beginning.

Some other manufacturers can't offer you standard 8k byte memory FOB from the factory. Others can't give you optional RAM capacity. We come to you with 8k and an optional 16k or 32k. And since we're on the subject of options, our Citel System 37 offers you optional remote control making it the ideal mate for your development system.

You want more?

How about complete memory editing, automatic power-up self-testing, and an upgrade path for programming future devices?

The fact of the matter is, we've got something for everybody: for hard-nosed production types looking for high through-put and low cost, we have the ideal 16 EPROM Gang for programming anything from 4k to 256k at the flick of a switch. We designed and built our Citel System 37 with development, quality control and manufacturing people in mind.

More, for less.

This may be the first time in the history of advertising it could be claimed that our Citel System 37 does indeed give you more, for less.

But, we won't make that claim.

It's been done so many times before, who'd believe us?

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I'm more than a little skeptical about your claim and your prices. They may be too good to be true. Send me proof your system is all your ad says it is.

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Electronics international

and vending system. Watermarked magnetic-stripe banking cards have already been adopted by National Westminster, one of Britain's five big banks, while Swedish banks have standardized on them. In the U. S. the bulk of Malco's output goes to the banking sector, where magnetic-stripe cards are used as a customer's security pass.

The vending industry takes on a new dimension, Wyatt argues, when the machine is freed of the tasks of accepting high-denomination notes and giving change, and the operator no longer has to empty coinboxes. He says it then becomes immediately possible to sell valuable items through card-operated vending mechanisms. Such a microprocessor-controlled vending module, competitive with coin mechanisms, will be launched this year in the UK only.

The group has also teamed with a Swiss telephone manufacturer to develop a telephone money card purchasable over the counter. Its value appears on a fluorescent display as the card is inserted and decrements automatically as the call progresses. British Telecom is to evaluate the Emidata card in trials alongside a holographic system from Landis & Gyr Ltd. [*Electronics*, May 8, 1980, p. 67]. **-Kevin Smith**

Japan

Very small computer lures users upward

Upward software compatibility with four new larger office computers in the same series and more powerful software differentiate Nippon Electric Co.'s new very small business computer from the personal hobby computers that it resembles at first glance. And while there are other very small business computers in the same price range as the system 20/25 in Japan, it appears to be the only one with upward object-code compatibility.

Furthermore, NEC supplies the 20/25 with a wide variety of utilities and application packages written professionally in Cobol, so that users do not have to resort to commercial programs of unknown quality written in the much less efficient Basic language.

The new line of five computers upgrades an earlier series introduced more than two years ago [*Electronics*, Dec. 7, 1978, p. 71] and fills in a hole at the bottom of the series with a powerful machine for small business. In fact, since the computer runs on Cobol object code, users can easily recompile the source code for any tailor-made programs so as to run them on other computers—even on a mainframe.

Businesslike. The professional features of the NEC system 20/25 and its bigger brothers start with a 14-inch cathode-ray-tube monitor that displays 2,000 characters on 25 lines of 80 characters, each an easy-to-read seven-by-nine-dot matrix. Built into the processor are two 8-inch double-sided double-density floppy disks with 1-megabyte capacity per disk in IBM format.

Professional printers included with the standard system print 136-character-wide lines. The dot matrix printer for users desiring high speed races along at 100 characters per second, while the so-called Spinwriter for correspondence-quality output works at 35 characters per second. NEC says that its printers are three times as reliable as the average personal computer printers, which are generally five-by-seven-dot-matrix types and print lines 80 characters long at a speed of 80 characters per second.

Storage space. In its stand-alone configuration, the system 20/25 has a total memory of 192-K bytes. User space is 48-K bytes, with the remainder reserved for the operating system. The maximum 256-K bytes of memory is installed for on-line communications applications. The memory device used here and throughout the series is the firm's 16-K dynamic random-access memory; moreover, the memory circuits of all the computers are said to permit upgrading with 64-K chips.

The step-up 50/35 features Japanese language output as an option

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and we'll help you discover simple, effective solutions to difficult troubleshooting problems.

FAULT	STIMULUS	RESPONSE	TEST METHOD
Shorted Node	546A Pulser[1]	547A Current Tracer	• Pulse shorted node • Follow current pulses to short
Stuck Data Bus	546A Pulser[1]	547A Current Tracer	• Pulse bus line(s) • Trace current to device holding the bus in a stuck condition
Signal Line Short to Vcc or Ground	546A Pulser	545A Probe Current Tracer	• Pulse and probe test point simultaneously (short to Vcc or Ground cannot be overridden by pulsing) • Pulse test point, and follow current pulses to the short
Vcc to Ground Short	546A Pulser	547A Current Tracer	• Remove power from test circuit • Disconnect electrolytic bypass capacitors • Pulse across Vcc and ground using accessory connectors provided • Trace current to fault
Internally Open IC	546A Pulser[1]	545A Probe	• Pulse device input(s) • Probe output for response
Solder Bridge	546A Pulser[1]	547A Current Tracer	• Pulse suspect line(s) • Trace current pulses to the fault • Light goes out when solder bridge passed
Sequential Logic Fault in Counter or Shift Register	546A Pulser	548A Clip	• Circuit clock de-activated • Use Pulser to enter desired number of pulses • Clip onto counter or shift register and verify devices truth table

1. Use the Pulser to provide stimulus, or use normal circuit signals, whichever is most convenient

HP's IC Troubleshooters make troubleshooting digital circuits fast and less frustrating. Take a look at the chart and see why more than 50,000 people use these simple, rugged, low-cost Hewlett-Packard instruments.

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CURRENT TRACER inductively senses and displays logic current pulses. Finds shorts and stuck nodes with no unsoldering or trace cutting. Uses in-circuit current or pulses from Logic Pulser. $400*

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Electronics international

and can handle about 8,000 different characters—as many as a mainframe or a specialized Japanese word-processing system.

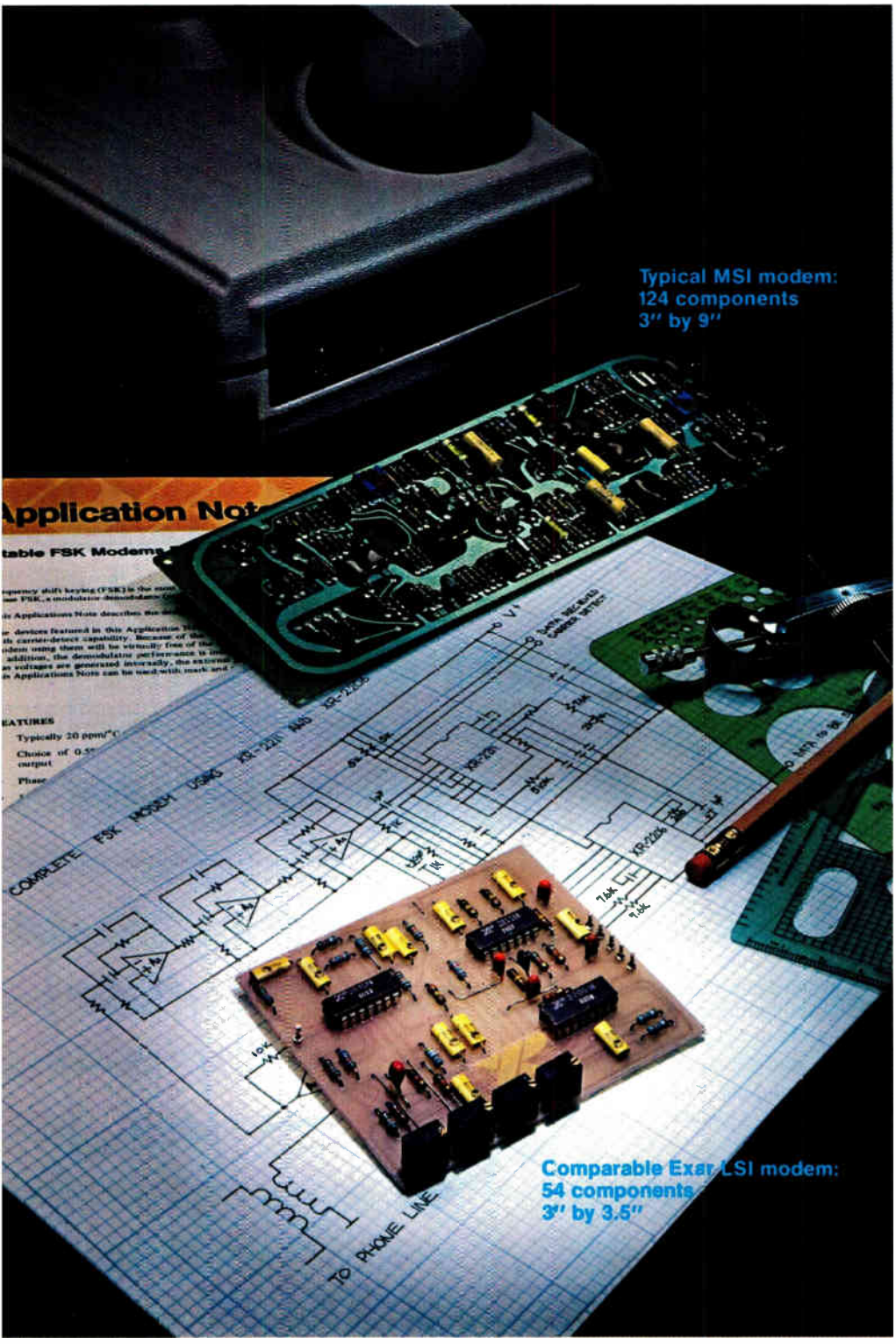
For speed, this computer and the others in the series use an 18-by-18-dot matrix, though the somewhat nicer-looking 24-by-24-dot matrix is available as an option. The keyboard serial printer zips along at 70 kanji characters a second. High-speed kanji printers operating at 60 and 100 lines per minute are also available. Backup memory for either the alphanumeric or Japanese language versions is a 19-megabyte hard disk and up to three 1-megabyte floppies. Although RAM capacity is the same size as in the 20/25, this computer will compile its own Cobol programs.

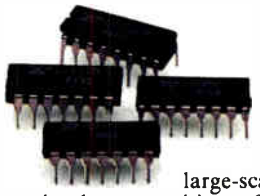
The middle member of the series, the 100/45, is the largest using an n-channel processor. It has a user memory of 512-K bytes and one or two 31-megabyte disks. It can operate with four work stations and four printers concurrently. It is the smallest model that can handle alphanumeric line printers and magnetic tape and also the smallest to have available a cartridge tape unit, the first in Japan, for backing up disks and open-reel tape. The three largest units can also use a higher-level Cobol compiler than the 50/35 does, as well as a Fortran compiler.

Two at the top. System 100/85 has a 4-bit-slice 2901-type central processing unit, implemented in emitter-coupled logic for speed, and 768-K bytes of user memory. It can handle eight work stations and eight printers—up to six of each concurrently. Finally, the system 150/55 has a more advanced version of the ECL CPU and 1,024-K bytes of user memory. It can handle 12 work stations and 12 printers, up to 8 of each concurrently. Both systems come with up to four hard disks of 64-megabyte capacity.

In line with NEC's communications and computing thrust, all systems, even the smallest, have enhanced communications capabilities to implement distributed processing, including built-in facilities for binary synchronous links and NEC's own DINA protocol. **-Charles Cohen**

Let Exar show you how to simplify modem design with LSI circuits.





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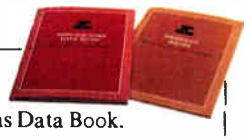
Our LSI circuits help you save 50% or more over MSI and other design techniques, because you reduce your component inventory, your board size, your design time and your labor costs in manufacturing.

Improve modem performance.

Designed specifically for modem applications, Exar LSI circuits have superior frequency stability (typically 20 ppm/°C). Modems built with Exar ICs are virtually free of temperature and voltage-dependent drift problems of other designs.

With Exar LSI circuits, modems can be designed up to 100 kilobaud (using XR-2206 and XR-2211) to over 10 megabaud (using XR-210 or XR-215).

Learn more about LSI modem design.



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Circle 89 on reader service card

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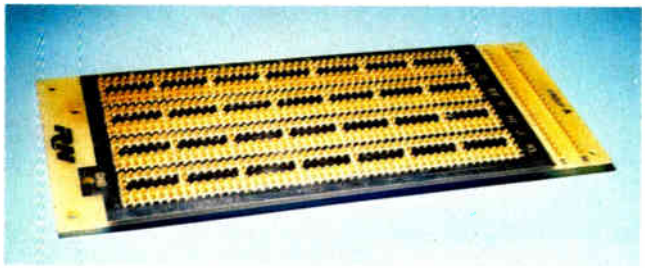
Here is a wiring system that does what wrap/pin does—but does it faster, easier. The wire is simply pushed into the "Quick/Connect" tine which pierces the insulation (IDC) making a gas-tight connection between wire and terminal. "Daisy chain" wiring is accomplished with no break in the wire, no insulation stripping.

You'll never willingly use wrap/pin for boards again. Consider these advantages:

- **High speed wiring simplicity**—You connect just **one** wire per connection. There is **no time-consuming insulation stripping** as needed with wrap/pin.
- **Fast, easy wiring changes**—Repair or modify boards by simply removing the individual wires and quickly re-wiring. Field wiring modifications are simple and fast.
- **Meets highest reliability standards**—Durable four-finger BeCu contacts and fully heat treated IDC tines insure gas-tight performance.
- **High density low profile boards**—The "Q/C" board profile is only 0.235" compared to the 0.703" wrap/pin board. "Quick/Connect" boards go right into production racks.
- **Wiring machines available**—The semi-automatic wiring machines now in use can be readily modified for the "Q/C" system. Also, semi-automatic "Q/C" machines are available.

This is not just a "dream" system. A major electronics firm is currently using the "Quick/Connect" system on a regular basis.



"Quick/Connect" socket boards, ready for wiring, are available in several standard configurations or can be developed to meet customer specifications.

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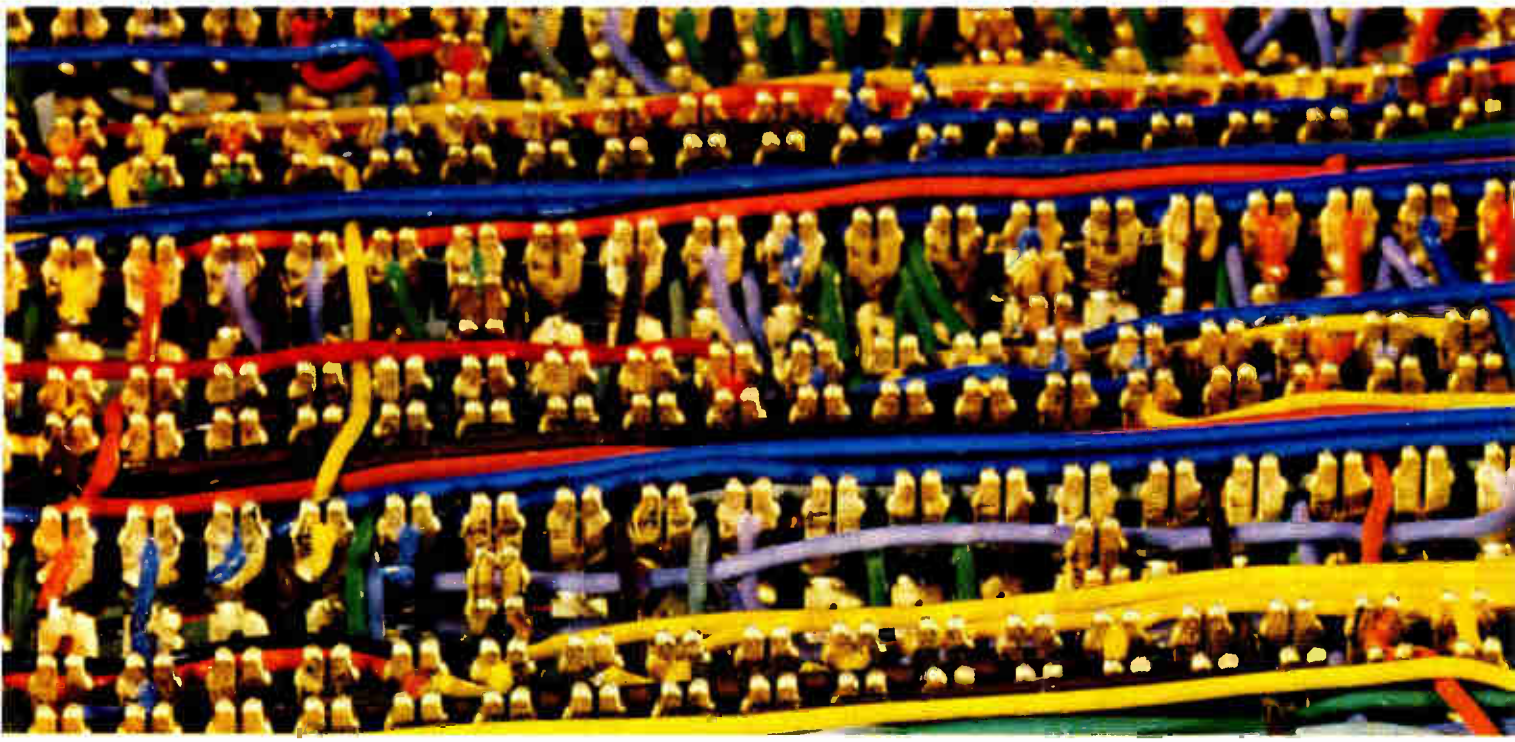

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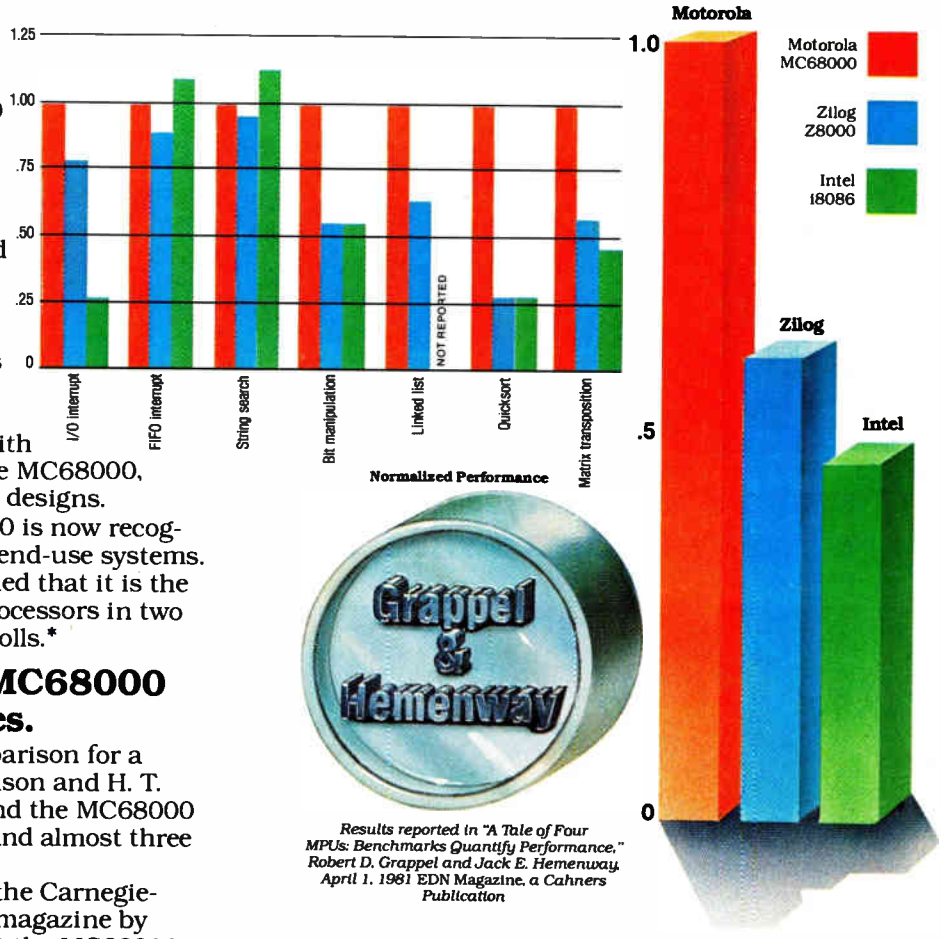
Circle 91 on reader service card

Independent benchmarks MC68000 is first choice



Motorola's advanced MC68000 microprocessor is demonstrably superior for a broad range of 16-bit applications. The evidence is in, and it's conclusive.

The MC68000 consistently and significantly outperformed both the Z8000 and the i8086 in three current independent benchmark studies. Evaluations by engineers not associated with any microprocessor supplier demonstrate that the microprocessor system with the best overall performance is the MC68000, making it the clear choice for new designs.

And it's clear that the MC68000 is now recognized as the competitive edge for end-use systems. Design engineers recently confirmed that it is the first choice among 16-bit microprocessors in two independent product preference polls.*

Benchmarks measure MC68000 performance advantages.

Results of a performance comparison for a digital filter application by V.P. Nelson and H. T. Nagel, published in *IEEE Micro*, find the MC68000 nearly twice as fast as the Z8000 and almost three times as fast as the i8086.

A variety of benchmarks from the Carnegie-Mellon series as reported in *EDN* magazine by Grappel and Hemenway show that the MC68000 is significantly faster than each of these devices in handling routines for Bit Test/Set/Reset, Linked Lists,† Quicksort, and Boolean Matrix. In the same study, it also compares favorably for I/O interrupts. Overall, it outperforms the i8086 by 2.16 to 1.0 and the Z8000 by 1.71 to 1.0, even with the MC68000 addressing its full 16-Megabyte address space and the other two MPUs addressing only 64K.

Benchmarks from the Blacksburg Group, being published by Howard W. Sams and Co., indicate that the MC68000 is two times to three times as fast in four out of five routines compared, including Sorts, Square Root, and Sine Look-up.

Still other benchmarks give the edge to the MC68000 for execution of multiprecision binary and BCD arithmetic operations, 32-bit array scans and string translations. Floating Point arithmetic operations can be carried out almost as fast as hardware implementations.

Results reported in "A Tale of Four MPUs: Benchmarks Quantify Performance," Robert D. Grappel and Jack E. Hemenway, April 1, 1981 EDN Magazine, a Cahners Publication

Memory address, 32-bit features enhance performance.

The performance advantages of the MC68000 demonstrated in the studies are impressive. And the MC68000 has still other capabilities of equal importance in helping keep you ahead of your competition.

The MC68000 has seventeen 32-bit multipurpose registers, with data and address registers separated for parallel operation. All registers can be used as index registers, and all address registers can be used as stack pointers.

No other 16-bit MPU can match the 16-Megabyte direct memory addressing, and programmers need not worry about segmentation and the overhead associated with it.

The simple, efficient instruction set includes 56 powerful types designed to minimize the number of mnemonics a programmer must know. Software development costs are minimized because addressing modes are usable with all applicable instructions.

One other thing. The MC68000 provides, in one high-quality device, what is often found in multi-

*Annual Minicomputer Survey, November 1980, with permission of DATAMATION MAGAZINE, G.S. Grumman/Cowen & Co.

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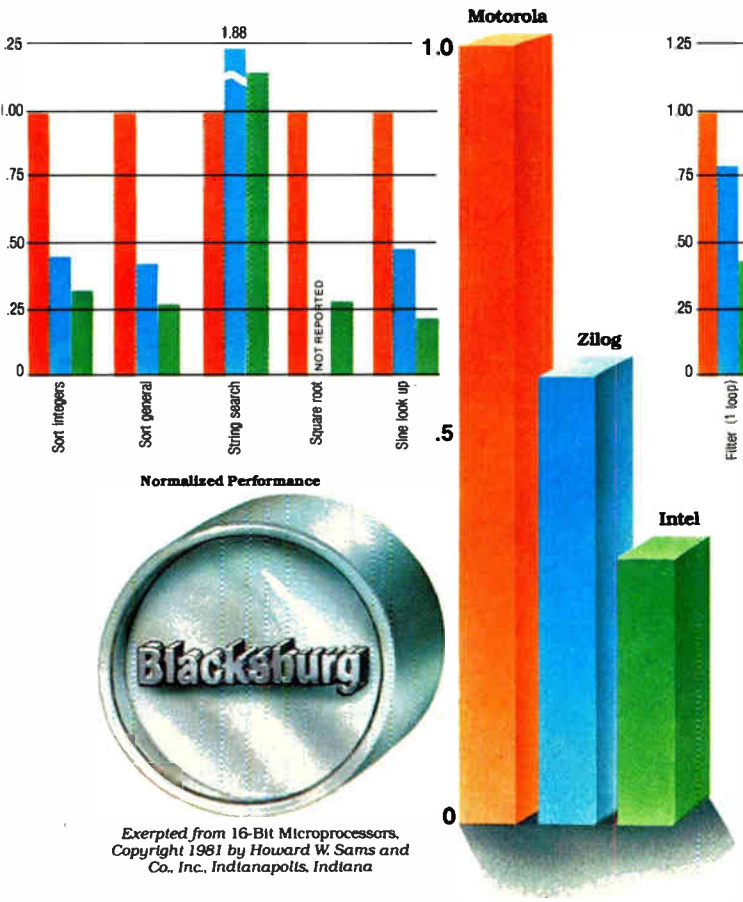
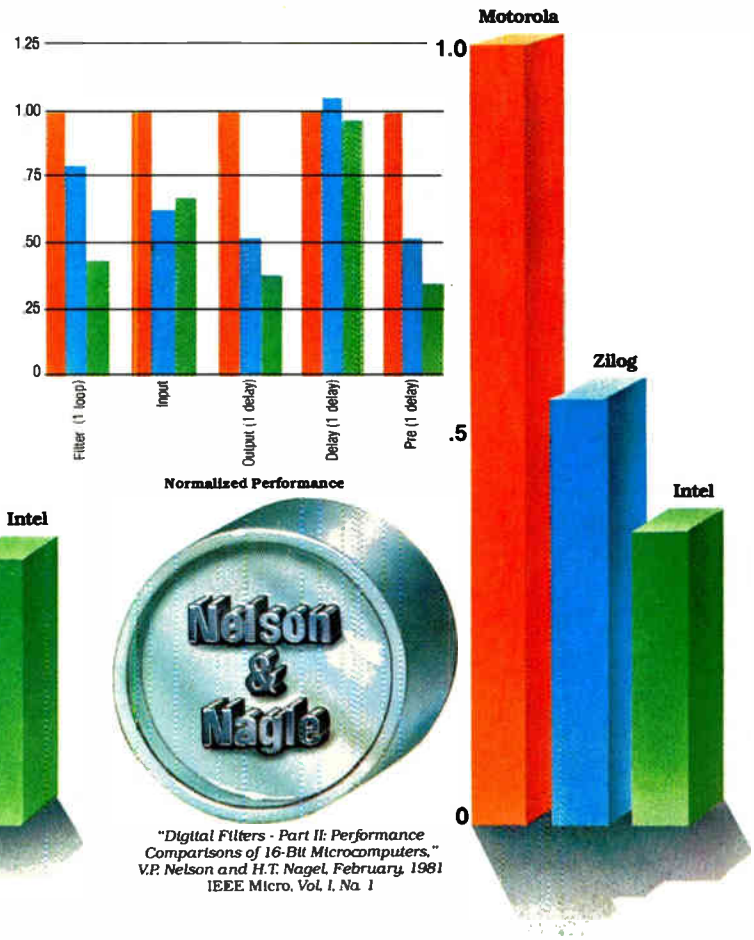
†Not reported for i8086, but Motorola data indicates the MC68000 is more than 20% faster.

demonstrate why the for 16-bit MPU applications.



Exerpted from 16-Bit Microprocessors, Copyright 1981 by Howard W. Sams and Co., Inc., Indianapolis, Indiana



"Digital Filters - Part II: Performance Comparisons of 16-Bit Microcomputers," V.P. Nelson and H.T. Nagel, February, 1981 IEEE Micro, Vol. I, No. 1

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Optical disks excite industry

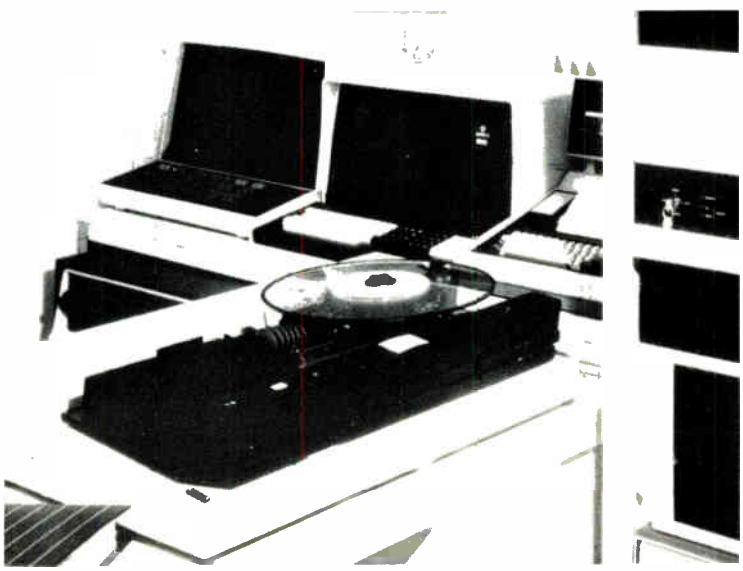
Their promise as a digital data-storage medium spurs a market expected to grow to $1 billion annually by 1990

by Martin Marshall, West Coast Computers & Instruments Editor

Today it replays "The Godfather," "Love Story," or "Saturday Night Fever," but soon the optical disk will be used in a far more sophisticated fashion: as a mass-storage device for digital information, both as a read-only and as a read/write medium. It will become a linchpin of the automated office. It will also make cost-effective whole new system applications and compete significantly with such present technologies as microfiche, magnetic tape, the high-capacity magnetic-disk drive, the magnetic-stripe credit card, and even, in the audio field, the long-playing record.

According to Strategic Inc., of San Jose, Calif., publishers of the most in-depth study on the subject, the optical disk "has the potential of offering greater price-performance ratio improvements in space and cost than any electronic product yet introduced, with the possible exception of the microprocessor." As part of a larger study, the London firm Mackintosh Consultants Ltd. predicts 6,000 optical-disk–based units will be installed by 1990 [*Electronics*, Oct. 23, 1980, p. 95].

These implications have not been lost upon the computer and office automation industries. Although no digital products incorporating optical disks have been announced, the list of companies developing optical players or recorders is a veritable who's who of the industry. Included are such big names as IBM, Exxon, Xerox, Philips, RCA, Bell Laboratories, Thomson-CSF, Wang Laboratories, Control Data, Storage Technology, Burroughs, NCR, Hitachi, Toshiba, Sony, JVC, DiscoVision Associates, Hewlett-Packard, Magnavox, General Electric, and Atlantic Richfield. Smaller firms like DRC-Soundstream Inc. of Salt Lake City, Utah, also want some of the pie. Much of the work is in its early stages; a number of companies will not even admit that they are doing it.



Medium from France. Thomson-CSF developed this prototype of a digital optical-disk system. The list of firms working on recorders or players is long.

The emerging industry will use materials from other companies such as 3M, Drexler Technology, Laser Diode Labs, Optical Coating Laboratory, Energy Conversion Devices, Eastman Kodak, Corning Glass Works, and Matsushita. Still others, like Westinghouse and Hughes Aircraft, as well as universities like the Massachusetts Institute of Technology and Utah State, will add sophisticated software to incorporate optical disks into interactive laser systems.

No boundaries. The interest in optical disks is worldwide. As Jerome Drexler, president of Drexler Technology Corp. of Mountain View, Calif., notes, "Without giving names, I can say that we are currently supplying media to 18 commercial firms, 8 of them American, 5 Japanese, 4 European, and 1 Canadian. Of those, 16 are major companies."

Some of the manufacturers, such as GE, DiscoVision, JVC, and Sony, are expected to remain on the analog, or video disk, side of the optical-disk market [*Electronics*, March 24, p. 42], while others will focus upon digital applications. One of them, IBM Corp., is pursuing both analog and digital technologies. IBM owns half of DiscoVision Associates, a Costa Mesa, Calif., firm that is the largest U. S. supplier of industrial analog video disk players. IBM is also believed to have digital optical-disk development programs in its San Jose, Calif., and Austin, Texas, facilities, as well as ongoing work at its Yorktown Heights, N. Y., research center.

What has attracted this impres-

sive research and development power is the tremendous potential of the optical disk. Like a large magnetic-disk drive, it is a randomly accessed medium. Yet the largest magnetic disk announced so far, the IBM 3380, holds 2.5 gigabytes, and optical disk systems under development can store between 1 and 50 gigabytes per disk.

Not so fast. It is unlikely that optical disk drives will reach the 3380's 16-millisecond access times within the foreseeable future, but many in the field think that they will reach access times of less than 100 ms. Predicts Juan Rodriguez, vice president of technology at Storage Technology Corp. in Louisville, Colo.: "We expect to produce and deliver in quantity a family of digital optical-disk drives by 1984. I would expect them to have capacities of from 10 to 50 gigabytes and access times reaching well under 100 ms, but not as fast as 22 ms."

Storage Technology has had an optical disk program for more than a year. It currently involves more than 60 persons and the company is recruiting heavily. "We expect that number to grow very rapidly very soon," Rodriguez adds. "We believe we are addressing a market that will be direct-read-after-write [DRAW], which is a write-once-only technique, but the company is also very interested in an erasable optical medium as direct competition for magnetic disks."

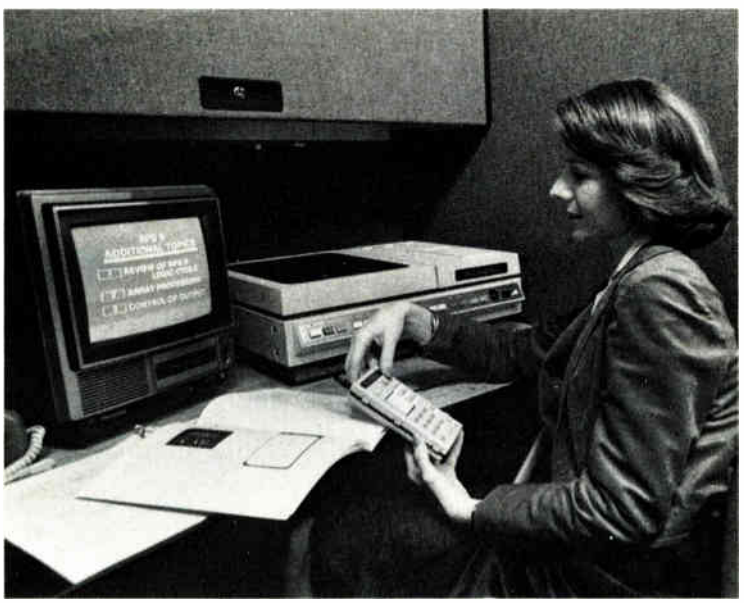
Larry Fujitani, product manager for the Optimem division in Palo Alto, Calif., of Xerox Corp.'s Shugart Associates subsidiary, agrees with the goal of 100 ms but also talks of a second approach. "I can see the achievement of average access times on the order of low-end Winchester disk drives—possibly under 100 ms," he says. "I can also see an approach in which a 700-ms access time is adequate and which results in a much lower-cost system."

Optimem's initial product line is expected to begin with a 1-gigabyte drive using the DRAW technology. The product line is expected to be announced in early 1983, with production units available in late 1983 or early 1984. In keeping with Shugart's low-cost, relatively low-performance strategy, Fujitani notes, the target price of production-run systems in quantities for original-equipment manufacturers could be as low as $3,000 to $4,000. That is significantly lower than expected by outside analysts.

Star player. While both STC and Xerox gear up for 1984, the company thought to be furthest along in the development of a digital optical system is the Star division of Exxon Enterprises Inc., located in Pasadena, Calif.—which, ironically, is for sale. The division generally refuses to talk about its products, but a project manager, Leonard Laub, told an Institute of Electrical and Electronics Engineers conference in Denver last year that the division's player would be deliverable in 1982, that it holds 7.5 gigabytes per disk, and that it will be compatible with recent large IBM computers. The disks alone were expected to be priced at $150 each, or $350 for a two-sided disk enclosed in a cartridge.

Other analysts have added that Exxon plans to use a low-end optical disk drive as part of an office work station targeted at $10,000 to $15,000 for a single-user setup and $5,000 to $10,000 for a single-user station within a multiple-work-station system. The Exxon recorder-player is also believed to incorporate several advanced still-frame video features.

The division is thought to be pursuing another strategy at the same time, one that emphasizes massive storage capacities for government data banks. Those plans, however, may be subject to delay given recent events. After increasing the number of personnel from 45 to about 100 during 1980, the division cut 59 in February and March of this year—and now, as noted, Exxon officials acknowledge that it is up for sale.

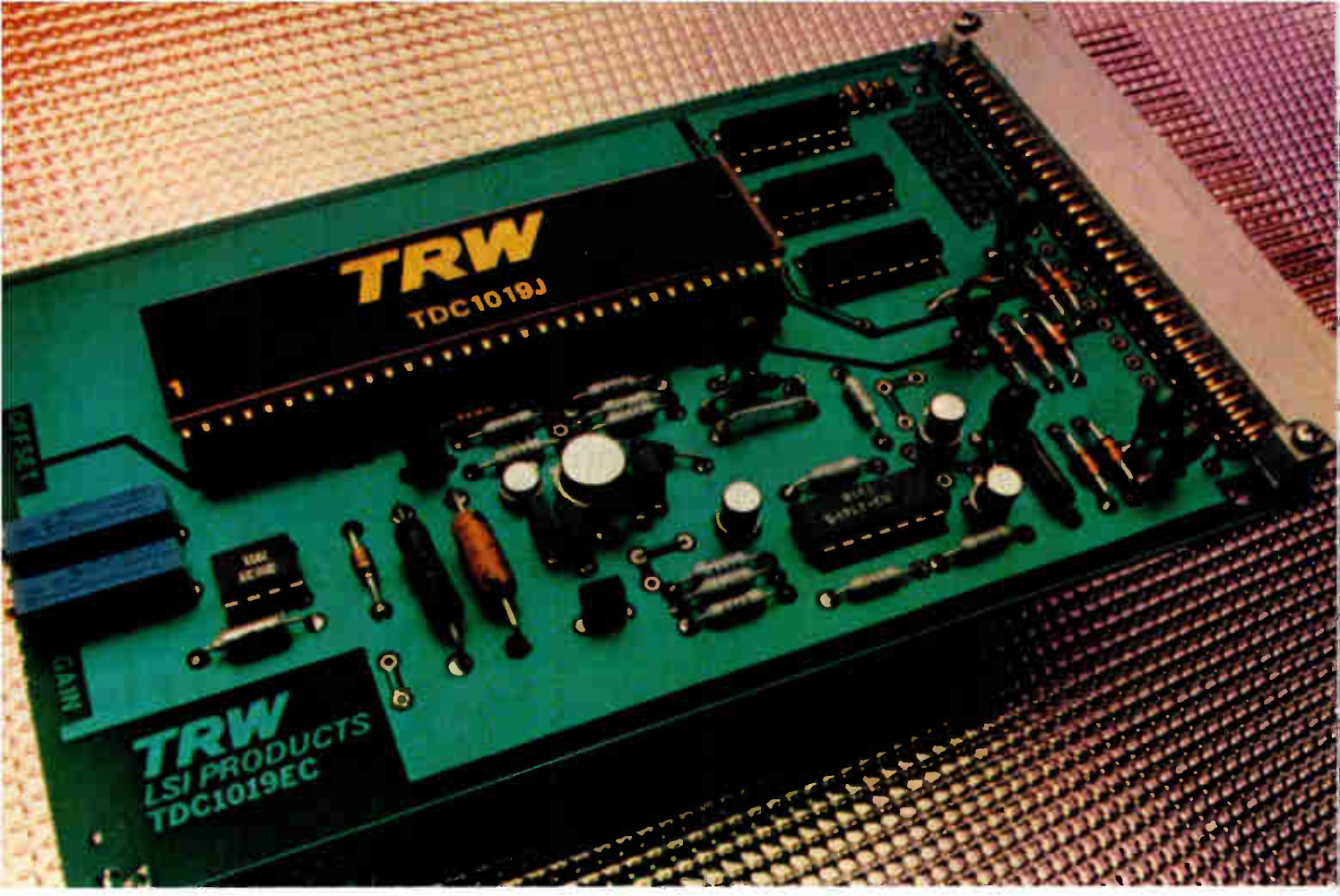


On line. Video disks such as this DiscoVision system installed at an IBM training center in Atlanta are already in use in industrial and commercial environments.

Optical disks have the advantage of being removable and storable, whereas magnetic disks have the advantage of faster access and erasability for rerecording. As a removable medium, optical disks will also present an alternative to magnetic computer tapes. They are more than a hundred times denser than magnetic tape while presenting a significant reduction in the amount of warehouse space required for archiving.

Bits by the quadrillion. As John Woodman, vice president of research at Dean Witter Reynolds Inc. in San Francisco, noted at his firm's seminar last fall, "Friendly Computer Systems": "An oil company, for example, would need to store about 10^{15} bits of data. That would require about 1,350,000 reels of magnetic tape, while the same quantity of data can be stored on 1,000 optical disk packs. The optical disks would require 325 square feet of room space, while the equivalent in magnetic tape would require 8 acres."

Woodman points out that the oil



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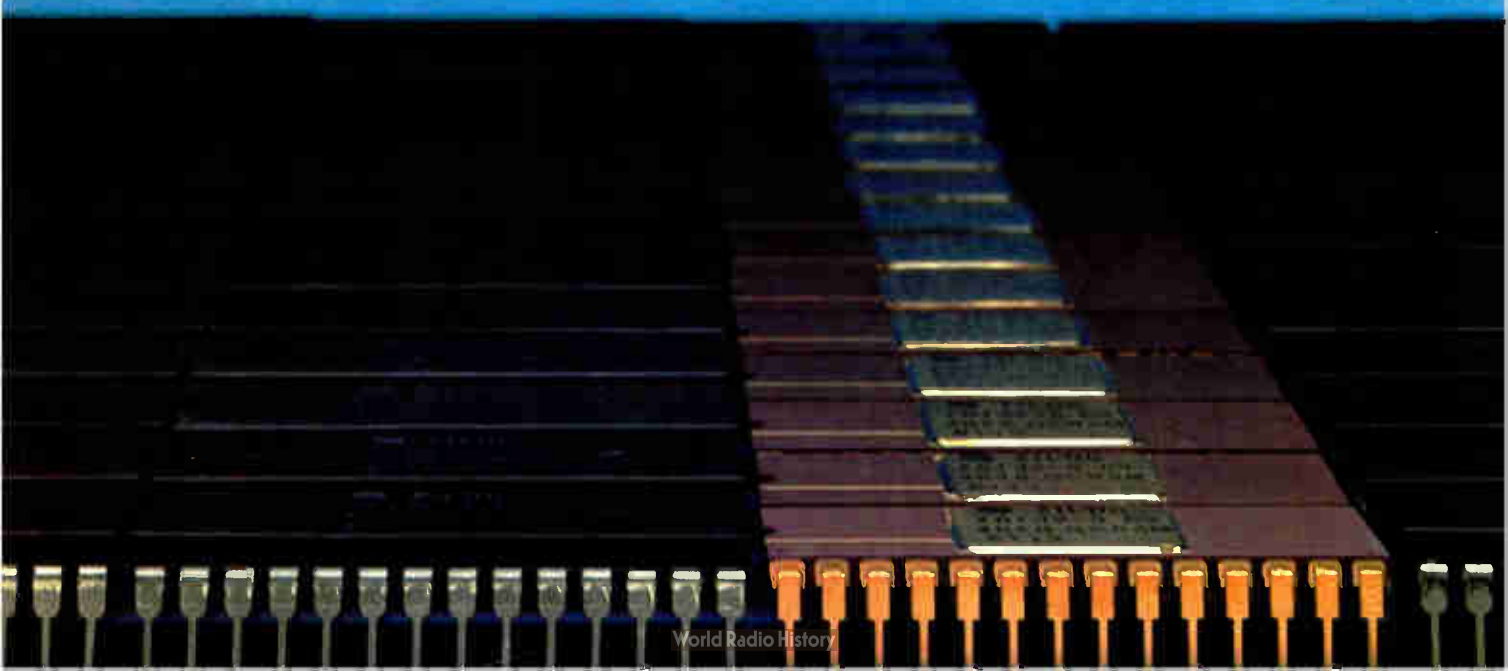


companies would have the largest needs for data storage, followed by the U. S. Social Security library at 350,000 reels of tape, large banks and insurance companies at 10^{14} bits of storage each, and satellite and Census Bureau applications at 10^{13} bits each. Not only that, says Woodman, but goes beyond a relatively few giant companies and Government agencies.

"In terms of the market size for such products, it should be noted that more than 4,000 large-business and scientific computer systems exist today with on-line storage capacity in excess of 2.5 gigabytes," he says.

Another significant advantage that optical disks offer over magnetic tape is that magnetic tape must be rerecorded every six months to two years to avoid data loss, whereas some optical-disk manufacturers are claiming stored data lasts as long as 25 years. These claims have not yet been validated, however, and most of the optical disk researchers claim that even the 10-year claim has yet to be proven.

Media costs. One factor in the tape-disk comparison is becoming clear, however. The cost for media, as calculated by Strategic Inc., will be significantly lower for optical disks than for magnetic tape—by a factor of 3 when comparing silver halide–based optical disks. Data-transfer rates for the two media are about the same, 10 megabits per second, but this factor can be increased for optical disks by using lasers more powerful than 15 milliwatts.

A major use of optical disks will be as the heart of document-storage systems. Applications of the Exxon system, for example, include the storing of images of checks along with accounting information and the establishment of an optical memory "filing cabinet" for the criminal justice system that includes the storage of arrest records together with alphanumeric data.

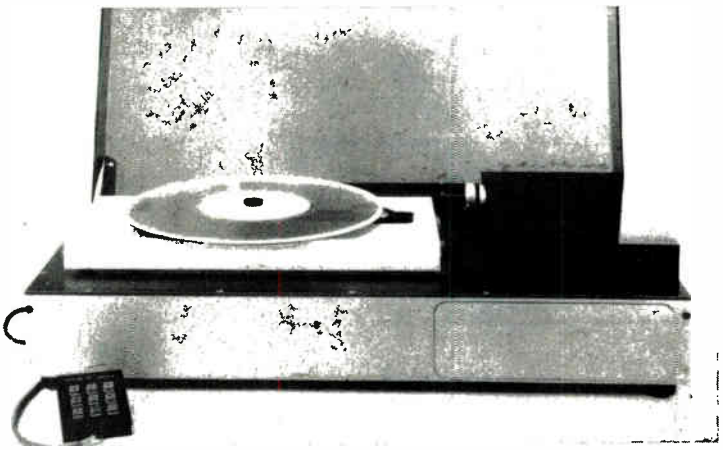
In the image-processing area, optical disks should compare favorably with microfiche in a couple of areas. One optical disk, for example, has the same image-storage capacity as 182.5 feet of microfilm. Optical disks have another advantage in that microfiche is distributed by shipping the microfiche itself, but the contents of an optical disk can be transmitted along any public communications system to another computer or recording system. Microfiche has the advantage, however, of preserving information in a form that is immediately readable by humans.

Four for storage. At least four other manufacturers—Xerox, Toshiba, Philips, and Thomson-CSF—are developing document-storage systems based upon optical disks. Xerox is expected to demonstrate a prototype of its system this summer, targeted for the $15,000-to-$20,000 range and containing a cathode-ray-tube display with a resolution of 1,000 by 1,000 pixels (picture elements). This system will not become a commercial reality until the late 1983 production runs of the Optimem disk system begin. Earlier versions of the Xerox system may appear, however, using an alternative technology as a mass-storage medium.

Toshiba Corp. in Kawasaki, Japan, is scheduled to demonstrate a prototype of its DF-2000 document filing system at this week's National Computer Conference. The system, whose initial development was done by SRI International of Menlo Park, Calif., combines a laser-scanner and laser-printer module with an optical-disk memory module to form a complete system whose price is to be $60,000 when it is commercially introduced in late 1982. Outside analysts, however, believe the system will be priced closer to $45,000.

It will hold 10,000 letter-sized documents and be able to handle a slightly larger B4-sized document. A document is scanned for input within 8.5 seconds; tagging information—such as title and identification number and other flags—is then manually entered through a keyboard and stored with the image. The document reproduction quality is expected to be greater than 200 lines per inch horizontally and about 180 lines vertically, and the system is expected to have gray-scale capability.

With the addition of a one-page storage unit and a high-resolution CRT, it is possible to "browse" through the documents stored on a disk. The time it takes to retrieve a document for display is 4.5 seconds. The compression of 10,000 documents onto a single disk is achieved through a run-length encoding technique that stores only the data and not the spaces in the printed matter.



For broadcasters. Thomson-CSF has incorporated into a broadcast-quality video system a write-once video optical-disk system that can be digital.

Another document storage system under development is the Megadoc system from NV Philips Gloeilampenfabrieken in Eindhoven, the Netherlands. This system uses a "juke box" disk-handling system capable of automatically selecting and playing up to 64 optical disks. Each two-sided disk can store up to 2,500 pictorial documents, or with run-length coding, up to 25,000 per disk with a resolution of 2,400 lines/in. For an ordinary typewritten document, 1,200 lines/in. can be used, which raises the total capacity to 50,000 documents. By going to a complete coding of typewritten documents, capacity can be increased to 500,000 documents per disk. Neither a price nor an introduction date has

been set for the Philips systems.

Paris-based Thomson-CSF has also developed a write-once system that it has incorporated into a broadcast-quality video system. "An important point about the system is that it doesn't have to be analog video—it can be digital," notes Warren Singer, vice president of Thomson-CSF's marketing arm in New York. The system can also store frames.

More than storage. Beyond document storage and aside from its efforts in the consumer video disk field, RCA Corp.'s Applied Physics Laboratory in Camden, N. J., is working on the high-performance end of the digital optical field. Using more powerful gallium-arsenide lasers and an ablative recording technique, RCA has successfully recorded more than 50 megabits per second onto a disk with more than 12 gigabytes of storage. Though this recording was done using a DRAW system, RCA has also done some work with erasability and is evaluating an erasable disk from Corning Glass Works. RCA expects to deliver a specialized, high-performance system in 1982 at an estimated price of $500,000, with disks costing $50.

The projects involving the use of digital optical disks are numerous, but before any of them reaches a mass-production level, the industry must make some technical advances in the key components of the optical disk system. The recent availability of a semiconductor diode laser, Hitachi Ltd.'s 15-mW HLP-1400, has proved to be a great step toward the practicability of optical disks. And the OLX-9000 laser diode and ODX-100 laser driver, to be announced in July by Exxon's Optical Information Systems division in Elmsford, N. Y., should bring lasers close to the life goal of 15 mW for 10,000 hours that many manufacturers have set for commercial success of a DRAW optical-disk system

There is still improvement needed in the disk media themselves, in the read/write head design, and in the lasers. These and other technical barriers, such as reducing the bit-error rate to 10^{-12}, remain to be lowered. □

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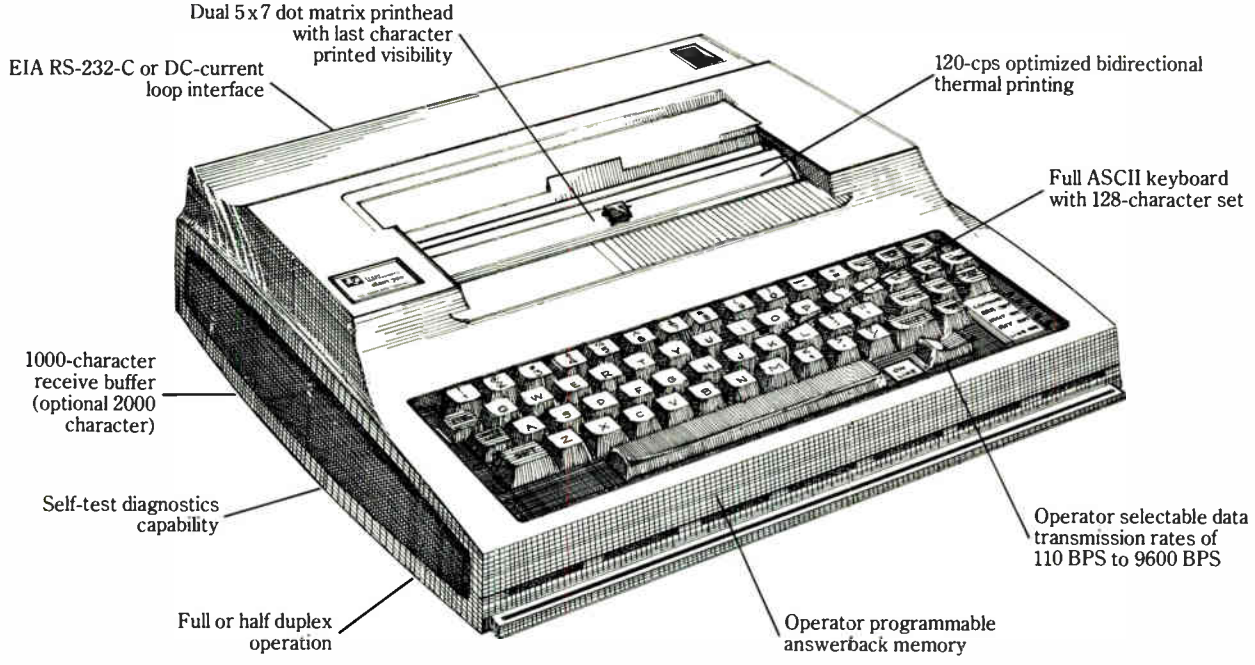

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Advanced Schottky battles MOS

ALS from TI and Fairchild's FAST are leading technologies from TTL makers in their effort to head off rival

by Bruce LeBoss, San Francisco regional bureau manager

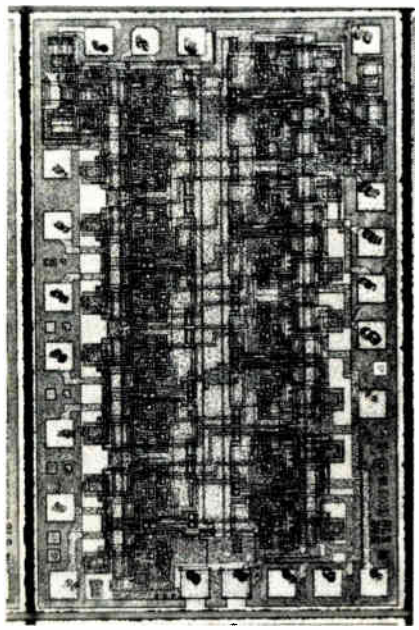
They have more than two thirds of the estimated $1.5 billion U. S. market for standard logic devices and want to keep it, so manufacturers of bipolar TTL families are rising to meet the challenge of new high-speed MOS devices. Traditional suppliers of Schottky and low-power Schottky small- and medium-scale integrated logic are using several advanced Schottky technologies to fortify their position.

Two appear to be the major weapons against complementary-MOS and high-performance n-channel MOS, or H-MOS, logic devices. They are Texas Instruments Inc.'s advanced low-power Schottky (ALS) family of TTL circuits, and the Fairchild Advanced Schottky TTL (FAST) line of bipolar circuits from Fairchild Camera & Instrument Corp.

The ALS family will initially consist of some 60 to 70 functions that exist in present low-power Schottky, or LS, devices but at half the power-per-gate dissipation and improved speed—a 4-nanosecond gate delay. It is expected to grow to 150 functions by the end of 1982, when it will cost about half again more than its LS equivalents. At present, there is an 80% premium for ALS family members, with parity expected in 1983. Advocates include National Semiconductor Corp. and Motorola Inc.'s Semiconductor Group, both of which have disclosed plans to make ALS products, as well as Signetics Corp. and Monolithic Memories Inc., which are leaning in that direction, as is Japan's Hitachi Ltd.

In contrast, Fairchild's FAST family is a pin-for-pin replacement for current standard Schottky logic circuits. These devices employ an oxide isolation process that imparts a 50% speed improvement over standard Schottky parts and, with typical internal gate delays of 1.5 ns, are perhaps the fastest form of TTL on the market; the process uses 75% less power.

Taking two routes. Most recently, Signetics hedged its ALS bet by becoming the first official entrant into the FAST camp with the signing of a second-source accord to make and market all 37 products in the family, as well as some proprietary products of its own design [*Electronics*, Feb. 24, p. 36]. And Monolithic Memories, like Signetics in Sunnyvale, Calif., is similarly committing itself to a FAST-like offering, but not before 1982.

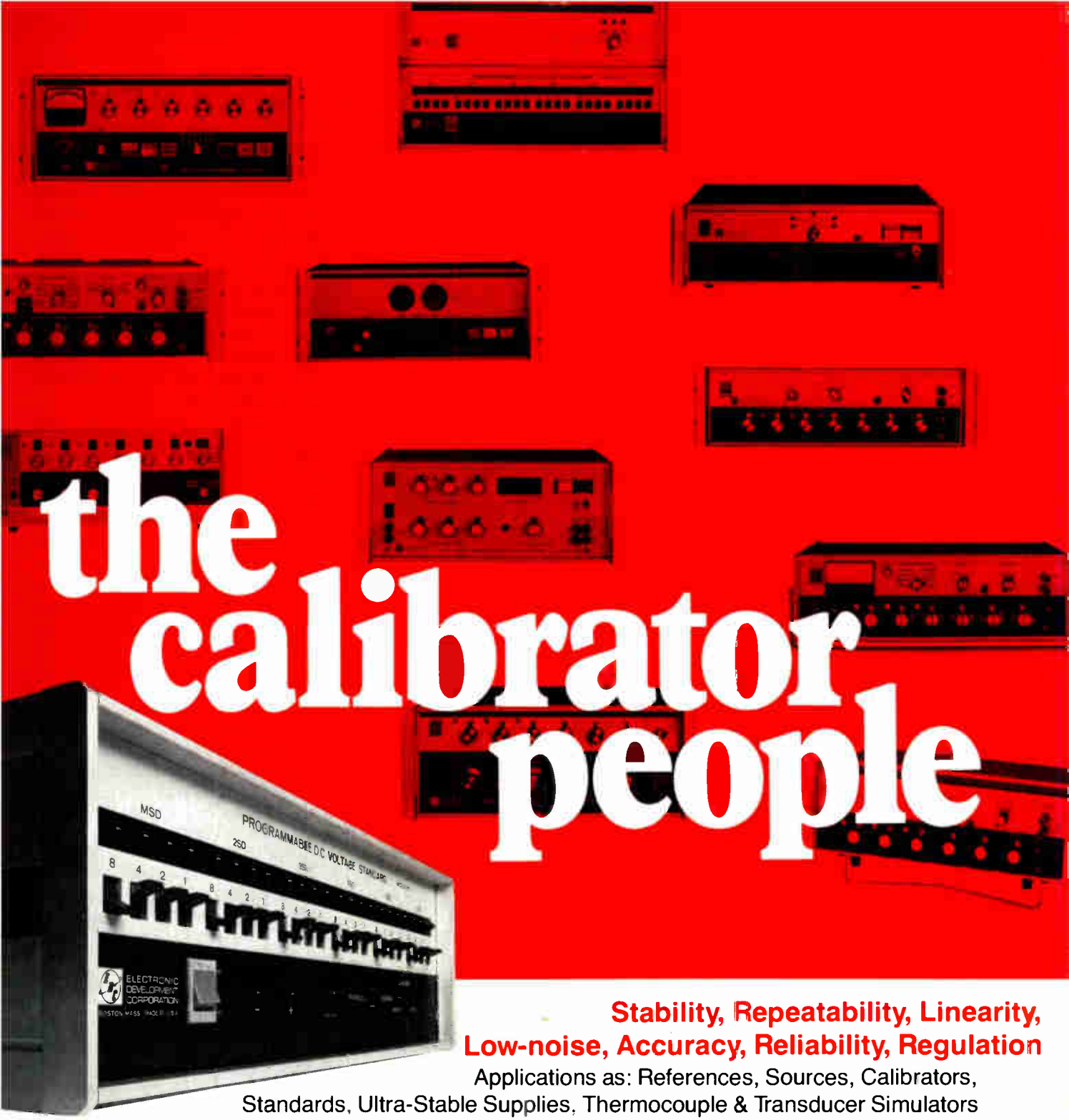


Part of quartet. Built with TI's ALS, or advanced low-power Schottky, technology, this 54/74 ALS245 octal bus transceiver is one of Motorola's first four ALS parts.

Though there are at least two other advanced Schottky technologies, they are meeting with limited, if not questionable, success. One is National's LSS family, which "was never really intended to be another family, as are AS and ALS, but is the result of several revisions of our existing LS family that enhanced its speed and noise immunity," states Tom Thorkelson, director of digital logic marketing for the Santa Clara, Calif., firm. Another is TI's advanced Schottky, or AS, family, which was initially planned for new functions not existing in the firm's 74S series.

However, the Dallas company is now shifting its AS strategy to include functions that are pin-compatible with its current Schottky lines. The move comes after it "detected an interest in duplicating some of the current Schottky functions in the new AS line," says Tom Balch, marketing manager for digital circuits logic. "Although TI doesn't plan to duplicate its entire 74S line in AS," he adds, "we will initially target some of the octal functions and microprocessor-support functions," among others.

The switch in AS strategy, Balch notes, was not a result of sluggish customer acceptance of the line, which is based on a new technology with tighter geometries than the firm's earlier Schottky offerings. "The big difference in the original AS program is that we conceptualized a totally new family of higher-complexity logic products in 20- and 24-pin, 300-mil-wide packages, which would effectively enhance utilization of board space through closer packet densities," he explains. "We are changing the program



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Thus far, TI has not unveiled any AS products for the market, but it plans to begin providing samples of 8 to 10 functions this quarter and a like amount in the third quarter. "We will be in production some time in the second half of 1981," estimates Balch, who says TI is planning to introduce about 50 AS functions in all.

Meanwhile, TI's ALS operation is gearing up for the production of its first medium-scale products, according to Bill Kean, operations marketing manager. "We have just finished full engineering characterizations of our first set of MSI products, the parts that will really tell customers what the speed and power of the family is," he says.

The ALS operation, which to date has offered small-scale integration gate and dual flip-flop devices, will soon release the 74ALS574, among other MSI units. It is like the older LS374, Kean says, except for changes to a couple of the I/O pins that make it easier for the customer to lay out on the board.

What's more, the ALS function demonstrates "tremendous improvement in power and speed," when compared with the LS part, Kean says. The LS374 has a maximum power dissipation of 40 milliamperes, while the ALS574's is a third lower. Also, the LS374 was rated at 28 ns at 5 volts (±5%) and 25°C operation. The new ALS574 is rated at 12 ns at 5 V (±10%) over the full commercial temperature range of 0°C to 70°C.

Another idea. Meanwhile, TI is not the only supplier giving second thoughts to its strategy in the market. For example, at Motorola's Semiconductor Group in Phoenix, the initial plan was to aim for the most complex, high-power small-scale LS sockets with lower-power, slightly faster ALS parts, and the 25 to 30 ALS parts set for introduction this year reflect that.

"Our original thought was that ALS is more of a supplement than a replacement" to LS, says George Turner, TTL/MECL product engineering manager at Motorola's Bipolar IC division in Mesa, Ariz. "But now the market is getting a little confusing," he adds, noting that there is a question about whether users "are going to dive in and replace all LS immediately." If so, the Motorola marketer notes, his firm would be hard pressed to change plans rapidly.

In the interim, Motorola is just now releasing its first four ALS parts built under its licensing accord with TI. All octal devices, they are the ALS245 octal bus transceiver, ALS640 inverter, ALS641 open collector, and ALS642 inverting octal bus open collector.

Out in Silicon Valley, the trend appears to be to plant a foot in both ALS and FAST camps. In explanation, Phil Ortiz, TTL marketing manager for Signetics' Logic division,

A view of advanced Schottky circuits

The way Monolithic Memories Inc.'s product planning and applications manager, Shlomo Waser, sees things could be the way users will perceive advanced Schottky device. He concurs that "ALS is a good way to go for those people who are more concerned about power than speed. It is likely we will offer something along the lines of ALS." For high-speed applications, however, Waser sees two approaches being taken by his Sunnyvale, Calif., company. One, where users are more concerned about speed almost at any price, they are opting for emitter-coupled-logic devices. The other is where it isn't necessary to "eke out every nanosecond" and, he states, "Fairchild's FAST is a nice compromise."

"AS is attempting, unsuccessfully, to reach ECL performance, yet it has all of ECL's drawbacks, including very high power dissipation. Also, when working the FAST in TTL-type circuits, the AS devices have very fast rise times when switching from 0 to 5 V. These FAST edges will create lots of noise and make it very difficult to design with the parts," Waser says.

says it is "a lot faster than standard Schottky at a fraction of the power, and users can receive immediate speed/power benefits."

First parts. Initially, Signetics plans to offer about three dozen FAST parts that, unlike AS parts, will fill standard Schottky and LS sockets. The first four are slated for availability by the end of the year, and introductions of the rest are divided almost equally between the first and second halves of 1982.

"We have also made a commitment to do some form of low-power Schottky logic, but haven't yet decided how to pursue this," says Ortiz. "We definitely will participate in the ALS arena, as ALS is emerging as a major technology, and we will have some standard and some proprietary parts," the first of which will be available next year.

"As yet, there's no clear conviction from the marketplace that AS is a winner," he adds. "We did customer surveys, and there's not a single major data-processing user who isn't evaluating FAST. That's not true with AS, so we have ruled out AS as a viable product line."

Daily double. However, National is counting on both AS and ALS to be winners, notes Thorkelson, who says the firm's "goal is to be an additional source of both families, and not do any oneupmanship on the families." Rather, the firm will simply make "pin-for-pin, spec-for-spec" replacements, he adds.

National's current plan calls for it to produce about 75 to 90 products in these families, about three quarters of which will be of the ALS variety. The first AS devices will be ready in sample quantities in the third quarter. The following quarter, about a dozen devices will surface, most, if not all, ALS. The remainder of the currently planned AS and ALS devices are slated for availability by the end of 1982, he notes.

"For the guy who is absolutely a speed freak and who wants to squeeze out the last nanosecond of propagation, AS is the way to go, at the expense of the older standard Schottky devices," Thorkelson says. "However, where the speed-power product is of greater importance, people are tending toward ALS in place of the older LS parts." □

Computers

System maintenance firms find a niche

Third-party repair contractors establish a growth industry as growing complexity of systems bedevils users

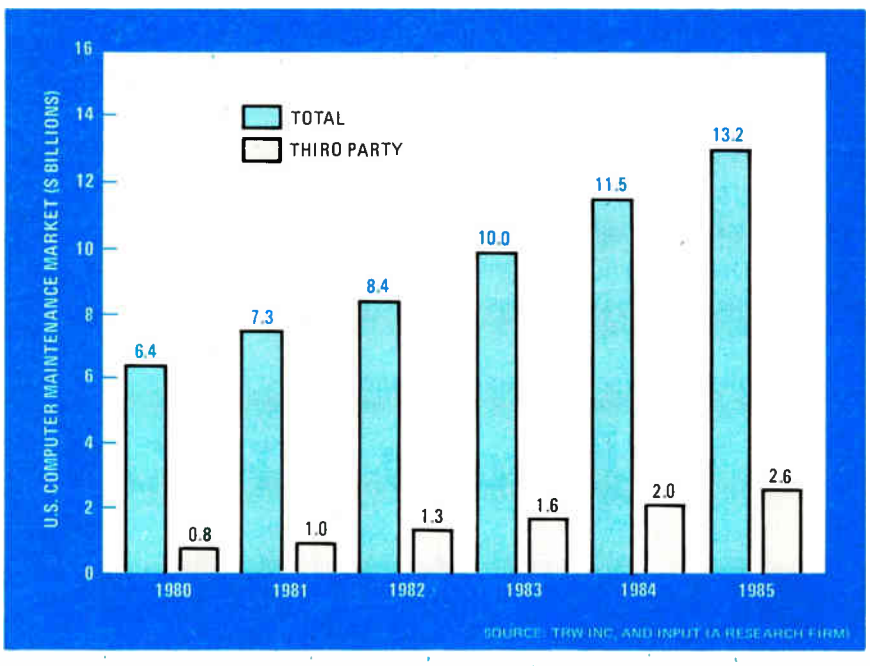
by Terry Costlow, Costa Mesa bureau

As the number of computer installations increases, the costs and complexities encountered by manufacturers servicing them in the field have also skyrocketed. For this reason, outside, or third-party, maintenance firms have grown in both size and number, much faster than anticipated, with no signs of slowing.

"The subscriber business [as some call third-party maintenance] is growing like crazy. More and more manufacturers are finding they don't understand maintenance, and it's costly to start a service organization from scratch," says Pat Lydon, vice president and general manager of Pertec Computer Corp.'s Service division in Los Angeles, which services Printronix Inc., Cincinnati Milacron Inc., and Ultimate Corp. products along with its own.

Rapid growth began after 1975, with 40% of the current participants in the market opening their doors since then, according to a recent report from Frost & Sullivan Inc., the New York market-research firm. Even though computer maintenance has become big business, the growth prospects for the third-party industry are still shrouded in uncertainty, as is evidenced by the disparity in projected industrywide revenue figures. Frost & Sullivan predicts revenues of $432 million this year, jumping to $620 million in 1985. In contrast, TRW Inc.'s Customer Service division in Fairfield, N. J., the largest service firm, estimates industrywide revenues of $1 billion in 1981, increasing to $2.6 billion in 1985.

TRW and the Sorbus Service division of MAI in Frazer, Pa., are the two largest in the field, with a combined market share of 41%, according to the Frost & Sullivan report. Below that, rankings are skewed by maintenance divisions that handle both third-party servicing and repairs for their parent company.



Long road. In spite of their size and numbers, the third-party companies have a considerably long way to go before they comprise more than a fraction of the total maintenance marketplace, which is estimated by Input, a Menlo Park, Calif., research group, at $7.3 billion during 1981. Maynard Smith, vice president and general manager of TRW's Customer Service division, notes that projected 1981 revenues of $120 million to $150 million place TRW only eighth on the maintenance scorecard, which includes the likes of IBM Corp. and Honeywell Inc. "We look large in the third-party market, but we're low in the total marketplace," he says.

Future growth is also hamperd by a feeling by many manufacturers that they can handle repairs much better themselves. Even some users of third-party maintenance regard it as a necessary evil. For example, Four Phase Inc., a Cupertino, Calif., manufacturer, used third-party maintenance for years, but gradually phased it out as the firm grew large enough to support a service division. "You can't control your own destiny without your own organization," says Ron Garrison, vice president of field engineering.

Other firms find that use of a third party is vital. Dataproducts Corp., a Woodland Hills, Calif., printer manufacturer, moved to third-party maintenance after letting original-equipment manufacturers handle on-site servicing when the

firm began a distributor network. "We felt we had to supply servicing in order to help the distributors. We couldn't be as successful in the distributor marketplace without national servicing," says Dennis Bentson, program manager.

Attitudes have improved, though. "I've seen the field of third-party maintenance go from a dirty word to a respected industry," says William J. Herbert, president of Indeserv Inc., a Littleton, Mass., firm that services companies like Centronics Data Computer Corp. and Nixdorf Computer Corp.

Common woes. The very factors that lead manufacturers to these service groups—the costs of maintaining inventory and personnel at remote stations—also cause the repair companies the most headaches. Sorbus carries more than 100,000 parts in 3,200 locations. TRW's rule of thumb at service sites is one set of spares for each 10 machines being handled, giving them a total inventory of more than 700,000 parts.

Also vital is efficient personnel management, since the keys to a successful operation are quick response and repair times, and keeping the field engineers productive. They must have a wide scope of knowledge and the ability to work under time pressure, repairing a critical machine while office personnel sit idly waiting. "We've always had trouble finding trained people," says Ivan S. Jaffe, vice president of Olivetti Corp.'s customer engineering and supply sale division in Tarrytown, N. Y. Sorbus estimates its turnover rate at 12%, but says that industry-wide the figure is about 30%.

Most executives feel that the trend toward self-diagnostics and user-replaceable modules will do little to alleviate their present personnel problems. "For example, at Chase Manhattan Bank customers will not do their own maintenance," Stephen J. Keane, Sorbus president, notes. Although these trends may make it easier for engineers in the field, the sheer number and complexity of models on the market makes repairs increasingly difficult. Most firms have specialists to handle problems field engineers cannot.

A neglected area that is now moving into the spotlight is servicing software. Field engineers need not be programmers, but they must know something about it. "Understanding software is part of identifying where a problem lies, and when it's in software, that can be subtle," says Indeserv's Herbert.

Choosing which machines will be serviced is the first decision for a firm, since a lemon could require an inordinate amount of repair time. The service groups first analyze a product line to forecast the number of breakdowns and the time required to get them up again, and then decide whether to take on the line. "We can't service everything," one executive says. Service pricing is also based on this analysis.

Each firm has its own criteria for pricing. TRW makes agreements with manufacturers, but signs the repair contracts with end users. TRW's charges range from 5% to 18% of the cost of the product per year, depending on the cost of the unit and the company's analysis. Past pricing has been contracted for unlimited services calls, but TRW is now testing transaction pricing, in which a set number of calls is included in the contract, and the cost of each additional call increases as the number of calls goes up. Smith feels this approach may become popular, partially because it will lower the number of unnecessary calls.

Same prices. End users also choose between third-party service organizations designated or simply equipped to maintain their equipment—even in preference to a manufacturer's own service organization. Although competition is heavy in metropolitan areas, pricing doesn't vary much. Response time, repair time, the number of service representatives in an area, and the location of service sites determine who gets the contract.

Some third-party firms will contract with their regional counterparts when they get a contract in a city where they don't have a service site. Speculation on the possible growth of these regional firms, or a possible shakeout that would see them disappear, is another area of disagreement across the industry. Olivetti's Jaffe sees them as fading away because of the personnel and inventory expenses. □

Communications

NTT tells how to crack its market

Two three-day seminars in U. S. were designed to acquaint Americans with rules governing interconnection gear in Japan

by Harvey J. Hindin, Communications & Microwave Editor

Normally, Japan's giant Nippon Telegraph & Telephone Public Corp. does not visit people who want to do business with it. It doesn't have to: the company that provides Japan with all its internal telephone, Telex, leased-circuit, and data-communications services has a monopolistic structure that even old-timers at American Telephone & Telegraph Co. view with envy.

But even so, NTT last month finally went shopping for suppliers. Meeting with prospective vendors in Los Angeles and Washington, D. C., officials of the company worked hard as they sought to spread the word that anyone anywhere who meets its technical requirements can be a supplier.

NTT did not volunteer for the mission. Rather, it was the result of the bilateral agreement between Japan and the U. S. that opened the NTT market to companies other than the big four—Toshiba, Hitachi, Nippon Electric, and Fujitsu—and the 200 other companies that are NTT-authorized to supply components to them. Still, the always pragmatic Japanese had a job to do and they managed it well.

The message of the smooth, three-day presentations is summed up best by Toshiro Nagasawa, senior staff engineer at NTT's plant engineering bureau, when he says, "If you conform to the technical requirements, then your equipment can be connected to the NTT network." What attendees got in return for sitting through the long drawn-out proceedings—one Washington listener from the Department of Commerce said they could have been given in one day—was an outline and details of the steps required for selling equipment to the Japanese interconnection industry. This includes private automated branch exchanges (PABXs), modems, and acoustic couplers, all to be sold to NTT's customers. NTT, by means of its concept of type acceptance, has the final say on what may be connected. An analogy drawn by David R. Macdonald, deputy U. S. trade representative, likens the NTT procurement process to that of a U. S. Government agency.

Detailed data. There was much repetition of the obvious, but the high point and conceivably most valuable information taken away from the session by prospective vendors was the literature package distributed by NTT that described the specifications for interconnection equipment. Included were detailed data on PABXs, terminal equipment for leased circuits, key equipment, Telex equipment, acoustic couplers, telegraphy circuits, and other customer-premises gear that make up a billion-dollar market.

How sincere was NTT? As Rene M. Valverde of International Telephone & Telegraph Corp. puts it, "By design this seminar shows foreign vendors how to sell to NTT's customers. While there is a certain amount of public relations involved, it's clear to me that NTT really means it." Valverde is ITT's manager for business systems, Asia-Pacific and Latin America.

Others echo that opinion. For example, John G. Rehak, vice president of Siemens Corp. stationed in Washington, says that there is "no question that NTT was serious." Rehak cautions, though, that technical requirements are one thing but language is another. "You must do business in Japanese," he says. "If you were to bring specs in, say, French to this country your custom-

SIZE AND GROWTH OF INTERCONNECT MARKET IN JAPAN
(Estimated in millions of dollars)

Equipment	Fiscal 1978		Fiscal 1979	
	NTT	Customer-provided equipment	NTT	Customer-provided equipment
Private branch exchange	6	90	17	95
Telephone equipment	265	90	285	110
Facsimile	20	175	25	265
Modem	25	25	30	40
Data terminal equipment	120	285	175	405
Network control units	4	3	4	3
Acoustic coupler	– –	16	– –	25
Other	10	40	10	50
Total	450	724	546	993

Source: NTT

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ers would probably laugh at you."

Nevertheless, some session participants were skeptical that the seminars would provide a way to counterbalance the flow of Hondas and Toyotas to the U. S., saying that only time would tell. "Sure," said one, "there will be some contracts let—Motorola, for one, has just gotten one for pagers—but the real question is final market share. Talk to me in five years—then we will know if we have made a dent in the NTT market."

That view assumes that American companies will make the admittedly major effort needed to crack the market. But it is not yet clear that this will be the case. There are barriers: language, the cost of a Japanese office (maintaining one staff member and a secretary in Tokyo can cost upwards of a quarter of a million dollars a year), and the maze of compliance procedures. Products for the interconnection market must be certified and tested by NTT-licensed engineers and often must have protective devices to isolate them from NTT circuitry should problems occur. Furthermore, NTT often requires self-test capabilities to protect its network.

The key to what kind of effort will be made is the question of whether there is real interest. True, major companies interested in selling to the giant Japanese market have not been sitting around waiting for three-day seminars dealing a good deal of the time with amenities and good will. They have been doing their homework through Japanese representatives, consultants, and their own people. However, though such major companies as Codex, Comsat, and Atlantic Research were represented at the Washington seminar, it appeared that most of the slightly fewer than 100 who attended were members of the press, lawyers, consultants looking for work, or members of various U. S. Government agencies. Not only were major firms not out in force, but small companies also were absent. If this is an accurate indication of interest, market penetration will be shallow.

Varied interest. William J. Sullivan, industry analyst for the science and electronics division of the Commerce Department, took the optimistic view that the seminars were but a first step. "We are working hard to get more and more companies—especially the medium-sized and small ones—to look into the Japanese market," he says. "We are ready to do all we can to make their efforts profitable."

Sensing those profits, AT&T had representatives at the meeting, perhaps gathering information for its as yet unborn unregulated subsidiary. That company, already dubbed Baby Bell, should be able to sell interconnection equipment in Japan as well as or better than any other company. After all, it was an AT&T team, working under the auspices of American occupation authorities after World War II, that helped to organize NTT. □

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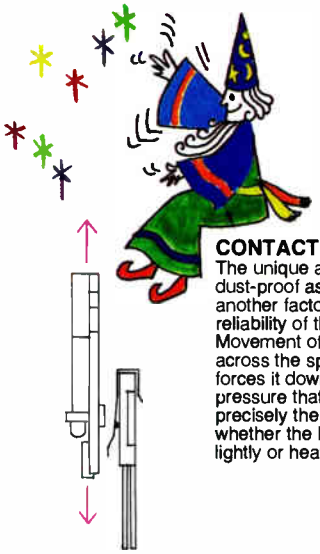

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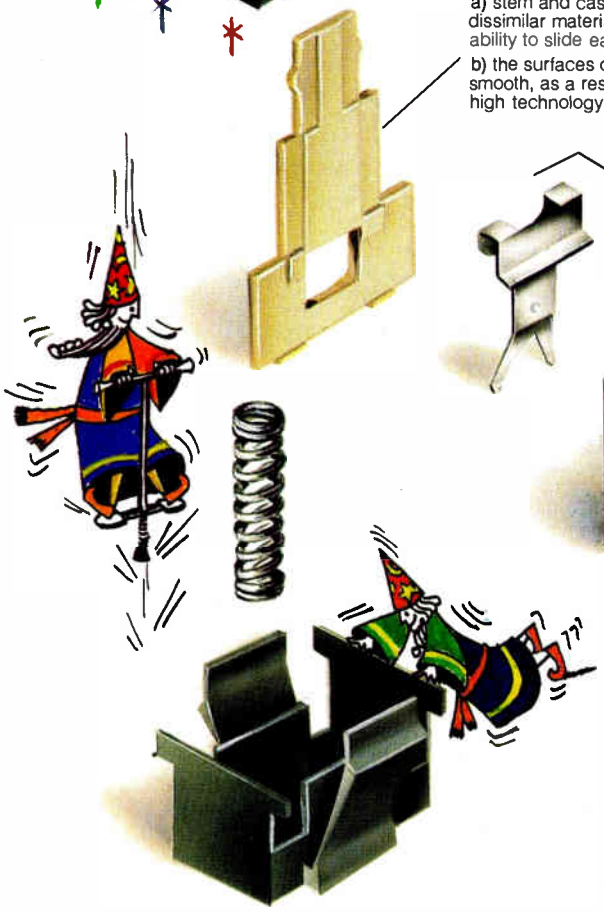

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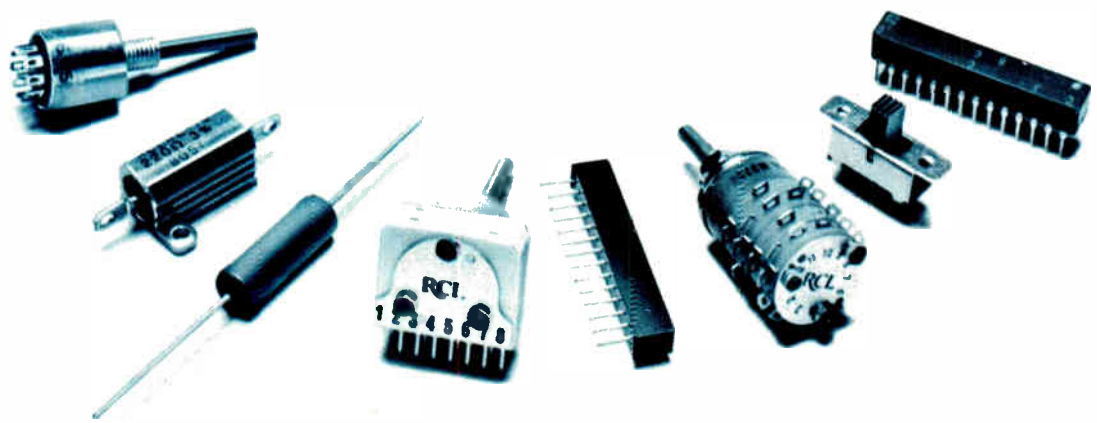

AMF Electro-Components Division manufactures RCL Resistors, Delay Lines, Switches & UID Switches

Circle 117 on reader service card

The weapon that helped change WW II was a small piece of carbon.

The strategy was sound. Fly higher. Get above the limits of the fighters. Get beyond the range of the ground batteries.

But the wild blue yonder is a forbidding place. It's colder and drier than you can imagine. So, as our aircraft tried to fly higher and higher, they soon had to come right back down. The generator brushes were rapidly wearing away to dust in the superdry air of the stratosphere.

We went to work on the problem. And, in 1942, Stackpole helped perfect the first high-altitude aircraft brushes. To shorten a war. To pave the way into space.

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We cite this bit of history for two reasons. One: because we're proud of it. And two: because it's a good example of how we work. Every day.

A lot of companies come up with a product, then look for needs or applications where it *may* fit. We work the opposite at Stackpole. Someone has a need or application, then we come up with the product that *will* fit.

What and how are inseparable.

We know materials and how to work with them.

We know the what: carbon and graphite in powder, bulk and fiber forms; ceramic ferrites; precious metals; and powder metallurgy.

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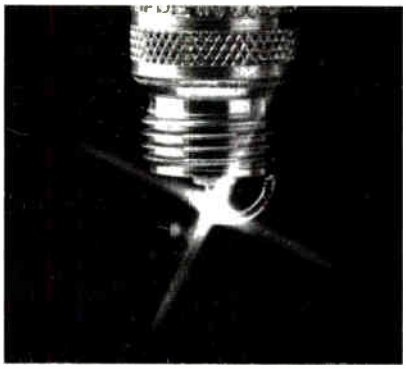
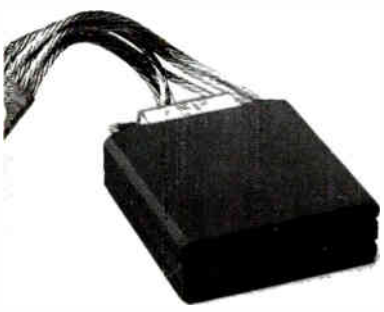
Next time you have a specific need, call our application engineers. For the product that fits. In the meantime, get to know our resources better. Call or write: Dauer Stackpole, The Stackpole Corporation, St. Marys, Pa. 15857. (814) 781-1234.

STACKPOLE



Once, someone needed a ceramic resistor for spark plugs. To make the car radio a static-free reality. We now make millions of such resistors every week.

Once, someone wanted to move the television set from the laboratory to the living room. But it had to be safe. We helped develop the ferrite flyback transformer core. Today, our ferrite cores are in millions of TV sets and switch-mode power supplies, worldwide.



Once, someone needed a railroad brush suitable for both heavy freight and high-speed commuter traffic. Today, our wafer brushes are in thousands of diesel locomotives.

Our workday runs from 1906 through tomorrow.

Circle 119 on reader service card

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The Gould ES 1000 analog electrostatic recorder combines high speed, flexibility and digital accuracy, for new highs in performance.

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- Permanent, high contrast record on low cost paper.
- Simultaneous printing of grids and alphanumeric annotation for accurate and complete records.
- High transient response up to 40 μs.

For full information, write Gould Inc., Instruments Division, 3631 Perkins Avenue, Cleveland, Ohio 44114. Or call toll-free 800-331-1000.

GOULD

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Circle 120 on reader service card

Quality at Low Cost.

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- Full scale zero position.
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To learn more about our 3050 series analog X-Y recorders and our compatible signal conditioners, write Gould Inc., Instruments Division, 3631 Perkins Avenue, Cleveland, OH 44114, or phone 800-331-1000. (In Oklahoma, call collect 918-664-8300.)

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The Gould TA600 uses fixed thermal linear array writing to bring digital accuracy and full annotation to analog recording.

Features include:

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- Chart speeds from 1 mm/h to 50 mm/s.
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- Simultaneous printing of traces and grids on low cost paper.
- No moving writing mechanism.

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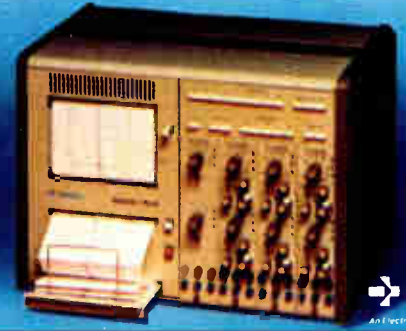

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The Instant Replay Family.

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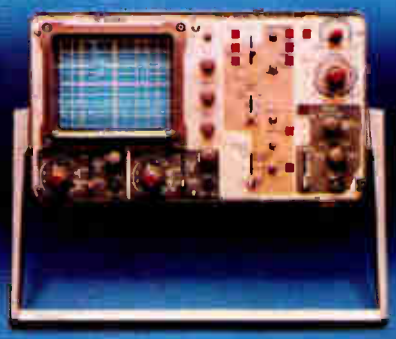

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Three ways of correcting erroneous data

Memory and data-transmission errors yield to hardware implementations of detection and correction techniques developed by mathematicians

As memory densities continue to increase, so does the risk of errors. Alpha particles and electric noise plague the newer, denser semiconductor memories, and surface damage on magnetic disks is becoming more troublesome now that bits are being crammed into smaller areas.

To remedy these problems, more and more manufacturers are adopting error-detection and -correction schemes. The grandfather of them all uses the parity bit, which simply records whether the number of binary 1s in one memory location is even or odd and thus detects only single-bit errors. Luckily mathematicians are forever contriving new ways of uncovering even multiple-bit errors.

One of the most advanced uses Fire code to detect and correct up to 12 erroneous bits. In this method, the iterative division of a data stream produces a fixed number of check bits that are appended to each disk record. When that same record is read, its check bits are used to detect, locate, and correct any error bursts that might be due to imperfections in the disk. The first of the following three articles describes how hardware, in the form of a unique large-scale integrated chip, can be used to realize the Fire codes.

Hamming codes have proved particularly useful in a semiconductor memory context. They append a fixed number of check bits to each byte or word of data. Upon reading from that location, the check bits will detect and correct all single-bit errors and will flag as impossible to correct all multibit errors. A board of standard TTL devices can implement such a system, as the second article in the series explains.

Both the Fire and the Hamming codes started out as purely mathematical models that were then adapted to hardware. The third article describes another such mathematical model that has not yet attained hardware form. It uses a highly inventive encoding scheme—the orchard code—that detects and corrects all single-bit errors and some multibit ones while appending only one check bit to each memory location. **-R. Colin Johnson**

Fire codes on custom chip clean up hard disk data

by Mohammad Maniar and Krishna Rallapalli
Advanced Micro Devices Inc., Sunnyvale, Calif.

☐ Although high recording densities enable modern disks to achieve very high data-transfer rates and storage capacity, they also increase the probability of errors. Moreover, defects in the recording media that were only a minor concern at lower recording densities can become a significant source of hard errors at higher densities.

The simple cyclic redundancy check [*Electronics*, March 27, 1980, p. 153] is adequate for detecting errors but far less so for correcting them. Modern disk systems use Fire codes (named after their originator, Philip Fire) for a superior method of error detection and correction.

The burst-error processor

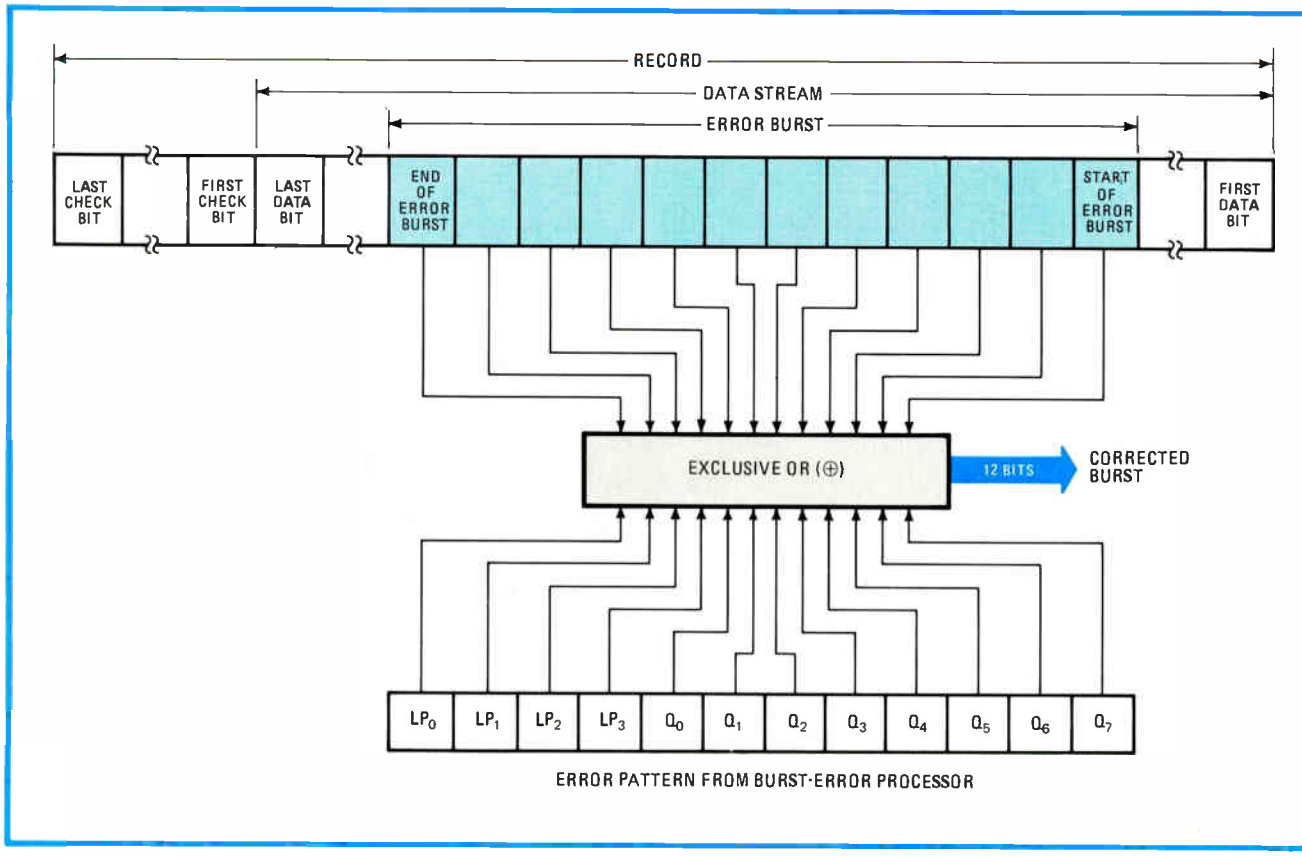
The AmZ8065 burst-error processor (BEP) is a new large-scale integrated MOS circuit that facilitates the hardware implementation of Fire codes in high-speed serial data-handling systems such as hard disks.

Each time a record, consisting of a number of data bits, is written onto the disk, a predetermined number of check bits (Fig. 1) is appended to it. When reading from the disk, the BEP recomputes the check bits and compares them with the ones that were read back to determine if there are any errors. Once the error location has been found, the 12-bit error pattern, also produced by the BEP, identifies the erroneous bit by a corresponding binary 1. To complete the correction process, the error-bit pattern is aligned with the record at the error location and a bit-by-bit exclusive-OR operation is performed to obtain corrected bits. It should be noted that both the maximum number of bits allowable in a record and the number of bits that can be corrected depend on which of the four Fire-code polynomials available on the BEP is used to compute the check bits.

Four functional units

The BEP has four major sections: a register array, a polynomial divide matrix, status logic, and control logic (Fig. 2). The register array consists of 56 flip-flops. The BEP computes check bits during write operations and what are called syndromes for detecting erroneous bits during read operations, and it extracts error patterns during error correction.

In general, the polynomial divide matrix provides the bit pattern the register array requires to form an 8-bit parallel feedback shift register (see "Fire code basics," p. 124). When the correction operations are complete, the error pattern is available on 12 outputs: 8 bits on the Q_0–Q_7 outputs and 4 on the LP_0–LP_3 outputs. The control logic generates the signals necessary for the register array. The status logic monitors the register arrays to



1. Error correction. An error burst can be corrected by an exclusive-OR with the error pattern obtained from the BEP. Each record written to disk has a fixed number of check bits appended to the data stream. Recalculation of the check bits during a read operation flags errors.

generate the error flags available on external pins.

The polynomial divide matrix is the heart of the BEP. The control logic decodes the polynomial-select (S_0–S_1) and function-select (C_0–C_2) inputs in order to generate the necessary gating signals to the matrix. The matrix establishes interconnections so that a byte of data presented on the D_0–D_7 inputs will be suitably divided by one of the four selected generator polynomials.

Modes of operation

The BEP is used in three distinctly different types of operations: write, read, and correct.

While data is being written on the disk, the BEP is in the mode in which it computes check bits, digesting the data bytes without affecting the flow of data to the disk. After the last data byte, the BEP is switched to writing the check bits, producing 4, 5, 6, or 7 check bytes. This additional information is appended to the data stream, enabling the subsequent detection and correction of possible read errors.

During check-bit computation, the polynomial divide matrix and the register array act as a feedback shift register. When the last data byte is entered, the register array holds the check bits. These check bits become available on the Q_0–Q_7 outputs, 1 byte at a time.

While information (data plus appended check bits) is being read, the BEP must be in one of two read modes: normal or high-speed. They differ only in the correction algorithm that will be used if an error has occurred. In both read modes, parallel bytes are read into the BEP, and after the last check byte has been entered, the error output indicates whether an error has occurred.

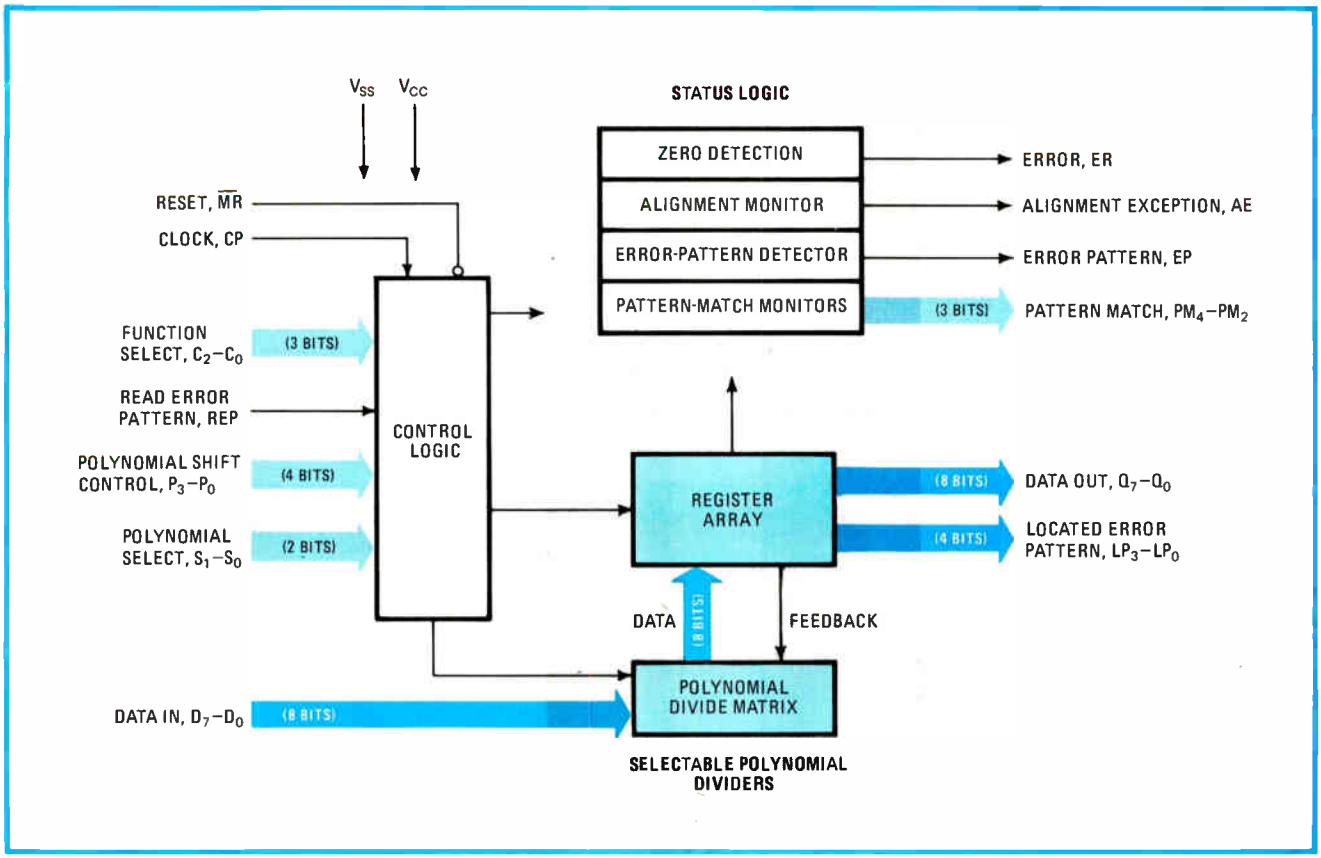
After the read operation, the syndrome held in the register array contains all the information necessary to find the location of the error and the error pattern needed to correct it.

The normal read function must be used for reading data from the disk if the normal method is used for error correction. (When high-speed error correction is in order, the high-speed read mode must be employed.) When normal read is selected, the polynomial divide matrix establishes the polynomial in the expanded form. In this mode, the input stream consisting of data and check bytes is divided by the selected polynomial to obtain the syndrome. If the resulting syndrome is not zero, an error is indicated by the ER output.

The syndrome obtained from normal read operations is manipulated to extract the error pattern and its location using the normal correct function. Of the four polynomials listed in the table, the 48-bit version requires a separate explanation. For all normal cases except the 48-bit version, the polynomial is established in the expanded form.

The normal mode

In the normal correction mode, the syndrome is repeatedly divided by the expanded polynomial until the error pattern is located. This division is accomplished by repeated clocking while ignoring the D_0–D_7 inputs. The error pattern (EP) output signals when the pattern has



2. Relationships. The polynomial divide matrix is the heart of the BEP. It supplies the bit patterns that the register array needs in order to compute check bits during a write operation, derive a syndrome during a read operation, and extract error patterns for error correction.

Fire-code basics

Error-detection and -correction codes are winning a lot of well-deserved attention nowadays. Among the most common are the Fire codes that enable errors to be corrected as well as detected. The burst-error processor, or BEP, is a hardware implementation of these codes that can correct bursts of errors up to 12 bits long in a data stream being read from a disk. It does so by dividing the data stream, a byte at a time, by a fixed binary number represented mathematically by a polynomial; for example, $x^0+x^2+x^5+x^7$ stands for a binary 10100101 since each exponent indicates the position of a 1.

Even though the data stream is being constantly divided as it passes through the BEP, the actual data is unaffected. However, at the end of the data transmission the internal registers of the BEP contain the remainder of the division. For write operations the remainder bits are appended to the data to produce a disk record. For read operations, the BEP continues to divide the check bits after the data has passed to obtain a bit pattern called the syndrome. For error-free operation, the syndrome should be 0. If it is not 0, it contains the information about the location of the error burst as well as about the position of the errors.

In the error-correction mode the BEP uses the syndrome to find first the error location and then the error pattern, which is exclusive-ORed with the error burst to correct it. The protocol for handling those errors is usually to load data from the disk directly into memory, on the assumption that it is error-free. When the BEP detects an error, it signals the host processor with an interrupt, after which it calculates the error location and the error pattern before sending them to the host, where the exclusive-OR operation is performed to correct the errors.

Remarkably, the error burst may be anywhere in the data stream and may be as long as 12 errors in a row. However, only one burst can be corrected—two or more bursts have to be flagged as uncorrectable.

Four different generator polynomials are provided as well, one of which is compatible with the internal standard of IBM Corp.'s disk controllers. **-R. Colin Johnson**

been found. The error pattern is always characterized by a known number of consecutive 0s in specified register array locations. The exact number of 0s and their location is a function of the selected polynomial. The status logic detects this unique combination to generate the error pattern output. The number of clock cycles needed to locate the pattern is a measure of its location.

If the number of clock cycles has exceeded the natural period of the selected polynomial—the maximum data stream length—without the error pattern having been found, then an error has occurred that cannot be corrected. Figure 3 explains the normal correction process.

In the normal mode of operation with the 48-bit polynomial, ordinary division is not practical because the polynomial's period is so long. In this case the polynomial divide matrix establishes the reciprocal of the expanded polynomial. Because of this, the syndrome obtained using the normal read mode with the 48-bit polynomial is not used directly for extracting the error pattern and calculating its location. Instead, the reciprocal of that syndrome must be used.

The reciprocal is formed externally by reading out the syndrome using the write-check-bits function and reversing all the syndrome bits so that the previously most significant bit becomes the least significant bit. The load function then loads the reciprocal syndrome into the BEP. Once the reciprocal syndrome is loaded, the normal correction function performs the correction. The maximum number of clock cycles needed to find the error pattern using the normal correction method is N where N is the period of the polynomial. Thus a polynomial with a large period may require a large number of clock cycles for error correction. This is not acceptable in some applications.

Chinese speed

For faster operation the BEP has facilities for high-speed correction using the Chinese remainder theorem method. The high-speed read function must be used for reading data if the Chinese remainder theorem is to be used for error correction. In general, the Chinese remainder method corrects errors in fewer clock cycles than the normal method. The only difference between the normal and high-speed read modes is that normally the input stream is divided by the expanded version of the polynomial, whereas in the high-speed mode, the

THE FOUR POLYNOMIALS USED FOR BURST-ERROR DETECTION AND CORRECTION

Generator polynomial	Number of check bits	Maximum data stream length (bits)	Maximum error burst length (bits)
$(X^{22}+1)(X^{11}+X^7+X^6+X+1)(X^{12}+X^{11}+\cdots+X^2+X+1)(X^{11}+X^9+X^7+X^6+X^5+X+1)$	56	585,442	11
$(X^{21}+1)(X^{11}+X^2+1)$	32	42,987	11
$(X^{23}+1)(X^{12}+X^{11}+X^8+X^7+X^3+X+1)$	35	94,185	12
$(X^{13}+1)(X^{35}+X^{23}+X^8+X^2+1)$	48	$13\cdot(2^{35}-1)$ (>446,667 Mb)	7

input stream is divided simultaneously by all factors of the polynomial. Thus, the high-speed mode results in as many syndromes as the number of factors of the polynomial, and all syndromes must be zero to indicate error-free operation.

This is done by dividing the register array into sections so that as many syndromes as the number of sections are produced, each section implementing one factor of the polynomial. This allows each factor to be divided separately, but in parallel—simultaneously—with the others.

When an error is detected, the Chinese remainder theorem method requires the syndrome obtained by the error-pattern polynomial to be repeatedly divided until the error pattern is found. After locating the error pattern, the error-pattern register is prevented from further clocking. Next, the register corresponding to the second factor is repeatedly clocked until it matches the error pattern, and then this register is prevented from further clocking. This procedure is repeated for all of the remaining factors until the error pattern is found for each section.

The P_0–P_3 inputs are provided in the BEP to control clocking of the individual registers, and the PM_2–PM_4 outputs are provided to indicate matching of each register with the error pattern. Also just as in the normal method, every error detected by the BEP may not necessarily be correctable. If the number of clock cycles to find the error pattern exceeds the period of the error-pattern polynomial, or if the number of clock cycles required to match a register exceeds the period of the polynomial corresponding to that register, the correction process must be aborted. The Chinese remainder method is slightly more complicated to use, but it can often result in a much faster correction process.

Successful conclusion

The AmZ8065 places the error pattern on 12 outputs—8 bits on the Q_0–Q_7 outputs and 4 bits on the LP_0–LP_3 outputs. The calculated error location is such that when 12 consecutive bits of the record are exclusive-ORed into the error pattern, the entire error burst is corrected. □

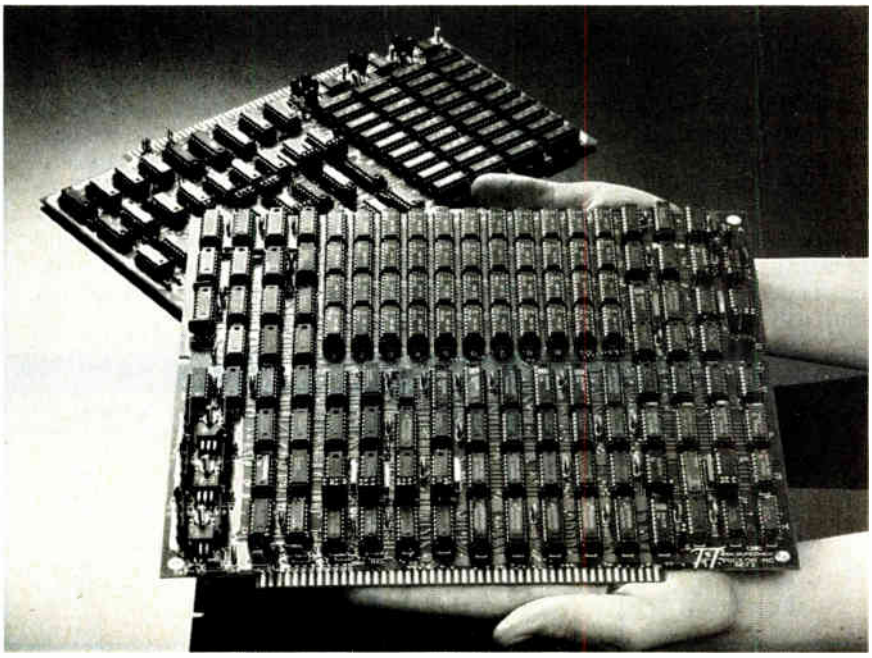
Board applies Hamming codes to small-computer memory

by Harry Masuda
Piiceon Inc., San Jose, Calif.

□ Finding and fixing intermittent errors in memory—most often changes of single bits that go unrecognized as they occur—is the remedy for many costly operational and service problems. These soft errors increase as memory chips become denser, so error-checking and -correcting (ECC) techniques like Hamming codes have become as essential in small computer systems as they are in large ones.

A dynamic random-access memory board that incorporates Hamming code error detection and correction dramatically increases mean time between failures from a typical 1,000 hours to 300,000 hours. The Piiceon 64-K-byte Supermem ECC 3 board (Fig. 1), with its built-in ECC circuits, is one of the first devices designed to be compatible with the S-100/IEEE-696 standard bus; it will find applications in both 8-bit and 16-bit microcomputer systems.

Supermem's ECC circuits can find and correct single-bit errors and detect double-bit errors on the fly. The board operates with microprocessors at clock rates of up to 3 megahertz and is 300 times more reliable than



1. Reliable. The Piiceon 64-K-byte Supermem ECC 3 for small computers based on the S-100 bus uses Hamming code error checking and correction. This dynamic random-access memory board is 300 times more reliable than dynamic memories without error correction.

dynamic memories without ECC. Though its initial cost is higher than that of other dynamic RAMs, it can thus be less expensive in the long run.

From a price-performance standpoint, the board is comparable to a 64-K-byte static memory. But designers who have turned to static RAM boards to enhance reliability can improve their mean time between failures even over that of the static devices by using the Supermem ECC 3.

Memory error—a nemesis

Undetected errors in digital systems create havoc and costly repairs. If a single bit in a memory array changes, the central processing unit has no way of knowing that it has occurred and continues with its task. Regardless of what is stored in memory—operating code, operand, or data—the CPU processes the bit as if it were correct. If the incorrect bit is then stored on a disk file, and this is most likely, it may be two or three weeks before the error surfaces for the first time. At that point there is probably no way of knowing if the error is in the printer, the disk, the CPU, or the memory.

A frequent cause of memory errors is power-line disturbance. In dynamic RAM systems, refreshing usually occurs at least every 2 milliseconds. If power supply voltage fluctuates even slightly, it may disturb data cells in a RAM or easily trigger a signal or gate, inhibiting essential refreshing.

The board facts

The board, 10 inches wide by 9 in. high in accordance with the new IEEE-696 standard for the S-100 bus (see "The S-100 bus—an update," below) is a double-height version of the more commonly encountered 5-by-10-in. S-100 board. It has an array of 16-K dynamic RAMs that maximize bit density, minimize power dissipation, and also optimize the price-performance ratio. A memory relocation feature allows any 16-K bank of memory to be relocated to any 16-K boundary within the 64-K address field. Should a memory bank develop a double-bit error, it may be turned off and 48 K of contiguous memory supplied.

The extended address capability gives a full 24-bit address space for direct addressing of 16 megabytes. This serves the newer microprocessors such as the Z8000, the 68000, and the 8086.

The S-100 bus—an update

It's now six years since Ed Roberts sired the S-100 bus (originally called the Altair bus) for use in the Altair 8800, a computer kit manufactured by his company, Micro Instrumentation and Telemetry Systems (MITS). Along with the Altair 8800 came S-100–compatible peripheral plug-in boards. By the end of 1976, there were more than half a dozen companies building S-100–compatible mainframes and close to 30 suppliers of compatible plug-in boards. By the year's end, 30,000 S-100–based systems had been sold, and MITS began redirecting its efforts toward commercial and business users.

But the company was subsequently acquired in 1977 by Pertec Computer Corp., Los Angeles, which in turn was acquired by Triumph Adler Inc. of West Germany. Though the S-100–compatible market continued to mushroom—over 60,000 systems were sold in 1977—the Altair system itself was soon eclipsed by competitors.

In 1978, nearly 100,000 S-100 systems were made. By 1979, there were 17 makers of S-100 mainframes. Some 60 companies supplied plug-in boards and over 140 offered S-100 software packages, making computer systems using the bus among the most widespread. Today S-100 users can select from among at least seven 8-bit central processing units and five 16-bit CPU boards.

As sales of both S-100 mainframes and peripheral plug-in boards boomed, it became apparent that the bus needed tighter specifications. The 19 undefined pins as well as other redesign factors had to be addressed. This was due to the arrival of the new 16-bit microprocessors, which expanded system capabilities with features such as multiprocessing, higher-speed operation, and enhanced interrupt vectoring. So in mid-1978 several companies began developing, under the aegis of the Institute of Electrical and Electronics Engineers, what is now known as the IEEE-696 standard (see table).

In the past, some so-called S-100–compatible boards worked with some S-100 systems but not with others—a problem the new IEEE-696 standard should eliminate. Its principal stated objective is "to define a rational, general-purpose interface system for designers of new computer system components that will ensure their compatibility with present and future S-100 computer systems."

When the S-100 bus was first conceived, no one envisioned either expanding direct memory addressing beyond 64-K bytes or putting multiprocessors on the bus. The IEEE-696 standard defines these powerful applications. Memory addressing is expanded to 16 megabytes and input/output addressing to 64,000 ports. The vectored interrupt system is also expanded to 11 inputs and will provide for up to 16 masters on the bus. What's more, the 8- and 16-bit data transfer will enable both 8-bit and 16-bit masters to coexist in a single system.

A COMPARISON OF SPECIFICATIONS FOR THE S-100 BUS AND THE IEEE-696 STANDARD

Bus type	Address bus	Data bus	Interrupt structure	Master	Board size
S-100 bus	16-bit (64-K bytes)	dual 8-bit (8 in and 8 out)	none	single	single height (5 by 10 in.)
IEEE-696 standard	24-bit (16 megabytes)	16-bit (8 in and 8 out or 16 in and 16 out)	vector interrupt; bus arbitration scheme	multiple (up to 16)	single and double height (9 by 10 in.)

TABLE 1: FORMING ERROR-CORRECTION CODE IN THE SUPERMEM ECC BOARD

A: Forming data subgroups

Bit position	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
Typical word	0	1	1	0	1	0	1	1	0	1	1	0	1	1	1	0
Data subgroup																
1		X	X	X	X	X	X		X							X
2	X	X		X		X		X		X		X		X		
3			X	X			X	X			X	X			X	X
4	X				X	X	X	X					X	X	X	
5									X	X	X	X	X	X	X	X
6	X	X	X		X				X	X	X		X			

B: Data subgroup and check bit for a typical word

Data subgroup	Selected bit combinations								Check bit
1	1	1	0	1	0	1	0	0	0
2	0	1	0	0	1	1	0	1	0
3	1	0	1	1	1	0	1	0	1
4	0	1	0	1	1	1	1	1	0
5	0	1	1	0	1	1	1	0	1
6	0	1	1	1	0	1	1	1	0

For systems using Z80-based microcomputer systems, bank selection lets the user switch 16-K memory banks one at a time. Though software-intensive, this technique enables users to address banks of 64-K memory sequentially. These can be turned on and off with hardware switches or with software commands to the input/output ports.

Bank selection is often desirable for memory management applications. Banks can be assigned to either specific users or specific tasks. Each memory bank can be enabled or disabled via jumpers. A phantom-enable signal can disable one of the banks (depending on the jump configuration) during power-up.

The Supermem can be used in systems employing either 8- or 16-bit word lengths. Though the 16-bit data-transfer network always operates in a 16-bit mode, it can serve either as a bidirectional 16-bit I/O network or as a combination 8-bit input circuit and 8-bit output circuit. The on-board refresh logic makes the refreshing cycles transparent to the processor.

All operations are performed as if they were read/modify/write operations. During a write, data from the processor is written into the memory unaltered. During a read, data is read from memory and corrected if single-bit errors are detected. The resulting data is then fed to the processor and rewritten into memory.

Before ECC, systems used bit-per-byte parity to check for errors. That is, a parity bit was required for each byte of memory. If a bit was dropped or added, this technique could detect that a byte was in error but could not locate the bit responsible.

ECC bits used according to the Hamming technique [*Electronics*, Nov. 22, 1979, p. 103] are generated in the Supermem board over the entire word (in the 16-bit system) or over two separate 8-bit bytes.

Keeping track of changes

If a data bit should change between the time it is stored in memory and the time it is read out of memory, the parity of 1 or more of the bytes containing the erroneous bit will change.

Comparing the stored ECC bits with the ECC bits generated by using the data read from memory will indicate which data bit was changed. The bit is then corrected by inverting it.

When the data and ECC bits are reread from memory, 6 new ECC bits based upon the data actually read from memory are generated and compared with the old ECC bits read from memory.

Before writing each 16-bit word, a sequence of 6 check bits is generated, as illustrated in Table 1. As shown at top, data subgroup 1 comprises bit positions D_1–D_6, D_8,

TABLE 2: NO-ERROR AND DOUBLE-BIT-ERROR LINE STATES

	$\overline{\text{NO ERR}}$	$\overline{\text{DBE}}$
No error	0	0
Single-bit error	1	1
Double-bit error	1	0

and D_{15}; data subgroup 2 uses bits D_0, D_1, D_3, D_5, D_7, D_9, D_{11}, D_{13}, and so on. The actual bits that would be generated for a typical word are shown at the bottom of the table. One check bit is generated for each subgroup, as shown in the table's right-hand column.

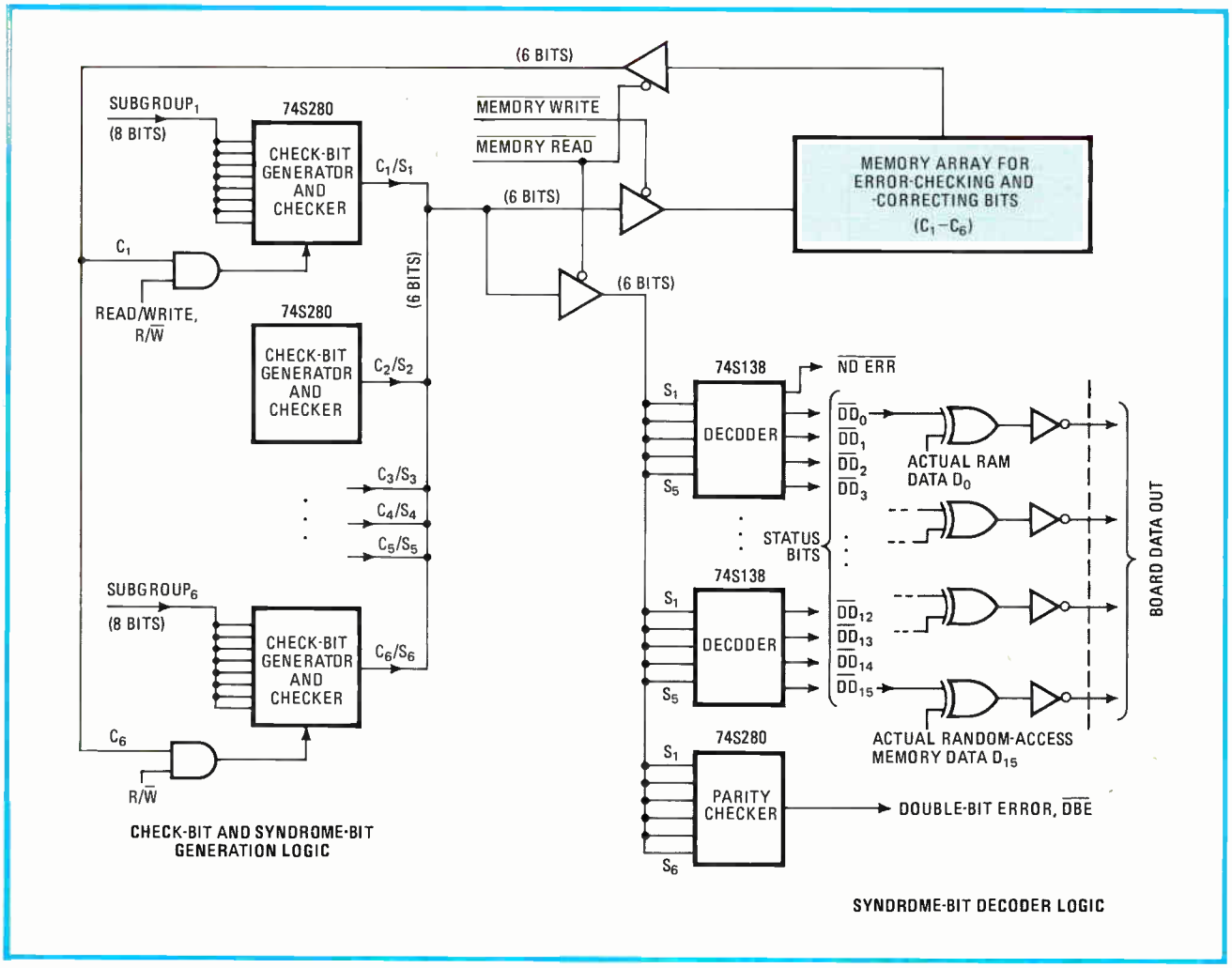
Hardware implementation of the check-bit generation is shown in the simplified schematic in Fig. 2. During memory write, each of the read/write lines is in the write mode, inhibiting the feedback lines. Each subgroup is fed to a 74S280 parity-checker integrated circuit. These devices generate the check bits C_1–C_6, which are then stored in the ECC bit memory array.

At each reading of memory the subgroups are again recomputed in the 74S280s and check bits are generated. However, this time the gates are in the read mode, and the check bits generated during write and stored in the ECC bit memory are fed to the 74S280s, to be added to the newly computed check bit. The 74S280s generate syndrome bits that are fed to the 74S138 decoders.

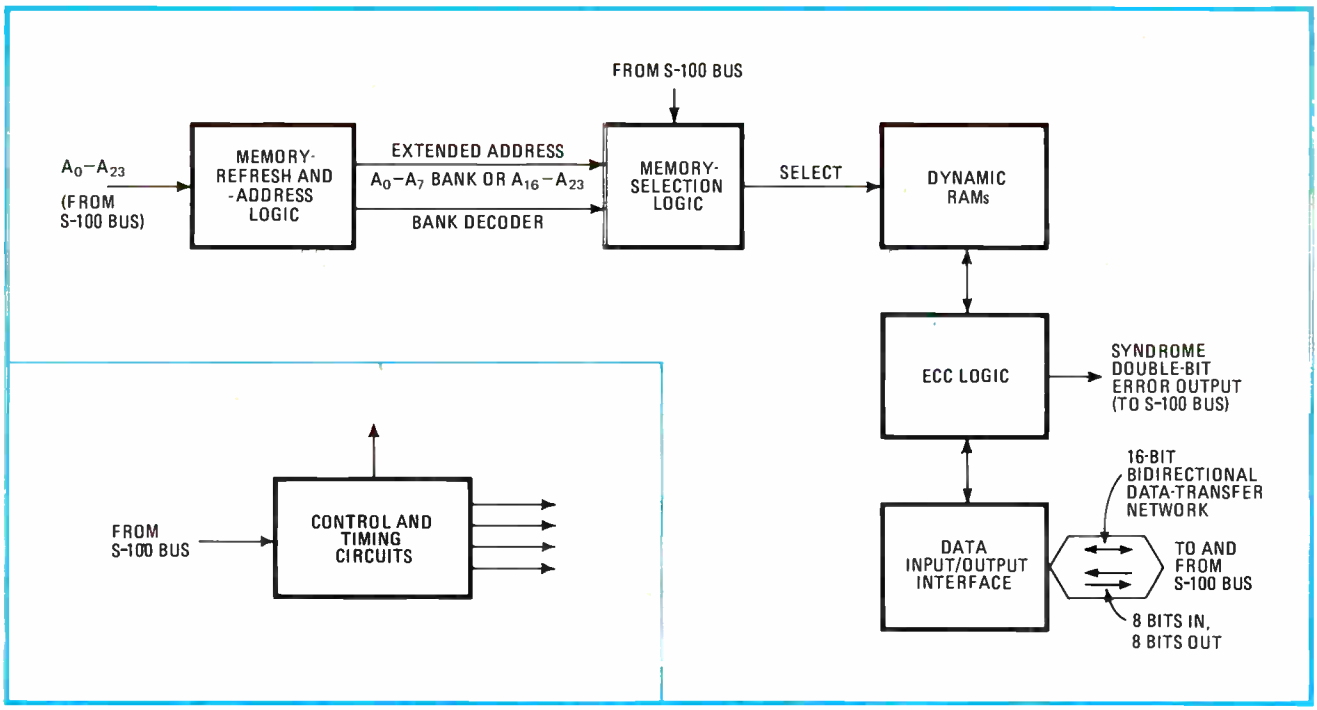
The 74S138s decode as shown in the upper half of Table 1 and thereby convert the syndrome bits into status bits. Consequently, if syndrome bits are true for subgroups 2, 4, and 6, this indicates that D_0 is incorrect and therefore would drive $\overline{D}_0$ low. Likewise subgroups 1, 2, and 6 would drive $\overline{D}_1$ low, and so forth.

With a single-bit error, these decoders develop an error signal ($\overline{\text{NO ERR}}$ goes high). Also one of status bits $\overline{DD}_0$–$\overline{DD}_{15}$ goes low, designating the invalid bit. This status bit, along with the original bit stored in RAM, drives an exclusive-OR gate in cascade with an inverter to correct the error. If there is no error, the bit stored in RAM is transmitted through the exclusive-OR and inverter combination unchanged.

In the case of a double-bit error, the $\overline{\text{NO ERR}}$ signal is driven high. Two of the syndrome bits are also driven high, driving the $\overline{\text{DBE}}$ double-bit error line low. The signal that is generated in this way notes the occurrence of a double-bit error. The various states for the $\overline{\text{NO ERR}}$



2. Catching errors. Several 74S280 parity checking and 74S138 decoding integrated circuits form the logic for check-bit and syndrome-bit generation. The ICs also form the syndrome-bit decoder logic modules that chase and catch errors in the dynamic RAM modules.



3. Precision control. The control and timing circuit module contains circuitry for exact timing of the memory and of ECC functions such as the ECC logic detailed in Fig. 2. The memory refresh and address logic and the memory selection logic address and refresh the RAMs.

and $\overline{DBE}$ lines are given in Table 2.

The control and timing circuits shown in the Supermem board block diagram in Fig. 3 ensure sequencing and proper timing of memory board functions. A 200-nanosecond delay line and various gates perform the highly reliable and exact timing, giving greater system margins than are possible with other methods. The memory refresh and address logic plays two roles: it interfaces with the memory address lines on the S-100 bus and generates refresh addresses for the dynamic RAM devices. The memory selection logic chooses the appropriate memory portion for the current operation, depending on whether the processor is addressing the memory in bank mode or extended address mode. The data I/O interface, via the ECC logic, connects the RAM to the S-100 bus. The ECC logic contains the error-detection and -correction circuits. The dynamic RAMs store both data and the check bits to test memory content validity during each read cycle. Data I/O is handled by a 16-bit data-transfer network. This circuit has been designed to handle data transfers in both 8-bit and 16-bit systems.

In the same order

Sequences of events are essentially the same in read, write, and refresh. First, the memory address is applied to the memory and refresh logic (A_0– A_{23}). The address selection (read, write, or refresh) is clocked to initiate the timing circuit on the active board. A row address is then fed to the RAMs.

In the refresh mode, the selected bit row of all RAMs is refreshed. This completes the refresh cycle.

In both the read and write modes, delay initiation is followed by a column address strobed into the memory-selection logic. Then data is read from memory and, if necessary, corrected by the ECC logic. The syndrome bits and error bank number are stored in on-board latches for later reading by the CPU.

In the write mode, ECC check bits are generated for storage with the data. Then data and check bits are written into memory.

Addressing memory

Each 64-K-byte Supermem board is divided into four banks of 16-K bytes each, called A, B, C, and D. The memory can be addressed in either the bank mode or the extended address mode. In the bank mode 16 address lines are used. However, the first 8 (A_0–A_7) are time-shared to make, in effect, 24 address lines. Lines A_0–A_7 are compared with the eight address-decode jumpers in the memory selection logic (Fig. 3). If all 8 bits have a one-on-one correspondence, the board is identified as active and is used to set up the bank register based on data bits 0 through 3.

Now bits A_0–A_{15} are utilized. Bits A_{14} and A_{15} select the correct memory bank. The selected outputs (0 through 3 on each encoder) show that memory in the desired address range has been installed and that that bank will then be selected. At this point bits 0 through 6 select the row and 7 through 13 select the column address in each RAM.

In the bank mode, the hardware jumper settings can be changed by software. An I/O port latch is set up so that D_0–D_3 (corresponding to banks A–D) form a bank-enable register that is used for this purpose.

In the extended address mode, a full 24 address lines are used. The contents of A_{16}–A_{23} are compared with the address set by the eight address-decode jumpers. As in the bank mode, if all 8 bits match one on one, the card is selected. Bank and bit selection are done the same way as in the bank mode. □

One check bit per word can correct multibit errors

by Ed Scott and Dan Goetschel
Analytical Engine Works, Glendale, Calif.

☐ The ability to guarantee information integrity has been a major goal since the early days of data communications, and various coding systems have been devised for detecting and correcting erroneous bits. For the most part, however, these have paid for performance with proportionately high bit redundancy—and a proportional decrease in data throughput.

A new method, called the orchard scheme, raises error-correction and -detection performance with a minimum increase in bit redundancy. Using multiple vectors through the data, whether in serial or parallel form, the orchard method approaches a redundancy rate of 1 check bit per word by combining the encoding of multiple vectors through the data into that correction bit.

The orchard system, with patent pending and available for licensing, offers better capabilities than conventional parity schemes, which only detect errors, yet has only slightly greater redundancy. It is also impressive when compared with more sophisticated coding systems. The table shows such a comparison for a block of 32 successive data words, each consisting of 8 data bits (the number of words and bits is arbitrarily chosen for the sake of comparison).

As the table shows, conventional blocking code is the only other correction system to approach orchard's redundancy rate, but it trails in correction and detection capabilities. Hamming and redundancy codes about equal orchard in performance, but both require a significant increase in additional bits. Of all the listed methods, only orchard can always detect multiple errors and correct double errors for the 32-data-word blocks. Using other block and word sizes may yield different quantitative results but the trends remain the same.

The orchard scheme is useful for digital information storage systems such as floppy disks, hard disks, eight-track tapes, and bubble memories. And systems that use parity checking—the most common procedure—can easily be adapted to orchard, since both systems add only 1 correction bit per data word and allow continuous data flow. Data-communication modems and other equipment for transmitting video information and measurement data can also benefit from the new code. Though orchard does have a slightly slower throughput than conventional parity, this is not really a significant disadvantage since most current transmission and storage methods have a still slower throughput.

ORCHARD CODING COMPARED WITH COMMON ERROR-DETECTION AND -CORRECTION SCHEMES

Coding scheme	Errors detected			Errors corrected			Redundant bits required per word
	1	2	many	1	2	many	
Repetition	y	y	u	y	u	u	16
Parity	y	u	u	–	–	–	1
Blocking	y	y	u	y	–	–	1.3
Hamming	y	y	u	y	u	m	5
Orchard	y	y	y	y	y	m	1

Note: comparison made using 32 successive 8-bit words
y = yes u = usually m = maybe

Pick a tree

The original conception of orchard error correction came from the visual perspective a person would have passing by the equidistant rows of, for example, an apple orchard. A single tree can first be observed as the viewer looks into the orchard at a 45° angle. The tree can be seen farther along by looking perpendicularly into the orchard. After another short distance, it is seen again by looking back into the orchard at a 135° angle. Thus, any tree in the interior can be located by describing the location of just two trees at the edge of the orchard that lie in the same vectors as the interior tree.

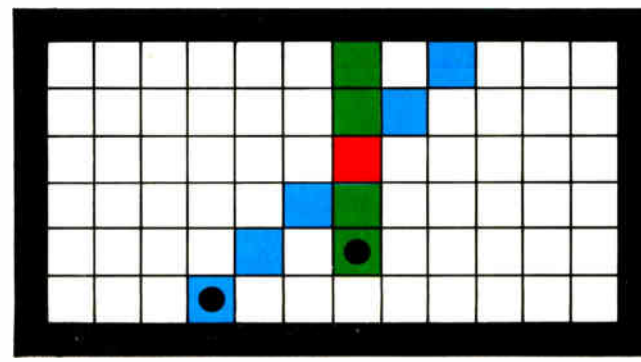
In a similar manner, the orchard scheme uses 1 parity bit per word to represent the modulus-2 or exclusive-OR sum of several vectors through a data path. Here all the vectors are thought of as having a straight-line construction, but the pattern does not have to exhibit any such regularity.

A hardware implementation of orchard error correction may be more practical in commercial applications, but software routines have been written also. Routines written in assembly language or even in Fortran, Pascal, or C can run quickly enough for many applications.

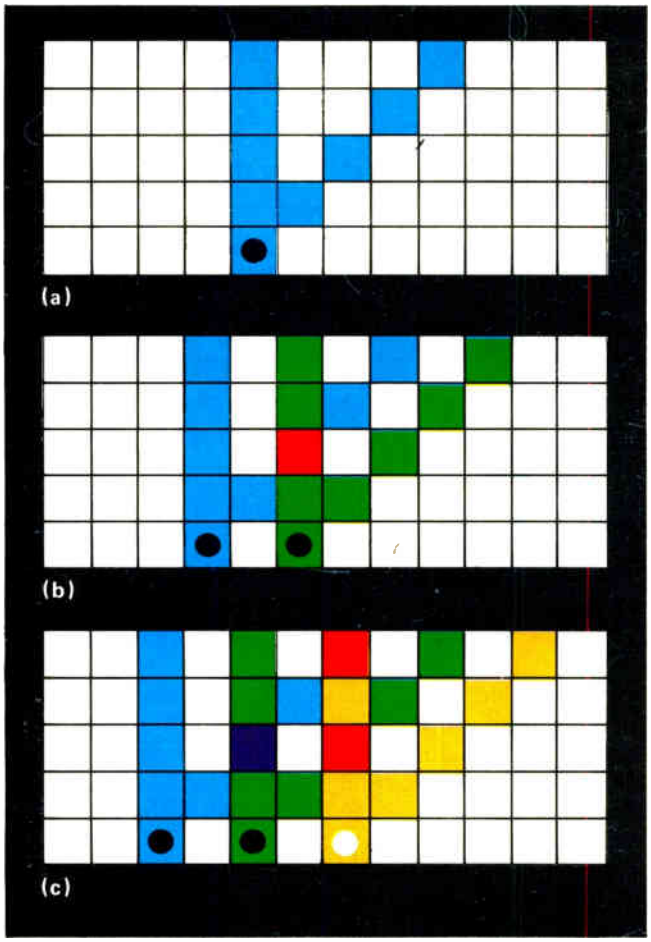
Before orchard

The orchard concept evolved from earlier coding schemes. Conventional parity systems, with their 1 extra error-detection bit per digital word, detect odd numbers of errors within that word. Even numbers of errors go undetected. Such systems are commonly used and are adequate for most simple systems, which do not require perfect transmissions.

If the data is transmitted in a parallel rather than serial format, the addition of a parity word after a



1. Better than parity. In this correction system, one parity bit (black dot) is used to represent a conventional parity row (green) and another parity bit shows a diagonal parity vector (blue). The conjunction of the two vectors uniquely locates a data bit in error (red).



2. Simple. In pattern (a), 1 correction bit represents a conventional parity row and a diagonal parity vector to locate single errors. A bit in error can be located by 2 flagged orchard bits (b). For multiple errors (c), this scheme produces additional errors.

specified parallel word length allows single errors to be uniquely located and corrected. The parallel word length, in this case, is the number of data words bounded by the leading and trailing edges of the parity word. This system is commonly known as a blocking code. Each error is uniquely located by 1 column parity bit and 1 row parity bit in the rectangular bit array.

Blocking can detect most multiple errors but cannot correct them since no more than one error per block can be uniquely located. Reducing the block size increases the correction rate but also the redundancy rate. Another disadvantage of blocking is that continuous data flow is not possible—the messages must be broken up into segments so that a column parity word can be appended.

In one elaboration of simple parity and block codes, 2 parity bits are appended to each data word, as shown in the rectangular bit array of Fig. 1. The first of these is a conventional row (green) parity bit. The other represents a diagonal vector (blue) through the data path. Thus, an error (red) is located by 1 conventional row parity bit and 1 diagonal vector parity bit. This allows continuous bidirectional data flow with considerably improved correction capabilities.

With this approach, however, a problem arises whenever an even number of errors occurs in either the conventional parity row or in the diagonal parity vector. This prevents correction since no parity bit discrepancy occurs for that row or vector. Another disadvantage is that this method requires 2 parity bits per data word, which increases the redundancy rate.

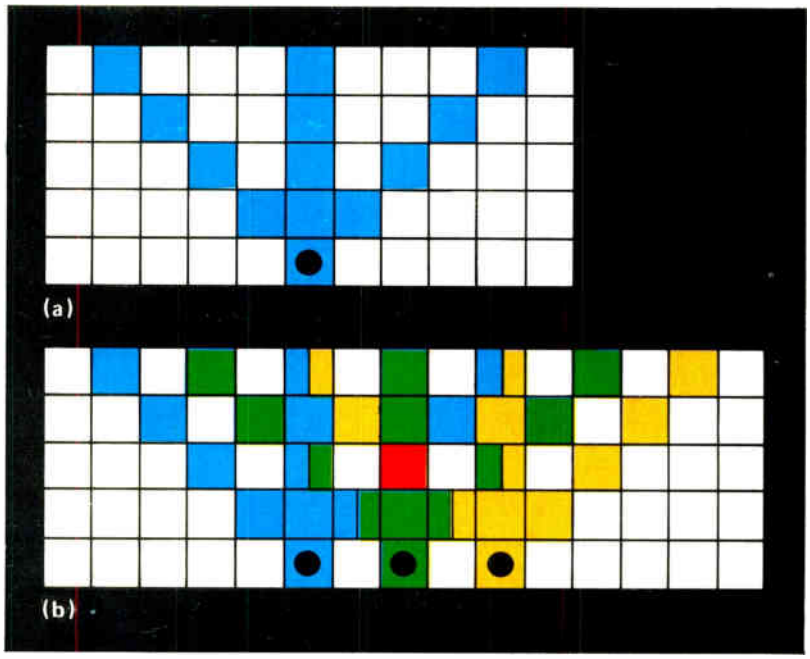
Making the most of 1 bit

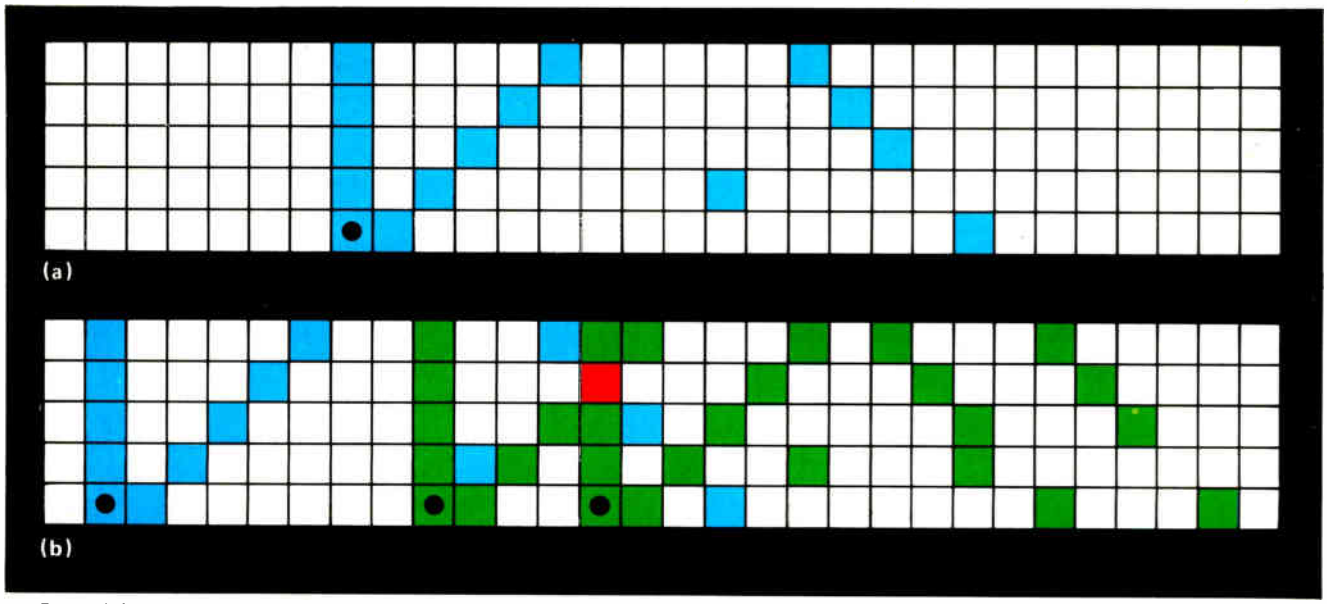
With orchard, 1 correction bit represents two or more vectors through the data path, so a simple orchard pattern can correct all single errors (Fig. 2a). Here, 1 bit represents both a conventional parity row and a diagonal parity vector. In addition, an erroneous bit is easily located by 2 flagged orchard bits (Fig. 2b). In this figure, the red space is a bit that is uniquely located by the conjunction of the green conventional row and the blue diagonal vector.

Such simple orchard patterns are useful as illustrations, but they run into serious problems when multiple errors occur. For example, as seen in Fig. 2c, the two red spaces are the actual bits in error. These errors occur in the diagonals of the blue and green orchard patterns, and the black-dotted orchard bits are flagged. They also occur in the yellow pattern, but since there happens to be an even multiple of errors in this pattern, the orchard bit is not flagged.

A correction system structured as in the previous paragraph would mistakenly correct the violet space,

3. More. Adding another vector to the pattern in Fig. 2a yields significantly better detection and correction capabilities (a). In (b) an erroneous bit (red) shows up in the leading diagonal vector of the blue pattern and two other places.





4. Powerful. This pattern always corrects single- and double-bit errors, frequently corrects higher multiples of errors, and always detects higher multiples of uncorrectable errors (a). In (b), a bit in error (red) shows up in the first vector of the blue pattern and in two other places.

leaving the two real errors uncorrected. Such a system could actually increase the number of errors in a digital message without notifying the host system of the existence of uncorrectable errors.

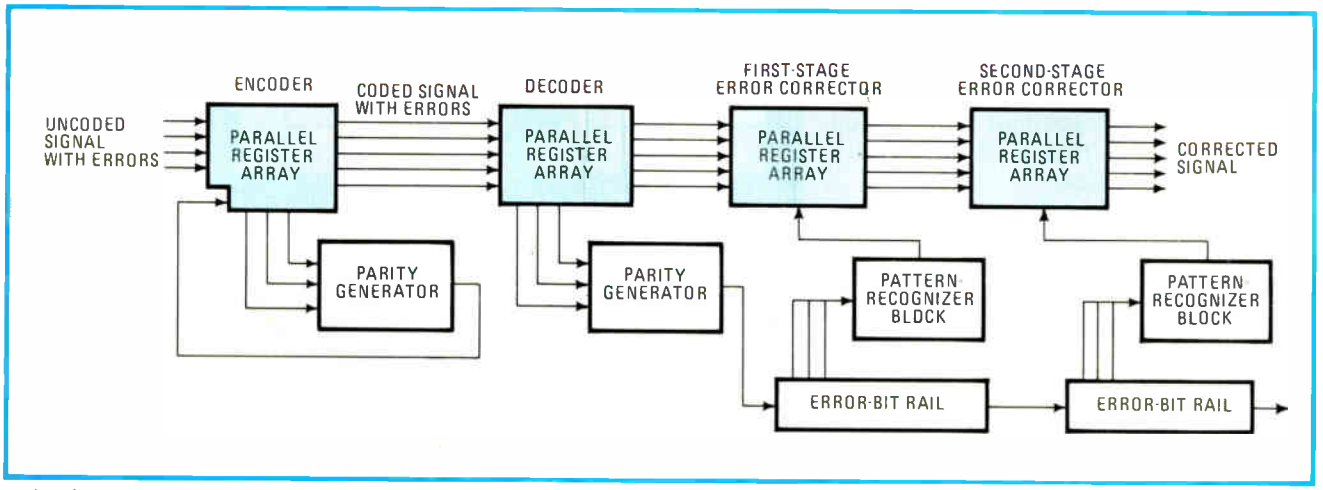
Fortunately, an orchard pattern in which each orchard bit encodes the parity for three or more vectors through the data can very nearly eliminate the chance of increasing the error rate. In one such three-vector pattern (Fig. 3a), an error will flag 3 orchard bits (Fig. 3b). Here the multicolored squares represent overlapping patterns. This orchard pattern will not create new errors, though there are several rare combinations of double errors that flag the same orchard bits. This ambiguity makes it impossible to correct these double-bit errors.

But the vector orchard pattern can be further improved to the point where it can correct all double-bit errors, correct many higher multiples of errors, and detect all higher multiples of errors that occur within the parallel word distance (Fig. 4a).

In Fig. 4b, the conjunction of the three orchard bit patterns (blue, green, and yellow) uniquely locates a bit in error (red). In fact, a single error will always flag 3 orchard bits. Some double errors may cancel out an orchard bit and thus result in only 2 orchard bits being flagged per bit in error. But this is not really a problem: the pattern is always chosen so that the column spacing between any 2 encoded bits is unique, with unique spacing between flagged orchard bits, so correction is still possible if only 2 orchard bits remain uncanceled. An additional feature of the pattern is the encoding of the correction bits. This allows correction of erroneous orchard bits and prevents them from being mistaken for data-bit errors.

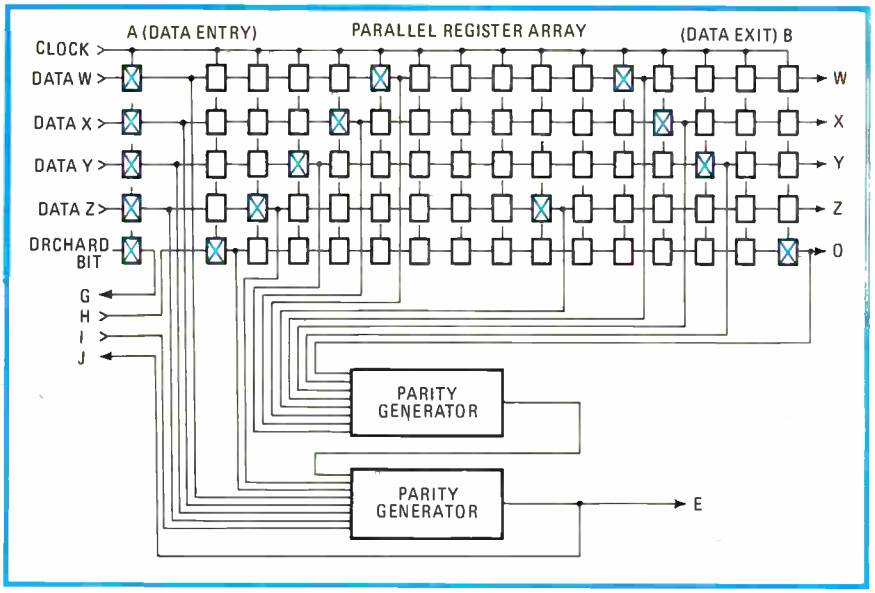
Implementation is easy

In a typical three-vector orchard pattern generator, the encoder consists of a parallel register array and a parity generator (Fig. 5). The parity generator's output is fed back to the register array to form the orchard bit. The decoder is similar to the encoder except that the



5. Implementation. The circuit shown is one possible design for the encoder, decoder, and corrector stages for the orchard pattern in Fig. 4a. It can be built with discrete components or as an LSI device. It is also possible to implement the orchard scheme in software.

6. Dual functions. The circuit shown can either encode or decode the orchard pattern shown in Fig. 4a, depending on how it is connected. It can also be used for other orchard patterns as required by the circuit designer.



incoming parallel message already has an orchard bit and the output of the parity generator is fed to the first corrector-stage error-bit rail, or connection bus. The first corrector stage consists of a parallel register array, an error-bit rail, and a pattern-recognizer block. The pattern recognizer circuitry is the primary element that changes in subsequent corrector stages.

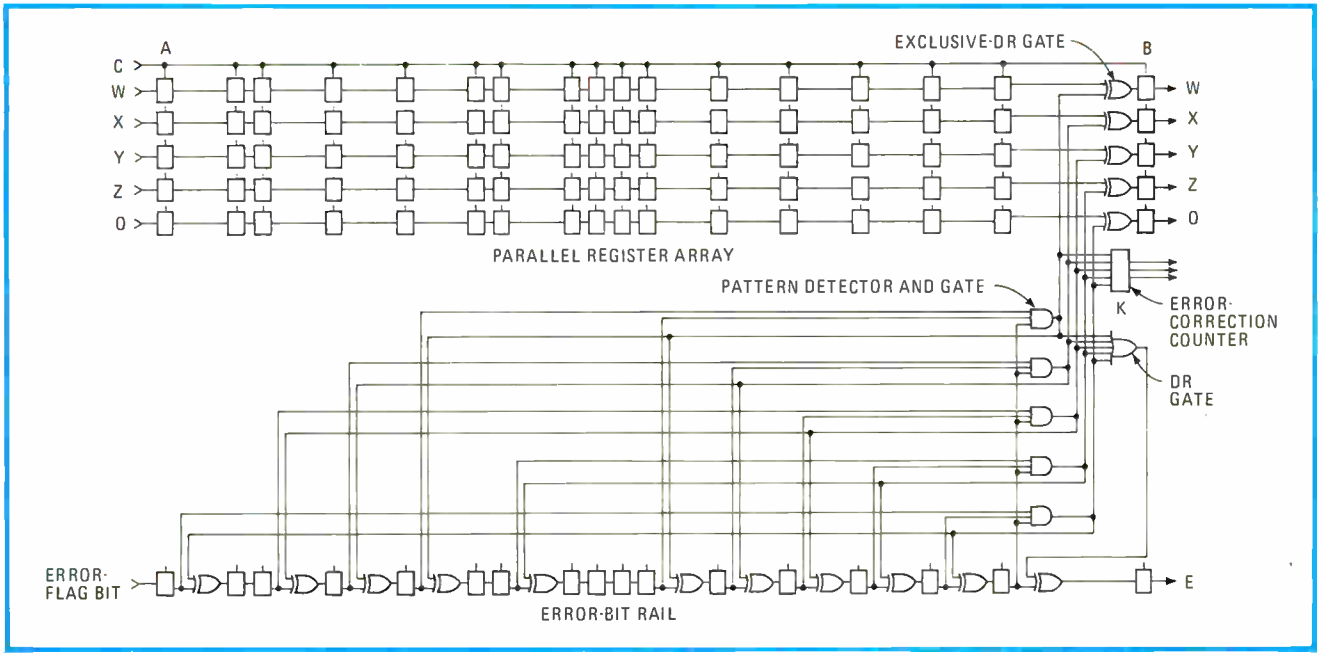
More than three

Orchard patterns with more than three vectors through the data are also possible. For example, an n vector orchard pattern would have $(n-1)$ corrector stages. The first corrector stage would correct all errors that flagged n error bits into the error-bit rail. Each succeeding corrector stage would correct errors that flagged 1 fewer error bit into the error-bit rail than the previous stage. The final corrector stage would correct all errors that flagged 2 error bits into the error-bit rail.

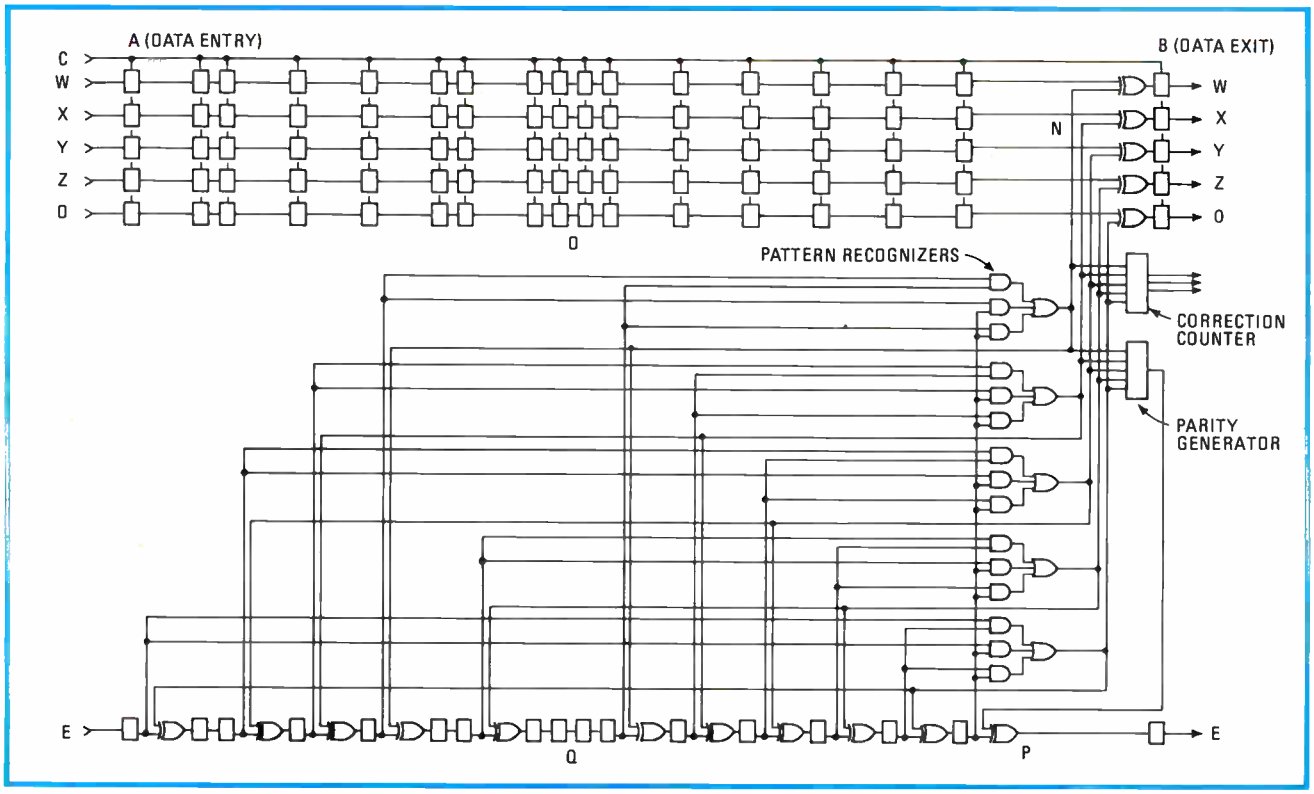
An encoder or decoder circuit can be easily constructed from TTL integrated circuits. Such a circuit will either encode or decode the pattern, depending on how it is connected (Fig. 6). Even parity and active-high logic, though not necessary, are used for clarity in this design.

The circuit contains a parallel register array consisting of D-type master-slave flip-flops. In the drawing, the bits being encoded or decoded are represented by the Xs in some of the flip-flops. A clock signal steps the data and orchard bits through the array. The width of the register array is 1 data word (WXYZ) plus 1 orchard bit. The array must be long enough to contain the orchard pattern used or, in this case, 16 parallel words.

Standard parity-generator integrated circuits are used



7. Corrections, please. This first corrector stage for the pattern in Fig. 4a corrects errors that have flagged 3 bits into the error-bit rail. The TTL logic is straightforward. Operation of this circuit can be understood by following a set of data and orchard bits through the registers.



8. Another corrector. All multiple errors that have flagged only 2 bits into the error-bit rail are corrected in the pattern's second corrector stage. Other implementations are possible for this and the other circuits shown depending on the logic family the designer favors.

to determine the modulus-2 or exclusive-OR sum of the orchard pattern bits. In the encoder mode the modulus-2 sum is fed back into the orchard bit row by connecting terminal J to H and I to ground (Fig. 6). G is not connected, as the first orchard bit flip-flop is not needed in the encoder mode. A 4-bit data word (WXYZ) enters the parallel register array at A, and a 5-bit word (WXYZ0), consisting of 4 data bits and 1 orchard bit, leaves the array at B. The orchard bit is set to either a 1 or a 0 to make the total number of 1s within the orchard pattern even.

In the decoder mode, the modulus-2 sum is fed out to the error-bit rail of a corrector circuit at E (Fig. 7). To do this, G, H, and I are connected and J is not used (Fig. 5). In the corrector circuit, a 5-bit word consisting of 4 data bits and a previously encoded orchard bit enters the parallel register array at A. A 5-bit word leaves the array at B along with a bit from an error-bit rail at E. Whenever an odd number of 1s is found within the orchard pattern bits, an error has occurred, and a 1 is flagged into the error-bit rail. The corrector circuit uses the pattern of 1s flagged into the error-bit rail to invert any erroneous bits.

Corrector circuits

Figure 7 is a first-stage error corrector for the orchard pattern presented in Fig. 4a. A data word plus an orchard bit (WXYZ0) enters the parallel register array, and at the same time an error flag bit enters the error-bit rail. The latches of the parallel register array and the latches of the error-bit rail have been drawn in Fig. 7 so that they are horizontally aligned. This indicates their time correspondance. The same clock signal that was used with the decoder steps the latches of the data array and the error-bit rail.

When a pattern detector AND gate detects a 3-bit pattern in the error-bit rail, it activates the appropriate exclusive-OR gate to correct the erroneous bit associated with that pattern. It also corrects flag bits in the error-bit rail by driving the exclusive-OR gates associated with the error-flag bits. The last exclusive-OR gate in the error-bit rail is driven by an OR gate whenever a correction occurs. The bits in the error-bit rail that are associated with corrected data or orchard bits must also be corrected out of the error-bit rail to ensure reliable error correction in subsequent data. An error-correction counter informs the host system of how many corrections have occurred. The data word and orchard bit (WXYZ0) and any uncorrected error-flag bits are then transferred to the second corrector stage.

All errors that have flagged two error flag bits into the error-bit rail are corrected in the second error-corrector stage (Fig. 8). The second corrector stage operates like the first corrector stage, with a few minor exceptions. Since each of the pattern recognizers is looking for any of three possible combinations of 2 error flag bits, they consist of three AND gates ORed together. The exclusive-OR gate at P should only be driven when an odd number of corrections are being made. The gate is driven with the odd sum output of a parity generator. A second-stage correction counter informs the host system the number of corrections that are made. The corrected data and orchard bits are available to the host system at the output port B. □

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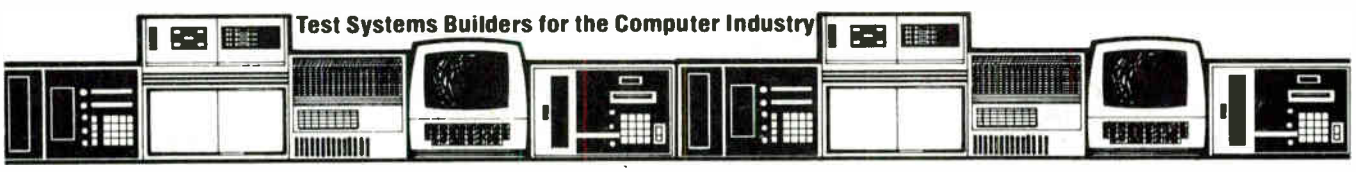

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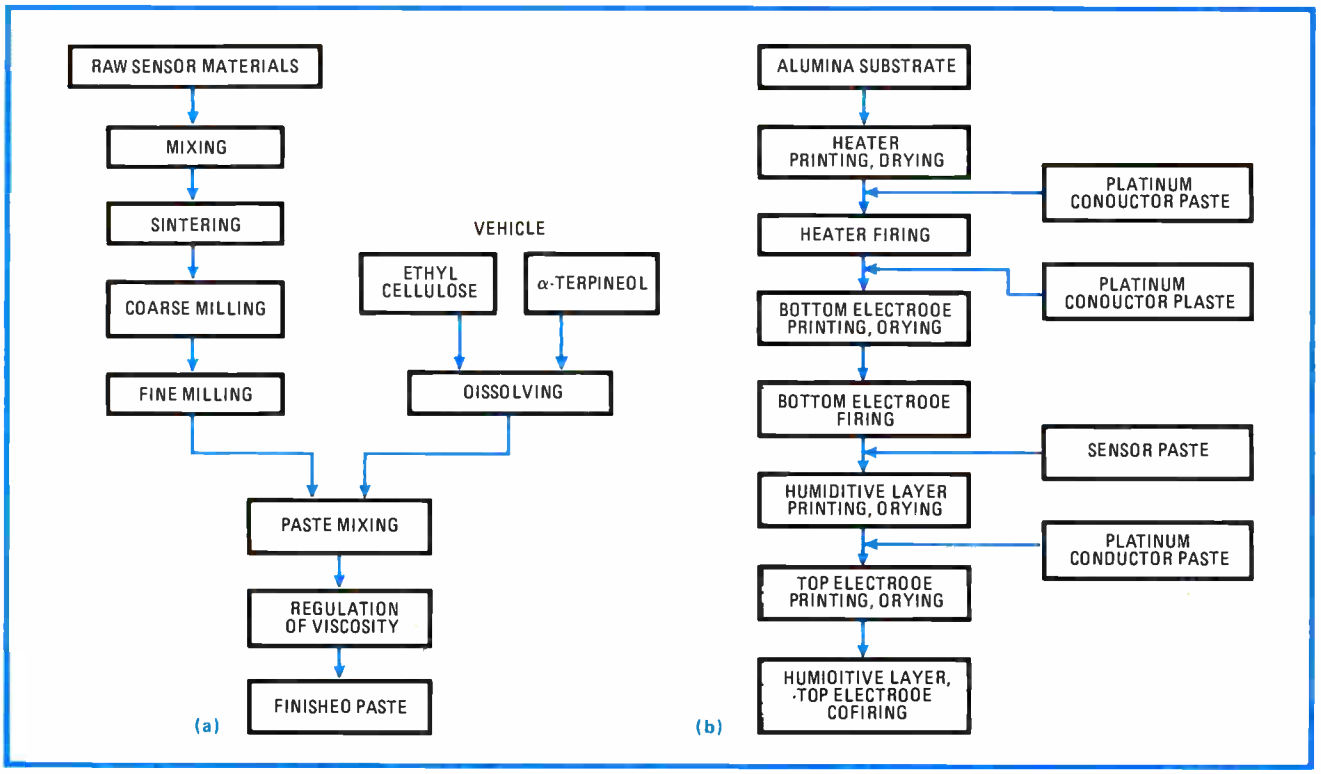
A fiber-optic switch, a new semiconductor oxide, and a silicon-tantalum hybrid are among the advances discussed at this year's Electronic Components Conference

by Vincent Biancomano, *Circuit Design Editor*

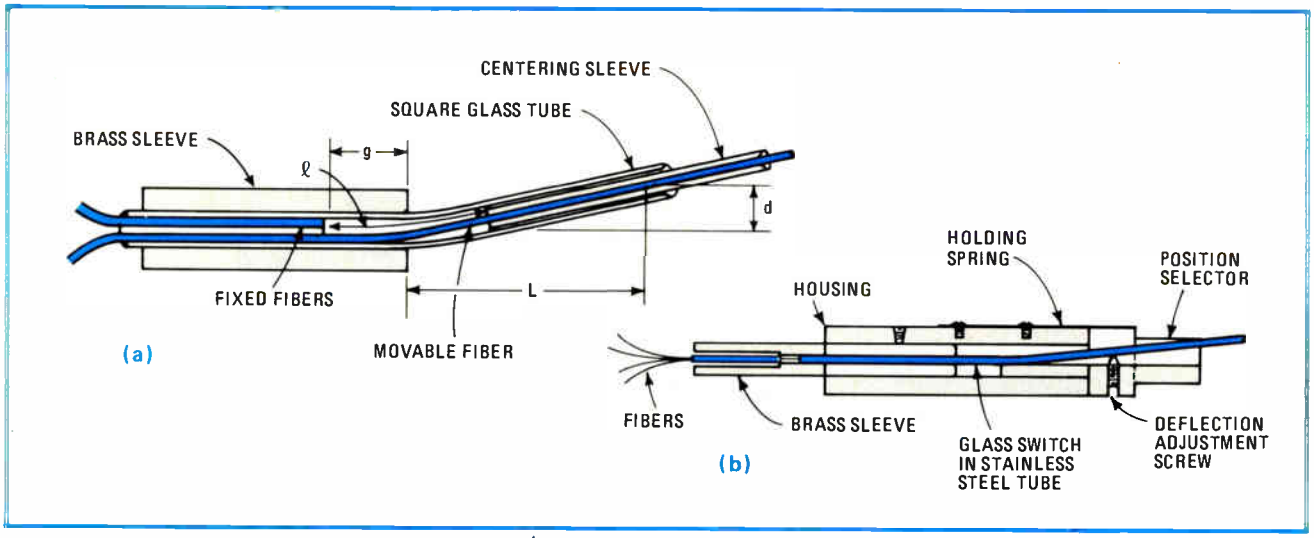
☐ The ever greater performance at higher frequencies being achieved by electronic devices produced with the discrete, integrated- and optical-circuit technologies rarely fails to excite both users and design engineers, who marvel at their future capabilities. But proclaiming these advances in the inherently low-profile manner that everyone has come to expect of the Electronic Components Conference can be difficult. The design professional may not find the description of hybrid fabrication particularly exhilarating, and the technician, who works with the finished product, may have little desire to learn of the nitty-gritty of thin- and thick-film bonding, manufacturing technology or connector construction. Nevertheless, this year's conference, which will be held in Atlanta, Ga., from May 11 through 13, again promises to hold interest for both.

The conference, sponsored jointly by the Institute of Electrical and Electronics Engineers and the Electronic Industries Association, will devote two sessions each to discrete devices, manufacturing technology, circuit reliability, and device interconnections, and three to the processing and capabilities of integrated optical circuits. Sessions will also be devoted to hybrid technology, connectors and contacts, and polymers for encapsulation. And all this will be capped by the conference's special evening event on May 11, where the packaging of computers for high-performance applications, particularly for the 580 series of Amdahl and the IBM 3081 machines, will be examined in three concurrent sessions.

Of the regular sessions, the second and tenth will be devoted to discrete devices, with session 2 focusing on largely theoretical matters and session 10 probably containing more information pertinent to the circuit designer than any other. In session 2, a wide range of topics



1. Moist milling. Hitachi has fabricated a thick-film humidity sensor from a new semiconductor material, manganese tungstenate, by milling (a) and firing (b). The device has high sensitivity, low resistance, and a relative humidity detection error due to airborne pollutants of only 4%.



2. Light loss. Cross-sectional view of optical-fiber switch with an average loss of only 5 dB shows switching layout (a) and protective stainless-steel tube (b) that has a rudimentary position selector and an adjustment screw incorporated into it as an actuation mechanism.

will be covered including the properties of base-metal thick films on porcelainized steel substrates (A. N. Prabhu, from RCA Corp. in Princeton, N. J.), the effects of dopants on cadmium oxide thick-film resistors (Shen-Li Fu and Gi-Chang Lin from the University of California at Los Angeles), the use of titanium-gold–based conductors in microwave applications (F. Dizon, R. J. Thompson, and B. W. Whitaker from Hewlett-Packard Co., Santa Rosa, Calif.), the performance of cermet resistors on ceramic substrates (H. S. Hoffman and E. S. Stephens from IBM Corp., Essex Junction, Vt.), and a report on a new failure mechanism in thin-film resistors (R. E. Lund and J. M. Gorres from Sperry Univac division, Blue Bell, Pa.).

The session paper of perhaps the most interest to circuit designers will be delivered by S. Iwanaga and A. Ikegami of Hitachi Ltd. in Yokohama, Japan, who discuss how a new semiconductor oxide material, manganese tungstenate ($MnWO_4$), is used to fabricate a thick-film humidity sensor that has high sensitivity and low resistivity. The sensor developed has a sandwich configuration similar to that of a thick-film capacitor, with its refresh heater located on the back side of an alumina substrate (Fig. 1). The sensor is mounted on a TO-5 header and bonded with gold wire. Having a (resistance) sensitivity of 7.8% for each percent change in relative humidity, the finished $MnWO_4$ sensor has a response time of only 30 seconds. Its temperature coefficient is 0.5% relative humidity per °C, and its stability is within ±1% for 5,000 hours. Accelerated life tests have confirmed that the resistance drift caused by corrosive gases such as hydrogen sulfide, sulfur dioxide, and nitrogen dioxide is less than 40%. This corresponds to a detection error of only 4% in relative humidity.

Schottky treatment

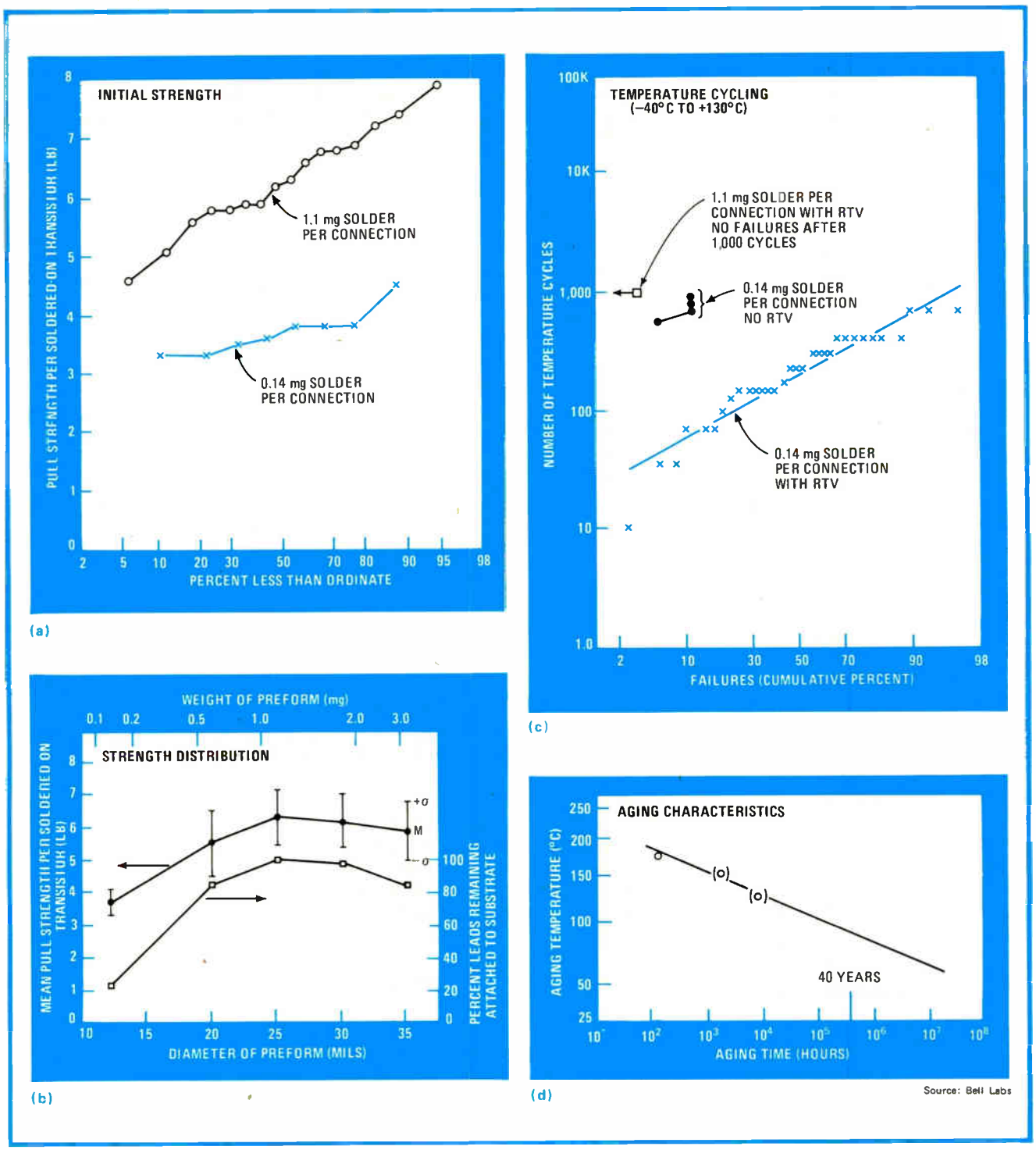
In session 10, N. Christian McGrath from Sprague Electric Co., Inglewood, Calif., will introduce a new solid tantalum capacitor, and a group from the Nippon Electric Co., Kanagawa, Japan, will detail a large-capacitance multilayer ceramic capacitor. Other topics are a polymer-based polyswitch (F. Doljack and G. Ballog from Raychem Corp., Menlo Park, Calif.) and a vertical-groove junction field-effect transistor for power applications (D. Simpson of Mostek Corp., Carrollton, Texas, and O. Eknoyan of Texas A&M University).

A short paper, presented by M. Weichold and O. Eknoyan of Texas A&M, with J. A. Coquat of Sandia National Laboratories, Albuquerque, N. M., reports the results of measurements made on platinum, chromium, aluminum, and nickel-based Schottky diodes for high-temperature applications. The researchers subjected these devices to heat aging at 275°C for 1,000 hours and then evaluated them by considering the barrier height and leakage-current density as a function of time. The results indicate that the most important factor affecting the performance of these devices is surface-state density, which can be minimized by prolonged aging. In these tests, nickel Schottky diodes emerged as the most stable devices. However, more work on reliable bonding techniques is needed to resolve the leakage-current problem that exists in present-day packaged devices.

Manufacturing technology will be the subject of sessions 7 and 9 and will include discussion of test systems, insulation reliability evaluations, the fabrication of high-density multilayer substrates, and ultrasonic wire-bonding techniques. Of particular interest to designers should be two papers delivered in session 9. In one, authors H. Nakamura, T. Inoue, and H. Sasake from Nippon Electric explain how thick-film multilayer substrates with very dense circuit patterns have been developed using a thick-film paste.

Present-day substrates include thick-film conductors that have a width and spacing of 50 micrometers, which is suitable for existing multichip hybrid integrated circuits with large-scale and very large-scale integration chips. The new dielectric paste, however, is pinhole-free at thicknesses as low as 15 to 20 μm, and circuits thus far produced are highly reliable in operation.

The question of density is also taken up in a paper by K. Otsuka and T. Usami of Hitachi Ltd. in Tokyo, which demonstrates how ultrasonic wire-bonding is achieved on a custom IC having 108 pins. Otsuka and Usami show that the most common wire-bonding technology, the



3. Attachment. Extensive work on soldering leaded components to thick-film hybrids concludes that 1.1 mg of solder per lead gives optimum initial strength (a) and strength distribution (b), reduces the number of failures to zero (c), and extends reliability many years (d).

flying-wire bond, has a number of advantages over the tape-carrier or flip-chip techniques for ICs with a large number of pins. These include its suitability to standard manufacturing facilities and packaging technology. Wire bonding is also the most cost-effective choice if high bonding accuracies are to be achieved.

The treatment of optical-circuit, optical-processing and optical-fiber technology has been well integrated in the highly technical session 3. Fabrication is the main issue, with F. J. Leonburger and L. M. Johnson of the Massachusetts Institute of Technology discussing the manufacture of multibranching, single-mode waveguides from lithium niobiate. Also included are presentations on stoichiometry control, fabricating a 16-channel integrated optical data preprocessor, and the evaluation of surface acoustic-wave devices using X-ray spectroscopy.

In a related session on integrated optics and semiconductor processing, the resistance characteristics of highly

doped, large-grain silicon films will be discussed by a forum from Stanford University, Advanced Research & Applications Corp. in Sunnyvale, Calif. and National Semiconductor Corp. in Santa Clara, Calif., and electrical activation and impurity redistribution of amorphized silicon during laser pulsing will be examined by A. Bhattacharya and B. G. Streetman from the University of Illinois. The fabrication-oriented topics in session 4 will include a discussion of optical coupling between single-mode fibers and $LiNbO_3$ waveguides by several members of the Naval Research Laboratory in Washington, D. C., and a report by S. Naumann, R. W. Wu, and J. T. Boyd from the University of Cincinnati on a mask-making process for integrated optical circuits.

For those interested in optical-fiber components, Jeff Montgomery and Frank Dixon of Gnostic Concepts Inc., Menlo Park, Calif., will discuss the state of the art in long-wavelength fiber-optic sources and detectors in session 12. M. Entenberg, G. H. Olsen, and D. J. Channin from RCA will speak of the reliability of fiber-optic sources, and E. R. Nichols and G. W. Bickel from the U. S. Air Force research facilities at the Wright-Patterson Air Force Base in Dayton, Ohio, will report on optical couplers.

As for the devices that have been constructed, a group from Bell Laboratories in Norcross, Ga., will review their work in fabricating a mechanical fiber-optic switch that has a lower insertion loss than any previously reported (Fig. 2). In addition, H. M. Berg, G. L. Lewis, and C. W. Mitchell from the Motorola Semiconductor Group in Phoenix, Ariz., will describe a high-performance package, equipped with connectors, that is useful for housing a double-heterojunction light-emitting diode.

Richard A. Davis from Spectronics Inc., the Honeywell division in Richardson, Texas, discusses the development of a fiber-optic star-coupler for a 32-terminal data-bus system, which will be used in a future 128-terminal system. The mixing-rod type of 64-port coupler has excellent optical characteristics, with a port-to-port excess loss average of 5.4 decibels, a connector-interface loss of only 1 dB, and a tuning range of at least 10 dB for most cases, with a minimum loss of 1 dB.

Making the connection

A problem fundamental to all integrated circuits, that of connecting the die to various internal and external points, is covered in sessions 1, dealing with bonding interconnection, and 6, covering soldered interconnections. One of the most important papers presented will be that by T. S. Liu and O. E. Pitkanen of Honeywell Inc., Minneapolis, who will discuss the surface treatment and bondability of copper thick-film circuits. These copper circuits are among the most recent arrivals brought about by the shortage of noble materials. Their lab findings confirm that copper films can indeed be metallurgically stable if suitable precautions are observed.

Related material presented in the session includes a discussion by a group from DuPont, Wilmington, Del., of the ultrasonic bonding of aluminum wire to thick-film copper conductors. The researchers conclude that the wire deformation that occurs in the process, although bordering on the optimum range for ultrasonic wedge bonds, is within mil spec 883, which calls for deformation to be maintained within 1.2 to 30 times the original wire diameter. They also found that bond failures occur exclusively near wire breaks. The process proved extremely stable in that little or no diffusion occurs during high-temperature storage at up to 250°C and no electrochemical corrosion occurs during storage at high humidity. Further, the group says minimum pull-strength, in excess of the military specification of 2.325 grams for 1 mil and 3.0 g for 1.25-mil wires, can be achieved by this method for all bonds following storage at elevated temperatures for 1,000 to 2,000 hours and thermal cycling between −55° and +150°C.

Forming a bond

The bonding problems associated with the titanium-platinum-gold metalization of hybrid microwave thin-film circuits will be addressed by R. Thompson, D. Cropper, and B. W. Whitaker from Hewlett-Packard, and T. J. Matcovich of Kulicke & Soffa Industries, Horsham, Pa., will present an overview of the trends in bonding technology. Rounding out the session, S. L. Grovender from 3M Co., St. Paul, Minn., will describe the firm's Quip system approach to bonding.

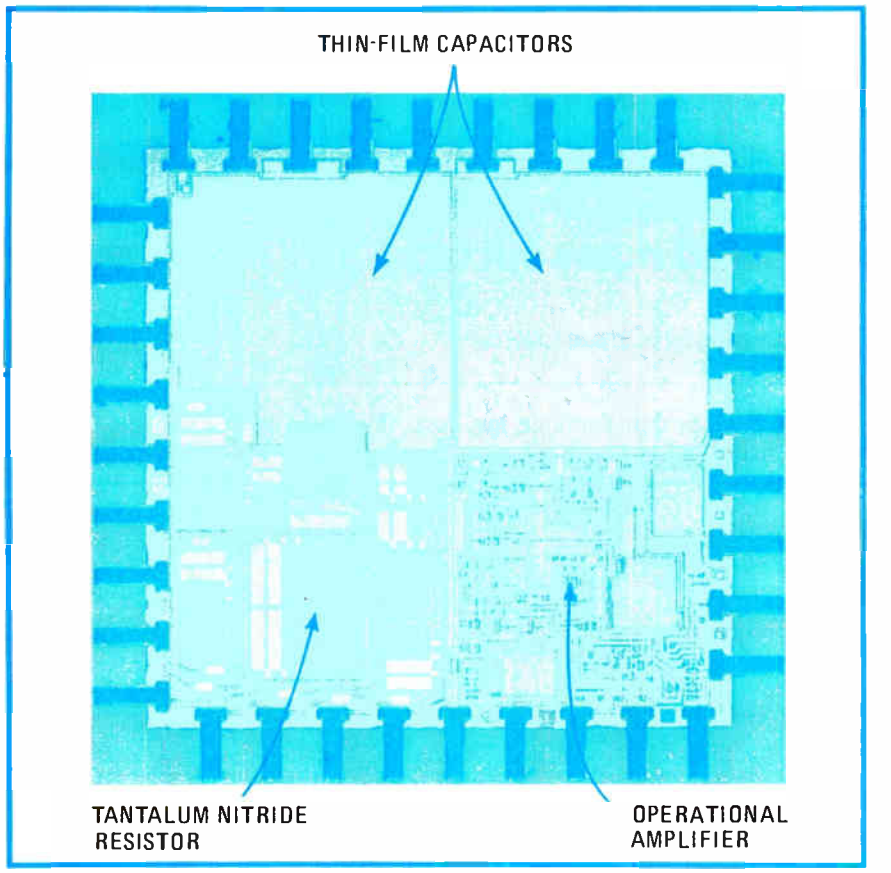
Soldered interconnections present similar problems, and these are addressed in session 6. Included is a description by a group from Hitachi of a process for fabricating solder bumps by electrochemical means and one of ways to attach lead components to thick-film hybrids (N. Panousis and R. Kershner of Bell Labs, Allentown, Pa.). Peter M. Hall, also of Bell Labs, explains how to attach a solder post of a ceramic chip carrier to a ceramic-film–type IC.

In both of the last papers, the real parameters controlling the process efficiency are the amount of solder used per given connection or volume per post respectively. In particular, Panousis and Kershner have found that soldered-on transistors surface-mounted by reflow soldering to standard platinum-palladium-silver thick films using a 60%-tin-to-40% lead alloy require about 1.1 mg of solder per connection for optimum results (Fig. 3). Solder amounts between 0.6 and 2.0 mg will give acceptable results, and quantities down to 0.14 mg will take hold initially, but are clearly inferior.

Hall has found that there are several advantages in making the standoff height of soldered leadless carriers as large as 0.010 to 0.020 inch, rather than 0.001 to 0.020 in. or, as is often the case, 0.001 to 0.002 in. These include easier cleaning and subsequent encapsulation, more compliant joint configurations, better accommodation of nonplanarity, and relief from problems associated with differential thermal expansion. Such standoff heights can be obtained by solder-bumping the chip-carriers prior to their attachment to the IC. The larger solder volume also improves self-alignment capabilities and decreases gold embrittlement.

With chip densities increasing all the time, keeping the various sections of hybrid ICs totally isolated from each other is becoming of greater interest to designers. Session 5 is dedicated to this subject. Six papers will be presented, but the ones of greatest interest should prove to be that by R. C. Mancke (Bell Labs, Allentown), who

4. Mixing. Bell Labs has incorporated this active filter on a silicon chip containing laser-trimmed tantalum nitride resistors, thin-film capacitors, and an op amp. The resulting chip design has 36 beam leads.



discusses a moisture-protection screening test for hybrid-circuit encapsulants, and the presentation by Belani and Sporck from National Semiconductor Corp., who use a negative-resist process for laying down a polyimide as a dielectric in dual-layer metal structures.

Breeding new hybrids

Recent advances in hybrid technology will dominate session 14. Among the papers is one by a group from Bell Labs in Allentown that discusses a silicon-tantalum integrated circuit process for combining both thin-film technologies on a single chip to provide greater flexibility in circuit design and significant economy in production (Fig. 4). A group from Hughes Aircraft Co., Los Angeles, Calif., will deliver its findings on the Kovar large-area hybrid module, a 3.23-in.^{2} device that has great application in ultrahigh-speed avionics signal processors. Also of note is the presentation of a paper outlining an 800-megahertz adjustment-free power amplifier, by the experts at Oki Electric in Tokyo.

The six-paper session 13 will update the industry on advances in connectors and contacts, including a mention of the environmental factors affecting the life of palladium plating, lubrication films, and metallic-finish systems for microelectronic components and the factors influencing thin-gold performance in separable connectors. The most noteworthy of the papers on a practical level, however, will be an analysis of press-fit technology by R. P. Goel of Amp Inc. in Harrisburg, Pa., that considers the optimum connector-pin shape and flexibility for maximum reliability and life on a given board.

High reliability is, of course, desired for any process or product, and ECC has two sessions devoted to this subject. Fittingly, George Harman of the National Bureau of Standards presides over the first session, at which a group from Sandia Labs will discuss the extreme radiation tolerances expected of high-temperature solid-state microelectronic devices.

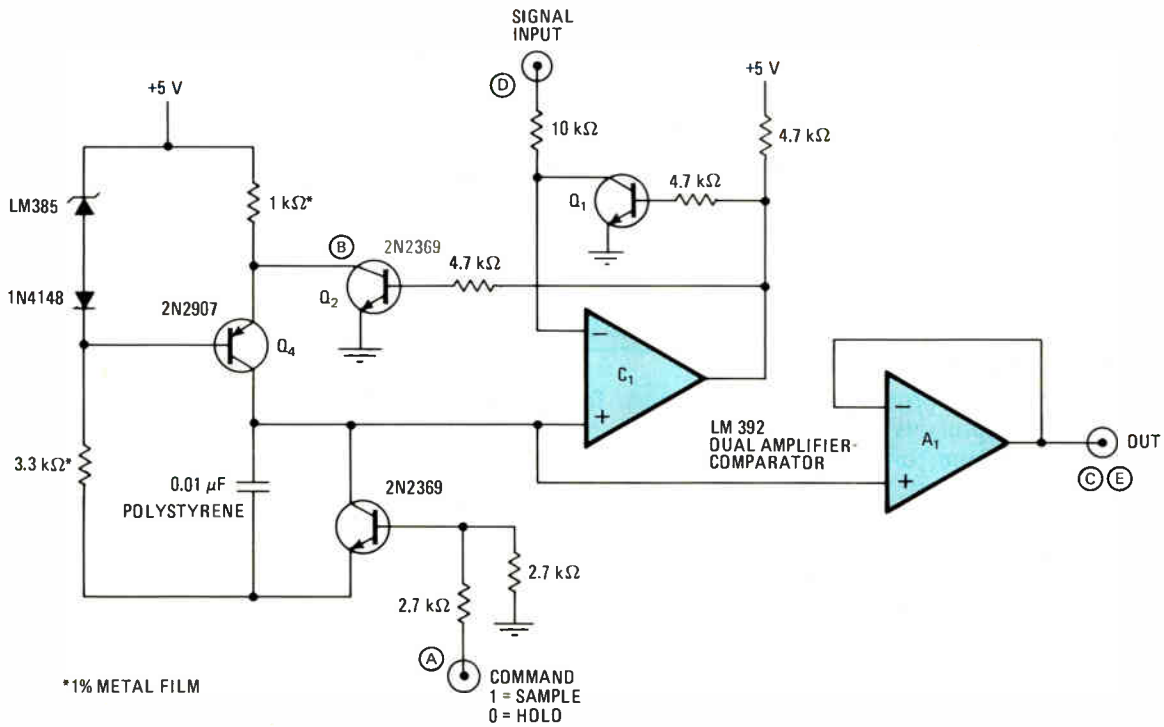
Also included are discussions of the electronic stability of an epoxy-bonded surface, the development of a pre-encapsulation cleaning process to improve the reliability of hybrids, reliability tests of aluminum-metalized MOS dynamic random-access memories, and the integrity criteria for gold-based bonds placed on crescent-type pins. The most notable paper here is probably one by a second group from Sandia, which has developed an LSI package that can pass the stringent particle-impact noise detection test of MIL STD 883B with an assurance of 90%.

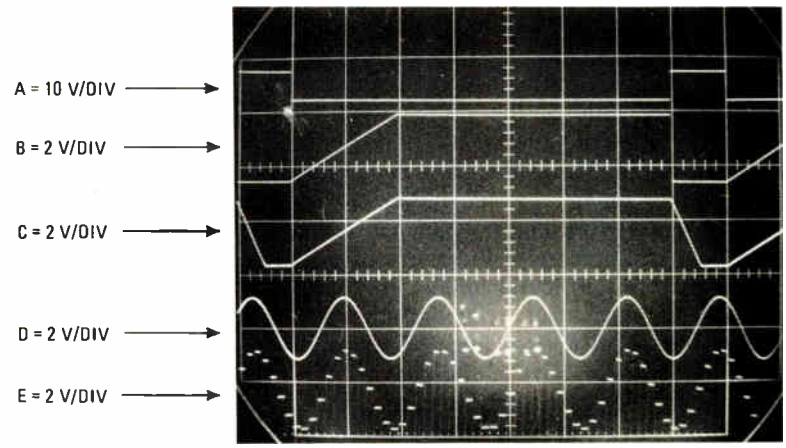
The second reliability session includes papers advancing techniques for examining thermal-cycle fatigue damage in microsocket solder joints (E. Levine and J. Ordone of IBM in East Fishkill, N. Y.) and data-based reliability assessments of selected electronic parts, with comparisons to handbook-derived assessments, by G. T. Merren of Sandia. Another paper by a group from Westinghouse Corp. in Baltimore, Md., assesses the reliability of currently obtainable multilayer leaderless ceramic chip-carrier hybrids. Other rather specialized papers include presentations on an electrochemical corrosion model for conductor lines on a microelectronic substrate, component field-failure data analysis, and an empirical Bayes analysis method for any component. □

Dual-function amp chip simplifies many circuits

by Jim Williams
National Semiconductor Corp., Santa Clara, Calif.

Various circuits that combine low cost, single- or dual-supply operation, and ease of use can easily be built with comparators and operational amplifiers like National Semiconductor's LM339 and LM324 because of their general applicability to a wide range of design problems. Now circuit complexity can be reduced even further with up-and-coming dual-function devices like the LM392, which put both a comparator and an op amp on one chip. Besides allowing a degree of flexibility in circuit function not readily implemented with separate chips, this device retains simplicity at low cost. The building of such circuits as a sample-and-hold circuit, a feed-forward low-pass filter, and a linearized platinum thermometer is





1. Compact sampler. A comparator and op amp chip consolidates a sample-and-hold circuit, which utilizes only one supply, has virtually zero gain error, and will not self-trigger. Owing to the configuration, the device does not have to rely on the hold cycle, so that the circuit is simplified.

discussed here in the first of two articles.

The circuit in Fig. 1 is an unusual implementation of the sample-and-hold function. Although its input-to-output relationship is similar to standard configurations, its operating principle is different. Key advantages include no hold-step glitch, essentially zero gain error and operation from a single 5-volt supply.

When the sample-and-hold command pulse (trace A) is applied to transistor Q_3, it turns on, causing Q_4's collector to go to ground. Thus the output sits at ground. When the command pulse drops to logic 0, however, Q_4 drives a constant current into the 0.1-microfarad capacitor (trace B). At the instant the capacitor ramping voltage equals the signal input voltage, comparator C_1 switches, thereby causing transistor Q_2 to turn off the current source. Thus the voltage at Q_4's collector and A_1's output (trace C) will equal the input.

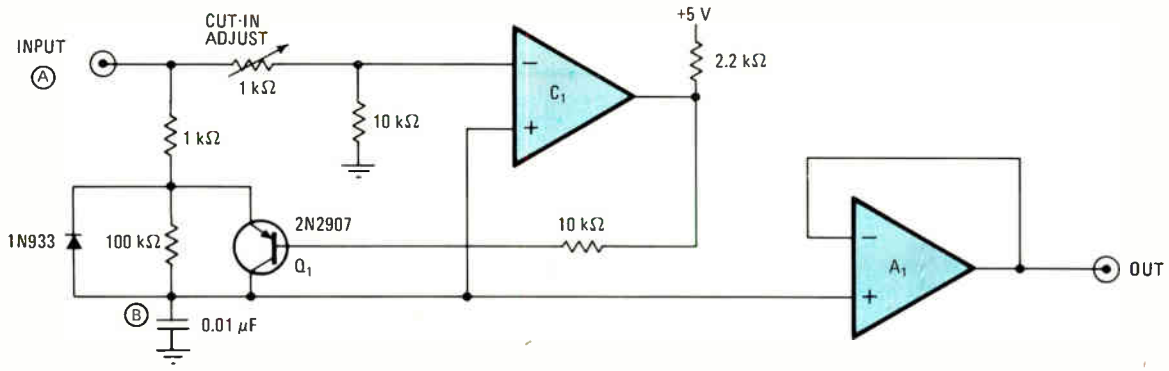
Q_1 ensures that the comparator will not self-trigger if the input voltage increases during a hold interval. If a dc-biased sine wave should be applied to the circuit (trace D), a sampled version of its contents will appear at the output (trace E). Note that the ramping action of the current source, Q_4, will just be visible at the output during sample states.

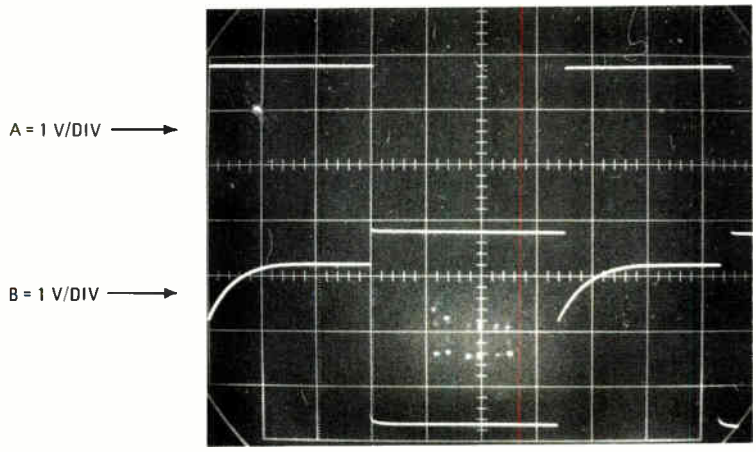
In Fig. 2, the LM392 solves a problem common to filters used in multiplexed data-acquisition systems, that of acquiring a signal rapidly but providing a long filtering time constant. This characteristic is desirable in electronic scales where a stable reading of, for example, an infant's weight is desired despite the child's motion on the scale's platform.

When an input step (trace A) is applied, C_1's negative input will immediately rise to a voltage determined by the setting of the 1-kilohm potentiometer. C_1's positive input, meanwhile, is biased through the 100 K −0.01 F time constant, and phase lags the input. Under these conditions, C_1's output will go low, turning on Q_1.

This action causes the capacitor (trace B) to charge rapidly up to the input value. When the voltage across the capacitor equals the voltage at C_1's positive input, C_1's output will go high, turning off Q_1. Now, the capacitor can only charge through the 100-kΩ resistor and the time constant must therefore be long.

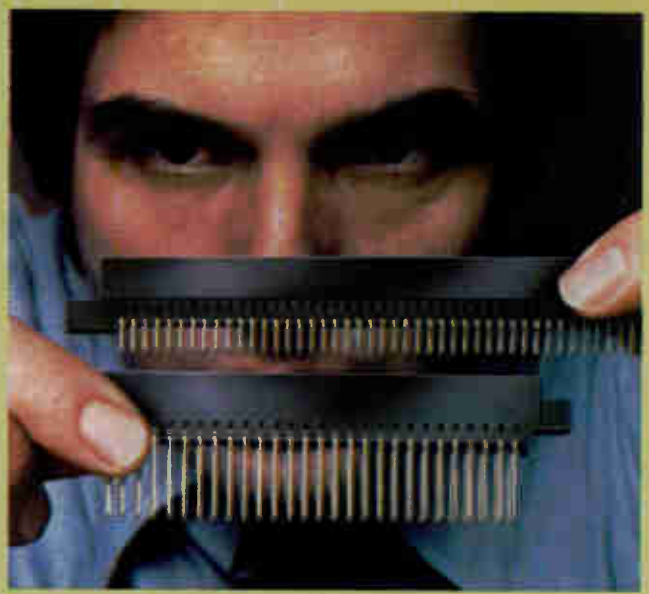
The point at which the filter switches from the short to the long time constant is adjustable with the potentiometer. Normally, this pot will be set so that switching occurs at 90% to 98% of the final value (note that the trip point is taken at about the 70% point in the photo so that circuit operation may be easily seen). A_1 provides a buffered output. When the input returns to zero, the





2. Feedforward. This simple low-pass filter provides sharp acquisition and long decay, so that it is perfect for multiplexed data systems and electronic scales for infants. Its time constant is adjustable with the potentiometer and is typically set to 90% to 98% of the full input value.

For a standard edge connector, our low-cost standard stands out.

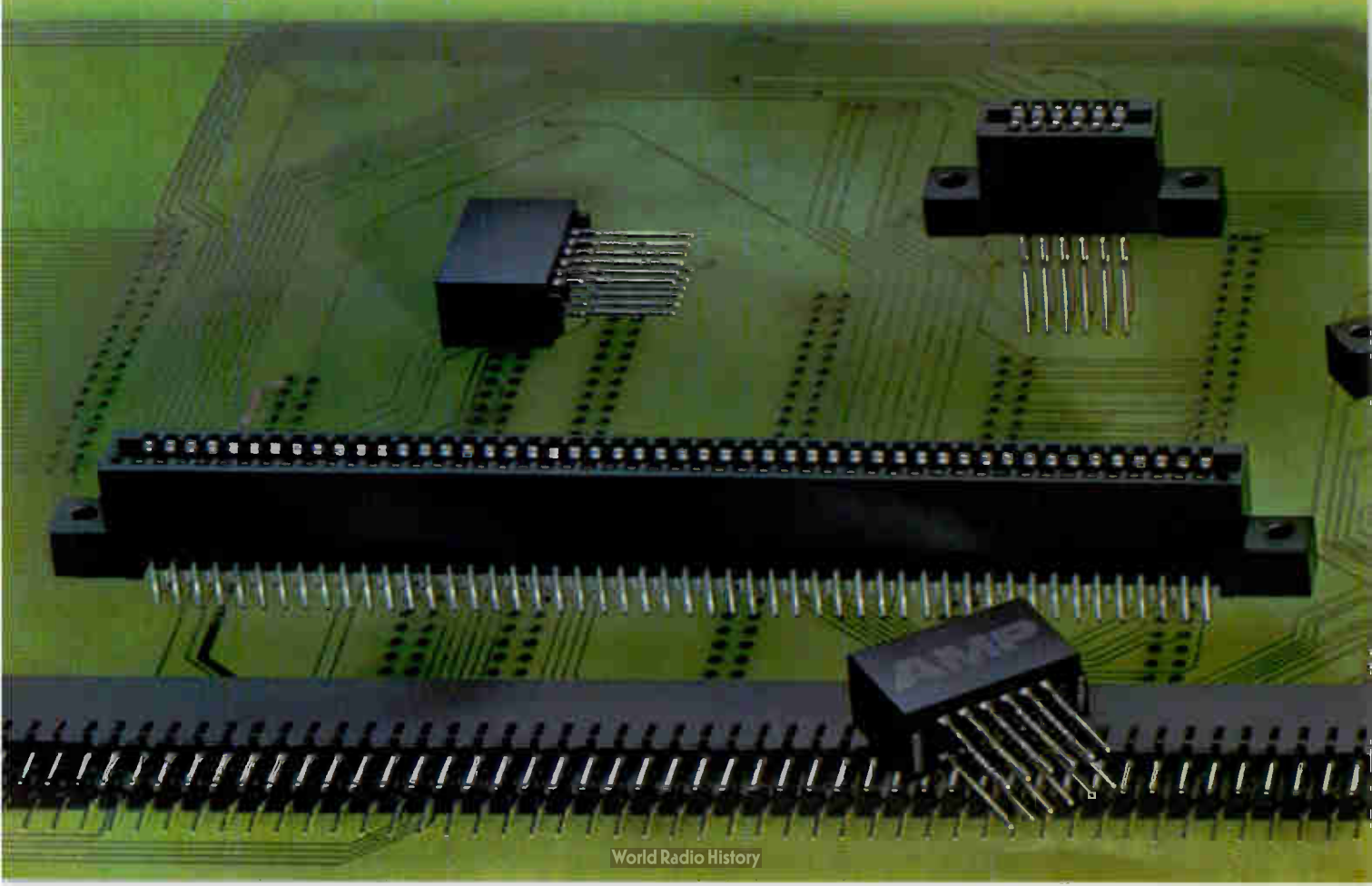


Standard dimensions are only a small part of the AMP Standard Edge Connector story.

Another part is Accu-plate, the exclusive plating process that precisely plates different metals on the same contact—without waste. Nickel underplate, gold only where it's needed and tin lead on the legs for easy solderability.

For high reliability, the bifurcated leaf spring contact compensates for board warp. And now you can have a version with our compliant ACTION PIN contact for solderless board mounting.

Delivered on time through our computer-linked regional inventory system, these quality connectors even compete in price with more ordinary types.

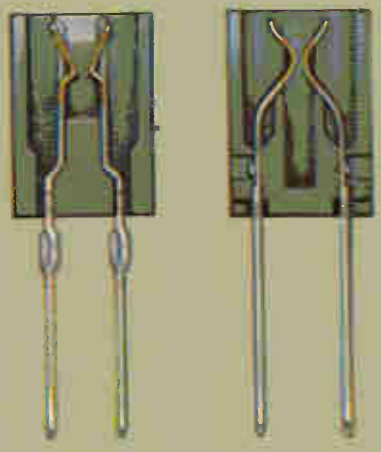


AMP Facts

Sizes and Dimensions: 6 to 50 positions on .100" centers (.200" row-to-row) and .125" centers (.250" row-to-row). Height—0.610". Card slot depth 0.295". Card extender version also available.

Current Rating: 3 amperes.
Resistance: 12 milliohms.
Voltage Capability: 1000 VAC at sea level
Operating Temperature: -55°C to +105°C.
Insulation Resistance: 5000 megohms (minimum after humidity test).
Vibration Test: 10 to 500 cycles per second (10 G's peak).
Engagement Forces: 8.0 ounces typical for .062" board.
Humidity Test: 90-95% for 96 hours.

Accu-plate precision-plated gold only in contact area keeps costs down while maintaining performance.



Contacts are nickel-plated phosphor-bronze.

Available with .025" wrap-type posts or solder tails.

ACTION PIN contact available for solderless application.

For a free sample, call the AMP Standard Edge Connector Information Desk at (717) 780-8400.

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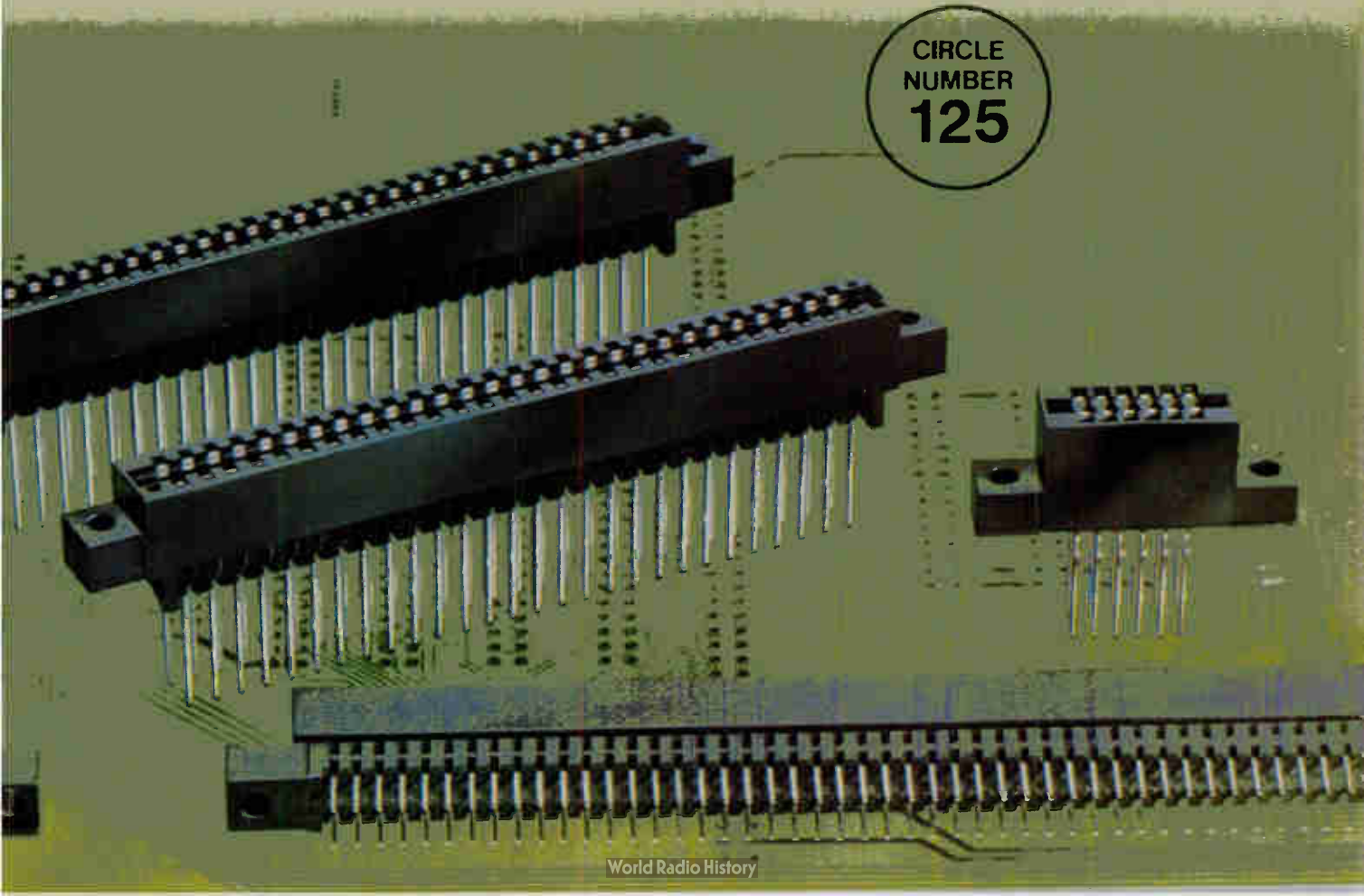
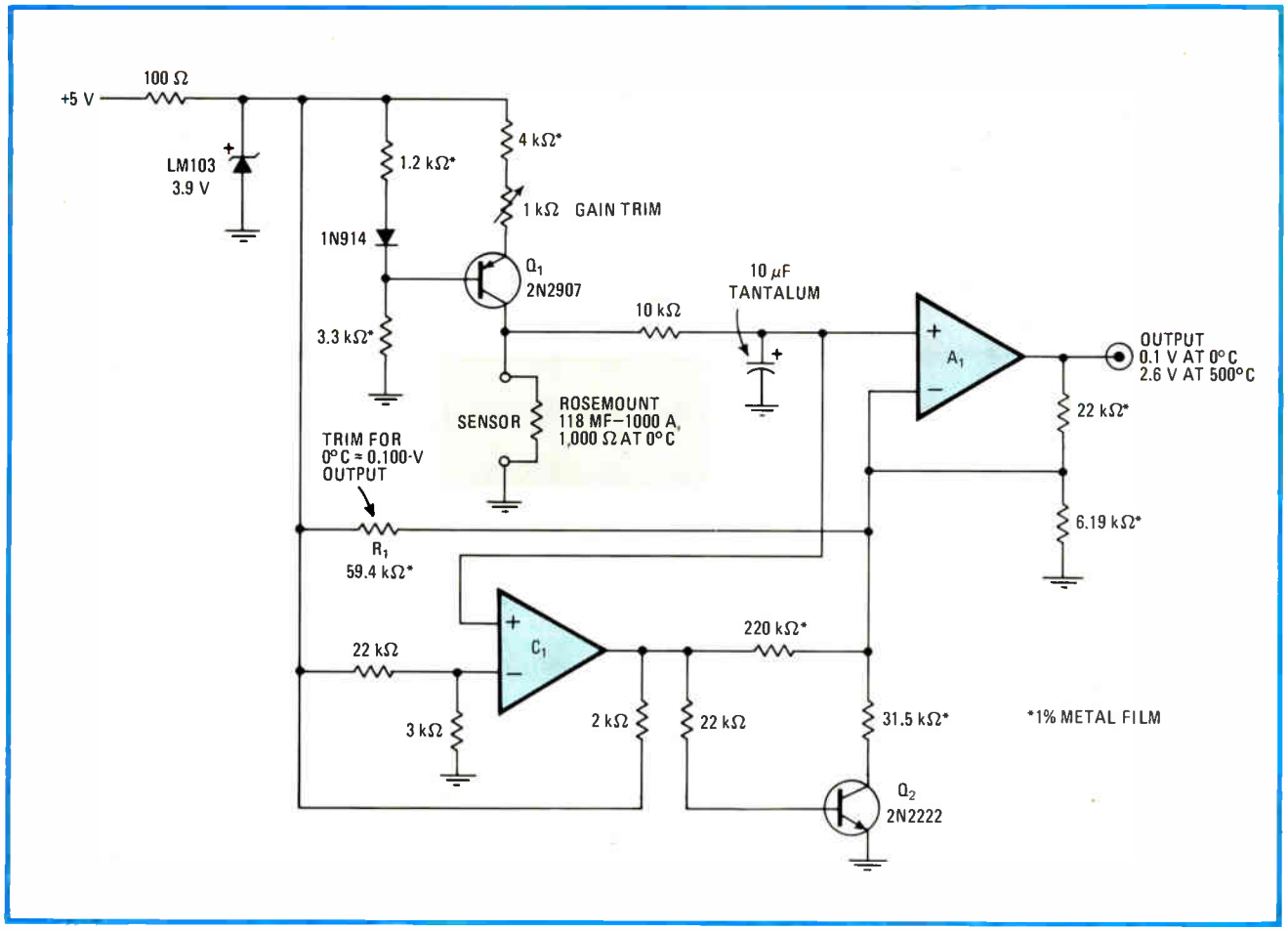




3. Tracking thermals. This platinum RTD thermometer has 99% accuracy over the 0°-to-500°C range. C_1 derives the breakpoint change in A_1's gain for sensor outputs exceeding 250°C, compensating for the sensor's nonlinearity. Current through the 220-kΩ resistor shifts A_1's offset voltage, in effect preventing glitches at the breakpoint. The instrument is calibrated only at two points with a decade resistor box.

1N933 diode (a low forward-drop type), provides rapid discharge for the capacitor.

In Fig. 3, the LM392 is used to provide gain and linearization for a platinum resistor-temperature device in a single-supply thermometer circuit. This one measures from 0°C to 500°C with ±1° accuracy.

Q_1 functions as a current source that is slaved to the 3.9-v reference. The constant-current–driven platinum sensor consequently yields a voltage drop that is proportional to its temperature. A_1 amplifies the signal and provides the circuit output.

Normally, the slightly nonlinear response of the sensor would limit the circuit accuracy to about ±3°C. C_1 compensates for this error by generating a breakpoint change in A_1's gain at sensor outputs corresponding to temperatures exceeding 250°C. Then, the potential at the comparator's positive output exceeds the potential at the negative input and C_1's output goes high. This turns on Q_2, which shunts A_1's 6.19-kΩ feedback resistor and causes a change in gain that compensates for the sensor's slight loss of gain from 250° to 500°C. Current through the 220-kΩ resistor shifts the offset voltage of A_1 so no discernible glitch will occur at the breakpoint.

A precision decade box should be used to calibrate this circuit. Once inserted in place of the sensor, it is adjusted for a value of 1,000 ohms and a 0.10-v output by means of resistor R_1. Next, its resistance is set to 2,846 Ω (500°C) and its gain trim control adjusted for an output of 2.6 v. These adjustments are repeated until the zero and full-scale readings remain fixed at these points. □

One-chip alarm scares auto thieves

by Andrei D. Stoenescu
Bucharest, Rumania

Most of the burglar alarms that have been designed in recent years to discourage automobile thieves contain too many parts (thus raising doubts about their reliability), need special parts, draw too much current, or cost too much. Actually, a circuit that provides the very same features as most alarms now available can be built around only one integrated circuit and a power transistor. Such a circuit is shown here. Its power drain is only

6.2 milliamperes in the idle state, and its cost can be held to under $10.

Once activated by a hidden switch inside the car, the alarm, which uses the LM2900 quad amplifier:

- Will be inhibited for a few seconds to enable the driver and passengers to exit from the vehicle.
- Will sound 10 seconds after the opening of any door and remain on independently of the position of any door.
- Will time out after about 400 seconds unless a door is open, in which case the alarm will continue to sound.

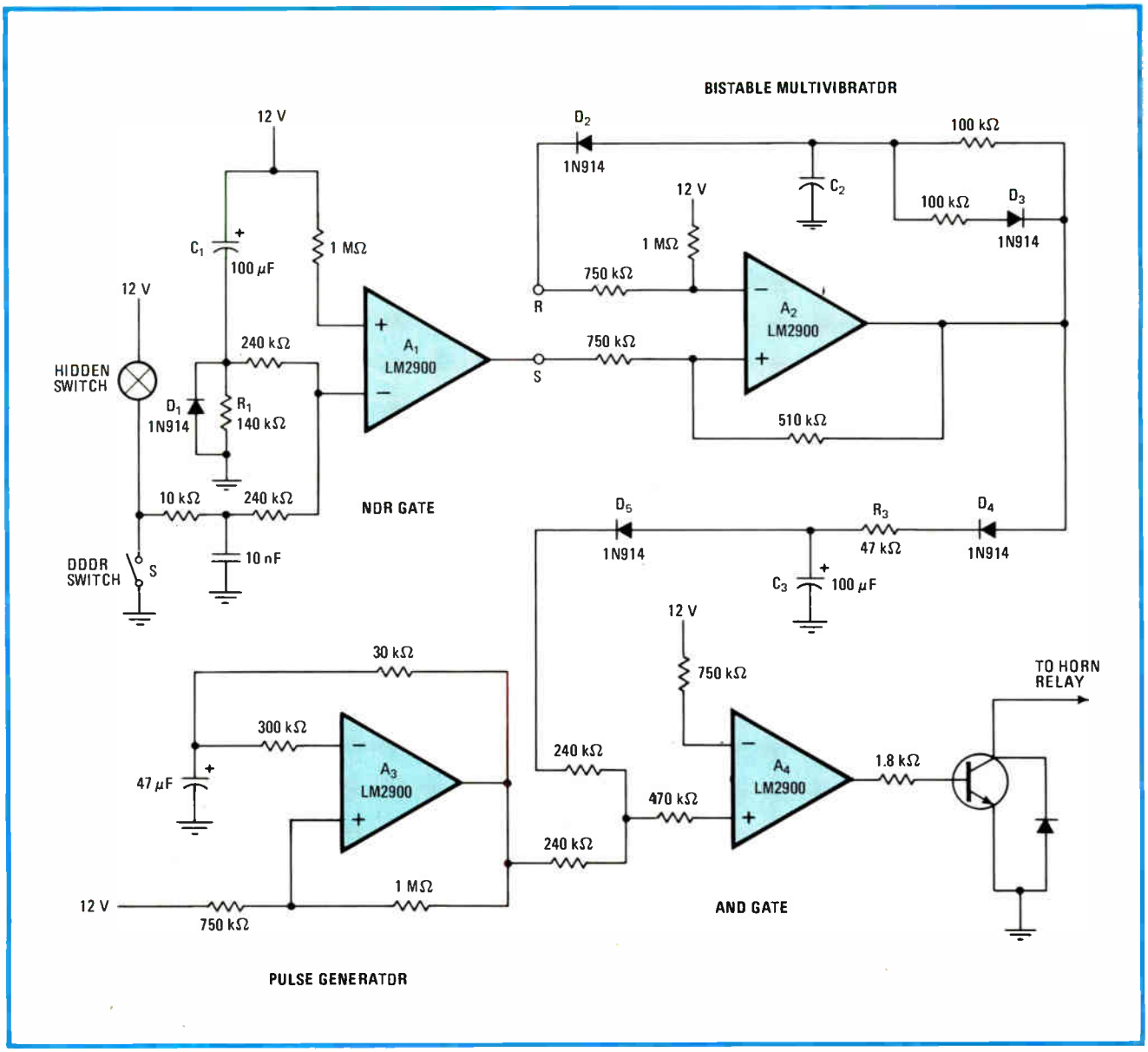
When the circuit is initialized, capacitor C_1 begins to charge and turns the NOR gate A_1 on after a period equal to R_1C_1. After this time, during which the driver leaves the car, a door switch closure to ground is required to set bistable multivibrator A_2 low. The circuit is thus armed.

Opening any door sets the output of the bistable device high, thus allowing capacitor C_3 to charge through resistor R_3. Unless the circuit is disarmed through the hidden switch, the alarm will sound after 10 seconds because the voltage across C_3 will be sufficient to turn on the AND gate A_3, passing the control output of pulse generator A_4 through to the horn relay.

The R_2C_2 combination determines the bistable multivibrator's reset time, which in this case is approximately 400 seconds. Thus the bistable will again be set high if any door is open, and the horn will continue to sound.

Of course, the same logic functions as are needed for this alarm could also be designed using a quad comparator, such as the LM239. The circuit would then require an idling current of only 0.8 mA. Several additional resistors would have to be added, however. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $75 for each item published.



Sedan sentry. This simple alarm uses only two active devices—an LM2900 quad amp and a power transistor—yet performs as efficiently as some of the more complex and expensive circuits. The circuit is activated only after the owner leaves the car and can be disarmed before sounding after he returns. For an intruder, the horn sounds after 10 s and remains on for 400 s. The device can then retrigger.

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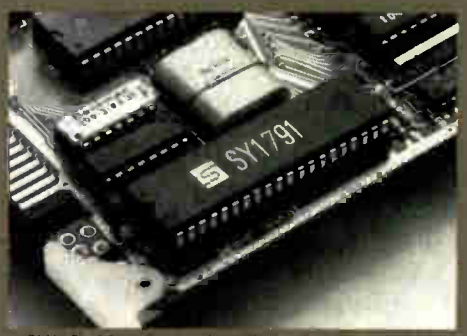

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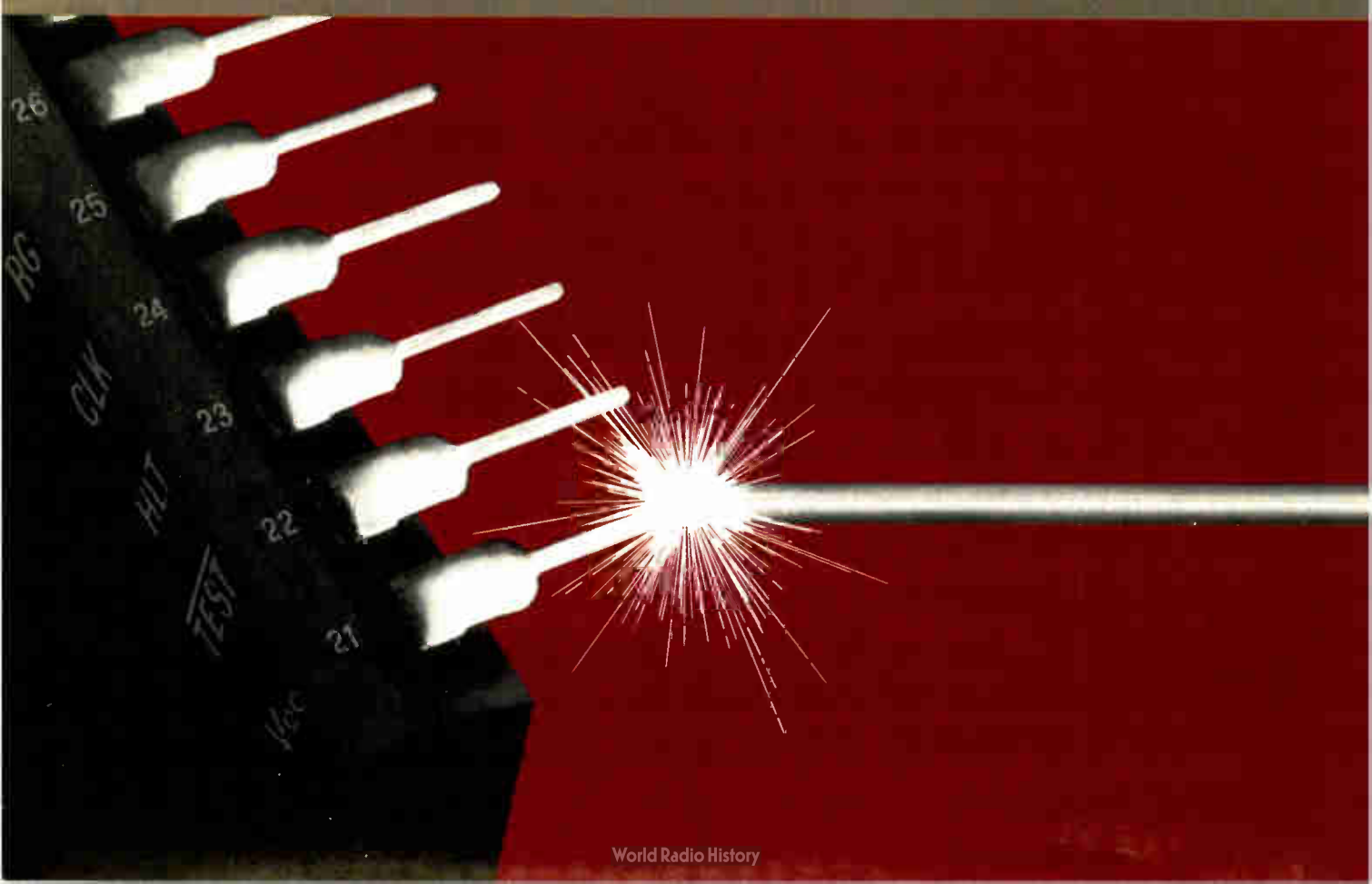


Product development profile

Built-in sensor adjusts operation of bubble cassette to temperature

Removable storage cartridge functions reliably over −20° to +70°C by varying its drive currents and duty cycle

by Les Bury, Ravi Luthra, and George Reyling Jr.
National Semiconductor Corp., Santa Clara, Calif.

☐ Magnetic-bubble memory technology appears destined for widespread use, now that quarter-million and million-bit devices are available along with the necessary support circuits. But perhaps the most dramatic applications will be those that exploit the devices' solid-state ruggedness. Many of these, such as numerical machine-tool control and data-logging in seismic exploration and flight recorders, also require an extended temperature range as well as removable storage media and have been previously addressed by paper-tape and magnetic-tape cartridge systems.

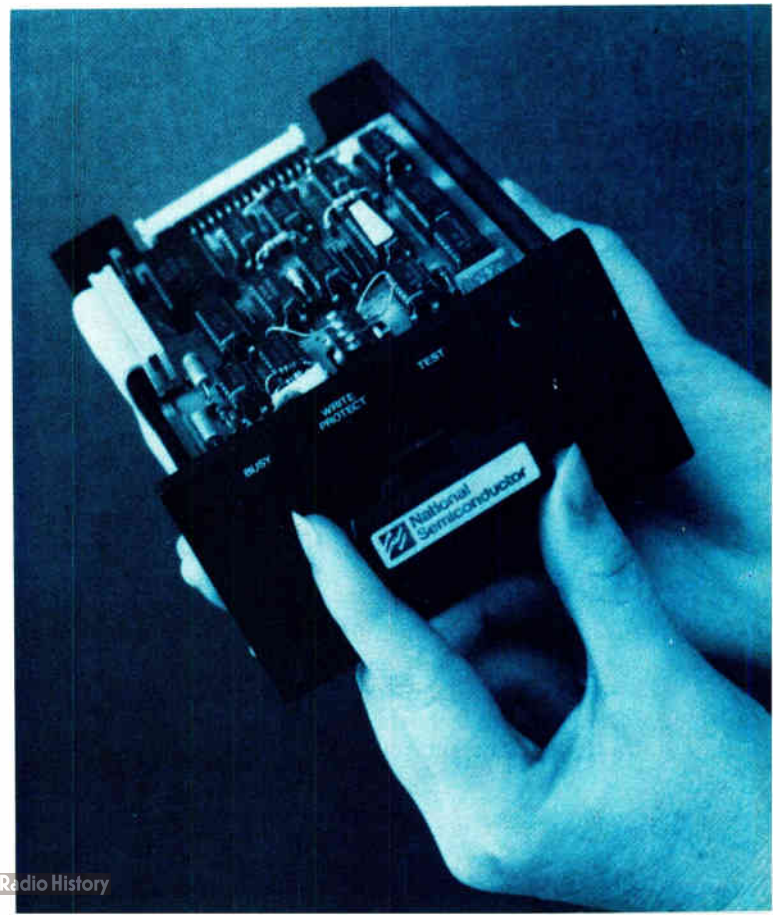
The Bublset subsystem offers nonvolatile solid-state storage in a removable cartridge and operates over an ambient temperature range of −20° to +70° C. The cartridge itself is only 1.8 by 2 by ⅞ inch, while the entire subsystem is less than 2½ by 4 by 5½ in. The table lists other features of the system.

The system is designed to accept interchangeable cassettes with a variety of storage capacities, yet does not require the user to specify that information. Such an arrangement is possible because the quarter- and full-megabit memory chips used in the Bublset share the same pinout, and the controller determines capacity information directly from the cassette. To achieve the goal of a minimum-size, lowest-cost medium, the parts count within the cassettes was kept to a minimum—not a trivial feat, considering that absolutely reliable driving and sensing of the bubble chips through a connector had to be ensured.

Bublset meets that goal. Only the bubble component and temperature-sensing integrated circuit are packed into each cassette, thanks to the design of special bubble-interface circuits for the controller—most notably, a sense amplifier that features automatic zero restoring.

Each cassette may be used in either a read-only or a read-write mode as determined by a three-position indicating selector tab on its body. A cassette can only be written into if its tab is moved to the write position as the unit is inserted. Once the cassette is removed, the tab will automatically move to a second position, indicating that the memory has been written into but not yet read. Finally, when the cassette is to be inserted into another subsystem for reading, its tab must be put into the third position: pressed down flush with the cassette body into the read-only mode, which will serve to indicate later that its data has already been read at least once. This arrangement will prove desirable in data-logging applications where it is important to prevent cassettes containing data from being mixed up with others that have not yet been written into.

The nature of bubble memories clearly demands that the devices must be compensated for at the extremes of their temperature range. Operation at high temperature reduces detector signals as well as margins for starting and stopping; what's more, inadvertent bubble nucleation will occur at elevated temperatures, and also the



Handy. The Bublset cassette stores information in nonvolatile quarter- and full-megabit magnetic-bubble memories. The subsystem operates over a wide ambient temperature range thanks to a temperature-sensing element within the cassette.

FEATURES OF THE BUBLSET REMOVABLE CARTRIDGE	
Small size	2.5 by 4 by 5.5 in. for the complete system
Standard power supplies	+5 and +12 V, for a 4-W power consumption
Dual-capacity cassettes	choice of 256-K or 1-megabit bubble memory chips
Extended temperature range	−20° to +70°C
Two operating modes	data recording and general storage
Data buffer	first-in, first-out memory storing one page of data
Serial interface	300 to 19,000 b/s (per byte) via RS-232-C
Parallel interface	controlled with 8-bit microprocessor
Maximum average data rate	8 kb/s
Maximum access time	30 ms (or 60 ms)
Data integrity	interlocking, self-test mode, power-fail detection
Error detection and correction	based upon 8-bit Fire code
Panel indicators	indicating normal operation, write protection, and test passed
Miscellaneous features	long-life connectors, flush mounting, automatic write protection, dust flap, and resistance to vibration

driving current of the bubble generator must be reduced. Low temperatures, on the other hand, demand higher coil-drive and replicate currents and can cause excessive phase shifting, as well as intolerable chip-to-bias-magnet mismatching. These symptoms are eliminated in the Bublset through a variety of compensatory techniques.

Self-calibration

To begin with, temperature is measured within every cassette by an LM235 temperature-sensing integrated circuit. The sensors, working in conjunction with a microprocessor-controlled analog-to-digital converter within the subsystem, provide the microprocessor with information as to how it should adjust the function-drive current levels at extremes in temperature. The microprocessor sets the sense-amplifier threshold, for example, by searching for the optimum level while it reads data from the cassette. This self-calibrating technique, in fact, compensates for systematic noise pickup in the cassette connector, as well as for manufacturing, temperature, and drive variations in the detector signal.

Also, the high temperature limit is extended significantly by operating the bubble memory with only a 10% duty cycle, which reduces the temperature rise within the device to just a few degrees during operation. Finally, the low temperature limit has been extended through a correspondingly increased drive current that overcomes the reduced bubble mobility encountered at subfreezing temperatures.

The low duty cycle still allows a respectable data rate of 8 kilobits per second, and access times are kept short—30 milliseconds maximum in the quarter-megabit cartridge and 60 ms in the megabit device—thanks to a high field-rotation frequency. Of course, like most operating functions, field frequency tracks with temperature under microprocessor control in the Bublset, and access times will drop to 100 ms and 200 ms, respectively, when the device is used continuously at high temperature.

As an added measure of reliability, tolerance to extreme temperatures is enhanced by error-correction techniques. Thus, some error-rate degradation—which is the first effect of temperature extremes—is acceptable.

Bubble technology has been proven through extensive testing to be highly reliable—a prime reason for its increasing use in telephone and military systems. However, this inherent reliability must be supported by a system design that does not degrade data as a result of unexpected operator actions, system failures, or environmental conditions. The Bublset design incorporates a number of features that maximize system reliability.

One key requirement is to ensure that data integrity will not be affected if the cassette is removed during data transfer. This is accomplished through the use of a microswitch that opens prior to the release of the cassette. The switch senses when the cassette is almost fully engaged upon insertion. The additional expense of sensing a fully engaged position is avoided through the use of multiple-contact-point connectors to prevent any contact from opening during the final stage of insertion travel.

These same connectors ensure the subsystem against open circuits during vibration and in dusty environments. What's more, they are designed for negligible degradation over a lifetime of more than 20,000 insertions.

Ensuring reliability

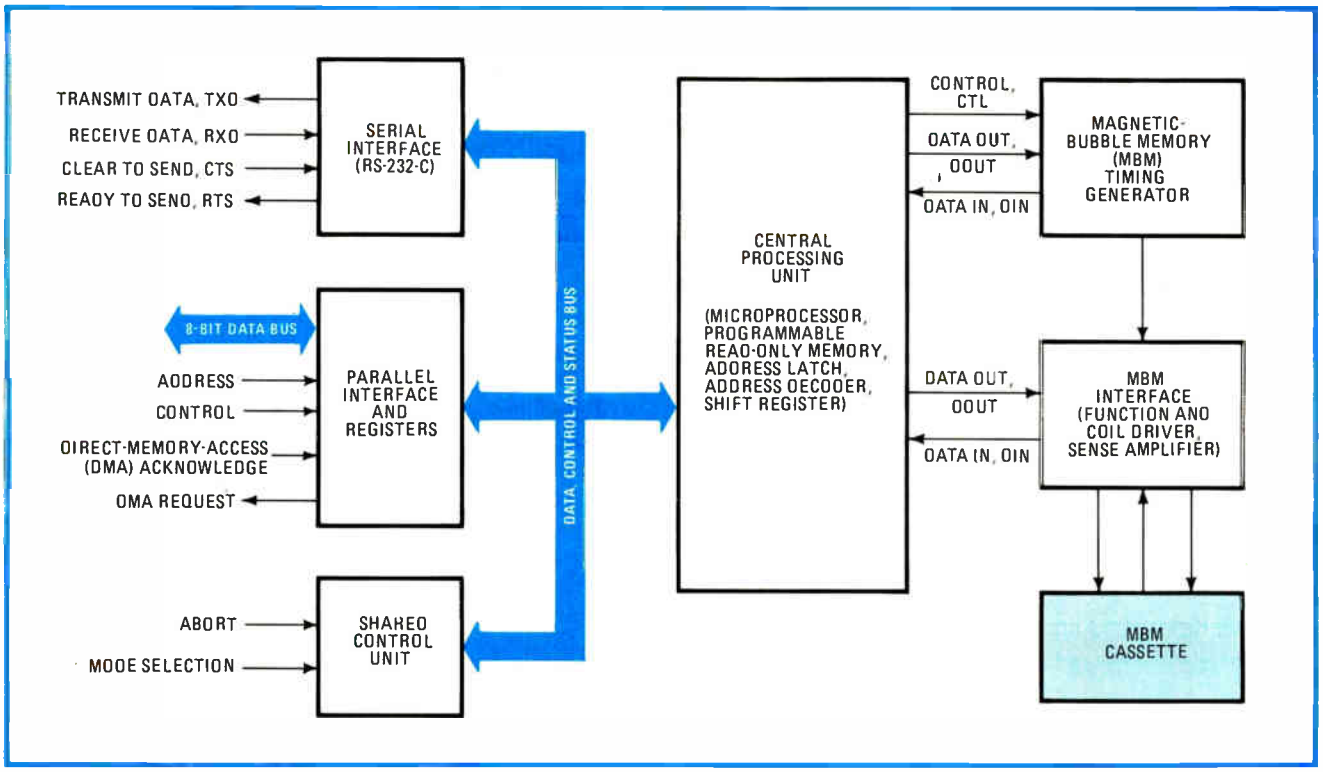
In many applications it is not desirable for the user to remove the cassette intentionally during data transfer, even though data on the cassette will not be affected. That is why the Bublset supplies the front panel with a light-emitting diode that glows whenever the data is being transferred.

The complete Bublset system runs off standard +12- and +5-volt supplies and typically dissipates 4 watts. System power-supply failures are sensed in the cassette subsystem, and all cassette drivers are turned off within 20 microseconds of the occurrence of a failure to prevent data loss.

The power-fail alert

In addition, a power-fail signal input is provided to allow an early warning shutdown based on sensing the state of affairs on the ac power line. During powering up, the same sensing circuits ensure that subsystem supplies are within specification before the cassette is activated. An initialization is then performed that verifies that the redundancy map (which is critical to subsequent bubble-memory operation) contains no errors. Following that, the host system has the option of executing the verify command, which checks to see that the data stored in the cassette is error-free.

Communication with the subsystem is possible through a general-purpose 8-bit parallel interface or, as



1. Smart action. The emphasis on optimizing the operation of the magnetic-bubble memory over a wide temperature range and the requirement for multiple-capacity cassettes led to a microprocessor-based implementation of the control unit in the Bublset cassette.

an option, through an RS-232-C serial interface. Both interfaces may operate in either a general-purpose storage mode—offering all the commands and random access to data pages normally provided by a bubble-memory subsystem—or in a data-recorder mode that provides continuous transfer of data in a read or write mode. The data-recorder mode makes it easy to replace magnetic-tape cassettes or paper tape without a significant degree of software modification, whereas the general-storage mode provides much greater operating flexibility. Interface signals supply interrupts, abort, direct-memory-access transfer, and mode-select capabilities.

Commands provide ease of use

A full set of commands has been implemented in a manner that eases software considerations. The basic commands include read, write, position, initialize, and test. Data may be transferred using the conventional page mode, but the number of bytes per page changes with cassette size. The optional use of a sector mode under software control, however, eliminates this variable by providing a constant sector size.

The read command includes automatic error correction in a form transparent to the user, eliminating the need for user software to handle an excessive number of exception conditions. A full set of status indicators simplifies the handling of exceptions; they include: data request, controller not busy, no cassette, protected cassette, protected write attempt, error detected, uncorrectable error, initialize error, and operating mode. Finally, while not normally used in an end application, a full capability for reading and writing the bubble redundancy-map loop is provided with the device. This is primarily intended for use in field-service operations.

Once a cassette has been inserted in the subsystem, the integrity of its data can be verified by pressing the test switch on the panel. This initiates a reading of the cassette map and data sections (using the error-checking and -correcting parity bits) for verification that they are error-free. Successful completion is then indicated by the illumination of a green LED. Also on the panel is a yellow LED that warns the user that a write-protected cassette has been inserted.

The cassette is keyed to prevent it from being inserted upside down, and once inserted, it is held in place by a mechanical catch and a spring to prevent it from vibrating off the connector. When no cassette is inserted, the cavity and connector in the subsystem are protected against dust and grime by a spring-loaded door. The rugged, heavy-walled construction of both the cassette and the subsystem, which is enhanced by a flush-front-panel design, protect them from impact.

Flexible electronics

The emphasis on optimizing the control of drive and sense parameters over temperature, along with the requirement for multiple-capacity cassettes, led to a microprocessor-based implementation (Fig. 1). The processor also simplifies the implementation of the optional serial interface, the asynchronous data transfer that avoids an overrun condition, the self-testing routine, and the transparent error-correction. On the other hand, use of standard bubble-memory interface circuits kept the package count reasonably low while still providing the necessary flexibility for temperature compensation of driver and sense-amplifier parameters. □

N-channel process increases speed and density of MNOS EE-PROMs

Easy to manufacture and to use, these devices are bidding to expand the MNOS share in the reprogrammable memory market

by M. Kalet, J. Multani, K. Rajkanan, and A. Sass
General Instrument Corp., Microelectronics Division, Hicksville, N. Y.

☐ For almost all their 10-year existence, EE-PROMs have been p-channel metal-nitride-oxide-semiconductor devices, limited by their low speed and density to consumer applications and the low-performance end of the market in electrically erasable programmable read-only memories. But their shift within the last year to an n-channel process makes them fast enough for use with microcomputers and indeed computers in general.

By now General Instrument Corp.'s application of the p-channel EE-PROM to television tuners and the manufacturing experience it therefore gained in supplying such a high-volume market has poised the EE-PROM on the brink of extensive applications in word processing, distributed processing systems, process control, navigation, and telecommunications. And following the GI lead in the EE-PROM market, other integrated-circuit suppliers such as Hitachi, Mitsubishi, and Toshiba are in various stages of developing, supplying samples of, or shipping MNOS devices, thereby assuring the establishment of a future broad supply of EE-PROM components.

It was the prospect of great application diversity that prompted the development of an n-channel MNOS technology, to serve those markets requiring performance, TTL compatibility, and read and write characteristics superior to those of p-channel devices. The p-channel MNOS technology will, however, remain as a low-cost, lower-performance alternative to the n-channel approach and continue to serve its own growth market. In parallel, n-channel MNOS memories with computer-speed–compatible read and write access will serve the higher-performance, higher-cost end of the market.

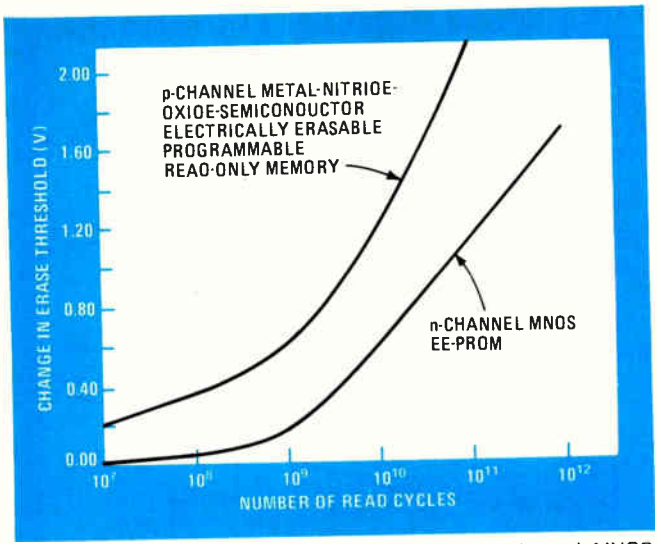
A 1-K n-MNOS EE-PROM, organized as 128 by 8 bits, is available now from General Instrument Corp. A 16-K version, organized as 2 K by 8 bits, is due out by the end of the year.

The difference

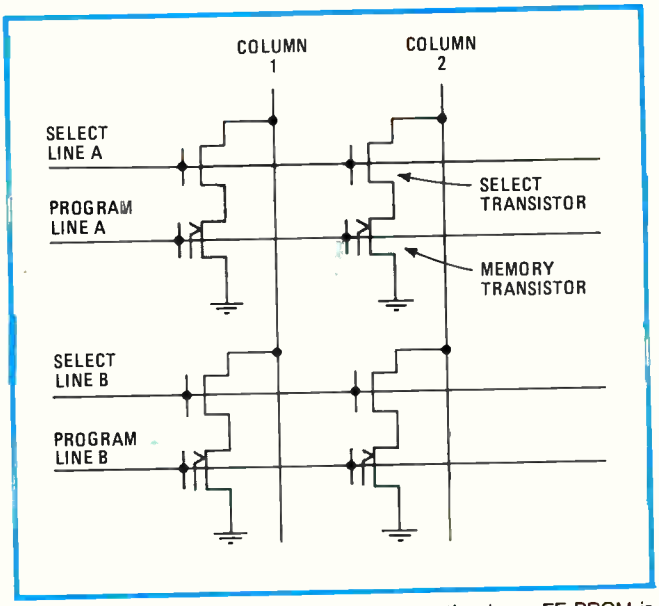
Because p-channel devices suffer from severe density limitations, the memory cells in a p-channel EE-PROM have generally only one transistor each. This cell serves to store a bit of information and is interrogated by applying a voltage directly to its gate. Each read operation diminishes the level of the stored charge until eventually it is depleted. Typically stored charge is maintained for greater than 10^9 read cycles.

CHARACTERISTICS OF 16-K ELECTRICALLY ERASABLE READ-ONLY MEMORIES IN MNOS AND FLOTOX TECHNOLOGIES

	MNOS – silicon-gate	Floating gate
Power supplies for read mode and write/erase mode	+5 V, 25 V	+5 V, 20–25 V
Write time	1 ms/word	10 ms/word
Erase time	100 ms	10 ms
Write/erase cycles	10^4	10^4
Read cycles	unlimited	unlimited
Data retention	10 years	10 years
Power dissipation in read mode and write/erase mode	210 mW, 315 mW	350 mW, 500 mW
Access time	140 ns typical	200 ns typical
Cell size	0.62 mil^2	0.85 mil^2
Chip size	177 by 157 mil^2	165 mil^2



1. Remember when. One advantage that the n-channel MNOS EE-PROM has over its p-channel counterpart is several orders of magnitude more immunity to read disturb effects. This is because it requires less read time and less read voltage.



2. Two are better. The ultimate in data retention in an EE-PROM is achieved by using separate memory and select transistors. The read cycle interrogates the select, not the memory transistor, so no read disturbance effects ever deplete the stored charge.

An n-channel EE-PROM, however, using one-transistor memory cells is orders of magnitude more immune to such read-induced disturbances because it requires a lower read voltage—4 versus 9 volts—and thus bleeds off much less of the stored charge (Fig. 1). This results in 10^{14} read cycles prior to loss of the stored charge. Also, the n-MNOS device is estimated to be able to retain data for 10 years, provided there are not more than 10^5 erase and write cycles.

For enhanced data retention, GI has exploited the greater density possible with an n-channel device by fabricating two-transistor MNOS memory cells. The two-transistor cell can be read a virtually infinite number of times without degradation of its stored information because the read pulses are applied to the series select transistor and not the storage transistor, whose charge therefore remains undepleted (Fig. 2).

The choice of a two- over a one-transistor cell is a cost-performance tradeoff that depends on whether the system application in question does or does not require unlimited read capability. For example, a television tuner application requires only limited read capability during its useful life, whereas a computer store application requires virtually infinite read capability.

Figure 3 depicts the processing steps for both the memory cells, shown on the left side, and the ancillary elements such as the decoders, shown on the right, of an n-channel EE-PROM. The starting wafer is <100> silicon with a p-doped epitaxial layer. Memory array blocks and peripheral devices such as buffers and decoders are formed in separate isolation cells (a) bounded by the n-type barriers. As in conventional MOS technology, this step is followed by the source and drain diffusion and gate oxidation steps (b), which are used to define both nonmemory and memory devices. Ion implantation then tailors the thresholds of the various enhancement and depletion devices. At this stage, the gate oxide on the memory device is etched and an ultrathin oxide is regrown (c), followed by chemical vapor deposition of the silicon nitride layer (d). Electrons tunnel through the ultrathin oxide during the write/erase cycle. Conventional metalization and alloying steps then follow.

Flat-gate memory structures, in which the gate covers the entire channel area, are achievable. But split-gate structures, in which the gate covers only the center of the channel and the enhancement devices on both sides, are generally preferred, since they prevent depletion-mode operation and enhance the memory's endurance.

In another version of the n-channel MNOS EE-PROM, polysilicon gate electrodes replace the aluminum ones [see also *Electronics*, Feb. 24, 1981, p. 154].

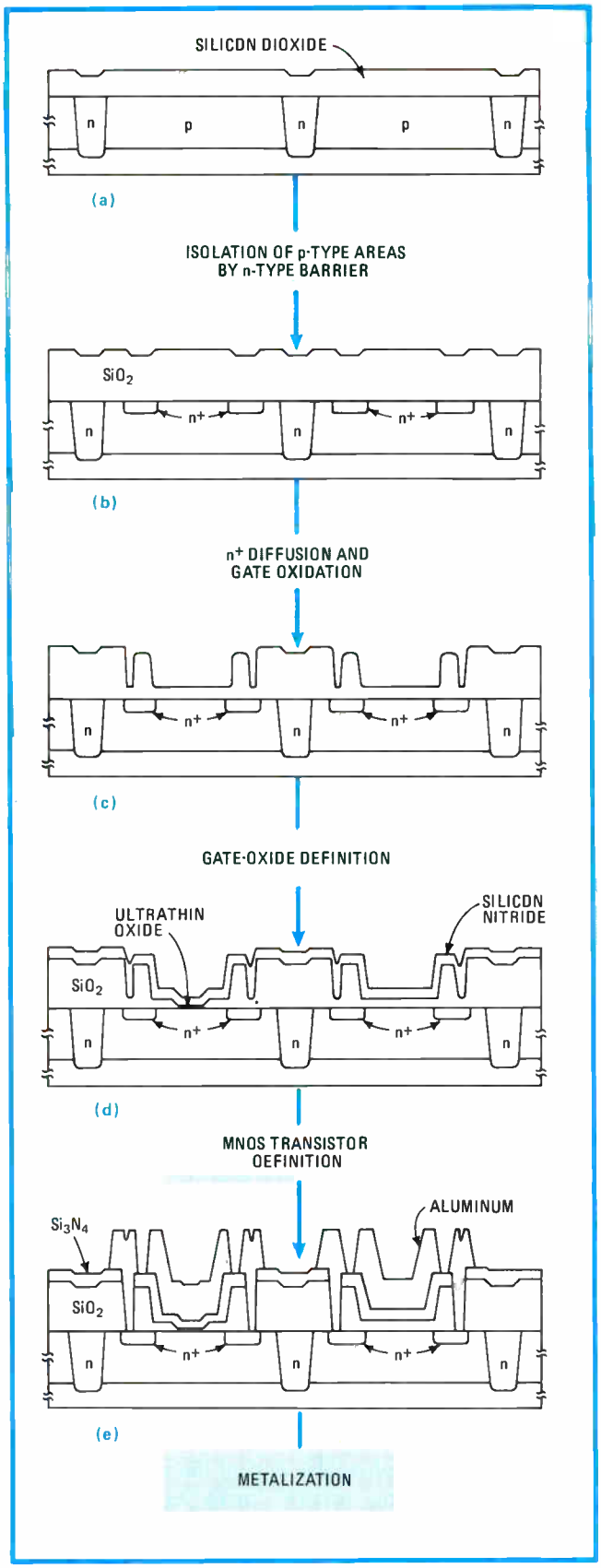
The similarity

The n-channel metal-gate and polysilicon-gate processes are similar. For either of these techniques, the additional requirement beyond standard MOS processing is to control the tunnel oxide and memory nitride. In terms of horizontal processes, various cell structures and design rules lead to EE-PROMs with high bit densities currently ranging from 0.1 to 0.4 bit per square mil.

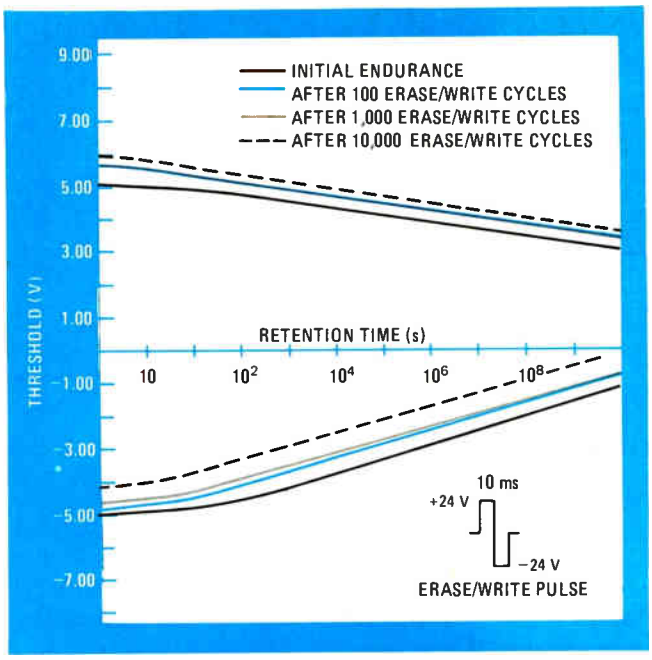
Typical erase and write characteristics of an n-channel EE-PROM are shown in Fig. 4. In the write state, electrons tunnel from the channel area and are stored in the traps in the silicon nitride gate, while in the erase state holes are stored.

The tunneling mechanism for the write and erase states can be different. Experimental evidence suggests that a modified Fowler-Nordheim tunneling [*Electronics*, Sept. 13, 1979, p. 39] occurs during the write operation and direct tunneling occurs during erasing. A fast write/erase time, about 1 to 10 milliseconds for a 20- to 24-V pulse, is easily attainable.

The data-retention characteristics of the n-channel EE-PROM are also shown in Fig. 4 and indicate a nominal retention of 10 years. Retention characteristics are affected somewhat with the erase and write cycling.



3. Fabrication. The processing steps for n-channel EE-PROMs draw heavily on standard MOS technology, but differ from other components in the formation of an ultrathin oxide layer through which charge carriers tunnel during programming.



4. Repeat performance. The threshold voltage is affected by both time and the number of read and write cycles that the n-channel EE-PROM undergoes, but less so than with p-channel. Data retention still lasts about 10 years if the erase/write cycles do not exceed 10^5.

However, no significant retention loss occurs if the number of erase and write cycles does not exceed 10^5.

Recently technologies competitive with MNOS have been introduced to serve the EE-PROM market [*Electronics*, Feb. 28, 1980, p. 113]. Foremost among these is a floating-gate process developed by Intel. Called Flotox, it stores data as charge on a floating conductive polysilicon gate, as opposed to the nonconductive nitride gate in the MNOS case.

The two technologies exploit the same semiconductor mechanisms. Both use thin oxide tunneling for transferring charge. One- and two-transistor cells are possible in both and MOS peripheral circuitry is integrated on the same chip as the memory cells.

However, the nitride gate is superior to the floating conductive gate in one respect. In the event of even a single pinhole defect in the oxide of a floating gate device, all the stored charge will flow to ground, since the charge resides on a conductive layer. On the other hand, the charge stored in a MNOS device is located in discrete trap sites within the nitride; pinholes in the oxide will affect only the area immediately below them and not the total charge. Therefore, MNOS charge storage has an inherent advantage over floating-gate technology in terms of processing flexibility and control.

Its rightful position

The EE-PROM takes its place in the programmable read-only memory spectrum as the product that offers completely electrical reprogrammability. Its popularity will continue to grow mainly as a result of new applications, impractical prior to its advent, rather than its replacement of PROMs or E-PROMs. The identification of these new applications remains among the most promising aspects of the EE-PROM's development. □

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Five-chip meter measures impedances ratiometrically

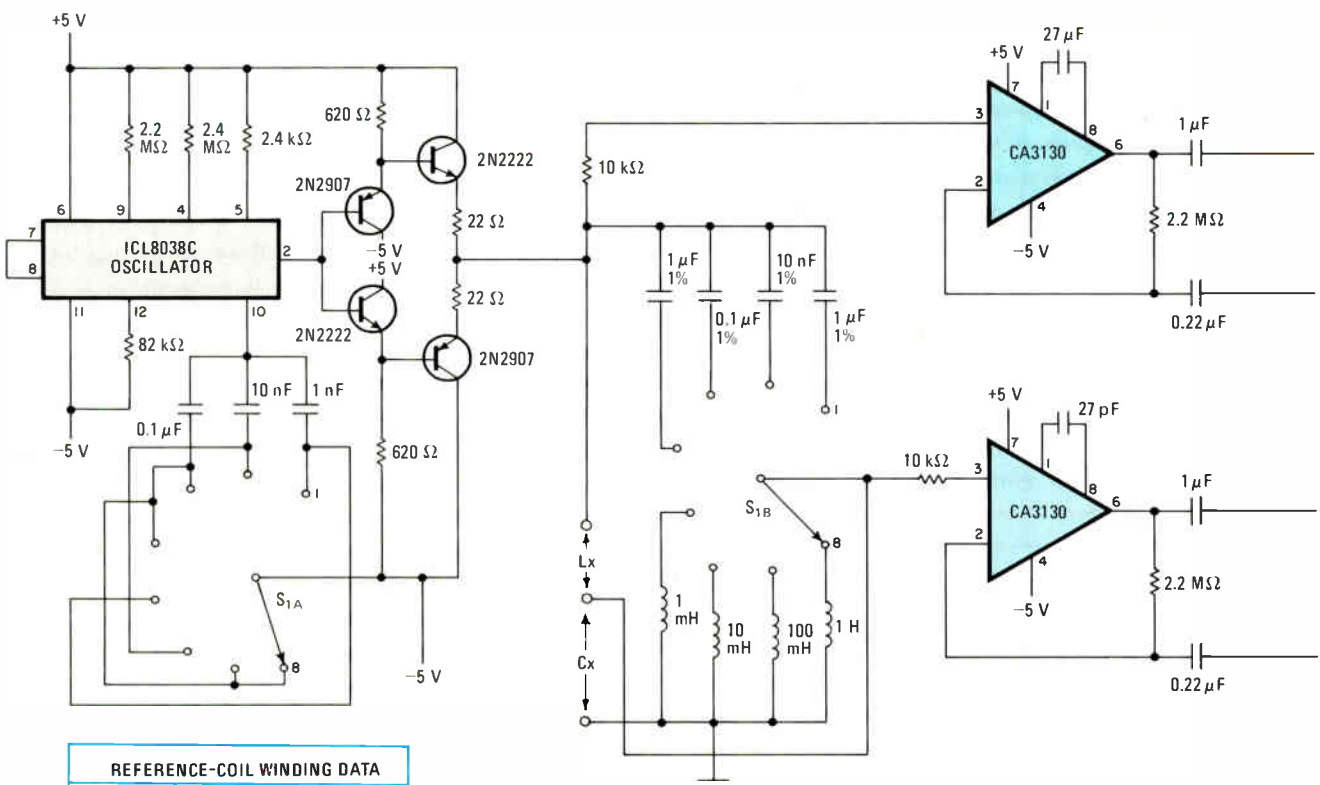
by N. E. Hadzidakis
Athens, Greece

Measuring both inductance and capacitance usually requires either a manual bridge, which is difficult to use, or a digital bridge, which is expensive. Recently, inexpensive hand-held capacitance meters have appeared on the market, but they employ a time-to-charge technique that cannot be applied to the measurement of inductance. The circuit shown here, however, utilizes a ratiometric method that is suitable for both types of measurement. Its only disadvantage is the requirement for one calibrated reference component per range. Still, it is inexpensive and easy to use.

Generally, the potentials across a reference and test inductor or capacitor, which are dependent on the frequency of the 8038 square-wave driving source, are applied to two ac-to-dc converters built around CA3130 operational amplifiers. The converters' output is then compared at the ICL7107 ratiometric converter. Because the value of the reference inductor or capacitor is a multiple of 10, the value of the test element can be read directly from the display.

In the case of measuring inductors, it can easily be shown that:

$$L_x = \frac{L_{ref}\,e}{2+1/e} + \frac{L^2_{ref}e^2(e+1)}{(2e+1)-R^2/4\pi^2f^2}$$



REFERENCE-COIL WINDING DATA		
VALUE	CORE TYPE	TURNS
1 mH	PC-2213-77	17
10 mH	PC-2213-77	55
100 mH	PC-2616-77	150
1 H	PC-3019-77	420

SWITCH POSITION	1	2	3	4	5	6	7	8
FULL-SCALE INDICATION	2 nF	20 nF	200 nF	2 μF	2 mH	20 mH	200 mH	2 H
TEST FREQUENCY (kHz)	100	10	1	1	100	10	1	1

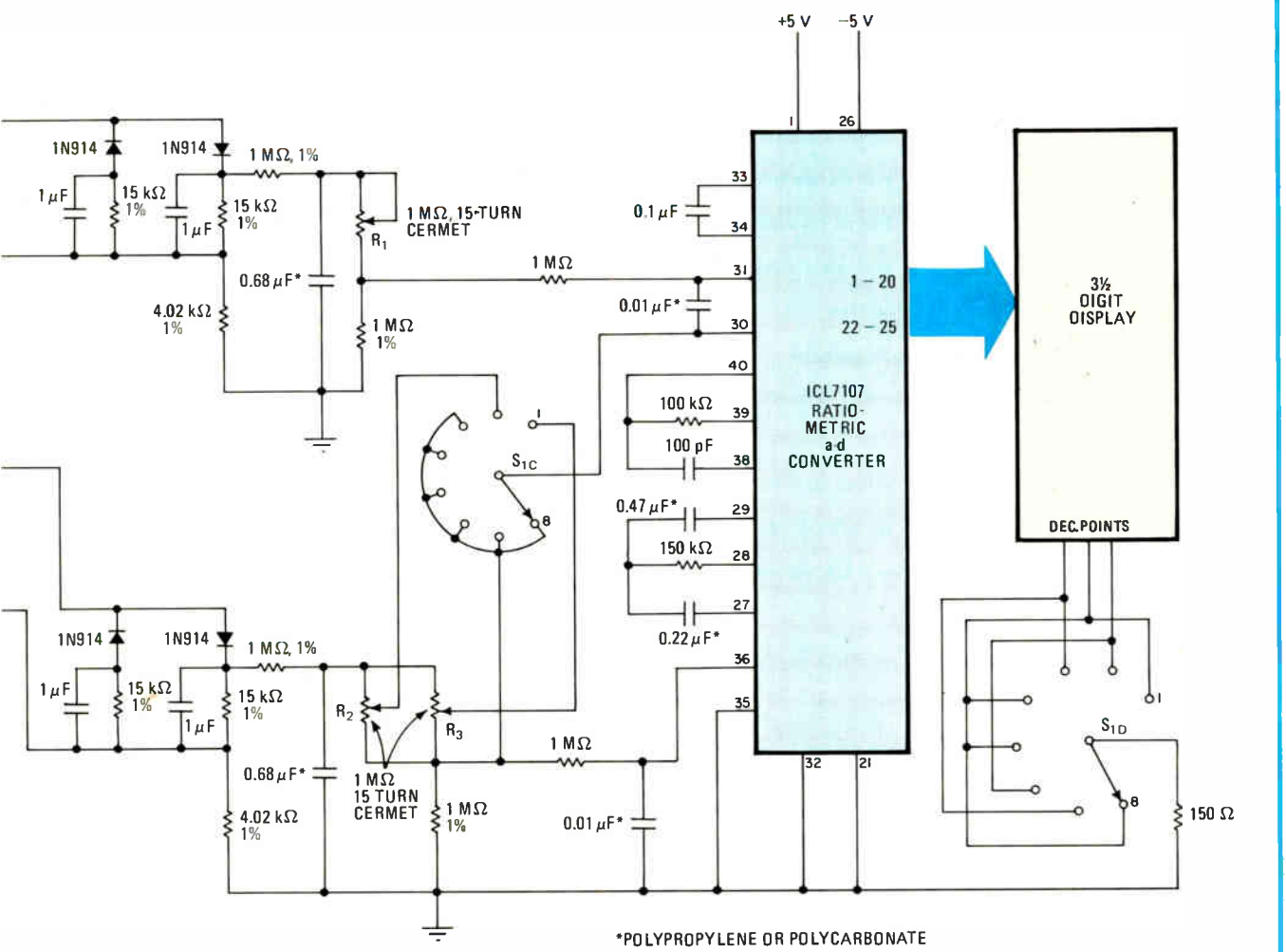
where R is the dc resistance of L_x, f is the test frequency, and e is the display indication divided by 1,000 and with the decimal point disregarded. Because f is varied appropriately with range and the Q of L_{ref} is greater than 100 at 1 kilohertz—coils are hand-wound on Amidon pot cores using the largest-diameter wire possible (see table)—the equation given above reduces to $L_x = L_{ref}e$ for almost all practical measurements. For example, the error in measuring a 1-millihenry inductor having a Q of only 0.1 at 1 kHz will be less than 1%.

The concept of measuring capacitance is similar. Potentiometers R_1, R_2, and R_3 are used to cancel out the effect of parasitic capacitance at the converter's input terminals so that the display will read zero with no test capacitor connected. When that is done, the display will read $1{,}000C_x/C_{ref}$.

Construction is not critical. The only exception to that is the wiring to the input terminals, which should be kept reasonably short.

The calibration procedure for the circuit is straightforward. S_1 is set to 2 microfarads full scale and R_1 is adjusted for a zero display reading. Then S_1 is placed in the 20-nanofarad full-scale position and R_2 adjusted for a zero reading. Finally, the switch is set in the 2-nF full-scale position and R_3 adjusted for a zero display reading. In the prototype tested, no readjustment was necessary over a nine-month period of normal use, and accuracy was maintained to within 1%. □

Coils and capacitors. Ratiometric meter, easier to use than manual bridges and less expensive than digital types, measures inductances of reasonable Q over the 2-mH-to-2-H range and capacitances over the 2-nF-to-2-μF range to within 1%. Calibration, required for capacitance measurements, is easy and maintains long-term stability.



TRS-80 program helps to load cassette data twice as fast

by H. Lee
Dover Heights, New South Wales, Australia

Radio Shack's TRS-80 level 2 personal computer is becoming increasingly popular for simple control tasks such as monitoring instruments that measure various physical quantities. Unfortunately, however, users who lack the expensive disk operating system must store and call data on or from the standard cassette tape source, and the machine's 500-bit-per-second read and write speeds are often too slow to satisfy the average engineer, especially if the program is 12-K bytes long or longer. But the short program shown here allows machine-language software to run on the computer at twice the speed (1,000 b/s) without any change having to be made to the hardware.

The increase in speed is achieved by altering the machine's standard read and write formats. The original

TRS-80 PRINTER LISTING FOR FAST TAPE LOADING

```
00010  START   EQU   5000H    ; start of program, may be changed
00020  NDBYTS  EQU   2000H    ; no. of bytes in user's program
00030          ORG   7F60H    ; location of 1000 bauds drivers
00040  FASWR   LD    HL,START ; start of user's program
00050          LD    DE,NDBYTS ; no. of bytes to write
00060          XOR   A        ; zero accumulator
00070          CALL   212H    ; switch on tape recorder
00080          CALL  287H     ; write out tape leader
00090  W1      LD    A,(HL)   ; put byte into accumulator
00100          CALL  WRITE    ; write byte at 1000 bauds to tape
00110          INC   HL       ; next byte
00120          DEC   DE       ; decrease count
00130          LD    A,E      ; check if completed
00140          OR    D
00150          JR    NZ,W1    ; all bytes completed ?
00160          CALL  1F8H     ; yes, switch off tape recorder
00170          JP    6CCH     ; go to Basic interpreter
00180  ;
00190  ; WRITE ROUTINE
00200  ;
00210  WRITE   PUSH  HL       ; save registers HL
00220          PUSH  DE       ; and DE
00230          LD    C,9      ; transfer 9 bits (1 synch and 8 bits)
00240          LD    D,A      ; save byte in register D
00250  W2      CALL  PULSE    ; write pulse on tape
00260  W3      DEC   C        ; decrease count
00270          JR    Z,W4     ; all 9 bits done ?
00280          LD    A,D      ; restore data byte
00290          RLCA           ; rotate data byte
00300          LD    D,A      ; save accumulator
00310          JR    C,W2     ; if carry then it's 1
00320          LD    B,54H    ; delay here for 0 bit
00330          DJNZ  $
00340          JR    W3       ; return for more bits
00350  W4      POP   DE       ; restore registers DE
00360          POP   HL       ; and HL
00370          RET            ; subroutine ends
00380  ;
00390  ; PULSE SUBROUTINE
00400  ;
00410  PULSE   PUSH  AF       ; save registers AF
00420          LD    HL,0FC01H ; set a positive pulse to tape
00430          CALL   221H    ; output to tape
00440          LD    B,5
00450          DJNZ  $        ; for about 50 microseconds
00460          LD    HL,0FC02H ; set a negative pulse to tape
00470          CALL   221H    ; output to tape
00480          LD    B,5
00490          DJNZ  $        ; for about 50 microseconds
00500          LD    HL,0FC00H ; set tape output to zero level
```

system inserts 8 sync-reference bits for every byte of data. Here, only 1 sync bit is used for each byte. The bit time has also been shortened slightly. These fast tape drivers have worked reliably with the original tape recorder supplied with the machine, provided Radio Shack's XRX-111 hardware fix for tape loading has been implemented.

Users need only specify the program with the starting memory address of interest and the length of the routine they wish to convert. Providing a jump-to-execute address is optional, but the default address will initiate a return to the Basic interpreter. As for the drivers, they may be either loaded using a monitor program such as T-BUG or entered using the poke command. The drivers are location-independent so they may be loaded anywhere in free memory.

The tape can be saved or loaded using a jump to FASWR or FASRD, respectively. It would also be advantageous to note the location of the software driver for the fast read (FASRD). This would facilitate reliable power startup. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $75 for each item published.

```
00510           CALL   221H
00520           LD     B,32H      ;delay after each pulse
00530           DJNZ   $
00540           POP    AF         ;restore A
00550           RET
00560   ;
00570   ;1000 BAUDS LOAD DRIVER
00580   ;
00590   FASRD   LD     HL,START   ;start of program
00600           LD     DE,NOBYTS  ;no. of bytes
00610           XOR    A          ;zero accumulator
00620           CALL   212H       ;switch on tape recorder
00630           CALL   296H       ;look for tape leader
00640   R1      CALL   READ       ;read 1 byte from tape
00650           LD     (HL),A     ;store it in memory
00660           INC    HL         ;point to next memory
00670           DEC    DE         ;decrease count
00680           LD     A,E
00690           OR     D
00700           JR     NZ,R1      ;continue if not completed
00710           JP     6CCH       ;go to Basic interpreter
00720   ;
00730   ;READ SUBROUTINE
00740   ;
00750   READ    PUSH   HL         ;save registers HL
00760   R2      IN     A,(0FFH)   ;get byte from tape
00770           RLA               ;rotate until synch bit appears
00780           JR     NC,R2      ;synch bit ?
00790           LD     B,0AH      ;delay
00800           DJNZ   $
00810           CALL   21EH       ;reset input flip-flop
00820           LD     B,3AH      ;delay after first bit
00830           DJNZ   $
00840           LD     C,8        ;read remaining 8 bits
00850   R3      PUSH   AF         ;save accumulator
00860           LD     B,21H      ;delay for next byte
00870           DJNZ   $
00880           IN     A,(0FFH)   ;read next byte from tape
00890           LD     B,A        ;save bit in register B
00900           CALL   21EH       ;reset input flip-flop
00910           POP    AF         ;restore byte
00920           RL     B          ;add bit from carry
00930           RLA
00940           LD     B,2AH      ;delay before next byte
00950           DJNZ   $
00960           DEC    C          ;decrease bit count
00970           JR     NZ,R3      ;again if not completed
00980           POP    HL         ;restore registers HL
00990           RET
01000           END
```

Engineer's newsletter

Keeping fat Cerdips out of trouble

With the increase in width of Cerdip ceramic and glass dual in-line packages, the center-to-center spacing of the leads along the sides is running to as much 0.325 in., notes Richard Grubb, corporate vice president of marketing, Augat Inc., Attleboro, Mass. That presents a serious interface and reliability problem when the Cerdips are plugged into sockets designed for 0.300-in. centers. Even when soldered directly into a pc board, they run **a high risk of having the seal between the shoulder of the lead and the ceramic broken,** thus disturbing their hermeticity. The cure for this situation, according to Grubb, is to hold to the Joint Electron Device Engineering Council's specification for this Cerdip dimension—0.300 ± 0.010 in.

6800, 8080, and Z80 testing for hire

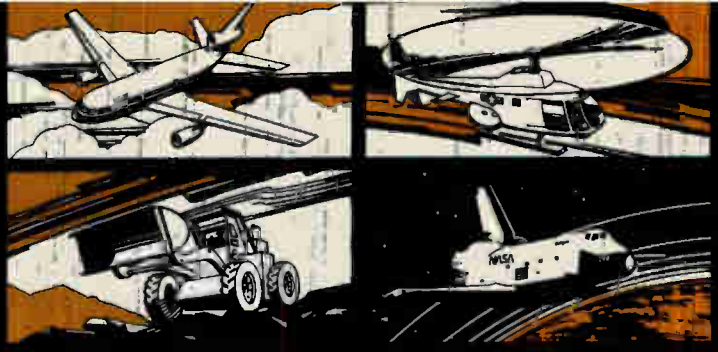
If testing the 6800, 8080, or Z80 microprocessors is beyond the capabilities of the automatic test equipment you have in house, a new service furnished by Solid State Testing Inc. should interest you. The company uses a Fairchild Sentinel system to put these devices through a complete set of functional and dynamic tests, which consist of **a run through the instruction set plus ac and dc electrical measurements selected from the manufacturer's data sheets.** For other tests, often an existing program can be modified at nominal cost to provide the exact testing required. For more information, contact James R. DiGiacomo, vice president of marketing, Solid State Testing Inc., 56 Middlesex Turnpike, Burlington, Mass. 01803; (617) 272-0972.

Diffusion furnaces can be safer

Whether because of improperly connected supply lines, broken gas inlets, or inaccurate temperature measurements, semiconductor diffusion furnaces that use an oxygen-hydrogen atmosphere are all too prone to explode, destroying thousands of dollars' worth of wafers. Application note 93-00-070-09 from Honeywell Inc's. Process Control division says you can reduce that risk by installing its flame detector system, which checks that the furnace flame is present throughout the entire thermal oxidation cycle. The flame-detection circuit is energized when the hydrogen or hydrogen-oxygen valve(s) are open. If the flame does not develop in a preset time, **the detector closes the hydrogen valve.** Then if the flame fails subsequently, the system sounds an alarm. For further information, contact the division, M S. 436, 1100 Virginia Dr., Fort Washington, Pa. 19034.

How to move into management

Both the engineering manager with one to five years of experience and the engineer who wishes to advance to the management stage will find that a two-day program from Battelle Seminars and Studies Program called "The Engineer As a Manager" will aid in their professional development. The course will cover such topics as: the five major responsibilities in engineering management; how to develop a strong working relationship with your superiors; **how to develop self-starters among your staff;** and how to communicate ideas clearly and acquire the needed feedback. The course will be given in Denver, June 15–16; Boston, June 18–19; and St. Louis, July 16–17. The fee for the course is $495. For additional information, contact Battelle Seminars and Studies Program, 4000 N. E. 41st St., P. O. Box C-5395, Seattle, Wash. 98105. **-Jerry Lyman**



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For more information on any product in our full line, contact your Cutler-Hammer Aerospace Products Specialist or distributor—they know your business. And, write for our free catalog. Eaton Corporation, Aerospace Control/Systems Division, 4201 N. 27th St., Milwaukee, WI 53216.

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ADVANTEST by Takeda Riken. The new generation in LSI/VLSI testing.

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(ADVANTEST was developed in cooperation with N.T.&T. Musashino Electrical Communication Lab.)

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If you're looking for a functional analog/digital tester that can test at a full 5MHz, our 70/76 gives you unprecedented flexibility.

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The analog section provides complete software control of all signal switching paths and instruments through a standard IEEE 488 Bus. The digital section uses a stored program

technique for real time testing of all microprocessors, RAMs, ROMs and dynamic devices. And each pin is backed by 4K RAM for high-speed parallel patterns up to 512 pins.

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For more information on Series 70 test systems, write or call Fairchild Test Systems Group, Fairchild Technical Center, 3 Suburban Park Drive, Billerica, MA 01821; (617) 663-6562, TWX: 710-349-7580.

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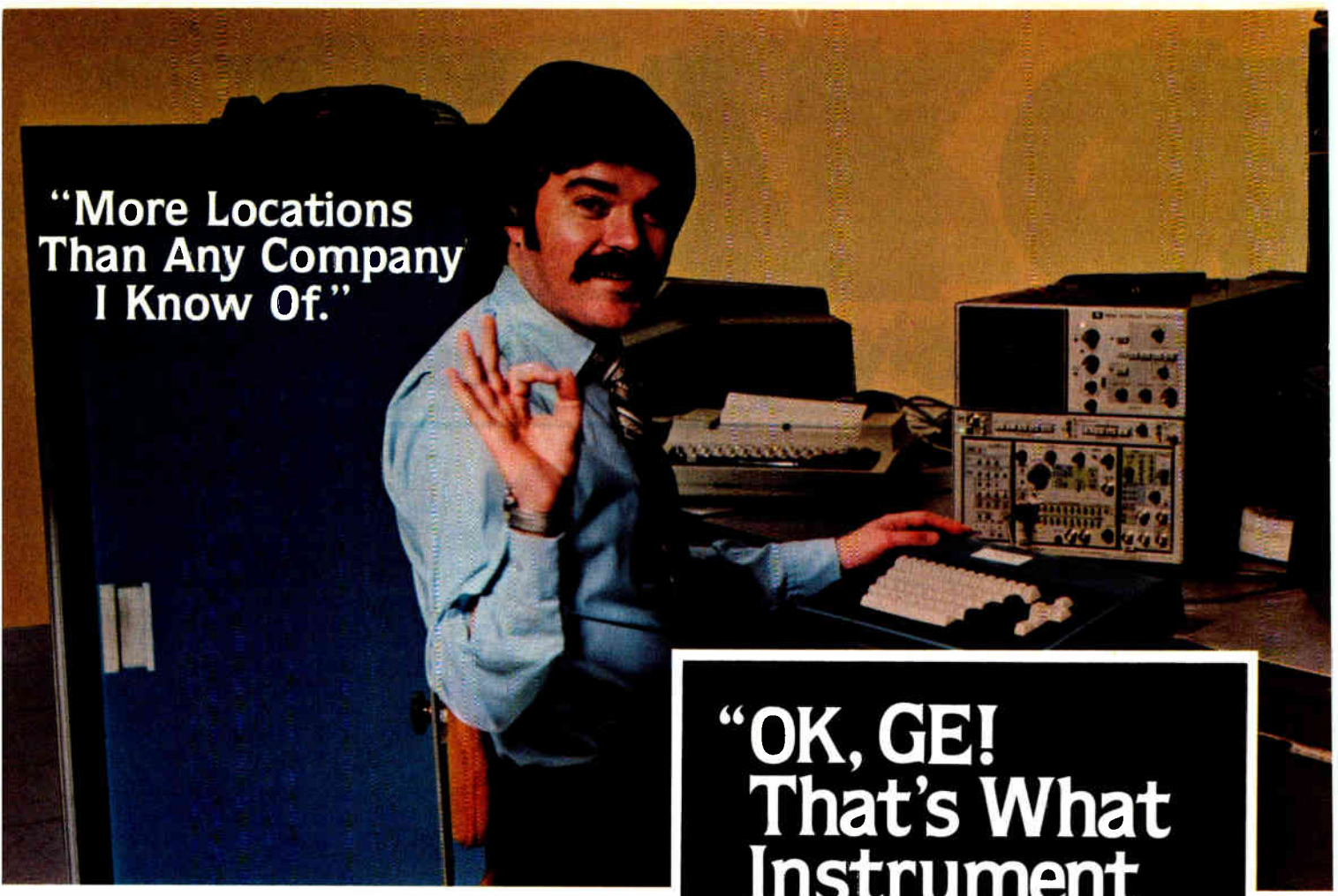

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Circle 168 on reader service card

Analyzer tests bare and loaded boards

Performing continuity, functional, and many in-circuit tests, system supports up to 64-K points on four fixtures

by Bruce LeBoss, San Francisco regional bureau manager

Manufacturers of circuit-board systems have traditionally offered users continuity testers for either bare or loaded boards. In the latter case, users have had a choice of either functional or the more expensive in-circuit testers. A new circuit-board analyzer from Fluke Automated Systems Inc. performs functional tests on both bare and loaded circuit boards, as well as most of the tests performed by in-circuit testers costing two to three times as much.

The 3200A is controlled by an iSBC 86/12A, an 8086-based 16-bit single-board computer from Intel Corp., backed by 64-K bytes of random-access memory. This test processor, as it is called, detects such manufacturing defects as opens, shorts, and resistive leakage on both bare and loaded circuit boards, as well as on more complex subassemblies. Engineers at the subsidiary of John Fluke Manufacturing Co. say the 3200A can support up to 65,536 test points.

The system has a test speed of 10,000 to 100,000 points per second and "can test a typical loaded board in one tenth of a second, which makes it the fastest circuit-board tester available on the market," claims product planner Dave Sellinger. Such speeds are attained using Fluke's proprietary Quick-Chip scanning switch circuits. Each of these custom complementary-MOS chips has 32 pairs of intelligent solid-state switches that are used to check each test point's integrity in relation to all the rest with just one software instruction.

The 65,536 test points that the 3200A can support are split among four fixtures, "all testing the same or different programs simultaneously," Sellinger says. Each fixture has its own dedicated remote-control panel with a 35-column fault printer, status indicators, a data-entry keypad with four-digit liquid-crystal display, pass-fail lamps, and a cycle-test key for easy fixture debugging.

To be formally introduced at the Automatic Test Equipment Seminar and Exhibit in Boston, June 8–11, the 3200A can generate and edit its own test programs, with the help of an off-line programming station. Based on an Intel 8085 8-bit microprocessor, this station consists of a keyboard, a cathode-ray tube, and 64-K bytes of RAM, as well as dual 8-in. floppy disks storing 2.5 megabytes, half of which is available to the user for test program storage.

The 3200A's menu-driven displays make it easy to select from its software capabilities. The system software can assign individual alphanumeric names to test points. An optional "learn" probe may be used in this process; it is placed in contact with a test point as the name is entered on the keyboard. "This capability allows easy random wiring of the fixtures, with assignment of the point via system software." The test heads of existing test systems

New products

"are [physically] wired from an interface block to the spring-loaded probes, according to a wire list"—an arrangement that makes it difficult to accommodate changes in test programs, says Sellinger.

Besides testing circuit boards, the 3200A also can test backplanes, card cages, cables, and harnesses. Different UUT types can be tested simultaneously on different stations. These subassembly tests can be performed with daisy-chained paddleboards inserted into the connectors that form the motherboard. Each paddleboard consists of an extender card with a scan module installed and is connected to the adjacent paddleboard.

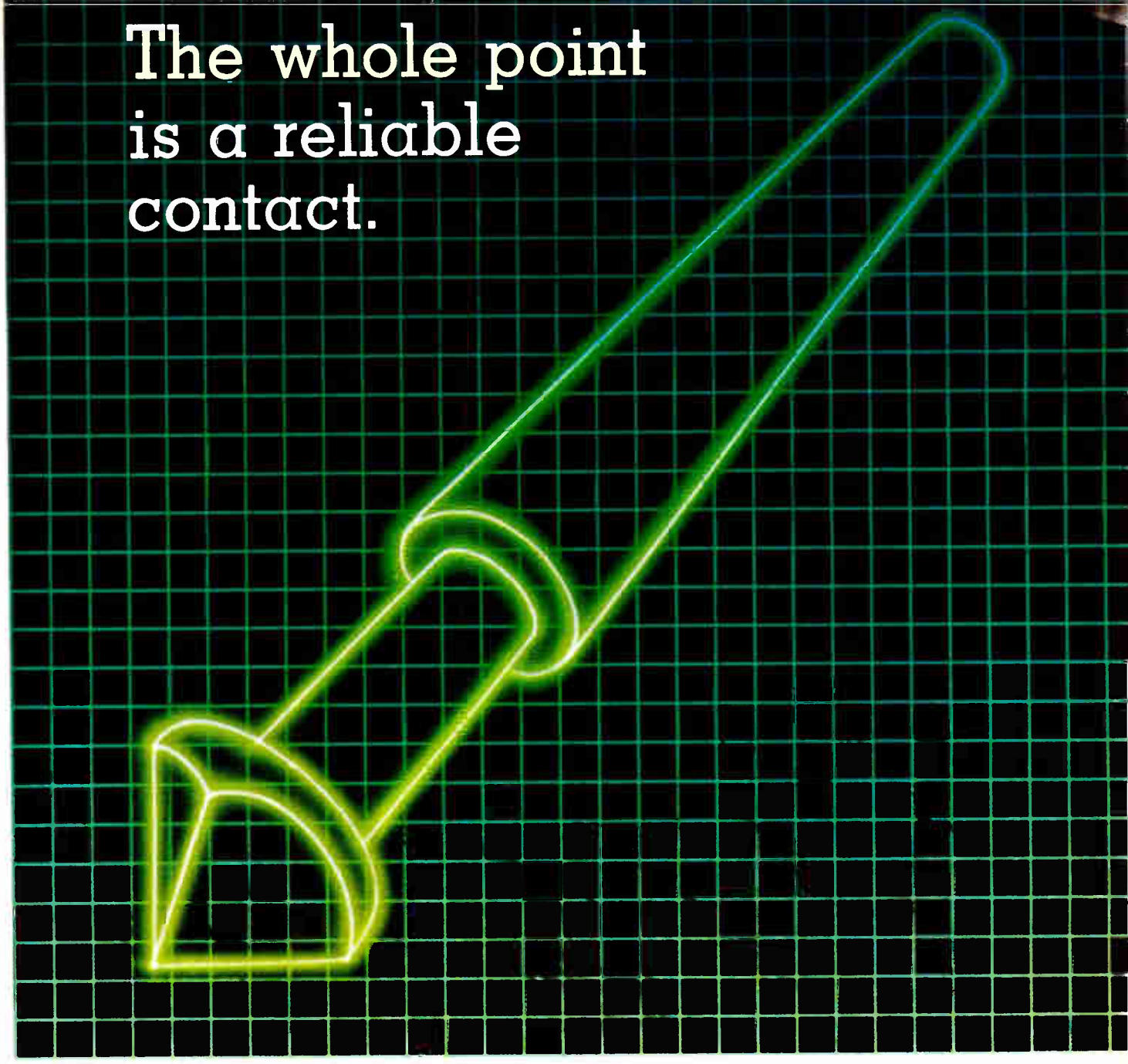
By using information about the semiconductor junction characteristics of a loaded circuit board, the 3200A will detect and report faults caused by missing, backward, and wrong components. These may be integrated circuits, diodes, transistors, zener diodes, or any other components that exhibit low-voltage breakdown characteristics, says Sellinger. The stimulus voltage is programmable, as is the tolerance range for accepting a junction, so that components will not be damaged.

Classification. The 3200A has a programmable dual-threshold capability that automatically classifies continuity tests into three categories—opens, shorts, and leakage. For loaded boards, both opens and shorts can be programmed over the range of 50 to 10,000 Ω. For all other UUT types, opens are programmable over the 5-to-100-kΩ range, and shorts can be set from 50 to 6,000 Ω.

To be ready for shipping in October, the 3200A will be priced around $33,000 for a system with about 2,000 test points, one remote station, one off-line programming station, dual floppy disks, 64-K bytes of RAM, and the scanner electronics. Typical systems with a second remote station, an additional memory card with 32-K or 64-K bytes of RAM, plus additional scan electronics ($4 per test point), will sell for about $50,000.

Fluke Automated Systems Inc., 930 Clyde Ave., Mountain View, Calif. 94043. Phone (415) 965-0350 [338]

The whole point is a reliable contact.



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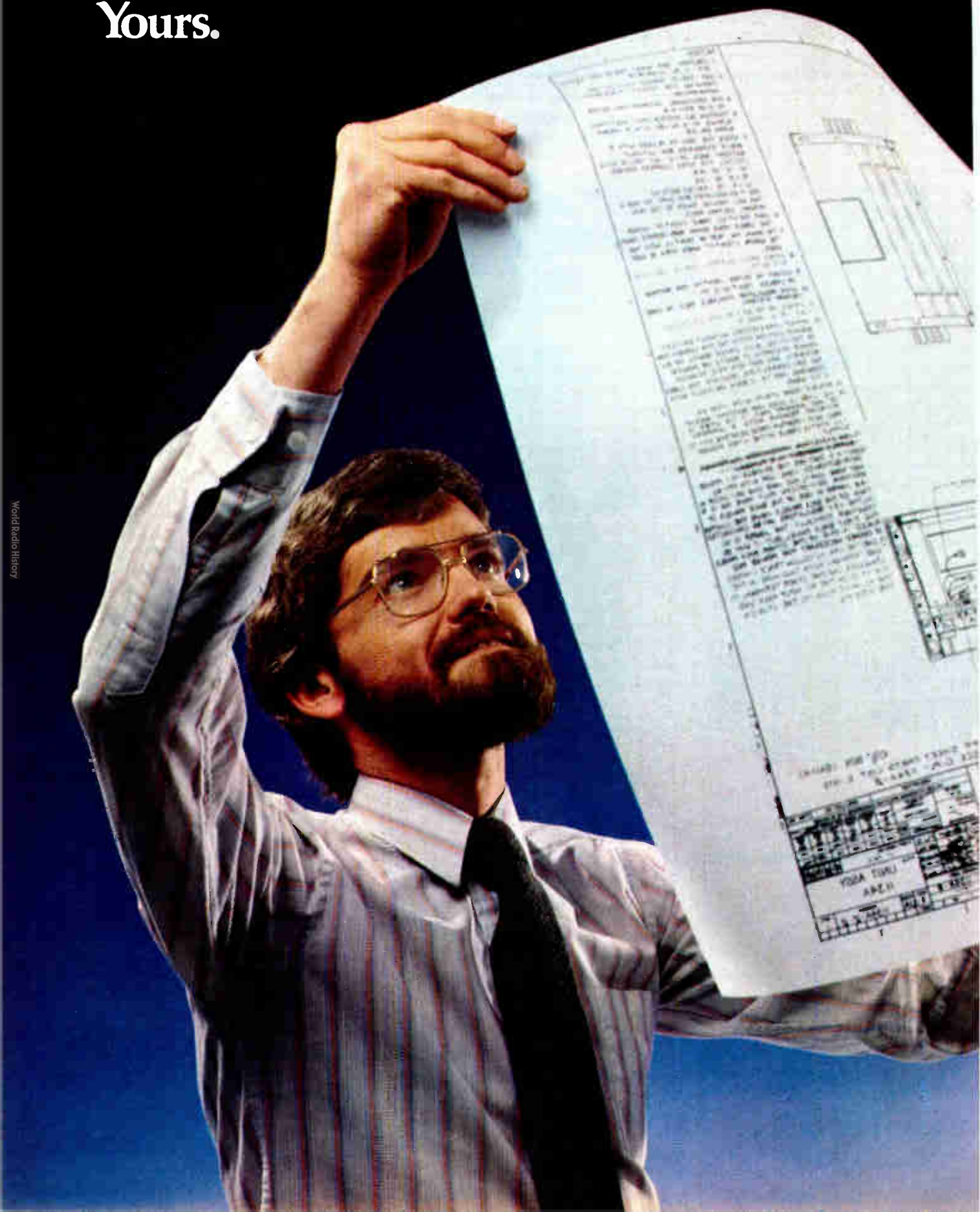

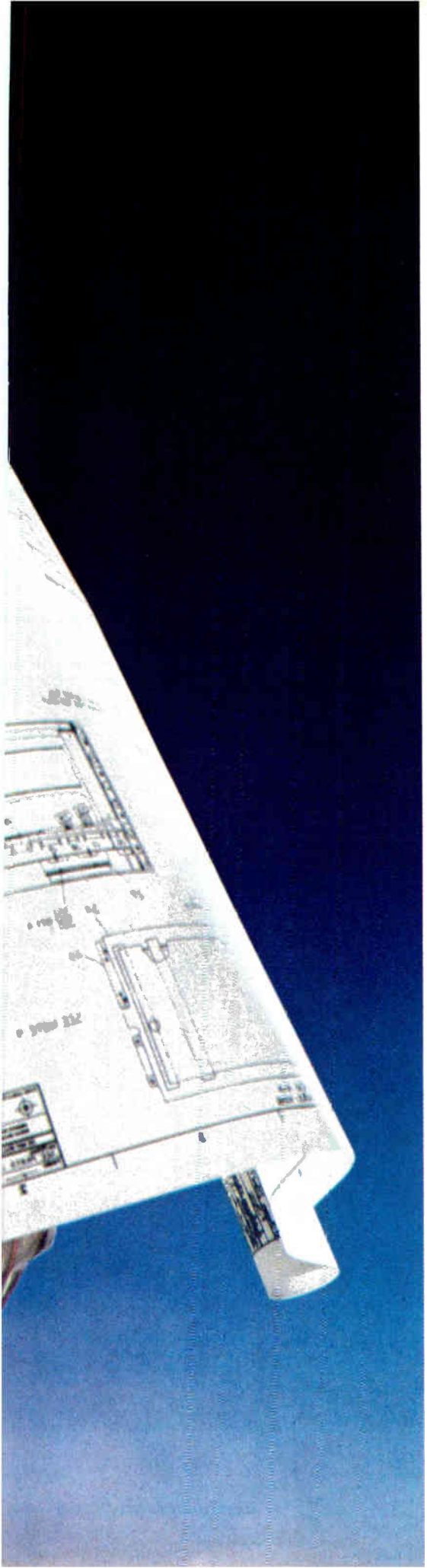

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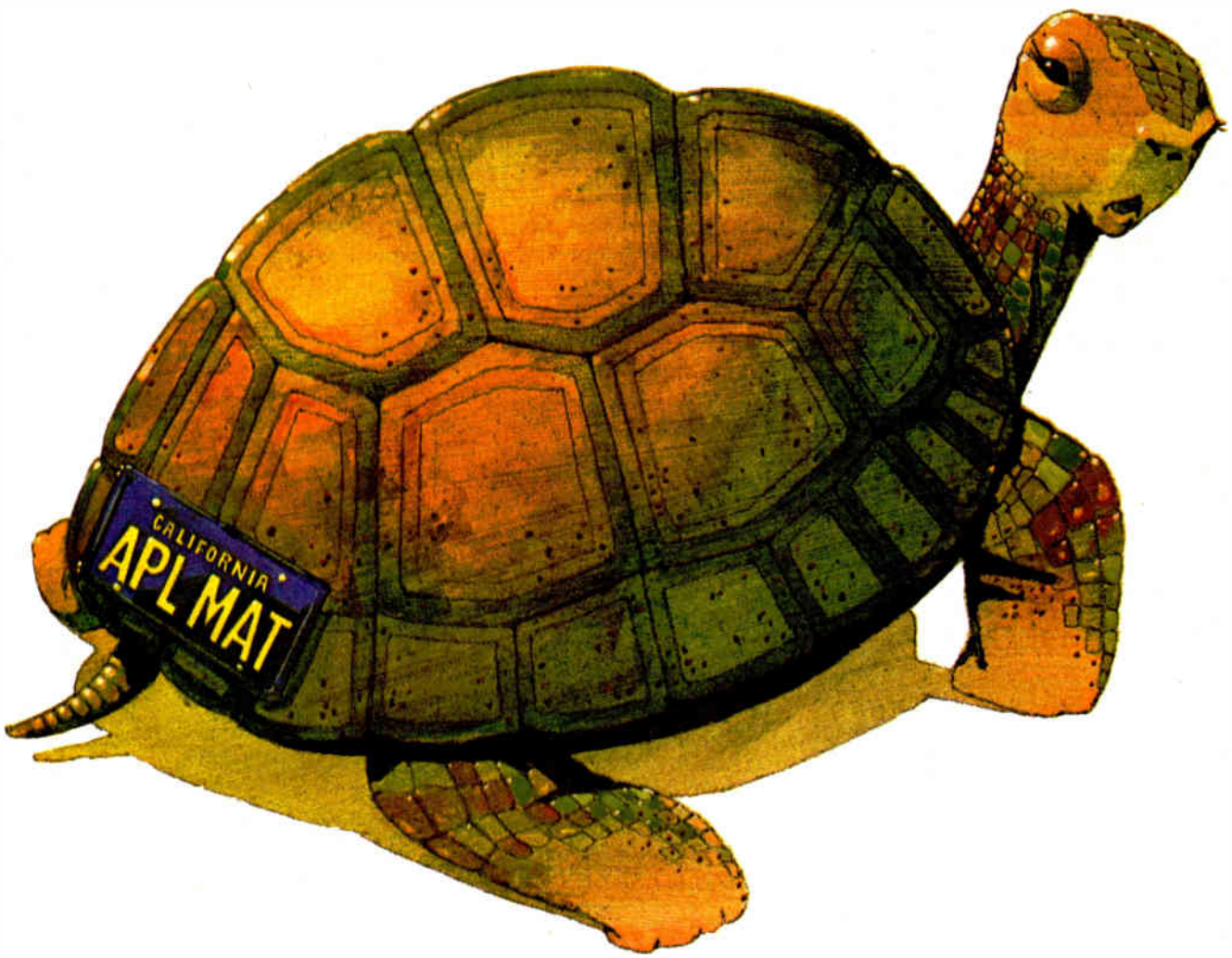
SORRY, WE'RE A LITTLE LATE WITH OUR PLASMA ETCHER, FOLKS



BUT AFTER MAY 18 EVERYONE ELSE WILL BE RUNNING TO CATCH UP WITH APPLIED MATERIALS' AME-8100 ION ASSISTED REACTIVE SPUTTERING ETCHER.

...An apology from APPLIED MATERIALS

Applied Materials apologizes to those who ordered a plasma etcher without knowing we were developing the AME-8100 Ion Assisted Reactive Sputtering Etcher. We can appreciate the disappointment you'll feel with the system you ordered when you see this revolutionary vertically loaded batch etcher and hear our guaranteed specs on uniformity, reproducibility and throughput. Then when you analyze the results the AME-8100 achieves in etching fine line geometries below the 2-micron range, you'll wonder if it isn't the manufacturer you ordered from who should be apologizing.

YOU (AND YOUR WAFERS) ARE CORDIALLY INVITED...

From May 18–21 we'll be having Open House to demonstrate the AME-8100 for those who haven't ordered a plasma etcher yet—and those who want to see what they missed. Come and *bring your wafers with you.* We're proud of our achievement and want to demonstrate it on the only wafers you care about. If you come on May 20, our engineers will also be conducting plasma etch seminars throughout the day. Call us at (408) 738-3600 and tell us which day is best for you.

Find out for yourself why the AME-8100 is the *one* plasma etcher that was worth waiting for.

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Applied Materials
3050 Bowers Avenue
Santa Clara, California 95051
(408) 727-5555.

Flexible PROM programmer costs $450

Controlled by a separate terminal, programmer can be reconfigured with DIP-sized wrapped-wire boards

by James B. Brinton, Boston bureau manager

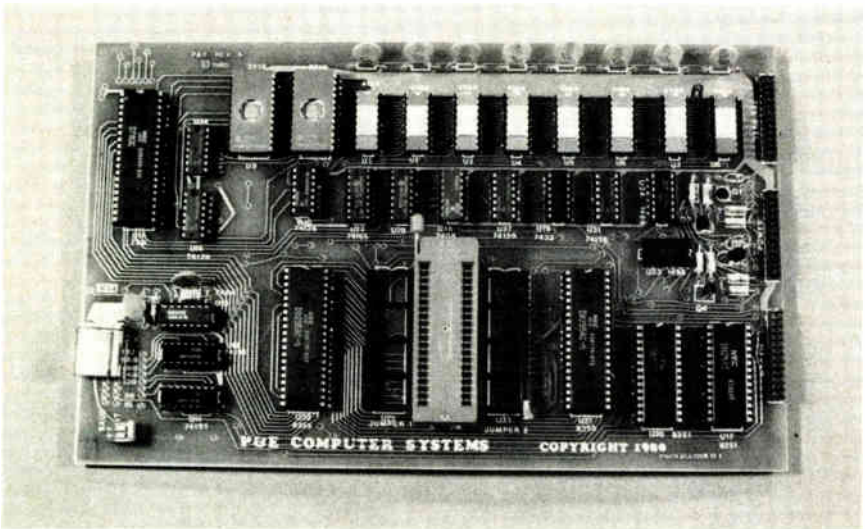
Almost every available programmable read-only memory should be grist for the Programmer from P&E Microcomputer Systems. And at $450 in single units, the Programmer may have the lowest price—and best price-performance ratio—in the programmer market.

The Programmer's design is based on the assumption that anybody programming a PROM or an erasable PROM already has some digital hardware on hand. The unit has been pared down for minimal redundancy and cost; there is no keyboard or keypad, no display or power supply. The Programmer is wired into benchtop or other available power supplies; it is controlled through two RS-232-C ports capable of data transfers as rapid as 19.2 kb/s.

The system can be used in three modes, depending on requirements and available equipment. In one mode, the Programmer communicates with any RS-232-C–compatible terminal, with the latter controlling the Programmer's firmware routines and the data to be burned into the PROM. Alternatively, the other RS-232-C port allows modem communication with a computer system that in turn can be programmed to handle the task and check the results through the Programmer's facilities. This mode would be especially valuable in short production runs or prototyping where PROM programs must be replicated rapidly with minimum risk of human error. In the computer-driven mode, fast file transfers take place in Intel hexadecimal format.

The Programmer can also make communication between a terminal and a host computer possible. When used with a cross assembler resident in the host, the Programmer can become the center of a low-cost mini-development system.

In contrast to programmers with keypads and light-emitting-diode displays, with the P&E device, the user has the flexibility offered by a full video terminal—probably one already on hand. P&E's programmer is Z80-based, uses 4-K bytes of random-access buffer memory, and stores its firmware in two 2716 E-PROMs. The latter also holds the protocols needed to program 15 standard types of ROMs and E-PROMs.



Rewire. Once a PROM's program has been established, it can be burned in with minimal effort—by entering a few keyboard commands. Adapting the programmer to a new PROM is only slightly more demanding. Instead of the expensive personality modules that characterize some PROM programmers, the only hardware that must be altered in the P&E system is a pair of jumper or profile cards—small assemblies that fit into 40-pin dual in-line sockets on either side of a familiar zero-insertion-force PROM socket. By running wrapped-wire jumpers across these tiny boards, almost any standard or nonstandard PROM can be accommodated in minutes. The small profile cards give the user complete control of pinout, control voltages, and timing sequences.

Though initial units will be offered with wrapped-wire profile boards, P&E expects to offer miniature printed-circuit profile boards for the most common PROMs, thus cutting set-up time to seconds.

As delivered, the Programmer supports the following E-PROMs: Texas Instruments TMS2708, 2716, 2516, 2564, and 2758; Intel 2704, 2708, 2716, 2732, 2764, 2758, 8741, and 8755. Price is $450 each with quantity discounts available.

P&E Microcomputer Systems, P. O. Box 2044, Woburn, Mass. 01888. Phone (617) 944-7585 [339]

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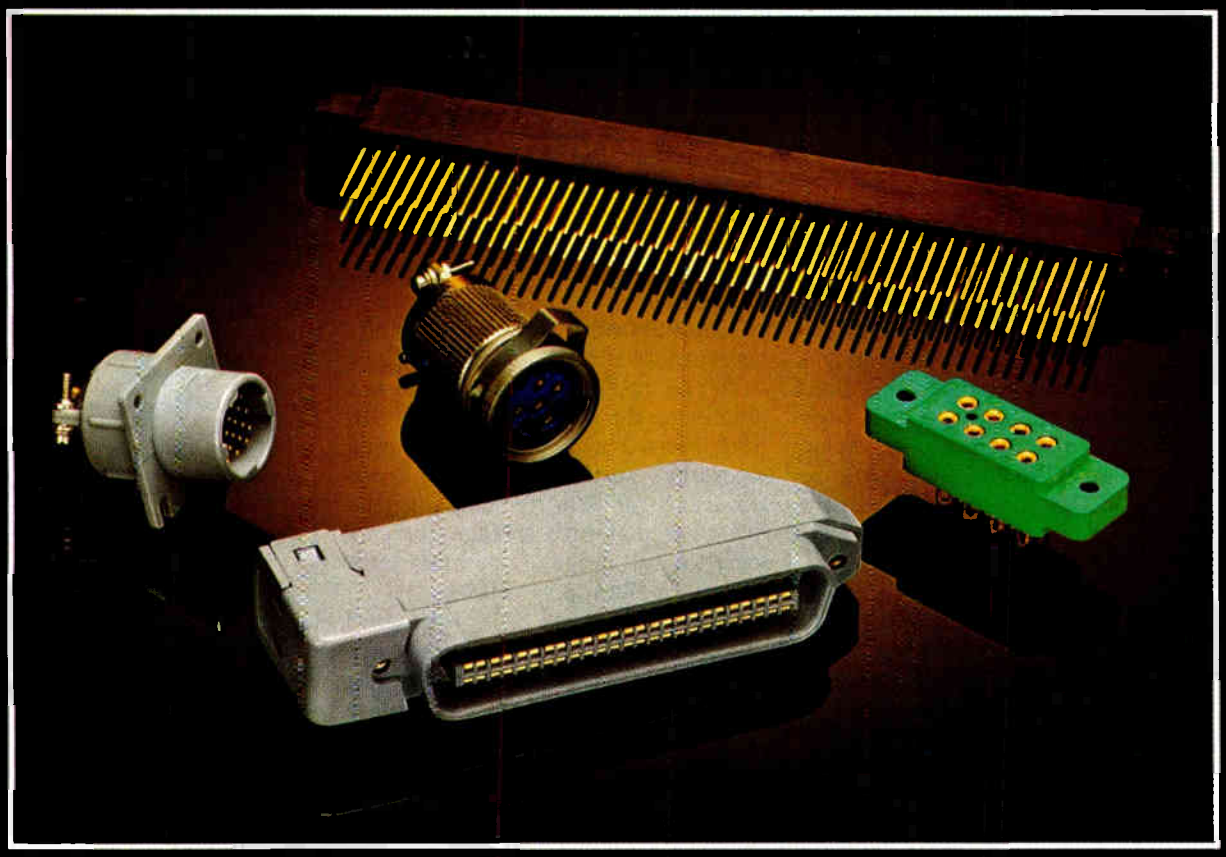

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Circle 179 on reader service card

Semiconductors

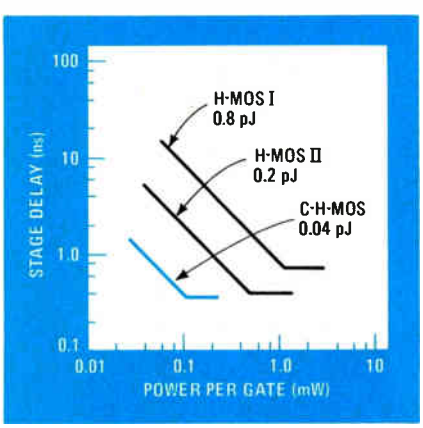
4-K C-MOS RAMs access in 100 ns

4-K-by-1-, 1-K-by-4-bit static random-access memories reduce standby power use

The 5104 and 5114 4-K static random-access memories are the first in a line of micropower memory components to be manufactured by Intel Corp. using its new complementary-MOS technology. This technology is named C-H-MOS because it is a direct extension of the chip maker's high-performance n-channel MOS structure, H-MOS; indeed, C-H-MOS requires just a few processing steps more than the scaled-down H-MOS II [*Electronics*, Dec. 4, 1980, p. 39].

Both in standard 18-pin packages, the 5104 is organized as 4,096 by 1 bit and the 5114, as 1-K by 4 bits. With 100-, 150-, and 200-ns access-time selections, they are compatible—in terms of pinout and speed—with the company's 2114A and 2141 H-MOS static RAMs.

However, even though they operate at two to five times the speed of typical C-MOS static RAMs, the new memories consume about half the standby power. Moreover, the 5114 incorporates a special power-off feature that reduces power dissipation to microwatt levels and, unlike ordinary C-MOS devices, achieves this with TTL-level input signals. So a major application for the RAMs is likely to be in computer systems that use batteries for back-up power.



Forty femtos. The power-delay product achieved by Intel's complementary-H-MOS process in the 5104 and 5114 static random-access memories is a mere 0.04 pJ.

All-static peripheral circuits are used on the 5104 and 5114 because many of the system design problems associated with C-MOS memories stem from the use of dynamic peripheral circuitry. Although dynamic circuitry reduces power dissipation at low operating rates, such frequencies characterize older system designs.

The fully static integrated circuits ask for less current throughout their wider operating frequency range and eliminate the noise associated with the internal switching of dynamic operation. Further, Intel opted to use six-transistor storage cells in the RAMs to minimize leakage currents over the full range of operating temperatures and supply voltages.

The conventional 6514 4-K C-MOS RAM draws 7 mA at 1 MHz, 14 mA at 2 MHz, and cuts power consumption by a factor of seven on standby, assuming operation at 25°C and a 50% duty cycle, with a nominal 5-V supply. Not only does the 5114 reduce standby power use significantly, to 0.01 mA, but it can be employed in higher-performance systems at an operating frequency of 5 MHz, at which the 6514 often cannot be used. An active 5114 draws 7 mA whether operating at 1, 2, or 5 MHz. The new devices also need less idle current than available 16-K C-MOS static RAMs.

Unusual. The special power-off feature of the 5114 enables it to outperform both the conventional 4-K C-MOS RAMs and 16-K chips like the 6116 in large, modular memory systems. For example, assuming that such a system must be expanded from 2-K bytes to 64-K bytes of storage capacity in 2-K-byte increments, at the 2-K-byte level, 5114 or 6116 static RAMs would both dissipate about 20 mA of total current and 6514s would use about 30 mA.

But while the power consumption of the 5114 system remains at about

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New products

20 mA as storage capacity is increased to 64-K bytes and as the clock frequency is cranked up to the 5-MHz level, the 6116s would burn about 140 mA under these conditions. And if 6514s are used, 140 mA would be drawn with only 32-K bytes at 2 MHz.

Samples of the 5104 are available now with production scheduled for the second half of this year. In 100-piece lots, pricing for the 5104 has been set at $11.00, $10.20, and $6.80 for the 100-, 150-, and 200-ns versions (the P5104-10, -15, and -20), respectively. Samples of the 5114 will be available within three months—along with pricing—with third-quarter production scheduled.

Intel Corp., 19440 S. W. Shaw Ave., Aloha, Ore. 97005. Phone (503) 642-6344 [411]

Family gains 16-K RAMs, Schottky PROM series

A family of 16-K dynamic random-access memories and four Schottky TTL programmable read-only memories have been added to Fujitsu Microelectronics' line of integrated circuits. The MB8117 and MB8118 n-channel MOS RAMs are both available with either a 100-ns access time and a 235-ns cycle time or a 120-ns access time and a 270-ns cycle time. Their maximum dissipation is 182 mW (active) and 19.5 mW (standby), and their voltage tolerance is ±10% on a 5-V power supply. Housed in a standard 16-pin dual in-line package, they have an on-chip bias generator, TTL-compatible inputs, and Jedec-approved pinout, plus read-modify-write, row-address-strobe–only ($\overline{\text{RAS}}$-only) refresh, hidden refresh, and page-mode capability. In addition, the 8117 has an automatic-refresh function.

The PROM family consists of the MB7122H, -7128H, -7132H, and -7138H, which are organized as 1 K and 2 K by 4 bits and 1 K and 2 K by 8 bits, respectively. The H series of PROMs have a 10-ns faster access time than the earlier E series of PROMs. They feature low power dissipation; a +5-V power supply requirement; programmability by Data I/O's and other leading programmers; low-current pnp inputs; three-state outputs and chip-enable leads for simple memory expansion; and Fujitsu's diffused eutectic aluminum process technology for maximum reliability.

Fujitsu Microelectronics, 2945 Oakmead Village Court, Santa Clara, Calif. 95051 [413]

Controller supports standard communications protocols

The 8274 serial data-communications controller can operate in an asynchronous, byte-synchronous, or bit-synchronous mode, having been designed for multiple-protocol, high-speed system applications.

The 8274, a 40-pin chip fabricated in Intel's high-performance MOS (H-MOS) technology, has an 880-kb/s data rate in its standard version. It features two full-duplex transmitter/receiver channels as well as a comprehensive interface for the bus structures of Intel's MCS-48, −85, and iAPX families. The integrated circuit's general programmable functions include clock rate multiples of 1× to 64×; combinations of polled, ready, interrupt, and direct-memory-access handshake modes; and assignments of four DMA handshake channels to the two transmitters and two receivers.

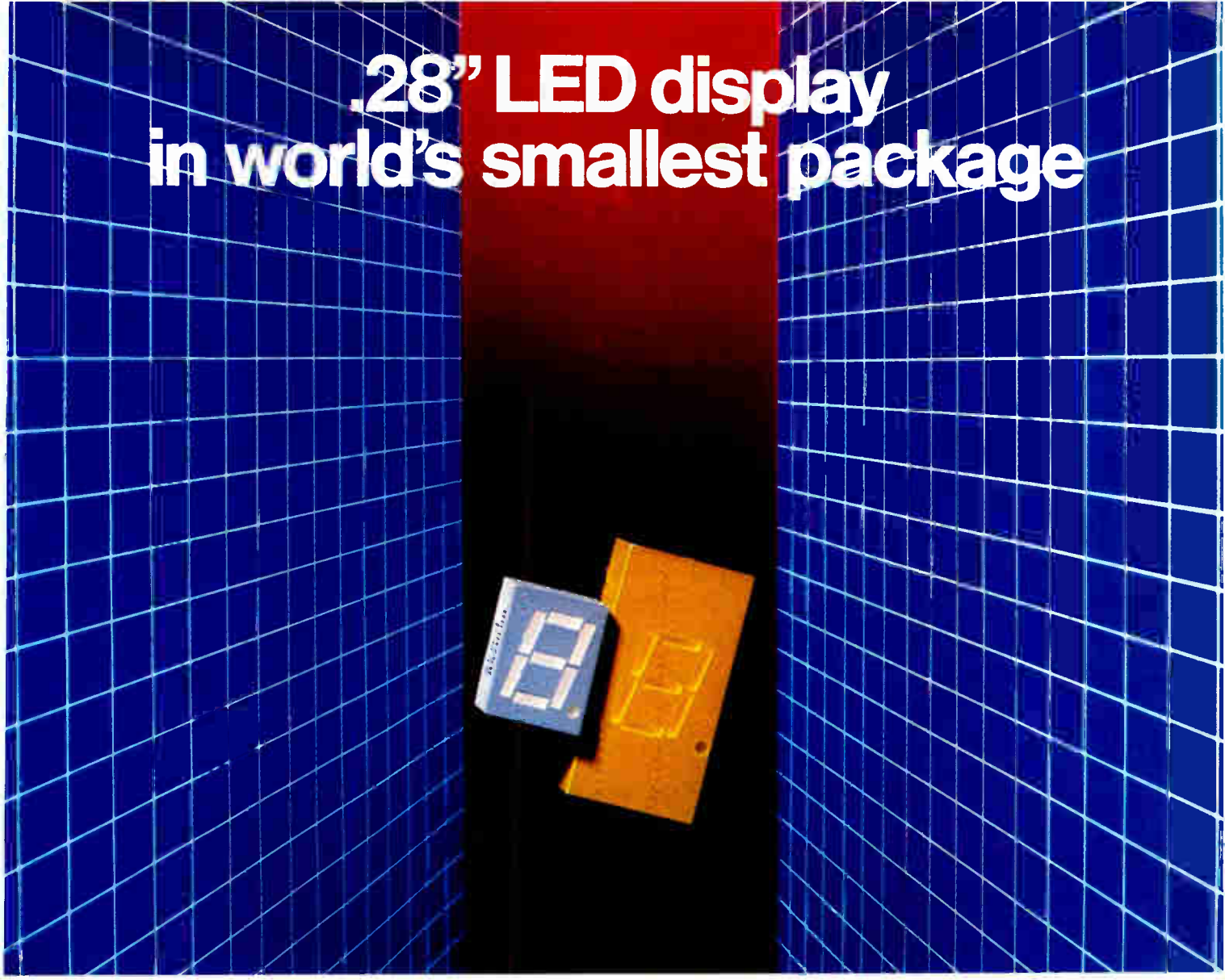
The controller is priced at $30.30 in quantities of 100. Deliveries will begin in June.

Intel Corp., 2625 Walsh Ave., Santa Clara, Calif. 95051. Phone (408) 987-7465 [415]

Array devices integrate custom circuits

Ten arrays with a rating of 20-V maximum and three arrays with a 40-V maximum rating make it possible to integrate custom circuits rapidly and at a low price. The Uniray (universal array) devices include 20-, 100-, and 200-mA npn transistors, lateral and vertical pnp transistors, Schottky diodes, and a wide selec-

.28" LED display in world's smallest package

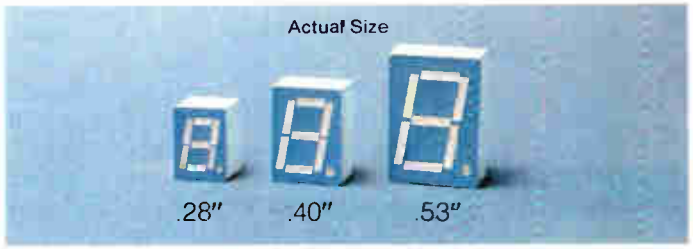


Shown above is the new .28" LED display VS the standard .3" display.

It's one of three compact Siemens digits available from Litronix.

When we became affiliated with Siemens, we joined forces to form the world's broadest and most innovative line of opto-electronic devices.

For example, we can now offer this family of extremely compact single digit displays which are less than one half the size of standard .3" displays on the market.



The HD 1075 (C.A.) and HD 1077 (C.C.) single digit LED display is a full 7mm (.28"), and the package is only 10mm x 7.6mm. On boards where space is tight and every little millimeter counts, our .28" digit will brighten a designer's eyes.

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The light gray face of Siemens displays enhances the on/off contrast ratio. And they are available in red, orange, yellow and green.

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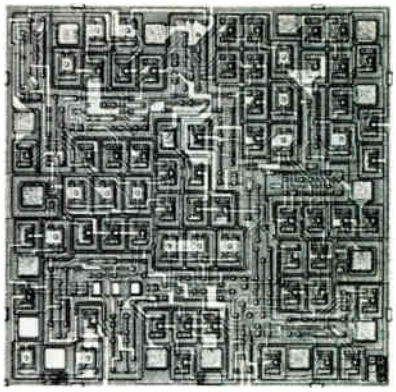
New products



tion of diffused resistors. They can be used in interface circuits, oscillators, biasing circuits, voltage regulators, amplifiers, comparators, and active filters.

Uniray layout worksheets, a 200-times enlargement of the actual Uniray provided by the company, enable the designer to sketch his metalization requirements. From this sketch the company will perform the final metal masking step, package and test the circuits, and ship evaluation quantities within five to seven weeks.

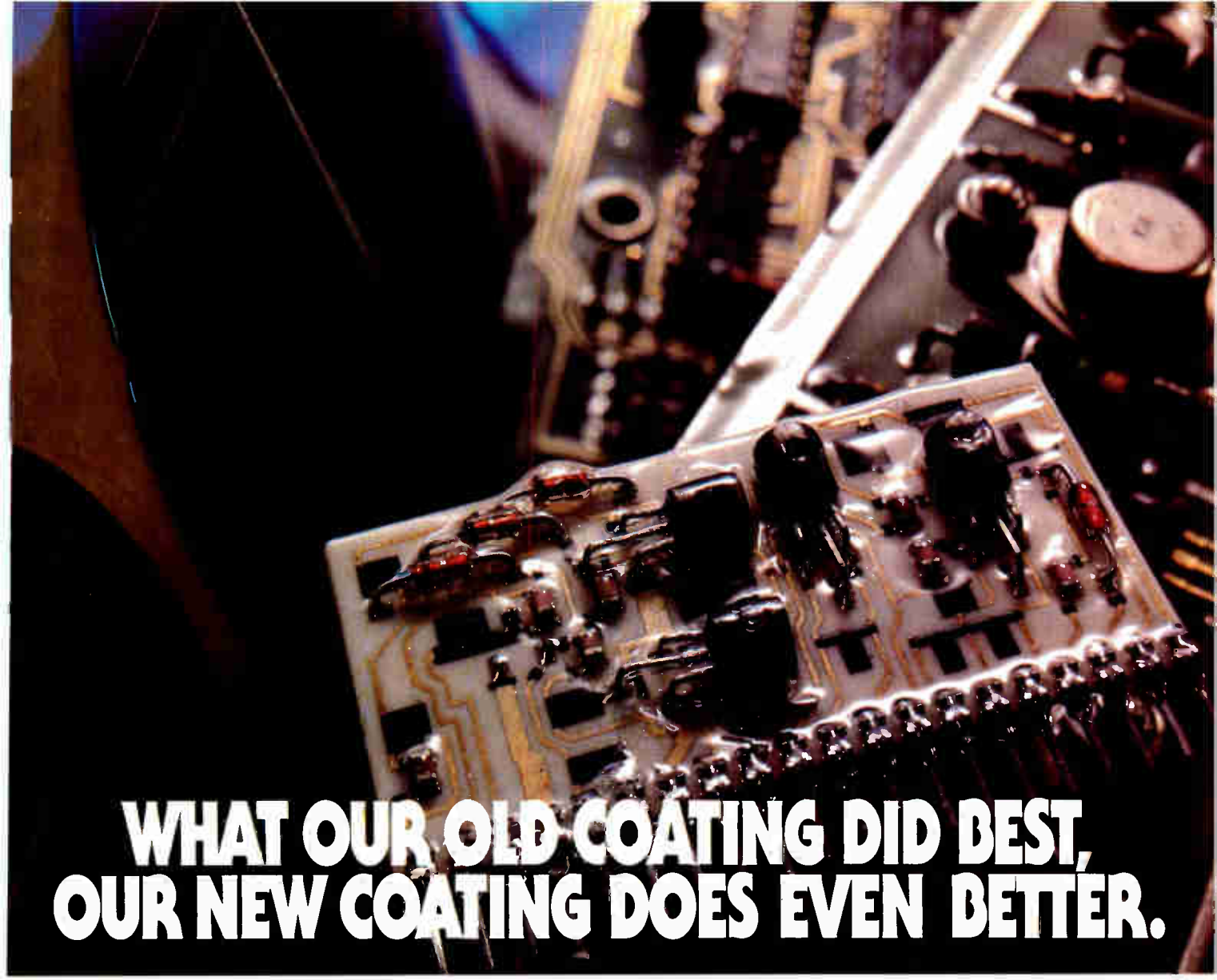
Micro-Circuit Engineering Inc., 1111 Fairfield Dr., West Palm Beach, Fla. 33407. Phone (305) 845-2837 [414]

Chip carries photodiode, linear amp, Schmitt trigger

Available in TO-18 hermetic packages, the OPL 800, OPL 800-OC, OPL 801, and OPL 801-OC Photologic chips come in buffer totem-pole, buffer open-collector, inverter totem-pole, and inverter open-collector configurations, respectively. The monolithic integrated circuits have a photodiode, a linear amplifier, and a Schmitt trigger that provides a high immunity to input and V_{CC} noise. Each device can drive up to eight TTL loads directly and has a typical propagation delay time of 2 μs and typical rise and fall times of 25 ns.

The Photologic chips are available immediately from stock and cost $3.60 each at the 1,000-unit level.

TRW Optron, a division of TRW Inc., 1201 Tappan Circle, Carrollton, Texas 75006. Phone (214) 323-2200 [416]



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New products

Computers & peripherals

Q-bus systems start at $8,500

Packaged computers include 5¼- or 8-in. Winchester and floppy-disk drives

Microcomputers packaged as systems are coming along well enough equipped to challenge some microcomputers. One integrated system is the WCF-1 from North Atlantic Industries' Microcomputer division, a fully tested, rack-mountable system containing either an LSI-11/2 or LSI-11/23 central processing unit from Digital Equipment Corp., a 5¼-in. Winchester drive, a 5¼-in. floppy-disk drive, wired Q-bus backplane, up to 64-K bytes of memory with the 11/23, an input/output interface with four RS-232-C ports, and all necessary power supplies. Another model, the WCF-3, is the same basic system but with 8-in. Winchester and floppy-disk drives.

The 5¼-in. Winchester drive offers 5 megabytes of storage and the 5¼-in. floppy disk is a 1-megabyte version. The 8-in. Winchesters are available in 10-, 35-, and 70-megabyte sizes, along with a 1-megabyte 8-in. floppy disk.

A controller card for the disk drives is included in the system, as is direct-memory-accessing circuitry. Front-panel controls and indicators are supplied as well. The system is delivered ready to go as soon as the desired software is loaded.

The WCF-1 and WCF-3 can be used by system builders in the LSI-11 community that have the necessary software for applications such as word processing, graphics, instrument control, process control, or data acquisition. Delivery of the WCF-1 takes 60 days from receipt of order, with the LSI-11/2 processor and 64-K bytes of memory putting the cost at $8,500. The LSI-11/23 version with 256-K bytes of memory is $13,500. Fixed pricing for the WCF-3 models has not been established but will probably range from $13,000 to $18,000.

North Atlantic Industries Inc., 60 Plant Ave., Hauppauge, N. Y. 11787. Phone (800) 645-5292 or (516) 582-6500 [369]

Distributed system supports 16 users

CP/M-compatible systems link independent stations, protect files in central storage

Although more users can enter and access information in a distributed data-processing system than in a centralized processing system, the performance of the distributed system typically suffers degradation as more users are added. Engineers at TeleVideo Systems Inc. have a new family of small-business computer systems with, they say, a distributed-processing environment to which equipment for up to 16 users can be added without degrading throughput. The family also has faster response times than are possible with single-user microprocessor-based systems.

For growth. To be introduced at the National Computer Conference in Chicago this week, the CP/M-compatible family offers a growth path from an entry level, single-user system up to a 16-user distributed system. Says Richard DuBridge, executive vice president of TeleVideo, "Each additional work station is a stand-alone computer containing its own microprocessor and random-access memory."

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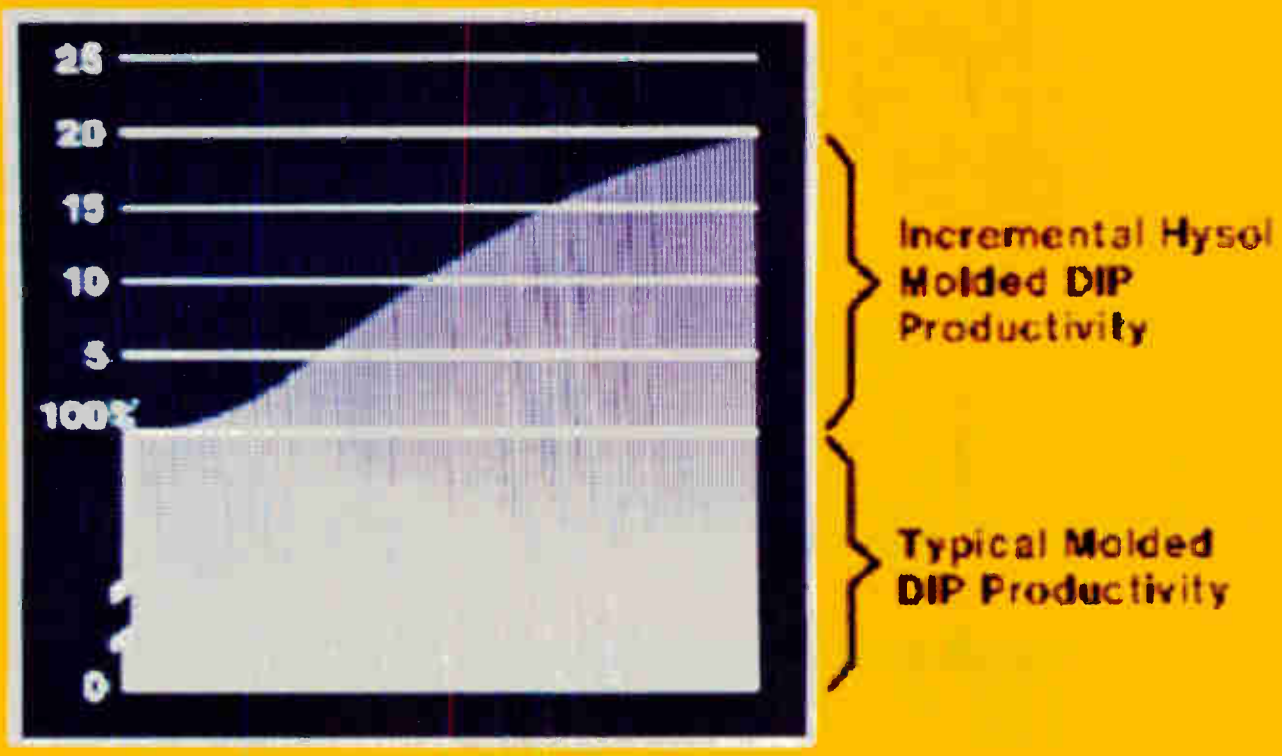

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These advanced epoxy compounds are formulated for optimum production characteristics as well as superior device performance.

For example, Hysol epoxies develop a higher hot hardness than conventional epoxy compounds. So instead of an average three minute mold cycle, the same mold press can produce a finished shot in *two*.

Hysol epoxies can also significantly reduce the need for deflashing. Or eliminate it completely.

They can help reduce post-cure time by a hefty 60 to 70 percent.

And because they leave your molds clean more than twice as long, they can reduce cleaning maintenance from once per shift to just once every two shifts or three.

Result?

You get five, ten—up to 20 percent extra molded DIP production per shift. With no extra investment.

Along with better productivity, of course, you get the extra assurance of Hysol quality.

Plus all the advantages of Hysol performance. Like improved moisture resistance, better thermal cycling characteristics and increased thermal stability—for better reliability.

Hysol is the leader in semiconductor epoxy technology. And to prove it, we'll supply the Hysol epoxy and qualified field support for a full productivity and performance comparison on your test line.

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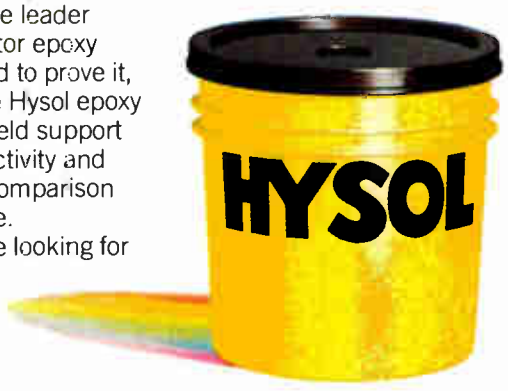

Circle 189 on reader service card

New products

The single-user system, designated the system I, is based on the Z80A 8-bit microprocessor and its support family. It features 1 megabyte of (dual) minidiskette storage, 64-K bytes of random-access memory, a 4-K-byte erasable programmable read-only memory for diagnostics, and the CP/M level 2.2 microcomputer operating system. It also has RS-232-C and RS-422 input/output ports to which peripheral systems can be connected. Also included in the $3,995 system I configuration is TeleVideo's existing model 950 smart terminal with standard features that include a detached keyboard, smooth line scrolling, line graphics and editing capability, and an I/O data rate of up to 19.2 kb/s.

The system II and III multiuser systems are supported by TeleVideo's proprietary operating system, called MmmOST. This multiuser, multitasking operating system handles all communications between the shared files and independently operating satellite user stations. It provides what DuBridge claims is "the interlocking protection and file security not previously available in CP/M-based systems." Users can now realize the benefits of a low-cost interactive system having a high throughput, he adds, and take advantage of the existing CP/M applications library of data and word-processing programs.

The system II enables up to six system Is or model 1000 satellite user stations to be connected in a distributed processing environment. Its TS83 service processor also uses the Z80A and has the MmmOST operating system residing within it. Additionally, the TS83 has 64-K bytes of RAM and supports 1 megabyte of data storage on a single minidiskette. A Winchester disk drive provides an additional 10 megabytes

of on-line storage capacity.

Among other standard features in the system II are two RS-232-C serial ports that allow interfacing with any of several types of printer and implementation of field-service procedures. Each model 1000 satellite user station is itself an intelligent terminal containing a Z80A, 64-K bytes of RAM, RS-232-C and RS-422 ports, and its own 4-K-byte E-PROM for diagnostics.

The high-end system III supports 16 users with up to 70.5 megabytes of hard-disk on-line storage. It, too, has a Z80A-based service processor, the TS86, containing 64-K bytes of RAM and MmmOST. The TS86 comes with a 30-megabyte Winchester disk drive and controller as standard features and has provisions for supporting additional external hard-disk storage. A 17.2-megabyte tape cartridge drive and controller serve as backup.

Furthermore, two model 1000 stations are connected to the service processor's eight standard RS-422 ports as a basic configuration. An optional port-expansion system allows the addition of eight more RS-422 ports, permitting up to 16 model 1000s to be on line simultaneously.

Languages. Each of the microcomputer systems can be programmed in RM/Cobol, Basic 80, and PL/1-80, with compilers for all of these initial language offerings available from TeleVideo to be run under CP/M. Plans call for implementation of Cobol-80, Fortran-80, APL, Pascal, C-Basic, and C. Programs are fully transportable from system I through system III.

TeleVideo Systems will also unveil at the NCC a low-cost ($699) conversational terminal, the model 910, whose features include switch-selectable compatibility for emulating the Lear Siegler ADM-3 or ADM-5, Hazeltine 1410, and ADDS 25 dumb terminals, among others. This compatibility permits use of the 910 without modification in existing systems that have many of the more popular cathode-ray-tube terminals.

The model 910 will be available in June, as will the system I. Initial shipments of system II and system

Intel–soaring aloft with the M2732 EPROM.

Introducing the M2732 EPROM. Now available for VLSI military microcomputer designs that soar above the rest.

For military and hi-rel systems, Intel's new 32K EPROM is ready to take off today. Built in full compliance with the Class B requirements of MIL-STD-883B, Methods 5004 and 5005, the M2732 is the newest member of Intel's growing family of military VLSI products. And it's available in volume now.

For applications ranging from shipboard and ground communication systems to avionics and missile control, the M2732 offers distinct advantages. It's not only the highest density military EPROM available, it's also designed to maximize the performance of today's advanced 16-bit microprocessors, like the M8086. Plus its pinout provides the natural upgrade path from 32K to 64K, 128K and even 256K-bit parts.

An EPROM to match your microprocessor

To get all the high-flying performance possible out of today's military microprocessor-based systems, it takes memory components with features as advanced as the M2732.

Features like high speed and low power. With an access time of 450 ns, the M2732 is fast enough to operate with the M8086 or M8085A. And its automatic power-down capability cuts average power dissipation by 60-80%.

The M2732 also features superior control capabilities. Its 2-line control structure eliminates bus contention—an important consideration in today's multiplexed-bus microprocessors.

Plus the M2732's reliability is unsurpassed. Like our M2716 EPROM, the M2732 undergoes tougher-than-military quality control tests to insure they'll retain their programs for years to come. With Intel's decade of EPROM experience, it's no wonder we've shipped more military EPROMs to more military programs than any other supplier.

A JEDEC-approved pinout to set your sites on today

Right now you can start planning for future memory upgrades, by designing in the M2732. Its pinout conforms to the JEDEC-approved Standard for Byte-Wide Memories, from 16K through 256K bits. So you'll be able to upgrade easily from an M2732, without changing your design or board layout. And because of this compatibility, the M2732—like the industry standard M2716—will be available from second source suppliers.

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Our advancing line of military VLSI products—like the new M2732—reflects our strong commitment to military customers: namely, to continue to deliver the broadest line of VLSI devices possible to military systems designers. From devices like the M8086, M8085A, and M8048, to military EPROMs, bipolar PROMs, static and dynamic RAMs, and microprocessor peripherals.

We've shipped hundreds of thousands of these high-performance VLSI devices to vital military programs over the past four years. And we'll continue this commitment for years to come. Not only in components, but in support, such as our advanced development tools, including the Intellec® system and ICE™ in-circuit emulation modules.

So the next time you're on the lookout for state-of-the-art military VLSI devices, look to the leader—Intel. For further information on military products, or a copy of our 1981 *Military Products Data Catalog,* contact your local Intel sales office/distributor. Or contact Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

Circle 193 on reader service card

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III are slated for July and August, respectively. A system II with one model 1000 satellite user station is priced at $8,995, and the system III with two stations sells for $19,995. Additional model 1000 stations are priced at $1,795 each.

TeleVideo Systems Inc. 1170 Morse Ave., Sunnyvale, Calif. 94086 [361]

1-lb data-entry terminal has phone coupler on its back side

The MSI 84 portable terminal's firmware, an intelligent liquid-crystal display, and multiple-use components trim its size and weight. It is the smallest terminal produced by MSI Data Corp. and will be directed towards use by large sales forces.

The package containing erasable programmable read-only memory, called a custom application module, can be removed and replaced easily by the end user, greatly increasing the unit's versatility. Available direct-sales and sales analysis programs can be altered for new tax structures, ordering formats, or other changes. The 4-K-byte package can be programmed to user specifications by the firm or by users who have one of MSI's systems for programming the module, such as its recently announced field-service terminal.

Outdoors. The Hitachi 16-character dot-matrix LCD allows the system to be used outdoors and enables users to employ special characters. The display can be programmed for a variety of alphanumeric prompts.

The unit measures 3.5 by 6 by 0.5 in. deep, small enough to fit into a coat pocket; its weight is less than 1 lb. Pricing is $650 in quantities up to 500, dropping to $575 for larger orders. Initial delivery of the system is set for August.

Data is entered via 24 keys arranged in six rows of four. Interrupts drive the keyboard and other devices that operate when the keyboard is not being used. The alphanumeric keys each serve as inputs for two letters, with some also handling digits. Color-coded keys determine which of a key's two letters and one numeral a key will enter.

Data is stored in 4-K-byte random-access memory. It is transmitted to the host computer via a built-

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Circle 195 on reader service card

New products

in acoustic coupler or an optional coupler, which can be plugged into the unit. The coupler on the back of the terminal attaches to the telephone mouthpiece, transmitting at either 300 or 600 b/s. The speaker used for this transmission is also used for the unit's alarm.

The optional coupler has improved noise reduction and a transmission rate of 1,200 b/s. With both units, the user must dial the phone and listen for tones that tell him when to begin transmission.

The MSI 84 is powered by four AA batteries. Unlike other portable terminals from MSI Data Corp., it has no backup batteries for support when the primary source is changed. This model utilizes a large capacitor to retain data in memory for about an hour.

The operating software is stored in 8-K bytes of ROM to keep power consumption as low as possible. Low-power complementary-MOS devices are used throughout the terminal, among them the RCA 1802 microprocessor. The low power consumption of the E-PROM module was also a factor in selecting it over RAM for program storage.

The company is introducing the model 2741 transmitter converter and the 2743 receiver converter along with the MSI 84 at the National Computer Conference this month. The 2741 has two asynchronous inputs; its output is bisynchronous for communication with the host. Its price is $2,000 in single quantities. The 2743 is a protocol converter with a floppy-disk drive and a base price of $7,000.

MSI Data Corp., 340 Fischer Ave., Costa Mesa, Calif. 92626. Phone (714) 549-6393 [367]

DEC-compatible systems boost throughput with cache

Able Computers, a maker of add-on products for Digital Equipment Corp. computers, is offering for the first time DEC-compatible systems, the 34 Magnum and the 44 Magnum. The former sports some en-

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New products

hancements over DEC's PDP-11/34. The 44 Magnum, though fully software-compatible and up to most of the PDP-11/44's specifications, does not meet a very few of those specs in areas the manufacturer sees as less than crucial. Both the 34 and 44 Magnums use DEC central-processing-unit boards, but both also use hardware designed by Able. The six-year-old firm is authorized to sell licenses for DEC's TSTS/E, RSX-11M, and RT-11 operating software.

Standard offerings on the Magnum machines that are options on the DEC products include dual TU 58 cartridge tape drives, an 8-K-byte cache memory, and floating-point math software. Able uses heftier power supplies with 75-A output and remote sensing to ensure equalized power levels. Enhanced input/output structures and the cache increase the throughput of the machines.

The 34 Magnum has 256-K bytes of memory, is said to match or exceed the PDP-11/34A in all hardware areas, and is priced at $21,000 in single units. It can be upgraded to a 44 Magnum with up to 4 megabytes of main memory. The 44 with 512-K bytes of main memory costs $27,000. Delivery of either is in 60 days.

Able Computers, 1751 Langley Ave., Irvine, Calif. 92714. Phone (714) 979-7030 [362]

Small system cluster has large-system capabilities

The first computer system to come from the May 1980 TRW and Fujitsu joint venture is a multitasking, multiuser data-processing system called the TFC 8500. It consists of a complete family of small general-purpose information-processing systems that offer capabilities normally asso-

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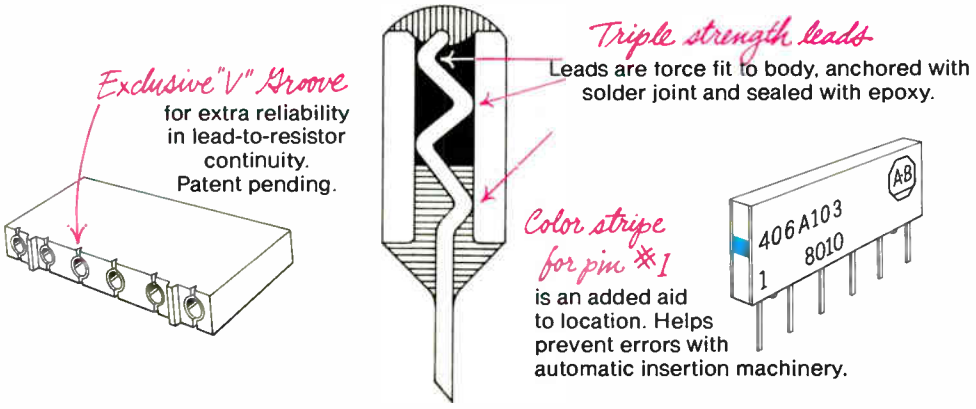

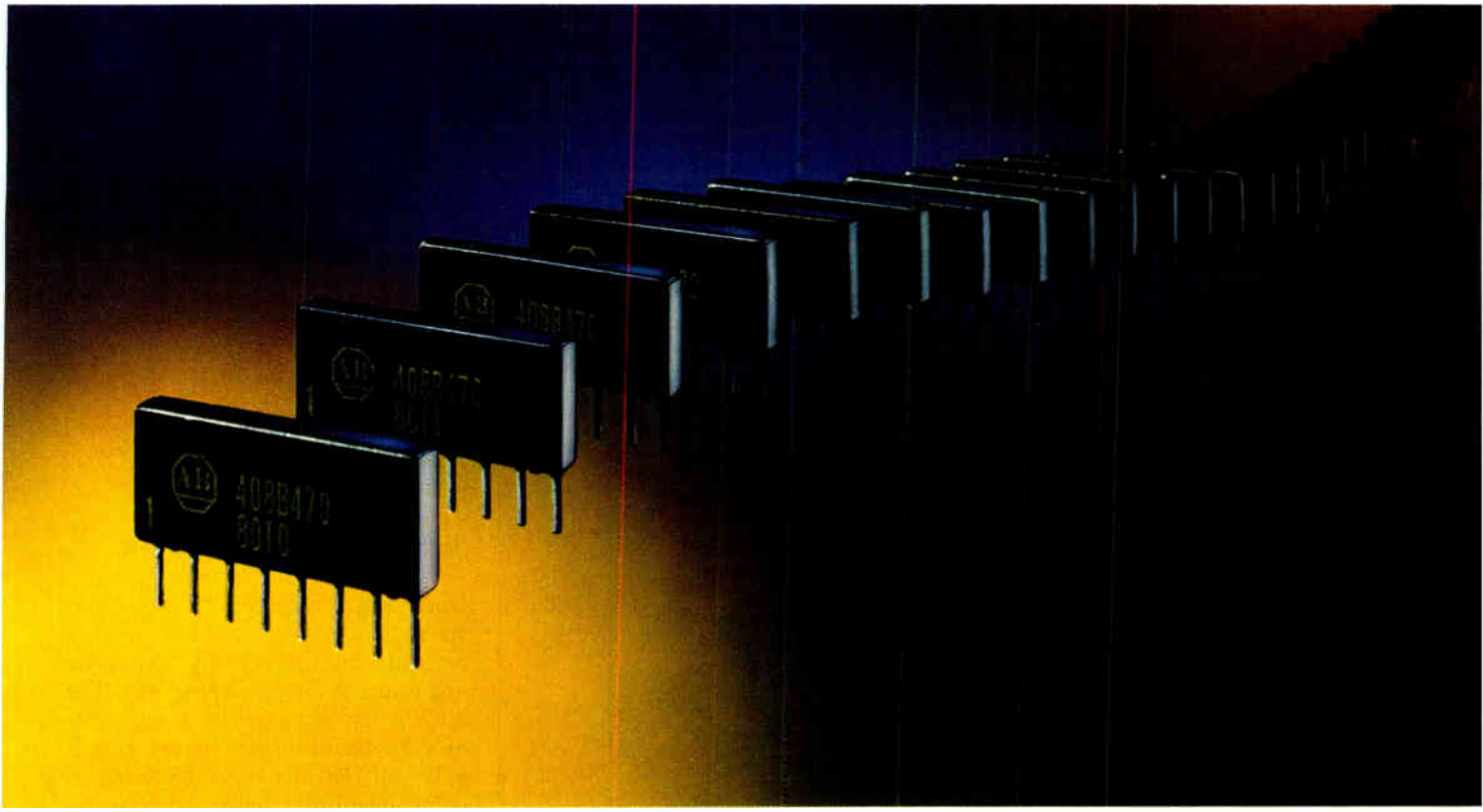

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Circle 199 on reader service card

New products

ciated with large systems that will operate as a stand-alone unit, on line to a central computer, or inside the TFC 8500 network. For example, each family will perform in batch, on-line, and distributed-processing applications.

The entry-level configuration starts with a single work station. It may be expanded to include as many as 80 local and remote work stations, with complete software compatibility throughout all configurations.

The main storage unit uses 64-K MOS large-scale integrated circuits and has 256-K bytes of system memory. Add-on storage units permit expansion up to a maximum of 2 megabytes. Storage cycle time is 400 ns for every 2 bytes. The central processing unit contains a one-chip, 10,000-gate microprocessor and 700-gate-per-chip high-speed bipolar LSI circuits and features virtual memory.

The system comes with such high-level languages as Fortran, Cobol, and RPG. Peripheral equipment includes disk storage, displays, and printers, magnetic tape units, and line printers. Error-checking and -correction code is included for both main and disk storage.

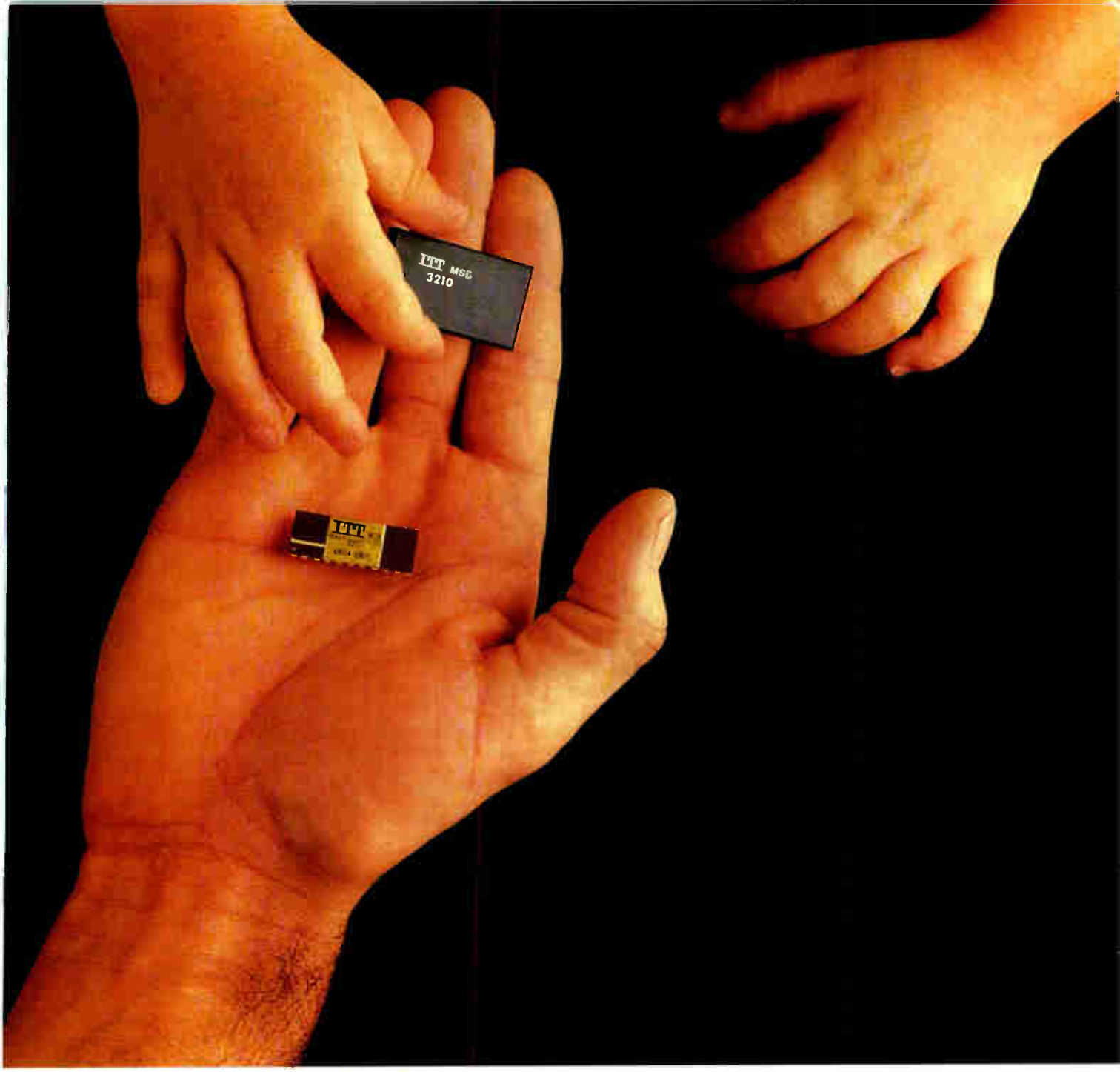
Prices range from $25,000 for a single work station to $200,000 for a maximum-configuration multistation system. Initial deliveries are scheduled for July.

The TRW-Fujitsu Co., 9841 Airport Blvd., No. 620, Los Angeles, Calif. 90045. Phone (213) 535-3821 [363]

Dot-matrix unit prints 350 characters per second

Operating at a speed of 350 characters/s, the AP200 dot-matrix printer performs more effectively than other line printers and at a lower cost. The AP200 can be used with the company's keyboard-display–based terminals and the model 43 BSR multipoint teleprinter series and as an auxiliary printer.

The high-speed matrix printer has a legible printout on forms of up to six ply; a print head with a life expectancy of 300 million characters



Introducing the 3210 DTMF tone receiver. The newest member of an old established family.

First came the ITT 3201, a fully integrated DTMF receiver that combined both digital and analog functions on a single CMOS/LSI chip.

Now ITT adds the 3210 which allows you to select from a broad range of tone receiver designs. The ITT 3210 combines the latest advancements in LSI technology with the stability, reliability and accuracy inherent in thick film hybrid technology to produce a combination of quality and versatility in a DTMF tone receiver that is unmatched.

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For complete specifications, contact: ITT North Microsystems Division, 700 Hillsboro Plaza, Deerfield Beach, FL 33441. Phone: (305) 421-8450, Telex: 512329, TWX: 510 953 7523.

ITT

ITT North Microsystems Division

Circle 201 on reader service card

New products

without maintenance that can be replaced by an operator; adjustable tractors to accommodate forms ranging from 3 to 16 in. wide and 3 to 14 in. long; a maximum printing line of 132 characters at 10 characters/in.; and a 218-character line at 16.7 characters/in.

The AP200 features form feeding, perforation skip-over, soft roll with vertical paper positioning, a fast slew rate, front or bottom paper loading, a snap-in ribbon cartridge, and a display to indicate function and diagnostics results; 110/220-V universal power supply, paper tray, and pedestal are optional. It sells for $3,868. Deliveries start in July.

Teletype Corp., 5555 Touhy Ave., Skokie, Ill. 60077. Phone (312) 982-2000 [364]

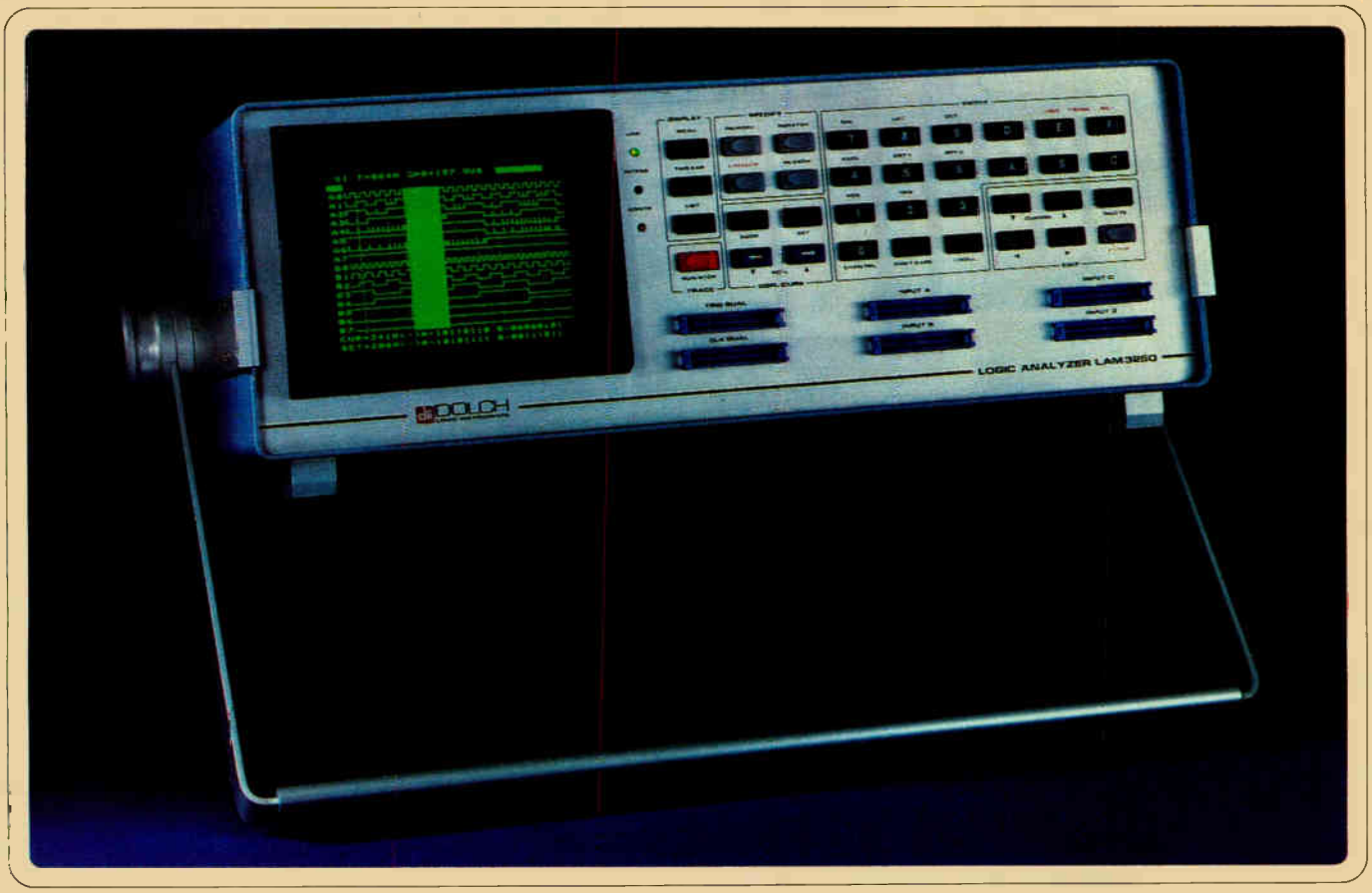
Small terminal has dot-matrix printer, graphics mode

The Quint KSR-743 keyboard send-receive terminal is designed for telecommunications and computer peripheral applications. Half the size of competitive printer terminals, it weighs only 12 lb and contains internal and remote-controlled diagnostics; a Z80 microprocessor; a line-switched power supply for operation from 87 to 132 V ac, 50/60 Hz, at less than 35 W; a 20-character answer-back nonvolatile configuration; and a standard RS-232 and 4-to-20-mA current-loop interface with a selection of 110 to 1,200 b/s.

The KSR-743's printer features the Collinear 7 print head, which eliminates needle bending, reduces needle wear, and improves dot alignment. A self-inking ribbon cartridge is provided for a long ribbon life. Fourteen fonts can be selected, ranging in density from 5.0 to 20.0 characters/in. The printer has a speed of over 50 characters/s and a graphics mode with 120 dots/in. horizontally and 60 vertically. The 62-key keyboard generates the full ASCII 128 characters with a capital-lock mode.

In single-unit quantities, the KSR-743 terminal sells for $995.

Quint Systems Inc., 3693 Commercial Ave., Northbrook, Ill. 60062 [365]



32 TO 64
Channels...with a Battery

Dolch Logic Instruments' third generation logic analyzer, the LAM 3250, lets you meet your troubleshooting needs now, and expand for the future. The LAM 3250 records up to 32 channels of information at sampling rates to 50 MHz, and with optional Channel Expansion Probes, its capability can be extended to 64 channels. And there's more.

Sophisticated clocking.
Since it incorporates dual 16-channel X 1000-bit recording blocks, the LAM 3250 can accept up to two independent external clocks for sampling data, letting you independently monitor both address and data on a multiplexed bus.

Powerful triggering.
Four-level sequential triggering, each level with an independent pass counter ranging from 1-255 counts, lets you debug programs containing nested subroutines. There's even a Restart function to guide you through data on the bus. All of this is easily programmed in a separate trigger menu.

Battery back-up.
The LAM 3250's revolutionary new BATTERY-BACKED MENU MEMORY feature allows you to store up to 6 separate files of display and menu parameters in CMOS RAM for up to three months without power. This means that you can recall complete test set-ups in a matter of seconds. No more time wasted rewriting menus.

Check these features and compare:
- 32 channels X 1000-bit memory
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- Sampling rates to 50 MHz
- 5 ns glitch capture
- Timing capability for 16 or 32 channels
- Hex, octal, binary and ASCII displays
- Powerful word search feature
- Window triggering
- Real-time trigger tracing
- Non-volatile menu memory
- GPIB and RS-232 interfaces standard
- Personality probes and disassemblers for many popular uP's and bus systems (optional)

This is only part of the story. For more details on this and other dynamic troubleshooting tools, contact the logic analyzer experts today. Dolch Logic Instruments,
230 Devcon Drive, San Jose, CA 95112.
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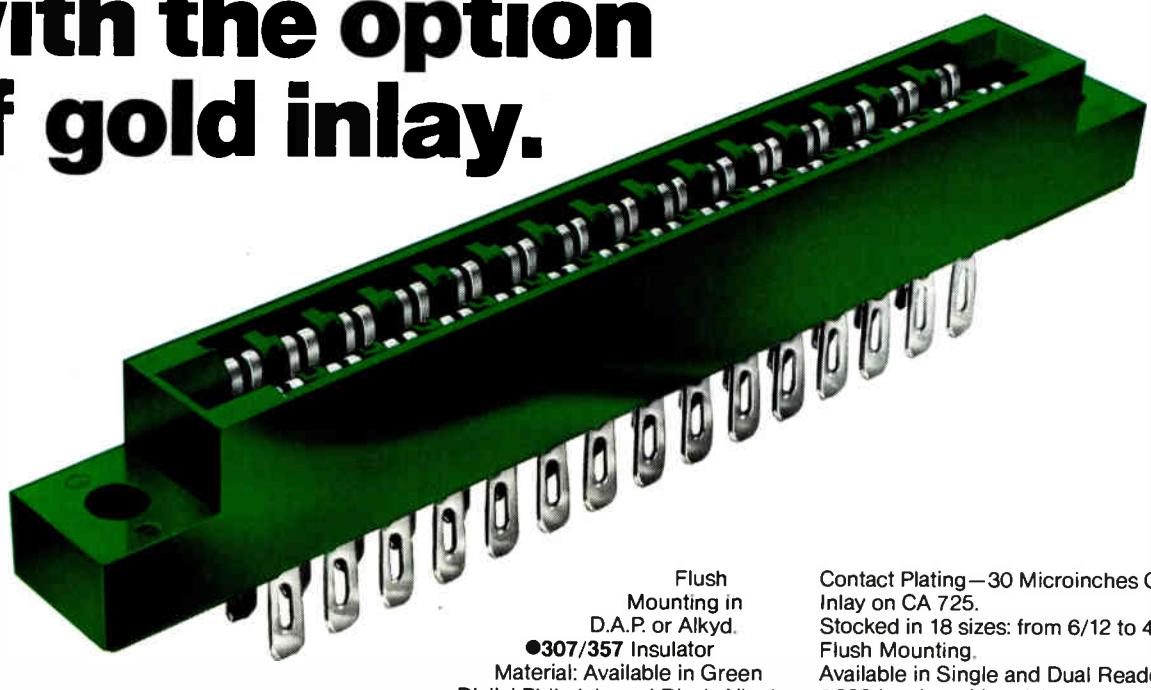
Circle #122 for further information

Circle #203 for demonstration

No Other North American manufacturer produces this many .156" spacing, "Off the Shelf" connectors with the option of gold inlay.



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Other sizes available.

●**305/355** Insulator Material: Available in Green Diallyl Phthalate and Black Alkyd.
Contact Plating—30 Microinches Gold Inlay on CA 725.
Stocked in 18 sizes from 12 to 86 contacts.

●**306/356** Insulator Material: Available in Green Diallyl Phthalate and Black Alkyd.
Contact Material: Phosphor Bronze per QQ-B-750 Composition A.
Contact Plating—Gold, 10-20 Microinches, over Nickel, 30-150 Microinches.
Stocked in 19 sizes from 6 to 43 contacts.
Flush Mounting in D.A.P. or Alkyd.

●**307/357** Insulator Material: Available in Green Diallyl Phthalate and Black Alkyd.
Contact Material: Phosphor Bronze per QQ-B-750 Composition A, or CA 725.
Contact Plating—Gold, 10-20 Microinches over Nickel, 30-150 Microinches, or CA 725: 30 Microinches Gold Inlay.
Stocked in 16 sizes: 6/12, 7/14, 10/20, 11/22, 12/24, 13/26, 14/28, 15/30, 18/36, 22/44, 24/48, 25/50, 28/56, 30/60, 36/72, 43/86. Available in Single and Dual Readout.

●**315** Insulator Material:
Green Diallyl Phthalate.
Contact Material: Copper, Nickel, Tin Alloy 30 Microinches Gold Inlay.
Stocked in 11 sizes: 12, 20, 24, 30, 36, 44, 50, 56, 60, 72 and 86 Contacts.

●**316** Insulator Material:
Green Diallyl Phthalate.
Contact Material: Phosphor Bronze per QQ-B-750 Composition A.
Standard Plating—Gold, 10-20 Microinches over Nickel 30-150 Microinches.
Stocked in 12 sizes: 6, 10, 12, 15, 18, 22, 25, 28, 30, 36, 40 and 43 contacts.

●**337/387** Insulator Material: Available in Green Diallyl Phthalate and Black Alkyd.
Contact Material: Copper, Nickel, Tin Alloy, CA 725.
Contact Plating—30 Microinches Gold Inlay on CA 725.
Stocked in 18 sizes: from 6/12 to 43/86.
Flush Mounting.
Available in Single and Dual Readout.

●**338** Insulator Material:
Green Diallyl Phthalate.
Contact Material: Phosphor Bronze per QQ-B-750 Composition A.
Contact Plating—Gold, 10-20 Microinches, over Nickel, 30-100 Microinches.
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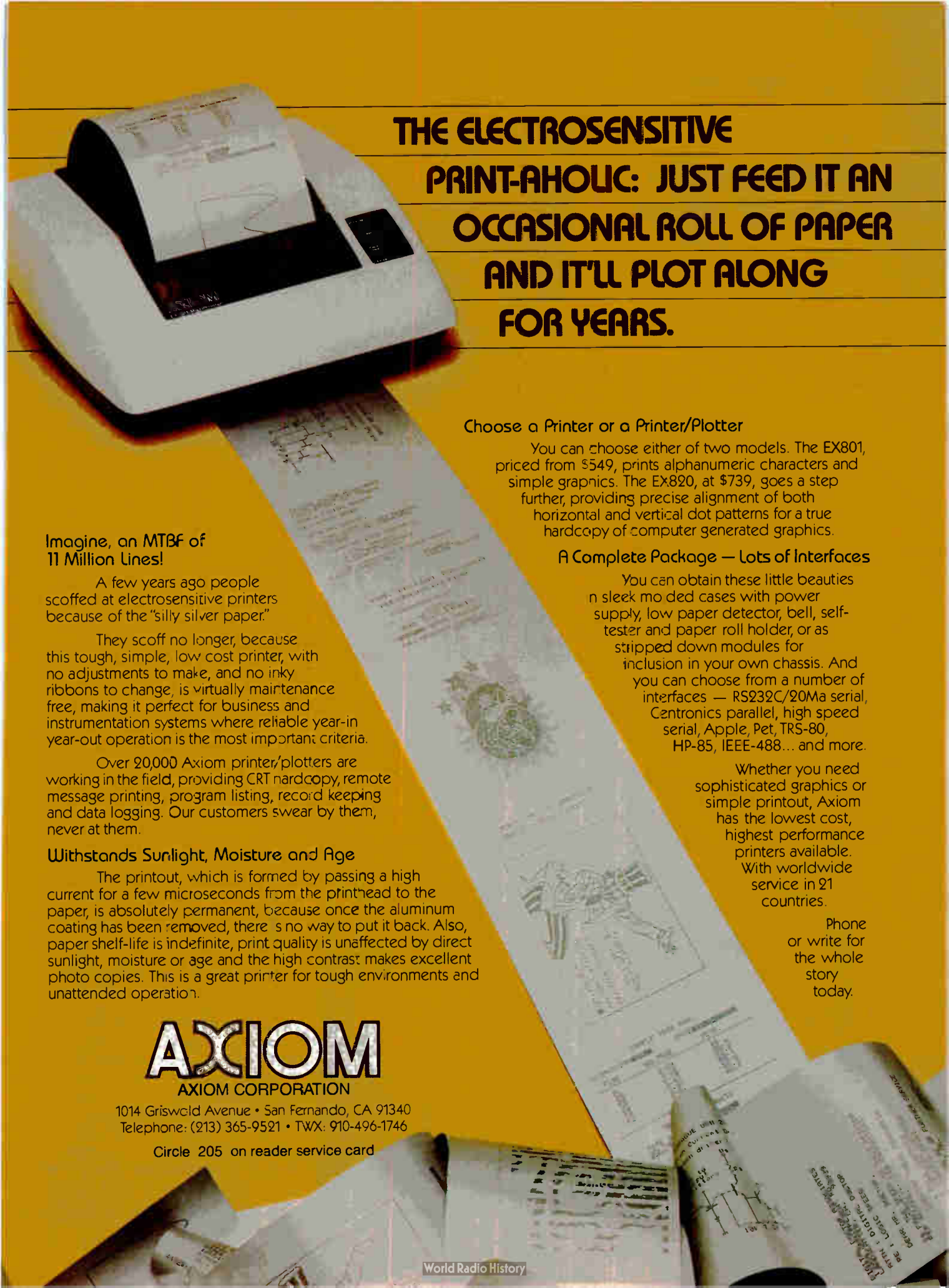
Circle 204 on reader service card



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You can choose either of two models. The EX801, priced from $549, prints alphanumeric characters and simple graphics. The EX820, at $739, goes a step further, providing precise alignment of both horizontal and vertical dot patterns for a true hardcopy of computer generated graphics.

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A Complete Package — Lots of Interfaces

You can obtain these little beauties in sleek molded cases with power supply, low paper detector, bell, self-tester and paper roll holder, or as stripped down modules for inclusion in your own chassis. And you can choose from a number of interfaces — RS232C/20Ma serial, Centronics parallel, high speed serial, Apple, Pet, TRS-80, HP-85, IEEE-488... and more.

Whether you need sophisticated graphics or simple printout, Axiom has the lowest cost, highest performance printers available. With worldwide service in 21 countries.

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Withstands Sunlight, Moisture and Age

The printout, which is formed by passing a high current for a few microseconds from the printhead to the paper, is absolutely permanent, because once the aluminum coating has been removed, there is no way to put it back. Also, paper shelf-life is indefinite, print quality is unaffected by direct sunlight, moisture or age and the high contrast makes excellent photo copies. This is a great printer for tough environments and unattended operation.

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Circle 205 on reader service card

Components

Buffer amplifier puts out 100 mA

Low-cost bipolar hybrid drives high-current loads with dc-to-125-MHz signals

The MOS-100 hybrid bipolar buffer amplifier affords fast, stable performance and high-current output drive over a dc-to-125-MHz typical bandwidth. Originally built by Analog Devices Inc.'s Computer Labs division for internal use in high-speed analog converters aimed at video applications, the unity-gain buffer amp addresses a number of other areas as well.

"The part is a low-cost alternative to buffer amplifiers with input field-effect transistors, if the application is one where minimum input bias current and maximum input impedance are not required," notes Mark D. Skillings, product marketing engineer at the Greensboro, N. C., facility. Such applications can include current boosters, line drivers, high-speed analog-to-digital input buffers, nuclear instrumentation amplifiers, and video impedance matching. The HOS-100 also can drive 50-Ω coaxial cables and act as a yoke driver for high-resolution cathode-ray-tube displays.

In hundred-unit lots, the HOS-100AH commercial-grade model costs $12.25, and the HOS-100SH military version $23; processed to MIL STD 883, the part costs $29.50. That makes the HOS-100 about 25% to 35% less expensive than buffer amplifiers containing FETs, estimates Skillings.

The HOS-100 has a typical input bias current of 5 μA; input impedance typically is 200 kΩ. The unit maintains a minimum output voltage of ±10 V, at a continuous load of ±100 mA minimum (±250 mA peak). Typical output impedance is 8 Ω. The buffer amplifier's typical slew rate is 1,400 V/μs in the commercial model, and 1,500 V/μs in the military version.

Other typical specifications of the HOS-100 include a 2-ns rise time, phase nonlinearity of 2°, and harmonic distortion of less than 0.1%.

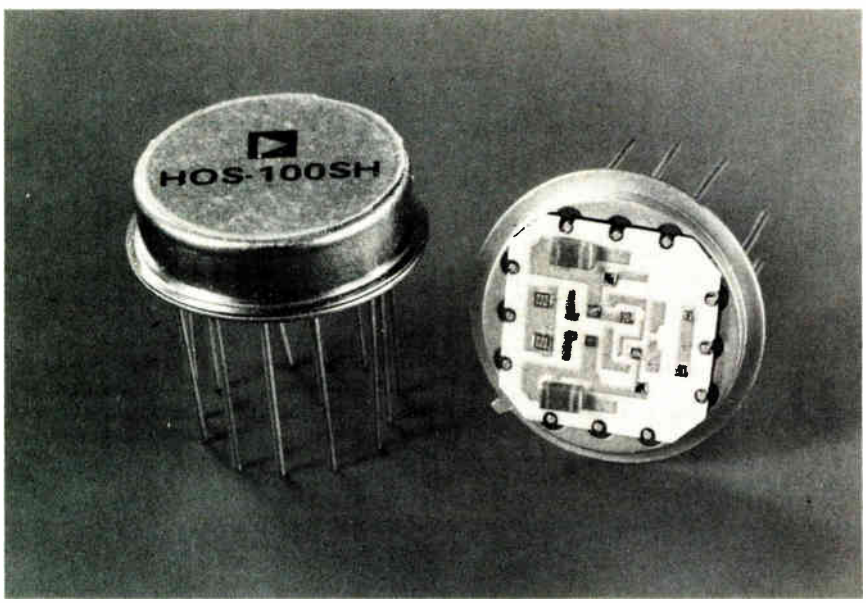
The buffer's voltage gain is between 0.94 (0.95 in the military model) and 1.0. Typical output offset voltages in the commercial and military versions of the HOS-100 are 10 and 5 mV, respectively. The output offset-voltage temperature coefficient typically is very good at 25 μV/°C in both models.

The HOS-100's rated performance requires a +15- and −15-V dual power supply. Quiescent power consumption in commercial models is a maximum of 600 mW, and 480 mW in the military-grade model. Maximum power dissipation for both models fully loaded is 1.5 W.

The HOS-100's rated mean time between failures is in excess of 560,000 hours. The commercial-grade HOS-100AH operates over case temperatures of −25° to +85°C, and the military model HOS-100SH operates at −55° to +125°C. Both units are housed in TO-8 metal cases.

Delivery of parts processed to MIL STD 883 takes four weeks; all other deliveries are from stock.

Analog Devices Inc., Route 1 Industrial Park, P. O. Box 280, Norwood, Mass. 02062. Phone (617) 329-4700 [341]



Fixed-vocabulary ROMs cut synthesized-speech costs

Texas Instruments' VM61002, VM7001, -02, and -03 are p-channel MOS read-only memories encoded with speech patterns for standard vocabularies. The fixed vocabularies target consumer and industrial markets. TI intends to cut synthetic speech costs with the speech ROMs: the three VM7 series 32-K ROMs are priced at $6.50 each in orders of 5,000. The VM61002 is a 128-K ROM with a 240-word vocabulary geared towards industrial control and priced at $10 in similar lots.

The firm uses two voice synthesis processor formats: an 8-bit-wide format that allows TI to offer both male- and female-pitched synthesized speech, and a 4-bit-wide format capable of male-pitched speech output only. The 128-K VM61002 is in the 8-bit format, and so will come in male and female versions. Its vocabulary includes numbers, letters, colors, measurement-related words such as milli, micro, amp, and meter, and other words used in industrial control applications.

The VM71001 is a 32-K ROM containing 50 words also aimed at industrial applications. The 71002 and 71003 share a 50-word vocabu-

Pin up of the year. The 28-pin 64K ROM from Synertek.

Make a smooth transition to the new standard in ROMs with the JEDEC-approved 28-pin 64K ROM from Synertek. Smooth because our pin up from 24 pins to 28 pins takes into account today's—and tomorrow's—board design needs.

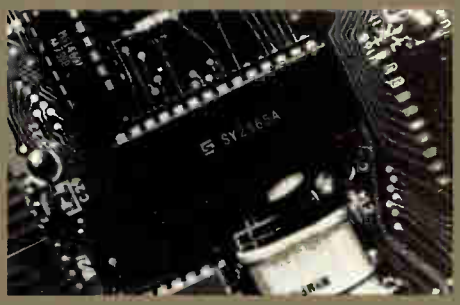
Now you can make the move to flexibility in new board layouts with a whole new generation of 64K ROMs. The SY2365A offers you two-way compatibility—step down to the 24-pin SY2333 32K ROM of today or up to the 28-pin 128K/256K ROMs of the future.

Not only that, but it's fast too. At 200nsec (max), the SY2365A delivers the kind of high performance you need to meet the demands of today's system designs. With the organization to match—8192x8.

The SY2365A also features automatic power down through its Chip Enable ($\overline{CE}$) input that translates into system level power savings of up to 85 percent. And because it's pin-for-pin compatible with 2764 EPROMs already in your system, it's your answer when it comes to making a cost-effective—and quick—move from EPROM prototyping to high volume ROM production.

A true beauty, for now and the future—that's the SY2365A 64K ROM from Synertek. We're the company that built its name in servicing the ROM marketplace. Call Memory Product Marketing direct at (408) 988-5611 or contact your area Synertek representative.

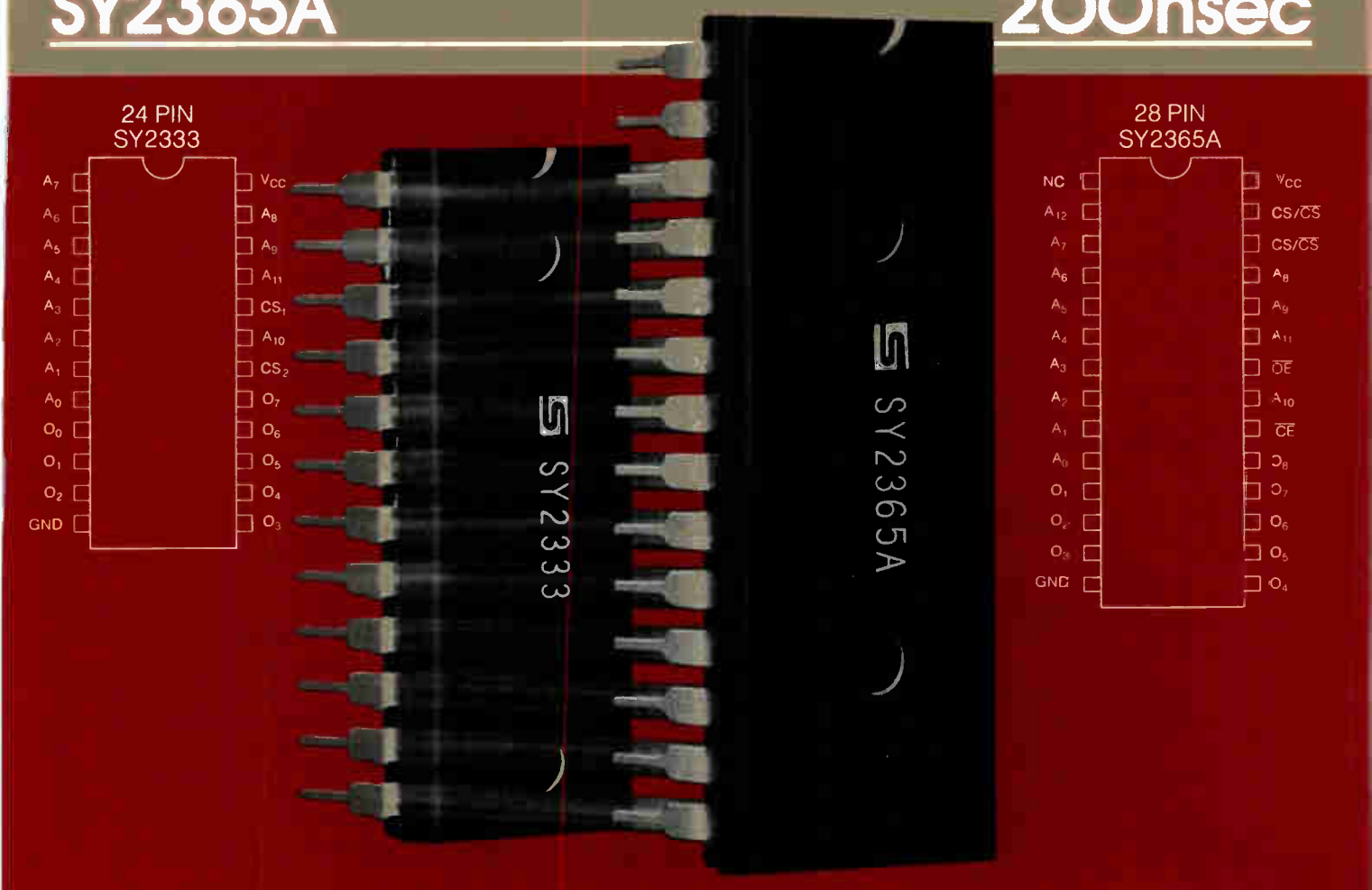
Synertek is a major MOS supplier of high volume parts with advanced technologies and techniques behind everything we make. ROMs. Static RAMs. Custom circuits. Single-chip Microcomputers. Systems. 6500 Microprocessors and Peripherals.



SYNERTEK

3001 Stender Way, P.O. Box 552
Santa Clara, California 95052
(408) 988-5600
TWX: 910-338-0135

SY2365A 200nsec



lary targeting consumer applications—numbers, "good evening," a-m and pm, and others. The 71002 is in the 4-bit format; the 71003 is in the 8-bit format. Samples will be available in early June, and quantity orders later that month.

Texas Instruments Inc., P. O. Box 202129, Dallas, Texas 75220 [342]

$340 keyboard sends Morse, ASCII, and Baudot codes

The MFJ-496 keyboard puts out Morse, Baudot, and ASCII codes for amateur radio and other radioteletype transmission. The $399.95 unit has two 256-character memories—one an error-forgiving text buffer and the other for four user-programmed messages—in which four automatic messages can be stored and later retrieved by button. A meter reads out the amount of room left in the text buffer, and an audible warning is given as the buffer approaches being full. The unit also has a deleting and a buffer-hold function, as well as automatic serial numbering.

Morse-code (continuous-wave) keying speed is set before transmission begins, and a meter reads the actual output speed. Two buttons initiate a cw or RTTY station identification. Five-level Baudot code is sent at 60 words per minute, the ASCII code at 110 b/s. The Super Keyboard can also be used as a full-function memory keyer just by plugging in a paddle. It operates on 9 to 12 v dc or from a $7.95 110-v ac adapter. For any units ordered directly from the manufacturer, there is a 30-day money-back trial period.

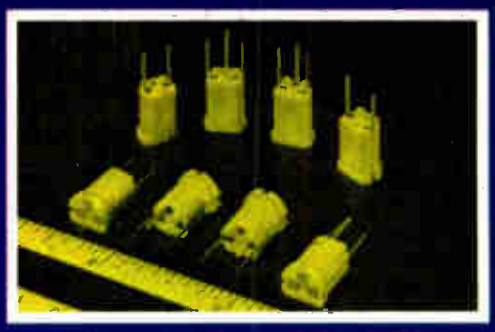
MFJ Enterprises Inc., P. O. Box 494, Mississippi State, Miss. 39762. Phone (800) 647-1800 [343]

DRO comes in 4-, 6-, 12-, and 16-GHz frequency ranges

The DO series of dielectric resonator oscillators is available in the 4-, 6-, 12-, and 16-GHz frequency ranges. They incorporate either silicon bipolar transistors or gallium arsenide field-effect transistors and can be provided with load isolation. Packaged in 1.0-by-1.5-by-0.75-in. packages, the DROs are suited for mili-

Interconnection City News

Methode Electronics, Inc.
7447 W. Wilson Ave.
Chicago, Il. 60656



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METHODE TAKES LEADERSHIP IN MASS TERMINATED IDC PRODUCTS.

CHICAGO —The JAGUAR system offers the speed, flexibility and economy that is required in today's new designs. It also provides a cost reduction replacement (with dimensional interchangeability) for existing systems with no sacrifice in performance or reliability.

WIRE-TO-POST SYSTEM

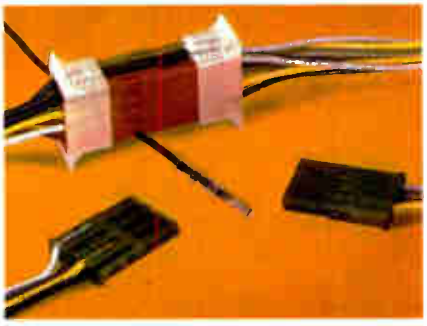
The original Methode JAGUAR Series is a complete wire-to-post interconnect system combining the proven reliability of the bellows contact, and the labor savings inherent with insulation displacement terminations.

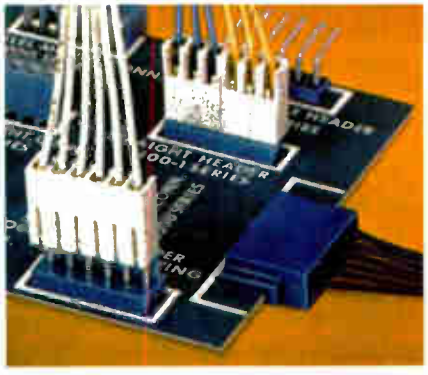
HIGH CURRENT TYPE

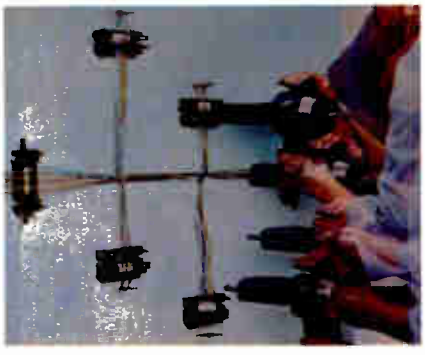
In November, 1979, Methode introduced its IDC power connector with unique modular construction and high current hermaphroditic contacts. For the first time, package designers can obtain the cost effectiveness of mass termination at current ratings up to 9 amps and voltages up to 250 VAC.

CARD EDGE CONFIGURATION

In February, 1980, Methode introduced its card edge connector version of the JAGUAR IDC family. Depending upon the number of terminations on the connector, the JAGUAR card edge system can save from a mimimum of 50% up to 90% of the labor time required for termination by solder or crimp type connectors.







CHICAGO —Developed for use with the JAGUAR Series mass termination connectors, our new harness terminator gun simultaneously terminates 2 through 24 position circuit harnesses at a rate of 500 assemblies per hour.

The air tool locks easily into IDC connector fixtures arranged to the harness shape on the assembly board . . . then trims and terminates the pre-positioned wires.

"DELTA-C" COMPLIANT OR PRESS-FIT TERMINALS NOW OFFERED FOR HYBRID RELI-APLANES

CHICAGO —These new Hybrid RELI-APLANE 200 amp press-fit backpanels permit higher density for faster computer switching . . . provide more critical voltage control at low levels . . . and eliminate the need for bus bars.

The 200 amp capacity is attained by incorporating solid copper plates up to .051" thick into a multi-level laminated or stacked construction.

"DELTA-C" compliant contacts provide a reliable high retention force that does not damage the plated-thru holes of expensive multi-layer backpanels.

SUPER-PLY FLEXIBLE FLAT CABLE JUMPERS WITH ROUND ENDS OFFER MORE FLEXIBILITY.

CHICAGO —SUPER-PLY flat wire jumpers offer exceptional flexibility and round-end conductors. Soft tin-plated wire is flattened along the jumper's internal length, however the conductor ends are left round. This provides improved flexibility over ordinary round conductors and eliminates the fragile ends encountered with flat or stranded wire.

CIRCLE 209 ON READER SERVICE CARD, OR CALL (312)867-9600 U.S.A.

New products

placed on dual in-line packages.

The thermometer consists of up to seven reversible indicator strips rated in successive 5°C increments whose color changes can be observed. The black color of the LCD strips changes to blue when the surface temperature is slightly above the rated temperature, which is printed on each black strip; it changes to green when within ±1°C of rated temperature; and it turns brown when slightly below the rated temperature.

For industrial applications, the thermometers come in the model 770-1, which has a range of 0° to 30°C and 32° to 86°F, and the 770-2, with a range of 30° to 60°C and 86° to 140°F. An introductory kit with three reversible models and three permanent temperature recorders is available for $10 if payment accompanies order for LCD Kit No. 2.

Telatemp Corp., P. O. Box 5160, Fullerton, Calif. 92635. Phone (714) 879-2901 [346]

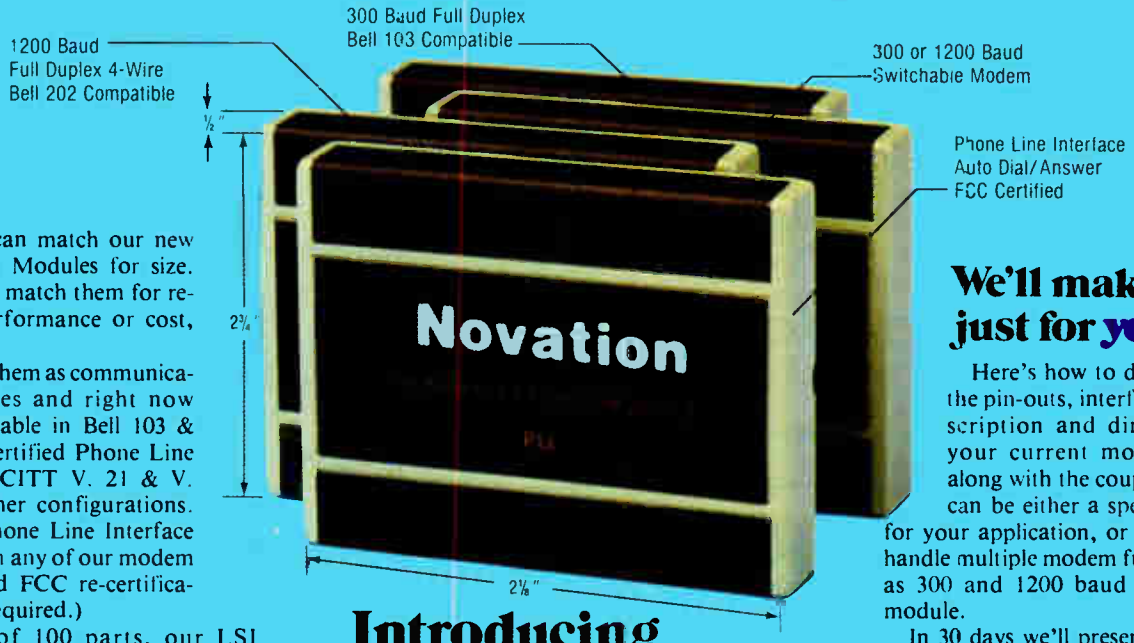
Computer-controlled rf filters cover from 48 MHz to 4 GHz

This family of digitally addressable tunable radio-frequency filters is computer-controlled and includes 22 models that cover 11 frequency bands between 48 MHz and 4 GHz. Each Chebyshev filter tunes over a 2:1 frequency range for full-octave coverage. The new filter, with its microprocessor-based control, tunes in less than 2 seconds and costs $2,500 for a single unit.

These filters should help eliminate the interference problem that exists at sites where several antennas are located in close proximity. The units can preselect frequencies in automatic test equipment and are useful for instantaneous frequency monitoring because they can identify incoming signals in wideband receiver systems. Production quantities are available in 60 days; small quantities are available in one week.

Telonic Berkeley, 2825 Laguna Canyon Rd., Laguna Beach, Calif. 92652. Phone (714) 491-9401 or outside Calif. (800) 854-2436 [348]

If you're now designing a low-speed modem into your system, you suddenly need a lot less space.



Introducing Novation's LSI Modem Modules

Nothing can match our new LSI Modem Modules for size. Nothing can match them for reliability, performance or cost, either.

Think of them as communication modules and right now they're available in Bell 103 & 202, FCC certified Phone Line Interface, CCITT V. 21 & V. 23—and other configurations. (Use our Phone Line Interface alone or with any of our modem modules and FCC re-certification is not required.)

Instead of 100 parts, our LSI Modem Modules have 11. All of which means that whatever your modem surface area is now, you can cut it by at least 1/3.

Performance is better. Reliability is better. Even the cost is a lot better. You'll save *at least* 10% compared with what you're now paying for low-speed modems.

The only way for you to know just how great our LSI Modem Modules are, is to have one for yourself.

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Here's how to do it: Send us the pin-outs, interface signal description and dimensions of your current modem card—along with the coupon below. It can be either a specific modem for your application, or one that can handle multiple modem functions such as 300 and 1200 baud in the same module.

In 30 days we'll present you with a working modem system that can be plugged right into your system. Tell us how many you need, and we'll hang a price tag on it, too.

Modem Modules are not hybrids. They're the world's first custom LSI low-speed modem series to include all analog and digital functions. And something of a small miracle.

Send in the coupon below, or if you want to get things going right now, just pick up the phone and call us today.

Yes, you've got me thinking. Tell me more.

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Title_____ Phone (_____)_____

Mail to: LSI Modem Modules, Novation, Inc., 18664 Oxnard Street, Tarzana, CA 91356

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Circle 213 on reader service card

Instruments

Digital recorder, computer team up

One-channel recording system catches 200-kHz transients, sells for under $5,000

Instrumentation used to analyze transients with frequencies to 200 kHz has traditionally been quite expensive and difficult to operate. But by modifying an inexpensive computer and adding its own waveform recorder and software know-how, GHI Systems Inc. has developed the Triad II system, which sells for as little as $4,950.

The least expensive version of the system is composed of a single-channel digital waveform recorder, the model VK12-1, and a model 2001 Commodore computer. Added to the computer is a special 8-K-byte RAM board that controls each of the 200 by 360 data points that can be put onto the computer's screen. The full-scale sensitivity of the cathode-ray-tube display is 80% of the recorder's, so if the recorder is set for 100 mV, the CRT display would be 80 mV full scale or 0.4 mV per line.

Making use of this high-resolution measurement capability for typical engineering tasks is quite easy, thanks to the operating software supplied with the system. Taking up about 4-K bytes of the computer's 32-K-byte RAM, the operating system supplies menus that prompt the user to select any of the eight operating modes with a single key.

Four of the eight operating modes permit measurement of amplitude, period, rise time, or frequency. The others allow data to be integrated, stored for recall, or displayed in either condensed or expanded form. For each mode, the CRT will display the value selected by a cursor directly in engineering units, and the measurement period can be varied from less than a millisecond to several seconds.

Expert or not. For speed, the actual data plotting, transfer, and cursor functions are done by a machine-language subroutine called by the Basic operating program. So while an inexperienced operator can use the system without any programming knowledge, an experienced one can use the machine-language code developed by GHI to develop specialized programs that will provide the performance needed.

Connection to the signal source can be made directly or, since the transient recorder input is 1 MΩ, 40 pF, with typical oscilloscope probes. Since input sensitivity is adjustable, the system can easily be used with a wide range of transducers such as accelerometers, load cells, pressure transducers, and photodiodes, to name a few. A $6,490 dual channel version that uses the VK22-2 recorder is also available, as are custom programming consultation and special systems using other VK-series recorders.

GHI Systems Inc., 6217 Picardie Rd., Rancho Palos Verdes, Calif. 90274. Phone (213) 548-6544 [351]

Multifunction counter fits in small panel area

Measuring just 3 by 2.15 by 1.75 in., the PC-6 is a programmable, six-digit counter designed for panel mounting. The 7-oz, dual-input instrument can read frequency to 10 MHz, give a frequency ratio of channel A to B, measure a period from 40 ns to 0.999999 s, note a time interval of as little as 250 ns, or work as an accumulating counter.

All functions, input ranges, and the slopes of either input can be programmed manually from the front panel or electrically by TTL-compatible digital inputs. The unit reads out on 0.3-in.-high light-emitting diodes and requires regulated +5 V dc, 350 mA power. In single quantities, the PC-6 sells for $179. Deliveries are in two weeks.

Datel-Intersil, 11 Cabot Blvd., Mansfield, Mass. 02048. Phone (617) 339-9341 [353]

LSI ups performance of frequency counters

A counter on a chip, designed and made in-house at Philips Test & Measuring Instruments Inc., meshes with the one-chip microcomputer inside the company's 6670 series of high-accuracy frequency counters, reducing their size and extending the speed and reliability with which they

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Circle 217 on reader service card

New products

can count and handle signals.

The 120-MHz PM6674, 550-MHz PM6674, and 1,500-MHz PM6676 have a maximum input sensitivity of 10 mV. A wideband continuously variable input attenutator ensures error-free triggering by allowing optimum matching of trigger sensitivity. Moreover, in conjunction with a built-in noise filter, it also ensures immunity to noise over a wide dynamic range from 20 mV peak to peak to 10 V p-p. A choice of five crystal oscillators, rated at an accuracy of to within $5 \times 10^{-10}/24$ h makes it possible to match each instrument's stability to a particular application's needs.

Options include battery operation for field testing. The three units sell in their basic configurations for $800 to $1,500 and are available now. The direct-gated 600-MHz PM6675 will be available in the fall.

Philips Test & Measuring Instruments Inc., 85 McKee Dr., Mahwah, N. J. 07430 [354]

4½-digit DMM computes, measures rms ac to 20 kHz

The 6504 microcomputer-based portable 4½-digit multimeter from Weston Instruments has a base price of $690, which is low for an instrument with its accuracy and complement of features. It has five ranges each of dc and ac voltage and current, and six resistance ranges, with a basic accuracy specified as ±0.03% ±2 counts. True-root-mean-square ac measurement extends to 20 kHz.

The 4-lb 6504 measures 8.66 by 3.25 by 10.25 in. deep. It supplies easy-to-use computing power for field, shop, or lab. The computing modes are Ax + B, percent deviation, null, minimum and maximum moni-

The New µP-Based Scalar Network Analyzer System.

Running it is as simple as A, B, C, D, E, F!

It's a Wiltron. You're going to make accurate automated measurements far easier using the new Wiltron Series 5600 Automated Scalar Network Analyzer from 10 MHz to 40 GHz. And for less!

You'll discover this 3-element system offers a much better way to measure return loss, transmission loss or gain and power automatically. You'll find the powerful Wiltron Series 5600 features distributed microprocessor architecture and storage of 99 test set-ups.

40 dB Directivity. Series 5600 offers 40 dB directivity over a 10 MHz to 18 GHz continuous sweep range. Dynamic range is 66 dB with −50 dBm sensitivity. The system offers 82 dB attenuation programmable in 0.1 dB steps. ROM corrected frequencies are accurate to +/− 10 MHz from 10 MHz to 18 GHz. Six models span the 10 MHz to 40 GHz range.

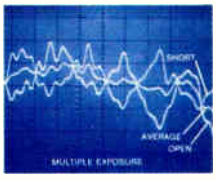
The new 6600 Programmable Sweep Generator, a key element. Fundamental oscillators used in the 6600 avoid substantial errors generated by the harmonic products of multiplier type oscillators. The result, low harmonic content, −40 dBc, 2-18.6 GHz, low residual FM and greater stability.

Unpack and you're ready to go. Connect the SWR Autotester and detector, plug-in the factory programmed cartridge, turn on the power, enter a few simple inputs and you're ready to measure. It's all as...

Simple as A, B, C, D, E, F!

A. System Setup
Enter date and type of measurement.

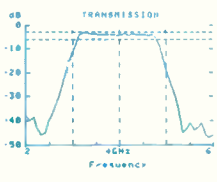
B. Frequency Selection
Enter frequency range limits and frequency step size of number of test points.



C. Calibration
Enter ID for device under test. Select averaging of open/short residuals and store normalized residuals.

D. CRT display of characteristics
Select marker frequencies and amplitude limits and adjust device under test, if necessary.

E. Measurement
Press key to start automatic measurement sequence.



F. Hard-copy output
Select plotted curves or tabular data.

Ask for an early demonstration, write for 16 page brochure. Call Walt Baxter, (415) 969-6500 or write Wiltron, 805 E. Middlefield Road, Mountain View, CA 94043.

toring, high and low limits, and filter. The filter mode minimizes bounce due to noise by displaying a binary-weighted average of the last four measurements. Conversions occur at 2.5 to 5 per second, depending on input level.

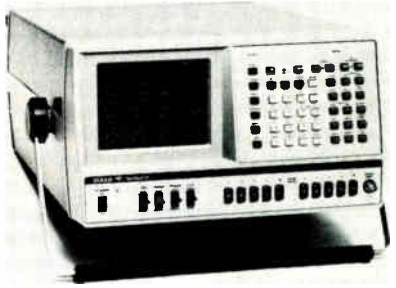
Options include an IEEE-488-bus interface, rechargeable battery with eight hours of operation, and a probe that permits freezing a display remotely to allow the operator to focus on the probe tips. Probes extending the unit's ac voltage capability to 50 MHz and 520 MHz, its dc voltage to 50 kV, and its ac current range to 200 A (clamp-on) are also available, as is a −50°-to-+150°C temperature probe. Delivery is in 30 days after receipt of order.

Weston Instruments, 614 Prelinghuysen Ave., Newark, N. J. 07114 [355]

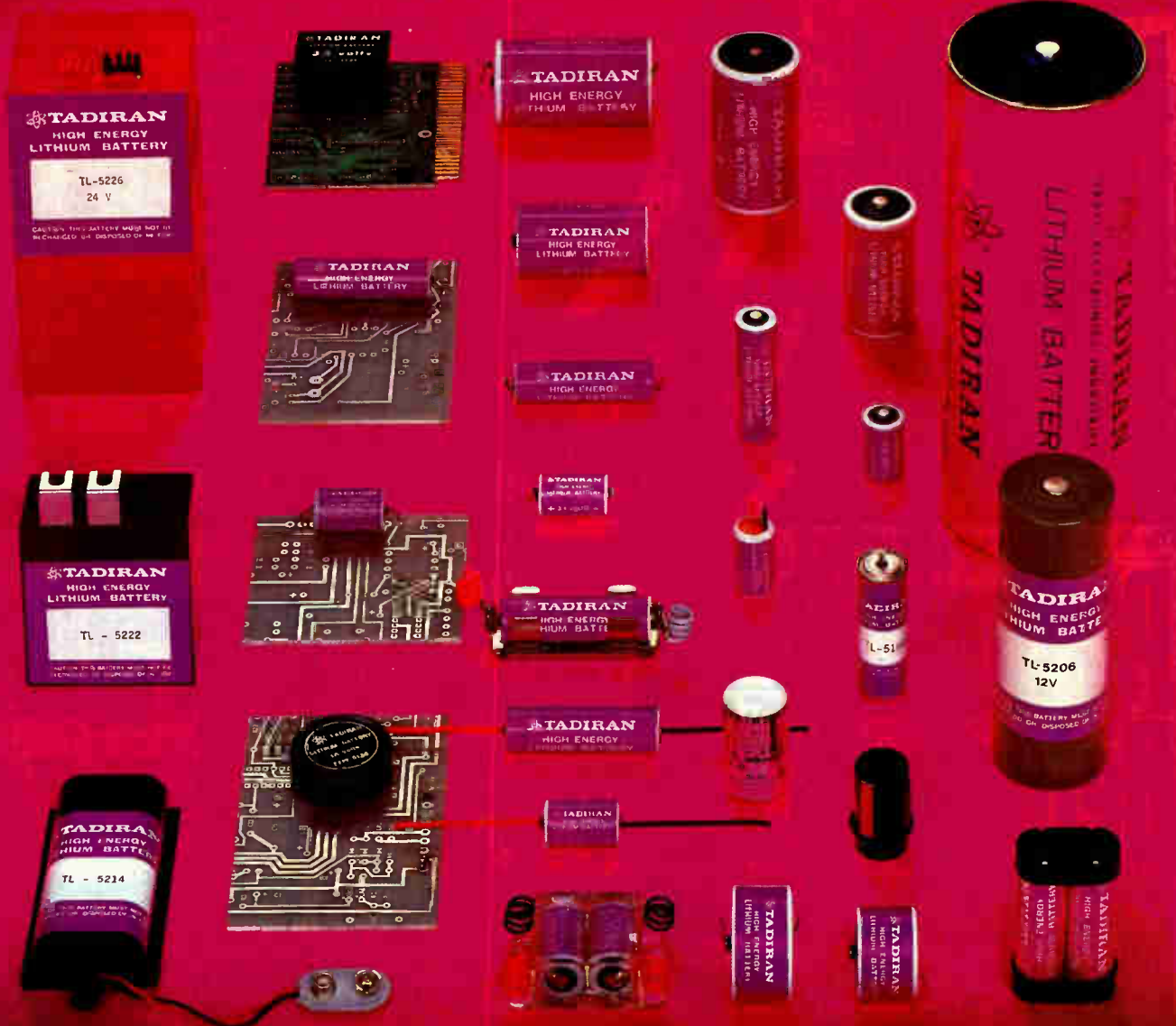
High-speed logic analyzer has 2-ns timing resolution

The 500-MHz clock rate of the eight-channel K500-D logic analyzer gives it the ability to capture and sample glitches or transitions every 2 ns. The unit is based on an 8086 processor and 2-K words of random-access memory. Its analog capability depends on a 100-MHz 4-bit analog-to-digital converter. An analog waveform can be displayed with four digital signals, or eight digital signals can be shown as timing diagram, binary, octal, or hexadecimal ASCII representations. Eight 6-ft active probes come with the $22,625 unit; deliveries begin in June.

Gould Inc., Biomation Division, 4600 Old Ironsides Dr., Santa Clara, Calif. 95050. Phone (408) 988-6800 [356]



Sentence your CMOS-based equipment to a lifetime of hard labor - with a TADIRAN™ lithium inorganic battery.



The Tadiran Lithium Inorganic Battery, with a shelf-life of more than ten years and a very flat discharge curve, can be mounted on a printed circuit board and forgotten. It is the ideal power source for CMOS circuits for applications in advanced telephony equipment, industrial controls, data processing, sensing and monitoring devices, microwave transmission equipment, and portable instrumentation.

Australia: Technico Electronics Ltd., Sydney, Tel. 02-427-3444; **Austria:** Sonnenschein GmbH, Linz, Tel. 0732-55529; **Belgium:** S.E.B. Souriau, Bruxelles, Tel. 02-2423370; **Canada:** CPU Electronic Components Ltd., Point Claire, Quebec, Tel. 514-697-8286; **Denmark:** Erik Westerberg A. S, Herlev, Tel. 02-929-000; **France:** Diode, Fresnes, Tel. 02-666-9801; **Germany:** Accumulatorenfabrik Sonnenschein GmbH, Buedingen, Hessen, Tel. 06042-91; **Italy:** Compelet, Milano, Tel. 02-688-8196; **Japan:** Union Engineering Ltd., Kobe, Tel. 078-331-2270; **Netherlands:** Sonnenschein (Netherland) B.V., Arnhem, Tel. 085-455041; **Norway:** Ingenior Harald Benestad AS, Oslo, Tel. 02-555-190; **Spain:** Diode, Madrid, Tel. 01-455-0139, 01-455-3686; **Sweden:** Mittor AB, Solna, Tel. 03-823-210; **Switzerland:** Metronic AG, Zurich, Tel. 01-418484; **United Kingdom:** Suvicom Ltd., Shirley, Solihull, West Midlands, Tel. 021-745-3251; **USA (East & Midwest):** Plainview Electronics, Plainview, N.Y., Tel. 516-249-6677; **USA (West, Alaska & Hawaii):** Carefree Unlimited, Placentia, Ca., Tel. 213-323-0603, 714-996-9400

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Circle 221 on reader service card

Communications

Ethernet boards aid software work

Boards provide physical-link and data-link control for net evaluation and development

The interest in Ethernet local networks has snowballed since specifications were published last year. To ensure that this interest does not melt away, Intel Corp. is about to make available its first Ethernet offerings, among them a board-level controller that will give designers a way of developing applications software and evaluating the network prior to the availability of Ethernet-based production hardware.

The two Ethernet controller boards will be shown at the National Computer Conference in Chicago. They provide the physical and data-link control interface as described in the specifications published jointly by Intel, Digital Equipment Corp. and Xerox Corp., [*Electronics*, Oct. 23, 1980, p. 42].

Designated the iSBC 550, the pair of controller boards is compatible with Intel's line of Multibus single-board computer products. They use the firm's high-performance iAPX 88/10 (formerly 8088) 8-bit microprocessor, as well as 8-K bytes of erasable programmable read-only memory, 16-K bytes of random-access memory, and a separate 8-K bytes of RAM configured for direct memory access to support high-speed operation.

According to Bob Brannon, marketing manager at Intel's OEM Microcomputer Systems group in Hillsboro, Ore., "the iSBC 550 is designed to offer users a quick means to implement Ethernet control in an iSBC-based prototype. It is also a cost-effective solution for rapid market entry of a moderate number of production systems," he adds.

Most of the development work that Ethernet systems designers will be faced with, Brannon says, is software-related. "They don't need to be concerned with what the controller looks like at this time, be it a board or a chip, but rather with being able to develop software so they can get their systems on the network quickly." Brannon doesn't expect any supplier to hit the market with significant Ethernet end-user products in less than two years. "By that time, we'll have our component-level, very large-scale integrated controller available to solve the needs of high-volume system designers," he adds.

The first two layers in Ethernet's multilayered architecture are the physical- and data-link layers. "These layers are the least application-specific," Brannon continues, "and therefore most appropriately implemented in hardware and firmware."

One of the two controller boards will provide the medium-scale-integrated serial interface that satisfies the 10-Mb/s transceiver specification. The other board, with the iAPX 88/10 on it, will serve as the physical-link and data-link controller. As a physical-link controller, it is responsible for cable access and the actual transmission and reception of Manchester-encoded message signals onto and from the cable. Except for the actual transceiver hardware, Brannon notes, "all of the specifications described in the joint Ethernet publication are fully implemented by the iSBC 550."

Control layer. The data-link–control layer, Brannon explains, is responsible for arranging the message in the specified Ethernet frame sequence, including the appending of the 32-bit Autodin cyclic-redundancy-check value. This layer also enforces one-at-a-time cable access and handles the errors during collisions, or multiple accesses.

Application programs for Ethernet-linkage prototypes can be developed in the same manner as programs for any iSBC-based system, Brannon says. The iSBC 550 works under Intel's real-time multitasking executive (RMX) operating system. Consequently, application programs executed by iSBC central-

1 TECHNOLOGY FOCUS.

First in a series of reports to detail the custom MOS, Bipolar and hybrid research and production underway at Sperry Univac's Semiconductor Division. This account highlights historic engineering accomplishments and describes current opportunities in MOS, Bipolar and Thick Film development.

FOR THE RECORD.

Sperry Univac's engineering legacy spans over three decades of uninterrupted commitment to the computer industry. It began in 1946 when we introduced the world's very first electronic digital computer. As the success of this development snowballed, so did progressive innovations which included: the first solid state processor, the first use of magnetic cores, drums, thin-film memories, real-time applications, and nano-second computers.

Technical excellence has proved vital to gaining and retaining a substantial segment of the computer user market. Today, Sperry Univac's installed systems base is valued at over $11 billion, second only to IBM.

FOR PROGRESS.

The needs of computer users have grown as sophisticated as the equipment they buy. The immediate promise for VLSI applications has substantially heightened user expectations for attaining record-breaking levels of cost-efficient productivity.

To satisfy this market objective while continuing to provide competitive and reliable computing power for applications ranging from medical research to pipeline construction, millions of dollars have been invested to establish an advanced in-house R&D semiconductor facility.

The challenge of gearing up this new Division is continuing to attract some of the best engineering minds in the field. In a brief three-year period, these professionals have effectively designed, developed and implemented custom techniques utilizing Schottky TTL, CMOS, NMOS and high speed ECL circuits using double and triple level metalization employing 2 micron type device structures.

FOR MORE.

Backed by Univac's corporate research investment of $189 million, current development programs are accelerating in areas of E-beam lithography, laser annealing, submicron device physics, and refractory metal silicide gate structures.

SEMICONDUCTOR OPPORTUNITIES.

The anticipation of further VLSI developments has created a uniquely dynamic and rewarding working environment at Sperry Univac. With more significant opportunities still to come, challenging positions exist in a wide range of disciplines.

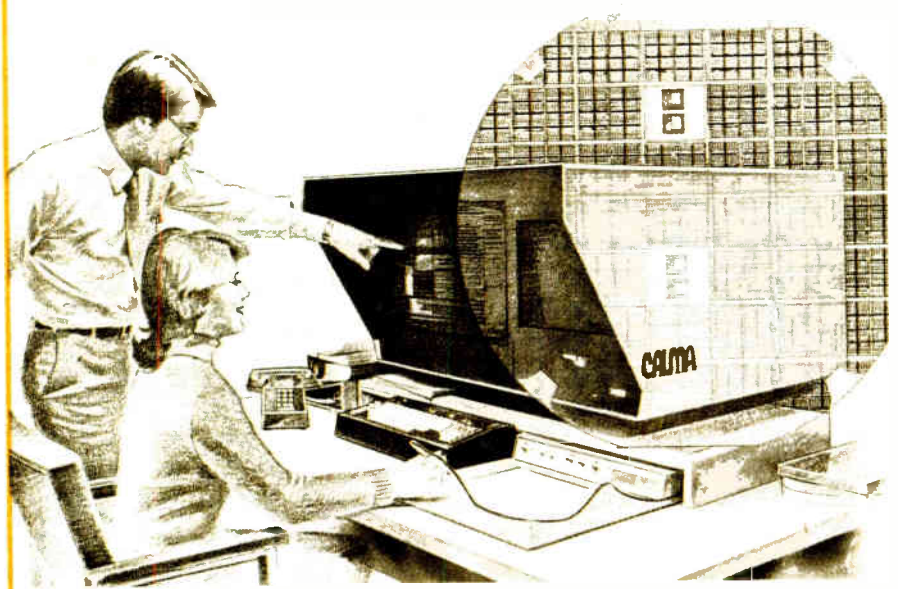
Bipolar Project Engineer/ Manager – Requires background in product or customer engineering for responsibilities involving the design, fabrication, assembly, testing, and systems implementation of advanced ECL, VLSI and analog integrated circuitry. BSEE or MSEE with 2+ years experience in engineering or marketing above technologies. Budget management experience also desired.

HMOS Product Engineer – BS or MS in EE or physics for position in VLSI device development environment. Requires 2+ years product engineering experience.

Thick Film Technology/Sr. Process Engineer – Extensive experience in fabrication of thick film circuits. Will be responsible for all aspects of thick film screen printing and firing, including: process specifications, material usages and capital equipment selection, and production aspects. Management potential.

MOS Circuit Design Engineer – 2 year minimum CMOS or NMOS circuit design experience. VLSI + complexity with 2 micron channel lengths.

Facilities/Equipment Engineer – Experience in semiconductor facility construction, plant engineering, or equipment evaluation and maintenance desired.



CONTACT:

Call Bill Dahlen collect: (612) 456-2894, or send a resume to his attention at Sperry Univac Semiconductor Division (E), Y11D1, P.O. Box 3525, St. Paul, MN 55165.

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SEMICONDUCTOR DIVISION

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Circle 225 on reader service card

New products

processing-unit boards can pass messages to the Ethernet controller with the support of Multibus message-exchange software.

Intel's Intellec microprocessor development system can be used to write Ethernet applications software, as can a new Ethernet development system that the firm will also unveil at NCC. The latter will enable users to link up two Intellec mainframes and evaluate programs in a realistic network environment. These programs will be usable in the actual target system, as well. Similarly, programs written for the board-level controller will be compatible with the VLSI controller, slated for introduction in 1982.

Scheduled for delivery around the first of next year, the iSBC 550 controller-board pair for physical- and data-link Ethernet control will sell for about $4000.

Intel Corp., 3065 Bowers Ave., Santa Clara, Calif. 95051 [401]

300-b/s modem connects directly or acoustically

The LEX-12 is a 300-b/s modem for the personal computer and terminal markets. It can be directly coupled at the telephone handset jack to the phone line to provide immunity to acoustic noise and distortion. Acoustic coupling through the telephone handset allows the modem to be used where no direct-connection possibilities exist.

The LEX-12 can communicate with the LEX-11 acoustical modem, Bell 100 series–compatible modems, and other LEX-12 modems and can be used with any other phone by

Mallory tantalum capacitors earn top MIL reliability ratings.

In solid tantalums, Mallory is now qualified to provide Level S, the highest reliability rating, for styles CSR 13 and CSR 91. Level S, under MIL-C-39003, means a life failure rate of only 0.001% per 1,000 hours. Here is our current QPL line-up in solids:

MIL Style	Mallory Type	Life Failure Rates
CSR13	TER	M, P, R, **S**
CSR23	TXE	M, P, R
CSR33	TXR	M, P
CSR91	TNR	M, P, R, **S**

In wet slug tantalums, we have become the first source qualified at Level R, under MIL-C-39006, for style CLR69 — the extended capacity range wet tantalum, which makes our wet QPL list look like this:

MIL Style	Mallory Type	Life Failure Rates
CLR10	XTM-XTK	L, M, P
CLR14	XTL-XTH	L, M, P
CLR17	XTV	L. M. P
CLR65	TLX	L, M, P, R
CLR69	TXX	L, M, P, **R**

They're all available from authorized Mallory Distributors. Send for our latest QPL bulletins. Mallory Capacitor Division, Mallory Components Group, P.O. Box 372, Indianapolis, Indiana 46206. (317) 636-5353.

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ELECTRICAL/ELECTRONIC GROUP

EMHART

Circle 227 on reader service card

Honeywell

Circle 229 on reader service card

New products

The 3705-80 controllers can be attached to the IBM 4300 processors, System/370 and 303X processors, and many System/360 processors operating in an IBM 2701, 2702, or 2703 emulation mode.

The 4-line model M81 and its channel adapter sell for $39,940. It can be leased for $1,314 a month on a two-year agreement or rented at $1,544. The 16-line model M83 and adapter is priced at $55,940, leased for $1,954, or rented at $2,296. Both 4- and 10-line models will begin shipments in the second quarter of this year; the 16-line model will begin deliveries in the third quarter.

IBM Corp., Data Processing Division, 1133 Westchester Ave., White Plains, N. Y. 10604 [405]

Fiber-optic data multiplexer has 16 ports, backup system

The model LDM-9500 multiplexes up to 16 Electronic Industries Association RS-232-C data channels in asynchronous or synchronous formats at rates from dc to 19.2 kb/s and from dc to 64 kb/s, respectively, for full-duplex transmission over a pair of optical fibers.

According to the company, the LDM-9500 is guaranteed to provide a continuous flow of data using a redundant hot standby transmission system. If any components fail or a fiber is broken during transmission, the backup system will automatically turn on. Also available are 16- and 8-port unprotected versions.

The LDM-9500 multiplexer features a standard diagnostic and visual indicators for easy monitoring of both channel and system status and full RS-232-C handshaking capability. It accepts the EIA 25-pin electri-

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TRW metal films with muscle are offered in popular RL05 to 32, RN55 to 65, and industrial equivalents. For standards in all types of resistors, contact your local TRW distributor. Or TRW/IRC Resistors, an Electronic Components Division of TRW, Inc., Greenway Road, Boone, N.C. 28607. Dept. G (704) 264-8861.

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Circle 272 on reader service card

New products

cal plug as its input and converts it directly into optical digital transmission. CCITT and MIL Standard 188 interfaces are optionally available. The unit is powered from a wall outlet and is available in desktop- or rack-mounted configurations. The 16-port fully protected unit costs $6,000.

Valtec Corp., West Boylston, Mass. 01583. Phone (617) 835-6082 [406]

Smart RS-232-C modem dials with pulses or tones

Smartmodem, an intelligent data-communication system approved by the Federal Communications Commission, has been designed to be used with RS-232-C–compatible computers or terminals, to communicate through the telephone system with other computers or time-sharing systems. It is program-controlled to analyze and execute commands in any language by means of ASCII character strings.

Smartmodem has automatic dialing and answering capabilities; an audio monitor to allow the user to follow the progress of the call and watch for wrong numbers and busy signals; set commands that select various operational parameters such as dialing speed, escape code character, and number of rings to answer on; and light-emitting-diode indicators on its front panel to show the unit's operational status. Power-on default options are controlled by seven switches; four of the options can be overridden by a software command.

The system can be connected to any telephone system in the U. S. since dialing can be either Touch Tone or pulse, says the manufacturer. It operates in full- or half-duplex at a rate of 0 to 300 b/s. The suggested retail price for the Smartmodem is $279, which includes a power pack, one modular telephone cable, and an owner's manual. There is a two-year limited warranty.

Hayes Microcomputer Products Inc., 5835 Peachtree Corners East, Norcross, Ga. 30092. Phone (404) 449-8791 [407]

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Circle 274 on reader service card.

Software

Unix look-alike runs on Z8002

Multiuser, multitasking operating system package includes numerous utilities

Original-equipment manufacturers using the Zilog Z8002 microprocessor have another operating system choice. The Coherent operating system from the Mark Williams Co. is source-code–compatible with version seven of Unix from Bell Laboratories. The Chicago-based company originally developed Coherent independently of Bell for use on PDP-11–type minicomputers but has now transported it to the Z8002. Coherent is written almost entirely in C, except for about 400 lines of assembly language in the kernel, making it easy to transport to other machines. The company plans to transport Coherent to Motorola's 68000 next, with several other adaptations in the works.

Coherent is a multiuser, multitasking operating system that features, like Unix, device-independent input/output, a command line interpreter (called the shell) that is adaptable to particular applications, pipes (the ability to direct the output of one program to the input of another from the user console), a tree-structured file system, loadable device drivers, and fast disk access through a buffer cache. It encompasses over 100 utilities, including an assembler, debugger, and C compiler for the Z8002; it also includes versions of such popular original Bell Labs utilities as Lex, a regular expression analyzer and YACC, a compiler compiler for producing custom languages.

The Z8002 version of Coherent looks the same to the user as the PDP-11 version; all C programs already developed for Coherent can be run under the new version. Furthermore, the user has access to the large number of programs written to run under Unix itself. But with Coherent, OEMs should be able to configure systems at a lower cost than the original Unix. An ISO standard Pascal and XYBasic will also be available soon.

Coherent is available under several flexible licensing agreements. It is $20,000 for the Z8000 source code, and royalties start at $500 per machine, with outright purchase options also available.

Mark Williams Co., 1430 W. Wrightwood Ave., Chicago, Ill. 60614. Phone (312) 472-6659 [371]

8086 OS supports multiple users

Compatible with CP/M-86, real-time operating system is multitasking for each user

The first multiuser operating system for the 8086 microprocessor has arrived—the MP/M-86 from Digital Research, which developed the CP/M operating system for 8080-based systems that is now in use in over 200,000 installations.

MP/M-86 is a real-time operating system that allows multitasking for each user signed on with the computer. It is compatible with CP/M-86—the single-user version—but adds many new features like file and record lockout, password protection of individual blocks as small as 128 bytes, time and date stamps on disk records, and the capability of handling 8 gigabytes of storage using random and sequential file access.

The designer of MP/M-86, Frank Holsworth, received his degrees from Stanford University, where he had extensive experience with the inner workings of the Unix operating system from Bell Laboratories. He has built into MP/M-86 many of the facilities that make Unix as popular as it is. Standard input/output allows the input or output of a program to be redirected to any I/O device without changing code in that program. The user merely informs the processor from the console which I/O device he wants to use.

The terminal message processor (TMP) is the program that communicates with the user in much the same way that the Unix shell does. It has been specifically designed for easy modification by the original-equipment manufacturer to produce a custom version that serves a unique application, say, for word processing or data-base queries. It also includes a function—commonly called a submit facility—that allows files of TMP commands to be executed not only by a single command from the user console but also when called from a program that is running.

MP/M-86 also supports pipes, mutual exclusion between tasks (for instance, reading and writing a disk but not both simultaneously), and synchronization between tasks, all of which make extensive use of queues. It handles both interrupt-driven and polled I/O devices.

The original release is configured for an Intel iSBC-86/12 computer with an Intel 204 floppy-disk system, but like CP/M it is designed for easy reconfiguration by the OEM to its particular hardware. It runs in 20-K bytes with a minimal real-time version for embedded applications requiring only 7-K bytes. It will be priced at under $500 and will be available in 90 days.

Digital Research, P. O. Box 579, 801 Lighthouse Ave., Pacific Grove, Calif. 93950. Phone (408) 649-3896 [372]

6809 executive software controls 255 tasks at once

When equipped with the RMS09 real-time multitasking executive package, an M6809 Monoboard microcomputer, the M68MM19 Micromodule, or any 6809-based microcomputer system can simultaneously control up to 255 different

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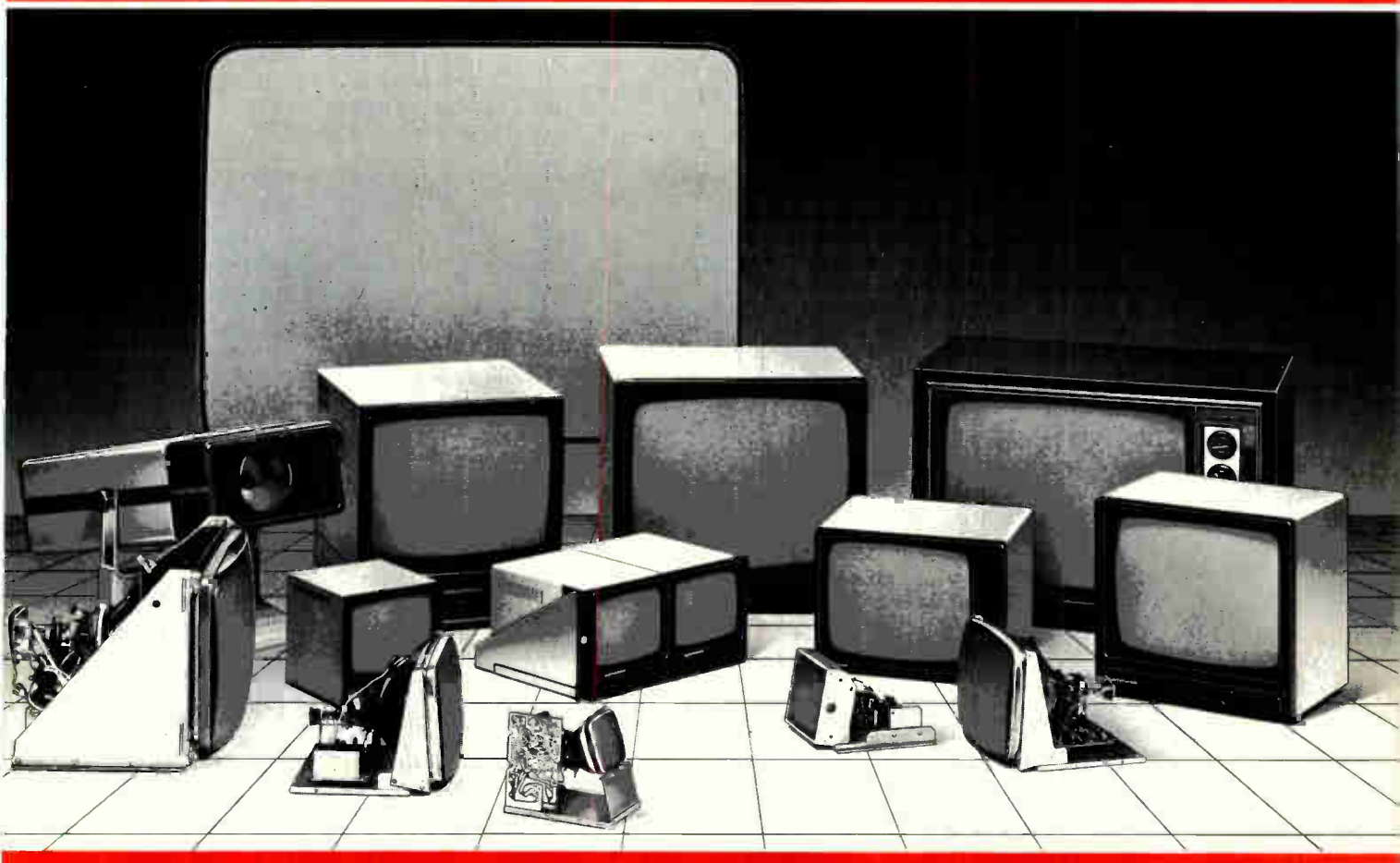

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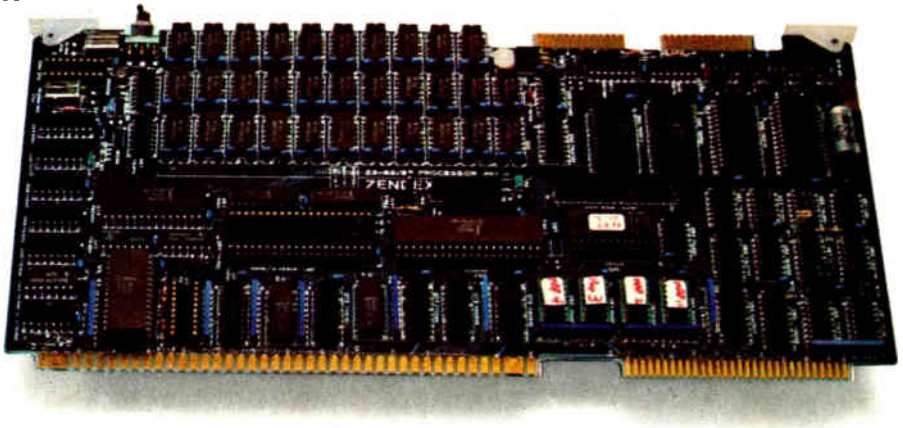
The ZENDEX ZX-88 is a versatile CPU 8board compatible with the INTELLEC[1] Series II Development System. CP/M-86[2] from ZENDEX allows the ZX-88[3] to boot and run the CP/M[2] software resident within the MDS. The ZX-88 can also have its CPU chip exchanged for an 8085A-2 to allow compatibility with ISIS-II and CP/M-80[2].

Since June of 1980, our customers have used the ZX-85/88 as an extra Development System or an upgrade to the MDS. During this introduction of the ZX-88, ZENDEX will provide (at no extra charge) a copy of the CP/M-86 on an INTEL format MM FM diskette. ZENDEX also offers an INTEL format compatible Disk Controller Model ZX-20DA that is an excellent choice for use with the ZX-88.



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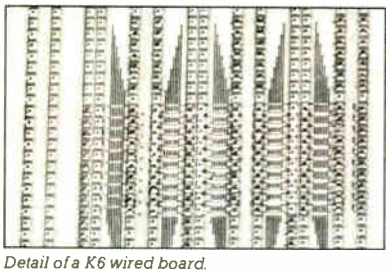
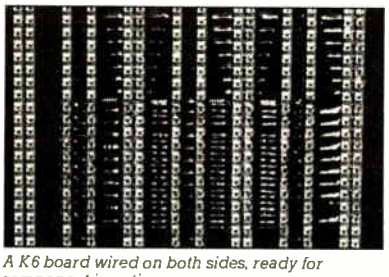
Circle 236 on reader service card

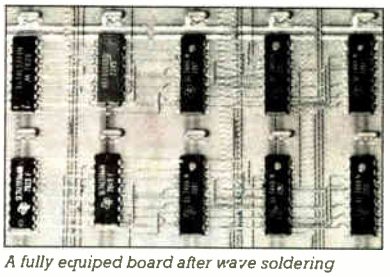
K6 divides by 10 the wire – weaving time for prototypes.



Detail of a K6 wired board.



A K6 board wired on both sides, ready for component insertion.



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Speed: after computer-aided programming, all wiring operations are automatized.
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Evolution: K6 system is the only one suitable to the new generation of components, avoiding plated-through holes and using surface mounting (chip carriers).

K6 **the new interconnection**
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tasks. The package is useful in both development system and application system environments.

Supervisor calls included in the executive control task synchronization manage resources and handle time-dependent operations (a hardware timer must be part of the system to implement the variety of timer options). Provision is made for all types of interrupts, and interrupt response time is fast: 150 μs. Input/output operations are device-independent, handling custom I/O environments and standard asynchronous-communications interface adapters and peripheral interface adapters. Supplied system routines can be used, or the user can configure his own customized directives and interrupt-handling routines. The system-generation process is flexible enough to set up as simple or as complex a system as is desired. An optionally configurable system monitor provides specialized control and debugging commands.

The M6809 RMS09 resident real-time multitasking system package on MDOS diskette for the M6809 EXORciser development system is priced at $2,700. A user's guide can be had for $10. The software is available now, as is quantity pricing.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 244-5714 [373]

Plain-English–query software is adapted to VSAM, Adabas

Two new versions of the Intellect query system operate directly with data bases managed by IBM Corp.'s Virtual Storage Access Method and Software AG's Adabas data-base management system. They will be released in June. The language currently runs on IBM 370 computers and interfaces with both IBM's Time Sharing Option, its conversational monitor system, and its Customer Information Control System.

Intellect is a software package that makes it possible for users to communicate with their data bases in conversational English. It can

New products

interpret complex sentence structures, pronoun references, and even sentence fragments and poor grammar. It also responds to the queries in English, so that company personnel may use the data base without the aid of the data-processing staff.

Thanks to an expandable vocabulary, Intellect can be customized to a user's specific application, data, and linguistic style. It prepares a daily list of queries it was unable to answer, to show quickly what new words should be added to its vocabulary. The software package also sorts data, performs statistical and arithmetic functions, generates bar graphs and formatted reports, and carries out process linking, logging, and data-security functions.

Intellect is available under a perpetual licensing agreement or a one-year license arrangement.

Artificial Intelligence Corp., 200 Fifth Ave., Waltham, Mass. 02254. Phone (617) 890-8400 [374]

Multitasking operating system for 68000 supports Pascal, C

Idris is a general-purpose multitasking operating system for the Motorola 68000 microprocessor that was written for Chromatics Inc.'s 68000-based CGC 7900 color graphics computer. Priced at $2,000, it supports compilers for C and a version of Jensen and Wirth Pascal. The compilers cost $1,000 each.

Idris includes a 68000 assembler and text editor. An assembler and text editor for CGC 7900s running under the firm's previously announced disk operating system are available now for $1,000 and $750, respectively. A Basic interpreter can be had later this summer for $750.

"We believe Idris will give the CGC 7900 an operating flexibility that normally isn't found yet in color graphics systems [based on 16-bit central processing units]," says Lowell Coulson, a Chromatics marketing executive.

Chromatics Inc., 2558 Mountain Industrial Blvd., Tucker, Ga. 30084. Phone (404) 493-7000 [375]

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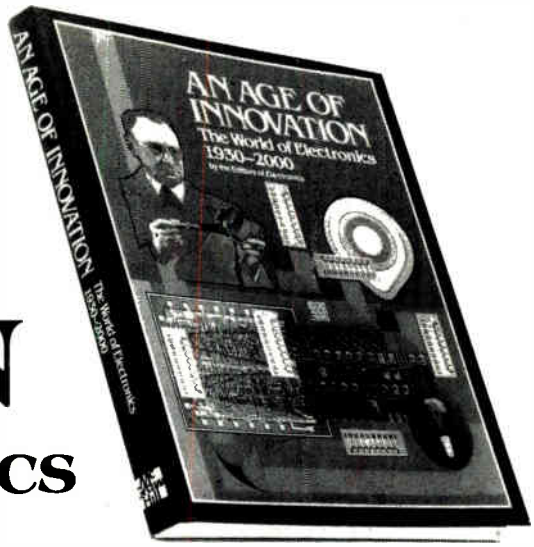

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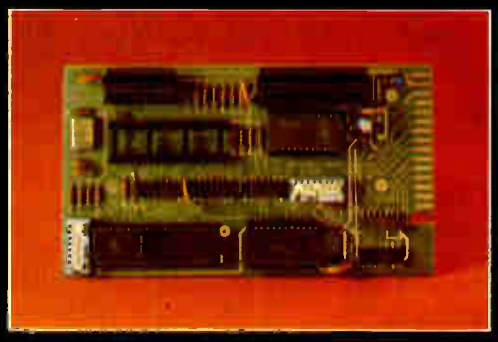

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Products newsletter

Thinner design rules yield 55-ns 8-K PROM

Monolithic Memories Inc. is showing samples of a fast (55-ns) version of its 8-K programmable read-only memory. The Sunnyvale, Calif., firm improved upon the speed of the Nichrome-fused PROM by going from 4- to 2-μm design rules and from a 3-in.-wafer, negative-resist process to one using 4-in. wafers and a positive resist. As a result, the 6381-2 is about three quarters the size of the earlier, 90-ns 6381-1; has about double the yield; and **costs a third less, or around $12.** Also, the new part fits in a 24-pin skinny dual in-line package.

National, Harris agree on pinouts for codec chips

As part of a long-term agreement on specialized telecommunications integrated circuits, National Semiconductor Corp. of Santa Clara, Calif., and the Harris Semiconductor Group of Melbourne, Fla., intend to produce complementary-MOS codec-plus-filter chips to pinout standards developed by National together with Eurotechnique SA of France, a joint venture of National and the St. Gobain group. **The aim is to enlist the participation of other French manufacturers in making the parts a *de facto* worldwide standard.** Second-source information has already been exchanged on National's C-MOS filter and codec parts, as well as details on Harris's advanced SLIC (subscriber-loop interface circuit) design.

France's EFCIS to build AMD modem

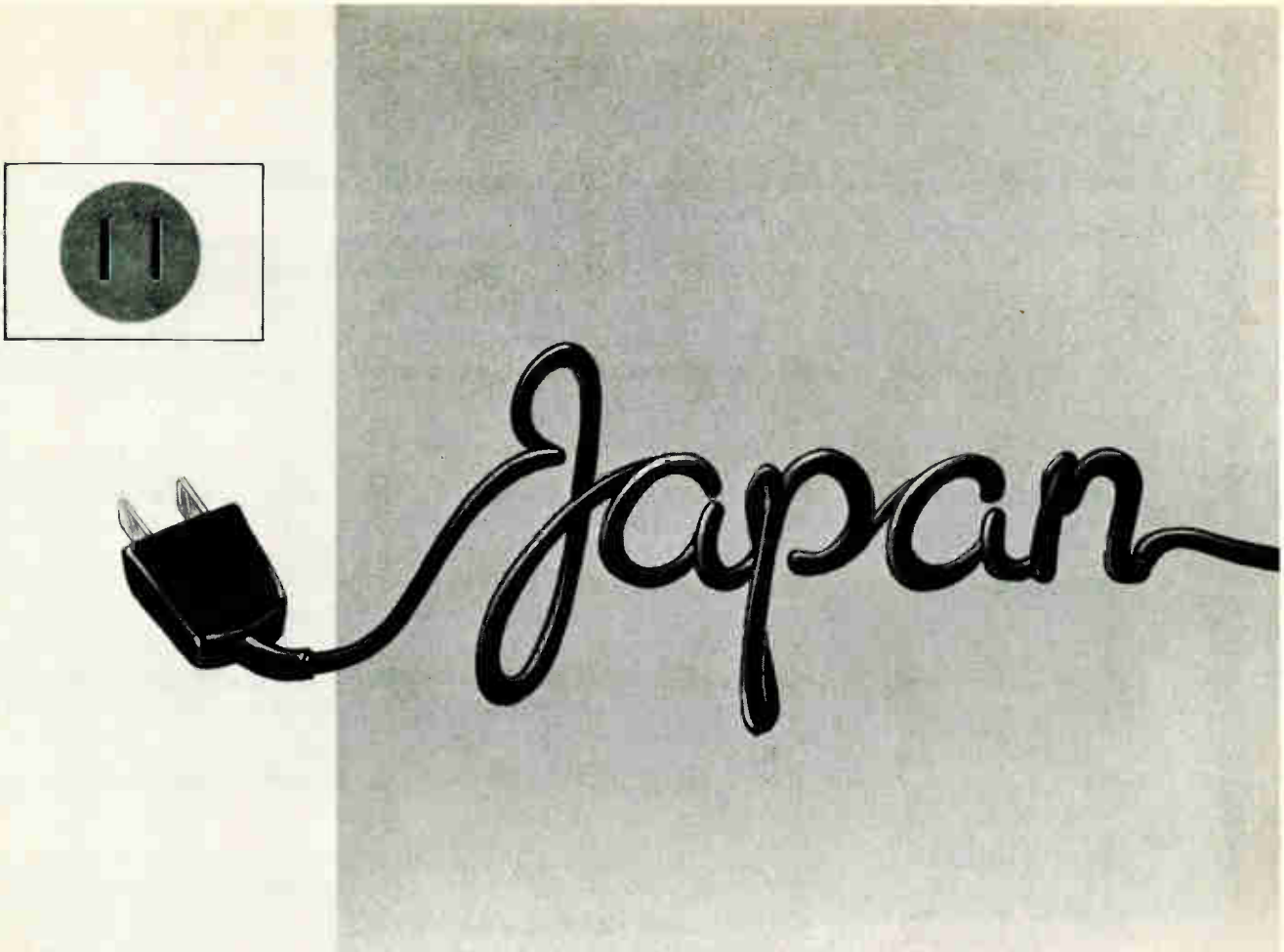
Advanced Micro Devices Inc. of Sunnyvale, Calif., and EFCIS (the Société pour l'Etude et la Fabrication de Circuits Intégrés Spéciaux) of Grenoble, France, have agreed that EFCIS will second-source the Am7910 (frequency-shift-key) modem, now in development at AMD. **The Am7910 will be a complete digital signal processor, capable of everything from data conversion to signal filtering, modulation, and detection.** It will include the essential terminal-control signals required by RS-232-C and CCITT V.24 specifications and come in a 28-pin dual in-line package requiring ± 5 V. First samples are expected late in the year.

Olivetti gets rights to 10-megabyte disk

Adding a third 5¼-in. Winchester drive to its line of products for original-equipment manufacturers, Olivetti Peripheral Equipment SpA of Ivrea, Italy, has obtained from Irwin International Inc., Ann Arbor, Mich., the exclusive European manufacturing and marketing rights to the Irwin 510 10-megabyte disk drive with its integrated tape cartridge. **Olivetti's other two 5¼-in. Winchesters are a 5- and a 17-megabyte drive.** The Irwin unit is the only 5¼-in. Winchester with a built-in tape backup.

Price changes

- **Spectronics Inc. of Richardson, Texas,** a division of Honeywell Inc., is cutting prices of its Sweet Spot fiber-optic component series by 50%. **Included in the series are the Sweet Spot light-emitting diode and three photodetectors.** The LED and each of the photodetectors are available for $4.50 apiece in quantities of 1,000, $2.50 in quantities of 50,000, and $1.50 in quantities of 100,000.
- **Nitron Inc. of Cupertino, Calif.,** has announced a price reduction of 40% on its new real-time clock, the NC8000. The microprocessor-bus–oriented product, which has a maximum count of 128 years and a maximum resolution of 15.3 μs, **is said to interface easily with any microprocessor using a multiplexed address and data bus,** such as Motorola's 6805 and 6801, and Intel Corp.'s 8080, 8048 or 8086.



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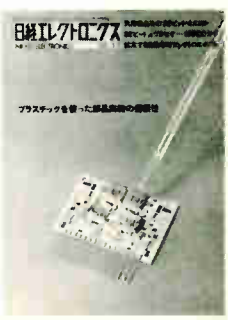

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Career outlook

Avionics engineers flying again?

■ The emphasis on military spending promised by the Reagan Administration is already giving the engineering job market a lift, according to the results of a January survey released late last month by Thomas-Mangum Co. The Los Angeles–based firm, which specializes in executive search and management consulting for high-technology clients, has found a shortage of avionics engineers is already looming.

Ever since the sharp reductions in military spending in the 1970s, when many an avionics engineer ended up selling real estate or fled the profession along other routes, this specialty has been in the doldrums. Now avionics engineers have replaced software specialists on the most-wanted list, according to the survey. William T. Mangum, president, attributes this upcurve to the anticipation of improvement programs for existing electronic systems on such aircraft as the F-15 and F-5.

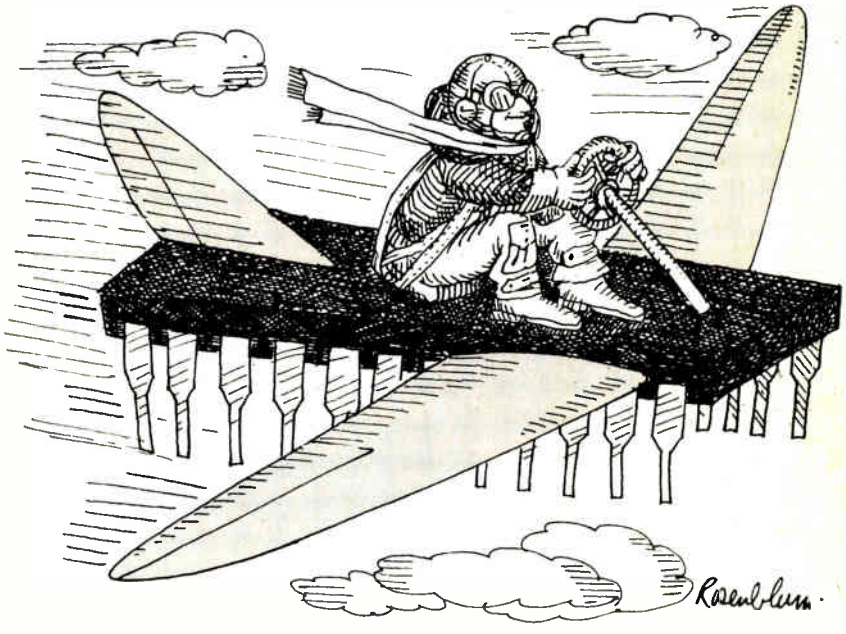
Scarce, too. Another scarce skill is expertise in computer-aided design and manufacturing. "The only way to attract these people is to offer a more interesting professional challenge—money alone won't do it," Mangum observes.

Other difficult jobs to fill are in research laboratories and all levels of data processing, where firms not in high technology are also competing for people. Overall, demand for engineers and scientists remains strong.

"I'm really amazed that with high interest rates, inflation, and recession we are still having a hard time finding people," Mangum states. More than 100 companies filled in the company's questionnaire, the second annual survey to be conducted by the firm.

There have been some changes in the demand picture. For example, 69% of the companies report having recession problems, up sharply from 39% a year ago. Some 58% report experiencing enough difficulty in hiring personnel for their production and growth goals to be adversely affected, down from 82% last year. This year 74% of the respondents said they are having difficulty in hiring executives, down slightly from 79% in 1980, but 93% still intend to hire new personnel in 1981.

Rehousing a problem. The biggest barrier to recruiting personnel from another geographic region remains housing. "This is the main reason for losing out in hiring, and not just in California," Mangum notes. In fact, assistance in paying for new mortgages has become the top inducement in recruiting. **-Larry Waller**



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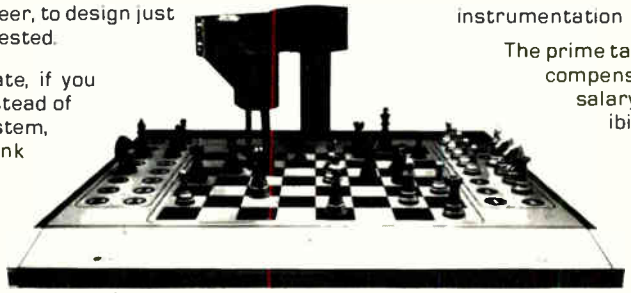

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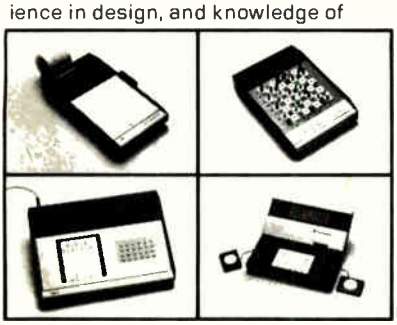

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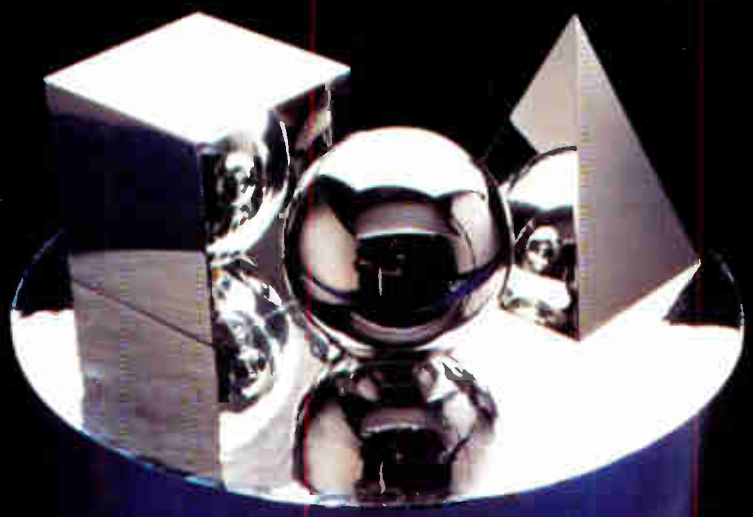

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