SEPTEMBER 11, 1980

**SMART FIFO HOOKS FAST PROCESSORS TO SLOW PERIPHERALS/131**

What gear will the new AT&T company need?/100

Pullout guide to the world's communications satellites/150

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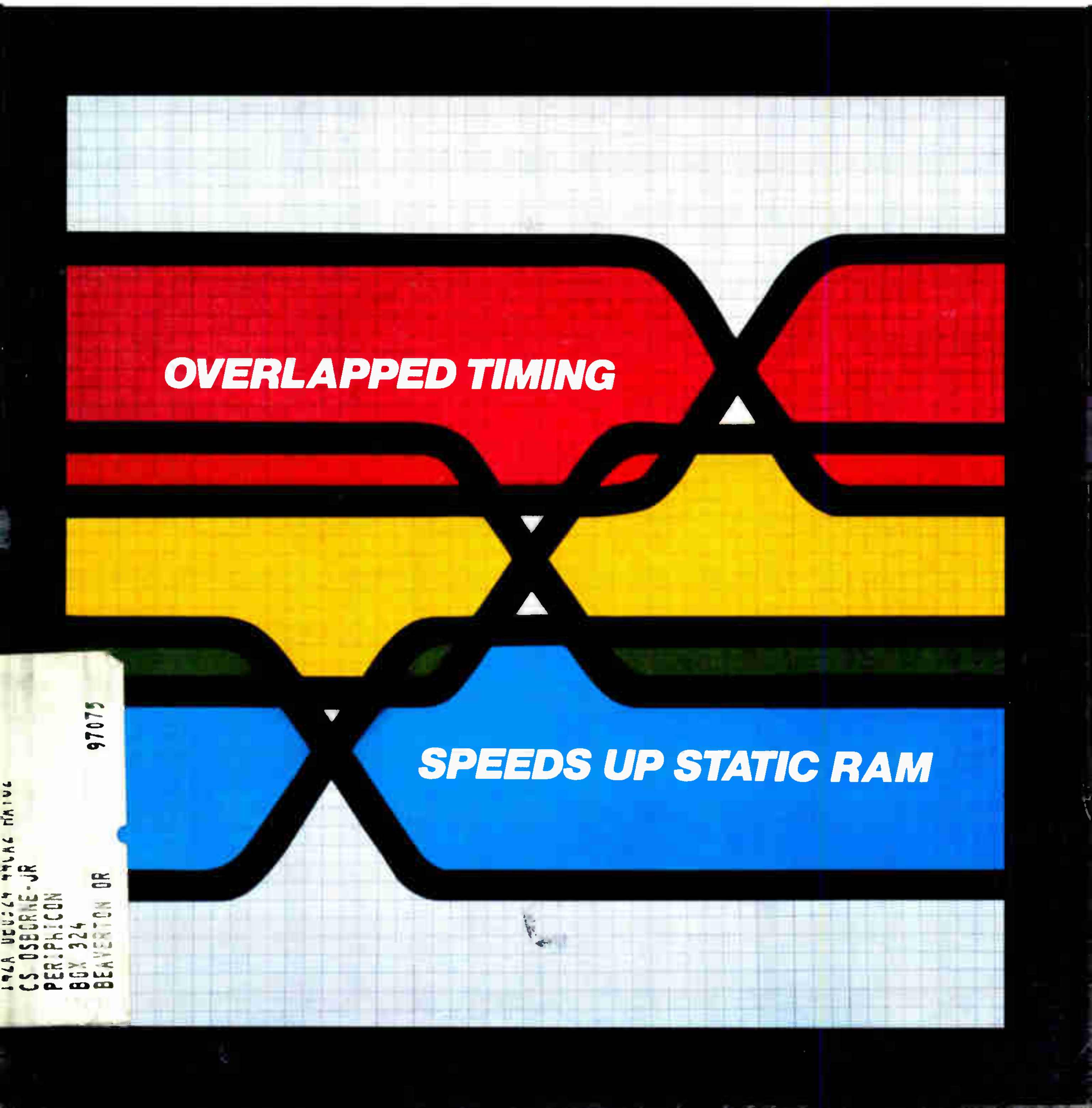
# 50 YEARS Electronics



# HOW DEPENDENT SHOULD YOU BE ON THE ATE SUPPLIER?

Automatic board test equipment can provide a powerful solution to today's testing needs. But choosing the right system can be a complex and bewildering task, because of all the non-hardware factors to be assessed.

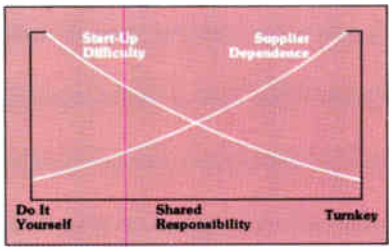
**Purchase alternatives.**
One factor is the question of system responsibility. At one end of this spectrum is a turnkey system. Here the ATE manufacturer assumes total responsibility and the user is dependent upon the supplier for hardware, software and system implementation. At the other end is the do-it-yourself system tailored to your exact application, in which case the user is almost self sufficient. Other alternatives also exist. So how can you choose the right one?

**Some helpful criteria.**
The three most important criteria are: your environment, departmental resources, and the system supplier.

Production environment is critical. How high is the PC board volume? Are the boards extremely complex? How many new products are anticipated? For example, if you have fairly simple boards and few requirements for changes, a turnkey solution may be your answer. But for highly complex boards and a stream of new products, you may wish to keep expansion and revision control in-house. What about departmental resources? Do you have the technical people to assemble and program a do-it-yourself system?

Finally, the system supplier should be evaluated. Does the company have knowledge of your business and applications engineers familiar with your needs? Will service and support personnel be available when and where you need them?

**The concept of shared responsibility.**
HP's answer is shared responsibility . . . a concept that minimizes both start-up difficulty and your dependence upon outside suppliers (see chart below).



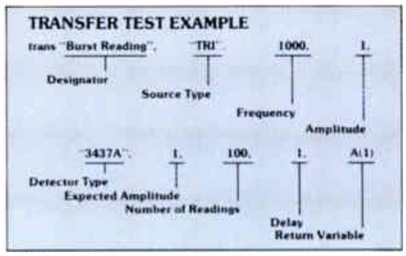

When you choose the HP 3060A Board Test System, you get a system designed to put you on the road to independence. Here's why:

First, you get two weeks of intensive training in system use and software development. Second, HP supplies the software aids that take the mystery out of programming. Non-technical people can easily program in-circuit tests by entering node numbers plus parts values and tolerances. HP's In-circuit Program Generator (IPG) does the rest, selecting appropriate test methods, determining uncertainty, generating the test program and more.

Then, your technical people can easily master BTL (Board Test Language), using commands such as the one shown, to program functional tests. Because they know the circuit best, testing becomes more thorough and more meaningful.

Third, you get reliable hardware that's ready to operate. Most systems are up and running the same day they're installed. And because the system is HP-IB compatible, you can modify and expand its capability right in your facility without a major software investment.

If you have problems, HP doesn't desert you. Our specialists are available to help. And with the self-diagnostics built into the system, you'll be up and running again quickly.




**Supplier independence.**
The net result is greater independence. With the HP 3060A, you learn to solve your own problems. That means faster response to changing needs. Direct control over expenses. And, generally, lower overall cost of ownership.

**For additional information.**
There are numerous other reasons to consider the HP 3060A ($85,000* for standard operating system). To get complete details, write: Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304. Or call your nearest regional sales office: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.

*Domestic USA price only.

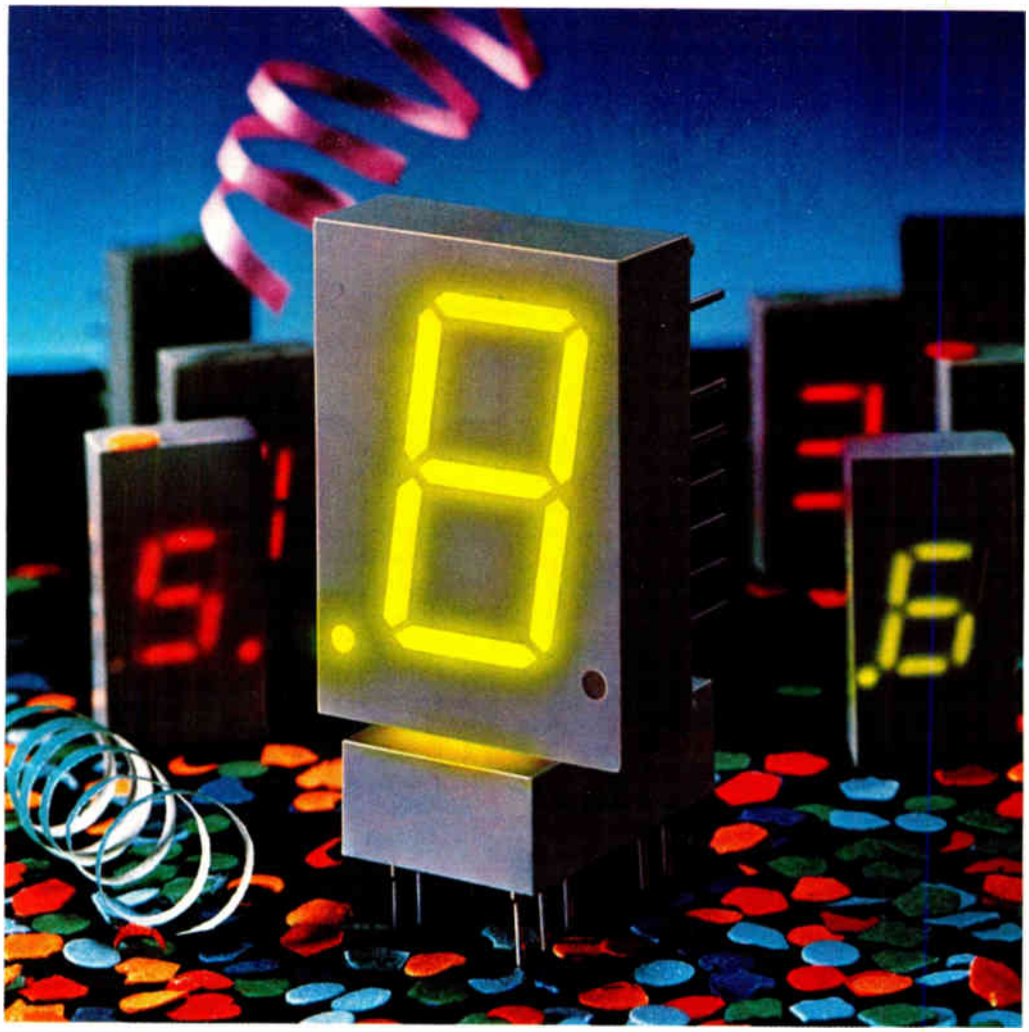
090/45

**HP Circuit Testers — The Right Decision**

HEWLETT PACKARD

Circle 900 on reader service card

# SURPRISE!



## HP's New Display is a Big Yellow Show Off.

Yellow joins High Efficiency Red in HP's popular 20mm (0.8") high displays. Both can be viewed clearly from as far away as 10 metres. They show off well too, with excellent readability in bright ambient conditions because of their gray body color and untinted segments. This is HP's family of HDSP-3900 Series of red displays and HDSP-4200 Series of yellow.

IC compatible, they're ideal for electronic instrumentation, point-of-sale terminals, TV's weighing scales, digital clocks, and other applications where you need a big, easy-to-read display. And power requirements are low since they utilize a chip made from GaAsP on a transparent GaP substrate.

Units are priced at $2.55* in quantities of 1000.

For immediate delivery, call any authorized HP components distributor. In the U.S. contact Hall-Mark, Hamilton/Avnet, Pioneer Standard, Schweber, Wilshire or the Wyle Distribution Group (Liberty/Elmar). In Canada, call Hamilton/Avnet or Zentronics, Ltd.

HEWLETT PACKARD

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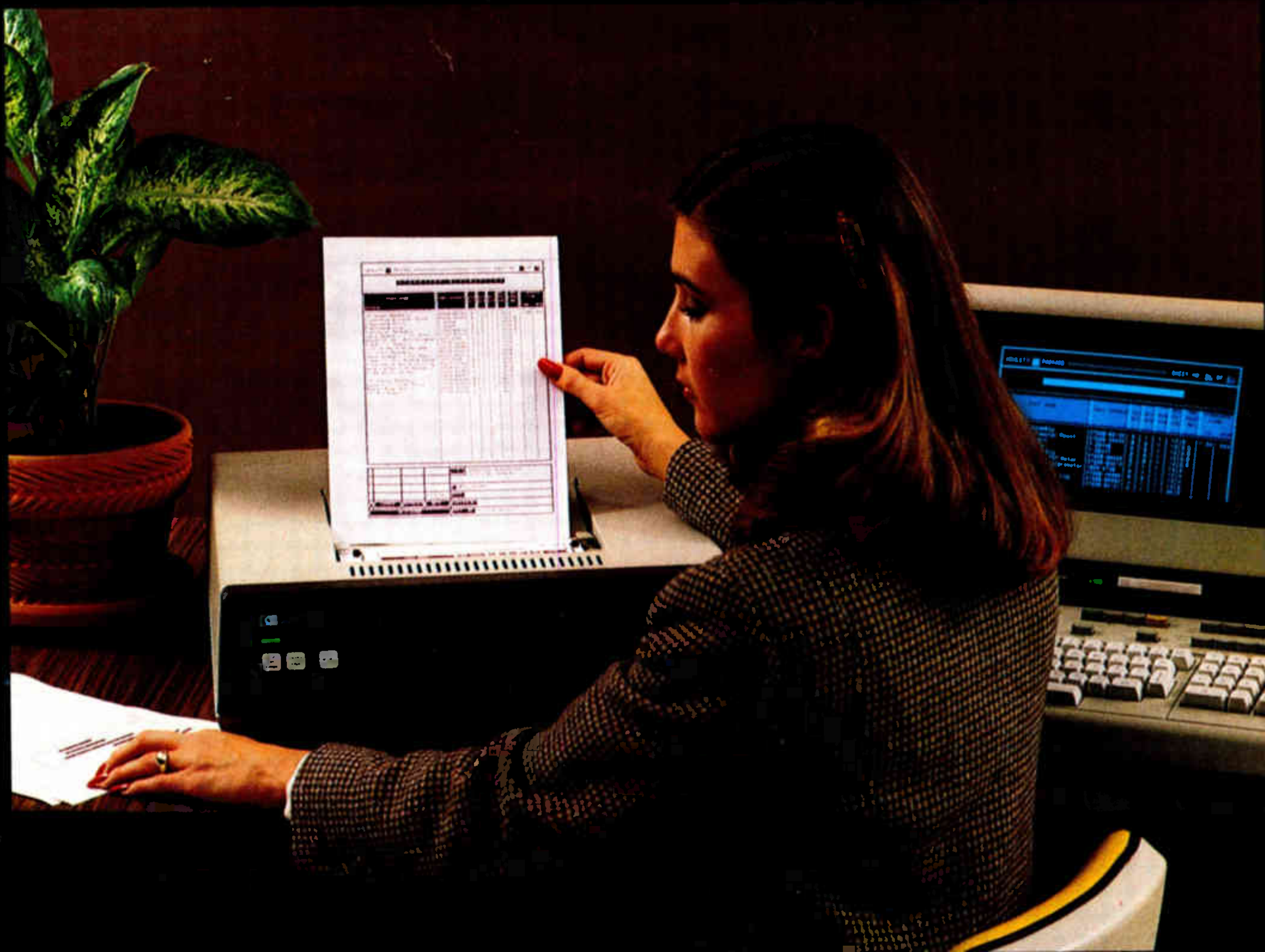
*Suggested U.S. Domestic Price Only.



# HP introduces forms and graphics to desktop printing.

HP's new 7310A Graphics Printer mixes forms, text and graphics in any arrangement you need. And it prints text up to 500 lines per minute.

On demand from your terminal, the 7310A prints out your forms, and what goes on them at the same time. Work orders, assembly information, material lists, accounting reports, employee records, and all other forms with data, are printed and then sized to your needs by an automatic paper cutter and page stacker.

Besides being fast and versatile, one of the printer's nicest qualities is just that. Printing quality. Readability can be enhanced with proportionally spaced type, reverse printing, and underlining. And programmable character height allows you to produce bold face headlines or titles in characters up to twice normal height.

In addition to supporting HP terminals and computers, four different interfaces let you adapt the 7310A to many other terminals and computers. For complete information, including OEM discounts, contact your local Hewlett-Packard sales office or write to Hewlett-Packard, Attn: Bill Fuhrer, 16399 West Bernardo Drive, San Diego, CA 92127; (714) 487-4100.

11001

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# Electronics

**The International Magazine of Electronic Technology**

**Vol. 53, No. 20 • September 11, 1980**

**117 Technical Articles**

# Electronics

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# Highlights

## Cover: Fast 16-K static RAM brings back circuit innovation, 117

New circuit techniques, rather than scaling, characterize an extremely fast 16-K-by-1-bit static random-access memory. Asynchronous bootstrap circuits, for one, help bring about a typical access time of 30 nanoseconds. What's more, the chip typically dissipates only 375 milliwatts when active. On the manufacturing side, a single level of polysilicon, 2.7-micrometer channel length, and redundant bits make it easy to build.

Cover design by Bob Strimban.

## Artificial intelligence: moving out of the university, 93

The first annual National Conference on Artificial Intelligence, held last month at Stanford University, was marked by substantial participation by industry. Included were such notables as Hewlett-Packard, Texas Instruments, and Schlumberger, all of whom are actively investigating applications in this field. In addition, small companies, many of them spinoffs from university research projects, are springing up to exploit the commercial possibilities of artificial intelligence.

## Smart buffer coordinates traffic for microprocessor systems, 131

An intelligent 128-by-8-bit first-in–first-out buffer synchronizes free-running devices that operate at different speeds. Accepting and delivering data at the same time and including programmable interfaces for various computers and input/output devices, it allows each one to work at its own speed. The buffer, designed for both 8- and 16-bit systems, works with multiplexed and nonmultiplexed address and data buses.

## Voltage converter achieves unparalleled efficiency, 141

A dc voltage converter on a single complementary-MOS chip produces negative or positive multiples of any input from 1.5 to 9 volts to within 0.1%, and it does so with a power-conversion efficiency of up to 98%—all at the expense of a large number of discrete components and integrated circuits.

## Bird population growing rapidly, 148

To help users cope with the growth of communications satellites—up by more than a third in less than two years—the guide originally published in the Oct. 12, 1978, issue has been completely updated. The fold-out wall chart contains both the new systems and the latest data on the old.

## And in the next issue . . .

Local network links just about any computers or peripherals . . . a special report on arrays . . . a low-power microcomputer system . . . controlling operating junction temperature in semiconductors.


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# Publisher's letter

**Launching itself into** the static memory field, Inmos Corp. has taken a different tack for its first offering, and this issue's cover article will tell you about the approach the British-sponsored company took for its 16-K-by-1-bit random-access memory that boasts a typical access time of 30 nanoseconds. This speed, and a low typical power dissipation of 375 milliwatts, were realized through circuit, rather than process, innovation, write codesigners Rahul Sud and Kim C. Hardee.

"This is an area that has been neglected for a long time," says Sud. "There is a widely held feeling in the industry that circuit cleverness is dead and process innovation is the only thing that will allow us to go beyond very large-scale integration."

Working with John Heightley, vice president for memory products; David R. Wooten, manager of strategic marketing and applications; and others, the designers set out to make a part that is "very manufacturable," Sud says. And so the process parameters are conservative—2.7-micrometer channel lengths and a single level of polysilicon, notably.

What are the innovations in the Colorado Springs, Colo., company's first offering? As the article that begins on page 117 makes clear, the designers worked on circuit solutions to what Sud calls "some of the classic design problems with static RAMs."

For one, to realize the low-power and high-speed potential offered by bootstrap circuits, he and Hardee developed ways to counter the input transients that can plague them. Similarly, they designed actively precharged bit lines with loads that turn on only when needed, thereby avoiding continuous dissipation.

The bit-line design also aims at overcoming word-line delay, with overlap circuitry using that time to drive the lines to the equilibrium point between the old and new data states. "We buy over 30% of the access time of the memory right there," Sud says. Also, the column-select line is driven above the power-supply voltage, with circuitry maintaining that signal indefinitely.

Sud reports that he and Hardee worked with Michael J. Griffus on computer simulation, with James R. Adams and Richard M. Basecki on process development, and with Jay C. McBride and Arthur G. Smith on the chip's layout. "The first wafer probed from the initial lot out of our brand-new pilot production line yielded fully functional dice," he says happily.

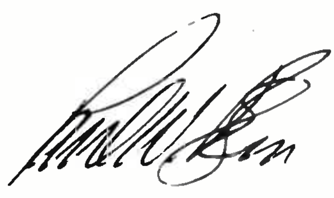
**A popular 1978 offering** was "A user's guide to communications satellites," a handy wall chart, and its originator, Satellite Systems Engineering Inc., has revised it to reflect the latest developments in this fast-moving field.

As the introduction to the chart on page 149 notes, there is better than a third more of the birds flying around the earth—and that portends a crisis, says Wilbur L. Pritchard, president of Satellite Systems. "It's like the sword of Damocles hanging over our head; there is the finite resource of the geostationary orbit."

It won't be long before there is just no more room there, he continues. "So that means a move to other orbits and higher frequencies with more power and less bandwidth.

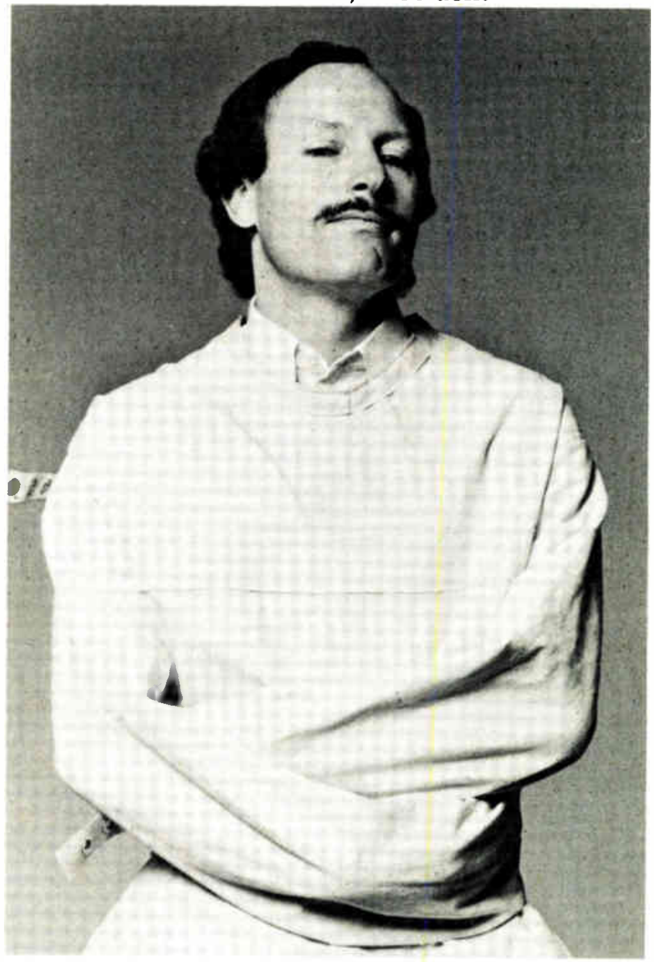
"Of course, higher power in the satellites means cheaper ground stations. On the other hand, the narrower bandwidth runs counter to the trend toward digital systems, which tend to use wider bandwidths."

Still, digital systems will flourish because they can exploit time-division multiple access, with its inherently superior capacity, a trend that undoubtedly will be reflected in our next edition. Pritchard reports that putting the chart together is a fairly easy task because his Washington, D. C., consulting firm publishes the Satellite Systems Digest, a continually updated reference tool from which our User's Guide is drawn.



# "How did we manage to be first with intelligent analog peripherals? By working like madmen."

Fred Molinari, President



We worked days and nights, weekends and vacations to develop the intelligent analog peripheral.

It was time well spent.

Because now we can offer you a complete microcomputer data acquisition system on a single Multibus™ board.

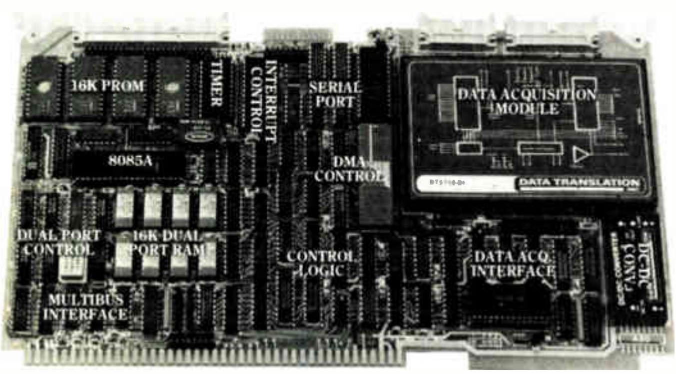
Decentralizing your computer function has finally become a practical possibility.

You see, this intelligent analog peripheral pre-processes data without involving the host CPU.

And thanks to a unique DMA controller, this peripheral also acquires analog data independently, at rates up to 125KHz.

Our new peripheral can function as an intelligent A/D slave. Or as a stand-alone microcomputer with A/D capabilities. Or as a remote system, transmitting data via a serial line.

Convenient? Our peripheral even includes a system monitor in preprogrammed ROM to communicate with the board, debug, and access A/D conversions.




**Our intelligent analog peripheral features: A dual port memory controller. A 8085 CPU. Four PROM sockets. Two programmable timers. A baud rate generator. A complete priority interrupt controller. 12 bit A/D with 125KHz throughput to memory. A 16K byte dual-ported dynamic RAM. A self-contained four-channel multi-mode DMA controller. And quite a bit more.**

In short, we have brought high-speed capability down to low-end computers. And, we might add, we are the first to do so.

Working like madmen has its advantages. We hope you'll let us work like crazy for you.

We can be reached at 4 Strathmore Road, Natick, MA 01760. Or by phone at (617) 655-5300. Telex: 948474. In Europe: Data Translation Ltd., Reading, Berkshire/England. Phone (0734) 669-335; Telex: 847482.

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Circle 7 on reader service card

# Readers' comments

## The software approach

**To the Editor:** Though "Development system networks: the last link in automated manufacturing" [July 3, p. 134] was comprehensive, it should not dismiss software development systems. Our customers estimate that 80% of a project's development is performed before hardware integration. This is as true when using a BSO universal development system as when using a system from a semiconductor manufacturer.

Since BSO also specializes in microprocessor simulators, I must point out that though the simulator is a sophisticated and complex tool, it does not require excessively large computers if properly designed. We routinely sell simulators for DEC's PDP-11/23. With demand, we could even put a simulator on the PDP-11/03.

Also, I disagree that simulators rely on ideal operating conditions. Ours let a user set up interrupt and data-input/output simulation to a disk file or a peripheral device. The user can, in advance, set up any conceivable operating condition to test the program more exhaustively and more repeatably. The software will not be affected by environmental factors when running in the simulator, but that's exactly the benefit. First debug the software, then check out the hardware.

Further, BSO has 16-bit simulators and is developing very large-scale integrated simulators and multiprocessor system-debugging capability right now, unlike most emulator manufacturers.

BSO is using powerful and stabilized 16-bit minicomputers from DEC or Data General with operating systems and utilities proven over 15 years of user testing. Multimicroprocessor system testing will demand an independent development system manufacturer to ensure support over the different manufacturers. And a networked approach will not give the debugging and control capabilities a powerful, centralized CPU can provide.

Simon Wieczner
Boston Systems Office
Waltham, Mass.

# Interested in higher performance software?

The Mark Williams Company announces **COHERENT**,™ a state of the art, third generation operating system. The design of **COHERENT** begins with the basic technology of the highly-acclaimed Western Electric UNIX operating system. From this starting point, it goes on to include further substantial software innovation. The primary goal of **COHERENT** is to provide a friendly environment for program development. The intent is to provide the user with a wide range of software building blocks from which he can select programs and utilities to solve his problems in the most straightforward manner.

**COHERENT** and all of its associated software are written totally in the high-level programming language **C**. Using **C** as the primary implementation language yields a high degree of reliability, portability, and ease of modification with no noticeable performance penalty.

### FEATURES

**COHERENT** provides **C** language source compatibility with programs written to run under Seventh Edition UNIX, enabling the large base of existing UNIX software (from numerous sources) to be available to the **COHERENT** user. The system design is based on a number of fundamental concepts. Central to this design is the unified structure of i/o with respect to ordinary files, external devices, and interprocess communication (pipes). At the same time, a great deal of attention has been paid to system performance so that the machine's resources are used in the most efficient way. The major features of **COHERENT** include:

- multiuser and multi-tasking facilities,
- running processes in foreground and background,
- compatible mechanisms for file, device, and interprocess i/o facilities,
- the shell command interpreter—modifiable for particular applications,
- distributed file system with tree-structured, hierarchical design,
- pipes and multiplexed channels for interprocess communication,
- asynchronous software interrupts,
- generalized segmentation (shared data, writeable instruction spaces),
- ability to lock processes in memory for real-time applications,
- fast swapping with swap storage cache,
- minimal interrupt lockout time for real-time applications,
- reliable power failure recovery facilities,
- fast disc accesses through disc buffer cache,
- loadable device drivers,
- process timing, profiling and debugging trace features.

### SOFTWARE TOOLS

In addition to the standard commands for manipulating processes, files, and the like, in its initial release **COHERENT** will include the following major software components: **SHELL**, the command interpreter; **STDIO**, a portable, standard i/o library plus run-time support routines; **AS**, an assembler for the host machine; **CROSS**, a number of cross-assemblers for other machines with compatible object format with **'AS'** above; **DB**, a symbolic debugger for **C**, Pascal, Fortran, and assembler; **ED**, a context-oriented text editor with regular expression patterns; **SED**, a stream editor (used in filters) fashioned after **'ED'**; **GREP**, a pattern matching filter; **AWK**, a pattern scanning and processing language; **LEX**, a lexical analyzer generator; **YACC**, an advanced parser generator language; **NROFF**, an Nroff-compatible text formatter; **LEARN**, computer-aided instruction about computers; **DC**, a desk calculator; **QUOTA**, a package of accounting programs to control filespace and processor use; and **MAIL**, an electronic personal message system.

Of course, **COHERENT** will have an ever-expanding number of programming and language tools and basic commands in future releases.

### LANGUAGE SUPPORT

The realm of language support is one of the major strengths of **COHERENT**. The following language processors will be supported initially:

- **C** — a portable compiler for the language **C**, including stricter type enforcement in the manner of **LINT**.
- **FORTRAN** — portable compiler supporting the full ANS Fortran 77 standard.
- **PASCAL** — portable implementation of the complete ISO standard Pascal.
- **XYBASIC™** — a state of the art Basic compiler with the interactive features of an interpreter.

The unified design philosophy underlying the implementation of these languages has contributed significantly to the ease of their portability. In particular, the existence of a generalized code generator is such that with a minimal effort (about one man-month) all of the above language processors can be made to run on a new machine. The net result is that the compilers running under **COHERENT** produce extremely tight code very closely rivaling that produced by an *experienced* assembler programmer. Finally, the unified coder and conformable calling sequences permit the intermixture of these languages in a single program.

### THE OPERATING SYSTEM

In part because of the language portability discussed above, and in part because of a substantial effort in achieving a greater degree of machine-independence in the design and implementation of the **COHERENT** operating system, only a small effort need be invested to port the whole system to a new machine. Because of this, an investment in **COHERENT** software is not tied to a single processor. Applications can move with the entire system to a new processor with about two man months of effort.

The initial version of **COHERENT** is available for the Digital Equipment Corporation PDP-11 computers with memory-mapping, such as the PDP 11/34. Machines which will be supported in the coming months are the Intel 8086, Zilog Z8000, and Motorola 68000. Machines for which ports are being considered are the DEC VAX 11/780 and the IBM 370, among others.

Because **COHERENT** has been developed independently, the pricing is exceptionally attractive. Of course **COHERENT** is completely supported by its developer. To get more information about **COHERENT** contact us today.

**Mark Williams Company**

1430 W. Wrightwood Ave., Chicago, IL 60614
TEL: 312-472-6659 TWX: 910-221-1182

You're designing an intelligent CRT terminal and you're looking for the best 16-bit CPU for your application.

Congratulations. Your search is over.

## "The AmZ8000 is better at handling strings of characters or data words."

The AmZ8000 has special block I/O instructions that allow you to move from 1 byte to 64K bytes of data in a single instruction. Into or out of memory. Ascending or descending addresses.

With our standard 4MHz CPUs, you can move a data item every 2.5 μsec. And you can interrupt the instruction to take care of other business.

## "The AmZ8000 has a better development system."

Our System 8/8 was designed especially for the AmZ8000.

It comes with 64K bytes of RAM, dual double-density floppy disks, an optional cartridge disk and piles of software. It's Multibus* compatible. And it's even got an optional in-circuit emulator that runs in real time: 4MHz. No wait states.

Rick McCarthy
Manager,
Field Applications,
Engineering

*Only the AmZ8000 offers string instructions for exceptionally efficient I/O.*

# "The AmZ8000 is better for intelligent CRT terminals."

## News update

■ On tap at TRW Inc.'s Microelectronics Center are fully operational bipolar chips with minimum line widths of 1 micrometer. Researchers at the Redondo Beach, Calif., facility have spent the last year or so putting experimental test chips through their paces, with encouraging results.

"We now have sufficient characterization data and processing ability to manufacture full-size chips," says Barry Dunbridge, manager of the center. The test chips [*Electronics*, Aug. 2, 1979, p. 52] held some 10,000 devices and were the first reported bipolar very large-scale integrated circuits with 1-μm minimum dimensions.

**Parts.** The first two products, containing about 20,000 devices, "are very ambitious in their complexity and will provide a new level of high performance for digital signal-processing functions," says Dunbridge. They have two immediate outlets: to support TRW's work on the Department of Defense's very high-speed integrated circuits (VHSIC) program and to appear in applications built by the neighboring LSI Products division.

Both chips will be completed within several months, Dunbridge says, in plenty of time to support the next VHSIC round, a follow-on proposal submission scheduled for December. For this, the chips provide basic building blocks for signal processing: a multibit, multistage convolver and an 8-bit analog-to-digital converter whose speed of 75 million samples per second bids to break the sound barrier for this type of job.

**Better.** The TRW manager reports that the new chips actually exceed requirements of the first phase of VHSIC. "They have a gate–clock-frequency product better than the specified $5 \times 10^{11}$ gates-hertz called out by the DOD," he says.

Besides putting them into the early VHSIC brassboard subsystems, TRW expects the chips to become the basis for a whole new generation of products whose speed is ideally suited for such other defense systems as electronic warfare, radar, and missile guidance. *-Larry Waller*

## For BNR's Magelby, Canadian decision means challenge

**New field.** Magelby sees new interconnect market opening in Canada for BNR.

The past decade has been one of growth for interconnection companies in the U. S.—growth triggered by the Supreme Court's 1969 Carterfone decision permitting non-Bell attachments to phone lines. It also created opportunities to sell private branch exchanges (PBX) into the market for firms such as Canada's Northern Telecom Ltd. Now Canada has opened up its own interconnection market and for Kay B. Magelby, that means a challenge ahead.

Magelby is the newly appointed president of BNR Inc. of Mountain View, Calif., a research arm of Northern Telecom and Bell Canada. "That [Canadian decision] means that BNR must develop interconnect systems," he says.

Keeping up with the explosion in telephone interconnection and phone-oriented office systems in the 1980s may be an ambitious enterprise, but it is consistent with Magelby's nature. His projects have included putting Hewlett-Packard Co. into the computer business, developing high-speed communications terminals for a fledgling Sycor Inc., steering Cushman Electronics into the digital microwave radio field, and, now, guiding BNR's office-automation efforts.

Though it is true that no single person can claim to have gotten HP into computers, Magelby is generally credited by his former colleagues there as the one most responsible. While working at HP Laboratories in 1963–64, Magelby interfaced instruments with a computer, which lead to the development of an instrument-oriented computer. Since then, Magelby has concentrated his efforts in the communications field.

In addition to his June promotion to president of BNR, late last month Magelby was also given responsibility for the former Sycor laboratories in Ann Arbor, Mich., and the former Data 100 laboratories in Minnetonka, Minn.

Looking toward the office of the future, Magelby sees introduction soon of such items as voice-data switching PBXs, modem pools, and keyboardless terminals. "Local networking, including voice/data switching, will become an important part of the office, and we think it should be done in a way that avoids the duplication of a building's wiring system," Magelby asserts.

## Moore of Cetec recalls 'wild and woolly' days

Involved in California's electronics industries since World War II, Hugh P. Moore, chairman of El Monte–based Cetec Corp., likes to reminisce about the early days of those industries' dazzling growth out West. "Wild and woolly, but in a gentlemanly kind of way," is the way he describes them. And now that Moore has turned over his chief executive's job at Cetec to president Robert A. Nelson, he will have more time to recall the good old days.

Moore, who will still serve as an advisor to the company while retaining 4.3% of its common stock, says that whether the civilized nature of the business, which demands a higher educational level than most others, is a cause or effect of such growth is not the point.

What is most important is that "it attracts a high type of person, and when you surround yourself with intelligent people there's a better

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Circle 15 on reader service card

## People

**Looking ahead.** Moore recalls old days fondly, but looks forward to opportunities.

chance of success," he says.

Moore, who founded Cetec (then Computer Equipment Corp.) in the early 1950s, himself tried to tap these qualities in his company. "We wanted it to be small enough so an entrepreneur could get personal satisfaction, but big enough to be stable," he says.

With $65 million in sales last year, the diversified firm (it handles component distribution and broadcast equipment, among others) hits this balance pretty squarely, Moore feels. He is proud of keeping many executives around for the long haul.

Well-known in the region because he toiled mightily in early Wema (now the American Electronics Association) and Wescon affairs, Moore is proud of his connection to one of the most glamorous electronic products of the 1940s. "I was production manager at Bendix Corp.'s North Hollywood plant that made 'Gibson Girls.'" (The Gibson Girl was a hand-cranked radio transmitter that downed pilots used to signal for help.)

The low-keyed executive enjoys looking back, but he would rather talk about the future and "believes opportunities are rife." The fact is underlined lately by eagerness to invest in high-technology companies, in contrast to most of the 1970s. "There has never been as much venture capital available as there is today, and one reason is the well-publicized big winners." □

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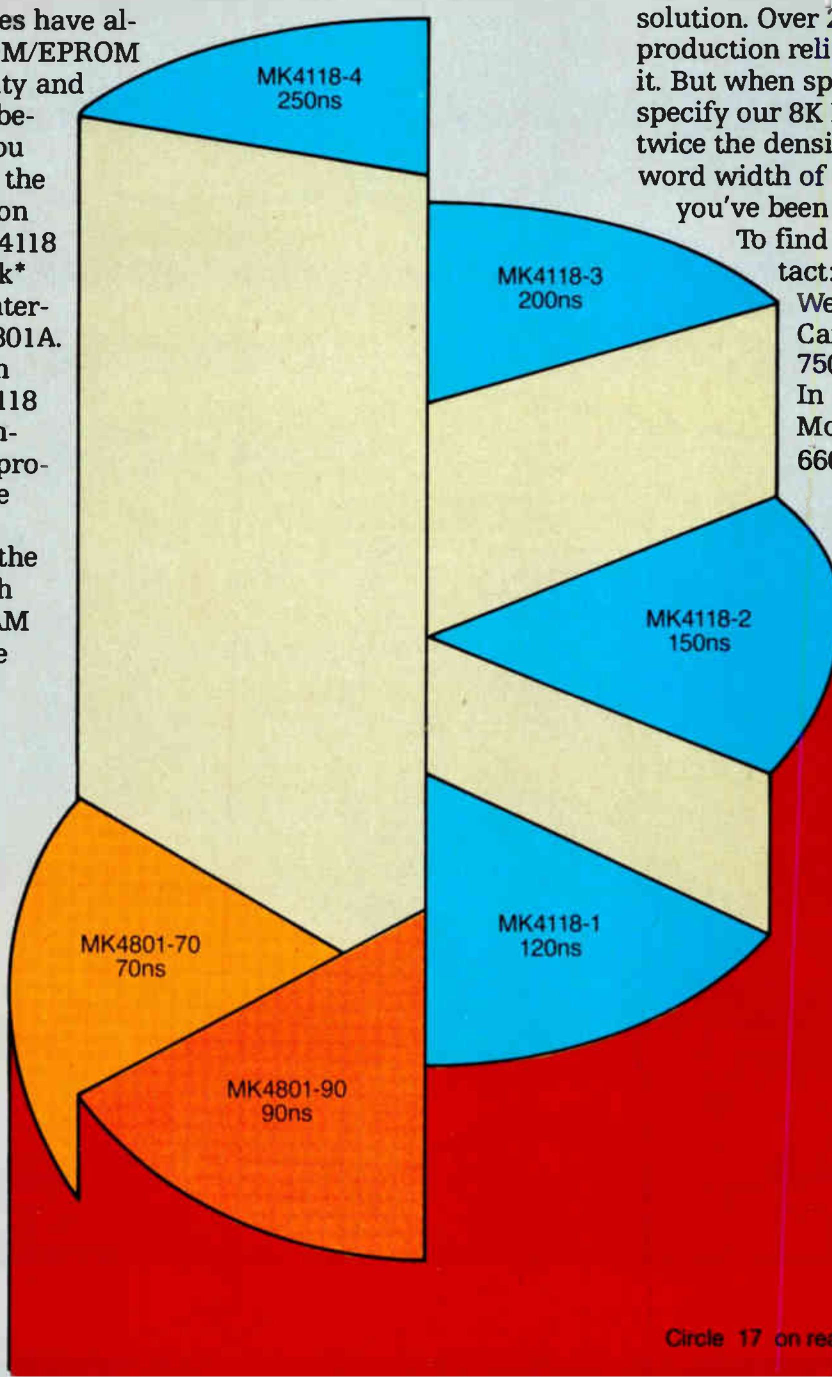
To find out more, contact: Mostek, 1215 West Crosby Road, Carrollton, Texas 75006 (214) 323-6000. In Europe, contact Mostek Brussels 660.69.24.



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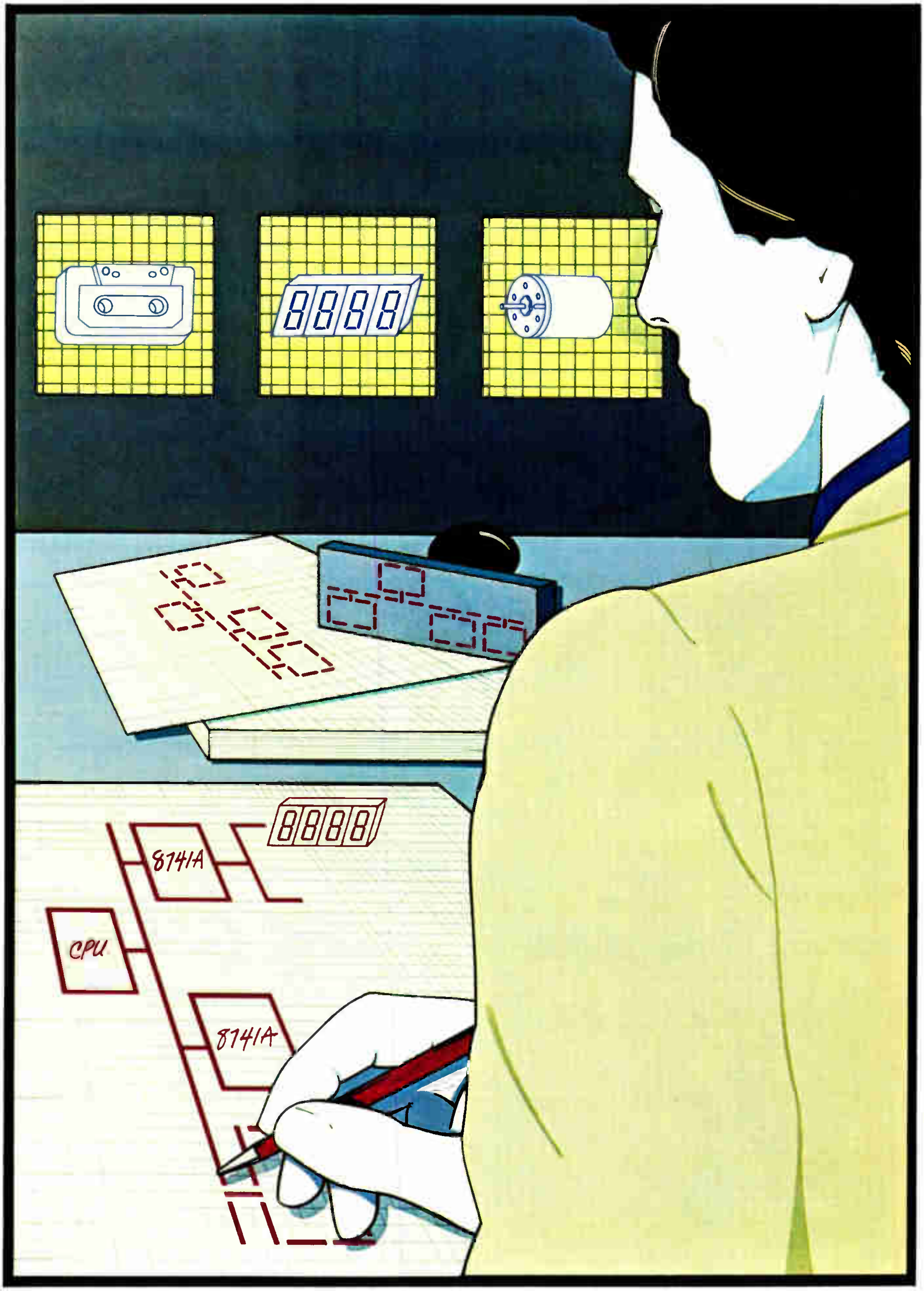
8888
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# Consider the Options

## Choose Intel's 8741A: the only peripheral controller with on-chip EPROM memory and unparalleled development support.

For almost any application where a system peripheral device interfaces to a microcomputer, Intel delivers the flexible design solution: our 8741A. It's the only UPI™ controller in the industry to give you EPROM memory *and* vital support that minimizes design and debug time. It's the proven peripheral controller available now ... in your choice of ROM and EPROM versions.

**Easy-to-instruct slave processor puts you in control.**

If you demand more flexiblity from your controller, our 8741A delivers. The 8741A assures that everything from keyboard control to complex process control tasks within your system design can now be efficiently developed as separate projects... simplifying your design and making your project more manageable.

Because Intel's 8741A controller is a true slave processor, it acts under control of the host processor. And it never monopolizes the system bus. By executing macro commands from the host, our UPI controller executes from on-chip program memory... operating in parallel with the host CPU and freeing the host CPU to do its job.

More than just an intelligent controller, our 8741A contains an 8-bit CPU, 1K byte program memory, 64 byte data memory, clock, timer/counter plus I/O ports. But the performance features of Intel's 8741A go way beyond that.

**EPROM programmable memory helps stamp out high design costs.**

In terms of both redesign and testing, Intel's 8741A with on-chip memory offers freedom and flexibility to incorporate new features into the controller. No cost sacrifices or wasted time. Change your software as many times as necessary during development, or when new features are added to the product.

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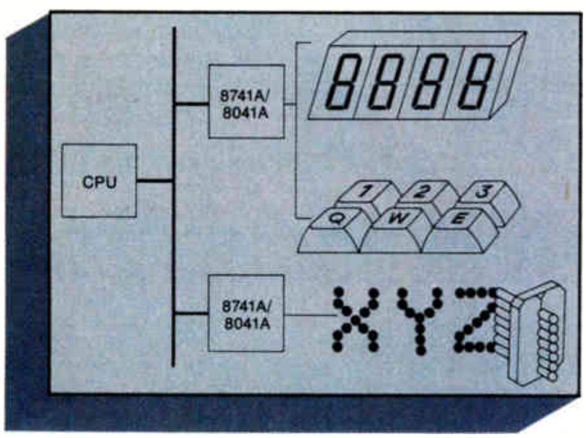
The result? Our 8741A, a controller for peripheral devices that have no other "off-the-shelf" solution.




**No other development support can serve you better.**

Intel doesn't just deliver a powerful controller, we also give you powerful debug tools. With our ICE-41A™ in-circuit-emulator, Multi-ICE™ software package and Intellec® development system, you can locate design flaws and software bugs in even the most complex multiprocessor designs.

Consider Intel's ICE-41A emulator and Multi-ICE software as your direct diagnostic connection. With Intel ICE™ modules, you can debug the peripheral controller and an entire system... all in real time. You can also rely on Intel to deliver Multi-ICE software. This unique tool lets you have two ICE modules running in parallel, plus macro and compound command extensions to the ICE-41A software that reduce testing time, errors and inconsistencies.

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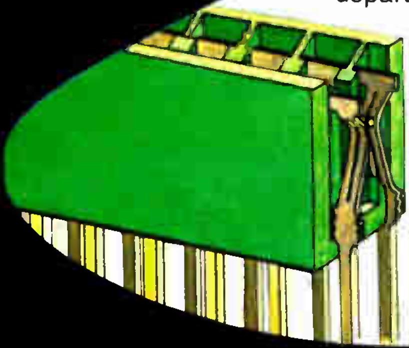

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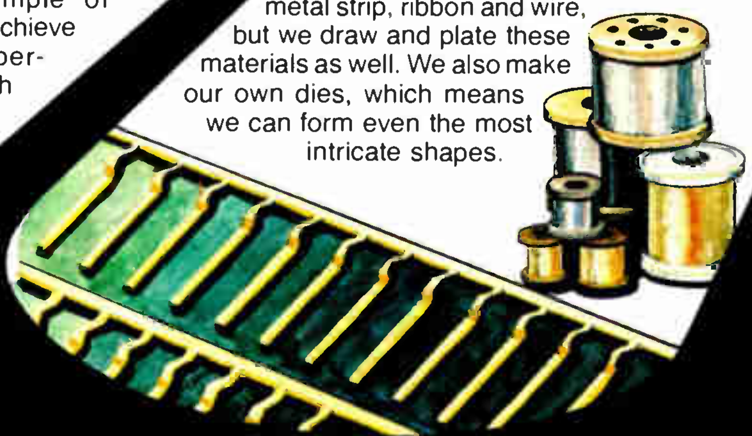

Complete in-house capability is GTE's greatest strength. This total control assures the highest degree of quality and performance while reducing connector applied costs. And since we control every aspect of the entire connector assembly, we're able to perfect it from all angles. That's why we're billed as "The Connector Perfector." For a better understanding of how this benefits you, send for our new brochure to GTE Products Corporation, P.O. Box 29, Titusville, PA 16354.

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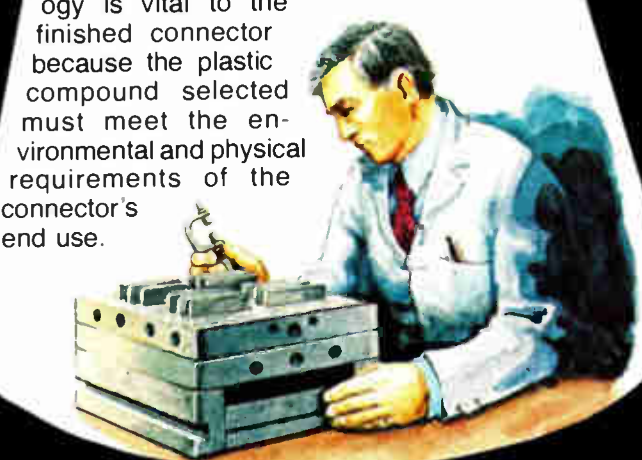

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# Announcing the HP 1000
# Separate I/O processors let the

Our new HP 1000 L-Series is designed to give you outstanding processing performance—even in the most demanding applications.

The reason is our innovative distributed intelligence architecture. Each I/O interface has its own processor—made with our exclusive SOS LSI process—and its own direct memory channel. Which means each interface can control and monitor data transfers—without interrupting the central processor.

So the CPU can concentrate on its main job of computation.

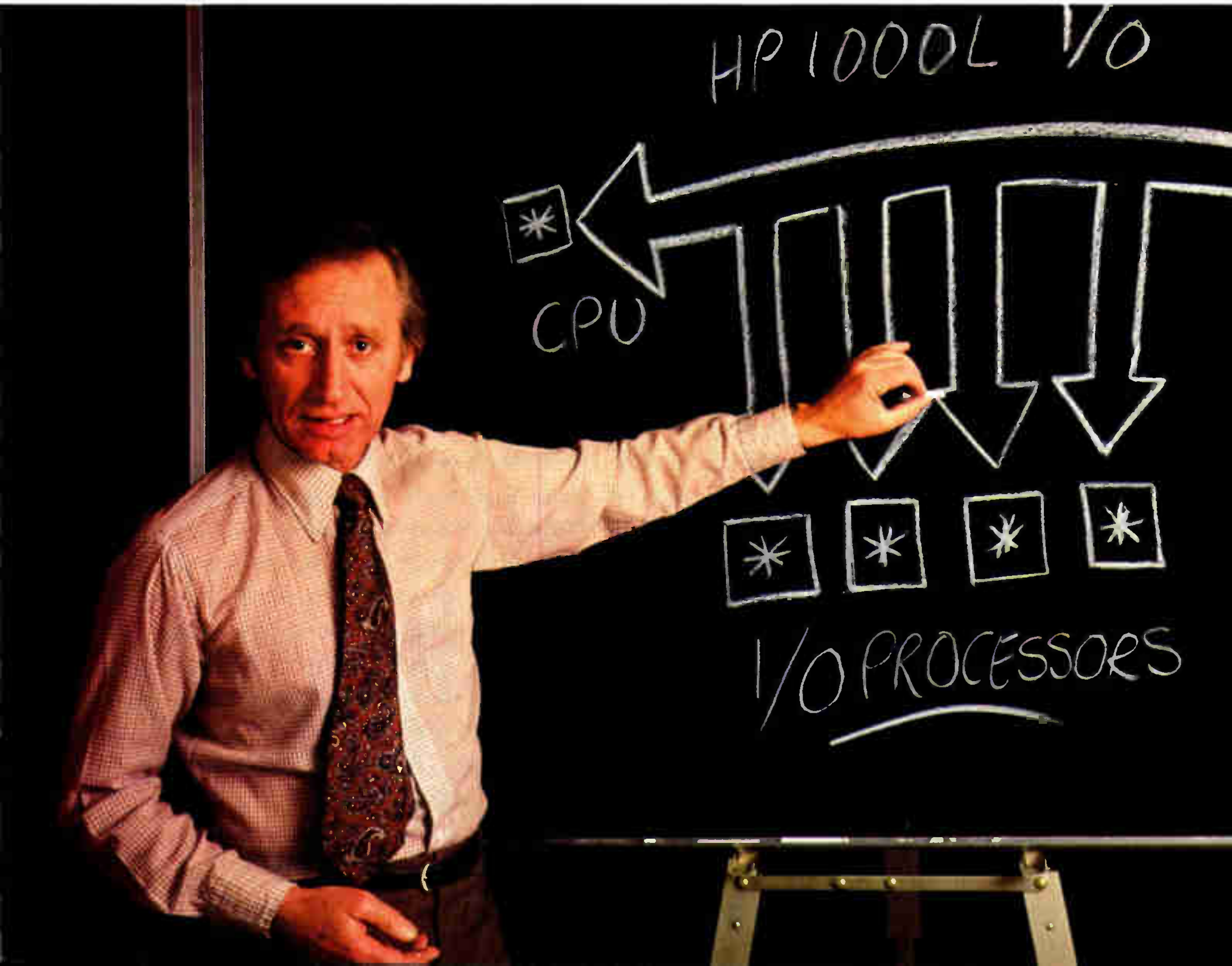
And you get faster response, higher throughput and superior system performance.

But what's really surprising about the L-Series is that you get all this performance at prices that start as low as $1968 for our starter set.† Or $15,510 for a complete disc-based system.††

## Nobody makes processors like we do.

The key to the HP-1000 L-Series' impressive new architecture is our own Silicon-On-Sapphire technology. SOS lets us make CPU and I/O chips with extremely high circuit density, low power consumption, high processing speeds and high reliability—at a very low cost.

It's this combination of high performance and low cost that make the L-Series appropriate for the whole range of OEM and industrial appli-



# L-Series Computer.
# CPU concentrate on computation.

cations — including data management, process control and instrumentation.

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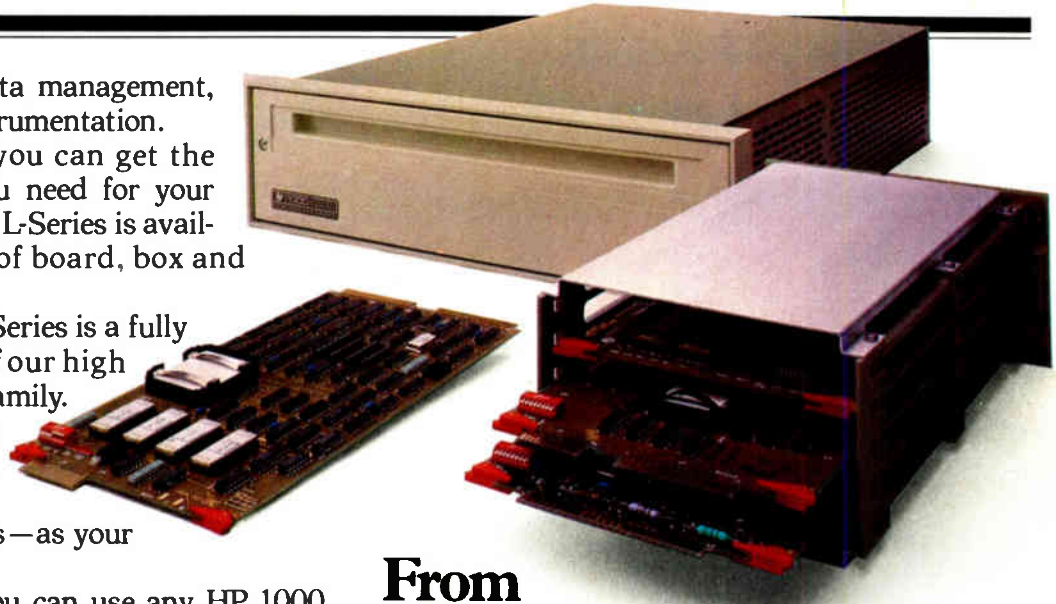

The HP 1000 L-Series is a fully compatible member of our high performance HP 1000 family. Which means you can move up to a larger computer—all the way to our powerful F-Series—as your application grows.

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Like all HP computers, the HP 1000 L-Series is designed to give you outstanding reliability. Reliability that's significantly enhanced by our SOS technology — processor boards have fewer active parts, so fewer things can go wrong. In addition, the L-Series has its own self-test programs and diagnostics.

And, of course, the L-Series is backed by our full range of support and documentation services—including our worldwide service network.

For more information or a hands-on demonstration of our high performance, low cost L-Series, contact your nearest HP sales office listed in the White Pages or write to: Roger Ueltzen, Dept. 673, 11000 Wolfe Road, Cupertino, CA 95014.

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## The NSA has no lock on computer coding

Scientists and the military establishment in peacetime are, more often than not, contestants on opposing teams in a tug of war. After all, the military is paid to prepare for and win battles; it believes it can do this best if its weapons are kept secret from any prospective adversaries.

The scientist, on the other hand, benefits from free exchange of information. Cross-fertilization of ideas is the most efficient and fastest way to solve scientific problems and apply those solutions to technology. Scientists like to think that they function irrespective of borders or other political hindrances.

That's the background for the contretemps involving the National Security Agency (the military) on one side and the National Science Foundation and those doing research on advanced computer coding on the other. The NSA has for some time been monitoring all cryptography-related research proposals submitted to the NSF. Now, in what is viewed by some as an attempt to sweep the whole field of computer cryptography under its cloak of secrecy, the military agency seems to be moving towards taking over and funding any such research that in its judgment may turn out to be crucial to national security. And in such cases, it will withhold permission to publish—anathema to the academic community.

The tight-lipped folks at the NSA make their opposite numbers at the Central Intelligence Agency look like village gossips; it is no surprise that they would attempt to take over a field such as computer cryptography. But where does that leave the banks, insurance companies, and all the other commercial enterprises in this country that need advanced coding to keep their computers safe from penetration by outsiders? It is difficult to see how the records of, say, the Prudential Insurance Co. involve U. S. security. However, it is not difficult to see what could happen to such records with the NSA jealously hoarding the potential cryptographic safeguards for them. So-called computer crime grows as the applications of computers proliferate. For any agency, particularly one as routinely secretive as the NSA, to control research into computer cryptography would seem to be contrary to the best interests of the people charged with performing that research.

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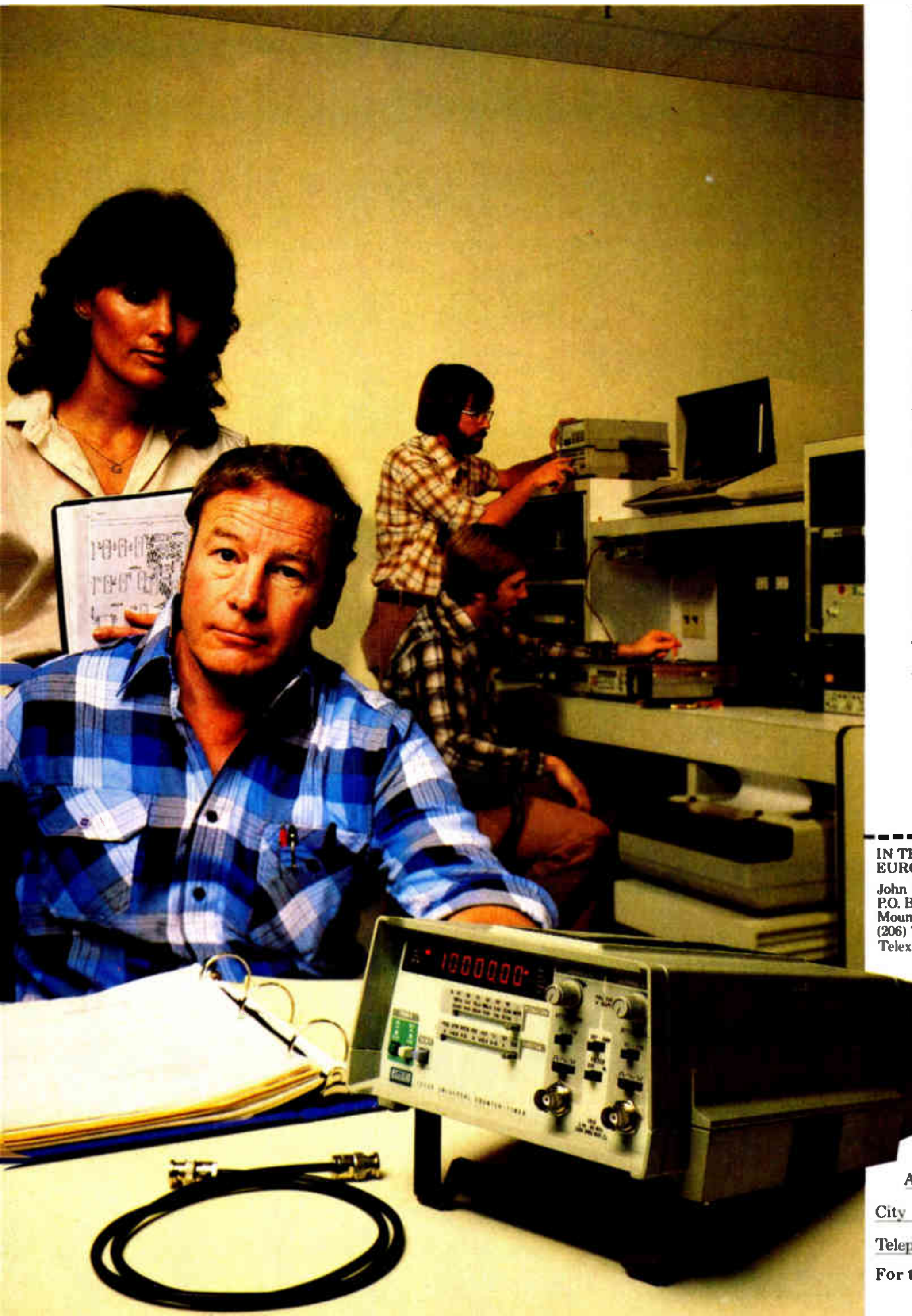

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# Meetings

**Convergence 80—30th International Congress on Transportation Electronics and Vehicular Technology Society Conference,** IEEE and Society of Automotive Engineers, Hyatt Regency Hotel, Dearborn, Mich., Sept. 15–17.

**Essderc 80—1980 European Solid State Device Research Conference,** Institute of Physics (47 Belgrave Sq., London SW1X 80X, England), University of York, York, England, Sept. 15–18.

**Sixth European Conference on Optical Communication,** Institution of Electrical Engineers (1 Savoy Pl., London WC2R 0BL, England), University of York, York, England, Sept. 15–19.

**Euromicro 80,** Institution of Electrical Engineers (L. R. Thompson, Hawker Siddeley Dynamics, Manor Road, Hatfield, Herts. AL10 9LP, England), Imperial College, London, Sept. 16–18.

**FOC 80—Fiber Optics and Communications,** Information Gatekeepers Inc. (167 Corey Road, Suite 111, Brookline, Mass. 02146), Hyatt Regency Hotel, San Francisco, Calif., Sept. 16–18.

**Wescon/80,** IEEE, Anaheim Convention Center and Disneyland Hotel, Anaheim, Calif., Sept. 16–18.

**Eusipco—European Signal Processing Conference,** IEEE *et al.*, Swiss Federal Institute of Technology, Lausanne, Switzerland, Sept. 16–19.

**ACM Symposium on Small Systems,** Association for Computing Machinery (Liza Loop, 3781 Starrking Circle, Palo Alto, Calif. 94306), Hyatt Rickey's, Palo Alto, Sept. 17–19.

**30th Sicob—Salon International de l'Informatique, de la Communication, et de l'Organisation de Bureau** (6 Pl. de Valois, 75001 Paris, France), Init—Paris La Défense, Sept. 17–26.

**30th Annual Broadcast Symposium,** IEEE, Washington Hotel, Washington, D. C., Sept. 18–19.

**Eighth IBC—International Broadcasting Convention,** Electronic Engineering Association *et al.* (1 Savoy Pl., London WC2R 0BL, England), Metropole Conference Center, Brighton, England, Sept. 20–24.

**Sixth European Solid State Circuits Conference,** Eurel *et al.* (G. Grunberg, Thomson-CSF, B.P.5., 92403 Courbevoie, France), University of Grenoble, Grenoble, France, Sept. 22–25.

**Semicon/East 80,** Semiconductor Equipment and Materials Institute (625 Ellis St., Suite 212, Mountain View, Calif. 94043), John B. Hynes Auditorium, Boston, Sept. 23–25.

**1980 European Conference on Optical Systems and Applications,** IEEE *et al.* (D. J. Kroon, Philips Research Labs, 5664 An Geldrop, The Netherlands), Jaarbeurs, Utrecht, The Netherlands, Sept. 23–25.

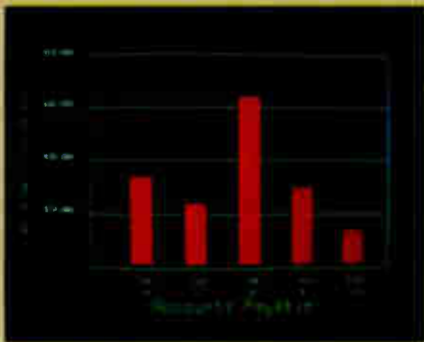
**Compcon 80 Fall,** IEEE Computer Society, Capital Hilton Hotel, Washington, D. C., Sept. 23–25.

**1980 International Conference—Security Through Science and Engineering,** West Berlin Technical University *et al.* (Sue McWain, Conference Coordinator, College of Engineering, University of Kentucky, Lexington, Ky. 40506), West Berlin Technical University, West Berlin, West Germany, Sept. 23–26.

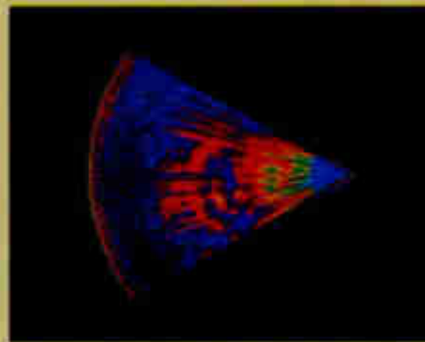
**Society for Computer Medicine 10th Annual Conference,** SCM (1901 N. Fort Myer Dr., Suite 602, Arlington, Va. 22209), San Diego Hilton, San Diego, Calif., Sept. 24–27.

**Fourth International Conference on Magnetic Bubbles,** Magnetics Society of Japan (Hiroshi Kobayashi, School of Science and Engineering, Waseda University, Tokyo), Garusmuin University, Tokyo, Japan, Sept. 24–27.

**Eascon 80, Electronics and Aerospace System Conference,** IEEE,



Management Information Display



Ultrasonic heart sector scan

High-resolution display with alphanumerics

# Get the professional color display that has BASIC/FORTRAN simplicity

## LOW-PRICED, TOO

Here's a color display that has everything: professional-level resolution, enormous color range, easy software, NTSC conformance, and low price.

Basically, this new Cromemco Model SDI* is a two-board interface that plugs into any Cromemco computer.

The SDI then maps computer display memory content onto a convenient color monitor to give high-quality, high-resolution displays (756 H x 482 V pixels).

When we say the SDI results in a high-quality professional display, we mean **you can't get higher resolution than this system offers in an** NTSC-conforming display.

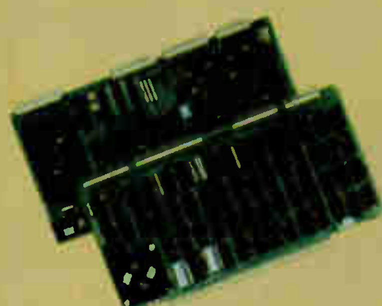
The resolution surpasses that of a color TV picture.

## BASIC/FORTRAN programming

Besides its high resolution and low price, the new SDI lets you control with optional Cromemco software packages that use simple BASIC- and FORTRAN-like commands.

Pick any of 16 colors (from a 4096-color palette) with instructions like DEFCLR (c, R, G, B). Or obtain a circle of specified size, location, and color with XCIRC (x, y, r, c).

*U.S. Pat. No. 4121283



Model SDI High-Resolution Color Graphics Interface

## HIGH RESOLUTION

The SDI's high resolution gives a professional-quality display that strictly meets NTSC requirements. You get 756 pixels on every visible line of the NTSC standard display of 482 image lines. Vertical line spacing is 1 pixel.

To achieve the high-quality display, a separate output signal is produced for each of the three component colors (red, green, blue). This yields a sharper image than is possible using an NTSC-composite video signal and color TV set. Full image quality is readily realized with our high-quality RGB Monitor or any conventional red/green/blue monitor common in TV work.


Model SDI plugs into Z-2H 11-megabyte hard disk computer or any Cromemco computer

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The Model SDI has been used in scientific work, engineering, business, TV, color graphics, and other areas. It's a good example of how Cromemco keeps computers in the field up to date, since it turns any Cromemco computer into an up-to-date color display computer.

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Sheraton National Hotel, Arlington, Va., Sept. 29–Oct. 1

**International Symposium on Telecommunication Processing,** Société des Electriciens, des Electroniciens, et des Radioélectriciens (Secrétariat Général du Colloque International sur la Planification des Réseaux, 11, rue Hamelin, 75783—Paris Cedex 16, France), Tour Oliver de Serres, Paris, Sept. 29–Oct. 2.

**SPIE's Huntsville Electro-Optical Technical Symposium,** Society of Photo-Optical Instrumentation Engineers (P. O. Box 10, Bellingham, Wash. 98225) *et al.*, Von Braun Civic Center, Huntsville, Ala., Sept. 29–Oct. 2.

**ICCC 80—International Conference on Circuits and Computers,** IEEE *et al.*, Rye Town Hilton Inn, Port Chester, N. Y., Oct. 1–3.

**Sixth International Conference on Very Large Data Bases,** IEEE, Hotel Méridien, Montreal, Oct. 1–3.

**Information Processing Joint Exhibition,** Japan Electric Industrial Development Association *et al.* (3-5-8 Shiba Koen, Minato-ku, Tokyo 105), International Fairgrounds, Tokyo, Japan, Oct. 3–8.

**Info 80—Information Management Conference and Exposition,** Clapp & Poliak Inc. (245 Park Ave., New York, N. Y. 10017), New York Coliseum, Oct. 6–9.

**Eighth World Computer Congress,** International Federation for Information Processing (U. S. Committee for the Eighth World Computer Congress, c/o Bowery Savings Bank, 110 East 42nd Street, New York, N. Y. 10017), Sunshine City, Ikebukuro, Tokyo, Japan, Oct. 6–9; Melbourne, Australia, Oct. 14–17.

**Military Electronics and Defense Exposition,** Industrial and Scientific Conference Management Inc. (222 W. Adams St., Chicago, Ill. 60606), Rhein-Main Halle, Wiesbaden, West Germany, Oct. 7–9.

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## The K100-D wins over Hewlett-Packard's 1615A hands down!

Logic designers have made Gould's powerful Biomation K100-D our fastest selling logic analyzer ever. You'll see why once you compare it to its nearest competitor, the 1615A from Hewlett-Packard.

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With a 100 MHz clock rate, the K100-D gives you resolution to 10 ns—*five times better than the 1615A's.* Use the K100-D's latch mode to catch gliches as narrow as 4 ns. It gives you the most precise logic analysis for today's high speed minicomputer, mainframe and microprocessor systems. Best of all, you're already prepared for faster designs as they arrive.

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**Compare your productivity.**

Finally, the K100-D makes designers more productive with convenience features superior to those of the 1615A. The K100-D has a larger keyboard, plus an interactive video display. Comprehensive status menu. Data domain readout in hexadecimal, octal, binary or ASCII. And the list goes on and on.

**The final analysis.**

To help you evaluate these two fine instruments before you buy, we've prepared a point-by-point *competitive comparison* of the two. If you're designing and debugging high-performance digital systems, you'll want to read this document carefully. To get your free copy, just use the reader service number or write Gould Inc., Biomation Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For faster response, call 408-988-6800.

**Hewlett-Packard 1615A**
**A very good logic analyzer**

*Speed: to 20 MHz*
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*Memory: 256 words*
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**Biomation K100-D**
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*Channels: 16 timing or 16 data, or 32 data*

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# Intel® RAMs advance

## Now at your command: Our full line of military RAMs.

In military and high-reliability applications, Intel's full line of MIL-spec RAMs continues to advance. Produced under our military products program, the RAMs listed below represent the pacesetters in memory devices, all built in full compliance with the Class B requirements of MIL-STD-883B, Methods 5004 and 5005.

**Intel® Military RAMs (Class B, MIL-STD-883B)**

| Model | Organization | Maximum Access (ns) | Current Active/Standby (mA) |
|---|---|---|---|
| **Static**[1] | | | |
| M2115A | 1Kx1 | 55 | 125 |
| M2115AL | 1Kx1 | 75 | 75 |
| M2125A | 1Kx1 | 55 | 125 |
| M2125AL | 1Kx1 | 75 | 75 |
| M2114AL-3 | 1Kx4 | 150 | 50 |
| M2114AL-4 | 1Kx4 | 200 | 50 |
| M2114A-4 | 1Kx4 | 200 | 70 |
| M2114A-5 | 1Kx4 | 250 | 70 |
| M2148H | 1Kx4 | 70 | 180/30 |
| M2147H-3 | 4Kx1 | 55 | 180/30 |
| M2147H | 4Kx1 | 70 | 180/30 |
| **Dynamic**[2] | | | |
| M2118-4 | 16Kx1 | 120 | 25/2 |
| M2118-7 | 16Kx1 | 150 | 23/2 |

[1]TA: −55° to 125°C
[2]TA: −55° to 85°C

For systems ranging from shipboard and ground communication systems to avionics and missile controls, these RAMs offer a way to forge ahead with cost-effective designs. And, because they're available now in volume, you can press them into service immediately.

### The RAM brigade, HMOS company

Intel revolutionized RAM design when we introduced our proprietary HMOS* technology. With HMOS, power consumption and corresponding cooling requirements are drastically reduced — both critical factors in military applications. In the denser static RAMs (M2147H and M2148H), automatic power down on deselection further reduces system power dissipation — a very important power and reliability advantage in larger systems.

Furthermore, with RAMs like the M2115A, M2125A, and M2147H, you can achieve fast access times for cache memories and for systems that process data in real time.

For microprocessor applications also, you need all the performance you can muster. For those, Intel offers the low-power MOS microprocessor-compatible M2114A. Or the high-speed M2148H, suitable for fast random logic and bipolar microprocessor designs. And for very high density applications, you can call out the M2118. It provides 16K of dynamic storage in a 16-pin package. Plus it uses only a single +5-volt supply, which reduces space requirements and increases system reliability.


### The vanguard in military microelectronics

Intel's advancing line of RAMs reflects our strong commitment to military customers: to continue to deliver the broadest line of LSI devices to military systems designers. From devices like the M8080A, the first microprocessor to receive JAN approval (QPL-listed as M38510/42001), through the M8085A, the world's highest performance 8-bit microprocessor, to the first military computer-on-a-chip: the M8048. And continuing on with other MIL-STD-883B products, such as EPROMs, bipolar PROMs, and microprocessor peripherals. We've shipped hundreds of thousands of these high-performance parts to vital military programs over the past four years. Proof of our commitment to remain the leader in military microelectronics.

### Our military aid program

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So the next time you're on the lookout for state-of-the-art military LSI devices, look to the leader — Intel. For further information on Intel's advancing line of military products, contact your local Intel sales office/distributor.

Or contact Intel Corporation, 3065 Bowers Ave., Santa Clara, CA 95051. Telephone (408) 987-8080.

*HMOS is a patented Intel process.

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"VISIT US AT WESCON BOOTH #2630"

# Electronics newsletter

**Inmos promises even faster 16-K RAM**

Inmos Corp., the British-backed semiconductor house raising industry eyebrows with an n-MOS static random-access memory that accesses typically in 30 ns (see p. 117), will offer "significantly higher performance" 4-K-by-4-bit versions of that device next year. Unlike the 16-K-by-1 IMS1400, which exploits novel circuit design for high speed but with conservative, 2.7-$\mu$m minimum features, **the 1420 and 1421 follow-up chips will use process enhancements as well**—like scaling down to tighter geometries—for even shorter access times. Since it is committed to step-and-repeat equipment, shrinking geometries to 2 $\mu$m would be no big feat for the Colorado Springs, Colo., firm. In addition, the 1421 will drop the automatic power-down feature to squeeze out another 5 to 10 ns. Intel Corp., now starting to ship samples of its 2167 16-K-by-1-bit fast static RAM, will also come out with a 4-bit-wide part. But at least for now, its Aloha, Ore., memory operation does not see a sufficient market for a 4-K-by-4-bit memory without power-down.

**Fast C-MOS process for ULA family under development**

A number of West Coast semiconductor firms are known to be working on low-power, high-speed processes similar to the Iso-CMOS popularized by Canada's Mitel Semiconductor, and now Semi Processes Inc. of Santa Clara, Calif., has developed a selective-oxidation, silicon-gate complementary-MOS process. Semi plans to use its technique in its first family of metal-mask–programmable uncommitted logic arrays, called Masterchips. **The initial offering from the supplier of custom wafer-processing services will be 1,000- and 544-gate versions with typical gate delays of 3 ns,** slightly faster than competitive ULAs made with the Mitel process. Semi achieves such speed with a 5-$\mu$m process that, when scaled down to 3-$\mu$m H-MOS geometries, is expected to yield subnanosecond gate delays.

**STC to acquire Florida maker of high-speed printers**

Storage Technology Corp., the Louisville, Colo., maker of high-performance tape drives and IBM-plug–compatible disk drives, has moved to broaden its coverage of the peripherals market. Itself the target in the past year of several acquisition and merger efforts, **Storage Technology has agreed to acquire Documation Inc.** of Melbourne, Fla., a maker of high-speed printers, for about $52 million in stock. STC's revenue in 1979 was $480 million; Documation's sales were $90 million for the fiscal year ending Feb. 1, 1980, which reflected a loss of $9.5 million.

**HP entering market for power FETs with D-MOS line**

Look for an introduction later this month of the first power field-effect transistors to be offered by Hewlett-Packard Co., Palo Alto, Calif. They will be produced using a double-diffused MOS process **and will have a guaranteed 450-V breakdown voltage and a surprisingly low on-resistance of 0.75 Ω.** Called H-Power, the product line will have HPWR model prefixes, and the first one being prepared is the HPWR-6501, packaged in a TO-3 can. Though prices have yet to be established, HP claims the line will be competitive with the 450-V, 1-Ω IVN6000 series recently introduced by Intersil Inc. [*Electronics*, July 17, p. 166]. The HP devices have a lower on-resistance, but their switching speed—below 50 ns—is somewhat slower. The devices are useful in switching power-supply systems, ac motor controls, and other high-voltage, ac-line applications.

# Electronics newsletter

**NCR to receive masks for 68000 in Motorola deal**

NCR Corp. of Dayton, Ohio, is acting as though it has big plans for the 68000 microprocessor. Hedging against the chance that its requirements will exceed Motorola Inc.'s capacity to produce the 16-bit devices, NCR will receive masks as part of its five-year contract for Motorola's flagship processor. Behind the concession by Motorola is the knowledge that **all of NCR's manufacturing plants are looking at the 68000 family,** and at least three—the Columbus, Ohio, plant, where point-of-sale equipment is made; Ithaca, N. Y.; and Raleigh, N. C.—have 68000-based projects under way for 1981 introduction. Under the deal, NCR is to receive mask sets for the 68000 and a minimum of three peripheral chips: the 68120 intelligent peripheral controller, the 68450 direct-memory-access controller, and the 68451 memory management unit. Up-front money also is involved.

**Digital scope with difference to bow in 1981**

Data Precision Corp., the Danvers, Mass., firm known for its digital meters, will introduce sometime in 1981 what insiders call a new concept in digital waveform analysis and display systems. The instrument, say knowledgeable sources, will "merge Data Precision's instrumentation know-how with [parent company] Analogic Corp.'s high-speed analog-to-digital conversion capability." **Data Precision sources do not even think of the unit as a digital oscilloscope,** feeling that it will mark a step in the state of the art beyond such devices. The instrument will fit a benchtop and be "very, very smart."

**Wired city closer with experimental communications test**

A new packet-switched local-area digital data-distribution system will begin operations in New York and San Francisco this November using a combination of existing cable TV lines and cellular radio communications. The service is a joint experiment by Satellite Business Systems Inc., Tymnet Inc., and LDC—a joint venture of M/A-Com Inc. and the Aetna Life & Casualty Co. [*Electronics*, April 24, p. 107]. The cities will be linked via an SBS satellite channel, Tymnet will operate the central node and switching systems in each city, and LDC (using hardware from another M/A-Com subsidiary, DCC Inc.) will coordinate the program and provide subscriber transceivers. **Local distribution is expected to get the most attention in the test.**

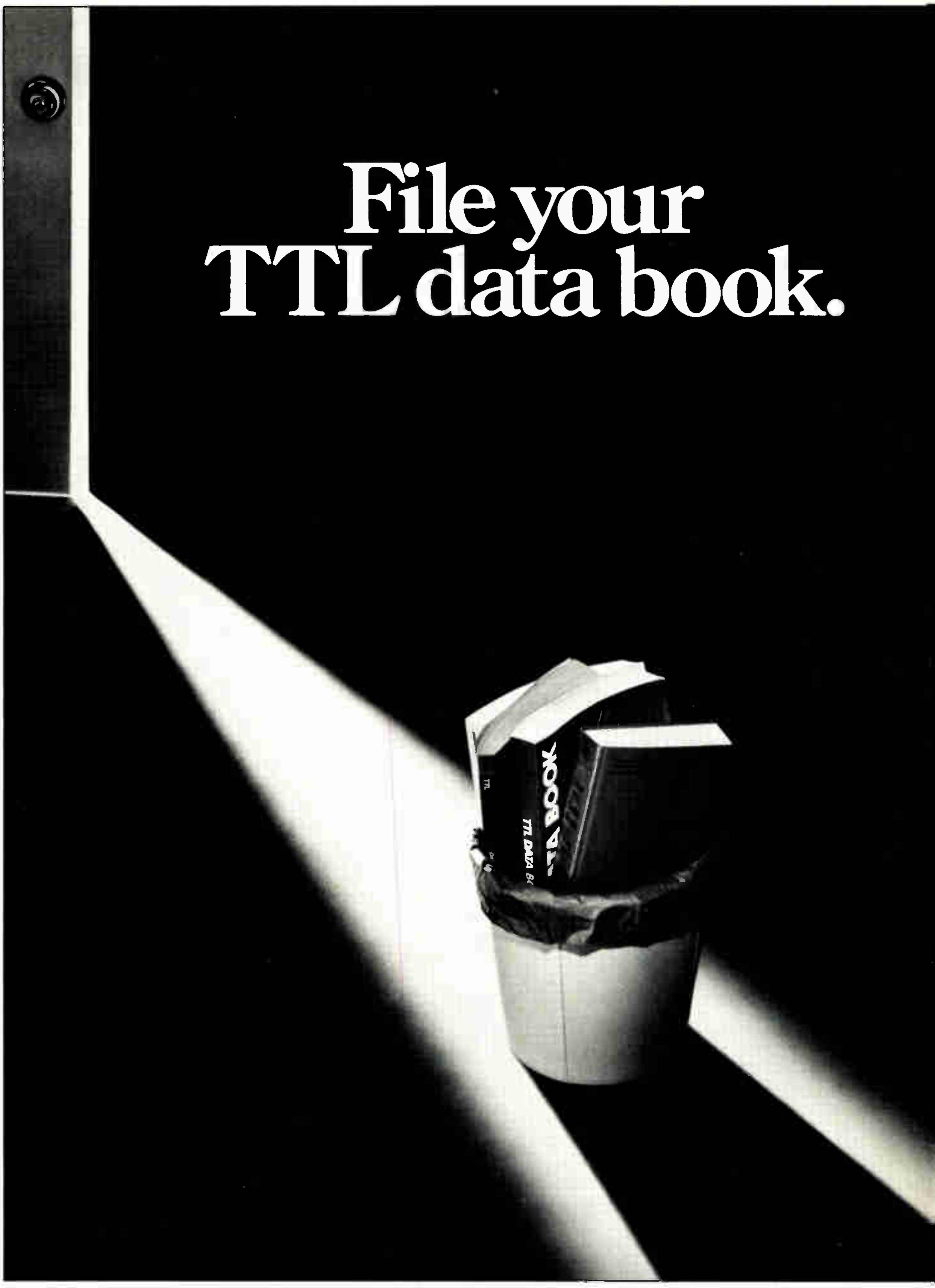
**Digital, analog abilities due in Teradyne tester**

The next generation of automatic test equipment from Teradyne Inc. will combine digital and analog in-circuit capabilities with emulation of final system environments for full functional testing of printed-circuit boards—**a first, according to the Boston firm.** Bowing at the Cherry Hill, N. J., test conference this November will be the $500,000 L260, representing the middle range of Teradyne's planned L200 series and slated for first deliveries in March 1981.

**Addenda**

Mostek Corp. is jumping on the complementary-MOS bandwagon with a **C-MOS version of its 3870 microprocessor family** suitable for battery-operated equipment. Due from the Carrollton, Texas, MOS house is a pin-compatible 38C70 with two power-saving instructions; also being developed is a real-time clock peripheral chip. . . . **Intersil Inc. and General Electric Co. are believed to be discussing merger possibilities.** GE is said to have made an offer of $35 a share.

Circle 35 on reader service card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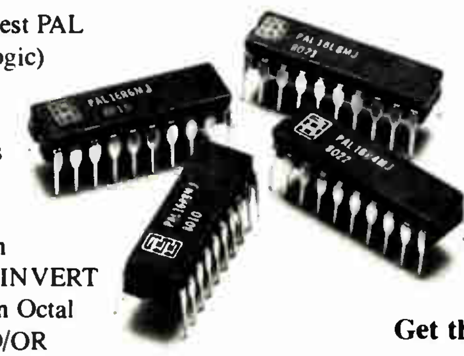
TTL data book.

# Four new PAL® devices join the family that's making TTL logic obsolete.



They're here. Our 4 newest PAL (Programmable Array Logic) devices make a total of 13 in the instant custom logic family that replaces up to 90% of the entire 54/74 *S* and *LS* series logic. Meet PAL16L8, an Octal 16 Input AND/OR/INVERT Gate Array, PAL16R8, an Octal 16 Input Registered AND/OR Gate Array, PAL16R6, a Hex 16 Input Registered AND/OR Gate Array, and PAL16R4, a Quad 16 Input Registered AND/OR Gate Array. And soon MMI will introduce two additional PALs with arithmetic functions.

**PAL—The Programmable Solution™ — saves you space, time and aggravation.**

A single PAL 20 pin SKINNYDIP™ can replace from 4 to 12 TTL devices. But pc board space isn't all you save. Lower system cost, smaller inventory requirements, reduced parts count and high-volume, off-the-shelf, multiple sourced availability,* make PALs the most cost-efficient logic devices on the market. And every PAL can be programmed by any PROM programmer with a PAL personality module.

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For your complimentary copy of the new Bipolar LSI Data Book and further information on the revolutionary PAL logic family, contact your local MMI stocking distributor or sales representative. Monolithic Memories, Inc., 1165 East Arques Avenue, Sunnyvale, California 94086.

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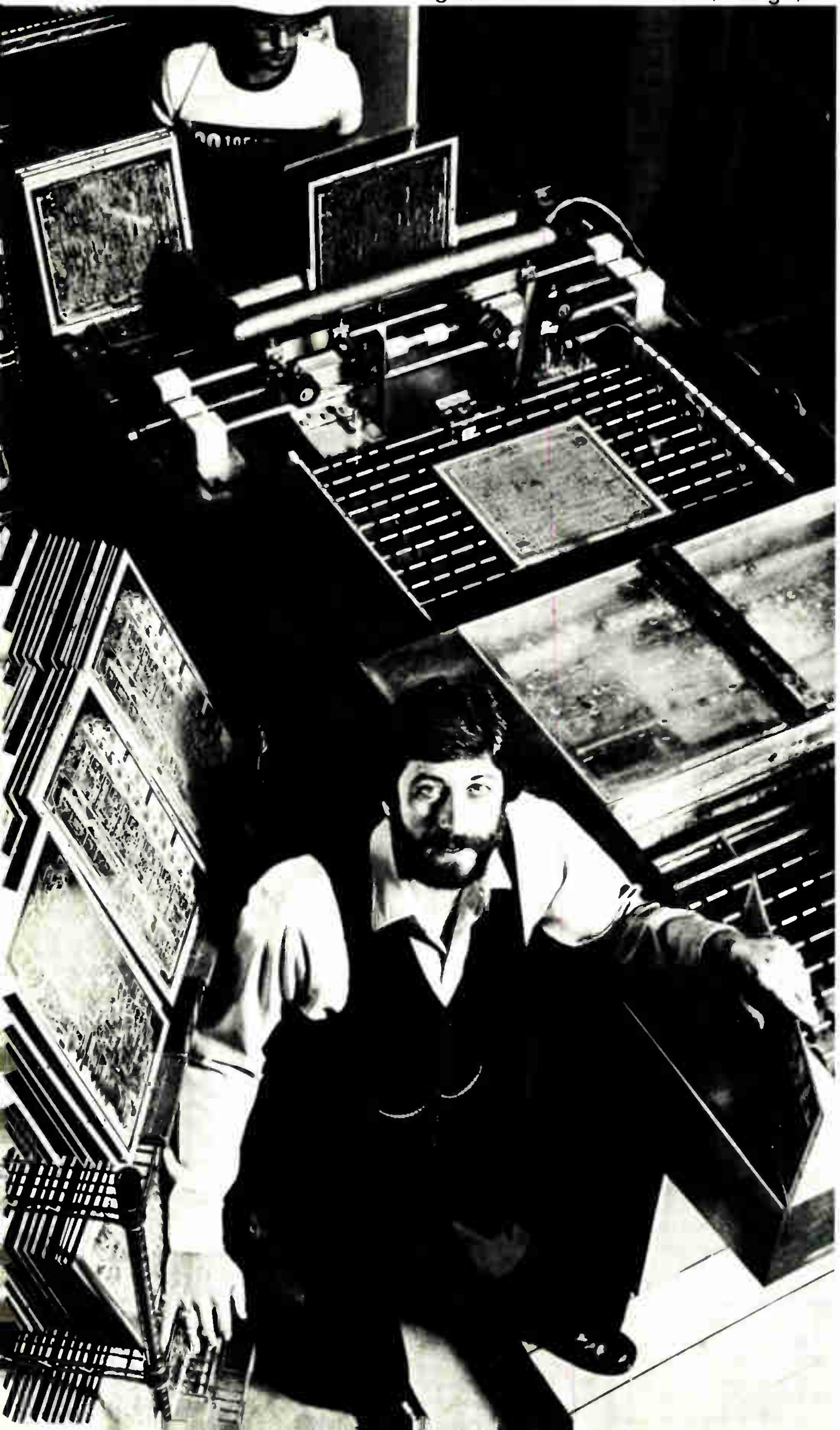
**Monolithic Memories** MMI

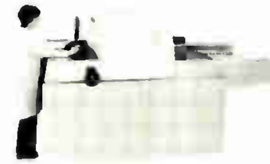
# "360 panels an hour outstrips any aqueous system we've ever used."

Dana Schofield, Plant Manager, Hadco Printed Circuits, Owego, NY



## A Riston® UAS-24 Ultrasonic Aqueous Stripper works hard at boosting Hadco's productivity.

Now that they're using a RISTON Ultrasonic Stripper, Hadco Printed Circuits of Owego, N.Y., can process double-sided, plated-through-hole boards with RISTON aqueous films at the rate of 4 to 6 panels a minute. That's up to 360 panels an hour.



The ALL-AQUEOUS UAS-24 is designed for high productivity and in-line operation with etching. It has an automatic panel transport mechanism which processes panels (up to 24" x 24") in one continuous operation.

Using ultrasonics, the UAS-24 removes resist cleanly and completely from plated boards with up to 6 mils of overplate—even on fine-line circuitry down to 3 mil spacing. And the system is reliable and easy to service because it's operated by a programmable controller.

We've shown you how HADCO maximized their stripping productivity with the new RISTON Ultrasonic Stripper. We'd like to show you how *you* can, too. For more information and a brochure on RISTON all-aqueous film and equipment systems, write: RISTON High Productivity Systems, DuPont Company, Room 38132, Wilmington, DE 19898.

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# Metallurgical silicon comes into play for solar cells

by James B. Brinton, Boston bureau manager

Relatively impure silicon, cost-saving production processes are being tried

**Metallurgical-grade** silicon, plus more efficient crystal-growth and -slicing technologies, is brightening the prospects for much cheaper solar cells. The photovoltaic materials maker Crystal Systems Inc. is developing use of the relatively impure silicon and of its Government-funded cost-saving production techniques to help the industry reach the Department of Energy's 1986 goal of 70¢-per-watt cells.

In fact, Fredrick Schmid, president of the Salem, Mass., company, is so confident of the potential of the research effort that he is projecting 25¢/W cells, perhaps well ahead of the DOE's 1990 goal of 15 to 50¢/W. A major reason for this reduction would be the switch from costly semiconductor-grade silicon to metallurgical-grade material. Another possibility, which others are considering, is amorphous silicon [*Electronics*, Aug. 28, p. 40].

**Purity.** Semiconductor-grade silicon is typically better than 99.999% pure and sells for from $65 to $70 per kilogram. Metallurgical-grade silicon is usually about 99% pure—though many lots are purer—and costs only about $1.20 a kilogram.

Schmid's firm has made solar cells using both types, achieving a 15% conversion efficiency with semiconductor-grade silicon and 12.33% with metallurgical-grade material. Since the work with the cheaper material is still new, Schmid expects better efficiencies to emerge. Even if they fail to materialize, today's 2% to 3% efficiency difference is not a bad trade for a sixty-fold reduction in materials cost, he feels.

"If he can reproducibly use this inexpensive material to make cells, Schmid will have gone a long way toward meeting our price-performance goals," says Paul Maycock, head of the Department of Energy's photovoltaic energy systems division. "So far, he has shown that he can use it to make good single crystals and reasonable solar cells."

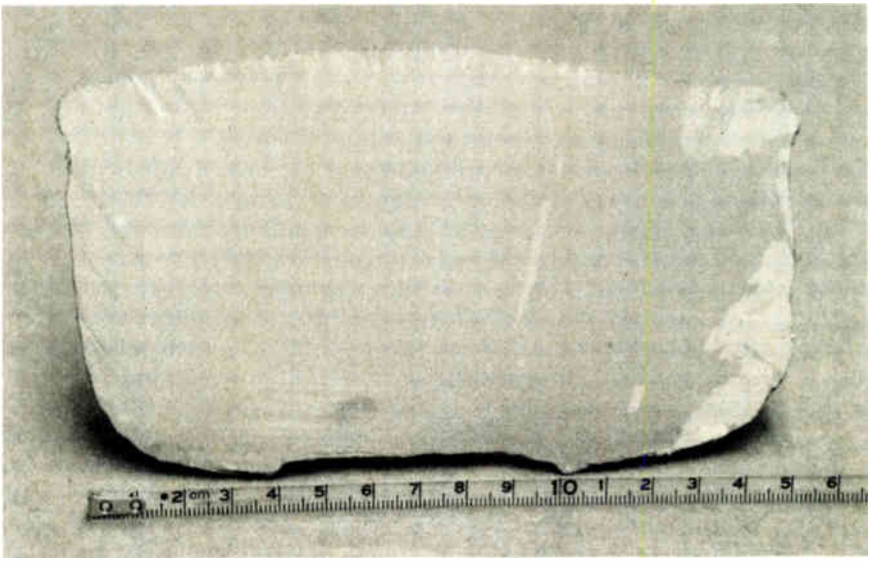
But reproducibility may be a problem. Crystal Systems often must request special lots of metallurgical-grade silicon with higher-than-average purity. Obviously, for production quantities of low-cost cells, supplies of this slightly purer metallurgical-grade silicon must be dependable.

"We can tolerate about 10 parts per million of impurities and still make good cells," he says. "But it is necessary to be selective; what's needed is an intermediate grade of silicon."

He says silicon vendors respond favorably when approached about such a new silicon grade. But he notes "a chicken-and-egg problem."

**Dilemma.** Solar cells are now such a small part of their business that it is hard to justify the capital expenditures an intermediate grade would dictate. "On the other hand, solar cells are a potentially huge market," he says. "Right now, vendors are falling between two stools."

Help may already be on the way, though. A source at the DOE's Solar Energy Research Institute, Golden, Colo., says that companies like the Dow Corning Corp., Midland, Mich., are attacking the problem by



**Solid stuff.** Using metallurgical-grade silicon melt stock, Crystal Systems is manufacturing an ingot intended for photovoltaic use that is close to being single-crystal in structure.

using purer starting materials and cleaner production techniques.

Cheaper silicon alone will not make possible 15¢-to-50¢/W cells, says Schmid. His optimism is partly based on Crystal System's HEM, or heat-exchanger method, for making large ingots of single-crystal silicon [*Electronics*, Oct. 25, 1979, p. 12]. Not only is HEM said to save a third of the power, labor, and materials used in the more common Czochralski process, but it also allows production of ingots with a square cross section. Some are as large as 13 by 13 inches and weigh up to 110 pounds, Schmid says.

**Stack.** He already is producing square ingots and wafers for sale to makers of solar cells. Its present commercial stock is based on 8-by-8-in. ingots and is being sold to Arco Solar Inc., among others.

Arco Solar says it has bought evaluation quantities of the square wafers. The DOE's Maycock notes that square ingots are 25% cheaper than round ingots and wafers, which must be trimmed to rectangular shape, wasting silicon.

Crystal System's other cost cutter is its FAST, or fixed abrasive slicing technique [*Electronics*, July 20, 1978, p. 44]. Though about a year away from commercial use, FAST already is capable of getting as many as 68 wafers from an inch of ingot, versus the 24 to 25 possible with current technology, Schmid says. He is looking for yields of up to 100 wafers per inch with FAST which could mean the equivalent of a fourfold materials-cost reduction.

Together, the move to lower-cost silicon, HEM's 30% efficiency edge and its square ingots' 25% cost benefit, and FAST's expected 400% improvement in wafer yield per inch of ingot make Schmid's price projections reasonable. But use of metallurgical-grade silicon may be the keystone; as one of Schmid's competitors noted, "if Fred can do that, he's got a big advantage."

## Photovoltaics

# Thick film, plating cut cost of laying down solar cell contacts and conductors

The struggle to cut the costs of photovoltaic cells has many facets, including cheaper fabrication methods for the metal conductors and contacts on the cells. A small solar-cell maker in Tempe, Ariz., may have developed just such a technique, which depends on using thick-film nickel contacts and electroplated copper conductors.

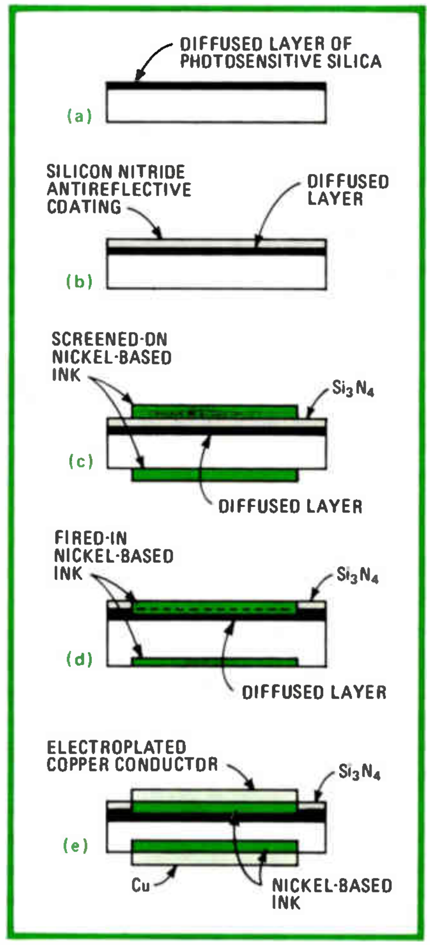
In Photowatt International Inc.'s method, there are many fewer steps than in evaporation techniques for forming thin-film contacts. What's more, there is no need for the expensive photolithographic techniques used to make thin-film conductors.

**Screening.** Instead, Photowatt uses a simple screening and firing of thick-film conductors, followed by a plating step. With thin-film methods, there can be five or six steps.

As the figure shows, the first step in the Photowatt method is to evaporate an antireflective thin layer of silicon nitride over the diffused junction layer of a silicon solar cell. Then a special air-fireable nickel-based thick-film ink, developed by Photowatt with Thick Film Systems Inc., Santa Barbara, Calif., is screened on to form the contacts.

Then the nickel paste is fired, driving it through the silicon nitride into the diffused silicon and forming an ohmic contact. This step is carefully controlled through an exact, proprietary temperature-time relationship, says Clayton Olson, manager of Government contracts for Photowatt.

Finally, a copper conductor layer is selectively electroplated over the nickel surface. The method was developed at Selectrons Ltd., Waterbury, Conn., for repairing traces on printed-circuit boards. Vanguard Pacific Inc. applied it to the problem of low-cost, high-conductivity solar-cell contacts. The anode is a graphite stylus wrapped with an absorbent material and dipped into an organic copper solution. The stylus traces the pattern of the nickel contacts, which act as a cathode in the process.




**Simpler metalization.** Photowatt International needs only three basic steps to fabricate solar-cell contacts and conductors: steps (c), (d), and (e) above.

**Copper.** Previous attempts at screening on thick-film conductors could not use copper pastes because copper diffuses into silicon. Instead they have used silver or aluminum pastes, which have much lower conductivity—but which are compatible with silicon.

The Photowatt developers got around the problem by electroplating the copper. This method also costs much less than either screening or evaporation of metals.

Photowatt's development so far has been internally financed, but the company is applying for funds from the Jet Propulsion Laboratory, Pasadena, Calif., to make the process commercially viable. The proposed program would result in a pilot line, and cell samples would be used in extensive life tests. -Jerry Lyman

## Memories

# Overcoats protect RAMs from alphas

Keeping those troublesome alpha particles at bay is forcing the semiconductor industry to apply protective coatings as random-access memories move to the 64-K level. Cleaner packaging materials, clever circuit design techniques, and other efforts aimed at reducing alpha sensitivity may not be enough to meet users' requirements.

Already, the list of 64-K RAM manufacturers who supply, or profess plans to supply, parts with protective die coatings includes Texas Instruments Inc., Motorola Inc., Hitachi Ltd., Toshiba Corp., Mitsubishi Electric Corp., and Fujitsu Ltd. Despite some disagreement, many RAM makers, including Intel Corp. and Inmos Corp., believe that die coats are likely to become a requirement for 64-K dynamic and 16-K static RAMs.

**Natural.** Ionizing alpha radiation emitted by naturally occurring trace thorium and uranium isotopes in packaging materials was first uncovered as a source of nondestructive soft error problems in charge-coupled-device and 16-K dynamic memories [*Electronics*, June 8, 1978, p. 42]. It is more of a problem as geometries and critical charge levels diminish.

"We have looked at 64-K parts from about a half-dozen manufacturers, some U.S. and some Japanese," says Dennis Wong, component engineer in charge of RAM qualification at Hewlett Packard Co.'s Data Systems division in Cupertino, Calif. So far, Wong says he has not seen any 64-K part without a die coat capable of meeting HP's goals for resistance to alpha-induced soft errors.

"Almost universally, the 64-K vendors are going to die coats," says an engineer, who asked to remain nameless, at another large computer house. He reports test results that are similar to HP's.

In general, users are looking for 64-K parts that achieve alpha-tolerance levels at least equal to those measured on 16-K RAMs. That level is pegged at from 1,000 to 2,000 FITs—a designation for failures in $10^9$ hours.

Some RAM makers claim to have met that goal with their 64-K offerings, whereas others admit to falling significantly short. At Texas Instruments Inc. in Houston, MOS memory development manager Dick Gossen says the TMS4164 comes in at about 1,200 FITs on tests using an accelerated alpha source.

Gossen says the Dallas-based company will begin converting to a die coat on 4164 products during the fourth quarter this year to get even better reliability. He foresees more stringent user requirements on alpha sensitivity even for chips going into large systems that employ error-correction circuitry.

**Shipping.** At Motorola Inc.'s MOS Integrated Circuits operation in Austin, Texas, MOS memory strategic marketing manager David C. Ford indicates that even best-case projections show that his company's MCM6664/65 devices would suffer soft-error rates between 10,000 and 100,000 FITs without a protective die coating. Motorola began shipping 64-K parts using an organic poly-

### Die-coating techniques diverge

There's no question that die coatings will help ward off the onslaught of alpha particles, but there is some question about the best techniques to use. Users have expressed concern over potential reliability problems associated with some of the coatings.

Though the semiconductor industry has examined a variety of coating materials including silicones and epoxies, an organic polyimide seems to be the most frequent material of choice. Motorola is applying a commercially available polyimide substance in liquid form to its 64-K RAMs during package assembly. The coating varies in thickness from about 1 mil across the array to about 5 mils around the edges of the device.

Hitachi uses a polyimide of its own development known as PIQ [*Electronics*, July 31, p. 103] and says that a thickness of about 2 mils will sufficiently reduce the energy of incoming alpha particles. The company has been using this type of resin for several years in linear circuits, both as an interlayer insulator and as a moisture shield for aluminum wiring. Toshiba and Mitsubishi say they will use a polyimide coating, and Fujitsu says it will use some type of resin coating but it will not specify the material.

In contrast, Texas Instruments Inc. has developed a technique that uses a polyimide film about 3 mils thick that is machine-cut and applied to the die with a silicone adhesive. Since the coating will be form-fit to cover only the array and sense amplifiers, TI officials believe the technique will be more uniformly reproducible and may avoid potential problems with some liquid application techniques in which the polyimide covers the bonding areas.

In the liquid approach, differing thermal expansion coefficients of the polyimide and the die could result in bonding wires being pulled off during the curing process or later in the field, TI says. Motorola's David Ford concedes that bonding integrity is a valid concern, but notes that some nine months of reliability testing done by his firm included thermal cycling tests that revealed no problems.

Other concerns involving potential for die contamination or corrosion were also allayed by the testing, he says. Motorola has developed a liquid application technique that ensures reproducible uniform coating thickness, he claims. The company also looked at using film but saw such potential difficulties as alignment problems, adhesion breakdown in the field, and higher cost than liquid application techniques, he reports. -W. I.

mide overcoat in July [*Electronics*, July 31, p. 33].

Still, there are some holdouts. Mostek Corp., for example, does not plan a die coat on its 64-K product scheduled for fourth quarter introduction. The Carrollton, Texas, company can add it if necessary, says Sam Young, a Mostek memory-marketing official.

"Coating is a step in the right direction," remarks Kirk MacKenzie, strategic marketing manager of Intel's Aloha, Ore., memory components division. But "it doesn't replace trying to reduce alpha sensitivity in the design."

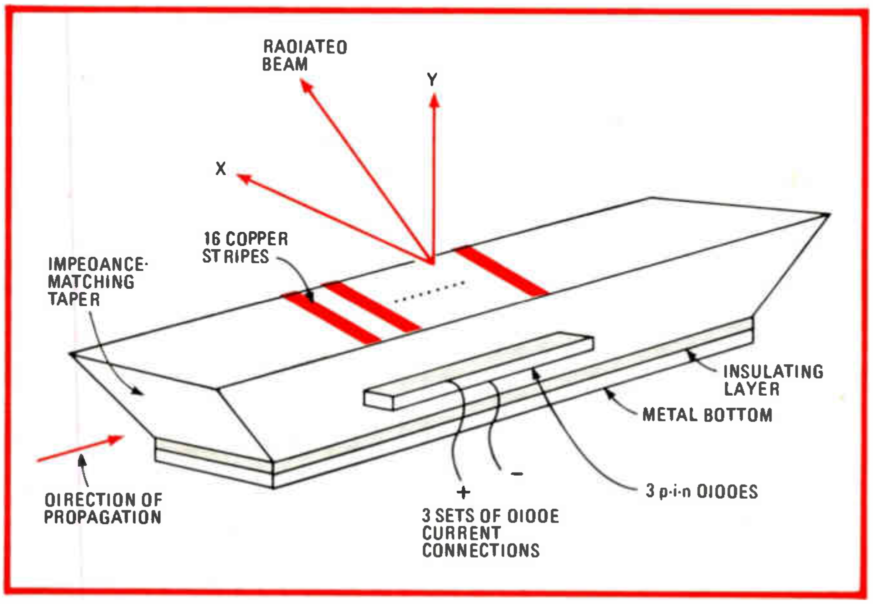
The company has used a coating in a 16-K CCD memory, now discontinued. It has both a 64-K dynamic and a 16-K static RAM in the sampling stages, and as for coating them, "between now and the end of the year, we'll figure that out," says MacKenzie.

Inmos also has a 16-K static RAM (see p. 117) and a 64-K dynamic part planned for production, though the latter is not as far along as Intel's. The Colorado Springs, Colo., company has not yet settled the coating question, says David R. Wooten, manager of strategic marketing and applications. One point to consider, he says, is that even if 64-K cell sizes were as large as in 16-K dynamic parts, alpha particles still would cause trouble. **-Wesley. R. Iversen**

## Military

# P-i-n diodes steer silicon antenna

Electronical steering of antennas' output beams from millimeter-wavelength radars may be about to move from the realm of "nice ideas, but . . ." into the real world. Researchers at the U.S. Army Research and Development Command at Fort Monmouth, N. J., are working on such a replacement for expensive and slow mechanically steered antennas by using p-i-n diodes for steering the beam.




**Silicon steering.** Current in the diodes of this silicon-slab antenna steers the radiated beam. The reflecting metal bottom plate ensures that all power radiates from the top.

"Our development may lead to future beam-scanning antennas for operation at millimeter frequencies," says Harold Jacobs, millimeter-wave devices team leader at the Electronic Techniques and Devices Laboratory. "For now, it can be said that it is low-cost and easily fabricated and has a lot of potential for practical radar scanning."

**Useful.** Such attributes are important, for other attempts to design electronically scanned millimeter-wave antennas have foundered on the rocks of cost and complexity. The interest in these designs stems from the military's emphasis on developing millimeter-wave radars, because they have much better resolution than do lower microwave frequencies and so stand a better chance of identifying ever faster flying targets.

Jacobs and his colleagues Robert E. Horn, Elmer Freibergs, and Kenneth L. Klohn started with a 0.1-by-0.1-by-13-centimeter silicon rod with 16 copper foil strips cemented across the top (see figure) These strips direct the microwave energy that would otherwise propagate straight through the silicon dielectric slab into a beam that radiates off the rod at an angle.

This phenomenon is well known, and the innovation of the group lies in its having determined that the spacing between p-i-n diodes on the rod's sidewalls and their impedance, plus the wavelength of the microwave energy within the silicon and several other parameters, interact to determine the angle of the beam.

"When the diodes are nonconducting or unbiased by an external voltage, the wavelength is some constant predetermined value, which in turn determines the radiation angle," says Thomas. To vary the wavelength and thus the angle, the researchers simply change the dc voltage on the diodes.

"When the diodes are biased in the forward direction, this is equivalent to the mechanical movement of a metal wall up the side of the silicon slab," he says. "This changes the wavelength of the energy inside the slab and varies the angle of the radiated energy beam."

**Angles.** Typical changes in the beam's angle are from 8° to 10° at 63 gigahertz with as much as 13° in some cases. A bias current of only 100 milliamperes is needed in each of the three diodes used.

The scanning angle in the patented device is not always a continuous function of the diode current. To obtain this analog scanning for more accurate target acquisition, the researchers are varying the rod dimensions, the copper strips, and the

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diodes. They have met with some success already, Thomas notes.

What's more, they are trying to expand the scan angle to 20° or so, thereby increasing the usefulness of their antenna, which even now has enough angle variability for some applications. **-Harvey J. Hindin**

## Solid state

# Custom designers seek standard test chips

Designers of custom integrated circuits are banding together in search of a standard for test chips, the patterns added to semiconductor wafers to check the quality of fabricated IC dice. Without the test patterns added to a wafer of custom ICs, they find they are facing costly and often imprecise testing procedures, stemming from the low production volumes of their designs.

Custom design by its nature produces nonstandard ICs and testing has always been a problem, though less acute with large runs that in effect become standard circuits. But a burgeoning user group of university research and development laboratories, government agencies, and small original-equipment manufacturers are ordering small runs of their own designs from semiconductor makers.

**Meeting.** Representatives of this group met recently on the Pasadena, Calif., campus of the California Institute of Technology and took the first tentative steps towards standard test chips. They also found themselves in debate with representatives of the IC production houses on the issue of process versus device testing.

"We need test chips in multipurpose chip runs to determine whether a fabricator has done his job in providing the devices the designer specified," says George Lewicki, organizer of the Cal Tech session and a staff member at Information Science Institute, Los Angeles, which coordinates design R&D for the Pentagon's Defense Advanced Research Products Agency. The need is for a check on device performance, not process parameters, said Lewicki and designers at the session.

Such a vision of the test chip runs counter to the accepted wisdom. For example, the National Bureau of Standards (another sponsor of the conference, along with the Jet Propulsion Laboratory at Cal Tech) has developed a number of test chips to verify processing quality, and these work well for the semiconductor makers.

However, IC makers balk at disclosing their test methods, because they could reveal process secrets. Lewicki and others say that reluctance makes it difficult to get the

## Dictaphone doubles up on processors

Not one, but two single-chip microcomputers nestle inside Dictaphone Corp.'s new line of dictation/transcription equipment. The Rye, N. Y., subsidiary of Pitney Bowes Inc. has put processors in past products, but the new Dictamation line is the company's first double-barrelled use.

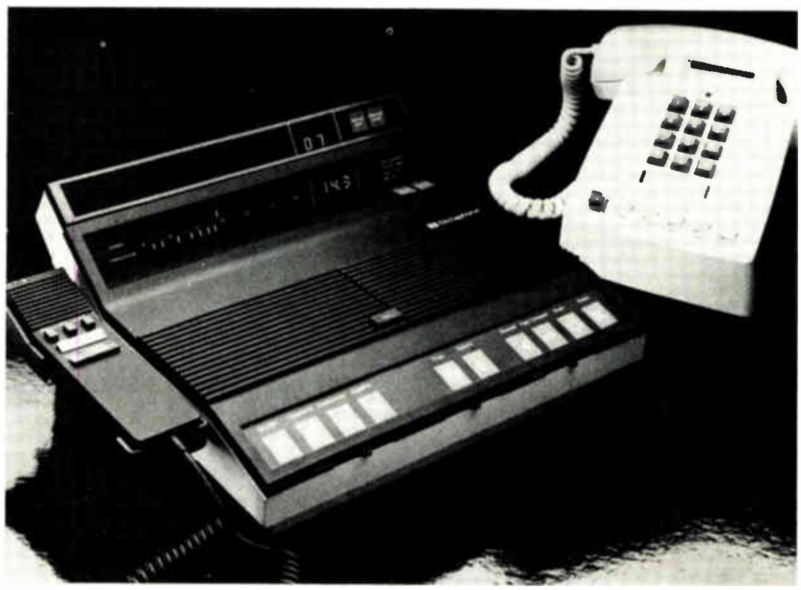
As before, the processors' primary functions are to provide the user with control features and information about the machine's operation. However, the degree of control and the amount of information is greatly expanded.

One of the microcomputers, a National Semiconductor Corp. 4-bit COP 420, controls up to 15 touch-sensitive function keys, including the row of 11 at the base of the machine in the photograph. "The processor controls the interrelationships among various functions, including a full remote-control microphone," says William R. Blash, director of program management.

The other chip, an 8-bit 3870 from Fairchild Camera & Instrument Corp., controls display functions by interacting with the 420 or by reading out tone-coded data indicating the beginning or end of a letter or the presence of special instructions entered on the tape by the dictater.

The light-emitting-diode displays run across the top of the machine and include a time-chart display that shows the times on the 30-minute tapes where letters begin and where special instructions have been dictated. An alphanumeric display shows such information as the length of a letter, and four LED rectangular lamps light to indicate the lack of a cassette and other warnings. Prices in the Dictamation product line will range from $495 to 650, depending which control features are included.

An option on the new family also shown below is the Messagemaster telephone message center, a module that fits on top and includes another display and two function keys. Users may control it remotely, over the telephone line. **-Pamela Hamilton**



(Advertisement)

Don McCafferty

# Choosing the right mechanical fastener

When choosing a mechanical fastener for a particular application, following past company design practices or an in-house preference list may cause you to overlook current "state of the art." When viewing an application, start fresh and consider the following:

MATERIAL COMPATABILITY between fastener and components is a must. If dissimilar materials are to be used, check a galvanic series chart to assure compatibility of base materials. Don't forget to investigate plating or other special finish options.

STRESS AND VIBRATION are factors that dictate type, diameter and number of fasteners, which, in turn, affect spacing. Spacing rules are: 1) On-center spacing between fasteners should be *no less* than three fastener diameters. 2) Fasteners should be placed no less than two diameters in from the edge of materials being joined.

USE A SINGLE FASTENER TYPE for comparable functions to save money.

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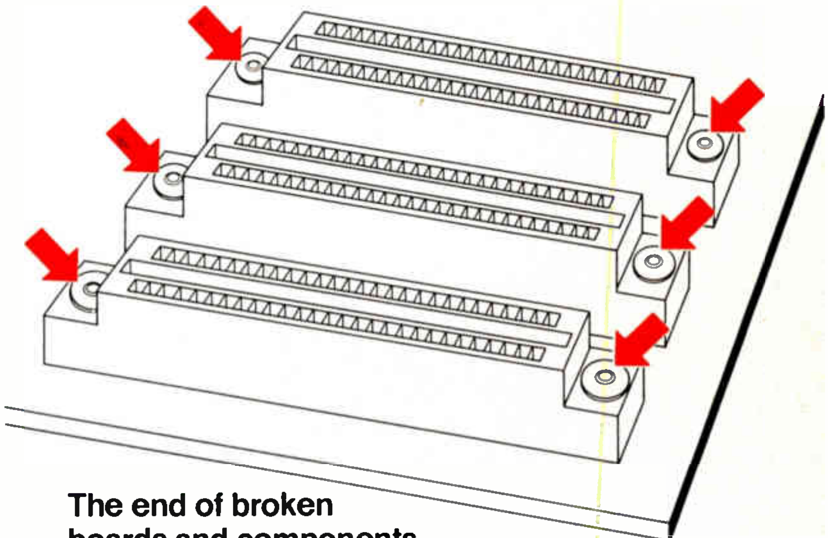

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specific performance data needed to build good test chips.

Actual working circuits cannot function as benchmarks when the custom ICs are few in number. Similarly, it would be impossible for each of the organizations at the Cal Tech conference to design its own test chips. "None can afford to invest enormous time or resources in test vehicles," says Lewicki.

**Consensus.** Thus standardized test structures holding devices that should meet known performance parameters are needed. The conference did not reach agreement on exact test chip configurations, but there was a consensus that the structures must give specific data on the performance of elementary devices like transistors and inverters.

Considering reactions from semiconductor houses, conference attendees decided they need to come up with test vehicles that provide useful data, not "jury chips" that can be used to determine the fate of an entire chip run. Also, "we have to make it clear that processing is the fabricator's business, and we have no interest in spotting any troubles," says Lewicki. **-Larry Waller**

## Microwaves

# All's quiet on the front for military uses

The U. S. military microwave market will march along at an annual growth rate of 15% to 20% in the next five years, but technologically the period will be at parade rest. In fact, there will be no radical shifts in components or systems, in terms of their dollar impact on the market, says a just published study from the New York consulting firm, Frost & Sullivan Inc.

Evolutionary technology—a continuing trend—means that established firms must look for growth by increasing share in their traditional markets, rather than by opening up new markets with technological breakthroughs. For new firms, which traditionally are born with a technologically innovative product to offer, evolution means it will be difficult for them to make their mark.

MICROWAVE CONTENT OF MAJOR U.S. MILITARY SYSTEMS (millions of dollars)

| Systems | 1980 | 1981 | 1982 | 1983 | 1984 | 1985 | Total |
|---|---|---|---|---|---|---|---|
| Radar | 665 | 810 | 985 | 1,155 | 1,330 | 1,500 | 6,445 |
| Electronic warfare | 420 | 510 | 630 | 745 | 880 | 1,005 | 4,190 |
| Communications | 38 | 44 | 50 | 56 | 61 | 63 | 312 |
| Navigation | 48 | 55 | 65 | 73 | 80 | 88 | 409 |
| Other | 33 | 36 | 38 | 40 | 38 | 38 | 223 |

SOURCE: FROST & SULLIVAN

"It is true the market will expand [see table], but this will be because of additional quantities of both present and gradually changing components," says Henry M. Berler, Frost & Sullivan's vice president for research. "Even if there were a significant technological change, by the time planning, funding, and development cycles are considered, we would be in 1987."

**Decade.** Since nothing technologically of note has taken place during the past five years, these time scales make it clear that the next five will be less than exciting, says the study. "Even the much heralded developments in microwave gallium-arsenide field-effect transistors are not an exception," Berler says.

"Sure, this is a growth area, but it is not a structural shift of any appreciable magnitude in the microwave components market." Of course, he is referring to dollar content, and not to the ultimate technological significance of GaAs FETs.

The consulting firm does expect better than a fivefold increase in sales of millimeter-wave parts, from $20 million in 1980 to $110 million in 1985. Yet the base is very small, it points out, and "even at the wildest prediction, total millimeter-wave sales will not exceed 5% of the military microwave market." By 1985, Frost & Sullivan expects applications in missiles and point-to-point communications.

The 1975–85 evolutionary trend indicates that microwave components and systems are mature technologically. The parts available can do the jobs that users want accomplished. True, the standard evolutionary trends are there—ever-improving bandwidths, the endless search for lower-noise parts, and solid-state parts nibbling away at microwave vacuum tubes.

**More.** Add to evolutionary technology the industry's other problems, says Frost & Sullivan. There is a shortage of engineers, both because military procurement cycles have caused major personnel upheavals in the past and because engineering schools are turning out predominantly digital designers.

Perhaps even more important is the classic inability of most microwave firms to attract large capital infusions so that they may fully adopt modern industrial engineering techniques to increase productivity. The great bulk of the companies, especially in the components end, remain mom-and-pop operations, garnering annual revenues of $3 million or less. **-Harvey J. Hindin**

## Military

# 'Invisible-plane' plan has many goals

"Invisible" aircraft that can defeat enemy radar are suddenly very visible, with the Carter Administration preparing for battle in this fall's presidential election. But, as interviews with Department of Defense and industry officials make clear, Circle 46 for literature

Circle 47 for demonstration

accelerated development is under way on a second-generation subsonic Cruise missile and pilotless reconnaissance planes employing a mix of technologies to make them virtually undetectable by ground or airborne radar or infrared systems.

A manned bomber is the ultimate goal. A secondary goal for the Stealth program is the development of manned tactical fighters and reconnaissance planes using a similar mix of advanced aerodynamics, absorbent plastics and ceramics, and other technologies. Such planes also would be enhanced by active electronic countermeasures considered too costly for missiles like the Cruise family.

**History.** The effects on radar of absorbent paints have been known since Hitler's Luftwaffe used them, and absorbent materials for radio-frequency and radar anechoic chambers and for aircraft have been available for more than two decades. Now the Pentagon is committing more than $100 million a year to advance the technology.

"The problem is that an aircraft, or parts of it, either can act like an antenna, reradiating radar signals that strike it, or because of its design, say, around the air intakes, wing roots, tail, and so on, can act like a corner reflector, bouncing the incoming wave back in the direction from which it came," says M. William Frasca, sales manager of the microwave products group of Emerson and Cuming, Dewey & Almay Chemical. The Canton, Mass., subsidiary of W. R. Grace & Co. makes absorbers for anechoic chambers and absorbing material for aircraft applications.

However, "radar cross section is more than a matter of covering an airframe with an absorptive material," Frasca continues. "It has to take the physical relationships of the various parts into account to minimize re-emission and reflections."

Equally important are infrared emissions, for they attract radar-controlled heat-seeking missiles. One goal of Stealth is prototypes of a new Cruise missile class with movable forward-swept wings that conceal

## News briefs

### Amdahl seeks to sell 2,000,000 new shares

In a move that should raise over $50 million in capital for the development of new computers, Amdahl Corp. of Sunnyvale, Calif., is planning to sell over 2 million new shares of common stock. The mainframe computer maker will sell about 1.35 million shares to the public and another 650,000 shares to its largest shareholder, Fujitsu Ltd. Although the official announcement specified only that the money would "be available for the expansion of working capital and to finance computer leases to customers, as required," a company spokesman suggested still other uses. Amdahl needs to add capabilities in the front-end processor and communications areas beyond its acquisition of Tran Telecommunications Corp. of Marina del Rey, Calif., in July, he said. Since the corporation does not see the right kind of company available for acquisition, it will probably build up its own capability. The financing of computer leases mentioned by the company, other sources indicate, points to the introduction of a new generation of computers. "They're just waiting for IBM to announce the H series next year," claims one expert. The company spokesman acknowledged that Amdahl is currently spending heavily on research and development for the new computers and that some of the new capital will be used there.

### Photons help NBS, IBM study surface of solids

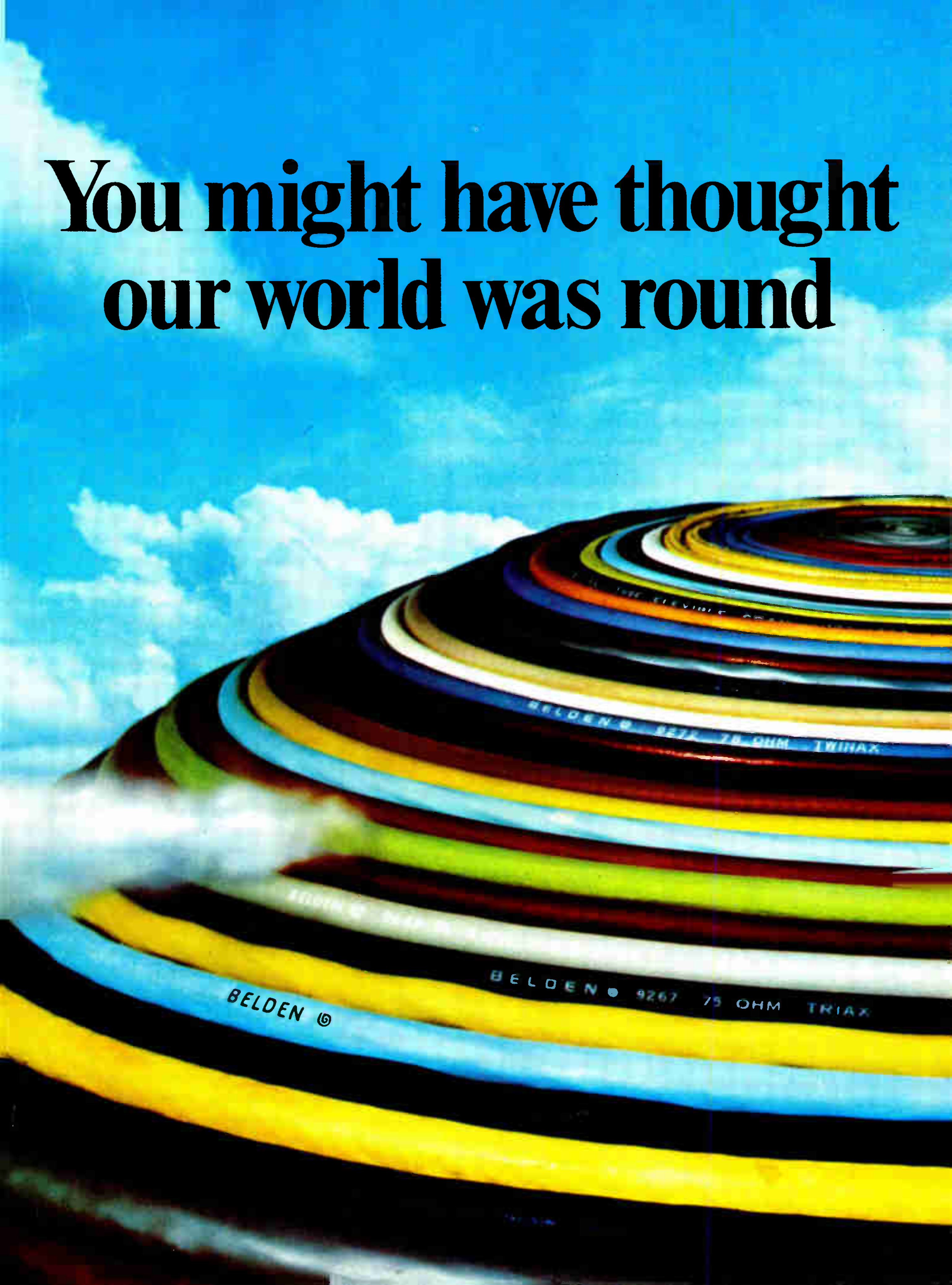
Researchers at the National Bureau of Standards in Washington, D. C., and International Business Machines Corp.'s Thomas J. Watson Research Center, Yorktown Heights, N. Y., have jointly developed an improved technique for studying the surfaces of solids, possibly including semiconductor crystals. In the new method, termed angle-resolved photon-stimulated desorption, selective cleaving of surface chemical bonds provides information about their angular orientation. Unlike electron-stimulated desorption systems, the quantized photons impart either all or none of their energy to a target surface atom. Using 8-to-120-electronvolt X rays derived from a tunable synchrotron, inner atomic-shell electrons that have absorbed photon energy are selectively stripped off, causing positive ions to be released from a crystal's surface. Low-energy electron diffraction has also been used to determine surface states, but a highly ordered crystal is required. What's more, the new technique will both locate and determine the angle of surface bonds for samples lacking such long-range order, and relatively little mathematical computation is required.

### AT&T to replace Comstar satellites with Hughes-built Telstar 3

American Telephone & Telegraph Co. wants Federal Communications Commission approval for a June 1983 launch of the first of three high-capacity domestic communications satellites. The series, called Telstar 3, is to be built by Hughes Aircraft Co. under a $137 million contract awarded at the end of August; FCC approval is expected this year. The satellites will handle 21,600 simultaneous conversations and have a 10-year design life, compared with the 18,000 links and seven-year lifetime of the Comstar satellites they will replace. The Comstar satellites are leased by AT&T from Comsat General Corp., the Washington, D. C., subsidiary of Communications Satellite Corp. Hughes will also build a new 13-meter antenna at AT&T's Hawley, Pa., tracking station to help place the satellites in orbit, as well as serve as a backup control for the three 30-meter antennas there. The second satellite is set for launching in 1984 and the third for 1985 or 1986.

### Module turns scope into waveform recorder

To replace special-purpose units costing thousands of dollars, a small instrumentation company in Foster City, Calif., has developed a $295 front-end module that transforms an ordinary oscilloscope into a waveform recorder. Dubbed the Wavesaver by Epic Instruments Inc., the module acts as a triggered 1,000-sample buffer that digitizes its samples with an 8-bit resolution accurate to within 1 least significant bit.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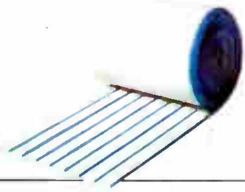

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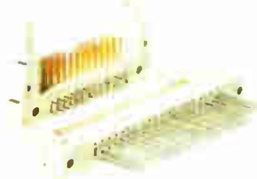

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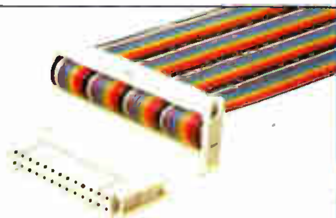

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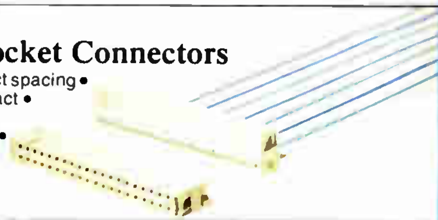

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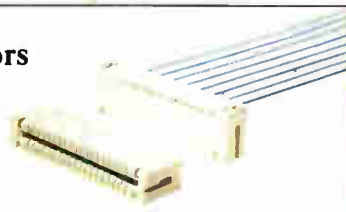

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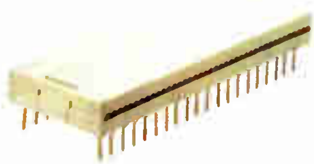

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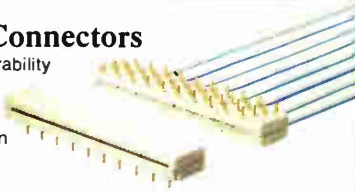

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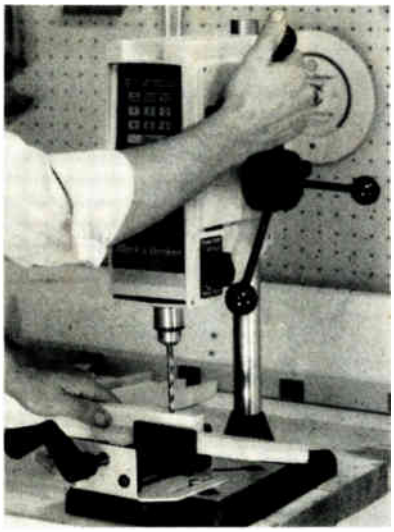
## Processors control home drills



Now it's going to be microprocessors in the home shop, as well as in the kitchen range, the bathroom scale, and the stereophonic receiver. Black & Decker Manufacturing Co. has a drill press (right) and a hand-held drill controlled by 8-bit 3870 microcomputers from Motorola.

"We wanted to improve the speed-control aspects of our tools," says John W. Casner, product manager for the Towson, Md., firm. "Most tools' torque diminishes at low speeds, but many situations require the low speed for the user to be in command of the tool. With digital control, we are able to maintain torque even at low speeds." The microcomputer uses a triac to control conduction of current to the motor. The 3870 monitors the motor's speed 120 times a second.

Both the 9413 drill press and the 7266 reversing drill have a shut-off controlled by the microprocessor, to stop them if incorrect speed or drilling pressure is used too long. "We've developed algorithms that model how a drill fails and use these instead of a thermocouple or heat sensor," says Casner. "They're better than a heat sensor that depends on heat transfer and that can't be put on a rotating armature anyway."

Under processor control, the drill press indicates the depth of the hole being drilled in 20-mil increments, also storing in memory the last speed used. The user can check on the current drill speed as well. It will carry a suggested retail price of about $180, while the reversing drill will sell for about $100. For the drill press, that is roughly 20% more than comparable units without microprocessor control; the reversing drill has a number of features that other drills do not, so prices cannot be compared directly. **-Pamela Hamilton**

engine intakes and a minicomputer-controlled movable exhaust nozzle to deflect the IR output.

DOD funds are going to a handful of airframe, engine, and electronics firms participating in an effort guided by a Lockheed Aircraft Corp. team. Under Secretary of Defense William J. Perry acknowledges that Stealth's budget "is 100 times greater than when we decided to accelerate the program in 1977," but he declined to specify amounts. He did say that Stealth-like programs have been going on for two decades.

Perry said the Soviet Union "has built thousands of surface-to-air missile systems employing radars with high power and monopulse tracking systems, which are very difficult to jam. In the past few years, they have developed air-to-air missiles guided by look-down radars that are capable of detecting low-flying aircraft in ground clutter."

Three years ago, he continued, the DOD concluded that the "invisible" technologies found in first-generation Cruise missiles could make manned aircraft "so difficult to detect that they could not be successfully engaged by any existing air defense system." Perry asserted that "existence of the Stealth program has become public knowledge because of the program's rapid growth and the consequent need to involve more people in Government and industry."

He claims "excellent success" for Stealth flight tests, and other DOD officials claim that two crashes so far in the program were not caused by technology failures. The result of the program may well be aircraft with re-emission and reflection signatures undetectable by present Soviet radars—but an open question is whether such planes will be invisible to future, more powerful detection gear. **-Ray Connolly**

**Computers**

## Updated hardware is route for mini net

With competition getting rough in the field of minicomputer-based distributed data-processing systems, manufacturers are busily upgrading their offerings. Among them is Computer Automation Inc., which is keeping intact all its proven networking software and upgrading its hardware.

"Our goal is to push for maximum hardware performance without going out onto any shaky technological limbs," says George Dashiell, who runs the Irvine, Calif., firm's Commercial Systems division. While the Syfa 2000 can operate with an IBM host computer, like the predecessor Syfa 1000, it adds processing muscle for more powerful remote data processing. Among the changes:

- A central processing unit based on the company's LSI 2/120 processor, rather than the earlier LSI 2/60.
- A cache memory for instructions, plus modules of 256-K instead of 64-K bytes, operating at 525 nanoseconds rather than 700 ns.
- Microprocessor-based front-end controllers for peripheral interfacing, data-base management, and communications protocols.
- A "semiconductor disk" that is in effect a cache for two disk drives.

The result is throughput at least twice as fast as the Syfa 1000. Interestingly, other minicomputer makers like Digital Equipment Corp. have found their route to upgraded distributed processing is improved software [*Electronics*, Feb. 14, p. 183]. The impetus for much of this upgrading is IBM's System 8100, the computer giant's maiden effort in the field. **-Larry Waller**

# The Pacesetter.

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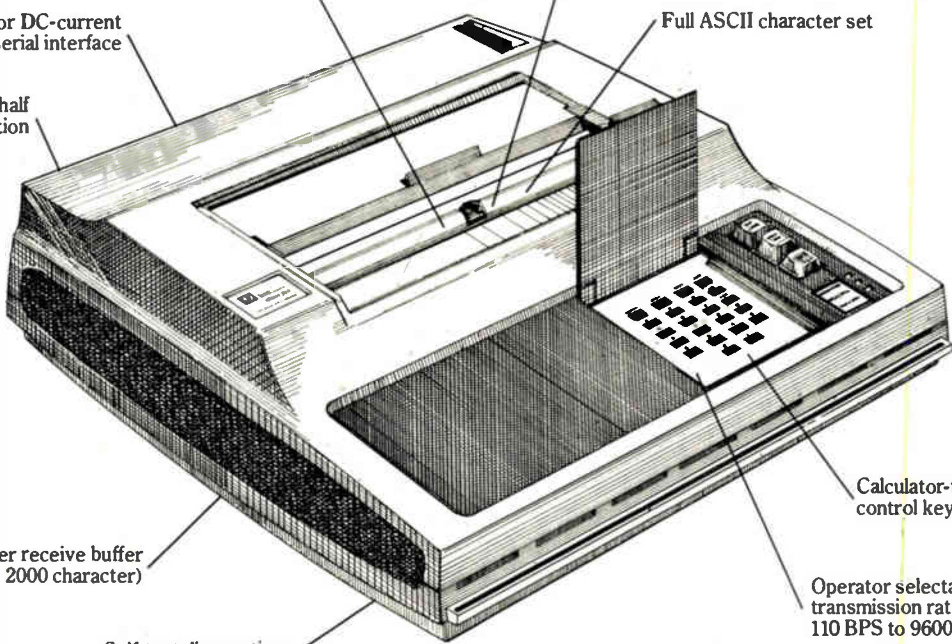


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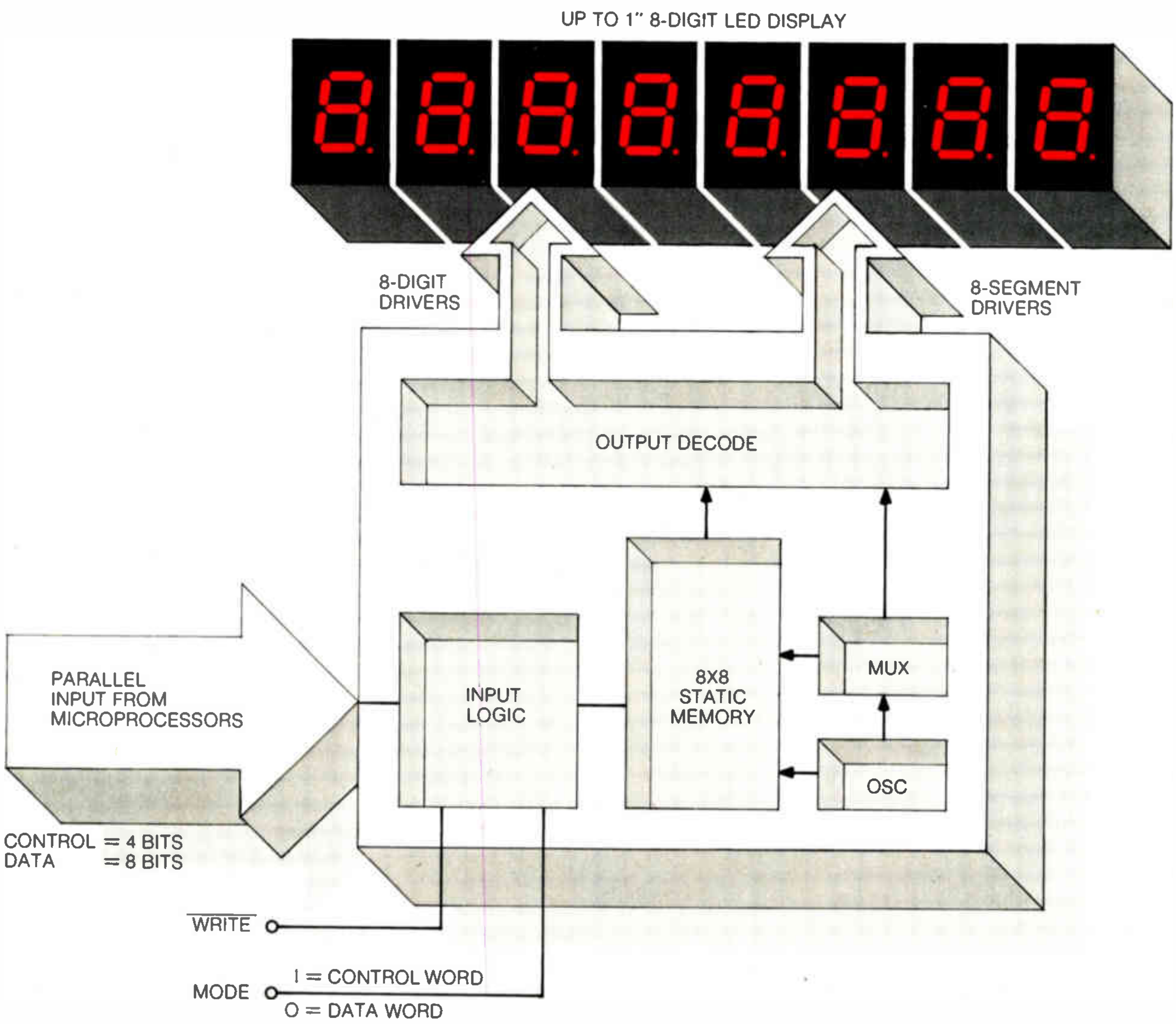


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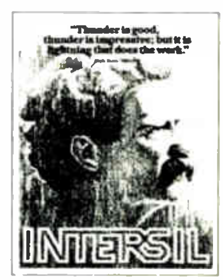


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**Adapso battling Bay State tax plan for EDP services**

Not since Colonial protesters dumped British tea into Boston Harbor has a tax proposal produced greater distress. This time the rebels are the 425 corporate members of the Washington-based Association of Data Processing Service Organizations (Adapso). They are fighting the proposed extension of a 5% Massachusetts sales and use tax to computer program transactions—including **most timesharing services, remote and batch processing, keypunching, and other forms of data conversion—and professional software services.** All of these, of course, are the corporate lifeblood of Adapso's members, who view the Massachusetts tax program's passage as part of a trend that could become a national threat. California, Connecticut, and Wisconsin already have software service sales taxes, and Tennessee imposes a property tax.

Thus, more than 100 industry members descended on Massachusetts Commissioner of Revenue L. Joyce Hampers at the end of August to vigorously protest the plan to tax computer program transactions. "The regulation exceeds the limits of Massachusetts law," argues Adapso attorney Ronald J. Palenski, since **the computer services offered by association members "are personal service transactions,** within which sales of tangible personal property [now subject to tax] are either absent or inconsequentially involved." Purchasers are buying the professional or personal services that went into developing a computer program, Palenski contends, rather than property containing the program, such as a reel of computer tape.

**Survey satellite with 10-terabit memory forecast**

A highly automated earth-survey satellite with a 10-terabit memory is among the proposals to emerge from a National Aeronautics and Space Administration workshop. The 10-week summer session assessed potential systems for space in the next 25 years. Using its vast memory to store a periodically updated world model, **the satellite would report only exceptions to the model,** such as crop condition changes, ignoring established phenomena. This approach, concludes the workshop of engineers and scientists from NASA, universities, and industry, would result in a "major reduction in the amount of data that must be transmitted and analyzed."

**Solarsat heating of ionosphere is negligible, says NTIA**

Would microwave transmissions from a solar-power satellite (SPS) to a ground antenna for electricity production raise the temperature of the ionosphere, damage its value as a telecommunications medium, and alter the earth's environment? The threat is negligible, replies a new report by the Commerce Department's National Telecommunications and Information Administration following **simulations of ionospheric heating** at its Boulder, Colo., facility. The NTIA's Charles Rush, principal author of the report, says high-frequency radio waves were used, since less energy density is required to achieve the heating effect in the ionosphere. Then Omega (very low frequency), Loran-C (low frequency), am radio broadcasts, and other **known signals were monitored after passing through the heated ionosphere.** The impact on the signals was minimal, it says, as was the level of ionospheric heating that a solar-power satellite operating at 23 $mW/cm^2$ could be expected to produce. The NTIA report, number 80-37, by Rush and others at the Institute of Telecommunications Sciences is entitled "Impact of SPS heating on Vlf, Lf, and Mf Telecommunications Systems Ascertained by Experimental Means." It may be obtained for $9 from the National Technical Information Service, Springfield, Va. 22161.

# Washington commentary

## The politics of Stealth

Technology and politics are mixed regularly in Washington, but rarely with such a heavy hand as when Defense Secretary Harold Brown briefed the press on Stealth—the label assigned to the $100 million–plus research and development effort to reduce radar detection of U. S. subsonic cruise missiles and aircraft (see p. 46). Brown and his under secretary for research and engineering, William J. Perry, are being accused of playing election-year politics with a top-secret program to bolster the Carter Administration's sagging defense image. And there is much evidence to support the charge.

After a story citing successful flight tests using the mix of technologies that make up Stealth appeared late in August in the Armed Forces Journal, a monthly publication with close ties to the military establishment, Brown got a lot of media mileage by confirming the program's existence, saying, "It alters the military balance [with the Soviet Union] significantly." Yet the fact that the Defense Advanced Research Projects Agency (Darpa) is heavily involved with the Air Force in the Stealth program is evidence that Brown was overstating the Pentagon's case. Darpa projects are invariably 7 to 10 years away from producing a deployable weapon. Darpa's role, as Brown himself put it in congressional testimony early this year, is "to explore the leading edge of technology."

### Conning the Congress

Congress wants a new bomber, as it recently demonstrated by giving the Pentagon some $300 million it had not requested for fiscal 1981 to begin exploring the parameters of such a weapon. At the same time, the legislators called on the President to decide by next March 15 whether the new bomber would be a stretched General Dynamics FB-111, a resurrection of the Rockwell International B-1 canceled earlier by President Carter, or an altogether new weapon employing advanced technologies.

The potential for Stealth's technologies—a complex mix ranging from super-strong absorbent plastics for new aerodynamic structures to computer-dispensed aerosols laden with particles to decoy enemy radar—is certainly excellent for the long term. But their use for a long-range manned bomber is more than a decade away, according to countermeasures specialists, whereas cruise missiles, followed by tactical reconnaissance aircraft, promise a much earlier payoff. Thus the Darpa-USAF program is pursuing the advanced cruise missile option, even though Pentagon leaders continue to give the distinct public impression that Stealth's greatest promise is in bombers.

Political rhetoric aside, a computer-controlled flying bomb with extended range holds the greatest promise for balancing the military scales in the U. S.–USSR arms contest in the shortest possible time. Secretary Brown acknowledged in January that the Soviets now have some 12,000 surface-to-air missiles for bomber defense, plus about 2,600 manned interceptors. Moreover, the Soviets are developing what he calls "a significant look-down, shoot-down capability in some versions of the MIG-25," a plane with an exceedingly powerful radar. Says one Pentagon analyst: "We can buy a host of cruise missiles that could be indistinguishable in radar for the price of one highly visible bomber. And that should be made clear to Congress. It is going to take a lot of weapons to penetrate that [Soviet] air defense network, if we are ever forced to do that, and a new bomber is not the answer. The strategic bomber, like the battleship, is obsolete."

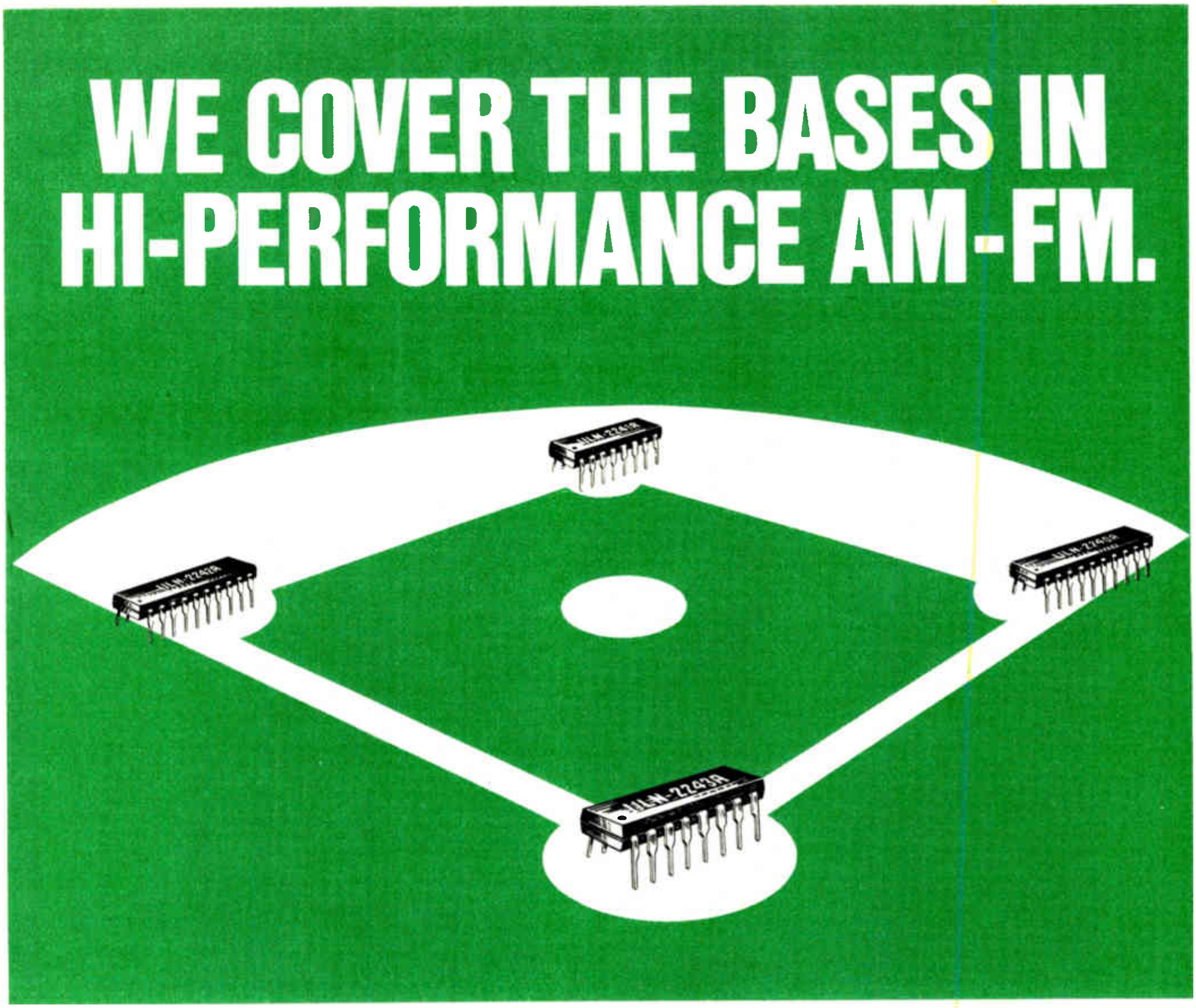
### Changing ECM pattern

Such judgments are bound to upset makers of airborne electronic countermeasures hardware, for most ECM systems are now considered far too costly for one-shot cruise missiles. Cruise missile designers are now concentrating on Stealth's materials program to further reduce their radar detectability, which could eventually provide a boost to ECM producers. For tactical manned aircraft, ECM techniques developed under Stealth should keep the latter busy.

Even busier will be makers of airborne minicomputers that must be able to do much more than perform the primary role of guidance and navigation. With new lightweight materials for airframes and engines providing extended range, cruise missile computers must be programmed to carry out a variety of evasive actions on longer flights to targets. These functions, too, are a part of Stealth's technologies.

Under the guidance of Air Force Lt. Gen. Kelly H. Burke, deputy chief of staff for research, development, and acquisition, and Darpa director Robert Fossum, the Stealth program stands an excellent chance of reaching its targets. But they and the countermeasures community know—just as Secretary Brown and Under Secretary Perry know—that it will be some time before the military balance between America and the Soviet Union is altered by Stealth and the weapons improvements it promises.

**-Ray Connolly**

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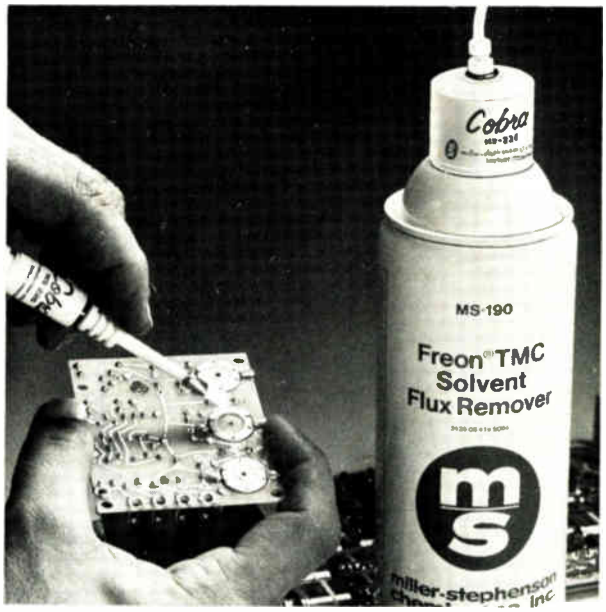


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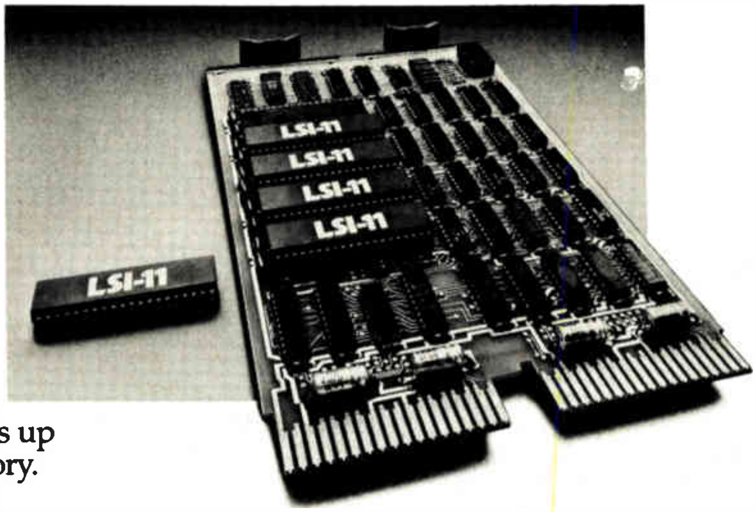


**It took the minicomputer company to make micros this easy.**

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**UK moves to second-generation fiber optics . . .**

British Telecom, part of the British Post Office, is likely to speed its move from first- to second-generation fiber-optic systems as a result of successful systems trials at its Martlesham Research Centre. In them, **optical data was transmitted in one hop on low-loss graded-index fiber over 49 km** with a margin of 3 dB remaining at the repeater. The data rate was the 140 Mb/s typical of first-generation systems now going operational. But by moving from a 0.85-$\mu$m to a 1.5-$\mu$m operating wavelength, fiber losses are cut by almost an order of magnitude to less than 0.5 dB/km, greatly extending the repeater spacing from the 10 km adopted in first-generation systems and enhancing the economic attractions of fiber-optic systems.

Trials have awaited the development of a suitable high-sensitivity detectors, and for this purpose p-i-n diode structures have been optimized for operation at 1.3- and 1.5-$\mu$m wavelengths. At 1.3 $\mu$m, a gallium indium arsenide diode on a gallium arsenide substrate from Plessey Co.'s Allen Clark Research Centre is used; at 1.5 $\mu$m, an indium gallium arsenide diode on an indium phosphide substrate is used.

**. . . as first British fiber links cut over to public service**

Fiber-optic systems are now moving from evaluation to routine operation on Britain's telephone network following the switchover last week of a 9-km, 8-Mb/s link carrying live traffic between Brownhills and Walsall. Engineered for the post office by Plessey Telecommunications Ltd., the system—to be followed shortly by the first section of General Electric Co. Ltd.'s Reading-to-London 140-Mb/s Link—is **one of 15 totaling 450 km and operating at 8, 34, and 140 Mb/s.** They have been ordered by British Telecom from Plessey, GEC, and Standard Telecommunications Laboratories Ltd. as part of its so-called shop-window fiber-optic program and scheduled for completion by 1982. Follow-on orders are expected shortly, with a likely first order for more advanced systems operating at a 1.3-to-1.5-$\mu$m instead of 0.85-$\mu$m wavelength and with intermediate repeaters spaced at 30-km instead of 10-km intervals.

**Data processing boosts employment in West Germany**

While West German entertainment electronics producers are plagued by slumping business, shorter work weeks, and other production curtailments, makers of data-processing equipment are wallowing in orders and facing production bottlenecks. For example, in "reacting to lively domestic and foreign demand," Nixdorf Computer AG is **resorting to overtime work and special weekend shifts** for 2,000 employees at its Paderborn manufacturing facility. Also, after adding some 1,400 new jobs last year, the firm has increased its work force by more than 1,000 in West Germany and abroad during the first seven months of this year, bringing the worldwide total to about 12,300. Siemens AG, too, is keeping up its hiring campaign to attract more people to its Munich-based data-processing equipment division. That division's work force increased by about 12% over that of a year ago and now stands at more than 20,000.

**East Germans trade medical electronics with rest of Comecon**

The policy of "socialist integration"—that is, joint research, development, and supply efforts in various economic and technical fields among Comecon Bloc countries—has of late been extended to medical electronics after having been practiced for some time in computers and communications. Among the latest results is an agreement whereby East Germany will deliver between 1981 and 1985 **such products as electrocardiographs,**

**patient-monitoring systems, electroencephalographs, and fetal monitors** to the Soviet Union and other East Bloc countries in return for medical apparatus from its Comecon partners. At the same time, cooperation in producing medical electronic subsystems and modules will be intensified now that Comecon-wide standards have been agreed upon.

## IBM Japan Ltd. takes over IBM's business in China

International Business Machines Corp. has transferred its operations in the People's Republic of China to IBM Japan Ltd. to take advantage of the geographical proximity and support capability of the Japanese subsidiary. The business was formerly handled by IBM World Trade Americas/Far East Corp. The People's Republic now has one IBM computer, a 370/138 that was installed in April 1979 in the Shenyan Ventilator Works for production control. It is to be replaced by two 4331 mainframes. The First Ministry of Machine Building also has a 4341 on order. Furthermore, **a United Nations–supervised census scheduled to start next year will use 21 computers in the 4300 series**—IBM will not say which model.

## NATO awards UK air defense contract to international group

A first-stage $240 million contract for updating Britain's air defense system—known as Ukadge, or UK air defense ground environment—has been awarded by the North Atlantic Treaty Organization to an international consortium **consisting of Plessey Avionics and Communications, Marconi Avionics Ltd., and Hughes Aircraft Co., with Thomson-CSF as an equipment contractor.** Announced at last week's Farnborough International Air Show, the contract is the first of several expected to be awarded as NATO completes the modernization of its European air defense net.

## New Siemens computer takes on jobs just beyond microcomputers

Look for Siemens AG to introduce at next month's Interkama exhibition in Düsseldorf a read-only memory version of its well-proven disk-based R10 computer, a member of the company's 300 systems family. The new R10, which extends the 300 series downward, is **intended for solving simple tasks in automated production** where existing microcomputer systems are limited in central memory capacity and processing speed. It has a 16-bit structure, boasts 16 universally applicable registers, implements more than 300 commands, and features an optional floating-point processor. The central memory may consist of erasable programmable and random-access memory modules, the latter expandable up to 40 kilowords. As for the ROM set, it is expandable up to 64 kilowords. The R10 programs are compatible with those for the Siemens 300 computer models.

## Sweden to launch first satellite

The Swedish government has given final approval for the nation's first satellite. Named Viking, it will be used for research into the ionosphere and magnetosphere in northern latitudes and will cost $25 million. **The main contractors will be Saab-Scania, which will supply electronics and instrumentation, and Boeing Co., which will provide the platform.** The satellite, to be launched by an Ariane rocket from the European Space Agency launching site in French Guyana in 1984, will be **in a polar orbit, with the highest point 15,000 km and the lowest about 800 km.** An on-board solar energy package will have an output of up to 80 W. Data transmission will be at 7,000 b/s.

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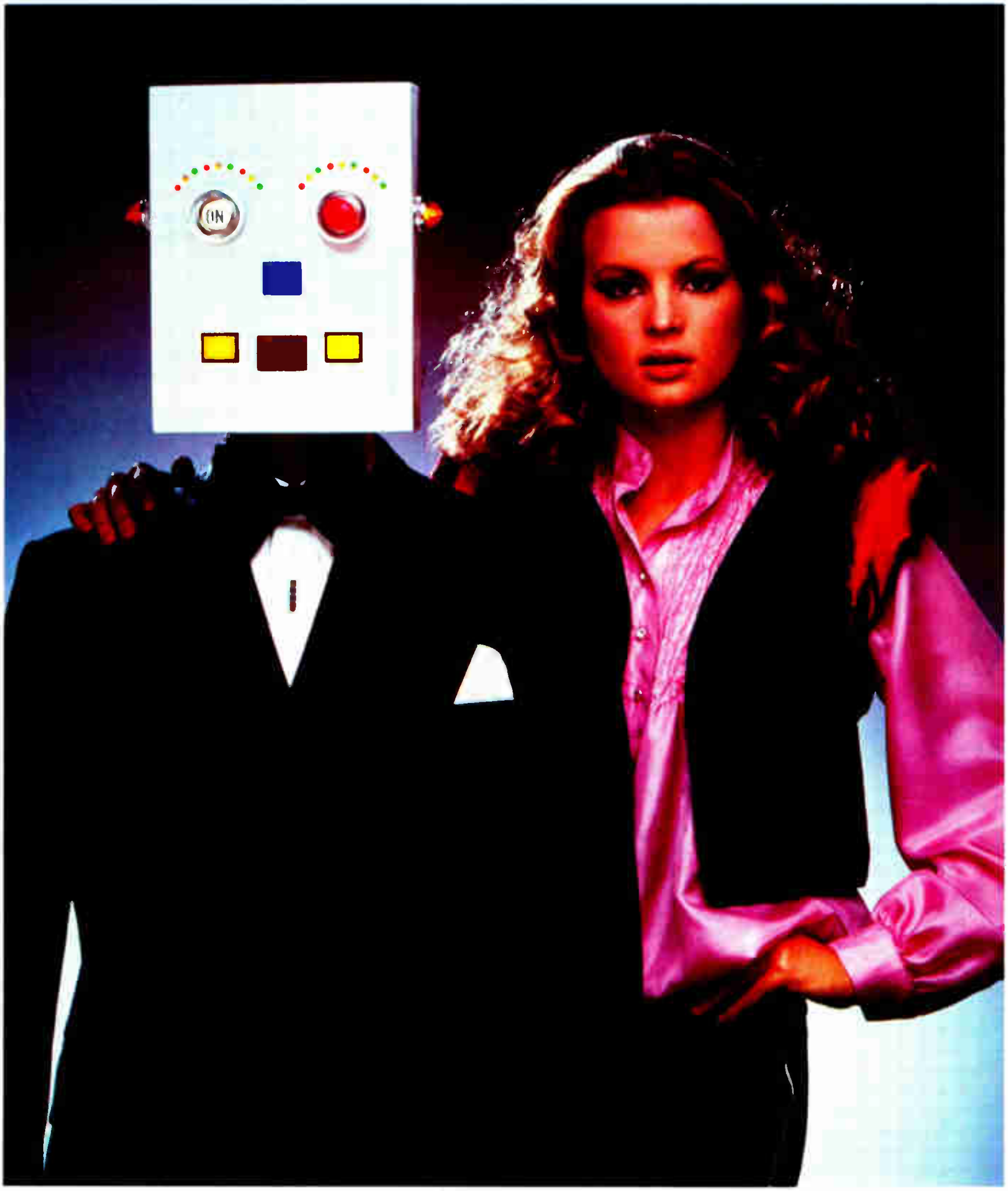

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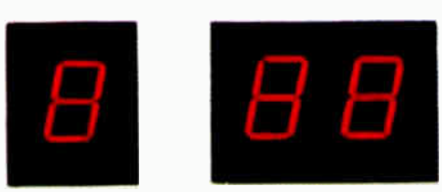

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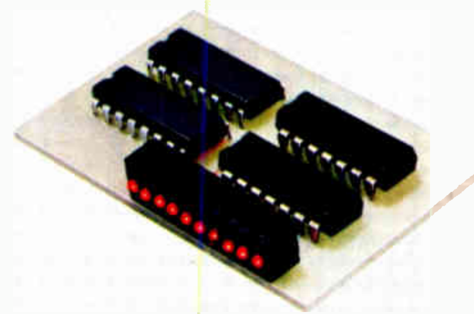

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| SA2210/SA2310 | 1.0 | 64 | X |
| S2215/S2315 | 1.5 | 96 | |
| SA2215/SA2315 | 1.5 | 96 | X |
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| SA2220/SA2320 | 2.0 | 128 | X |

Phoenix 1 comes with everything you need for program development: CRT, keyboard, 48K of RAM, 3 mini disk drives, 2 RS232C ports, AMIX™ operating system, screen-oriented editor and assemblers for the S2200 as well as AMI's S2000, S6800 and S9900. All for only $5495.

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Circle 75 on reader service card

# Aids for blind 'read' books, speak temperatures

*by John Gosch, Frankfurt bureau manager*

TV set add-on unit that turns teletext, viewdata information into braille is latest in series from West German firm

**Troubled by his** failure to find a reasonably priced braille-type calculator for his handicapped daughter, Lothar Limmer, an AEG-Telefunken engineer, persuaded his company to put one on the market three years ago. That was the first of the half dozen or so devices now being manufactured for the blind and visually handicapped at the West German firm's new technologies group in Wedel, near Hamburg.

Besides the table-top calculator with a braille output, various character-into-braille converters and readers are already on the market. A talking thermometer is among others to be introduced soon, points out Limmer, the project leader for such equipment at Wedel.

With such equipment, the Frankfurt-based firm has entered a market that by all indications—and quite unfortunately—is growing. Experts put the present number of blind people in West Germany alone at some 80,000 and see that number increasing at about 2% a year. In the U. S., they estimate, the number is around 437,000 and worldwide the estimate is for a staggering 42 million.

With its know-how in character recognition, speech synthesis, and the related software, AEG-Telefunken has advanced to a leading position as a producer of equipment for the blind. One character-detecting device is a reader that converts book pages or single sheets in any typeface into braille and is scheduled to hit the market in 1982.

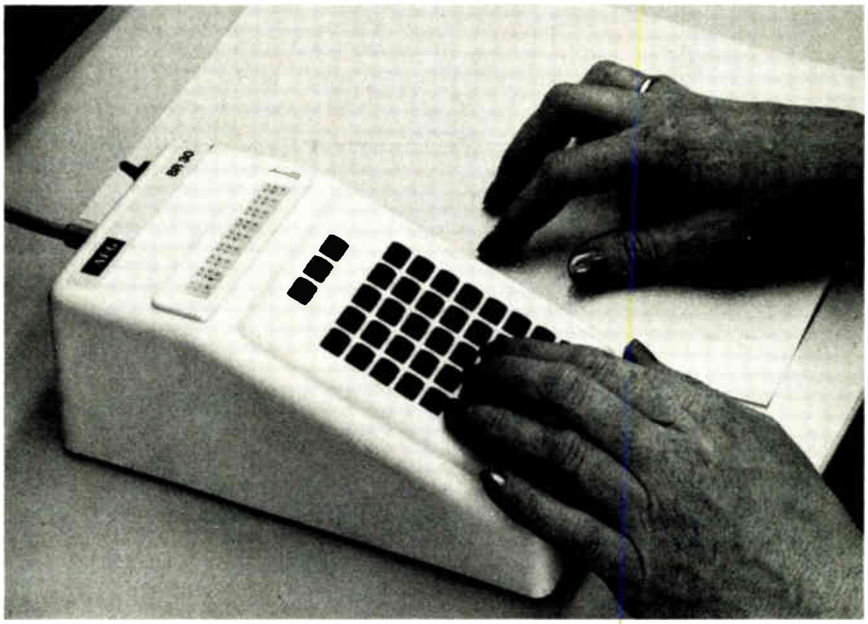
The page to be read is placed on the reader's scan window, and a special camera then scans the page character for character and line for line. The camera output is fed to pattern-recognition circuitry, where the characters are segmented, centered, normalized, and classified in a process similar to the one AEG-Telefunken uses in its mail-sorting and address-reading systems for West Germany's post office [*Electronics*, Dec. 21, 1978, p. 60].

A 40-digit braille line then appears on 40 field segments on a braille display. Electromechanically activated pins protrude through each segment so that the blind person can sense the braille configuration with his fingertips.

Limmer figures the reader will sell for about $11,000. Even so, he says, not only institutions for the blind but also private persons have expressed interest in it.

**TV, too.** Another piece of equipment from AEG-Telefunken's Wedel facilities converts viewdata and teletext information shown on a television screen into braille. An add-on unit interfaces with the TV set's viewdata or teletext decoder to produce braille on a display like that used with the reader. It will be made available to a selected group of blind people during viewdata trials this fall in Düsseldorf and West Berlin.

Instead of braille, synthetic speech is used in the TBS 80 thermometer, intended to measure body, room, and water temperature. When a button is



**Braille calculator.** Identifying keys by raised markings that indicate their figures or functions, blind person enters data from sheet at right, touches braille display for answers.

pushed on the handheld, battery-powered device, it announces the temperature measured in the form of tens, ones, decimal point, and tenths of a degree centigrade. The speech is produced by an integrated circuit from Telesensory Systems Inc. of Palo Alto, Calif.

The thermometer probe senses temperatures from 0° to 60°C. In the 0° to 42°C range, resolution is within 0.1°. When that range is exceeded or the 9-volt battery output falls below 4.5 volts, the probe says the word "error." The TBS 80 will be on sale for around $480 early next year.

Already available to the blind for performing mathematical operations is AEG-Telefunken's braille desktop calculator. The unit has keys with raised markings, and the calculated results appear on a row of nine braille display fields—one for the sign and eight for the figures—that take the place of a regular calculator's light-emitting diodes.

**Powerful.** Selling for about $890, the calculator has 47 functions, allowing the blind to solve even the complex technical-scientific problems engineers often encounter. A buzzing tone alerts the operator to conditions such as overflow and the like. A magnetic-tape cassette contains operating instructions and practice examples.

Another desktop calculator for the visually handicapped has an oversized LED display. The 2-centimeter-high figures are four times larger than those on a regular calculator. The display can be tilted for an optimum viewing angle, and a filter cuts down stray light from the environment.

## Japan

# New VLSI is focus of follow-on project

Japan's five major semiconductor manufacturers have been assessed $45 million by the VLSI Technology Research Association to pay the first year's costs of an industry-sponsored three-year very large-scale integration project, with the goal of developing the crystal technology, production technology, and new devices that will be needed for the nation's next generation of computers.

This new project, administered by the same association as the recently completed four-year government-sponsored VLSI project, is but a shadow of the earlier one. Mainly it aims to show compliance with the spirit of the government project's provisions that the companies pay back its subsidies during the eight years following. The first three of the eight years is a period of grace, though.

**Who's involved.** The five companies paying for the three-year follow-on are Nippon Electric Co., Toshiba Corp., Hitachi Ltd., Fujitsu Ltd., and Mitsubishi Electric Corp. Two other companies, which have no income from the sale of semiconductors, will participate in the research and thus also be recipients when the funds are distributed. They are NEC-Toshiba Information Systems Inc., a joint venture of the first two companies on the list, and Computer Development Laboratories, a joint venture of the last three. NTIS sells computers to Toshiba's mainframe customer base, but CDL is merely a paper company. Research and development by both of these joint ventures is carried out in specially designated areas in their parents' laboratories and plants.

The four-year government project ended March 31. During it, government subsidies amounted to about $135 million, while the companies spent another $180 million of their own. Its accomplishments included the development of electron-beam, X-ray, and optical lithography systems; inspection systems; and basic crystal research.

The new three-year project, which nominally began on April 1, the start of Japan's fiscal year, will concentrate on developing practical devices and their production technology. From the profits made on those device, the companies will be able to pay back the government during the five-year period extending from 1983 through 1987. **-Charles Cohen**

## Great Britain

# CCD imager fits 625-line TV systems

Closed-circuit and industrial television cameras using solid-state black and white imagers may emerge in Europe before next year, now that a British company has designed the first charge-coupled-device sensor capable of handling the 625-line systems standard there. The chip's U. S. and Japanese predecessors of course conform to the needs of the 525-line NTSC standard.

Developed by General Electric Co. Ltd.'s Hirst Research Centre in Wembley, Middlesex, the MA357 crams 220,000 elements into an area of 1 by 1.4 centimeters (394 by 552 mils). A monochrome prototype camera designed around it with no attempt at miniaturization occupies approximately 15 by 8 by 6 cm (5.9 by 3.1 by 2.4 in.), including power supply, uses 20 commercial packages, and consumes about 3 watts.

**New market.** To David J. Burt, who heads the CCD imager program in Wembley, the development seems likely to inaugurate a European market for solid-state imagers in industrial, professional, and military applications. The Hirst center is already supplying key customers with samples, and GEC is increasing capacity and upgrading its CCD line in advance of the expected demand. As the specification for the CCD imager was drawn up in collaboration with camera manufacturer and sister company Marconi Communications Ltd., the new part is likely to find its way into equipment before the end of the year.

In terms of complexity, according to Burt, the 385-by-576-element device bears direct comparison with Japanese and U. S. counterparts. Burt hopes to have out a color version in 1981, though at this stage it is still unclear whether a one-, two-, or three-chip configuration will provide the most economical solution.

The present device employs a three-level polysilicon-gate bur-

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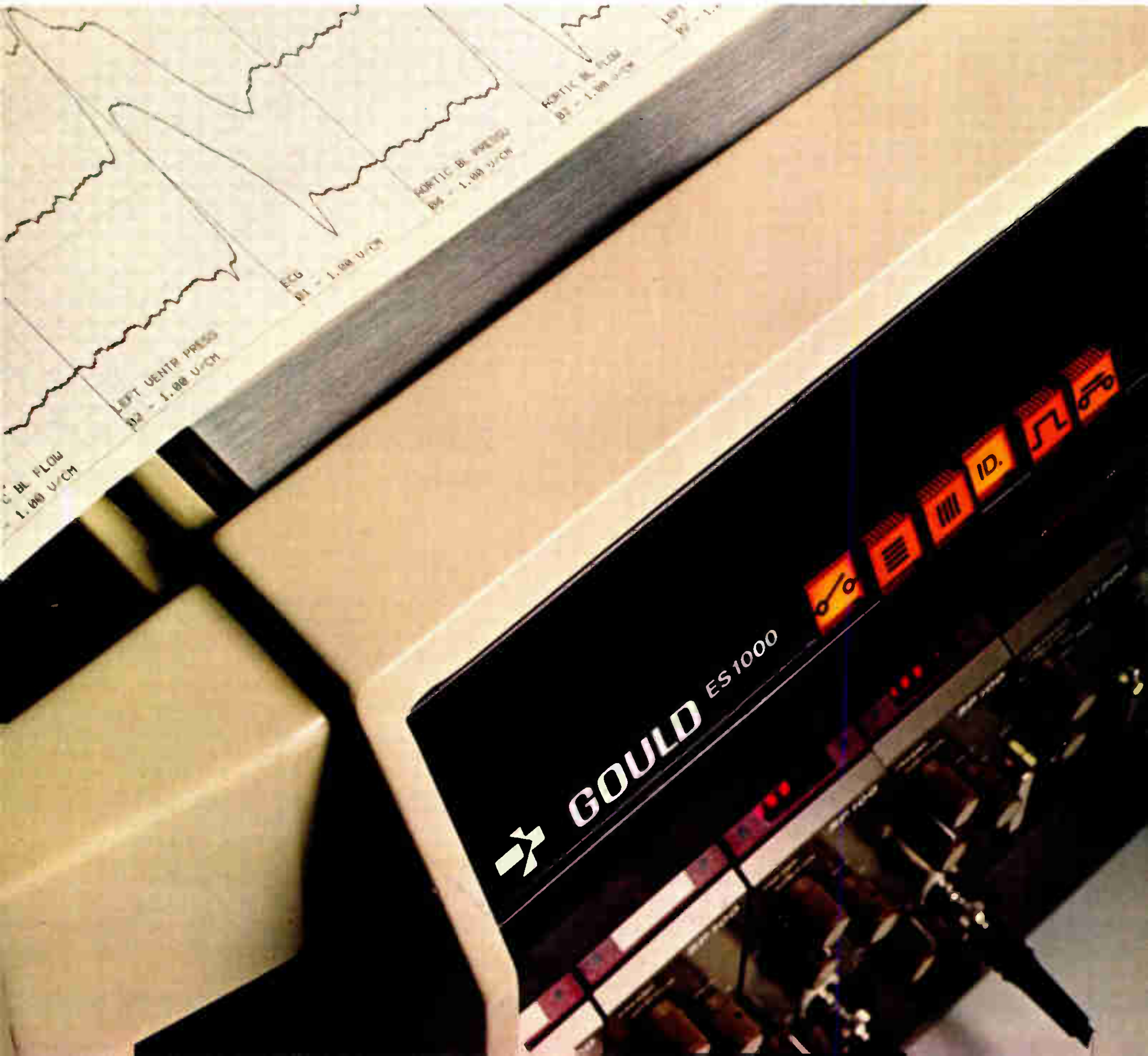
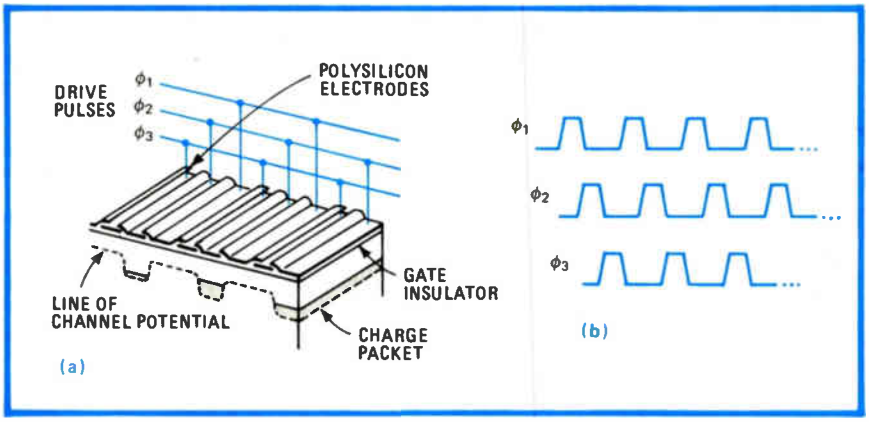





**Double.** CCD imager gets 576 lines out of 288-line frame by clocking out charge alternately from active electrode—$\phi_1$ in (a)—and from the other two, one of which is by then active (b).

ied–n-channel process. It operates in the frame-transfer mode and is split into an imager and a storage section with 864 horizontal electrodes. Image transfer from one section to the other takes place during the field-blanking period and is then read out a line at a time.

Because of the three-phase technique used to transfer packets of charge, the 864 horizontal lines actually produce a frame with 288 lines, or one third the number of electrodes. But by interlacing successive fields, the resulting horizontal resolution is twice that, or 576 lines. And since in a 625-line system 50 lines are used for the field-blanking period, the imager's 576-line output is directly compatible with European 625-line standards.

**Turn and turn about.** Interlacing is achieved by clocking out first the charge under every third electrode to generate one field and then the charge under the other two electrodes to generate the other field (see figure). In this way the center of charge collection is shifted up and down between fields to yield an effective 2:1 interlace. The number of columns employed—385—was chosen to give equal horizontal and vertical resolutions—about 67% of a TV studio broadcast camera tube. To match the tube, Burt believes the group will have to move from its present 8-micrometer geometries to 5-μm geometries.

But still other problems have to be overcome before the CCD imager can match the studio tube. For instance, when the device is illuminated above peak white, an excess of carriers is generated and spreads to adjacent picture elements. In fact, the group has demonstrated experimental structures incorporating diffused drains in the image section. These in turn, operating like the overflow pipe of a domestic bath, permit highlights to be presented at 100 to 1,000 times peak white before spreading occurs.

According to Burt, these structures will be incorporated at a later date, despite their need to steal real estate from the sensitive area. His group is also working to improve the optical response of the device, particularly in the blue sector, to make possible the design of a color camera. **-Kevin Smith**

## Japan

# Low-power RAM uses SOS, silicides

Cache memories for the next generation of computers may use complementary-MOS devices with metal silicide gates fabricated on silicon-on-sapphire wafers. A prototype 4-K-by-1-bit static random-access memory built at the semiconductor device engineering laboratory of Toshiba Corp. has a typical access time of 20 nanoseconds with a power dissipation of only 250 milliwatts when operating from a single 5-volt power supply.

In comparison, a 4-K RAM built with Intel Corp.'s HMOS II process typically dissipates twice the power (500 mW) to achieve much the same access time (22 ns) [*Electronics*, Sept. 13, 1979, p. 124].

The new design features a negligible standby power drain without incurring the additional chip-select time typical of n-channel MOS devices operated in a power-down mode. Moreover, tests indicate that the lower resistance of the silicide word lines reduces the propagation delay and thus access time by about 6 ns compared with similar RAMs using polysilicon word lines.

The basic SOS process will also be used to fabricate microprocessors. But polysilicon gates will then be used because long connections in these chips are made using aluminum rather than the gate material, as in memories.

**Solutions.** By using enhancement-mode field-effect transistors in conjunction with double ion implantation under molybdenum silicide gates, the device succeeds in eliminating problems that have plagued earlier SOS devices, including anomalous drain currents and poor control of threshold voltage. Enhancement design, together with deep boron implantation in the n-channel transistors and deep phosphorus implantation in the p-channel transistors, eliminates current flow in the portion of the epitaxial layer close to the sapphire. This cuts off the leakage that would otherwise occur in this region, which has a high defect density.

Shallow phosphorus implantation in the n-channel transistors and shallow boron implantation in the p-channel transistors sets the threshold value in these devices. The high work function of the molybdenum silicide gates—about 0.5 to 0.8 V above that of polysilicon gates—biases both the n and p transistors off and thus makes it simple to adjust the thresholds with the shallow implants.

**Foundation.** The starting material for the devices is a 0.7-micrometer epitaxial layer of high-resistivity n-type silicon on sapphire. Gate oxide is 500 angstroms thick. The

molybdenum silicide films are then deposited on the gate oxide using a magnetron-type sputtering apparatus. The target is made of hot-pressed molybdenum silicide, and the process is carried out at room temperature in argon at a pressure of 3.5[3] torr. The silicide film typically has a thickness of 2,200 Å. Its sheet resistivity after being annealed for 30 minutes at 1,000°C is 3.5 ohms per square, about one tenth that of polysilicon.

The silicide film after annealing is polycrystalline, with a grain size of about 2,000 Å. This is finer than the grain size of polysilicon and makes it easy to fabricate fine-pattern devices designed to 2-$\mu$m rules. Photolithography and dry etching are used to define the silicide gates and word lines. The effective channel length in these devices is 1.5 $\mu$m, which is large enough for devices operated from a 5-V power supply despite short-channel effects.

The cell size for this RAM is 36 by 36 $\mu$m (14 by 14 mils) and chip size is 3.23 by 4.19 millimeters (127 by 165 mils). -Charles Cohen

## West Germany

# Universally applicable technique linearizes microwave power amp tubes

Regardless of its input-versus-output characteristics, any microwave power amplifier tube can be linearized by a method developed by a research team at the University of Stuttgart's Institute of Radio Frequency Technology. Based on a new amplitude- and phase-predistortion technique, the method also allows linearization over virtually the whole output power range of a tube, points out Alois Egger, director of the institute and head of the team.

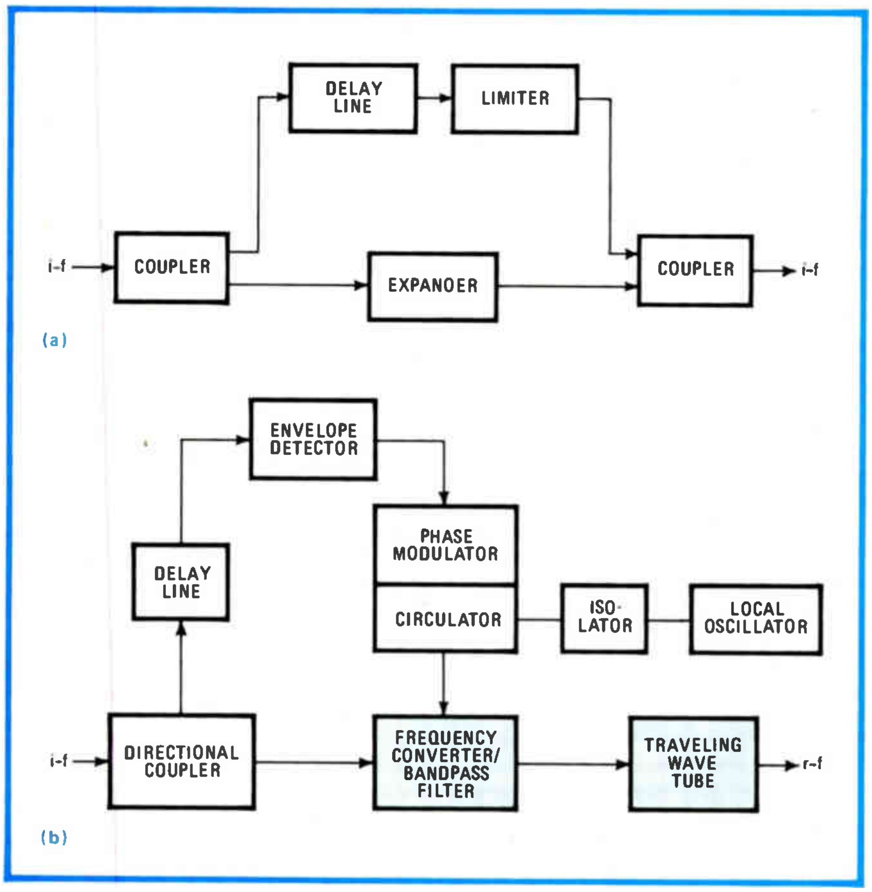
A subject of discussion at the Sept. 8–12 Tenth European Microwave Conference in Warsaw, the method is claimed to be superior to other predistortion linearization schemes, which must be tailored to specific tubes. What's more, the Stuttgart method linearizes the characteristics of, for example, a 20-watts power tube up to 16 W or so, whereas the others are limited to at most 14 W or so.

**Radio and TV.** Supported by the German Research Society, the work at the institute is being done with a view toward future cable distribution networks that are to give West Germans additional radio and television programs. These programs, some to be transmitted to communications satellites and picked up at suitable ground terminals, will be fed to the cable networks over microwave links operating at 2 and 11 gigahertz.

The links will use single-sideband, amplitude-modulated transmissions to pack into a 105-megahertz band either seven TV channels, including sound, or five TV channels together with a number of radio programs. It is for possible use in the 11-GHz SSB/a-m transmitters that Egger and co-workers Manfred Horn and Vietnamese-born Tong Vien have devised their linearization method.

To ensure distortionless multichannel SSB transmissions, the transmitter's power amplifiers and frequency converters must exhibit a very high linearity. Up to 1 GHz, the familiar negative feedback technique can achieve such linearity, but in the 11-GHz range, when a traveling-wave tube is used, it fails because of the delay the TWT would contribute to the feedback loop. The best way to obtain linearization, then, is by using the predistortion technique, Egger says.

In the transmitter, the SSB input signals are first converted into the




**Two steps.** New predistortion technique for input signal's amplitude (a) and phase (b) can linearize the output of any microwave power amplifier tube.

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105-MHz intermediate-frequency band extending from 650 to 755 MHz. A frequency converter then transforms the i-f band into the 11-GHz radio frequency range. Finally a TWT boosts the signal amplitude to the required output level.

Nonlinearities are due to a tube's gain compression and relative phase shift between its output and input signals. Assuming that a 20-W TWT must be linearized up to a peak envelope power of around 16 W, then its corresponding input power must be raised (or "distorted") by more than 5 decibels and the input signal must be made to have a leading phase. By using these predistortion principles, the output becomes an ideally amplified replica of the input. In short, linearization is obtained.

Egger's method carries out the predistortion of the input's amplitude and phase in separate circuits (see figure). The gain compression in the TWT and the frequency converter is compensated with a nonlinear network exhibiting a gain expansion that is the inverse of the tube's gain compression.

In principle, such compensation could be achieved with a diode network by varying the diodes' bias. But a better way, according to Egger, is to use a bridge circuit with a gain expander—functionally the opposite of a compressor—in one branch and a network with compression characteristics—a limiter, for example—in the other. This circuit, designed for the i-f band, is diagrammed in (a) on page 82. It can be precisely tuned and improves the amplitude linearity of the complete transmitter—that is, of its i-f amplifier, frequency converter, and TWT.

For phase linearization, the necessary leading phase is achieved with the circuit shown in (b). After the amplitude predistortion process, a part of the i-f signal is shunted off, amplified, and detected by the envelope detector.

**Change.** The voltage obtained drives a phase modulator that changes the phase of the local oscillator signal and hence the phase of the rf signal at the output of the frequency converter. **-John Gosch**

## France

# 'Quasi-topological' OCR approach has more than 80% success with handwriting

An optical-character-recognition system capable of distinguishing between nonstandard, handwritten characters at least 80% of the time has reached the prototype stage at France's central government telecommunications laboratory, the Centre National d'Etudes des Télécommunications. But internal politics and labor problems at the French postal and telecommunications authority have halted its further evolution there into a commercial product, and Morton Nadler, the American expatriate largely responsible for its development so far, wants someone else to pick up where the CNET left off.

Originally conceived to read postal codes, the system could also be adapted to industrial recognition applications like robot vision, notes Nadler, a free-lance consultant working out of his home in the Paris suburb of La Celle Saint-Cloud. Using an unconstrained randomly selected data base of 8,000 characters, taken from actual letters handled by the French mail, the system identified over 80% correctly and 5% incorrectly, rejected 4% as unreadable, and was unable to decide on a further 7% to 8%.

"The system needs to be perfected," admits Nadler, adding quickly that it is still the only OCR system known to him that can distinguish between the numerals 9 and 8 with the lower loop unclosed.

**Vertical raster scan.** At the heart of the system is a structural, or what Nadler calls a "quasi-topological," pattern analysis, done though a vertical raster scan, with pairs of adjacent columns scanned simultaneously from top to bottom and successively from right to left. At the CNET, the work was carried out on a scanner with a 2,000-photodiode array, with a resolution of 5.6 points per millimeter.

Significant changes in contrast between pairs of points in the adjacent columns are measured along four axes—vertical, horizontal, and two diagonals. This four-way comparison provides the data primitives necessary for calculating the eight quasi-topological codes, or QTCs, used to map the structure of the pattern to be recognized. The scanner data is fed into a preprocessor for code generation, with code processing handled by a computer—the CNET worked with a Hewlett-Packard 9640, but Nadler thinks a battery of microprocessors would do.

**Contrast.** A change in contrast from light to dark in the left column, while the right column stays light, indicates the start of a pattern. If the same data results from the following pair of points scanned, then the two dark points in the left-hand column are arranged vertically, and a vertical QTC is generated. Similarly, a change from dark to light in the left-hand column, while the right-hand column continues to read dark, results in a finish QTC. A change from dark to light along both columns at the same time generates not only a finish QTC, but also a horizontal QTC. Contrast changes along the two diagonals indicate convexity and concavity.

Although Nadler suggests 8- to 10-points/mm resolution for more accuracy, he says that even at 5.6 points/mm, quasi-topological analysis can recognize about three quarters of any random group of patterns. For example, a single vertical stroke, even if tilted somewhat, is readily recognized as the numeral 1. For recognition of more complex patterns, especially those where different writing styles can cause confusion, Nadler supplements structural analysis with a comparison of the relative positions of specific points on a character. **-Kenneth Dreyfack**

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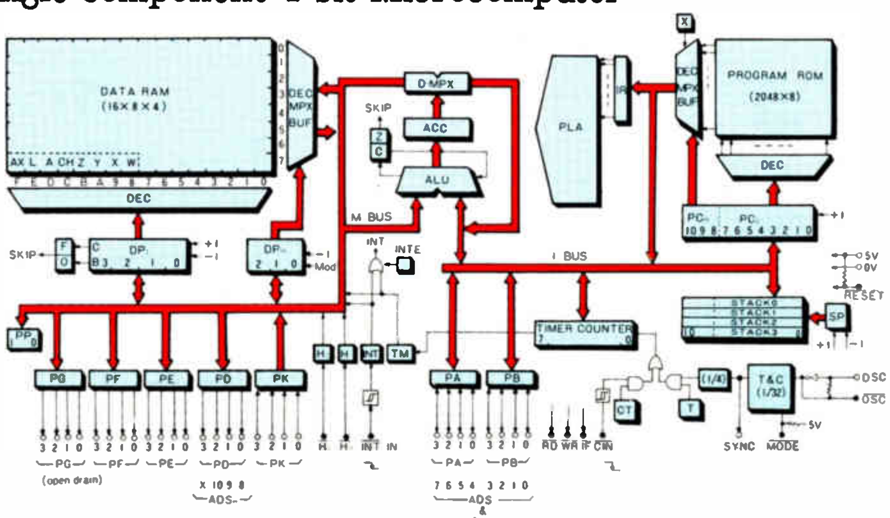


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| MPB 202 | MPB202 Users Manual |
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| MPSP-C | SDP40-C Users Manual |
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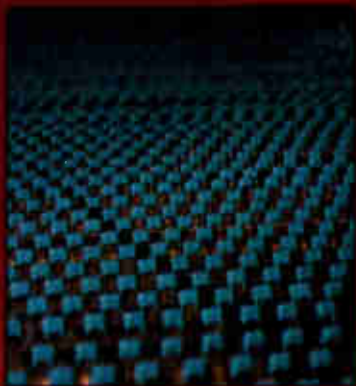

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# Artificial intelligence: on the brink

New conference features first industrial applications of the concept and spurs predictions of rosy future

*by Martin Marshall, West Coast Computers & Instruments Editor*

**Man has** yet to fathom the depths of his own intelligence, but he has already begun to transfer the lower workings of that intelligence into his machinery. To describe this transfer of methods, reactions, interactions, and assimilations into metal, silicon, and plastic, researchers have adopted the term "artificial intelligence" for overlapping subsets called expert systems, knowledge representations, inference schemes, program synthesis, scene analysis, and robotics.

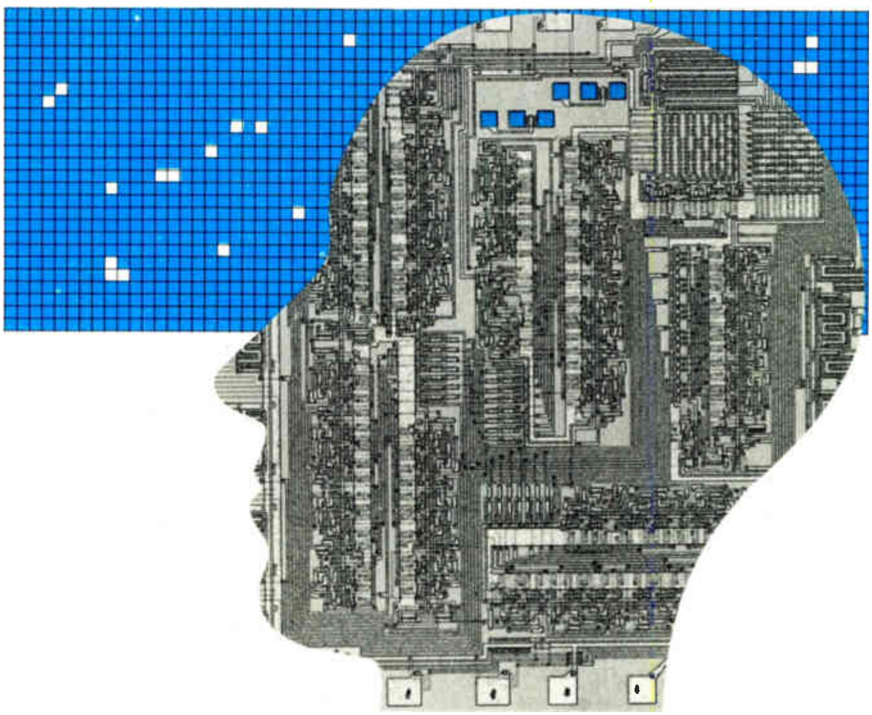
For 15 years, this small but rapidly growing body of researchers, based in the universities, has been developing concepts and theories about artificial intelligence, but now their work has begun to leak out into real-world applications. Giants of the electronics industries are beginning to develop programs employing their techniques, as are small specialty companies spun off from the academic community.

One sign of the industrialization of artificial intelligence appeared last month at the first annual National Conference on Artificial Intelligence, held at Stanford University in Palo Alto, Calif., where for the first time industrial applications were exhibited. The conference, sponsored by the newly formed American Association for Artificial Intelligence, was not the first ever held to discuss the concept, but it differed significantly from its predecessors in that it reflected strong industry involvement.

Aside from a number of panels describing developments at universities, the conference also featured reports of efforts in industry, including those of such giants as Hewlett-Packard, Texas Instruments, and Schlumberger, as well as smaller specialty firms. HP has not yet offered equipment using artificial intelligence, notes Egon Loebner, manager of the data-base management department of HP's Computer Resources Laboratory, but it is preparing them. "There are three departments where we are applying AI research, including voice recognition and generation, providing a better environment for programmers, and in data-base management systems," he observes.

The HP programming effort, Loebner notes, includes "a very impressive set of software tools that give the programmer more power to do his job." Other sources added that the HP effort includes an interactive, autoprogramming system that allows the programmer to use very powerful "primitives" to assemble a program. Loebner confirmed that in his area of data-base management systems, HP is developing a quasi-natural language along the lines of the California Institute of Technology's Rapidly Extendable Language (REL) and Stanford's First Order Language (FOL).

**TI in business.** After a somewhat rocky start, efforts at Dallas-based Texas Instruments Inc. now involve more than 20 persons, with plans for rapid expansion. As a measure of its commitment, TI's manager of artificial intelligence research, Mark Miller, quotes TI vice president George Heilmeyer as saying, "We are in the AI business." To back up



his statement, Miller points to TI's development of the Entice programming environment for its future personal computer system. Entice, which stands for Easy-to-use Novice-Oriented TI Computing Environment, will be used on computers developed for the mid-1980s and beyond.

Miller will not discuss details of Entice, but he does indicate the areas of computer research in which TI expects to make breakthroughs. "TI's involvement in speech I/O is well known, but you can also look for a very intelligent 'help' system on the computers, interactive color graphics, and new kinds of 'pointing devices' that will provide alternatives to keyboard design," he notes.

TI is also investigating the use of natural languages, for the development of robust parsing algorithms, as well as of a restricted natural-language system. "We want to choose a subset of English that optimizes intelligibility to both the user and the machine," Miller says.

Other work at TI is focused on developing expert systems for the design of very large-scale integrated circuits, as well as establishing a microprocessor architecture that is suited for artificial intelligence work. "The VLSI design project is just getting under way," notes Miller. "As for the microprocessor architecture for AI, it will include a large address space and such things as tag architectures."

**First steps.** At Schlumberger Ltd., the commitment to artificial intelligence research comes straight from the top. As Schlumberger chairman and president Jean Riboud puts it: "We have hardly begun to understand what this abundant and cheap intellectual power will do to our lives. It has already started to change physically the research laboratories and the manufacturing plants. It is difficult for the mind to grasp the ultimate consequences [of artificial intelligence] for man and society."

Schlumberger's representative at the conference, David Barstow, the program leader for software research at Schlumberger-Doll Research in Ridgefield, Conn., indicates that the conglomerate is involved in a number of projects. With a primary emphasis on equipment for oil exploration, he notes, Schlumberger is putting much of its research money into the development of expert systems. The company is also involved in programs for automated design, automatic programming, robotics, deductive planning, and interactive environments. To expand its research capabilities—and to recruit personnel from the artificial intelligence community concentrated on the San Francisco Peninsula—Schlumberger will establish a new artificial intelligence center this fall, to be housed at one of the Silicon Valley facilities of its Fairchild Camera and Instrument Corp. subsidiary in Mountain View.

**Finding work.** Between the theoretical concerns of the universities and the long-range projects of the electronics giants, the field is also spawning a number of small companies specializing in applications. One such is Machine Intelligence Inc. in Mountain View, whose president, Charles Rosen, asserts: "Almost any infusion of intelligence represents a great step up over present manufacturing machinery. Almost without exception, the machines used to manufacture automobiles in Detroit are deaf, dumb, and blind."

Rosen's firm develops, among other artificial intelligence products, "simple" vision systems for robotics applications. "Simple vision is a large subset of scene analysis that lends itself to computer analysis. Binary vision [reduction to pure black or pure white shades] is particularly useful, because it dispenses with the computing complexity involved in gray-scale analysis." Machine intelligence is also involved in developing expert systems at every level of manufacturing, as well as in work on language understanding by computers.

Another small company, Automatix Inc. of Burlington, Mass., sees robotics from a software viewpoint. "While most AI companies have been heavy-equipment manufacturers, Automatix has approached it from an information-systems orientation," observes company president Vic Scheinman. Scheinman, who developed an early robotics system called the Stanford Arm, now sees robots as terminals connected to a host computer system.

**Put it together.** In spite of the delineation of the different components that researchers use, artificial intelligence still seems to be the total combination of machinery, monitoring systems, and software that makes a useful, intelligent product. Thus, the distinction between knowledge-based systems, expert systems, and robotics blur when the research ends. □

## IBM's Epistle reads the mail

How about a machine that reads the mail, understands it, digests it, informs, the recipient of its important parts, and even writes replies on routine matters? Well, it will be at least five years before such an electronic secretary shows up as a product, but International Business Machines Corp.'s Epistle, a system for the automatic analysis of business correspondence, is intended to do just that.

Epistle, which stands for Executive/Principal's Intelligent System for Text and Linguistic Endeavors, was described at the National Conference on Artifical Intelligence by Lance A. Miller, the manager of behavioral science and linguistics at IBM's Thomas J. Watson Research Center in Yorktown Heights, N. Y. As Miller sees it, applications of the Epistle software will include the synopsis and abstraction of incoming mail and a variety of critiques of newly generated letters, all based on the capability of the software to understand a natural-language text.

It will combine such aspects of AI research as semantic representations, parsing, meaning assignment, text interpretation, adaption, abstraction, and critique—each performed by the software. The specific processes will relate to a set of "typical" business letters that are in the Epistle data base. When a letter is read, the planned system will provide surface syntactic parses for each sentence, interpret the meaning of each adjusted to the context of prior sentences, and synopsize the overall meaning of the letter. **-M. M.**

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## Ohio Scientific's New OEM Program

Ohio Scientific now recognizes the importance of the OEM marketplace and is introducing a complete program for the board level OEM user as well as the system OEM. The program starts with our standard products including three CPU boards, a broad range of static and dynamic memory boards, mini and 8″ floppy disk controllers, printer controllers, multiple RS-232 port boards, a hard disk controller, and video interface with optional keyboard. Backplanes with two, four, eight or sixteen slots are available. These standard products are now being supplemented by a broad range of products specifically for the OEM user including:

- New universal telephone interface board which has auto-dial capability, auto-answer capability, tone encoding and decoding, answer and originate 300 baud modem and voice I/O via tape recorder or optional phonetic voice output system.
- New calendar-clock with several month battery backup capability which can be programmed to automatically restart the computer or shut off the computer at set times. The circuit board also includes automatic power-fail restart capability.
- Instrumentation quality high speed, 12-bit analog A/D – D/A module with a 16-channel input multiplexer and two 12-bit D/A converters.
- A large range of parallel interface options including circuit cards containing 48 parallel I/O lines.
- New solderless prototyping board which connects to the computer system and allows rapid prototyping of new interface ideas.
- System PROM blaster which accepts 8K through 64K bit industry standard EPROMS and a universal EPROM-ROM card.
- A card edge extender, bus analyzer and bus compatible breadboards.

## Documentation

All of Ohio Scientific major circuit boards are now fully documented by Howard Sams (the originator of the Sams Photofact series for Consumer Electronics) servicing manuals which include block diagrams, schematics, detailed pictorials, parts placement diagrams and parts lists providing the designer, systems integrater and serviceman with detailed hardware information. Ohio Scientific is offering qualified OEM users its principal disk operating system (OS-63D V3.2) which supports multiple languages, mini-floppies, 8″ floppies, printers, modems and other accessories in documented Source Code and machine readable form which can be reassembled on standard OSI computers. This gives the product developer the ultimate flexibility in integrating these components into his total system design.

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Because of Ohio Scientific's hundreds of thousands of boards per year volume for the consumer and small business market, these products cost a mere fraction of the corresponding LSI-11, SBC or S-100 bus boards. This economy allows you to utilize a floppy subsystem in your product at a total cost typically less than an EPROM based system from other vendors.

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Electronics abroad

# German consumer firms face bad times

## Japanese goods reducing economic miracle of 1950s to fond memory as only big-screen TV sets are unthreatened — for now

by John Gosch, Frankfurt bureau manager

**West Germany's entertainment** electronics producers are facing a crisis widely regarded as the biggest since the country performed its economic miracle in the 1950s and early 1960s. Behind it is the fierce and unrelenting competition from the Far East, particularly Japan, which has made some fear that the entertainment equipment market may become as heavily Far East–dominated as that for motorcycles, cameras, and pocket calculators.

At least in one area, that assessment may be a bit too pessimistic. The production of large-screen color television sets, which accounted for more than 40% of West Germany's $4 billion consumer electronics equipment market last year, is still firmly in domestic hands. Also testifying to the industry's strength in that sector is the large export volume: of the 3.3 million color sets made in 1978, more than a million were sold abroad. But even there a cloud hangs over the horizon: by the mid-1980s, when all PAL color-TV patents have expired, the Japanese are certain to start pecking away at Germany's big-screen market.

The manufacture of other products, however, either has been completely wiped out or is hurting considerably. For example, portable radio sets are no longer made in West Germany and neither are portable black and white receivers and cassette recorders. And few radio recorder combinations are produced, though—like cassette recorders—they were originally developed in Europe.

**Hi fi, VCRs too.** Still other product sectors are reeling. An estimated 40% of domestic high-fidelity equipment sales are made by producers in the Far East, and 8 out of 10 video cassette recorders sold in the country come from Japan.

On top of the losses of market segments and sales shares comes another development: the acquisition of West German equipment makers by powerful foreign firms. Only recently, France's Thomson-Brandt SA took over Saba Werke GmbH [*Electronics*, April 10, p. 63]—after Nordmende KG the second German TV producer to wind up in Thomson's fold. Such acquisitions are a bitter pill to swallow, but most observers feel that a "European solution" to a company's financial problems is better than a Japanese takeover of the company.

These woes are a hard blow to the industry's pride. For many years, sales of TV sets and audio equipment outpaced those in telecommunications and industrial electronics, for example. Consumer hardware makers consistently gobbled up about half of domestic components production and provided much business even for foreign parts producers.

Technologically, too, the entertainment industry established standards of excellence or came up with notable firsts. One example is AEG Telefunken's TED radio disk system [*Electronics*, Aug. 3, 1970, p. 127]. Though it never became a market reality, it did point the way to a new medium for video information.

Acting as official spokesman for

**Endangered species.** Jobs of 100,000 workers at West German entertainment electronics plants are threatened by Japanese imports, says ZVEI, an industry trade association.

the 100,000-employee entertainment electronics industry is West Germany's Central Association of the Electrotechnical Industry (ZVEI). In a report issued earlier this year, the Frankfurt-based ZVEI analyzes the industry's problems, points an accusing finger at the Far East, notably Japanese manufacturers, and clamors for measures to dampen the Far East export offensive.

The ZVEI talks of an "acute threat to the entertainment sector's innovative and competitive stance, job security, and economic future," a threat resulting from several negative factors: the industry's wages are among the world's highest; the numerous revaluations of the West German Deutschmark in recent years have made imports cheaper and exports more expensive; and the domestic market is the world's most liberal, amounting to a free-for-all for competitors from everywhere.

Excellent engineering, ever better product quality, and high productivity have not prevented Germany's position in entertainment electronics from deteriorating during the past decade, the report says. It adds that with many markets in Europe and elsewhere being regulated via orderly marketing policies or import restrictions, foreign producers are concentrating more and more on Germany's open market. "This has already caused irreparable damage to the electronics industry, damage that equipment makers and components producers have to bear."

To support its complaints about marketing practices by Far Eastern producers, the ZVEI points out that while 37% of West Germany's total imports of entertainment electronics products came from Japan in 1978, that country accounted for only 0.0003% of West Germany's total exports of such products that year.

Mindful of the nation's own big exports of entertainment products, the ZVEI is not demanding that the Bonn government close its borders to Far Eastern imports. Neither does it want to regain lost ground via high import duties. What the association is seeking, however, is government help through some sort of orderly marketing agreement and in getting the Japanese to "rethink their restrictive import policies."

The Japanese, of course, have not let the ZVEI charges go unrebutted. In a sharply worded reply, the Düsseldorf office of the Electronic Industries Association of Japan (EIA-J) flatly states that the "difficulties the German consumer electronics industry is facing are not mainly due to Japanese competition," but to a number of other factors. One is that the industry has not spent heavily enough on research and development and new production technologies to stay competitive.

The West German industry, the EIA-J maintains, "has long enjoyed a quasi-monopoly market position in

## Companies report bad news

The West German entertainment electronics industry's crisis, stemming from Far Eastern competition and being aggravated by a slump in consumer spending, is claiming a heavy toll. Hardly a week goes by without some company reporting a disquieting event. NV Philips Gloeilampenfabrieken, Europe's biggest consumer electronics maker with strong activities in West Germany, reports a decrease in profits in various sectors, including home video and audio. This, the Dutch company says, is "mainly due to losses in the manufacturing sector and to pressure on the selling price of important product categories."

Grundig AG, West Germany's No. 1 in entertainment equipment, recently announced some sharply curtailed operations. Following the news that it would close its 1,000-employee factor in Ireland (where it makes dictating machines and cassette-recorder–radio combinations) comes word that the company will shut down a car radio parts plant near Munich by the end of this year. Many other firms that make such products, among them Telefunken GmbH, Blaupunkt-Werke GmbH, and the ITT Consumer Products Group, have already curtailed production through plant shutdowns or shorter work weeks or are about to do so.

**-J. G.**

the most lucrative consumer electronics fields, namely color TV, which is still protected from Japanese competition thanks to the PAL patents." While the Germans were milking that field and doing little to open up new ones, "the Japanese established hi-fi equipment and video cassette recorder markets."

**Easy out.** Another factor responsible for its ills, the Japanese say, is that the German industry did not try to create new employment at home but, like the U.S., chose the easy way out by moving production to low-labor areas and by having equipment made by foreign manufacturers to supplement its own product range. Instead, the German industry should have made "audacious investments in new technologies and combined the technologies with its engineering capability and highly skillful labor force." Only lately is the German industry following the Japanese example and investing more in automation, the EIA-J says.

The charge that their market for entertainment products is closed to foreigners is unfounded, the Japanese contend. "Rather, it is open to all who try hard enough to go after it." But they ask how hard and how long the West German consumer electronics industry has tried to enter foreign markets. Japanese success in foreign markets, they say, "is simply a result of long-term efforts to understand local consumers' needs and to supply reliable products."

Thus far, the Bonn government has done little more than lend a sympathetic ear to the complaints of the country's entertainment electronics industry. And judging by recent statements by high government officials, it is unlikely that Bonn will readily advocate import controls for fear that they could boomerang.

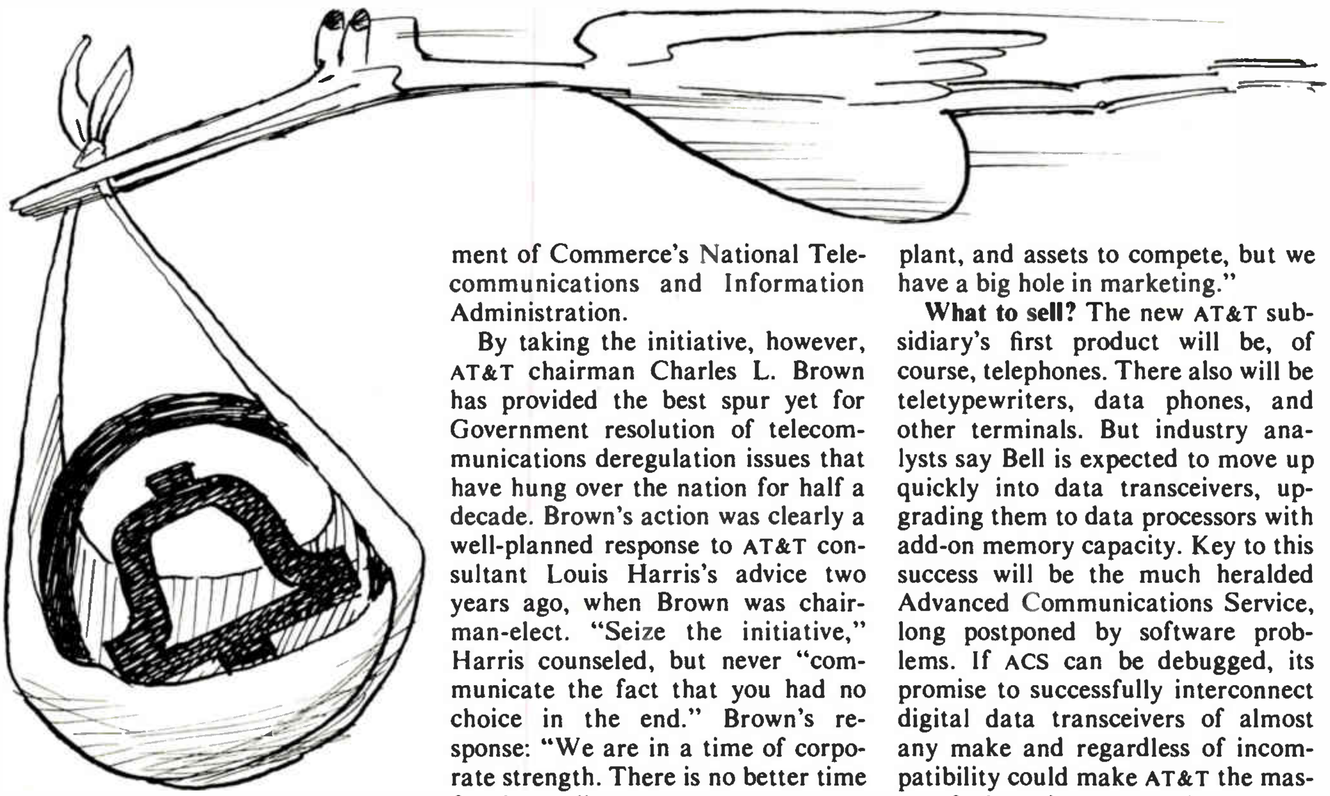
Like Japan, West Germany is one of the world's biggest exporting countries, with one out of four jobs dependent on foreign sales. About half of its automobile production goes abroad, as does a substantial share of its output of machine tools, chemical products, electrical equipment, and other industrial goods. Under these circumstances, the Bonn government can hardly endorse restrictions on imports from its trading partners in the Far East. ☐

Communications

# For AT&T, hard part is still to come

Now that it has announced the birth of its subsidiary for unregulated businesses, details must be added and approved

*by Ray Connolly, Washington bureau manager, and Harvey J. Hindin, Communications & Microwave Editor*



**The hardest parts**—the details—are yet to come for American Telephone & Telegraph Co. now that it has lifted the curtain on plans to compete in deregulated markets through a fully separate subsidiary [*Electronics*, Aug. 28, p. 59].

Before Bell's plans for its research, development, manufacturing, and marketing structure can be accepted, it faces political as well as technological challenges. One challenge is that new Federal legislation will be interpreted by such administrative bodies as the Federal Communications Commission, the Department of Justice, and the Department of Commerce's National Telecommunications and Information Administration.

By taking the initiative, however, AT&T chairman Charles L. Brown has provided the best spur yet for Government resolution of telecommunications deregulation issues that have hung over the nation for half a decade. Brown's action was clearly a well-planned response to AT&T consultant Louis Harris's advice two years ago, when Brown was chairman-elect. "Seize the initiative," Harris counseled, but never "communicate the fact that you had no choice in the end." Brown's response: "We are in a time of corporate strength. There is no better time for change."

As AT&T gears up for next year's new congressional battle to restructure the FCC and deregulate most telecommunications except basic telephone service, Bell System insiders say there are a host of internal problems to resolve as well. Vice chairman James E. Olson, new head of what has been dubbed the FSS (fully separated subsidiary) that will incorporate a new AT&T international unit to compete overseas, "can be expected to begin heavy recruiting of good marketing talent from competitors soon," says one corporate insider. That source contends, "We have the best technology and engineers, plant, and assets to compete, but we have a big hole in marketing."

**What to sell?** The new AT&T subsidiary's first product will be, of course, telephones. There also will be teletypewriters, data phones, and other terminals. But industry analysts say Bell is expected to move up quickly into data transceivers, upgrading them to data processors with add-on memory capacity. Key to this success will be the much heralded Advanced Communications Service, long postponed by software problems. If ACS can be debugged, its promise to successfully interconnect digital data transceivers of almost any make and regardless of incompatibility could make AT&T the master of a booming new market.

If successful, ACS could seriously undermine market opportunities for the IBM-backed Satellite Business Systems, which is set to begin operations next year after its first satellite launch this fall. Another potential loser would be Telenet, the special data-services carrier now owned by General Telephone & Electronics Corp.

AT&T clearly sees opportunities to compete also in the coming electronic mail market with the new call-answering-and-forwarding service—a store-and-forward service it is now trying out through its Pennsylvania Bell operating company. This is real-

ly a form of electronic mail, with the sender specifying phone numbers, the message, and the delivery time. As a service for both the home and office, it could compete with the U. S. Postal Service and other specialized forms of electronic mail.

**Video test.** AT&T has also been testing the waters of the videotext business with an eye to offering such products. To do this a selected group of customers in Albany, N. Y., has been hooked up to an electronic information service. This is simply a video access—connected by telephone lines, of course—to Bell's computers for directory information, weather, time, and sports updates.

No Yellow Pages or classified ads are being supplied with the Albany test, although AT&T is expecting to offer such services in the future, much to the dismay of newspaper publishers as well as cable televison operators who are also interested. CATV may be added to the alphabet soup list of industries that opposes Bell's entry into their businesses.

Finally, Bell's new FSS may take over its cellular mobile telephone service for highway vehicles. This service has been tested in Chicago, and Bell, happy with the results, wants to pursue the issue. But among other problems, there are numerous private communications companies moving into this new business and FCC rules restrict the number of separate services that can be available in one geographic area. These rules are being challenged.

**Big baby.** AT&T says it is pushing for a single conglomerate for all of its deregulated home and business product sales—a giant that could have beginning assets of $18 billion, competitors say, and initial annual revenues of $10 billion or more. The prospect that this will lead to unfair competition scares them, as they have indicated in a sharp letter to White House assistant Stuart E. Eizenstat dealing with the pending rewrite of the 1934 Communications Act. The seven industry organizations signing the letter faulted the National Telecommunications and Information Administration's failure to support legislative amendments

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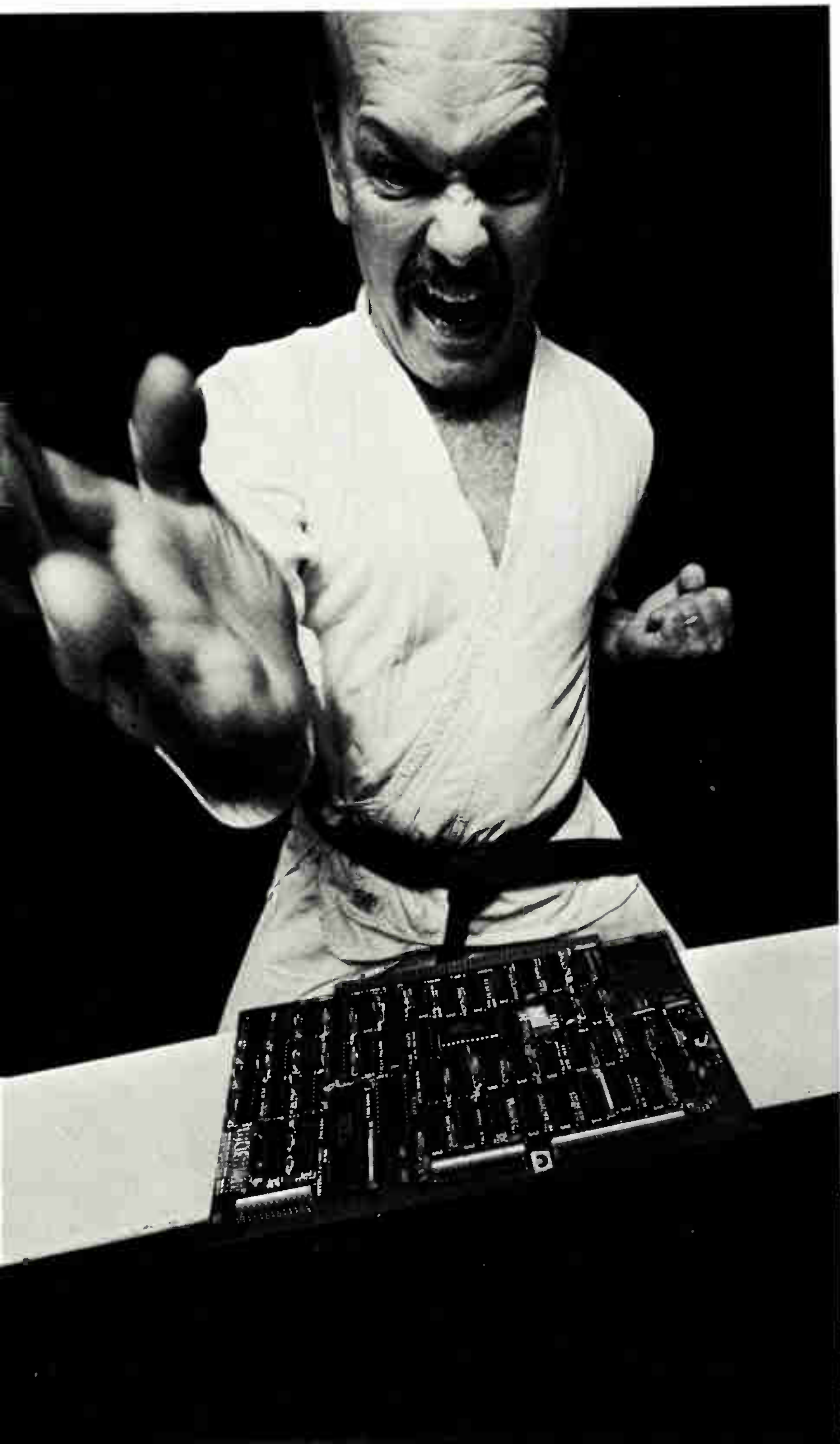

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they believe are required for fair competition, which must:

- Give the FCC flexibility to control AT&T, including policing of cross-subsidies between regulated and unregulated entities.
- Prevent AT&T's creation of a conglomerate subsidiary with initial annual revenues of $10 billion to $20 billion "with unbridled opportunities in cross-subsidies internally."
- Require the AT&T subsidiary to be fully responsible for its own basic research and development, limit its ability to buy subassemblies and components from its parent, and prevent joint ventures with the joint use of property and joint institutional advertising programs.
- Control the "immense financial advantages available to the subsidiary in comparison with its competitors," including "at least a 2% difference in the cost of borrowing . . . and enormous tax benefits made available to regulated utilities" but not to competitors.

Signing the letter--which the White House calls "full of inaccuracies"—were the Ad Hoc Committee for Competitive Telecommunications, the Computer and Communications Industry Association, Datapoint Corp., MCI Telecommunications Corp., the North American Telephone Association, the Association of Data Processing Service Organizations, and the Independent Data Communications Manufacturers Association.

AT&T has a distinct time advantage as its competitors, the White House, the Congress, Federal agencies, and the courts continue to haggle over details of new legislation. For example, chairman Lionel van Deerlin of the House Commerce communications subcommittee wants to know if the new FSS "will handle only marketing," as required by the FCC's Computer Inquiry II ruling, "or will it have independent research and manufacturing that pending reform, H. R. 6121, orders?" AT&T says it has not made that decision yet, indicating that it is ready to negotiate hard to limit any corporate changes to those that best serve its interests. □

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Solid state

# HP vetoes advanced SOS process

But company emphasizes commitment to the technology, using metal-gate fabrication with 3-to-4-$\mu$m features

*by Bruce LeBoss, San Francisco regional bureau manager*

**Becoming less bullish** about the prospects of silicon-on-sapphire technology, Hewlett-Packard Co. has backed off from further developing SOS 2, its third-generation process. But the Palo Alto, Calif.–based computers and instruments manufacturer is charging ahead with an earlier process, SOS 1.5, with which it expects to build most, if not all, SOS circuits for at least another decade.

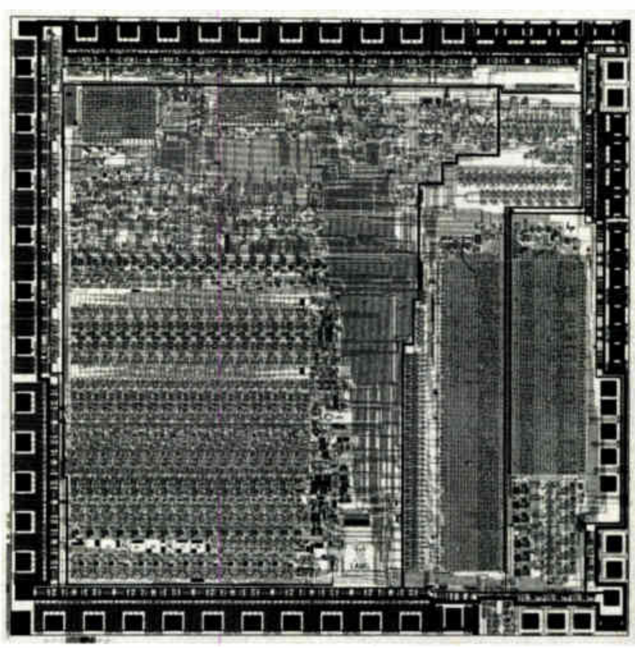
The management at HP's Technical Computer group concluded recently that SOS's earlier advantages over other MOS technologies will not be as pronounced for fabricating devices with smaller geometries as they are for those with larger ones. What's more, though management is optimistic about resolving technical problems that remain, SOS yields continue low, primarily due to leakage. However, the decision "not to pursue development of the third-generation process at this time is for business—not technological—reasons," states Paul C. Greene, general manager of HP's Cupertino, Calif., integrated-circuit operation.

SOS 2 is a polysilicon-gate complementary-MOS-on-sapphire process with 2.5-to-3-micrometer features. There are a number of reasons for halting its development, not the least of which is the fact that "we don't want to be supporting too many process developments, especially when you consider that market conditions are softening," he states.

But perhaps the most significant factor in the decision, Greene points out, is that the IC operation has now "made the transition from a mostly research-and-development facility producing small volumes into a large-volume manufacturing operation more concerned with costs, yield projections, and designing for manufacturability."

Also, because of the increased capital investment required to start operating an IC process, "we can't afford to have a whole bunch of IC operations," each supporting its own division, notes Douglas C. Chance, general manager of the Technical Computer group.

"In general, there were no major technical problems associated with SOS 2," Greene states. "We made good, if not great, technical progress with it and the old leakage problem was greatly reduced." Much of the development work on the SOS 2 engineering effort, he adds, is directly applicable to SOS 1.5, a second-generation aluminum-gate process with 3-to-4-$\mu$m features, as well as to one that HP calls n-channel MOS C. The latter is a new workhorse process that is expected to be better at meeting the requirements, in terms of good design turnaround and modest cost, of HP's terminals, peripherals, and low-cost computers.



**HP SOS.** One of the latest Hewlett-Packard chips is this 16-bit CPU with 2 K by 8 bits of on-board ROM for the HP 1000 series.

**Evolutionary steps.** "Over the next five years, we will be investing a sizable amount of money in SOS process development to enhance the technology," Greene says. Rather than making step-function, revolutionary changes, he stresses, "we will incorporate unit steps into the existing manufacturing process."

Though some semiconductor manufacturers are dropping efforts to develop standard SOS circuits, or are emphasizing other processes, HP is increasing its SOS circuit development activity. "SOS will continue to make a contribution for many years where very high performance with low power dissipation is needed," says Chance.

At present, HP is using SOS to build many 16-bit microprocessors, as well as bus-controlled chips for the HP-IB (IEEE-488) in-

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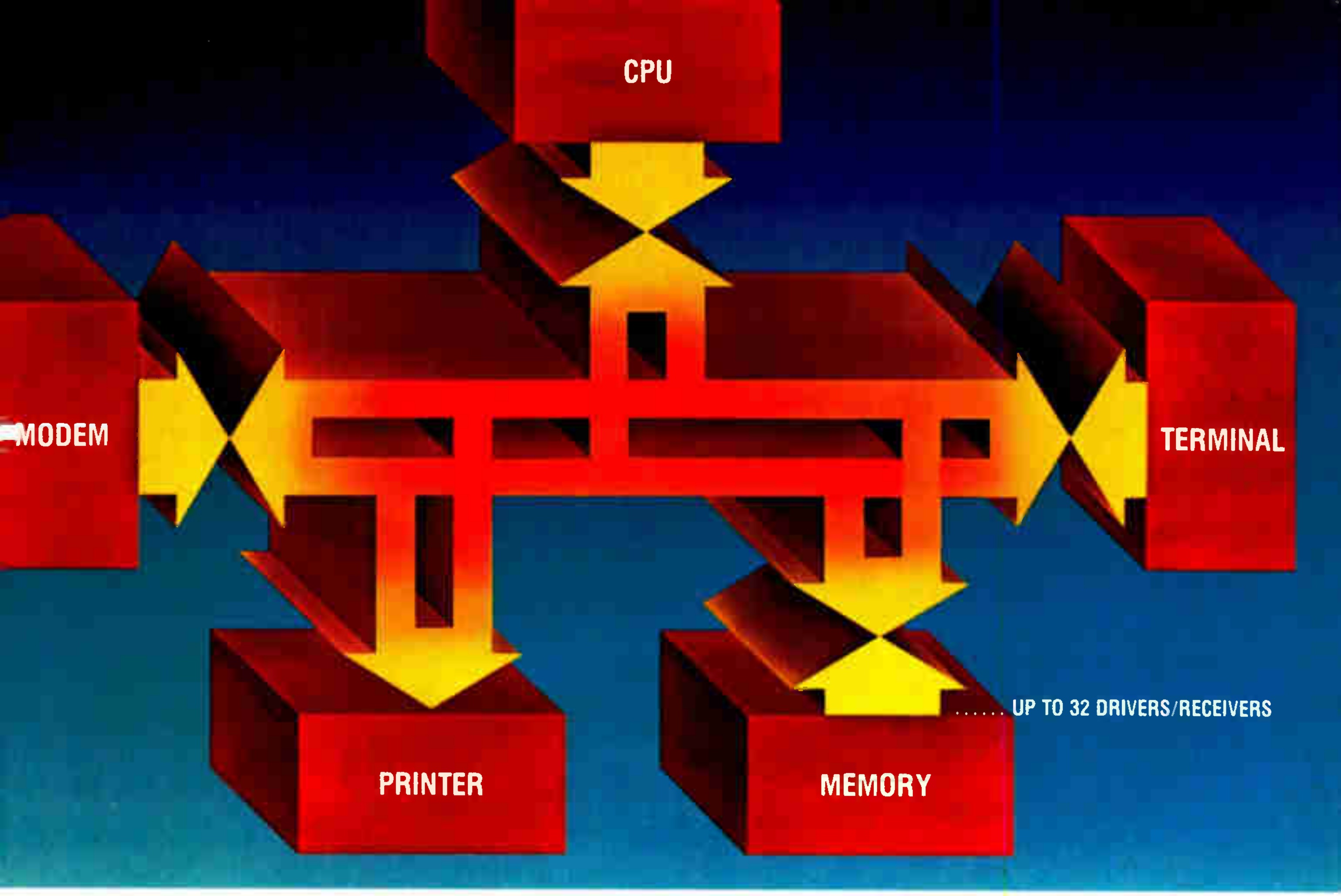
terface bus and other communications chips. Greene claims they outperform what is on the market commercially. One of the firm's biggest SOS chips, a logic device, is contained in its new 2626A terminal [*Electronics*, July 31, p. 130]. It also plans to continue developing higher-density and higher-speed SOS memories, beyond the 2-K RAM and 32-K read-only memory already developed. One is a 128-K ROM.

**Varied routes.** Even as HP continues to lead the parade of manufacturers pursuing SOS for commercial applications, the enthusiasm of some devotees is waning.

EFCIS (Société pour l'Etude et la Fabrication de Circuits Intégrés Speciaux), the French MOS manufacturer jointly owned by Thomson-CSF and the French Atomic Energy Agency, says it has all but dropped its efforts to develop standard SOS parts. The firm's market strategists estimate that substrate costs will keep them from being competitive.

Recently, RCA Corp.'s Solid State division in Somerville, N. J., disclosed it was partially deemphasizing its SOS efforts for commodity parts and adopting a dual-technology approach that would include a new bulk-silicon C-MOS process as well [*Electronics*, July 31, p. 82; Aug. 14, p. 8]. Meanwhile, Rockwell International Corp.'s Microelectronics division in Anaheim, Calif., perhaps most active in building SOS circuits for military applications, has yet to set a timetable to move the technology into the commercial market.

**Japan's views.** The outlook in Japan is cloudy. Toshiba Ltd. says it is ready to start sales of a C-MOS-on-sapphire microprocessor and static random-access memory next year. "These will be high-performance devices that cannot be built without using SOS," claims Yoshio Nishi, manager of MOS device technology at Toshiba's semiconductor device laboratory. Less optimistic is Fujitsu Ltd., which has made 1-K and 4-K SOS memories that were no faster than bulk silicon devices. Fujitsu researchers say they do not think SOS will be used for memories in the future. □

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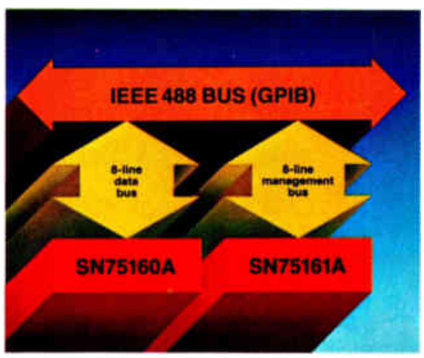


**PARAMETER CHART**

| PARAMETER | | SN75160 | SN75160A |
|---|---|---|---|
| MAX POWER (mW) | UNLOADED<br>LOADED | 761<br>953 | 525<br>717 |
| MAX SPEED (ns) | DRIVER<br>RECEIVER | 35<br>50 | 25<br>20 |
| DRIVER $I_{OL}$ (mA) | | 48 | 48 |
| MAXIMUM SPEED—POWER PRODUCT (pJ) UNLOADED | | 38050 | 13125 |

**CURRENT AND TEMPERATURE CHART**

| | | |
|---|---|---|
| MAX SUPPLY CURRENT (mA) | 145 | 100 |
| OPERATING FREE-AIR TEMPERATURE RANGE (°C) | 0-70 | 0-70 |

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82172

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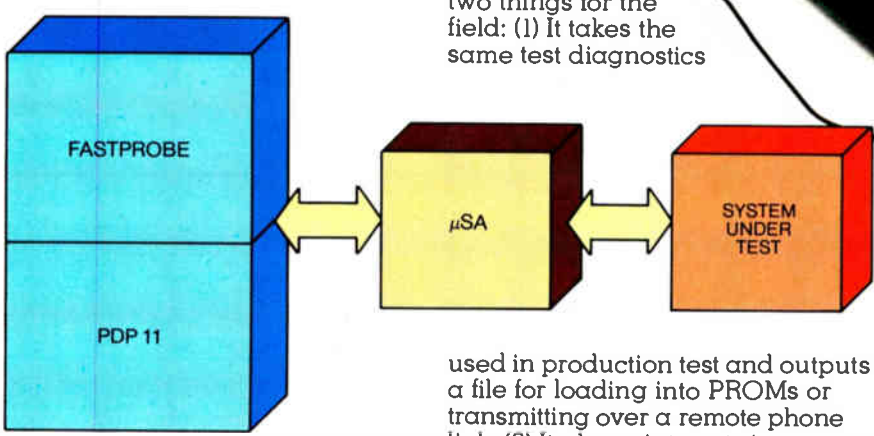


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**THOMSON-CSF is an international leader in the fast-paced telecommunications industry. They've found Tektronix 8002A emulation and support keeps their projects on schedule.**

Jean-Luc Gerner
System Engineer
THOMSON-CSF
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**"Emulation is the quickest, and we think the only way to debug microprocessor designs."**

At Thomson-CSF microprocessor designs have to move quickly from concept to marketplace. That's why engineers like Jean-Luc Gerner prefer the emulation capabilities of the Tektronix 8002A. Says Mr. Gerner: "On paper emulation is supposed to be the same. But we've used other development systems and their emulation has crashed. Tektronix emulation works consistently." The 8002A's three progressive stages of emulation provide a fast, simplified approach to microprocessor hardware and software integration.

With software development and debug, software/hardware integration, and prototype monitoring emulation modes, Thomson-CSF hardware and software engineers are able to use the same design tool to make changes and corrections right on the spot. "The time saving is incredible," adds Mr. Gerner.

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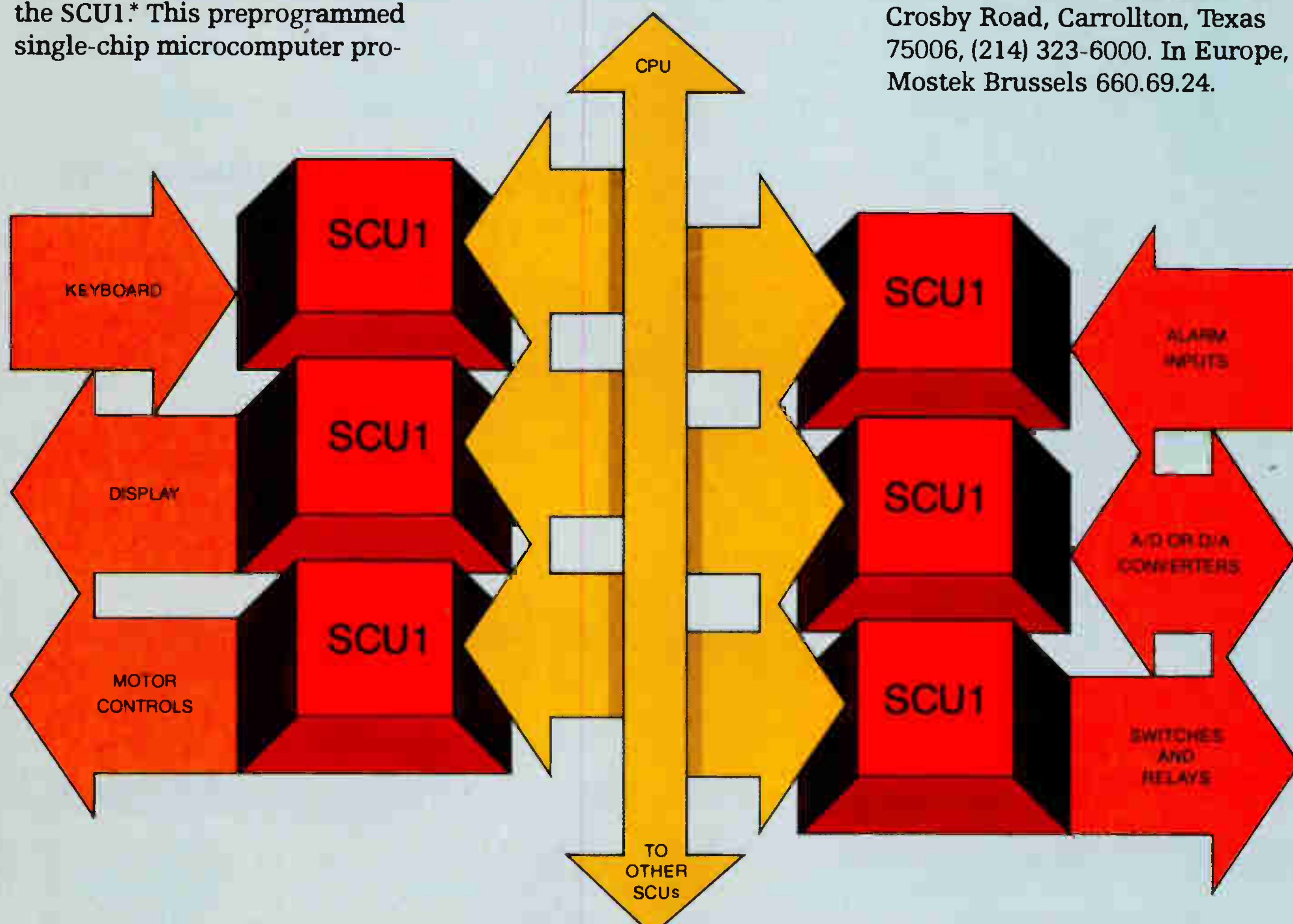





Circle 116 on reader service card

Technical articles

# 16-K static RAM takes new route to high speed

Novel circuit techniques instead of brute-force scaling achieve 30-ns, 375-mW typical performance; redundant bits and single-polysilicon process make part easy to build

by Rahul Sud and Kim C. Hardee, *Inmos Corp., Colorado Springs, Colo.*

□ A very fast 16-K static random-access memory is proof that producibility need not be sacrificed to high performance. Brute-force scaling is not used. Instead, new circuit techniques overcome the classic problems in static RAMs and allow the use of novel asynchronous bootstrap circuits, which help the chip attain a typical access time of 30 nanoseconds despite its highly manufacturable single-polysilicon process.

Until now, scaling of transistor channel lengths down to 2 micrometers has been used to produce MOS static RAMs with speeds that rival those of bipolar memories. However, process control problems associated with these tighter geometries have made the parts difficult to manufacture. The necessity for multiple threshold-adjusting implants and dual levels of polysilicon has made these MOS processes as complicated as complementary-MOS and bipolar technologies.

Departing markedly from conventional design approaches, the IMS1400 is a fully asynchronous 16-K-by-1-bit RAM fabricated with a 2.7-$\mu$m single-polysilicon process that uses one type each of enhancement- and depletion-mode n-channel devices and no zero threshold transistors (see Table 1). The problems of threshold variation, punchthrough, and subthreshold current asso-

**TABLE 1: COMPARING THE IMS1400's PROCESS WITH HMOS II**

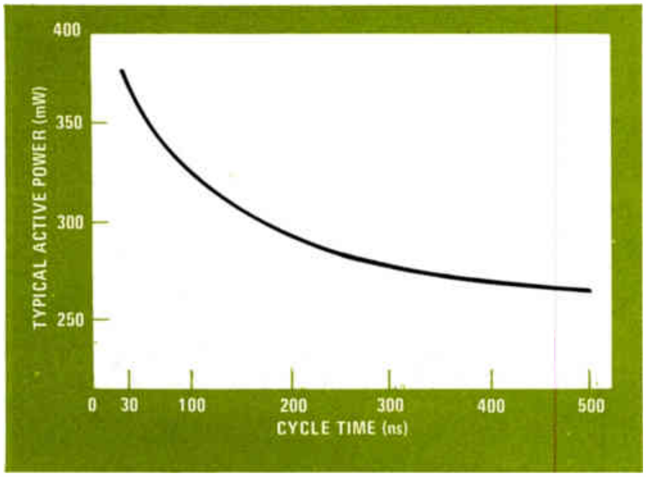
| Process parameter | HMOS II | IMS1400 |
|---|---|---|
| Channel length | 2 μm | 2.7 μm |
| Gate-oxide thickness | 400 Å | 500 Å |
| Number of polysilicon layers | 2 | 1 |
| Number of transistor thresholds | 4 | 2 |
| Zero-threshold transistors | yes | no |

SOURCE: INMOS CORP. AND INTEL CORP.

**TABLE 2: COMPARING TYPICAL PERFORMANCE CHARACTERISTICS OF 16-K STATIC RAMs**

| Specification | Intel 2167 | Inmos IMS1400 |
|---|---|---|
| Address access time (ns) | 40 | 30 |
| Chip-enable access time (ns) | 40 | 35 |
| Cycle time (ns) | 40 | 30 |
| Active power dissipation (mW) | 500 | 375 |
| Standby power dissipation (mW) | 75 | 35 |

SOURCE: INMOS CORP. AND ISSCC DIGEST 1979




**1. Reduced power.** The IMS1400 dissipates typically just 375 milliwatts during active operation and only 35 mW during standby. A unique circuit design, quite unlike that of conventional static RAMs, automatically reduces its power requirements at longer cycle times.

ciated with short-channel transistors are avoided, because relatively conservative channel lengths are used.

Nor is very fast operation the only outcome of the innovative circuit design. The memory dissipates typically no more than 375 milliwatts of active power and just 35 mW during standby (Table 2). In fact, unlike conventional static RAMs, it actually needs less active power with longer cycle times (Fig. 1).

## Direct stepping on wafer

Direct wafer stepping is used for all critical photolithographic operations, allowing a registration tolerance of better than ±0.5 μm to be achieved in production. Ion implantation is used for threshold adjustment and resistor value control and to dope the source and drain regions. Plasma etching is used extensively throughout, especially where dimensional control is critical. Proximity printing is employed for noncritical photoresist levels, and phosphorus diffusion is used to selectively dope polycrystalline silicon for low-resistance areas.

The chip's architecture is illustrated in the die photograph of Fig. 2. The row decoders split the 128-by-128-bit memory array in half. The column decoders are at one end of the array, and adjacent to them are the column-address buffers, control circuits, substrate bias generator, and sense amplifiers. Located at the other end of the chip are row-address buffers and bit-line equilibration and precharge circuits. The memory contains two spare columns, one on each side of the row decoder array, so that partially defective chips may be repaired electrically during wafer probing.

Housed in a standard 20-pin 300-mil-wide package, the IMS1400 has a pinout that is a simple extension of the 2147 4-K static RAM's. All inputs and the output have direct TTL compatibility. The RAM requires a single 5-volt (±10%) power supply; an on-chip bias generator supplies a negative voltage to the substrate. The memory has equal access and cycle times, and a chip-enable ($\overline{CE}$) pin is provided that, when taken high, puts the chip in its low-power standby mode.

## Single poly will do

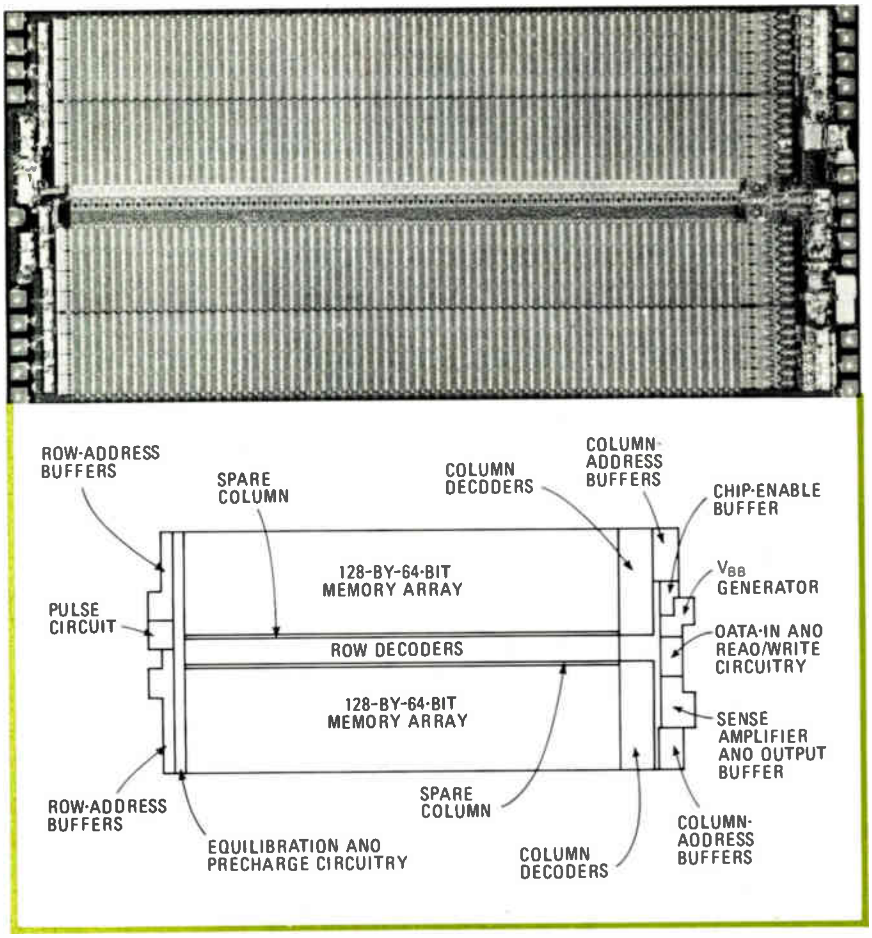
Over the years, efforts to reduce cell size and power dissipation have taken static RAM cells from saturated enhancement loads to depletion loads and now to polysilicon resistor loads. Further reductions in cell size were realized either with an extra level of polysilicon or by connecting the load resistors to a bit line [*Electronics*, July 20, 1978, p. 39; Sept. 27, 1979, p. 131].

Both techniques have limitations. The double-polysilicon approach suffers from reduced wafer yields because of the extra interconnection level and its associated buried contacts. Also, the increased vertical dimensions that result from a double-polysilicon process, together with the reduced lateral dimensions, adversely affect step coverage and high-resolution resist processing.

Connecting the load resistors to one of the bit lines does eliminate the $V_{cc}$ line in the memory cell but at the same time severely complicates internal circuit timing and the associated peripheral logic. Even with this trick, cell size remains significantly larger than in the double-polysilicon cell configurations.

The IMS1400 has a unique layout that implements the cell with a single level of polysilicon while keeping it comparable in size to a double-polysilicon structure with the same layout rules. The cell size is 1.07 mil$^2$ (689 μm$^2$), which is smaller than any previously disclosed double-polysilicon cell. This results in a chip size of just 30,950 mil$^2$ (19.9 mm$^2$).

The memory cell uses the familiar cross-coupled flip-flop with four transistors and a pair of polysilicon load resistors that are tied to $V_{cc}$. The $V_{cc}$ and the word lines are formed in polysilicon. The aluminum bit lines run vertically through the array, as in other static RAM designs. However, the key to the IMS1400's small cell size is to use polysilicon for $V_{cc}$ and an $n^+$ diffusion for the ground or $V_{ss}$ line.




**2. Speed with yield.** The memory is made with a highly manufacturable 2.7-μm single-polysilicon process. Row decoders split the 128-by-128-bit array in half. A spare column on either side allows partially defective chips to be repaired during wafer testing.

The load resistors are conservative in length to eliminate problems resulting from lateral diffusion of the dopant in the polysilicon. The 2.7-μm transistor channel lengths minimize subthreshold currents, allowing very high-resistance loads to be used in the cell. This, in turn, provides for reliable operation of the cell while reducing the power requirements of the memory array.

**Why wait?**

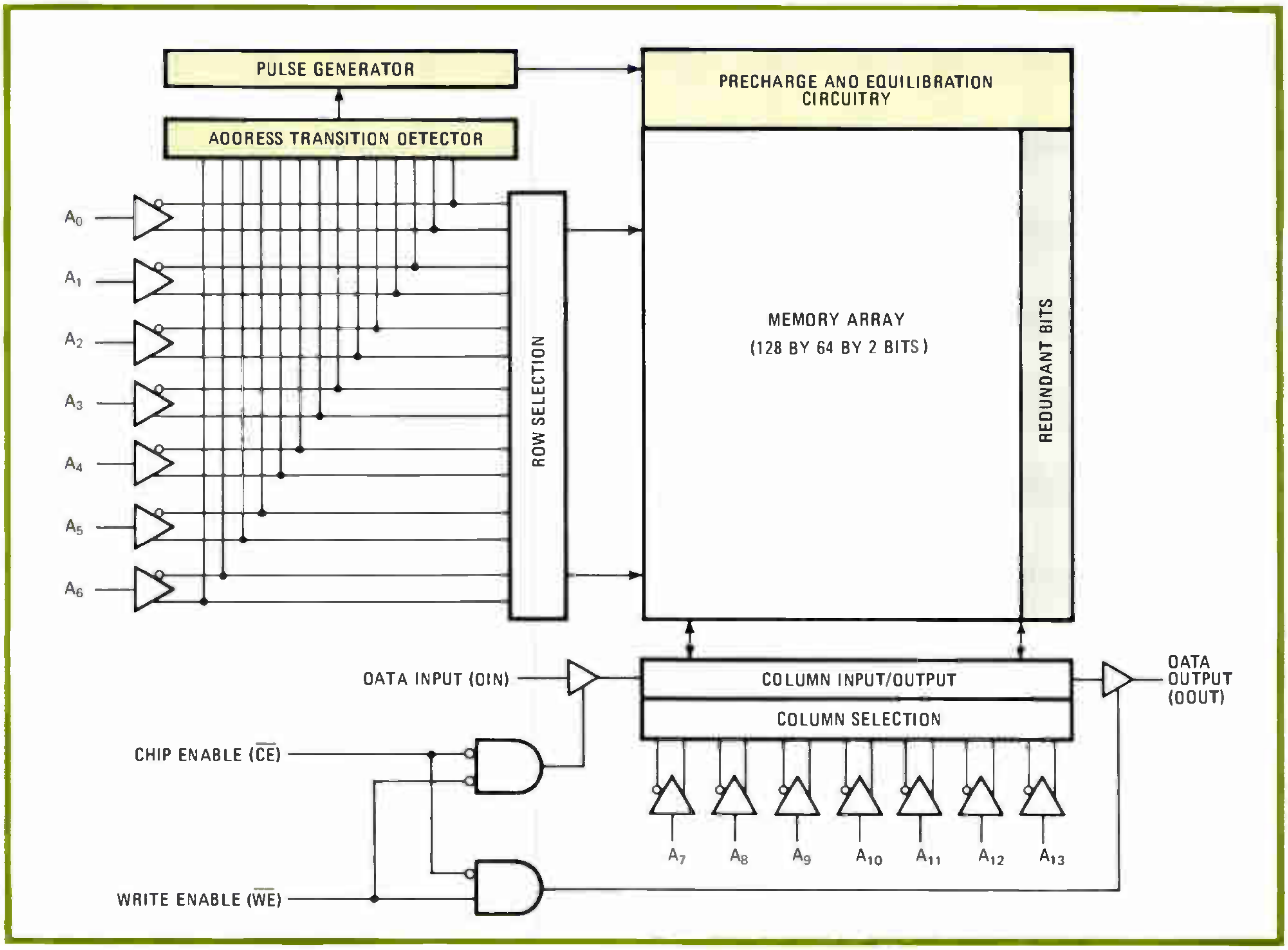
A new circuit technique of the IMS1400 overcomes word-line delay and the delay associated with having the memory cell drive the bit lines. In conventional fast static RAMs, polysilicon–word-line delay may cost as much as 20% of the access time. Efforts are therefore being made in the industry to develop low-resistance materials to replace or augment polysilicon.

Another obvious—but unsatisfactory—solution is to use extremely short word lines. This approach has, in fact, been adopted by one manufacturer of a 16-K static RAM; it uses a 64-column-by-256-row memory array, split in half by the row decoders [*Electronics*, July 3, p. 175]. However, not only does this result in an undesirable chip aspect ratio of 3:1, but it also doubles the bit-line capacitance over that of a 128-by-128-bit array. As a result, part of the word-line delay is simply transferred to the bit lines since the cell now has to drive twice the capacitance.

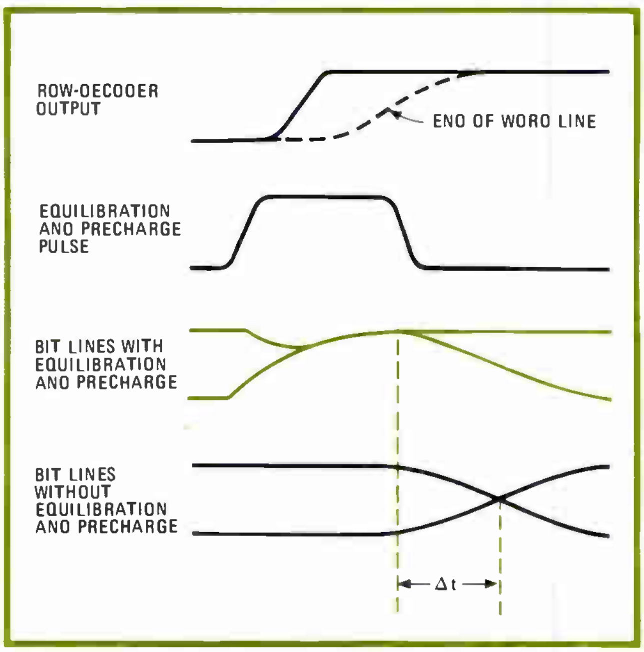
The large bit-line capacitance also contributes to the other significant delay that occurs in conventional static RAMs. When a memory cell is selected by the word line, it must drive the bit lines from their previous data state into the new data state. Since the memory cell devices are quite small and the bit lines exhibit relatively large capacitances, the time required for the bit lines to attain an equilibrium point may be inordinately long. Sensing of the data obviously cannot occur until after this equilibrium condition is reached and the bit lines begin to move in the direction of their new voltage levels.

Whereas other efforts have been directed toward reducing or eliminating the word-line delay, the IMS1400 uses this time to force the bit lines to an equilibrium point, thereby giving the memory cell a head start in driving the bit lines to their new data states. Referring to the block diagram of Fig. 3, an address-transition detector coupled to the row-address buffers senses any changes at the row-address inputs and activates a pulse generator. The pulse generator rapidly develops a self-timed pulse of a preset duration that tracks any change in polysilicon–word-line resistance, as well as changes in other device parameters.

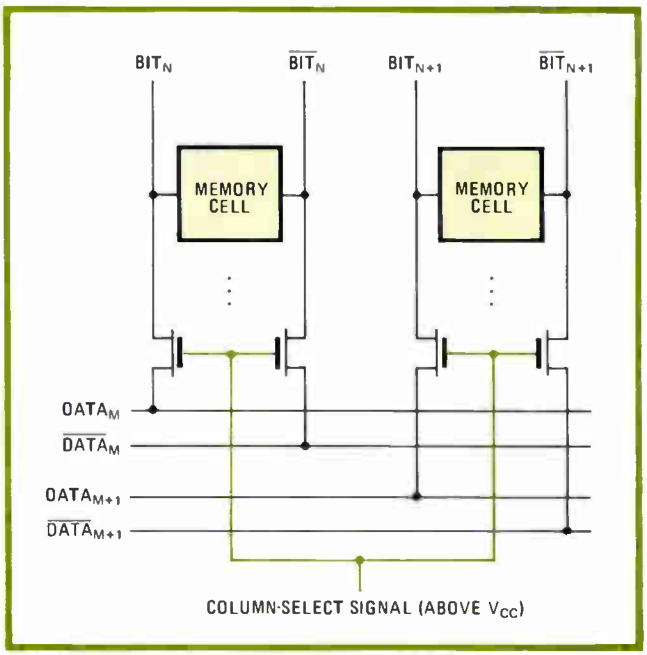
This pulse forces the bit lines to an equilibrium state before the output of the row decoder has propagated all the way to the end of the word line. As shown in Fig. 4, since equilibration of the bit lines is accomplished concurrently with the word-line delay time, the time required for the bit lines to switch to their new data states is reduced by a period Δt. Sensing of the data can thus begin immediately after the row decoder output



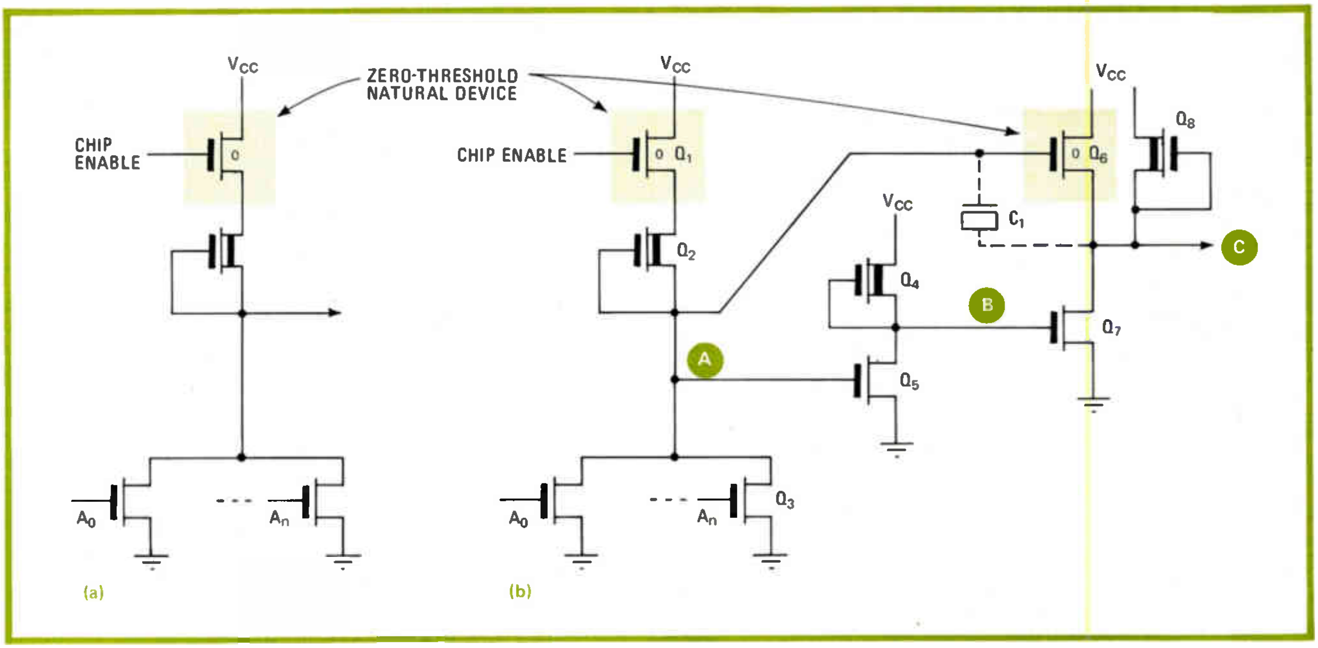

**3. To good use.** Instead of trying to eliminate the word-line delay, Inmos has designed its IMS1400 to use that time to force the bit lines to an equilibrium point, thereby giving the cell a head start on its path toward a new state. A pulse generator activates the equilibration circuitry.




**4. Overlapped timing.** Since equilibration of the bit lines is accomplished during word-line delay, the time required for the bit lines to switch states is reduced by the period Δt. This technique can reduce the access time of the memory by more than 30%.




**5. Bootstrapped and doubled up.** Bootstrapping the column-select signal results in a stronger drive on the column-select gate, enhancing the transfer of data from the bit to the data line. An interleaved column-decode scheme reduces data-line capacitance.




**6. Goodbye to naturals.** Decoders have evolved from the simple NOR circuit (a) to the buffered NOR with bootstrapping (b). The IMS1400's decoder eliminates zero-threshold devices, dissipates less power, is twice as fast, and operates reliably and asynchronously.

reaches the end of the word line instead of having to wait for the cell to drive the bit lines to an equilibrium point first. This technique can reduce the access time of the memory by more than 30%.

### Active precharge keeps it cool

High-speed asynchronous static RAMs traditionally suffer from extremely high active-power dissipation. The 2147 dissipates almost 1 watt. Memories like the 2147 use saturated enhancement-load devices to pull one of the bit lines high in each column. The power dissipated by these load devices during the active cycle can amount to more than 35% of the total active power of the chip.

The IMS1400 uses active precharging to pull up the bit lines each time a row-address transaction is sensed. This precharging of the bit lines is initiated by the same pulse that accomplishes bit-line equilibration. As mentioned earlier, this pulse is designed to be self-terminating. Once the precharging is complete, the active bit-line loads are cut off altogether, thus reducing their power dissipation to zero.

Yet another delay that limits the speed of conventional static RAMs is associated with the column-select transistors connecting the selected pair of bit lines to the data lines (see Fig. 5). In previous designs, the column-select signal is driven to the power supply potential for column selection. Since the bit lines are initially at one enhancement threshold drop below $V_{cc}$, the column-select transistors are off until the selected memory cell begins to pull one of the bit lines to a level lower than $V_{cc}$. Since they are operating in a weak conduction mode (the gate drive is very small with such a minor gate-source voltage, $V_{gs}$), significant delays arise as data is transferred from the bit lines to the data lines.

A new bootstrapping technique drives the gates of the column-select transistors above $V_{cc}$. These devices must operate in a highly conductive mode to effect rapid transfer of the data from the bit lines to the data lines. It has not been possible in the past to use signals above the power supply voltage to advantage in fully asynchronous static RAMs. However, the circuit used in the IMS1400 allows the column decoder output to remain at a voltage above $V_{cc}$ indefinitely.

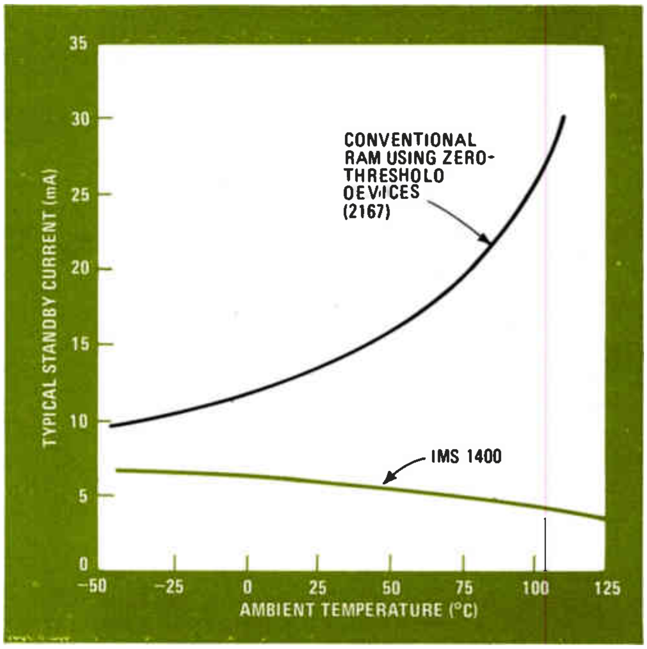
To reduce data-line capacitance, a fully interleaved two-stage column decoder is used. As shown in Fig. 5, adjacent columns are connected to separate pairs of data lines when a common column-select signal goes high. A second stage of decoding connects one of the two data-line pairs to the data bus. Since only one out of four column-select transistors is connected to each data line pair, and since the column-select transistors can be made smaller as a result of being driven with a signal above $V_{cc}$, the data lines see a significantly reduced capacitive loading. This makes the part even faster.

### Asynchronous, glitchproof bootstrapping

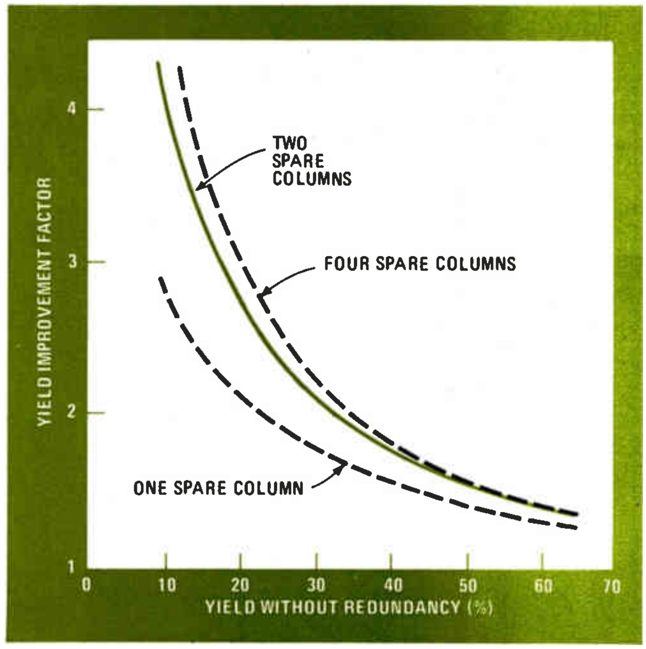
Although the power and speed advantages of bootstrap circuits have been proven in dynamic RAMs, conventional configurations have not been used effectively in asynchronous static RAMs because of the following inherent limitations:

- A precharge setup time is required that cannot be guaranteed in an asynchronous environment.
- Input noise spikes, or glitches, may cause the bootstrapping action to fail, thereby resulting in speed loss or even functional failure.
- The bootstrapped node will eventually leak to a lower level, thereby eliminating the use of voltage above the positive power supply voltage.

Figure 6 shows the evolution of decoders in fast asynchronous static RAMs. The circuit in Fig. 6a is a simple depletion-load NOR decoder with the addition of a 0-V-threshold, or "natural," transistor used to power down the decoder when chip-enable signal CE is low. The




**7. Inversely proportional.** Other static RAMs use 0-v–threshold transistors as power switches to turn off circuitry for standby. But at elevated temperatures, these devices tend to conduct. Since the IMS1400 does not employ such transistors, its power stays low.




**8. Redundancy.** Up to two defective columns may be repaired in the IMS1400. Two spare columns are almost as efficient as four, and they occupy less area. In the IMS1400, the extra circuitry consumes less than 2% of the chip area and does not affect speed or power.

output switches to approximately $V_{cc}$ when all address inputs are low, and it is pulled near ground when any address input is high. This type of circuit is used as a row decoder in the 2147 4-K static RAM.

To improve speed and reduce power dissipation, a buffered NOR decoder (Fig. 6b) is used as a column decoder in the 2147. The advantage of this circuit over the simple NOR decoder is that the power-consuming input stage is buffered from the output. Also, capacitor $C_1$ is added to bootstrap the gate of transistor $Q_6$ to improve the drive of the output stage.

Normal operation of the circuit in Fig. 6b may be described as follows. When one or more of the address inputs is high, node A is pulled to ground, node B rises toward $V_{cc}$, and node C—the output—is low. When the address input goes low, node A rises to create a voltage differential across $C_1$. At this time, the bootstrap capacitor is said to be precharged.

Next, node B goes low, turning off $Q_7$. (The delay through the inverter composed of $Q_4$ and $Q_5$ must be long enough to ensure that a sufficient voltage differential has developed across $C_1$ before $Q_7$ is turned off.)

Node C then rises, causing node A to be capacitively coupled—bootstrapped—above $V_{cc}$. $Q_6$ is therefore turned on hard, quickly pulling node C to $V_{cc}$. $Q_8$, a high-impedance depletion-mode transistor (often called a keeper), is used to hold the output node C at $V_{cc}$ potential in the selected state.

This circuit suffers from several basic problems. The bootstrapping action will actually fail if input glitches or random voltage transitions occur at the input. This failure mode may be understood by noting that the $C_1$ may not have a positive voltage across it when the decoder is in a selected state. Owing to junction and subthreshold leakage, this will happen when node A falls to $V_{cc}$ while node C is still held at $V_{cc}$ by $Q_8$. When one or more address inputs go high, node A begins to fall immediately, whereas node C will start dropping after a delay through the $Q_4$–$Q_5$ inverter.

Should the address inputs now go low, node A will rise, causing node B to fall, shutting off $Q_7$. At this time node C may be between 0 V and $V_{cc}$ and node A may be at a voltage equal to or less than the voltage at node C. Since $C_1$ does not have a positive voltage across it, the required bootstrapping action will not occur. The circuit will behave as if the capacitor did not exist, severely degrading the speed at node C.

Since in a fully asynchronous static RAM any random voltage transitions may occur, this bootstrap circuit will not function reliably at all times. Even when the bootstrapping action does occur, node A is not isolated from the large capacitance associated with the address gates, and the resulting capacitive divider action reduces the efficiency of the bootstrap, impairing circuit speed.

Bootstrapping in the IMS1400 is intended primarily for asynchronous environments. The circuits are faster, consume less power, and allow the use of signals above $V_{cc}$ since the bootstrapped nodes are capable of maintaining their levels indefinitely. They place no precharge setup-time requirement on an input signal.

The bootstrapped nodes are isolated from the capacitance of the address gates, and new circuit techniques guarantee the existence of a sufficiently positive voltage differential across the capacitor at all times. Specifically, the circuits are insensitive to input glitches and will respond reliably to any input signal.

In addition to ordinary enhancement- and depletion-mode transistors, conventional fast static RAMs employ zero-threshold transistors to act as power switches. Their use allows nearly all peripheral circuitry to be powered down with a single external control signal. In principle, the threshold voltage of these so-called natural devices is zero, so that they act as nearly ideal current switches. However, control of their threshold voltage is very critical to the performance of the circuit. On the one hand, if the threshold voltage is slightly negative, these devices cannot be turned off, with the result that standby power increases dramatically. If, however, the threshold voltage is slightly positive, loss of circuit speed results because of transistor current gain degradation and voltage drops on internal signals.

### No need for naturals

In addition, wafer yield is affected because zero-threshold transistors necessitate an additional masking step and increased handling of unprotected gate oxides in the manufacturing process.

Besides having an adverse effect on yield and throughput, a significant system-level problem arises through the use of zero-threshold transistors. Even if the threshold voltage is exactly zero with back biasing, when power is initially applied, these transistors will be depletion-mode because the substrate is at 0 V. A large transient current will therefore occur until the on-chip bias generator has pumped down the substrate, and it could lock out the power supply servicing a large system that exploits the power-down feature.

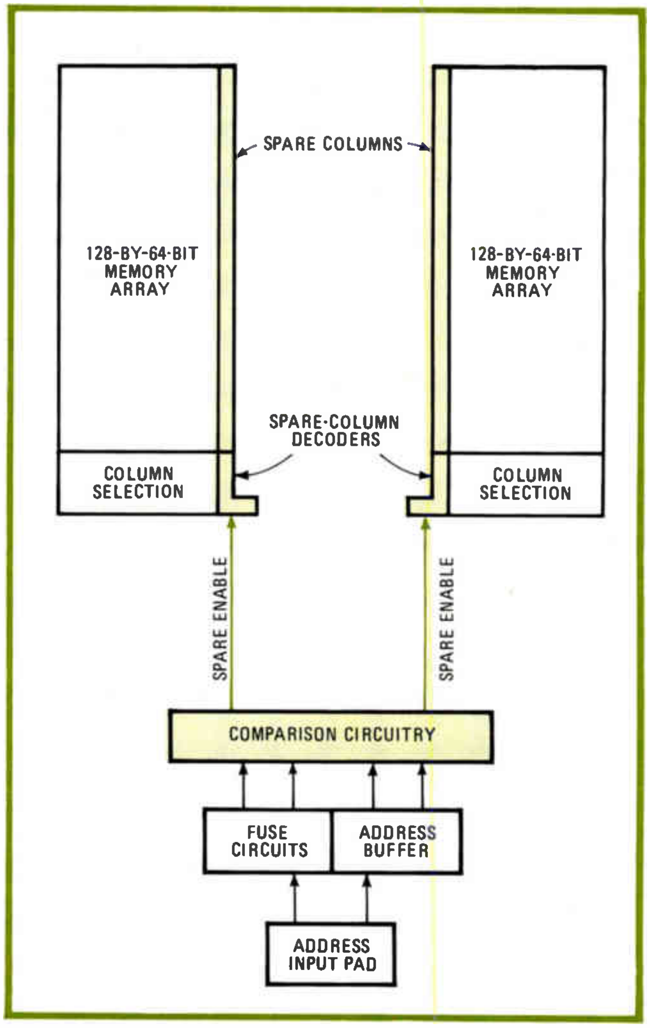
The bootstrap drivers and circuit techniques used in the IMS1400 eliminate the need for zero-threshold transistors. In fact, only enhancement- and depletion-mode transistors are used (instead of the four different types of transistors used in some H-MOS II fast static RAMs). Not only are the technological and applications-related problems eliminated, but standby power at elevated temperatures is also significantly reduced.

Figure 7 compares the standby power of the IMS1400 with that of Intel Corp.'s forthcoming 16-K static RAM, which employs zero-threshold devices. Though the standby power of the other static RAM more than triples during a −50° to 115°C temperature excursion, the standby power of the IMS1400 actually drops at elevated temperatures. Part of this difference stems from the fact that the zero-threshold transistors become depletion-mode at higher temperatures and so do not turn off.

### Just enough redundancy

The yield of memory chips is reduced by localized defects that affect a small number of single bits, rows, or columns of the array. To deal with this problem, multiple row and column redundancy schemes have been proposed. Previous techniques are hard to use (requiring, for instance, lasers), impair the performance of the circuit, or require too much chip area.

The fault-tolerant design of the IMS1400 can permanently correct up to two defective columns of memory cells. Figure 8 shows the impact of redundancy on yield, based on a statistical model of random defects. As seen from the curves, the optimal amount of redundancy is two extra columns. The use of two spare columns also enables the correction of a defect occurring on the boundary of two adjacent columns. This particular redundancy scheme uses less than 2% of the total chip area, requires essentially no extra power, and does not impair the speed of the circuit.




**9. Swapping.** Improving on hard-to-use or area-consuming schemes, programmable fusible polysilicon links store redundancy information. Since the column-access time is inherently faster than the row-access, spare-column selection does not slow the chip.

Figure 9 presents the basic redundancy technique. The addresses of the defective columns are permanently stored on the chip using programmable polysilicon fusible links. During memory operations all incoming column addresses are compared with the stored fuse information. Should they match, a spare column is automatically selected instead of the defective column. Since the column access time of the memory is inherently faster than the row access time, selection of a spare column does not result in any speed degradation.

### Just the beginning

The IMS1400 attains performance equal to or better than that of today's fastest MOS RAMs—like the 4-K 2147H—yet uses design rules that are significantly more relaxed than the 2-$\mu$m dimensions of such RAMs. Future products from Inmos will, in fact, further utilize direct-stepping-on-wafer photolithography to shrink device dimensions to 2 $\mu$m and beyond, resulting in even more impressive performance and density. □

# Achieving stability in IC oscillators

Waveform-generator chips that operate above 1 megahertz rely on emitter-coupled circuits needing sophisticated temperature compensation

by Ilhan Refioglu, *Exar Integrated Systems Inc., Sunnyvale, Calif.*

☐ Monolithic waveform and function generators form the backbone of circuits in a wide range of applications—telecommunications, data transmission, and test-equipment design and calibration. These integrated-circuit oscillators are characterized by an output waveform that is well-defined, repeatable, and stable despite changes in ambient temperature and power-supply level.

Modern waveform- and function-generator ICs are overcoming the limitations of older IC oscillators like phase-locked loops and voltage-to-frequency converters. The latter type of device is limited in performance by the fact that it provides only pulse-train or square-wave outputs. Waveform and function-generator chips, on the other hand, provide a wider variety of output waveforms, and do so at lower cost.

A function-generator IC generally consists of a current- or voltage-controlled oscillator section that generates the periodic waveform and allows for frequency variation, a wave-shaping section—basically, a sine-wave shaper—and a modulator (Fig. 1).

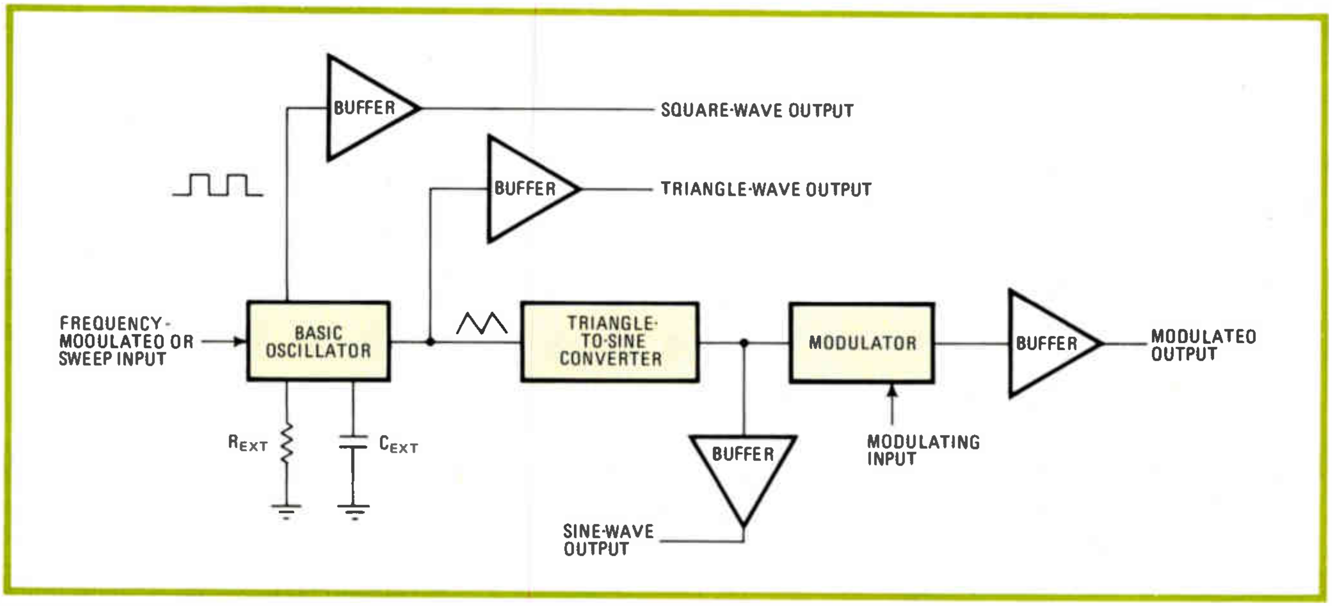
The heart of any function-generator IC is the oscillator section. This circuit determines the chip's most important performance characteristics. These include stability with power-supply voltage and temperature changes, frequency range, sweep linearity, and so on.

There are two major types of IC oscillators, differentiated mainly by their ability or inability to operate at frequencies above 1 megahertz. Oscillators that operate under 1 MHz generally employ lateral pnp transistors for switching and saturated logic. Their operating frequencies are limited in practice to several hundred kilohertz. But they also feature high stabilities of 50 parts per million per °C or less, thanks to careful compensation techniques employed in their designs.

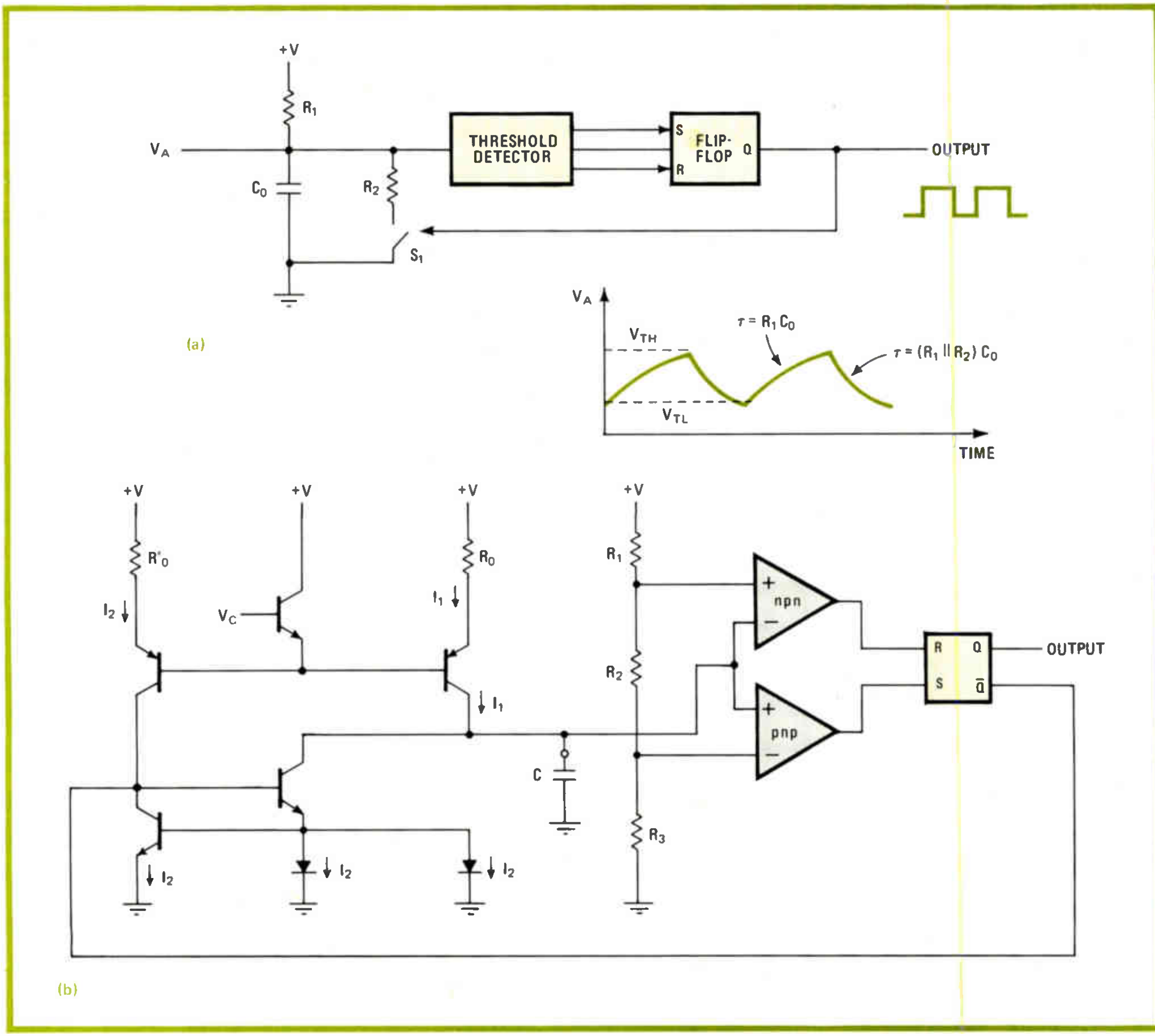
## Speed versus stability

Oscillators that operate above 1 MHz employ emitter-coupled multivibrators and npn transistors. They are inherently capable of operation up to 10 MHz. But they also suffer from frequency instabilities of more than 150 ppm/°C and low-frequency inaccuracy.

Figure 2a shows a basic RC multivibrator low-frequency oscillator circuit that has gained wide acceptance among IC oscillator designers. Capacitor $C_0$ is exponentially charged through resistor $R_1$ to the supply-voltage level. When the voltage across $C_0$ ramps up to




**1. Functions.** Generating waveform functions involves three major circuit elements: a basic oscillator to produce a periodic and variable-frequency wave, a wave-shaping section, and a modulator. The oscillator frequency is controlled by either a voltage or a current.



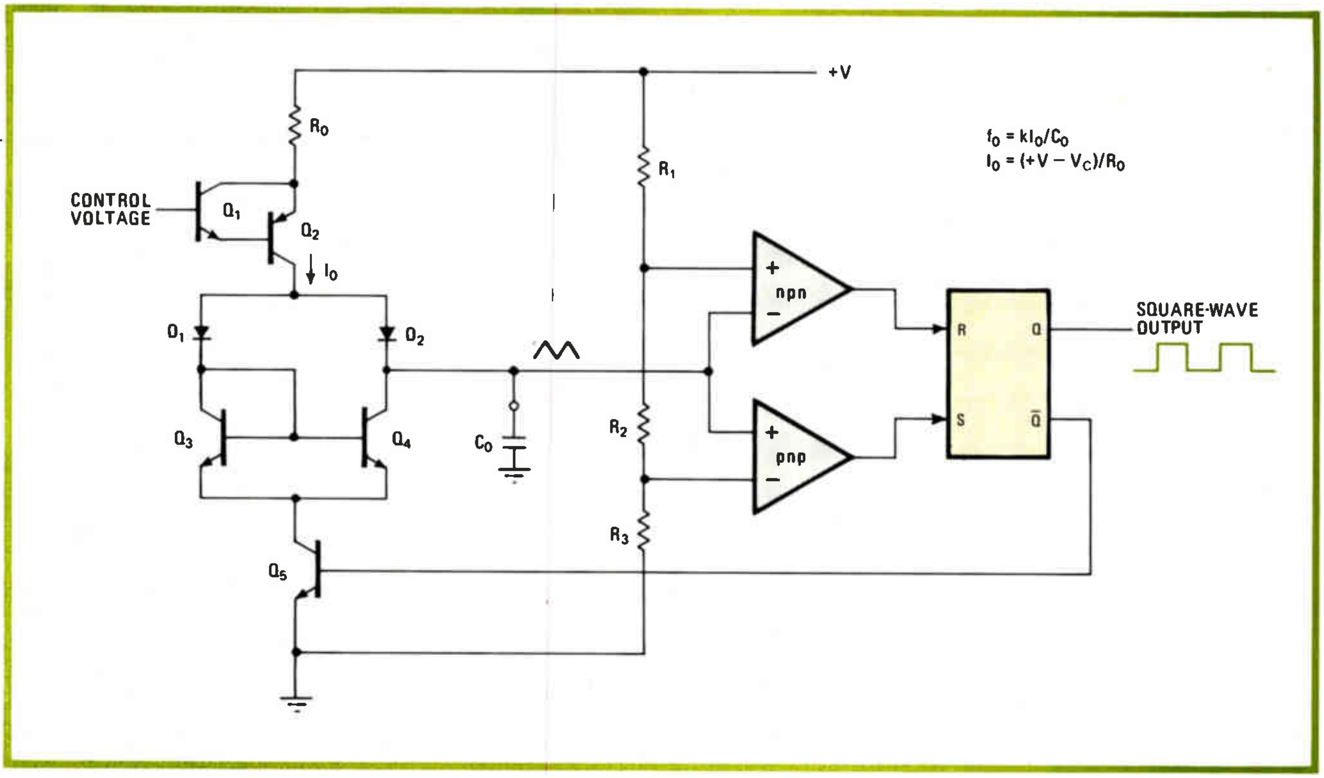

**2. Stable.** A basic RC multivibrator oscillator (a) offers high stabilities, but its lateral pnp transistors limit it in operating frequency to about 100 kilohertz. An implementation similar in concept (b) differs in that two current sources, $I_1$ and $I_2$, are used in place of resistors $R_1$ and $R_2$.

the higher of two threshold values, $V_{TH}$, the threshold detector changes the flip-flop's state, thus closing switch $S_1$ (usually a transistor). With $S_1$ closed, $C_0$ starts discharging its voltage exponentially to ground through the parallel combination of $R_1$ and $R_2$. When $C_0$'s voltage reaches a lower threshold, $V_{TL}$, the threshold detector is once again activated, causing the flip-flop to revert to its original state, and the charging process is repeated. Note that if $R_1$ is small, an exponential sawtooth waveform is obtained. If $R_2$ is much larger than $R_1$, the output waveform will be symmetrical.

A circuit similar in principle to that of Fig. 2a uses two current sources, $I_1$ and $I_2$, in place of $R_1$ and $R_2$ to generate a linear ramp waveform across the capacitor. When current $I_2$ is equal to $2I_1$, a symmetrical-output triangular or square waveform is obtained. A practical implementation of this circuit is shown in Fig. 2b. This type of circuit is employed in the ICM8038 IC oscillator from Intersil Inc., Cupertino, Calif. Charging and discharging of capacitor C are performed by currents $I_1$ and $I_2$. $I_1$ and $I_2$ are equal to the supply voltage minus $V_C$ divided by resistors $R_0$ and $R_0'$, respectively. Although $I_1$ is always on, $I_2$, which is doubled by the current mirrors, is switched on and off by the flip-flop's output. $I_1$ performs the charging function while current $2I_2 - I_1$ does the discharging.

If resistors $R_0$ and $R_0'$ are equal, then $I_1$ equals $I_2$ and C is charged and discharged by identical currents, leading to symmetrical output waveforms. Oscillator frequency for this case is a constant value, k, multiplied by $I_1C$. Since current is set up by a control voltage, this circuit is known as a voltage-controlled oscillator.

A different type of VCO circuit is the one used in the popular type NE566 function-generator IC from Signetics Corp., Sunnyvale, Calif., and others. It is also used as the VCO for the Signetics 565 phase-locked loop IC. The circuit and its implementation are shown in Fig. 3. The same voltage-controlled current, $I_0$, is used to




**3. Voltage-controlled.** This voltage-controlled oscillator is used in the popular 565 phase-locked-loop integrated circuit and in a function-generator IC, Signetics' NE566. Another astable multivibrator, it uses one voltage-controlled current, $I_0$, to charge and discharge capacitor $C_0$.

charge and discharge capacitor $C_0$ via the actions of the flip-flop circuit.

When transistor $Q_5$ is off, $I_0$ charges $C_0$ through diode $D_2$. When the voltage across $C_0$ reaches the trip point of the comparator, the flip-flop changes state and $Q_5$ is turned on. At this point $D_2$ becomes back-biased and $C_0$ is discharged through $Q_4$ by the mirrored current, $I_0$, until the voltage across $C_0$ reaches the lower threshold level. Then the flip-flop reverts to its original state, turning off $Q_5$ and repeating the charge-discharge cycle. Since the same current is used for charging and discharging, the circuit's duty cycle cannot be varied.

The oscillators of Figs. 2 and 3 are astable multivibrator circuits. They exhibit good stabilities, in the range of 50 to 100 ppm/°C. Unfortunately, they are limited to a maximum frequency of about 100 kHz due to the use of lateral pnp transistors.

## Emitter coupling for higher frequency

Figure 4a shows a simplified schematic of an emitter-coupled multivibrator oscillator capable of 20-MHz operation. This circuit is difficult to compensate for changes in temperature, however, for very good frequency stability at high operating frequencies.

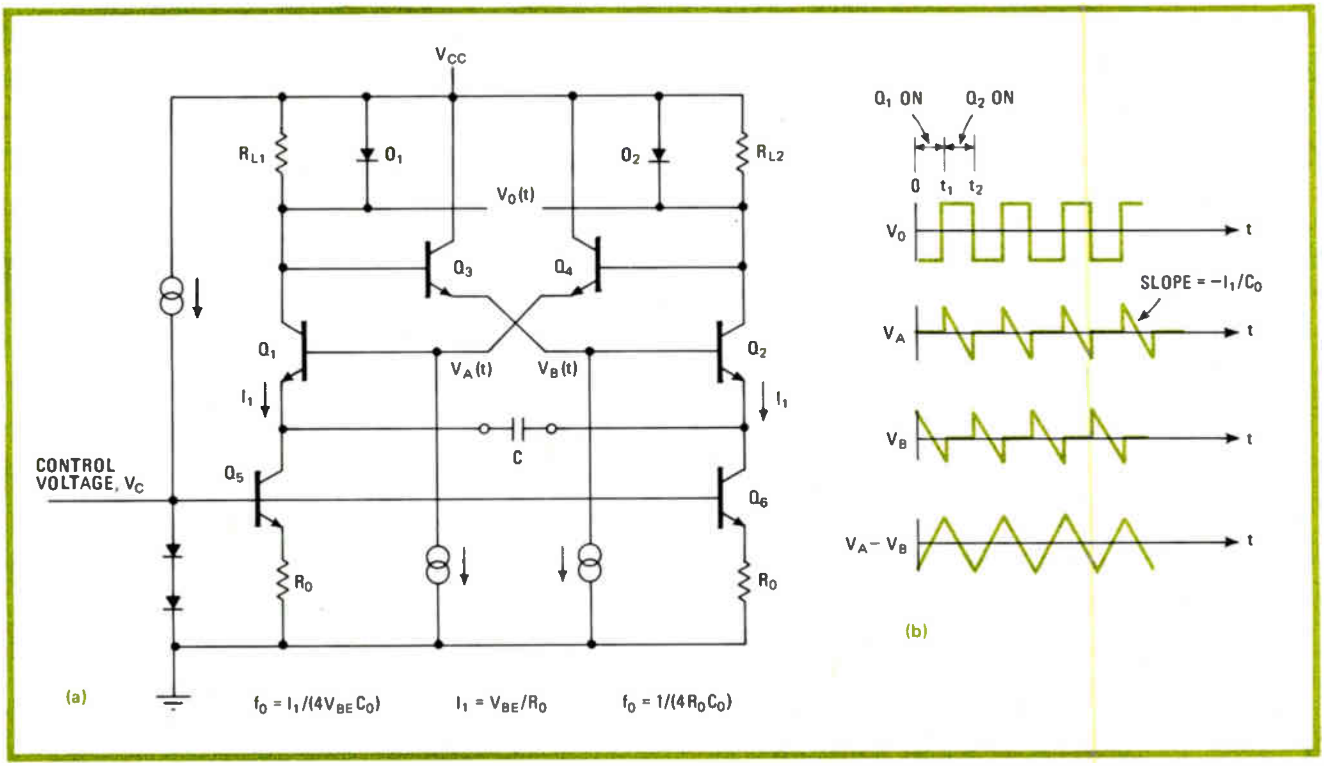
Transistors $Q_1$ and $Q_2$, resistors $R_{L1}$ and $R_{L2}$, and the timing capacitor C form the heart of the multivibrator. The clamping action of $D_1$ and $D_2$ and the level shift of emitter-followers $Q_3$ and $Q_4$ (which are always conducting) keep the circuit from saturating and firmly establish the voltage swings. At a given time, either $Q_1$ and $D_1$ or $Q_2$ and $D_2$ are conducting, so that C is alternately charged and discharged by constant current $I_1$, which is generated by $Q_5$ and $Q_6$. When $Q_1$ is on, the output $V_A$ is constant at $V_{CC} - 2V_{BE}$ (where $V_{CC}$ is supply voltage and $V_{BE}$ is $Q_1$'s base-emitter voltage), and the output $V_B$ is a linear ramp with a slope equal to $-I_1/C$, since $Q_2$ is off. When $V_B$ is pulled low enough (1 $V_{BE}$ below $Q_2$'s base, which is at $V_{CC} - 2V_{BE}$) by $I_1$, $Q_2$ turns on and regenerative switching occurs. The collector of $Q_2$ is pulled down to a diode drop below $V_{CC}$ and the base of $Q_1$ is pulled down to $V_{CC} - V_{BE}$, turning off $Q_1$ and raising its collector rapidly by 1 $V_{BE}$ to the supply level. This step of 1 $V_{BE}$ appears at the emitter of $Q_2$ and is transmitted to the emitter of $Q_1$ by C. The emitter of $Q_1$ is now 1 $V_{BE}$ above its base and must slew a full $2V_{BE}$ at $I_1$, with a slope equal to $-I_1/C$, before the oscillator changes state again.

The waveforms generated by this oscillator circuit are shown in Fig. 4b. The voltage at the collectors of $Q_1$ and $Q_2$ are two symmetrical square waves, with peaks between $V_{CC}$ and $V_{CC} - V_{BE}$. The differential output $V_0$ across diodes $D_1$ and $D_2$ corresponds to a symmetrical square wave, with a peak-to-peak amplitude of $2V_{BE}$. $V_A(t)$ and $V_B(t)$ are linear ramp waveforms with peak-to-peak amplitudes of $2V_{BE}$. They can be subtracted from each other to produce a linear triangular waveform, which is the voltage across the capacitor. Subtraction can be performed by a simple differential amplifier stage whose output voltage is a triangular waveform. The same differential amplifier circuit can also be used to obtain a sinusoidal output.

The frequency of oscillation $f_0$ of the emitter-coupled multivibrator of Fig. 4a can be expressed as:

$$f_0 = I_1/(4V_{BE}C)$$

The frequency can be controlled by varying $I_1$ by means




**4. High frequency.** An emitter-coupled multivibrator oscillator (a) allows the generation of waveforms (b) of up to 20 megahertz. Unfortunately, this type of circuit is difficult to compensate for changes in temperature, leading to poor stabilities at high frequencies.

of a control voltage, $V_C$. The symmetry of the triangular- and square-wave outputs can be offset by changing the ratio of emitter resistors of $Q_5$ and $Q_6$. This ratio effectively changes the ratio of the current that charges capacitor C to the current that discharges it. In this manner, the triangular- and square-wave outputs can be converted to sawtooth or pulse waveforms.

The emitter-coupled multivibrator circuit shown is widely used for high-frequency applications. Oscillator types NE560 and NE562 from Signetics and others, as well as Exar phase-locked loops type XR-S200, XR-210 and XR-215, use it. The Exar XR-205 monolithic waveform generator also uses a similar emitter-coupled astable multivibrator design.

### Strong temperature dependence

The frequency of this emitter-coupled multivibrator circuit is a function of $V_{BE}$, which in turn is strongly dependent on temperature. To overcome this strong temperature dependence, the timing current $I_1$ is also made a function of $V_{BE}$, such that $I_1 = V_{BE}/R_0$. Thus to a first-order degree, $f_0$ is temperature-compensated and is expressed as:

$$f_0 = (V_{BE}/R_0)/(4V_{BE}C) = 1/(4R_0C)$$

This compensation is only effective at the center frequency. Since the control current that modulates the frequency is not compensated, even very small control-current deviations degrade the temperature coefficient drastically (typically ±300 ppm/°C at ±10% current deviation).

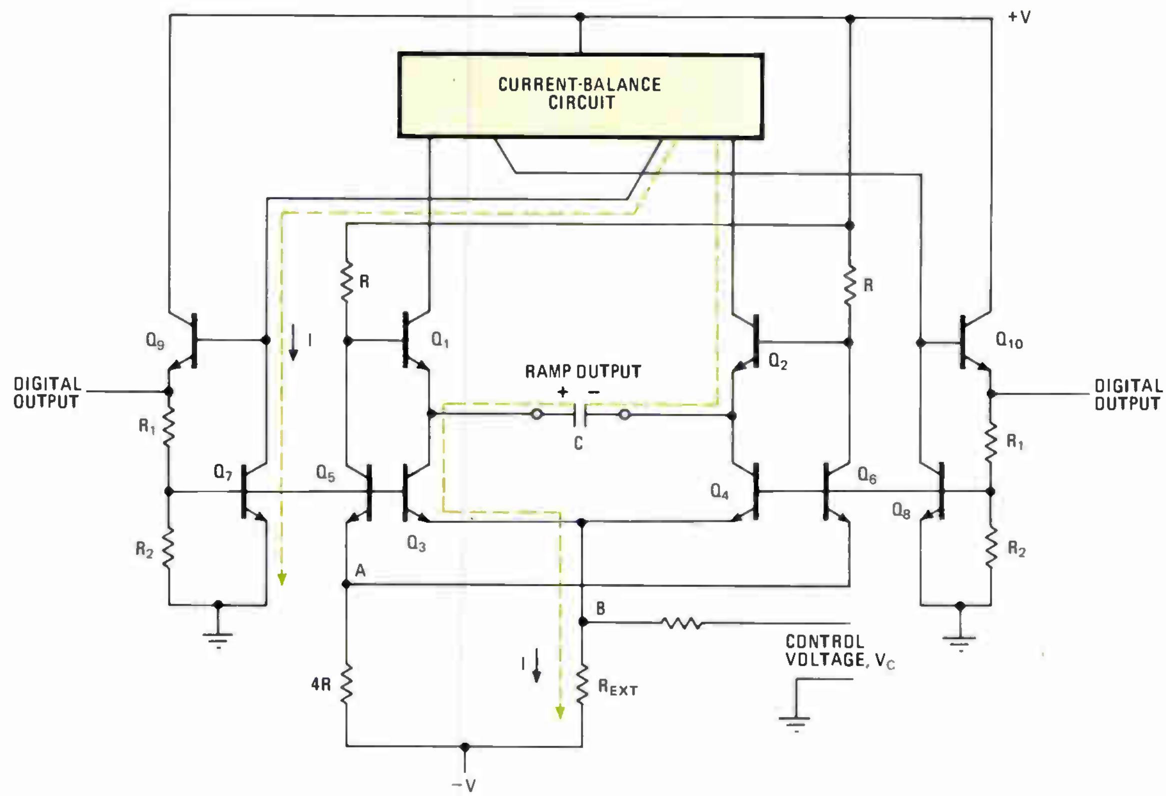
Despite center-frequency compensation, the emitter-coupled multivibrator still exhibits a temperature coefficient of 200 to 300 ppm/°C. The culprits are the charging-current imbalance in $Q_1$ and $Q_2$ near the switching thresholds and the switching transients. The transients depend on circuit resistances, transistor transconductances, and input resistances, which all are temperature-sensitive. Temperature drift of the circuit is inherent in its emitter-coupled multivibrators. There are other compensation techniques that can be used to make a high-stability (typically 50 ppm/°C or less) oscillator out of the circuit in Fig. 4a, but this is usually achieved at the expense of speed.

### Improving temperature compensation

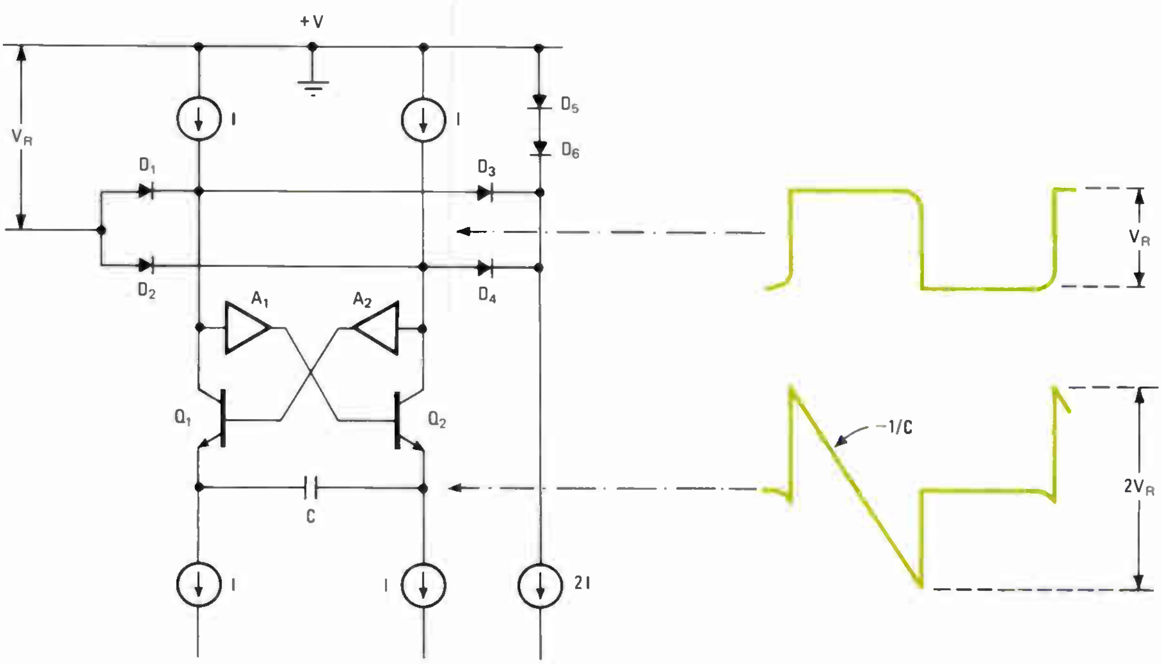
Two very stable temperature-compensated oscillator configurations are used in Exar's XR-2206 and XR-2207 function-generator ICs as well as in the company's XR-2211 and XR-2212 phase-locked-loop ICs. They use a temperature-compensated emitter-coupled astable multivibrator circuit that has a typical temperature stability of 30 ppm/°C (Fig. 5).

Timing current, I, set up by $R_{ext}$, flows in $Q_2$, C, and $Q_3$ when transistors $Q_5$, $Q_7$, and $Q_9$ are on. The timing current is inverted by the current balance and establishes an identical emitter current density in $Q_7$. The voltage at the control input B is thus held at 0 over a wide range of timing currents. At an optimum current value, point A is also at 0 V, eliminating the temperature coefficient introduced in this area. When the state changes, I flows in $Q_1$, C, and $Q_4$; all the compensation transistors on the right are turned on; and I is inverted by a current balance. As a result, I establishes an identical emitter current density in $Q_{10}$.

The instability introduced by a shift in the regenera-




**5. Compensation.** Emitter-coupled astable multivibrators can be stabilized using this temperature-compensated circuit. Typical temperature stabilities of 30 parts per million per °C are possible. This circuit is used in Exar's XR2207 function-generator and XR2211 PLL chips.




**6. Clamped.** The emitter-coupled multivibrator in Analog Devices' AD537 voltage-to-frequency converter relies on another temperature-compensation method. The collectors of $Q_1$ and $Q_2$ are clamped and a differential reference voltage across them charges capacitor C.

tion point arising from $dV_{BE}/dT$ (where T is temperature) in $Q_1$ and $Q_2$ is minimized by the current balance, which forces the currents in these two transistors to be equal at the switching point.

The square-wave output is obtained differentially at the emitters of $Q_9$ and $Q_{10}$. A linear ramp is obtained across capacitor C. The frequency of operation is given by $f = 1/(CR_{ext})$ and can be controlled by modulating the current, I, via the control voltage, $V_C$, applied to control node B.

### Clamped collectors

Another temperature-compensated emitter-coupled multivibrator, used in Analog Devices' AD537 voltage-to-frequency converter chip, is shown in Fig. 6. In this precision collector-clamping scheme, a differential voltage, $V_R$, generated by a bandgap reference circuit, appears across the collectors. $V_R$ is independent of the current, the temperature, the absolute value of $V_{BE}$, and the supply voltage. This precise reference voltage is then transferred to the timing capacitor via two-stage emitter-followers $A_1$ and $A_2$ and transistors $Q_1$ and $Q_2$. Thus, the capacitor charges to $2V_R$ twice each cycle, yielding a frequency expression of $f = 1/(4CV_R)$.

To compensate for the temperature drift mechanisms inherent in emitter-coupled multivibrators mentioned earlier, a small temperature coefficient in the opposite direction is deliberately added to the voltage reference $V_R$. Using this technique, excellent stabilities of around 20 ppm/°C are possible.

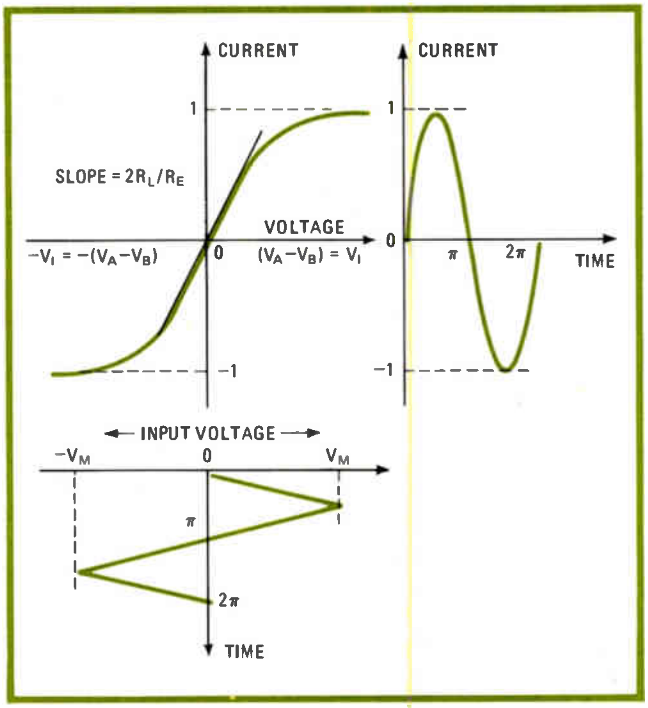
After the generation of a basic waveform such as a triangular or square wave, the next step is to convert the waveform into a low-distortion sine wave. A triangular wave is usually preferred over a square wave, since the former's harmonic content is significantly lower. This initial harmonic content is further minimized by using a symmetrical triangular waveform that has negligible even-harmonic content. Such a waveform can be converted into a sine wave by rounding off its peaks. This is generally accomplished in one of two ways, each of which is suitable to monolithic integration.

### Converting into a sine wave

One method involves a piece-wise linear approximation using breakpoints to round off the triangle wave. This is usually done by diode-resistor or transistor-resistor circuits. A disadvantage of these types of wave-shaping circuit is that the input signal level, active device characteristics, and resistor ratios must be accurately controlled.

The other common method of converting a triangular wave into a sine wave is through the gradual cutoff of an overdriven differential transistor pair with an appropriate value of emitter resistance.

The differential gain state of the transistor pair used to generate the triangular wave can be adjusted to produce an overdrive condition by decreasing emitter resistance to a point where the input transistors are driven into cutoff. Figure 7 shows the voltage-current transfer characteristics of a such an overdriven circuit, with a triangular-wave input and a resulting sinusoidal output. The gradual transition between the active and




**7. Sine shaping.** A common method of converting a triangular wave (bottom left) into a low-distortion sine wave (right) is through the gradual cutoff of an overdriven differential transistor pair, whose transfer function is at top left, with an appropriate emitter resistance.

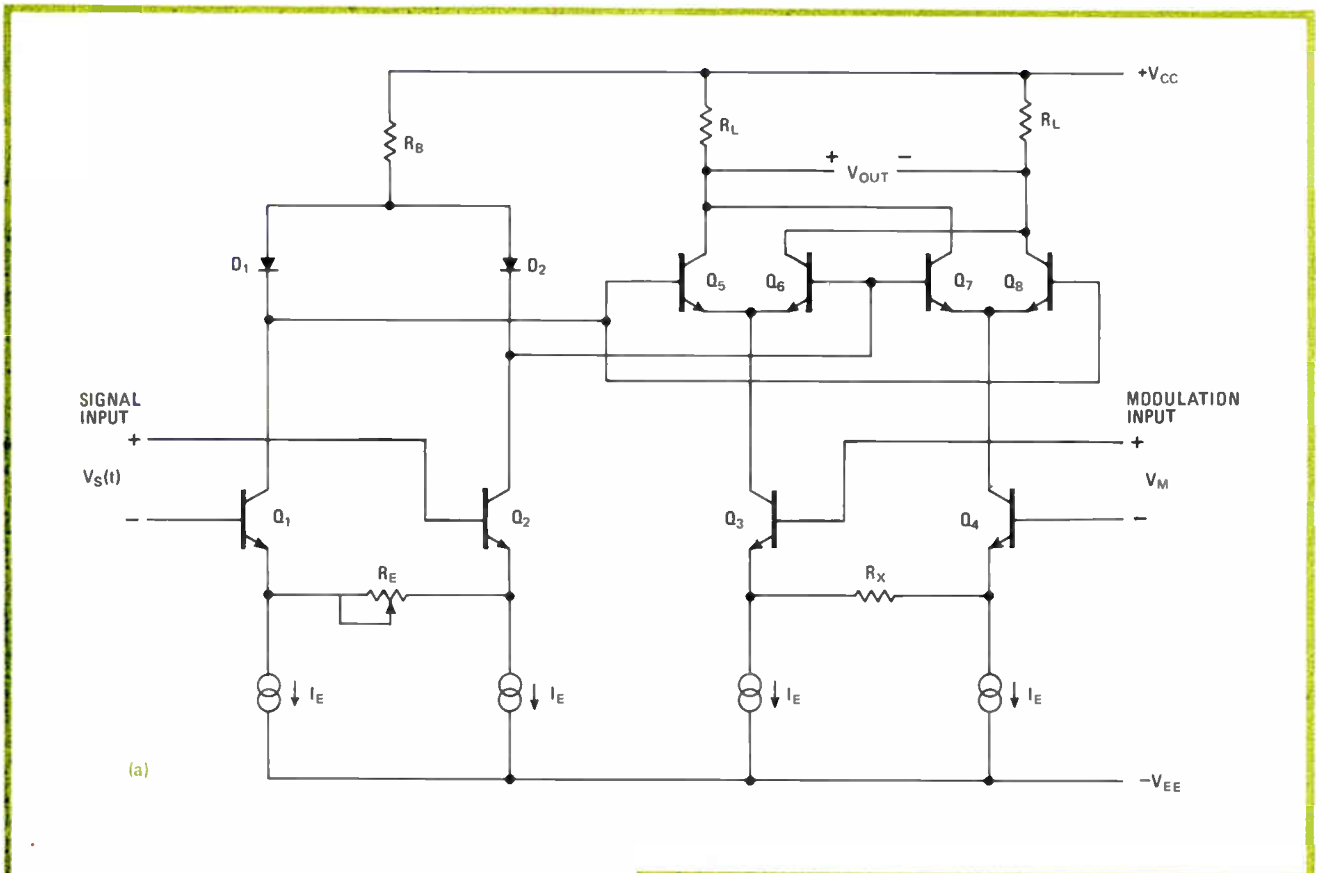
the cutoff regions is logarithmic. Thus the triangular wave is amplified linearly near the center but logarithmically at the peaks. As a result, the sharp peaks of the input signal are rounded off and it is transformed into the desired sine wave.

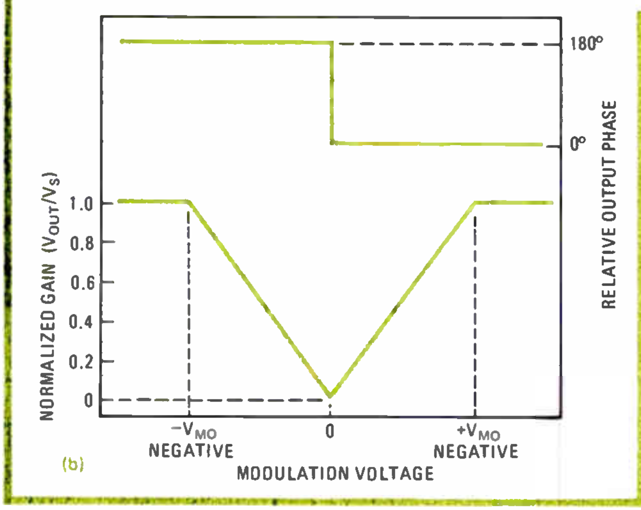
The advantage of the second approach is circuit simplicity. However, it also requires a constant-amplitude input adjustment for low distortion at a given emitter resistance. Both methods can, with adjustment, provide total harmonic distortions of less than 0.5%.

The last building block of the typical waveform generator in Fig. 1 is the modulator section. For function-generator applications, balanced modulators are preferred over conventional mixer types. Balanced modulators offer a high degree of carrier suppression and can be used for suppressed-carrier modulation, as well as for conventional double-sideband amplitude modulation. A simplified circuit diagram of a balanced modulator circuit is shown in Fig. 8a. It is used almost exclusively by manufacturers of this type of IC because of its versatility and suitability for monolithic integration. In addition to performing amplitude modulation, this circuit also functions as a linear four-quadrant multiplier and phase detector. The balanced modulator's phase and amplitude transfer characteristics are shown in Fig. 8b.

### Timers also work like oscillators

The well-known 555 timer IC operates much like the RC multivibrator low-frequency oscillator circuit of Fig. 2a when in its astable mode. The only difference is that resistor $R_2$ is in series with $R_1$, in place of $R_1$ alone. Switch $S_1$ is hooked up between ground and the connection between $R_1$ and $R_2$. Again, operation is by the same




**8. Modulation.** For function generation, a balanced modulator (a) is preferred for its higher carrier suppression and flexibility. Used nearly exclusively by makers of IC function generators, this modulator has the phase and amplitude transfer characteristics shown (b).

charge-and-discharge cycle of capacitor $C_0$, except that the charging voltage is passed through the series combination of $R_1$ and $R_2$, instead of $R_1$ only. The output of the timer circuit is thus determined by the total resistance of $R_1$ and $R_2$ divided by the capacitance of $C_0$.

When the upper threshold of the timer circuit is reached, the circuit's output goes low and $S_1$ is turned on, discharging $C_0$ to ground through $R_2$. When the voltage reaches the lower threshold level, the threshold detector is triggered to begin a new cycle. During the discharge period, which is determined by $R_2C_0$, the output stays low, allowing a digital output waveform to be generated. If $R_1$ is made very small in value compared with $R_2$, the output becomes a square wave. As it is in the low-frequency oscillator circuit, the waveform across $C_0$ in a timer circuit is an exponential ramp.

When the circuit of Fig. 2a is combined with a one-shot multivibrator circuit, a voltage-to-frequency converter is the result. As shown in Fig. 9, the voltage comparator first compares the input voltage $V_I$ with $V_B$. When $V_I$ is greater than $V_B$, the comparator turns on the multivibrator, whose output will then go low for a timing period T, causing current source $I_0$ to turn on. At the end of the period, the multivibrator output goes high and $I_0$ is turned off.

## V-f converter cycling

As long as $V_B$ is not greater than $V_I$, the multivibrator keeps turning on and off for T-length durations until a sufficient charge (determined by the product of $I_0$ and T) is injected into the $R_B$ and $C_B$ network to cause $V_B$ to become higher than $V_I$. When that happens, $I_0$ stays off and $V_B$ decays until it equals $V_I$. This completes one cycle, and the V-f converter runs in a steady-state mode.

In the steady-state mode, $I_0$ charges $C_B$ fast enough to keep $V_B$ equal to or greater than $V_I$. Since the discharge rate of $C_B$ is proportional to $V_B/R_B$, the frequency at which the circuit runs is proportional to the input voltage. The circuit's output is a series of pulses, with the length of durations, T, determined by the external RC components of the multivibrator. □

# Intelligent buffer reconciles fast processors and slow peripherals

First-in–first-out device speeds communication between multiple microprocessors and shared peripherals

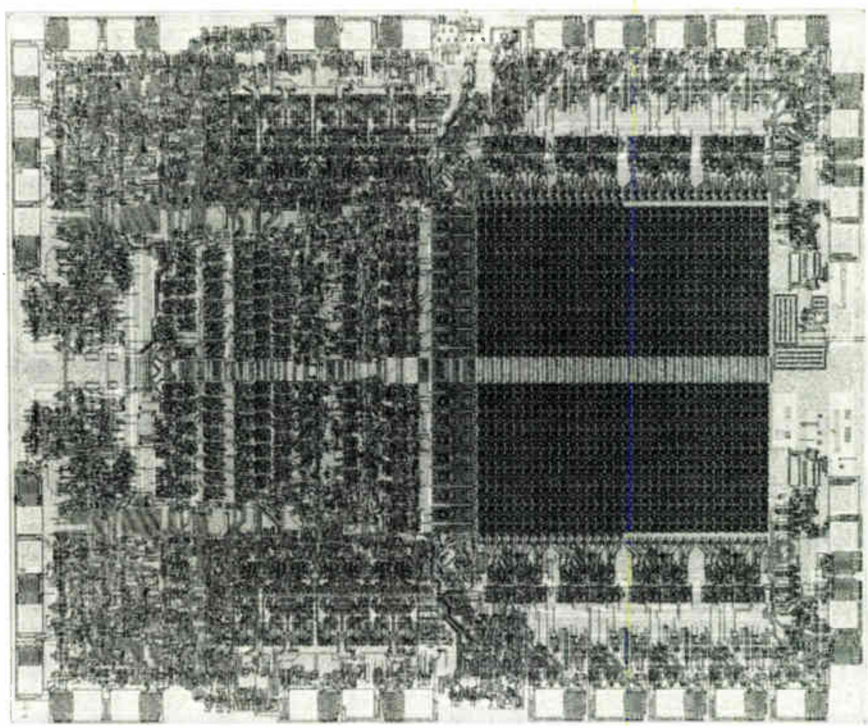
by Daniel L. Hillman, *Zilog Inc., Cupertino, Calif.*

☐ Putting two or more microprocessors to work on a given set of tasks is now a practical system design approach. Special input/output processors are used increasingly, as are those devoted exclusively to number crunching. But a way of coordinating their activities has been needed, and now the ZFIO, a special data buffer, has arrived to solve that problem.

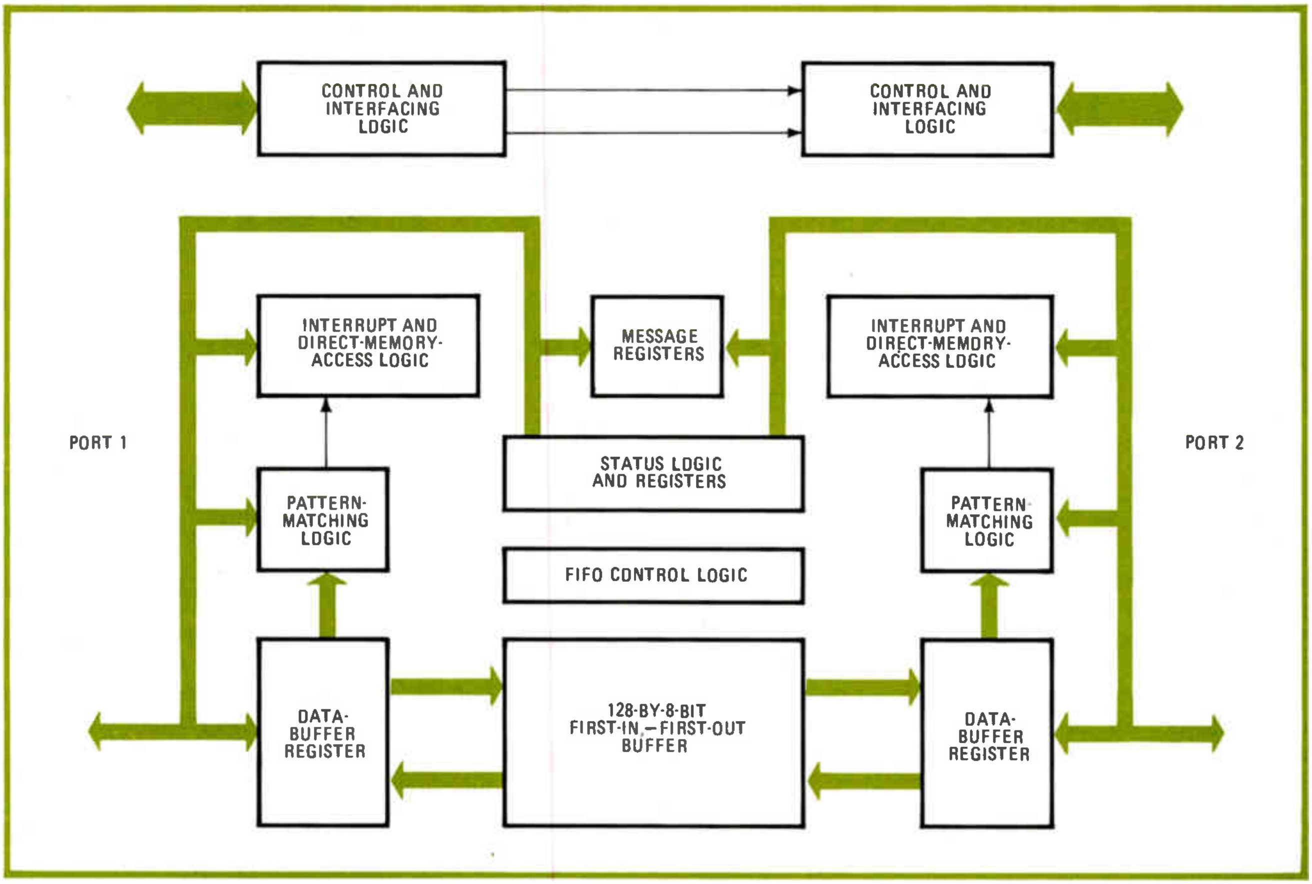
Of course, software must be developed to segment and assign tasks, but equally important, hardware must synchronize devices that operate independently, often at different data rates. The ZFIO enhances system throughput as it accepts and delivers data simultaneously. Moreover, it generates interrupts to notify devices of data availability. The ZFIO is a 128-by-8-bit first-in–first-out (FIFO) buffer memory that includes programmable interfaces with various computers and input/output devices; it forms an elastic link that allows each device to read or write at its own speed. For example, a Z8000 can execute a high-speed block move to fill the ZFIO buffer. The data can then be read out on the other side of the memory at the data rate of a slow peripheral such as a line printer or disk. But even when two devices can operate at the same data rate, it is not always possible for both to operate synchronously. The ZFIO chip provides the necessary data buffering in this case as well.

With its large data buffer, the device can reduce I/O overhead by as much as two orders of magnitude. It supports direct-memory-access (DMA) devices for high-speed data transfers, generates programmable interrupts, and coordinates fast asynchronous block data transfers. What's more, the depth of buffering can be increased to any desired depth in 128-byte increments by adding the ZFIFO, which is essentially the buffer portion of the ZFIO in a 28-pin package.

The chip manages data transfers on a multiplexed (address/data) bus, a nonmultiplexed bus, the standard two-wire (request/acknowledge) handshake port, or the three-wire handshake port used by the IEEE-488 instrumentation bus. Devices running at different speeds and using different interfaces can thereby transfer data.



**Built-in smarts.** There is more to this chip than just a first-in–first-out memory; the die area taken up shows how much intelligence is built into the device. Control logic, as well as several internal control and message registers, make byte comparisons and generate programmable interrupts.




**1. Details.** The ZFIO contains a data buffer comprising 128 bytes of dual-port RAM, the interface logic for various buses, message registers for controlled communication, and the logic for generating unique interrupts under several different conditions.

The buffer (Fig. 1) is implemented with an internal dual-port random-access memory. The RAM is addressed by a read counter and a write counter, a technique that has the advantage of showing the exact number of bytes of valid data in the buffer as the difference between the read count and the write count. The exact number of bytes can be read out by either device. In addition, by comparing the difference with a programmable number in the byte-count register, an interrupt can be automatically requested or a DMA transfer started at a specified level of buffer fullness.

### Bypassing the buffer

When two microprocessors are linked together, it is often necessary for them to exchange information other than blocks of data. Two message registers, IN and OUT, allow bypassing of the buffer. A message can be written by one microprocessor that causes an interrupt request, if enabled, to be sent to the other microprocessor. The message might be the length of the file being transferred or an end-of-file character to stop the transfer.

With the versatile ZFIO interface, the most common bus structures are supported by making the control pin definitions programmable (see table). Pins $M_1$ and $M_0$ program the port 1 side, and 2 bits, $B_1$ and $B_0$, in one of port 1's registers, program the port 2 side. In all operating modes, the port 1 side is always a computer interface. It is possible to use port 2 as either as a computer interface or as an I/O port with handshake.

With the multiplexed address/data bus, the width of the memory can be increased beyond 8 bits (Fig. 2). The low-byte mode is used on $AD_0$–$AD_7$ lines, the high-byte mode on lines $AD_8$–$AD_{15}$. A 32-bit bus can be similarly accommodated. The $A_0$–$A_3$ pins, which are attached to $AD_0$–$AD_3$ on all high-byte ZFIOs, provide direct addressing of all internal registers.

An address-strobe ($\overline{AS}$) pin is used to latch address and chip-select information. A read/write pin and a data strobe pin are used just as in reading and writing normal memory locations.

In the nonmultiplexed version, the control/data ($C/\overline{D}$) pin is used to access the FIFO buffer directly (when $C/\overline{D} = 0$). Reading or writing into other control registers is done in two steps. First, the desired register number is written into the pointer register, with $C/\overline{D} = 1$. Secondly, the register indicated by the pointer register is read from or written into with $C/\overline{D} = 1$. The chip allows continuous monitoring of the status bits by doing a control read, where $C/\overline{D} = 1$.

### Handling interrupts

The ZFIO supports Zilog's prioritized daisy-chain interrupt protocol as well. Each of its sides, when configured as a computer interface, can interrupt its respective microprocessor for any of the following reasons: a write into the message register (by the other microprocessor), a change in the direction of data through the buffer, a pattern match, a byte-count match, an overflow/under-

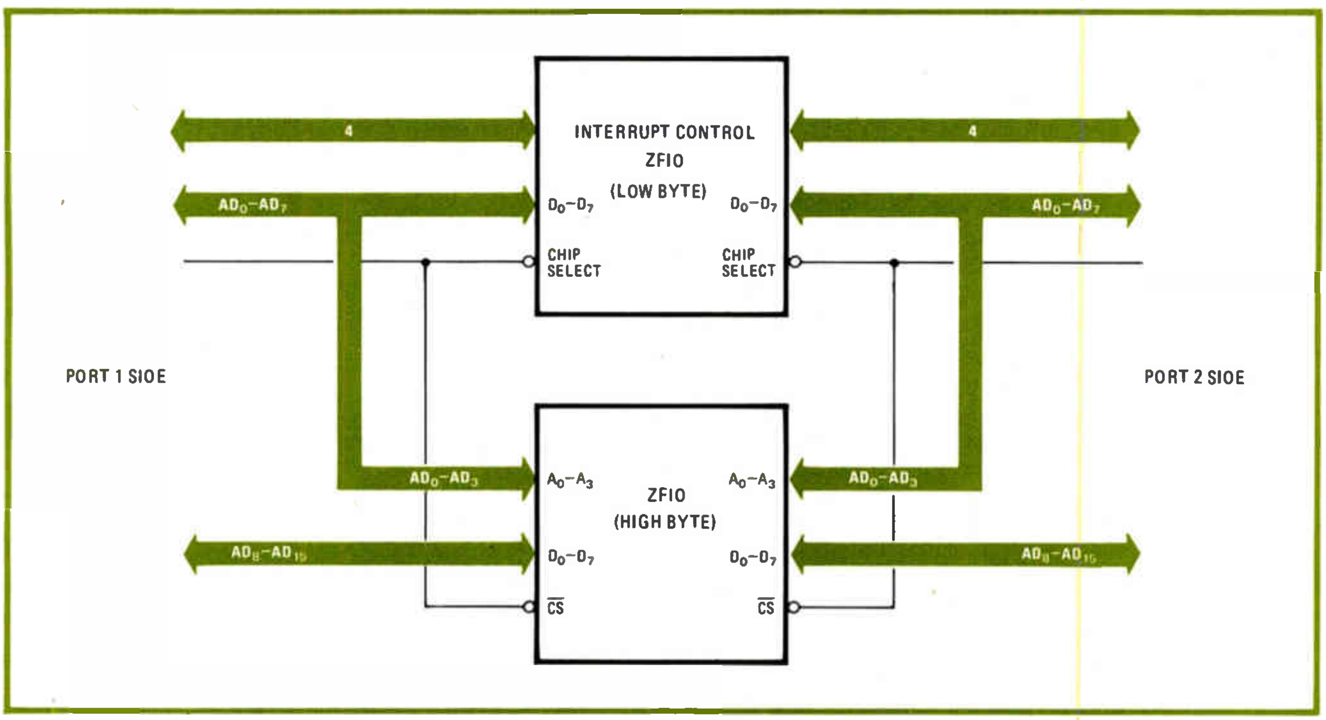
| OPERATING MODES FOR ZFIO DATA BUFFER | | | | | | |
|---|---|---|---|---|---|---|
| Mode | Port 1 programming | | Port 2 programming | | Port 1 pin definition | Port 2 pin definition |
| | $M_1$ | $M_0$ | $B_1$ | $B_0$ | | |
| 0 | 0 | 0 | 0 | 0 | multiplexed bus, low byte | multiplexed bus, low byte |
| 1 | 0 | 0 | 0 | 1 | multiplexed bus, low byte | nonmultiplexed |
| 2 | 0 | 0 | 1 | 0 | multiplexed bus, low byte | three-wire handshake |
| 3 | 0 | 0 | 1 | 1 | multiplexed bus, low byte | two-wire handshake |
| 4 | 0 | 1 | 0 | 0 | multiplexed bus, high byte | multiplexed bus, high byte |
| 5 | 0 | 1 | 0 | 1 | multiplexed bus, high byte | nonmultiplexed |
| 6 | 0 | 1 | 1 | 0 | multiplexed bus, high byte | three-wire handshake |
| 7 | 0 | 1 | 1 | 1 | multiplexed bus, high byte | two-wire handshake |
| 8 | 1 | 0 | 0 | 0 | nonmultiplexed | multiplexed bus, low byte |
| 9 | 1 | 0 | 0 | 1 | nonmultiplexed | nonmultiplexed |
| 10 | 1 | 0 | 1 | 0 | nonmultiplexed | three-wire handshake |
| 11 | 1 | 0 | 1 | 1 | nonmultiplexed | two-wire handshake |

flow error, or buffer-full and buffer-empty status. Each interrupt source can be independently enabled or disabled and can place a unique interrupt vector on the data-bus lines.

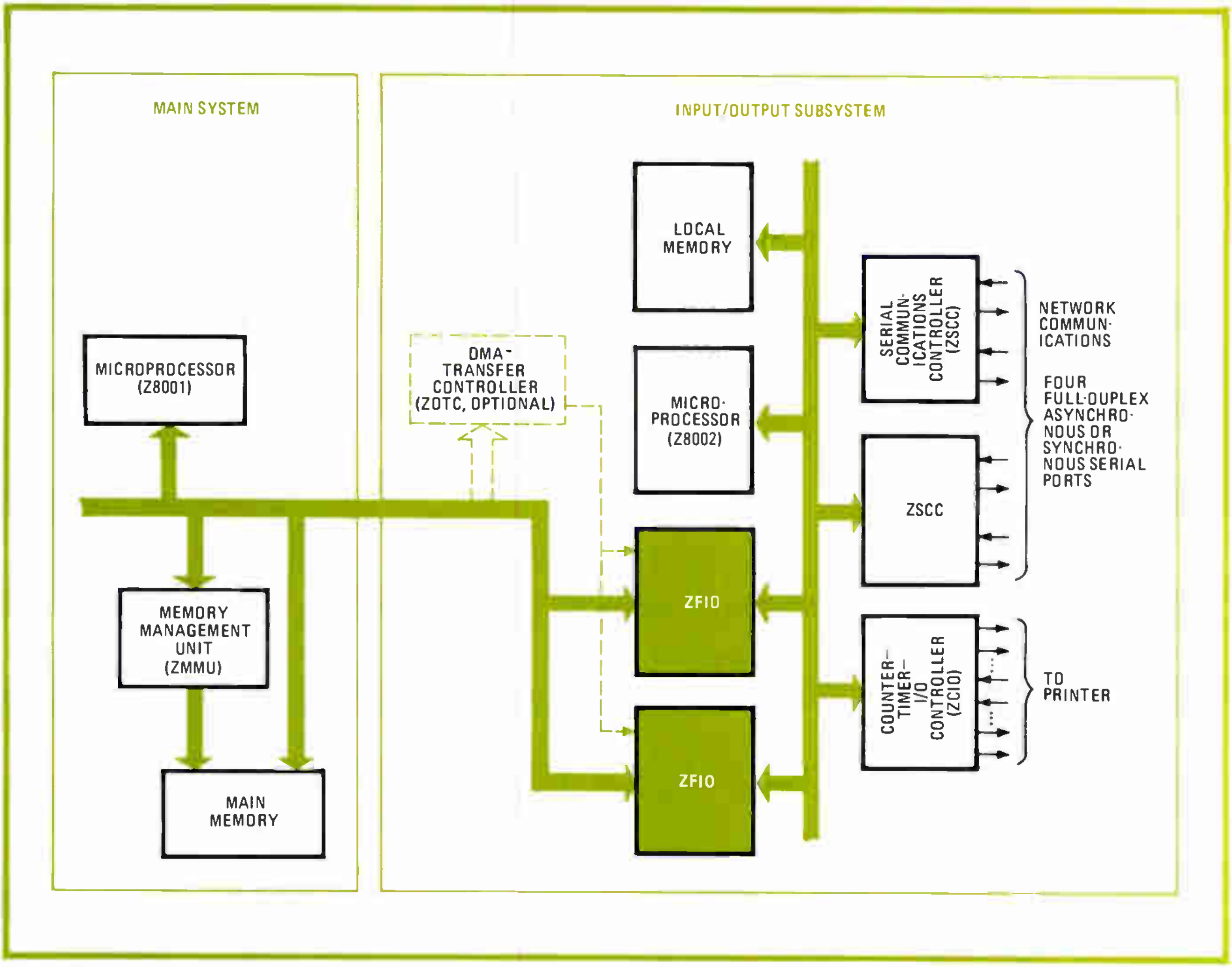
The ZFIO is particularly well suited to work with a DMA device in both multiplexed and nonmultiplexed modes. A transfer of data between the chip and system memory can take place every machine cycle, eliminating the typical two-cycle I/O-to-memory transfer sequence—that is, reading from I/O and then writing into memory. In addition, DMA can be used by both sides of the buffer simultaneously, with the DMA device supplying memory address and read/write information and the buffer supplying or receiving data. In this way, transfers can be made into and out of memory at nearly the full bandwidth of each bus—a desirable feature because it reduces the time that I/O traffic ties them up.

A special pin (and mode) gives buffer-status information. When data is moved into the memory, the request pin ($\overline{\text{REQ}}$) is active until the buffer is full. It then goes inactive until the number of bytes in the buffer is less than a value programmed in the byte-comparison register. $\overline{\text{REQ}}$ then goes active and the sequence begins again. When data is moved out of the device, the request signal is inactive until the number of bytes in the buffer is greater than the value programmed in the byte-comparison register. It then goes active and stays active until the buffer is empty. The request then goes inactive and the sequence starts over. The system designer can use this pin—and the byte-comparison value—to optimize the number of DMA requests issued.

An I/O subsystem may be linked to a main system via

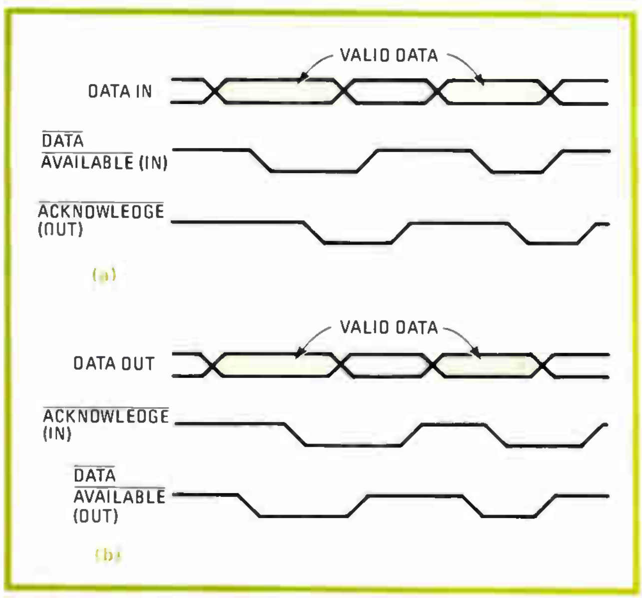



**2. Parallel ZFIOs.** Any data path that is a multiple of eight can be handled by adding more ZFIOs in parallel. Depth of buffering beyond 128 bytes can be accomplished by adding ZFIFOs—essentially the same as the buffer portion of the ZFIOs but housed in 28-pin packages.

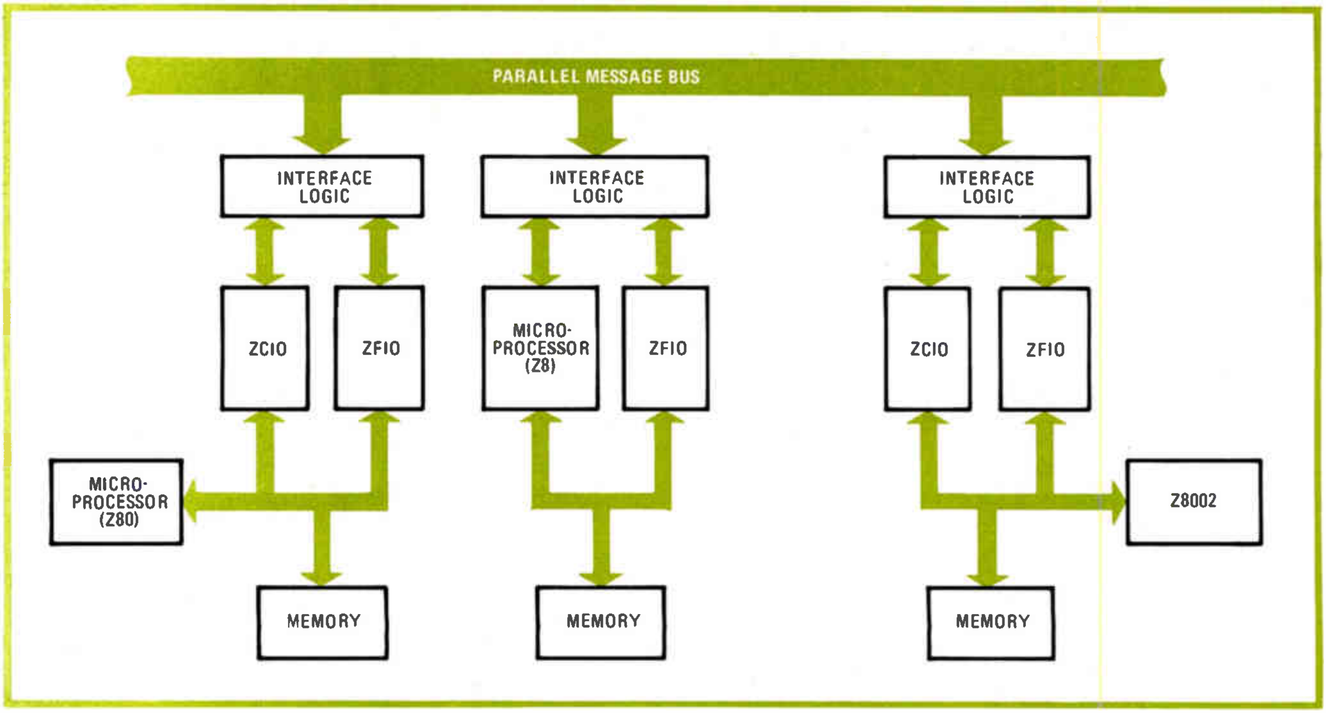



**3. Building a high-end system.** A single main processor (Z8001) uses two paralleled ZFIOs to communicate with the second processor (Z8002), which coordinates I/O subsystem data transfers. The ZSCCs provide four serial ports and the ZCIO handles the printer.

two ZFIO chips. In Fig. 3 a Z8002 is used as the I/O processor, handling all low-level peripheral control as well as buffering of data. Four full-duplex serial ports are supported by the ZSCC, which provides the network with synchronous and asynchronous communications. The ZCIO supports the I/O subsystem line printer. The main computer (Z8001) sends high-level commands to the I/O subsystem through the two message registers. These commands include intended destination of the data, block length, and other relevant information. The Z8001 and Z8002 can do a block-I/O move, allowing one instruction to transfer a block of data between an I/O device and memory. The main computer starts a block I/O move into the two ZFIO memories; if the subsystem is not ready at that time to read the data, the ZFIOs will interrupt the main computer when the buffer is full, suspending the block move and freeing it for other tasks until it is interrupted again. After the subsystem starts reading data, a second interrupt to the main computer will occur on byte-count-match when the buffer is emptied to a predetermined programmable level. The subsystem can use the ZFIO's interrupt capability in a similar fashion, to avoid waiting for data transfers from the main system.




**4. Two-wire handshake.** Handshaking is available on the port 2 side. Request line (marked data available) for inputs (a) signals receiver that valid data is being transmitted. Outputs (b) also generate a request, and both wait for acknowledges before changing data.




**5. A multiprocessor application.** In a loosely coupled multiprocessor situation, a very long message bus can be supported because it can run at relatively low speed. The ZFIOs handle the necessary speed conversion so that the processors are not slowed down during I/O.

A DMA transfer controller (ZDTC, shown as optional in Fig. 3) provides the fastest data transfer. The main system ZDTC can be set up and begin transferring data to the two buffers. When one is full, the request signal goes inactive, allowing the main system to do other tasks while the I/O system reads the data. This bursting of data can continue until the entire block is transferred. The chip can then activate a request signal when the buffer is nearly empty, allowing the I/O system to do a continuous block move of data.

## Controlling communications

The data-direction bit controls the flow of data in the buffer. For proper system control, the port 1 computer programs the side of the memory that controls the data-transfer direction, in addition to enabling the interrupt signal.

In the computer-to-I/O mode, the direction of data transfer can be under software control by port 1 or hardware control by port 2. With data direction under port 1's control, port 2's data-direction pin is an output. This output is useful for managing other ZFIOs or external bidirectional bus drives. When it is controlled by port 2, the data-direction pin is an input giving control of the data flow to external hardware.

The clear bit zeros out the data buffer without resetting the ZFIO. For system control, port 1's computer programs the side that can clear the buffer. In the computer-to-computer mode, software controls the clear operation in both computers. In the computer-to-I/O mode, clearing can either be under software control by port 1's computer or hardware control by external logic. When port 1 controls the clear operation, port 2's CLEAR pin is an output. This output is useful to clear other ZFIOs or to initialize external logic. When the clear operation is controlled by port 2, the CLEAR pin is an input that allows for external logic to clear the buffer.

In the two-wire interlocked handshake, the ZFIO's action must be acknowledged by the other half of the handshake before the next action can take place (Fig. 4). For example, an output handshake will not indicate that new data is available until the external device shows it is ready for the data. Similarly, an input handshake will not show that it is ready for new data until the data source indicates that the previous byte is no longer available, thereby acknowledging the input port's acceptance of the last byte. The two-wire handshake is useful for interfacing with typical I/O devices.

The three-wire handshake is for applications in which one output port is communicating simultaneously to many input ports. It is basically the same as the interlocked handshake, except that two signals indicate that an input port is ready for new data or that it has accepted the present data. In the three-wire handshake, the handshake lines of many input ports can be bused together with open collector drivers to form a wired OR. In this way they can indicate whenever any or all of the devices are ready. This handshake is used in the IEEE-488 instrument bus. Since the port's direction can be changed under software control, bidirectional transfers can be made.

In a loosely coupled multiprocessor application, the ZFIO chip gives the speed buffering necessary for a very long message bus (Fig. 5). The interlocked two-wire handshake for transfer between two systems only or the three-wire handshake for transfers among more than two systems can be used. The ZCIOs are used for address recognition and bit manipulation of other control signals. After the link is established, the data is transferred via the ZFIOs. □

# Train speed controller ignores track resistance

by Stephen H. Burns
*U. S. Naval Academy, Electrical Engineering Department, Annapolis, Md.*

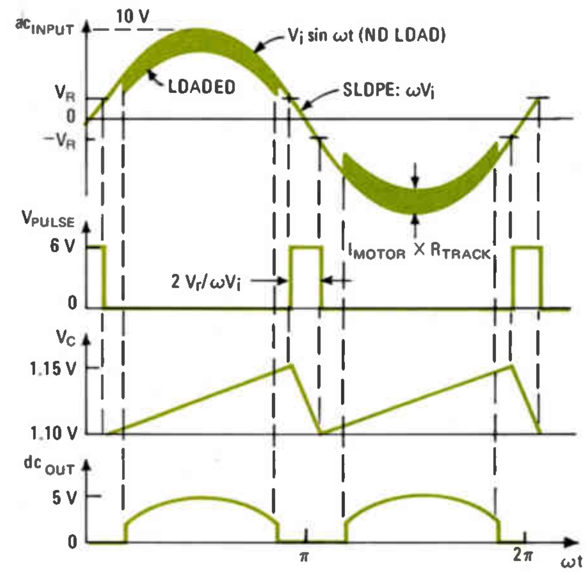
Because it keeps the voltage applied to any universal motor constant and independent of line resistance for a given line voltage, this circuit will be especially attractive for use with model trains, for which it will maintain speed independently of the resistive joints in the tracks. No modification of the speed-controlling transformer used with the trains is required.

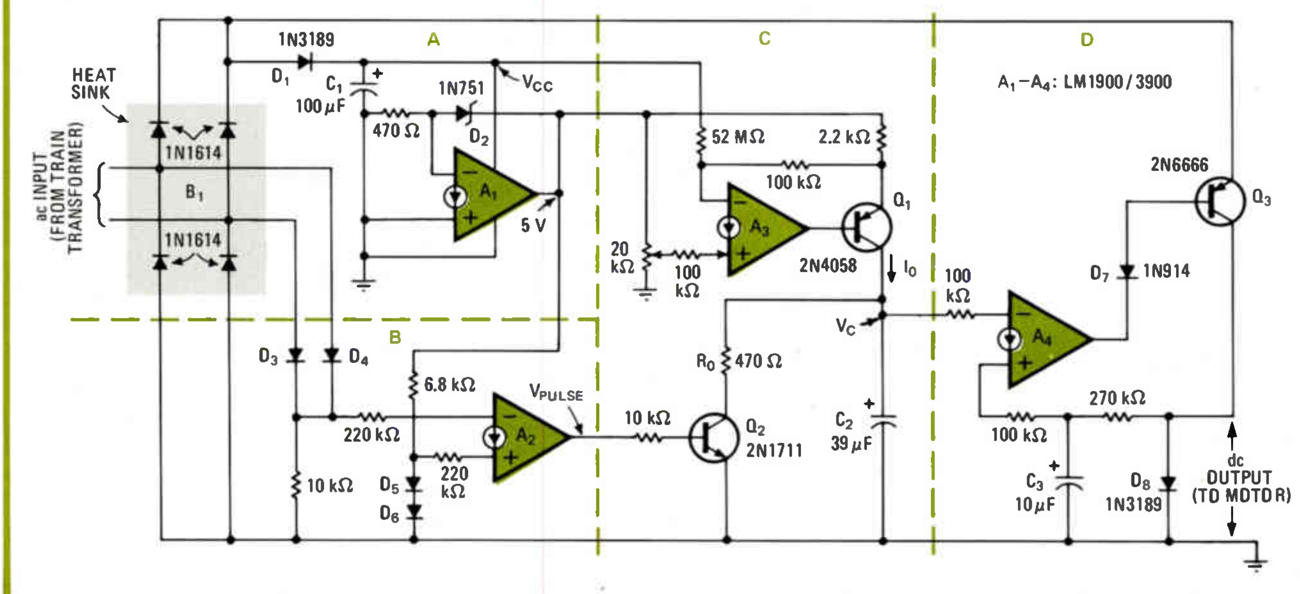
This circuit rides within or near the locomotive and is inserted in the electrical path between the motor and the track pickup and return. Thus it is necessary to connect the ac input of this circuit to the track pickup and frame of the locomotive and to connect the dc output of the circuit across the motor windings. This way the circuit develops a constant average voltage across the motor for a given transformer setting.

This is accomplished with a four-section circuit, with block A containing the supply for powering the unit. Blocks B and C derive a gate pulse inversely proportional to the magnitude of the input voltage and a control voltage proportional to the input signal so that motor speed can be set. Block D handles the power-switching function.

Diode bridge $B_1$, diodes $D_1$ and $D_2$, capacitor $C_1$, and Norton amplifier $A_1$ constitute block A, which is actually a three-stage supply. $B_1$ provides full-wave rectified dc for power stage $Q_3$ and $D_1$ and $C_1$ extract and filter power for $A_1$–$A_4$. Zener diode $D_2$ and $A_1$ provide a regulated 5 volts for current source $Q_1$ and to establish a switching reference voltage for amplifier $A_2$.

In operation, $B_1$ and $Q_3$ electrically disconnect the motor from the power source near each zero crossing of the ac input. At this time, a pulse is developed at the output of $A_2$, its width equal to $P = 2V_r/\omega V_i$, where $V_r$ is the switching reference voltage, $\omega$ is $120\pi$ radians/sec,




**Rail tamer.** Controller keeps driving voltage to model trains independent of the resistance in the track joints. Output voltage is derived from pulses whose widths are inversely proportional to the ac input, generated at zero crossings so that load variations on the line are disregarded. Timing diagram details the operation.

and $V_i$ is the input voltage (see timing diagram). Note that by sampling near the zero crossings, the width of the pulse is made independent of the load on the ac line. One sense diode, $D_3$ or $D_4$, reference diodes $D_5$ and $D_6$, and one bridge diode set the switching threshold, $V_T$. This reference voltage is thus equal to four diode drops, or approximately 2 V.

$A_3$, $Q_1$, and $Q_2$ develop from the pulse a control voltage, $V_c$, whose average value can be expressed as $V_c = \pi I_o R_o V_i/(2V_T)$. $A_3$ and $Q_1$ constitute a 0.3-milliampere ($I_o$) constant-current source. A total resistance of 52 megohms placed in series between $V_{cc}$ and the inverting input of $A_3$ was found best to compensate for changes in $I_o$ versus supply variations.

The power switching stage includes feedback capacitor $C_3$, amplifier $A_4$, isolation diode $D_7$, damper diode $D_8$, and $Q_3$. $C_2$ and $C_3$ were selected so that $Q_3$ switches efficiently under all load conditions. Smaller values of $C_2$ result in more efficient switching but increase output resistance. Larger values of $C_3$ will result in greater overshooting in response to a transient.

With a source voltage of from 7 to 25 V rms and a load of 10 ohms, the circuit will generate an output of from 3 to 12 V. Increasing the line resistance from 0 to 4 Ω will cause a typical change in output voltage of only 0.1 V for a line drop of several volts. □

## Two-chip generator shapes synthesizer's sounds

by Jonathan Jacky
*Seattle, Wash.*

Generating the same adjustable modulating waveforms for a music synthesizer as the circuit proposed by Kirschman[1], but using only two integrated circuits, this generator also works from a single supply. It has, in addition, separate gate and trigger inputs for providing a more realistic keyboard response.

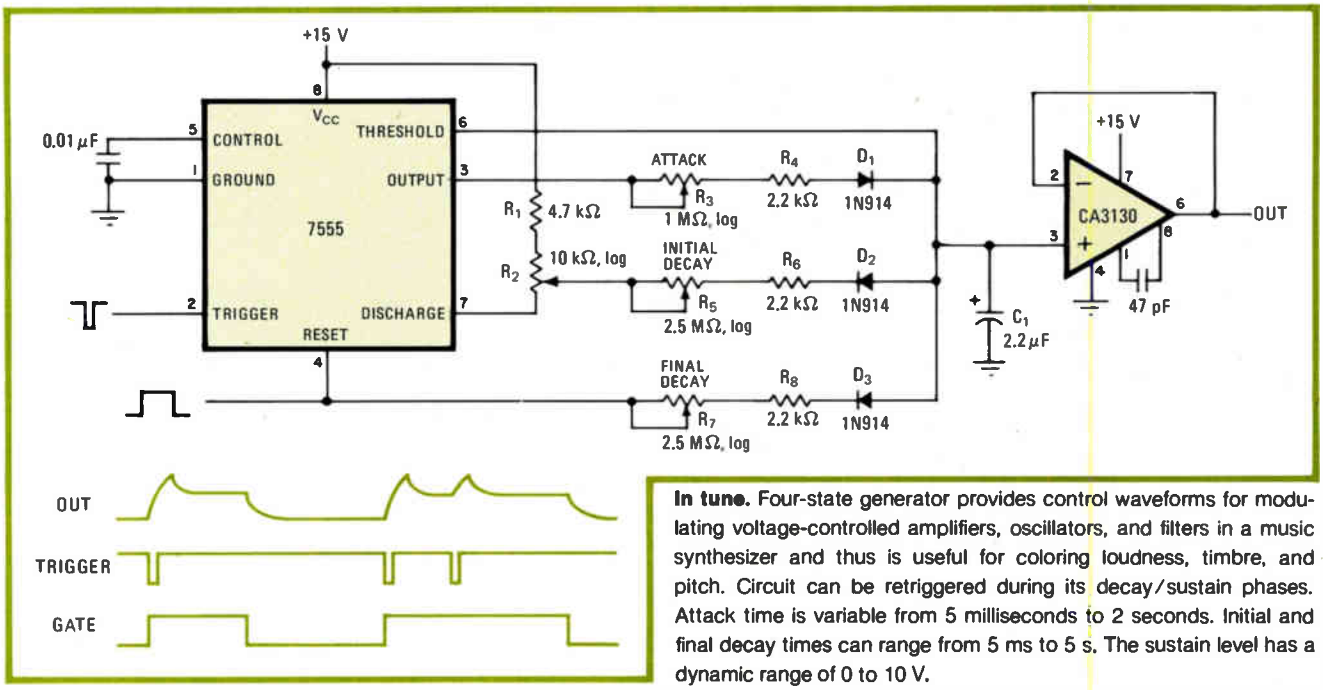
When gated or triggered, the generator, which is built around Intersil Inc.'s C-MOS 7555 timer, produces a waveform that passes through four states:

- An exponential attack.
- An initial decay, or fallback.
- A sustain, or steady dc level.
- A final decay, or release.

Each of these four parameters is continuously variable, so that waveforms having a wide variety of shapes can be generated.

The waveforms are generated by the sequential charging and discharging of capacitor $C_1$. Here, the 7555 controls the sequencing while diodes switch the currents, unlike Kirschman's circuit where comparators and flip-flops control the stepping and analog switches steer the currents. Furthermore, the 7555 is well suited for handling the two logic signals provided by most synthesizer keyboards—the gate, which is high as long as any key is depressed, and the trigger, which provides a negative pulse as each key is struck. The gate and trigger features eliminate the need to release each key before striking the next to initiate an attack phase.

In the dormant state (the gate input at pin 4 of the 7555 is low), capacitor $C_2$ is discharged. When the gate goes high and a trigger pulse appears at pin 2, the 7555 output (pin 3) goes high and charges $C_1$ through $R_3$, $R_4$, and $D_1$, producing the attack segment of the waveform. Note that diode $D_2$ is reverse-biased because pin 7 of the 7555 is high and that diode $D_3$ is back-biased by logic 1




**In tune.** Four-state generator provides control waveforms for modulating voltage-controlled amplifiers, oscillators, and filters in a music synthesizer and thus is useful for coloring loudness, timbre, and pitch. Circuit can be retriggered during its decay/sustain phases. Attack time is variable from 5 milliseconds to 2 seconds. Initial and final decay times can range from 5 ms to 5 s. The sustain level has a dynamic range of 0 to 10 V.

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signal applied to the gate input.

When the voltage across $C_1$ reaches 10 volts, pin 3 of the 7555 goes low and pin 7 is grounded, terminating the attack phase. $D_1$ and $D_3$ are now reverse-biased and $C_1$ discharges through $D_2$, $R_5$, and $R_6$ to produce the initial decay. The sustain level reached is determined by the voltage divider formed by resistor $R_1$ and potentiometer $R_2$. During this phase, a second attack can be obtained by striking another key (see timing diagram). When the last key is released, the gate goes low and $C_1$ will discharge through $D_3$, $R_7$, and $R_8$ to produce the final decay. The CA3130 operational amplifier serves as a buffer to protect $C_1$ from excessive loading. □

**References**

1. Randall K. Kirschman, "Adjustable e* generator colors synthesizer's sounds," Electronics, July 17, 1980, p. 123.

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.

# Multiplier increases resolution of standard shaft encoders

by Frank Amthor
*School of Optometry, University of Alabama, Birmingham*

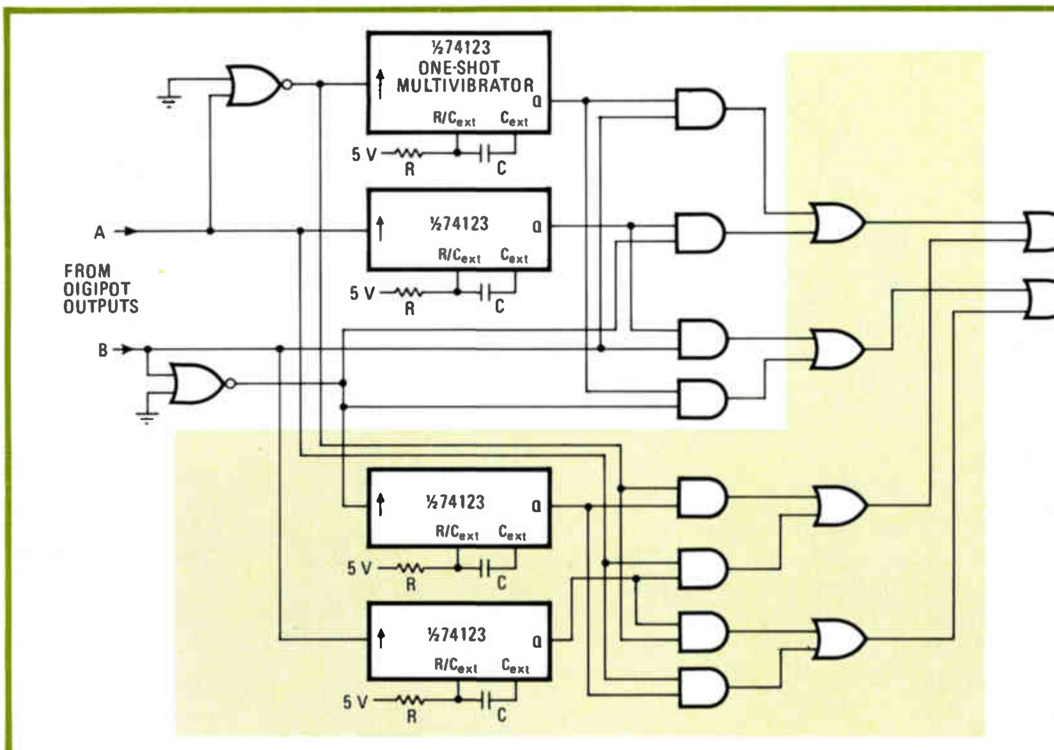
The resolution that can be attained by two-channel shaft encoders of the type used in speed controllers and optical-positioning devices may be increased by employing a digital frequency multiplier to derive a proportionally greater number of pulses from its TTL-compatible outputs. In this way, an up/down counter, which is normally driven by the encoder in these applications, can position the shaft more accurately and is more responsive to changes in speed and direction. Only two one-shot multivibrators and several logic gates are needed for the multiplier circuitry.

The circuit works well with a typical encoder such as the Digipot (manufactured by Sensor Technology Inc., Chatsworth, Calif.). In this case, the 128 square waves that are generated per channel for each shaft revolution (with output from the other channel in quadrature) are transformed to 512 bits per cycle.

When the shaft rotates in a clockwise direction, the output from port A of the encoder always leads the output from port B by 90°, and the logic will generate pulses only to the up input of the counter on both edges of both channel outputs. Thus, four pulses per square wave are generated. Rotation speed is limited by the duration time of the positive-edge–triggered one-shots, which should be kept to a few microseconds or less. Note that both the count-up and the count-down inputs of the counter are normally held high.

On the other hand, when the shaft's rotation is in a counterclockwise direction, the output of B leads that of A by 90°. In this case, four pulses per square wave are presented to the down input of the counter. □

**Increments.** Pulse multiplier yields 512 count-up or -down bits for 128 square-wave cycles (one revolution) from two-channel shaft encoder, for more resolution in speed controllers and optical positioning systems. Eliminating tinted area yields 256 bits per revolution.




| | Multiplier logic | |
|---|---|---|
| A | B | COUNT |
| ↑ | 0 | UP |
| ↓ | 1 | UP |
| 1 | ↑ | UP |
| 0 | ↓ | UP |
| ↑ | 1 | DOWN |
| ↓ | 0 | DOWN |
| 0 | ↑ | DOWN |
| 1 | ↓ | DOWN |

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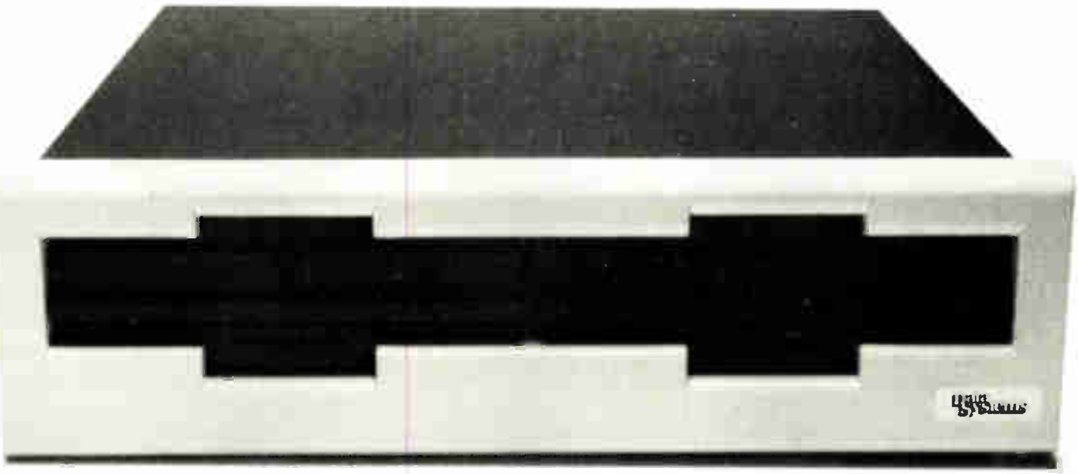

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Circle 140 on reader service card

# C-MOS makes voltage converter a paragon of efficiency

With inputs spanning 1.5 to 9 V dc, single chip delivers negative or positive multiples to within 0.1% and at an efficiency of 98%

by David Bingham, *Intersil Inc., Cupertino, Calif.*

☐ Single +5-volt power supplies are gaining in popularity. However, for circuits where input and output signals approach 10 V peak to peak—such as the new analog data-acquisition circuits using n-channel and complementary-MOS devices on one or more chips—an additional −5-V supply is needed.

Generating a −5-V supply is typically expensive and inefficient. Usually, a large number of discrete and integrated-circuit components (for example, timers and discrete resistors, capacitors, and diodes) are needed to convert the common +5-V line into a negative one.

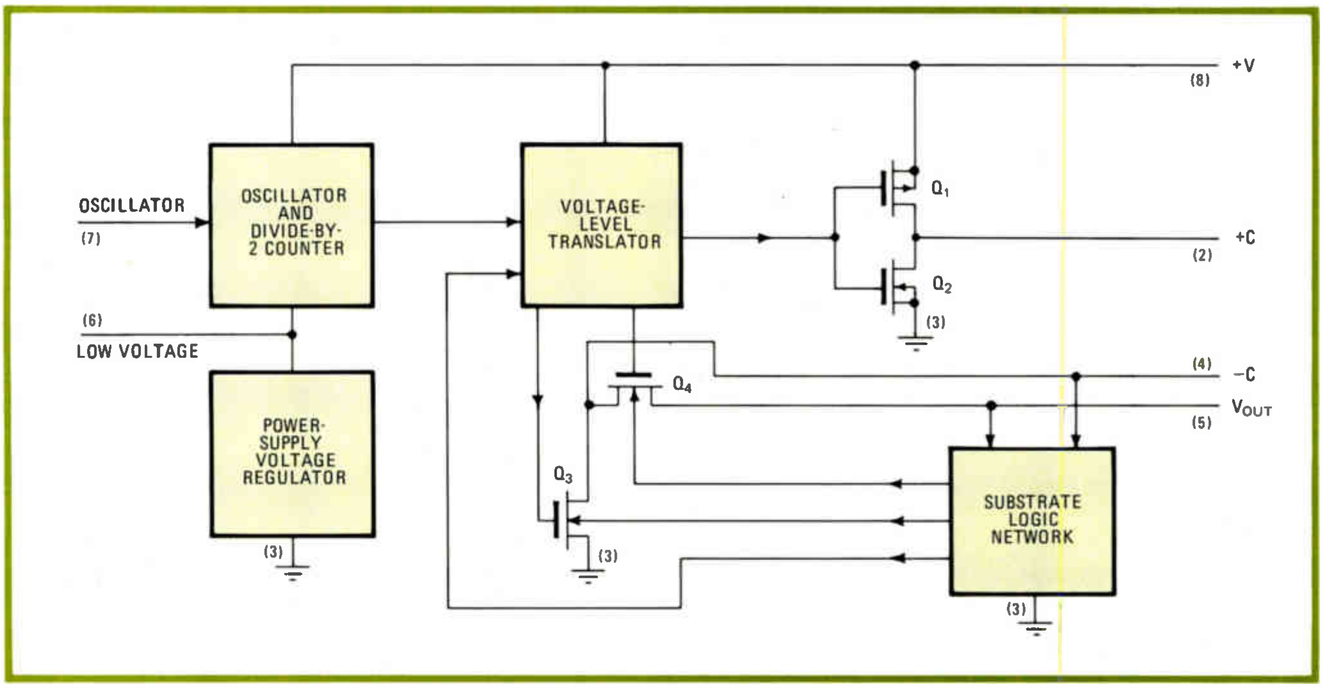
Drawing upon its considerable experience in making C-MOS ICs, Intersil has come up with a dc voltage converter chip that eliminates the disadvantages of other voltage-conversion methods [*Electronics*, Oct. 11, 1979, p. 212]. Accepting inputs from 1.5 to 9 V dc, the ICL7660 delivers an output equal to the negative of the input voltage to within 0.1%. Capable of producing 20 milliamperes, the device has a power-conversion efficiency of about 98% for load currents of 2 mA and higher and is aimed at low-power secondary power-supply lines like the −5-V line in ±5-V supplies. The use of two or more 7660s extends the device's capability.

Since the 7660 also multiplies a voltage, either positive or negative, by a factor of two, it can be considered a simple voltage doubler. It differs from most voltage doublers in that the usual blocking diodes are replaced by on-chip active n-MOS transistor switches. The 7660's high conversion accuracy is due to the transistor switches' low offset voltages and currents. Voltage-doubling accuracy approaches 100% with no loads.

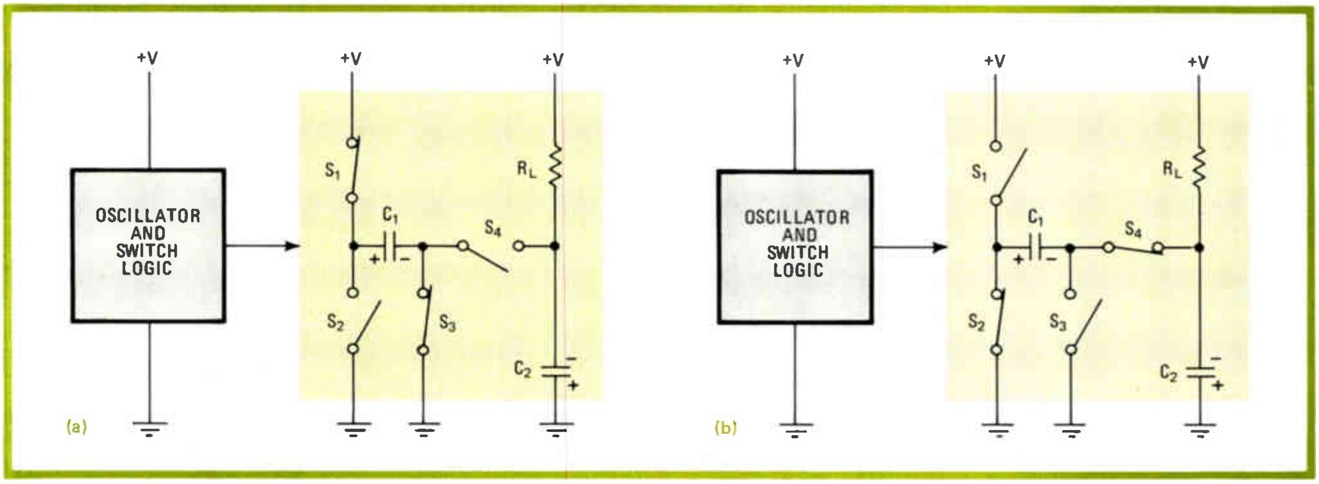
## Capacitors needed

The 7660 contains all the necessary conversion functions on chip, save for pump and output reservoir capacitors, which are needed externally. These capacitors are about 10 microfarads in value, and capacitors with such large values are unsuitable for integration on the same chip as the voltage converter.

The device is made with a low-threshold C-MOS tech-




**1. Efficient.** Oscillator, level translator, voltage regulator, and substrate biasing for the ICL7660 reside on a single complementary-MOS integrated circuit. The device is designed to convert conventional +5-volt supplies to −5-V outputs accurately—to within 0.1%.



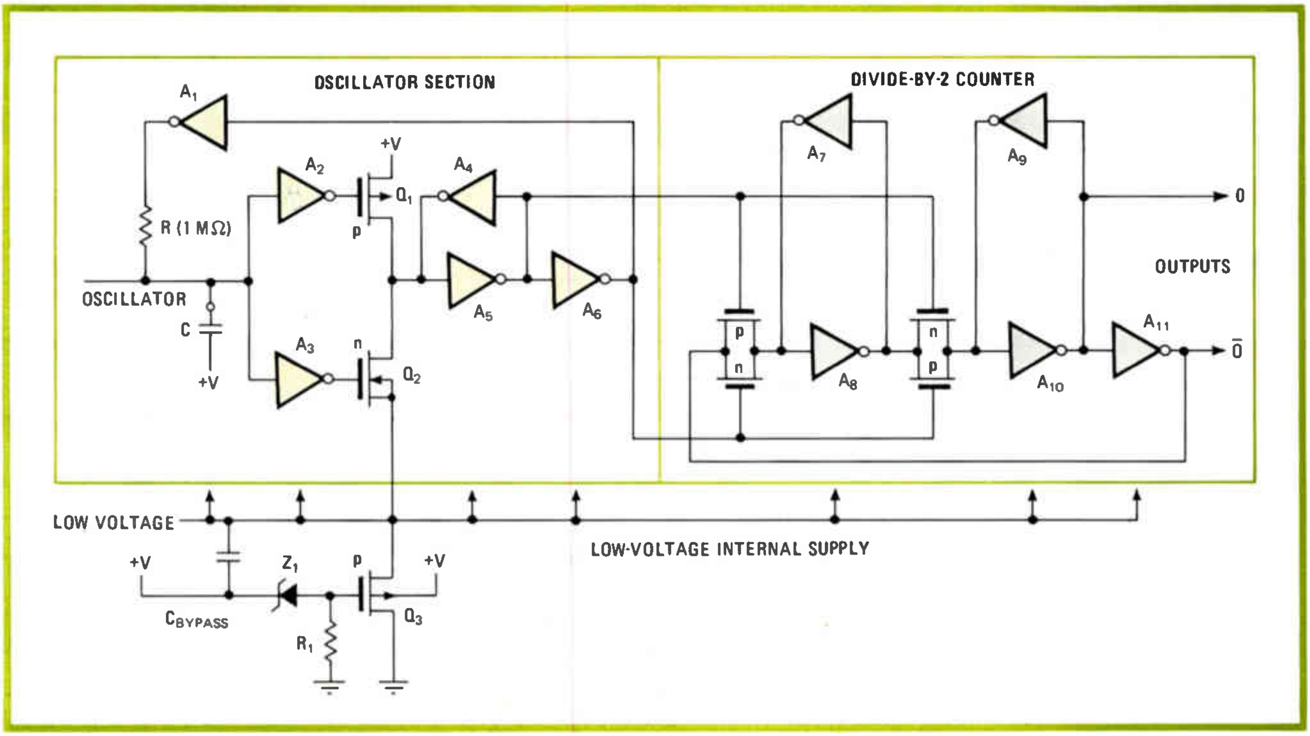

**2. Doubler.** The 7660 voltage-converter IC acts like a classic voltage doubler during charge (a) and pump (b) phases. Switches $S_1$–$S_4$ correspond to transistors $Q_1$–$Q_4$ of Fig. 1. In the classic voltage doubler, $S_3$ and $S_4$ are usually discrete silicon diodes and rectifiers.

nology using p- and n-channel transistors that turn on at 0.6 V. The low power dissipation, simplicity, and small chip size of C-MOS make it a near-ideal technology to use. The one C-MOS drawback of potential device failure due to its inherent latchup has been to a large extent solved in the 7660 and is not a problem for most operating conditions.

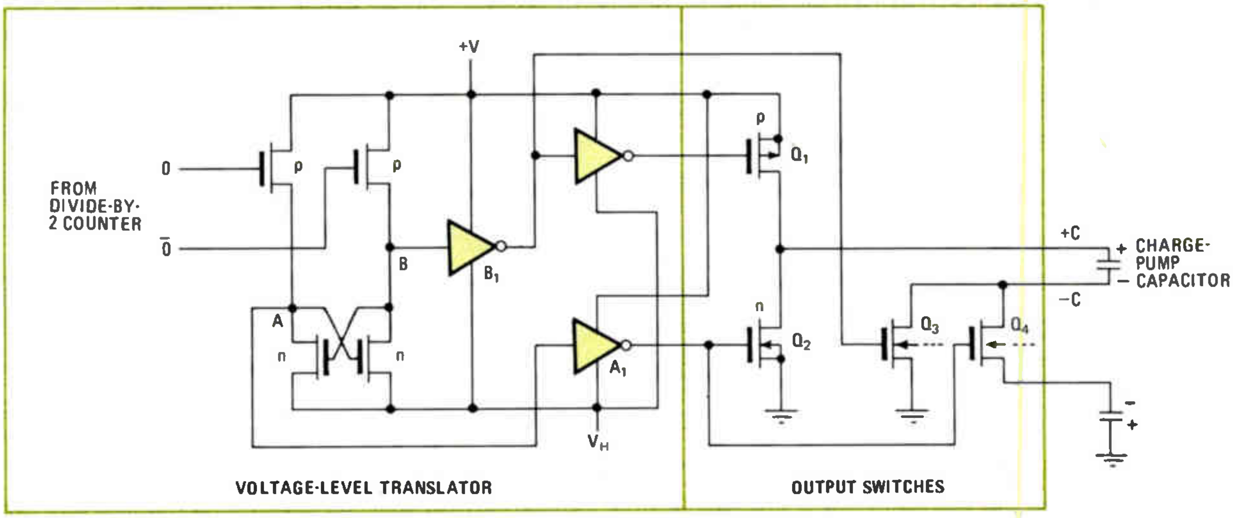
## A problem

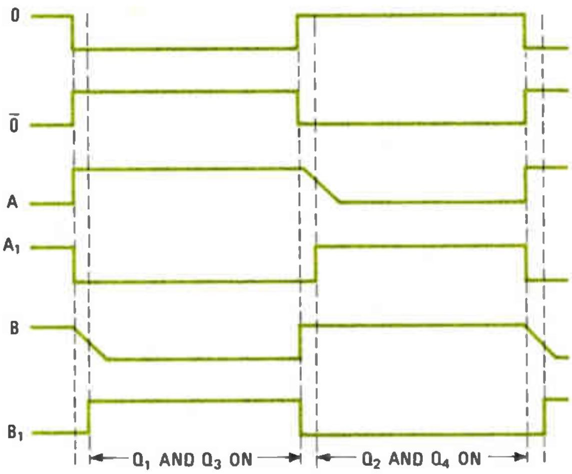
A C-MOS device is inherently a four-layer, or silicon-controlled-rectifier, structure. This structure can be turned on through the forward biasing of the inherent pn junctions, and unless external current-limiting circuitry is used, latchup and resultant failure can occur.

In a C-MOS structure, the n-channel transistor acts as the cathode of the SCR, and the $p^+$ source of the p-channel transistor acts as the anode. With a positive potential of about 2 V or more across the anode and cathode, the SCR can have either a low-impedance (on) or high-impedance (off) state. For the on state to occur, three things must happen: the product of the transistors' current gains, or betas, must be at least unity; a current greater than the holding current must be present; and a trigger pulse must be applied to either gate of the transistors. Trigger signals may be caused by static discharge on the gates or by connecting either transistor's gate to $G_1$ or to the power supplies before connecting power-supply lines to the other terminals of the SCR. Even extremely high rates of voltage change across any two or more SCR pn junctions can produce latchup.




**3. Oscillator.** The 7660's oscillator, with a natural frequency of 10 kHz, drives a conventional divide-by-2 counter that supplies an output signal and its complement. The counter supplies a 50% duty cycle output (at one half the input frequency) to the level translator.




**4. Translating.** The 7660's output switches are driven by signals provided by the voltage-level translator circuit. The voltage waveforms shown for output transistors $Q_1$–$Q_4$ are equal in amplitude to the sum of the output voltage and the power-supply voltage, +V.

Triggering a C-MOS SCR causes it to present an extremely low impedance (1 to 100 ohms) across the power supply. Unless the power supply is current-limited, the device latches up and is often destroyed, usually by the vaporization of one of the bonding wires used to connect the C-MOS chip electrically to the leads of its package.

## Preventing latchups

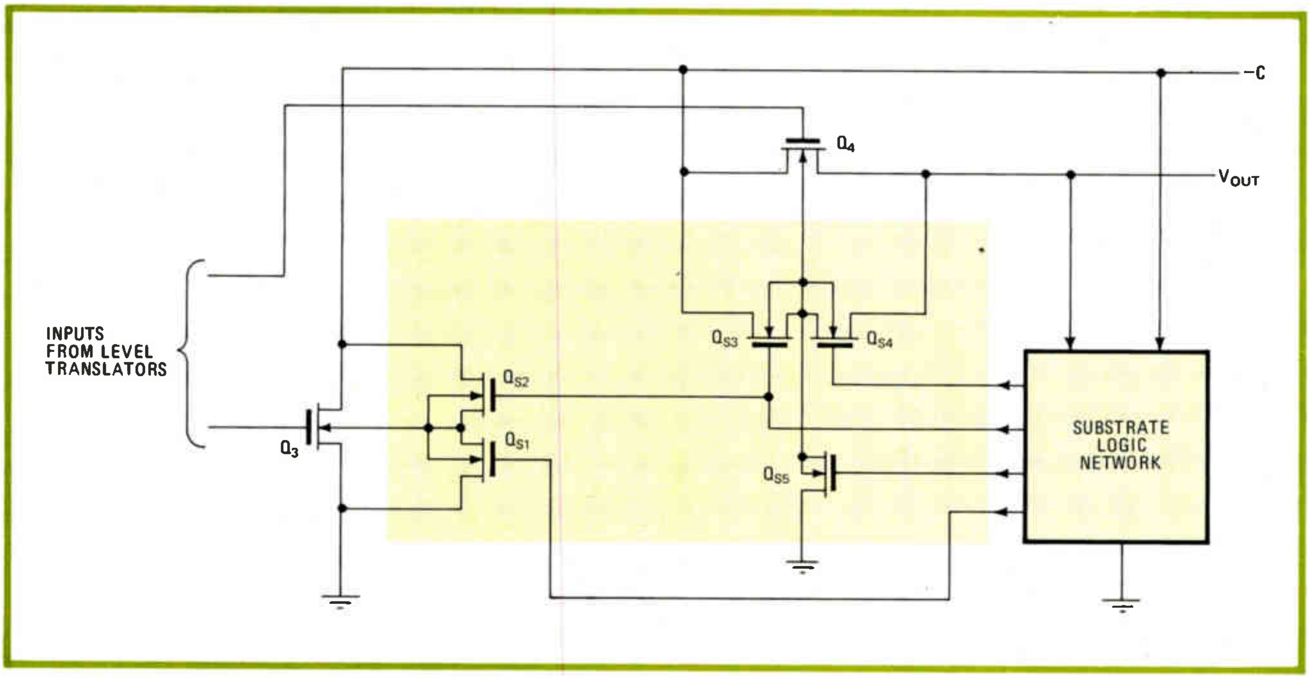
The 7660 is designed to minimize its susceptibility to latchup. It contains an RC oscillator, a series voltage regulator, a voltage-level translator, and a logic network (Fig. 1). The logic network senses the voltage on the sources and drains of the two output n-channel transistors $Q_3$ and $Q_4$ and ensures that their substrates are always correctly biased. Should the sources start to swing to more than −0.5 V with respect to the substrates, the substrate logic network acts to keep the substrate bias under +0.5 V and prevents the device from latching up.

The 7660's operation can best be understood by referring to Fig. 2. Switches $S_1$ through $S_4$ correspond to transistors $Q_1$ through $Q_4$ in Fig. 1. The oscillator and voltage-level translator sections provide the control signals to the four switches such that, during the charge phase (a), capacitor $C_1$ is charged through $S_1$ and $S_3$ to a voltage nearly equal to the supply voltage, +V. In the pump phase (b), $S_2$ and $S_4$ are closed and the charge is pumped and transferred from capacitor $C_1$ to $C_2$. Assuming no system losses, the voltage on $C_2$ is equal in value and opposite in polarity to +V with respect to ground. This circuit is a classic voltage doubler, where $S_3$ and $S_4$ are usually replaced by conventional silicon diodes or rectifiers. The load, shown connected between $V_{OUT}$ and +V, usually consists of operational amplifiers, comparators, and data-acquisition components; in some systems, the load may be ground.

The 7660's oscillator (Fig. 3) includes an RC network whose open-circuit natural frequency is about 10 kilohertz. The oscillator drives a conventional divide-by-2 counter whose principal function is to supply a 50% duty cycle output (at half the input frequency) to the voltage-level translator circuit. The conventional static counter requires a two-phase clock and supplies an output signal and its complement.

When the output of inverter $A_1$ is switched high, capacitor C charges positively until inverter $A_2$ (which has a high input-voltage trip point) switches its output low, to turn on transistor $Q_1$. $Q_1$ in turn forces the ratioed-inverter latch $A_4$–$A_5$ to switch its output low. C then discharges negatively until inverter $A_3$ (which has a low input-voltage trip point) switches its output high, turning on transistor $Q_2$. The output of $Q_2$ resets $A_4$–$A_5$ and restarts the cycle.

Since the oscillator has a high input impedance of about 1 megohm, either it may be driven from an external source such as a TTL gate or equivalent or its frequency may be lowered by the addition of an external




**5. Steering.** Transistors $Q_{S1}$–$Q_{S5}$, together with the substrate logic network, ensure that the substrates of output transistors $Q_3$ and $Q_4$ are correctly biased, to prevent device latchup. Latchup in a C-MOS device, if allowed to continue, can cause eventual device failure.

capacitor. At room temperature and with a +5-V supply, an external 1-picofarad capacitor results in a 10-kHz oscillator frequency. The frequency drops off with increasing capacitance values—to 5 kHz at 10 pF, to 1 kHz at 100 pF, and to about 15 hertz at approximately 10,000 pF (0.01 $\mu$F).

A series voltage regulator consisting of zener reference diode $Z_1$, resistor $R_1$, and source-follower p-channel transistor $Q_3$ provides a partially regulated supply for all the low-voltage circuitry on the chip. The regulator can supply up to −5 V (with respect to the positive power supply) for input supply voltages of about 6 V and higher. Because of the modest size of $Q_3$, the voltage regulator not only reduces power consumption at high supply voltages, but also limits the maximum current taken by the oscillator and the divide-by-2 counter to a value less than the holding current of the inherent SCR on the chip.

The level translators (Fig. 4) provide switching signals to the gates of the four output transistors $Q_1$ through $Q_4$, with amplitudes equal to the sum of the output voltage and +V. They also ensure that a break-before-make sequence takes place, as switching alternates between pump-and-charge and charge-and-pump transitions.

### A critical element

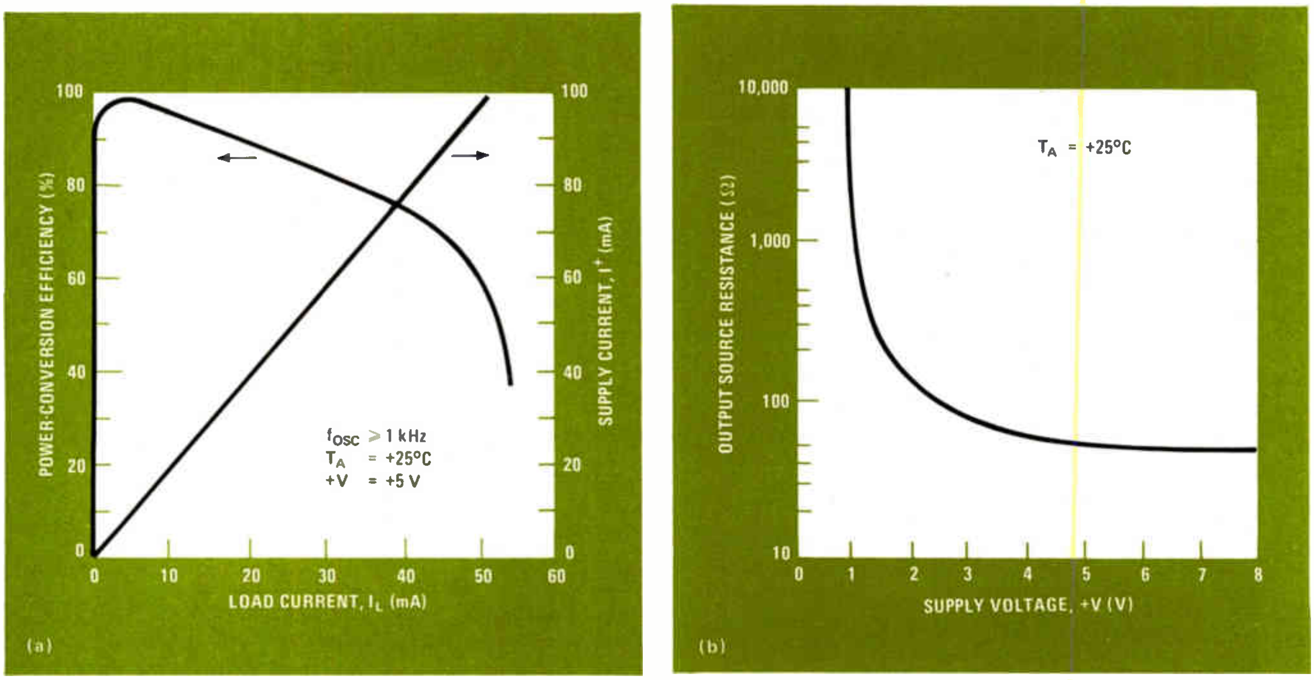
The substrate logic network is the most critical part of the converter chip. Its two main functions are to make sure that the substrates of $Q_2$ and $Q_4$ in Fig. 4 are never forward-biased with respect to their sources and drains and to establish the most negative voltage of any part of the circuit in either the charge or the pump cycles. This internal negative supply, $V_H$, is used to power the level translators. It drives the gate of either $Q_3$ or $Q_4$ to a voltage similar to that of the sources to ensure transistor turn off.

Transistors $Q_3$ and $Q_4$ require special drive considerations, since the sources and drains are inverted on each device during pump and charge phases. Consider $Q_3$'s operation, for example. During the charge phase, the most positive source/drain terminal is connected to the external charge-pump capacitor. This terminal is then by definition the drain, whereas the source which is more negative is connected to ground. To minimize $Q_3$'s resistance, it is desirable to also connect its substrate to ground and not to the output voltage or to $V_H$. This is because reverse-biasing the substrate of an MOS transistor with respect to its source increases its threshold voltage. Thus, for a given gate-to-source voltage, the effective turn-on voltage—that is, excess gate-to-source voltage over threshold voltage—is reduced, decreasing the transistor's resistance.

### The pumping phase

During the pumping phase, the external capacitor's negative terminal is shifted negatively by a voltage approximately equal to +V. In this case, the most negative source/drain terminal is connected to the negative side of the external capacitor (and thus becomes the source of $Q_3$), and its drain is connected to ground.

Similar arguments can be made for transistor $Q_4$ concerning its source-drain reversals, except that here conditions are different for startup and output short-circuit operations than during normal operation. Sensing circuitry monitors the voltages on the external capacitor's negative side and $V_{OUT}$ terminals and compares them with ground. The substrate of $Q_4$ is then connected to the most negative of the $V_{OUT}$, external-capacitor negative, or ground terminals. Figure 5 shows the substrate steering transistors for $Q_3$ and $Q_4$. The steering transistors are relatively small n-channel devices and share $Q_3$ and $Q_4$'s substrates.




**6. Efficient.** When converting a +5-V supply into a −5-V one, the 7660 achieves efficiencies of 98%, as a function of the load current (a). The 7660 can be used down to 1.5 V, below which its output source resistance rises rapidly as a function of the supply voltage (b).

During the charge cycle ($Q_3$ on and $Q_4$ off), steering transistor $Q_{S1}$ connects the substrate of $Q_3$ to ground and the substrate of $Q_4$ is connected to ground or $V_{OUT}$, whichever is more negative. During the pump cycle, the external capacitor's negative terminal is normally the most negatively biased point and is connected to the substrates of $Q_3$ and $Q_4$ by $Q_{S2}$ and $Q_{S3}$. Fault conditions (for example, the capacitor's negative terminal connected to +V or $V_{OUT}$ connected to +V) are also sensed and the substrates of $Q_3$ and $Q_4$ connected to the most negative of any of the three terminals—ground, the external capacitor's negative terminal, or $V_{OUT}$. Fault conditions can be handled by the 7660 for short periods of time. Prolonged fault conditions at high voltages, however, will cause excessive power dissipation, leading to eventual device failure.

Finally, both the timing interval between the signals applied to the gates of $Q_3$ and $Q_4$ and the reaction time of the substrate logic network should be short. This is achieved by slowing down the rate of rise and fall of the gate signals to $Q_3$ and $Q_4$.

For the 7660 to be useful, as low an output impedance as possible is desired, so that useful output currents of several milliamperes can be achieved at high power-conversion efficiencies. Transistors $Q_1$ through $Q_4$ are therefore chosen as extremely large. At a 5-V gate-to-source drive, each has an on-resistance on the order of 10 Ω or less. The chip area of the four output transistors represent about two thirds of the total area.

### Efficiencies of up to 98%

The effectiveness of the 7660's design can be seen from Fig. 6a, where power-conversion efficiencies for converting a +5-V into a −5-V supply can typically be as high as 98% for medium to low oscillator frequencies. At high oscillator frequencies, switching transient losses of the output transistors and the substrate logic network reduce overall efficiencies somewhat. Figure 6b shows the 7660's output source resistance as a function of supply voltage. Useful operation can typically be achieved with a supply voltage as low as 1.5 V.

At first glance, the maximum power efficiency would seem to approach 50%. This is certainly true of any situation in which a capacitor is charged from 0 V up to some value, then discharged into a load. However, in the case where a capacitor is charged and discharged between two voltages, $V_1$ and $V_2$, the energy lost is defined by:

$$E = C(V_1^2 - V_2^2)/2$$

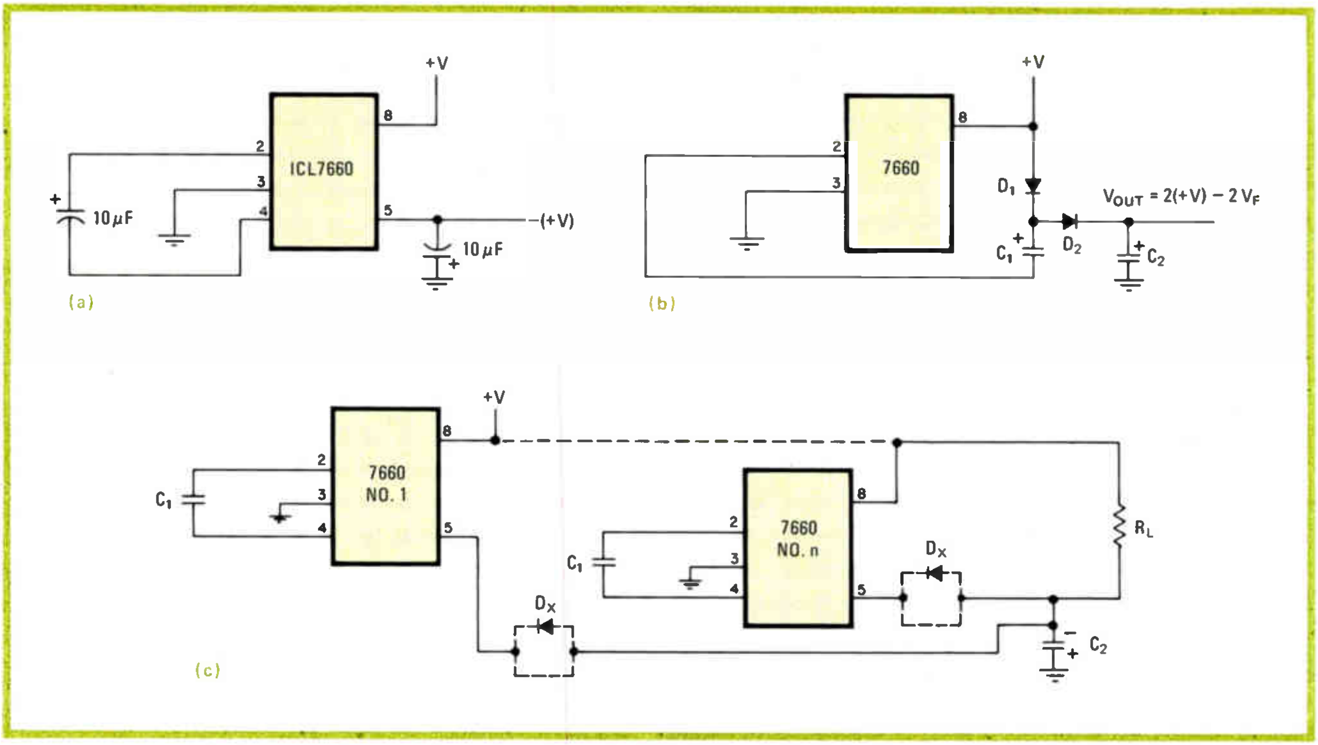
where C is value of the capacitor in farads and E is the lost energy. If $V_1 - V_2$ is very small compared with $V_1$, the percentage energy loss is also small, given as:

$$100(V_1^2 - V_2^2)/(2V_1^2)$$

At the limit, when $V_2 = V_1$, no energy is lost. If the values of $C_1$ and $C_2$ in Fig. 2 are made very large and their impedances at the switching frequency are very low compared with the load resistance, energy-conversion efficiencies approaching 100% can be obtained. Energy is lost only in the transfer of charge into and out of a capacitor during a change of voltage.

Although output-section switching transients are mainly capacitive, they inject currents into the substrate. At high input supply voltages, these transients can forward-bias junctions associated with the $p^-$ well or the $Q_4$ substrate. This in turn may trigger the inherent SCR in $Q_4$ and the adjacent on-chip circuitry. The result is to discharge the reservoir capacitor rapidly.

After the reservoir capacitor is almost totally discharged and the current in the SCR has fallen below the capacitor's holding value, the device again operates cor-




**7. Hooking up.** The usual 7660 configuration is a negative-voltage generator from a positive source (a). It can also do positive-voltage multiplication (b) and may be paralleled (c) for increased current output; diodes $D_x$ are needed for $V_{OUT}$ of 6.5 to 10 V.

rectly, until the output voltage (reservoir capacitance voltage) reaches the same critical value, and the latchup phenomenon starts again. Since this effect occurs only during the start of the charge cycle and not during the pump cycle, isolating the reservoir capacitor with an external diode at the $V_{OUT}$ terminal prevents capacitor discharge. Connecting a 10-μF capacitor from the $V_{OUT}$ terminal to ground (the positive side of capacitor is grounded) results in a simple negative-voltage converter.

Also, the 7660 has a terminal that can be used to short out the on-chip series regulator for better operation at low supply voltages. With the low-voltage terminal connected to ground, operation with an input supply voltage as low as 1 V is possible. At higher voltages, however, it is mandatory that the low-voltage terminal be open, in order to allow the internal voltage regulator to stop device latchup.

## Applying the 7660

The majority of 7660 applications involve the generation of a negative supply, particularly of −5-V supplies. All that is required additionally are two capacitors. For applications requiring the doubling of 6 V, a diode is placed in series with the reservoir capacitor. This diode isolates the reservoir capacitor from the 7660 during the charge phase. (The diode is necessary to avoid capacitive feedthrough on chip, which is aggravated at high temperatures, causing the output section to momentarily latch up at the beginning of the charge phase and discharging the reservoir capacitor.) The choice of values for the pump and reservoir capacitors depends primarily on the desired output current and the peak-to-peak output voltage ripple. For oscillator frequencies below the natural oscillator frequency of 10 kHz, an additional external capacitor connected to the oscillator terminal is required. For maximum efficiency, a low oscillator frequency of about 1 kHz is desirable. At this frequency, however, a tenfold increase in pump and reservoir capacitor values is needed for a given output voltage ripple.

## Cascading for negative multiplication

Two or more 7660s may be cascaded to produce negative multiples of the initial supply voltage ($V_{out}$ equals the number of 7660s times +V). Because of the finite efficiency of each device, however, the practical limit for light loads is about 10 stages. Note that each device is exposed to a maximum of twice the input supply voltage, and not the total output voltage.

The most common arrangement of the 7660 for generating a negative voltage equal in magnitude to a positive one is shown in Fig. 7a. The 7660 can also be used to obtain positive-voltage multiplication (Fig. 7b). There, the pump output driven at the external capacitor's positive terminal charges $C_1$ to a voltage level of $+V - V_F$, where $V_F$ is the forward voltage drop of diode $D_1$. During the pump phase, the voltage on $C_1$ and +V is applied through $D_2$ to $C_2$. The voltage thus created on $C_2$ becomes $2(+V) - 2V_F$.

Both positive- and negative-voltage multiplications can be combined using a single 7660. This approach is suitable for generating +9 and −5 V from a +5-V supply. Furthermore, 7660s may be paralleled to increase the output current or to decrease the output source impedance (Fig. 7c). A single reservoir capacitor suffices, but individual pump capacitors are required for each converter. There is no limit to the number of devices that may be paralleled. □

# More communications in orbit

## Updated table gives operating characteristics of orbiting satellites and those soon to be launched

by the staff of Satellite Systems Engineering Inc., Washington, D. C.

☐ *Over 75 active communications satellites are in geostationary orbit today—some 20 more than when* Electronics *first published this chart on Oct. 12, 1978. Others are fully designed but not yet launched or else still in the early planning stages. Four of the most important new systems (Anik-D, Palapa 2, Marecs, and Telecom 1) have been added to the chart; the now inactive systems (Marots 1, ATS-6, CTS, and Skynet 2B) have been dropped; and information on all the others has been updated.*

*The operational satellites handle 30 communications programs. The service each program offers is indicated by International Telecommunications Union designations and the band letters for its frequency. Specific frequency assignments, which vary from region to region, may be obtained from the system operator or from the Federal Communications Commission's Radio Regulations.*

### What's new?

*The satellites in Canada's Anik-D series will replace the three now orbiting in the Anik-A series, which will near the end of their useful life in 1982. The D series is to be launched by the U. S. space shuttle, unless further slippage in this program should cause a change of plans.*

*In the program for ship-to-shore communications called Marecs (for maritime versions of the European Communications Satellite), the first two satellites are to be put into orbit in 1981 by the European rocket system Ariane. The complete program will call altogether for three Marecs and three Intelsat Vs with maritime payloads.*

*Europe will also have Telecom 1—a two-satellite system developed by France—in operation by 1983.*

*In Asia, the Palapa 2 satellites will replace Palapa 1, now supplying telecommunications to Indonesia and other members of the Association of South East Asian Nations (ASEAN). To be launched in 1983, these satellites will have twice as many transponders as Palapa 1 and twice its output power and will be placed in a longitude somewhere between 108° and 118° east.*

*Almost all the satellites are in a circular orbit in the plane of the equator and about 19,323 nautical miles above it. Their rotational periods of 23 hours, 56 minutes, and 4.09 seconds keep them in fixed positions relative to any point on earth, or geostationary orbits.*

*Only the Soviet Union's Molniya System is different. It employs a highly elliptical orbit with a period of about 12 hours, an apogee of 40,000 kilometers, and a 63.4° inclination to the equator. In this alignment, the major axis of the ellipse does not rotate, the apogee remains over the Northern Hemisphere, and most of the time the individual satellites stay within view of the far northern reaches of the USSR. Tracking earth stations are required, however, as is periodic handover from one satellite to another.*

### More than one choice

*The stabilization system for satellites is usually described as either spin or three-axis. But since spinning satellites with despun platforms are also stabilized along three axes as far as the antenna beams are concerned, it would be more accurate to describe the two types as drum- and wheel-stabilized. Except where noted, the mass is the initial weight on final orbit, including station-keeping propellant.*

*The primary power figure is the total wattage available from the on-board solar array during equinox at the beginning of the satellite's life. Typically requirements vary not only with total radiated power but also with receiver system, degree of redundancy, and service to be provided during a solar eclipse.*

*Only an approximate picture of transponders and antenna beams can be given because the system block diagrams show a great variety in redundancy, switching possibilities, and bandwidths. The number of transponders equals the number of rf channels with the bandwidths as shown in the row below.*

### Multiple values

*Where the satellite figure or merit has more than one value, they apply to the different beams or transponders or bandwidths noted in the rest of the row. Similar considerations hold for some other specifications.*

*It is important not to confuse the rf carrier modulation system with the multiple-access scheme for many earth stations using the same transponder. Note also that the single-channel-per-carrier technique is a special type of frequency-division multiple access.* ☐

# Electronics

## A GUIDE TO COMMUNICATIONS SATELLITES

| System | Intelsat IV | Intelsat IV-A | Intelsat V | | Molniya 1 | Molniya 3 | Stat-sionar | Anik A |
|---|---|---|---|---|---|---|---|---|
| System operator | Intelsat | Intelsat | Intelsat | | USSR/Inter-sputnik | USSR/Inter-sputnik | USSR/Inter-sputnik | Telesat Canada |
| Service[1] | fixed tel., TVD | fixed tel., TVD | fixed tel., TVD | | fixed tel., TVD | fixed tel., TVD | fixed | fixed tel. |
| Frequencies[2] | C | C | C | Ku | C, uhf | C | C | C |
| Launch vehicle | Centaur | Centaur | Centaur (shuttle or Ariane) | | A−2 Soyuz | A−2 Soyuz | A−2 Soyuz Proton SL-12 | Thor Delta 2914 |
| Prime contractor | Hughes | Hughes | Ford | | | | | Hughes |
| Stabilization | spin | spin | 3-axis | | 3-axis | 3-axis | 3-axis | spin |
| Mass (kg) | 731 | 790 | 1,020 | | 1,000 | 1,000 | 1,250 | 272 |
| Primary power (W) | 569 | 708 | 1,220 | | 500 | 500 | 700 | 260 |
| Coverage[3] | global spot | global hemisphere spot | global hemisphere zonal | spot | global USSR | global USSR | global spot | Canada |
| Number of transponders | 12 | 20 | 15 | 6 | 1 | 3 | 6 | 12 |
| Transponder bandwidth (MHz) | 36 | 36 | 36 41 72 77 | 72 77 241 | 50 | 50 | 40 | 36 |
| Number of antenna beams | 6/4 | 7/3 | 5/5 | 2: east and west | 1 | 1 | 2−4 | 1 |
| Polarization | circular | circular | circular | linear | circular | circular | circular | linear |
| G/T (dB/K) (figure of merit) | −18.6 | −18 −11.6 −11.6 | −18.6 −11.6 − 8.6 | 0.0 E 3.3 W | −15.8 to −18.6 | −10 | −15.8 | −7 |
| EIRP (dBW) (effective isotropic radiated power) | 22.5 34.2 | 22 26 29 | 23.5, 26.5 26, 29 29 | 41.4 E 44.4 W | 30 | 35 | 25 to 36 | 33 |
| Modulation[4] | FDM/fm fm QPSK SCPC | FDM/fm fm QPSK SCPC | FDM/fm fm QPSK | FDM/fm fm QPSK | FDM/fm | FDM/fm | FDM/fm | FDM/fm QPSK, SCPC |
| Multiple access[5] | FDMA TDMA | FDMA TDMA reuse | FDMA TDMA reuse | FDMA reuse | FDMA | FDMA | FDMA | FDMA TDMA |

| System | Anik B | Anik C | Anik D | RCA Satcom | WU Westar | TDRS Advanced Westar | | Comstar | Indonesia Palapa 1 |
|---|---|---|---|---|---|---|---|---|---|
| System operator | Telesat Canada | Telesat Canada | Telesat Canada | RCA American Comm. | Western Union Telegraph | Western Union Telegraph | | Comsat General | Indonesian government/Perumtel |
| Service[1] | fixed tel. | fixed | fixed tel., TVD, telegraph | fixed tel., TVD | fixed tel., TV, TTY | fixed | | fixed tel. | fixed tel., TV |
| Frequencies[2] | C/Ku | Ku | C | C | C | C | Ku | C | C |
| Launch vehicle | Thor Delta 3914 | Thor Delta 3910/STS | Thor Delta | Thor Delta 3914 | Thor Delta 2914 | STS | | Atlas Centaur | Thor Delta 2914 |
| Prime contractor | RCA | Hughes | Spar Aerospace | RCA | Hughes | TRW | | Hughes | Hughes |
| Stabilization | 3-axis | spin | spin | 3-axis | spin | 3-axis | | spin | spin |
| Mass (kg) | 440 | 522 | 635 | 461 | 297 | 2,132 | | 810 | 300 |
| Primary power (W) | 840 | 925 | 1,000 | 770 | 260 | 1,700 | | 760 | 300 |
| Coverage[3] | Canada | Canada | Canada, northern U.S. | Conus, Alaska, Hawaii | Conus | Conus, Alaska, Hawaii | Conus | Conus, Puerto Rico, Alaska, Hawaii | Indonesia |
| Number of transponders | 12/6 | 16 | 24 | 24 | 12 | 12 | 4 | 24 | 12 |
| Transponder bandwidth (MHz) | 36 72 | 54 | 36 | 34 | 36 | 36 | 225 | 36 | 36 |
| Number of antenna beams | 1 4/1 | 4/1 | 5 | 2 | 2 | 2 | 7 | 4 | 1 |
| Polarization | linear | linear | linear | linear | linear | linear | linear and circular | linear | linear |
| G/T (dB/K) (figure of merit) | −6/−1 | 3 | −37.5 −27 −28 | −5 −10 | −6 | −7 −12.5 −12.5 | −5 to 4.4 | −8.8 | −7 |
| EIRP (dBW) (effective isotropic radiated power) | 36 47.5 | 48 | 36 | 33 26 | 33 | 33 28 26 | 42 to 50.3 | 33 | 32 |
| Modulation[4] | FDM/fm QPSK, SCPC | FDM/fm QPSK, SCPC | FDM/fm fm/TV SCPC | FDM/fm QPSK SCPC | fm QPSK | fm QPSK | 250 Mb/s TDMA | FDM/fm | fm fm/SCPC |
| Multiple access[5] | FDMA TDMA | FDMA TDMA reuse | FDMA | FDMA | FDMA TDMA | FDMA TDMA | beam switch-ing | FDMA reuse | FDMA |

| System | S.E. Asia Palapa 2 | SBS | Comsat Marisat | Marecs | Insat | | France Telecom I | |
|---|---|---|---|---|---|---|---|---|
| System operator | Indonesian government/Perumtel | Satellite Business Systems | Comsat General/RCA Global Comm./ITT World Comm./WUI | European Space Agency | Indian government | | French government | |
| Service[1] | fixed tel., TV | fixed tel., TV | mobile tel., TTY | mobile tel., telegraph | fixed TV and radiometry | | fixed tel., TVD | |
| Frequencies[2] | C | Ku | L ship C shore | L ship C shore | S | C | C | Ku |
| Launch vehicle | shuttle or Thor Delta | Delta 3910 or STS | Thor Delta 2914 | Ariane | 3910 | | Ariane | |
| Prime contractor | Hughes | Hughes | Hughes | British Aerospace Dynamic Group | Ford | | Matra | |
| Stabilization | spin | spin | spin | 3-axis | 3-axis | | 3-axis | |
| Mass (kg) | 628 | 546 | 326 | 466 | 1,054 (into transfer) | | 1,100 (at launch) | |
| Primary power (W) | 1,108 | 1,000 | 330 | 500 | 1,250 | | —— | |
| Coverage[3] | S.E. Asia | Conus | global | global | India | | semi-global spot | France |
| Number of transponders | 24 | 10 | 2 | 1 | 2 | 12 | 4 | 6 |
| Transponder bandwidth (MHz) | 36 | 43 | 4 | 5.9 ship to shore 4.75 shore to ship | 36 | 36 | 40 120 | 36 |
| Number of antenna beams | 2 | 1 | 1 | 2 | 1 | 1 | 3 | 2 |
| Polarization | linear | linear | circular | circular | linear | | circular | linear |
| G/T (dB/K) (figure of merit) | −5 | 2 to −2 | −17 −25 | −12.8 ship to shore −16.5 shore to ship | —— | | −13.6 | 6.5 |
| EIRP (dBW) (effective isotropic radiated power) | 34 | 40 to 43.7 | 20−29.5 18.8 | 18.8 ship to shore 20, 26, 29.5 shore to ship | 34 | 42 | 26 34.6 | 49 |
| Modulation[4] | fm fm/SCPC | QPSK | fm BPSK | PSK fm, SCPC | fm QPSK | | FDM/fm | 25 Mb/s TDMA |
| Multiple access[5] | FDMA | TDMA | TDMA FDMA | TDMA FDMA | FDMA | | FDMA SCPC | TDMA |

| System | Japan BS | Japan CS | Sirio | OTS/ECS | DSCS II | DSCS III | NATO III | Fleetsatcom |
|---|---|---|---|---|---|---|---|---|
| System operator | Japanese government | Japanese government | Italian government | European Space Agency | U.S. government/Department of Defense | U.S. government/Department of Defense | NATO | U.S. government/Department of Defense |
| Service[1] | broadcast experimental | fixed experimental | fixed experimental | fixed | fixed military | fixed military | fixed military | mobile military |
| Frequencies[2] | Ku | K, Kc, C | Ku, Kc | Ku | X | X | X | uhf, X |
| Launch vehicle | Thor Delta 2914 | Thor Delta 2914 | Thor Delta 2910 | Thor Delta 3914 | Titan IIIC | Titan IIIC shuttle | Thor Delta 2914 | Atlas Centaur |
| Prime contractor | Toshiba/GE | Mitsubishi/Ford | Campagnia Nazionale Aerospaziale | Hawker Siddeley Dynamics | TRW | GE | Ford | TRW |
| Stabilization | 3-axis | spin | spin | 3-axis | spin | 3-axis | spin | 3-axis |
| Mass (kg) | 352 | 340 | 218 | 444 | 536 | 748 | 349 | 1,005 |
| Primary power (W) | 1,000 | 521 | 118 | 700 | 520 | 800 | 538 | 1,425 |
| Coverage[3] | Japan | Japan | North Atlantic, Europe spot | spot Europe A Europe B | global spot | global spot | Atlantic Europe | global |
| Number of transponders | 2 | 6/2 | 1 | 6 | 4 | 6 | 2 | 12 |
| Transponder bandwidth (MHz) | 50 80 | 200 | 32 | 120 40 5 | 410 total | 395 total | 17 85 50 | 0.005 0.025 0.500 |
| Number of antenna beams | 1 | 1 | 3 | 3 | 3 | multiple array | 2 | 1 |
| Polarization | linear | circular | circular | linear, linear, circular | circular | circular | circular | circular |
| G/T (dB/K) (figure of merit) | −8.2 | noise figure = 13 dB/9 dB | −22.2, −17.2 | 4.2 −4.8 −2.2 | 8.5 20.2 | −16 to −1 | −14.1 | −16.6 (uhf) |
| EIRP (dBW) (effective isotropic radiated power) | 55 | 37 29.5 | 24 | 45.8 36.5 42.0 | 28 40 | 23−40 | 35 29 | 26−28 (uhf) 27 |
| Modulation[4] | fm and digital | 100 Mb/s digital | PCM−PSK and fm video | fm PSK | fm QPSK | fm QPSK | fm QPSK | fm QPSK |
| Multiple access[5] | SCPC | TDMA | SCPC | TDMA | FDMA TDMA CDMA | FDMA TDMA CDMA | CDMA FDMA | FDMA |

[1]fixed — satellite service to specified fixed points
mobile — satellite service to ships, airplanes, and mobile ground terminals
broadcast — satellite service intended for reception by the general public
TTY — teletypewriter
tel. — telephone
TVD — television distribution

[2]P band or uhf — 200 to 400 MHz
L band — 1,530 to 2,700 MHz
S band — 2,500 to 2,700 MHz
C band — 3,400 to 4,200 MHz
4,400 to 4,700 MHz
5,725 to 6,425 MHz
X band — 7,250 to 7,750 MHz
7,900 to 8,400 MHz
Ku band — 10.95 to 14.5 GHz
Kc band — 17.7 to 21.2 GHz
K band — 27.5 to 31.0 GHz

[3]Conus — continental United States without Alaska and Hawaii

[4]SCPC — single channel per carrier
FDM — frequency-division multiplexing
fm — frequency modulation
PCM — pulse-code modulation
PSK — phase-shift keying
BPSK — binary phase-shift keying
QPSK — quadri phase-shift keying (four-phase-shift keying)
CPSK — coherent phase-shift keying

[5]CDMA — code-division multiple access
FDMA — frequency-division multiple access
TDMA — time-division multiple access
frequency reuse — same carrier frequencies assigned to different users through use of separate beams or polarizations

This chart was compiled by Satellite Systems Engineering Inc., Washington, D.C. 20014.

# Handling exceptions gracefully enhances software reliability

## The 68000 processor vectors to special routines upon encountering divide-by-zero operations and other exceptions

by Thomas W. Starnes, *Motorola Inc., Austin, Texas*

□ The main task of any computer system is to execute instructions. Illegal instructions and other exceptions to this process often cause unpredictable behavior unless the processor's design takes them into account.

The 68000 is uniquely well defended against such eventualities. When confronted with bus errors indicative of some kind of memory failure or with undefined operations like divide by zero, it vectors to a trap—a known memory location containing the user-supplied exception-handling routine. Such a routine might, for example, notify the operator of an attempt to execute an illegal instruction and then let the machine resume its normal activities. This feature, which greatly increases the 68000's reliability, is to be found on few other microprocessors.

In addition, the 68000 is exceptional in its handling of multiuser environments such as swapping user programs in and out of main memory. These kinds of tasks are conventionally serviced entirely in software, with program swapping, for instance, being handled by means of an executive subroutine that is either periodically called by the operating system or vectored to by an external interrupt. But in the 68000, built-in hardware supports a privileged, supervisory level of operation that makes this exception processing much easier to implement.

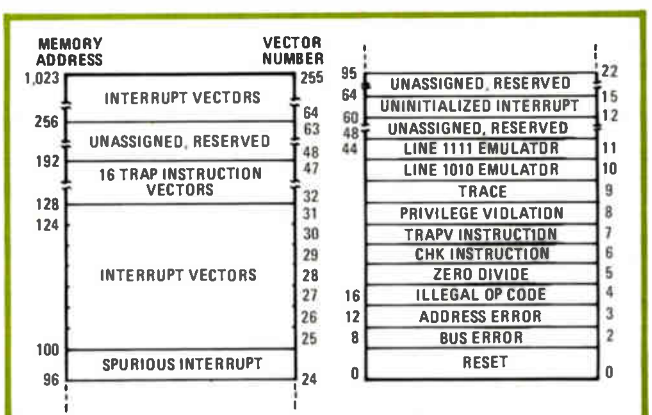
Traps also count as exceptions. Besides being caused by undesirable occurrences within the processor, they may be called expressly by instructions or requested during the execution of certain instructions. Each type of trap is associated with a vector which points to a service routine. The old program counter and status register are restored after execution of the routine. Any task can call the trap and utilize the trap routine.

Finally, to ease software development, the 68000 supports a trace function, in addition to the usual single-step mode that utilizes the halt pin. Like the other new features, it aids the designer of sophisticated systems but may be left unused in less complex systems. Figure 1 shows the memory locations of all exception vectors.

### User and supervisor levels

The 68000 operates at all times on one of two levels: supervisor or user. Operation at the supervisor level has certain privileges attached that are not permitted at the user level (Table 1). Programs other than those designed for system control execute for the most part at the 68000's user level. Operating system chores, such as task or context switching, should execute at the more privileged supervisor level. At this level of operation, the program's regular complement of instructions is available, allowing the operating system to vary the working environment of the microprocessor, service interrupts or act-on-error conditions caused by hardware or programs.

Whether the processor is at the supervisor level or at

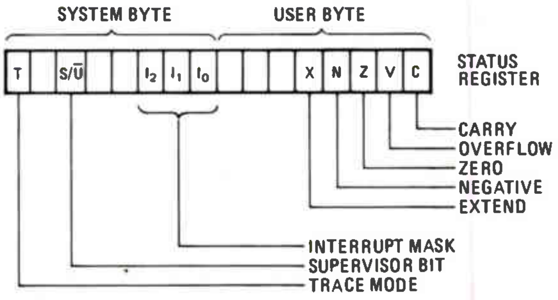



**1. Exception-handling vectors.** All exceptions cause a vector to be fetched from this map and loaded into the program counter. The old program counter and status register are saved on the supervisor stack and are restored at the end of the routine.

TABLE 1: PRIVILEGES OF THE 68000's USER AND SUPERVISOR LEVELS

| | User level | Supervisor level |
|---|---|---|
| Enter level by | clearing status bit 'S' | recognition of a trap, reset, or interrupt |
| Function code output (FC2 = ) | 0 | 1 |
| System stack pointer | user stack pointer | supervisor stack pointer |
| Other stack pointers | registers A0–A6 | user stack pointer and registers A0–A6 |
| Status bits available (read) (write) | C,V,Z,N,X,$I_0$–$I_2$,S,T<br>C,V,Z,N,X | C,V,Z,N,X,$I_0$–$I_2$,S,T<br>C,V,Z,N,X,$I_0$–$I_2$,S,T |
| Instructions available | all, except those listed at right | all, including:<br>STOP<br>RESET<br>MOVE to SR<br>ANDI to SR<br>ORI to SR<br>EORI to SR<br>MOVE USP to (ea)<br>MOVE to USP<br>RTE |

**TABLE 2: EXAMPLES OF STATUS REGISTER OPERATIONS**




| Executed at supervisor level | | Action taken |
|---|---|---|
| MOVE | #$0400, SR | Turn off trace; change to user level, clear condition codes; load interrupt mask with 100 |
| ANDI | #$DFFD, SR | Clear V; change to user level; no change: all others |
| EORI | #$2000, SR | Change to user level; no change: all others |
| ORI | #$8700, SR | Turn on trace; set interrupt mask to NMI; no change: all others |
| **Executed at user level** | | **Action taken** |
| MOVE | #$00C0, CCR | Set N, Z; clear X, V, C; no change: all others |
| ORI . B | #$01, CCR | Set C; no change: all others |
| ANDI . B | #$01, CCR | Clear C; no change: all others |
| EORI . B | #$08, CCR | Toggle N; no change: all others |
| EORI . W | #$8008, SR | Trap through privilege violation vector |

the user level is determined by the S/$\overline{U}$ bit in the status register. Transition from one level of operation to the other is accomplished in a number of ways.

The processor will go to the user level from the supervisor level if the S/$\overline{U}$ bit is reset by a MOVE, ANDI (and immediate), or EORI (exclusive or immediate) instruction (Table 2). Conversely, the trap instructions are the only means of getting from the user to the supervisor level in software. For example, certain instructions can cause such a switch to the supervisor level if particular conditions arise during the instructions' execution. In addition, a bus-error signal or any of the other hardware traps will also force the processor to the supervisor level, as will the servicing of an interrupt request.

If the microprocessor is at the user level before an exception is processed, then it will normally return to that level once the routine is closed with the RTE (return from exception) instruction. This instruction also serves to reset the S/$\overline{U}$ bit.

## Traps

There are 16 user-definable trap instructions that, when executed, always direct program control to a designated trap routine at the supervisor level. These software interrupts are useful for calling the operating system, simulating interrupts during debugging operations, signaling the completion of a task, or indicating that an error condition has appeared in a routine.

Two additional instructions—trap-on-overflow and check—examine operating conditions and cause a trap if those conditions are not satisfied. Trap-on-overflow (TRAPV) will cause a trap if the overflow bit in the status register is set (V = 1). A single routine at the operating system level may then handle every overflow occurrence. The check instruction (CHK) determines whether a chosen register's contents are within the bounds of zero and a specified upper limit and, if it finds the register is outside of the designated bounds, initiates a trap. It may be used to verify that a stack does not overrun, that a string of characters will fit into the allocated space, that an entry into an array is within the dimensions of the array, or that a task does not access data outside its designated space. Failure to remain within bounds causes a call by the operating system to the check service routine.

The two divide instructions—DIVS, which is signed, and DIVU, which is unsigned—can also cause a trap. The attempt to divide a number (dividend) by zero (divisor) is detected before the operands are modified, and a trap is taken automatically. This turns program control over to the supervisor for alternative action.

The divide instructions may encounter one other situation that will divert the normal divide operation—an overflow condition during the division. When this happens, the overflow bit (V) is set, but the result is not written to the destination and the original operands are left intact. Instruction execution continues with the next instruction, though a succeeding TRAPV instruction could call the supervisor for special processing.

## Undefined instructions

The attempt to execute certain instructions not implemented in current versions of the 68000 can cause one of two traps to occur. These instructions have op codes whose first 4 bits are 1010 ($A_{16}$) or 1111 ($F_{16}$) and are reserved for future enhancements to the instruction set. In anticipation of the expanded instruction set, the "line 1010 emulator" and the "line 1111 emulator" traps are provided to allow the user to imitate the operation of future instructions with macroinstructions. When specific op codes become available for the additional instructions, those can be included in programs. Currently, when an instruction op code is fetched whose first 4 bits are 1010 or 1111, a trap is made to the emulator routine—the "line 1010 emulator" and "line 1111 emulator." When the operation becomes available as a machine primitive, the macroinstruction routine can be eliminated.

There are other op codes that would otherwise cause problems but instead initiate exception processing. Those, for example, that neither decode into valid instructions nor fall into the line 1010/1111 category are considered illegal, and the attempted execution of one will result in a trap. This is a particularly valuable exception because it helps to catch incorrect machine code. Most microprocessors perform some unknown or variable operation when an undefined op code is fetched, inviting the destruction of program or data. Software integrity is improved by forcing an operating-system call to be made upon receipt of an invalid op code.

Unlike most instructions, which may execute at either the user or the supervisor level, privileged instructions, listed in Table 3, may execute only at the supervisor level. Privileged instructions are designed for system control; hence any instruction that modifies the entire status register is privileged. This privilege prevents a user-level program from turning on or off the trace feature, from changing the privilege level, or from changing the interrupt mask level.

The stop, reset, and return-from-exception instructions are also privileged. STOP suspends execution of instructions, loads the status register (including the interrupt mask), and awaits an external prompt (unmasked interrupt or reset). RTE is privileged, since all exception processing takes place at the supervisor level and hence the return instruction must also be on that level. Neither can RESET be used by a program operating at the user level, for this instruction holds the reset pin low long enough to initialize all devices tied to that line, which is clearly a supervisor operation. Any attempt to execute a privileged instruction while on the user level would be a privilege violation and would therefore result in a trap.

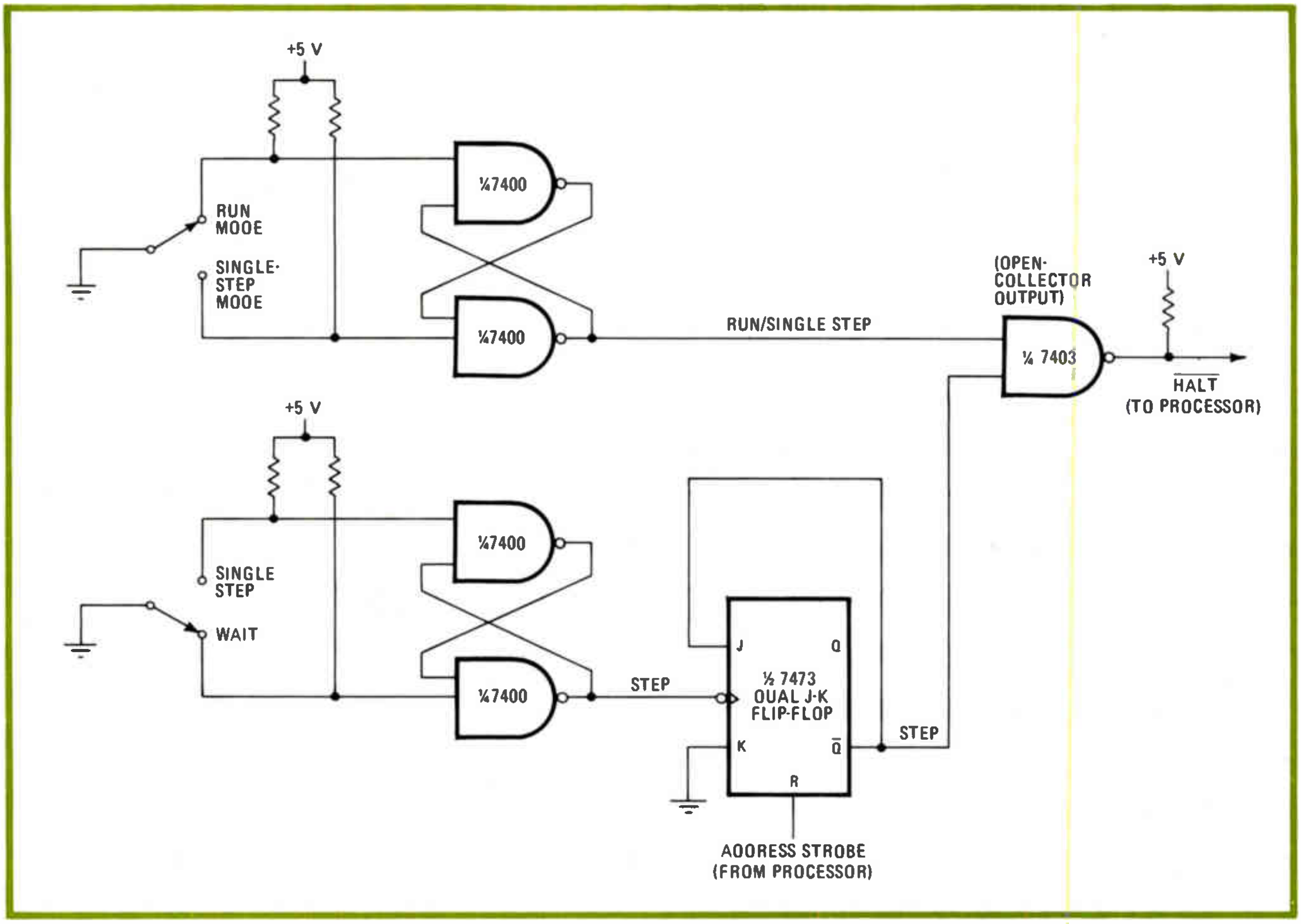
In addition, while operating at the supervisor level, the operating system can use both the supervisor stack pointer and the user stack pointer. That privilege allows it to change the user stack location in the course of switching from task to task.

To assist in program development and debugging, the trace feature is provided along with the standard halt feature. The trace routine is written by the programmer and might print out register and memory contents or whatever debug operation is desired. Instruction tracing is initiated by turning on the trace bit (T) in the status register. Once that is done, the execution of each instruction is followed by the tracing operation. This is done by the trace trap vector, which directs program execution to the trace routine.

Jumping to the trace routine is slightly different from jumping to the other traps. The program counter and status register of the main program are stored on the

**TABLE 3: PRIVILEGED INSTRUCTIONS**

| Privileged instruction | Operation |
|---|---|
| RESET | reset external devices |
| RTE | return from exception |
| STOP | stop program execution |
| ORI to SR | logical-OR to status register |
| MOVE USP | move user stack pointer |
| ANDI to SR | logical-AND to status register |
| EORI to SR | logical-EOR to status register |
| MOVE EA to SR | load new status register |




**2. Single-step using halt.** With this circuit, the operator can control memory accesses by stepping through them one at a time. Each time an address strobe from the processor is issued, it resets the flip-flop. If the upper switch is in the single-step position, then the processor will halt and remain halted until the lower switch is toggled. In this way the asynchronous buses can be exercised under manual control.

supervisor stack and the trace bit is turned off (T = 0), while the S/U bit is set to the supervisor privilege level. The trace vector is then fetched and loaded into the program counter.

The trace routine is terminated, as are all exceptions, with an RTE, which causes the processor to fetch and execute the next instruction in the main program. To turn off the trace function, the stack location containing the saved status register must be modified to reset the T bit. Then when the RTE instruction pulls the program counter and status register from the supervisor stack, trace has been disabled, allowing normal instruction execution to resume.

The HALT pin on the 68000 may also be used in evaluating a program's execution. With the circuit shown in Fig. 2, the processor can be halted after each bus cycle is completed.

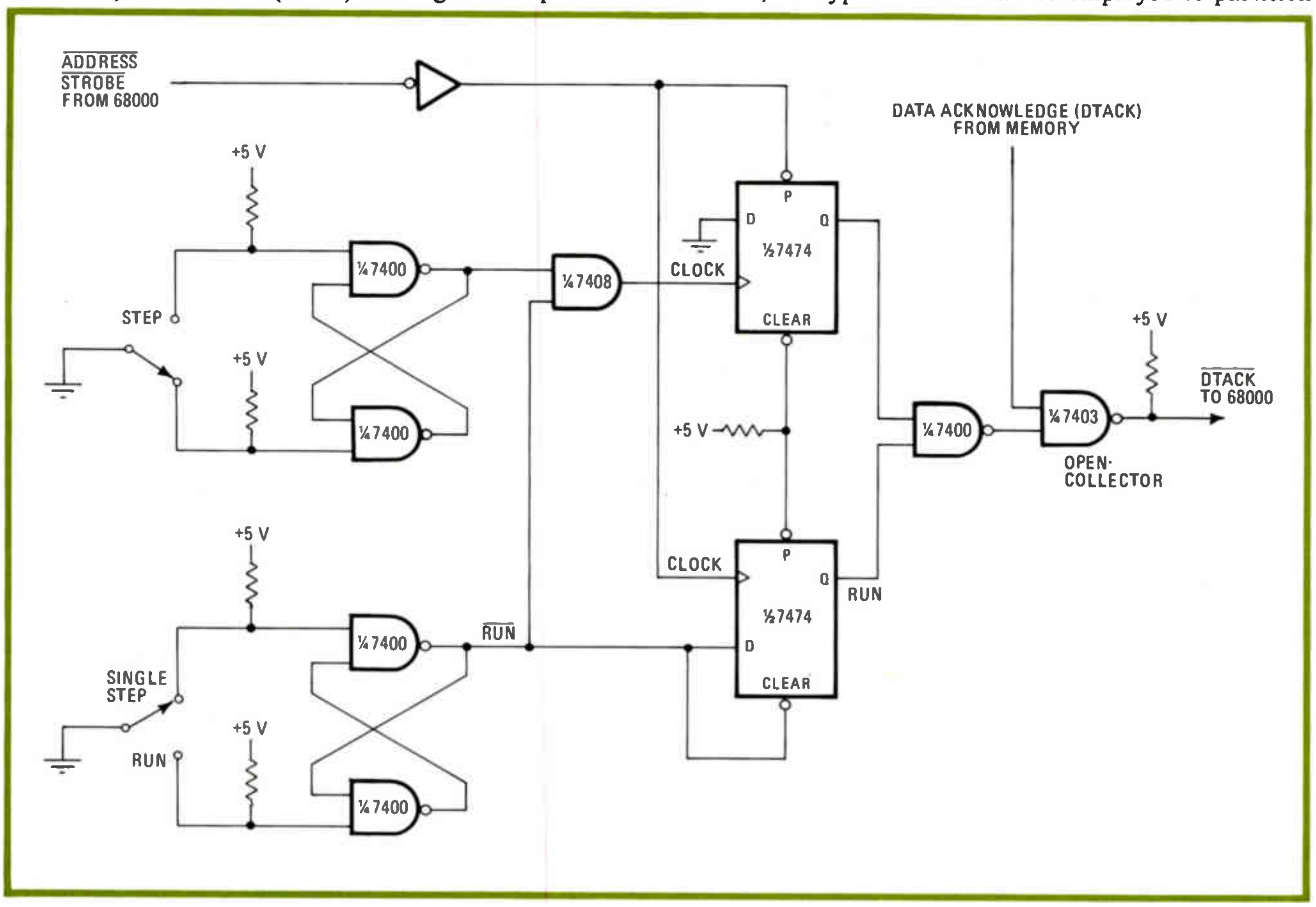
By delaying the data transfer acknowledge, DTACK, signal with intercepting logic (Fig. 3), the buses will remain asserted by the processor indefinitely. The buses and control signals can then be inspected. When the examination is complete, the intercepting logic allows DTACK to propagate through to the 68000, completing the bus cycle.

On every memory access, after sufficient time has passed, the memory or peripheral uses the 68000's asynchronous bus to send the processor a signal acknowledging the data transfer. Should an error be detected during an access, a bus error (BERR) can signal the processor that the bus cycle should be aborted.

The faulty memory accesses that prevent a bus cycle's completion may be due to any of several conditions. External circuitry to detect parity errors or—in more sophisticated systems—Hamming codes or other techniques detecting single- or double-bit errors might activate the BERR. In the absence of a DTACK from a block of memory, a timer should flag the processor with a BERR after the access time of the memory has been exceeded. The timer also notifies the processor whenever an interrupting device is not responding to an acknowledge signal, resulting in a trap to the spurious-interrupt routine. The unitialized interrupt vector handles interrupts arriving from uninitialized peripherals.

Finally, memory management systems may decide that the memory access is outside of the memory or I/O space currently active and, if they take advantage of the function codes, that the access was not within the bounds of the space allotted to that type of program or data.

For example, the three function-code outputs on the chip provide information on the type of memory cycle about to take place and can activate the bus-error line if anything is out of order. The three pins ($FC_0$–$FC_2$) (Fig. 4) can be decoded to tell whether the processor is attempting to access writable memory or instructions and whether it is doing so while operating at the supervisor or user privilege level. They also may acknowledge interrupts for vectoring by device. By using a 74LS138 decoder, the type of access can be employed to partition




**3. Single-step using DTACK.** Here the user can implement a single-step mode by delaying the data-transfer–acknowledge signal. In an error-correcting system, the upper manual switch might be replaced by logic that recognizes the proper bus behavior.

memory into blocks of supervisor code, supervisor data, user code, and user data. Data space is defined as being the memory locations containing variables, vectors, stacks, queues, strings, tables, lists, or any other type of data found separate from the instruction, and fixed (immediate) operands, which are found with the instructions using them. The failure of a memory access to remain within its allotted memory space can be indicated to the microprocessor using the bus-error ($\overline{BERR}$) signal.

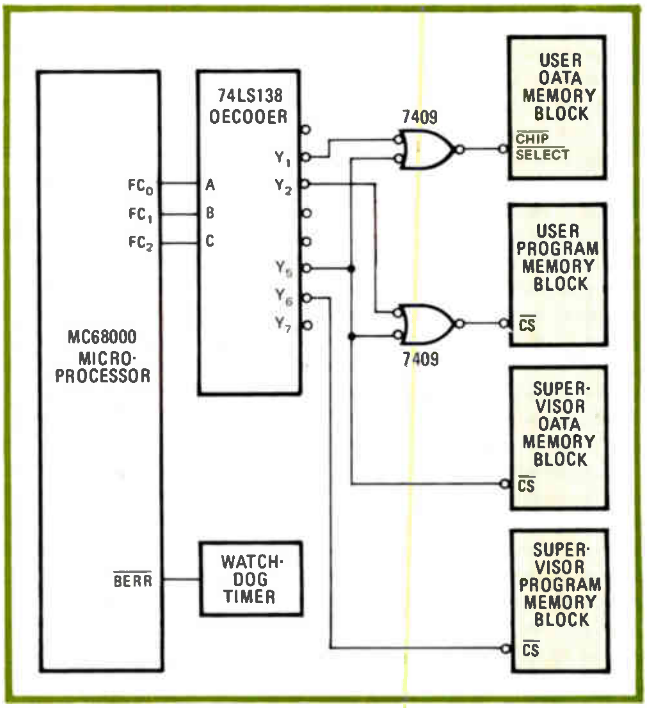
### Response to error

There are two forms of responses the 68000 might have to a bus error, depending on whether or not the halt line is asserted at the same time as $\overline{BERR}$. With both signals asserted, the 68000 will make an attempt to rerun the same bus cycle. The rerunning of the cycle will take place when the $\overline{BERR}$ and halt lines are released. Rerunning the bus cycle gives the memory system another chance to respond correctly. This type of bus error would be most useful for parity or other error-checking methods, in which noise or other extraneous signals might have caused the soft error.

When the $\overline{BERR}$ pin alone is asserted, the processor aborts the current bus cycle and initiates bus-error exception processing. Because a bus-error trap might be taken at any time, extra information is pushed onto the supervisor stack to ease recovery from the condition. Though currently the exact state of the processor cannot be retained to effect a complete recovery, sufficient information is stored to allow the operating system to determine the cause of the bus cycle failure. When a bus-error trap is taken, a copy of the program counter and status register is placed on the stack, as well as the op code being processed and the address on the bus at the time of the bus error. Also placed on the stack is whether or not an instruction was being processed, whether the access being made was a read or write, and the condition of the function codes when the $\overline{BERR}$ line was pulled.

From the information on the stack after a bus-error trap, the conditions leading to the error can be analyzed. Comparison of the address with the function codes might indicate that the wrong memory space was accessed. Further inspection of the address may reveal that the access was outside the range of the physical or active memory. Perhaps a virtual memory system needs to be reloaded. Possibly the section of memory accessed simply did not respond or is providing garbled data or instructions and should be deactivated and listed as bad memory. Maybe a stack or data space has grown out of its allotted block of memory and a new block needs to be allocated.

Examination of the op code may indicate that after the cause of the error is corrected, the instruction can be rerun—a possibility only if any operands or pointers used were all recoverable and if the condition codes did not affect the instruction execution, since it may not be known whether the condition code saved has been modified by the instruction. If it is determined that the instruction can be re-executed, further examination of the op code will indicate how much the saved program counter must be backed up. If data is lost, if the cause of




**4. Simple memory segmentation.** The function outputs are utilized here to separate memory into four areas. The "watchdog timer" notifies the processor of a bus error whenever an access is requested but a data-transfer-acknowledge signal has not been received within a reasonable time limit (say, 30 milliseconds).

a bus error cannot be determined, or if the software for one reason or another cannot continue normal processing, then the operating system will have to initiate a trouble call to an operator.

Current versions of the 68000 do not allow instructions, word (16-bit) data, or long-word (32-bit) data to be aligned on odd-byte boundaries; to do so would require an additional memory access to perform a read or write operation. Attempts to fetch or write an instruction, word or long word at an odd-byte address will cause a trap. This address-error trap lets the operating system realign data on even-byte boundaries or correct the program counter.

The same information saved during a bus-error trap is also saved when a trap is caused by an address error. This information is useful for recovering from the address error in much the same way as from a bus error.

### Catastrophic halt

There are several situations that will cause the 68000 to discontinue all processing. These are the double bus errors and double address errors. The detection of a second error during the exception processing (including vector fetches) of a bus error, address error, or reset will shut down the microprocessor. When any of these conditions appear, the processor determines that correct processing is impossible, halts further execution of any operations, and, in a unique use of the halt line, drives it as an output to flag an operator. That response to double errors prevents the processor from running away and destroying data or other tasks when it knows the system has had a catastrophic failure. □

## D-a converter also performs a-d translation

by Michael Parsin
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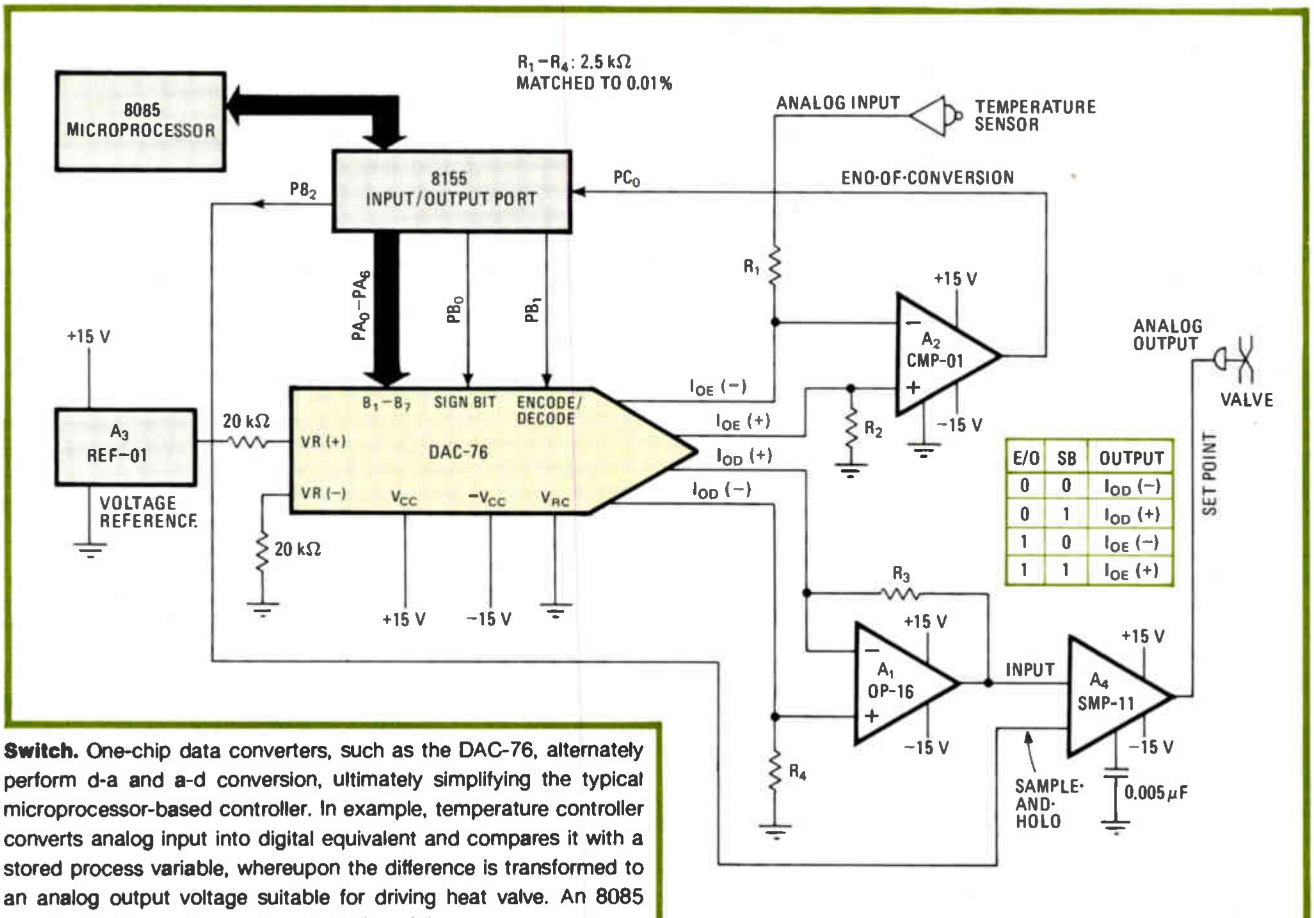
Complex microprocessor-based systems that require both analog-to-digital and digital-to-analog conversion, such as gas-flow and motor-speed units and antenna positioners, will be simplified by using multiplexing one-chip converters such as PMI's DAC-76. One of the advantages gained is elimination of an a-d converter and the inherent interfacing problems between two converters that would normally exist. System accuracy is also maintained, because the a-d and d-a conversions are processed and controlled via the same chip.

As shown in Fig. 1, the DAC-76 logarithmic (companding) d-a converter is alternately switched from its encoding or measurement (a-d) mode to its decoding or control (d-a) mode by placing the appropriate signals at its E/D port. An 8085 microprocessor and an 8155 input/output port provide the digital data (see program table). Operational amplifier $A_1$, comparator $A_2$, voltage reference $A_3$, and sample-and-hold amplifier $A_4$ come into use during the a-d portion of the cycle.

The measurement is initiated when the E/D line goes high, and the bipolar 0- to 5-volt analog input signal is sampled. The 8085 then commands the d-a device to generate a ramp, which appears at the $I_{oe}$ (+) port. When the ramp voltage equals the analog input, $A_2$ fires, generating an end-of-conversion signal. The processor's internal counter, which had initiated counting at the beginning of the cycle, is then frozen and its binary contents stored in a 1-byte memory location. Note that the DAC-76's companding feature makes it possible to compress 12-bit accuracy into a 7-bit format. This format, combined with a sign bit, makes it an ideal interface for the typical 8-bit microprocessor.

During the decode cycle, the data previously measured is compared with the control variable, which is stored away in a separate register, and the system acts to minimize the difference. For example, if the set point in a temperature controller has been adjusted at 100°, and the measured value is 110°, a correcting voltage that corresponds to the 10° offset must be generated for




**Switch.** One-chip data converters, such as the DAC-76, alternately perform d-a and a-d conversion, ultimately simplifying the typical microprocessor-based controller. In example, temperature controller converts analog input into digital equivalent and compares it with a stored process variable, whereupon the difference is transformed to an analog output voltage suitable for driving heat valve. An 8085 program (table) orchestrates the handling of data.

**8085 PROGRAM FOR DUAL DATA CONVERSION**

| Location | Label | Source statement | | Comments |
|---|---|---|---|---|
| 2000 | | ORG | 2000H | |
| 2000 | BEGIN: | LXI | SP,20C2H | ; INITIALIZE STACK POINTER |
| 2003 | | MVI | A,03H | ; SET POINTS A ANO B TO OUT ANO C TO IN |
| 2005 | | OUT | 20H | ; THIS SETS 8155 CSR |
| 2007 | ENCOO: | MVI | A,07H | ; START ENCOOE |
| 2009 | | NOP | | |
| 200A | | OUT | 22H | ; SET ENCOOE/OECOOE (E/O) TO ENCOOE ANO SIGN BIT TO (–) |
| 200C | LOOP: | INR | B | ; INCREMENT UP COUNTER |
| 200D | | NOP | | |
| 200E | | MOV | A,B | ; COUNT TO ACCUMULATOR |
| 200F | | OUT | 21H | ; OUT COUNT TO OAC-76 OIGITAL IN |
| 2011 | | IN | 23H | ; MONITOR ENO OF CONVERSION |
| 2013 | | ANI | 01M | ; MASK $PC_0$ |
| 2015 | | JNZ | LOOP | ; LOOP WHEN ENO-OF-CONVERSION IS HIGH |
| 2018 | | MOV | A,B | ; MOVE RESULT TO ACCUMUALTOR |
| 2019 | | STA | 203CH | ; STORE RESULT IN MEMORY 203C |
| 201C | | MVI | B,00 | ; CLEAR B REGISTER |
| 201E | OECOO: | MVI | A,7FH | ; START OECOOE |
| 2020 | | OUT | 21H | ; OUT TO OIGITAL-TO-ANALOG CONVERTER ALL 1's +5 V |
| 2022 | | MVI | A,01H | ; SET E/O TO OECOOE ANO SHIFT BIT TO (+) |
| 2024 | | OUT | 22H | ; OUTPUT TO SAMPLE-ANO-HOLO (S/H) ANO OAC-76 |
| 2026 | | MVI | A,05H | ; S/H TO HOLO ANALOG OUT TO +5 V |
| 2028 | | OUT | 22H | ; OUT TO S/H |
| 202A | | MVI | A,00H | ; ANALOG OUT TO NEGATIVE |
| 202C | | NOP | | |
| 202D | | NOP | | |
| 202E | | OUT | 22H | ; OUT TO S/H ANO OAC-76 |
| 2030 | | MVI | A,04H | ; S/H TO HOLO ANALOG OUT TO –5 V |
| 2032 | | OUT | 22H | ; OUT TO S/H ANO d-a CONVERTER |
| 2034 | | NOP | | |
| 2035 | | NOP | | |
| 2036 | | JMP | ENCOO | ; START ENCOOE AGAIN |
| | | END | | |

controlling the heat valve. The processor does this by addressing a lookup table to determine the required change in valve position that is proportional to the offset. The E/D line is then brought low, and a constant current is steered by processor control through the d-a converter's $I_{od}$ (+) port and thus to the inverting input of the operational amplifier, $A_1$.

Thus capacitor $C_H$ of the sample-and-hold device charges linearly as long as digital signal $PB_2$, which has been set low by the 8155 output port initiating data proportional to the offset voltage, remains low. When $A_4$ is placed in the hold state, the sampling period ends, and the voltage across the capacitor is transferred to the analog output line in order to drive the valve and thus set its position.

The aforementioned stand-alone configuration represents one good example of a direct digital control system, where a single host computer can be placed at the hub of a multitude of remote controllers. It should be kept in mind, however, that this system could easily be made part of a distributed digital control network, where the host computer has many remote minicomputers that have a hand in presiding over the major control loops. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.

# Interfacing TTL with fast bipolar drivers

by J. A. R. Ball, P. J. Grehan, and P. Welton
*Darling Downs Institute, School of Engineering, Queensland, Australia*

Surprisingly, there are as yet no suitable integrated circuits for translating the 0-to-5-volt output swing of TTL into arbitrary bipolar levels. But even the discrete interfacing circuits that have appeared over the years will fall short in performance, especially if the requirement calls for a high-speed switch to drive the relatively high capacitance of a power device or load. The solution lies in modifying the typical textbook interface with a circuit that acts to decrease the input-circuit storage time of the output transistors but does not appreciably affect any other interface parameter or specification.

A slightly modified ±10-V TTL interface is shown in (a), which will be suitable for relatively high-speed switching at low to medium current (below 100 milliamperes). In this circuit, $Q_1$ turns on and remains in the active region when the TTL output exceeds 1.5 V. Providing the current drawn out of the base is sufficient, $Q_3$ will saturate and the voltage applied to the load will be almost 10 V. When the TTL output falls sufficiently, $Q_1$ and $Q_3$ turn off, and charge stored in the base of $Q_3$ escapes via resistor $R_3$. Transistors $Q_2$ and $Q_4$ compris-

ing the other half of the circuit act in a complementary fashion, conducting when the TTL output falls below 1.5 V and applying −10 V to the load.

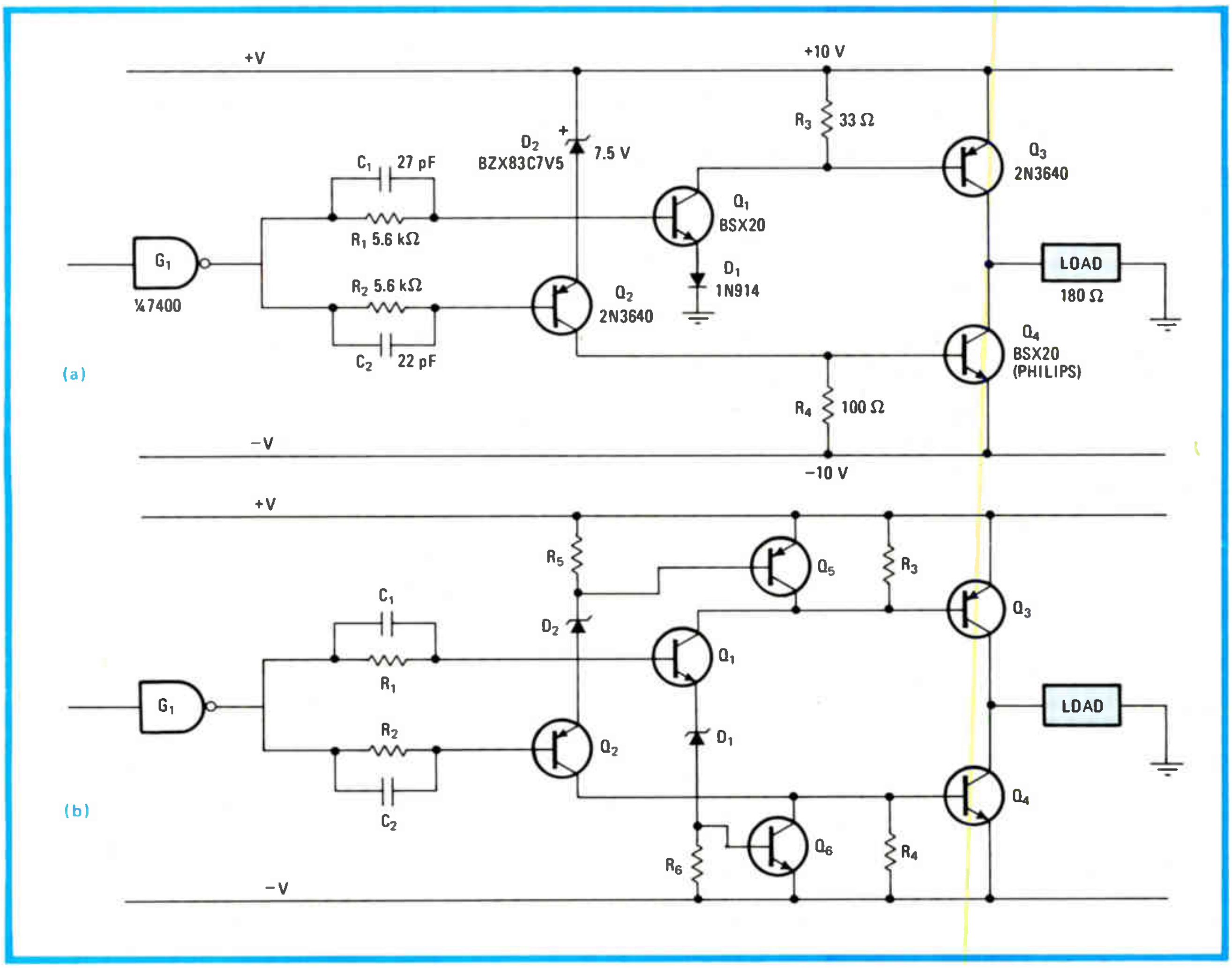
One disadvantage of this circuit is that it is possible for $Q_3$ and $Q_4$ to be conducting at the same instant during a change of state to cause a supply current spike whose magnitude may exceed the nominal load current by more than three times. Also, most of the power lost in the output transistor will be dissipated during a change of state when both are in the active region. Thus, the average dissipation will be proportional to the switching frequency. These problems may be minimized by increasing the zener voltage, $V_Z$, so as to increase the dead zone between the input threshold levels of the circuit. Switching speed may be increased by optimizing the value of the speed-up capacitors $C_1$ and $C_2$, operating $Q_3$ and $Q_4$ at very large base currents, and reducing $R_3$ and $R_4$ to minimize storage time.

This basic circuit can also be used to control far larger currents than 100 mA, providing appropriate output transistors are used. However, the storage time of these devices then becomes a major problem, and so speed is sacrificed. The circuit in (b) shows how to reduce the delay time by adding two transistors for supplying reverse base current to whichever output transistor is in the act of turning off.

Here, when the TTL output goes high, $Q_1$ conducts and $Q_3$ saturates as before, while $Q_2$ turns off and $Q_4$ begins to come out of saturation. In addition, the emitter current of $Q_1$ turns on $Q_6$, which provides a path for the escape of charge stored in the base of $Q_4$. This effectively shortens $Q_4$'s turn-off delay.

When the TTL output goes low, then $Q_1$ and $Q_6$ turn off, $Q_2$ and $Q_5$ conduct, $Q_4$ saturates because of the base current supplied by $Q_2$, and $Q_3$ is rapidly turned off because of the action of $Q_5$. Discharge transistors $Q_5$ and $Q_6$ should be selected for high-speed saturated switching, so that they will not delay the turn-off of their associated output transistors.

Adding $Q_5$ and $Q_6$ will reduce the storage delay of the output transistors by a factor of from 2 to 4. The circuit in (b) provides a rise and fall time of about 80 nanoseconds for a load of 11 ohms (2-ampere load). The active pull-up output ensures the interface's low output impedance in either the logic 0 or logic 1 state. A further advantage is that the output voltage is specified within narrow limits in both states, unlike the case with totem-pole–type circuits. □




**Conversion.** Interface (a) for translating the 0-to-5-V TTL swing into arbitrary bipolar levels at moderate switching speeds works well at low load currents. For increased loads, circuit (b) offsets the large storage delay of the output transistors and reduces crossover switching.

# Engineer's newsletter

### Two pages pack in info on the 8080/8085

For engineers and programmers working with the 8080 and 8085 microprocessors, there's a useful new design aid and instant reference called a Micro Chart—two colored 8½-by-11-inch plastic sheets with punched holes for notebook use. Micro Chart 100A consists of useful software and hardware information for the two processors, including a full-page **instruction-set summary, a hexadecimal-to-operation-code conversion, software interrupts,** the ASCII character set, hexadecimal-to-decimal conversion, status flags, restate instructions, and timing examples. The price is $2.95, plus $1.00 for postage and handling. Write to Micro Logic Corp., Department CE, P. O. Box 174, Hackensack, N. J. 07602.

### How to specify printed-circuit boards

Ever find that information on printed-circuit manufacturing and specifying is hard to come by? If so, you'll be glad to have a 16-page technical manual from Dynacircuits that gives a clear, concise description of single-sided board manufacturing. It has sections on the selection of laminates and laminate properties and two special sections in which over 30 typical **questions are answered about dies and tooling and how to design pc boards** in terms of artwork, legends, and solder resist. Contact Fred Stein, Dynacircuits Inc., 11230 Addison St., Franklin Park, Ill. 60131.

### NBS offers standard measurement for optical line-widths

As integrated-circuit line widths head down, optical measurement of line-width accuracy on the photomask becomes ultracritical. The National Bureau of Standards is now offering a Standard Reference Material for calibrating optical microscopes used to measure line widths on IC photomasks. It is **made from an antireflective chromium photoplate using standard photolithographic techniques** and measures 6.35 by 6.35 by 0.25 cm (2.50 by 2.50 by 0.10 in.). For line widths in the 0.5-to-10-$\mu$m range and accurate to within 0.05 $\mu$m or better, it can be used for calibrating opaque lines on clear backgrounds or clear spaces on opaque backgrounds and for calibrating line spacings and line-to-line space ratios on video micrometer systems. It also includes a series of lines for checking for mechanical and optical errors in the measurement system. It is unsuitable for calibrating systems using partially transmitting systems such as iron oxide photomasks, opaque materials, or silicon wafers or for use with scanning electron microscopes. The optical microscope line-width measurement standard, SRM 474, is available for $3,600 from the Office of Standard Reference Materials, National Bureau of Standards, Washington, D. C. 20234.

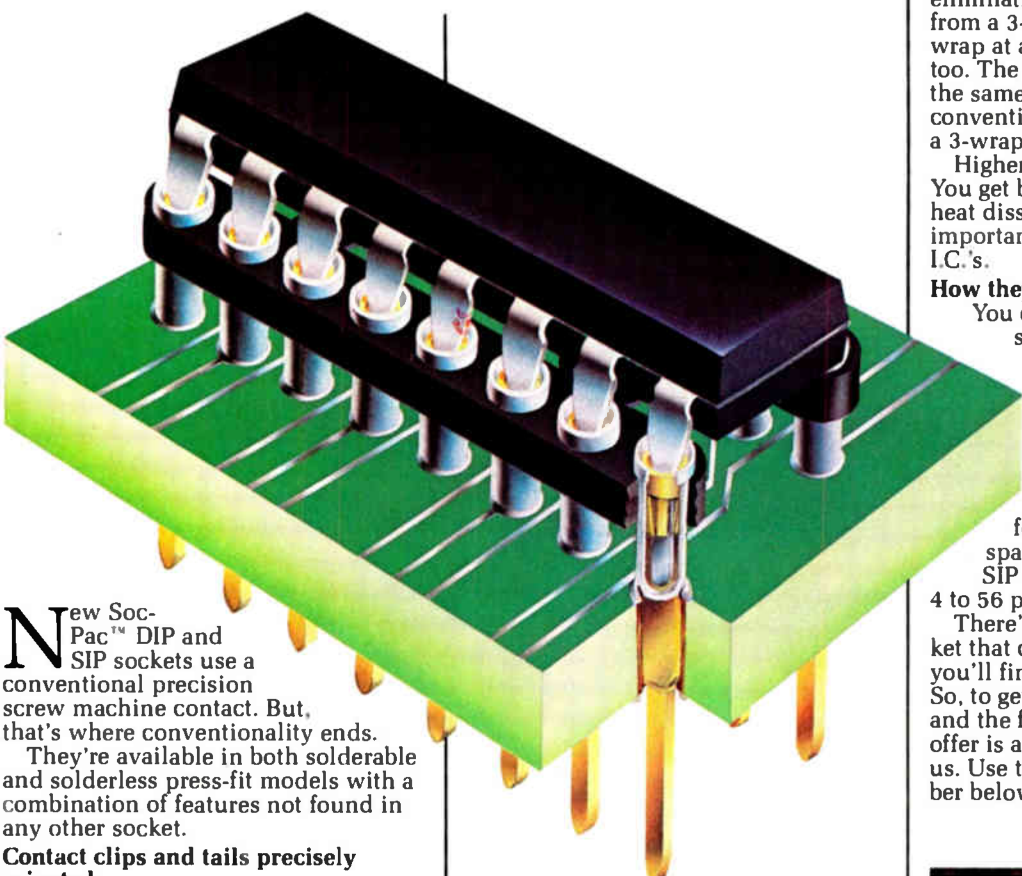
### Frequency-response analyzers can solve mechanical problems

Frequency-response analyzers using digital signal processing can be a great help in solving mechanical problems encountered in vibration analysis, acoustics, and automatic control. Hewlett-Packard Co., Palo Alto, Calif., is presenting a free one-day seminar on this topic at 30 locations throughout the U. S. and Canada from September through December. The seminar will cover the details of basic measurements. Numerous actual case histories will be reviewed, emphasizing the benefits that can be derived from effective measurements. There will be **demonstrations of problem solving in nodal analysis, machine balancing, servo design, signature analysis of rotating machinery, and acoustic intensity,** all employing the frequency-response analyzer. For more information, contact the closest HP field sales office.

**-Jerry Lyman**

# A major improvement over traditional I.C. packaging methods.

## How a simple socket can mean greater reliability, greater design flexibility at a lower cost.



New Soc-Pac™ DIP and SIP sockets use a conventional precision screw machine contact. But, that's where conventionality ends.

They're available in both solderable and solderless press-fit models with a combination of features not found in any other socket.

**Contact clips and tails precisely oriented.**
Tines of each contact clip are precisely oriented for perfect alignment with I.C. leads. The result — four contact points at every lead every time, a redundancy that costs you no more than conventional designs.

Also, each tail is oriented square and parallel with the others to easily accept mating connectors.

**Selective gold plating.**
The contact clip is plated with 30μ in. gold over nickel. The screw machine contact can be selectively plated starting from the tip of the tail (.250" minimum) — with the exact gold thickness you need. That can mean significant savings.

**Solderless press-fit advantages.**
With solderless press-fit Soc-Pac sockets, you get the savings that eliminating the soldering step make possible. And, you get a gas-tight mechanical *and* electrical interface with the plated-thru hole in the PCB. There are still more advantages to the Soc-Pac design.

**Get higher density, more flexibility.**
Contrary to the trend to low profile sockets, Soc-Pac sockets stand relatively high on the PCB. There are very good reasons for that.

It allows us to reduce pad size to 0.055" on press-fit and 0.050" on solderable sockets. Which means you can run a trace between contacts for greater printed circuit density. And greater design flexibility. Additional printed circuitry translates to eliminating at least one tail wrap — from a 3-wrap tail to a 2-wrap, or no wrap at all. You keep compactness, too. The two-wrap tail allows about the same board to board spacing as conventional low profile sockets with a 3-wrap tail.

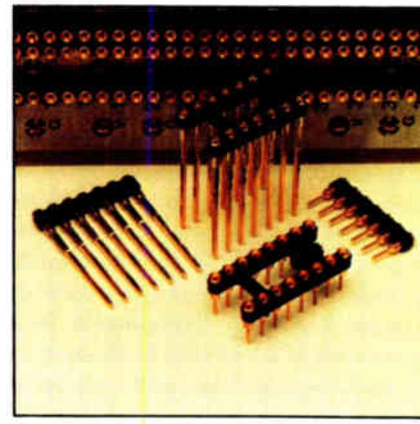
Higher sockets also add reliability. You get better air flow, thus better heat dissipation. That's particularly important with higher pin count I.C.'s.

**How they come.**
You can select either solderable or solderless press-fit Soc-Pac sockets in selective gold over nickel, tin, or nickel finishes.

DIP sockets come in 8, 14 and 16 pin counts for a 0.100" x 0.300" grid spacing and 24 and 40 pin counts for 0.100" x 0.600" grid spacing.

SIP Sockets come in strips from 4 to 56 pin counts.

There's no other socket on the market that combines all the features you'll find in the Soc-Pac™ socket. So, to get the savings, the reliability, and the flexibility Soc-Pac™ sockets offer is a simple matter of contacting us. Use the address and phone number below.



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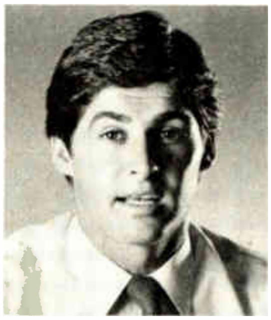
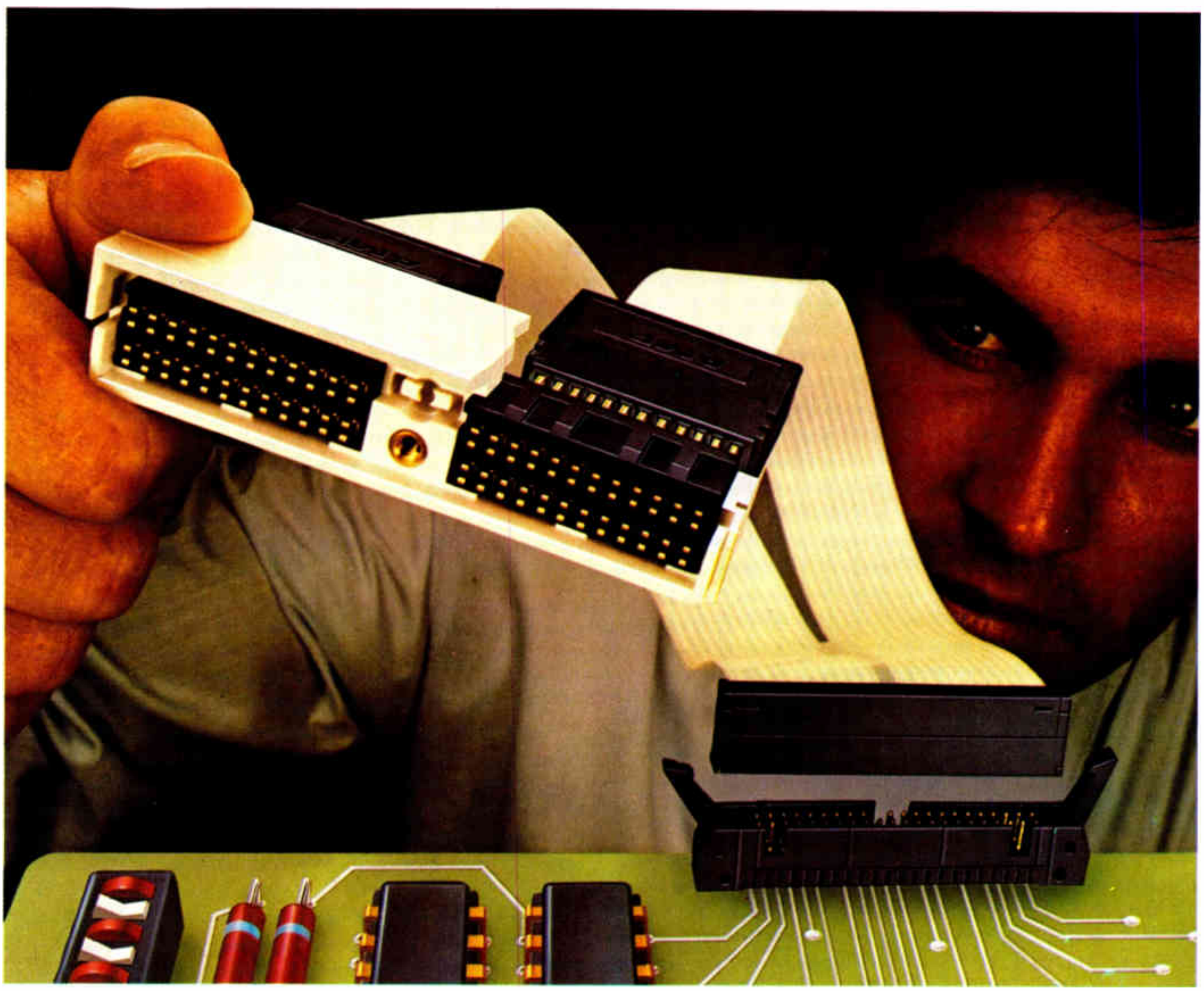
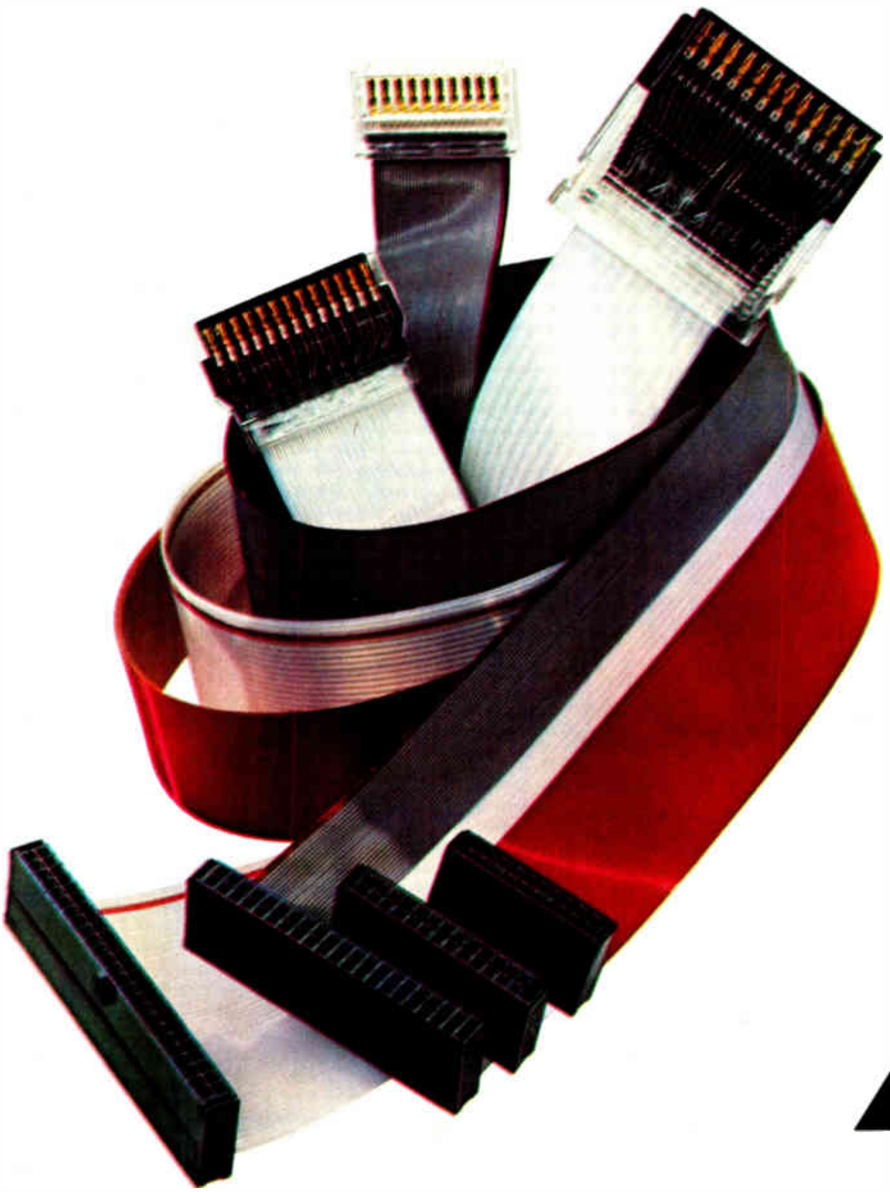
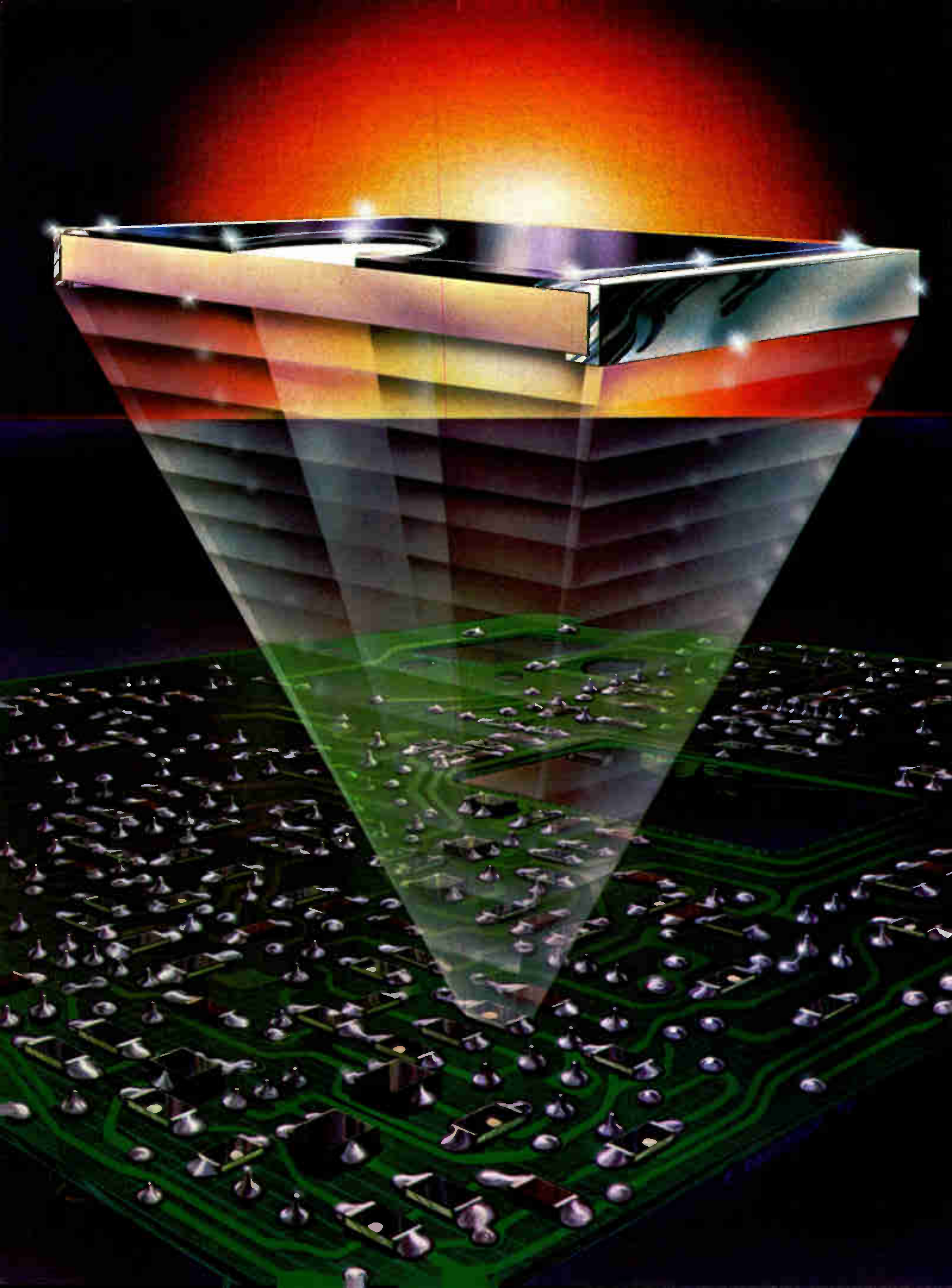
Circle 163 on reader service card



# "AMP has revolutionized transmission cable interconnects with low-cost assemblies."



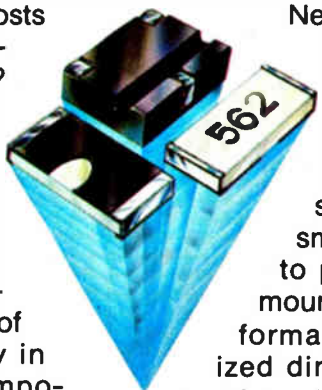




# MOUNT AN ATTACK ON ASSEMBLY COSTS

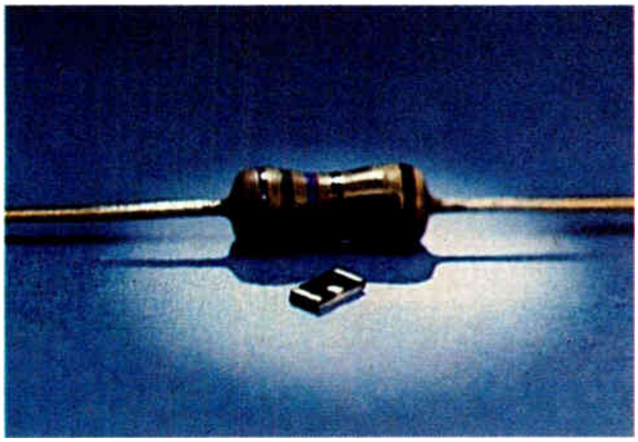
## WITH R-OHM'S NEW FLOW-SOLDERABLE CHIPS

Now you can slash your assembly costs and create thinner, smaller, more reliable products at the same time. How? With our new flow-solderable resistor and semiconductor chips.




### Start using both sides of your PC boards

Hundreds of these new chip components can be attached to either side of your PC boards in seconds. Already in widespread use in Japan, these components have fostered the development of high-speed magazine loading and tape and reel attachment methods. Once attached, the chips can be flow-soldered along with axial or radial-leaded components. Together, these developments are making dramatic reductions in assembly and labor costs possible.



Nearly 200 chip resistors (1/16W) can be mounted in just four square inches. This great density, coupled with the fact that the chips can be mounted on both sides, drastically reduces PC board size. The end result is thinner, smaller, lighter products that cost less to produce. In addition, the ability to mount chips opposite IC's provides performance improvements. And, standardized dimensions are making board layout and product design faster and more straightforward.

### Make a solid connection to reliability

Flow-soldering directly to the chip instead of to leads provides a solid, more dependable connection — a connection you can trust even in the most severe environments.

R-Ohm already offers a wide variety of dependable chip components. Chip resistors are available for 1/16, 1/8 and 1/4W applications with 2%, 5% and 10% tolerances over a wide range of ohmic values. Chip transistors and diodes are offered for a variety of functions and applications. Many more components are on the way.

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Circle 167 on reader service card

# Super D*

Rapid Solderless Termination 4-point Contacts Eliminate Wire Stripping.

Super D Adaptor System For D-type Connectors

Choose From Four Standard Super D Connector Sizes...
9 (on left), 15, 25, and 37 (right) contacts.

# A unique all plastic snap-locking connector system that costs less and does more than standard D-Subs.

## Here's Why Super D* is "The D With The Difference".

Different? You bet! TRW Cinch's all new Super D connector system has the exclusive design features and cost saving benefits that move it to the top of any D-Sub line!

Let's begin with cost savings. Most D-subs require soldering or crimping. Not Super D connectors. Our new pre-loaded pin/socket contacts provide solderless insulation displacement 4-point termination.

This unique contact also gives you twice as many contact points at mating end as other D-sub designs. All without wire prepping or stripping. Result? Immediate assembly time reduction and a positive cost savings with increased reliability!

But that's not all! Besides fast, solderless termination, Super D connectors also have snap-on plastic hoods that feature an exclusive Latch-N-Lock design for positive, audible locking with no additional tools, parts or labor. Just push to connect, squeeze and pull to disconnect. It's that easy!

To convert standard TRW Cinch D-subs to the Super D system, ask us about our special adaptor system for D-type connectors.

Looking for style and design? Look no further! Super D's cost-effective all-plastic assembly is both smooth and functional to complement the styling of your computer, peripheral, data communication, instrumentation or video equipment.

This plastic design effectively insures against shock hazards.

Super D connectors employ *selective* gold plating only where it is needed. We've eliminated expensive gold from non-functioning surfaces. So you get performance without added cost.

The Super D connector is available in four sizes (9, 15, 25, and 37 contacts) for cable-to-cable and cable-to-panel modes. Each will intermate with existing D-type connectors. And, you'll be glad to know that the Super D system is designed to meet EIA Standard RS449 plus IS04902 and 4903 for your DTE and DCE equipment.

To further speed your termination time, TRW Cinch has designed three terminating tools specifically for the Super D connector system. Use Auto-Clinch D* for high volume; Certi-Clinch D* for moderate production and field installation; and Uni-Clinch D* for field repair.

So take a long, hard look at the D-subs you're using now. Then, take a look at Super D connectors. There *is* a big difference! To get the Super D difference, write or call your TRW Electronic Component Sales Office ...listed in EEM, or TRW Cinch Connectors, A Division of TRW Inc., 1501 Morse Avenue, Elk Grove Village, IL 60007. 312/981-6000

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# 8-bit a-d converter has 12-bit linearity

Error-distribution scheme and fast conversion time ensure reliable output in noise-filled environments

*by Linda M. Lowe, Boston bureau*

**The ADC-881 successive-approximation** analog-to-digital converter overcomes the effects of its own nonlinearity. It accomplishes this by effectively scattering linearity errors over its own full-scale range. Thus randomized, the errors average out over a large number of samples, just as noise does, to leave a high-quality signal.

Datel-Intersil Inc., which originally designed the ADC-881 for medical-imaging systems, reports that its method of diffusing nonlinearities makes the 8-bit unit better than 11 times more linear than comparable converters. In fact, its integral and differential nonlinearity, rated at 0.0087% of full-scale range (or 0.022 least significant bit), are specifications more likely to be found in a 12- or 14-bit device. [*Electronics*, Aug. 28, p. 33].

This, along with the converter's 1.5-$\mu$s maximum conversion time, suits the ADC-881 to environments where analog signals may be buried in noise. Under such conditions, useful conversions usually depend on making many fast, repetitive measurements to improve certainty of the signal's level by averaging out random noise.

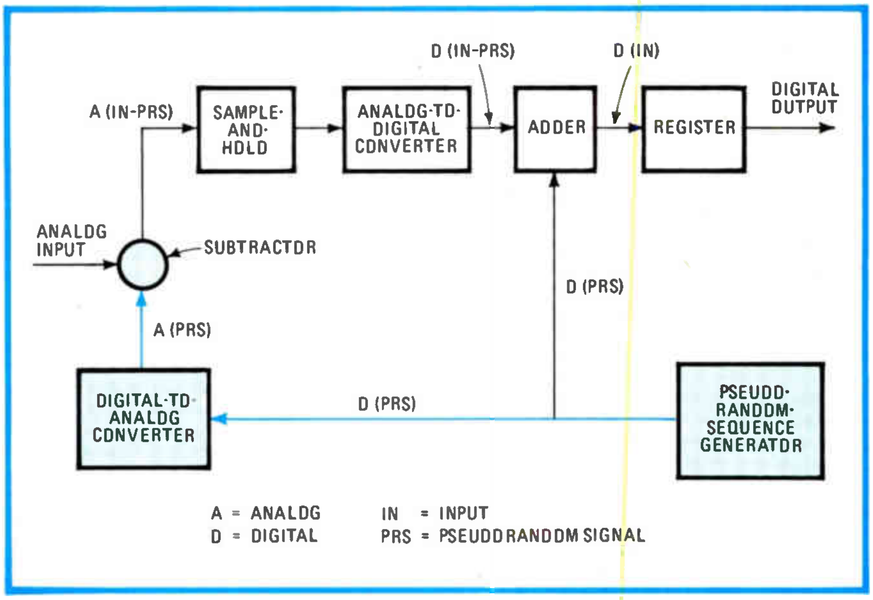
**How they do it.** In a standard device, such repeated conversions of the same analog input would build up a large, cumulative linearity error, since nonlinearities tend to cluster at the transition (also called major-carry) points of any conversion. If the analog input signal remains the same, so will the transition points. And that effectively confines errors to one narrow band of a converter's full-scale range, where they repeat with each successive sample and combine to degrade linearity.

So the trick is to shift the transition continually, thus making errors occur at different parts of the full-scale range with each successive conversion. This the ADC-881 does by incorporating a pseudorandom sequence generator to produce a new 8-bit noise signal for each analog input (see illustration). A digital-to-analog converter changes that signal to analog form for subtraction from the input. Thus altered, each input goes into conversion, each transition point shifts slightly from those of other conversions, and linearity errors subsequently appear as random occurrences.

Following conversion, the sequence generator's original noise signal is added back in digitally. That restores the complete input signal for digital output.

External techniques that average the results of numerous measurements include histograms compiled from digital outputs and autocorrelation. In the case of a histogram—a frequency distribution of sample data into discrete categories—the ADC-881's differential nonlinearity is so slight as to eliminate the computational processing of digital data generally needed to compensate for converter distortion, according to Datel-Intersil. The result is that the new converter can be used to perform real-time, statistically valid processing of analog data.

**Where the markets are.** The new and still developing field of medical imaging is one of many possible markets for the ADC-881, believes




**Error correction.** Analog-to-digital converter uses noise to reduce linearity error. An 8-bit pseudorandom digital noise signal is converted to analog form and subtracted from analog input. Then each noise byte is added to result of a-d conversion.

## New products

Wayne E. Marshall, senior project engineer at Datel-Intersil. "Anywhere you have to cope with massive amounts of noise, requiring repeated measurements to obtain accuracy, this approach works without sacrificing throughput," he says. The firm looks for applications in a variety of areas, including signal and spectrum analysis, vibration analysis, industrial testing, sonar digitizing, and geographical research.

The ADC-881 will sell for $445—high for an 8-bit converter, but not so out of line in Marshall's view, considering the unit's exceptional linearity. "You'd probably have to resort to a 14-bit converter to get comparable performance for the tasks we're addressing," says the project engineer.

**Some of the specifications.** The ADC-881 uses a magnetically and electrostatically shielded enameled-steel case measuring 3 by 5 by 0.375 in. Depending on the model, it operates at 0° to +70°C, or at −55° to +125°C. Maximum gain and offset temperature coefficients respectively are ±30 parts per million/°C and ±25 ppm/°C. Gain and offset errors adjust to zero, and internal (unaveraged) noise is 0.2% of full scale.

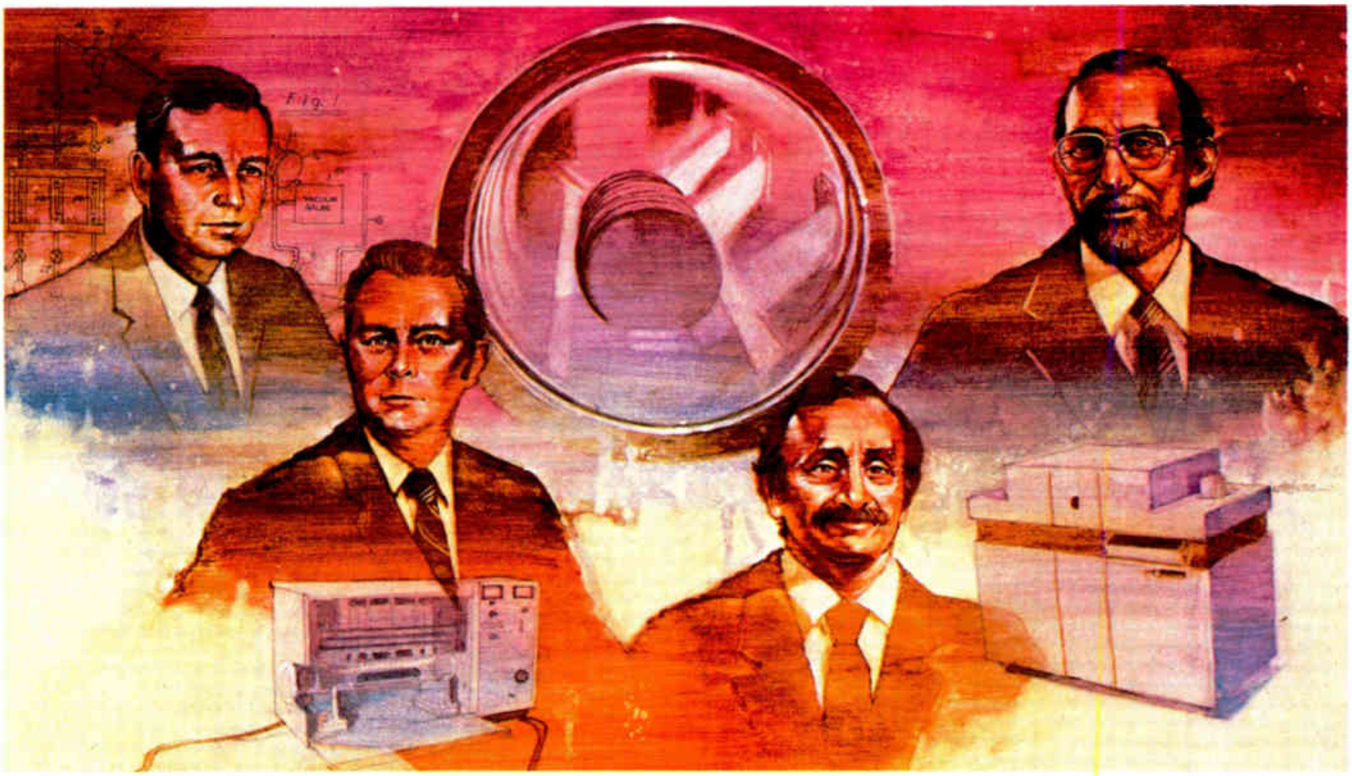
Able to accomplish an 8-bit sampling and conversion in a maximum of 1.5 µs (1.3 µs is typical), the ADC-881 may well be one of the fastest successive-approximation converters around, claims Datel-Intersil's Marshall.

It accepts analog inputs of ±5 V. The output is in offset binary code, with an output-overrange logic signal flagging any values outside the unit's range.

Datel-Intersil intends the ADC-881 as the first of a line of linearity-enhancing devices. "This approach is applicable to other products, obviously," says Marshall. "We'll be paying attention to the experience and the responses we get with this first one to determine where to take the technique from here."

Delivery of the ADC-881 will take eight weeks. Quantity discounts will be available.

Datel-Intersil, Inc., 11 Cabot Blvd., Mansfield, Mass. 02048. Phone (617) 339-9341 [338]



*Gene Lemons (upper left) and Steve Irving (lower left) first recognized the potential for plasma processing at Signetics. Their work in the 1960s with Richard Bersin (lower right), first at LFE and then at International Plasma, resulted in the first plasma etchers and strippers. In the 1970s, Alan Reinberg (upper right) at Texas Instruments explored plasma deposition and brought about wide-scale use of planar plasma reactors. Lemons' and Irving's early equipment (left) is contrasted with today's automated plasma systems.*

*No. 8 in a series*

# SEMI Presents... Great Moments in Semiconductor History

Plasma technology, which is replacing many wet chemical processes with more-controllable dry processes, had its first great moments in the early 1960s. While searching for an improved way to strip resists from silicon wafers, Stephen Irving and Gene Lemons at Signetics began exploring plasma equipment made by LFE Corporation for analysis of organic matter. The result, after a period of development with LFE's Richard Bersin, was a patent for Irving and Lemons and the first plasma photoresist stripper for LFE.

After founding International Plasma Corp., Bersin worked with the Signetics team on extending plasma chemistry to etching; in fact, Irving left Signetics to join in this effort. The result this time: another patent for Irving and Lemons and IPC's introduction of the etcher/stripper.

Other developments were taking place at Texas Instruments, where Alan Reinberg was pursuing the use of plasma for nitride deposition, based on exploratory work by Sterling and Swann at STL Laboratories in England. His efforts brought about the first wide-scale use of planar plasma reactors.

Now both Reinberg and Bersin are at Perkin-Elmer, pursuing future great moments in plasma technology. Many such advancements first surface on the exhibit floor or in the technical sessions at SEMICON—such as the upcoming SEMICON/East (where Dr. Reinberg will chair a technical session) and our new SEMICON/Southwest. Plan to be at one or both of these shows. Don't miss out on a single great moment in semiconductor history.

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**SEMICON/Southwest**
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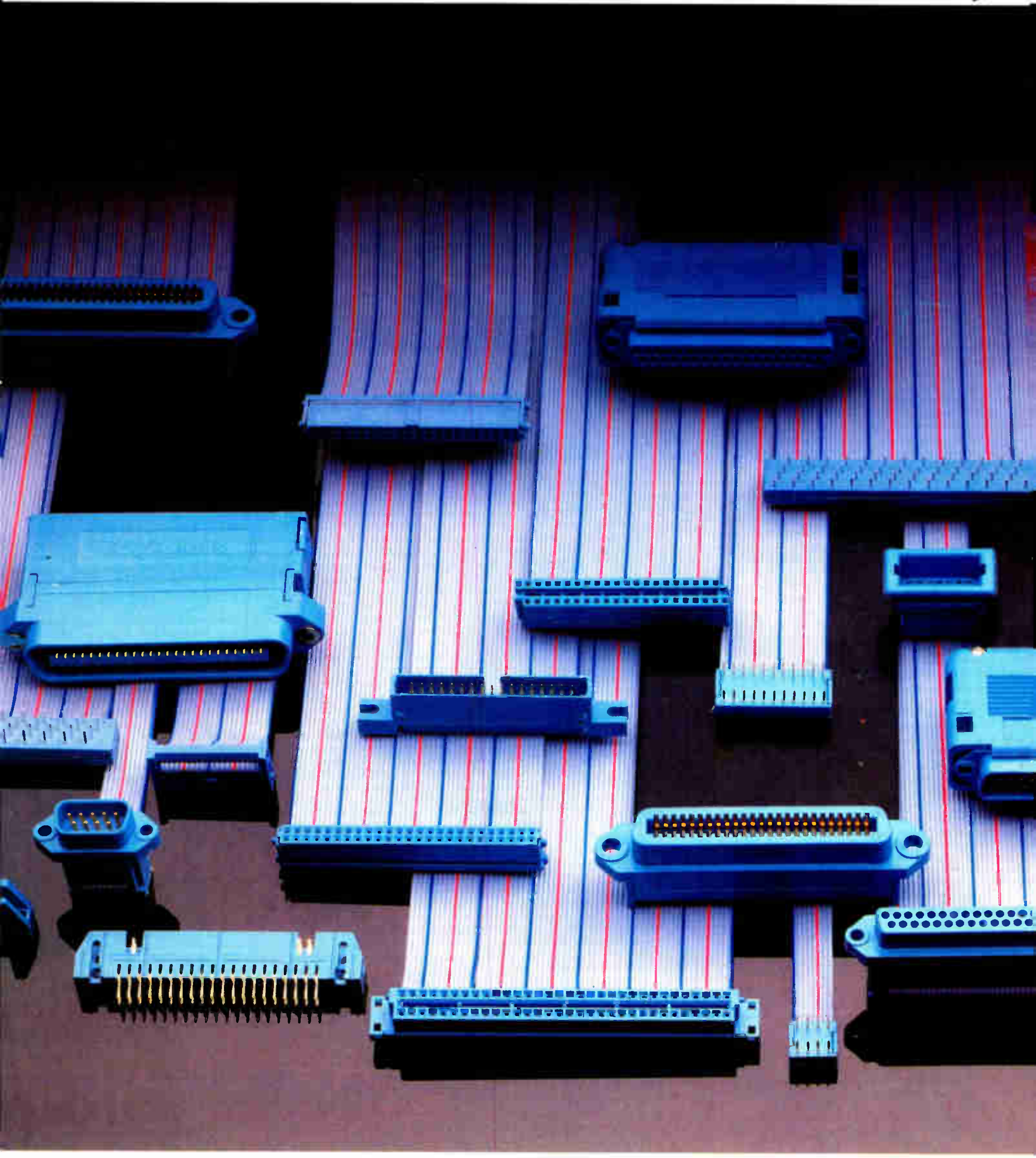
# You either have it,



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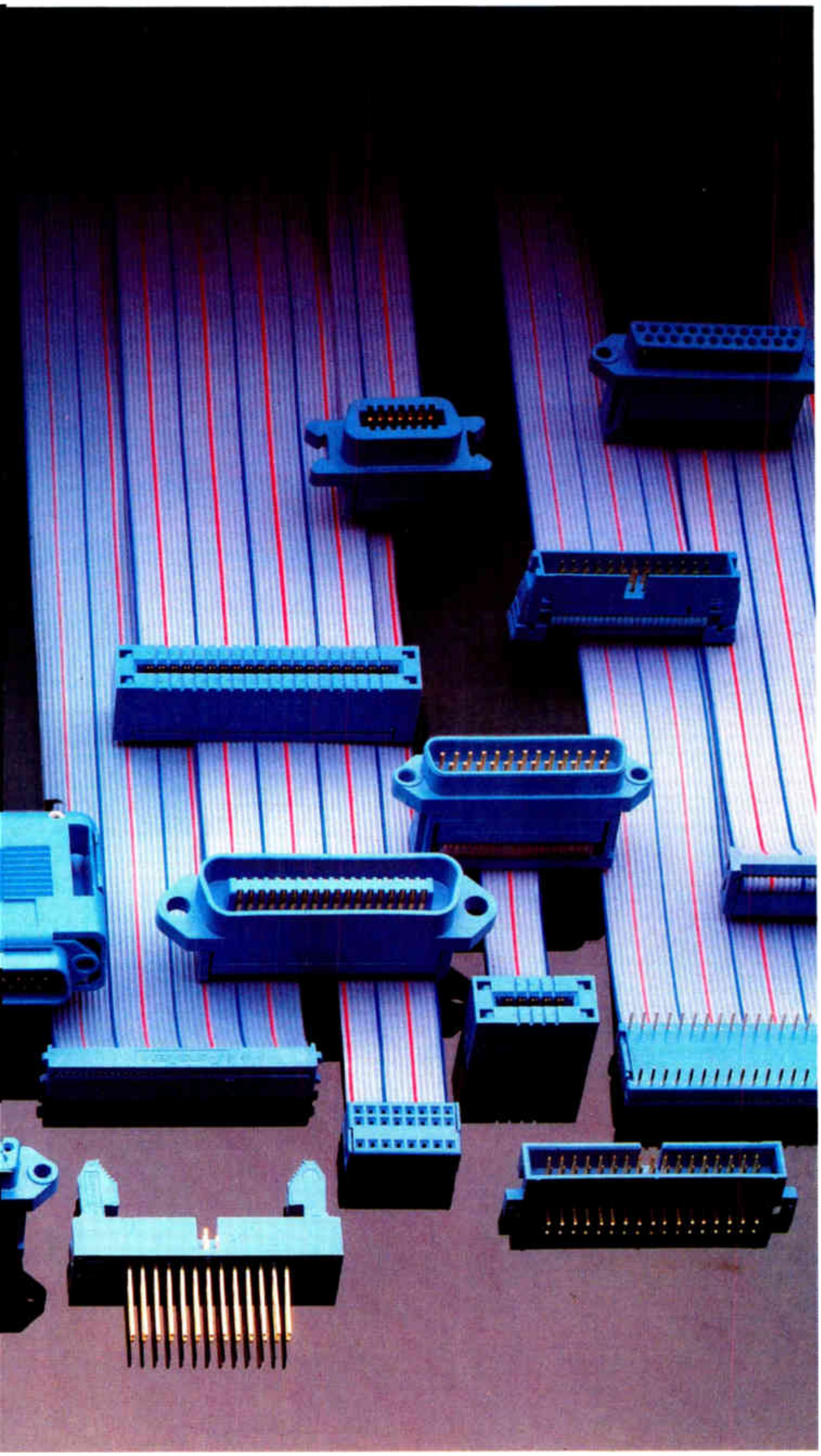

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Circle 175 on reader service card

# Computer board has room for more

A low-cost 8086-based single-board computer includes on-board area to accommodate user breadboard designs

*by Martin Marshall, West Coast Computers & Instruments Editor*

**Filling a perceived** gap in the Intel single-board-computer product line, a company founded by former Intel employees has created a unit based on an 8086 16-bit microprocessor that lets the user breadboard his application on the same card. "Generally, Intel is not interested in customizing boards or in consulting," asserts Microbar president Ray Burkley, "and that's where we come in."

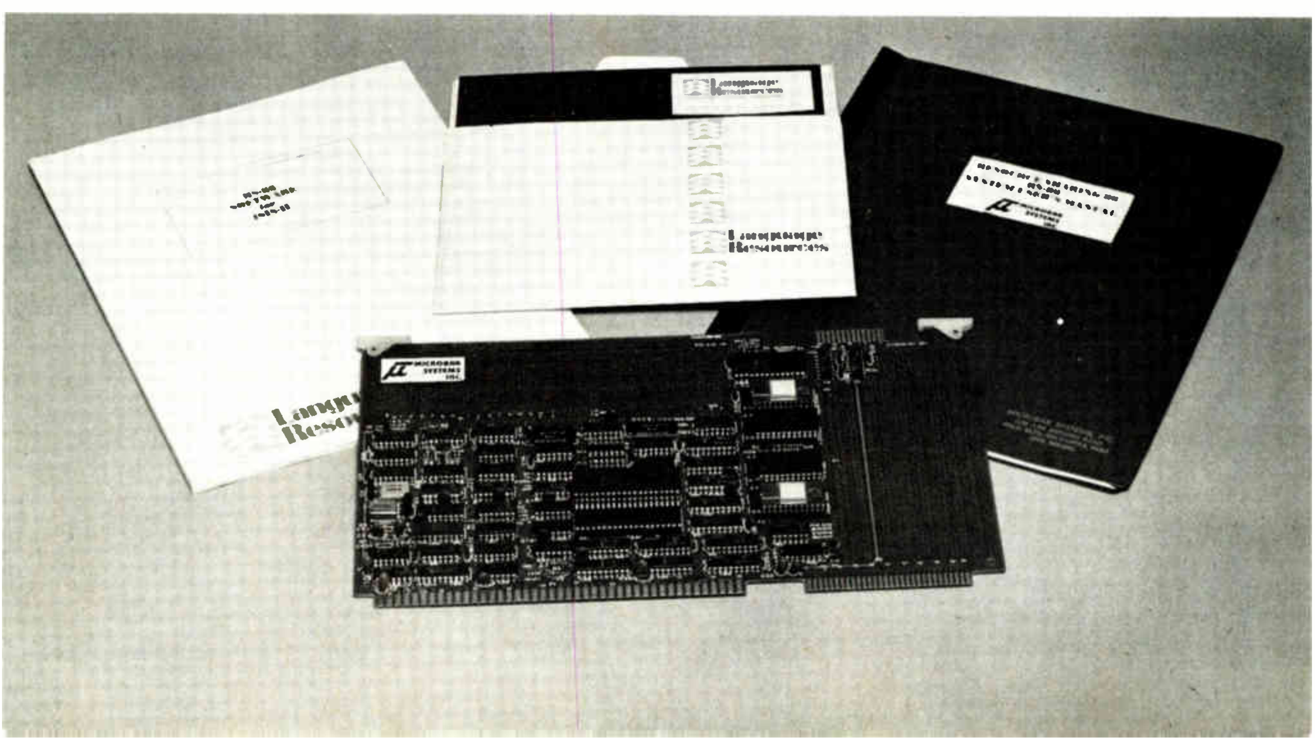
The Custom-86 printed-circuit card conforms to Intel's Multibus form factor; it contains Multibus and RS-232 interfaces, a complete 16-bit computer, and a breadboarding area. What it does not have is the 32- to 64-K bytes of random-access memory, the interrupt chip, and some of the input/output and timer functions residing on Intel's 86/12B single-board computer. It also does not have the $2,460 price tag of a fully loaded 86/12B. Instead, the Custom-86 sells for $995 (in single quantities) in the 5-MHz processor version with 4-K bytes of RAM or for up to $1,395 for the 8-MHz version with 4-K bytes of RAM.

The Custom-86 provides two breadboarding areas on the card with a total space available for about 45 16-pin integrated circuits. One area, between the serial port and connector, is for additional memory. This section has connections for the 20-bit address and 16-bit data-bus lines of the microcomputer, all fully buffered.

**A place for connections.** A second breadboarding area above the microcomputer is intended primarily for I/O functions. Here are the connections for the microcomputer's control lines, interrupt control section, programable read-only-memory chip-selection lines, I/O chip-selection lines, and some prototyping interconnections that feed into the Multibus interface. At the top of this breadboarding section, connection points are provided for a 50-pin wrapped-wire flat-cable connector.

Aside from the 2- or 4-K bytes of RAM in the microcomputer section, there are four sockets that can mix and match up to 32-K bytes more of RAM and PROM. An additional 40-pin socket near the 8086 is intended to hold an 8087 math-processor chip, if needed by the user. The serial RS-232-C port provided by the Custom-86 has user-selectable transmission rates, and it can have either a synchronous or asynchronous interface.

**Also an upgrade.** Building upon the features of the Custom-86, Microbar also offers the upgraded RS-86 development system for the 8086. This includes the Custom-86 board, an 8086 monitor program, a microprocessor disassembler, some additional firmware that allows the Custom-86 to function in a development system, some ISIS-compatible control software on a single- or double-density diskette, and an RS-232



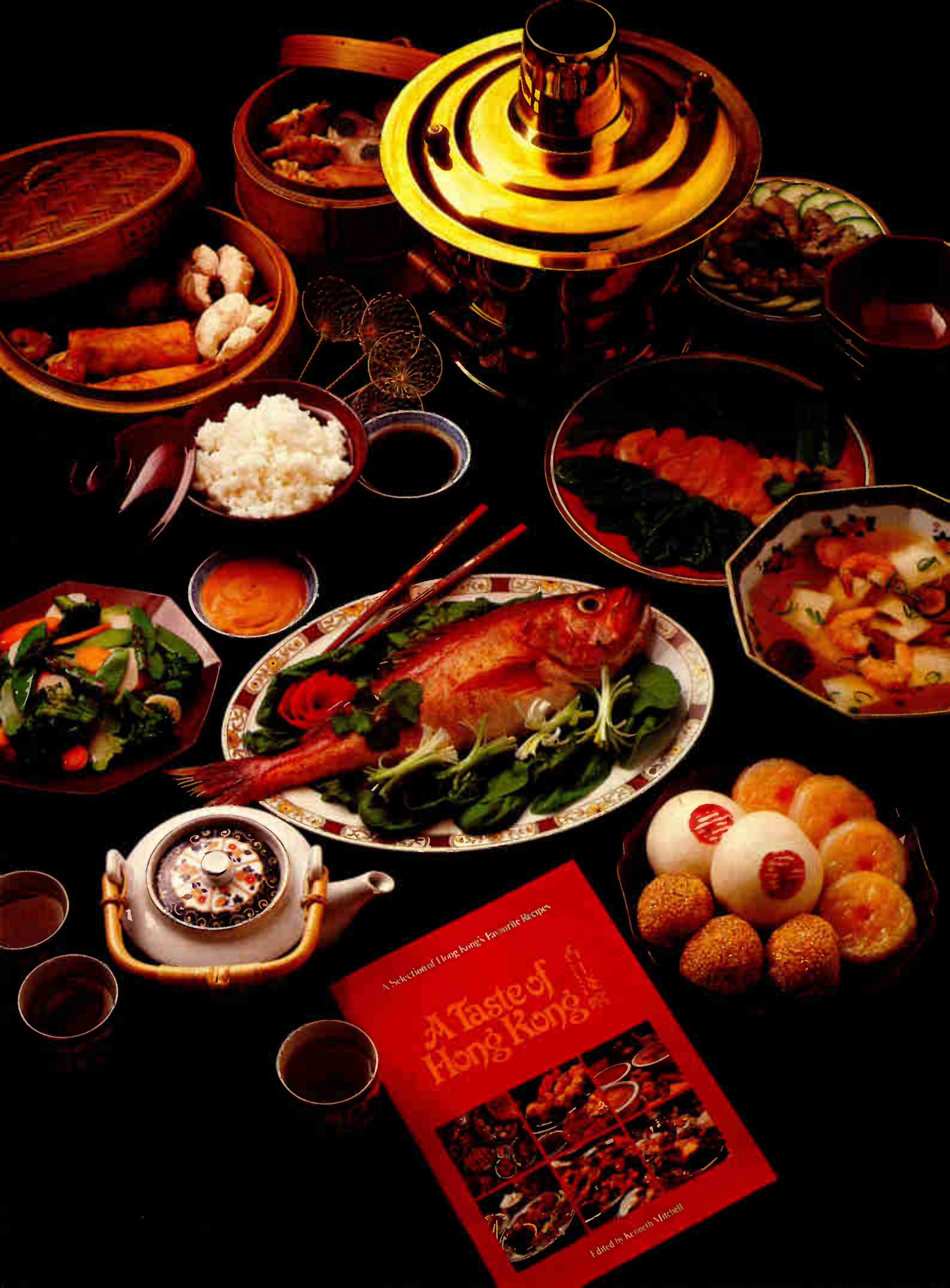
connector and cable. The 8086 monitor program, MON86, is contained in two 2716-type ROMs. It provides a downloading file command, single-step execution, setting of up to two breakpoints, and the display, substitution, comparison, filling, and moving of memory. It can also receive or transmit through an I/O port and examine the registers of the microprocessor. The disassembler program, DIS86, resides in an enhanced version of the MON86 ROMs. It generates assembly-level instructions from 8086 machine code. Both the monitor and the disassembler can change relative jumps into absolute locations and then display those locations.

"Basically, the RS-86 provides an 8086 execution vehicle for a model 800 or series II Intellec development system for a much lower price than the Intel upgrade while also allowing the user to develop his software on the target system itself," notes Rod Allen, Microbar's vice president of engineering.

**The comparison.** The upgraded Intel 8086 (model 556) costs $7,500, and Microbar's 5-MHz, 2-K-byte version of RS-86 costs $2,450. These are not exact comparisons, however, since the Intel upgrade includes the added memory of the 86/12B processor board. Intel also offers more development capability in its ICE module ($5,500 extra). "It's true that our RS-86 doesn't have the emulation capability of the ICE 86, but the primary use of that emulation would be in debugging the hardware of the Multibus interface and the microcomputer," notes Allen. "We already supply a debugged microcomputer and interface."

The RS-86 is aimed at the market for upgraded Intellec systems, but it can also be applied to other IEEE-796-Multibus-based development systems. With changes in its software only, the RS-86 could also be used to upgrade National's Starplex development system or the System 29 available from Advanced Micro Computers.

Microbar Systems Inc., 1120 San Antonio Rd., Palo Alto, Calif. 94303. Phone (415) 964-2862 [339]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Circle 181 on reader service card

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While other testers operate at a leisurely 1.8 MHz, Series 70 gives you data rates to 5 MHz across all digital pins in parallel and collects probe data at full test speed. It offers faster, more accurate fault isolation, and it lets you program timing increments with 20 ns resolution. You can even track bus-related faults at full speed with Series 70.

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Compared to today's best known functional tester, Series 70 offers specifications that are truly impressive:

| | Series 70 | An older tester |
|---|---|---|
| SPEED | 5 MHz | 1.8 MHz |
| PROGRAMMABLE PULLUP RESISTORS | Yes | No |
| COMPUTER | Specially designed dual bus architecture 16 bits 64 K words memory (128 K bytes) | PDP-8 12 bits 32 K words memory (48 K bytes) |
| SIMULATOR | High accuracy Can be run on tester | Longer debug time Have to add memory |
| MASS STORAGE | 12 or 24 MB disk | 2.4 MB or 4.8 MB disk |
| SOFTWARE | Virtual memory | Overlay & linking |
| EDITOR | Continuous on-line operation | Call-up mode |
| SYSTEM INITIALIZATION | Totally automatic | Boot from TTY |
| DIAGNOSTIC CAPABILITY | Fault tracing to the component level with FLO-TRACER | No equivalent |
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# Manchester converter fits service bus

Intended for MIL-STD-1553 serial bus, device decodes data, then converts it from serial into parallel form

*by Pamela Hamilton, New York bureau manager*

**A committee of** Air Force, Navy, and Army representatives recently adopted the MIL-STD-1553 as a serial data bus to transmit information between electronic subsystems in military equipment. In order to convert this information from a serial format into a usable parallel format, ILC Data Device Corp. has designed the Bus-8937—a Manchester II converter—to be used with the MIL-STD-1553 data bus.

The 8937 accepts the serially encoded data from the company's Bus-8553 transceiver, decodes the Manchester data, and then performs a serial-to-parallel conversion. The device transmits this parallel data as a 16-bit TTL signal to the operational subsystem through internal double-buffered three-state outputs. When parallel data from the subsystem is presented to the 8937, the process is reversed. Any data going to or from the subsystem is transferred over a common 16-bit bus.

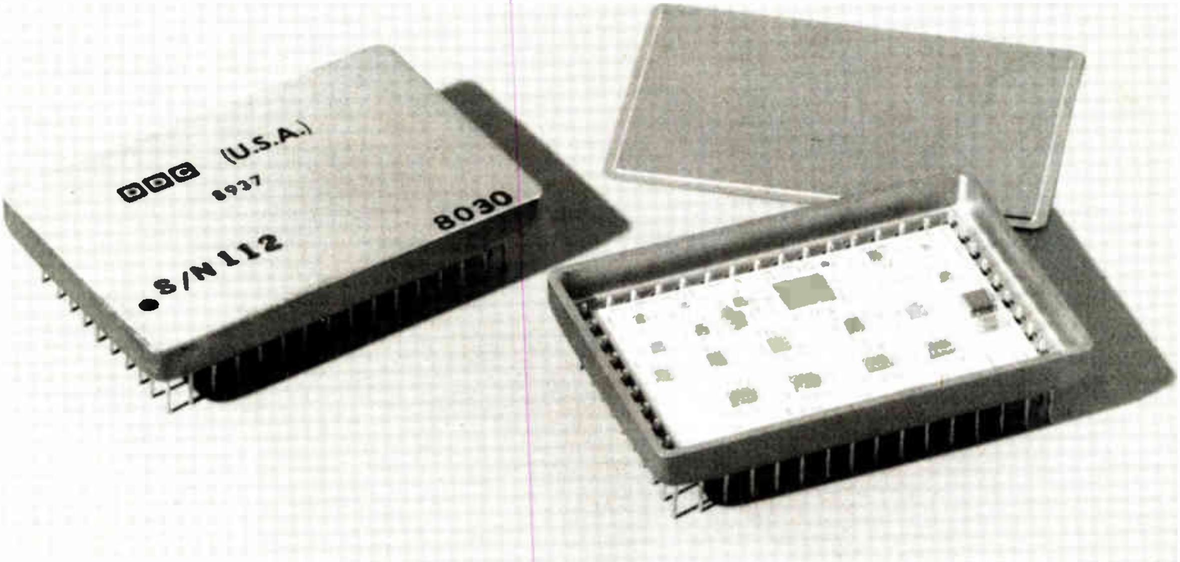
The word length of the Manchester-encoded data used over the 1553 bus is fixed at 20 bits sent at a 1-MHz rate. The first 3 bits form a synchronization period and as such are an invalid Manchester signal. Next come 16 bits, compatible with microprocessor operations, carrying the information. Last is a parity bit. Each bit is sent in 1 $\mu$s. "The decoder in the 8937 strips off the synch pulses and parity bit and sends the remaining data to the serial-parallel converter," notes Albert DiMarino, product manager.

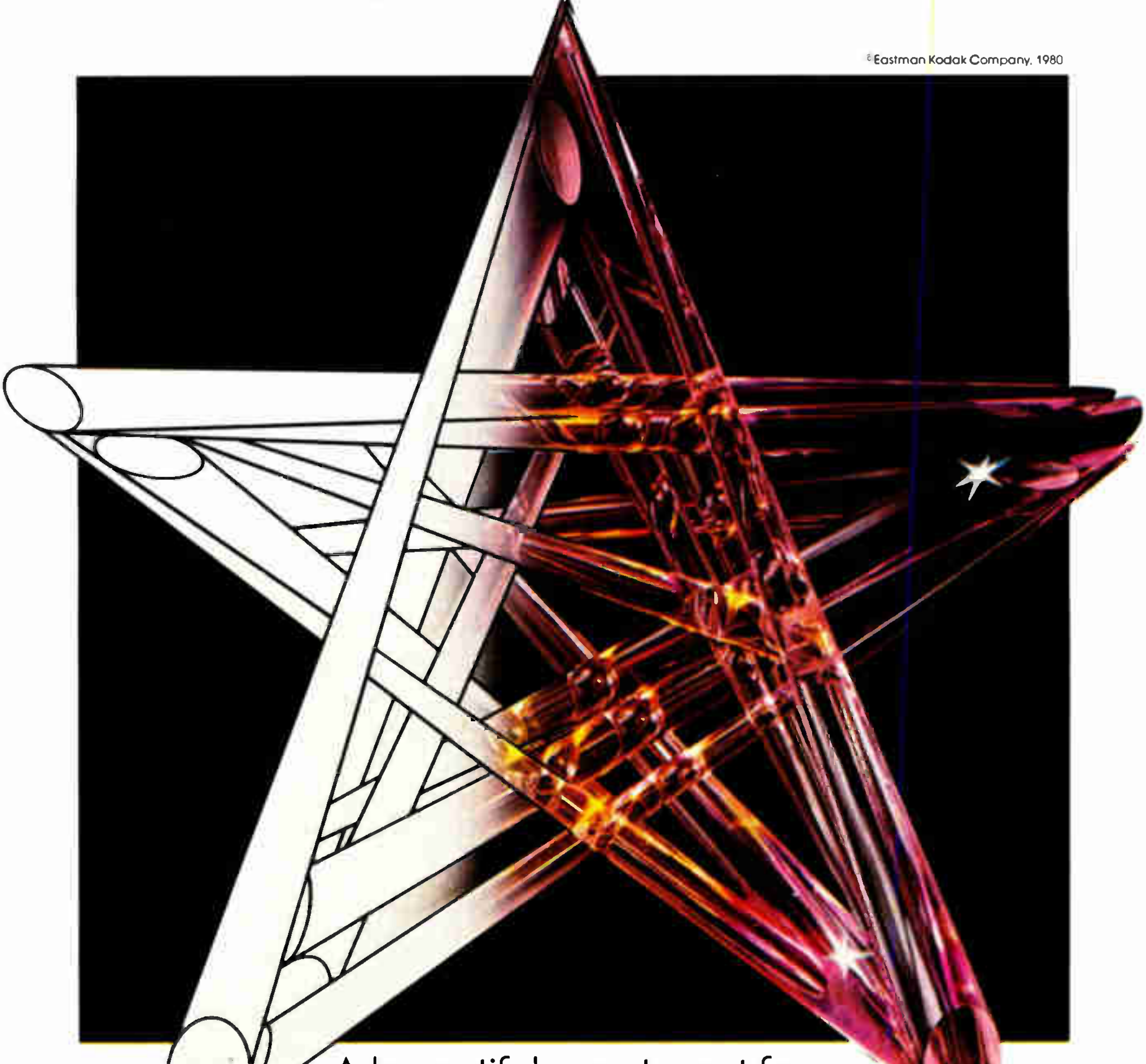
**Address recognition.** Up to 32 subsystems may be hung from a single MIL-STD-1553 data bus. Therefore DDC has provided an address-recognition capability with its 8937. The device incorporates 5-bit address decoding and can provide a valid-address signal to the subsystem once that address is verified. The unit is also equipped with a wraparound self-testing capability.

The 8937 is a hybrid device built to MIL-STD-883 and is screened to applicable portions of methods 5004 and 5008. The circuit contains 18 integrated circuits housed in a 1.7-by-1.1-by-0.2-in. package. The unit requires 200 mA maximum from a +5-V dc power supply. The operating temperature range of the device is −55° to +125°C measured at the case, with a storage temperature range of −55° to 150°C.

The Bus-8937 sells for $450 in single quantities, with delivery from stock to 90 days.

ILC Data Device Corp., 105 Wilbur Place, Bohemia, N. Y. 11716 [340]





Instruments

# Modular DMM starts at $765

### 8 plug-in cards adapt multimeter for a variety of tests and buses

Data Precision might well have called its new 5½-digit multimeter an MDMM, or modular digital multimeter. Although essentially a $765 conventional DMM with most of its functions under microcomputer control, a library of eight modules can equip it to do quite a bit more than just measure dc voltage and make three-wire ratiometric dc voltage measurements.

The modules can be installed in the field into the half-rack-wide 3600. Though the use of some of them precludes the use of others, a fully equipped 3600 could perform a broad range of measurement chores. Among the features:

- Resistance measurement, 1 to 20 MΩ, for $120.
- Average ac voltage measurement, 1 μV to 800 V, for $145.
- True root-mean-square nonsinusoidal ac voltage measurement to 800 V in two versions priced at $200 and $325.
- Binary-coded-decimal remote-programming and data-output interface for $100.
- IEEE-488 bidirectional bus interface for $200.
- 1-GΩ impedance with an isolated, four-wire ratiometric input costing $200.
- A rear-panel input jack set for an additional $50.

Therefore "the user buys only as much meter as necessary," says Harold S. Goldberg, president. Later addition of a new function is a simple matter of inserting a card in an edge-connector slot reserved for it, plus calibration if needed.

**Using the interface.** No external translator is required for the IEEE-488 bus: the interface card is simply inserted and the unit's address keyed in with a miniature switch housed in a dual in-line package. As soon as the bus cable is connected, the system can begin operation.

Either the IEEE-488 or BCD input/output cards suits the 3600 to systems operation. These are especially low-priced options when compared with those for ac voltage measurement. The reason is the unit's 6500/1-based microcomputer; it gives some interface management to any instrument configuration purchased. But Data Precision's engineers have put the microcomputer to work in other areas, too, making use of its 2 K by 8 bits of read-only memory, 64 bytes of random-access memory, timer, counter, and four 8-bit ports.

"There is a complete self-test routine performed at turn on," says Goldberg. The unit's display, analog-to-digital converter, and other key circuits are exercised, and in the event of malfunction an appropriate code appears on the display. Typically, all a user sees is the unit counting down as its display is exercised. After this and between each

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measurement, the unit automatically zeros itself in analog fashion.

The microcomputer also is responsible for the unit's automatic-ranging function, called "opti-ranging." It reduces the search time associated with some other autoranging schemes and also eliminates the confusing displays that can flicker across some DMMs as they range and then settle.

In the opti-ranging mode, the 3600 selects a middle range and, if there is no overload indication, backs down to ranges of increasing resolution, seeking the correct one. An overload indication triggers upward movement to a higher range. This approach is quicker than the frequently used system of moving downward from the highest to successively lower ranges, according to Goldberg.

**Right the first time.** While ranging, the display is blanked; it is also blanked for a brief period while the meter and display settle. Thus the user's first reading will be the right reading.

Should a user try to measure a parameter the 3600 is not equipped for, the display reads out "error." There are error indications for almost all of the common mistakes possible with such instruments—wrong range selection, for one.

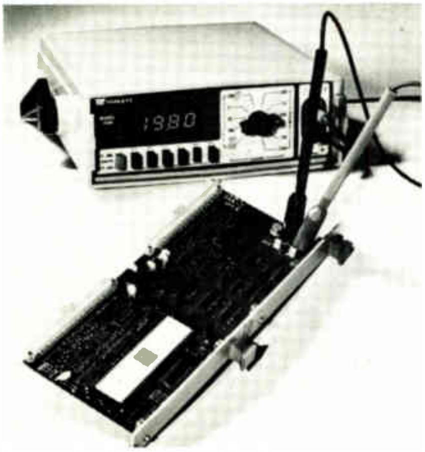
Three- or four-wire ratiometric measurements are simple: they can be set up with a push button. The standard three-wire capability enables the ratio of two voltages to be measured relative to a common point. The optional four-wire capability allows ratio measurements of dc voltage relative to separate points in a circuit offset by as much as ±7 V. Users making frequent measurements in bridge-transducer systems will find this feature useful.

Delivery is from stock.

The Data Precision Corp., a division of Analogic Corp., Electronics Avenue, Danvers, Mass. 01923. Phone (617) 246-1600 [351]

## $235 benchtop 3½-digit multimeter has 31 ranges

A 3-lb, 4-oz benchtop 3½-digit multimeter for use in circuit design, production, and maintenance testing has a wide-angle light-emitting-diode display for ease in viewing. The model 4000 has a single range-selector switch and two input jacks to serve all functions and ranges. It also offers automatic zeroing and polarity selection when used for voltage and current measurement. Full scale ranges from 200 mV to 1 kV dc or ac. For current, full scale ranges from 200 μA to 2,000 mA ac or dc; for resistance it is from 200 Ω to 20 MΩ. Input impedance is 10 MΩ on all ranges and accuracy is within ±0.2 to ±0.5%, depending on the range



selected. The LED display is 0.43 in. high. Multiple fusing to 1 kV on 31 ranges is provided, with ⅛-A power-line, 2-A input, and 3-A high-energy–type fuses included in the $235 price. The multimeter is available from stock and will be on display at Wescon.

Triplett Corp., One Triplett Dr., Bluffton, Ohio 45817. Phone (419) 358-5015 [353]

## Microprocessor system analyzer sells for $1,995

Without the need for user programming, the CT-150 microprocessor systems analyzer examines data in any of six operating modes and sells for $1,995 with a probe. The analyzer is intended for the design, development, debugging, and testing of microcomputer-based systems. The instrument offers 128-by-30-bit data collection and storage through 30 channels. It can be used with either static or dynamic memory, operating on the user's system clock or on an external clock. The analyzer is available within 30 days after receipt of an order.

Creative Technology Inc., 14415 N. Scottsdale Rd., Scottsdale, Ariz. 85260. Phone (602) 991-1491 [354]

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A rugged 1-to-520-MHz service monitor priced at $5,920 in the U. S. includes a lab-quality signal generator with a sweep-generator function, a frequency measurement system, and an oscilloscope. The signal-generator portion of the model 4200 is a synthesized source with 0.0001% (1 ppm) accuracy, 50-Hz resolution, and an output range of 316 mV to 31.6 nV. The measurement section has an input sensitivity of 2 μV and measures carrier frequency and modulation of externally generated signals, including off-the-air signals. The scope features a three-position vertical sensitivity selector and three sweep rates. Delivery is in 60 days.

Wavetek Indiana Inc., 66 N. First Ave., P. O. Box 190, Beech Grove, Ind. 46107 [356]

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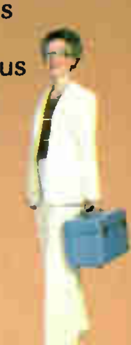

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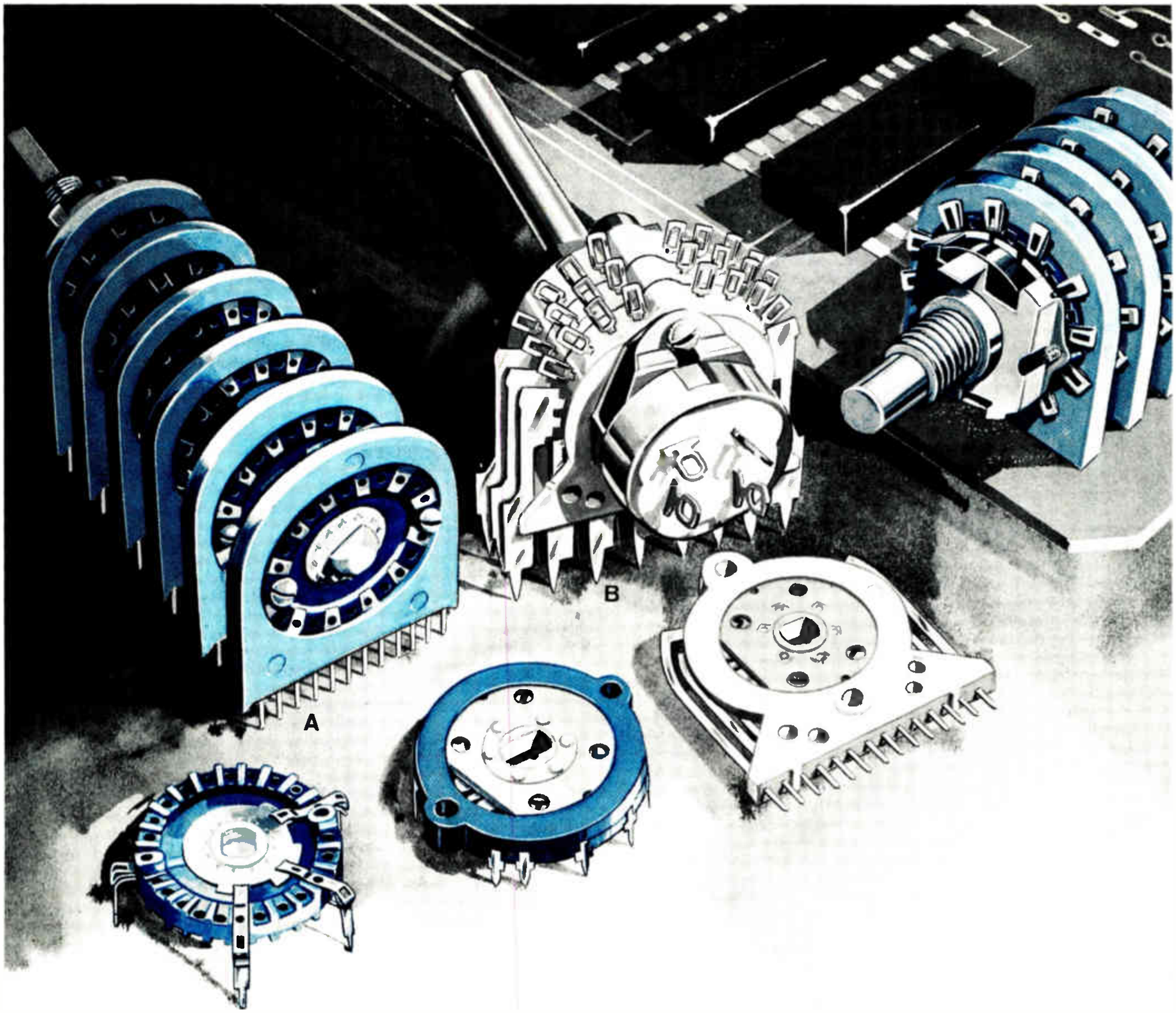


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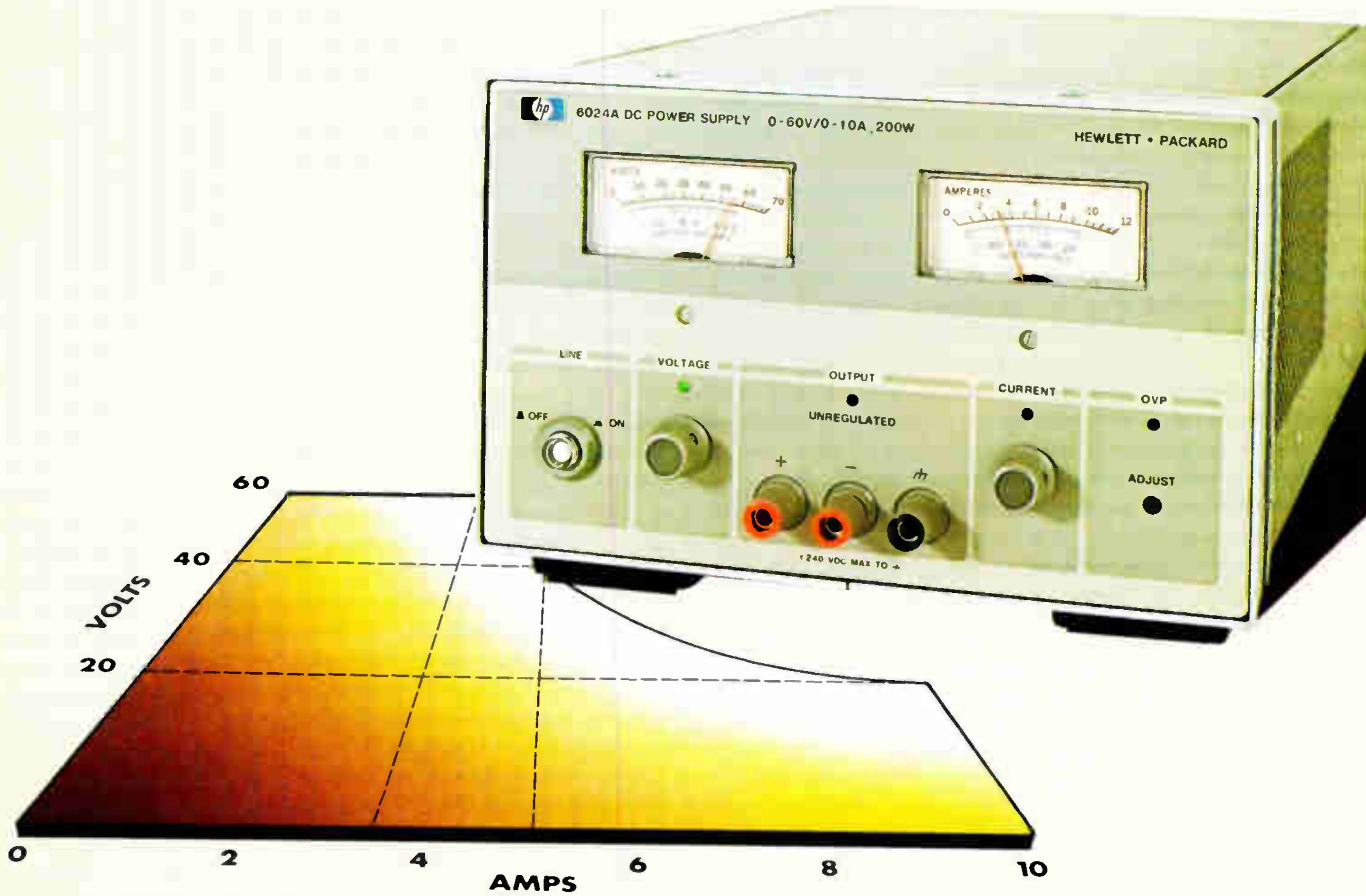


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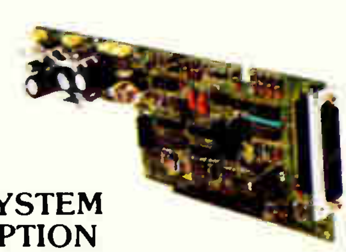

## SYSTEM OPTION

Convenient system interfacing board allows complete remote control of output voltage and current — also provides isolated readback of supply status.

Circle 196 on reader service card

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Semiconductors

# FET-input op amp slews at 120 V/μs

## Unit has 1-MHz bandwidth, 100-MHz gain-bandwidth product, 20-ns rise time

The HA-5160 operational amplifier from Harris Corp.'s Semiconductor Products division offers input performance approaching that of the firm's chopper-stabilized HA-2905, but its dynamic specifications are more like those of the company's high-slew-rate and fast-settling operational amplifiers.

Using a new monolithic integrated circuit that combines a junction-field-effect-transistor input and dielectrically isolated bipolar transistors and employs on-chip laser trimming, the HA-5160 yields input characteristics like these:

- 2-pA typical offset current, 10 pA maximum.
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- 1-mV typical offset voltage, 5 mV maximum.
- 10-to-20-μV/°C offset voltage drift.
- 10-TΩ input impedance.

All these specifications apply over a full operating temperature range of from −55° to +125°C.

The new op amp's 120-V/μs slew rate, 1-MHz full-power bandwidth, and 100-MHz gain-bandwidth product put it in a class with Harris's HA-2525 high-slew-rate device. Further, the 5160's 400-ns settling time (to 0.1%) is only somewhat less than 10 times that of Harris's HA-5195 fast-settling op amp; the 5160 has a typical rise time of 20 ns.

Thus the new device offers an offset voltage somewhat higher than on earlier high-performance units, but better input-current specifications and very good dynamic characteristics. And since input offset voltage can be trimmed to zero, there is little sting in this tradeoff.

Some of the 5160's input characteristics can be traced to the use of leakage-limiting dielectric isolation. This design feature also eliminates the phantom silicon controlled rectifiers sometimes caused by parasitic signals found in other monolithic op amps; consequently, Harris claims complete freedom from latchup for the 5160.

**Satisfaction.** Paul S. Smith, Harris's product line manager for linear products, calls the 5160 "the first FET-input op amp I have been really satisfied with" and adds that some of the techniques used to reach its levels of performance may be applied to the company's other bi-FET op amps, which combine bipolar transistors and FETs, in a future product improvement program.

He notes that the 5160's mix of specifications, plus its high gain of up to 150-kV/V input and its uncompensated closed-loop stability at gains of up to 10, suits it to a variety of applications in instruments, communications, process control, display terminals, and other areas.

According to Smith, there is no direct competition for the 5160. Though there are a number of JFET monolithic op amps available, the company's market research shows that the 5160 outslews potential competitors and may offer a higher gain or gain-bandwidth product; sometimes the difference is a factor of two or three.

Meanwhile, the 5160's input characteristics are at least comparable with those of other high-performance JFET op amps, and in many instances they are better.

Supply voltage may range from ±10 to ±20 V, and the unit dissipates about 225 mW. The typical power-supply-ripple rejection ratio is 86 dB.

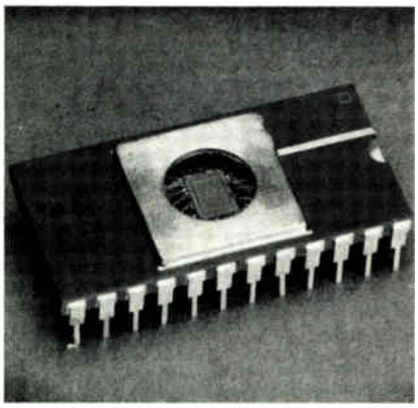
The 5160 is offered in a variety of packages, including leadless chip-carriers, and in both commercial- and military-temperature-range models. It is manufactured in compliance with MIL-STD-883, class B.

Depending on quantity, package, and temperature range, the price ranges from $4.98 to $32.10. Limited production quantities are available from stock in most package styles.

Harris Semiconductor Products, a division of the Harris Corp., P. O. Box 883, Melbourne, Fla. 32901. Phone (305) 724-7000 [411]

## 16-K E-PROM needs only one power supply

Only a single 5-V supply is required to run Motorola's new 16-K erasable programmable read-only memory, which is organized as 2 K by 8 bits. The series MCM2716 units have



access times of 250, 350, or 450 ns. They come in standard- and low-power versions. Power dissipation in the former is from 50 to 70 mA—about half that of other 16-K E-PROMs. The E-PROM is available in a frit-sealed 24-pin, dual in-line package (C-suffix). In quantities of 100 or more, the versions in this type of package range in price from $20.80 for the 100-mA, 450-ns MCM2716C to $35.95 for the 70-mA, 250-ns MCM27L16C25. All parts are available from either factory or distributor's stock.

Motorola Semiconductor Products Inc., MOS Integrated Circuit Division, 3501 Ed Bluestein Blvd., Austin, Texas 78721. Phone David Ford at (512) 928-6660 [413]

## Op amps combine p-MOS and bipolar transistors

The CA3193B, CA3193A, and CA3193 precision operational amplifiers employ both p-channel MOS and bipolar transistors on one chip to achieve a gain-bandwidth product of 1.2 MHz. The bi-MOS op amps are internally phase-compensated. Input voltage for the model B is 75 μV maximum, 40 μV typically, with a maximum temperature coefficient of 2 μV/°C. The noise at 0.1 to 10 Hz is typically 0.36 μV peak to peak. The devices are all pin-compatible with the industry-standard 741 op amp and can serve as direct replacements for the 741 and as functional replacements for the 725, 108A, OP-5, OP-7, LM11, and LM714 op amps where nulling is not employed.

The CA3193 and CA3193A operate from supply voltages of ±3.5 to ±18 V, and the premium version, CA3193B, operates from ±22 V over the military temperature range of from −55° to 125°C. All the units are available in TO-5 packages in a variety of configurations. Depending on the model and packaging, they sell for between $1.20 and $4.75 apiece in 100-unit quantities.

RCA Solid State Division, Box 3200, Somerville, N. J. 08876. Phone (201) 685-6423 [414]

## 64 frequencies generated by programmable clock-pulse IC

The 8650 and 8651 programmable clock-pulse generator integrated circuits provide outputs at frequencies ranging from 0.0005 Hz to 60 kHz (one pulse every 33.3 minutes to one every 16.6 μs) and from 0.00083 Hz to 100 kHz (one pulse every 26.5 minutes to one every 10 μs). The 8650 has an output pulse frequency accuracy to within ±50 ppm, and the 8651 is accurate to within ±5 ppm. Every IC can generate 64 frequencies from the original frequency of its built-in crystal oscillator when programmed through a complementary-MOS divider. The operating current is less than 0.5 mA. Samples are from stock. The 8650s cost $10 apiece; the 8651s, $12.

Epson America Inc., 23844 Hawthorne Blvd., Torrance, Calif. 90505. [415]

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Circle 199 on reader service card

Packaging & production

# Production testers emulate disks

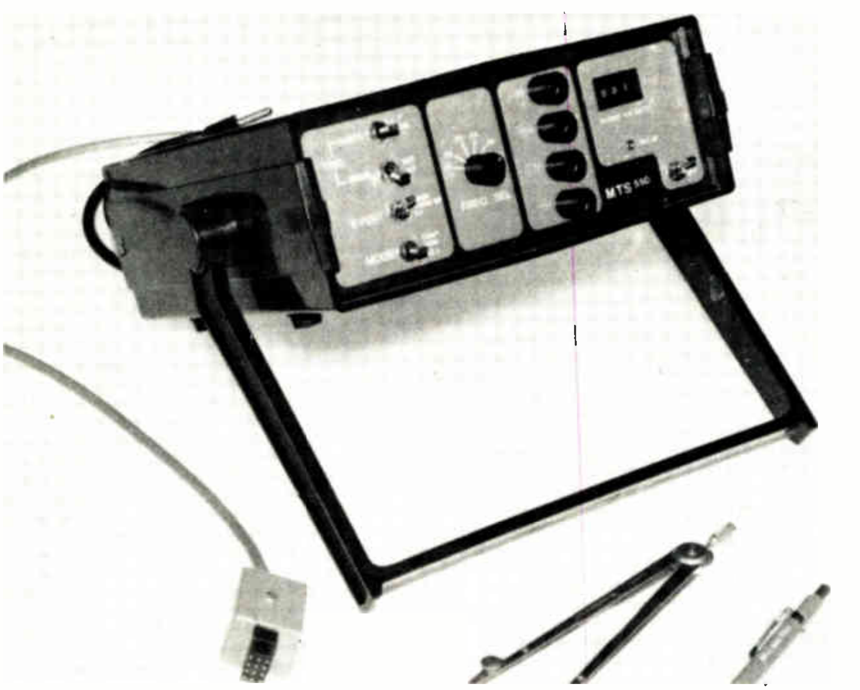
## Electronic simulation replaces electromechanical standard head-disk interface

Production testing in much of today's high-technology industry demands just as much accuracy and sensitivity as in any laboratory. Thus, the disk-manufacturing facility and disk user's facility both need to calibrate the factory's media-related test equipment. Most commonly, a reference that characterizes the standard head-disk interface is generated. However, the electromechanical nature of such a standard introduces drift uncertainties. That's where a development from Media Test Associates comes in.

The model 550 signal simulator reproduces the standard head-disk interface response electronically, and with much more control over the variables. It simulates such events as an extra bit, negative modulation (a missing bit), or positive modulation. These events, in turn, simulate defects in the disk like thin or thick coating, substrate gouges, and errors in the modulation of the coating jet spray. The length of the events are switch-programmable from 0 to 999 bits, with a resolution of 1 bit. The modulation range for missing pulses is from 25% to 90% of the average track amplitude, and positive modulation ranges from 100% to 150% of the average track amplitude. An extra pulse may be selected to have a base-to-peak amplitude of from 0.1 to 0.6 V.

**Hard or floppy disks.** The simulator can be used for both hard- and floppy-disk equipment, since it has a working frequency range of from 100 kHz to 6.4 MHz. This corresponds to a data transfer rate of 25 kilobytes/second, which is usable for floppy-disk equipment, to 1.6-megabyte/second, which is characteristic of advanced hard-disk equipment. The user can specify from one (which is standard) up to an optional five crystal-controlled frequencies that can be internally generated by the simulator. An external signal generator may also serve as a frequency source.

Two outputs are provided. The first is a single-ended, 50-Ω output, and the second is a balanced, 50-Ω differential output. The amplitude of the first output can be varied from 0 to 1.0 V peak to peak; the amplitude of the second ranges from 0.0 to 2.0 V p-p. Delays from either output can be varied from 0 to 100 μs.



Modulation events are generated only after a trigger pulse is created either internally (in the free-running mode) or externally by the application of a TTL-level signal. The triggering slope may be selected as positive-going, negative-going, or both.

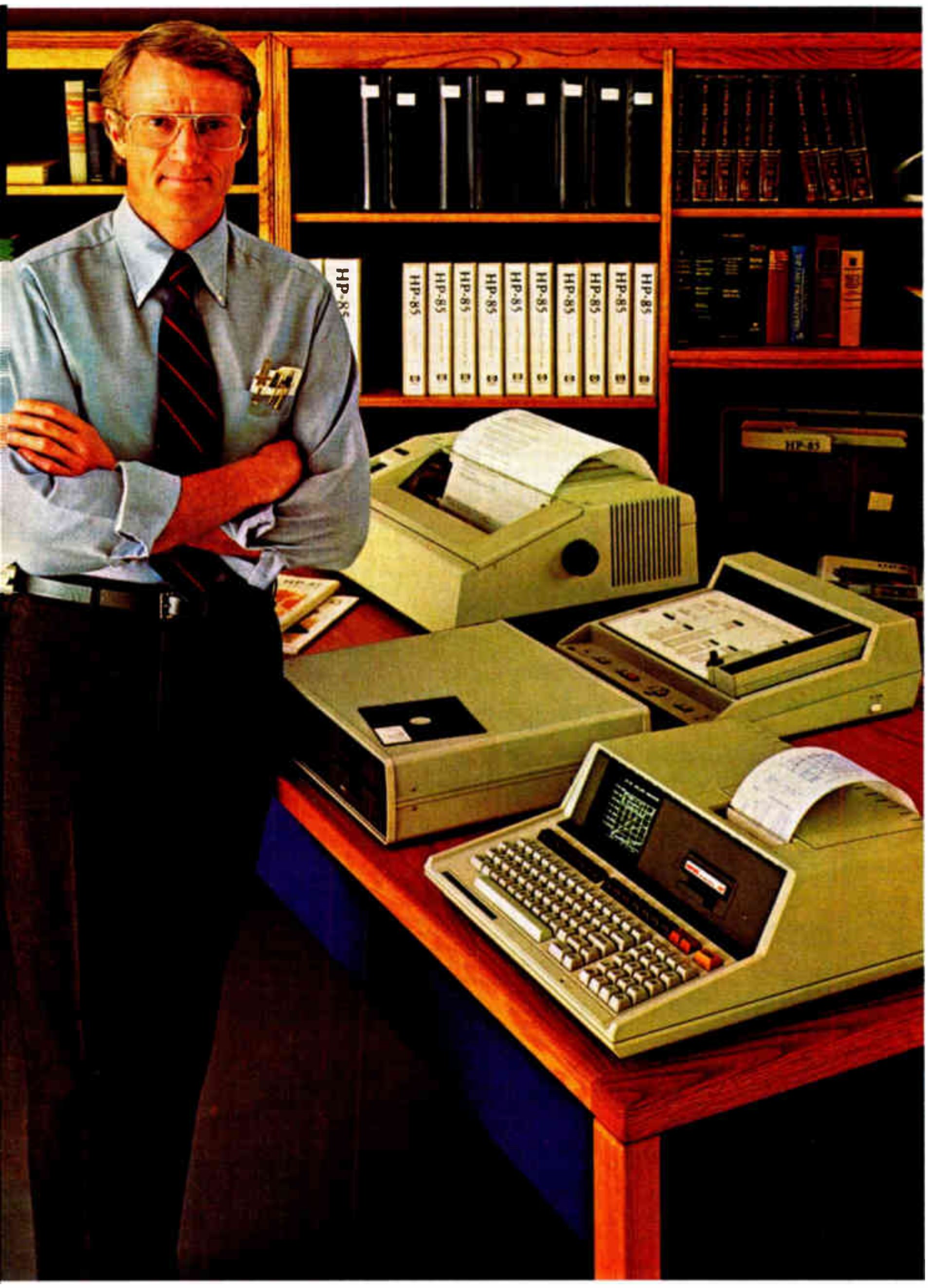
The price of the model 550 varies from $3,950 to $4,450, depending on the number of optional frequencies selected ($50 each) and whether the optional termination module ($250) is included. (The termination module interfaces the model 550 directly with the user's preamplifier and allows it to be connected directly into the head connector receptacle on the user's system.)

Media Test Specialists Inc., 761 Mabury Rd., Bldg. 14, San Jose, Calif. 95113. Phone (408) 295-8840 [391]

## Tungsten probe tips have 5-mil diameters

Because the tungsten points of the model CW-100 Catwhisker probe tips have a radius of 0.2 μm, they can test very large-scale integrated wafers and chips. The electrolytically etched tungsten point is shaped like an S spring and is 5 mils in diameter. Continuous reduction in shank diameter from tip to loop provides a spring action that protects the tip in normal usage. The Catwhisker probe is welded to the end of a 20-mil-diameter Dumet wire that is 1.375 in. long. The wire, made of a copper sheath welded to a nickel-iron core, is securely fastened to the

# Think system. Grow systematically. HP-85.

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The Personal Computer For Professionals: HP-85 specifications: Memory—16K RAM expands to 32K, 32K ROM expands to 80K; CRT—32 chars./line, 16 lines; graphics—256 X 192 dots; thermal printer—2 lines/sec.; magnetic cartridge capacity —200K; I/O—HP-IB (IEEE 488), RS-232, 16-bit GP-IO, BCD; Application Pacs include Statistics & Regression Analysis, Finance, Math, Linear Programming, Text Editing, Waveform Analysis, Circuit Analysis, BASIC Training, & Games.

HEWLETT PACKARD

Circle 201 on reader service card

probe arm. In quantities of 1 to 49, the probe sells for $5 each; for 50 or more, it sells for $4.50 apiece. Delivery takes one week from receipt of order.

Alessi Industries, 3195 Airport Loop Dr., Building C, Costa Mesa, Calif. 92626. Phone (714) 979-8912 [393]

## Sonic-beam tester measures wafer flatness in 10 s

The Flatgage test instrument uses a high-resolution sonic technique to measure wafer flatness in as little as 10 seconds, offering a resolution of ±0.1 μm. It performs 32 individual measurements on the surface of the wafer every ¼ in. For every 100-mm (4-in.) wafer, the Flatgage takes 5,760 measurements, averages them, compiles them into 180 data points, and stores them in system memory. The sonic beam allows the tester to measure the wafer without contact regardless of its optical or electrical

properties.

The fully automated system has an optional cassette-to-cassette handling and sorting subsystem that virtually eliminates operator intervention. The wafer's flatness can be displayed digitally and graphically on a cathode-ray-tube screen.

The basic tester sells for $65,000. Delivery will start in the fourth quarter of the year.

Tencor Instruments, 2426 Charleston Rd., Mountain View, Calif. 94043. Phone (415) 969-6767 [394]

## 8-slot Multibus chassis includes quad power supply

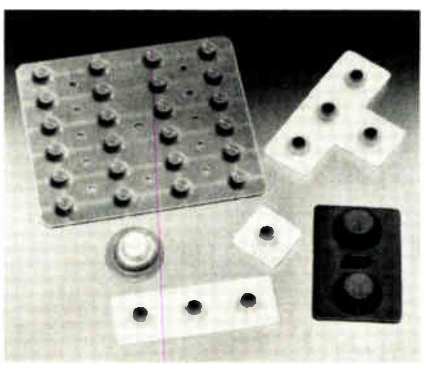
The ZX-660 8-slot Multibus chassis from Zendex is designed to be a direct form, fit, and function replacement for the Intel SBC-660. The ZX-660 features a four-output supply with 30 A available from the +5-V source. It also has NSC BLC-604/614 cardcase backplanes. Cooling is provided by fans.

The cardcase and supply may be reversed for front access to the cards, and the top and back panels can also be quickly removed. In quantities of one to nine, the ZX-660 sells for $1,929 and is available immediately.

Zendex Corp., 6398 Dougherty Rd., Dublin, Calif. 94566. Phone Rick Main at (415) 829-1328 [395]

## Conductive silicone rubber replaces metal in contacts

The series 300 and 400 contacts, made of conductive silicone rubber, can replace metal units. The devices are designed for such applications as watches, toys, calculators, and portable electronic equipment. Depending on the model, the devices have a contact-current rating of 5 or 500 mA and a contact resistance of from 100 to 1,000 or 0.5 to 5 Ω. The resistivity of the insulation used is $10^{14}$ Ω-cm. The devices have a mechanical life of 1 million cycles and a contact bounce of less than 5 ms. The operating temperature is from −40° to +100°C. The contacts



sell for from 10¢ to 20¢ each in quantities of 2,500.

Tecknit, 129 Dermody St., Cranford, N. J. 07016. Phone R. Ventimiglia at (201) 272-5500 [396]

## Gauging plunger measures holes in less than 2 s

In less than 2 s the Zi-Check gauging plunger accurately measures the diameter of small punched, drilled, or reamed holes with an accuracy of within ±0.0003 in. Useful for inspecting printed-circuit boards, as

well as electronic connectors and injection nozzles, it comes with English or metric dials and can check diameters from 0.010 to 0.330 in., or 0.25 to 8.35 mm. The price starts at $145. Delivery is from stock.

Zi-Tech Division/Aikenwood Corp., 2151 Park Blvd., P. O. Box 26, Palo Alto, Calif. 94302. Phone Jeff Ziman at (415) 326-2151 [397]

## Machine tapes component leads at 15,000/h rate

The model 2315 taping machine packages axial-lead circuit-board components for automatic board insertion at a rate of 15,000/h. The machine automatically trims and straightens leads, positioning components on double strands of pressure-sensitive tape that sandwiches the ends of the trimmed leads. Pricing starts at less than $9,000.

Universal Instruments Corp., Kirkwood Industrial Park, Box 825, Binghamton, N. Y. 13902. Phone (607) 772-7522 [398]

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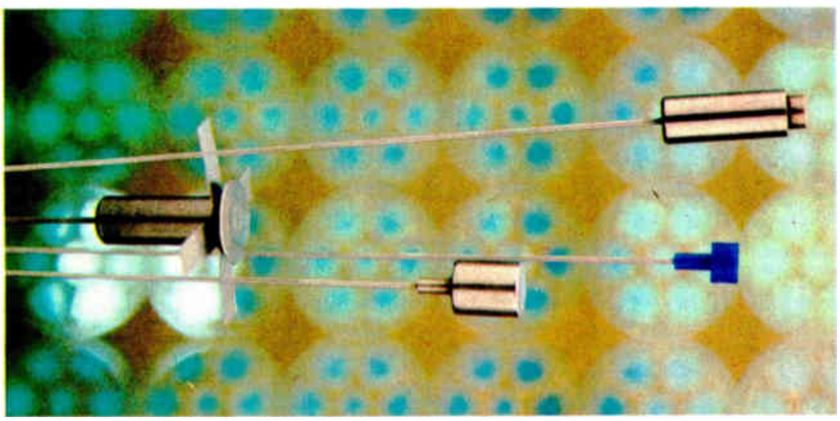
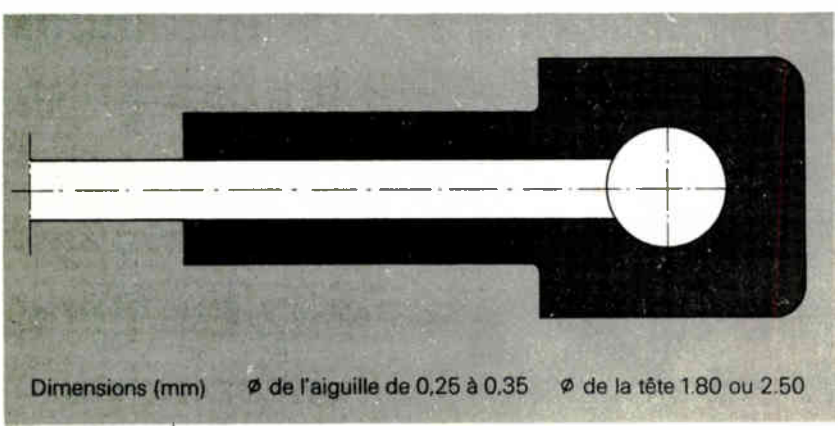
Wires for printers

Seitz

**Seitz, c´est sûr !**



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Seitz experience in the machining of hard materials has contributed to the realization of wires enabling to print characters of a perfect quality.
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Circle 205 on reader service card

Data acquisition

# Series of cards termed universal

## Variety of functions fit broad range of computer-sensor needs

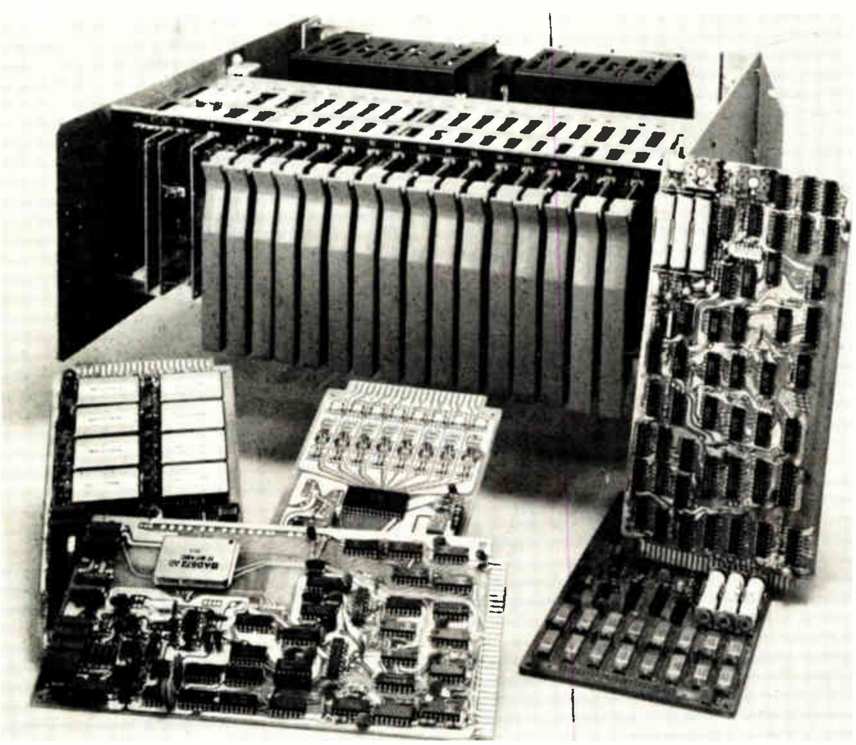
Computer Products Inc. is offering a new series of universal analog-input cards for use with its RTP line of data-acquisition and -control systems. Though universal may be a strong term, the new RTP7436 analog-to-digital converter and gate cards come in enough variety that, in combination, they should fit between computer and sensor in a wide range of applications.

One of the firm's gate cards and one converter card, for example, provide the user with analog measurement capability, while optional programmable gain stages in both card types allow them to accommodate both low- and high-level signals from such sensors as thermocouples, resistance temperature transducers, pressure transducers, strain gauges, flow meters, and thermistors.

**That's the least.** But one gate and one converter card are a minimal configuration. The RTP7436 series allows users to insert several gate cards in front of a converter card, with their number limited only by converter throughput and the number of connectors in the controller. The maximum is 15 gate cards in the company's RTP7431 universal controller and 7 in its RTP7320 universal Procom II microprocessor-based controller. For larger applications, eight RTP controllers can be linked on a single parallel bus. Coordination of gating and conversion—timing, triggering, and so on—is supplied by the rack-mount controllers. Among the new cards are:

- A 12-bit successive-approximation a-d converter card capable of 25,000 samples per second, the /20, at $630.
- A similar 12-bit converter capable of 50,000 samples/second, the /21, at $1,575.
- A 14-bit successive-approximation converter card that samples at up to 38,000 Hz, the /22, at $910.

Each converter is available with four programmable gain ranges (±1.28 V to ±10.24 V), a choice of unipolar or bipolar output formats, and programmable single-ended or differential inputs. Typically there will be one such single-input converter card for each controller rack.



**The gate in the middle.** Between the a-d converters and the sensors are gate cards to select the sensor input to be converted. Here the user has a choice of six solid-state, fast-switching gate cards or two slower, relay-based gate cards. The solid-state gate cards have a variety of characteristics:

- The /40 offers a choice of 8 differential or 16 single-ended inputs under program control and a maximum sensor-to-sensor switching rate of 38,000 Hz. The price is $180.
- The /41 has eight differential inputs only, samples at 200 Hz, and includes an 11-Hz single-pole, low-pass input filter. Its price is $210.
- The /42 is identical to the /41 but uses a 7-Hz double-pole, low-pass filter to roll off high-frequency noise. The price is $240.
- The /43 is similar to the /40 but samples at up to 50,000 Hz and lacks input filtering. The price is $220.
- The /44 has eight differential inputs, a 750-Hz sampling rate, and an 11-Hz single-pole, low-pass filter. It costs $270.
- The /45 is similar to the /44 but has a 7-Hz double-pole, low-pass filter. The price is $300.

There are two relay-based gate cards: the /30 at $425 has four differential inputs, programmable gain, a 3.3-Hz single-pole, low-pass filter and a 12.5-Hz sampling rate; its companion, the /31, is similar but has eight differential inputs and costs $730.

**All for flexibility.** This combination of gate and converter cards allows considerable applications flexibility. Add to this the capability of the RTP universal controllers to interface with more than 25 different mini- and micro-computers and the system's versatility becomes apparent. In addition, there are 8- and 16-bit digital input cards, a variety of analog and digital output cards, multichannel a-d converter cards, and other cards for special purposes such as communications, memory,

# Introducing GenRad's 1731 A/D, D/A tester.

# And how to turn it into a complete linear IC test system.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The 1731 comes with GenRad's worldwide service capabilities behind it, including local application support, handler interface expertise, and a free program library.

If you need an A/D, D/A tester with room to grow, call toll-free 1-800-343-4470. (In Mass. call 617-890-4900.) Or write: GenRad, Concord, MA 01742.

**GenRad**

Put our leadership to the test.

Circle 209 on reader service card

interrupt, and counter applications.

Delivery of cards in the RTP7436 series takes about 120 days.

Computer Products Inc., 1400 N.W. 70th St., Fort. Lauderdale, Fla. 33307. Phone (305) 974-5500 [381]

## Low-noise isolation amp works over 10-kHz bandwidth

The model IA297 isolation amplifier features both low noise and high input/output isolation over a bandwidth of 10 kHz. The amplifier operates at common-mode voltages of up to 5,000 V dc continuous. The common-mode rejection ratio is 170 dB from a balanced source impedance; with an unbalanced source, it is 160 dB. An instrumentation input provides approximately 120 dB of CMRR, but this is increased by an additional 60 dB by allowing the user to drive the amplifier shield by an active source within the unit.

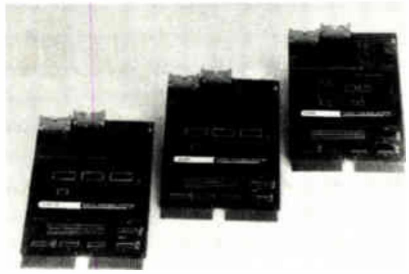
The input voltage noise is held to 1.0 $\mu$V over the bandwidth from 10 Hz to 10 kHz and current noise to 10 pA from 0.5 Hz to 1 kHz root mean square. In quantities of 1 to 9, the IA297 is priced at $225. Delivery is from stock to six weeks.

Intronics, 57 Chapel St., Newton, Mass. 02158. Phone (617) 332-6835 [383]

## Three boards expand channel capacity of analog inputs

Both hardware- and software-compatible with Digital Equipment Corp.'s LSI-11 dual-height Q-bus backplane, three dual-height expander boards increase the channel capacity of the DT2760 series of analog input systems. A single expander card can extend a 10-channel system to one with a 64-channel capability.

The model DT2772 dual-height single-board expander extends the DT2762 and DT2764 analog interface boards to factory-configured 64 single-ended (SE) or 32 differential input (DI) analog input channels. The DT2762 accepts full-scale in-



puts of ±5, ±10, or 0 to 5 V.

The model DT2775 extends the DT2765 flying-capacitor–isolated, low-level and wide-range analog interface board in increments of eight differential input channels per expander board.

In quantities of 1 to 9, the prices are broken down thus: the DT2772 sells for $225 for 32 SE or 16 DI channels and for $350 for 64 SE or 32 DI channels; the DT2774 with 64 SE or 32 DI channels is $350; and the DT2775 expander is $445 for 8 isolated DI channels. Delivery takes five days upon receipt of order.

Data Translation Inc., 4 Strathmore Rd., Natick, Mass. 01760. [385]

## Digital-to-synchro unit has ±0.05% transformation ratio

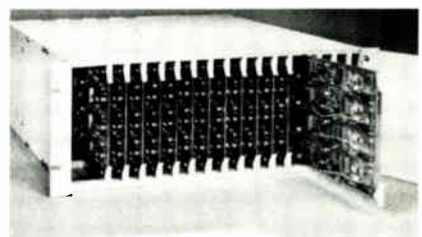
With an accuracy of to within ±4 minutes, the DSC5116 digital-to-synchro converter is pin-programmable for either 16- or 14-bit resolution with a ±0.05% transformation ratio. The device eliminates the need for a +5-V power supply and is useful for such applications as plan position indicators and radar display systems, for testing other synchro converters, and for optical alignment. With an output of 2 VA, it can directly drive control transformer loads from a power supply of ±15 V. Its output is compatible with any three-wire synchro or four-wire resolver. The reference input can be either 26 V root mean square or 115 V rms at 60 or 400 Hz. Pricing starts at $495 for orders of up to nine units. Delivery is from stock to 10 weeks.

Natel Engineering Inc., 8954 Mason Ave., Canoga Park, Calif. 91306. [384]

## Plug-in card has four independent amplifiers

Selling for less than $125 per channel, the model 540 is a single plug-in card that incorporates four independent direct-coupled differential amplifiers with optional strain-gage signal conditioning. It is designed as the front end in data-logging or data-acquisition and other systems where signal conditioning is required.

Common-mode rejection is 110 dB from dc to 60 Hz with 350-Ω unbalance; the operating common-mode voltage is ±10 V including signal,



and overload is ±50 V continuous without damage. The full power bandwidth is dc to 20 kHz, and the frequency response is dc to 80 kHz ± 3 dB. Delivery takes 60 days.

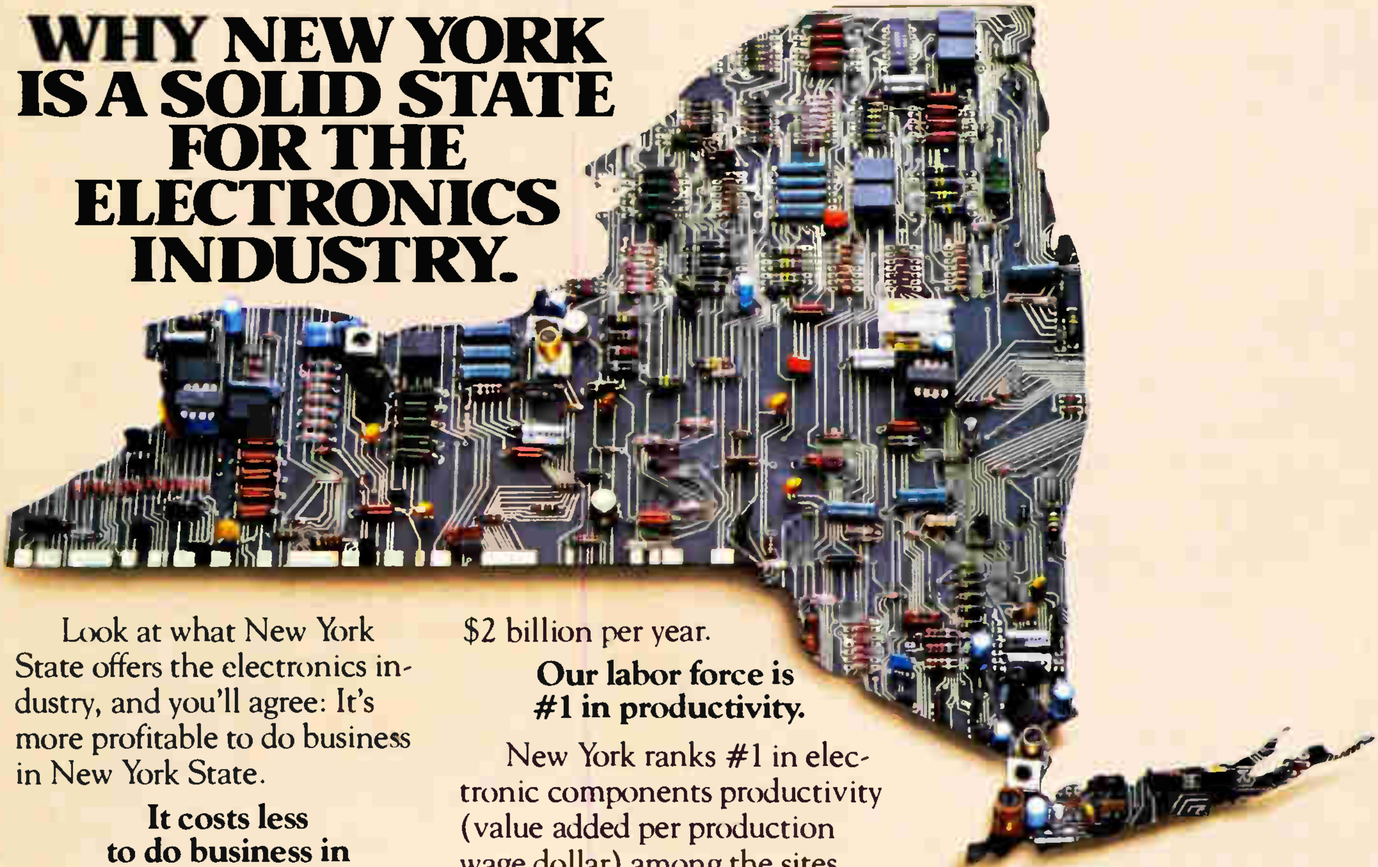
Ectron Corp., 8159 Engineer Rd., San Diego, Calif. 92111. Phone (714) 278-0600 [386]

## 12-bit d-a converter is fully compensated

The D/A 4000 is a 12-bit thin-film digital-to-analog converter that is fully compensated. Operating over the temperature range of −55° to +85°C and compatible with emitter-coupled logic, the device settles in 40 ns to within 1%. It contains an R-2R ladder network that is laser-trimmed to ensure optimum performance. The hybrid unit is housed with its own internal reference in a 24-pin hermetic dual in-line package. It can be screened to MIL-STD-883/B. In quantities of 1 to 49, it sells for $215. Delivery time is two weeks.

HyComp Inc., 146 Main St., Box 250, Maynard, Mass. 01754. Phone (617) 897-4578 [387]

# WHY NEW YORK IS A SOLID STATE FOR THE ELECTRONICS INDUSTRY.



Look at what New York State offers the electronics industry, and you'll agree: It's more profitable to do business in New York State.

**It costs less to do business in New York State sites than in San Jose, California. And we can prove it.**

An independent study analyzed the four critical costs of taxes, wages, power and construction for a model new electronics firm. It showed that New York State offers sites where these costs are less than they are for choice electronics industry sites around the country.

For example, these costs would total $7.6 million annually in San Jose, versus only $6.4 million in, say, Brookhaven, New York.

**New York has the best business advantages in America.**

Our costs are lower because we have the best tax incentives and credits. We have on-the-job training and job incentive programs. Long-term, low-cost financing. And, we've cut personal and business taxes by $2 billion per year.

**Our labor force is #1 in productivity.**

New York ranks #1 in electronic components productivity (value added per production wage dollar) among the sites analyzed. And in the past five years, New York's number of idle man-days due to work stoppages was half that of the national average.

**We graduate more electronics engineers than any other state.**

Thanks to universities like RPI and Cornell – and dozens of other fine colleges – more electronics engineers are graduated each year in New York State than any other state including California or Massachusetts. And since many of the largest electronics firms are already doing business here – GE, IBM, to name only a couple – our graduates are quickly turned into seasoned professionals.

**When you look into New York, you'll love New York.**

We have an abundance of electric power. Lots of affordable housing for your employees. And our 30 million acres include thousands of available plant sites. Not to mention some of the most magnificent outdoors and year-round recreation on the American continent.

Tell me more about why New York is a solid state for business. I am particularly interested in information on:

- ☐ Electronic Components
- ☐ Small Computers
- ☐ Semiconductors

William D. Hassett, Jr.
Commissioner of Commerce
New York State Dept. of Commerce
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**NEW YORK STATE.**
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Circle 212 on reader service card

# BECKMAN Announces Large Area LCD's For All Reasons

## Thanks To The World's Largest Watchmakers.

So, what do Liquid Crystal watch displays have to do with other applications? Everything! Yes, for small instruments, clocks, appliances, even point-of-sale equipment. Here's why:

Early on, Beckman developed superior LCD's . . . because of an already extensive knowledge of materials. This helped win contracts with the World's largest watchmakers. So, when the

market opened for large-area LCD's, Beckman was there waiting . . . with the know-how, the resources, and the experience of performing for the best!

Today, Model 737 is aimed squarely at the clock market, while Models 741-3 and 741-4 are primarily for small instruments. The many versions of Model 739 can be used for either. More importantly, these latter types were joined recently by Models 740-56 and 742-58, six and eight digit displays, respectively. The result: At least one large-area LCD for every application.

Meanwhile, there exists a huge custom capability . . . that can build an LCD for your application — just the way you want it.

All because Beckman got a head start in the watch business.


That experience also provided the know-how to maintain quality while reducing costs. And, it helped to develop these other advantages for Beckman LCD's:

- Low power consumption. CMOS compatible.
- Excellent contrast ratios; won't wash out, even in direct sunlight.
- Fewer drive components required.
- Choice of designs for night viewing.
- Long life expectancy.
- Fast (100 mS) Total Response time.

One clock manufacturer was so impressed that he wrote:

"Beckman LCD's are the best on the market. In a side-by-side comparison, any knowledgeable user would choose Beckman every time. The contrast ratio is better. Viewing angle (at 3V rms or above) is almost double that of the others. Switching time is almost instantaneous. And, besides, Beckman is a company you can rely on."

What more can we say, other than, "try Beckman large area LCD's . . . for whatever your reason — or, application!"

*For complete details, write:*
Display Systems Division,
Beckman Instruments, Inc.,
350 North Hayden Rd.,
Scottsdale, AZ 85257.
Phone: (602) 947-8371.
TWX: 910-950-1293.
*In Europe, Write:*
Beckman Instruments (Belgium) S.A., 14, Avenue Hamoir,
1180 Bruxelles, Belgium.
Phone: (02) 275.44.30.
Telex: 23577.

**Beckman Displays. The Visible Edge.**

**BECKMAN**

Software

# Subroutines allow modular software

Library includes 20 subroutines written in DEC Fortran IV/RT-11

As data-acquisition hardware advances, conversion times fall and sampling rates increase. Unfortunately, though, the software often cannot keep pace, slowing data acquisition or cutting flexibility. For instance, the software guiding the mini- or micro-computer in a data-acquisition system can impose excessive overhead penalties on the host. Or the needed software may not even exist, forcing a user to spend valuable time writing applications and routines.

Users of Data Translation Inc.'s hardware can take heart, though; the firm has announced a new library of real-time subroutines in Digital Equipment Corp.'s Fortran IV/RT-11 for use with the LSI-11, -11/2, and -11/23. Optimized at the machine-language level, the routines are said to be as much as 78 times faster than equivalent DEC software.

In addition to data-acquisition operations, DTLIB, as the library is called, supports high-resolution point plotting on either a CRT display or point plotter; light-pen interactive graphics can be programmed, and there is also support for auxiliary-display functions such as pen-up and -down on plotters, as well as erase, store-through, and other storage-CRT functions.

A completion-routine capability enables DTLIB users to write Fortran-IV and Micro-11 subroutines. They can be activated asynchronously upon completion of events like filling a data buffer.

**Checks and reports.** Finally, an error reporter checks for programming errors and reports those in syntax and usage, speeding correct entry. The routines also incorporate flags to indicate attempts to operate data-acquisition or other interfacing gear in illegal modes; such attempts are flagged before loss of data or damage to equipment can occur.

DTLIB supports a wide variety of data-translation hardware, from analog input and input/output systems, real-time clocks, and point-plotter systems.

The library also supports up to four isolated, stand-alone analog-input systems for a total of 240 isolated input channels; Data Translation claims this feature is not available from DEC. Another unique feature is said to be DTLIB's direct-memory-access capability that allows it to work with very high-speed I/O peripherals.

DTLIB also operates with up to 124 kilowords of memory on the LSI-11/23, and up to 30 kilowords on the LSI-11 and -11/2. The same is true for DEC's extended instruction set/floating-point instruction set for these machines, as well as for the FPP-11 floating-point processor.

The DTLIB SP101 is available under license only, on a floppy diskette; the price is $795. Software updates will be provided for a year after purchase for the cost of the diskette alone. Delivery takes five days.

Data Translation Inc., 4 Strathmore Rd., Natick, Mass. 01760. Phone (617) 275-2846 [401]

## A list of mix-and-match choices for the user

DTLIB includes some 20 subroutines that users can mix and match to form their own data-acquisition, -processing, and -display programs. The subroutines—with calls—are:

- IDAS: single analog-to-digital conversion.
- RTS: real-time sampling of a-d conversion.
- SETR: setting of real-time clock rate and mode of operation.
- HIST: real-time sampling of histogram time data or memory locations.
- IDIR: reading of a digital input channel or memory location.
- IDOR: loading of a digital output channel or memory location.
- DRS: clock- or event-driven real-time sampling of digital input channels or memory locations.
- DINP: clock-driven digital input polling and event latency measurements.
- IDAC: loading or reading an analog output channel.
- CLRD: scaling display data.
- DIS: continuous data display.
- DXY: continuous display of X-Y data pairs.
- SDIS: stop real-time data display.
- FSH: display of data once.
- FXY: display of X-Y data pairs once.
- KBCD2B: conversion of 16-bit binary-coded decimal to INTEGER*2.
- KB2BCD: conversion of INTEGER*2 to BCD.
- LWAIT: waiting for event.
- INT16: conversion of REAL*4 to unsigned 16-bit integer.
- FLT16: conversion of unsigned 16-bit integer to REAL*4.

## CP/M benefits available in network configuration

CP/NET, an operating system for microcomputer networks, supports rapidly evolving network technology by allowing independent microcomputers access, via a network, to common facilities such as peripherals, programs, and data bases. It operates with CP/M and MP/M to support hundreds of CP/M-compatible products. CP/NET consists of one or more masters under which MP/M runs and one or more slaves under which CP/M or MP/M runs. It is network-independent; with simple modifications, a network may be constructed with any combination of shared memory, serial links, or parallel input/outputs with any protocol, such as X.25, Bisync or SDLC.

CP/NET will be licensed on a per-

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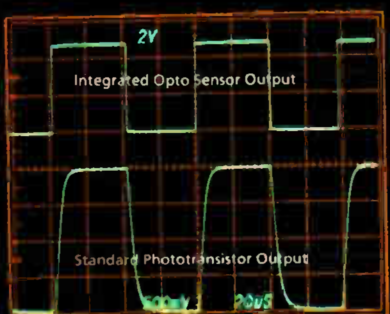
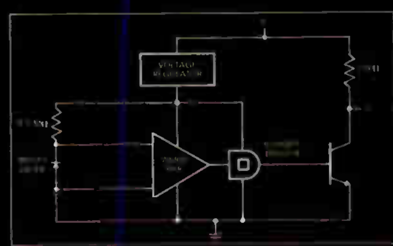
It's a logical breakthrough from Spectronics. We've designed the first opto detector IC offering compatability with TTL, CMOS and other standard logic families.




The SDP 8600 integrates a Schmitt trigger, voltage regulator, differential amplifier and photodiode onto the same substrate—replacing a complete PC board. This neat integration hasn't cost any performance. It has a propagation delay time of only 5 $\mu$s and a 50 ns rise and fall time.

Designed for use with an infrared LED, it's ideal for sensing applications such as computer peripherals, toys and automatic cruise control systems. With significant benefits like improved



noise immunity, higher reliability and better performance.

The 8600 is just one example of a long line of optoelectronic firsts from Spectronics.

So, if you're looking for better design solutions, call Spectronics. We do smart things with light.

For more information, contact a Spectronics distributor. Or call us at 214/234-4271. Address: Spectronics, 830 East Arapaho Road, Richardson, Texas 75081.

**Spectronics**
**A division of Honeywell**

**Light years ahead.**

Circle 215 on reader service card

Circle 216 on reader service card





master basis for about $200.

Digital Research, P. O. Box 579, Pacific Grove, Calif. 93950. Phone (408) 649-3896 [403]

## Data-encryption system does binary or character processing

A generalized software system for the encryption of data and programs is available for use on a wide variety of minicomputers and mainframes. Psypher takes input files (binary and/or ASCII-EBCDIC) and puts them through either binary processing that transforms the files into a completely unintelligible stream of random-bit patterns or through character processing that produces random-character streams. The encoded binary file has records of random length; the character file is fixed. The file to be encoded is not altered. Each copy distributed has its own unique algorithm, so no two copies of Psypher are alike.

The system requires approximately 8-K 16-bit words to run; run time varies from machine to machine. Psypher is now available in load-module form for operation on Data General, Digital, IBM, and CDC hardware. Prices range from $800 for minicomputers to $1,800 for mainframes.

MBS Consulting, 6407 Irwin Ct., Oakland, Calif. 94609. Phone (415) 658-4622 [404]

## Modular software upgrades Intel MDS hardware

P/B-MDS modular software is designed to upgrade the performance and utility of Intel's microprocessor development system. The software system includes a multiuser real-time operating system for 8- and 16-bit Intel microprocessors, a file management system, an interactive Basic interpreter, a Basic compiler, a text editor, and the ISIS operating system.

Panatec Inc., Dept. PB, 1527 Orangewood, Orange, Calif. 92668. Phone (714) 633-8961 [408]

Microcomputers & systems

# Unit develops wide bit-slice CPUs

## Development system has 80-bit logic trace, new examine command

True to its name, the Step-3 development system provides a step up in development system capabilities for designers using bit-slice processors or other designs employing programmable read-only memory as a microcontrol store. The Step-3, which competes with Advanced Micro Devices' system 29 development system, contains a number of improvements on the Step-2 system introduced in early 1978 and the logic trace feature of the Step-2 introduced a year ago [*Electronics*, Aug. 30, 1979, p. 226].

The logic trace of Step-3 is 80 bits wide, compared with the 32 channels available in the Step-2. Moreover, the use of logic analysis for system tracing is greatly aided by a new command—examine—in the Step-3's repertoire. The command recalls 16 to 20 coding registers to the cathode-ray-tube screen. These registers contain the user's architecture-dependent coding commands needed to implement the tracing function.

Two new control lines, one to indicate bus usage and the other to flag a last sample, have also been added to the logic analyzer's clocking circuitry. These allow the trace memory to be loaded only when the bus is valid, rather than recording one sample per system clock cycle.

**The force.** On the development system side, a new command—force—allows the designer, while the system is still in the monitoring mode, to create a new instruction that can last a programmable number of clock cycles. In the Step-2, the user could create such an instruction only by going to the editing mode, moving an instruction to location 0, creating the new instruction in its place, then reinserting the original instruction in its location later. Even then, the new instruction would last only for one clock cycle.

Another new feature of the Step-3 is its jam command, which lets the designer put new addresses into the instrument's writable control store. With this instruction, the system can ignore the address indicated by the program counter on the control store sequencer in order to force a direct jump to the specified address. Jamming, too, can be specified for a programmed number of clock cycles and is useful in creating pipelined architectures.

Like its predecessor, the Step-3 receives assembled code generated by Step's transportable meta-assembler (TMA), which is run on a host minicomputer or mainframe. The Step-3 appears to the system under development as a memory containing this microcontrol code. A macro-TMA is also offered that contains the original TMA with an added list of features. The new assembler can generate multiple-microword instructions, allowing a single mnemonic to generate several lines of code. It can also produce one-line macrostatements, which themselves can contain several multiple-microword mnemonics.

**Recursive call.** Other features of the macro-TMA include a recursive call capability that lets a subroutine call itself and single-bit parity on individual microwords. In addition, the Step-3 system has a number of self-testing capabilities, including an optional real-time access test, sum checking, a galloping test pattern (galpat), a partial galpat, a fast-port function test, and an abbreviated access-time test.

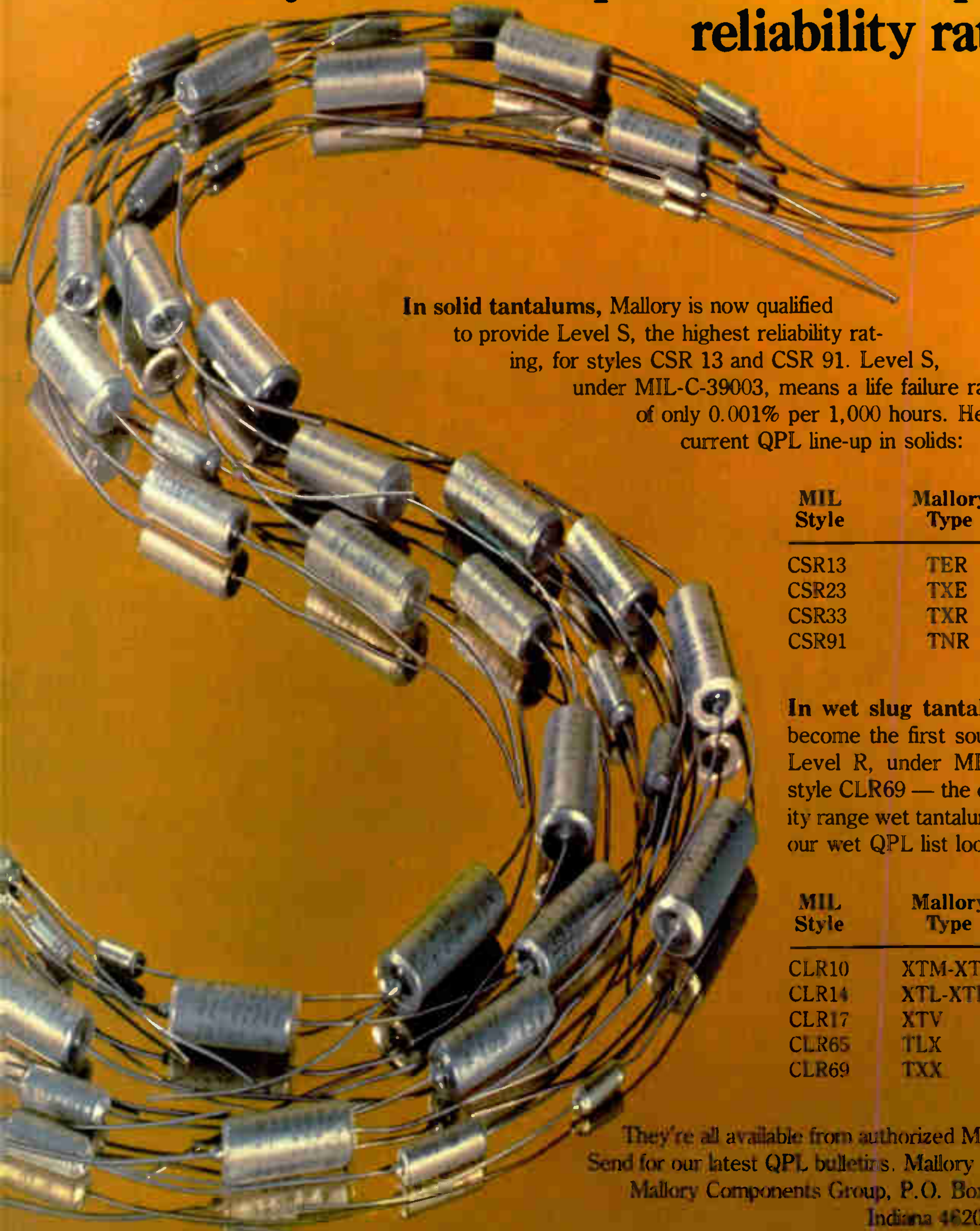
Pricing varies significantly according to memory size, the width of the trace chosen, and whether the real-time access test is included. A minimum configuration costs $8,450, and a maximum configuration with 96-bit-wide words is $36,650. Delivery is stock to 30 days.

Step Engineering Inc., Box 61166, Sunnyvale, Calif. 94088 [371]

## Interface links GPIB to S-100 microcomputers

A universal interface connects the general-purpose interface bus (GPIB) with all microprocessor systems that use the S-100 bus. The interface complies fully with the IEEE-488 standard and the proposed IEEE-696 (S-100) standard, says the manufacturer. Configured for either polled or interrupt-driven input/output functions, the model 1020A interface allows users of S-100–based systems to integrate multiple instruments and devices for data acquisition. The 1020 unit also permits such systems to perform auto-

# Mallory tantalum capacitors earn top MIL reliability ratings.



**In solid tantalums,** Mallory is now qualified to provide Level S, the highest reliability rating, for styles CSR 13 and CSR 91. Level S, under MIL-C-39003, means a life failure rate of only 0.001% per 1,000 hours. Here is our current QPL line-up in solids:

| MIL Style | Mallory Type | Life Failure Rates |
|---|---|---|
| CSR13 | TER | M, P, R, **S** |
| CSR23 | TXE | M, P, R |
| CSR33 | TXR | M, P |
| CSR91 | TNR | M, P, R, **S** |

**In wet slug tantalums,** we have become the first source qualified at Level R, under MIL-C-39006, for style CLR69 — the extended capacity range wet tantalum, which makes our wet QPL list look like this:

| MIL Style | Mallory Type | Life Failure Rates |
|---|---|---|
| CLR10 | XTM-XTK | L, M, P |
| CLR14 | XTL-XTH | L, M, P |
| CLR17 | XTV | L, M, P |
| CLR65 | TLX | L, M, P, **R** |
| CLR69 | TXX | L, M, P, **R** |

They're all available from authorized Mallory Distributors. Send for our latest QPL bulletins. Mallory Capacitor Division, Mallory Components Group, P.O. Box 372, Indianapolis, Indiana 46206. (317) 636-5353.

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ELECTRICAL/ELECTRONIC GROUP

EMHART

Circle 219 on reader service card

Another Able First

# Paydirt for VAX and PDP-11 users. One blue-chip card delivers 16 DZ lines per slot.

## Key Features

### 1 SELF TEST
(ON-BOARD LED DISPLAY)

**Self test feature is unique. No other DZ has it.**

**Executes** – at every power on.

**Identifies** – any malfunction and directs attention to the specific area of the DZ board affected. No lights, no problem.

**Controls** – fault isolation/repair by means of related options.

### 2 CONFIGURATION CONTROL
(ON-BOARD ADDRESS/VECTOR PENCIL SWITCHES)

**Complete configuration control – not matched by other DZ's.**

**Compatibility** – assured with all DEC address/vector/interrupt level disciplines.

**Easy Integration** – no etch-cuts, no jumpers.

**Priority Selection** – plug provided just like with DEC.

**Automatic Assignment** – one setting establishes base address & vector for both logical controllers.

### 3 STAGGERED LOOP-AROUND
(BUILT-IN MAINTENANCE AID)

**Another Able exclusive found only on the DZ/16**

**Complete Checking** – provides the only way to effect total parity/framing error check. Uses one UART to drive another for fault isolation. Alternative internal loop-around gives partial check only.

**Diagnostics** – support loop-around capability which is built-in to DZ/16 panel. Connectors are built-in. Guess where the other kind are anytime you need them.

Now you can add twice as many DZ lines to your PDP-11 in half the space and at a lower cost than ever before. Our new DZ/16 is a microprocessor-based controller which fits 16 asynchronous communications channels into a single board but sells for much less than the two-board DZ11-E it replaces. There's no waiting either. You'll probably have your card plugged in and running less than 30 days after we get your order.

The unique multiplexer installs in any standard hex-width slot and presents only one load to the Unibus. It supports all DZ11 baud rates, provides modem control on all lines and is compatible with DEC diagnostic and operating system software. The data format is program-selectable for each channel.

This isn't the first time we've been first. It won't be the last. The advantages we've sent your way again and again will keep coming. Get the most out of your VAX or PDP-11. Write today for details on our remarkable line of memory, communications and general-purpose cards for use in the PDP-11 family.

## Able, the computer experts

ABLE COMPUTER, 1751 Langley Avenue, Irvine, California 92714. (714) 979-7030. TWX 910-595-1729.

ABLE COMPUTER-EUROPE, 74/76 Northbrook Street, Newbury, Berkshire, England RG13 1AE. (0635) 32125. TELEX 848507 HJULPHG.

matic device testing and to be used in laboratory applications. The 1020 interface sells for $375, and delivery takes 30 days.

Dylon Corp., 3670 Ruffin Rd., San Diego, Calif. 92123. Phone (714) 292-5584 [373]

## Desktop computer has fixed and removable disks

A 64-K-byte table-top computer system's $16,500 price includes a 32-megabyte hard-disk drive with one removable and one fixed disk; its capacity can be expanded to 96 megabytes. The disks have an average access time of 30 ms and a maximum access time of 55 ms. The SD-700 can be configured as a single- or multiuser system. The latter can support up to 5 users with an expanded 256-K bytes of semiconductor memory partitioned into 48-K bytes per user (the operating system occupies 16-K bytes). The SD-700 includes two Z80 microprocessors and two input/output ports. Delivery takes 30 days.

SD Systems, P.O. Box 28810, Dallas, Texas 75228. Phone (214) 271-4667 [375]

## Tiny $2,600 computer makes dumb terminals smart

Selling for less than $2,600, the Smarts Box is designed to make dumb terminals intelligent. Based on the LSI-11/2 processor, the 16-bit computer comes in a box measuring 5½ by 8 by 11¾ in. that includes all power supplies, cooling fans, interfaces, and memory necessary for stand-alone operation. The Smarts Box comes with two independent RS-232-C interfaces, 8-K bytes of random-access memory that can be expanded to 32-K bytes, space for 8-K bytes of read-only memory, a quartz-crystal clock with a 60-Hz output, and two vacant Q-bus-compatible card slots. Delivery time is three weeks for evaluation units and six weeks when ordered in quantity.

North Atlantic Industries Inc., 60 Plant Ave., Hauppauge, N. Y. 11787 [376]

# TRANSISTOR SOCKETS

## NEWLY DESIGNED
# SNAP-IN SOCKETS
## FOR TO-3 & TO-66

*The most complete line of transistor sockets and mica insulators in the industry. Our sockets are designed for the TO-3 and TO-66 transistors. Available from stock. Introducing our latest design in printed circuit sockets plus an extensive line of snap-in sockets. Sockets are available in the latest UL approved materials.*

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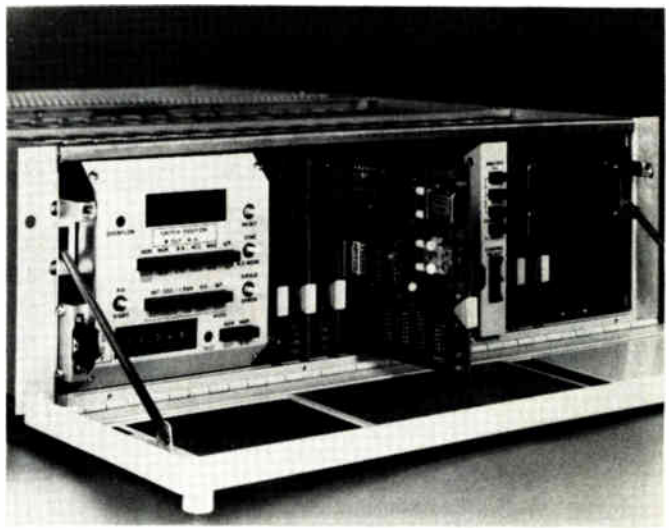


# A 1 TO 10 CHANNEL MODEM THAT TAKES ITS OWN PULSE AND RUNS AT UP TO 5,000,000 BITS PER SECOND.

Use this unique unit as a self-standing modem on wideband telephone and signal circuits. It provides encode/decode capability between analog and digital information in M², Miller or Biphase-L codes, at rates as high as 5 mega-bits/second.

The Ampex M² Digital Encode/Decode Unit is available in channel capacities from 1 to 10, and offers a built-in test option that functions as an error counter with a digital readout. It displays number of errors in either $10^6$ or $10^8$ bits, and can be used by itself as a frequency counter.

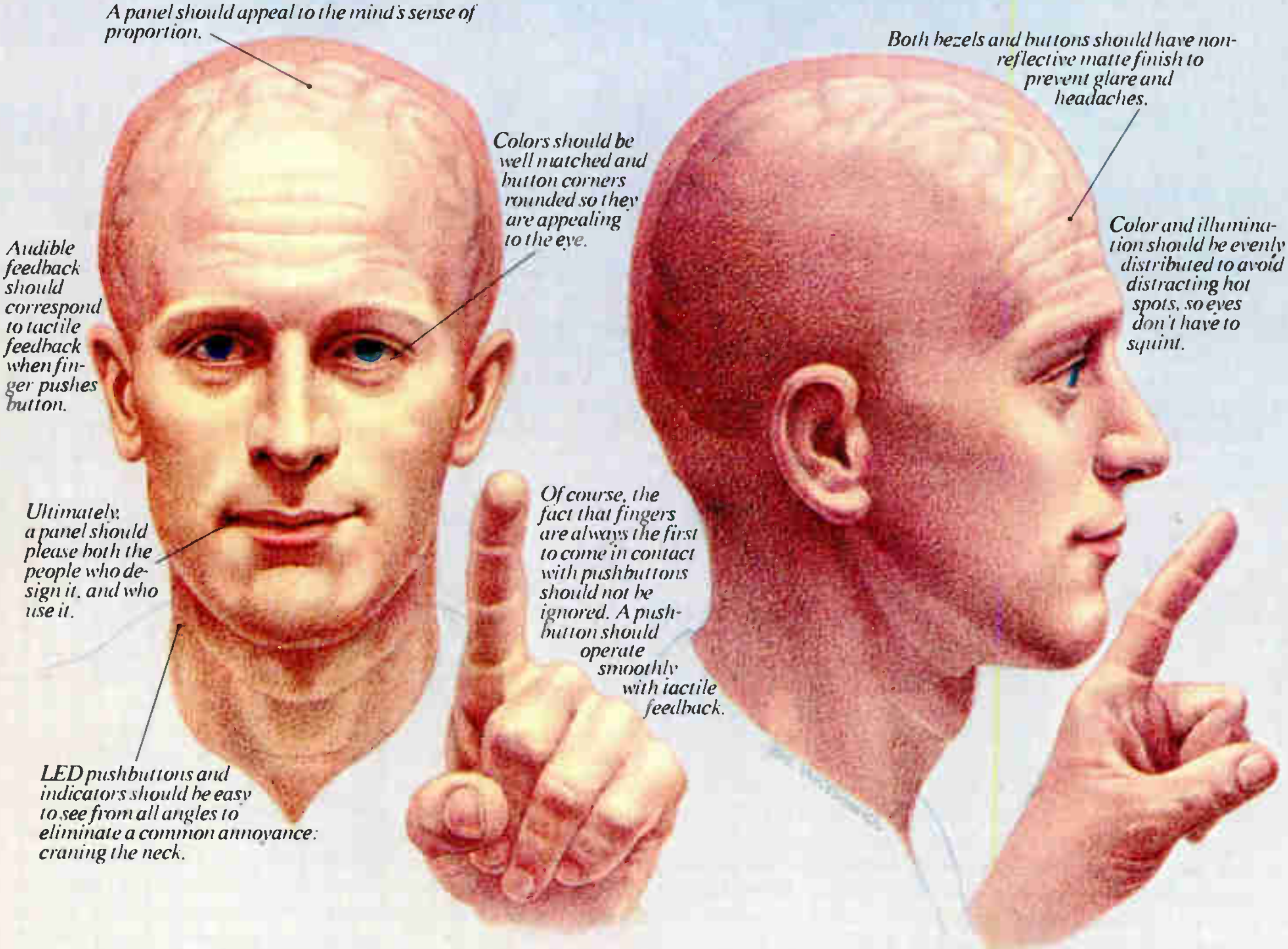
Much more than a modem, this unit can also be used as a front end with an analog instrumentation recorder, providing instant digital data recording capability.

The compact package measures only 5¼ inches high by 19 inches wide, and the power supply is 115/220V, 47 to 400 Hz. Price ranges from about $6000 to $12,000, depending upon channel count and installed options.

Rene Chikhani can provide complete technical and performance specifications, and he'll work with you on custom system applications. Call Rene at 415-367-2758, or write to him at Ampex Data Systems, 401 Broadway, Redwood City, California 94063.

**AMPEX**

# A pushbutton panel should be designed for parts of the body besides fingers.




When we designed the Advanced Manual Line (AML), we included everything a designer could want.

Like a broad selection of pushbuttons, indicators, paddles and rockers. In a variety of shapes, sizes and colors. With LED, incandescent or neon illumination.

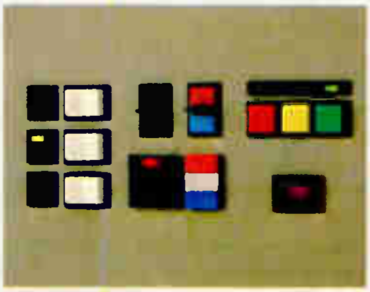
But what really makes AML unique is a small detail that others seem to have overlooked.

The people who use them. Which is why they're not only appealing to fingers, but other parts of the body as well.

That isn't to say we've neglected the person who puts the panel together. Because AML has single level termination for easy wiring and low installation cost. And electrical flexibility that ranges from solid state to electronic and power duty control.

With AML, you clearly design panels around people who use them, and not just their fingers.

For details, and the location of our sales offices and distributors around the world, write MICRO SWITCH, Freeport, Illinois 61032. Or call 815-235-6600.



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a Honeywell Division

Circle 225 FOR DATA

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# Battery puts out 5-kW peak power

## 12-V, 55-Ah uninterruptible supply yields 200 cycles of full-depth discharges

In designing its 12-V, 55-Ah Gel/Cell lead-acid battery, the Globe Battery division of Johnson Controls kept in mind that a battery supplying uninterruptible power to a computer must be able to sustain short-term discharges of very high currents. Although some wet-cell batteries can do this, they are often limited in life to one or two years. Globe's new sealed battery, which uses a gelled electrolyte, not only has 5,000 W of available peak power, but its cycle life, says Richard J. Scarvaci, application engineer at Globe, is in excess of 200 cycles of full-depth discharges. Used as a standby supply, the battery lasts between four and six years.

"When the Globe Gel/Cell was introduced over 15 years ago, its design incorporated a lead-calcium grid alloy to give the battery a very low self-discharge rate and to significantly reduce water loss," Scarvaci says. The new battery is sealed, and all cells are connected through the partitions of its case by welding opposing cell connections. "This results in a very short interconnection path," he adds, "reducing the internal resistance and increasing the battery's mechanical strength."

**Heat-sealed mating.** The new battery uses a polypropylene container, which lets all mating container surfaces be heat-sealed. Also, the use of polypropylene makes possible thin cell partitions, increasing the useful internal volume and thus the power density—up to 830 A of current-carrying capacity calculated at half the voltage.

The battery comes in a standby-power version and one for frequent discharges. Since the rechargeable battery is made with a gelled electrolyte, it can of course be used in any position—an advantage over wet-cell batteries, which must be upright. In production quantities, the 10-by-7-by-9-in. battery sells for approximately $50. It will be on display at Wescon.

Johnson Controls Inc., Globe Battery division, 5757 N. Greenbay Ave., Milwaukee, Wis. 53209. Phone (414) 228-1200 [361]

## Dc-to-dc converters come in dual in-line packages

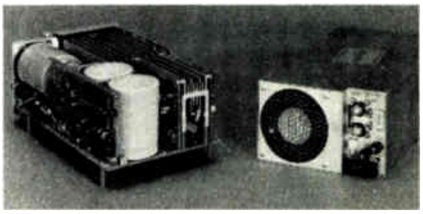
The 500 series of dc-to-dc converters for both analog and digital applications comes in a 24-pin integrated-circuit package that allows each converter to be mounted directly on a printed-circuit board. The series provides a variety of isolated outputs from either 5- or 12-V inputs. Input to output isolation is 300 V dc minimum with an impedance of 10 MΩ. The 10 models in the series have both single-polarity outputs (5 V at 100 mA, 12 V at 80 mA, and 15 V at 65 mA) and dual outputs (±12 V at 80 mA and ±15 V at 65 mA). The temperature coefficient is ±0.015%/°C over the full operating range of −25° to +70°C. The single-output models sell for $29, and the dual-output units sell for $34. Delivery is from stock.

Power General, 152 Will Drive, Canton, Mass. 02021. Phone (617) 828-6216 [363]

## 1,500-W switcher comes in 750-, 1,000-W-sized package

A 1,500-W switching power supply made by Boschert comes in the 5-by-8-in. package that is the industry standard for 750- and 1,000-W supplies. Thus, the model HL 1500 can replace lower-power units in computers, test systems, and industrial controls, allowing the systems to be upgraded to levels that require more power without having to change the system housing to fit a larger-sized power supply.

The first model in the series is a



+5-V, 300-A unit. Power density is 2.5 W/in.$^3$ at the nominal 5.0 V and over 2.8 W/in.$^3$ at 5.75 V. Its efficiency is 82% at full load. The supply controls output voltage to within 1% during a 25% change in load and recovers to a flat output in 0.5 ms. Typical line regulation is 0.2% and load regulation is 0.3%. Line-power interruptions are masked by a 30-ms holdup. Brownout tolerance is wide: the ac-line power can vary from 167 to 250 V. The 5-V, 300-A unit is available within 60 days. U. S. prices are $1,220 for a single unit and $960 apiece in quantities of 100.

Boschert Inc. 384 Santa Trinita Ave., Sunnyvale Calif. 94086. Phone (408) 732-2440 [366]

## Lab supplies offer dual or triple outputs

A range of compact laboratory power supplies manufactured by Sweden's Power Box AB that offer either dual or triple outputs are being marketed in the U. S. The supplies come in two series: the PB-3000 series, which offers three independent and floating output voltages, and the PB-2000 series which offers two. Both series are designed for inputs of 110 or 230 V ac, at 47 to 60 Hz. The dual or triple outputs are at 4 to 6 V, 11 to 16 V, 0 to 20 V, or 0 to 40 V in various combinations. The outputs—which can be connected in series and parallel or can float from ground—have 500-V isolation, with 2,500 V to chassis. The units are insensitive to radio-transmitter and other radio-frequency interference. Leakage current is less than 10 μA. Prices range from $495 to $845, depending on specifications.

Norman R. Sutherland & Associates Inc., 6290 Sunset Blvd., Suite 1126, Los Angeles, Calif. 90028. Phone (213) 463-5090 [365]

# New iSBX™ Multimodule™ boards

## Intel® introduces a whole new dimension in configuring single board computer systems.

Intel pioneered the concept of flexible microcomputer *system* design in 1976, with our family of iSBC™ single-board computers interfaced via the Multibus™ system bus—presently accepted as the industry standard.

Now we've extended this well-accepted concept to *board*-level design: A new generation of Multimodule boards interface to iSBCs via the new iSBX bus. So now you have a second design option. You can expand systems in large increments with Multibus boards. Or in smaller, more economical increments with Multimodules.

### The key to configuration flexibility

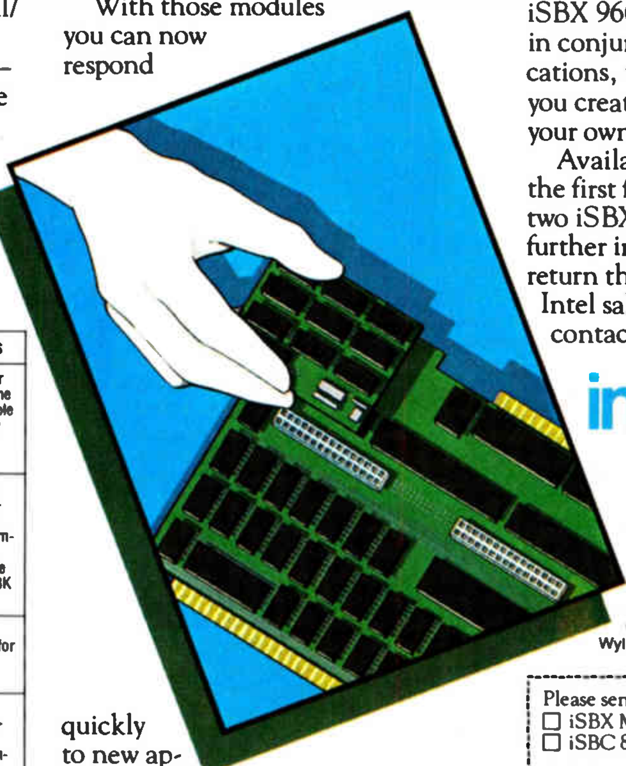
The iSBX bus—the first physical/electrical interface for direct on-board expansion of iSBC systems—assures compatibility between these systems and the emerging Multimodule product line.

Present on all future Intel single-board computers, the iSBX bus saves design time and space, and facilitates fast, easy upgrading. System performance is also improved because Multimodules tie directly to the iSBC internal bus. Connection to the iSBX bus is made with a set of rugged connectors—one on the iSBC board, the other on the Multimodule itself.

### The new Multimodule family

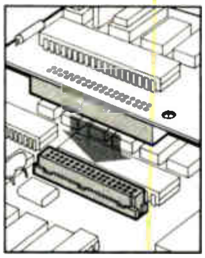
Multimodules represent a whole new family of plug-in expansion boards. They allow you to add a variety of special performance features to your existing iSBC system. Currently available add-ons are shown below. Soon you'll also be able to add other Multimodules for D-to-A and A-to-D conversion, communications, peripheral interfaces—and more.

With those modules you can now respond



quickly to new applications opportunities. Examples? Take data acquisition or industrial control: to add extensive I/O processing power, you simply plug in the iSBX 350 board. Or consider communications networks. Now there's no need to add entire USART boards; just use the iSBX 351 unit. In laboratory control applications, instead of an independent math processor, now you can choose the more economical iSBX 331 or 332 math modules.

### New Multimodule-compatible iSBC boards



iSBX 960-5 Connector

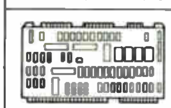
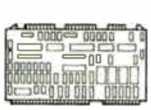
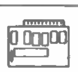
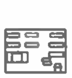
Intel's new 8-bit iSBC 80/10B and 80/24 single-board computers are the first of many iSBCs to offer iSBX Multimodule expansion capabilities. Both are improved versions of widely used iSBC boards. (See table).

### Custom tailoring, too

For users who want to design their own Multimodule boards, Intel offers iSBX 960-5 connectors. When used in conjunction with the iSBX specifications, this set of connectors lets you create modular boards that meet your own unique requirements.

Available from Intel today are the first four iSBX Multimodules and two iSBX-compatible iSBCs. For further information, or to order, return this coupon or call your local Intel sales office or distributor. Or contact Intel at the address below.

**New Multimodules and iSBX Bus-compatible iSBCs**

| | |
|---|---|
|  | **iSBC 80/10B Single Board Computer** 8080A-based microcomputer with one iSBX bus connector; 48 programmable I/O lines; one USART; timer; capacity for 1K-4K bytes RAM; up to 16K EPROM |
|  | **iSBC 80/24 Single Board Computer** 8085A-2 based microcomputer operating at 4.8 MHz (2.4 MHz optional); two iSBX bus connectors; 48 programmable I/O lines; one USART; three programmable timers; programmable interrupt controller; capacity for 4K-8K bytes RAM; up to 16K EPROM |
|  | **iSBX 350 Parallel I/O Multimodule** 24 programmable I/O lines; sockets for inverting and noninverting transceivers |
|  | **iSBX 351 Serial I/O Multimodule** Programmable synchronous/asynchronous communications channel; standard RS232C or RS449/422 compatibility; software-selectable baud-rate generation; two programmable 16-bit BCD or binary timers/event counters |
|  | **iSBX 331 Fixed/Floating Point Math Multimodule** Fixed point single- (16-bit) and double- (32-bit) precision arithmetic; floating point single- (32-bit) precision functions; floating-to-fixed and fixed-to-floating point conversions; transcendental functions |
|  | **iSBX 332 Floating Point Math Multimodule** Single- (32-bit) and double- (64-bit) precision arithmetic; compatible with proposed IEEE format and existing Intel floating point standard. |

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Please send information on:
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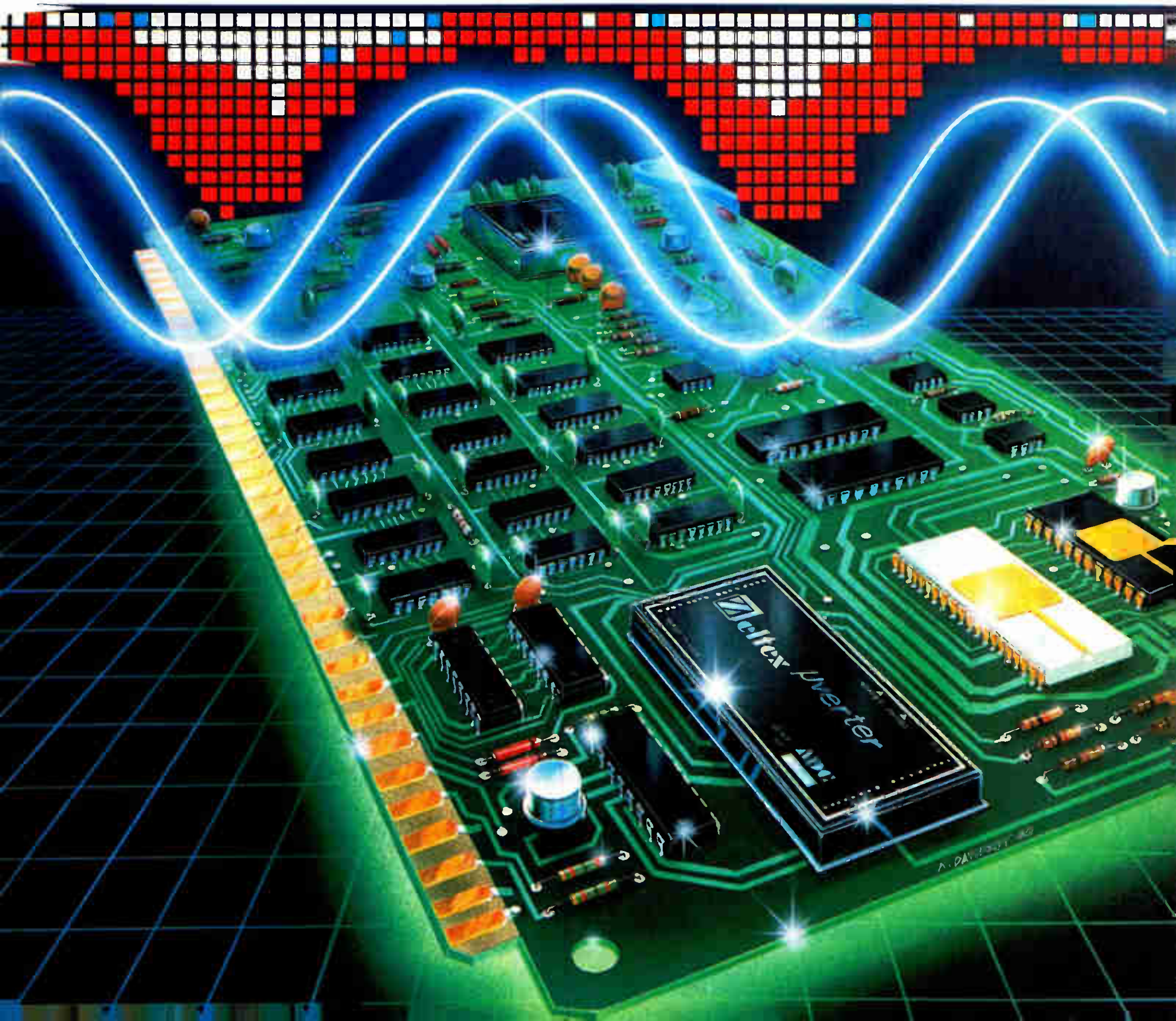


# Products Newsletter

**Philips to unveil 4-channel, 100-MHz scope at Wescon**

Look for Philips Test and Measuring Instruments Inc. of Mahwah, N. J., to introduce a 100-MHz, four-channel oscilloscope—the model 3264—at next week's Wescon. According to product manager Hans Toorens, **the $4,995 scope's four channels make it "sort of an analog logic analyzer," with real-time, rather than clock-pulse, glitch display.** A 17-kV accelerating potential ensures bright display, and triggering and delay can be independently set by any channel or an external source.

**Winchester drive has 675-megabyte memory capacity**

The Computer Systems division of the Harris Corp. is about to introduce a 675-megabyte 14-in. Winchester disk drive, **said to have the largest capacity of any such drive offered so far.** The Fort Lauderdale, Fla., division's drive will feature an average seek time of 25 ms, an average latency time of 8.3 ms, and a data-transfer rate of 1,209 kilobytes/s. The model 5660/5661 is optimized for use with Harris computers and includes a controller capable of managing seven added stores for a system capacity of 5.4 billion bytes of data. The drive is priced at $71,260, with deliveries starting in January.

**GE adds to market for programmable industrial controls**

Expecting the market for industrial programmable controllers to top $250 million in orders this year, General Electric Co. is introducing its Series Six family of controllers priced between $3,500 and $100,000. Based on a 16-bit bit-slice processor, the models 60, 600, and 6000 from GE's Industrial Control Department in Charlottesville, Va., will have **scanning times ranging from 8 to 40 ms, 2- to 32-K (16-bit) words of complementary-MOS read-only memory or programmable ROM, and 512 to 4,000 input/output lines.** The family can handle networking and remotely distributed I/O. Deliveries begin in March 1981.

**Floating-point library offered for 8080/8085, Z80**

Formerly a custom software house, Cogitronics Corp. of Portland, Ore., is breaking into the open market with the FPAC floating-point library for original-equipment manufacturers' microprocessor systems. The library includes floating-point **capabilities for four-function arithmetic operations, trigonometric functions, exponentiation, and logarithmic functions.** It costs $1,500 for a site license, which includes the right to distribute the library in machine-language form. The library is written in assembly-level source code and comes in two versions, one optimized for the 8080/8085, the other for the Z80.

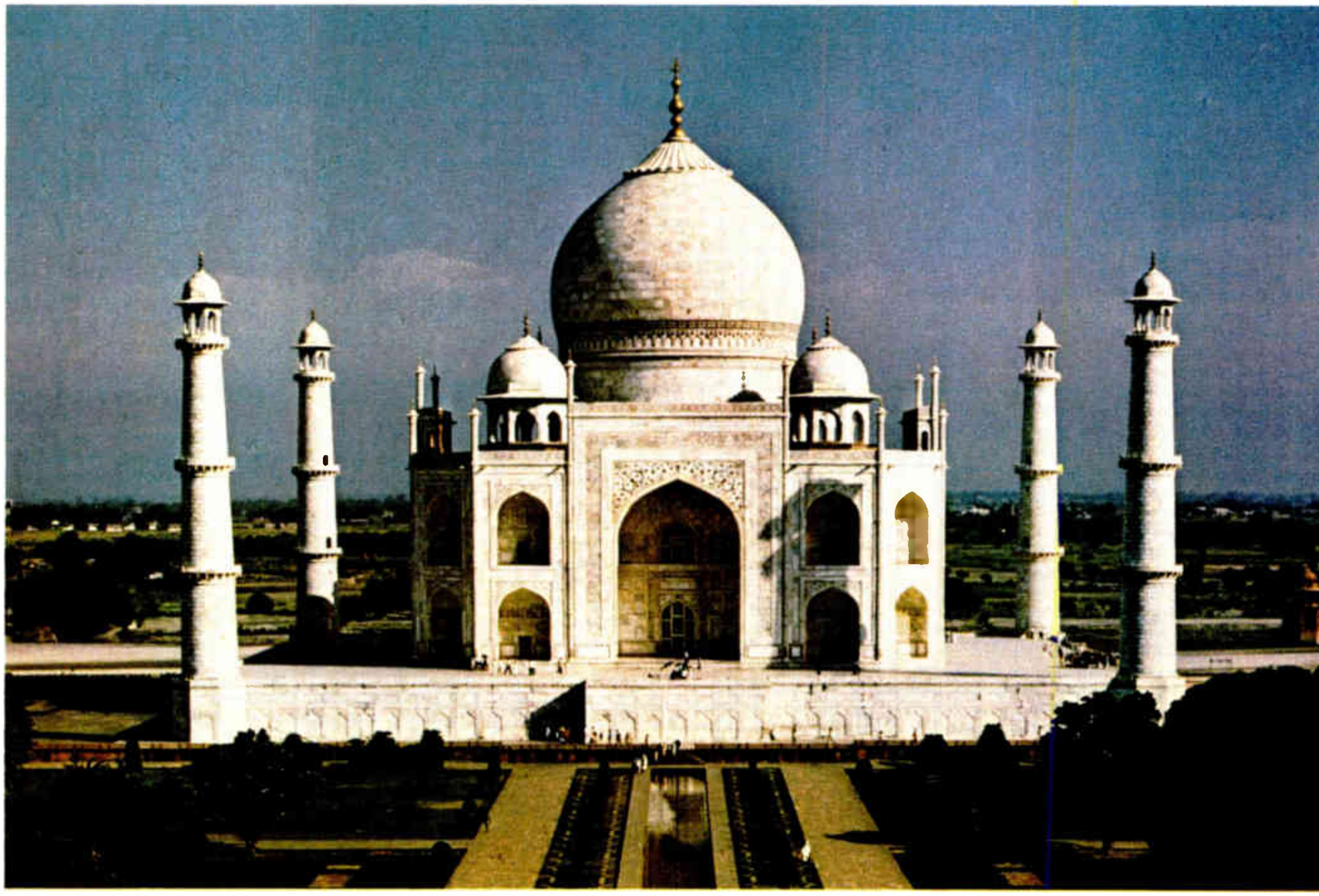
**Cipher doubles capacity of ½-in. magnetic tape**

A new version of the Microstreamer streaming tape drive from Cipher Data Products Inc., San Diego, Calif., doubles the capacity of ½-in. magnetic tape. The Microstreamer 2 can store up to 92 megabytes of unformatted data on a 10½-in. reel of tape at **a density of 3,200 bits/in. and can transfer at 160 kilobytes/s.** The higher density is optional at a new speed of 50 in./s. The drive will also operate at the standard 1,600 b/in. at 100 in./s in the streaming mode and at 25 in./s in the start and stop mode, making it compatible with two other types of drive. The new drive will be priced at $2,350 in large quantities, with evaluation units to be available in December and production shipments to begin in early 1981.

## New literature

**Measurement.** A 32-page application note from Hewlett-Packard, "Accurate and Automatic Noise Figure Measurements," explains how to assemble an automated system that will make accurate noise-figure measurements. The system described consists of a microwave source and mixer used as a tunable down-converter, along with an HP model 436A digital power meter, a 346B 10-megahertz-to-18-gigahertz-noise source, and off-the-shelf components. Demonstration software routines in application note 64-3 include techniques for measuring the noise figure and gain of microwave components. The free booklet includes block diagrams and program listings. Hewlett-Packard Co., Inquiries Manager, 1507 Page Mill Rd., Palo Alto, Calif. 94304 [421]


**Oscillators.** "Frequency control devices" is a 16-page technical catalog designed to provide both purchasing and engineering information on quartz crystals and clock oscillators. All the popular crystal cuts are shown, with the advantages and limitations of each listed. The section on clock oscillators covers the critical performance parameters, as well as offering complete technical information. In addition, the booklet includes an extensive discussion on equivalent circuit and oscillator theory. Northern Engineering Laboratories Inc., 357 Beloit St., Burlington, Wis. 53105 [422]



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4,000 North Americans work for Aramco in Saudi Arabia. They're helping the Kingdom develop energy resources that are being used all over the world.

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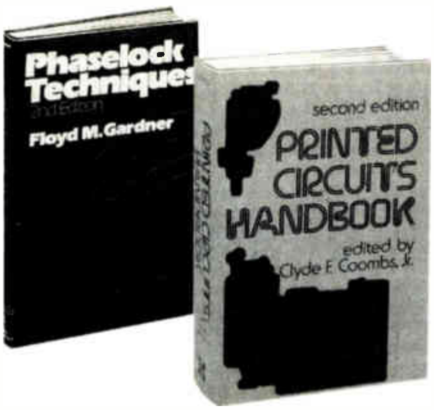


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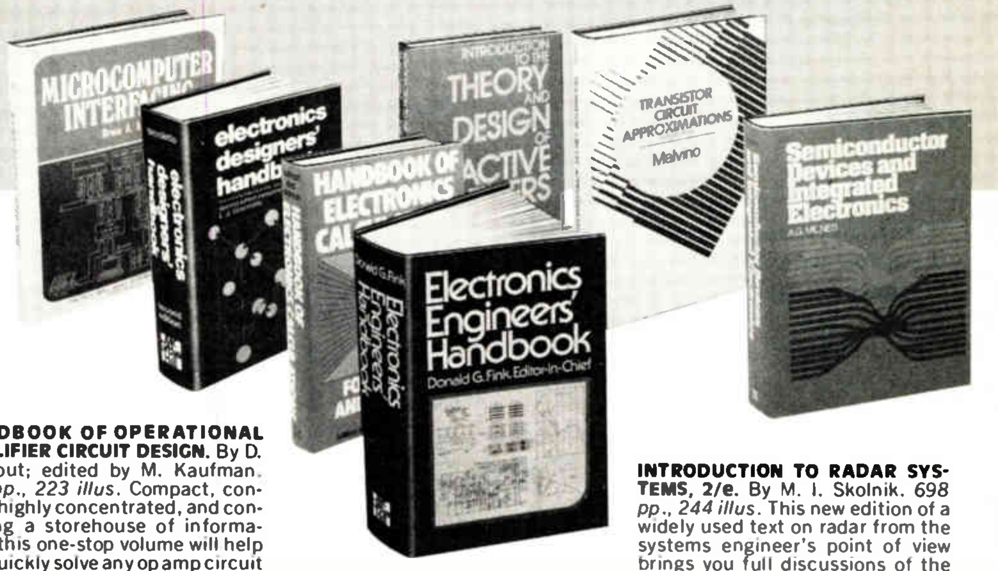


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# Career outlook

**GE faces age-bias charges**

■ Charges of discrimination against the older electrical engineer are once again rearing up as the recession spreads. At Appliance Park in Kentucky, just outside of Louisville, General Electric Co. has had to lay off some 400 salaried workers in the last nine months. Of those 400 workers, about 130 are electrical engineers, and many are over age 40.

"The lack of work seems to have a disparate impact on older workers," notes Richard Caslin, an attorney representing some of the laid-off workers and himself a former GE employee. At present, Caslin has three Federal court actions pending against GE and has filed more than 10 age-discrimination complaints with the Kentucky Commission on Human Rights.

"The Kentucky Commission and I are trying to get the Federal EEOC [Equal Employment Opportunity Commission] to file a systemic, or class action, charge against the company on a nationwide basis," notes Caslin. "We have reason to believe that age discrimination is a deep-seated company policy," he adds.

A spokesman for GE notes that the company "looks at all possibilities for work within GE first in Louisville, then outside Louisville in Texas, Milwaukee, Bloomington, and anywhere else the Appliance division has manufacturing facilities. If the search inside is unsuccessful, then we have an outplacement service."

**DOD fiber-optic papers.** The Electronic Industries Association is calling for technical papers in preparation for a program for a joint Department of Defense and industry fiber-optics standards conference to be held next March or April. The conference—for which North Atlantic Treaty Organization participation has been requested—is to identify military fiber-optic standardization issues. Noncommercial, unpublished technical papers are sought in the following areas: real applications involving systems or installations; individual components such as fibers, cables, interconnections, transducers; instrumentation for testing components in the laboratory; field-testing considerations; and standard procedures. Persons wishing to offer a paper for consideration should by Sept. 15 submit eight copies of a 300-word summary, complete with the author's name, address, and telephone number in the heading. Send them to Steve Forish, EIA Headquarters, 2001 Eye St., N. W., Washington, D. C. 20006. Notification of acceptance will be made by Nov. 1.

**Computer club affiliation.** In addition to offering full membership to vendors, consultants, manufacturers, and end users, the National Computer Association now offers membership to computer clubs. With this membership, each club will receive all NCA publications for an annual fee of $50 per year. The NCA is also establishing subgroups of 200 or more interested members along product and individual interest lines. Individual membership in the NCA is $35 per year. For more information write to Floyd L. Burton, Director, National Computer Association, 1485 E. Fremont Circle S., Littleton, Colo. 80122, or call (303) 797-3559.

**Troubleshooting microprocessors.** Participants in the "Hands-on Microprocessor Troubleshooting" course 142, offered by Integrated Computer Systems Inc., will learn programming fundamentals for troubleshooting; bus, processor, and input/output basics; and systematic procedures for isolating hardware and software faults as well as methods for designing testable microprocessor systems. The four-day course costs $795; it will be given in Anaheim, Calif., beginning on Sept. 23. Later this fall it will also be given in Washington, D. C., Boston, Houston, and other locations. For further information, write to Michael B. Sanson, Integrated Computer Systems Inc., 3304 Pico Blvd., Box 5339, Santa Monica, Calif. 90405, or phone him at (213) 450-2060.

**Private practice trends.** Looking at current trends in private practice, the National Society of Professional

## Career outlook

Engineers will hold a series of conferences starting in Denver, Oct. 3–4. "Engineering in Tea Leaves—A Look at the '80s," will identify trends that concern engineers who are assuming management positions in private practice. Some of the areas that will be covered are: anticipating a firm's financial needs; identifying the types of technical people who will be needed; the staffing costs of a computer or word-processing installation; and the procurement trends and professional liability of engineers. Jean Robertson at the NSPE information center has more information; her address is 2029 K St., N. W., Washington, D. C., 20006, or call (202) 331-7020.

**Pocket-sized computer.** A Radio Shack hand-held computer has a 24-character liquid-crystal display with English language prompting and includes a 1.9-kilobyte random-access memory that retains information for the 300-hour life of the internal batteries. Ideal for those engineers who wish to carry computing power with them, the TRS-80 pocket computer weighs 6 ounces and is less than 7 inches long. It can be programmed in Basic, and preprogrammed tapes for real estate, civil engineering, personal finances, aviation, math drill, and a games pack are also available. These tapes may be loaded into the unit with an optional cassette interface. The TRS-80 may also be used as a powerful calculator with up to 15 levels of parentheses. The computer is priced at $249.95, with the optional


cassette interface priced at $49.00. A printer will also be available soon. Tandy Corp./Radio Shack, 1800 One Tandy Center, Fort Worth, Texas 76102.

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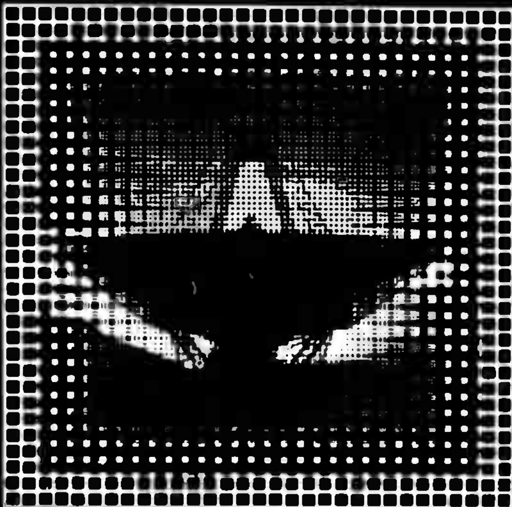

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(Ref: 80/58)

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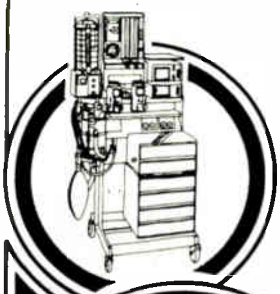

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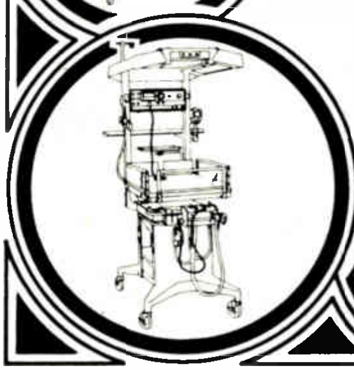

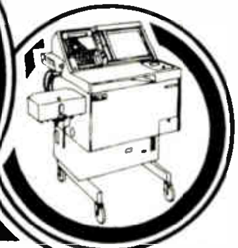

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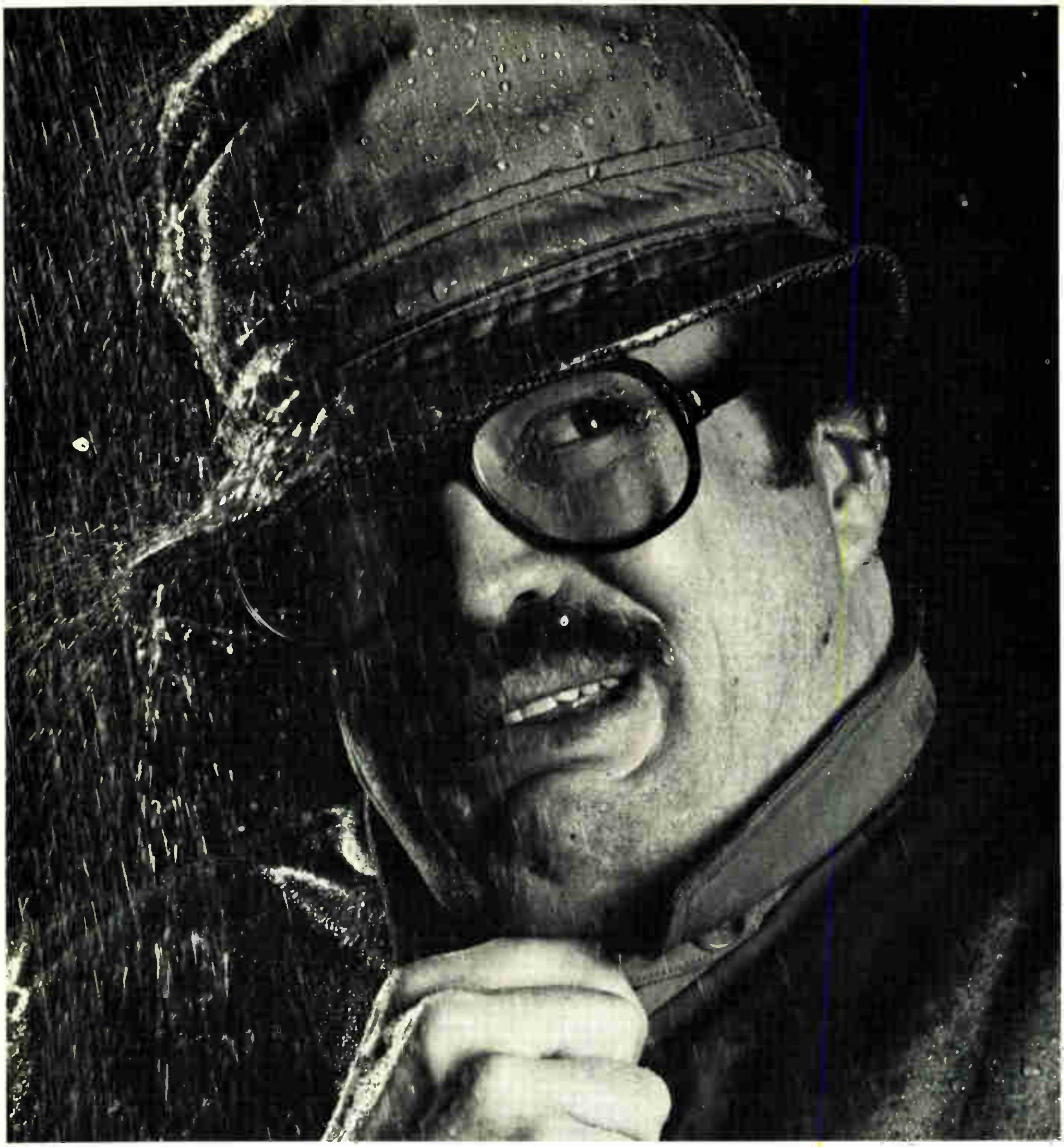

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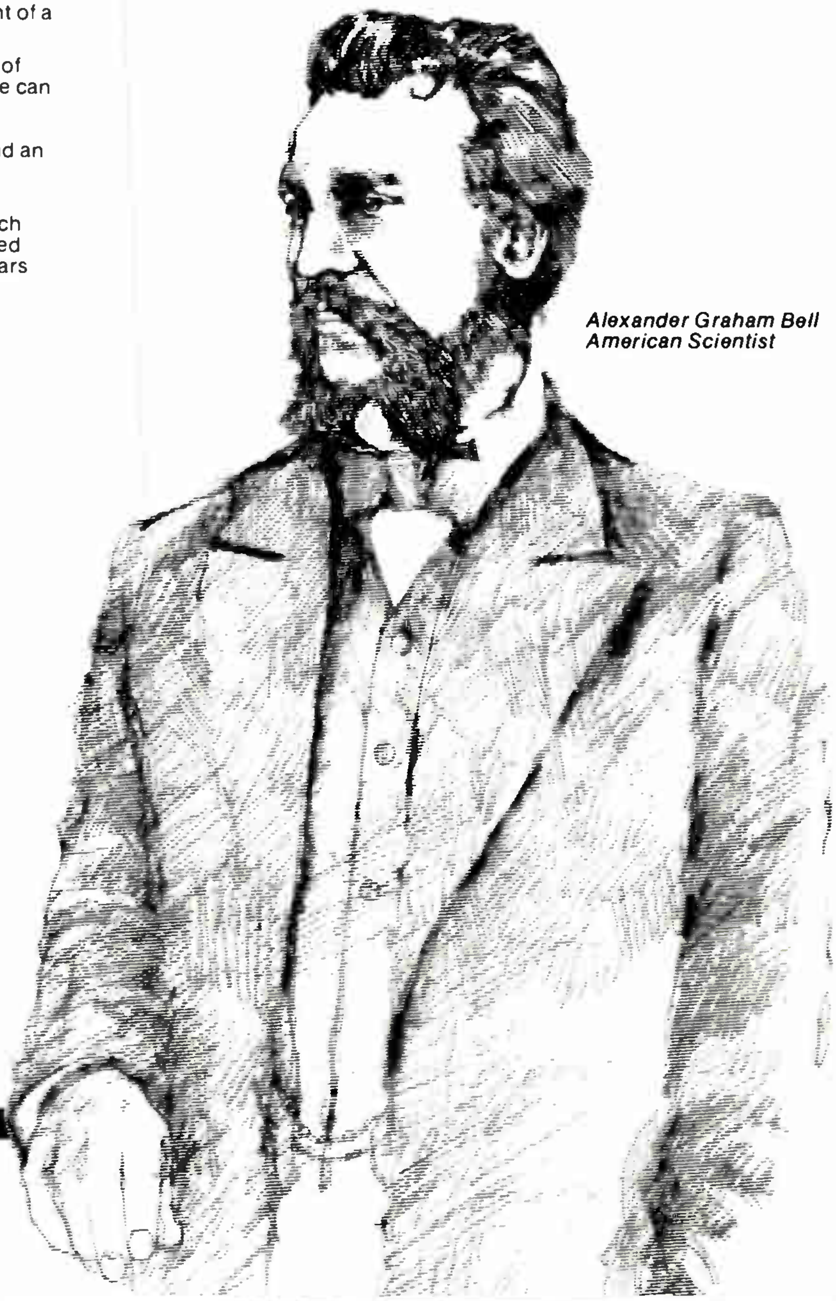

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