JULY 31, 1980

RESEARCHERS TACKLE MEASUREMENT OF HIGH-SPEED SIGNALS/86

Heat pumps cool circuit packages electronically/109

Electrically erasable PROM mates with C-MOS systems/89

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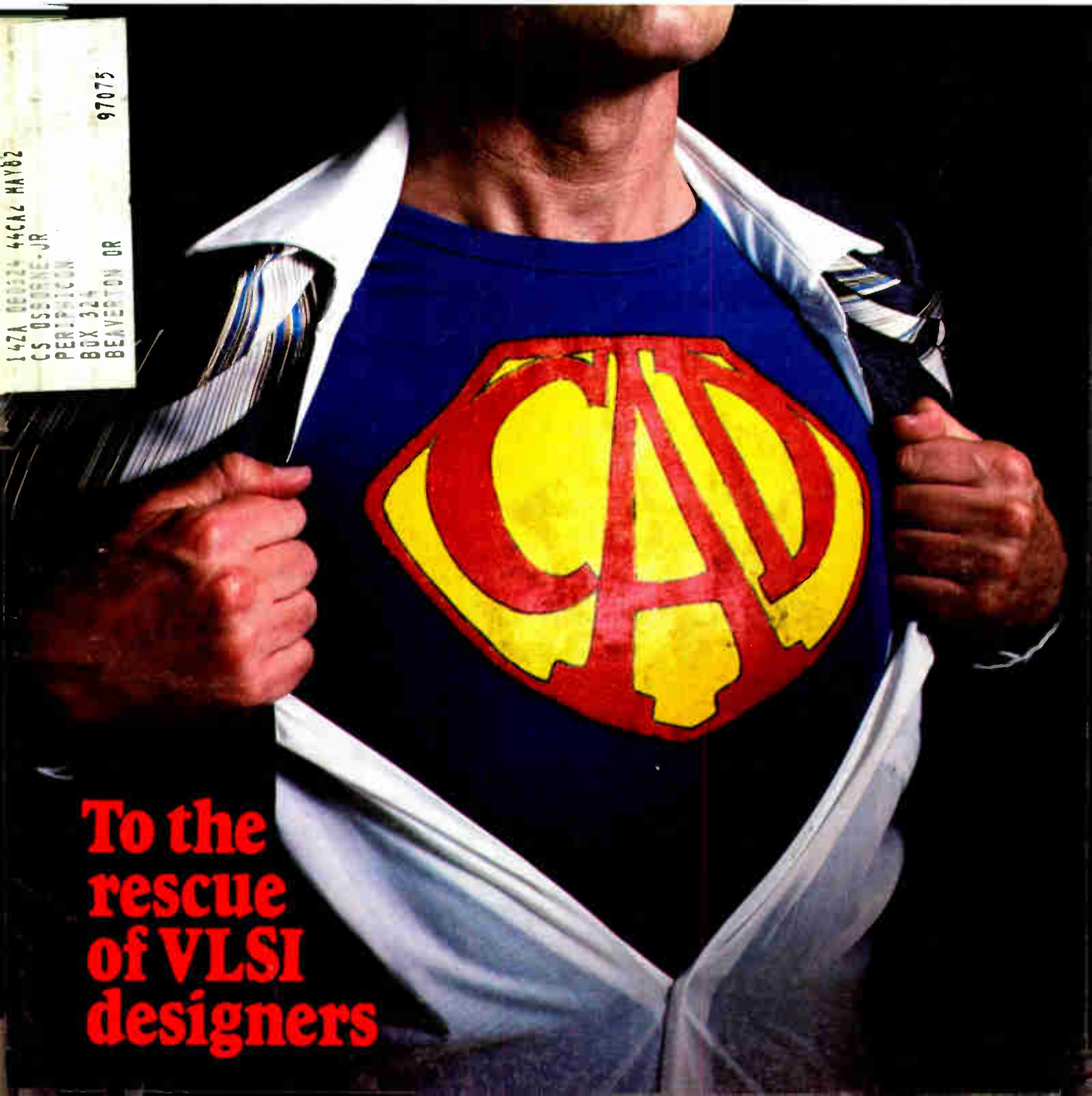

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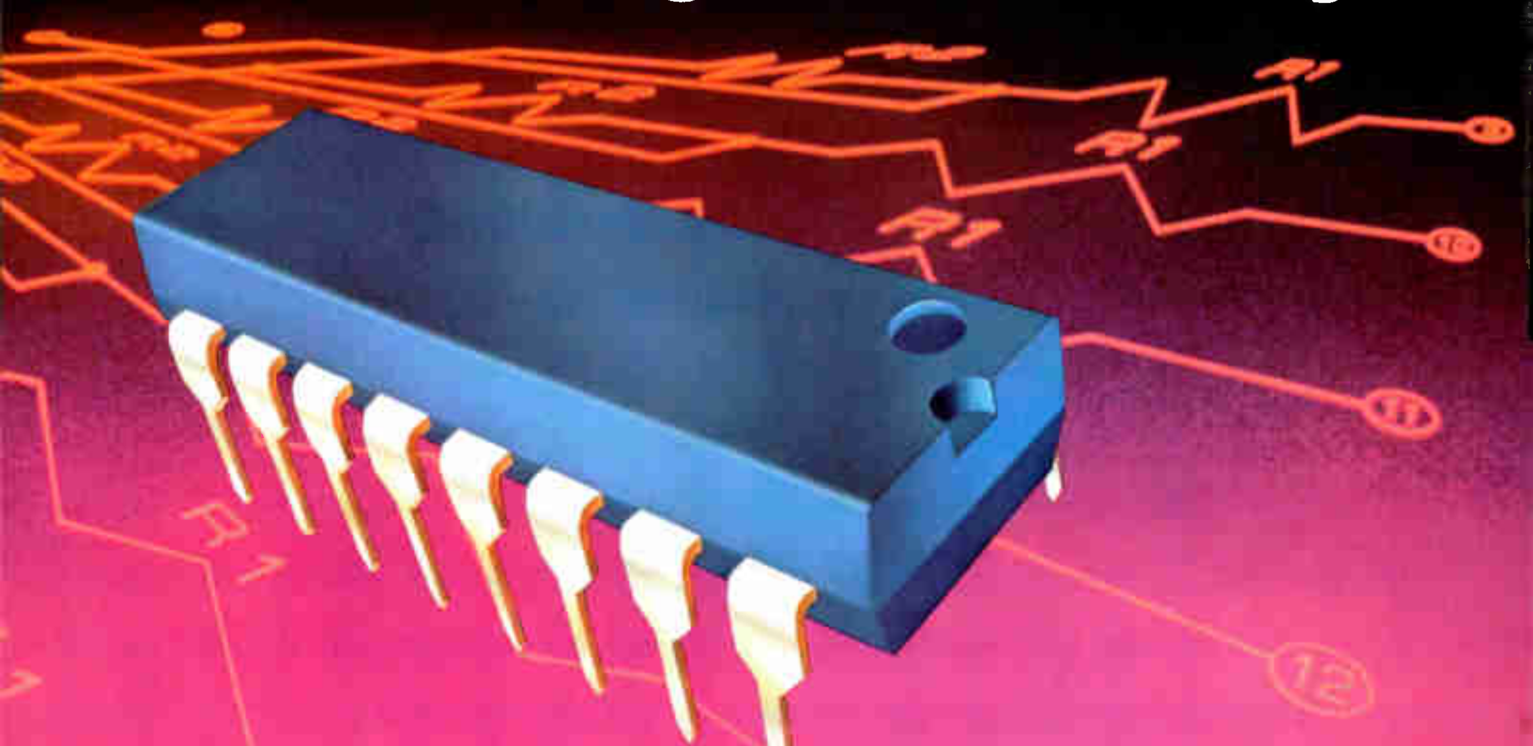

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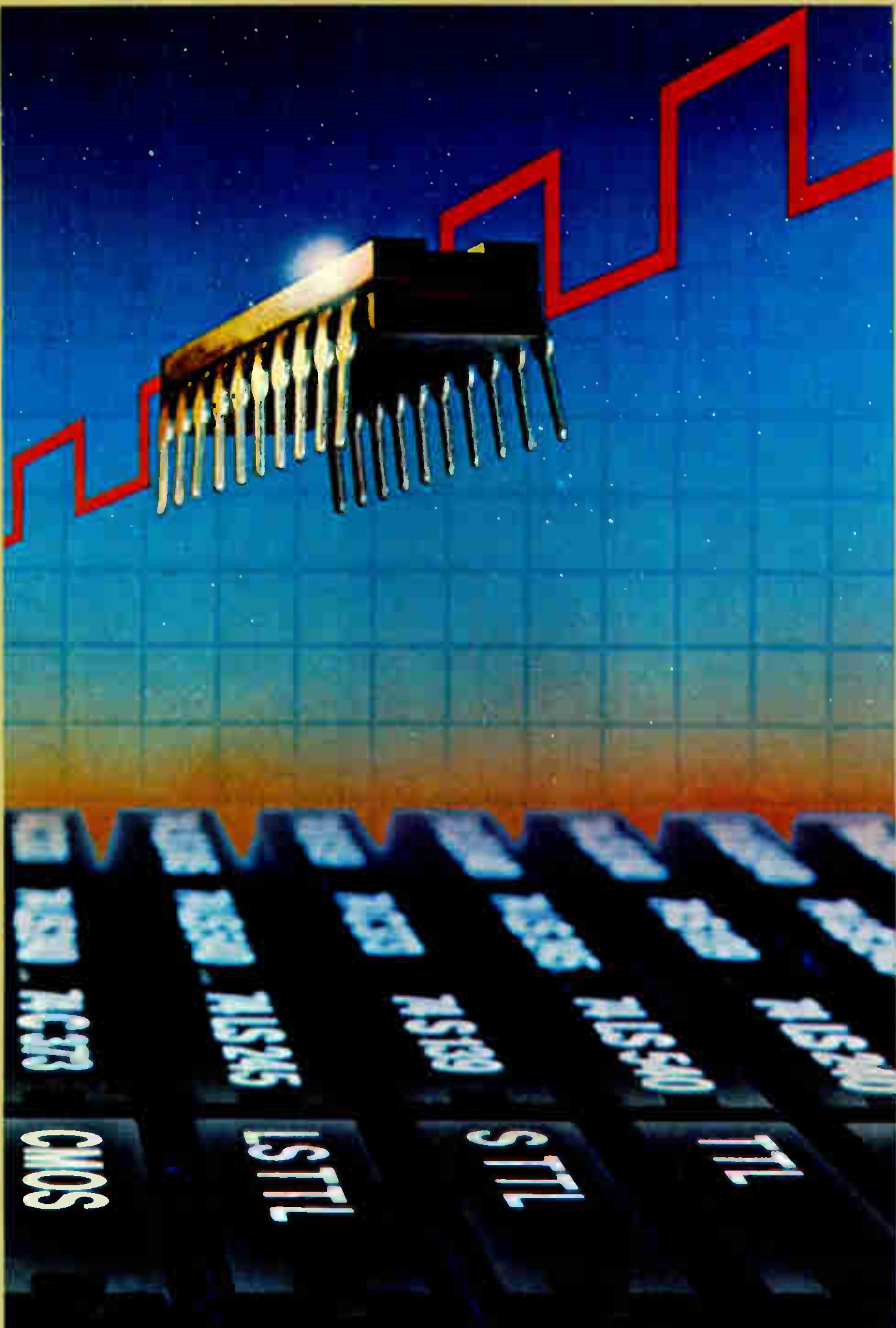

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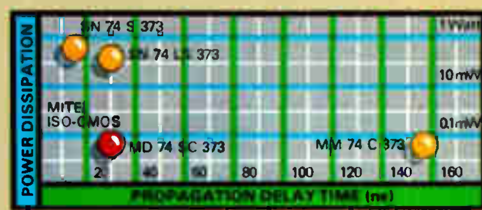

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Electronics
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Highlights

Cover: Super CAD races to VLSI designers' rescue, 73

True automated design of integrated circuits is still a dream, but computer-aided design is growing rapidly in power and sophistication. An extensive probe of the field describes software tools that have been developed independently at universities and by computer companies for work at various levels of the design process. Many of these tools are now being knitted together for a more unified approach to the prodigious tasks faced by designers of the coming very large-scale ICs.

Cover photograph is by Judy Gurovitz.

Low-power EE-PROM uses electron tunneling and floating gates, 89

Complementary-MOS peripheral circuitry surrounds an array of n-channel MOS cells in an electrically erasable programmable read-only memory that draws little power, even during its fast erasure and programming cycles. The electron-tunneling mechanism used with floating gates combines long data retention with good device endurance.

Development system debugs two-processor designs, 93

Putting two microprocessors to work together can do a lot for system throughput, but working out the kinks with a development system made to emulate one processor at a time is difficult at best. A software package that supports two synchronously operating emulators allows interprocessor-communications problems, for instance, to be dealt with.

64-K RAM turns a deaf ear to external noise, 103

The small cells and single 5-volt supply of a 64-K dynamic random-access memory increase the challenge of building in insensitivity to power-supply fluctuations, data patterns, and alpha radiation. This 64-K RAM owes its high noise immunity to folded metal bit lines and a special protective coating material.

Thermoelectric heat pumps keep circuits cool electronically, 109

Exploiting the Peltier effect discovered in 1834, the thermoelectric heat pumps developed in the 1960s were expensive and troublesome. Improved reliability, availability in a variety of configurations, and lower price now make these versatile and efficient devices attractive for controlled cooling of temperature-critical parts.

. . . and in the next issue

A delay pulse generator for synchronizing instruments in IEEE-488 test rigs . . . reliability testing and screening of E-PROMs . . . power MOS FETs that can be driven by TTL-level voltages . . . a peripheral controller for 8- and 16-bit systems . . . a dc-to-ac inverter for solar power systems.

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Publisher's letter

Computer-aided design for very large-scale integration is in full flower. Both Marty Marshall, West Coast computers and instruments editor, and Larry Waller, Los Angeles bureau manager, who put together the cover article on CAD (p. 73), found a wealth of material everywhere they went.

Virtually every source had something brand-new to discuss. So even though this report is probably the most comprehensive of its kind, it is essentially a snapshot of present CAD activities—there is more, much more, in the works.

As often happens in reporting and writing such extensive stories, the subject takes over the reporters. Thus, for example, Larry suggests that this Inside the News was fashioned like a CAD project. The outline of the story resembled a rough architectural layout; the reporting done at universities, semiconductor companies, and computer firms was like preparing the circuit and logic descriptions; and the writing and editing was similar to the preparation and editing of CAD software.

Marty agrees with the analogy: "We wrote in modules, as if building up CAD cells, then compared the modules to put it all together, as if implementing a hierarchical design."

One of the observations they made along the way is that universities are once again in the mainstream of feeding important research efforts into industry. Concurring, one industry contact pointed out that companies are now designing their fifth generation of computers, and this is the first time since the initial generation that universities are a vital cog in their development.

"This is an interesting time for these CAD projects," Larry observes. "Everyone is curious about programs others are doing, but there is no recognized clearinghouse of information. In most cases the people we interviewed asked what is going on elsewhere."

The sense of excitement and rapid change surrounding what we call super-CAD is everywhere, particularly on the campuses. "If these CAD programs had been going on at Caltech when I was there [1966–70], I would probably have graduated in electrical engineering instead of physics," Marty remarks.

It's always tricky the first time a new semiconductor process negotiates the dangerous passage from research lab to production floor. And for author E. Keith Shelton, section head for the Hughes Aircraft Co.'s research center in Newport Beach, Calif., his first time was a biggy.

The project was Hughes' recent entry into electrically erasable programmable read-only memories, which he describes in the technical article starting on page 89. Managing the transition from lab to pilot plant to full production is never easy, but in the case of the electron-tunneling oxide process developed for Hughes' EE-PROM, it was particularly tough.

Would he like to do it again? "Sure, it was a lot of fun," Shelton admits, adding that he also learned that Murphy's law (if anything can go wrong, it will) is indeed a factor.

In his five years at Hughes Research Center, he has spent most of his time working on charge-coupled devices, but he moved to the nonvolatile memory project about a year and a half ago when Hughes relocated most of its CCD work.

What Shelton walked into was one of the company's highest-powered projects—its entry into a potentially major market for EE-PROMs. "It's exciting to work on a product that is going to be big. You get a lot of attention from management and you either do well or go down the tubes," comments the 40-year-old graduate of the University of Kansas.

Shelton expects to remain with his newfound interest in nonvolatile memory. Hughes has other projects in the works, including development of nonvolatile memory in complementary-MOS on sapphire.

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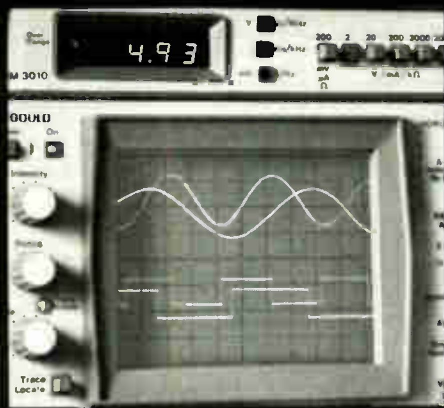

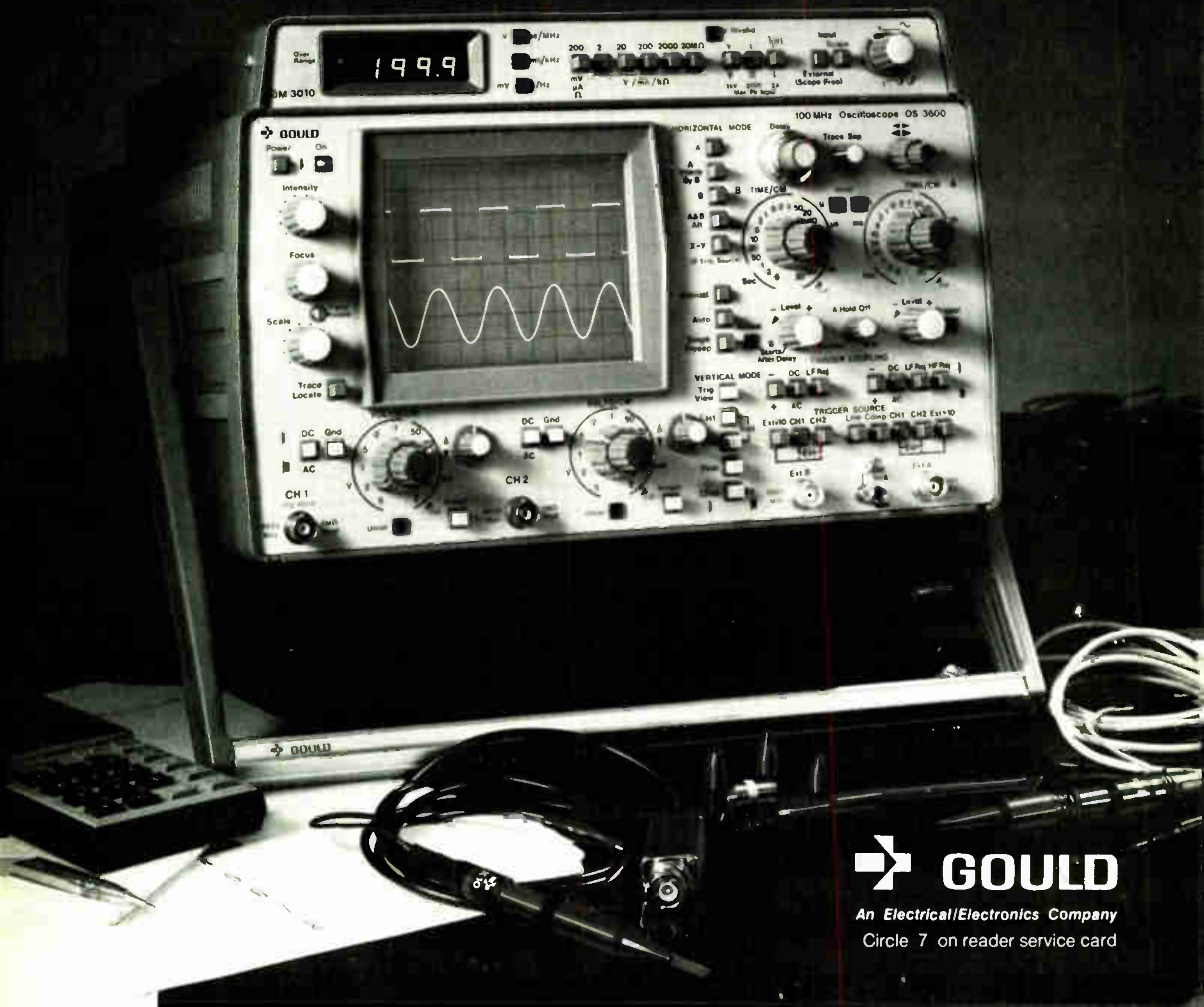

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Circle 7 on reader service card

Readers' comments

Not so great a range

To the Editor: "Airborne YAG unit to chart ocean shallows with sonar accuracy but 100 times the speed" (Jan. 17, p. 49), concerning the Hydrographic Airborne Laser Sounder that Avco Everett Research Laboratory Inc. is building for the U. S. Navy, correctly describes the general operation of the system but misstates the range over which the system's logarithmic amplifier can distinguish returned laser signals as 10,000,000:1 over a 100-megahertz bandwidth.

The range is, in fact, 10,000:1 over that bandwidth, which, to our knowledge, is the present state of the art for that type of amplifier. It is the high bandwidth at which the system operates rather than the dynamic range, as stated in the article, that allows for quick differentiation of the signals from backscatter.

Also, the laser peak power is 400 kilowatts rather than 400 megawatts and the laser pulse is 0.1 rather than 5 nanometers.

Joseph E. Nunes
Avco Everett Research
Laboratory Inc.
Everett, Mass.

A similar focus

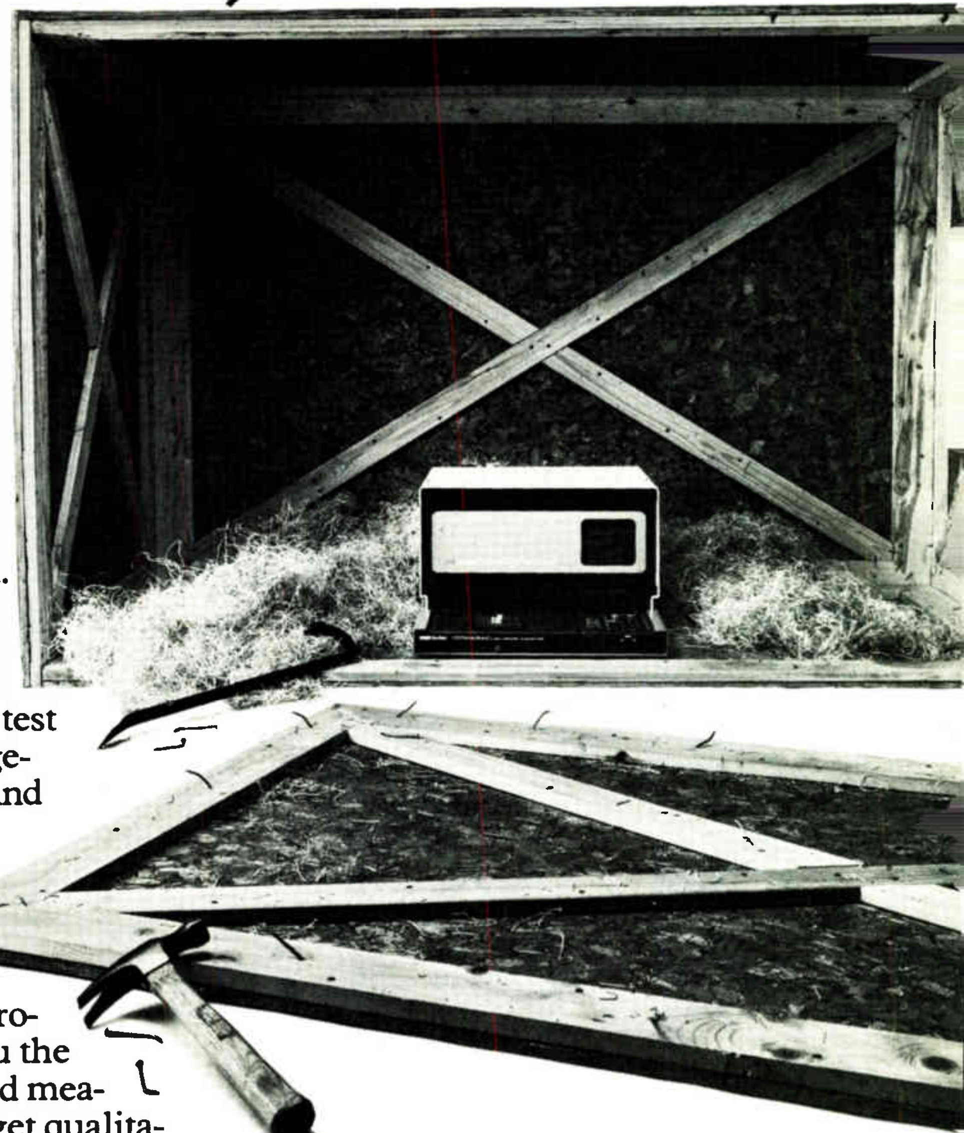
To the Editor: In reference to "Optical electronic sensor makes images quasi-one-dimensional for fast processing" (May 22, p. 84), I would like to inform your readers that an instrument using a very similar system—Auto-Focus, made by Carl Zeiss—has been on the market for about seven years. For focusing a microscope, it uses a camera to simulate the eye and a motor to drive the focusing mechanism of the scope. The system basically hunts for maximum contrast, which is a function of a properly focused image.

Tom Calahan
New York, N. Y.

Federal albatrosses

To the Editor: It is difficult to conceive of a more crippling blow to the American electronics industry than Leo Young's plan for a "presidential commission" leading to "cabinet-level" control ["A good place to start

GenRad offers a major reduction in big IC testers.



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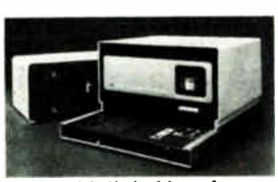

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Readers' comments

the counterattack," May 22, p. 24]. Mr. Young wants to do exactly the same thing to the American electronics industry that has already been done to the American public school system.

What is wrong with our industry is governmental macho-ism in the economy. History proves that any area [in industry] in which the government decides to become involved is doomed. If it were not for Government-caused inflation and taxes, no country anywhere would be able to come close to catching up with our electronics industry.

What the American electronics industry needs is to rid itself of all those albatrosses and millstones that have been placed there by the Federal government.

Cecil A. Moore
San Jose, Calif.

Time and space division

To the Editor: In "Digital telephone switching system compares with those in the West" (June 5, p. 78), John Gosch describes the East German system Ensad. But he fails to mention an important point for those following the "digital switching" scene—that is, that Ensad is a space division system using reed crosspoints.

This system is proof that the switching of digital signals need not employ the time-division technique that limits the bandwidth to half the sampling rate. The bandwidth capability of space-division switching, which many call analog, may be appreciably higher than that of time-division switches being deployed currently, and as in this example they may pass digital signals.

A. E. Joel Jr.
Bell Laboratories
Holmdel, N. J.

Correction

In the June 19 issue (p. 100), John R. Opel was mistakenly identified as both the president and chief executive officer of IBM Corp. Opel is currently president and will become chief executive officer as of Jan. 1, 1981, when Frank R. Cary resigns from that position.


JUST PLUG IT IN...
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People

Grua making Dictaphone a factor in word processing

The word. Dictaphone's Grua says understanding the office environment is critical.

Last month a $1 million campaign got under way to bring the name of Dictaphone—long associated with dictating equipment—into the word-processing marketplace.The effort began last January, when Pitney Bowes Inc., which had recently acquired Dictaphone, also acquired Artec International Corp. of Santa Clara, Calif. [*Electronics*, Jan. 17, p. 44], a word-processor manufacturer. In charge of the campaign is 51-year-old Rudy Grua, who is president of Dictaphone's Products and Systems group.

Grua, who has been with Dictaphone since 1973 and president of the Rye, N. Y.-based group since last August, has a 30-year history in sales and service of office equipment. He is putting that experience to work in marketing Artec's word processors under the Dictaphone label.

"An understanding of the office environment is so critical. The customer is crying for a reasonable bridge between the state-of-the-art technology and what he actually needs," observes Grua. That was IBM's original failure when it tried marketing office text processors in the early 1970s, he believes: "On paper, IBM's process looked super-efficient. But the resistance and resentment of the people trying to use the products arrested the growth of word processing at that time."

In his view, "what the customer is really looking for is the most benefit along with the fewest changes in personnel, and that doesn't necessarily mean the latest technology."

Grua received his early training using and servicing electronic equipment in the Army. He later went on to take courses in business and marketing at both Syracuse (N. Y.) University and the University of Hartford (Conn.).

He is adamant about Dictaphone's maintaining a realistic approach to marketing word processors because office personnel need "a subtle, almost transparent tool." He adds, "Until you can smell, feel, and touch the user market, it's difficult to innovate. We'll be starting out in a very ordinary, businesslike fashion. We want to understand our product marketplace; we need the pulse of the marketplace.

"The 1980s could easily be a graveyard of companies in office automation, and Dictaphone isn't going to be one of those companies," he concludes.

Groner to broaden TSI speech chips' horizon

Now that the speech-synthesis technology it developed for aids to disabled persons is spreading to a wide range of consumer and industrial applications, it is no surprise that Telesensory Systems Inc. has created a Speech Products division. Nor is it any surprise that Gabriel F. Groner has been chosen as vice president and general manager of the division, whose charter is to accelerate and expand the commercialization of the sophisticated speech-synthesis technology developed by the Palo Alto, Calif., firm for original-equipment manufacturers.

Formerly TSI's senior program manager responsible for research and development, manufacturing, and marketing of a family of synthetic-speech-output reading machines—using optical character recognition—for the blind, Groner is keenly attuned to the market. His

People

In the middle. TSI's Groner wants to bridge gap between the chip makers and the OEMs.

goal is "to get new products developed and out into the hands of users with as much haste and as little waste as possible," he says.

Spearheading such activity might test the patience of the 42-year-old Groner, but his experience should help him to meet the challenge successfully. He received a bachelor's degree in engineering from the University of California, Los Angeles, in 1960 and followed that with master's and doctoral degrees in electrical engineering from Stanford University in Palo Alto in 1961 and 1964.

Groner is now awaiting the availability of a pair of TSI-developed integrated circuits. Called the programmable digital signal processor (PDSP), this chip set can be programmed to implement a wide range of synthesizer structures, including both linear predictive coding and format synthesis techniques.

Hopeful of having the first PDSP samples this fall, Groner is responsible for their development and also for new products now in the lab that will use the n-channel chip set. He sees his division's role in this burgeoning area as "filling the gap" between the semiconductor makers producing speech-synthesis chips and the OEMs. "It takes more than a handful of silicon to get the job done," Groner states. "Our emphasis will be on full customer support, providing the OEMs with boards and speech-encoding services that are targeted at the higher-quality end of the applications spectrum." □

Another major milestone in MOS memory technology from Texas Instruments . . .

TI's 64K dynamic RAM is ready for delivery. Now.

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Ready with 4 times the capacity of 16K RAMs in the same size package.

Ready with 65,536 bits of random access memory — and that's more than many board-level computers.

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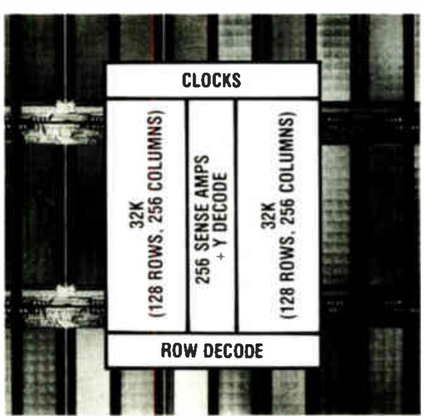
Improvements in density, reliability, system cost and ease of use are some of the features, functions and benefits system designers will appreciate. Here's more:

- 64K bits in a standard, 300-mil, 16-pin package saves valuable board space and reduces system size
- Single 5-volt operation lowers power supply cost and system cooling requirements and improves reliability

TMS4164 256 CYCLE REFRESH ARCHITECTURE



- JEDEC-approved pinout with N/C on pin one assures standardization and guaranteed availability
- High speed: 150-ns access and 280-ns cycle times (min.)
- TTL compatible I/O and clocks
- Lowest power dissipation available: 125 mW typical
- 256 cycle architecture means lower current peaks and reduced system noise
- State-of-the-art SMOS (Scaled MOS) processing

TI's new TMS4164 is perfectly suited for use in mainframe computers and large minicomputers. It also finds ideal application in microprocessor-based systems where smaller size, lower cost and improved performance are important considerations.

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TMS4164. Truly another major milestone in MOS memory technology. Truly another example of the total commitment Texas Instruments is making to leadership MOS memory products.

For more information about the deliverable 64K RAM, call your nearest TI field sales office, or write to Texas Instruments Incorporated, P.O. Box 1443, M/S 6965, Houston, Texas 77001.

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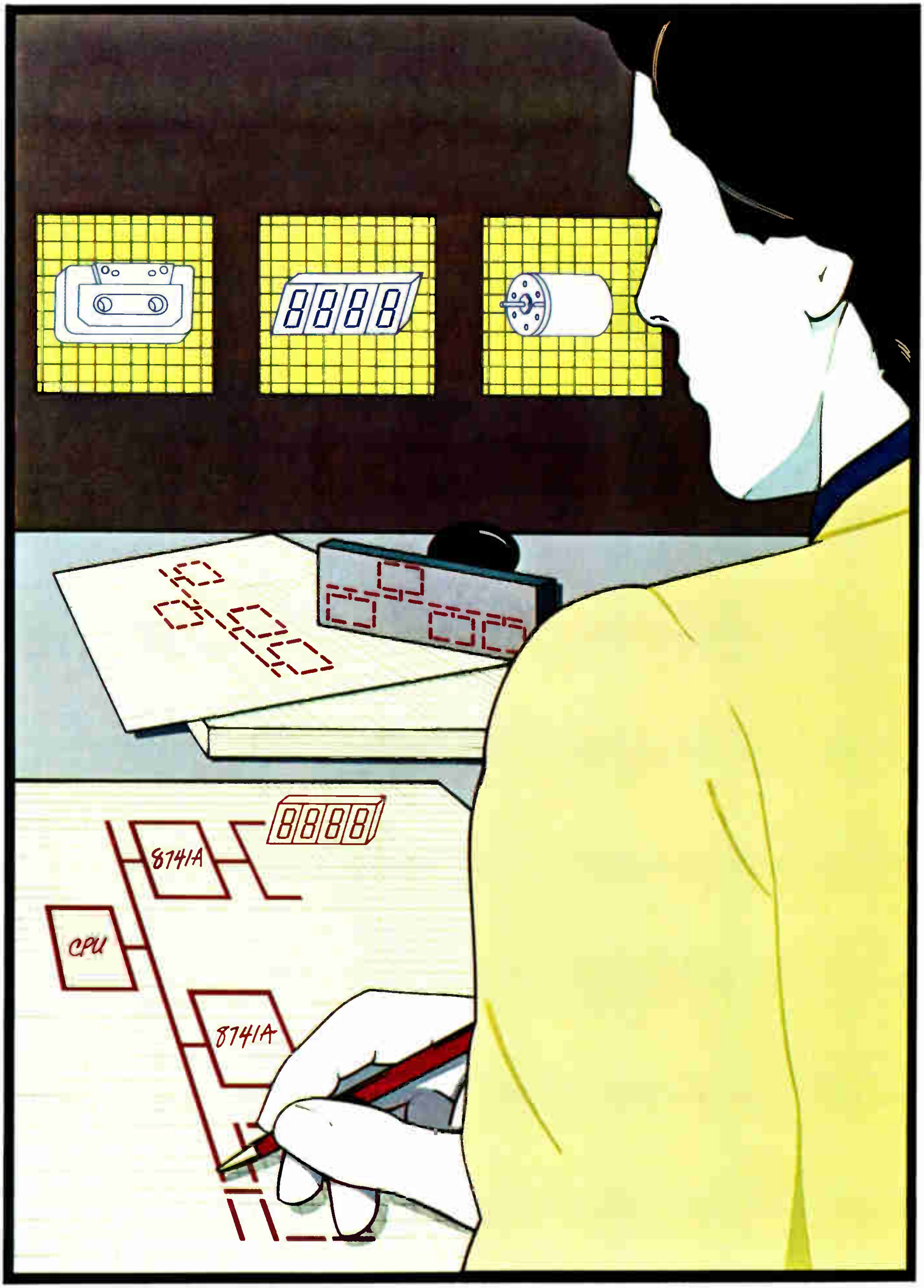
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Consider the Options

Choose Intel's 8741A: the only peripheral controller with on-chip EPROM memory and unparalleled development support.

For almost any application where a system peripheral device interfaces to a microcomputer, Intel delivers the flexible design solution: our 8741A. It's the only UPI™ controller in the industry to give you EPROM memory *and* vital support that minimizes design and debug time. It's the proven peripheral controller available now ... in your choice of ROM and EPROM versions.

Easy-to-instruct slave processor puts you in control.

If you demand more flexiblity from your controller, our 8741A delivers. The 8741A assures that everything from keyboard control to complex process control tasks within your system design can now be efficiently developed as separate projects... simplifying your design and making your project more manageable.

Because Intel's 8741A controller is a true slave processor, it acts under control of the host processor. And it never monopolizes the system bus. By executing macro commands from the host, our UPI controller executes from on-chip program memory... operating in parallel with the host CPU and freeing the host CPU to do its job.

More than just an intelligent controller, our 8741A contains an 8-bit CPU, 1K byte program memory, 64 byte data memory, clock, timer/counter plus I/O ports. But the performance features of Intel's 8741A go way beyond that.

EPROM programmable memory helps stamp out high design costs.

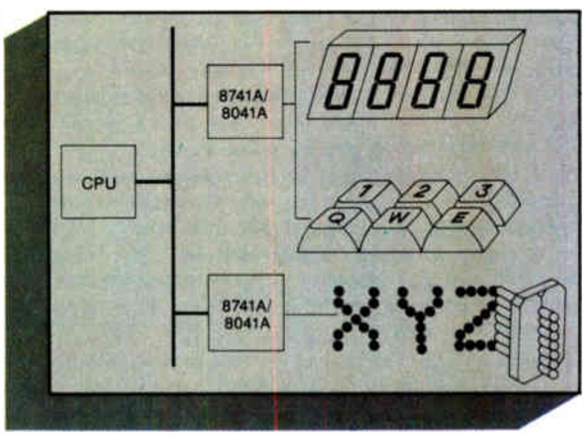
In terms of both redesign and testing, Intel's 8741A with on-chip memory offers freedom and flexibility to incorporate new features into the controller. No cost sacrifices or wasted time. Change your software as many times as necessary during development, or when new features are added to the product.

When your programs have been developed, just switch to our pin-compatible ROM version of the UPI controller, our 8041A... it's the economical solution for volume production usage.

A versatile controller with an easy instruction set.

If you're familiar with the instruction set for Intel's industry standard 8048, you've already made the investment in learning the instructions for our 8741A. The majority of the 8741A's instructions are control oriented, so you can easily program your controller to handle a wide range of I/O tasks.

The result? Our 8741A, a controller for peripheral devices that have no other "off-the-shelf" solution.



No other development support can serve you better.

Intel doesn't just deliver a powerful controller, we also give you powerful debug tools. With our ICE-41A™ in-circuit-emulator, Multi-ICE™ software package and Intellec® development system, you can locate design flaws and software bugs in even the most complex multiprocessor designs.

Consider Intel's ICE-41A emulator and Multi-ICE software as your direct diagnostic connection. With Intel ICE™ modules, you can debug the peripheral controller and an entire system... all in real time. You can also rely on Intel to deliver Multi-ICE software. This unique tool lets you have two ICE modules running in parallel, plus macro and compound command extensions to the ICE-41A software that reduce testing time, errors and inconsistencies.

The ICE-41A module lets you use English-like commands and symbolic debugging to monitor hardware and software operation. It lets you modify registers, memory locations and I/O ports. With ICE-41A modules, Intel delivers the only intelligent solution for designing intelligent controllers.

Intel's 8741A, the designer's choice.

If you want shorter design cycles, cost reduction, reliability and performance, you want Intel's 8741A. Proven in hundreds of designs worldwide, it's the best supported UPI controller you can incorporate into your design. And it's available in quantity now.

For more information, contact your local Intel sales office or distributor. Or write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051.

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Today's microprocessor development systems are more sophisticated than ever. If you select the right one, it can make your job easier and help speed the development process. But to choose such a system requires more than just a knowledge that it's compatible with your microprocessor.

True transparency?

The first contribution of any microprocessor development system is in the area of software development. Beyond this, it must provide a RAM environment, downloading capability and run controls. That's where emulation comes in. Ideally, the development system should be totally transparent to your target processor. However, complete transparency is prohibitively expensive. Thus some compromises must be made.

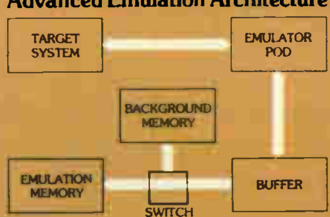
Some criteria.

How can you judge how close a particular development system actually comes to true transparency? We think there are three important criteria: How emulator control is isolated from the user system; the RAM environment; and the speed of real-time emulation.

A better answer to interrupts.

With many systems, when you wish to take control of the processor to initialize a program counter to a particular value, interrogate a register, or single step through a program, the target processor must be interrupted via an interrupt line. In contrast, HP's 64000 Logic Development System 8-bit emulators incorporate a different architectural philosophy. Instead of calling for an interrupt, they achieve functional transparency through the use of bank switched background memory where all emulator control programs reside. As a result, no interrupt lines are usurped and no processor address space is occupied by emulator control programs.

Advanced Emulation Architecture



All the memory you're paying for.

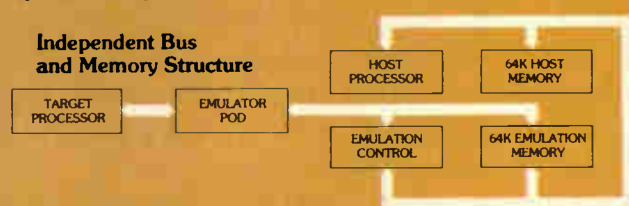
Another way in which HP steps closer to true transparency is in RAM environment. While other systems may have memory that can be accessed by both the host and target processors, the HP 64000 separates the host and target processors, buses and memory. The host processor executes the monitor program, operating system and application program, and manages the system options and I/O. It executes out of its own 64k memory in conjunction with a choice of 12 to 120 Mbyte hard disc, which functions as a virtual memory and provides mass storage.

This means you get the use of all available emulation memory . . . and you have no contention problems. What's more, the 64000 architecture lets you do other tasks while emulation is in progress. For example, you can modify emulation memory while your processor is executing a program.

The meaning of real time.

How close a system will run to real-time is a function of memory chips and system architecture. The HP 64000 uses high-speed memory chips and microprocessors which impose fewer artificial speed limitations. Since both the host and target processors each have their own dedicated memory and buses, there's never a contention problem; and in most applications your system runs at operating speed with no wait-states. And the 64000's optional internal analyzer gives you a real-time, transparent view of target processor bus activity to help you spot problems that show up when your system operates at speed.

Independent Bus and Memory Structure



Other important differences.

The HP 64000 ($23,500* for the basic system including emulator plus 8K of emulation memory) offers other important advantages. It uses a universal, rather than a dedicated approach, so that you can use it with most of today's popular microprocessors. Its directed syntax utilizes "soft keys" that speed learning and simplify operation. HP's shared peripherals approach means that a common data base can serve up to six development stations for team software development. And its user-oriented display editor speeds both editing and debugging.

Find out how close to true transparency a development system can come. For a copy of the HP 64000 brochure, write to Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304. Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.

*Domestic U.S.A. price only.

080/5

HEWLETT PACKARD

Circle 23 on reader service card

Editorial

The wrong kind of tax cut at the wrong time

The sight of members of Congress from both sides of the aisle falling over themselves in their eagerness to cut taxes (see p. 50) is one of the more amusing yet least enjoyable sights that the nation's capital has to offer this election year. In fact, the computer used by congressional committees and the Treasury Department to analyze the cost of the tax proposals even broke down.

The cruel irony of this exercise in confusion (how many Americans can select from the pros and cons of tax-cut economics?) is that across-the-board tax cuts are designed to create demand, and demand is one of the reasons we are in the condition we're in today. Instead of compounding that error, the thinkers in Congress might pay more attention to supply—the supply of technology needed to solve America's problems of productivity and competition on a global basis—and the jerry-built tax structure that actually seems to penalize research and development as well as entrepreneurial zeal.

What is plainly needed is not so much a general tax cut that would encourage citizens to spend more of their income for cars and houses and refrigerators, but an overhaul of the tax laws to place greatly increased outlays for R&D within the budgetary limits of even smaller companies. But this is an election year, alas, and it is difficult to force the attention of our leaders past the quick and easy and palatable fix, past the first Tuesday following the first Monday in November.

Taking the statistics a step further

The new, more detailed reporting of semiconductor imports by the Federal government due to start this month [*Electronics*, July 17, p. 61] is bound to please those in the industry and those who follow it closely. Dependable information from U. S. agencies has been hard to come by, most notably that dealing with imports from Japan. In fact, one of the ironies of the data-gathering trade has been that some professional industry watchers trust Japanese sources more than domestic ones. In the words of Mel Eklund, president of Integrated Circuit Engineering, a Scottsdale, Ariz., consulting firm, "Given the choice, I'd believe the Japanese data first."

But now that the Departments of Commerce and Treasury and the International Trade Commission have reached agreement, with the Semiconductor Industry Association serving as a kind of watchdog to ensure the continued accuracy of the numbers, there is more to be done. As Eklund points out, "We still need to separate the import data between the various foreign manufacturers," particularly the Japanese. Also, since most manufacturers declare items' value lower than the ultimate market prices (to keep the tariff bite smaller), there is a big difference between reported semiconductor import figures and actual sales dollars. Even though foreign manufacturers profess not to know the market values, the SIA should push guidelines using only final market values—a difficult task, Eklund concedes, but one worth the effort. Finally, the new categories that separate microprocessors and memory chips help but do not go far enough. Memories themselves should be further subdivided—Eklund finds about a dozen categories of random-access and read-only devices, as well as electrically erasable programmable ROMs.

A good start has been made, and the logjam appears to have been broken. Industry, spearheaded by the SIA, should continue to press the Government for more cooperation and the better statistics that are bound to result.

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Impact of the AT&T Business Unregulated Subsidiary and the Restructuring of the Computer/Communications Industry, The Yankee Group (Box 43, Harvard Square Station, Cambridge, Mass. 02138), Meadowlands Hilton, Secaucus, N. J., Aug. 5–6, and Palo Alto Hyatt, Palo Alto, Calif., Aug. 12–13.

1980 Joint Automatic Control Conference, IEEE, Instrument Society of America, *et al.*, Sheraton-Palace Hotel, San Francisco, Aug. 12–15.

Electronics/China 80, U. S.–China Trade Consultants Inc. (Clapp & Poliak Inc., P. O. Box 277, Princeton Junction, N. J. 08550), Guangzhou (Canton), China, Aug. 14–24.

First Annual National Conference on Artificial Intelligence, American Association for Artificial Intelligence (AAAI 1980 Conference, Stanford University, P. O. Box 3036, Stanford, Calif. 94305), Stanford University, Aug. 19–21.

International High-Fidelity Trade Fair with Festival, Nowea (D-4000 Düsseldorf 30, P. O. Box 320203, West Germany), Fairgrounds, Düsseldorf, Aug. 22–28.

First Annual Hewlett-Packard 1000 International Users Group Conference (Glen A. Mortensen, Intermountain Technologies Inc., P. O. Box 1604, Idaho Falls, Idaho 83401), San Jose Hyatt House, San Jose, Calif., Aug. 25–27.

The 12th Conference on Solid-State Devices, The Japan Society of Applied Physics (3–5–8 Shiba Koen, Minato-ku, Tokyo 105), Tokyo Chamber of Commerce & Industry Building, Aug. 26–27.

10th Symposium on Electromagnetic Theory, Verband Deutscher Elektrotechniker (D-6000 Frankfurt 70, Stresemannallee 21, West Germany), Munich Technical University, Aug. 26–29.

The 15th International Conference on the Physics of Semiconductors, Physical Society of Japan (Hiroshi Kamimura, Department of Physics, Tokyo University, Tokyo), Kyoto International Conference Hall, Kyoto, Sept. 1–5.

Electronic Business Communications Conference, Electronic Industries Association (2001 Eye St. N. W., Washington, D. C. 20006), Las Vegas, Convention Center, Las Vegas, Sept. 3–5.

Second International Colloquium on Reliability and Maintainability, Centre National d'Etudes des Télécommunications and Centre National d'Etudes Spatiales (CNET Reliability Center-Lannion B, B. P. 40—22301 Lannion, France), Perros-Guirec and Trégastel-Lannion B, Brittany, France, Sept. 8–12.

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The MC68000 processor is now available

The best available 16-bit microprocessor is now available from authorized Motorola distributors everywhere. The MC68000.

Since its introduction in September, 1979, the MC68000 generally has been recognized as the most advanced high-performance 16-bit microprocessor in the industry.

The MC68000 is the first, the only, 16-bit microprocessor with a large set of seventeen 32-bit registers, and the only one with 16-megabyte direct memory addressing.

Its uniquely powerful yet easy-to-use micro-coded architecture, combined with the inherently high-performance characteristics and reliability of Motorola's HMOS VLSI technology, offers the designer unmatched advantages in system design, software cost reduction and product capabilities.

As a vital aspect of future systems, efficient multiprocessing capability received special attention in design of the MC68000. With the asynchronous bus, a multiple bus-master technique is used to achieve high-efficiency multiprocessing.

Expanded register set allows enhanced performance.

The 32-bit registers eliminate the need for pairing, and data and address registers are separated to allow the performance enhancements of parallel operation. All the registers can be used as index registers, and all address registers may be used as index stack pointers to reduce programming bottlenecks.

High-efficiency instruction set.

The simple, efficient instruction set was designed on information developed in extensive instruction-usage studies. The 56 powerful instruction types are designed to minimize the number of mnemonics a programmer must remember. Addressing modes are usable with all applicable instructions for additional ease-of-use

for advanced systems from Motorola distributors.

and reduced software debugging time, with resulting software development-cost reduction.

Asynchronous, non-multiplexed bus.
Implementation of the asynchronous bus allows optimum utilization when supporting devices requiring different access times, and allows implementation of cache memory or other hierarchical memory schemes without bus rule changes. The non-multiplexed bus is up to 30% faster than a multiplexed bus, and improves overall system performance because interface to the processor is not a bottleneck.

Designed for high-level language support.
As the processor for the '80s, the MC68000 was carefully designed for the high-level languages of the '80s. With Link and Unlink instructions, the large number of general-purpose registers, address manipulation on stack, and a variety of additional features, the MC68000 is, by design, the ideal MPU for an easy-to-use, block-structured high-level language. It's equally fluent with Pascal or assembly language.

Efficient operating system support.
Numerous features offer valuable operating system support. Among the most important is the distinction between the user mode and the supervisor mode which improves system reliability and allows resource protection. Also included for such support are specific instructions such as the Test and Set instruction (for semaphore operations), Traps (for efficient operating system calls), and the Move Multiple instruction (for streamlined context switching).

Code reliability for system integrity.
Code reliability and maintainability are key issues for any system designer in this day of large software development efforts. Illegal instruction and illegal addressing mode detection aid system designers in guaranteeing system reliability.

The user/supervisor distinction, privileged instructions, and traps on unauthorized activity aid the system designer in guaranteeing systems integrity.

The choice of winners.
The power and versatility of this total system approach is more apparent than ever as the tremendous scope of the entire M68000 family concept is revealed.

Designers who require the very best in advanced high-performance microprocessors turn to Motorola. The M68000 family, present and future, will be the choice of winners throughout the '80s. Shouldn't it be yours?

With the flexibility of the developing total-system M68000 family, and the system-development support of EXORmacs™, VERSAbus™ and the VERSAdos™ multi-tasking, multiprocessing operating system, there is no contemporary approach to microcomputers that offers so much for so many systems. The MC68000 is your best bet for the '80s for

Innovative systems
through silicon.

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Everybody talks about 64K ROM's. We're delivering. In quantity. Now. 2364's. And 2332's. And 2316's. All compatible with your 2700 Series EPROM's. Eight week delivery in production quantities. Five week delivery in prototyping quantities. Guaranteed.

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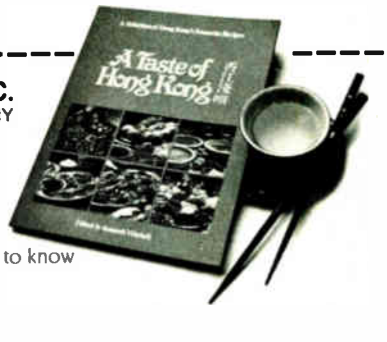

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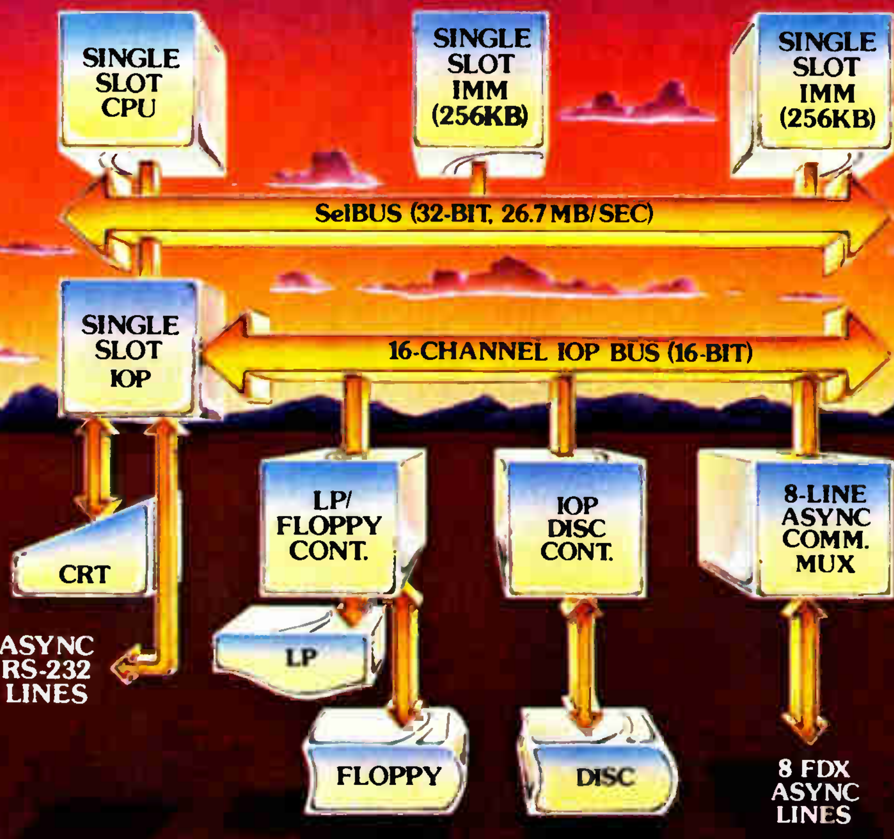

The trouble with most small minicomputers is that they started out as big minis and were simply scaled down. Same functionality. Similar performance. Lower cost. (You've seen the ads). If you're an OEM, you also know those "minis" retained all their complexity. Big mini interfaces. Expensive memory. Costly device controllers. Complex architecture. A big machine, in a cumbersome cabinet. Functionality? Sure. But with all the problems still there for you to solve with your bucks.

Now there's a better way. Want to move to 32-bit mini functionality, without investing in the problems? CONCEPT/32 is your answer. A single slot LSI processor with the proven 26.7MB SelBUS. Integrated Memory Modules (IMM) for faster data access, more functionality, and single-slot memory in 256kB increments. An I/O Processor (IOP) to off-load I/O management functions from the CPU and make the total system more efficient. Specially designed intelligent IOP controllers on a unique, smaller IOP bus for "friendly I/O and interfacing". Control Panel functionality on the console CRT. And all with enhanced reliability, lower cost, and requiring 40 percent less power than any comparable mini.

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Circle 32 on reader service card

Electronics newsletter

'Silicon foundry' operation eyed for Mostek, tech center

A so-called silicon foundry operation, offering complete circuit design and fabrication services to outside design groups, could be in the works for United Technologies Corp.'s upcoming microelectronics center. The center will primarily develop computer-aided design and software tools to be used by UTC's operating divisions to design circuits for their own use. Though full-blown operation is several years away, **UTC's long-term plan reportedly envisions one of those divisions, Mostek Corp. of Carrollton, Texas, as the merchandising arm** for such services, by which software tools supplied to outside designers would be linked via data-network lines to a central silicon fabrication facility. Such an approach would be similar to the silicon foundry idea advocated by circuit design expert Carver A. Mead of the California Institute of Technology [*Electronics*, March 13, p. 90]. Though a small Los Gatos, Calif., firm known as VLSI Technology Inc. is planning to pursue Mead's idea on a startup basis, no major semiconductor manufacturer has yet embraced the concept.

Alpha radiation spurs Motorola to use polyimide coat

Those gremlins known as alpha particles have been causing some soft-error problems in Motorola Inc.'s 64-K dynamic random-access memory—the MCM6664/65—despite the company's use of folded metal bit lines and other design techniques aimed specifically at combatting alpha radiation. As a result, the firm this month began applying an organic polyimide die coat to all production 64-K dice. In tests using an accelerated alpha source, **the polyimide coating has provided an effective shield without affecting device performance.** It will also be used on forthcoming production units of the company's single-power-supply 16-K RAMs, say officials at Motorola's MOS memory group in Austin, Texas. Among companies that plan to supply 64-K RAMs for the merchant market, Hitachi, for one, will also use a polyimide die coat (see p. 103), and IBM Corp. does likewise on 64-K parts built for internal use.

Mostek tests bipolar technology for telecommunications

With an eye toward potential future telecommunication circuit needs, Mostek Corp. has begun experimenting with bipolar technology. Within recent weeks, the Carrollton, Texas, MOS manufacturer has begun running a small number of bipolar wafers **using a simple process on an existing MOS fabrication line.** Though Mostek already supplies a broad line of complementary and n-channel MOS telecommunications chips, the impetus for the move is the potential requirement for a bipolar process to produce certain circuits that may eventually be needed to fill out the family as the telephone industry goes digital. Two device types have been identified—the side-tone network and the subscriber-loop interface circuit (SLIC). The firm hopes to have masks for the side-tone network device by year-end.

Radio Shack ready to lower TRS-80 price floor

Already the volume leader in personal computer sales, Tandy Corp.'s Radio Shack division is broadening its line. The 1981 Radio Shack catalog—due out Aug. 1—is expected to contain three new personal computer products that will supplement the Fort Worth, Texas, company's existing TRS-80 family. Officials at the firm are keeping mum about specific market segments targeted, but the new offerings are believed to include **at least one product that will be priced lower than the current $500 minimally configured TRS-80 model I** desktop machine. Tandy is also thought to be aiming at some new higher-end applications as well.

Electronics newsletter

Exxon purchases piece of V-MOS power FET house

Supertex Inc. has spent most of its first five years making a name for itself with vertical-groove MOS power field-effect transistors. Now, Exxon Enterprises Inc., the venture capital subsidiary of Exxon Corp. in New York, is understood to have acquired 15% to 20% of Supertex. The Sunnyvale, Calif., firm may, indeed, prove to be a tiger in Exxon's tank, for it has been quietly developing a new series of V-MOS power FETs **with current-handling capability more than three times that of devices with equivalent die size and voltage ratings.** With modifications to its device structures and double-diffused MOS (D-MOS) process, Supertex has lowered on-resistance to 0.25 Ω or less, improving the efficiency of high-voltage devices so they can handle a continuous current upwards of 30 A.

Microcontrollers to be first COPs made with C-MOS

National Semiconductor Corp., Santa Clara, Calif., is about to take the wrapping off four new members of its COP (control-oriented processor) family of single-chip microcontrollers containing all system timing, internal logic, read-only and random-access memory, and input/output capability necessary to implement dedicated control functions in a variety of applications. **The new devices have the lowest power dissipation, typically 50 μW in standby, in the family.** COPs have been fabricated up to now in n-MOS technology only.

AMI to build C-MOS version of Motorola 6809

Joining the rush to build complementary-MOS versions of popular n-MOS microprocessors, American Microsystems Inc. of Santa Clara, Calif., will soon move its C-MOS rendition of Motorola's high-end 8-bit processor, the 6809, to the mask shop for production next year. That adds AMI to the list that includes Harris Corp. (making Intel's 16-bit 8086), Intersil and National Semiconductor (reworking the Intel 8-bit 8048 microcomputer) and Mitel Semiconductor (which has seen several passes of silicon on the Motorola 6802 in C-MOS). **Also, Mitel and AMI reportedly have struck a deal to exchange their C-MOS Motorola copies and to jointly design support chips.**

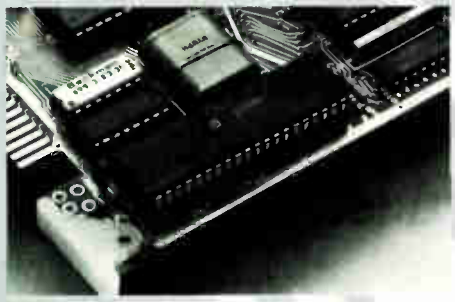
Perkin Elmer adds CAD to 32-bit minis

Joining other makers of 32-bit minicomputers in the computer-aided design market, Perkin Elmer Corp. is adding a CAD capability to its 32-bit mini family. **Using the $95,000 AD-2000 mechanical design and drafting software package from Manufacturing and Consulting Services Inc.,** Santa Ana, Calif., the Computer Systems division in Oceanport, N. J., has configured three systems based on the 3220 and 3240 computers, ranging in price from $179,000 to $300,000.

System polices cable receiver

Stopping the kids from watching R-rated movies—or any other undesired programming—on cable television is going to be easier now that Tocom Inc. of Irving, Texas, has made available its self-policing system. **This computerized control equipment allows selection of programs by means of code words.** The concerned party simply punches a code word into the receiver to allow only certain categories. According to Tocom chairman John G. Campbell, several of the cable television suppliers bidding for a new system for Dallas, Texas, have included the coding feature.

Synertek's 1791 Floppy Disk Controller can take the heat.



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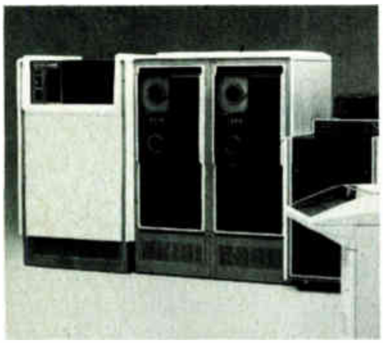

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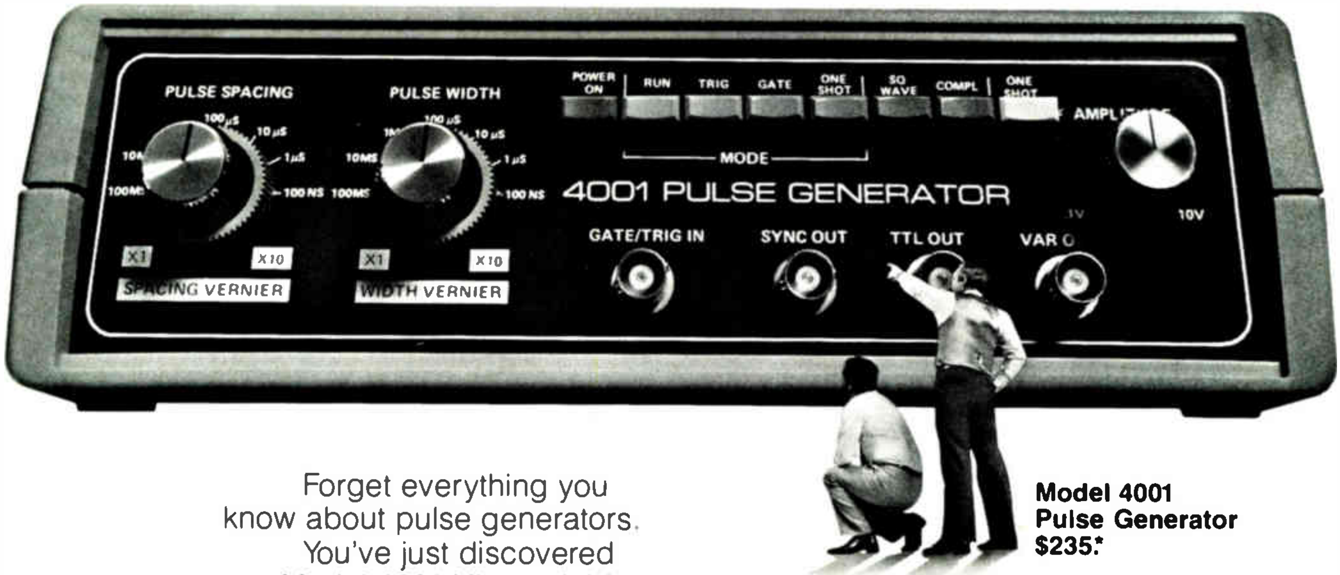

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LSI solution handles phone call routing in central offices

by Harvey J. Hindin, Communications and Microwave Editor

Bell system on a board includes big n-MOS chip performing time-slot control, address functions

A T1 digital transmission line is carrying as many as 24 voice and data signals when it enters one of American Telephone & Telegraph Corp.'s switching offices. Since it is costly to route these signals through a great many components occupying a lot of board space, a team at Bell Laboratories has designed AT&T's largest n-channel MOS chip—the time-slot assigner, capable of distributing any of the T1 system's 24 incoming streams of signals to any of 256 outgoing lines.

The large-scale integrated circuit and its associated custom ICs (see photograph) are the heart of what the telephone people call a digital access and cross-connect system. A typical DACS allows a 26:1 space saving over a system that uses medium- and small-scale ICs. The new time-slot assigner chip alone replaces three 8-by-10-inch circuit boards.

Necessary. All this routing is necessary because the signals that come into the central office are a mix of types. Some, such as private-line or tie-line calls, must be switched from one T1 system to another. Others—ordinary telephone calls, for example—may have to be converted to analog form for immediate delivery. With DACS, all this is done automatically, whereas previously it might have had to be done by mechanical switching and wiring procedures.

DACS not only routes calls, it also segregates voice messages by type and collects messages with common destinations so as to increase the average message load of the T1 channels. Furthermore, it simplifies the connections and testing required between central offices.

One big advantage is that only those signals that need it are converted into analog form. In older system approaches, all the signals had to be converted for routing and then reconverted into digital—a tactic that degrades their signal-to-noise ratio.

A big one. The new IC, called a time-slot assigner, is 10.64 by 8.13 millimeters and has 3.5-micrometer line widths. Despite the size, "its yield is pretty good," says John R. Colton, supervisor of the controller group in the Holmdel, N. J., lab.

Most of the chip's 36,000 transistors perform control and address functions, with but 3,500 bits of on-board random-access memory for control and data handling. The rest of the system has 32 kilobytes of RAM and 192 kilobytes of read-only memory, but this total can serve as the equivalent of 1 megabyte of storage because of what Colton calls DACS' state-of-the-art memory management software.

"This kind of memory management is usually only applied to mini- and maxi-computers," he says. The DACS' great memory demands made such an operating system necessary, he adds.

Eight microprocessors, distributed throughout the system, operate DACS. Two, Bell's own MAC-8, are "the brains of the system," Colton says. They handle the time-slot assignments and testing between central offices.

The six other processors are commercially purchased parts, whose identity Bell will not disclose. Four are in the synchronizer that controls the timing of the myriad of signals in the system; one is the controller for the backup bubble storage; and the sixth is in the alarm interface and controls circuits warning of various

LSI solution. One of several custom chips in Bell's new line-distribution system is the carrier-alarm IC, which monitors all incoming T1 channels for signal loss.

system failures, such as loss of signal in the T1 channels.

Since the system RAM is volatile and loses its information in a power failure, DACS has a bubble memory backup. Made from standard Western Electric products, it constantly memorizes the latest assigned routes for protection of the operation.

Having undergone extensive tests at the Holmdel facility, DACS is scheduled to enter the telephone company's installation cycle in the second quarter of 1981. Offices having it will be able to handle as many as 127 bidirectional T1 lines.

Solid state

GaAs test memory with 100-ps delays has structure of MOS statics

Anticipating a need for the speed of gallium arsenide integrated circuits by the end of the decade, engineers at Lockheed Missile and Space Co. have started developing GaAs ICs for spacecraft communications systems. Their latest achievement is a GaAs static random-access memory operating from a ±0.5-volt power supply and with gates that have propagation delays of about 100 picoseconds.

Made with both enhancement- and depletion-mode metal-semiconductor field-effect transistors, the part uses 1-micrometer design rules for a cell size of 57 by 40 μm and an overall size of 20 by 10 mils. "Long term, we expect to produce GaAs memories that are three to five times faster than silicon memories," says Donald K. Kinell, staff engineer at Lockheed's Microelectronics Center in Sunnyvale, Calif. Production parts with 2-μm geometries should have access times of between 5 and 10 nanoseconds, whereas 1-μm ICs could have access times of 2 to 4 ns, he predicts.

The Lockheed engineering team has just designed the mask set for a divide-by-2 prescaler that will be its next GaAs chip. It will be followed by a 2-bit adder. "We will design a 16-bit memory next and test out the various buffers and decoding logic," Kinell notes.

The test IC uses the cross-coupled flip-flop design with depletion transistor loads commonly found in static MOS RAMs. Lockheed thinks it is taking a major step in including both enhancement- and depletion-mode devices on the same GaAs chip. Enhancement-mode devices do not have the drive capability of depletion-mode devices and are more difficult to fabricate because they require tighter control of pinch-off voltages, Kinell notes.

However, "coupling the two will yield the higher densities and reduced power (0.5 milliwatt per gate) associated with enhancement-mode circuits, while keeping the speed close to that of depletion-mode circuits," he says.

Speed. The speed potentials of GaAs circuitry are breathtaking. For example, a Lockheed test logic IC demonstrated gate delays of 50 picoseconds, corresponding to a clock frequency of 2 gigahertz. The best present silicon circuits are emitter-coupled logic with delays between 700 ps and 2 nanoseconds.

Researchers at Nippon Telegraph and Telephone Public Corp.'s Musashino Electrical Communication Laboratory recently developed a GaAs test IC holding a 15-stage ring oscillator with a gate delay of 30 ps alongside 3-GHz divide-by-2 and divide-by-8 prescalers. Fabricated with electron-beam direct exposure, the IC has ½-μm gate lengths.

By comparison, experimental Josephson-junction circuits at IBM Corp.'s Thomas J. Watson Research Center have achieved gate delays on the order of 13 ps. However, Josephson circuits require cryogenic cooling to work.

At Rockwell International Corp.'s Electronics Research Center, engineers are concentrating on a low-dissipation, planar MES FET process involving multiple localized ion implantations. Recently fabricated ICs include a ring oscillator with 62-ps gate delays, says Richard C. Eden, principal scientist at the Thousand

Ovshinsky, A. B. Dick form joint venture

Stanford R. Ovshinsky's Energy Conversion Devices Inc., Troy, Mich., and A. B. Dick Co., Chicago, Ill., have formed a joint venture to make updatable microfiche systems that use the former's amorphous films. The A. B. Dick–MicroOvonics Inc. desktop imaging and verifying systems will use ECD's instant dry-process microimaging film. Ovshinsky had an earlier joint venture on the same technology with the 3M Co., which subsequently withdrew its support.

The agreement calls for Ovshinsky's company to supply the technology to the new company, which will do the manufacturing, says Ned Kight, executive vice president of A. B. Dick. He would not specify the investment involved beyond characterizing it as multimillion-dollar.

"Unlike 3M's arrangement, in which it was simply a distributor of the microfiche machines, ours is more involved, since we have a joint interest with ECD," Kight says. A 3M spokesman says it terminated its agreement with the Ovshinsky company last September because the machines did not meet specifications. However, an Energy Conversion Devices spokesman retorts that the machines did meet specifications.

In photovoltaics, ECD has a $25 million research-and-development pact with Atlantic Richfield Co. for amorphous solar cells [*Electronics*, Jan. 31, p. 40], and that agreement follows an earlier arrangement with United Nuclear Corp., which now is suing on the grounds that it has 50% of the rights to proceeds of ECD's solar-cell research. It has included Arco Solar Inc., Atlantic-Richfield's subsidiary, in at least one of its three suits, which are in the early pretrial stages.

-Roger Allan

Oaks, Calif., research facility.

The 1-μm geometries were fabricated with optical lithography and step-and-repeat projection masks. The center's largest circuit so far is a 5-by-5 parallel multiplier with 260 gates and delays of 150 ps.

"Some initial memory devices are in process," Eden says. Rockwell plans "to start development later this year of a 4-K static RAM that should be able to achieve access times of from 1 to 2 ns."

Soon. By 1985, predicts D. Howard Philips, manager of Lockheed's Microelectronics center, GaAs logic ICs should achieve 4-GHz or better speeds, nearly a tenfold advantage over what is being forecast for ECL and complementary-MOS-on-sapphire chips. He also predicts that discrete GaAs FETs will be showing similar speed advantages—40 versus 4 GHz—over their best silicon rivals, having already demonstrated twice the cutoff frequency—12.7 GHz.

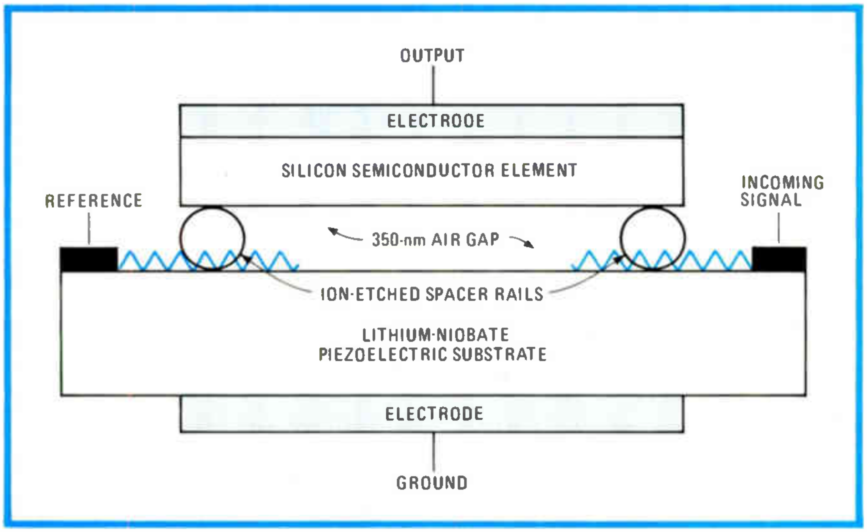
The impetus for the Lockheed work is the expected hike in data-transmission rates from space. By 1986, the down-link data load will jump an order of magnitude or more from the present 10^{15} bits per year, Phillips says.

What's more, the National Space and Aeronautics Administration "projects that by the end of the decade the down-link data load will increase by more than a factor of 10,000," he adds. The 1-gigabit-per-second data rate achieved by the fastest present silicon ICs "is about the best that can be expected" from them, Phillips says. **-Bruce LeBoss**

Military

SAW filter can track fast coding changes

Spread-spectrum communications systems, long used by the military for their resistance to jamming, may become even more resistant to it, thanks to a surface-acoustic-wave filter capable of processing rapidly changing waveforms in real time. Unlike conventional SAW matched filters, whose signal-matching references are fixed patterns etched on their substrates, the new SAW part uses as a reference a time-reversed waveform corresponding to the incoming signal.



Decoding. The programmable SAW convolver integrates acoustic waves derived from incoming and reference signals, giving a real-time decoded output.

Thus a receiving operator can program the system with appropriate reference signals to accommodate bit-to-bit changes in waveform encoding. That capability is good news: even though spread-spectrum techniques force a noise-jamming system to spread its available power over a wide bandwidth, thus decreasing the spectral power density that makes its interference effective, any signal waveforms that are constant or change predictably can still be matched in frequency by more sophisticated jamming.

Till now, the only means of equipping a communications system to accommodate fast, random changes of waveform encoding has been the correlator, which must search blindly for incoming signals. But the synchronization problems make it too slow to handle very short, burst-type military messages.

So coupling the speed of matched filters for real-time signal processing with the programmability of the correlator produces a real advantage, says John H. Cafarella, assistant group leader at the Massachusetts Institute of Technology's Lincoln Laboratory, where the new part was developed. It would take "a deskful of electronics" performing 10^{11} mathematical operations per second to achieve the same functions, he remarks.

For signal processing, the part uses a technique called convolution, as do conventional matched filters. That is, its impulse response is the time reverse of the waveform to be received. This response is produced whenever the signal arrives, eliminating the search time required by correlators.

Varying response. Where ordinary filters' hardware limits their response to one waveform pattern, the response of the SAW convolver can vary each time a new reference is applied. A suitably programmed waveform generator supplies the varying references.

One version of the new part couples a piezoelectric substrate with a semiconductor across a narrow air gap (see figure). It converts both incoming signal and reference into acoustic waves, which propagate past each other from opposite ends of the piezoelectric substrate.

Electrical fields accompanying the wave interact with free electrons in the semiconductor. The semiconductor spatially integrates the products resulting from its nonlinearity, giving an output that represents the convolution of the two acoustic waves shifting past one another. Lincoln Lab reports a processing gain of 34 decibels and a dynamic range of 46 dB for 200-megahertz bands.

Somewhat lower performance coupled with lower production costs than the acoustoelectric version may come in an alternative, monolithic structure. It uses a piezoelectric substrate only.

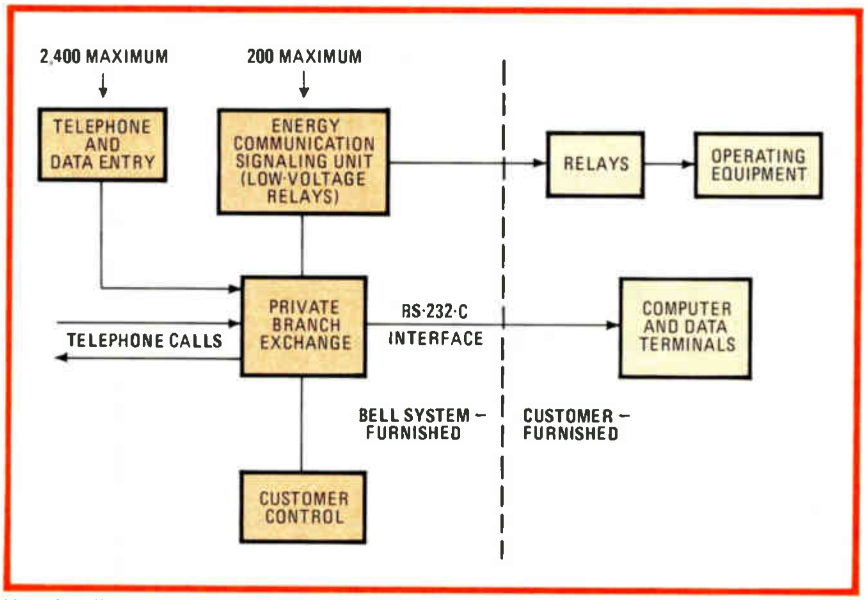
Elastic. This elastic version, as it is called, creates a different kind of nonlinear interaction, involving the strain waves produced in the substrate by the acoustic waves propagating past one another. A deposited electrode running the length of the substrate picks up and integrates the products from the strain interaction.

The elastic SAW convolver has been tough to develop because strain-wave interactions are much weaker than acoustoelectric ones, but it can compensate for that problem by compressing the acoustic-wave beams to produce higher power densities. First engineered in 1974 by Thomson-CSF in France, it is now under development at the Lincoln Lab, in Lexington, Mass., and at Andersen Laboratories Inc., a Bloomfield, Conn., custom house.

Andersen plans to deliver prototype models under a military contract in the next six months. Vice president Thomas Martin estimates eventual production costs could be under $100 each. **-Linda Lowe**

Communications

Bell PBX snuggles up to computers



Very intelligent PBX. Bell's new Dimension 2000 PBX can handle data entry for a computer from 2,400 handsets and energy management at the same time.

Added features are making Bell System equipment look more and more like small computers. A prime example is a new private branch exchange aimed at controlling hospital energy-management and data-entry functions, as well as routine voice communications.

The telecommunications giant will not make the claim that the new Dimension 2000 is either data-communications or computer gear. But the features added put the PBX unit right next door to such hardware.

The user may program the relays, the hospital's computer connected to the Dimension 2000 by means of an RS-232-C interface. In this way the PBX acts as a data-entry terminal in a computer network. It can interface with a total of 2,400 telephone handsets, Bell says.

Expansion. The new Dimension 2000 provides some of the features that would be needed once Bell's long-awaited data-communications network, the Advanced Communications System, comes on the market. However, Schindler is not ready to say that this PBX will positively play a part in such a scheme.

"As part of an integrated strategy, it always behooves one to look at a product's answering of customer needs in the form of network and on-premise capabilities, with a view toward making sure that there is integration," he says.

The new offering is controlled by a microprocessor Bell designed for the Dimension family and contains 448 kilowords of random-access memory. Four 16-K RAM chips bought from an outside vendor have been added to the original Dimension 2000 to handle the added functions. No added read-only memory was required, although some manipulation of the software resident in ROM was needed.

High on the list of pluses touted by American Telephone Telegraph Co. is the energy-communications signaling unit that interfaces with the PBX. As many as 200 of these devices may be attached (see figure) to provide interconnections for turning lights on and off, opening and closing doors, or performing any other task under a relay control that is driven by a low-voltage signal put out by the unit.

The unit's relays put out 24 volts at 2 amperes and can switch up to 240 V. The customer adds all sensors or other attachments that connect with these relays.

"There's an interface between the customer's air-conditioning unit or what-have-you and the Dimension PBX. So all we do is to turn it on or off. What the user wants to do beyond that is up to him," observes Gary N. Schindler, AT&T marketing manager for the health care and lodging industries, Morris Plains, N. J.

Data entry. Another feature helping to turn the Dimension 2000 into a computerlike unit is the ability to enter data over a Touch-Tone telephone set. Such information as the number of empty beds or a patient's status may be keyed into the system from any designated handset's keypad in the network.

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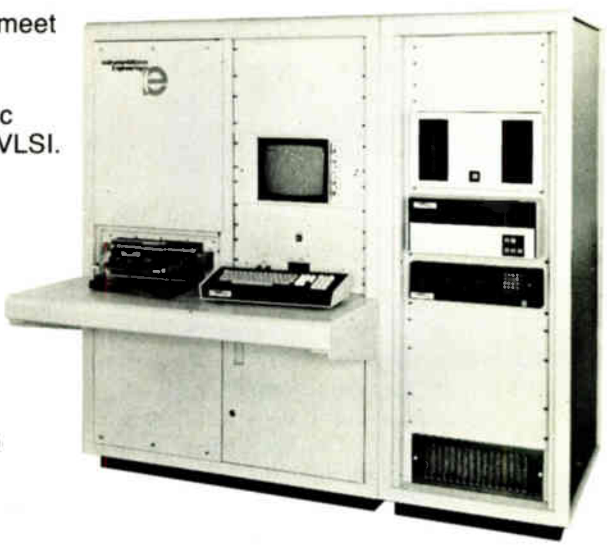

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each handset's access number, and restrictions placed on specific lines via what Bell calls a customer-administration panel ("customer control" in figure). This makes changing telephone numbers or relay controls in the system a matter of pushing a few buttons with no need for extensive rewiring by Bell.

Obviously the Dimension 2000 will have applications outside the hospital environment. Other possibilities include offices and manufacturing facilities, although Schindler is not ready to speculate on exact markets, or the pricing of specific configurations. -Harvey J. Hindin and Pamela Hamilton

Consumer

Bell, Knight-Ridder launch viewdata test

Compared with its English, French, and Canadian counterparts, American Telephone & Telegraph Co. comes late to the electronic home-information game. But having quietly laid the groundwork, Bell is joining with Knight-Ridder Newspapers Inc. to test a viewdata system, sending data over telephone lines.

The two companies are heralding their announced Coral Gables, Fla., test setup as a true home-information system, even though it is limited in scope. News, information, and in-home shopping will be offered to 160 selected homes for the next six months. The lucky viewers will be treated to some 15,000 pages of information.

Phone lines. With no sound and freeze-frame graphics only, the transmissions can be sent over regular telephone lines without bandwidth problems. The viewers see the output on special TV receivers, calling up pages with a control unit.

AT&T hopes such tests will lead to telephone lines, rather than television signals, playing the major role in home video-information systems. It has had a previous viewdata test trial for the deaf in New York and another continues in Albany, N. Y., for what is billed as an electronic telephone directory. The latter system actually gives customers access to Bell computers for weather, time, and sports updates, plus directory information [*Electronics*, Sept. 13, 1979, p. 40].

Others. Great Britain's Prestel system has been extensively tested for some years now and has gone through several versions. It is available commercially, offering some 150,000 pages of information, and is licensed in the U. S. by General Telephone & Electronics Corp. Another English invention was a similar system called teletext that sends the data over the air during the blanking interval of television signals.

The Bell tests are not the only effort in the U. S. The French teletext system, Antiope, has undergone tests in St. Louis (vying with the British version) and Los Angeles. In France, a viewdata and teletext experiment involving 3,000 households is scheduled to start at the end of the year near Paris.

Finally, the Canadian Department of Communications has the Telidon system, with technology claimed to be the most advanced and distinct from other viewdata and teletext approaches [*Electronics*, April 10, p. 44]. U. S. and Venezuelan tests were set recently, and extensive testing has already been undertaken in Canada.

For all these systems, the problem has been to decide what kind of services to offer at a price that consumers are willing to pay. This is no small feat, as the pages of information are often available from other sources, such as the daily newspaper.

Now operational, the Bell-Knight-Ridder system, Viewtron, is interactive in that the user has a keypad to order goods and electronic banking services. Self-instruction features and games will also be available.

Very special. Viewtron is not readily transferable to the mass market, since the home TV set needs an interface that is not currently in production. The sets being used for the test cannot receive regular broadcasts, a move that ensures that the research data will be unaffected by other variables. Also, dedicated phone lines will handle the information transfer, although the system could share the existing lines.

It is, however, no problem to build a dual-function TV receiver. It is also possible to produce an adapter for conventional TV sets.

For now, the test merely shows Bell's commitment to the concept of phone-based video-information systems. In the limited trial, pricing is not a consideration, since the equipment and service are furnished free of charge. The kind of setup—and the price structure—that would be offered to a large-scale market are still unknown. -Harvey J. Hindin

Medicine

Smart gamma unit forms images faster

Designers at the Israeli medical electronics manufacturer Elscint Ltd. have combined the sensing and computational functions of a gamma camera system so that its operation is refined by the computer's input. They have modified the electronic architecture of the firm's computerized-axial-tomographic scanners to serve in the new Apex gamma camera, giving radically faster and more accurate heart examinations.

Gamma cameras form images of internal organs by sensing gamma radiation from a patient injected with a radioactive isotope. In older systems, a minicomputer constructs a black and white TV image based on the number of emissions, or counts, that occur within a given area.

Apex's integrated setup, which uses four microprocessors, automatically measures the nonuniformity and nonlinearity of the sensor and corrects images on the fly, thus improving sensor resolution while maintaining a high count rate. What's more, the various models cost between $90,000 and $200,000, whereas the older setups can cost as much as $300,000 for the camera plus $200,000 for the minicomputer.

The design uses four tightly cou-

SCIENCE/SCOPE

Ultra high-speed satellite communications are closer to reality with the development of unique pseudo-random code generators. The hybrid circuits, which operate at more than 1 billion bits per second, were built with gallium-arsenide field-effect logic. They demonstrate that the problems of making such chips -- problems including layout, construction, die and wirebonding, and chip handling -- can be solved. Researchers at Hughes will use the chips as signal sources for gigabit logic experiments.

The unique method for ejecting Leasat satellites from the cargo bay of NASA's Space Shuttle -- a process that has been likened to flipping a flying disk -- has been proven in simulation tests. In a test designed to imitate the zero gravity of space, small explosive charges were fired to release a mock spacecraft weighing 15,000 pounds and measuring 14 feet in diameter. The simulated craft, hung from a 70-foot cable attached to a low-friction trolley, cleared its cradle and the bay as expected. Hughes is building five Leasat satellites to fill the communications needs of the U.S. Navy and other armed services. The spacecraft are to be launched aboard the Space Shuttle into low orbit, then released and boosted into synchronous orbit 22,300 miles above the earth.

Designers of computer software systems can expect help from other computers in the near future. A computer aid being developed by Hughes serves as draftsman, librarian, and report writer of a design session. The system, appropriately called AIDES (for Automated Interactive Design and Evaluation System), converses with the designer in near English and draws charts on TV-like terminals and plotters. It also analyzes designs for soundness and testability. AIDES reduces the labor intensity associated with software design, while improving consistency and overall quality. Studies indicate the system trims design time by 30 percent and slashes costs for structure chart documentation by 95 percent.

Hughes is seeking engineers to develop advanced systems and components for such weather and communications satellites as GOES D, E, and F, Anik C, GMS II, Leasat, SBS, Westar IV, and Palapa B. Immediate openings exist in advanced communications, scientific and engineering programming, systems test and evaluation, microwave and RF design, power system design, spacecraft alignment, thermal and vibration test, and reliability and quality assurance. Please send your resume to Tom W. Royston, Dept. SE, Hughes Space & Communications Group, P.O. Box 92919, Los Angeles, CA 90009. Equal opportunity M/F/HC.

Better ways to help pilots visualize the performance characteristics of their weapons, particularly during the stress of combat, should reduce the chance of missiles being fired in such instances as when the aircraft is in the wrong attitude or the target too far away. Hughes, under U.S. Air Force sponsorship, is evaluating new display techniques and algorithms (data processing formulas) for fire control systems. After these concepts have been analyzed in ground simulations, the best will be demonstrated in flight tests in an F-15 fighter.

Creating a new world with electronics

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pled microprocessors. The main central processing unit, a 16-bit 8086, does the system's number crunching while two other Intel processors, an 8085 and an 8089, manage the system memory.

The 8-bit 8085 takes care of the slower permanent storage—a 1.2-megabyte floppy-disk drive, which can be used for individual patient workups, and up to eight 15-megabyte hard disks, which provide program and on-line archival storage. The 8089, an input/output peripheral processor that is a member of the 8086 family, provides fast access to the system's 545-kilobyte semiconductor memory in which the corrected image data is initially stored.

Corrections are done on the fly on incoming data by an Advanced Micro Devices Am2901 bit-slice processor. Data from the sensor-photomultiplier tube in the camera is first digitized by a 12-megahertz analog-to-digital converter with 9-bit precision and fed to the 2901, which applies the corrections generated during the system's latest self-calibration round.

Apex's camera uses a single crystal, an approach that in other systems gives good resolution but poor speed. However, the digital integration gives a maximum speed of 500,000 counts per second, equivalent to that obtained by multicrystal cameras, but without the latter's poor resolution. Apex achieves a resolution of 1.8 millimeters in its small-field model, the equivalent of the older, much slower models. Nonlinearity is 0.1% and nonuniformity is 2%; in a typical single-crystal camera, nonlinearity is 2% and nonuniformity ranges from 8% to 15%.

Two studies. The combination of high speed and good resolution makes feasible first-pass examinations, in which the images are obtained when the isotope passes through the heart for the first time. It may also be used for multigated studies, in which counts taken during a number of cardiac cycles are stored in memory and analyzed to produce succeeding frames in a kinetic picture of the heart's action.

Older systems typically have been multigated, because their high-resolution single-crystal cameras have not been able to achieve the high count rates necessary for single-pass studies. Of course, Apex speeds up multigated studies, taking several minutes to form the image whereas older systems need 10 to 20 minutes.

For Elscint, the system represents a move towards greater emphasis on high-technology medical products. Later this year, the company plans to introduce an ultrasonic body scanner, based on the CAT scanner technology. It also plans word-processing packages that can be used for semiautomatic production of medical reports. **-Richard W. Comerford**

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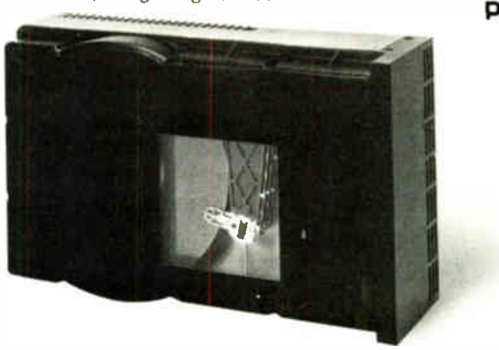

Washington newsletter

Alarmed ITU protests FCC desire to see private lines shared

A unanimous Federal Communications Commission decided last April that corporations ought to be allowed to share the private lines they rely on to conduct their business overseas or to resell unneeded communications capacity. But other countries believe the FCC has overstepped its bounds: a strong letter to the U. S. State Department from the world agency responsible for coordinating international communications policies **claims the commission is violating international guidelines against reselling and sharing that the U. S. agreed to four years ago.** Leon Burtz, a key official in the 154-nation International Telecommunications Union, expressed his "surprise" and "deep disappointment" at the FCC's action and asks the State Department to persuade the FCC to reconsider.

FCC stumped over choice of quadraphonic system

The Federal Communications Commission would like to approve a new quadraphonic broadcasting system for fm radio stations but is unsure how to go about selecting a standard. **The commission has decided unanimously not to determine what kind of standard should be adopted for quadraphonic broadcasting.** Several companies, including RCA, CBS, Zenith Radio Corp., Quadracast Systems Inc., and General Electric, have designed systems. But for the most part they are incompatible. The FCC has decided to ask the public to comment on whether a specific system should be selected or a general standard adopted with the marketplace free to choose the system to be used. If the public persuades the FCC to choose a specific design, the commission indicates it would favor those proposed by RCA and Quadracast, which are compatible.

Communications bill should be delayed, Rodino maintains

Rep. Peter W. Rodino Jr. (D., N. J.) and the House Judiciary Committee he heads believe Congress should hold off on H. R. 6121, the communications legislation that would restructure the industry, until the U. S. government's antitrust case against American Telephone & Telegraph Co. is resolved. In a letter to the chief sponsor of a bill in the House that would revise the Communications Act of 1934 by changing the rules under which AT&T does business, Rodino suggests that legislative intervention in the industry when the trial is to begin in October "is, at best, highly unusual." The Congressman told Rep. Lionel Van Deerlin (D., Calif.) that he will not support the bill if it lifts AT&T's 1956 consent decree with the Justice Department **and allows the telephone company to get into data processing through a separate subsidiary.**

U. S. accuses Belgian of acting for USSR in source-code deal

Now that the State Department is keeping tighter control on high-technology items that had been finding their way to the Soviet Union through third parties, **the USSR allegedly has been trying other means to acquire the classified technology and equipment.** In one case, a Belgian businessman is awaiting Federal court trial in Washington, D. C., after being charged with an attempt to buy the source code for a military data-management software system from an undercover agent of the Federal Bureau of Investigation. The system—dubbed Adabas—was developed by Software AG of North America in Reston, Va., and is used at 700 installations around the country by banks, oil companies, and state governments, as well as the military. Adabas, which anyone may purchase for $160,000, runs on IBM, Siemens, and Digital Equipment computers. But the source code is not sold by Software AG to anyone.

Washington commentary

Some tax cuts for technology?

Congressional Democrats have caught tax-cut fever from their Republican counterparts ever since GOP Presidential nominee Ronald Reagan proposed at the end of June a $35.8 billion tax-reduction program. As a result, both parties are pushing proposals of nearly every description to attract votes in November. Not many of these tax-cut plans can be called practical solutions to the fiscal problems of the U. S., however. The idea of a 10% across-the-board cut being promoted in the Senate by Kansas Republican Robert Dole is maybe the most simplistic.

Although a general reduction in taxes has broad political appeal, it would only compound the huge increases in the Federal budget deficits just predicted for this fiscal year and next by President Carter. In its revised economic forecast to Congress, the White House estimates that the fiscal 1980 deficit will hit $60 billion—a 64% jump from the March projection of $36.5 billion—without a tax cut. The March forecast of a $16.5 billion surplus in fiscal 1981 has now become a deficit of almost $30 billion. And that deficit could climb by another $10 billion with the enactment of a $25 billion tax cut to become effective in calendar 1981.

Though tax cuts may only aggravate these dismal figures, there are some sensible long-term solutions now pending before Congress that can stimulate American competitiveness in the world's markets. Four programs being pushed vigorously by the American Electronics Association deserve attention.

Giving credit for R&D

One is S. 2906 just introduced by Senators Bill Bradley (D., N. J.) and John C. Danforth (R., Mo.). Called the "Research & Development Act of 1980," it would allow a 25% tax credit for corporate increases in new R&D that exceed a company's average outlay for the three previous years. Originally drafted by an AEA task force of leaders from 13 member companies, the Bradley-Danforth bill would adopt the Financial Accounting Standards Board definition of R&D long used in industry but would exempt from credit all R&D contracts and subcontracts funded by Federal, state, or local governments.

Startup companies would operate on a three-year base of zero spending in their first year and could carry forward unused tax credits for seven years. AEA is driving hard, but prospects for passage of S. 2906 in the time remaining seem dim because of its late introduction and the fact that it lacks counterpart legislation in the House. Moreover, it may face trouble with its exclusion of credits for R&D in the social sciences or the humanities.

Another valuable and equally promising bill is the "Research Revitalization Act of 1980" introduced as H. R. 6632 by Rep. Charles A. Vanik (D., Ohio), which already has six cosponsors, and as S. 2355 by Sen. Paul E. Tsongas (D., Mass.). The Vanik-Tsongas bill would permit a 25% tax credit for corporate contributions for research to colleges and universities. Funds placed in corporate reserves for this purpose would have to be spent within four years or be subject to a 300% tax—a definite discouragement to tax dodgers. In these bills, AEA sees three principal benefits: a reorientation of academic programs and facilities away from "red-tape–laden Federal sponsorship" toward programs to assist industrial innovation and productivity directly; an urgently needed increase in the supply of technical graduates; and approval for groups of companies in one or several industries to sponsor joint programs.

Stock options and capital gains

The two remaining tax-cut proposals deal with longer-standing issues and are more financially oriented. The first is H. R. 5060, the "Employee's Incentive Ownership Act" sponsored by Rep. James R. Jones (D., Okla.) and its companion Senate bill, S. 2239, sponsored by Sen. Bob Packwood (R., Ore.). This bill would restore the restricted stock option as a means of employee-incentive compensation. With 23 pledged votes in the House and 9 in the Senate, it is the most likely to become law this year.

The second bill, S. 2293, sponsored by Sen. Alan Cranston (D., Cal.), would reduce the maximum capital gains tax from 28% to 21%—an action that AEA contends would attract more risk capital to the capital-hungry electronics industries. While AEA is convinced that the bill can pass, the association overlooks the apparent impossibility of getting similar legislation introduced and passed in the House, where it is viewed as a bill that would do little more than help the rich get richer.

Three possible enactments out of four programs is not bad. The 25% tax credits for new corporate R&D and academic research grants may not be the best-known bills now in the Congressional hopper, but they might just make it with more widespread support. With today's technological competition with Europe and Japan, they should not be made to wait until next year.

-Ray Connolly

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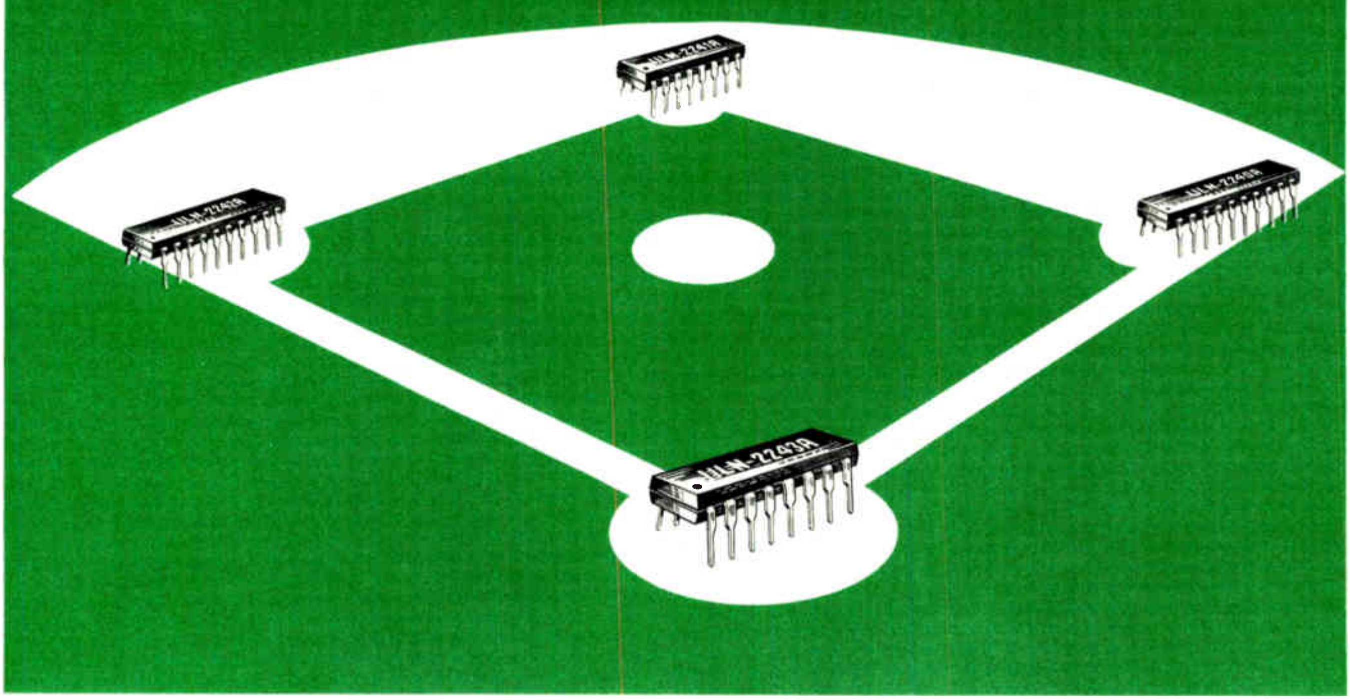

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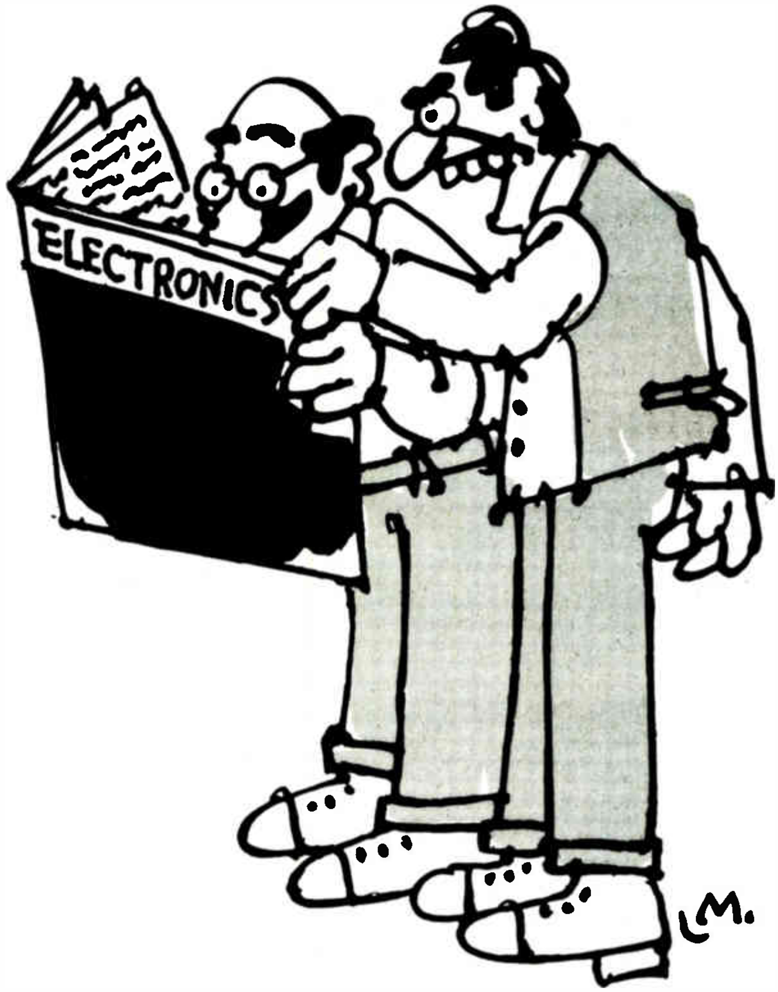

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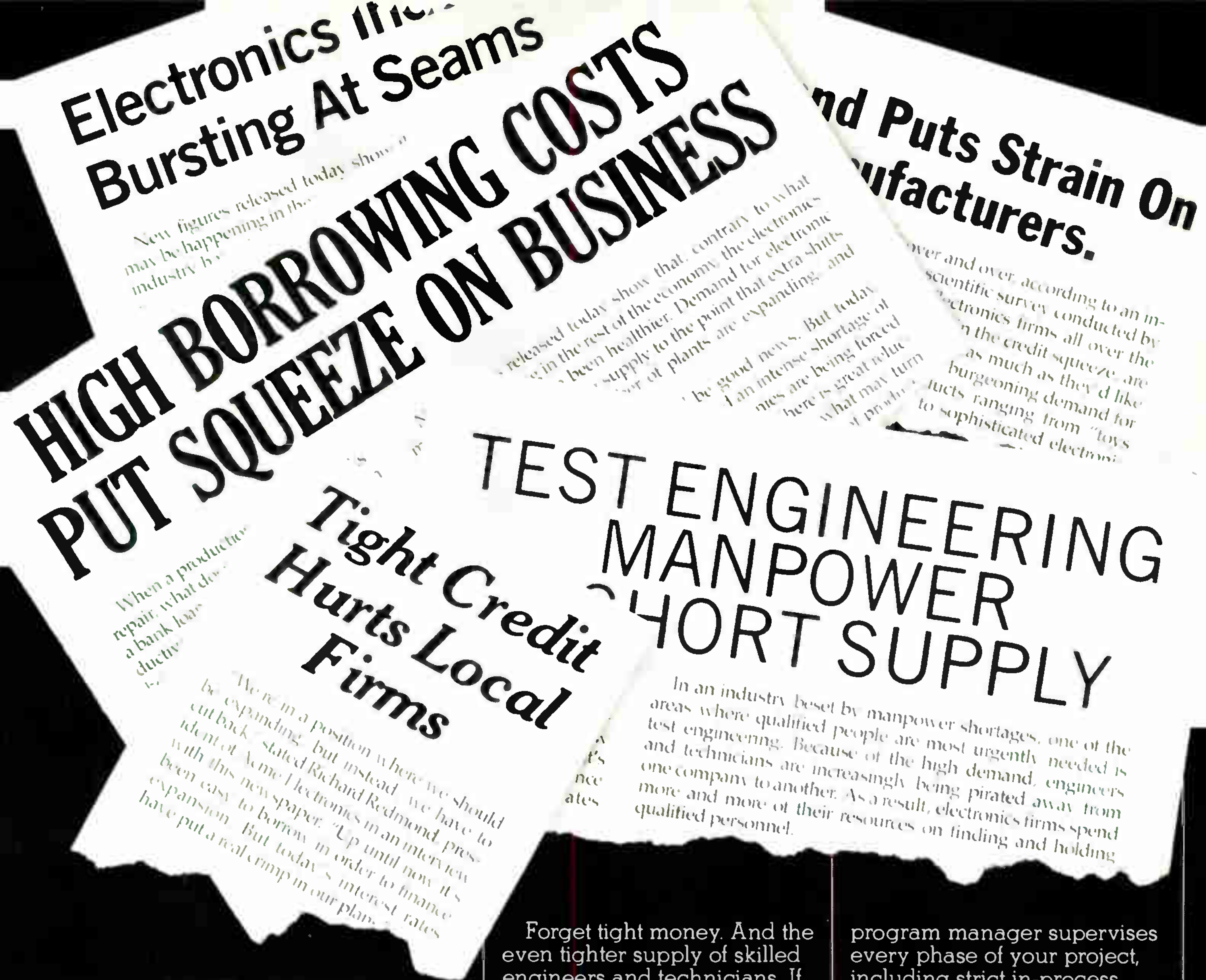

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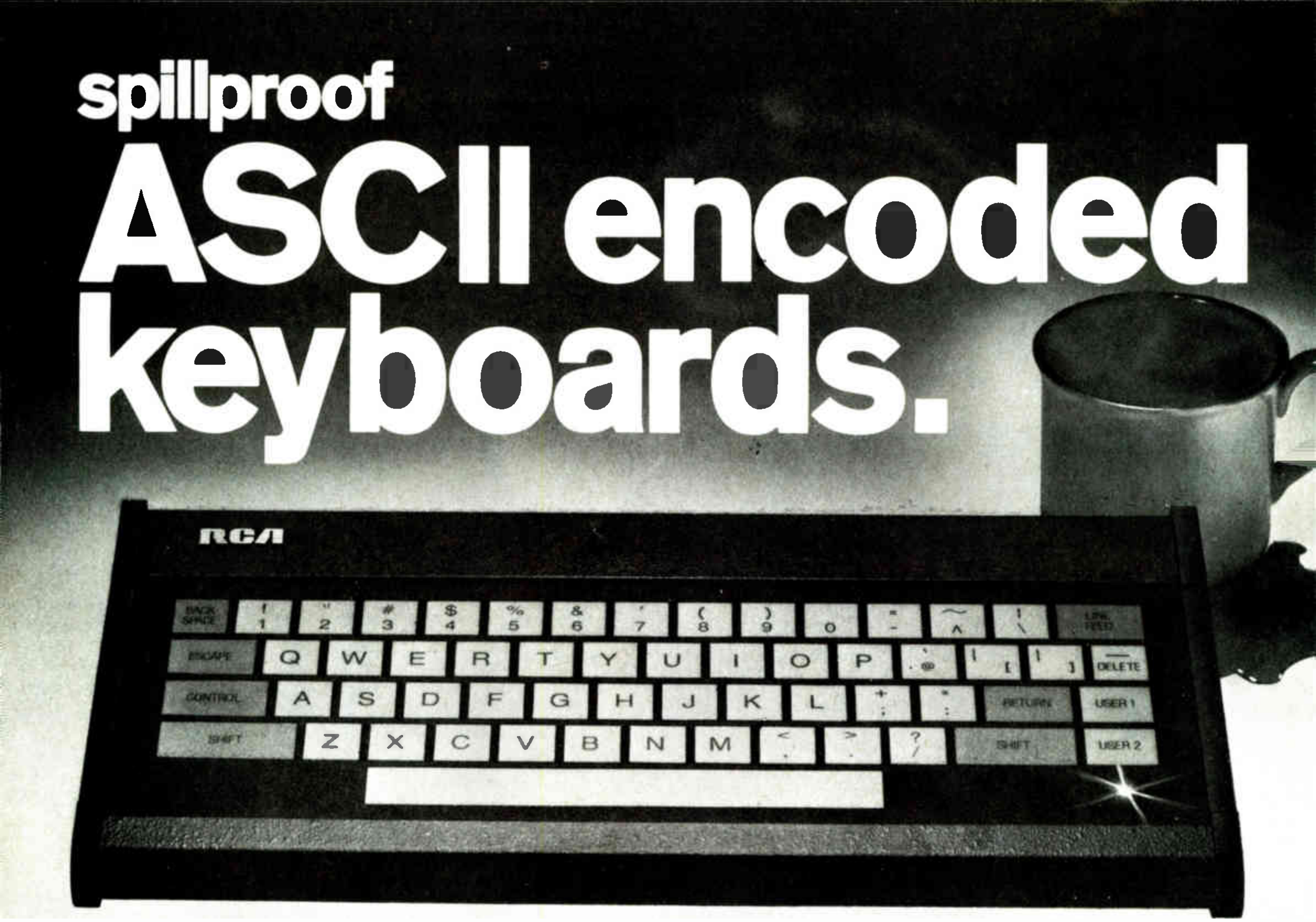

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RCA

International newsletter

French electronic payment cards to get three-city trial

In conjunction with 10 French banks, CII-Honeywell Bull, Philips Data Systems France, and the Flonic division of Schlumberger Ltd. will equip three French cities with experimental off-line payment card systems by 1982. The CII-HB and Philips cards contain 8-bit microprocessors coupled with 4,096 bits of programmable read-only MOS memory, though both firms are planning to put a single custom chip on later versions of their cards; the Schlumberger card is simpler, as it includes several dozen logic gates rather than a microprocessor [*Electronics*, Jan. 17, p. 68]. Although the banks jointly conducting the experiment have yet to let out contracts, **each manufacturer is expected to provide upwards of 50,000 cards and 100 point-of-sale terminals.**

Siemens to deliver power MOS FETs with 800-V breakdown voltage

West Germany's Siemens AG is now starting deliveries of high-voltage power MOS field-effect transistors with a breakdown voltage of more than 500 V. Designated BUZ 44, the devices feature a turn-on resistance of less than 1.1 Ω. To follow in August is the BUZ 83, also a power MOS FET, with **a breakdown voltage of better than 800 V and a turn-on resistance of less than 2.6 Ω.** The two parts belong to a components family that the Munich-based company announced as Sipmos (for Siemens power MOS) devices earlier this year [*Electronics*, Feb. 18, p. 63, and March 13, p. 92].

Thin-film transistors radically simplify matrix displays

Polycrystalline thin-film MOS transistors fabricated on a glass substrate are expected to decrease the number of pins needed in liquid-crystal and other matrix displays by as much as 100 times. Furthermore, fabricating the switching and drive circuits directly on the periphery of the display **eliminates the parallel leads to the pins, enhancing contrast by greatly reducing crosstalk.** In preliminary work, the Central Research Laboratory of Hitachi Ltd. deposited by molecular-beam epitaxy a 1-mm-thick film of silicon with crystalline grains about 100 to 200 mm in diameter. Transistors are fabricated using low-temperature chemical vapor deposition of silicon dioxide for the gate insulator. Channel length (in the direction of current flow) is 20 mm; channel width is 2 mm. The early devices have an on-off resistance ratio of 4. When operated with a drain voltage of 30 V and a gate voltage of 10 V, drain current is 20 mA. The minimum pulse width is on the order of 200 ns, sufficient for small displays.

Swiss set time for launching TV satellite

In a report to the Swiss government, the country's postal and telecommunications authority says it is ready to be responsible for constructing and operating a communications satellite. In outline, the plan resembles the proposals of Tel-Sat, a private group of publishers and media agencies that two months ago announced its intention of seeking governmental permission to run a television satellite service in the frequency band assigned to Switzerland at the 1977 Geneva Convention. Since then, **a government commission of media experts has ruled that satellite communications should not be a private interest,** and this ruling, together with the report, seems to have shot down most of Tel-Sat's hopes, except that it or its members could eventually be involved in the TV programming.

A favorable decision seems likely by year's end, and the satellite could begin broadcasting in the mid-1980s.

International newsletter

EC plans to get into VLSI production gear, telecomm standards

Anxious about the lead opened up by the U. S. and Japan in integrated-circuit technology and concerned as well about the evolution of advanced telecommunications networks among its nine member nations, the Commission of the European Community has blocked out a pair of five-year action plans that it hopes the EC's decision-making Council of Ministers will put into force by the end of the year. The first aims mainly to **foster development of production equipment for submicrometer-feature ICs in Europe.** The commission figures a competitive European industry could do $1 billion of business over five years in microlithographic and related machines. The second plan would ensure common standards for truly international digital telecommunications services. It also calls on the government-run telecommunications networks to open up 10% of their equipment procurement to EC-wide competition starting in 1983.

Britain to loosen post office's monopoly of telecommunications

Legislation about to be introduced by the British government will liberalize the telecommunications monopoly of the post office by empowering private companies to compete with it in offering would-be users telephones and other terminal equipment. Responsibility for supplying the first telephone and maintaining private automatic branch exchanges will remain with British Telecom, the post office's telecommunications wing that itself may shortly be legislated into independence of the mail services. To safeguard British companies after a three-year transitional period, **import licenses will require the importer's home market to be accessible to British companies**—a move that would hit Japanese but not U.S. firms.

In addition, the private sector will be able to provide value-added network services not currently available from British Telecom, and this may be extended to complete liberalization of such services as electronic office facilities. The government is also reviewing the private provision of telecommunications services such as a satellite business system.

Jerusalem to be site of Intel's first overseas IC plant

Intel Corp. has selected Jerusalem as the site for its first overseas wafer fabrication facility. Israelis now expect that a deal involving **a plant costing several tens of millions of dollars,** with hefty incentives in the form of government loans and grants, will be signed by September. Intel already has an integrated-circuit design center in Israel, at Haifa, and will expand that as well as part of its upcoming Israeli investment.

Addenda

For the first time, **Japan's exports of integrated circuits to the U. S. exceeded its imports from the U. S. during the first half of this year,** according to statistics just out from the country's Ministry of Finance. Compared with the first half of 1979, Japanese exports to the U. S. rose by 160.2% to $175.85 million, while imports from the U. S. about held their level at $155.12 million.Partly responsible was a great shortage of devices in the U. S. . . . Gallium-arsenide dual-gate metal-semiconductor field-effect transistors are now being used in a Japanese ultrahigh-frequency TV tuner and will probably be used in export sets next year. Use of the new transistors should enable Matsushita Electrical Industrial Co. to meet the Federal Communications Commission noise figure regulation scheduled to go into effect in 1982. The 3SK97 has a noise figure of 1.3 dB and a typical gain of 17 dB, both measured at 1 GHz. For the best dual-gate silicon devices, comparable figures are 3.5 to 4 dB and 12 to 14 dB.

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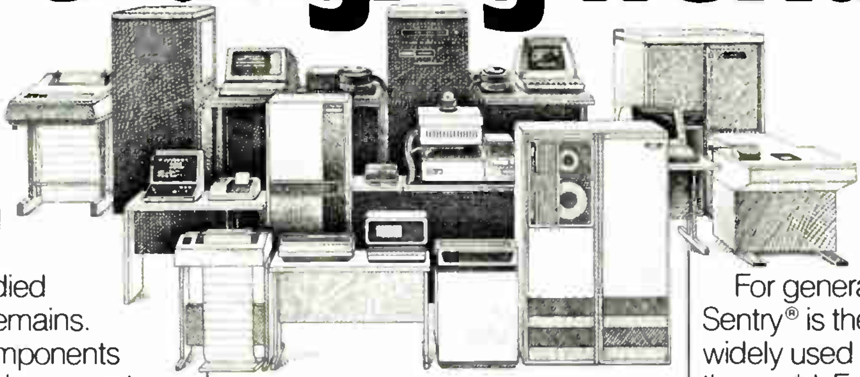

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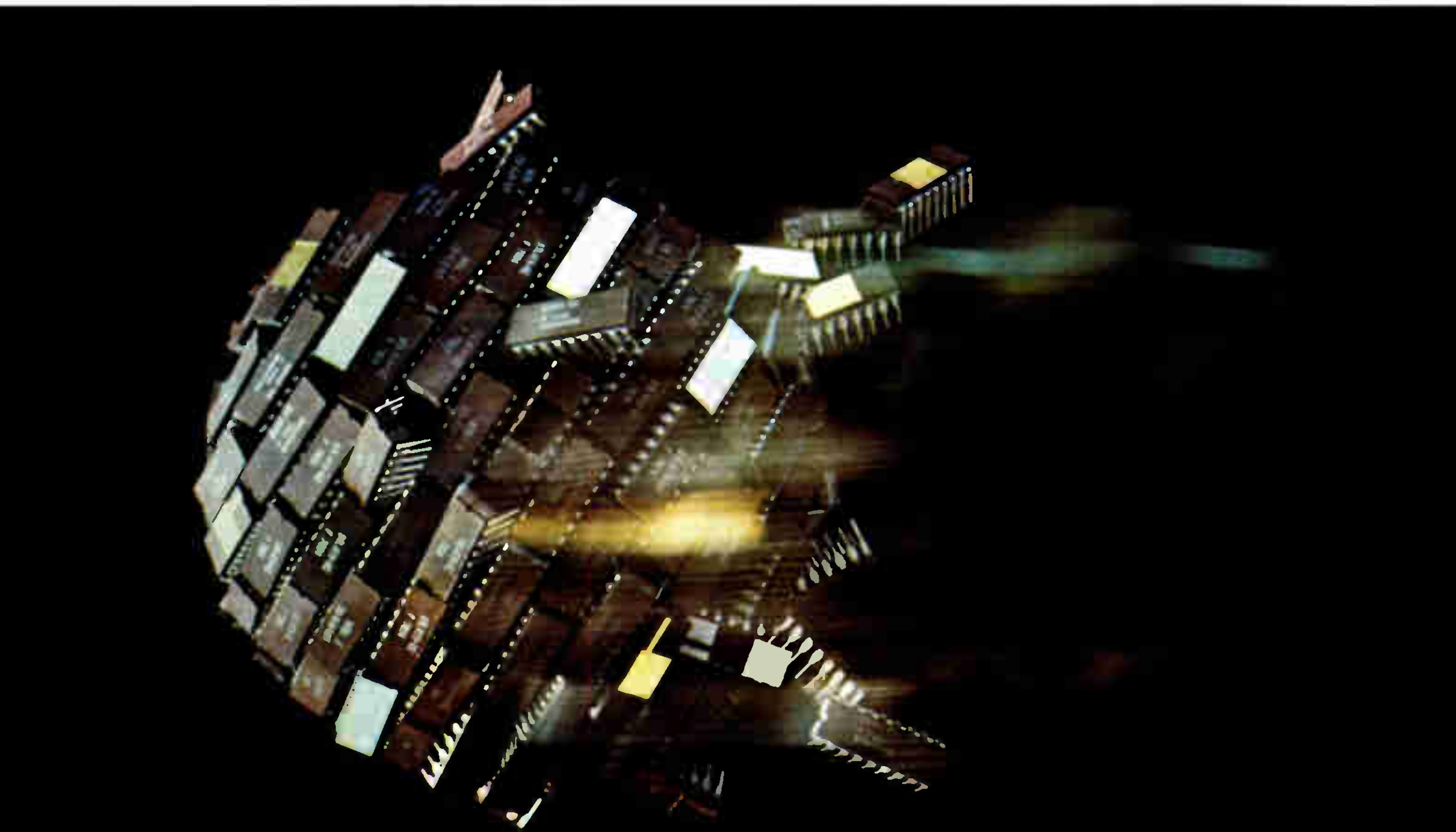

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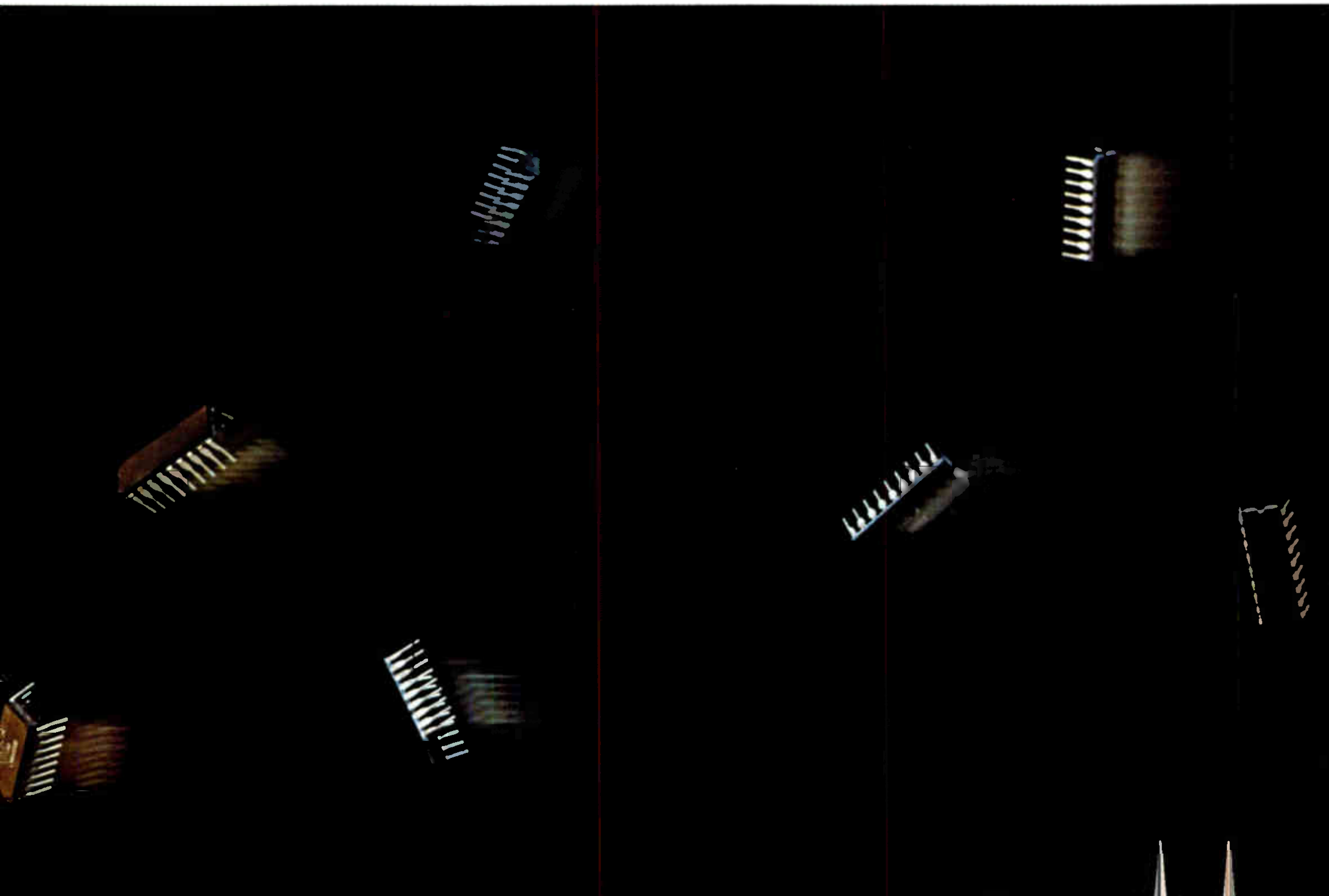

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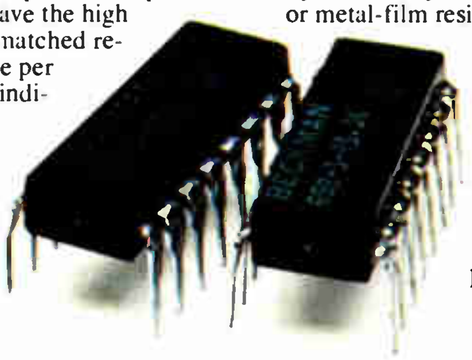

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Electron beam harmlessly probes high-density chips

by John Gosch, Frankfurt bureau manager

Beam diameter could easily be reduced to 0.1 micrometer to test 1-μm-wide features

An electron-beam test system at Siemens AG's Components Group is routinely measuring the voltage waveforms of large-scale and very large-scale integrated circuits—a parameter that till now has been difficult or even impossible to check. Intended initially only for in-house use, the system was developed by the scanning electron microscopy section of the Munich company's central laboratory. According to industry sources, both IBM Corp. and Intel Corp. are experimenting with similar systems.

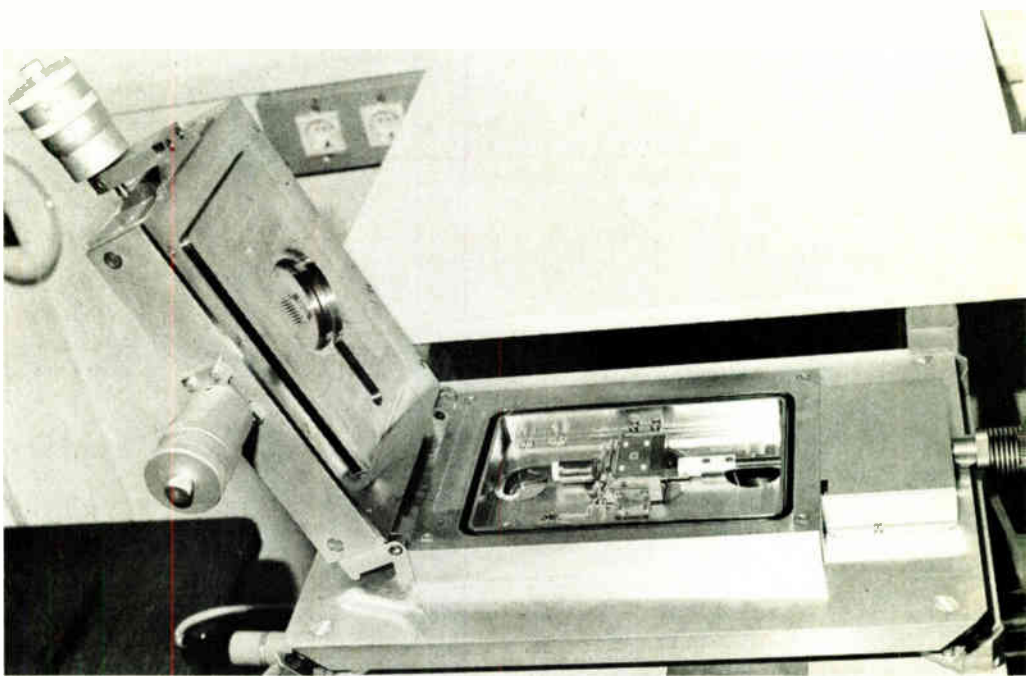
In the new equipment, the electron beam functions as a test probe. As such, according to Eckard Wolfgang and his section associates, it is superior to its mechanical counterpart in conventional IC test systems, for it constitutes an almost negligible load and cannot do mechanical damage to the IC surface. What's more, its typically 0.5-micrometer diameter makes the beam valuable for in-circuit testing, for it is easy to position on the 3- to 4-μm-wide metal lines found on today's integrated circuits. Finally, by scanning the IC surface and producing a voltage contrast pattern on a cathode-ray-tube screen, it can provide qualitative information on the electrical states of large circuit regions.

In contrast, the mechanical probe is becoming steadily less suitable for testing increasingly complex and dense ICs during their development, according to Wolfgang. Its capacitive load of at least 1 picofarad introduces errors, prohibits accurate measurement of high-bandwidth signals, and may even cause circuit malfunctioning. In addition, positioning it takes time and may harm the circuit's surface.

Moreover, shrinking line widths and channel lengths will impair the ability to test an IC through its external leads and force more measurements to be made within the circuit. "Such measurements are especially crucial during circuit development to determine whether and to what extent electrical functions are consistent with calculated computer data," explains Hans-Peter Feuerbaum, a member of Wolfgang's team.

The concept. The basics of electron-beam testing are simple. Upon striking the point of measurement, generally a node, the beam causes it to emit secondary electrons. These electrons are collected, and from their energy the node's voltage is determined and displayed in digital form on a CRT screen with a resolution of better than 10 millivolts.

The setup implementing these principles consists essentially of an electron gun and a vacuum chamber containing a spectrometer and the circuit under test. The latter fits into a socket inside the chamber's cover



Electrons probe VLSI. When cover (left) is closed, IC mounted in socket in racquet-shaped recess encounters electron beam from gun (not shown) below vacuum chamber. Spectrometer in middle of chamber collects electrons bounced off IC nodes.

but with its pins outside, so that operating voltages and clock signals are easy to apply and there is no need for the long supply cables that could cause noise and ringing. The spectrometer collects the secondary electrons and determines their energy and voltage.

Specifications. To perform its job, the electron-beam probe must meet certain specifications, Feuerbaum explains. Its acceleration voltage must be around 2.5 kilovolts, so as not to cause radiation damage to the circuit or charge its oxide layers. In conjunction with that voltage, the beam current must be on the order of 10 to 100 nanoamperes, to keep the beam diameter to the 0.5 μm suitable for 3- to 4-μm-wide lines. Since circuits with lines 2 μm wide are already in production and 1 μm or so can be expected, the diameter of the electron-beam probe will have to be reduced to about 0.1 μm. This, Feuerbaum says, should be possible with a lanthanum hexaboride or field-emission electron gun and appropriate values for beam current and acceleration voltage.

The equipment operates principally in the sampling mode, which allows voltage waveforms to be observed in the megahertz, and even gigahertz, ranges. By means of a blanking system that produces beam flashes down to a width of 0.3 nanosecond, the beam is pulsed synchronously with the waveform at the measuring point. The total period of a waveform is sampled by the temporal shifting of the pulses relative to the phase of the waveform.

The Siemens equipment should also be capable of under-the-surface measurements. In principle this is possible if the beam's energy is high enough to penetrate an overlying oxide and set up a conductive channel to the metal line beneath.

Such below-oxide measurements pose no problems with bipolar circuits, Feuerbaum says. With MOS circuits, however, the beam will cause radiation damage if its electrons enter the gate oxide, so in them, he cautions, "the electron-beam technique must be confined to uncritical circuit regions."

Great Britain

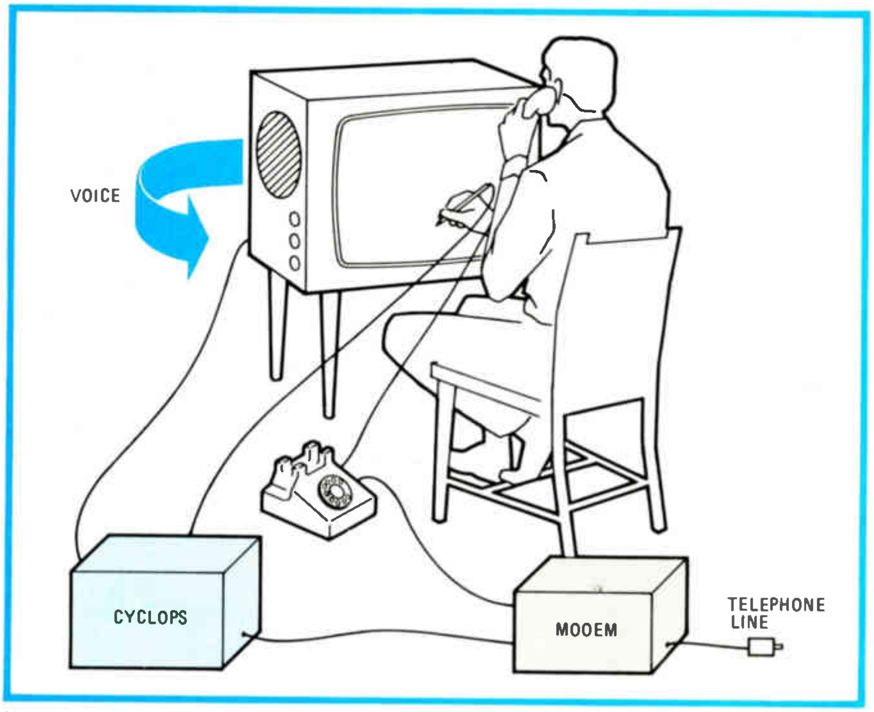
Cyclops will equip TV sets to receive and send color or monochrome graphics

Besides entertaining its owners, playing games with them, and supplying them when requested with phone-based or broadcast stockmarket and catalog information, the domestic television set can now double as a blackboard and turn their living room into a remote classroom.

Currently nearing completion at Britain's Open University is the development of a system called Cyclops that converts the TV set into a cassette-driven audiovisual aid combining sound track and high-quality color graphics. The size of a conventional cassette recorder, it plugs into the antenna terminal of a standard TV set and uses conventional stereocassette tapes prepared at a computer studio. Then, with the addition of a light pen and modem, Cyclops can be used to reproduce on its TV screen drawings and diagrams written on another, remote television screen (see illustration). Adding an alphanumeric keyboard creates a complete computer graphics terminal, add developers Mark I'Anson and David Liddell.

Cyclops was developed on limited research funds to meet the educational requirements of the Open University in Milton Keynes, Bucks. The university provides degree-level correspondence courses supported by off-peak radio and television broadcasts and also runs a network of 250 regional centers using technical colleges and adult educational centers where evening tutorials are held; students and tutor communicate over the university's telephone network, but providing a second telephone line would make it possible to supplement speech with drawings and diagrams.

Industrial. The system's versatility has also attracted industrial interest. A year ago Aregon International Ltd., the London-based software



Homework. By plugging Cyclops into a TV set and phone via a modem, student can use light pen to send sketches to remote professor's TV screen and receive others back.

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Accutest Corporation 25 Industrial Avenue, Chelmsford, MA. 01824 ■ Telephone 617-256-8124 marketing company backed by the government's National Enterprise Board, signed a long-term research and development contract with the Open University that gave it manufacturing and world marketing rights to Cyclops. The Open University researchers will also explore the relationship with viewdata systems, with which Cyclops is downwardly compatible (Aregon is marketing the British Post Office's Prestel viewdata system internationally).

Also, British Telecom—now being formed from the British Post Office—is interested in the use of Cyclops as an adjunct to its remote teleconferencing service [*Electronics*, May 8, p. 78] and is funding field trials later this year at several Open University regional centers.

For the inexperienced. Much of the group's effort has gone into developing studio hardware so that inexperienced users, knowing nothing about computer technology, can prepare and edit their own audiovisual presentations. A basic studio, comprising standard audio recording equipment, visual display units, a TV camera, and a digitizer, would cost in the region of $20,000 to $30,000, which is very low in comparison with film and TV studios, according to I'Anson. In pilot production, the basic Cyclops terminal, complete with an integral modem, costs around $2,000, but in volume I'Anson believes the price would be half that. The cost of preparing both presentations and tape is so low that Aregon sees a big potential for Cyclops in industrial training.

Color Cyclops, developed from the black and white version at the behest of Aregon, is built around a Motorola 6800 microprocessor controlling a jumbo-sized page store for color information and a stereo cassette deck for graphics data and sound.

Though Cyclops is similar in concept to the graphics capability of Canada's Telidon system, I'Anson says that there are differences, and his group plans to propose the system as a future CCITT graphics coding viewdata standard.

The system should attain marketable form within 12 months, but how soon it can actually reach the market will depend on the speed with which Aregon can put the terminal into manufacture and on their marketing strategy. **-Kevin Smith**

Japan

Current trims, adds to resistor values on chip

Analog circuits requiring resistors trimmed to precise values can now be fabricated completely by semiconductor technology, eliminating the need for mixing the technology with thin-film laser-trimmed resistors. Researchers at the Musashino Electric Communication Laboratory of the Nippon Telegraph and Telephone Public Corp. have trimmed highly doped polysilicon resistors to within 0.01% of the desired value merely by passing a controlled current through them. What's more, if the resistance is decreased too much, they can restore up to 90% of its initial value, also by passing a current through the resistors.

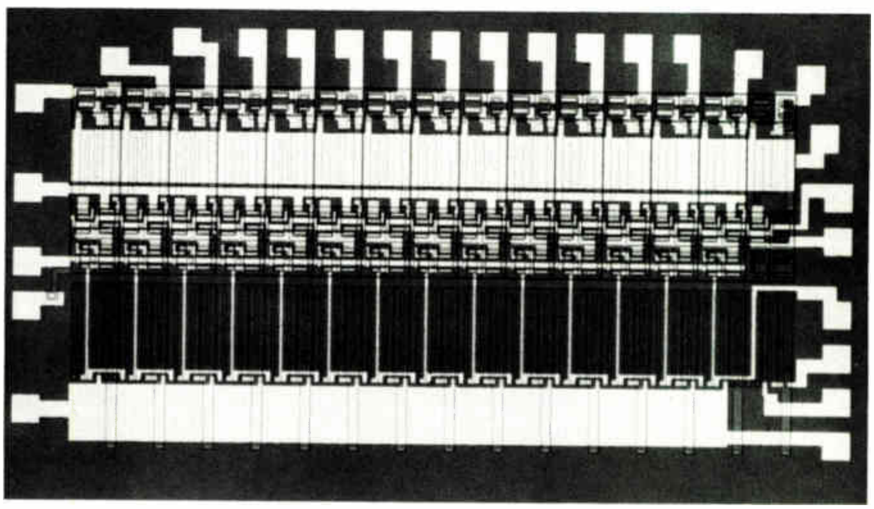
With this technology, a 14-bit digital-to-analog converter has been fabricated on a chip measuring 1.7 by 3.0 millimeters (67 by 118 mils) [*Electronics*, July 3, p. 45]. Nonlinearity after trimming is within $1/4$ least significant bit, indicating that the technology is sufficient for a 15-bit device. Also, as trimming is performed after a device is packaged, the user rather than the device manufacturer can do it, while the risk of resistance change during packaging is eliminated.

Staff engineer Kotaro Kato says that he came up with the highly doped polysilicon resistors after being assigned to develop circuits that could be trimmed without a laser. Laser-trimmed thin-film resistor networks are often as large as or larger than the semiconductor portion of devices because minimum resistor width is about 50 micrometers. In contrast, the polysilicon resistors are 10 mm wide by about 95 mm long.

With laser-trimmed resistors problems of stability still remain in the precision range that Kato aimed for. Also, methods of routing current away from areas damaged by laser trimming, such as opening shunt paths in resistor networks, further increase size. An added disadvantage of laser trimming is that the equipment can cost $1 million.

Kato says that the mechanism of the new resistor has been studied and that calculations based on the theory agree well with practice. The doping of polycrystalline resistors to be trimmed must exceed a threshold value, typically about 10 atoms per cubic centimeter. Neither the meth-

Laser-free trimming. In this 14-bit digital-to-analog converter, polysilicon resistors in the emitter circuit of individual current generators for each bit were trimmed electrically.



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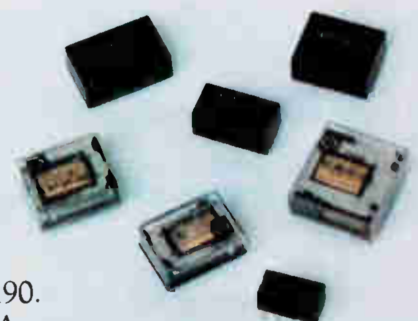

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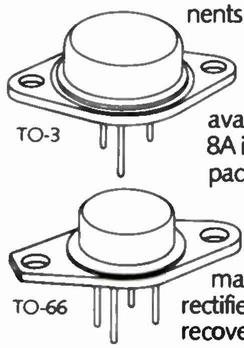

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02173, U.S.A. Telex 95-1064,
TWX 710-326-6509.

UNITRODE

od of doping nor the dopant is important—arsenic, phosphorus, and boron have all been used successfully. Trimming current must also exceed a threshold value, typically 10 amperes per square centimeter. Current is normally pulsed, but for time periods in excess of milliseconds the precise time is not critical because the resistance value soon reaches an equilibrium.

What happens. In highly doped polycrystalline silicon the resistivity is very low within individual grains but is high at the interfaces between grains. High-density currents through the resistors cause localized heating and melting at the grain borders, segregating the dopants into the molten regions (as in zone refining) and thus decreasing the resistivity in these regions. Time is not important because the process is self-limiting—the segregation of the impurities prevents further heating and the process saturates.

If a current somewhat lower than that used for trimming is passed through the same resistor, temperature at the grain boundaries rises to a slightly lower level than previously and causes diffusion of impurities out of the grain boundary region. Although restoration of trimmed resistance can repair errors in processing, it has an even more important function: if resistors are trimmed to slightly below their desired end point and then restored to the desired value, they are stabilized against change from exposure to high temperatures. **-Charles Cohen**

Earth station can sit in the window

Innovative antennas being developed by two companies, one in Japan and the other in the U. S., presage a new international market in satellite earth stations for the home and office. Key to both developments is the technique of constructing the dish itself out of inexpensive metal-coated glass-fiber–reinforced plastic.

With an eye primarily to institutional use, the Yokosuka Electrical Communication Laboratory of the Nippon Telegraph and Telephone Public Corp. designed its small offset parabolic antenna, complete with built-in receiver, for satellite data communications. Researchers there have successfully transmitted data simultaneously to a number of these stations from a data center in Yokosuka via Japan's experimental stationary-orbit communications satellite. Each station decodes only that portion of a transmission addressed to it.

In the test, the signals were transmitted at 64 kilobits per second and were used to set up 11 separate circuits of 4.8-kb/s facsimile. The antenna's gain is 26.3 decibels.

Window seat. The 90-kilogram unit is only 70 centimeters wide by 98 cm deep and 126 cm high. With a 60-cm effective aperture, it is small enough for use indoors behind a window that has a view of a satellite. Yet it is sturdy enough in construction for use outdoors.

So far, only a technical feasibility study has been made and there are no plans to put the equipment into production. But the company estimates that the system could be produced for $1,000 to $2,000 depending on volume.

Meanwhile, in the U. S., Gardiner Communications, a Burnup and Sims Inc. subsidiary located in Houston, Texas, expects its 5.6-meter-diameter glass-fiber panel antenna to have a big impact on the market in satellite TV-signal reception. According to president Clifford T. Gardiner, the unit is especially good for fringe reception areas.

The design of the antenna feed horn and the precision tolerances obtained with the glass-fiber construction give Gardiner's system a gain of 46 dB at a price of under $10,000. Other units with the same gain sell for nearly twice as much, and "similarly priced antennas have 43.5- and 44-dB gains," Gardiner notes.

Like the Japanese system, the panel antenna is designed for a standard 6-gigahertz up link and a 4-GHz down link. **-Charles Cohen and Harvey J. Hindin**

VLSI pushes super-CAD techniques

Computer-assisted design development is led by universities and computer makers as true design automation is still sought

by Martin Marshall, West Coast Computers & Instruments Editor, and Larry Waller, Los Angeles bureau manager

Like the miller maid in the fairy tale "Rumpelstiltskin," the designer of very large-scale integrated circuits may see his task as one of spinning mountains of straw into gold overnight. The complexity of designing chips containing 100,000 transistors is just plain intimidating; with present design tools it is impossibly slow. As William Lattin of Intel Corp.'s computer-assisted design group defines the problem: "With present design methods, a 100,000-transistor MOS chip will take 60 man-years to lay out and another 60 to debug."

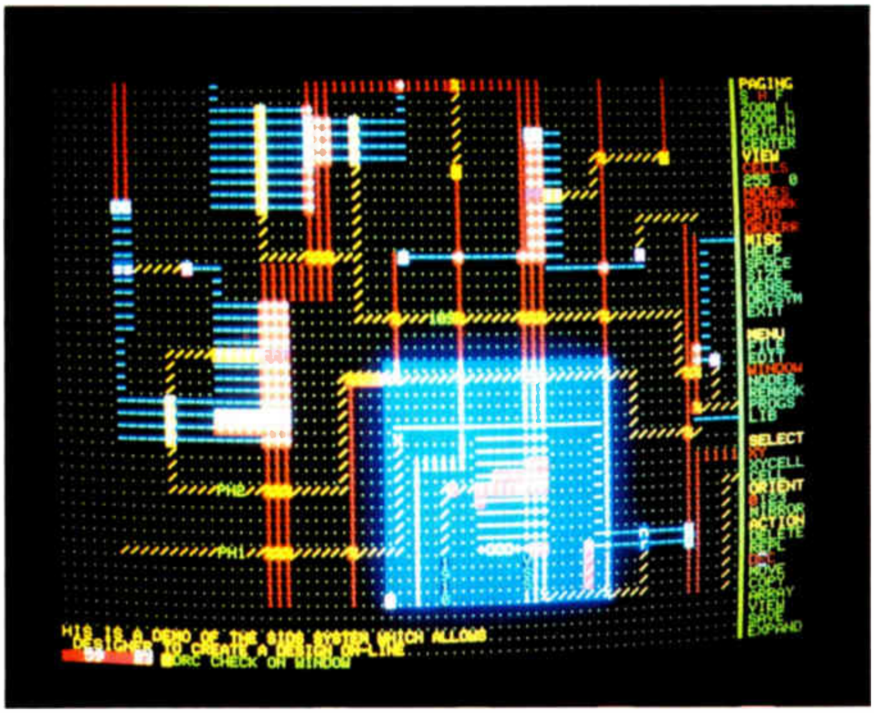
For most semiconductor manufacturers, a time of wrenching change in integrated-circuit design methodology is about to dawn—but not without some resistance. After all, the process has functioned for years without much change, until it became tedious and painstaking at the LSI stage.

Even today, a typical procedure at a major semiconductor house consists of the so-called paper doll approach: the topology of a chip is created by manually drawing shapes, polygon by polygon, on layers of Mylar. That layout must then be digitized, point by point, and entered into memory before a designer can use the power of the computer to perform elemental tasks such as design-rule or interconnection checking, logic or circuit simulation, or other necessities.

Building cells. This methodology is being attacked, from top to bottom, and being replaced with artwork techniques based totally on cathode-ray-tube displays and by an explosive growth in the power of programs used in all stages of the design process. Symbolic approaches have reached very high levels of design, as have the "cells" stored in computer memory, which can be recalled and used like cookie cutters to build up larger arrays. The entire process of chip composition, in fact, is being methodically automated to the point where, as VLSI pioneer Carver Mead of Caltech—the California Institute of Technology in Pasadena—puts it: "People will be able to complete microprocessor designs as fast as they can define the properties of the microprocessor."

It may take several years or longer for such a dream computer-aided design system to reach the marketplace as a commercial product, but the universities and advanced computer manufacturers are not waiting for commercial CAD firms such as Calma of Sunnyvale, Calif., and Applicon Inc. of Burlington, Mass. They are building those systems in house now. The systems are based upon fundamentally new concepts, such as "stretchable cells," "spacing synthesis," a new form of transfer functions, and hierarchical, iterative simulation processes for both logic and timing.

But what is possibly most important, the various software pieces of the CAD puzzle—usually incompatible programs written at different universities in different languages running on the different operating systems of different computers—are being knitted together into cohesive operational programs drawing upon unified data bases.



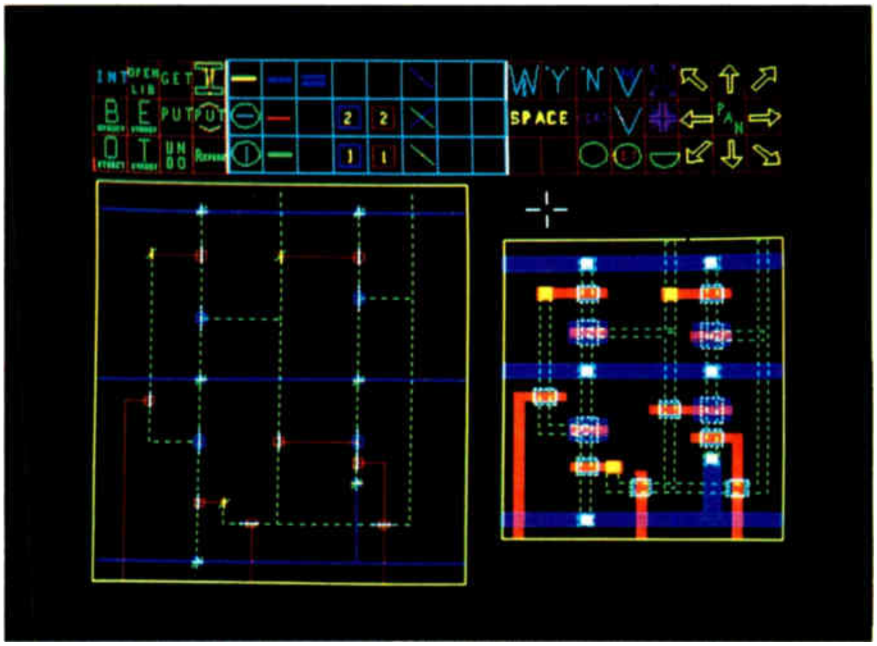
SIDS. Inspired by Rockwell's symbolic approach, SIDS (symbolic interactive drawing system) from AMI elevated it from batch processing to on-line, interactive design.

This unification movement has its roots in CAD development projects at major universities that are in turn generously subsidized by the computer and semiconductor industries. The first appearance of a symbolic approach to CAD, however, is traceable to the Microelectronic Devices operation of Rockwell International Corp. in Anaheim, Calif. Spurred in the late 1960s to break a production bottleneck, Rockwell began evolving a gridded CRT-based formula for describing logic. American Microsystems Inc. of Santa Clara, Calif., advanced the batch-processing technique a step further to on-line interactive design with SIDS, for symbolic interactive drawing system.

At Rockwell, the group still uses Mylar to lay out a device. However, once the device design is digitized and entered into a computer, the system's program abstracts the polygon level one step up into a matrix representation.

Using Sticks. The next step up is the Sticks level, the brainchild of John Williams, who developed the idea from his master's thesis at the Massachusetts Institute of Technology, Cambridge, into a working tool at Hewlett-Packard Co. [*Electronics*, April 10, p. 40]. Sticks is a totally CRT-based method in which the designer can use a light pen to draw representations at the schematic level on the CRT. Each of the elements drawn must correspond to a multilevel polygon representation stored in the computer, but as that library becomes established, the designer becomes free to work at the schematic level.

Perhaps more important than the higher level of symbology, Sticks introduced the concept of spacing synthesis. The Sticks system does not display a grid, as does the Rockwell system, because the actual spacing between the elements in the schematic is performed by the Sticks program. That program, in fact, shrinks the design down along the X and Y axes until it has the minimum spacing allowed by the design rules. One very important aspect of this process is that it makes the circuit representation independent of the design rule; going from n-channel MOS to Intel's high-performance HMOS II, for example, becomes a



Sticks. First developed at Hewlett-Packard and now working at Calma, Sticks provides spacing synthesis and schematic-level design. It is based totally on CRT and light pen.

simple matter of recompilation using new design rules.

Beyond Sticks is a concept called bristle blocks [*Electronics*, Jan. 3, p. 40] developed by David Johannson at Caltech. This program treats giant lumps of circuitry (the blocks) as single rectangular entities with well-specified interconnections at their boundaries (the bristles). When two such bristle blocks are set together, the combined cell should meet all the criteria of stimulation, continuity, and design-rule checking that had been verified in the original blocks.

"The bristle blocks are an example of what we call correctness by construction methods," notes Caltech's Mead. "It includes a great deal of semantic processing that transforms the functional description of the instruction set into a layout that creates new cells. The idea is that if you build the little pieces correctly and put them together correctly, then the chip-composition process will yield a larger block that has certain freedoms. These include freedom from race conditions, freedom from logic level mismatches, and freedom from polarity problems, among others."

Stretchable cells. A great aid to the orderly chip-composition process that Mead describes is the concept of stretchable cells. Stretching a cell under program control in order to make its interconnections match those of a neighboring cell may cause a slightly larger cell, but the loss in cell density is more than compensated for by the elimination of wire-routing real estate. "These chip composition techniques give the designer seven-league boots to work in," asserts Mead. "Already, we can do in a couple of days what used to take tens of man-years."

Mead notes that bristle blocks and the stretchable-cell concept are only two results of a number of projects under way in the Silicon Structures program at Caltech. The most recent products of the project, which is jointly funded by HP, Digital Equipment Corp., Burroughs, Intel, IBM, Honeywell, and Xerox, include a hierarchical design approach based upon leaf-cell (a coined term for the lowest common denominator in a circuit) functions [*Electronics*, June 19, p. 56] and a Sticks-like program called REST (Ricky's editor for Sticks) that can both stretch and contract. "The REST program has the hooks in it to become the bottom end of our silicon compilation program," notes Mead.

Polycells. Before Caltech's chip-composition techniques, there was the polycell approach taken by Bell Laboratories in Murray Hill, N. J. Instead of Mead's symbolic layout—which Bell Labs is also pursuing—polycell relies upon a library of cells having the same height. The width varies according to cell content, but the uniform height allows the specification of uniform interconnection points and functions along the vertical walls of the cells. Thus, when the standard cells are laid side by side, they can be routed automatically using LTX algorithms (see "A glossary of CAD terms," p. 79). "A second advantage of polycells is that the logic of the interconnected cells can be verified," notes Robert C. Fletcher, the executive director of the labs' Integrated Circuit Development division.

Bell uses the polycell approach on its LTX automatic LSI layout system. So far, one of the system's largest chips has been an echo canceler using 34,000 transistors. "The design used approximately 100 different cells," notes Fletcher. He sees such a layout system going on to design hybrid chips like codecs and delta-sigma digital filters.

The futuristic methods described so far can be generically labeled as chip-composition strategies, but a group in Livermore, Calif., has shown that decomposition can work, too. The basic idea, according to L. Curtis Widdoes and Tom McWilliams of the S-1 project at the Lawrence Livermore Laboratory, is to address the design of a giant computer system at the highest level.

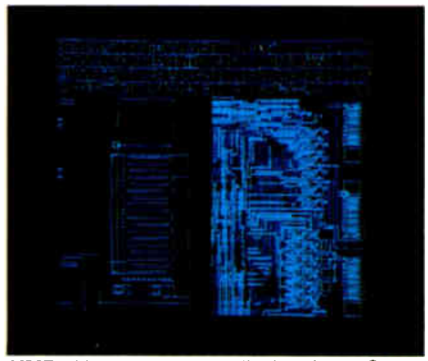
That basic functional description is then broken down, in successive hierarchies, so that each functional block in the highest-level diagram is divided into subfunctional blocks on the next lower level in the hierarchy. Eventually, the functional description reaches the level of a recognizable cell or points to a new kind of cell that needs to be created.

The basic idea is simple, but what makes it work is the Scald (structured computer-aided logic design) program, which provides for functional, logic, and even timing simulation routines on each level of the hierarchy. "In this method, partitioning *is* the design process," reports Widdoes. "The way that the functional blocks are specified includes, for example, timing information, so that you can run timing checks at a very high level. On the surface, this may seem like a straight top-down method, but in practice the designer is often steering his higher-level descriptions in the direction of known lower-level blocks, then jumping down to work on a new lower-level block or someplace in the middle of the hierarchy. The beauty of this approach is that it allows simulation on many levels and before the design is completely defined."

Scald was created to help design a computer, the S-1 Mark I, which has computing power in a league with the giant Control Data 7600. Widdoes points out that though the design time was estimated at about 100 man-years, Scald enabled his group to complete the Mark I design in 2 man-years. (Control Data Corp. has since developed an automated gate-array approach, available on the Cybernet service, with which it cut a computer's design cycle to 120 days.) Currently, Scald can take a design from basic architectural definition into a wire-wrapped board-based system. However, a variation of Scald intended for VLSI design is already being developed under the tutelage of Forrest Baskett at Stanford University in Palo Alto, Calif. "Widdoes and McWilliams are heroes," claims Baskett. "They not only had the audacity to attack design at the highest level, but they also had the tenacity to work through the sticky detail required in the timing-verification program."

The Scald package consists of a graphics editor (SUDS, for Stanford University drawing system), which allows the designer to create drawings on the CRT; a macro-expander, which compiles the drawings; a packager, which embeds them in a physical package; and a timing verifier. The macro-expander, since it expands the design to smaller circuits by iteratively substituting the appropriate macrodefinition for each macrobody in the drawings, is the program's key to hierarchy. The timing verifier does a complete, state-independent verification of all timing constraints in any synchronous digital design, including an incomplete design.

Pegasus to fly. The implementation of the Scald program at Stanford—with a new module that aims it toward chip design—is only part of Baskett's work on a larger chip-composition process that he dubs Pegasus, after the mythical flying



VMD. Vector memory display from Calma provides panning and zooming on both sides of a split-screen display. This gives the designer both a global and a local view.

horse. It is two or three years from completion, but in its final form it will contain parallel layout and logic-design paths that are joined by a circuit extractor routine that generates an interconnection list.

The logic-design portion begins with an interactive drawing system, which creates a file used by the Scald design program. Scald then creates a logic-design file that undergoes functional simulation checking. The result is combined with the interconnection list information and verified for circuit equivalence and wiring delays. Having achieved the layout level, this file is given to the last level of the Scald timing-verification program and goes in turn to pattern generation for mask making.

The layout scheme in Pegasus feeds layout instructions for the programmable logic array into Icarus, an interactive layout editor developed by Xerox. Icarus turns the edited layout into CIF—for Caltech intermediate form—for a circuit extractor routine designed by Clark Baker at MIT, which in turn generates the interconnection list. The interconnection list then passes through switch-level simulation before being combined with the logic-design file. "What we're trying to achieve with this system is a good human interface and high system speed," notes Baskett. "I think that is more important than extreme functionality." Baskett's contribution to the scheme is the interfacing of the program modules, and the develoment of the circuit-equivalence verification program.

More recently, efforts at Stanford have been focused upon creation of

Japanese believed to be ahead

It is difficult to tell where Japanese firms stand with computer-aided design because of its critical role in highly proprietary plans for very large-scale integrated circuits. Semiconductor houses, for instance, mostly do not disclose what they are doing and computer heavyweight Fujitsu Ltd. will not discuss CAD. But CAD experts believe Japanese firms overall lead U. S. counterparts in two key phases: symbolic design of chips, where software programs that generate layouts replace manual drawing and digitizing; and greater use of large computers to run CAD design, simulation, and checking software, rather than the minicomputers largely employed in the U. S.

Generally, CAD now in operation resembles the U. S. mixed bag of commercial equipment and improvements of both in-house software and programs turned out by American universities. At Nippon Electric Co., new-process simulation is done by its own program and Stanford's Suprem. Circuit simulation is by in-house software and Spice from the University of California at Berkeley. NEC also has a program to perform logic checking from a layout, both drawing and comparing it with a simulated circuit, says Tadashi Nishide, supervisor of the IC division's CAD department.

Hitachi Ltd., on the other hand, uses improved versions of commercial units from Calma of Sunnyvale, Calif., and Applicon Inc. of Burlington, Mass., with throughput stepped up with parallel Hitachi M-180 computers (equivalent to IBM 370-68s). According to Akira Osawa, manager of the software engineering center at the Musashi works, CAD processes at Hitachi include circuit, logic, and fault simulation; generation of art from digitized output; and checking of art and topology. But plotter outputs are gone over by hand before undergoing automated checkout, he says, pointing up the continuing importance of the human role in Japanese CAD. **-Charles Cohen** an Ethernet-based low-cost work station for CAD. Dubbed SUN, for Stanford University network terminal, the terminal can provide eight high-resolution channels (1,280 by 819 pixels) or 32 medium-resolution channels (640 by 409 pixels). They are expected to cost as little as $1,000 each in a 16-terminal system.

Scheme-79. The circuit (or node) extraction program used in Pegasus also forms part of a chip-composition scheme at MIT. As MIT's Jonathan Allen, a professor of electrical engineering and computer science, describes it, the system allows a designer to request the generation of a programmable logic array (by supplying Boolean equations that describe the PLA), then query the system about the silicon area the design will occupy. One can change the design's aspect ratio; check its speed, power dissipation, and connectivity; and flag semantic errors.

So far, Allen's system has designed a 10,000-transistor single-chip microcomputer, dubbed Scheme-79. The chip, which interprets a version of the LISP computer language, was designed in one month by researchers at MIT's Artificial Intelligence Laboratory in what Allen terms a "heroic" effort. Like Stanford, MIT is developing its own IC-fabrication facility.

Spice and Splice. While several universities have concentrated on the chip-composition process, none has been as prolific in generating simulation and verification tools as the University of California at Berkeley. "We have what we call the toolbox approach to CAD," observes Berkeley's Richard Newton. "We realize that the term 'design automation' is still a misnomer at this point. The best we can do is to construct these design aids and slowly build a toolbox of useful programs."

Berkeley's most used tool to date is Spice (simulation program with IC emphasis), which emulates a chip's circuitry at the layout level. Spice has been distributed to more than 2,000 installations so far, and Berkeley computers alone accessed the program over 60,000 times last year. Spice, in fact, has entered its second generation, a portion of which Newton developed.

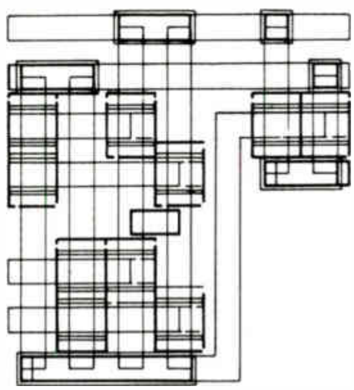
Newton's larger contribution,

Structured cell-based symbolic strategy

Besides the device simulation and various layout and checking routines, Hewlett-Packard Co. has also tried to maximize the designer's effort with a chip-synthesis tool dubbed the structured cell-based symbolic strategy. This strategy relies heavily upon the development of standard cells, which are interconnected automatically when they abut. Though the cells HP currently uses are fixed in size, the incorporation of stretching algorithms into the program is under way.

To optimize the designer's participation in the chip-composition process, moreover, the HP system displays high-level symbolic representations on its color-CRT–based system without the clutter of a great deal of lower-level information. "The more concise the information that we display to the designer, the better will be his optimization of design at the higher levels," notes Merrill W. Brooksby, manager of corporate design aids. In this representation, for example, a complex, multilevel object such as a large gate is described with a single-level symbol. The strategy also calls for small increases in the amount of material displayed, such as the use of labels, which greatly increases the intelligibility of the information presented.

In successive representations, the lowest level of design, the layout polygons (a), can be represented as a Sticks diagram (b) composed of positive and negative transistors. This diagram, in turn, can be represented in schematic fashion (c) or as a labeled gate (d). At the gate level, only the labeled interconnections and functional description of the gate need be represented, so that the designer can focus upon a much broader scope in the design. "In this case interconnection is the primary consideration, not the size of the cell," Brooksby says. There are two techniques that can help this process. One is keeping bus lines straight through the chip, even at a slight expense in area, because the regularity is likely to reduce the overall area. A second technique is that of running various interconnection lines through the cells themselves to connect nonadjacent cells. **-M. M. and L. W.**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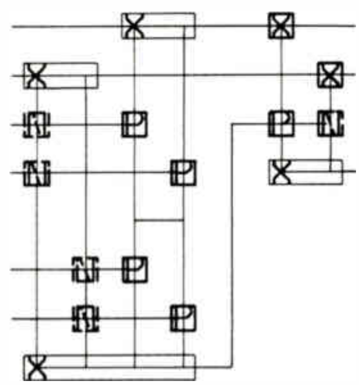
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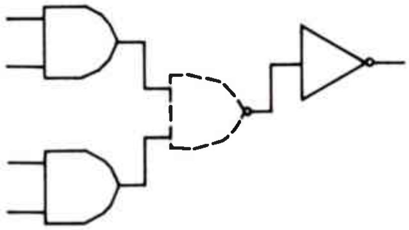
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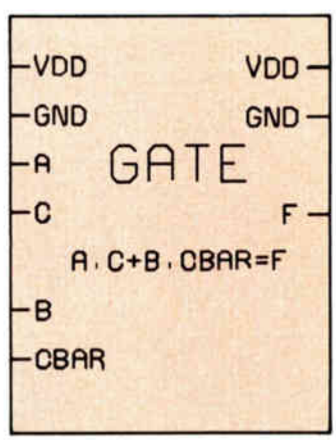

(d)

however, has been as the author of Splice (simulation program with large-scale IC emphasis), a hybrid (logic and circuit) emulation program that runs approximately 100 times faster than Spice. It gains its speed advantage by emulating only the portions of a circuit that are showing activity. Newton is currently revising Splice into a commercially usable product that should be available by the end of summer.

Another simulation tool in development at Berkeley is a method of mixing simulation among different levels of hierarchy. Notes Berkeley's David Patterson: "We are determining whether it is possible to get just as good a simulation as Spice while mixing simulation at the circuit level with simulation at the register-transfer level. The basic idea is to interface simulations at the polygon, transistor, gate, block, register, adder, and processor levels. This work should reduce the computer time required for a simulation by a factor of 10 to 100."

Patterson's simulation cannot be carried out, however, using CIF as a language because CIF has no provisions for simulation at the higher levels of abstraction. CIF has been proposed as the standard layout language because many of the universities are using it as the final expression of layout, which can then be taken automatically to pattern generation.

The structured interchange format (STIF) developed by Berkeley's Carlos Sequin does have these higher-level simulation properties, however. STIF provides the language in which Patterson's simulations can describe the parameters surrounding a block to be simulated. Using this process, a designer can construct circuitry down to a minute level in one area of a chip and then run a simulation of the chip while major portions of the circuitry are still only broadly defined.

Greater computing power. These efforts to cut down the computing time involved in simulation are well-founded, because, by all accounts, the computing power of a CAD system is a major limiting factor in the designs that these systems can create. For example, the verification of masks for Texas Instruments' 64-K dynamic random-access memory took 56 hours on an IBM 3033 using 12 megabytes of memory.

Allen of MIT and Newton of Berkeley see special-purpose computing hardware being developed to act as coprocessors for the CAD system's general-purpose computer. "I would expect to see something like a hundredfold speedup in checking topology, for example, with the use of specialized hardware," predicts Allen.

Lack of computing power, in fact, is one of the most often-heard criticisms of commercial CAD equipment on the market. "We are not in the business of simulation," responds Calma's Ben Lee. "Besides, if somebody wanted to run extensive calculations, our system can off-load its data into a larger computer."

HP's grand scheme. Still, some computer companies—notably Hewlett-Packard, DEC, and IBM—have decided not to wait for usable commercial CAD systems to appear. HP, for example, has had its own CAD program since 1975 and is heavily engaged in combining synthesis and verfication techniques into a single, unified data base. "We found that we couldn't buy what we needed, so we set out to build our own," recalls Merrill W. Brooksby, HP's manager of corporate design aids.

As he saw it, commercial systems provided computer-aided artwork for the implementation stage of design, but programs for the definition of ICs and for their evaluation were virtually nonexistent. He places system design and functional simulation in the definition stage. The implementation stage includes artwork, design-rule checking, and mask modification. After these stages come the evaluation tools—test vector generators—and the documentation programs.

Currently, HP is working on a unified process that provides for three levels of interactive editing, including programs for the text level, the schematic level, and the artwork level. In this grand scheme the data bases describing a VLSI chip's schematic, functional behavior, electrical performance, and actual geometries are coresident and accessible to the operational programs.

The operational programs include a process simulation routine (Suprem), a device-parameter simulation routine (Tecap), circuit-modeling routines (MGP, Smosi), and circuit timing simulation routines (Spice, Motisc). When a device has passed these design stages, it is ready for system design. The library cells are built up to logical and functional blocks that undergo functional simulation and testing (IFS). Next, the composite is put into artwork and verified using design-rule checking and mask modification. The resulting artwork is then translated by a mask-generation routine (Smash) that produces the patterns necessary to fabricate the actual masks.

Brooksby hastens to add that not only are the operational programs in varying stages of refinement, but also new, synthesis-oriented blocks are still being added to the system description. In particular, the process could take on higher-level functional simulation, such as the descendants of Scald and Pegasus.

The process could also be expanded to include automatic placement and routing such as that advanced by Bell Labs, RCA, CDC, and IBM, but Brooksby is not leaning that way. "Those programs waste too much area in interconnection," he asserts. "If you cannot look at a piece of silicon and see that at least 80% of its real estate has been utilized, then there is something inefficient in the way that chip was developed. Those techniques sacrifice both performance and density."

Instead, he looks toward HP's structured cell-based symbolic strategy, developed by Kent Hardage of the Colorado Springs (Colo.) division. Unlike Bell's polycell approach, this one seeks to regularize cells by placing data buses vertically and control lines horizontally on standard—soon to be stretchable—cells (see "Structured cell-based symbolic strategy," p. 77). "This strategy speeds up development time by an order of magnitude or better without losing performance on the chip," Brooksby claims. As an example, he cites a chip containing over 3,000 gates that HP designed in four weeks.

An integrated VLSI design system

A glossary of CAD terms

Bristle blocks: a chip-composition program that combines blocks of circuitry with such attention to interconnections that the combined cell automatically meets the same verification criteria passed by the individual cells (California Institute of Technology).
Cabbage: computer-aided building block generator, a Sticks-like compaction program that iterates X and Y compactions (University of California at Berkeley).
Calmos: computer-aided layout for MOS, an automatic placement and routing routine for a standard cell strategy (Catholic University of Louvain, Belgium).
CIF: Caltech intermediate form, a machine-readable language used to describe polygon-level layout features for mask-generation equipment (Caltech).
Diana: a mixed-mode simulation routine similar to Splice (Catholic University of Louvain).
EDS: engineering design system (IBM).
Icarus: IC artwork utility system, interactive graphic software using a grid display at the polygon level (Xerox Corp.).
Ice cubes: a chip-composition strategy that freezes a cell's design inside a design-rule dimension while leaving the cell edge eligible for modification.
Ideas: an interactive graphics design subsystem that converts a logic schematic in the SUDS data base to a physical gate-array chip layout (Digital Equipment Corp.).
IFS: interactive functional simulator, a functional simulation routine that can operate at the gate level or higher (Hewlett-Packard Co.).
ISP: instruction set process, a higher-level language used for functional description in Carnegie-Mellon University's design-automation system.
IV: interconnect verifier, software that compares a SUDS wire list with a wire list drawn from a tape generated by the pattern generator (DEC).
LTX: LSL to X–Y mask, a system that translates a circuit description written in Bell Labs' LSL (logic simulation language) into the X–Y coordinates of a mask design expressed in another Bell language, X–Y mask.
MGP: modified Gummel-Poon, a circuit-modeling program that calculates the beta factors of a circuit's transistors, using Tecap's parameters (Bell Laboratories).
Motisc: MOS field-effect transistor timing simulation program, a Spice-like routine that has been trimmed down. It sacrifices some accuracy and flexibility to run an order of magnitude faster than Spice (Berkeley, Bell Labs).
MP2D: multiport two-dimensional routine, an autorouting program similar to that used for polycells (RCA Corp.).
M-SINC: MOS simulator for integrated nonlinear circuits, a circuit simulator similar to Spice, but with some modeling capability (Stanford University).
Oliver: a verification program that analyzes the data base from which the mask-generation tape is derived (1:1 with the tape itself) by running a series of checks of the inter- and intra-mask design rules (DEC).
Pegasus: a chip-composition scheme incorporating the work of several universities (Stanford).
PG: pattern generator, a program that uses the data base from Ideas to generate the instruction tape for an automated mask generator (DEC).
Polycell: a chip-synthesis approach that uses autorouting and abutment to combine cells of uniform height (Bell Labs).
REST: Ricky's editor for Sticks, a Sticks-like graphics editing program that can stretch cells as well as compact them (Caltech).
Sage: a logic simulation program that verifies the gate-level implementation of an IC design created using SUDS. It dynamically surveys all networks for proper dc loading, pull-up and pull-down, and for illegal combinations of input and output connections (DEC).
Scald: structured computer-aided logic design, a design methodology supported by a simulation program that provides for functional, logic, and timing simulation routines on each level of hierarchy (S-1 project, Lawrence Livermore Laboratory).
Sedan/Tandem: one-dimensional semiconductor device analysis/two-dimensional analysis for device modeling, routines used to calculate transistor betas and the threshold voltages of MOS processes from a profile (Stanford).
Siclops: Sandia IC layout program, a hierarchical automatic placement and routing program (Stanford, Sandia National Laboratories).
SIL: simple illustrator, a recent successor to SUDS, released by Xerox in April.
SLAP: stretchable layout and placement, a chip-composition scheme that is constructed along the lines of bristle blocks but containing both stretching and compaction algorithms (Caltech).
Smash: a program for converting polygon-level layouts into patterns for mask generation (HP).
Smosi: simplified MOS model I, a circuit-modeling device-simulation program (Berkeley).
Spice: simulation program with IC emphasis, time- and frequency-domain circuit simulation at the layout level, currently the most popular simulation tool (Berkeley).
Splice: simulation program with large-scale IC emphasis, a hybrid (logic and circuit) emulation program that runs approximately 100 times faster than Spice (Berkeley).
Sticks: a method based totally on the cathode-ray-tube display whereby the designer can use a light pen to directly draw representations at the schematic level (HP).
STIF: structured interchange format, a CIF-like language that provides a framework for higher-level and mixed-level simulations (Berkeley).
Stretchable cells: a concept of stretching circuitry so that interconnections at cell boundaries are made through abutment (Caltech).
SUDS: Stanford University drawing system, an interactive graphics system that allows complex symbols to be stored and recalled and provides for easy movement and replication of circuit blocks (Stanford).
Suprem: Stanford University process engineering models, a process-simulation routine that predicts electrical parameters based upon oven time and temperature; it creates parametric profiles of impurity concentrations (Stanford).
Tecap: transistor electrical characterization and analysis program, a device-simulation routine that characterizes device parameters (Stanford, HP).
Testaid: a simulation of logic and timing, as well as a simulator of stuck input/output faults (HP)
VMD: vector memory display, a split-screen, independent pan-and-zoom display enhancement to the GDS-II color display station (Calma).
WRC: wire rule check, a program that analyzes networks for loading, run length, metal widths, and metal resistivity (DEC).

is also a hot topic at Digital Equipment Corp., which uses a "chip assembler" developed by Craig Mudge, technical director of DEC's VLSI advanced development group. The chip assembler is an umbrella program that manages the various chip-composition, simulation, and layout routines. It stores all design information in a single data base, which serves to make iterative simulation and modification a much simpler process. The chip assembler also takes on the complex task of interconnection management, even allowing mixtures of four different connection techniques: abutment, stretching, a routing subroutine, and hand routing of interface blocks.

Mudge prefers the chip assembler's PLA-based approach to IBM's gate-array approach, because, as he notes, "bipolar gate arrays run out of steam between 1,000 and 2,000 gates." Other researchers at DEC, however, have developed a gate-array method to fulfill the company's short-term IC needs.

DEC's chip assembler will be used this summer to create a VLSI floating-point processor chip. "The chip is a very irregular type of architectural subassembly, so if we can map that we will have proved the value of the chip assembler," Mudge says. The chip will contain about 100,000 transistors on its 200-by-400-mil surface.

Enter IBM's EDS. Though some may charge that it wastes chip real estate and others assert that it compromises a chip's performance, advocates of IBM's engineering design system (EDS) point out the system was largely responsible for the timely arrival of IBM's impressive 4300 series of mainframes. The elaborate system is used to design the metal interconnection layer for IBM's gate-array master-slice chips. These chips contain predefined pieces of circuitry that lack only the interconnection layer to determine the functions that the circuitry will perform.

In using EDS, the designer first expresses the concept as a logic diagram on a system terminal. This establishes the functional partitioning of the chip and creates a data base that is acted upon by various simulation and verification routines, including logic-delay checking. Then it automatically maps the logical design into a physical chip layout using a placement routine. When it reaches this point, the computer checks to make sure that the circuit complies with applications rules and fanout limits. As a final step, EDS then generates the test patterns necessary to verify the completed chip.

New directions. From the EDS system to the various chip-composition schemes on university drawing boards, the semiconductor companies must soon decide which CAD tools will best help them meet the VLSI design crisis. Since, by one estimate, about 70% of U.S. semiconductor designs are currently composed in the "Mylar jungle," such a decision will represent a major retraining effort and a major capital-investment effort.

The effort, by all accounts, will be made, with the cost of the CAD system becoming only a secondary factor. Intel, for one, will devote a third of its capital-expenditure budget this year to CAD equipment. The effort will be made not just because the Japanese are doing it, and not just because the complexity of VLSI demands it, but because these new CAD methods will greatly improve the productivity of the individual designer. As TI's Spence puts it: "My company will be designing ICs in 1985 and 1990. The degree to which I am successful now will determine the productivity of our people designing ICs then." □

Reporting for this article was also done by James B. Brinton and Linda Lowe in Boston, Wesley R. Iversen in Dallas, Pamela Hamilton in New York, and Charles Cohen in Tokyo.

Turnkey CAD systems scramble to keep up

As the two largest producers of commercial computer-aided design systems for integrated-circuit design, Calma of Sunnyvale, Calif., and Applicon Inc. of Burlington, Mass., are under fire. Criticism of the two firms' products centers on the cost of the systems, their lack of computing power, and the limitations of the systems, which produce only artwork at the lowest level of design, the polygon level. "They are concerned with geometry, but we're not designing geometry, we're designing circuits," sums up the California Institute of Technology's James Rowson. Adds Digital Equipment Corp.'s Craig Mudge: "Single stations, for only one operator, are generally quite costly, about $100,000 to $200,000."

But the two firms are not standing still. Spurred by a market expected to pass $400 million in sales this year, both are already shipping upgraded systems and have more advanced systems under development. Calma, for example, is delivering its vector memory display (VMD) station after a two-year delay. VMD gives the designer a split-screen display of chip layout, one side zeroing in on a detailed part, the other on a global view of where the part fits in. Earlier this year, Calma announced its GDS II color display station, with improved computing power and a much finer grid containing 32-bit rather than 16-bit data points. Working in the laboratory, however, is Calma's next-generation system, which contains a Sticks-like program. Beyond Sticks—and not yet implemented—is Calma's so-called ice cube concept, which contains a mixture of high-level symbolic representation with low-level representation of interface circuitry. At Applicon, the switch to color displays begins this month. The company notes that it is currently working on programs for compaction, on-line electrical rule checking, on-line conductivity checking, and fast feedback analysis of circuits. According to Phillip R. Rossignol, the company's marketing manager for microelectronics, Applicon may hear the giant footsteps of IBM. "If IBM decided to take its in-house CAD system to market, it would be a very serious threat," he says. Francis G. "Buck" Rodgers, IBM's vice president for marketing, has said that CAD is an area that IBM would like to pursue aggressively in the 1980s. However, sources at the company say it has no plans to do so now.

In the meantime, Calma and Applicon see competition from small, new companies that are formed to produce less costly CAD systems. One such company, Avera Inc. of Scotts Valley, Calif., has already been formed and will introduce its GT-1 system this fall. The company president, Mike Dickens, came from Applicon. He describes the GT-1 as a microprocessor-based graphics input and editing work station. **-M. M. and L. W.**

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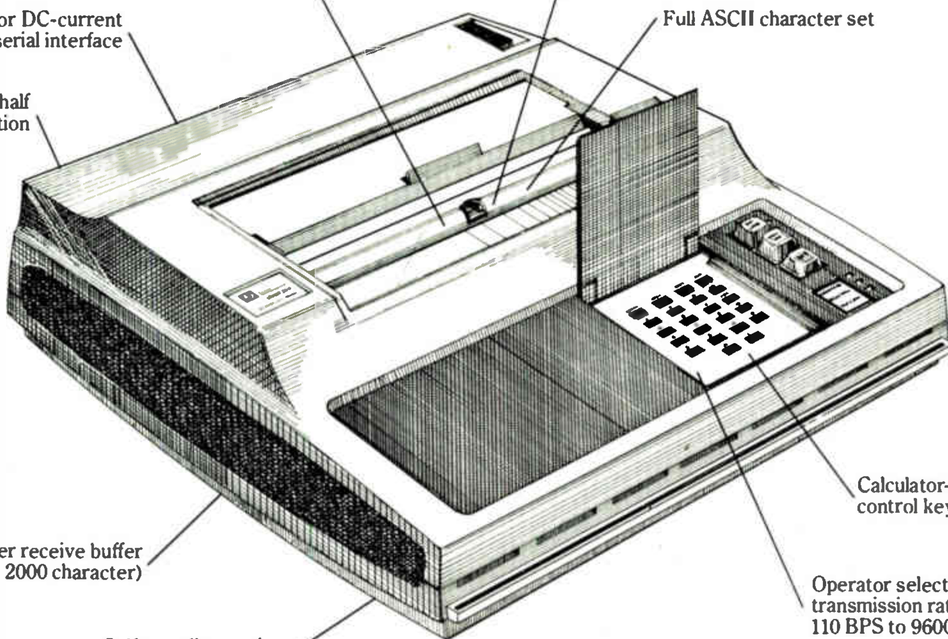

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RCA sets SOS aside

New management team prepares to embark on strong C-MOS program now that drain of sapphire work has been pinched off

by John G. Posa, Solid State Editor, and Pamela Hamilton, New York bureau manager

Intoxicated by silicon-on-sapphire technology and its promise of dazzling speed and mighty densities, RCA Corp.'s Somerville, N. J., Solid State division has found, instead, more headache than profits and has decided to swear off the stuff.

Unable to bring the prohibitively high cost of sapphire and the processing it entails down into the realm of commercial volume production, RCA's semiconductor wing, which expects to gross about 5% of the $8 billion in sales that the corporation will chalk up this year, is shifting its focus to a mainstream market and a bulk complementary-MOS process now in development.

This decision took more than a reshuffling of top management; it practically called for a new deck. Robert S. Pepper was recruited almost a year ago while vice president and general manager of Analog Devices Inc.'s Semiconductor division in Wilmington, Mass., to replace Bernard V. Vonderschmitt [*Electronics*, Aug. 2, 1979, p. 46].

Then, less than a month ago, Carm Santoro left American Microsystems Inc., where he was senior vice president, to supplant Carl Turner as RCA's vice president in charge of integrated circuits. And even more recently, Ralph Simon stepped down to be replaced by Erich Burlefinger, previously general manager of ITT Semiconductors in Great Britain, as the division's vice president for electro-optics and power device operations.

The division's energies had been sapped by the elusive goal of cheap sapphire—still a contradiction in terms. By drawing thin ribbons of the semiprecious material from the melt, RCA hoped to bring sapphire substrate costs to within 20% of those of bulk silicon wafers. Ultimately, it intended to convert to square-wafer-handling equipment for 30% more dice per wafer.

Ribbon goals unmet. RCA projected that it would be pulling 100,000 ribbons by this year and three times that many by 1983. Those goals will not be met. Still unable to handle square wafers at its Mountaintop, Pa., ribbon-growing facility, it continues to grind the squares into circles. It was also anticipating ribbons of high enough quality to allow epitaxial layers to be grown directly

Pushing it out. General manager Robert S. Pepper says, "Success hinges on taking the product out the door on a timely basis."

Out of the West. Carm Santoro, who joined RCA from AMI, says, "C-MOS will be a winner and RCA is dominantly a C-MOS house."

upon them, thus skipping a surface polish. Pepper explains, "There was a thrust to go to 4-inch [ribbons], but I said let's wait and up the quality on the 3-in."

Pepper estimates that the SOS trip set the division back about two years in terms of working with bulk. But, he asserts, "we don't intend to stay behind for very much longer—we're not behind when it comes to process technology. SOS appeared to have tremendous speed and density advantages, and maybe at submicron geometries it will be back to sapphire. But we're still at 3, 4, and 5 microns." He admits that SOS does not make sense "unless you must have the speed or the radiation hardening—in sum, SOS will no longer be tried for commodity parts."

Big spending. The new team is determined to pick up the pieces. Indeed, corporate finance has already doubled the division's capital budget for 1980 over 1979. While being wooed by RCA, "I asked [chairman Edgar H.] Griffiths some direct questions," says Pepper. "He said, 'RCA has to be a leader in electronics. Its board and stockholders perceive it as a leader in electronics.' " Santoro adds, "You have to be a components company to be a successful electronics company. The commitments are here. It doesn't make sense to bring in some heavyweight people and then tie their hands."

Back in 1978, the division said it would produce—cost-effectively on sapphire—a 4-K static random-access memory, a 16-K static RAM in 1979, a 32-bit microprocessor by the early 1980s and, by 1983, chips with a million active devices.

But only the 4-K RAM went into production. The company says it is pushing thousands of these per month out the door today, but another promise of SOS was for speed—about five times that possible with bulk C-MOS. But while companies like Hitachi Ltd. have broken the 55-nanosecond barrier with their bulk 4-K parts, RCA's replacement for the 2114 plods along with its 650-ns maximum access time.

The division said that it was developing a floating-gate process for ultraviolet-light–erasable read-only memories and that it would deliver 16-K erasable programmable ROMs by last year. It also hoped to have a 32-K mask-programmable C-MOS ROM in 1979 and a 128-K chip this year. Those hopes turned out to be no more than that.

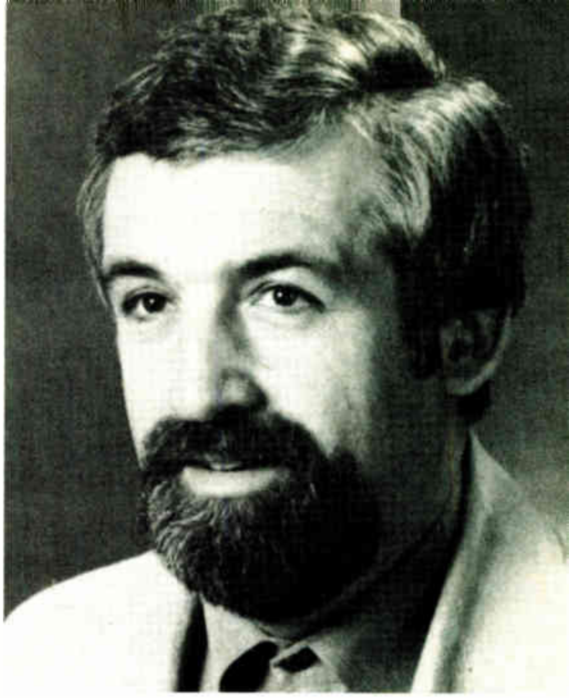
Micros successful. As for microprocessors, the company's proprietary 8-bit 1802, second-sourced by Solid State Scientific Inc. of Montgomeryville, Pa., and Hughes Aircraft Co.'s Solid State division in Newport Beach, Calif., has certainly been successful. However, it is built with a bulk C-MOS process called C^2L (for closed-cell logic) and, until recently, the device was basically alone in the field.

But again, in SOS, the firm pledged a single-chip version of the 1802—the 1804—and, through a technology swap with Intel Corp., it was to put the 8048 single-chip microcomputer and the 8085 8-bit microprocessor on sapphire last year. It did not happen that way and, losing faith in SOS, Intel is said to be working all out on its own high-performance C-MOS process.

"We terminated the 8085 project after we got some working parts," states Pepper. "It's not the thing for SOS. The 1804 is alive and viable in Somerville, but we are undergoing a major program to convert it from sapphire to bulk." He was disappointed to discover that "you can't just take a mask set and put it into bulk. I still think we can generate an algorithm to translate from one into the other, but it may be that we do the whole thing over."

The recast 1804 will, in fact, be the first of RCA's chips to sport the new bulk process. "We have just made that commitment with the labs [in Princeton, N. J.] and the Tech Center [the Advanced Technology Center in Somerville] and we expect production quantities in 18 months. I would like to cut that to a year."

The 16-bit question. In looking to the future, Pepper is unsure what RCA will be doing for a 16-bit microprocessor. "We've got to have a 16-bit machine. We've looked at the question of whether we should fashion one after the 1802 or whether we will act as a second source," says Pepper. However, it is unlikely that RCA will back the development effort needed to market its own 16-bit microprocessor this late and instead will be a second source.



From Europe. Erich Burlefinger, from ITT Semiconductor in England, will head electro-optics power device operations at RCA.

C-MOSI, a quick name given to the new process, will use oxide isolation and 5-micrometer-minimum features. Pepper says that it will resemble the Iso-CMOS pioneered by Mitel Semiconductor Inc., Kanata, Ont., Canada. C-MOS I will later be scaled to 3 μm and become C-MOS II.

Scaling was the bugaboo with C^2L and the reason why that bulk process will not be prolonged. Says Pepper: "We couldn't scale it below 5 microns and we want a process that clearly goes to 3 microns and beyond."

It is rumored—and not denied by Pepper—that the division recently purchased a mask set from Toshiba Corp. for an improved 4-K static RAM, which the new managers also have scheduled for production. Pepper characterizes the RAM as "nice-looking." He adds, "We have a shot at getting it into the marketplace this year—or definitely next."

A sense of purpose now runs high at the division. "There are incredible resources here," says Pepper, refering to the people at the labs and the tech center. "I'm still peeling the onion." He is working hard to coordinate research and production, realizing that "The success of a semiconductor company hinges on getting the product out on a timely basis."

"We had more processes than manufacturing could absorb here," he observed. Downplaying SOS and emphasizing its new oxide-isolated bulk process should take care of that problem, though. Other jobs in the queue for the general manager include upgrading in the wafer fabrication area, with more equipment for environmental control and more mechanization of offshore manufacturing and testing.

Santoro, too, has a positive approach to the manufacturing problems that have been preventing the corporation from getting products out of the door. "RCA has conceptualized a lot, but has not mobilized these ideas," the 39-year-old Santoro observes. "There's a wealth of C-MOS capability here that needs to be marshaled. Over the long term, C-MOS will be a winner, and RCA is dominantly a C-MOS house."

AMI-trained. Santoro, who holds a Ph.D. in solid-state physics from Rensselaer Polytechnic Institute, Troy, N. Y., was the very man who ordered the demise of V-groove MOS at American Microsystems Inc. "V-MOS was a good idea when we got into it, and it was a good idea when we got out," he recalls.

"I bring conceptual development experience and high-volume manufacturing management ability to the party," Santoro says, adding that "disciplined creativity is the key to semiconductor business." In which areas does he see this disciplined creativity being put to work? "Telecommunications and automotive electronics," he replies. "Telecommunications has become an absorber and a driver for the semiconductor industry. If RCA couples that with auto industry needs, it will maintain a dominant position in the industry."

As the third in RCA Solid State's management trio, Erich Burlefinger, 41, division vice president for electro-optics and power devices, will be responsible for the engineering manufacturing, and marketing functions for electro-optic devices, closed-circuit video equipment, discrete power semiconductors, microprocessor development systems, and single-board computers.

Simon had already bootstrapped the electro-optics product line into the black for the division, and Burlefinger will go on to enhance the power semiconductor capability of the operation. "We should be doing a fine job in power [devices] and we're not," says Pepper. "Erich can do that. He's a bright, articulate guy and a strong team builder." □

Sapphire moves further into the future

The use of sapphire substrates for building complementary-MOS (or even just n-channel) circuits has been pursued for more than a decade because of its promise—in theory, at least—of denser circuits and greater switching speeds than the usual bulk-silicon processes. Sapphire is an insulator, so that transistors residing in wells formed in a silicon epitaxial layer on the sapphire are automatically isolated from each other. That eliminates both the need for space-consuming oxide between devices and the circuit-slowing capacitance resulting from reverse-biasing pn junctions for isolation.

But it has not proved easy to exploit sapphire. Unexpected problems, especially in the silicon-sapphire interface, have not only made the process far more difficult than standard bulk C-MOS processes but have also cut into the performance advantages. Moreover, sapphire is an expensive insulator, costing hundreds of dollars per wafer, as opposed to a few dollars for silicon. As a result, nearly all semiconductor manufacturers have labeled SOS an exotic technology for only those applications in which—whether in speed, radiation hardness, or density—bulk C-MOS does not suffice. Finally, RCA Corp. has joined the pack and ceased trying to make sapphire fly in commodity products.

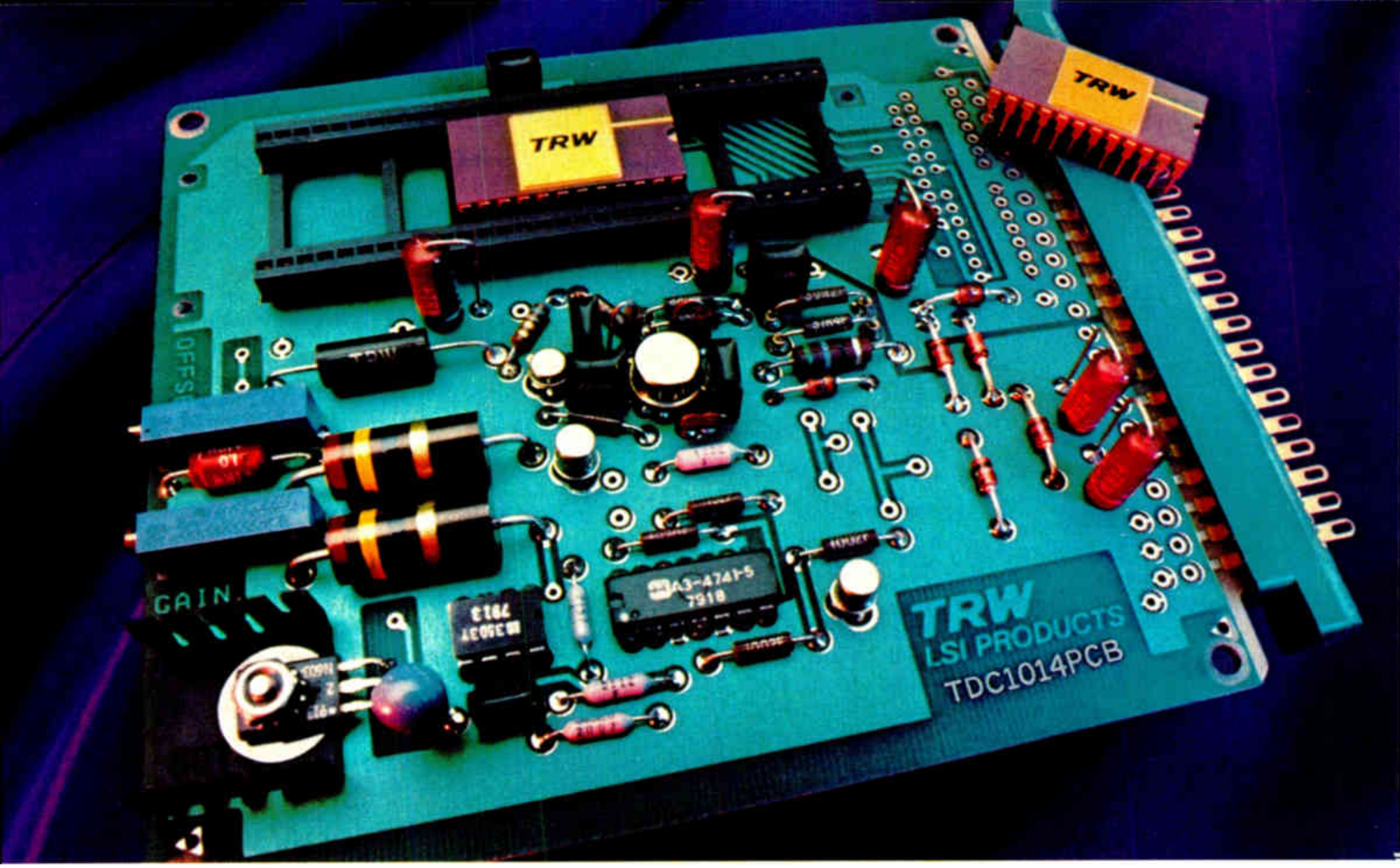
Probably most active in SOS is Rockwell International Corp. It has built many circuits for military applications that, by their speed and power specifications, reach into that range beyond bulk-silicon C-MOS performance. Its Anaheim, Calif., Microelectronics division, in fact, is bringing eight more SOS devices out of research and into final engineering design for limited production later this year. This gives Rockwell a total of 20 SOS devices for military and space customers, primarily such other Rockwell divisions as Collins Radio and Electronic Systems.

Most of these parts are intended for signal processing, where SOS speed and power advantages stand out, says Robert L. Doty, business director of military device products. Rockwell employs 4-micrometer line dimensions in production, but since SOS scales down well, he says, researchers are building devices with geometries down to 2 μm. An improved Viterbi decoder, for instance, packs 33,000 transistors into a 170-by-250-mil area [*Electronics*, Dec. 6, 1979, p. 42]. Apart from research, 80 to 90 people are involved in military SOS work.

However, Rockwell still has no timetable set for moving into commercial SOS, says Richard C. Pinto, division vice president and general manager for microelectronic devices. "Until now, it would have been an academic exercise and premature," with Rockwell lacking enough production experience and yield data, and with the work just at the point of gelling, he adds. But Pinto expects within five years that Rockwell SOS sales will have a 50-50 inside-outside mix.

Elsewhere, Hewlett-Packard Co., Cupertino, Calif., made a major commitment to SOS for microprocessors and other proprietary circuits it uses in its instruments and computers. But it now appears that HP may also be shifting its emphasis to bulk silicon. At a recent device research conference in Ithaca, N. Y., HP researchers presented a paper that painted a cloudy scenario for the future of SOS. In particular, it cited experiments on device saturation current, which ultimately determines MOS switching speeds in digital circuits. The results showed that bulk n-MOS at very short (0.5-μm) channel lengths attains 70% the theoretical limit, whereas at the same channel length, n-MOS on sapphire reaches only 55% and p-MOS on sapphire only 42%. Those findings could explain why, although HP is currently in production with its second-generation (4-μm features) metal-gate SOS process, it has reportedly put a hold on producing a third-generation process—silicon-gate C-MOS on sapphire with 2.5- to 3-μm features. HP confirms that it has "chosen not to pursue development of its next-generation process at this time, but for business—not technological reasons." HP adds that more SOS devices will be used in various products.

-Raymond P. Capece



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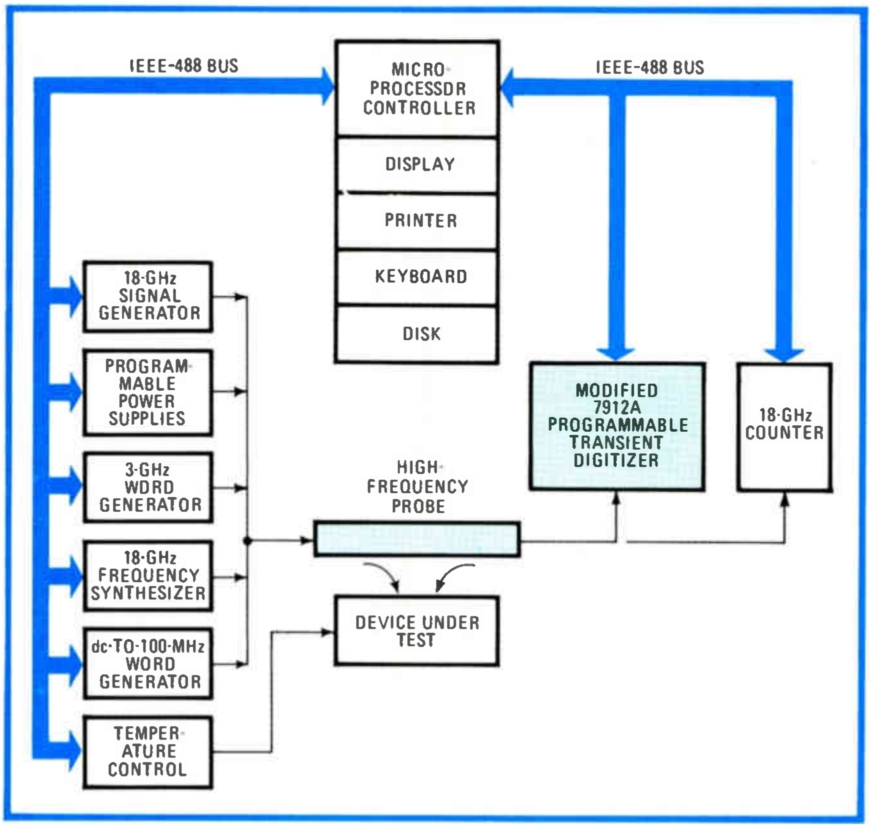
Measurement science is catching up

High-speed signals of new ICs have labs pushing resolutions of test devices down to a few picoseconds or less

by Richard W. Comerford, Test, Measurement & Control Editor

With the speed of commercial integrated circuits breaking into the nanosecond region, both commercial and research facilities are looking for new ways of accurately and repeatably measuring the high-speed signals produced. At Lockheed Missile and Space Corp.'s Palo Alto (Calif.) Research Laboratory; Tektronix Inc. in Beaverton, Ore.; the National Bureau of Standards in Boulder, Colo.; International Business Machines Corp.'s Thomas J. Watson Research Center in Yorktown Heights, N. Y.; and other such facilities, workers are pushing measurement resolutions down to a few picoseconds or less.

To test gallium arsenide devices, researchers at Lockheed's Microelectronics Center in Sunnyvale, Calif., have used IEEE-488–compatible instrumentation to build a system for testing wafers of large-scale integrated circuits. The system, shown below, has at its heart a Tektronix 7912A digitizer modified by Ray Smith of the company's research lab to work at a minimum bandwidth of 3.5 gigahertz.



Home brew. Researchers at Lockheed's Microelectronics Center in Sunnyvale, Calif., built this system to test the operation of next-generation high-speed integrated circuits.

Smith's modifications involved changes to the input and output electronics, which resulted in "pushing the [scan converter] tube a bit," the physicist notes, without changing its internal electronics. Smith, who emphasizes that the basic 7912A is a fine instrument, says the change in the unit's vertical input amplification scheme was simple: "We threw it out," he explains. The amplifier limited the 7912A's bandwidth to about 500 megahertz or, at what Smith calls a "brutal" sensitivity of 4 volts/division, to 1 GHz.

The next limiting factor, the tube's native 2.5-GHz bandwidth, was overcome by equalization—attenuating the low-frequency response so that it matched the high-frequency response. Referring to the techniques used in long-distance cable transmission, Smith says, "Usually that's done passively. What we've done is to apply it to the microwave region and we've done so without using an amplifier." The actual circuit details are proprietary, but Lockheed will modify one or two units on an accommodation basis at cost, currently about $15,000.

Without input amplification, it might be expected that the sensitivity of the unit would be extremely low. But to his surprise, Smith found that it was not deflection but the correct location of a trace's charge center that was essential to a digitizing instrument's operation. Finding that center by integrating the trace, as is done in phased-array sonar, resulted in a 2-millivolt sensitivity and an 8-V input range. Signals could therefore be digitized with 12-bit accuracy.

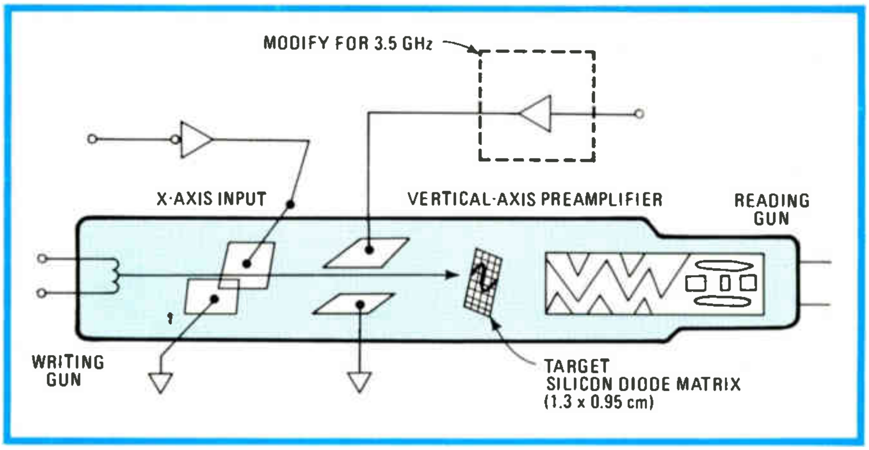
About a year ago, Smith presented his findings and their result to Tektronix—which verified the modified unit's operation—and offered the company the rights to incorporate the changes. But the timing was not right, according to Jim Cavaretto, business unit manager for signal-processing laboratory oscilloscopes at Tektronix. The company had just spent a lot of time adding programmability and processing capability to the unit, turning it into the 7912AD version, to which Smith's modifications are not readily applicable.

"At the time he approached us," Cavaretto also notes, "we didn't have enough information to determine if we should turn right around and produce another product." Then too, Smith's modifications reduced the 7912's overall throughput—the time it takes to store as well as digitize waveforms—which Cavaretto feels is essential to a general-purpose instrument.

But with the success of instruments like the 7104 1-GHz oscilloscope, Tektronix sees the need to push on. "We're already getting questions and comments that lead us to believe that 1 GHz is certainly not the stopping point," Cavaretto says, and he thinks that scan conversion will be the way to go.

But the silicon target now used in the digitizer "has some inherent limitations in terms of signal-to-noise ratio," he notes, so "in the future, CCD targets may become the vehicle." The charge-coupled devices would be used much as in vidicon cameras today. Then, too, a general-purpose instrument will require high-speed input amplifiers that provide a range of sensitivities, and for that Cavaretto leans toward LSI GaAs devices. "But trying to extend waveform measurement capabilities well into the gigahertz region, regardless of which technology one chooses, is not going to come easily or cheaply," he cautions.

Looking out. While he may come down on the side of direct-reading instruments that use transferred-electron devices and GaAs, Cavaretto keeps a sharp eye on sampling technologies that may up measurement capability, including those based on Josephson devices. "We've spoken with IBM concerning that technology and their need for extremely precise measurement, and we're continuing to try and mold that into a product development strategy."



Scan converter. The heart of the 7912A digitizer was modified to increase the operating speed. Such tubes will probably be even further modified, using GaAs devices and CCDs.

IBM's Josephson work is still centered in its research center at Yorktown Heights, and spokesmen for the company continue to stress that the work is experimental. But IBM's recent slew of discussions about Josephson devices could indicate that the move from experimental to rental is not far off. And though the work is essentially devoted to computer efforts, the company also sees its importance to metrology. In fact, the company's most recent announcements have dealt primarily with such applications.

For example, the most recent IBM Josephson announcement has been the experimental demonstration of an ultrashort-pulse generator that makes possible a novel sampling technique for on-chip measurements. Sadeg Faris, the IBM research staff member responsible for the new measuring scheme, explains that for the experiment two pulse generators and a sampling gate were integrated onto a single Josephson chip. The generators were used alternately to provide sample gate triggers and test signals, with the result that "what we measure and what we predict from simulation agree very well," notes Faris happily.

The present circuit's sampling gate has a plasma frequency whose period is about 2 ps. "The plasma frequency really determines the [measurement] bandwidth in our scheme," Faris notes, "it has the capacitance of the device in it. We can make devices that ultimately have zero capacitance—Josephson weak links. Using materials with high temperature coefficients like niobium-germanium, the resolution can be about 0.1 ps."

9 ps at NBS. Similar work is being carried out at the National Bureau of Standards in Boulder. There, researchers have constructed measurement systems using supercooled Josephson logic circuits and a sampling oscilloscope. The sampling system is able to measure with a resolution of 9 ps, three times faster than the sampling scope alone.

Now, the detector on the NBS's supercooled logic must communicate with the sampling logic in the room-temperature scope, unlike the integrated logic that IBM has built. "Since IBM did that [integration] work, we're taking a slightly different direction," says NBS researcher Clark Hamilton. Like IBM, the NBS is headed toward a system that will measure signals transmitted to it from a room-temperature source, work that should be completed in the next few months, Hamilton says.

But IBM does not plan to let the NBS stake out new territory without a fight. Faris notes that work in this direction is also beig done at IBM. He will not say when it is likely to bear fruit, adding that "all I can say is that it's do-able." And though he cannot tie a dollar figure to this type of equipment, he says that "it is practical for most laboratories to do it—I think the semiconductor people, who already have most of the equipment for Josephson device fabrication, should get into it." □

Technical articles

Low-power EE-PROM can be reprogrammed fast

C-MOS peripheral circuitry surrounds n-MOS array in which electrons tunnel to and from floating gates

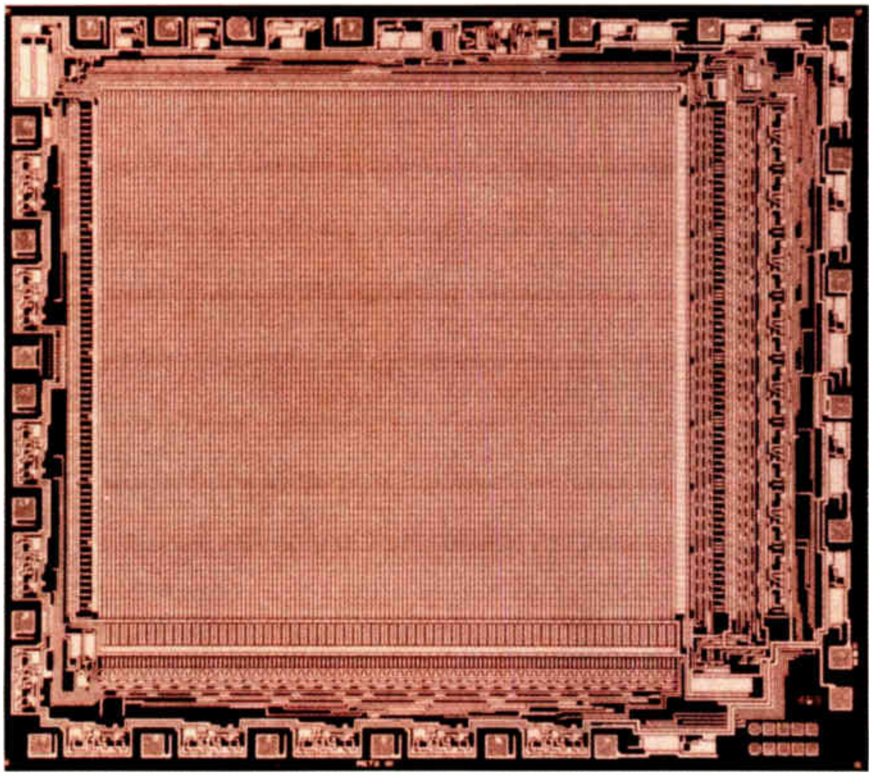
by E. K. Shelton, *Hughes Aircraft Co., Hughes Research Center, Newport Beach, Calif.*

☐ When it comes to in-circuit reprogramming, an electrically erasable memory is inherently more convenient than one that must be cleared with ultraviolet light. So it is only a matter of time before the UV-erasable programmable read-only memory, or E-PROM, relinquishes some of its substantial market share to the EE-PROM.

In addition to electrical erasure, a new 8-K EE-PROM has two other assets—low power consumption and low current requirements for erasing and programming—that make it particularly attractive for portable applications like hand-held instruments. It can also be programmed very quickly, in about 0.1 second, since bulk erasure and byte programming typically require only 100 microseconds each. Access time is less than 600 nanoseconds.

The HNVM 3008 owes its low power consumption to the choice of complementary-MOS technology for its peripheral circuitry, which surrounds a high-density n-MOS memory-cell array. Density is achieved by merging storage and select transistors; nitride is used only to enhance coupling between the two. The chip's n-type substrate contains a large p-type well comprising 8,192 bits of nonvolatile storage, seen from the outside as 1,024 bytes. Outside this well, p-channel transistors reside in the substrate and n-channel devices are fabricated in other, smaller p-type wells, just as in standard C-MOS chips.

The device typically consumes only 25 milliwatts during programming and erasing, 10 mW during reading, and less than 500 microwatts on standby. These figures reflect the use of electron tunneling as the mechanism of charge transfer and the efficiency of the C-MOS circuitry as well. Metal-nitride-oxide-semiconductor EE-PROMs also employ electron tunneling, but they require a pro-

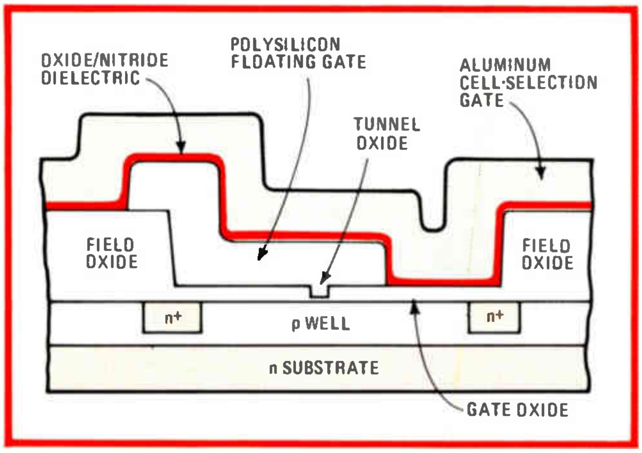


1. C-MOS EE-PROM. With C-MOS peripheral circuitry and a dense n-channel array, this nonvolatile memory needs little power. The cells use a floating gate for the highest retention and, for the best endurance, charge is transferred by tunneling electrons.

gramming voltage of at least 25 volts. In contrast, the HNVM 3008 requires 17 V for programming and erasing; for any other purposes, the voltage on its single power supply pin is 5 V.

The use of a floating gate as the storage element optimizes the new circuit's memory retention, estimated at 10 years at 125°C. The combination of tunneling and floating gates provides both excellent retention and minimal degradation with repeated erasing and programming cycles, estimated in this case at an endurance of more than 10^5 cycles.

The chip's pinout is similar to that of the 2708 E-PROM, the 2308 mask-programmable ROM, and the Hughes HCMP 1834 mask ROM.



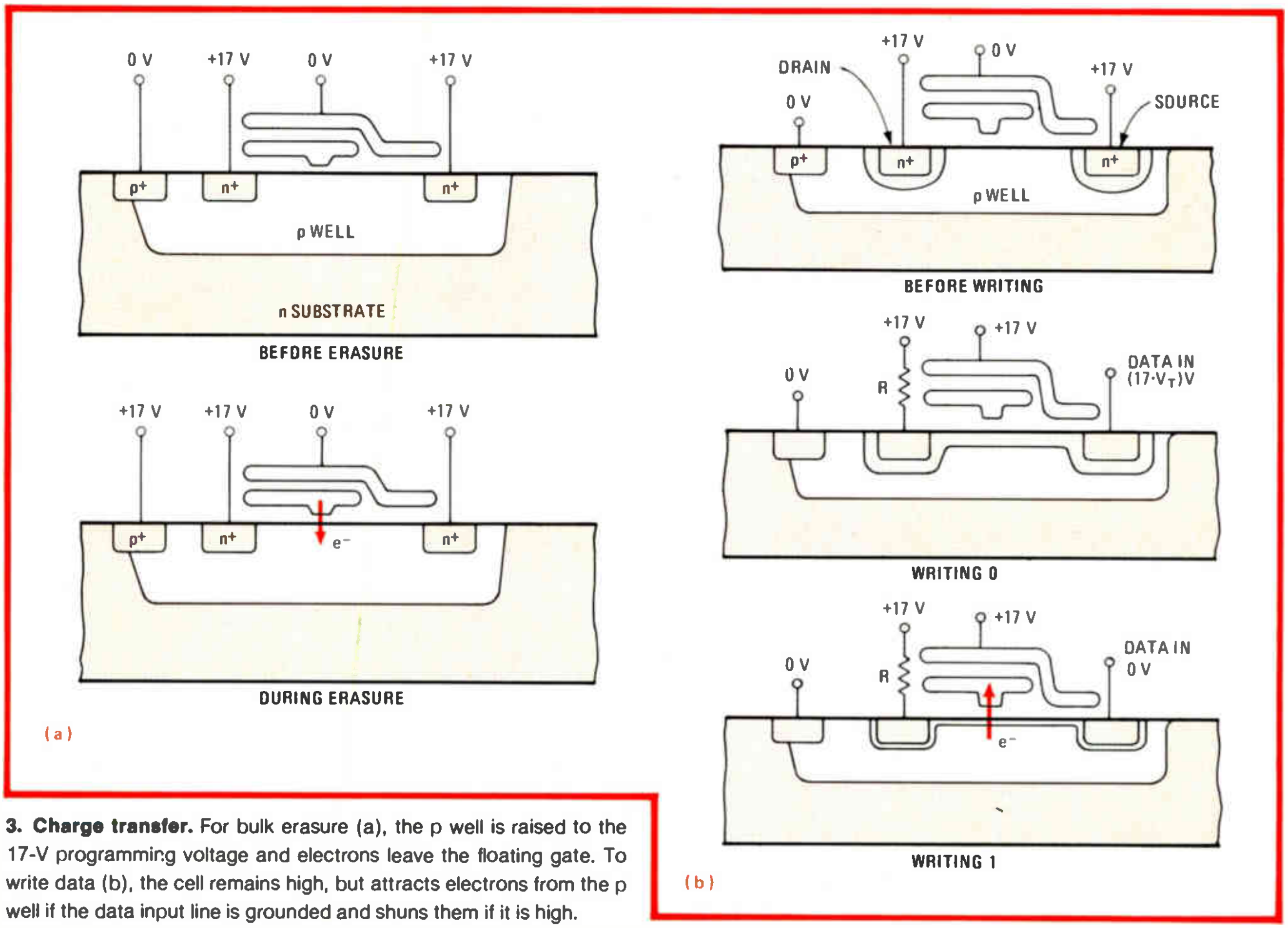
2. Thin oxide. On the left half of the transistor, polysilicon forms a floating gate. Above this rests an aluminum control gate that also extends to the right where it serves as a cell-selection gate. A thin nitride-oxide sandwich enhances capacitive coupling.

Why the floating gate?

In floating-gate structures like E-PROMs, charge is stored on an electrically isolated gate electrode and erased with ultraviolet light. MNOS memories, on the other hand, trap charge at the nitride-oxide interface and are electrically erased and programmed. E-PROM floating-gate devices retain charge better than MNOS devices because the stored charge is isolated with a thicker oxide.

To make a floating-gate device electrically erasable in a manner similar to an MNOS memory, a thin tunnel oxide must be present. However, this layer need not be nearly as thin in a floating-gate cell (less than 200 angstroms versus about 25 Å for MNOS), so charge will not leak off as quickly. In fact, a floating-gate device should have approximately 100 times better data retention than an MNOS structure.

To transfer charge, MNOS structures use an electron-tunneling mechanism. This requires such a thin oxide that early electrically programmed floating-gate structures avoided the technique. Instead, they opted for techniques such as avalanche injection of charge through a thicker oxide, despite the fact that this mechanism



3. Charge transfer. For bulk erasure (a), the p well is raised to the 17-V programming voltage and electrons leave the floating gate. To write data (b), the cell remains high, but attracts electrons from the p well if the data input line is grounded and shuns them if it is high.

Thin oxides gain wide appeal

Thin tunnel oxides and polysilicon floating gates appear to be a winning combination for EE-PROMs. The thin layer enables bidirectional electron tunneling to be used in lieu of harsh avalanche injection for charge transfer, and the floating gate may replace, as a storage node, a nitride-oxide sandwich that demands an even thinner oxide for the same programming voltage and is hence more prone to leakage.

Intel Corp. of Santa Clara, Calif., recently used a process similar to Hughes' called Flotox to build a 16-K EE-PROM compatible with the ultraviolet-light-erasable 2716 E-PROM [*Electronics*, Feb. 28, p. 113]. Flotox stands for floating-gate tunnel oxide. The two processes are similar, as shown in the cross sections below. A major difference is that Intel uses two MOS transistors per cell (the cell-select device is not shown), whereas Hughes has merged these into a single device. In each case an oxide layer less than 200 angstroms thick serves as a valve for electron traffic to and from a floating polysilicon gate.

Both Intel and Hughes use a second, capacitively coupled control layer to alter the potential of the floating gate. For instance, by pulling the overlapping control gate to a high voltage, the floating gate voltage rises, and electrons hop the thin oxide and become trapped. Some minor differences here include Intel's use of polysilicon for the control level versus Hughes' use of metal and its inclusion of silicon nitride to enhance the capacitive coupling between the control gate and the floating gate.

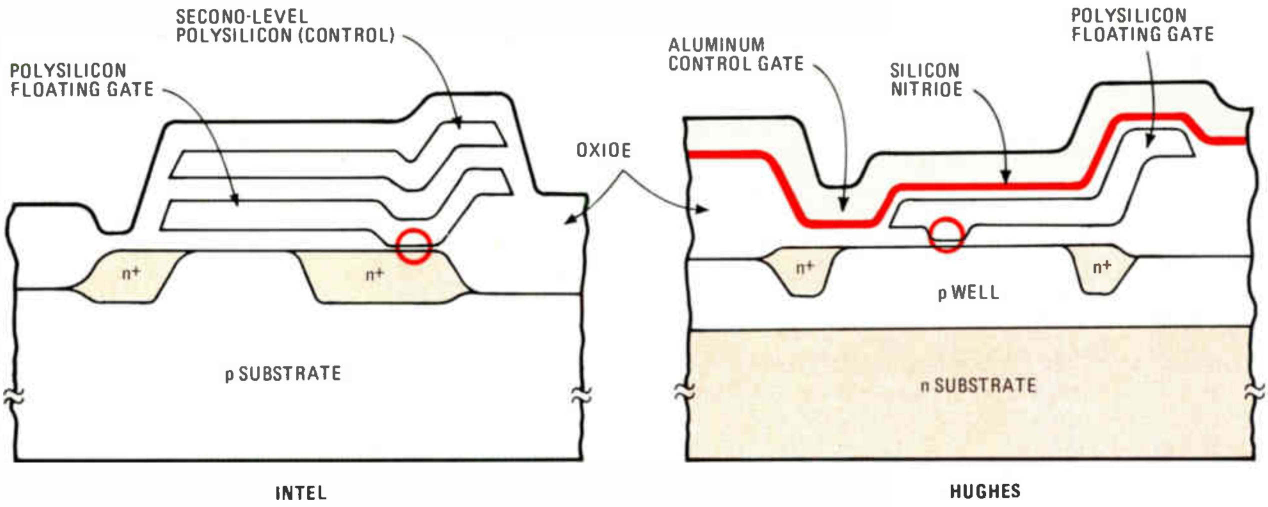
Intel's thin oxide is grown on a heavily doped n^+ region, whereas Hughes' is over the lightly doped p well. Growth over a heavily doped region may be more difficult since some impurities may wind up in the tunnel oxide. However, by placing the tunnel oxide over its n^+ drain region, Intel is able to offer single-byte erasure, a feature that Hughes wants to add at a later date. To erase a cell, Intel grounds the control electrode with the drain positive and electrons jump the gap and leave the floating gate. In contrast, Hughes must raise the potential of its entire p well, thus forgoing individual cell control.

Motorola has a series of tunnel-oxide EE-PROMs planned and is predicting that its cells will be 20% to 30% more compact than Flotox cells. Theoretically, if thin oxide could be made thin enough, all operations—including programming—could be accomplished with a single +5-V supply or, more likely, with a high voltage generated on chip. Alternatively, Xicor Inc. of Sunnyvale, Calif., has shown that a somewhat thicker oxide will also support low-voltage tunneling if it is carefully grown on rough-textured polysilicon.

Metal-nitride-oxide-semiconductor, or MNOS, devices use an even thinner tunnel oxide, but since charge in them is bound at the nitride-oxide interface and so is not mobile, the superthin layer need not be perfect. Indeed, MNOS cells can have a few pinholes in their thin oxide with no ill effects. In contrast, since the charge stored in a floating gate is mobile, a pinhole in its thin oxide would behave as a low-resistance pipe, rendering the cell useless. The closer tunnel oxide growth comes to perfection, however, the more likely are the MNOS nitride-oxide sandwiches to be replaced with floating polysilicon gates.

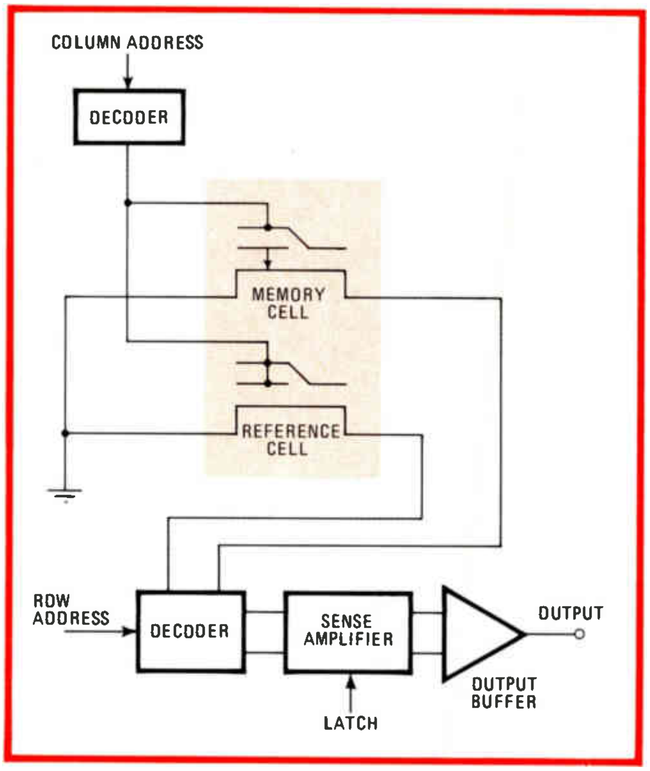
Nevertheless, MNOS replacements for E-PROMs are surfacing. Hitachi Ltd. is now supplying samples of a 2716-compatible EE-PROM called the HN48016. It does not feature byte erasing, but its price is very aggressive—only $70 a unit in quantities of 100. Intel's 2816 is going for 8 to 10 times the price of a 2716, which ranges from $7 to $20. General Instrument Corp. of Hicksville, N. Y., which is now switching from a p-channel to an n-channel MNOS process, is also eyeing the E-PROM replacement market.

-John G. Posa



degrades with successive erasing and programming cycles—in other words, it exhibits poor endurance. A floating gate combined with a thin tunnel oxide provides the best endurance and retention.

Since electron tunneling within a floating-gate structure appeared to be the best arrangement for electrically erasable PROMs, Hughes undertook an extensive three-year program to develop a reliable, high-yield tunnel-oxide process and a floating-gate structure to support the charge-transfer mechanism. Along with these, a floating-gate process was developed, put into production, and subsequently applied to the development of a floating-



4. Comparator. The state of a memory cell is determined by comparing it with a reference cell that differs from it in having no tunnel oxide and a fixed threshold voltage. An output latch compares the conductances of the memory and reference cells.

gate memory cell. Various cells were designed and compared in terms of performance, reliability, and yield.

The cell finally selected is near optimum for retention and endurance. In comparison with MNOS, it produces a memory that retains data better by at least an order of magnitude and, as mentioned, can be programmed with a lower voltage.

A cross section of the cell is shown in Fig. 2. It consists of a single transistor having a split-gate structure. On the left side of the transistor is the dual-gate storage portion of the cell, formed by a polysilicon floating gate overlaid by an aluminum control gate. The aluminum layer also extends to the right, where it serves as a cell-select gate.

The polysilicon floating gate is isolated from the MOS channel beneath it by the tunnel oxide and the normal gate oxide and from the control gate above it by a nitride-oxide sandwich. This thin dielectric sandwich is crucial since it ensures such a strong capacitive coupling between the gates that 17 V is enough to charge and discharge the floating gate.

Reading and writing

A memory cell is erased as electrons tunnel from the polysilicon floating gate to the p well (Fig. 3a). This is done by first grounding the control gate and then raising the potential of the p well to the +17-V programming voltage. Electrons tunnel through the thin oxide, causing the floating gate to acquire a net positive charge.

This procedure is reversed to write data into an erased memory cell—that is, electrons are made to tunnel into the floating gate from the p well (Fig. 3b). The p well remains grounded during programming, but the drain of the memory cell transistor is connected through a load resistance to the programming voltage. The source is connected to either the programming voltage or ground, depending upon whether a 1 or a 0 is to be stored.

Next, to start the programming cycle, the gate is raised to +17 V. If the source potential is also +17 V (to program a 0), the transistor does not turn on, and the surface of the p well below the floating gate is depleted of electrons. Only a small potential difference then exists between the surface of the p well and the floating gate, so that no electrons tunnel into the gate. There is no change in the floating-gate potential and the cell remains erased in a 0 state.

On the other hand, if the source potential is 0 V (to program a 1), the transistor turns on. The surface potential under the floating gate drops to close to 0 V, and electrons from the inversion layer tunnel through the thin tunnel oxide and into the floating gate, causing it to require a net negative potential.

To the control gate, the charging and discharging of the floating gate look like changes in the threshold voltage of the memory transistor. For an erased cell, this threshold voltage is between −1 and −3 V; in the written state, the threshold is raised above normal to from +1 to +5 V.

The state of a storage location is determined by an output latch that compares the memory cell's conductance with a reference cell's (Fig. 4). The reference cell resembles the memory cell except that it has no tunnel oxide and its floating gate is tied to the control gate so that its threshold voltage remains fixed.

Easy activation

In the HNVM 3008 circuit, the erasing and programming operations are initiated by simply raising the supply voltage pin to the +17-V programming voltage and then applying TTL-level signals to the chip-enable ($\overline{CE}$) and output-enable ($\overline{OE}$) inputs. An internal voltage detector monitors the power-supply voltage level and, if it is elevated above about +8 V, automatically throws the chip into the erase-and-program mode. A logic low pulse on the $\overline{OE}$ input now causes bulk erasure of the memory, and a logic low pulse applied to $\overline{CE}$ programs the byte at the location selected by the address bus with the information present on the data bus. During erasure or programming, the output bus drivers are automatically turned off so that the raised supply voltage does not damage any devices connected to the E-PROM.

The HNVM 3008 is in the erase and program mode when the high-voltage line is high (true). As mentioned, this line will be true whenever the power supply voltage is above 8 V or so. At normal +5-V levels, $\overline{CE}$, $\overline{OE}$, and chip select (CS) are used to read the memory. CS and $\overline{OE}$ control the output drivers to the 8-bit data bus.

When CS is low and/or $\overline{OE}$ is high, the output drivers are disabled, or put into the high-impedance state, so that any of the devices attached to the common output bus may be selected independently. When $\overline{CE}$ goes low, the input address is held and the addressed data byte is latched into the output sense amplifiers. □

Development system puts two processors on speaking terms

Software for Intellec development systems interactively controls two in-circuit emulators so that interprocessor communications can be debugged more easily and with greater speed

by Christopher P. Zing, *Intel Corp., Santa Clara, Calif.*

☐ Dividing data-handling chores between two microprocessors—coprocessing—is becoming a common design approach because of the overall system benefits that it can provide. But translating such designs into hardware and software is not always easy: doubling the number of processors in a system can more than double the development effort, since it adds the twist of interprocessor communications.

To simplify the debugging of dual-processor designs, Intel has introduced Multi-ICE software for the 8085, 8049, and 8041A chips. This software package allows two in-circuit emulators (ICEs) resident in a host Intellec development system (Fig. 1) to operate synchronously under the user's control, thus providing him or her with information on how the two microprocessors being emulated would interact in the target system. With it, the user can isolate a problem involving two interacting processors even if the problem is intermittent. Of course, quick and easy modification of the program code for interacting processors promises to make multiple-processor system development less time-consuming.

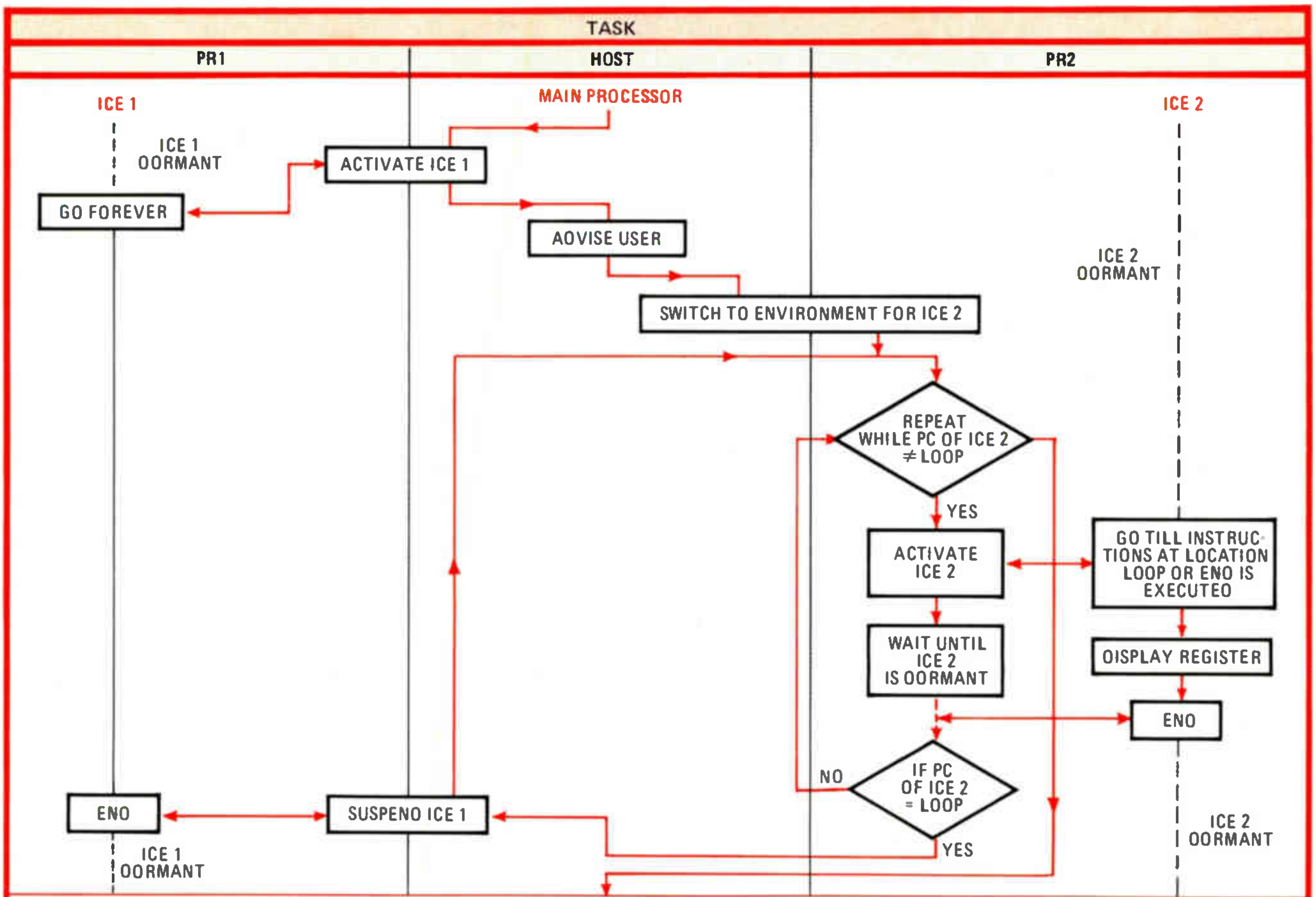
Pre-Multi-ICE

To realize coprocessor designs before Multi-ICE, designers basically had two techniques for debugging their systems: sequential emulation, using a single emulator for one processor and then the other, or asynchronous dual-processor emulation. Each of these techniques has its drawbacks.

To design interprocessor communications when only a single development system and emulator are available requires a piecemeal approach. The untested software for one processor is placed in firmware—usually an erasable programmable read-only memory—in order to give the second processor a unit to talk to. Then the second processor is emulated and the communication links are checked.

Since the first processor's program is fixed in E-PROM,

1. Double duty. With Multi-ICE software, the Intellec development system shown is able to interactively control the operation of two in-circuit emulators, such as the ICE-49 and -85, so that interprocessor communications may be examined with greater ease.




```
*ACTIVATE PR1                    ; Activate ICE 1; environment EN1 assumed by default
. *GO FROM 800                   ; Start ICE 1 at instruction cycle 800
. *END                           ; End of ACTIVATE block
PR1 EMULATION BEGUN              ; System advice to user
*SWI = EN2                       ; Switch execution environment to EN2
*REPEAT                          ; Repeat the following block of commands while the program counter is not equal to LOOP
*WHILE PC <> LOOP                ; LOOP is the symbol for an instruction or fault condition that the user wants to detect
. *ACT PR2                       ; Activate PR2 (the host recognizes the first three letters as the key word ACTIVATE)
. . *GO TILL .LOOP OR .END       ; Go till instruction at location LOOP or at location END is executed
. . *REGISTER                    ; Display the registers
. . *END                         ; End of ACT block
. *WAIT PR2                      ; Wait until PR2 is dormant
. *IF PC = .LOOP THEN
. . *SUSPEND PR1
. . *END                         ; End of IF block
. *END                           ; End of REPEAT block
```

2. Gadabout. With dual emulation, the Intellec's central processing unit spends its time ordering the three task sets shown above. The CPU's operating milieu is determined by the program at bottom, which has been written by a user in the Multi-ICE command language, Emula.

changes can be made easily only on the program in the emulated processor's memory, and the development system cannot observe and depict both systems at the same time. Therefore, when bugs exist the designer has to resort to a trial-and-error method—going back and forth between processors and changing emulator memory and E-PROMs until the system works.

With two development-emulation systems—or with one system that can handle two emulators—program changes can be made more readily, since both emulators and their programs are accessible to the user. However, a trial-and-error approach for finding and fixing bugs may still be needed, because the two in-circuit emulators cannot be controlled synchronously.

The most efficient way to develop a multiple-processor system is to use a software tool that lets processors be interactively controlled. The Multi-ICE package provides simultaneous support and control of two in-circuit emulators while sharing development system resources such as memory, peripherals, and console. It also permits hardware and software starts and stops to be synchronized by the user.

These synchronized operations are useful for debugging. The user can establish software or hardware stop conditions for the processors such that, say, they both trigger at a particular fault condition, and then he or she can review the logic trace in both emulators from the time of a handshake until the fault appears. With parallel trace records from both ICE modules, he or she can quickly zero in on the communications problem.

Using dual-processor emulation, a designer can test programs with a minimal amount of hardware—just a

Why two processors are better than one

Despite the added complexity that making two processors talk to each other can bring, designers are finding several reasons to turn to dual-processor designs. For one, the price of processors has dropped to the point where it makes economical sense to partition a product into several functional areas, each with its own processor. The separation shortens development time, since different groups can work in parallel on individual areas. The shorter development time means that products can bring a return on investment sooner. Further, this functional segmentation permits the generation of standard, proprietary circuits that can be used in a number of different products requiring those functions, thus reducing a company's total design cost as well as its engineering effort.

Equally significant is the fact that these designs do not limit the overall system performance to the maximum throughput of a single central processing unit. Handing off more mundane tasks to an intelligent peripheral controller like the 8041A frees the CPU for more complex tasks that it alone can perform efficiently. One pocket-sized data-entry terminal, for example, uses the CPU to interpret data entered by way of a keypad and a peripheral processor to establish communication with a data base via telephone. With two processors, the system operates faster, the operator experiences less real-time delay, and telephone costs are reduced.

printed-circuit board with bus lines, for example. Running the programs from the emulator memory using two in-circuit emulators, he or she can study the operation at key points to determine if the communication software is running smoothly.

Achieving joint control

To obtain these capabilities, Intel's Multi-ICE software configures the Intellec development system so that its main processor can perform different sets of tasks in three different modes, or environments. Two sets of tasks, processes PR1 and PR2, interface the development system's main processor with two ICE modules, which emulate the processors designated 1 and 2, respectively. In performing these tasks, the main processor can be regarded as operating in the ICE 1 or ICE 2 environments (EN1 and EN2, respectively).

The third set of tasks lets the development system and the user communicate and controls the synchronization of the other two sets of tasks. This last set is referred to as the host set and is performed in the host environment.

A general understanding of how the main processor performs in each of these modes can be gained from Fig. 2. Here, a program operating under Multi-ICE software controls the activities of two emulators in accordance with the flow diagram. When a fault occurs, both processors are stopped so that the source of the error can be located.

In this example, the main processor, initially running in the host mode, is switched to the EN1 environment. After giving instructions to the emulator associated with PR1 (start at 800), the main processor leaves this emulator (ICE 1) to run in its environment (EN1), returns to the host mode, communicates status information to the user, and reads the next instruction, which switches it to the EN2 mode.

Under the EN2 environment, emulator 2 is instructed via the main processor to perform a repeat routine. At the start of each cycle of the routine, the main processor checks the program counter (PC) of ICE 2 to see whether its value is equal to that of the symbolic location LOOP. LOOP is a macrocommand defined by the user and may, in this instance, correspond to a fault condition or data-transfer point that needs to be analyzed.

The result of this check determines how the main processor should proceed. If the program counter is not equal to LOOP, ICE 2 is activated and runs until it executes the instruction at LOOP or END, at which point the processor stops. Meanwhile, the main processor waits until emulator 2 goes dormant, and if it does so because the LOOP and program counter values are equal (that is, if the last instruction performed was the LOOP instruction), the main processor deactivates ICE 1 and returns to the host mode. Thus the user can now communicate with the main processor and call information from the trace memories of both ICEs, triggered at the same point, to evaluate the steps leading up to the LOOP state. He or she can do this by looking at the traces simultaneously on the development system's cathode-ray-tube display or by printing them out for later study.

The program also permits the user to search for intermittent faults. If the program counter and LOOP values are not equivalent after any pass, the main processor continues to exercise ICE 2 while ICE 1 keeps running. Since this process could go on indefinitely if the fault were particularly infrequent, a KILL command is provided that lets the user exit a test routine and return to the host environment. The record prior to the KILL command is available in trace memory for diagnosis.

For real

Multi-ICE software has proven invaluable in simplifying designs using Intel products such as the iSBC 80/30 single-board computers. For example, consider the case where the iSBC 80/30 is used for processing and sends the result to a light-emitting-diode display located on another board.

The iSBC 80/30 uses its 8085 to execute applications programs and its 8041A to control a seven-segment driver for the LED display. In essence, the 8041A reads ASCII characters sent to its data-bus buffer by the 8085, decodes them, and formats them for display. Therefore, when the wrong character is shown, it is necessary to determine if the problem lies in the 8085, the 8041, their firmware, or the link between them.

This determination can be made by replacing both processors with their respective ICE modules, storing their source programs in the Intellec system's random-access memory, and running an emulation of the target system's operation. If the problem does not recur after

```
-8541                                   ; Define system being emulated

ISIS-II MULTI-ICE 85/41

* ACTIVATE PR2
*. LOAD 41PROG.AGX                      ; Execution list for PR2 (the 8041) loads program and emulates
*. GO FROM IBFULL
*. ENDACTIVATE

* ACTIVATE PR1
*. LOAD 85PROG.DBG                      ; Load 8085 program
*. DEFINE .CHAR = 0                     ; Define Emula variable, CHAR
*. REPEAT
*.. RB = .CHAR                          ; In each loop, register B = CHAR
*.. GO FROM .XMIT TIL .THEND            ; Emulate the 8085 program
*.. .CHAR = .CHAR+1                     ; Increment CHAR
*.. COUNT 15000                         ; Timing count
*..; ENDCOUNT
*.. WHILE .CHAR <= 0FFH                 ; Repeat loop for CHAR through 255
*.. ENDREPEAT
*. ENDACTIVATE
```

(a)

```
IBFULL:   SEL   RB1       ; Enter CHAR from data-bus
          IN    A,DBB       buffer, wait until received
          .
          .               ; Decode and display routine
          .                 borrowed from application code
          .
          .
CNTNU:    NOP             ; Send acknowledgment of receipt
          .                 to 8085
          .
          .
          JMP   IBFULL    ; Loop indefinitely
```

(b)

```
; On entry, register B contains the character to be displayed

XMIT:     MOV   A, B      ; Move register B to register A
          OUT   0A0H      ; Send register A to port A0(16)
READY:    IN    0A1H      ; Enter port A1(16) to register A
          ANI   02H       ; Has the 8041 acknowledged receipt?
          JNZ   READY     ;       No, not yet
THEND:    HLT             ;       Yes
```

(c)

3. If it's hard. The three programs above let users find hard errors in the transmission of numbers from an 8085 to an 8041A on an iSBC 80/30 single-board computer. Program (a) sets up the ICE-85 and −41A to perform programs (c) and (b) respectively. The COUNT 15000 instruction in (a) gives the user time to examine the display to see if the correct number appears.

the emulation is run repeatedly, most probably it was due to a faulty processor or memory chip. Replacing the chip should fix the problem.

If the problem does recur, the user can eliminate these possible sources of error and concentrate on the actual communications link between the processor. This can be done by using Multi-ICE software along with designer-generated programs that check for hard (consistent) or soft (intermittent) errors. For finding hard errors in the aforementioned system, the programs shown in Fig. 3 may be used.

Hard errors, easy solution

Program (a) in Fig. 3 is another example, similar to that in Fig. 2 and showing control of the emulation through the keyboard. The commands from ACTIVATE PR2 to the first ENDACTIVATE create an execution list for the 8041A's emulator. In this example, the 8041A ICE is ICE 2. On entering the ENDACTIVATE command, the main processor sends this list to PR2, which then begins to control ICE 2.

The list tells ICE 2 to load the 8041A program from a disk file named PROG. AGX into the ICE-41A and make the ICE module begin executing it. That program, entered onto disk by the user, is shown in Fig. 3b. Basically, it tells the emulator to read a character from its data-bus buffer (DBB), decode and display it, send an acknowledgment to the 8085 emulator, and repeat the operation. This program, which is activated by the main processor, runs to the IN A, DBB line, at which point it waits for a character input from the other emulated processor.

Meanwhile, the main processor, having returned to the host environment, reads the next command, ACTIVATE PR1, which takes it into the EN1 environment. As in EN2, the commands from ACTIVATE PR1 to the second ENDACTIVATE create an execution list, here for the 8085's emulator.

As for the first execution list, this list is sent to PR1 when the main processor enters the ENDACTIVATE command. ICE 1 then loads the program shown in Fig. 3c, noting that the term CHAR has been defined as the value stored in register B of the emulated processor, which is initially zero. The program runs from XMIT to THEND, whereby it reads the character value stored in register B, then writes it to port $A0_{16}$'s data-bus buffer, whence it is transmitted to the waiting 8041A emulator's. It then loops until it receives an acknowledgment from the 8041A emulator, after which it halts.

After each character is sent and acknowledged, PR1 updates the value of CHAR by 1, and waits for a count of 15,000. It does so until the final character, $0FF_{16}$, in a

```
* DEFINE MACRO CHARRANGE
* . REMOVE SYM .CHAR
* . DEFINE .CHAR = %0
* . REPEAT
* . . RB = .CHAR
* . . GO FROM .XMIT TIL .THEND
* . . CHAR = CHAR + %1
* . . WHILE .CHAR <= %2
* . . ENDREPEAT
* . ENDM
```

(a)

4. If it's soft. In order to find soft transmission errors on an iSBC 80/30, program (a) defines a macrocommand, CHARRANGE, that causes numbers to be transmitted in a nonconsecutive sequence. Program (b) substitutes for the PR2 list of program 3a, halting the test when the sent and received numbers do not match.

```
* KILL PR2

* ACTIVATE PR2                         ;
* . DEFINE .MISMATCH = 0               ;
* . REPEAT                             ;
* . . GO FROM .IBFULL TIL .CNTNU       ; Read and display character
* . . IF DBB <> PR1 .CHAR              ; If character read is wrong
* . . . THEN .MISMATCH = 1             ; Then MISMATCH = 1;
* . . . ELSE                           ; If not, acknowledge receipt
* . . . ENDIF                          ;
* . . WHILE .MISMATCH = 0              ; If MISMATCH = 1, loop ends
* . . ENDREPEAT                        ;
* . ENDACTIVATE                        ;
```

(b)

string of 256 has been sent. Thus it transmits in sequence all characters that the target system can display.

Introducing the 15,000-count wait between character transmissions gives the user time to examine the display visually to see if the character transmitted is the correct one. If it is not, he or she can enter a KILL command and examine the trace to see what went wrong.

Not hard enough

Although stepping through characters one at a time at slow speeds will permit hard, or repetitive, errors to be detected visually, stepping through 256 characters in sequence will probably not reveal an intermittent failure. Therefore, if the error does not appear after the first test is run, the test can be modified to display characters more rapidly in a variety of sequences and to halt automatically when one is found.

To modify the test procedure, the user first defines a macrocommand named CHARRANGE, which will make PR1 instruct ICE 1 to transmit various sequences of characters. This macrocommand, defined in Fig. 4a, has three parameters that must be defined by the user each time it is employed: %0, the first character to be displayed; %1, the increment between characters; and %2, the last character to be displayed. After it is defined, all the user need do is write the command CHARRANGE followed by the appropriate values for %0, %1, and %2 for the sequence to be executed by the 8085. There is no need to put the statement in an execution list, since the main processor in the host environment assumes that any single command not in a list is for PR1—here the 8085.

Note that although the CHARRANGE command is defined to do essentially the same task as the original PR1 execution list, it differs in four ways:

- The load statement is omitted because the 8085 program (Fig. 3c) is still loaded from the first test.
- A REMOVE statement has been added to delete CHAR so that DEFINE CHAR will not result in a duplicate-symbol-definition error.
- The initial, incremental, and ending values of CHAR are taken from the macrocommand rather than being fixed at 0, 1, and $0FF_{16}$.
- The count loop has been dropped, since the error will be detected by the system rather than visually.

Along with the CHARRANGE command, a new execution list for PR2 is needed to automatically capture errors. The list (Fig. 4b) begins with a KILL PR2 statement in order to get rid of the old execution list that PR2 is still running.

The new PR2 execution list defines a variable MISMATCH, which initially has the value 0, and enters the loop from REPEAT to ENDREPEAT. In this loop, the routine of Fig. 3b is run until the label CNTNU. Before going further in that program, the value in the data-bus buffer compared with that of PR1's CHAR.

If they match, CNTNU is performed to acknowledge proper receipt of the transmitted character, and the routine continues to loop until the last character defined by the CHARRANGE command is transmitted. If they do not, the MISMATCH value is changed to 1, which terminates the loop and the execution list. By examining the trace record stored in ICE-41A (ICE 2), the processor's status for the last 256 instructions can be viewed. Evidence of what went awry should be in those records. □

Voltage-controlled integrator sets filter's bandwidth

by Henrique Sarmento Malvar
Department of Electrical Engineering, University of Brazilia, Brazil

Because it uses operational transconductance amplifiers as electrically tuned integrators for selecting a state-variable filter's center frequency and bandwidth virtually independently of one another, this circuit is ideal for use in music and speech synthesizers that require individual voltage-controlled setting of these parameters.

As shown, input signals to be processed are applied to transconductance amplifier A_1, whose bias current is derived from voltage-to-current driver A_5Q_5. The bias current, in turn, is set by control voltage V_ω, which ultimately determines the filter's center frequency. In general, $I_{bias} = V_\omega/2R_{11}$.

Placing the capacitor C_ω across the output of the operational transconductance amplifiers A_1 and A_2 converts the two-stage network into a noninverting integrator, the transfer function becoming $V_o(s)/V_i(s) = k/s$, where k is the 3080's transconductance factor k'/C, and transconductance k' as given in its data sheets is $k' = 19.2\ I_{bias}$. Substituting for I_{bias}, $V_o(s)/V_i(s) = 19.2\ V_\omega/sRC_\omega$.

Placing integrator A_3 in the feedback loop of A_1 and A_2 equips the basic filter with the capability to control bandwidth. As seen from inspection of the circuit:

$$V_x(s) = R_1\|R_2\|R_3\|R_4\left[\frac{V_i(s)}{R_1} + \frac{V_y(s)}{R_3} + \frac{V_{LP}(s)}{R_4}\right]$$

where the low-pass function is given by:

$$V_{LP}(s) = -(k_2/s)^2V_x(s)R_6/(R_5+R_6)$$

and where $V_y(s) = -k_1V_x(s)/s$. Constants k_1 and k_2 are given by:

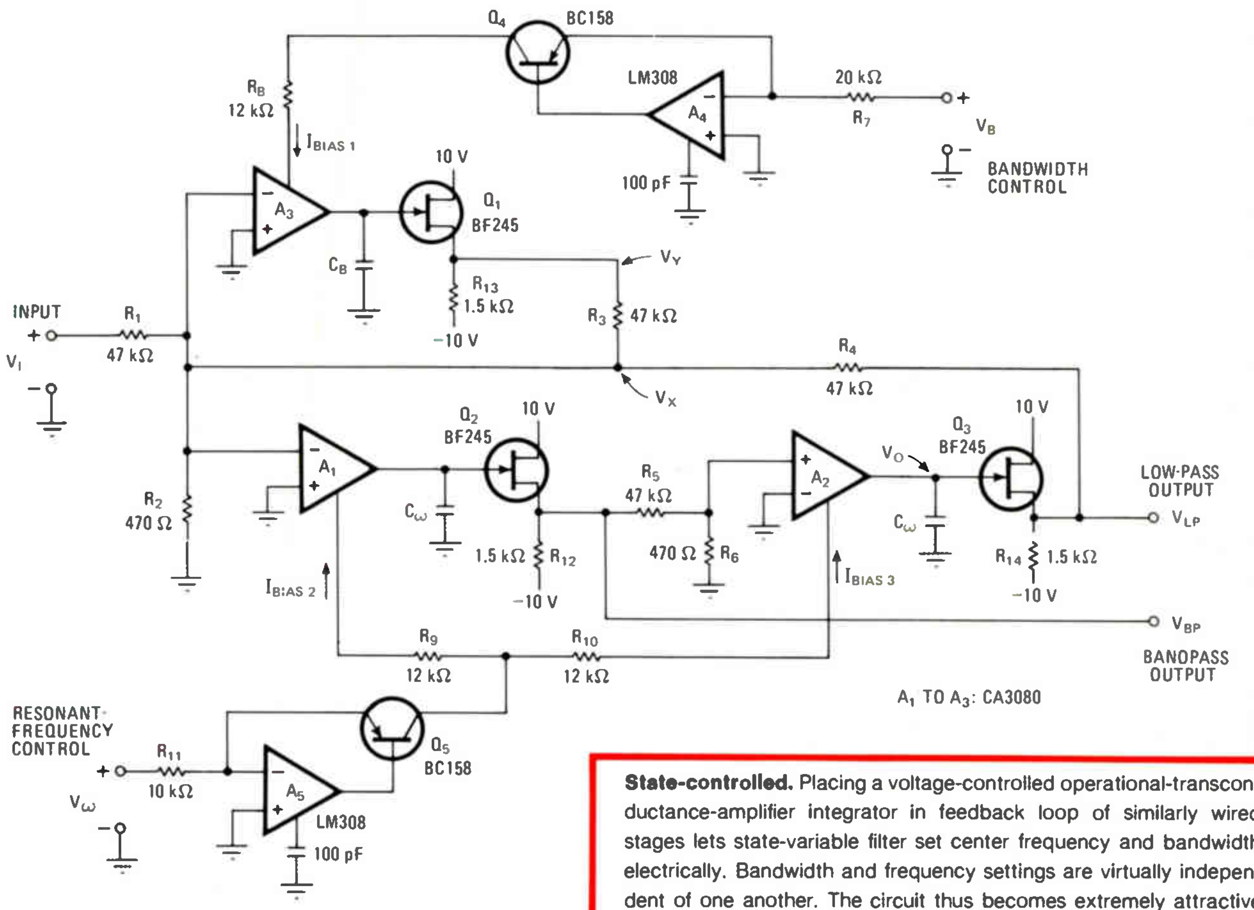
$$k_1 = 19.2\ V_B/R_7C_B$$

$$k_2 = 19.2\ V_\omega/2R_{11}C_\omega$$

and the bandpass function, $V_{BP}(s)$, equals $-k_2V_x(s)/s$.

Assuming $R_1 = R_3 = R_4 = R_5 = R'$ and $R_2 = R_6 = R''$, with $R''/R' = a \ll 1$, it follows that $R_1\|R_2\|R_3\|R_4 = R_2$. Substituting the appropriate quantities back into all the above equations, it is seen that:

$$V_{LP}(s)/V_i(s) = -1/[(s/\omega_o)^2 + (B/\omega_o)(s/\omega_o) + 1]$$



State-controlled. Placing a voltage-controlled operational-transconductance-amplifier integrator in feedback loop of similarly wired stages lets state-variable filter set center frequency and bandwidth electrically. Bandwidth and frequency settings are virtually independent of one another. The circuit thus becomes extremely attractive for music and speech synthesis applications.

$$V_{BP}(s)/V_i(s) = -(s/\omega_o)/[(s/\omega_o)^2+(B/\omega_o)(s/\omega_o)+1]$$

where the resonant frequency and the bandwidth are given by:

$$\omega_o(rad/s) = ak_2 = 19.2aV_\omega/2R_{11}C_\omega$$

$$B(rad/s) = ak_1 = 19.2aV_B/R_7C_B$$

Parameter a should be near 0.01, to ensure the best compromise between distortion and signal-to-noise ratio. The bias current of the operational transconductance amplifier should not be more than 500 microamperes. □

Dc-coupled trigger updates quickly

by Andrzej M. Cisek
Electronics for Medicine, Honeywell Inc., Pleasantville, N. Y.

Two operational amplifiers and a few components build this broadband trigger, which is absolutely immune to the problems created by dc offset and base-line wandering. A self-adapting stage for maintaining a constant level of hysteresis, as well as dc coupling at the input, permits a low-cost yet superior performance over a wide range of input signals that makes the circuit very attractive for biomedical applications.

Input signals are applied to the LM307 amplifier, A_1, through charge-storage network $D_1D_2R_1R_2C$ (a). Diodes D_1 and D_2 quickly charge capacitor C to the peak of the input voltage (less one diode drop) and minimize C's discharge until the signal falls more than two diode drops below the peak voltage.

The output of A_1 is then compared with the original signal at A_2. The amount of hysteresis is set by constant-current source Q_1 and Q_2, two p-channel field-effect transistors wired as diodes in A_2's positive feedback loop, and R_3. Q_1 and Q_2 ensure that the level of hysteresis is maintained virtually constant for any dc offset at the input. Resistor R_1 provides a zero level for input signals whose amplitude is smaller than one diode drop, and R_2 protects the input-signal source.

Such an arrangement has a reliable triggering level and responds fast, its speed being limited only by time constant $(R_{D1,2}+R_2)C$. This time constant can be easily adjusted to meet the requirements of practically any application.

As for the circuit's use in medical electronics, consider the two cases illustrated in (b) and (c), where a cardiac signal representing heart rate is superimposed on the respiratory (breath) signal. Depending on the trigger level, either heart rate (b) or respiration rate (c) may be counted. □

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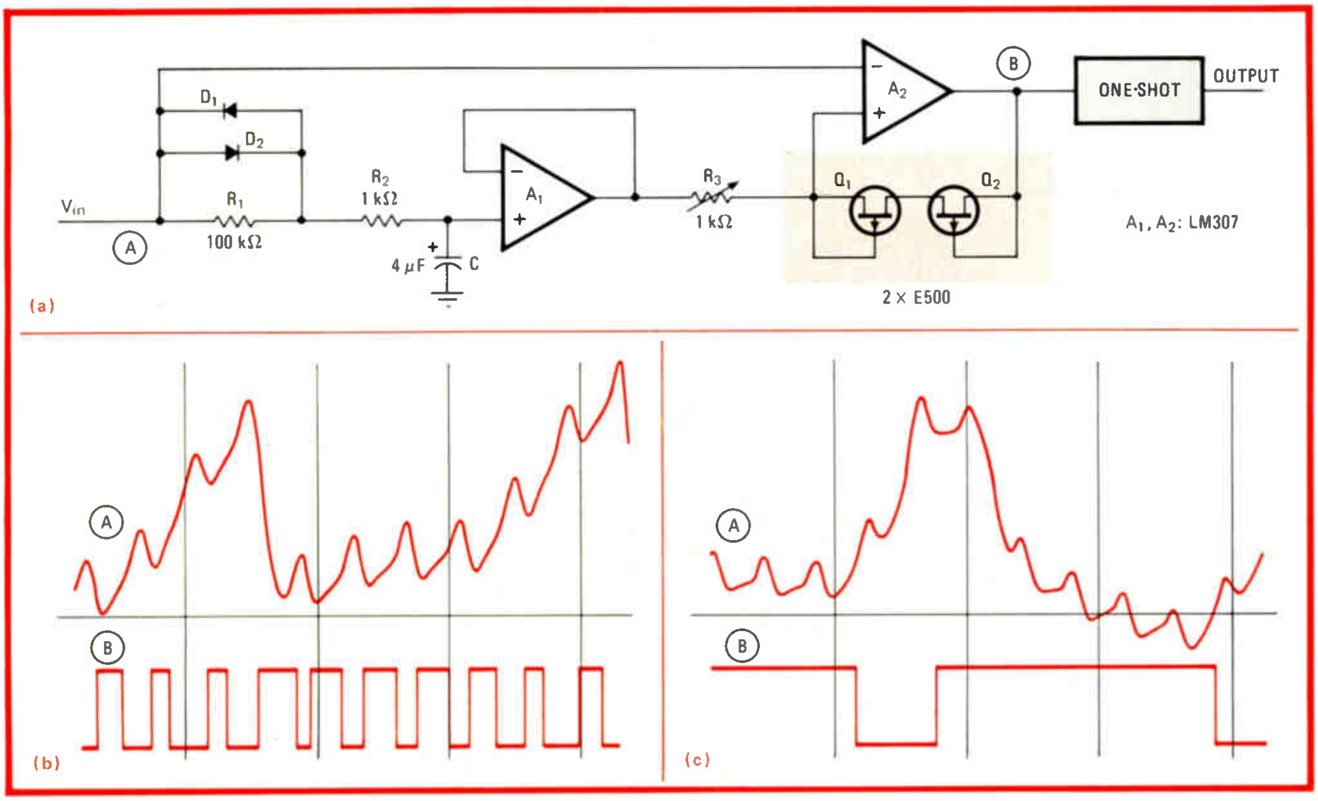


Flat. Trigger (a) maintains switching level over a wide band of frequencies and input-signal amplitudes. Operation is independent of input dc offset and problems created by baseline shift. Directly coupled arrangement at input contributes to circuit's high-speed response. In biomedical application, trigger switches on superimposed signals produced by heart rate (b) and respiration rate (c).

Circle 147 on reader service card

Serial-to-parallel converter decodes width-modulated BCD

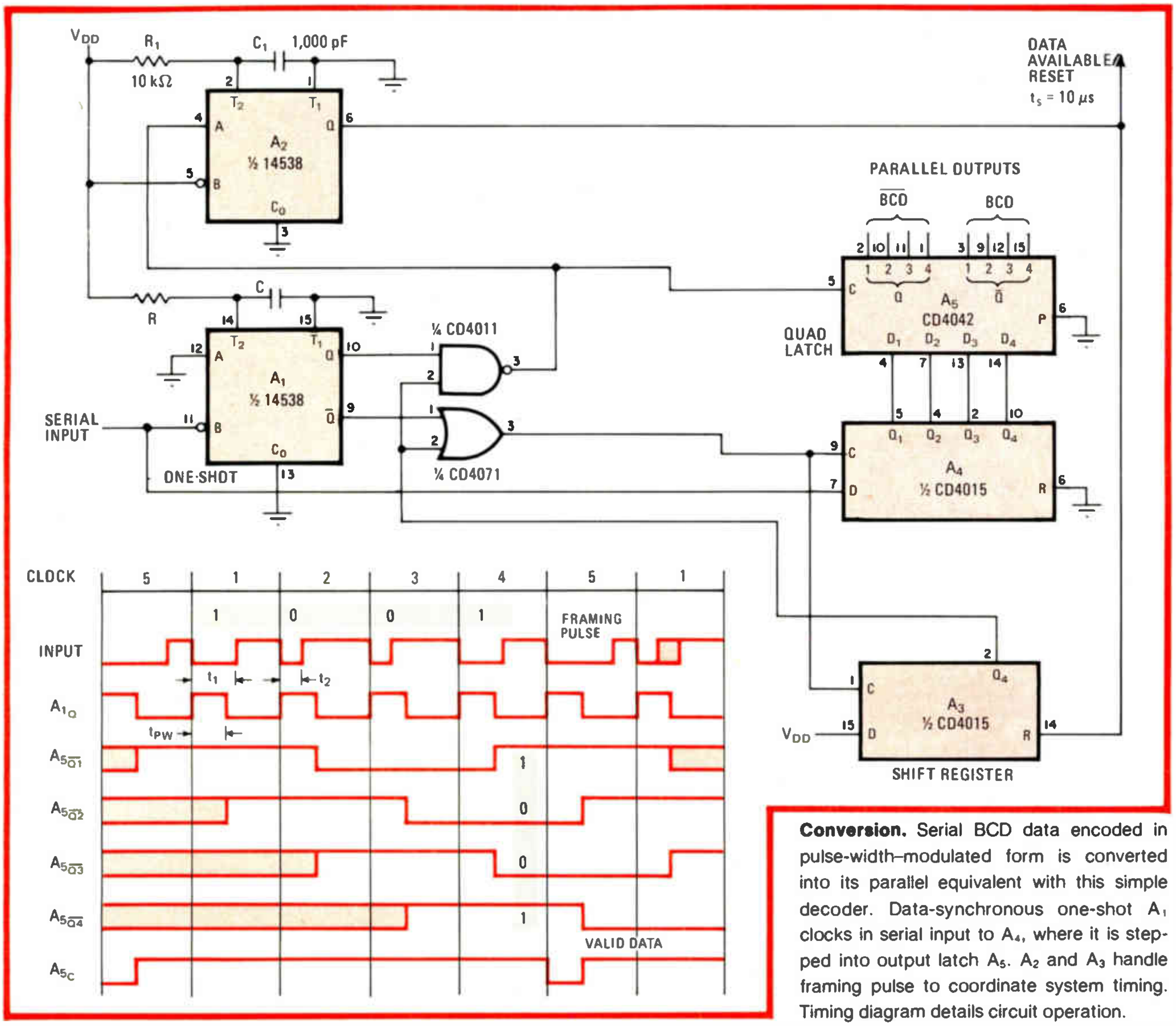
by William D. Kraengel Jr.
Valley Stream, N. Y.

Converting a binary-coded-decimal pulse train into its parallel equivalent is normally straightforward, unless of course, the signal assumes the form of a pulse-width–, pulse-code–, or pulse-position–modulated data stream. In data-processing cases where the stream is encoded by means of pulse-width modulation, however, this simple 4-bit decoder will serve well in performing the serial-to-parallel transformation.

The MC14538 one-shot, A_1, and the CD4015 4-bit shift register, A_4, form the central part of the decoder, serving as the timing and storage elements. As can be seen from the schematic and the timing diagram, the BCD input data is grouped into 5-bit cycles, with bit 5 being the framing pulse. A_1 must generate a pulse width of $t_{pw} = RC = \frac{1}{2}(t_1+t_2)$ when triggered, and one-shot A_2 has a very small triggering time of $t_s = R_1C_1 = 10$ microseconds, where both times are defined as shown in the timing diagram.

The firing time for A_1 must be selected to correspond to the input frequency of the serial BCD data. Under this condition, the one-shot is triggered by the negative edge of each serial input data bit, and if the serial input data line is low at the time the one-shot times out, a logic 0 is introduced into the shift register. On the other hand, a logic 1 will be read into the shift register if the input data goes high by the time A_1 times out.

Shift register A_3 serves as a counter, acting to disable A_4 and enable quad latch A_5 and one-shot A_2 during the framing pulse. The valid data from A_4 (which is inverted) is latched into A_5 as A_1 times out during the framing pulse. Simultaneously, A_2 is triggered so as to generate a data available/reset strobe signal for any peripheral control circuitry. The parallel equivalent BCD data and its inverse are available at the outputs of quad latch A_5. □



Conversion. Serial BCD data encoded in pulse-width–modulated form is converted into its parallel equivalent with this simple decoder. Data-synchronous one-shot A_1 clocks in serial input to A_4, where it is stepped into output latch A_5. A_2 and A_3 handle framing pulse to coordinate system timing. Timing diagram details circuit operation.

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64-K RAM rebuffs external noise

Circuit design reduces data-pattern sensitivity and problems caused by power supply fluctuations; polyimide coating foils alpha particles

by H. Katto, H. Kawamoto, K. Mitsusada, and K. Itoh, *Hitachi Ltd., Tokyo, Japan*

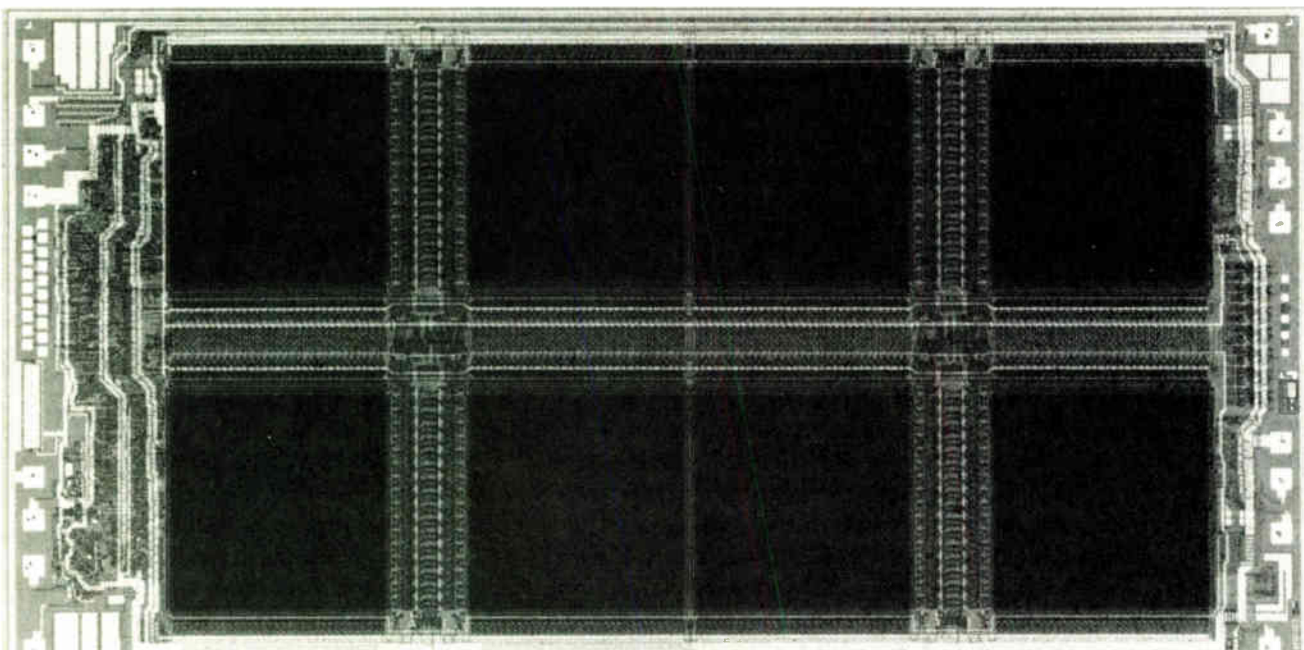
☐ The 64-K dynamic random-access memory is presenting challenging targets to device and circuit designers. Its storage cells are about half as large as those in its 16-K predecessor and one power supply must suffice instead of three. The 64-K RAM must also provide high speed and low power dissipation and, of course, a capacity four times as great as that of the older memory.

Reducing the amount of stored charge and limiting the source of power to a single +5-volt supply leaves a memory open to the effects of externally generated noise. This noise can take the form of a particular input data pattern, fluctuations or bumps in the power supply, overshoot on input signals, and alpha radiation. In the HM4864 64-K dynamic RAM, these potential error sources are not only taken into account, but they are also substantially subdued through proper circuit design and layout. Alpha particles, too, are kept at bay through the right choice of a protective coating material.

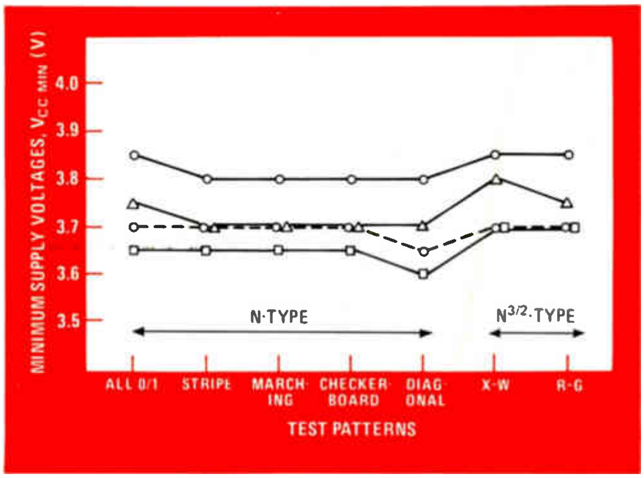
Low cost is without doubt the most significant attribute of a successful dynamic RAM. The goal is to get the greatest number of good chips from a silicon wafer for the lowest per-bit cost. The highest yield stems from the smallest die, yet the chip should be as large as possible for maximum memory cell dimensions. One restriction is that a 64-K RAM has to be smaller than 50,000 square mils if it is to be mounted in a standard 16-pin, 300-mil dual in-line package. Inevitably, then, to get the necessary density—65,536 bits—each memory cell must be reduced to about half the size of those in a 16-K dynamic RAM. The availability of just one power supply compounds the difficulty of storing and sensing this smaller charge packet.

Laying out for noise

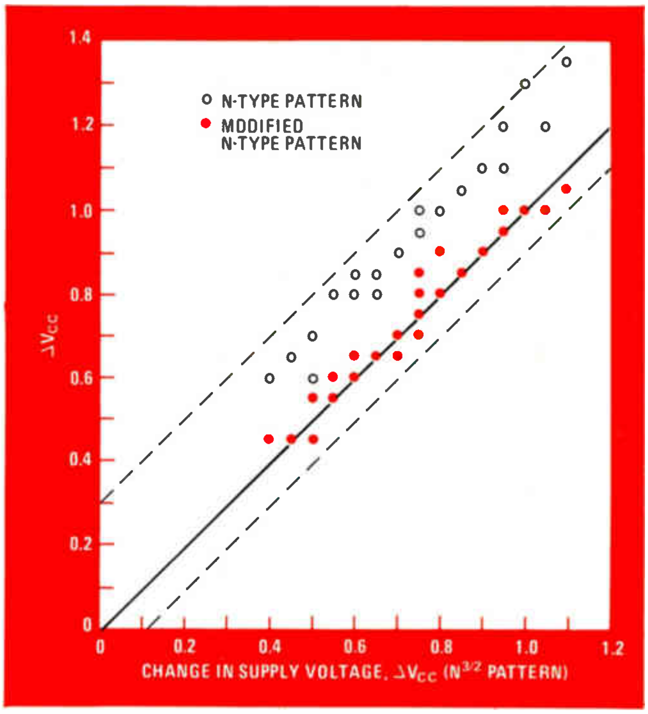
The high signal-to-noise ratio of the 4864 is achieved in part through the adoption of an aluminum folded bit-line scheme. This reduces bit-line capacitance from that of the traditional diffused approach. But metal bit lines demand the use of polysilicon for the word lines. The memory array is therefore subdivided into eight



1. Reliably yours. The HM 4864 64-kilobit dynamic RAM stands up to externally generated noise. A higher signal-to-noise ratio is realized, in part, through a folded metal bit-line layout. To avoid long polysilicon word lines, the memory is broken into eight sections.



2. V_{CCmin} test. In the V_{CCmin} test, the device is stressed by lowering its power supply to a value just above that required to support normal operation. The results shown in the figure above indicate a consistency in the cell-to-cell behavior of the device.



3. Bump test. For the results shown above, the chip was subjected to the V_{CC} bump test. In this test, the power supply voltage is changed between read and write operations. Ideal results would all lie on the solid diagonal; the points above come close.

sections to minimize word-line delay, which is proportional to the square of the length of the word line (see Fig. 1).

With the diffused open–bit-line layout popular in the 16-K dynamic RAM, noise on either bit line creates an imbalance that may cause an error in memory-cell signal detection by the sense amplifier. In the folded–bit-line structure, the common-mode noise cancels itself out since each word line crosses both bit lines with the same row (or X) address. The configuration also minimizes substrate noise coupled to the bit lines through junction capacitances.

Testing for noise

The best way to prove that the 4864 is insensitive to circuit noise is to perform V_{CCmin} and V_{CC} bump tests, as they are called, using various input data patterns. During the V_{CCmin} test, the supply voltage is reduced to a value slightly above that required for proper operation. With the V_{CC} bump test, the data patterns are applied while the supply is varied from a minimum to a maximum value.

Figure 2 shows V_{CCmin} test results using several data patterns. With N-type test patterns, the number of read and write operations required to perform the test grow in integral multiples of the number of bits in the memory. With $N^{3/2}$ patterns, testing complexity grows more rapidly because the exponent exceeds unity.

For the all-0/1 pattern named in the figure, each memory location is first written with a 0; then each location is read out and its data verified. After this, each cell is written with a 1 and similarly verified. With the stripe pattern, odd rows are filled with 0s and even rows with 1s. Then this data is verified. Next the even rows are filled with 1s while the odd rows are loaded with 0s. Again the data is checked. Finally, this entire process is repeated for the columns in the memory.

Even without a detailed description of each specific pattern, the test results can be appreciated. In Fig. 2, for the V_{CCmin} test, the lines should be horizontal; this reveals a consistency in the cell-to-cell behavior of the device. Also, uniform pattern sensitivity is always good news for the test engineer, since with N-type patterns the tests can often be performed in less than a second, whereas $N^{3/2}$ tests for a 64-K RAM take several minutes.

The results of the V_{CC} bump test can be even more revealing. For this test, within a 2-millisecond time period, the chip's supply voltage is changed from that for a read cycle to that for a write cycle. More specifically, the worst-case test conditions present the highest possible voltage during the read operation and the lowest value for writing, with 0s being written into the memory.

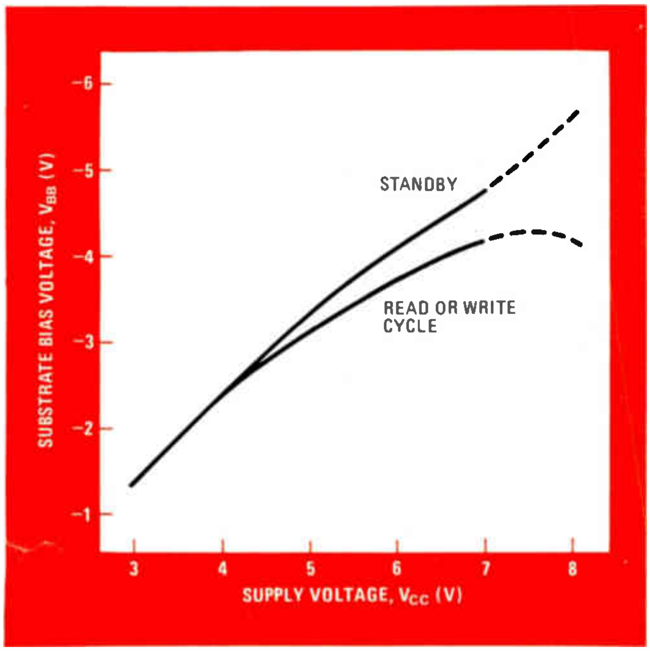
Figure 3 shows how about 20 arbitrarily chosen samples stood up to the V_{CC} bump test using 4.5 volts as the minimum level of the supply voltage. Ideally, all the results would lie along the 45° solid diagonal line, indicating little deviation in sensitivity between the N and $N^{3/2}$ patterns. This goal was not met but the spread is inconsequential: the worst-case difference in writing and reading voltages—V_{CC}—is 0.4 V for the $N^{3/2}$ patterns, and the difference in V_{CC} between the $N^{3/2}$ patterns and the N patterns is less than 0.3 V. Had a traditional open–bit-line approach been adopted without an optimized circuit design, there would have been a much greater difference—possibly twice as great—in the results obtained for the N and $N^{3/2}$ patterns.

Substrate biasing

A negative substrate bias voltage, V_{BB}, whether it is external or on chip, is desirable because of its higher speed and stable circuit operation. This negative potential also helps to keep the chip's operation immune to statistical scattering of threshold voltages, which can occur during manufacturing. The higher speed is a result

HM4716A VERSUS HM4864 TIMING SPECIFICATIONS (IN NANOSECONDS)

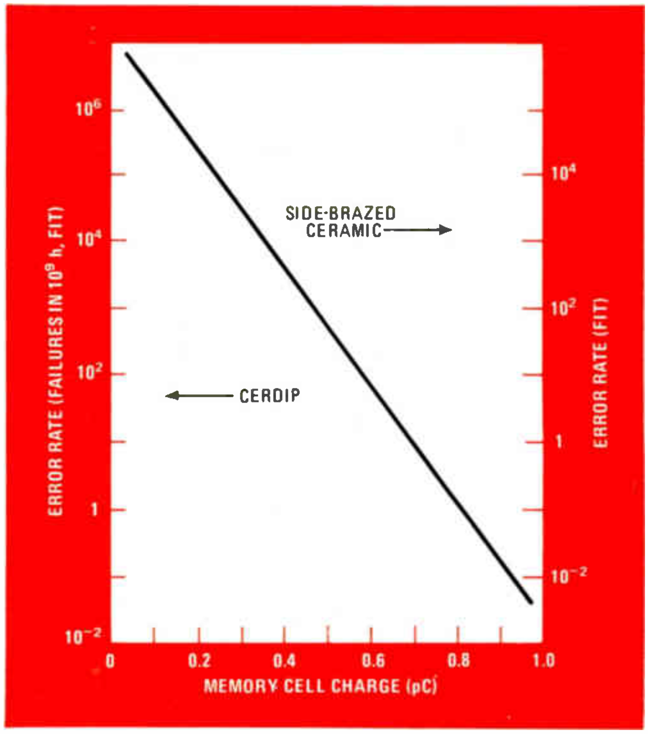
Parameter	Symbol	16-K RAM	64-K RAM	
		HM4716A-3	HM4864-3	HM4864-2
Access time from row address select, RAS	t_{RAC}	200		150
Cycle time	t_{RC}, t_{RWC}	375	335	270
RAS precharge time	t_{RP}	120	120	100
Delay from RAS to write enable, WE	t_{RWD}	160	145	110
Write command to RAS lead time	t_{RWL}	80	55	45
Delay from RAS to column address setup time, CAS	t_{RCD}	30/65	25/65	20/50
RAS setup time	t_{ASR}	0	0	0
Row address hold time	t_{RAH}	25	25	20
CAS time	t_{ASC}	−5	−10	−10
Column address hold time	t_{CAH}	55	55	45



4. On-chip bias. Like most 64-K RAMS, the HM4864 incorporates an on-chip substrate bias generator. It is composed of a five-stage oscillator and V_{BB} is set to about −3 volts whether the chip is in standby or operation. The generator consumes very little power.

of reduced junction capacitance.

With a substrate bias, the negative undershooting of the TTL input signal (−2 V) can be safely tolerated. The biasing also prevents the reduction of the memory cell's data-retention time, which is caused by the undesirable electron injection from the bootstrap capacitances in the peripheral circuitry. Further, with an on-chip generator, as the V_{CC} power supply voltage varies, the level of V_{BB} will automatically adjust for stable circuit operation. At deeper V_{BB} biases, threshold voltages are less dependent upon V_{BB} or V_{SS}, which leads to more stable operation of inverter circuits in the chip's periphery.



5. Packaging matters. The soft-error rate of a dynamic RAM depends primarily on the stored charge, regardless of the circuit design techniques adopted for the memory. Soft errors go up as cell charge is reduced; a side-brazed ceramic package is best.

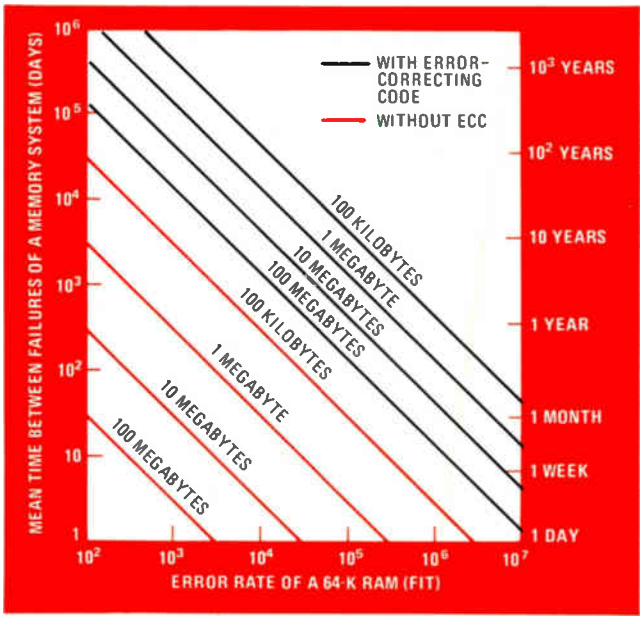
The 4864's substrate bias generator is composed of a five-stage oscillator; V_{BB} is set to about −3 V whether the circuit is on standby or in operation (see Fig. 4). Despite its ability to maintain the desired bias, the generator scarcely contributes to the chip's overall standby current consumption—typically under 2 mA.

Designing for timing and speed

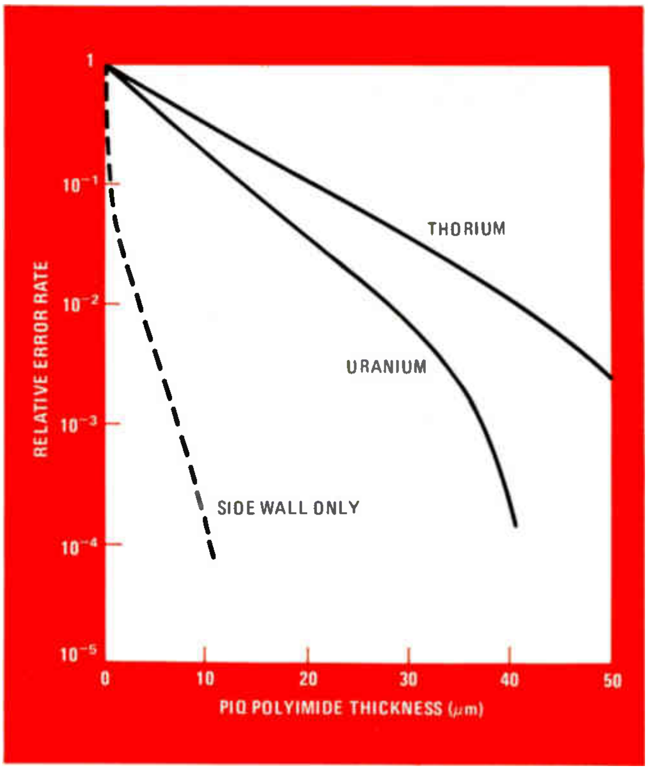
The basic requirement for the timing and speed specifications of a 64-K dynamic RAM is compatibility with—and, if possible, improvement upon—those of existing 64-K parts. Without detailing every timing specification, The table shows important differences between the 4864 and the HM4716A-3 16-K dynamic RAM.

In the (preliminary) specifications of the 64-K memory, t_{RWD} and t_{RWL} and the cycle times t_{RC} and t_{RWC} are much shorter than those for the 16-K device. The cycle times t_{RC} and t_{RWC} are approximately equal to $t_{RAC} + t_{RP}$ and $t_{RWD} + t_{RWL} + t_{RP}$, respectively, with some margin to include the transition times of the pulses. Therefore, the improvement in cycle time t_{RWC} is due to the shortening in the delays of t_{RWD} and t_{RWL}. (These time periods are defined in the table).

In addition to these key specifications, no timing characteristics of the 4864 are inferior to corresponding 16-K specifications. All in all, the 4864 is more than fast enough to replace existing 16-K dynamic RAMs with the same access time. The introductory access time of the 64-K device will be 200 nanoseconds. This will be followed later by 150-ns and then 120-ns chips, just as in the case of 16-K RAMs. Also, nothing more than power supply modification and the provision for one more



6. Bad bits. For a large 10-megabyte system, the use of 64-K RAMs having a failure rate of about 10^5 FIT gives double-bit errors on about a yearly and single-bit errors on about a daily basis. To stay below 1,000 FIT, cell capacitance must not be smaller than 0.07 pF.



7. Overcoat. A direct way to halt alpha particles is to coat the memory with an organic material such as polyimide. A 45- to 55-μm-thick layer of Hitachi's polyimide—PIQ—should reduce the frequency of soft errors—theoretically, by a factor of 1,000.

address signal is needed for designs based on the newer memory device.

It is now known that uranium and thorium isotopes in packaging materials—be they ceramic metal, glass, or even plastic—emit an alpha particle (a helium nucleus) on a daily to weekly basis. These cause soft errors but no permanent damage. They are detectable even in existing 16-K dynamic RAMs that use 12-V V_{DD} supplies, but single-supply 64-K RAMs are far more susceptible. The charge stored in the memory cell is reduced because the cell is smaller and because a lower voltage is available for the top plate of the cell capacitor.

Protective coat

Without a protective coating, the soft error rate of a dynamic RAM depends primarily on the stored charge (oxide capacitance multiplied by an effective voltage equal to or smaller than V_{CC}) in the memory cell regardless of the layout and circuit design philosophies adopted for the memory. Figure 5 shows how soft errors increase as the charge on the memory cells is reduced.

Figure 6 shows the worst-case mean-time-between-failure (MTBF) rate of a memory system with and without error-correcting code (ECC). It is assumed that the ECC can correct a single-bit error out of 72 bits and that any 2-bit errors will be detected. Worst case means that the data written into the memory is continuously read with a minimum cycle, with no intervening write or read-modify-write cycles. For a large 10-megabyte system, the use of 64-K dynamic RAMs having a soft error rate of about 10^5 FIT results in yearly double-bit errors and daily single-bit errors. (FIT stands for failures in time. One FIT equals 10^{-9} errors per hour.)

Assuming that a tolerable soft-error rate is 1,000 FIT or 0.1%/1000 hr (though this may still be unsatisfactory in some situations), with a side-brazed ceramic package cell capacitance must not be smaller than 0.07 pF. This must be so even if the threshold voltage loss of the transfer MOS transistor is eliminated and full V_{CC}-level signals are written into and read from the cells.

One way to combat alpha particle problems is to introduce new circuit techniques that increase the amount of stored charge. There is another, more direct approach to soft errors, however. A 45- to 55-micrometer overcoating of a contamination-free organic material such as polyimide reduces the energy of incoming particles. Theoretically, assuming that the memory cell is insensitive to alpha particles with an energy of less than about 2 million electron volts (MeV), this should reduce the error rate appreciably, perhaps by a factor of 1,000. As Fig. 7 shows, to obstruct an alpha particle of the highest possible energy (8.8 MeV from thorium) about a 70-μm layer of polyimide is needed.

The polyimide developed by Hitachi, called PIQ, is pure enough to contain no detectable amounts of uranium or thorium. (PIQ is the abbreviation of the chemical's full name, polyimide isoindoloquinazolinedione.) Long experience in using PIQ for large-scale integrated applications has shown that the material exhibits the proper rate of expansion for use not only with silicon but with silicon dioxide, aluminum, and gold.

For maximum suppression of alpha particles it was also discovered that the aluminum deposited for metal interconnections should be contaminant-free. Thus, for the smallest number of soft errors in the 4864, the PIQ organic overcoating is used with ultrapure aluminum and a side-brazed ceramic package. □

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Thermoelectric heat pumps cool packages electronically

Decreased costs and improved reliability of these solid-state modules warrant a new look at a versatile thermal management technology

by Dale A. Zeskind, *Consultant to Cambridge Thermionic Corp., Cambridge, Mass.*

□ As the packing density of integrated-circuit–chip packages continues to soar, the heat dissipation in equipment grows proportionally, making heat management of electronic systems vital to the design engineer. The improved and cost-efficient thermoelectric heat pump—a fully electronic module that can heat or cool a component or group of components—represents a versatile and available thermal management tool that engineers cannot afford to overlook.

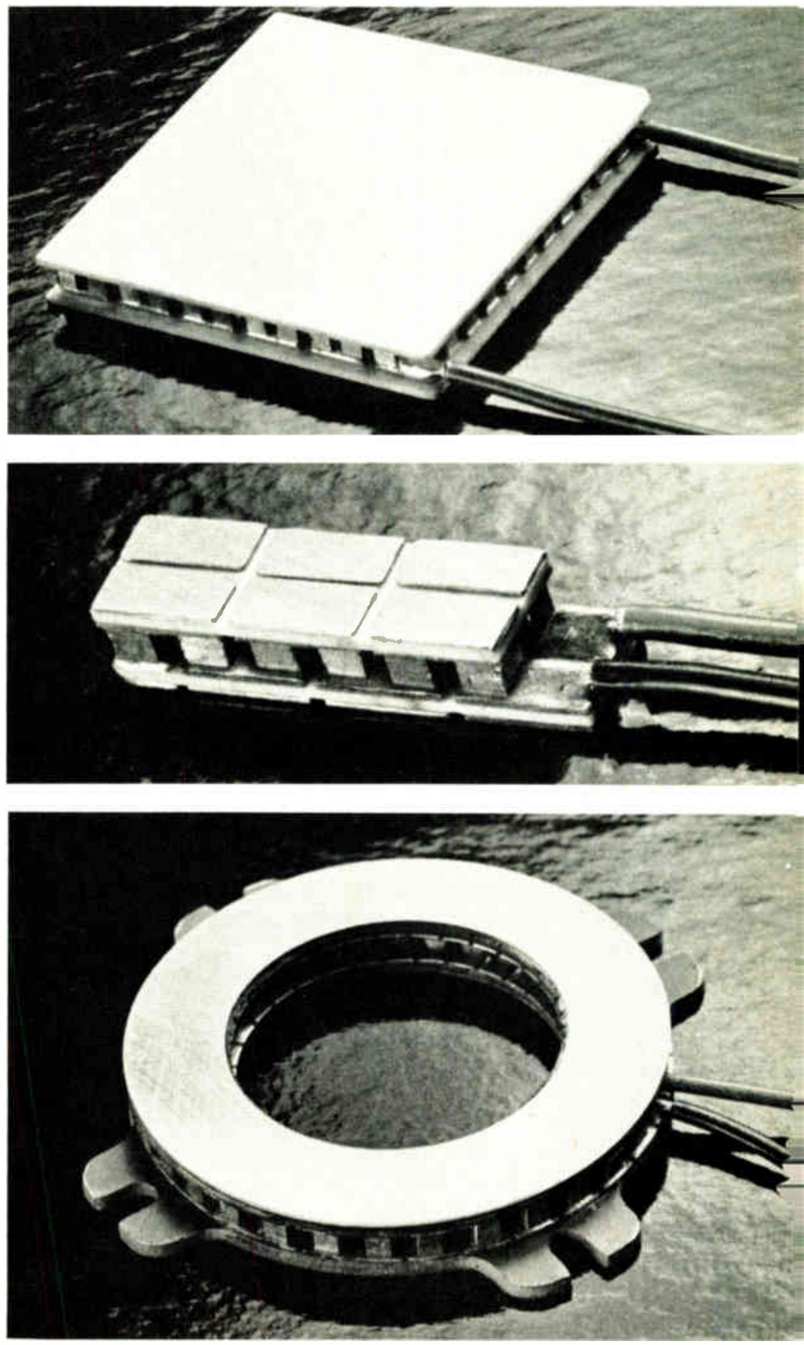
Thermoelectric heat pumps are solid-state devices with no moving parts. With a suitable electrical power input, they pump heat from one side of the device to the other. Available in a variety of shapes and sizes, they provide one of the few means to cool objects to well below ambient temperatures. In addition to cooling, thermoelectric (TE) devices can generate heat and electric power. Some typical devices, or modules, are illustrated in Fig. 1.

Renewing interest

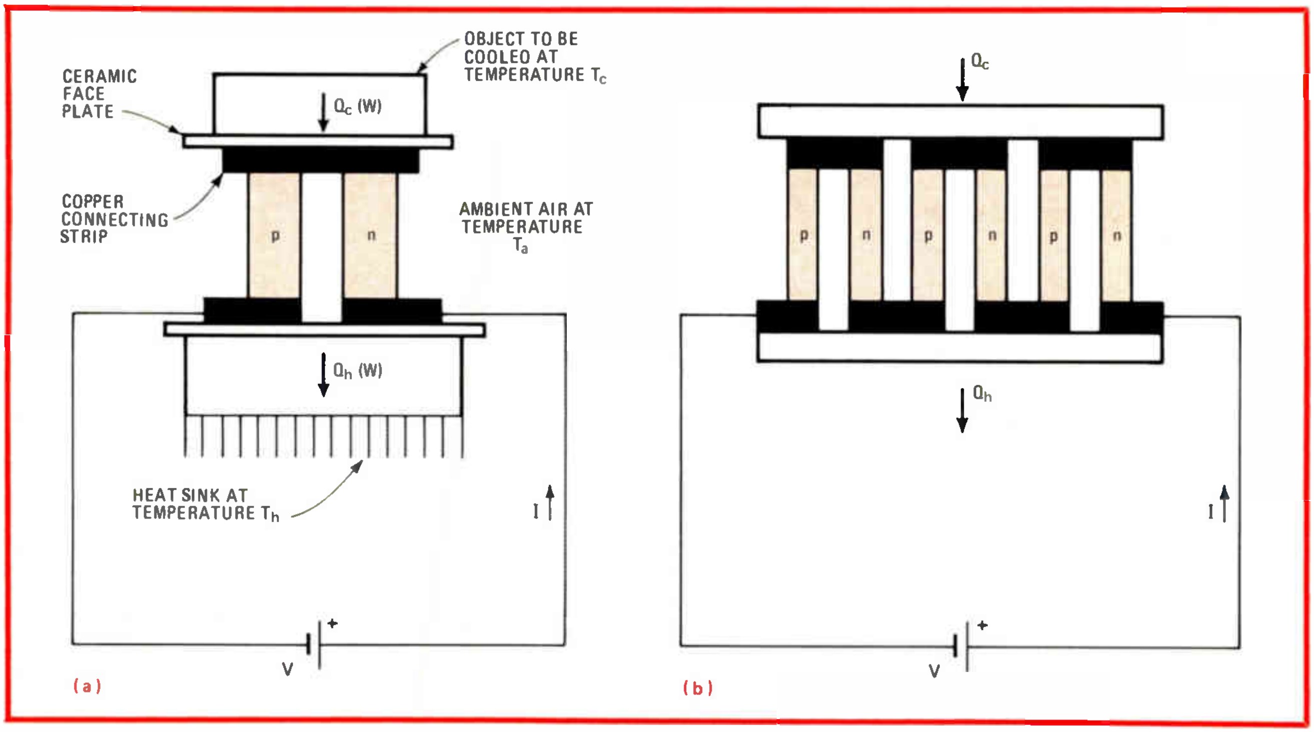
TE devices were originally developed during the 1960s to meet exacting, bulky, and expensive military and aerospace temperature-control applications. When they failed to compete economically with conventional electromechanical cooling techniques for mass applications (such as home refrigerators), most large companies, and industry in general, lost interest. Since then, they have found use primarily in special-purpose applications, such as cooling infrared detectors and maintaining sample temperatures in blood analyzers.

Throughout the 1970s, thermoelectric devices suffered from a distinct lack of promotional effort. Most recent graduates know little about them, though more experienced engineers remember the difficulties that plagued them during the 1960s. Recently, however, the following important developments have shown that thermoelectric cooling deserves closer examination by today's design engineers:

- TE device cost has fallen dramatically. A typical cooling module that sells for from $20 to $30 today sold for over $100 in 1975. (These figures are for quantities



1. Electronic heat pumps. These thermoelectric modules are solid-state electronic heat pumps. With a suitable electrical power input, they actively pump heat from one side of the device to the other and can cool objects to well below ambient temperatures.



2. TE operation. In a single thermoelectric couple (a), application of suitable electric current causes heat to be pumped from cold object to heat sink. Several of the TE couples in (a) can be connected electrically in series and thermally in parallel (b) to increase capacity.

below 10 and have not been adjusted for inflation.)

- TE devices are now available in a wider variety of shapes and sizes for a much wider variety of applications than before.
- Device quality, reliability, and delivery time have all improved greatly.

Peltier effect

At the foundation of today's thermoelectric heat pumps is the Peltier effect. In 1834 Jean C. A. Peltier discovered that the passage of an electrical current through the junction of two dissimilar conductors can either cool or heat the junction depending on the direction of the current. Heat generation or absorption rates are proportional to the magnitude of the current and dependent on the temperature of the junction.

Figure 2a shows a simplified schematic of a single thermoelectric couple. The thermoelectric modules of Fig. 1 consist of many such couples connected electrically in series and thermally in parallel (Fig. 2b). The p- and n-doped semiconductors form the elements of the couple and are soldered to copper connecting strips. Ceramic faceplates electrically insulate these connecting strips from external surfaces. In most thermoelectric modules, doped bismuth telluride is the semiconductor material. For high-temperature applications, however, lead telluride is often used.

At open circuit, the TE module of Fig. 2a acts like a simple thermocouple. A temperature gradient maintained across the device creates a potential across its terminals proportional to the temperature difference, ΔT. If ΔT is maintained and if the device is connected to an electrical load, power is generated.

If, instead, the device is connected to a dc source (as shown in Fig. 2), heat will be absorbed at one end of the TE module, cooling it while heat is rejected at the other end, where the temperature increases. Reversing the current flow reverses the flow of heat, so the module can generate electric power or, depending on how it is connected to external circuitry, heat or cool an object.

Thermoelectric heat pumps have found use in a wide range of applications, including the following, for which other cooling and heating methods are undesirable:

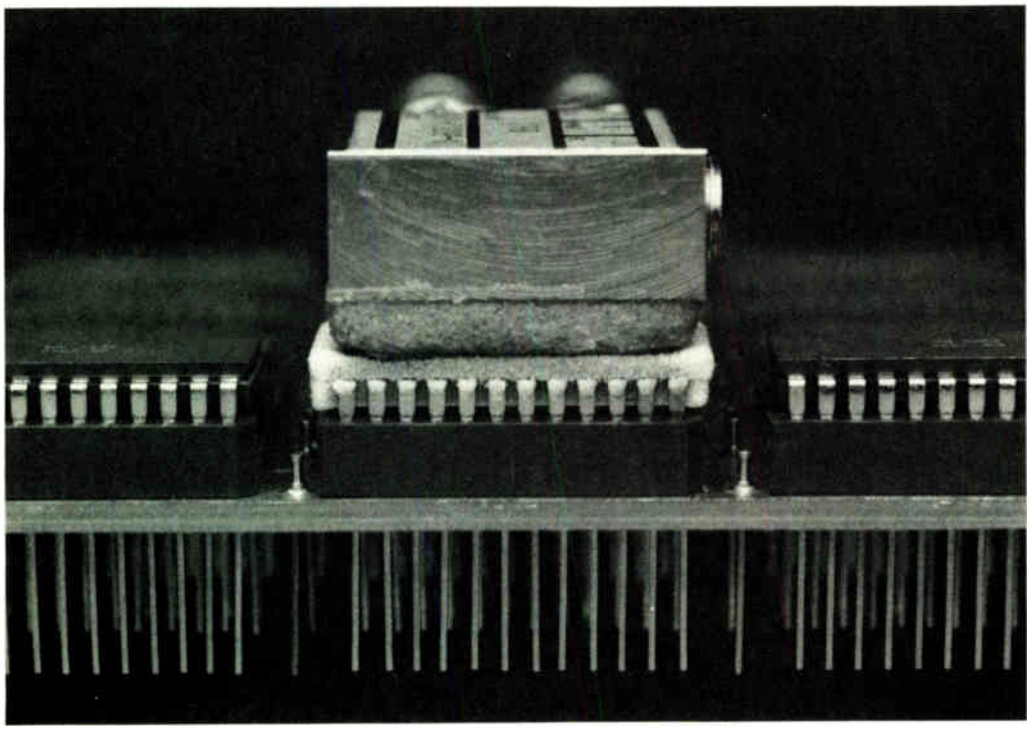
- Controlling temperature-sensitive electronic parameters such as noise or bias current in instrumentation operational amplifiers.
- Cooling infrared and charge-coupled-device detectors.
- Maintaining sample temperatures in medical and laboratory instruments.
- Laser-tuning through temperature control.
- Cooling photomultiplier tubes.
- Semiconductor testing (hot and cold wafer-holding chucks).
- Cooling microprocessors and other devices operating in industrial environments that have high ambient temperature.

Figures 3 and 4 illustrate some of these applications.

Smooth control

Because they can be proportionally managed by a control system that smoothly varies input current or voltage, TE devices provide a unique tool for stabilizing component temperatures in widely varying ambients. Also, in contrast to electromechanical cooling systems with on/off actuators, proportionally or servo-run TE modules allow tighter stabilization of both thermal and electric variations and transients.

Furthermore, the units can operate at up to 150°C or



3. Device cooling. Thermoelectric devices can cool electronic components to control critical parameters such as noise or bias current. In the photo, a TE module is used to cool a critical integrated circuit on a pc board. Note the accumulation of frost on this IC.

higher, even in a vacuum. Compared with electromechanical cooling systems, the solid-state modules combine reduced size and weight with long-term reliability approaching that of other solid-state devices.

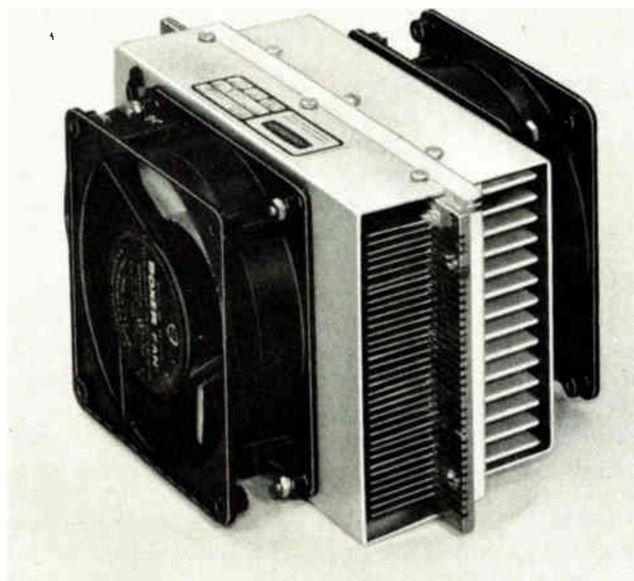
One of the better ways of designing in a TE module is to work with parametric performance curves such as those shown in Fig. 5. These transfer functions relate all the important input and output parameters of the module, including operating current, heat absorbed at the cold side, the temperature difference between the hot and cold sides (ΔT), and the module's thermoelectric efficiency.

In Fig. 2a, Q_c represents the heat in watts absorbed at the cold side of the TE couple and Q_h is the heat in watts rejected at the hot side. ΔT is the temperature difference between the hot and cold sides. A coefficient of performance (COP) is defined as the ratio of Q_c to electrical power in. Since the TE device uses electrical power primarily to transport rather than generate heat, under some circumstances COP can even exceed 100%.

Figure 5 illustrates the performance graph for a typical module at a fixed hot-side temperature of T_h = 50°C. One set of curves relates Q_c to electrical input current, I, at various values of ΔT. The other set of curves relates COP to I, again at various temperature differences.

These curves illustrate several important aspects of TE operation. First, it should be noted that temperature differences between hot and cold sides of up to 60°C can routinely be obtained. However, as the temperature difference increases, both Q_c and COP decrease. In optimally adapting TE performance to particular applications, the designer can use these performance curves in a variety of ways. Several design examples are discussed below.

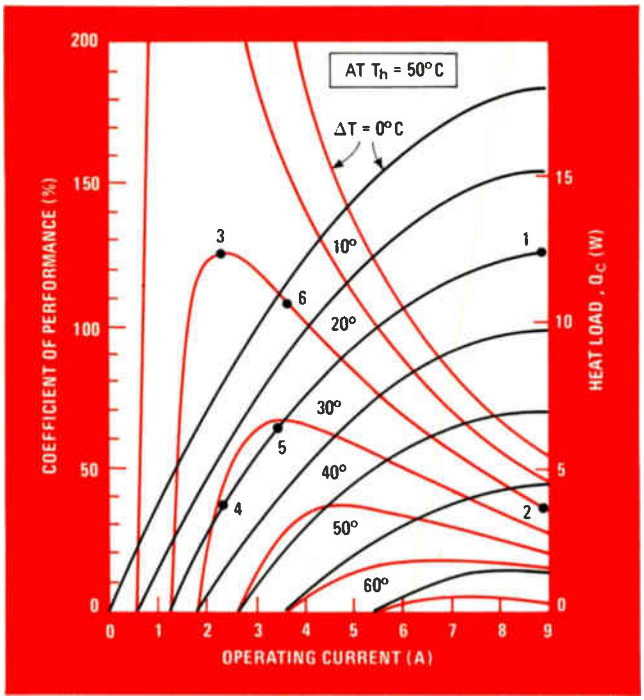
Specification curves from competing manufacturers



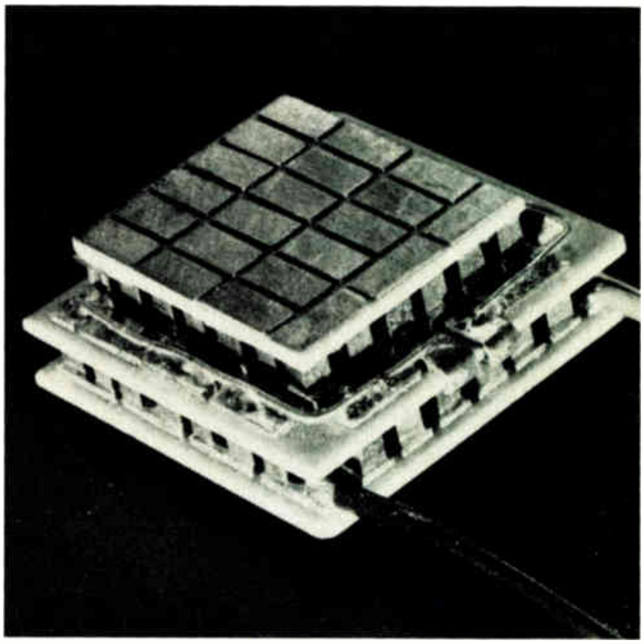
4. Cool instruments. Air-to-air thermoelectric heat exchanger cools interior of sealed electronic instrument cabinet. Exchanger is mounted through cabinet wall with its cold side facing the interior. TE modules are sandwiched between two heat sinks.

are not always directly comparable. For instance, some manufacturers evaluate their device performance in a vacuum instead of air. Under these conditions, maximum ΔT can be 10% to 15% higher. Similarly, mounting conditions during test should be carefully compared. If the TE module is soldered to the test fixture heat sink, it will perform better than it does with a thermal grease and a mechanically clamped mounting.

Operating temperature ranges of competing devices also tend to vary. Standard modules from some manu-



5. Thermal performance curves. A typical thermoelectric module's performance curve relates the heat absorbed at the cold side, Q_c, and the coefficient of performance, COP, to the operating current at the fixed value of the hot-side temperature, T_h.



6. Cascade. TE modules can be connected thermally in series to increase ΔT. The copper pads visible on the top of the module allow modules to be thermally connected by soldering. These copper pads are not electrically connected to the semiconductor elements below.

facturers have a maximum T_h of 110°C compared with 150°C for similar units from other manufacturers. The devices' electrical connection techniques differ as well. Special bismuth solder must be used to connect to modules from some manufacturers, whereas standard lead-tin solder suffices for other manufacturer's modules.

Design example

TE cooling becomes attractive when 200 W of heat or less must be pumped in applications where some part of the system has to be cooled to temperatures below ambient. To increase heat pumping capacity, TE modules can be connected side by side, thermally in parallel. To increase ΔT they can be cascaded thermally in series, as shown in Fig. 6.

An example is the case of an object that generates 10 W of heat, where the designer wishes to maintain its temperature at 30°C or lower and the ambient temperature is 40°C. Referring back to Fig. 2a, heat must be actively pumped from the object that is to be cooled to the heat sink by the TE module. T_h, the temperature of the heat sink, is higher than T_a, the ambient air temperature. Therefore, the heat the module sends onto the sink will flow out into the ambient by natural (or forced) convection.

As a first step in solving any TE design problem, the designer should calculate the total heat load, Q_C, considering both active heating sources and a phenomenon known as heat leak. Active heating sources are components on the cold surface that generate heat—those that dissipate electrical power, for example. Heat leak is defined as the passive absorption of heat into the cold surface from the warmer surrounding ambient and often represents a significant portion of the total heat load.

Calculating heat leak is a complicated procedure, in which the TE manufacturer's applications department can offer assistance to the user. The major factors involved in calculating heat leak are the temperature difference between the ambient and the object being cooled, the object's surface area, and the thickness of its surface insulation.

In general, heat leak is inversely proportional to insulation thickness (as insulation thickness doubles, heat leak is halved). In contrast, heat leak is linearly proportional to the cooled object's surface area. As surface area increases, heat leak increases linearly.

The slope of the increase depends mainly upon the magnitude of the temperature difference ($T_a - T_c$). For instance, with a 1-in. polyurethane insulation and a temperature difference of 10°C, heat leak increases at a rate of 22 W/1,000 in.^{2} of surface area. With a temperature difference of 70°C, the rate is 73 W/1,000 in.^{2} of surface area.

Total heat load, then, is the sum of the active heat sources and heat leak. This example assumes active generation of 10 W and a heat leak of 2 W, for a total heat load of 12 W. Total heat load is designated Q_{cT}.

Next, a designer must determine the required heat-sink temperature. Selecting a base temperature, T_h, determines the size and type of heat sink needed as well as the number of TE modules necessary to handle the heat load. As T_h moves closer to the ambient air temperature, T_a, fewer modules and less electrical input power are required, though a larger and more effective heat sink is needed.

In this example, the heat-sink base temperature is 10°C above ambient, or T_h = 50°C. Then T_h = 50°C; T_c = 30°C or lower; ΔT = 20°C; and Q_{cT} = 12 W.

To complete the design the following parameters must be determined: input current, I; input voltage, V; input power, P; heat rejection, Q_h; the number of TE modules that are necessary; and the heat sink required.

A designer has several choices in this example. He can design for maximum Q_c (heat absorbed) per module, minimizing the number of modules required. He can maximize COP, minimizing electrical input power. Or he can do a compromise or practical design. The table summarizes the results of these three approaches for the example under discussion.

Maximizing heat absorption

The first approach is designing for maximum Q_c per module and therefore for a minimum number of modules. From the performance curves of Fig. 6, with $\Delta T = 20°C$, a maximum Q_c of 12.5 W occurs at I = 9 amperes (point 1 on the curves). Since 12.5 W exceeds the required Q_{cT} of 12 W, only one module will be needed.

With $\Delta T = 20°C$ and I = 9 A, COP is 40% (point 2 on the curves). The designer can then calculate power input as:

$$P = Q_c/COP = 12.5/0.40 = 31.3 \text{ W}$$

Input voltage becomes:

$$V = P/I = 31.3/9 = 3.5 \text{ V}$$

Heat rejected at the hot side of the TE module, Q_h, is the sum of Q_c and electrical power dissipated by the module, P, or:

$$Q_h = Q_c + P = 12.5 + 31.3 = 43.8 \text{ W}$$

Finally, the required thermal resistance of the heat sink is found from:

$$\theta = (T_h - T_a)/Q_h = 10°C/43.8 \text{ W} = 0.23°C/W$$

Maximizing COP

As a second alternative, the designer can choose to maximize COP, which minimizes the electrical input power required and reduces the heat sink requirements, increasing the required thermal resistance.

From the curves of Fig. 6, for a ΔT of 20°C, a maximum COP of 125% is found at I = 2.3 A (point 3 on the curves). The corresponding Q_c is 3.3 W (point 4 on the curves).

The number of modules required to meet the total heat pumping capacity of 12 W, Q_{cT}, is:

$$N = Q_{cT}/Q_c \text{ (per module)} = 12 \text{ W}/3.3 \text{ W} = 3.6$$

Therefore, four modules will be needed. Next, the total electrical power is calculated as:

$$P = (Q_c \text{ [per module]}/COP)(N) = (3.3/1.25)4 = 10.6 \text{ W}$$

When the four modules are connected in series, the input voltage becomes:

$$V = P/I = 10.6/2.3 = 4.6 \text{ V}$$

Heat rejection from the four modules is calculated as:

$$Q_h = Q_c \text{ (per module)} \times N + P = 3.3 \times 4 + 10.6$$

SUMMARY OF RESULTS FOR THREE THERMOELECTRIC DESIGN ALTERNATIVES

Parameter	Maximum power dissipation	Maximum coefficient of performance	Practical design
Input current, I (A)	9	2.3	3.4
Input voltage, V (V)	3.5	4.6	3.6
Input power, P (W)	31.3	10.6	12.4
Heat rejection, Q_h (W)	43.8	23.8	25.4
Number of TE modules	1	4	2
Required heat-sink thermal conductivity (°C/W)	0.23	0.42	0.39

$$Q_h = 23.8 \text{ W}$$

Finally, the heat sink's required thermal resistance, θ, is found from:

$$\theta = T_h - T_a/Q_h = 10°C/23.8 \text{ W} = 0.42°C/W$$

Practical design

In the final approach, the designer may wish to compromise between the preceding alternatives in order to accommodate some other system constraint such as voltage, current, or space availability.

For example, space constraints may allow the use of no more than two modules. Each of the modules must therefore pump at least half of Q_{cT}:

$$Q_c = Q_{cT}/N = 12 \text{ W}/2 = 6 \text{ W}$$

With a ΔT of 20°C and a Q_c per module of 6.5 W (and a 0.5-W design margin), the curves of Fig. 6 predict 3.4-A operation (point 5 on the curves). At 3.4 A and a ΔT of 20°C, COP is found to be 105%.

The total electrical power consumed by the module is:

$$P = (Q_c/COP)\,N = (6.5/1.05)2 = 12.4 \text{ W}$$

With two modules connected electrically in series:

$$V = P/I = 12.4/3.4 = 3.6 \text{ V}$$

Total heat rejection is then calculated as:

$$Q_h = Q_c \times N + P = 6.5 \times 2 + 12.4 = 25.4 \text{ W}$$

Finally, the heat sink's required thermal resistance is found from:

$$\Theta = (T_h - T_a)/Q_h = 10°C/25.4 = 0.39°C/W$$

Mechanically, thermoelectric modules are only as strong as the semiconductor materials used in their fabrication. These units should never be designed as the mechanical supporting members of an assembly, since stress can damage them.

TE modules can be mounted in various ways. They can be clamped between a heat sink and the object to be cooled, or epoxied or soldered to a heat sink. Mechanical clamping generally gives a more versatile mounting, but soldering offers a better thermal connection.

In general, mounting surfaces should have a flatness of better than ±0.001 in. Furthermore, when mounting several modules side by side, their thicknesses should match to within 0.002 in. □

Counter indicates when its probe is compensated

by Dale Carlton
Tektronix Inc., Beaverton, Ore.

Using a scope probe with a counter or other measuring instrument has a number of well-known benefits—namely, it ensures minimal source loading, physical ease of circuit connection, and minimum distortion of high-frequency signal components. Still, matching the probe to the counter's input impedance to secure wideband response can be troublesome, especially if the elements needed to perform the standard compensation procedure (a scope and a source of square waves) are not available and the input impedance of the scope and counter are not identical. Fortunately, the counter's own input-trigger circuit may be employed as a peak detector to indicate that proper probe compenstion has been achieved.

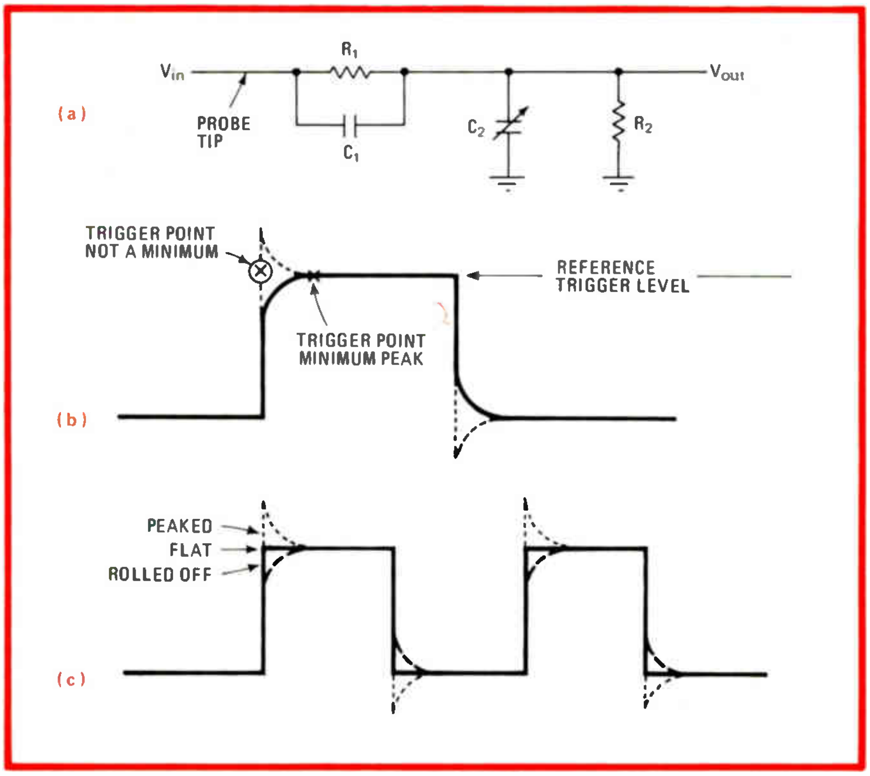
The equivalent input circuit of the typical 5× and 10× (attenuating) probe appears as in (a), where C_1 is the ac coupling capacitor and C_2 represents the probe's compensating capacitance, cable capacitance, and the input capacitance of the measuring instrument. R_1 is the dc coupling resistance. R_2 is the instrument's input resistance. For flat response, the product of R_1 and C_1 should be equal to the product of R_2 and C_2.

Compensation is achieved by applying to the probe/counter a 1-kilohertz square-wave signal having a rise time of less than 100 microseconds. The amplitude of the square wave should be as large as the counter's dynamic range will allow. The counter should be set to trigger on the low-frequency components of the square wave so that a reference level is established. Then the probe's compensating capacitor is adjusted so that the counter will trigger on the highest-frequency components of the signal.

Specifically, the counter should be set to the 1× position. The counter's function control is then set to the frequency, period, or event position, so that the counter's display or input-trigger LED will indicate triggering when the square wave is applied.

To establish the reference level, the probe is adjusted so that triggering occurs in the waveform's so-called roll-off region. This is done by setting C_2 and the trigger level in turn so that triggering occurs at the peak of the acquired signal and at the minimum level required to ensure consistent operation. The point at which this occurs for a given trigger level is reached when an increase or decrease in C_2 does not stop triggering. If the acquired signal could be observed, it would appear as in the illustration in (b).

For compensation at the high frequencies, the response of the probe must be flattened (c). This is achieved by setting the trigger level to a position where triggering just stops or is erratic. C_2 is then adjusted to



Match. Universal counter's display or trigger LED is used to indicate that probe/circuit's elements $R_1C_1C_2$ (a) are matched to input impedance (R_2) of measuring device. Procedure used is to first position triggering region on roll-off of input-signal curve (b) with C_2 and counter's trigger-level control. Probe will be compensated over a wide band after C_2 is peaked (c) to detect high-frequency components of square wave.

the point where triggering is again reliable, and probe compensation is complete.

Availability of a constant-amplitude sine-wave oscillator greatly simplifies the compensation procedure. Setting sine-wave frequency at 100 hertz and a convenient amplitude, the user need only set the counter's trigger level at the sine wave's peak voltage. The frequency is then increased to 10 kHz or higher and C_2 is adjusted to just restore triggering. Typically, the flatness achieved by this method will be 2%. In equation form, $\%F = (AS)(100)/V_{in\ p\text{-}p}$, where A is the probe's attenuation factor, S is the settability or trigger-level resolution, and $V_{in\ p\text{-}p}$ is the peak-to-peak amplitude of the input signal.

Some counters have a tapered trigger-level knob and the maximum setability occurs at the 0-volt level. For best accuracy when using one of these counters, a waveform that is square near 0 V or an offset sine wave that has peaks near 0 V should be used.

It should be noted that many of the newer counters now available have a large input capacitance, and some conventional scope probes may not have sufficient compensating capacitance. Using such a probe in this situation reduces system sensitivity above 1 kHz and could cause additional time-interval measurement error. □

Engineer's notebook is a regular feature in Electronics. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.

Calculator notes

TI-59 solves network equations using complex matrixes

by Frans Cornelissen
Belgische Radio en Televisie, Brussels, Belgium

Providing an even more flexible and compact means for analyzing electrical networks than the routine proposed by McIntyre[1], this TI-59 program uses the method of matrixes to solve the simultaneous equations that define the response of any three-mesh linear circuit. Once the components of the 3×3 complex matrix are known, a solution may be realized in less than three minutes.

The program solves the matrix equation:

$$[ABC] \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = [D]$$

where [ABC] represents the terms of the square matrix shown in (a), I_1 to I_3 are the unknown variables, and [D] contains V_1 to V_3, the complex driving functions. Contrary to McIntyre's routine, the matrix elements are presented to the calculator from top to bottom, left to right, as indicated by the subscripts of the variables. The subscript of the next variable to be stored also appears on the display.

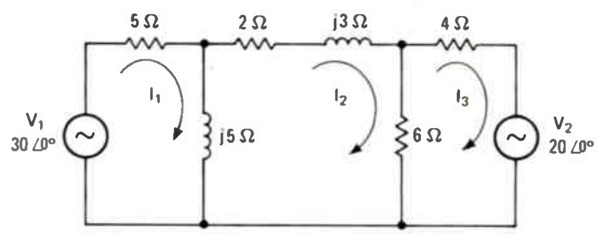
The real and imaginary components of the driving sources are then specified, whereupon the matrix determinant, Δ = [ABC], corresponding to the given circuit is readily found and the three currents I_1 = [DBC]/Δ, I_2 = [ADB]/Δ, and I_3 = [ABD]/Δ are calculated directly. Then these variables are displayed in both rectangular and polar form.

Consider the example where the program is applied to a three-mesh circuit whose matrix is found to be that shown in (b). Keying in the program and entering the data as given in the instructions yields the rectangular and polar representations of the aforementioned variables, as shown in (c). □

References
1. Chris McIntyre, "SR-52 solves network equations by finding complex determinant," *Electronics*, May 12, 1977, p. 121

(a)

$$\begin{bmatrix} R_0 \pm X_1 & R_6 \pm X_7 & R_{12} \pm X_{13} \\ R_2 \pm X_3 & R_8 \pm X_9 & R_{14} \pm X_{15} \\ R_4 \pm X_5 & R_{10} \pm X_{11} & R_{16} \pm X_{17} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$$



$$\begin{bmatrix} 5+j5 & 0-j5 & 0+j0 \\ 0-j5 & 8+j8 & -6+j0 \\ 0+j0 & -6+j0 & 10+j0 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} 30 & 0 \\ 0 & 0 \\ -20 & 0 \end{bmatrix}$$

(b)

(c)

	Δ	I_1	I_2	I_3
X	70.000	3.104	−1.325	−1.205
Y	620.000	−1.779	−1.117	0.670
θ	83.558	−29.812	220.131	150.904
R	623.939	3.577	1.734	1.379

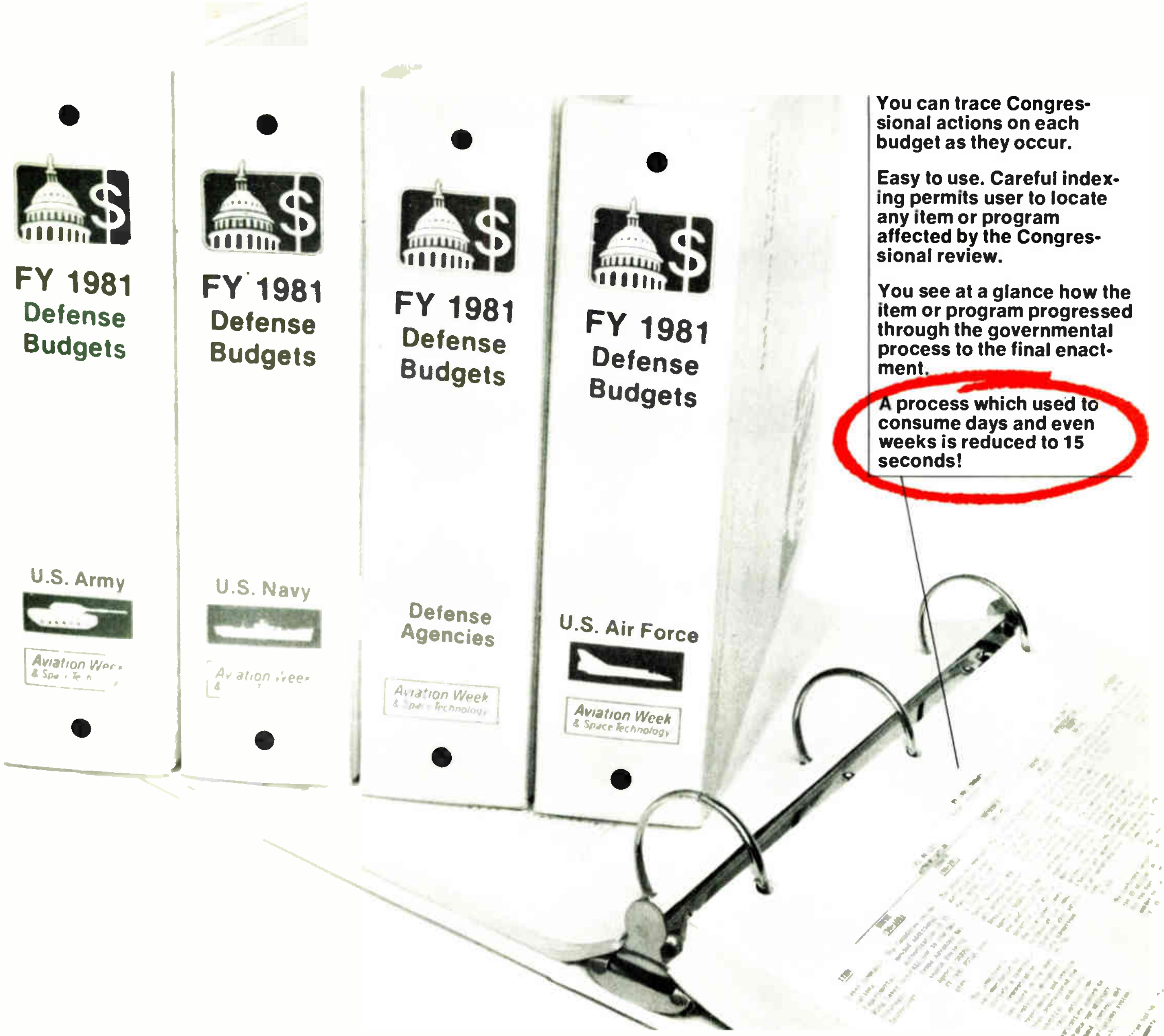
Linear algebra. TI-59 program utilizes method of matrixes (a) to solve mesh equations characterizing small linear networks. In typical example (b), matrix defining the network shown is presented to calculator, which yields the real and imaginary components of the dependent current variables I_1, I_2, and I_3 (c), represented both in rectangular and polar form. Total solution time is about three minutes.

TI-59 PRINTER LISTING FOR A 3 x 3 COMPLEX MATRIX

Loc	Key	Loc	Key	Loc	Key	Loc	Key	Loc	Key	Loc	Key	Loc	Key	Loc	Key
000	LBL	045	9	090	09	135	SUM	180	38	225	RCL	270	A	315	2
001	A	046	STO	091	X	136	33	181	X²	226	32	271	LBL	316	2
002	PRT	047	36	092	RCL	137	GO•	182	=	227	X	272	C	317	STO
003	ST•	048	D'	093	16	138	36	183	STO	228	RCL	273	3	318	50
004	37	049	1	094	–	139	RTN	184	37	229	38	274	8	319	PRT
005	1	050	+/–	095	RCL	140	LBL	185	2	230	+	275	STO	320	R/S
006	SUM	051	PRD	096	10	141	D'	186	2	231	RCL	276	50	321	2
007	37	052	12	097	X	142	0	187	STO	232	33	277	PRT	322	3
008	RCL	053	PRD	098	RCL	143	STO	188	50	233	X	278	R/S	323	STO
009	37	054	13	099	15	144	35	189	2	234	RCL	279	3	324	51
010	PRT	055	LBL	100	–	145	RC•	190	3	235	39	280	9	325	PRT
011	R/S	056	E'	101	RCL	146	35	191	STO	236	)	281	STO	326	R/S
012	LBL	057	RCL	102	11	147	EX•	192	51	237	÷	282	51	327	LBL
013	E	058	08	103	X	148	34	193	C'	238	RCL	283	PRT	328	RCL
014	CMS	059	X	104	RCL	149	ST•	194	2	239	37	284	R/S	329	RC•
015	CP	060	RCL	105	14	150	35	195	0	240	=	285	SBR	330	50
016	CLR	061	16	106	=	151	1	196	STO	241	ST•	286	RCL	331	PRT
017	PRT	062	–	107	STO	152	SUM	197	50	242	50	287	1	332	R/S
018	R/S	063	RCL	108	31	153	34	198	2	243	(	288	8	333	X ⇌ T
019	LBL	064	09	109	RCL	154	SUM	199	1	244	RCL	289	STO	334	RC•
020	B'	065	X	110	00	155	35	200	STO	245	33	290	50	335	51
021	2	066	RCL	111	X	156	(	201	51	246	X	291	PRT	336	PRT
022	7	067	17	112	RCL	157	5	202	C'	247	RCL	292	R/S	337	R/S
023	STO	068	–	113	30	158	–	203	1	248	38	293	1	338	INV
024	36	069	RCL	114	–	159	RCL	204	8	249	–	294	9	339	P/R
025	GTO	070	10	115	RCL	160	35	205	STO	250	RCL	295	STO	340	PRT
026	E'	071	X	116	01	161	)	206	50	251	32	296	51	341	R/S
027	4	072	RCL	117	X	162	GE	207	1	252	X	297	PRT	342	X ⇌ T
028	3	073	14	118	RCL	163	01	208	9	253	RCL	298	R/S	343	PRT
029	STO	074	+	119	31	164	45	209	STO	254	39	299	SBR	344	R/S
030	36	075	RCL	120	=	165	RTN	210	51	255	)	300	RCL	345	RTN
031	6	076	11	121	SUM	166	LBL	211	LBL	256	÷	301	2	346	LBL
032	STO	077	X	122	32	167	B	212	C'	257	RCL	302	0	347	D
033	34	078	RCL	123	RCL	168	B'	213	0	258	37	303	STO	348	2
034	D'	079	15	124	00	169	RCL	214	STO	259	=	304	50	349	4
035	1	080	=	125	X	170	32	215	32	260	ST•	305	PRT	350	STO
036	+/–	081	STO	126	RCL	171	STO	216	STO	261	51	306	R/S	351	34
037	PRD	082	30	127	31	172	38	217	33	262	RTN	307	2	352	D'
038	00	083	RCL	128	+	173	RCL	218	2	263	LBL	308	1	353	R/S
039	PRD	084	08	129	RCL	174	33	219	4	264	A'	309	STO		
040	01	085	X	130	01	175	STO	220	STO	265	2	310	51		
041	GTO	086	RCL	131	X	176	39	221	34	266	3	311	PRT		
042	E'	087	17	132	RCL	177	X²	222	D'	267	STO	312	R/S		
043	1	088	+	133	30	178	+	223	B'	268	37	313	SBR		
044	3	089	RCL	134	=	179	RCL	224	(	269	GTO	314	RCL		

Instructions

- Key in program
- Initialize:
  *CMs, E
- Enter all matrix coefficients:
  (0), A, (1), A, (2), A . . . (17), A
  The number 18 is displayed after the last data entry
- Press A'
  The number 24 will be displayed
- Specify driving sources
  (24), A, (25), A, (26), A . . . (29), A
  The number 30 will be displayed after the last data entry
- Press B
  The program finds the matrix determinant, $\Delta = |ABC|$, and separately stores its real and imaginary components in the appropriate data registers. The determinant is also stored away in polar form. Similarly, $I_1 = |DBC|/\Delta$, $I_2 = |ADB|/\Delta$ and $I_3 = |ABD|/\Delta$ are calculated
- Press C
  Number 38 is displayed. Successive pressing of the R/S key yields, in succession, 39, Δ_{real}, Δ_{imag}, Δ_{θ}, Δ_R, followed by 18, 19, I_{1X}, I_{1Y}, $I_{1\theta}$, I_{1R}, 20, 21, I_{2X}, I_{2Y}, $I_{2\theta}$, I_{2R}, 22, 23, I_{3X}, I_{3Y}, $I_{3\theta}$, I_{3R}



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ELECT7/31/80

Engineer's newsletter

Welded wire suspends cable inexpensively

A computer manufacturer recently found it needed a lightweight, low-cost component for suspending electric cable inside the frame of one of its larger machines. As it turned out, plastic was light enough, but proved too costly and also failed Underwriters Laboratories flame-retardant specifications for office equipment.

The solution, found by engineers at E. H. Titchener & Co., was a frame of welded steel wires that has a black, mar-resistant epoxy finish and easily conforms to UL requirements. The dielectric qualities of the electrostatically applied epoxy coating **helps eliminate any possibility of electric shock,** while the unit's inherent conductivity prevents static charge from building up. For more information, contact E. H. Titchener & Co., 9 Titchener Place, Binghamton, N. Y. 13902.

How to pick the right small computer

An initial mistake in selecting a small computer can be costly in more ways than one. So a checklist of 322 points has been devised to aid the potential computer user in making an intelligent choice of computer features and purchase plans.

The questions it asks also cover display, keyboard, printer, and controller features, as well as the costs of software, maintenance, and training, to help the would-be customer determine **which vendor comes closest to satisfying all his or her requirements.**

The "Checklist/Guide to Selecting a Small Computer" is available solely from its publisher, Pilot Books of 347 Fifth Ave., New York, N. Y. 10016 at $5 a copy, postpaid.

Hidden 8085 op codes may be invalid

While there might be a thrill in uncovering the existence of unspecified operating codes in a microprocessor and exploiting them, there is great risk in it, too. For example, according to sources outside the company, a recent mask change on Intel Corp.'s 8085 central processing unit may have eliminated those hidden instructions that were given last year in an Engineer's Notebook [*Electronics*, Jan. 18, p. 144, 1979], although Intel is unwilling to comment.

There's a moral here—taking advantage of a hidden instruction in a calculator is one thing, but it's **simply not advisable to design around any device feature not specified on the data sheet.**

Update your knowledge of wire and cable

Wiring and cabling, the warp if not the woof of electronic systems, are the subject of a seminar to be held in central New Jersey this fall (Oct. 15–17) by the Center for Professional Development. The course will cover wire types, connectors, and terminations; **insulation displacement connectors for flat cabling, as well as flat cable;** ribbon coaxial cable; fiber optics; and the performance and testing of interconnections.

Director of the course will be John W. Balde of Western Electric's Research Center in Princeton, N. J. Cost will be $575.

For additional details, write or call the Center for Professional Advancement, P. O. Box H, East Brunswick, N. J.; (201) 249-1400. **-Jerry Lyman**

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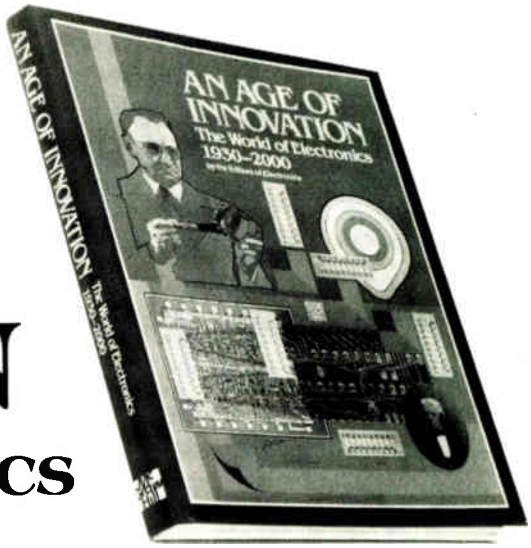

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EL 1

Generator delivers new byte every 20 ns

Built with off-the-shelf emitter-coupled logic, programmable unit produces 100-MHz digital waveforms using pipeline processing

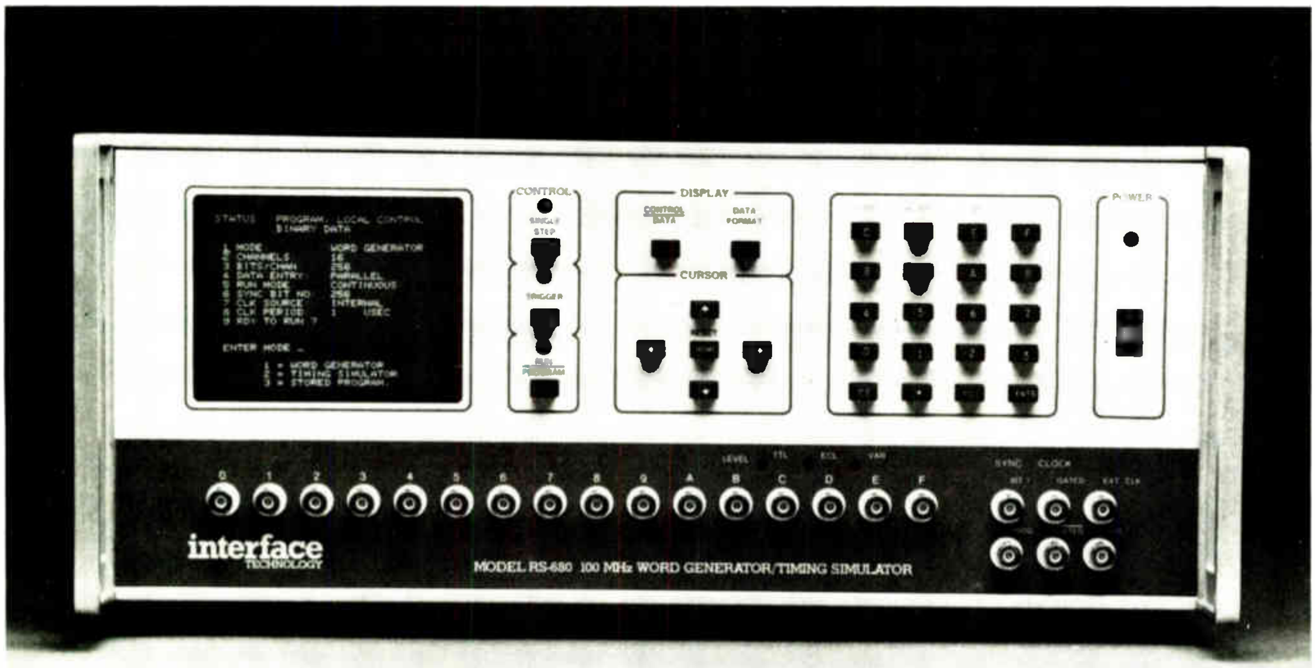
by Larry Waller, Los Angeles regional bureau manager

Commercial automated test equipment can generate byte-wide test signals at 50 MHz—fast enough for most production testing. But for engineers working at the leading edge of semiconductor technology, such systems may not be fast enough. Interface Technology is introducing a programmable digital-waveform generator that puts out eight digital signals simultaneously at 100 MHz, with a skew of only 2 ns between channels [*Electronics*, July 17, p. 33]. The RS-680 makes it much easier for engineers needing this speed to put together their own test systems.

Until now, builders of high-speed test systems have had to choose between commercial word generators capable of delivering eight outputs at 50 MHz, such as the Hewlett-Packard 8016A, and faster pulse generators that provide only one or two outputs. The RS-680 not only provides 8 channels at 100 MHz, but can deliver 16 at 50 MHz. Thus it is capable of generating test data for the latest 16-bit microcomputers. A total of 4,096 bits of memory can be allocated for storing the waveforms to be reproduced.

Unlike word generators that generate bit-parallel bytes at one user-selected frequency, each of the eight RS-680 channels can be individually programmed to produce a digital waveform of varying frequency; up to 256 states can be programmed with resolution of 10 ns for from one to eight channels. The unit can therefore recreate the complex timing schemes required by some of the most recently developed integrated circuits.

To achieve the RS-680's speed, Interface Technology based its design on emitter-coupled-logic devices, since they are the fastest parts available commercially. But the designers did not have the wealth of parts available for bipolar or MOS designers to choose from. Also, they found that ECL's reputation for being slippery to work with is well earned. For example, the edges of waveforms produced by ECL parts tend not to be uniform. They also found that ECL memory, in spite of being the fastest available, was not



fast enough for their purposes, its 20-ns access times being only half the speed needed.

To match edge outputs, therefore, the final circuitry has been designed with just one ECL gate between registers. The memory-access speed limitation has been overcome by using an architecture in which two waveforms can be generated simultaneously—much as in the pipeline processing schemes used in high-speed computers.

Waveform timing programmability was attained by using the RS-680's 100-MHz reference oscillator in conjunction with a separate timing memory, in which the variable signal transition times are stored by the user. When the RS-680 begins to reproduce these varying waveforms, it accesses both the data that defines the waveforms' states and the timing data that specifies how long the states will stay in the output register. The timing bits go to a countdown circuit that counts against the reference oscillator and advances to each set of states in turn, changing the waveforms or not depending on how they have been programmed.

Although the unit is capable of providing complex TTL- or ECL-level waveforms, its operation is not complex. The user is presented with a menu for manual programming; all he or she need do is choose the operating mode and enter the pertinent data. It is likely, however, that the digital waveform generator will end up as part of a system, so IEEE-488 and RS-232-C interfaces are offered as options.

The basic RS-680, without a system interface, is priced at approximately $15,000, and each interface option is priced at $795. For an additional $150, an erasable programmable read-only memory card (without the E-PROMs) can also be obtained for storing frequently used patterns and keeping them ready for quick transfer to the unit's operational random-access memory. Deliveries are scheduled to begin this month.

Interface Technology, 150 East Arrow Highway, San Dimas, Calif. 91773. Phone Stan Kubota at (714) 599-0848 [338]

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Instruments

Tester fits many tools into one box

Unit checks digital and analog parameters of microsystems in the field

Signature analysis may prove to be one of the most effective methods for testing microprocessor-based products operating in the field, but it is not the complete answer, according to Solartron Electronics group, a British subsidiary of Schlumberger. The company believes there is still considerable need for complementary logic-testing methods, and for basic measurement functions as well.

To meet that need, Solartron plans a third-quarter U. S. introduction of a multifunction instrument designed specifically for testing microprocessor-based products. Recently unveiled in Europe as the Locator, the instrument can apply any of a number of tests to an obstinate fault, including such procedures as signature analysis.

Among the procedures is trace analysis, a complementary technique borrowed from the world of advanced automatic test equipment. According to digital instrument product manager, Brian L. A. Kett, trace analysis is most useful in checking feedback loops, where signature analysis often fails. Kett explains that error signals at faulty nodes can propagate through the system in time with each clock transition, until all nodes generate a fault signature. Trace analysis catches the fault before it travels through the system; it also allows the engineer to trace the fault signal back to the earliest time frame and the first node at which it occurred.

The Locator's 7-by-12-by-4-in. frame also houses frequency-measurement circuitry to check clock rates to 20 MHz with 1 Hz resolution. For asynchronous logic functions, there is an event/transition counter, and a timer helps monitor the activity of, say, monostable vibrators, or the occurrence of interrupts.

Also in the package is an autoranging 3½-digit multimeter that eliminates the need for an additional hand-held unit. Four ranges are provided for each of five functions—ac and dc voltage, ac and dc current, and resistance. Maximum readings possible are 1,000 V dc, 500 V dc, and 2 A ac or dc. The meter also has resistance ranges and measures temperature from −10° to +150°C (read in Celsius or Fahrenheit).

A data-pod connector provides the interface between the test instrument and the unit under test; it connects to the system clock and trigger-pulse sources. An optional micropod makes it possible to test a microprocessor apart from its system with a specially devised emulator program. The pod also enables the operator to use that microprocessor to exercise the unit under test. To date, Solartron has pods designed for use with the 6800, 6802, and 8080; others are said to be in the works. The user may also store his own exercise program in a programmable read-only memory included in the system.

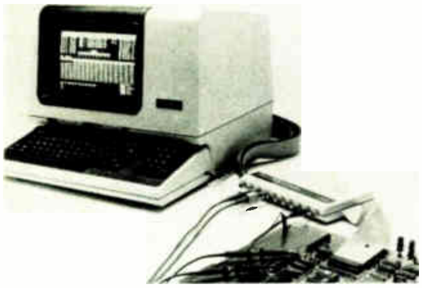
The Locator is scheduled for introduction in the U. S. sometime in September and is tentatively priced at about $4,000.

Sangamo Weston Inc., Solartron Instrument group, 2021 Business Centre Dr., Suite 113, Irvine, Calif. 92715 [351]

Development system emulates 4- to 32-bit microprocessors

The ECL-3211 microprocessor development system can link up to 64 stations and emulate any 4- to 32-bit microprocessor in real time. It provides in-circuit emulation of chips at up to 30 MHz, acting as a standalone system or accepting downloaded programs from a host computer. New emulator hardware does not have to be installed every time a new chip is introduced; only the software for the new chip and a plug-in adapter card for the chip family are needed for the system to operate.

A basic ECL-3211 includes an LSI-11/2 processor, 64 kilobytes of 210-ns random-access memory, a 1-megabyte double-density dual floppy disk, a 512-by-64-bit trace buffer, a terminal, a DEC RT-11 operating system and software, and the full hardware and software support for any one-chip family. It sells for $23,990. Full emulation support for each additional chip family,



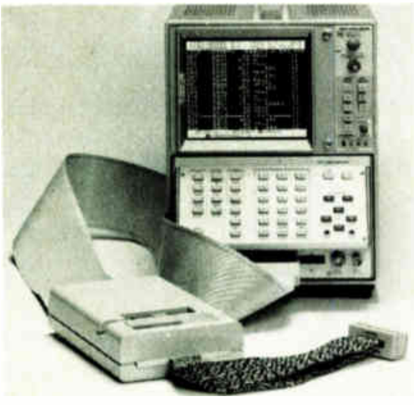
including assembler and linker, costs $1,500.

Emulogic Inc., 362 University Ave., Westwood, Mass. 02090. Phone (617) 329-1031 [353]

Logic analyzer handles both 8- and 16-bit microprocessors

By using a series of personality modules, the 7DO2 logic analyzer can adapt to the characteristics of 8- and 16-bit microprocessors targeted for design. These plug-in modules provide mnemonic decoding for the Motorola 6800 and 6802, Intel 8085, and Zilog Z80 8-bit processors and for the Intel 8086 and Zilog Z8002 16-bit units. Personality modules for the Motorola 68000 and Zilog Z8001 are being developed.

The analyzer can acquire up to 52 channels of state information in the synchronous mode at 10 MHz, using the clock of the system under test. For $3,975, the basic instrument contains 28 channels but can be expanded to handle 44 at additional cost. A timing option that sells for $1,500 has eight more channels that can provide asynchronous information using the 7DO2's own clock at up to 50 MHz. The unit's bus-oriented memory is 52 by 256 words. The logic analyzer is designed to plug into a Tektronix 7000-series oscilloscope.



Tektronix Inc., P. O. Box 1700, Beaverton, Ore. 97075. Phone (800) 547-1517 [354]

Codec tester allows direct a-d, d-a measurements

Codec manufacturers can get into the middle of a bit stream to make direct and separate analog-to-digital, digital-to-analog, as well as analog-to-analog measurements with the AMS-952 automatic measuring system. Half-channel testing of codecs is done using the μ255 encoding law.

Housed in a standard 72-in. rack, the AMS-952 is controlled by a Hewlett-Packard 9825S and includes a frequency-selective level meter, wideband noise meter, level generator, four-tone noise source, channel demultiplexer and generator, and impedance and switching panel. It sells for $98,000. The unit measures frequency response over the entire voice frequency range with accuracies of ±0.05 dB and also measures 60-Hz and out-of-band rejection characteristics. It measures signal-to-distortion values to better than 40 dB. Level-tracking measurements can be made in 0.1-dB steps.

W&G Instruments Inc., 119 Naylon Ave., Livingston, N. J. 07039. Phone (201) 994-0854 [355]

IEEE-488-bus instrument controller sells for $3,495

A Z80A-based instrument controller for use on the IEEE-488 bus is priced at $3,495 but has features found on more expensive controllers. The Direktor can alternatively be used as a general-purpose microcomputer system.

The general-purpose interface-bus controller contains two Z80A microprocessors with 4-MHz clock frequencies, one for system and screen-related functions and one to be down-loaded by the host computer to execute disk input and output using direct-memory access. The controller includes 65 kilobytes of dynamic random-access memory, 242 kilobytes of mass storage capacity on two Shugart double-density mini-floppy-disk drives, a cathode-ray-tube display, a keyboard, an IEEE-488 controller port, and two RS-232 ports with selectable parity and stop bits and baud rates up to 9,600 b/s.

Software includes a CP/M disk-operating system and an extended-disk Basic interpreter to control the GPIB port. An upgrading kit to convert Intertec Data System's Superbrain computer into a GPIB controller sells for $895 in single quantities. Deliveries of the instrument controller start this month.

The Harrex Corp., P. O. Box 249, Kenmore, Wash. 98028. Phone (206) 488-4552 [356]

Function generator lets user draw his own waveform

The Z80-based MDE-8000 programmable function generator for biomedical applications lets the user draw the waveform he wants to reproduce. The wave shape to be generated is defined on a digitizing pad with a pen. Resolution is 0.2 mm per digitized sample.

The time base may be selected to generate the drawn form in less than a second or up to 100 seconds. Waveforms may be repeated or several different forms may be cascaded. The unit stores data for up to 32 seconds. The MDE 8000 can drive up to four independent amplifiers and create four waveform sequences with lengths of up to 8 seconds apiece. Output frequency response is dc to 50 Hz. Full-scale, adjusted calibrated outputs are up to ±5 mV and ±5 V.

The generator, with pad, pen, and a digital cassette recorder for filing and later retrieval of waveform information, sells for $3,300 and can be delivered within 60 days.

Medical Data Electronics, 4726 Daleridge Rd., La Canada, Calif. 91011. Phone (213) 790-8152 [358]

Semiconductors

New PALs can do arithmetic, too

Programmable-array logic units expand to perform more ALU functions

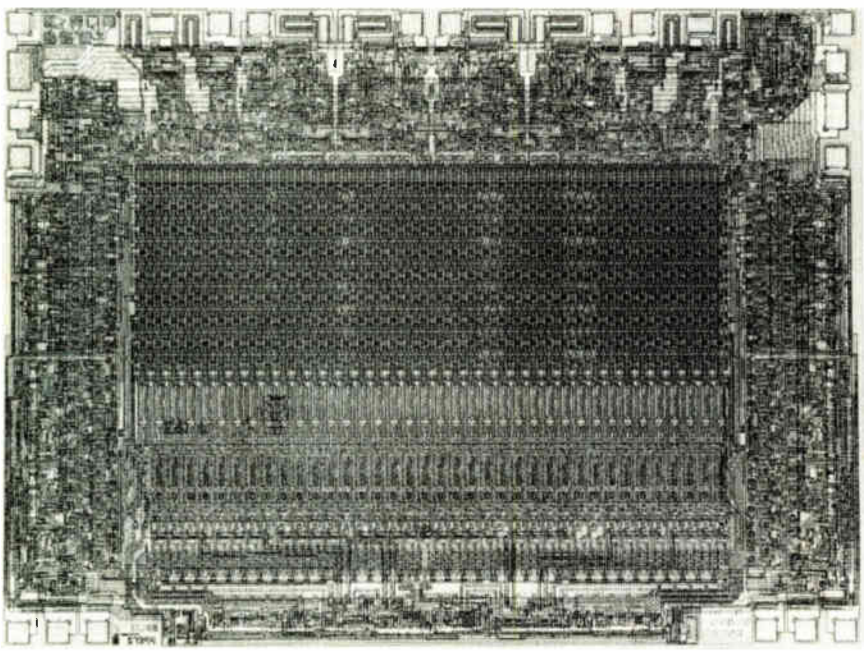
Two new members have been added to the 13-member family of programmable-array logic (PAL) devices introduced in 1978 by Monolithic Memories Inc. Those early components gave designers a programmable alternative to the 7400 series of TTL devices, capable of performing all or most of the 7400 functions but requiring only one quarter the number of circuit components. The new devices add complex arithmetic functions to the tasks already performed by existing members, thus rounding out the company's 20-pin PAL family.

Designated the 16A4 and 16X4, the new PALs measure 19,000 mil^2 and are the largest made with MMI's bipolar process. Containing four registers and four programmable input/output ports each, they introduce several notions new to small and medium-sized PALs. For instance, both the 16A4 and 16X4 contain exclusive-OR gates and gated feedbacks that allow the user to perform arithmetic functions, like addition and counting.

New concepts for PALs. According to John Birkner, MMI's product planning manager for programmable devices, the gated-feedback feature combines a feedback term with an input term in a decoder and thus forms all possible functions of two variables, including "always on" and "always off." The exclusive-OR feature groups two arithmetic products into a summing device, or a 1-bit adder (A + B). "This gives the unit the ability to add, without gobbling up product terms," he notes.

However, the 16A4 features a third new concept for PALs, called "parallel carry," that makes it possible to program the device to perform most of the functions of an arithmetic and logic unit (ALU). The parallel feature, Birkner explains, represents a fixed pattern of additional products that enable the formation of a 4-bit adder.

The principal application of the 16A4 is as an ALU accumulator, according to Birkner. In contrast with ALUs built with conventional logic, such as the 74181 Schottky TTL series, the 16A4 has an on-board accumulator and needs no additional device to perform that function. Also, it has three output states, as opposed to the straight drive of the 74181, which requires an additional device, an octal buffer, to achieve a three-state output. What's more, the 16A4 is housed in a skinny 20-pin dual in-line package and thus occupies less space than the 24-pin package of the 74181.



The 16X4, on the other hand, is suited for such applications as between-limits comparison or as a 4-bit up/down counter with shift. "In many systems applications, it is desirable to keep a running check on the data passing certain points in the system," Birkner says. "This can be done for system security or simply as part of system diagnosis and self-checking."

Limit-switching. Sometimes the limit checker may search for specific values. At other times the need may be for missing values, values in a specific range, or those out of a certain range. The last might occur in a microcomputer bus-watching application, for example, where the gated-feedback feature is used to continually compare a value in a registered comparator with a value on the bus.

Commenting on the 4-bit up/down counter with shift, Birkner notes it is possible to do "limited counting" without the exclusive-OR feature offered in the 16X4. "However, you use up most of the products, and not much is left over for other functions. But with the exclusive-OR feature," he points out, "you can do extensive counting."

With the addition of these new PALs, each of which has a typical power dissipation of 800 mW, Birkner claims that "we now have a family approach that allows a designer to use one generic family of PALs to completely replace 7400 series random logic."

Both the 16A4 and 16X4 are priced at $39 each in 100-piece quantities. Delivery takes four weeks from receipt of order.

Monolithic Memories Inc., 1165 East Arques Ave., Sunnyvale, Calif. 94086. Phone (408) 739-3535 [411]

8-bit-wide interface circuits offer low power, high speed

As an alternative to low-power Schottky diodes in bus-oriented systems, a family of Iso-CMOS octal interface circuits offers high speed together with low power. The circuits' gate delays are typically 5 ns. This fast gate propagation speed has been achieved by using an oxide-isolated silicon-gate process that minimizes the inherently long time constants of traditional metal-gate complementary MOS. As examples of the high speeds and low-power features, the MD74SC373 latch has a 20-ns propagation delay, and the MD74SC241 bus buffer dissipates 0.5 mW.

Other circuits offered include decoders, demultiplexers, and three-state octal buffers and line drivers. Each of the 20 devices operates over −40° to +85°C with a 3-to-6.5-V supply. In quantities of 100 and up, they range in price from $3 to $4.50, depending on complexity. For example, the MD74SC374 latch in a plastic package is $4.38 apiece in these quantities. All circuits are available in samples and most are already available in production quantities.

Mitel Semiconductor, P. O. Box 13089, Kanata, Ottawa, Ontario, Canada K2K 1X3. Phone (613) 592-2122 [413]

Low-voltage zener diodes also provide low impedance

Avalanche zener diodes for regulating power supplies at 2.8 to 10 V exhibit sharp knees and dynamic impedance between 10 and 75 Ω. The diodes can be stored at −65° to 200°C and offer 400 mW of power dissipation and 1 V of maximum forward voltage at 100 mA. They come packaged in DO-7 cases, priced at about 25¢ each for large quantity orders. Samples are available from stock, and larger quantities take two weeks to deliver.

Compensated Devices Inc., 166 Tremont St., Melrose, Mass. 02176. [416]

Computers & peripherals

Terminal attaches to two computers

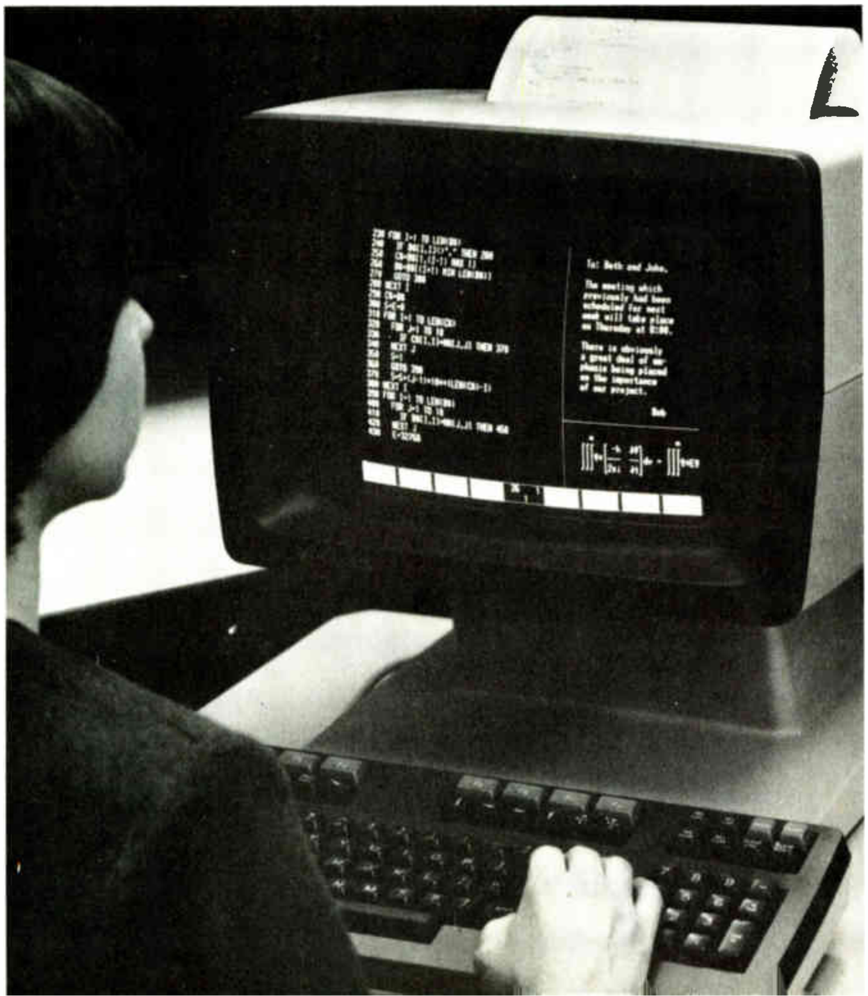
CRT terminal provides multiple work spaces and dual communication ports

Intended to aid program development and data-entry applications, a new microprocessor-based cathode-ray-tube terminal lets its display and display memory be divided into as many as four independent work spaces. The intelligent terminal also has two communication ports to facilitate its attachment to two different computers.

Dubbed the HP 2626A, the unit is the latest in the HP 2620 series of terminals from Hewlett-Packard's Data Terminals division. Considered by the company as a high-end smart terminal, the unit is aimed at the teletypewriter-compatible market with a collection of unusual features that HP says are not available from competitors.

The model 2626A is built around a proprietary 16-bit microprocessor fabricated in complementary-MOS on saphire. It has a 9;520-character display memory that can be configured to hold up to 119 display lines of between 80 and 160 characters each, so long as the total does not exceed the 9,520-character limit. This memory can be divided by the user into four independent work spaces any or all of which can be displayed on the 24-line, 80-character screen. Horizontal and vertical scrolling let all contents of a memory work space be displayed even if they are bigger than the display.

In addition, the terminal has two independent teletypewriter-compatible (RS-232-C) communication ports that can operate in full- or half-duplex, hardwired, or multipoint modes either synchronously or asynchronously at speeds of up to 9,600 b/s. The parts allow the terminal to be attached to two separate computers or to appear to a single computer as though it were two separate terminals.



Multitasking. These two features let operators use the terminal to perform more than one task simultaneously. For example, while data is being entered into one memory work space, another memory space can be transmitting previously entered data to the computer. Or the user can be connected to a computer as a data-entry terminal through one memory work space and communication port and simultaneously make inquiries of a data base—perhaps to refer to customer or product listings before entering an order, for instance—through another memory work space connected to the second communication port.

To aid programmers in setting up the terminal for data-entry applications, the 2626A has an interactive forms-design capability, programmable function keys whose labels will appear at the bottom of the display screen, and programmable audio prompts that offer 15 pitches with 16 duration periods and two volume levels.

Also, a thermal forms printer is available that can be integrated into the top of the unit. It reproduces the display exactly, including line drawings, special symbols, and inverse video and other displays.

The standard 2626A sells for $3,950, and the unit with the optional forms printer is priced at $5,100. Quantity discounts are available. Deliveries are currently estimated to be within 12 weeks after receipt of order.

Hewlett-Packard Co., 1507 Page Mill Rd, Palo Alto, Calif. 94304 [361]

Single-board multiplexer has dual interfaces

For PDP-11 minicomputer owners, MDB Systems Inc. is offering a single-board eight-line multiplexer. It combines RS-232 and 20-mA current-loop interfaces on one board, replacing two separate packages sup-

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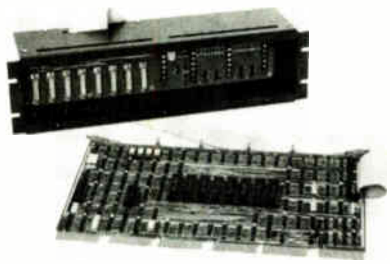
plied by Digital Equipment Corp. for this workhorse machine.

With PDP-11s, "it is common to have a mix-and-match array of terminals, printers, and other peripherals," says Sandy E. Traylor, MDB systems staff engineer. Since these peripherals often come with only the RS-232 or the current loop, the operator had to acquire two boards that take up two rack spaces.

Any of the eight multiplexer lines on the model DZ11AC board may serve either of the two interfaces, and expansion to 16 lines is accomplished by simply adding another board. Translation circuitry is built into the separate distribution box



that contains the cable connectors. The multiplexer operates on a programmed input/output and interrupt basis. Each line is programmable to a standard rate of from 50 to 19.2 kilobits/second, with variable character length and stop bits. Other programmable line features include parity, data set control, and break generation and detection. The multiplexer is transparent to standard DEC operating and diagnostic software.

A feature unique to the board is optical isolation for enhanced noise immunity, Traylor notes. It provides 3,000-V dc electrical insulation and 500 V/ms of transient immunity.

The unit comes with a hexadecimal module, distribution panel, test connectors, and 15-ft cables. In a standard cabinet, the distribution panel needs a 5¼-in. height. Electrical requirements are +5 V at 2.2 A, −15 V at 0.2 A, and +15 V at 0.3 A. A single DZ11AC costs $1,950.

MDB Systems Inc. 1995 North Batavia St., Orange, Calif. 92665. Phone (714) 998-6900 [363]

Components

Smart LEDs are visible from 8 ft

0.225-in.-high characters bring intelligent display capability to instruments

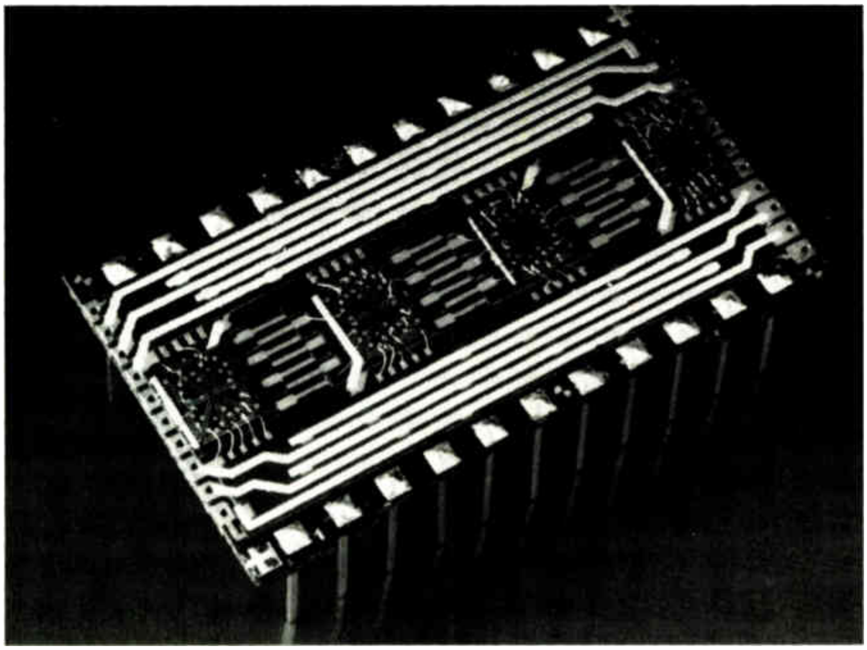
Litronix Inc.'s introduction three years ago of the first intelligent displays made the use of alphanumeric displays practical in such hand-held products as language translators. Now, by developing new light-emitting-diode chips that are, perhaps, the largest being produced, the affiliate of West Germany's Siemens AG expects to provide similar benefits for instrumentation panels.

The new intelligent display, designated the DL-3416, is a four-character module featuring 0.225-in.-high characters that, says Litronix product manager David M. Barton, "have two to four times the display area of prior units" and "are well suited to the display for instrument panels that must be viewed from some distance," typically 8 ft. Principal applications are expected to include process control monitors, medical systems, appliances, vehicles, and computer terminals, he adds, "where they are viewed by an operator who must be several feet away."

Like earlier intelligent displays from the company, the DL-3416 is driven just like a random-access memory, usually from a microprocessor. The display consists not only of four 17-segment (16 segments plus decimal) LED chips, but also of a bipolar digit driver, a complementary-MOS chip containing a small, 28-bit memory for storing character codes, built-in ASCII-character-generator read-only memory, and built-in multiplexer and LED segment drivers. It operates from one 5-V power supply and draws 200 mA of peak current—150 mA typically—and is compatible with standard TTL logic levels.

Stackable. Measuring 0.8-by-1.3-by-0.5-in., the DL-3416 modules are end-stackable to create displays of any length. In fact, a display system can be built with any number of DL-3416s since each digit of any module can be addressed independently and displays the character last stored until replaced by another, Barton notes. Access time is 500 ns.

Specified for operation over the temperature range of from −20° to +70°C, the DL-3416 has a wide off-axis viewing angle of ±50° and, at 25°C, the luminous intensity of eight segments at 5-V operation is specified at 0.5 millicandela. The module provides standard 0.1-in. pin spacing and is encapsulated in a solid plastic block for rugged applications.



In addition to standard display-blank and memory-clear functions, the DL-3416 has an independent cursor function that illuminates all segments of a digit position. However, the cursor is not a character and upon its removal the previously displayed character reappears.

Barton expects the new displays to be "especially useful in replacing whole groups of 'legend lights.' One intelligent display delivers any number of different messages to the viewer" and, adds the Litronix product manager, "messages are delivered sequentially or, in case of emergency, by priority."

Available 60 days after receipt of order, the DL-3416 will be priced at about $30 at the 1,000-piece level.

Litronix Inc., 19000 Homestead Rd. Cupertino, Calif. 95014. Phone (408) 257-7910 [341]

Droop rate of sample-and-hold amps drops with heat

Using bipolar Darlington transistors instead of field-effect transistors for its output-buffer input stage, the SMP-10 is a monolithic high-speed sample-and-hold amplifier with an extremely low droop rate over the operating temperature range of −55° to +125°C, says its manufacturer. With a 5,000-pF capacitor, the droop rate is as follows: at 25°C, it is 20 μV/ms maximum; at 125°C it is 300 μV/ms maximum; and at −55°C it is 100 μV/ms maximum. The temperature-compensation droop rate was achieved by trading off settling time—which is 7 μs—in the hold mode. The unit's acquisition time is typically 3.5 μs to 0.1% of full scale using the 5,000-pF capacitor. Other specifications for the device include a 10-V/μs slew rate and a 160-mW power dissipation. Packaged in a 14-pin dual in-line package, the SMP-10 sells for from $12.35 to $45.50 each. Delivery is from stock.

Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, Calif. 95050 [342]

Band-pass filter comes embedded in coaxial cable

The In-A-Cable band-pass filters in semirigid coaxial cable operate over a frequency range of 1,000 MHz to 18,000 MHz. The filter elements are implanted in a continuous section of cable that measures 0.141 in. in diameter and can be bent or formed to customer specifications. The company says the cable joins with any connectors that fit 0.141-in. cables, thus eliminating the need for the additional cable assemblies required by conventional, rigid tubular filters. The new devices operate over the temperature range of from $-54°$ to $+125°C$. Since the filters are made to suit each user, prices vary with specifications. Delivery time is eight weeks.

Uniform Tubes Inc., MicroDelay Division, Collegeville, Pa. 19426. Phone (215) 539-0700 [343]

Five-phase stepping motor yields 0.72° full-step angle

A five-phase permanent-magnet stepping motor provides a 0.72° (full) and 0.36° (half) step angle with accuracy to within ±3 min. Designated RDM 596/50, this device is for use in computer peripherals, instrumentation, and automation equipment. Measuring 85 by 55 mm, the device has a typical stepping rate of 30,000 kHz, a start or stop speed of up to 2,500 full steps per second, and a slew speed of up to 100,000 steps/second at 6,000 revolutions per minute. The motor sells for less than $60 each in large quantities. For prototype quantities, delivery is from stock; for large quantities delivery time is from three to six months.

Berger-Lahr Corp., Fritz von Mering, Fitzgerald Dr., Jaffrey, N. H. 03452 [344]

Power supplies

Supply regulation is 0.2% under load

Tight regulation of 30-W switching supply is designed into 4.25-by-7.75-in. board

The demand for multiple-output switching power supplies has been served by only a few firms. Now newcomer Power General Corp. is offering a line it claims has tighter regulation, as well as lower weight, volume, and prices, than other units of the same size.

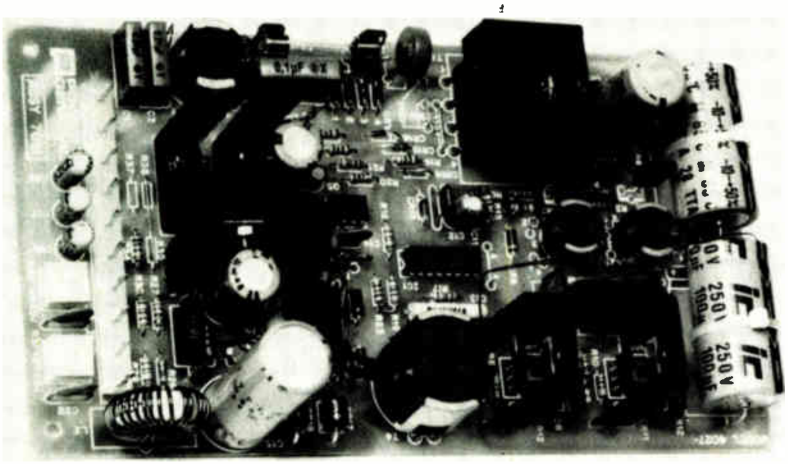
The 4027s are off-line switchers with 70% efficiency, +5%, −2%. They accommodate two broad voltage ranges without derating—90 to 130 V or 180 to 260 V—and can either be ordered for a specific range or jumpered for one or the other by the user. Input voltage frequency range is 47 to 450 Hz, suiting the units both to civilian uses, domestic and foreign, and to some military applications. Again, there is no output derating over the range.

Each of the 4027 switchers delivers 30 W from a 4.25-by-7.25-in. printed-circuit board. "We figure this product line is a good 10% lower in price than the competition," says Power General president John C. Gallagher. "Also, at 1.75 in. high, the models are more than an inch lower, and at 1.2 lb they are about 1.5 lb lighter." The 30-W 4027 series units are about the same size as some competing 50-W models, but somewhat larger and heavier than some 27-W competitors.

Regulation is 0.2% under load at the main 4.5 to 5.5 V at 4 A and 0.5% for five auxiliary outputs of +12 V at 0.4 A; −12 V at 0.4 A; −9 V at 0.4 A; −5 V at 0.3 A; and an adjustable output of −2.5 to −0.2 V at 0.1 to 0.4 A. The dc output is said to be spike-free and to have 50-mV maximum peak-to-peak ripple—10 mV root-mean-square. Each output is equipped with a low-pass filter for shunting unwanted high-frequency energy to ground.

Gallagher feels that his firm's switchers may find their niche in point-of-sale terminals, portable processors, and other systems where weight, efficiency, volume, and tight regulation are important. He says he already is receiving inquiries from a variety of terminal firms and microcomputer manufacturers.

Power General's engineering vice president George C. Chryssis notes a feature of the switches that is rare and may be unique: output overvoltage protection that, instead of a crowbar, uses a proprietary voltage sensor to close down all output taps in the event of overload. Some competing switchers apply a crowbar to only the main output, an arrangement that sometimes fails to prevent damage to system components.



In addition, a TTL-level input allows a microprocessor to turn a 4027 off for those applications in which a supply may seldom be needed, inhibiting it to save power. Alternatively, this feature allows systems using several supplies to turn them on in sequence to avoid sudden drains on the ac line.

Line isolation. Because the ac line does not always behave well, the unit's wide input voltage range protects it against brownout and input overvoltage. Also, in the event of loss of ac-line voltage, a voltage hold-up time is available of more than 32 ms, or roughly a couple of cycles at 60 Hz.

A radio-frequency-interference filter at the units' input is designed to make the unit conform to recently revised Federal Communications Commission regulations covering interference on the ac line. The filter prevents its own 20,000-Hz switching frequency from escaping onto the line, and offers up to 60 dB of attenuation at frequencies from 450 kHz to 30 MHz.

Finally, to protect itself, each 4027 includes a 10-A in-rush limiter, in the form of an easily replaced cartridge fuse, and features a soft start, to prevent both the turn-on transients that might damage downstream circuitry and the transformer saturation that can blow out components on the supply board.

The five models in the 4027 series all have the basic 4.5-to-5.5-V, 4-A output. The 4027-1 offers only the primary voltage and costs $75 in single units. The 4027-2 also offers ±12 V and is priced at $96.

The 4027-3, -4, and -5 have taps for +12 V at 400 mA, plus a mix of outputs of −12 and −9 V at 400 mA and −5 V at 300 mA. All three units offer a variable −2.5-to-−12-V output able to supply up to 400 mA. These units sell for $99 each.

The 4027s are available at slight variations in price in printed-circuit form, open-frame construction, or enclosed. Delivery of small lots is from stock.

The Power General Corp., 152 Well Drive, Canton, Mass. 02021 [381]

Switching dc-dc converter features 2 : 1 input range

The UM and UMC series of regulated switching dc-dc converters has a 2:1 input range, going from 9 to 18, 18 to 36, and 35 to 70 V dc. These three units can withstand surges of 25, 40, and 100 V, respectively, for as long as 8 ms before shutting down. They offer input filtering to hold the reflected ripple to 40 mA peak to peak. The series features single outputs of 5, 12, and 15 V dc at 800 mA to 3 A. The UM versions are designed to be mounted on printed-circuit boards; the UMC models are for chassis mounting. With up to 80% efficiency, the series has input/output isolation of 1,500 V dc and operates at full power to 71°C with no derating. Prices begin at $99.95 with discounts for original-equipment manufacturers. Delivery takes six weeks.

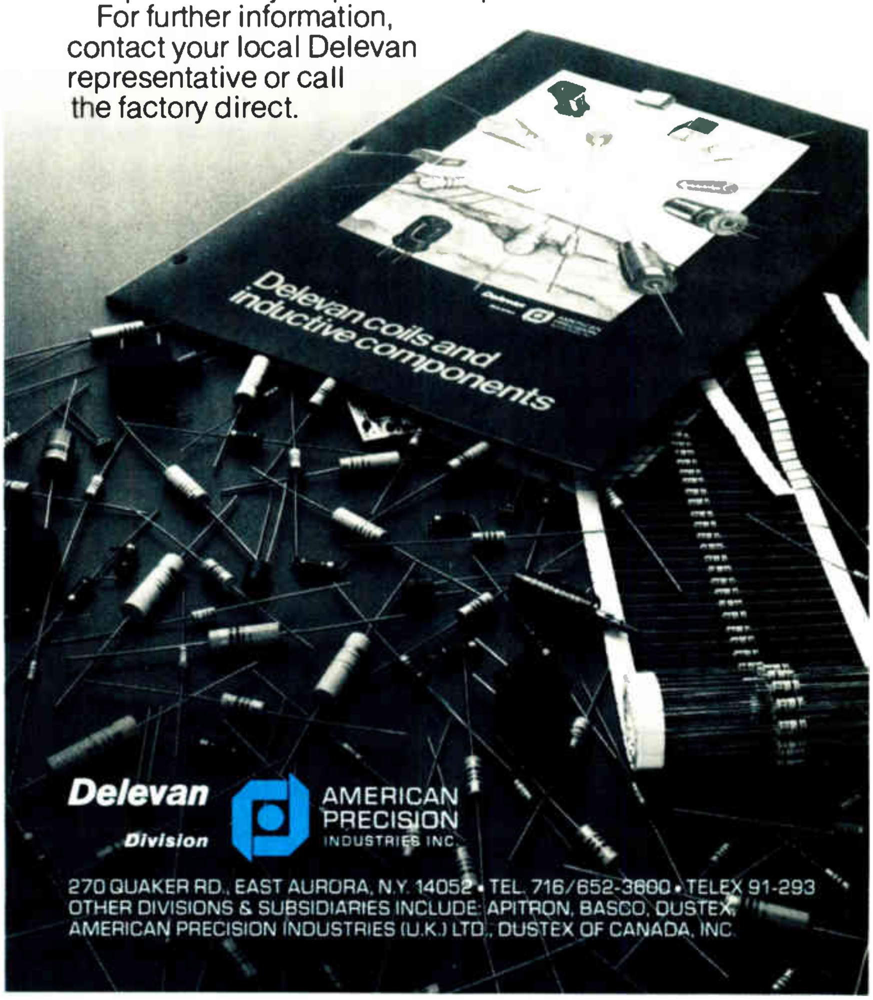
Semiconductor Circuits Inc., 218 River St., Haverhill, Mass. 01830 [384]

0-to-50-kV supplies can be programmed by computer

With dc outputs up to 50 kV, the series 205A and 210 solid-state power supplies for laboratory use have an option that allows the output voltage level to be programmed by a digital computer. Remote programming of the high-voltage output can be done with either a four-decade binary-coded decimal or a 16-bit binary TTL-compatible input. Models come with output ranges as low as 0 to 1 kV and as high as to 0 to 50 kV. The series 205A provides up to 30 W of power; the 210 provides up to 225 W at high voltage. Regulation and ripple are within 0.001%, and the temperature coefficient is 50 ppm/°C.

Single-unit prices start at $595, and the supplies are available from stock.

Bertan Associates Inc., 3 Aerial Way, Syosset, N.Y. 11791. Phone (516) 433-3110 [386]



New products/materials

Phenolic thermosets have the high strength and high heat resistance of asbestos-reinforced engineered thermosets and thermoplastics used in automotive and electrical applications, but are asbestos-free. The glass-fiber–reinforced material possesses the high-performance mechanical, electrical, and thermal properties normally found in asbestos-reinforced compounds, says the manufacturer. There are six versions of the material: RX 862, RX 865, RX 866D (glass fiber); RX 867, RX 867D, RX 867A (glass and cellulose fiber).

According to the company, the RX 800 series exhibits good processing characteristics in screw injection, transfer, or compression molding, and shows excellent creep resistance under load at high temperatures. Depending on the type, the thermosets feature: a tensile strength from 6,000 to 7,500 lb/in.^{2}, an Izod impact strength from 0.6 to 1.3 ft-lb/in., flexural strength from 11,500 to 15,000 lb/in.^{2}, and dielectric strength from 180 to 300 V/m depending on conditions. The materials sell for between 93¢ and $1.30 per lb.

Rogers Corp., Molding Materials Division, P. O. Box 550, Mill & Oakland Streets, Manchester, Conn. 06040 [475]

A resin system called PR-2042, a 100% solid epoxy-casting resin for potting and encapsulation applications, displays a linear shrinkage of 0.006 in./in., thermal conductivity of 3.0 BTU/hr/ft^2/°F/in., compressive strength of 16,000 lb/in.^{2}, and a tensile strength of 7,000 lb/in.^{2} The viscosity of the material is 6,000 centipoises at 25°C. The rigid material is intended for the impregnation of coils, chokes, resistors, solenoids, transformers, rectifiers, and electronic assemblies. A choice of three catalysts is provided. PR-2042 can be cured for 12 to 16 hours at room temperature. The pot life of the material for a 100-gram mass is 30 minutes at 25°C. Prices of the resin vary from $6.05 to $1.26 depending on catalyst and on quantity ordered.

Formulated Resins Inc., P. O. Box 508, Greenville, R. I. 02828 [476]

Products newsletter

Mostek expands family of 8-bit microcomputers

In some of the seven additions to its MK3870 family of 8-bit single-chip microcomputers Mostek Corp., Carrollton, Texas, is **offering 1 and 3 kilobytes of read-only memory** to fill the gaps left by existing 2- and 4-kilobyte 3870 family products. The 1- and 3-kilobyte ROM versions will sell in volume for about 16% and 20% less, respectively, than comparable 2- and 4-kilobyte ROM versions. In 100,000-unit quantities, a 3870 with 2 kilobytes of ROM currently sells for about $6 each; an MK3872, which contains 64 bytes of executive random-access memory in addition to 4 kilobytes of ROM, sells for about $12. Mostek will begin taking orders in late August.

AMI unveils n-MOS microcomputers, development system

American Microsystems Inc. of Santa Clara, Calif., is about to take the wrappings off its new S2200 family of single-chip microcomputers. The seven new n-channel MOS devices have on-board read-only memory ranging from 512 to 2,048 bytes. Three members of the family also have 8-bit analog-to-digital or d-a conversion capability. At Wescon '80 in Anaheim, Calif., AMI will also unveil **its new Phoenix-1, a low-cost (under $5,500) microprocessor development station** that will support the S2200, as well as Motorola's 6800 and Texas Instruments' 990 microprocessors, among others.

Harris 8-K PROM accesses in 50 ns

The latest model in a line of field-programmable read-only memories from Harris Corp.'s Semiconductor Products division is a **bipolar 8-K PROM with a 50-ns maximum access time.** The HM-7681A also has a 1,024-by-8-bit organization and three-state outputs. Housed in a 24-pin Cerdip package, it costs $35.75 in lots of 100. Production deliveries from the Melbourne, Fla., firm take eight weeks.

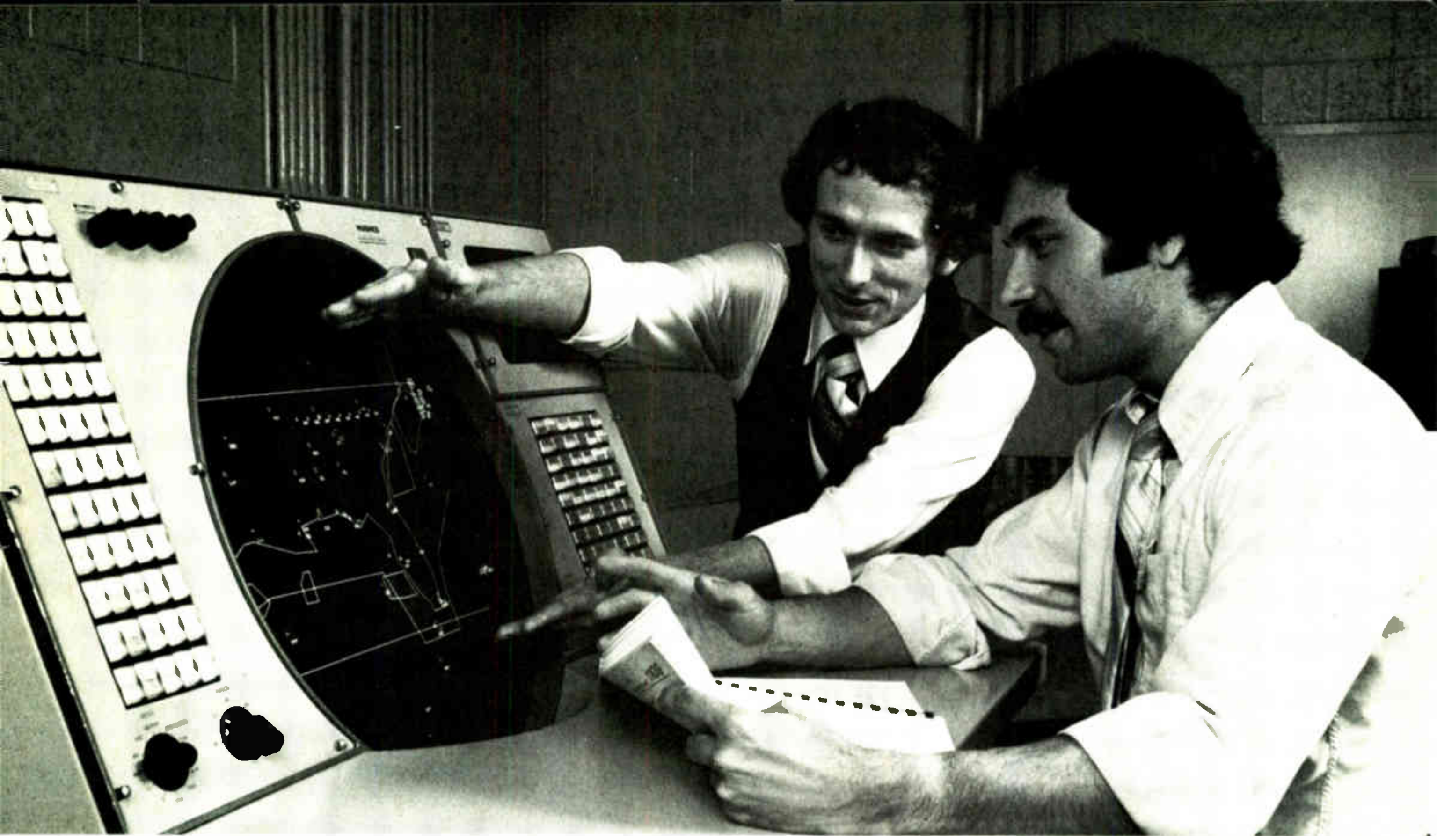
Software customizes I/O boards for data acquisition

ADAC Corp., Woburn, Mass., has designed a software package to **drive its analog and digital input/output boards that fit Digital Equipment Corp.'s LSI-11, -11/2, and -11/3 computers.** The software, called Adlib, runs under DEC's RT-11 operating system and consists of a library of subroutines that allow users to customize real-time data acquisition in Fortran or Basic. Included are routines for sequential or random-access channel selection, programmable gain or external triggering, and real-time clock functions. The package, which sells for $300, comprises a user manual and a floppy diskette containing source codes, object codes, and other library file information. Delivery is from stock.

Low-profile unit prints 100 characters/s

The DIP-81 dot-matrix impact printer from DIP Inc., Boston, has a 100-character/second bidirectional printout and costs $399 in quantities of 100 or $499 per single unit. **The 17-by-9.75-by-3.5-in. printer uses 7-by-7 or 14-by-7 matrixes,** has a full 96-character ASCII set, and prints lines of 40 or 80 upper- and lower-case characters. A Centronics-compatible parallel interface is standard; serial RS-232-C or 20-mA current-loop interfaces are optional. Delivery takes two weeks.

Classified section FOR ENGINEERING/TECHNICAL EMPLOYMENT OPPORTUNITIES



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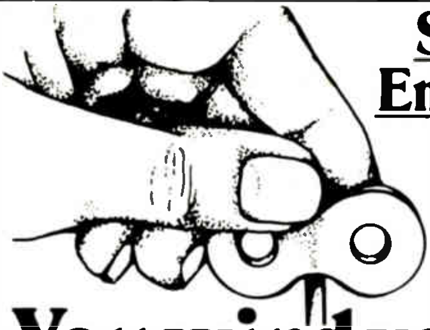

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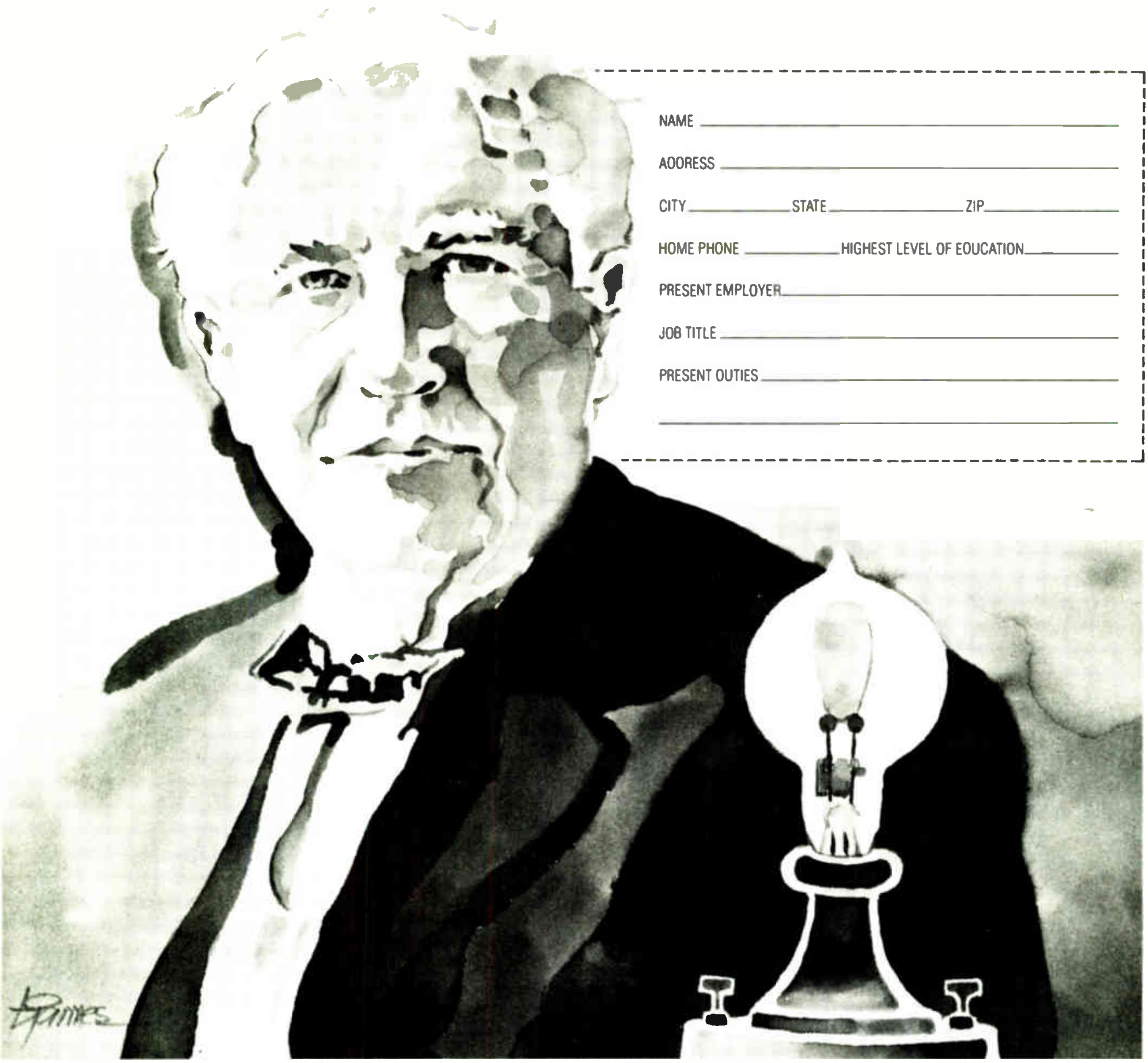

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Systems Engineer—Interface graphics terminals to SEL 32/35 computer; write I/O handlers. Provide maintenance for interactive graphics software. Development of mathematical models in their simulation, including models of 6 DOF rigid body kinematics. Operate and serve as Systems Coordinator for SEL system. Requires knowledge SELRTM operating system and job control language. Position requires MSEE, at least 1 year systems programming experience and knowledge of Fortran assembly and microprogramming. Salary is $19,000 per year, 40 hours per week. Send resumes to: Denise Deffe, Rothe Development, Inc., P.O. Box 53038, Houston, TX 77058. 713-488-7529. Equal Opportunity Employer.

The Department of Electrical Engineering of Gonzaga University invites applications for a tenure track position at the Assistant Professor level. Desired areas of expertise are: electromagnetic fields, communications and solid state electronics. A Ph.D. and some practical experience are desirable. Send resume to: W.P. Ilgen, Dean, School of Engineering, Gonzaga University, Spokane, WA 99258. An equal opportunity/affirmative action employer.

Control Engineer/Pilot—M.S. in E.E. or Aero E. needed for helicopter cockpit design and control. Position requires cockpit experience in helicopter and strong background in graduate level optimal control theory, man-machine interaction and hand-eye coordination problems. Salary range $22 to 28 K. Send resume to: SDI, P.O. Box 13687, Gainesville, FL 32604. (Location—1219 N.W. 10th Avenue, Gainesville).

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Electronic engineering growth posi-tions with clients located nationally. Our service is enhanced by the fact that I am an EE with 20 years in industry and over 10 years in placing professionals on an employer fee paid basis. Send your resume to Joe Torcassi, Director, J. Anthony & Associates, PO Drawer AD, Lynchburg, OH 45142. 513/364-2305.

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Faculty Positions in Electrical Engineering Technology Undergraduate teaching positions in electrical engineering technology available on August 16, 1980 in Tuscaloosa, Alabama at The University of Alabama. Teaching duties will be in the area of circuits and electronics and one or more of the following areas: power, controls, communications, digital electronics. Master's degree or equivalent and at least one degree in EE or EET desirable. Some recent relevant industrial experience required. Some teaching experience desirable. P.E. registration desirable. Although positions are tenure track, applications are desired from those wishing a temporary appointment for all or part of the 1980-81 academic year. Applicants should send a complete resume to: Dr. John D. Antrim, Director, Engineering Technology Programs, The University of Alabama, P.O. Box 1941, University, AL 35486. An EO/AA employer.

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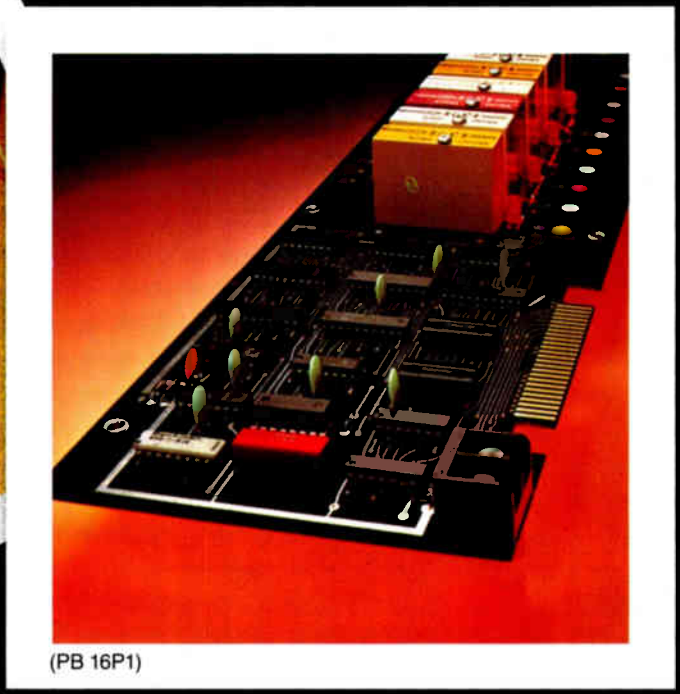

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