JANUARY 17, 1980

ASSEMBLY LANGUAGE PLAN STIRS CONTROVERSY/98

Four-chip hybrid carrier — the optimum IC package?/113

Bit-mapping techniques populate boards with partial RAMs/131

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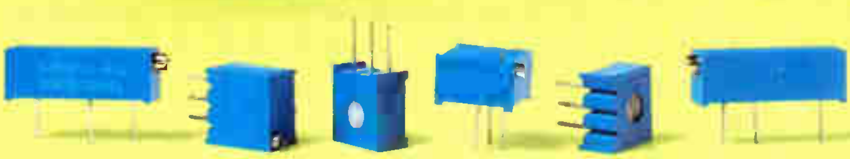

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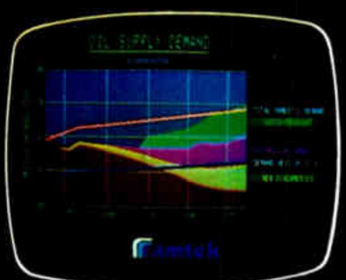

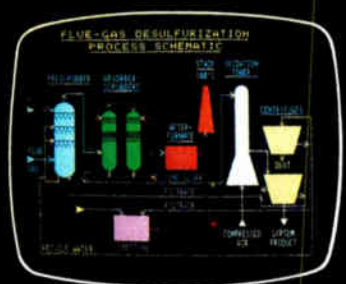

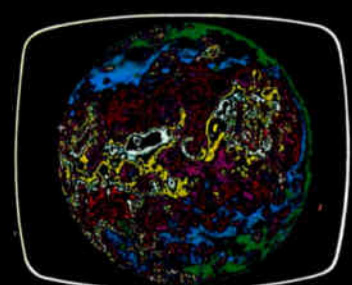

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Electronics

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Highlights

Cover: The level in the R&D well is dropping, 81

An in-depth analysis (more like it are on the way) takes a hard look at research and development in the U. S. Despite the fact that U. S. companies are spending more dollars on R&D each year, expenditures are falling behind inflation. As a percentage of sales, R&D outlays are only constant, and as a percentage of profits they are declining. As a result, the U. S. is falling behind in the race for new ideas and the Government is taking a lot of flak for policies that impede capital formation.

Cover photograph is by Don Carroll.

Four-chip SSI hybrids mix well with LSI, 113

A cost analysis of possible package-mix options finds dual in-line packages wanting. Chip-carriers with leads on 50-mil centers reduce board costs, as does mounting in them the 10% of a hypothetical central processor not yet in large-scale integration. Carriers with four small-scale integrated circuits on a one-layer hybrid substrate offer future cost reduction as they are replaced by single-chip gate arrays—without redesigning the boards.

Easing communication between man and microprocessor, 118

SMAL/80 is a compiled assembly language for small machines. Microprocessors can ill afford the extra storage and slowed execution required by structured high-level languages, but SMAL/80 is memory-efficient even as it offers structured, top-down, modular programming. And its symbolic notation is easier for humans to deal with than that of other assembly languages.

Partials fill in for scarce RAMs, 131

A new generation of random-access memories would suffer an unbearable infant mortality rate were it not possible to work around a few defects. With RAM in short supply, schemes for reliable storage using mostly good chips cannot be ignored.

Multiple keys fit encryption chip set, 136

The design of a two-chip data-encryption set provides for boosting data security with double and triple keys without major hardware or software additions. The fastest version of the chip set executes the National Bureau of Standards' algorithm at a rate of 11,500 bits per second.

. . . and in the next issue

Speech synthesis with an analog microprocessor . . . the effect of a contact temperature probe's design on its accuracy . . . a custom LSI integrated-injection-logic chip set for computer-peripheral control . . . a microprocessor with a memory socket on top for microcomputer system design . . . a microprocessor development system ready for chips unborn.

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Publisher's letter

Research and development spending at times seems much like the weather—everybody talks about it, but nobody does anything about it. There has certainly been a lot of talk about support of R&D as the United States has seen its assumed technological leadership challenged over the last decade and felt the impact of these challenges in the form of tougher competition for both domestic and foreign markets.

But something is in fact being done about R&D, though many wonder if it is enough. The article on this subject (p. 81) is the first of a new type of story we will be presenting called Inside the News. Research and development, we think, is a good kickoff topic.

It's a subject close to the heart of Boston bureau manager Jim Brinton, who put together this report with the support of our domestic and overseas bureaus. "There is genuine concern in America on the part of industry, academia, and Government," Jim remarks. "Yet it seems that the three groups need a means of getting together and converting their concerns into goals. It's not just a matter of funding—although that is an important consideration. It's a matter of balancing long-range, pure research against short-range product development. Many worry that the pressure to get hardware obscures the need for basic research."

Meanwhile, the governments of Japan and Western Europe have long taken a partnership view of supporting technology as part of their national welfare. Without enormous defense budgets to fund, these countries have been able to focus on long-range commercial development.

"This story is kind of a snapshot of how high-technology companies view R&D," says Jim. "But the message is clear that its costs are rising, that product life cycles are shorter, and that other countries are breathing down our necks. It seems we have to run faster just to stay in place."

Another new feature in this issue is In My Opinion, on page 26. This commentary from various industry sources will appear from time to time when we feel it will be valuable to air outside opinions on hot topics.

The first subject—transfer of technology to the Soviet Union—could not be hotter these days in the light of the recent tensions between the U.S. and the USSR. Our guest commentator is J. Fred Bucy, president and chief operating officer of Texas Instruments, Dallas.

Bucy has strong opinions on the possibility of establishing a "militarily critical technology" system to guide companies and countries in the Coordinating Committee of the Consultive Group of Nations (the U.S., Western Europe, and Japan). Essentially, TI's president argues that it is possible to encourage trade and at the same time protect technology that might aid the military effort of hostile nations.

We will be identifying other issues and inviting other guest observers in the coming months.

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Readers' comments

Faulty table

To the Editor: In your issue of Oct. 11, 1979, a table appeared on page 113 containing comparisons of several technologies for the realization of electrically erasable programmable read-only memories (EE-PROMs). In the part about the SGS-ATES nonvolatile random-access memory we have noted several errors. First, it is realized using MOS, not C-MOS, technology. Secondly, there are only two transistors per cell, not six—of obvious importance where very large-scale integration is concerned. Third, the memory does not work on the principle of transferring data from a RAM to a ROM, as is implied by labeling the device's two supplies as "RAM" and "RAM-to-backup" voltages. Also, the two voltages should be +12 and +25 V. Finally, regarding the electronic program memory circuit for television controllers, we have been in full-scale production of the M193, with 272 bits of nonvolatile memory, for over one year now.

Chris Wallace
SGS-ATES Componenti
Elettronici SpA
Milan, Italy

Spending on the sun

To the Editor: Your exhortations to the Government to further fund the solar electric industry are amusing. We have yet to reap any benefit from the money already pumped in. The retail cost of solar arrays still stands where it was five years ago, around $30 per watt, despite all the "goals" and claims which I've read in your articles.

If you disbelieve, consult your Edmund Scientific catalog.

I have a kilobuck ready to spend on some silicon, but I'm waiting for even the $10 watt to show on the market. Where is it?

T. J. Lally
St. Ann, Mo.

Correction

On page 126 of Electronics, *Jan. 3, 1980, the price of a reprint of the three 1980 market reports was misquoted at $4. The correct price is $3.*

"THE 8086 IS HERE TODAY!"

Well, Intel's still out there shouting about the 8086. Still making lots of claims, still running pages and pages of advertising, still forgetting to mention one little fact:

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"So is the AmZ8000. And it's better."

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To demonstrate the capability of the AmZ8000 we developed a fully assembled and tested Evaluation Board. It's got the AmZ8002 CPU on it, along with RAM, EPROM, and I/O. It plugs right into System 8/8 and can execute the assembler or PASCAL object code. Ask for it by name: AMC96/4016.

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Better yet, buy an AmZ8000. Check it out for yourself. Put it through its paces. Compare it with the 8086.

Intel can beat their chests all they want. But they can't beat the AmZ8000.

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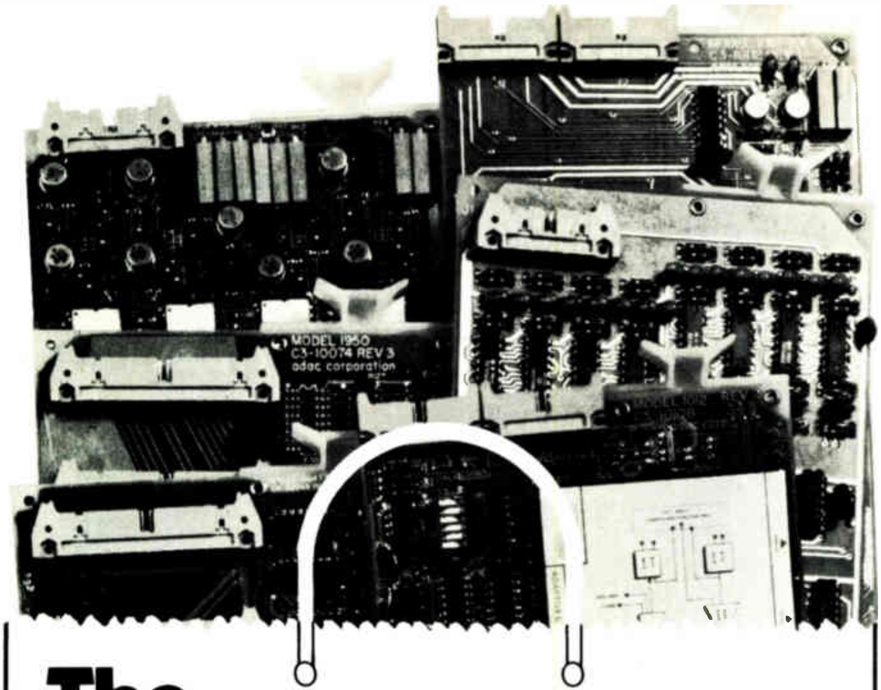


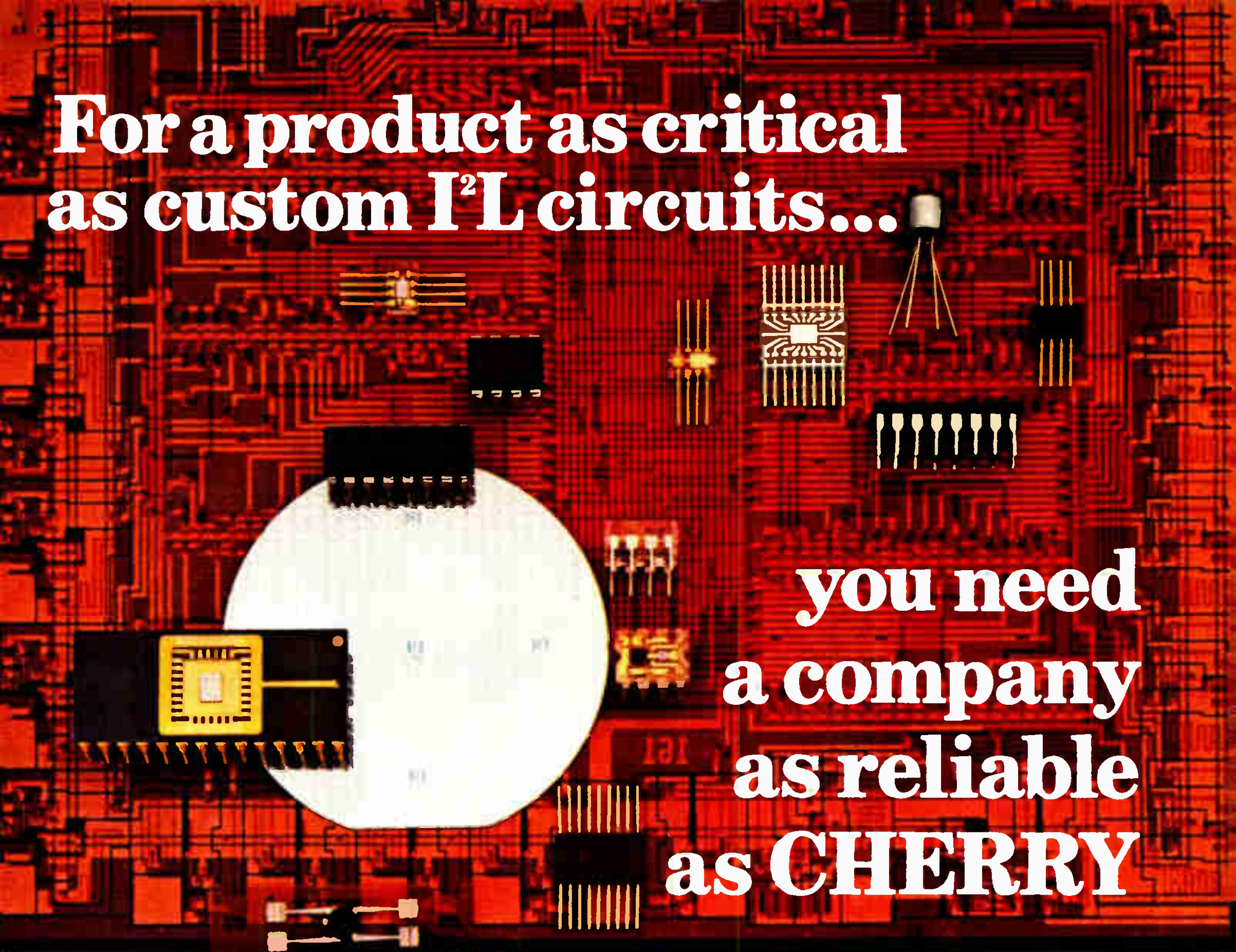
News update

■ The 64-bit peripheral array processor unveiled last June by Computer Signal Processors Inc. [*Electronics*, June 7, 1979, p. 161] is making its debut in the lab and in systems—but slowly. The Burlington, Mass., firm has shipped one MAP-6400 to the University of Arizona's mechanical engineering department for structural analysis applications. Two more, shipped to Systems Inc. (formerly Systems Engineering Laboratories Inc.) in Florida under an original-equipment-manufacturer agreement announced last year, are going into that company's new mini vector processor.

No other firm orders are yet on CSPI's books, but the inquiries received so far from scientific engineering people are encouraging CSPI to gear its production for volume deliveries of the MAP-6400 by the second quarter, says John H. Meyn, product line manager for the machine. CSPI is also offering a package of matrix functions for the processor "to satisfy all but the most esoteric use," Meyn adds.

Other software offerings are in the works as well. "This is a new area for us," says Meyn, "but we're learning from the kinds of inquiries we've been getting what kinds of packages users want." CSPI, accordingly, is looking actively "to cultivate some close relationships with software people to adapt specialized array-function software routines."

■ Direct-step-on-wafer lithographic equipment retrofitted to yield circuit line widths less than 1 micrometer [*Electronics*, Nov. 22, 1979, p. 46] have produced consistent, good-quality lines between 0.425 and 0.65 μm for interdigital transducers on surface-acoustic-wave delay lines. According to Andrew J. Slobodnik Jr., engineer at Rome Air Development Center, the 1.25-microsecond delay line is the highest-frequency operating SAW device yet fabricated optically, having a center frequency of 2.2 gigahertz. The device's transducers consist of 10 pairs of single electrodes with 100-μm acoustic aperture. **-Linda Lowe**



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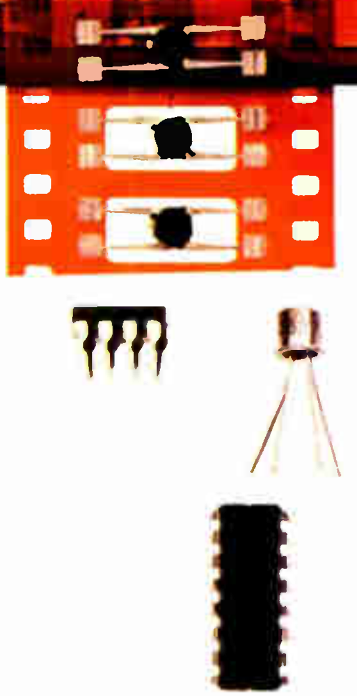

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People

Nonken putting software on level equal with hardware

In the minicomputer business, the trend now is to develop operating software in house. Smaller firms particularly are fast moving away from just "selling iron" in order to get value-added financial benefits, keep better total product control, and (they hope) make customers happier. For example, in Irvine, Calif., Microdata Corp. recently created a new post putting software on an equal footing with traditional engineering and moved an industry veteran into it.

Actually, the software moves are "a lot of trends that fit a pattern," observes Howard R. Nonken, Microdata's new vice president for systems and software engineering. The obvious one: "Mini makers are now writing their own operating software as the mainframers do," instead of letting customers hire third-party systems houses to do it. Nonken comes out of big computers, having spent 22 years at Burroughs Corp. "doing every engineering job there," before joining Microdata in 1978 as a project manager.

But more challenging tasks still remain. "The next step is recognizing what an operating system does and what is better done with firmware," he says. What Nonken calls a "migrating trend" is shifting software programming into firmware, largely dedicated semiconductor memory. Microdata has started—Nonken says one example is process scheduling, or firmware that sets priorities on machine routines, judgments that previously a programmer had to make.

However, Nonken still believes in the sharp distinction between operating system software and programs for specific customer applications and thinks companies must continue to handle these separately. "The systems side is engineering and design, while applications should be part of marketing support." Otherwise, coordination troubles result: he says there are numerous horror stories about software written in

New approach. Microdata's Nonken expects firmware to get stronger in minis.

isolation that ends up useless.

Finally, Nonken looks for an even broader trend to gain speed—by moving away from general-purpose architecture and toward special-purpose computers. However, this is not an opinion that yet finds wide support among mini makers, he admits. "The goal is to make programming easier for the customer; it's terribly expensive now."

As if the pitfalls of marrying software internally to hardware were not enough, the personnel problem, or lack of enough good programmers and engineers, also lurks in the wings. Nonken says Microdata is forced to use consultants to help with software development, despite its preference for hiring them outright.

Simpson switches his terminal from IBM to Amdahl

Nearly a decade after hardware innovator and IBM Fellow Gene Amdahl went off to form Amdahl Corp., he has been joined by an expert of equal stature on the software side. Thomas H. Simpson, also an IBM Fellow, has joined the Sunnyvale, Calif., firm as its technical director. Simpson, a native Texan with a John Wayne–sized frame, is best known for his work in developing the Houston automatic spooling priority (HASP) operating system for the IBM System/360 and

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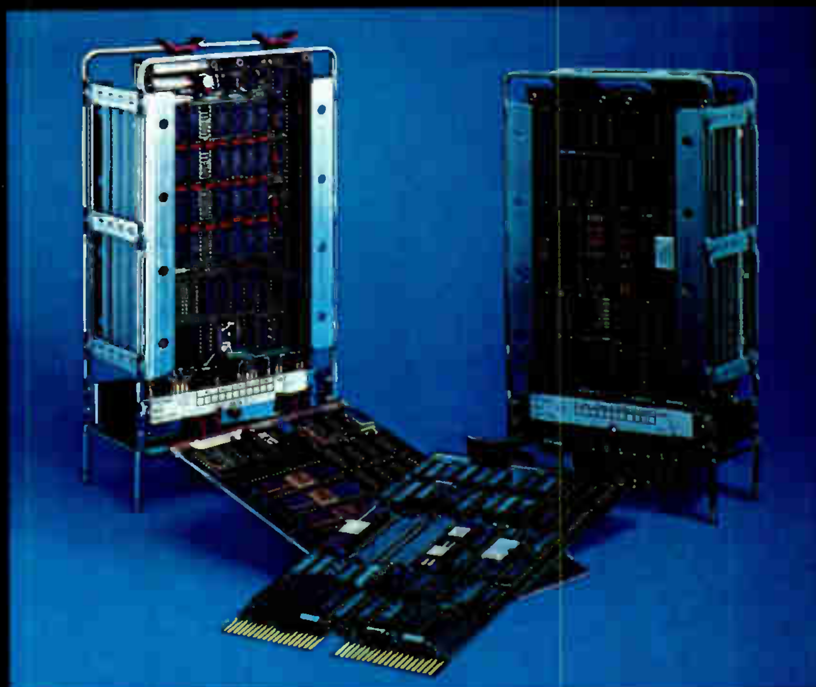

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™Trademark First Computer Corporation ®Registered trademark of Digital Equipment Corporation the JES-2 remote job entry system for IBM's current multiple virtual systems (MVS) operating system.

His move was not prompted by a preference for California scenery, for Simpson will communicate with Amdahl through a terminal at his home in Dallas—just as he did with IBM. Rather, he attributes the change to his attraction to Amdahl as "a company quick to respond to changes and to take on new ideas."

Simpson offers these observations of changes to look for in the 1980: "First of all, you can look for Amdahl to place much more emphasis on software development than it has in the past. You may also see the disappearance of user modifications to the operating software. The reason for this is that hardware has become much cheaper while the labor involved in software is becoming much more expensive. Thus, it simply isn't worth it for the user to change his operating software to squeeze out another 12% or so in performance and in the process lose his software support."

Virtual memory fades. Following the logic that hardware is cheap and that programmers are expensive, Simpson calls the No. 1 priority for the 1980s the simplification of IBM's MVS operating software. In fact, Simpson sees the importance of the virtual memory system itself—the darling of the 1970s—declining in this decade. "The virtual memory will not become obsolete," he cautions, "but it will become less important."

The simplification of the MVS program may also improve the reliability of large computers. "We have finally reached the point where hardware is more reliable than software," Simpson notes. In fact, he would like to see more of the functions of the on-site support engineer replaced by remote diagnostics and by increased monitoring maintained by independent circuitry. "With microcomputers coming along the way they are," he asserts, "we should be able to sprinkle a handful of service processors here and there throughout the mainframe at essentially no increase in overall cost." ☐

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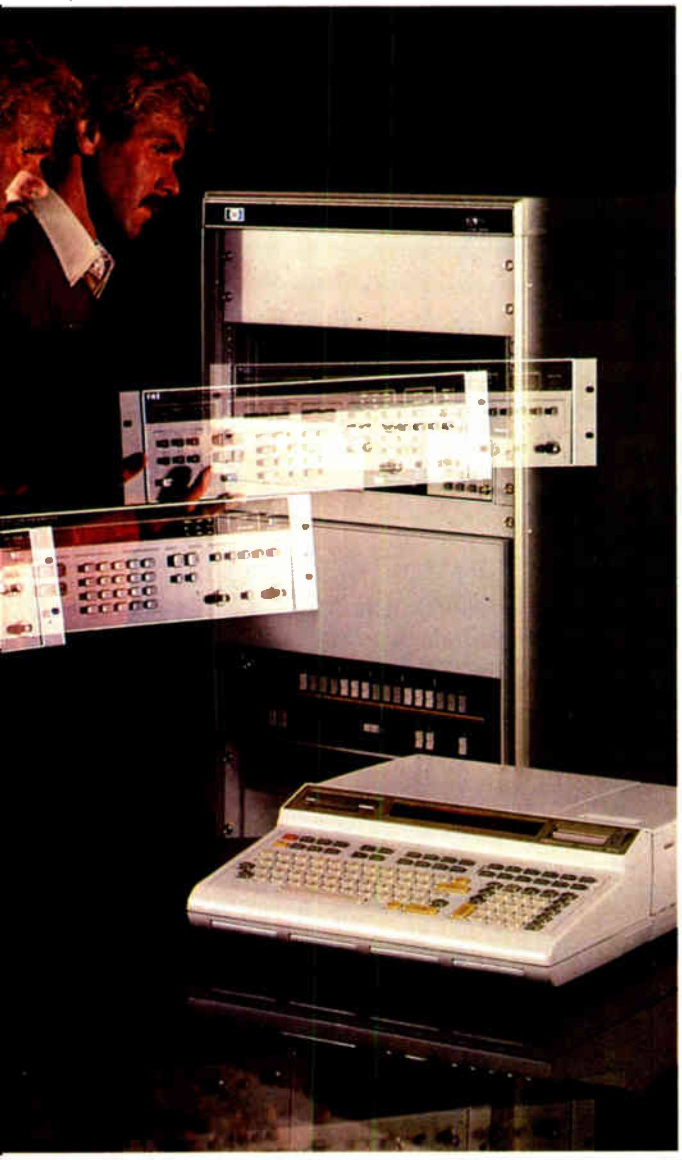

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60		2147 (55-85ns)	2148H* (45-55ns)
80			2148 (55-85ns)
100			
200		2141 (120-250ns)	2114A (120-250ns)
300			

*Available Q1, 1980

For highest speed and low power, no bipolar can touch our HMOS II 2115H/25H 1K static RAMs. One version gives you record access times of 20ns; three others let you choose speed/power combinations to 35ns. For designs requiring speeds from 45-70ns, our 16-pin industry standard HMOS 2115A/25A series covers the spectrum. All of these 1Ks are pin-compatible replacements for 93415/25 bipolars, and all give you dramatically lower power, too.

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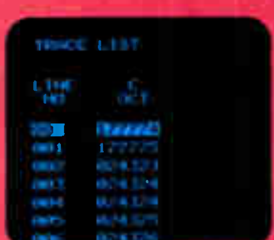
Our menu concept with simple keyboard entries and plug-in interfacing reduces set-up time to a minimum. Add the advantages of better insight and faster debugging and, chances are, you'll make the transition from hardware assemblies to operating systems more rapidly.

With simple matrix programming, the 1640A Serial Data Analyzer ($5,800*) monitors RS-232C interfaces, measures time intervals and simulates network components. It's flexible triggering lets you trap on data errors, time-interval violations or invalid protocol sequences. For subtle problems, or loop-back tests, it simulates a CPU, terminal or modem. And you can operate with any combination of standard transmission modes.

Now you can capture state, timing and glitch information simultaneously with the 1615A Logic Analyzer ($6,800*). It acts as a 24-bit state analyzer or an 8-bit timing analyzer. You can also combine the two modes to trigger on timing while viewing program flow. And vice versa—at your choice of specific points in address flow.



Save both debugging and development time by relating parallel data transactions to handshake protocols; verifying time sequences; detecting and triggering on glitches; and evaluating system performance at the time of a glitch.

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R&D is developing a case of malnutrition

Along with agriculture, the technology-intensive industries show the only sizable positive international trade balances the U. S. has to its name. But, as the article beginning on page 81 points out, the nation has been slowly starving technology for years.

In real terms, the country as a whole is spending less on R&D now than in 1969; Government alone is spending 17.7% less.

R&D funds also have more differing calls upon them now than they did a decade ago:

- A greater proportion of R&D money is aimed at compliance with Government regulations.
- More is going to pay for the ever-growing paperwork required in any Government-funded project.
- Because good people are scarce, salaries of research workers are rising faster than those of other employees, and R&D-intensive firms often find themselves bidding against each other for gypsy scientists and engineers, taking another chunk of the R&D dollar.

Simultaneously, inflation is robbing U. S. currency of its buying power while increasing the cost of capital equipment necessary for R&D. And productivity is in decline here while growing abroad.

The result of all these factors is that despite level or growing R&D investment in terms of today's dollars, the U. S. is not only investing less in real terms, but is spending it less efficiently than before.

The business climate for R&D is very unfavorable. According to the New York–based Committee for Economic Development, U. S. capital investment as a percentage of industrial output is lower than that for most other industrialized countries—its world trading competitors. And this comes at a time when much United States industrial plants are, or are becoming, obsolete.

At least partly because of the R&D funding slump, nations like Japan and West Germany are overtaking what has been a traditional U. S. technological lead. In some areas, like industrial robotics, they are already ahead, according to the Stanford Research Institute in Palo Alto, Calif.

Meanwhile, colleges and universities, the traditional strongholds of basic research, faced with the same economic plague afflicting industry, in addition to falling enrollments, plead for funds. Though R&D funding dropped as a whole, basic research took a steeper tumble. Now some institutions are wondering if they will be able to afford tomorrow's scientists and educators.

Thus, R&D in North America gives the appearance of running faster while simultaneously falling behind. Technology executives see a variety of reasons: a stifling governmental presence; a patent system which, as Thomas Edison said, is only an invitation to a lawsuit; the high cost of money, which forces managers to shoot for short-term returns on investment rather than roll the long-term dice of R&D.

It's a bleak situation. As Texas Instruments vice president George H. Heilmeier puts it, "This nation looks like it's trying to shoot itself in the foot."

There are many suggested cures, some of them in bills now before the Congress. Among those cures are patent policy revisions, tax-law changes, and realistic regulations. But this is an election year, which generally sees little legislative progress. Yet the decisions taken now will establish the international economic position of the nation in the 1980s and 1990s: its standard of living, its ability to deal with social problems, and its defense posture. In that light, surely Congress should do more of this spring's campaigning in the Capitol.

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Protecting 'militarily critical technology'

by J. Fred Bucy, ***president and chief operating officer, Texas Instruments Inc., Dallas***

When the promise of warmer U.S.-USSR relations of the early seventies was chilled by Soviet actions in Africa and the Middle East in the mid-seventies, the Congress and the Executive Branch began a reassessment of the role of export controls in this country. Like others in the private sector, I felt a need for a revamped, better-focused system to replace that developed in the fifties and modified in the late sixties but seemingly inadequate for meeting national security and international trade requirements of the seventies.

With the recent passage of another extension of the Export Administration Act and the reorganizations at the Office of Export Administration and the Department of Defense's research and engineering section, there is a feeling that the reassessment is over. But the task is not yet completed.

We must proceed to implement what is known as the militarily critical technologies approach to export controls. Not everyone agrees with this concept, however.

Conflicting views

Opposition to focusing export controls on militarily critical technologies may be summarized as follows:

- The way for the U.S. to maintain its technological advantage, where it exists, is to conduct more research and development.
- If the U.S. does not export this technology, someone else will because we do not have a corner on the world's brain power. In addition, the Coordinating Committee of the Consultative Group of Nations (CoCom), organized to monitor technology transfer to Iron Curtain Countries, is not working.
- The DOD has yet to define adequately militarily critical technologies three years after acknowledging the sound reason of the concept.

There is some validity in each of these statements. But they do not, in my opinion, lead to the conclusion that the critical technologies approach won't work. In fact, the realities associated with the three statements underscore the need to implement the critical technologies approach. Consider opposition to such implementation in the light of the following:

- In real dollars, we have had a declining military research and development budget over the past decade, even though one of the principles of U.S. defense posture is weapon superiority through advanced technology. During this period, the defense weapon cycle has lengthened. Militarily significant technologies, such as large-scale integration, may not be represented in operational weapon systems until 10 years or longer after their initial appearance in commercial applications.

The purpose of export controls must be kept in mind. They are meant to delay the acquisition and practice of militarily critical technologies by forces hostile to this country. The amount of delay necessary depends on the capability of the recipient to absorb it and, perhaps more importantly, the rate of R&D and technology implementation of the U.S. Faced with realities of declining R&D and stretched-out lead times, the case for controlling the rate of militarily significant technology transfer is overpowering.

- The U.S. must accept part of the responsibility for CoCom's inadequacies. We should limit controls only to the really critical technologies, and explain their direct linkages to weapon systems to other member nations. We should request fewer exceptions to CoCom guidelines. Commercial technologies of military significance are being diffused with greater rapidity among the most developed nations. Japan, Germany, France, and other CoCom members are developing technology and are interested in selling it. They often have a more liberal interpretation of controls and are confused by our own schizophrenic behavior regarding trade and controls.
- Technology-intensive firms already use concepts similar to the critical technologies approach to protect their competitive position, identifying their most sensitive technologies as trade secrets or proprietary data or applying for patents and copyrights. Over the past 20 years, several major sectors of electronics, particularly computers and semiconductors, have aggressively participated in world markets, gaining significant market share and contributing a positive margin to U.S. balance of trade. The leading firms in these sectors have accomplished both tasks—emphasizing the sale of products, while at the same time protecting their technology.

Electronics *will periodically invite the expression of outside views on this page on issues of importance to the electronics industries.*

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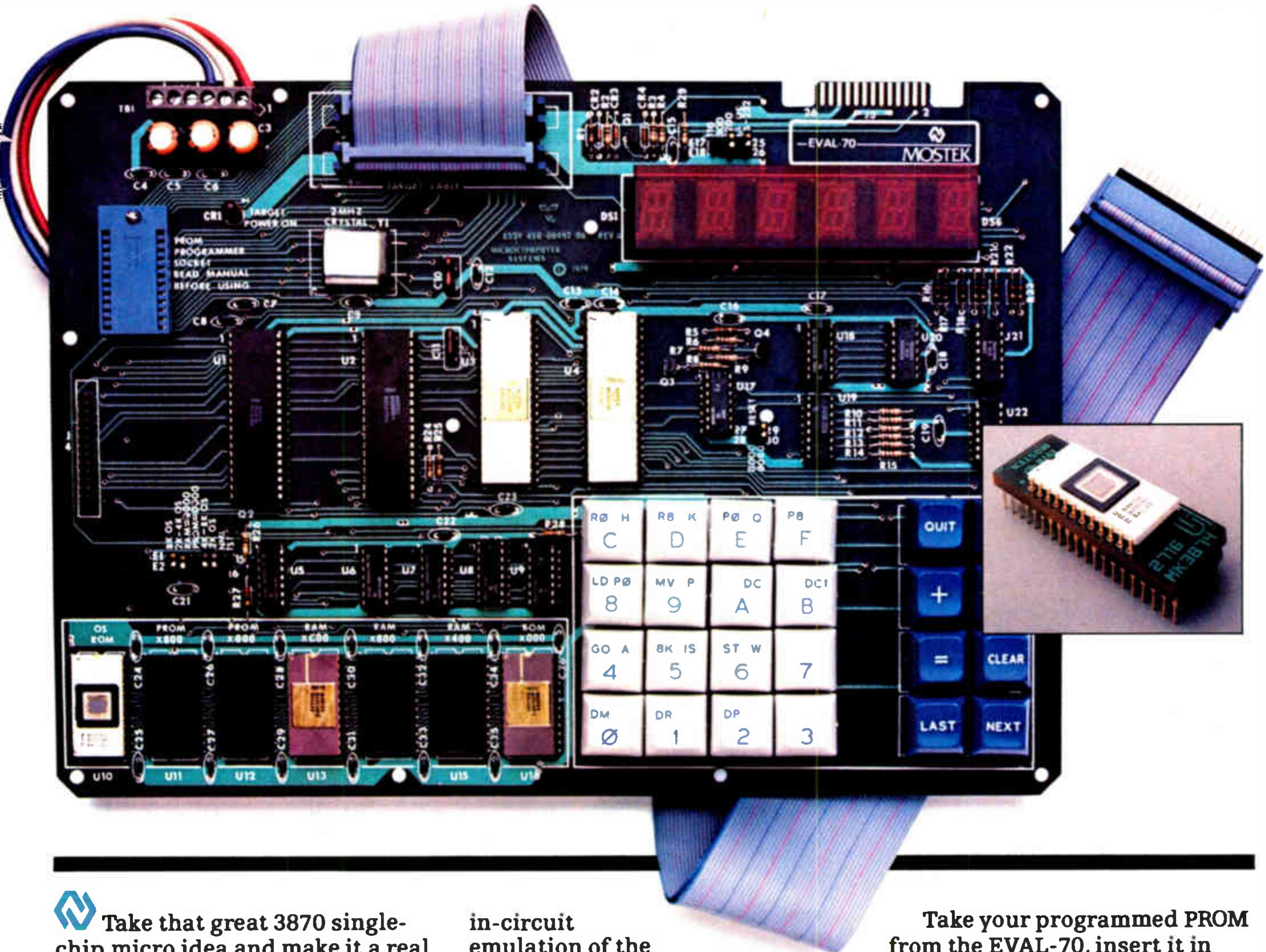

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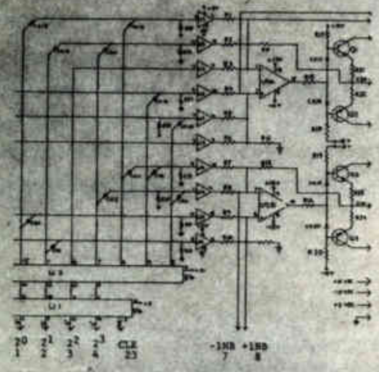

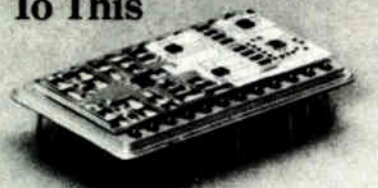

Meetings

Third Annual SEMI Information Services Seminar, Semiconductor Equipment and Materials Institute (625 Ellis St., Suite 212, Mountain View, Calif. 94043), Marriott Hotel, Newport Beach, Calif., Jan. 27–30.

Software Quality Assurance and Configuration Management Seminar, American Institute of Aeronautics and Astronautics (P. O. Box 91295, Los Angeles, Calif. 90009) *et al.*, Colonnade Hotel, Boston, Jan. 28–29, and International Inn, Washington, D. C., Feb. 21–22.

Status '80, The Changing Semiconductor Industry, Integrated Circuit Engineering Corp. (6710 E. Camelback Rd., Scottsdale, Ariz. 85251), Quality Inn, Arlington, Va., Jan. 29, and Hyatt Rickey, Palo Alto, Calif., Feb. 6.

Communication Networks '80, The Conference Co. (60 Austin St., Newton, Mass. 02160), Sheraton Washington, Washington, D. C., Jan. 28–30.

Fifth Topical Meeting, Integrated and Guided Wave Optics, Optic Society of America (200 L St. N. W., Washington, D. C. 20036) and IEEE, Hyatt–Lake Tahoe, Incline Village, Nev., Jan. 28–30.

The Automated Office, American Institute of Industrial Engineers, (P. O. Box 3727, Santa Monica, Calif. 90403), Statler Hilton Hotel, New York, Jan. 28–30, and Twin Bridges Marriott Hotel, Washington, D. C., Feb. 11–13.

11th International Symposium for Mini and Microcomputers, International Society for Mini and Microcomputers (P. O. Box 2481, Anaheim, Calif. 92804), Asilomar Conference Grounds, Pacific Grove, Calif., Jan. 30–Feb. 1.

Export Administration Act of 1979, Law & Business Inc. (Harcourt Brace Jovanovich, 757 Third Ave., New York, N. Y. 10017), Mark Hopkins Hotel, San Francisco, Jan. 31–Feb. 1.

Annual Television Conference, Society of Motion Picture and Television Engineers (862 Scarsdale Ave., Scarsdale, N. Y. 10583), Sheraton Centre Hotel, Toronto, Canada, Feb. 1–2.

Eighth Semiannual Conference on Federal ADP Procurement: New Departures, American Institute of Industrial Engineers (P. O. Box 3727, Santa Monica, Calif. 90403), Shoreham Americana Hotel, Washington, D. C., Feb. 4–6.

Los Angeles Technical Symposium, Society of Photo-Optical Engineers (P.O. Box 10, Bellingham, Wash. 98255), Sheraton-Universal Hotel, North Hollywood, Calif., Feb. 4–7.

Third International Business Computing, Word Processing and Information Management Exhibition and Conference (Info '80), BED Exhibitors Ltd. (Bridge House, Restmor Way, Wallington, Surrey SM6 7BZ, England), Cunard International Hotel, London, Feb. 12–15.

The IBM Evolving Network Strategy, The Yankee Group (Box 43, Cambridge, Mass. 02138), Hyatt Rickey, Palo Alto, Calif., Feb. 13–14, and the Harvard Club, New York, March 25–26.

ISSCC'80, International Solid State Circuits Conference, IEEE and the University of Pennsylvania, San Francisco Hilton Hotel, San Francisco, Feb. 13–15.

Southwestern Tool and Manufacturing Engineering Conference and Exposition, Society of Manufacturing Engineers (P. O. Box 930, Dearborn, Mich. 48128) and National Tool, Die and Precision Machining Association, Albert Thomas Convention Center, Houston, Texas, Feb. 19–21.

Alternate Energy Sources of the 1980s Conference, IEEE, Town and Country Hotel, San Diego, Calif., Feb. 20–22. (For information, write to George Seebeck, San Diego Gas & Electric Co., San Diego, Calif. 92101.)

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Saxon Business Products, Inc.: "Mostek's 3870 cost-effectively replaced a three-chip microprocessor set. As the controller in the Saxon 301, 302, and soon—the 301R—bond copying machines, the 3870 has improved the Saxon-line reliability with field uptime at all time highs." *Mike Bonavia, Electronic Engineer.*

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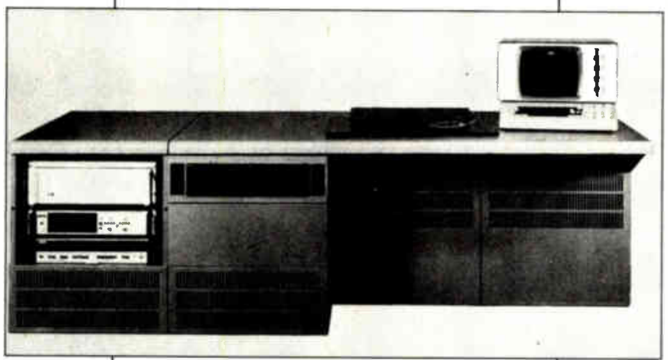
Series 70's high-level programming language helps the system adapt easily to all makes and models of instrumentation.

And with Series 70, you also get your choice of fixturing systems—universal, edge connector, or optional vacuum-operated bed-of-nails interface.

ALL THIS AND 5 MHz TOO.
Most popular board testers run at relatively slow data rates. Series 70 operates at 5 MHz across all digital pins in parallel and collects probe data at full test speed.



In addition to its super system speed, Series 70 offers faster, more accurate fault isolation. It features multiphase clocks, which let you program timing increments with 20ns resolution. And its new dynamic current measurement technique lets you track bus-related faults at full system speed.

SOFTWARE THAT SPEAKS YOUR LANGUAGE.
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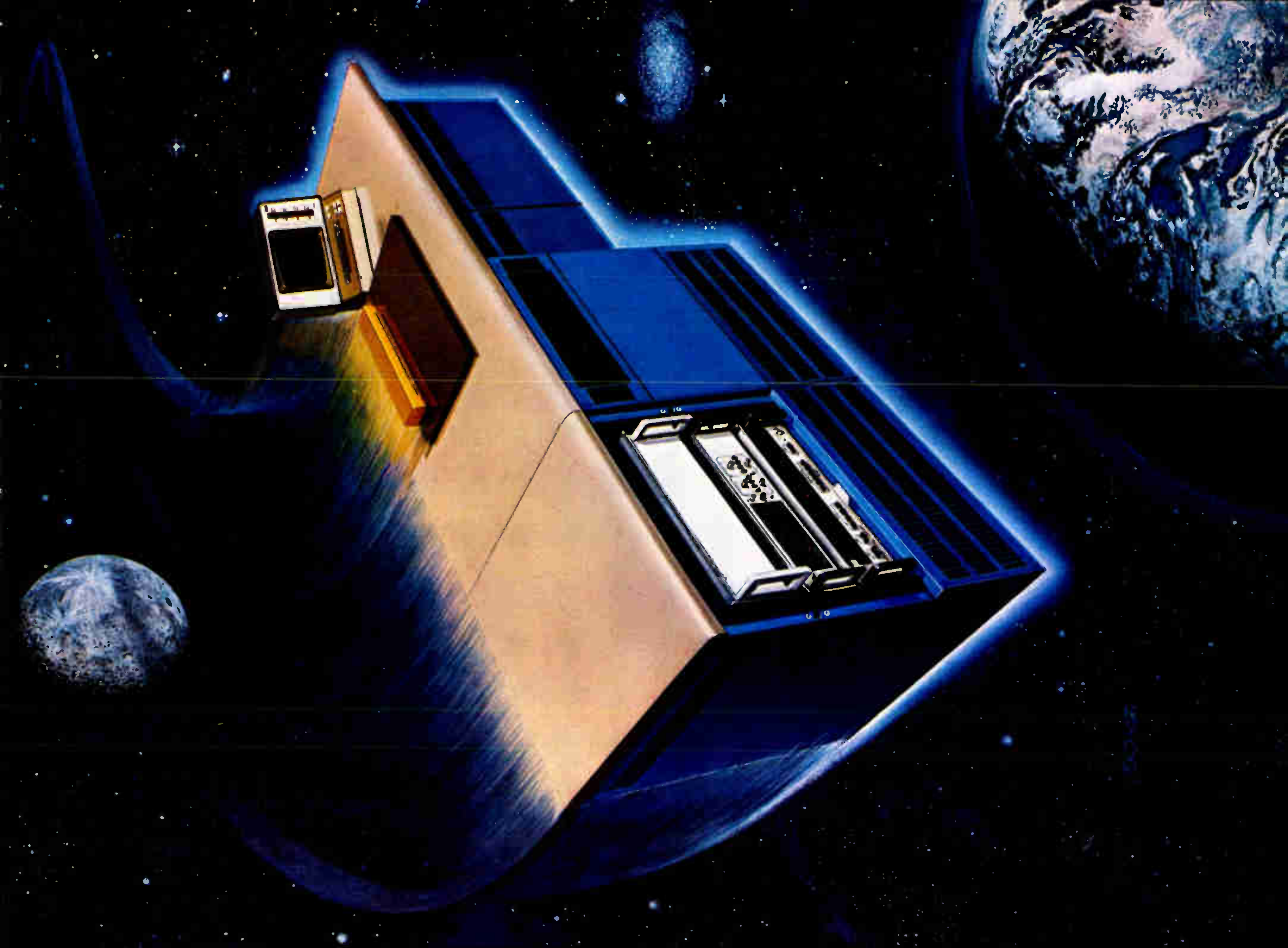


32-bit machine from Prime Computer aimed at OEMs

Two new low-cost midrange minicomputers from Prime Computer Inc., Newton, Mass., are on the way, including Prime's **first 32-bit computer for original-equipment manufacturers.** The Prime 150 and 250 should be announced within a month. Both are software-compatible with Prime's 750 and other 50-series 32-bit machines. The OEM-oriented 150 should come with 256 kilobytes of MOS main memory, an 80-ns cache, operating system, floating-point package, 32-megabyte Winchester disk drive, and other features. Base-priced at $49,000, the 150 should be driven by aggressive discounting into the mid-$30,000 range when purchased in quantity, putting it into competition with less powerful 16-bit machines. The 250 will have similar features, but 512 kilobytes of main memory and a cathode-ray-tube console rather than the 150's virtual-control panel. The $59,000 250 is aimed at end users.

250-Mb/s modem for Westar developed by TRW

A modem that handles communications satellite data at 250 Mb/s has been successfully demonstrated at TRW Defense Space Systems. Developed at Redondo Beach, Calif., for Western Union Space Communications' advanced Westar network, it attains this rate (present commercial ground equipment, by comparison, operates at 64 Mb/s) **by employing time-division multiple-access modulation.** Use of TDMA modulation in commercial satellite hardware also is a first, say TRW engineers.

Hybrid multiplying converter is fast and inexpensive

Hybrid Systems Corp. of Bedford, Mass., is preparing to announce a hybrid digital-to-analog converter **with 16-bit resolution and true 16-bit linearity priced at only $99 in hundreds.** Chiefly behind its low price are its two-chip hybrid design and the firm's new 24-pin commercial package that combine reliability with extremely low cost [*Electronics*, Sept. 27, 1979, p. 168]. Although the 9331-16's 1-μs settling time and its two- and four-quadrant multiplication capability already set it apart from competing devices, its price will be of most interest—other converters approaching the 9331-16's performance cost up to $407 in hundreds.

Mostek to add high-performance 8-bit Z80

Though 16-bit microprocessors are today's state of the art, **Mostek Corp. sees plenty of long-term market potential for 8-bit machines such as the Z80 central processing unit** that it builds as a second source to Zilog. Expected from Mostek during the second quarter is a high-performance version of the Z80 CPU believed to be geared to a 5-to-6-MHz clock rate. The Carrollton, Texas, firm is also continuing to fill out its line of peripherals that work with its 4-MHz Z80 and may duplicate the five-chip set it supplies for the standard 2.5-MHz Z80.

Intel second-sources quad floppy-disk controller chip

Intel Corp. is about to unwrap its 40-pin model 8272, a floppy-disk–controlled chip that supports double-sided, double-density disk drives. It is compatible with both IBM single-density and double-density formats, and it is pin- and functionally compatible with Nippon Electric Co.'s μPD 765. The 8272 uses Intel's HMOS (for high-performance MOS) technology, and it operates at a clock rate of 8 MHz. **It is the first domestic second source of this long-awaited chip,** which allows a 20:1 parts count reduction over conventional controller boards.

20 U. S. companies climb aboard GTE's viewdata

With an eye to the future market for low-cost computer-based information services, over 20 major U. S. corporations have contracted for space in the viewdata system, developed by the British Post Office, that General Telephone and Electronics Corp. is establishing at its computer center in Tampa, Fla. The corporations—among them Chase Manhattan Bank; J. Walter Thompson Co.; McGraw-Hill Inc.; Merrill Lynch, Pierce, Fenner & Smith Inc.; and Time Inc.—are installing **between one and five terminals each tied to Tampa via GTE's Telenet** packet-switched system.

Insac Viewdata Inc., the British software marketing company that along with GTE is offering the service in the U. S., expects many corporate users to move to a private in-house viewdata system with enhanced capabilities and is negotiating with several. The system can be used for communication and for interactive operations such as reservations, ordering, and data base.

Intelligent terminals from IBM do data entry, distribute processing

Further updating its distributed processing offerings, IBM Corp. has introduced the model 5280 Distributed Data System. Coming from the corporation's Atlanta-based General Systems division, the new system includes the model 5285 and 5286 intelligent terminals, as well as the model 5288 controller that can support clusters of up to four model 5281 or 5282 terminals. In addition to being programmed to do data entry for larger System/32, System/34, System/370, or 4300 processors, **the units can be programmed in Cobol to do stand-alone data processing.** The products use a new packaging technique that places up to four large-scale integrated logic chips onto a 36-mm, ceramic chip-carrier.

GenRad company aims at VLSI test equipment

GenRad Inc. of Concord, Mass., a major maker of automatic board test equipment, is going after the coming boom market in testing very large-scale integrated circuits through a new venture: GenRad Semiconductor Test Inc., Santa Clara, Calif., known as GenRad STI. GenRad will invest about $4 million this year in exchange for 80% of the new firm's stock, and in an effort **to transfer some of its computerized board test expertise into the market in bipolar and MOS VLSI quality control and assurance. The other 20% of the stock is owned by GenRad STI managers. GenRad insiders expect initial deliveries of test systems by 1981 and that GenRad STI will be folded into the parent company by 1985.**

Z8000 gets disk operating system

Hemenway Associates Inc. has unveiled what may be the first disk operating system for Zilog Inc.'s Z8000 microprocessor, interfacing it with Winchester and floppy disks. Available for sale at $500 and up or through licensing from the Boston firm, **the HA-CP/Z8000 needs less than 8 kilobytes of memory,** combines memory-resident and transient commands, and transfers data between devices via its Peripheral Interchange Program.

Software package to get Perkin-Elmer into CAD arena

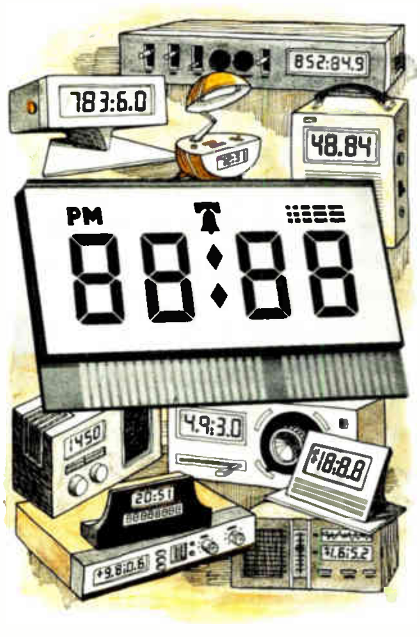
With its 16- and 32-bit minicomputers already widely used in simulation and computer-aided manufacturing systems, Perkin-Elmer Corp.'s Computer Systems division, Oceanport, N. J., is apparently looking to expand into the burgeoning computer-aided design applications. The company is putting the final touches on **a CAD software package that sources say will be released in March.**

BECKMAN Announces Large Area LCD's For All Reasons

Thanks To The World's Largest Watchmakers.

So, what do Liquid Crystal watch displays have to do with other applications? Everything! Yes, for small instruments, clocks, appliances, even point-of-sale equipment. Here's why:

Early on, Beckman developed superior LCD's . . . because of an already extensive knowledge of materials. This helped win contracts with the World's largest watchmakers. So, when the



market opened for large-area LCD's, Beckman was there waiting . . . with the know-how, the resources, and the experience of performing for the best!

Today, Model 737 is aimed squarely at the clock market, while Models 741-3 and 741-4 are primarily for small instruments. The many versions of Model 739 can be used for either. More importantly, these latter types were joined recently by Models 740-56 and 742-58, six and eight digit displays, respectively. The result: At least one large-area LCD for every application.

Meanwhile, there exists a huge custom capability . . . that can build an LCD for your application — just the way you want it.

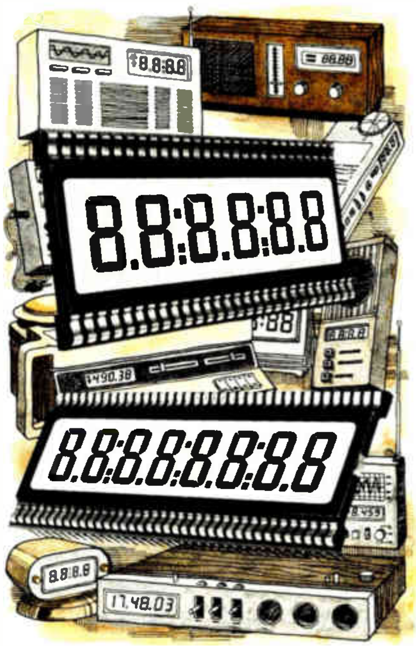
All because Beckman got a head start in the watch business.

That experience also provided the know-how to maintain quality while reducing costs. And, it helped to develop these other advantages for Beckman LCD's:

- Low power consumption. CMOS compatible.
- Excellent contrast ratios; won't wash out, even in direct sunlight.
- Fewer drive components required.
- Choice of designs for night viewing.
- Long life expectancy.
- Fast (100 mS) Total Response time.

One clock manufacturer was so impressed that he wrote:

"Beckman LCD's are the best on the market. In a side-by-side comparison, any knowledgeable user would choose Beckman every time. The contrast ratio is better. Viewing angle (at 3V rms or above) is almost double that of the others. Switching time is almost instantaneous. And, besides, Beckman is a company you can rely on."



What more can we say, other than, "try Beckman large area LCD's . . . for whatever your reason — or, application!"

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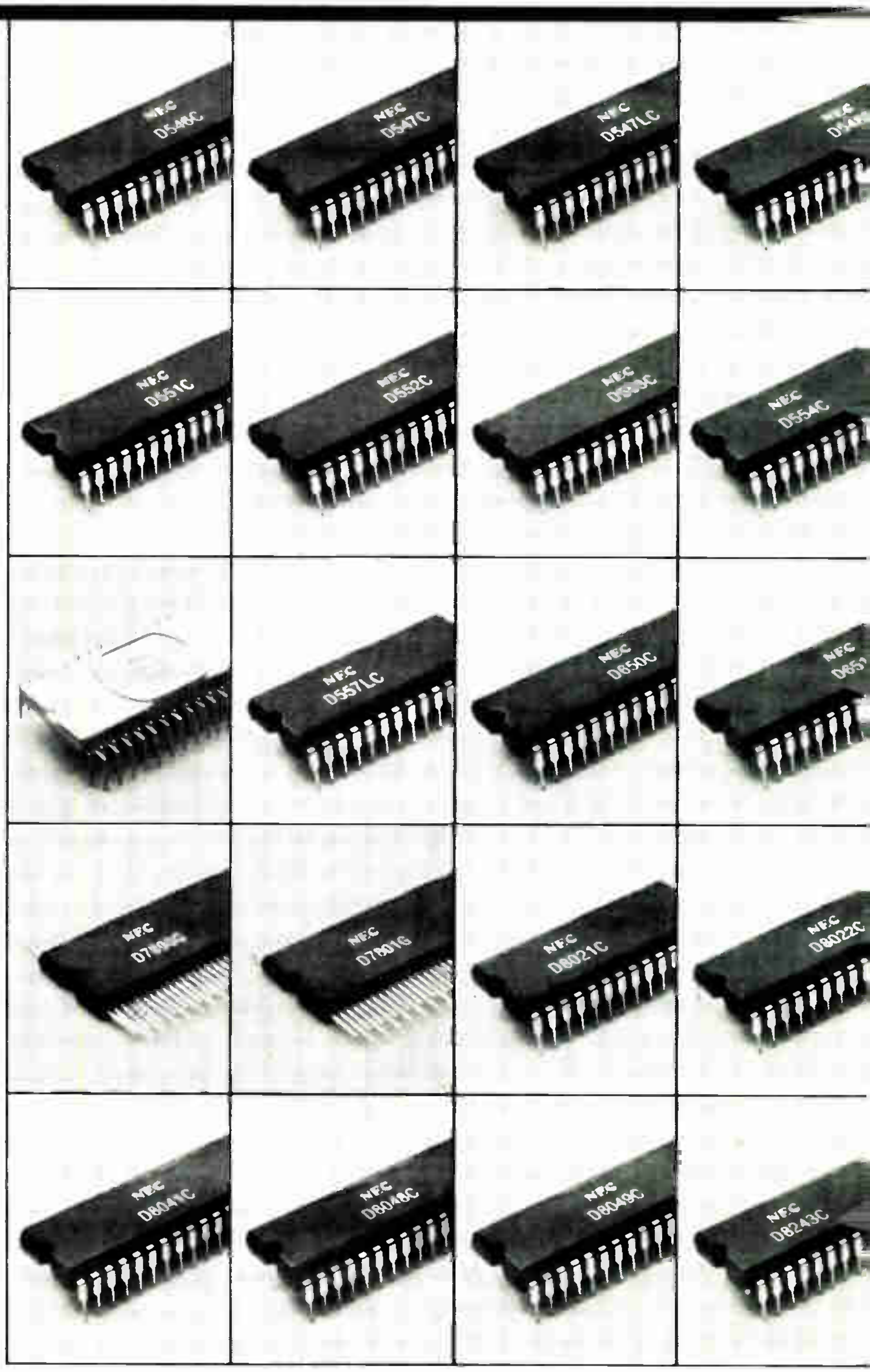
μPD547L	1000 x 8	64 x 4	35	PMOS	−8	Low Power μPD547
μPD548	1920 x 10	96 x 4	35	PMOS	−10	ECR/Scale Applications
μPD550	640 x 8	32 x 4	21	PMOS	−10	FIP Drive/TTL Comp Outputs
μPD550L	640 x 8	32 x 4	21	PMOS	−8	Low Power μPD550
μPD551	1000 x 8	64 x 4	27	PMOS	−10	On Chip A/D
μPD552	1000 x 8	64 x 4	35	PMOS	−10	FIP Drive
μPD553	2000 x 8	96 x 4	35	PMOS	−10	FIP Drive
μPD554	1000 x 8	32 x 4	21	PMOS	−10	FIP Drive/TTL Comp Outputs
μPD555	External	96 x 4	35	PMOS	−10	Development Chip
μPD556	External	96 x 4	35	PMOS	−10	Development Chip
μPD557L	2000 x 8	96 x 4	21	PMOS	−8	Low Power/Small Pkg μPD546
μPD650	2000 x 8	96 x 4	35	CMOS	+5	Icc = 2 mA Max.
μPD651	1000 x 8	64 x 4	35	CMOS	+5	Icc = 2 mA Max.
μPD652	1000 x 8	32 x 4	21	CMOS	+5	Icc = 2 mA Max.
μPD7520	768 x 8	48 x 4	24	PMOS	−6 to −10	On-chip Display Cntrlr
μPD7800	External	128 x 8	48	NMOS	+5	Development Chip
μPD7801	4096 x 8	128 x 8	48	NMOS	+5	Addresses 64K Memory
μPD8021	1024 x 8	64 x 8	21	NMOS	+5	Zero Cross Detection
μPD8022	2048 x 8	64 x 8	28	NMOS	+5	On-chip A/D
μPD8035L	External	64 x 8	27	NMOS	+5	8048 Compatible
μPD8039L	External	128 x 8	27	NMOS	+5	8049 Compatible
μPD8041/A	1024 x 8	64 x 8	18	NMOS	+5	Peripheral Cntrlr
μPD8048	1024 x 8	64 x 8	27	NMOS	+5	Industry Standard
μPD8049	2048 x 8	128 x 8	27	NMOS	+5	11 MHz Clock
μPD8243			16	NMOS	+5	4. 4-Bit I/O Ports
μPD8741A	1024 x 8	64 x 8	27	NMOS	+5	UV EPROM Version of 8041A
μPD8748	1024 x 8	64 x 8	18	NMOS	+5	UV EPROM Version of 8048



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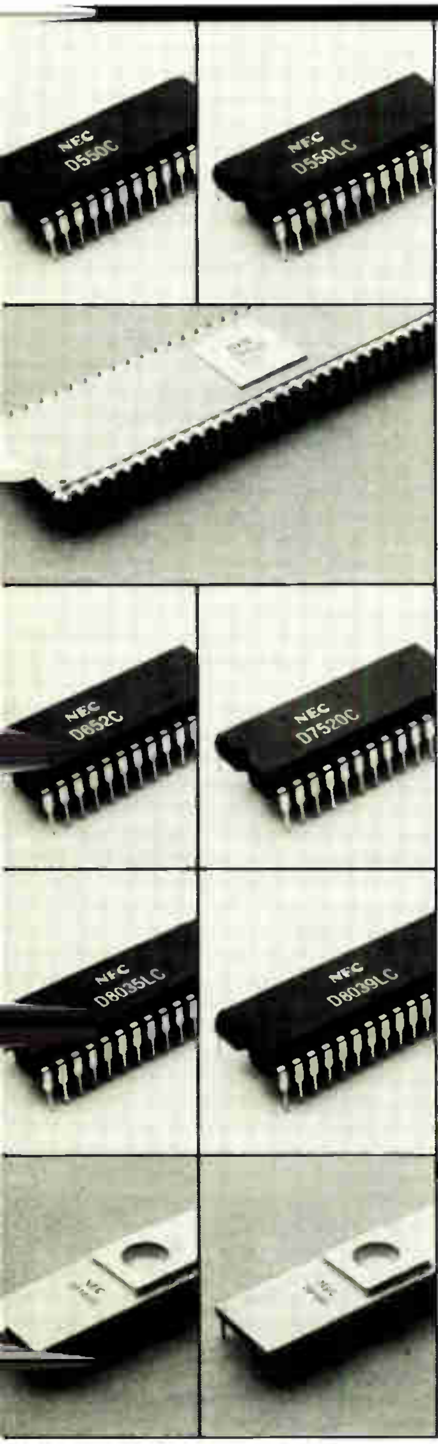

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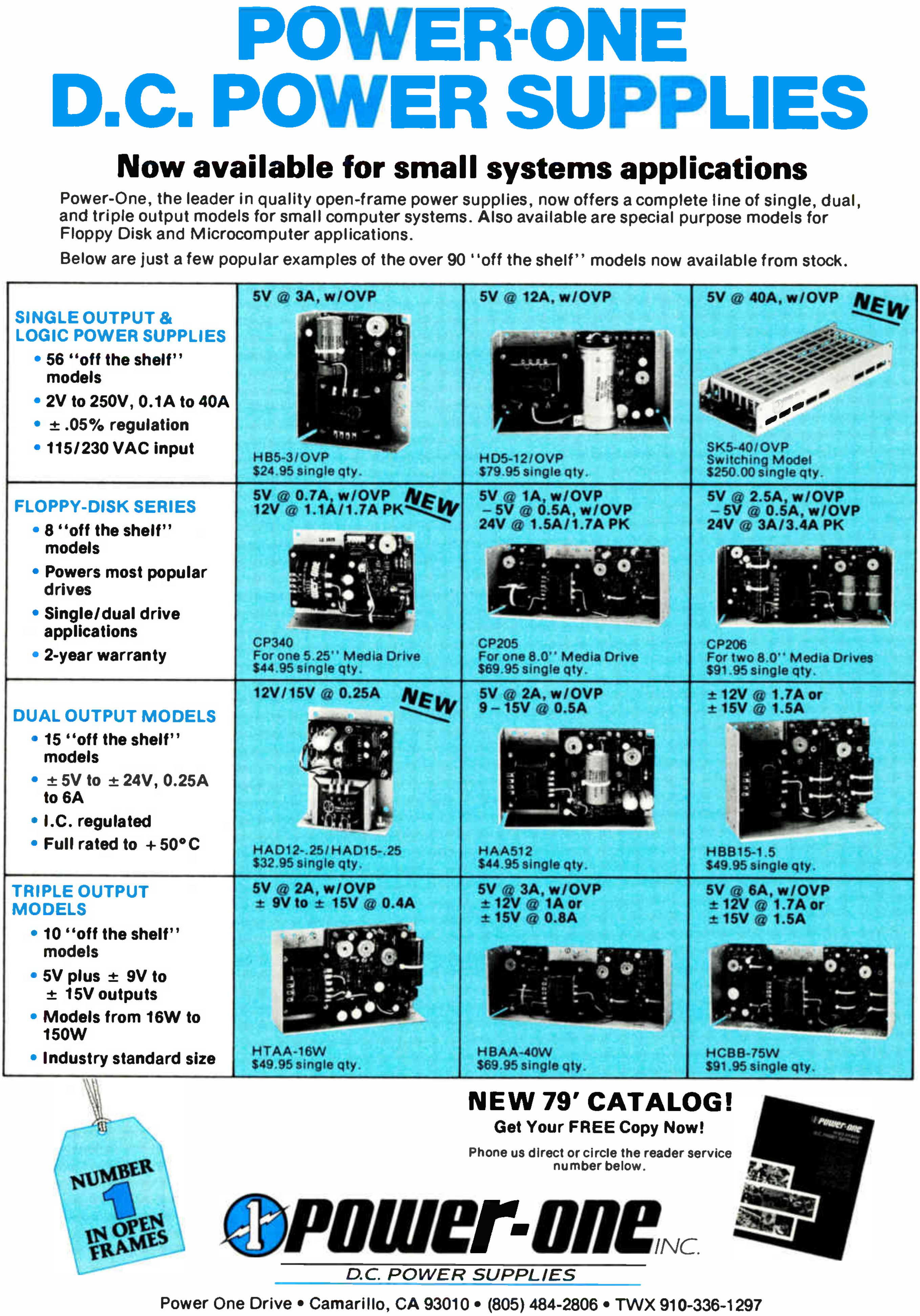
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Talking products, voice response star at consumer show

by Bruce LeBoss, San Francisco regional bureau manager

Prototypes and introductions run gamut from calculators to personal computers; Japanese firms appear in the forefront

Even if the Consumer Electronics Show in Las Vegas had not been crowded, it still would have sounded like a sellout because microcircuits for speech synthesis and speech recognition in a wide range of new products had a lot to say.

It seems clear that the early 1980s will see an explosion of such consumer products. Interestingly, Japanese companies appear to be in the forefront of applying large-scale integration to speech technology, at least for consumer products.

Unveilings. Among the first-generation and prototype products shown were a calculator, digital clock, and microwave oven that talk, as well as a television receiver and a high-fidelity system that are voice-actuated. Also previewed were prototype electronic games and personal computers with speech-synthesis and -recognition capabilities.

Sharp Corp. took the wrappings off a talking calculator that uses a microprocessor-based voice synthesizer to confirm all calculating processes. A similar digital clock reports the correct time when a special key or a remote control is touched. The clock will be available in the U.S. this spring; the calculator will hit the stores this summer.

Their voice-synthesis system uses two 4-bit complementary-MOS microcomputers. One handles such functions as display, keyboard, and clock control, and the other provides digital-to-analog conversion and voice generation. Both custom devices were developed by Sharp's semiconductor division near Osaka, Japan.

The speech generator uses pulse-code modulation that compresses data 5,000%. The calculator, with its greater vocabulary, uses an outboard read-only memory the clock can forego. The technology "will be expanded to translators, hand-held calculators, and other products especially for the sightless market," says a Sharp spokesman.

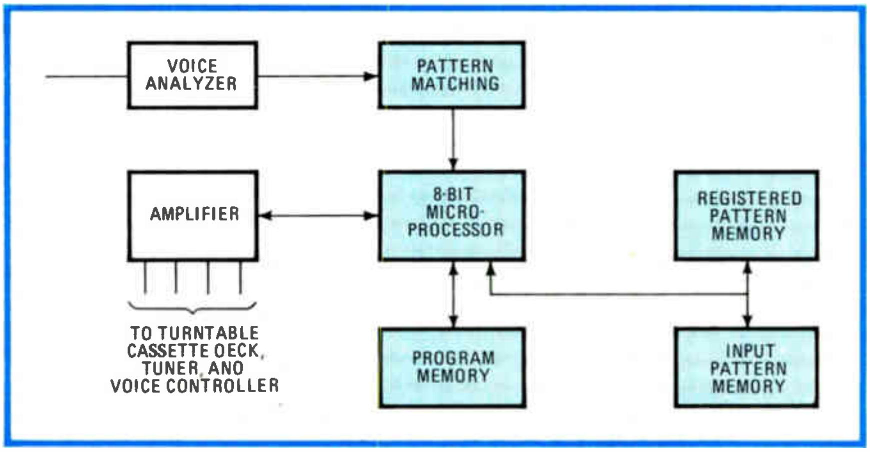
Toshiba Corp. of Yokohama demonstrated voice-actuated TV and hi-fi prototypes [*Electronics*, Jan. 3, p. 46]. They use microprocessor technology (see figure) to respond only to a specific voice whose pattern they store.

The custom p-channel MOS microcomputer has 2 kilobytes of ROM and 3 kilobytes of random-access memory. It is a member of a family of chips similar to the Intel 8085. A C-MOS version is under development, as is a voice-synthesis chip, both of which could be "incorporated in ovens and other kitchen appliances, as well as in doors and other products," a spokesman says.

Talking oven. Also at the consumer show was the prototype of a talking microwave oven from Quasar Co., the U.S. subsidiary of Matsushita Electric Corp. of America. It can announce such news as the temperature of the food in the oven and cooking time remaining.

The oven uses microcomputer and voice-synthesis chips, both p-MOS and both developed in Japan. Quasar also plans to use them in other products, such as TV sets. Its Information Processor, a language translator that also serves as a four-function calculator, is expected to talk within a year. Craig Corp., a pioneer in language translators, also is working on speech synthesis.

Equal interest in talking products comes from the electronic games corner, though some manufacturers



Responsive. With the owner's voice pattern in the registered pattern memory, Toshiba's voice actuator responds by comparing the digitized voice input to the stored pattern.

think the chips the semiconductor makers are going to offer are not yet capable enough. Other game makers are plunging into speech.

For example, Mattel Inc.'s Electronics division, Hawthorne, Calif., showed Talk to It, a voice-actuated game, and says it has plans all the way up to home message centers and beyond. Atari Inc., Sunnyvale, Calif., showed the prototype of a new video game, Home Run, that has limited speech capability.

Also at the show was Texas Instruments Inc.'s speech synthesizer for its 99/4 home computer [*Electronics*, June 21, p. 93] and a voice synthesis prototype for Commodore's Pet home computer. The Pet prototype has a string of phonemes with variable pitch, which makes them sound more natural.

Software

High-level language is interactive and fast; software pack is aimed at microcomputers

In enhancing its microcomputerized health information system, General Health, a small, Washington, D. C.-based company has come up with a high-level language that combines efficient execution with considerable interactivity. Though designed for in-house use, Simpl mushroomed into a complete software package, including an operating system and extensive utilities, appealing to microcomputer users.

Dual-purpose. Simpl sprang from a need to use a single language both for software development and customer data entry. Although one other interactive language is ubiquitous—Basic—General Health, like many others, is appalled by it. Rather than succumb to poor software tools, it put its foot down and decided to start from scratch.

So the company developed Simpl as a super-interactive microprocessor language. The system includes the language, a compiler and assembler written in Simpl, a text editor, and utility routines. It can serve many applications outside the medical field and has recently been fitted with a speech-synthesis software option (see "Simpl can talk, too").

Hugo Feugen, vice president of computer development for the company says Simpl's advantages are three-fold. First, its highly interactive nature is particularly friendly to users. Random portions of a cathode-ray-tube screen can be selectively addressed or erased, and output is free-format. Also, built-in subroutines make short work of otherwise key-intensive tasks like string manipulation and branching to a program section off-screen.

The second advantage for software developers as well as users is the language's calculational ability. Feugen says that languages like Tiny-Basic and Tiny-C do not have sufficient calculational ability. Floating-point Basic does, but all operations must be done in the floating-point mode, which can degrade efficiency. Simpl can work on bytes, words, and floating-point operands with 13.4-decimal-digit precision, and these data types are automatically converted from one to another.

Finally, the language allows easy access to large data bases. Access to files is by name, and the files may be nested several levels deep in heirarchical subdirectories.

Compiled. Simpl is compiled, not interpreted like other interactive languages such as Basic. General Health says this arrangement does not cut down on the level of interaction and actually increases speed. A program with 2,800 source lines would take about 5 minutes to compile.

The language currently runs on a Z80 microcomputer with 56 kilobytes of memory, but the company stresses that it is not tied to the one set of hardware. It intends to transport the language to other microprocessors. **-John G. Posa**

Simpl can talk, too

General Health's goal is to evolve the Simpl system into a stand-alone station for the control of a variety of functions in homes, schools, or offices. To make it even more interactive, Feugan developed a speech synthesis program that executes three times faster than real time. This does not mean that the output sounds like a Chipmunks' record; it means that the program takes about 2 seconds to generate 6 seconds of speech, so the remaining 4 seconds are available for other processing chores.

The speech synthesis routine converts ASCII textual information into spoken output. It now works for English, Spanish, and German. In development are programs for Dutch, Italian, Russian, and French. Whereas other text-to-speech synthesis programs use character-replacement techniques to generate speech, Feugen's program has an unlimited vocabulary and fast rule processing. Even rules governing stress, intonation, and rhythm can be incorporated with little difficulty. **-J.G.P.**

Financing

Chip maker forming R&D partnerships

At first glance, semiconductor research and development may appear to have nothing in common with oil drilling and real estate development, but Western Digital Corp. chairman Charles W. Missler saw a link. Chip R&D, he realized, can tap the same capital source as these other high-risk ventures: tax-sheltered limited partnerships.

The first such partnership, involving $800,000 for three chips, was organized late last month following an earlier trial run with Missler as principal. The chairman of the

Late entrants star at solid-state parley

As expected, the late papers will be some of the great papers at next month's International Solid State Circuits Conference in San Francisco. Two heights in solid-state memory technology will be marked; anticipated but nonetheless enterprising, they are the 256-K random-access memory and the 64-K static RAM. These and other late and regular papers will underscore Japanese semiconductor expertise.

- A 256-K dynamic RAM from NEC-Toshiba Information Systems features a 160-nanosecond access time and a 350-ns cycle time.
- A 256-K RAM from NTT Musashino Electrical Communication Lab is made with molybdenum-polysilicon technology. Access time is 100 ns, and cycle time is 200 ns.
- A 64-K static RAM from Matsushita has an access time of 80 ns. It consumes 300 milliwatts while active and only 75 mW on standby.
- A stacked-high capacitor RAM from Japan's Cooperative Laboratories uses tantalum oxide as a dielectric. A 512-K RAM has been fabricated.
- A color image sensor from Matsushita uses heterojunction thin-film photoconductors. It has a 413-by-506-element array and an on-chip filter.
- A numerical analysis program from the Musashino lab simulates the characteristics of a semiconductor device regardless of technology.
- An erasable programmable read-only memory family from Texas Instruments uses a new approach to cell design that permits dense 128-K and high-speed 32-K memories.
- Charge-domain recursive filters from General Electric eliminate the need for feedback amplification.
- A switched-capacitor filter from Reticon is programmable and fast enough for real-time applications.
- A monolithic filter from Bell Northern Research is fabricated with n-channel technology and incorporates line-balancing circuitry.
- An n-channel MOS low-power filter from Mostek, for pulse-code-modulation applications, filters transmitted and received signals. **-John G. Posa**

Irvine, Calif., company hails the concept as good for the company and equally attractive for investors.

Chip makers who enter limited R&D partnerships will find such advantages as:

- No increase in bank debt or dilution of shareholder equity.
- Favorable price-to-cost ratio for the capital, especially in the present era of high interest rates.
- No charge against operations for R&D (when internally financed) or for interest (when the money is borrowed).

For their part, investors in high-risk limited partnerships will find such advantages as:

- A tax write-off within one year of as high as 85% (if the Internal Revenue Service accepts the partnership).
- Independently of the tax advantages, a potential return on the individual investment of as high as 30%.
- Ownership of the chip design and therefore a right to royalties (if the chip is patentable, royalties may be considered capital gains).

Missler says another partnership is in organization, and the firm hopes to use it and suceeding ones to raise millions of dollars into the 1980s. He expects other semiconductor firms, even well-financed ones, to look closely at such arrangements to help defray what look to be staggering R&D costs—and even more staggering equipment costs—covered under slightly different IRS provisions for limited partnerships.

Risks. Of course, most drillers for oil find dry holes, and many real-estate ventures flop. Similarly, many chips fail to make it out of R&D or die in the marketplace.

The risks involved are the genesis for the Internal Revenue provisions that can make limited partnership so attractive to investors. On the other hand, there must be a genuine risk involved, or else the IRS will not accept the partnership.

An oil industry source says first-year write-offs run from 50% to 75%, and similar substantial write-offs must be justified in semiconductor limited partnerships for the IRS to accept them, say tax authorities. Most industry sources agree with Missler that action from other semiconductor firms awaits Western Digital's track record. Then, they say, small companies will be the first to jump in.

The way Western Digital is working its partnerships is to get outside investors to put up cash in blocks of $50,000 for specific chips. Its first partnership with Missler covered its data-encryption part [*Electronics*, Jan. 4, 1979, p. 41], and the new partnership with a total of 16 investors covers the X.25 packet-switching chip [*Electronics*, Dec. 20, p. 89], an avionics chip, and a microcontroller. **-Larry Waller**

Communications

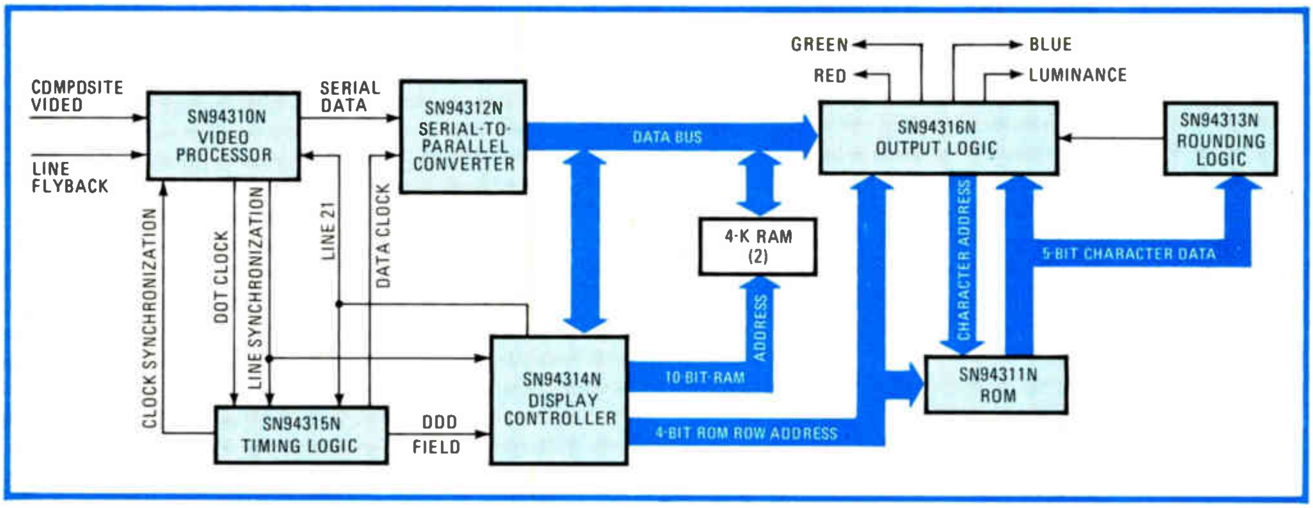
Chip set captions TV programs for deaf

Beginning this spring, deaf and hard-of-hearing TV viewers will gain new access to prime-time programming, thanks to a captioning project that depends on a custom chip set developed by Texas Instruments Inc. The captions will be visible only on specially equipped TV sets.

Project. The Federally sponsored project calls for digitally encoded subtitles corresponding to a program's soundtrack to be transmitted on line 21 of the TV vertical blanking interval. A new nonprofit agency known as the National Captioning Institute will put the caption information on floppy disks for network use with videotape equipment.

TI developed the seven-chip caption decoder over a two-year period under contract to the Public Broadcasting System. With speed and linear requirements in mind, it uses a variety of bipolar techniques, notes L. Dwain Chaffin, advanced circuits department manager at the company's Sherman, Texas, plant.

The heart of the system is the display controller, which combines



Six chips. Texas Instruments has developed a six-chip set that turns digitally transmitted codes into subtitles not otherwise visible on the TV screen. There also is a random-access memory that temporarily stores the data necessary for character generation by the ROM.

linear bipolar circuitry with integrated injection logic on a 47,000-square-mil chip. The controller works in conjunction with a linear video processor chip and a 5,760-bit read-only-memory chip that stores the captioning characters. (see figure above).

The ROM is made with Schottky TTL, primarily for speed, says Chaffin. Each of the 96 ASCII and 8 special characters is stored in 45 bits, and access time is 280 nanoseconds. The 250-milliwatt typical power dissipation is low in view of the quantity of circuitry on the 18,000-mil² ROM, Chaffin observes.

Other devices in the chip set are four low-power Schottky parts that handle such functions as timing and output logic and "rounding" logic to make characters easier to read. Chaffin says TI drew upon earlier development work for its Teletext chip set for the British video information system.

Prices. Without the chip set, the $249.95 retail price for decoder units would be more than double, he adds. Sears Roebuck and Co. is the sole distributor for these adapters and for the 19-inch color TV receivers to incorporate the circuitry. To be available next fall, the receivers will cost around $500, with about $100 attributable to the built-in captioning circuitry.

Sanyo Electric Co. of Japan is making both adapters and TV sets for Sears. TI is shipping 100,000 chip sets to Sanyo.

The Public Broadcasting System initiated work on the captioning project in 1972, under contract with the Department of Health, Education and Welfare. The National Captioning Institute, in Falls Church, Va., is currently operating under HEW grants, but will receive an $8 royalty for each adapter and receiver sold and will charge networks $2,000 per program hour for the coded floppy disks. In addition to

Automated tellers hit Illinois

Recent changes in the restrictive Illinois banking laws are opening up a fertile new market for automated teller machines—and the regulations also mean that the banks and their system vendors will develop new software. Until this month, Illinois treated the machines as branch banks, forbidden under state law. Now, automated tellers get an official blessing, but to ensure that the big state's many small financial institutions do not get left out, the new law requires mandatory sharing among banks of remote machines.

Thus the state's setup will require massive new communications switching schemes to link more than 600 banks, 150 data-processing centers, and about 500 new teller machines. Adding to the complexity, several big Chicago banks and independent contractors are developing the required special networks for the teller machines—several times larger than those attempted elsewhere in the U. S.

For example, First National Bank of Chicago and Continental Bank are each planning new networks they will share with other banks. Each net may have more than 100 automated tellers, more than triple the size of the only currently operating multibank network, in Seattle.

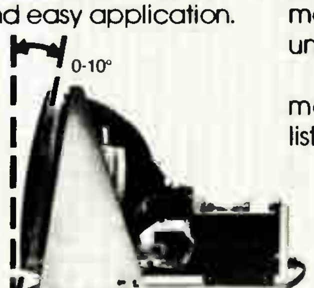
The activity in Illinois comes during a surge in nationwide interest in automated tellers. More than 5,000 of the machines were sold in 1979, better than double the annual level of 1978.

Other electronic funds transfer services are largely shunned by consumers, but the convenience of 24-hour-a day automated tellers sparks their interest. One survey indicates that about 80% of bank customers in a position to take advantage of EFT services now base their choice of banks on the availability of teller machines.

Improved automated tellers introduced in the last year feature lower operating costs, increased reliability, and better interfacing with the customer. For example, one system in New Jersey communicates in English, Spanish, or Portugese, based on input from the user's magnetic-striped card.

-Larry Marion


SANYO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proprietary rights to the circuits, the Public Broadcasting Service turned over to the institute 20 Z80-based editing consoles and associated captioning software. As well as the public network, ABC and NBC will participate beginning in March with a total of 19 hours of weekly programming. More programming will come later. **-Wesley R. Iversen**

Computers

ICL enhances U. S. push in business systems with new model offering more pheripherals

To reassert its presence in the market for small business systems, ICL Inc. is launching the System 10 model 320, a more competitive replacement for its model 220 stand-alone system. The announcement last week coincides with the third anniversary of the U. S. subsidiary of Great Britain's International Computers Ltd.

From its East Brunswick, N. J., headquarters, the firm has been marketing the System 10 and 1500 series computers, acquired from the now defunct Singer Business Machines operation, the 2903 model from the British computer giant, as well as the 220. But competitors have never given it credit for much of a U. S. market presence.

The model 320 and a new marketing thrust are out to change that low profile, says Chuck Barnes, executive vice president and general manager of the Irving, Texas–based Distributive Systems division, marketer of the new computer.

Indeed, the 320 has features to overcome deficiencies of the model 220, which it replaces. Primary among these are a new range of peripherals, especially disk drives with larger capacities.

Memory. Although it uses basically the same central processing unit as the 220, the 320 replaces the former's core memory with less expensive and more compact semiconductor storage. Thus maximum memory capacity has jumped 25% from 160 to 200 kilobytes.

The completely redesigned disk-drive controller uses a Z80 microprocessor to reduce size and cost. It can support as many as four drives for a maximum of 60 megabytes.

To attach to this controller, the 320 offers two basic types of drives: cartridge module and Control Data Corp.'s popular Storage Module Drive. The cartridge module offers 10 megabytes of removable memory and 10, 30, or 50 megabytes of fixed disk. The Storage Module Drive offers 40, 80, or 160 megabytes of totally removable disk storage.

ICL makes the point that configurations may mix the two types of drive to the maximum supportable 160 megabytes. In contrast, the 220 offered a maximum of a 40-megabyte removable disk.

Another major peripheral addition is a new cathode-ray-tube terminal with two 8085 microprocessors. Like the basic unit, it was designed and will be built at the Product Development Group in Utica, N. Y., which is the former Singer factory.

The choice of printers has been expanded to include three matrix printers with speeds ranging from 60 to 180 characters per second. Four line printers run between 75 and 600 lines per minute.

Software-compatible with the older system 10 units, the 320 uses the same multiprogramming architecture, supporting up to 20 partitions (tasks) at a time. Both asynchronous and binary synchronous communications are available.

The tab. Prices will range from $35,000 to more than $100,000 depending on system configuration. Barnes says the 320's price/performance ratio will be aggressively competitive with such small business computers as IBM's System/34 and/38 and Sperry Univac's BC/7, as well as units from Basic Four Corp. and Wang Laboratories Inc.

In addition to the new hardware, ICL Inc. has now set up its own U. S.

Pitney Bowes into word processing

Fresh from its purchase of Artec International Corp. of Santa Clara, Calif., Pitney Bowes Inc. is assigning marketing responsibility for Artec's Dual Display text processor to another recently acquired subsidiary, Dictaphone Corp. The combination of a full-page cathode-ray tube and a single-line keyboard users to look at the line just typed, which should increase productivity, according to Artec.

The system also features concurrent processing so that non-keyboard functions like sorting and selecting can be performed simultaneously with typing or editing. The basic system (right) of CRT, keyboard, 40-character to second daisy-wheel printer, and floppy-disk module that can hold 200 text pages per floppy costs $15,950. Each additional work station is $2,995. **-Benjamin A. Mason**

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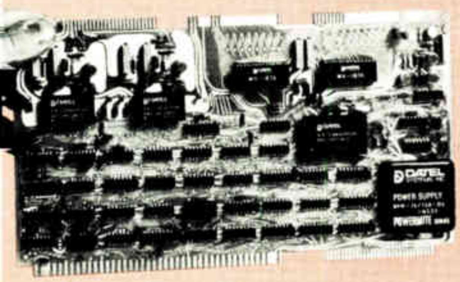

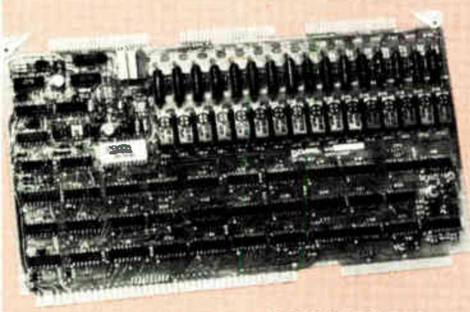

ST-711RLY8D
ST-711RLY16D

ST-711............$625 SINGLES
ST-732............$788 SINGLES

(NON-ISOLATED)

- Model ST-711: 32S/16D A/D Channels, no D/A Channels........$625 (Singles)
- Model ST-732: 32S/16D A/D Channels, includes 2 D/A Channels plus current loop outputs.............$788 (Singles)
- Full mechanical, electrical, and pinout compatibility to Intel's SBC-711/732 Analog I/O Boards.
- Operates with all Multibus and SBC-Series compatible microcomputers including the 16-bit SBC-86/12 (except SBC-80/04).
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- Includes program-gatable Pacer start clock, 1 mS to 1 sec., crystal-controlled.
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- Includes Programmable Gain Amplifier.
- Includes Diagnostic Program tape for immediate TTY or CRT print-out.
- 12 bit binary conversion; 20 microsecond throughput period.

ST-711RLY8D.....$683 SINGLES
ST-711RLY16D...$1045 SINGLES

(ISOLATED)

- 8 or 16 differential A/D channels using a "Flying Capacitor" relay multiplexer for high common mode noise rejection (126 dB) and high isolation (±250V RMS).
- Complete hardware and software compatibility to Multibus and SBC-Series microcomputers. Uses identical programming and register assignments to SBC-711/732, and ST-711/732 A/D-D/A boards.
- 10 mV to 2V input ranges including Programmable Gain Amplifier. 12 binary bit A/D resolution.
- Includes Diagnostic Program for immediate TTY or CRT printout.
- Includes 10-stage Pacer Start Clock.
- ST-711RLY8D (8 Channels) $683, singles
- ST-711RLY16D (16 Channels) $1045, singles

ST-724............$595 SINGLES

- 4 D/A Channels plus 4 4-20 mA current loop amplifiers.
- 12 binary bits, Multibus compatible.

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Circle 45 on reader service card

service operation. Barnes says a two-year program will expand this service system nationwide.

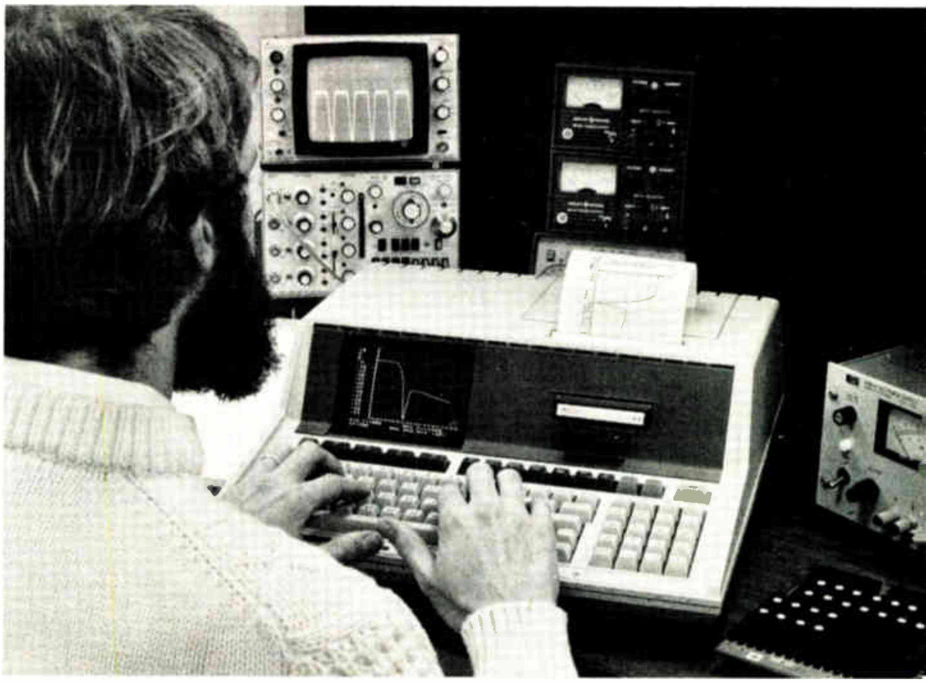
Unchanged is the marketing set-up, through 40 exclusive dealers, which Barnes claims has proved successful. "We sold some 1,200 model 220s last year, and that's more than Singer sold in their best years," he says. -**Anthony Durniak**

Consumer

Compact computer packs in functions

Shying away from the highly competitive marketplace for low-end home computers, Hewlett-Packard Co. is launching a $3,250 personal computer for technical and business use. The HP-85 packs such features as a display, thermal printer, and extensive input/output capability into a 16-by-18-by-8-inch unit that weighs 18 pounds.

The new computer uses an enhanced version of the Basic language with editing capabilities and extensive software packs for its intended users. It also has built-in, interactive graphics (see photograph).



Compact. The typewriter-sized HP-85 personal computer for business and technical users has a high-resolution CRT display, thermal printer, and cartridge tape drive—all built in.

Hardware. HP has tailored the hardware package to the demands that technical and professional users will make. It uses an 8-bit n-channel MOS microcomputer developed at the Corvallis (Ore.) division, which will manufacture and market the HP-85. The four I/O ports can hold a range of optional interface modules that permit many data-acquisition and control applications.

There is also plenty of data and program storage. Standard is 16 kilobytes of read/write memory, expandable to 32 kilobytes by plugging a module into one of the four I/O ports on the rear. The built-in read-only memory is 32 kilobytes, expandable to 80 kilobytes.

The long-awaited machine [*Electronics*, Jan. 3, p. 33] bowed at the Winter Consumer Electronics show. Interestingly HP thinks that the market at which it is aimed is pretty much untapped, in spite of the top-end Pet and Apple home computers that come with enhancements that appeal to professional users.

The HP-85's programming language offers 146 commands with 12-digit accuracy and unlimited string length. There are 42 predefined functions, four levels of program security, and flexible output formatting. Applications cartridges include general statistics, mathematics, electrical engineering, finance, linear programming, and the like.

Graphics. The highly automated graphics capability is designed to draw plots on the cathode-ray-tube display that will clarify complex data pictorially. Also, a single key stroke will cause a hard copy of the plot to come out on the built-in thermal printer.

This printer also offers the full 128-character ASCII set, as well as underlining, and can print two 32-character lines a second. Furthermore, it can rotate the data from the display 90° when plotting so that it can print a chain of strip charts.

Optional interface modules, to be introduced gradually, include IEEE-488; RS-232-C; binary-coded decimal, and general-purpose 16-bit bidirectional interfaces. They will interconnect through the I/O ports, which also will let the user expand capabilities through a variety of peripherals to be introduced.

The 5-in. CRT is monochromatic, but color is expected to be offered. It can display as many as 16 alphanumeric lines of 32 characters each. As a graphics display, it has a 256-by-192-dot field, extremely high density for a personal computer.

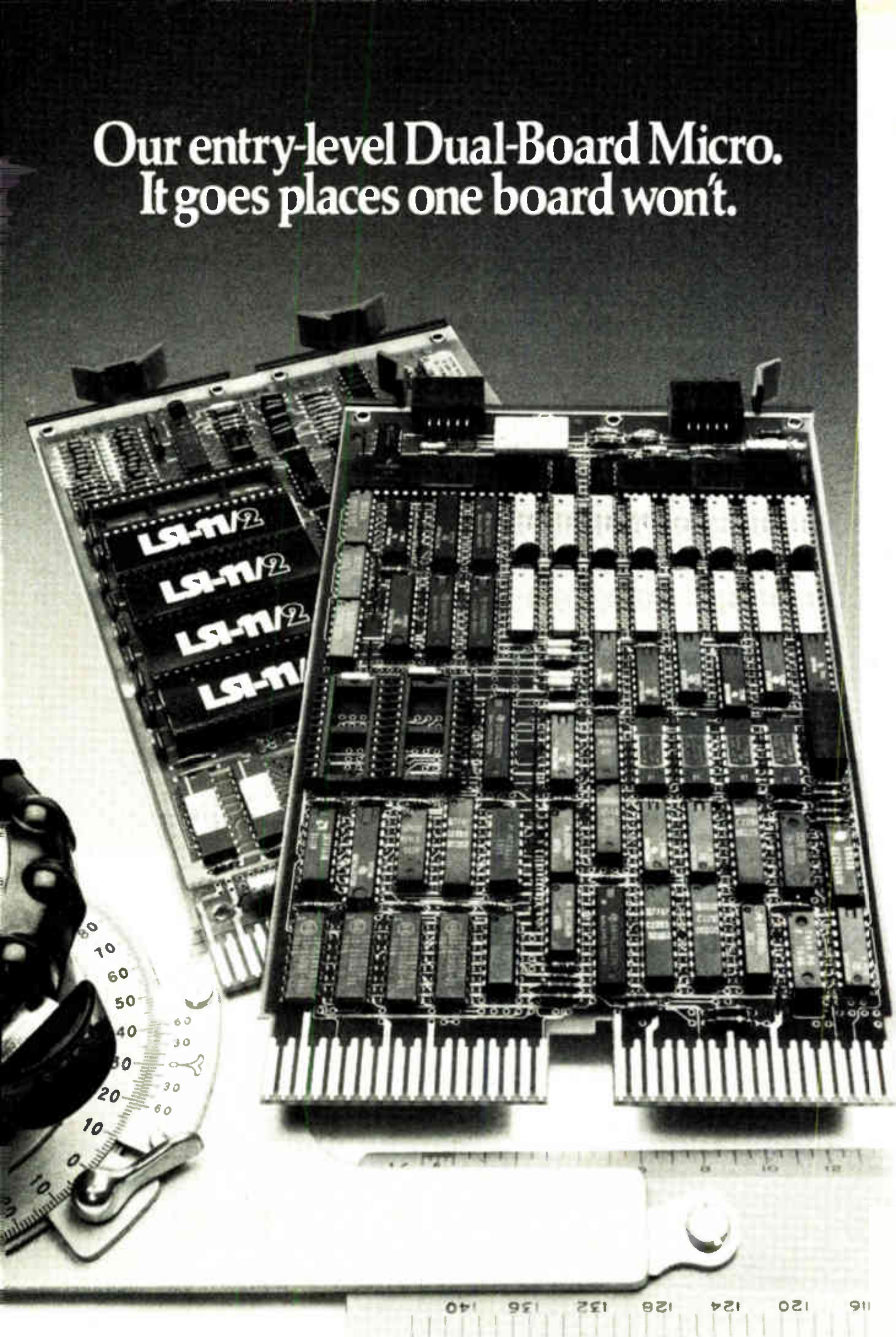
The HP-85 also has a cartridge tape drive with a user capacity of 217 kilobytes. Read/write speed is 10 inches per second, with a search speed of 60 in./s and a transfer rate of 650 bytes/s. -**Bruce LeBoss**

Lasers

Line-of-sight unit links teletypewriters

Solid-state lasers appear to have a future in high-speed digital transmission, and security-conscious dedicated data networks are indeed the principal application of American Laser System Inc.'s 10-kilobit/second gallium arsenide unit. Somewhat to the surprise of the small

Our entry-level Dual-Board Micro. It goes places one board won't.



Instead of putting all the capability we could on one large board, like other micro companies, we put it on two very small boards. The result is the best form factor you can find in 16-bit entry-level micros.

And for just $826 in 100's.

On one 5.2" x 8.9" (13.2 cm x 22.8 cm) board you get the 16-bit LSI-11/2 microcomputer, with the PDP-11 instruction set and a 380ns cycle time. On the other board you get everything else to implement your system—8Kb RAM standard (or 32Kb optional), space for up to 8Kb PROM, console interface port, asynchronous serial I/O, and clock.

You also get the flexibility to configure more powerful systems simply by replacing the LSI-11/2 processor board with our new LSI-11/23.

At Digital, we look at micros with a systems understanding. That's why we offer our 16-bit microcomputer family—in boards, boxes and systems—with the most powerful, advanced, and proven software on the market. And why we offer hundreds of hardware tools—memory and interface boards, complete development systems, peripherals and terminals. All backed by over 11,000 support people worldwide.

It's the total approach to micros, only from Digital.

For more information, contact **Digital Equipment Corporation,** MR2-2/M70, One Iron Way, Marlborough, MA 01752. Or call toll-free 800-225-9220. (In MA, HA, AL, and Canada, call 617-481-7400, ext. 5144.) Or contact your local Hamilton/Avnet distributor. In Europe: 12 av. des Morgines, 1213 Petit-Lancy/Geneva. In Canada: Digital Equipment of Canada, Ltd.

It took the minicomputer company to make micros this easy.

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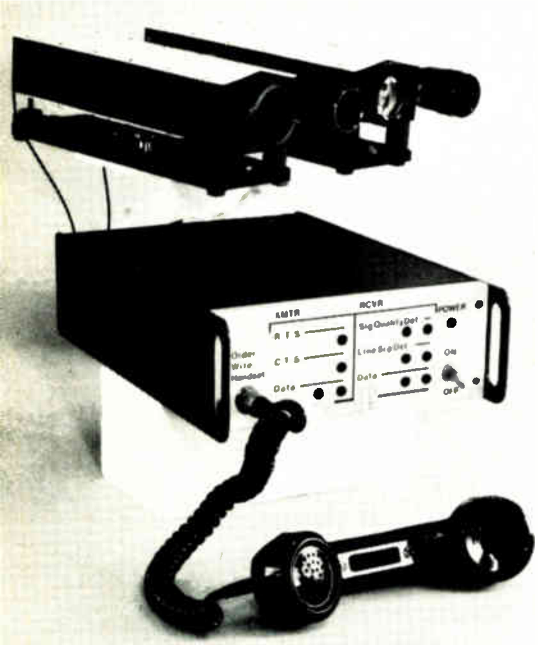


Many uses. A GaAs laser unit, designed for secure data transmission over fiber-optic cables, is serving as a line-of-sight teletypewriter link. It also can carry voice traffic.

Goleta, Calif., firm, its model 736 is also attracting attention as a line-of-sight transmission system.

The first such installation is a two-mile link for teletypewriter traffic in Trinidad. The advantages of the link between the Trinidad External Telephone Co. and a downtown Port-of-Spain building are twofold.

Advantages. "Land lines did not have to be installed through the city, and licences for microwave did not have to be granted," says Duncan B. Campbell, American Laser's president. Not only are lasers simpler to put into operation, but the $10,000 system cost for two transmitters, two receivers, and interface modules proves much less than the $40,000 or so price of the equivalent microwave tab. Cables are even more costly.

"All we had to do was put together interface modules so it can tie into telephone equipment," Campbell adds. These standard telecommunications modules, made by Wescom Inc. of Downers Grove, Ill., were configured specifically for Trinidad. "Wescom acted as a go-

News briefs

Color may be coming for Commodore's Pets

Coming soon may be color displays for the Pet personal computer and CBM business systems from Commodore Business Machines (Canada) Ltd. of Santa Clara, Calif. A video interface circuit from its MOS Technology subsidiary would make this possible. Now in prototype, the silicon-gate n-channel 6552 provides 40 columns of screen data and has high-resolution color graphics and tone color, among other functions. The chip will be available commercially from the Valley Forge, Pa., subsidiary.

Commodore also is introducing a line of calculators based on a new complementary-MOS 4-bit microcomputer that reportedly is smaller than competitive chips and can directly drive multiplexed liquid-crystal displays. Also in development by the company is a large-area LCD for computers and consumer products.

Job hopping doesn't pay, says the University of Illinois

The less engineers, including electrical engineers, change jobs, the more they are apt to make, the University of Illinois says. From the class of 1969, 308 engineering graduates, including 90 EEs, reported in a survey that those with three or more job changes had an average monthly salary of $2,353 and those with one job change had the highest average, $2,491. From the class of 1974, 347 engineers, including 70 EEs, reported an average monthly salary for job hoppers of $1,579 and for one-time job changers of $1,897.

Computer pioneer John Mauchly dies

John W. Mauchly, co-inventor of Eniac, the first electronic digital computer, died early this month at the age of 72. Mauchly, who received his bachelor's and Ph D. in physics from John Hopkins University, worked with J. Presper Eckert Jr. to complete the design of Eniac at the University of Pennsylvania's Moore School of Engineering in 1946 [*Electronics*, April 1946, p. 308].

Tracor, RCA cooperate on custom SOS

Tracor Inc., Austin, Texas, says it will use custom complementary-MOS-on-sapphire chips from RCA Corp. to enter the market for military and commercial special-application computers. A prototype microcomputer developed for the Air Force and the Navy that uses 29 C-MOS-on-sapphire circuits to emulate the Navy's standard AN/UYK-20 computer is the basis for the move. The company designed the chip set, which includes large-scale integrated 8-bit arithmetic-and-logic and controller circuits, as well as devices laid out from RCA gate arrays of 300- and 452-gate complexities. RCA's Solid State Technology center, Somerville, N. J., turned the designs into chips. Though C-MOS on sapphire has proven too costly for widespread use in commercial applications, officials in Tracor's aerospace group are eyeing the technology for its speed and low power consumption, plus its inherent radiation resistance.

Digital typesetting gets more affordable

Digital typesetting has descended a notch or two on the price scale with the introduction of Autologic Inc.'s APS-Micro 5—a high-speed, cathode-ray-tube based typesetting system. Priced at under $55,000, the unit is Multibus-compatible and uses an 8085 as a controller. Aimed at the mid-range market of small to medium-sized newspapers and the like, it may be used with word processor systems, says the company. The compact typesetter from the Newbury Park, Calif., company has an on-line storage capacity of over 200 fonts and can set up to 1,250 lines per minute with a resolution of up to 3,600 lines per inch. It is available in 45-, 57-, and 70-pica line widths and uses Winchester disks in combination with floppy disks; if the user opts for just floppies, the price goes under $50,000. A patented vacuum transport system is used to move the print medium—either film or paper—eliminating tension and ensuring placement accuracy. The APS-Micro 5 will accept inputs from paper and magnetic tapes, as well as floppy disks.

No. 5

NATIONAL ANTHEM

SEMICONDUCTOR NEWS FROM THE PRACTICAL WIZARDS OF SILICON VALLEY

Doing more with less.

SINGLE-CHIP CRT CONTROLLERS SIMPLIFY DESIGN.

The LM385 12μW power reference

8-bit A/D in 100μsec

High-speed buffer amps drive heavy loads

New low-cost BIFETs in National service

The latest BIFET wizardry unveiled

Free literature/ details inside

Data Acquisition Logic Transistors Hybrids Linear Interface Bubble Memory RAMs/ROMs/PROMs Transducers Displays Custom Circuits Memory Boards Microprocessors Development Systems Microcomputers Modules

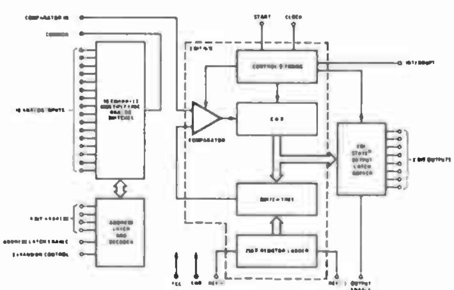
NATIONAL ANTHEM

Showcasing National's new family of 8-bit A/Ds.

A lot of people in the semiconductor industry sell low-cost 8-bit A/D converters. But only National offers self-contained 8-bit A/Ds with 100μsec conversion. And only National can build this kind of performance into A/Ds with single-channel differential or 8- and 16-channel single-ended analog inputs. All of which are fully μP-compatible.

The ADC0801/2/3/4 are 20-pin DIP, single-channel differential analog input A/Ds. The ADC0808/9 8-bit converters also feature 8-channel analog input multiplexers, each in a 28-pin DIP. The top-of-the-line ADC0816/17 each contain a 16-channel analog input mux in 40-pin DIPs.

The new line of 100μsec A/D converters eliminates the need for external zero and full-scale adjustments and features an absolute accuracy as good as ±¼ LSB.



National's 8-bit A/Ds not only interface to any μP bus, they also feature absolute or ratiometric operation, and require just a single 5V supply at almost no current at all.

National Semiconductor, the leader in innovative, cost-effective data acquisition products, now boasts the best price/performance of any A/D available. In 100-piece lots, the ADC0804, for example, costs only \$2.95; the ADC0809 a low \$3.60; the ADC0817 costs just \$7.95.

Practical Wizardry strikes again – all the way down to the bottom line.

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Single-chip CRT controllers need less support.

DP8350 Series of programmable controllers most widely used among major CRT makers.

National's powerful CRT controllers require considerably less support circuitry than any other CRTC available. Due in part to single-chip bipolar circuitry, the DP8350 Series CRTCs serve as fully dedicated CRT display refresh circuits in 40-pin packages.

This, combined with the DP8350's enhanced versatility provides an unprecedented ease of system design.

Single-chip versatility. The DP8350 Series, which includes the DP8350, DP8352 and DP8353 CRTCs, offers a wide range of programmability using internal mask programmable ROMs. In the character field, for example, both the total number of dots per field (up to a 16 x 16 dot matrix) and the number of scan lines per character may be specified. The number of characters per row (from 5 to 110) and character rows per video frame (from 1 to 64) may be programmed as well.

A complete set of video outputs is available including cursor enable, programmable vertical blanking and programmable horizontal and vertical sync.

In addition, the DP8350 CRTCs feature an internal dot rate crystal controlled oscillator. For those systems where a dot rate clock is already provided, the DP8350 Series may use an external clock input. Either way, the buffered dot rate clock output ensures system synchronization.

The DP8350s also provide such system sync and program inputs as 50/60 Hz control, system clear, external character/line rate clock and a character generator program. Also featured are three on-chip registers for external loading of the row starting address, cursor address, and top-of-page address. Twelve bits (4K) of bidirectional TRI-STATE character memory addresses allow interface to character memory.

DP8350 at the heart of the best designs. The popular DP8350 Series has already been designed into the terminals made by nearly every major CRT terminal manufacturer. Because the Wizards at National not only offer superior controllers, they also produce a wide variety of complementary design components. Character generators, μPs, memory products, just to name a few.

And what's more, it's all ready for immediate delivery.

New Military Temperature Range BIFET™ Op Amps inducted into National service.

The inventors of BIFET Op Amps are in the military with the LF151, LF151A, and LF153.

In 1975, National Semiconductor invented BIFET technology. Because of their low bias current and high-speed performance, these op amps quickly became the new industry standards. But while the competition continues to imitate what National introduced, National has moved on.

Their latest offering is three new low-cost, high-performance military temperature range op amps – the LF151, LF151A, and LF153.

A single op amp. A lot of features. The LF151 and LF151A were designed to fill a long-vacant price/performance gap between the LF156H workhorse and the top-of-the-line LF156AH. And both models come with a solid list of guarantees over the −55° to +125°C temp range.

For example, the LF151A comes with a maximum input offset voltage of 2mV and a maximum input offset voltage drift of less than 20 μV/°C. You also get a minimum slew rate of 10V/μ sec and a bandwidth of 3MHz minimum. These parameters are 100% tested, including temperature drift, and are guaranteed with no exceptions, qualifications, asterisks, or footnotes.

Two into one equals a dual. For those who need a dual op amp, there's the LF153, simply two LF151's in the same package. Although National doesn't guarantee a maximum input offset drift spec, they do guarantee that the input offset voltage won't exceed 7mV over the full military temp range. Couple that with low bias current and high speed, and you have a very capable pair of op amps in a single 8-pin package.

The bottom line. Perhaps the most appealing features of these three new op amps, however, are their price and availability. All three models are available now – for as low as $3.25 for the single and $6.00 for the dual (100 unit price). For further information, call your local National distributor or sales engineer.

They'll show you how the people who invented BIFETs just made it easier to own them.

6000V/µsec buffer amps drive heavy loads.

The LH0002, LH0033, and LH0063 have been the industry's most popular buffer amps for some time now, simply because their high-speed special function circuits drive the kind of high-capacitive lines that can choke typical buffers. And to make a great thing even better, National has just assembled two brand new documents full of innovative applications and other detailed information about their buffers. (Check out the Special Functions Databook and Applications Note 227 on the coupon below.)

The LH0002/33/63 current amps will drive up to ±500 mA into a 50Ω line at slew rates from 200 to 6000 V/µsec.

National's laser-trimmed current amps solve design problems with respect to high-capacitive coax line drivers, video amps, high impedance input buffers for fast A/Ds and comparators, and diddle yoke drivers.

The Practical Wizards of the Special Functions Group offer both mil- and commercial-temp versions of the LH0002/33/63s. The LH0002 and LH0033 come in either metal can or dual in-line packages. The LH0063 is available in the 8-lead TO-3 package.

Low-cost commercial temp BIFET™ op amps guarantee lowest drift.

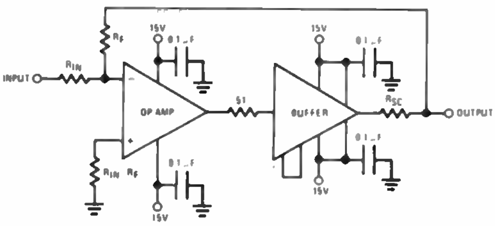
National Semiconductor guarantees the industry's lowest Vos drift with their new line of commercial temp BIFET op amps. With these new low-cost op amps, the need for costly special testing has been eliminated.

The LF351A-1 and LF351B-1 single BIFET and the LF353B-1 dual BIFET op amps require 1.8mA current yet maintain a 4MHz gain bandwidth and a 13V/µsec slew rate. But perhaps of greater significance is their offset voltage drift:

	Max Initial Vos	Max Drift of
LF351A-1	2mV	20µV/°C
LF351B-1	5mV	30µV/°C
LF353B-1	5mV	30µV/°C

These new op amps are ideal for applications such as high-speed integrators, fast D/A converters, and sample-and-hold circuits.

The Wizards, known for their premium mil-temp BIFET op amps, are now setting the pace for high-quality, yet low-cost commercial temp BIFET op amps. Each with a guarantee that can't be beat.



New LM385 12µW micropower reference.

The lowest power reference available.

LM385 Design Features

– operating current of 10µA to 20mA
– 1% and 2% initial tolerance
– low voltage reference – 1.235V
– stable under large capacitive loading
– low temperature coefficient
– low noise, good long-term stability
– 1 dynamic impedance
– replaces older devices with a tighter tolerance

The new LM385 is yet another example of National Semiconductor's commitment to supply high-performance references. Where power is a primary concern (as in battery-powered equipment, portable meters, or general-purpose analog circuitry with battery life approaching shelf life), this device provides performance unmatched by traditional discrete devices.

For applications requiring other reference voltages or performance specifications, National Semiconductor has the device you're looking for. For example:

– Vref 2.5V; 5.0V; 6.9V; 10V
– Initial Tolerance as low as .01%
– TCmax as low as 0.5ppm/°C

Is it any wonder that more and more design engineers are looking to National Semiconductor's linear references to solve problems?

What's new from the National archives?

006 ☐ Special Functions Data Book ($6.00)
007 ☐ Interface Data Book ($6.00)
013 ☐ LF 151, 151A, 153 Data Sheet
014 ☐ New Data Acquisition Products Brochure
017 ☐ LM185/385 Data Sheet
021 ☐ LH0002/33/63 Application Note 227
022 ☐ LF351A-1/351B-1/353A-1 Data Sheet
023 ☐ ADC0801, ADC0808, ADC0816 Data Sheets
024 ☐ DP8350 Series Application Notes 198, 199

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National Semiconductor
The Practical Wizards of Silicon Valley

NA5

between to help out, since it too sees a new market," he says.

Laser communications seem best suited for phone lines in urban and industrial areas where rights of way, permits, conduits, digging, and delays conspire to run costs up. Another example is the Atlanta, Ga., laser link of computer and traffic lights [*Electronics*, Nov. 9, 1978, p. 41].

Uses. In many developing countries, telephone cables are frequently overtaxed or simply nonexistent. A good example of a dedicated link that a line-of-sight laser setup could serve is between airline and travel offices in a city and the local airport, which usually is within the model 736's 15-mile range. Such a link already is in the works for Cairo, Campbell reports.

The American Laser unit has built-in alignment mechanisms, with sighting by a telescope aligned to the optical axis. Power consumption for the receiver is 360 milliwatts, for the transmitter, 2.2 watts—typical figures for such units.

Peak output power for the transmitter is 10 W, with the average 1.5 mW. It has a pulse width of 100 nanoseconds and wavelength of 9,040 angstroms.

Although the Trinidad laser link is handling only teletypewriter data, the equipment can accommodate voice information as well. The only hampering condition is heavy fog, whose suspended water-vapor particles absorb and dissipate the 904-nanometer light. Rain, snow, sleet, hail, and electrical storms have no impact on the line-of-sight system, claims Campbell. **-Larry Waller**

Airborne YAG unit to chart ocean shallows with sonar accuracy but 100 times the speed

The U. S. Navy is eyeing an airborne laser measurement system to replace shipboard sonar setups that map shallows along ocean coastlines. The two techniques are roughly comparable in terms of charting accuracy, but the laser has a great advantage in speed.

Survey boats carrying the sonar systems must proceed slowly and cautiously in uncharted shallows, but a helicopter-borne laser measurement system can scan 100 times faster, covering 7 to 10 nautical miles an hour. Sonar must be in contact with the water to work, and microwaves and millimeter waves will not transmit through water.

Plans. The Hydrographic Airborne Laser Sounder (or HALS) is coming from Avco Everett Research Laboratory Inc., under contract from the Naval Ocean Research and Development Agency. Norda hopes to turn the system over to the Naval Oceanographic Office for worldwide coastal surveys that are scheduled to begin in 1981.

Avco, based in Everett, Mass., is bringing out of the laboratory a solid-state yttrium-aluminum-garnet laser with a frequency doubler converting the YAG crystal's red light into a blue green beam. Such a beam, with a wavelength of 532 nanometers, will penetrate water.

The laser in a HALS system will emit a beam only 5 nm wide, pulsing it 400 times a second to a rotating mirror that reflects each signal down in a circular scanning pattern 700 feet wide. The laser's peak power output during each pulse is 400 megawatts, and its average output is 0.8 watt.

Part of the beam reflects off the water's surface, and the remainder reflects off the ocean floor. A photomultiplier tube, equipped with a specially designed logarithmic amplifier, can distinguish amplitude variations in the returning signals for a 10-million-to-1 range over a 100-megahertz bandwidth, according to Frank J. Cook, Avco's director of engineering.

Accuracy. This wide dynamic range allows quick differentiation of signals and screening out of backscatter. The result is accuracy to within 1 foot to depths of down to 65 feet and to within about 3.5 ft for

100 ft below that distance.

After testing a demonstration unit, Norda concluded that it would come within 1 foot of sonar's accuracy. The agency does note that the laser system's accuracy depends on the clarity of the water.

Counter. To measure water depth, the HALS system has a counter that notes the time lag between the first and second parts of the signal, producing a digitized record for storage on magnetic tape. Measurement of the laser beam's angle as it hits the water fine-tunes the depth figures.

HALS also records the helicopter's position on tape for later correlation with depth measurements during charting. Altitude measurements also will allow surveyors to calculate the water surface's plane for correction of waves up to 5 ft.

Avco has already built a bulky demonstration system using a gas laser, but the HALS with solid-state laser should weigh no more than 880 pounds and be under 2 cubic meters in size, Cook says. It will use a militarized version of Data General's Eclipse S/130 minicomputer for storage and processing, with power drawn from standard helicopter supplies. **-Linda Lowe**

Industrial

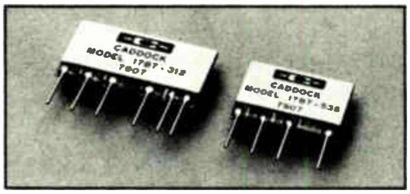
Study forsees lag in U. S. CAD, CAM

Despite the U. S. lead in computer technology, the nation may fall behind West Germany and Japan in using it to develop computer-aided design and manufacturing. That grim forecast is contained in a new 560-page study by the National Academy of Sciences.

The CAD/CAM situation in the U. S. "contrasts sharply with that in West Germany and Japan, which have well-established national research programs with joint industry-government funding," the NAS report notes. Not only is U. S. research falling behind, but the large capital investment required for new technol-

Current sensing resistors for multi-range instruments.

NEW



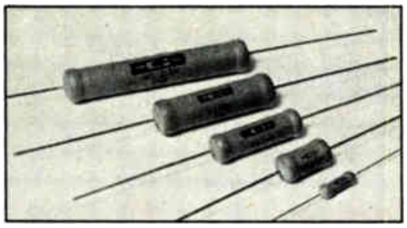
Caddock's Type 1787 Current Shunt Resistor Networks.

Absolute resistance tolerances of 0.25%, 0.1%, 0.05% and 0.02% make these 2-, 3- and 4-decade current shunt resistor networks the ideal replacement for expensive, bulky discrete resistors.

16 standard models are now available. The basic network design provides a series total resistance of 1000 Ω, 100 Ω, 10 Ω and 1 Ω. Other standard models provide commonly used variations of this basic design.

For Type 1787 data, circle Number 201.

Non-inductive precision resistors for power switching circuits.



Caddock's Type MS Power Film Resistors.

Caddock's patented Non-Inductive Design in power ratings from 2 watts to 15 watts assures minimum voltage transients in all types of power switching circuits.

High stability Micronox® resistance films operate to +275°C and years-long load-life tests demonstrate extended-life stability better than 0.05% per 1000 hours.

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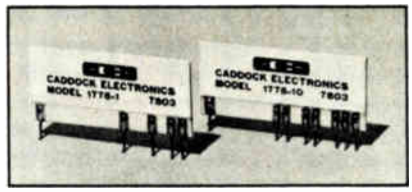
Off-the-shelf precision decade voltage dividers.



Caddock's Type 1776 Precision Decade Resistor Voltage Dividers.

When used as a 10 Megohm input voltage divider, the Type 1776 family can provide high accuracy voltage division in ratios of 10:1, 100:1 and 10,000:1.

Type 1776 Precision Decade Resistor Voltage Dividers are now available in 25 standard models with ratio TCs from 50 ppm/°C to 5 ppm/°C. Caddock's laser production techniques keep OEM quantity prices low, too.

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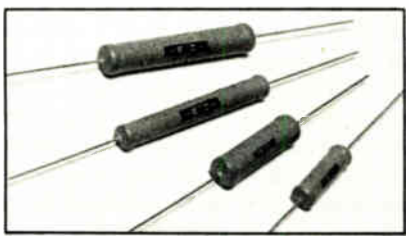
CADDOCK Resistor Technology solving problems across the board!

High stability resistors for very-high voltage control and measurement circuits.



Caddock's Type MG High Voltage Resistors.

High voltage probes and control circuits make wide use of Type MG resistors for precision high voltage regulation and high voltage measurements.

Long-term stability — plus proven reliability — have also made these precision resistors first choice in communications satellite voltage control circuits.

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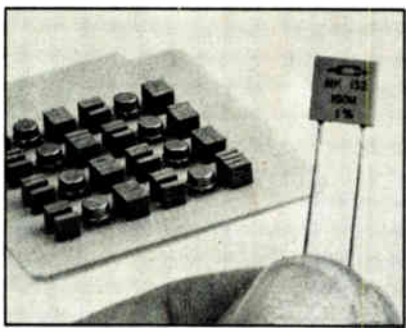
100 Megohms in a miniature package.



Caddock's Type MK Precision Film Resistors.

Precision values to 100 Megohms in a miniature CK 06 case make the Type MK ideal for low current designs.

These non-inductive resistors find wide application in high-impedance analog circuitry.

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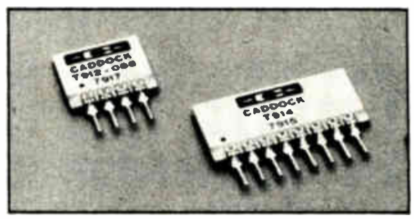
NEW

Resistor pairs and quads with very low ratio TC.



Caddock's Type T912 and T914 Precision Resistor Networks.

Ratio tolerances to ±0.01%, ratio TCs of 2, 5 or 10 ppm/°C and ratio stability within ±0.01% at full load for 2000 hours provide exceptional stability in precision analog circuits.

Both pairs and quads have isolated resistors of equal value. Standard resistance values are 5 kΩ to 1 Megohm and custom variations with unequal values are available.

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Caddock's latest General Catalog provides complete performance data and specifications on over 100 models of these outstanding 'problem-solving' resistors.

For your copy, just write or call to Caddock Electronics, Inc., 3127 Chicago Ave., Riverside, Calif. 92507 — Tel: (714) 683-5361

CADDOCK

HIGH PERFORMANCE FILM RESISTORS

ogy in materials processing inhibits full-scale adoption in the U. S. to the point where "60% of our machine-tool base is more than 10 years old, compared with only 30% in Japan and West Germany," the study says.

U. S. industry needs an economic climate that encourages development and adoption of new technology to improve productivity, the study argues. Such an argument parallels that made by leaders of the electronics industries contemplating the parlous state of U. S. research and development (see p. 81).

Education. Compounding the CAD/CAM problem, says the report, is the low academic status of materials processing technology. "Little current research in the schools is relevant to major developments" in the field, it says.

Moreover, overall engineering and science education trends provide discouraging numbers for American electronics manufacturing hungry for new talent. The study shows an annual decline in the number of engineering and science doctorates awarded since the peak of 14,311 in 1971. Six years after that, the number of Ph. D.s awarded had dropped nearly 18%, to 11,777.

Restructured national priorities in the 1968–78 decade changed Federal agency research budgets and, in turn, those of engineering schools teaching electronics that get much of their support from mission-oriented defense and space programs. During that period Federal funds clearly identified with technology dropped from 54% of the total to 33%.

The report is drawing some criticism because it does concentrate on computers, communications, and energy and materials processing, ignoring many areas outside electronics. But the selection is as much a matter of deadline pressure as of anything else—the NAS study group took on the task of writing the report in midstream as the result of Government economizing. More serious are the complaints of some specialists in areas included in the survey that its contents are uncoordinated history and the product and market forecasts have little depth. -**Ray Connolly**

It's a well known fact that the major semiconductor manufacturers have now copied the SEMIPACK®, the original hybrid power module developed by SEMIKRON. The copy may look-a-like but the similarity ends when you look for performance and price. Why?

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SEMIPACK, the modular building block based on series connected pairs of diodes, thyristors, or one diode and one thyristor, is readily assembled into single and three phase bridges as in half-controlled, fully controlled, diode bridges and ac controllers. Typical applications include: phase and inverter motor controllers; welding, plating and lighting controls; power supplies . . .

For super-fast air freight delivery of our extensive line of power semiconductors (diodes, SCR's, transistors, bridges, SEMIPACKS) from our modern centralized and computerized inventory control system call collect Tel. 1–800–258–1308.

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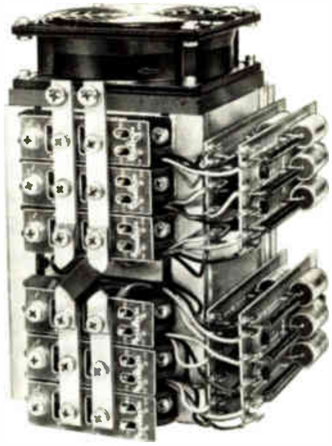

The SEMIPACKS are available as components or integrated in a completed assembly. The unit shown above is a quad drive circuit employing 6 SEMIPACK. Our engineers will design a custom assembly to meet your specific need.

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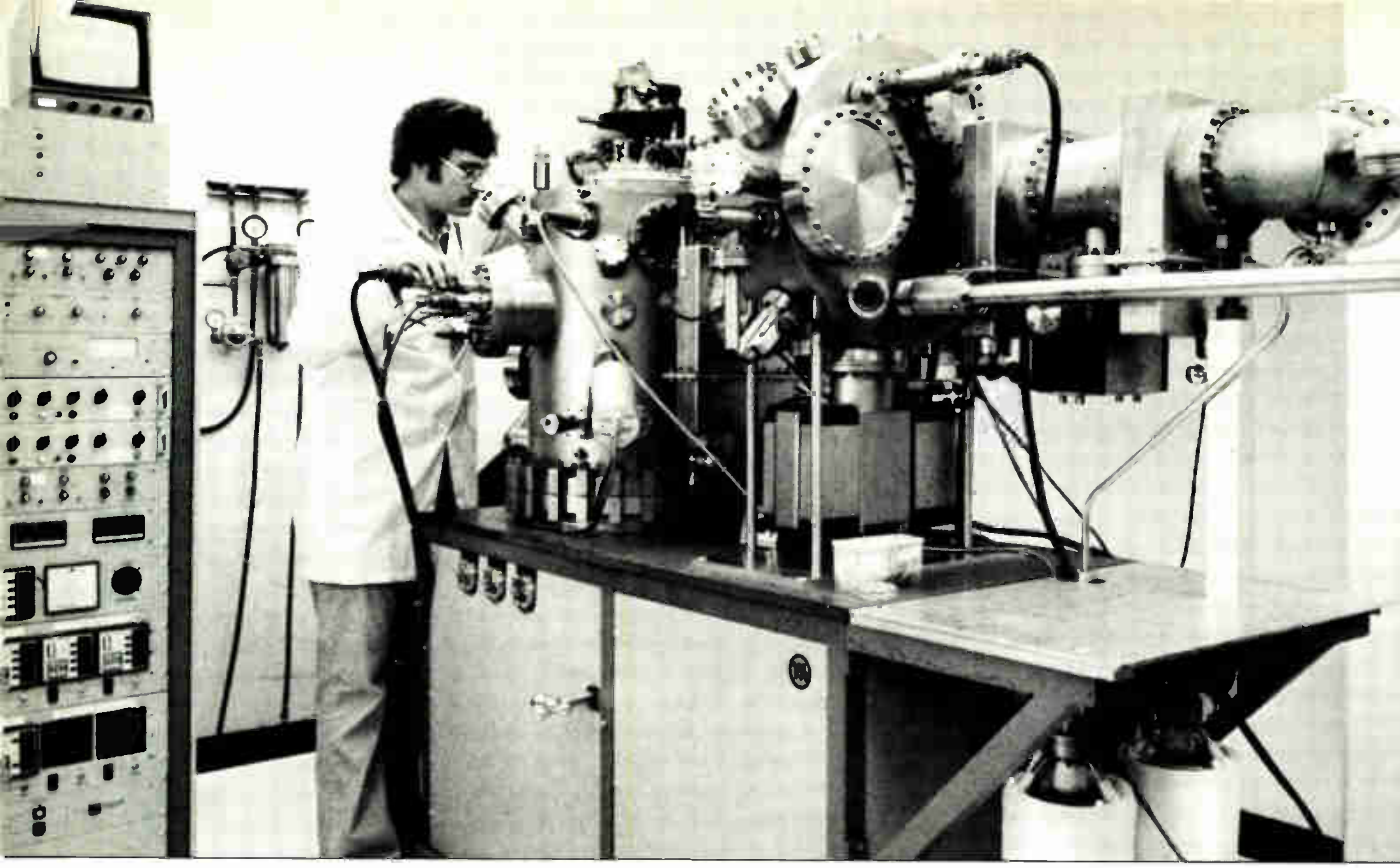
...but not in cutting prices

Circle 53 on reader service card



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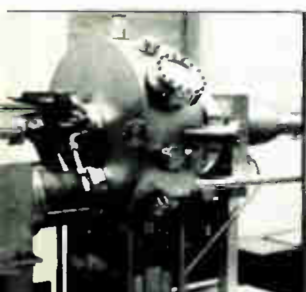
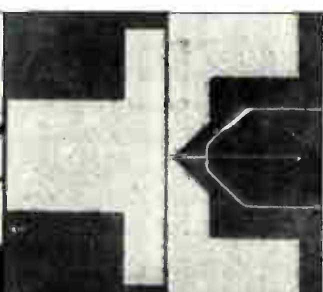
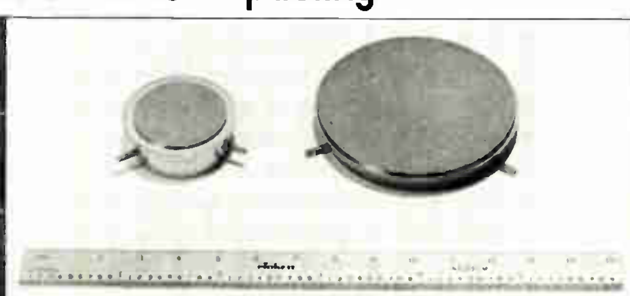


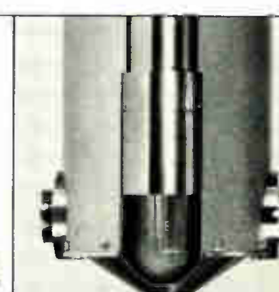
Optional chamber for substrate preparation or analysis simultaneous with growth



8 GHz MESFET grown in Varian process development laboratory.



Systems for MBE growth over one and two inch wafers



Direct measurement of molecular beam flux from each furnace at deposition position

Circle 54 on reader service card

No laws cover possible losses from Soviet trade bar . . .

No Federal laws or rules appear to exist by which the U. S. could compensate American electronics manufacturers and exporters of high-technology products for losses they may incur from revocation of a valid license for exports to the Soviet Union. That is the unofficial judgment of Government lawyers and congressional sources surveyed following a Commerce Department disclosure that it is **looking at the prospect of compensation for losses if any exports are canceled** as a result of President Carter's moratorium on the U. S.-Soviet trade in high-technology as well as agricultural products. When Carter promised farmers to buy and stockpile U. S. grain proposed for export in order to stabilize the domestic market, Federal officials sought a comparable law permitting U. S. manufacturers to be compensated if a license is revoked.

. . . rare-mineral users in U. S. viewed as biggest losers

Shutting the door to U. S. trade in electronics with the Soviet Union "probably will hurt us more than it hurts them," says one Commerce Department specialist, noting that Russia is the second largest supplier of gold after the Union of South Africa. It also is a major source of other rare ores like chrome used by U. S. makers of semiconductors and other high-technology products. "Our relations with South Africa are not particularly good, and gold prices are already out of sight," the analyst noted. "U. S. electronics exports, on the other hand, account for about half the $216 million in high-technology shipments in 1978, our best year in the last five." Moreover, the official points out that **the Soviet Union probably will experience no difficulty acquiring whatever Western electronics products it wants from Europe or Japan.**

NTIA urges competition for digital service proposed by Xerox

The National Telecommunications and Information Administration (NTIA) believes "it is crucial that the Federal Communications Commission seize the opportunity for competition" and quickly allocate 60 MHz in the 10-GHz band to multiple licensees for provision of a digital termination service (DTS) to business users. The service would be based on a 1978 proposal by Xerox Corp. to establish a national service called XTEN, for Xerox Telecommunications Network, using 100 MHz. Under Docket 79-188, the FCC proposed last summer to permit competitive entry into the DTS market with an initial allocation of 60 MHz while holding 30 MHz in reserve [*Electronics*, Aug. 16, 1979, p. 59]. NTIA chief Henry Geller, in supporting the plan this month, urges the FCC to require channel applicants **to provide regional and local DTS service in at least 50 of the top 200 small and medium markets,** as well as national service, and to guarantee that the service be predominantly nonvoice.

First tech standards for telephone hardware issued by EIA

First industrywide technical standards for the telephone equipment industry have been issued by the Electronic Industries Association to meet the needs of manufacturers whose hardware is used with the public network. The RS-464 standard, covering private branch exchange switching equipment for voiceband applications, **will be followed soon by companion standards for key telephone systems, telephones, and auxiliary devices.** The 140-page document is priced at $27.50. Copies are available from the EIA's sales office at 2001 Eye St. N. W., Washington, D. C. 20006.

Washington commentary

The dilemma of technology transfer

The U. S. Treasury and American multinational corporations dealing in high technology face a genuine dilemma when it comes to technology transfer. How can the U. S. continue to earn the necessary foreign exchange to maintain its purchases of energy and other raw materials in the world's markets if the transfer of technology to foreign operations is curbed? The other side of that coin: how can the U. S. successfully maintain its leadership role if the diffusion of its technology abroad continues to strengthen the hand of foreign competitors?

"The one and only solution," says Robert Gilpin, "is to maintain here in the United States a strong commitment to scientific research and technological development. We must maintain a strong lead over both our economic competitors and our military antagonists. The only real and long-term solution to a world in which technological leadership is increasingly transitory is to maintain a healthy climate for innovation at home rather than to seek to close ourselves off from the rest of the world."

Gilpin, who is professor of politics and international affairs at Princeton University, made a strong and favorable impression when he laid his views before the members of the House Science and Technology Committee as it sought to shape a national policy on technology last year. The committee is still at it.

Foreign multinationals expand

American electronics multinationals, meanwhile, are becoming increasingly anxious as their foreign counterparts make the most of the depreciated dollar and the national shortage of venture capital by establishing U. S. plants and acquiring control of smaller innovative U. S. companies. Japan's home entertainment electronics manufacturers have been copying the multinational techniques of their American counterparts and setting up U. S. plants for their own products. The approach of most cash-rich Europeans, on the other hand has been to play technological catch-up: they prefer to buy U. S. component companies whose reserves of technology and talent exceed their economic resources after a decade of inflation.

Moves of this sort appear to trouble the Treasury and organized labor much less than they do the Department of Defense. "How can we complain?" asks one Treasury official. "Foreign operations here pay U. S. taxes and provide jobs for U. S. workers who also pay taxes. Remember that the multinational corporation may have been an American concept but we don't have a patent on it."

On the defensive

This shortsighted economic view worries DOD's top technologists, who see foreign ownership narrowing the list of U. S. electronics companies that can compete for Pentagon R&D contracts. The law requires that contractors be under U. S. control. Moreover, the DOD is troubled by the prospect that potentially useful technology may be transferred abroad and get into hands of potential enemies. "You don't find out about those transfers until it is too late, and proving that something was deliberately leaked is probably impossible," complains one monitor of military electronics. "The rules are unenforceable." (See also p. 26.)

The Defense Department therefore prefers to invoke technology transfer controls at the source—the U. S. manufacturer. If the company is taken over by foreign interests, it cannot contribute to the national defense and it gets no military money—the largest share of Federal R&D funding by far. If it is an American multinational, its positive contribution to the sagging U. S. trade balance can be diminished by tighter controls on exports of production and test equipment and techniques that will keep it competitive in foreign markets.

Professor Gilpin's call for a stronger national R&D effort as the "one and only solution" to this dilemma is perfect, of course, but we live in an imperfect world and cannot rely only on private R&D initiatives that have neither national focus nor coordination.

Toward a positive policy

Congress could begin to correct that if it will provide appropriate incentives to industry in the form of greater tax relief for corporate investment in domestic R&D as well as increased university funds for research and for bringing engineering education at least up to the level of the industries that employ its graduates. These should be the first steps toward developing a national science and technology policy built on positive Federal programs, rather than negative and unenforceable controls. **-Ray Connolly**

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For complete technical data, write for Engineering Bulletin 6250B to: Technical Literature Service, Sprague Electric Company, 35 Marshall Street, North Adams, Mass. 01247.

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3870	✓		✓		✓		✓		✓		✓	
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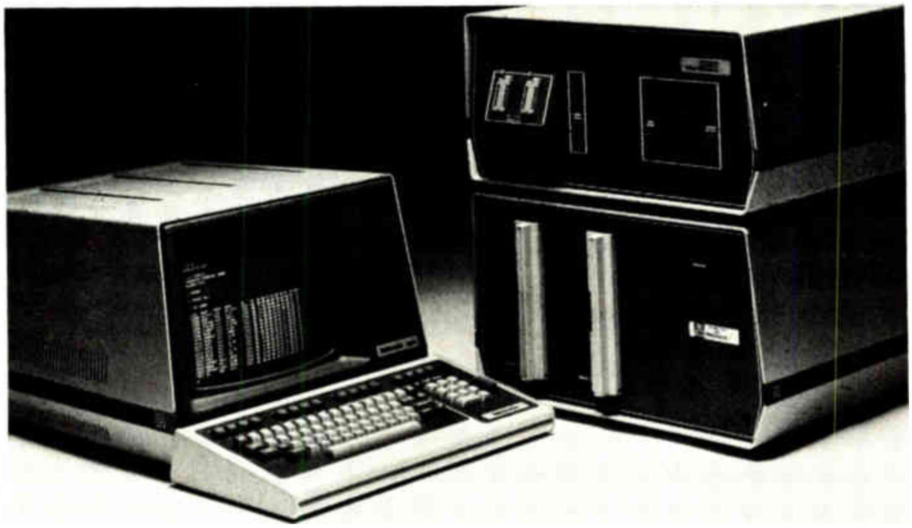

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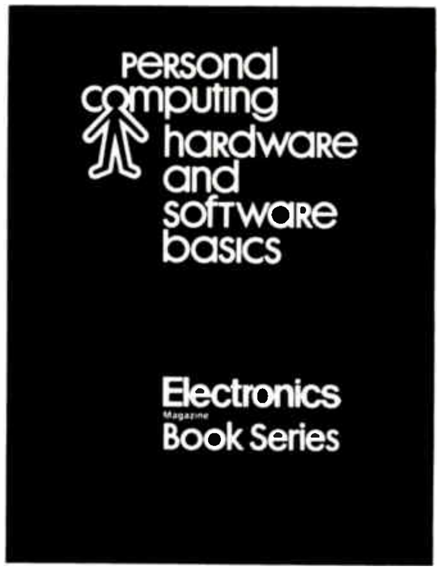

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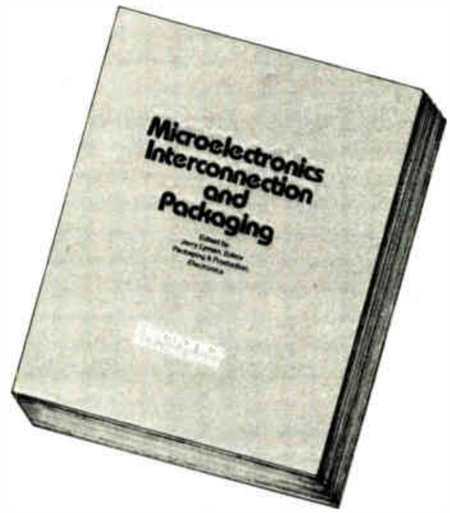

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International newsletter

Japanese make ferrite inductors on single chips

TDK Electronic Co. has started making monolithic ferrite inductors. However, production is limited and the company has no idea when it can begin exports. The device is **made of alternate layers of conductor and dielectric in a manner similar to the one it uses to make multilayer capacitors,** except that the conductor on each layer is patterned to form one turn of a coil. These single turns are then connected to form a continuous multiturn coil. The result is a leadless chip identical in size with the firm's monolithic capacitors. Chips 3.2 mm long by 1.6 mm wide by 0.6 mm high have an inductance of 10 nH to 2.4 μH. Chips 4.8 mm long by 2.4 mm wide by 1.1 mm thick will have an inductance initially of 2.4 to 50 μH, to be increased in the future to a maximum of 220 μH. The devices are limited to applications where their minimum Q of 10 can be tolerated.

Only moderate growth seen for Western European electronics

Growth in West European electronics markets will drop by half this year, Mackintosh Consultants Ltd. reckons. In the 1980 edition of its annual market yearbook, the Luton, Beds., organization **forecasts that the markets will total $63.8 billion, a gain of only 7% over last year,** when they bounded up 14%. Its projections are more sober than *Electronics'* own growth estimate of 11.5% [Jan. 3, p. 126] and well below the 14% growth predicted in August 1979 for Western Europe over the next three years by the U. S. market research outfit Gnostic Concepts Inc., which maintains an outpost in Darmstadt, West Germany.

Japan's 1979 exports of ICs to exceed imports for first time

Worldwide exports of integrated circuits from Japan will exceed imports for the first time in 1979, but such imports from the U. S. still exceeded exports. During the first 11 months of the year, Japan exported $402.7 million worth of devices while importing $381.8 million worth, which should ensure that exports will run in the black for the entire year. **Exports grew 82% over the $224 million in ICs exported for all of 1978,** and imports increased 45% over last year's $262.9 million figure.

Although worldwide IC exports ran $20.9 million in the black for the first 11 months of 1979, **exports to the U. S. were still $133.4 million in the red.** The latter ran to only $154 million, compared with imports of $287.4 million. Comparable figures for 1978 were $74.6 million and $175.5 million.

Electronic trigger for cars' restraining systems developed by Bosch

Anticipating more stringent car passenger safety regulations in the U. S. and Europe during the early 1980s, the West German automobile accessory maker Robert Bosch GmbH is readying an electronic triggering device for occupant-restraint systems such as air bags and seat-belt tighteners. Built around two Bosch-developed integrated circuits, it produces a number of current pulses that, in a crash, trigger and initiate the inflation of the driver's and co-driver's air bags or the tightening of the seat belts. Implemented in a unit about the size of two cigarette packs and now undergoing field tests, the device is claimed to be **both highly reliable functionally and highly foolproof.** It can distinguish an accidental impact with another car or object from a bounce, such as may occur on a bad road, or from hammer blows against the chassis, such as may be encountered during car repair, the Stuttgart firm says. A built-in check circuit monitors the device's reliability and prevents erroneous triggering, and a charged capacitor supplies power should the car's regular supply fail.

International newsletter

Danish firm wins telecomm award from NATO

Christian Rovsing A/S, in Ballerup, outside Copenhagen, will build the hardware to safeguard the North Atlantic Treaty Organization's telecommunications lines. NATO headquarters in Brussels has signed a letter of intent **to buy 12 message-processing centers** for installation throughout the NATO area starting about mid-1981. The order, worth about $27 million, will be followed up by others if NATO's plans are carried out.

Christian Rovsing's CR80 computer, which won out among a field of 50 entries, including ones from IBM and other major computer makers, **was adjudged to be 99.999998% reliable.** It can transmit 1 million instructions per second.

Britain must innovate for its trade to survive, report says

Britain must speed up the introduction of new technology—**possibly by a greater use of licensed foreign technology**—if it is to survive as a trading nation. So says a report from the Advisory Council for Applied Research and Development, a government think tank. Threats to the country's survival come both from faster-innovating developed countries and, in traditional products, from low-wage developing countries. Among specific proposals made in the report, which was sparked by the last government's concern about the social and industrial effect of microprocessors, are a new agency to promote the licensing of foreign technology; greater research in the service sector, allied with an industry-by-industry strategy; government measures to help small firms spend more on research; and fiscal incentives to large firms to seek out or set up spinoff firms capable of exploiting unwanted research. Further underlining Britain's woes, a report out last week from a government committee headed by Sir Montague Finniston makes wide-ranging proposals aimed at correcting the low status and inadequate training and career structure of much of the engineering profession in the United Kingdom.

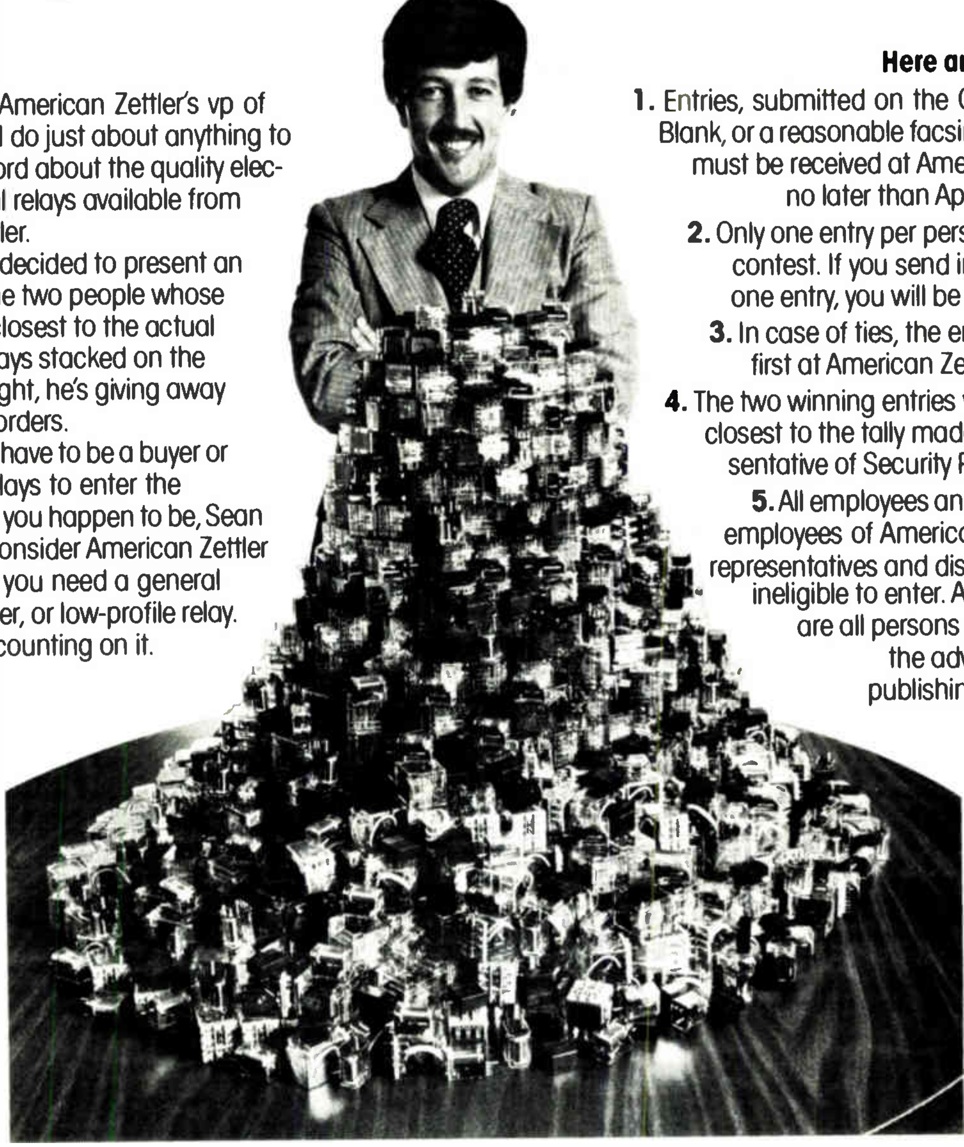
CIT-Alcatel preparing electrochemical low-cost digital fax

Researchers at CIT-Alcatel's Electronic and Energy Applications division are putting the finishing touches on an electrochemical reproduction system for use in a low-cost digital facsimile machine it is developing. Although the Paris-based company will not reveal details of the system, the chemically treated paper is said to react to 0.5 mA at 15 V. Printing time for a single point is 10 ms. CIT-Alcatel believes the new system will prove substantially cheaper than thermal or electrostatic systems because **its low power consumption eliminates the need for complex multiplexing.** The company is discussing with Burroughs Corp.'s Graphic Science Inc. subsidiary the introduction of the machine in the U. S. and is looking into the possibility of a joint venture with a major Japanese manufacturer.

AEG-Telefunken to make thermal-imaging modules for military use

AEG-Telefunken is readying a $60 million production plant for thermal-imaging modules using infrared technologies, which the firm says "are nonexistent outside the United States." **With the approval of the U. S. government and under a technology transfer agreement with Texas Instruments Inc.,** Dallas, the West German company will build detector Dewars and coolers. The modules are intended for infrared sighting equipment like those used on tanks or other armored vehicles. Located at AEG-Telefunken's semiconductor facilities in Heilbronn, the 50,000-ft^2 plant will meet the entire needs of the West German armed forces for such equipment. Eventually, such modules will be made for civilian use, too.

Win an RCA Video Cassette Recorder. Tell Sean how many relays are on the table.



Sean Tierney, American Zettler's vp of marketing, will do just about anything to get out the word about the quality electromechanical relays available from American Zettler.

Now he's decided to present an RCA VCR to the two people whose entry comes closest to the actual number of relays stacked on the table. That's right, he's giving away two video recorders.

You don't have to be a buyer or specifier of relays to enter the contest. But if you happen to be, Sean hopes you'll consider American Zettler the next time you need a general purpose, power, or low-profile relay. Actually, he's counting on it.

Here are the rules.

1. Entries, submitted on the Official Entry Blank, or a reasonable facsimile thereof, must be received at American Zettler no later than April 30, 1980.
2. Only one entry per person for each contest. If you send in more than one entry, you will be disqualified.
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Portable front-line radar detects moving targets fully automatically

by Kevin Smith, London bureau manager

Manpack uses highly efficient InP Gunn oscillator that delivers tens of watts in the 12-to-20-GHz region

Portable radar for front-line troops, on the scene since the mid-1960s, has taken another step forward, thanks to solid-state technology. A mechanically scanned manpack designed to detect moving targets completely automatically on the battlefield in the fogs and mists of a North European winter or during long night watches has been developed by the British government's defense research center, the Royal Signals and Radar Establishment, Malvern, in collaboration with industry.

The system comprises a small antenna and radar head with an indium phosphide microwave power source and a separate control console in which targets within a broad azimuth sector are displayed on a dc electroluminescent plan-position indicator (see photo). The pulsed-doppler techniques adopted, coupled with advanced signal processing, provide automatic target detection and alarm. Targets can be identified by listening to the characteristic noise signature of the doppler-shifted echo.

Getting ready. Marconi Avionics Ltd. was the prime contractor for the system, called Scampi, and Plessey Co.'s Allen Clark Research Centre, Caswell, Northants., developed the needed high-efficiency indium phosphide Gunn-oscillator module. Having undergone field trials by the British army and subsequent design iterations, the equipment is now ready for preproduction contracts.

The program was triggered in the late 1960s by speculative RSRE research on solid-state microwave oscillators. These devices opened the door to a new generation of lightweight, compact radars by providing an alternative to bulky, high-voltage, and power-hungry magnetrons and klystrons.

Gallium arsenide Gunn oscillators developed at the Allen Clark Research Centre under RSRE sponsorship were first used, but indium phosphide devices looked more attractive theoretically because of their excellent negative resistance characteristic, whereby current actually decreases with increasing voltage. As a result, work was begun on such a device capable of delivering tens of watts in the 12-to-20-gigahertz region.

Efficiency. Says George Gibbons, general manager for microwave and optical research at the center, "Efficiencies are better, perhaps by a factor of two, than those of gallium arsenide devices. We've achieved peak efficiencies of 17% under pulsed conditions."

The center is one of a handful of laboratories around the world working with the material. Gibbons hopes to see some spinoff from the program, with devices available commercially in 6 to 12 months, perhaps making them the first of their type to reach the market.

Perfecting the device technology

On display. British radar manpack, in development, features clear, continuous display of all moving targets within a broad azimuth sector. Range and bearing can be displayed digitally.

involved a fine control of the doping profile in the epitaxial material used and optimizing contact metalization using a germanium-gold-nickel sequence. The circuit techniques used to couple the diodes into a cavity-stabilized oscillator operating in the J band were first described at the Ninth European Microwave Conference in Brighton, England, Sept. 17–21.

Unlike an earlier system, explains B. C. Taylor, who heads the program at the RSRE, Scampi has storage to preserve target information from scan to scan. Thus it features a continuous, clear visual display of all moving targets within a broad azimuth sector on a postcard-sized display. What's more, a moving cursor can be placed over any target and the range and bearing are then displayed digitally as well.

In addition, a display option also shows clutter—reflections from points of high reflectivity—as in a conventional radar. A further enhancement could provide overlying map information and extended range information.

France

Payment cards aim to replace personal checks at point of sale

Hand-written personal checks are something of an expensive anachronism in this age of electronic banking. But two Franco-American companies, CII-Honeywell Bull and Schlumberger Ltd., are developing an electronic alternative for point-of-sale use. Their proposed plastic payment cards—the size of a credit card and containing memory and either a microprocessor or logic—would be faster and cheaper than checks, would maintain a running account, and would also offer greater protection against fraud.

A payment card is actually only one of many possible applications. CII-HB foresees using such cards for, say, medical records, billing for computer time-sharing, and electronic security systems.

Apart from the cards, the two companies' basic systems are similar. Each has three additional elements: a programming unit at the bank, where a specific sum is entered into the card's programmable read-only memory; a point-of-sale terminal to carry out transactions; and a retailer's memory card to record sales.

With the systems, a customer would go to his bank and transfer a certain sum from his account to his personal payment card, which would also contain his name, the date of issue, his account number, a serial number, and most importantly, a personal identification number, or code, designed to protect access to the card.

In use. When the customer wanted to make a purchase, he would insert his card into the retailer's point-of-sale terminal and key in his code. The retailer would then record the sale, as on a conventional cash register. The customer would receive a receipt, including, if desired, the balance remaining in his card's memory. The transaction would be recorded on the retailer's memory card, with the data either physically transported to the retailer's bank or transmitted via telephone lines for processing.

CII-HB has opted for a microprocessor-equipped card [*Electronics*, Dec. 2, p. 63]. "Past experience has shown that whenever there was a choice between hardwired circuits and programmable microprocessors, the microprocessors always won out," explains Robert Hervé, manager of applications for the Paris firm's payment card project.

For its working prototype, called the CP8, CII-HB is using two integrated circuits, but intends to put all the circuitry on one MOS chip if it gets an order large enough to cover design costs. Economy is not the only reason: its two-chip payment card measures 1.2 millimeters thick, but the international standard for embossed credit cards is 0.8 mm. "Using a single chip, we will have a standard-sized card," Hervé says.

The microprocessor program prevents any access to the card's memory without the correct code. The principle is the same as in automatic cash cards. The difference is that the payment cards are designed for off-line as well as on-line use and so require much greater security than is offered by the simple magnetic strip employed on cash cards.

Using logic. A simpler and cheaper approach comes from Schlumberger Ltd.'s Flonic subsidiary, in Mountrouge, outside of Paris, which combines several hundred logic gates with a 4-K PROM [*Electronics*, Jan. 3, p. 63]. However, at present, it has only breadboarded versions of its proposed terminal and of the IC for the card.

"What interests us first and foremost is the point-of-sale terminals," says company marketing director Pierre Bouvier, to explain why a firm whose principal activity is in water, gas, and parking meters is now expanding into electronic payment cards. "Measuring money is a logical diversification for us."

Schlumberger's approach rests heavily on a patented card-access protection system developed by Roland Moreno, a French inventor. Moreno's idea is the use of logic circuits to limit access to memory.

Protection. Each card's memory contains a four-, five-, or six-digit identification code. Before any transaction can be made, the correct code must be keyed in to the card. A simple comparator ensures that the code is correct and, if it is, permits input and output access. "About 140 logic gates suffice to create the comparator, a simple arithmetic and logic unit, and the I/O controls," Moreno says.

He conceives a card using TTL gates and 4 K of electrically programmable ROM to ensure a maximum of security. "Once a fuse in an E-PROM has been broken, there is absolutely no way to reconstruct it," he says.

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Although MOS circuits are vulnerable to electrostatic charges, both Schlumberger and CII-HB say they have licked the problem and are also convinced that their MOS memories are fraud-proof. Schlumberger intends to insert a metallic foil as one layer of its laminated card to protect its chip from electrostatic charges; CII-HB uses a metallic ring around the two chips on its card to achieve the same end. **-Kenneth Dreyfack**

Thomson readies radar family for maritime surveillance

Airborne sea-surveillance radars are first and foremost weapons for war, but they also have important peacetime roles like air-sea rescue. In addition, they have become essential for spotting oil slicks and the tankers that cause them, particularly since many maritime nations now consider that their coastal waters extend 200 nautical miles out from shore.

Two ways. The market for these radars consequently has two ways to grow, and Thomson-CSF, France's largest producer of high-technology electronics, is moving in both directions with its Iguane family of radars. By midyear, the company's Avionic Equipment division in Malakoff, on the outskirts of Paris, will be delivering production models to the French navy for the Alizé, an aging carrier-based submarine hunter-killer that is being modernized [*Electronics*, Dec. 20, p. 56].

Upgraded with identification friend or foe (IFF) and discontinuous target tracking, the basic Iguane has also been tapped for the navy's new generation of the Atlantic maritime patrol plane, which is also used by several other European nations. A prototype is scheduled for its first flight within the next six months.

Prototypes of two other members of the family are also scheduled for tryouts this year. One is the Varan, intended originally for the Dassault-Breguet Mystère 20H coastal patrol plane; it can spot oil slicks and also single out targets for over-the-horizon sea-to-sea missiles. The other, the Agrion, can shift from a scanning to guiding air-to-surface missiles fired from helicopters.

All the variants of the Iguane—which means "iguana" and also is the acronym for the full French name, *instrument de guet pour avion naval embarqué*, or "surveillance instrument for embarked naval aircraft"—are put together from a set of five basic building blocks: a transmitter-receiver package, a radio-frequency power module, a servomechanism unit, a control module, and a display. Obviously, the antenna structure has to fit the plane. For the Alizé and the Atlantic, the new radar will drive the existing antenna, but for the Mystère 20H and for helicopters, the company designed new antennas.

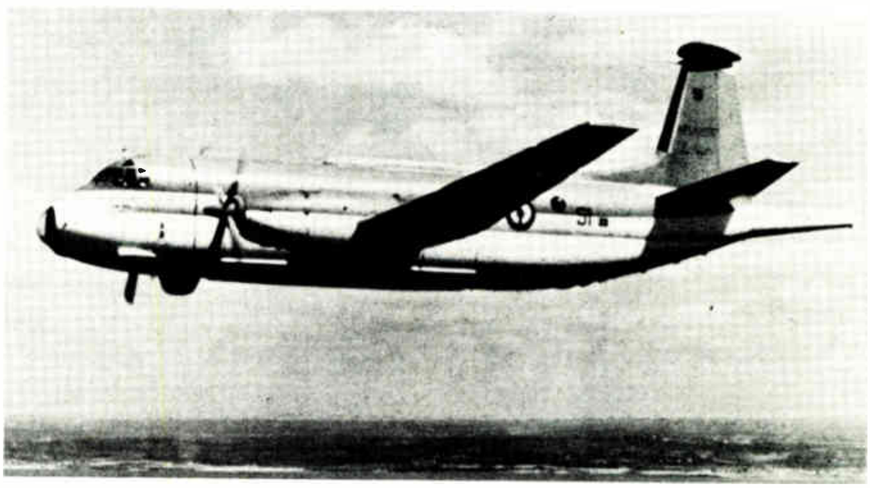
Doubly capable. These X-band radars can spot large ships at ranges up to 150 nautical miles and submarine snorkels in heavy sea at some 25 nautical miles. The double capability stems from a choice of pulse widths. For long-range work, the effective pulse width is several tenths of a microsecond, long enough to wholly illuminate a target several tens of meters long. The duration is slashed to a few nanoseconds to pick up a small target in a rough sea.

Actually, the real pulse length is several tens of microseconds. The transmitted pulses are coded and the echoes processed using the code to compress them in time by a factor of several hundred.

Low power. Because the transmitted pulses are relatively long, the peak power required is relatively low—several kilowatts, instead of the several hundred kilowatts needed for a classic radar having a pulse duration of a few nanoseconds. Iguane's performance, say division officials, matches that of the 500-kW peak-power APS 116 radar found on the U. S. Navy's S3A patrol plane.

The longer-lasting pulses do have a greater chance of being picked up by enemy countermeasure gear, but that drawback is offset by frequency agility, another mark of a modern radar. To pick up the low-power echoes, the Iguane uses a receiver with a field-effect-transistor amplifier that is four times as sensitive as the company's classic receivers.

Iguane also offers optional packages. The Varan, for example, can be fitted with a module that converts its side-looking antenna into a synthetic antenna with a resolution of about 40 by 40 m, good for spotting oil slicks. As the plane flies along, its antenna transmits a narrow beam extending out to about 40 kilometers at right angles to the plane's course. Doppler frequencies of the returns are digitized and processed to obtain resolution over the wide swath of sea



Airborne. The French navy's Atlantic patrol plane is equipped with Thomson-CSF's Iguane sea-surveillance radar. The radar is being improved for an updated version of the aircraft.

swept as the plane advances that with conventional processing would require an antenna several hundred meters long.

Another option converts the basic Iguane into the search and missile-control version, Agrion. Built to control the all-weather air-to-surface missile AS 15 TT developed by SNIAS (Société Nationale Industrielle Aérospatiale), Agrion scans a full 360° when it searches. When the operator switches to missile guidance, the radar locks on the target and codes bearing and range commands for the missile into its transmission. To keep the target and missile echoes distinct, the missile retransmits the radar signal back to the radar. The missile develops its own altitude-control inputs through an altimeter. **-Arthur Erikson**

Italy

Three-chip precision positioning system offers high accuracy, 100-W motor drive

Usually, the designer of a precision positioning system for an office machine or like-sized hardware winds up with a fairly complex circuit and a heavily populated circuit board. Some simplification is possible by using a stepping motor, which takes on a precise angular position each time it is pulsed. But stepping motors generally are too slow for applications like high-speed impact printers, where print wheels must be stopped at the right spot every 30 milliseconds or so. Consequently, the choice usually goes to a fast-accelerating dc motor paired with highly accurate servo control.

This choice will be easier for designers to make from now on, maintains SGS-ATES Componenti Elettronici SpA, the largest Italian semiconductor house. The company, based in Agrate, outside of Milan, has gone to market with a set of three monolithic chips that carry all the linear circuitry needed for a high-accuracy positioning system [*Electronics*, Jan. 3, p. 64]. One chip, the L290, generates a tachometer voltage; the second, the L291, serves as a digital-to-analog converter and a position amplifier; and the third, the L292, powers the motor. Together with a microprocessor and an optical encoder, they make a complete positioning system.

Useful. Actually, the chip set was developed for Olivetti for an electronic typewriter. But SGS-ATES figures there will be many other applications for the chips, and now that Olivetti's exclusive rights have run out, it has put them on the market. The initial price is $6.50 for the set in quantities of 100,000 and up.

The kingpin chip in the trio is the L292 motor-drive circuit. It contains, on a slab of silicon 160 by 120 mils, a complete switched-mode power amplifier. The power-handling capabilities, designed to drive the motor windings in an H-bridge configuration, are eye-opening—100 watts. That works out to an efficiency of 80%, the firm points out.

To drive its output stages, the L292 generates a pulse-width-modulated dc signal. To do that, it converts a bipolar input signal into a unidirectional one (from 0 to +20 volts) and compares it with a motor-current feedback signal in a local-error amplifier. This error signal, together with a triangular waveform generated on chip, is fed to a comparator. The resulting PWM signal drives the output stage.

Because it has an H-bridge configuration—two legs across the power supply, each having a pair of switching transistors, with the motor windings connected between the center points of the legs—the chip has commutation delay circuits that make sure that transistors in the same leg of the bridge are not conducting simultaneously. This delay can be programmed externally, as can the on-chip oscillator frequency and the overall gain.

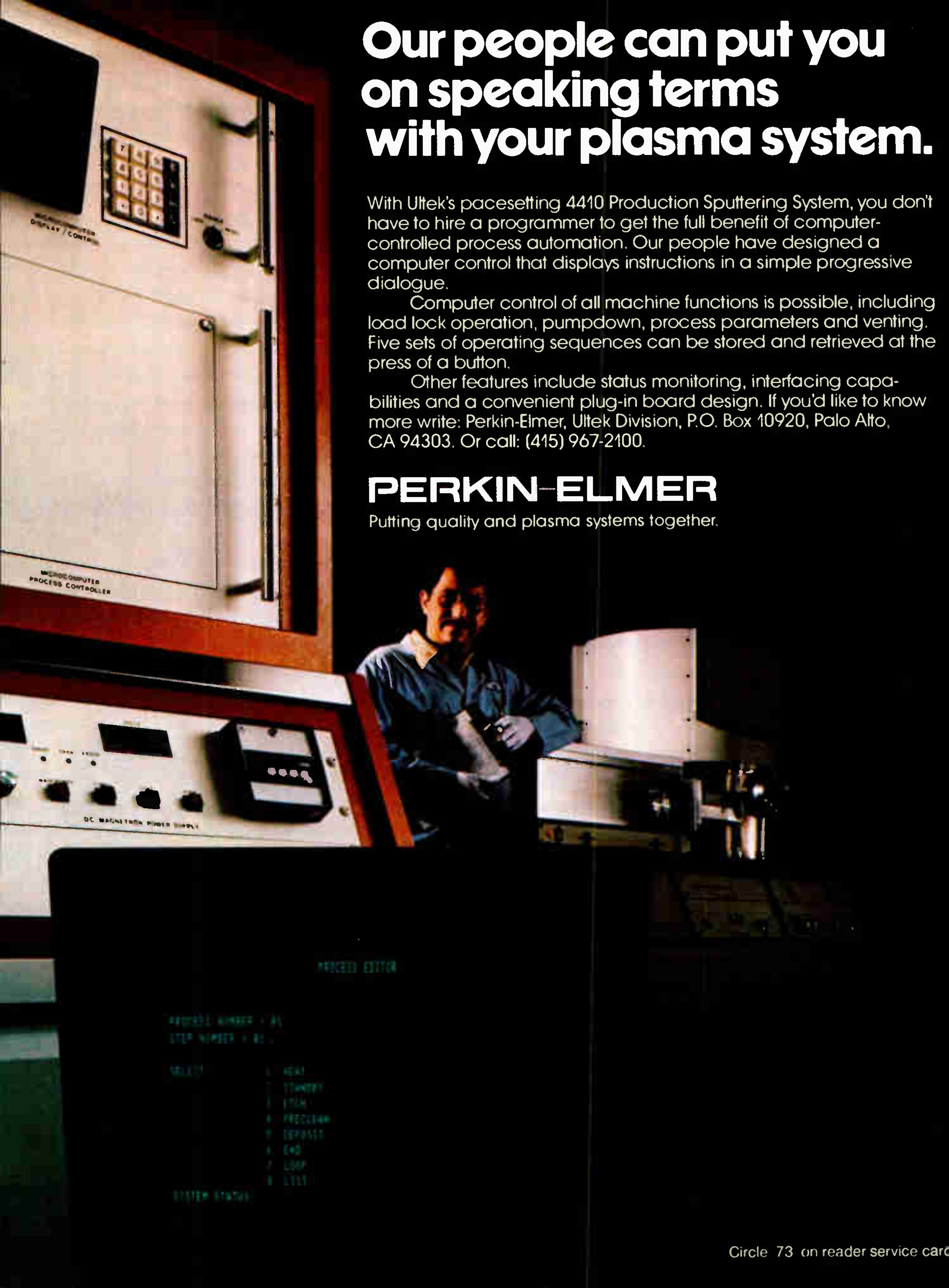
Speed commands for the system originate in the microprocessor. It is continuously updated on the motor position by means of pulses from the L290 tachometer chip, which in turn gets its information from the optical encoder. From this basic input, the microprocessor computes 5-bit control words that instruct the system to speed the motor up, brake it, or hold it constant.

The L291 turns the 5-bit words into the bidirectional signal that is fed to the drive chip by converting the digital command to an analog voltage and comparing that with an internal reference from the L290; this process makes the system self-compensating for variations in input levels, temperature changes, and aging. The comparator output level depends on the speed demanded, and its polarity is indicated by a sign bit in the control word.

The L291 also takes over as a position-signal amplifier when the microprocessor instructs it to, using the zero-crossing point of a sine wave generated by the optical encoder as the target point. In addition, it carries the overall loop-error amplifier for the system and its main summing junction.

Startup. When the motor is stopped and the microprocessor orders it to a new position, the system operates in an open-loop configuration at the outset because there is no feedback from the tachometer generator. Maximum current is fed to the motor, and as it reaches maximum speed, the pulses from the tachometer chip cause the microprocessor to cut the demand signal. The motor continues to run at top speed but under closed-loop control.

As the target position is approached, the microprocessor lowers the value of the speed-demand word; this reduces the voltage at the main summing point, in effect braking the motor. The braking is applied progressively until the motor is running at minimum speed. At that time, the microprocessor orders a switch to the position mode, and within 3 to 4 ms, the L291 drives the motor to a null position, where it is held by electronic detenting. **-A. E.**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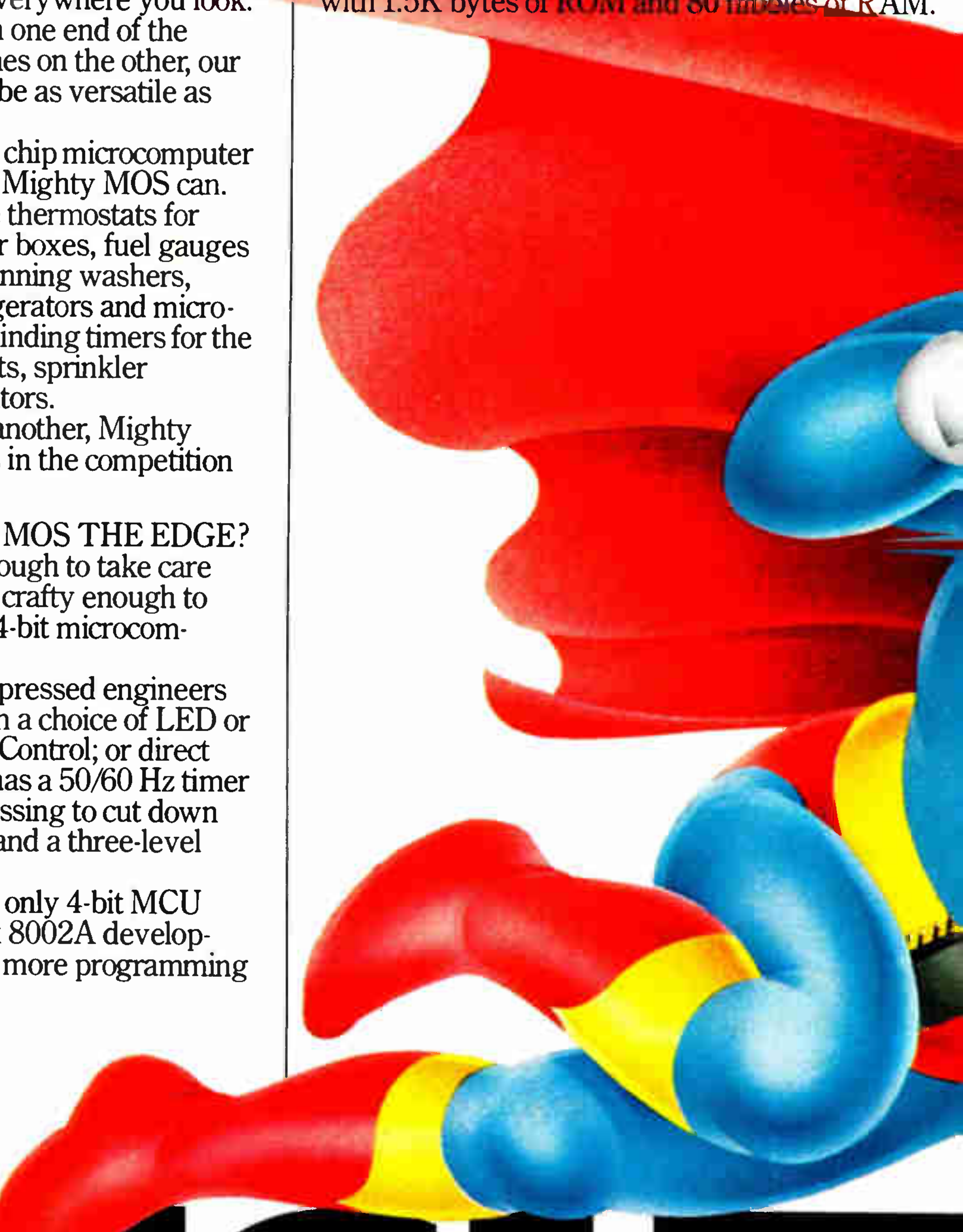
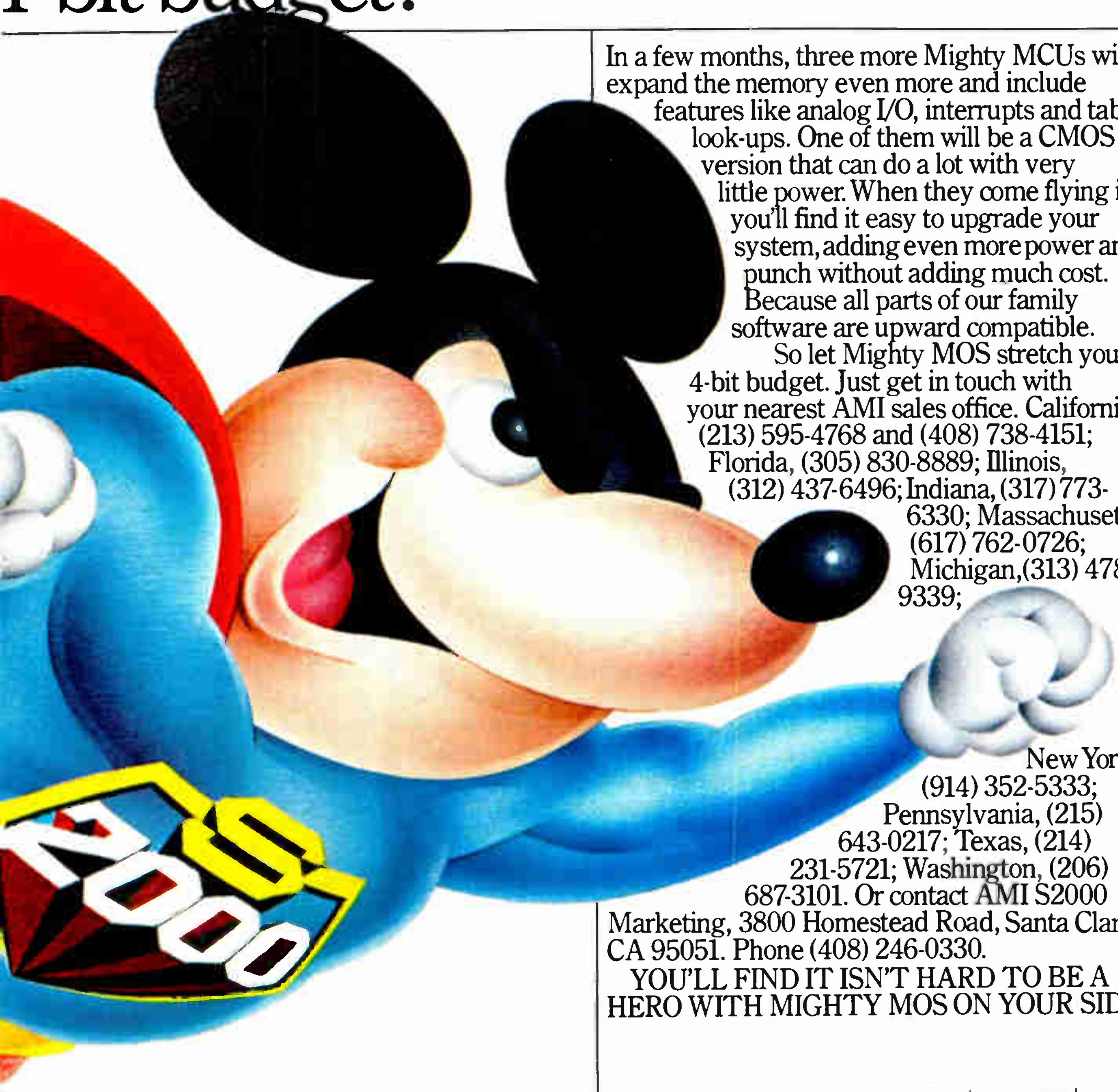


MIGHT

4-bit budget?



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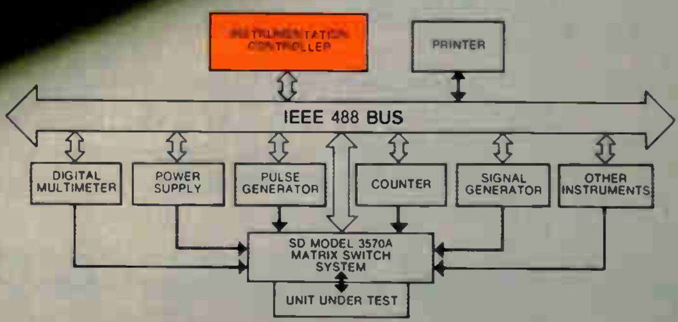

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Here is a representative but by no means complete sampling of bus compatible Systron-Donner instruments. Let us know what your exact requirements are. Contact Scientific Devices or Systron-Donner, 2727 Systron Drive, Concord, CA 94518, U.S.A.; phone: (415) 676-5000.

Frequency Counters. S-D's wide selection of IEEE-488 compatible counters ranges from 100 MHz all the way to 26 GHz. Model 6043A shown here is one of several thin-line designs with bus interface standard. This 1,250 MHz counter is ideal for communications work and other frequency measurement applications. Note front panel lights that tell the operator the status of the instrument while it's active in the system.

Signal Generators. One of S-D's most popular signal generators is the Model 1702 which provides a range of 100 Hz to 999.999 MHz in a single range with 100 Hz resolution. It's fully programmable on the IEEE-488 bus. For microwave frequency applications, Models 1618 and 1626 extend coverage to 18 and 26 GHz respectively.

Digital Multimeters. Systron-Donner's 4½ and 5½ digit multimeters for systems use include the Thin Line Model 7344A pictured here. This 4½ digit autoranging DVM includes the bus interface, DC volts, resistance, true RMS as standard. In the 5½ digit category, consider Model 7115 with microprocessor control, auto-calibration, and automatic fault detection and isolation.

Pulse Generators. Model 154-4 is an automatic pulse generator which is fully programmable with its IEEE-488 interface and the Model 3520 Controller. Model 154-4 provides a repetition rate of 10 Hz to 50 MHz, pulse delay and width from 10 ns to 10 ms, and outputs of 0.5 to 10 V within a −10 to +10 volt window. An exceptionally versatile instrument for the systems user.

Systems Power Supplies. Systron-Donner's P series of power supplies receives its bus commands via the S-D Programmer module shown here. Controls up to 6 supplies. One DAC board controls V, I, and V limit. Modular flexibility allows anywhere from 50 to 500 watts.

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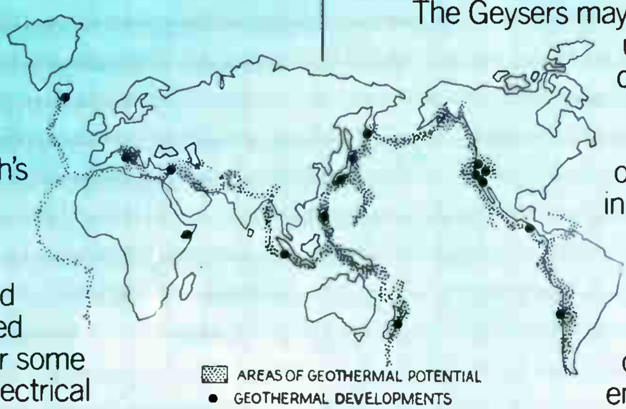
MOTOROLA HELPS GET ENERGY FROM

In northern California, the natural heat of the earth is being harnessed to serve the energy needs of man. Natural steam, heated by the molten rock below the earth's crust, is being tapped, extracted and piped to power some of the electrical generators that help light up San Francisco, 90 miles to the south.



The place is called The Geysers, and it's part of a pioneering effort by Union Oil Company of California to make geothermal energy a practical alternative to expensive imported oil.

The Geysers may be an unorthodox power source, but it has one thing in common with every other branch of the energy industries: the need to maintain good, reliable communications, no matter how remote or primitive the site.

At The Geysers, as in many places around the world, the solution to that problem is Motorola communications.

ELECTRONIC PROBLEM-SOLVING.

One problem at The Geysers, for instance, was the rolling terrain and steep, narrow canyons, among which conventional high-frequency radio signals could get diffused and lost. Motorola solved that one with ingenious simplicity: a low-band two-way radio system that, as one engineer put it, "gets into the nooks and crannies."

ELECTRONICS EVERYWHERE.

But this is merely the tip of the iceberg of Motorola's experience in energy-industry communications.

One of America's largest oil refineries has 35 Motorola

R&D is a shrinking resource

Percentage of GNP and of sales and profits invested in R&D is going down as inflation also cuts into figure

by James B. Brinton, Boston bureau manager

China was the most sophisticated society in the world until the Ming Dynasty effectively outlawed innovation. History can repeat itself.—Charles A. Zraket, executive vice president, Mitre Corp., Bedford, Mass.

The electronics industries in the United States, and industry in general, are spending less each year on research and development. And it is becoming increasingly clear that basic changes in Federal tax policy and patent law will be necessary to reverse the trend.

What is ironic with respect to electronics R&D is that in a period of economic decline, the fastest-growing, most productive industries are the ones that invest most heavily in research and development. While most industry executives would like to see the U. S. spend more on R&D, there is a question whether even technology-intensive industries are spending enough.

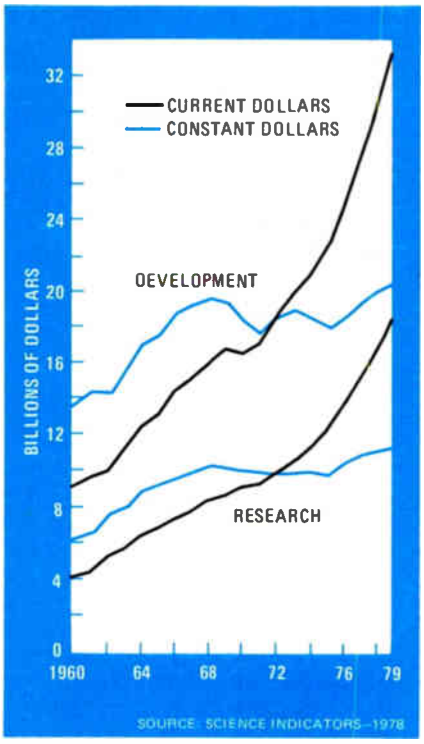
Looking only at dollars can lead to misinterpretation. According to Business Week magazine, 683 major U. S. firms spent about $20.5 billion on R&D in 1978. That's up about 16.4% from 1977, which itself saw a similar percentage gain over 1976.

Complications. But it's not that simple. For one thing, in generating its figures, Business Week added 59 firms to the 624 reviewed in 1977. For another, it noted that R&D outlays as a percentage of sales stagnated at about 1.6% for all industries, while R&D funding as a percentage of profit fell by about 0.6%.

During the same brief period, the nation's Gross National Product rose about 12% and inflation robbed the dollar of at least 7.4% of its purchasing power. Thus the percentage of GNP invested in industrial R&D as a percentage of either sales or profits dropped between 1977 and 1978. And though gross dollar amounts rose, inflation and rising costs disemboweled these investments.

Richard T. Knock, assistant executive director for advanced development at the Stanford Research Institute, Palo Alto, Calif., is blunt: "We are living in the past. This country is underinvesting in R&D and losing its edge."

Straight talk. Since 1968, not only have more R&D dollars been spent for development than for research, but total spending in constant dollars has been essentially flat.



William C. Hittinger, executive vice president for research and engineering at RCA Corp., New York, agrees that the U. S. is not putting enough of its Gross National Product into research. And he warns that the U. S. is being challenged by other countries. "Ideas are mobile" and "we're no longer alone" in world markets, he says.

Even though the nation's R&D investment is growing in current dollars, GNP and inflation also are growing fast. Many executives, like Knock and Hittinger, would like to see R&D investment at least keep pace with GNP and grow in constant dollars. Without such growth, most see a continuing decline in the nation's competitive position and economic health.

Government lags. Data on U. S. government-funded R&D is no more cheerful. During the same 1977–78 period, the Federal government increased its outlays from $23.93 billion to $26.42 billion. That comes to $2.49 billion in current dollars but only $305 million in constant 1967 dollars, according to the National Science Foundation. The NSF's estimates for 1979 look even worse despite an increase in Federal outlays to $27.97 billion—a $1.55 billion paper increase that results in a constant 1967 dollar decrease of $544 million.

Federal R&D expenditures are down for the decade in constant 1967 dollars. Although they increased from $15.64 billion in 1969 to $27.97 billion in 1979, in constant dollars the actual investment was $14.69 billion in 1969 and $12.08 billion in 1979, a decline of almost one fifth—and the 1979 estimate is based on an optimistic deflator derived in May 1979; the actual drop is probably larger.

The decline in R&D funding—whether in terms of percentage of GNP or in constant dollars—worries observers such as Guy Fougere, vice president of Arthur D. Little Inc., Cambridge, Mass. He sees Japan and other countries spending ever larger percentages of GNP on R&D at the same time that the share in this country continues to dwindle. "Over a span of years, this sort of trend compounds itself," he says. Coupled with Japan's accelerating productivity, it could make the U. S. a "second-rate technological power before the end of the century." Fougere also considers West Germany a strong technological competitor and dislikes the idea of facing such countries in a contest for world and domestic markets in the 1990s.

Automation key. SRI's Knock also respects Japan and West Germany. He cites industrial automation as one index of their R&D efforts. "SRI rates Japan most advanced in this area, West Germany as second, and the U. S. as third," he says. Japan, he points out, "already has two fully automated factories," whereas in the U. S. there is none. West Germany has assembled a robotics effort that combines universities, trade groups, and companies. "Mercedes, for example, already has a full assembly line worked by intelligent robots," he notes. Meanwhile, General Motors' much touted robots perform spot welding and are being groomed for continuous welding jobs.

Robotics is of interest to any country planning to compete in the world's markets—according to Knock, it is a $250 billion market for the remainder of the century—and the U. S. is behind.

The gap in technical sophistication, if not already closed as in the case of robotics, is closing, according to George H. Heilmeier, vice president for corporate research at Texas Instruments Inc., Dallas. He is not sure the gaps will close completely, because of what he sees as the country's tradition of innovation. But, he says, "foreign countries will become

Does the U. S. have a problem?

Critics of research and development policy in this country point to a variety of indicators they say are declining because funds are being routed away from R&D. Among them are balance of trade, productivity, the number of patents issued to Americans versus the number issued to foreign citizens, the number of foreign patents acquired by the U.S., and the number of technical papers published by Americans.

Balance of trade. According to National Science Board (NSB) figures, the United States has good luck selling R&D-intensive products abroad. From 1960 through 1975, such goods sold well, and the nation sold more than it bought, reaching a peak positive balance in 1975 of about $29.3 billion. Since then there has been a slump, with 1977's balance only about $27.6 billion. Still, that is better than trade in all manufactured goods. In 1977, the nation paid out $26.5 billion more than it took in. During the same 17-year period, there has been a deceleration in sales of non-R&D-intensive goods. The deficit grew from $179 million in 1960 to 1977's $24.4 billion.

The board blames the post-1975 trade-balance decline in R&D-intensive goods on a major influx of Japanese consumer electronic goods, plus the drop in value of the dollar versus the yen and West European currencies.

The trade-balance situation becomes even clearer when only R&D-intensive goods are examined. Sales of U. S. R&D-intensive goods begin to droop in the mid-1970s almost regardless of the country traded with. Throughout the decade, the United States has almost maintained parity with West Germany. But the U. S. trade balance with Japan has gone from minus $133 million in 1966 to minus $3.5 billion in 1977. And the balance of technology-intensive exports even to developing nations has been approximately flat at about $16 billion since 1976. So with respect to Japan and West Germany, the United States is already a net importer of R&D-intensive goods, a situation that worries industry observers.

Productivity. Figures on productivity also are gloomy. The board reports that whereas most other countries have generally increased the rate of growth of their productivity over the past decade, the growth rate in the United States has slowed by comparison. Both the National Research Council and Comptroller General Elmer B. Staats suggest that the slowdown may be due partly to "a waning U. S. ability to innovate." U. S. Department of Labor figures show that between 1967 and 1977, Japan's productivity grew by 99.2%, France's by 72.6%, West Germany's by 69.6%, Canada's by 46.1% and the United Kingdom's by 26.3%. By comparison, that of the United States grew only 26.1%. And far from just slowing its rate of advance, by 1979 U. S. productivity had scored an absolute drop in the first half of the year, declining at an annual rate of 5.7%, according to Congress's Joint Economic Committee.

Admittedly, Japan's 1977 productivity was still only about two thirds that of the United States, according to the Department of Labor. Still, the trend is an uncomfortable one, and it is an argument many use to justify increased R&D expenditures.

Patents. According to the NSB, researchers find a strong correlation between a company's R&D activities and the number of patents it acquires and between the number of patents on capital goods products and value added in an industry. By this yardstick, patents mean corporate growth and increased productivity. Patents also are said to be a good index of technological change. Annual patenting activities and sales growth appear strongly related in high-technology industries and weakly related in low-technology industries, according to the American Economic Review, making patents an even greater growth indicator. Patents also seem to grow in number as an industry grows and then to taper off as industry matures or declines.

Thus it is worrisome to many that while U. S. inventors are generating fewer, overseas inventors are getting more U. S. patents. U. S. patenting activity peaked in 1971 with 55,979 patents issued to Americans. Since then the falloff has been rapid, with only 41,452 patents issued in 1977. Meanwhile, patents issued to foreign inventors have climbed from 7,698 in 1960 to 23,766 in 1977, according to figures from the Office of Technology Assessment and Forecast and the U. S. Patent Office. In 1960, 83.7% of U. S. patents went to U. S. citizens or corporations and 16.3% to foreign inventors; in 1977 the proportions were 63.6% and 36.4%, respectively.

Perhaps just as worrying, U. S. patent activity as a whole, without regard to nationality of inventor, has been dropping since 1971 from its peak of 78,320 to 1977's 65,218 U. S. patents. Finally, with overseas markets of acknowledged importance to U. S. exports, even the number of patents applied for overseas by U. S. citizens or firms is falling steadily, while filings from other countries are holding about level. From 49,098 foreign patents secured by the U. S. in 1966, the curve rose slightly to peak at 50,852 in 1969, then slumped rapidly to its 1976 level of 34,796. Though other countries were granted fewer foreign patents, their yearly numbers were about constant over the decade, except for Canada's which declined somewhat.

Of the various indicators, patents may be the least reliable. There is some tendency in industry to depend on "trade secret" protection rather than patents these days—if only to keep proprietary information out of the hands of the National Technology Information Service (NTIS) and thus away from competitors here and abroad. Also, a patent granted may not be a patent brought to market; in the case of government-financed R&D, for example, the NSB estimates that only 7% to 13% of such patents make it into commercial use. By contrast, the rate for patents growing out of industrial R&D is about 50%.

Technical papers. According to the science board, the early 1970s constant-dollar declines in research spending have caused a two- to four-year lag between the performance of research and its publication. In addition, from 1973 to 1977, all fields of research except for clinical medicine and biomedicine saw a falling number of publications ranging from 5% to 25%, with physics down 6%, engineering and technology down 16%, and mathematics off 25%.

There are other indicators mentioned in this context as well, such as the decreasing number of new companies formed in the past 10 years, compared with the 1960s. But balance of trade, productivity, patents, and technical publication seem more directly associated with R&D spending. Though it may be fair to question the validity of any one of these indicators, it would be unseemly to ignore the fact that all of them point downward and that the decline approximately coincides with the point at which national research and development funding changed from growth in constant dollars to a pattern of limited growth and sometime decline.

In constant dollars, the United States as a whole is spending only a little more on R&D now than in 1968. National Science Foundation (NSF) figures show the country budgeted about $19.581 billion for development in 1968; this fell to about $17.887 billion by 1971, rose slightly to $18.961 in 1973, fell off to $17.873 in 1975, and in 1979 rose to an estimated $20.418 billion. That's only about 4.27%, or $837 million more than in 1968.

The constant-dollar story for basic research is similar, but written in smaller figures. Again funding peaked in 1968 at $10.21 billion and then began an almost linear decline to $9.811 billion in 1975, rising again to an estimated $11.354 billion in 1979, a decade's increase of only 11.1%.

In contrast with these fairly level years of R&D spending after 1968, the period from 1960 to 1968 was one of rapid growth—and the indicators now in decline were rising during that period and continued to do so for several years afterward. Funding for development rose from $13.552 billion in 1960 to $19.581 billion in 1968, an increase of about 44.5%. During the same period, research funding rose from $6.141 billion to $10.217 billion, for a constant-dollar increase of about 66.4% in the eight-year period.

Critics of R&D funding in general, and the space program in particular, often blame the fall in R&D funding growth to the peaking of the space program. However, space funding peaked in 1965 at 34% of Federal R&D obligations, according to the NSF; that is three years before the malaise in national R&D funding set in.

Even though these indicators are susceptible to varied interpretation, even a cautious evaluation would be that the U. S. does in fact have an R&D funding problem. And though the nation may not have to match foreign competition dollar for dollar, it may well need to spend more than it is now.

far more competitive in world markets than they are today in high-technology products. I don't like the way the vectors are pointing. We're sure trying hard as a nation to shoot ourselves in the foot."

For N. Bruce Hannay, vice president for research and patents at Bell Laboratories in Murray Hill, N. J., the U. S. and Japan are now on a competitive level, with "European countries at this time a distant third and not yet a force equal to the other two."

Against a background like this, few executives, especially in high-technology industries like electronics, need to be convinced that R&D is a good investment.

Spending vital. R&D spending is crucial to corporate survival, according to John F. Mitchell, assistant chief operating officer of Motorola Inc., Schaumburg, Ill. R&D spending means higher growth and profitability, he says, noting that the reverse is also true.

John P. Stenbit, manager of requirements and group development at TRW Defense and Space Systems, Redondo Beach, Calif., says baldly, "We would die in an instant if we did not continue to invest." He adds that TRW's management unquestioningly supports the company's high rate of R&D investment—typically 10% to 15% of yearly sales.

Still, R&D investments, even in the high-technology sector, are large only by comparison with the national average and may be low compared with national needs. According to data from Standard & Poor's, high-technology R&D broke down this way in 1978, with the middle column showing percent of sales and the right one percent of profits:

National average	1.9	43.4
High-technology average	4.0	65.4
Aerospace	3.7	93.0
Electronics (general)	2.6	56.1
Data processing	6.0	54.8
Instruments	3.9	69.9
Semiconductor	5.8	102.3
Telecommunications	1.9	16.1

Except for some data-processing and semiconductor firms, the often-

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mentioned 10%-of-sales investments in R&D appear to be the exception rather than the rule. Yet there is a large body of data showing that investments in R&D boost both sales and productivity ("R&D helps fuel growth," p. 86) and thus contribute to national economic health, perhaps tempering inflation and aiding the country's balance of payments.

In the opinion of Sen. Adlai E. Stevenson (D., Ill.), "Development of new products, services, and industrial processes based on advances in knowledge [have] contributed more than anything else to our nation's productivity, growth, its trade performance, increases in wages, and stable prices." Stevenson made the remarks during a recent symposium on innovation at Massachusetts Institute of Technology.

Innovation index. Yet R&D in real terms has been declining throughout the 1970s. Only recently, with the nation verging on recession, have large numbers of industry observers begun wondering aloud about the pace of innovation. Implicit in their remarks are questions about R&D funding, for though R&D and innovation are different, dollars spent on R&D are an index of a nation's intent to innovate.

With R&D a fashionable concern, there is the usual difference of opinion. Historian of technology David F. Noble of MIT has been quoted as arguing that today's concern with lagging technical innovation is just industry's way of getting taxes reduced. But Harvard University economist Dale W. Jorgenson, on the other hand, feels that the key to improved technology is enhanced capital formation, and his view is widely shared in industry.

Jeffrey C. Kalb, engineering vice president of Data General Inc., Westboro, Mass., notes that with interest rates high and with pressures working against capital formation, his firm would probably be very careful before investing in a new semiconductor operation as it did in Sunnyvale, Calif., in the 1970s. And like other managers, he points out that capital formation has a direct effect on R&D decisions.

Thomas A. Vanderslice, president of General Telephone & Electronics Corp., Stamford, Conn., agrees. "The R&D portion of a product development may account for only 10% of the cost needed to bring that product to market. Therefore, any reasonable manager has to have some assurance that the other 90% needed for plant and capital equipment is going to be there at the conclusion of development. Some firms are being forced to drop worthwhile R&D plans not because they can't afford them, but because they can't afford to capitalize on them."

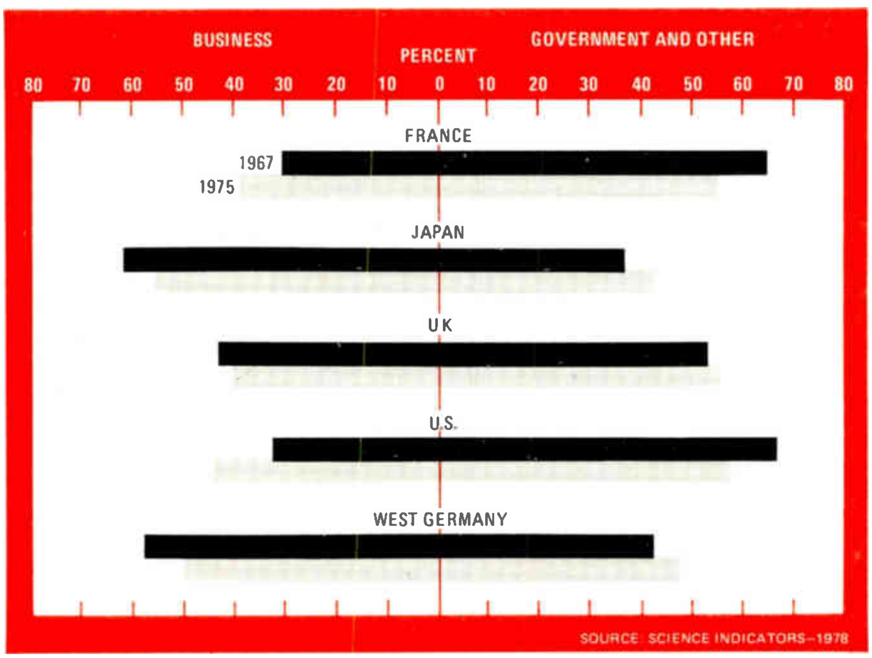
Vanderslice feels that the tax and regulatory burdens government places on industry strangle technological progress. Arthur D. Little vice president Derek Till agrees and estimates that an astonishing 25% to 50% of every R&D dollar may fall prey to government regulation; either it is used to pay for the multiplicity of reports, audits, and reviews so common today, or it is invested in work whose only real payoff is regulatory compliance.

Blame Washington. So, if there is a whipping boy in industry's executive suites, it is the Federal government. One instrument manufacturer, after citing a laundry list of complaints, winds up with a Bryanesque flourish: "If government would like to give the research community some incentive to work harder, it might try loosing it from the rack of the capital gains tax."

Mitre's Zraket is characteristically direct: "U.S. industry is being killed by disincentives. We need revisions in tax law, patent law, and other areas. Industry in other countries has it much easier by comparison; the usual examples are Japan and West Germany, but even in Sweden you find capitalism in socialist clothing. A Swedish firm can set aside a given percentage of its profit as an investment in R&D—tax free."

Other observers wish the Federal government could create a fiscal climate somewhat like that in Japan. Data General's Kalb notes that Japanese firms have easier access to funds and thus more ready money to spend on R&D than similar American firms. "A Japanese company is given a 200% tax credit for R&D," he says.

"They can write off R&D expenses in only one year, versus, say, six to eight years for United States firms. This generates an enormous amount of capital in Japan, despite the fact that the average Japanese firm has only about half the profit margin of an American company. Japanese bankers also tend to be easier to deal with in terms of lending against profit margins than their U.S. coun-



Where other nations spend. When comparing expenditures by business for R&D with what is spent elsewhere, Japan and West Germany are spending more than is the U.S.

terparts. There's a lot of unnecessary pressure on U. S. firms to keep profit margins high as a result of taxation and banking pressures."

If industry complains, it also suggest remedies. The Committee for Economic Development, a New York–based private organization of 200 business people and educators, warns in a report to be published Jan. 18 that "some public policies actually discourage capital investment . . . and have caused business to shift . . . R&D efforts from longer-term to more defensive short-term goals." Further, "unless there is speedy correction of these policies . . . the nation will find it increasingly difficult to solve its . . . economic problems."

The nonprofit CED notes in its new report that, as a percentage of GNP, Federal tax revenue has grown from 18.5% in 1976 to about 20% in 1979 and should reach 21% in 1981. This increase is said to have drained off monies that would otherwise have funded R&D and capital investment. And according to the Department of Commerce, R&D and plant and equipment investments follow cash flow closely.

And because of inflation and unfavorable regulations governing depreciation of existing plant and equipment, taxable profits are higher than constant-dollar profits. In inflationary times, according to the CED study, the effective corporate tax rate can therefore be much higher than the reported average rate of taxation.

Inflation has the same effect on the cost of capital and on current and actual rates of return on investment. The dollars that flow in, says the study, are worth a lot less than the cost to replace them so as to make new investments.

Thus, the CED feels its No. 1 tax-reform priority is one that would allow a more rapid capital recovery allowance. It believes that such reform would trigger increased investment in plant and equipment.

A second priority would change the tax laws to allow for flexible depreciation of R&D assets, taking into account the uncertainty of their usefulness. The CED would like to see both one-year and optional multiyear write-offs.

More credit. The CED also would like an increase from the present 10% investment-tax credit for investment in R&D facilities to 20% (still

R&D helps fuel growth

Does increased research and development guarantee corporate growth? Not necessarily, but it is almost always a help, according to figures from both government and industry.

Analog Devices Inc., Norwood, Mass., as part of a corporate strategy workshop, gathered figures on a dozen other high-technology firms in an attempt to correlate sales growth with R&D expenditures over the same period as a percent of sales. It found that higher R&D investments generally generated faster growth, but there were significant departures from this rule, with some firms getting far more—and less—bang for the R&D buck than the uninitiated might expect.

According to a Brookings Institution study, about 34% of measurable economic growth in the United States between 1948 and 1969 resulted from advances in knowledge. A Department of Commerce study covering 1929 to 1969 reckoned that technological innovation accounted for 45% of the country's economic growth.

Grouping industries by R&D intensity, as Data Resources Inc., Cambridge, Mass., did in a 1977 study, showed a marked difference between growth in productivity and output between firms with heavy investments in R&D and those with low to moderate investments. R&D-intensive industries showed a 4% yearly average growth in productivity between 1950 and 1974, and a 6.7% yearly increase in real output. The "electrical equipment and communications" industries led the pack with 4.4% productivity growth and 7.2% output increases. The averages for moderately R&D intensive industries were only 1.4% and 3.6%, respectively. Industries with little R&D averaged only 2% yearly productivity growth and 2.3% yearly increase in real output.

Already strong, the economic case for R&D can be further strengthened using the National Science Board's "Science Indicators—1978," which quotes National Science Foundation studies showing that $30 to $50 increases in annual output can result from a single $100 investment in R&D. That's a payback period of as little as two years.

A number of other studies quoted in the NSB report indicate that R&D return on investment can range from 25% to 35%. The NSB is quick to point out that this is a higher return than that yielded by almost any other form of investment. But as with all investments, there is an element of risk; a substantial fraction of companies sampled earned far less and some earned nothing on their investments. Managers still have to back the right horses.

The benefits of R&D, says the study, are higher productivity and output for the developers—and perhaps the same for their customers. Semiconductor and computer technology are prime examples of this effect. One recent study estimated that the average productivity returns on R&D conducted in industry during the 1960s was about 30% per year; for the customers of R&D-intensive firms the productivity increases averaged about 50%.

Admitting that it is possible to measure return on R&D investment only quantitatively, the NSB report adds that if qualitative measures were available, the return would be even higher. All these statements apply to industrial R&D; the NSB notes that estimates of the return on government R&D are unreliable.

The conclusions, then, would seem to be that properly managed R&D can be an extremely good investment for industry, producing returns to a firm and its customers exceeding typical corporate growth rates, or average return on equity, and the rate of inflation.

Further, there is some correlation between R&D spending by a firm and its rate of sales growth. It is by no means unambiguous, but the correlation exists.

So the answer to the question, "Does R&D pay?" appears to be yes, and the smarter the management and the greater the investment it is willing to make, the greater should be the return.

well below Japan's 200%), faster depreciation for patents (a rate more in keeping with accelerating technical change), tax credits for support of university R&D, substantial tax incentives for the smallest innovative companies, and reduced or deferred income-tax provisions for firms so heavily invested in R&D efforts that they have little or no real income.

The CED, like most executives, would like government regulations to reflect reality. Statistically impossible "zero-risk" goals, regulations that call for "best-available" technology when the definition of "best" is continually changing, and frequent changes in production standards that can often gut prior investments have all raised the cost of complying with regulations. And higher compliance costs mean lower R&D and capital investment budgets. Delays and court fights also accompany regulation; these add uncertainty and further cut the rate of possible innovation, the CED feels.

The group would like to see standards set realistically and industry left to meet them cost-effectively. It would also like increased congressional oversight, as well as sunset laws (those containing a provision for review or repeal after a specific period) to reshape, curtail, or remove unreasonable regulations. The CED also would like an in-depth study of the effect of regulation on the innovative process.

The falloff in patents during the last decade is chalked up by some to industry cynicism about the effectiveness of such protection. The CED is most concerned with patent disputes and timing.

Patent mechanisms. The CED suggests that, first, compulsory arbitration be used to settle patent disputes; second, that a single national court of appeals be established to ensure uniform application of patent law; and third, that a new mechanism be devised to strike "obviously invalid patents" from the rolls.

As to timing, the CED would like to see the life of a patent be delayed by regulatory questions. Second, it favors a "first to file" procedure with personal right of use granted to later filers who were prior inventors. Additional suggestions on patent policy include copyright protection for computer software and giving U.S. patent holders the right to enforce patent rights against imported goods made royalty-free.

For patents generated by government contractors, the CED thinks the contractor should receive title to these patents; at present, the Federal government assumes title in most case where its money—occasionally even minority funding—is involved. Given some legal protection, the CED feels that new technology is more likely to appear in the market if the patent is not in the public domain. And statistics on the poor use rate of government-owned patents tend to support this contention. If the original contractor did not move fast or far enough the government could mandate licenses to other firms. Finally, the CED would like to see more Federal investment in basic research.

Warnings. Mitre Corp.'s Charles A. Zraket (above) says revisions are needed in tax and patent laws to enable American R&D to keep pace with that of other nations. And RCA Corp.'s William C. Hittinger (left) notes that ideas are mobile, and other nations are taking advantage of heftier outlays for R&D to challenge the U. S. in world markets.

There seems little unreasonable in the CED's suggestions. It simply appears to be saying with one voice, minus some picturesque language, what most of industry is saying.

Bell Labs' Hannay leaves no room for doubt when he says that government R&D programs will not produce the technology of the future.

"There are people who would give

all credit for technological progress to government procurement programs, but it is private industry spending its own money that is producing the developments," he says. "For instance, the invention of the transistor was with Bell's own money," he adds. "It is difficult to find basic advances that have flowed from government procurement programs. The role of the government is important, but private industry can provide all the stimulation that is needed," he says.

Credits, not cash. Certainly TI's Heilmeier agrees: "The most important thing government should do is give tax credits to industry for R&D. Don't tell me they are going to dish out more R&D funds from Washington—the same wonderful people who brought you the post office are going to bring you innovation? Ridiculous—you need market incentives to innovate."

Richard A. Nesbit, director of research at Beckman Instruments Inc., Fullerton, Calif., feels strongly that just stepping up industrial R&D investment "to counter challenges from abroad won't be effective unless investment tax laws . . . patent laws, etc., also are changed."

He knocks "archaic" patent laws, and their interpretation allowing some firms to copy original devices without licensing or royalties, calling it a "basic challenge" to private property. And like Data General's Kalb, he is particularly concerned about the poor protection now offered software.

H. William Collins, vice president for advanced products at International Rectifier Corp., El Segundo, Calif., says it is more difficult to protect R&D results stateside than overseas because the U. S. court system, as reflected in its interpretations and comments, "considers patents instruments of monopoly and seldom rules against offenders." Since this limits returns on patented techniques, it is a disincentive to R&D, he feels.

Judges unqualified. An anonymous New England executive says that one reason the present use of multiple Federal courts to resolve patent disputes is so unsatisfactory is that "most judges are technological dolts." He definitely favors the CED's national patent court proposal.

RCA's Hittinger zeros in on incentives and capital. "We have to increase savings and capital accumulation because there is real risk in [R&D and] innovation, and this risk has to be hedged by incentives." He also agrees with the CED that "we need a national resolve [to spend more] money for basic research."

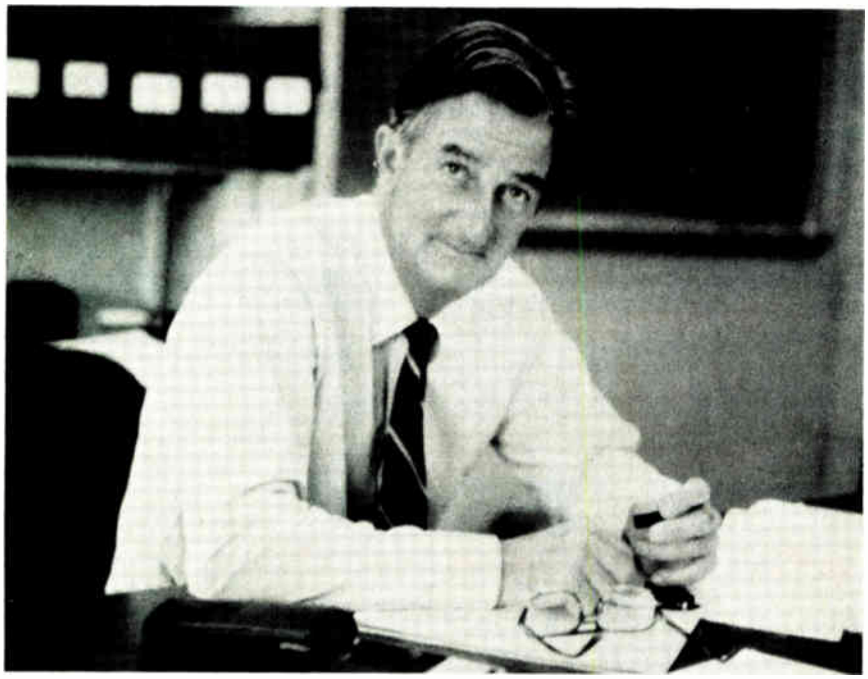
At the Hewlett-Packard Co., Palo Alto, Calif., Al Bagley, instruments group engineering manager, feels that a major U. S. problem is that "we have too many regulations—too many cost disclosures, for one, which get in the way of research itself." "It would be nice . . . if the government didn't demand so many program reports," he adds.

Last, but certainly not least, is the question of just how much basic research should be funded by any company. Bell Labs' Hannay is emphatic about the importance of such work by private industry.

"I have always felt that too few companies do basic research," he says, "and that a great many who do not would benefit from it." He thinks that 5% to 10% of an R&D budget is about the right sum to be earmarked for basic research, assuming that a company has reached what he calls a critical size, though he will not specify what size that is.

Legislative outlook. There's nothing like a friend on Capitol Hill. Sen. Stevenson feels today's situation "demands an 'ungentle' review of tax

Trouble ahead. Guy Fougere (left) of Arthur D. Little Inc. says America's shrinking spending on R&D could result in the nation's becoming second-rate technologically. Another ADL executive, Derek Till (right), notes that Federal regulation takes up to half of each R&D dollar.



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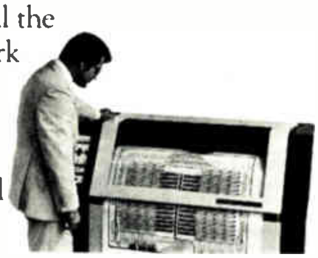

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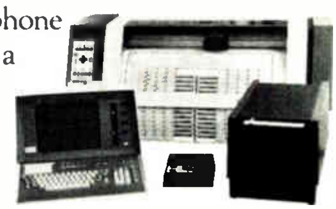

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codes and monetary instruments, export promotion and adjustment assistance, patent laws, and antitrust rulings—[we must] reassess traditional attitudes about the relationship between government and business." All of which should strike responsive chords in the hearts of technology executives.

Despite Stevenson's pronouncements, there's no rush to legislate. According to a senior House committee aide, "Right now there are five or six dozen bills pending on aspects of this issue that treat almost as many different issues. [Some legislators] have *ad hoc* efforts going to coordinate these, though I personally doubt that very much will get through chambers in the five or six months of real work time left" in this election year.

Nevertheless, staff members on both sides of the Hill are optimistic about getting something through on R&D policy this session. "The members are truly alert and concerned now that the country is being challenged in industrial as well as military markets" dependent on technologies like electronics, says one.

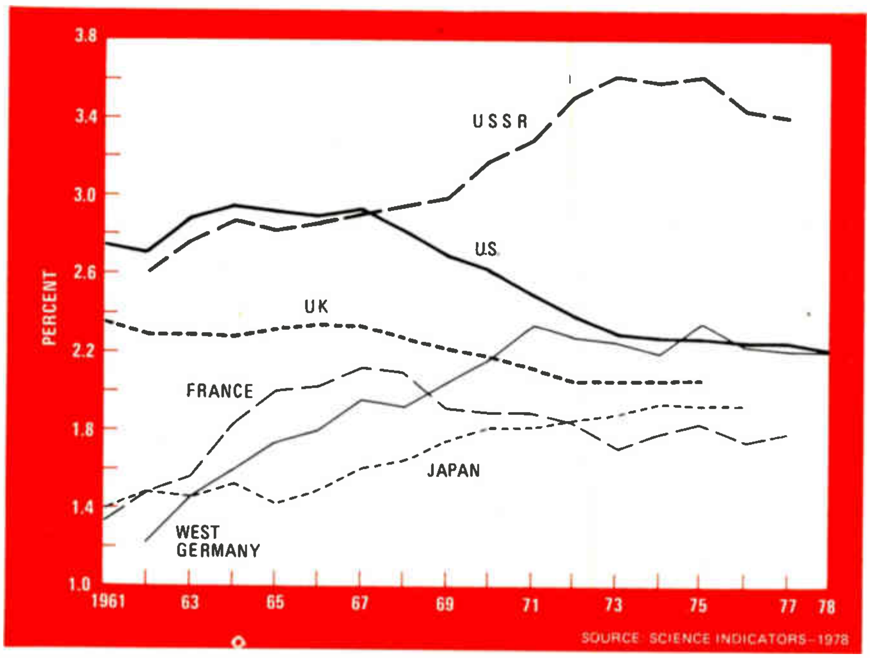
Some members are said to be suspicious, remembering the palmy days of the 1960s when some feel industry took advantage of Federal largesse, but "most appreciate that the problem is different now—there is a real challenge from abroad," says the staff member.

Tight cash. Data General Corp.'s Jeffrey Kalb says difficulty in capital formation has a direct effect on decisions concerning R&D.

But even with senators and congressmen becoming believers and executives in agreement with legislators, the nation is far from a full solution to its R&D problem. There is a legion of related issues waiting to be addressed, among them the problem of the risk-reward climate existing within many companies, which can turn creative minds into banker mentalities and choke innovation.

List of woes. There are the organizational and legal problems of justifying R&D inside, or cooperative research outside, a company, problems that make today's R&D managers a sorely tried group. There's the question of what the United States can learn from successful efforts here and abroad and what methods firms are using to make themselves more innovative. There is the nerve-wracking question of backing the right projects, when research funding is limited and money is a precious seed that must be planted in the most fertile soil. There is the question of technology exchange; it is possible that the U. S. may have hurt itself by selling its technology rather than the products of that technology. Finally, there is a coming decade of financial agony on campus, bringing with it questions about relations with industry and government and the amount of work—traditionally basic research—academe can perform, the number of new scientists and engineers colleges and universities can graduate, and the question of where new faculty will come from as the "Ph. D. pipelines" empty.

But, even if the answers are grim ones, SRI's Knock would have us persevere; high-technology markets are going to be too important to ignore. "In the near future, sales of high-technology products will grow three times as fast as those of low-technology products," he predicts. "The productivity growth of high-technology firms will be twice that of low-technology firms; the increase in employment due to high technology will be nine times that from low technology. The health of the United States economy is tied to R&D. It's a long-term investment in tomorrow, but we must make it." □



Falling. U. S. spending on R&D as a percentage of GNP has been falling steadily since the mid-1960s. It peaked at just under 3%, but by 1978 had dipped to a little under 2.2%.

This is the first of two parts. The second will deal with company R&D strategies in the U. S. and abroad.

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British decline has a bright spot

Electronics industries expected to grow 12.5% this year even as the overall economy continues to slide

by Kevin Smith, London bureau manager

Britain enters a new decade knowing full well that it will be worse than the last in economic terms. Even by the government's traditionally optimistic forecasts, the UK's economy—almost alone among European nations—will see a decline in real gross domestic product of 2%.

Britain is managing to run a trade deficit even with the help of North Sea oil. In fact, say some observers, that oil has added to the manufacturing industry's woes by inflating the purchasing power of the pound, thus sucking in imports and making exporting that much harder. The medicine administered by the new Conservative government is a tight control of the money supply, including a record hike in the minimum lending rate to 17%. This policy, plus a cut in state spending and a move toward greater personal incentives, is seen as a cure-all for Britain's long-term industrial decline. But when—or indeed if—this occurs, Britons face a tough intervening period made worse by a mounting world recession based largely on the soaring cost of oil.

Against this gloomy industrial landscape, electronics is one of the few bright spots. During 1979, sales of finished equipment grew at a steady 14% to finish the year at $6.54 billion (including inflation), according to *Electronics*' estimates. Solid growth in computers and telecommunications in particular should help to keep the bandwagon rolling into the 1980s—though at a slightly reduced pace, with equipment sales predicted to increase 12.5% to $7.35 billion.

In fact, nothing short of an apocalypse seems capable of stopping the headlong march of the computer industry, which in 1979 managed a 15% growth rate to close the year with sales to the home market of $2.06 billion. According to *Electronics*' survey, the industry should start the decade with growth running at 13%. "We have found the market to be in very good shape, surprisingly so in view of the economy," says Terry Stones, marketing manager of Honeywell Information Systems Ltd., London, "and we are planning to book even more business next year."

Confirming this estimate, Britain's indigenous computer manufacturer, International Computers Ltd., London, finished the year with very healthy results: a 22% growth in sales while retaining profit margins. Even more encouraging, UK sales were up 30%. Far from hurting sales of mainframes, IBM's announcement of its 4300 has stimulated the market, according to ICL's managing director, Christopher Wilson.

The minicomputer market has been particularly buoyant, with a growth of about 20%, compared with 12% for mainframes. But Mike Borschell of the market support group at Philips Data Systems Ltd., London, cautions that small businesses and companies that are using magnetic ledger cards and other systems for the first time are the very ones most likely to be hit by the 17% interest rate and so are the most likely to defer equipment purchases. As a result, growth of systems in the $14,000-to-$20,000 bracket may slide to a more restrained 15% level in 1980.

In the telecommunications sector, there is an air of confidence abroad

BRITISH ELECTRONICS MARKETS FORECAST
(IN MILLIONS OF DOLLARS)

	1978	1979	1980
Total assembled equipment	5,686	6,536	7,353
Consumer electronics	1,665	1,873	2,002
Communications equipment	1,501	1,809	2,173
Computers and related hardware	1,786	2,060	2,327
Industrial electronics	315	341	365
Medical electronics	205	210	211
Test and measurement equipment	184	210	239
Power supplies	30	33	36
Total components	1,814	1,998	2,125
Passive and electromechanical	954	1,032	1,080
Discrete semiconductors	237	259	278
Integrated circuits	287	340	381
Tubes	336	367	391

(Exchange rate: $1 = 48 pence; £1 = $2.05)

Note: Figures in this chart are consensus estimates of consumption of electronics equipment obtained from a survey made by *Electronics* magazine in September and October 1979. Domestic hardware is valued at factory sales prices and imports at landed costs.

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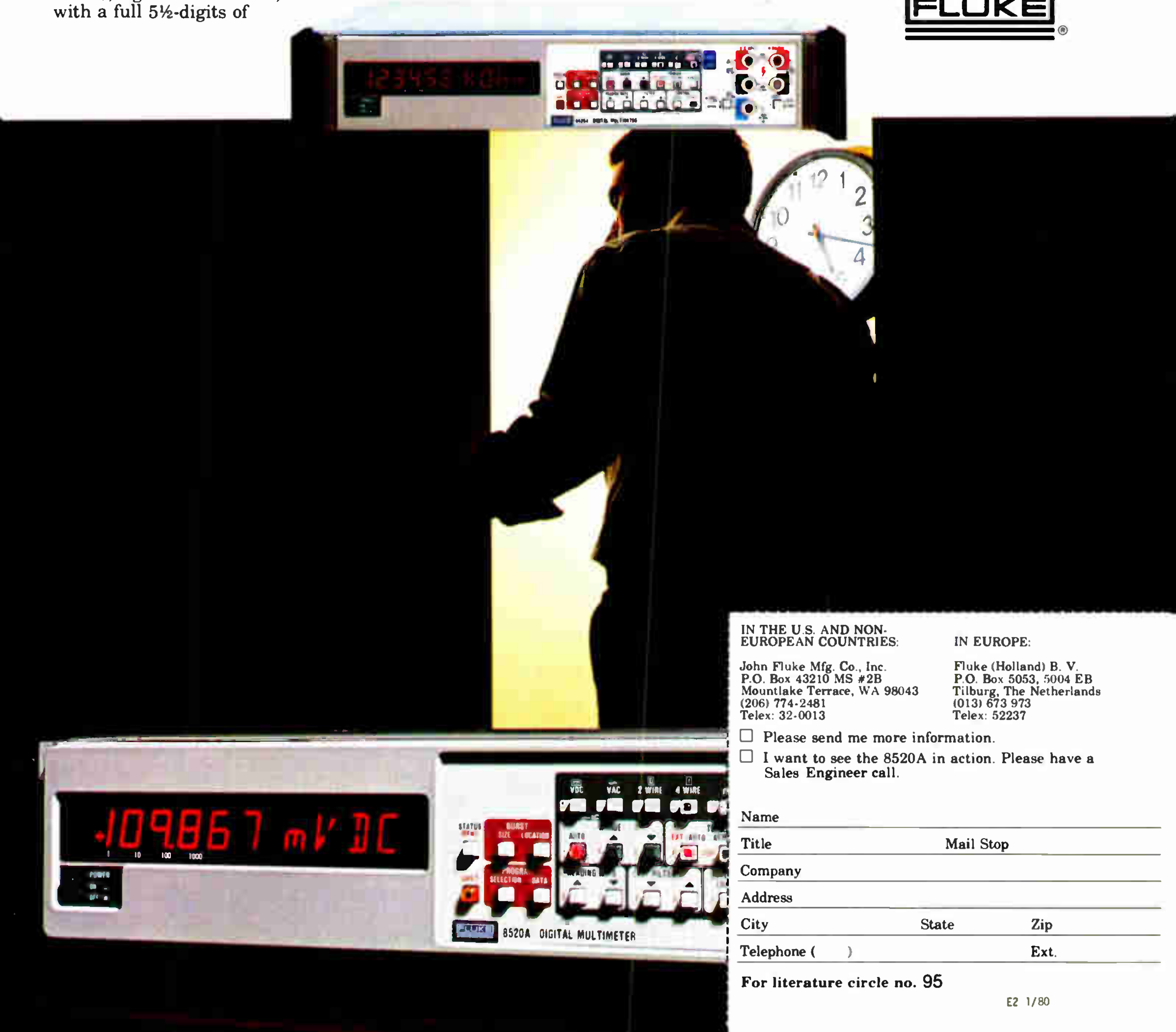

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that has not been seen for several years. With the large public-exchange sector well on course in its move to solid-state switching technology, the sector as a whole is enjoying a steady growth of some 20% to take total sales in 1980 to $2.7 billion, according to *Electronics*' estimates.

All three British Post Office suppliers, Standard Telephones & Cables Ltd., Plessey Telecommunications Ltd., and GEC Telecommunications Ltd., are now manufacturing the post office's intermediate semielectronic TXE-4 exchange. At the same time, the growth rate of the System X all-digital exchange program, developed by all three suppliers and the BPO, has quickened.

Consumer. Last year was a sluggish one for the consumer sector. The figures for color TV sales show an increase from 1.74 million sets in 1978 to 1.85 million units in 1979. These figures indicate a saturated market with first color replacement sales. But with a big squeeze on consumer spending in 1980, the industry will be lucky to match last year's figures; the forecast points to a fall in the growth rate from 12% in 1979 to 7% in 1980.

Video cassette recorders provide one growth point. Sales should reach 125,000 units in 1980, compared with 100,000 in 1979, says Nigel Schofield, a marketing executive with Thorn Consumer Electronics Ltd., London. The new year could also see the first significant sales of teletext- and viewdata-equipped TV sets. As volume production of the decoder chip sets builds and prices fall, sales of sets with teletext could climb from 40,000 to 100,000. By 1984, one source says, a third of all sets manufactured in the UK will have teletext. He is more bullish on viewdata, which gets under way as a public service in 1980, and sees sales—including monochrome business sets—jumping from next to nothing to 50,000 in 1980.

Test and measurement. *Electronics* projects a growth rate of 14% from a year-end figure of $210 million for the instrumentation and automation sector. But this figure masks the varying fortunes of its constituent areas. Test equipment sales, for example, are still surging, while the first signs of softness are appearing in the instruments market. Says Tony Davies, who until recently was a division manager with Schlumberger Measurement and Control (UK) Ltd., "We are still seeing a healthy demand for automatic test equipment, though there is a slight softening compared with a year ago." The 20% to 30% growth rate, Davies says, is fueled by the post office's switchover to semielectronic exchanges.

In comparison with ATE, the instruments market is "considerably softer," and some companies "are having difficulties meeting their quota" particularly in the more mature products, he believes. But front-end products like logic analyzers and microprocessor development kits are doing well.

Defense. In defense, an area where UK companies have traditionally excelled, growth has been solid, with a secure home market and a healthy export market. But export sales in an increasingly unsettled political climate look "somewhat volatile," according to Frank Chorley, managing director of Plessey Electronic Systems Ltd., Ilford, Essex. Still, defense spending under the Conservatives is getting a higher priority and spending is going up 3%.

Components. Mirroring the slowing growth of the equipment industry it serves, Britain's components sector is slated for a 6% growth rate in 1980 from a 1979 total of about $2 billion. Semiconductor business should grow by 9%, a figure that squares well with the 8% predicted by Dedy Saban, director of European marketing for Motorola Inc.

Integrated-circuit sales should grow 18%. Mike Young, a marketing analyst at Texas Instruments in Bedford, however, believes the increase will be below 15%.

The microprocessor is changing the industry structure by generating new products and new companies in data communications, computers, and industrial products, according to one components company, but the resulting growth may not help the balance of payments very much, as the trend is to import fully equipped microprocessor boards.

Topping the growth league is, of course, memories. "The demand for memory parts, and in particular 16-K random-access memories, is explosive," says Ken Davies, marketing director of ITT Semiconductors Ltd. Worldwide, he says, the demand for the 16-K parts will double to 120 million next year. □

Third in a series examining European markets.

Good defense. Typical of British products intended for the military is this digital message terminal, in use with a vhf radio manpack, called the Supertalk, from Plessey Co.

Computers

Assembly language plan raises dust

Mnemonics standard for microprocessors leaves semiconductor makers cold, and others say effort comes too late

by Martin Marshall, West Coast Computers & Instruments Editor

After 2½ years of effort, the IEEE Computer Society's subcommittee on standardization of microprocessor assembly language has proposed its standard and started a controversy. Industry members are challenging both the content and the concept of the document.

"We don't see much use for a single set of assembly-language mnemonics that tries to fit all microprocessors," says Terry Opdendyk, manager of software development for Intel Corp. of Santa Clara, Calif. Others say that even if the standard is useful, it comes too late, with microprocessors already in widespread use. Not only that, but a great deal of software already has been written for them.

Assembly language consists of alphanumeric mnemonics that generally correspond one to one with the all-numeric machine instructions and is thus considered a low-level programming language that varies from machine to machine. Hence, a standard assembly language will limit manufacturers' freedom in determining their microprocessors' instruction sets—a feature the manufacturers feel is proprietary and critical to differentiating among their various products.

No rule. There is thus no standard assembly language in the computer or microprocessor industry, although there are standards for machine-independent high-level computer programming languages such as Cobol and Fortran.

One important and enthusiastic supporter of the standard is Robert Stewart, chairman of the Institute of Electrical and Electronics Engineers' Computer Standards Committee, which will rule upon the final acceptance of the proposal. "This effort at standardization has been fueled by six years of user frustration with the divergence of existing microprocessor instruction mnemonics," he asserts.

Software producers and users want an assembly-level mnemonic standard because they need to apply programs written for one microprocessor to a system using a different one. There is also an increasing number of applications where two or more different microprocessors are used in the same system. But the ultimate rationale for a standard is that a single universal set of mnemonics greatly reduces the burden of educating the designer.

A universal standard could also eliminate situations in which the same mnemonic means the opposite in different microprocessors. A case in point is the instruction "Move A, B": it moves the contents of "A" into "B" in the Intel 8080, but moves data the other way in Zilog's Z80 and other processors.

Makers vs users. "The key issue here is the difference in self-interest between the microprocessor manufacturers and the microprocessor users," asserts subcommittee member Andrew Allison. He points out that it is clearly in the manufacturers' interest to have a unique set of mnemonics, thus making it inconvenient for the user to change to a machine from a different maker.

As Allison puts it, "For the IC makers to come out in favor of the

STD OPERATOR ABBREVIATIONS

Arithmetic mnemonics		Logical mnemonics		Program control mnemonics	
AD	add	Logical word operators		JP	jump
AC	add with carry	AN	and	JS	jump to subroutine
SU	subtract	OR	or	JI	jump to interrupt
SC	subtract with carry	XR	exclusive-or	RT	return
SB	subtract with borrow	CP	compare	NO	no operation
MU	multiply	CM	complement	HL	halt
DV	divide	CL	clear	EX	execute
IC	increment	SR	shift right		
DC	decrement	SL	shift left		
Data transfer mnemonics		RR	rotate right		
		RL	rotate left		
		AJ	adjust		
LD	load	TR	translate		
ST	store	Logical bit operators			
MV	move	TS	test		
XC	exchange	SE	set		
PS	push	RS	reset		
PL	pull	EN	enable		
IP	input	DS	disable		
OP	output	BS	bank select		

standard at this point would be analgous to IBM coming out in favor of plug compatibility." Says Intel's Opdendyk, "We are strongly in favor of the various IEEE efforts to reach a high-level language standard, a bus standard, and a floating-point standard, but we don't see much use for a single set of assembly mnemonics."

Wrong time. Ken McKenzie, marketing manager for microcomputer components at Zilog Corp. in Sunnyvale, Calif., adds, "This standard has arrived too late, when the inroads have already been made into the 8-bit and 16-bit microprocessor application areas. Just look at all the things that would have to be changed to accommodate it. All the application programs and their documentation, the assemblers, the programmer's reference cards, the manuals, the data sheets, and even the [high-level language] compilers will have to be changed because they output code at the assembly level. Then our customers who write their own documentation will also have to change it."

At Motorola Inc.'s Semiconductor Products Group in Phoenix, the reaction is similar. "It is usually not realistic to try to impose retroactive standards," says Jim Gunderson, manager of product planning for microsystem development equipment. "Applying the standard to future microprocessors is another question, however," he notes.

In spite of the generally negative comments from the IC executives, it is interesing to note that the official positions at Motorola, Intel, Zilog, and the Maynard, Mass.-based Digital Equipment Corp. are the same: they are studying the proposed standard and will not rule out its application in their products.

The proposed IEEE standard also comes under some friendly fire from the proponents of yet another proposed mnemonics standard. Pro-Log Corp. of Monterey, Calif., after years of conducting seminars to teach assembly languages to hardware designers, created its own "universal" mnemonics set—the STD mnemonics. "Our mnemonics are designed to make things simple from the working engineer's point of view, whereas the IEEE mnemonics were designed from a higher-level, data-processing point of view," notes Matt Biewer, Pro-Log's vice president of engineering.

Same length. More specifically, all of Pro-Log's instruction operators are exactly two characters long (see table); the subcommittee's proposal, on the other hand, suggests instructions of one to four characters. Pro-Log builds a single statement by joining mnemonics for the operator, locator, qualifier, and modifier functions. The fundamental difference in orientation between the two sets of mnemonics is exemplified by the use of "jump," a hardware-oriented term, in the Pro-Log mnemonics, versus "call" and "branch," both data-processing terms, in the IEEE formulation.

Biewer notes that the two formulations emerged because "we [the IEEE and Pro-Log] were both too far downstream to back off." The STD mnemonic, he points out, has at least one head-start on the IEEE proposal. That is that Pro-Log is negotiating with Digital Research Corp. of Pacific Grove, Calif., to create a modified version of its CP/M operating system to accommodate STD.

Test coming. If the IEEE computer standards committee adopts a version of proposal 694, which is expected to happen after a review-and-input period of about six months, then there may be a real test of the IEEE's power. Against the studied indifference of the semiconductor makers, the IEEE must generate a bandwagon behind its standard that will have enough momentum to force the integrated-circuit manufacturers to join it. However, the first assemblers will probably be made independently of the IC makers.

Although no one is putting down bets at this point about the power of the IEEE versus the likes of Intel, Motorola, and Zilog, advocates of the proposal can extract a glimmer of hope from the sphinx-like statement of Intel's Opdendyk. "All I can say is that new microprocessors will continue to change," he responds, "and as with IBM's change from the 1401 to the 360 series, sometimes that will involve new rules." □

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When TI talks, the message moves fast

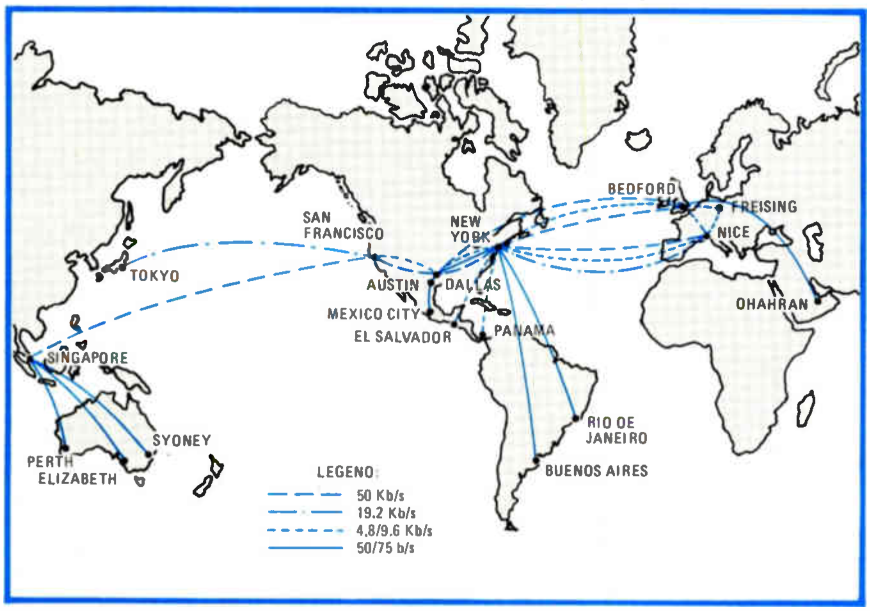
What may be world's largest private on-line system for data communications uses 4 of 10 available 50-kb/s channels

by Wesley R. Iversen, Dallas bureau manager

The decreasing cost of computing power coupled with the need for improved productivity is moving distributed computing from buzzword to reality for an increasing number of applications. Perhaps nowhere in the industrial world is the trend more evident than at Texas Instruments Inc., where commitment to the concept has led to the establishment of an integrated system supported by what some believe to be the world's largest private, on-line data-communications network.

In terms of international wideband satellite circuits—those that handle 50 kilobits/second or more—TI uses 4 out of the total of 10 such channels that are currently available for nongovernment use, says John W. White, TI assistant vice president who heads the Dallas company's information systems and services group. Also in use are a multitude of lower-speed circuits (see illustration), producing a network that ties together TI operations worldwide and also includes distributors, suppliers, and customers. A sampling of the capabilities supported includes word and data processing, electronic message switching, engineering design transmittals and order entry, and various personnel, manufacturing, inventory, and financial management and control functions. Voice communication is also integrated into the system.

The TI network is "definitely one of the most advanced in the world," says Larry Day, director of the Diebold Automated Office Program, a New York–based research service. "The number of applications they have included and the level of organization they've penetrated there is unique in my experience. The network and its whole approach are not a sideline activity. It's a very major part of the way they run their business," Day observes. "Everybody from the president on down uses a terminal."

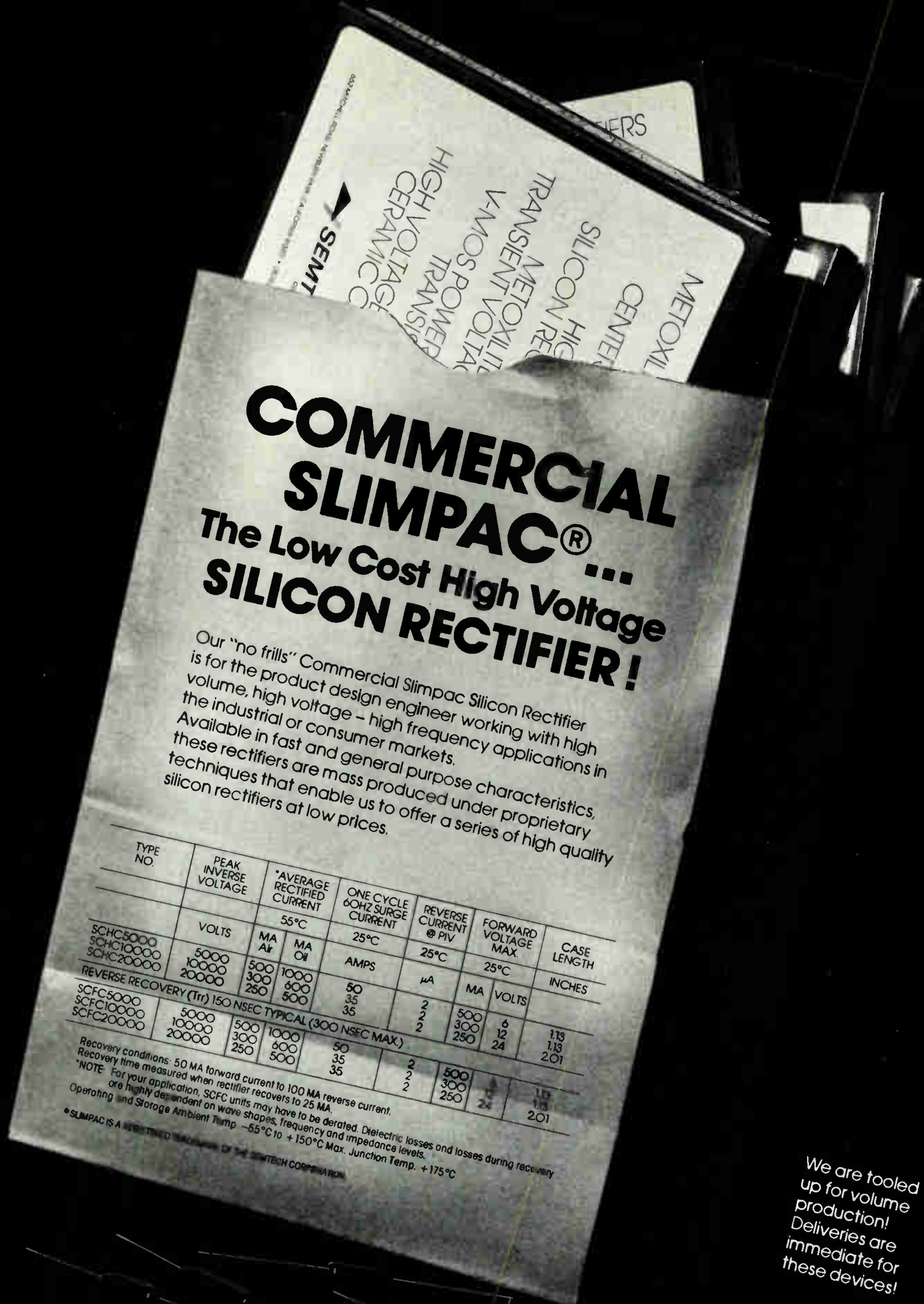


Major circuits. Besides those shown, TI also has links to Seoul, Hong Kong, Kuala Lumpur, Bagyio, Taipei, Osaka, Hiji, and Hatagoya in the Far East and Campinas in Brazil.

Indeed, TI president J. Fred Bucy has a dedicated terminal not only in his office, but also in his home, as do about 50 other TI executives. And like other top officials, Bucy carries a dial-up terminal with him when he travels that provides access to any of the company's 45 plants worldwide, as well as to TI geophysical exploration ships at sea.

While the TI system is under constant evolutionary development, its size and utilization have recently grown rapidly. During the last 18 months, about 4,500 keyboard inquiry terminals have been added to the network, bringing the total on line to around 8,000. That's a dramatic growth rate, TI sources point out, since the first 3,500 terminals were installed over a period of six years.

Mail call. Among other things, the 8,000 terminals are used for TI's internal electronic mail, with the ability to interface with outside Telex networks as well. The number of messages sent per week has risen from 90,000 last March to 130,000 now, White indicates, with each message routed to an average of four destinations. The inquiry terminals work in conjunction with about 1,400 printers. In addition to the 8,000 inquiry terminals, the system also ties in some 275 remote batch job-entry terminals as well as 135 distributed processors that maintain local data bases on hard disk. Also



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SCHC5000	5000	500	1000	50	2	500	6	1.13
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on the network are 30 to 40 word-processing computers, says White, each of which works with one or two letter-quality printers and has floppy-disk storage.

Of the 8,000 inquiry terminals, about 6,000 are TI-built, says White, and some IBM terminals are used at the Corporate Information Center. However, the computers on the distributed network are all TI products, he says.

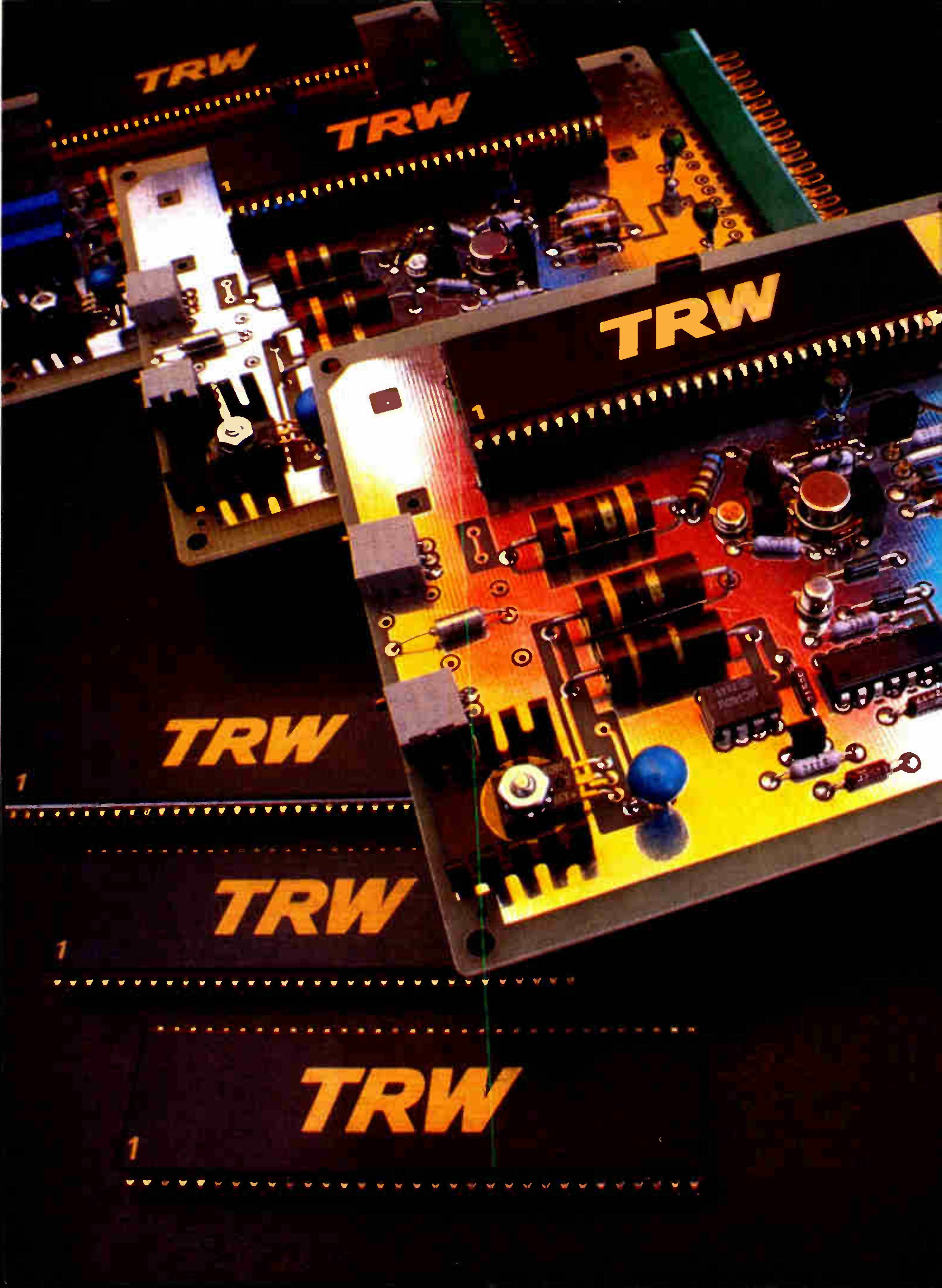
The CIC is the heart of the TI system. Located in Dallas, it consists of six IBM 3033 central processors, each with a minimum of 12 megabytes of memory. Additional storage includes 348 disk drives with capacities ranging from 200 to 317 megabytes each, as well as 80 tape drives that handle 86,000 reels of magnetic tape. CIC power is distributed through interface with a system of TI 980 minicomputer-based boxes known as Ticogs (for TI communication grid) that manage the network in a packet-switching mode.

Other functions. In addition to functions already described, TI maintains numerous other applications systems that make use of the network for productivity improvements, including the following:

- Engineers can pull up documentation from an on-line terminal relating to parts that are going into a design. CIC power can be used for logic verification during semiconductor circuit design. Completed designs can be shipped to another TI location for mask generation, while the necessary test data goes to the appropriate test center computer for use when the product comes off the manufacturing line.
- Various manufacturing work-in-process systems provide mechanized control and tracking from slice generation to assembly. Yields, scrap rates, and other data taken at various points are fed into a cost accounting system for detailed tracking of manufacturing costs on a product-by-product basis. Shipping documents are automatically generated for assemblies and products in transit between TI locations.
- TI customers may place orders and make inquiries through their own dedicated terminals that are tied into the TI network. As shipments go out, inventory and receivables status is maintained accordingly.
- Modeling systems that draw on current data bases provide TI managers with financial planning information. Data stored on more than 4,000 individual cost centers within the company can be consolidated in various ways to show the short- or long-term corporate impact of differing strategies.
- A personnel management system enables TI managers in remote locations to take part in a voting system for ranking the value of particular employees to the company. Managers use touch pads for voting on paired comparisons—two employees at a time. Salary and incentive pay decisions based on the voting can be fed directly to the payroll system.
- Inquiry terminals may be used for access to on-line textual material, including company newspapers, reference information, installation/training documentation, and sales catalogs. Use of the system is currently running at 2.4 million inquiries per month, says White.
- Teleconferencing with the real-time images of people has not been found cost-effective, says White. But financial planning meetings that make use of projection TV systems coupled to an inquiry terminal for display of real-time data-base graphic material are conducted regularly with participation by TI managers in remote locations.

Annual cuts. TI goals call for a 5% reduction annually in data-processing costs to internal users of the network, says White. Considering current inflation rates, he notes, that means 5% plus double digits. Nevertheless, the CIC learning curve shows that the goal has been met, with a 64% cumulative cost reduction for the system since 1967.

Under terms of an agreement signed in 1973, TI uses International Telephone & Telegraph Corp. as its sole vendor for international satellite communication service. TI does not think that launching its own satellite would ever be cost-effective, says White. But the company does have plans to install its own private earth station for direct reception capabilities in Dallas, he says. ☐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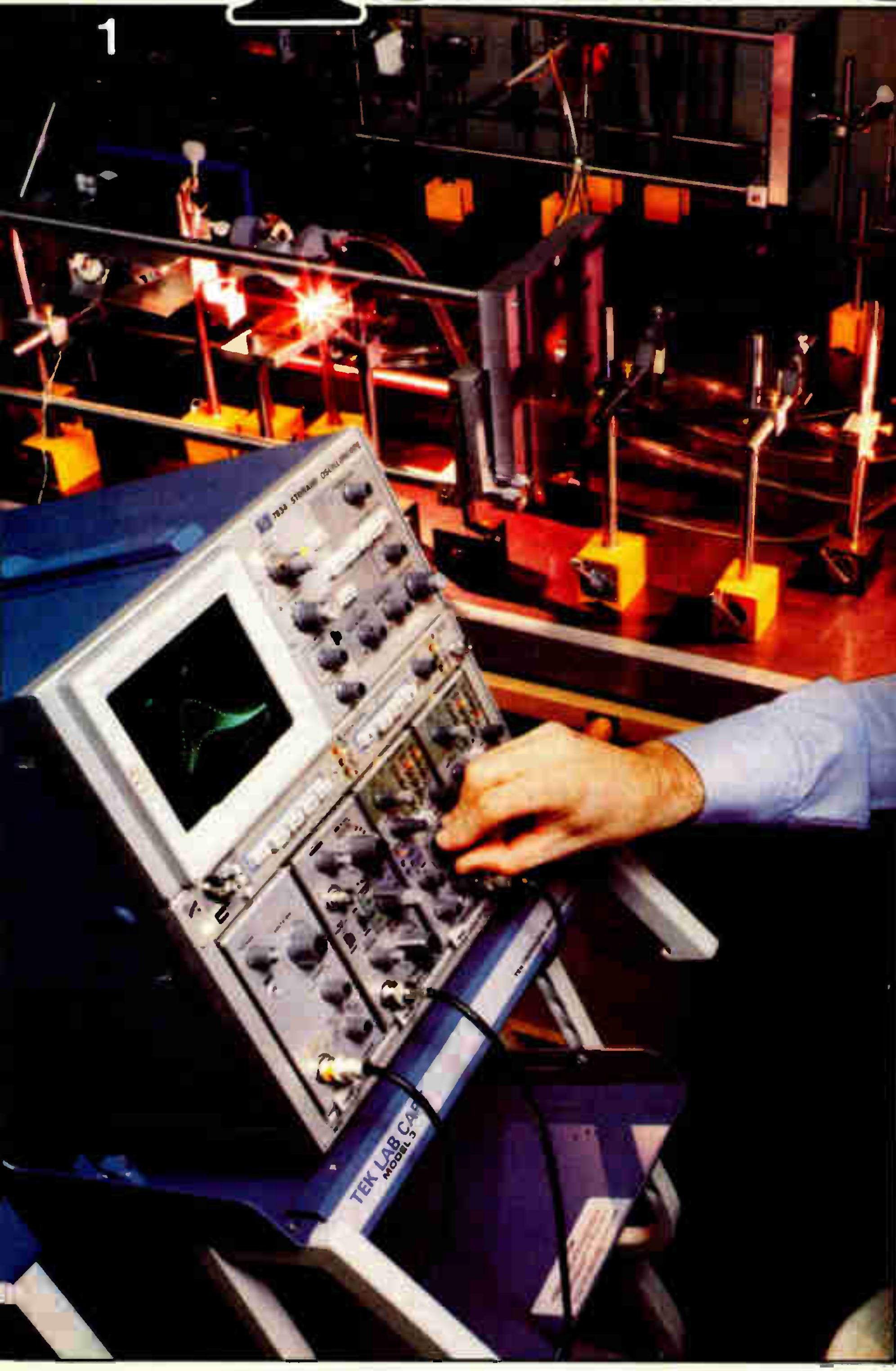

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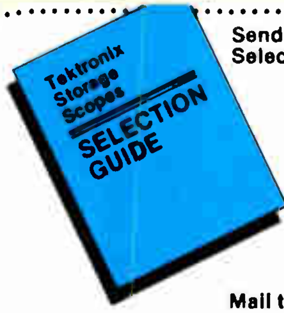

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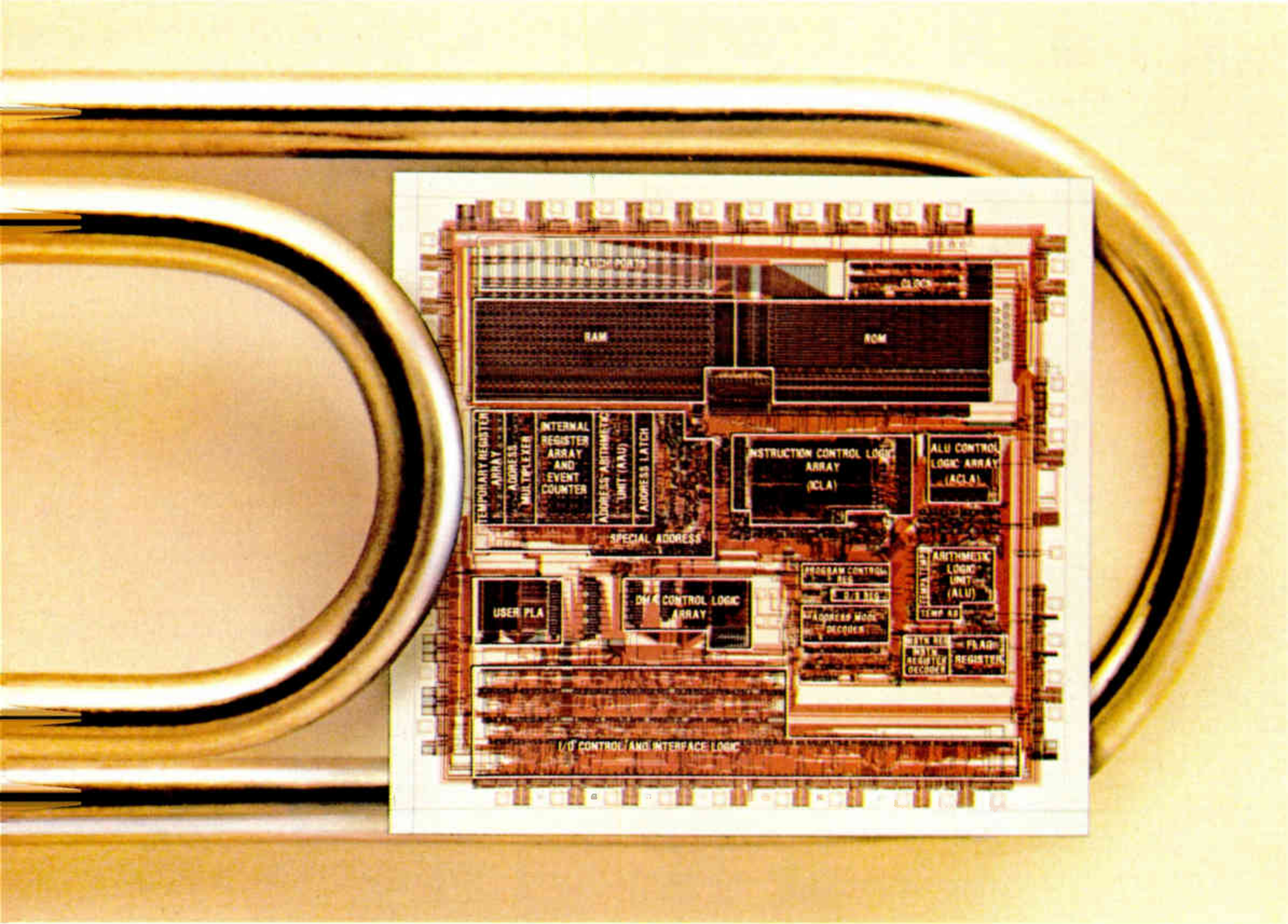
The one-chip computer: offspring of the transistor



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Four-chip hybrid carrier holds down system costs

An analysis of packaging options settles on four-chip hybrids for small-scale–integrated portion of central processor

by Dan I. Amey, *Sperry Univac, a division of Sperry Corp., Blue Bell, Pa.,*
and Jack W. Balde, *Western Electric Co., a subsidiary of American Telephone & Telegraph Co., Princeton, N. J.*

☐ During the next few years, packaging engineers will be designing with a mix of large- and small-scale integrated circuits housed in a number of different packages. There is no simple formula that determines the most cost-effective combination of package types—dual in-line packages and the newer square chip-carriers with leads on four sides, made with varying lead spacings in either ceramic or plastic.

A joint study made by Sperry Univac and Western Electric examined the costs that would be incurred in building similar central processing units using several possible package mixes and current printed-circuit board technology. The chip-carrier is clearly taking the place of the DIP. This is most obvious in the case of LSI chips with 68 or 84 leads: DIPs with this many leads waste far too much board real estate; electrical performance requirements also help eliminate DIPs of this size.

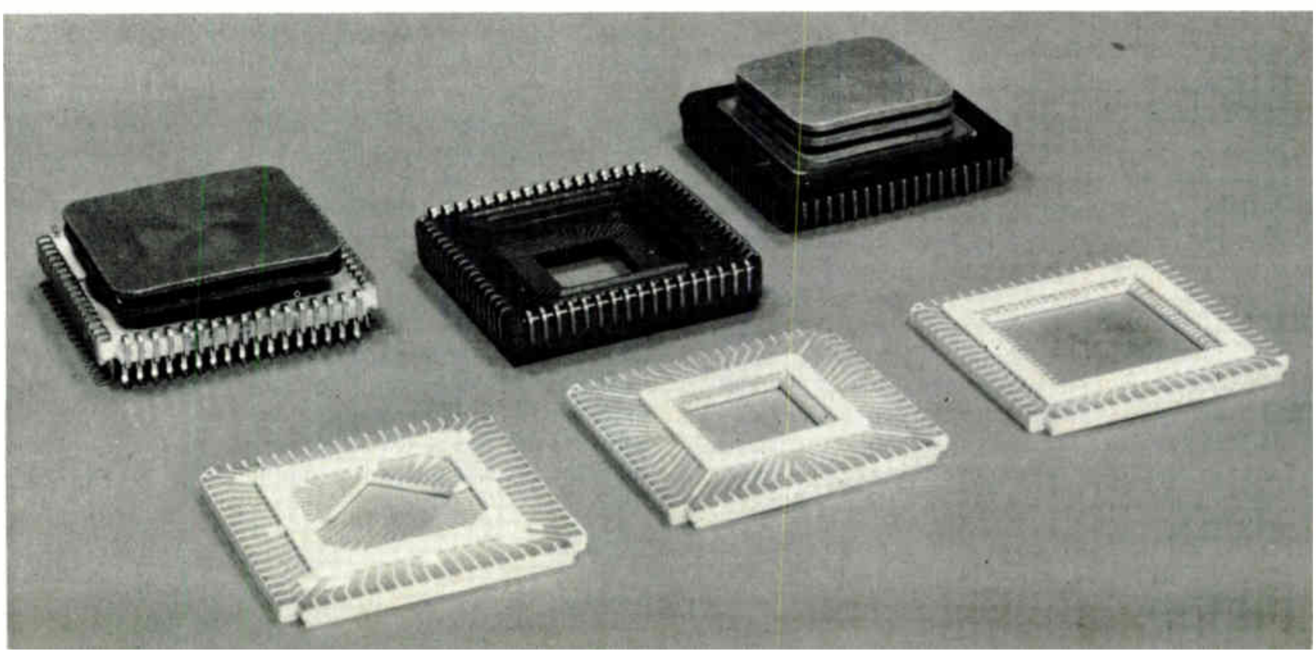
It is much less clear how the SSI circuits should be housed. DIPs are a viable alternative, small chip-carriers with a single SSI chip in each are another, and larger carriers with anywhere from 3 to 14 SSI chips on a hybrid substrate mounted on a single carrier represent yet another set of choices. The study concludes that large chip-carriers with leads on 50-mil centers housing three or four SSI chips are the most cost-effective choice. These hybrid packages also can be converted relatively easily to custom LSI in the future.

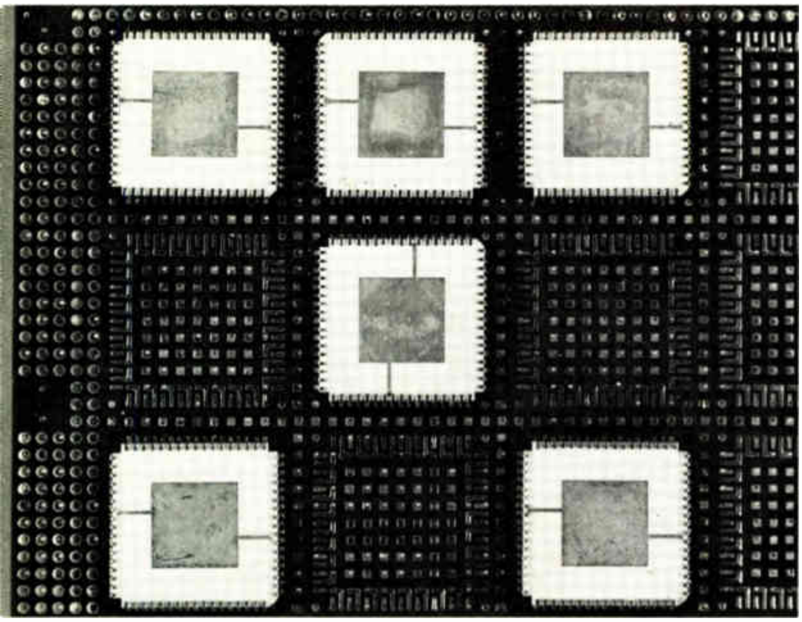
The Joint Electron Device Engineering Council's recent standardization program [*Electronics*, March 17, 1977, p. 89] considered the family of ceramic chip-carriers with leads on 40-mil centers and the family of ceramic and plastic chip-carriers with leads on 50-mil centers (Fig. 1). Plastic carriers are significantly less expensive than their ceramic counterparts, but the choice of package size and type has a much larger economic impact on the finished system. The package size and the spacing of the leads determines the cost of the printed-circuit boards and system interconnections, which are far more important factors than the carriers themselves.

Boards must keep pace

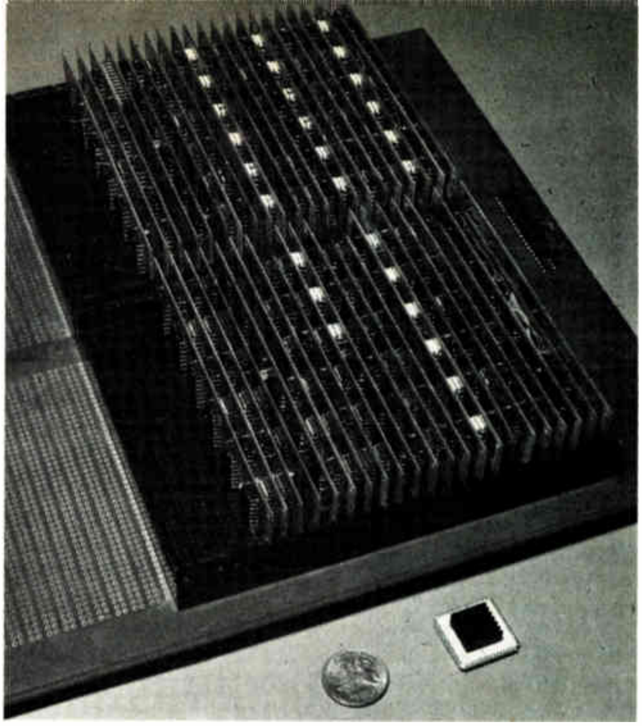
Ever since the Computer Packaging Committee of the Institute of Electrical and Electronics Engineers' Computer Society first began to promote chip-carrier standardization, it has been clear that the choice of contact spacing—and therefore the packing density of the circuit—should be dictated by the economics of the interconnecting substrate. Using contacts spaced too

1. Cost cutters. The family of standardized (by Jedec) chip-carriers with 50-mil pad or lead spacing includes leadless ceramic members (front) and plastic carriers with leads (rear). The 0.540-inch-square cavity of carrier at right is intended to house multichip hybrids.





2. Standards in harmony. Chip-carriers with 50-mil lead spacing can be mounted on multilayer printed-circuit boards with the standard 100-mil grid of vias using a simple wiring pattern. Carriers with 40-mil spacing complicate wiring, requiring more board layers.



3. Large is small. The large-scale integrated circuit in the foreground is equivalent to the 220 small-scale integrated circuits in dual in-line packages behind it. A practical system average of 150 SSI chips replaced by one LSI chip can be achieved without much difficulty.

closely asks an interconnection density of the board so great that its costs overwhelm any savings that might accrue from a smaller package size.

Hypothetical devices with 10-mil pads on 20-mil centers or 15-mil pads on 30-mil centers call for multilayer ceramic substrates or pc boards as the interconnecting medium—boards with 6 to 10 signal layers, fine lines, and tight tolerances. These boards are expensive. Striving for the highest possible IC packing density offers little or no economic advantage.

This point of view was supported by Walter Vilkelis, a senior engineer at IBM Corp., East Fishkill, N. Y., in a presentation before the IEEE Computer Society Packaging Committee in October 1978, analyzing the effects on performance of increased packing density of ICs. "The trend to higher circuit packing density must be supported by reductions in the cost of building the assemblies," he said. "There is little or no return on performance as density increases in packaging when the same cooling technology and wiring medium are used."

50-mil vs 40-mil centers

The differences between chip-carriers with leads on 40-mil centers and those with leads on 50-mil centers might seem insignificant at first. But there are inherent advantages in 50-mil spacing when pc boards are to be used. John Bauer, manager of design and development engineering for RCA in Moorestown, N. J., has demonstrated that hybrid assemblies using chip-carriers with leads on 40-mil centers on ceramic substrates are economically viable when there is a military requirement for hermetically sealed devices. Ceramic boards with 10-mil-wide paths and 10-mil vias can cost more than the equivalent pc board with two signal layers. The ceramic carriers also cost more than plastic carriers.

Ceramic substrates also cannot be made in as large sizes as can printed-circuit boards. The larger pc boards provide better options for partitioning a system. And printed circuitry is a more suitable medium for high-speed designs, both for delay and conductivity reasons. The predominant application of LSI circuits will be on pc boards.

A chip-carrier should therefore be compatible with the 100-mil grid of pads and holes currently in international use as the printed-wiring standard. Even metrification is not expected to change this 100-mil grid. This standard spacing makes it possible to put two or three wiring paths between the vias—the holes that connect layers of multilayer pc boards. The width and thickness of the paths are constrained by physical properties that affect the circuit's characteristic impedance, line inductance, series resistance, and circuit coupling. The standard also allows relatively inexpensive manufacturing.

With vias on 100-mil centers, 50-mil lead spacing on chip-carriers permits surface interconnection to the pc-board grid with a simple pattern (Fig. 2). Chip-carriers with leads on 40-mil centers complicate the interconnection considerably.

Sockets for LSI devices represent another reason for 50-mil lead spacing. Some engineers want sockets for these high-lead-count ICs because the board is too costly to risk frequent unsoldering and removal of faulty chips. Easy chip removal may also be required to open up loops and networks for troubleshooting and testing purposes.

Socket tolerances

Sockets become a severe problem with terminals on centers 40 mils or less apart. Tolerances due to ceramic shrinkage and manufacturing tolerances of carriers and sockets bear a linear relationship to the length of the longest side. A 156-lead chip-carrier with 50-mil lead spacing (39 leads on a side) and its socket can be made economically. For 40-mil spacing, tolerance considerations suggest a maximum of 100 leads; a 70-lead maximum is indicated for 30-mil spacing; and 40 leads is the upper bound for 20-mil centers.

The five designs for a medium-sized CPU listed in the table were based on costs typical in the industry. Actual cost experience will certainly differ, but data for a particular application may be substituted and more pertinent comparisons obtained.

The first design assumes 3,600 SSI circuits mounted exclusively in DIPs. At just over 80¢ for chips so packaged, the IC cost alone is about $3,000. The printed-circuit board cost to mount 3,600 DIPs on 300 small (6-by-6-inch) double-sided boards with bus-bar power distribution would be $2,000, assuming just under $7.00 for a board and its connector. (Costs for the 60 7-by-10-in. boards required to package 3,600 DIPs would be comparable.) Costs of cabinet, assembly, cable, wire, and testing are proportional to board size; they come to about 150% of board interconnection costs. Exactly 150% was used here for simplicity, to give a feel for the relative system economics; a specific cost analysis will determine whether this factor is appropriate.

There are additional system costs for power supplies and cooling. If different designs are relatively alike in energy efficiency, a reduction in power supply cost resulting from the smaller number of cabinets may be offset in part by the increased cost of cooling the high-density package. Again, to simplify the analysis, the power supply and cooling cost was assumed to be constant. The cost of the CPU using all DIPs comes to $8,000.

Mixing DIPs with chip-carriers

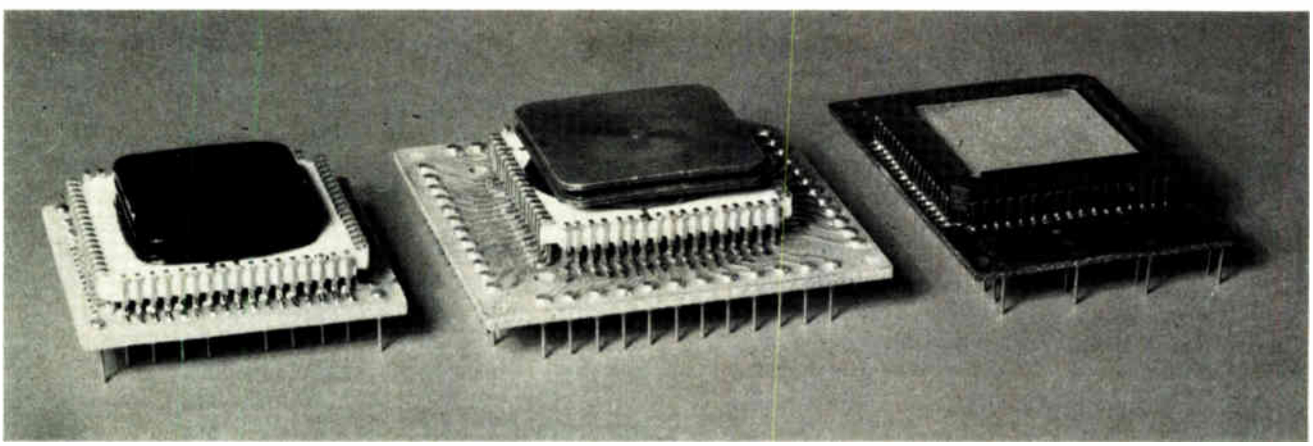
Some designs reported in the literature have a single LSI chip replacing up to 220 individual DIPs (Fig. 3). It is not difficult to achieve a practical system average of 140 or 150 DIPs replaced by one LSI circuit. If 90% of the CPU's circuitry can be handled by LSI circuits, the hypothetical system with 3,600 DIPs can be replaced by 25 LSI chips and 360 DIPs, as in the second option in the table. (It is difficult to imagine an all-LSI design; the chips would require too much design effort and would result in insufficient quantities of infrequently used devices to justify the cost.)

If the LSI circuits cost about $30 apiece, the costs are $750 for the LSI and $300 for the remaining 360 DIPs, a total of $1,050. Printed-circuit board cost is based on seven multilayer boards, required since the remaining 360 DIPs dominate the physical design. Each one of six

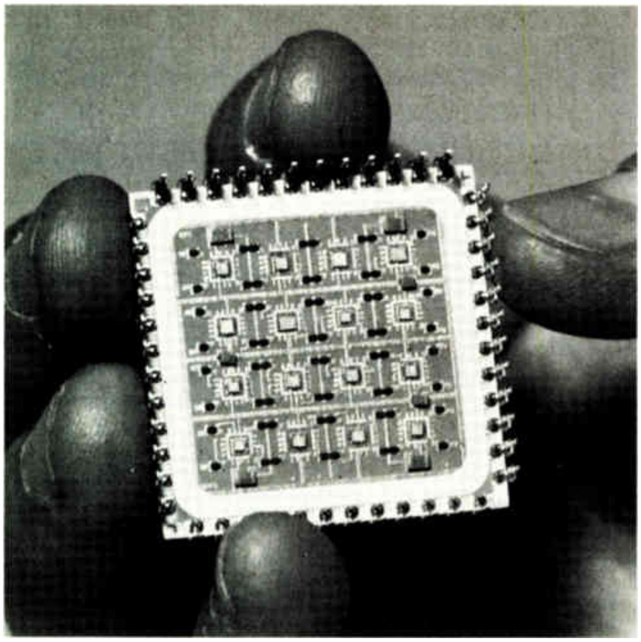
COST ANALYSIS OF CENTRAL PROCESSING UNIT BUILT WITH SEVERAL PACKAGE MIXES

Package types	Integrated circuits	Boards	Cabinet, cable, assembly, testing	Total, without power or cooling
All small-scale ICs in dual in-line packages (DIPs), 300 boards	$3,000	$2,000	$3,000	$8,000
SSI chips in DIPs and large-scale ICs in chip-carriers, 7 boards	$1,050	$1,050	$1,500	$3,600
14-chip SSI hybrids and LSI chips on carriers, 1 board	$1,920 ($1,050)*	$500 ($1,370)	$750	$3,170
Single SSI chips in 24-lead carriers and LSI chips, 3½ boards	$1,050	$525	$1,000	$2,575
4-chip SSI hybrids and LSI chips, 1 board	$1,300 ($1,050)	$400 ($600)	$750	$2,450
Partial conversion of 4-chip hybrids to LSI	$1,000	$400	$750	$2,150

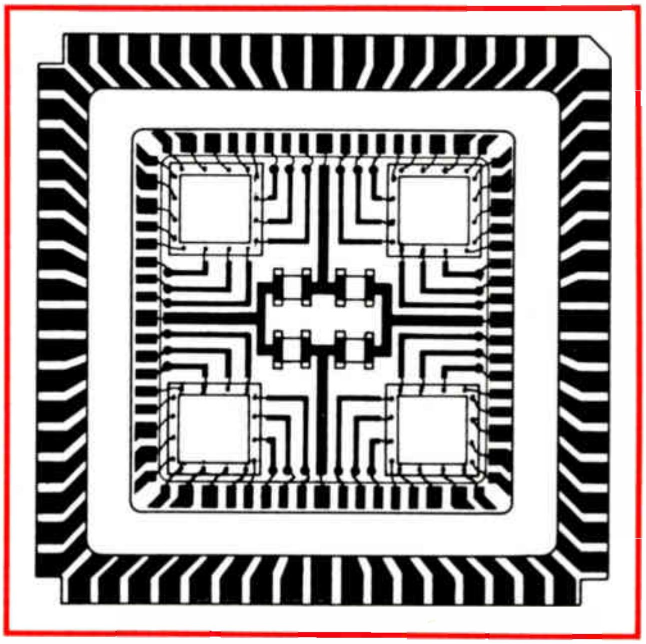
*Figures in parentheses are restated costs with hybrid substrates counted as boards.



4. DIP-like chip-carriers. An adapter that makes a chip-carrier with leads on 50-mil centers look to the printed-circuit board like a DIP with leads on 100-mil centers can simplify the problem of designing boards for mixed arrays of SSI chips in DIPs and LSI chips in carriers.



5. Hybrid in carrier. This multilayer, multichip hybrid is mounted in a 48-lead chip-carrier; it takes the place of 16 SSI chips in DIPs. The hybrid can be reworked quickly in response to system redesign, and leads to a dramatic drop in the number of boards in a system.



6. Eye to the future. A four-chip hybrid on a simple one-layer substrate not only is an immediately cost-effective package for SSI chips that lets all leads be directly wired to the board, but can also be replaced by one gate-array chip later without board redesign.

boards could have 60 DIPs and four LSI chips, each on its own chip-carrier. The six boards would be interconnected by a seventh backplane board, which is more expensive. (Alternatively, a mixture of boards that have DIPs only and others with a higher percentage of LSI chips could be used.) In any event, a board cost of at least $150 or $1,050 total would be likely. Cabinet and associated wiring costs are reduced to $1,500, giving a total cost for this configuration of about $3,600.

It should be noted that boards so heavily dominated by DIPs will probably not be able to use the few chip-carriers efficiently. Some sort of an adapter will most likely have to be designed in order to make the chip-carriers look like DIPs as far as the pc board is concerned. Such adapters make the contacts on the board compatible with DIPs (Fig. 4).

14-chip hybrids

Another alternative, the third listed in the table, is to repackage the 10% of the circuit that is on SSI chips into multichip hybrids. The multichip hybrid of Fig. 5, for instance, can be altered or reworked for a quick response to design changes. If these multichip hybrids are then packaged like chip-carriers, a board design that is all chip-carriers results, although it is not all LSI.

The LSI cost again would be $750, and 26 hybrids with 14 chips each at slightly over $45 each would cost $1,170, for a total of $1,920. These would mount on a single 18-by-18-in. multilayer board costing $500 and would have a related cabinet, assembly, wire, and testing cost of $750 for a total of $3,170. This is somewhat less expensive than the previous design; it represents a smaller unit with some possible speed benefits.

The 14-chip hybrids are not likely candidates for conversion to LSI at a later stage of production since each is unique and used only in small annual volumes. Note that the IC cost is very much inflated in this case because of the high cost of the multilayer ceramic hybrids. These could be figured in as interconnection boards, providing the data in parentheses in the table. This is appropriate because it is the interconnection cost, not the IC cost, that is high.

The effect of package size

The design using LSI in 68- to 84-lead chip-carriers and SSI in DIPs can be updated by converting the SSI chip packages to chip-carriers—the fourth option in the table. If package costs for 24-lead chip-carriers were comparable to package costs for the 360 DIPs, the IC costs would remain at $1,050. (This assumed equivalence of cost is expected soon, but is not here yet.) The advantage of this scheme is found in the board and assembly costs.

The CPU using a combination of larger chip-carriers and 24-lead carriers can be mounted on three pc boards of a size comparable to those used for the LSI and DIP option above. Backplane size would be halved, suggesting $525 for board costs and perhaps $1,000 for the reduced assembly and cabinet costs. A CPU cost of just under $2,600 is the result.

The possibility of converting circuits first made of multichip hybrids to LSI chips suggests a fifth option, which turns out to be the most cost-effective: four SSI chips per hybrid package. The cost of the hybrids becomes much lower because a four-chip hybrid in a 68-terminal chip-carrier can use a less expensive package. More importantly, a simple one-surface metallized ceramic substrate and simple wire bonding can be used. There is no need for the multilayer hybrid substrate that is required for the higher-level hybridization.

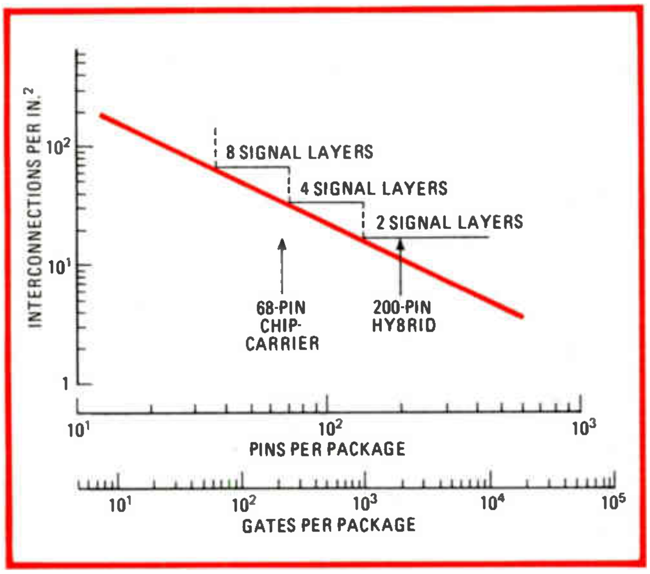
A four-chip hybrid should not cost more than $6.00, giving a $550 cost figure for 90 hybrids. With $750 for the 24 LSI chips, the total IC cost is $1,300. The 114 68-terminal devices could be mounted on 1.5-in. centers on a multilayer board only 16 in. square, which would cost about $400. If the cost of the cabinet, assembly, and wiring stays the same at $750, the total is only $2,450. If the hybrid costs for these four-chip assemblies are allocated to board costs, as in the figures in parentheses in the table, the result again is the usual ratio of IC costs to board costs indicative of an efficient design.

Note that the single metallization pattern on a ceramic hybrid substrate can bring all signal leads of 16-terminal chips to the outer pad contacts of the 68-terminal chip-carrier (Fig. 6). Chips originally packaged in DIPs can have all leads available for external connection. Alternatively, the ceramic substrate can provide interconnections between chips, including deposited resistors and capacitors as required.

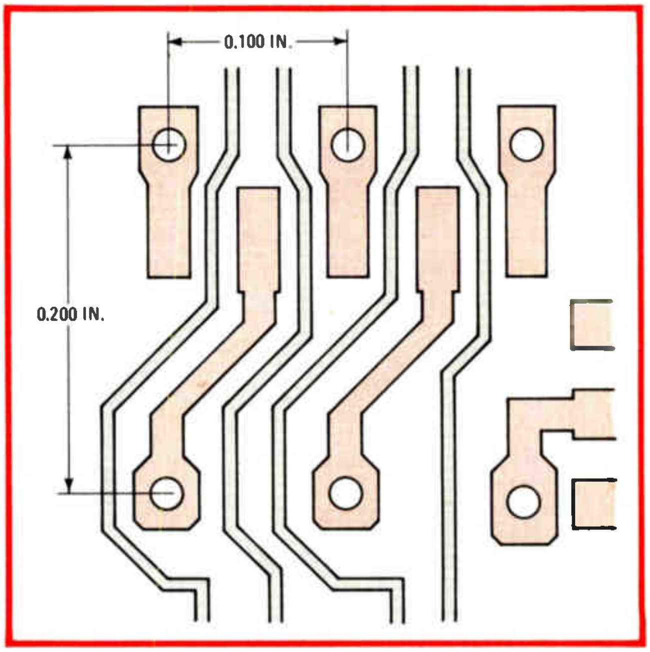
Saving board layers

Charles T. Goddard, head of the hybrid circuit department at Bell Telephone Laboratories, Allentown, Pa., in a paper delivered at the May 1979 Electronic Components Conference, indicated that four signal layers in the pc board may not be enough when 68-lead chip-carriers are used (Fig. 7). But this analysis was based on 40-mil lead spacing. Carriers with 50-mil pad spacing located on 1.5-in. centers do not make eight signal planes necessary. Also, some wiring capability can be provided on the component and reverse-side pad layers of the pc board. A routing layout developed by Steven Pardee, head of computer-aided design at Bell Telephone Laboratories, Whippany, N. J., is one way of providing through-the-pattern routing on a pad layer (Fig. 8). Boards with 68-terminal carriers have been fabricated with just four internal signal layers.

One of the advantages anticipated for a four-chip hybrid is the possibility of substituting gate arrays or custom chips for some of the hybrids. Once the design becomes stable enough to make the conversion to gate arrays worthwhile, substituting single $2.00 chips for the $6.00 hybrids would yield an additional savings of about $300, or almost 15% of the total cost. The important thing here is that no system redesign is needed when it seems advantageous to replace the hybrids with single-chip devices. For example, gate arrays could be substituted three years after the original design work is done, when volume manufacturing is taking place. The four-chip hybrid design is not only slightly cheaper initially than the design that uses single-chip packages, but it offers a cost reduction impossible with the other scheme.



7. Circuit density. Four signal layers on the board are sufficient when 68-pin chip-carriers with leads on 50-mil centers are used; a simpler two-layer board requires the use of costly 200-pin hybrids. The chart is based on a board with an array of 25,000 gates.



8. Room at the pad layer. Staggering the chip-carrier with respect to the via grid allows printed wiring to be put on the same layer with the 50-mil-spaced carrier pads, saving an internal layer. Four-layer boards with 68-lead carriers have been fabricated with this scheme.

If eight chips are mounted on a single square substrate, more leads must be handled on the substrate, a much larger package will be necessary, and there will be less likelihood of converting the hybrid to a single LSI chip. Some five- or six-chip hybrids may occasionally be useful, but the costs seem to favor three- or four-chip units as a design strategy.

These cost figures are merely illustrative; probably each one can be challenged in some respect. It is important to look at the method and to judge whether the data mirrors the economic tradeoffs involved.

This analysis is based on the supposition that the lowest interconnection cost is of principal importance, not the highest packing density. Jedec chip-carriers with 50-mil lead spacing on a pc board with four signal layers offer the lowest cost, particularly if sockets are required for testability and maintenance and if ceramic packages are not required for hermeticity. The future acceptance of AMP Inc.'s very low-cost nonhermetic chip-carrier filled with silicone gel [*Electronics*, March 17, 1977, p. 89] could bias economic analysis in the direction of plastic packages instead of ceramic ones. □

Structured assembly language suits programmers and microprocessors

SMAL/80 combines high-level control mechanisms and easy-to-read mnemonics; preprocessor executes even user-defined macros

by Morris Krieger, *Chromod Associates,* New York, N. Y.*

□ Programmers, being human, prefer high-level languages that isolate them from the confusing detail of machine specifics. But microprocessors do best with assembly language, which stays close to the system level and requires much less memory.

SMAL/80 is a compiled, structured macro-instruction assembly language that satisfies both man and machine. Intended for the 8080, 8085, and Z80 microprocessors, it at present runs under the CP/M and ISIS operating systems. It allows microprocessor programmers to use the same structured, top-down, modular-design concepts they would enjoy when using such structured high-level languages as PL/1, Algol, Pascal, or C.

Three assets

SMAL/80 incorporates three innovations in assembly-language design. First, it has a symbolic notation similar to that used in structured high-level languages. Secondly, it incorporates the three primitive structured-programming control structures: the begin-end, if-then-else, and loop-repeat structures. Finally, SMAL/80 is compiled and not assembled.

The combination of these features makes SMAL/80 different from conventional microprocessor languages. In addition, SMAL/80 incorporates a macro preprocessor that allows a programmer to add a great many high-level-like programming conveniences to a source program; these will be described in detail later.

Appearances

The most obvious characteristics of SMAL/80 are its symbolic notation and indented, structured appearance. Table 1 compares typical SMAL/80 instructions with their Intel equivalents.

In fact, it is somewhat surprising that a symbolic notation such as SMAL/80's has not been more widely used for assembly-language programming, especially since microprocessor manufacturers have long used a similar notation in their publications to explain what their mnemonics mean.

Zilog, for example, in its Z80 manuals, prints a column of symbolic notation alongside a descriptive listing of its mnemonics to explain the action of each instruction:

```
LD HL, (nn)          H ← (nn+1)
                     L ← (nn)
```

Both notations say the same thing: "Transfer the 16-bit number contained at memory addresses nn+1 and nn into the HL register pair." It is unnecessary to be a programmer or even especially familiar with computers to appreciate that the symbolic notation on the right shows more clearly what the function of the instruction is. The SMAL/80 instruction for this particular operation is:

```
HL = M(address)
```

Of equal importance are SMAL/80's three primitive control structures (Fig. 1 shows two of them). These can be combined with or nested within each other up to the limit of available memory. The structures give a programmer logical functional blocks to design with, following exactly the same principles used to develop programs in structured high-level languages.

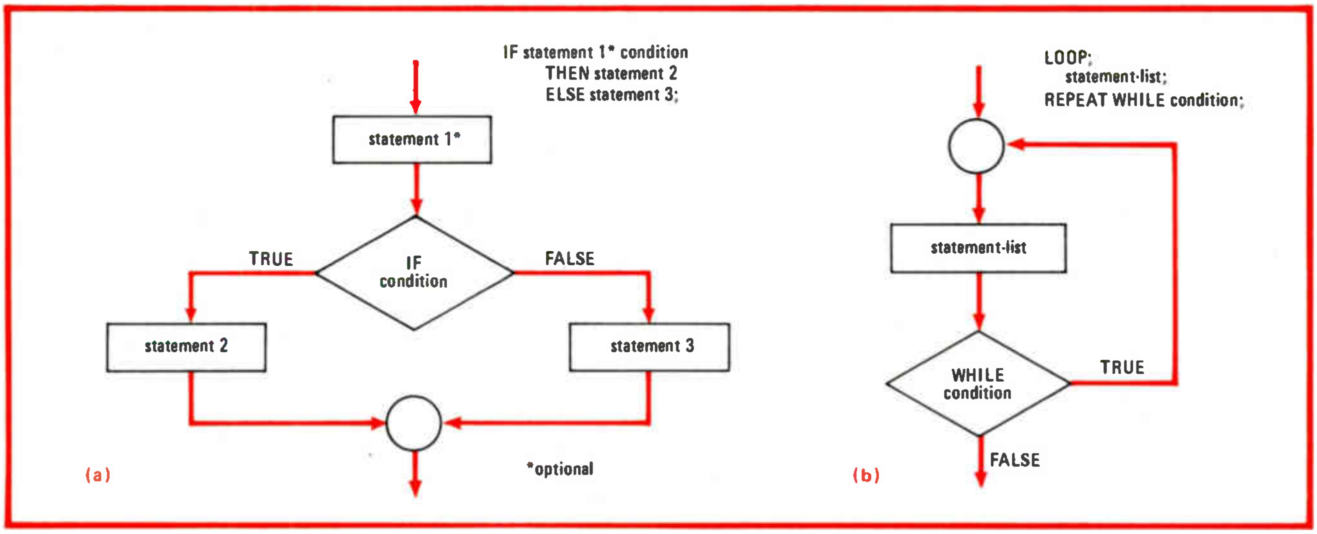
Structured programming

It is perfectly feasible to write a SMAL/80 program in which the control structures are ignored and the only change is the substitution of SMAL/80 notation for the conventional Intel or Zilog mnemonics. But to use SMAL/80 in this way is to miss the point entirely. To repeat, the rationale of SMAL/80 and its predecessors (see "A short history of SMAL," p. 120) is that they enable microprocessor programmers to use the same structured programming and modular design concepts that have proved so valuable in the writing of high-level language programs. SMAL/80 and these concepts should therefore be considered inseparable.

It is a basic tenet of these concepts that programs should be designed in a top-down manner; that is, a programmer ought to begin with a general specification and then expand upon it in greater detail until the actual program statements are written. The writing of these statements should come as the very last step in the design process—not the first step as it often is with a great many programmers. If the programmer has thought out carefully what the program is to do, then the writing of the code will be an almost trivial last step in the overall procedure.

These ideas should not be new to engineers at all. An engineer follows precisely the same procedure when

*The distribution of SMAL/80 is now being handled exclusively by the software products group of Yourdon Inc., 1133 Avenue of the Americas, New York, N. Y. 10036.



1. Structures. Two of the most beneficial of SMAL/80's structured control constructs are the if-then-else (a) and the loop-repeat-while (b). In the latter, statement-list refers to one statement or a group, and it may include next or break statements for exit control.

TYPICAL SMAL/80 INSTRUCTIONS

SMAL/80	Standard format	
Data movement		
reg1 = reg2	MOV	reg1, reg2
A = M(xreg)	LDAX	xreg
M(xreg) = A	STAX	xreg
HL = M(address)	LHLD	address
M(address) = HL	SHLD	address
SP = HL	SPHL	
HL <=> M(SP)	XTHL	
PUSH HL	PUSH	H
HL = POP	POP	H
DE <=> HL	XCHG	
Data manipulation		
++reg	INC	reg
++xreg	INX	xreg
HL = HL + HL	DAD	H
CY = NOT CY	CMC	
A : data	CPI	data
A = A AND reg	ANA	reg
A = A OR reg	ORA	reg
A = A XOR reg	XRA	reg
A = A + data + CY	ACI	data
ROTATE A RIGHT data	RRC	data times
Control		
GOTO address	JMP	address
GOTO M(HL)	PCHL	
Peripherals and pseudo-operations		
ENABLE	EI	
DISABLE	DI	
A = IN(data)	IN	data
OUT(data) = A	OUT	data
ORIGIN	ORG	address
RESERVE address	DS	address
WORD address-list	DW	address-list
BYTE data-list	DB	data-list
TITLE = char-string		
MODULE = char-string		

designing any electronic circuit; he proceeds from a general specification to the selection of specific integrated circuits. If the design has been well thought out, the decision which chips to use will be obvious.

A CRC example

To illustrate structured programming concepts, a cyclical redundancy check routine will be used (Fig. 2). This is an error-checking program used to determine whether any faults have occurred during the transmission of data between a computer and one of its peripherals or between two computer installations. It has two virtues. It reveals whether a message has been garbled during transmission (though it cannot determine which bits are in error).

Also, if the data is being transmitted through parallel lines such as those between a computer and a disk drive, the CRC will reveal whether any of the lines are not functioning. Other commonly used error-detection techniques such as parity checking or check-summing may not reveal a dead transmission line.

The cyclical redundancy check derives a CRC value that is unique for the particular block of data being transmitted. The routine in Fig. 2 uses a function that is applied recursively to the data and a series of intermediate CRC values.

The routine

One of the registers in the central processing unit (the C register) is set aside to hold the CRC value. This so-called CRC register is set initially to 0 while the value of the second, fourth, and seventh bits of the CRC value are summed in another register (the D or toggle register). The toggle register is then set either to 1 or 0 depending upon whether these 3 bits sum to 1 or 0. Initially, this makes the toggle register a 0, of course.

The toggle register is then exclusive-ORed with the first byte of the message. This message byte and the CRC value are then jointly shifted 1 bit to the right. Consequently, the lowest-order bit in the result of this exclusive-OR operation is now transferred into the high-

A short history of SMAL

SMAL/80 originated as SMAL, an 8080 language developed at Bell Laboratories in 1974 by Charles Popper and described in the IEEE Computer Society Compcon 74 Fall conference proceedings. Popper was originally dissatisfied with the assembly-language mnemonics that had been selected by Intel for writing 8008 programs. He wondered why the changes should be limited to the mnemonics. Why not adopt an entirely different notation, he thought, a symbolic notation similar to that used for such high-level languages as Algol and C? (At this time C was rapidly consolidating its position at Bell Laboratories as the preferred programming language.) Why not, in fact, design an entirely new language, one that would also include control structures similar to those used in Algol and C?

These ideas resulted in the original SMAL, which was eventually designed for the 8080, not the 8008. In about three weeks' time, Popper had implemented his ideas in the form of a Snobol4 program that ran on an IBM 370/168. The Snobol4 program translated Popper's SMAL notation and structured-programming constructs into standard Intel 8080 assembly code that could then be assembled into 8080 object code.

Before he left Bell Laboratories in 1975, Popper began work on SMAL2, which was SMAL modified to include many C-like features. SMAL2 has since become the standard 8080 language at the labs. SMAL2 and SMAL/80, while obviously close cousins, are quite distinct from one another. SMAL2 was designed to be as compatible with C as possible and to run under Bell Laboratories' UNIX operating system. SMAL/80, on the other hand, was designed to be a free-standing language for the world of 8080/8085 users outside of Bell Laboratories.

Studies made on the original SMAL language at Bell Laboratories showed that SMAL programs required less memory and ran about 5% faster than comparable assembly-language programs because of their superior organization. Add the fact that SMAL programmers spend less time testing their programs and hunting down and eliminating bugs, and the differences in efficiency between conventional assembly-language programming and SMAL programming become even more significant. And these same advantages apply to SMAL2 and SMAL/80 programs, of course. The experience of those who have switched from writing conventional assembly-language programs to writing SMAL, SMAL2, or SMAL/80 programs has been that the symbolic notation and the constructs allow them to express their ideas more naturally and more quickly and to convert these ideas into code more easily.

est-order position of the CRC register.

This procedure is repeated recursively for all 8 bits of the first message byte. As each bit is transferred into the CRC register, it bumps the previously transferred bits to the right. The result is a new CRC value that depends on the first byte of the message. The entire process is then repeated for the remaining bytes of the message.

What finally ends up in the CRC register is a unique 8-bit value that depends on the value of each byte in the message and the peculiar way these characters have been combined with the intermediate CRC values.

The final CRC value is appended to the end of the transmitted message. At the other end of the transmission line, a CRC value is derived in exactly the same way from the message and compared with the transmitted CRC value. If the message has been transmitted without error, they should be identical. If they are different, the message may be retransmitted and the same cyclical redundancy check performed.

Suppose a programmer now wants to transform this algorithm into a SMAL/80 program. In order to do so, a series of pseudocoded programs of increasing complexity might have to be written.

Each would have the form of a structured SMAL/80 program, but be written in plain English. A first pass at writing the program might look like this:

```
CRC calculation routine:
    initialize registers;
    LOOP;
        add values of 2nd, 4th, and 7th bits in CRC
        register;
        set toggle register according to parity of
        result;
        exclusive-OR value of toggle register with
        message byte;
        shift message byte and CRC 1 bit to right;
    REPEAT WHILE additional chars remain to be
    transmitted;
    return to main routine with CRC value;
```

As mentioned, the programmer may expand upon these statements in the form of increasingly detailed pseudo-coded programs until the program looks like this:

```
main CRC routine:
    set address of first character in message;
    set length of message;
    CALL subroutine to calculate CRC value;
    save CRC value;
    return to main program;
            .
            .
            .
            .
CRC calculation routine:
    assign CPU registers to hold intermediate values;
    initialize CRC register to zero;
    LOOP;
        set number of loop repetitions;
        transfer message char to CPU register;
        set pointer to fetch next char in message;
        LOOP;
        initialize toggle register to zero;
        check bit 2 of CRC value;
        IF it is a 1 THEN
          increment value in toggle register;
        check bit 4 of CRC value;
        IF it is a 1 THEN
          increment value in toggle register;
```

```
ORIGIN X'100'                        /* set origin, but use monitor stack */;

CRCtest:
    HL = MESSAGE                     /* set beginning addr */;
    DE = 14                          /* set length */;
    CALL CRCcalc                     /* calculate CRC(C) */;
    M(HL) = C                        /* store result */;
RETURN;                              /* return to monitor */

MESSAGE: BYTE 'SAMPLE MESSAGE';

CRChere: RESERVE 1                   /* computed value should be X'9C' */;

CRCcalc:                             /* compute 8-bit CRC over given message—
                                     upon entry    HL = beginning addr of message
                                                   DE = length of message
                                     upon exit      C = CRC
                                                   HL = end of message + 1
                                                   DE = 0 */;
    PUSH AF                          /* save work registers */;
    C = 0                            /* initialize CRC */;
    LOOP                             /* over message bytes */;
        PUSH DE                      /* save aux work registers */;
        E = 8                        /* set bits/byte control */;
        B = M(HL)                    /* get message byte */;
        ++HL                         /* advance pointer */;
        LOOP                         /* over bits in byte */;
            D = 0                    /* initialize toggle register to 'no' */;
            A = C;
            A = A AND X'04'          /* bit 2 of CRC set? */;
            IF NOT ZERO /* if 'yes' */ THEN
                ++D                  /* advance toggle register */;
            A = C;
            A = A AND X'10'          /* bit 4 of CRC set? */;
            IF NOT ZERO /* if 'yes' */ THEN
                ++D                  /* advance toggle register */;
            A = C;
            A = A OR A               /* bit 7 of CRC set? */;
            IF NEG /* if 'yes' */ THEN
                ++D                  /* advance toggle register */;
            A = D;
            A = A AND 1              /* isolate bit 0 of toggle register */;
            A = A XOR B              /* apply to bit 0 of message byte */;
            ROTATE A RIGHT 1         /* rotate byte into CY. . . */;
            B = A;
            A = C;
            ROTATE ACY RIGHT 1       /* . . . and CY into CRC */;
            C = A;
        REPEAT WHILE -- E NOT ZERO;
        DE = POP                     /* retrieve aux work register */;
        -- DE;
        A = D;
        A = A OR E;                  /* done? */
    REPEAT WHILE NOT ZERO            /* repeat while 'no' */;
    AF = POP                         /* retrieve work registers */;
    RETURN;
END PROGRAM X'100';
```

2. CRC program. This SMAL/80 routine performs a cyclic redundancy check. It can be derived by writing the program in a series of pseudo-coded programs of increasing complexity. It looks like a high-level-language program but executes much faster.

```
            check bit 7 of CRC value;
            IF it is a 1 THEN
              increment value in toggle register;
              mask off all but bit 0 of toggle register;
            exclusive-OR bit 0 in toggle register with
            message byte;
            shift message byte and CRC 1 bit to right;
            has inner loop been repeated eight times?;
        REPEAT WHILE no;
        are there more characters to be transmitted?
REPEAT WHILE yes;
return to calling routine;
```

The final SMAL/80 program is shown in Fig. 2. With this introduction, the reader should not find it too difficult to follow the actual program statements.

The value of SMAL/80 is greatly enhanced by its macro preprocessor. The preprocessor can: nest macroinstructions without limit (up to the capacity of available memory); expand macros conditionally, even when they are embedded within other macros; incorporate variables into macros; and write recursive macros.

Like any preprocessor, all that the SMAL/80 preprocessor does is translate one set of symbols into another set of symbols. In SMAL/80's case, the symbols are the complete set of ASCII characters and control codes. At the most elementary level, the preprocessor allows a programmer to replace standard SMAL/80 notation with a notation of his or her own devising. For instance, a simple and obvious move might be to replace the SMAL/80 assignment operator (=) with any other assignment symbol such as ← or :=.

French, too

More exotic changes can also be made, such as changing all the keywords of SMAL/80 from English into their French equivalents. When that is done, statements in English like:

```
REPEAT WHILE [A = D; A = A OR A] NOT ZERO;
```

become statements in French like:

```
REPETER PENDANT [A = D; A = A OU A] PAS ZERO;
```

Incidentally this statement combines three separate statements into one, which certainly makes the intent of the program clearer. The two statements within the brackets set up a condition—a flag—that the third statement can test for a zero or nonzero status.

On an even higher level, a programmer may invent entirely new instructions that enable him, through appropriate macro calls in a source program, to write instructions that are otherwise impossible to write in the standard SMAL/80 language.

User-defined

For example, 8080 and 8085 microprocessors lack the Z80's block move instruction. However, by writing the following macro definition:

```
.DEFINE
BLOCK MOVE;
AS
PUSH AF;
LOOP;
        A = M(HL);
        M(DE) = A;
        ++DE;
        ++HL;
REPEAT WHILE[--BC; A=B; A=A OR C]NOT ZERO;
AF = POP;
ENDMACRO;
```

block move instructions in 8080 or 8085 source programs will execute just as if a Z80 were used—albeit without the Z80's execution efficiency. Features of other microprocessors may also be simulated in SMAL/80 source programs. Macros can be written that will allow SMAL/80 to simulate the memory-to-memory transfers of the 6800 and 6502, for example.

In fact, a package of Z80 macros are provided with the 8080/8085 version of SMAL/80 that converts it into a full Z80 language. When these macros have been expanded into Z80 operation codes and compiled, the Z80 sees an ordinary Z80 source program, the instructions of which it proceeds to execute as it would any other Z80 program.

For more sophisticated applications, it is possible to write SMAL/80 macros that allow the language to emulate the control structures of such high-level languages as PL/1, Pascal, and C. A programmer writing machine-level routines for incorporation into a Pascal program can, by writing the appropriate macros, convert the SMAL/80 structures into Pascal-like structures. The machine-level program can then be written in exactly the same way as the Pascal program. For example, Pascal has a WHILE construct that allows a programmer to write loops like:

```
WHILE (condition) DO
  statement(s);
```

The programmer can incorporate this Pascal construct into SMAL/80 source programs by writing the following macro definition:

```
.DEFINE
WHILE {condition} DO
          {statements};
AS
LOOP;
      IF NOT {condition} BREAK;
      {statements};
REPEAT;
ENDMACRO;
```

The words "condition" and "statements" in this macro definition are simply placeholders; they can be replaced by any legal SMAL/80 instruction, statement, symbolic name, constant, variable, or macro call whatever. As another example, the programmer can write the following SMAL/80 source code statements:

```
WHILE (A == M(addr)) DO
    statement(s);
```

with the symbol == functioning as an equals sign, as it does in the C language. The use of this equality relation requires another macro definition (the one for ==), so this particular example shows how one macro can be embedded within another.

However, not every embedded macro may nest properly. There may be undesirable side effects, but it is beyond the scope of this article to describe the precise rules for writing SMAL/80 macros.

Adding variables

The ability to incorporate variables into macros also allows a programmer to do such things as write subroutine calls having arguments, just as he does in a high-level program. A call to a subroutine may be written as follows:

```
CALL subr(arguments);
```

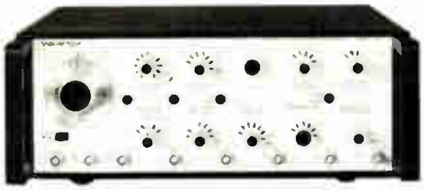
After writing the following macro definition, "arguments" may be any list of statements and "subr" the name of a subroutine. The following definition would suffice:

```
.DEFINE
CALL {subr}({arguments});
AS
{arguments};
CALL {subr};
ENDMACRO;
```

Best of both worlds

At the highest level of all, a programmer may invent a special-purpose high-level-like language—a process-control language, for example—tailor-made for particular requirements. It is entirely conceivable that complete routines (assuming they are short enough to be used efficiently as in-line code) can be written in the form of macros, which can then be called in a program merely by writing their names. The programmer could as a result have the best of two worlds. He or she would be able to combine in one language all the programming conveniences of a high-level language and all the speed and efficiency that is inherent in a conventional assembly language. □

There are two kinds of people in the world.



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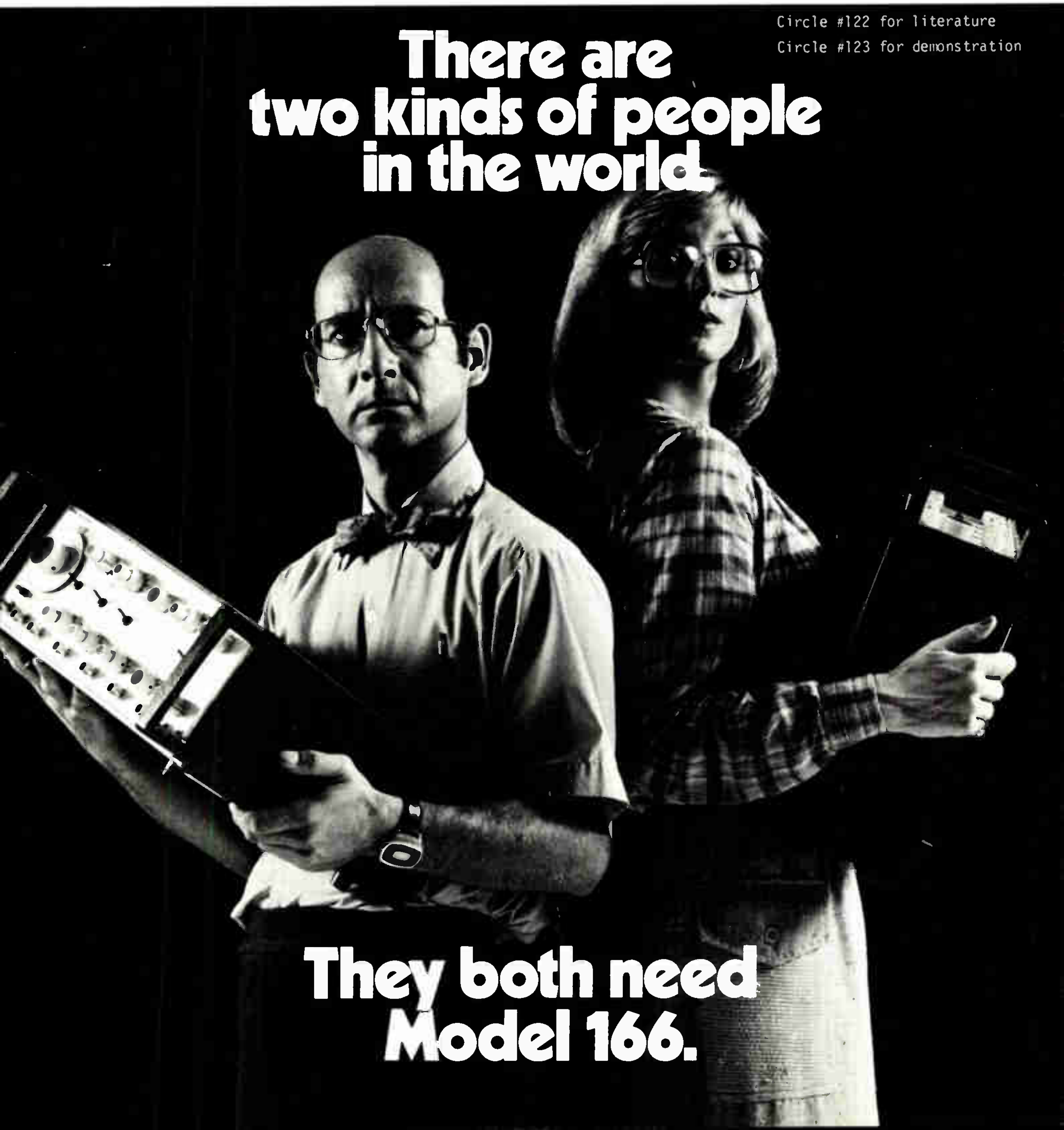
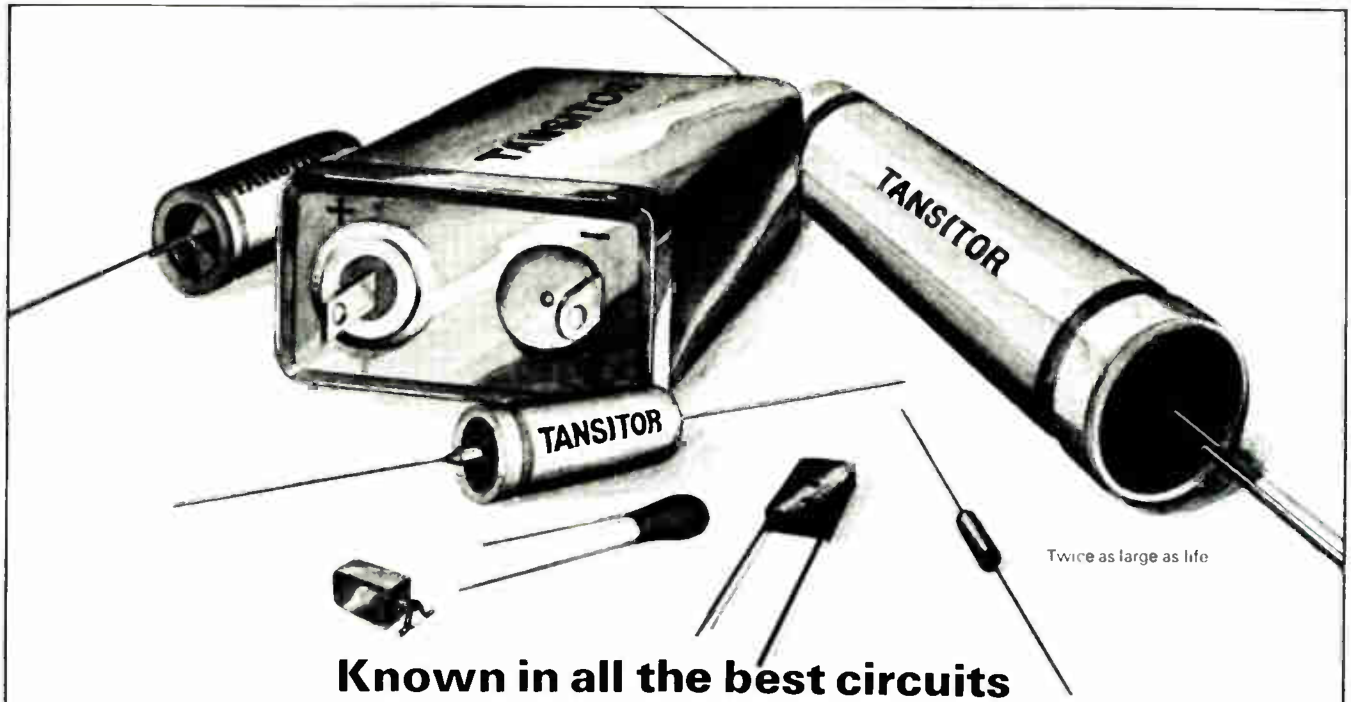


They both need Model 166.



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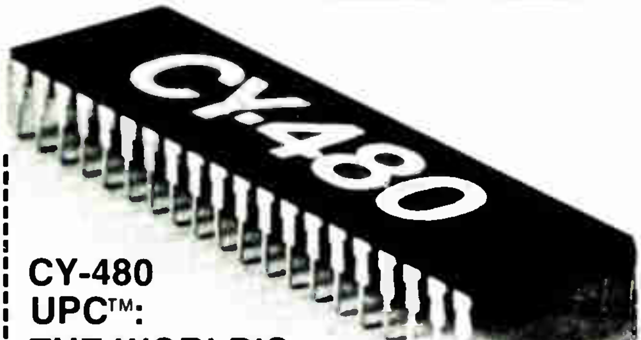

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Autocorrecting driver rights pulse polarity

by Shlomo Talmor
Hartman Systems, Huntington Station, N. Y.

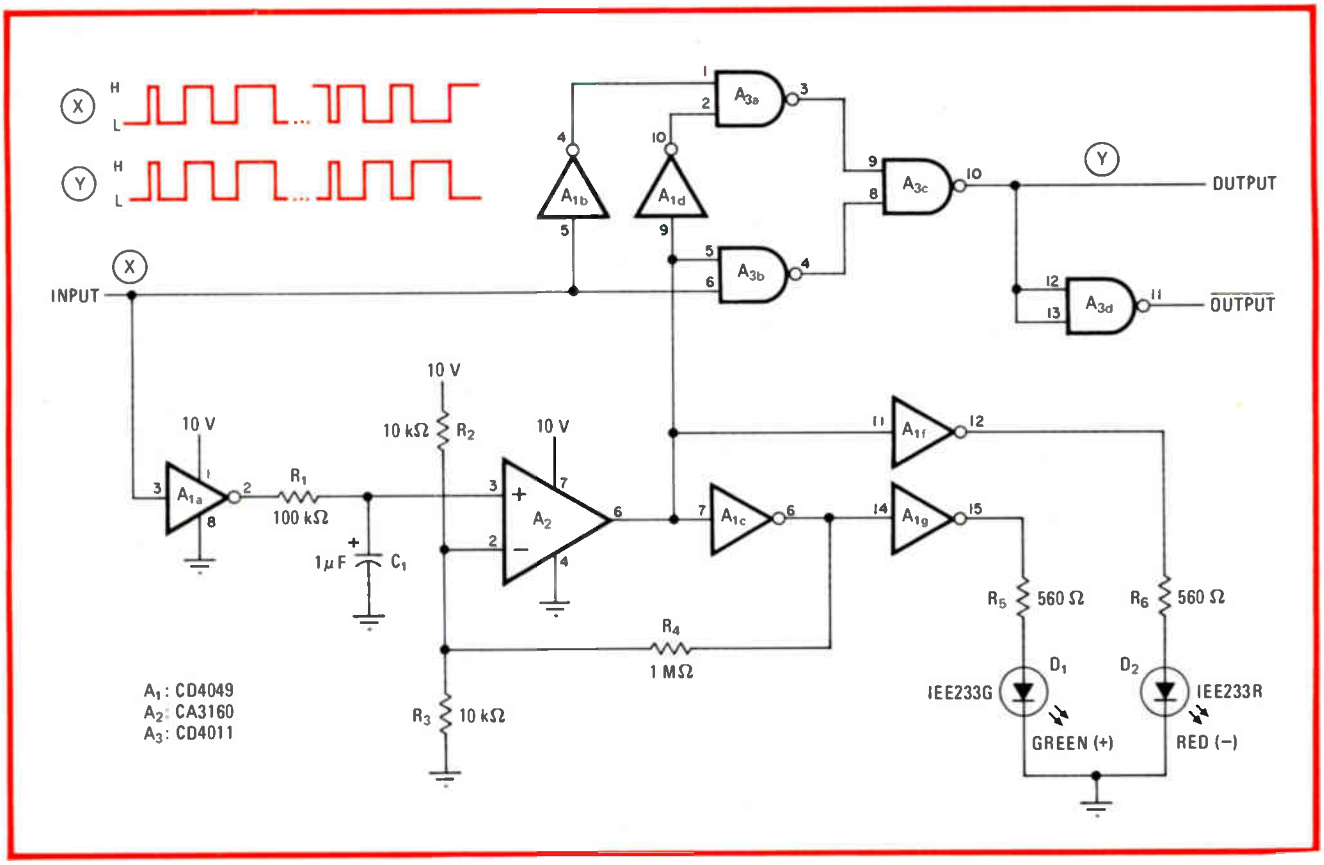
This circuit provides positive-going output pulses for corresponding input signals of either polarity without the need for any manual intervention (that is, polarity switches). Utilizing a simple RC integrator, the unit automatically propagates positive-going signals having a duty cycle of less than 50% through to the output and inverts signals that have a duty cycle of greater than 50%, or are negative-going. The circuit is particularly useful in instrumentation and test-facility applications, where the polarity of the signal emanating from a port is often both positive- and negative-going at different stages of a complicated test sequence.

As shown in the figure, input pulses having a width and rate in the range of 1 microsecond to 1 millisecond are applied through inverter A_{1a} to integrator R_1C_1, thereby developing a dc voltage across the capacitor. Thus, operational amplifier A_2 goes high for positive-going input pulses having a duty cycle of less than 50%. A_{1b} and A_{1d}, along with NAND gates A_{3a} to A_{3c}, therefore propagate the input signal through to the output without an inversion.

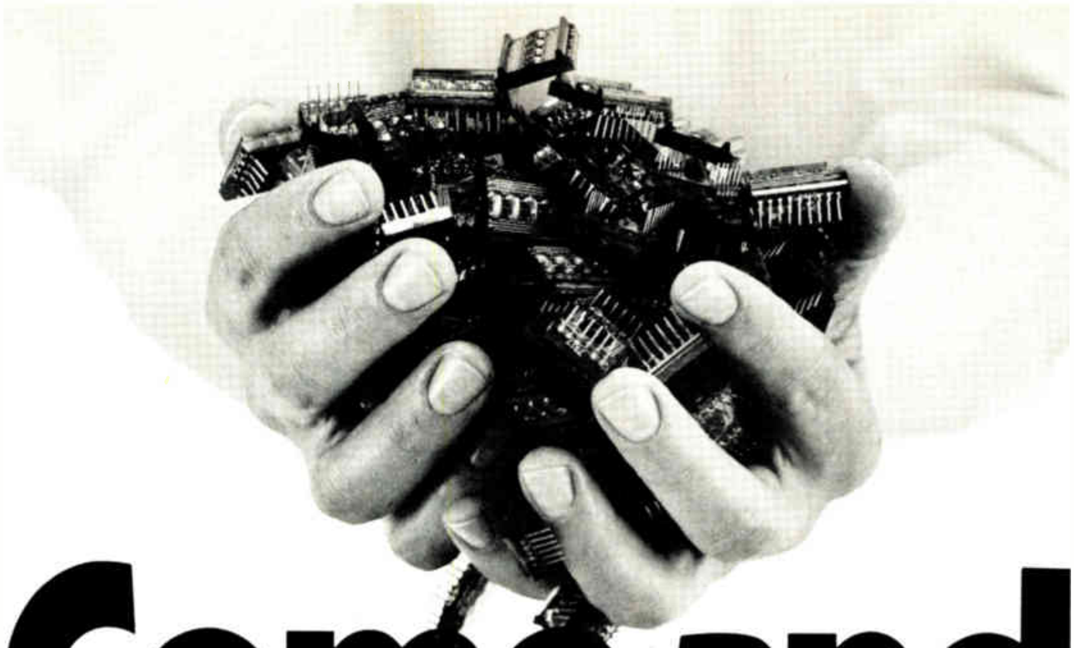
If the duty cycle is greater than 50%, or if the incoming pulses are negative-going, the voltage developed on the integrating capacitor will be below 5 volts, which is the potential applied to the inverting input, and A_2 goes low. A_{1b}, A_{1d}, and A_{3a} to A_{3c} then act to invert any negative-going wave at the input to a positive one at the output and vice versa. In the case where the duty cycle is 50%, inverter A_{1c} provides the necessary hysteresis to A_2 for proper switching.

Light-emitting diodes D_1 and D_2, with A_{1f} and A_{1g}, provide visual indication of pulse polarity. Both the red and green diodes will light softly when the input signal has a duty cycle approximating 50%.

The range of the pulse width handled can be extended, at the expense of a lower rate, by increasing R_1. The response time of the circuit will of course be lowered. The supply voltage can vary from 5 to 15 volts, but if it is less than 7.5 V, a 15-kilohm resistor should be placed in series with pin 6 of A_2 in order to properly drive the rest of the circuit. □



Switch. Three-chip driver accommodates both positive- and negative-going input signals, converting them both into positive-going output. Circuit propagates positive-going signals having a duty cycle less than 50% through to the output while inverting all other signals.



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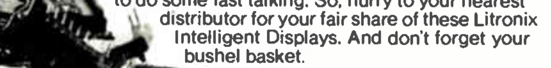

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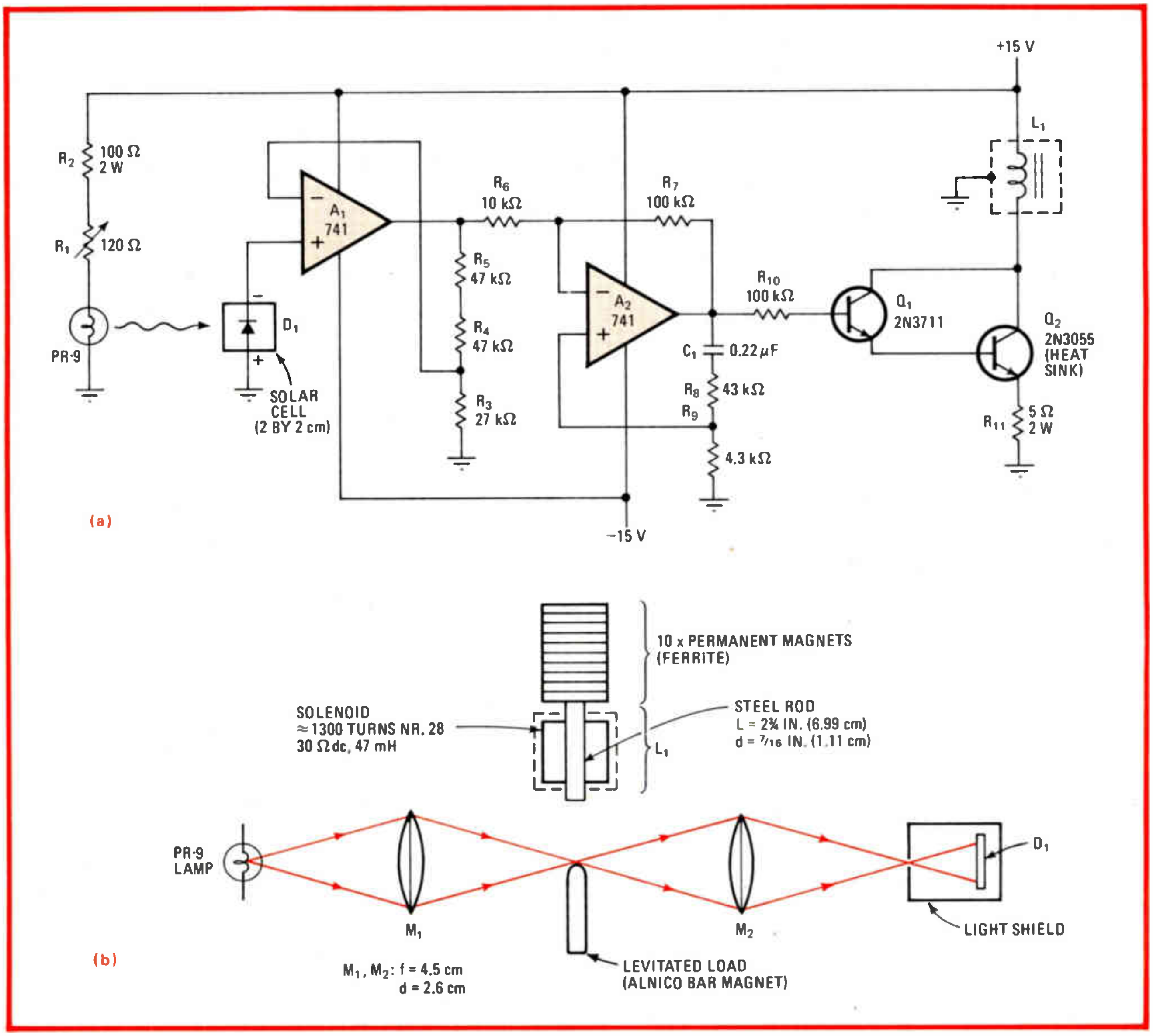
Magnetic levitator suspends small objects

by Bob Leser
Desert Technology, Las Cruces, N. M.

This circuit is a modern solution to the problem of securing frictionless bearings for small rotors and levitating small magnetic objects a few millimeters in space. Operational amplifiers replace the tubes used in earlier approaches, and an optical arrangement replaces the radio-frequency induction circuit originally used to position the object.

Potentiometer R_1 (a) sets the current through the PR9 lamp and thus its brightness and the gain of the position-sensing circuit. R_1 thus provides a fine adjustment of the position of the magnetic object that is suspended beneath the levitation coil L_1. The optical position-sensing circuitry (b), which should be mounted horizontally under L_1 if possible, includes two lenses to focus the beam via the levitated load to solar cell (photodetector) D_1. The light shield, with an aperture of approximately 3 millimeters, effectively eliminates background light. The suggested focal lengths and lens diameters are shown; as a check on the optics system, the beam should be aligned to yield a short-circuit current of 4 to 25 microamperes in D_1.

As for the basic circuitry, D_1's output is amplified by about 5 by operational amplifier A_1 and is then introduced to A_2, which is the all-important servo-loop stage. C_1, R_8, and R_9 provide positive feedback of the high-frequency components of the positioning signal. The stage thus generates the voltage derivative of the amp's output, preventing oscillations in the closed loop that would otherwise occur because of the lack of damping in



Rising rotors. Levitator circuit (a) suspends 1-in. steel spheres up to 2½ millimeters off reference surface. Optical arrangement (b) sets object distance. Details of levitation coil construction are outlined. Permanent magnets set ultimate levitation range.

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the position servo portion of the circuit. Any closed-loop oscillation will be manifest as vibration of the levitated object.

Output stage Q_1 to Q_2 is a discrete darlington pair that drives L_1. The coil itself has 1,300 turns around a steel rod 2.75 inches long and 7/16 in. in diameter. A stack of 10 small permanent magnets atop the coil provides a bias field extending the range of levitation beyond that which would be normally attained. The coil is surrounded by a grounded shield to reduce the amount of stray coupling to the op amp inputs.

The most stable closed-loop condition is set by adjusting Q_2's collector voltage to about 7.5 volts by altering the levitation distance between the sensing optics and L_1. Levitation distances in this circuit range from about 20 millimeters for a small Alnico bar magnet to 2½ mm for a steel ball with a diameter of 1 in. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.

C-MOS counter sets divider's modulus

by Arie Shavit
Kiriat Tivon, Israel

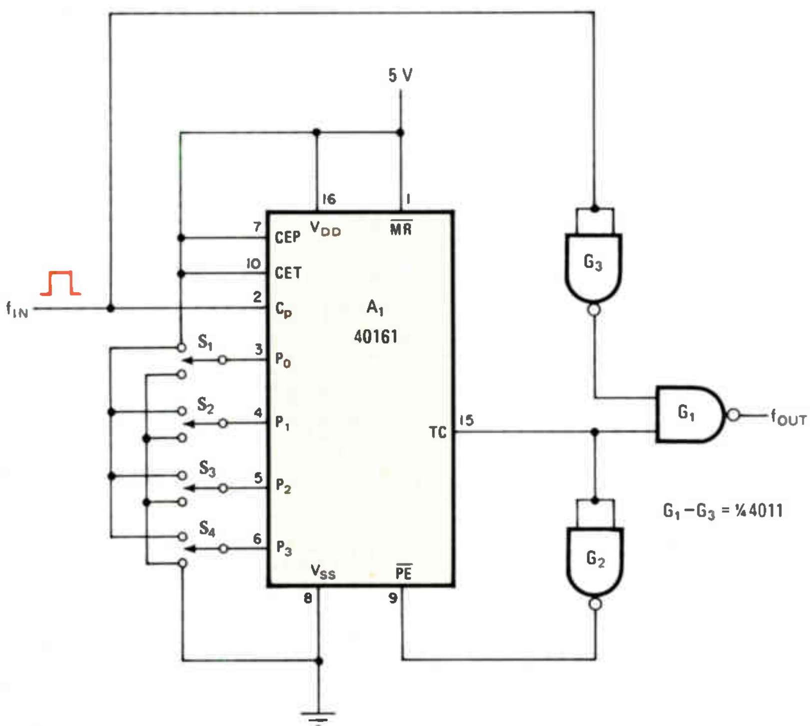
The cost and power consumption of Albing's C-MOS variable-modulo divider[1] can be reduced even further with this circuit, which uses logic gates and four low-cost binary switches to replace one counter and the multiple-pole selector, respectively. Although the counter's modulus is set with the binary elements, thereby sacrificing the convenience of ordering up values in the familiar decimal form, the ease of interfacing the counter to microprocessor-based control systems is immensely enhanced. Divider ratios of from 1 to 16 can be selected.

The 40161 synchronous binary counter, A_1, which has parallel-load capability, is stepped by input frequency f_{in}, as shown in (a). Switches S_1–S_4 set the binary representation of $16-n$ at the parallel-load inputs P_0–P_3, where n is the desired divider ratio, as shown in (b).

Output pin TC of A_1 moves high after n cycles of f_{in}. Thus the output signal from gate G_1 is a pulse of short duration having a frequency of $f_{out} = f_{in}/n$. TC is then inverted by gate G_2 and used to reset the counter.

Gate G_3 comes into play if a modulus of 1 is set. Under these conditions, TC remains high and f_{in} serves to gate itself to the output. □

References
1. Bradley Albing, "C-MOS counter-decoder pair sets divider's modulus," Aug. 30, 1979, p. 140.



(a)

Binary code				Divider ratio n
S_4	S_3	S_2	S_1	
1	1	1	1	1
1	1	1	0	2
1	1	0	1	3
1	1	0	0	4
1	0	1	1	5
1	0	1	0	6
1	0	0	1	7
1	0	0	0	8
0	1	1	1	9
0	1	1	0	10
0	1	0	1	11
0	1	0	0	12
0	0	1	1	13
0	0	1	0	14
0	0	0	1	15
0	0	0	0	16

(b)

Binary breakup. Single counter and three gates simplify design of variable-modulo divider (a). Binary switches S_1–S_4 set counter to $16-n$, where n is desired divider ratio (b). Output of gate G_1 is a pulse with a frequency equal to $f_{out} = f_{in}/n$, for $1 \leq n \leq 16$.

Partial RAMs can fill today's memory boards

Bit-mapping hardware rescues mostly good random-access memory chips for use in designs that will later switch to fully functional devices

by Jerry Donaldson, *Teradyne Inc., Western Technical Center, Sunnyvale, Calif.*

☐ When any new generation of random-access memories starts to roll off the production line, the yield of good devices is usually low until the bugs in the process can be found and squashed. Even on established lines there are usually some dice from a wafer that have a few defective columns or rows.

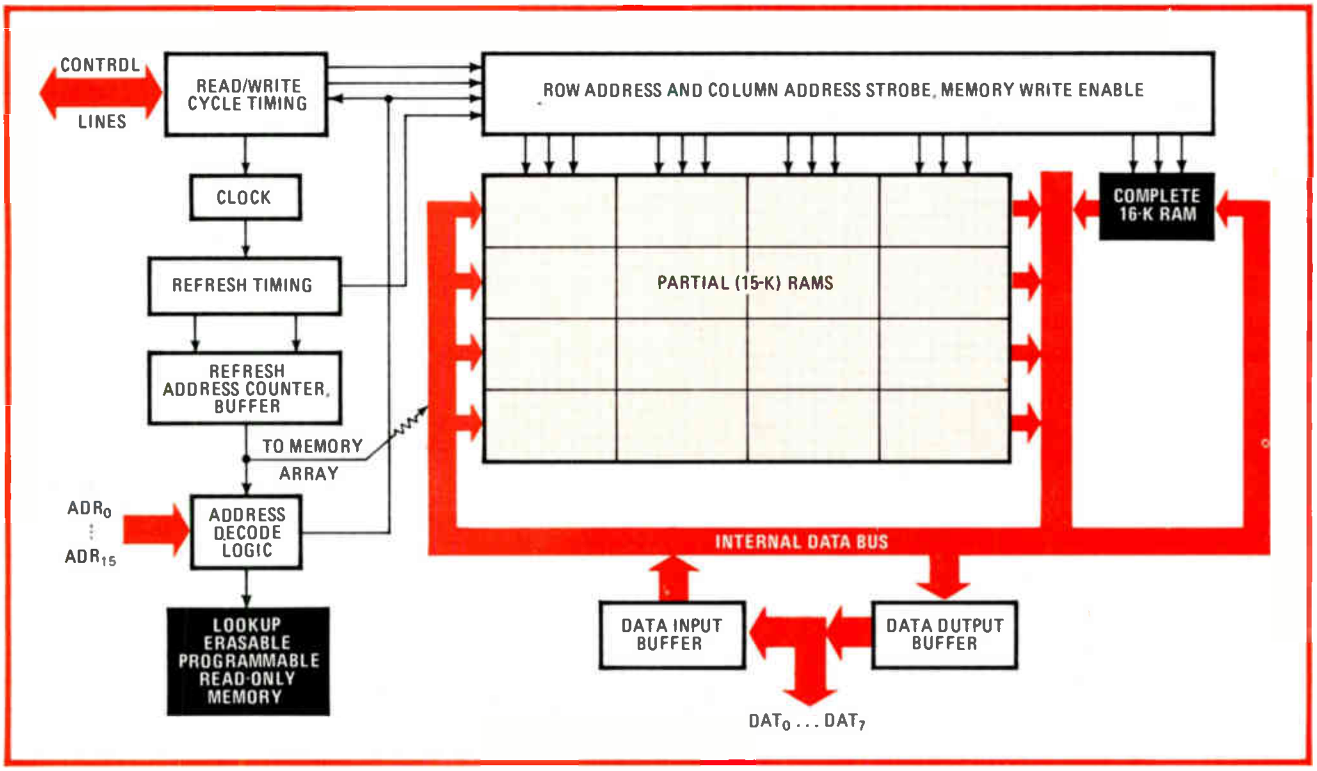
To improve the yield of their production lines, semiconductor manufacturers have taken to packaging devices with less than the total designed storage—devices usually referred to as partials. Partial 16-K dynamic RAMs are already available from some manufacturers, and the first volume appearance of the 64-K devices will probably be in the form of partials. Indeed, one manufacturer has already given the specifications for its 32-K partial.

Far from being inferior parts whose operation is questionable, these parts are tested to the same functional standards as whole devices. Such RAMs enable memory board builders to bring dependable products to market in the earlier stages of a memory family's development or when full-storage parts are scarce.

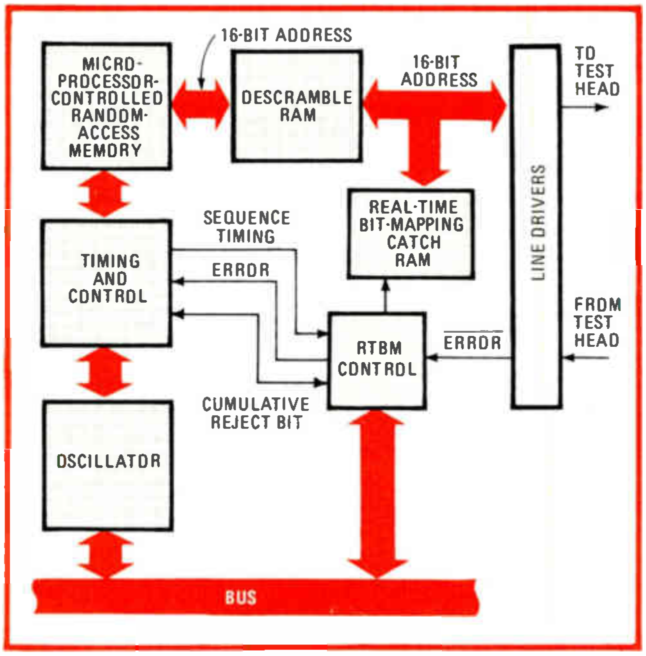
In evidence

There are many reliable memory board designs in which partials can be used, but one should suffice as an example of their efficiency. Figure 1 shows the general layout of a memory board that employs partial 16-K RAMs—chips that have 15 K of usable storage. Added to the on-board logic and the partial parts are a whole 16-K RAM and a 16-K erasable programmable read-only memory.

The E-PROM and whole RAM are added to store the addresses and data, respectively, of the nonfunctioning locations in the partial devices. After the board is loaded



1. Partial devices, full capacity. A memory with 32 kilobytes of storage can be built with 16 15-K partial dynamic RAMs by adding a 16-K E-PROM and a full 16-K RAM. The E-PROM stores failed locations in the partials; the extra RAM provides substitutes for those locations.

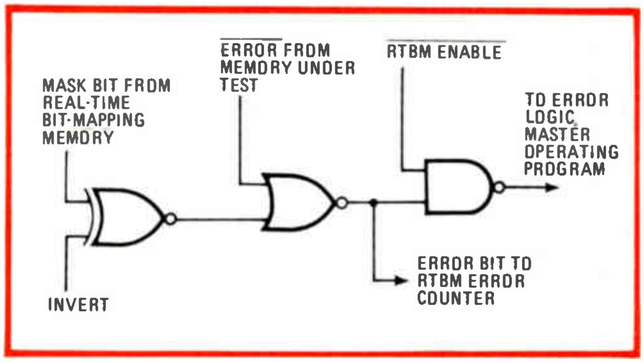


2. RTBM. Adding real-time bit-mapping hardware—the catch RAM and control logic board—to the J387 test system enables thorough testing of partials. At the control logic's command, the RAM stores 1s in locations corresponding to failed bits in memory under test.

with partials, it is tested; the nonfunctioning addresses found by testing are burned into the E-PROM, forming a lookup table. The E-PROM is then plugged into the memory board.

In operation, when an address is given to the memory board, the board logic compares the address to those in the lookup table. If it finds the address there, the extra 16-K RAM is enabled. Data is then written into or read from a row or column in the extra RAM corresponding to the address of a failing row or column in the partial memory.

With this method, the partial memory bank can have a combination of 128 rows and columns containing failing cells, or 8 per device. Since the extra RAM is on the data bus, the board can handle a full 256 K. Later—for example, if the cost and supply of whole RAMs becomes more favorable—the partials can be replaced with them and the lookup logic inactivated.



3. Error-processing logic. NAND gate at right hides error signal when RTBM is enabled so that pattern processor keeps running. To count bit errors, 1s from masked catch RAM are inverted and combined with 0s in place of error signal from memory under test.

As indicated earlier, partial devices for use in such designs are not operationally inferior. Semiconductor manufacturers subject them to full functional testing by means of special hardware and software; a RAM that fails as a full-storage device does not as a matter of course become a partial.

When to look

Usable partial memories are identified at the wafer-sorting stage using real-time bit-mapping hardware (provided as an option to Teradyne's J387 memory test system) and a software program that permits recording and counting of the number and location of bit failures. The hardware-software combination results in an automatic testing scheme that does not require special training for the tester operator. Further, the additional time required to perform the test for partials is low, so that the devices can be offered at reasonable, competitive prices.

The hardware needed for real-time bit mapping (RTBM) consists of two printed-circuit boards that are inserted into the M385-04 pattern generator of the J387 test system. One of the boards contains the control logic for RTBM and a counter used in determining the number of rows or columns that have failed bits. The other is a RAM board called the catch RAM because its function is to store the location of failing bits in the memory under test. Figure 2 shows how these boards interface with the pattern processor.

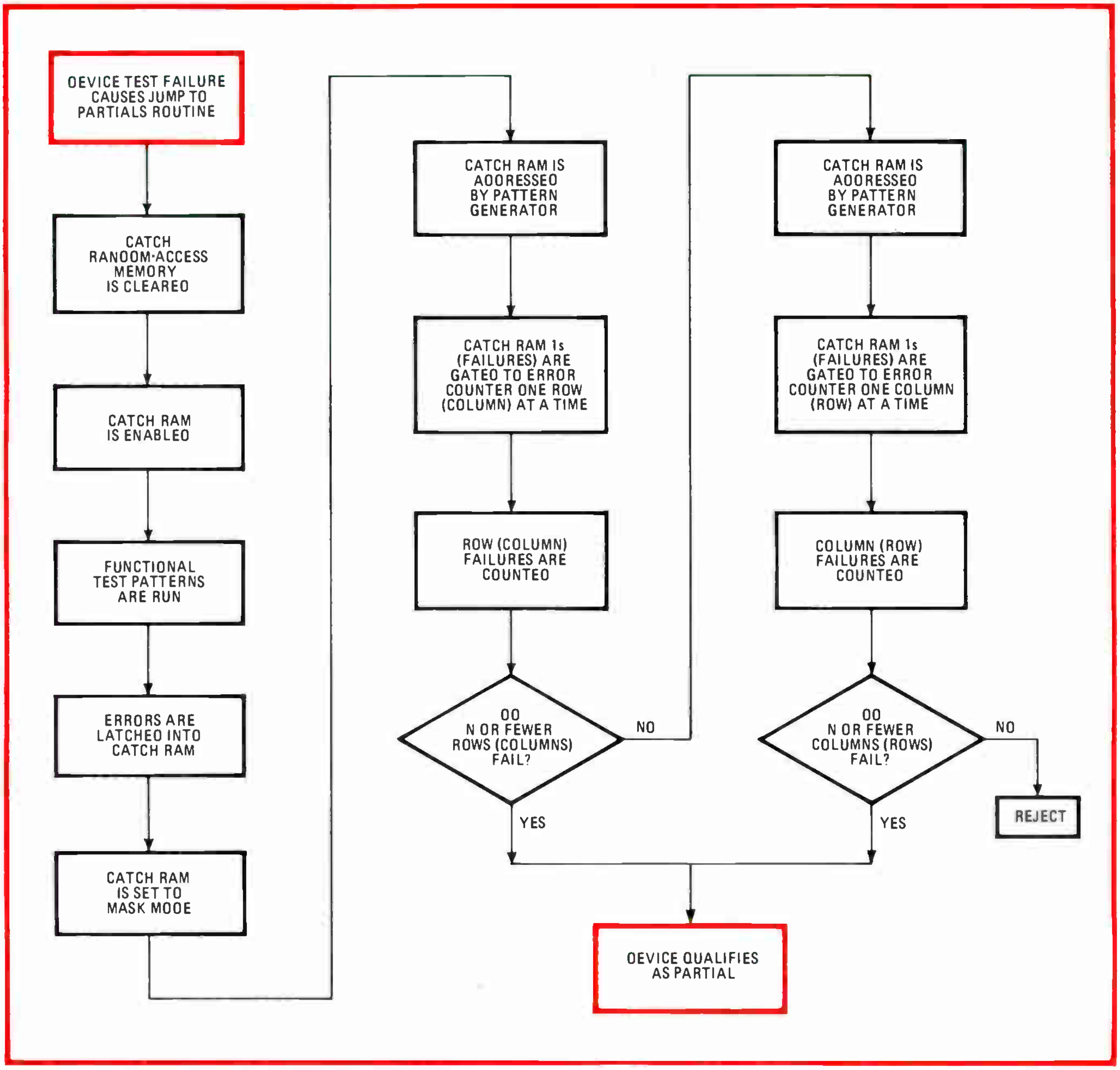
The operation of the RTBM hardware is controlled by a series of partials testing routines written in the test language of the Teradyne tester. These routines are linked to the device test routine so that they are called automatically, without operator action.

When a bit failure occurs during the normal device test, the operating program of the J387 jumps to the partials testing routines. They enable the RTBM hardware and clear the catch RAM. The catch RAM is then set to the latch mode so that if a bit failure occurs it is latched into the RAM in a location corresponding to that in the device under test.

With the RTBM hardware disabled, a bit error from the memory under test would signal the J387's master operating program (MOP) to shut down the pattern processor and no further testing would be done. But when the RTBM hardware is enabled, the error signal and a signal from the RTBM control logic are fed to a NAND gate. The output of this gate is such that the MOP does not see the error and the pattern processor continues to function, so partial testing can be performed.

With the catch RAM in the latch mode, functional tests are performed on the memory under test. Any failures are automatically logged in real time and the entire memory is tested. After the functional tests are performed, the catch RAM has a complete record of all bit failures, so it is no longer necessary to address the device under test to find the number of rows or columns that have failed.

To find that number, the catch RAM is set to the mask mode. In this mode, it can be addressed by row or column and only the failed bits read. These bits are fed to the counter and, after each row or column is read, the



4. Complete partial test. Partial testing program is linked to device test routine so that when a failure occurs during normal testing the partial test is called automatically. Clearing the catch RAM and checking its contents by row and/or column adds very little to total wafer test time.

counter is examined by a software routine that keeps track of row and column failures. Figure 3 presents a simplified logic diagram of the error signal flow in the processor.

A 16-K test case

Applying this procedure to 16-K dynamic RAM testing serves as a practical example of how test parameters related only to partials are determined. Since the catch RAM forms a clone of the memory under test, it must equal it in size. Therefore, for 16-K devices, the catch RAM is organized as 2,048 8-bit words. Teradyne also supplies a 64-K catch RAM so that larger devices can be tested as partials too.

Assuming that the 16-K devices being tested are organized into internal rows of 128 bits with columns of equal length, and that production yield increases significantly if partials with 15-K or more of usable storage are packaged, the maximum number of failed rows or columns that can be accepted must be set at 8. For a different, nonsymmetrical internal organization, the acceptable number of rows and columns would have to be adjusted independently.

The program flow chart for testing these devices is pictured in Fig. 4. To determine whether or not the device under test is acceptable, one axis—the rows, for example—is checked first. If it passes, it is marked for packaging as a partial. If not, the columns have to be checked.

Obviously, an investment must be made to reap the partials dividend, and that investment is test time. For partials testing, certain unique routines must be

RTBM—a memory user's tool, too

Real-time bit mapping is often used as a production technique; in addition to the application outlined in this article, it is also used to find mask defects and to overcome process problems. But memory users as well as manufacturers can profitably employ it.

For example, part purchasers may use it to look at the possible pattern sensitivities of incoming devices so that they can gear their test procedures to hunt for them. They can also use it to determine a device's sensitivity to parameter variations—changes in supply level, for instance—so that they can set practical design rules for their products. Having once done so, they need have less worry about board design changes adversely affecting product performance and lead time.

The "real time" in the technique's name refers to the gathering of data. When this is done, the catch RAM is addressed in parallel with the device under test using unscrambled addresses—addresses that are based on the topological location of cells inside a device rather than the scheme adopted by the manufacturer for his pinouts. Thus the stored data can provide a picture of the physical area in the device in which problems occur.

One of the catch RAM modes is the latch mode. When operated thus, the catch RAM holds a bit failure until it is cleared. If a functional test is repeated a number of times, the catch RAM contains the total number of bits that failed during these tests, whether they occur repeatedly at each test or whether they occur intermittently.

The catch RAM can also be operated in the nonlatch mode. In this mode, a catch RAM bit indicating a failure is not held but reset if the bit passes a subsequent test. By using both modes, users can distinquish between hard and soft failures and determine the parameters that affect the soft error rate of a device.

Another mode mentioned is the mask mode. It is particularly useful for incoming inspection of partial devices as well as production testing. The mask mode can be used to ignore specific bits in a memory. So after a functional test has been performed with the catch RAM in the latch mode, the error bits in the RAM can be used as a mask and the functional test run again to be certain that the partial works as it should.

Where RTBM is probably of greatest value to the user is in determining the sensitivity of a device to parametric variation. It not only allows him to set design limits for a particular device but it also permits him to evaluate various devices of the same type so that he can choose the one that best suits his needs.

The contents of the catch RAM can be recorded on magnetic tape after each test and the collected data analyzed and displayed on a color cathode-ray tube. Different colors can be used to indicate different frequencies of failure.

Along with the failure pattern, the parameters to be varied can be displayed on the screen. Using a joy stick, an engineer can vary the parameters and observe the result of those changes on the device under test, either sequentially or as a composite. In this way he not only finds the sensitivity of the device, but he gains a better understanding of its operation.

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performed, such as clearing and interrogating the catch RAM.

Either of two methods can be used to clear the catch RAM. Using a simple RSEND (transmission of consecutive memory locations) command, the catch RAM is cleared in 8-bit bytes. The clear execution time using RSEND, T_{cr1}, is given by the formula:

$$T_{cr1} = (D_{cr}/8 \times 10\ \mu s) + 320\ \mu s$$

where D_{cr} is the density of the catch RAM in bits. The 10-μs multiplier represents the time it takes the hardware to execute each RSEND command, and 320 μs is the time it takes the system to set up the clear procedure, a one-time event for each partial tested. For a 16-K device, this method takes 28.8 ms to clear the catch RAM.

A faster, alternative means of clearing the catch RAM—but one that requires more complex programming—is the single-bit method. Here, the catch RAM is cleared 1 bit at a time at the pattern processor's maximum speed. The clear execution time using the single-bit method, T_{cr1}, is given by the formula:

$$T_{cr2} = (D_{cr} \times 100\ ns) + 1{,}804\ \mu s$$

The 100-ns multiplier is the cycle time of the pattern processor. The complexity of the program needed to set up this procedure is reflected in the fact that it takes the system 1,805 μs to set up as opposed to 320 μs in the previous case. For 16-K devices, the time it takes to clear the catch RAM using this technique is 3.4 ms.

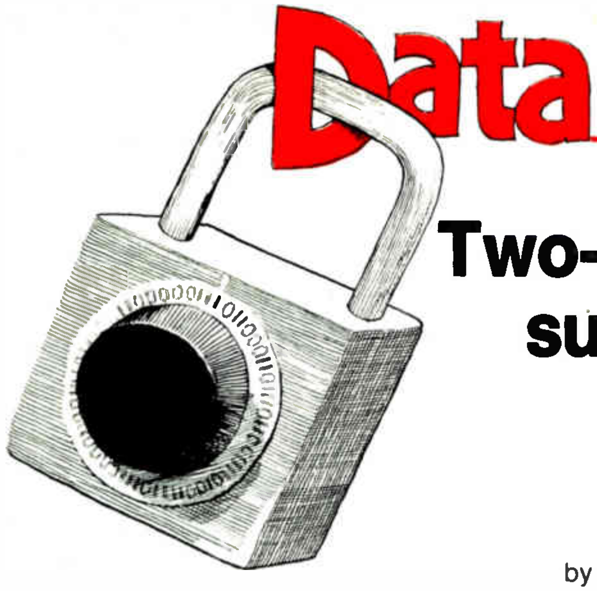
Since the catch RAM is loaded in real time—that is, the time the functional tests take to perform—the burden put on tester overhead for functional testing of a partial is no different than for a good device. The only remaining test time that must be considered is that for interrogating the catch RAM to find row and column failures.

The worst-case test time can be determined by assuming that the entire catch RAM must be scanned by row and column to detect errors. The total interrogation time, T_i, is then the sum of the interrogation time for rows and that for columns. The interrogation time for a row or column is given by:

$$T_n = [(N_{bn} \times 100\ ns) + 655\ \mu s]N_n + 1{,}485\ \mu s$$

where N_{bn} represents the number of bits in a row or column and N_n represents the number of rows or columns. As before, 100 ns is the cycle time of the processor. The system program time for each row or column operation is 655 μs and the device-independent program time is 1,485 μs.

For a symmetrical 16-K device of the kind discussed, the interrogation time for rows is equal to that for columns—86.00 ms. Therefore the worst-case interrogation time is 173.98 ms, and the worst-case overhead for partials testing is between 177.39 and 194.78 ms greater than for whole devices, depending on the type of procedure used to clear the catch RAM. The manufacturer's cost for this additional test time is made up for by the sale of devices that would otherwise wind up in the test floor sweepings. □



Two-chip data-encryption unit supports multi-key systems

One version of the set operates at a data rate of 11,500 bits/second

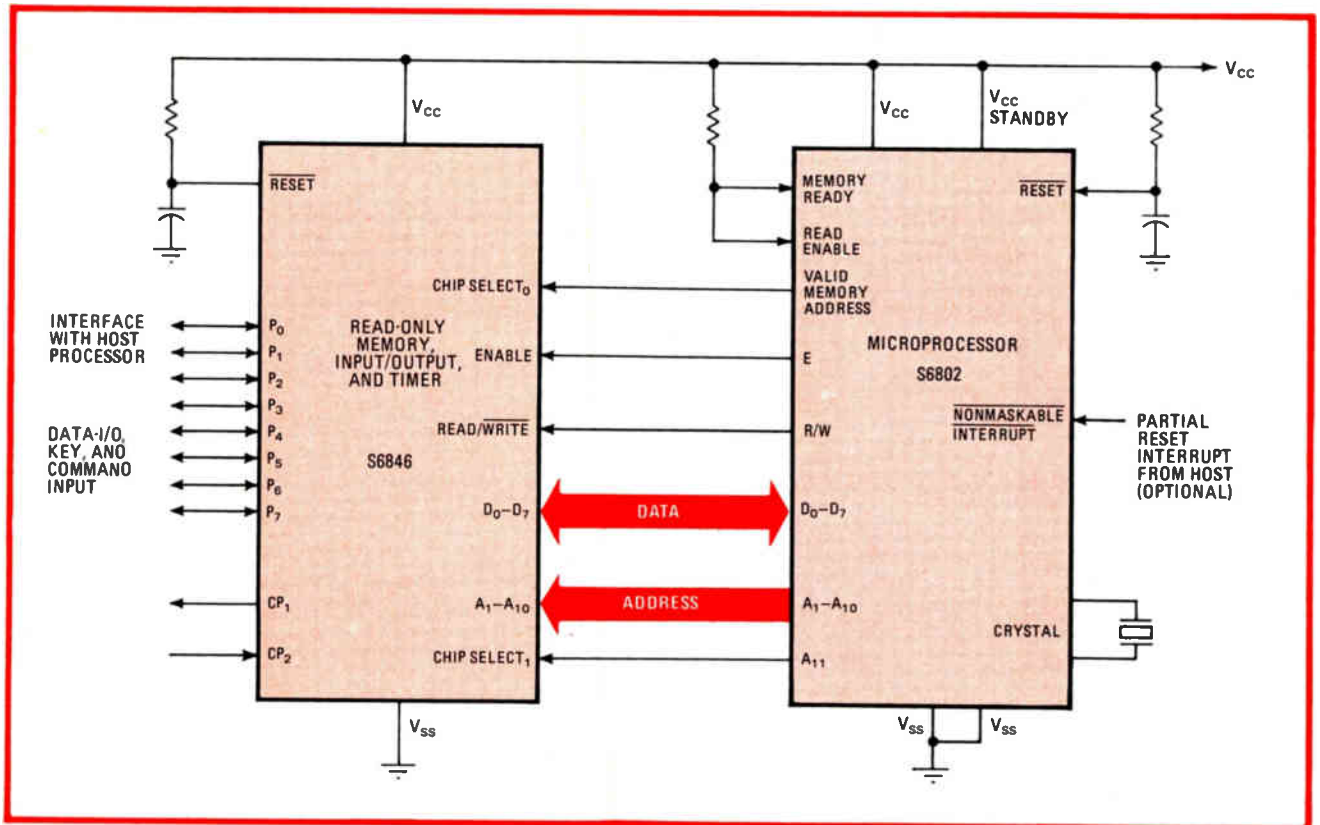
by Thomas Humphrey and Frank L. Toth, *American Microsystems Inc., Santa Clara, Calif.*

☐ With more data-encryption and -decryption chips coming onto the marketplace, the choice confronting potential users is widening. However, applications requiring a high degree of security call for the use of multiple keys, and most of these dedicated integrated circuits are geared toward systems using a single encryption key. The S6894 data-encryption chips set, though, is adaptable to multiple-encryption-key systems with a minimum of software and hardware fuss.

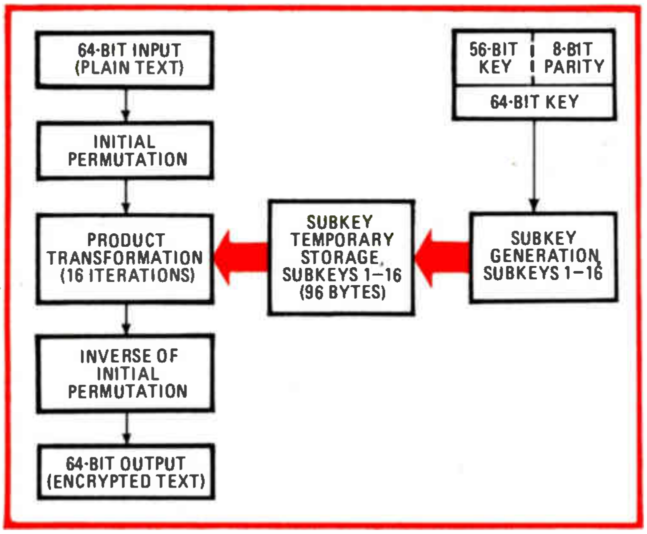
This is the third in a series of articles on data-encryption devices that implement the National Bureau of Standards' data encryption standard. The first two articles appeared in the July 19 issue, page 140, and the Aug. 2 issue, page 126. A special report on the DES appeared in the June 21 issue, page 107.

As a bonus, the set can operate at data rates of up to 11,500 bits per second—in contrast to many data-encryption units, which can handle only several thousand bits per second. The S6894 is thus suitable for most data terminals, credit-card validation and verification systems, point-of-sale terminals, and banking equipment that incorporate microprocessors and their peripherals.

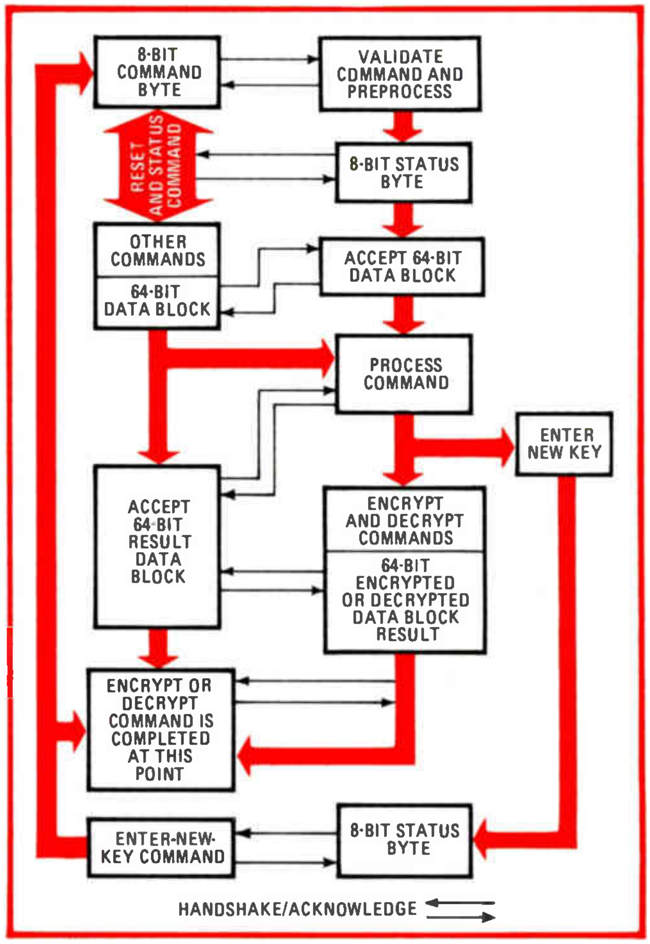
A full understanding of how to use this data-encryption unit requires adequate knowledge of the design and operation of the chip set itself.



1. Encryption brothers. American Microsystems' S6894, a two-chip data-encryption and -decryption unit, contains an S6802 microprocessor and an S6846 read-only memory that also has I/O and a timer. Models handling data rates of up to 11,500 bits per second are available.



2. Best choice. The 16 subkeys required for the NBS data encryption standard are computed each time a new 56-bit data-encryption key is entered in the system. This approach minimizes the encryption time but uses most of the random-access memory.



3. Data flow. All input/output signal transfers are individually acknowledged by handshake signals in the S6894 data-encryption system. The set will not proceed to the next step in an operation unless each step is acknowledged by the host processsor.

The S6894 implements the complete NBS DES algorithm [*Electronics*, June 21, 1979, p. 107] using a proprietary program written for the S6800 family of microprocessors. It consists of two chips. The S6802 is the microprocessor itself, with an on-chip clock generator and a 128-byte random-access memory. The second chip is a programmed S6846 read-only memory with input/output and a timer.

Two-chip subsystem

Together, these circuits perform as a complete microcomputer encryption subsystem (Fig. 1). Depending on the model chosen, they are capable of encrypting an entire standard 64-bit data block input in 5.5 milliseconds. This speed corresponds to a data rate of 11,500 bits per second in sustained operation. Even allowing for communication protocol control and checksum bits, this rate is more than adequate to support a fully utilized 9,600-baud synchronous data link. This speed in turn is fast enough for most of the applications mentioned earlier.

Designing the set

There were two principal design objectives for the S6894 chips. Users generally want both a very high data-encryption rate and easy interfacing with microprocessor systems. Achieving these goals would simplify their applying the set.

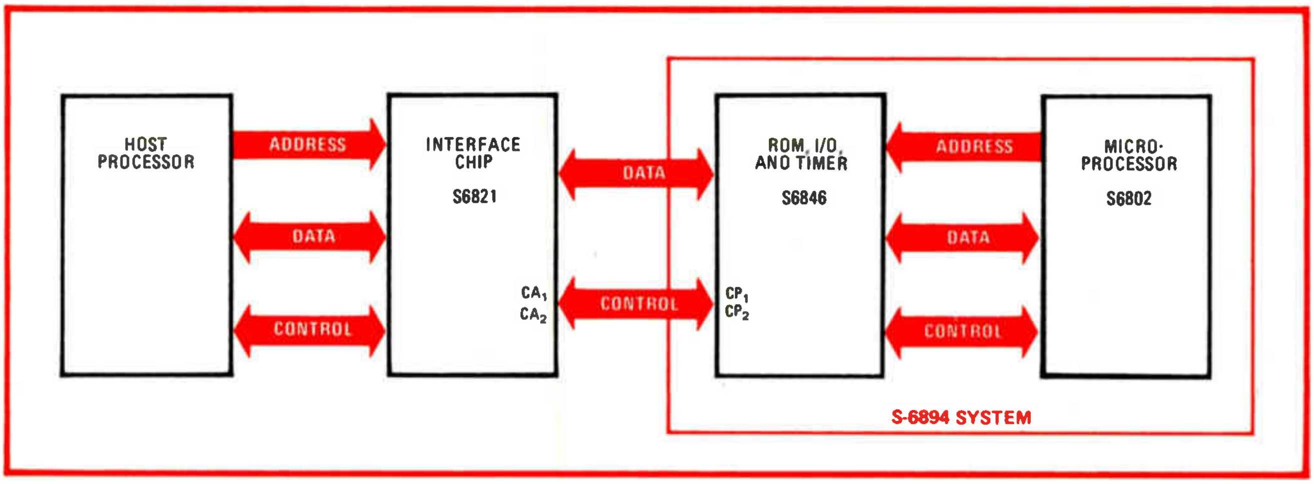
But because the microprocessor hardware configuration—a standard circuit that is widely used—placed several constraints on the software design, there were certain difficulties to overcome in realizing the objectives. For one, all variable data—including a stack area to service subroutine calls and processor interrupts—must fit within the 128-byte RAM of the S6802. For another, the program for encrypting data, with its constants and lookup tables, must fit within the 2-kilobyte ROM of the S6846. Finally, all the command words from the host processor, status indications from the data-encryption unit (DEU), and data input and output must be transferred through the single bidirectional 8-bit parallel I/O port of the S6846.

Yet the 6800 series devices were up to the job. What was required were the usual tradeoffs between software and hardware that are inherent in any microprocessor-based system. The necessity for the tradeoffs was based on the simple fact that the amount of RAM and ROM available in the S6802 and S6846 dictated the design approach to the set. The method used to generate and store subkeys illustrates the tradeoffs.

Providing for subkeys

In the DES algorithm, the 56-bit encryption key is not used directly during encryption and decryption. Instead, each of the algorithm's 16 product-transformation steps uses a different permuted selection, or subkey, of 48 bits from the basic 56-bit key.

One method of implementing the subkey is to store only the 56-bit encryption key in RAM. Then the 48-bit subkeys may be computed as required during encryption. The benefit of this approach is that the encryption key occupies only 7 bytes of RAM (8 bytes if the key is stored as two 28-bit half blocks). The DEU can thereby be made to support multiple encryption keys, with most of the



4. Complete system. The S6894 two-chip data-encryption and -decryption subsystem can be connected to a host processor through an S6821 interface chip or its equivalent. Encryption time can be as low as 5.5 milliseconds.

128-byte RAM still available for work space, stack area, and other data storage. The disadvantage is that computation of the subkeys adds significantly to the data-encryption time.

An alternative approach is to precompute the 16 subkeys each time a new 56-bit encryption key is entered (Fig. 2). This method minimizes the encryption time. With this method, 96 bytes of RAM are required to store the 16 48-bit subkeys. In the S6802, that leaves 32 bytes of RAM for other uses—adequate for the applications at hand.

Because one of the design objectives was to maximize the encryption speed, precomputation was chosen. This decision was a major tradeoff, since, as noted, little RAM was available for variable data storage, work space, and the stack area.

Subroutine nesting, for example, was now limited to two levels. That means that a data-encryption key, once entered into the DEU, must be used for several encryption or decryption operations. In applications in which a different key is used for each encryption or decryption of 64-bit data blocks, the other design approach would be preferable and result in faster encryption.

Making the chips perform

How the data-encryption unit operates can be best understood by remembering that the DES algorithm and the S6894, as well as all other encryption devices, rely on one basic principle: the most critical factor in protecting the data transmitted through the chips is guaranteeing the secrecy of the encryption key.

In the S6894, the encryption key, once entered, cannot be accessed by external means in either its original or its processed form. Each key is entered only once—when the unit is turned on, following a DEU reset, or when the key is changed.

All these operations begin with an 8-bit command byte that comes from the host processor in the terminal after it is turned on. This command is validated by the DEU, and a status byte is returned to the host processor. The S6894 uses a set of five separate commands to interact with the host: enter new key, encrypt data, decrypt data, reset, and return status. They are all part of the data-flow sequence used to control the unit's encryption and decryption functions (Fig. 3).

In this sequence, the enter-new-key command instructs the data-encryption unit to enter a new encryption key. This key is a sequence of eight 8-bit bytes. The 7 leftmost bits of each byte are data and the rightmost (least significant) is an odd-parity bit. A parity error on any data byte causes the key to be rejected and command processing to abort; a status indication is then returned to the host processor. If there are no parity errors, the 56-bit key data block is readied for use in encryption or decryption, and a ready-status signal is sent to the host processor.

The encrypt- and decrypt-data commands instruct the DEU to convert the 64 bits of data into encrypted code or plain text, respectively. The encrypt-data command is rejected if no valid encryption key has been entered since the most recent reset of the S6894. Otherwise, the 64-bit result will be returned to the host processor as a sequence of eight 8-bit bytes.

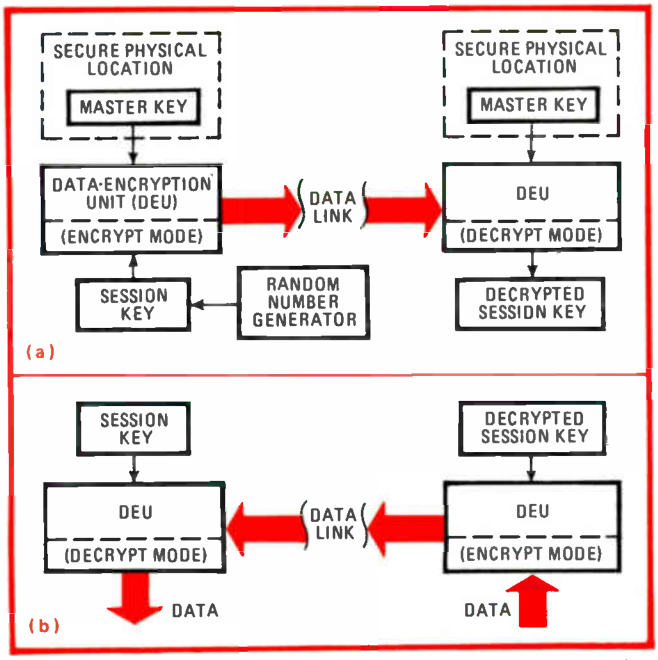
The reset command returns all DEU controls to an initial state. A full reset (the encryption key is cleared) or a partial reset (the current encryption key is preserved) is controlled by the setting of the key bits in the command byte. Finally, the return-status command returns the current value of the DEU status byte to the host processor.

A good example

In a typical encryption system, the host processor communicates with the S6894 through a S6821 or equivalent interface chip (Fig. 4). All handshaking functions are performed through lines CA_1 and CA_2.

A negative-going transition on the S6894's CP_1 input line signals the presence of valid input data on lines P_0–P_7 (see Fig. 1 again). This transition latches the data into the DEU input port buffer, and its receipt is signaled by a negative-going transition on the CP_2 output line. The port is then ready to accept the next input, if any.

Valid output data on lines P_0–P_7 is signaled by a negative-going transition on output line CP_2. Receipt of this data must be acknowledged by a negative-going transition on input line CP_1 before the unit will proceed



5. Pick a key. The S6894-2 can be used in the master-key (a) or the session-key (b) mode. Two new commands are required for two-key operation. These are included in software.

immediately on to the next operation.

The speed of American Microsystems' encryption system can be enhanced by using selected devices. For example, whereas the S68A94—one of the models available—can handle 4,600 bits per second, the S68H94 runs at 11,500 bits per second and an encryption time of 5.5 ms, the top figures mentioned earlier.

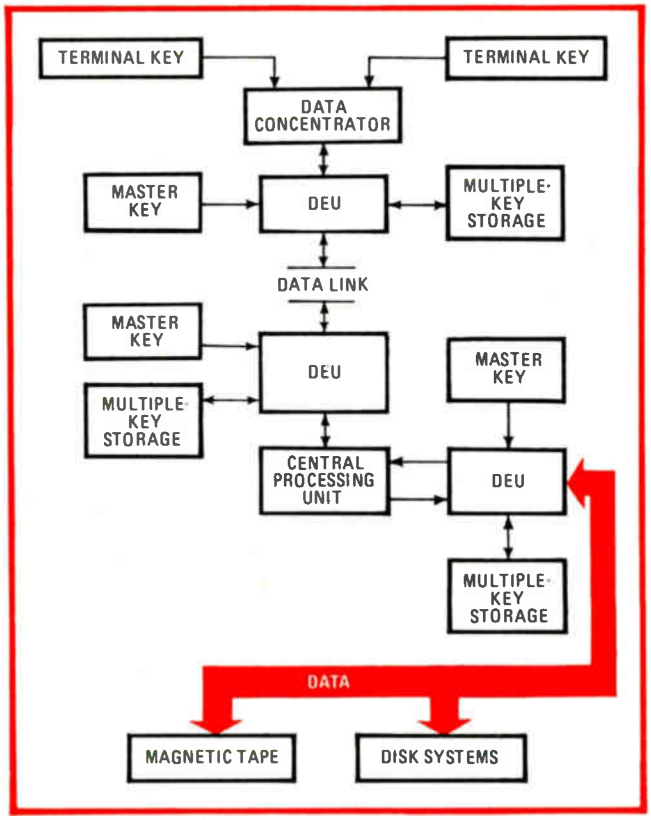
This figure is an "average minimum" time. It occurs when the host processor conforms fully to S6894 data-I/O and control-signal timing requirements without introducing any additional delays. Although the operating time of the S6894 may vary with data patterns because of random differences in encryption and decryption and key-processing times, variations—even in the worst case—from any specified times are less than 2%.

Multiple-key systems

Added security can be gained in a data-encryption system by using multiple-key, or master-key, systems. In this approach, a single key is used to generate (encipher) other keys, known as session keys. The master key is the only key that is stored in plain-text form. Therefore the problem of guaranteeing the security of the keys is reduced because only the master key must be kept in total security, and even if it were obtained, outsiders would also have to know how to generate the subsidiary keys. Usually, the master key is protected in a vault or other type of sealed unit.

The encrypted session key is transmitted over a data link or other communications medium to be decrypted. Once the decrypted session key is available at both ends of the link, encrypted data transmission can begin.

At no time is an unencrypted key transmitted outside the data-encryption device itself. A person trying to read the key or data (by a wiretap or other means) would intercept only the enciphered key and data. Without the master key, he could not easily decipher the data.



6. Computer safety. Three DEUs are needed for this system, which consists of remote terminals, a CPU, and magnetic memories. A separate key may be specified for each reel of tape or disk.

The session key could be generated by a random number generator. Every attempt should be made to keep the key truly random. For example, it should not be tied to personal variables such as birthdays or unique names that may make decoding easier.

The S6894 chip set can be expanded to a two-key version—the S6894-2—by adding external RAM for key and command storage. In this approach, the unit's encrypt and decrypt commands designate which key is to be used.

The S6894-2 can serve two data paths—for example, to two data terminals—having different encryption keys and can be used in the master-key or session-key modes (Fig. 5). Here the device utilizes two special commands, decrypt key and process decrypted key, in order to prevent external access to the intermediate key value. These commands allow an encrypted key transmitted from a remote location to be decrypted using either one of the two existing keys. With this approach, either existing key can be replaced with a new key as desired.

A three-key version, the S6894-3, is also available, although at extra cost.

A data-encryption unit may be placed in two locations within a computer system—most obviously, at both ends of the data link—and between the computer and peripherals (Fig. 6). A multiple-key storage unit stores master keys for each terminal and many session keys. The other multiple-key unit contains keys for each peripheral device and a separate key for each reel of tape or disk. □

Programmed regulators check system's operating margins

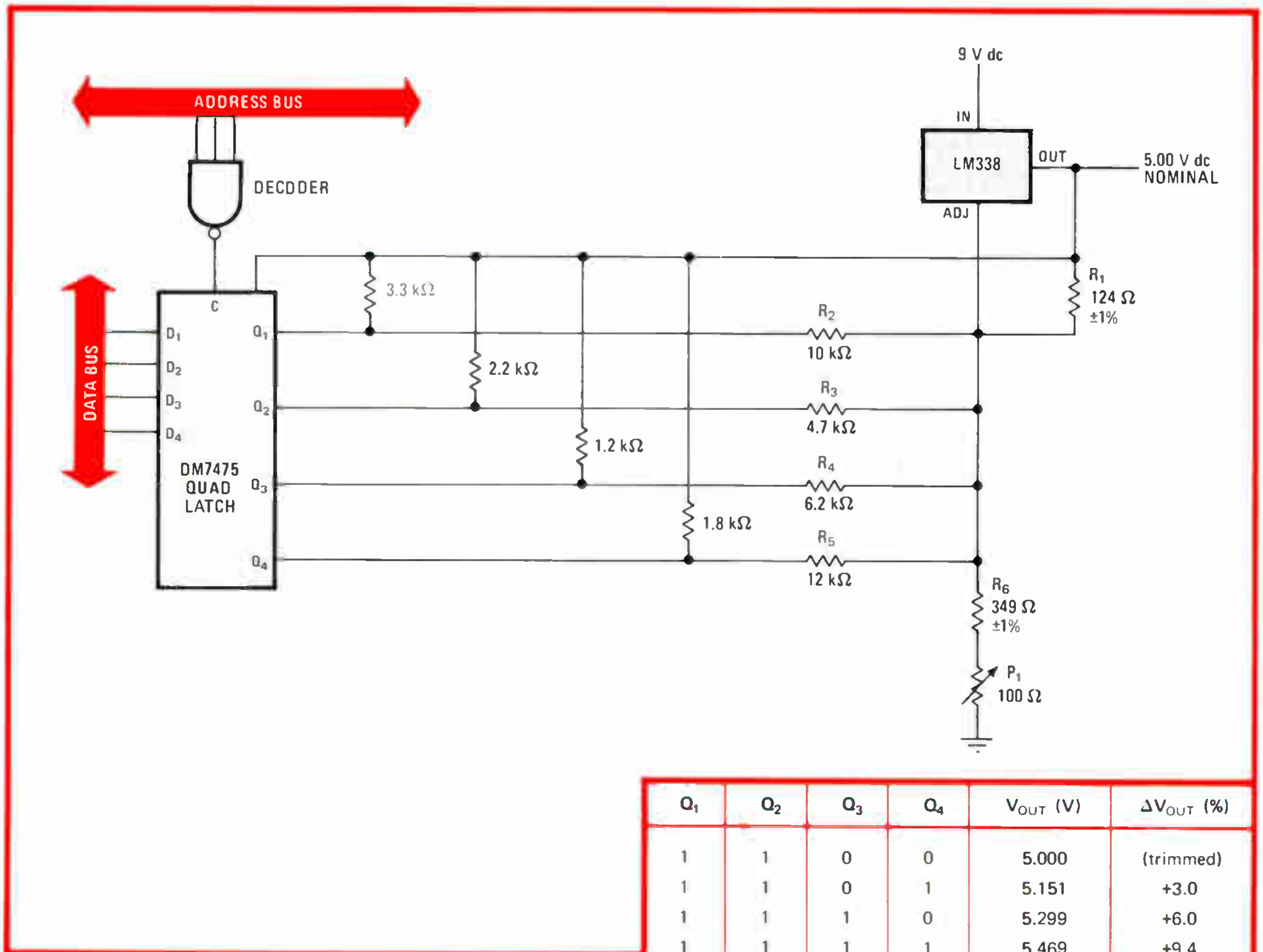
by Robert Pease
National Semiconductor Corp., Santa Clara, Calif.

Some computer systems that are functional with a nominal 5-volt supply may run only marginally at 5.1 V and not at all at 5.3 V, or vice versa, even though all voltages are within the system's specifications. By making programmable voltage regulators part of the computer's power supply, however, and placing the regulators under computer control, the true limits of the system can be easily determined. In addition to detecting any impending device malfunctions or solid failures at any given supply voltage, the test will be useful for diagnosing skew, race, and timing problems and will help to pinpoint noise and threshold difficulties.

The test setup is shown in Fig. 1. During operation at a nominal voltage of 5.0 V, the 7475 latch is programmed so that Q_1 and Q_2 are high, and Q_3 and Q_4 are low. Thus resistors R_4 and R_5 are effectively connected in parallel with R_6. Potentiometer P_1 is used initially to set V_{out} of the LM338 to exactly 5.00 V.

If Q_4 is commanded high, the net conductance from the adjust bus to ground will decrease, and V_{out} will rise 3% to 5.151 V. Conversely, if Q_1 is commanded low, the output voltage will fall 3.3% to 4.835 V. The list of intermediate output voltages that may be secured is shown in the chart. The range covered will be ±9.5%.

The same basic function can be provided for systems that are powered by negative voltages (Fig. 2). Here, the LM337 regulator is used. Resistors R_3–R_6 are switched



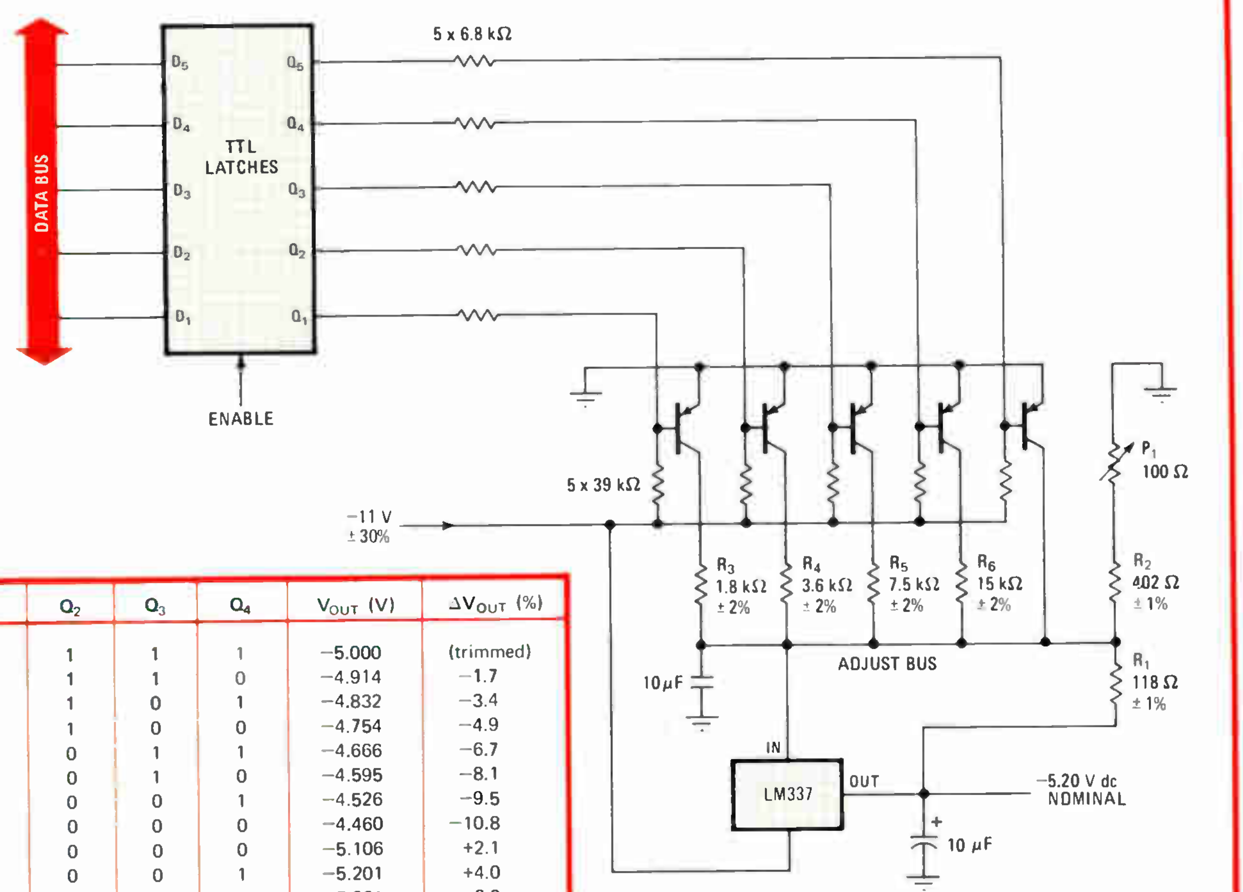
Q_1	Q_2	Q_3	Q_4	V_{OUT} (V)	ΔV_{OUT} (%)
1	1	0	0	5.000	(trimmed)
1	1	0	1	5.151	+3.0
1	1	1	0	5.299	+6.0
1	1	1	1	5.469	+9.4
0	1	0	0	4.835	−3.3
1	0	0	0	4.669	−6.6
0	0	0	0	4.526	−9.5

1. Variation. Auto-programmed regulator checks computer system for failures and malfunctions at any given supply voltage, thereby testing its operating margins. Table provides list of output voltages that may be ordered. The range covered is ±9.5%.

by pnp transistors much as they are in Fig. 1. Note that the resistors are in a binary-weighted proportion. To decrease V_{out} by 2%, Q_4 is brought low from its normally high state. To increase V_{out} by 2%, Q_1 is set high and Q_2–Q_4 is kept low. The range of voltages that may be ordered up is displayed in the chart.

Note that this circuit provides for a system shutdown. If output Q_5 moves low, the rightmost transistor will saturate and pull the adjust bus to within 100 millivolts of ground. V_{out} will then collapse to −1.35 V, and the computer will draw substantially zero power. ☐

Engineer's notebook is a regular feature in Electronics. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.



Q_1	Q_2	Q_3	Q_4	V_{OUT} (V)	ΔV_{OUT} (%)
0	1	1	1	−5.000	(trimmed)
0	1	1	0	−4.914	−1.7
0	1	0	1	−4.832	−3.4
0	1	0	0	−4.754	−4.9
0	0	1	1	−4.666	−6.7
0	0	1	0	−4.595	−8.1
0	0	0	1	−4.526	−9.5
0	0	0	0	−4.460	−10.8
1	0	0	0	−5.106	+2.1
1	0	0	1	−5.201	+4.0
1	0	1	0	−5.301	+6.0
1	0	1	1	−5.406	+8.1
1	1	0	0	−5.536	+10.7
1	1	0	1	−5.654	+13.1
1	1	1	0	−5.779	+15.6
1	1	1	1	−5.911	+18.2

2. Driving ECL. Same margin-checking function may be provided for computer systems powered by negative voltages. Circuit's trim resolution is 3%, enabling V_{out} to be set within 2% of any desired value. Programming information is secured from table.

Calculator notes

HP-41C tweaks vertical antenna arrays

by Walter J. Schulz
Philadelphia, Pa.

Aiding on-site adjustments of multi-element vertical antennas, this program tweaks arrays comparatively quickly. Using the relatively new HP-41C, a scientific pocket calculator with nonvolatile memory and an automatic turn-off feature for conserving battery energy, it is ideal for in-the-field plotting of the radiation pattern of the directional array.

The program sums the field contribution of each quar-

HP-41C FIELD PLOTTING PROGRAM

Line	Key	Line	Key
01	LBL ARRAY	30	+
02	−10	31	ENTER
03	STO 00	32	RCL 08
04	LBL 05	33	P−R
05	10	34	Σ +
06	ST + 00	35	RCL 00
07	RCL 00	36	RCL 09
08	PSE	37	−
09	CLX	38	COS
10	CLΣ	39	RCL 10
11	RCL 00	40	×
12	RCL 01	41	RCL 17
13	−	42	+
14	COS	43	ENTER
15	RCL 02	44	RCL 18
16	×	45	P−R
17	RCL 03	46	Σ +
18	+	47	RCL 13
19	ENTER	48	ENTER
20	RCL 04	49	RCL 11
21	P−R	50	R−P
22	Σ +	51	PSE
23	RCL 00	52	CLX
24	RCL 05	53	RCL 00
25	−	54	360
26	COS	55	x > y ?
27	RCL 06	56	STOP
28	×	57	GTO 05
29	RCL 07	58	END

Registers	
R_0	ϕ
R_1	ϕ_1
R_2	S_1
R_3	ψ_1
R_4	E_1
R_5	ϕ_2
R_6	S_2
R_7	ψ_2
R_8	E_2
R_9	ϕ_3
R_{10}	S_3
R_{17}	ψ_3
R_{18}	E_3

Instructions

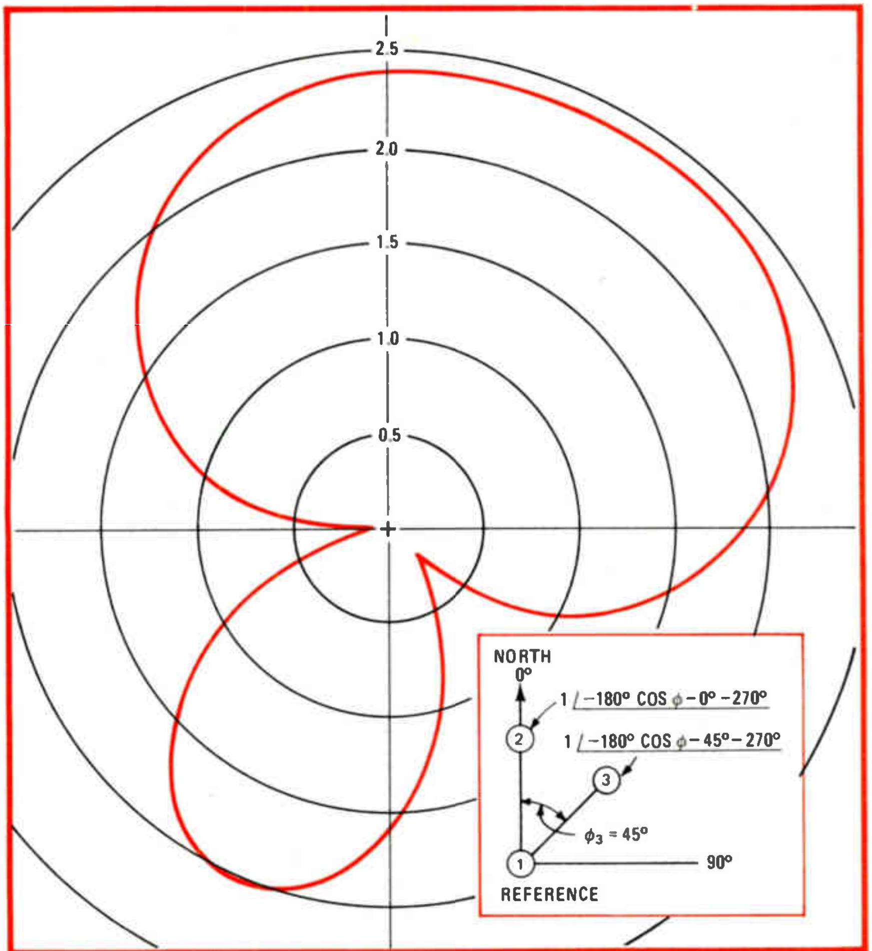
- Specify the number (abc) of memory registers required for the calculation, and the number of significant digits (n) to which each field-ratio value is to be found:

  EXC, α, SIZE, α, (abc), FIX, (n)

- Enter array parameters — azimuth, element position, spacing and phase with respect to reference for all antenna members:

  (ϕ), STO 0, (ϕ_1), STO 1, (S_1), STO 2,
  (ψ_1), STO 3, (E_1), STO 4, etc.

- Execute program:
  Calculator finds field ratio for 10° steps in azimuth to 360°, first displaying each azimuth angle, followed by its corresponding resultant.



BEARING	E_t	BEARING	E_t	BEARING	E_t
0°	2.4	120°	1.0	240°	1.0
10°	2.4	130°	0.6	250°	0.5
20°	2.4	140°	0.2	260°	0.1
30°	2.4	150°	0.3	270°	0.4
40°	2.4	160°	0.8	280°	0.8
50°	2.4	170°	1.2	290°	1.2
60°	2.3	180°	1.6	300°	1.4
70°	2.2	190°	1.9	310°	1.7
80°	2.1	200°	2.0	320°	2.0
90°	1.8	210°	2.0	330°	2.1
100°	1.6	220°	1.8	340°	2.3
110°	1.3	230°	1.4	350°	2.4

ter-wave element at all points in the horizontal plane from the equation given by Smith[1]:

$$E_t = \sum_{n=1}^{N} E_i (S_i \cos \phi - \phi_i + \psi_i)$$

where:

E_t = field ratio

E_i = magnitude of field intensity radiated by ith element, normalized to 1

N = number of elements, a maximum of 3

S_i = spacing of ith element, in degrees, with respect to the user-defined reference element

ϕ = azimuth, which is stepped in 10° increments over the range 0° to 360°

ϕ_i = position of ith element, in degrees, with respect to true north

ψ_i = electrical phase of ith element, in degrees, with respect to the reference

The program converts the given space factor vector (magnitude and angle) for each element from polar into rectangular form. The three individual vectors are then added for each 10 degrees in azimuth and the result converted back into polar form and displayed.

This routine accommodates three-tower arrays, which are probably the most popular found in amateur work and broadcasting. The program can be extended to handle a maximum of N=5 elements if necessary, however. Care should be taken in implementing the vector (tip-to-tail) additions.

As a check on the program, consider the three-element array configured as shown within the resulting polar plot of the system. Entering the required information as instructed in the program table yields the tabulated data from which the plot is constructed. □

References

1. Carl E. Smith, "Theory and Design of Directional Antennas," Smith Electronics Inc., Cleveland, 1969.

Engineer's newsletter

Seminar probes telephone's digital future

Probe Research, perhaps the first company to conduct an independent study of the future of AT&T and the telephone system, will host an intensive seminar on the "Digital Future of the Telephone Network" on Jan. 22 in New York. Aimed at designers, manufacturers, distributors, and users of digital networks, the seminar will explore a number of **alternatives open to professionals with a stake in both voice and nonvoice communications.**

The seminar will be led by Lee Goeller, assisted by Walter Gorkiewicz and Victor Schnee. The fee is $195, which includes all seminar materials and lunch. The program will be held at the Biltmore Hotel, 43rd St. and Madison Ave. For further information, contact Ms. Rita Tannenbaum at (212) 732-5415.

Microcomputer design through self-instruction

Bringing users one step closer to understanding and developing their own microcomputer systems, Advanced Micro Devices Inc. offers **a seven-booklet course entitled "Build a Microcomputer" free of charge.** The booklets discuss computer architecture, microprogrammed design, the data path (two booklets), programmed control units, interrupts, and direct memory access. The course will thoroughly familiarize students with AMD components in particular. Write or call Bob Grossman at AMD, 901 Thompson Place, Sunnyvale, Calif. 94086. Phone (408) 732-2400 for more information.

Symposium investigates plasma etching in semiconductors

Dry plasma processing has become an essential method in the production of advanced semiconductors, so much so that LFE Corp., a leader in the field, will hold a two-day symposium on state-of-the-art plasma technology. Called "Plasma U. S. A. '80," it will be held June 19–20 at the Hyatt Regency Hotel in San Francisco.

Structured for personnel involved in research and development and production of microcircuits, the session will consist of **detailed technical presentations by recognized plasma authorities in industry** and will include discussions of reactive ion etching, planar etching, barrel etching and stripping, silicon nitride deposition, silicon dioxide deposition, and automation of plasma processes.

Attendance will be limited, with reservations on a first-come, first-served basis. The registration fee of $325 includes two luncheons and morning and afternoon coffee breaks. To register, write or call Ms. Julie Dawson, Plasma U. S. A. '80 Symposium, LFE Corp., 1601 Trapelo Road, Waltham, Mass. 02154. (617) 890-2000.

Connector Symposium proceedings now available

The proceedings of the Twelfth Annual Connector Symposium of the Electronic Connector Study Group (held on October 17–18) are now available. **Included in the 400-page manual are 44 illustrated technical papers** in the areas of materials, finishes, and plating; fiber optics; coaxial connectors; interconnection; test methods, materials evaluation, and printed-circuit board packaging. The cost is $25 ($30 outside the U. S.). Write the Electronic Connector Study Group, P. O. Box 167, Ft. Washington, Pa. 19034.

-Vincent Biancomano

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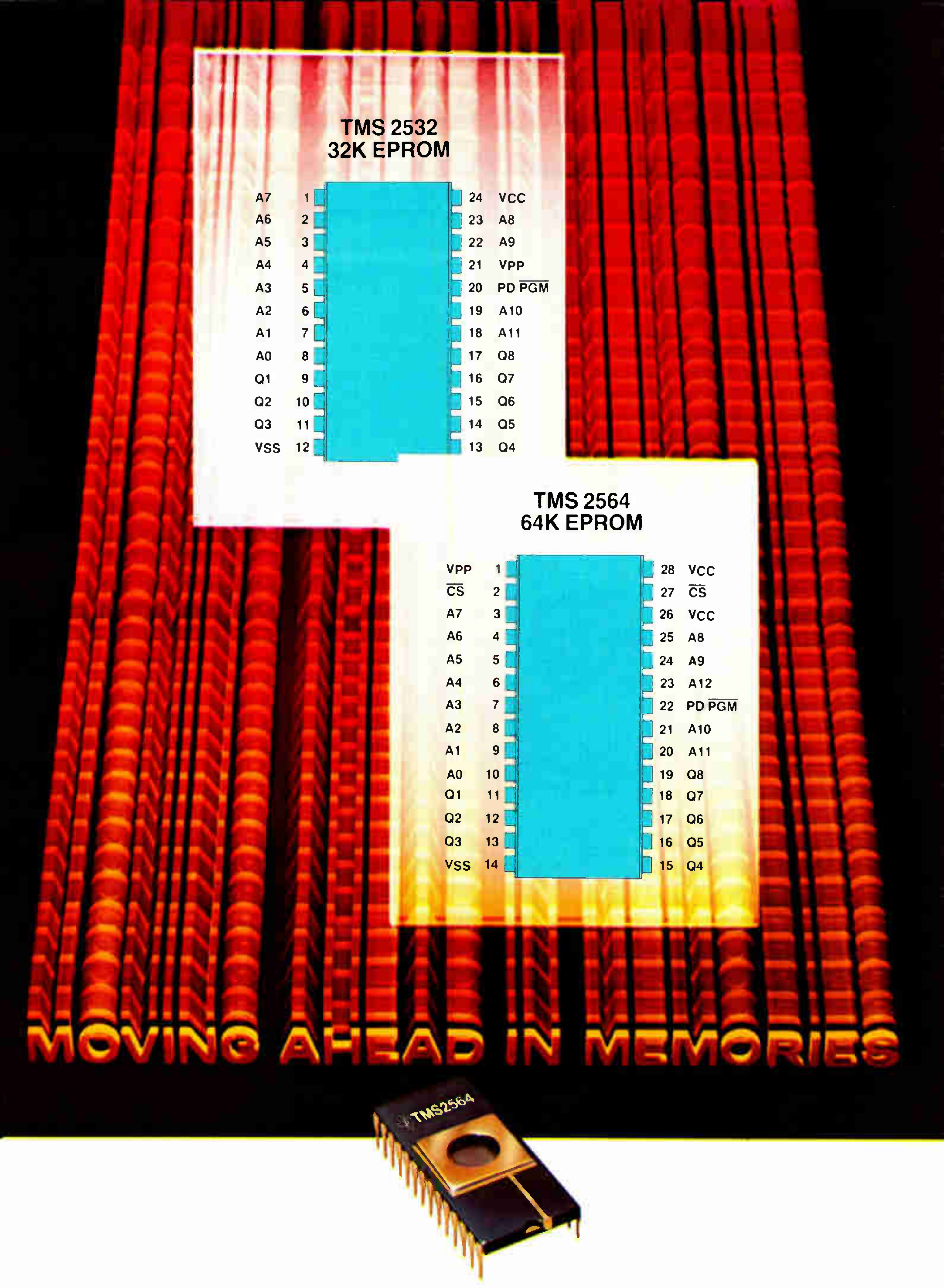
Circle 147 on reader service card


TMS 2532
32K EPROM
A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q1 9
Q2 10
Q3 11
VSS 12
24 VCC
23 A8
22 A9
21 VPP
20 PD $\overline{PGM}$
19 A10
18 A11
17 Q8
16 Q7
15 Q6
14 Q5
13 Q4
TMS 2564
64K EPROM
VPP 1
$\overline{CS}$ 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
Q1 11
Q2 12
Q3 13
VSS 14
28 VCC
27 $\overline{CS}$
26 VCC
25 A8
24 A9
23 A12
22 PD $\overline{PGM}$
21 A10
20 A11
19 Q8
18 Q7
17 Q6
16 Q5
15 Q4
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11903

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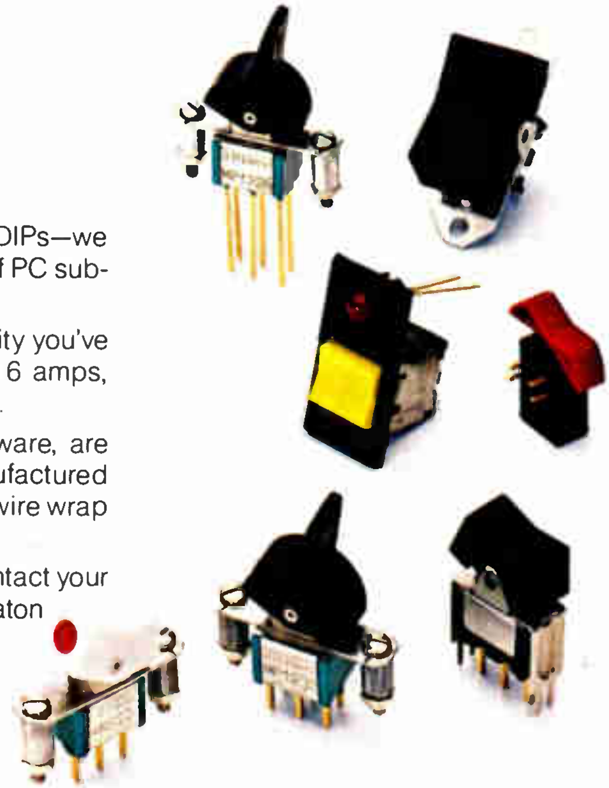
Circle 151 on reader service card

Four very small ways Cutler-Hammer switches improve your PC design.



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Circle 152 on reader service card

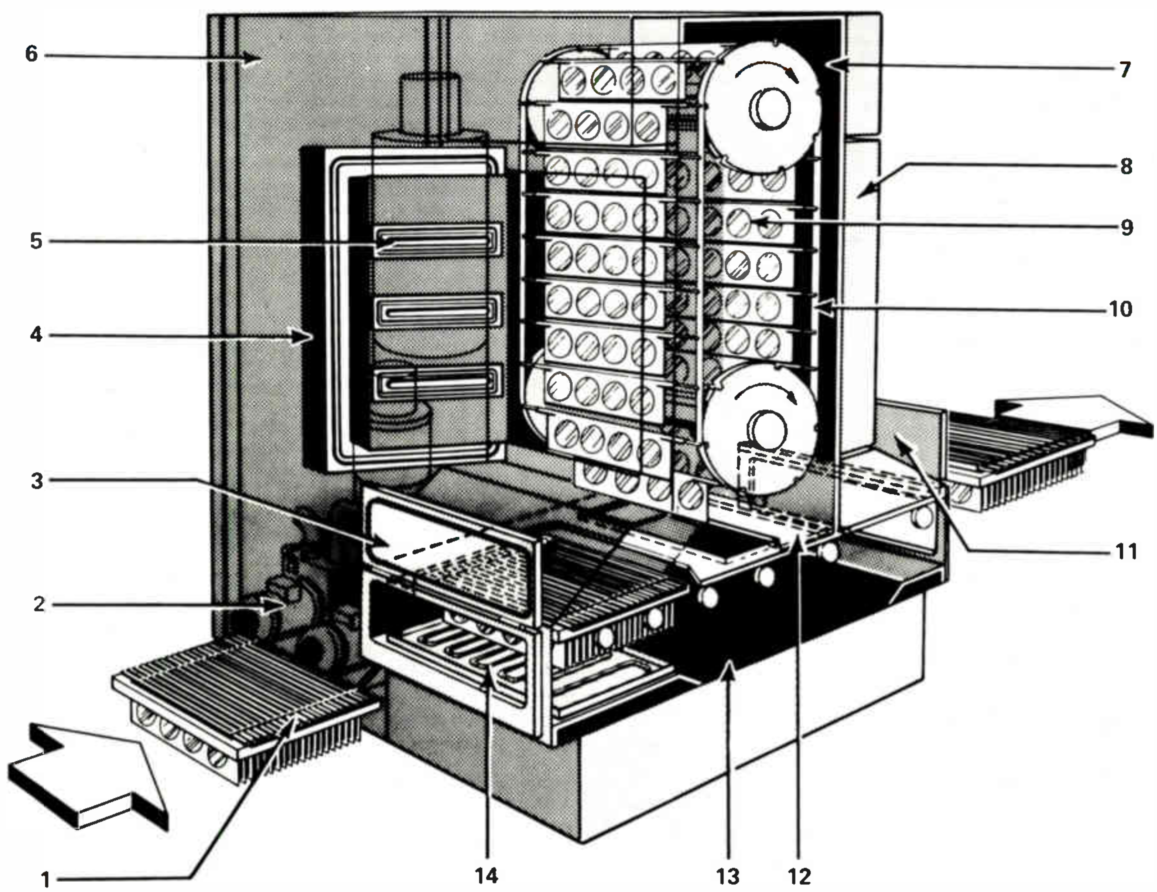
Sputtering system has high yield

Plant uses up to six high-rate cathodes, two vacuum chambers and a vertical transport system to keep both throughput and reliability high

by John Gosch, Frankfurt bureau manager

As fabrication technologies for electronic equipment—particularly microcircuits—become more and more exacting, there is an increased demand for equipment that offers high process reliability and yield coupled with high productivity. To help meet that demand, at least as far as sputtering systems go, West Germany's Leybold-Heraeus GmbH is readying the first model of a new generation of sputtering plants claimed to have capacities and throughputs up to four times higher than those of competing equipment. At the same time, they greatly improve the yield, according to the company.

The first model, the A 400 Z3 PS, is a two-chamber, high-rate-cathode sputtering plant. According to Gonde Dittmer, a project manager at the Hanau-based Vacuum Process Technology group of L-H, it can coat



What's inside. Cutaway view shows magazine with carriers holding unsputtered substrates (1); vacuum pumps (2); magazine loaded in lock chamber (3); front door with set of vertically oriented cathodes (4); type PK 500L high-rate sputtering cathode (5); supply cabinet (6); coating chamber (7); rear door on which cathodes cannot be seen (8); substrate carrier (9); conveyor belt (10); unloading of magazine with carriers containing sputtered substrates (11); load-transfer door (12); lock chamber (13); and infrared heat source (14).

one or both sides of about 13 square meters' worth of substrates in one cycle for a total capacity of about 26 m^2.

The time required to process a substrate is between 20 and 90 minutes, depending on the pretreatment and coating processes involved and on a number of other factors. That translates into an average throughput of up to 250 substrates per hour, depending on their size. The plant can handle rectangular substrates or circular ones with diameters up to 6 in.

The A 400 Z3 PS has two high-vacuum sections—a lock chamber and a coating chamber—separated by a lock. Equipped with an infrared heater and a high-vacuum pump, the lock chamber is loaded with a magazine that holds a number of substrate carriers, each with up to 28 substrates. The coating chamber contains the substrate transport system, which consists of a two-chain endless conveyor belt. The lock between the plant's two chambers is closed during magazine loading so the coating chamber is kept under a continuous vacuum.

Plant operation is relatively simple: after a magazine with uncoated substrates is loaded into the lock chamber, the latter is evacuated and the substrates are degassed and preheated to temperatures as high as 300°C. This ensures that the substrate surfaces are clean and free of residual gases before sputtering. The magazine then moves to the coating chamber for the substrates to be sputtered.

The key to the plant's high capacity and throughput is the design of its transport system, as shown in the illustration. Vertically installed, the endless belt picks up the substrate carriers, one after another, with the carriers hanging loosely between the belt's two chains. The belt then moves the carriers past two sets of vertically mounted cathodes, or targets, one on each side of the transport system. Thus, the substrates are coated on one side on the way up and on the other side on the way down.

The coating chamber may have as many as six cathodes, depending on

the quantity of material needed for layer construction, on whether the substrates are to be coated on one or both sides, and on whether they are to be sputtered once or several times with the same material. (The need to sputter a substrate more than once with a given material may arise if certain process parameters require that the substrate temperature be kept below a certain value and the required coating thickness cannot be achieved in one shot at that temperature. In such cases, the sputtering cycle may be repeated once or several times.)

Up to three cathodes, made of different materials, if necessary, may be installed on each side of the transport system. This makes it easy to fabricate multilayer constructions.

Yield is improved over competing technologies' by a combination of factors, Dittmer says. One is the system's vertical orientation, which prevents contaminating particles from settling on the substrate or cathode surfaces. Another is the use of turbo-molecular vacuum pumps, which provide an oil-free vacuum.

The plant's high-rate PK 500L cathodes, which may be operated with dc or radio-frequency voltages, are mounted on hinged doors that enclose the coating chamber during plant operation. When the doors are shut, the cathodes are adjacent to the two sides of the transport system; the average cathode-to-substrate spacing is about 60 mm. For coating substrates on one side only, one set of cathodes may be removed or shut down.

The A 400 Z3 PS will be available by mid-1980. The basic equipment, with one cathode, will sell for about $280,000. More elaborate multicathode systems will, of course, cost more. "But even the basic version has all the features plus the flexibility to expand it step by step into a high-capacity, high-throughput plant that can construct complex layers," Dittmer says.

Leybold-Heraeus Vacuum Systems Inc., 120 Post Rd., P. O. Box 483, Enfield, Conn. 06082

Leybold-Heraeus GmbH, 6450 Hanau 1, P. O. Box 1555, West Germany [338]

NO OTHER TAPE SYSTEM

LEAVES SO LITTLE TO CHANCE.

The Honeywell Model 101—it's like no other tape system you've ever used. Because no other system makes it so easy for you to get all your data—and get it right—on the first try.

HERE'S WHY:

Auto Test. Initiate this automatic routine and the Model 101 tells you if it's correctly calibrated. If not, the control panel display identifies the required adjustments.

Preamble. This unique feature simultaneously records calibration signals on all channels. Your playback instrument can then be adjusted to match the setup of the recording system for optimum reproduction.

Selective Track Recording. This lets you program the tracks you wish to record. You can automatically record forward on odd-numbered tracks, for example, then in reverse on even-numbered tracks. The result is maximum use of the tape and fewer tape changes.

Transport Sequencing. Two or more Model 101's can be programmed to record sequentially for continuous recording with no gaps in the recorded data.

Multipurpose Meter. During checkout or calibration this built-in meter can measure frequency, Vdc, Vac peak, or Vac rms. During actual operation it becomes a monitor meter that gives you a real-time look at the normalized inputs or outputs.

Built-in Calibration Equipment. A small screwdriver is all you need to calibrate the Model 101. Since there is no external test equipment to hook up, and no test points or calibration signals to remember, calibration takes just half the usual time.

The Model 101 also offers such advanced features as an adjustment-free triplanar tape path for exceptionally gentle tape handling, microprocessor control of operation and checkout functions, wideband and intermediate-band 3000-hour heads of solid ferrite, large reels for up to 32 hours of recording time, and up to 32 data channels in a single unit.

For more information on the Model 101, just call Darrell Petersen at (303) 771-4700. Or write for a free illustrated brochure that describes all our magnetic tape systems and other instrumentation products. Honeywell Test Instruments Division, Box 5227, Denver, CO 80217.

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Micro Component Technology, Inc.

P.O. Box 43013, St. Paul, Minn. 55164

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BUY A LINEAR LSI TESTER WITH YOUR EYES WIDE OPEN AND YOU WON'T LOSE SLEEP LATER.

In linear LSI test systems, like anything else, you only get what you pay for. And if you don't look before you leap, that "entirely new approach" to linear LSI testing could turn out to be the very same old computerized tester hiding behind some new metal, complete with all of yesterday's bottlenecks.

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What you need is the LTX Spacesaver LLSI Test System. It's a unique modular integration of hardware and software that's easy to use and easy to program. Our Spacesaver puts computer power where you need it. All with an eye towards speeding up payback by increasing throughput and yield.

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alignment techniques for better resolution and, therefore, speed.

According to Waser, several potential and existing users of the 67401 were operating in a byte (8-bit) mode that would require them to link two of the devices to provide a 64-word-by-8-bit FIFO. However, when they wanted a parity bit, he adds, "they would be required to use a third device for parity, even though that FIFO is only partially functional." That real estate can be reduced by one third, Waser notes, now that MMI has developed two new FIFOs organized as 64 words by 5 bits. Available in both 10-MHz (model 67402) and 15-MHz (67402A) versions, the 64-by-5-bit FIFOs come in 18-pin packages. Like the 67401A, they will be offered in both standard commercial (5 V ±5%, 0° to 70°C) and military (5 V ±10%, −55° to +125°C) versions.

Available off the shelf, the 67401A, 67402, and 67402A are priced at $38, $32, and $48 apiece, respectively, for quantities of 100 and up.

Monolithic Memories Inc., 1165 East Arques Ave., Sunnyvale, Calif. 94086. Phone (408) 739-3535 [411]

Fast 1-K-by-4-bit RAM aims at bit-slice applications

Fleshing out its line of fast static RAMs, Intel Corp. is now offering a pair of 4-bit-wide memories aimed at bit-slice and other fast microprocessor niches. The 2148H and 2149H are built from high-performance HMOS-II technology [*Electronics*, Sept. 13, 1979, p. 124], and both are organized as 1,024 by 4 bits.

The 2148H is a faster follow-on to the 2148 [*Electronics*, June 21, 1979, p. 40]—reaching down to an address access time of 45 ns. The 2149H, offered in 45- and 55-ns versions, is a similar part but without the automatic power-down feature that has become Intel's trademark.

Although the new devices have the same storage capacity as the 4-K-by-1-bit 2147 family of memories, their organization will sort them into markedly different applications areas, according to Kirk MacKenzie, strategic marketing manager of random-access memory components at Intel's Aloha, Ore., operation. The 2147 is being used in cache and main memories and has so far seen very little microprocessor application. The 2148H and 2149H, on the other hand, can be arranged for memory arrays with depths of 1,024 bits and this, coupled with their 4-bit width and compatibility with TTL, makes them very attractive for bit-slice microcomputer markets, at present dominated by bipolar components.

Both the 2148H and 2149H are available in two versions with worst-case address access times of 45 or 55 ns, and both draw 180 mA (900 mW) during active operation. The 2148H's power-down feature, activated by the chip-select line, automatically slashes power consumption by about 85%, down to 150 mW (30 mA) in standby.

Lacking the power-down, the 2149H sports a 20-ns chip-select access time—superior to the 45-ns premium chip-select access time of the 2148H—for nearly double the throughput in many applications. "The 2149H is for speed-sensitive applications where every nanosecond counts," says MacKenzie.

Both memories come in 18-pin packages and have common input and output pins for three-state operation. They are truly static memories, requiring no external clocks or timing strobes, and access times and cycle times are identical to increase data rates when system cycle times are longer than access times.

The devices are available in volume now, but pricing has not yet been determined.

Intel Corp., 3065 Bowers Ave., Santa Clara, Calif. 95051. Phone (408) 987-8080 [412]

Power-switching transistors range from 300 to 400 V

A family of six high-voltage power-switching transistors packaged in TO-3 metal cases is available for use in output stages of switching power supplies, automotive devices, and audio and stereo systems. The voltages for the npn units are either 300 or 400 V; the continuous current is 5, 8, or 15 A; power ratings are 100, 125, or 175 W. Deliveries of models 2N6542 through 2N6547 are from stock to eight weeks. In lots of 1,000, prices range between $1.70 and $4.95 per unit.

Panasonic Co., Electronic Components Division, One Panasonic Way, Secaucus, N. J. 07094. Phone Bill Bottari at (201) 348-7276 [415]

Infrared detector responds in 50 ns

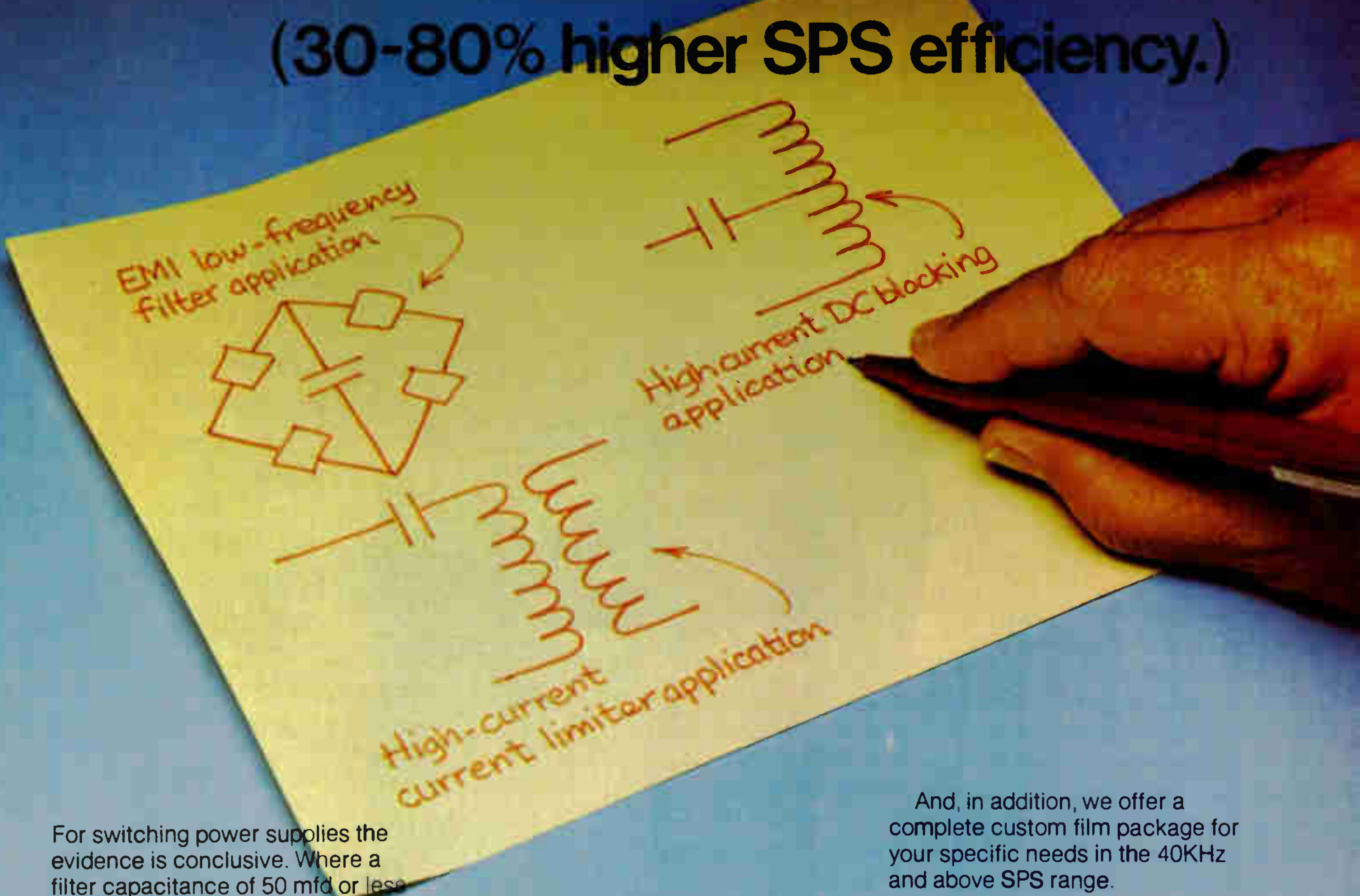
A high-speed infrared detection photodiode has a highly selective spectral response and a built-in transmissive filter for remote-control applications. The Ferranti BPW41 silicon p-i-n photodiode's filter has a peak response at 925 nm and a bandwidth of 730 to 1,040 nm at the 50% level. This, says the manufacturer, helps to make the BPW41 virtually immune to extraneous visible radiation. A junction capacitance with a maximum of 40 pF at the 3-V assigned value ensures the fast response time required in pulse-code-modulation systems. Turn-on and turn-off times are each 50 ns. The diode has an active chip area of 7.5 mm^2.

Among the remote-control applications for the BPW41 are TV channel selectors, toys, and remote keyboards for videotext systems, as well as fiber-optic termination and optical isolation. Modulated-signal TV remote controls that use the device would allow channel selection without having to go past each channel sequentially. For optical isolators, the use of a gallium arsenide emitter and this infrared photodiode makes a separate lens unnecessary because the diode includes the photodetector. The BPW41 sells for $2.02 apiece in lots of 100 or more, and delivery takes from four to six weeks.

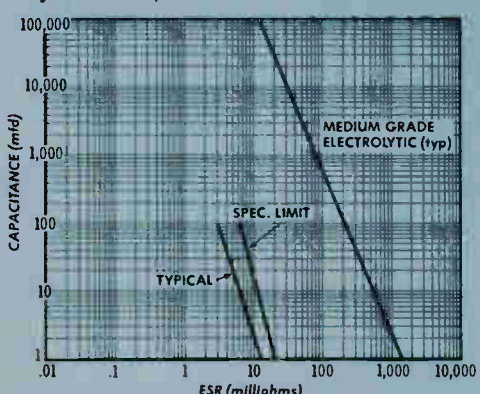
Ferranti Electric Inc., Semiconductor Products, 87 Modular Ave., Commack, N. Y. 11725. Phone (516) 543-0200 [414]

Why the switch is on to film capacitor filters.

(30-80% higher SPS efficiency.)



For switching power supplies the evidence is conclusive. Where a filter capacitance of 50 mfd or less will do, metallized polypropylene (film) capacitors far surpass electrolytics in impedance characteristics.



TRW-35 VS. ELECTROLYTIC ESR LIMITS

Here's why:

At resonance, ESR for a film capacitor is less than *one-tenth* that of an electrolytic. The film's capacitance won't dwindle at higher switching rate frequencies, so you can design with a lower value cap.

With a constant 2 amp ripple current, a film cap will cut I^2R losses—by *orders of magnitude*. Its current-carrying capacity is greater, so paralleling is usually not required. And ripple voltages are significantly less.

Film caps can be round or flat—you gain design versatility. And weight reduction: 16 grams/cu. in. vs. 26 for electrolytics. The bottom line: maximum current, minimum size and minimum loss.

At TRW, we're past pioneering a superior concept. We're delivering a buttoned-down product: the TRW-35 film capacitor is available now for input/output filtering in your state-of-the-art SPS design.

And, in addition, we offer a complete custom film package for your specific needs in the 40KHz and above SPS range.

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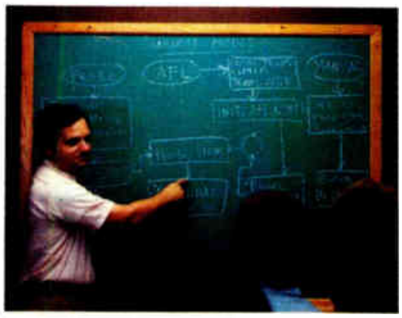

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GenRad's Programming Services Group is always ready to off-load your programmers whenever you need help.

And our Programming Services Group, made up of full-time applications specialists, can off-load your programmers whenever you need help.

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Altogether, GenRad offers you eight different levels of support. No other ATE company even comes close.

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For details on our complete ATE line—from product development to field testing—write GenRad, Concord, MA 01742.

GenRad

Put our leadership to the test.

Circle 169 on reader service card

Buying too much DMM makes some people feel secure.

Everybody has his own idea of security. Like some people just can't feel safe about a DMM unless it's over-specified and over-priced. That's OK for them. But what about people like you, who know that buying more than what you need is a waste?

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Of course, we'll be glad to sell you all the capabilities you want whether you need them or not. The important thing is that with Keithley the choice is all yours. We think a DMM on this page will show you exactly what we mean.

Our new, rough-and-ready 169.
The tough, battery-powered 169 is a 3½ digit DMM which delivers .25% DC accuracy. MTBF is 20,000 hours. Electrical parts are kept to a minimum for long life and fast, easy maintenance. It's the only low-powered DMM which displays both function and range along with the reading. You'll never settle for analog meters again. Price: $149.

The 191 outclasses its class.
Our newly introduced 191 is a μcomputer-based, 5½-digit DMM. It offers 1μV sensitivity, ±200,000 count resolution, 0.004% basic DC accuracy, 4 readings per second, non-linear digital filtering, pushbutton offset compensation and 2 or 4-terminal ohms measurement from 1mΩ to 20MΩ across 6 ranges.

It is a manual ranging bench DMM with DCV and ohms standard. ACV is optional. The μP design makes possible a 12-month recalibration cycle—twice that of its nearest competitor. Price: $549.

The 179 is a full function DMM and a 4★ value.
The 4½-digit 179 expands 178 capabilities with true RMS, 10μV sensitivity, 1kV protection on Ω, DC & AC current to 2A. It is also available in a 20A version.

Battery operation and BCD output are optional. 179 Price: $319. 179-20A Price: $359.

The 177 is total measurement capability.
The most sensitive DMM in its price range, the 177 offers outstanding specifications on all functions with 1μV, 1nA, and 1mΩ sensitivity.

True RMS, 5-functions, 0.03% basic accuracy, analog output, optional BCD output or battery pack—the 177 is a first rate bench DMM. Price: $429.

The 172A and 173A offer added features and performance.
Keithley's top-of-the line 4½'s offer 30,000 count display and auto or manual ranging on *all* functions including AC & DC current. Basic DC accuracy is 0.009%. Resistance capability spans seven ranges to 300MΩ. Both 2 or 4 terminal and Hi-Lo ohms are switch selectable. The 173A adds increased current capability to the 172A. Battery pack, BCD interface, and IEEE output are available on both models.
172A Price: $545. 173A Price: $675.

We sell satisfaction.
At Keithley we feel the best judge of what's best for your DMM application, is you. That's why we continue to expand our broad product line with a stream of first-quality, user-oriented DMMs.

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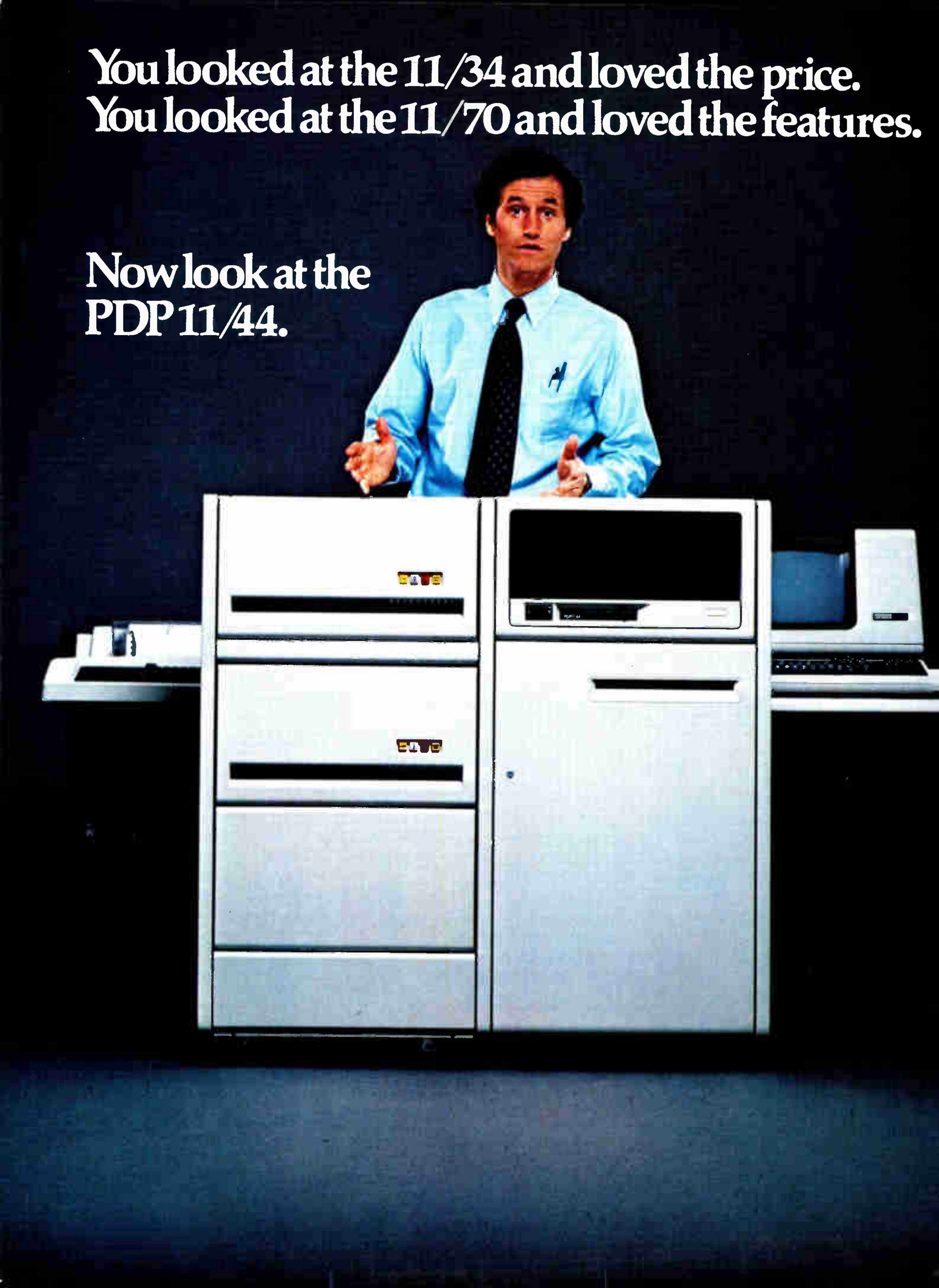
You looked at the 11/34 and loved the price.
You looked at the 11/70 and loved the features.
Now look at the PDP 11/44.

Digital introduces a mid-range mini with a megabyte of main memory, decimal arithmetic, and an expanded 11/70 instruction set.

Now for little more than the cost of an 11/34, our new PDP-11/44 gives you features previously found only on superminis. Like PAX, a physical address extension that gives you a full megabyte of main memory for more users, larger programs, greater throughput. A new MOS ECC memory with interleaving for faster access time. 8KB cache memory for faster program execution and greater DMA bandwidth. Sophisticated memory management. And an expanded 11/70 instruction set.

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Of course the 11/44 shares the design advantages of our entire PDP-11 family. Most importantly, it guarantees software compatibility the way only the world's broadest range of 16-bit compatible computers can. So your software investment remains intact no matter which system you choose. RSX-11M, the most versatile real time system in the industry. The new RSX-11M-PLUS. Or the new enhanced version of our proven general purpose and timesharing system, RSTS/E. You can also tailor the 11/44 to your exact application by choosing from a broad line of interfaces and peripherals, like our new 20 megabyte RL02 disk subsystem.

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digital

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Packaging & production

Units stabilize wafer exposure

Constant-intensity controllers for mercury arc lamps provide 2% regulation

Of the many steps that can be taken to improve yields in the manufacture of integrated circuits, one of the cheapest and simplest is the installation of instrumentation to control the intensity of the mercury arc lamps used to expose ultraviolet-sensitive resists in photolithography. Two such instruments, the model 762 and 764 from Optical Associates Inc., employ an optical feedback technique that detects changes in lamp intensity at the wafer plane and adjusts the lamp current to restore that intensity to its proper value. The constant-intensity controllers have response times of less than 20 ms and provide regulation within 2%.

The use of a constant-intensity controller facilitates the establishment of repeatable wafer exposure because it allows the total radiant energy applied to a wafer to be calculated as a simple time-intensity product. Without such a controller, the intensity must be integrated over time to get the total energy.

The 762 and 764 differ from each other principally in that the 762 is an analog instrument that displays lamp power consumption in watts or intensity in milliwatts per square centimeter on a mirror-scale meter whereas the 764 presents its data on a digital liquid-crystal display. The 762 has four push buttons for range selection—1, 5, 10, and 50 W or mW/cm²—but the 764 is autoranging. The 764 also features an alarm that sounds to alert the operator whenever the lamp goes out.

Both units provide dual intensity settings so the operator may shift from one preset level to another at the touch of a button. Both also provide an idling capability. In the idle mode, the lamp is kept operating at a power level optimized for long lamp life and stable emissivity.

Both controllers protect the lamp and the process against some of the effects of variations in line voltage. For example, the 117-V version of each controller will maintain lamp output within the specified limits even when the line voltage drops to 90 V. Besides this brownout protection, both units also protect the lamp against overvoltage by automatically shutting down when the line voltage gets too high.

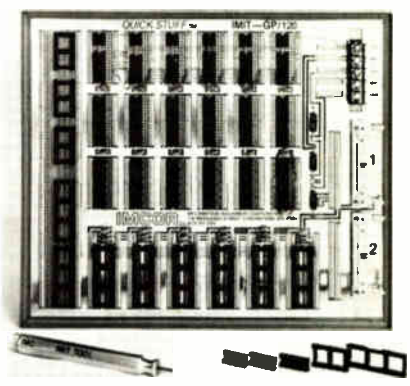
The controllers, which weigh approximately 15 lb, have delivery times of four weeks. The model 762 sells for $2,650, and the 764 goes for $2,950.

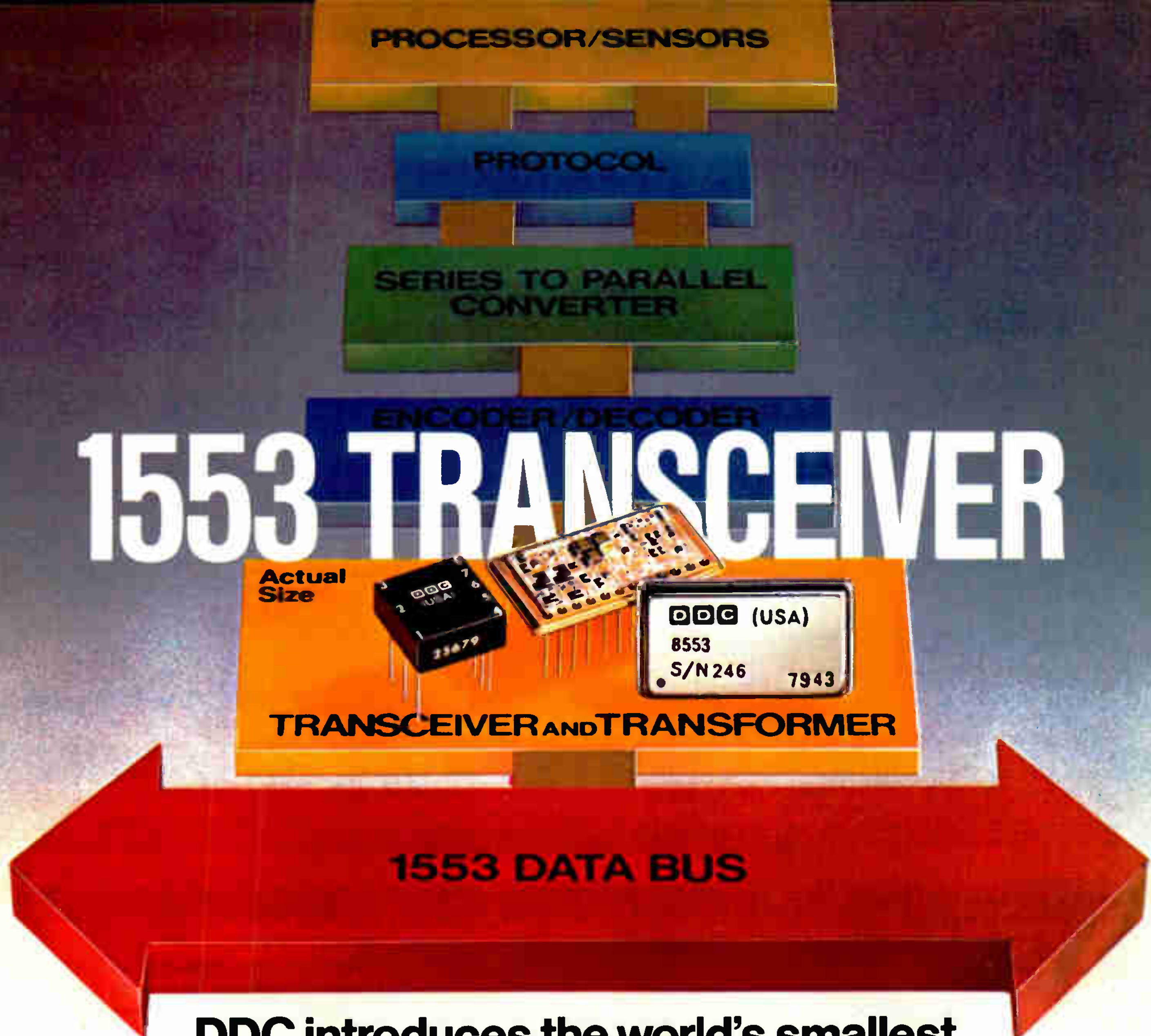
Optical Associates Inc., 3300 Edwards Ave., Santa Clara, Calif. 95050. Phone George Lee at (408) 988-6900 [391]

Insulation displacement speeds breadboarding

The fairly recent commercial emergence of insulation-displacement-contact (IDC) methods of circuit-board wiring is challenging traditional wrapped-wire systems with a number of design advantages [*Electronics*, Sept. 13, 1979, p. 98]. Faster wiring and altering of circuits, elimination of wire stripping and broken wires, point-to-point wiring with only one connection per contact, and board reusability—these IDC capabilities all promise simpler, more cost-effective designs.

The latest IDC-based circuit-fabrication product comes from Information Machinery Corp. The Quick Stuff GP/120 general-purpose breadboarding tool consists of a 10-by-12-in. fiberglass-reinforced epoxy printed-circuit board and an assortment of 16-, 18-, 20-, 24-, and 40-pin sockets, which may be combined on the board to accommodate all popular discrete components and integrated circuits in dual in-line pack-





DDC introduces the world's smallest 1553 data bus transceiver.

The DDC-8553 data bus transceiver is small in size and big in benefits. Packaged in a single 24-pin DDIP hybrid, the 8553 consumes about one-half the power of other units. The hybrid is supplied with an external transformer for easy interfacing with the 1553 data bus.

DDC's capability extends to the complete MIL-STD-1553 A and B. The transceiver/transformer is also available as part of a discrete RTU module, complete with encoder/decoder and serial-to-parallel converter.

Consider the DDC-8553 transceiver for your 1553 data bus requirements and see how it can benefit your design. To find out more, write or call Department A-1 today.

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LOS ANGELES: ILC Data Device Corporation, Dept. A-1, 7337 Greenbush Avenue, No. Hollywood, CA 91605 (213) 982-6454, TWX 910-499-2674; **LONDON:** DDC United Kingdom Ltd., Dept. A-1, 128 High Street, Hungerford, Berkshire RG17 ODL, England (44) 4886-2141/2142, TLX 851-848826; **PARIS:** DDC Electronique, Dept. A-1, 4 Rue De Abreuvoir, 92400 Courbevoie, France TLX 842-630609

Circle 175 on reader service card

ages with up to 64 pins. The GP/120 also comes with bypass capacitors, power connectors, and a pencil-like, hand-held wiring tool.

Each socket in the GP/120 contains an insulation-displacement contact made of beryllium-copper for durability. The contacts accept one or two AWG 30 solid copper wires, piercing their insulation as they are pushed into the socket by the wiring tool. Wrong connections are corrected by simply lifting the wire out of its contact; omissions are corrected by adding new leads, since the IDCs allow the equivalent of four wrapped-wire levels on one surface. At the end of a project, a designer can strip the board by pulling out all the leads, making it ready for reuse in a matter of minutes.

The GP/120 operates from 0° to 50°C at 90% noncondensing humidity. The system has large power and ground planes and heavy decoupling capacitance to reduce noise and crosstalk.

Pricing on the GP/120 starts at $215, with delivery of the device in three weeks.

Information Machinery Corp., 110 Middlesex St., Chelmsford, Mass. 01863. Phone (617) 251-3270 [392]

Test system accepts up to 64-lead sockets and carriers

A socket-and-carrier test system series accepts a wide range of leaded chip-carriers and four-sided flat packs with leads on 0.040- and 0.050-in. centers (up to 64 and 48 leads respectively). The series is designed for leaded chip-carriers and other four-sided packages that measure up to 0.600 and 0.750 in. on a side, but will accept other package sizes after minor tooling adjustments. The contacts give firm wiping action but do not damage device leads. The carrier protects the device leads completely, allowing testing or aging setups to be made quickly and efficiently. The sockets' lid design eliminates shorting against contacts; the lid will not separate from the socket body under normal usage. Other features include integral chassis mounting holes and minimum lid overhang at the back of the socket to maximize the density with which printed-circuit boards may be mounted.

The socket-and-carrier systems are available from stock. Prices vary according to material, number of contacts, and quantity required. For example, at the 100-unit quantity, a typical Polysulfone 40 contact socket is priced at $11.62 and its carrier sells for $1.15.

3M Electronic Products Division, Textool Products Department, 1410 West Pioneer Dr., Irving, Texas 75061. Phone (214) 259-2676 [393]

System solder-coats, levels more than 100 boards an hour

A system for automatically solder-coating and leveling up to 140 printed-circuit boards per hour is fully enclosed and features photoelectric cells to protect the operator. The Levelair model 07 also has an automatic fail-safe mechanism for holding boards. This mechanism may be equipped with a pneumatic board clamp for higher production rates. The board clamp has a quick-release safety fixture and handles boards or panels up to 0.25-in. thick and 18 by 24 in. in size. The system automatically fluxes, solder-coats, and levels a board in one operational sequence. It measures approximately

5 by 4 by 8 ft. Production rates will generally range between 100 and 120 panels/hr, but some test facilities have reported 140 panels/hr. The standard 07 model starts at $46,000. Delivery is between 20 and 22 weeks.

Electrovert Inc., 86 Hartford Ave., Mount Vernon, N. Y. 10553. Phone (914) 664-6090 [398]

S-100 boards are coated with positive resist

Custom circuit boards can be prepared for S-100 bus systems without photonegative processing by using a five-component system that requires less than an hour to do the job. At the heart of the system is a positive-resist-coated circuit board that is double-sided and copper-clad—the model 8800R2. The FR4, G10 epoxy-glass board measures 5.3 by 10 by 0.062 in. and is form- and bus-compatible with the S-100 convention. At the lower edge there are 100 contacts (50 on each side) on 0.125-in. edges.

The card-edge contacts, which are gold-flashed and nickel-plated, continue into the 2-oz copper fields so that no jumpers are required after etching. Both sides of the board are precoated with positive photoresist. The board comes with layout paper, clear Mylar film for artwork, a heavy plastic bag for etching, and complete instructions. To fabricate a custom board with this system, artwork is rubbed down on the Mylar film, then placed over the sensitized board and exposed to an ultraviolet lamp or direct sunlight. Etching is accomplished with either ferric chloride or ammonium persulfate in the heavy plastic bag that is supplied. The positive photoresist boards are priced at $19.95 each and are available from stock.

Vector Electronic Co., 12460 Gladstone Ave., Sylmar, Calif. 91342. Phone (213) 365-9661 [394]

1,600-point test heads lock in place with one motion

Each of the five test heads in an OB8000 interface test fixture has a 1,600-point capacity. The heads lock easily into place with a single hand motion that establishes electrical and vacuum connections. The OB8000 has a vacuum seal, impact-resistant construction, and a tough vinyl coating. Recessed construction protects electrical contacts from damage, and the test fixture's design ensures easy access to the probes. The unit is readily interfaced with virtually any automated test equipment. Prices for the heads start at $525; deliveries start this month.

Ostby and Barton Co., 487 Jefferson Blvd., Warwick, R. I. 02886. Phone (401) 739-7310 [396]

Instruments

Smart digitizer resolves 8 bits

Computer-controlled fast instrument has 32 kilowords of memory, sells for $27,000

$27,000 sounds like a lot of money to pay for two channels of analog-to-digital conversion, and for most converters it is. But the model WBD-210 wideband 8-bit digitizer from Bancomm Corp. puts enough analysis capability behind those two channels to justify the price for users who want to perform very complex signal capture and analysis routines totally under the control of a PDP-11 computer.

The instrument contains 32,768 16-bit words of read/write random-access memory, which alone can cost about $12,000, according to David C. Robinson, Bancomm's vice president of marketing. "When the memory isn't being used for signal processing," he notes, "it can be used as additional RAM by the PDP-11." Robinson characterizes the intended applications of the WBD-210 as those in which minute transient analysis is very important. Examples are the analysis of radar returns by the military and the study of power-line deviations by electric utilities.

The digitizer can sample signals at each of its two ports at rates up to 10 MHz or at a single port at rates to 20 MHz. It can also convert digital data back into analog samples at the same rates. For simultaneous reading and writing, however, the rates are reduced by half.

The WBD-210's memory structure allows digitized data to pass through it continuously while the data is being analyzed for certain features. Once a feature is recognized, the data segment of interest may be captured for further analysis, modification, or transmission to external analog or digital analysis equipment. The transmission rate is under software control, as are all the digitizer's control settings. This not only means that the digitizer's control functions can be altered on the fly, but also that it can put out data at rates that are not related to the input rate—in synchronism with an external clock, for example.

The digitizer's 32-kiloword memory is partitioned into 32 K high- and low-byte sections. It may be further partitioned into 256 subpartitions whose size, address range, and allocation are under software control.

Management of the bidirectional flow of data between the digitizer and the PDP-11's Unibus is handled by the instument's priority arbitration and control section. This section sets the software-controlled sample rates, address locations, and PDP-11 interrupts and also establishes priorities among its read, write, and simultaneous read/write functions.

Delivery time for the digitizer ranges from stock to 120 days.

Bancomm Corp., 1121 San Antonio Rd., Palo Alto, Calif. 94303. Phone (415) 969-7555 [351]

Digital rf power meter performs nine functions

A nine-function digital directional radio-frequency wattmeter operates at power levels from 100 mW to 10 kW and from 500 kHz to 2.3 GHz. The model 4381 RF Power Analyst calculates parameter products, such as the voltage standing-wave ratio, that used to require consulting a graph or a chart. The VSWR is calculated continuously and is displayed at the touch of a button, as is decibel return loss. By pushing another button, continuous-wave or frequency-modulation power in both forward or reflected directions is displayed in watts or dBm. The device also indicates whether undesirable amplitude modulation is present and, if so, how much. Two other buttons call up peak envelope power in watts, and a third is for percent modulation. Another set of three buttons includes a delta function that identifies either rise or fall

in displayed values, and a minimum or maximum memory that recalls optimum conditions during adjustments.

The model 4381 is the first of a 4380 series of devices; other models in the series measure up to 250 kW, are panel-mounted, or both. The accuracy of model 4381 is within ±5% of nominal full scale, and the VSWR is a 1.05 maximum to 1 GHz in 50-Ω systems. The unit includes a light-emitting-diode display with decimal point. Overranging of up to 120% in watts and 400% in dBm retains up-scale accuracy and often makes it unnecessary to change to a higher-power plug-in element (which determines full-scale power and frequency range).

The model 4381 sells for $590, with 90-day delivery.

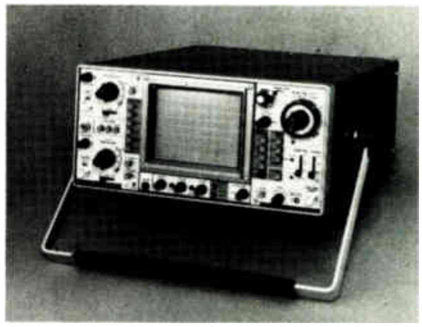
Bird Electronic Corp., 30303 Aurora Rd., Cleveland (Solon), Ohio 44139. Phone (216) 248-1200 [355]

Dual-channel 35-MHz scope is priced at $1,595

A 35-MHz dual-channel portable oscilloscope with a chopping frequency of 500 kHz will sell for $1,595. The model 5630 has sweep rates of 0.1 µs/cm to 0.5 s/cm in 21 steps for both the main (A) and delayed (B) sweep channels. A 10× magnifier can increase the maximum sweep rate to 10 ns/cm.

The vertical axes have 3-dB passbands that extend from dc to 35 MHz. Normal sensitivity is 5 mV/cm to 5 V/cm in 10 steps. A 5× magni-

New products



fier increases this sensitivity to 1 mV/cm. A signal-out port on one channel permits the scope to be used as a preamplifier for other instruments. It also allows cascading of the two vertical amplifiers for increased sensitivity.

In its XY mode, the scope has a 3-dB passband that extends from dc to 2 MHz with deflection factors that range from 5 mV/cm to 5 V/cm in 10 steps. The Z-axis bandwidth is dc to 5 MHz.

Maintenance of the 5630 is made easy by its modular construction and by the manufacturer's board-swapping program. Except for the cathode-ray tube, which has a one-year warranty, the scope is guaranteed for two years. Delivery time is about four weeks.

Kikusui International Corp., 17121 South Central Ave., Unit #2M, Carson, Calif. 90746. Phone (213) 638-6107 [354]

100-MHz dual-trace scope has digital multimeter option

The OS3600 is a portable dual-trace oscilloscope with a 3-dB passband that extends from dc to 100 MHz. Vertical sensitivity is 5 mV/cm over the full bandwidth and 2 mV/cm up to more than 85 MHz. The 8-by-10-cm cathode-ray tube in this instrument has a parallax-free illuminated internal graticule and uses a 16-kV accelerating potential so that it can display narrow pulses that occur at low repetition rates. The two channels can be displayed individually, alternately, chopped, or added algebraically. In addition, an XY mode can be displayed.

A trigger-view facility displays up

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Circle 183 on reader service card

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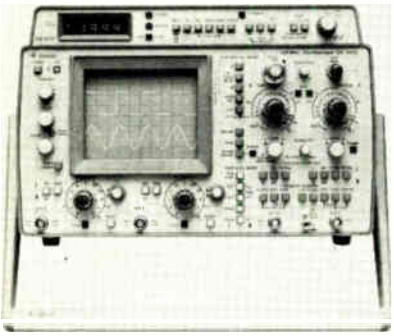


to three traces; up to four traces may be displayed in the alternate-sweep mode—the two channels, the intensified main time base, and the delayed time base. Horizontal sweep speeds of both the main and delayed time base are continously variable over 22 steps from 50 ns/cm to 0.5 s/cm in a 1-2-5 sequence, with a maximum effective sweep speed of 5 ns/cm at 10× magnification. The oscilloscope weighs 22 lb. An optional 3½ digit multimeter option—the DM3010—is available to be fitted or retrofitted at the factory. When used with the scope, it measures signal amplitude (±2% ±2 digits uncertainty), time (±1% ±2 digits), and frequency (reciprocal of an equivalent period ±1 digit). It can also be operated independently to measure dc voltage, current, and resistance. The oscilloscope with probes sells for $2,699; with the DM3010 option, it is $3,299. Both units carry a two-year warranty and can be delivered in 60 days.

Gould Inc., Instruments division, 3631 Perkins Ave., Cleveland, Ohio 44114. Phone (216) 361-3315 [356]

Ramp-function generator controls voltage or current

A digital ramp- and step-function generator—the model 338—has both voltage and current source outputs. The voltage source output provides 0 to ±12 v dc into a minimum load of 250 Ω. The current source output provides 4 to 20 mA dc into a maximum load of 2,000 Ω or 10 to 50 mA dc into a maximum load of 800 Ω. An overall current source range of 0 to 120 mA dc is possible under proper load considerations with derated accuracies. Thumbwheel switches set the upper and lower limits of the voltage or current span with an uncertainty of ±0.05% of the full-scale range.

The output level may be held and then stepped immediately to either limit or from limit to limit. The output may ramp at rates ranging from 10 V/min to 0.25 V/min toward either limit. An external hold input stops the ramp and holds the output at a constant level until the input goes high. The normal mode may be switched off, and the output may be controlled by a 10-turn manual potentiometer.

The unit may be used as a dynamic calibrator for signal-conditioning devices which normally receive 4-to-20-mA, 10-to-50-mA, or 0-to-12-V input signals from sensors or transducers. The unit's ramp is made up of 119,990 steps for the 0-to-11.999-V span. This provides a ramp-step resolution of 100 microvolts per step.

The generator occupies 5¼ in. in a standard 19-in. rack by means of rack mounting adapters supplied with the unit. The model 338 is priced at $2,495.

Exact Electronics Inc., P. O. Box 347 Tillamook, Ore. 97141. Phone Joe Foster at (503) 842-8441 [358]

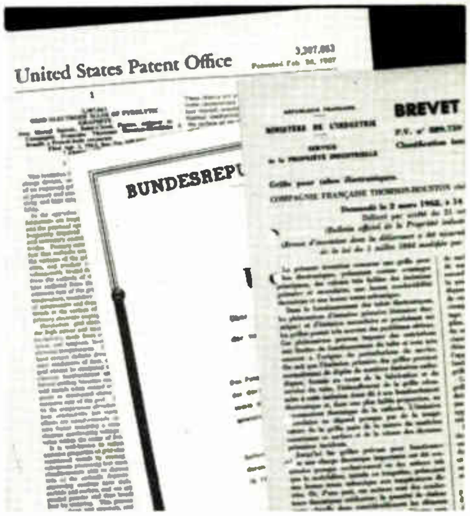
30-MHz scope has delayed sweeps from 1 μs to 100 ms

A 30-MHz oscilloscope offers delayed sweeps in five ranges—from 1 μs to 100 ms. Vertical input sensitivity is 2 mV/9.5 mm. Waveforms with repetition rates to 25 kHz can be expanded up to 1,000 times; minimum expansion at 30 MHz is five times. The time-base calibration is no more complex than on ordinary triggered scopes. The model 1530 also features variable hold-off. It sells for $1,340 and is available from distributors.

B&K-Precision, Dynascan Corp., 6460 West Cortland St., Chicago, Ill. 60635. Phone (312) 889-9087 [359]

15 years of progress in pyrolytic-graphite grids

Today, THOMSON-CSF is not alone in vaunting the merits of pyrolytic-graphite grids. There is one highly important fact to remember, though – **no one has more experience with pyrolytic-graphite grids than** THOMSON-CSF. Why? Simply because **we developed these revolutionary Pyrobloc® grids way back in 1964!** And we've been improving them ever since. By now, pyrolytic-graphite grids have become world-famous, because of their vastly improved mechanical and electrical characteristics. Nearly all high-performance THOMSON-CSF tubes now have Pyrobloc grids. For example, the five tubes in our radio-broadcasting-tetrode line – which provide from 50 to 500 kW of carrier power from a single-tube final RF stage. With Pyrobloc grids and **Hypervapotron® anode cooling** – another THOMSON-CSF discovery – they offer an unbeatable combination of high power, compactness, overload safety, low weight and reliability, for **any** short-wave transmitter. To sum up, for the **latest and best in power-grid tube technology,** there's only one place to come: **the Electron Tube Division of THOMSON-CSF.** Where we're now celebrating 15 years of progress in pyrolytic-graphite grids!



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Circle 187 on reader service card

New products/materials

A dispersed-nickel coating can be sprayed onto plastic enclosures to shield against electromagnetic interference. Xecote has a surface resistivity of 1 Ω/sq. The conductive material can be applied to such plastics and metals as acrylics, polycarbonates, polyphenylene oxide, fiberglass, and sandblasted steel. A 2-to-3-mil coating of Xecote can provide 45 dB of attenuation at 10.3 GHz, 39 dB at 1.0 GHz, 53 dB at 0.45 GHz and 64 dB at 0.09 GHz. The materials were subjected to five thermal shock cycles according to MIL STD 202E, method 107D, condition A, and to a 48-hr salt spray test per MIL STD 202E, method 101D, condition B. One gallon of the material can cover 270 ft^2.

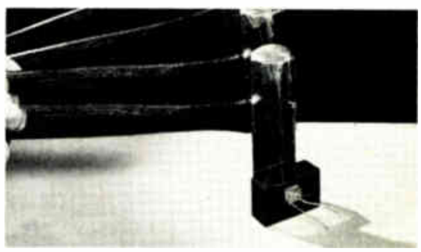
Metex Corp., Metex Electronic Shielding Group, 970 New Durham Rd., Edison, N. J. 08817 [476]

A glass paste fired at 560° to 600°C can be used to seal alumina and other substrate materials with similar coefficients of expansion. When fired, ESL 4026 sealing glass produces a clear transparent seal with a controllable 8-to-25-μm thickness. The material may be used in contact with various thick- or thin-film conductors.

Electro-Science Laboratories Inc., 2211 Sherman Ave., Pennsauken, N. J. 08110 [477]

This epoxy-resin system, Stycast 1426, has a high impact strength. The one-component material has a shore D hardness of 72 and a flexural strength of 15,500 psi. Viscosity is 70,000 cps at 25°C, and the volume resistivity is more than 10^{14} Ω-cm at 25°C. The material can be cured at 175°F.

Emerson & Cuming Dielectric Materials, Dewey and Almy Chemical Division/W. R. Grace & Co., Canton, Mass. 02021 [480]



Microcomputers & systems

Unit emulates slave processors

ICE-41A makes possible the simultaneous emulation of an 8085 and an 8741A/8041A

When Intel Corp. introduced its Multi-ICE software package for multiprocessor system development last year [*Electronics*, June 21, 1979, p. 191], it promised to come up with in-circuit emulation for combinations of chips other than the 8085 and 8049 families at a later date. And Intel has delivered. The new offering, ICE-41A, allows the emulation of slave chips such as the 8741A and 8041A universal peripheral interface microcomputers. Last year's Multi-ICE software enabled concurrent operation of two ICE-85s or an ICE-85 and an ICE-49; now ICE-85 can be teamed with ICE-41A.

The ICE-41A in-circuit emulator not only supports the specialized mnemonics of the 8741A/8041A, but it also provides the Intellec development systems with a way to examine previously inaccessible nodes that connect on-chip memory and logic in these processors. Accessing these nodes is especially important with the 8741A and 8041A because, unlike the 8085 and 8049 families of processors, these slave chips do not access the system bus. The appearance of the ICE-41A package should thus bring great relief to users of the SBC-80/30 single-board computer and other designs that contain 8085-type master processors and 8741A/8041A slaves.

Like its ICE-85 and ICE-49 predecessors, ICE-41A allows system designers to perform symbolic debugging of programs. Symbolic debugging frees the designer from having to keep track of addresses. Instead, names or symbols are assigned to subroutines and other data, letting the ICE-41A and Intellec keep track. In all, 18 symbolic commands, along with a broad range of modifiers, allow the designer to do such things as insert subroutine names into breakpoint commands to start and stop real-time emulation at specific points in the program. And with the Multi-ICE software, breakpoints in the ICE-41A emulation program can also be used to start and stop the activity of the 8085 processors; similarly, breakpoints in the 8085 can start and stop the ICE-41A. This allows the designer to coordinate the simultaneous activities of the master and slave processors.

The complete ICE-41A emulation package, with emulation and control boards that plug into the Intellec chassis, buffered cabling to interface the development system with the user's prototype, and an operating manual, costs $4,200. An enhanced Multi-ICE software package, able to recognize the ICE-41A emulator, costs $1,750. However, those who purchased the original Multi-ICE software package can have the enhanced version of the software free of charge.

All these configurations are available from stock.

Intel Corp., 3065 Bowers Ave., Santa Clara, Calif. 95051. Phone (415) 987-8080 [371]

Package adapts Exorcisors for 6805 development

The USE-6805 support package adapts existing Exorcisor development systems and Exorterm data terminals so they can function as development stations for the 6805 microprocessor. Included in the package are a printed-circuit module, extender cables for the system under test, and a diskette containing a macro assembler and a program for debugging and monitoring called Fivebug.

In addition to comprehensive debugging features, the package allows true, real-time emulation of the 6805 microprocessor. Moreover, the system can develop multiprocessor configurations while debugging one processor at a time. It can do this because of the two-processor architecture used in the USE-6805. The 6805 on the module communicates with a 6800 in the development system through special status/control registers and shared memory. This arrangement is isolated enough, however, to permit full use of existing 6800 hardware and software.

The package allows the use of all on-board memories—random-access, erasable programmable read-only, and external. It also permits the use of the single-step and set-breakpoint functions—halt on address—for programs in these memories. Up to eight breakpoints can be set in programs in an on-board RAM. Memory block A–F in the user's Wire-Wrap area is fully decoded, for whatever circuit implementation is required by a custom user. The user may operate the system in the standalone mode by forfeiting interrupt-driven debug capabilities. A program in E-PROM, internal ROM, or external memory can be run in real time.

The minimum system requirements for the use of the MC6805 are: an Exorcisor 1, 2A, or 2, with Exorterm 100 or 150—or an Exorterm 200 or 220; an Exordisk II or III/IIIE; and a 24-kilobyte memory.

The USE-6805 support package, which can be ordered from the company as part number MEX6805, sells for $2,000. A user's guide is included.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 962-2209 [375]

Database manager meets Codasyl recommendations

A data-base management system for microcomputers meets the recommendations of the Conference on Data Systems Languages, better known as Codasyl. The system is called Micro-SEED because it is a compatible subset of the SEED DBMS that was originated by International Database Management Systems Inc.

in Philadelphia, Pa. Micro-SEED runs under Digital Research Inc.'s CP/M operating system with the manufacturer's own Fortran-80 as the host language and is especially useful for microcomputers whose data base is too large for conventional file-handling methods. In addition to meeting the Codasyl recommendations, Micro-SEED self-optimizes find commands. The system is written primarily in Fortran with isolated assembly-language routines for input/output and buffering. It is easily transported to various 8080 or Z80 hardware configurations. Because it is implemented under CP/M like a Fortran application, it does not place much of an extra burden on operating system tasks. A 64-kilobyte microcomputer system is required to support the data-base management system.

Micro-SEED uses the Codasyl-recommended schema, sub-schema, and area methods to divide and define the data base, thus providing easy access from user programs. The routines for managing the data base are then called from the user's application programs, written in Fortran, or in another host language. Additional host languages will be supplied later this year along with a relational query language and report generator and with an interactive system utility program that will both be available as add-ons to versions of Micro-SEED that are upward-compatible and utilize 16-bit microprocessors.

The single-copy price for Micro-SEED is $900. License agreements are available for original-equipment manufacturers.

Microsoft, 10800 Northeast Eighth, Suite 819, Bellevue, Wash. 98004. Phone Bob O'Rear at (206) 455-8080 [373]

Macro assembler and loader developed for 8086/8088

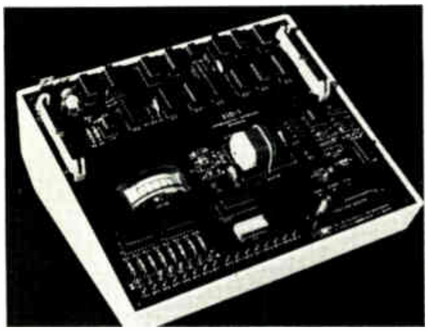
A relocatable macro assembler, linking loader, and simulator for the 8086/8088 microprocessor has programs written in the ANSI standard Fortran IV and will run on any general-purpose computer, including 16-bit minicomputers. The assembler includes conditional and macro assembly and a symbol or cross-reference table. The object module output of the assemblers may be in a relocatable format or may be produced directly in Intel's hex format. The assembler provides for program, data, stack, and common segments. The linking loader combines several independently assembled relocatable object modules into a single absolute program. Thus, large programs are subdivided into smaller units, reducing assembly time and allowing errors to be corrected efficiently. The simulator simulates all aspects of the microprocessor, including the full 1 megabyte of memory. It provides input/output simulation for debugging a program easily. The user may specify any memory location to have a breakpoint or to be read only.

The assembler and linking loader together sell for $1,250. The simulator is $1,000. Accompanying each software order are: a manual, source program and listing, and test program and output listing.

Microtec, P. O. Box 60337, Sunnyvale, Calif. 94088. Phone (408) 733-2919 [374]

Trainer emphasizes analog interfacing

A trainer for demonstrating the principles of analog interfacing with a microcomputer can be adapted for use with 8080-based microcomputers. The EID-1 Experimental Interface Designer can be connected directly to the manufacturer's own 8080-based training and design microcomputers—the MMD-1 or the MMD-2. Built-in components such as a photocell, temperature sensor, dc meter, slide potentiometer, and dc motor provide input/output signals that represent such variables as light intensity, speed, temperature, and position. A light-emitting-diode readout displays analog signals that have been converted to digital form. Digital signals can be generated using an on-board eight-position



dual in-line package switch. Computer output can be converted to analog signals for meter display or motor speed control. The on-board analog-to-digital and digital-to-analog converters can also be used to bring in or send out control voltages directly on breadboarding terminals.

An assembled EID-1 sells for $225. In kit form it sells for $160. Both are available from stock or up to 30-day delivery.

E&L Instruments Inc., 61 First St., Derby, Conn. 06418. Phone (203) 735-8774 [377]

Racks hold 4.25-by-6.5-in. STD BUS IC cards

Four-, eight-, and sixteen-slot card racks, each containing an STD BUS motherboard and card edge connectors, hold all standard 4.25-by-6.5-in STD BUS integrated-circuit cards. The STD BUS, conceived by Pro-Log Corp. and developed with Mostek Corp., permits design engineers to interchange cards on 8-bit microprocessors for maximum flexibility. The racks have open-end panels and are convection cooled. They are made of injection-molded thermoplastic polyester.

The four-slot card rack (model CR4A-1) is priced at $120; the eight-slot rack (CR8A-1) sells for $150; and the 16-slot version (CR16A-1) goes for $195. Purchasers of large quantities of racks can receive substantial discounts. An optional nine-pin locking power-supply cable assembly and mating connector are also available with each model for an additional cost.

Pro-Log Corp., 2411 Garden Rd., Monterey, Calif. 93940. Phone (408) 372-4593 [378]

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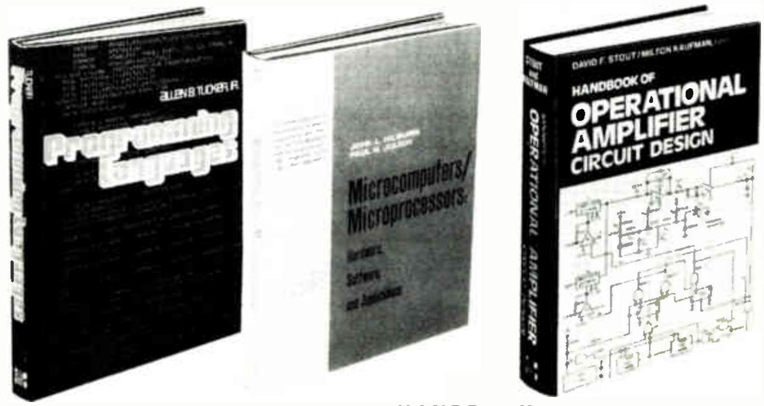

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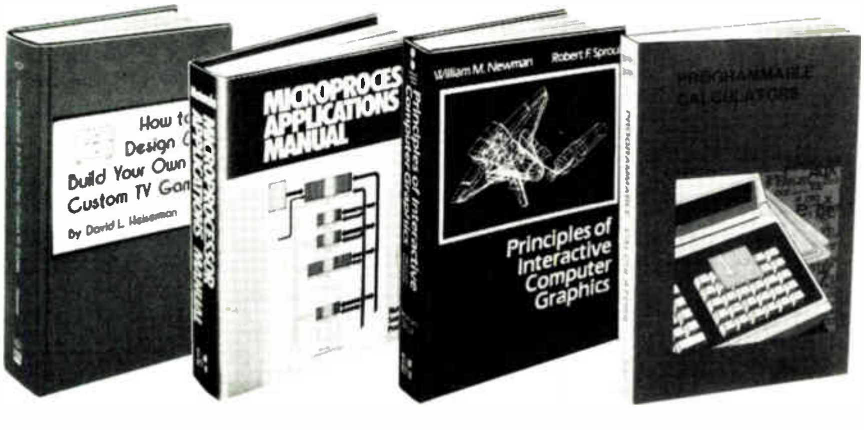

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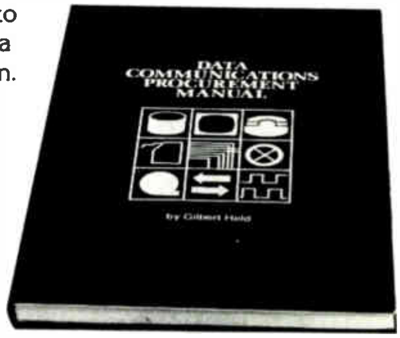

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Du Pont to test screenless pc-board printing system

The Du Pont Co., Wilmington, Del., plans to field-test a screenless image-transfer printing system for printed-circuit boards this year. Called Cirtrak, **the system uses thermomagnetographic technology, which is especially suitable for producing boards with line widths and gaps as narrow as 15 mils.** The heart of the system is a premagnetized printing plate with a chromium dioxide coating. When covered with conventional artwork and exposed to a special light source, the plate loses its magnetism in the transparent areas of the artwork. The image thus formed, developed by a magnetic toner, is then transferred to a copper panel, where it is fixed by heating. At least 500 copies can be run from each master plate. The hardware for the Cirtrak system will probably range between $80,000 and $100,000, with leasing a possibility. The concept will be introduced in the U. S. at Nepcon next month.

National sets new AS/7031 pricing

The purchase price of the AS/7031 processor from National Advanced Systems Corp., Palo Alto, Calif., has been established at $600,000 and leasing arrangements have been realigned to offer three short-term options—18, 24, and 36 months. (National Advanced Systems is the company formed by the transfer of Itel Corp.'s IBM-compatible computer operations to National Semiconductor Corp. [*Electronics*, Jan. 3, p. 50].) **The AS/7031, which is comparable to IBM's 3031, uses 16-kilobit memory technology and supports all IBM 370 and 303X operating systems and their extensions.** New list prices for the company's 370/158, 168, and 3033 memory are set at $40,000 a megabyte.

Symmetry improves multiprocessor throughput by 50%

Throughput improvements of up to 50% over traditional master-slave dual-processor DECsystem-10 configurations are claimed for the full Symmetric Multiprocessing (SMP) capability recently announced by Digital Equipment Corp. for its DECsystem-1090. According to the Maynard, Mass., firm, **SMP can accommodate up to 175 active jobs or 512 transaction-processing or dedicated terminals.** A minimum configuration DECsystem-1090 SMP, with two processors, 1 million words of memory, one disk drive, 16 terminal lines, and an SMP operating system, is priced at $1,250,000. Master-slave configuration DECsystem-1090s can be adapted in the field to SMP at prices starting at $10,000.

In dual-processor SMP operation, such as in the DECsystem-10, both processors are operationally equivalent, with each performing both computation and input/output functions. The operating system is re-entrant, and monitor calls can be executed by either processor.

Tally pares printer prices

Tally Corp., Kent, Wash., is cutting prices up to 20% on M series printers in the Tally/Mannesmann line. **The price of the M80 MC, a fast 80-column serial printer with optical character recognition and bar-code printing, has been reduced to $2,445.** An M78 Trimform printer that automatically cuts forms to any length has had its price rolled back to $4,345. Finally, the price of the M184 dual-document printer has been lowered to $4,545. Substantial quantity discounts are available.

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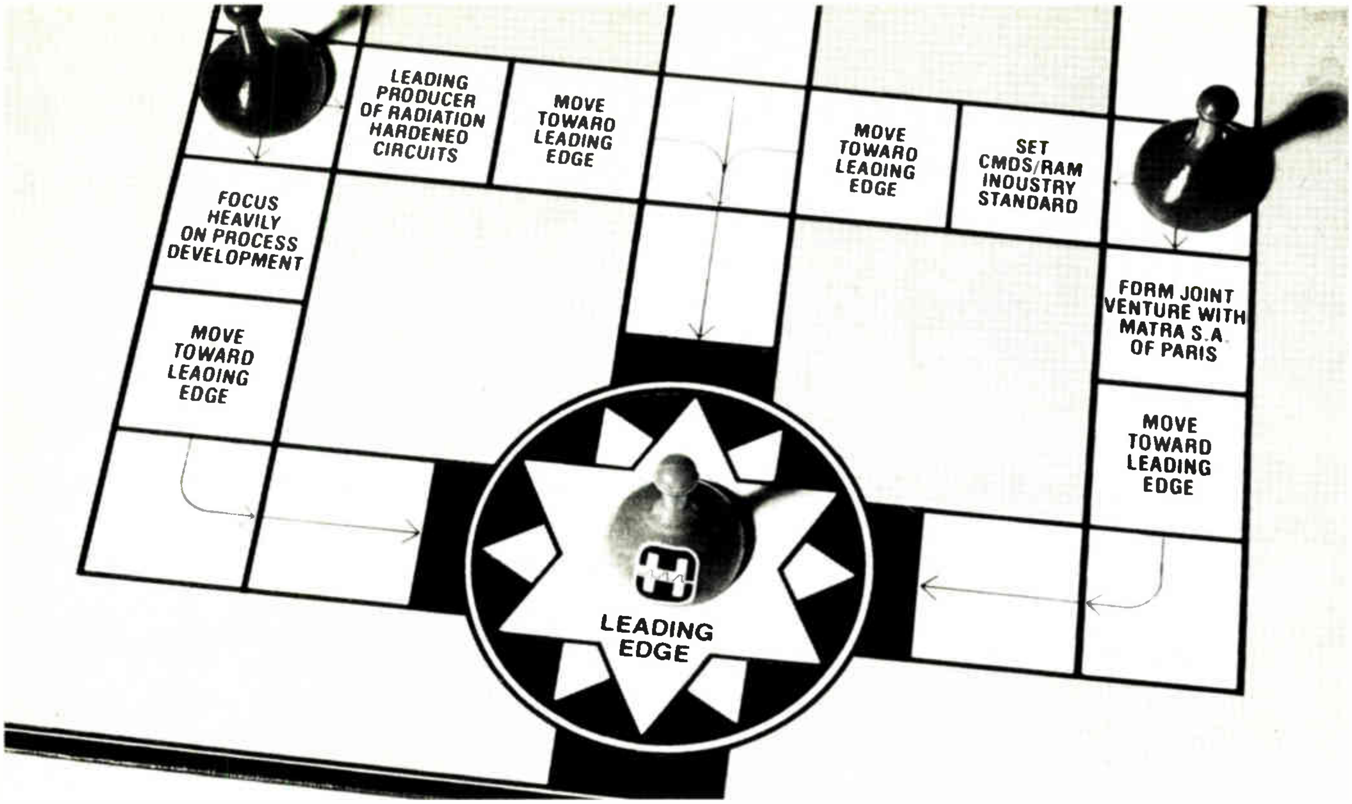

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