DECEMBER 20, 1979

ISSCC: NO SLOWDOWN IN INNOVATION/73

Developing a microcomputer operating system/104

Single chips tackle digital filter algorithms/109

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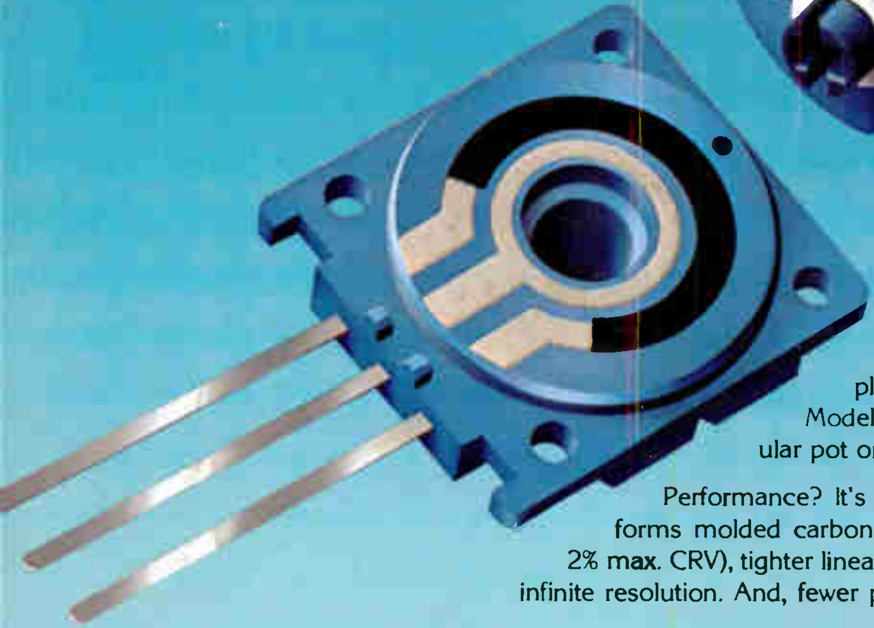

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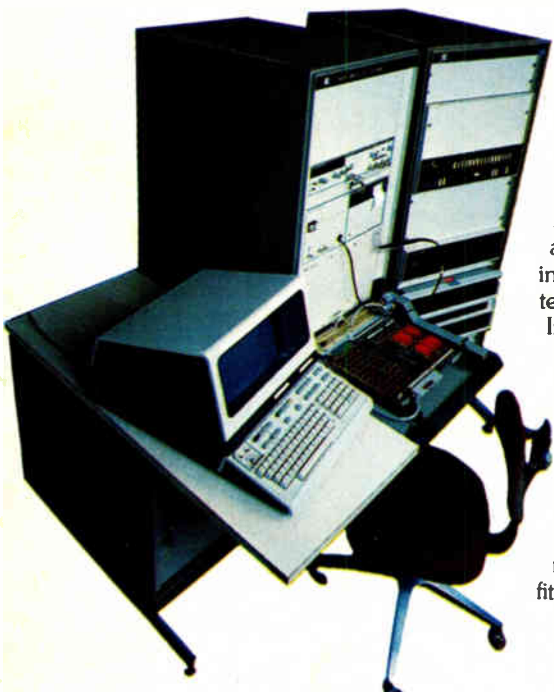
Simulator-based testing defined. Board-test simulation is a technique in which the circuit to be tested is modeled—component by component and node by node—in the test system computer. From this model, the system can calculate the correct response to any input pattern, plus predict failure modes and their responses. This allows only those patterns which identify faults to be used as the test pattern stimulus.

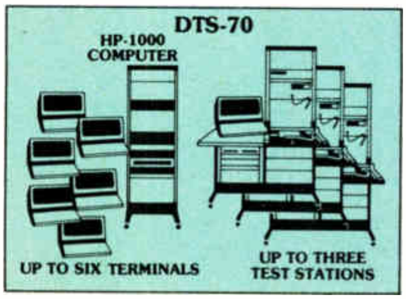
A major benefit of simulation is that it provides an accurate measure of test effectiveness. You know to what extent you're exercising board components. Thus you can determine test efficiency, and, just as important, you know when to halt test software development.



"SEE US AT THE ATE SEMINAR EXHIBIT, PASEDENA, CA'., BOOTHS 422-427"

Another benefit of having the circuit and all of its failure modes stored in the computer is that you then have detailed information to aid in fault isolation. Finally, advanced simulation techniques allow circuit modeling in the test system so that engineering can test designs before they're built and thus eliminate many problems before they reach production.

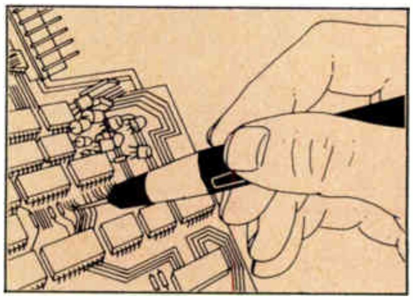
The advantages of test flexibility. HP's answer to simulation and to the reduction of testing costs and time is the DTS-70 Digital PC Board Test System ($90,350* for standard operating system). It provides the benefits of a simulator and offers other advanced features as well.



When you expand your production capacity, you can add test stations (to a total of three) without buying additional computing power. Need more test software development capability? Then simply add an inexpensive CRT terminal to your basic system. You can add up to six software development terminals, as shown, and they won't interfere with your production testing.

In addition, the DTS-70 software is compatible with data base management software to keep track of data and help you better manage your production. For example, the system can store test data and give you reports such as specific board or component failure rates and modes. The DTS-70 will easily fit into your long range computer network plans, too, providing distributed processing and communication to your data processing center.

Simplified troubleshooting. Testing isn't the only problem. You also need a rapid and inexpensive way to locate the specific faulty component or components for replacement. Using HP's FASTRACE software,



the DTS-70 accesses faulty board models developed by the simulator and guides the operator in a quick series of probe tests to isolate faults. Unlike many simulator systems, the DTS-70 catches intermittent faults. And it has zero delay capability, allowing you to detect races and hazards—a critical problem in logic circuit operation.

For more information. There are other benefits to PC board testing with the HP DTS-70. And for analog and hybrid circuit testing, HP offers the 3060A with combined functional and advance in-circuit testing. For data sheets on both these systems, write to Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304. Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.

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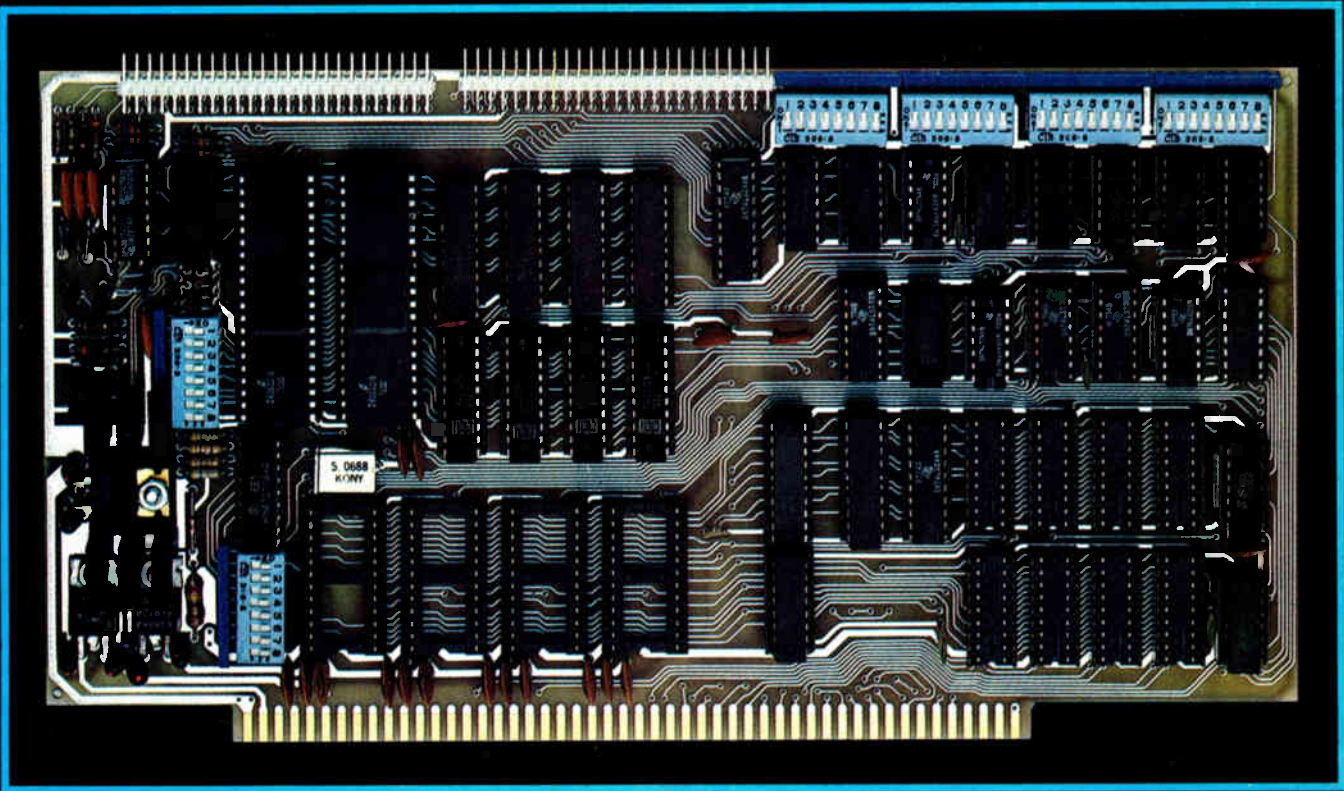

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Electronics

The International Magazine of Electronics Technology

Vol. 52, No. 26 • December 20, 1979

Highlights

Cover: Chip controls packet-network link, 89
A dedicated large-scale integrated circuit relieves a data terminal of time-consuming link-control chores at its interface with the packet-switching network and replaces a boardful of hardware.

Cover illustration is by Katrina Taylor.

Showdown postponed at WARC, 76
By putting off controversial issues—geostationary satellite spots and shortwave broadcast frequency allocations—the World Administrative Radio Conference avoided pitting industrialized nations against Third World countries.

Software mediates microcomputer conflict, 104
A modular operating system for 16-bit microcomputers provides many useful program-development tools and allows unneeded modules to be banished from main memory at run time to speed execution.

Math chips make one-board filters possible, 109
Real-time digital signal processors have become much easier to design since the advent of multiplier-accumulator chips. The resulting digital filters are both smaller and more economical.

. . . and in the next issue
The annual market survey and forecast for the U. S., Western Europe, and Japan . . . liquid-crystal-display array multiplexing . . . error-correcting circuits for microprocessor memory.

Electronics

Publisher's letter

Victor Hugo was not in the electronics industries, but his famous line "Greater than the tread of mighty armies is an idea whose time has come" has become a cliché in our technology. Clichés become so largely because they are true and easy to remember.

Once again it's true, this time in the case of the cover article (p. 89) on packet switching. Here the idea is a practical design of a packet-switching interface chip developed by Western Digital Corp., Newport Beach, Calif.

True, packet switching is an idea that has been around for some time—15 or 16 years ago this telecommunications concept was touted as a panacea for data transmission. Now, though, thanks to the availability of low-cost large-scale integration, it is possible today to design practical chips for packet-switching applications.

In the case of the Western Digital device, the final result was based on a considerable amount of consultation with network designers and telecommunications customers worldwide, according to author Geary Leger, systems applications engineer for Western Digital. In addition, Leger gained much insight into what would be required—and what would be the optimum number of features—by participating on the American National Standards Institute Public Data Networks Committee (X-3S37).

"Participation on standards committees is very important in the semiconductor industry," Leger stresses. "We cannot wait for a standard to be adopted before designing LSI parts. When you work on a committee, you see trends early."

The hardest part of the packet-switch interface chip design was holding down its size, Leger reports. A whopping 292 mils by 295 mils, the chip packs the equivalent of some 30,000 transistors. Along the way, Western Digital had to take out some of the features originally planned on the chip, which are now accomplished externally.

With a BSEE and an MSEE from the University of Missouri, 38-year-old Leger came to Western Digital in 1978 with data communications experience. He had never designed a chip before. "It was a new experience combining two different sciences," he recalls.

Speaking of communications, the 1,900-odd delegates to the World Administrative Radio Conference wound up 11 weeks of talks recently and the news is that the meeting did not turn into a pushing match between the developed nations and the developing nations.

The summary by Ken Dreyfack of our Paris bureau (p. 76) points out that like most successful deliberations, no one came away completely victorious nor was anyone completely beaten in the negotiations over the communications spectrum. However, a couple of the key issues on short-wave allocations and satellite positioning were left unresolved.

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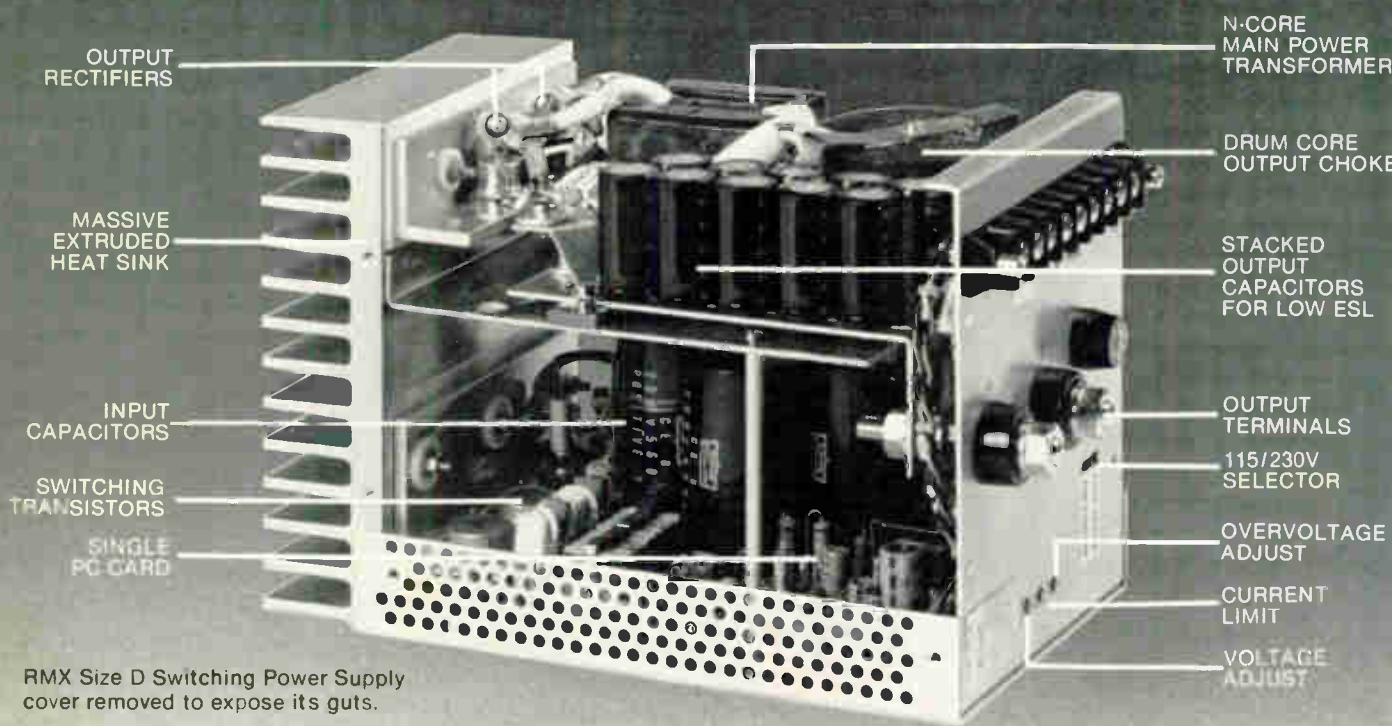

RMX Size D Switching Power Supply cover removed to expose its guts.

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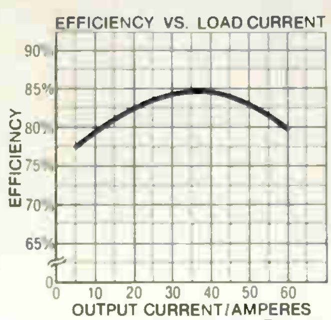
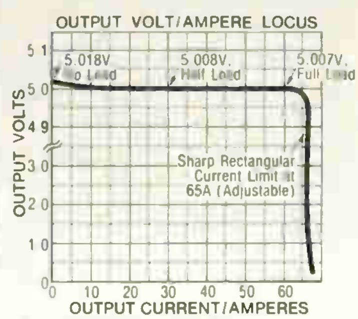
RMX 15-D	10.5-16.5	23A
RMX 24-D	16.8-26.4	16A
RMX 28-D	19.6-30.8	13.7A





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Readers' comments

Ground breakers

To the Editor: Your Sept. 13 article about Quick Connect, a Bell Labs insulation-displacing contact system for breadboard wiring, was of interest because 3M Electronic Products division has sold IDC breadboarding systems since 1975. Since 3M's pioneering work with Bell Labs was not mentioned, we feel your readers may be interested to learn about our breadboarding activities.

The first successful prototype ID-contacts used by Bell Labs for breadboarding were pulled from a Scotchflex connector. To simplify handling and soldering, Bell initially chose to group the contacts by cutting a 16-position connector for a dual in-line package into two contact strips, a configuration used by 3M today.

The latest 3M breadboarding system resulted from pioneering work done by Charles von Roesgen of Bell Labs. His laboratory experience was followed closely by 3M in designing reliable and practical techniques for breadboards to meet general needs. The 3M system allows the user to place contact strips on the board only where required and to feed two levels of wire (equivalent to four wrapped wires) through the contact.

Richard G. Barker
3M Center
St. Paul, Minn.

Computer error

To the Editor: In my letter on page 6 of your Oct. 25 issue regarding the "Which way is up?" editorial, the two computers I referred to were the TMS 1000 and IBM 4300, not the TMS 100 and IBM 4330 as they appear in print.

Andrew Allison
Los Altos Hills, Calif.

Off the drawing board

To the Editor: The Packaging and Production technology update [Oct. 25, p. 21] states that "better resolution is theoretically possible by using a scanning, or focused, ion-beam source, but this approach is still on paper." This approach is not still on paper: we have already developed and built an ion projection system

Readers' comments

using focusing ion-optical lenses. This system was described at a lecture held in Boston at the 15th Symposium on Electron, Ion and Photon Beam Technology.

Dr. Rudolf Sacher
Sacher Technik Wien
Vienna, Austria

A bit behind the times

To the Editor: In your Oct. 25 issue, in "Israel sweetens the pot" [p. 84], the caption accompanying the photographs contains a couple of glaring errors.

First, it should be quite obvious that the Egyptian president who appears here is Sadat and not Nasser. And the Egyptian and Israeli flags are flying side by side at the Advanced Technology Center—not Technion City.

Yoram Kenig
Motorola Israel Ltd.
Tel Aviv, Israel

■ *Reader Kenig was one of many to call our attention to this most embarrassing error.*

Not U. S. this time

To the Editor: In your Oct. 25 issue (p. 223) you state that the WARC (World Administrative Radio Conference) is a "U. S.-sponsored meeting." This meeting is under the sponsorship of the ITU (International Telecommunication Union), a United Nations entity.

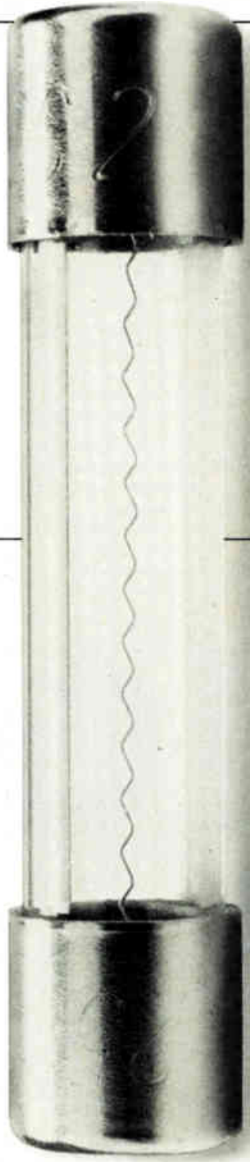
Jean-Pierre Bonneau
Montreal, P.Q.
Canada

■ Electronics *apologizes for the typo, which changed U. N. to U. S.*

Corrections

Analog Devices derives 10% of its total sales dollars from its system and subsystem level products, which include both the Macsym line and Analog input-output boards. The figure reported in the Nov. 8 issue [p.43] for the Macsym line of industrial controllers is incorrect.

On Fig. 3 and 4 of "Microcomputer can stand alone or join forces with other chips" [Electronics, *Dec. 6, p. 143*]*, serial input and output pins 11 and 12 were inadvertently transposed.*



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MATH CHIPS: PART TWO.

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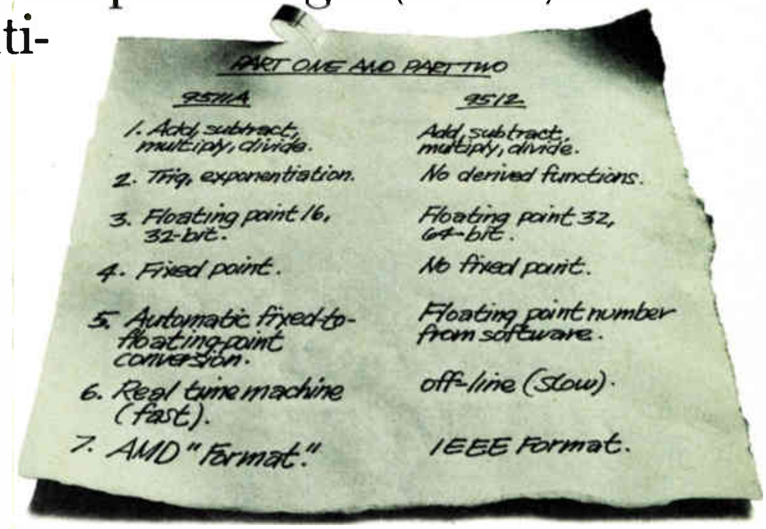
It's a monolithic arithmetic processor in the proposed IEEE format that offers the full range of simple math functions with floating-point single (32-bit) and



News update

■ The Federal Communications Commission's recent decision to deregulate private reception of domestic television broadcasts via satellite is good news to companies now marketing home earth stations [*Electronics*, Sept. 27, p. 46]. It may, however, also encourage the cable TV industry to tighten its control of satellite transmissions.

Earth station owners no longer face the expense of getting an FCC license, but they must still have permission from the common carrier whose transmissions are to be received. This is a regulation not easily enforced, notes Edward Taylor, president of Southern Satellite Systems Inc. in Tulsa, Okla. He says that broadcasting customers such as Home Box Office or Showtime are unhappy about the easy access nonpaying viewers will have to programs—pirating of broadcasts is a particular concern. Taylor believes the industry's response will be to install scrambling systems.

"Deregulation has given tremendous impetus to efforts at developing scrambling schemes, especially for video security," agrees Walter H. Braun, director of engineering at RCA American Communications Inc., Piscataway, N. J. The operator of two RCA Satcom satellites, the subsidiary is itself actively working on scramblers, Braun adds.

That a number of other firms are, too, may reflect a feeling that private earth stations, still a new and expensive phenomenon, may proliferate and become a threat (or at least a significant source of subscription revenues) in the future. One scrambling system, in the final development stages at ITT Space Communications Inc., will not only scramble video signals, but also multiplex audio into the video picture, says Emanuel Stein, research and development manager at the Raleigh, N.C., facility. The would-be pirate will thus face the double problem of unscrambling the video and retrieving the audio signal embedded in it. Such schemes should frustrate the estimated 1 million people illegally enjoying satellite broadcasts. **-Linda Lowe**

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People

Flat panels a coming market, says Stone—and Exxon

In early 1976, Garrett Stone had a great idea for a new product for Exxon Enterprises Inc.: a variable-displacement gasoline engine. But Exxon had a better idea: forget the engine, hire Stone. That's how Stone joined the company's technical ventures team and how in January 1978, at the age of 35, he helped found Kylex Inc., an Exxon subsidiary in Mountain View, Calif.

Stone is understandably bullish about Kylex's position. "No approach is funded by Exxon Enterprises unless it feels that the market addressed can become $100 million a year in 10 years or less," he says. "That ought to say something about how we view the flat-panel display market."

Kylex is not Stone's first startup venture. In the early 1970s he cofounded Micronetics Inc. in Burlington, Mass., a manufacturer of laser-trimming equipment that was sold to GenRad Inc. in 1973. And when he approached Exxon with the engine idea it was as cofounder of Tronchemics Research Inc., San Diego. With a BSEE from the Massachusetts Institute of Technology and an MBA from Harvard University, it is easy to see why Exxon felt Stone had just the right combination of technical and managerial skills to pilot the fledgling company.

Now after nearly two years of development, Kylex has entered the market with a liquid-crystal flat-panel display, the LX140 [*Electronics*, Nov. 22, p. 46]. "The need that we are addressing is that huge gap between a cathode-ray-tube display and a simple watch display," he observes. "A CRT can display about 2,000 characters and a watch is typically limited to 4. We are looking at those microprocessor-based applications where an inexpensive, interactive display of 40 to 400 or so characters can be useful."

Following Exxon policy, Stone is tight-lipped about products under development at Kylex, but it is not difficult to guess what will follow.

Getting under way. Stone says his market will be at least $100 million in a decade.

The present one-line display will become a two-line, four-line, or eight-line display. Then, instead of moving characters right to left on a one-line display, entire lines will scroll upward and downward in a semblance of a page.

Beers mans Boston post and prepares for ATE battle

In the early part of the 1980s, the fiercest instrumentation battle will be fought for shares of the automated test equipment market. And Terry Beers, head of Fairchild Camera and Instrument Corp.'s new Boston division, is already in the midst of that battle.

A seasoned campaigner who previously worked for Fairchild in the early 1970s before returning last January, Beers has also seen duty selling Teradyne test equipment. He was most recently the sales and marketing manager for Computer Automation Inc.'s 4900 series board testers.

In his new position as business unit director, Beers' first assignment will be to set up a command post in the Boston area. He has already narrowed the choice to somewhere near the northern intersection of Routes 3 and 128, long known as a strategic area for the electronics industry in the Northeast. From

there, he will direct the introduction in the U. S. of the Series 70 line of functional board testers, based on the Membrain line sold in England by Schlumberger Ltd's tester division.

"The System 70 represents the first major technology exchange between companies in the Schlumberger family," Beers points out. "Fairchild was missing a board tester from its line, and with the market in the $102 million to $105 million range, it made a lot of sense to get into it now."

It was logical for another reason, he points out. "Although the System 70 is based on a British design, it uses mostly American parts." This fact will make system integration, which will be done here in the U. S., much easier.

Changes coming. It will also make it easier to adapt the system to the U. S. market, and already Beers sees some changes that will be made. "The first thing that will probably happen is that the system will acquire some new technology Winchester disk drives that will be coming out in the first quarter of 1980—they're a good way to provide inexpensive mass memory."

Further down the line, he sees a change in pin electronics that takes advantage of one of Fairchild's fortes—emitter-coupled logic. "Americans are into ECL, and with the way the technology is going, it will definitely be needed to get faster test speeds."

Technological proficiency in such areas as ECL is one of the two major factors that will determine who will win the lion's share of the ATE market, Beers feels. "The silicon boys" he jokes, "are coming up with something new every day, and to be able to test all the functions that they're providing, the ATE business will have to become even more engineering-intensive."

The other major factor will be "the ability to provide the high level of support needed for sophisticated testers." Both will require a lot of money, Beers says, "so the deciding factor in the 1980s will be sustaining capital." □

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HP-IB: Not just a standard, but a decade of experience.

HP-IB is much more than just HP's implementation of IEEE Standard 488-78. It reaches beyond IEEE-488-78 to cover the operational area as well as the mechanical, electrical and functional specifications. For example, HP-IB systems incorporate a built-in, high level I/O language that saves you the time and expense of writing instrument drivers and configuring operating systems. It means powerful interfacing through a system in which a lot of the work has been done for you.

Expand your system through HP peripherals.

Many data acquisition and control applications require external mass storage for large volumes of data. HP mass storage media include high speed flexible discs capable of handling data at burst rates and a selection of fixed discs offering storage up to 120M bytes. These and other input and output peripherals tailored for HP desktop computers allow you to configure the system that meets your needs today and accommodates future growth, as well.

A wide selection.

We build a broad range of desktop computers, with one just right for your data acquisition and control application. From the low cost HP 9815 through the HP 9825, the standard for HP-IB controllers; the HP System 35 with BASIC and assembly language; and the HP System 45B with advanced graphics capability, every HP desktop computer has superior interfacing characteristics in terms of human engineering, ease of use and power.

A growth path.

HP can meet expanding needs with communication links from desktop computers to HP 1000 series computers. For multi-user, multi tasking problems, HP 1000 systems offer a range of compatible RTE operating systems with software options for data base management, factory data collection and graphics.

For more information. Call 800-821-3777, extension 137, toll-free day or night (Alaska and Hawaii included). In Missouri, call 800-892-7655, extension 137. Or write 3404 E. Harmony Road, Fort Collins, Colorado 80525.

For a demonstration. Call the HP regional office nearest you: East 301/258-2000; West 213/877-1282; Midwest 312/255-9800; South 404/955-1500; Canada 416/678-9430.

408/10

HEWLETT PACKARD

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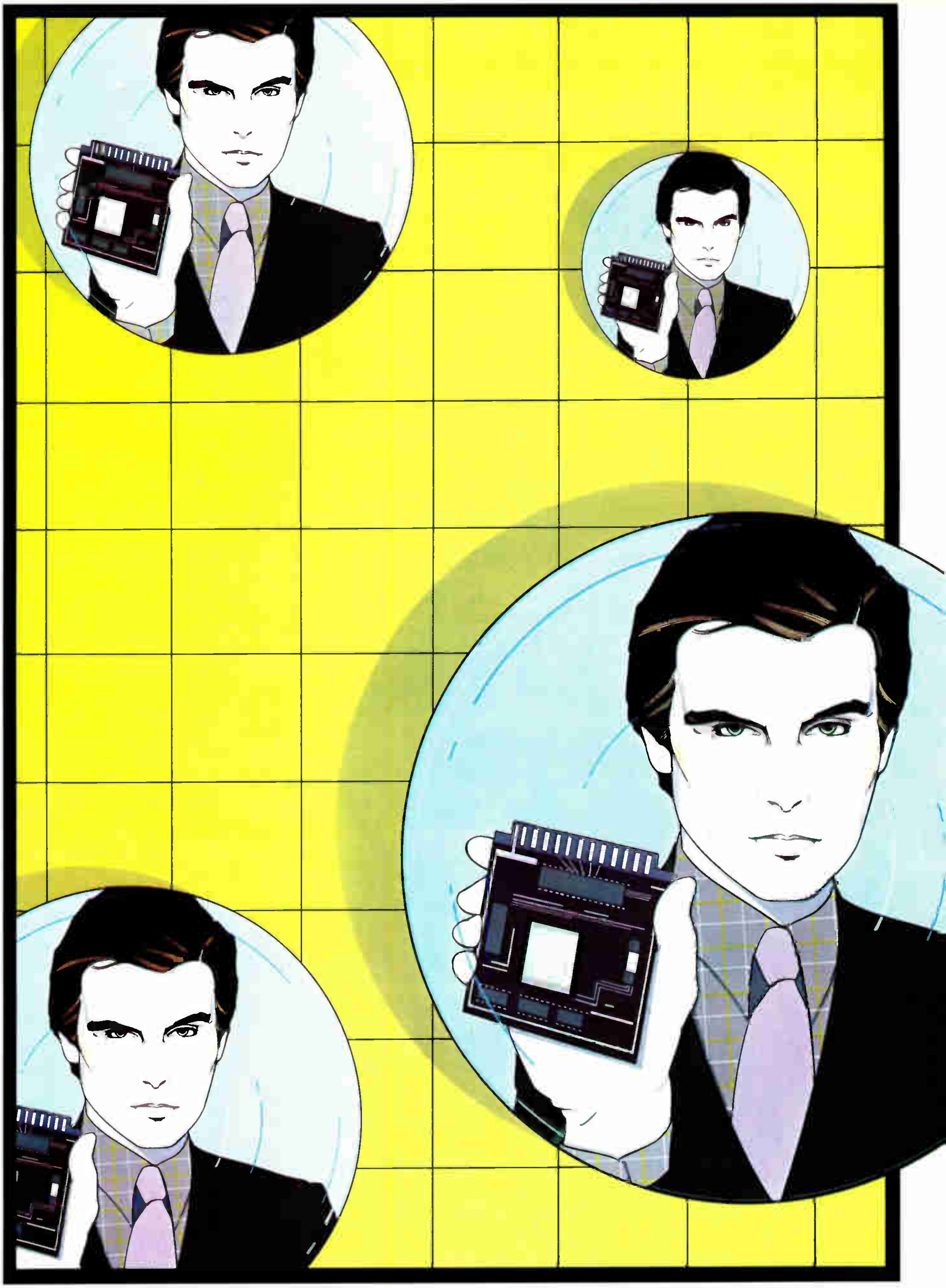


Million Bit Memory Kit

Intel delivers the first megabit bubble system and all the support you need to start designing today.

Step into the megabit bubble. You'll find an entirely new class of non-volatile storage—and vast new opportunities to exploit the microcomputer.

Bubble memory for microcomputers

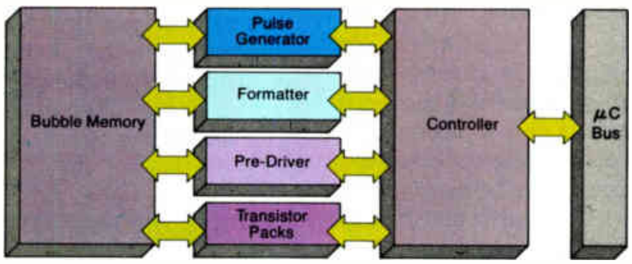
System designers have always been attracted to bubble memory for compact, low power, high reliability applications. Until now, though, bubble memories have been difficult to use and costly, since they require complex address, control and interface circuitry.

Today, Intel introduces a million bit bubble system perfectly matched in size and performance to the world of microcomputers. Intel's bubble memory gives you 128K bytes of low power read-write memory, plus all the system components you need for compatibility with advanced microcomputers like our 8-bit 8080, 8085 and 8088 and our 16-bit 8086.

Our system makes it simple

To simplify designing and manufacturing, Intel's bubble memory system consists of only seven components. All of them fit easily on a pc board as small as 4"x 4".

The heart of the system is our 7110 Magnetic Bubble Memory chip. It interfaces directly with our 7242 Formatter/Sense Amplifier, 7230 Current Pulse Generator, 7250 Coil Pre-Driver and two 7254 Quad Transistor Packs.



Intel® Bubble Memory System

The user interface, system timing and control functions are provided by our 7220 Controller, available Q1, 1980, or by our Controller Emulator Kit CPK-72, here today.

For systems exceeding a megabit, you can design with the same component family. Since one 7220 Controller will accommodate up to eight megabit chips and their support devices, larger system designs are simplified dramatically.

Bubble you can believe in

Intel's bubble memory means unparalleled data integrity. It's a rugged, solid state device. And it's completely non-volatile, so your data remains when the power goes off. No battery backup is necessary.

But the bubble system goes even further to ensure reliability. Intel's megabit chip works with the 7242 Formatter to give your system built-in error correction and detection. The 7110's ECC detects and corrects burst errors.

Start designing today

Intel's megabit bubble memory system is an ideal solution for microcomputer-based instrumentation, terminals, process controls and telecommunication systems. Everything you need to start designing is here today. Build your own system with our bubble memory prototyping kit. It gives you all the components for a one megabit system, plus complete documentation for easy designing. Or get a head start with our ready-to-use development board with complete system software. For a copy of our Bubble Memory Design Handbook, contact your local sales office or distributor. Or write Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call (408) 987-8080.

intel® delivers.

Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Arrow Electronics, Alliance, Almac/Stroum, Component Specialties, Cramer, Hamilton/Avnet, Harvey, Industrial Components, Pioneer, Wyle/Elmar, Wyle/Liberty, L.A. Varah and Zentronics.

Circle 21 on reader service card

The more you dema
the more you sh

Chances are, you'll find that the performance you need is already there.

At HP, our long experience in developing instruments for engineering and manufacturing has given us a real good idea of what's needed in computer systems for technical applications. That's why Hewlett-Packard's family of computer products can meet your needs so closely in the lab or on the factory floor.

Matching the computer to the job.

Take our 9800 Series Desktop computers. For single-station interactive computing, they're in a class by themselves. With up to 449K bytes of memory, enhanced BASIC, graphics capabilities, and a built-in keyboard and display, you get the power of a minicomputer in one complete, integrated package. And there's easy interfacing with HP instruments and peripherals for jobs like control and testing, statistical analysis, and even engineering design.

For more complex multi-processing tasks, the HP 1000 computer has the power and flexibility to meet your needs. You can choose from a broad range of computation power to process your data, from the low-cost M-Series to the high-speed floating point F-Series. All of the configurations use upward-compatible RTE operating systems, so you don't have to rewrite your programs when you change jobs or move up to another model. And if you need additional storage, you can expand the systems to two megabytes of main memory starting at only $18K/per megabyte.

The HP 1000 system also comes with a number of applications tools to minimize your programming costs. HP's new DATACAP/1000 software, for example, lets you design a real-time factory data collection system according to your shop floor needs. And to help you manage vast quantities of technical data, we developed our powerful IMAGE/1000 data base management system. Just a few simple keystrokes give you up-to-the-minute information on inventory levels or instrument check-out status. If you'd like a really clear picture of your information, HP's GRAPHICS/1000 will plot your data in a way you can understand.

nd from a computer, ould look at HP.

Communication made simple.

General purpose interface cards let you adapt the HP 1000 to a variety of tasks, including A/D conversion and multi-point communications. What's more, with the plug-in HP-IB (interface bus), you can process and control data from over 200 sophisticated measurement and testing instruments.

Talking to the computers is easy, too. The HP 1000 uses BASIC and FORTRAN as well as assembly and micro-code languages. And our powerful communications software, DS/1000, lets you hook HP 1000 computers together in any network configuration you want—across your plant or around the world.

A continuous growth plan.

HP's family of computer products is constantly growing to meet your scientific, engineering, and manufacturing needs. Whether it's instrumentation front ends, CRT terminals, plotters or digitizers, HP's compatible products let you add to your system at any time without writing new software. And of course, you get HP's full support, service, training and documentation.

Go ahead and ask your own computer some tough questions. Then ask ours and see the difference. For a hands-on demonstration of the HP 1000, just call your nearest HP sales office listed in the White Pages. Or for more information write Hewlett-Packard, Attn: Roger Ueltzen, Dept. 659, 11000 Wolfe Road, Cupertino, CA 95014.

Here are just a few of HP's range of products for manufacturers and engineers:

1. HP 9845 Desktop Computer.
2. HP 9825 Desktop Computer.
3. HP 1000 Model 45 Real-time System with HP 7906 Disc Drive and HP 2648A Graphics Terminal.

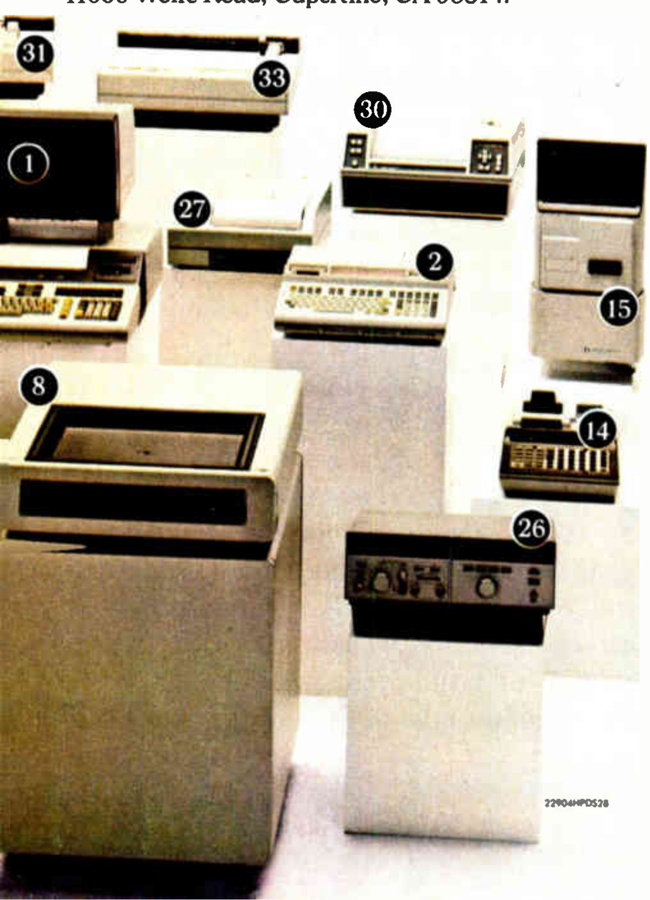
4-6. HP 1000 F-, E-, and M-Series Computers.

7. HP 2108 Board Computer.
8. HP 7925 Mass Storage Unit.
9. HP 2240 Measurement & Control Processor.
10. HP ATS Automatic Test System.
11. HP 12050 Fiber Optics.
12. HP-IB Link IEEE-488 Standard Interface.
13. HP 2621 CRT Terminal.
14. HP 3075 Data Capture Terminal.
15. HP 3077 Time Reporting Terminal.
16. HP 3455 Voltmeter.
17. HP 3495 Scanner.
18. HP 5328A Universal Counter.
19. HP 5342 Microwave Frequency Counter.
20. HP 436A Power Meter.
21. HP 4262 LCR Meter.
22. HP 8566A Spectrum Analyzer.
23. HP 8754A Network Analyzer.
24. HP 3325A Synthesizer/Function Generator.

25-6. HP 8660A & HP 8672A Synthesizer/Signal Generators.

27-8. HP 9876A & HP 2608A Printers.

29. HP 2635 Printer.
30. HP 7245A Thermal Plotter/Printer.
31. HP 7221A Plotter.
32. HP 7225A Graphics Plotter.
33. HP 9872A Programmable Graphics Plotter.
34. HP 9874A Digitizer.
35. HP keeps it coming.



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Facing the challenges of the 1980s

It has been a decade of upheaval, but it is only a prologue to more of the same. The 1970s will be remembered for the emergence of what might be termed one world of electronics, when the technology became, for better or worse, a global possession. They were also a time of challenges met and deferred, of economic highs and lows, of crowning achievements and noteworthy failures.

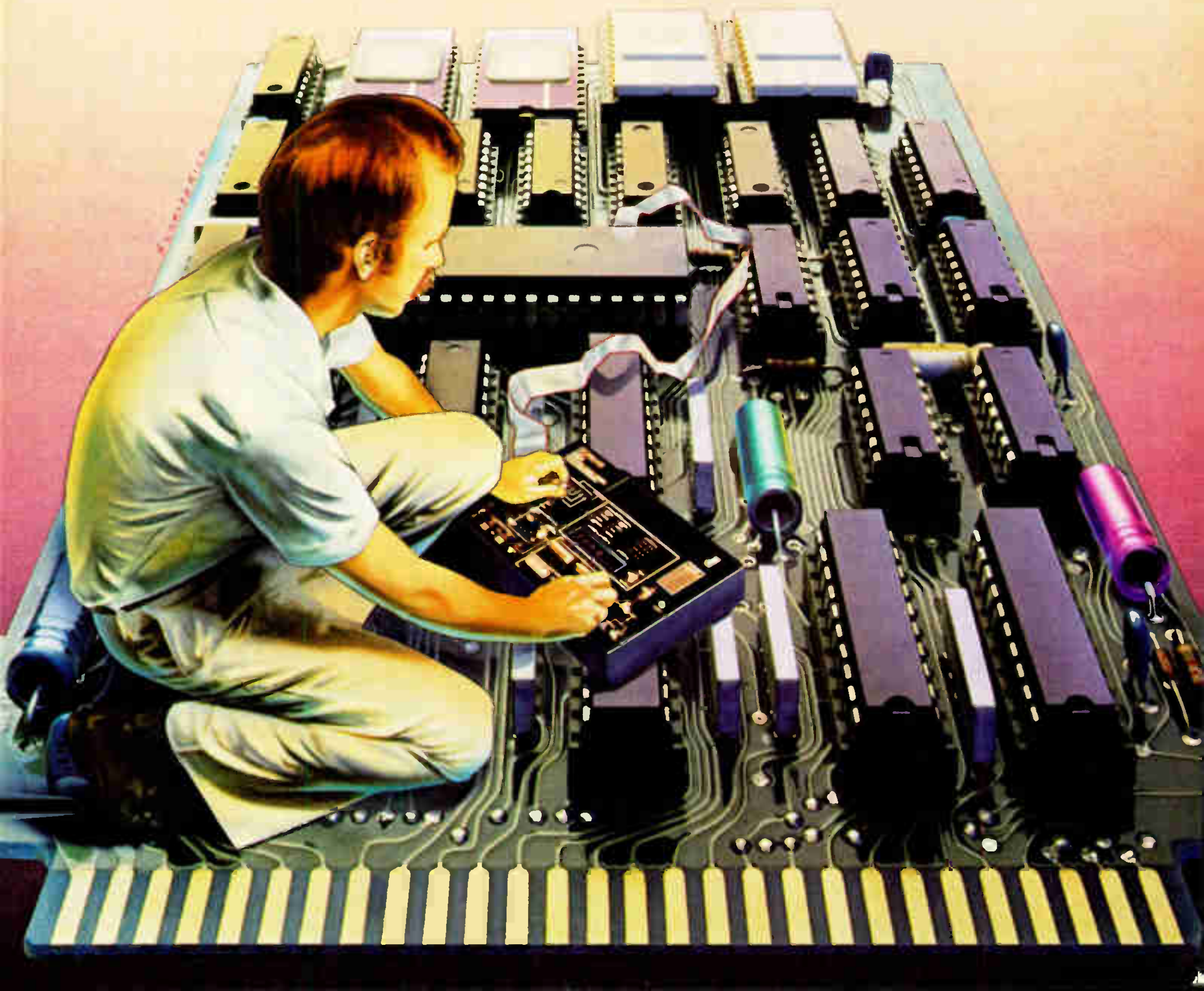
As it leaves the 1970s, the electronics community finds facing it serious problems engendered in part by profound changes in the structure of the marketplace. For not only has innovation been internationalized, but so has international competition—particularly from the Japanese. And there also has been increased foreign ownership of American electronics companies, particularly semiconductor makers. On the home front, the U. S. is facing falling productivity as well as energy problems.

Those are some of the challenges coming the way of the electronics industries in the next decade. Judged only from that viewpoint, the picture is a gloomy one. But fortunately there is another, broader view, one that also encompasses opportunity. The truth is that the 1980s will be a decade filled with opportunity, most of it springing from some of the challenges that loom as obstacles now. The reason is that in many cases electronics is part of the solution. Energy and productivity are just two examples. In the former, electronic instrumentation can become an integral part of energy management and control, even generation. In the latter, microprocessors alone have already markedly increased productivity in selected areas, and those devices are still in their infancy. Most of industry is just beginning to appreciate the enormous potential of robotics, even as the robots themselves become capable of handling more intricate and demanding work assignments.

Then there is very large-scale integration, a technology in which America still leads the world. Out of the ever-spiraling complexity of VLSI will come more and more applications from which new businesses, new markets, and new opportunities will arise.

Also consider the role of the Government and its influence on the design and procurement of electronic systems and devices. The past decade saw it wane almost to the point of disappearing, particularly when compared with the high-water marks reached in the 1950s. But now Government influence is being felt again—for example, the Department of Defense's challenge to the semiconductor industry to develop very high-speed integrated circuits, a challenge that could rank with the one that led to the first volume production of ICs for Minuteman missiles.

That program is one sign that the Government recognizes the importance of electronic technology and what it means to our future as a nation. Other governments have long seen the need to support technology and it seems that the U. S. is beginning to. In an increasingly competitive world, nurturing and encouragement will be necessary to maintain growth, produce innovations, and fulfill the bright promise of the 1980s.



Meetings

Winter Consumer Electronics Show, Electronic Industries Association, Convention Center, Hilton and Jockey Club Hotels, Las Vegas, Nev., Jan. 5–8.

Sixth Semiannual ATE Seminar and Exhibit and First Annual Test Instruments Conference, Benwill Publishing Corp. (1050 Commonwealth Ave., Boston, Mass. 02215), Convention Center, Pasadena, Calif., Jan. 7–10.

Export Administration Act of 1979, Law & Business Inc. (Harcourt Brace Jovanovich, 757 Third Ave., New York, N. Y. 10017), One World Trade Center, New York, Jan. 10–11, Mark Hopkins Hotel, San Francisco, Jan. 31–Feb. 1.

Second Design and Finishing of Printed Wiring and Hybrid Circuits Symposium, American Electroplaters' Society (1201 Louisiana Ave., Winter Park, Fla. 32789), San Francisco Hilton, Jan. 15–17.

TV Mex, the TV Microelectronics and Microprocessing Exhibition, and IDEA, the International Domestic Electrical Appliances Exhibition, Montbuild Ltd. (11 Manchester Sq., London W1M 5AB, England), National Exhibition Centre, Birmingham, England, Jan. 15–17.

VHSIC—A New Era in Electronics, American Institute of Aeronautics and Astronautics (Box 91295, Dept. VHSIC, Los Angeles, Calif. 90009), Hyatt Regency, Cambridge, Mass., Jan. 21–22.

Advanced Semiconductor Equipment Exposition, Associated Ad-Ventures Inc. (Suite V, 4546 El Camino Real, Los Altos, Calif. 94022), Convention Center, San Jose, Calif., Jan. 22–24.

Short courses

Computer Communications Networks, Jan. 15–18, Hyatt Hotel, Burlingame, Calif., and subsequently in other locales. Write to Integrated Computer Systems Inc., Box 5339, Santa Monica, Calif. 90405.

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The right kind of experience. In the toughest jobs in the most demanding environments. For more than a decade, Hybrid Systems has been building products that stand up to every challenge. Data converters. Thin film resistors.

We're proud of our record as a world leader in hybrid microelectronics technology, and we fight hard to protect it. Our expertise in hybrid integrated circuit converters, for example, is backed by the design and manufacture of hundreds of different modules incorporating proprietary thin film nichrome ladder networks for superior tracking and matching.

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Not all our products are for defense. But we design our commercial and industrial products the same way as the military ones. Send for our latest 120-page catalog. It presents many new data converters and other products — more new ways in which you can benefit from our experience.

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Sure Winners

Competitive systems start with Intel® static RAMs. Now you can choose a champion for any design.

High performance memory design is a fast track. The winners are those who match advanced components precisely with today's system requirements. When it comes to static memory, only one supplier has the broad selection of high speed, low power RAMs, and the delivery you need to bring your product to market ahead of the field.

Over 50 Purebred RAMs

From the beginning, Intel has been the leader in practical, producible MOS memory technology. First NMOS. Then high performance HMOS,* the high reliability technology that's produced more than 14 million fast static RAMs —as well as our industry standard 16-bit microcomputer, the 8086. Now HMOS II* is here, bringing you the same reliability and a new generation of even higher speed static RAMs.

Today, Intel gives designers the widest selection of 1K and 4K static RAMs in the industry. Over 50 different versions let you tailor speed, power, density and organization precisely to your system requirements.

Record breakers for high speed systems

Nowhere is the precision matching of memory components to function more important than in high speed cache, buffer, control store and main memory. At Intel, you'll find static RAMs to cover your full range of design goals.

*HMOS and HMOS II are patented processes of Intel Corporation.

SPEED (ns)	1K x 1	4K x 1	1K x 4
20	2115H/25H (20-35ns)		
40		2147H (35-55ns)	2149H* (45-55ns)
60	2115A/25A (45-70ns)	2147 (55-85ns)	2148H* (45-55ns)
80			2148 (55-85ns)
100			
200		2141 (120-250ns)	2114A (120-250ns)
300			

*Available Q1, 1980

For highest speed and low power, no bipolar can touch our HMOS II 2115H/25H 1K static RAMs. One version gives you record access times of 20ns; three others let you choose speed/power combinations to 35ns. For designs requiring speeds from 45-70ns, our 16-pin industry standard HMOS 2115A/25A series covers the spectrum. All of these 1Ks are pin-compatible replacements for 93415/25 bipolars, and all give you dramatically lower power, too.

In a 4Kx1 format, our HMOS 2147 is the industry standard for low power and speeds to 55ns. Today, designers requiring even higher performance will find a winner in our new HMOS II 2147H—with versions as fast as 35ns and standby power dissipation of only 30mA.

Finally, for special wide-word memories, including control store and bit slice designs, Intel's 1Kx4 bit 2148 is out in front. It gives you all the performance advantages of the HMOS 2147, plus the modularity that lets you save 75% on board space compared with 1K designs. And, you can expect even faster speeds in the future as we apply HMOS II to wide-word memory devices.

Pick the best performer for microcomputers

For years, microcomputer system designers have relied on Intel's 18-pin industry standard 2114 static RAM in 1Kx4 designs. Now we've used HMOS technology to improve performance with our new 2114A. It's a direct descendent of our 2114, but with a 30% smaller die size, 40% faster speeds, and 43% less power dissipation. The 2114A gives you performance equal to that of our 4Kx1 bit 2141, so you get optimum efficiency no matter what modularity you need—no matter how basic or how advanced your microcomputer application.

Intel gets you off and running now

We're delivering all of these fast static RAMs today. To order, or for more information, including our HMOS Reliability Report, RR18, contact your local Intel sales office or distributor. Or write Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

intel® delivers.

Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Arrow Electronics, Alliance, Almac/Stroum, Component Specialties, Cramer, Hamilton/Avnet, Harvey, Industrial Components, Pioneer, Wyle/Elmar, Wyle/Liberty, L.A. Varah and Zentronics.

Circle 29 on reader service card

BUY A LINEAR LSI TESTER WITH YOUR EYES WIDE OPEN AND YOU WON'T LOSE SLEEP LATER.

In linear LSI test systems, like anything else, you only get what you pay for. And if you don't look before you leap, that "entirely new approach" to linear LSI testing could turn out to be the very same old computerized tester hiding behind some new metal, complete with all of yesterday's bottlenecks.

With today's LSI devices, you need a sophisticated, accessible and powerful computer to execute the complex test algorithms.

What you need is the LTX Spacesaver LLSI Test System. It's a unique modular integration of hardware and software that's easy to use and easy to program. Our Spacesaver puts computer power where you need it. All with an eye towards speeding up payback by increasing throughput and yield.

Your test engineers can be just that, test engineers, and quickly program, debug and update job plans in a high level language that doesn't require a Computer Science degree to use or understand. They can mix forced or measured variables and obtain rational results without scaling. They can debug and edit online anytime without interruption of production testing. All at a quarter of the cost of competitive systems that may be nothing more than the same old tester hooked to a host computer that does nothing for your testing capability.

Best of all, the new LTX Spacesaver can handle all your testing requirements on everything from op amps to CODECs, as well as thick and monolithic thin film trimming, too.

So open your eyes and get a good night's sleep. Find out about the LTX Spacesaver LLSI Test System today. Call Bob Bazner at (617) 244-7800. LTX Corporation, 160 Charlemont Street, Newton Highlands, MA 02161.

LTX

THE LEGEND CONTINUES.

By continuing to exceed all expectations for versatility, reliability and economy, the Teletype* model 43 teleprinter family has earned a reputation that is tough to live up to.

However, the new tabletop buffered 43 bears that burden with ease. This remarkable terminal reduces transmission costs by reducing transmission time.

Information can be keyboarded off-line and stored in the 16K buffer for subsequent high speed transmission. And editing capabilities correct errors off-line before they can enter the system.

At the same time, the buffered 43 is just as reliable as any member of the 43 family. Backed by a nationwide service organization to make installation and maintenance simple and quick.

It's so affordable for most any application. And it's quiet and compact. More reasons why model 43 teleprinters show up to work in practically every kind of office environment.

Call or write for more about the entire line of model 43 teleprinters. Learn about the legend that continues to get better as it gets bigger. **THE TELETYPE MODEL 43 FAMILY.**

Teletype Corporation, 5555 Touhy Avenue, Dept. 3141-O, Skokie, IL 60077. Tel. (312) 982-2000.

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Circle 32 on reader service card

Electronics newsletter

Xerox tosses Ethernet into data ring . . .

Xerox Corp. has joined the rush to the gold-paved data-communications market of the 1980s—information teleprocessing—with Ethernet, **a digital packet-switching network that will be functioning by late 1980.** James Campbell, president of Xerox Business Systems in Dallas, points out that the coaxial network has no switching logic and is not controlled by a central computer—logic and control are in individual work stations. Therefore, failure at one point cannot bring down an entire system.

Information will be generated at a rate of 3 Mb/s using an asynchronous protocol. Packets are 500 characters, or 4,000 bits, long. The network will interface internally with individual work stations as well as remotely with other Ethernets or public networks (like Xerox's Xten) via a microprocessor-controlled gateway. Ethernet also will be able to communicate with non-Xerox terminals, such as the IBM 2780, and with data-processing systems and nonintelligent terminals.

. . . and goes head on against IBM 5520 and Wang system

First to use Ethernet will be Xerox's new 860 Information Processing System. It will compete with the new IBM 5520 shared-logic word-processing system [*Electronics*, Nov. 22, p. 92], which sells for about the same $15,000 for a base system but lacks data-processing capabilities. **But the 860 is aimed more directly at Wang Laboratories Inc.'s system 5, model 3,** which sells for $11,900 per work station.

The basic 860 consists of a controller with an Intel 8085 microprocessor; two single-sided floppy disks that store 300,000 characters each, expandable to more than 10 megabytes via Winchester technology; and a 96-kilobyte random-access memory, expandable to 128 kilobytes. Prerecorded system software disks accommodate a variety of applications—for example, the user will be able to write custom programs in Basic. Also included are a cathode-ray tube that displays 66 lines of 102 characters each, a keyboard, and a 35-character-per-second daisy-wheel printer.

GTE forms group to manage growth in voice, data

In a major organizational reshuffle designed to help it meet the telecommunications needs of businesses in the 1980s, General Telephone & Electronics Corp., Stamford, Conn., has formed a Communications Network Systems Group. The group will manage GTE's growth in the voice-communications market and establishment of a base in data communications. Initially it will oversee the expansion next year from 90 to 250 central offices for trunk lines, **in addition to the startup of a satellite packet-switching system with 30 earth stations operating by 1981.** The company also plans to incorporate short-haul (packet) radio in the switching network, and to increase ground transmission rates from 56 kb/s to 1.5 Mb/s. In 1980, GTE will add electronic mail facilities and network interfacing capabilities for terminals operating at speeds of 2.4 to 56 kb/s.

Oki to introduce C-MOS, n-MOS families in the U. S.

Although not affiliated with Japan's group of companies funded by the Ministry of International Trade and Industry, Oki Semiconductor is planning an aggressive assault on the U. S. market in complementary-MOS memories and microprocessors and n-MOS static random-access memories. The Santa Clara, Calif.–based division of Oki Electric Overseas Corp. will soon begin marketing in the U. S. three 4,096-bit static RAMs in C-MOS. These include: the 5104, with a 4-K-by-1-bit organization; the 5114, a 1-K-by-4-bit part that is a C-MOS version of the n-channel 2114L1; and the 5115, a 1-K-by-4-bit device with on-chip registers. Also planned for 1980 introduction are several 4-K static RAMs in n-MOS, among them the 1-K-by-4-bit 2114L and the 4-K-by-1-bit 2141. Oki also is beginning to offer samples of a 16,384-bit n-MOS static RAM, the 2-K-by-8-bit 2128, and plans to offer a compatible 2-K-by-8-bit electrically erasable programmable read-only memory, the 2716, that operates off a single 5-V power supply. Toward the end of the first quarter, the firm is also **planning to introduce a line of single-chip 4-bit C-MOS microprocessors.**

First Inmos RAMs to be 16-K statics

Confounding the experts, the first random-access memories from Inmos Corp. will not be dynamic. The British-government–financed semiconductor company, which has headquarters in Colorado Springs, Colo., expects to have masks in the second quarter of 1980 for a high-performance 16-K-by-1-bit static memory **"that will be elegantly designed and use dynamic circuit expertise,"** according to a company spokesman. A 64-K RAM will follow by about three months. Inmos also plans programmable read-only memories and an advanced microcomputer family and expects to have a half dozen wafer-fabrication lines and the beginnings of microcomputer production in three to five years.

Hughes wants to fly 24-channel domsat system

Hughes Aircraft Co. is asking approval to build and operate a U. S. domestic communications satellite system that would cost about $190 million for two 24-channel satellites, a ground spare, construction, and launches. Through its Hughes Communications Service subsidiary **the firm would compete with a number of domestic satellite links already in operation.** Approval by the Federal Communications Commission could arrive in "three to six months," according to Clay T. Whitehead, president of the subsidiary and director of the White House Office of Telecommunications Policy from 1970 to 1974.

TI adds capacity for p-MOS chips

Although n-channel MOS represents the mainstream of today's semiconductor device technology, the surging demand for lower-cost, lower-performance chips for consumer applications **is bringing renewed vigor to the older p-MOS approach.** In fact, Texas Instruments Inc. is so convinced of the trend that it is building a new p-MOS wafer-fabrication facility. The company's highly successful TMS 1000 4-bit microcomputer is fabricated in p-MOS, as are a variety of calculator chips and memory devices that are used in such products as TI's Speak & Spell electronic learning aid and the 99/4 home computer.

Addenda

Control Data Corp. of Minneapolis will shortly sign a licensing agreement with Licensintorg, the Soviet Union's foreign trading organization, **to make available to U. S. industries some 30 new energy technologies.** . . . TRW Electronics Inc. is organizing and staffing an Array Processor division in Sunnyvale, Calif. Its nucleus is a group spun off from ESL Inc., acquired in 1978, which made **high-speed digital array processors for number-crunching military and scientific uses.** . . . RCA Corp.'s Satcom 3 satellite, devoted to cable TV, is lost. **The $20 million geostationary bird disappeared after a course correction** and is the subject of a concentrated search, with even the Air Force helping.

DATEL-INTERSIL

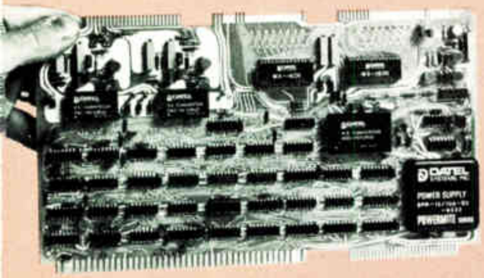
SBC-80 A/D-D/A Boards

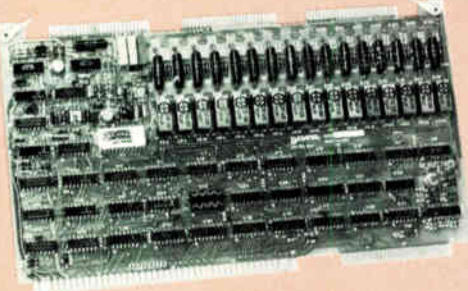
OURS $788

Exactly Replaces INTEL'S .... $1420 *

DATEL-INTERSIL SINETRAC SERIES

ST-711
ST-732





ST-711RLY8D
ST-711RLY16D

ST-711 .... $625 SINGLES
ST-732 .... $788 SINGLES

(NON-ISOLATED)

- Model ST-711: 32S/16D A/D Channels, no D/A Channels .... $625 (Singles)
- Model ST-732: 32S/16D A/D Channels, includes 2 D/A Channels plus current loop outputs............. $788 (Singles)
- Full mechanical, electrical, and pinout compatibility to Intel's SBC-711/732 Analog I/O Boards.
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- 12 bit binary conversion; 20 microsecond throughput period.

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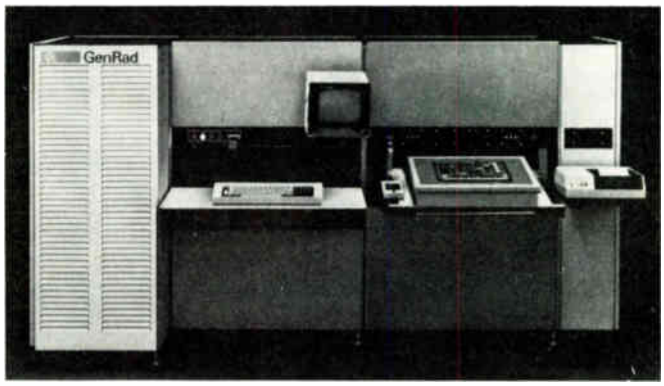
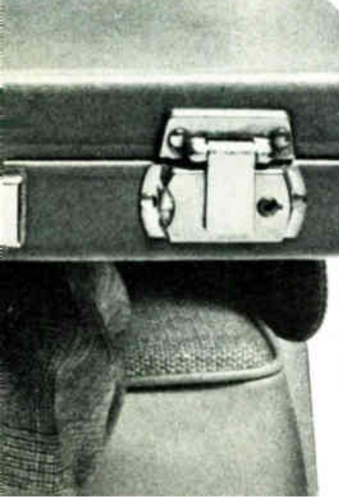


The GenRad 2270's powerful and flexible Automatic Test Generation software package automatically defines digital stimulus and expected responses for each IC.



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Circle 38 on reader service card

High-level language will run on all microprocessors

by Larry Waller, Los Angeles bureau manager

Block-structured PLMX gives freedom in design by letting users switch programs easily among types of processors

A new high-level language called PLMX is set to storm the barriers that impede the spread of programs from one microprocessor type to another. Developed in San Diego by the California division of Systems Consultants Inc., it is designed to run on any existing microprocessor and is ready to go onto the market.

"PLMX is a block-structured programming language that can handle any 8- or 16-bit microprocessor—it doesn't matter how many or what kind," says Jack Ingber, manager of product development. It was written over the past 2½ years for internal use at the $50-million-a-year SCI, till now largely identified with computer work related to big-ticket consulting and systems engineering for military, government, and industry clients.

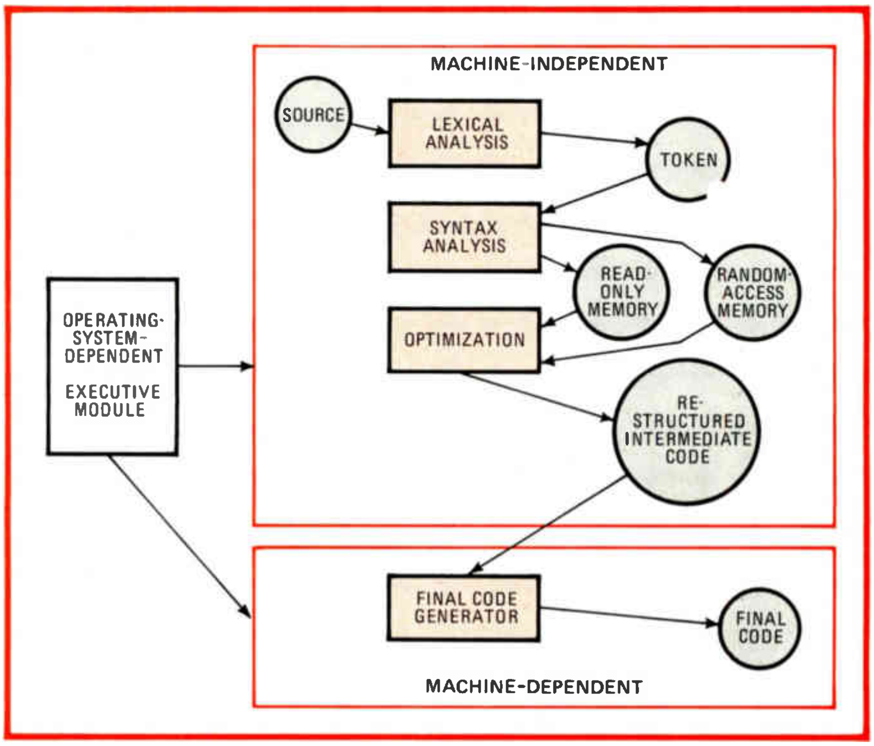
Freedom. The language gives more freedom in design choices because its programmers can use it to program any processor they choose. Since it is from an independent source, it also releases users from ties binding them to a high-level language compatible with a single vendor's microprocessor types.

The company claims that PLMX (see figure) is the first universal high-level language for microprocessor programming. Actually, the compiler for the language is not unlike most; after analyzing and optimizing input source code, it generates an intermediate code, which is translated into assembly language for the various microprocessors it serves.

While there are high-level languages that will execute on more than one microprocessor, the compilers necessary for the translation almost always come from a variety of sources. In contrast, SCI will provide all of the code generators and executive modules that allow the language to be compatible with a variety of operating systems.

Furthermore, the output of the PLMX compiler will always be assembly language, not machine code, making human optimization of critical program portions much easier. Such optimization is crucial for microprocessor system development to speed up execution and to reduce memory requirements, especially for applications that are based on read-only memory.

Compiler. The firm bills its software creation as "a true compiler, not an interpretive one such as Pascal in many of its current implementations." The main difference is that an interpreter itself needs considerable ROM to execute programs, which restricts development of ROM-based programs. A second drawback, says SCI, is that an interpreter executes instructions one at a time, which limits real-time work.



Three in one. Roughly 85% of the PLMX compiler is a machine-independent module producing an intermediate code. The final code is assembly language for any processor type.

Compiled code from PLMX, says SCI, can run up to 15 times faster because the output is optimized native machine code.

Syntax is identical to the PL/M language formulated by Intel Corp. for its processor family. "This makes the entire library of 8080 [PL/M] programs—by far the most extensive of any—available to be compiled by PLMX for non-8080 microprocessors. Intel users can go to other devices too," says Ingber.

The compiler can also accommodate other versions of this language: PLZ for the Z-80, MPL for the 6800, and within a year many others. Current versions can run on two microprocessor development systems: Tektronix' 8002A and any that uses CP/M, which supports 8080-based devices (including many hobbyist and process-control systems).

Stored on an 8-inch floppy disk, PLMX is termed "very easy to learn" by Ingber. Programmers familiar with PL/M "are off and running in less than an hour, others in a matter of days," says Frederick A. Stearns, who is the senior systems analyst chiefly responsible for the versatile new language.

Ingber says the single-disk price of $1,000 is about half the cost of PL/M, Pascal, and other software packages. Additional PLMX packages cost much less. Versions for the 9900 and 1802 will appear early in 1980, and the 16-bit packages will follow later in the year.

Solid state

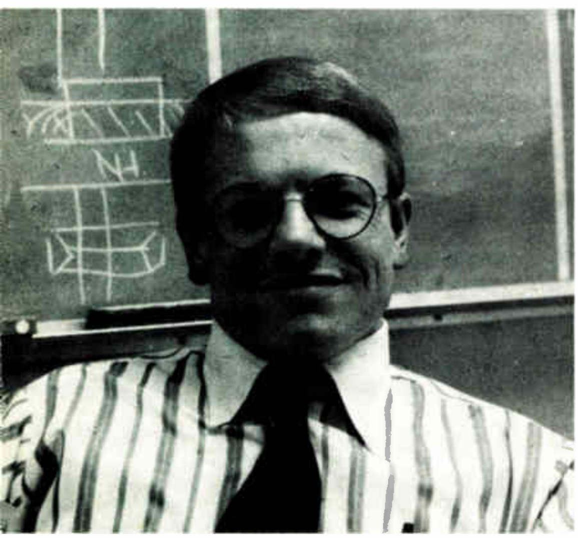
Yield problems that spelled doom for V-MOS did not involve grooves, says developer

As recently as the first quarter of this year, production of dense, fast V-groove MOS 4- and 16-K static random-access memories was rolling along smoothly at American Microsystems Inc., according to T. J. Rodgers, then the company's chief technologist for the process. The process used to make the parts "had positive margins," he says. Then, bang—in the second quarter there came "a deep, long, devastating yield bust that ran for six weeks."

Although Rodgers says that he worked out suitable remedies for the yield problems, by that time it was all over. The Santa Clara, Calif., firm was forced to scuttle V-MOS [*Electronics*, Oct. 11, p. 42], and he still respects that decision. His account, given at the International Electron Devices meeting early this month in Washington, D. C., is a *caveat* to any chip maker with limited resources and plans to pursue an offbeat production process.

Two problems. Although V-MOS had the usual lithography-induced defects on the production line, two other problems—diode pipes and edge shorts of the gate oxide—were the killers. Yet neither one is directly involved with the V-MOS transistors used to make the RAMs.

Diode pipes can occur when two silicon layers doped to the same polarity are separated by a thin layer of opposite polarity. When there is a vertical grain boundary present in the thin layer, the top layer is diffused more rapidly along this dislocation and shorts out to the bottom layer through a tiny conduit.



Understanding. V-MOS guru T. J. Rodgers says his former employer, AMI, had good reason to drop the memory technology.

This mechanism is usually restricted to bipolar devices, because MOS structures generally lack the cross sections that induce it. But AMI used special wafers that, when processed for V-MOS, turned out to have thin p-type layers sandwiched between two n-type levels.

Edge shorts. Even worse than the diode pipes were the shorts along the edges of the gate oxide. The static RAM cells consisted of two V-MOS storage transistors, two polysilicon loads, and two n-channel cell-select transistors. The shorts occurred in the n-channel devices—not the V-MOS transistors.

AMI protected the gate regions of those n-channel devices with a layer of silicon nitride as it performed a local oxidation around the rectangular gate regions using steam. The water vapor reacted with the nitride to form silicon dioxide; however, an undesirable byproduct was also produced: ammonia (NH_3).

The ammonia in turn reacted around the edges of the gate region to form a thin strip of nitride called a white ribbon. Subsequent growth of the thin gate oxides was inhibited where the parasitic nitride had formed, resulting in processing-induced pinholes that rendered the transistor—and hence the cell—useless. This phenomenon is known as the Kooi effect.

Sensitive. In the n-channel devices in the V-MOS memories, local oxidation was performed around the entire periphery of the gate regions. Oxidation of standard n-MOS transistors is usually confined to the two short sides of the rectangular gate regions. Thus, "the n-MOS devices in the V-MOS process were 100 to 1,000 times more sensitive to the Kooi effect," explains Rodgers.

Having the process buried was to Rodgers like climbing a mountain only to be denied a flag to plant there. So many technical problems had been solved before the final blow, he reports.

AMI had to invent a new substrate

that had to be doped with antimony, a rarely used impurity. And, of course, there was the actual etching of the V-groove wells and then the covering of them with reflow oxide—a problem on which AMI spent two years.

On your own. When working on such a different technology, "the entire learning curve belongs to you," says Rodgers. "You can't just go and steal somebody else's processing. It was a real battle all the time."

Although he has been courted by numerous semiconductor companies, Rodgers is going to form an MOS house of his own. He has defined seven top technical positions, filled five of them, and is preparing a business plan for a venture capital group. He expects to take a little over two years to start up his operation, but he will not be making V-MOS ICs.

"In the real world, V-MOS now has a stigma," he says, adding that if the technology "didn't have the financial crisis at the end, I'd still be doing it." In sum, "taking the company [AMI] as a black box, the decision [to drop the process] could not have been avoided." **-John G. Posa**

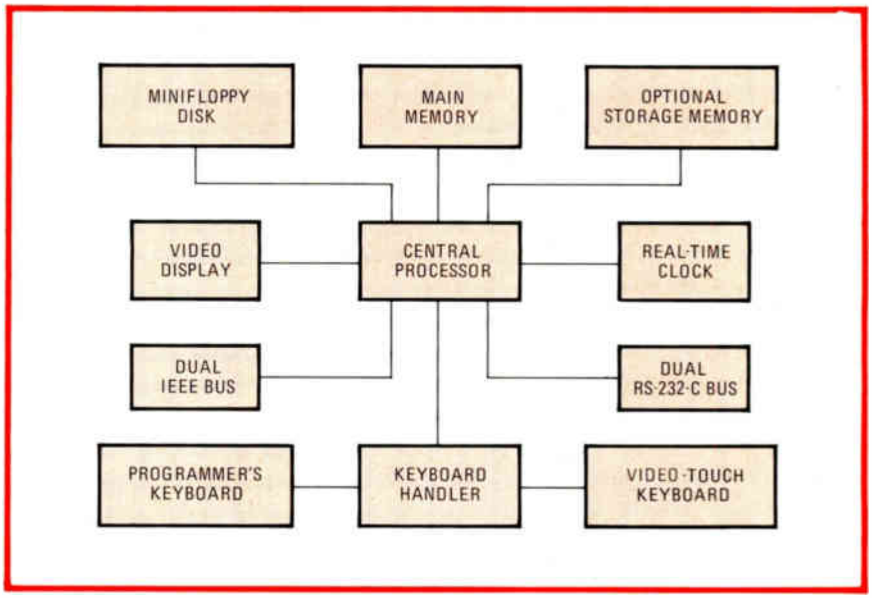
Instruments

Bus controller boasts high programmability

Instruments have been getting smarter for quite a while now, but their IQs are about to take a giant leap forward. With engineers becoming more familiar with software design, the microprocessor, already used to automate some measurement tasks, will be exploited more fully.

The form instruments are likely to take in the 1980s is evident in a forthcoming IEEE-488 bus controller, the model 1720 from John Fluke Manufacturing Co. Built around the 16-bit TMS 9900 microprocessor, the 1720 (see figure) clearly demonstrates how the capability of instruments is being expanded by applying software to the measurement task.

The controller has a user-software-configurable keyboard, as well as a detachable keyboard for programming. It also offers an optional solid-state disk adjunct, which hikes operating speed, and dual bus interfaces for more flexible use.



Doubling up. New Fluke IEEE-488 bus controller features two keyboards—one using its CRT—dual bus interfaces, and both minifloppy and optional solid-state program storage.

Predictor. That the shape of instruments to come will first be seen in a computer used to control the operation of instruments linked by the IEEE-488 bus is not surprising. After all, instruments are quickly becoming portable computers dedicated to measurement.

The dual keyboards most clearly underscore the shift to software. In the 1720, which should be available from the Mountlake Terrace, Wash., firm in the second or third quarter of 1980, they also emphasize a sharpening division between the tasks of engineers and technicians.

Magic keys. One keyboard is a detachable, 65-key unit for use by a bus system designer or programmer. Using 59 ASCII keys and the 6 editing command keys, an engineer can write in Basic test programs to be stored on floppy disks, thus forming a library of test routines. In operation, the programs on any disk can be put to use by a technician using the second software-configurable keyboard.

Basically, this second keyboard is the 1720's green-phosphor 5-by-9-inch cathode-ray tube. Overlaying the CRT is a transparent, touch-sensitive matrix that divides the screen into six rows of 10 ohmic contacts.

This configuration permits the "keys" for any operation to be determined completely in software. Menus of operational choices, for example, can be put on the screen and all a system user need do is touch the one he wants. For feedback to the operator, the program can direct the key to blink, sound a beeper, or provide both signals.

Optional memory. For increased operating speed, Fluke will offer an optional solid-state program memory that works like a fixed-head disk. It provides a transfer rate of 130 kilobytes per second, as opposed to the floppy disk's 31.5 kilobytes/s. Two boards, each containing 128 kilobytes of storage, can be added to a 1720A, and programs stored on floppy disk can be downloaded to this electronic disk for faster access.

The company's experience with IEEE-488 system design is visible in the fact that the 1720 offers dual bus interfaces. One may be used with slower instruments, whereas the other is used with faster ones, increasing overall throughput.

For calibration systems, the dual setup permits one interface to be dedicated to the unit under test. If that unit ties up the bus, the whole system does not go down. Two buses allow greater separation than the 20 meters to which a single-bus system without bus extenders is limited. -**Richard W. Comerford**

Medical

System to detect and treat cancer, using microwaves for both tasks

Joining two threads of cancer research, an experimental microwave system aims at both detecting and treating tumors. What's more, the heat that treats cancerous tissue may also help detect tumors so small they otherwise pass unremarked.

The dual-mode system from Microwave Associates Inc., Burlington, Mass., combines a radiometer for temperature measurement and a bipolar transistor oscillator for tissue heating, or hyperthermia. The radiometer has been tested successfully on breast cancer in human beings [*Electronics*, Dec. 6, p. 36]. Soon to come are tests on animals of the oscillator and its ability to enhance tumor detection.

Frequencies. The radiometer operates at 4.7 gigahertz, where there is little interference and relatively low attenuation of the microwaves passing through the body. Its 2-decibel noise figure may be crucial in detecting ultrasmall tumors.

The oscillator operates at 1.6 GHz, where the resonant heating that causes hyperthermia is optimal [*Electronics*, April 26, p. 88]. Both subunits' antennas are joined in a single assembly (see photograph).

Double duty. Microwave system uses one assembly for detecting and treating cancer. Small white rectangle is detector antenna; big one around it is treatment antenna.

Microwave detection of tumors is based on the greater energy that the slightly hotter tumors emit than the surrounding healthy tissue [*Electronics*, April 12, p. 85]. Hyperthermia, at a variety of radio frequencies, is showing promise as a well-controlled, nonsurgical technique for heating tumors to temperatures that destroy them while leaving healthy tissue unaffected.

Benefits. A dual-mode system, such as the unit devised by Microwave Associates, could check many patients rapidly without exposure to potentially harmful X radiation. It could also provide near-simultaneous treatment, since the present system's 25-watt output will raise tumor temperature the few degrees that can trigger remission.

Further, used with X-ray therapy, the radiometer already has monitored the temperature—and thus condition—of tumors, according to members of the team conducting the tests at Eastern Virginia Medical School at Norfolk General Hospital.

Most exciting to Microwave Associates' vice president Kenneth L. Carr is the possibility of combining hyperthermia with radiometry for finding very small tumors, whose temperature, though elevated, is still too low for detection without heating. He has no doubt it will work.

"Early in 1979, we hid a ferrite sphere in layers of dielectric material, simulating a tumor embedded in flesh," he says. "After a small amount of microwave heating, we were able to locate the 'tumor' to within $\pm 1/8$ inch and were able to resolve temperature differences as small as 0.1°C. The present radiometer is an improved design, which should be able to resolve differences as small as 0.05°C." (In the Norfolk tests, tumors were about a degree hotter than healthy tissue.)

Carr plans to develop a closed-loop hyperthermia system in which the radiometer would monitor tumor temperature and generate a feedback signal, varying oscillator output to maintain tumor temperature at the desired level. First, though, Microwave Associates is building another dual-mode system to test slightly different operating frequencies. -**James B. Brinton**

Industrial

Numerical controllers sport bubbles

As nonvolatile storage suited for dirty industrial environments, magnetic-bubble memories are making their way into computerized numerical controllers. Two U. S. CNC suppliers plan volume production early next year of bubble-based systems that can provide individual machining instructions for a wide variety of different production parts.

Optograms Inc., Oakland, N. J., will be using 92-kilobit bubble chips from Texas Instruments Inc. General Numerics Corp., Elk Grove Village, Ill., will be using 256-kb bubbles from Rockwell International Corp and Hitachi Ltd. The memories will store perhaps a week's worth of programs, probably read in all at once from permanent storage, such as the paper tape found in most numerical control setups.

Advantages. Unlike paper-tape CNC systems, bubble-based controllers offer easy program modification without the bulky battery backup required by dynamic semiconductor memories, points out Optograms president Geza von Voros. Unlike magnetic-tape cassettes and floppy disks that other controllers use, the bubble devices have no moving parts and so will be less subject to malfunctions that can occur in dirty factories, he adds.

Von Voros plans a January production startup of his company's

Dina-Mite system, with two to four 92-kb bubble parts on a single card. Exanded bubble capacity will come later.

An 8-bit Intel 8085 microprocessor controls the system, which also includes read-only memory for the operating system, as well as complex logic circuitry for control of as many as five axes of movement of the machine tool.

Prices. In its minimum configuration, the Dina-Mite will sell for $32,000 installed, with one unit necessary for each industrial machine being controlled. Comparable price for Optograms' controller with a cassette memory is $25,000. The company had sales of less than $2 million last year and is hoping the use of bubble technology will help propel demand to as high as 100 systems next year.

Also coming next year are two lines of CNC units from General Numerics. One of the lines, for industrial lathes, was designed and is being made in Elk Grove Village by one of GN's parents, Fujitsu Fanuc Ltd., a subsidiary of Japan's Fujitsu Ltd. Its other parent, Siemens AG of Germany, will make a line for machining centers and milling machine already introduced in Europe [*Electronics*, Aug. 2, p. 65] in its Cherry Hill, N. J., facility. Both controller types will be marketed under the General Numerics name.

The Fanuc line will offer up to half a megabit of bubble storage, and the Siemens line, up to a megabit, says Ted Smith, executive vice president of General Numerics. Sources within the company say the Fanuc units initially will use Hitachi bubble chips and Siemens will use Rockwell parts. Eventually, each may use bubble memories developed by the parent companies.

Intel 8086 microprocessors provide control in both General Numeric lines, designed independently by its parents. The 16-bit processor was chosen because its fast cycle time suited the complex, four-axis tasks the units will control, according to a GN spokesman.

Saving space. Smith says that a megabit of bubble storage for a numerical controller is equivalent to about 2,000 feet of punched paper tape. A program for a typical lathe part might take 30 to 40 ft of tape, he says, while a complex milling machine part might require a program of 200 ft. Thus storage of the varied programs that might be used on a single machine in a given week can take up a lot of room.

All solid-state memories are great space savers, but bubble chips are growing increasingly attractive as their nonvolatility is coupled with decreasing costs, Smith says. Other makers of CNC units such as Bendix, General Electric, and Allen-Bradley acknowledge that they are watching the technology closely, waiting for changes in factors like cost and availability. **-Wesley R. Iversen**

Chip makers urged to grow their own EEs

American integrated-circuit makers must begin training their own design and process engineers if they are to avoid a shortage of some 2,000 such specialists in 1985, says Jack Saddler, VHSIC program manager at Motorola Inc.'s Integrated Circuits division in Austin, Texas. He told a two-day conference on the U. S. military's very high-speed integrated-circuit program that, according to a Motorola estimate, there are 3,750 design and process engineers in the free world, with U. S. firms employing 56.5% of them. But only 180 new such specialists enter U. S. industry each year, he says.

Supporting Saddler at the Washington, D. C., conference was Kenneth A. Pickar, director of advanced technology for Signetics Inc., Sunnyvale, Calif. "We should train them, not raid them," he says, as well as work with many universities on training "and not restrict ourselves to those schools just in our immediate areas." Saddler speculates that a shortage could lead to "a free-agent draft system," with electrical engineers commanding multiyear contracts and six-digit salaries, just as many professional athletes do.

Trade

SIA, Japanese exchange blows

Stepping up its attack on Japan's semiconductor industry, the Semiconductor Industry Association is raising the specter of a Japanese-government–backed effort to weaken SIA member firms through artifically low U. S. prices. What's more, prices will be so low that American firms will not be able to raise the capital to remain competitive, the association predicts.

These dark clouds are on the horizon, unless the Federal government comes up with effective solutions, including legislation, according to a panel of executives from SIA member firms. They recently painted this gloomy picture in San Jose, Calif., before the House subcommittee on trade. However, their charges provided a strong reaction from Japanese sources (see "Japanese dispute SIA charges vigorously", p. 44).

Panel members at the hearing chaired by Rep. Charles A. Vanik (D., Ohio) included:

- George M. Scalise, vice president of administration, Advanced Micro Devices Inc., Sunnyvale, Calif.
- Charles Harwood, president, Signetics Corp., Sunnyvale.
- Andrew Procassini, vice president of worldwide semiconductor marketing, Fairchild Camera and Instrument Corp., Mountain View, Calif.
- Earl Rogers, president of Precision Monolithics Inc., Santa Clara, Calif.

The brunt of the SIA's testimony was aimed at a recently published International Trade Commission report [*Electronics*, Dec. 6, p. 41] that concluded that the U. S. semiconductor industry will maintain its leadership and profitability in the foreseeable future. On the contrary, "U. S. leadership in integrated circuits is threatened," says Scalise.

The basic trade problem, Scalise says, is the Japanese system of targeting an industry for growth and helping it with vast government financial resources and close relationships with private banks. This financial support "permits the Japanese firms to price their products with a view toward long-run market penetration strategies," he maintains, and to ignore free-market capital formation procedures applying to U. S. firms.

The evidence the SIA presented to the trade commission "strongly suggests that the Japanese semiconductor industry has plans to exploit its technological advances with a two-pronged strategy," adds Scalise. They are: "first, to capture a significant share of the U. S. market as a necessary proving ground for the most advanced products; secondly and more perniciously, to deny the U. S. semiconductor industry the cash flow required for the capital expansion and research and development which is essential to continue its technological leadership."

Pricing hit. Echoing recent charges that Japanese makers of 16-K random-access memories offer artificially low U. S. prices [*Electronics*, Oct. 25, p. 40, and Nov. 8, p. 40], Signetics' Harwood submits that "the only explanation for these erratic Japanese pricing decisions . . . is predatory market penetration—an all-out effort by the Japanese to buy a share of the U. S. semiconductor market and to weaken the U. S. industry.

"If forced to meet these prices, the U. S. firms will not be able to form capital in our free capital markets." According to Harwood, U. S. firms must maintain current earnings in order to expand capacity and finance R&D.

The panel's recommended remedies call upon the Government to take steps to resolve the artificial pricing effects that "will injure the U. S. industry" by diluting its capital-formation potential and learning-curve benefits; provide tax and other financial incentives to keep U. S. industry on a parity with the Japanese firms; negotiate with Japan for immediate implementation of tariff cuts already in the works; and consider legislation to tax U. S. operations of foreign-owned firms amounts that will offset the structural advantages they derive from foreign government target-industry programs. **-Bruce LeBoss**

Japanese dispute SIA charges vigorously

The Semiconductor Industry Association's attack on the Japanese is harsh indeed, but the defense across the Pacific is equally forceful. Company representatives and a Tokyo-based American expert on semiconductor markets take issue with almost all the points raised.

"We have no intention as a group to dominate price in the United States or anywhere else," says Taizo Nishimuro, manager of Toshiba Corp.'s international electronic components department. Noting that "competition with Japanese companies is sometimes keener than with foreign firms," he suggests Japan's capture of much of the U. S. market for 16-K dynamic random-access memories can be attributed to the failure of American producers to add capacity quickly enough.

Surprisingly, Keisuke Yawata, general manager of Nippon Electric Co.'s International Electronic Devices division, does admit that some Japanese semiconductor makers are charging 20% to 25% below market (and NEC's) U. S. prices on some products. Such companies make money but fail to recognize that fatter margins are necessary to fund the vast capital spending the future will require, he says. Adds Nishimuro, Toshiba believes in adhering to the market price and is not selling merchandise at a sacrifice.

Yawata argues that the way profit margins are listed in annual reports may mislead. They consolidate all product lines and so obscure the relatively low margins from semiconductor sales, he maintains.

Of the SIA's claim that Japanese firms can ignore free-market capital demands, Nishimuro says, "I have to agree to some extent." But he points out that the Japanese economy has been structured that way since before World War II. Structural differences like lower interest rates and easier availability of capital, he maintains, cannot legitimately be called unfair. Similarly, Yawata argues that government subsidies must be paid back. Toshiba is no big beneficiary of captive or government lending, says Nishimuro. It borrows from dozens of banks, with no more than 10% of its debt coming from any one and with at most 5% to 6% coming from government banks.

The American consultant dismisses the idea of a plot against the U. S. semiconductor industry. Pricing differences are the result of the differing structures of the economies, he says, such as a more relaxed view of borrowers' profitability taken by Japanese lenders.

Nor are the big five electronics companies lavishing as much money on semiconductor development as the SIA may think, he says. At one of these firms, for example, the head of semiconductor operations constantly battles with top management for capital and development funds, he maintains. **-Robert Neff, McGraw-Hill World News**

Packaging & production

Static electricity attracts attention

Static energy is generating a lot of excitement these days among system assemblers. Electrostatic discharges can cost them 10% or better of their daily production—and ever thinner layers of integrated-circuit oxide make punchthrough even more of a problem.

Giving added impetus to the campaign to control static discharges is a Department of Defense move to make contractors more responsible for antistatic standards. It is a campaign bound to succeed, maintains Stephen Halperin, vice president of Analytical Chemical Laboratories Inc., Elk Grove Village, Ill. "Static is not like the weather: there is a cure," he says.

Testing. Halperin's firm is one of a trio that have come up with an electrostatic discharge simulator test systems or assemblies. The instru-

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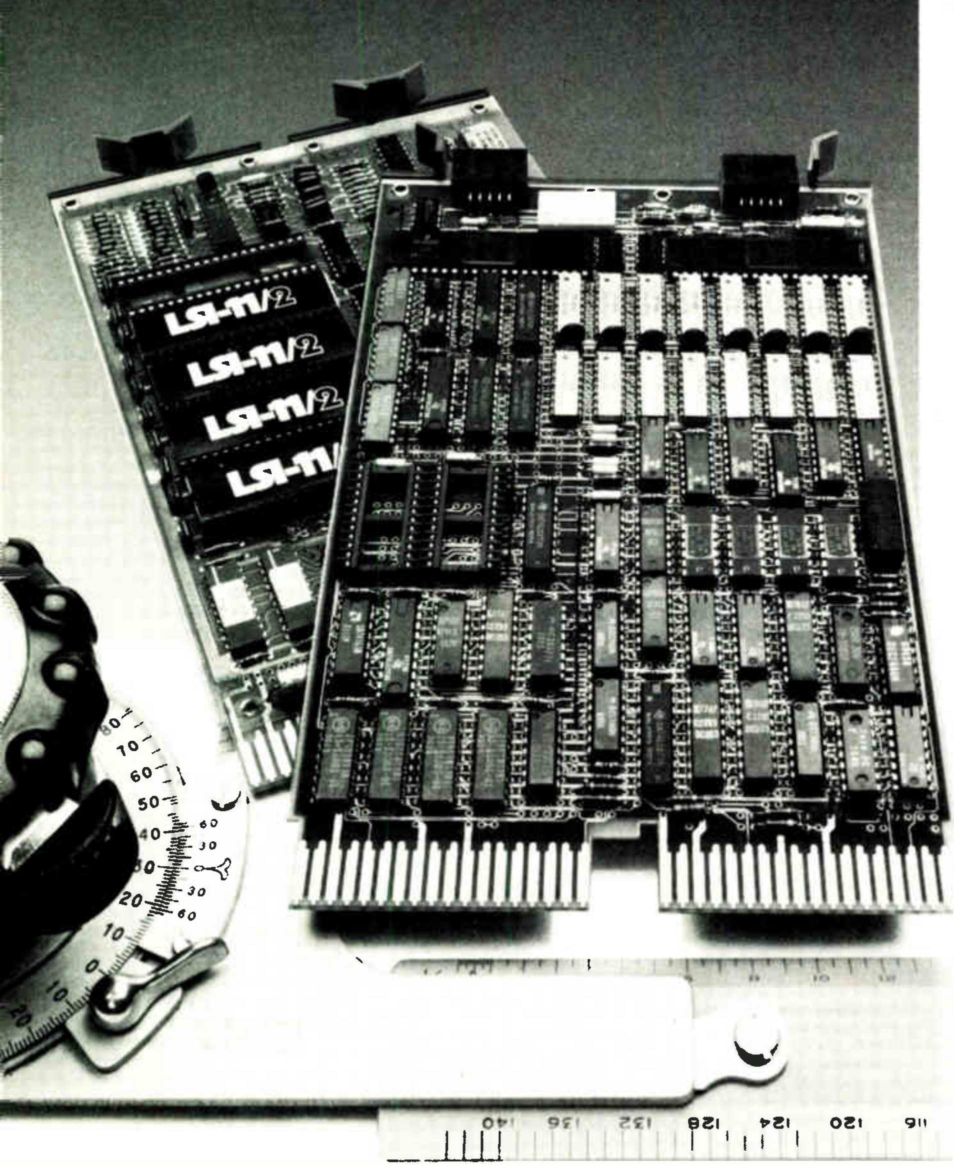

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Circle 45 on reader service card

News briefs

National, Zilog settle dispute on trade secrets
National Semiconductor Corp., Santa Clara, Calif., agreed to drop its suit charging Zilog Inc. and six former National employees with misappropriation of trade secrets. National, which filed the suit last May, now says that no member of Zilog's management induced the former employees to divulge trade information. Also, a third-party arbiter found that Zilog did not use any proprietary information from National in the development of the Cupertino, Calif., firm's products.

Mostek stands alone—sort of
A corporate realignment of United Technologies Corp.'s electronics operations leaves recently acquired Mostek Corp. with its own identity. With L. J. Sevin continuing as chairman and chief executive officer, Mostek will be one of four subunits of the new Electronics Group, but will function as a stand-alone subsidiary. The other three (confusingly called groups, also) are Controls, Automotive, and Essex—the latter incorporating the Essex Magnet, Wire, and Insulation division.

RCA bows out of VHSIC competition
Although Government funds seem assured for the Pentagon's very high-speed integrated-circuit research and development program, RCA Corp.'s Government Systems division, Cherry Hill, N. J., is dropping out of the competition to choose companies for the Phase Zero studies. RCA top management decided "we have to begin making profits," said James E. Saultz, manager of its VHSIC program in a conversation at a seminar on the program in Washington, D. C., earlier this month. The withdrawal from the planned six-year $200 million program to develop very fast ICs for military systems leaves RCA's proposed prime system contractor, Martin Marietta Corp., out in the cold for the Phase Zero awards, expected within a month.

ment originated in Honeywell Inc.'s Defense Systems division in Minneapolis, where assembly components and test equipment were shorting out and stopping production, says Fred Mykkanen, component applications engineer there.

Shooting for a failure rate due to static of under 1%, Honeywell conducts regular static studies at its plants. The problems IC users face may be garnered from a study conducted for the Naval Ship Engineering Center by Reliability Sciences Inc. of Arlington, Va.

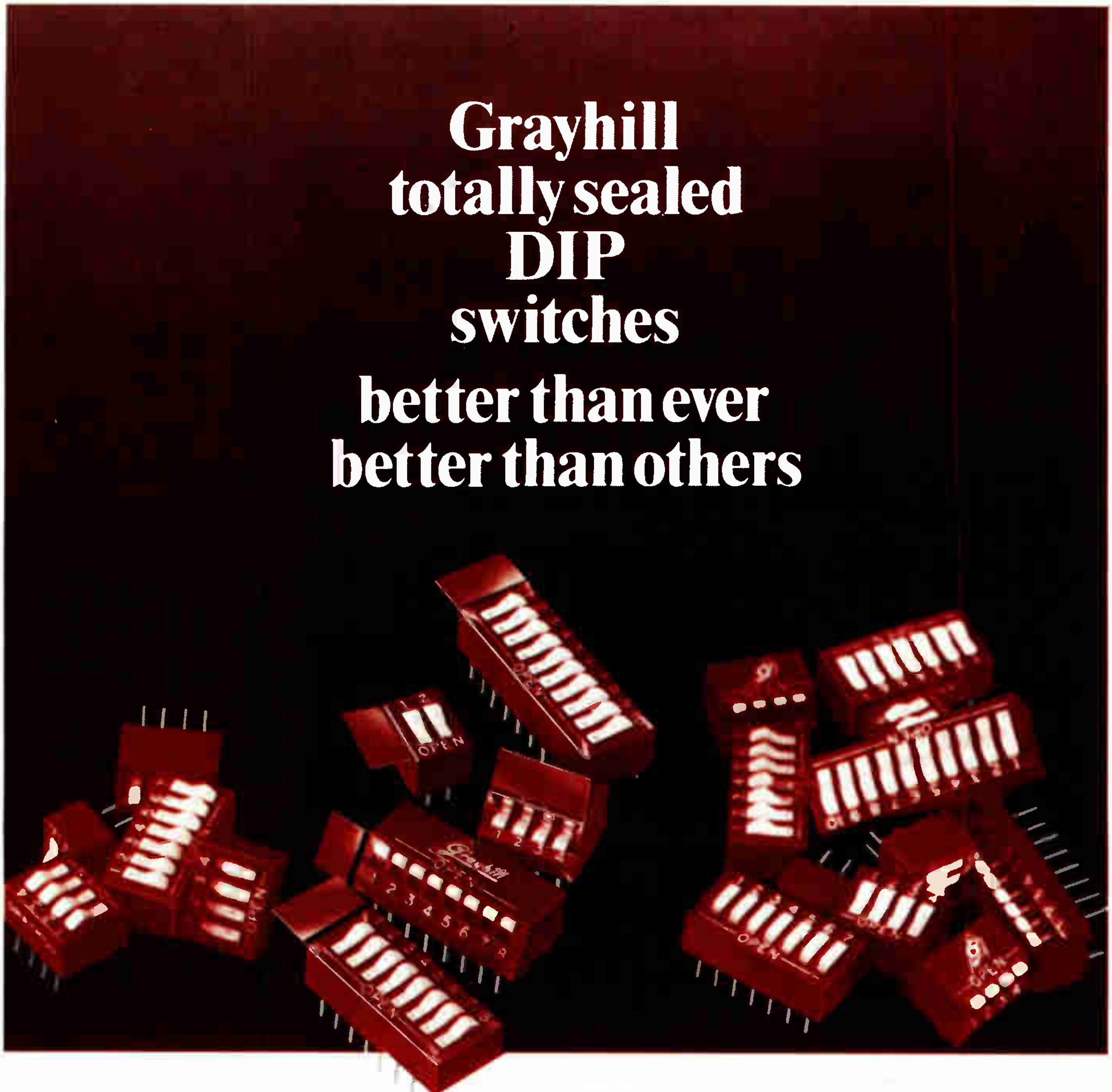
Susceptibility. The study found that susceptibility to destruction by static charges varies widely. The problem becomes even more crucial when components of varying susceptibility are assembled into systems.

So it is that the DOD is proposing a 1980 revision to the military standards for electronic systems and components. The revision would require manufacturers to monitor static levels in production plants and to substantiate the level of static control maintained at assembly lines.

The proof of the pudding is the failure rate of the electronic assemblies, and it is here that the model 900 electrostatic discharge simulator comes in. It performs a destructive test by simulating the effect of static discharge caused by human contact, says Stanley Weitz, president of Electro-Tech System Inc., Glenside, Pa.

Honeywell and Electro-Tech worked with Halperin to refine the breadboard design, and Analytical Chemical Laboratories will market the 900 beginning next month, as part of its line of static-measurement tools for industrial environments. The operator can vary voltage applied through the typewriter-sized instrument up to 15 kilovolts. A built-in voltmeter measures the discharge through the unit under test. However the simulator does not come cheap; it is slated to go for $2,995.

-Larry Marion



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Washington newsletter

New FCC battle: open competition for world traffic . . .

A major new action to open the $500 million U. S. market for international data communications to competition is beginning at the Federal Communications Commission. The FCC Common Carrier Bureau, after a 10-year battle that opened the domestic telecommunications market to competitors of American Telephone & Telegraph Co., **has moved quickly to let AT&T, Western Union Telegraph Co., and others into the international record carrier market. This nonvoice market is** now dominated by ITT World Communications, RCA Global Communications, TRT Telecommunications Corp. (which deals mostly with South America), and Western Union International (which is owned by Xerox Corp. and is not related to the U. S. carrier).

At the same time, the international record carriers would be permitted to use satellites and land lines to serve 21 U. S. cities directly with international data traffic—as well as audio and video signals from which they are now barred—in addition to the five coastal "gateway" cities to which they have been restricted since the days of transoceanic cables. AT&T and other record carriers historically have been restricted to voice when transmitting internationally.

. . . could be spur to digital market

"This proceeding is not over yet, since there are sure to be legal and other challenges," says one FCC staff member, citing chairman Charles D. Ferris's observation that **the proposal will "dramatically change 40 years of history in the international record carrier business."** Nevertheless, telecommunications equipment suppliers—including makers of computers, terminals, satellite antennas, and other peripherals—expect the eventual result will break open the tightly controlled international data market and prove a major spur to sales. A Common Carrier Bureau internal study contends that the four dominant international record carriers earn excessive rates of return ranging from 35% to 60% of their rate base, compared with 10% for domestic carriers. The bureau wants the FCC to let AT&T and others compete in the transmission of international digital, facsimile, and Telex data via cable and satellite to bring prices down.

Computer trade gains, but consumer buys of TV, radio slip

The good news for makers of computers and related equipment is that their third quarter exports hit $1.35 billion, a 26% gain on last year. Other business equipment exports rose nearly 21% in the quarter to $289 million, paced by soaring shipments of word processors and automatic typewriters, up 137% to $36.7 million. The gains put 1979 export totals for the first three quarters at $2.87 billion, **nearly equal the $2.86 billion total for all of 1978.** The nine-month totals pushed the industry's positive trade balance to $1.02 billion, or more than 36% ahead of the 1978 level, says the Computer and Business Equipment Manufacturers Association.

On the domestic front, the Commerce Department's bad news for home entertainment electronics makers is that 1980 will be marked by retailers and wholesalers maintaining "lean inventories" in anticipation of cutbacks in consumer shopping trips as the energy market tightens. Sales dollar volume may climb by 10% next year, equivalent to this year's percentage gain, but not enough to counter inflation. As the same time, the Electronic Industries Association reports that November sales of color TV receivers dropped for the fourth consecutive month to 888,000 units, off 10.3% from last year, pushing 11-month totals down by 3.4% to 8.8 million units.

Total radio sales also declined 10% for the month to 2.9 million, producing an 11-month drop of 12% to 41.6 million compared with 1978.

Forecasts show mixed bag for electronics sales

New Commerce Department and industry data presents a mixed bag for key segments of the electronics industries, **indicating further gains in 1980 for aircraft, missile and spacecraft builders, and computer makers**—but distinct uncertainties for the home entertainment market. This year's capital investment by aircraft and missile and spacecraft manufacturers will top $5 billion, up 41% from 1978. Planned outlays by the electrical machinery industry, which includes electronics but not utilities, will surpass $5 billion this year, up 27% from a year ago, with plant and equipment investment plans totaling $1.1 billion in the first 1980 quarter, a 16% rise from 1979.

Closer ties urged for VHSIC subs and military primes . . .

U. S. integrated-circuit makers unaccustomed to dealing with the military but who lead the way in semiconductor technology are going to have to work out long-term business agreements with the military prime contractors who are their customers. That will have to be done **if the Pentagon's very high-speed integrated-circuit** (VHSIC) **program is to get beyond the research and development stage,** says National Semiconductor Corp.'s Roy J. Thiels. His call for a new cooperative program came at a two-day December seminar on VHSIC sponsored by the American Institute of Aeronautics and Astronautics and the Technology Transfer Society in Washington. The triservice VHSIC program [*Electronics*, Sept. 4, 1978, p. 81] finally won congressional approval for $30 million in fiscal 1980 funds to begin its $200 million six-year effort.

Specifics cited by Thiels for VHSIC success drew general agreement from executives of other IC houses and military prime contractors among the 159 conference registrants. The Santa Clara, Calif., company's director of very large-scale integration says long-term agreements that could run to five years should: guarantee VHSIC production profit levels of 5% to 10%; not disrupt an IC maker's high-volume output for nonmilitary markets; and include documentation that semiconductor and systems houses are operating under the same rules for circuit design, layout, mask making, and chip size, stressing computer-aided design and eliminating customization wherever possible.

. . . but CAD bank for custom chips is called premature

Motorola Inc.'s Jack Saddler believes the success of the VHSIC program would be enhanced by use of a telecommunications network—like the long-established Darpanet of the Defense Advanced Research Projects Agency—to give the prime contractors for weapons systems access to a national computer-aided–design data bank of custom chips for their use. National's Thiels and others surveyed at the VHSIC meeting suggested the Saddler proposal was premature in view of the high degree of competition within the integrated-circuit community. Saddler, manager of Motorola's VHSIC program, acknowledged that such an intra-industry technology-exchange program **might make the VHSIC effort resemble the government-directed program in very large-scale integration in Japan and elsewhere** but added, "Maybe we could use a little of that." Japan's VLSI investment is $225 million vs the Defense Department's $200 million, West Germany's $300 million, and France's $200 million.

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RCA crosspoint switches are available in three types. The CD22100, a device that combines a 4 to 16 decoder with a 4 × 4 array of crosspoints.

The CD22101 which combines a 4 to 16 decoder with a 4 × 4 × 2 array of crosspoints. And the CD22102 version which has a different input logic configuration.

All three devices feature low on-resistance, built-in control latches, 10 MHz switch bandwidths.

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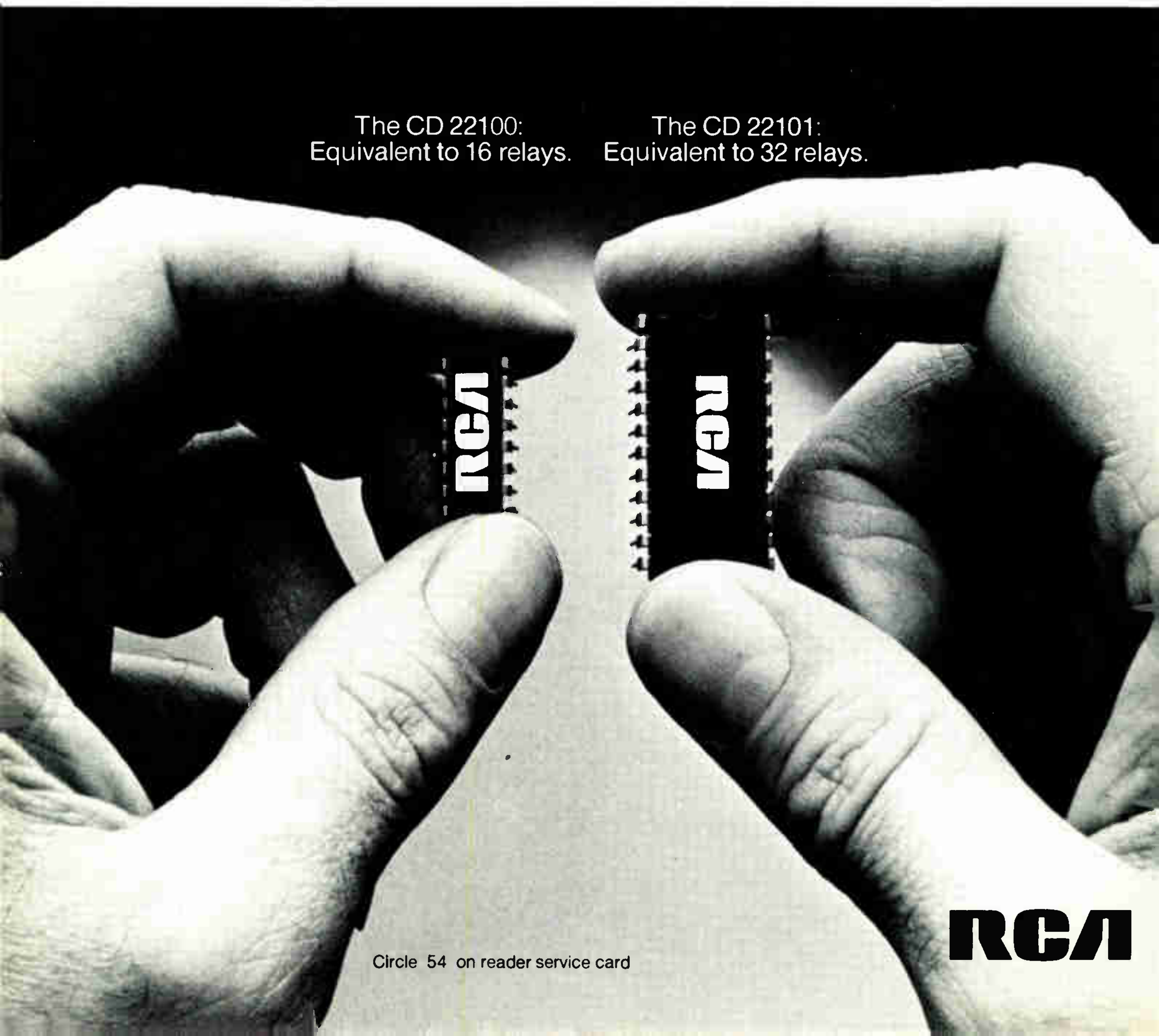
For further information, contact your local RCA Solid State Distributor.

Or RCA Solid State headquarters in Somerville, N.J. Brussels, Belgium. Tokyo, Japan.



Calculator speaks to Japanese users

A talking calculator developed by Sharp Corp. will go on sale in Japan in early January for approximately $250. A built-in speech synthesizer vocalizes the number or function of each key touched, the result after pressing the equals sign, and a recap of up to 100 steps of a calculation, contained in a playback memory. During keying, individual digits are vocalized, but to hear the result or the playback of a previous calculation, **the operator can select either individual digits or overall numbers.** Synthesis is performed by a fast n-MOS 4-bit microcomputer. The 60 words the calculator can vocalize are stored in a 6-kilobyte on-board read-only memory in the form of a pulse-code-modulated signal compressed to about one fiftieth of its normal number of bits. Part of the synthesis control is performed by a p-MOS 4-bit microcomputer, also with a 6-kilobyte ROM, that performs calculator functions as well. A single 16-K dynamic random-access memory external to the microcomputer provides the 100-step playback memory. Designed for business use, the CS-6500 calculator also features a 16-digit fluorescent display.

Marconi launches virtual instrument at Brighton ATE show

Add a new concept to the language of automatic test equipment—the virtual instrument. The concept was conceived by Marconi Space and Defence Systems Ltd. in Hillend, Dunfermline, Scotland, which has embodied it in a universal functional board tester called the Graduate. Introduced at Automatic Testing '79 in Brighton, England, Dec. 11–13, **the highly modular desk-sized system will eventually provide digital and analog functional testing from dc to microwave** but is initially offered with a low-frequency testing capability only.

In operation, the cathode-ray-tube display presents the user with a mimic front panel of any needed instrument. This panel allows him to select instrument functions and set levels for any test. It also indicates where to plug the needed power supplies and instrument function, and switching and other modules into bus-wired shelving. The approach, which uses stripped-down, single-function instrument modules, permits a limitless variety of test configurations, cuts costs by eliminating huge functional redundancies when standard instruments are used, and allows for technology updates, Marconi says. To make the interactive system work, the company uses a powerful 24-bit-slice processor with a random-access memory, built with 16-K dynamic chips, expandable from 64-K words to 256-K words of 24 bits each.

Plessey cuts bubble components, concentrates on systems

Plessey Microsystems Ltd. in Towcester, Northants., will not be committing to volume manufacture of bubble memory components and will cease all such manufacturing by mid-1980 after present commitments have been met. **The firm, however, will pursue its board systems activity in both the custom and standard markets.** It recently introduced a Multibus-compatible 1-megabit board [*Electronics*, Sept. 13, p. 75] and has demonstrated a capability in custom bubble work with a memory for a portable billing system. The company will also be looking to sell off its technology, which allows very thin packaging techniques, to other manufacturers. The move is part of a general pruning, which has seen the demise of the company's holographic memory [*Electronics*, Aug. 16, p. 67], in order to develop as a systems company.

International newsletter

Israel enters microcomputer market

Silma Ltd. of Kibbutz Kfar Masaryk says it has developed Israel's first microcomputer—and the firm claims it is much cheaper than others now on the market. Geared for businesses that have not previously thought of buying or using a computer, the 8-bit DOK-100 will cost between $10,000 and $11,000 and will be available in February. It includes 52 kilobytes of random-access memory, 4 kilobytes of programmable read-only memory or erasable PROM, and half-megabyte dual floppy-disk drives. For data entry, the DOK-100 has a 24-line cathode-ray-tube console with an alphanumeric keyboard. By February, the firm hopes to up the capacity of its mass storage to 1 megabyte per drive using double-density disks. **It also hopes to configure the machine to be compatible with IBM equipment so that it can function as a data-entry station.** Data-entry software is ready now, and a comprehensive software package is in the works.

Japan begins trial of first digital phone network nodes . . .

Nippon Telegraph and Telephone Public Corp. has begun the field trial of a digital exchange and digital terminals, which together constitute a digital network node, at its Karagasaki office in Tokyo. The present plan calls for the system, the first of its kind in Japan, to be placed in service at the end of 1980. Designed for switching telephone signals encoded in standard 64-kb/s pulse-code-modulation format, **it is capable of handling 50,000 lines, about five times as many as present large electronic exchanges.**

NTT's toll network has many 24-channel, 1.5-Mb/s short-haul digital transmission systems. Recently, long-haul digital lines operating at 400 Mb/s and using repeaters have been introduced. These will enable the newly developed digital exchange and terminals to be coupled with digital facilities to form a digital toll network. A digital local exchange, under development, will extend the digital path toward subscribers.

. . . and Canada gets first industrial fiber cable

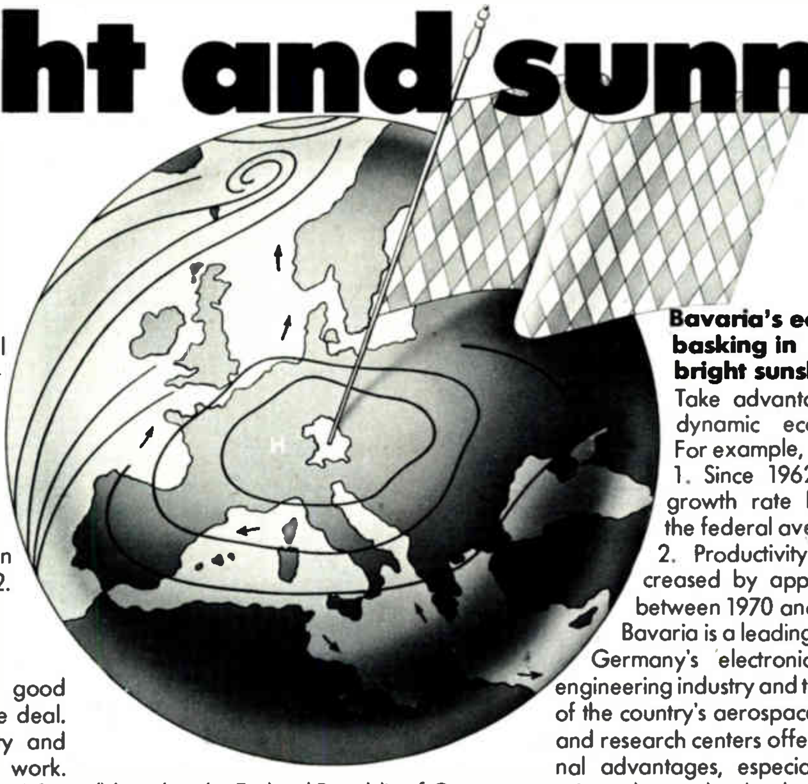
The first fiber-optic data link at General Motors of Canada Ltd. is now connecting the parts department's System 3 computer to the main computer in the data center at the firm's Oshawa location. **It is also the first of its kind for any GM unit** and the first use of optical fiber in the Canadian manufacturing industry. The link connects two 9.6-kb/s synchronous RS-232-C fiber-optic modems with 350 meters of graded-index duplex fiber cable. The hookup is now being tested for reliability; the results will provide the basis for evaluating future fiber-optic applications at GM.

Thomson readying versions of long-range sea-surveillance radar

Thomson-CSF is well along with three follow-on versions of its long-range maritime-surveillance radar, Iguane, although first production units will not start coming out of the assembly shops until mid-1980. The basic radar was developed by the company's Avionic Equipment division in Malakoff, outside of Paris, for the aging Alizé sea-patrol aircraft being refurbished by the French navy. One version of it, intended for new-generation Atlantic long-range surveillance aircraft, adds identification friend or foe and target tracking. A second, designated Varan, for patrol craft like the Mystère 20H, offers **optional circuitry that enables it to spot oil slicks.** The third, called Agrion, for missile-carrying helicopters, can switch from the search mode to guidance of an all-weather air-to-surface missile. Prototypes of all three are slated for tests in 1980.

Weather forecast outlook for your investments in

Bavaria: bright and sunny



General climatic conditions
In every respect Bavaria offers an ideal climate for business initiatives. The political and economic stability which this West German state has enjoyed for many decades helps to safeguard your capital investments. The profound confidence placed in Bavaria's economic and political development is reflected in the high level of foreign investments: DM 3.7 billion since 1962.

No dark clouds over the labor market
Bavaria's well-trained workers are good partners who will give you a square deal. They are known for their reliability and loyalty to the firms in which they work. Statistics show that strikes are few and far between. The large number of qualified young people coming to work in Bavaria shows that the state is a magnet for highly skilled personnel.

Infrastructure helps to generate a favorable investment climate
Bavaria's infrastructure meets the exacting requirements of a modern industrial state. (Note that the Federal Republic of Germany has the most extensive network of autobahns or superhighways in Europe.) The international airports in Munich and Nuremberg and many strategically located airfields throughout the state link Bavaria to Europe and the world. The sources of available energy range from natural gas to nuclear power. Industrial sites with utility connections are laid out in all parts of the state.

Bavaria's economy basking in bright sunshine
Take advantage of Bavaria's dynamic economic growth. For example,
1. Since 1962 Bavaria's GNP growth rate has been above the federal average.
2. Productivity in industry increased by approx. 50 per cent between 1970 and 1978.
Bavaria is a leading location for West Germany's electronics and electrical engineering industry and the principal center of the country's aerospace industry. Science and research centers offer valuable locational advantages, especially to companies using advanced technologies.

Fruitful showers – of public funds to promote sound investment projects
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Circle 58 on reader service card

Simple technology irons out kinks in laser diode output

by John Gosch, Frankfurt bureau manager

V-groove diffusion layer defines stripe width and makes possible extremely small light-emitting area

A simple-to-make but stable laser diode has emerged from AEG-Telefunken's research laboratory in Ulm, West Germany, the source of a number of basic inventions in optical communication. Its stripe-geometry diffusion-type laser transmitting diode exhibits curves of laser output power versus current without any nonlinearities, or so-called kinks.

In continuous-wave operation, these curves are kink-free over a laser output range of better than 25 milliwatts. In pulsed operation, the curves are free of kinks over a range up to several hundred milliwatts, depending on the laser pulse length and repetition rate.

Stable. In laser diodes, a kink-free output power vs current curve over a wide range is crucial because it spells stable transmissions for optical communication systems. Furthermore, such a curve ensures that the radiation characteristics, and thus the coupling of light into the optical fiber, are independent of the laser-driving current, explains Oskar Krumpholz, head of the lab's optical device development section.

To achieve a kink-free curve, however, the width of the stripe from which the laser light emanates must be as narrow as possible. In conventional laser transmitting diodes with a stripe width of 6 micrometers or more, a kink-free curve is difficult to obtain. To get around that problem, makers have reduced the stripe width to below 6 μm. But achieving such narrowness usually calls for rather complex manufacturing.

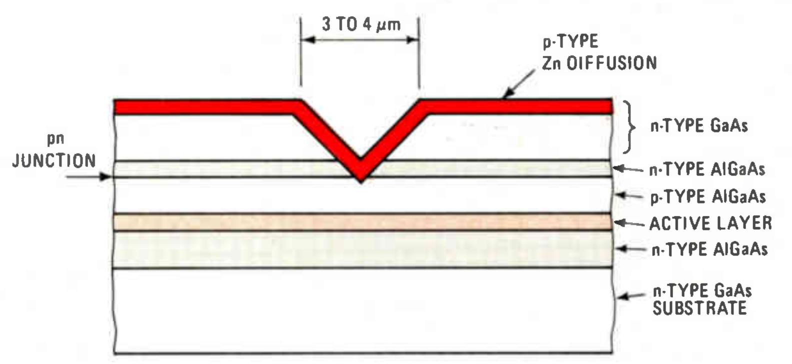
V groove. That is where the lab's simple fabrication technology comes in. Its key is a V-shaped groove etched into the surface of a gallium arsenide–aluminum gallium arsenide laser crystal system. (RCA has also chosen V grooves for its laser diode, but it uses two per device [*Electronics*, April 12, p. 52].)

The groove, from 3 to 4 μm wide at its broadest spot, determines the shape of the diffusion front and defines the stripe width (see diagram below). The diffusion is controlled such that its front extends through the first pn junction (which is reversely polarized) only over a very narrow width. Since the diffusion can be precisely controlled, the stripe width can likewise be accurately controlled.

To start, an n-type AlGaAs layer, about 0.5 μm thick, is grown on the p-type AlGaAs layer of a conventional double-heterostructure laser diode. Next, an n-type GaAs layer, roughly 3 μm thick, is grown on top of the first layer. Layer growth is by the liquid-phase epitaxy processes generally used to make laser diodes.

Subsequently, the V groove is made in a preferential etching process through a photoresist mask in the surface of the crystal. After removing the mask, a shallow p-type zinc diffusion, at about 700°C, converts the adjacent n-type AlGaAs layer into a p-type layer below the V groove only. Then, ohmic contacts are applied to the top and bottom surfaces, and finally the laser diode is mounted, with the V groove face down, onto a copper heat sink.

As the groove profile determines the diffusion front, a very narrow current channel can be obtained simply by adjusting the diffusion depth. That channel forms the light-emitting area in the active layer. From the point of view of technology, the technique is much simpler than that used in laser diodes with a



Groovey. V-shaped groove is key to simple fabrication of AEG-Telefunken's laser diode. It also yields a small light-emitting area, which makes possible efficient coupling into a fiber.

Eliminating the kinks

In what way is AEG-Telefunken's laser diode better than other such devices? That's the question potential buyers might ask, given what is available from RCA, Laser Diode Labs, and Hitachi [*Electronics*, March 29, p. 35], to mention but a few. All claim to be producing easy-to-make, inexpensive, reliable devices with kink-free outputs and other desirable electrical and optical characteristics.

But the rub is, as Oskar Krumpholz, head of the optical device development section at Telefunken's research lab in Ulm, puts it, "Laser diode development is very much in a state of flux now." For one thing, many design approaches are being tried. The goal: manufacturers know they must end up with new techniques in order to make the devices economically.

To complicate matters, according to Krumpholz, diode makers are no longer concentrating solely on making their device live longer. Now, they are working on things like the long-term constant behavior of such parameters as linearity, noise, and radiation characteristics.

Kink-free output vs current curves are the prerequisite for the long-term stability of these parameters. How much can be done and needs to be done depends on the application. **-John Gosch and Harvey J. Hindin**

built-in waveguide, for example. Such diodes require many more fabrication steps, which raises the cost and may reduce the yield.

Small. Using the new technology, Krumpholz's team has produced laser diodes with a light-emitting area measuring only 0.1 to 0.2 μm vertically and up to 5 μm laterally [*Electronics*, June 7, p. 69]. As a result, as much as 80% of the light can be coupled into a graded-index fiber with a core diameter of 50 μm and a numerical aperture of 0.2.

The experimental block-shaped diode, about 80 μm high, 250 μm wide, and 400 μm long, puts out light at a wavelength of 800 to 860 nanometers. The light-beam width is 30° to 40°. The laser's operating life at room temperature is estimated at 1 million hours, Krumpholz notes.

The diode has already been tested in a trial pulse-code-modulation optical-transmission system operating at up to 1 gigabit per second, a rate that allows the simultaneous transmission of as many as 15,000 telephone channels. Because of its high linearity, the diode is also suited for analog communication systems—for TV signal transmission, for one. In fact, the team is already preparing to use its diode in such an application.

West Germany

Data-input link goes infrared for process-control applications

Portable input terminals for process-control computers have been around for quite a while. They use one of two standbys—wires or radio links. Electronics giant Siemens AG, though, believes there is a use for a new link employing infrared light.

Its IR-based data-input system (see photo) is the latest in its arsenal of remote-control equipment. Early next year, the system, together with a process computer of the company's 300 series, will be installed at the West German auto maker Volkswagenwerk AG. There, inspectors will use the portable calculatorlike terminal to enter data on production flaws of cars as they come down the assembly line. At the end of the line, the defective cars can be routed onto a repair line.

The system may also be used to trigger the operation of motors, relays, and related equipment controlling an assembly line. Other uses are in monitoring numerically controlled machine tools or process equipment. A more common application is sending data to a process computer for storage and later processing for statistical purposes.

Why? But why use IR beams instead of cables or radio links? Obviously, a cable attached to a portable terminal restricts mobility. On the other hand, radio waves are susceptible to the electromagnetic fields that originate, for example, from arc- or spot-welding equipment that are found in many plants and that could render a radio-based input system inoperable.

"No such problem exists with an infrared light link because such a link is virtually immune to interference," Erich Gelder, head of the electronic subsystems group in Siemens's Munich-based Components division, points out. (IBM Corp. agrees on the benefits—it recently announced a similar system that is still in the experimental stage.)

System operation is relatively simple. As Gelder explains it, the data signals keyed into the battery-powered terminal modulate a 90-kilohertz carrier, which in turn modulates the invisible IR beams. The latter are picked up at a so-called data collector mounted on the ceiling or high enough on the wall not to be cut off from the beams by intervening equipment.

After demodulating and amplifying the signal, the collector feeds the data over wires to an interface and then to the computer. The amplification is such that interference from, for example, welding equipment has no effect.

Two-way. Communication may of course also occur the other way. The return data, which may indicate a decision the computer has made, is shown on the terminal's light-emitting-diode display. The transmission speed in both directions is either 2,400 or 4,800 bauds. The terminal-to-collector IR link may be up to 20 meters, or 66 feet, long.

To generate the beams, the terminal uses nine Siemens LD271 IR transmitting diodes whose current of 2.5 amperes, in pulses up to 10 microseconds long, produces enough

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Beaming in. Siemens' data-input system links a portable, calculatorlike terminal (left) via IR beams to a "data collector" (right), which is connected to a computer by wires.

light power to bridge the 20-m maximum terminal-collector distance. The 950-nanometer light is picked up by the data collector's two silicon photodiode receiving elements, type BP104, also from Siemens, having a light-sensitive area of 16 square millimeters. These elements are installed at opposite ends in the glass-bulb-type collector so they can receive light from any direction.

For communication in the other direction, the collector uses 84 LD271 transmitting diodes, and the terminal a single BP104 receiving element. The large number of transmitting diodes in the data collector ensures that the data can be received by many terminals used within the 20-m range. -J. G.

Japan

Scanning electron microscope examines fine-line integrated circuits

A low-acceleration scanning electron microscope developed by Hitachi Ltd. promises to fill the void in visual inspection equipment suitable for keeping fine-pattern integrated-circuit production lines operating smoothly.

Conventional scanning electron microscopes with acceleration voltages of about 20,000 volts have the required resolution but charge up insulating layers, which distorts the image. Removing the insulating layers before using the microscope means destroying the wafer or device. So would coating the product with a thin layer of aluminum, which also adds a processing step.

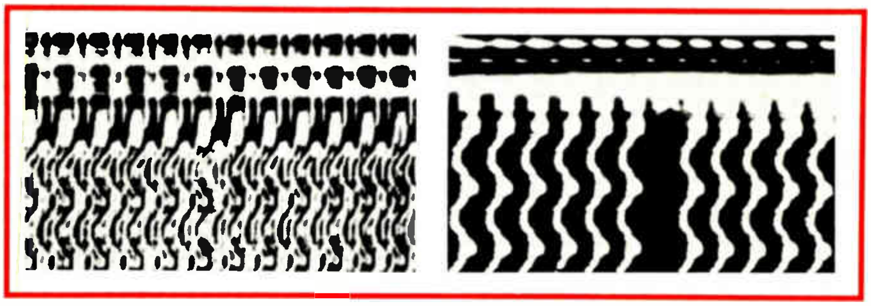
The nominal 1,000-V potential of Hitachi's microscope—in fact variable from 500 to 7,000 V—does not charge up the insulating layers, however. The unit can scan the lower of two layers of aluminum metalized wiring, except where it passes under the upper layer. It can also view the device through the micrometer-thick layer of polyimide with which Hitachi coats some devices.

The microscope uses a new electron gun with a field-emission–type cathode similar to one in an electron-beam exposure unit recently built by Hitachi [*Electronics*, June 21, p. 70]. The gun has a higher current density than conventional cathodes; thus the beam comes from a smaller spot and can be focused down to the desired small-spot size more easily.

The gun also greatly reduces the differences in the initial velocities of electrons that are encountered when thermionic cathodes are used. The larger velocity differences would prevent the electron lens from focusing the beam to the desired size.

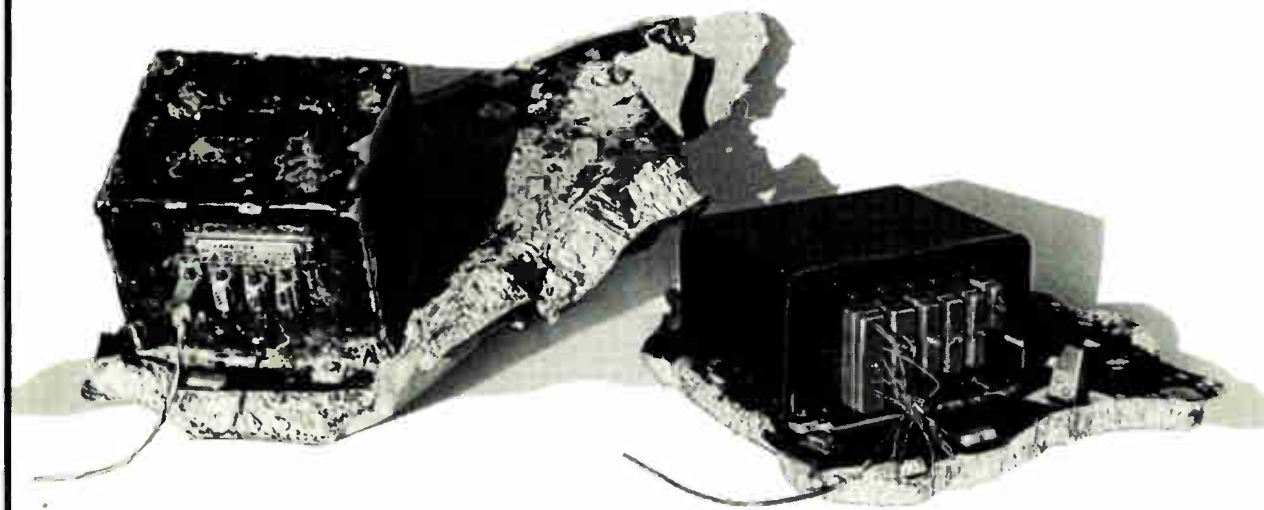
Also featured is an energy filter with a maximum resolution of 200 millivolts. The filter passes only those secondary electrons emitted from portions of the sample having more than a given potential. Thus the potential distribution on a device can be measured to obtain design data or to determine the integrity of metalized interconnections. The potential measurement range is ±15 V, and the resolution when using the filter is 500 angstroms.

Along the way. The microscope thus permits wafers or chips in process to be checked and then returned to the assembly line. Mounted and assembled chips can also be checked through all process steps up to sealing in a molded package or attachment of a cover in the case of a ceramic package. The sample table is fitted with a 120-pin probe for wafers up to 4 inches in diameter and a socket for chips



Fine work. Conventional scanning electron microscopes use thermionic cathodes to produce images (left). Hitachi uses a field-emission cathode, which permits greater resolution (right).

THE ONE THAT GOT AWAY...



...ALMOST

At 23.51 on September 13th, 1977 the range safety officer at Cape Canaveral destroyed the OTS-1 launch vehicle in response to alarm signals from one of its engines.

The separated satellite continued to return normal telemetry until it slid beneath the waves off the Atlantic coast.

Over a month later, the corroded remains of the satellite were recovered, and returned to their manufacturers. The above photograph shows the Instrumentation Electronics and Squib Driver units as received back at BTM, where they were connected, unopened, to their checkout equipment and subjected to full electrical acceptance tests. They passed. 100 %.

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mounted in dual in-line packages.

Hitachi has its prototype system at work in one of its semiconductor plants and is ready to take orders for similar systems. It estimates that the price in Japan will range between $400,000 and $480,000, depending partly on the options chosen. Because of the high cost of these systems, they will likely be used mostly for solving particular production problems rather than for routine checking. **-Charles Cohen**

Great Britain

Simple keying method prints Chinese fast

Chinese-language text, extending generally to some 7,000 characters, has resisted modern printing and communications technology despite many attempts to tame it. One of the latest, though, appears to have gone a good way in getting it under control. Monotype International Ltd. is teaming its advanced laser photocomposer to a keyboard and editing system for Chinese characters that has been rushed from concept to development in only six months.

The principles on which the keyboard is based derive from S. C. Loh, a professor of computer science at the Chinese University of Hong Kong. Monotype has merely implemented his ideas with the aid of the microprocessor in its editing terminal and a minicomputer in its laser photocomposer, Lasercomp.

Explains Brian Gaines, the Redhill, Surrey, firm's technical director, the printing problem is even more severe for the Chinese language than for Japanese, as the latter is confined to 3,000 characters. Consequently, many solutions developed for Japanese need further tailoring for Chinese.

After surveying the options, Monotype, which is backed by Britain's National Enterprise Board, took a license on Prof. Loh's system. "It was simple, aesthetically pleasing, and it appealed to my engineering instincts," says Gaines.

Each character is determined by a series of keystrokes. In effect, the operator specifies the character by choosing each element in the traditional vertical and horizontal sequence taught to Chinese children. Simple characters would thus comprise two strokes side by side; the more complex ones might comprise six or more strokes:

Even so, the resulting keyboard is relatively complex, requiring 236 keys. However, Monotype needed only to adopt a printer's keyboard for mathematical text to fit on both the Chinese radicals, or subcharacters, and a full alphanumeric text.

The characters are not composed from the keyboard. Rather, they are already stored with fine precision on an 80-megabyte disk pack. The keyboard is used only to specify identifiers by which characters can be called up. Therefore there is no need to enter any positional information, as in some systems that build the image with each keystroke.

Speedy. Keying with this system comes naturally to Chinese operators, although they may never have seen a keyboard before. "Skilled Chinese operatives can achieve speeds of 10,000 to 12,000 keystrokes, or between 2,000 and 2,700 characters, per hour," Gaines says.

He bases the estimates for his system on one sold to the Chinese Printing Corp. This system links a photocomposer in Peking and one in Shanghai, together with keyboard systems and editing terminals.

In operation, each keystroke produces an 8-bit output on punched tape. If the resulting tape is fed directly to the composer, the byte sequence defining a character is referred to a directory in one section of the disk cartridge and an address is called up at which the matrix defining the character is held. For recent demonstrations for the Chinese Printing Corp., 4,800 characters were stored on disk, but the total will eventually be raised to 7,000.

Composing. The Lasercomp itself operates by raster-scanning a laser beam across photosensitive film under computer control at a resolution of 1,000 lines per inch. As the beam scans, a laser modulator switches the spot on or off every 0.001 in. High-resolution characters can thus be built up in matrix form from data held on the disk.

For editing purposes, Monotype has come up with a cathode-ray-tube display terminal and keyboard controlled by a Z80 microprocessor. The system repeats in miniature the operation of the photocomposer. It has a directory of the 4,800 keystroke combinations defining each character, and for each a simplified 14-by-16-dot matrix representation can be called up from main store. The directory and the matrix representations fit into 256 kilobits of random-access memory. With the terminal, a user can edit text before transferring final copy to the compositor. **-Kevin Smith**

Around the world

Japanese VHS video cassette recorder gets fast search . . .

Speedy search for program material—at 15 times the six-hour playback speed—is featured for the first time in a VHS video cassette recorder. The unit, from Mitsubishi Electric Corp., also has a two-hour playback speed. Sony Corp., which this spring pioneered a picture search at 20 times the playing speed in its Betamax recorders, had implied that only Betamax machines were capable of adding a fast search.

. . . as VCRs sell out in West Germany

Sales of video cassette recorders in West Germany have risen so sharply that producers, primarily Japanese, are up against supply bottlenecks. "Above-average sales increases," says Sony Corp., maker of the Betamax. Victor Co. of Japan, producer of the VHS, reports that "the supply from our factories in Japan isn't keeping up with demands from the West German market."

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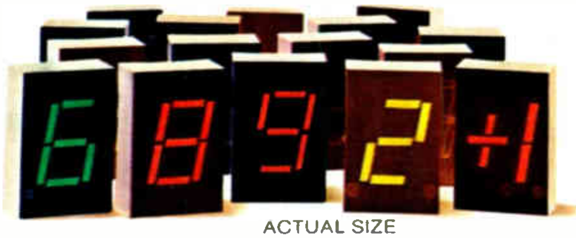

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DLY 7663	Yellow†	C.C. 7 seg D.P. right	1500	$1.95
DLY 7666	Yellow†	Univ. ± polarity overflow	1500	$1.95
DLG 7670	Green	C.A. 7 seg D.P. left	640	$1.95
DLG 7671	Green	C.A. 7 seg D.P. right	640	$1.95
DLG 7673	Green	C.C. 7 seg D.P. right	640	$1.95
DLG 7676	Green	Univ. ± polarity overflow	640	$1.95

†Samples now, production 1st quarter 1980.

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Circle #67 for information on touch switches

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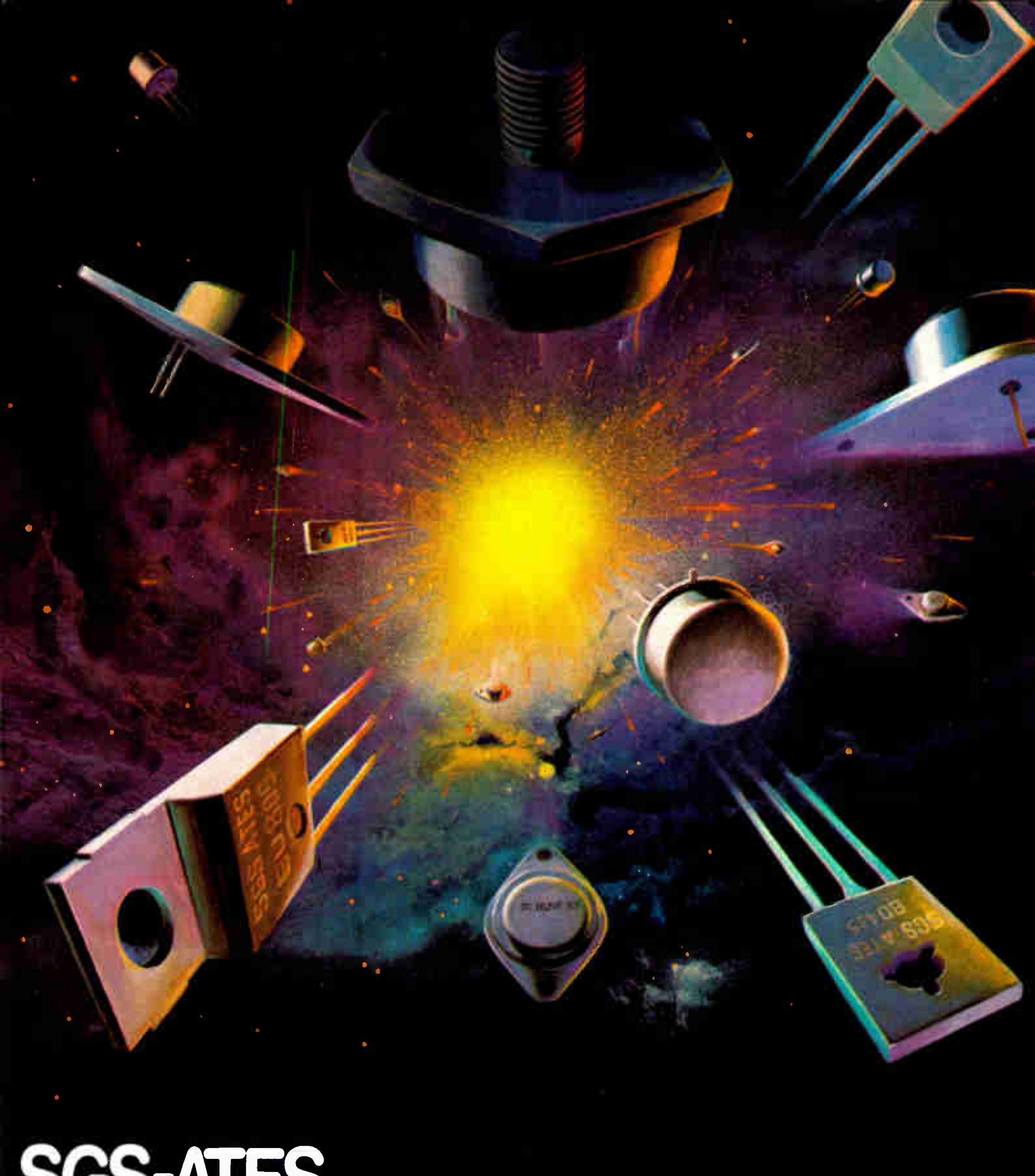
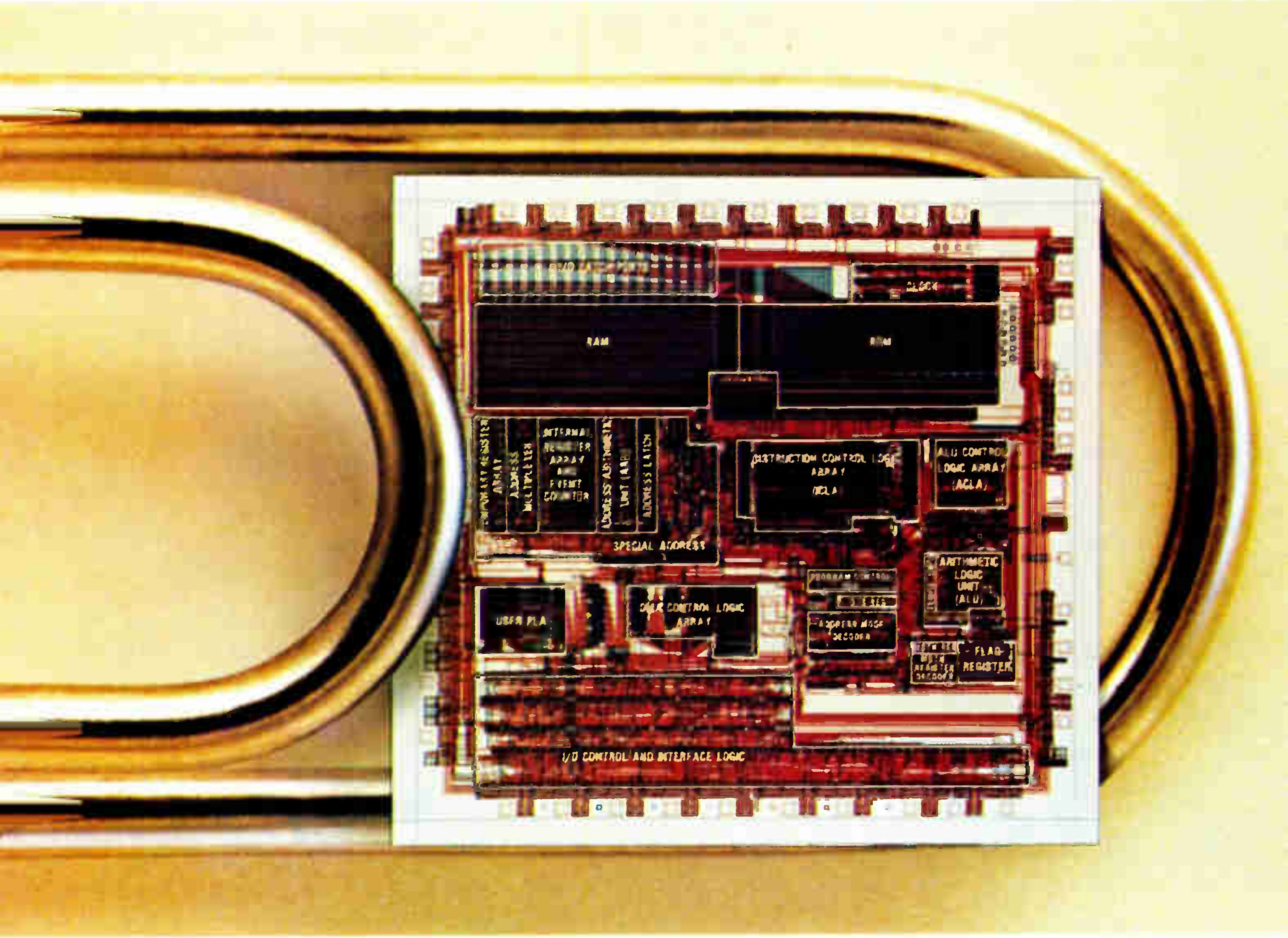


The one-chip computer: offspring of the transistor



The MAC-4 one-chip computer, developed for a variety of telecommunications applications, is compared to a standard-sized paper clip. The chip's numerous functional areas are labeled.

One of the transistor's latest descendants is the Bell System's 30,000-element MAC-4 "computer-on-a-chip." It's another in a long line of microelectronic developments that have come from Bell Laboratories.

The MAC-4 is so efficient that a program written on it takes 25 percent less storage space than that required by most other microcomputers. Its assembler language, C, also developed at Bell Labs, has features that make MAC-4 easier to program, debug and maintain. And the MAC-4 can handle anything from nibbles to bytes to words with its 4-, 8-, 12-, and 16-bit operations capacity.

Like other one-chip computers, the MAC-4 has sufficient memory to support its varied tasks—3000 nibbles of read-only memory and 200 nibbles of random access memory coupled to 34 input/output ports.

Fabricated with the latest CMOS technology, the MAC-4 needs little power. Thus it is well matched to a variety of telecommunications applications.

It started with the transistor

MAC-4 is just one current example of the many microelectronic devices to come from Bell Labs since we started the solid-state revolution with the invention of the transistor in 1947.

Over the past three decades, our advances in materials, processing, and devices have been vital to solid-state technology. These include:

- The Junction Transistor
- Crystal Pulling
- Zone Refining
- Field-Effect Transistor
- Diffusion
- Solar Cell
- Oxide Masking
- Thermocompression Bonding
- Photolithography
- Epitaxial Film Process
- Magnetic Bubble Memory
- Charge-Coupled Device
- Semiconductor Heterostructure Laser Used in Lightwave Communications
- Electron-Beam Exposure System

Today and tomorrow

Today, we continue to make important contributions to solid-state technology. For example, we've developed a rugged 65,536-bit RAM that can tolerate processing faults. Corrections can be made on the chip itself, so we can get more usable chips out of each manufacturing batch—and thus lower unit costs.

In materials processing, we've developed a technique for precisely controlling the growth of successive atomic layers of single crystal materials. This "molecular beam epitaxy" process is finding increasing use within Bell Labs and elsewhere in the electronics industry. We've used it to fabricate a device that permits us to double the speed of electrons by channeling them into crystal layers where they meet less resistance.

Other advances, in X-ray lithography and new resist materials, for example, promise to help place more elements on microelectronic devices and thus enhance their ability to perform important tasks.

As the solid-state revolution continues, these and other developments from Bell Labs will play an important part in it. What's important to us is the promise these advances offer for new telecommunications products and services. Like the transistor, MAC-4 and its solid-state relatives will find more and more applications in the nationwide telecommunications network.

For further information, or to inquire about employment opportunities, write: Bell Laboratories, Room 3C-303, 600 Mountain Avenue, Murray Hill, N.J. 07974.

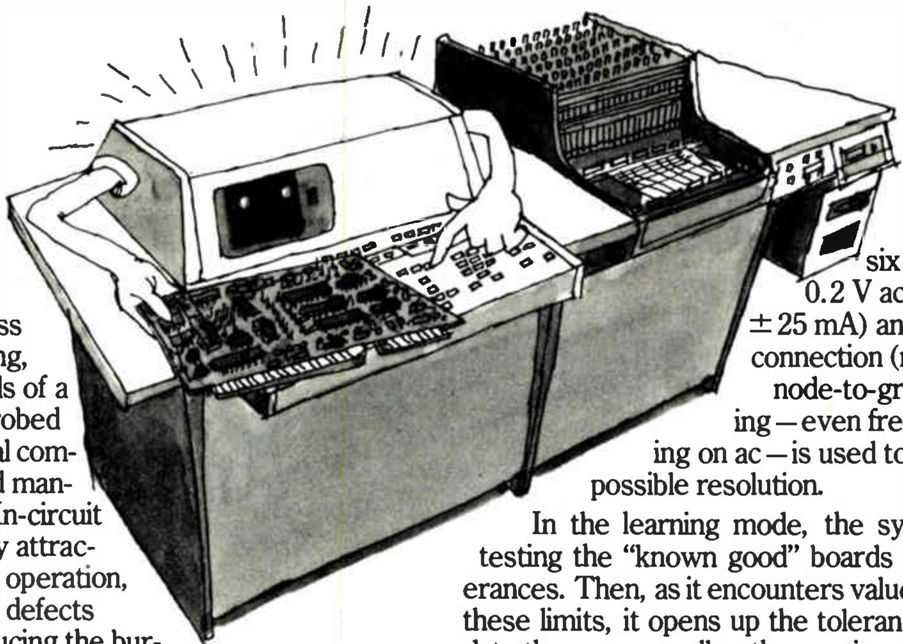
Bell Laboratories

From Science: Service

Teradyne finds the practical solution.
No. 11 in a series.

The self-programming board tester

Just give it a dozen good boards.



One of the fastest growing segments of the ATE business is "in-circuit" testing, in which the innards of a circuit board are probed and tested to reveal component defects and manufacturing errors. In-circuit testing is especially attractive as a screening operation, weeding out gross defects early and thus reducing the burden on the more expensive functional test systems.

As many people are finding out, however, the heaviest burden of all has less to do with testing than with test programming. Thus, if the in-circuit tester is to pay off as a screening device, it should not consume programming time more urgently needed somewhere downstream.

Teradyne's solution to this problem is an in-circuit tester (the L529) that writes its own test program while examining a small sample of "known good" boards. The human contribution to the process consists of telling the tester what kind of component (resistor, capacitor, semiconductor, etc.) appears at each node. This is a button-pushing exercise requiring not a semester's worth of electronics, but to make things even simpler the buttons are keyed to the user's own component designators (e.g., Q for transistors, R for resistors, etc.).

To develop the tests required for each type of component, the system employs various combinations of six stimuli (0.2 V dc, 0.2 V ac, ±2.5 V dc, and ±25 mA) and two methods of connection (node-to-node and node-to-ground). Autoranging—even frequency autoranging on ac—is used to achieve the best possible resolution.

In the learning mode, the system first starts testing the "known good" boards to fairly tight tolerances. Then, as it encounters values that fall outside these limits, it opens up the tolerances to accommodate the new as well as the previous values. The ideal limits will of course be just outside the range of actual values measured on the sample of good boards, and the system automatically settles in on these tolerances.

After about a dozen boards have been examined, the test system has a very good idea of what constitutes a "good board." The system, in other words, has been programmed—without tears.

The self-programming in-circuit tester is only the latest round in a full-scale Teradyne attack on test programming costs. Some years ago, we began offering industry's first self-programming backplane testers, and more recently we mounted a massive effort to develop an automatic test-generation system for functional board testers.

It's not that we don't like programmers. But when it starts costing more to program testers than to buy them, it's time to realize that we need automatic programming equipment no less than we need automatic test equipment. It's time for the ATE industry to go APE.

TERADYNE

ISSCC: a sumptuous feast

Gathering of experts from around the world will focus on wide-angle view of solid-state technology

by Roger Allan, Components Editor, and John G. Posa, Solid State Editor

Nowhere has such a diverse program of solid-state topics been assembled under one roof as it has been for the upcoming three-day International Solid State Circuits Conference. The roof belongs to the San Francisco Hilton Hotel, but the floor will be held by the authors of more than 80 technical papers and by 80 panelists as they discuss memories, image sensing, analog and digital circuit design, and data-acquisition and telecommunications integrated circuits.

The conference will run Feb. 13–15, 1980. The 11 evening panels will closely track the daytime topics, and will cover the manufacture and application of large- and very large-scale ICs. Speakers and panelists from nearly every industrialized country will be there. J. Fred Bucy, president and chief operating officer of Texas Instruments Inc. of Dallas, will deliver the opening address, entitled "The Semiconductor Industry Challenges in the Decade Ahead."

New charge-coupled and memory devices will be discussed by many. Two Japanese companies, Nippon Electric Corp. and Hitachi Ltd., will each report in session 2 single-sensor color imagers of similar resolution, proving that the dream of cigarette-pack–sized color video cameras is nearing reality. Fairchild Camera and Instrument Corp.'s MOS/CCD division in Palo Alto, Calif., will describe a 131,840-element monochrome device for use in a periscope camera system.

NEC's Central Research Laboratories in Kawasaki have come up with a 384-by-490-element CCD chip for use in a single-sensor color camera,

ISSCC HIGHLIGHTS

Session	Circuit	Source	Features
MEMORIES AND CHARGE-COUPLED DEVICES			
2.1	Color CCD image sensor	NEC	384-by-490-element monolithic device has a signal-to-noise ratio of 71 dB at 1.5 lux light level.
2.2	MOS color imaging device	Hitachi	485-by-384-element device with on-chip filter resolves 2/3-in color image.
6.2	Battery backup for memories	Mostek	Static 4- and 8-K MOS RAMs operate from 150-μW battery source.
7.1	Cosmic ray memory effects	IBM	Cosmic-ray nucleons and muons may cause errors, especially at high altitudes.
12.1	64-K E-PROM using scaled MOS	Intel	Two polysilicon levels are self-aligned for 0.24-mil^2 cells and a 200-ns access time.
12.2	200-ns, 150-mW HMOS E-PROM	Motorola	Programming of 8-K-by-8-bit memory is quasi-static, with one TTL-level pulse per word.
12.3	64-K E-PROM with redundancy	Mostek	Static 300-ns, 200-mW device has redundant bits for improved yield.
12.4	35-ns, 16-K PROM	Intel	140-mil^2 fuse-link PROM accesses in 25-ns typically, consumes 600 mW.
12.5	4-megabit full-wafer ROM	NTT Musashino Laboratory	3-in. wafer stores Chinese ideograph characters using multigate MOS.
12.6	16-K EE-PROM	Intel	Electrons tunnel through oxide layers less than 200 Å thick in 2-K-by-8-bit memory.
17.1	64-K fractional bipolar memory	IBM	Polysilicon and thin dielectrics are used for MOS densities but at bipolar speeds.
17.2	16-K static MTL/I^{2}L memory	IBM	26,970-mil^2 chip features a 45-to-100-ns access time and a 170-mW power consumption.
17.3	2-K-by-8-bit C-MOS static RAMs	Hitachi	Using buried J-FET technology, 74-ns RAMs consumes 200 mW but only 25 μW on standby.
17.4	Fully static 16-K bulk C-MOS RAM	Toshiba	Six-transistor coplanar silicon-gate cells access in 95 ns and use 1-μW standby power.
17.5	Single-5-V 64-K dynamic RAM	Hitachi	The 40,000-mil^2 RAM dissipates 170 mW, accesses in 120 ns, cycles in 300 ns.
17.6	5-V-only 64-K dynamic RAM	Texas Instruments	Interlocked clock circuits, dynamic sense amps, and a grounded substrate raise performance.

but the 485-by-384-element device from Hitachi's Central Research Laboratory in Tokyo seems more impressive. Interestingly, it is made with MOS technology and not CCDs, and it has an on-chip color filter array.

Don't forget memory. Sessions 12 and 17 hint at what is in store for system designers next year: 64-kilobit ultraviolet-erasable programmable read-only memories and random-access memories; and at the 16-K level, electrically-erasable PROMs and static RAMs, with the Japanese leading the way in complementary-MOS designs. Moreover, it is rumored that late papers may include a 256-kilobit dynamic RAM and/or a 64-K static RAM.

Three U.S. chip makers—Intel Corp. of Santa Clara, Calif.; Motorola Semiconductor Product Group's Mesa, Ariz., IC operation; and Mostek Corp. of Carrollton, Texas—will each give a 64-K E-PROM paper. Although Mostek's 300-nanosecond access time is 50% slower than that of the Intel and Motorola memories, it includes redundant circuitry on its die for a yield advantage.

Intel's sole 16-K EE-PROM paper does not represent all the work being done in this area, as several other semiconductor manufacturers are known to be developing electrically erasable replacements for the 2716 E-PROM. Intel will also report on a quick fuse-link 16-K PROM built with polysilicon fuses that has a typical access time of 25 ns.

Dynamic session. In session 17, "RAMs," three 64-K dynamics will be described. TI will go into the most depth yet about its grounded-substrate part and Hitachi will bring the listener up to date on its MOS memory. IBM's General Technology division in Essex Junction, Vt., will unveil what it calls the 1/N fractional memory; it has the density of MOS and the speed of the bipolar technology it is built with.

Three 16-K static RAMs make up the rest of the session. IBM Labs in Böblingen, West Germany, will report on a fast (45- to 100-ns) bipolar RAM, and Hitachi and Toshiba Corp. of Kawasaki will each present

ISSCC HIGHLIGHTS

Session	Circuit	Source	Features
DIGITAL CIRCUITS			
6.1	MOS buried-load logic	Hitachi	Buried J-FET loads provide gate delays of 0.34 ns and a 0.17-pJ power-delay product.
6.3	Gigabit MOS logic circuit	Fujitsu	Dry processing and E-beam masks build a sub-100-ps-delay frequency divider.
6.4	Emitter-coupled injection logic	Technische Hochschule Aachen, Germany	Self-isolating gates allow I^2L densities at ECL speeds.
7.3	Nitride gates for VLSI MOS FETs	Fujitsu	For submicrometer FETs, silicon nitride is grown for a 70-Å gate insulator.
9.1	10,000-gate C-MOS processor	Fujitsu	Device dissipates 130 mW, has a 400-ns instruction cycle; gate delays are 4–10 ns.
9.2	Single-chip math processor	Intel	Chip multiplies, divides, finds square roots, and evaluates transcendental functions.
9.3	n-MOS computer architecture	Data General	Family of CPU chips executes 16-bit register-to-register operations in one 400-ns cycle.
9.5	400-ps, 18-bit bipolar ALU	NEC-Toshiba	A 0.4-ns, 2.5-mW ALU has 1,300 gates and a 7-ns read-modify-write cycle.
16.5	C-MOS PLL with prescaler	Matsushita Electronics	Phase-locked loop, best suited for 4-bit microprocessors, operates at 200 MHz.
ANALOG AND DATA-ACQUISITION CIRCUITS			
1.1	12-bit a-d converter	Advanced Micro Devices	C-MOS converter uses successive approximation, has laser-programmed ROM for 50-μs conversions.
1.4	5-ns, 8-bit d-a subsystem	Plessey Research	Also on chip is a 1.3-ns comparator and a stable reference for 15-MHz conversions.
7.5	Pressure sensor with pulse output	Stanford University	14,756-mil^2 die contains capacitive sensor and may replace piezoresistive transducers.
11.4	8-channel data-acquisition system	Analog Devices	C-MOS chip contains dual-port memory and DMA; operation is microcomputer-transparent.
13.1	X-band pulsed GaAs FET	Microwave Semiconductor Corp.	Amplifier delivers 10 W peak at 8 GHz, 5 W continuous at 6 GHz.
15.3	Two-quadrant analog multiplier	Analog Devices	Laser-trimmed device affords ± 0.25% accuracy with 100-MHz signal bandwidth.
15.4	I^2L servo for video	Sony	Containing 3,000 I^2L gates and 350 linear elements, chip controls VTR servo motors.
TELECOMMUNICATION AND SIGNAL-PROCESSING CIRCUITS			
3.2	Signal processor for voiceband	NEC	Using parallel multiplications, the 3-μm n-MOS chip samples voiceband signals at 8 kHz.
3.3	VLSI echo canceller	Bell Labs	111,428-mil^2 n-MOS chip has 2,704 shift-register bits and 3,300 gates – 35,000 devices in all.
3.4	Telecommunications signal processor	Bell Labs	In 80 ns, it will decode an instruction, fetch data, and perform a 16-by-20 bit multiply.
8.2	Gyrator video filter	Philips Research	6-MHz, 17,050-mil^2 bipolar chip separates luminance, chroma, teletext, and sound in a TV receiver.
14.1	500-V 2-by-2-element cross-point array	Bell Labs	IC employs gated diode switches to replace metallic switches in telephone loops.
14.4	Digital line interface	BNR Inc. Bell Northern Research	C-MOS IC does clock recovery, speed conversion, multiplexing, synchronization and interfacing.
14.6	Subscriber line interface	Bell Labs	Device uses floating power conversion to minimize size and energy consumption.

C-MOS designs. The Toshiba chip, which consumes a paltry 1 microwatt in standby, was discussed previously at the International Electron Devices Meeting [*Electronics*, Dec. 6, p. 124].

Aside from memories, the papers concerning digital electronics span a range from fast logic design to LSI circuits dedicated to specific applications. Session 6, entitled "Digital Circuit Techniques," includes four papers that explain how to make electrons go faster. Hitachi uses buried-load MOS for an incredible power-delay product of only 0.17 picojoule. Fujitsu Ltd.'s laboratories, Kawasaki, uses 1-micrometer lithography and dry processing for buried MOS field-effect transistors with switching delays of less than 100 picoseconds. The Technische Hochschule in Aachen, West Germany has merged emitter-coupled logic with integrated injection logic for what it calls emitter-coupled injection logic, and Mitsubishi Electric Corp. of Itami, has found a way to run its static induction transistors at 1 gigahertz. Finally, in session 7, Fujitsu will show how it grows 70-angstrom-thick nitride insulators, a technique that can improve almost any VLSI device.

Let chips fall. Session 9 comes back down to earth with systems on chips. Fujitsu is there, too, and it will tell why it designed a 10,000-gate microcoded C-MOS microprocessor. The chip sports a 400-ns microcycle, and so does the n-channel MOS microprocessor to be explained in the same session by Data General Corp. of Westboro, Mass. Intel will finally discuss its nearly VLSI math processor chip [*Electronics*, April 26, p. 33], and NEC-Toshiba Information Systems Inc. of Tokyo will reveal a very impressive 18-bit bipolar arithmetic and logic unit that can, among other things, support a 7-ns read-modify-write cycle.

The importance of data acquisition and conversion is underscored by three day sessions. Session 1, "A-d and D-a Converters," includes a paper from National Semiconductor Corp., Santa Clara, Calif., on a monolithic 12-big analog-to-digital converter that includes a direct-memory-access port and interfaces directly with a microprocessor. Researchers at Plessey Research Ltd., Towcester, England, will talk about an 8-bit monolithic 15-megahertz successive-approximation a-d converter that features an incredible settling time of 5 ns. Session 1 also includes a paper from Analog Devices Inc., Wilmington, Mass., on a monolithic bipolar a-d converter with a calibrated voltage output that eliminates the need for conventional power-supply voltage trimming.

Session 11, "Data Acquisition," contains two papers from Harris Semiconductor, Melbourne, Fla., one on an autozeroing sample-and-hold integrated circuit and another on a monolithic 5-volt reference for 12-bit a-d converters that is temperature-regulated and trimmed. National Semiconductor will discuss an instrumentation amplifier IC that is 99.99% linear will be discussed. And Analog Devices will report on an eight-channel data-acquisition system with a DMA porto.

Monolithic talk. "Analog Circuit Techniques" is the title of session 15, which deals with a variety of monolithic device developments. For example, a peak detector that combines a transconductance amplifier with a differential current-switching circuit will be reported on by Precision Monolithics Inc., Santa Clara. Two of the more notable speakers in this session are Barrie Gilbert of Analog Devices and Robert Widlar, now a consultant living in Jalisco, Mexico. Gilbert will talk about a two-quadrant analog multiplier whose bandwidth is 100 MHz and accuracy is within ±0.25%. Widlar will talk about a bipolar operational amplifier (National's LM11) whose dc error-reduction scheme allows 100 microvolts of offset error, 1 μV/°C of drift, and 20 picoamperes of bias current at 125°C [*Electronics*, Nov. 8, p. 44].

Microwave ICs are becoming a subject of major importance as communications frequencies increase and the desire for higher power levels at those frequencies also increases. Session 10, "Microwave Circuits," contains several papers on gallium arsenide FETs. Rockwell International Corp.'s Science Center, Thousand Oaks, Calif., will report on multilevel logic-gate implementation of GaAs ICs using Schottky-diode FET logic. And an example of how high in frequency some microwave device developments have gotten will be heard in a paper from the Hughes Aircraft Co., Torrance, Calif. Its researchers will talk about power combiners near a frequency of 94 GHz. They used double-drift Impatt diodes to generate 20.5 watts of peak power from two diodes and 40 W of peak power from four diodes at that frequency, with over 80% efficiency.

Systems approach. Session 13, "GaAs FET Amplifiers," discusses microwave device developments on a system level. One paper from Microwave Semiconductor Corp., Somerset, N. J., discusses a pulsed GaAs FET amplifier for the X band. The amplifier reportedly delivers 10 W of peak output power at 8 GHz. Fujitsu Laboratories will talk about the design of a 12.5-GHz amplifier capable of delivering 3.5 W, and engineers at Watkins-Johnson Co., Palo Alto, Calif., will present a paper on a GaAs metal-semiconductor FET am-frequency coverage from 350 MHz to 14 GHz.
coverage over 350 MHz to 14 GHz.

Two areas where dedicated LSI makes sense are telecommunications and signal processing. Three very complex signal-processing devices will be covered in session 3. NEC of Kawasaki will present its answer to Intel's 2920 analog microprocessor and American Microsystems Inc.'s S2811 signal-processing peripheral chip: a voiceband signal processor made with 3-μm n-MOS technology. Bell Laboratories in Murray Hill and Holmdel, N. J., will give a paper on a VLSI echo-cancelling chip; the Holmdel and Allentown, Pa., labs will present another on a telecommunications processor that can churn through a 16-by-20-bit multiplication in 80 ns.

Bell Labs will also present two papers in session 16. The first, from Murray Hill, is on a 2-by-2 crosspoint array that can withstand 500 volts and surge currents of up to 1 ampere. The second, out of Naperville, Ill., concerns a floating-power subscriber-line interface circuit that uses an energy-conversion technique to provide 1,000-V transient isolation in low-level analog and digital switching networks. □

Communications

WARC puts off major decisions

But failure to act on shortwave allocations as well as frequencies and positions for satellites prevents split

by Kenneth Dreyfack, Paris bureau

A wave of relief swept through Geneva's International Conference Center as the 1,900-odd delegates to the World Administrative Radio Conference (WARC) ended 11 weeks of talks with the realization that they had managed to keep the session from splitting along north-south lines, as had been feared.

But in keeping the conference together, the representatives of more than 30 countries left unresolved two of the most sensitive issues before them: allocations for shortwave broadcasting and reservation of frequencies and orbital positions for geostationary satellites. What's more, it was clear as the conference closed on Dec. 5 that some nations were planning to ignore rulings on some of the issues that WARC did resolve.

"I am not going to pretend that everything that happened pleased us," summed up U.S. delegation chief Glen O. Robinson. "But there was no overall north-south division, and that is what is encouraging." Delegates from many other countries, from both the developed and developing worlds, echoed Robinson's evaluation. "Nobody was forced to his knees," said René Bletterie, a leading member of France's delegation. "There were no stunning defeats and, of course, no stunning victories either."

Although regional and limited-scope conferences are held fairly often by the International Telecommunication Union, the United Nations body that rides herd over the spectrum, full-dress WARCs occur not more than once every 15 or 20 years. The allocations decided upon, covering virtually the entire electromagnetic spectrum, will essentially determine how the spectrum will be used until the turn of the next century. Hence the importance of the decisions taken for all spectrum uses—from radar and ship-to-shore radiotelephone to direct-broadcast satellites and microwave ovens.

Until recently, the ITU was firmly controlled by a handful of highly developed countries that viewed frequency allocation as a nonpolitical, technical matter to be worked out by engineers. But since the last WARC was held, in 1959, ITU membership has nearly doubled, and nearly all the new members represent the less developed countries. This means they hold the balance of power under the ITU's one-nation, one-vote decision-making process. Further, the new members strongly believe that past WARCs have in fact had unmistakable political repercussions—namely, holding the less developed world down.

Fight expected. One area where a bitter conflict between the less developed nations, with their numerical superiority, and the developed countries, with their economic and technical strength, was expected was over so-called "*a priori* planning" of frequencies and orbital positions for geostationary satellites for both fixed services and direct broadcasting. Whereas the U.S. and other developed countries argued for maintaining the present first-come, first-served system for assignments,

WARC talk. Delegates to World Administrative Radio Conference gather at International Conference Center in Geneva.

the others insisted that unless orbital slots were set aside for eventual use by developing countries, the industrial countries would freeze out everyone else by using up all of the limited space available. Unable to reach a substantive compromise, the WARC deferred the issue.

Two stages. The delegates decided to schedule a two-stage geostationary satellite planning conference, tentatively set for 1984 and 1986. The first session is to "decide which space services and frequency bands should be planned" and then "establish the principles, technical parameters, and criteria for the planning." The second session is to make the actual assignments.

But though this may sound as if the smaller countries got their way, the developed countries are convinced that the first session will demonstrate that planning is technically impracticable. U. S. delegates insist that the 1984 conference will examine alternatives to planning to guarantee all nations equitable access to geostationary orbital satellites.

The WARC also decided to hold a two-session conference beginning in 1983 to assign specific frequencies to specific countries for broadcast in the high-frequency band. Increased allocations for shortwave broadcasting was one of the top U. S. priorities going into the WARC, and the conference did allocate 850 megahertz of new frequencies. But there was no increase in the existing 6- or 7-megahertz bands, and the U. S. says it will not pledge compliance with the WARC regulations unless the future conference expands them.

Satisfied. Glen O. Robinson, head of U. S. delegation, said he was pleased that there was no split along north-south lines.

The Americans "reserve the right to insist that the future conference make allocations in the bands adjacent to the existing 6- and 7-MHz bands. If not, we might operate in those adjacent bands anyway," Robinson threatens. Canada, Great Britain, Italy, the Vatican, Israel, and West Germany joined him.

But several other nations, including the Soviet Union, refused to pledge compliance with the WARC decision because they felt too much of the hf band was allotted to broadcasting. In some cases, the motivation is political—some countries do not want their citizens to receive foreign broadcasts. But much of the opposition from Third World countries stems from the fact that increased broadcasting allocations come at the expense of frequencies previously set aside for the inexpensive point-to-point hf communications links extensively used in the developing world.

Although the U. S. and Canadian delegations were happy with the compromise worked out over use of the 11.7-to-12.7-gigahertz band for feeder links for fixed-service and direct broadcasting satellites [*Electronics*, Dec. 6, p. 35], the U. S. officially took exception to the WARC decision on another U. S.-Canada issue—increased allocations for land mobile services in the uhf band, especially 470 and 806 MHz.

The U. S. went into the conference seeking equal sharing of the 470-to-890-MHz band among broadcasting, fixed, and mobile services in the ITU's Region 2, which includes North and South America. The WARC gave its blessing for equal sharing above 806 MHz, but would afford land-mobile services only secondary status below 806 MHz. The U. S. WARC delegation says, "U. S. land-mobile interests were protected and the opportunity for future growth in the U. S. was preserved. However, the conference imposed certain regulatory agreement procedures . . . which in essence did not provide for equality of operation."

Part success. The U. S. likewise obtained only partial satisfaction in its effort to raise the top end of the a-m radio broadcast band from 1,605 kilohertz to 1,860 kHz, with part of the increase devoted entirely to broadcasting and part shared with other services, most importantly radar. As it turns out, broadcasting will have exclusive use of the band up to 1,625 kHz and will be the primary user of the 1,625-to-1,705-kHz band. Actual broadcasting above 1,605 kHz will not begin before the late 1980s, as a regional conference to assign new frequencies will not take place before 1988.

In addition to its official objections to the WARC rulings on hf broadcasting and uhf land mobile communications, the U. S. refused to pledge observance of WARC allocations for hf maritime mobile services, for radar in several bands within the spectrum, and for mobile satellite services in the uhf band, between 225 and 400 MHz. The WARC did make new hf allocations for maritime mobile communications, but not below 10 MHz. The U. S. desire for a clear frequency within the uhf band for mobile satellite communications stems from the Pentagon's plans to establish satellite-based comunications systems capable of linking mobile land, air, and maritime stations worldwide.

In past ITU and WARC sessions, the U. S. has only once refused to pledge compliance. Asked about the five U. S. rejections registered this time, Robinson tried to downplay their significance. "It doesn't imply a lack of faith in the system as a whole," he says. "We are not talking about operating willy-nilly anywhere we want." The U. S. is far from alone in refusing to go along with decisions taken by the WARC, something that poses a serious threat to the validity of future ITU regulations. "If it becomes standard practice for important countries to take exception to decisions on significant issues, the whole legitimacy of the ITU comes into question," explains France's Bletterie. □

Electronics abroad

French electronics outpacing economy

Though nation's overall growth will be relatively modest, electronics producers foresee another good year

by Kenneth Dreyfack, Paris bureau

French President Valéry Giscard d'Estaing has to perform much the same economic juggling act as other West European leaders, somehow keeping unemployment and inflation under control while business is sluggish and energy prices are zooming. But the French usually manage to be different from their neighbors, and one big difference at the moment is the election that Giscard will have to win in early 1981 if he wants the job of running the country for another seven years.

Votes of the out-of-work almost always go to the out-of-power. The result is that Giscard may well decide to stoke the economy with public spending if necessary next year so that the lack of jobs will not cost him his.

For the moment, though, Prime Minister Raymond Barre does not show signs of easing up substantially on his austerity program. Barre's forecasters say the economy will grow a modest 2.5% in 1980, but some nongovernment forecasters expect that the figure will turn out to be closer to 2%. Either way, the year ahead should be a lackluster one for French business overall.

For electronics markets, it will be a different story. "In 1980, I believe that we will see a continuation of the trends characterizing 1979, which will not have been a bad year overall," says Pierre-Leonard Mestre, director of components and electronic-tube activities for Thomson-CSF, France's largest commercial electronics group. *Electronics*' consensus forecast, although it does predict slowing growth, by and large confirms his reading. It pegs total 1980 markets at $9.96 billion, up 10% over the total estimated for 1979. Components markets should fare reasonably well, too.

In the equipment chart, the difference stems mainly from computers and communications equipment. They are recession-proof in 1980, believes Jacques Lorre, an electronics market specialist at the quasi-governmental Bureau d'Informations et de Prévisions Economiques (BIPE). A serious slowdown in the economy, he adds, would stifle business in consumer goods, instruments, and industrial electronics. But like nearly all French forecasters, Lorre does not foresee a serious recession in 1980.

That's entertainment? Consumer electronics, then, is the soft sector. The survey predicts factory sales of $2.70 billion for 1980, a modest 7% rise over the 1979 figure. If the forecast is on the mark, this means some improvement for set makers after a mediocre year.

The key, of course, is color television. Set sales bounded up to $1.048 billion last year, partly because masses of French soccer fans wanted to watch the nation's team play in the World Cup, a semiannual event that was telecast by satellite from Argentina. But color TV stagnated this year. Sales are likely to peak up again, thinks Henri Battle, chief of economic studies at the industry association Groupement des Industries Electroniques. The stimulus will be another feast for sports gourmands: the 1980 Olympic Games in Moscow. *Electronics* forecasts a market of $1.190 billion next year, up from $1.095 billion. But the mark will not be made if there is a substantial drop in real household

FRENCH ELECTRONICS MARKETS FORECAST
(IN MILLIONS OF DOLLARS)

	1978	1979	1980
Total assembled equipment	**7,939**	**9,003**	**9,959**
Consumer electronics	2,356	2,517	2,701
Communications equipment	2,080	2,510	2,760
Computers and related hardware	2,808	3,218	3,650
Industrial electronics	241	264	295
Medical electronics	192	212	234
Test and measurement equipment	191	212	236
Power supplies	71	76	83
Total components	**1,653**	**1,819**	**1,979**
Passive and electromechanical	915	1,001	1,076
Discrete semiconductors	211	229	245
Integrated circuits	238	288	346
Tubes	289	301	312

Note: Estimates in this chart are the consensus estimates of consumption of electronic equipment obtained from a survey made by *Electronics* magazine in September and October 1979. Domestic hardware is valued at factory sales prices and imports at landed costs. Exchange rate: $1 equals 4.20 francs.

incomes as inflation inexorably continues to take its toll.

Among other mature entertainment electronics hardware, hi-fi equipment figures to do best, even though buyers in France get stung with a 33% value-added tax. The chart puts the market at $436 million, up 10%. Video cassette recorders once again will spurt, but the market is still small, only some $26 million; VCRs have yet to catch on in France. But nonvideo games are catching on. "The market is developing very fast, almost as fast as in West Germany," reports the BIPE's Lorre.

Aware of software. Computer makers and their blood brothers, the office equipment makers, will provide the major lift for equipment markets next year, according to *Electronics'* survey. The sector surged past the $3 billion mark in 1979, the chart shows. Another bound upward, this time 13%, is forecast for 1980. That would put the market at $3.65 billion. (In these estimates for computer hardware, leased equipment is counted as if it had been sold outright.)

Marketing experts at a major computer maker in France see three significant trends developing next year. One is a continuing explosion in distributed processing. That will continue to cause accelerated sales of minicomputers and terminals, the building blocks for distributed systems.

The other two notable market developments, say these marketing men, concern software. As the software content of systems continues to rise, customers are balking at ordering it along with hardware in a package and instead want to order the two separately, often with custom software. As a result, a growing collaboration between hardware manufacturers and software or systems houses seems inevitable. This would be particularly important in France, whose software industry is large and active, ranking second only to that of the U. S.

Within a few years, the reasoning is, computer customers may go to service companies for their needs rather than to computer companies. The service companies would then be the ones to pick the right hardware to answer the user's needs.

In the meantime, "the French telephone network is developing very quickly, at the rate of 2 million lines per year, with about 70% of them digital in 1980," says Jean Syrota, head of the Direction des Affaires Industrielles et Internationales of the Direction Générale des Télécommunications, the agency that runs the country's telecommunications networks.

The added lines alone would keep the country's telecommunications equipment suppliers humming nicely through the year ahead. But there is more. The DGT, the money-making half of the Secrétariat aux Postes et Télécommunications, has a series of ambitious programs on the drawing board to bring new services to France.

Contracts have been awarded, for example, for the hardware needed for a trial videotext service that will be inaugurated next year in a Paris suburb. Also ordered are preproduction versions of low-cost digital facsimile machines and the small interactive terminals for what might well become a nationwide computer-based telephone directory. All this, plus export business, will keep telecommunications equipment makers on a high plateau for the next few years.

As for the other major categories of commercial equipment—radars, navigation aids, radio equipment, and the like—they will run much as they did this year, reckons Edouard Guigonis, vice president of Thomson-CSF. Guigonis points out that "most telecommunications equipment contracts cover several years, and as far as actual sales are concerned, we already have 90% of our orders for 1980," so any monetary disorders will have little effect [*Electronics*, Dec. 6, p. 116]. The survey puts the 1980 market for communications equipment, including electronic telephone hardware, at $2.76 billion, a 9% rise. That is much less than the spurt recorded this year, when electronic exchange gear bounded up to its currently high level.

Good parts. "The electronics business is far from being in bad shape," maintains Thomson-CSF's Mestre, who says that 1979 growth of between 7% and 8% for components markets should be matched in 1980. *Electronics'* survey is a little less optimistic than Mestre about 1979 growth but tallies essentially the same growth for 1980—an 8% rise that will boost the markets to $1.98 billion.

Drug computer. French pharmacists use this CIT-Alcatel Magenta terminal to order the drugs they need via a central computer at a supply house. It employs phone lines.

There is no quarrel anywhere about the explosive growth of integrated circuits. They came in for heavy demand this year by communications equipment makers, computer makers, and even consumer electronics producers. That demand should continue into 1980. *Electronics* projects the IC market at $346 million, 20% over the 1979 level. All the same, Lorre of the BIPE is slightly leery about what will happen as the months go by. "The curves could be a bit flatter for the last six months," he explains, "because we are now seeing the rate in growth of orders slowing down a bit. That does not mean the growth is ending, just that it is slowing."

Other components sectors will head downward or at best stay flat. But Mestre says there are some notable exceptions among passives—multilayer capacitors and connectors, "especially connectors for avionic and IC applications." Among discrete semiconductors, the notable exception figures to be power semiconductors. □

Solid state

C-MOS picks up ground

Low power, high noise immunity, thermal advantages draw attention as n-MOS becomes more expensive

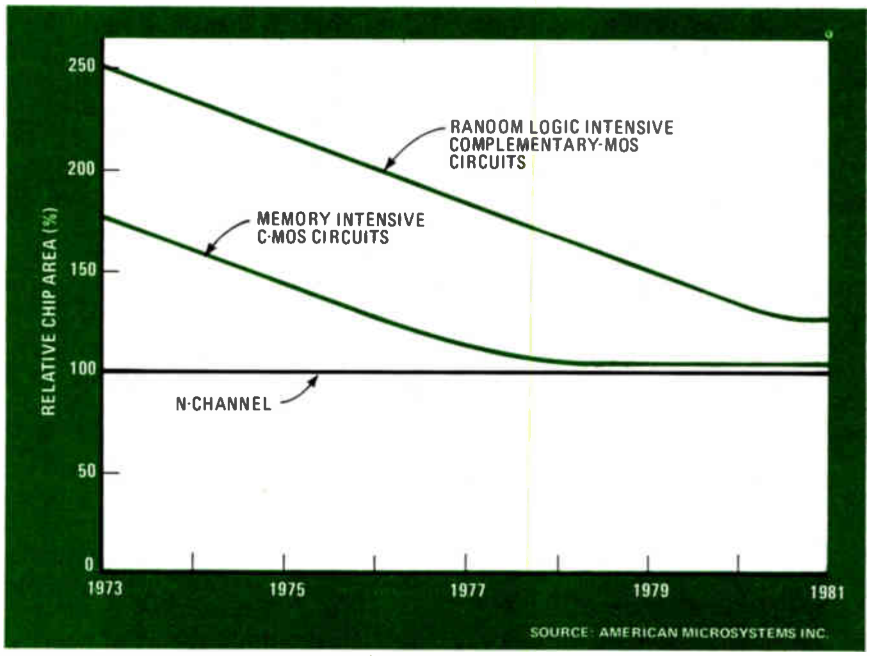
by Bruce LeBoss, San Francisco region bureau manager

Now that n-channel MOS is neck and neck with bipolar technology in the high-speed, high-performance derby, n-MOS producers would do well not to look back: someone might be gaining. And that someone might just be the makers of complementary-MOS, a technology that got off to a slow start but is now picking up speed, especially in microcomputer but also in random logic and linear applications.

Historically a more complex (hence more costly) technology, C-MOS has several inherent advantages over n-MOS, such as very low power dissipation, high noise immunity, a wider power-supply range, and an extended temperature range. Perhaps the two biggest drawbacks for C-MOS, and the reasons its acceptance and support have been marginal, are that it generally has been considered to be slower than n-MOS and, adds Dan Hauer, vice president and general manager of Micro Power Systems Inc. of Santa Clara, Calif., "it was half as dense—a cell that was 50 mil² in n-MOS was 100 mil² in C-MOS."

C-MOS has trailed n-MOS in density and speed principally because of economics. Explains Donald L. Wolleson, C-MOS research and development manager of American Microsystems Inc., Santa Clara: "If you look at wafer costs, C-MOS has been more expensive than n-channel. That's because it requires a few extra furnaces, and the wafers have to sit in the furnaces longer, to drive the p well." That cost penalty, he notes, was about 2:1 about five years ago. Today, while C-MOS wafer costs have held fairly constant, n-MOS is getting more expensive as producers add masks for such things as depletion and depletion-blocking implants. As a result, Wolleson says, "fundamental wafer costs for n-MOS and C-MOS are converging."

C-MOS density also has trailed n-MOS because of its use of guard rings and greater line widths, among other looser design rules. In 1973, there was about a 2:1 penalty in layout area, "which is squared when determining die costs," notes Wolleson. Thus, there was a four-times penalty for die costs and a two-times penalty for fundamental wafer costs that made C-MOS eight times as expensive as n-MOS. Today, with C-MOS density approaching that of n-MOS for memory-intensive circuits, he adds, the economic incentives that favored n-MOS are disappearing.



Downward curve. The die costs of C-MOS and n-MOS are coming closer as it becomes possible to use almost the same size chip for the same number of functions.

Better. Brightening the picture for C-MOS is new high-performance C-MOS processes—such as C-MOS on sapphire from RCA Corp., a pioneer in C-MOS work, Mitel Semiconductor Inc.'s Iso-C-MOS, and National Semiconductor Corp.'s P²C-MOS. "C-MOS speed will now equal or beat its n-MOS counterparts," states Anne Wagner-Korne, National's product marketing manager for low-power microprocessors. And the ratio of function to die area, she continues, "has been greatly improved, although there's still a 20% to 25% penalty." In fact, to build National's NSC800, a new 8-bit central processing unit that is fabricated with a new double-polysilicon C-MOS process, "would not have been possible with older C-MOS processes as it would not have fit in the package," she adds.

A prime example of the improved performance of the new C-MOS processes is Hitachi Ltd.'s new 5147, a mostly C-MOS version of Intel Corp.'s 4,096-bit static n-channel random-access memory, the 2147. The Japanese part has a typical access time of 43 ns, whereas the 2147 using the Intel standard HMOS process has a typical access time of 70 ns. However, as an example of its efforts to keep n-MOS in the forefront even as it experiments with C-MOS, Intel has also introduced a 2147H, fabricated with a scaled n-MOS process called HMOS II, that allows it to achieve a typical access time of 22 ns.

Mitel's soon-to-be-introduced C-MOS version of Motorola's 5802 microprocessor, though designed primarily for low-power functions, is essentially the same size as and expected to be faster than its n-MOS counterpart. The improvement in density comes primarily from the elimination of guard bands and a new isolation technique that involves only a single doping of polysilicon. "Previously, we used a p^+ dopant for the p gate and an n^+ dopant for the n gate. Now, we use only an n^+ dopant and run polysilicon straight between the p and n channels, without any metal bridging," explains Alan Aitken, vice president for operations. This technique reduces the spacing between devices, as well as the area required for interconnections, he adds, and also improves the overall speed of the device.

As an indication of how fast C-MOS is getting, Micro Power Systems has developed a new C-MOS process soon to surface in 4-K static RAMs and other standard and custom products. Developed principally to obtain tighter package density, the process now in production is operating at 50-MHz speeds (20 ns), notes Hauer. Much of the improved performance, he adds, is "the result of new maskmaking and photoresist techniques," among them a dry plasma etch that "enables us to obtain isolation and eliminate capacitance."

These new C-MOS processing techniques are, according to National's Wagner-Korne, "a half step behind n-MOS when they come to the market." Being in that position, she adds, C-MOS vendors "can cleverly copy process improvements, such as electron-beam masks, oxide isolation, and double polysilicon, that are tried and proven, and it eases the acceptance of C-MOS products in the marketplace."

What took C-MOS vendors so long to adopt n-MOS processing enhancements? "At first there wasn't enough demand to justify the R&D money to improve C-MOS technology," explains Jim Coe, director of microprocessor and telecommunications products at Intersil Inc., Cupertino, Calif. Thus, "C-MOS had to wait for the C-MOS microprocessor and associated memories before it would be cost-effective. When the demand grew, vendors began pouring R&D money into C-MOS technology."

Retains advantages. Factors in C-MOS' new life are some of the traditional advantages it has offered, principally low power. "There's about one to two orders of magnitude savings in power that comes from using C-MOS instead of n-MOS," says Jacob Fattal, marketing engineer at Motorola Inc.'s MOS division in Austin, Texas. While low power has always been an advantage, he notes, "we didn't have the technology to implement it. There was not the same density that allows us to put the entire microcomputer on one chip." The density achievable today by C-MOS producers is within 20% or 25% of n-MOS densities and, he continues, "that's why we expect the price of C-MOS eventually to be only 25% to 30% higher than n-MOS.

However, "C-MOS will not replace scaled n-MOS in microprocessor applications," observes Mel H. Eklund, vice president at Integrated Circuit Engineering Corp., Scottsdale, Ariz. Rather, "the two technologies will co-exist, but with C-MOS increasing its market share."

Because of the interest in C-MOS, ICE forecasts that "the C-MOS market will grow from the present 9% (or about $390 million) of ICE sales to 15% in the mid-1980s, or the equivalent of $2 billion annually. This penetration," Eklund adds, "will be at the expense of bipolar linear, Schottky TTL, and scaled n-MOS. □

Instrumentation

ATE companies tackle the data glut

Teradyne and Fairchild have already attacked the problem, with Macrodata also due to add data-management capabilities

by Richard W. Comerford, Test, Measurement & Control Editor

Among semiconductor manufacturers, one thing that isn't in short supply is test data. In order to get parts out the door faster, manufacturers have been demanding and getting faster automated test equipment. The result: more test information, to the point where so many reams of raw test results are being spewed out by the testers that it is just about impossible to keep track of what is actually happening on the test floor, let alone to see what is going on in the overall process.

The ATE manufacturers have seen this problem coming and have started to look for ways to make practical use of all that information. Among those that have already started to provide solutions are Teradyne Inc. of Woodland Hills, Calif., and Fairchild Test Systems Group in San Jose, Calif. In addition, Eaton Corp.'s Semiconductor Test Systems division, which produces the Macrodata line, has announced its intention of providing tester management capabilities in the third quarter of 1980. These companies see the problem in different ways, and their approaches to solutions vary.

A key distinction between the two systems already available, the Test System Administrator from Teradyne and the Integrator II from Fairchild, is the management levels they are aimed at. The TSA is primarily for the test floor manager, who must decide how effectively his testers are being used and what the status of the lot being tested is. Once the information is provided, the system can also communicate it to a higher-level computer for use by upper-level management. The Integrator II, on the other hand, directly provides the higher levels of management with information, while taking care of the test floor manager, too.

According to Hira Ranga, software manager of Teradyne, the TSA philosophy is that "test-system computing power can be joined with general-purpose computing power to solve the test-data reporting problem. Semiconductor manufacturers already have enough computing capability in place to accomplish this."

A package. The TSA is actually a software and interface package that is added to a Teradyne off-line computer, the M365, with a cathode-ray-tube terminal and a minimum memory of 48 kilowords of 32 bits each. This unit was originally designed for off-line program generation for Teradyne's J283 and J325 logic testers and the J384, J387, and J387A memory testers. With the TSA package, it still can operate as a program generator with the added feature that programs can be directly downloaded to the test station.

The TSA hardware consists of two types of interface cards and interconnection cables. The TC492 card controls the data transfer to and from the test system; a card of this type is needed in each tester, as well as in the M365 computer. It contains both an RS-422 and RS-232-C port for communication with a host computer. The other type of card, the TC581, resides in the computer. Its primary function is to cause an interrupt when data is received from

Straight to the top. Integrator II from Fairchild gets data from wide test base, then analyzes it for higher management at the same time as working for the test floor manager.

any tester. Up to seven testers of mixed variety can be controlled from one computer.

Teradyne's system relies on the power of its tester's minicomputer to do much of the data analysis. The tester can present histograms, for example, to the M365 computer for the manager's review. In addition, the TSA itself can generate two types of summary reports. This concentrated data can be passed on to a higher computer for management reporting.

Specialist. Whereas Teradyne relies on the tester itself to do much of the data analysis, Fairchild believes that the test system cannot perform the kind of analysis that today's semiconductor manufacturers need. It provides a host computer that takes the data generated by individual Sentinel and Sentry test systems in different locations and applies sophisticated analysis programs to a wide data base.

Randy Hughes, Integrator program manager, says that the people who really need to look at the test data are not only the people who run the test operation. "It is the yield people, the overall process managers, who have to get a clear picture of what is going on too. For them, it's really a question of synthesizing overall status data quickly and presenting it in an easily graspable form."

Along with the basic system, which consists of an HP 2117F central processor, a 19.6-megabyte disk, an interactive video terminal, and a line printer, comes a large variety of processing programs that are oriented toward both device users and manufacturers. Using these programs, a wide variety of useful graphic displays can be generated. Data can be displayed in histograms, shmoo plots, scatter plots, and wafer maps, as well as in detail reports. Further, the system memory can be expanded to 120 megabytes and data can be stored for months so that composite maps, plots, and records can be used to spot trends and failure modes.

Different path. Eaton Corp.'s Macrodata line has taken still another approach. In mid-1980, it will provide a hardware interface for its M-1 memory test system that will let users hook the tester to any computer compatible with Digital Equipment Corp. equipment. Bob Adler, sales manager for the M-1, says that this approach "will let the user decide at what level and to what extent the tester data should be processed." He points to the fact that the M-1 can be equipped with a PDP 11/23 if the user wants to perform analysis at the tester.

At the same time as this capability is being designed for the M-1, sister division Kasper Instruments is working on a similar interface for its wafer fabrication systems. Thus, it will eventually be possible to put the entire fabrication process under computer control. Undoubtedly, other ATE companies are going in the same direction. □

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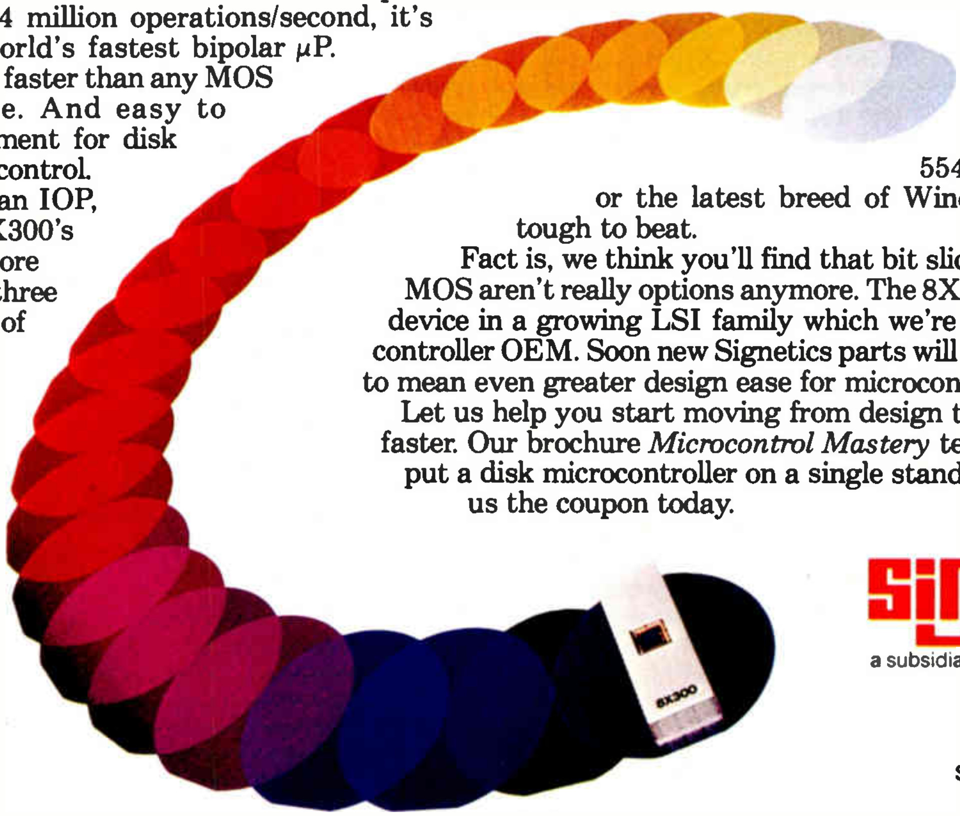

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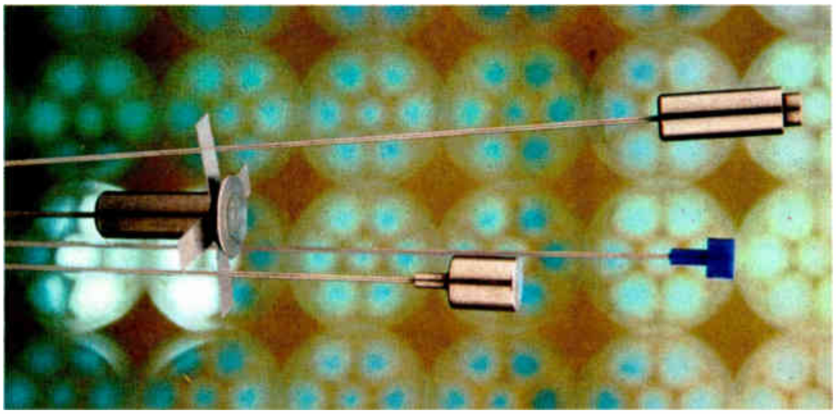

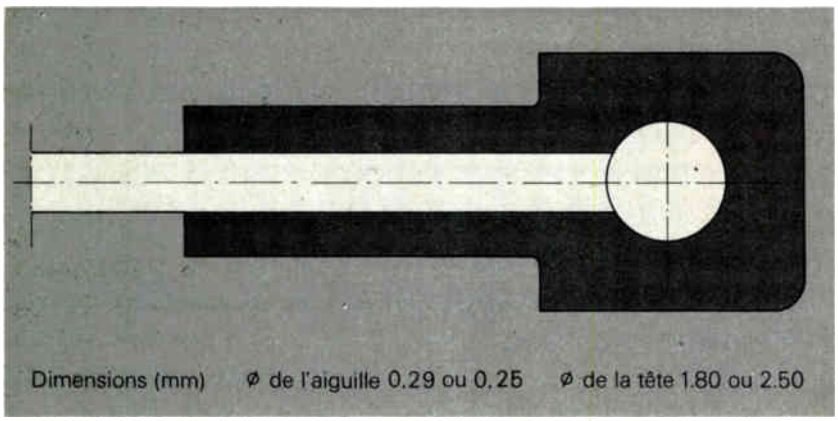

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LSI ready to make a mark on packet-switching networks

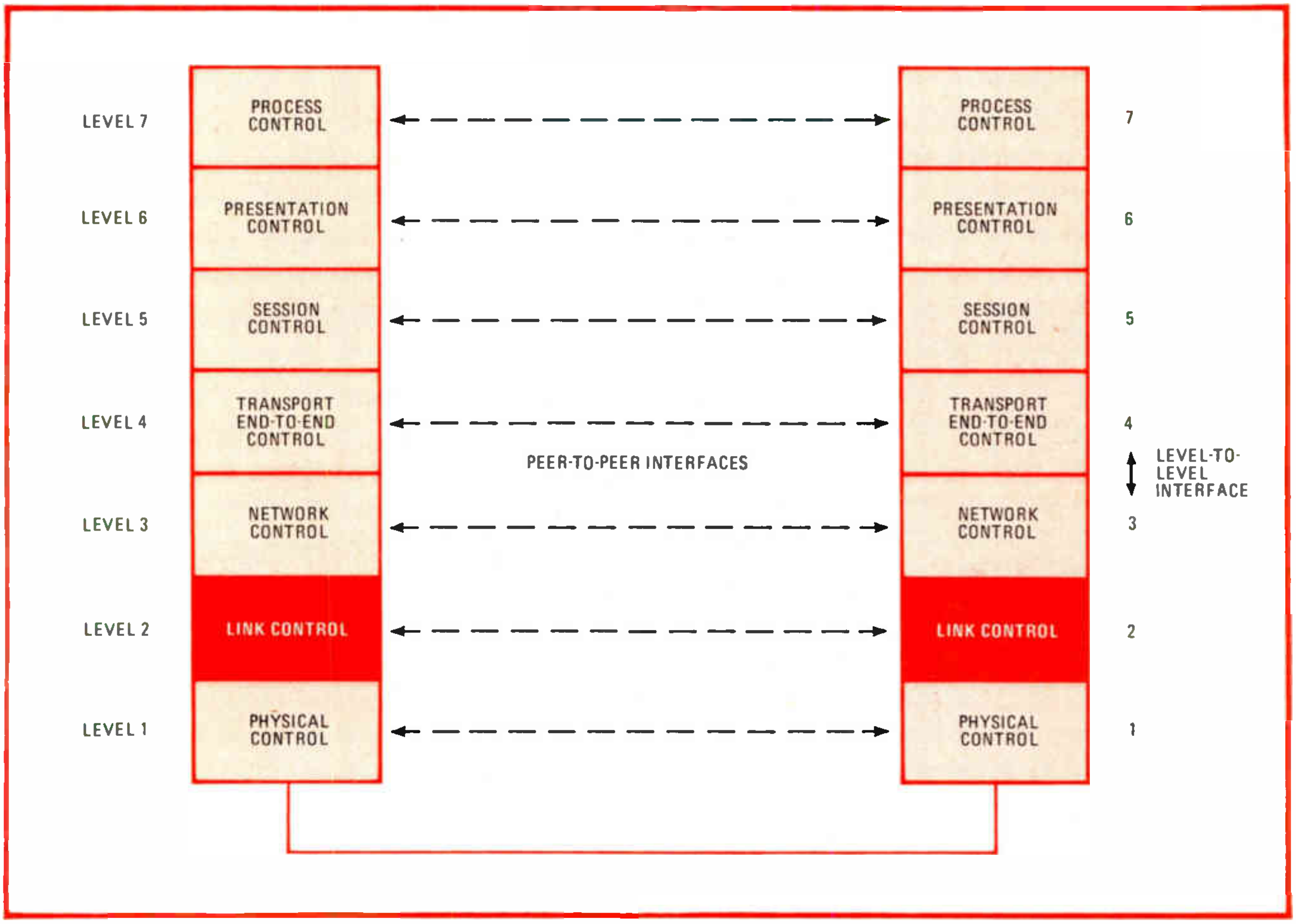
New chip's link-control capabilities ease connection to terminals: Part I

by Geary L. Leger, *Western Digital Corp., Newport Beach, Calif.*

☐ Packet-switching networks are prime targets for the application of large-scale-integrated circuit technology. In fact, sometime during the first quarter of next year, this useful and expanding approach to data communications will have its first dedicated LSI circuit, one designed to take advantage of LSI's potential for lower cost and greater reliability.

This is the first of two articles. It deals with the overall characteristics of packet-switching networks. Part 2, which starts on page 95, describes an LSI chip being developed for Level 2 control per the X.25 protocol for packet networks.

The circuit is the Micro Packet Interface chip, or μPAC, being developed by Western Digital. It will handle Level 2 control of the link between a data terminal and a network node as set forth in the X.25 protocol established by the Consultative Committee for International Telephony and Telegraphy (CCITT). Because these



1. Layered architecture. Independence among system levels allows changes to be made to one level without disrupting the operation of other levels; and adjacent level is affected only if the changes affect the interface to that level. Standards apply to peer-to-peer interfaces.

Recent efforts in packet switching

The security, survivability, and economic advantages of packet-switching data-communications networks have not gone unnoticed in either the military or the corporate sectors. Though still in its infancy, this type of communication is growing rapidly.

According to Defense Advanced Research Project Agency director Eugene H. Kopf, the latest military packet effort aims to find the optimum architecture for a command and control network of 5,000 to 10,000 small packet radio relay terminals whose purpose would be to insure survivable control over strategic weapons. The network voice and data-packet radios would provide line-of-sight communications throughout the continental U. S. after an attack.

The civilian sector has continued the development of packet networks from their modest beginnings. In 1972, Bolt Beranek & Newman Inc. founded Telenet, a public packet-switching network taken over this year by General Telephone & Electronics Corp. GTE Telenet Communications Corp., Vienna, Va., completed installation this month of a packet-switching exchange in San Juan, Puerto Rico, for ITT World Communications Inc. The new service allows businesses and industrial organizations to link to the ITT gateway and transmit and receive data over shared transmission lines to data terminals or computers on the U. S. mainland.

Tymnet Inc., Cupertino, Calif., is the largest public packet-switching network in the U. S. It has so many customers that it issues a 34-page directory describing 200 data bases accessible through its network. Tymnet now serves 250 computers in the U. S.; it recently added New Zealand to its list of countries served, bringing the total to 26.

The Japanese have not been idle in adapting packet technology to their needs. Nippon Telegraph and Telephone Public Corp. started work on its digital data-exchange system in 1971 and had installed packet-network equipment in seven cities by late 1978. This commercial packet-switching network (called D50) is expected to go into full service this year. D50 conforms fully to Recommendation X.25 of the Consultative Committee for International Telephony and Telegraphy.

The packet network industry has come a long way since the first operational system (Arpanet) was installed by the Defense Advanced Research Projects Agency in 1969. In 1976, the CCITT adopted X.25 as a standard three-level protocol for interfacing terminals to public packet networks—a major step for the industry. Even though it has been criticized as being too complicated, X.25 has stimulated interest in packet networks.

However, packet switching is not the answer to all data and voice communications problems, as some have claimed. Gino J. Coviello of the Defense Communications Agency in Arlington, Va., concluded in a recent study that the number of channels traversing a particular transmission link and the network topology and architecture have a significant impact on the cost-effectiveness of a packet-switching network. Ray W. Sanders, president of Computer Transmission Corp., says, "Packet switching will take its rightful place alongside circuit switching." A hybrid approach combining features of both circuit and packet switching "provides the best of all possible worlds," according to Sanders. **-Harvey J. Hindin**

networks are relatively new, familiarity with the Level 2 link control and other details of their operations is not widespread. Yet the purpose of the μPAC is intelligible only in the context of such an understanding.

To date, most data-communications systems use circuit-switching techniques. A physical circuit is assigned either permanently (a private, leased line) or for the duration of the call (a dial-up line). But of a given line's total available time, only a small percentage is actually taken up by data transmission. A system for dynamic allocation of the physical circuits, in contrast to static circuit-switching allocation, requires the logic and memory capabilities of computers.

Prior to the late 1960s, static circuit allocation was more economical than using computers in a dynamic allocation system. The low cost of today's minicomputers and microprocessors and the dramatic drop in the cost of memory, however, make dynamic allocation more economically feasible in many cases. It is most suitable in multipurpose applications—digital communications systems linking various types of data terminals such as facsimile machines, computerized data bases, interactive keyboard printers, or cathode-ray-tube terminals.

Historically, communications systems have been developed to satisfy one application at a time. The wide variety of computers, terminals, and technologies has led to the development of many incompatible networks. A time-sharing network may connect many asynchronous interactive keyboard printers on dial-in lines at 110 or 300 bits per second. A clustered CRT application such as IBM's 3270 may operate synchronously at 1,200, 2,400, or 4,800 b/s.

The incompatibility of different types of equipment and the protocols they use for communicating greatly reduces the reliability and efficiency of data communications as a whole. A single corporation may, for example, use several incompatible networks.

Security and survivability

The technique of sending a digital data in short packets, rather than in a continuous stream, was first suggested by Paul Baran of the Rand Corp. more than a decade ago. The packets are transmitted between intermediate points in the network, called nodes, or DCEs, for data-circuit–terminating equipment (see table).

This dynamic-allocation technique has two major inherent advantages over circuit-switching methods. It increases data security, since the message is broken up: all the packets would have to be picked up and combined by an intruder before he could use the data. And system survivability and reliability are enhanced by the large number of linked nodes. Alternate routes will get a message through if some of the nodes or links are malfunctioning or destroyed. The security and survivability are of great interest to the military. The commercial sector is also developing this type of system (see "Recent efforts in packet switching," above).

The problem of equipment and communication-protocol incompatibility is an international one, since data communications is international. This question is addressed at the global level by the CCITT (see "Setting the standard," p. 93).

The difficulty of expanding, modifying, or upgrading existing data-communications networks is another problem that is tackled by the new packet-switching systems. Any communications system represents a large capital investment, and down time can be disastrously expensive. A user cannot simply tear down an old network and substitute a new one with the latest advances. New terminals and technologies must be phased into the existing structure without interrupting operation. This calls for a degree of system flexibility.

Layered architecture

Packet-switching networks achieve this flexibility through layered (or multilevel) architecture [*Electronics* May 24, 1979, p. 111]. Several standards organizations have been working on the specifics of this concept.

The importance of layered structure is easy to understand. Suppose Mr. Jones, an executive, wishes to talk to Ms. Smith, another executive. Jones (level 4) tells his secretary (level 3) to get Smith on the line. Jones' secretary dials the number (level 2). An electromechanical switching mechanism connects the two phones (level 1). Smith's phone rings (level 2). The two secretaries converse (level 3) and pass on the information that the call is ready to their bosses. Smith and Jones now communicate (level 4).

Jones was never concerned with the electromechanical switching mechanism, nor with Smith's telephone number; he was primarily concerned with talking to Smith (peer to peer) and secondarily with talking to his secretary to get the call set up.

Multilevel communications systems are structured in a similar fashion. The protocol standards are prepared for connection in the peer-to-peer layer. Standards do not define the interface between adjacent layers. This is intentional: terminal manufacturers are thus left free to design the adjacent-layer interface in their own way. This enhances system flexibility. If a layer is changed or upgraded, nonadjacent layers are not affected.

X.25 defines and standardizes three levels. There are as many as four more definable levels (Fig. 1), but much work remains to be done to standardize these higher levels. Level 1 may be viewed as a data-exchange mechanism serving Level 2. Level 2 is a data-exchange mechanism serving Level 3, and so on.

Three standardized levels

Level 1 concerns itself with the link's physical interfaces. Level 2 deals with link control. It includes setting up and disconnecting a link, the control of flow between data generators and data receivers, and bit-oriented frame structure. The μPAC from Western Digital is designed to perform the Level 2 functions. Level 3, network control, includes the procedures for establishing and disconnecting the virtual circuit and for controlling the flow of data packets in the network.

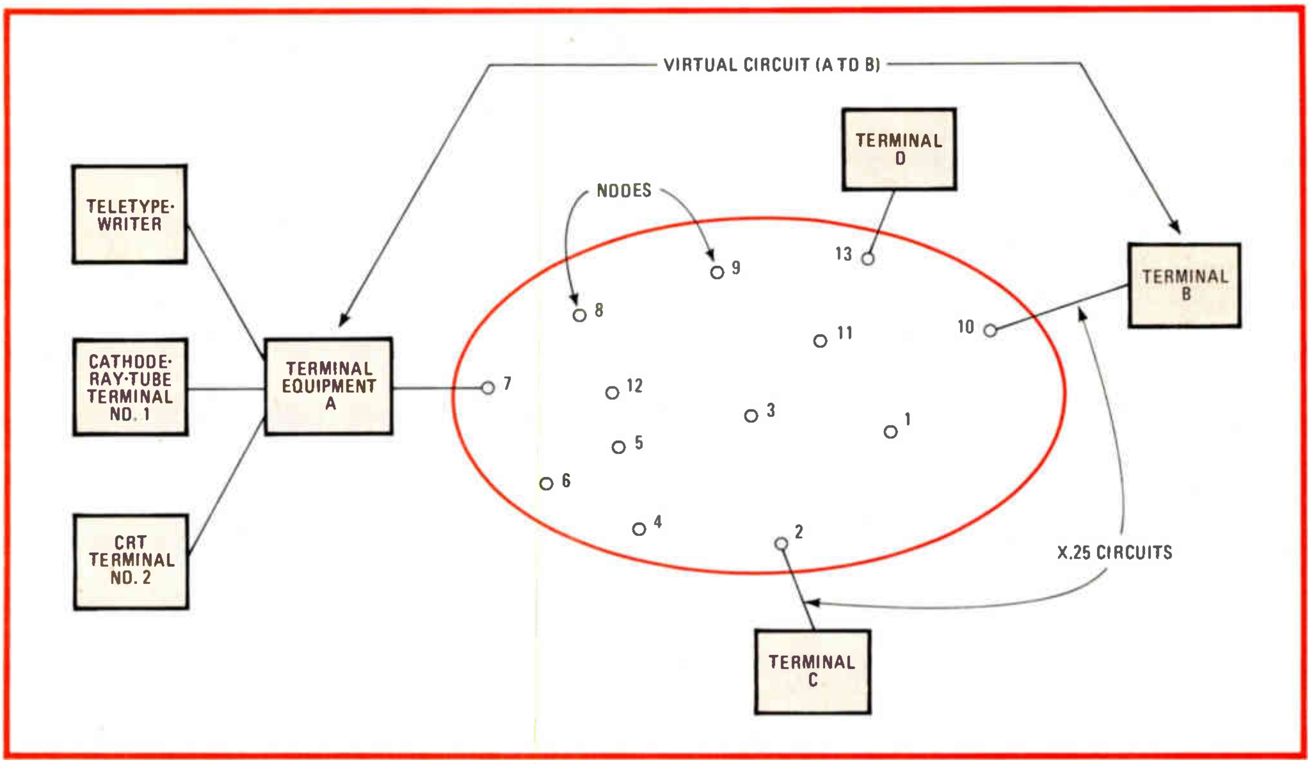
In a packet network, the sender or receiver has a terminal (commonly called DTE, for data-terminal equipment) with a distinct address. Part of the gear at a network node might also be called data-terminal equipment. The packets of data are transferred from node to node and finally to the receiver's terminal.

When a node receives a packet, it stores the packet, decides where and when to forward it on the basis of the packet's destination and priority and the load conditions of the network, and then does so. This store-and-forward facility is the key to the network's ability to allocate circuits dynamically. Packets going from terminal A to terminal B in Fig. 2 could follow the node path 7-12-11-10, 7-5-3-1-10, or any of a number of others.

Dynamic routing within the network is transparent to the users at their terminals. The path data takes is called a virtual circuit between A and B: the terminals communicate as if a dedicated circuit joined them. In order to

PACKET-SWITCHING NETWORK TERMINOLOGY

ADCCP	Advanced Data-Communications Control Procedure (ANSI X3.66)
ANSI	American National Standards Institute
ATDM	asynchronous time-division multiplexing
BOP	bit-oriented protocol
CCITT	Consultative Committee for International Telephony and Telegraphy
DCE	data-circuit-terminating equipment (network node)
DTE	data-terminal equipment (user's terminal)
FCS	frame check sequence
HDLC	High-level Data-Link Control protocol (ISO 3309)
ISO	International Standards Organization
ITU	International Telecommunications Union
I frame	information frame, known as a packet under X.25
LAP	Link-Access Procedure (X.25)
LAPB	Link-Access Procedure, Balanced (X.25)
Link control	X.25 Level 2 control for linking DTE and DCE, including link initialization, establishment, and disconnection, and control of data flow on the link
Network control	X.25 Level 3 control of virtual circuits in network, including circuit establishment, disconnection, and reset, and the control of packet flow
N1	maximum number of bits in a packet
N2	maximum number of command retransmissions
PAD	Packet Assembly/Disassembly facility (defined in CCITT recommendations X.3, X.28, and X.29)
Physical interface	X.25 Level 1 specifications for the physical connection of DTE and DCE, including electrical parameters and transmission rate
S frame	supervisory frame
SDLC	Synchronous Data-Link Control protocol
T1	time minimum before retransmission of unacknowledged command
U frame	unnumbered frame
X.25	CCITT recommendation for packet-switching network protocols (others include X.3, X.28, and X.29)

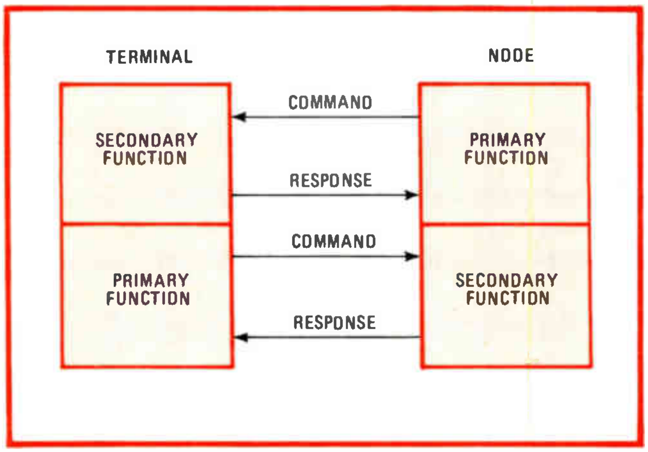


2. Many possible paths. The user of a packet-switching network at his terminal sees no difference between the virtual circuit and an ordinary physical link. Network control may send the data packets through a changing series of nodes as system traffic conditions change.

establish a virtual circuit, terminal A transmits a call-request packet that includes the caller's address and the address of terminal B, the destination. Terminal B accepts the request by returning a call-accepted packet to A, and the virtual circuit is set up.

Circuit sharing

Several simultaneously active virtual circuits can be set up by interleaving packets. This asynchronous time-division multiplexing (ATDM) exploits the fact that a typical virtual circuit carries data for only a small percentage of the time it is set up. It differs from other time-division multiplexing schemes in that a dedicated time slot is not provided for each virtual circuit being multiplexed.



3. Addressable functions. A terminal or node has a primary function that sends commands and receives responses. Its secondary function, which has a different address, responds to received commands. Arrows represent system logic, not physical wires.

In the multilevel packet-switching architecture, Level 2 (also known as the link level or the frame level) involves the point of contact between the subscriber's terminal and the network node it is linked to directly.

Each station, be it terminal or node, has two logical functions needed for addressing and signal implementation, called primary and secondary (Fig. 3). The primary function transmits commands and receives responses; the secondary function does the reverse—it receives commands and transmits responses.

The structure of the data frames used for this communication is common to all bit-oriented protocols (BOPs)—High-level Data-Link Control (HDLC), the essentially similar Advanced Data-Communication Control Procedures (ADCCP), and the Synchronous Data-Link Control (SDLC) protocol worked out by IBM [*Electronics*, Jan. 18, 1979, p. 137]. The Level 2 protocol defined by X.25 is an outgrowth of HDLC.

The frame is simply a block of serial data exchanged between two terminals or a terminal and a node. It consists of a flag, an address field (or A field), a control field (or C field), an information field (or I field), a frame-check sequence (FCS), and another flag. Depending on the frame type, the information field may or may not be included.

There is a flag at either end of a frame; a single flag may close one frame and open the next. Data transparency is provided within the frame by the transmitting station: a logic 0 is inserted after all sequences of 5 contiguous logic 1 bits, so that no transmitted data is inadvertently read as a flag, which has the binary form

Setting the standard

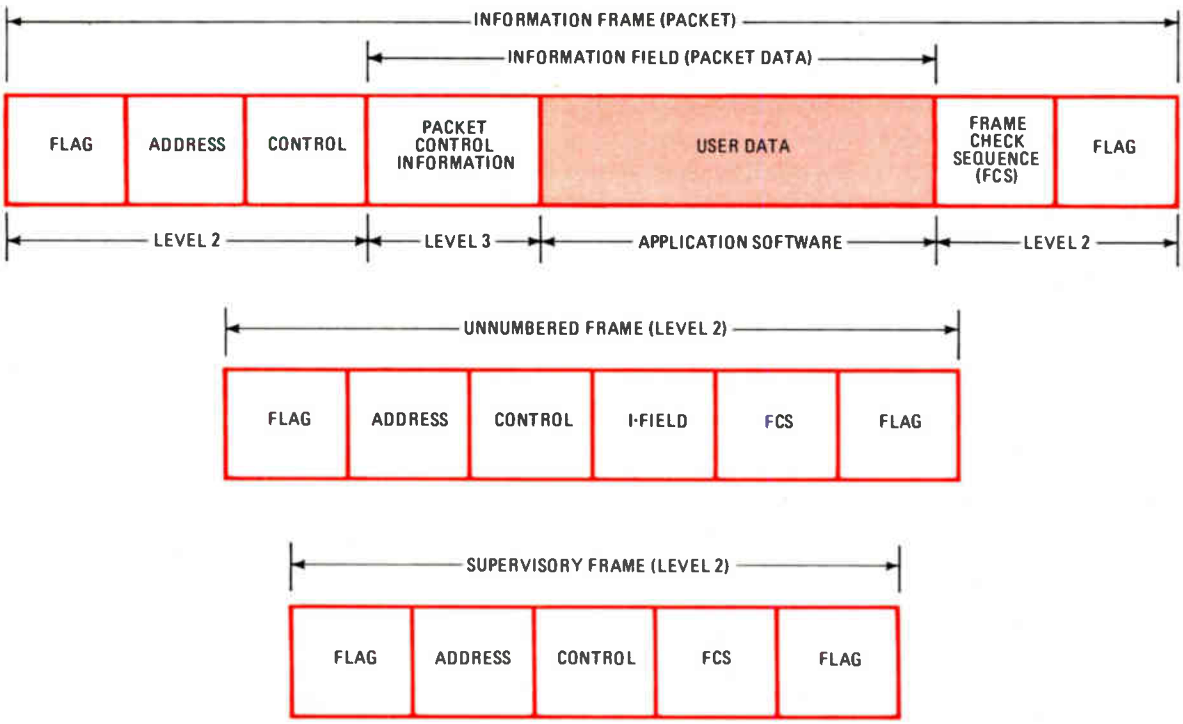
International interface standards are vital to the development and growth of packet-switching networks. Standards lead to lower costs for equipment bought by network users, since this equipment can be manufactured in much larger quantities. The user also benefits from the interchangeability of gear from different vendors. Manufacturers reap the rewards of a global market rather than a local one, and network organization is made vastly easier.

A number of U. S. and international standards organizations are working together to set up interface rules. The International Telecommunications Union (ITU), formed in 1865, operates under the auspices of the United Nations. Under the ITU is the Consultative Committee for International Telegraphy and Telegraphy (CCITT), which is primarily an organization of carriers.

Study Group VII is a CCITT organization that handles public data networks. SG VII is responsible for publishing a number of standards or recommendations for packet-switching networks. The best known of these is Recommendation X.25.

The International Standards Organization (ISO), which is composed of representatives from the manufacturing and user community, works closely with the CCITT; the ISO also has a group under its wing with responsibility for public data networks.

In the U. S., the American National Standards Institute (ANSI) is a clearinghouse that coordinates activity for voluntary standards. Its X3S37 committee, which has the responsibility for public data networks, does liaison work as well as coordination. This committee represents a cross section of U. S. industry: manufacturers, users, and carriers. It offers inputs to both the ISO and the CCITT.



4. Standard frames. Three types of data frames may be sent over a packet network. All data except the user data in the information field of an information frame is system overhead required for synchronization, data checking, verification, and bookkeeping functions.

01111110. The receiving station automatically deletes the inserted 0s from the data.

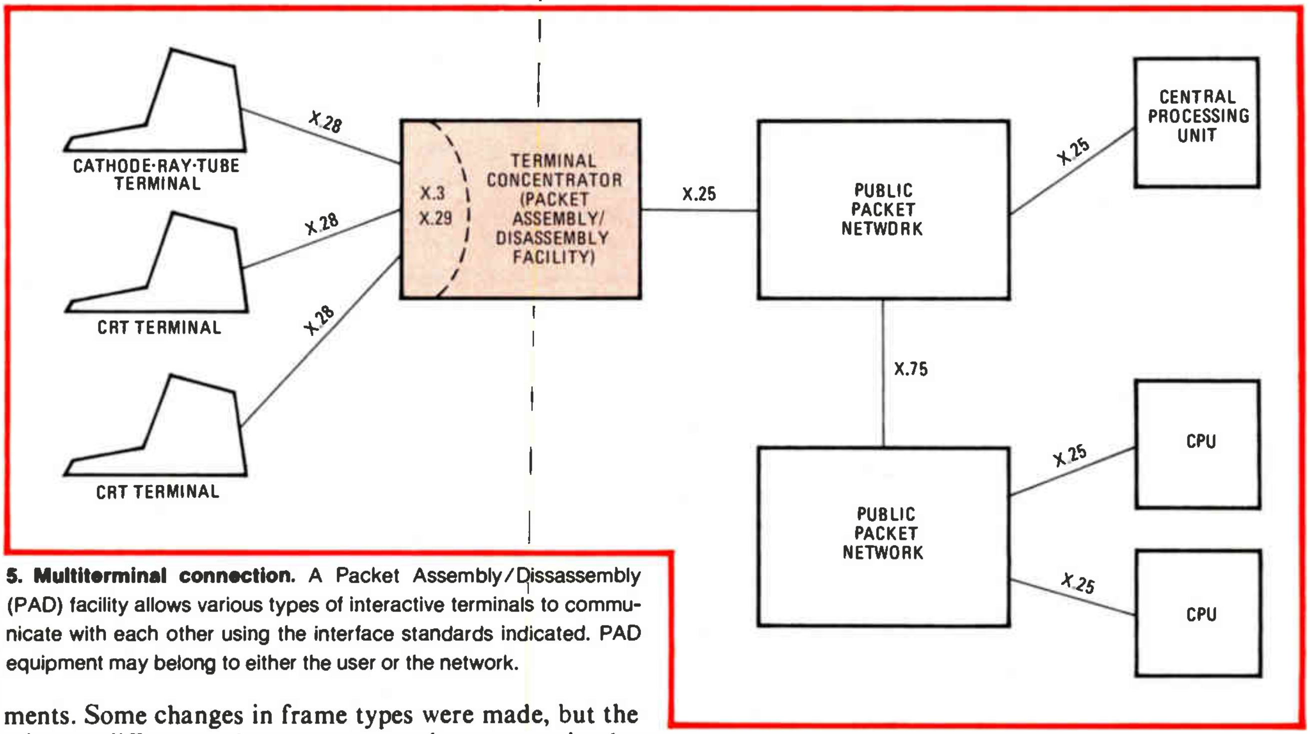
The frame-check sequence is the last 16 bits before the closing flag. They are produced by a calculation that checks all data between the opening flag and the first bit of the FCS. The logic 0s inserted for data transparency are not checked.

A frame may be one of three types (Fig. 4): a supervisory frame (or S frame), an unnumbered frame (or U frame), or an information frame (or I frame).

Level 2 control does not involve itself with the data within the information field of an information frame. It simply encloses the packet data in an HDLC frame and sends it out onto the network.

Supervisory frames are used to perform supervisory control of a link, such as acknowledging packets, requesting retransmission of packets, and requesting temporary suspension of transmission. Unnumbered frames are used to set up, disconnect, and reset links.

The Level 2 protocol may take one of two forms: Link-Access Procedure (LAP) and Link-Access Procedure, Balanced (LAPB). When it was originally written in 1976, Recommendation X.25 contained LAP only. LAPB has been added since that time, offering some improve-



5. Multiterminal connection. A Packet Assembly/Disassembly (PAD) facility allows various types of interactive terminals to communicate with each other using the interface standards indicated. PAD equipment may belong to either the user or the network.

ments. Some changes in frame types were made, but the primary differences between LAP and LAPB are in the functions that set up, disconnect, and reset links. (Two models of the μPAC, the WD 2501 and the WD 2511, are geared to the LAP and the LAPB, respectively.)

There are four system parameters defined by the X.25 Level 2 protocol: T1, N2, N1, and k. T1 is the time limit set for the primary timer; when T1 runs out, an unacknowledged command may be retransmitted. N2 is the limit set for a counter that is incremented each time a command is retransmitted because time T1 ran out without its being acknowledged. N1 is the maximum number of bits in a packet; it depends on the maximum length of the information field. And k is the maximum number of sequential packets that a terminal or node may have outstanding (transmitted but unacknowledged) at any given time. In the μPAC, T1, N2, and N1 are programmable. The number k can never exceed seven under X.25, and it is fixed at seven in the μPAC.

Multiplexing terminals

Since each user of the packet network typically has many different types of data generators and receivers, multiplexers must connect the network to the existing equipment. This multiplexer has been defined by the CCITT as the Packet Assembly/Disassembly (PAD) circuit (Fig. 5). The PAD is specifically for use with asynchronous terminals; it combines or separates the multiple signals that are sent to or received from the network.

CCITT protocol standards X.3, X.28, and X.29 are used together to define a PAD interface. A PAD facility may be viewed as a terminal concentrator that connects several asynchronous terminals to a single X.25 link. The PAD circuit is sometimes called an interactive-terminal interface because in practice most terminals connected to PAD interfaces require human interaction via keyboards and CRT displays or printing equipment.

When a PAD interface is used between the packet network and the terminals, two stations that are incompatible by themselves can communicate. They need only be able to talk to the PAD. The μPAC chips will allow them to do this. Another advantage of this approach is that new types of equipment added at a terminal are transparent to the network.

On the other hand, changes and improvements within the packet network are transparent to the user. These improvements could include increasing node-to-node communication speed, increasing the number of nodes, and changing node-to-node connections to fiber optics.

Variations on the theme

Many packet systems are available; they vary according to the network organization. Several networks, such as Montreal-based Bell Canada's Datapac, offer (in addition to the standard virtual circuit) a permanent virtual circuit that requires no call for link establishment and is continually available.

Another possible service, Datagram, when made available, will not require the initial establishment of a virtual circuit. In this approach a packet is merely put out on the line—typically by users of so-called transaction-based networks. There is no call procedure, and duration of connection is not of concern for billing purposes. Users may, for example, pay a flat fee. Short, independent data bursts will ultimately work their way through the network to their destinations.

A closed user group, available from Datapac and others, is like a private network. Users in a group, actually connected to a public network, can communicate with one another, but access is barred to and from all other users of the network. AT&T's proposed Advanced Communications Service includes this feature; the company calls it a virtual subnetwork. □

Part 2: LSI circuit simplifies packet-network connection

48-pin chip replaces entire board and thousands of lines of software

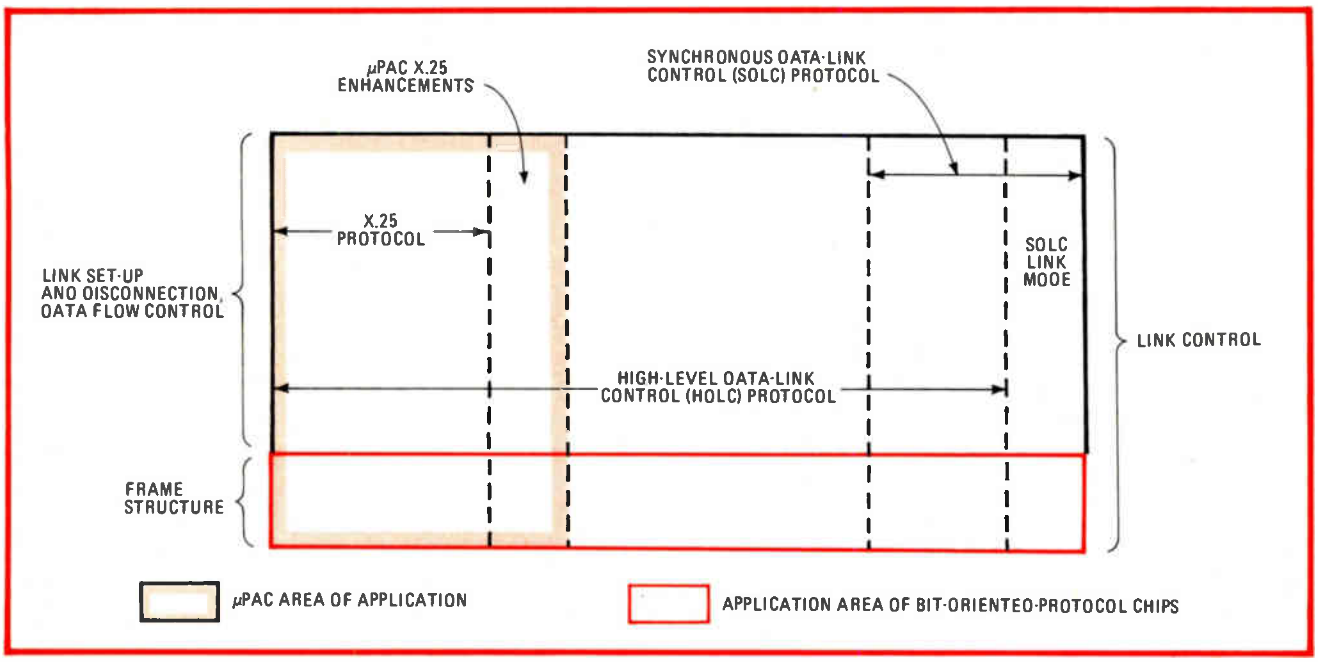
by Geary L. Leger, *Western Digital Corp., Newport Beach, Calif.*

☐ Packet-switching data-communications technology can now claim its first dedicated large-scale integrated circuit. Called the Micro Packet Network Interface chip, or μPAC for short, it is a complete X.25 Level 2 controller with on-chip bidirectional direct-memory-access facilities. This n-channel silicon-gate MOS chip in a 48-pin package replaces a board full of electronics.

The μPAC goes way beyond the functions performed by the bit-oriented-protocol (BOP) control chips currently in widespread use. It includes the circuitry of a BOP chip. But it handles many other operations, eliminating the need for separate DMA circuits and associated address latches, timing chips, and the system software (more than 1,000 lines of code) required until now to perform Level 2 control of the link between a data terminal and a node of a packet-switching network. It has an 11-K read-only memory and the equivalent of three microprocessors: one to handle data-transmission operations, another for dealing with received data, and a third central processor to coordinate all chip functions. Sample quantities of the controller will be available from Western Digital Corp. in the first quarter of 1980.

The data-link controllers already on the market (Western Digital 1933, Signetics 2652, Intel 8273, Zilog SIO, and others) handle BOP frame structure in a broad range of applications. For example, the WD 1933 can be used with the High-level Data Link Control (HDLC) and Synchronous Data-Link Control (SDLC) protocols, including the SDLC loop mode. This chip and others like it handle zero-bit insertion and deletion, the frame-check sequence (FCS), and the flags that define the beginning and end of a data frame.

The μPAC trades some of this protocol flexibility for the sake of greatly enhanced usefulness within its area of application (Fig. 1). It is restricted to the Level 2 packet-switching protocol defined in Recommendation X.25 from the Consultative Committee for International Telephony and Telegraphy (CCITT), a protocol developed from HDLC. But other BOP chips do not set up, disconnect, or reset the link; they do not automatically retransmit up to seven information frames (I frames); nor do they have a timer for retransmission control. These are



1. Targeted. The Micro Packet Interface (μPAC) chip is the first large-scale integrated circuit designed specifically for packet-switching applications. The application range of other chips that handle bit-oriented frame structure is wider, but the μPAC does much more in its area.

TABLE 1: COMPARISON OF FEATURES OF BIT-ORIENTED-PROTOCOL CHIPS

HDLC/ADCCP protocol feature	X.25 Level 2	Bit-oriented-protocol chips	μPAC
Basic bit-oriented frame structure	yes	yes	yes
Retransmission of up to 7 I frames (modulo 8)	yes	no	yes
Asynchronous response mode	yes, LAP	no	yes, 2501
Asynchronous balanced node	yes, LAPB	no	yes, 2511
Control of S, U frames	yes	no	yes
Link set-up, disconnect, and reset procedures	yes	no	yes
Time-out recovery	yes, T1/N2	no	yes, T1/N2
Multipoint operation	no	no	yes
Normal response mode (NRM)	no	no	no
Level 2 modulo 128	FS	no	no

FS = item for further study by the CCITT

all features of the μPAC chip (see Table 1).

Two versions of the μPAC will be made available. One, the WD 2501, uses the Link-Access Procedure (LAP) defined in the first version of X.25. The WD 2511 is for networks using the Link-Access Procedure, Balanced (LAPB) added to X.25 subsequently. The two chips differ only in the program stored in ROM. They are pin-compatible and interchangeable without hardware or software modifications. Both may be used either in a terminal (DTE, data-terminal equipment) or in a network node (DCE, data-circuit–terminating equipment).

Direct memory access

Because of the HDLC feature that allows up to seven packets (I frames) to be outstanding (transmitted but unacknowledged) at any time, the μPAC has information-field data (the I field of an information frame) buffered for up to eight packets both when transmitting and when receiving. In other words, the μPAC may have to retransmit up to seven packets. It must therefore be able to retrace its steps through as many as seven of its eight buffers.

DMA circuitry, included in the μPAC, is the best way to achieve this. A number of other control chips (floppy-disk controllers and data-link controllers) are DMA-compatible, but they do not actually include DMA. General-purpose microprocessors that have their own DMA, such as the Intel 8089, are not in the same category as the μPAC.

DMA control on the μPAC is simple, requiring only three pins ($\overline{\text{DRQW}}$, $\overline{\text{DROR}}$, and $\overline{\text{DACK}}$) for handshaking with the central processing unit's bus (Fig 2.). There are 16 address-output pins (A0 through A15) that are separate from the eight data pins (DAL0 through DAL7). This means that the DMA transfers are fast—they occur in a single cycle. Unlike the μPAC, DMA chips such as Western Digital's 1883 or Intel's 8257 require external address latches. This means that some or all of the address must come through the data bus and two or three cycles are required for data transfer.

In general, DMA control is either of the block-transfer type or the transparent type. In block-transfer DMA control, the DMA controller transfers several bytes of data while the CPU is disabled from using the bus. If transparent, the DMA control is imbedded in the CPU's clock cycle in such a way that the transfers are invisible, or transparent, to the CPU. Since the μPAC must be able to transmit and receive data on two DMA channels at once (for full-duplex operation), the only logical choice for the μPAC is transparent DMA, since block-transfer DMA would restrict operation to half-duplex.

All Level 2 data is appended and checked automatically by the μPAC. The I-field data is accessed via DMA channel. All supervisory frames (S frames) and unnumbered frames (U frames) are automatically transmitted and checked by the μPAC. The user's CPU operates only on the I field of I frames.

Keeping track of packets

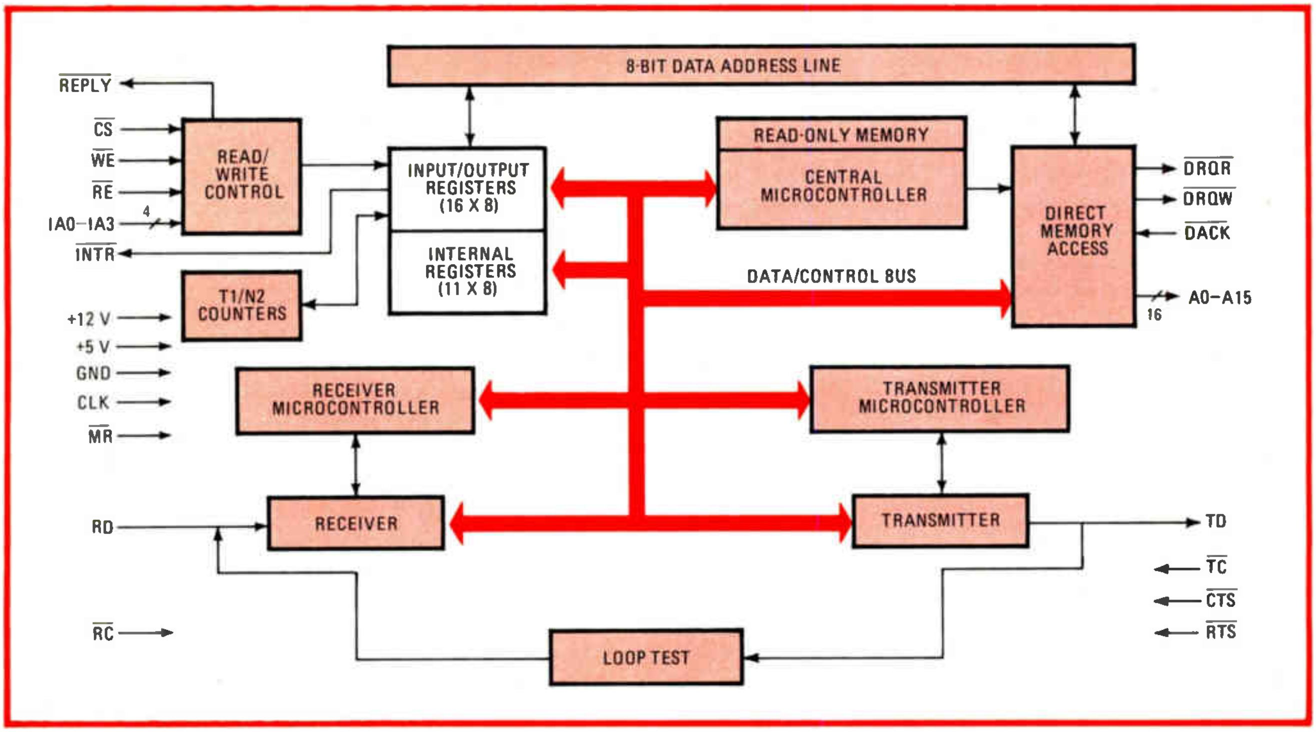
The DMA uses two lookup tables—one for transmitted frames (TLOOK) and another for received frames (RLOOK). These contain addresses and control bytes for the individual packets. Thus packet data is addressed indirectly. This method is best suited for most software applications.

The 16-bit starting address for TLOOK is loaded into the μPAC by the CPU. RLOOK must follow immediately, and both TLOOK and RLOOK are stored in random-access memory external to the μPAC.

There are a total of eight segmented control sections for each table. Each section contains 8 bytes, 4 of which are used for memory starting address and length. The rest are for control.

In the transmit mode, the μPAC reads (from TLOOK) the starting address and length of the first packet to be transmitted. The chip then automatically transmits the flag, address, and control fields. Next, the information-field data is transmitted using DMA and the memory location called "send #0 packet." At the end of the information field, the μPAC automatically sends the FCS and closing flag. It then moves on to the next packet.

If retransmission of one or more (up to seven) packets becomes necessary, the chip automatically retraces the previous transmissions through the TLOOK table. The user's CPU software does not become involved in the retransmission. An error counter is incremented.



2. Inside the μPAC. The Level 2 controller has its own timer and direct-memory-access circuitry and is the logical equivalent of three microprocessors. Routines stored on the chip allow it to relieve the network user's central processor of a large software overhead burden.

Each received frame is checked for correct address and FCS fields and for type of control field. If the frame is an I frame, the I field is placed in the assigned memory location using a method similar to that used in transmission. After the packet is received error-free and in proper sequence, an interrupt is generated and the μPAC is ready for the next packet, which will be placed in the next location.

Ten 8-bit error counters follow RLOOK in the external RAM. These counters do not cause an error interrupt, but maintain a running count of error activity. The contents of the counters include: the number of frames received with FCS error; the number of times T1 (the time minimum set for a timer that allows retransmission of an unacknowledged packet) ran out; and the number of packet retransmissions.

Control bits are included in TLOOK, RLOOK, and the μPAC to ensure orderly transfer of data blocks. For example, the control bits are designed to prevent what is known as "deadly embrace," a situation in which the μPAC and the user's computer are waiting for one another to start.

Self-testing

Self-testing features are critical to proper operation. The μPAC does a comparison test, an internal RAM register test, and a loop-back test. All three are suitable for use during manufacturing and inspection. The internal RAM and loop-back tests are also useful for system diagnostics and troubleshooting.

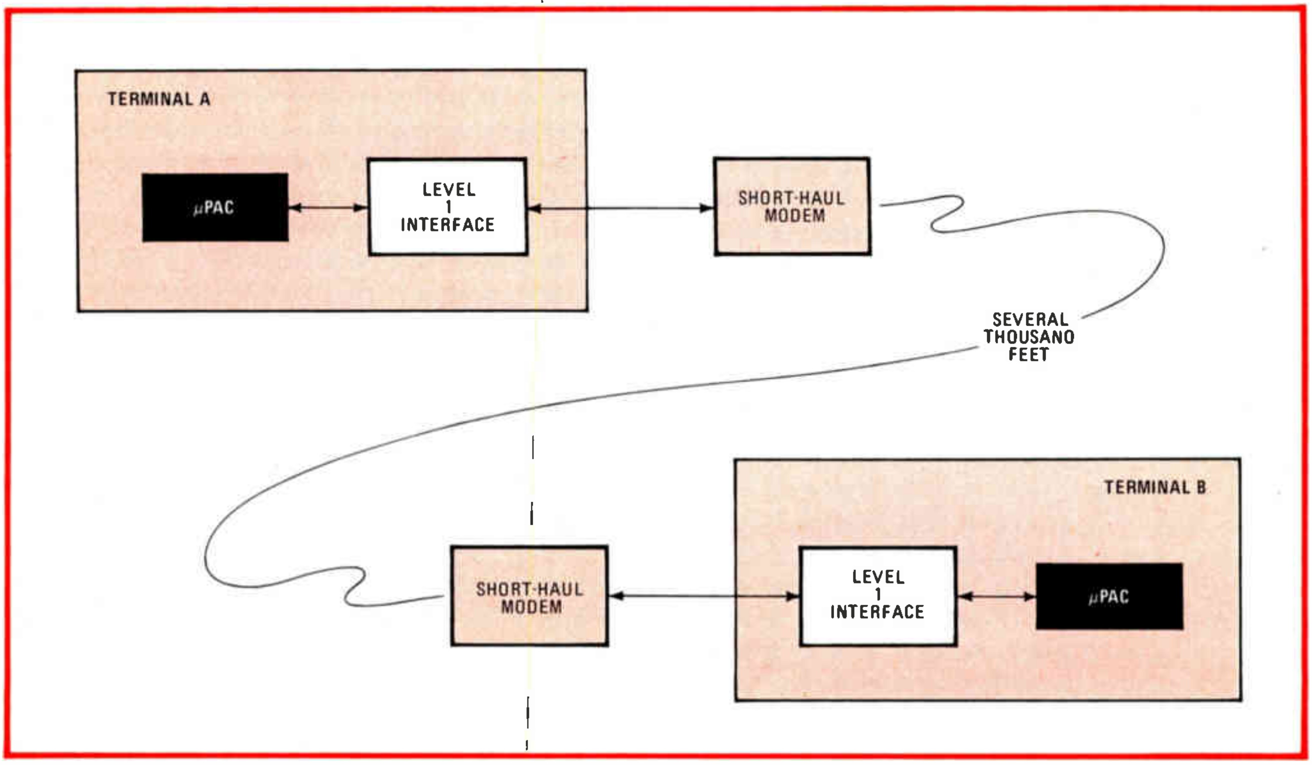
The comparison test requires a device known to be good or a stored list of known good responses. The program location counter (PLC) for the main ROM is halted so it may be incremented under external control.

TABLE 2: MICRO PACKET INTERFACE CHIP (μPAC) TERMINOLOGY	
ABM	asynchronous balanced mode
ARM	asynchronous response mode
CMDR	command reject (U frame, LAP only)
DISC	disconnect (U frame)
DM	disconnect mode (U frame, LAPB only)
FRMR	frame reject (U frame, LAPB only)
REJ	reject (S frame)
RNR	receiver not ready (S frame)
RR	receiver ready (S frame)
SABM	set asynchronous balanced mode (LAPB only)
SARM	set asynchronous response mode (LAP only)
UA	unnumbered acknowledgement (U frame)

All jumps stored in ROM are disabled so that each location of the PLC may be counted. As the PLC is incremented, the responses of the output pins and status registers are compared to the known good responses.

There are 11 8-bit registers in the μPAC that are not directly accessible by the user's CPU, which complicates testing somewhat. The internal RAM register test provides a means of checking these registers. The contents of register A are placed in six even internal registers and the contents of register B in five odd internal registers. The 11 registers are then added together without carry and the result is placed in status registers. This test is initiated by a control bit in the μPAC. The loop-back test is discussed later.

For the purposes of discussing link establishment procedures, it will be assumed that there is a 2501 μPAC at each end of the link. In practice, the 2501 can



3. Off the network. The μPAC is also useful in non-network applications that use bit-oriented protocols. It provides full-duplex capability, does error detection and recovery, and gives systems the option of hooking directly to a packet-switching network at some future date.

communicate with any device meeting X.25 Level 2 specifications.

When a link is set up, it is said to be in the information-transfer phase. This means that the terminal and node will accept and transmit I and S frames. When a link is logically disconnected, only U frames—DISC, SARM, or UA (disconnect, set asynchronous response mode, and unnumbered acknowledge; see Table 2)—will be accepted or transmitted.

Link supervision

A link-connect frame is not the same as a link-reset frame. A link in the information-transfer phase may be reset in one direction by a SARM transmission. A link is up after both ends send a SARM command and receive a UA response.

Since a SARM can be either a command to reset or set up a link, misinterpretation by the receiver of a SARM is possible. This could happen when a link is established if one end momentarily loses power. When that end tries to bring the link up by sending a SARM, the other end may interpret the command as a link-reset.

There are two ways to get around this problem. Suppose a terminal or node attempting to bring a link up sends a SARM command and receives a UA. After time T1, if the station does not receive SARM, it assumes that the other end considered the link up. It will then disconnect the link by sending DISC and receiving a UA, and attempt to set up a link a second time.

The other way around the problem is the method used by the 2501. The 2501 will always send DISC and receive a UA before attempting to bring the link up. This will assure a logically disconnected link so that it may attempt to set one up. Immediately after the link is up, the 2501 generates an interrupt.

It is possible to recover a single error on a packet with μPAC control. The error makes the received FCS bad, so B does not recognize A's first transmission of frame 1. When B receives frame 2, something is wrong since the last successfully received packet was frame 0. Thus, at the next opportunity, B sends a REJ (reject—an S frame) asking A to retransmit frame 1. This opportunity comes after B completes sending its frame 2.

When A receives the REJ frame, it is sending frame 3. There is no need to continue with frame 3, so A aborts transmission of frame 3 and goes back and retransmits frame 1. After retransmitting frame 1, A will retransmit frames 2 and 3. Finally, A will continue transmitting other frames.

Loop-back

A loop-back condition exists when a station receives the same serial information it has transmitted. In the loop-back test, the serial-transmit output is connected to the serial-receive input in order to test the transmitter and receiver channels. Each station has both primary and secondary functions, so there are two logical primary-to-secondary associations on a terminal-to-node link, and each association is identified by a different address field. This makes loop-back testing impossible when a strict X.25 connection is made. Commands will have the A field of a response and vice versa. One way around this is to make the A fields of the two associations equal for the duration of the loop-back test. (The A fields are programmable in the μPAC.)

Another problem with loop-back testing is the actual detection of the condition and the detection of the condition's removal. There is no simple way around this problem, and the µPAC gives only limited assistance.

First, detecting the existence of a loop-back condition is the responsibility of the CPU driving the µPAC. If the CPU sees that a link cannot be brought up, or if a link is up and suddenly has excessive link resets and CMDRs (command reject, a U frame), the CPU could assume the presence of a loop-back condition. After making the two A fields the same, if a disconnected link is successfully brought up, then the loop-back condition exists.

To detect the removal of this condition, a particular control bit (RRT1) in the µPAC may be used. It causes the µPAC to send an RR (receiver ready, an S frame) or an RNR (receiver not ready, also an S frame). These frames are sent at T1 intervals as long as the µPAC is not commanded to send a packet. As long as the µPAC receives those S frames, the loop-back condition exists. However, if the µPAC fails to receive an S frame for a time equal to T1 × N2, an interrupt is generated, signalling that the loop-back condition has been removed.

Modified X.25

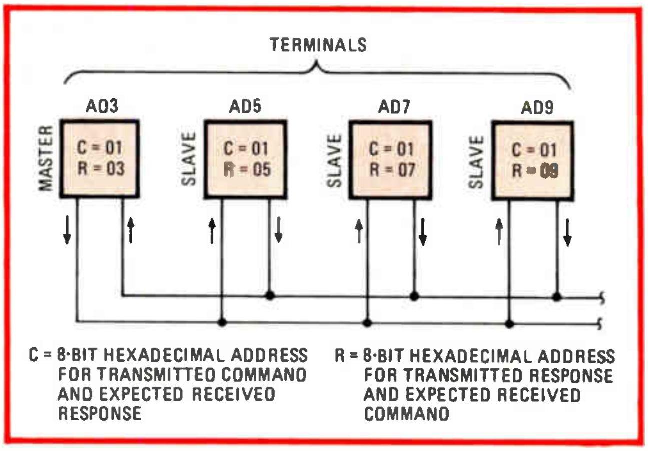
The original design intention was to use the µPAC in a strict X.25 terminal-to-node application, the only application covered by X.25. However, by taking advantage of the terminal-node symmetry of the µPAC (the fact that it can be used in both DTE and DCE), other applications are possible that use its built-in features.

For instance, the user does not need to develop the software for error recovery since this is a µPAC feature. For another, using a µPAC makes it possible to connect a non-packet terminal to an X.25 link at a future time. And lastly, the chip's protocol is bit-oriented. It has a number of advantages over older, character-oriented protocols, such as code transparency, full-duplex capability, flexibility, and modularity [*Electronics*, Jan. 18, 1979, p. 137].

One possible application is the connection of two terminals at Levels 1 and 2 (Fig. 3). How much of Level 3 is used would depend upon the individual application; the more of Level 3 used, the better standardized the interface is. One of the terminals in Fig. 3 could be a terminal concentrator (a Packet Assembly/Disassembly facility, or PAD, as defined by Recommendations X.3, X.28, and X.29) on a factory floor, and the other could be a host computer in a data-processing center.

Modified X.25 could also be used in a multipoint system (Fig. 4). Idle terminals in this type of system must transmit an "idle" sequence, not continuous flags. The terminal addresses (AD3, AD5, AD7, and so on) correspond to the transmitted response A field. The transmitted command A field is the same for all terminals and is chosen to be hexadecimal 01 in this case. All A fields are selected with odd values (least-significant bit transmitted first) to conform to the extended-address format of the Advanced Data-Communication Control Procedures (ADCCP).

Two terminals on the multipoint line may establish and discontinue communications by exercising X.25 procedures for setting up and disconnecting a link. But only two terminals can communicate at any one time.



4. Multipoint line. The programmed features of the µPAC chip enhance the flexibility of a system comprising one master terminal and up to 128 slave terminals. Hardware and software savings are possible when the µPAC is used in this off-network context.

Suppose that AD3 wishes to communicate with AD7. AD3 will first make sure that its receiving line is idle (a status bit in the µPAC). Next, AD3 will change its transmitted command and response A fields to be the reverse of AD7 (command field is set to 07, response field is set to 01). Then AD3 will initiate link establishment by setting a control bit, called "active," in the µPAC. Once the link has been established (the µPAC generates an interrupt when the link is first set up), AD3 and AD7 may exchange I frames. To discontinue the session, either AD3 or AD7 will set the mandatory-disconnect control bit in its µPAC. This will cause that terminal to initiate a logical-disconnect procedure.

Contention and roll-call methods

The multipoint system may be implemented by either contention or roll-call polling. In the roll-call method, the master terminal will initiate link establishment with one of the slave terminals, communicate with that slave, discontinue the session (disconnecting the link), and go on to the next slave. This process continues until all slaves are polled and then starts over. One advantage of the roll-call method is that the master has tight control over the line for efficient operation.

A disadvantage is that slaves must be queried (polled) before sending data, and the more slaves on the line, the longer it takes for the master to poll them. Therefore it is essential that each slave be designed to exchange a relatively small amount of data with the master in a single session, lest it tie up the line for long periods. Large amounts of data should be broken up and exchanged in more than one session. This method is suited to applications where the multipoint line has a high usage.

In the contention method, any terminal may initiate a session at any time. This is similar to a party telephone line and is suited to applications where line usage is low. All sessions are between the master and one of the slaves, but unlike the roll-call method, a slave may initiate the session. The terminal that initiates a session must send an I frame with its unique address immediately after the link is set up. □

Ramp generator has separate slope and frequency controls

by Henrique Sarmento Malvar
Department of Electrical Engineering, University of Brazilia, Brazil

Isolating with four analog switches the frequency-determining portion of the circuit from that controlling the charging and discharging of its RC integrator, this ramp generator achieves independent selection of slope ratio and repetition rate. Such a unit is useful in a music synthesizer, where timbre must be changed without affecting a note's fundamental frequency.

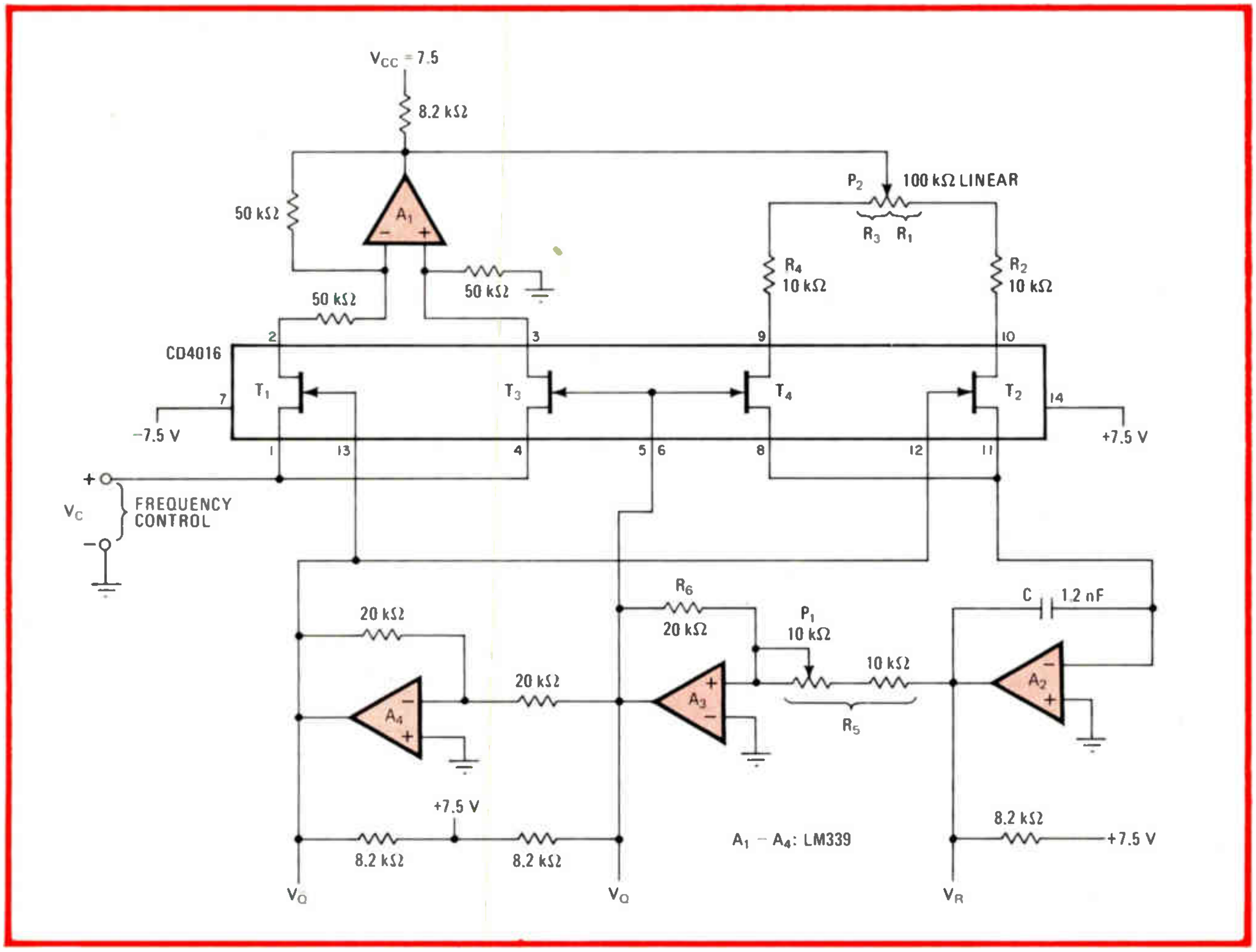
Analog gates T_1 and T_2 are initially switched on, and therefore V_c is applied via operational amplifier A_1 to the integrator built around A_2 (see figure). Thus, $-V_c$ appears at the inverting input of A_2, and its positive-going output reaches voltage V_H in $T_1 = 2V_HC(R_1+R_2)/V_c$ seconds, where $V_H = V_{cc}R_5/R_6$.

At this time, A_3 switches on and A_4 goes off. T_1 and T_2 are thus disabled, and T_3 and T_4 are brought high so that $+V_c$ is applied to the integrator. The output at A_2 thus falls linearly toward $-V_H$, where time $T_2 = 2V_HC(R_3+R_4)/V_c$.

The frequency of the ramp is given by:

$$f = 1/(T_1+T_2)$$
$$= R_6V_c/[2CR_5V_{cc}(R_1+R_2+R_3+R_4)] = kV_c$$

where k is a constant (in the approximate range of 1 kHz/V) that can be adjusted with potentiometer P_1. Because R_1+R_3 is a constant, it is seen that an adjustment in potentiometer P_2 will affect the slope ratio, but not the frequency. With the values shown, the slope ratio can be selected from 1/11 to 11. The slope ratio is given by $T_1/T_2 = (R_1+R_2)/(R_3+R_4)$. □



Separation. Transmission gates T_1–T_4 separate the portion of the ramp generator that determines the frequency from the circuitry that sets the charge and discharge times of its integrator, so that the up/down slope ratio and frequency can be independently selected. The inexpensive circuit, which costs less than \$10 and works in the audio range, is a useful timbre control in music synthesizers.

Eight-port counter handles coinciding input pulses

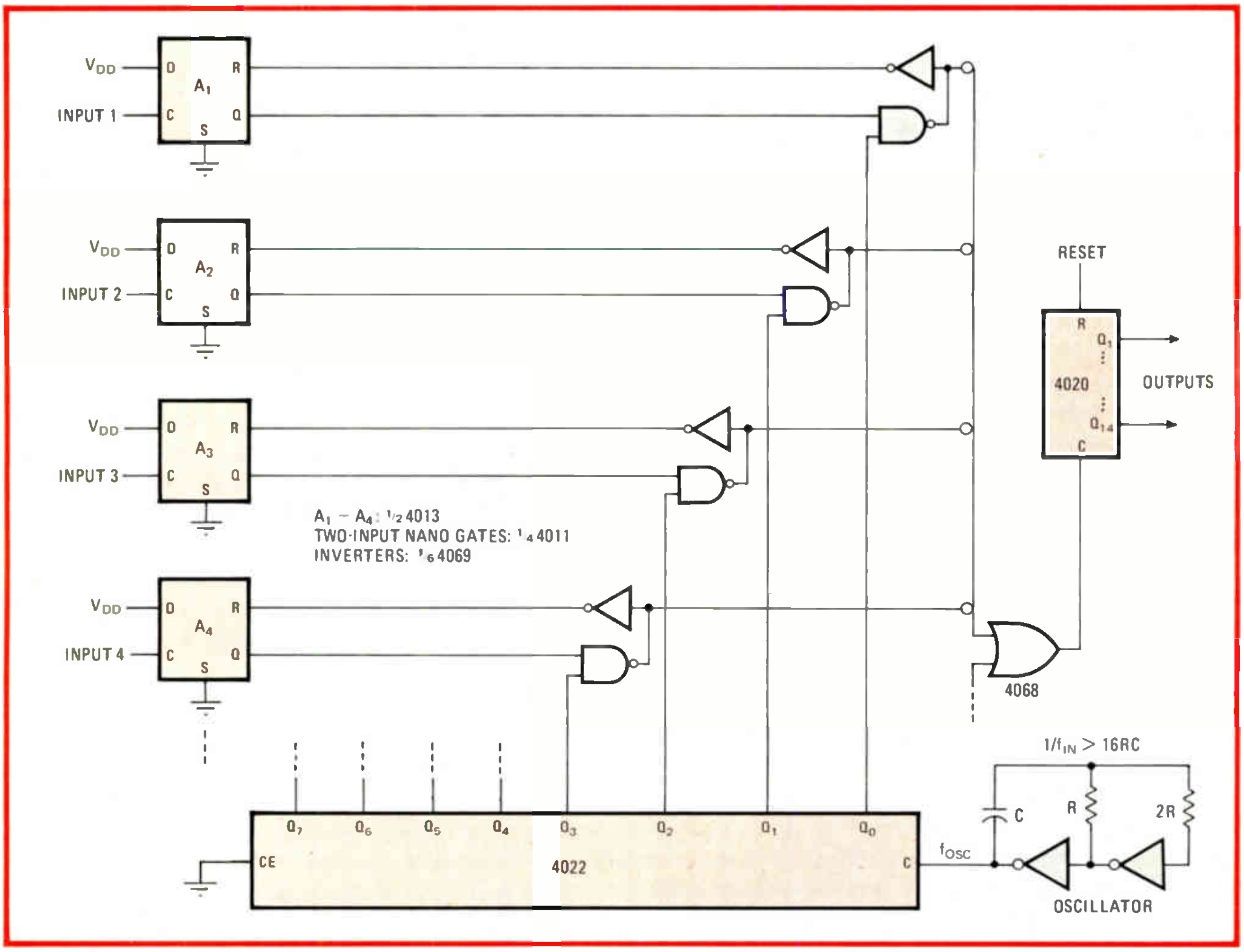
by Gary Steinbaugh
Owens/Corning Fiberglas Corp., Technical Center, Granville, Ohio

In applications where an asynchronous counter is driven by more than one input source, there is always the possibility that pulses will arrive simultaneously, causing an incorrect count. This circuit overcomes the problem by latching all input pulses as they occur and multiplexing the latch outputs so that the pulses may be applied to the counter one at a time.

As shown in the figure, four 4013 dual latches and their associated gates, in conjunction with a clocked 4022 Johnson counter, drive the 4020 ripple-carry binary device that is used to accumulate a count. (In the interests of space, the identical circuitry of A_5–A_8 and their gates is not shown.) One eight-input NAND gate, the 4068, is used to clock the 4020.

A_1–A_4 will latch on the rising edge of any pulse that appears at their respective inputs. The 4022, driven by an oscillator, scans the contents of each flip-flop; if the output of the flip-flop scanned is at logic 1, a pulse appears at the output of the 4068 and the 4020 is advanced. At the same time, the flip-flop is reset.

The counter may be configured for any number of inputs. Note that the frequency of the oscillator driving the Johnson counter must be high enough to permit each flip-flop to be reset before it is set by a following input pulse; otherwise, the event will not be recorded. For an n-input counter, $f_{in} < nf_{osc}$, where f_{in} is the highest input frequency expected (the reciprocal of the time between any two pulses at a given input) and f_{osc} is the frequency of the oscillator. □



Serial stepping. This multiplexer circuit avoids the difficulties associated with multi-input counters that are called upon to handle simultaneously occurring pulses. The clocked 4022 Johnson counter, driven by a simple RC oscillator, scans each flip-flop so that input pulses previously latched are applied one by one to 4020 accumulator. The counter can be easily configured for any number of inputs.

One-chip power amplifier controls dc motor's speed

by Kuang-Lu Lee and Dennis Monticelli
National Semiconductor Corp., Santa Clara, Calif.

Circuits for regulating the speed of small dc motors need not be expensive or complicated now that one-chip power operational amplifiers are available. In fact, using the power device (such as the LM13080) in a simple negative-feedback configuration provides better regulation than many speed controllers now on the market. In addition, common-mode rejection of power-supply transients is large.

As shown in (a), the circuit's reference voltage is established by D_2 and R_3 and filtered by R_5 and C_1. D_1 simply serves as a common-mode level shifter for the inputs of the op amp. Negative feedback around the op amp provides the contolled-voltage drive to the motor. Thus:

$$V_{motor} = (V_{D2} + I_m R_3)(R_2/R_1) + V_{D2}$$

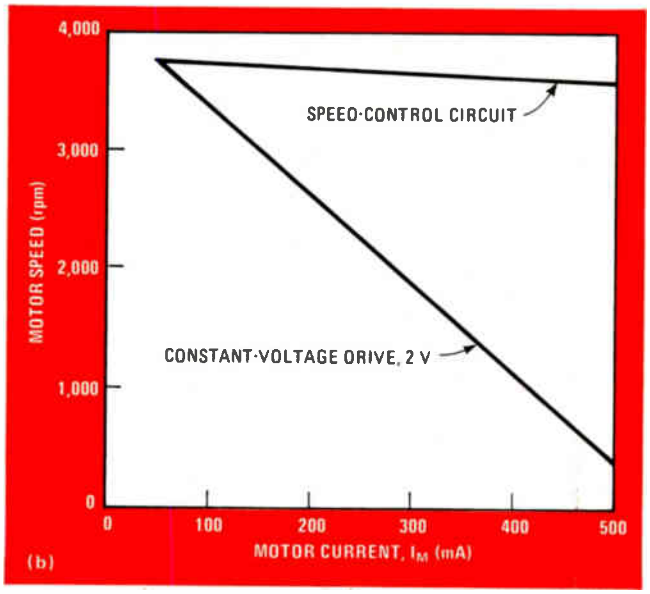
where V_{D2} is the forward voltage drop of diode D_2 and I_m is the current through the motor.

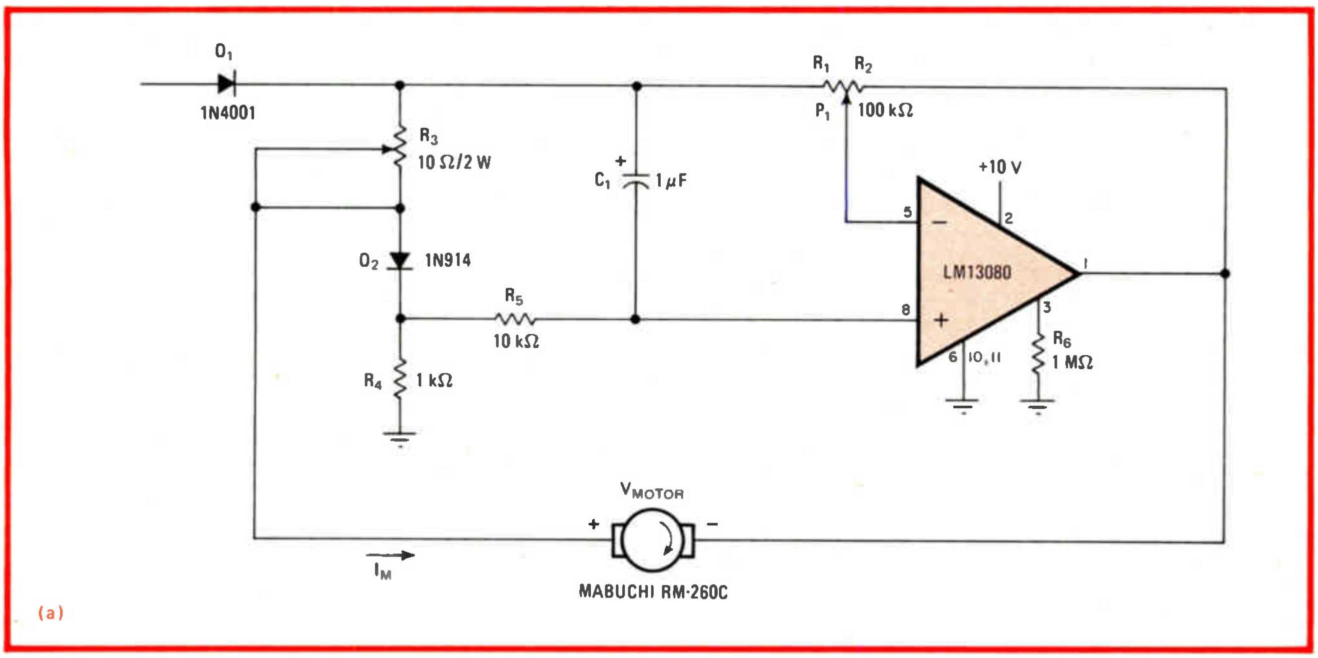
As the motor load increases, I_m increases, and this results in a corresponding increase in V_{motor}. To accommodate large changes in load, V_{motor} varies considerably. The amp therefore needs a 10-volt source voltage to provide sufficient swing, current, and power dissipation for most small motors. Powered by such a source, the LM13080 will handle up to 2 watts in free air and can deliver 0.5 ampere.

The optimum settings for potentiometers P_1 and R_3 are those that provide stable regulation. They are found empirically with the actual motor to be used. P_1 is first adjusted experimentally so that the motor will provide slightly fewer than the desired number of revolutions per minute. R_3 is then increased until a minimal loss in speed is observed for a substantial increase in motor load. Note that excessive positive feedback via R_3 will cause instability. Because the adjustments of P_1 and R_3 interact, it will be necessary to readjust both until the best settings are obtained.

The circuit's performance for a small motor is shown in (b). Note its superior performance with respect to a popular configuration that drives the motor from a constant-voltage source. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.





Speedy solution. One-chip power op-amp circuit (a) makes simple, low-cost speed control for small dc motors. Circuit affords excellent common-mode rejection. Controller's rpm-vs-load performance (b) is superior to that of circuits utilizing a constant-voltage drive.

Microcomputer software satisfies conflicting programming needs

Operating system lets support elements be added to develop a program, removed to run it with minimum memory

by James Isaak, *Data General Corp., Westboro, Mass.*

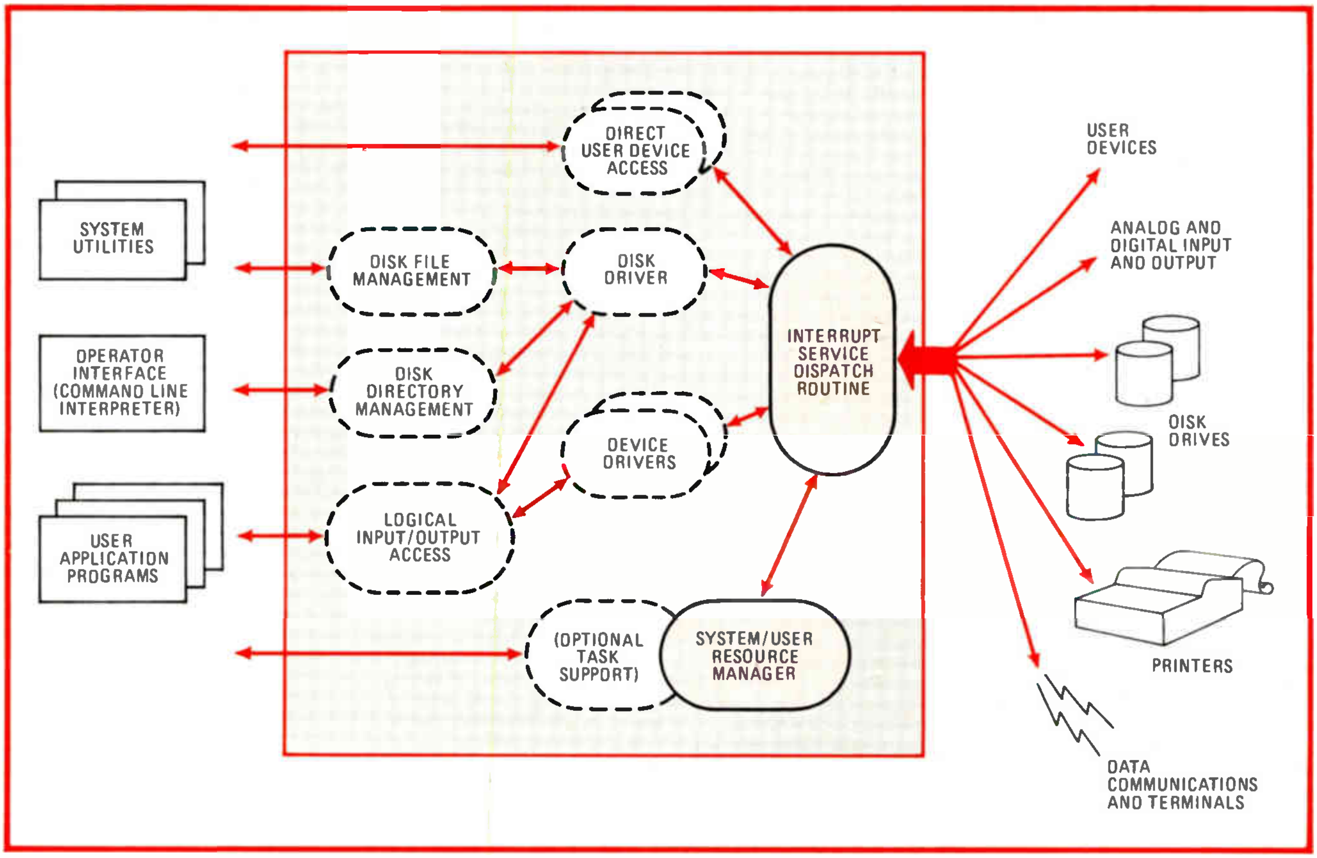
☐ Too short a lever on a fulcrum too far from the load guarantees inefficiency. Yet that has been the situation confronting microcomputer programmers.

True, they are beginning to obtain somewhat longer levers in the form of tools like compilers and utilities and high-level languages. But the fulcrum of their efforts to get a program off the ground—the operating system—has received far less attention, even though it is crucial to cost-effective programming.

MP/OS, an advanced operating system for the microNova microcomputer line, aims to lower software costs. It enables its user to develop a program and to run it as easily as an engineer breadboards a circuit and gets it into production.

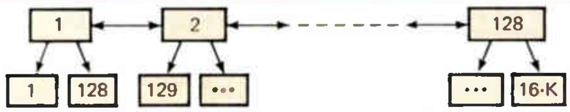
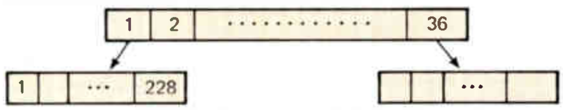
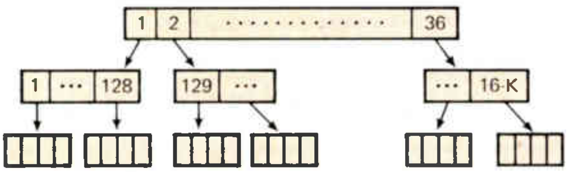
Earlier microcomputer operating systems failed at one or other of those tasks. The pared-down versions of minicomputer operating systems with which minicomputer manufacturers have endowed their microcomputers are still too bulky to run programs efficiently on a chip. On the other hand, the primitive systems that microcomputer manufacturers offer extend program development time expensively because of their very limited ability to coordinate management and system functions, to support languages and utilities, and to interact with a wide enough variety of peripheral devices.

MP/OS is designed specifically for 16-bit microcomputers and is suited for interactive program development as well as efficient run-time execution. It offers device-



1. Glue. The operating system (shaded) interfaces the user on the left with the hardware on the right. The utility programs circled with dashed lines are optional and may be eliminated for minimum overhead in run time. The dispatcher and resource managers ensure efficient operation.

TABLE 1: DISK FILE ORGANIZATION VERSUS SEEK TIME

File structure	Logical layout for 8-megabyte file	Random access (1/3 assumed)	Comments
Contiguous	 uses 16,384 (2^{14}) data blocks	1 seek maximum	• cannot be extended • must have full contiguous space to allocate
Linked list	 uses 16,384 data plus 250 pointer blocks	5,000 seeks, on average	• is not suitable for random access files • is easily extended
Linked list index	 uses 16,384 data plus 128 index blocks	42 seeks, on average	• was state of the art until about 1973 • is easily extended
Advanced file tree (large elements)	 uses large (228-block) segments plus 36 resident pointers	1 seek maximum	• has best possible access • allocates in large (114-kilobyte) segments
Advanced file tree (small elements)	 uses 16,384 4-block elements plus 36 resident pointers	2 seeks maximum (1 is possible)	• costs 1 seek • allocates easily since 2-kilobyte element is just 4 disk blocks • can be extended, with little or no impact on seek

(assumes 512-byte disk blocks, with 128 pointers in an index block)

independent input/output, interrupt- and/or priority-driven multitasking, complete facilities for memory- and file-management, field-tested and time-proven utilities, and extensive language support. Such a flexible and versatile operating system relieves programmers of concern for hardware idiosyncracies, allowing them to concentrate on developing the applications software.

Modular and orthogonal

It is important that development software and application programs execute on the same machine. Otherwise, a lot of time may be wasted on programming around the discrepancies of different systems (often with incompatible hardware) or different operating systems or both. The keys to operating system compatibility with both the developmental and application environments are modular construction and orthogonal design.

Modularity gives the user a few well-chosen building blocks that can be combined to yield more complex functions without adversely affecting the rest of the system (Fig. 1). Orthogonal, which literally means "at right angles," refers to the independence of modules within the system. Just as a room may match any width with any length, an orthogonal system lets users select features in one dimension, such as disk management, independently of another dimension, like task management. Thanks to these capabilities, the software and hardware can be expanded for program development and then cut back at run time to minimize memory requirements in the final product.

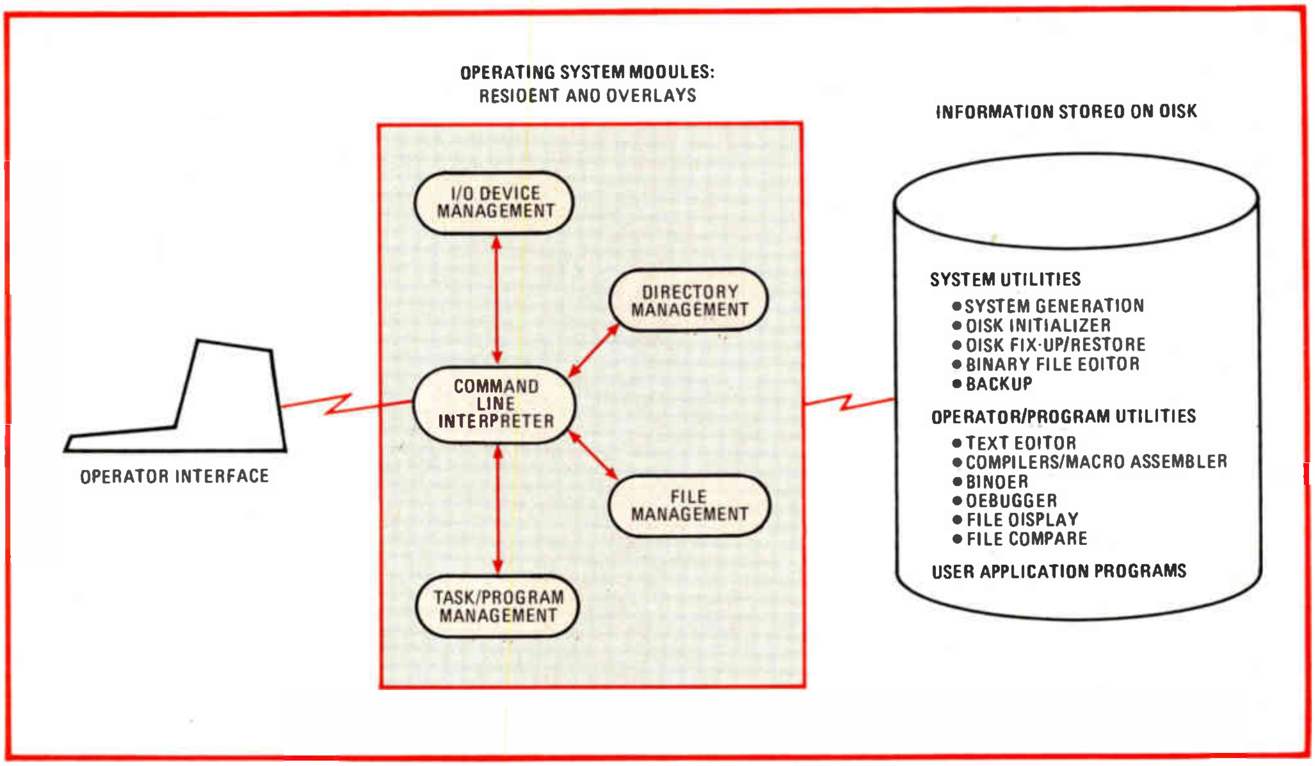
Stated differently, the MP/OS system lets the user remove unnecessary overhead function by function. For example, peripheral device drivers—the software that translates a user's read or write request into the input/output instructions needed to "drive" the device—can be modularly added to or removed from MP/OS without system modification. Similarly, if a user needs to read and write only bytes and not entire lines, the overhead associated with MP/OS's line-buffering feature can be removed to trim the system for run time. In short, the orthogonality of task and file management makes it easier to adapt a microcomputer application program to the two different hardware environments.

MP/OS manages I/O data transfers between a program and a device or file at a high level. Each file and device is assigned a symbolic name, and all data is buffered by the operating system to isolate the user from the hardware differences between different devices. Devices built by the user may be incorporated into the system by using the IDEF command (which defines an interrupt-handling routine for the device) and then by adding the appropriate device driver.

The IDEF command

The IDEF command introduces the device to the system and initializes it, while the remove-interrupt (IRMV) command releases it from the system. In this way, the programmer easily can add or delete devices during program development or at run time without modifying the operating system.

MP/OS accommodates peripheral devices whether or not they have directory structures. Directories contain names and other identifying information about files on disk, thus providing a technique for grouping disk files in



2. Console link. The command-line interpreter is an interactive operator interface. It is the principal key to easy development of application programs because it can directly access files, input/output devices, directories, and program management facilities.

a logical organization consistent with the program.

MP/OS also recognizes selected control characters from the terminal for editing and interrupt functions. For instance:

- Control D provides end of file.
- Control S suspends output to console.
- Control Q resumes output to console.
- Control U erases current command line.
- Control C followed by control A interrupts a program.
- Control C followed by control B aborts a program.
- Control C followed by control E aborts the program and saves memory image on disk.
- RUBOUT erases the last character to be typed.

Communication with peripheral devices takes place over any of 16 system-defined I/O channels or data paths, 2 of which are initialized for console I/O. Transfers can be in direct block form, or else they can be either dynamic or data-sensitive. Dynamic transfers enable the user to read or write any specified number of bytes from or to any file with a single system call. Data-sensitive I/O terminates on predefined characters (such as that for a new line) and is therefore ideal for text processing.

Multitasking

Primitive operating systems handle each program task sequentially, which is adequate for batch processing in a stand-alone environment. But interactive data collection, real-time data processing, process control, and instrumentation applications all require asynchronous multitasking. The operating system must be able to manage multiple interrupts yet also be able to continue executing the original program.

Up to 256 tasks can be active at a given time with the MP/OS system. They may be created or deleted at run time, and each has a priority used to determine the order in which the central processor is assigned to it. A scheduling routine switches control from task to task to create the appearance of parallel processing. However, the user can at will disable multitasking to ensure that a critical operation is not interrupted by other tasks.

Program management

A stack structure is used for program management. Any program may invoke another program. As control is passed to descendant programs, the state of the parent program is saved on disk so that control can later be returned to it. The status of I/O channels is also passed to descendant programs, and messages may be passed between programs.

I/O calls from tasks may or may not be pended. A task using a pended call stops until the I/O operation is complete. With an unpended call, however, the task continues executing.

General-purpose program development and the stand-alone run-time environment have markedly different memory requirements, and an advanced microcomputer operating system must be able to accommodate both. Whereas program development demands the flexibility afforded by ample random-access memory, not to mention a wide variety of peripheral devices, dedicated run-time applications typically require the efficiency of read-only memory and minimal or no utilization of magnetic-disk storage.

Advanced operating systems like MP/OS have the ability to separate "pure"code and data, which must remain unaltered, from "impure," which must be modified at run time. The MP/OS compilers and assemblers have separate designations for the two categories of data, and a binder program locates the constant data in a pure storage area and the dynamic data in an impure area. Other duties of the binder utility are: to assign memory areas to object modules and locate the data within them; to keep track of data and routine linkages; and to select the required system and language run-time modules from the libraries.

Better reliability

Having its memory organized into pure and impure storage improves the reliability of the MP/OS system, for it can check out the constant data by performing checksums on it to detect any hardware or software failures that violate the integrity of the system. MP/OS also catches attempts to loop at location zero, an error that is difficult for programmers to detect without the old-fashioned light-and-switch panel not found on many microcomputer systems.

In order to reduce memory requirements, the MP/OS system provides an overlay technique. This procedure involves storing seldom used program code on disk until the time it is needed. The overlays are managed by a combination of language directives, binder options, and library routines.

MP/OS's high-level management of I/O data transfers is made possible by a hierarchy of files that simplifies data retrieval and the organization of data on disk. Primitive operating systems use linked lists or require the user to preallocate disk space for each file. Linked lists consist of pieces of data, often physical disk blocks, each containing the address of the next piece. These structures are inefficient for accessing data randomly; for example, to access disk block 25, the user must read the previous 24 blocks. But the MP/OS system employs file indexes and dynamically allocates or deallocates file space as needed.

MP/OS files are grouped into directories for ease of use and protection. Any file in a directory may itself be a directory containing more files, resulting in a theoretically infinite nesting of subdirectories.

A file consists of elements ranging in size from 512 bytes to 16 megabytes, and the system maintains a set of pointers to them. The file elements occupy contiguous blocks on the disk. The larger the file elements, the greater the efficiency with which the disk data can be accessed, since the disk heads need not be continuously moved around to find the proper data. On the other hand, the smaller the file elements, the more freely can disk blocks be allocated.

For a file contained within 32 elements, access to any area within it requires just one seek operation. But additional levels of indexing are possible, allowing the use of larger files or smaller elements or both to meet the needs of the application.

Since many applications are disk-bound, being dependent upon the speed of disk transfers, the number of seeks required to access a given piece of data is critical. The combination of variable-size file elements and multiple index levels in MP/OS makes it possible to access any piece of data within a 512-megabyte file in a single seek. In fact, accessing of up to 2^{11} megabytes takes three seeks at most, using minimal element sizes. In comparison, accesses to a 10-megabyte file using a linked-list index scheme would take an expected 20 to 40 seeks (see Table 1).

The indexed directory approach to file management also contributes to overall system reliability. MP/OS can rebuild the entire directory structure in the event of some hardware or software failure. This is done through a disk fix-up program, able to identify the files on disk and reconstruct all the index structures. The same program also detects errors by performing checksums on key disk structures and uses duplicate structures to recover and continue operations. The resultant fault tolerance improves the reliability of application programs.

TABLE 2: EXAMPLES OF THE COMMAND LINE INTERPRETER

Development	Macroinstruction
)XEQ EDIT PROGRAM	EXECUTE EDIT %1%
)X PASCAL PROGRAM	EXECUTE PASCAL %1%
)X BIND/DEBUG PROGRAM	EXECUTE BIND/DEBUG %1%
) DEBUG PROGRAM	DEBUG %1%

XEQ and X are accepted CLI abbreviations for EXECUTE

Utility and language support

Without utility and language support, however, many of the gains made by the operating system would be lost. As a minimum, an advanced microcomputer operating system should provide the following utilities: a symbolic debugger to assist in the repair of multitasking applications; an interactive text editor that can manage display screens as well as hard-copy units; and miscellaneous utilities for comparing files, displaying data in numerical formats, and moving data from one disk or diskette to another for backup and system management.

Perhaps the most important utility is the one that interfaces the programmer with the system. MP/OS's command-line interpreter is an interactive, easy-to-use console interface (Fig. 2). It has a straightforward, English-language, free format, unlike the hard-to-grasp job-control languages used with some systems. It will accept single-word requests for information (like "help") and even acts on any unambiguous abbreviation ("H"). It can also handle macroinstructions for standardizing repetitive operating sequences and reducing errors.

As for programming languages, Pascal is easier to learn and use than most, and programs in it run more reliably and are easier to debug and maintain. The MP/OS system supports extended versions of both Pascal and Fortran, as well as a powerful macro assembler language that can accept any set of mnemonics and generate binary code that will run on any target machine (see Table 2).

With the right utilities and languages, advanced microcomputer operating systems clearly offer the leverage to improve programming productivity and help to bring software costs under control. □

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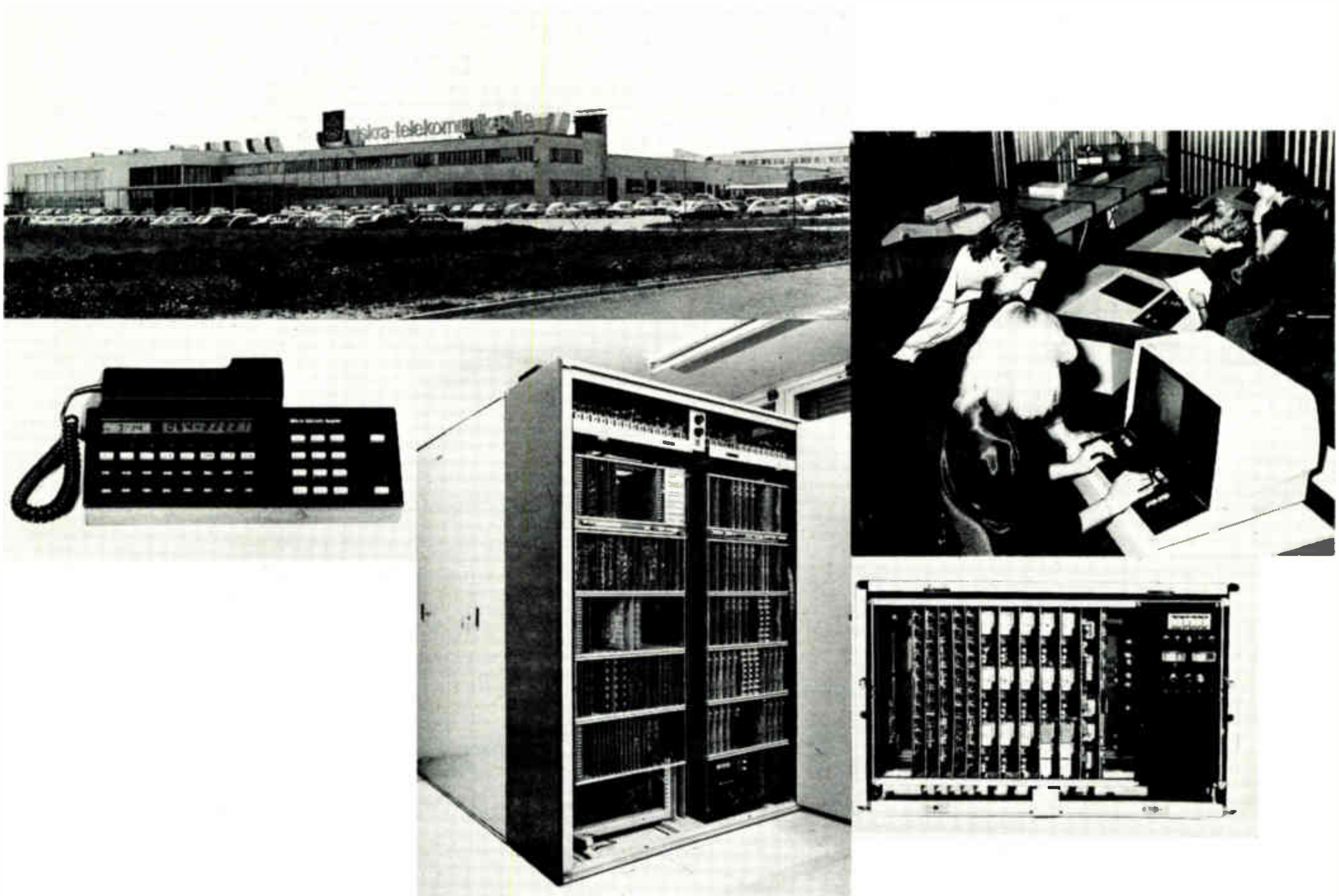

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Packing a signal processor onto a single digital board

8-, 12-, or 16-bit multiplier-accumulator chip computes filter functions, Fourier transform in real time for microprocessor-based systems

by Louis Schirm IV, *TRW Inc., TRW LSI Products, Redondo Beach, Calif.*

☐ Thanks to large-scale integration, real-time signal processing by digital means has become cost-effective. All the high-speed number crunching needed to compute a fast Fourier transform (FFT) or digital filter algorithm may be delegated to single-chip multiplier-accumulator (MAC) components. Functions that just a few years ago were exclusive to $50,000 array processors occupying 3 or 4 feet of rack space are today being carried out on 50 square inches of printed-circuit board for a cost of around $800.

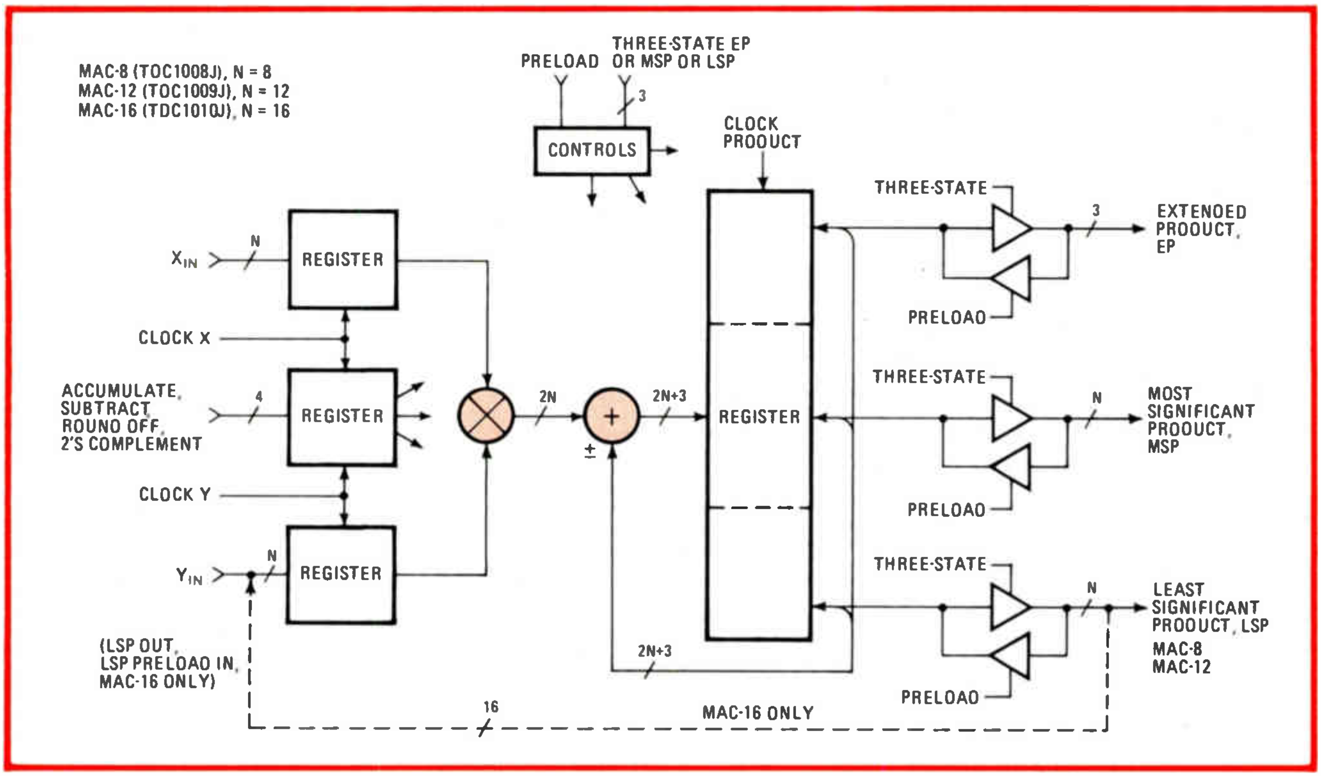
MAC-8, MAC-12, and MAC-16 are informal ways of designating the TDC1008J, TDC1009J, and TDC1010J and their handling of 8-, 12-, and 16-bit words, respectively (Fig. 1). Being specialized devices, they carry out the myriad multiplications and additions of an FFT very much faster than even a bit-slice microprocessor. Their big breakthrough is a multiplier that operates as fast as their double-precision adder-subtracter.

Not so long ago, the multiplier was the signal-processor designer's thorniest problem. It was bigger, slower, and costlier than the adder, and the arithmetic unit they made up was in turn the largest and most expensive part of the signal processor, followed by memory and control hardware in descending order.

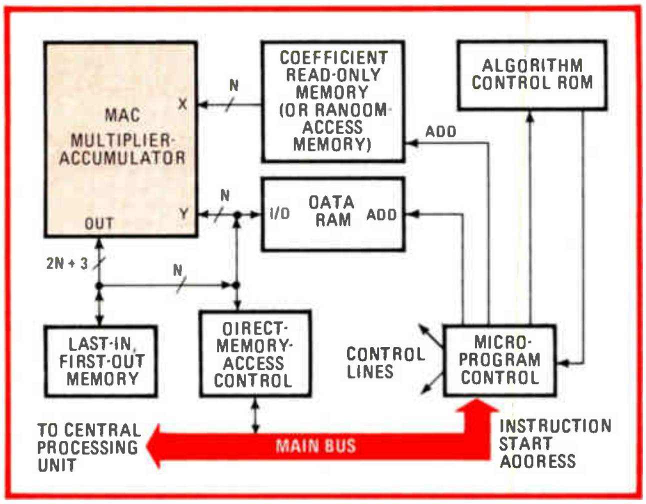
Then and now

A favorite solution was to tinker with the algorithm. The number of multiplications (and hence the size of the multiplier) could often be reduced by increasing the number of additions, among other things. But the side effects were unfortunate—system performance was compromised, and system data control became more complicated.

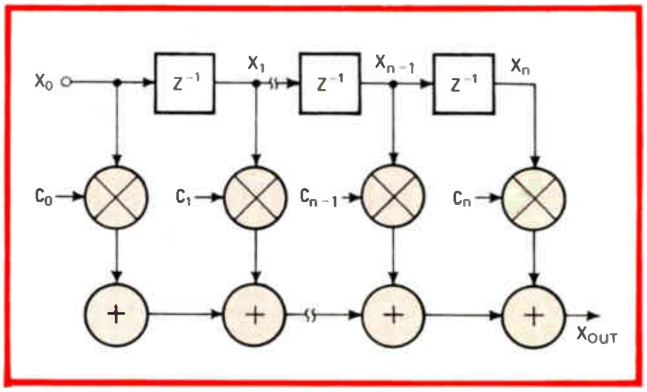
The MACs have upended this situation. They are now



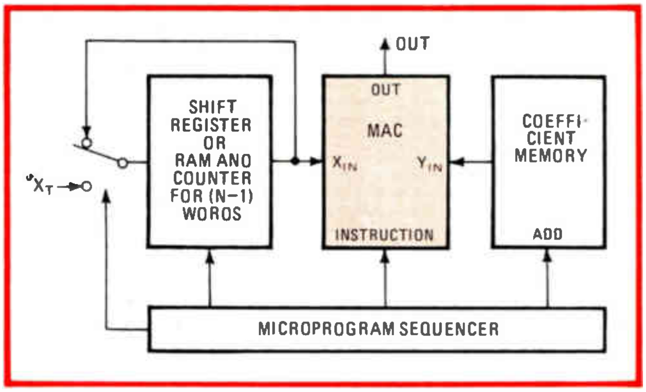
1. Number crunchers. New multiplier-accumulator integrated circuits are now available to do far more number crunching on a chip than previously possible from racks full of equipment. The basic logic diagram for TRW's 8-, 12-, and 16-bit MAC units is shown.



2. Signal processor. A MAC chip can be used with a few other chips to build a small signal processor. Here, an external microprocessor acts as the system controller, sending only macro-instructions and memory block locations to the signal processor section.



3. Canonical form. A nonrecursive, or finite-impulse-response, digital filter has a regular structure, is easily understood, requires simple control hardware, and has minimal internal-word growth. Its canonical form can be shown as a number of mathematical operations.



4. Filter hardware. A nonrecursive, or finite-impulse-response, digital filter can be implemented with a MAC and few additional ICs. The representative hardware shown is for a single-channel filter whose sequence of calculations is illustrated in Table 1.

the smallest and least expensive parts, followed by memory and control hardware. It no longer makes sense to use a more complicated algorithm than necessary, and in fact, the simple canonical algorithms are beginning to be attractive. In some applications, for example, the discrete Fourier transform is being preferred to the FFT because the MACs are fast enough to process the greater number of multiplications and additions involved in the time available. The payoff is reduced control hardware.

A MAC and a micro—the ideal match

The MAC-8, MAC-12, and MAC-16 are being used to upgrade the real-time capability of microprocessor systems. The microprocessor is left to perform the tasks it is more efficient at—memory management (getting data into and answers out of the MAC) and control. The MAC, on the other hand, does the number-crunching operations on the data, at speeds a hundred times faster than possible with the microprocessor.

Even memory management tasks are sometimes too time-consuming for the microprocessor central processing unit, necessitating the use of a separate high-speed memory-address generator and a direct-memory-address controller. This arrangement leaves the microprocessor with just the job of system controller, sending only macro-instructions and memory-block locations to the signal-processing section.

A signal-processing circuit that assumes such a system organization is shown in Fig. 2. It can perform real-time FFTs, vector or array multiplications, and digital filtering functions, to name a few. (The read-only memories shown could be replaced by random-access memories, but at the cost of extra system hardware and software.)

For a minimal-hardware signal processor, the various memories, the microprogram control section, and the DMA controller can all be done away with. The tradeoff is a tying up of the system's data bus and CPU and hence decreased MAC utilization. Even so, a system with a MAC operates much faster than if the CPU were used by itself.

In operation, the CPU of Fig. 2 uses the DMA controller to transfer a block of data from main memory to the signal-processor circuit. The CPU also sends a macro-instruction word and block-start address (for multichannel applications) to the microprogram-controller/address generator, and the signal processor begins operating. The CPU at this point is free to perform other management functions.

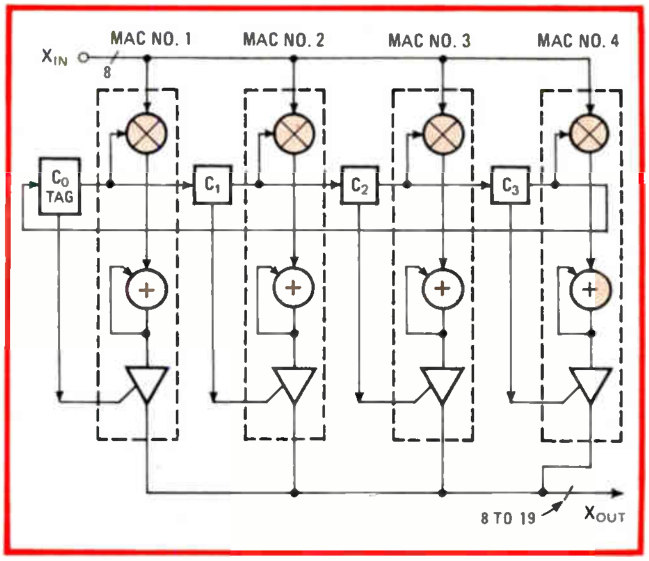
Should a signal-processing task with a higher priority arise, the CPU can halt the signal processor and load the 2N + 3 bits of data from the MAC into a last-in, first-out memory, either in a single step or in three cycles, depending on how wide the LIFO memory is. At this point, the signal processor is loaded with data from the main memory via the DMA controller to perform the higher-priority task at a new memory page. When the new task is completed, the LIFO memory pushes out the previous partial answer and the signal processor picks up where it left off before it was interrupted by the CPU.

There are many signal-processing algorithms that are nothing more than a string of sums of products, such as finite-impulse-response filters. All that is needed is for the microprogram controller to send a series of coefficients and data words into the MAC and read out the answers once the MAC has exercised its number-crunching expertise.

Note the single-port RAM of Fig. 2. Such a RAM is

Step	Inputs to the MAC: Data	Accumulate	Round off	Outputs from the MAC	Input/output operations
1	X_n, C_n	0	1	–	Load X_T into memory
2	X_{n-1}, C_{n-1}	1	0	–	
3	X_{n-2}, C_{n-2}	1	0	$X_n \cdot C_n = P_1$	
4	X_{n-3}, C_{n-3}	1	0	$X_{n-1} \cdot C_{n-1} + P_1 = P_2$	
⋮	⋮	⋮	⋮	⋮	⋮
n	X_0, C_0	1	0	$X_2 \cdot C_2 + P_{n-3} = P_{n-2}$	
n+1	–			$X_1 \cdot C_1 + P_{n-2} = P_{n-1}$	
n+2	–			$X_0 \cdot C_0 + P_{n-1} = P_n$	Read single-precision rounded answer from most-significant-product output of MAC
		(note: SUB = 0)			

TABLE 1: NONRECURSIVE (FIR) FILTER CALCULATION SEQUENCE



5. Pipelining. A series of MACs can be multiplexed in a pipelined fashion for the hardware implementation of a high-speed nonrecursive digital filter. Each of the MACs in this circuit starts and finishes the algorithm in use at a different time from the other MACs.

preferred to a two-port (separate input and output) device for two reasons. First, most single-port RAMs have a wider word—that is, they are configured as 1,024 by 4 bits or 2,048 by 8—so that fewer memory chips need be used. Second, it may be assumed that a memory read cycle takes about as long as a memory write cycle, so that very little time would be saved by going to a two-port RAM since the same two read and write memory cycles would be required in either case.

The microprogram controller of Fig. 2 is physically the largest section of the signal processor. Typically it must not only sequence rapidly through the system's software, including branch instructions, but must also calculate the addresses of data and coefficients. Its size therefore depends on how much flexibility it has.

The circuit of Fig. 2 can be configured in several ways, each with its own hardware and software tradeoffs. No single design has yet emerged that is clearly superior to the rest. The basic choices are: optimally configured counter, shift-register, RAM, and ROM ICs; a microcontroller chip for the software program and one or two for generating the data addresses in memory; a multiport bit-slice microprocessor like the Texas Instruments 74S481; and some combination of the previous three.

Implementing filters digitally

For purposes of digital signal processing, digital filters can be characterized as performing functions that have a number of delay elements and require several multiplications and additions. The MACs are optimally configured for these kinds of problems.

Most digital filters are either finite- or infinite-impulse-response types. The FIR filters, also called nonrecursive, exhibit only feedforward terms in their algorithms, in such numbers that they require a lot of memory. The IIR filters, also called recursive, have feedback as well as feedforward terms. Less popular, and so omitted from this discussion, are wave or lattice filters, which have lengthy, interconnected feedforward and feedback terms.

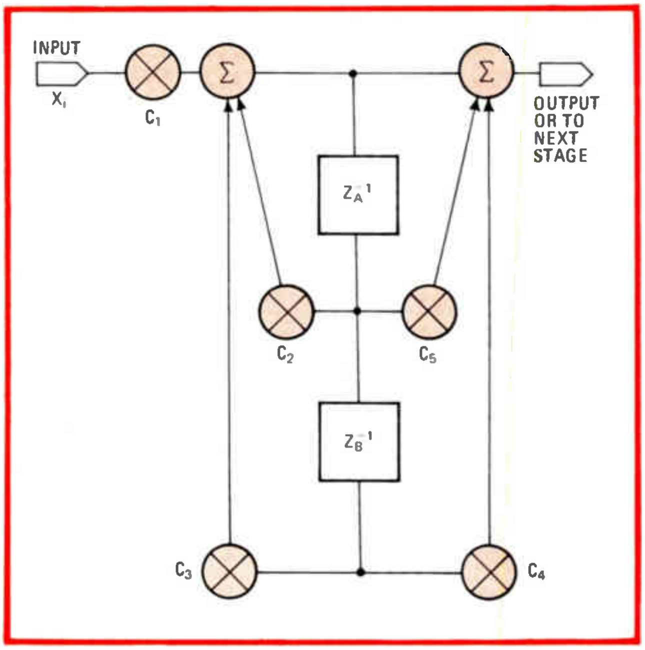
FIR filters (Fig. 3) are the most popular of digital filters. They are regular in structure, are easily understood, need only simple control hardware, and do not require large internal word sizes. Because they are relatively insensitive to coefficient accuracy, smaller coefficient word sizes can be used; furthermore, the coefficients can be adjusted for size while in operation. Adaptive filters and linear predictive coders-decoders are examples of such variable filters. Another advantage of the FIR filter is its linear phase response.

Because a FIR filter has only feedforward and no feedback terms, its algorithm need be calculated only once for every output sample, provided the output sampling rate is less than the input sampling rate. This characteristic is useful for low-pass filtering and band-pass demodulation filtering.

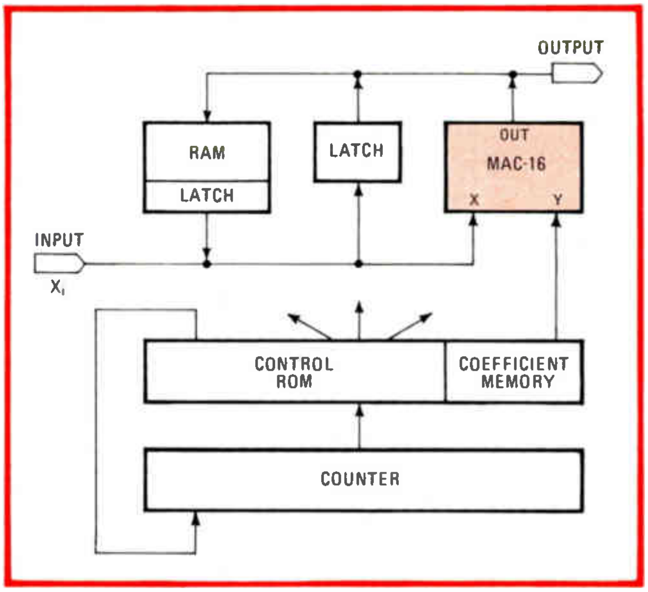
On the negative side, FIR filters require the most memory, the most multiplications, and the most additions of any digital filter. The typical requirement is from 32 to 512 memory words, multiplications, and additions. Figure 4 shows the hardware for a single-channel FIR filter. Its sequence of operation is shown in Table 1.

Each of the steps listed in this table represents one cycle of the master system clock of the circuit in the figure. Depending on the MAC used, the clock frequency may be as high as 14 megahertz (the assumption is made that the memories and sequencers used are capable of keeping up with the master clock's speed).

If a shift register were used instead of a RAM in this circuit, system speed would be limited, since the MAC would have to calculate the entire number-crunching problem it has before another word of data was loaded into the shift register. (Loading the shift register moves over all the other data bits in it serially and when done too soon interferes with the MAC's input data.) The use of a RAM eliminates this problem, since the new values can be written into the RAM in locations already included in the MAC's calculation. With enough RAM and some extra control circuitry, a single MAC can actually become a multichannel filter. In this case memory is divided into N word blocks, and pointers are



6. Canonical form. Just two or three stages of a recursive (infinite-impulse-response) digital filter are capable of yielding the same or better performance than a large nonrecursive filter. The canonical form for a single-stage recursive filter is shown.



7. Recursive hardware. A MAC can be used to make a recursive digital filter. The RAM is a latch type capable of a read and write operation within a single multiply-accumulate cycle. Timing instructions for calculating such a filter are listed in Table 2.

set up in a scratchpad memory for each block of data.

The use of a coefficient symmetry in a FIR filter may be necessary should the output sample rate of the circuit times the number of multiplications exceed the maximum speed reasonably attainable with the use of a single MAC. Its use doubles the MAC's effective rate of multiplying and adding, at the expense of extra medium-scale integrated circuits.

Should the data rate be so high that the output sample rate would equal the MAC's cycle time, a series of MACs can be multiplexed, each starting and finishing the algorithm at a different time. Instead of storing the coefficients in a very high-speed ROM, they can be loaded into the system from RAM, ahead of time, by means of a slow system controller.

An example is shown in Fig. 5. Four MACs are used in parallel. The coefficients are held by an external four-stage register. A tag bit, circulated in the shift registers, operates the accumulator and output controls. The outputs of the accumulators are three-state and therefore can be bused in sequence. The system's 10-MHz clock operates the input, output, and C registers directly.

In operation, a MAC accumulates four products and is then gated to the output bus. On the next clock cycle, the adjacent MAC is similarly gated to the output bus. This sequence is repeated for each adjacent MAC, on successive clock cycles, as steady-state 10-MHz outputs are sustained.

Recursive filters are more complex

Compared with nonrecursive FIR filters, recursive IIR filters exhibit a better frequency response while using fewer parts. However, they run the risk of instability through oscillations, they are susceptible to offsets, and they may suffer from a nonlinear phase response. They are also more complex than nonrecursive filters, since they have feedforward as well as feedback terms.

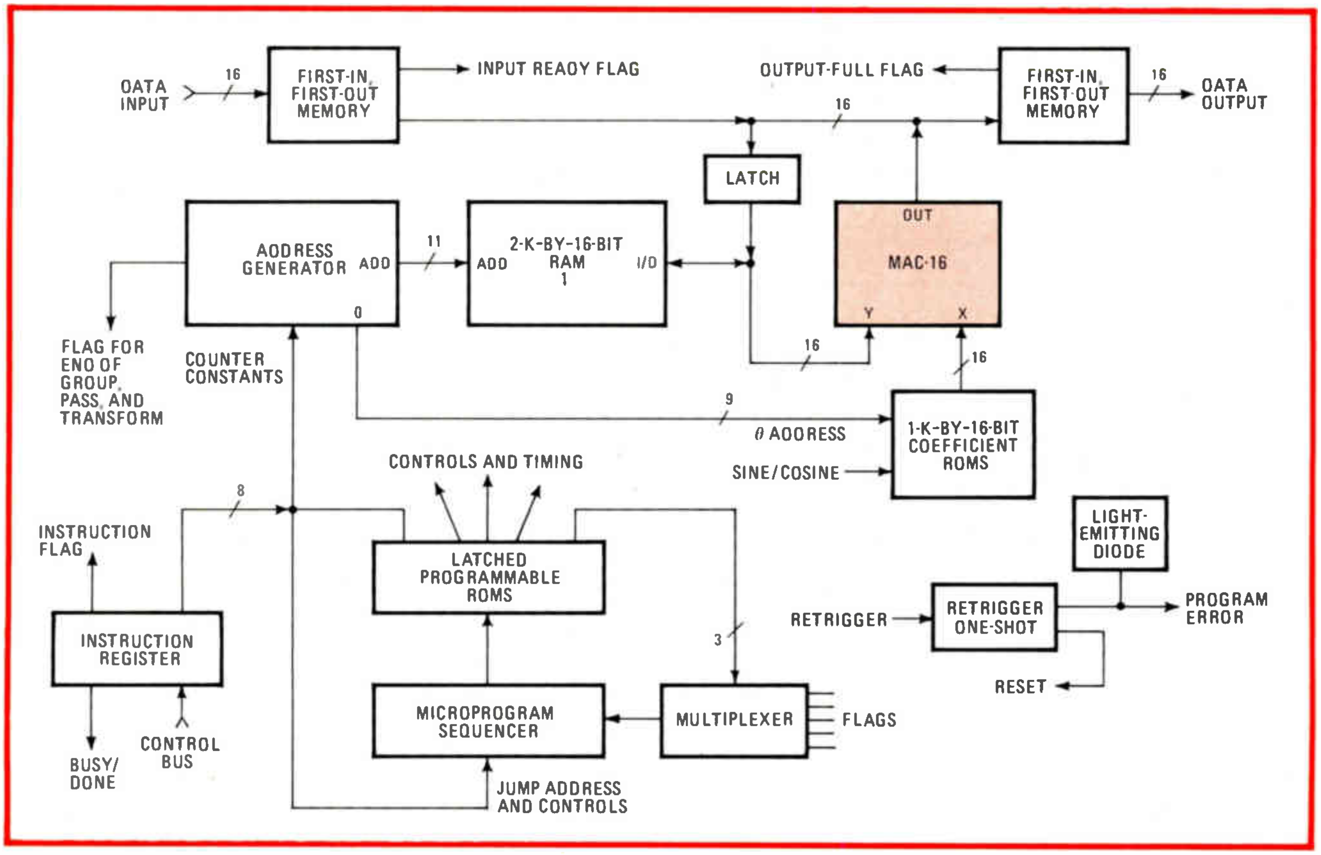
Figure 6 is a single stage of a canonical form of an IIR filter. Two or three such stages hooked up in series can offer the same or better performance than a much larger multitap nonrecursive filter. A big design drawback of recursive filters, however, is the careful attention that must be paid to the coefficients, since the words for the feedback terms can grow excessively large. Recent developments in this area, however, are providing some solutions to these problems.

Figure 7 illustrates a typical configuration using one or more MACs. For the sake of simplicity, the memory coefficients C_1 through C_5 of Fig. 6 are not shown and are kept separate from the RAM used to store the Z values. The latch in Fig. 7 performs the Z_a^{-1} to Z_b^{-1} shift of Fig. 6. The RAM in Fig. 7 is a latch type capable of a read and write operation within a single multiply-accumulate cycle.

Table 2 lists the timing instructions needed to calculate a single recursive-filter stage. Each of the instruction cycles shown corresponds to a single multiply-accumulate cycle. The MAC input terms in Table 2 are

TABLE 2: RECURSIVE (IIR) FILTER TIMING

Cycle	Memory	Latch	MAC		Coefficient
			Inputs	Outputs	
1			X_i, C_1		C_1
2	A_{out}	load A	A, C_2		C_2
3	B_{out}, B_{in}	A_{out}	B, C_3	$X_i \cdot C_1 = (1)$	C_3
4			hold B, C_4	$(1) + A \cdot C_2 = (2)$	C_4
5	A_{out}, A_{in}		A, C_5	$(2) + B \cdot C_3 = (3)$ out	C_5
6				$(3) + B \cdot C_4 = (4)$	
7				$(4) + A \cdot C_5$ = stage out	



8. FFT on a card. The wide variety of LSI circuits available allows the implementation of an FFT processor on a single printed-circuit board. A key element of such a processor is a low-cost and tiny large-scale integrated multiplier-accumulator such as TRW's TDC1010J 16-bit unit.

those operands and controls that are made available to the MAC circuit before the appropriate clock edge to load the MAC circuit is received. The output terms of Table 2 are the contents of the accumulator register, after the clock system edge occurs.

Coefficient C_1 is an interstage gain value for presetting the valid input data down to a few bits to preclude large-scale overflow. Typically, one or two such gain settings are present throughout a cascaded filter circuit. In this manner, a MAC-16 is capable of calculating a complete two-pole, two-zero complex filter stage in just 600 nanoseconds.

Since complex recursive filters require larger word sizes than nonrecursive types, their internal word sizes in each stage can often be 16 bits wide to match 8-bit analog-to-digital converters. Depending on the Q of the filter, the coefficients can also be 12 or 16 bits wide.

The fast Fourier transform

The FFT, a more complex but more efficient version of the discrete Fourier transform, can be implemented digitally in real time on a single pc board thanks to LSI components. The basic number-crunching operation, often called a butterfly, can be accomplished by a single MAC at a pipeline rate of 8 or 10 microcycles. The decimation-in-time version of the butterfly is shown in Fig. 11, broken down into real multiply and add components. For the MAC-16, this corresponds to a calculation time of 1,200 or 1,500 ns. Should two MACs be used (one for the A and C data outputs and one for the B and D data outputs), this pipeline rate could be cut in half.

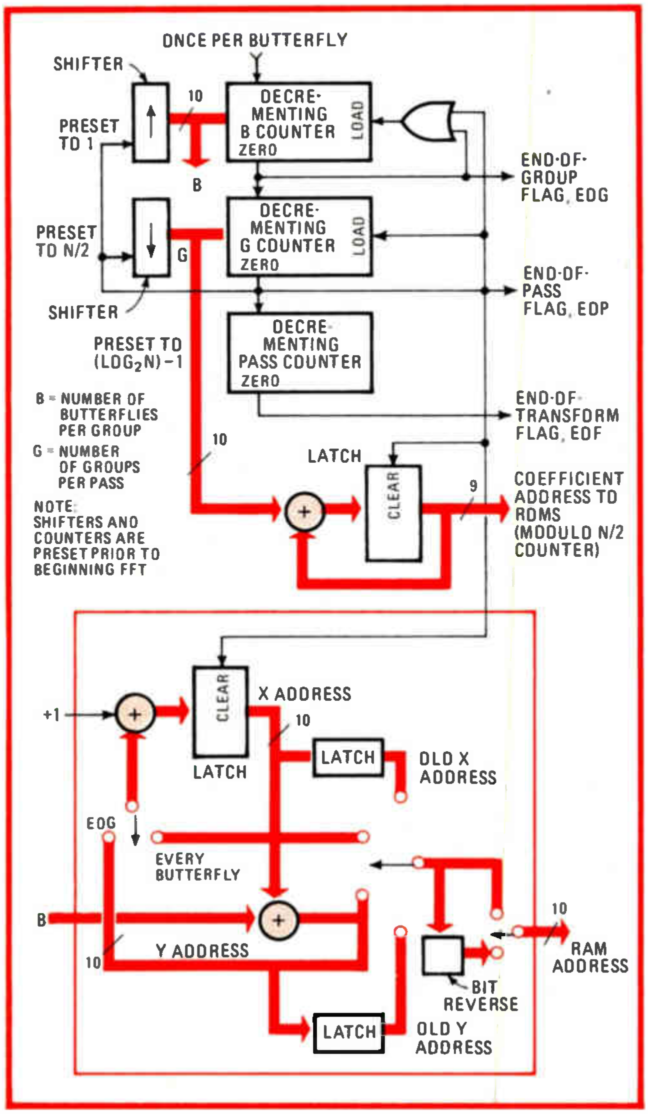
Figure 8 shows the hardware needed to implement an FFT operation. The MAC-16 (shown as the TDC1010J) is the butterfly circuit. The data RAM can be split among two n-channel MOS RAMs each organized as 2,048 by 8 bits. The pair of first-in, first-out circuits is optional and is used to simplify input/output interfacing for an external controller. Timing and control are performed by the sequencer and the programmable ROMs.

Instructive details

Software instructions from the system controller to the instruction register are decoded to tell the FFT processor what the transform length is (2 or 3 bits) and provide it with the necessary macro-instructions (3 or 4 bits). Such macro-instructions are typically: load and perform an FFT; load and perform an inverse FFT; produce a complex output; and Hanning-weight the memory contents and output. A single instruction is sent by the system controller for each block of data transferred into or out of the circuit or operated on within the circuit.

The one-shot multivibrator of Fig. 8 is retriggered continually by the system's clock. Should the system's program hang up, as it were, the system's clock will reset all operations and produce an error flag.

The address generator can be designed in a number of ways. The MSI devices used for it here lack the performance flexibility of a bit-slice microprocessor, but occupy less real estate and cost less. Similarly, in the choice of a sequencer circuit the small size and the small quantity of



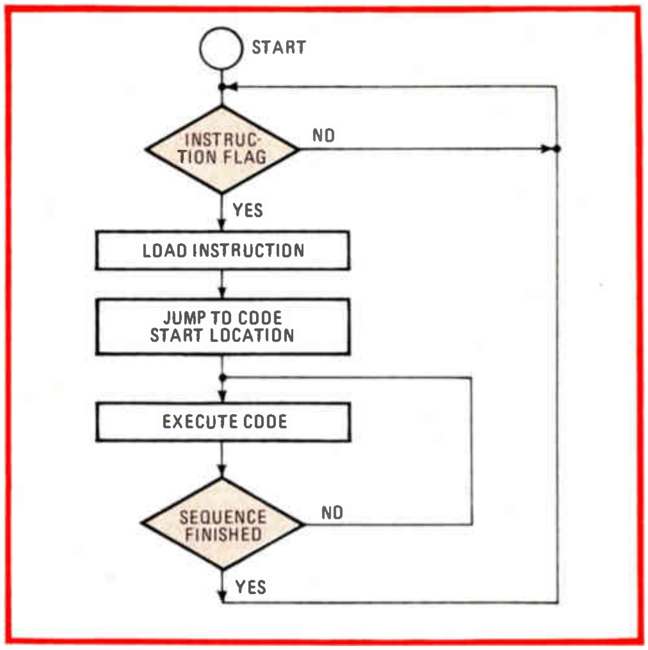
9. Address generator. For the FFT circuit illustrated in Fig. 8, address generation is required as shown. This circuit may not be an optimum one from a hardware viewpoint but has instead been configured both for simplicity of operation and for low parts costs.

control required for this application should weigh heavily. In this circuit, after all, the sequencer has only to set up loop counters in the address generator and then run repeatedly through 8 or 10 cycles per butterfly until instructed to stop. A sample block diagram of an address generator circuit (not optimized for a minimum amount of hardware) is shown in Fig. 9.

Keeping the software simple

Software for calculating the FFT was designed to be simple. However, it is not necessarily the optimum in terms of hardware and performance. The software resides in the system in programmable ROMs.

Figure 10 is a flow chart of the basic FFT software. Instruction bits direct the sequencer to the first few addresses of the PROMs. Each address contains a separate unconditional jump instruction. This instruction directs the program to start at a location where the necessary code exists to execute the desired macro-



10. Software. This software algorithm is used to implement the FFT processor whose circuit is shown in Fig. 8. Like the address-generator circuit of Fig. 9, this software algorithm, which resides in programmable ROM, is not optimized but kept simple.

instruction. After examining the flags for the task at hand, the program implements that task, sets the "done" flag, and jumps back into the program loop to wait for the next instruction.

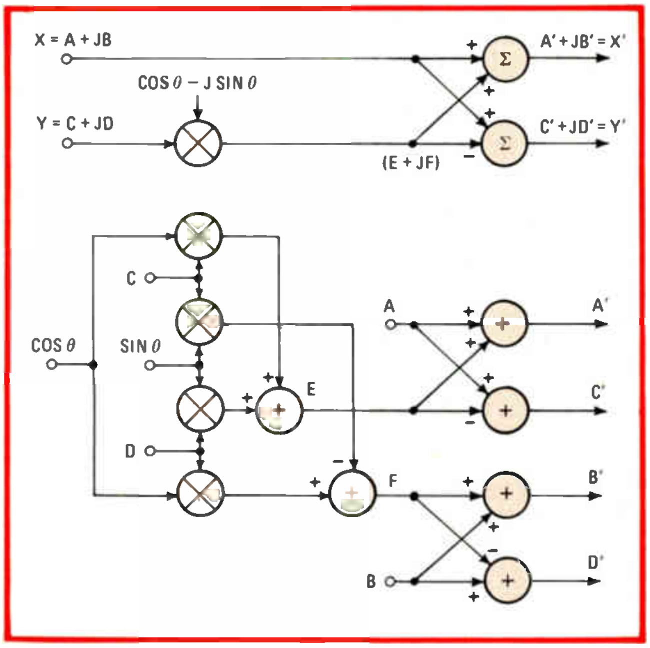
The microcode for a multiplier-accumulator needed to calculate a 10-cycle butterfly circuit is given in Table 3. As previously noted, the complex form of a basic decimation-in-time FFT is shown in Fig. 11, which is broken up into real multiplication and addition components.

As Table 3 indicates, the first butterfly of a pass starts at step 1. After the 14th step, the program goes back to step 5 and repeats the sequence of steps 5 through 14 until all the butterflies of a pass are completed. The use of a fall-through latch IC (74LS373) between the MAC's output and RAM allows data to be written from the MAC either immediately into memory (steps 5 and 10) or later into memory (steps 7 and 12). Note that only the old Y address need be stored in step 14.

To be precise

Most FFT designers use 2's complement arithmetic to maintain single-precision calculations. That is why the constants shown in Table 3 are 0.9999 instead of 1.0, 0.9999 being the maximum positive number possible. Since the additions in the algorithm of Table 3 can cause overflows into integer-number fields (that is, 1.0 and greater), a divide-by-two scheme is usually implemented, either at the butterfly inputs or at the outputs before data is written into memory. The 1-bit shift inherent in the most-significant-product output format compared with the input data format of a MAC readily allows for a divide-by-two scheme at the MAC's output. As a result, the butterfly sequence of instructions shown in Table 3 is automatically scaled down when using such MACs. The round control can be used to shorten the double-

TABLE 3: TEN-CYCLE FAST-FOURIER-TRANSFORM BUTTERFLY TIMING						
Step	Load (L)/hold (H) input data, coefficients	Accumulate	Subtract	Round	Contents of MAC output register	Memory operations
1	L C, Lcos	0	0	1		C_{out}
2	L D, Lsin	1	0	0		D_{out}
3	L A, L0.9999	1	0	0	C • cos	A_{out}
4	H A, H0.9999	1	1	0	D • sin + C • cos ≡ E	
5	H A, H0.9999	1	0	0	0.9999A + E = A' out	A_{in}
6	L C, Lsin	0	0	1	0.9999A − (0.9999A + E) ≡ −E	C_{out}
7	L D, Lcos	1	1	0	0.9999A − E = C' out (hold in latch)	D_{out}
8	L B, L0.9999	1	0	0	C • sin	B_{out}
9	H B, H0.9999	1	1	0	D • cos − C • sin ≡ F	C_{in}
10	H B, H0.9999	1	0	0	0.9999B + F = B' out	B_{in}
11	next inputs	0	0	1	0.9999B − (0.9999B + F) ≡ −F	new C_{out}
12	next inputs	1	0	0	0.9999B − F = D' out (hold in latch)	new D_{out}
13	next inputs	1	0	0		new A_{out}
14	next inputs	1	1	0		old D_{in}
	go to step 5					



11. Butterfly. The complex form of a basic decimation-in-time butterfly circuit consists of real multiplication and addition components. Such an algorithm is used to simulate digital filters, which in turn make possible the FFT processor of Fig. 8.

precision calculations to turn them back to rounded single-precision answers.

For a little more speed, the divide-by-two scheme can be implemented at the MAC's inputs. This reduces the number of cycles for a butterfly from 10 to 8, with steps 3 and 4 and steps 8 and 9 in Table 3 being consolidated. But there are disadvantages to this approach compared with the use of the sequence of Table 3. Two fixed coefficients, 0.5 and 0.9999, must be used as inputs to the MAC. The sine and cosine coefficients are prescaled down by 1 bit to make the divide-by-two scheme possible, causing a 1-bit decrease in coefficient accuracy. The MAC output bits are similarly scaled down by 1 bit. In the case of TRW's MACs, this means that the most-significant-product word (less the most significant bit) is read out along with the MSB of the least-significant-product word. Although this is no problem for the MAC-8 and MAC-12, it is one for the MAC-16. That is because the least-significant-product output word is multiplexed with the Y input word, and data is pipelined into and out of the MAC simultaneously on four out of eight cycles. In addition, the rounding feature cannot be used, since it adds a 1 to the MSB of the LSP. The output answers are therefore truncated.

More pros and cons

The error resulting from truncation rather than rounding will cause a slight increase in the computationally induced noise, compared with the noise for a 10-cycle butterfly circuit. The 8-cycle method also requires more hardware. The old X and Y addresses must be stored in memory, a four-word two-port file (type 74LS670) must be added, and 6 more bits of microcode added to control the file. And should the MAC-16 be used, an extra latch IC must be added for purposes of bus interfacing.

Nevertheless, an 8-cycle butterfly circuit offers higher performance than a 10-cycle one. For example, a 1,024-point FFT can be performed in real time on data with a 50-kHz bandwidth. Furthermore, the additional file and address storage available in an 8-cycle circuit allows more efficient data handling for such functions as array multiplications, multichannel digital filters, integrators, and correlations. □

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New Multiwire meets the challenge of interconnecting chip-carriers

Two layers of the new Multiwire can replace 11 layers of printed-circuit conductors

by George Messner and R. Page Burr, *PCK Technology Division of Kollmorgen Corp., Glen Cove, N. Y.*

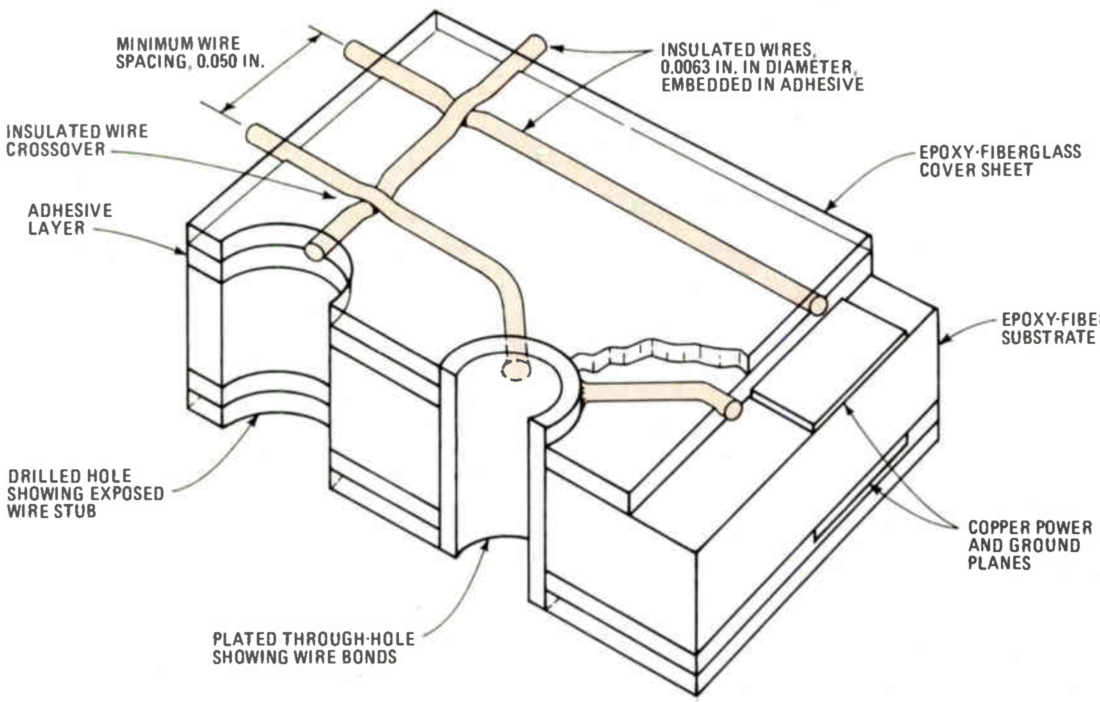
☐ Multiwire, a technique for automatically "writing" insulated wires onto an adhesive-coated printed-circuit board, has been highly successful as an alternative to the more complex and expensive multilayer board approach. Originally designed to interconnect 14- and 16-pin dual in-line packages, it has now been upgraded to face the soaring interconnection densities that will be needed for the new, small chip-carriers housing large- and very large-scale integrated circuits.

Multiwire for the 1980s is based on a new computer-controlled machine, the T-14. It has a redesigned wiring head that can put down finer wires on a much tighter grid—25 to 18 mils—than the original system's 50-mil grid. The T-14 can thus place a layer of wires with a density of 80 inches of conductor per square inch for its normally used 6.3-mil wire and 100 inches of conductor per square inch for 4-mil wire. By comparison, the older system has a maximum density of 40 inches of 6.3-mil wire per square inch per layer of wiring.

An examination of the pc wiring requirements for the 1980s shows the advantage of the new Multiwire system over the multilayer board method.

The familiar dual in-line package, or DIP, has been efficiently accommodating small- and medium-scale integrated circuits for over a decade. However, for devices with 40 pins or more, this package becomes large and unwieldy and, furthermore, cuts the electrical performance of the chip. Consequently, small square packages called chip-carriers are emerging that have their terminals spaced on centers 50, 40, or even 20 mils apart [*Electronics*, Sept. 28, 1978, p. 120].

Connecting these multipin packages on a printed-



1. Wire over wire. This is a three-dimensional view of a typical Multiwire board. Insulated wires are embedded in an adhesive layer on an epoxy-glass substrate. Wire terminations are formed by drilling through a wire and the board and then plating both the hole and wire ending.

circuit board requires significant changes in the manufacture of board substrates. The table, based on theoretical derivations by Donald Seraphim of IBM Corp., lists some typical changes in conductor-density or connective-capacity demands when these newer packages are used.

Increasing connections

This data indicates that the connective capacity of a circuit board is moving from about 30 in. of wire per square inch of substrate for a relatively simple two-sided board interconnecting DIPs, to 80 or even 200 in./in.² for interconnecting chip carriers requiring dense multilevel conductor structures. A similar analysis was presented recently by Charles L. Lassen of Exacta Circuits Ltd. [*Electronics*, Sept. 27, 1979, p. 113].

Other aspects of modern electronics also contribute to the increasing density of interconnection. The desire to package all the electronic circuitry of a controller or an instrument on a single board, the inclusion of diagnostic circuitry, the need to reduce conductor lengths for devices operating at ever increasing speeds, and the need to control impedances of the interconnecting circuits all are likewise pushing up board densities.

CONNECTIVE CAPACITY REQUIREMENTS FOR VARIOUS PACKAGING SITUATIONS

Typical packaging situation	Approximate number of pins/in.²	Amount of needed conductors (in./in.²)	Printed wiring levels		
			50-mil grid	24-mil grid	20-mil grid
1 16-pin dual in-line package/in.²	15	34	2 (1.7)	1 (0.8)	1 (0.7)
2 16-pin DIPs/in.²	30	67	3–4 (3.4)	2 (1.68)	2 (1.34)
24-pin chip-carriers on 0.5-in. center	96	216	11 (10.8)	6 (5.4)	5 (4.3)

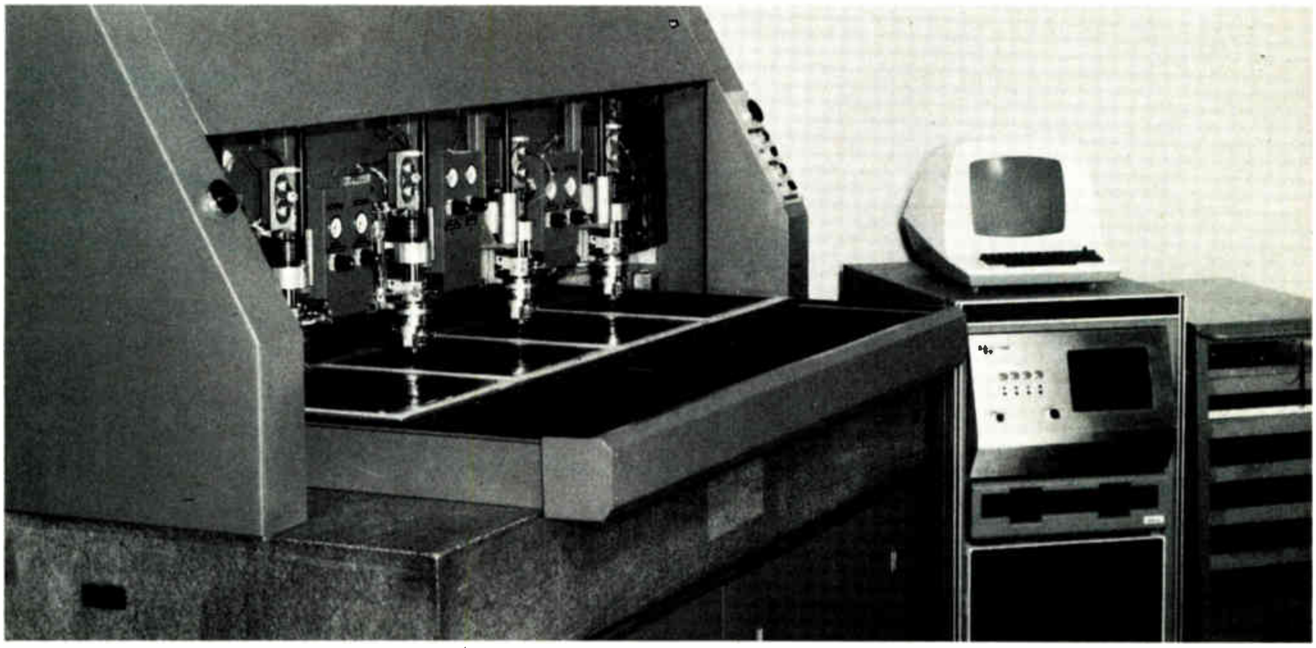
Board designers and manufacturers must meet these demands either by reducing the width of printed-circuit conductors and the spacing between them or by increasing the number of conductive layers vertically. However, both choices invoke definite penalties in terms of producibility. Ensuring the integrity of hundreds of feet of 3- or 5-mil-wide conductors on the large boards or panels (up to 2 square feet) that are typically processed in the circuit-board shop—a size necessary for processing economics—is a difficult feat. Nor is the design, tooling, and manufacture of 15- or 20-layer boards a simple, high-yield process.

Benefiting from insulation

Some of these circuit manufacturing pressures may be eased if the printed and etched conductors are replaced by Multiwire's insulated wire. The insulation in effect eliminates shorts between conductors. As a result, thin wires may be placed close to or actually in contact with each other and may cross one another without restriction on the same plane, thus considerably reducing the number of conductive planes needed for dense interconnections and greatly simplifying the design.

As an example of the new Multiwire's advantage over the multilayer board method, consider the third case presented in the table. Interconnecting 24-pin chip-carriers on 0.5-in. centers on the surface of a pc board designed with a 50-mil wiring grid would require an 11-layer board to meet the resulting 216-in./in.² wiring density. The same design could be accommodated in two layers of the new Multiwire (the density of two layers is 220 in./in.² for 4-mil wires). Thus the use of advanced Multiwire cuts the pc requirement to that of a simple two-sided board.

The Multiwire process is an automated interconnection system in which 6.3-mil or thinner polyimide-insulated magnet wire is laid down on an adhesive-



2. Third generation. PCK Technology's advanced T-14 Multiwire system is a four-headed machine that can wire 6.3- and 4-mil wires on a 25- to 18-mil grid. A completely redesigned wiring head and ultrasonic bonding proportional to table speed make this possible.

coated substrate with or without etched power and ground planes. The terminations are formed by drilling through the wire and board and plating through the resultant holes. These holes are then used for component insertion and subsequent soldering operations. A cutaway view of a Multiwire board is shown in Fig. 1.

If the design requires placing more interconnections than can be accommodated on both sides of the substrate, a layer of adhesive can be placed over the wired surface and the wiring process repeated. Thus three or even four levels of wiring patterns may be formed on a single substrate.

Extension of the connective capacity in Multiwire depends primarily on the precision with which the wire is manipulated by the wiring machine and not in any way on the improvements in process control, air quality, or image-formation techniques that are essential to achieving great precision with graphic processes.

The length of the manufacturing process is essentially independent of the complexity of the circuit board. The layout of the circuit is formed entirely by a computer-controlled wiring machine in a single step.

A crucial step in the Multiwire process is the formation of the wire pattern on the surfaces of the adhesive-coated Multiwire board. A typical wire path, for example, often involves execution of 135° or even 180° turns to intersect component holes.

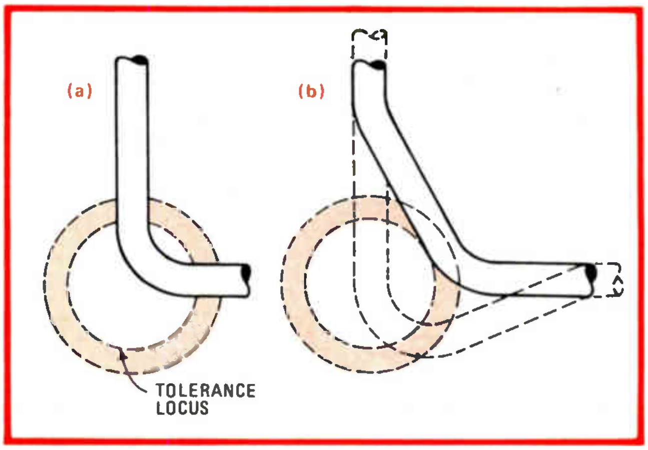
The ability of the Multiwire system to lay down wire precisely has evolved over a period of several years and has involved the development of considerable new technology in the area of wire handling and writing. The newest machine, the T-14, is the third generation of production wiring machines designed and built in the past 10 years by the PCK Technology division of Kollmorgen Corp. and reflects the latest advances in the state of precision wire placement.

Multiwire wiring machine

The machine consists of a table capable of translation in the X direction under an overhead frame upon which four in-line wiring leads are mounted (Fig. 2). The four heads are capable of moving in the Y direction. Both motions are controlled by precision optical scales and dc servo motors, thus providing highly accurate split-axis motion. A third dc motor drive rotates the heads within the overhead frame with a resolution of 200 steps per revolution. Normally only eight vector directions are used for wiring. Other wiring head functions are implemented by electrical and pneumatic actuators mounted within the head assemblies.

The positioning motors, the various wiring-head motions, and the control functions are directed by a DEC PDP-11/03 master computer and a pair of 8-bit Motorola 6800 microcomputers from manufacturing data files. These files are stored on floppy disks installed in a dual disk drive that is part of the machine control system. The control electronics for the system, housed within a single cabinet, is modular to facilitate servicing.

Vacuum shuttle plates help perform the loading and unloading of jobs on the table. The boards to be wired are mounted on the shuttle plates on a loading jig off the machine to minimize machine idle time. The maximum speed of the table and the overhead frame of the T-14 is double that of previous models. The use of microprocessor control with a crystal-controlled clock ensures precise timing of the head functions. Also, the table design allows panels as large as 24 by 24 in. to be wired instead of the previous maximum size of 15 by 20 in.



3. Dragging it. For turns of 90° (a) and 135° (b), disturbances or variations in the drag tension may be critical. The effect can be to pull the wire completely out of the circle of tolerance in which it is to be wired. The T-14's head minimizes this effect.

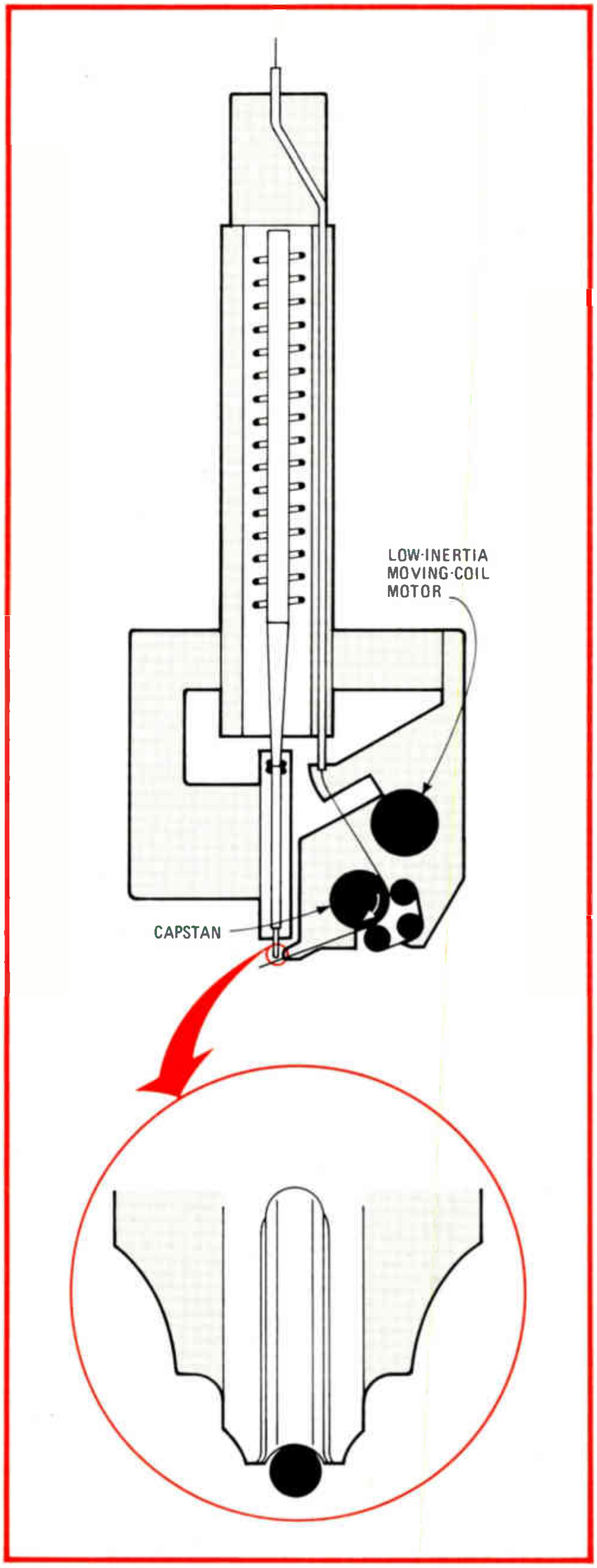
Wiring head

The wiring head must reliably perform several important functions. It has to feed, locate, and affix to the board surface the start of each new wire; it must cause the entire wire to adhere to the board; it must form and guide the wire at each inflection point; and it must cut the wire at the end of the wire run in such a way that the next wire may be reliably started.

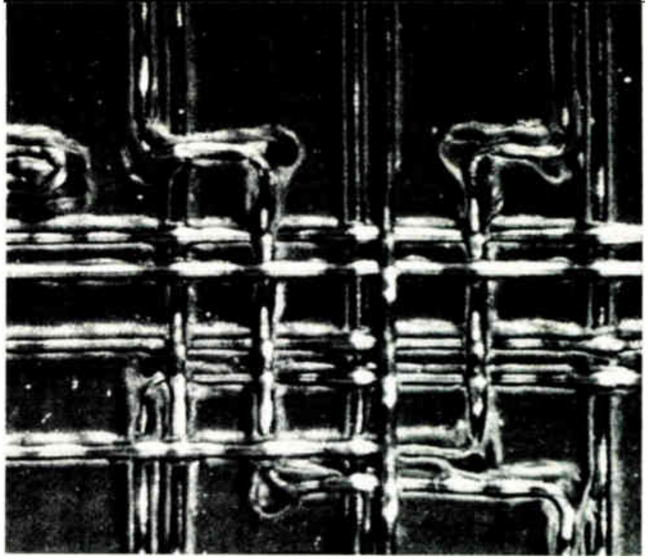
To start the next placement, the feeder mechanism drives a short length of new wire into the guide groove at the bottom of the stylus. The head is then lowered to the surface of the board and ultrasonic energy is applied to the stylus synchronously with the start of the table motion. The wiring stylus is connected to a magnetostrictive stack in the body of the head by an exponentially tapered horn section. It is driven with ultrasonic energy at a frequency of about 25 kilohertz from a coil mounted in the body of the head and surrounding the magnetostrictive stack.

The wire is physically bonded to the adhesive by simultaneously applying heat and pressure from the head suspension system. The heat is generated at the wire-adhesive interface by ultrasonic vibration transmitted to the wire. This method offers a highly desirable byproduct in that it reduces the friction between the wire and the stylus essentially to zero. The ultrasonic transducer and stylus assembly rides on a spring- and air-suspension system designed to allow the stylus at the wire to float freely over the irregularities of the board surface and over the wire crossings. Consequently, constant pressure and adequate coupling with the wire are maintained.

As a result of this operation, the path of the wire laid down on the board is essentially congruent with the path described by the writing head moving over the board; in other words, the exact position of the wire on the surface



4. New head. In T-14's wiring head, wire is guided down through Teflon tube. Near entrance to the feed, the wire is captured and driven by a small low-inertia moving-coil motor and capstan. A special stylus (inset) firmly captures the wire in a deep groove.



5. Hairpin turn. Piece of work by new Multiwire machine shows the wiring density and tight maneuvers possible. Patterns like these have unlimited crossover capability and can pack in 160 to 200 inches of wire per square inch on the two sides of a board.

of the board is everywhere precisely controlled. Many of the desirable properties of Multiwire and several significant elements of the concept are derived from this precision. Because the wires are written on the board surface by the numerically controlled system, the relative locations of all points of the conductors with respect to each other and with respect to the future sites of the termination holes are not only known and reproducible but are, of course, specified in advance. The Multiwire machine may therefore be thought of as a "wire plotter."

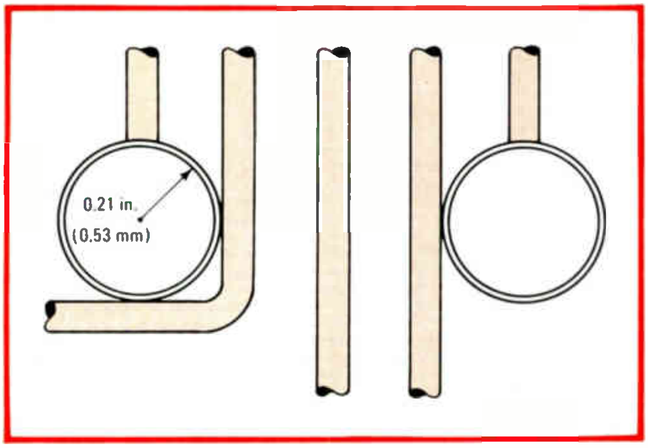
Precision wiring improvements

Analysis of the performance of older versions of wiring machines indicated that increased precision could be achieved if improvements were made in three critical elements of the wiring process.

First, it was important to devise a system to almost completely decouple fluctuations in the wire-feeding tension from the wiring operation itself. Good wire bonding and closely controlled wire placement would not be possible, it was felt, so long as tension disturbances existed at the wiring point. Figure 3 shows the impact of drag-tension disturbances on critical maneuvers for a 90° and a 135° turn. Note that if the drag level is high enough, it may pull the wire completely out of the terminal area and disconnect the hole from the net.

Second, major changes in the head and the stylus geometry were necessary to improve wire guiding and therefore the final precision of wire placement on the board surface. Third, relating the ultrasonic bonding power level to the motion was expected to complement the enhanced wire guidance and to improve the ability of the machine system to articulate the wire in high-density circuit patterns.

The wiring-head design of the T-14 machine (Fig. 4) incorporates these improvements. The wire enters the head at the top and is guided downward through most of its length by Teflon tubing. Near the entrance to the feed tube, the wire is driven positively by a small low-inertia moving-coil dc motor and capstan arrangement mounted in the feeder assembly. The motor armature voltage is applied to the motor terminals through slip



6. Traffic jam. As this diagram shows, a uniform 25-mil wiring grid runs into problems when three conductors are run between holes on 100-mil centers. The new Multiwire eliminates this trouble with a modified wiring algorithm based on a 16-mil grid between holes.

rings on the head assembly and is programmed by the logic system controlling the head. Wire may be delivered from the feeder with a positive, zero, or negative drag force, as desired. Hence this arrangement not only isolates the tension but also provides an additional degree of freedom in wire articulation control.

In the groove

Considerable experimentation with configurations for the wiring stylus has led to a new design in which a long, deep groove firmly captures the wire as it emerges from the feeder (Fig. 4, inset). The depth, configuration, and positioning of the groove is such that the stylus actually bends the wire into the desired shape when the head makes a tight maneuver.

Since the wiring process is dynamic in the sense that the wiring conditions are continuously changing as a result of the table motion, the new ultrasonic system is designed so that the power delivered to the transducer and therefore to the wire is a function of the speed of the wire passing under the tip. The digital control system maintains the ultrasonic power output at a level roughly proportional to the table speed. It does so by pulse-width-modulating the output signal from the ultrasonic generator with a duty cycle that is determined by the table drive logic.

The effect of this additional control is to maintain the ultrasonic bonding energy per unit length of wire at a relatively constant level independent of table—that is, wiring—speed. More particularly, the adhesive is not overheated when the machine makes small motions or the intricate wiring maneuvers that necessarily take place at less than maximum wiring speed. The bonding action therefore tends to be much more uniform throughout the wire pattern, eliminating one of the shortcomings of earlier machines.

The net result of these advances in the wiring system design is that the T-14 wiring machine can generate wire patterns with 6.3-mil insulated wire having the complexity of 40 wires per inch (see the table again). That is to say, if all wires are evenly spaced on a 25-mil grid, the machine will produce a connective capacity of 80 inches per single wiring level (in the X and Y directions, because of unlimited crossover capability), as stated earlier, or 160 inches per inch square of two-sided Multiwire board. Figure 5 shows the precision wiring performance of the system. The sharpness of wire articulation achieved in tight maneuvers is clearly visible.

It is well known to most circuit designers that, as a practical matter, a uniform 25-mil grid does not offer much relief to the problem of between-the-holes congestion for component holes centered 100 mils apart. As can be seen in Fig. 6, the higher density is obviously useful in the "streets" and "avenues" of the pattern, but the hole clearance constraints permit use of only the center one of the three equidistant conductors that can theoretically pass between component holes.

A modified design algorithm producing more closely spaced wires is therefore desirable. Since the T-14 machine system can, in fact, place wires with a center-to-center spacing as narrow as 12 mils, a wide variety of design algorithms can be used to avoid the 25-mil blocking problem. With one of these algorithms, the center-to-center distance between wires in the densest portions of this pattern is 16 mils. This algorithm therefore permits three wires per wiring layer to be placed between holes that are 100 mils apart.

The basic technology of the Multiwire system has recently been extended to the use of 4-mil-diameter wire (No. 38) so as to provide a significant additional enhancement in connective capacity. With this wire, the T-14 can generate the patterns on an 18-mil grid. The corresponding connective capacity of the system is therefore about 110 inches per square inch per layer, or 220 inches per square inch for a conventional two-layer Multiwire board.

Wiring speed and productivity

The productivity of this $195,000 wiring machine depends partly on the character of the wiring pattern.

After a short acceleration, wire bonding takes place at a speed of approximately 240 inches per minute, but a substantial portion of the total wiring time is devoted to auxiliary operations. The wire-starting sequence takes approximately 1.5 seconds, of which 0.5 s is a programmed delay to allow the adhesive to cool after the initial tacking down of the wire. The head rotation, which occurs at each inflection point of the wire, takes place in 0.1 to 0.4 s, depending on the angle of rotation. Finally, wire cutting and ending is done in 0.5 s. In addition, repositioning of the board to the beginning of the following wire is programmed at the maximum permissible machine speed.

On the average, a four-headed wiring machine produces approximately 2,400 wires per hour. A substantial percentage of wires connect more than two points or holes—in fact, the average number of interconnections per wire has been found to be about 1.6. Therefore, the average productive capacity of a wiring machine is about 3,840 connections per hour. As a typical example, a four-headed machine in one hour wires four 10-by-10-in. logic-type boards, each one interconnecting 120 16-pin dual in-line packages and the required input/output points. □

Peak-reading millivoltmeter responds instantaneously

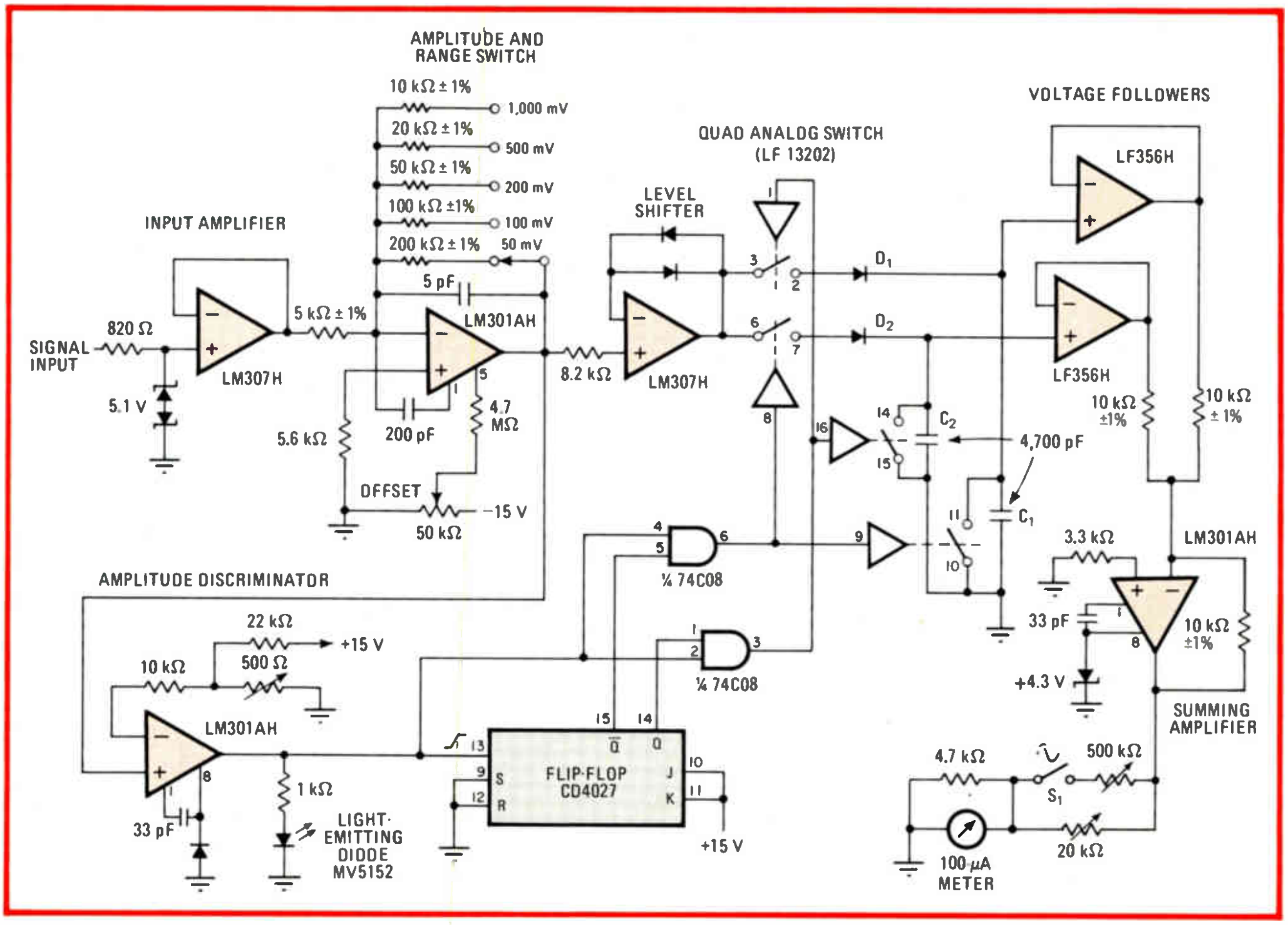
by William J. Mundl
Department of Psychology, Concordia University, Montreal, Quebec, Canada

Requiring but a single pulse or cycle of a sine, square, or triangular wave in order to determine its peak value, this millivoltmeter-microammeter will serve as a respectable substitute for an oscilloscope, oscillographic recorder, or other instrument that must deliver an instantaneous response. Such a low-cost unit is extremely useful in biomedical applications, where the amplitude of certain electrophysiological variables of small magnitude has to be closely monitored.

The millivoltmeter processes either negative-going pulses or the negative portion of the incoming waveform. The signal voltage first passes through the LM307 input amplifier and through the LM301 range amplifier (see figure). The level shifter that follows imparts a positive offset to the signal to compensate for the voltage drop of charging diodes D_1 and D_2, which transfer the peak value of the wave to holding capacitors C_1 and C_2. The voltages on C_1 and C_2 are then alternately applied to the input of the LM301 summing amplifier; any change in the amplitude of the input signal will thus be instantly reflected at the output.

Capacitor switching is achieved with a quad analog switch (LF13202), which in turn is driven by a toggled 4027 flip-flop that is triggered by the input signal and the LM301 amplitude discriminator. The 500-ohm potentiometer is used to set the input trigger voltage at any point near zero, a necessary condition for detecting small input voltages.

As C_1 is charged, C_2 is discharged, and vice versa. Thus the stored voltage on C_1 or C_2 is constantly and quickly updated without the need for a discharge cycle. Note that the zener diode at the input to the summing amplifier prevents it from overdriving the output meter.



1. Quick update. This meter requires only one negative pulse or half cycle of sine-, square-, or triangular-wave input to determine peak current or voltage amplitude. The applied signal charges capacitors C_1 and C_2 alternately, so that either can update immediately without the need for a separate discharge cycle. The meter's range is 0 to 1 V or 0 to 100 μA. The output meter reflects instantaneous changes.

The output microammeter may be calibrated in millivolts through the use of its associated 20-kilohm and 500-kilohm potentiometers. Switch S_1 must be closed in order to measure sinusoidal waveforms.

Although this meter has been used mostly for measurement tasks below 100 hertz, it will work over a wide range of frequencies and thus is suitable for general-purpose audio-rate applications. As shown, the meter is useful for square waves to 8 kilohertz, sine waves to 10 kHz, and pulse widths down to 15 microseconds. □

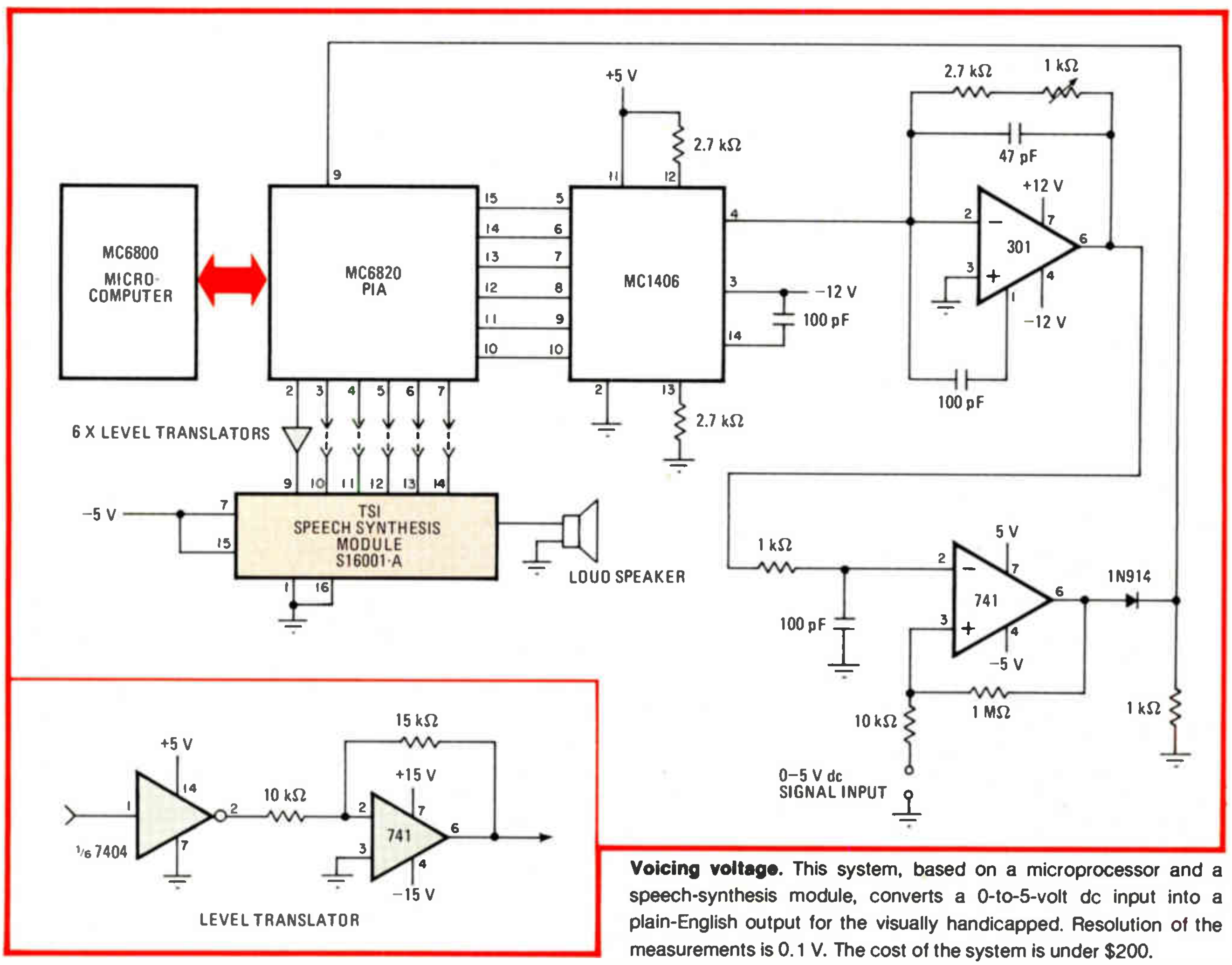
Talking meter voices dc voltage readings

by William S. Wagner
Northern Kentucky University, Highland Heights, Ky.

A relatively low-cost ($150) speech-synthesis module, combined with an interface and a small program written for Motorola's 6800 microprocessor, will convert a dc input signal of 0 to 5 volts into a plain-English output with a resolution of 0.1 V. Thus the meter will be very useful to visually handicapped technicians.

The system is configured in much the same manner as the audible voltmeter previously described, which generates a set of short and long tones corresponding to the voltage measured.[1] But in this instance, the S16001-A speech-synthesis module (from Telesensory Systems Inc., 3408 Hillview Ave., Palo Alto, Calif. 94304) serves as the output device. As a consequence, the software necessary to perform the voltage-to-audio conversion is much less, because it is handled by the synthesizer's internal circuitry.

As shown in the figure, the 0-to-5-V dc test voltage is compared with the output of the 6-bit 1406 digital-to-analog converter at the inputs of the 741 operational amplifier. If there is a voltage difference, the digital input to the 1406 is adjusted, under program control, until the voltage difference is minimized. The binary-coded-decimal word at the output of the 6820 peripheral interface adapter then represents the digital equivalent of the voltage measured. This word addresses the speech-synthesis module, which generates the corresponding voice response. Typical outputs will be heard as "three



Voicing voltage. This system, based on a microprocessor and a speech-synthesis module, converts a 0-to-5-volt dc input into a plain-English output for the visually handicapped. Resolution of the measurements is 0.1 V. The cost of the system is under $200.

6800 TALKING-VOLTMETER PROGRAM

Address	Mnemonic	Address	Mnemonic	Address	Mnemonic
0000	LDX 7F04	002B	TAB	0059	LDX FFFF
0003	STX 8000	002C	ORAB 20	005C	DEX
0006	LDX FF04	002E	STAB 8000	005D	BNE FD
0009	STX 8002	0031	LDX 0055	005F	DECA
000C	LDB FF	0034	DEX	0060	BNE F7
000E	CLRA	0035	BNE FD	0062	PULA
000F	STAB 8002	0037	ANDB 0F	0063	ANDA 0F
0012	LDX 0055	0039	STAB 8000	0065	TAB
0015	DEX	003C	LDAA 02	0066	ORAB 20
0016	BNE FD	003E	LDX FFFF	0068	STAB 8000
0018	TST 8000	0041	DEX	006B	LDX 0055
001B	BPL 06	0042	BNE FD	006E	DEX
001D	DECB	0044	DECA	006F	BNE FD
001E	ADDA 01	0045	BNE F7	0071	ANDB 0F
0020	DAA	0047	LDAB 33	0073	STAB 8000
0021	BRA EC	0049	STAB 8000	0076	LDAA 04
0023	LDS 00B0	004C	LDX 0055	0078	LDX FFFF
0026	PSHA	004F	DEX	007B	DEX
0027	LSRA	0050	BNE FD	007C	BNE FD
0028	LSRA	0052	ANDB 1F	007E	DECA
0029	LSRA	0054	STAB 8000	007F	BNE F7
002A	LSRA	0057	LDAA 02	0081	JMP 000C

point seven," "one point oh," and "oh point nine."

The 66-instruction program is fairly simple. The first four steps initialize the system. The instructions contained between addresses 000C and 0021 make up the digital-voltmeter portion of the routine, where the aforementioned comparison and minimization of voltages at the inputs of the 741 op amp take place.

At minimization, the BCD word is stored in accumulator A at location 0024, which is the second location of the speech-synthesis section of the program. The analog equivalent of the most significant digit of voltage is then voiced at location 0039.

After a short delay to allow time for the word to be read, the word "point" is brought to the module's output register at 0047 and announced at location 0054. Following a second delay, the least significant digit of voltage is similarly presented to the output register at 0068 and transmitted at location 0073. The program then returns to the digital-voltmeter section of the routine. ☐

References

1. William S. Wagner, "Digital voltmeter has audible output," *Electronics*, March 29, 1979, p. 120.

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.

Engineer's newsletter

Make the connection and keep cool

Engineers who work with Josephson junctions and other devices requiring temperatures near absolute zero will welcome a simple, repeatable method for soldering superconducting wire to cryogenic leads. Developed by W. David Lee and J. Thomas Broach of the U. S. Army Mobility Equipment Research and Development Command in Fort Belvoir, Va., the technique is particularly suited for joining a multifilament superconductor and a braided copper wire conductor when a series of samples must be tested.

Clever use of a copper tube filled with solder is the key to the method's success. For further information, write to Lee and Broach at the Fort, or phone them at (703) 664-5081 or (703) 664-5584, respectively.

There's more to digitizers than bits and megahertz

Number of bits and sampling rate are invariably the most prominent pieces of information on a data sheet or advertisement for an analog-to-digital converter. And well they should be, being important first-glance indicators of performance.

But in order to really determine whether a particular digitizer will do the job properly, you have to look at a number of other parameters—dc accuracy, gain error, linearity, and quantizing error, to name just four of them. Particularly for high-speed waveform digitizers, you need to **look at the impact of aperture uncertainty as you approach the digitizer's Nyquist frequency.** Increasing uncertainty means fewer effective bits at the high end, so that just when you need it most, an 8-bit digitizer can drop to a resolution of 4 effective bits.

Robert W. Ramirez of Tektronix Inc. has spent a lot of time lately looking at digitizer specifications, more graphically than mathematically, and to observing their effect on data, particularly in terms of dynamic performance. Contact him at Box 500, Beaverton, Ore. 97077, or call him at (503) 644-0161 to share ideas.

NBS seminars teach measurers better measurement

The National Bureau of Standards will soon be holding its 1980 Measurement Seminars at its headquarters in Gaithersburg, Md., and at its laboratories in Boulder, Colo. Each lasts from one to five days and offers a practical course in the techniques and instruments used in making precise measurements. Basically, the seminars discuss the different levels of accuracy appropriate for research work, factory production, or field evaluations and explain how measurements and calibrations can best be traced to the appropriate NBS standards. Topics to be discussed in 1980 will include micromeasurement on integrated-circuit silicon wafers, measurement at high voltage levels, the metrology of modern instrumentation, and electromagnetic interference metrology.

Because these seminars and workshops emphasize hands-on training using equipment in NBS laboratories, **enrollment is limited to individuals from measurement and standards laboratories** who must regularly make precise measurements in their work and who have the appropriate prerequisites in education and experience.

Further information on this series of NBS courses can be obtained from Joanne Marshall, Office of Measurement Services, Physics Building, Room B362, National Bureau of Standards, Washington D. C. 20234; phone (301) 921-2805.

-Harvey J. Hindin

Power transistors rated to 500 V

MOS field-effect transistors use Hexfet technology for second-breakdown freedom and ease of paralleling in switching power supplies

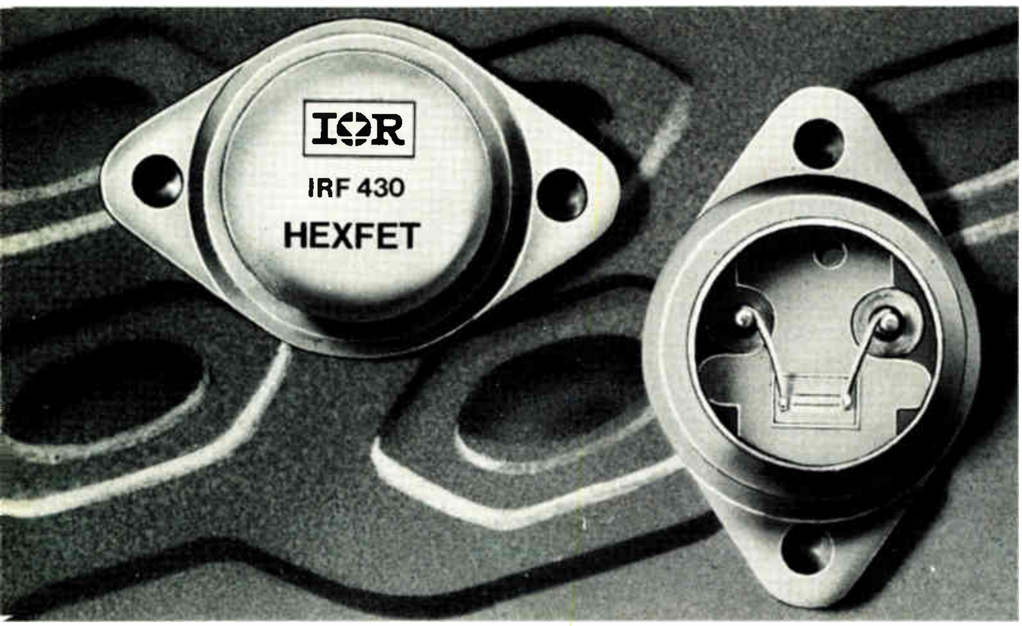
by Larry Waller, Los Angeles bureau manager

High-power transistors rated up to 500 V are now being offered as part of International Rectifier Corp.'s product line. Like the series of MOS field-effect transistors rated to 400 V and introduced earlier this year [*Electronics*, July 5, p. 209], this family of four also incorporates IR's innovative planar MOS FET technology. Called Hexfet, for a structure composed of hexagonal source cells fabricated on the silicon chip's surface, the technology has enabled the company to expand its line of power devices greatly beyond bipolar transistor capabilities.

This Hexfet implementation is basic to the high power and current ratings, with low on-state resistance, says H. William Collins, vice president for advanced products. The highest-rated of the new devices, for instance, is the IRF 430, which operates at 500 V with a continuous drain current of 3.5 A or a pulsed current of 6 A. On-resistance is 1.5 Ω.

POWER-TRANSISTOR PARAMETERS

	Source voltage, V_{ds} (V)	On-state resistance, R_d (Ω)	Continuous drain current, I_d (A)	Pulsed drain current, I_{dm} (A)
IRF 430	500	1.5	3.5	6
IRF 431	450	1.5	3.5	6
IRF 432	500	2.0	3	5
IRF 433	450	2.0	3	5



Offering the 500-V IRF family is important, Collins explains, "because it represents the continuing march of MOS FETs into power switching." MOS FET advantages over bipolar transistors include: voltage control, high input impedance, fast response, second-breakdown freedom, and ease of paralleling. "What's more, they achieve voltage, current, and power ratings equivalent to state-of-the-art bipolar transistors," Collins says.

"The prime feature of Hexfet is a low on-resistance that can be attained with a die area less than one third that possible with previous MOS FET technologies," asserts Collins. IR has developed a design and processing technique (the firm has applied for patents) that fabricates this hexagonal-cell structure to greatly increase density. The source cells are formed by a large-scale integration process that gives a density of over 500,000 cells per in.^{2} "It is actually LSI masquerading as a power device," he explains.

Collins expects the 500-V series to supplement, rather than supplant, IR's 400-V devices, with big initial interest coming from manufacturers of off-line switched-mode power supplies. Although many such firms are already designing circuits with existing 400-V IR devices, the higher ratings will give better safety margins in guarding against transients and wide swings of input voltage. This is particularly true for the export market, where higher voltages are usually employed, according to Collins. Also, with the 500-V family, circuits may be simplified and equipment ruggedness improved. The higher power rating opens up wider use in motor controls, besides such applications as inverters, choppers, audio amplifiers, and high-energy pulse circuits.

Key electrical characteristics include a minimum gate threshold voltage of 1.5 V (3.5 V maximum), a typical off-state drain current of 0.1 to 0.2 mA (1.0 to 4.0 mA maximum), and a forward transconductance of 1.5 to 2.5 siemens. Also, input capacitance, which limits the response time, is 700 pF typical, 900 pF maximum.

The maximum power dissipation for all of the four devices is 75 W; the operating and storage temperature ranges are −55° to +150° C. All the units are available in standard TO-3 packaging.

At the moment, IR has the highest-rated commercial power MOS FET, according to Collins, but he expects competitors to challenge IR soon. Industry sources confirm that Siliconix, the first U. S. manufacturer of power MOS FETs, is readying a higher-rated line, said to approach IR's. Intersil, Texas Instruments, and others are also pushing to get new entries into this 400-V-and-up market. These firms are already selling lower-rated MOS FETs, which were available before IR's.

Filling in the gaps. IR's strategy is one of leapfrogging existing competition with high-power devices to demonstrate its own technology and then filling in lower-power levels later, Collins says. Although still higher ratings are possible with Hexfet, no such upward extensions are currently planned. "Our existing line now will satisfy 75% to 80% of the power switching market," he estimates.

The new line, to be available initially in small quantities with a four-to-six-week delivery, is not finally priced, but will go at somewhat higher levels than the 400-V series. A 500-V device, for example, will sell for $22 to $28, in quantities of 1 to 9, compared with equivalent 400-V units in quantities of 100 or more for $16.70 to $21.30 apiece.

International Rectifier Corp., Semiconductor division, 233 Kansas St., El Segundo, Calif. 90245. Phone (213) 772-2000 [338]

Computers & peripherals

System links host, LSI-11s

Interprocessor offers DMA, programmed I/O link from host to six satellites

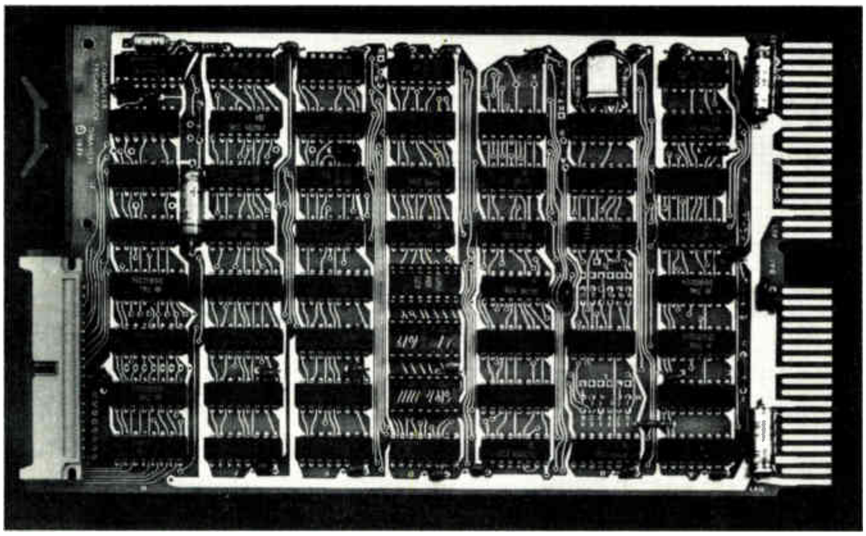
The cost of distributed processing has taken a quantum leap downward, thanks to an interprocessor from the Computer Technology division of Peritek Corp. It is the HEX-L11, a two-board linking system that interfaces a host computer with as many as six of Digital Equipment Corp.'s LSI-11 computers in a radial formation.

"The HEX-L11 can reduce the hardware cost of our targeted customer's system by as much as 50% to 65% and perhaps more," asserts Thomas Birchell, Peritek's vice president of marketing. "It opens up distributed processing applications that were previously simply too expensive to implement."

The HEX-L11 is unlike competitive interprocessors in that it creates a direct-memory-access link between the host processor and a multiplicity of satellites. DEC's DAV-11B, for example, creates a DMA link between a host computer and a satellite, but extra satellites must be placed on a serial data link. "Using very conservative numbers, I don't think anything else on the market can duplicate the work of the HEX-L11 for under $10,000," Birchell notes. In a six-satellite configuration, the system sells for $4,455, with cabling extra. It sells for $3,075 for a three-satellite system, and $1,596 for a binary link.

DMA, programmed I/O. Since it can support both programmed input/output and direct memory access, the HEX-L11 is uniquely suited for handling a mixture of short and long data blocks. The programmed I/O can be used for binary flags and for data blocks up to three words long, and the DMA can be used to transfer longer data blocks at a rate of over 100,000 16-bit words/s. By using a DMA link to transfer the large data blocks, the HEX-L11 greatly reduces the interrupt overhead required of the host.

Initially, the HEX-L11 will be available only in a Q-bus format, but a Unibus-compatible HEX-L11 will be forthcoming in the third quarter of 1980. Whichever bus is used, the HEX-L11 provides intermediate data buffers, as well as control and status registers and special "mailbox" registers for both the host and the selected satellite computer. The control bits within these mailbox registers synchronize the system's operation by locking in the selected satellite and excluding the others. Each satellite, however, has its own interrupt flag bit in the satellite interrupt register of the HEX-L11. These flags interrupt the host's servicing of one satellite in order to alert it to a higher-priority request from another. They will also signal the host when the selected satellite's operation is completed.



The HEX-L11 is especially useful with LSI-11/2s, not just because these computers are inexpensive, but also because the 18-bit interprocessor can quadruple the 16-bit addressing capability of the LSI-11/2. Thus, each LSI-11/2 satellite may be extended from 64 kilobytes of random-access memory to 256 kilobytes. If the host is an LSI-11/2, it can communicate with its own extended RAM by treating it as a satellite of the HEX-L11.

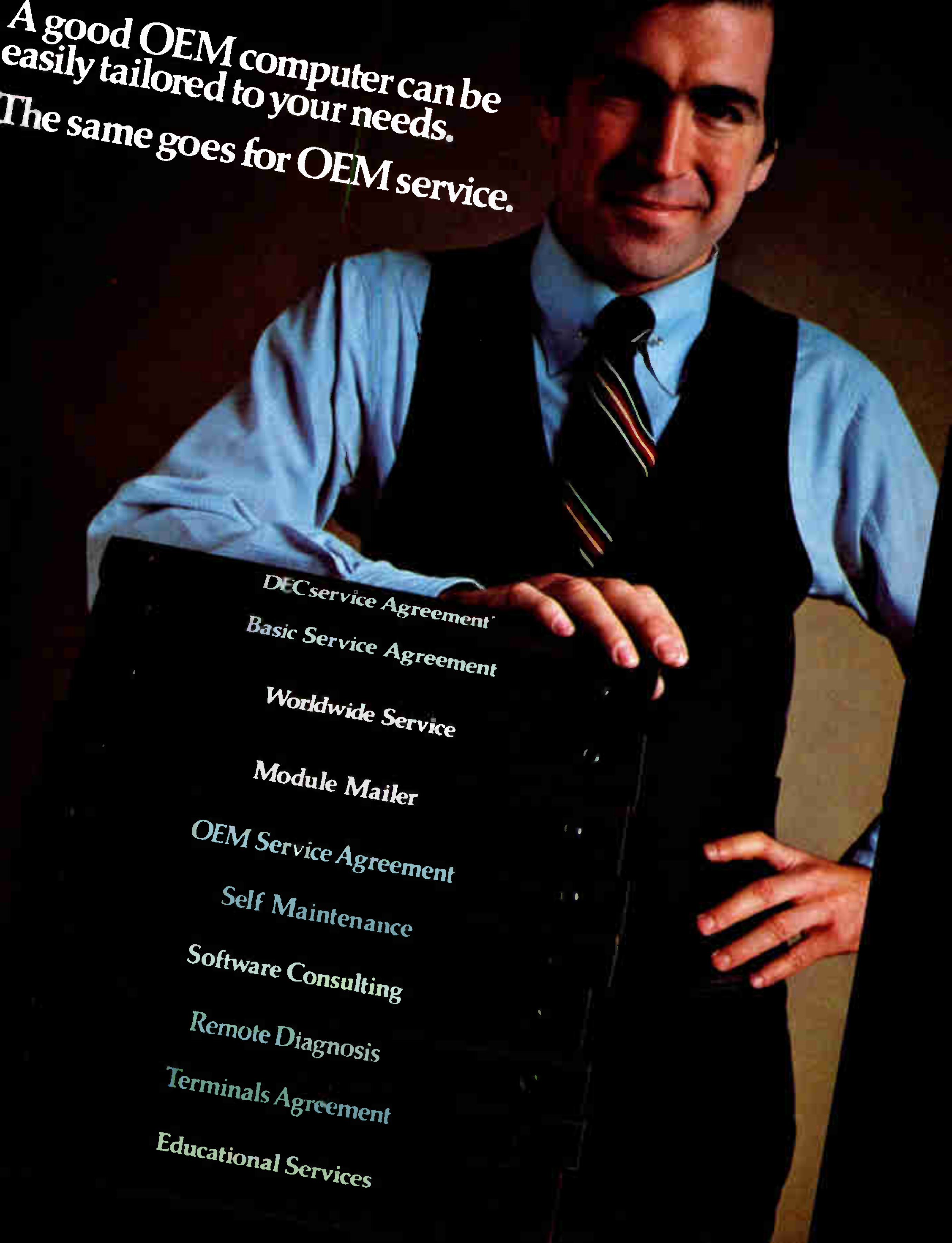
Those using the PDP-11/2 as a host computer will be pleased to note that the boards of the HEX-L11, which reside in the host, conform to a double-height form factor, so that no special allowance for a quad-height card need be made.

What the HEX-L11 does not provide is a serial interface. It can be augmented, however, by separate purchase of DEC's DLV-11 serial interface units. Although an automatic bootstrap capability is designed into the DMA-L11 cards that are part of the HEX-L11 subsystem, the necessary complexity of a six-satellite system can dictate extensive status checking and other refinements during the bootstrap operation. Much of this can be avoided by sending a small bootstrap program from the host to the satellites through the serial link.

The company believes that uses for the HEX-L11 can only begin to emerge when deliveries of the product start in late January, but two test cases have already provided what may become typical examples. In one, the LSI-11 satellites are used as signal conditioners in a scientific data-acquisition system. In the second, the satellites are used as concentrators that form a two-way link over a cable TV network.

Peritek Corp., Computer Technology division, 3014 Lakeshore Ave., Oakland, Calif. 94618. Phone (415) 465-9000 [361]


DIRECTION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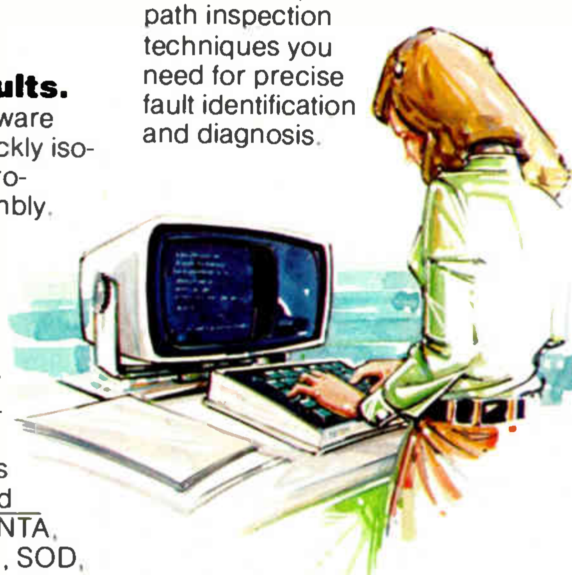

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The First Family of ATE

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Industrial

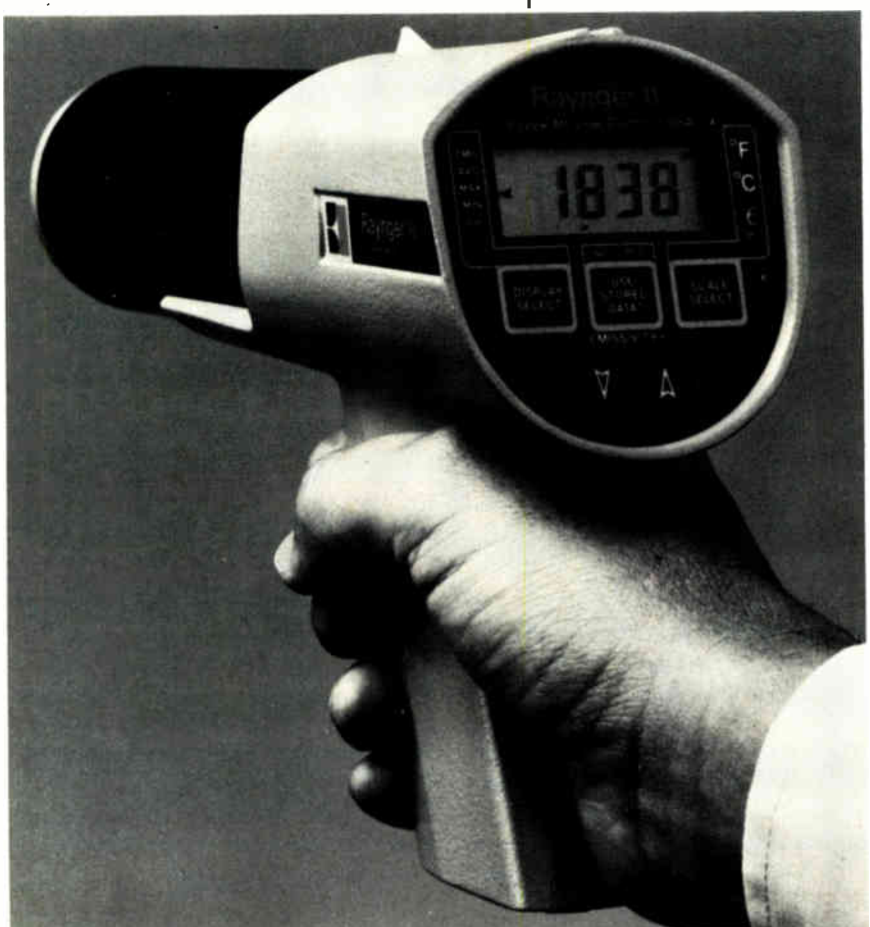
Temperature gun has intelligence

Noncontact thermometer has microprocessor for accurate, wide-range, infrared readings

The microprocessor has been put to use in yet another measurement instrument: the Raynger II hand-held digital temperature-measuring gun, which is the first noncontact temperature gun with intelligence. The battery-operated unit includes measurement capabilities generally found only in larger and more expensive temperature data systems.

Based on Intel's 8048 microprocessor, the Raynger II's microprocessor provides a number of measurement functions over a wide temperature range. The gun's panel has touch-operated membrane switches and a four-digit liquid-crystal display. The gun is easy to operate: a user simply aims it at the target to be measured, pulls and holds the trigger, and the temperature data is displayed instantly on the LCD. The target can be as close as a few inches or as far away as several hundred feet.

Any one of five types of data may be displayed at a touch: the target's radiated temperature, its average temperature, its maximum and minimum temperatures, and a differential temperature value for two radiating surfaces. The Raynger II may display—accurate to within 1%—readings either from −20° to +200°F or from −30° to +1,100°C. Regardless of the type of scale employed to make the measurement, the memory-stored data can be instantly displayed as either Fahrenheit or Celsius values.



The self-calibrating instrument makes four temperature readings per second. It corrects for an object's emissivity factor in one of two ways. (The emissivity factor compares the amount of infrared energy reflected from a surface to the energy level radiated from it.) If the emissivity factor of the surface to be measured is known (from a table of values), the operator inserts this value into the gun, before making a measurement, through an appropriate up-and-down-ranging emissivity switch. The Raynger II then automatically adjusts its measurement readings.

If the emissivity value is not known, the operator can calibrate the instrument by pointing it at a standard target whose emissivity is known. The gun is pointed at the target and a measurement is made. The gun then calculates and displays the unknown emissivity factor.

The Raynger II is designed to monitor product and process temperatures directly. It can also be used in preventive maintenance procedures by monitoring electrical-circuit panels, bearings, heaters, and steam lines and traps in large processing plants. It sells for approximately $1,595. Deliveries are scheduled to begin by late March 1980.

Raytek Inc., 325 E. Middlefield Rd., Mountain View, Calif. 94303. Phone Bob Mangold at (415) 961-1650 [371]

CCDs operate in imaging or line-scanning modes

Two charge-coupled imaging devices can be operated in either of two modes—as area imagers, much like a camera, or as line scanners. One of the CCDs has 1,024 picture elements and the other has 10,000 pixels. Called Omneye, the units are designed for use in sizing, orienting, identification, and other control functions. The output of the Omneye CCDs operating as imagers is a series of pulses with the height of each pulse proportional to the intensity of the light incident on the associated pixel. As line scanners, they have time delay and integration—valuable when images are moving and maximum response with low noise is necessary. With an analog-to-digital converter, the image can be converted to data compatible with digital computers.

The HCCI-032A has a 32-by-32-element imaging array and the HCCI-100A has a 100-by-100 array. Respectively, they provide 32 and 100 stages of time delay and integration. Both are illuminated-register frame transfer CCDs with a buried n-channel and a transparent polysilicon gate structure. As imagers, the CCDs offer three modes of readout—burst mode, strobe illumination, and time-delay integration. Four-phase clocking is used in the devices and both input and output registers contain an on-chip two-stage amplifier with a 3-MHz maximum output rate. Instantaneous dynamic range ratio is 700 to 1. A 100% perfect 100-by-100 CCD array sells for approximately $1,400.

Hughes Industrial Products Division, 6155 El Camino Real, Carlsbad, Calif. 92008. Phone (714) 438-9191, Ext. 335 [373]

Miniature linear actuator weighs 0.5 ounce

A linear actuator with an overall diameter of 0.375 in. weighs only 0.5 oz. The miniature actuator's stroke is 0.100 in., which gives it an overall length of 1.750 in. extended and 1.650 in. retracted. The unit has an inner member that weighs 0.14 oz with a permanent magnet. The housing has coils that generate a variable magnetic field, which can be reversed, making the unit bidirectional. Force is proportional to current, with a peak force of 1.3 oz, a maximum continuous force of 0.5 oz without cooling, and a force constant of 5.5 oz per ampere. Resistance at 25°C is 65 Ω. The actuators sell for $500 apiece, with delivery set for 10 to 12 weeks.

Kimco Inc., 1045 Linda Vista Dr., San Marcos, Calif. 92069. Call Jack Kimble at (714) 744-5672 [377]

Computer compresses traced shape data

The Automatic Parts Programming System (APPS) consists of a computer that can calculate frequently changing radii rapidly and pass the information to a numerical control program. To operate, a user simply traces a two-dimensional drawing or model with the stylus of a digitizer included in the system package. The APPS computer accepts Z and Y coordinates from the digitizer, smoothes out the tracing, analyzes the points, and generates a sequence of circular interpolations and straight line commands that will reproduce the trace; every traced point does not require a separate command. APPS can scale up or down by any factor entered on the keyboard.

APPS can also serve as a regular computer- and part-programming center. It has Digital Equipment Corporation's PDP 11/03 with 32-K words of main memory, plus dual floppy-disk memory. Each disk provides half a megabyte of storage. The computer can handle Fortran, Basic, the maker's own N/C Teco language, word-processing, and business data-processing programs, as well as the automatic parts program. Software rights for this program can be bought separately. APPS can be connected directly to a machine tool to eliminate tape handling.

The system, which includes the digitizer, computer, and interfaces, sells for under $30,000, with delivery set for 60 days unless basic components are unavailable.

Alden N/C Div., 2 Mercer Rd. Natick, Mass. 01760. Phone Robert Witten at (617) 655-6610 [378]

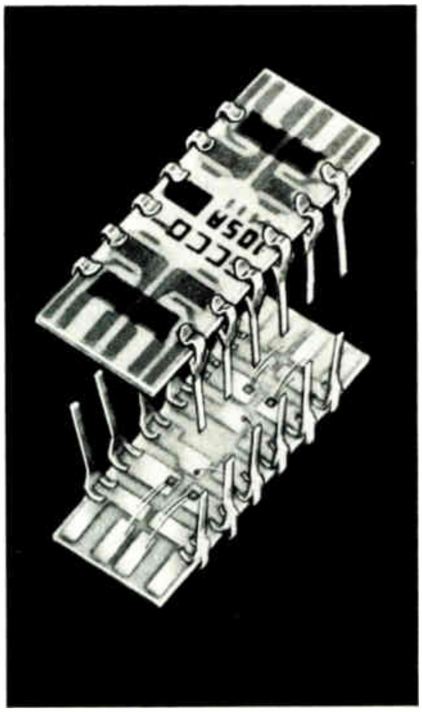
Communications

Crosspoint switch does it with light

Optically based unit uses LEDs, SCRs to improve telephone switching matrixes

Optically coupled crosspoint switches promise lower cost, better performance, and easier hookup than electrically triggered solid-state devices currently used for telephone switching systems. Theta-J Corp. claims it is the first out of the laboratory with such devices and is aiming its OCP series of single-circuit, optoelectronic switching devices at applications in space-division switching control (as in private branch exchange systems) and in telephone test equipment.

The units are fabricated on both sides of a hybrid substrate. One side of the thick-film microcircuit contains two light-emitting diodes and four independent, photosensitive silicon controlled rectifiers. Bonded to the reverse side are four multilayer resistor/capacitor transient-suppression networks—one for each SCR.



Each light-emitting diode activates a pair of SCRs using light signals coupled by reflection through a clear silicone film. Breaks in the film isolate the two sets of LEDs and SCRs from each other. The patented scheme, says Theta-J president Edward T. Rodriguez, eliminates the need for careful alignment of separate LED and SCR chips, a problem encountered by other researchers [*Electronics*, March 1, p. 41]. A standard 14-pin dual in-line package houses each of the units.

100 lines. Telephone switching matrixes using the OCP modules could handle up to about 100 lines, Rodriguez estimates, before time-division switching with a microcomputer becomes a more attractive alternative. He adds that since at least 75% of U. S. companies employ fewer than a hundred people, that limitation is not troublesome. The microcomputer-compatible OCP modules can operate in a time-division switching system, too.

Optically coupled devices, unlike electrical ones, can work at low impedances that are compatible with existing telephone circuitry and therefore do not require associated amplifiers or impedence-matching devices [*Electronics*, Oct. 11, p. 43]. Since the OCP modules would not connect electrically with a phone system, Rodriguez notes, users avoid having to meet extensive Federal Communications Commission requirements for systems hooking up to Bell System equipment.

Another advantage of optical coupling is high isolation between signal and switching paths, eliminating current leakage that causes noise in telephone voice channels. The OCP devices protect against power surges with an input/output isolation of 2,500 V ac. The input current requirement is 15 mA. Two models are available; the OCP2 and the OCP2H, with SCR ratings of 60 V and 300 V dc, respectively.

Prices are $2.50 each for the OCP2 and $3.25 each for the OCP2H, in lots of 10,000 or more. Delivery takes two to four weeks after receipt of order.

Theta-J Corp., 208 West Cummings Park, Woburn, Mass. 01801. Phone (617) 935-7600 [401]

Solid-state source delivers 50 mW across Ku band

Model DMS-12418 is an yttrium-iron-garnet–tuned broadband oscillator that covers the Ku band—12.4 to 18 GHz. Without amplification, it supplies a minimum of 50 mW, 60 mW typically, into 50 Ω over the full band. Frequency sensitivity is 15 MHz/mA ±0.15%. Maximum harmonic content is 20 dB below the carrier frequency; other spurious outputs are 60 dB down. Operating temperature range is 10° to 50°C. The source is priced at $1,800 and is available within 90 days after receipt of order.

Weinschel Engineering, One Weinschel Lane, Gaithersburg, Md. 20760. Phone (301) 948-3434 [404]

Fiber-optic link goes from dc to 200 kilobits/s

A low-speed TTL-compatible fiber-optic data link that uses a nonreturn-to-zero format with no coding restrictions operates from dc to 200 kilobits per second. The link has a bandwidth of 100 kHz and is available with cable up to 150 meters long in a flat version and up to 1 km long in a round version. The manufacturer is offering a one-year limited warranty on the system. Like all optical links, this one offers protection against electromagnetic interference as well as complete electrical isolation. Each link consists of two transceiver modules that are thin enough to be used in a card cage and a preterminated flat or round duplex cable. Interconnection is through standard 3M printed-circuit-board headers.

The link uses two discrete, low-loss, plastic-clad silica fibers in a polyvinyl chloride jacket, allowing simultaneous transmission and reception of data. Typical cable attenuation is 25 dB per km, and connector attenuation is less than 2 dB per mated pair. The link requires a +5-V dc power supply. By connecting a jumper from the power supply to the module, data can be transmitted beyond 200 meters.

Each transceiver module has a gallium arsenide infrared light-emitting-diode as a light source and a p-i-n photodiode light detector. The complete data link without the cable costs $228. Reinforced pre-terminated duplex cable is $4.10 per meter. The data link comes fully assembled and tested. Delivery time is approximately eight weeks after receipt of order.

3M Co., Dept. EP9-19, Box 33600, St. Paul, Minn. 55133. Phone (612) 733-9214 [403]

Doppler transceivers sell for $40 each

A $40 X-band transceiver for continuous-wave doppler radar systems comes in two models that are preset in the factory at 10.525 GHz and meet Part 15 of the Federal Communications Commission's regulations. The units can be used in industrial process controls and in speed and motion-detection systems. The die-cast units consist of a stable 10.525-GHz Gunn oscillator for the transmitter and a sensitive Schottky-barrier mixer diode for the recovery of the doppler-shifted frequencies. The model GDHM1 operates at 8 V, 90 mA, and yields a mixer output of 20 μV for a return signal 100 dB below the transmitted signal. The GDHM2 operates at 8 V, 140 mA, and yields an output of 30 μV.

The units can be supplied with other internationally allocated frequencies at the customer's request. The company says the transceivers will meet the harmonic emissions standards of the major industrial nations. Any standard X-band horn may be used with these transceivers. By installing an additional mixer at the factory (at extra cost), the transceivers can provide phase information to enable the user to determine the direction of a target. The $40 price holds for the transceiver ordered in quantities of 50 to 90 units. Plessey's ANT 160 series horns that offer a gain choice of 10, 12, and 15 dB are available at $8 each. The transceivers and horns are delivered from stock.

Plessey Optoelectronics and Microwave, 1641 Kaiser Ave., Irvine, Calif. 92714. Phone (714) 540-9934 [405]

GaAs FET features 3.3-dB noise, 5.0-dB gain at 18 GHz

An unpackaged gallium arsenide n-channel metal semiconductor field-effect transistor has noise figures of 3.3, 2.5, and 1.9 dB with associated gains of 5.0, 9.0, and 11 dB at 18, 12, and 6 GHz, respectively. The transistor is designed for high-gain, low-noise amplification in both wideband communications and radar amplifiers.

The model AT-8060 is a packaged version of the transistor, recommended for operation up to 12 GHz. It comes in a 50-mil² metal and ceramic stripline package that minimizes parasitic reactances and is suitable for X-band microstripline circuitry. The unpackaged version, model AT-8061, operates at up to 18 GHz. This 10-by-14-mil chip uses gold exclusively for its metalization, so that it offers good bond strength and is compatible with the wire-bonding techniques used in both thin- and thick-film microwave hybrid-circuit construction.

The two versions have relatively constant insertion power gain, maximum available gain, and noise-figure characteristics over a wide range of drain current levels, all of which simplify the bias design of amplifiers using the GaAs FETs.

In small quantities, the packaged transistor, AT-8060, is priced at about $130, and the AT-8061 unpackaged chip is about $120. Both versions of this GaAs FET device are available as off-the-shelf items.

Avantek Inc., 3175 Bowers Ave., Santa Clara, Calif. 95051. Phone (408) 249-0700 [406]

Semiconductors

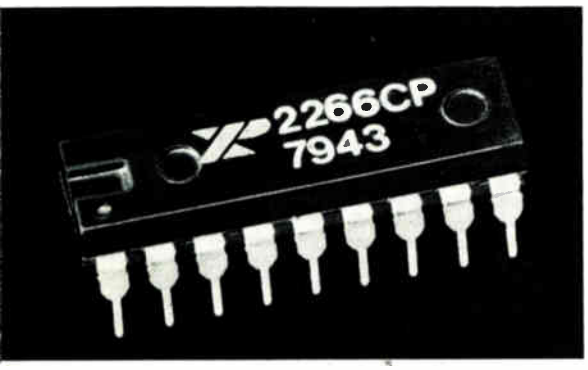
Monolithic IC drives toy cars

Chip puts sense, drive, and decoder functions for remote control into single package

Perhaps the hottest items on toy department shelves this Christmas are remotely controlled toy automobiles. They vary from a prototype Porsche racing car to a miniature Peterbilt truck, but they all have one thing in common: they could use the XR2266 integrated circuit from Exar Integrated Systems Inc. Housed in an 18-pin dual in-line package, this IC combines both the decoder and the sense and drive functions and though not available this year, it should be in many of these toys by next Christmas.

"This chip addresses a market that will sell 5 million remote-controlled cars next year," says Exar vice president Alan Grebene. "Three million will be in the under $60 price range, and another 2 million will be in the $150-and-up range."

Steering speed controls. The internal ±350-mA output drive capability of the XR2266 lets it drive the steering servo of the car directly. It also directly drives the backup lights and turn signals, giving a car an aura of even greater sophistication. To provide enough power for the forward and backward speed servos, however, external power transistors must be added.



The XR2266 combines low-power integrated injection logic (I^2L) with precision analog circuitry; it runs on supply voltages of 3.5 to 8 V. Besides its steering and speed-control servo circuitry, it has reverse detection circuitry that drives the back-up lights and steering-window (dead-band) detection circuitry that drives the turn signals, plus channel divider and integrator circuitry that demodulates the incoming signal and separates the steering-control information from the speed-control information.

"With the XR2266," notes Grebene, "we have cut the circuitry necessary to remotely control a racing car by at least a factor of two. When you compare this IC with discrete circuitry, it shows at least a four or five times improvement."

The XR2266 is priced at $4.45 each for orders of 100 units or more and at under $2 each in mass-production quantities.

Exar Integrated Systems Inc., 750 Palomar Ave., Sunnyvale, Calif. 94088. Phone (480) 732-7970 [411]

3- to 8-W amplifiers sell for $1.50 to $2.05

The members of a six-type family of integrated-circuit audio power amplifiers are available in prices ranging from $1.50 to $2.05 each in 1,000-piece lots. The devices are suited for such applications as radio and TV receivers, tape recorders, and stereo equipment. All the units offer two-channel or one-channel connection to a speaker with no need for a transformer. The units come in plastic dual or single in-line packages. The single-channel DIP amplifiers have outputs of 3.0 to 15.5 W with a voltage of 20 to 24 V, whereas the two-channel devices range from 1 to 7.5 W per channel with the same voltages. The single-channel SIP amplifiers provide from 5.5 to 18 W at voltages ranging from 13.2 to 24 V. Deliveries take up to eight weeks.

Panasonic Co., One Panasonic Way, Secaucus, N. J. 07094. Phone Bill Bottari at (201) 348-7276 [419]

High-speed multiplexers have two operating modes

The newest members of Harris Corp.'s family of monolithic analog multiplexers far outstrip any other devices of their kind in speed and accuracy, claims Frank R. Cooper, supervisor of data-acquisition design. Both models require 90 ns to open a channel and 800 ns to settle to within 0.01% of final value. The 8-channel HI-518 and the 16-channel HI-516 use 3-bit and 4-bit addresses, respectively, in randomly accessing channels for high-speed data acquisition.

Channel-switching charge injection is less than 0.3 picocoulomb for both models, suiting them to low-level, high-impedance applications such as direct sensor-output switching in industrial process control, says Cooper. Other applications will include military and avionics uses, he adds.

Manufactured using an advanced, dielectrically isolated silicon-gate complementary-MOS process that allows inclusion of bipolar and MOS devices on the same chip, the multiplexers are compatible with both TTL and complementary-MOS. They can operate in either single-ended or differential modes; in the latter, they address pairs of channels and have two outputs. Input/output leakage current is less than 100 pA. Channel-to-channel off-isolation is very good—86 dB at 500 kHz and 75 dB at 1 MHz.

A 28-pin ceramic dual in-line package houses the HI-516; the HI-518 comes in a similar, 18-pin package. Operating temperature ranges for the multiplexers are 0° to 70°C for commercial versions and −55° to +125°C for military versions.

In lots of 100 or more, commercial versions of the HI-518 and HI-516 each cost $11.71 and $22.50, respectively. Military models cost $24.18 and $45, respectively. Delivery is from stock.

Harris Corp. Semiconductor Division, P. O. Box 883, Melbourne, Fla. 32901. Phone (305) 724-7538 [412]

Packaging & production

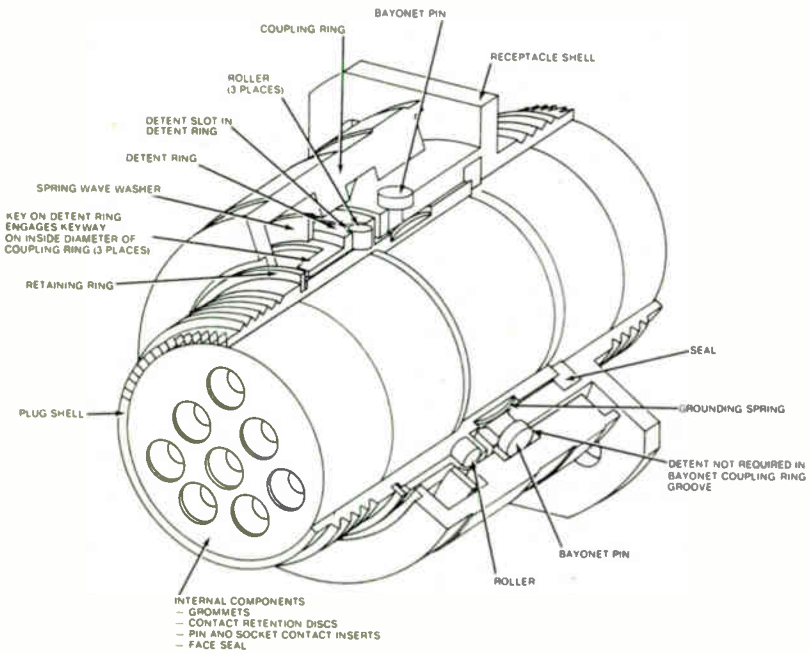
Plug doubles connector life

Unit uses detent ring instead of bayonet holes for better emi resistance, too

Users who thought that upgrading their Series I connectors to meet the requirements of MIL-C-38999 Revision G would require replacing both plugs and jacks were only half right. The Super Series I plug connector meets the shock, vibration, and interference requirements of the new specification with no need to replace the receptacles. The new plug utilizes a coupling design that doubles lifespan to 500 mating and unmating cycles.

It does this by eliminating the bayonet holes normally found on bayonet coupling rings and using instead a stainless-steel detent ring at the rear of the coupling ring. Eliminating the bayonet holes also improves the connector's resistance to electromagnetic interference and prevents the possible intrusion of dirt and moisture. A third benefit of the new design is that the plug produces an audible click whenever it mates—an important convenience for repairmen who must often make blind connections.

Like other military-type connectors, the Super Series I units have self-sealing rear grommets, closed-entry hard-front socket inserts, and rear-release removable contacts. The scoop-proof design protects pins from damage during blind mating. Existing backshell hardware, such as cable clamps, radio-frequency adapters, and withdrawal tools are interchangeable between the Series I and the Super Series I.



Amphenol offers the new plug in 29 insert configurations in shell sizes 9 through 25 and six shell styles, including straight plug, wall mount, jam nut, and box mount.

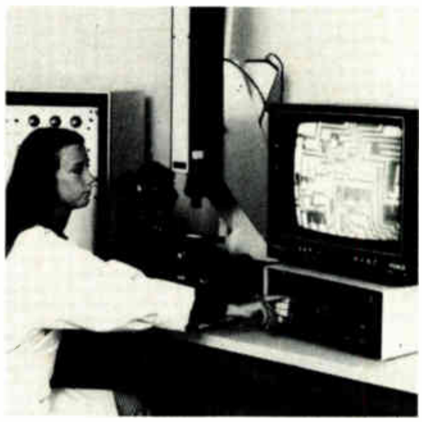
Prototype quantities are available now, with production quantities to be available next year. Prices will be comparable to those of the Series I.

The Amphenol North America Division of Bunker Ramo Corp., 2122 York Rd., Oakbrook, Ill. 60521. Phone (312) 986-2700 [391]

Turnkey system for automated soldering costs $30,000

A $30,000 turnkey laser system is capable of computer-controlled soldering of small and microscopic components. Called the LMS-1 laser microsoldering system, it is designed for such uses as soldering fine insulated or stripped wires onto small solder pads automatically or semiautomatically or soldering wire-wrapped pins onto circuit boards. The LMS-1 can also fuse fiber optics, scribe ceramics, cut and slit dielectrics, and cure and drill a variety of materials.

The system is a work station that includes a flowing-gas industrial carbon dioxide laser, an X-Y work table, a fully programmable microprocessor controller, and a binocular viewer. The laser is nominally rated at 20 W and is mounted vertically over the numerically controlled X-Y positioner. A beam-locating coaxial light pointer and a high-resolution closed-circuit TV system are avail-



able as options. The company says that the $30,000 price tag is the lowest for any available automated laser soldering system. Delivery takes 90 days.

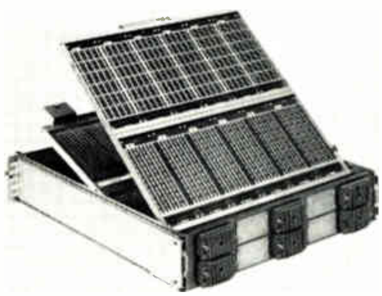
Apollo Lasers Inc., 6357 Arizona Circle, Los Angeles, Calif. 90045. Contact Stanley J. Parnas at (213) 776-3343 [394]

Dual-plane drawer houses four full socket panels

Two 16-pin pattern or universal pin socket panels fit in each plane of a dual-plane packaging drawer for a total of four full panels. The high-density model LPD-11 provides from 30 to 720 integrated-circuit positions, depending on the size of the IC, with up to 1,200 input/output connections.

With the company's dual-contact interconnection panels, a user may choose face-wipe or edge-wipe interfacing between the wrapped-wire pin socket and the IC-lead frame. The panels are mounted with the pin sides facing each other on hinged frames for simple interpage wiring. I/O panels come with cutouts for 1 to 10 connectors. If there are no connectors, the panel cutouts can be protected by a cover provided by the manufacturer. The front panels of the drawers have mounting surfaces for switches, meters, lights, and other accessories. Both single- and double-plane drawers are available with slides and handles and with or without installed socket panels. The dual-plane drawer lists for $270, and the single for $196.

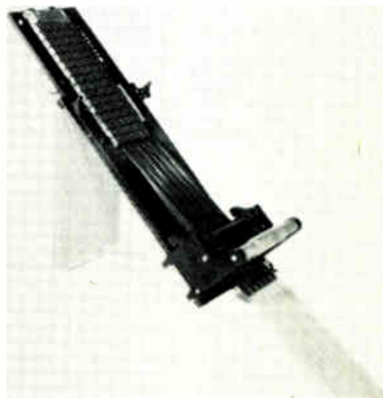
Scanbe Division of Zero Corp., 3445 Fletcher Ave., El Monte, Calif. 91731. Phone Elvira Nagle at (213) 579-2300 [396]



$3,950 tool removes ICs from burn-in board sockets

An "Un-loader" tool priced at $3,950 has been designed for the rapid removal of integrated circuits from sockets mounted on burn-in boards and trays. The model 1217 is capable of removing more than 6,000 16-lead ICs per hour and is specifically designed for removal of ICs in Robinson-Nugent model S2 0.300-in. center dual in-line package sockets. Other models are available to handle most IC sockets in current use.

The device removes ICs, even from high-density boards, without bending leads or damaging packages. A simple hand action moves a counterbalanced moving carriage with replaceable unloading fingers over the board, and as the ICs are removed,



they are gravity-fed into reservoirs. The reservoirs hold the ICs until removal, or the unit may automatically pass them to carrier tubes that can be attached to the end of each reservoir.

The un-loader tool weighs 30 lb and is bench-mounted. It measures 24.5 by 27 by 13 in. without carrier tubes. Since each board is grounded to the tool, there is no danger of static damage to MOS or complementary-MOS devices. Delivery takes six to eight weeks after receipt of order.

Reliability Inc., P. O. Box 3709, Houston, Texas 77036. Telephone (713) 492-0550 [397]

Demo kit aids programmers of M6805 microcomputer

Designed to give users more expertise in programming the M6805 microcomputer family, the SCPROM03 demonstration kit from Motorola Inc.'s Integrated Circuits division is assembled using an MC6805P2P1 microcomputer, together with optional components mounted in a small circuit board in up to 10 different configurations. **By using the available random-access memory and the subroutines present in the read-only memory, the programmer can configure the various components to operate in three main modes.** The monitor mode allows the processor to be connected directly to a terminal running at 300, 1,200, or 9,600 bauds; the games mode tests the user's memory skills in following tone-sequence routines generated by the microcomputer; and an on-chip self-check mode can be initiated to verify whether the processor is operational or not. The Austin, Texas, division sells the kit for $29.95.

Intersil expands V-MOS FET line

Intersil Inc., Cupertino, Calif., will be introducing 30 additions to its V-groove MOS field effect transistor line. **The new devices are function-for-function and pin-for-pin replacements of a number of V-MOS power FETs from Siliconix Inc.** The power device families that are being replaced include: the VN30A, 35A, 46A, 66A, 67A, 88A, 90A, 98A and 99A. Applications for these units cover switching power supplies, dc-to-dc inverters, high-current analog switches, laser diode pulsers, logic buffers, and pulse amplifiers, among others. The devices will be available from stock in metal can TO-3 and TO-39 packages, as well as in plastic TO-202 encapsulations. Prices at the 100-piece level range from 78¢ to $5.81 each.

HP improves thermal printer . . .

Hewlett-Packard Co., Palo Alto, Calif., is preparing to introduce two recorders that considerably advance the image quality obtained from thermal printing. **The recorders use a soft platen made of a new material that does not act as a heat sink as the head moves across it.** As an indicator of the recorders' printing quality, the units, which will be available in January, will offer black-on-white printing, as well as the traditional blue-on-white.

. . . and betters microwave detector

HP is also offering a general-purpose microwave detector, the model 420C, that boasts improved specifications over the model 420A detector discontinued several years ago. The model 420C, covering the range from 10 MHz to 12.4 GHz, **has a ±2-dB frequency response, a maximum sensitivity of greater than 0.15 mV/μW, and a 2:1 standing-wave ratio.** Corresponding figures for the 420A were: ±3 dB, more than 0.10 mV/μW, and 3:1. The new detector will sell for $110, with delivery in four weeks.

Price changes

The SMG switching power supplies from **the Electronic Power Supply division of Gould Inc., El Monte, Calif.,** now sell for up to 12.5% less. . . . Prices on light-emitting-diode panel lights have been cut 20% to 35% by **Data Display Products, Inglewood, Calif.** . . . A 30% price reduction on miniature inductors from **the Millen Components division of E. I. & S. Corp., Winchester, Mass.,** was recently announced.

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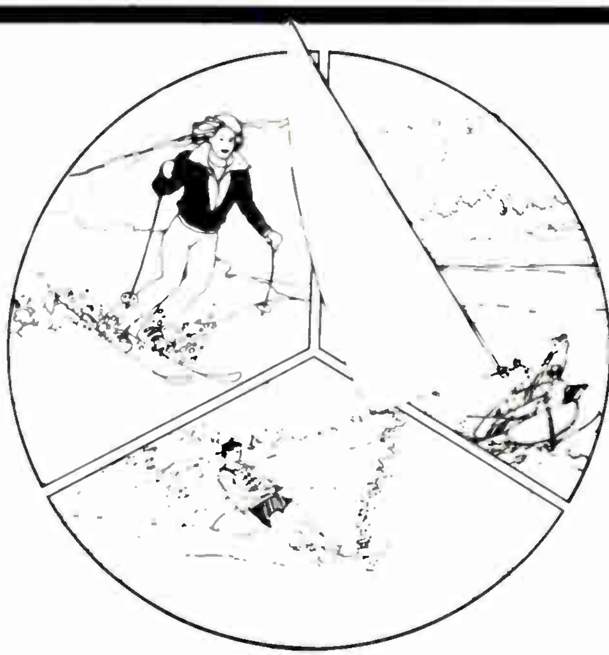

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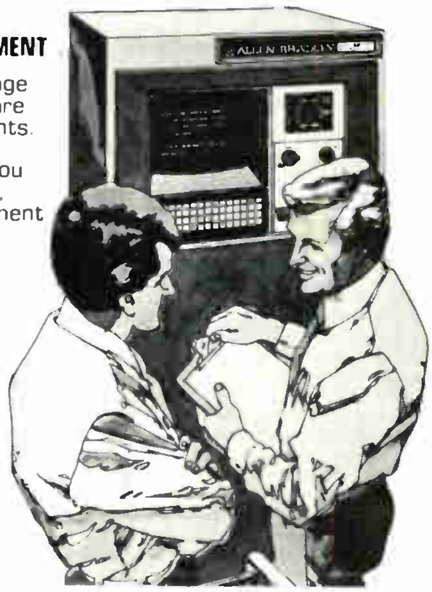

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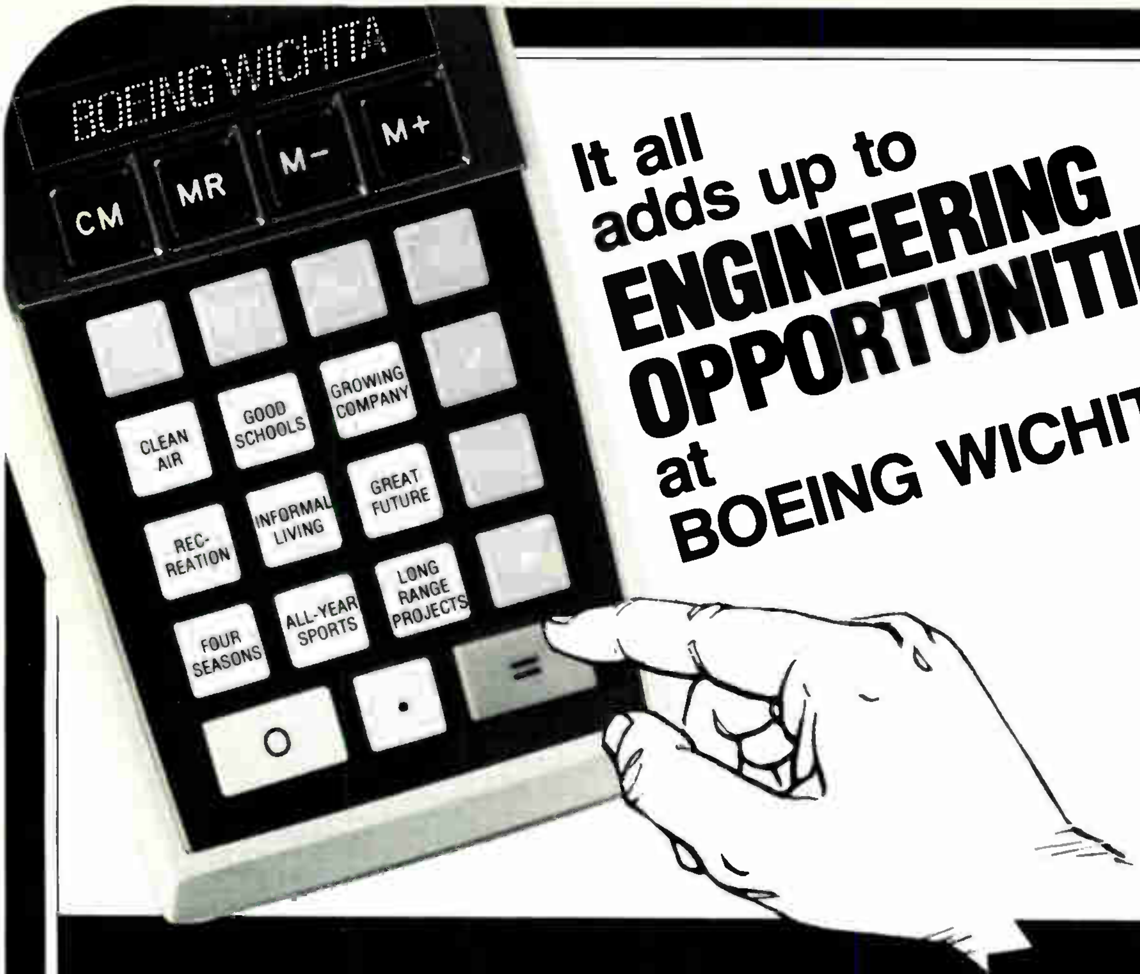

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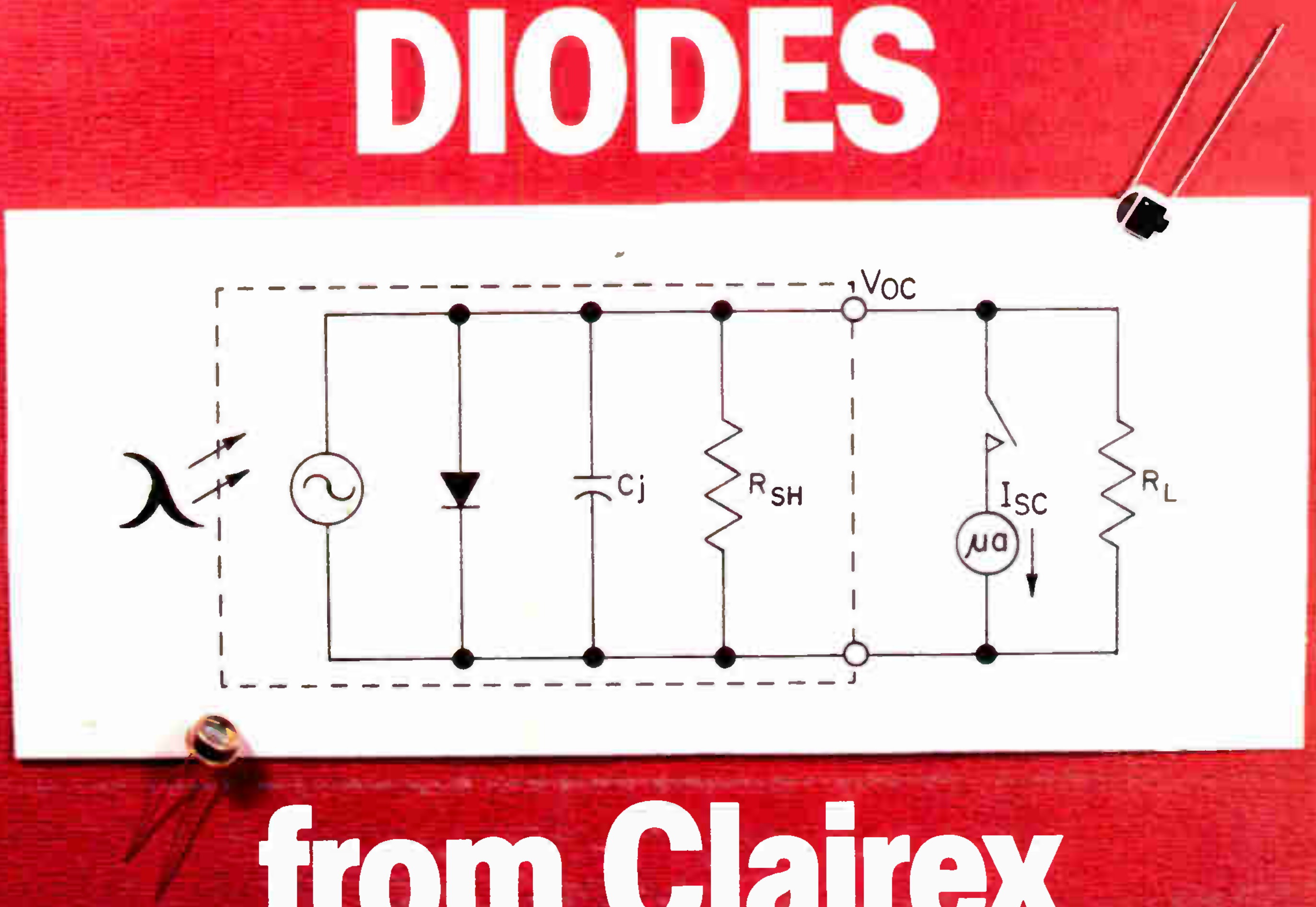

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