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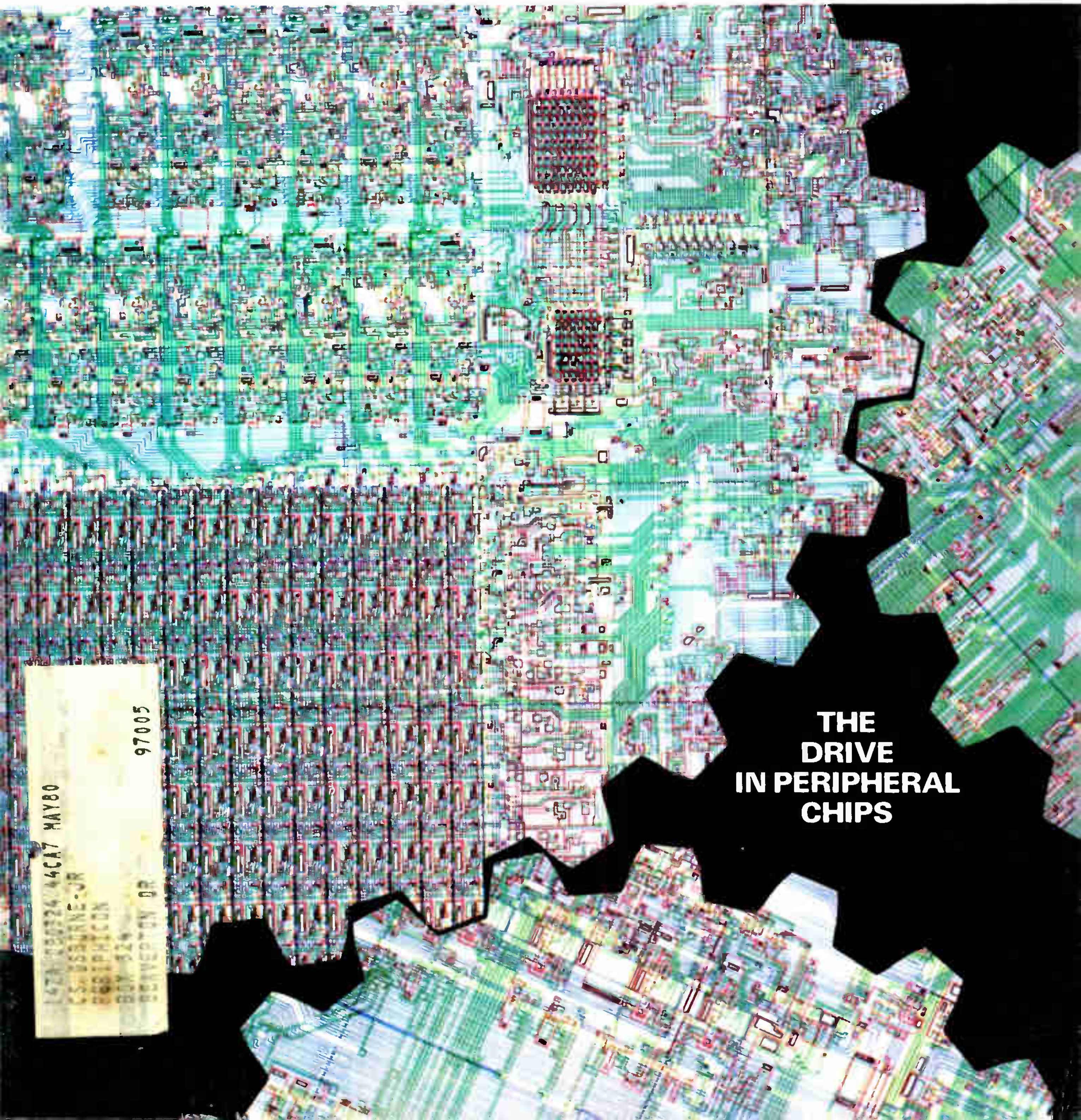

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Electronics

The International Magazine of Electronics Technology

Vol. 52, No. 17 • August 16, 1979

Highlights

Cover: Peripheral chips mesh with micros, 93
By off-loading processing tasks onto specialized peripheral chips, microprocessors continue to move into minicomputer territory. The new wave of high-performance peripheral hardware supports bus arbitration, memory management, mathematics and signal processing, peripheral-equipment control, and more.

Cover, by Art Director Fred Sklenar, shows parts of the 8086 microprocessor (copyright Intel 1978).

Berlin show to highlight the virtuoso TV, 84
The International Radio and Television Exhibition is a good place to spot hot new items on the European consumer market. Devices that turn the TV into an information terminal figure in this preview, as do video games and video cassette recorders.

Array processor boasts real-time response, 118
With the latest LSI low-power Schottky TTL and its own real-time operating system, this peripheral processor handles big repetitive arithmetic chores to up a minicomputer's throughput.

32-K E-PROM retains 16-K pinout, 126
To upgrade electrically programmable memory from 16-K to 32-K parts without revamping entire systems, compatibility with the fully utilized 16-K pinout is needed. Multiplexing two function signals on a single pin solves the problem.

. . . and in the next issue
Special Wescon preview . . . a signal-processing peripheral chip with over 30,000 transistors . . . an economical universal microprocessor development tool.

Electronics

Publisher's letter

There has been a lot of action of late in the design of peripheral chips for use with microprocessors. So put a handful of them together with a processor and memory, and chances are they will strongly influence the performance of the resulting system.

With this in mind, microsystems and software editor John Posa prepared the special report on peripheral chips (p. 93). He focused on the two major types—the well-known controllers for cathode-ray tubes and floppy disks and the system support devices.

The latter have become particularly intriguing. These devices basically enhance the performance of the central processing unit. And some of them are actually being made out of microprocessors.

"We now have 'intelligent' peripherals complete with CPU, input-output, and memory," John points out. "When you've got those elements, you've got a microcomputer."

These advanced devices are the result of the arrival of 16-bit microprocessors and will play an increasingly important role in the future.

"If you are waiting for distributed processing to become a reality, it has already happened quietly with these peripherals creeping into systems. In many cases the chip most capable of handling the processing function required does so with little or no central processor intervention," John observes.

It raises a question of how in-circuit emulators will function when there is more than one intelligent subsystem in a distributed network. Obviously, development systems will have to change with the times, John says, and become very flexible.

Another important trend already underway is development of single-chip microcomputers that can be programmed to perform as a peripheral controller of the user's choice. Such devices will grow more sophisticated, but so will applications, and it seems the chips cannot catch up.

Particularly fascinating to John is how quickly the chip producers respond to the demands for support of general-purpose processors. "Every time there is a function that becomes common to a majority of applications, it also becomes a candidate for integration. And the demands never cease," John explains.

Well, the much-discussed Data Encryption Standard (DES) is hardly out of the starting blocks in data communications and the long-range thinkers are already discussing systems to replace it.

The Probing the News story on public-key systems (p. 81) discusses the benefits and drawbacks of these new encryption and decryption concepts, primarily the public-key approach. As communications editor Harvey Hindin reports, this is much more secure potentially than the DES because only the receiver knows the decryption key. And while the public-key systems are still a way off, it's a good idea to prepare for the eventual DES replacement, Harvey advises.

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Readers' comments

Why a heap is not a stack

To the Editor: Thank you for publishing two fascinating articles about Pascal [June 7, pp. 111 and 117]. For those of us who wondered why we need new languages, Texas Instruments has supplied some answers. However, it invented the heap to do what we have been using a stack to do for years.

Is there any difference?

E. Amazon
DST Computer Services SA
Geneva, Switzerland

■ **Douglas S. Johnson replies:** *All TI Pascal programs use a "stack" for storage of variables and essential process history. A stack area is allocated in memory at process initiation. As each individual routine is entered, a "frame" at the top of the stack is used for control information, parameters, and local variables. Exit from a routine releases its stack frame.*

A "heap," on the other hand, is a storage area used for dynamically allocated variables created by a running process without correlation to the static structure of the program. Linked lists and trees are examples of data structures built from dynamic variables. A dynamic variable is created (and space is allocated in the heap) by calling the procedure NEW. Conversely, a dynamic variable is destroyed (and space is released in the heap) by calling the procedure DISPOSE. A Pascal program uses a heap only if it needs the dynamic features.

Dynamic variables, one of Pascal's most powerful features, are described in two books by Niklaus Wirth, "Pascal User Manual and Report," Chapter 10, and "Algorithms + Data Structures = Programs," Chapter 4.

Help wanted

To the Editor: The bus structures that will be required for future microprocessor applications are one area being covered by the microcomputer standards subcommittee of the Institute of Electrical and Electronics Engineers' Computer Society. A recent development has been the formation of a separate working group under my leadership to concentrate on backplane buses for microcomputer-based systems. We would welcome comments and suggestions either at our meeting or through me; monthly mailings will keep active participants informed of our progress.

As at present conceived, the backplane bus is a 20-megahertz, 50-centimeter interconnection scheme for high-performance subsystems. Although the subsystems are expected to be asynchronous, the bus may have to be synchronous to obtain the desired system performance. Minimum word size and expansion increments, types of data transfer, and control strategies are also being considered.

Meetings of the working group are usually held at Stanford University, Palo Alto, Calif., on the second Thursday of the month. So that Wescon attendees may participate, a meeting has also been arranged for Sept. 20 at 2 p.m. in the Kent room of the St. Francis Hotel, San Francisco.

Andrew Allison
(415) 941-6065
27360 Natoma Rd.
Los Altos Hills, Calif. 94022

Nemo nos impune lacessit

Viri: De "Like Gaul, LSA [the Low-Cost Solar Array project] is divided into parts—four to be exact" [July 19, p. 108], omnis Gallia in tres partes divisa est.

C. Julius Caesar
Massachusetts Institute of Technology
Cambridge, Mass.

■ *Nimirum omnis Gallia divisa est in tres partes, o Caesar qui venisti, vidisti, ac vicisti. Verum nonne licet iocari? Interea iacta alea est. (Of course all Gaul is divided into three parts, O Caesar who came, saw, and conquered. But surely one is allowed to joke? Meanwhile the die has been cast.)—ED.*

Correction

"Chips" should have read "circuits" in the headline of the article "Making 100,000 chips fit where at most 6,000 fit before" (Aug. 2, p. 109). Also, the correct spelling of the first co-author's name is G. G. Werbizky.

"I need a filter that eliminates interference. Period. That's the difference I'm looking for."

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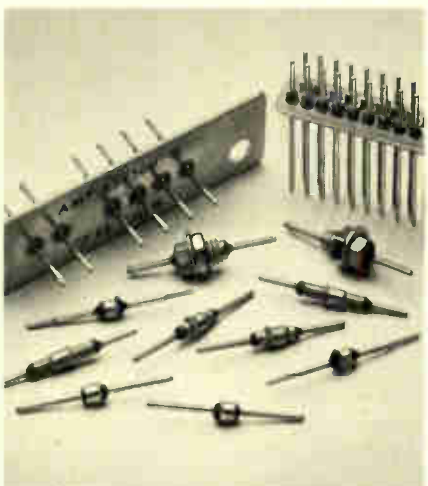
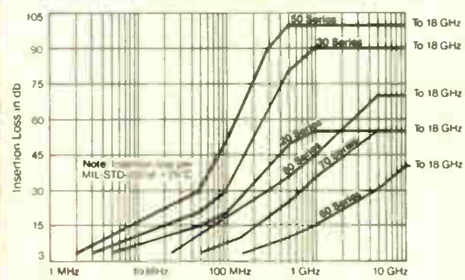
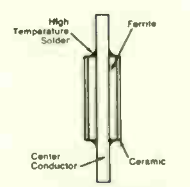


Quiet-Line Series—Comparison of Minimum No-Load Insertion Loss.





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AMP Quiet-Line miniature and sub-miniature EMI filters have, in fact, more than one performance-superiority difference.

Start with operation. Quiet-Line filters use an advanced absorptive concept that dissipates interference as a small amount of heat. The result—interference is eliminated. Other filters reflect interference which can cause undesirable ground current loops.

Quiet-Line construction is another advantage. For reduced chance of breakage during handling and no internal resonances, there's a rugged one-piece sleeve—along with a .040" diameter pin. No more ferrite beads and ceramic sleeves.

Performance? Quiet-Line filters have the highest insertion loss specifications in the industry. With ratings to 15 amperes, you also get high-power capability.

Across-the-board design coverage is another plus. There's a standard and premium series, and a low-capacitance series for high-speed digital pulse applications. You also have .025² post filters, an industry first from AMP.

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News update

■ Waveguide directional coupler switches with crosstalk isolation better than 30 decibels and switching voltages as low as 3 volts have been demonstrated by Ronald V. Schmidt at Hewlett-Packard Laboratories in Palo Alto, Calif. That level of isolation is suitable for digital signal processing. His device switches in subnanoseconds and can modulate amplitude at 1 gigabit per second. Another of Schmidt's devices has five waveguide directional coupler switches integrated on a single substrate to form a four-by-four optical switching network with crosstalk levels over 18 dB.

Such switches are one means of providing optical signal processing. They can be fabricated in the electro-optic material lithium niobate by planar processing techniques like those used for electrical integrated circuits [*Electronics*, Aug. 31, 1978, p. 39]. Everything is thus compatible with integrated-circuit control electronics and single-mode fiber optics.

The switch usually consists of a directional coupler formed by two closely spaced parallel waveguides with electrodes on top. By applying a voltage to the electrodes, the relative phase velocity of the energy in the waveguides can be changed via the electro-optic effect. If two or more sets of electrodes are used the switch can be tuned so light incident in one waveguide splits off into the other in any desired proportion.

■ The Canadian government is continuing its aggressive support of local industry with the goal of developing a complete satellite production capability.

First, there was the increase in funding to its Department of Communications David Florida Laboratory [*Electronics*, Nov. 23, 1978, p. 14]. Now the government is "giving a contribution" of $20 million to back the bid of privately owned Spar Aerospace Ltd. of Toronto to win construction of Anik-D satellites for Canada's Telesat satellite agency. In the past, Canadian satellites were built by American companies with major subcontracting to Canadian industry. **-Harvey J. Hindin**

"THE 8086 IS AN ARCHITECTURAL TRIUMPH!"

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The AmZ8000 is.

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System 8/8 speaks four languages fluently including PASCAL and COBOL. MDS doesn't. System 8/8 has a multi-master bus

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One last thing: We know it hurts to drop Intel for someone else. We've just been through it ourselves. But it's going to hurt a lot more two years from now. By then your competitors could be so far ahead of you, you might never catch up.

Call Advanced Micro Devices and we'll send you everything we've got on the AmZ8000. Or come to one of our 4-day seminars.

Once you've compared the AmZ8000 with the 8086, you'll know what we know. The AmZ8000 is the best 16-bit CPU there is.

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"What do you mean, microprocessors can

It's a fact. Versatile as microprocessors are, there are some functions they perform poorly or not at all. And other functions require such a complicated system design that you *know* there's got to be a better way.

Well, there is. Many AMI customers have found it in a combination of standard MPU and custom peripherals.

Where off-the-shelf circuits can't provide such things as A/D conversion, high-speed calculations, graphics output and multiple I/O interfaces, custom circuits can. And where the microprocessor doesn't work quite the way you want, we can customize it to meet your design objectives.

Or, of course, we can build you a custom system from scratch.

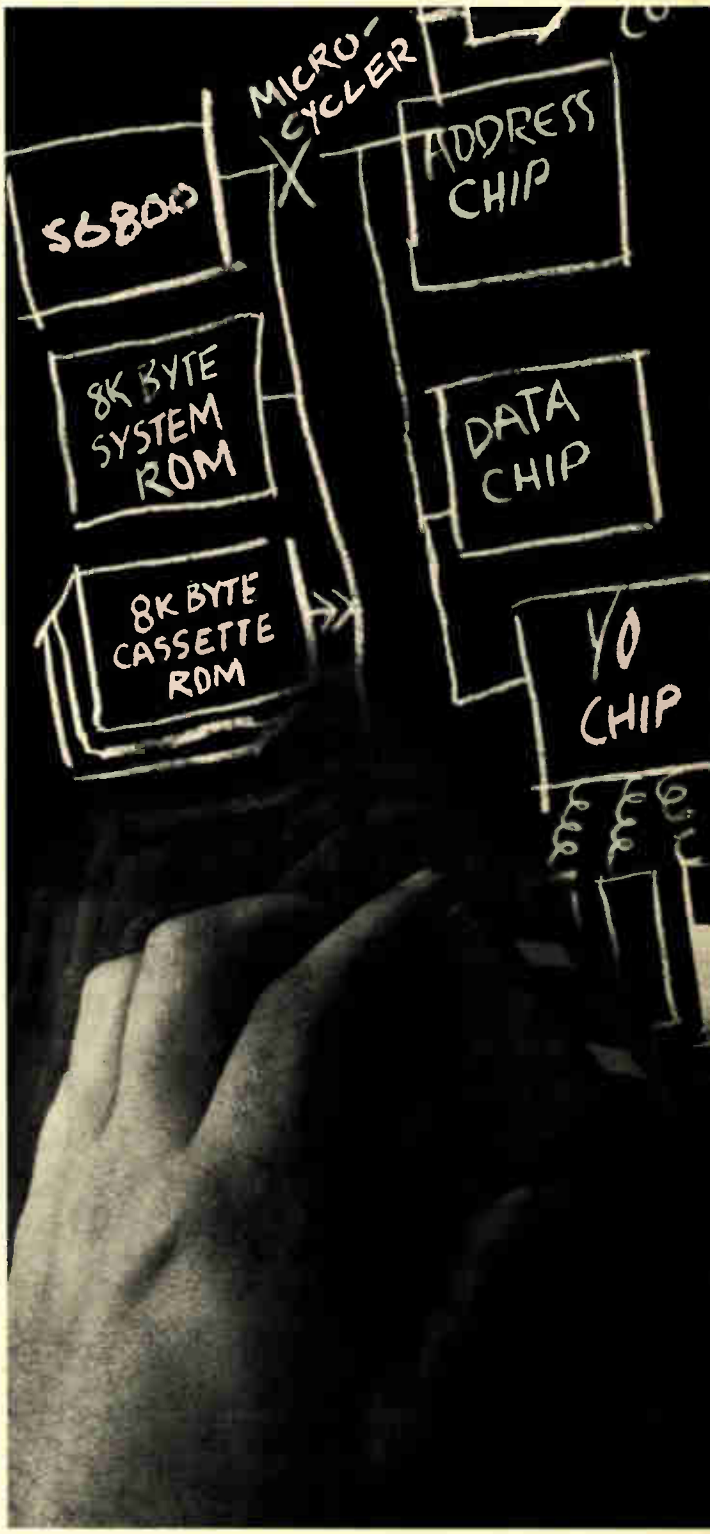
"How do I know which way to go?" Turn to an expert. But not one that specializes in standard or custom. Talk to the one company that specializes in both.

Since 1966, AMI has led the way in custom LSI. We've developed more than 1200 different circuits for an astonishing variety of applications.

And today, nobody offers a broader line of microprocessors, including the 4-bit S2000, the 8-bit S6800 and the 16-bit S9900. Along with their large families.

We're in a unique position to analyze your product's needs, and advise you on standard or custom or a combination of both.

"How can I justify the cost of custom?" You don't have to. In many cases, custom can be the most cost-effective choice. When you calculate the number of parts, board



only do half the job?"

space, assembly time and testing involved in a standard approach, you're often better off with custom. And, if you're using a microprocessor-based system, you have the added expense of software development.

You should also consider the priceless advantage of having a system that's yours and yours alone. That marketing edge has helped many of our customers establish themselves as the leaders in their field. And, by continually adding new bells and whistles to the original custom design, they keep pulling away from competitors trying to play catch-up.

"Suppose I want to control the design?" No problem. If you have designers on staff or have a working relationship with a design house, maybe all you need is manufacturing help.

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We do in two new booklets called "MOS Systems Solutions: A Dozen Case Histories Using Custom Circuits and Microprocessors" and "Six Steps to Success With Custom LSI." Between them, they cover most of the questions you might have about selecting the right process, design, fabrication and testing. And they show how LSI has helped a variety of companies steal a march on the competition.

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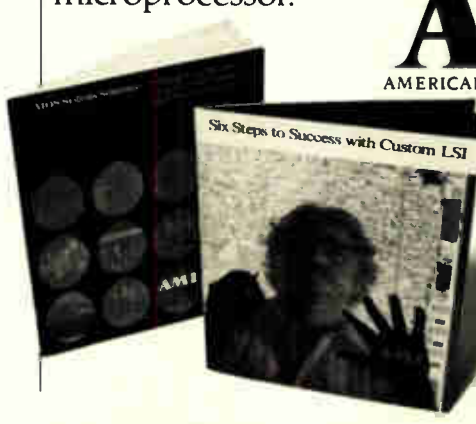


People

Amphenol's Makuch has his mind on standards

Connection. Setting standards for fiber-optic connectors is John Makuch's goal.

Like every new technology, fiber optics is at the point where it needs carefully drafted standards if it is really to take off. So believes John A. Makuch, recently appointed special projects director for Bunker-Ramo Corp.'s Amphenol North American division. Standards are demanding much of Makuch's attention, for he chairs the Electronic Industries Association's P-6.3 working group on standards for fiber-optic interconnection devices.

"What we need is a standard, reliable interconnect," he says. The standards will provide original-equipment manufacturers with assured specifications and test procedures. Developing technology will take care of the reliability factor, as well as boost acceptance, he adds.

Performance. The standards group is considering such performance characteristics as optical loss, dispersion, and vulnerability to environmental effects, as well as physical characteristics like number of channels and mechanical considerations like coupling torque. Its work may be done within a year, the 36-year-old chairman says.

The standards are vitally important to Makuch. His prime responsibility now at Amphenol's Danbury, Conn., Radio Frequency Operations is to develop a burgeoning fiber-optic connector line into a viable business. He has spent the last three years there as fiber-optics technical products development manager.

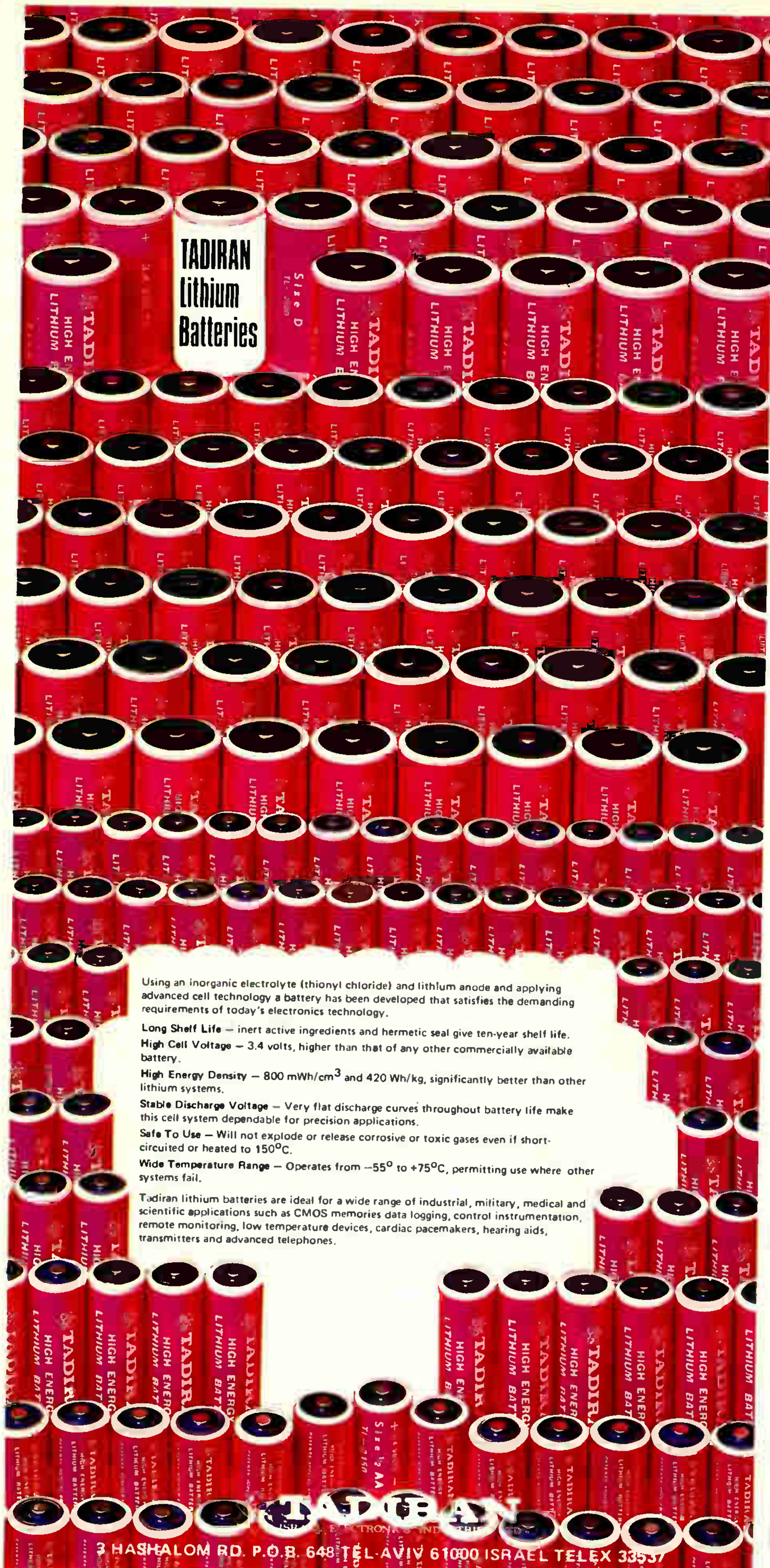
Makuch is well aware that fiber diameter affects the interconnection. The smaller the diameter, the harder it is to align the two separate fibers that must butt against each other in an interconnect device. The answer could be to standardize on a fiber 150 to 200 micrometers in diameter. He does not think this standardization would affect the data-transmission rates or dispersal for most users. The ultra-low-loss fibers needed for long telephone links and some computer lines may need to be somewhat smaller, however.

Still, the fiber problem is more easily solved than the cable problem. Here the issue is strain relief, for a glass fiber has no ductility. Once a cable is fixed to a connector, any stresses that are applied can be transferred to the fiber—a problem that should be the responsibility of another P-6 working group, Makuch points out.

Calming things down was first on Mackenzie's agenda

Every professional hockey team has a "policeman," a big bruiser of a player adept at intimidation. But Leonard N. Mackenzie, the new president and chief operating officer of Northern Telecom Systems Corp., Minneapolis, and former semiprofessional hockey player, says his priority when he took over last spring was to restore calm as well as order.

Troubles. Despite expected sales of $276 million in 1979, NTSC—formed late last year from the merger of intelligent-terminal maker Sycor Inc. and remote-batch-terminal vendor Data 100 Corp.—was in turmoil. Even with strong annual sales increases, an exodus of employees and rumors about the future of the two companies and their weak earning records created a tumultuous situation at the subsidiary of the Canadian electronics giant,



People

Restorer. Len Mackenzie is bringing back calm to Northern Telecom Systems.

Northern Telecom Ltd. (NTL). "It was panicsville," says Mackenzie.

The 41-year-old former general manager and marketing vice president of TRW Inc.'s Communications group, where he spent eight years, quickly "slowed things down," ending what outsiders saw as an anti-Data 100 housecleaning. In fact, notes Mackenzie, who joined parent company NTL as marketing vice president only last fall, several former employees are coming back "to better jobs than the ones they had before."

Canadian-born Mackenzie says he also began evaluating how the two companies' product lines are regarded in the marketplace, partly by talking with customers in person. The results of the evaluation will be unveiled beginning this fall, he says [*Electronics*, Aug. 2, p. 50].

Mackenzie expects his company and NTL's other American subsidiary, telecommunications hardware vendor Northern Telecom Inc. of Nashville, Tenn., to double sales volume over the next five years. They will do this through the evolution of existing hardware and software, not by revolutionary adoption of the dream office of the future.

He will concentrate on software to reduce costs with broadly based application programs. Yet he is anxious to maintain enough flexibility so users can make changes. He also hopes to target marketing opportunities "much more carefully than the mainframers have done." This philosophy seems consistent with the temperament required by his current hobby, the restoration of old cars. Len Mackenzie would rather restore than discard. □

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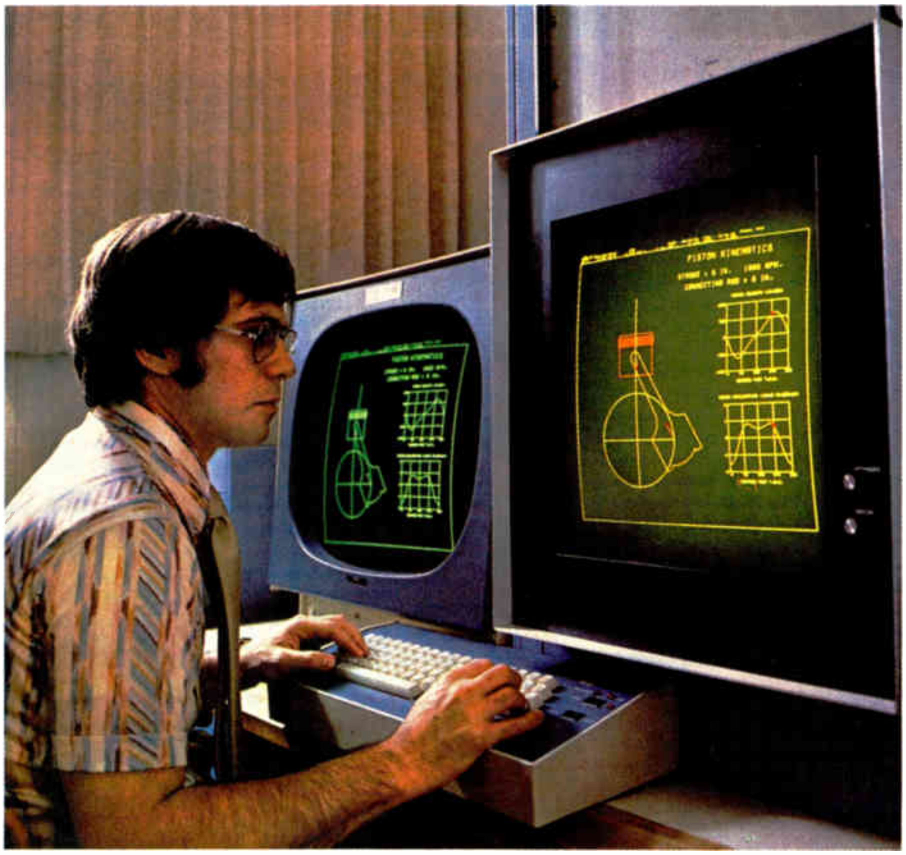

Exemplifying what state-of-the-art CAD technology can do for manufacturers, Chrysler Corporation Chief Engineer Robert Brauburger reports dramatic gains in the speed and efficiency of their design process. Above: a Chrysler engineer uses a color graphics terminal to analyze piston performance. Below: the control room at Chrysler's Technical Computing Center, where an operator monitors four interconnected Control Data® CYBER 170 systems.

American manufacturers are challenged by spiraling inflation and increasing competition. They must keep pace with productivity gains abroad to maintain market share and protect the jobs of their employees.

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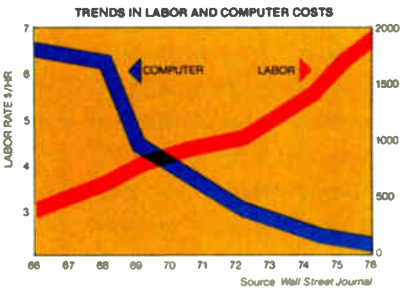
Control Data also offers manufacturers a wide range of data services through some of the world's foremost data processing networks.

Through our CYBERNET® Services we provide the benefits derived from processing on Control Data computer systems, along with sophisticated application programs

the Manufacturing Industry



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And when our new CAD/CAM technology is available, manufacturers will be able to go from a design on a CRT screen to a finished part—all with greater productivity and better use of resources than offered by the present technology.

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Boeing, a long time user of Control Data computers, recently installed two CYBER 175's in a CAD/CAM center to assist in the design of its new generation of passenger aircraft.

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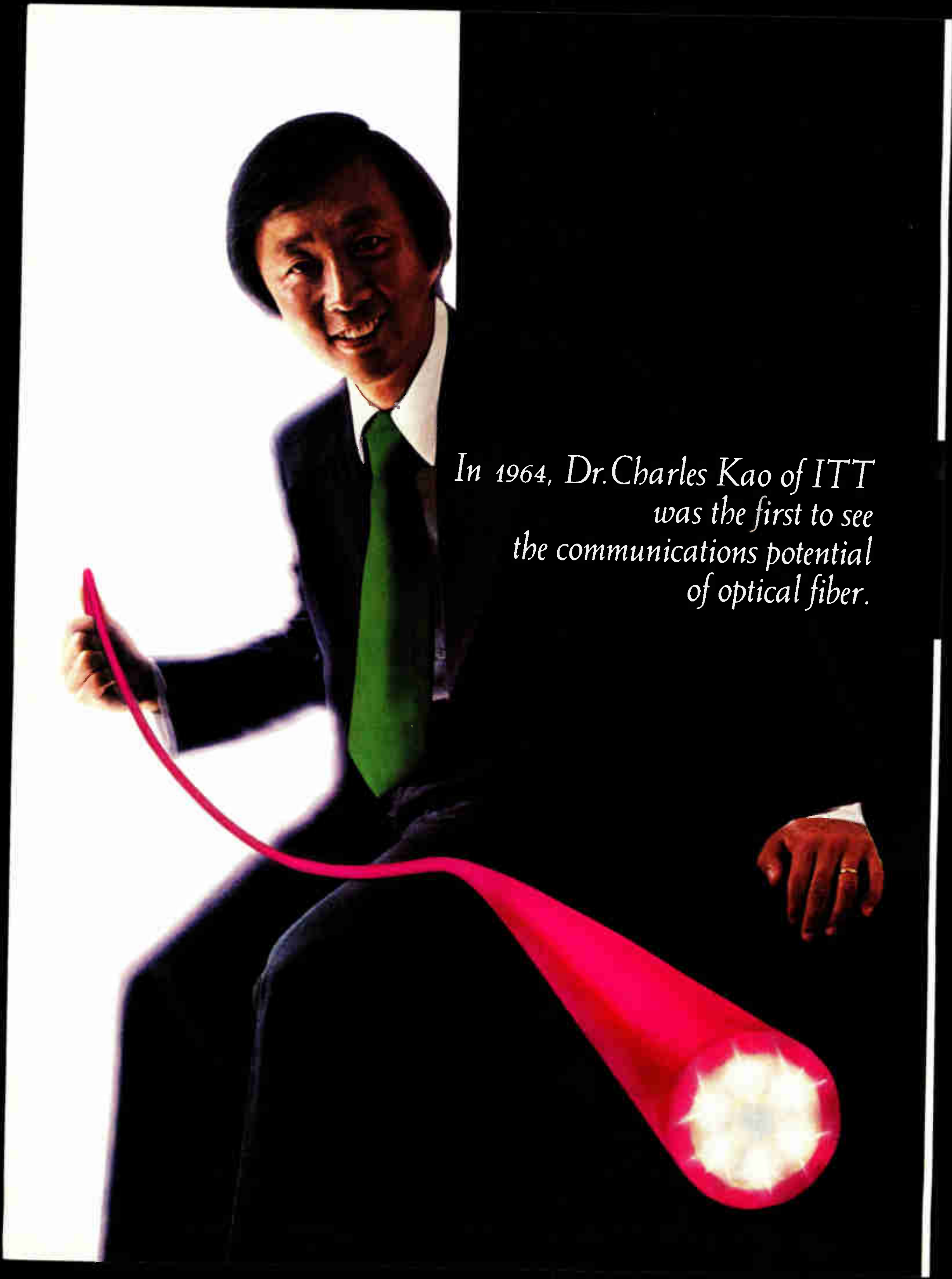
In 1964, Dr. Charles Kao of ITT
was the first to see
the communications potential
of optical fiber.

Many commercial ITT designed and installed fiber optic systems ranging to 45 Mb/s are already in use. All are delivering the interference-free communications expected. Additional systems are currently in production.

A unique record. A record only made possible by our early recognition of the potential of fiber optics, and the willingness to concentrate the scientific, technical, and production resources required to turn feasibility into practical reality.

Today, the Electro-Optical Products Division of ITT can offer design and application engineers either complete systems or any components their work requires. • Optical fiber cable. • Light source and detector packages. • Electro-optical transmitter and receiver modules (digital or analog). • Star, tee, directional and bidirectional couplers. • Connectors. • Connector and splice installation equipment. All provide interference-free information handling capacity not achievable in conventional wire systems. All are compatible. All are field proven.

If you envision use of fiber optics in your computer system, telecommunications, industrial applications, or for any other purpose, write us on your letterhead. Because we may already have gone over the same ground. And because we both know the optical fiber communications age has begun.

Imagine what we can do together.

ELECTRO-OPTICAL PRODUCTS DIVISION ITT

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It's a name that is already well known in semiconductor products as well as in data systems, cable TV products, and industrial components. Now, we're taking it into another area of high technology.

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The same conscientious and dedicated people will continue to back up our product line. With the same prompt product and technical assistance, order processing and after-sale service. Even the product

We are the new name in optoelectronics...

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Over 50 of the most competent distributors throughout the world will continue to provide our customers with immediate availability of our wide variety of optoelectronic products. And our sales representatives are strategically located to give on-the-spot assistance in design and product selection.

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During the past year we "enlightened" the industry with better ways to use alphanumerics, new approaches to panel design and how to get bigger, brighter digits in less space. And that's just the beginning. You'll soon see the result of constant research and development as we announce a number of creative new products in the months to come. As the "oldtimer-newcomer" in optoelectronics, we'll continue to design, produce and improve the products that best fill your design needs. That's a promise.

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GENERAL INSTRUMENT

and we will continue to make a name for ourselves.

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Wafer-scale integration is on the way

Even in a progress-oriented field like electronics, most people talk of evolutionary change, rather than revolutionary upheaval. Then something grabs our attention and reminds us that progress often occurs step-function style even in evolutionary times.

Wafer-scale integration (p. 88) is a case in point. Long sought by researchers, WSI holds a variety of promises that could have a solid impact in the 1980s.

For one thing, it is possible to imagine entire data processors on a wafer. Today's modern production equipment already makes it possible to get away from the sort of step-and-repeat methods that have characterized the fabrication of integrated circuits until now. So why not all the various parts of a data processor on a single large wafer? —except for hand-and-eye–oriented input/output devices, of course.

A WSI data processor with multiple arithmetic and logic units, a very large main memory, and even some solid-state bulk storage is at least plausible now. And it could be fast—very fast. Propagation delays would be measured in picoseconds as signals flashed across a wafer rather than across a mother board and a backplane as in today's computers. In addition, a WSI system could have a built-in test and diagnostic system, so the wafer could take care of itself.

It is impossible to anticipate all the potential cost, size, packing density, performance, and other improvements WSI could provide. And it is necessary to point out that it will be years before these things start appearing. Still, by the mid- or late-1980s wafer-scale integration could be in use even though many problems remain to be solved. How the industry takes hold of this unusual technology remains to be seen. As in other new developments, the obvious applications ultimately may not be the most important. Users may once again "tell" the industry what the future will be.

An IEEE election without the 'gadfly'

The reform movement in the Institute of Electrical and Electronics Engineers is getting old. It has been almost a decade since the first grumblings from the grass roots about the ultimate aims of the IEEE were first heard.

It has been an interesting period—sometimes stimulating, sometimes irritating. Among the personalities that have influenced this on-going reform movement has been Irwin Feerst—who himself is sometimes irritating. With his now-familiar brusque manner, he has banged away at the institute leadership, seeking to alter the direction of the organization.

Feerst has run for IEEE president more times than we care to recall—always unsuccessfully, but always ready to pick up the pieces and start over. Now perhaps as a sign of age in the movement he has had to withdraw from this year's balloting to give himself time to recover from a heart attack.

As we have pointed out in the past, if IEEE politicos could only look past Feerst's bravado, they might find more in his proposals than first meets the eye. He has struck a responsive chord with many an EE tired of business as usual in the institute. He has backed the principle that the IEEE should support the career aspirations of its members.

It is difficult to assess Feerst's influence on the IEEE—some has been positive, some not. The institute has become more responsive to the career needs of the members, but this very shift has polarized the membership.

One thing is sure: the election will not be the same without Feerst. We hope the elected candidate will fashion a steady course for the institute, one designed to resolve the conflicts surrounding professional activities.

Meetings

Compcon Fall '79—19th IEEE Computer Society International Conference, IEEE, Capital Hilton Hotel, Washington, D. C., Sept. 4–7.

Second International Fiber Optics and Communications Exposition, Information Gatekeepers Inc. (Brookline, Mass.), Hyatt Regency O'Hare Hotel, Chicago, Sept. 5–7.

25th Annual Holm Conference on Electrical Contacts, Illinois Institute of Technology (Chicago), Palmer House, Chicago, Sept. 10–12.

Dielectric Materials, Measurement and Applications Conference, Institution of Electrical Engineers (London), University of Aston, Birmingham, England, Sept. 10–13.

Fall Conference, USE Inc. (the organization for those who use Sperry Univac's series 1100 computers, Bladensburg, Md.), Diplomat Hotel, Miami, Fla., Sept. 10–14.

Optical Communication Conference, IEEE, RAI Conference Building, Amsterdam, Sept. 17–19.

Ninth European Microwave Conference, Institution of Electrical Engineers (London), The Brighton Centre, Brighton, England, Sept. 17–21.

Impact of Improved Clocks and Oscillators on Communication and Navigation, National Bureau of Standards, NBS headquarters, Gaithersburg, Md., Sept. 18–20.

Wescon/79 Show and Convention, IEEE and Electronic Conventions Inc. (El Segundo, Calif.), Brooks Hall, San Francisco, Sept. 18–20.

Autotestcon—Automatic Support System for Advanced Maintainability Conference, IEEE, Radisson Hotel, Minneapolis, Sept. 19–21.

29th Annual Broadcast Symposium, IEEE, The Washington Hotel, Washington, D. C., Sept. 19–21.

Telecom '79—Third World Telecommunications Exhibition, International Telecommunications Union, Palais des Expositions, Geneva, Sept. 20–26.

IPC Fall Meeting, The Institute for Interconnecting and Packaging Electronic Circuits (Evanston, Ill.), Sheraton Palace Hotel, San Francisco, Sept. 23–27.

Electrical Overstress/Electrostatic Discharge Symposium, ITT Research Institute (c/o RADC/RBRAC, Griffiss Air Force Base, N. Y. 13441), Stouffer's Denver Inn, Denver, Colo., Sept. 25–27.

Mini/Micro Computer Conference and Exposition, sponsored by the organization of the same name (Anaheim, Calif.), Convention Center, Anaheim, Sept. 25–27.

Second International Conference on Electrical Variable Speed Drives, Institution of Electrical Engineers, at the IEE headquarters, London, Sept. 25–27.

Ultrasonics Symposium, IEEE, Monteleone Hotel, New Orleans, Sept. 26–27.

Gallium Arsenide Integrated Circuit Symposium, IEEE, Sahara Tahoe Hotel, Lake Tahoe, Nev., Sept. 28–29.

Short courses

Computing and Communications in the 1980s, a seminar to be held Sept. 11–12 at the Park Lane Hotel, New York. For information, write to Martin Simpson Research Associates Inc., 63 Wall St., New York, N. Y. 10005, or phone Sande Grant Goldman at (212) 344-3480.

The International Standard X.25 Interface Protocol for Packet Networks and Related Network Protocols, a seminar to be held Sept. 25-26 at the Capital Hilton Hotel, Washington, D. C. For information, write to McGraw-Hill Conference Center, 1221 Avenue of the Americas, Room 3677, New York, N. Y. 10020, or phone (212) 997-4930.

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They did.

You'd expect our design engineers to be biased in favor of these new counters. But when we challenged them, they convinced us by going back to basics:

"Face it, in a counter, basically two elements determine whether or not you can get accurate repeatable readings: the input amplifier and the crystal oscillator.

In these new counters we've used new thick film hybrid circuits to control input amplifier circuit characteristics and reduce instrument costs.

With these new hybrids we get excellent sensitivity, a flat response and, at the same time, we have reduced the effect of parasitics.

As a side benefit, with hybrids the parts counts are less. This means there are fewer components to fail.

The new ovenized oscillator options were designed especially for these new counters. That means you get better temperature spec's, aging rates, and better short term stability than with either free air crystals or TCXO's.

As a result, measurement accuracy is improved and calibration cycles can be extended.

And because these low-power ovens can operate from batteries, there's no time wasted in the cal lab waiting for the oscillator to warm-up. More importantly, cal lab accuracy is preserved when you take the instrument back to the bench."

The engineers went on and on. For example, to reduce false triggering due to noise, they incorporated stainless steel RFI shields. They're standard on all models.

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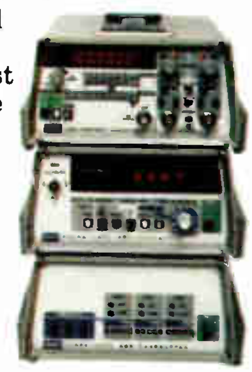
Fluke solved the problem of putting low-cost products on the IEEE-488 bus with the Model 1120A IEEE Translator. With it, you can use any of these new counters with a number of other Fluke instruments in compact, portable IEEE-488 mini-test systems.



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Period Average		×	×	×
Time Interval		100 ns	100 ns	10 ns
Time Interval Average			×	×
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T20 miniature size thumbwheel. It's a back mount design, comes in from 2 to 16 positions and measures just 1.150″ high with .500″ wide modules.

T56 sub-miniature pushwheel rotary switch. Wheel indexing is controlled by two plungers—one above (−) and one below (+) the lighted legend to control up/down counting. Front mount, requires no hardware to gang. Just snap into panel cutout. Measures a small .945″ high with .300″ wide modules.

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Electronics newsletter

Softech acquires control of UCSD Pascal

Softech Inc., a 10-year-old software technology company in Waltham, Mass., has signed a licensing agreement with the University of California at San Diego to take over full responsibility for UCSD Pascal, including the right to improve the existing package, increase fees and draw up licensing agreements with others. To handle the highly regarded implementation of Pascal developed by the university's Institute for Information Systems, **Softech has formed a subsidiary in San Diego, called Softech Microsystems Inc.** The new firm is staffed by former UCSD employees and several people from the parent firm. This arrangement ends a six-month effort by the university to divest itself of the Pascal project, whose successful licensing activities were threatening the school's tax-exempt status.

First bubble-memory test system delivered to National

National Semiconductor Corp.'s Bubble Memory group has accepted the initial delivery of the Xincom 5585 magnetic-memory test system [*Electronics*, March 15, p. 33] from Fairchild Camera and Instrument Corp.'s Test Systems group in San Jose, Calif. Based in nearby Santa Clara, **the device manufacturer has ordered several other 5585s that are scheduled to be delivered over the next 18 months** and, a company spokesman confirms, will be used for both characterization and production testing. Meanwhile, Fairchild has received several other orders for the 5585.

Honeywell to add fiber-optic link to process controllers

Honeywell Inc.'s Process Control division, Fort Washington, Pa., will soon be installing fiber-optic data-communications links between loop controllers and a central computer control room for one of its best-selling process-control systems. The company's corporate technology center in Minneapolis, with some help from recent acquisition Spectronics Inc. of Richardson, Texas, is completing development of the fiber-optic link for the popular TDC-2000, a microcomputer-based chemical-process-control system. The fiber-optic hookup, Honeywell claims, **would be several times faster than the 1-million-bit-per-second speed via coaxial cable currently considered the fastest in the field.**

High-speed fax introduced by Xerox for international sales

Xerox Corp.'s new Telecopier 485, with a maximum transmission speed of 1 minute per page, will also enter the international facsimile market at high speed. At the U. S. introduction earlier this month, it was learned that Fuji Electric Co. will sell a version in Japan and that Rank Xerox Ltd. will market one in Europe. The machine, which uses an 8-bit Toshiba microcomputer, **can skip white spaces on a paper, thereby boosting maximum speed for a typical business letter to about 1 min. when linked to another 485 over a telephone line.** It also offers 2-, 3-, 4-, and 6-min. speeds, achieving compatibility with Xerox's other telecopiers and with other facsimile machines. The 485 was developed by Fuji Xerox Co., a joint venture, and will be made in Japan.

U. S. gets lower berth in maritime satellite project

Some of the wind is out of the sails of the United States bid to get a say in the running of the International Maritime Satellite Organization (Inmarsat) equal to its world shipping operations. **The U. S., with around 30% of world shipping, angled for a minimum 25% share in Inmarsat but netted just 22% compared with a 15% share for Russia and 11% for Great Britain.** The organization, which involves 20 maritime nations, will spend some $230 million to provide global satellite communications for more than 2,000 ships. Completion is expected sometime in the mid-1980s.

HP decides not to make bubble memories

After nearly 10 years of quiet research and development on magnetic-bubble memory technology, Hewlett-Packard Co. has even more quietly dropped plans to manufacture the devices. **In fact, the Palo Alto, Calif., firm is likely to decide later this month whether it will even continue R&D on this fast-moving technology.** HP insiders indicate that high startup costs and the availability of outside suppliers suggest a "buy" decision.

SIA sets sights on R&D spending

The Semiconductor Industry Association's top priority for the 1980s is promoting the availability of capital to finance research and expansion. But to achieve its goal will require changes in government finance, tax, and antitrust laws, the SIA says. Two changes it will especially push to encourage investment in high-technology companies are: **letting investors sell securities and reinvest the profits tax-free** into new securities of technology companies; and reducing the term of maximum tax credit to three years from seven years.

Jedec committee to fix military hybrid specs

Jedec, the Joint Electron Devices Engineering Council of the Electronic Industries Association, hopes to bring order out of hybrid circuitry's present specification and qualification chaos by reviving the long-dormant JC-30 committee. Plans are to rationalize supplier qualification procedures, specification techniques, and qualification of parts and makers for military applications. **New JC-30 chairman G. James Estep of Hybrid Systems Inc., Bedford, Mass., hopes to make hybrids as easy to qualify as present day monolithic devices.** At present there are no hybrid circuits on the defense electronic supply center's Qualified Parts List.

Now there's IBM-compatible remote maintenance

One of the legion of IBM-compatible computer makers who imitate the industry giant's machines, Two-Pi Corp., will now also imitate the remote service techniques IBM introduced on the new 4300. **This fall, at its Santa Clara, Calif., headquarters, Two-Pi is establishing a remote diagnostic center that will receive all service calls.** Users will be instructed to unplug the console from Two-Pi's V32 computer and substitute a modem connected to the remote center thereby allowing technicians at the center to run diagnostic routines and pinpoint the trouble to a single board. If the bug cannot be ironed out over the phone, a service technician will be sent.

Addenda

National Semiconductor Corp., Santa Clara, Calif., plans next month to produce sample quantities of its 64-K dynamic random-access-memory, NMC4164, a single-supply 5-V device using a triple polysilicon structure with 3.5-μm geometries. . . . **CII-Honeywell Bull will be supplying Datapoint Corp. of San Antonio, Texas, with disk drives for computer terminals and minicomputers.** . . . . Oak Industries Inc. of Crystal Lake, Ill., plans to invest $17 million in two joint ventures in Taiwan **to produce materials used by its existing off-shore operations in that country.** One will produce copper foil and the other will produce laminates.

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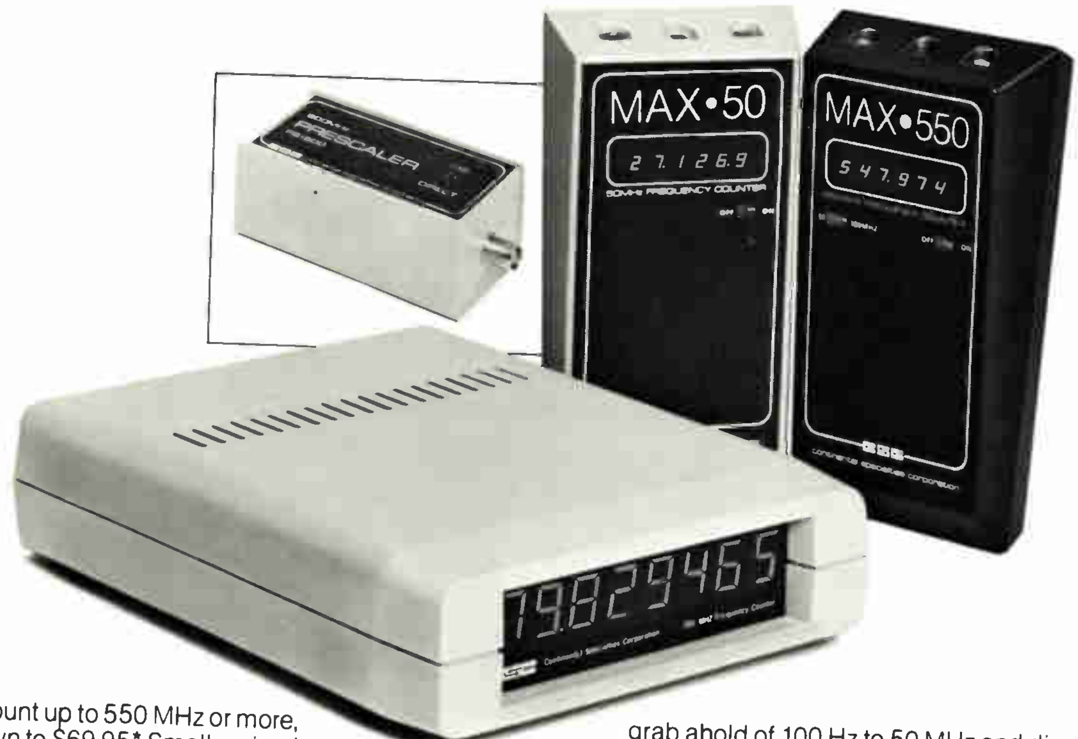

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MAX-50 in its calculator-sized case lets you grab ahold of 100 Hz to 50 MHz and displays the count on six bright LED digits. Its accessory mini-whip antenna even lets you pick up RF fields when a cable is inconvenient. And it's a speed reader, with six updates per second. All for just $69.95.*

PS-500 is our very capable Buffered Prescaler, which extends the range of almost any frequency counter ten times, up to 500 MHz. Its buffered 400 mV output can drive even tired old counters reliably. And you can add this extra capability for just $59.95.*

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Elliptical antenna for ground stations fights off noise

by James B. Brinton, Boston bureau manager

Off-center feed in oval dish keeps beam narrow and sidelobes low, even when site is a city roof

For fear of terrestrial interference from radar, microwave communications, and some broadcast services, the antennas of satellite ground stations have historically been sited in the sticks and in the pits. They are commonly 20 or more miles from cities and below the line of sight, in deep valleys or old rock quarries or other man-made holes.

Now GTE International Systems Corp., Waltham, Mass., thinks it has a better way. At Telecom '79, opening in Geneva, Switzerland, on Sept. 20, it is unveiling a new ground station antenna so immune to ground-based interference that it could operate from urban rooftops [*Electronics*, Aug. 2, p. 35].

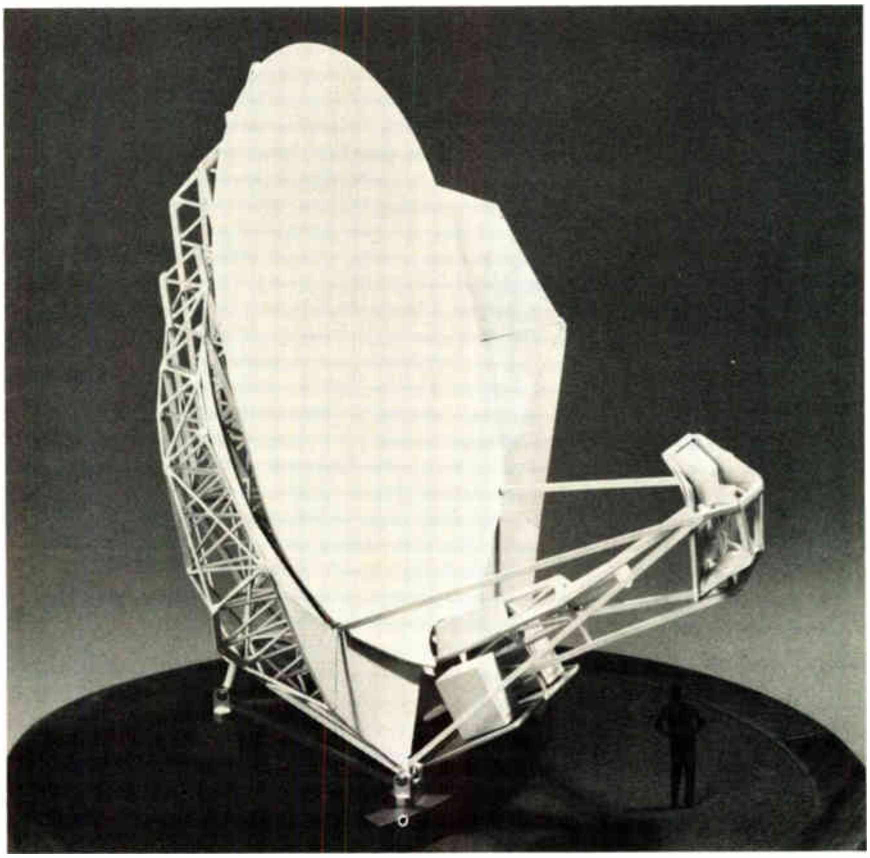
Gregorian feed. The keys are a narrow beam, low sensitivity to interference from outside the beam—called low sidelobes—and strategically placed microwave absorbing material. In a break with tradition, the new antenna has its feed not in the center but offset to the side of a not-quite-circular reflector. Because this Gregorian feed, as it is called, is out of the way of the beam, terrestrial interference cannot bounce off it into the dish and degrade the signal. Nor will outgoing signals bounce off the feed and broaden the beam. Similar antennas are used by the military.

The resulting system has a very narrow beam—only about half a degree wide at its −3-decibel points—and very low sidelobes. According to antenna program director, Paul J. Nordquist, the antenna's sidelobes are at least 10 dB lower than those of conventional dishes and this means 10 dB more rejection of off-axis interference.

Silenced. As for the microwave-absorbing material, it covers the rim of the reflector and parts of the feed. Any fugitive energy that somehow finds its way into the antenna's "optics" will usually be absorbed instead of adding noise to the signal.

The dish is not the customary circular parabola but an elliptical one. As such, it will cost somewhat more to produce, as also will the offset feed. Nordquist nevertheless figures the antenna will be a bargain because of the money it will save in siting. For instance, eliminating 20-odd miles of land line between ground station and city would more than compensate for the slightly higher cost of the antenna.

In addition, because the feed



Gregorian. Developed by GTE for satellite ground stations, elliptical antenna, shown in model, is electrically equivalent to 7.6-meter-diameter circular paraboloid for 4-6 GHz band.

structure and the transmitting and receiving electronics are near ground level, the new system should be easier, safer, and less expensive to service. Finally, the antenna's narrow beam promises a future payoff; it could make possible closer spacing of communications satellites. Some of these even now are only 4° to 5° apart in synchronous orbit. But with the pencil beam and low sidelobes of the new antenna, there would be far less chance of illuminating more than one satellite. Also, sometime in the future, Nordquist figures, it might be possible to squeeze satellites as close together as 2° to 2.5°.

GTE plans to have a working model of the antenna in Geneva. It offers no pricing figures, saying the unit will be sold as part of a ground station system.

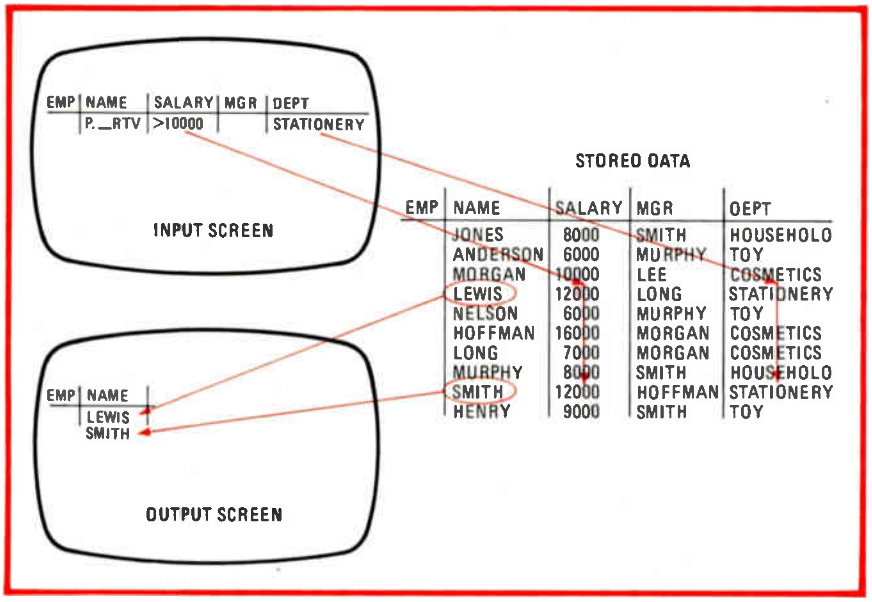
According to Nordquist, the hottest market for the new antenna should undoubtedly be in the United States. "Not only is there more interference here," he says, "but satellites are spaced more closely over the western hemisphere than elsewhere."

Software

IBM offers menu-like language to unsophisticated business users

Easing the task of communicating with computers, International Business Machines Corp. is quietly promoting a language it calls QBE, for query by example. It requires minimal programming skills, yet it permits unsophisticated commercial system users to extract, manipulate, and update information in a System 370, 303X, or 4300 mainframe, or any computer that runs IBM's Virtual Memory operating system.

To query the computer for data QBE does not require sentences constructed in a special syntax, as do most high-level languages. Rather, the user works from data on a cathode-ray-tube display. Basically the display is in the form of a table with the column heads specifying the classes of information and the rows containing the data.



Sample. QBE user begins with an input table, top left, that consists of column headings for the data in the computer. By filling in a command like P. and constants like >10000 and Stationery, the user calls up an output table, bottom left, culled from the stored data. It lists the names of those in the stationery department earning more than $10,000 yearly.

The user still must learn a list of commands ranging from single letters and symbols to one-word instructions. The software package rents for $325 a month. IBM hopes its simplicity will attract the business-office market that many see as the next important beachhead in the spread of computers.

Visualizing. The typical office worker should find the table format a great boon in working with the computer, says Michael Bushell, product administrator for QBE at IBM's Data Processing division in White Plains, N. Y. "It allows me to visualize better what I'm trying to do: by actually seeing the column headings of the data, I can much more easily put together a query."

There are tradeoffs. Like other menu approaches, QBE offers the user a range of possibilities, but ease of use takes precedence over flexibility and precision, observes Eugene I. Lowenthal, vice president and director of advanced product design for the Dallas software house, MRI Systems Corp.

When the user types in a column name, what appears is a skeleton table, showing only the column headings. By typing P. and moving it by cursor into the appropriate column, say "Name," as shown in the figure, the user can obtain a list of employee names. The symbol RTV is what is called the example element; it need not be an actual name.

In the illustrated query, the user asks for a list of employees in the stationery department earning more than $10,000. This is done by entering actual data values, "10000" and "stationery"—or what IBM calls constant elements, in the "Salary" and "Dept." columns. The result is a display of the simple table shown at the bottom of the figure.

To print out salaries as well, a P. would be typed before the constant element entered in the salary column. The program does contain safeguards against unauthorized access—a user may be barred from just the "Salary" column, for example, and not even get the simple table shown at the bottom left.

"I think the guys in research [IBM's Watson Laboratories in Yorktown Heights, N. Y., where QBE originated] have made a real breakthrough in the way the language allows the user access to multiple tables with a single simple query," Bushell says. It depends on a common example element that can link columns in two or more tables.

QBE also lets the user specify ranges of data to be considered and to perform grouping operations, insertions, deletions, and so on. It also can do simple arithmetical operations, such as figuring out averages or percentage increases, and it lets the user create new tables.

However, the range of possible data manipulations is not as great as with a formal high-level language, points out MRI's Lowenthal. "You can only go so far with a simple structure," he says. A high-level language more precisely expresses complex queries.

Bushell says there is room in QBE for IBM to add more commands to get more functions. IBM believes the language is powerful enough for the typical office environment. For more complex tasks, there are, as Lowenthal points out, more complex languages. **-Benjamin A. Mason**

Industrial

OCR unit for factory use deciphers fainter-than-usual figures and letters

Optical character-recognition systems do well reading print off high-contrast surfaces like white paper. But how about reading alphanumeric characters having much lower contrast because they have been stamped, etched, or embossed on metal, plastic, ceramic, or rubber?

Unquestionably, that is a hard job. Seemingly, it can be handled at present only by a new system being put on the market by DataCopy Corp., a small, six-year-old Palo Alto, Calif., design house specializing in electronic cameras. Called the System 200 Factory Data Entry System, it is the brainchild of DataCopy president Armin Miller.

Miller believes his system will be a boon to many industrial applications involving inventory control, inspection, and manufacturing. Moreover, he points out, it could advance the use of industrial robots. They could read their coded instructions off the very parts they were assembling. From a stamped metal surface, for example, the unit would read characters despite pits, mars, dents, protrusions, and gall marks.

Under test. One unit that identifies part numbers on nuclear fuel rods is already being tested. Another is being bought by an auto maker to read stamped labels on car bodies.

"It appears that no other nuclear organization has found another supplier to identify rods for them," says James Thornton, manager of test, fabrication, and assembly at Westinghouse Hanford Co., a Westinghouse Electric Co. subsidiary that manages the Hanford, Wash., engineering development laboratory for the U. S. Department of Energy. "We might put it together for other organizations," he says, calling the unit "quite reliable." Used to identify each of 50,000 fissionable rods, it reads six stamped or laser-etched characters.

Camera. DataCopy has added two important design elements to a standard OCR system to yield the unusual capabilities. One is centered around a solid-state camera and illuminating incandescent lamp. The camera, either hand-held or mounted on a work station, contains a vertical array of 512 self-scanning linear photodiodes on 1-mil centers. The array, which operates at a 312-kilohertz clock rate, is made by Reticon Inc., Sunnyvale, Calif., and horizontally scans the characters.

The second element is an image-processing system depending on circuitry and software that feeds a conventional OCR subsystem made by Dest Data Corp., also of Sunnyvale. Both these units and the camera act as peripheral devices to a Texas Instruments TMS 9900 16-bit processor running the system.

The image processer "cleans up" the characters scanned by the camera. It does so by performing a 12:1 data compression on the 512-by-512-bit camera field, converting each 4-by-3-bit section into a single bit. Normally, if 6 bits or more are dark, the compressed bit is a 1 and appears as a dark space on the image; if fewer than 6 bits, it is a 0 (white). The processor transmits the compressed image at 625 kHz to the recognition logic, which smoothes the image by comparing it with data stored in read-only memory, according to DataCopy engineer Melvin Herman.

Working it out. If one of the characters is indistinct, the processor will adjust the threshold—the number of bits out of 12 to make a dark 1—up or down depending on whether it senses that a lighter or darker image will clarify the character. If that does not work, the processor will adjust the threshold of the video signal the opposite way to see if that helps. The action is automatic and quick, Herman notes.

Actually, it is not that quick, which does not matter for this system. "In a factory environment, serial numbers are short, and you have two or three seconds to process them," says Miller. "That's a lot of time to process the image."

The result is a system—its electronics package is 10½ inches high and fits in a standard 19-in.-wide rack—that can read up to 100 characters per second with a rejection rate of less than 1 in 10,000 characters. Both the camera image and the OCR image can be displayed on a cathode-ray-tube terminal for visual checking, and the digital output can be converted into ASCII code for computer processing.

Three 2708 1-K-by-8-bit programmable ROMs hold a particular character font like OCR-A Alphanumeric or Farrington 7B, but the system could handle multiple fonts, Herman says. Moreover, "you can read new fonts in with the camera," Miller adds. The first unit in a system customized for a particular application will cost $140,000; the rest, under $15,000. **-William F. Arnold**

Microprocessors

AMD planning a 16-bit ECL chip

Large-scale integration of emitter-coupled logic and 16-bit microprocessors each reflect the state of the semiconductor fabricating art. Now Advanced Micro Devices Inc. is combining the two in order to produce the first full-blown 16-bit ECL microprocessor.

Dubbed the Am29116, the new part is intended primarily for use as a peripheral-equipment or communications controller. It complements the Sunnyvale, Calif., firm's popular 2900 family of 4-bit-slice microprocessors, although it is not a bit-slice part itself. It is not yet in silicon, but a sneak preview will be given at next month's Wescon show in a paper written by William J. Harmon, manager of bipolar microprocessor systems and applications, and applications engineer Warren K. Miller.

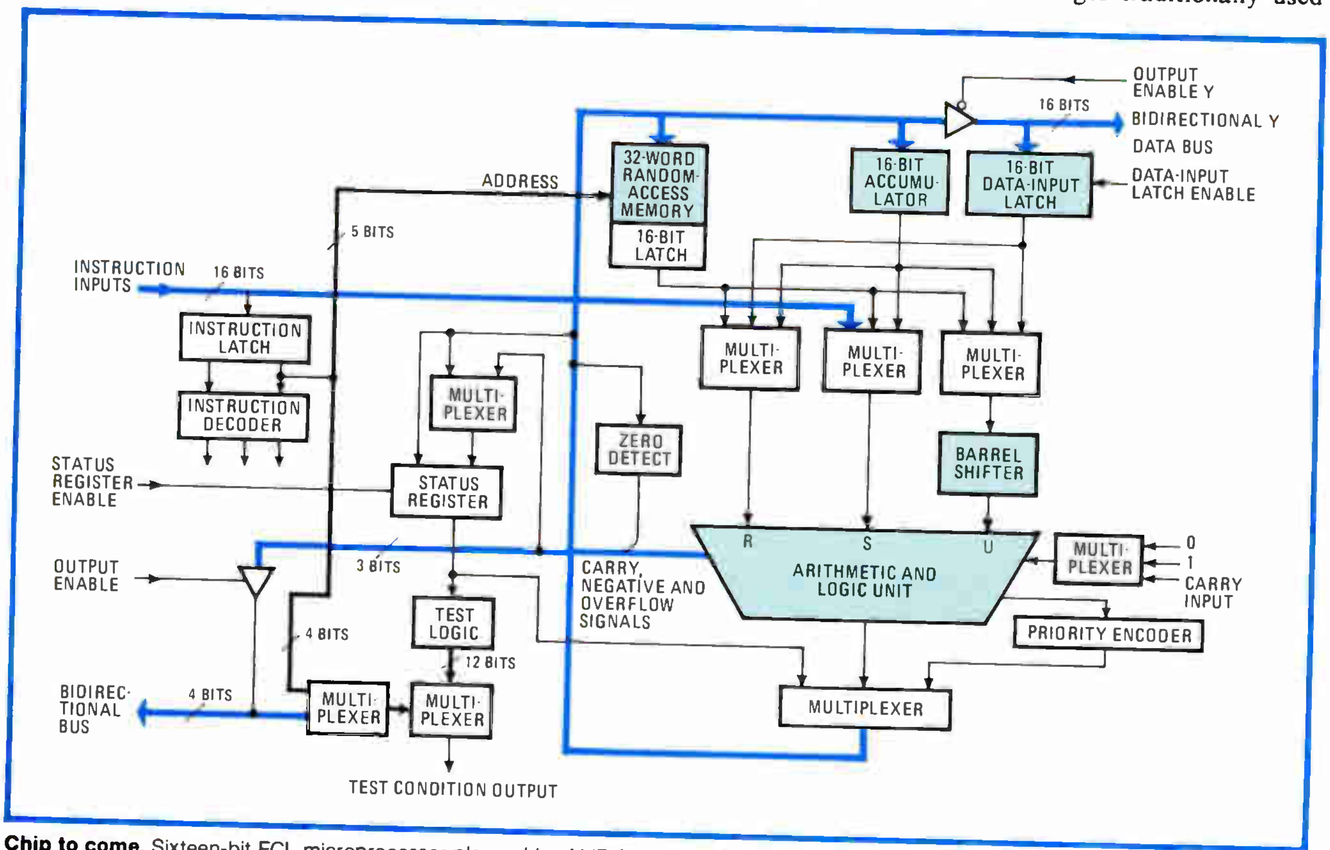
The 29116 does almost everything a general-purpose microprocessor does except the addressing. Because it is intended to operate with the microprogrammed bit-slice parts, the addressing is left to a separate microprogram-sequencer chip. But whatever flexibility this approach may compromise is balanced by the chip's compactness and the speed inherent in ECL.

Dozen. The new microprocessor will have 16-bit data paths and combines 32 registers, the arithmetic and logic unit, input/output control and other data-manipulation elements that would otherwise take at least a dozen chips to implement, observers note. What's more, operating at a clock rate of 100 nanoseconds—some 20% faster than the 2901 processor slice—it will probably outperform those chips.

In addition, the 29116 has 11 types of instructions in its powerful instruction set, including commands like prioritize and generate cyclic-redundancy-check digits. Up to now, such operations have required several lines of microcode and thus several cycles to execute, but the 29116 can execute the prioritize instruction in one cycle.

A 16-bit barrel shifter enables the part to perform rotate, rotate-and-merge, and rotate-and-compare instructions in a single cycle as well. Furthermore, the 29116 can execute so-called immediate instructions that other 2900 parts cannot.

The trick apparently will be to cram all these capabilities onto an ECL chip without running into overheating caused by ECL's relatively high power dissipation. Company sources indicate that this will be achieved by running the gates at less than the voltages traditionally used



Chip to come. Sixteen-bit ECL microprocessor planned by AMD for production in third quarter of 1980 will include complete arithmetic and logic unit, 32 words of RAM for registers, and barrel shifter. Most instructions will be executed in a single 100-ns clock cycle.

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by ECL circuits, resulting in a dissipation of 1.1 watts per package.

Faster operation. Using lower voltages will result in a speed penalty, but it still gives AMD faster operation than it would have achieved with the next fastest logic family, Schottky TTL, which is used in the 4-bit-slice family.

Although he will not discuss details of the tradeoffs, Harmon says the company "elected to go for higher density and function," rather than for maximum speed. The payoff comes from the completeness of the 29116. "We don't have to pay the additional speed penalty bit-slice processors do because we don't have to send the data between chips. We get a single input and produce a single output in one cycle."

Samples of the part will not be available until the middle of next year, so the company is reluctant to discuss details of the chip's fabrication. But it is expected that it will be built using a new oxide-isolated bipolar process. AMD is planning to produce the 29116 in the third quarter of 1980. **-Anthony Durniak**

Consumer

Canadians to wire diversity of services into homes over coaxial cable

When Ida Cates became the first woman telephone operator in Canada's Manitoba province in 1882, she provided her several score of "customers" with a wide range of information. Weather reports, hockey scores, medical advice, recipes, and fire alarm reporting were said to be among her specialties. Now, almost 100 years later, Manitoba Telephone is setting up Project Ida to provide 50 homes in rural South Headingley in the wide open spaces of Canada's wheat belt with electronic services that would make Ida proud.

Signals. A coaxial cable hookup to the telephone company's central office will be the link that allows more experimental services to be furnished to the home and more devices in the home to send signals out on the network than is possible with any other existing system. For example, video text information—everything from stock market reports to video games—may be called up at the touch of a button.

What is more, the lucky 50 homes will be wired to receive closed-circuit television, movies, and stereo music. Their water, gas, and electric meters will be automatically read, and the information fed directly to the utilities for billing. Fire, police, and medical center links will be also available.

In contrast, the Qube system recently installed in Columbus, Ohio, is really a multichannel cable-television operation and has only a keypad link to just some of the households hooked to the system. According to project manager Dennis McCaffrey, Ida will ultimately allow a similar direct subscriber response to television queries but "not on day one."

More than 20 different suppliers of services will be hooked up to the system, McCaffrey says. Manitoba Telephone will only provide the electronic highway. This is critical to the experiment's success, he notes, because, "if a host of services can be carried over one electronic highway—in this case the coaxial cable—the revenue from each helps to pay for the cost of the network." This is most important in rural areas where the cost of individual telephone-alone installations is high.

State of the art. Unlike some other tests of the "home of the future" that have been announced, the connections are being made without use of the broad bandwidth capabilities of fiber optics. It turns out that high-grade coaxial cable both is cost-effective and has more than adequate bandwidth for the purpose. In fact, while state-of-the-art equipment is being used throughout the installation, no exotic developments have had to be included.

All that needs to be done, says McCaffrey, is to provide a terminal in each home. A multidrop system connects the terminal to each communication device in the house, be it television or smoke detector. Transducers on each device generate or receive the analog or digital signals that travel along the full-duplex coaxial line. Adding these transducers should pose little problem, says McCaffrey. They will be commercial items such as digital encoders and voltage-to-frequency converters.

Fiber optics is not being ignored by the Manitoba Telephone people, however, and Project Elie, a "farm of the future" experiment using a fiber network, will start up in 1981 in the town of Elie in Manitoba. Project Ida will start in January 1980 and will be carefully compared with Elie as to costs and social benefit. Manitoba Telephone hopes that the results of the study will point the way to improved, more cost-effective communications services for its geographically dispersed rural customers. **-Harvey J. Hindin**

Solid state

TI readies I^2L peripherals

Within the next few months, Texas Instruments Inc. plans to begin supplying samples of four new microprocessor peripheral chips fabricated in integrated injection logic.

The new I^2L peripheral chips will be the first to be offered for use with the I^2L version of the Dallas company's 9900 16-bit microprocessor—the SBP9900A, which was introduced in March 1978. These chips are expected to find widespread use in military systems built around the 9900A, the fastest 16-bit part available to the military. They replace from 20 to 40 TTL packages with one I^2L chip, says Jerry Samsen, a TI applications merchandising official in Houston.

Developed by TI's Digital Circuits

division in Houston, the new peripherals—designated SBP9960, -61, -64, and -65—will be programmable devices to handle input/output control, timing and interrupt (two chips), and memory-mapped interfacing with system peripheral devices like printers. Each of the new chips will be fabricated using a standard array of 1,300 gates on a 28,000-square-mil die.

By using the gate-array approach, TI expects to reduce production costs and save on design time for extra I^2L peripheral devices to be added later, because the first seven diffusion mask steps will be identical on all devices built with TI's oxide-separated I^2L gate-array process technology. Differentation among the devices does not come until the final four mask steps, which define the metal gate interconnections, Samsen explains.

A number of other manufacturers, including Signetics, Motorola, and Fairchild, have previously supplied gate-array devices in bipolar technologies such as I^2L, TTL, and emitter-coupled logic that are aimed at commercial, rather than military, markets [*Electronics*, April 27, 1978, p. 84]. But TI officials are keeping mum about any commercial plans for their I^2L gate array. Initial applications for devices built with the array will come in military systems, where the overwhelming majority of SBP9900A microprocessors are now used, they say.

Three more. In addition to the four new peripherals that are expected in production-level quantities by the first quarter next year, TI has defined specific functions for three additional peripheral chips to be built with the gate array, says Don Walker, manager of TI's military products department in Dallas. These chips are not expected to be available in sample quantities before mid-1980, however.

Besides saving board space and weight, which is particularly important in many military applications, Walker says designers using TI's new I^2L peripherals will be able to reduce system power requirements by as much as 30%, in many cases,

News briefs

Amdahl beats IBM to the punch, while Itel reels

Expectation of new large-scale computers to come from International Business Machines Corp. is causing customers to hesitate in placing orders for current IBM or plug-compatible models (see related story p. 90). But Amdahl Corp., even as it considers merging with peripherals maker Memorex Corp., has apparently decided not to wait for IBM.

The Sunnyvale, Calif., firm has unveiled new 470 V/7A computers aimed directly at IBM's current top-of-the-line 3033. Claimed to outperform the 3033, the Amdahl unit with four megabytes of memory and 12 input/output channels is priced at $2.45 million—some 27% under IBM's 3033 price. The biggest 470 V/7A, with 16 megabytes of memory and 16 channels, is priced at $3.44 million.

Meanwhile, Itel Corp., San Francisco, paying dearly for underestimating IBM in the plug-compatible market, now says it will lose $60 million during its second quarter instead of the approximately $10 million it first reported [*Electronics*, July 5, p. 54].

Pay TV eyed for satellite to home

Comsat Corp. says it is talking with hardware and programming suppliers about providing subscription TV service via satellite over several channels directly to the home. The programs would be broadcast to small antennas on the subscriber's roof top. "The technology for such a system already exists and we are investigating the business potential," says Joseph V. Charyk, president and chief executive officer of Comsat in Washington, D. C. The new service could be introduced by 1983, he says.

Satellite TV service to the home is being tested experimentally in Japan. Canada and the United States have already run experiments and Comsat has conducted demonstrations using Canada's CTS satellite and a Comsat-developed small antenna.

X rays could focus on densest ICs

An IBM research scientist has devised an X-ray tube for the microscopic study of living cells that might also be used to expose submicrometer features of integrated circuits. It produces soft X rays, with a wavelength of 10 to 100 angstroms, exposing a picture of a live cell on an X-ray resist in 100 nanoseconds. Invented by Richard A. McCorkle at IBM's Thomas J. Watson Research Center, Yorktown Heights, N. Y., the tube works by creating a hot, dense plasma of carbon ions and electrons through which an electron-beam passes, causing X rays to be emitted by the carbon ions. Because the electron beam has a diameter of less than 100 micrometers as it reacts with the plasma, X rays are emitted from a very small region, which is desirable for high resolution.

Microdata finally lands a suitor

After several months of negotiations with some half-dozen companies, Microdata Corp. has reached an agreement to be acquired by McDonnell Douglas Corp. The Irvine, Calif. maker of minicomputer-based small business systems is waiting for the St. Louis aerospace company's board to approve the move and begin a tender offer of $32 in cash for each share of Microdata stock. It is expected that Microdata's operation will complement McDonnell Douglas Automation Co.'s computer services operation.

Penril acquires Ambac line

Penril Corp., Rockville, Md., continues to expand as a data-communications equipment maker with the $2.3 million acquisition of the Tele-Dynamics division product line of Ambac Industries Inc., Fort Washington, Pa. Products in the line, which has annual revenues of about $2 million, include a series of 1200- to 4800-bit-per-second synchronous and asynchronous modems for private-line and switched networks. Penril's revenues for its fiscal year ending July 31 reached an estimated $22 million, according to the company.

SCIENCE/SCOPE

The first close-up pictures of Saturn and its rings will be taken when NASA's Pioneer 11 spacecraft makes an historic swing by the planet September 1. The spacecraft, launched in April 1973, previously visited Jupiter in December 1974. Pioneer 11 carries two instruments built by the Santa Barbara Research Center, a Hughes subsidiary. One, an imaging photopolarimeter, will take about 100 high-quality pictures. It has been used to help guide the spacecraft ever since the mission was extended past Jupiter and the regular navigation sensors no longer pointed at the correct stars. The other device, an infrared radiometer, will take heat pictures of Saturn and study the chemical make-up of its atmosphere.

An exotic chip that would alert a pilot when he has been detected by enemy radar promises to open a new arena in modern electronic warfare. The unique wafer, called an integrated optic spectrum analyzer (IOSA), would allow a pilot to prepare for a dogfight, turn on jamming equipment, or take any other appropriate action. The device works by having a surface acoustic wave device convert processed radar signals into sound waves. These sound waves interact with light from a tiny solid-state laser and cause the beam to bend toward a detector array of charge-coupled devices. The amount of deflection indicates the frequency of the radar signal. The IOSA is being developed by Hughes for the U.S. Air Force.

The F-18A Hornet will be the first tactical aircraft with a radar that can make high-resolution radar pictures of the ground. The Hughes AN/APG-65 radar creates sharp real-time imagery from standoff distances in all kinds of weather. A pilot uses the imagery to navigate, select and designate tactical targets, and deliver weapons. This mode employs the technique of Doppler beam sharpening, which separates closely spaced ground points by filtering small frequency differences in radar returns.

The equipment that actually prepares the imagery is a programmable signal processor. This high-speed, special-purpose digital computer processes and stores the large amount of data required to produce a high-resolution map. The pilot commands the radar to expand a portion of the imagery for closer study. The radar, developed under contract to McDonnell Douglas, made its first flight aboard the new U.S. Navy and Marine Hornet in June.

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The day when satellites will broadcast television directly into the home has drawn closer with the development of a receiver that can be mass produced at low cost. The unit, delivered by Hughes to NASA's Goddard Space Flight Center, is used with an antenna and amplifier to tune in TV signals from any particular transponder of a broadcast satellite. It serves as a prototype for inexpensive models to be developed in the next decade. Rooftop terminals are expected to become commonplace in many countries by the mid-1980s.

compared to a TTL implementation. In addition, he notes, I^2L devices are believed to be even more radiation-tolerant than TTL devices. Besides the speed advantages and wider temperature range, improved radiation tolerance and reliability have been the primary advantages enabling bipolar parts to win military design-ins over their otherwise more cost-effective MOS competition.

By moving to provide I^2L peripheral support for the 9900A, TI may be positioning itself to take advantage of a "major change" coming in military system design technology, Walker indicates. "Most military systems for the last 10 years have been designed using standard TTL technology," he notes. "But in the next three years, I think we'll see a big shift to the next generation of military systems." The bipolar technologies of I^2L and Schottky TTL are both currently in the running for honors as the military technology of choice, he says. **-Wesley R. Iversen**

Military

Marines order Litton terminals

The U.S. Marine Corps has given the go-ahead to Litton Industries Inc. for full-scale development of a hand-held communications terminal with a light-emitting-diode display. Destined for tactical use in the field, 54 displays will be built under a two-year, $6.5 million contract from the Naval Electronic Systems Command to Litton's Data Systems division, Van Nuys, Calif. Over the last few years, Litton has received $1.25 million for development of a feasibility model and nine test models of the 3.7-pound digital terminal [*Electronics*, Nov. 11, 1976, p. 29].

Communicator. Book-sized terminal displays alphanumerics and graphics on LEDs.

Production. Referred to as digital communications terminals, the units will be delivered over the next 18 months for field-performance and reliability tests. Litton says current long-range plans envision production of approximately 3,500 units for the

Honeywell develops heat-pump controller

Honeywell Inc. begins shipping this month a new microprocessor-based controller for residential heat pumps, which are used to heat and cool air. Honeywell's goal: to develop a line of electronic devices that save fuel by carefully controlling how heating and cooling equipment operate.

The heat-pump controller comes from Honeywell's Residential Controls Center, Minneapolis. It relies on several thick-film sensors to monitor temperatures and pressures inside and outside the heat pump. It then makes operating decisions based on algorithms contained in memory. In contrast, an electromechanical controller might monitor just one parameter.

Plus. One big advantage of the new controller is that it saves wear and tear on the heat pump's compressor. It does so by substantially reducing the number of defrost cycles needed during humid weather to remove ice that forms around the condenser coil. Built around an Intel 8049-type microprocessor, the controller also pinpoints equipment failures.

Honeywell is also offering analyzers with which to service its new equipment, in addition to a microprocessor-based thermostat and electronic duct vent damper already on the market. Also planned for the near future are gas- and oil-furnace controllers.

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Usually, when the package gets smaller, so does the performance. For the OEM with big ideas and no place to put them, this means making a compromise on computer capability.

But all small packages are not equal, as the SCOUT NAKED MINI 4/04 demonstrates.

The form factor, to be sure, is rather remarkable. All boards are a mere 6.25" x 8.3."

But still more remarkable is the extraordinary performance produced by a machine this size.

The SCOUT NAKED MINI 4/04 CPU archilecture is fully compatible with other NAKED MINI 4 family members. SCOUT provides multiply/divide instructions, a real-time clock, power-fail and auto-restart as standard features. Floating point instructions are available as an optional feature.

What's more, SCOUT is word or byte addressable – with direct addressing of 128K bytes – and fully supports multiple DMA and interrupt devices.

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Your choices include: A RAM memory with up to 128K bytes. A RAM/EPROM memory. A remote console. A 16-channel analog-to-digital converter. An 8-channel relay output module. A parallel 16-bit I/O controller. A serial I/O controller. An extender card (to permit system expansion). Plus a prototype module and, last but not least, two +5V power supplies and card cages.

Obviously, a minicomputer that gives you the flexibility to configure so many ways is a lot more than just a hot-shot new computer. It's a computer system.

Predictably so, because ComputerAutomation has always been the place the pros go for systems-oriented minicomputers.

So from the word go, SCOUT gives you everything you need to succeed. In terms of size. In terms of 16-bit computer power. And because it's a complete system.

SO MUCH SOFTWARE, SO SOON?

Sure. Because SCOUT is a compatible member of the NAKED MINI 4 family.

For openers, there's our Real-Time Executive (RTX). It's precisely what you need for building your own real-time applications.

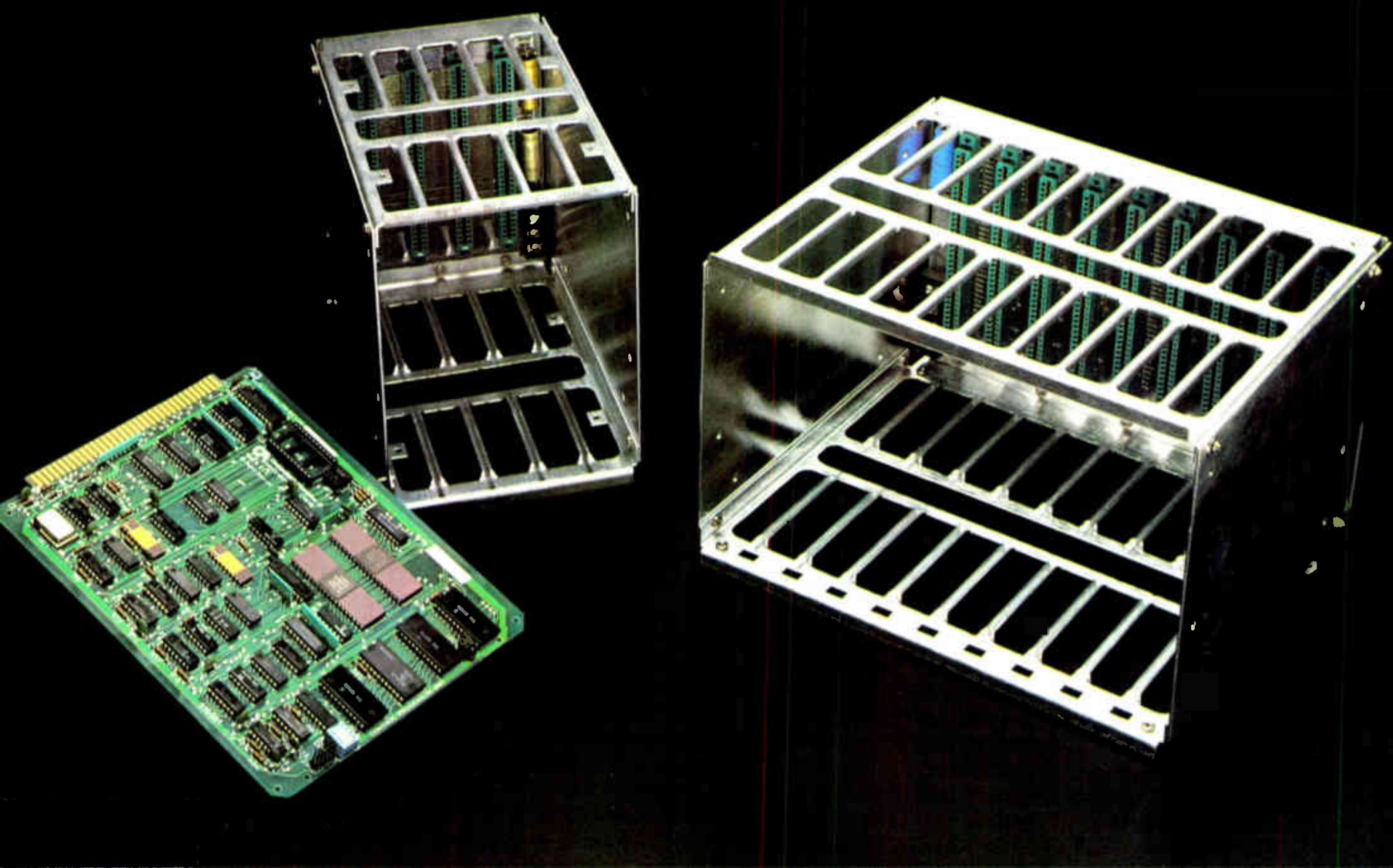
Also, SCOUT will execute any Fortran IV program you've compiled on another NAKED MINI 4 development system.

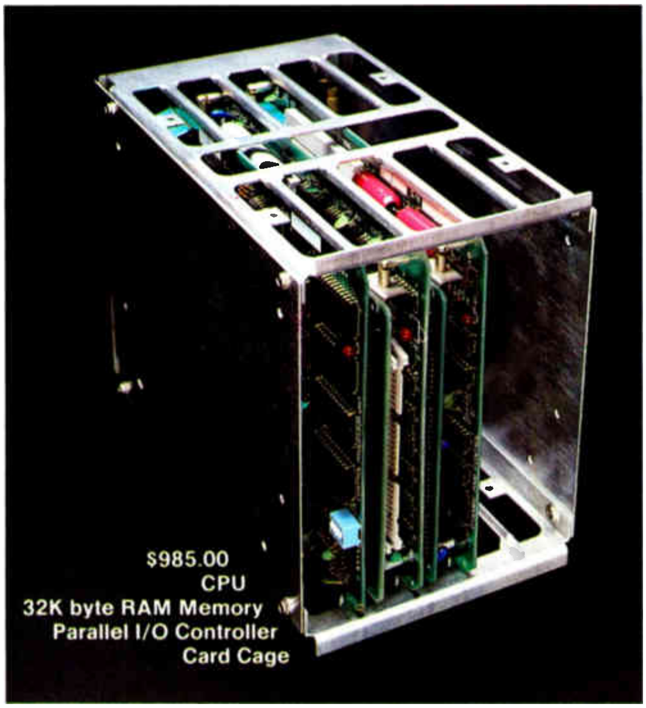
Then there's our special INTRACOMM™ communications package to make computer-to-computer communication between NAKED MINI-based systems a snap. You can communicate data, or you can down-line load application programs to a remotely-located SCOUT.

For program development, there's OMEGA 4, our general-purpose, memory-based assembly language development system that runs on SCOUT.

Or, you get the flexibility to develop SCOUT software on any other NAKED MINI family computer. And that gives you access to our powerful OS4 software development system, multi-terminal editor, extensive utilities and high-level languages.

And that gives you everything you need to succeed – in terms of software.





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Obviously you'd like your systems to be more competitive – and profitable.

So we suggest you do a little comparison shopping. Compare, for example, a typical SCOUT configuration consisting of, say, a CPU, 32K bytes of RAM memory, a parallel I/O and a 4-slot card cage.

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And that means, with SCOUT, you can trim your cost-of-product *and* beef-up your profit margins. All in one simple step.

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Because like every other Computer-Automation NAKED MINI computer, SCOUT is covered by the industry's only full-year warranty.

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Marine Corps over a period of five to seven years beginning in 1982.

The terminals are used to send data back and forth between a remote (field) location and a central data base (headquarters). The units can be used to format, transmit, receive, and display on a red LED panel measuring 3 by $4^1/_4$ inches, both alphanumeric and graphic information.

The material on the display is transmitted over standard military field radios or land lines. Via a programmable keyboard, the terminals will provide field forces with the ability to compose and edit both preformatted and text messages as well as map data, eliminating the need for long and potentially confusing voice transmissions. Lithium batteries will power the unit for weeks at a time. **-Ray Connolly**

Software

Pascal added to board tester

Chalk up another use for the Pascal high-level computer language as it picks up momentum in taking over programming chores of large and small systems alike. For its line of automatic testers for circuit boards, Computer Automation Inc. is offering a Pascal-based programming language that simplifies the writing of test programs. Called Integrated Circuit Design Language, or ICDL, it is part of an optional emulation package offered with the company's Capable ATE series of board testers.

It's not just that Pascal has the advantage in simplicity and structure over previous programming methods [*Electronics*, June 7, 1978, p. 111], notes Bradley Klein, applications engineer at Computer Automation's Industrial Products division, Irvine, Calif. "Creating software models of LSI chips for testing boards can't be done any other way." What worked with simple small- and medium-scale integrated parts flunked out when it ran up against the many complexities inherent in

Cut the cost of digital system checkout with Biomation's DTO-1.

There's a whole new approach to test, calibration and maintenance of digital systems. It's Biomation's DTO, the first Digital Testing Oscilloscope. Here's how it works. The DTO's front panel functions very much like a traditional oscilloscope but provides additional capabilities. It automates testing without having to worry about software implementation. Simply step through your test sequence once using the DTO to record the entire program on a tape cartridge. Then DTO plays it back to guide technicians, even setting up the instrument's front panel to match the reference program. All in all, DTO provides a faster, easier, far more accurate approach to the otherwise time-consuming, error-prone task of system checkout.

DTO-1: For production test.

Now there's a better way to move new products out of engineering and into production accompanied by a comprehensive production test program. Just use DTO to record the test sequence you want technicians to follow. Step by step, it enables them to compare the system under test with your "known good" system, automatically flagging any discrepancies. Compare DTO with the test equipment you're now using.

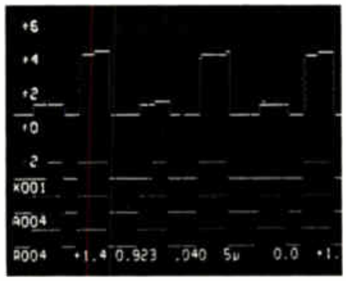
SYSTEM TEST CAPABILITY COMPARED

Testable system elements	Oscilloscope	Signature analyzer	In-circuit emulation with signature analysis	DTO-1
Power supplies	yes	no	no	yes
System clocks	yes	no	no	yes
Processor/control logic	no	no/yes	yes*	yes
Digital input/outputs	no	yes	yes*	yes
Analog I/O	yes	no	no	yes

*System must have a processor.

DTO-1: For calibration & repair.

The most sophisticated calibration and repair labs are using DTO to "document" digital systems they must service.



By developing a tape for each new piece of equipment and instrumentation, troubleshooting and recalibration is faster and more precise. The DTO's screen displays both reference traces and test traces simultaneously, highlighting any disagreement and enabling technicians to zero in on faults.

DTO-1: For facility maintenance.

When it may be weeks or months between repair and maintenance of complex digital systems, DTO brings technicans back up to speed in a hurry. DTO can be used to make a record of the system operation, so it remembers exactly how a perfectly functioning system operates. By following the test procedures and adjusting the system signals to match recorded logic traces, maintenance is virtually automated.

For details on how Biomation's DTO-1 can cut the cost of digital system checkout for you, write Gould Inc., Biomation Division, 4600 Old Ironsides Dr., Santa Clara, CA 95050.

Or, call for a demonstration. (408)988-6800

GOULD

developing an LSI model, he says.

He refers to writing test programs in assembly codes, which require routines to be broken down into microsteps, each expressed in very intricate machine instructions. "We tried to do it with the simplest LSI—shift registers, not microprocessors—and we just didn't have the brainpower. It was a bear," he says.

Simulated logic. The crux of testing LSI-crammed boards is creating the comprehensive models that can truly simulate every logic function of each part and of the entire board itself. "It literally is a software representation of chips," he explains.

These models then serve as software entities that become the ideal standards against which actual output responses of boards can be compared when automatic test patterns are generated. Typically, testing a board requires 4,000 to 5,000 individual test patterns.

The Pascal package operates with English-language command statements that are directly related to logic functions. So a user looking to test a board that has Zilog Z80 chips, for instance, "would crank in the manufacturer's coding and let the ICDL software take over."

In contrast to the industry's usual way of announcing a product long before delivery, Computer Automation has for the past year been quietly supplying customers with its package, which consists of software and extra memory modules to customers. "We've learned our lesson, and we did this the right way," says Ed Harrell, vice president of marketing for the division.

More than 31 Capable installations use the Pascal-based emulation package, primarily for board testing, but the package is also used in two cases for wringing bugs out of custom LSI chips, he says. The lowest price of a stand-alone Capable tester with the Pascal package is about $80,000. Adding it to an existing ATE unit runs up a tab in the $50,000 range. The overall response has been so positive, claims Harrell, that a users group meeting, to compare notes, took place in July at Fort Lauderdale, Fla. **-Larry Waller**

Washington newsletter

FCC approval for new Xerox service seen for early 1980

Approval of the Xerox Corp.'s digital, end-to-end business message service could come early next year. That would be a lightninglike timetable for the Federal Communications Commission, which got Xerox's proposal last November. Nevertheless, that is the conclusion being drawn from the FCC's 6-to-0 approval of a combination notice of rule making and inquiry before it adjourned early this month. The service—called XTEN for Xerox Telecommunications Network—would use existing terrestrial microwave satellite facilities for intercity transmission and digital communications service in the 10.55-to-10.68-GHz band to reach transceivers on a customer's premises. Though the Stamford, Conn., firm sought for at least 90 MHz for the service, **the FCC ruling proposed use of only 60 MHz initially, with another 30 MHz held in reserve** if the demand warrants.

AEA pushes for more favorable stock options

The American Electronics Association is backing legislation that would mean more favorable tax treatment for electronics company employees holding stock options. The AEA-initiated measure, introduced into the House of Representatives earlier this month, **would restore the "restricted" stock option** by which an employee pays capital gains tax only when he or she sells the stock. An option means that an employee may buy his or her company's stock at the option price even though the actual trading price may be higher. Since 1976, however, an employee pays both ordinary income tax on the difference between his option price and the higher market price when purchased and capital gains tax when sold. The AEA contends that the change would help new electronics companies attract top-flight engineers.

Color TV sales up 2.8% in July; imports decline

The good news for U. S. color TV makers is that July sales to dealers rose 2.8% from last July's level to 686,629 units, pushing volume for the first seven months up 1.3% to more than 5.3 million sets. At the same time, **imports in the second quarter were cut in half** compared with the same period in 1978, dropping to 332,358. The decrease left color TV imports for the first six months at 754,717 sets, down 37.8%. Sales of monochrome receivers—with most U. S. brands produced offshore—showed different trends. July sales dropped 18.4% to 371,380 units, but at 3.1 million sets, volume for the first seven months was 2.8% ahead of last year. In addition, black-and-white imports rose 5.2% to nearly 1.5 million sets, raising the first-half total to 2.6 million, an increase of 2.1%.

Air Force splits Samso into two new commands

U. S. Air Force space and missile system contractors will again have two organizations to deal with starting on Oct. 1, instead of one, as the service splits its Space and Missile System Organization (Samso) into two new California-based organizations: the Ballistic Missile Office (BMO) at Norton Air Force Base and the Space Service Division (SSD) at the Vandenberg base. The realignment "reflects the increasing importance of the development of the new land-based intercontinental missile, the MX, and the expanded role of Air Force space activities," says Air Force secretary Hans M. Mark. The two new organizations, similar to those that existed 12 years ago before being combined into Samso, will report to the Systems Command, as did Samso. Personnel changes will be minimal, and no reductions in staff are expected.

Washington commentary

Making air traffic control work

The Federal Aviation Administration's proposal early this month to spend $100 million by 1982 on upgrading airport safety—and its own image—represents a late start based on makeshift plans. The aim is to improve 86 satellite airports for smaller aircraft near 56 hub airports in as many cities, but that is small potatoes in view of the size of the FAA's Airport/Airways Trust Fund. Designed to pay for the program with taxes on airport users, this fund has accumulated more than $2.5 billion in a decade in which air traffic has soared yet only five new satellite airports have been built to relieve congestion around major terminals.

The makeshift nature of the FAA proposal is evident from the fact that 24 of the 55 new instrument landing systems to be installed will be systems already on order. These will not be used to replace older systems, as originally planned, but will be diverted to airports that have no ILS at all. In all, $40 million will be spent for instrument and visual landing aids and automated weather-reporting systems for all 55 fields.

The program has been "a little accelerated," FAA administrator Langhorne Bond concedes, by criticisms of the congestion around San Diego's Lindbergh Field that produced last year's mid-air collision between a small, general-aviation Cessna practicing ILS approaches and a Boeing 727 of Pacific Southwest Airlines. The Cessna was there because none of San Diego's three reliever airports has an ILS.

The ILS shortage

As for the FAA's tardiness in dealing with the problem, instrument landing systems exist in only 29 of the nation's 147 airports designated as relievers, and 42% of those fields will still be without ILS when the FAA's $100 million effort is completed. The General Aviation Manufacturers Association makes a valid point when it complains that "instrument landing systems don't cost that much—about $250,000 installed. The annual interest earned by the huge uncommitted surplus in the Airport/Airways Trust Fund would itself pay for 1,000 or more instrument landing systems."

But the issue is not as simple as spending the trust fund surplus, as GAMA—and the Congress—well know. The Congress is still debating renewal of the Airport/Airways Development Act, the source of the trust fund and set to expire in 1980. Income from the trust comes from an 8% tax on airline tickets, a 5% tax on air cargo weight bills, a $3 departure fee on international passengers, a 7-cents-a-gallon aviation fuel tax, and registration and other fees.

The heart of the problem is that the U.S. Government operates under a unified budget in which all of this money, like Social Security taxes, counts as income to its general treasury and is not necessarily related to expenditures, which must be authorized by the Congress. A trust fund that brings in more than is spent can therefore be used to hold down the overall Federal deficit.

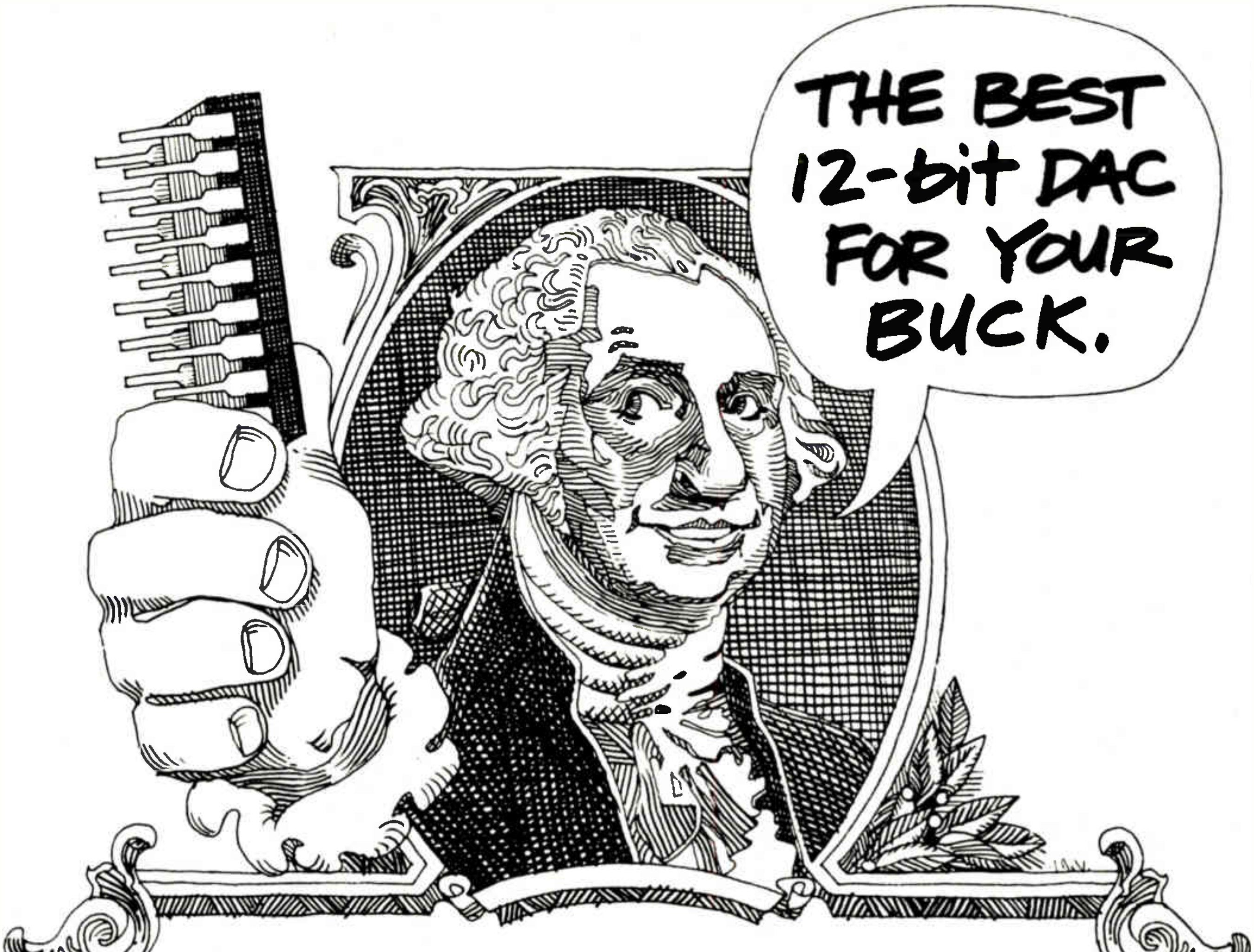
Matching money with plans

How did the trust become so big? After the original act was passed, the FAA sought to use the fund to cover operating and personnel costs as well as improve air safety. A 1971 congressional amendment prohibited using the money to pay FAA personnel, although a 1976 change allowed some operational costs to be covered by the fund. But income to the fund continues to far exceed FAA outlays for research and development on systems and airports, even though the Congress set minimum expenditure levels in the original law. Jimmy Carter's budget for fiscal 1980 calls for an obligatory level below the authorized minimum, for example.

Under an Administration proposal in April to extend the law five years through 1985, the trust fund would again attempt to cover FAA operating and maintenance costs, including salaries of air traffic controllers and technicians. The price for this would be $8 billion, compared with $6.7 billion for safety and capital outlays, leaving a $1.8 billion surplus at the end of the five years.

Airport users like GAMA dispute these priorities, of course. They want the trust fund spent for airports and equipment first, with FAA operating expenses covered by whatever might be left. However, such arguments only confuse the issue further, for airports and equipment cannot operate without trained personnel, and without people the equipment is useless.

What is more critical to effective use of the trust fund in the public interest is to get the FAA to recognize, plan, and budget for air traffic control before disaster strikes. With such a coordinated program, the responsibility for approval or disapproval will then rest squarely on the White House and the Congress where it belongs. Without it, all blame for inaction must continue to fall on the FAA. —**Ray Connolly**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The L529 and L527 quickly detect a high percentage of the faults most commonly found on circuit boards: shorts, opens, and missing, backward or wrong-value components.

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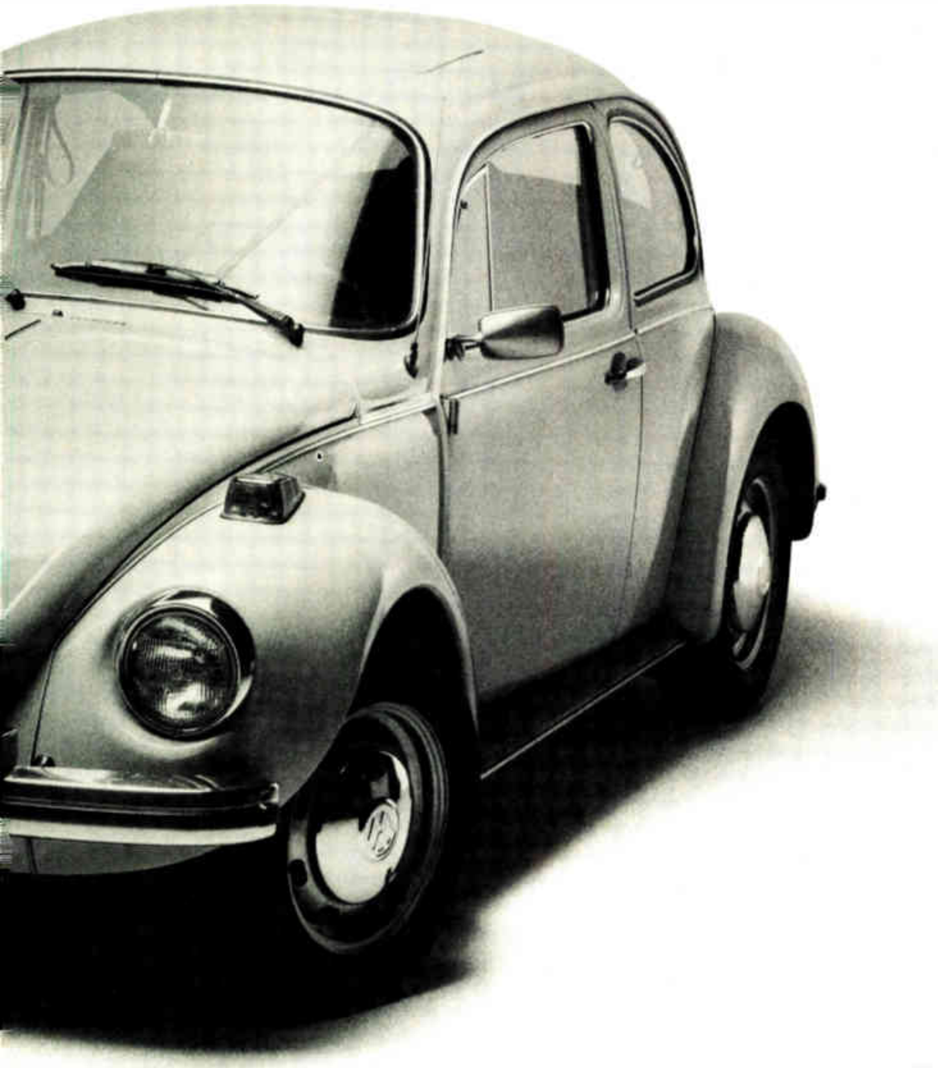

AND IS PRACTICAL AS A BEETLE?

Simple programming.

Teradyne in-circuit test systems self-learn from good boards and use pre-planned test routines. As a result, programming is simplified to the point that a junior technician can program a typical medium complexity, 50-IC board in only a day or two.

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Our feeling is that an in-circuit test system should be easy on the pocketbook, both when you buy it and when you operate it.

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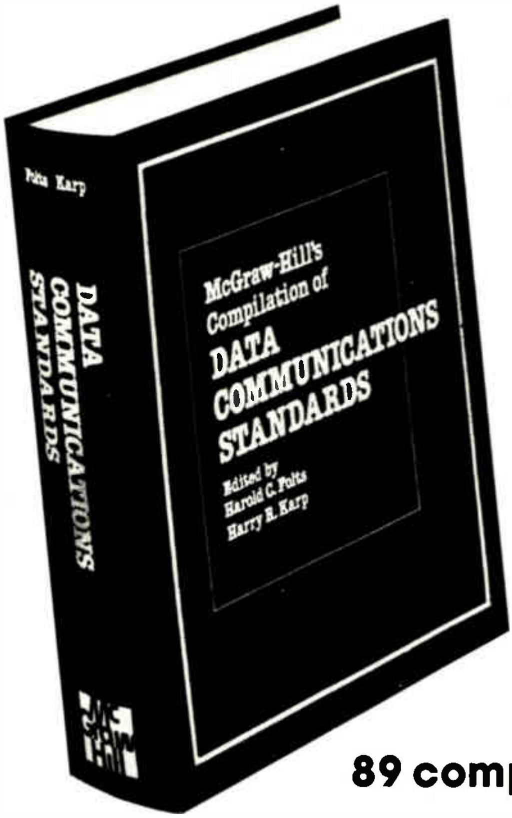
Circle 63 on reader service card



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Consultative Committee for International Telephone and Telegraph
43 standards, including...

V.2	Power levels for data transmission over telephone lines
V.15	Use of acoustic coupling for data transmission
V.54	Loop test devices for modems (and provisional amendments, May 1977)
X.25	Interface for terminals operating in the packet mode on public data networks
X.28	Interface for a start/stop mode on a public data network situated in the same country
X.29	Procedures for exchange of control information and user data between a packet mode DTE and a packet assembly/disassembly facility (PAD)
X.95	Network parameters in public data networks

Electronic Industries Association
13 standards, including...

RS-232C	Interface between data terminal equipment and data communication equipment employing serial binary data interchange
RS-269B	Synchronous signaling rates for data transmission
RS-363	Standards for specifying signal quality for transmitting and receiving data processing terminal equipments using serial data transmission at the interface with non-synchronous data communication equipment
RS-449	General purpose 37-position and 9-position interface for data terminal equipment and data circuit-terminating equipment employing serial-binary data interchange

International Organization for Standardization
11 standards, including...

ISO 646-1973	7-bit coded character set for information processing interchange
ISO 1745-1975	Information processing—basic mode control procedures for data communications systems
ISO 3309-1976	Data communication—high-level data link control procedures—frame structure

American National Standards Institute
11 standards, including...

X3.4	Code of information interchange
X3.24	Signal quality at interface between data processing technical equipment for synchronous data transmission
X3.36	Synchronous high-speed data signaling rates between data terminal equipment and data communications equipment
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Federal Standards
11 standards, including...

FED-STD-1003	Bit oriented data link control procedures
FED-STD-1010	ASCII bit sequencing for serial-by-bit transmission
FED-STD-1011	Character structure for serial-by-bit ASCII transmission
FED-STD-1012	Character structure for parallel-by-bit ASCII transmission

International newsletter

Toshiba readies 16-K static C-MOS RAM

Toshiba Corp. will start supplying samples in October of its TC5516P 16-K complementary-MOS static random-access memory, with sales to start at year-end. **The chip's 2-K-by-8-bit arrangement and 24-pin plastic package make it pin-compatible with the industry-standard 2716** electrically programmable read-only memory. It operates from a single +5-V power supply and features the fast access time of 250 ns. It will compete with the recently announced n-channel 16-K static RAMs from American Microsystems and Texas Instruments in microprocessor systems.

Hi-fi radio receiver from Philips to have highly accurate tuning

Look for the Netherlands' NV Philips Gloeilampenfabrieken to come out soon with a high-fidelity radio receiver whose microprocessor-controlled digital tuning system achieves an accuracy unattainable by mechanical means and obviates the need for automatic frequency control or for a ratio detector. In the receiver's fm range tuning is in 10-kHz steps and in its a-m and long-wave ranges in 0.5-kHz steps, with **the maximum error in all three ranges as low as 0.001%.** The receiver, designated 799 TA-DIG, will be shown for the first time at the Aug. 24–Sept. 2 International Radio and Television Exhibition in West Berlin.

Plessey Microsystems spin-off may take over holograpahic memories

Plessey Microsystems Ltd. is stopping its long-standing holographic memory program even before its first products—a read/write memory and a read-only memory for archival applications—have reached the market. But a new company, established by Peter Waterworth, an ex-Plessey engineer, **could be selling the read-only version within two months if negotiations with Plessey and with his financial backers are successful.** The spin-off company has no immediate plans for the more complex read/write memory but instead will concentrate on applications in scientific, seismic, governmental, and other fields. Holographic-memory systems offer up to a thousandfold increase in data density compared with magnetic tape, with extremely high data integrity and a data-transfer rate comparable to that of magnetic tape. In the prototype system built by Plessey, up to 10^{11} bytes of data can be stored on a 1,000-meter film spool having a 16-mm track, using a low-cost helium-neon laser. The read/write data-transfer rate is 800 kilobytes per second. Plessey, meanwhile, will be looking at ways to exploit its patented photochromic technology, developed for the read/write version, in other products.

UK report urges tie up with Americans or Japanese

Britain's computer industry should consider alliances with U. S. or Japanese companies as a means of increasing its competitive strength, according to a report from the National Economic Development Office, a tripartite planning group involving the government, management, and the trade unions. Says the report, **"The battle between the Japanese and the Americans for world computer markets may prove to be the single most important factor in the 1980s** in determining the structure of the worldwide supply industry, and casualties could be considerable." One answer to this threat would be to seek alliances in the U. S. or Japan, provided that such associations were genuine partnerships embracing manufacturing, research and development, and marketing. The report also looks to foreign-owned multinational computer companies to increase local manufacture of computers and subassemblies to cut a growing deficit in the balance of payments that was already running at $400 million in 1978.

Nonvolatile static RAM uses MNOS capacitors to retain data one year

An n-channel high-speed nonvolatile static random-access memory utilizing metal-nitride-oxide-semiconductor capacitors has been prototyped at the semiconductor device engineering lab of Toshiba Corp., Kawasaki. The design, to be discussed at the Aug. 27–29 International Conference on Solid State Devices in Tokyo, uses six transistors per cell, but adds two MNOS capacitors to retain data during power failure or power-down. Memory retention is at least one year, and Toshiba figures that **the MNOS elements will withstand about 100,000 cycles,** or about 30 a day for 10 years.

During normal operation, the part looks like a 5-V single-supply n-MOS static RAM with an access time of 100 ns. When the supply voltage starts to fall, a −30-V erase pulse resets the MNOS capacitors; it is followed by a +30-V pulse that stores the data in the capacitors for each cell. At power-up, a read pulse sets each cell according to the state of the capacitors. In the retention mode, the erase pulse erases the entire chip, but in the RAM mode information can be changed a bit at a time. A special integrated circuit generates the erase and read pulses, and the ±30 V comes from exernal power supplies. Toshiba researchers feel that the design is suitable for 4-K and larger devices. The cost will be higher than that of standard static RAMs because of the MNOS processing. However, company engineers estimate prices comparable to those of complementary-MOS RAMs, which require batteries for retention.

Shielding material cuts cable production costs, says French firm

France's Laboratoire d'Electronique et d'Automatique Dauphinois (LEAD) is seeking more applications for the plastic-based magnetic material it developed for use in high-immunity coaxial cable. The black rubbery substance, dubbed Musorb by Ferdy Mayer, founder and president of the Grenoble-based firm, consists of magnetic grains held together in a plastic matrix. It is designed to replace one of the braided copper shields and one layer of magnetic tape in a triple-shielded cable. The advantage, according to Mayer, is that Musorb can be applied with extrusion techniques, thereby lowering cable production costs by 25% to 30%. He says that **it can also be used to make a variety of inductive components,** such as rf chokes and high-frequency and ultrahigh-frequency transformers, replacing traditional ferrites. Mayer also contends that it saturates magnetically much less readily than traditional Permalloy or Mumetal and is also a good thermal conductor, making heat dissipation less of a problem. The temperature limit depends on the plastic used.

U. S.–West German cooperation ahead for TRSB landing systems

West Germany's Ministry for Research and Technology and the U. S. Department of Transportation have agreed in principle to cooperate in the development of electronic navigation and landing systems for commercial aircraft of the 1980s. The agreement stems from a **recommendation by the International Civil Aviation Organization (ICAO) to incorporate West German–developed equipment** into the U. S.-Australian–designed time-reference scanning-beam (TRSB) microwave landing system, in whose favor the ICAO had decided early last year [*Electronics*, April 27, 1978, p. 59]. The gear, called a distance equipment-supported azimuth system, or DAS, and developed by the ITT affiliate Standard Elektrik Lorenz AG, adds a distance-measuring capability over a 360° azimuth to the TRSB landing system, thus making possible localizing aircraft landing from any direction [*Electronics*, Oct. 26, 1978, p. 63].

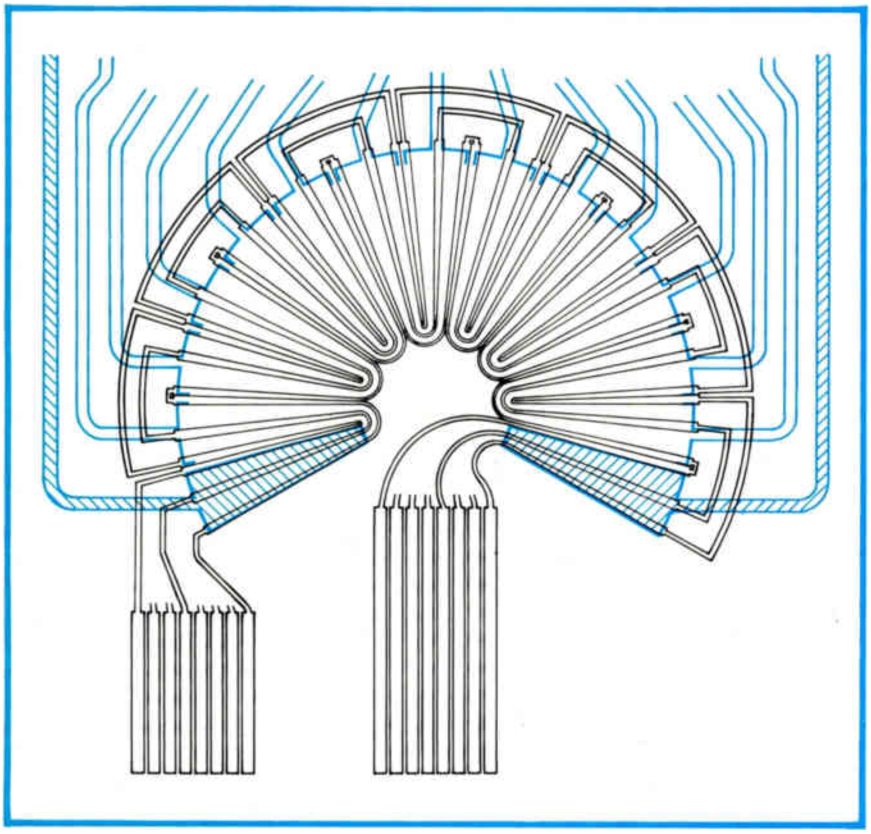
Addressing scheme overcomes problems for pointer LCD

by Kevin Smith, London bureau manager

Continuous-addressing technique minimizes temperature sensitivity, allows wide viewing angle

The electromechanical pointer display has held its own against digital displays in many applications because it can convey at a glance both absolute values and rates of change. But now researchers at the Royal Signals and Radar Establishment in Malvern, England, have come up with a practical dye-phase-change liquid-crystal analog display in which the pointer shows up as a blue sector on a light gray background.

Advantages. Ian Shanks, its developer, says the new display can be directly driven by logic circuits, consumes little power, operates over the full temperature range of the liquid-crystal material used without the need for temperature compensation, and drastically reduces the number of display connections compared with previous approaches. The addressing technique employed can easily be extended to drive clock displays having two or three hands of different lengths.



Meandering. Pointer LCD from Great Britain has 120 positions using 23 electrodes: 15 on backplane (color); 8, in the form of weaving lines, on frontplane (3 shown).

The prototype display is driven by eight standard 15-volt complementary-MOS integrated circuits clocked at 800 hertz. But, says Shanks, it could be powered by a single custom C-MOS large-scale integrated circuit with an on-chip analog-to-digital converter and driver electronics. At least one UK company is considering taking up the idea.

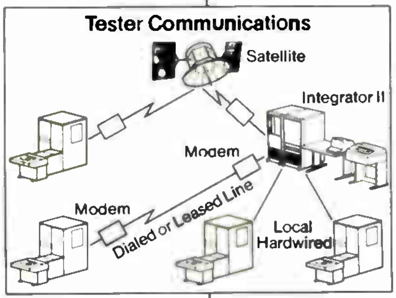
One big problem with LCDs is that the turn-on threshold is highly sensitive to temperature, so that display performance involves a compromise between operating temperature range and viewing angle. Though analog LCDs have already turned up in some watches, they are worn on the wrist and are at body temperature. Aerospace and automotive applications present tougher problems.

Temperature compensation in the display drive circuitry is one way to go, but Shanks' novel addressing technique provides a more complete solution [*Electronics*, March 29, p. 70]. It makes use of the correlation properties of differently shaped waveforms—in this case, binary sequences—to drive selected display segments continuously. The electrodes are arranged and driven in such a way that a high root-mean-square voltage appears across all segments of the display except the selected pointer segment, which has zero voltage across it, turning it off. Thus a blue pointer appears on a light gray, flicker-free background.

The display uses dye-phase-change liquid crystal with a 5-V threshold and electrodes formed

INTRODUCING INTEGRATOR® II. ONE PICTURE IS WORTH THOUSANDS OF WORDS.

Chances are you have Fairchild test systems spread around your plants, and your plants have spread around the world. Each of those test systems—Sentry,® Sentinel™ and Xincom—is spewing out data. Data that's important to you. To your quality control. To your customers. But, until Integrator II, Fairchild's host computer, there was no easy way for you to effectively use that data.



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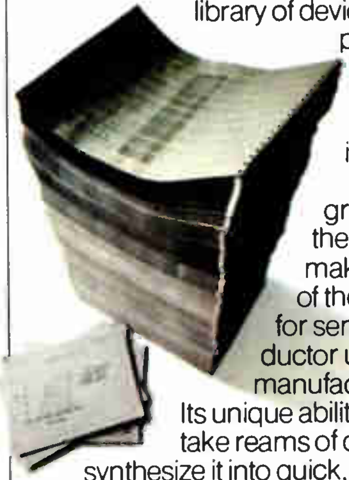

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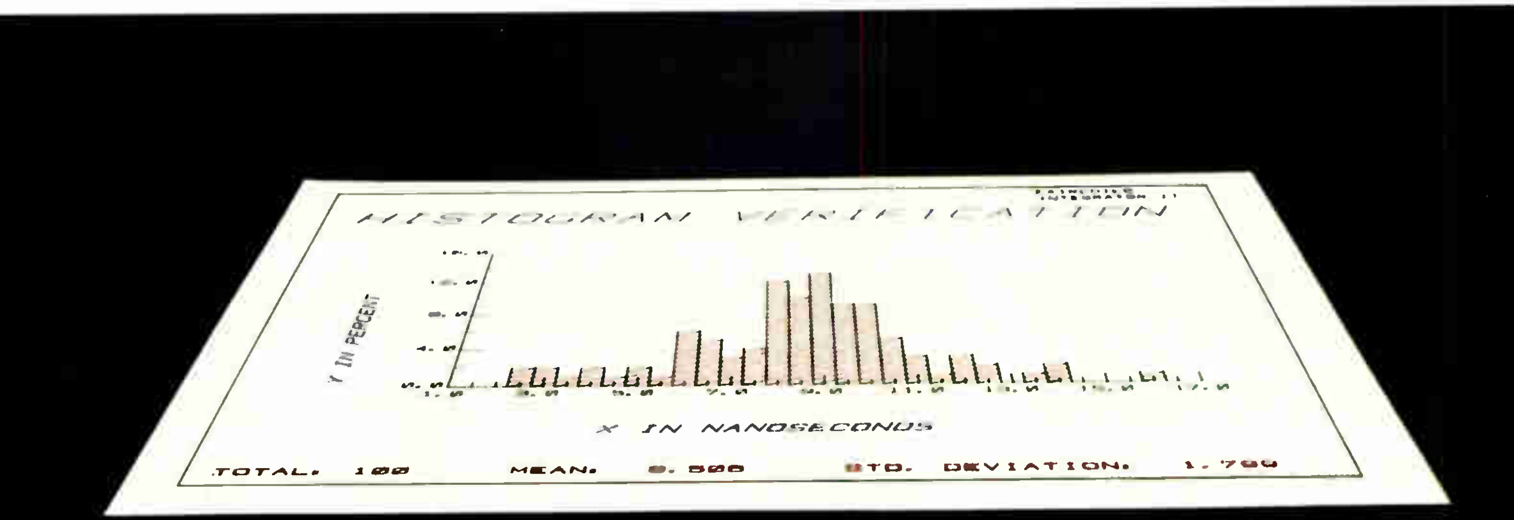
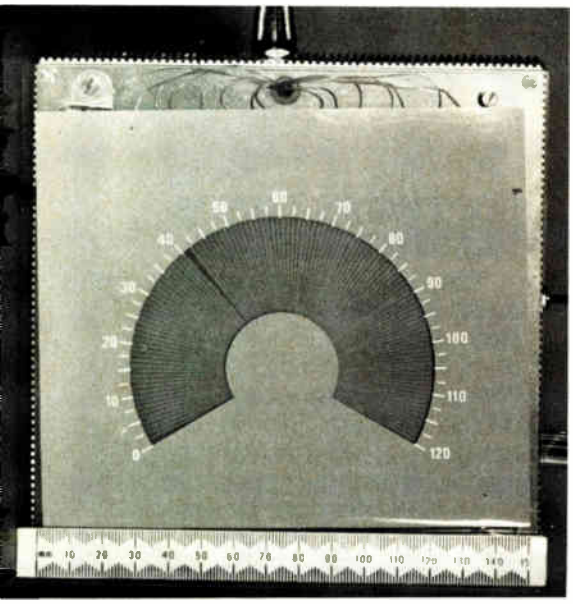


Circle 71 on reader service card



Blue on gray. LCD's blue pointer segment is off; background, gray, is uniformally on.

photolithographically from indium tin oxide. It "has good brightness and contrast, excellent viewing angle characteristics, and a uniform appearance," Shanks says.

Few pins. The matrix scheme minimizes the number of display connections. The display's backplane has 15 electrode segments, and the frontplane electrodes are eight meandering lines, all of which pass over each of the 15 back segments. The result is 120 pointer positions addressable by 23 pins.

The driving waveforms are generated using a shift register with an exclusive-OR feedback circuit. This circuit puts out a pseudo-random binary sequence. The 16 waveforms used possess the property that the voltage difference between any two of them has a constant rms value.

Different waveforms are applied simultaneously to each backplane segment. The sixteenth waveform is applied to all the meandering frontplane electrodes except the one selected to define the pointer. That one electrode has the same binary sequence applied to it as the rear segment in which the pointer is to appear. Thus the voltage difference between these two electrodes is zero. But the entire background area has a uniform high rms voltage across it and consequently appears evenly illuminated from all viewing angles.

The addressing method can be further simplified at a slight increase in the complexity of the electronics, according to Shanks. This variation has all the rear segments receiving one waveform except the segment containing the pointer, which is driven by a second waveform. All the meandering front electrodes except that selected to denote the pointer are driven by a third waveform. This method reduces the number of pseudo-random bits needed in the waveform patterns to three. It also brings the clock frequency down from 800 Hz to 90 Hz, with a corresponding cut in power consumption.

A similar meandering matrix of electrodes could be designed for a clock display with a very low pin count. "A two-hand clock that resolves individual minutes would need only 23 connections, and a three-hand display resolving individual seconds would have only 28 connections," Shanks says.

He also sees an important market in replacing various types of electromechanical displays. Unlike LCDs, these devices exhibit inertial lag and overshoot when tracking a varying quantity.

Japan

Tiny chip resistors simplify assembly

A new type of thick-film chip resistor is finding its way into compact Japanese consumer products such as super-thin pocket radios, calculators, TV tuners, and frequency-modulation tuners. The electrode design allows the chips to be wave-soldered directly to the bottom of a printed-circuit board in the same operation as the soldering of the rest of the board's components.

Toyo Electronics Industry Corp. (whose U.S. marketing arm is R-Ohm Corp., Irvine, Calif.) packages these chips in cartridges that allow automatic attachment to circuit boards. The resistors are built on an alumina substrate and measure 3 by 1.5 by 0.5 millimeters. A ruthenium-oxide resistive element is deposited so that it overlaps end electrodes made of a silver-palladium glass-frit paste.

Other chip resistors do not have the electrodes extending around the ends of the chip, so that they cannot be soldered directly to the circuit board face up. In addition, ordinary solder tends to rob the electrodes of silver and dissolve them. (Adding silver to the solder solves this problem but increases both the price and the melting temperature of the solder.) These chip resistors are connected to a board by wire bonding—an expensive, labor-intensive process.

How it works. In the Kyoto company's new process, the chips are formed on a large sheet of prescored alumina substrate. The top portion of the electrodes, the resistive element, and an overlying glass protective coat are first formed, and the rows of chips are snapped apart, separating the electrodes of adjacent chips. The long sides of the chips are still joined together to form the rows, which are stacked. The part of the electrode that extends around the chip's ends is then screened on.

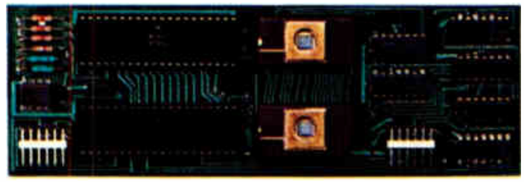
The electrodes extend slightly (about 0.25 mm) onto the bottom of the chip. This extension is minimized to allow the resistor to bridge a wiring trace on the board between the two traces it is connected to without danger of shorting.

In order to solve the soldering problem, Toyo adds a nickel barrier layer to the electrode, to protect the Ag-Pd layer, and then a tin outer layer, to facilitate soldering to the nickel. The Ag-Pd paste is specially formulated to withstand attack by the nickel-plating solution. (The primary purpose of the glass layer over the resistance element is also to protect the ruthenium oxide from this plating solution.)

After the three-layer electrodes are formed and the resistors snapped apart, they are sand-blasted to trim them to the specified resistance. This removes a small area of the glass coating and the resistive film without degrading the chip's characteristics. Heat dissipation remains excel-

Once you compare our new 191 digital multimeter to ordinary 5½-digit DMMs, we think you'll readily agree that it outclasses its class. For good reason.

The 191 is a ±200,000-count DMM capable of 0.004% accuracy and 1μV/1mΩ sensitivity. It delivers unsurpassed accuracy, faster, because firmware in the 6802-based μcomputer has replaced slower, less precise analog circuitry.



Displayed data is updated at the fastest rate of digit change readable by the human eye—4 conversions per second. Settling time of 0.5 seconds is easily half that of the 191's nearest competitor.

The μP combines both charge-balance and single-slope conversion techniques. Every displayed reading is automatically corrected for zero and gain drift.

If you've ever had to contend with the frustration of potentiometer zeroing, you'll appreciate the 191's null function. Automatic arithmetical correction of residual error is standard. With a touch of the button you can buck out any in-range signal, large or small.

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You don't need low-level noise either. So the 191 automatically suppresses it. The 191's non-linear digital filter is entirely free of dielectric absorption and leakage problems associated with analog techniques. On the 200mV and 200Ω ranges, the filter effectively attenuates noise by displaying a running average of the 8 previous readings. Yet it instantly displays input changes of 10 digits or more.

Another exclusive of the 191 is 2 and 4-terminal measurement from 1mΩ to 20MΩ across six ranges. Simply adding two more sense leads automatically enables Kelvin measurements. No changing input terminal links or even pushbutton settings.

And, finally, since μP design reduces component count, the 191 requires less servicing and calibration, increasing reliability and stability.

At $499 without plug-in ACV, the 191 is today's performance/value leader in 5½-digit DMMs. A year from now most people will agree. But you probably don't need that much time to make up your mind. And we're ready to help you with a demonstration or additional information. Call 800-321-0560. In Ohio, 216-248-0400.

Next year you'll be glad you did.

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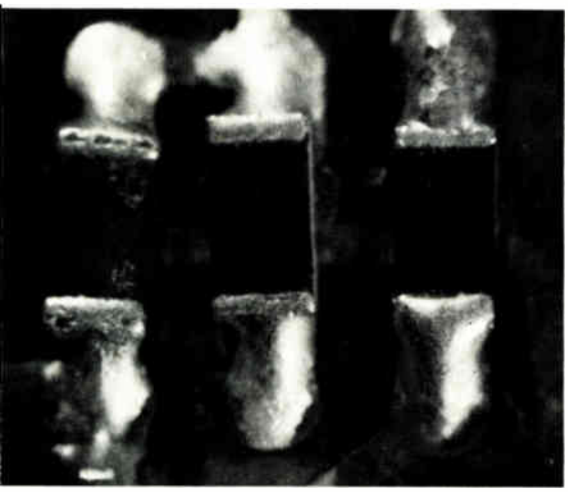
Circle #72 for literature

Circle #73 for demonstration



One time. Small chip resistors are mounted and wave-soldered with the rest of a board's components. Chip at left is capacitor.

lent because of the alumina substrate's ability to conduct heat.

The chips, stacked in rectangular plastic tubes, are pushed upward by automatic equipment so that their bottom sides adhere to a small drop of epoxy adhesive on the circuit board. When the epoxy cures, the boards are ready for soldering. Solder flows up the side of the electrode, making a dependable connection.

Comparably sized multilayer chip capacitors have been available for some time, as have miniature molded transistors that can be similarly attached to the bottom of pc boards; the advent of wave-solderable chip resistors thus fills a missing production link. The capacitors' electrodes also wrap around the chip's ends—this was inherent in the their design, as the end electrode connects the multiple layers of the capacitor elements. To form these electrodes, though, one row of capacitor chips must be dipped at a time, making them more costly than the stack-processed resistors. **-Charles Cohen**

The Netherlands

Audio cassette machine records and searches for coded markers

The ubiquitous though staid audio cassette recorder has not been forgotten by its designers, as will be evident at the International Radio and Television Exhibition opening Aug. 24 in West Berlin. There, at Europe's biggest entertainment electronics show, NV Philips Gloeilampenfabrieken of the Netherlands will unveil a stereo high-fidelity audio cassette recorder, the model N2554, that eliminates a time-consuming chore—locating the beginning of the section to be played.

The new machine does this automatically with what Philips calls computer-coded search. Simple enough, it asks the user to choose a code number via a set of push buttons that the microcomputer-controlled system, built around a Mostek 3870 8-bit device, then places as a magnetic marker before each segment as it is recorded.

On playback, a special magnetic head looks for the desired marker as the cassette moves through its fast-wind mode. When the head picks it up, the drive mechanism is switched to the slower playback speed and the material is played back.

To be sure, systems that perform a kind of search operation already exist. One used on many recorders is basically mechanical, coupling a counter to the take-up reel. Its disadvantage, besides a lack of standardization among recorders, is a lack of precision.

Another system uses no-signal areas between individual segments as the criterion for recognition. This scheme is unreliable, Philips points out, because it cannot distinguish between the true no-signal areas on the tape and the long pauses often encountered in, for example, classical music.

Positive start. The CCS system, in contrast, identifies the beginning positively. Moreover, not only does it play back segments in any sequence, but segments may be replayed using a repeat button on the front panel.

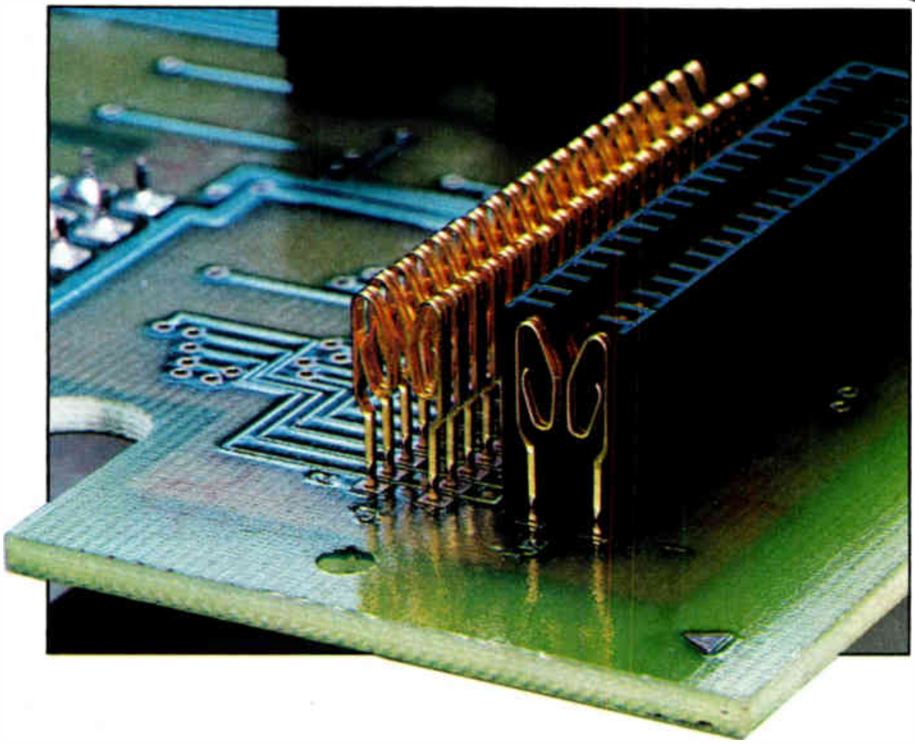
As Johannes Kerssen, head of audio recording development at Philips' Eindhoven facilities, explains it, the magnetic markers are recorded on the same two tracks used for the audio signals. Each marker consists of sine-wave pulses that stand for a seven-digit code number. The logic 1s and 0s making up that number are represented, respectively, by the presence or absence of a sine wave.

At the beginning and end of the marker pulse train are three more sine-wave pulses. These serve as synchronization signals for the recorder's marker-decoding circuitry during readout. The frequency of the sine waves is only 5 hertz. This low value, Kerssen says, makes the markers inaudible and provides positive marker recognition even during fast winding.

The sine waves are recorded with

Smart deck. Philips' audio cassette unit can record inaudible code signals to mark the start of each taped selection; a special head reads the codes even during fast winding.

Expanding the parameters of press-fit technology



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Circle 75 on reader service card

the same head that records the audio signals. However, that head would not be sensitive enough for reading out the sine waves. The special read head responds to the field itself instead of to magnetic-field variations with respect to time, as does a conventional head. The read head works on the familiar magnetoresistive principle whereby a thin nickel-iron film deposited on the head changes its resistance when subjected to a magnetic field. This resistance change signals the presence of a field.

The recorder is a top-of-the-line model (see photo, p. 74). It will sell for about $950 in Europe, offering lots of special features like dynamic noise limiting, Dolby noise reduction, and a post-fading system. It also will work with the relatively new "metal" cassettes. Using tape coated with very fine needle-shaped particles of pure iron, these cassettes yield a very wide frequency response ranging from 30 Hz to 20 kilohertz and a signal-to-noise ratio of better than 57 decibels. **-John Gosch**

Controlled environment for the very few

A Paris firm called International Home Systems SA is offering computer systems set up to manage the environment in buildings and adjust it to suit the owners' tastes. The systems are designed to handle regulation of temperature, humidity, and ionization of the air; communications; security; and information. The modular terminals employed use a pictographic coding system to overcome language-barrier problems in international institutions such as hotels.

The price tag does not indicate a high-volume market as yet. The first system, to be installed next year in a $4 million Belgian rest home, will cost almost $500,000. It uses a minicomputer and more than 100 distributed microprocessors. The cost for smaller systems for a proposed luxury development of 150 houses on the Spanish resort island of Ibiza would run about $25,000 per house, with the houses to be in the $200,000 to $400,000 class. Pierre Sarda, IHS's chairman, says that he plans a version for a 400-unit "economy" housing project. Houses costing some $65,000 each would have $11,500 worth of computerization.

-James Smith, McGraw-Hill World News

Japan

Software group faces linguistic problems

A joint government-industry software effort is laying groundwork for the coming information-processing age in Japan. Most present software has been written in English-based languages, but it is clearly not in Japan's interests to require English training for everyone programming or using computers.

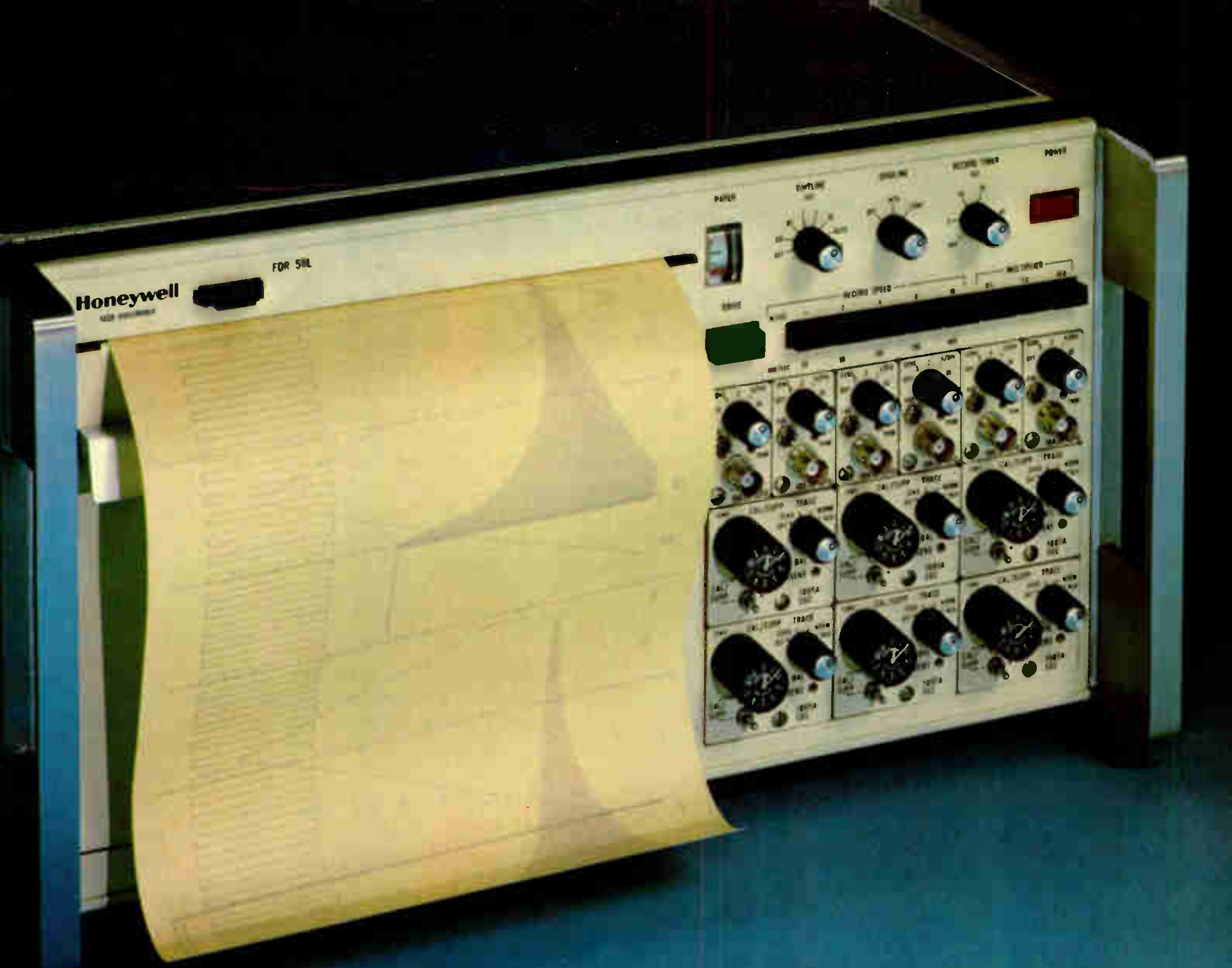
The five-year program, approved by the government last January [*Electronics*, Jan. 18, p. 63, and July 19, p. 63], involves designing an operating system for handling Japanese-language information. Participants also hope to anticipate problems that will arise with computers designed after the project's completion in 1983. They will be exploring basic software technology, network management, data base management, virtual machine management, and very high-level language processing. One major difficulty will be the need to accommodate processing of the huge applications software base that will have accumulated by 1983: it may not be practical to make a clean break with the American-influenced past.

Orthography. The U.S. model for operating systems cannot be followed because of the vast orthographical differences between the two languages. The American Standard Code for Information Interchange, with only 128 characters, can be handled by a single byte. The Japanese Graphic Character Set, for Information Exchange adopted last year, includes 6,349 Chinese characters, 169 for the Japanese hiragana and katakana syllabaries, the 10 Arabic numerals, 108 symbols, and the Roman, Greek, and Russian alphabets. This set requires 2 bytes for each character. Although many Japanese computers already handle Japanese-language information, their operating systems are usually extensions of those developed for U.S. systems and may be far from optimum for dealing with 2-byte characters.

Software will be the main thrust, but development of basic peripheral-equipment technology will also receive attention. Although applicable to word processing, this high-risk technology will be for more general computer input/output. Most present systems for Japanese-language computer entry by unskilled users require a large, cumbersome matrix input tablet with several thousand locations. Phonetic input in the katakana syllabary will be explored, but as no unique scheme exists for converting kana writing to a combination of kana and kanji, the computer would need some of the attributes of a language-translation machine—at present one of the least successful computer applications.

Voice recognition and Japanese hand written language optical character recognition will also be tackled. Less risky undertakings include high-speed printers using lasers or other advanced techniques, high-capacity disks, and bubble memories.

The 10 companies in the research association are Fujitsu Ltd., Hitachi Ltd., Mitsubishi Electric Corp., and their joint venture Computer Development Laboratories; Nippon Electric Co., Toshiba Corp., and their joint venture NEC-Toshiba Information Systems Inc.; and Matsushita Communication Industrial Co., Oki Electric Industry Co., and Sharp Corp. The top positions in the association will rotate yearly; Kazuo Iwata of Toshiba, Sadakazu Shindo of Mitsubishi, and Akisada Ogama of Matsushita will be the first chairman and vice chairmen, respectively. No single cooperative facility will be set up. **-Charles Cohen**



HERE'S EVERYTHING YOU NEED FOR HIGH-PERFORMANCE RECORDING. EVERYTHING.

Pick up the Visicorder Model 1858 and you have a complete system—up to 18 channels including signal conditioning—in a package less than nine inches high. Since it's self-contained, you simply plug in the power cord, connect your signal input cables and start recording. There are no separate cases to mount; no interconnect cables to hook up; and no powders, inks, chemicals or heaters to fool with.

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Whether you record in the lab or field, the Model 1858 quickly adapts to your changing requirements. Wide changes of input levels for different recording applications are easily accommodated, often with a mere change of the sensitivity setting on the front panel. Even a complete change of type of measurements is just a matter of inserting different plug-in modules in the appropriate channels. And you have a complete family of these signal conditioning modules to choose from, for strain gages, thermocouples, flowmeters, tachometers or voltage sources.

For detailed information on how the Model 1858 might meet your recording needs, call Lloyd Moyer at (303) 771-4700. Or write for technical data sheets on the Model 1858 and our illustrated brochure that describes all of Honeywell's oscillographic recorders, magnetic tape systems and signal conditioning modules. Honeywell Test Instruments Division, Box 5227, Denver, CO 80217.

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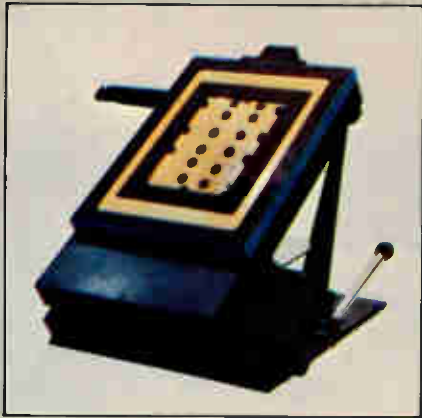
The Thinline® System. Nearest thing yet to universal fixturing.

Matching the test fixture to the PCB and the test system was often time-consuming and costly. Until the Thinline Vacuum Fixture System. With the Thinline System, you can finally achieve flexibility at the interface end of your test system. It's the first fixture system to approach universality.

The basic Thinline Vacuum Fixture System design solves several basic fixture problems. Storage, for example. The Thinline Product Access Unit (PAU) is only 3 inches deep so you can have compact, "bookshelf" storage. And it's made of precision-molded fiberglass and aluminum components for light weight and easy handling.

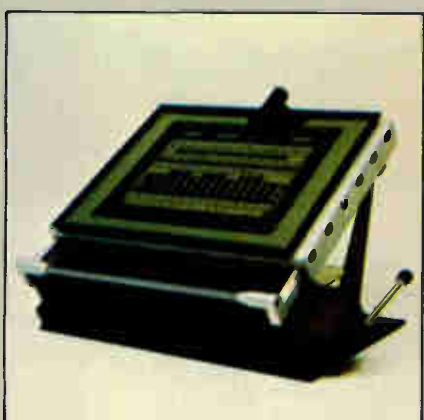
The PAU is designed for easy access to interface contact probes. Probing to any contact point during test program verification and maintenance can be done while the PCB is in the vacuum-actuated position.

The Thinline Probe Receiver is designed for easy loading, precise fixture alignment and positive locking. The receiver will accommodate more than 2800 points and it can be easily adapted for use with test systems fitted with Virginia Panel or other test system interfaces.



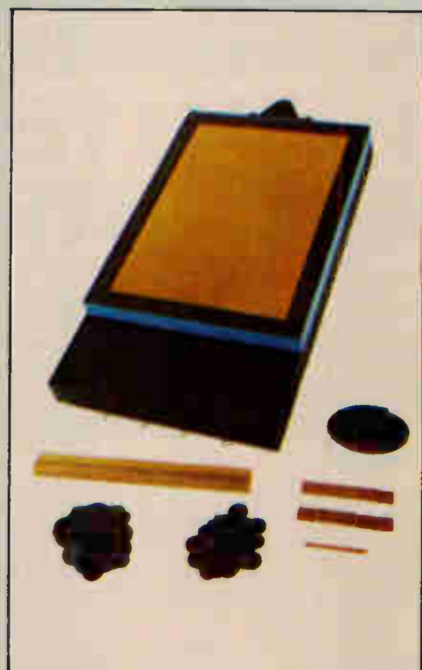
FAST TURNAROUND WITH THINLINE FIXTURE KITS.

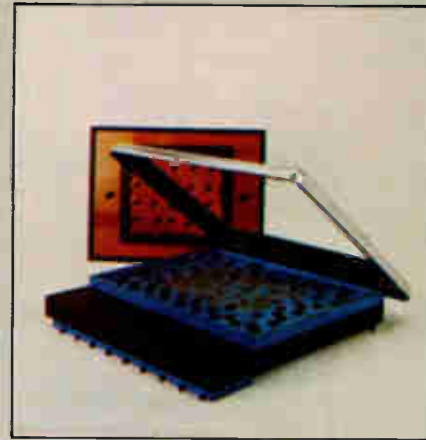
With the Thinline Fixture Kit, you buy a completely assembled unit and do the probe location drilling in your own shop, using the PCB mylar as a master for probe placement or by using the PCB as a drilling guide. All drilling can be done on a standard press or mill. When drilling is completed, point sets and wire wrap posts are easily inserted and wired. You build each fixture as you need it with shorter turnaround time and lower cost.



THINLINE UNIVERSAL CARD PERSONALIZER SYSTEM.

The Card Personalizer System modifies the PAU component of the Thinline System to permit testing of a variety of PCBs with a high percentage of common components on a single basic fixture. Each Personalizer Card is partially drilled to accept all of the probes in a predetermined fixed pattern. Holes are then drilled through at each point where a specific PCB requires access to the test system. The Card Personalizer is an effective, economical method for handling families of very similar PCBs when the total number of test points required for all boards does not exceed available points in the test system.





THINLINE UNIVERSAL WIRED PERSONALIZER EXPANDS THE SYSTEM.

By adding a Matrix Platen to the basic Thinline PAU and modifying the contact panel interface, the Universal Wired Personalizer makes it possible to test extremely large families of bare boards and loaded PCBs with *up to 65% reduction in normal fixturing costs.* It's the nearest thing yet to universal fixturing, making it possible to easily and economically interface with as many as 30,000 test points. The system utilizes a full matrix of spring probes with activation of only those probes required for testing each specific PCB accomplished through an interchangeable wired personalizer.

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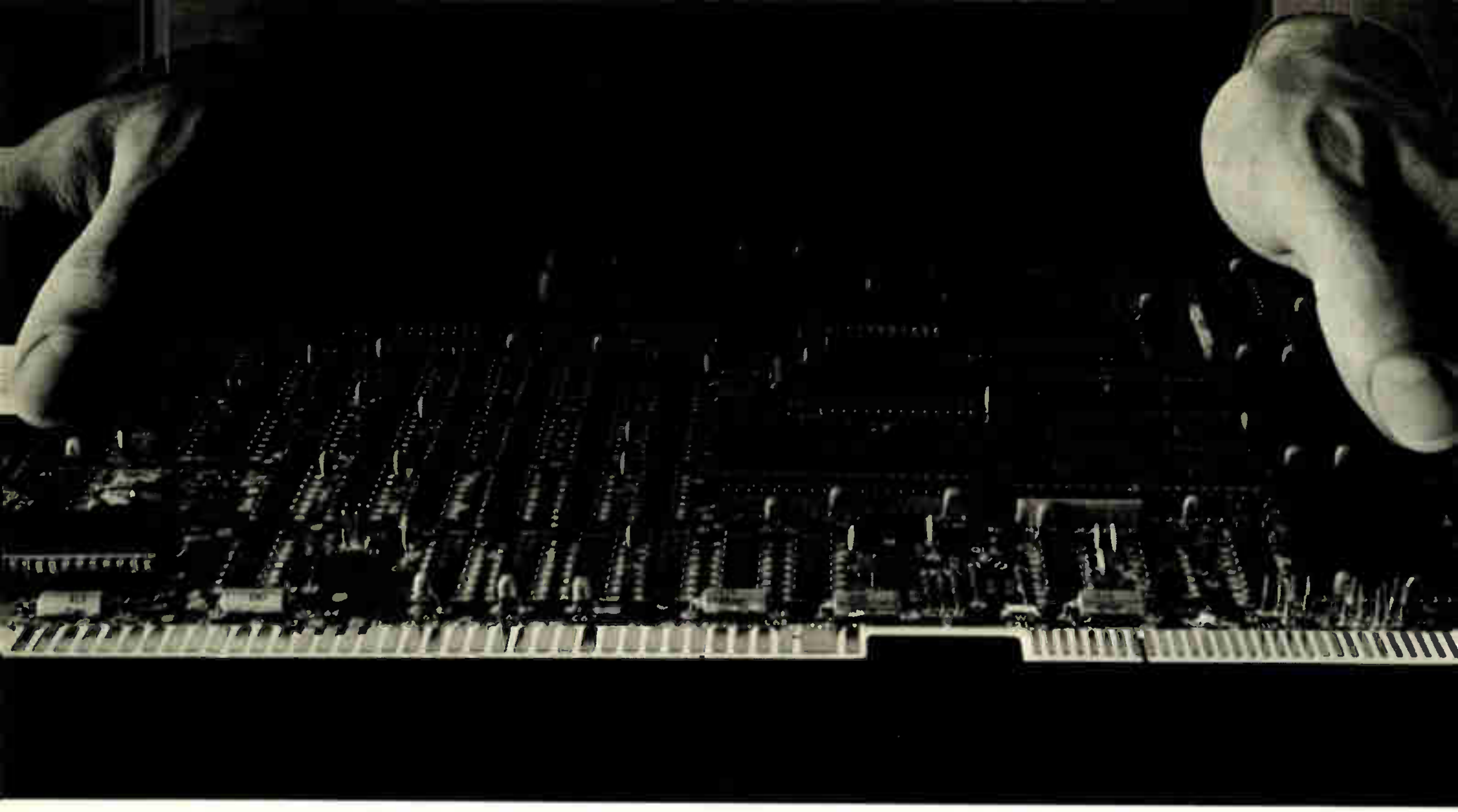

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Teradyne's L135 LSI Board Test System is designed to emulate full operation during board testing. Consider the advantages.

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Errors encountered testing a single board are far more easily located and corrected. Localizing problems during final product testing can take hours.

During board test, the L135's automatic diagnosis capability finds faults at speed. Faults that would take hours to locate manually following a full system test.

What's more, thoroughly qualifying all LSI boards individually greatly enhances final product quality. System test yields climb, as do profits.

EMULATING SYSTEM ENVIRONMENT.

First, you have to duplicate system speed, and the L135 does. Its 5-MHz test rate is equal to most of today's microprocessors.

Precise edge control is essential, as well. The L135 offers up to five edge delays programmable in one nanosecond increments.

In other words, the L135 has what it takes to board test LSI as if it were a system test. So you can locate and correct problems with the kind of speed that really boosts yields.

It all adds up to productivity which, with Teradyne's L135, is the bottom line.

For more information on these and other L135 features, contact your local Teradyne Sales Office. Or call Teradyne Boston, (617) 482-2700.

PRODUCTIVITY IS THE BOTTOM LINE.

Circle 80 on reader service card

TERADYNE

New security planned for data

Public-key systems are being devised for data-transmission encryption-decryption codes that are virtually impossible to break

by Harvey J. Hindin, Communications & Microwave Editor

In establishing the data encryption standard for use in distributed computing and communications systems, the National Bureau of Standards went a long way toward eliminating the triple threat to data security—electronic crime, sabotage, and invasion of privacy. The DES is an algorithm implemented either by hardware using recently introduced integrated circuits or by software.

DES has had problems from its beginnings [*Electronics*, June 21, 1979, p. 107]. Though it has been adopted, users wonder if and when it will be possible for data thieves to break a DES code. And, because the same combination scrambling key is used by both message sender and receiver, chances have increased for both key-security and transmission-security problems. Protecting the key is as great a concern as protecting the message.

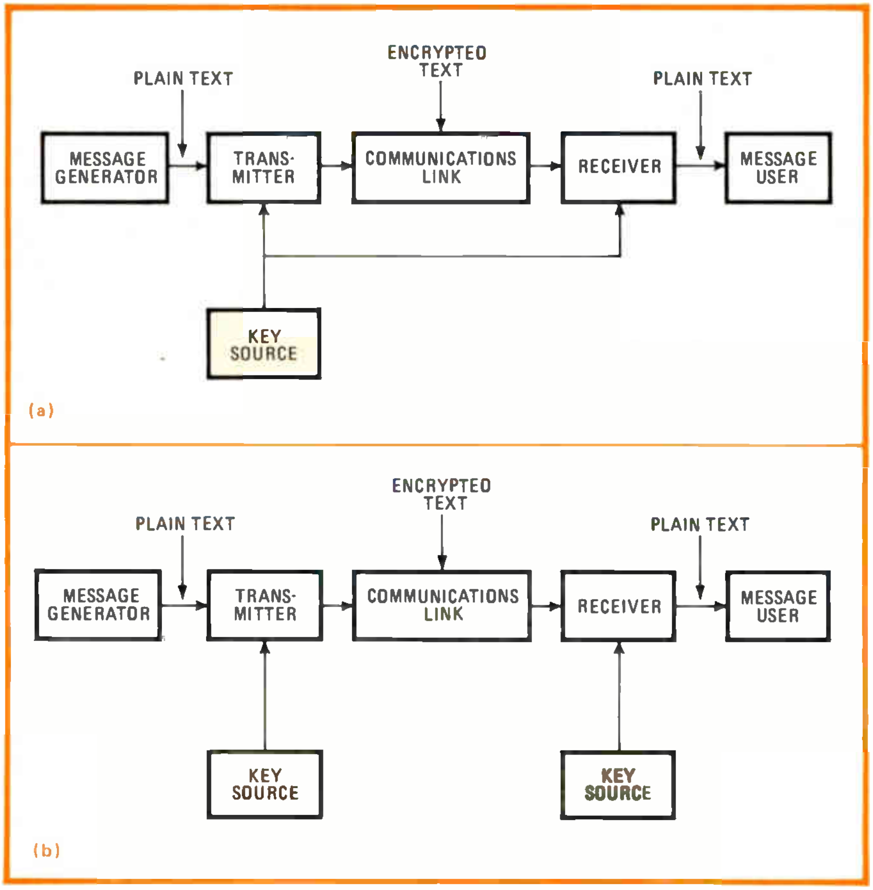
While the DES is the only encryption show in town now, most experts agree that it will ultimately be replaced by more sophisticated systems. "The DES will serve its purpose for at least five years," comments Whitfield Diffie, staff researcher for Bell Northern Research Inc. in Palo Alto, Calif., "but will have to be replaced as public-key systems become practical."

Unlike the DES, which uses the same algorithm for both encryption and decryption, a public-key coding scheme uses different ones for the two operations (see illustration). This is a major advantage in security as the sender is ignorant of the decryption code. "Knowledge of the encoding algorithm does not imply knowledge of the decoding algorithm," explains Stanford University encryption expert Martin Hellman, who, with Diffie, did some of the original work on the system.

Mates. In the public-key system, each encryption key has a decryption key mate. It is impractical to get the decryption key from a knowledge of the encryption key, and it is virtually impossible to decode a message without the decryption key.

With the public-key system, secure communication is possible even over a tapped line. A receiver publishes the encryption key in a directory. A sender can reach that receiver by looking up the public encryption key number in the published directory that gives the system its name. However, the receiver does not reveal the decryption key, which is the basis for message security.

While the public-key system has its appeal, some problems need to be solved before it can become widely used. For one, there is no standard public-key system, but several differ-



Scrambling codes. With the DES, keys are known by both sender and receiver (a). But with the public key system (b), only the receiver knows the decryption key.

ing versions from various sources.

Because there is no standard, there are no IC chips yet available to handle the coding and decoding or to generate the encryption and decryption keys, so for the moment the system can go nowhere.

Finally, there is the cost and trouble of converting from DES to a public-key system. Once users have the DES system in place, they will not be happy about switching to another system unless the economic tradeoffs are favorable.

Making it work. The public-key system is based on number theory—the study of the properties of integers. The encryption-decryption mates are established by using integers to make the decryption algorithm practically unobtainable from the encryption algorithm.

Perhaps the best-known method of generating the mates is the system devised by researcher Ronald Rivest and his associates at the Massachusetts Institute of Technology in Cambridge, Mass. The Rivest scheme depends on the properties of large prime numbers.

To use the system, it is necessary to generate two large prime numbers and multiply them to establish the encryption key. Given the resulting very large number, it is almost impossible to factor it to find out what initial numbers give the multiplied result. Therefore, the factors of the product of the original prime numbers are used to generate the decryption-key code. The security of the system depends on the fact that going one way with prime numbers—multiplying—is easy, but backtracking—factoring—is extremely difficult.

According to Hellman, if each of the original factors is 100 digits long, the multiplication can be done in a fraction of a second by computer. But factoring could take "a million years or so with the best-known algorithm using a 1-microsecond instruction time."

Several other public-key systems are being studied by Shyue-Ching Lu and Lin-Nan Lee of Comsat Laboratories in Bethesda, Md. They are geared to high data-rate communications systems and, according to the developers, "are simple to implement" electronically. Since Comsat is interested in encryption of transmissions from geostationary communications satellites to multiple network destinations, fast encoding and decoding of data are critical.

Another public-key coding system has been proposed by Robert McEliece of the University of Illinois in Urbana. It is based on the properties of certain error-correcting codes, but is said to be more difficult to implement than the Comsat systems. Other public-key systems in addition to these are still untested.

The major concerns in testing these new systems, in addition to security, are ease of implementation of the algorithms and their related computing times. This procedure will take some time, but meanwhile the potential impact of public-key coding will bring on another burst of encryption activity. The system will mean new encryption-decryption integrated circuits and certainly the need for new software. It will also mean another round of intense standards efforts as the data-communications industry seeks increasingly greater transmission security.

Already the education and public information aspects of the field are in full swing. Interest in the DES and public-key systems has particularly stimulated the lecture and seminar industry, with major figures lending their names to one or more organizations that offer to teach those interested—for a suitable fee—everything there is to know about the subject in one to three days.

Code experts and industry consultants are busy as well. Strategic Business Services of San Jose, Calif., and International Resource Development Inc. of New Canaan, Conn., have already prepared expensive reports on the DES. And it is said that consultants will soon prepare such reports on public-key systems, keeping up the educational pace. □

Communications systems that don't cheat

The security of public-key systems makes them particularly useful in specialized applications. A perfect example is the concept of "read-only communications," which could be used in surveillance of the parties agreeing to a nuclear test ban to determine compliance.

In this situation, seismic detectors relay test data to participating nations. But each party wants to be sure that the host country cannot tamper with the transmitted data. The host country, meanwhile, wants to be sure the detectors are sending only seismic readings and not spying.

How can this be done? The detector devices themselves can be made tamperproof. However, the transmission must be protected from surreptitious insertions of data that would give false readings. The obvious solution—encryption—will not work because the host could not be sure that espionage data other than the seismic information was not being transmitted. And, monitoring the transmission by the host does not help since it is impossible to read the encrypted data.

Letting the host country record the data and then periodically review the decryption key to determine (after the fact) that the transmissions were legitimate is not considered to be acceptable among those in military intelligence. Such an approach generally creates key management problems, in any case.

But there is a way out without enlisting the likes of James Bond. A so-called double public-key system is the solution. In this approach, the country to receive the transmission from the host generates a mated pair of encryption and decryption keys.

The decryption key—in this case the public key—is given to the host. At the same time the encryption key inside the host's seismic detector is used to encrypt its data.

Both parties have the decoding key and can monitor the transmitted signals. However, the host does not have the encoding key, cannot get it from the decoding key, and cannot tamper with the transmission.

So the host, in essence, can read the encrypted transmission but cannot write it. Both parties to the treaty are happy with the knowledge that their interests are being protected.

Consumer

Turning TV sets into terminals

Big Berlin show provides a stage for new television services with which European companies hope to lure consumers

by John Gosch, Frankfurt bureau manager

The International Radio and television Exhibition held biennially in West Germany is a big, noisy affair, but behind the hoopla the show provides an excellent opportunity to spot the hot consumer products coming onto the European market. This year's gathering of 525 exhibitors from Aug. 24 to Sept. 2 in West Berlin is no exception.

Sharp-eyed visitors among the 600,000 people expected to wander the 20 acres of floor space will discern one major trend gaining momentum: the television set is quietly undergoing a metamorphosis into a home terminal. No longer a device waiting to be switched on to air a transmitted program, the set is turning more and more into an alphanumeric information display, a playmate in video games, and a screen for taped programs made by the viewer with a TV camera.

Accordingly, the emphasis at Berlin this year will be on information systems like Britain's Prestel, France's Antiope, and West Germany's Bildschirmtext. Also to be highlighted are two-way broadband communications systems. Coming in for particular attention will be the video cassette recorder, one of the hottest competitive items at the show. Then there will be a good number of new video games, home computers, and video cameras—all using the TV screen as a display terminal.

VCR battle. To put themselves in a better position to do battle with the Japanese VCR companies in Europe, NV Philips Gloeilampenfabrieken and Grundig AG have jointly developed a recorder system using a reversible cassette whose half-inch tape provides up to four hours of playing time on each side, giving a total of eight hours. Both companies will unveil the first models of their so-called Video 2000 system at the Berlin show—so-called because actually the consumer Electronics division of Philips calls its model the VR2020 and Grundig has named its version Video 2×4 (see photo).

Showmanship. At the Berlin exhibit, Grundig AG will show its new Video 2×4 VCR. Grundig and Philips have introduced compatible VCR systems to counter Japanese competition.

Meeting the Far Eastern competition in video recorders will be hard. Not only do Philips and Grundig have to put up with direct entry of Japanese firms, they also must contend with a half dozen or so European companies that have opted to sell either Sony's Betamax or Matsushita's Video Home System originally developed by Victor Co. of Japan. But Philips and Grundig, which together have a 50% share of Western Europe's color TV market of some 9 million units, are hopeful they can lure other European firms into the Video 2000 camp to counter these Japanese moves.

Compatibility. To achieve this goal, they are banking heavily on one of the system's major advantages: compatibility. This makes it possible to use the same cassettes on either Grundig or Philips models—and eventually on Video 2000 models that other European firms may choose to build. Other features that should appeal to potential Video 2000 buyers are the system's tape economy and modularity. "The system's modular construction," says Roland Klink, head of product management in Grundig's video group, "makes it possible to build models that can handle different color-TV and line-frequency standards and different kinds of tape, as well as the stereophonic TV that

some producers are working on."

While the market for video cassette recorders is developing fast, that for new media and information systems is still in the embryonic stage. Britain was the first country to go into operational service with television-based information services such as Teletext and Viewdata. And though British component and set manufacturers have poured huge sums into the technology, the hoped-for boom in these systems has yet to start. In 1978 sales of Teletext sets in the UK were a mere 10,000 units and, predicts Nigel Schofield, a market analyst for Thorn Consumer Electronics Ltd., they will be around the 25,000 mark in 1979.

In West Germany, commercial sales have not even started. But the Berlin show will provide a preview. During the event, the country's First Television Network will stage nationwide broadcasts of a Videotext magazine encompassing 75 pages transmitted during the blanking interval produced after each TV frame. Early next year German broadcasters will begin large-scale trials in Videotext transmissions.

Also to be demonstrated will be West Germany's Bildschirmtext, a system based on Britain's Viewdata system. In this Post Office-run service, the user-requested information comes from a central computer and is fed over telephone lines to the viewer's screen. Beginning early next year, large-scale field trials with 7,000 subscribers participating will be staged in Düsseldorf and West Berlin. Since the market is international, Britain and France, too, will be demonstrating their new information systems at the Berlin show.

Gamesmanship. Other equipment that should capture attention are video games and learning systems. One system is the G7000 from Philips. In addition to game cassettes, it includes a cassette that the Dutch company terms an introduction to computer programming. The cassette has a data and program memory and a supply of 29 basic commands. The Philips system allows alphanumeric and control characters to be entered over a keyboard that is part of the equipment. The output is displayed on the screen.

Berlin showgoers will find a somewhat similar system on Grundig's stands. The microprocessor-controlled "Super Play Computer 4000" consists basically of control consoles that connect into a slot on the front panel of the company's top-of-the-line 26-inch color sets. With a view to the future, Grundig engineers designed these sets to accommodate also text information systems such as Videotext. Among the cassettes available for the Super Play Computer 4000 system are a number containing mathematics-learning programs.

Not to be outdone by their Japanese competitors, both Grundig and Philips will bring to Berlin color cameras for consumer use. The German company will present its FAC1800, a compact single-tube color camera with an electronic viewfinder. Suitable for hookup to either a video recorder or a color TV set with appropriate inputs, the camera has a 6× zoom lens with focal lengths of 17 to 102 millimeters. The 2.5-kilogram device has a built-in highly sensitive microphone for sound recording.

The Philips unit, the V200, uses three vidicon tubes that the company says provide the same color quality as those in professional TV cameras. The unit has automatic color correction as well as brightness and convergence control. The V200 sells for less than $1,500.

For all the emphasis on systems and devices that fit on the television set, the Berlin exhibition will not lack advances in receiver design. The microprocessor continues its penetration into TV receivers as a means of tuning and picture control.

Furthermore, big strides are also being taken in chassis design with a view toward reducing energy consumption. Blaupunkt-Werke GmbH, an affiliate of West Germany's Robert Bosch Group, will present a color TV receiver with a 26-inch, 110° display tube that consumes less than 100 watts—a big improvement over the 350 to 380 W sets demanded in the past. Blaupunkt's 20-in. sets consume only 70 W, not much more than the energy burned by a medium-power light bulb. □

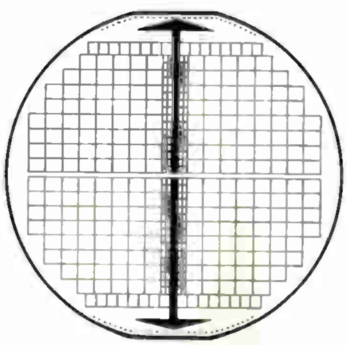
Memories

Wafers to challenge disks, bubbles?

Long in the lab, wafer-scale integration may now be ready to provide megabit memories that are superfast and nonvolatile

by James B. Brinton, Boston bureau manager

Despite work going on since the late 1960s in the U.S. and abroad, wafer-scale integration—that is, integration over the face of an unbroken wafer—has never made it out of the lab. However, the pieces seem to be coming together at the McDonnell Douglas Astronautics Co., Huntington Beach, Calif., a subsidiary of McDonnell Douglas Corp.

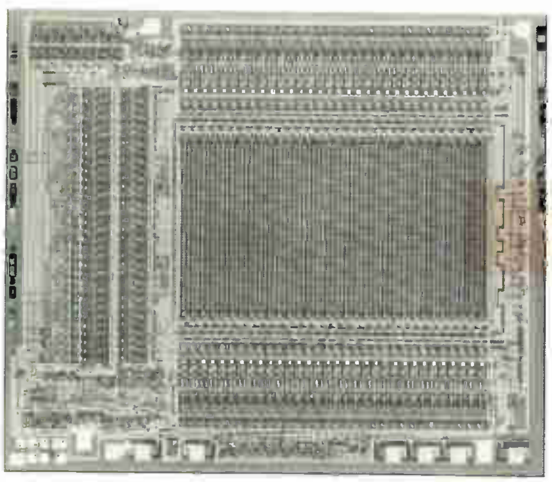


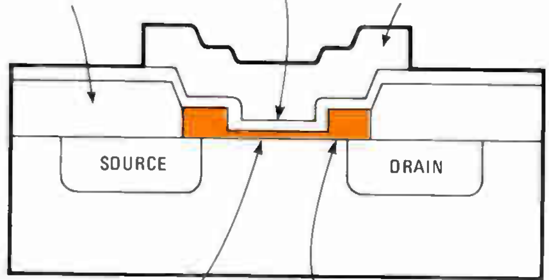
Under direction of microelectronics systems technology branch chief Yokun Hsia, a group of researchers aims to make WSI a production reality by the mid-1980s. The group has already designed experimental versions of near-megabit memory systems on single 4-inch wafers using an adaptive interconnection approach that not only could make WSI practical, but that also holds promise for very high-speed integration and adaptive multiprocessor computer architectures.

According to Hsia, WSI has been slowed because semiconductor and systems engineers have been working separately. McDonnell's WSI work began that way in the early 1970s with low-level work at its Actron division in Monrovia, Calif. Hsia's group added systems-engineering insight to that effort and has built a program now worth more than $1 million of McDonnell's yearly internal research and development funds.

McDonnell's 7½ years of effort have generated what Hsia calls "a systems approach to WSI," an adaptive interconnection scheme that makes possible a "system on silicon." The adaptive concept, called AWSI, includes features like error detection and correction in memory applications, plus fault diagnosis and self-repair through reconfiguration of the buses connecting memory or processor arrays.

Though Hsia's group has built only memories so far, that is "mostly because we are interested in the





Megabit memory system. The 4-in. wafer above would hold 250-plus MNOS memory arrays like the one shown. Each data bit is stored in a silicon-nitride field-effect transistor like that at right. System self-tests, can reconfigure itself to compensate for failed memory arrays.

interconnection system." For the early 1980s, Hsia sees wafers containing many microprocessors, arrays that could be arranged in real time to fit the computing task at hand. He feels that adaptive multiprocessor systems are a logical outgrowth of AWSI. These multiprocessors would have great speed potential because of the number of processors working in parallel and because of the short propagation delays between elements in an "on-wafer" system. This potential seems promising for the military's very high-speed integrated-circuit (VHSIC) program, even though McDonnell is not now part of any VHSIC team [*Electronics*, March 15, p. 41].

Bulky. Early commercial AWSI wafers would probably be targeted at "solid-state-disk" applications. AWSI's metal-nitride-oxide-semiconductor (MNOS) storage would be at least 10 times faster than magnetic bubbles, Hsia claims, and—like bubbles—could be multiplexed for higher data rates. "We have a megabit per second now," he reports, "and expect 2 megabits." Multiplexing could increase either of these figures by a factor of 10 or more.

Also, compared with disks with latency times of up to 10 milliseconds, AWSI latency time would be almost nil. Since data stored in an AWSI bulk store would be mapped, the wafer's controller would access only the desired file.

Problems and solutions. Much of Hsia's work has been aimed at solving problems like heat dissipation, radiation resistance, reliability, and testing, not to mention reducing cost. These problems were tackled with a combination of MNOS and adaptive interconnection.

On an AWSI megabit wafer, for example, storage would be divided among hundreds of 144-by-164-mil (or smaller) 4,096-bit MNOS arrays (see figure). MNOS is nonvolatile and therefore needs power only during a read or write cycle. Since one of these MNOS arrays uses only 200 to 300 milliwatts at most during read or write, the power consumption of a 1-megabit AWSI memory can average 2 to 2.5 W or less. This figure translates into the sort of heat a 4- or 5-in. wafer can dissipate easily.

On average, Hsia adds, MNOS uses about a tenth as much energy as the MOS approaches, but is compatible with almost all of them. MNOS also is resistant to ionizing radiation, a factor in military applications.

High reliability. Hsia figures that AWSI should be very reliable. The key is its organization: the use of adaptive, alterable interconnections and spare memory arrays or processor sites. Thus, in an AWSI bulk memory, a flawed memory array can be replaced with a spare so quickly that the user will notice nothing.

Hsia compares a dual redundant store using two stacks of 4-K memory arrays with an AWSI system using one 16-array stack plus either two or four spare 4-K arrays. With two spares, the AWSI system delivers a mean time between failures of more than 38,460 hours versus the dual redundant system's 5,000 hours. With four spares, it achieves an MTBF of almost 44,000 hours. □

Computers

Plugging along in IBM's shadow

Vendors of IBM-compatible computers and peripherals have survived market upset in the past—can they do it now?

by Anthony Durniak, Computers & Peripherals Editor

The market for IBM and IBM-compatible computers and peripherals is in a state of confusion. Dazzled by the introduction of dramatic new hardware and software technology in IBM's 4300 computers [*Electronics*, Feb. 15, p. 85] and expecting more dazzle early next year, customers are hesitating to place orders for current models and in some cases are canceling orders or are leasing.

Second-quarter financial reports released in the last month by Amdahl, Memorex, Cambridge Memories, and Itel tell the tale. All reported earnings adversely affected by the instability of the market. Even the industry giant is experiencing postnatal depression—IBM said last month that its second-quarter earnings were down (3.4%) compared with those of the same quarter last year, the first time that has happened in 17 quarters.

Getting together. Consolidation of the industry may be in the wind. Earlier this month the IBM-compatible computer maker Amdahl Corp., Sunnyvale, Calif., and the plug-compatible peripherals manufacturer Memorex Corp., Santa Clara, Calif. announced they were holding merger discussions—a possible portent of the future of the business, say observers.

"The industry is aiming more towards the systems," comments William Becklean, Boston-based computer industry analyst for New York's Bache Halsey Stuart Shields Inc. "They can no longer sell just hardware, they must offer a broader range of equipment and have other value-added features such as systems and software support."

Troublemaker? IBM's 4300 computers now being manufactured for fourth-quarter deliveries have turned the market for current equipment topsy-turvy.

Selling computer hardware alone will be most difficult in the 4300 market, some analysts believe, even though the vendors in that market are sure they can match the computer's performance. For instance, most of the 187 instructions recently revealed in IBM 4300 technical manuals were also included in the older System/370 instruction set. Only eight of the 183 Systems/370 instructions were deleted to make room for a dozen new instructions.

Positive thinking. But Robert T. Fertig, vice president of Advanced Computer Techniques Corp., New York, warns that because of its heavy use of microcode IBM can make the 4300 a technical "moving target." Still, that seems not to alarm Joseph L. Hitt, president and chief executive officer of Magnuson Systems Corp., Santa Clara, Calif. "We've been through a stack of IBM documents and don't anticipate any problems. We'll deliver our computers on schedule," he says.

And Jim Geers, marketing vice president at Two Pi Co., Santa Clara, Calif., says the uncertainty at the lower end of the market is starting to subside now that the 4300 deliveries are being scheduled by IBM. The question now is when the turmoil in the high end will end.

Bache's Becklean notes that in the almost 16-year history of the plug-compatibles such market disruptions have always occurred immediately before and after any major IBM product announcement. But generally, he adds, the plug-compatibles vendors have recovered. □

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Technical articles

Peripheral chips shift microprocessor systems into high gear

Support devices, peripheral controllers make short work of functions that microprocessor software toils over, says this special report

by John G. Posa, *Microsystems & Software Editor*

☐ If microprocessors have revolutionized attitudes to computers, peripheral chips are revolutionizing attitudes to microprocessor systems.

Peripheral chips are dedicated hardware that whiz through the chores that the processor would otherwise have to toil through in software. They began as the microprocessor itself began—as a replacement for random logic, an answer to the need to reduce package count, power requirements, and heat dissipation, not to mention design time. But now, especially in high-performance systems, they are being used to distribute processing—to off-load the central processing unit and free it for bigger and better things. While executing a complex operating system and high-level-language application programs, the CPU does not want to be bothered with scanning a keyboard, for example.

Yield economics

Giving added impetus to the trend to make peripheral chips ever more intelligent is yet another factor—the constraints of semiconductor technology itself. There is a limit to the number of active devices it is economically feasible, in terms of yield, to put on a single chip, and today's 16-bit microprocessors are coming uncomfortably close to that limit. Yet somehow they will have to circumvent it if they are to fulfill the chip makers' claims in their recent literature and challenge low-end minicomputers, which at present are used for advanced data and word processing; multitasking, multi-user software development; high-precision scientific processing; distributed networking; and data communications.

The obvious solution is intelligent, programmable peripheral chips. After a burst of commands, the processor can leave them alone and expect to be interrupted only when they have something important to communicate. No longer need a CPU be so bogged down with requests that it has no time to realize its full potential.

In a microprocessor-based system, practically every chip besides the CPU could be considered a peripheral chip, from gate packages to memories. This report will not cover so broad a range. Rather, it will focus on digital, bus-oriented devices that relieve the CPU of time-consuming tasks like timing a cathode-ray-tube display or calculating fast Fourier transforms. And although some data-acquisition and telecommunications components are bus-oriented, these will not be included because their application warrants treatment that is beyond the scope of this report and because they have been covered in other recent special reports on analog-to-digital converters and codecs [*Electronics*, Sept. 14, 1978, p. 105, and May 10, 1979, p. 105].

Still, that leaves seven categories to discuss:

- Bus arbiter chips are being used to circumvent contention in systems where there are a number of intelligent subsystems. One company has designed a microprocessor to further insulate other intelligent devices like peripheral controllers from the system bus.
- Memory-management units are emerging to allocate storage under the advanced operating systems that will ultimately be commonplace. Other peripheral chips, like the 8202 from Intel and the 9915 from Texas Instruments, automatically refresh arrays of dynamic random-access memories (RAM).
- Direct-memory-access (DMA) controllers are address-

ing larger spaces and transferring data at faster paces to and from more places and in many different ways.

- Mathematics and signal-processing peripheral chips will take high-precision calculations out of the CPU's domain. Thus, the processor will be freed from finding floating-point sums, products, and differences, trigonometric values, Fourier transforms, and so forth.
- Dedicated peripheral-equipment controllers are doing more with fewer external parts. Floppy-disk controllers can handle double-density formats and execute not merely single commands but macro-instructions, too. Controllers for Winchesters and other hard disks are beginning to appear. Cathode-ray-tube controllers can display high-resolution alphanumerics and graphics and perform transparent refreshing.
- Data-communications chips are tipping the scales in favor of synchronous data transfer and against the less efficient but also less expensive and less complex asynchronous approach. The devices take care of the electrical interface and avail themselves of numerous bit- and byte-oriented protocols. Accompanying chips encrypt and decrypt the data and check it for errors.
- Finally, various types of universal peripheral controller chips, including general-purpose single-chip microcomputers, are being programmed for a variety of tasks. Often they contain RAM and serial communications logic, making them perfect candidates for processing nodes in a distributed network.

Good business

Nor is there any reason to suppose that this list is final and that peripheral devices will stop proliferating, for their existence benefits their manufacturer at least as much as their user. Besides making the performance of a chip maker's microprocessor family more attractive, they are highly profitable.

"Our major thrust will be in peripherals rather than in CPUs," says J. E. Bass, marketing manager for the MOS microprocessor division of Signetics Corp., Sunnyvale, Calif. "They have a higher average selling price, and that makes good business sense."

"Peripheral chips will continue to be a major part of our business," says Steve Sparks, manager of microcomputer marketing and systems applications for Motorola Inc.'s Integrated Circuits division in Austin, Texas. "We built all these high-performance CPUs, with their powerful instruction sets, fast clocking, and extended addressing, but the key question remains: how does that processor work in the system?" His answer is support chips that interface the CPU to buses, memory, input/output devices, and peripheral equipment.

"You don't want the CPU to wind up being just a peripheral controller," agrees Dave Gellatly, marketing manager for the mid-range product line of Intel Corp., Santa Clara, Calif. "In an intelligent terminal, by the time the CPU has serviced all its peripherals—the CRT, disk, communications line, and perhaps even a printer—it has no time to do the general data processing."

A consensus has evidently emerged. However sparkling a processor's potential may appear, it is just a diamond in the rough, lacking the brilliance it can attain by interfacing with peripheral chips.

PART 1 SYSTEM SUPPORT DEVICES

Support devices include those chips that up system throughput by relieving a CPU of time-consuming tasks like direct-memory-access (DMA) transfers and mathematical calculations. Excluded are those chips that control peripheral equipment like disks and displays.

Clearly devices such as bus arbiters and DMA controllers help organize traffic in systems that are heavy on input and output. But Intel Corp. has gone a step farther; it has dedicated a microprocessor, the 8089, to the task of input and output.

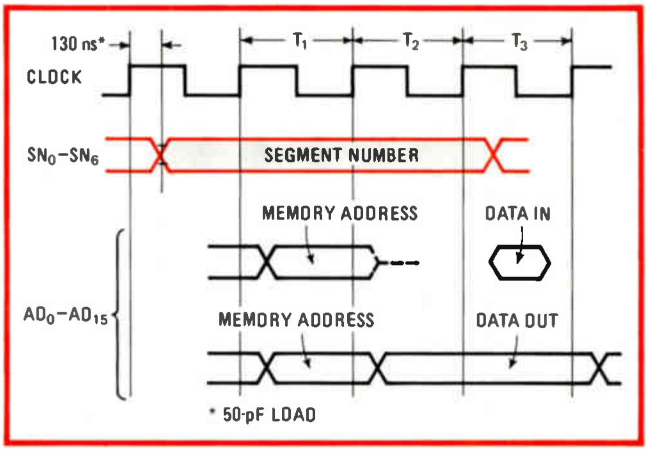
A dedicated CPU

"We're not brilliant," admits Intel's Gellatly, "we looked to the mainframers and found they had solved the problem with an I/O processor. IBM calls it a channel processor, but the 8089 is conceptually the same thing."

Gellatly argues that dedicating a CPU to the job is justified for two reasons. First, it unloads the principal processor. Secondly, the instruction set of a general-purpose processor is not always optimized for this work.

The 8089 is a fully parallel 16-bit machine with its own instruction set, fashioned for I/O control. It uses the same high-performance MOS (H-MOS) technology as the 8086, but the die is slightly larger as it has more devices. The chip incorporates two independent channels, each with its own set of registers. It has a 20-bit-wide arithmetic and logic unit and can address the 8086's full 1 megabyte of address space. The maximum transfer rate of either channel is 1.25 megabytes with a 5-megahertz clock, while maximum latency for a DMA request is 2.4 microseconds.

Intel claims that the I/O processor relieves the CPU by 30% to 80%, depending upon the application. "The 8089 has its own memory that tells it what to do. It never has



1. Lead time. First dedicated support device for memory management was Zilog Corp.'s Z-MMU. Segment numbers and addresses from the Z8000 are joined in this chip. The segment numbers are delivered early, though, to avoid delays through the device.

to tie up the system bus to execute its programs," says Gellatly. For instance, "in a disk controller, the chip can, under its own program control, search a disk for a track, search a track for a sector, find a character in a record, and test its parity without ever using the system bus."

Bus arbiters coming

Intel's 8289 bus arbiter is another new chip that in fact allows the 8089 to be used to full advantage. Because the 8089 can take control of the system bus in its remote mode, it has as much need of an arbiter as the main CPU.

Motorola also plans a bus arbiter for its long-awaited 68000 CPU. "With sophisticated processors and the latest intelligent peripherals, bus arbitration becomes a key feature of high-end microcomputers," says Motorola's Sparks.

Though Motorola's arbiter's ultimate specification has not yet been made final, some of its requirements appear to be concrete. The device sounds conceptually similar to Intel's. "The bus arbitration unit has a priority network, address decoding, and logic for hand-shaking," says Stan Groves, manager of microcomponent applications engineering at Motorola's IC division. "And," he adds, "if you design it properly, you can have multiple local buses talk to one global bus through the device. It is not necessary for all address and data lines to go through the bus arbitration unit—only the control lines."

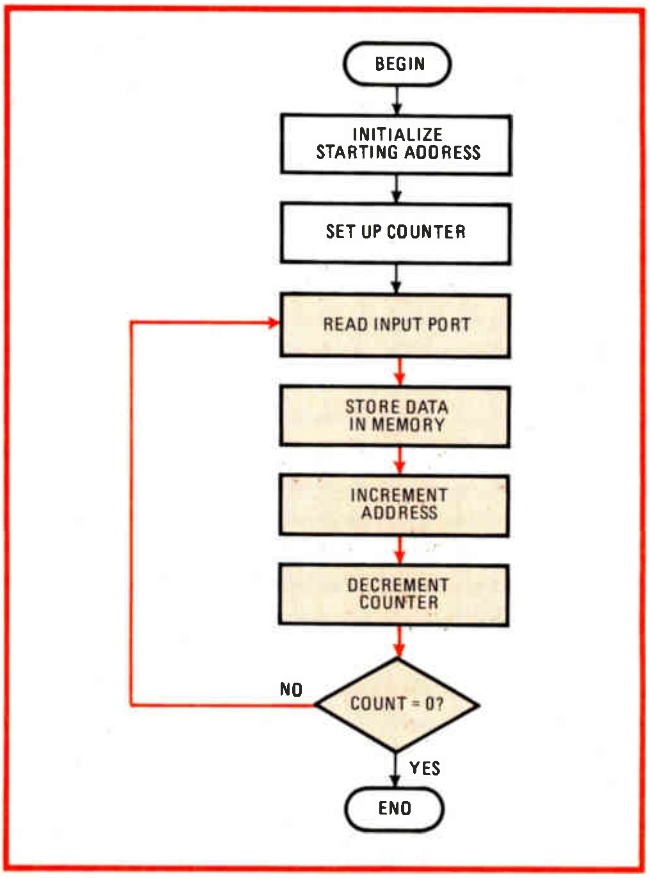
"With such a philosophy, you'd have three-state buffers on each bus and their enable lines would come from the arbiter," adds Sparks, "The enable lines would then control the communication paths. Thus, the chip would be a programmable device that would get loaded with the various priorities, etc. This demands that you have a master at all times to determine which would become next in the hierarchy of control—but it doesn't imply that the master function can't be passed around."

Sparks says that the arbitration chip might be able to control five or six buses, each capable of running independently until system resources are required. However, he also admits that the hardware could get so complicated that nobody could write the software to run it. With multiple buses, for example, "the operating system has to keep the 'hierarchy of mastership' in mind, and that," smiles Sparks, "is the tricky part—to design the hardware that makes those software problems as easy as possible to solve."

Memory management

With the latest 16-bit microcomputers, the range of direct memory addressing has swelled from the 64-kilobyte standard of their 8-bit predecessors up into the millions of bytes. Responsible for this trend is an increased use of high-level languages and their associated operating systems, fatter programs and data bases, and deflated memory costs.

This dramatic increase in available system memory has ushered in the need somehow to manage it. To come to grips with this problem, Intel, Zilog, and Motorola are all making provisions for segmented-memory addressing. Only the last two companies favor separate management chips, however. Intel claims that the degradation in throughput caused by the delay through a peripheral device warrants the inclusion of management and protection hardware within the CPU itself at some later date. National says management and protection deserve a dedicated unit, and may have plans for one for its NS16000 CPU to be revealed later this year. TI also promises what it calls a memory mapper.



2. Software DMA. Anything a CPU can do, a dedicated chip can do better. In this DMA example, the CPU must execute the tinted path each time a byte moves from an I/O port to memory, and with an 8080, this could cost as much as 50 clock cycles.

The most primitive form of memory management is segmented-memory addressing. The first microprocessor to offer it was the 8086 from Intel. With segmentation, a physical memory address is formed by concatenating an offset value with a segment number. At least two potential benefits can be realized with this facility. First, inherently different memory sections, such as those for programs and data, can be disjoined, allowing both complex application programs and system programs like operating systems to be implemented in a more straightforward fashion. Secondly, if the code in a segment refers only to itself, then dynamic relocation is simply a matter of changing the base-address value.

Zilog Inc.'s segmented 48-pin version of its Z8000, as opposed to the 40-pin nonsegmented version [*Electronics*, Dec. 21, 1978, p. 81], looks at its 8 megabytes of memory as a segmented rather than linear arrangement. Its space is divided into 128 relocatable segments, each of which can be 65,536 bytes. The Z8000's 23-bit segmented address comprises a 7-bit segment number and a

16-bit offset address that points to any location relative to the beginning of the selected segment.

However, rather than mesh the segment number and offset value within the CPU itself, the Cupertino, Calif., company chose to design a peripheral memory management unit (MMU). Advanced Micro Devices Inc. in Sunnyvale, Calif., will second-source the MMU along with both Z8000 CPUs and other Zilog peripheral chips [*Electronics,* July 5, p. 39]. The MMU can refer only to 64 segments at one time, so to get all 128, two MMUs must be paralleled. But the MMU also maps 23 bits into 24, so that the segments can be located anywhere in a 16-megabyte space. After a reset or at power-up, addresses pass right through the MMU and into physical memory for initializing the system.

The MMU also protects the segment contents. Each segment has associated with it a characteristic register that specifies its availability; that is, whether the segment is for system or user, to be read or executed, and so on. This register is compared to status lines from the CPU. If a conflict arises, a signal from the MMU, called suppress, acts to stop the operation.

The suppress signal is typically tied into the system's read/write logic and bus drivers. "It comes out fast enough to block write operations," says Joe Kroeger, manager of MOS peripheral applications at AMD, "but it just can't get there soon enough to stop a read operation." Figure 1 shows the relationship between the segment number and the 16-bit address offset for the segmented Z8000.

In the works

Motorola, National, and TI have as yet only plans for memory management units. Motorola's 68000 central processing unit will have two modes of operation: supervisor and user. Its proposed memory management controller will function in the user mode to manage the large address space in a transparent manner. It will be possible for the user to change or update it only when it is in the supervisor mode. The controller is being designed to manage a variable number of variable-size segments as well as handle the relocation and protection of the segments in a dynamic multitasking environment. The 64-pin chip has over 70 instructions and may support several users. Besides translating logical into physical addresses, it regulates accesses to sections for read-only, read or write, program code, and protected data or code.

National Semiconductor Corp., Santa Clara, Calif., may be working on a memory management unit for its 16000 microprocessor. "Memory management is important for those who wish to expand their memory space," comments George Chao, director of microprocessor marketing at National. "In the future, with 32-bit processors, you're going to be seeing a lot of it, and it warrants a separate chip." But he also adds that "the Z8000 and the 8086 have taken the minicomputer method of segmenting memory and it creates a lot of overhead. We're pushing for uniform memory addressing."

Texas Instruments Inc., on the other hand, is working on a chip it is calling a memory mapper. According to Jim Huffines, marketing manager for TI's MOS microprocessors division in Houston, the mapper will allow easy expansion of the 9900's addressing capabilities, but it will not make those users who can get by with 64 kilobytes of memory pay for unnecessary overhead.

Direct-memory access provides a means of transferring blocks of data, typically between a peripheral device and the system memory. The DMA procedure is actually quite simple in nature, and any microprocessor is more than capable of doing it in software by executing a loop like the one shown in Fig. 2. The routine represented by this flow chart fetches bytes from an input port, stores them in sequential memory locations, and decrements a counter. When the counter reaches zero, the transfer is complete and the loop is exited.

The catch is that all those load and store operations take time; an 8080 microprocessor might require as many as 50 clock cycles to transfer each byte. On the other hand, with a DMA controller chip, such transfers can take place in as few as 2 cycles per byte. So for repetitious data movement especially, it makes sense to use such a chip.

DMA techniques

There are several ways to achieve DMA, and the newer devices take advantage of most of them. The two most common methods, though, are called transparent and burst. Transparent transfers are interleaved with normal CPU cycles, hence the reference to their invisibility. But this requires extra logic and cuts DMA throughput at least in half. With burst transfers, the DMA controller takes full control of the system bus, transfers the data at top speed, and typically interrupts the CPU to notify it afterwards. This is not ideal, either, if the CPU is put on hold for a long while. But whenever a chip needs to get at system memory, for whatever length of time, tradeoffs like the preceding two must be made.

The 6102 from Intersil Inc., Cupertino, Calif., is interesting in that it provides for more than just DMA. A complementary-MOS device, it is meant to work with the company's 12-bit C-MOS 6100 microprocessor, which emulates the instruction set of Digital Equipment Corp.'s PDP-8/E minicomputer. Besides DMA, the 6102 provides memory extension (up to 32-K 12-bit words), interval timing, and interrupt control. The DMA section transfers data during idle bus periods so its operation is transparent. Word count and current address are under program control, and the chip can be used for dynamic RAM refresh as well.

Intel has two DMA controllers: an older 8257 and a newer higher-performance device called the 8237. (AMD second-sources the latter part and calls it the 9517.) A high-speed version, the 8237-2, works off a 5-MHz clock and will transfer data directly from peripheral to memory (or vice versa) at rates of up to 1.6 megabytes per second. This allows the 8080, the 8085, or the new 8088 microprocessor to be interfaced to fiber-optic links, some hard disks, and IEEE-488 parallel bus.

Intel's 8237, like the 8257, has four independent channels. But it has more modes of operation and it is much faster. The channels can initialize themselves; that is, they can carry out repeated functions like RAM or CRT refresh without needing any CPU intervention. Moreover,

"You can't define products from an ivory tower"

The idea grew out of an investigation into what holes existed in microprocessor systems, and "one was arithmetic," explains Joseph H. Kroeger, manager of MOS peripheral applications at Advanced Micro Devices Inc. in Sunnyvale, Calif. This is how AMD hit on the Am9511 arithmetic processor chip and its follow-on 9512 floating-point processor. But a lot more happened before AMD began shipping devices about 18 months later.

Kroeger's group at AMD is not a profit-and-loss center, but provides applications, technical, customer, and strategic marketing support to product groups that are. "You can't define products from an ivory tower," he says. Another committee, a design group, is also heavily involved with product definitions through formal and informal meetings. "The third group that participates is the customers," he says.

From that first idea, two to four persons each from the application and design groups spent six months in between working on other chips creating a "wish list" of features for the 9511, then honed it into a two-page "black box" specification that they could take to customers. "You can't go to customers naked and cold," Kroeger says. "Each of us has a network of customer contacts whose judgments and confidentiality we trust. We get their immediate reaction and then we let them chew on it for a week." Meanwhile, the design group studies internal configurations to get "a feel for the die size and critical parameters." (The 9511 wound up measuring 241 by 243 mils, AMD's biggest chip thus far).

If customer reactions are favorable, the design and applications groups spend several weeks further defining the product, ultimately making a formal presentation of its economic, marketing, and technological aspects to upper management. Once management approves, the design group begins about six months of intense effort while the applications group simulates the chip's functions on a computer. For instance, the 9511's 16-bit arithmetic and logic unit was simulated.

The applications group then has firmer specifications to show customers. "We're looking for confirming reactions," Kroeger says, "and with this input, we're ready to interact with the design guys again."

One issue was the number of power supplies. "We really wanted a single supply because microprocessors and memories were going that way, but we also wanted a fast part," Kroeger recalls. Eventually they decided to add a +12-V supply in return for twice the speed for the same die size—a necessity in some applications.

Another issue was whether the chip should be microprogrammed or use state machines or random logic. Microprogramming won because it could easily be changed to yield different math functions and algorithms for a different math chip (like the 9512) and it was easier to debug.

Farther into the design cycle, Kroeger's group wrote the part's microcode, instruction set, and software support in parallel with the hardware design by the design group. The instruction set was modified several times to increase speed and save read-only-memory space. Later Kroeger's group prepared the technical documentation and went out some time before the product appeared to notify customers about it. After that, it is just a matter of "getting the product into the customer's hands, answering questions, and providing technical support." **-William F. Arnold**

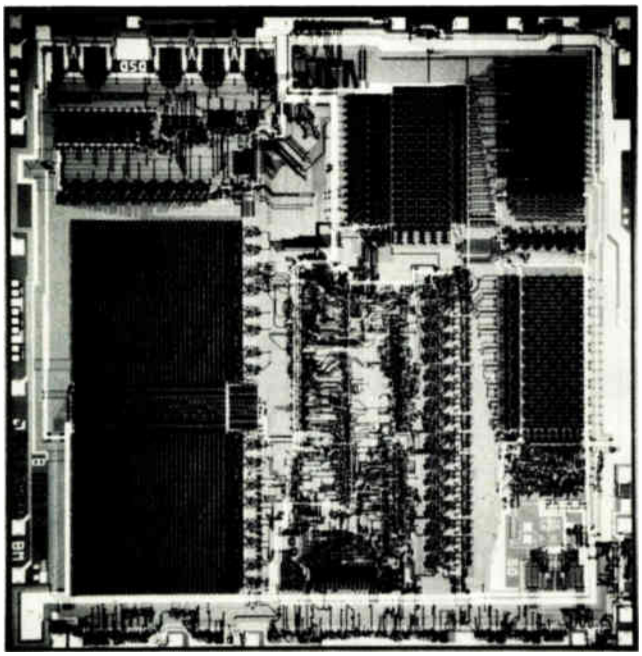
two of the four channels can be used for memory-to-memory transfers.

The 8237 is not a simple chip. AMD's version requires three ion implantations to put 6,350 enhancement- and depletion-mode MOS transistors on a die area of 41,580 mil². AMD is also working on a DMA controller for the Z8000. Like its 9517, the new chip, which will be out the first or second quarter of next year, will have modes other than just simple transparent and burst. It will also transfer data at rates up to 2 megabytes/s and be able to self-load its own control parameters. Thus, after the Z8000 has put the controller's commands in memory, the chip will be capable of unaided functioning for long periods. Indeed, the part will be able to keep going back for the commands and to chain operations together.

According to AMD's Joe Kroeger, the upcoming part is intended for two different operating environments. "The first is called centralized DMA," he says. "In this case, the controller is tied more intimately to the CPU than to any one peripheral in particular. And in this mode it can work on either side of the Z8000's memory-management unit; that is, it can access either logical or physical address locations."

The second alternative is for the DMA controller to be dedicated to a peripheral controller, like that for a disk. "This implies that you have several of the DMA controllers dedicated to the various peripherals," says Kroeger. "The chip transfers data from memory to peripheral, peripheral to memory, and memory to memory in a lot of different ways. And it will absorb bytes and form them into 16-bit words." AMD's DMA controller will be in a 48-pin package because it will be able to access an 8-megabyte source or destination, and that requires a lot of address lines.

Also working on an advanced DMA controller is Motorola for its 68000. In fact, this may be the first support chip to surface for the 16-bit family and may be announced about the same time as AMD's for the Z8000;



3. Math slice. This 9512 floating-point processor from Advanced Micro Devices cannot perform trigonometric calculations, unlike the earlier 9511. But the 9511 does not have the 9512's precision either: 64 bits with facilities for complex rounding.

it will also have some of the same capabilities, like being able to transfer data to and from logical or physical addresses. Motorola's chip will likely be in a bigger package, though, a 64-pin one, to cover the 68000's 16-megabyte addressing range. Besides, it will have four independent channels, each capable of transferring bytes, words, or long words, possibly at rates up to double that of the Z8000-family DMA controller.

Math chips

Any CPU can of course perform multiply and divide operations on numbers of any length—it just takes software time for, say, an 8-bit CPU to find a 32-bit product. If it takes too much time, a math-processor chip can be added. AMD introduced the first math chip for microprocessors, the 9511, over a year ago and recently has introduced another such chip, the 9512 (see Fig. 3). Intel may become an alternate supplier of the 9512 and is also building yet another microprocessor, the 8087, intended solely for arithmetic. And AMI has brought out a signal-processing chip to tackle math and more.

Some people seem to think that AMD's 9512 is simply an enhanced 9511, destined to make the older part obsolete. Actually, the two chips address different markets. The 9511 is oriented toward fast execution at the expense of precision. In contrast, the 9512 is geared toward data-processing environments. Though slower than the 9511, it can handle 64-bit numbers as against the other's 32-bit numbers. Also, the 9512 lacks the 9511's trigonometric capabilities.

However, the 9512 does have the same block diagram and essentially the same die as the 9511. The only circuit modifications were the addition of 3 more bits to all the internal registers and workspaces, enabling the 9512 to do a better job of rounding numbers. Also, to tackle its more complex underflow and overflow rules, the 9512's internal ROM is microprogrammed differently, which left no room for the 9511's sine, cosine, and tangent routines. However, the two devices are virtually pin-compatible, the one difference being that 9512 uses one of the 9511's no-connect pins to indicate that an error has occurred. If an error happened in the 9511, the only way to know was to read its status register.

AMD's 9511 and 9512 have two disadvantages. For one, they are oriented only toward 8-bit microprocessors, and for another, they are built with older technology and require two supply voltages. "What we'd really like to do is use Polyplanar technology to build a 5-volt-only part with a 16-bit data bus and higher speed and performance than the -11 or -12," comments AMD's Joe Kroeger, "but that's probably over two years away." (Polyplanar is AMD's version of H-MOS.)

Before that date, Intel Corp. will have introduced its answer to high-speed number crunching: the 8087 co-processor. This is a peripheral chip only in the sense that it is positioned outside of the CPU. It is a full-blown machine in its own right, with its own instruction set, dedicated to the task of arithmetic. In fact, when coupled with the 8086, the result is really one processing element with enhanced arithmetic capabilities.

Basically an n-MOS part, the 8087 also contains bipolar devices that interface it directly to the system bus. But rather than receive commands from the 8086, which would slow its performance, it monitors the instruction stream as the operation codes fly by, recognizing and executing those commands intended for it. It is a stack-oriented microprocessor, capable of handling multiple-precision (64-bit) floating-point arithmetic and advanced trigonometric functions like hyperbolics.

"If those applications required sophisticated arithmetic instructions, you simply can't build them into the main processor," declares Intel's Gellatly. "This is evidenced by the fact that, to get the job done, it took a processor that is more complex than the 8086 itself." The math chip will be integrated on a very large scale, nudging 100,000 devices. "It would be crazy to put it [and the 8086] all on one chip that's 350 mils on a side—technology simply won't support it," he adds.

. . . and a signal processor

Another ambitous support device is the S2811 signal-processing peripheral (SPP) from American Microsystems Inc., Santa Clara, Calif. At the heart of this high-speed arithmetic processor is a 16-bit adder/subtractor unit that will deliver a 2's complement 16-bit sum in 40 nanoseconds. The SPP also incorporates a parallel modified (Booth's algorithm) multiplier with inputs truncated to 12 bits and an output rounded to 16. A 300-ns (maximum) instruction cycle time is achieved by pipelining the multiplier; through a combination of clocked and static logic, the multiplications are allowed to overlap with read, accumulate, and write operations.

The SPP's high-speed number-crunching capabilities allow it to solve complex digital algorithms in real time. The device therefore has numerous applications in signal processing and telecommunications, including human

"Heavy documentation helps"

The first samples of American Microsystems Inc.'s 2811 signal-processing peripheral chips will reach customers this fall. According to Richard W. Blasco, manager, advanced development and systems, communications product engineering, at the Santa Clara, Calif., company, the parts validate several principles underlying the successful management of a two-and-a-half-year design effort on a complex proprietary device. His advice:

- "Don't put too many people on a project." By keeping the design "as lean as possible," AMI was better able to control costs, he points out, noting that the whole project will come in at a respectable $1.5 million to $2 million. After the basic concept was proposed, Blasco took care of the system design; Kadiri Reddy, the logic and circuit design; and Kenneth Campbell, the layout, backed up at times by four others on the layout team.
- "Put most of the work into the front end to make it easier at the other end." This means heavily documenting everything. Blasco keeps a fat binder full of dated notes explaining what was changed along the way and why. "It gives us control over the chip," he says.
- "Don't be afraid to stop the project, critically review progress, and throw out it all and start over, if need be." Blasco recalls that at one point after the project was more than a year old, "we essentially started again from scratch because we felt that was better than making patches on the existing design. We wanted a good, solid design because it would be with us for a while."
- "Do have the backing of upper management." According to Blasco, AMI president Glenn E. Penisten and the rest of upper management were solidly behind the project from the outset. Their conviction of the importance of the SPP helped to drive the project, he says.

Twice during the design effort, the team stopped for two to two and a half months of intensive review, Blasco says. And the design went through several iterations, some of them major changes, after "a series of concentrated head sessions" during the project, he says. For example, in one brainstorming session early in the project, the design team "was locked away for two weeks" and then decided there were things wrong with the original concept. The SPP was to be controlled by a second part called a peripheral communications controller, Blasco recalls. "The PCC was too powerful, it was more sophisticated than the SPP itself," he says. Consequently, the team put more intelligence on the SPP "so that a low-end microprocessor could run it," tabled the PCC, and took the funds for the PCC for use in developing a hardware emulator for the SPP, Blasco says.

Another major problem was that "the chip kept wanting to get big—250 mils on a side—yet it had to come in at 200 mils on a side." Layout techniques, such as putting the data memory in half the read-only memory, helped keep the die size down to 198 by 205 mils and the transistor count to 30,500, he says. Attention to functional details also was important, such as gating circuitry to detect a −1. "It detects a −1 and corrects for it because in 2's complement arithmetic that result is wrong," Blasco explains. "But you can safely use −1 in the SPP system," he adds.

The team used extensive benchmarking on such functions as DTMF, FFT, and V27 modems to find bottlenecks, Blasco says. A scratchpad memory was added for some algorithms as a result, he notes. Proof of the success of the team's approach to designing the SPP appeared early this year when a model device "played the first time on the simulator," Blasco says. **-William F. Arnold**

speech synthesis and recognition, filtering, finding Fourier and other mathematical transformations, image processing, and radar. The SPP can be viewed as a hardware subroutine module: after commands are given, the CPU is free to perform other operations until the SPP interrupts the microprocessor with results. The SPP's instruction set includes conditional branching and one level of subroutine nesting, and an internal loop counter will count up to 31 program iterations.

Two 4-kilobit memories occupy roughly half of the SPP's 198-by-205-mil² die. One is called the data memory; it has a 8-by-16-bit scratchpad RAM, a 16-by-128-bit RAM with one input and two output ports, and a 16-by-128-bit ROM that holds the user's code. The other 4-K memory is a 256-by-17-bit instruction ROM, on which AMI reserves addresses 250 through 256 to test the device. Another quarter of the chip is consumed by the multiplier and adder/subtractor unit, and the rest is random logic. All of this plus a 20-megahertz clock consumes 1 watt or less and fits into a 28-pin package.

The 2811 mates with the 6800 and 9900 microprocessors, both of which AMI second-sources, and has a serial interface that is completely compatible with AMI's codec chip. It is the first part other than AMI's memories to utilize the company's V-groove MOS processing; but according to Richard Blasco, manager of advanced development at AMI, an alternate supplier could produce the chip using double-polysilicon H-MOS. AMI is currently working on some preprogrammed versions of the SPP to be sold as standard parts, and Blasco and his team are developing a real-time in-circuit emulator, the RTDS2811, that will have a hardware emulator, software assembler, disassembler, and editor for program development and evaluation.

Still the most popular form of mass storage in microprocessor-based systems is the floppy or flexible diskette. Both sides of the disk are now used, and recording density is moving from single- to double-density. Thus, a fourfold increase in disk capacity, from 256 kilobytes to 1 megabyte, has been realized. The IBM 3740 and the IBM System 34 formats serve as *de facto* standards for single- and double-density recording, respectively.

Clearly, the most complex and timely of the floppy-disk controller ICs are those capable of complying with the double-density standard. So far, six such chips have been announced or are in the works (see Table 1). Western Digital Corp. of Newport Beach, Calif., started the race back in mid-1978 with its 1791 chip. Nippon Electric Corp. followed close on its heels with the μPD 765 controller. Both of these parts are available, and second sources have stepped forward. Later this year, Rockwell International Corp. will announce a part, and Texas Instruments will introduce its double-density controller, the 9909. Early next year, Motorola's 6849 and the 7003 from Standard Microsystems Corp., Hauppauge, N. Y., will be available. The possibility also exists that AMD will develop a compatible controller for the 16-bit Z8000.

Floppy-disk controllers are intended to mate a CPU with a drive (Fig. 4). The chips convert parallel data into a serial stream and do the reverse in the opposite direction. For single-density recording, frequency modulation (fm) is used to store a bit as two magnetic flux reversals per cell of disk medium; for double density, modified frequency modulation (mfm), which requires only one flux reversal per cell, is most commonly used. Besides the data conversion, the controller chips are capable of formatting a disk (setting up and remembering the number of bytes per sector) and performing cyclic redundancy checks on the data.

As is the case with CRT controllers, the floppy-disk controller chips can be used with or without direct-memory access. Without DMA, however, once again the CPU is interrupted to transfer data to and from the controller chip. This burden is acute: with single-density recording, it is interrupted roughly every 30 microseconds, and with mfm, about every 15 μs. In most applications, therefore, it pays to install the DMA controller.

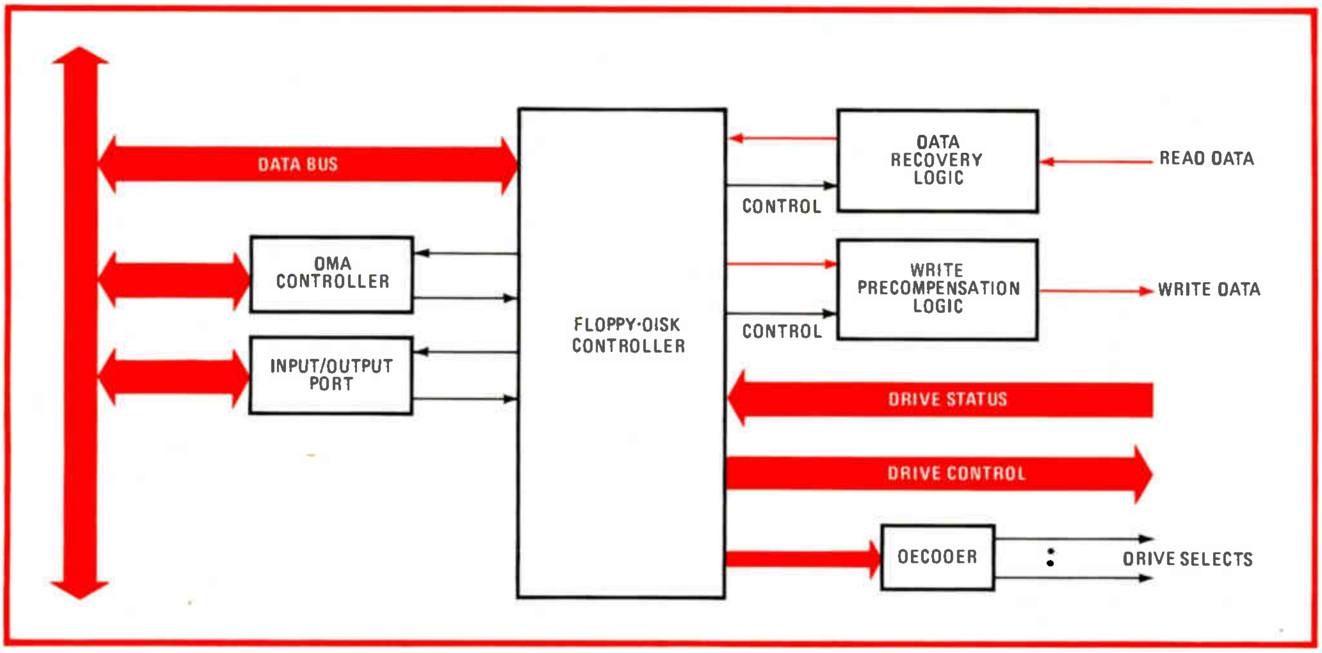
The place of a floppy-disk controller

Figure 4 shows how any floppy-disk controller would be positioned in a system. The differences between the chips lie in how they deal with the external components and the drive itself. The read-recovery logic, for example, might contain a phase-locked loop (PLL) to increase reliability, and NEC's part has handshaking signals that control a PLL directly. These signals are called VCO sync and mfm mode. "They make the interface straightforward," says Richard Weiner, manager of peripheral components at NEC Microcomputers Inc., Wellesley, Mass. "VCO sync tells the PLL when to lock and when to drop out, and mfm mode indicates when the data is

TABLE 1: PROGRAMMABLE DOUBLE-DENSITY FLOPPY-DISK CONTROLLERS

	Motorola 6849	NEC 765	Rockwell 6591	SMC 7003	TI 9909	Western Digital 1791/93
Pins	40 / 48*	40	40	40	40	40
Power supplies	+5	+5	+5	+5	+5	+5, +12
Number of track counters	1	4	2	2	4	1
Compatible DMA controller	6844*	8257	6544	n/a	9911	1883
One-command formatting	yes	no	yes	yes	yes	no
Track 00 restore command	yes	yes	yes	yes	yes	yes
Seek-and-read or -write	yes	yes	yes	yes	yes	no
Address-mark detection	yes	yes	yes	yes	yes	yes
Multiple-sector transfer	yes	yes	yes	yes	yes	yes
Phase-locked-loop control lines	no	yes	yes	no	no	no
Programmable head-load and -unload	yes	yes	yes	yes	yes	no
Multiple head-select lines	no	yes	yes	yes	no	no
Write precompensation	no	no	yes	yes	yes	no
Low write current	yes	yes	yes	yes	yes	yes
User-definable formatting	yes	yes	yes	no	yes	yes
Availability	1Q - 2Q, 1980	now	3Q, 1979	1Q, 1980	4Q, 1979	now
Second source	no	Intel	Synertek	no	no	National, SMC

*48-pin package has on-chip DMA



4. Floppy interface. A microprocessor sits on the bus at the left, and a floppy-disk drive is off to the right, and floppy-disk controllers incorporate as much in-between logic as they can. Some older controllers need all of the external logic shown; newer ones need hardly any.

double-density and when not," he explains.

NEC's part (like TI's) will control up to four disk drives. Weiner explains that this is not as simple as just having four select lines emanating from the device. "You need a track counter inside the chip for each drive, because you have to remember which head is on which drive," he says. The 765 device also has the ability to seek data on different drives simultaneously and to perform multiple sector transfer operations.

Motorola's dual-density controller, to be designated the 6849, will be the first programmable peripheral device the company has introduced on its own. "The chip will completely cover IBM's standard for dual-density formatting and will probably be the most comprehensive dual-density controller on the market," claims Motorola's Stan Groves.

He says it is not easy to format a disk to IBM standards using any device on the market today, whereas "using our chip, a single command will totally format a given track to IBM standards." Also, one particular demand of the IBM doctrine is that the first track be always single-density while all the rest are double-density. "With Western Digital's dual-density floppy-disk controller, a pin must be manipulated to make this change," continues Groves, "whereas ours is totally software-programmable. Control bits from the CPU determine the density and clock rates and also allow the user to device his own formats if he chooses not to incorporate IBM's." The 6849 has an on-chip RAM that stores the user's patterns.

Motorola's device, which will be compatible with a wide range of 8- and 16-bit CPUs, represents a brand-new machine architecture: an internal 16-bit arithmetic and logic unit that executes close to 70 instructions. The chip will ultimately be offered in three versions: two 40-pin packages without and one 48-pin package with direct memory accessing. The 48-pin version will probably be the first introduced, to insure that the concept works on its grandest scale. Then the DMA capabilities will be stripped out to make the 40-pin versions.

TI's 9909 and SMC's 7003 ease the need for the write precompensation logic shown in Fig. 4. This logic is required to adjust the timing of write pulses skewed by magnetic peaking effects. Both devices have the ability to make this time translation internally. TI's part has a pin called half bit-cell clock that can be used to alter the timing, and SMC's part has a control register that can be loaded with offset values. SMC's component also has on-chip data separation logic to further reduce the component count.

The IBM standards apply only to soft-sectored formats. There is another class of disk, termed hard-sectored, that has holes punched in the disk itself to indicate where the sectors are. Although the TI and Motorola controllers make some provisions for this type of drive, SMC designed a chip for them, the FDC3400 hard-sectored data handler. The chip converts parallel into serial data and can be used with up to four single- or double-density diskettes.

Winchester control

Although rumor has it that Western Digital will produce a hard-disk controller chip, evidently Nippon Electric Corp. will beat them to that marketplace. NEC already has samples of such a part, the 3302, and plans to have it available in quantity in the first quarter of 1980. "Basically, the chip will work with most 8- and 14-inch hard-disk drives," says NEC Microcomputers' Weiner, "but it is really geared for Winchesters."

The 3302 will handle data transfer rates up to about 1.3 megabytes per second. But to obtain these rates, the die size had to be bigger than an 8080's and a −2-V substrate bias voltage has to be applied externally. To do this at so quick a pace is so complex that "the chip does

TABLE 2: PROGRAMMABLE CATHODE-RAY-TUBE CONTROLLERS

	Intel 8275	Motorola 6845	National 8350	Signetics PVTC	SMC Solid State Scientific 5027 (TI 9927)	Synertek, Rockwell 6545
Pins	40	40	40	40	40	40
Power supplies	+5 V	+5 V	+5 V	+5 V	+5, −12 V	+5 V
Microprocessor family	8080	6800	n.a.	8048/8049	8080 with interface	6500/6800
Direct memory access required	yes	no	no	no	no	no
Interlaced scan	no	yes	no	yes	yes	yes
Refresh memory addressing	n.a.	binary	binary	binary	row/column	binary and row/column
Light pen	yes	yes	no	yes	no	yes
Cross-compatibility	no	Synertek 6545	no	no	no	Motorola 6845
Memory-contention circuit required	no	yes	yes	no	yes	no
Screen format selection	software	software	mask ROM	software	software external PROM mask ROM	software
Attributes controller	no	no	no	VAC	8002	no

not have as many "smarts" as, say, a floppy-disk controller," says Weiner. "For example, to read data, it can't just go and find the proper sector, read the data, and do all the transfers. Instead, you have to monitor the data coming off the hard disk, decide whether it's the proper sector, and start for transfers. In the case of this chip, there's got to be more interaction between the controller and the CPU," he says, adding that although some hard disks can transfer data at much higher rates, this chip cannot handle it. In fact, he feels a limit to MOS speeds is being approached, and that to comply with those rates probably warrants a bipolar device.

AMD, however, in its burst-error processor (BEP), has found a way to make MOS in effect eight times faster. The device is intended to finger errors in disk-based environments [*Electronics*, July 5, p. 39]. It scrutinizes data moving from memory to the disk, be it flexible or hard, and tacks on extra bits that represent the data. When the data goes the other way, the same calculation is made, and the two results are compared. If they are different, an error in the data exists, and if the bad bits are contiguous, they can be mended.

Through a serial-to-parallel converter, the serial stream is converted into bytes for processing by the BEP. "The tricky part of our device is how we're able to work on 8 bits at a time while everybody else does it 1 bit at a time," says AMD's Joe Kroeger. "We've done something unique that is in the process of being patented." AMD's device is thus able to perform error detection on data rates as high as 20 megabits per second.

CRTs in control

As Table 2 shows, numerous programmable CRT controller chips have been introduced. All of the chips, with the exception of Intel's 8275, have the ability to address the refresh RAM directly. The 8275 instead contains two row buffers; while data is being pulled from one for screen display, the other is being loaded with the next row of characters. Data can be transferred into this buffer-in-waiting by the CPU, or it can be filled by another of the company's DMA controllers. The number of characters transferred and the number of character clocks in between DMA requests (up to 64) are both programmable.

Unlike Intel's 8275, National's DP8350 is a bipolar device, made with integrated injection logic. It may use an on-chip (crystal-controlled) oscillator or be driven with an external clock. Being bipolar, the device is fast enough to display up to 64 rows of 110 characters in a 16-by-16 field. It interfaces directly with up to 4 kilobytes of RAM via 12 three-state address lines.

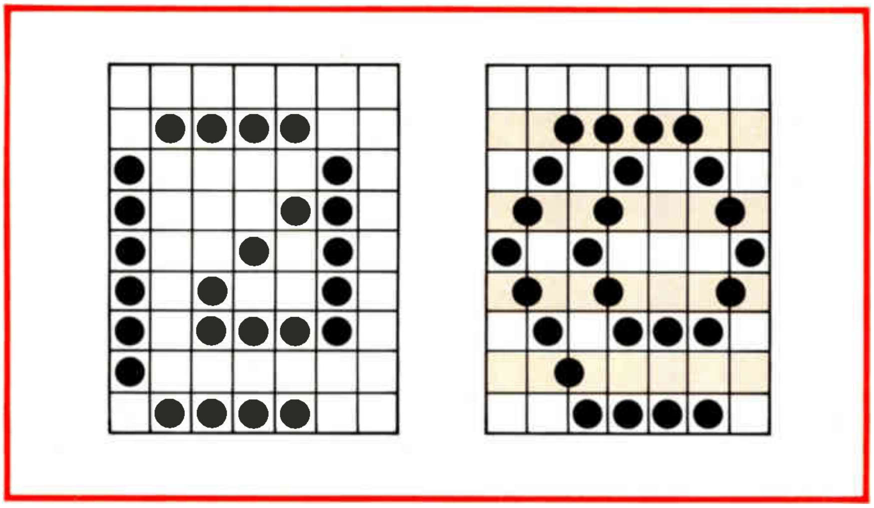
A complex device

Motorola's CRT controller has a 14-bit address bus to access up to 16 kilobytes of refresh memory. Timing can be programmed for a wide variety of screen densities (80 by 24, 72 by 64, or 132 by 20 characters, for example). Also, by using the chip's starting-address register, scrolling by line, page, or character is straightforward. The chip has facilities for interlaced refreshing and transparent (or contention-free) refreshing, although the latter needs external multiplexing hardware.

So complex is the Motorola device, in fact, that one of its second sources, AMI, plans to delete some of its functions in order to reduce its die size and cost. "In many instances, the customer doesn't need to change things like screen format," says George Nelson, AMI's manager of microprocessor product marketing. "So we plan to make them mask-programmable instead because ROM cells are smaller than RAM cells." AMI also plans to abandon the light pen. "Only 5% or 10% of the users really need it," Nelson contends. "Instead of the light-pen strobe, we're going to use the pin for the 50-/60-Hz select. AMI's version of the Motorola design, which should be out by the end of the year, will be called the 68045 and its price could be as low as $5 or $6. "We're shooting for high-volume stuff," smiles Nelson.

The SY6545 from Synertek, Santa Clara, Calif., is pin-compatible with Motorola's chip. However, the 6545 has some extra features to allow transparent refreshing to be set up without much external hardware. It also has even more programmable registers than the Motorola device, and these should not be accessed if the 6545 is used to replace the 6845.

One of the latest CRT controller schemes comes from Signetics. It has partitioned the function between four new integrated circuits: a programmable video timing controller (PVTC), a programmable keyboard and



5. Half-dot shift. Signetics recently introduced a four-chip solution to CRT terminal control. The ICs let a row of video data be displayed shifted by one-half dot. This allows angles other than 45°, as well as more pleasing characters, like the commercial "at," @.

communications controller (PKCC), a display character and graphics generator (DGCC), and a video and attributes controller (VAC).

The PVTC may be programmed for varying display formats, sync generation, and cursor control. The display may have as many as 128 rows of 256 characters, interlaced or noninterlaced, and a light-pen register is provided. The chip has six registers for timing, six for control, and three for status and interrupt conditions.

Unlike the other three chips, the video and attributes controller was designed as a bipolar device so that it would be able to drive a monitor without the need for external packages. It has an on-chip oscillator that can cycle from 3 to 40 MHz. It can produce black or white backgrounds and various cursor and character attributes. One of its most unusual features is its ability to "half-dot–shift" a row of video data. In conjunction with its on-chip character video-shift register and the DCGG's character-generator ROM, the half-dot–shift mechanism allows diagonal lines in characters or graphics to be drawn at angles other than 45° while still having the dots closely spaced. The effect of this on a commercial "at," @, is shown in Fig. 5.

Conflict resolution

Another new CRT controller design comes from Advanced Micro Devices as part of its commitment to the 16-bit Z8000 microprocessor [*Electronics*, July 5, p. 39]. Like Synertek's part, AMD's unit is being designed "to resolve refresh-memory contention problems," according to AMD's Joe Kroeger. AMD's design will circumvent refresh-memory conflicts in two ways. The first is by interleaving CPU and CRT controller accesses during a character time. However, this requires external logic and faster RAM. "But if you use an external line buffer, you can use slower memory and still resolve the contention problem," Kroeger adds.

AMD's 48-pin device, which is still about a year away, will treat the refresh memory like a linked list (see Fig. 6). "There is a control block at the start of each character row that contains the addresses of the data and all of the variable parameters for that row, like superscripts and subscripts. It also holds the address of the control block for the next scan," he explains. "Thus, we independently thread the data and control blocks." In this way, it does not matter where the two blocks are put in memory. They may be together or separate.

The AMD chip will have 14 address lines to access 65,536 locations of varying width. "By the time you get a large character set and quite a few internal and external character attributes, you can easily get to 24-bit words," says Kroeger. The chip will also allow at least four different windows on the screen, each with one or more cursors. And the number of characters per line could be as high as 132 to reproduce a computer printout.

Data communications

Data communications has become an important concern of chip makers. The cost of general-purpose processing is declining, so that functions like data communications are becoming a more dominant factor in total systems costs. Also, as computing power is distributed, the need for efficient data communications has become more acute. As Mark Olson, a peripheral product marketing engineer at Intel, puts it, "As you move the processors to where the problems are, you have to supply a means for them to talk to each other." Finally, the International Standards Organization and the American National Standards Institute have agreed on a seven-level hierarchy for communications protocols, thus giving the semiconductor manufacturers something to work from.

This hierarchy, termed the SC-16 Reference Model, spans the entire gamut from the physical communications line right up to the user's application station [*Electronics*, Dec. 7, 1978, p. 120]. At present, only the first two levels make sense for integration by chip makers. The upper levels are extremely software-intensive and application-dependent, and individual standards are not yet agreed upon.

Level 1, the physical layer, specifies the mechanical, electrical, and functional characteristics of the link and is well embodied in the EIA's RS-232 and RS-422/423 standards, for example. Level 2 controls the flow of data through the link by adding message addresses and providing for error detection and correction. Examples that may be used as illustrations here include control-character protocols such as IBM's BiSync and bit-oriented protocols like IBM's SDLC and the ISO's HDLC.

Level 1 is being addressed by all the asychronous and receiver/transmitter chips that are currently being supplied by just about every semiconductor company. And level 2 functions have been integrated in the form of numerous protocol control chips, also provided by numerous vendors. However, the two sets of devices blanket neither level comprehensively, says Alan Weissberger, formerly a data-communications engineer at Signetics Corp. and now a principal engineer at Memorex Corp. in Cupertino, Calif. Level 1 chips only do the electrical portion, he says, and software often has to be added into the loop monitor to control modem signals, for instance.

Similarly, in level 2, only the framing of the line and occasionally address recognition are accomplished by the protocol chips. "What's not done," comments Weissberger, "is the control procedures required to make sense of the addresses and of the commands and responses embodied in the control field."

Thus, at the present time, data-communications chip makers are hard at work to take up some of the slack that exists, especially in level 2. Some firms, namely Signetics and Western Digital, have disclosed that they will produce frame-control ICs for this purpose. Signetics plans three different versions for asynchronous, BiSync, and HDLC. Western Digital plans a frame controller called the WD2501 for X.25, level 2, which happens to be HDLC. Though others are reluctant to admit their intentions, "everybody's working on it," says Signetics' Everett Cole, marketing manager for data-communications products. "It's the next step."

Chip makers are also expanding horizontally within level 2 by designing multiprotocol chips. Signetics, Standard Microsystems, and Zilog, among others, already have devices that support several protocols, and other companies, like Intel, are said to be working on their own version of an all-protocol device. Such chips are very attractive to the original-equipment manufacturer. "They have to support a number of different line disciplines," says Memorex's Weissberger, "and would like to use a standard module for all of them."

Devices that support bit-oriented protocols almost always have cyclic-redundancy-check logic on chip because that is part of the standards that exist. But for character-controlled protocols like IBM's BiSync, ANSI's 3.28, and DEC's DDCMP, this usually demands extra software, hardware, or both—which may have been what led Signetics to develop its 2653 polynomial generator and checker chip.

The 16-pin n-MOS device can generate and detect block-check characters, as well as recognize specific characters and strings. It is bus-oriented, and full-duplex operation can be accomplished using two of the chips. "The 2653 has a great deal of intelligence," says Signetics' Everett Cole. By the polynomial the user chooses, coupled with parity selection, the part can tell whether EBCDIC or ASCII characters are being used.

Other peripheral chips help make data communications secure. Western Digital, Intel, Texas Instruments [*Electronics*, June 21, p. 107], and Motorola [*Electronics*, July 19, p. 153] have all announced encryption devices that will scramble 8-byte blocks of data in accordance with the National Bureau of Standards' recently adopted data-encryption standard. Typically, the devices are loaded with raw data over the CPU's bus. After they have encrypted a block of data using a 56-bit key, the block is usually read out and transmitted over a serial line.

In data rate, however, devices do differ, ranging from a low with Intel's 8294 of 80 bytes per second to a high of 167 kilobytes per second with Western Digital's WD2001 and 2002. Accounting for this difference is the fact that Intel's part (like TI's) is a preprogrammed single-chip microcomputer. Thus, the algorithm is figured with instructions rather than directly with gates.

Universal slaves

All of the devices discussed thus far could be termed dedicated. Programmable they may be, but they can only be coded to perform a single or limited number of peripheral-control or support functions. However, microprocessors, in particular general-purpose single-chip microcomputers, can also be used as peripheral chips.

A prime example of this is the serial control unit from Mostek Corp., Carrollton, Texas. It is a preprogrammed 3870 designed for use as a slave to be controlled by a master CPU over twisted-pair lines. According to Ron Baldridge, Mostek's strategic marketing manager for MOS microprocessors, it may turn out to be one of his company's "outstanding peripherals."

Zilog's single-chip Z8 also has a serial line, and it can transfer data at a rate of 62.5 kilobits per second. According to Janek Pathak, product manager for component marketing at Zilog, the Z8 may be preprogrammed and offered as other standard components. Indeed, it is scheduled to be a universal peripheral controller (the Z-UPC) for the 16-bit Z8000 microprocessor, though it will require more than just a new program to do the job; there will be slight mask changes.

Zilog is also toying with a Z8 multiply-and-divide subroutine library that would allow a user to select the operations needed. Another possibility is a debug monitor. "The user would down-load a program from an external device over an RS-232 line and be able to examine and change the data memory and register contents and do single-stepping," says Pathak. If there is room, a keyboard and display driver might be included in the package. "We're going to call it a canned-program Z8," Pathak avers.

Similar aims

Motorola has similar intentions for its family of single-chip microcomputers—for the 6809, a floating-point math package that will conform to the IEEE's standard, plus a Basic interpreter that will embody many Pascal constructs. And the 6801 may be programmed as an IEEE-488 bus controller. "We have drawn up specifications for external-clock versions of these parts," says Steve Sparks. "The 6801, for instance, was reconfigured to the point where we're going to call it a 6801 peripheral controller. It's got a dual-port RAM."

Don Phillips, product marketing manager for peripheral products at Intel, offers the firm's 8041A universal peripheral interface as an example of an outstanding

"Categorize the functions"

It was about 16 months ago when a new Mostek Corp. employee, Robert Burckle, got the assignment. The Carrollton, Texas, company was looking for someone to explore and promote advanced multiprocessing-type applications for its MK3870 family of 8-bit single-chip microcomputers, the 29-year old Burckle recalls. And four years of experience in digital communication and system design for his previous employer—Systems Research Labs Inc., Dayton, Ohio—equipped Burckle for the job.

Burckle estimates that initially he was spending a fourth of his time on the project while tending to the rest of his job as an applications engineer. Upon examining the market, he soon noted a lack of microprocessors being used as remote peripherals. They were being used remotely, but most often in a dedicated fashion, requiring software, discrete circuitry design, and what Burckle calls "a lot of duplication of effort." But "you could pretty well categorize the different functions they were being used for," he observes. "So we figured it might be possible to come up with some sort of standard product using the 3870 that could handle a variety of the most popular and needed functions with a single chip.

Thus was born the idea for what Mostek calls the SCU 1 (serial control unit), which the company began supplying in sample form last month. The device is a 3870 with its 2,048 bytes of on-board read-only memory programmed to perform a variety of tasks commonly needed for industrial control, and alarm and security applications [*Electronics*, Dec. 7, 1978, p. 46]. It is designed to work as a remote intelligent peripheral device, commanded by a host central processing unit over serial lines in an asynchronous, half-duplex, polled environment. The SCU provides up to 16 input/output lines for interfacing to devices such as analog-to-digital and d-a converters, switch closures, relays, and the like and is also suited for remote monitoring applications.

As Burckle worked on the project, he consulted regularly with various officials within Mostek's microcomputer group, and by June last year the decision had been made to go ahead with a preprogrammed 3870 product. Following a series of in-house design review meetings and consultations with eight major potential customers for the product, Burckle had by February defined a serial protocol and a set of rough specifications for the proposed SCU.

But at that point, "I realized that working only a quarter time on the project, I wouldn't be able to generate all the code, debug it and do what I considered to be a first-rate job within a reasonable period of time," Burckle relates. As a result, Jeff Owens, a 24-year-old Mostek lab electronics technician who calls himself "really a programmer" (in background of photo), wrote the SCU code on the basis of Burckle's proposed specifications.

Consulting frequently with Burckle, Owens spent the next several months working nearly full time on the SCU code generation and testing. The result was what Owens jokingly refers to as "our first final pass" on the SCU, since additional iterations were still to be done on the basis of customer feedback from samples.

The device was submitted to mask on May 1 this year, says Burckle, with the first working samples produced eight weeks later. Current Mostek plans call for formal SCU 1 introduction at the Wescon show next month.

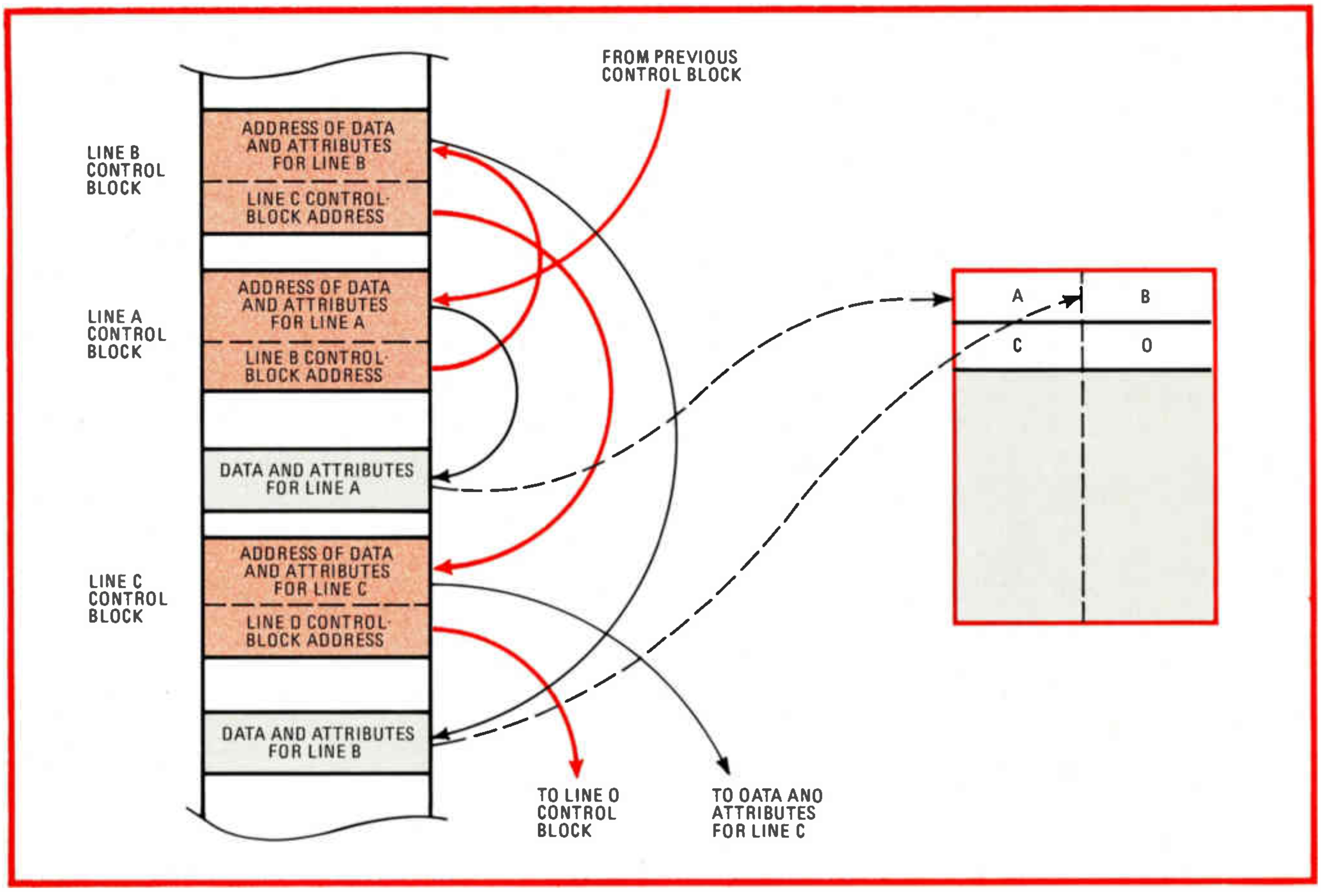
Depending on how well the SCU 1 is accepted by customers, Mostek officials say more SCU-type products with different functions may be produced later. Nor will SCU 1 suffer from lack of field marketing support. Burckle, who holds a BSEE and a master of engineering degree from the University of Louisville, Ky., is currently pursuing a master of business administration degree at North Texas State University in Denton and has become a Mostek product marketing engineer, with duties including the SCU 1. "I was the father of the product," he notes, "and I'm not going to let it die . . ."

-Wesley B. Iversen

intelligent peripheral chip. "It's unique," he says. "It's a user-programmable, single-chip microcomputer that eliminates the interface contention between itself and a main processor." So popular is the 8041A that Signetics also makes it and Intersil plans to produce a C-MOS version. "You're going to see a lot more in terms of slave chips," says National's George Chao, adding that an 8041A-like device is under consideration. "We'd put it in X-MOS, so it would be faster."

The 8041A has its buses and handshaking signals turned inside out, as it were, so that it looks like a slave (rather than a master) to the 8080, 8048, 8085, and 8086 microprocessor families. The 40-pin, +5-V-only part contains an 8-bit CPU, 64 bytes of data memory, 1 kilobyte of ROM (the 8741A has E-PROM), an 8-bit counter/timer, and 18 programmable I/O lines. Other features include an 8-bit status register, two data registers that act as an asynchronous slave-to-master interface, the ability to power-down the ROM, and the capability to work with a DMA controller.

Intel has already preprogrammed the 8041A as an IEEE-488 interface-bus controller (the 8292), a dot-matrix printer controller (the 8295), a data-encryption unit (the 8294), and the iSBC 941 industrial digital processor. The 941 is preprogrammed for stepper motor control, event sensing, frequency counting, and other useful industrial control functions. As for future generations, Intel's Don Phillips declines to get specific, but



6. Linked list. Advanced Micro Devices is working on a CRT controller for the Z8000 that will treat the refresh memory as a linked list. Control blocks in memory point to the location of data and attributes as well as the next control block. Here the screen is split in two.

suggests watching for the incorporation of more system functions on the chip, as well as more RAM and ROM, to increase printer capacity and to handle hard disks, for example.

Fairchild Semiconductor in Mountain View, Calif., plans to carry this idea a step further. According to Dean Bennett, microcomputer applications manager, it will allow the user to define his own microcomputer through the selection of four option modules: an analog section, a timer, an interrupt and control section, an I/O section, and one for time-related functions. The basic "engine" will be the 3870 CPU, and the other modules will supply such functions as analog-to-digital and d-a conversion, time-of-day clocks, and serial communications. The choices will be fed into a computer-aided-design system, and out will pop the chip. "As different configurations are designed, they will be added to the CAD library," says Bennett. "Ultimately the user will be able to mix and match [them]."

An all-powerful slave?

At this point, one may wonder if there will ever be, with tomorrow's technology, an all-powerful universal slave, capable of handling any peripheral function, regardless of complexity. It appears, however, that this will never be the case. Although chips like the 8041A point in this direction, applications do not stand still; the resolution of CRT displays gets higher, disk transfers get quicker, and protocols can always be emulated more completely. Thus, peripheral chips will always be forced to chase ever-demanding applications.

"You want to integrate as much of the common stuff as you can," says Intel's Dave Gellatly, in which he includes the CPU, RAM, ROM, and perhaps serial communications and a DMA interface. "But you always wind up trading performance for generality. Even with the 8086 there are communication controllers that you could not integrate onto the same chip. So you build a dedicated peripheral, optimized to get the performance you need."

Conrad Boisvert, Synertek's applications manager, says that chip makers are "running out of gas in terms of what can be put on a general-purpose controller and still have it be general-purpose. There may have to be programmable peripherals that allow the user to program them." "As a general rule," remarks TI's Jim Huffines, "programmable devices are used to address the lower-volume applications. As you move into higher volumes, and as the application becomes more cost-sensitive, you start to realize the demand for a dedicated peripheral design."

"The dedicated function controller is used where you can't take the degradation in throughput of a smart peripheral controller," says Motorola's Steve Sparks. Some applications "require that you remove all superfluous gate delays and let the commands blitz through at lightning speed to accommodate the function." □

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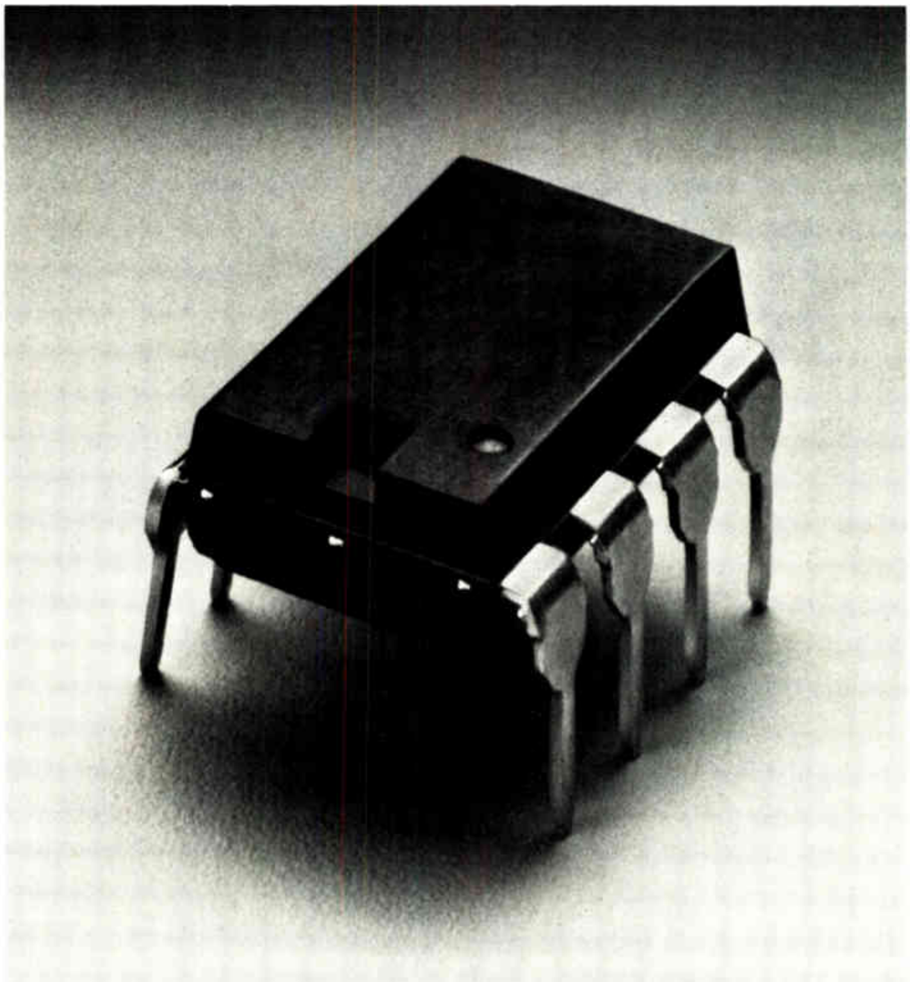

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Wafer stepper steps up yield and resolution in IC lithography

by Aubrey C. Tobey, *GCA Corp., Bedford, Mass.*

☐ The past five years have seen an enormous increase in the complexity and density of integrated circuits. As this density has increased, so has the need for greater resolution, better registration, greater throughput, and better yield. Classical lithographic techniques for exposing wafers, however, have been close to reaching the limits of their technology.

The direct-step-on-the-wafer (DSW) technique was introduced to meet the new needs that have arisen with complex ICs such as the 64-K random-access memory. In contrast to earlier lithographic processes, DSW projects a single IC master pattern at a reduction ratio, stepping and repeating it on the wafer to obtain an array of patterns over the entire surface. It combines basic photolithographic components with appropriate stage motions, controls, and software for modification of position and for repeatability of exposure.

With the advent of the 64-K RAM a year ago, it was evident that both a time gap and a technology gap existed. 16-K RAMs used 4-to-5-micrometer minimum geometries and had chip sizes on the order of 5 to 6 millimeters. But circuit technology had now improved to the point where it was possible to scale down detail enough to make a 64-K chip of the same size. This process required smaller, 2-to-3-micrometer geometries, which the available lithography systems could not produce if they were to maintain the throughput that was necessary.

The solution seemed to lie in electron-beam or X-ray exposure. But the throughput rates of commercial electron-beam machines available could not meet market demands and still give an attractive return on investment and bit cost. And though an X-ray technology existed, no machines were yet commercially available. Projection printing systems, at a ratio of 1:1, were experiencing considerable yield loss because image quality suffers at 3 μm; aberrations in the optical system also cause registration problems.

DSW promises to solve another problem. Wafer sizes have been increasing from 3 to 4 inches, and a size of 5 in. has been projected for 1980. This means that the competitive 1:1 projection systems will need to scale their optics up, which will cause greater problems of stability and focus.

To assess the DSW's potential, GCA Corp.'s Burlington, Mass., division conducted market research to establish criteria for selecting a microlithography system for the 1980s. The information obtained from this research is shown in Table 1.

Initially, bubble-memory manufacturers had the greatest interest in DSW because system performance specifications appeared to accommodate the resolution and tolerance constraints of bubble memories. Later, DSW became of great interest to MOS manufacturers, and it will be used primarily in that area.

A lithography comparison

A comparison of DSW with other lithographic techniques—1:1 projection printing, electron beam direct-write-on-the-wafer, X-ray lithography, and contact printing—does not imply that they are all competitors. In fact, these systems are complementary and can be used together, with the exception, perhaps, of X rays. The X-ray machine will be definitely competitive with the DSW, if and when it is developed commercially. Figure 1 shows the dates of production use, both historical and predicted, for various techniques. Note that the range of usefulness is a function of economics as well as a function of performance parameters.

In heavy use today, 1:1 projection printing is suitable for 4-to-5-in. wafers and minimum geometries of 3 μm. Throughput rates for this type of optical system are about 30 to 100 wafers per hour, depending on the minimum geometry and its requirements, which are directly reflected in the registration alignment time and the scanning rate.

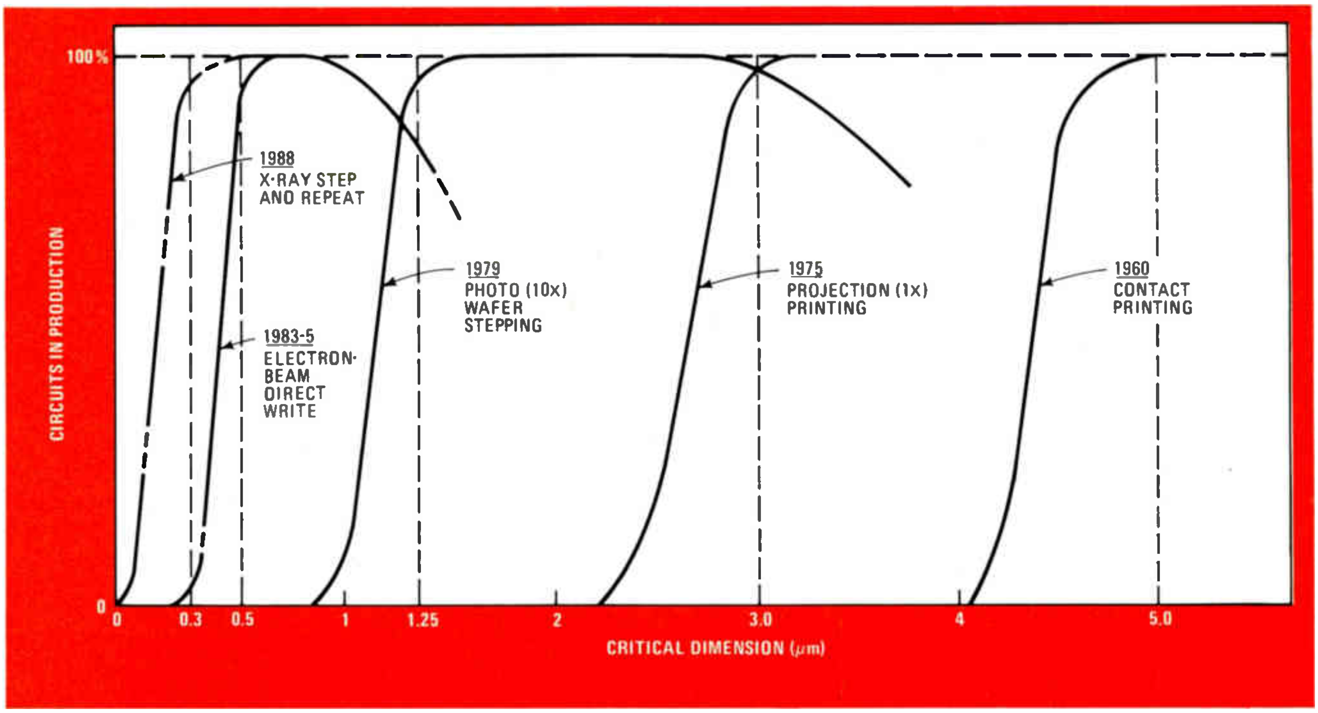
In a 1:1 projection system, decreasing the IC pattern's geometry slows the scanning rate, decreasing throughput considerably. Additionally, as geometries are reduced, the smaller size makes defects more critical. For example, if a circuit with 5-μm minimum features is being manufactured, then 1-to-2-μm dust particles are not a problem. However, if proper cleanliness is not maintained, these generally nonrepetitive defects will have a gross effect on yield.

Another major factor is system reliability—that is, consistency of performance in a variable environment. The optics of the 1:1 projection system are fairly complicated, requiring frequent realignment. Also, the system's physical layout limits its optical performance.

A solution to resolution problems with this type of

TABLE 1: SELECTION CRITERIA FOR LITHOGRAPHIC SYSTEMS

Criteria	1980 need	1985 need
Minimum geometry	2 μm	submicrometer
Size control	5 – 10%	1 – 10%
Die size	3 – 20 mm	2 – 20 mm
Wafer size	100 – 125 mm	75 – 150 mm
Accuracy	0.5 μm	0.5 μm
Precision	0.25 μm	0.125 μm
Throughput (bits/hr)	sufficient to maintain or decrease cost/bit	
Time required for turnaround or new design	days	days
Time required for return on investment	2 years	2 years



1. A lithography projection. This is a possible scenario for the evolution of lithographic techniques for integrated circuits. All dates are production-use dates. Note that direct-step-on-wafer systems are not economically competitive above about 4 micrometers and that X-ray step-and-repeat equipment will most certainly be competitive with direct-step-on-wafer, depending on its costs.

lithography is thought to be the development of a system using a deep ultraviolet light source instead of the near UV. If the deep UV is used, the indications are that it would be possible to image 0.5-μm geometries successfully. It should be remembered, however, that as the minimum linewidths and features decrease, defects become all-important.

The 1:1 projection system is vulnerable to 1- and 1.5-μm dust particles on both mask and wafer. As a consequence, if geometries of 1.5 to 1.8 μm or less are involved, the presence of this dust will seriously affect the yield. Furthermore, only one deep UV system has been developed in Japan and this has not proven itself in production for high throughput of wafers. Comparative yields versus defect sizes are shown in Fig. 2.

Another goal is to achieve the ability simply to change the wavelength of illumination and obtain appropriate results in both resolution and registration or overlay.

With regard to electron-beam lithography, its potential place in the microlithography spectrum is not in question. It lends itself easily to submicrometer geometry. Operating in a vacuum, electron beams are plagued by very few defect problems. The two major drawbacks at this time, however, are price and throughput rate. It is not economically possible to produce the kinds of circuits projected over the next five years using this technology without improvement in throughput and a commensurate reduction of cost per bit.

Contact printers can produce submicrometer geometries and can use the deep UV. However, the defect level and the overlay tolerances are major drawbacks, and contact printers will find very few applications in the circuits of the future.

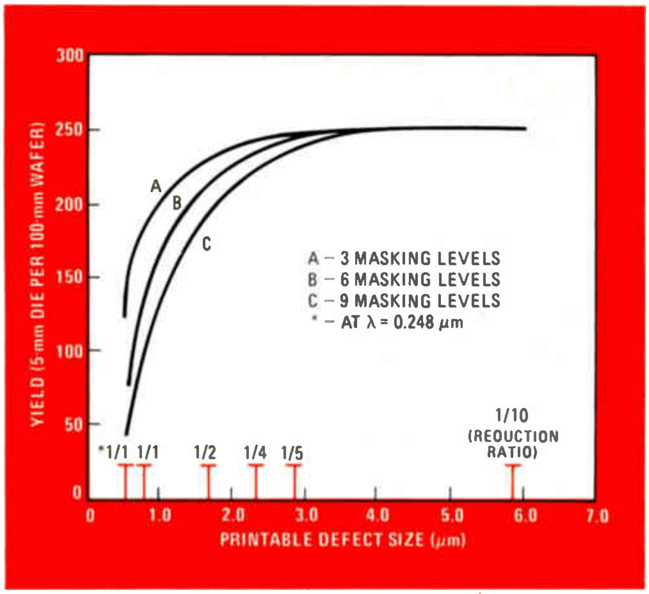
Another technique, proximity printing, deserves some mention. There is a printer on the market today that can achieve geometries down to 2 μm. And if it is used as a contact printer, it can go down to 0.5-μm geometries. Once more, however, throughput projections for it are fairly low and not consistent with industry needs.

Considering the economics of the situation, it appears that for production of today's circuits, such as 16-K memories, the scaling capability of the DSW makes it extremely attractive when compared with 1:1 projection printing. However, scaling capability is a function of optical resolution and registration performance.

Dollar figures

Estimates show that the cost of a DSW system over a one-year period for production of 16-K memories is in the order of $1.1 million. Comparable cost for the same yield of good dice of a 1:1 projection system is in the order of $1.6 million to $1.7 million, and, in fact, two 1:1 projection systems would be required for the same throughput in dice per year. Since the yield is much lower, and because scaling is not so good as with the DSW, costs go up. The basic cost of a DSW machine today is in the order of $500,000. The basic cost of a projection printer ranges from $180,000 to $230,000. In comparing the two systems, the highest number for the DSW and the lowest for the projection printer are used. Some real data is shown in Table 2. The integration densities result from the scaling capability of each system.

The unique advantages of the DSW system over 1:1 projection printers are, first, that it is able to take a wafer with any diameter up to 6 in., and second, its present resolution capability is in the order of 1.25 to 1.5 μm for 6-to-9-layer circuits that use the current wafer processing techniques.



2. Yield factors. Defect size, lens reduction ratio, and number of masking levels are all factors that affect the useful die per wafer. The plot shows that a 1:1 lens system is much more vulnerable to defects caused by small particles than a 10:1 lens system.

This means that 1.25-μm circuits can be imaged in 1-μm resist on topologies ranging from 0.5 to 1 μm in the Z direction and on physically distorted wafers that cause problems with 1:1 projection printers.

In contrast to other methods, the wafer stepper is not approaching the limits of its technology. Improved refractive optics are already under consideration, whereas the 1:1 system is about as refined as it will be.

The DSW also accommodates potential wafer distortion better than a 1:1 projection printing system because it exposes a small area at a time. Its adaptability is also evident in that, if a wafer's distortion can be characterized linearly, program corrections can be incorporated that will retain the overlay tolerances a circuit requires. If the wafer distortion is nonlinear and cannot be characterized in a linear fashion, then the potential exists for alignment by zone or by die on the wafer.

Another factor of great concern to an IC manufacturer is control over the size of each chip and of the area between chips on the wafer. A single scanning projection system cannot accommodate size-control variations caused by wafer distortion in the Z direction or by variations in intensity of illumination, which appear to be on the order of ± 10% for the projection printer.

The DSW specification on illumination uniformity is ±2.5%. This takes care of most size-control problems related to exposure time. The ability to autofocus—to maintain a fairly constant distance within ±0.5 μm with a 0.1-μm precision—eliminates variations caused by scanning the entire surface of the wafer, without control in the localized area of focus.

A major parameter that deserves mention is the effect of repetitive defects, which are extremely critical to the yield of good dice.

In equipment design, three basic parameters are numerical aperture (a measure of the resolving power of an optical system), wavelength, and field size. Simply reducing wavelength is insufficient to improve performance, since resolution appears to be more a function of field size than wavelength, especially in regions between 2,000 and 5,000 angstroms. While the DSW machine is limited by the field size of a single exposure, the 1:1 projection system is limited by the resolution obtainable at the field sizes equivalent to the wafer diameter. To design a system for the deep UV, some real and extremely major technological breakthroughs must be made. However, for DSW to accommodate resolution requirements, at least down to the 0.7-μm range, is a matter of good engineering.

TABLE 2: COMPARISON OF LITHOGRAPHIC TECHNIQUES FOR AN 8-BIT MICROPROCESSOR

	Traditional	Projection	Direct step on wafer (10:1)
Design rule	6 – 5 μm	4 μm	2.8 μm
Effective channel length of gate	4 – 3.5 μm	2.8 μm	1.5 μm
Inner gate transmit delay time (fanout 3)	8 – 10 ns/gate	4 – 6 ns/gate	2 ns/gate
Power-delay time table	4 pJ	1 pJ	0.25 pJ
Chip size	8.1 by 8.1 mm^2	5.4 by 5.4 mm^2	3.8 by 3.8 mm^2
Integration density	110 gate/mm^2	240 gate/mm^2	480 gate/mm^2
Process	photo mask; contact aligner; negative resist; wet etching	photo mask; projection aligner (1:1); positive resist; wet etching	EB mask; DSW; positive resist; wet and dry etching

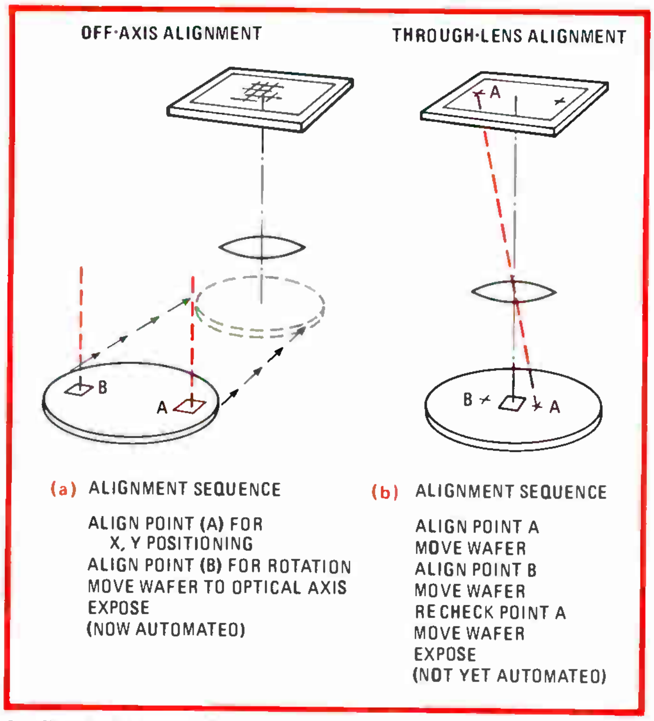
Through the lens versus off axis

Basically, in any DSW operation, the wafer is placed under the optical column and moved to discrete locations for exposure of a given chip. The system images a master pattern through a reticle, at a reduction ratio ranging from 4:1 to 10:1 onto the wafer. The reticle is manufactured by either a photo-optical pattern generator or an electron-beam reticle generator.

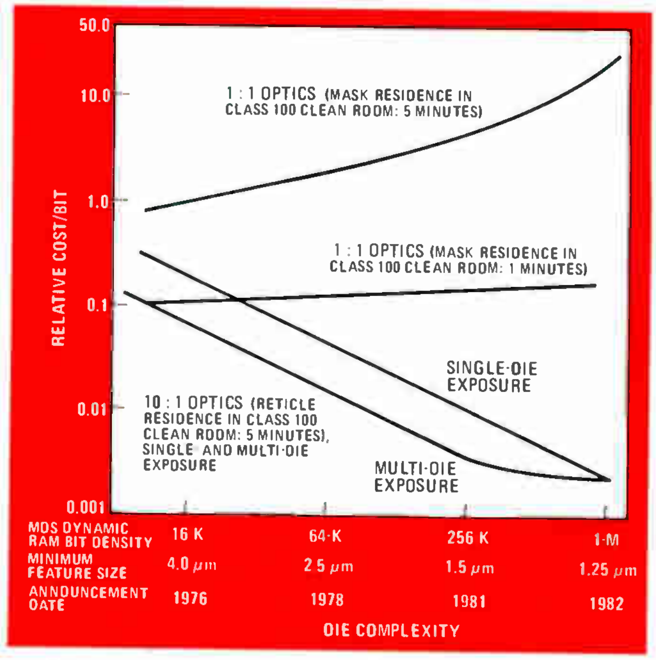
When the wafer is first placed on the stage, it must be aligned to the motions to obtain overlay when an array of exposures is made. The alignment may be off axis—that is, off the main optical train axis—or it may be through the lens that is used for the reduction and imaging of the pattern on the wafer.

The alignment capabilities for both methods are virtually equivalent, with two sigma-errors on the order of 0.25 μm. To date, no automatic wafer-to-master reticle-alignment (exposure-to-exposure) schemes are commercially available. The off-axis alignment of the 4800 DSW Wafer Stepper is now automated.

Either negative or positive resist can be used in a wafer-stepper machine. However, there is at present a trend toward positive resists, and future circuits using positive-resist processing exclusively may be expected. The uniform thickness of the resist is certainly of paramount importance, because the total exposure time is a function of this thickness and that time can vary across the wafer if the resist has not been spun on uniformly—a



3. Alignment methods. The two methods of aligning a DSW system are shown in (a) and (b). Off-axis alignment is simpler to automate and has a higher throughput. Through-the-lens alignment is capable of aligning even the most distorted wafer a chip at a time.



4. Cost per bit. This plot shows the relative cost per bit versus die complexity for a 10:1 lens reduction wafer stepper compared with a 1:1 projection system. Note that for the 1:1 system, as die complexity increases, cost per bit goes up. The opposite occurs for DSW.

problem that is inherent in all imaging systems.

The DSW system can expose any substrate that can be photosensitized and developed, including glass, silicon, garnet, and sapphire. Its optics include an illuminator with an intensity about 7 to 10 times that of ordinary photolithographic imaging systems.

The DSW uses a chrome-on-glass reticle rather than a mask. The mask is at final size and a reticle is considered to be from 2 to 10 times larger than the final image. This size ratio is a distinct advantage over 1:1 projection printing in terms of photolimited yield (Fig. 3).

As mentioned, the alignment can be done either through the lens or off-axis. The problems include wafer distortion, the impact of alignment technique on throughput rates, and the limits of overlay tolerances. If the distortion is great enough and nonlinear, alignment must be done die by die or zone by zone. This can best be done at present through the lens. However, that the off-axis technique is very suitable for the geometries anticipated over the next several years is a fact that should be underscored.

By far the fastest technique with minimum impact on throughput is off-axis alignment. During a given exposure sequence, the wafer is aligned to the stage only once with laser-metered interferometry to provide appropriate overlay. The stage motions are in turn referenced to the optical column through the laser metered beam.

Compare throughput using manual, off-axis, one-time alignment per wafer and automatic die-by-die alignment. With manual off-axis alignment, tests show the 100-mm-diameter wafer throughput with 89 exposures/wafer to be 39 wafers/hour.

If an automatic exposure-by-exposure (die-by-die) alignment is substituted, each alignment takes 1 second. Then 89 seconds per wafer is required as compared with one-time, manual alignment of about 15 seconds, with a consequent reduction in throughput to about 19 wafers/h. At 0.5 s/alignment, this would be about 25 wafers/h and at about 0.17 s/alignment, the throughputs would be equal.

Until appropriate assessment can be made of the extent of wafer distortion in a lateral direction (that is, "continental drift"), the off-axis alignment scheme seems much more appropriate than a through-the-lens scheme. If a through-the-lens scheme is adopted for research in circuit development, production demand must still be faced: how will circuits be produced in quantities commensurate with need, at prices that are acceptable to the customer?

Economics

Little can be said about the economics of electron-beam or X-ray microlithography since no data worthy of consideration is yet available for direct exposure on the wafer. But data is available for projection systems at 1:1 scanning exposure and for 5:1 and 10:1 reduction ratio step-and-repeat systems.

Analyses have been made that show the comparative impact of scaling—or "shrink"—and of defects caused by environmental dust on either a mask (for 1:1 projection) or a reticle (for DSW). The conclusions with regard to shrink are that the DSW resolution and alignment capability permit twice as many gates as those obtainable with commercially available 1:1 projection systems (Table 2). As to defects, yields are acceptable for the 10:1 to 4:1 reduction ratio range, but at 1:1, they are too low to be competitive with DSW (Fig. 4). This data is based on actual pilot production situations. □

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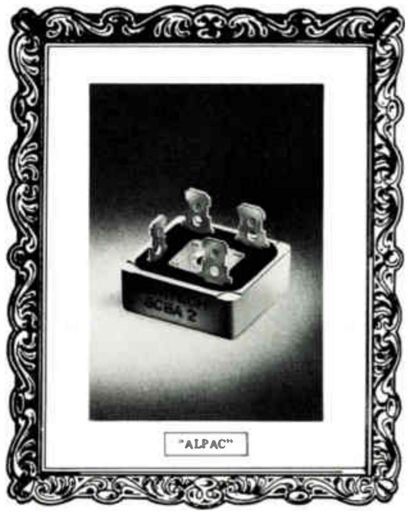

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Compact industrial ammeter measures 10-ampere peaks

by Paul Galluzzi
Beverly, Mass.

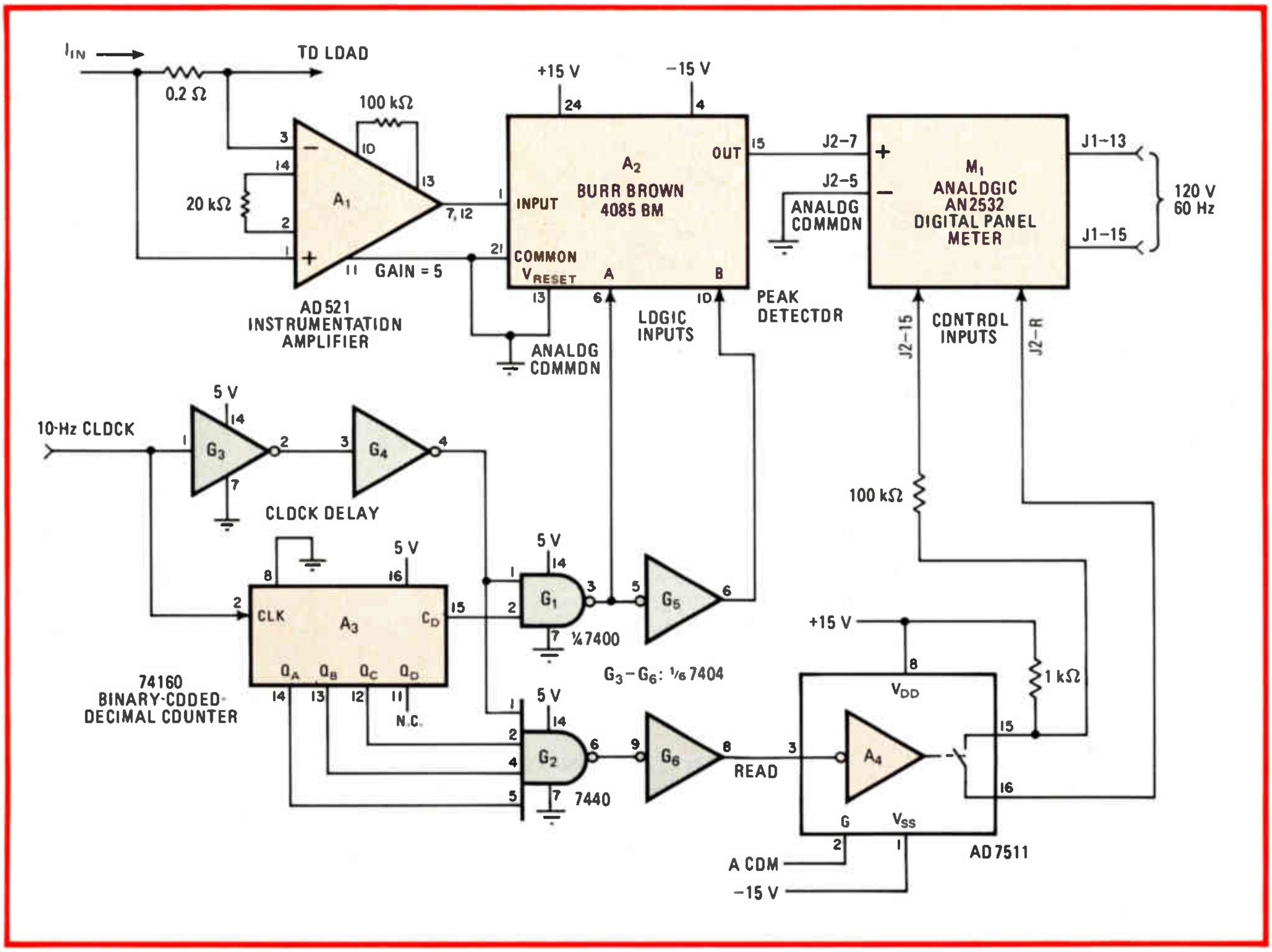
A self-contained sample-and-hold amplifier and a digital panel meter make this device small, rugged, and suitable for measuring peak currents in industrial applications. Although not inexpensive (it can be built for about $65 in small quantities), it is an easy to build, accurate, and reliable peak-reading ammeter.

The 0–10-ampere pulses to be measured are converted to a voltage by instrumentation amplifier A_1, such that the input to peak detector A_2 swings 1 volt for each ampere at the circuit's input. A_2's output voltage then drives digital voltmeter M_1.

The timing pulses for A_2's sampling cycle are derived from a 10-Hz clock signal by gates G_1–G_6 and binary-coded-decimal counter A_3. The decoded clock pulse introduced at gate G_2, along with the delayed clock pulse from G_3 and G_4, form the read pulse for sampling the output of the peak detector for a 50-millisecond interval, and holding that reading for the remainder of the one-second cycle.

During that time, clock inputs A and B reset A_2 to zero. Flutter caused by the 50-ms sampling pulse cannot be detected visually. □

Designer's casebook is a regular feature in Electronics. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.



Rugged and reliable. Ammeter using hybrid sample-and-hold amplifier, digital panel meter, and standard logic components is ideally suited for measuring pulses of peak current in hostile environments. Readout is in peak amperes, accurate to 0.1% over −25° to 85°C.

Current source for I^2L saves energy

by Stephen H. Nussbaum
Data/Wave Development Inc., San Diego, Calif.

To capitalize on the low-power advantages of integrated injection logic (I^2L), a power source that also dissipates relatively small amounts of energy is required. This switched-mode supply provides programmable currents of up to 300 milliamperes at 2.3 volts to boards utilizing I^2L loads, with an overhead of only a few milliamperes needed for running the circuit.

The voltage-current characteristics of I^2L devices resemble those of the standard switching diode, whose operation is determined by the amount of driving current available. It is therefore necessary to drive these loads with a current source. Although a single high-value resistor in series with a voltage source would serve to deliver constant current, large amounts of power would be dissipated in the resistor. The difficulty is overcome with this circuit.

Q_1 and its associated components provide a reference current for the complementary-MOS quad analog switch, A_1, in the reference-resistance subcircuit. The R_2C_3 combination helps to stabilize the output against changes in input voltages.

A_1's switches are wired together such that its equivalent series resistance may be set to one of two values by a control signal. It is possible to order as many as five current levels with this switch if additional programming inputs are introduced.

A_1, with the aid of R_3, serves partly as a current-to-voltage converter, so that low-power oscillator A_2 sees the reference current as a representative voltage at its inverting input. This potential will cause Q_2 to switch on periodically. R_4 provides positive feedback for hysteresis, thus controlling the rate at which A_2 and Q_2 are switched—16 kilohertz, in this case. The 10 to 30 millivolts of hysteresis also appears at the output, but this poses no problem with I^2L loads.

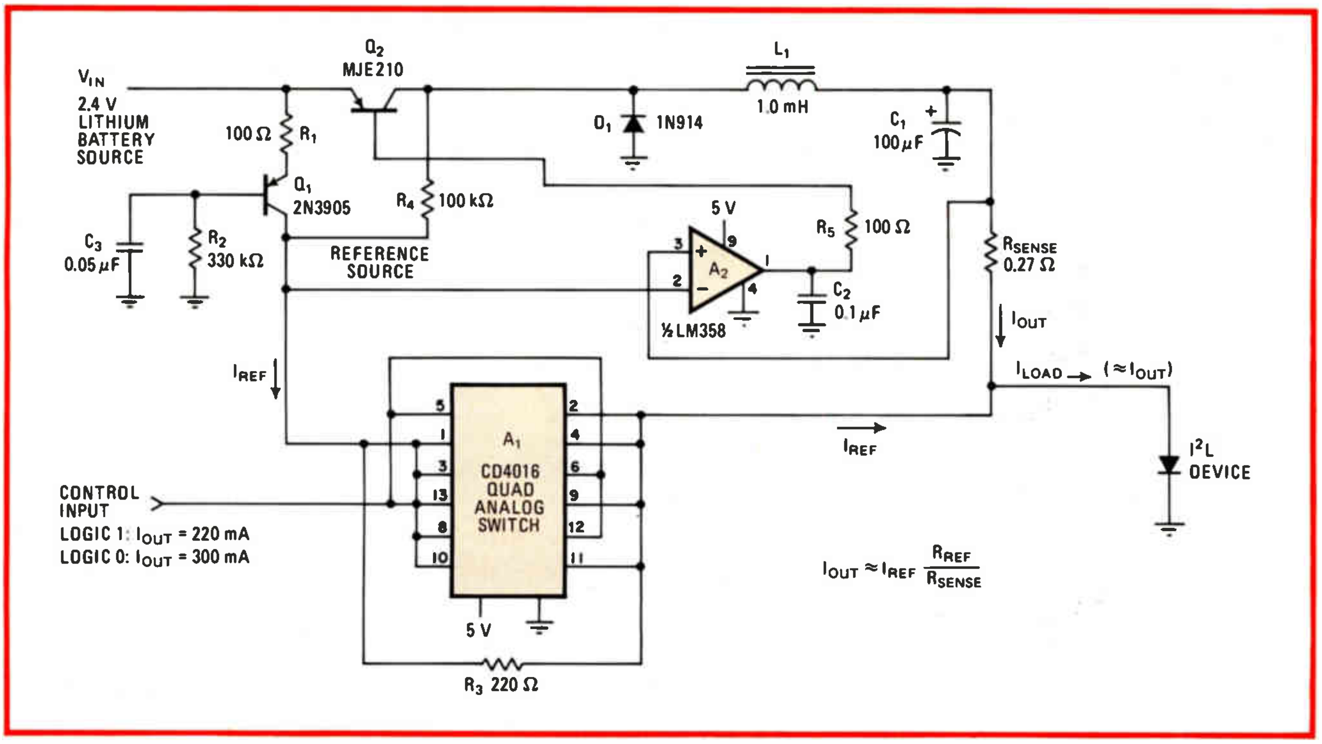
L_1 and C_1 comprise the switcher's required storage elements, acting to release energy to the load through R_{sense} when Q_2 is off. R_{sense} is part of a feedback network used to set I_{out}.

Because the reference current and the output current at summed at the output node, A_2's input sees only the difference of these currents scaled to a voltage by their respective resistors, R_{sense} and R_{ref}. Thus the output current is set solely by the feedback loop. As a consequence of this arrangement, $I_{out} \approx I_{ref}/R_{sense}$. The efficiency of the supply is maximized by using a lower value of R_{sense}, a faster op amp for A_2, and a storage inductor (L_1) with as little dc resistance as possible.

With R_3 = 220 ohms and with I_{ref} = 0.60 mA, I_{out} = 220 mA if a logic 1 is applied to the control input. I_{out} = 300 mA for a logic 0. These values can be changed by suitable selection of I_{ref}, of course, but R_3 may also be varied. Note that:

$$R_{ref} = [(r_{on}/n)R_3]/[(r_{on}/n) + R_3]$$

where n = number of switches and r_{on} = on-state resistance of one switch in A_1, typically 600 Ω. □



Injecting current. Switching source delivers constant current to members of low-power I^2L logic family without wasting much power. Small reference current, C-MOS switches, and low-power oscillator contribute to circuit efficiency. Two-level current source, which generates up to 300 milliamperes at 2.3 volts, can provide one of five current values if additional programming inputs are introduced at switch A_1.

High-speed generator pulses ECL loads

by Andrew M. Hudor Jr.
Department of Physics, University of Arizona, Tucson

Serving the needs of designers and technicians who work with high-speed digital circuits, this inexpensive two-chip pulse generator is invaluable in trouble-shooting emitter-coupled logic. Besides generating signals having frequency and duty cycles that are adjustable to its complementary outputs, the versatile generator also provides two ports at which pulses with a constant 50% duty cycle are available.

One section of a 10116 ECL line receiver, A_1, is used as an RC oscillator[1] whose period is determined by the potentiometer P_1 and the capacitor selected by the frequency-range switch. With the values shown, the oscillator frequency can be varied from a few hundred hertz to more than 50 megahertz. The output of the oscillator is then buffered and squared up by a Schmitt trigger, A_2, which is the second section of the line receiver.

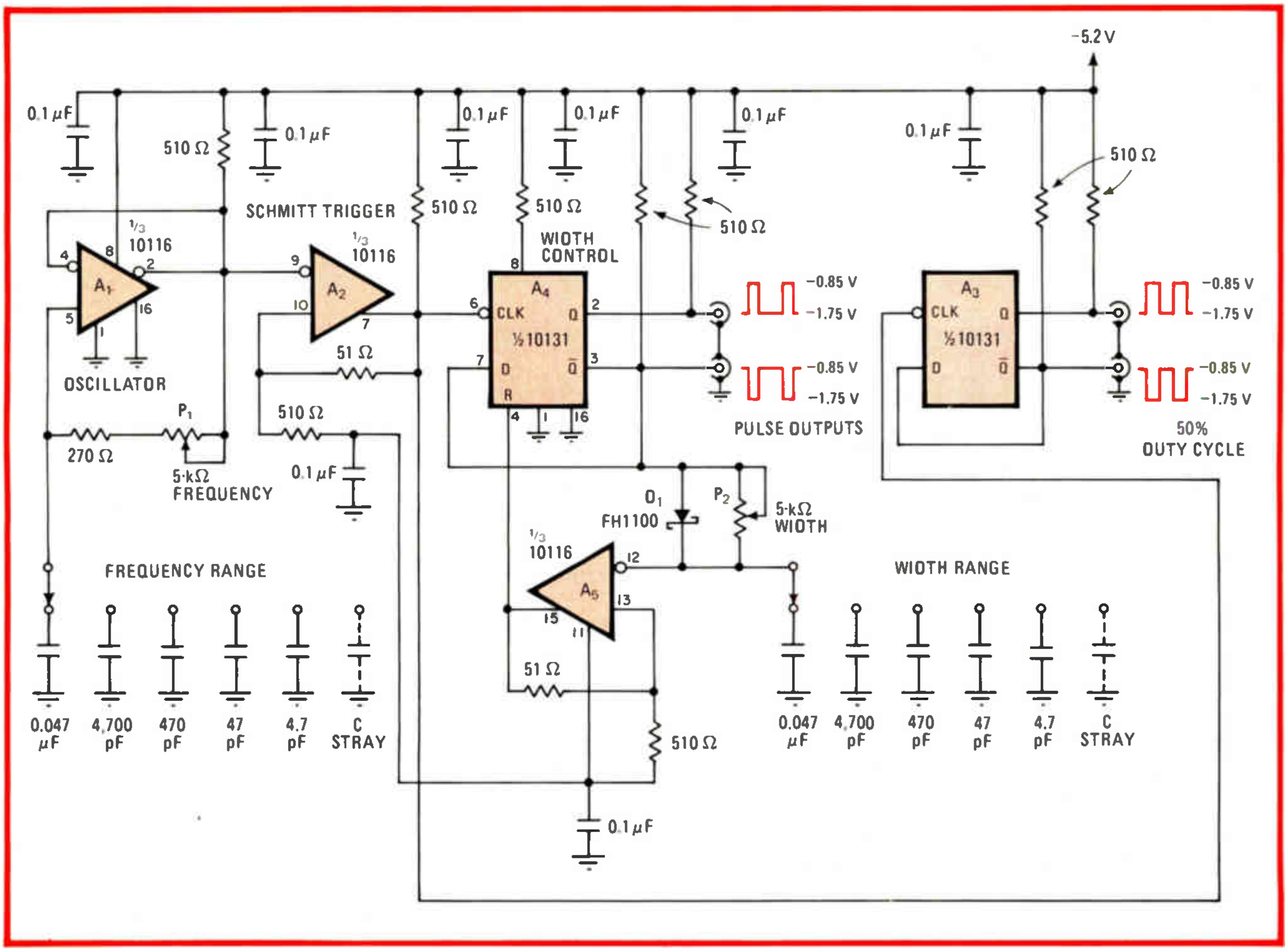
A_2's output toggles both sections of a 10131 dual-D flip-flop, A_3 and A_4. A_3 provides for a 50% duty cycle output, while A_4 and the remaining section of the receiver, A_5, form an adjustable one-shot multivibrator. Here, A_5 serves as a second Schmitt trigger.

The Q output of A_4 is fed to the input of the Schmitt trigger through an RC integrator formed by P_2 and the capacitor selected by the width-range switch. When Q toggles low, the input to the A_5 trigger slowly rises as the capacitor charges. When the trigger level is reached, the Schmitt trigger's output goes high, resetting A_3 and A_4, and the process is repeated.

The time it takes for the integrator to reach the trigger level defines the pulse width. With the values shown, widths from 15 nanoseconds to 10 milliseconds can be selected. Upon resetting of the flip flops, Schottky diode D_1 allows the capacitor to discharge rapidly. The width control allows adjustment of the duty cycle from nearly zero to 50%. For applications where a duty cycle greater than 50% is required, the complementary output should be used.

If desired, a buffer can be easily added at A_3 and/or A_4 in order to drive 50-ohm lines directly. □

References
1. William A. Palm, "ECL IC oscillates from 10 to 50 MHz," *Electronics*, Circuit Designer's Casebook 14D, p. 109.



Speedy. Line receiver and dual flip-flop generate high-frequency pulse trains for emitter-coupled logic. Signals to 50 MHz having widths that are adjustable from 15 ns to 10 ms appear at generator's complementary outputs. Circuit also provides output at duty cycle of 50%.

Array processor responds in real time

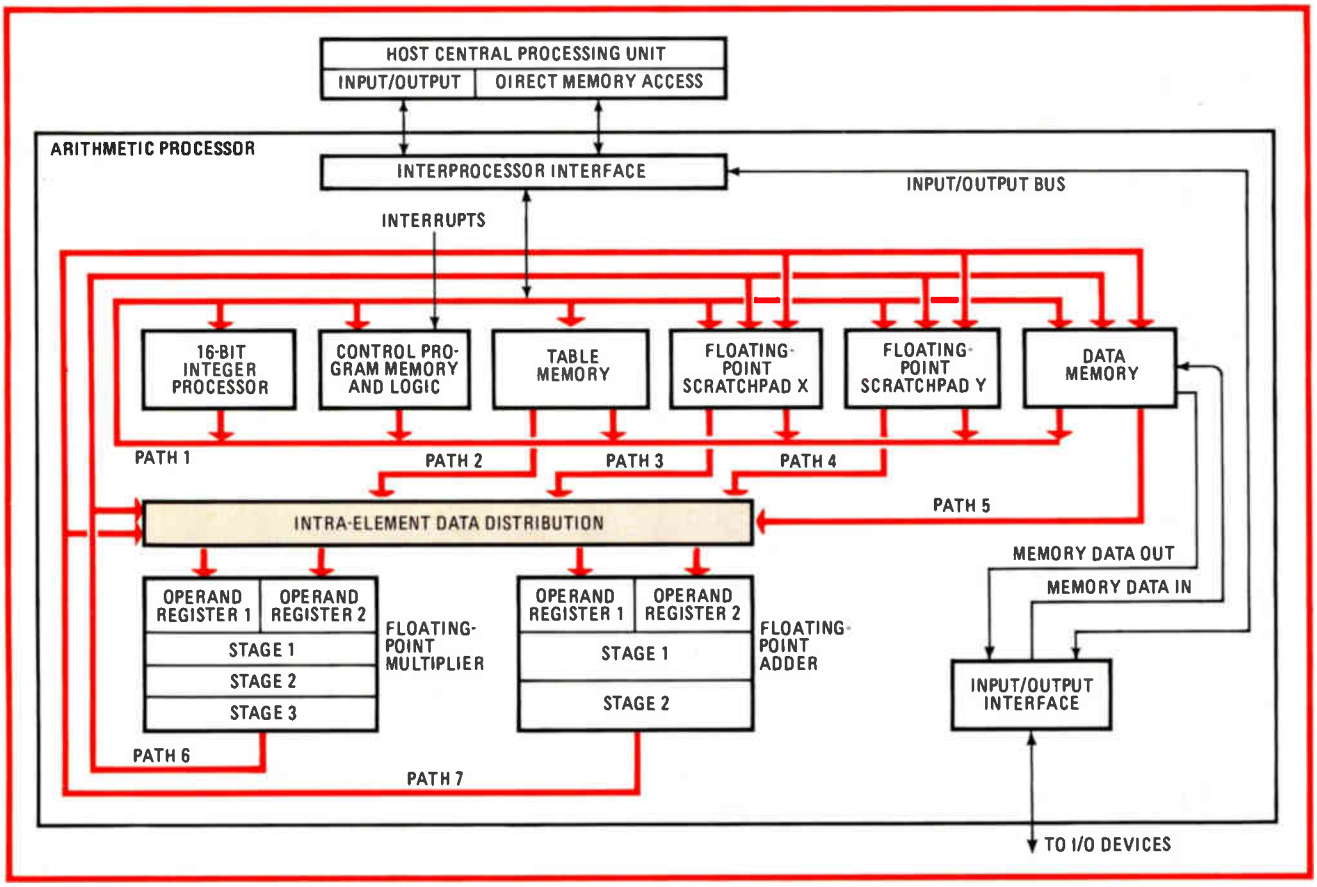
Peripheral machine has its own multitasking supervisor and performs up to 8 million floating-point operations per second

by James Strelchun, *Floating Point Systems Inc., Beaverton, Ore.*

☐ Specialized number-crunching machines able to perform rapid high-precision arithmetic over a large dynamic range are becoming very popular for beefing up the throughput of computer systems used in scientific applications. Often called array processors because of their optimization for performing repetitive calculations on an array of data, these peripheral arithmetic processors are not to be confused with machines having an internal array architecture, such as vector processors (see "Array processors, vector processors").

Floating Point Systems Inc. has added a new member to its line of array processors that incorporates up-to-date semiconductor technology and a priority interrupt scheme supported by the machine's own multitasking operating system, thus adding new real-time operating capabilities. These design changes make the FPS-100, which is intended for original-equipment manufacturers and systems integrators [*Electronics*, April 12, 1979, p. 209], easier to attach to the host computer system. The use of today's low-power Schottky TTL in medium- and large-scale integrated circuits reduces the new peripheral processor's chip count, physical size, and power consumption.

Applications such as flight simulation, radar signal analysis, X-ray tomography, image analysis, speech synthesis, and nuclear reactor monitoring require large



1. Parallel procedures. A separate floating-point multiplier and adder allow the FPS-100 to perform arithmetic operations in parallel. Seven 38-bit data paths distribute data among these arithmetic units and the parallel memories; a 16-bit integer processor handles control functions.

Array processors, vector processors

Array processors are computers dedicated by their design to performing repetitive arithmetical calculations on large arrays of data with high precision, wide dynamic range, and high throughput. Usually most input/output operations and file management chores are left to the host computer, in order to free the peripheral array processor to concentrate on its calculations.

As they become more popular, however, a semantic distinction must be made between array processors and other specialized processors with similar sounding names. An array processor consists of a single computer that operates on one piece of data at a time.

Vector processors are also specially designed for performing arithmetic on arrays of data, but they operate on an entire row or column of the array—the so-called vector—at once. Among new computer architectures, there is something called a distributed array processor. It consists of multiple arithmetic and logic units, each of which is associated with its own block of memory and operates on a separate piece of data simultaneously with all the others [*Electronics*, April 27, 1978, p. 69].

The well-known vector processors—the Illiac IV, Control Data's Star, or the Cray Research I—sell for several million dollars, much more than the minicomputer array processors available from several companies, including Floating Point Systems, Data General, and CSP. **-A. Durniak**

amounts of scientific computations such as fast Fourier transforms, convolutions, and vector and matrix arithmetic. Many of these applications require the calculations to be performed rapidly enough to provide almost instantaneous response, for so-called real-time operation. Programmable array processors attached to standard commercial minicomputers can provide designers or OEM suppliers of such systems with an inexpensive alternative to a large, specialized scientific processor.

After considerations of throughput, precision, and dynamic range, the interfacing flexibility of the array processor is of concern to the system designer. He may have chosen one of a variety of host computers based on other application requirements; of course the array processor must be compatible with that host. If system design is to be completed quickly, an array processor that is relatively easy to program is very desirable. This requires an easily understood high-level programming language, or at the very least assembly language; the availability of a library of standard mathematical software routines is also a big help. And the systems integrator must of course concern himself with questions of physical size, power consumption, reliability, serviceability, and cost. Tradeoffs between cost and the desired features must be carefully weighed in the design of a marketable peripheral processor.

The FPS-100 is easier to program and interface than the current models—the AP-120B, which is also intended to be attached to minicomputers by end users, and the AP-190L, designed for use with larger mainframe computers. The new arithmetic unit is also roughly half the size and uses half the power of the other models. It is as much as one third slower than the other models, however, even though it can perform some 8 million floating-point operations per second—some 50 to 200 times more than standard minicomputers.

System hardware overview

Based on the same synchronous, multiple-bus hardware architecture as the older models, the FPS-100 is divided into two sections: the arithmetic hardware and the interprocessor interface. Its 38-bit floating point numeric format, compatible with the other models, is maintained throughout the hardware with the exception of the 16-bit integer control processor. This floating-point format provides extended precision by devoting 28 bits to the mantissa and 10 bits to the exponent. (Binary coding rather than hexadecimal is used.) The result is precision of 8 decimal digits and a dynamic range of $10^{\pm 153}$. In contrast, 6 decimal digits and a range of $10^{\pm 38}$ are provided by a typical 32-bit minicomputer format.

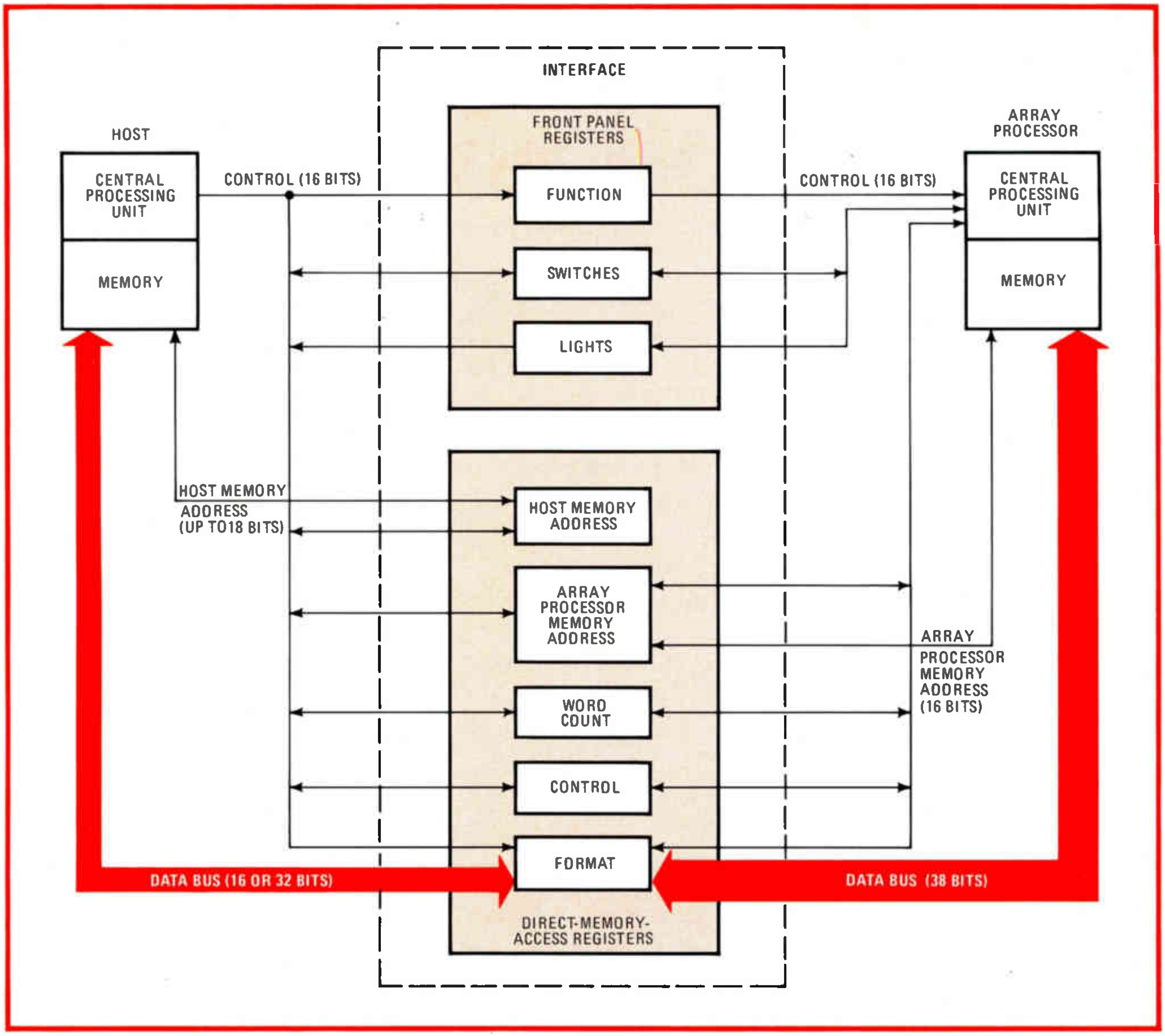
Because overall system control is handled by the host computer, the FPS-100's front panel consists of functional status indicators rather than operator controls. These indicators include power on, real-time mode, host interrupt enabled, direct memory transfer, array processor interrupt enabled, and array processor run.

The arithmetic processor section has a separate floating-point multiplier and floating-point adder that permit addition and multiplication to proceed in parallel (Fig. 1). Pipelining operations within these two units allow each to produce a new result every machine cycle (see "Pumping a full pipeline," p. 123). Given the processor's 4-MHz clock rate, this means computational results are produced as often as twice every 250 ns for a throughput of 8 million floating-point operations per second.

To keep up with these fast arithmetic units, parallel memories are used. One or 4 kilowords of memory are available for storing the 64-bit control program instructions; between 8 and 64 kilowords of memory are available for data storage. Numerical constants are stored in a separate table memory that consists of 2.5 or 4.5 kilowords of read-only memory or, optionally, 4 or 8 kilowords of random-access memory. Two banks of 32 38-bit floating-point registers are used as scratchpad memory for intermediate results. The FPS-100's synchronous design allows all of its memory elements to be accessed in a single 250-nanosecond clock cycle.

Seven data paths, each 38 bits wide, connect the various memories to the arithmetic units to avoid the delays which would result from all the data flow sharing a single bus. To simplify Fig. 1, the connections among these paths are labeled intra-element data distribution.

Overhead functions, including instruction decoding, address calculations, and program indexing for overall system synchronization, are performed by the arithmetic and logic unit of the separate 16-bit integer controller. This control unit has its own set of 16 16-bit general-purpose registers as well as a subroutine-return stack of



2. Host control. Two sets of registers provide the interface between the host computer and the arithmetic processor. One set performs functions analogous to the switches and lights on an operator's front panel and the second controls direct-memory-access data transfer.

16 12-bit registers. This frees the 38-bit floating-point hardware to concentrate on the programmed scientific computation, increasing throughput substantially.

To control the operation of so many parallel hardware elements, the 64-bit program instruction is divided into six groups of command fields. Just as a wide microcode instruction in a general-purpose computer will control many functions at once, so the program instruction of the FPS-100 simultaneously governs the operation of different parts of the hardware.

The first group within the program instruction is 14 bits long and directs the operation of the 16-bit integer controller. A 9-bit adder group controls the floating-point adder while a 9-bit branch group directs conditional branching. The next 19 bits in the program instruction, called the accumulator group, direct the flow of intermediate results between the floating-point arithmetic units and the registers. The floating-point multiplier is controlled by the next 5-bit group, and the final 8-bit group controls memory addressing.

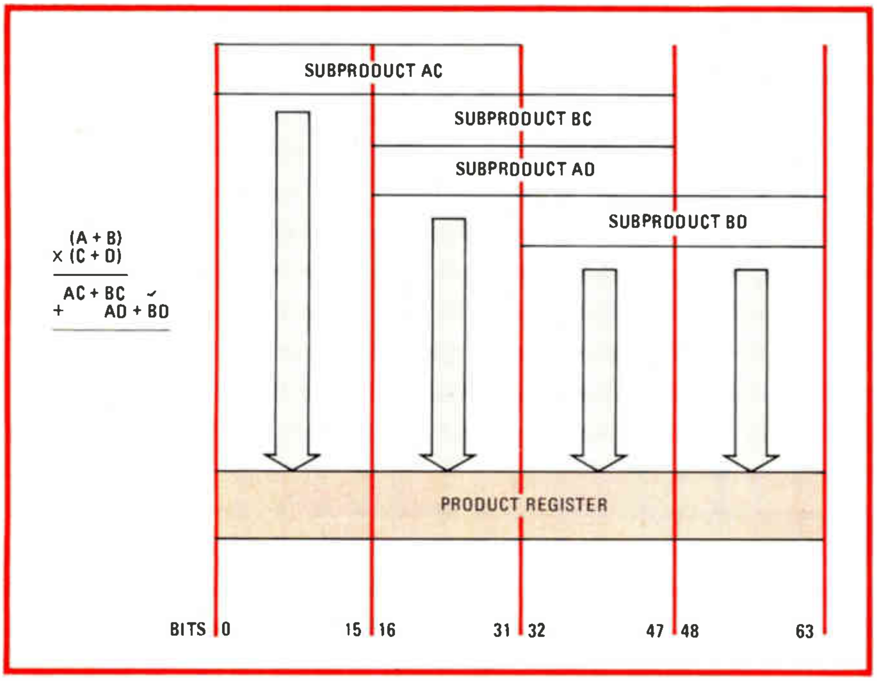
This 64-bit instruction word thereby allows up to 10 operations to proceed simultaneously—or some 40 million operations per second. This assures that in actual operation the arithmetic processor achieves most of its potential throughput of 8 million floating-point operations per second.

Communicating

The interprocessor interface provides communications between this parallel floating-point arithmetic hardware, the host computer, and additional input/output devices. Interfaces are available for operation of the arithmetic processor with a variety of hosts. Currently complete hardware and software support exists for operation with the Digital Equipment Corp. RSX-11M or RT-11 operating systems or the Data General RDOS operating system. Additional interfaces are planned.

The host computer and the arithmetic processor communicate through two sets of registers: one for the programmed I/O commands used for control and the other for data transfer (Fig. 2).

Although, as has been mentioned, the FPS-100 does



3. Dividing multiplication. Because the MPY-16 multiplier chip handles only 16-bit operands, four are needed to process the 28-bit mantissa used in the arithmetic processor. Each mantissa is divided in two and the subproducts added, with the result going into a single 64-bit register.

not have an operator's front panel, the control registers can be thought of as a simulated front panel controlled by the host. The first register is analogous to the front panel switches in that it is used to enter control or parameter data into the arithmetic processor. The second register is like panel lights; it is used by the host to examine the contents of the arithmetic processor's internal registers. The host writes front panel commands such as start, stop, reset, and continue into the third or "function" register.

Data transfer is accomplished using the direct-memory-access (DMA) technique on a cycle-stealing basis. A set of DMA registers accommodate data transfers in either direction between host and array processor, with either machine controlling the transfer.

Separate registers are provided for host memory addresses and arithmetic-processor memory addresses. The word count register keeps track of the number of data words transferred, while the direction of data transfer is governed by the control register. The actual data transfer is accomplished through the format register, a DMA register that converts data from the floating-point format of the host into the 38-bit floating-point format of the arithmetic processor on the fly. Control of this double-buffered 38-bit register is handled by 4 bits in the control register. Since there are many floating-point formats in use, the exact details of the format register are determined by the host chosen.

Although most input/output operations are handled by the host, a direct interface between the FPS-100 and the outside world is sometimes required. This is handled by disk-drive subsystems available separately or the I/O processors, which will be discussed later.

Implementation tradeoffs

The choice of a semiconductor family for implementing the arithmetic processor is based on a four-way tradeoff between speed, power consumption, reliability, and package size requirements. To reduce the amount of power needed, low-power Schottky TTL is used predominately in the design except for the MOS memory and logic areas where speed is an overriding concern. Although this allows a 250-ns machine cycle time, it is still as much as one third slower than the previous models, which use standard Schottky logic.

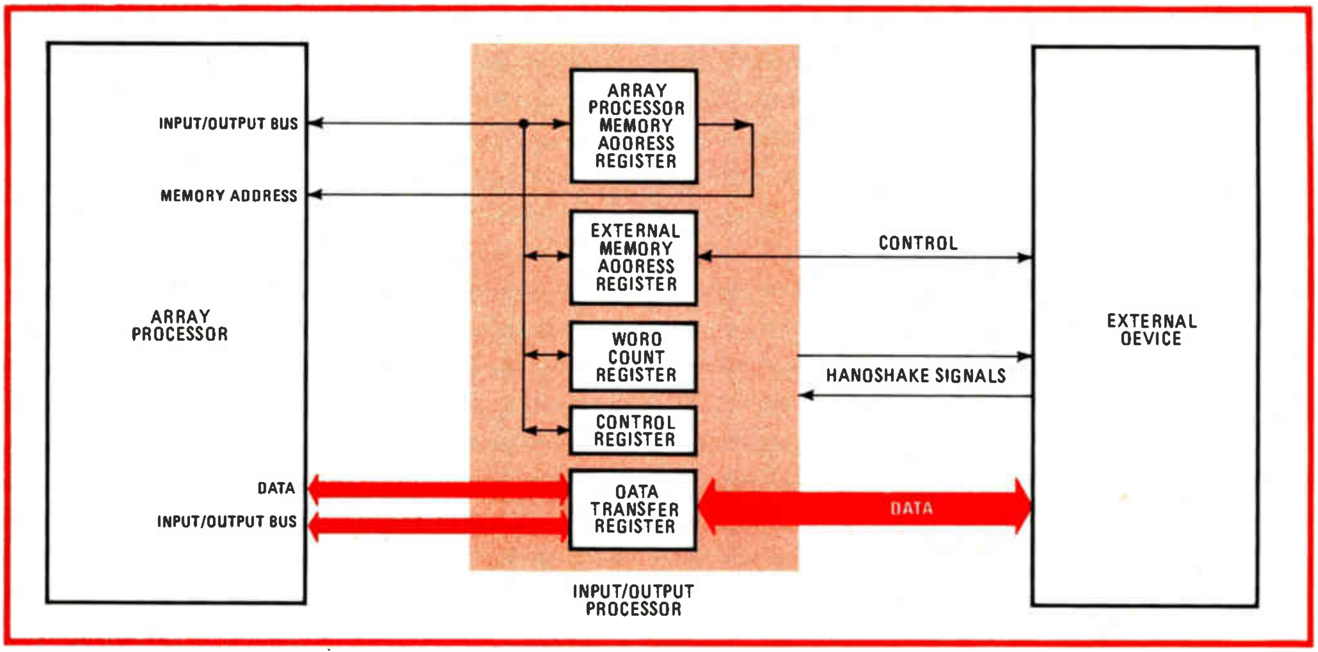
For some functions, such as the 38-bit floating-point multiplier, use of standard medium-scale integrated circuits results in a large chip count. This chip count combined with the substantial number of interconnections involved would increase packaging space. Instead, the MPY-16, a large-scale integrated circuit recently introduced by TRW, is used for the mantissa hardware of the multiplier, reducing package count from 112 to 24.

The MPY-16 multiplier chip is capable of taking a 16-bit multiplicand and a 16-bit multiplier and producing a 32-bit product. Since the mantissa of the FPS-100 contains 28 bits, a single MPY-16 is not sufficient. Each mantissa must, therefore, be divided into a high-order and a low-order set of bits. Since the multiplication of these divided mantissas results in four subproducts (Fig. 3), four MPY-16s are required for the operations to proceed in parallel. The four 32-bit subproducts are in turn each divided into the 16 high-order and 16 low-order bits and added as shown in the figure. The result is deposited in a 64-bit register; convergent rounding returns the product to a 28-bit format.

The four MPY-16s are actually capable of handling a 32-bit-by-32-bit multiplication. Since only 28-bit-by-28-bit multiplication is required, the 4 high-order bits on the inputs to two of the units are simply held at zero.

The total hardware required to arrive at the 64-bit product is now the 2-by-2 array of MPY-16s plus twenty adders for a total of 24 chips. Before the MPY-16, two 7-by-7 arrays of 4-bit-by-2-bit multipliers plus fourteen 4-bit adders were required, a total of 112 chips.

Another example of use of state-of-the-art LSI occurs



4. Intelligent I/O. Interfacing with fixed-protocol devices such as cathode-ray-tube terminals is done by the input/output processor (IOP). One set of registers provides for address conversion and control of the peripheral device, while the second handles data transfer.

in main data memory. As mentioned, the 38-bit main data memory may consist of 8, 16, 32, or 64 kilowords. It is desirable to fit the entire memory on one printed-circuit card to minimize packaging space. Using 16-K memory chips it is possible to put the 32-kiloword main memory—some 152 kilobytes—onto a single 10-by-15-inch board.

For the complete 64 kilowords, however, 128 packages would be required—more than a little unwieldy for a single card of reasonable size. To supply 64 kilowords without resorting to two boards, a dual-16-K memory package is used, supplying 32-K bits per package without increasing package size or pin count.

Packaging

The FPS-100 comes in a 19-inch-wide rack mountable chassis 10.5 inches high and 24.4 inches deep. Fifteen circuit-board slots accommodate the entire machine, including the floating-point arithmetic unit, the integer controller, all memories, the real-time hardware, the host-computer interface, and one I/O processor. Additional I/O processors and programmable I/O processors, if needed, are housed in an I/O expansion chassis. The power supply housed in the main chassis supplies 5 and 12 volts to power both chassis.

Cooling is provided by a push-pull system using separate input and output fans. In the event of a fan failure, either fan alone can provide adequate cooling air. As a further precaution, a thermal sensor triggers power disconnection should there be an excessive heat rise.

Serviceability is enhanced by a hinged power supply that swings out to reveal the printed backplane interconnecting the circuit boards. Printed boards can be pulled out of their zero-insertion-force connectors without removing the arithmetic processor from the rack.

To facilitate the system designer's task, ways must be found to minimize programming time and complexity while retaining the high throughput potential of the arithmetic processor. At the same time, software flexibility is desirable to allow the system designer to balance programming complexity against coding efficiency and throughput for a given application.

Programming methods

The easiest programming method on the FPS-100 is the Fortran call approach. A program is written for the host consisting of a series of Fortran call statements from the host to the arithmetic processor. Each call then initiates a standard manufacturer-written subroutine already stored in the arithmetic processor.

A Fortran cross compiler for the FPS-100 allows the system designer the convenience of generating his custom programs in that higher-level language. The compiler, which resides in the host, automatically converts the program into parallel instructions in the arithmetic processor's own language. This eliminates the need for parallel assembly-language programming of the subdivided 64-bit instruction word and provides a satisfactory level of coding efficiency for most applications.

Where the ultimate in throughput is required, careful parallel coding in assembly language allows maximum use of the machine's capabilities. Software pipelining can often be implemented more efficiently by a human programmer than by the automatic Fortran compiler.

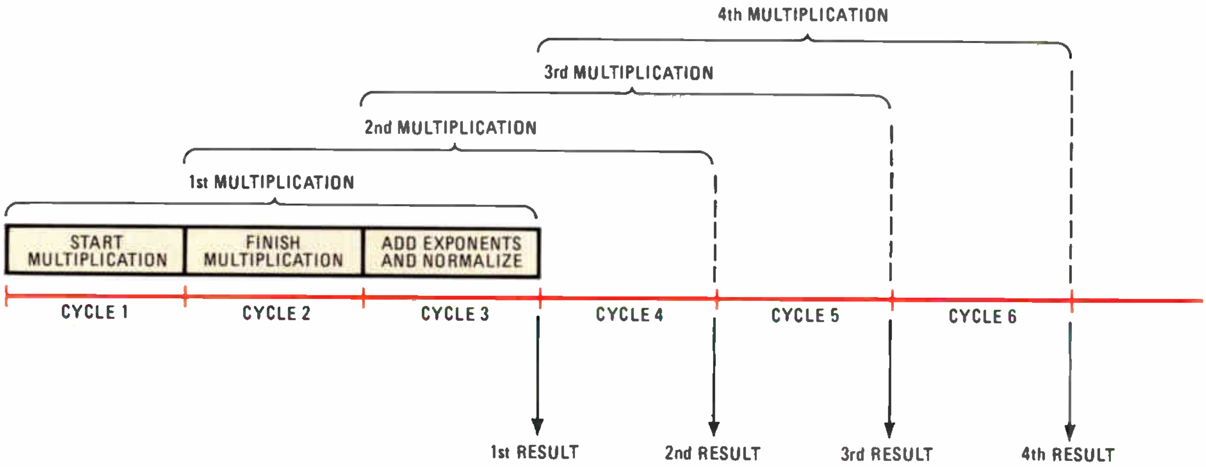
When preparing programs for an arithmetic processor, the differences between synchronous and asynchronous hardware architectures become apparent. As has been seen, array processors derive much of their high throughput from parallel hardware elements. Asynchronous designs offer a potential speed advantage since each of the parallel elements can operate at its own maximum speed, unconstrained by a common system clock cycle. Offsetting this advantage, however, is the necessity to write coordinated parallel programs for each of the

Pumping a full pipeline

In the operation of an oil pipeline, a second shipment is started down the line just after the last drops of the preceding shipment have entered the line; it would make no sense to wait until all of the first shipment had arrived at its destination, leaving the pipe empty. Similarly, hardware pipelining is a widely used technique for speeding up a computer by performing operations concurrently.

For example, a floating-point multiplication has three stages, each of which takes a machine cycle to complete. The product of the mantissas of the two operands starts in the first stage and is completed in the second stage, while the exponents of the two operands are added and any normalization and rounding of the product is performed during the third stage.

By pipelining, or staggering and overlapping, the sequential operations of many multiplications, the speed of the multiplier hardware is improved. As seen in the figure, although there is a delay of three machine cycles before the completion of the first multiplication, once the pipelining begins, a new result emerges each cycle.



asynchronous sections. In addition, the number of states in an asynchronous machine is indeterminate, making it impossible to write an exact simulator for debugging programs outside the machine.

Choosing appropriate parallel hardware elements and a clock cycle close to that of the fastest element, synchronous designs can provide throughputs equivalent to those of asynchronous designs in most applications. But the synchronous array processor is more easily programmed since there are no independent functions to coordinate. An exact simulator can also be written for a synchronous machine, since it has a fixed number of states. This makes it possible to develop software concurrently with machine hardware development and therefore to offer applications software such as math libraries at the same time as the hardware announcement.

Software support offered with the FPS-100 for speeding system design and reducing design costs includes special libraries of mathematical routines for signal and image processing, an interactive debugger, diagnostic routines, a linking loader, and programming aids for the I/O processors.

Real-time capability

While not all applications of arithmetic processors require real-time capability, the number of those that do make availability of such capability important. The real-time operating system software and hardware optionally available for the FPS-100 set it apart from the other models in the line.

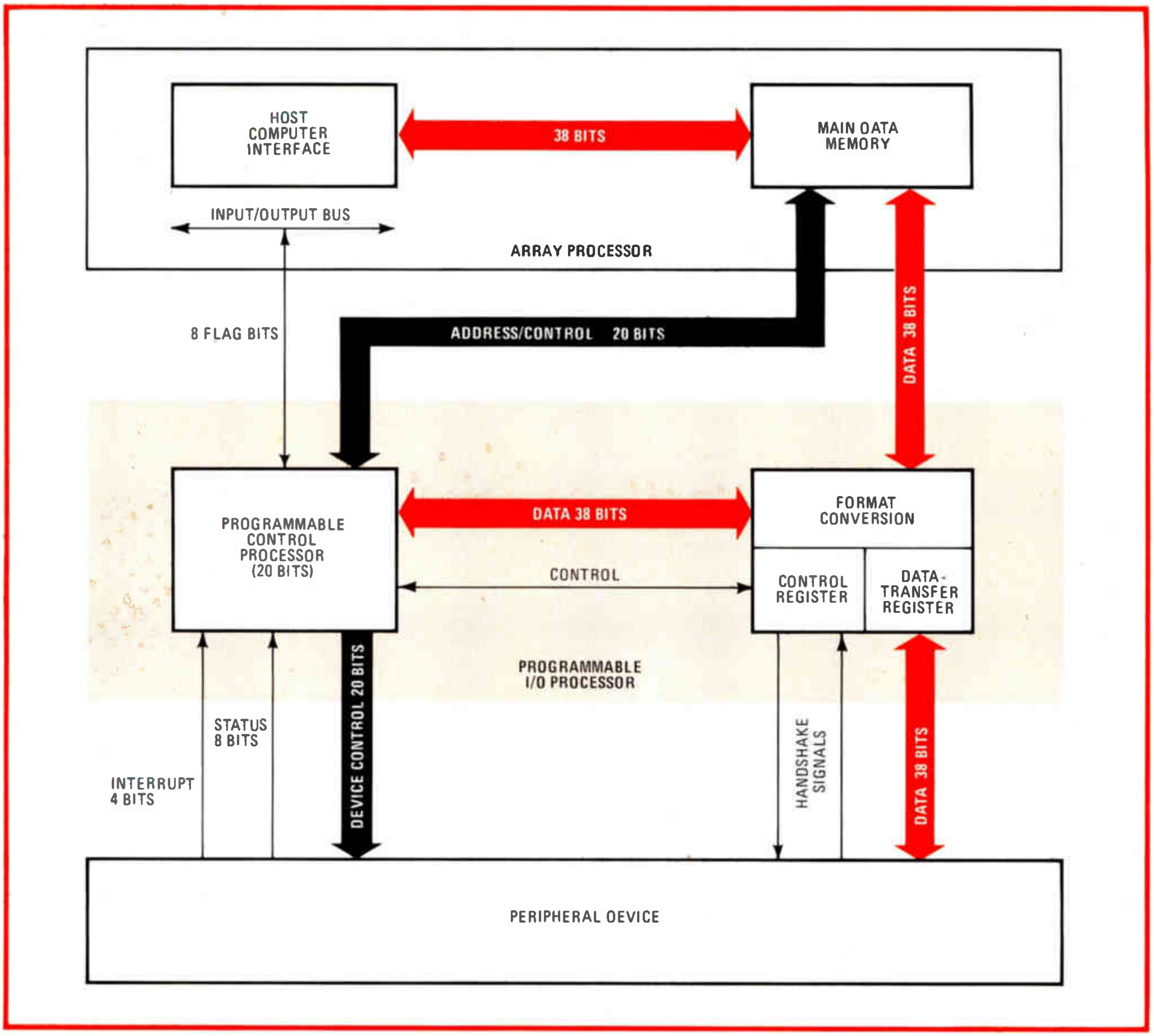
Central to the machine's real-time capabilities is the Super 100 real-time supervisor. In addition to supporting real-time applications, this resident operating system enables the FPS-100 to operate independently of the host computer for extended periods. Programs covering several computational tasks can be transferred from the host to the arithmetic processor at one time. When the programs are finished running, the results are stored in the arithmetic processor. Only when all tasks are completed does the arithmetic processor need to report back to the host.

To support real-time operation, the Super 100 supervisor works in concert with the real-time clock and the machine's interrupt structure. These features not only allow synchronizing the arithmetic processor with an external process, they also allow the machine to act as a system control clock.

The real-time clock is an up/down counter with a floating-point format. A 4-bit exponent allows selection of 1 of 16 counting rates ranging from 1 MHz to 60 Hz (1-microsecond to 16-millisecond resolution). Counting takes place in a 16-bit mantissa. The 4-bit rate selection register may also be disabled and the clock synchronized to an external source.

As a simple illustration of operation, a signal from an outside process could initiate an interval count in the clock. At the end of the interval the clock would interrupt the arithmetic processor so that computation on data from the outside process could be performed. Or the real-time clock might be used in asking for samples of data from the external process at regular intervals.

The priority interrupt structure is divided into three



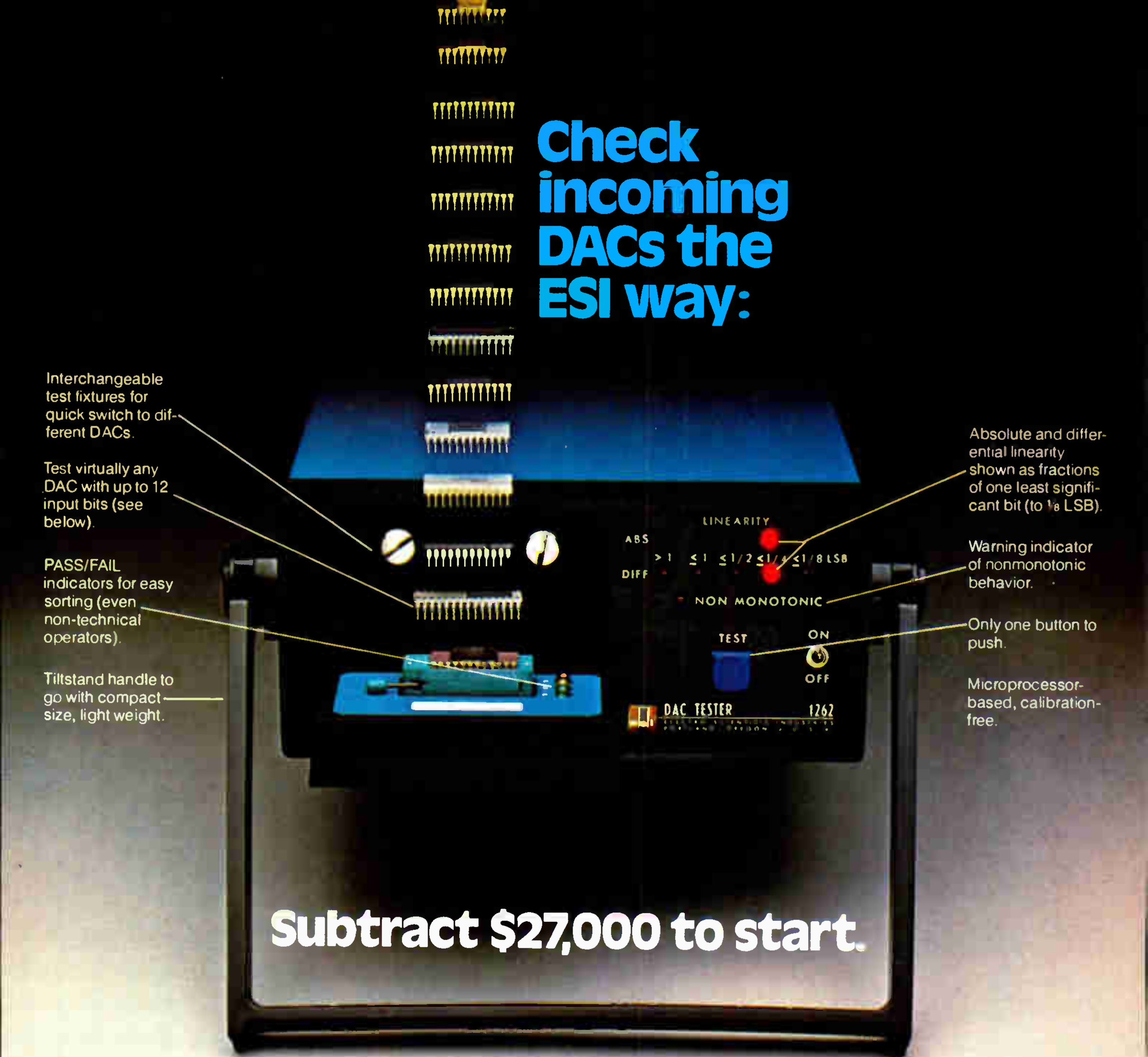
5. General-purpose. Because of its programmability, the general-purpose input/output processor (GPIOP) can control a variety of more complex external devices. Choice of source and destination within the array processor and data formatting are under program control.

internal priority levels and one external level. The first three interrupt levels are involved with internal control of the arithmetic processor. The fourth level of the interrupt is of more interest to the system designer because it allows the outside world to interrupt the processor. This level is subdivided into 15 priority sublevels. The highest priority in this sublevel interrupt structure is assigned to the real-time clock so that computations associated with a real-time process will always be performed first.

Priority sublevels 2 and 3 are typically assigned to requests from the host computer to perform additional calculations that are not in real time. In this way the arithmetic processor can be operated in the multitasking mode. Sublevels 4 through 15 are assigned to service requests from I/O devices attached directly to the arithmetic processor.

Interface between the FPS-100 and an external real-time process is accomplished through one of two I/O processor types. These I/O processors are not restricted to real-time applications, and can also be used whenever there is a need for a direct interface between the arithmetic processor and an external device. Functions of the I/O processors include control of the external device and data transfer.

The first type of I/O processor, called the IOP (Fig. 4), is designed to interface fixed-protocol devices such as cathode-ray-tube terminals. The interfacing procedure does not vary for such devices and address control is limited to a fixed set of algorithms; the data-transfer format is also fixed. For interfacing variable-protocol peripheral devices, the programmable general-purpose I/O processor (GPIOP, Fig. 5) is used. A microprocessor included in the GPIOP permits programmable addressing of the data source and data destination in the arithmetic processor and the external device. It also provides programmable data formatting and control of more complex external devices. □



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E-PROM doubles bit density without adding a pin

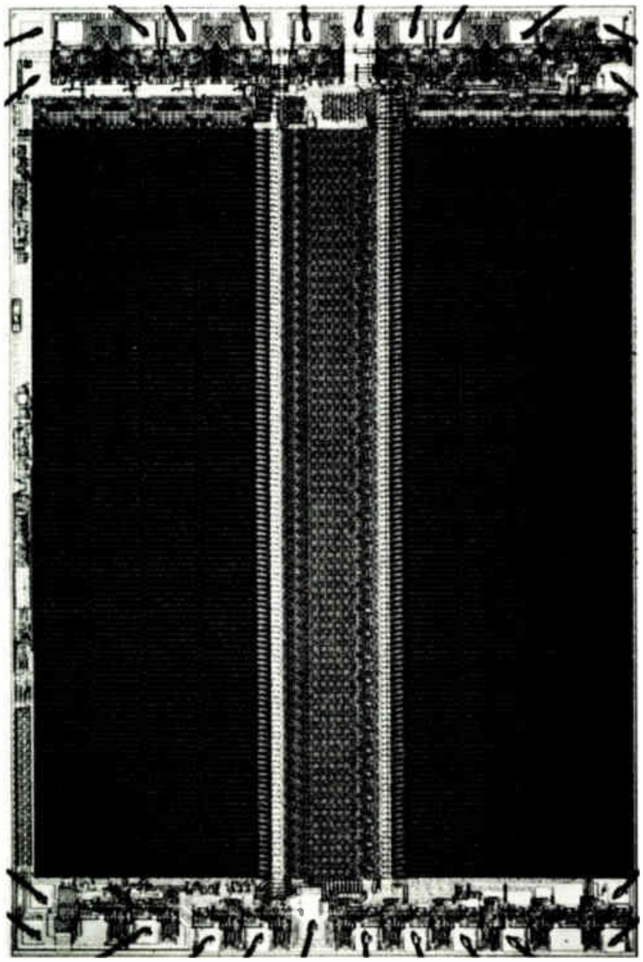
Multiplexing makes room for the extra address bit, keeping the 32-K memory compatible with 16-K devices and 64-K ROMs

by Bob Greene and Frank Louie, *Intel Corp., Santa Clara, Calif.*

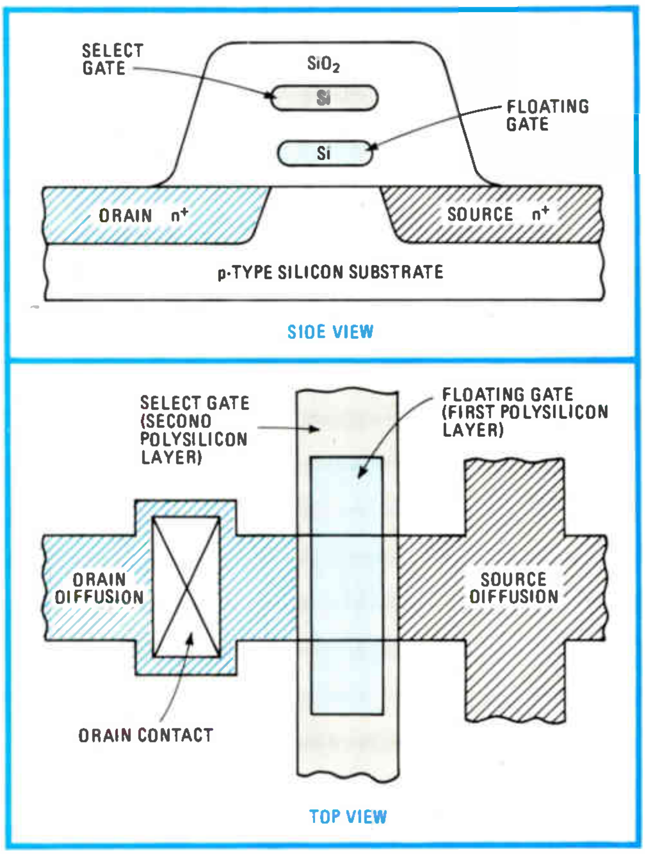
□ Given the inevitability with which memory chips increase in density, no crystal ball was needed to foretell the arrival of a 32-K enhancement of the widely used 16-K erasable programmable read-only memory. Much less predictable, however, was how the new device would be packaged. The only certainty here was that compatibility with the 16-K package would be optimized, to make it easy for designers to upgrade their memory systems with the denser chip.

But this requirement presented a real challenge. The 16-K 2716 E-PROM uses all of its 24 pins, so where was the 32-K 2732 to find the extra one needed for the extra address bit that its doubled memory size required? It makes the extra room by combining two 2716 functions on a single pin.

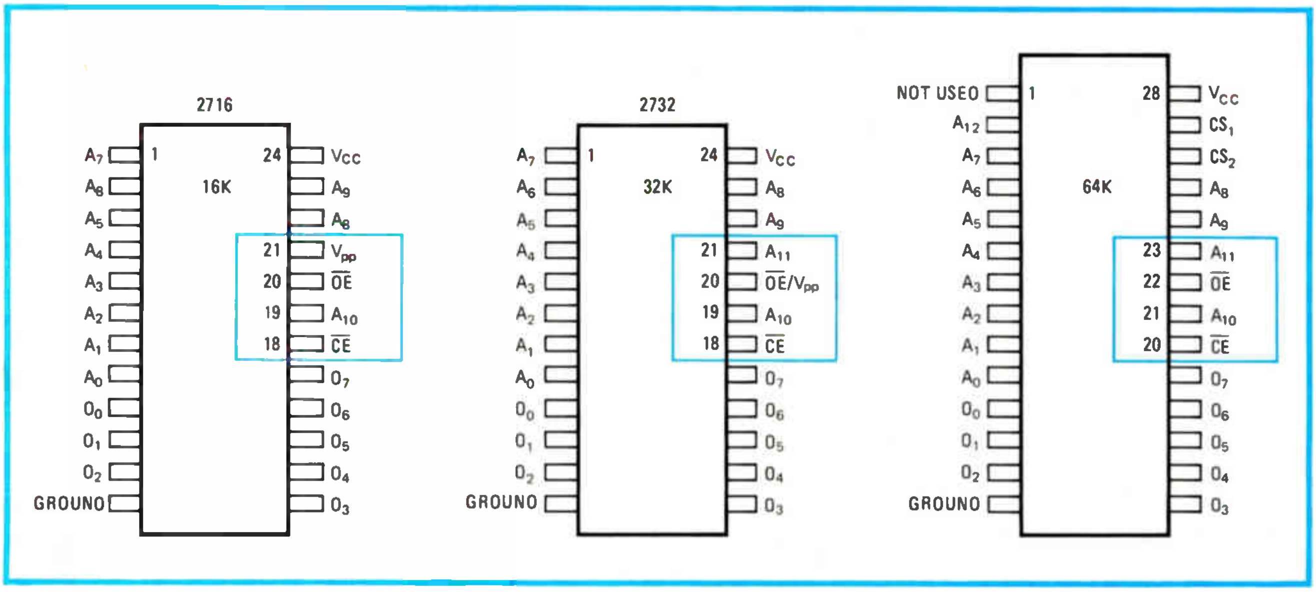
The final 2732 package truly meets the compatibility requirement. It can be used to build a memory board that is flexible enough to allow any mix of the read-only memory chips while affording a clear-cut modularity



1. Four kilobytes of E-PROM. The 2732 erasable programmable read-only memory packs 32,768 bits into a chip measuring less than 40,000 mil², an area that is only 30% larger than the earlier 16-k 2716 memory chip. Placing all the bonding pads at two ends of the die, rather than around the whole perimeter, also helps boost density.



2. Tighter cell. The 2732 uses the same basic double-polysilicon stacked-gate MOS cell as its 16-K forerunner, although the 32-K chip is only 30% larger. Greater density of the new E-PROM derives from improvements in layout and photolithographic techniques.



3. New pinout. To accommodate the extra address bit (A_{11}), the 2732 multiplexes the output-enable ($\overline{OE}$) with the programming-voltage input (V_{pp}) on pin 20. Compatibility is assured with next-generation 64-K E-PROM, which will be housed in a 28-pin package.

scheme for varying the page sizes and boundaries within a memory system.

The 2732 puts 32,768 bits of ultraviolet-light-erasable programmable memory on a chip less than 40,000 square mils in area (Fig. 1). It therefore packs twice the bits of the 2716 onto a chip only 30% larger. One reason is that all the bonding pads are on two opposing sides of the die, rather than around its entire periphery, as on the 2716. The advantage is an increase in the relative density of many of the circuits peripheral to the chip's actual memory array that would not be possible were those buffers and control circuits strung out around the chip perimeter.

In addition, improvements in circuit layout and photo-lithography have contracted the size of the die, even though the 32-K part is fabricated with the same two-level polysilicon stacked-gate MOS process as the 2716. In essence, the 2732 uses the same basic cell as the 2716 (Fig. 2).

The power dissipation of the 2732, which operates with a single +5-volt supply, is a maximum of 750 milliwatts—50% more power than the 2716. Like the 2716, however, the chip goes automatically into a stand-by mode when not selected, reducing its dissipation to the much lower value of 150 mW. That arrangement saves 80% of the power while not degrading system speed in the least—the access time of the device is 450 nanoseconds in the worst case.

Enter multiplexing

For compatibility with the 16-K E-PROM, the 2732 maintains the same two control lines: an output-enable input ($\overline{OE}$), which independently controls the chip's three-state output buffers, and a chip-enable input ($\overline{CE}$), which selects the device and provides the automatic power-down feature.

So that the 2732 would fit into the same 24-pin package as the 16-K E-PROM, the new twelfth address bit (A_{11}) is given the programming-voltage supply (V_{pp}) pin, while V_{pp} and $\overline{OE}$ are now multiplexed to share a single pin, as shown in Fig. 3. The multiplexing relies on a voltage-dependence scheme that is transparent to the user operating the chip in its normal read mode (see "New circuit for an E-PROM," p. 128).

System applications

With the new pin arrangement, an extremely flexible memory system can be planned around 28-pin package sites that allows the page size—the number of bytes per site—to change easily from 1 kilobyte to 8 kilobytes. (Although the largest increment, a 65,536-bit device, is available now only as masked ROM, the 64-K E-PROM will soon join the family.)

The 2732, with a 4-kilobyte capacity, is well suited to many microprocessor program-storage applications. Perhaps more important, the 2732 design and pinout allow a new degree of modularity with respect to system page size—the universal-board concept is closer than ever, for page sizes of 1, 2, 4, and 8 kilobytes can be designed into a system, and when the system is configured at the time of card assembly, the correct ROM or E-PROM can be inserted in the sockets provided. Moreover, the output- and chip-enable lines completely eliminate bus contention and keep the system operating at a minimum power dissipation.

Architecture for a flexible board

While it is generally true that the average ratio of read-only to read/write memory in a microprocessor-based system ranges from 3:1 to 5:1, systems often are of necessity committed to a hardware design well before the exact amount of RAM and ROM required has been established. But with a little advance planning, it is possible to execute a scheme that permits page size to vary by allowing the ratio of RAM to ROM to be decided after the hardware is built.

The key to such an architecture is a fuse-link-programmable ROM for address decoding. All that is needed

New circuit for an E-PROM

The basic repertoire of circuits used in the 2732 was developed for the 2716 erasable programmable read-only memory, including address buffers, decoders, sense amplifiers, data-input and -output buffers, and programming circuits. For the larger E-PROM, however, one new circuit had to be developed—a multiplexer that allows pin 20 to function as both the output-enable ($\overline{OE}$) input and the programming-voltage supply (V_{pp}) pin. Despite the necessary change, close compatibility with the 2716 was desired; thus the basic timing specifications had to be duplicated into the 2732.

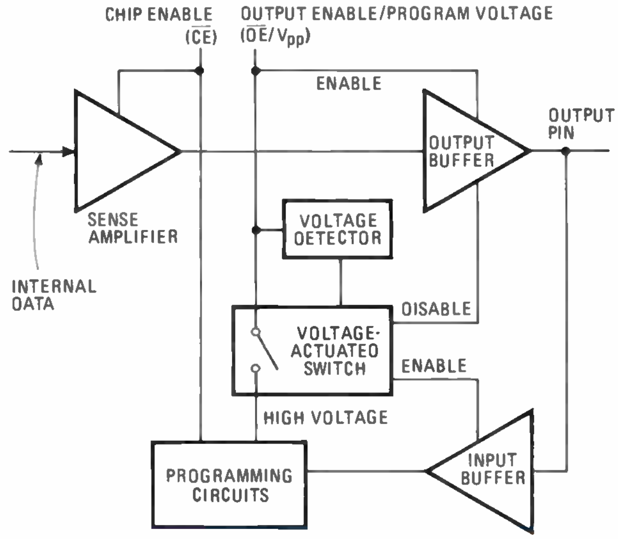
During the read mode, pin 20 functions as the same output-enable on the 2716: when the 2732 is selected by a signal that drives its chip-enable ($\overline{CE}$) input low, and the addresses at its inputs are stable, $\overline{OE}$ independently controls the device's three-state output buffers.

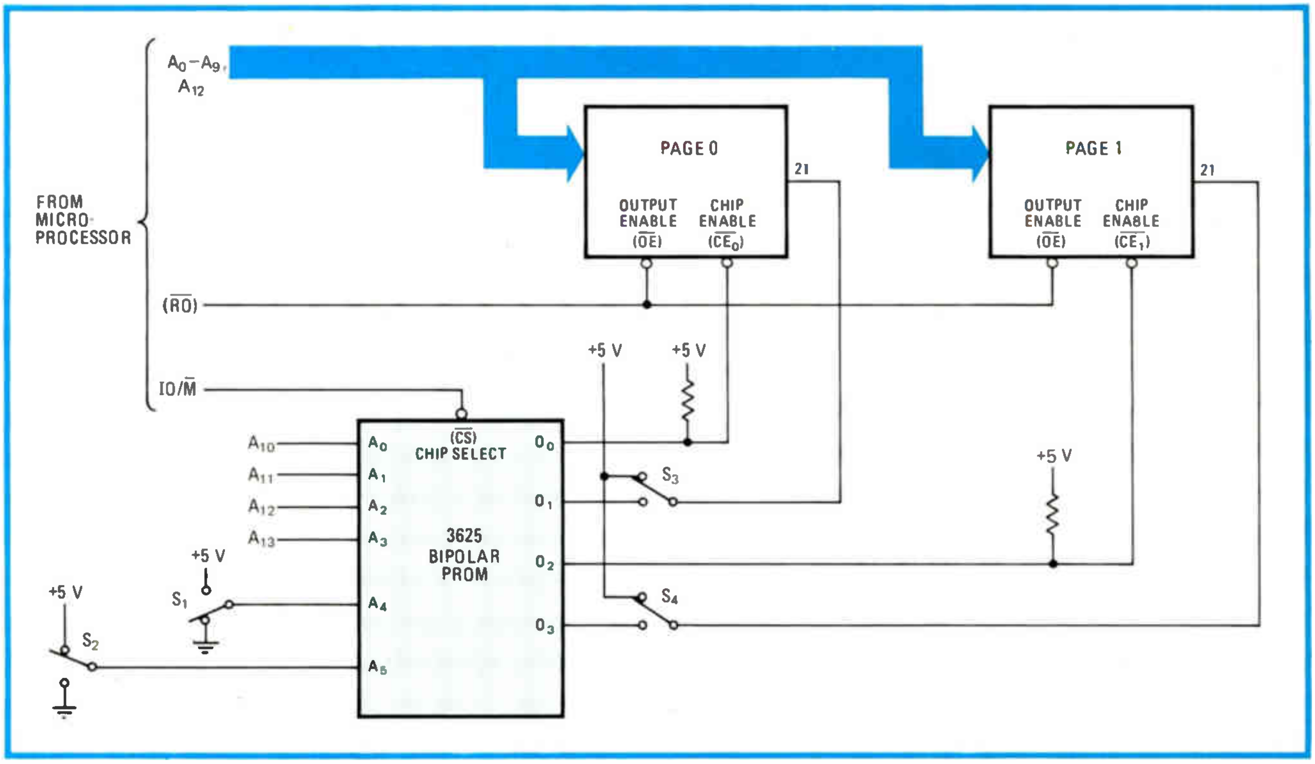
In the programming mode, however, pin 20 receives the +25-volt programming source. It was decided that the mere presence of that high voltage would switch the 2732 into the programming mode, which requires reversing the data outputs so that they become inputs, and switching the function of the chip-enable input to that of a programming-enable input.

The problem was in keeping the switch to the programming mode transparent to the chip's normal read operation. The solution for pin 20 was the voltage-activated switch whose circuit is diagrammed in the figure.

When a high voltage (V_{pp}) is detected at the pin, the output buffer is disabled and the programming-input buffer enabled, thereby turning the data outputs around so that they become inputs. The switch also allows that pin 20 become the source of the relatively high programming power. At the same time, application of that power to the array becomes the job of the chip-enable ($\overline{CE}$) pin, which applies V_{pp} to the appropriate column in the memory array.

Programming a byte into the 2732, as in the 2716, requires the application of a single TTL-level pulse of 50 milliseconds' duration to the $\overline{CE}$ input. Whereas the 2716 requires an active-low signal, however, the 2732 reverses the requirement to an active-high pulse. The advantage here is that memory systems can more easily accommodate in-system programming of the E-PROMs.





4. Variable-density pages. The key to a flexible memory board with variable page size—the number of bytes per socket—is a fuse-link PROM for decoding. Adding dual in-line switches lets page sizes and boundaries be set in the field after software is finalized.

TABLE 1: ADDRESS MEMORY MAP

	Page boundary for 1-kilobyte page	Page boundary for 2-kilobytes page	Page boundary for 4-kilobyte page	Page boundary for 8-kilobyte page		
	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}
64-K ⋮						
16-K	0	0	0	0	1	0
15-K	1	1	1	1	0	0
14-K	0	1	1	1	0	0
13-K	1	0	1	1	0	0
12-K	0	0	1	1	0	0
11-K	1	1	0	1	0	0
10-K	0	1	0	1	0	0
9-K	1	0	0	1	0	0
8-K	0	0	0	1	0	0
7-K	1	1	1	0	0	0
6-K	0	1	1	0	0	0
5-K	1	0	1	0	0	0
4-K	0	0	1	0	0	0
3-K	1	1	0	0	0	0
2-K	0	1	0	0	0	0
1-K	1	0	0	0	0	0

TABLE 2: PROGRAM OF DECODER PROGRAMMABLE READ-ONLY MEMORY

System address			A_{13}	A_{12}	A_{11}	A_{10}	CE_0	Pin 21	CE_1	Pin 21
Decoder programmable read-only memory	A_5	A_4	A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3
1 kilobyte/page	0	0	0	0	0	0	0	X	1	X
	0	0	0	0	0	1	1	X	0	X
2 kilobytes/page	1	0	0	0	0	0	0	X	1	X
	1	0	0	0	0	1	0	X	1	X
	1	0	0	0	1	0	1	X	0	X
	1	0	0	0	1	1	1	X	0	X
4 kilobytes/page	0	1	0	0	0	0	0	0	1	0
	0	1	0	0	0	1	0	0	1	0
	0	1	0	0	1	0	0	1	1	1
	0	1	0	0	1	1	0	1	1	1
	0	1	0	1	0	0	1	0	0	0
	0	1	0	1	0	1	1	0	0	0
	0	1	0	1	1	0	1	1	0	1
	0	1	0	1	1	1	1	1	0	1
8 kilobytes/page	1	1	0	0	0	0	0	0	1	0
	1	1	0	0	0	1	0	0	1	0
	1	1	0	0	1	0	0	1	1	1
	1	1	0	0	1	1	0	1	1	1
	1	1	0	1	0	0	0	0	1	0
	1	1	0	1	0	1	0	0	1	0
	1	1	0	1	1	0	0	1	1	1
	1	1	0	1	1	1	0	1	1	1
	1	1	1	0	0	0	1	0	0	0
	1	1	1	0	0	1	1	0	0	0
	1	1	1	0	1	0	1	1	0	1
	1	1	1	0	1	1	1	1	0	1
	1	1	1	1	0	0	1	0	0	0
	1	1	1	1	0	1	1	0	0	0
	1	1	1	1	1	0	1	1	0	1
	1	1	1	1	1	1	1	1	0	1

Note: All unused decoder PROM address inputs should be tied to ground. X = V_{CC} via switch S_3 or S_4.

for a basic system is a four-output PROM, such as a 3625 bipolar device. (A 1,024-by-4-bit device is used in this case; it is large enough to accommodate a universal coding scheme with many more combinations of page sizes and boundaries.)

As shown in the simplified two-page example of Fig. 4, the 10 least significant address bits (A_0–A_9, which address a 1-kilobyte space) are passed through the system and connect directly to pin addresses A_0–A_9 at all the memory sites. Bits A_{10}–A_{13} go to the PROM's least significant address inputs A_0–A_3. (In this example only a 16-kilobyte space is addressed; no use is made of the most significant address bits A_{14} and A_{15} that reach the 64-K byte address space found in most microprocessors.)

For an 8085 or 8086 microprocessor, the IO/$\overline{\text{M}}$pin, which determines whether the processor reads from the input/output lines or from memory, connects to the chip-select input ($\overline{\text{CS}}$) of the PROM. The microprocessor's read ($\overline{\text{RD}}$) signal (or the MRDC signal on an 8288 bus-controller used in conjunction with an 8086) drives the $\overline{\text{OE}}$ signals of all the memories in the system.

Table 1 shows the address-memory map for determining the page sizes and boundaries, which are fixed by the PROM. Note that the system address bit that controls the page boundary changes as the page size is changed. For the 4-kilobyte 2732, for example, system address bit A_{12} determines the page boundary, while if a 2-kilobyte 2716 were used, system address bit A_{11} would determine the boundary. (It is important in using 2716s to remember that pin 21 must be tied to +5 V.) In a similar manner, if 8-kilobyte 64-K ROMs or E-PROMs were used, system address bit A_{13} would determine the page boundary.

Coding the PROM

The PROM is coded so that its address bits A_4 and A_5 select the page size, which is determined in this case by switches S_1 and S_2. The switching scheme is as follows: for a 1-kilobyte page, A_4 and A_5 are both 0; for a 2-kilobyte page, they are 0 and 1, respectively; for a 4-kilobyte page, they are 1 and 0; and for an 8-kilobyte page, both A_4 and A_5 are 1.

The entire code for the 3625 is shown in Table 2. By utilizing additional switches and inputs to the PROM, the various combinations of page size can be provided. If desired, a universal code may be developed so that one PROM may accommodate any changes in page size. Ultimately, the unused address bits of the PROM could be utilized to allow the various page sizes to be assigned anywhere on the memory map, and single-pole, double-throw switches (the dual in-line package type) could allow the page configuration to be changed in the field to suit the software. □

Dual light-emitting diode synthesizes polychromatic light

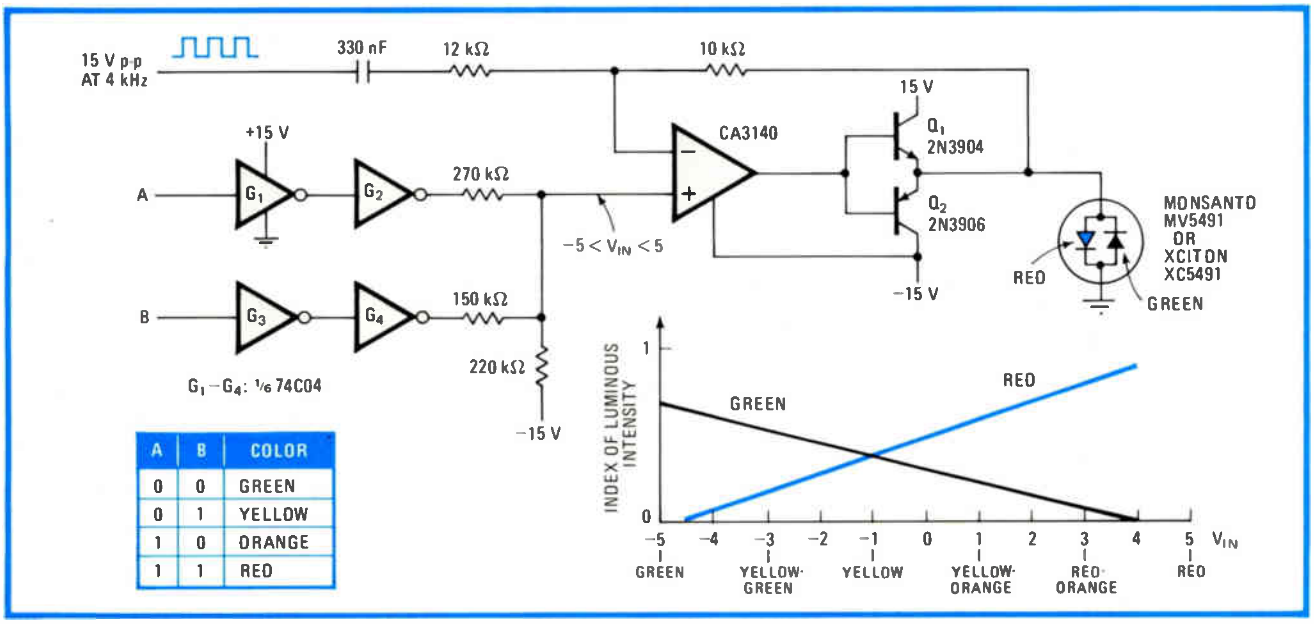
by Leonard M. Smithline
Ithaca, N. Y.

By controlling the drive to each element of a dual red or green light-emitting diode so as to mix the red and green lights in varying quantities, this digital circuit synthesizes four distinct hues from the two primary optical colors. With a slight modification, it can also make the diode vary gradually from green through yellow and orange to red in response to an analog input.

The LED used here may be either the Monsanto MV5491 or the Xciton XC5491 (Fig. 1). The diodes inside either device are wired back to back and so cannot be driven simultaneously. They therefore need a multiplexer circuit to drive them at a fast enough rate for them to appear to be on simultaneously. Here a 4-kilohertz square wave provides the desired chopping action. The relative proportions of drive to the green or red LED are controlled by adding a dc bias to the square-wave drive at the noninverting input of the CA3140 operational amplifier, as shown.

Thus, the states of A and B determine the color perceived by the mixing process, as seen in the table. Alternatively, an analog signal can be applied to the noninverting input of the op amp, whereupon the circuit response will be as shown in the graph.

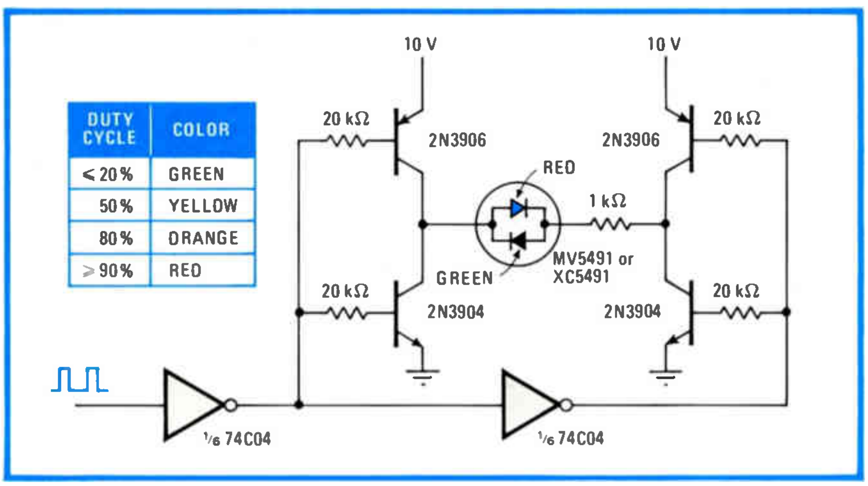
For a thorough mixing of colors, the primary light sources should not only be viewed simultaneously (as



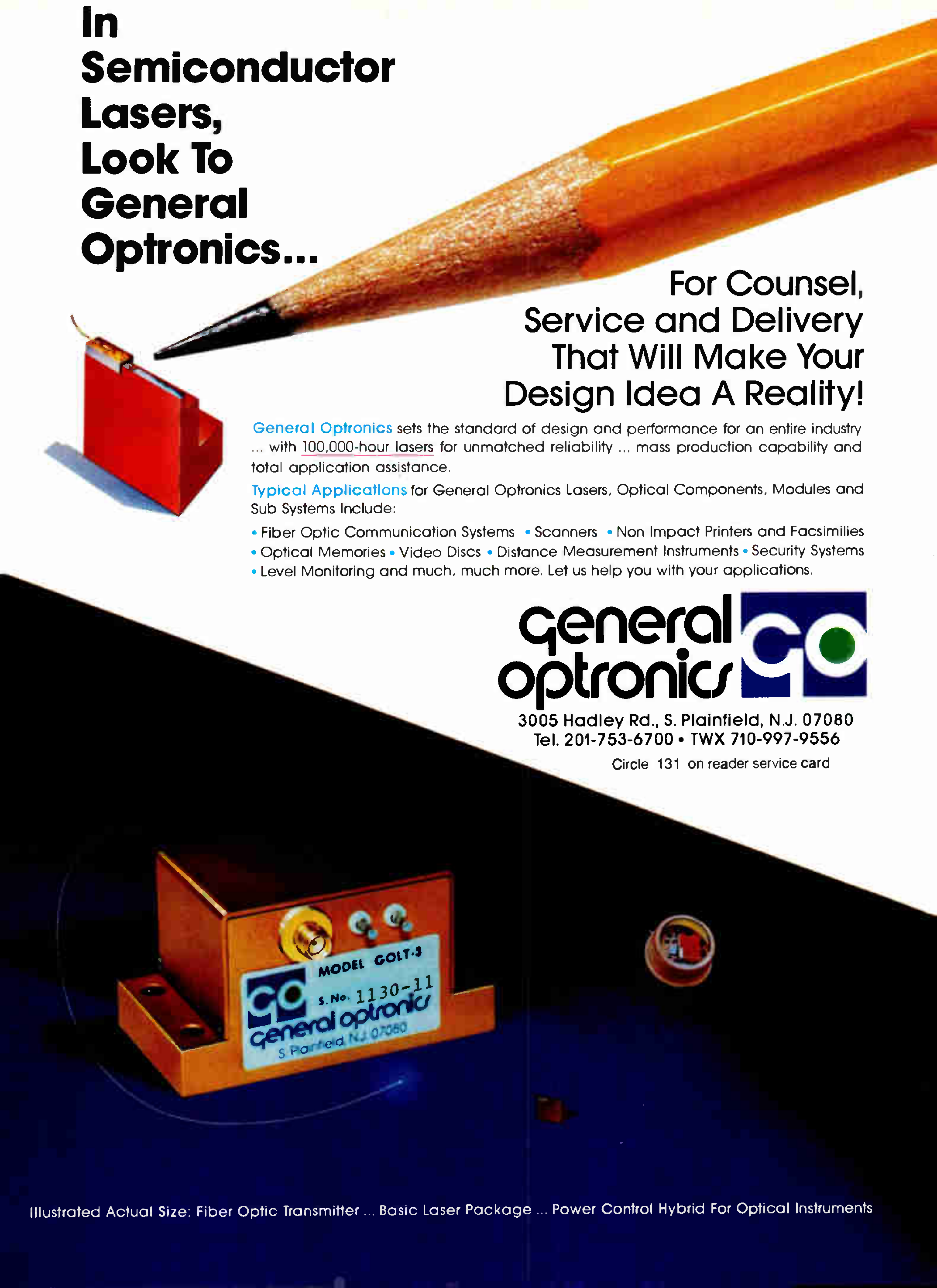
A	B	COLOR
0	0	GREEN
0	1	YELLOW
1	0	ORANGE
1	1	RED

1. Thoughts of hue. Multiplexer's 4-kHz square wave, suitably offset with dc bias controlled by states of A and B, provides desired drive to each element of green/red photodiode for deriving perceived four-color output. Alternatively, analog signal may be applied to noninverting input of op amp for effecting gradual change in color, from green through red. Circuit response in either case is given in table and graph.

2. Color cycle. Generation of yellow and orange from red and green light may also be achieved through control of duty cycle of pulses driving light-emitting diodes. Pulse-width modulation requires only single supply.



DUTY CYCLE	COLOR
≤ 20 %	GREEN
50 %	YELLOW
80 %	ORANGE
≥ 90 %	RED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they virtually are in this case) but ought also to overlap one another homogeneously. The concept is an old one and was first used widely in color television. (Note that the colors produced in this way are only products of the human visual system, and no objectively new optical wavelengths are actually generated.)

In fact, the sources in the MV5491 or XC5491 are in close enough physical proximity, but differences in the patterns of radiation of the two LEDs will prevent the color mixing from being entirely uniform, giving rise to unwanted tinges of color. This situation may be ameliorated either by roughening the lens slightly to increase the diffusion of light or by limiting the angle of view. Incidentally, the Xciton XC5491 has better uniformity of field than the Monsanto device, but the MV5491 has a decidedly better appearance in the red region.

As an alternative way of synthesizing colors the duty cycle of the pulses driving each LED may be changed as shown in Fig. 2. This circuit has the advantage of requiring only a single supply. □

12-hour clock tells time out loud

by William S. Wagner
Northern Kentucky University, Highland Heights, Kentucky

Combining a program written for the 6800 microprocessor and a four-chip interface, this system expresses clock time as an equivalent sequence of audio tones. Like the audio voltmeter previously described,[1] it allows determination of time when the clock face cannot be seen.

In this method, the exact time—expressed as xxyy, where xx denotes hours and yy denotes minutes—is converted to a series of tones of short duration (dits) to represent quantities extending from 1 to 9. The quantity 0 is represented by a single tone (dah) of a relatively long duration. A long pause separates hours from minutes. Thus, for example, a time of 02:41 would yield an audio output of dah, pause, dit-dit, long pause, dit-dit-dit-dit, pause, dit.

Three frequency dividers (A_1–A_3), two gates (G_1–G_2), and a few passive components comprise the clock-to-microprocessor interface. The actual clock signal is derived from the highly accurate 60-Hz power line.

A_1 and A_2, each a divide-by-10 chip, and A_3, wired as a divide-by-12 device, produce a pulse with a 20-second period from the line input. This pulse serves as the 6800's hardware interrupt, which initiates the program and the generation of time markers exactly three times every minute. Other intervals can be selected by appropriate action of the divider ratio.

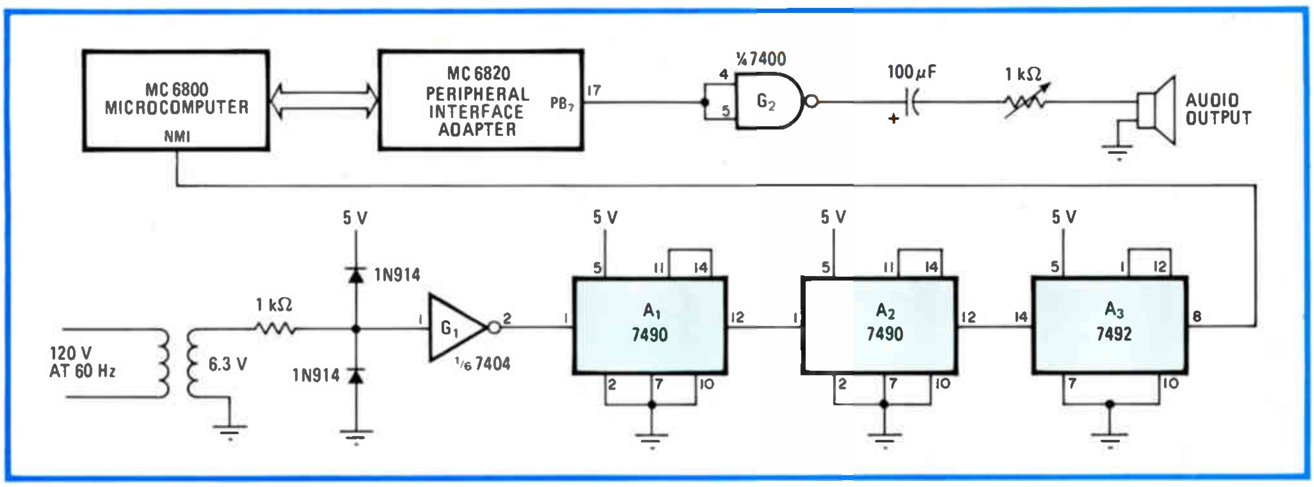
The clock is set to any desired starting time with software, where the initial hour is stored at program address 0002, minutes are stored in 0001, and seconds in 0000. Although seconds are not made audible, they are required in the program for updating the minutes unit once every three sampling periods.

When an interrupt is received, the initial time, expressed in hours and minutes, is converted to a set of four 4-bit binary-coded words in steps 0023–00A0 and is checked to determine if each word represents a 0 or an integer from 1 to 9. At this point the program determines whether short or long tones are to be transmitted. The instructions commencing at 0053 set the time interval between the processing of each individual word and between hours and minutes.

After the clock routine (01A0–01D6) increments the minutes and hours units as necessary, the dit and dah subroutines (at 0100 and 0120, respectively) are initiated. The program then halts and waits for a system interrupt, whereupon the process repeats. □

References
1. William S. Wagner, "Digital voltmeter has audible output," *Electronics*, March 29, 1979, p. 120.

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.



Tick tones. Microprocessor-based chronometer periodically derives audible time markers. System generates a pulse code, with numbers 1 to 9 represented by string of short tones and a zero represented by a long tone. Long pause between digits separates hours from minutes.

6800 PROGRAM FOR AUDIO CLOCK

Address	Mnemonic	Address	Mnemonic	Address	Mnemonic
0000	(STORAGE)	0073	PULA	0134	ASLA
0001	"	0074	ASLA	0135	ASLA
0002	"	0075	PSHA	0136	ASLA
0003	LDX FF04	0076	BCS 17	0137	ASLA
0006	STX 8802	0078	BRA 1A	0138	PSHA
0009	WAI	007A	LDA 08	0139	JMP 0053
000A	BRA FD	007C	JSR 0100	0140	LDX 03FF
0020	STX 0015	007F	BRA E8	0143	ORAB 7F
0023	LDS 00C0	0081	LDA 04	0145	STAB 8002
0026	PSHA	0083	JSR 0100	0148	LDAA 25
0027	ANDA 70	0086	BRA E6	014A	DECA
0029	BGT 03	0088	LDA 02	014B	BNE FD
002B	JMP 0120	008A	JSR 0100	014D	DEX
002E	PULA	008D	BRA E4	014E	BEQ 03
002F	ASLA	008F	LDA 01	0150	COMB
0030	ASLA	0091	JSR 0100	0151	BRA F0
0031	PSHA	0094	LDAA 02	0153	PULA
0032	BCS 0C	0096	LDX FFFF	0154	ASLA
0034	PULA	0099	DEX	0155	ASLA
0035	ASLA	009A	BNE FD	0156	ASLA
0036	PSHA	009C	DECA	0157	ASLA
0037	BCS 0E	009D	BNE F7	0158	PSHA
0039	PULA	009F	PULA	0159	JMP 0094
003A	ASLA	00A0	LDS 10	01A0	LDX 0000
003B	PSHA	00A2	LDX 15	01A3	LDAB 03
003C	BCS 10	00A4	RTS	01A5	SEC
003E	BRA 13	00A5	JMP 0140	01A6	BSR 0E
0040	LDA 04	00FD	JMP 01A0	01A8	LDAB 60
0042	JSR 0100	0100	PSHA	01AA	BSR 0A
0045	BRA ED	0101	LDX 00FF	01AC	LDAB 13
0047	LDA 02	0104	ORAB 7F	01AE	BSR 06
0049	JSR 0100	0106	STA 8002	01B0	BSR 15
004C	BRA EB	0109	LDAA 25	01B2	BSR 13
004E	LDA 01	010B	DECA	01B4	DEX
0050	JSR 0100	010C	BNE FD	01B5	RTI
0053	LDAA 01	010E	DEX	01B6	LDAA 00,X
0055	LDX FFFF	010F	BEQ 03	01B8	ADCA 00
0058	DEX	0111	COMB	01BA	DAA
0059	BNE FD	0112	BRA F0	01BB	CBA
005B	DECA	0114	LDX 1FFF	01BC	BCS 01
005C	BNE F7	0117	DEX	01BE	CLRA
005E	PULA	0118	BNE FD	01BF	STAA 00,X
005F	PSHA	011A	PULA	01C1	INX
0060	ANDA F0	011B	DECA	01C2	TPA
0062	BEQ 41	011C	BNE E2	01C3	EORA 01
0064	PULA	011E	RTS	01C5	TAP
0065	ASLA	0120	LDX 03FF	01C6	RTS
0066	PSHA	0123	ORAB 7F	01C7	DEX
0067	BCS 11	0125	STAB 8002	01C8	STS 10
0069	PULA	0128	LDAA 25	01CA	LDAA 02
006A	ASLA	012A	DECA	01CC	BEQ 05
006B	PSHA	012B	BNE FD	01CE	LDAA 00,X
006C	BCS 13	012D	DEX	01D0	JMP 0020
006E	PULA	012E	BEQ 03	01D3	INC 0002
006F	ASLA	0130	COMB	01D6	BRA F6
0070	PSHA	0131	BRA F0		
0071	BCS 15	0133	PULA		

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Circle 134 on reader service card

Back-to-back op amps stabilize constant-current source

Although the single operational amplifier configured with the usual input and feedback resistors provides a passable voltage-controlled current source in low-energy applications, circuit stability and component sensitivity problems may be encountered in actual operation. Christopher S. Tocci of Krohn-Hite Corp., Avon, Mass., suggests a better idea—use two op amps and a sensing resistor **to eliminate the compensating networks normally required with one-chip sources and to attain extremely high output impedance without closely matched resistors.**

At the input, Tocci connects the control voltage to the noninverting input of an op amp, A_1. A_1's output is connected to the noninverting input of a second op amp, A_2, which in turn is connected to A_1's remaining input. The sensing resistor is placed across A_2's inputs, with the load connected from A_2's inverting input to ground.

The transfer function for this circuit is $I_{o\ (ma)} = V_{in}/A_2R$, where V_{in} is in volts, A_2 is the differential gain of op amp A_2, and R, the sensing resistor, is in kilohms. The output impedance is $Z_o = RAA_2$, where A is the open-loop gain of op amp A_2.

C-MOS gates make good, low-cost touch switches

Utilizing the high-input impedance of a complementary-MOS inverter, Steve Newman of Los Angeles, Calif., finds they are ideally suited for use as low-power, low-cost touch switches having greater reliability than their mechanical cousins. He also observes their contacts can be made very large, and they can be built without protruding parts, thus aiding the handicapped person or protecting the young child.

Noting the C-MOS gate is a voltage-controlled device, Newman designs the fingertip resistance (about 1 MΩ) into a voltage-divider circuit, with a 10-MΩ resistor used between the gate input and a positive voltage, and the fingertip applied between the gate and ground. If an inverter is used, **touching the contacts brings the gate output high.** If debouncing is required, the position of the contacts and of the 10-MΩ resistor are reversed, and a 0.01-μF capacitor placed across the contacts. Two inverters placed in series are then required to bring the output high when the contacts are touched. Making a toggle switch is easily done by using a D flip-flop, such as the 74C74. With its $\overline{Q}$ output wired to the data (D) input, the clock input is driven by the output of the momentary touch switch or the debounced version as described previously.

ASTM issues standards for magnetic materials

To the many existing volumes of its "Annual Book of ASTM Standards," the American Society for Testing and Materials has added a new one that will be of particular use to those engineers who design and troubleshoot large electromagnetic systems for instrument and control applications. Called part 44, the 1,337-page manual provides a storehouse of information on **the properties of various magnetic materials, magnetic-amplifier cores, magnetic shields, and other metals,** and will be highly useful to manufacturers, university researchers, and the military as well.

The price is $43. When ordering, ask for Publication 01-044079-40 from ASTM, 1916 Race St., Philadelphia, Pa. 19103.

-Vincent Biancomano

Communications tester works on site

Portable tester simulates data-communications equipment and performs transmission link tests to isolate faulty subsystems

by Bruce LeBoss, West Coast Editor, Computers & Instruments

The rapid growth of increasingly complex data-communications networks is generating a need for instrumentation that quickly isolates a faulty network subsystem, significantly reducing the system's down time and service costs. Tektronix believes it will satisfy that demand with its new 833 Data Comm Tester, to be introduced next month at Wescon in San Francisco.

Unlike network analyzers that use cathode-ray tubes and keyboards, cost $6,000 to $10,000, and are used primarily at dedicated site operations by trained specialists, the 833 is designed for use by field technicians who generally require portable and easy-to-use instruments. For a base price of $2,750, the 12-lb tester provides 80% to 90% of the functions of data-communications analyzers costing three or four times as much, according to Tektronix.

By simulating data-communications equipment to verify the correct operation of the terminals or central-processing unit, or by performing standard bit-error-rate and block-error-rate tests (BERT/BLERT) on the entire transmission link to verify correct operation of the modems or telephone line, the 833 quickly pinpoints the malfunctioning item in the network. This saves the user a lot of service calls, says Garth Eimers, product manager for digital service instruments. "Most of the time the network user can only guess which equipment is faulty and ends up calling the wrong vendor's service organization," he adds.

The tester can be set to match the parameters of nearly any data-communications system, half- or full-duplex, synchronous or asynchronous, up to 9.6 kilobits/s. It comes with the widely used RS-232-C/CCITT V.24 interface and an adapter that enables users to monitor and simulate equipment using a current-loop interface.

Using a Motorola 6800 8-bit microprocessor as the system controller, the 833 performs standard BERT/BLERT on the data links and calculates error-correction codes—cyclical redundancy checks (CRCs) and longitudinal redundancy checks (LRCs)—for confirming the accuracy of data in the network. "Frequently, data-communications errors happen in groupings, and just a parity check is often inadequate," explains Eimers.

One especially convenient feature of the 833 is its ability to store frequently used test patterns in an electrically erasable, programmable read-only memory. The EE-PROM, a 2-kilobyte 2716 type, contains identification and directory sections followed by variable-length test patterns, or buffers, that the operator can call up using only four keystrokes. The EE-PROM capability complements the seven standard messages—"the Quick Brown Fox . . ."—and the ASCII and EBCDIC character sets stored in the 833.

The user can program the 833 to initiate transmission of the stored messages as soon as it has received certain specified data sequences. Also, trigger positioning permits selective analysis of data received before, during, and after the trigger sequence.

The 833 also has two light-emitting-diode displays: a three-digit display showing address information in the buffer and a two-digit hexadecimal representation telling the user what code is being examined.

Availability of the 833 is four to eight weeks.

Tektronix Inc., P. O. Box 500, Beaverton, Ore. 97077. Phone 1-800-547-1512 [338]

Data acquisition

A-d unit works in three modes

8-bit converter acts as RAM, ROM, or bulk memory under microprocessor control

Historically, the hardware for getting data into and out of computers has always seemed to cost more than the data processors themselves, a situation that has become more pronounced as inexpensive microprocessors have become widely available. Now a counter trend seems to be brewing, one towards low-cost converters compatible with microprocessors [*Electronics*, March 15, 1979, p. 39].

The latest example of the new trend is Analog Devices Inc.'s AD7574, an 8-bit, monolithic analog-to-digital converter that not only has three-state outputs, but also interfaces with a microprocessor as if it were a memory.

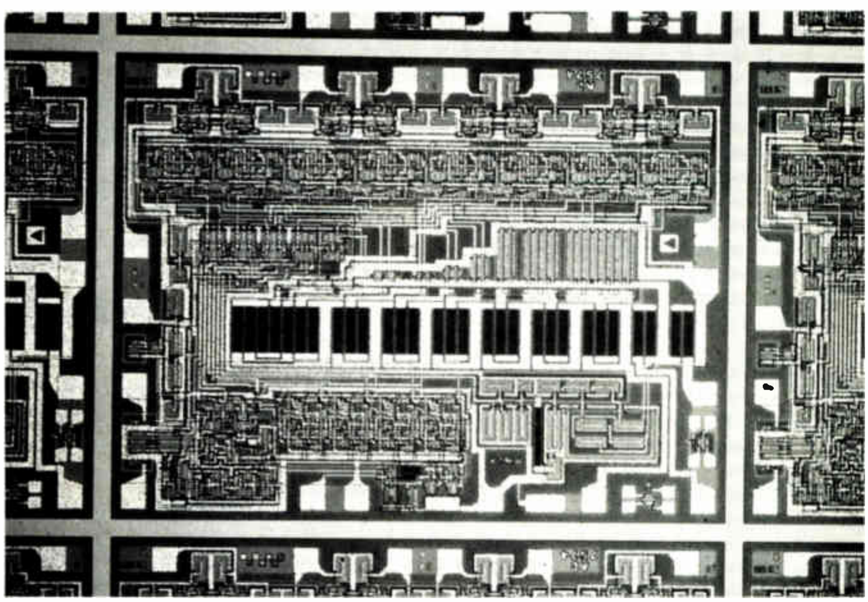
At the user's option, the AD7574 may be connected and operated as if it were a random-access memory, a read-only memory, or a bulk memory. Therefore, both the data conversion and the data readout can be directly controlled by the processor.

Not only is the AD7574 compatible with microprocessors, it also combines attractive specifications and low price. It is fully monotonic over its operating temperature ranges. It is possible to obtain relative accuracy of ±½ least significant bit, differential nonlinearity of ±¾ LSB, a gain error of 3 LSB, and a ±30-mV offset error in any of the three temperature ranges (from consumer through commercial to military) in the user's choice of plastic or ceramic packages. In its low-cost plastic-packaged version, the AD7574 JN, or KN, costs as little as $5 or $6, respectively, in 1,000-unit lots.

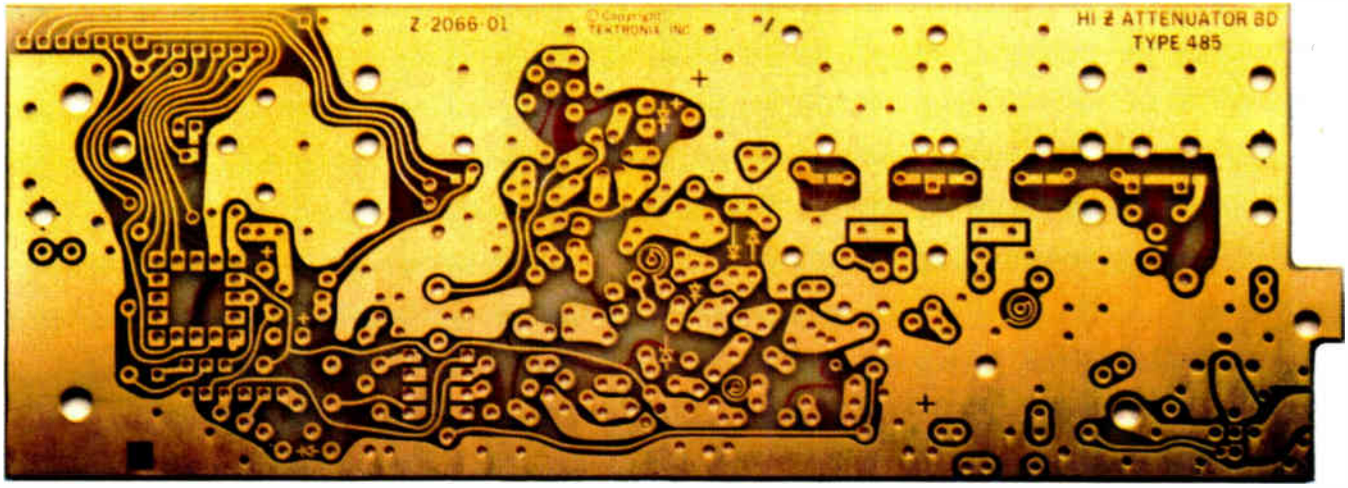
Conversion time is rated at 15 μs and is controlled by an outboard R-C network. Somewhat faster or slower conversions are possible, though Analog does not guarantee performance at speeds below 15 μs.

Handshakes. Working like a memory-mapped input device, the converter has three modes of operation with a microprocessor. In the static-RAM mode, conversion begins when the microprocessor sends a memory-write command to the unit. A data-read occurs when the microprocessor fires a memory-read toward the convertor's address.

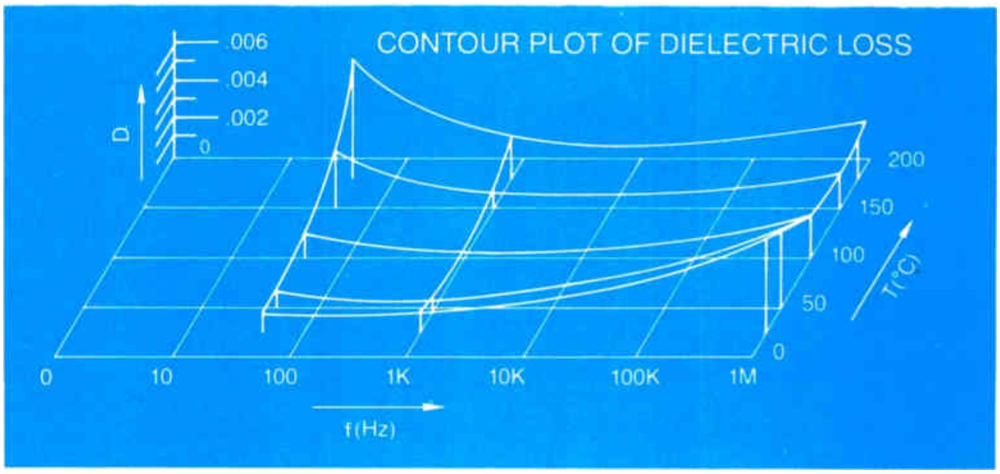
In the ROM mode, a memory-read instruction triggers data dump as well as automatically triggering the



POLYSULFONE PCB SUBSTRATE GIVES



PERFORMANCE CLOSE TO PTFE/GLASS,



AT A PRICE CLOSER TO EPOXY/GLASS

When you're looking for high performance in PCB's—particularly in high frequency applications—a polysulfone substrate can give it to you at far less cost than PTFE/glass. Polysulfone has excellent electricals: low dielectric constant and low dissipation factor for low loss (see graph). It withstands hand and wave soldering (500°F. bath for 5 seconds).

Polysulfone can be easily extruded for PCB substrate, and easily drilled. Copper-clad laminate of polysulfone has good peel strength and low z axis expansion. It can be processed by subtractive, semi-additive and fully additive processes. (Copper-clad sheet is available from Norplex.)

You can also *mold* polysulfone for PCB's with standoffs, holes of all sizes, and in almost any shape—to save finishing and machining time.

And cost is modest. Tektronix saved $120,000 annually by switching from polyphenylene oxide to extruded UDEL® Polysulfone.

For full data on UDEL Polysulfone for PCB and other electric/electronic applications, use the coupon below or the reader service card.

UNION CARBIDE CORPORATION
Engineering Polymers, Dept. XXX
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I'd like to get high performance in PCB's at lower cost. Please send me bulletin on UDEL® Polysulfone.

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Engineering Polymers

Circle 139 on reader service card

beginning of a new conversion.

In the "slow-" or bulk-memory mode, the AD7574's status output is used to control the READY input of a microprocessor. Conversion starts when a memory-read command is generated for the 7574. $\overline{\text{BUSY}}$ immediately goes low, indicating that conversion is underway and forcing the microprocessor into a wait state. It waits until $\overline{\text{BUSY}}$ goes high, then finishes executing the data-read instruction.

Obviously the AD7574 is compatible with most widely used microprocessors such as the Z80 and the 8080. It is almost self-contained, requiring a resistor and a capacitor for clocking, plus a 5-V power supply and a −10-V outboard reference. Analog suggests its AD584 for this purpose.

The C-MOS successive-approximation converter uses little power, consuming only 25 mW during standby. Also, the converter's clock oscillator is run only during conversions. Finally, the unit can be operated as a ratiometric device. It is not, though, tested and guaranteed for this purpose; its rated transfer accuracy applies only with a −10-V reference.

Prices for AD7574s, in lots of 1 to 24, range from $12.50 to $41.00, depending on package and temperature range. Delivery is from stock.

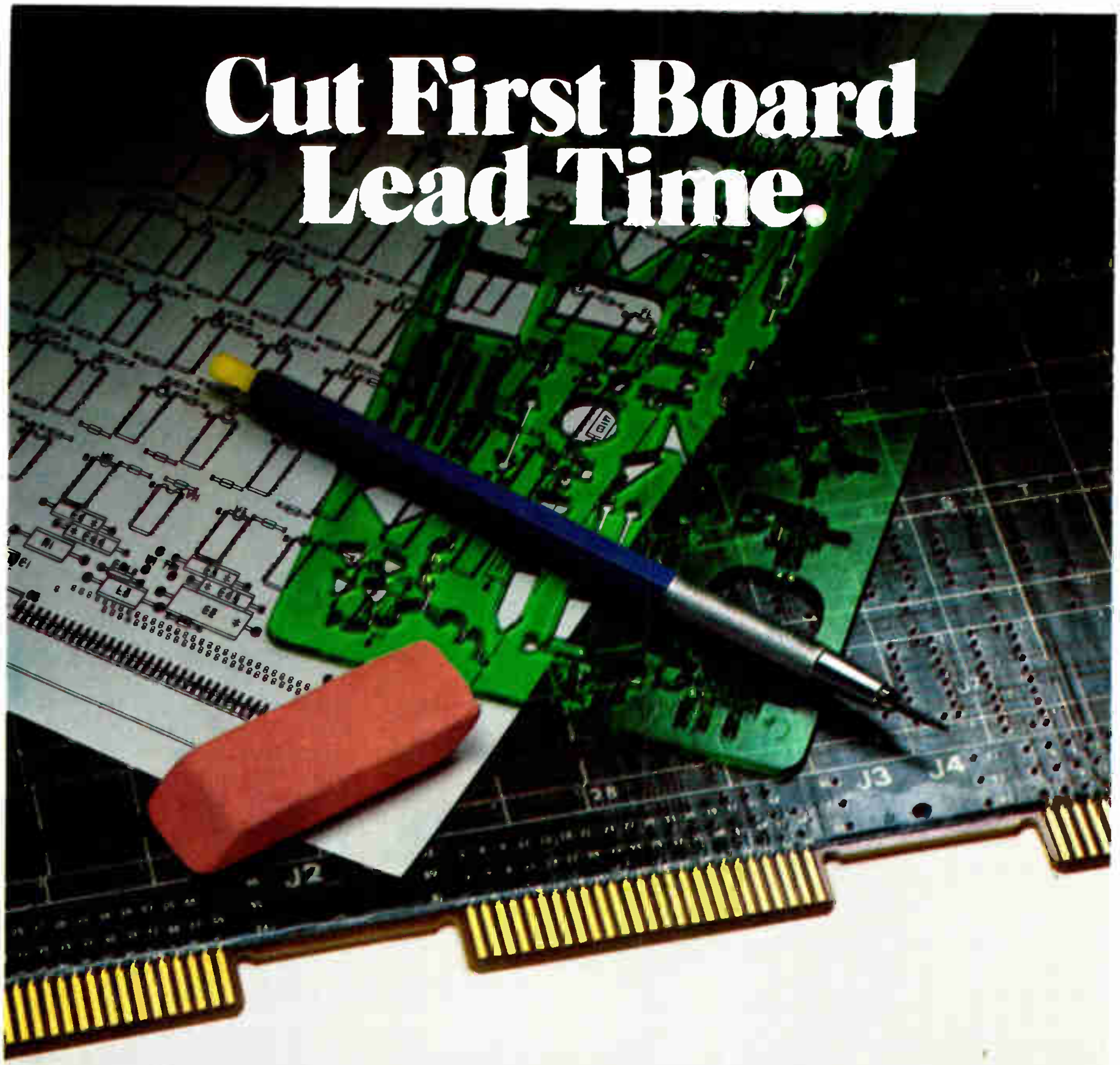
Analog Devices Inc., Route One Industrial Park, Norwood, Mass. 02062. Phone (617) 329-4700 [381]

D-a converter resolves 18 bits in 25 μs for $775

Offering 18-bit resolution, the ZDA1800 digital-to-analog converter has a temperature coefficient of 0.2 part per million/°C. With such stability, the converter will find use in medical instrumentation, flight control, and scientific equipment. The unit also features a voltage-settling time of 25 μs to within ½ least significant bit and a current settling time of 10 μs to within ½ LSB.

The ZDA1800 has a companion

Cut First Board Lead Time.



Circuit data to first board in just six weeks.

This Multiwire board, with 285 IC's and dozens of discrete components, went from circuit data to first board in just six weeks. Reason: our customer had only to supply art work for the power and ground planes, a net list and a fabrication blueprint. No need for artwork for each of the circuit layers.

These simplified input requirements for Multiwire boards get you into production faster than conventional wirewrap or multilayer techniques. You'll get the finished product as much as *10 weeks* sooner than other methods.

Multiwire boards also offer fast and easy circuit changes, controlled impedance, reduced inspection costs and higher production yields.

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Multiwire, 31 Seacliff Avenue, Glen Cove, NY 11542. Phone (516) 448-1307

MULTIWIRE

Multiwire is a registered tradename for Kollmorgen Corporation's discrete wired circuit boards.

Circle 141 on reader service card

d-a converter, the ZDA1600, which provides 16-bit resolution with a 0.4-ppm/°C temperature coefficient and settling times to within ½ LSB of 20 μs (for voltage) and 8 μs (for current). Monotonicity is guaranteed over a 0° to 70°C temperature range.

Both converters have on-board references and output amplifiers.

In quantities of one to nine, the ZDA1800 is priced at $775, the ZDA1600 at $275. Delivery is from stock to 30 days.

Zeltex Inc., 940 Detroit Ave., Concord, Calif. 94518. Phone Dick Terry at (415) 686-6660 [383]

On-board RAM allows signal-gain preprogramming

Featuring 12-bit resolution, the ADS1216, a 16-channel data-acquisition system for use with any size microprocessor bus, offers a 200-ns throughput time. Two specialized on-card memories allow asynchronous data communications between the analog and the digital portions of the system.

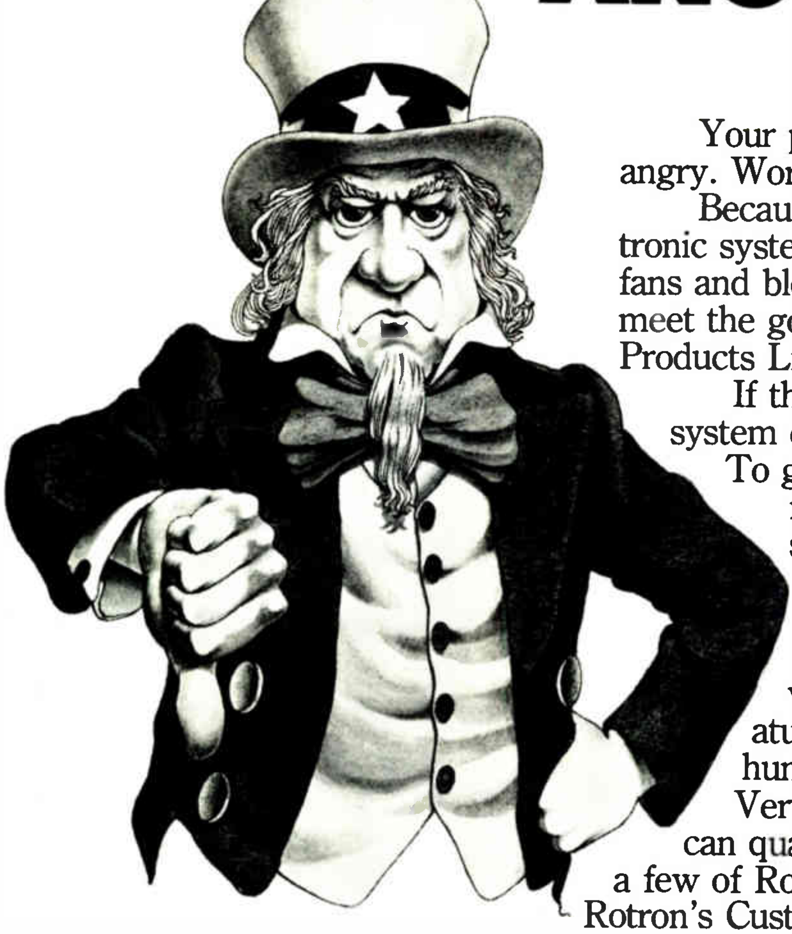
The first random-access memory allows preprogrammed signal gain for each analog signal input channel. A precision gain-setting network permits gains of 1, 2, 2.5, 5, 10, 20, 50, or 100. The acquired data can then be stored in a second 16-by-12-bit RAM until the system needs it.

The ADS1216 also has TTL bus drivers, a precision voltage reference, and a sample-and-hold amplifier, as well as all the timing, control, and interface circuitry required to interface the data-acquisition system with any 8-, 12-, or 16-bit microprocessor bus. Because it is memory-mapped, the 1216 may be treated as memory by the CPU. The 16-channel multiplexer may be configured as 16 single-ended, 16 quasi-differential or 8 differentation channels.

Priced at $540 each in quantities of 25 or more, the ADS1216 has delivery from stock to three weeks.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 737-5000 [384]

IF YOU DON'T USE QPL QUALIFIED FANS, SOMEONE COULD GET ANGRY.



Your project manager could get angry. Worse yet, so could Uncle Sam.

Because if you're designing electronic systems for the government, the fans and blowers used to cool them should meet the government's stringent Qualified Products List (QPL) requirements.

If they don't, your whole system could get rejected.

To get on the QPL, an airmover not only has to meet mil specs for its overall design; but also extreme service and environmental conditions.

Such as severe shock and vibration. High and low temperature operation. And resistance to humidity, salt, fungus and dust.

Very few airmovers on the market can qualify for the QPL list. But quite a few of Rotron's airmovers qualify.

Rotron's Custom Division has a surprisingly large selection of fans and blowers already on the Qualified Products List.

They're standard products. So they cost less than specially built models. They're readily available. And the specs are already written for them.

So you don't have to struggle to write them. And the government won't reject them. Because the government wrote them.

If you don't want your system to get turned thumbs down by Uncle Sam, use the airmovers he's already pointed out to you.

We'll be glad to tell you which ones.
Custom Division, Rotron Inc., Woodstock, N.Y., 12498, (914) 679-2401.

ROTRON INC.
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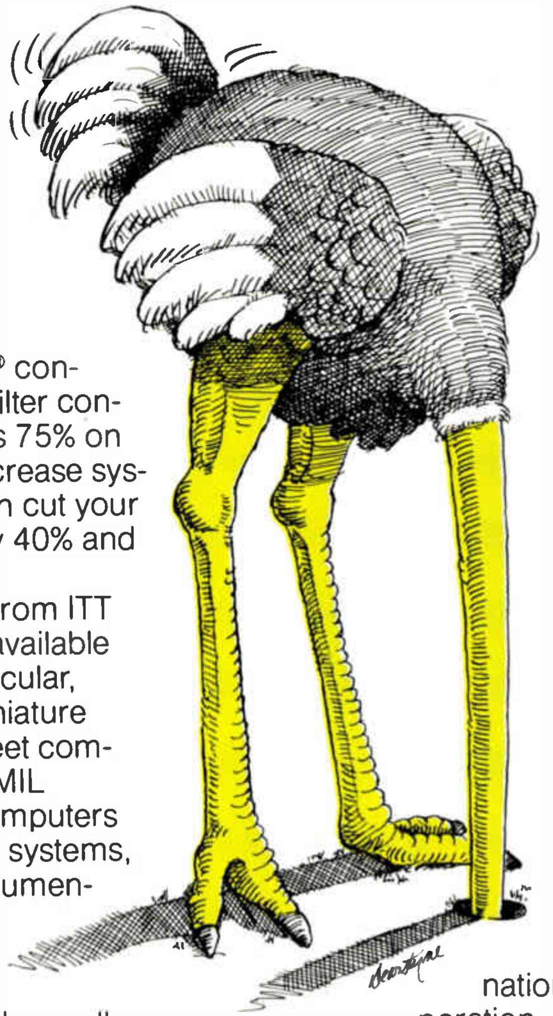
Rotron B.V., Oosterhout, Netherlands. Tel: 1620-32920.

6589

It has come to our attention that some designers are still using discrete EMI/RFI filters

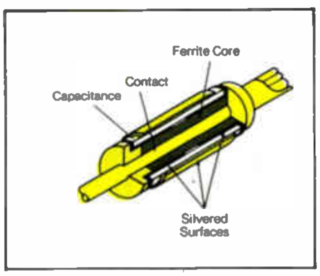


And that's a shame.

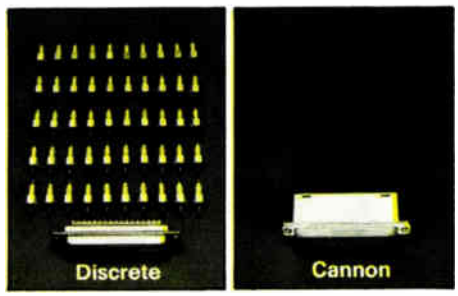
Because Cannon® connectors with integral filter contacts save as much as 75% on space and weight. Increase system reliability. And can cut your total installed costs by 40% and more.

Filter connectors from ITT Cannon Electric are available in rectangular and circular, miniature and subminiature configurations. To meet commercial, ARINC and MIL specifications. For computers and communications systems, medical and test instrumentation, aerospace and automotive applications.

Filtering is available on all or any contacts within the connector. A ferrite tube surrounding the contact forms a series inductor within a concentric, selectively-coated ceramic tube which forms the capacitors of a pi-filter.



Completed connectors, like the computer I/O configuration shown, aren't much larger than the standard connector, yet provide typical attenuation of 70 dB. They eliminate the components, wires and "dog box" that you've had to deal with,



Computer I/O filters

and all the engineering, assembly and testing that go with them.

And Cannon filter connectors can reduce your total installed costs by 40% or more. Now that you know, there's no excuse not to use them, so contact your nearest ITT Cannon field office today.

ITT Cannon Electric, International Telephone and Telegraph Corporation, 2801 Air Lane, Phoenix, AZ 85036, telephone (602) 275-4792.

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Microcomputers & systems

MDS supports GI's 8-bit PIC family

In-circuit emulator stands alone or mates with computer for a full development system

As nothing widens the spread of a microcomputer's applications like a development system, the makers of the 8-bit PIC family of single-chippers are offering an in-circuit emulator (ICE) that can stand alone or be attached to a computer to make a full development system.

The idea behind Pices—for PIC ICE system—is to offer a low-cost professional development system for the PIC series, says Alex Cilento, marketing manager for microprocessor products at General Instrument Corp.'s Microelectronics Group. It costs $2,500, and since it comes unbundled, it can link onto a computer or a development system like Intel's MDS (Microprocessor Development System) or Motorola's EXORciser.

The Pices features a module with a 1664B microcomputer, which uses an external random-access memory, but no internal read-only memory, to emulate the operation of the PIC 1650A, 1655A, or 1656. Housed in the Pices box is the control processor, a CP1600 16-bit microprocessor. Its predecessor, the DB 1650 emulator, used a PIC chip as control processor.

As a stand-alone unit, Pices attaches directly to a serial input/output device, typically a teletypewriter, for emulation and debugging. For a one-station development system it can function as a serial peripheral device for any minicomputer or mainframe that can support Fortran.

The system can operate in three modes: real-time, single-step, or program-trace. It single-steps in the program-trace mode, following the address limits, register identifications, or register contents specified by the programmer. Moreover, these conditions are cumulative. It has eight individually addressable breakpoints, active in all three modes.

Pices is a symbolic debugger that permits a program to be patched with mnemonics. Once these are entered, it translates them directly into binary object code. Cilento points out that the PIC microcomputers have a 512-by-12-bit ROM, so debugging of an entire instruction set need not be onerous with a stand-alone unit.

Major program writing and editing, however, call for a computer that can edit and assemble source code. The firm offers a Fortran PIC cross-assembler for users who plan to set up such a full development system.

The system, as a stand-alone unit, may have either an RS-232-C or current-loop interface, with a switch-selectable baud rate. For the full development system, it may be attached to the computer as a separate peripheral or it may be in series with the system's teletypewriter or cathode-ray-tube terminal.

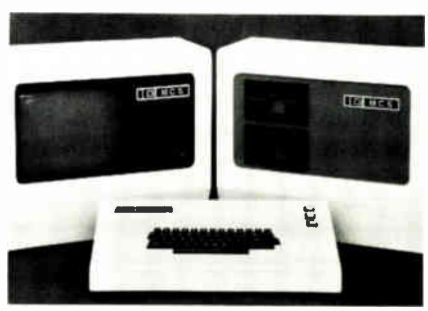
General Instrument Microelectronics, 600 W. John St., Hicksville, N. Y. 11802. Phone Alex Cilento at (516) 733-3352 [371]

Development system emulates several processors for $4,995

Supporting four real-time emulators, the ICC/MCS universal microprocessor development system is not locked into a specific processor from a single manufacturer. Currently the MCS will emulate the 8080, the 8085, the Z80, and the 1802, and several others are under development for introduction later this year. In both tape- and disk-based versions, the operating system offers an editor, an assembler, and a monitor; a Z80 Basic compiler is also available as an option.

Sporting 16-bit capability, the MCS system has a debugging monitor with a full register and a selected memory region display, as well as an extended command structure. Each development system includes a keyboard, a cathode-ray-tube display, 16 kilobytes of random-access memory, parallel or serial input/output ports, a Z80 master central processing unit, dual tape or disk drives, and a complete software package.

The tape version is best for users



who have applications where only a limited amount of software development is required, but who do a lot of debugging and emulation work. This cassette-tape version sells for $4,995. Disk-based systems—for users who need to do more than testing and product checkout—start at $8,450. Delivery on all systems can be made within 30 days.

Tecma Inc., 2366 Walsh Ave., Santa Clara, Calif. 95051. Phone Harry White at (408) 727-1997 [373]

Floppy-disk system provides two drives for AIM 65

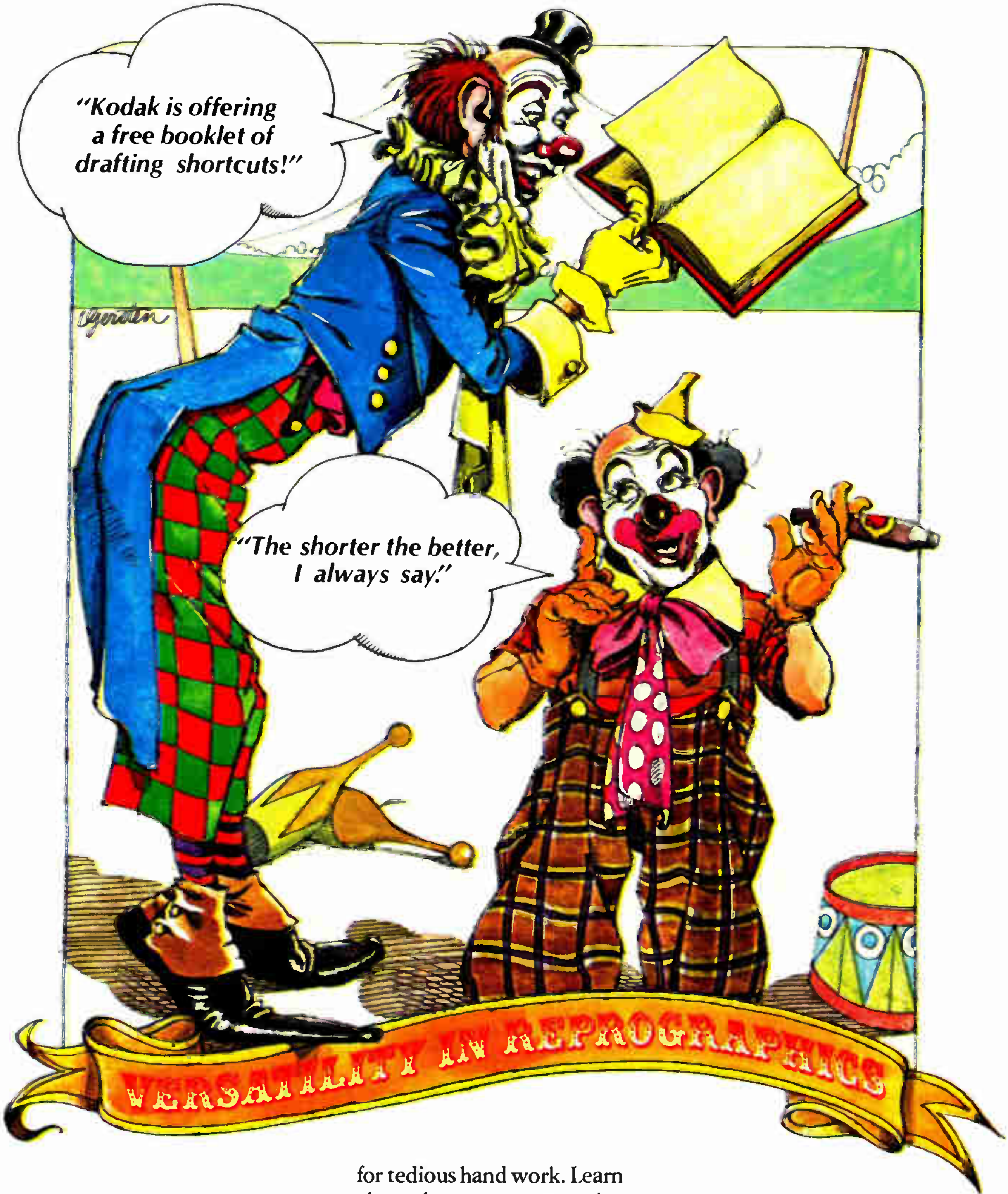
A floppy-disk system that is fully compatible with Rockwell International's AIM 65 is now being marketed. Consisting of a floppy-disk controller, a power supply, and one or two floppy-disk drives, the DAIM system is designed for use with the Rockwell expansion motherboard featuring the System 65 bus standard.

With all the features of the System 65 operating software, the disk operating system software for the DAIM controller board resides in erasable programmable read-only memories. Disks written on the DAIM system may therefore be used on a System 65 microprocessor development system and vice versa. Disk functions include loading and saving source and object files, initializing disks, zeroing a disk directory, listing files and disk directories, renaming files, deleting and recovering files, and compressing a disk to recover unused space. All commands are identical to those found on a System 65.

The power supply provides all power requirements for two disk drives and the controller board.

A DAIM controller board with all of its operating software in EPROM, a power supply, and one disk drive is priced at $850; an additional disk drive sells for $350. Delivery is scheduled from stock to 60 days.

Compas Microsystems, 224 S. E. 16th St., Ames, Iowa 50010. Phone (515) 232-8187 [377]



The long and short of it is that our booklet entitled "Versatility in Reprographics" can show you how to save time and money in your drafting operations. And it's free!

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Circle 147 on reader service card

Components

5-kV isolators degrade slowly

Optical devices offer high gain at low current, work well with microprocessors

The usefulness of opto-isolators in protecting people and sensitive equipment from high voltages is well established. Unfortunately, they suffer from some problems: the isolators are not always reliable, and many require too high a drive current to be easily interfaced with microprocessors. Now, however, Litronix is offering a new family of opto-isolators it claims helps solve those problems.

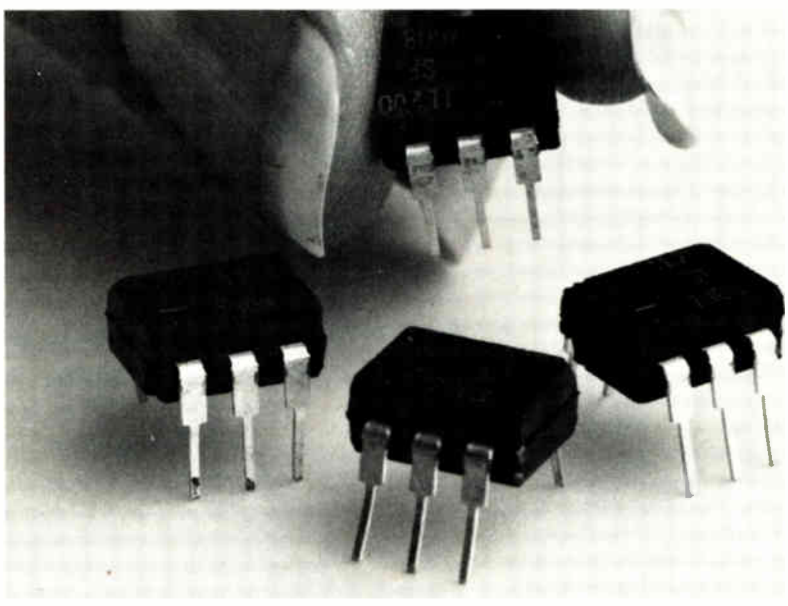
Called the IL-200 series, the three-part family has a typical degradation of less than 20% per thousand hours compared with about 50% per thousand hours for many similar products, according to Andrew Mann, product marketing manager. Actually, the figure is nearer 10%, Mann says, so "they should survive more than 10 years without any problem."

The current transfer ratio (CTR) of the IL-200 series units is specified at a current of 1 mA, making it easy to design them into microprocessor systems. According to Mann, most others are specified only at 10 mA, which is less useful in this application. The family has an input/output isolation rating of 5 kV—especially useful in Europe where high line voltages are standard.

At a drive current of 10 mA, members of the IL-200 family are offered with three CTRs: 75 to 150% for the IL-201, 125 to 250% for the IL-202, and 225 to 450% for the IL-203. At 1 mA, the respective CTRs are 10, 30, and 50%.

Mann attributes the long-term stability and high gain of the IL-200 series to proprietary advanced processing technology employed in the manufacture of the isolators' infrared-emitting diodes. These diodes are made for Litronix by parent Siemens of West Germany, using a special liquid-phase epitaxy technique. The devices' high voltage rating is largely attributable to a new double-molding process in which the inner section of the package, where the IR diode is optically coupled to a phototransistor, is made of clear epoxy, he says.

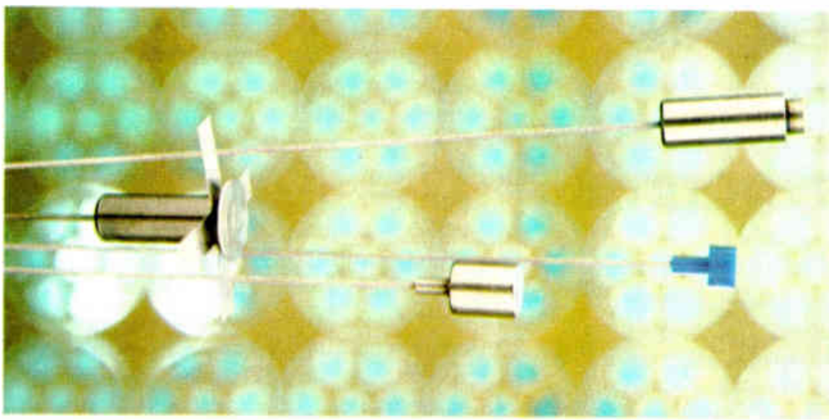
Thousand-piece prices for the IL-200 parts, which come in six-lead dual in-line packages, are $1.00 for the IL-201, $1.08 for the IL-202,

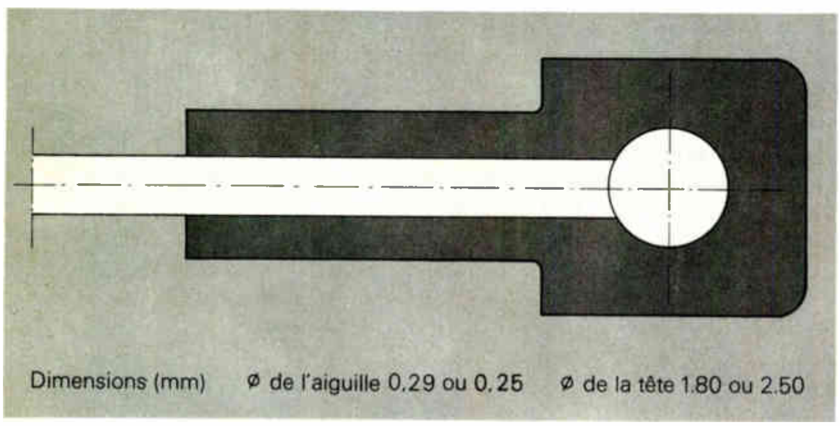


Wires for printers

Seitz

Seitz, c´est sûr !





Seitz technology

Seitz experience in the machining of hard materials has contributed to the realization of wires enabling to print characters of a perfect quality.
The materials used for these wires are extremely hard. They make it possible to obtain a highly polished surface and a great precision. They are resistant to wear (less than 0.1 mm per 30,000,000 characters), to chemical agents and heat.
Seitz research and developping departments co-operate closely with the manufacturers of printing heads.
The booklet «Wires for printers and their guides» will give you detailed information.

Design Borel

Seitz SA, CH-2416 Les Brenets, Tél. 039/32 11 12, Télex CH 35 505 SEITZ

Pierres Holding, Faubourg du Lac 6, CH-2501 Bienne
Téléphone 032 / 22 65 11, Télex 34 566

and $1.20 for the IL-203. Small quantities are available through distributors from stock to 30 days.

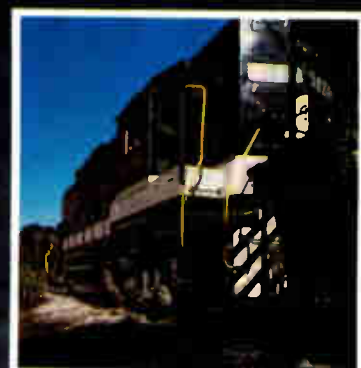
Litronix, 19000 Homestead Rd., Cupertino, Calif. 95014 [341]

Microprocessor-based readout displays 40 characters

With their combination of programmability, made possible by one-chip microprocessors, and a newly developed production technique, planar-gas-discharge displays continue to make inroads into the large-alphanumeric-display market long dominated by the cathode-ray-tube variety. The latest example is a 40-character five-by-seven-dot-matrix unit from Beckman Instruments Inc. The company has put many features in one plug-in package, including brightness and programming flexibility that "together amount to a real advance," claims Roger Frankland, program manager at Beckman's Display Systems division.

Topping Frankland's list of notable features for the model SM-810-001 are 0.25-in.-high characters, which provide 100 ft-L of orange illumination. The brightness drops to 50% at a viewing angle of 130°. An on-board Intel 8041A microcomputer increases the display's versatility, according to Frankland. "Any character or block [of characters] can be programmed to blink to highlight data," he adds. Furthermore, a blinking cursor can highlight any part of a message a user wants.

Also incorporated in the 8041A processor are characters that can now be entered randomly from either the left or the right, so data can be updated without rewriting entire lines. A random-access memory



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Items \ Model	XE-120	XE-121	XE-122
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Accuracy	±0.5%/FS	±0.1%/FS	±0.025%/FS
Power Supply	DC ±15V ±35mA		
Dimension	50W x 50D x 16H mm		

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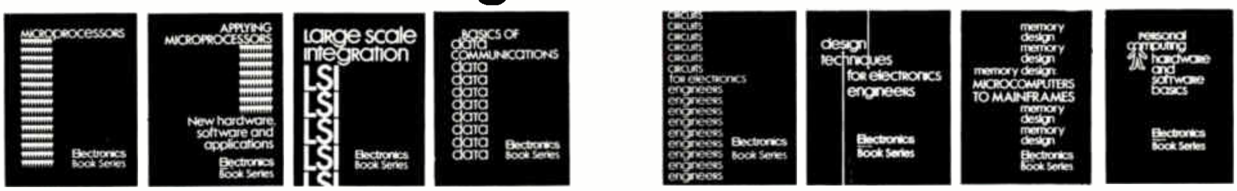

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stores the character set, while a read-only memory decodes and sends each character to the right place on the line. The set includes 52 upper- and lower-case letters, 10 numerals, and 34 symbols and punctuation marks.

Its compatibility with 8-bit bidirectional buses and its ability to run off a single 5-V dc supply should make the SM-810-001 particularly easy for designers to apply, Frankland feels. In effect, he points out, it becomes a peripheral.

The display, which measures 3 by 10.75 by 2 in. and has a write time of 310 ns, is expected to find major applications in such diverse areas as analytical instrumentation and point-of-sale terminals. It will sell for $475 in quantities of one to nine, $390 in lots of 10 to 49, and $350 for 50 to 99, as a standard off-the-shelf item.

Beckman Instruments Inc., Display Systems division, 350 North Hayden Rd., P. O. Box 3579, Scottsdale, Ariz. 85257. Phone (602) 947-8371 [342]

Metal-foil resistors cannot but stay dry

So that they can withstand exceptionally adverse environments and meet the performance requirements of MIL-R-55182, the series AF-102 precision metal-foil resistors are first encapsulated in two layers of silicone rubber and then completely sealed in a vacuum-transfer-molded moisture-proof epoxy case. Lead integrity is unusually high because of a patented lead-to-substrate connection.

The resistors have a resistance range of 1 Ω to 20 kΩ, a power rating of 0.3 W, tolerances of 0.005% to 1%, a temperature coefficient of better than ±3 ppm/°C, and tracking of better than ±½ ppm/°C. (Temperature coefficients to 1 ppm/°C are available.)

Price is $5 to $7 in quantities of 100, depending on tolerance, and delivery takes 6 to 10 weeks.

Angstrohm Precision Inc., 1 Precision Place, Hagerstown, Md. 21740. Phone (914) 232-7501 [343]

IBM's System/38 slips six to nine months

IBM's System/38 small business computer, which promises a new architecture and a dramatic new hardware technology (*Electronics*, November 9, 1978, p. 81; March 15, p. 101), has missed its original August delivery deadline. **The corporation's Atlanta, Ga.-based General Systems division said earlier this month it anticipates a delay of six to nine months.** Apparently IBM has run into problems with its ambitious plan to offer a sophisticated operating system and data-base management scheme, intended to insulate the user from hardware details and future changes.

Calma speeds up editing in VLSI design system

Calma is adding a new feature to its GDS II interactive VLSI design system that it claims offers faster editing than any other commercial system. To back the claim, the Sunnyvale, Calif., company says that **Edit-in-Place lets users modify any number of structures or cells without the repetitive loading and unloading of data** necessary in other systems. Moreover, it has a "creating-in-place" capability, allowing users to create a new device for a circuit and use it repeatedly with minimal data-storage requirements. The GDS II is priced at about $250,000.

New Fortran software attacks development costs

Recognizing that software development now accounts for over half of the systems development costs of its customers, Systems Engineering Laboratories Inc. is introducing six software products aimed at easing and thereby decreasing the cost of the development process. **Most interesting are a Fortran compiler said to surpass the ANSI 77 standard, two expanded run-time libraries, and two packages intended to aid performance analysis.** And because software also accounts for more than half its own development budget, the Fort Lauderdale, Fla., company is selling software separately and thus is one of the last computer vendors to unbundle software. Prices for a single system supplied in binary form range from $200 to $8,000.

National offers data logging, burn-in with 16-, 64-K RAMs

To help customers cut incoming test costs and set up logic better on their boards, National Semiconductor Corp. will begin offering this fall a unique service to buyers of 16- and 64-kilobit dynamic random-access memories. The service will combine **extended high-temperature dynamic burn-in with data logging of hard failures and soft errors** for three-power-supply 16-K RAMs and for National's upcoming 5-V single-supply 16-K and 64-K RAMs. Called Memory Systems Testing, the service will cost customers about $1 more per part.

Option extends universal counter's range to 1 GHz

By adding an option to its model 5315A universal counter/timer, Hewlett-Packard Co., Palo Alto, Calif., has extended the instrument's frequency-measurement range from a maximum of 100 MHz to 1 GHz. Because it measures the period of the input waveform and then finds the reciprocal of the measurement to determine the frequency, the 5315A has **a resolution of at least seven digits over its full frequency range of 1 Hz to 1 GHz, with the process taking only 1 second.** The extended frequency range makes the counter/timer suitable for communications, navigation, and fm and TV broadcasting applications. The 1-GHz frequency option, number 003, adds $250 to the 5315A's base price of $800.

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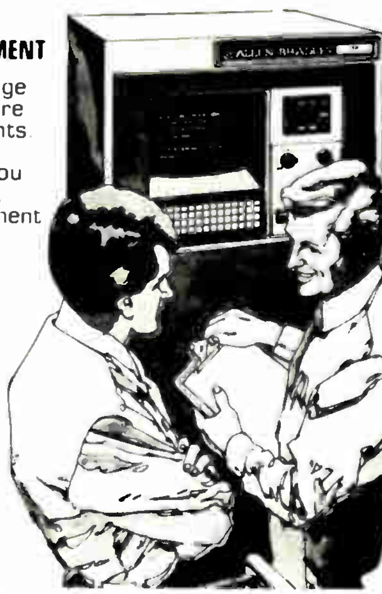

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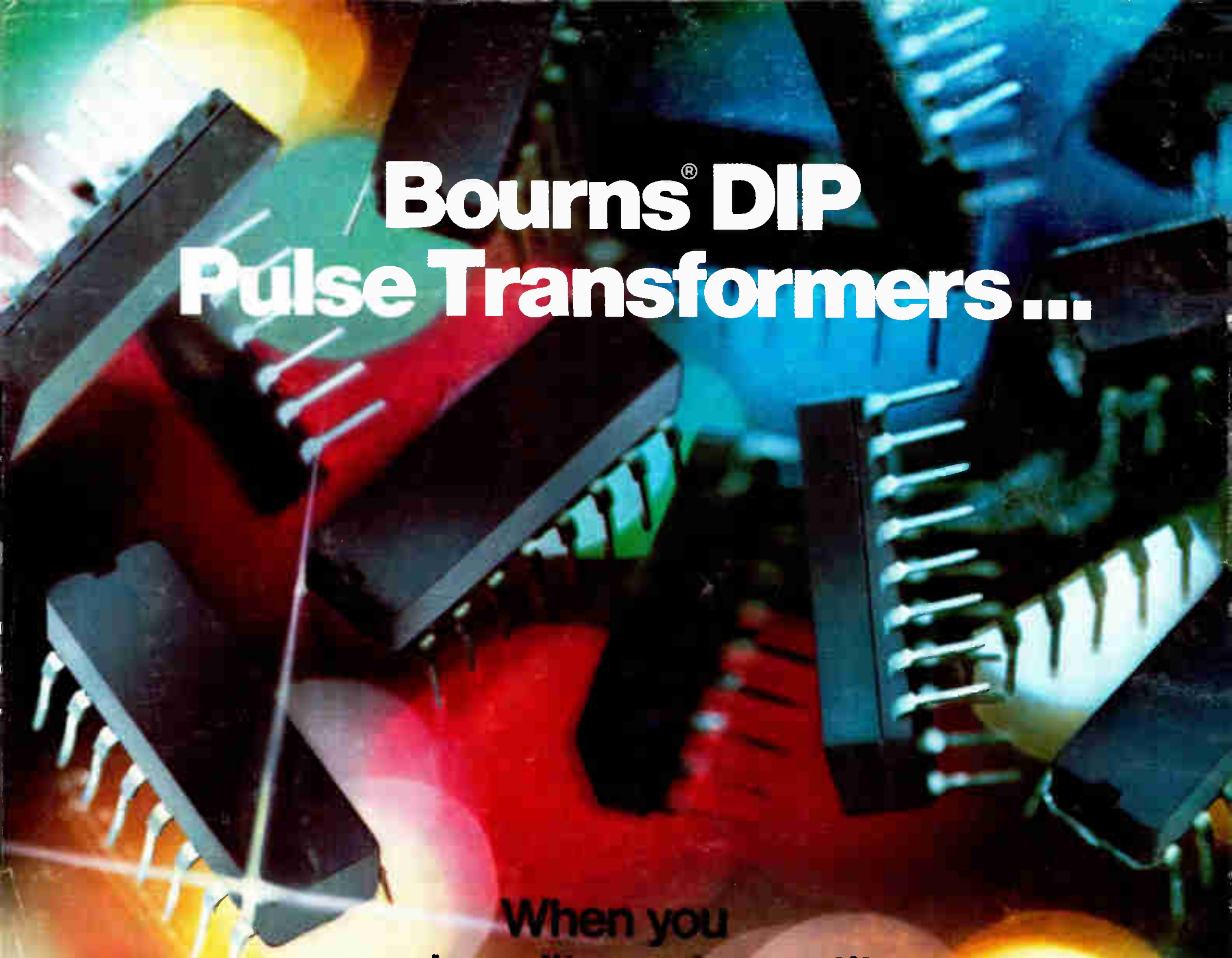

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