

JULY 5, 1979

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Parallel processing with minicomputers, part 1/125

Surface-acoustic-wave devices expand application range/136



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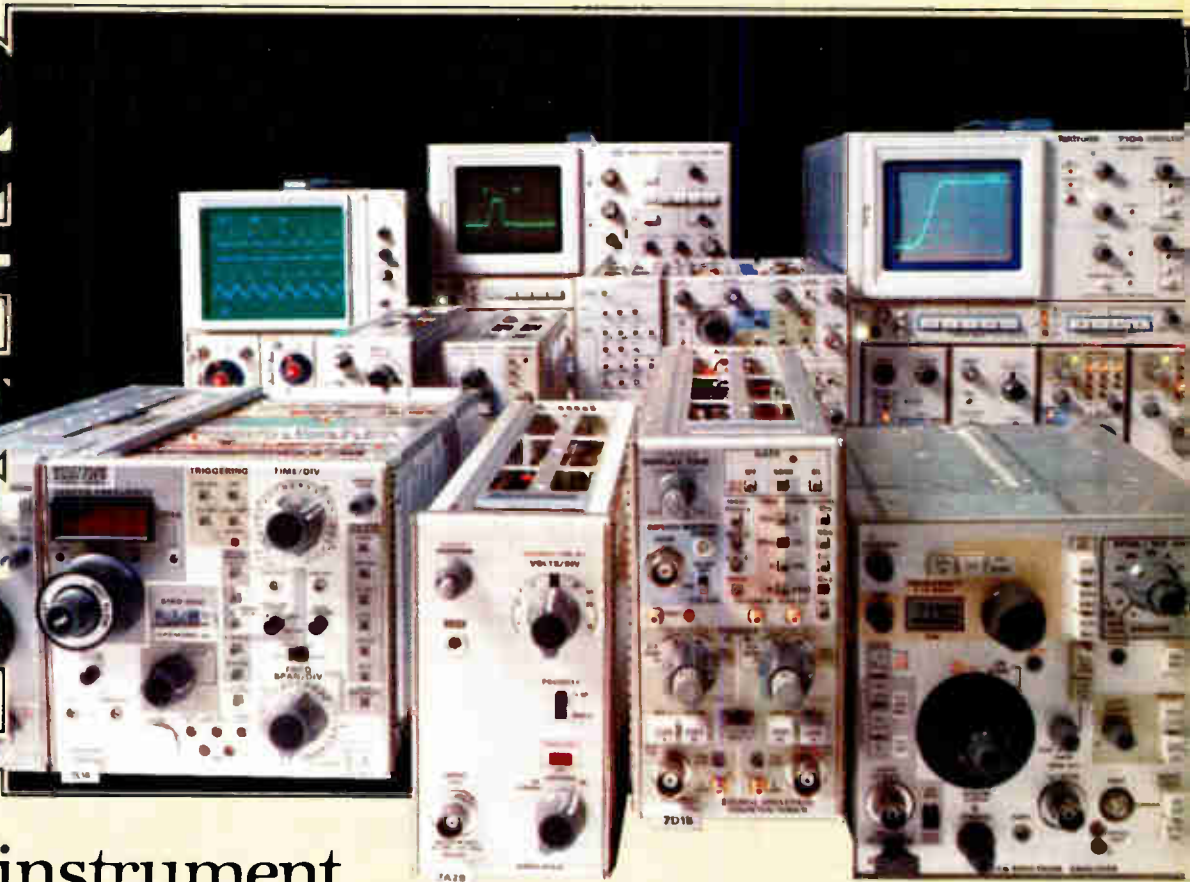


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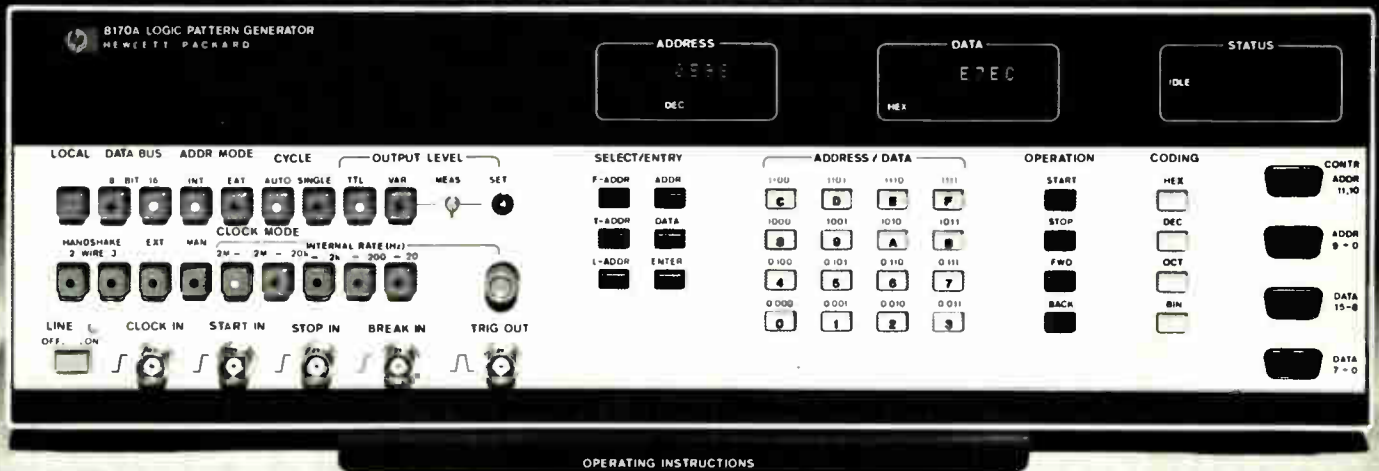
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Highlights

Cover: Customizing logic in house, 109

By selectively blowing fuse links in a chip's array, a user can configure multiple logic elements for a specific purpose while in the field, instead of using a fistful of discrete devices to build a bridge between large-scale integrated circuits. This is Part 1 of a two-part article on field-programmable logic arrays.

Cover is by Art Director Fred Sklenar.

Microprocessors get help with math, 99

Specialized number-crunching chips are being developed to take such chores as floating-point math and fast Fourier transforms off the hands of central processors. These peripheral processors offer tremendous speed advantages over software implementations.

SAW filters reduce trimming headaches, 115

Photolithographic techniques make possible surface-acoustic-wave chips with highly reproducible characteristics. They are versatile in such vhf applications as bandpass filters, delay lines, and convolvers.

Minis are moving to parallel processing, 125

Cheaper hardware is the reason. Part 1 of this two-part article examines the pros and cons of the architectural possibilities of ganging processors to increase system performance.

... and in the next issue

A special report on photovoltaic devices . . . a microcomputer adapted to encrypt and decrypt data . . . a programmable general-purpose slave processor (Part 2 of parallel processing article).

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A fascinating aspect of semiconductor technology has always been the way the increased complexity or speed of one family of devices creates the need for the development of another product. A perfect example is the field-programmable logic family introduced by Signetics Corp., Sunnyvale, Calif.

As described in the cover article (p. 109) of this issue, the field-programmable logic (FPL) family was developed to fill the need to connect large, complex "functional islands" in a system framework. The increased complexity and speed achieved in large-scale integration required a similar improvement in the clusters of small- and medium-scale integrated circuits used to link the LSI chips.

"The market need arose, but there was resistance to using custom logic," recalls one of the authors, Napoleone Cavlan, applications manager for Signetics. "The prime objective," adds senior applications engineer Stephen Durham, his co-author, "was to put custom logic functions in a standard package."

The resulting devices provide a compact alternative to random logic, replacing discrete gates, wires, and connectors and gaining reduction in

board space, power, and cost. All the FPL devices—field-programmable gate arrays, logic arrays, and logic sequencers—can be, as the name implies, programmed and modified in the field so that the logic can be changed without expensive retooling of printed-circuit boards.

The value of parallel processing in mammoth computers is well-known. But what are the techniques for applying the concept to minicomputers? They are described in the first part of a two-part article (p. 125) by Jerry Braun and George White of Computer Automation Inc.

"The impetus for a technique such as parallel processing is to get more performance out of a system without throwing away the bus and starting all over again," says White, manager of advanced architecture research and development for the company's Naked Mini division in Irvine, Calif.

Part 2, in the next issue, will present applications of this concept using Computer Automation's 4/10S slave processor.

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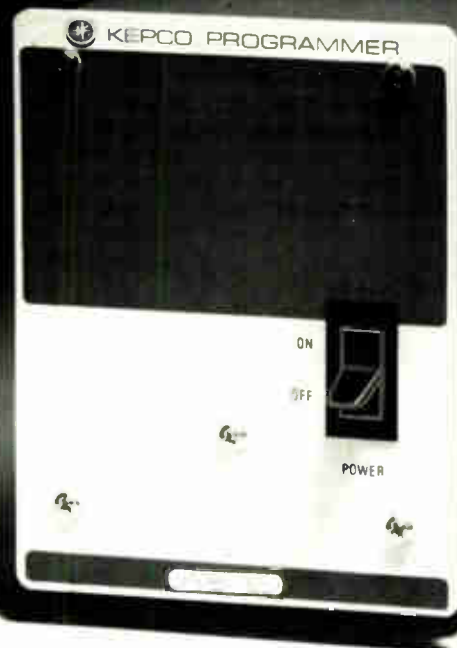
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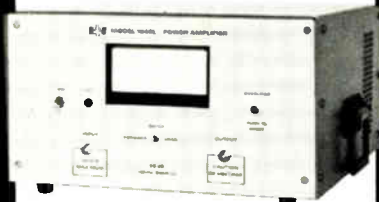
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Readers' comments

Make it natural

To the Editor: It was with much anticipation that I turned to the article on the Forth programming language ["Forth's forte is tighter programming," March 15, p. 114], since I had heard that it is becoming popular. However, I am very disappointed with it and would like to venture a few comments about Forth and language design.

Forth departs from conventional language design in ways that are not all beneficial. Reverse-Polish notation (RPN) is fine for command languages (for example, hand-held calculators), but it is not the way that we normally think. We think and write in algebraic in-fix notation.

Forth users are forced to express themselves first in the algebraic form they are used to and then hand-translate to RPN or else to contort their normal way of thinking and expressing themselves to conform to Forth. Why put users to this extra trouble for a peculiar notational requirement?

Compilers can do the translation from in-fix to post-fix notation with almost trivial effort. Therefore let the user express himself in a way that is more natural and familiar, and let the compiler do the work of translation.

In the example given of a general function to compute the formula $(2 * X - 14) * (X + 5)$ for any argument X, the user is required, in Forth, to engage in such activities as duplicating the top word of the stack, swapping the top two words of the stack, and hand-translating from the form $(2 * X - 14) * (X + 5)$ to the form `DUP 2 * 14 - SWAP 5 + *`;—all of which are unrelated to the problem at hand. In a somewhat more conventional language, one might write something like `FORMULA = (2 * X - 14) * (X + 5)`, which would look much more like the problem originally conceived by the user.

Another serious point of departure is the form of the IF statement. The use of THEN as a closing delimiter in the IF...THEN form reverses the natural order of the word "then" and the true clause associated with it,

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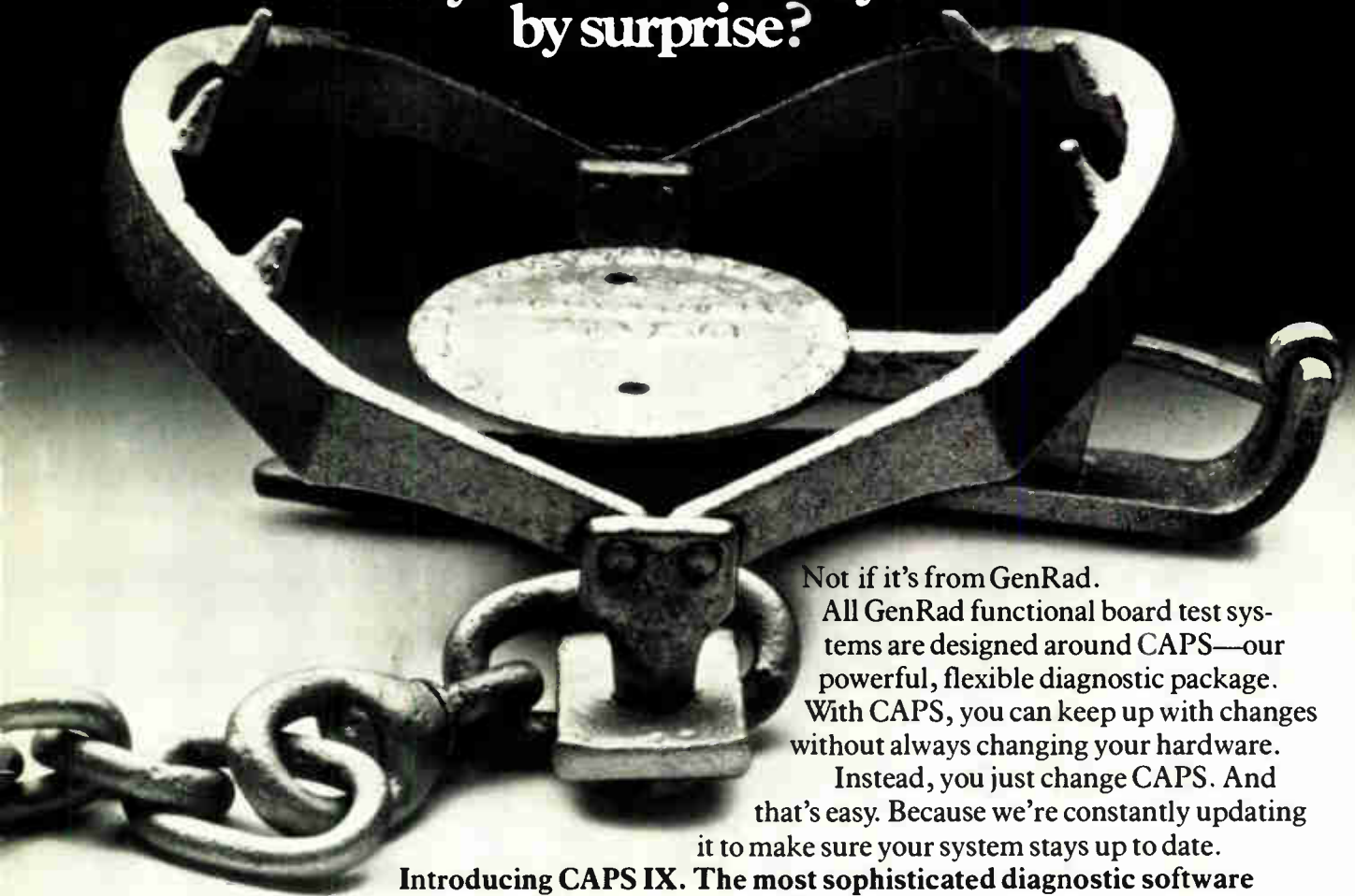
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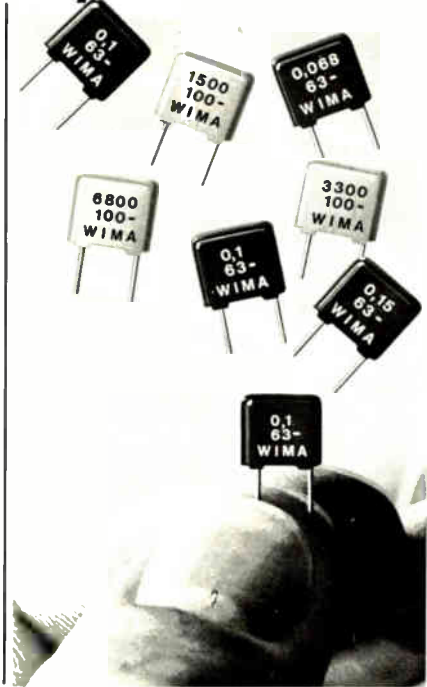
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Readers' comments

and in the form IF... ELSE... THEN they are completely separated by an intervening false clause.

This is a completely unnatural and counterintuitive arrangement. Once again, if a compiler can translate from a form natural for a human being to use into a form more efficient for the computer to use, why should one be forced to express oneself in such an awkward fashion?

Lest readers think that I am on a high horse against everything in Forth, I would like to say that there are some good features. An incremental compiler that translates each new statement into a dictionary definition is very useful. It allows for greater interaction with the user and makes the software-development task much less tedious. The indirectly threaded coding and dictionary structure makes for a compact representation of programs and is potentially very powerful.

The ability to call machine-language subroutines easily is also extremely useful, almost necessary, in microcomputer applications. In addition, language extensibility has long ago been shown to be beneficial. And nothing needs to be said about the benefits of structured programming language.

However, all these features can still be provided by a language that is much less awkward to read and write—one that permits the expression of solutions in a form much closer to the notation that a user is familiar or comfortable with.

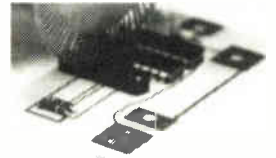
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Correction

Cray Research Inc., Chippewa Falls, Wis., will be manufacturing printed-circuit boards to meet the requirements of its Cray-1 and new Cray-2 processor. It seems the Cray-2 designers are experimenting with unusual boards—something original-equipment manufacturers aren't willing to produce in small numbers. But the company maintains it has no intention of making semiconductors, nor does it desire to do so, despite earlier reports (Electronics Newsletter, May 24, p. 34).

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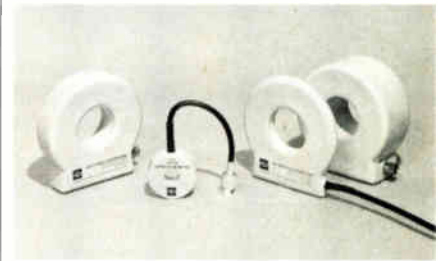
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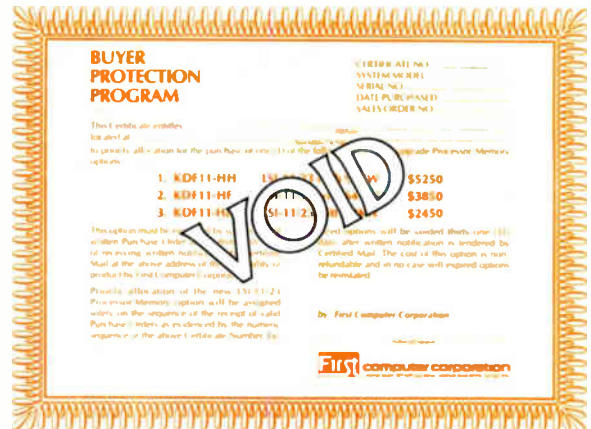
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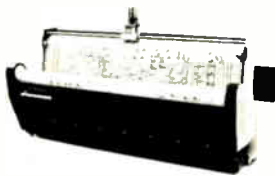
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People

Grisanti takes the pulse of General Automation

Management consultant Frank Grisanti of Grisanti and Galef in Los Angeles is well known for his work in helping to bring troubled companies back to financial health. His latest patient is General Automation Inc., Anaheim, Calif., ranked as the sixth largest minicomputer maker (1978 sales: \$98 million). The 58-year-old industrial engineer was named president in May after company founder Lawrence A. Goshorn was ousted as president and chairman of the board.

Using a medical analogy, Grisanti likens his task to the "diagnostic procedure of the internist." But instead of blood-pressure and pulse, he looks for the vital signs of a viable company: "It must have a quality product or service that is offered on a timely basis. There must be a market willing to pay a price that will net you a decent [profit] margin, and this market must be readily accessible to the company. That is, your company should offer something different."

General Automation seems to be suffering not from any one illness but from a malaise that keeps it from being as profitable as some believe it might be. Some trace this back five years to an abortive attempt to apply silicon-on-sapphire semiconductor technology. That failure precipitated the resignation of then-president Raymond J. Noorda and Larry Goshorn's reelection as president in August 1975, a position he had earlier relinquished.

Management turnovers. Since then, a series of management changes has caused almost semiannual turnovers. And though the company has been profitable and its hardware generally regarded as competitive, the cost of software development related to thrusts into the distributed-data-processing arena are said to be draining the company financially.

Grisanti says it is too early to discuss his prescription for the company, adding that "it's not really sick, like some companies I deal

with." He is particularly impressed by the employees. "If the quality of the people measures a company, General Automation has inherent strength," he says. But he cautions that he will be weeding out whatever dead wood there is.

Some analysts also look for him to narrow the company's marketing. It now spans a range of automation functions from numerically controlled machine tools through electronic transfer of funds to industrial processing, each demanding different and expensive software to be developed.

Grisanti's record of successes inspires confidence. Among electronics firms, he is noted for turning around MSI Data Corp., a maker of handheld data terminals, and Mohawk Data Sciences, a maker of data-entry terminals.

The curing of General Automation will take time. "I can't do much in less than a year," Grisanti says.

China will buy computers, says Pertec's Roby

Every industry visitor to the People's Republic of China—that vast potential market—comes back with bits of information that tantalize U.S. firms. The latest news comes from veteran computer marketer, Jerry Roby, who toured computer factories, learning about the needs of the Chinese computer industry. Along with two company engineers, the international sales manager for microsystems at Pertec Computer Corp., Irvine, Calif., was part of a 10-person group touring China May 19 to June 3 as guests of the Chinese Electronics Society.

Low-end machines. "My strong impression is they're looking first for low-end computing and peripherals," Roby says. "That represents their best chance to get technology at little cost. They don't really want products, but they're realists who know they have to buy one to get the other." Not by coincidence, Roby's company makes desktop computers and disk drives.

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People

Small computing capability at factory level is an absolute necessity, but it does not exist now and must be brought in, in Roby's view. "Their plan is to leapfrog into LSI, from the early-60s level where they are," he says.

Perspective. Roby, 39, has a long perspective with which to judge Chinese aspirations. He spent 12 years in international computer operations for Sperry-Univac Corp., including a stint as director of technical operations in Europe. He was also in Russia as part of Univac's abortive attempt to sell mainframe machines there.

On his trip to China, he had three advantages. First, his tour, organized by the California Trade Delegation, a private company in San Francisco, was much smaller and more flexible than most. Secondly, he speaks Mandarin Chinese, which he learned at the University of California, Berkeley, as an oriental language major. "You have to have someone who speaks the language in your party, because the quality of translation is so poor," he advises. "If you have the language, you're free to go around virtually anywhere. We got on buses and went downtown in Peking by ourselves."

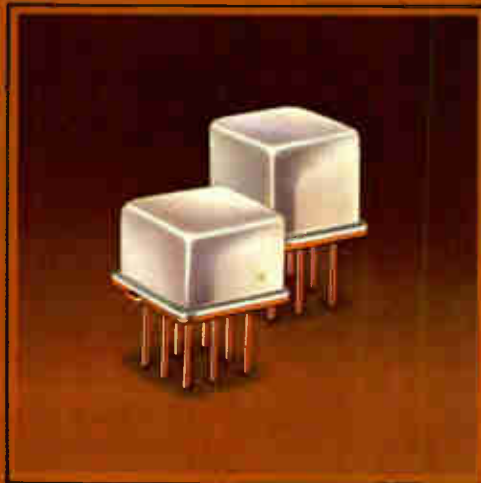
And the Perteq trio did not go to China empty-handed. "We took equipment with us, a PC2000 computer and 5¼-in. double-sided, double-density drive and spares," he says. "They loved it." This played to the lack of hands-on experience with equipment, a serious lack in China, in his opinion.

Roby does not believe the Chinese are "pulling back in their trade intentions," as some recent observers claim. Instead, they seem to him to be pausing while their electronics industry decides how best to proceed. "For one thing, they have to specialize manufacturing as we do. Right now, every single factory I saw makes every component. The duplication [of effort] is astronomical.

"But they are wide open to advice, in contrast to Russia which has a defensive attitude," he concludes. "They do not lack knowledge, just equipment," he concludes.

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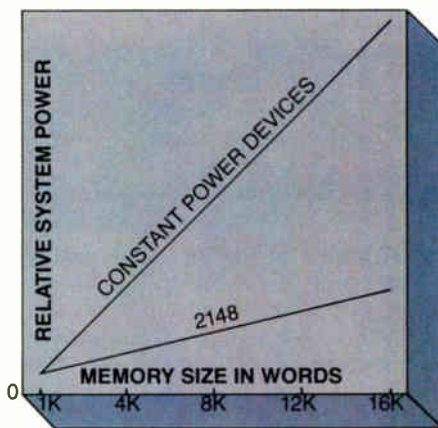
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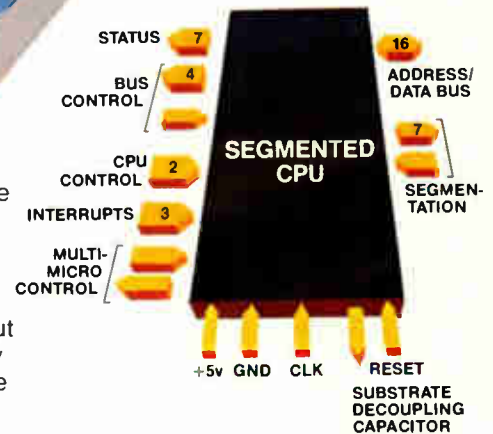
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The fireworks have just begun!



Is it possible to protect software?

As computers proliferate, so do the programs run on them. And along with this proliferation of software, the problem of its protection is growing. Yet on the face of it, there appears to be no completely safe legal means of protecting computer programs.

Essentially the way to put a shield over software is to use a patent or a copyright; another way is by claiming a trade secret. Each method has certain disadvantages; the protection is difficult either to obtain or to police and enforce.

The courts and the Government have not made the situation any easier. Once again it appears that the technology of which software is an integral expression has outdistanced the law and its interpretations. In short, there does not seem to be a well-defined place for software in the legal system, at least not as far as protecting programs is concerned.

Patents, for example, are difficult to secure. The courts have decided that programs are "mathematical" and as such unpatentable. Only very special applications have passed the test. What's more, patent attorneys agree that once a computer program receives a patent it is difficult, perhaps impossible, to spot infringements. In addition, the courts of late have been generally unsympathetic to companies claiming infringements. All this leads one to the conclusion that taking out patents on software does not look particularly attractive at present.

The situation in copyrights is unsettled. The new law governing copyrights that took effect in January 1978 gives short shrift to software, almost as though the Congress wants to avoid the issue. As a result, to use a lawyer's phrase, "the law is unclear" on the protection of computer programs because of the ambiguity that has been codified in

Section 117 of the copyright statute.

The new law has made copyright of any material extremely complicated; for software, it is virtually impossible. At the very least, the Congress should take another stab at clarifying copyright protection of software. But, based on how long it took to prepare the version now on the books, this rethinking is not likely to happen in the near future.

Considering the difficulty of gaining patent protection and the ambiguity surrounding copyright rules, the law of trade secrets may be the best alternative for covering computer programs. There are a number of factors making this choice the attractive one. For one, a trade secret need not pass a "novelty" test; that is, there are no standards requiring uniqueness in a trade secret—it need only be a piece of information that others do not possess. More importantly, a trade secret need not be disclosed as part of the process of gaining protection, as is the case with patents and, to an extent, copyrights.

Instead, the developer maintains the trade secret safeguards—internally to keep the information from getting out and externally by license agreements. And, although the courts have not been particularly kind in patent infringement cases, they have been favorable in trade secret litigation. The main problem with software licenses is that agreements have to be airtight with very specific terms covering applications. Nevertheless, until the law—and its enforcement—catches up with the complexities of computer software, the best protection seems to be in the direction of trade secrets. At the same time, the software issues should continue to be placed before the lawmakers, so that eventually there may be specific standards for protection.

EASY DESIGN



Pro-Log maps the STD BUS route to easy microprocessor design.

First checkpoint, our STD BUS Information Packet.

It explains the basics of the new STD BUS and Pro-Log's Series 7000 cards. With these, you can build 8-bit microprocessor systems around a standard bused motherboard. You can choose the functions in your system, the memory type, even the microprocessor type by simply selecting from among Series 7000 cards. The STD BUS is 86 lines wide, compatible with Pro-Log's standard 4-1/2 inch by 6-1/2 inch edge-connected cards, supported by other manufacturers, and freely available to the industry.

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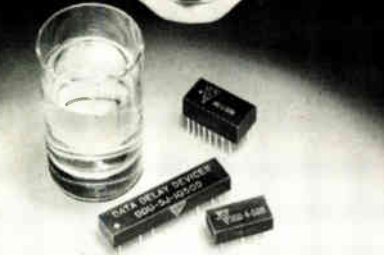


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Meetings

Second Joint Intermag—Magnetism and Magnetic Materials Conference, IEEE and American Institute of Physics, Statler Hilton Hotel, New York, July 17-20.

Video and Data Recording Conference, IEEE et al., University of Birmingham, Birmingham, England, July 17-20.

Computers in Manufacturing Conference, American Institute of Industrial Engineers (Santa Monica, Calif.), Jack Tar Hotel, San Francisco, July 30-Aug. 1.

IEECE—Intersociety Energy Conversion Engineering Conference, IEEE, Sheraton Boston Hotel, Boston, Aug. 5-10.

Pattern Recognition and Image Processing Conference, IEEE, Hyatt Regency O'Hare Hotel, Chicago, Aug. 6-8.

Siggraph '79—Sixth Annual Conference on Computer Graphics and Interactive Techniques, Association for Computing Machinery (New York), Hyatt Regency O'Hare Hotel, Chicago, Aug. 6-10.

Conference on Simulation, Measurement and Modeling of Computer Systems, National Bureau of Standards et al., University of Colorado, Boulder, Colo., Aug. 13-15.

International Conference on Parallel Processing, IEEE, Shanty Creek Lodge, Bellaire, Mich., Aug. 21-24.

23rd Annual International Technical Symposium and Exhibit, The Society of Photo-Optical Instrumentation Engineers (Bellingham, Wash.), Town and Country Hotel, San Diego, Calif., Aug. 27-30.

Comcon Fall '79—19th IEEE Computer Society International Conference, IEEE, Capital Hilton Hotel, Washington, D. C., Sept. 4-7.

Second International Fiber Optics and Communications Exposition, Information Gatekeepers Inc. (Brook-

line, Mass.), Hyatt Regency O'Hare Hotel, Chicago, Sept. 5-7.

Dielectric Materials, Measurement and Applications Conference, Institution of Electrical Engineers (London), University of Aston, Birmingham, England, Sept. 10-13.

Fall Conference, USE Inc. (the organization for those who use Sperry Univac's series 1100 computers, Bladensburg, Md), Diplomat Hotel, Miami, Fla., Sept. 10-14.

25th Annual Holm Conference on Electrical Contacts, Illinois Institute of Technology (Chicago), Palmer House, Chicago, Sept. 10-12.

Ninth European Microwave Conference, Institution of Electrical Engineers (London), The Brighton Centre, Brighton, Sussex, England, Sept. 17-21.

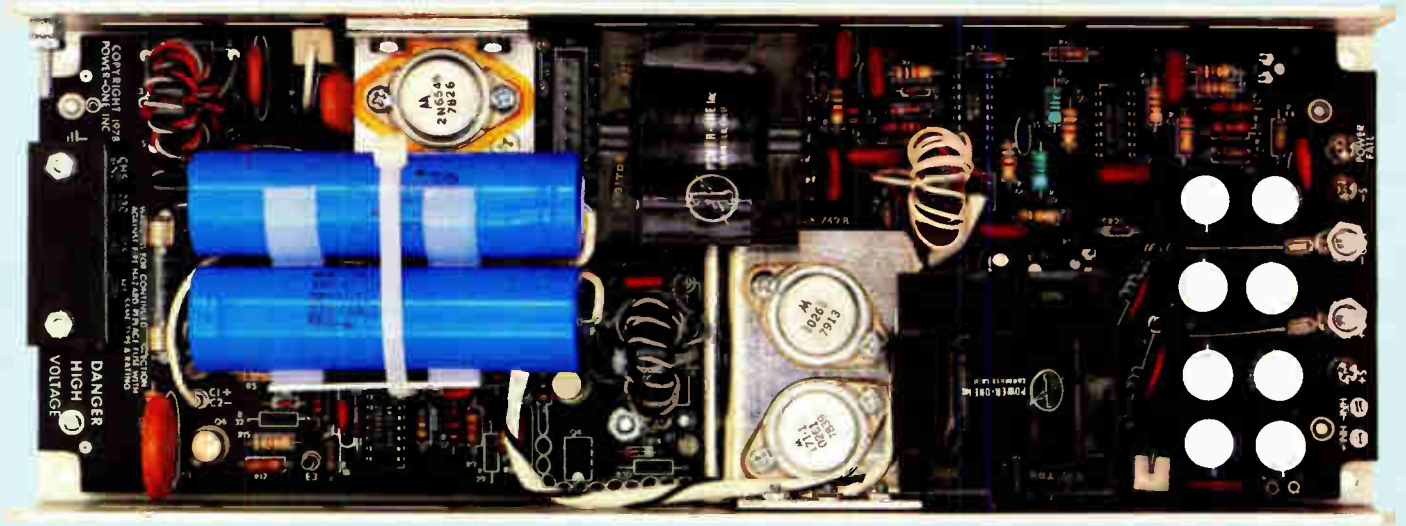
Wescon/79 Show and Convention, IEEE and Electronic Conventions Inc. (El Segundo, Calif.), Brooks Hall and St. Francis Hotel, San Francisco, Sept. 18-20.

Autotestcon—Automatic Support System for Advanced Maintainability Conference, IEEE, Radisson Hotel, Minneapolis, Sept. 19-21.

Short courses

Microprocessor design courses featuring instruction on the Z80 and 8085 microprocessors and the STD bus will be given during July through November in 10 cities including Seattle; Anaheim, Calif.; Boston; Cleveland; and Munich. For information, contact Becky Serdehely at Pro-Log Corp., 2411 Garden Road, Monterey, Calif. 93940, or telephone (408) 372-4593.

Time and Frequency User's Seminar sponsored by the National Bureau of Standards, Boulder, Colo., Aug. 29-30. For information, contact George Kamas, National Bureau of Standards, Boulder, Colo. 80303, or telephone (303) 499-1000, ext. 3378. The registration deadline is Aug. 1.



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of inputs, our dual range design permits either 115 or 230 VAC operation without changing jumpers.

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Switching frequency: 28KHz — stable as a rock. Size: a mere 4.88 x 13 x 2 inches — more watts to the inch and more power for the buck. The price: \$250 for single units.

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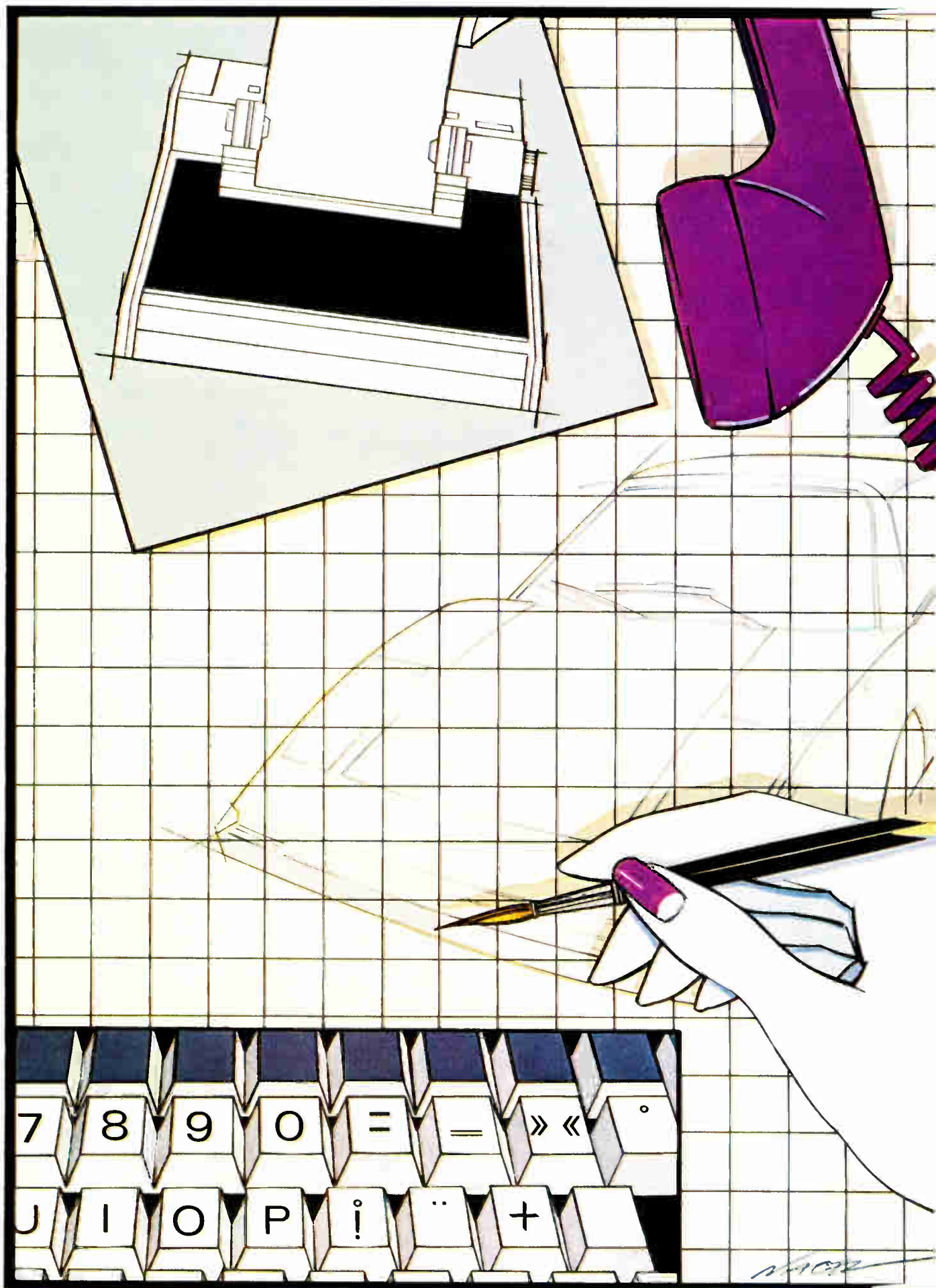


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It starts with an idea—your inspiration to add the power of microcomputer intelligence to create a new product, revitalize an existing one, add features or reduce manufacturing costs. What's the next step? Do you choose a computer-on-a-chip for performance, for capabilities, for economy... Or, should you first evaluate program development tools that can shorten the design cycle, reduce product development costs and simplify the whole process?

The answer: Intel. Because your success depends on choosing the right microcontroller and the right development support. That's why our 8048 family of microcontrollers has set industry-wide standards for performance, features and economy. And our Intellec system is far and away the most advanced approach to program development in microcomputer history.

A full spectrum of solutions

A microcontroller is a remarkable device—a complete computer-on-a-chip, with program storage, data memory, input/output circuitry and CPU, all etched on a single chip of silicon. Such integration, though, makes it important to choose the right family of microcontrollers with the right combination of features for your growing application needs.

Intel makes that easy by putting the industry's broadest selection on your palette. The foundation of the family is the 8048, the microcontroller that won industry acceptance for the computer-on-a-chip concept. Then there's the world's easiest to use microcontroller, the 8748. It's an 8048 with on-chip program memory

the user can erase and reprogram over and over, during development or when customizing products.

For sheer performance, nothing can match the 8049, with twice the program and data memory of the 8048—and twice the speed.

The 8021 provides full 8-bit power for cost-sensitive applications. And our newest family member, the 8022, offers a unique extra for control applications—an on-chip analog-to-digital converter.

All seven existing (see chart) and future Intel® microcontrollers provide software compatibility to permit easy upgrade flexibility. All operate from a single +5V supply and are fully supported by the Intellec development system.



Color yourself successful— with the Intellec® System

There's no quicker way to go from inspiration to completed masterpieces than our Intellec development system. From design through production, the Intellec system manages, cuts and compresses the development cycle. For new users, the Intellec system's sophisticated simplicity ensures a smooth transition to microcomputer technology.

At the Intellec console, you write programs using 8048 family assembly language, and let the system automatically translate them into appropriate machine code for your system application.

8048 Microcomputer Family

Model	Program Memory (Bytes)	Data Memory (Bytes)	I/O Lines
8021	1K ROM	64	21
8022	2K ROM	64	28
8048	1K ROM	64	27
8748	1K EPROM	64	27
8035 (External)		64	27
8049	2K ROM	128	27
8039 (External)		128	27

The ICE-49™ emulator brings a new standard of in-circuit emulation to the Intellec system, ending the frustration and time lost trying to merge hardware and software. From the beginning of your development cycle, the ICE-49 module provides you with a "diagnostic window" into the 8048 microcomputer family. And with the Intellec Development System you can emulate on-chip functions inaccessible by other approaches.

Get started today

Find out more about Intel microcontrollers and the Intellec system. Call your local Intel sales office or distributor for more information about our next MCS-48™ microcontroller workshop in your area. Or write for our complete Success Manual for Single-Chip Users. Intel Corporation, Literature Dept., 3065 Bowers Avenue, Santa Clara, CA 95051. 408/987-8080.

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The HP 2621: sim

Simple doesn't have to mean unsophisticated. The proof is in our new CRT terminal, the HP 2621.

Before building it, we took a long, hard look at the way you use a simple terminal. Then we took the knowledge gained in more than 10 years designing computer products and applied it to engineering an interactive character-mode CRT terminal from the user's point of view.

The outcome was actually two models. The HP 2621A, which sells for \$1450. And the HP 2621P, which has a built-in printer, costs \$2550. You obviously want the sharpest display made. So we used the 9x15 character cell you see on every HP CRT terminal, including the top-of-the-line. And, to help you look back at the data you've entered, we provided two full pages of continuously scrolling memory.

We designed the keyboard like the familiar typewriter, so you don't have to waste time relearning it. We built in eight function keys, too. These control the cursor, rolling and scrolling. And, to make life easier, they're labeled on the screen for self-test, configuration, display and editing.

Editing? On a simple terminal? Certainly. We included character and line insert and delete, clear line and clear display. And, since the 2621 keeps your input separate from your CPU's, you can edit data before sending it to the computer. All without writing a line of system software.

Since flexibility is important in interfacing, we included a user-definable return key that will send your computer whatever code it expects. We also made our terminals compatible with RS232C and Bell 103A, and

able to communicate with your CPU at 110 to 9600 baud.

If you need hard copy at your fingertips, take a look at the HP 2621P. With a keystroke, its built-in 120 cps thermal printer will deliver a printout from the screen in seconds.

So why don't you check out the HP 2621 by calling the nearest HP sales office listed in the White Pages. Or send us the coupon. Then see for yourself how sophisticated a simple CRT terminal can be.



Try this on your favorite CRT! With the 2621P, you just hit a key and in seconds you have hard copy of your CRT display. The built-in thermal printer prints upper and lower case at up to 120 cps.

The 2621's bright, high-resolution CRT, with enhanced 9x15 character cell, displays the full 128-character ASCII character set, including upper and lower case, control codes, and character-by-character underline, in 24 80-character lines.

Eight screen-labeled preprogrammed function keys magnify the power of the 2621's keyboard. Preprogrammed functions include editing, terminal configuration, printer control and self-test.

To make numeric data entry faster and easier, we put the 2621's numeric keypad right in the middle of the keyboard. And the 2621's familiar 68-key keyboard is almost as easy to use as a typewriter.

- I'd like to know more about HP's new 2621A and 2621P with built-in hard copy.
- I'd like to see HP's new 2621A and 2621P with built-in hard copy.
- I'd like to know more about HP's complete family of terminals.

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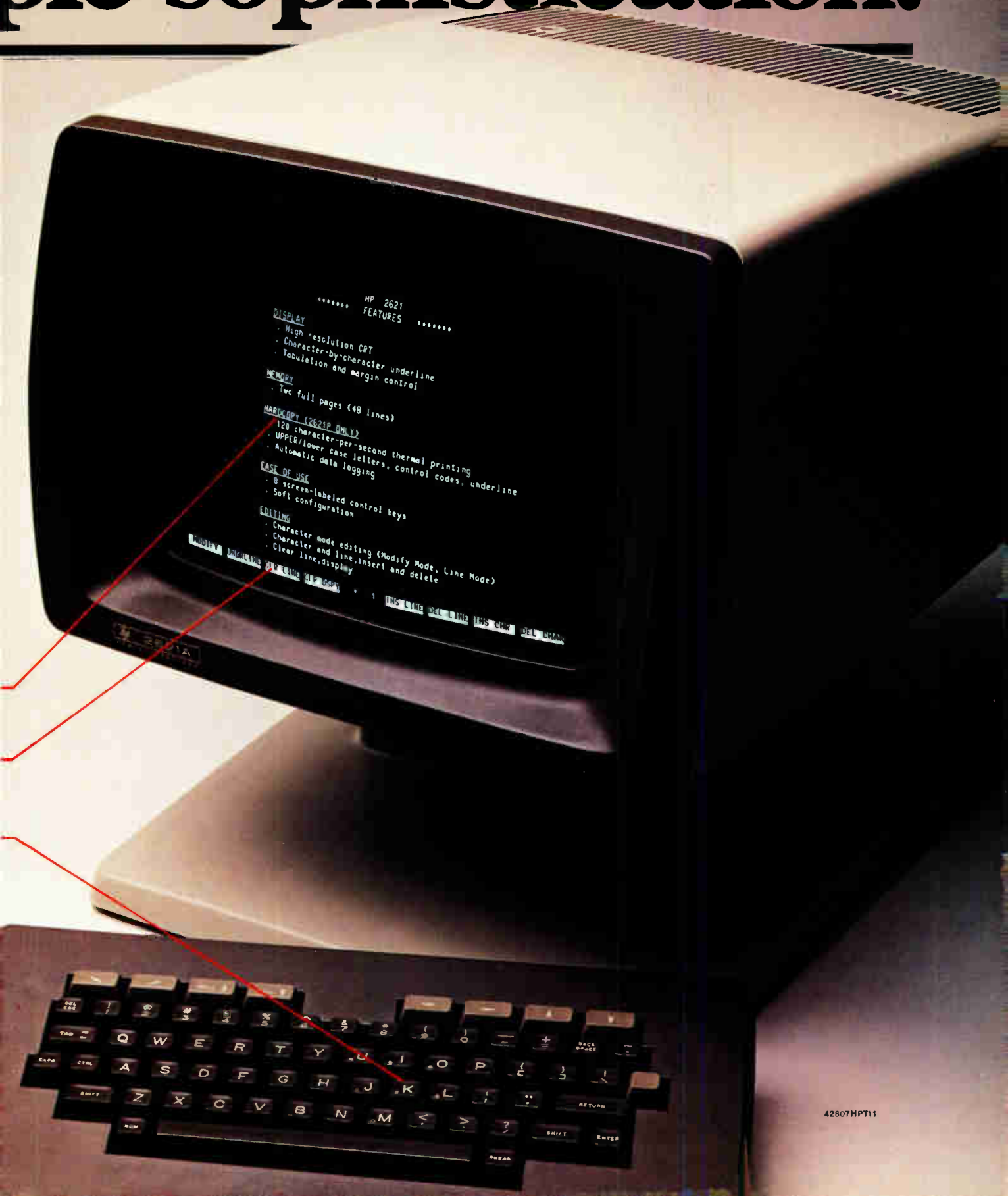
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***** HP 2621
FEATURES *****

DISPLAY

- . High resolution CRT
- . Character-by-character underline
- . Tabulation and margin control

MEMORY

- . Two full pages (48 lines)

HARD COPY (2621P ONLY)

- . 120 character-per-second thermal printing
- . UPPER/lower case letters, control codes, underline
- . Automatic data logging

EASE OF USE

- . 8 screen-labeled control keys
- . Soft configuration

EDITING

- . Character mode editing (Modify Mode, Line Mode)
- . Character and line insert and delete
- . Clear line display

INS LINE DEL LINE INS CHR DEL CHR

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more than 25 years. But, we're far from just a "custom" house. We've already helped solve a lot of "standard" problems that you'll find in our just-published catalog of non-custom digital and linear bipolar ICs.

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Low level amplifiers—differential amplifiers—level detectors—DC to DC converters—timing circuits—motor speed controls—optical detector systems—camera controls—flip chips.



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Circle 32 on reader service card

HP developing magnetic-bubble memory and tester

Although Hewlett-Packard Co. apparently hasn't yet committed magnetic-bubble memory technology to a commercial product, the computer and instrument maker will give some details of its development in two papers at this month's second joint Intermag conference in New York City. The papers may surprise some in the industry; the Palo Alto, Calif., company had been assumed to have dropped research on the emerging technology. **One paper will describe a second-generation in-house automatic tester** that originally was designed to analyze a 10-channel, 1.6-megabit bubble-memory chip since abandoned, but can easily be converted to test other chips with different architectures. The other describes the performance of a newer swap-replicated gate structure for a 1-megabit chip, still in development, that uses sine-wave drive fields instead of the triangular-wave drive fields others use.

16-K static RAM added to Inmos catalog

A 64-kilobit dynamic random-access memory is not the only type of device due to be hatched in the Rocky Mountains next year by Inmos Corp., the British government-backed semiconductor firm that is barely out of the nest itself. A parallel design effort under way at the company's Colorado Springs, Colo., offices is believed to involve a high-speed 16K-by-1-bit static RAM that is reminiscent of the fast MOS static parts pioneered by Intel Corp. As the first in a planned **family of original-design memory and erasable PROMs**, the 64-K dynamic and 16-K static parts are to be available in small quantities during the first quarter next year.

SMC to press Japanese firms for license fees

Watch for Standard Microsystems Corp. to push a Japanese licensing campaign for its Coplamos n-MOS process. SMC has just received a Japanese patent for the process [*Electronics*, Oct. 26, 1978, p. 100], which involves the use of self-aligned, field-doped, locally oxidized structures. Japanese semiconductor makers have been using similar processes, and SMC president Paul Richman told its annual meeting that **Nippon Electric Co. and Hitachi Ltd. in particular objected to the granting of the patent**. Since receiving its first U. S. patent in 1973, the Hauppauge, N. Y., firm has pursued a vigorous licensing program.

New TRS-80 language springs from Forth

The dictionary-organized computer language called Forth [*Electronics*, March 15, p. 114] has been optimized for the Radio Shack TRS-80 microcomputer system. Said by its manufacturer to be the most widely used microcomputer in the world, with more than 100,000 sold, the TRS-80 may account for 30% to 50% of the market—including a fast-growing segment in the small-business area. The new Forth, called MMSForth, is available from stock, costs \$60, comes on a single diskette, and **offers what its developers call professional-level programming for the hobbyist computer**. Available from Miller Microcomputer Systems of Natick, Mass., MMSForth claims greatly enhanced keyboard command interpretation and sophisticated quick, number, and string sorts. It has its own built-in disk operating system; it can work with arrays and double-precision arithmetic, and promises enhanced graphics capability, among other features. A Miller spokesman says that not only can the new version do more than the Basic supplied with the TRS-80, but on similar tasks is up to 15 times faster.

Signetics to join CRT controller chip set makers

The growing worldwide market in cathode-ray-tube terminals, expected to jump from 1.15 million in 1979 to 1.55 million next year, is attracting business from semiconductor makers who supply large-scale integration chips in an effort to cut down the component count in CRT controller circuits. **Most recent to show interest is Signetics Corp., Sunnyvale, Calif., which plans to put out a flexible four-chip set that will sell for about \$35 in volume and work with low- to high-end terminals.**

IBM moves to discourage renting older products

In a move viewed by analysts as aimed at encouraging customers to purchase rather than rent its equipment, International Business Machines Corp. has raised rental and lease prices 5% for most of the products and services from its Data Processing and General Systems divisions. The Armonk, N. Y.-based firm had **noted earlier that customers were tending to lease rather than purchase equipment**, a trend that is adversely affecting plug-compatible computer makers as well (see p. 54). Most notably exempt from the increases are the new 4300 processors, the System/38 small-business computer, and the 8100 distributed processing system.

SEL reaches agreement with array processor house

Watch for an OEM agreement between Systems Engineering Laboratories Inc., Ft. Lauderdale, Fla., and Computer Signal Processors Inc., Burlington, Mass., that would effectively combine the firms' data-processing capabilities. The multiyear agreement, initially worth about \$10 million, may be signed within the week; **the result would be a line of SEL-marketed computer systems with Computer Signal array processors supplied as standard equipment.**

64-K RAM from Motorola heads for add-ins

The MCM 6664, Motorola's 64-kilobit random-access memory, will be put to use soon by the company's Memory Systems group in Austin, Texas, on new add-in memory board products designed for use with minicomputers built by Digital Equipment Corp. **Formal product introductions are expected this quarter on the new boards.** One will be populated with 144 of the 64-K chips, providing a full megabyte of capacity for use with DEC's PDP-11 series machines. Another will provide 1/4 megabyte of storage for use with DEC's LSI-11/23. The move by Motorola to use fully functional 64-K RAMs on board-level products follows introduction by Texas Instruments last month of new board products that use partially good 64-K chips built by TI, providing 32 kilobits of storage per chip [*Electronics*, June 7, 1979, p. 44]. The move also follows display of a prototype 1-megabyte board using the Motorola 6664 by Prime Computer Inc., Wellesley Hills, Mass.

Addenda

Hewlett-Packard Co.'s Data Terminals division in Cupertino, Calif., is understood to be **developing a color-graphics capability for its 2600 series of interactive display terminals** to be available in the second quarter of 1980. Also understood to be in the final development stages is a new low-priced (around \$2,000) intelligent graphics terminal, the 2622, that would supersede the current 2640 display station. A spokesman for HP's Computer Systems Group neither confirms nor denies the reports. . . . Britain's **Thorn Electrical Industries Ltd. is acquiring Systron-Donner Corp., Concord, Calif., for \$27 million.**

Technological leadership.



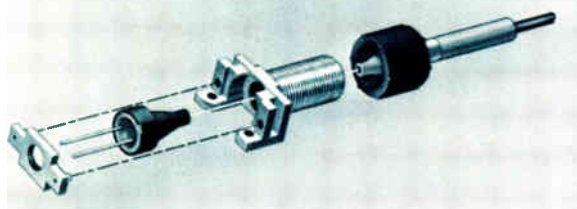
Motorola introduces Straight Shooter:TM the practical, easy-going fiber-optic semi that's right on target.

You know how pigtail and dome-lens fiber-optic devices are – klutzy assemblies here, inefficiency and handling hassles there, high cost all over and suddenly you're in the dark.

Well, Motorola technology's taken dead aim on all that and changed it, thanks to the new MFOE102F to MFOD402F family of ferruled plastic fiber-optic devices.

This IR gallium-arsenide emitter/silicon detector team offers excellent coupling efficiency, unprecedented low cost and ease of service through an entirely new, state-of-the-art packaging concept.

Ease and efficiency with FOACs



What we've done is bonded the semiconductor die directly to an 0.008" (200 micron) optical fiber and mounted it in a resilient plastic package with a polished end. This end, pressfit into a custom-tailored AMP Optimate connector, forms a common alignment surface with the optical cable. This fiber-to-fiber coupling, combined with the precise alignment demanded by the metal connector housing, ensures maximum light transfer between polished ferrule end and optical cable. Easy. Quick. Automatic.

We call the whole assembly a FOAC (Fiber Optic Active Connector) and, by gosh, it honestly increases coupling efficiency up to 50 times over older, TO-18-type systems!

Other performance includes speeds up to 20 megabits/sec and systems up to 5 km in length.

All you add is love

The Straight-Shooter package concept controls the source-to-fiber and fiber-to-detector light coupling variables for you, a task most difficult with conventional dome-lens units. The only remaining variables are diameter and numerical aperture of cables according to transmission requirements. Coupling losses (about 2 dB with similar core) are easily calculated.

We think you'll like this the most.

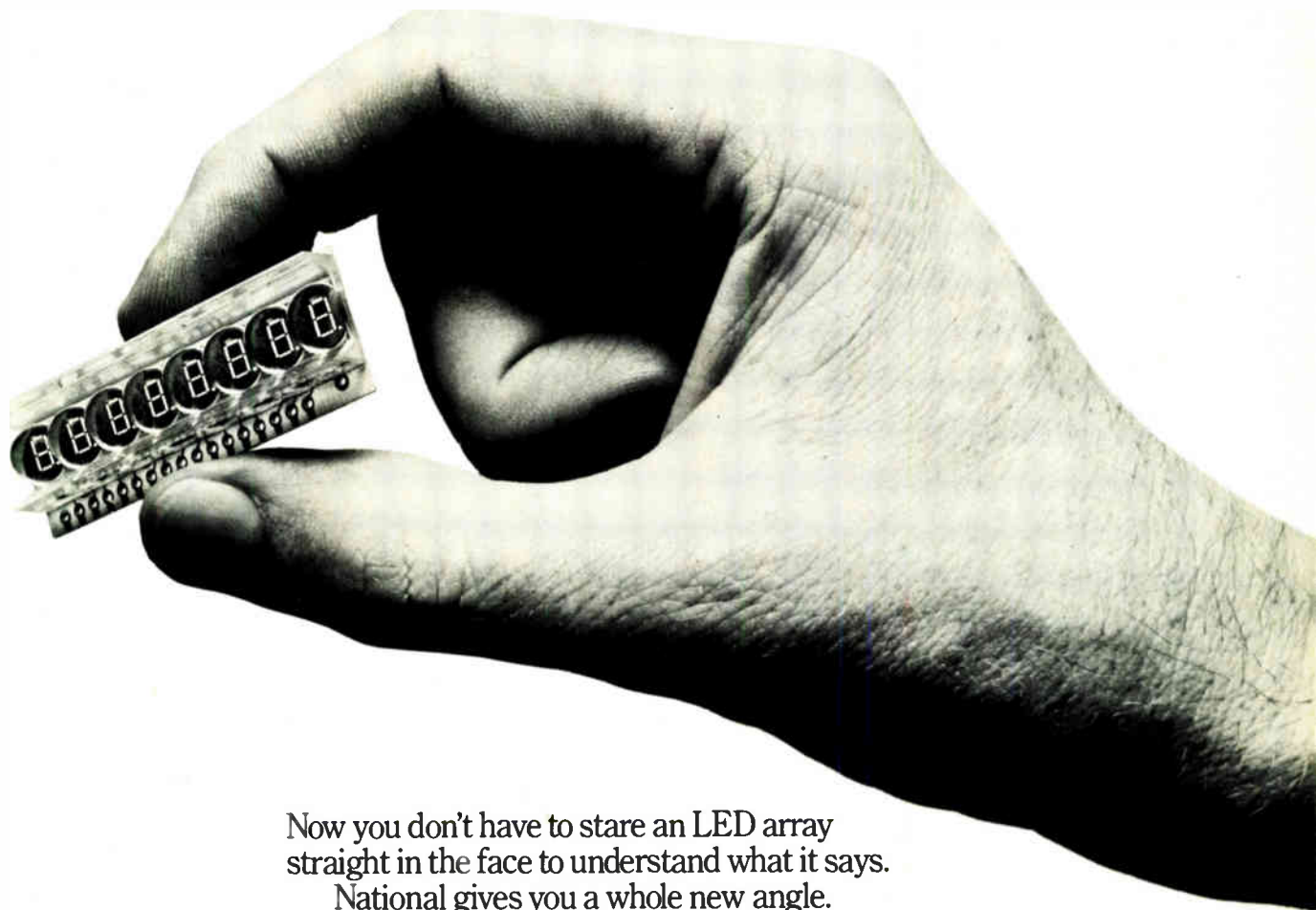
Right now we've got an emitter capable of 70 μ W output and four detectors with sensitivities from 1.5 mV/ μ W to 6,000 μ A/ μ W, with more in development. One of the detectors offers IC technology with detector/pre-amp capability. Contact Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036 for straight-shootin' data on all. Or see our friends at AMP for fiber-optic Experimenter's or Designer's kits. Either way, a bull's eye for

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We've incorporated a wide angle, easy reading lens into our 8-digit 0.14 inch and three digit 0.10 inch displays.

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So if you'd like to see the light, ask about our little numbers. And about their little cost.

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Circle 37 on reader service card

The Power Paradox:

The AC power your computer needs in order to operate is also a major cause of computer error, malfunction and damage.

The computers that control your operations (and therefore your profits) are designed to operate from a clean, steady supply of ac power.

This ac power *must* be kept within manufacturer-specified tolerances in order for the computers to operate properly and safely.

In fact, the U.S. Department of Commerce states that "if a computer's voltage exceeds 120% [of the rated voltage] for a duration as short as 1 to 10 milliseconds, the computer will make errors."¹ Unfortunately, interruptions and disturbances of this nature are commonplace occurrences within most computer facilities.

A comprehensive study of power line disturbances which affect sensitive computerized equipment was conducted by two IBM researchers. They concluded that such disturbances occur on an

average of 128 times each month.² For users of computer-based equipment, power disturbances can and do create a variety of costly problems.

Effects upon data processing computers.

When these power disturbances occur in your data processing center they can cause entry errors, program changes or loss, head crash, data loss, the generation of false or garbled data, the need to rerun programs, and computer downtime.

Effects upon computerized process control equipment.

Process control equipment is also vulnerable to power disturbances. Common problems created by these

disturbances include improper batch termination and even program changes. The program changes can result in the repetition of process errors and in downtime while equipment is being reprogrammed.

Effects upon energy management systems.

Most energy management systems use small computers to make energy-saving decisions, but their effectiveness can be offset by these same disturbances. Program changes and errors may prevent useful operation of these systems as energy savers.

Thus, the computers your company depends on to reduce operating costs actually may be increasing them.

Topaz power peripherals can protect all of your computers.

Topaz can provide the power peripherals specifically designed to keep your company's data processing, process control and energy management computers from making costly power-related errors.

And if you manufacture computers or computerized equipment, Topaz peripherals can make your product more reliable as well as reduce the requirements for needless service calls.

Immediate delivery and guaranteed solutions to power problems have made Topaz the leading computer power peripheral company in the world.

For more information about Topaz and its products:

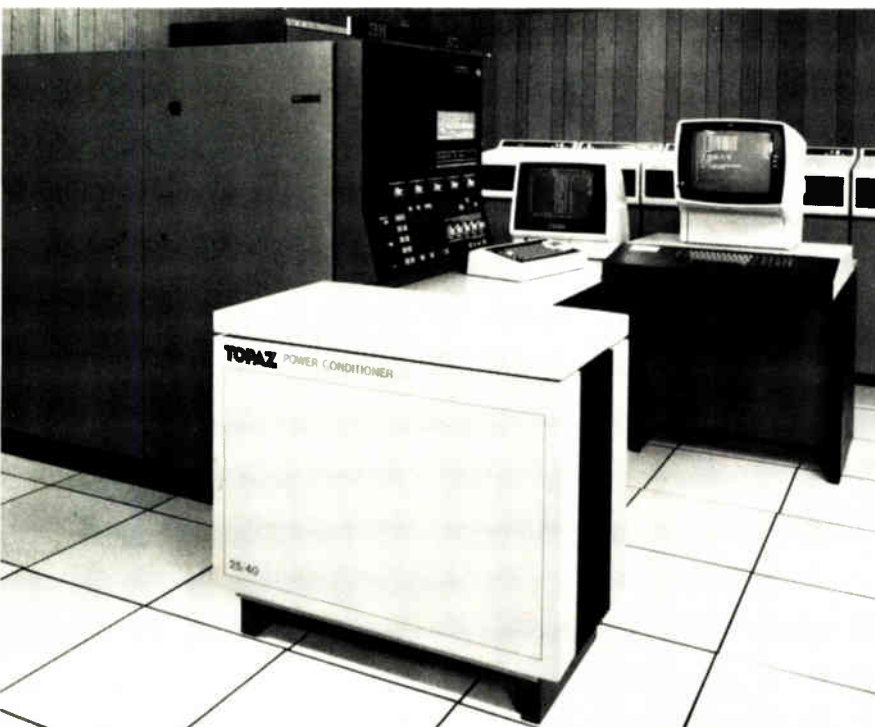
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Electronics/July 5, 1979



Topaz peripherals solve the power paradox by conditioning normal ac power for your computer and computer-based equipment.

New peripheral chips extend the range of 16-bit microprocessors

by John G. Posa, *Microsystems & Software Editor*

AMD will produce extremely flexible support devices for Z8000 that function with little or no CPU intervention

New peripheral chips coming from Advanced Micro Devices Inc. signal the future course for microcomputer systems: their processing capabilities will ultimately rival those of today's minicomputers.

AMD, of Sunnyvale, Calif., has disclosed details of three new chips it is designing as part of its agreement to second-source Zilog Corp.'s 16-bit Z8000 central processing unit, presently in pre-production silicon. (A fourth, yet to be chosen, will also be designed.) The chips combine a complexity and performance level simply not called for by the older generation of 8-bit CPU families, but necessary for taking full advantage of 16-bit processor chips.

Indeed, one of the devices, a burst-error processor (BEP) will keep up with data rates to and from hard disks, an impossibility with the 8-bit families. The other two chips, controllers for cathode-ray-tube (CRT) displays and direct memory access (DMA), will—like CPUs—fetch their own commands from memory.

Off-loading. The devices satisfy the primary objective of peripheral chips: to off-load the CPU to free it for other tasks. The 24-pin BEP does its job even without direct connection to the CPU. Designed for serial burst-error detection and correction in a microprogrammed disk controller, it monitors the data stream between the disk and a buffer. When

a data block moves from the buffer to the disk, the BEP appends bits on the end of the block in accordance with a polynomial calculation designed to detect and correct errors.

The BEP also scrutinizes data going into the buffer. It performs the arithmetic again and compares the two results. If they are different, it signals the controller, which enters memory and inverts the bad bits.

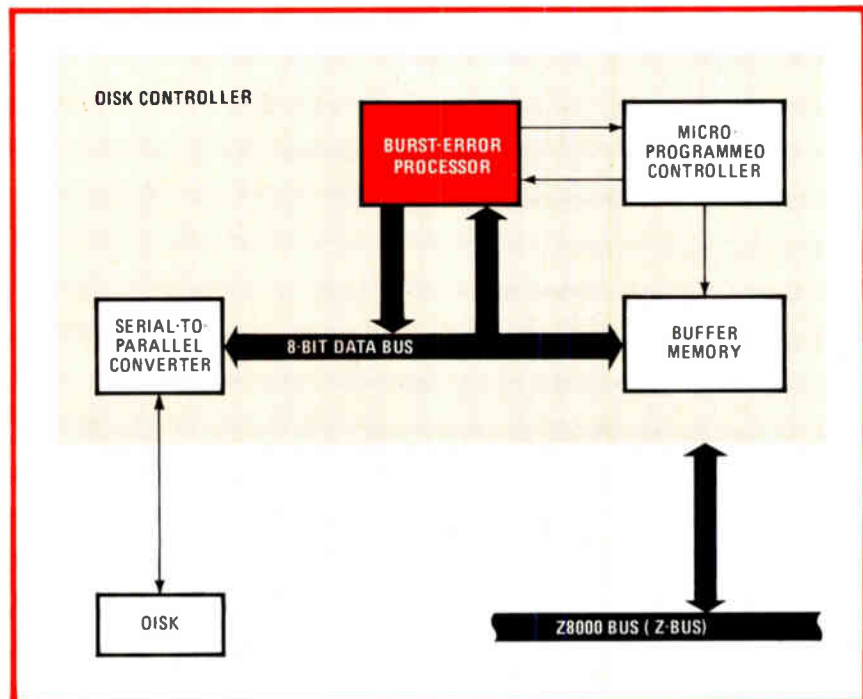
"Block lengths can be long, maybe 1,000 bits," says Joe Kroeger, manager of MOS peripheral applications at AMD, "and data rates can be as high as 20 megabits per second. Current hard-disk transfers occur at about 12 to 14."

Unlike the BEP, the 48-pin CRT

and DMA controllers interface directly with the Z8000's Z-bus.

"There are two things about the DMA function that we are doing differently," explains Kroeger. "First, the chip can load its own control parameters, and second, it gives you the option to chain DMA operations together automatically." Other DMA chips usually require CPU directives for these operations.

AMD's DMA chip refers to a memory location specified by the CPU and finds blocks of instructions that indicate, for example, the source and destination of data. After data transfer, the controller can go back, load a new set of control parameters, and continue. Moreover,



Error repairer. One of AMD's peripheral chips, a burst-error processor, watches data pass between disk and buffer. It signals the controller to correct any bad bits it finds.

if the user has an 8-bit peripheral chip and a 16-bit memory, the DMA controller will absorb bytes and connect them to form words.

AMD is also striving to include new features in its still unfinished CRT controller design. For example, it wants to provide for variable spacing between characters and words for pleasant-looking text with justified margins. The screen can have multiple windows with any number of cursors in each. And AMD wants high resolution: at least a full type-written page for word processing and, maybe, 132-character lines to reproduce a computer printout.

Zilog, which will second-source

the AMD chips, is also working on four peripheral chips that AMD will second-source. Included are a memory-management unit, serial communications controller, counter input/output, and a first-out buffer with on-chip input/output [*Electronics*, Dec. 21, 1978, p. 81].

Ten chips in all, then, will be available from the two firms, including both segmented and nonsegmented versions of the Z8000 CPU. The peripheral chips are all +5-v-only, 5-micrometer devices. "The BEP will be out before year-end, the CRT controller before 1981," says Kroeger, "and the others at intervals in between."

the commercially successful PDP-11.

The new MCF machines will be first to use Ada, the military's new higher-order language (see "Ada means secure savings") when the equipment is developed in mid-1983. The AN/GYK-12 is a machine originally developed by Litton Industries for tactical fire-control systems.

Although the MCF effort took on a triservice cast in November 1978 with the signing of a memorandum of understanding by the Army and the Air Force Systems Command and the Naval Material Command, the Army's battlefield requirements clearly put it at the front of the program. Standardized hardware and software are a necessity for battlefield computers of the future, the Coradcom commandant said during a panel at the Armed Forces Communications and Electronics Association (Afcea) meeting in Washington late last month.

The danger. "Can we survive on an automated battlefield? If tactical computer types are allowed to proliferate, the answer may be no," Dickinson warns. "There are currently 18 different computers proposed for battlefield systems, 16 of them from different sources."

To maintain competition, the Army will buy from multiple vendors central processors, memory, and other modules built to MCF specifi-

Military

Army to award first contracts soon for standard military computer family

The U. S. Army is ready to roll with its plan to develop a new standard military computer family (MCF) for the battlefields of the future. Three to five competitive contracts will be awarded for the initial, seven-month phase, to begin in September.

The contractors will supply form, fit, and function specifications for air-transportable tactical hardware—from micro to maxi systems—their operating environment, and required outputs and will also develop a standard interconnection, or bus. The emphasis will be on producibility and integration.

The winner will be named MCF systems integrator for the second, 17-month-long phase. This phase "will consist of development of the AN/GYK-12 and AN/UYK-41 tactical systems by multiple suppliers, demonstration of hardware interchangeability, and development of logistics and production plans," says Maj. Gen. Hillman Dickinson, whose Communications Research and Development Command (Coradcom) in Washington, D. C., is heavily involved in the initial effort.

Basis. The architecture for the triservice MCF derives from Digital Equipment Corp.'s PDP-11 comput-

er. The Maynard, Mass., company's approach was selected following a competition with IBM Corp.'s System/370 and Interdata Inc.'s 8/32 machines [*Electronics*, Oct. 14, 1976, p. 77]. Dickinson calls it "a major accomplishment" that the Army has "reached agreement in principle with Digital Equipment for use of proprietary data and patents on the AN/UYK-41," a military version of

Ada means secure savings

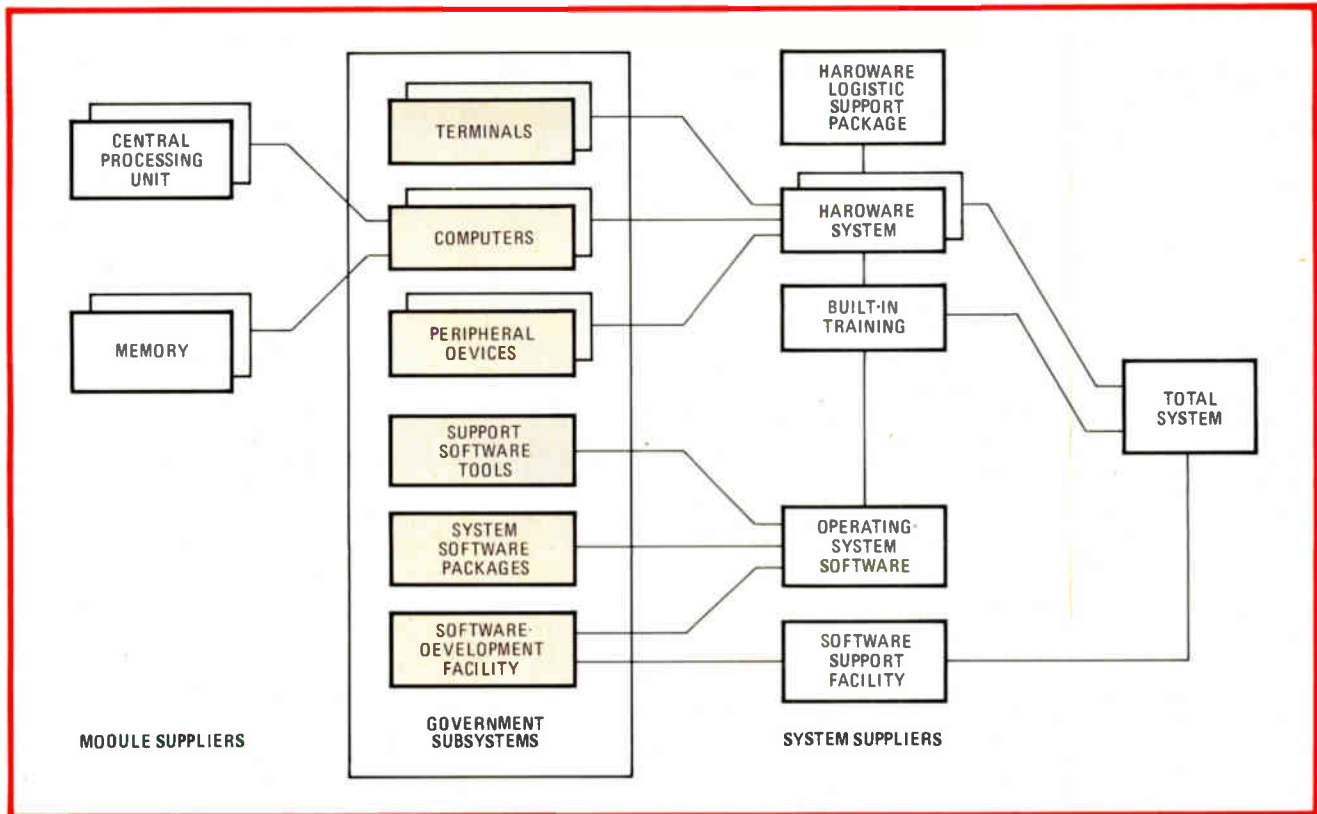
Military computer makers in the audience at a recent Afcea panel on battlefield automation and communications shuddered at Maj. Gen. Hillman Dickinson's disclosure that the cost of new software "is now approaching 90% of system cost." Then they listened carefully to the Army's plan to cut those costs sharply in developing the new military computer family (MCF).

The main method will be the adoption of Ada, the new military software package [*Electronics*, May 24, p. 64], as the standard language. With Ada, the Army believes it can not only cut out proliferation of separate software, but also eliminate duplicate expenditures for integrating systems, logistics, and software support, training, and built-in test equipment.

Besides saving money, Ada should provide tight data security through the use of a secure operating system being developed by Ford Aerospace & Communications Corp. for the National Security Agency. This system "is based on the Bell System's Unix operating system used on the PDP-11/70 and VAX-11/870 family of computers," Dickinson explains.

Another software package for MCF will be called Tacexec (for tactical executive). This development program, whose procurement terms are now being put together, should also help cut software costs.

-R. C.



Separation. The Army's MCF program separates module suppliers from the system prime contractors. Vendors will compete to supply CPUs, memory, and other modules, to be assembled into subsystems. The prime contractors will then integrate the total system.

cations (see figure). "The modules will be integrated [by the military] into subsystems and provided, along with peripherals and terminals, to system integrators, who, using software provided by software developers, will provide an integrated computer system," he explains. "We thus have a standard computer with modules acquired from multiple suppliers—giving us the required competition."

Software. A major driving force behind developing a standard computer family is the rapidly rising cost of software. Beyond employing the new Ada language (formerly called DOD-1)—for which the first compiler will be acquired by Coradcom—the Army is undertaking a common software development and support system (SDSS) as a separate effort. "We hope to place an order this fiscal year" for SDSS computers that will include a dual PDP-11/70 or VAX-11/780 linked by the Bell System's Unix operating system for development and testing the Ada

compiler and other components interacting with software," Dickinson says.

-Ray Connolly

Bubble memories

TI readies 16-megabit Air Force systems

The first bubble-memory system designed for disk and drum replacement in large military computer applications may be just around the corner. Late last month, the Air Force Avionics Laboratory at Wright Patterson Air Force Base, Ohio, was expected to take delivery on three 16-megabit units believed to be the largest bubble memory systems built to date.

Supplied by Texas Instruments Inc. under a \$2.6 million contract, the systems are part of the continuing Air Force bubble development program spearheaded by the lab's Electronic Technology division. The

systems are slated to provide the Air Force and Navy with their first hands-on bubble experience.

Arrived. For some military mass-memory applications, bubble technology has just about arrived in terms of proven reliability and cost-effectiveness, says Stuart Cummins, bubble memory program manager at the avionics lab. He would not be surprised to see bubble systems with much larger capacities than 16 Mb popping up soon as replacements for slower, less reliable disk and drum memories in some Air Force and Navy ground-based and shipboard computer applications.

Development work directed toward bubble use in spaceborne applications is also under way at the Air Force and the National Aeronautics and Space Administration as well. For example, NASA is currently working with Rockwell International Corp. on programs aimed at using bubbles in spacecraft data recorders.

As the culmination of development work begun in mid-1975, the



Handshake. Air Force project manager Stuart Cummins (left) greets TI's Greg Sloat. A 16-megabit bubble memory built for the Air Force and its test panel are on the table.

systems delivered by TI contain 140-kilobit chips that use 5-micrometer bubble technology, which has since been surpassed by 3- μ m bubble techniques used in today's 256-K devices available commercially from TI and Rockwell. Several new component and system features of the Air Force units may well be applied in future commercial bubble products, indicates Greg Sloat, program manager for the project in TI's Central Research Laboratories, Dallas.

High art. For one thing, the bubble components run faster than today's commercial devices. The chips are driven at 250 kilohertz, compared with 100 kHz for commercially available TI bubble chips and 150 kHz for Rockwell's 256-K devices.

Also worth noting is a piggyback scheme developed for housing two of the 140-K bubble chips in a single package that is smaller and has a lower profile than TI's commercial single-chip bubble packages. The two-chip-per-package approach doubles the data output rate per package compared to a single-chip implementation of equal capacity.

In combination with the faster operating rate, Sloat points out, the piggyback approach enabled TI to meet Air Force requirements for a 4-megabit-per-second output using less power and space than if more but slower devices were paralleled.

The 140-K chips employed by the

Air Force systems are fabricated in a block-replicate arrangement using 188 minor loops of 745 bits each. Allowing for expected redundancy requirements, each two-chip package equals about a quarter megabit of good storage capacity.

The bubble packages are mounted eight to a 6-by-9-inch board, with eight boards in a system. They are housed along with four additional support cards in a standard ATR box measuring 10.125 inches wide, 7.625 in. high and 19 in. deep.

Multifaceted. Each 47-lb system is controlled by an integrated injection logic version of TI's 9900 16-bit microprocessor, the SBP9900A. Each system is also equipped with standard Air Force and Navy interfaces, as well as a TI interface for hooking to a 990 minicomputer-based multipurpose bubble test system developed under the program. The 300 watts required to operate the system was about double the desired goal, a result, in part, Sloat says, of the large-number of integrated circuits needed for the interfaces. A test system is also part of the TI contract.

The Air Force is already evaluating bids for a next-generation system for airborne applications. The contract award is expected by early fall; goals include higher memory density, wider operating temperatures, and less power consumption, says Cummins. -Wesley R. Iversen

Fiber optics

Connector uses curved approach

TRW Inc. is throwing an actual curve at the fiber-optic connector market. Last month, it introduced a new connector for single fibers that requires no polishing or application of epoxy to the fiber ends yet, it says, achieves less than a 1 decibel loss per connection.

That is a 50% or better improvement over competing products, which require relatively complicated field assembly. What's more, the new connector will be comparatively cheap—\$50 per fiber pair. Traditional fiber-optic competitors, such as Bunker Ramo Corp.'s Amphenol RF group in Danbury, Conn., however, say they will introduce equivalent low-loss connectors in the next year.

Crucial to the Optalign hermaphroditic connector designed by TRW at its research and development laboratories in Philadelphia is a curved guideway delineated by a bundle of four fused-glass rods. Unlike connectors from AMP Inc., which use a ferrule-type alignment, the male plug holds the guideway, made up of two curved sections linked by a straight portion; the female position holds a spring-loaded piston.

Forced together. Optical fibers are threaded into the far end of each connector half, and the two halves plugged together (see p. 44). As that happens, the pistonlike section of the female plug retracts and the fiber is forced into the guideway in the male plug. The fiber ends butt up with a pressure of almost 300 pounds per square inch, high enough to keep the fiber ends in firm contact and guard against signal losses.

With the curved guideway, the fiber is under a slight strain and, along the straight portion, becomes tightly wedged in one of the V-groove-like interstices formed by the four-rod array, explains TRW. The two fibers in the connector can then

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Circle 43 on reader service card

Electronics review

Globe-Union engineering vice president and DOE, that should give ETV-1's batteries a lifetime of about 30,000 miles or three years, at which time a new battery pack would cost approximately \$700.

Each battery pack recharge will add about \$1 to a consumer's electric bill, based on utility rates of 4 to 5 cents per kilowatt-hour and a discharge level of about 80%, says DOE. Recharging takes 10 to 12 hours using a 110-volt, 15-or-30-ampere current or 6 hours with a 220-v, 60-A line. "However, we figure most commuters could get back up to full charge in about two hours since most urban drivers average about 31 miles a day," says one ETV-1 engineer. **-Ray Connolly**

Communications

Pieces of plastic filter phone voice

For the highest voice quality, digital speech transmission requires analog filters at the transmitting and receiving ends, even if the system includes digital filtering. At the transmitter, the analog filter limits the band of frequencies that are converted to digital equivalents; at the receiver, the filter cuts out unwanted harmonics produced by the digital-to-analog

conversion that produces speech.

Researchers at Bell Laboratories have contrived an inexpensive way to achieve this filtering by simply adding a plastic voice filter to the Western Electric microphone housings—the familiar mouth- and ear-pieces of the ordinary telephone. Such filters will replace the inductance-capacitance filters generally used in mobile radiotelephones and in the loop systems connecting the subscriber to the phone company office, according to James L. Flanagan, head of the acoustics research department at Bell Labs in Murray Hill, N. J., which is working on the new passive filters.

The design, still in an experimental phase, could be especially cost-effective in dedicated per-channel applications of digital voice systems, he says. As the cost of analog-to-digital and digital-to-analog conversion has decreased, this filtering has become a sizable portion of the total cost of the digital system.

Disk stack. The filter is a stack less than an inch high of different-diameter disks with different-size holes. These give the mechanical filtering for the voice frequencies provided by inductors and capacitors for electrical signals. The disks can be simply injection-molded or stamped out like the housing itself. Disk diameter and thickness are calculated from classic acoustic fil-

ter theory, according to Flanagan.

The filters fit up against the microphone, and the combination of housing and filter readily meet the Bell System's channel bank specifications for digital voice transmissions, Flanagan says. Further work, which is being pursued at the labs by groups in addition to Flanagan's, is needed before the filters are ready for use. **-Harvey J. Hindin**

Consumer

U. S. TV output up, imports decline

Orderly marketing agreements that curb exports to the U. S. of color TV receivers from Japan, Taiwan, and South Korea are helping to change the face of U. S. television manufacturing operations, say Commerce Department officials.

For one thing, the competitive position of U. S. manufacturers has been improved by foreign exchange rates that make imports more expensive. For another, the number of Far Eastern producers with U. S. production and assembly facilities is expected to rise to nine before year's end. Two Taiwan firms—Tatung and Sampo—and Japan's Hitachi and Sharp have disclosed plans to set up American plants by then. Five other Japanese manufacturers already operate U. S. plants—Sony, Matsushita (Quasar), Sanyo, Toshiba, and Mitsubishi (MGA).

As a result, the American output of color TVs in January-to-March exceeded 2 million sets for the fourth consecutive quarter—the first time that has occurred since color TV's introduction in the 1950s.

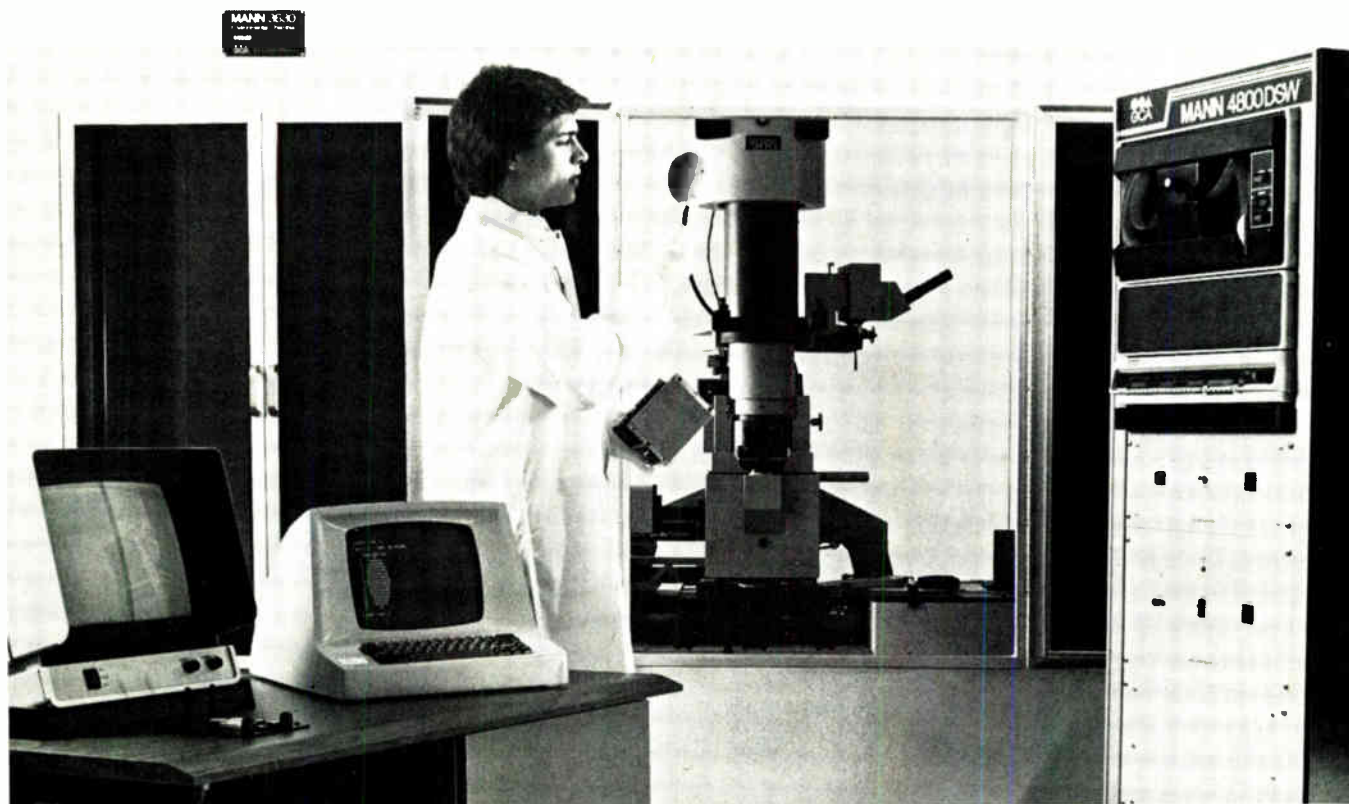
Meanwhile, three U. S. manufacturers—GTE Sylvania, RCA, and Zenith—are importing more partially completed color receivers from their own plants in Mexico for final assembly in this country.

That is the story behind the numbers showing a 23.5% decline in imports of completed color TV receivers in the first quarter of 1979 from the comparable 1978 period. In

Filter. Three plastic disks inserted in telephone between outer housing and conventional microphone act as a voice filter in experimental design from Bell Laboratories.



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the same period, incomplete set imports jumped 55% from the 1978 level to 601,452, with more than 58% of the total coming from Mexico. Most incomplete sets contain no picture tube.

The details. While the first-quarter count of fully assembled color TV imports hit a low for the last eight quarters, domestic production rose to 2.1 million units—up 12.7% from the 1978 level. The combination of higher domestic output and lower imports cut the import penetration level to 16.4%, the lowest posted in any quarter of the past three years.

Imports from Japan fell nearly 60% to 132,000 units from the first 1978 quarter, while Taiwan's shipments fell by one third to 77,000. South Korea was the only major foreign supplier to register a gain with shipments up 194% from 49,000 to 147,000 completed sets. Orderly marketing agreement limits with Korea and Taiwan only became effective Feb. 1, officials note, whereas Japan has been subject to such curbs since July 1977.

The agreements with all three countries will expire on June 30, 1980. Officials suggest that it probably will be unnecessary to renew them because most foreign producers are expected to be operating U. S. plants by then. **-Ray Connolly**

Software

Plans afoot for Master's programs

This fall, Texas Christian University intends to offer the initial course in a new 40-hour graduate program leading to a master of software engineering degree. Billed as the first such program of its kind, the offering by the Fort Worth, Texas, university is expected to be the forerunner of similar programs elsewhere as the nation's colleges and universities move to train specialists to work on today's complex software projects.

"There's an acute industry need that has not been filled by existing

computer science programs," observes Richard Fairley, associate professor of computer science at Colorado State University in Fort Collins, Colo. Fairley heads up a 16-month-old subcommittee of the Institute of Electrical and Electronics Engineers' Computer Society that expects to issue a final report this fall outlining a curriculum for the software engineering program. A committee of the Association for Computing Machinery is also working to develop a similar model curriculum, though its report is not expected until later.

New focus. Traditional master's programs in computer science tend to focus on research issues that prepare the individual for Ph.D. work. But the new software engineering curricula will concentrate on teaching skills needed to produce and maintain high-quality software, on time and within budget projections, in a corporate environment.

Essentially, says Fairley, the IEEE model curriculum will try to condense the experience of corporate software officials. Obviously, this will mean a heavy dose of courses on modern methodologies such as structured programming, modularization, software specification development, testing, and the like. But equally important in the training of a corporate software engineer are the kinds of communications and management skills needed for work on team software projects.

"There's an intrinsic difference between a single-man software project and the multiperson projects that are common in industry, and one of the reasons why computer software projects have been typically over budget is that people haven't understood this difference," observes Alex Hoffman, director of TCU's computer science program.

As a result, he says, TCU's curriculum will include communications-oriented courses with subjects ranging from "effective participation in small, task-oriented groups" to methods of writing effective software user documentation. Also included will be management and economics-related courses dealing with software

development costs, hardware-software tradeoffs, and techniques for managing software development personnel and resources.

In demand. Industry sources confirm the demand for more college-trained software engineers. "Software engineering with management overtones is a very recent development, and we need as much of it as we can get in the colleges," says Douglas S. Johnson, an official in Texas Instruments Inc.'s advanced software technology department in Dallas.

To date, industry has been attempting to take up the slack through in-house training and the use of independent companies that offer seminars on software engineering techniques. Several universities are also said to be developing full-blown graduate programs like the one planned at TCU. In general, Fairley notes, software engineering textbooks have become much better lately and should be adequate for the new educational thrust. "My biggest concern now," he concludes, "is whether there will be enough qualified instructors available to teach these courses." **-Wesley R. Iversen**

Military

New missile would bank to turn

Researchers at the Air Force Armaments Laboratory, Eglin Air Force Base, Florida, have completed simulations of the guidance and control sections of a new generation of air-to-air missiles known generically as bank-to-turn types, or BTTs. As described by Air Force personnel, BTT missiles sound almost unbeatable. BTT missiles would have a semi-elliptical cross section and an overall shape like that of a lifting-body reentry vehicle, but with additional stub wings, unlike the finned, pipelike missiles of today.

Rather than throwing over a rudder and skidding through a turn as present missiles do, BTTs would roll left or right, changing the direc-

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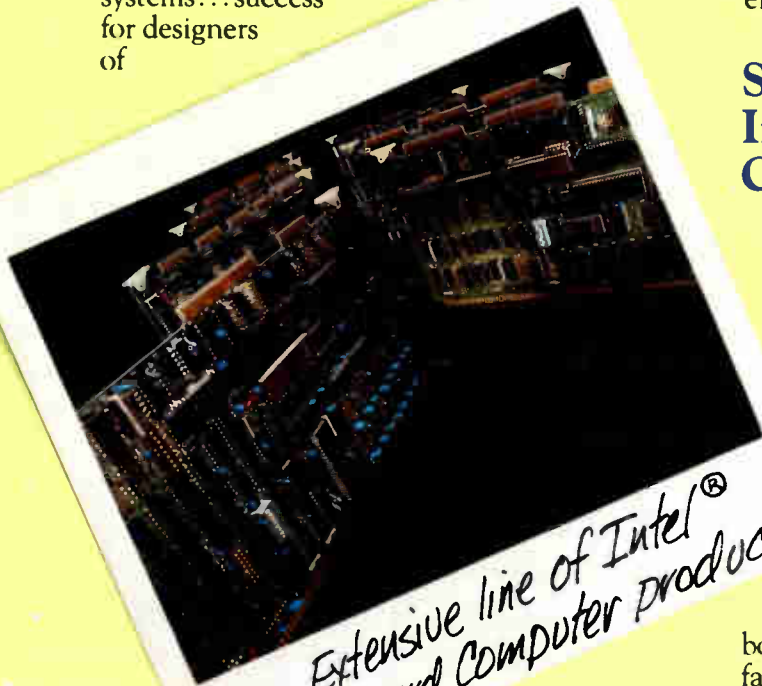


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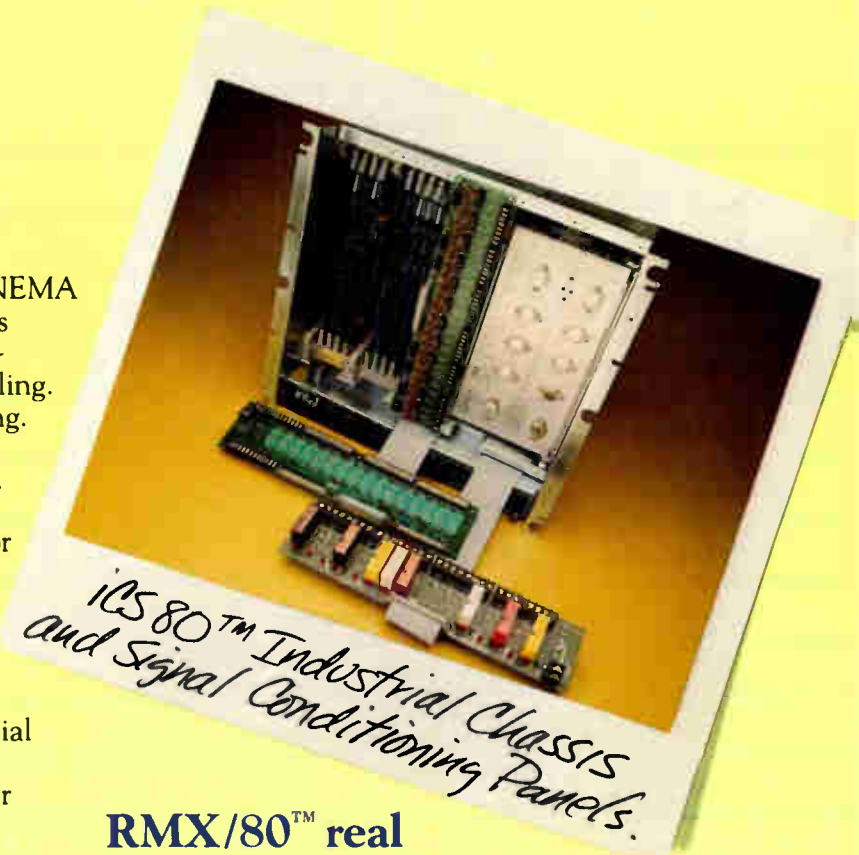
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tion of lift exertion, and so use lift rather than brute force to turn.

The payoff would be immense. Roll rates could exceed 600° per second, and BTTs could turn so tightly that they would pull more than 100 gravities. In addition to their high maneuverability, BTTs would have a speed range of Mach 0.5 to 2.5, an acceleration of 100 g or more, an altitude range from sea level to beyond 50,000 feet, and other advanced characteristics. All those, according to one Air Force source, would make a BIT "almost impossible to evade."

Difficulties. There was concern at first that this very performance would also make BTTs almost impossible to produce. For example, the common analog autopilots used in most missiles are fast-acting, but when confronted with a combination of fast changes in speed, g force, missile weight (with fuel burn-off), altitude, and tracking commands, analog units are just not adaptable enough. There were also questions about the ability of infrared seekers to hold onto a target through the tight maneuvers possible with a BTT. Finally, there was doubt about the speed, stability, and durability of existing control-surface actuators.

So the Eglin engineers assembled key sections of a simulated BTT missile in their lab using analog and digital computers to control the simulation, a test stand for an infrared seeker, dummy controls for the actuators to operate, and a digital autopilot to "fly" the simulated missile. The IR seeker came from the Missile Systems division of the Raytheon Co., Bedford, Mass.; the autopilot from the Columbus (Ohio) Aircraft division of Rockwell International Corp.; and the actuators from the Airesearch Manufacturing division of Garrett Corp., Los Angeles.

An IR source was suspended above the seeker head, which was then mounted in a six-degree-of-freedom gimbal system. The source was then moved by the Eglin computers to simulate the movements of a plane in wild evasive action. The seeker tracked the source successfully, held

lock, and generated accurate pointing data for the digital autopilot, which in its turn commanded the actuators at their dummy controls. The Eglin computers monitored the movements of the dummy control surfaces and found them accurately tracking their projections.

It all worked, and all with off-the-shelf hardware, according to Robert M. McGehee, BTT development program manager. That means that the electronics are equal to the task and that the BTT program can proceed with airframe optimization. Some wind-tunnel tests have already been performed, and the Air Force is closing in on a configuration with far less drag than present missiles—one more advantage of the BTT approach.

-James B. Brinton

Automotive

Ford to offer electronic door locks

Motorola Inc. will supply the bulk of up to 100,000 microcomputers to help lock and unlock the doors on Ford Motor Co.'s 1980 luxury cars. The microprocessors will be part of a system Ford is planning to offer on the new Thunderbird, Mercury Cougar XR-7, Lincoln Continental, and Continental Mark VI [*Electronics*, June 7, p. 36].

To protect the microprocessor from climatic conditions, Dearborn, Mich.-based Ford will mount it inside the passenger compartment or in the trunk, depending on the car. But the push buttons that signal combinations of numbers to the microcomputer are mounted, of necessity, on the outside of the door in a horizontal row above the keyhole. Each car will have an ordinary lock acting as a backup to the electronic locking system.

Subcontractors. The Motorola chip, one of its MC 141000 series of 4-bit microcomputers with on-chip read-only and random-access memory, from its Integrated Circuit division in Austin, Texas, is assembled into the controller module by the

Essex group, a subsidiary of United Technologies Corp. ITT's Automotive Electronic Products division supplies the button assemblies.

The system unlocks the driver's door when a preprogrammed five-digit code is entered through the keyboard. Although there are only five buttons, the codes are based on 10 numerals, with each button representing two numerals.

Each unit will come with a factory-set five-digit combination. This code is stored, along with the operating program, in a nonvolatile ROM. The driver can also change the combination—for example, when the car is left in a parking lot—simply by punching a new code into the keyboard within 5 seconds of entering the preset combination. The new combination, stored in the random-access memory, can be changed simply by repeating the sequence with a different code.

More. The "keyless entry system," as Ford calls it, can also open the other doors and release the trunk lid. Including powered door locks, it will sell for about \$200.

To lock the car, the driver pushes two specified buttons simultaneously as he leaves the car. The microcomputer relocks all the doors when the driver's seat is occupied, the ignition is turned to drive, and the transmission control lever is moved through reverse.

-David Whiteside,
McGraw-Hill World News

Sensors respond to fluid level

As self-service gas stations and long gas lines proliferate, more and more motorists suffer for lack of the simple, regular maintenance checks once performed by the gas station attendant. But Texas Instruments Inc. says a new silicon sensor it has developed can partially solve the problem. Believed by TI to be the first solid-state device to be used for fluid-level detection, the sensor has already been employed in some 1979 cars built in England. It serves as part of a system designed to warn a

motorist when the engine oil level is low.

The system does not replace the oil pressure switch but instead checks the fluid level each time the auto is started. When there is too little oil, it triggers a flashing dashboard light that remains on until the engine is shut off. The system could just as easily detect levels of engine coolant, transmission fluid, brake fluid, or other liquids.

The design of the tiny 20-by-20-mil sensor relies on the temperature dependence of the resistivity of silicon to differentiate between the presence or absence of a liquid. When current is applied to a silicon resistive element installed, for instance, in an engine crankcase, the voltage drop across the sensor depends upon whether or not it is immersed in the oil. The thermal conductivity of air is much lower than that of oil, so resistivity is measurably higher when the sensor is in air than when it is immersed in the oil, explains Klaus Wiemer, discrete products development manager at TI's Electronic Devices division in Dallas.

TI began developing the level sensor in 1977 on a nonfunded but proprietary basis with Chrysler Corp. More than 100,000 sensors were delivered to Chrysler, says Wiemer, to be used in 1979 Chrysler Avengers built in England. That contract has now ended, however, and TI is now talking with various automakers regarding the use of the device in U. S.-made cars as early as the 1982 model year. The Dallas firm is also working with one overseas manufacturer on a multiplexing arrangement so that several auto fluid reservoirs could be monitored with a single circuit package.

Though Chrysler provided its own discrete circuitry to work with the TI sensor, Wiemer says TI's linear design group is currently developing an integrated circuit that could handle the sensor outputs and could thus save automakers the trouble of designing their own. TI is also working on ways to automate further the manufacture of the tiny fluid level sensor, says sensor development

News briefs

National Semiconductor grows 46% to \$719 million

As evidence that the semiconductor industry is in a boom time, National Semiconductor Corp., Santa Clara, Calif., reports total fiscal year 1979 revenues were \$718.8 million, up 46% over 1978's \$494 million. Moreover, revenues for the fourth quarter, which ended May 31, were up 51% over a year ago to \$200.5 million, and profits for the fiscal year jumped 52% to \$34.3 million. President Charles E. Sporck attributes the growth to record production levels and additional capacity at plants worldwide. He states that the momentum in component demand has continued, adding that for the rest of calendar year 1979 "the rate of growth for components and systems orders is expected to slow, although we see no signs of slackening." Sporck says he expects National to become a billion-dollar company within the next few years.

Itel, Amdahl hit by IBM 4300

The aftershocks of IBM's 4300 series computers, coupled with an increasing industry trend toward leasing, hit two high-flying California plug-compatible mainframe manufacturers hard. Itel Corp., San Francisco, announced that "substantial losses" by its problem-plagued data-products group, about one half of the business, will mean a loss of approximately \$10 million in second quarter continuing operations, compared with \$9.4 million earnings for the same period last year [*Electronics*, Sept. 14, 1978, p. 96]. The marketing and leasing company says it will cut costs through layoffs and an aggressive new pricing and leasing program on its computers, which are supplied by Hitachi and National Semiconductor Corp.

In Sunnyvale, Amdahl Corp. says it expects only to break even in the second quarter, even though it is shipping as many or more mainframes as in any previous quarter, an announcement that sent its stock tumbling. The reason is that more customers are leasing than buying, which industry analysts attribute to expected price cuts by IBM and to the new high-end mainframes that are expected from Amdahl and IBM.

Action on the codec front

In what some observers believe to be a harbinger of more to come soon, Stromberg Carlson placed one of the largest orders to date for coder/decoder parts—for about \$2 million worth to be built by Mostek Corp., Carrollton, Texas. In a separate announcement, Mostek's telecommunications effort received an added boost with word that Fairchild Camera and Instrument Corp. will second-source the Texas company's MK5116, 5151, and 5156 codec parts. Fairchild will not receive masks but plans to make its own copies of the Mostek complementary-MOS parts—perhaps by year-end. The arrangement is the second involving codecs from major semiconductor manufacturers. Texas Instruments announced plans earlier to second source Itel Corp.'s codec design, which is done in competing MOS technology [*Electronics*, March 29, p.48]. Mostek is said to be negotiating with the French firm Thomson-CSF and with another U. S. company as possible additional sources for its codec parts.

The Mostek-Fairchild arrangement, which does not cover filters or other parts, could put added pressure on other codec manufacturers to sign up second sources. Motorola, which announced plans last year for a three-chip set, including a C-MOS codec and filter and a bipolar subscriber-loop interface circuit [*Electronics*, Sept. 14, 1978, p. 48], is holding discussions with RCA Corp. as a possible second source for telecommunications parts.

CCDs to help warn against intruders

RCA Corp.'s Advanced Technology Laboratories, Camden, N. J., and the Air Force are working on a perimeter surveillance system based on a chip that combines infrared sensors and charge-coupled devices. The IR-CCD chip, placed at various locations, would be tied into a microprocessor-based signal processor that compares a time-averaged video signal from each sensor element with the sensor's instantaneous output.

Technological leadership



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Electronics review

manager Wayne Tarpley. Though the units were sold for more than \$2 each under the Chrysler contract, automation is expected to bring the price to a \$1-per-unit range initially, with large-volume production eventually driving the price as low as 50 cents each.

-Wesley R. Iversen

Government

Remote monitoring checks out sites

The Federal Aviation Administration is pushing ahead with a program for monitoring the performance of its radar and communications installations remotely, over phone lines or microwave links. Meeting in Kansas City, Mo., in late March, FAA engineers made the final choice of equipment for the so-called R-2508 remote maintenance monitoring project, which joins microprocessor-based automatic test equipment via a general-purpose interface bus and controls it by a desktop computer.

R-2508 is the area designation on aviation maps that stretches north from Lancaster, Calif., about 140 miles and is approximately 110 miles wide. Within it are the Naval Weapons Center at China Lake, Calif., Edwards Air Force Base, and other small military enclaves. The remote maintenance monitoring project for the R-2508 area is a joint Air Force-Navy-FAA effort (with 86% of its funds from the military and 14% from the FAA) set up to provide the monitoring of eight remote radar sites in California and Nevada. The first three radars are slated to be installed at Navy facilities in California's Mojave Desert. The monitors are to be in place "before the end of 1980, perhaps in October," says Harvey Bresler, assistant in Los Angeles to the FAA's airways facilities service director.

By 1985, the monitoring scheme could be instituted at all 300 or more FAA radar facilities in the U. S. The first to get them will be sites, often containing long-range radars, that are remote and relatively inaccessible,

according to John Hesla, project engineer at the Los Angeles en-route automation engineering section.

At present, maintenance monitoring is performed by technicians who travel to the site. There they spend anywhere from one to four hours recording readings that ensure the correct operation of radar and communications equipment. It costs about \$140,000 to train the journeyman technician, whose GS-12 rating qualifies him for a yearly salary ranging from \$23,000 to \$27,000, according to the FAA. With remote monitoring, says Hesla, technicians of a GS-9 rating (\$15,000) could be hired and fewer would be needed.

In the monitoring setup, a desktop controller is programmed to coordinate readings that are sent to a central command center. Measurements are made by microprocessor-based programmable instruments, permanently connected to test points in the equipment, that rapidly communicate with the controller over a standard IEEE-488 8-bit parallel bus. For the R-2508 program, data will be transferred to the central facility via a microwave link.

Tests completed. The concept is not theoretical. A nine-month test conducted at the San Pedro, Calif., long-range, air-route-surveillance radar facility was followed by a 10-week trial at a Long Beach, Calif., airport-surveillance radar site.

"Overall system performance was virtually perfect throughout the demonstration period," says Hesla, who coordinated the program. "There were no failures in the [monitoring] equipment or in the interface even though the equipment was cycled hundreds of times and was sometimes operated for weeks without interruption," he continues.

The monitoring at San Pedro took only 40 seconds to make all the measurements usually handled by a technician, according to Hesla. He also points out the automated scheme is orders of magnitude more repeatable than a technician's measurements. For one thing, human errors in setup are eliminated, as are the parallax errors that occur during meter readings.

-Electronics staff

SCIENCE/SCOPE

In honor of their Pioneer Venus mission success, Hughes and NASA's Ames Research Center have received the Nelson P. Jackson Aerospace Award from the National Space Club. The award is made annually to the firm most responsible during the preceding year for outstanding contributions to the space, missile, and aircraft fields. Hughes designed and built the five spacecraft that penetrated the Venusian atmosphere last December, as well as the vehicle that was placed in orbit around the planet and continues to send information to Earth. Ames manages the project. Hughes previously won the award in 1968 for its Surveyor moon landers.

All three types of U.S.-built wide-body jetliners will carry Hughes passenger entertainment and service equipment now that Pan American World Airways has ordered the system for its new Lockheed L-1011s. The system, transmitting multiplexed signals at rates up to 5 million bits per second, provides stereo music and movie sound tracks, plus reading light and flight attendant call service. An earlier system is standard equipment on all McDonnell Douglas DC-10s. Also, 14 operators of Boeing 747s, citing high reliability and low operating costs, have chosen the system as either original or replacement equipment.

Old pastel masterpieces may retain their beauty with help from modern electronics, specifically from an electrostatic plate that prevents the chalky pigment from flaking. The plate consists of positive and negative circuits laminated in plastic. When placed behind a drawing and given a 10,000-volt potential, it generates a field of static electricity that holds the pastel particles to the surface of the paper. The unit and painting are enclosed in a dust-free frame to prevent contamination. Tests to date indicate the plate is superior to existing conservation methods because it virtually stops flaking. Also, unlike spray fixatives, it does not alter certain colors. Hughes built the plate at the request of the Conservation Center of the Los Angeles County Museum of Art. The Armand Hammer Foundation provided funds.

Hughes Industrial Electronics Group -- with locations in Carlsbad, Irvine, Newport Beach, Torrance, and Sylmar, California -- is seeking engineers, computer scientists, and physicists. Products include image processors/sensors, lasers, microelectronic production equipment, computer graphics, automated circuit testers, microelectronic devices, frequency control devices, microelectronic communication systems, facility management systems, electronic modules, connecting devices, flexible circuitry, solar cells/simulators, microwave traveling-wave tubes, microwave tube amplifiers, microwave solid-state products, microwave communications systems, and thermal products. Send resume to: John G. Wilhite, Hughes Aircraft Company, IEG-SE, P.O. Box 2999, Torrance, CA 90509.

A new traveling-wave tube amplifier (TWTA) designed for satellite communications uses offers high efficiency in a rugged but lightweight package. The device, designated Model 1264H, originally was developed and built by Hughes for the Tracking and Data Relay Satellite System. It operates in the range from 3.7 to 4.2 gigahertz with output power of 5.5 watts. Other specifications: saturated gain of 55 dB, an operating life of 10 years, and weight of three pounds.

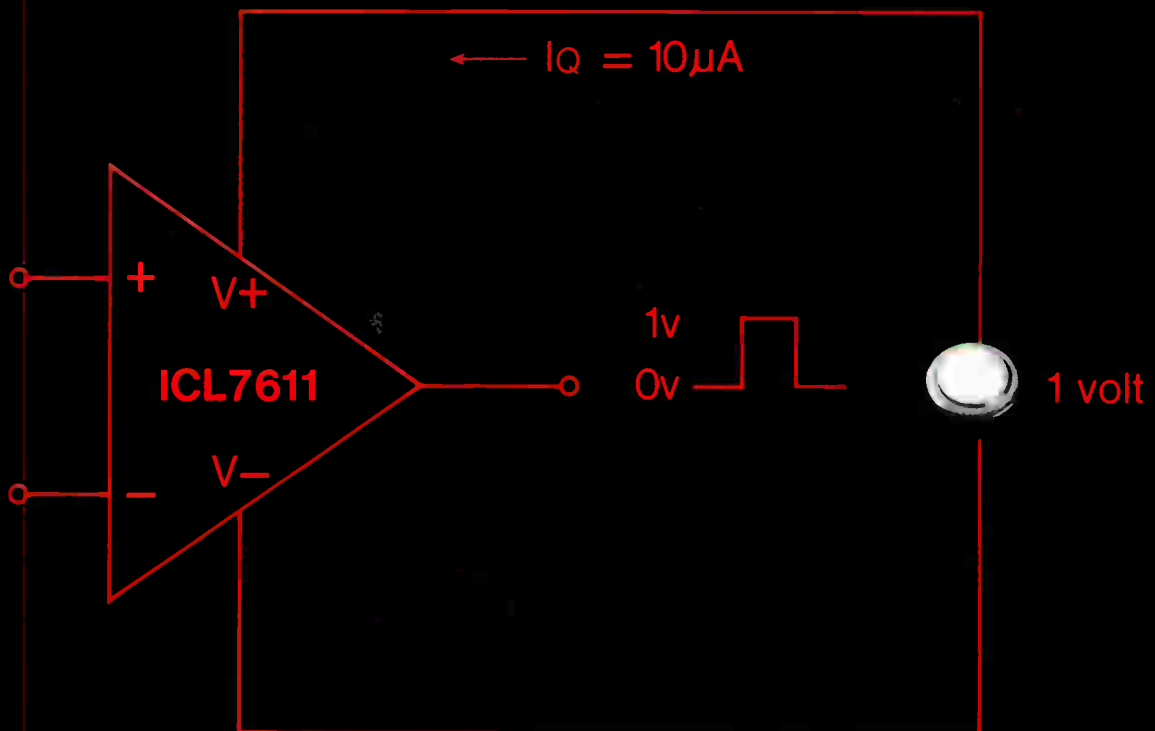
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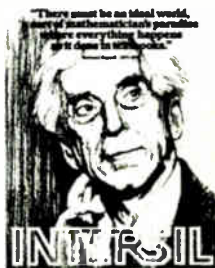
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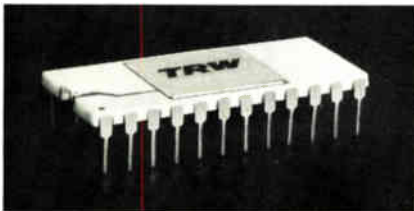
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VHSIC proposal seeks to maintain industry balance . . .

The Defense Department has altered the initial draft of its request for proposals to begin research and development on very high-speed integrated circuits (VHSIC). The move seeks to mollify the House Armed Services Committee, which fears the program **might alter the semiconductor industry's strong competitive balance by favoring some contractors.** Key elements of the VHSIC proposal request, called Phase Zero and delivered to 63 companies near the end of June, ask companies to specify plans to freely sell industry the products resulting from VHSIC—chips and production equipment; plans for second-sourcing other manufacturers; chip architectural approaches; VHSIC commonality potential among a spectrum of military systems; and corporate estimates of possible military market volume. An industry briefing is set for July 16 at the Army's Electronics Research and Development Command, Fort Monmouth, N. J., with industry responses to the Phase Zero request due Aug. 6.

. . . as Congress weighs funding compromise in conference

The Pentagon's move on VHSIC came just before the first July sessions of a House-Senate conference committee for resolving differences in the fiscal 1980 armed services budget. The House Armed Services Committee had eliminated the \$30.4 million sought to begin triservice R&D for VHSIC [*Electronics*, May 24, p. 63], while its Senate counterpart had approved the request after dropping plans to increase funds. **The Senate authorization calls for the Army to get \$12 million, the Navy \$10.4 million, and the Air Force \$8 million.** A decision is expected by the conference committee before September.

Pentagon promotes VHSIC's Sumney as Weisberg leaves

The Defense Research and Engineering directorate, which oversees VHSIC, underwent a management reshuffling June 30 with assignment of increased responsibility for all Defense Department electronic devices programs to project chief Larry H. Sumney [*Electronics*, Sept. 28, 1978, p. 12]. Sumney will report directly to Ruth M. Davis, deputy under secretary for research and engineering. His move stems from the return of Leonard Weisberg, until now director of electronics and physical sciences on Davis's staff, to industry after nearly four years of Government service. **Insiders say his successor will not be named for "a couple of months."**

Weisberg says he advanced his resignation from September to beat the July 1 start of a new ethics law that prevents Federal managers for two years from joining any company with which they have had business dealings while in Government. Weisberg, former research vice president at Itek Corp., Lexington, Mass., has made no commitments yet and will take an extended vacation.

ISA standards coming from DOD to include microprocessors

The Defense Department will recommend within 60 to 90 days **its first standardization form and process for an instruction-set architecture (ISA) for its computers "that will attempt to include the microprocessor as well,"** according to the Directorate of Defense Research and Engineering's H. Mark Grove, assistant for computer resources and electronics. ISA, a much-discussed issue at last month's Washington meeting of the Armed Forces Communications and Electronics Association, where Grove spoke, is defined as those computer properties a programmer must know to write a time-independent machine-language program, including instruction set, program-controlled registers, and data structures.

The poisoned environment of the EPA

The Environmental Protection Agency works out of a shopping mall's makeshift offices in the Washington waterfront section known as Southwest. The facilities mirror EPA's widespread image as an agency that was put together quickly on a foundation of good intentions and not much else. Thus far, its record of bureaucratic bungling has earned it almost as many enemies among the ranks of environmental professionals now as it initially had within the industries it is supposed to oversee.

Can capacitors cause cancer?

The most recent example of the EPA's ineptitude is its inability to follow through on its ban on the use of polychlorinated biphenyls. PCBs, now suspect as a possible cause of cancer, used to be a component of oil-filled capacitors as well as other nonelectronic products before the EPA's ban became effective earlier this year. Capacitor makers like Aerovox Inc. of New Bedford, Mass., saw the ban coming, of course, and substituted the compound known as DOP—diocetyl phthalate—for the PCBs in their products months in advance of the EPA deadline.

Now industry's problem is to get the EPA to follow through on its related ruling more than 16 months ago that PCBs must be destroyed by incineration. The agency has yet to designate a single industrial incinerator for burning PCBs despite the fact that containers of waste have piled up at industrial plants and warehouses leased by producers.

Aerovox president Clifford H. Tuttle Jr., who also chairs the Electronic Industries Association's *ad hoc* committee on liquid dielectrics, suspects the EIA "may have to respond as environmentalists do and take the EPA to court before we can get action on the incinerators." That should add substantially to the EIA committee's legal fees, which Tuttle estimates already amount to about \$150,000.

EPA administrator Douglas M. Costle got a strong letter from the EIA committee chairman in mid-June in which he argued that "despite frequent promises of action by the agency, no incinerator sites have been approved and no approval is expected in the near future. The time has come, therefore, for you to take firm and vigorous action to insure the prompt availa-

bility of incinerators for PCB liquids."

Asked for comment a week after the letter's delivery by hand, an EPA spokesman said the agency "doesn't know of the letter. No one here can find it." A subsequent call to the EPA a couple of days later determined that the letter had been located in the office of the general counsel but had not yet been read. The EPA's new position: the issue is "being studied."

What has the EPA been doing since it established the PCB incineration requirement more than 16 months ago? Trying to locate facilities capable of burning PCBs at a temperature high enough to destroy the chemical, according to another EPA source. Rollins Environmental Services has been trying to do "a test burn for several weeks," the official explained, but faces strong opposition from environmentalists living in the vicinity of its Bridgeport, N. J., incinerator.

Meanwhile, PCB wastes continue to accumulate at many sites, all of which require security precautions and any one of which could produce a dangerous leak or other environmental hazard. Tuttle estimates that one Arkansas site alone may contain between 500,000 and 1 million pounds of PCB. "This worries me much more than the economics of storage," says Tuttle. "I am not a strong environmentalist," he concedes, "yet I can see this as a dangerous problem."

Thinking things through

There are other valid conclusions that may be readily drawn from the bungling of the PCB issue, the broadest and most obvious being that the EPA is not protecting the environment. The agency has been around too long now for its apologists to proffer the argument that its errors are the product of growing pains in an organization still in its infancy. That excuse long ago lost what little credibility it may once have had.

The EPA has few, if any, friends in an industrial community that finds the economic burden of its regulations not being offset by the promised environmental benefits. Yet the agency might gain a modicum of respect from business if it could at least demonstrate an ability to clearly think through each step it must take to enforce its rules before they are promulgated.

-Ray Connolly

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② Chmn & CEO, Microprocessor Div of Computers Inc, 1023 W Warner Ave, Dayton, OH 45479, Tel (513) 555-2000. ③ Born: Mar 26, 1926, Philadelphia, PA. ④ Education: MBA, Harvard Business School, 1950; BSEE, Univ of Ill., 1946; PhD (Hon), Yale Univ, 1977. ⑤ Professional Experience: Natl Bur of Standards, 1956-74, Adm Eng; Litton Ind, 1954-56, Sr Eng; NCR Corp, 1950-54, Eng. ⑥ Directorships: Computers Inc since 1975. ⑦ Organizations: IEEE since 1946, Sec Head 1972-73; AAAS since 1971; Midwest Ind Mgt Assn since 1974. ⑧ Awards: Fellow, IEEE, 1977; Public Service Award, City of Dayton, 1976. ⑨ Patents Held: 8 in computer circuits, incl Special Circuit for Microcomputer Chip Design 1975. ⑩ Achievements: founded Microprocessor Inc 1974; project manager on first application of microprocessors for standard interfaces 1975. ⑪ Books: 4 incl *Small Circuits and Their Applications* (editor), McGraw-Hill, New York, 1975. ⑫ Personal: married 1950 to Mary (Smith), children John Jr, Jane Anne, Kevin. ⑬ Residence: 344 W 34th St, Dayton, OH 45403, Tel (513) 555-4343.

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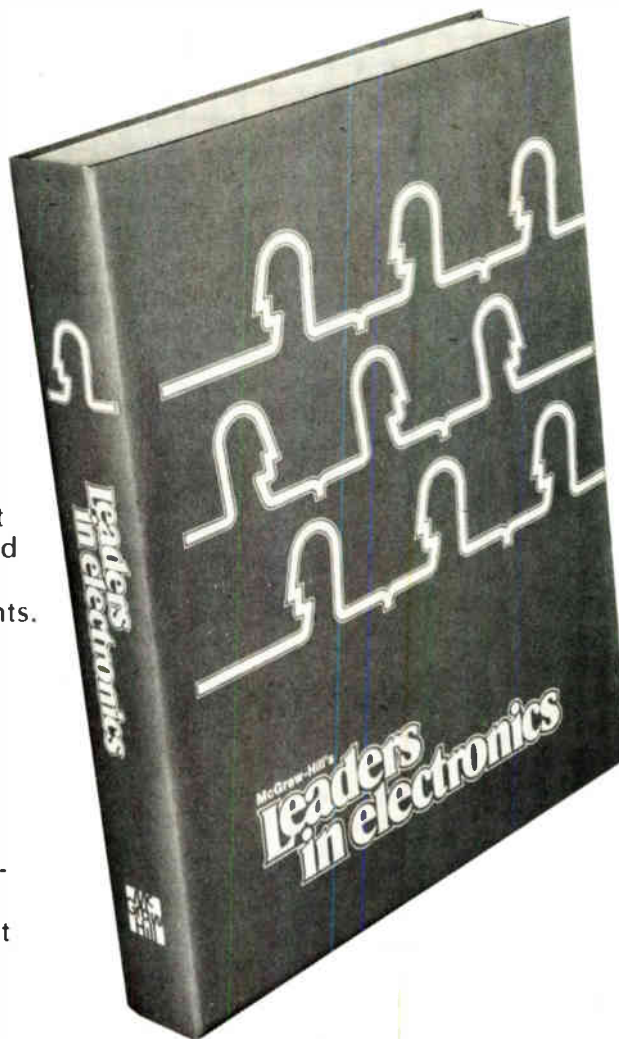
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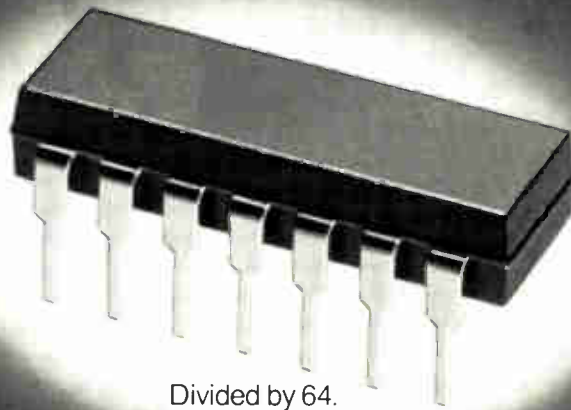
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Single CCD sensor, for VCR use, yields three colors

A two-dimensional charge-coupled-device image sensor developed by Nippon Electric Co. should enable its subsidiary, New Nippon Electric Co., to market a small, light video camera for home video cassette recorder applications late next year or early 1981. A prototype camera with only one CCD sensor chip shown by the two companies performs better than the consumer single-pickup-tube cameras now sold. The sensor, which operates in the interline mode for improved resolution, has 400 picture elements horizontally by 492 vertically. It offers improved sensitivity, especially at the blue end of the spectrum, because high-sensitivity junction photodiodes are used for photoelectric signal conversion rather than the MOS capacitors of other CCD arrays. Although standard scene brightness is 1,200 lux with an $f2.8$ lens, satisfactory operation can be obtained down to 80 lux with an $f2$ lens. **An organic filter laminated onto the 567-by-433-mil chip provides the chroma characteristics needed to derive a color signal from the output of a single chip.** A charge-transfer efficiency of 99.999% makes for good color reproduction.

British firm uses CRT technology for flat-screen TV

A miniature black-and-white television set with a 3-in. flat-screen display could be in production within two years if a joint venture between Sinclair Radionics Ltd., a National Enterprise Board-backed company, and an as yet unnamed manufacturer goes ahead. Unlike other proposals for flat-screen TV, Sinclair's uses conventional cathode-ray-tube technology, but with the axis of the electron gun parallel to the phosphor screen and a patented arrangement of electrostatic plates to deflect the electron beam onto the screen. **A prototype 3/4-in.-thick tube with 3-in. viewing area has already been demonstrated** and provides far higher resolution than other flat-screen technologies, according to the firm. The tube, which consumes less power than conventional CRTs, could be further developed to provide full color with projection screen sizes up to 4 ft, Sinclair says. But that is beyond the company's resources, so it is seeking a partner with the necessary financial and marketing strength.

Japanese ready another 64-K RAM

Mitsubishi Electric Corp. has unveiled its 64-K random-access memory. The M58746S operates from a single +5-v power supply and features a maximum access time of 120 ns and a minimum cycle time of 230 ns. The maximum power drain is a low 20 mW, with a standby power drain of 22 mW. Completely compatible with Texas Instruments' 64-K RAM, including the 256 refresh cycles every 4 ms and no connection on pin 1, it does have one major difference: **Mitsubishi uses a power supply on chip to generate the substrate bias.** The chip size is some 152 by 274 mils. Mitsubishi will begin supplying samples in September in Japan and overseas, with production quantities available sometime next spring.

Ex-Motorola head to breathe life into Plessey-GI talks?

Those flagging negotiations between Plessey Co. and General Instrument Corp. on the future of Plessey's microcircuit operation could be revitalized by the appointment of Melvin Larkin, head of Motorola Ltd., as director of technology for the Plessey Components group. Larkin will be responsible for strategic planning, reporting directly to managing director Michael Clarke. **Thus his input could determine the fate not only of Plessey's microcircuit operation but also of its bubble memory operations.** Both have sound technology but need a huge cash injection to make them go. If

Larkin can find the right formula, a joint venture with GI could solve some of the problems of Plessey's Semiconductor division and ease the strain on Plessey's cash resources should it go ahead with bubbles, too.

Japanese firms agreeing to license NTSC patents from RCA for VCRs

RCA Corp. is said by industry sources to be in the final phase of negotiations to license Japanese manufacturers to make video cassette recorders under its patents for NTSC TV transmission. **RCA claims that a VCR is a television receiver because it includes a tuner and can receive broadcasts off the air**, and it therefore wants Japanese firms to pay the usual royalty rate. The latter counter that a VCR is less than a complete receiver because it does not have its own display. The two sides appear headed for a compromise of about \$2.30, about half the rate paid for regular TV receivers. The agreement would run for five years, and **royalty payments will come to a considerable sum** because it is estimated that more than two thirds of the approximately 2 million VCRs to be produced in Japan this year will be the NTSC type; Japanese companies will also be liable for royalties on VCRs produced in the past.

French researchers record holograms in real time

A team of specialists in electro-optical phenomena at Thomson-CSF's central research laboratories in the Paris suburb of Corbeville has found a way to produce and display holographic interference patterns in real time, avoiding the delay incurred with photographic plates. In the new technique, the hologram is obtained by mixing an object beam and a reference beam from the same laser in a small, thin slab of a bismuth-silicate crystal (known as BSO) having a field of several kilovolts across it. With argon-laser illumination, the hologram forms in some 20 ms. It remains as long as the slab is lit and charged. **When the object beam is cut, the image can still be read out for about 20 ms more**; thus by using a storage tube for readout, holograms taken in short succession can be superimposed to show minute movements of moving objects.

Insac eyes future microprocessor-based teaching terminals

Insac, the software marketing consortium established by Britain's National Enterprise Board, **has signed a long-term research and development contract with the Open University to develop microprocessor-based teaching and training systems**. The university, established by the British government to provide adult degree courses through the use of the broadcasting media, has developed an experimental terminal called Cyclops that links a TV to a microprocessor-controlled cassette storing graphical information and a sound track. Material written on one Cyclops with a light pen can be sent to others over public telephone lines.

West German researchers near absolute zero

Scientists at the Institute for Solid-State Research in Jülich, near Cologne, **have managed to bring the temperature of a copper block down to 0.00016 K**—the lowest value ever achieved, they say. Such closeness to absolute zero has important implications in electronic component research, specifically for investigating certain processes and phenomena in solid-state materials. Using equipment of their own design, the researchers employ five steps. The first three, which involve cooling with liquid helium, lower the temperature to 25 mK. The last two, based on adiabatic demagnetization of atomic nuclei, reduces it to 160 μ K.

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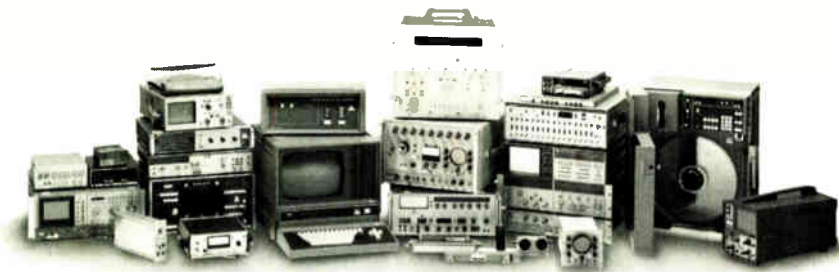
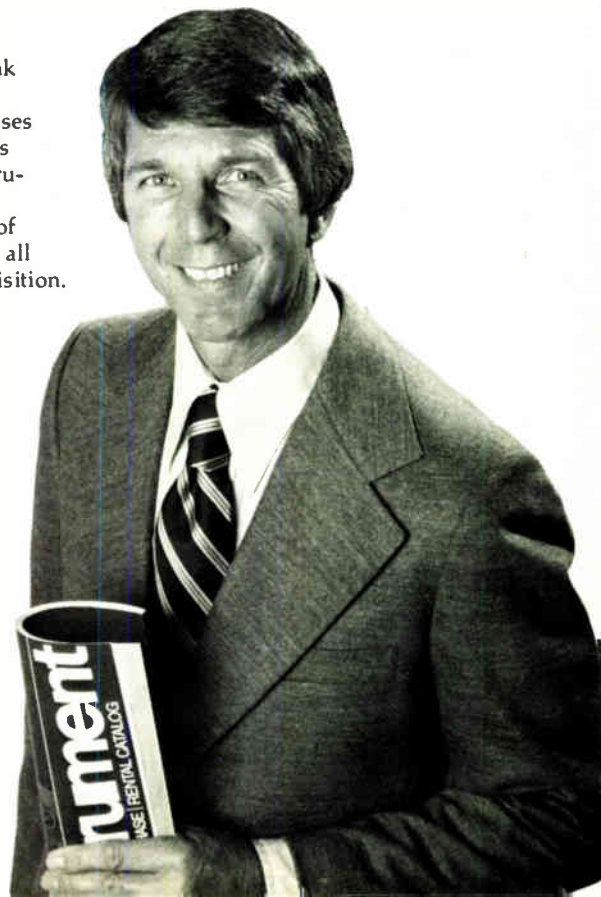


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Very quiet GaAs MES FETs coming for uhf TV tuners

by Charles Cohen, Tokyo bureau manager

Dual-gate devices have a typical noise figure of 1.3 dB at 1 GHz and a drain voltage of 5 V

A new Japanese technique for processing gallium-arsenide epitaxial wafers may soon pop one more problem from the consumer electronics stack: the poorer performance of television sets at ultrahigh than at very high frequencies.

With its technique, Matsushita Electronics Corp. plans to produce inexpensive dual-Schottky-gate field-effect transistors with very low noise figures for uhf operation. They would be used by TV set makers in

the radio-frequency amplifier stage of the uhf tuner.

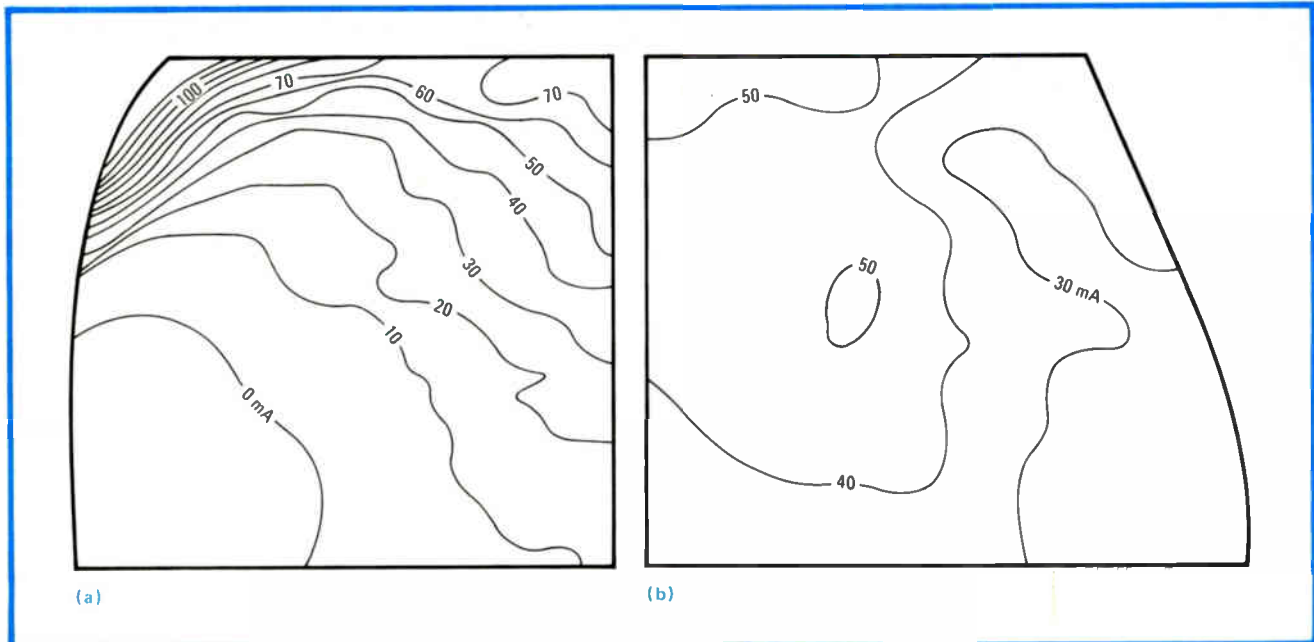
The bipolar transistors at present generally found there are far from satisfactory. For instance, though the goal is a uhf noise figure of 12 decibels in three years or less and the same as in vhf units eventually, the typical figure today is 14 versus 4 dB for vhf. Further, intermodulation distortion is usually far worse than for the dual-gate FETs used in the rf amplifiers of vhf tuners.

Not an obstacle. Lithography is not a major obstacle to this application of GaAs technology. For similar device dimensions, dual-gate n-channel GaAs metal-semiconductor FETs (MES FETs) have five times the carrier mobility of silicon MOS FETs—which are beginning to be

used in the rf amplifiers of uhf tuners—and hence a proportionally greater frequency response. Experimental devices yield the desired performance at 1 gigahertz—typically a 1.3-dB noise figure, 15 to 17 dB of gain, and a maximum frequency of oscillation of 8 gigahertz—all with the relatively low drain voltage of 5 volts.

The ability to operate at 5 v is an important bonus. The 15-v power supply required for the silicon dual-gate devices in uhf tuners is a problem because the other signal circuits in most console sets operate at no more than 12 v, those in portable sets at 6 v.

The real difficulty is controlling drain saturation current. A key parameter, it is proportional to the



Uniform. Controlled illumination of GaAs epitaxial wafers during anodic oxidation yields uniform drain saturation current for all MES FETs made on one wafer. The distribution maps of this parameter are for chip sections oxidized conventionally (a) and with controlled light (b).

product of the dopant concentration and the epitaxial layer thickness of a GaAs FET. The starting material of such a device is a thin epitaxial layer of GaAs overlying a buffer layer on a semi-insulating substrate of the same material. For optimum device characteristics, the thickness of the epitaxial layer must be on the order of 0.25 micrometer.

Constant. Despite variations in this thickness and in the initial value of the dopant concentration, Matsushita's technique maintains precise, automatic control over the product of these two parameters. The key is controlled illumination of the wafers during anodic oxidation.

The light forms a charge-depletion layer with a constant dopant concentration-thickness product in the epitaxial layer. The depletion layer protects the portion of the epitaxial layer in which the devices will be fabricated during anodic oxidation. The oxide layer is then dissolved, leaving the desired thin epi layer.

The result is a uniform drain saturation current for all FETs fabricated on the wafer. This ensures high device yields.

Sumitomo Electric Industries is preparing to mass-produce the wafers [*Electronics*, June 21, p. 66], so that it should soon be possible to fabricate GaAs dual-gate FETs for only a fraction of their present cost. That should drop their price from the high-flying range of space-program devices to the down-to-earth level of consumer electronics.

Matsushita expects to start supplying samples soon for less than \$2.50 each. It also says it will sell equipment for brightness-controlled oxidation of GaAs wafers. Prices will depend on the number and size of the wafers to be processed.

In addition, the same processing technology should also make possible reasonably priced large-scale integrated GaAs logic circuits with normally-off MES FETs on epitaxial layers only 0.08 μm thick.

family will go to market around the end of the year and retail for between \$1,250 and \$1,300. Designed for the PAL color TV transmission standard, they are intended primarily for West European consumption. Secam and NTSC recorders will follow later.

Philips will also take on the competition in the lush U. S. market. There, its affiliate, Magnavox Consumer Electronics Co., should be a valuable asset. Eventually, the Dutch electronics giant may venture into Japan itself.

Prompting Grundig and Philips, Europe's only two VCR makers, to join forces is the desire to halt further penetration by the Japanese into their home markets. With a position of strength in VCRs, coupled with a combined share of about 50% of Europe's color TV market, the two are confident they can lure other firms into the Video 2000 camp.

Separate. Though the system's parameters were worked out jointly, each company has developed its own model independently and will continue to do so. Likewise, each will produce only its own machines—Grundig at its VCR plant in Nuremberg and Philips at its facilities in Vienna. The Dutch firm has designated its first Video 2000 machine the VR 2020; Grundig's is called the Video 2x4.

For the two companies, the system's long playing time is only of secondary importance. More important to them, according to Philips' Maeyer, are features like upward compatibility and extendability, tape economy, and dynamic track following. With both its mechanical and electrical-electronic portions modularly designed, the system can easily be modified to handle different color TV and line-frequency standards, different types of tapes—chromium dioxide, metal powder, or any other type that may come later—or stereophonic television that some European set makers are considering.

"The new system will be able to handle any new TV developments or innovations that may come along in the 1980s," Klink maintains. It is primarily this upward extendability

Europe

Philips and Grundig team up to produce 8-hour VCR system

It all seems like a game of one-upmanship: no sooner does one producer of video cassette recorders introduce a unit with a certain playing time than another announces a machine that "out-times" the competition. This jousting has been going on since the early 1970s, when consumer VCRs first appeared on the market. Currently on top are Japanese firms with six-hour units that were recently shown in the U. S.

Now upstaging them is a European-designed eight-hour VCR system to be introduced at the Aug. 24-Sept. 2 International Radio and Television Exhibition in West Berlin. The result of a four-year cooperative effort by NV Philips Gloeilampenfabrieken in the Netherlands and Grundig AG in West Germany, the Video 2000 system is "our answer to the Japanese onslaught on the European VCR market," says William G.

Maeyer, deputy manager of Philips' Video division in Eindhoven, the Netherlands. "The fact that Europe's two biggest entertainment electronic producers have developed a common system is an important prerequisite for its market penetration," adds Roland Klink, head of product management for Grundig's Video group.

Flip side. The most striking feature of the new helical-scan VCR system is its notebook-sized video cassette that, just like the Philips-pioneered standard audio cassette, is simply flipped over to double the recording and playback time. The cassette's 1/2-inch tape accommodates a maximum of four hours of programs on 1/4-inch tracks on each of the upper and lower sides. It is the first time that a VCR uses a reversible cassette.

The first models of the Video 2000

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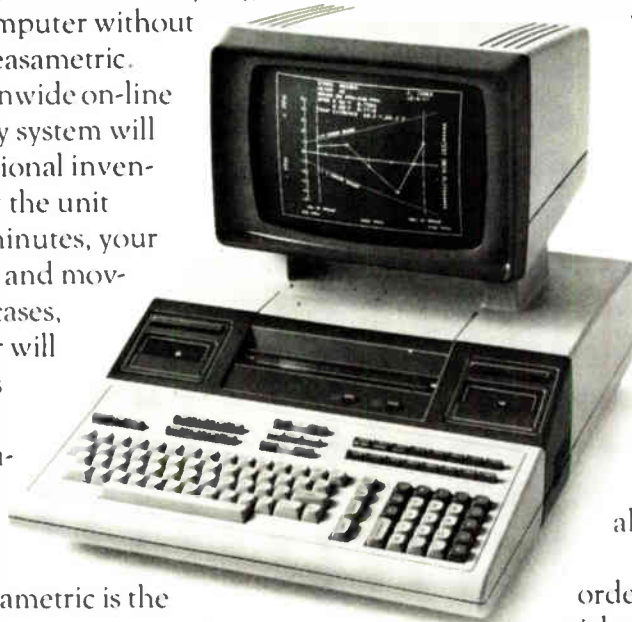
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that the two companies believe will induce other European firms that have thus far opted for selling Japanese VCR equipment to switch to the Video 2000.

Economical. High tape economy is achieved in several ways, besides the double use of the tape. One is the reduction of the video track width to only 22.5 micrometers, which is one quarter the track width on tapes employed with Philips' long-playing N1700 [*Electronics*, May 12, 1977, p. 55 or 5E].

Also, the tape speed has been reduced to 2.44 centimeters per second—which still allows an adequate audio response of up to 12.5 kilohertz. Furthermore, the relative speed between the video heads and the tape has been slowed to 5.08 meters per second.

Thus overall tape consumption comes to only 0.56 square meter per hour. That, Klink says, is 35% and 48% less than with the Japanese Betamax and VHS units, respectively. In terms more tangible to the

consumer, the tape consumption is about \$5 worth for one hour of playing time.

Another noteworthy feature is Dynamic Track Following (DTF). This electronic control system, which has thus far been used only on professional equipment in recording studios, ensures that during playback the recorder's two video heads automatically and precisely follow the video track. In fact, it is the DTF circuitry that allows the tracks to be only 22.5 μm wide and to be placed right next to each other, thus contributing to tape economy.

Also of note is the Video 2000's Dynamic Noise Suppression, a Philips-developed scheme akin to Dolby. Used during both recording and playback, it improves the recorder's signal-to-noise ratio by about 8 decibels, bring the total for the system to better than 52 db.

Philips will continue to make its N1700 equipment and Grundig its SVR4004 machines [*Electronics*, June 8, 1978, p. 70]. -John Gosch

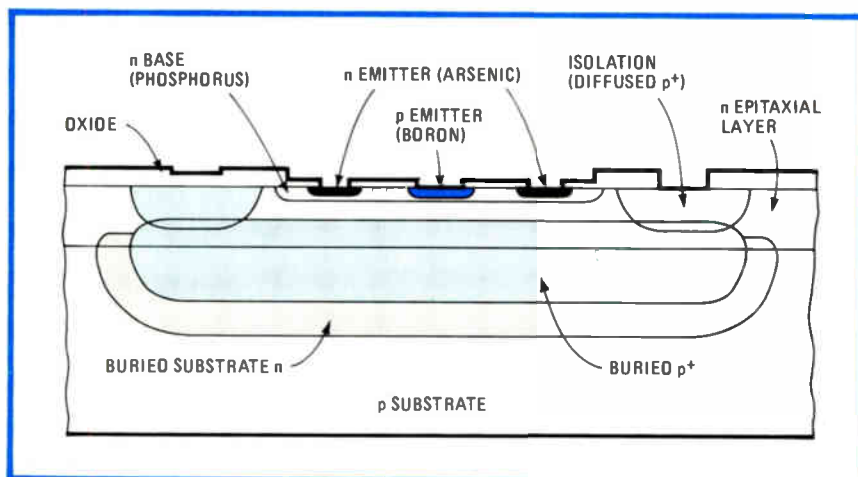
Great Britain

Ion implantation packs in high-performance circuit elements

Extensive use of ion implantation provides the needed control for a flexible bipolar process from Plessey Co. With it, the company is putting on a single chip low-power planar npn and npn transistors and junction

field-effect transistors with performances close to that of the best discrete versions of each.

Developed by the company's Allen Clark Research Centre in Caswell, Northants., the experimental process



is aimed at signal-processing applications. It could provide circuit designers with high-slew-rate operational amplifiers and low-noise front-end circuits, as well as high-performance digital-to-analog converters in a single package.

"This combination of circuit elements is not normally available with a bipolar process," according to Les W. Kennedy, who developed the process [*Electronics*, March 29, p. 66] to meet a Ministry of Defence requirement.

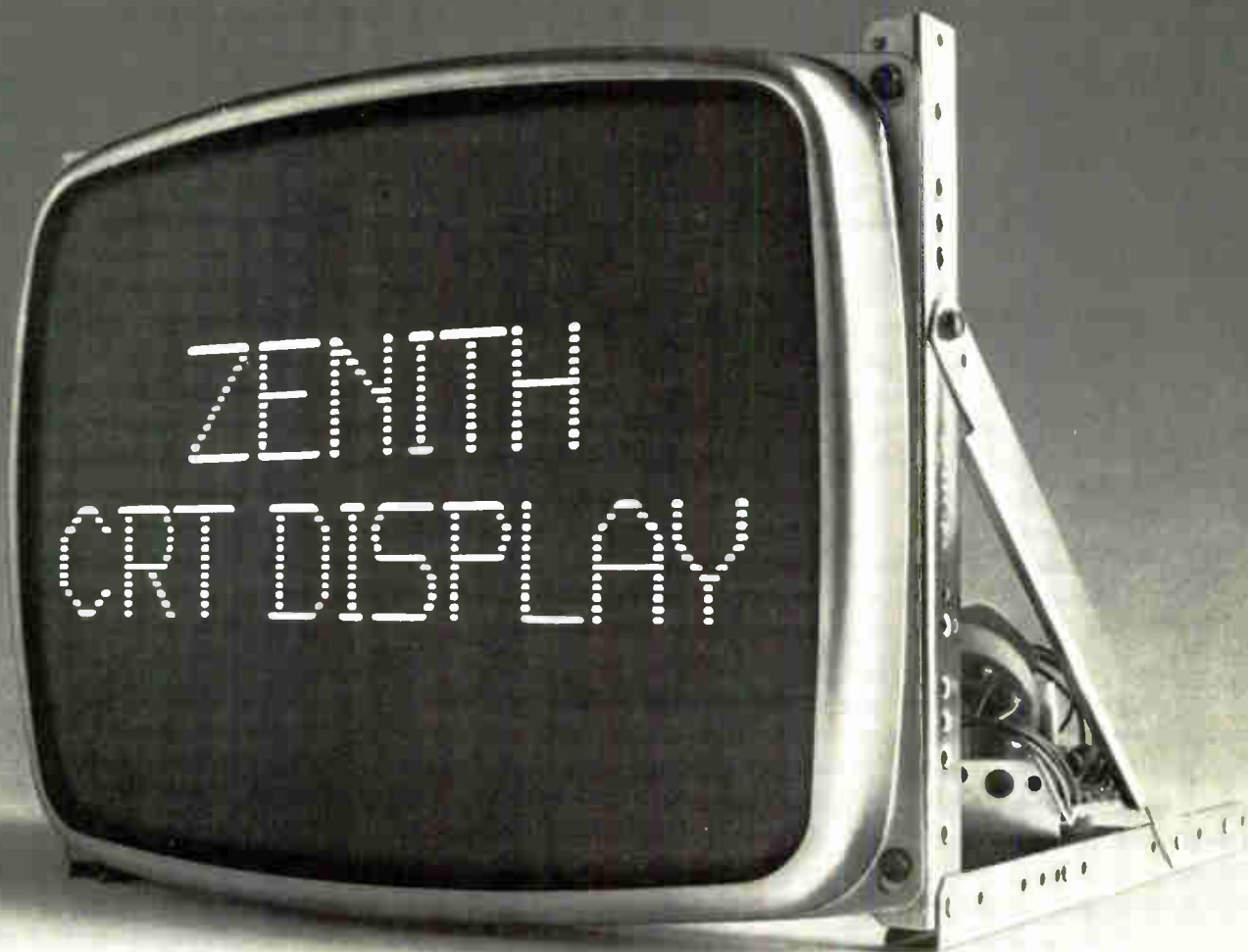
Achievable unity-gain frequency for the npn transistor is 2 gigahertz, he says, and for the pnp transistor more than 300 megahertz. Conventional planar pnp devices, on the other hand, "are very slow and have only a limited performance," Kennedy notes.

Steps. "It would have been exceptionally difficult and would involve unacceptable increases in process complexity to manufacture these devices without ion implantation," he continues. The pnp transistor (see figure) highlights the major differences between Plessey's and a conventional bipolar process.

First, a deep tub-shaped n region is diffused into the initial substrate material before epitaxial growth takes place to isolate the overlying pnp structure from the substrate. The following p layer is ion-implanted before growth of the n epitaxial layer and serves as the buried collector of the pnp transistor and also the back gate of the J-FET.

In order to form the base regions for both the npn and the pnp transistors, windows are opened in the silicon-dioxide layer in a single photoetching operation. Phosphorus and boron dopants are then implanted selectively with the use of masks that blank out first the pnp and then the npn base windows. The J-FET channel is also formed at this stage. A

Planted. Plessey relies on ion implantation to put high-performance planar pnp and npn transistors and J-FETs on the same chip. For low base contact resistance, all base regions are implanted with the emitter of the complementary device—in the pnp transistor shown here, the arsenic p emitter.



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Circle 75 on reader service card

single base drive-in is then employed.

Next, all contacts are photoetched and, again using selective implant masking, the arsenic emitters of the npn and the boron emitters of the pnp devices are implanted. The latter implant is also used for the J-FET's top gate. To ensure low base contact resistance, all base regions receive the emitter implant of the complementary device. After implantation, the emitters are simultaneously driven in. The result is washed-emitter bipolar transistors and washed-gate J-FETs with self-aligning metalization contacts.

Added. To combine pnp and npn device fabrication without adding complexity called for considerable process innovation. The scheme adds two diffusion and associated photoetching stages plus one implantation and two implant-masking stages to Plessey's conventional ion-implan-

tation process. In fact, Kennedy says, the new process could be employed on the line Plessey uses to make its fast frequency dividers.

The pnp transistor produced is a fully isolated planar device with a beta of 60 and a breakdown voltage of 15 volts. It is similar in structure to a discrete transistor and, says Kennedy, when designed with gate geometries of commercially available discrete types, has similar dc parameters. The noise figure at low frequencies has not yet been characterized, but Kennedy says it will be only slightly inferior to that of equivalent discrete devices.

Plessey is not the only company on the same track. Most notably, researchers at Bell Laboratories have been working on a similar process for pnp and npn devices for several years. Plessey, however, claims its process is less complex, as well as adding J-FETs. **-Kevin Smith**

any address, always with the guidance of the display. Once debugged, the program can be transferred to any kind of read-only memory directly from the working memory or by means of paper or magnetic tape. Sockets for electrically programmed ROMs like the 2716 will be optional.

Accidental success. Danfysik got into the development business in a roundabout way. "We needed a development system to program a microprocessor-based controller for a 3,200-channel photomultiplier power supply and could not find anything suitable," Antonsen explains. "We were not sure what microprocessor we wanted to use for the controller, and so a low-cost system good for only one microprocessor was not for us. And we didn't want to spend \$25,000 or more for a powerful universal system. Therefore, we did it ourselves, and it turned out so well we decided to sell it outside."

Danfysik eventually opted for a Signetics 2650 chip for the 3,200-channel multiplier supply and so the μ unique is based on a 2650. But it can handle other 8- or 16-bit microprocessors easily because the instruction set for the type of microprocessor being programmed is read into a 2-kilobyte instruction memory from a cassette. Actually, the instructions take up only one track of the cassette; the other track is available for the contents of the user's program.

A 20-column printer in the machine provides another means for recording the program, along with some limited comments for documentation. For full software documentation, the machine can be connected to an external line printer and keyboard.

For the basic price, Danfysik includes one prerecorded minicassette tape and the companion personality module for the emulation adapter. Cassette and personality module sets for additional microprocessors will run about \$350. So far, this firmware is ready for the 2650 and Intel's 8048, with more to follow soon. **-Arthur Erikson**

Denmark

Development system lets programmer order instructions and addresses from menu

So many microprocessor development systems have been unleashed during the past year that the market seems saturated with units for every device from the AM 2900 to the Z8000. Yet Danfysik A/S, a small Danish firm that has built a worldwide business in instrumentation for high-energy physics research, thinks it has a system using concepts so unique that it can still shoe-horn its way in.

It turned up at last month's International Microcomputers Minicomputers Microprocessors '79 exhibition at Geneva with a universal development system that is both extremely easy to use and very attractively priced—at about \$5,000 it is less than half the price of other universal development systems.

Danfysik's machine makes it almost trivial for a hardware engineer to work in assembly language. "You select instructions instead of writing programs," Peter Antonsen, the

firm's marketing manager, says. Called the μ unique, the system puts a menu of instruction mnemonics for the microprocessor in question in the four right-hand columns of its 9-inch cathode-ray-tube display, along with a set of hexadecimal values. In the four left-hand columns, blocks of 16 lines of program addresses are displayed.

Instructions or numerical values are assigned to the address lines by means of a cursor controlled by a touch panel. The standard working program memory available is 64 kilobytes (32 kilobits by 16 bits).

Once the program is "assembled," the microprocessor in question is plugged into the μ unique emulation adapter and the adapter cable plugged into the designer's prototype hardware for in-circuit debugging and testing. There are 128 labels available for breakpoints, triggers, and symbolic addressing. Instructions can be inserted or deleted at

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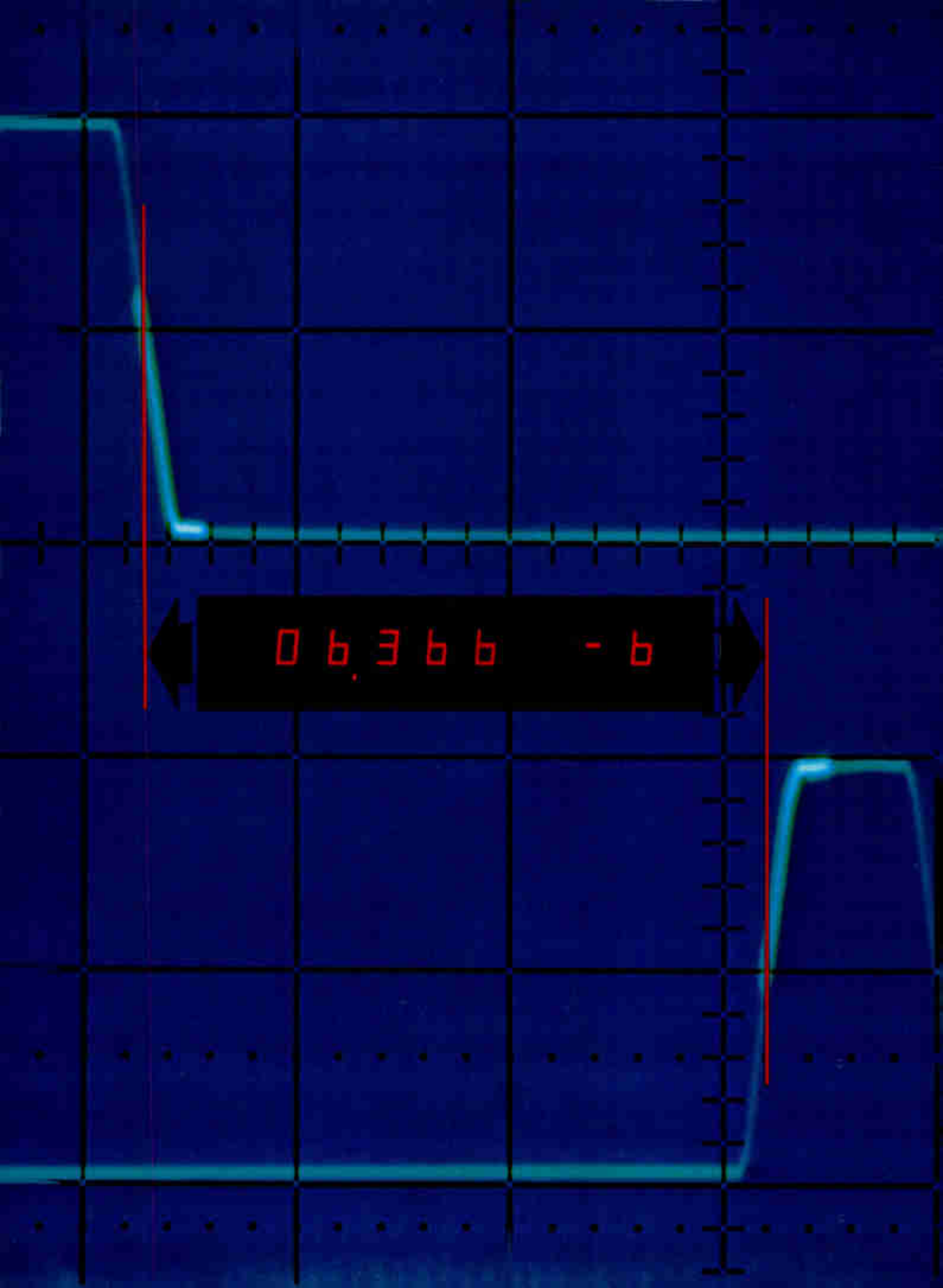
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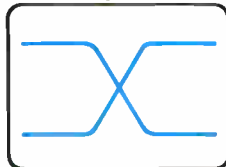
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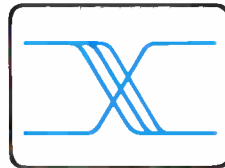
Ease of use. A Δ -time scope is an easy way to make time interval measurements such as periods, pulse widths and transition times. For example, to make a period measurement, just set the START marker at the beginning of one pulse and the STOP marker at the beginning of the next pulse. Then, simply read the time interval from the built-in DMM, the STOP control dial, or an external DMM. It's faster than aligning a pulse and counting graticule lines, and there's no mental arithmetic required. Δ -time is not only fast and easy—it also greatly reduces the chance of error. A case in point is the crystal-referenced HP 1743A. In the lab, it provides high accuracy and fast, easy time interval measurement. In production, it lets you adjust circuit parameters to meet timing specs without touching scope controls. Even busy production personnel can make fast, accurate measurements with ease.



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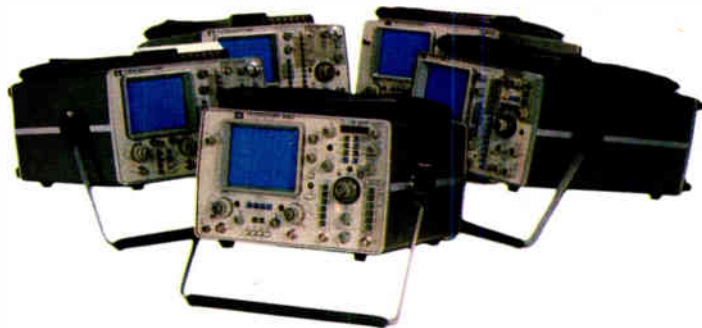
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Wednesday, May 28

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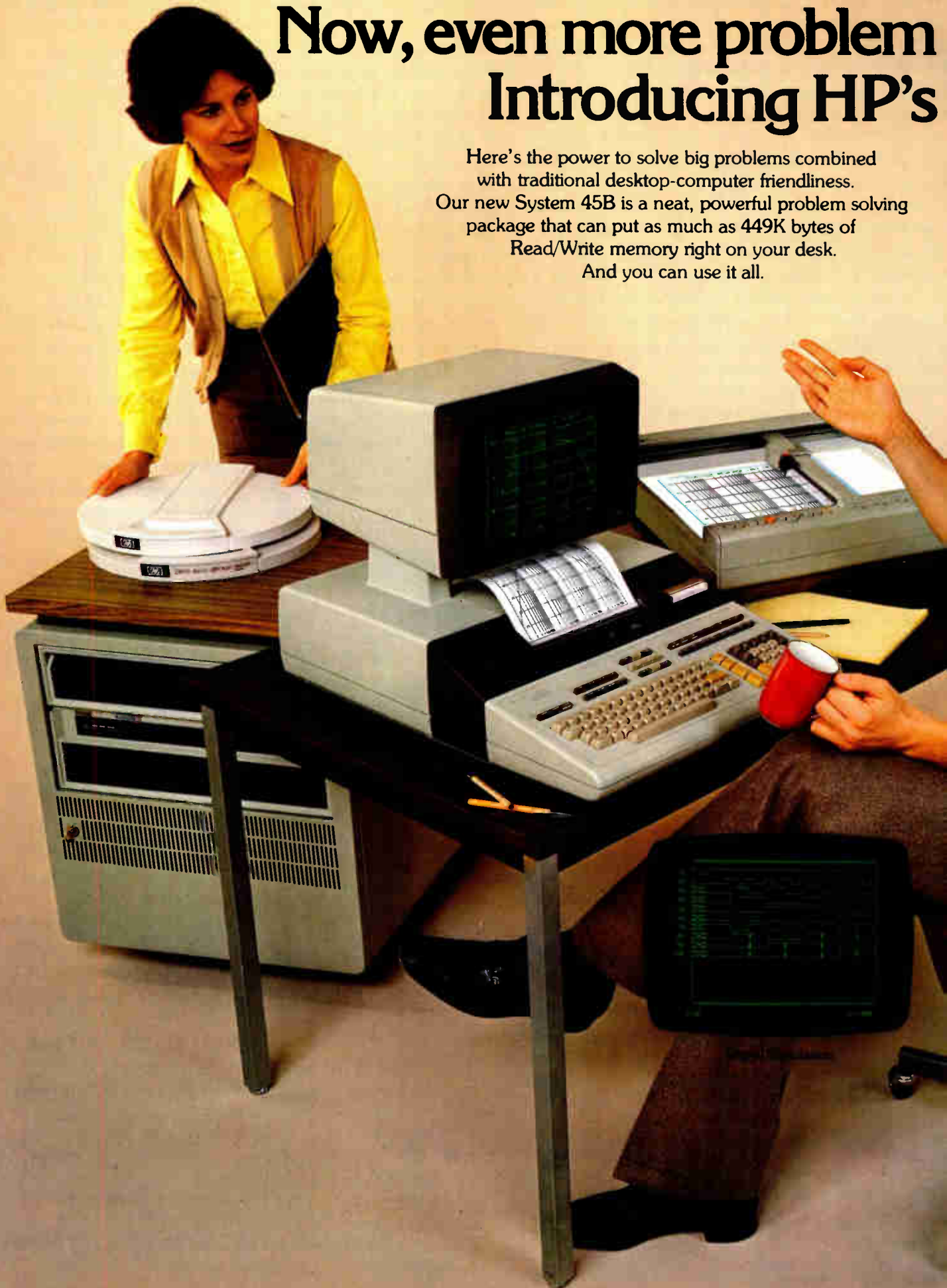
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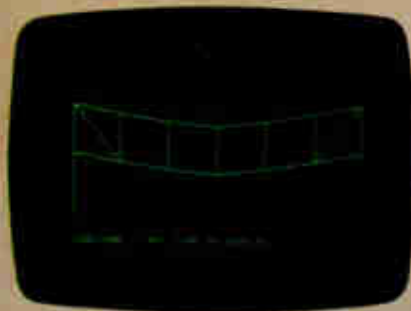
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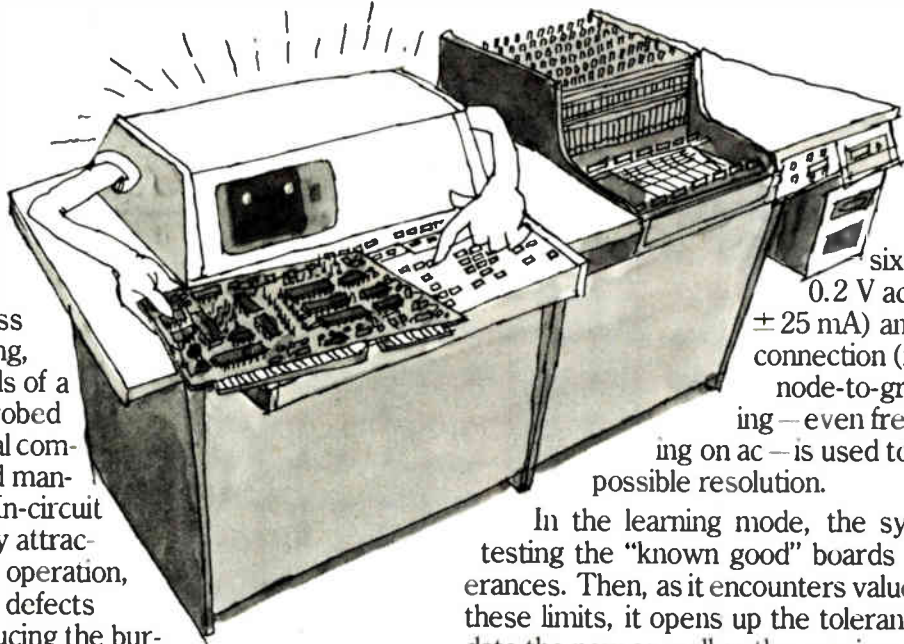
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As many people are finding out, however, the heaviest burden of all has less to do with testing than with test programming. Thus, if the in-circuit tester is to pay off as a screening device, it should not consume programming time more urgently needed somewhere downstream.

Teradyne's solution to this problem is an in-circuit tester (the L529) that writes its own test program while examining a small sample of "known good" boards. The human contribution to the process consists of telling the tester what kind of component (resistor, capacitor, semiconductor, etc.) appears at each node. This is a button-pushing exercise requiring not a semester's worth of electronics, but to make things even simpler the buttons are keyed to the user's own component designators (e.g., Q for transistors, R for resistors, etc.).

To develop the tests required for each type of component, the system employs various combinations of

six stimuli (0.2 V dc, 0.2 V ac, ± 2.5 V dc, and ± 25 mA) and two methods of connection (node-to-node and node-to-ground). Autoranging — even frequency autoranging on ac — is used to achieve the best possible resolution.

In the learning mode, the system first starts testing the "known good" boards to fairly tight tolerances. Then, as it encounters values that fall outside these limits, it opens up the tolerances to accommodate the new as well as the previous values. The ideal limits will of course be just outside the range of actual values measured on the sample of good boards, and the system automatically settles in on these tolerances. After about a dozen boards have been examined, the test system has a very good idea of what constitutes a "good board." The system, in other words, has been programmed — without tears.

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French mixing up a U. S. dish

Government maps attack on American telecommunications market
but some manufacturers wonder if it can succeed

by Kenneth Dreyfack, Paris bureau

Take a large quantity of private switching exchanges, sprinkle in a fair number of digital time-division switching systems, spice with a few telecopiers and telephone terminals equipped with cathode-ray tubes, and voilà, you have the French recipe for exporting more than \$200 million worth of their telecommunications equipment to the U. S. At least the telecommunications arm of the French Ministry of Posts and Telecommunications, known as PTT, exudes confidence about this concoction, but some of the companies whose hardware is in the mix wonder how it will turn out.

The export goals set by the PTT for 1982 are 30% of national production, with one third of that aimed at the U. S. This is considerable, especially in light of the current export levels of the French telecommunications-equipment industry.

The \$260 million total in export orders registered last year come to less than 10% of French production. But the PTT contends that market conditions are changing, as is French industry, and insists that the export goals are realistic.

"The American market is opening up," says Gérard Théry, head of the PTT's telecommunications division, the Direction Générale des Télécommunications (DGT). "The challenge of exporting to the U. S. should test the efficiency of the French telecommunications industry," adds Jean Syrota, director of industrial and international affairs for the DGT.

Syrota and others in the PTT believe that that part of the U. S. telecommunications equipment market open to foreign competition will come to \$4.5 billion within two or

three years. To realize their goal, the French would have to corner \$225 million of that market—only 5%, French are quick to point out. But \$225 million worth of what exactly do they plan to sell?

PBX out front. The thrust of the impending French invasion is to be in switching exchanges, especially in private branch exchanges (PBXs), where Syrota sees a potential market

of \$635 million. In an effort to tap that market, CIT-Alcatel, the telecommunications subsidiary of the CGE (Compagnie Générale d'Electricité) group, is considering setting up PBX manufacturing facilities in the U. S. that would make CIT-Alcatel more competitive, as well as put it closer to the market; the company now imports some American components and labor is cheaper in some

Rarin' to go. Jean Syrota, a director of the French post office's telecommunications division, is enthusiastic over the possibilities of exporting French-made telecopiers to the U. S.



Probing the news

parts of the U.S. than it is in France. CIT-Alcatel also has a research team in Washington, D. C., working on a switch design especially aimed at the U. S. market.

The PTT also believes there is a market for public digital-switching exchanges—among those independent companies that are not part of the Bell System—totaling some \$300 million to \$400 million a year. Some PTT officials cite the sale in 1974 and 1975, by Le Matériel Téléphonique, of two switching exchanges for the telephone system in Las Vegas, Nev., as evidence of the market. But industry officials are quick to point out the company was an ITT subsidiary at the time, and that the order was placed through ITT in the U. S. In other words, the sale was a one-shot deal.

Four French electronics companies are currently competing for a government contract for inexpensive telecopiers, another area in which the PTT has high hopes. The equipment will transmit standard-size copies over phone lines in 3 minutes, and have a price tag of about \$450. Still more than two years off by the PTT's reckoning, the product should prove "eminently exportable," to quote Syrota.

Terminal market. The government officials also believe that inexpensive terminals being developed for the French video-text system should also be successful abroad, especially in the U. S. The terminals will include a conventional handset, an alphanumeric keyboard and a display screen roughly 12 inches square, which could be either a cathode-ray tube or perhaps, in the future, a liquid-crystal display. The PTT figures the units would be reasonably priced when mass-produced. Video-text terminals are due to be installed in 3,000 homes in the Paris suburb of Vélizy next October, with each terminal linked to data banks containing such information as train schedules, weather forecasts, and bank statements.

While some within the French government foresee millions of inexpensive telecopiers and terminals sailing westward across the Atlantic

Teletel + Antelope = high hopes

Along with their push into telephony, the French are trying hard to gain the lion's, if not the cub's, share of the computerized communications market that uses television sets. The French PTT and its engineering group have set up aggressive marketing organizations that are pushing world-wide sales of both the version that uses a link by telephone wires (dubbed Teletel) and the one using radio transmission (Antelope).

They have been showing the equipment all over and, according to Sofratel, their group directly concerned with such matters, a radio-based system for Saudi Arabia is under discussion. More importantly, perhaps, tests are planned in the United States with both the National Broadcasting Co. and public broadcasting systems said to be interested.

Commercial television sets equipped to use the system must be modified with an add-on decoder, and there's the rub. These devices are manufactured by Thomson CSF and Texas Instruments Inc.'s French operation. Without the use of large scale integration techniques—not yet accomplished—the price is estimated at over \$1,000 and perhaps up to \$2,000 depending on production volume and features. This may be a rather high price to pay for weather and stock reports and the like. Right now, only several hundred television sets are set up at the Paris stock exchange, but several thousand units will be tested in 1980.

in five or six years, industry executives take a much more cautious view. The goal of exporting 30% of production is "a tough proposition," says Pierro Labro, an international marketing director for CIT-Alcatel. Labro notes that his company did export 28% of its production in transmission equipment and 25% in PBXs last year. But in public switching, which accounts for half of CIT-Alcatel's business, the export rate was less than 12%.

What's more, Labro's estimates of the size of the U. S. markets for public and private switching systems are way below those of the PTT—half as much as the market for PBXs. In public switching and transmission equipment, Labro sees no more than "drops in the bucket" for the French in the U. S., this despite the fact that CIT-Alcatel has sold some \$25 million worth of analog multiplexers to MCI Inc. of Washington, D. C., over the past five years. Peripheral devices are an area where Labro sees interesting, but not very concrete, market possibilities. "We must first see whether these new products will be successful in France," he says. "If so, there is no reason they should not be successful elsewhere."

Can't do it. Officials of the Thomson-CSF Electronics Group, whose principal telephone switching activities stem from the acquisitions in 1975 and 1978 of French subsidiar-

ies of Sweden's LM Ericsson and ITT, concede in private that they will not meet the PTT export goals by 1982. But Marc de Saint Denis, vice president of the group's newly-reorganized telecommunications division, Le Matériel Téléphonique Thomson-CSF, says the goal should be reached by 1984. The company has a long way to go. Export orders for public and private switching exchanges combined last year came to a mere \$36 million for switching equipment on annual sales totaling \$680 million. Saint Denis contends that the group is in much better shape than the figures indicate. Thomson has been getting its house in order internally, he says, so that it will be able to make a serious attack on the international market.

While Thomson executives refuse to say how the company plans to enter the U. S. market, there are strong signs that it will follow the same lines taken by CIT-Alcatel for reasons of economy—acquisition of relatively small U. S. firms and commercial agreements with American companies judged to have effective marketing networks. Actually, the French have little choice. As François Dufaux, head of Thomson's private switching and telephone division puts it, "It would cost us as much to set up our own marketing operations in the U. S. as it has cost us to set them up here in France." □

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Probing the news

Communications

How the Air Force found its signals

The true adventures of a team of troubleshooters
and some electronic detective work beneath the tropical sun

by James B. Brinton, Boston bureau manager

Bermuda Triangle fans would have loved it; the United States Air Force, however, was not amused.

Not that anything was disappearing into the thin Pacific air, but some readouts from its new Omega navigation sets were weird. Some refused to work near Hawaii, while others worked well. Some could only receive Omega signals in the air, never on the ground. Some never received enough signals to navigate with, while others would operate perfectly for up to 10 hours, then "get lost." Plainly, Air Force Omega had problems.

Built under a \$2.766 million contract for 679 units and spares by the Dynell Electronics Corp, Melville, N. Y., the Air Force version, AN/ARN-131, is supposed to be accurate to within 2 miles 95% of the time. And in worldwide tests, according to Harold W. Underwood,

Omega task force group leader at the Air Force Aeronautical Systems division at Wright-Patterson Air Force base in Ohio, it had performed up to specification. But, he adds, soon after installation aboard Pacific-based C-130s in late 1977 and early 1978, "reports started pouring in that the units were not performing as advertised."

The Air Force assigned its Systems and Logistics Commands to the problem, and the result was an eight-man engineering team based at Wright-Patterson and headed by Underwood. Soon the team and a Dynell field engineer were flying out to the Air Force's "Pacific triangle."

Going blank. On reaching Hawaii, the team was presented with a C-130 that normally lost its Omega capability on takeoff. Worse, it often could not receive the three Omega stations needed to establish position

even on the ground; when it did, the indicated position could wander several miles even with the plane immobile. Finally, when the plane flew through turns, its Omega set indicated a turn in the opposite direction. It seemed to be a good place to start.

From the outset, says Underwood, the team suspected electromagnetic compatibility problems. And the mysterious "no-Omega zone" around Hawaii's Hickam Air Force Base hinted at ground-based interference, too.

"We began by surveying the plane with an rf probe," says Underwood. Crawling around on hot aluminum under a tropical sun was nobody's idea of a vacation, but "we found significant interference."

There were three sources: the aircraft's very-high-frequency omnirange system (VOR), its tactical air

navigation system (Tacan), and its autopilot. All three were leaking 400-hertz power-line harmonics into the Omega antenna; this was particularly bad as one Omega frequency, 13.6 kilohertz, is an exact multiple of 400 Hz. The worst offender was the VOR, and since VOR installations were fairly standard throughout the C-130 fleet, the fix had to be in the Omega system.

More radio-frequency survey work located an area just forward of the vertical stabilizer that was relatively free of the interference; the Omega antenna was moved there and, suddenly, the Pacific triangle began to lose some of its mystery.

What had seemed like an occult 200-mile-radius anti-Omega zone around Hickam Field was suddenly explained. Flight crews normally turned on their VOR sets about 200 miles away from Hickam and the VOR's interference would knock out the Omega. Because of the long time constants built into the ARN-131's very-low-frequency receiver, 10 minutes could pass between VOR turn-on and Omega failure, making cause and effect hard to relate. As for the set's failure to track the aircraft through turns, there was an error in heading synchro wiring. Before Omega's installation, no one had noticed the reversal.

But the problems of poor reception and of immobile planes changing their Omega-derived positions still had to be dealt with. The team tackled this by changing the ARN-131's programming.

"We were ready to try some

changes even before leaving Wright-Patterson," says Underwood. Dynell representatives, working under a performance-improvement incentive clause, had already suggested some changes based on commercial Omega experience. These included one to the so-called range deselect, or close-station-lockout algorithm, allowing navigation sets to use signals from stations as close as 200 nautical miles instead of 600. Another change allowed use of signals from stations 8,800 nautical miles away, an increase from the former 8,000.

In a test flight comparing modified and unmodified ARN-131s, the modified unit not only used more stations, according to Underwood, but also was rock-solid in positioning. The unmodified set worked fewer stations, he says, and at times wandered several miles from its correct position. After checking other Hawaiian C-130s to make sure the new antenna solved the interference problem—it did—the team flew on to bases on Guam, in Japan, and in the Philippines. The antenna fix worked everywhere.

Interference. But on the flight from Japan to the Philippines, the team encountered a vlf effect known as modal interference. To very low frequencies, the space between earth and the ionosphere acts like a giant waveguide. Engineers make waveguide plumbing as smooth as possible to avoid discontinuities that can degrade the phase coherence of a signal. But nature supplies many discontinuities in its atmospheric

waveguide; near vlf stations, modal interference arises as part of the signal bounces up and down between earth and ionosphere, destroying phase coherence.

Something similar happens when a vlf wave passes through the earth's day-night line: the fact that the ionosphere is higher on the night side causes massive modal effects that can degrade Omega's positional accuracy.

Long-path reception was the cause of the unmodified set's positional wanderings in the last Hawaiian test flight, and in response the engineers turned out a new algorithm to detect either modal interference or long-path signals. With four or more signals present, the set now would ignore a contaminated signal; with only three signals available, the set would shift into a dead-reckoning mode until the situation changed.

Mystery solved. Other tests were made and other minor fixes suggested or rejected, but the bulk of the problem appeared solved by mid-1978. Later that year, a follow-on test and evaluation took place over an area from North Carolina to the western Pacific. All the fixes worked well, according to the team's report.

The Air Force approved the alterations for retrofit aboard Omega-equipped C-130s and changed antenna placement instructions for new installations. In addition, a new processor board equipped with electronically alterable read-only memory was ordered from Dynell in May 1979. Says Underwood, "We want to be able to change programming again to take advantage of experience, and we'll be able to do that cheaply with the new alternative stores."

For all the apparent trouble, the fixes turned out to be fairly low-cost ones. Dynell is supplying the new boards and a good deal of engineering for \$747,572 and antenna relocation is being done in most cases by Air Force personnel. Dynell will begin delivering the new processor boards in November with the last due in January 1980. Thus the alterations could be complete in early 1980. The Air Force will have solved the Pacific triangle mystery, and improved its Omega set's basic performance into the bargain. □

How Omega works

Omega was originally conceived by the Navy as a maritime navigation system. It now uses seven very-low frequency transmitter stations around the world from Japan to Norway. Receivers monitor the phases of transmissions from three or more stations and determine position by computing the range to each station. Omega does not use azimuth information, but will reject signals from stations too near the same bearing; such geometry cuts positioning accuracy.

In 1974, knowing that Coast Guard Loran-A stations were to go off the air in 1977, the Air Force began developing a low-cost airborne Omega set for transports like the C-130. Designated the AN/ARN-131, it consists of an antenna and preamplifier, a multichannel receiver, and data-processing and support electronics. The processor is a simple computer with instructions stored in the read-only memory; its output is position data, winds aloft, and other information useful for navigation. It also decides which Omega signals to accept or reject. □

Components

Discretes show new life

First quarter sales up by 32% with No. 1 Motorola crediting pull-through effect of microprocessors

by Larry Waller, Los Angeles bureau manager

A new semiconductor growth business has quietly appeared on the scene: discrete devices. Operating outside the spotlight illuminating the flashier integrated circuit sector, discrete component makers have been racking up impressive sales gains. The latest is 1979 first-quarter orders compiled by the Semiconductor Industry Association: discrete devices were up a whopping 32% to \$553 million from \$418 million in last year's first quarter. Shipments were worth \$454 million, up from \$364 million.

Although such gains no doubt reflect the superheated demand for semiconductors, they could be the first signs of what some in the industry see as a possible new era of even higher growth. Certainly it is a far cry from the 6%-or-so expansion chalked up in 1978 with \$1.590 billion in sales, compared with \$1.394 billion in 1977.

What's more, new markets are in sight. Industry consultant Glen R. Madland of Integrated Circuit Engineering Inc. in Scottsdale, Ariz., sees two important ones. By far the biggest promise is for components to implement new high-efficiency "rectified" electric motors, such as that proposed by Reliance Electric Co. It could amount to \$1 billion a year, he thinks, when the motors get into full production. Also, V-groove MOS rectifiers have much potential, with more flexibility in circuits than the silicon controlled rectifiers they will replace.

Another industry observer points out that makers of industrial motors are seeking to acquire makers of discrete devices or start up their own captive operations. The latter course

would permit them to put their investment only in the most up-to-date equipment and processes.

Moreover, even though discrete devices represented a declining portion of all sales, big semiconductor firms themselves never underrated their importance. They not only generate healthy profits, but are more stable and predictable than the mercurial ICs. Sales leader Motorola Inc.'s Discrete Semiconductor division, for example, rolled out about \$350 million worth in 1978, followed

Optimist. When Gary Tooker became head of Motorola's discrete division, he found it somnolent and in need of major renovations.



by Texas Instruments Inc.'s \$254 million. Clustered far behind the leaders, RCA Corp., General Electric Co., and Fairchild Camera and Instrument Corp. each did business at the \$100 million level. (Western Electric, the equipment arm of AT&T, is far and away the largest discrete producer, but it is a captive operation.)

A tip-off to profitability is found in Motorola's figures. Although the firm never breaks out discrete income from Semiconductor Group totals, sources say at least half of 1978's \$107 million pretax and overhead profit comes from non-integrated-circuit operations.

Micros do it. What, besides strong business conditions, supports the good health of the discrete components business, and prompts even rosier growth projections for the 1980s? The big factor, answer Motorola officials, is a fundamental change. "It's the pull-through impact that microprocessors have on some discrete product families," says John R. Welty, a senior vice president of Motorola and general manager of the Semiconductor Group. "Microprocessors cannot function by themselves, so their impact on discrete components is definitely positive." Four product lines hold dramatic potential and are emerging, he says—power transistors, rectifiers, thyristors, and optoelectronics. The last-named devices, in fact, are the hottest of all components, registering an 88% gain in orders during the first quarter over last year's similar period.

Indeed, the changes occurring at Motorola's discrete operation illustrate quite well what it takes to

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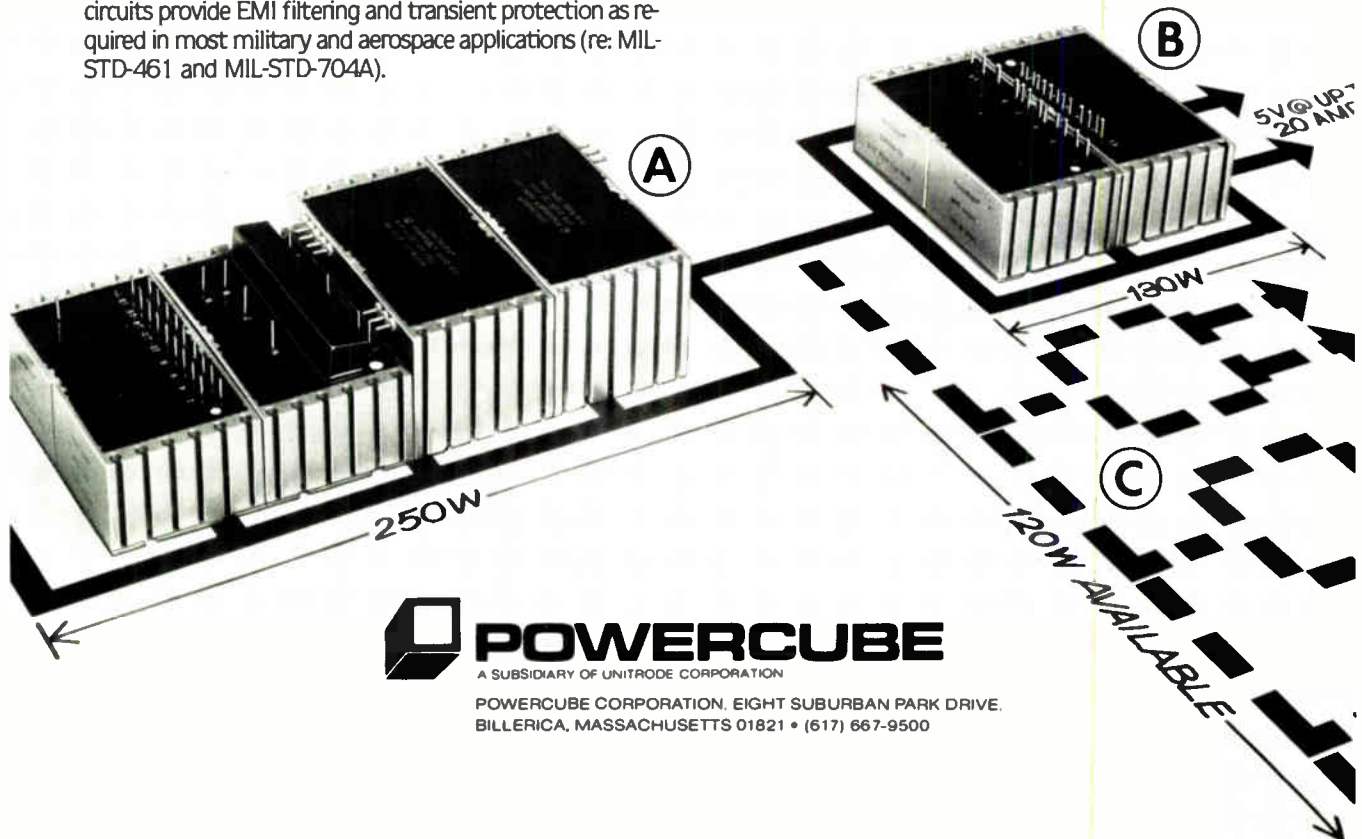
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Circle 92 on reader service card

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exploit the business to the fullest, point out industry sources. Guiding Motorola's discrete fortunes since recession-ravaged 1975 has been Gary Tooker, 39, who was tapped by Welty for the renovation job. An EE and Motorola veteran since 1962, he is given high marks for bringing the division out of doldrums stemming only in part from the business slump.

Furthermore, problems that Tooker encountered at the Phoenix-based division in 1975 applied to most other large suppliers. For one thing, there were large no-growth areas where products had been on the market a long time with no changes. Despite many lines selling fairly well—some stayed profitable right through the recession and the division itself stayed barely in the black—Tooker and his new staff knew these products could not last much longer.

Package hunt. "In power transistors, for instance, there wasn't the right package, especially in plastic, and we had no answer to single-diffused devices. Also, we had lost market share for three years in a row." Furthermore, the division kept adding device types, so that at peak it was saddled with about 200,000 different ones. Finally, Motorola discrete sales and service suffered from the unaggressive and unresponsive attitudes toward customers that hampered IC performance. "It was definitely an overhaul situation," now observes Tooker, who adds he did not listen to the talk—in those early days of the microprocessor—that discretely were doomed.

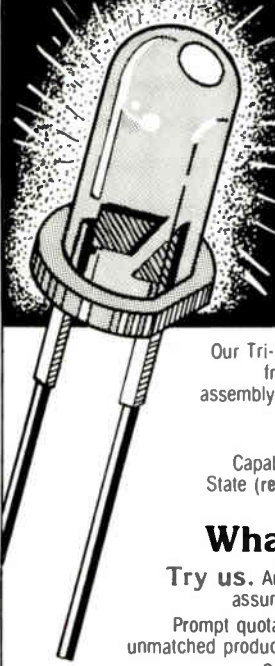
Motorola strategy took on a two-pronged approach to product planning and development. First, emphasis was placed on lines that were in demand and, second, products immune to integration were given priority. "It was not enough just to develop the right products in the right package," says Tooker, but it was critical for longer-term exploitation to come up with lines that would not be lost by fabrication into monolithic IC chips.

Even that early in the microprocessor era, it was apparent that discretely could continue as a strong

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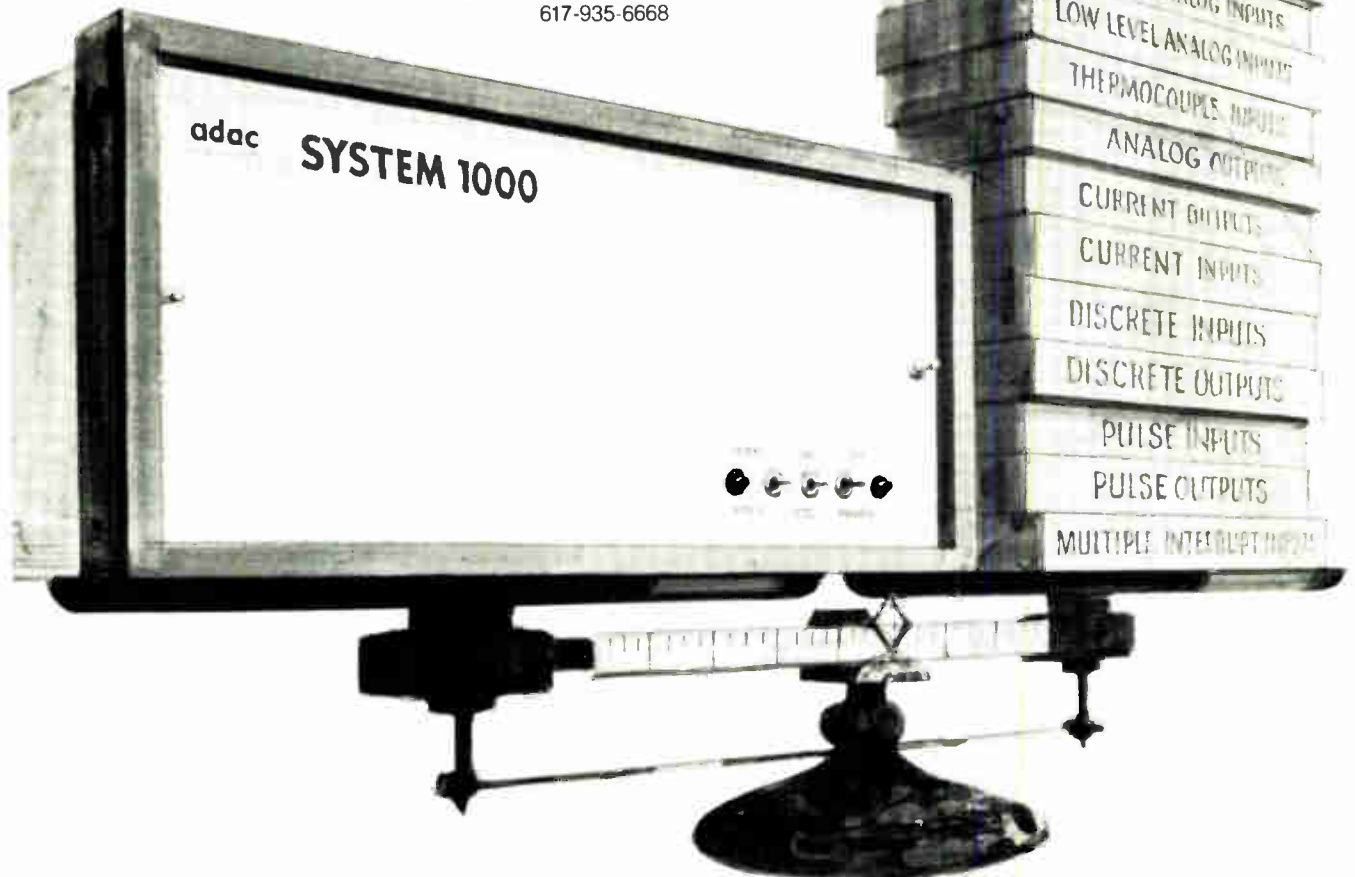
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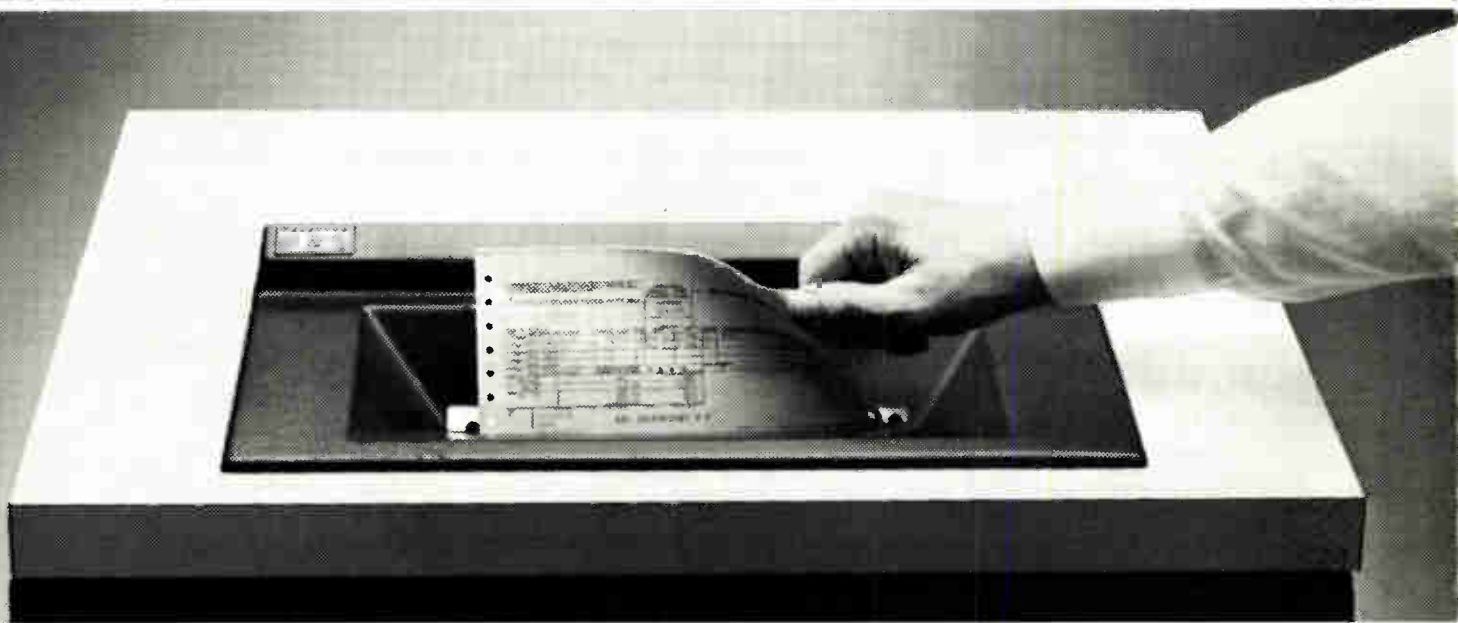
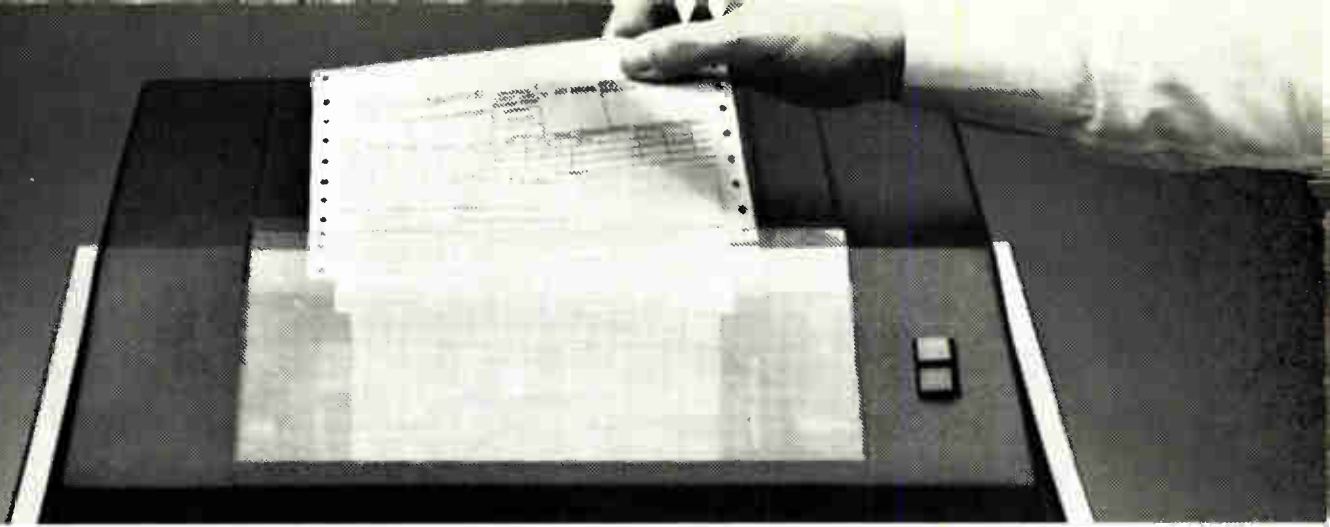
business, if positioned correctly. "Depending on the application," as Welty says, "a number of different types of discretes are required for rectification, voltage regulation, power handling, and for carrying out the actions determined and ordered by the microprocessor."

Although Tooker and his associates pushed changes at an all-out pace, their magnitude meant several years would pass before the full impact was felt. Not the least was correcting the single-diffusion omission by investing heavily in building an epitaxial technology base. Also necessary was conversion to mechanical wafer processing, another big capital outlay. Coming up with "hot" packages for small-signal power devices, namely the plastic TO-92 and TO-220, was another tardy move that had to be made, says Tooker.

Balance vital. One aspect of discretes that cannot be overemphasized, believes Tooker, is balance between lines. "It's the key to success, since each product is in its own unique marketplace." What works well in one line may fail in another, so having a broad base is vital, "because competition can get unbelievably fierce in some areas." An example, points out the Motorola vice president, was power transistors, "where we had 55 competitors, half of whom you never heard of."

After the record sales of 1978, the Motorola discrete outfit claims the top spot in the low-frequency, small-signal, radio-frequency power, and zener diode areas. The stream of new products included microwave and pulse power components, cable television and rf modules, optocouplers, and MOS field-effect transistors.

Worth noting are Motorola's thoughts on penetration into the non-microprocessor automotive market, largely rectifiers, zener diodes, and power and small-signal devices. From a value of about \$3.80 per car in 1978, the company expects the total to reach \$11.50 per car by 1982 or 1983. "The difference," says Welty, "will be almost entirely created by the variety of non-microprocessor-related uses." □



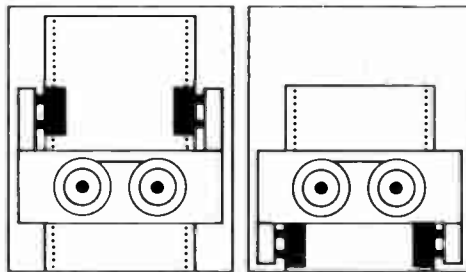
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Semiconductors

The shortage tune plays on

Makers of dynamic RAMs, E-PROMs, and low-power Schottky expect the tight situation to persist right into 1980

by Howard Wolff, Assistant Managing Editor

Some advice for amateur economists looking for signs of the oft-promised recession: you are wasting your time waiting for semiconductor memory lead times to start shortening. For the picture in erasable programmable read-only memories, 16,384-bit random-access memories, and low-power Schottky logic continues to show demand far exceeding supply, with no surcease in sight.

Among the factors expected to keep 16-kilobit RAMs from spending much time on manufacturers' or distributors' shelves in the foreseeable future are these:

- Intel Corp.'s new solid-state disk replacement, the FAST 3805 [*Electronics*, June 7, p. 43], will use so many 16-K RAMs that Intel is expected to go offshore to buy some.
- Storage Technology Corp. and Memorex Corp. plan to use 16-K parts in their memory peripherals instead of the charge-coupled devices with which they were designed [*Electronics*, June 21, p. 34].
- Other high-volume applications among users of the parts are being added almost daily.

Near panic. From the manufacturers, the vote is unanimous: the shortage goes on. A. C. D'Augustine, strategic marketing manager for MOS memory at Texas Instruments Inc. in Houston, offers this assessment: "If our customers are right and not overstating the demand, 16-K dynamic RAMs are going to be in short supply through 1980. It's damn near a panic situation out there with our customers going bananas trying to lock down supplies for 1980." D'Augustine says that the "very, very clear shortage of 16-K parts" was likely precipitated by customers

either underestimating their needs or not communicating their needs to vendors because they expected an oversupply and price cuts.

That's not all. Doug Turnage, who handles low-power Schottky (LS) product marketing for TI in Dallas, says the situation is similar with those devices. As with a number of TI memory products, LS devices are still on allocation. With this program, customers can obtain delivery within 16 to 20 weeks.

Demand has increased lately, Turnage says, adding, "There are some indicators that say the economy should soften, but it's not apparent in our business yet." As for double ordering, he is certain some is going on but does not know how much. On the memory side, D'Augustine notes: "We're not committing ourselves to the 1980 product right now. And the allocation should prevent double ordering in the short term."

Under the allocation program, TI is quoting 16-week deliveries on 16-K RAMs, and about the same on 4-K devices. In E-PROMs all TI products except the 2708 (a three-supply, 8-K part) are on allocation, with 12-to-16-week deliveries quoted.

For officials at Mostek Corp. in Carrollton, Texas, the situation matches TI's. "We're building far more [16-K RAMs] than what we said we'd build [this year] and it's still not enough," says Tim Propeck, marketing manager for the group that handles dynamic RAMs.

National sales manager Dick Konrad says that Mostek began allocating 16-K memories in mid-March. Deliveries are quoted at 26 weeks, and the shortage has reached the point where Mostek is unable to take on major new customers. Static RAMs are not on allocation and lead time is 26 to 30 weeks.

Mostek is an important market factor in 4-K RAMs, where Propeck notes that demand is also "very, very strong." He says that though "we do think that demand for 4027-type 4-Ks is peaking or about to peak," Mostek expects its business to remain strong mainly because a number of offshore competitors are building other parts.

Gene Miles, director of marketing for MOS memory operations at National Semiconductor Corp. in Santa Clara, Calif., says lead times have been fluctuating for some time

Not us, says Intel

Some competitors are saying privately that one reason for the shortage of 16-K dynamic random-access memories is that Intel Corp. is, in effect, getting out of the business to concentrate on higher-margin parts like static RAMs and larger erasable programmable read-only memories.

But Barry Cox of Intel vehemently denies that such is the case. Says the marketing manager at the Memory Components division in Aloha, Ore., "Intel is not, and has no intention of, going away from the dynamic RAM market." Cox explains that what has happened is that capacity limits have forced Intel to concentrate on products like static RAMs and E-PROMs for which it is the sole source.

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between 16 and 26 weeks. What's more, he sees no softening in the 16-K RAM market. "We estimate that the industry will ship in calendar 1980, 100 million to 110 million units of three-power-supply parts and 15 million to 20 million of 5-volt-only," he says. "The total will be double that of calendar 1979, which will come to nearly 60 million or maybe a little more."

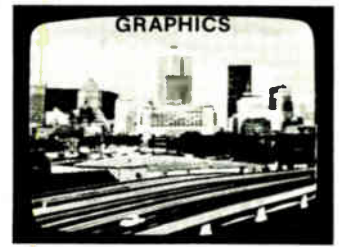
Capacity short. At RCA Corp.'s Solid State division in Somerville, N. J., Jim Magos, marketing manager for memory and microprocessor components, puts the 4-K RAM backlog at 30 weeks, up from 24 weeks two months ago. The part Magos refers to is the complementary-MOS-on-sapphire 5144, and he points out that the shortage is due to demand outstripping capacity, not to any process problems.

How do users view the situation? Analog Devices Inc. of Norwood, Mass., a user of low-power Schottky parts, decided to go to a distributor. The result, says Theodore G. Koukotos, purchasing manager for production components, is "they have backed us to the hilt and we are sticking with them. We can get delivery in as little as eight weeks."

Louis M. Hafeman, senior electronics buyer at Wang Laboratories Inc. in Lowell, Mass., says some U.S. makers of LS are just saying "1980" and letting it go at that. He says that 4-K and 16-K RAMs are among the most difficult of parts to get, with the latter "a nightmare."

Less frenzy. If there is any faint sign of a softening, it seems to be discerned by some distributors. Seymour Schweber, president of Schweber Electronics, Westbury, N. Y., says, "The situation seems to be the same, but the frenzy has let up." One reason, he says, is the long lead times themselves, which have discouraged users from ordering. For Roger E. Green, executive vice president of Arrow Electronics Inc. in Greenwich, Conn., there have been some surprises. Parts not expected for weeks or months turn up, and in memories, especially 2708s and 2114s, Arrow is getting "very regular, dependable deliveries." □

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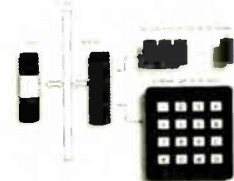
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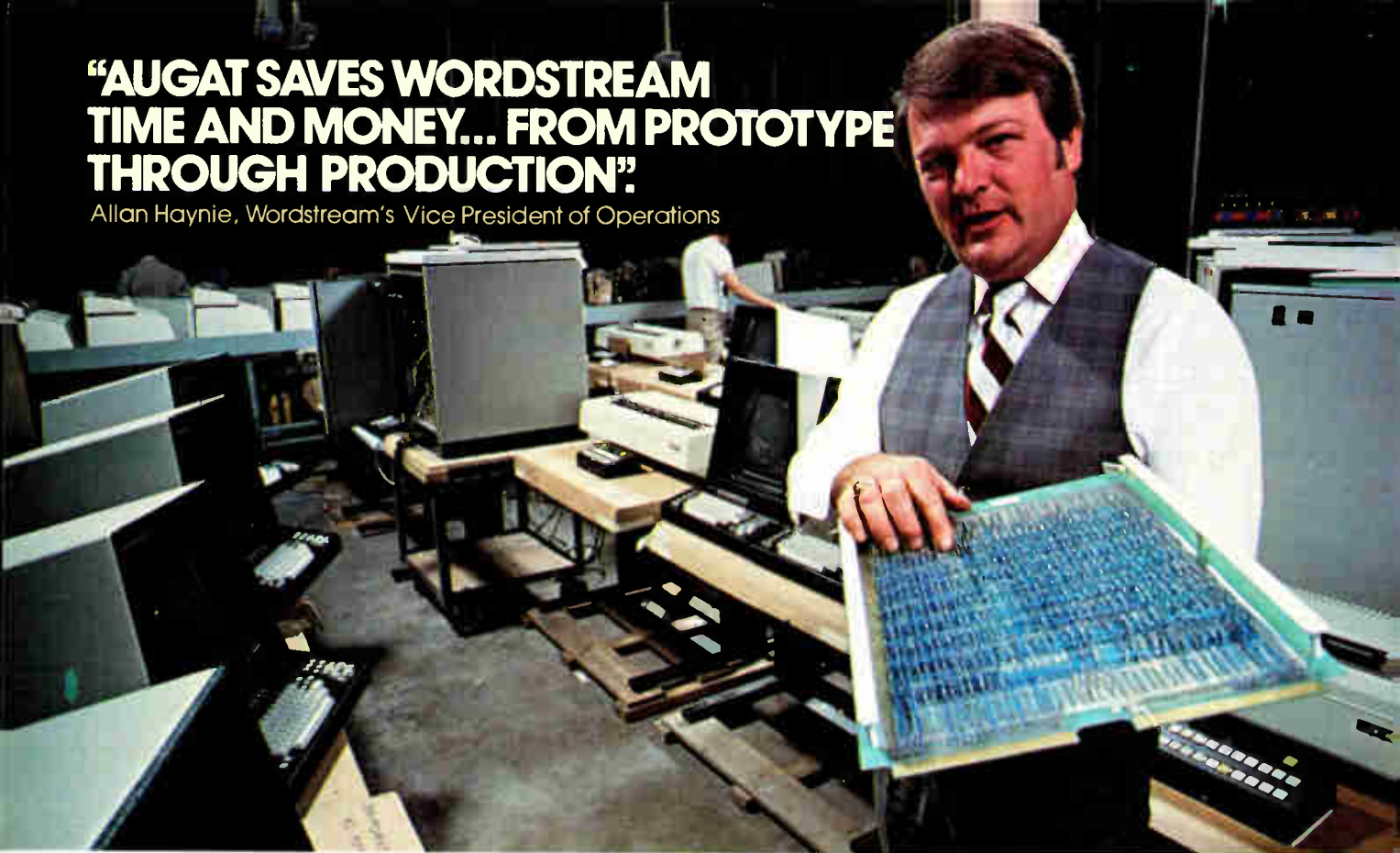
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Allan Haynie, Wordstream's Vice President of Operations



The Wordstream Corporations are subsidiaries of MAI Inc. They manufacture and market the Wordstream™ word processor, a shared logic system capable of handling 12 video display terminals, 10 diskette drives and three printers at once.

At the heart of the Wordstream system, you'll find Augat wirewrap* panels. Allan Haynie, Wordstream's Vice President of Operations, gives the details. "We use a large Augat board with about 250 integrated circuit chips in each printer station, diskette station, visual display and CPU. These boards are fabricated for us at Augat manufacturing facilities in Attleboro and Mashpee, Massachusetts and El Campo, Texas. Wire-wrapping is performed at their Datatex subsidiary in Houston."

At one time, Wordstream assembled their own IC panels. When asked why they switched to Augat wire-wrap, Allan Haynie replied, "basically, there were two reasons—the economy of Augat wirewrap panels and the service of Augat engineers. For

example, Augat people worked closely with ours to develop a prototype board using their Data-logic™ computer-aided design service. They also designed the most economic way to wrap the boards. As a result, we've saved time and money during our prototype and design stages."

In the past, some users felt that wire-wrapping was not cost effective in large volume programs. Wordstream's experience shows that the opposite is true. Says Haynie, "because Augat supplies completely wired boards, our in-process inventory costs are significantly reduced. In addition, Augat panels give us the flexibility to implement design

changes on the production line and in the field quickly and easily. We don't have to replace boards, just rewire them. And that means we can assure our customers that



their Wordstream system will always remain at the state of the art.

Even our final quality control is simplified with IC's replaced right at the test stations quickly and easily with no need for routing through production."

If you'd like to save time and money from prototype through production, listen to the words of Allan Haynie at Wordstream. Call your nearest Augat representative. Or contact us directly. Augat Incorporated, 33 Perry Avenue, P.O. Box 779, Attleboro, MA 02703. Tel. 617-222-2202.

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Peripherals

Now for the math-processing chips

New devices that perform floating-point, fast Fourier, and other jobs are designed to support microprocessors

by William F. Arnold, San Francisco regional bureau manager

As microprocessors appear in more sophisticated applications, they are getting a new kind of support: arithmetic-processing peripheral chips that are dedicated to performing floating-point, fast Fourier transform, or other operations not normally part of a processor's main instruction set. Consequently, potential vendors see them filling a gap between slower but less costly software written for specialized arithmetic processing and the faster, more expensive approaches using minicomputers or board-level processors.

The latest math chip is from Advanced Micro Devices Inc., the Am9512 floating-point processor chip, designed to conform to the floating-point standard proposed by the Institute of Electrical and Electronics Engineers [*Electronics*, May 24, p. 98]. It follows a sister part called the Am9511 arithmetic-processing unit, a general-purpose number manipulator that the Sunnyvale, Calif., company introduced last year as the first of its kind.

But AMD will not be out there alone for long. Giant Texas Instruments Inc. expects to announce early next year its plans to enhance the TMS 9900 family with arithmetic processors and possibly other special-function chips, such as fast-Fourier-transform, floating-point, and string-manipulation processors, says Tom Miller, strategic marketing manager for MOS microprocessors in Houston. Miller says he would not be surprised if other companies announce similar plans this year and next.

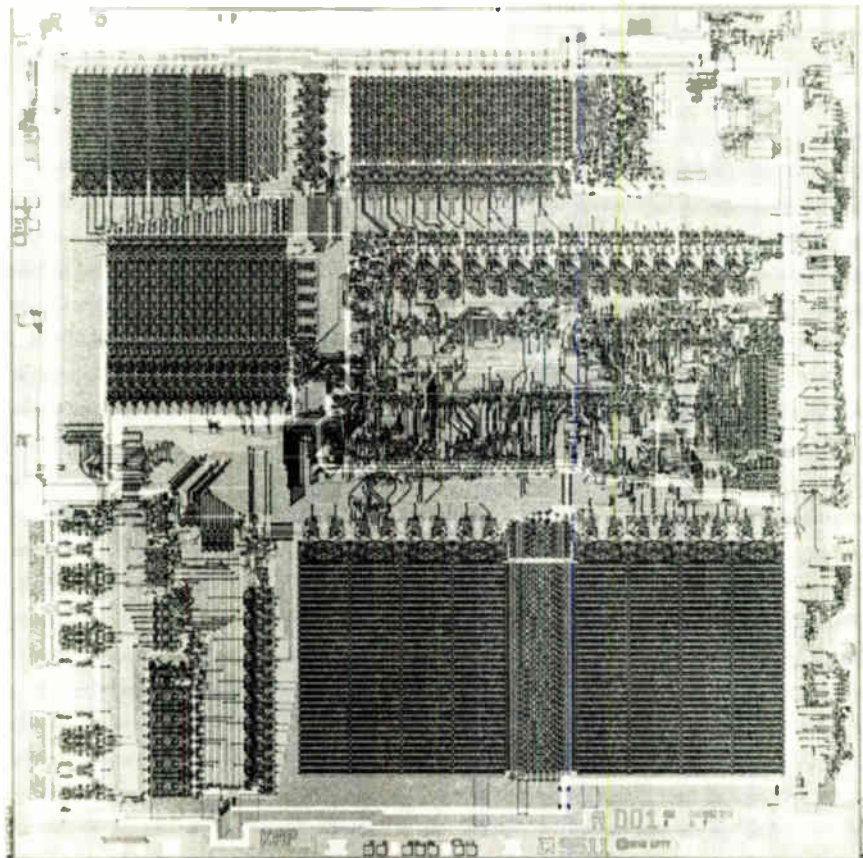
His hunch is correct. Intel Corp. of Santa Clara, Calif., is known to be developing an 8087 coprocessor

designed to do high-speed floating-point calculations for the 8086 16-bit microcomputer [*Electronics*, April 26, p. 33]. Neighboring National Semiconductor Corp. hints that it, too, is studying arithmetic processing chips, and Signetics Corp. of Sunnyvale, Calif., admits it is eyeing the concept. American Microsystems Inc., also in Santa Clara, says its signal-processing peripheral package will also include arithmetic func-

tions, such as fast Fourier transforms and multiplication [*Electronics*, Sept. 28, 1978, p. 50].

Giving a choice. Why are these chips emerging? "We're beginning to reach the limits of the capabilities of the processor itself," Miller explains. "From a cost standpoint, it's better to unbundle those functions so the customer can purchase what he wants, rather than embedding them in the processor and driv-

Started it all. This is Advanced Micro Devices' Am9511 arithmetic-processing unit. A general-purpose number manipulator that was introduced last year, it was the first of its kind.



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Probing the news

ing up its cost." Adds AMD's Joseph H. Kroeger, manager of MDS peripheral applications, "These chips allow you to pick up speed in the system without buying faster memories or microprocessors."

The need for arithmetic-processing chips is "definitely there," affirms Ron Baldrige, strategic marketing manager for microcomputer products at Mostek Corp. in Carrollton, Texas. Mostek has not yet decided on a course. It could second-source AMD's 9511 or Intel's planned 8087, which Baldrige says "would probably make sense, since we're doing the 8086" [*Electronics*, Nov. 23, 1978, p. 46]. Alternatively, Mostek could start from scratch on its own, but it would take longer to market the products.

The concept seems to be working for AMD—Kroeger says that "business is taking off nicely." One reason is that the 9511/12 family offers a gain of 5 to 50 times in performance over the use of software. It should, because the powerful 9511 handles 16- and 32-bit fixed-point operations as well as 32-bit floating-point arithmetic. Besides the usual add, subtract, multiply, and divide, it performs such complex operations as square root, exponentiation, and logarithmic and trigonometric function evaluation.

For real time. With those abilities, the 9511 is designed "to be useful in real-time environments like navigation systems, Fourier transforms, or graphics displays," Kroeger says. The new 9512 [*Electronics*, June 7, p. 35], on the other hand, is aimed at the very different data-processing market where "the primary interest is in the precision and dynamic range, so that we have to surrender some execution time [it's 10% to 20% slower]," he says.

The 9512 can perform 32-bit single- and 64-bit double-precision floating-point arithmetic in the four standard functions of add, subtract, multiply, and divide. To get that precision, however, AMD had to leave out the transcendental functions. "There was no room in the microcode," Kroeger says.

Even so, stuffing that much math

muscle onto an 8080-compatible device takes a lot of circuitry, such as a dedicated 16-bit processor, various registers and stacks, and a control read-only memory. It adds up to more than 21,000 transistors, or five times that of an Intel 8080, on an n-channel silicon-gate MOS chip more than double the size of AMD's version of the 8080. This is one reason AMD sells the two peripheral chips at \$195 each or \$175 in quantity—still less expensive than other hardware solutions costing \$500 and up, the company says.

Another way. TRW Inc.'s Electronic Components division in Redondo Beach, Calif., takes another tack with its "subsystem on chips," according to William Koral, manager of product development and applications of the LSI Products division. These are entirely dedicated parts for digital signal processing, designed to be a faster complement to a slow microcomputer.

Where AMD's devices are processors whose instructions between math operations slow them, the TRW versions are fully parallel 8- and 16-bit four-quadrant multipliers. They are not programmable, so there are no instructions to wait for. Also, because signal processing demands very high speed, TRW has turned to fast bipolar technology. The 8-bit multiplier, for example, works at 45 nanoseconds, the video rate. It has 5,000 active elements on a 150-square-mil chip and sells for \$59 in lots of 100. The larger multiplier/accumulator has 30,000 active elements and multiplies in 200 ns; it is on a 320-by-340-mil chip.

But is the potential market large enough to support all this interest? Although AMD says it is doing fine, Kroeger admits that the overall market "isn't that great—remember, a lot of people build systems that don't take math." Even so, he envisions product growth, such as a floating-point processor for the Z8000 16-bit microcomputer family that AMD second-sources from Zilog Inc. Mostek's Baldrige says that "three or four basic chips will be defined" after the dust settles from various chipmakers' product offerings, possibly including basic math, binary-coded decimal, and floating-point functions.

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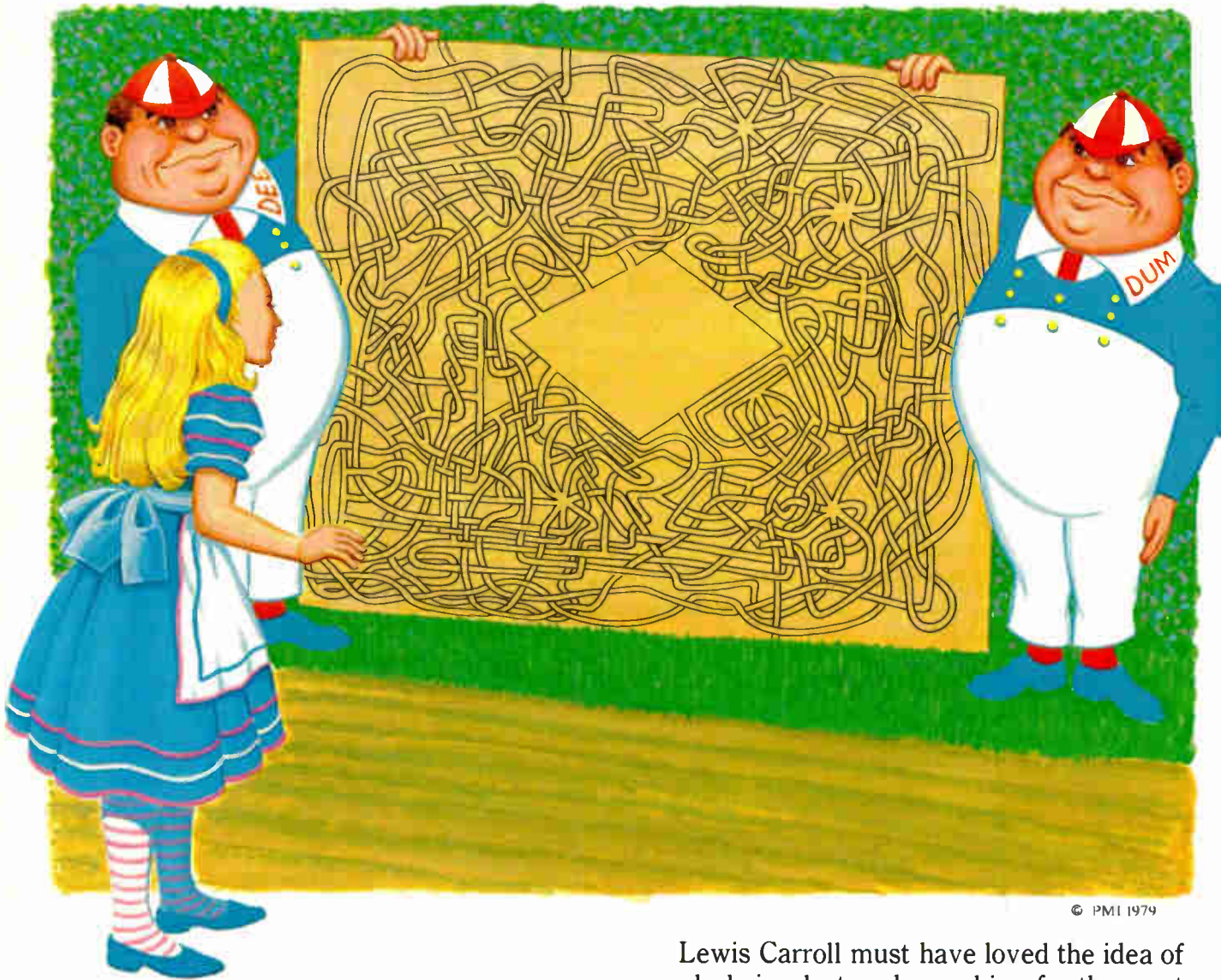
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The Linear Wonderland Op Amp Mischmasch



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“I was thinking,” Alice said very politely, “which is the best way out of this wood?”

But the fat little men only looked at each other and grinned.

—*Through the Looking Glass.*

Lewis Carroll must have loved the idea of people being lost and searching for the most logical way to turn, because he put Alice in that situation so often. His interest was further reflected in the complex mazes and labyrinths he drew for his friends, some of which he published in his family’s private magazine, *Mischmasch*.

By way of explanation, he noted, “The name is German and means in English ‘midge-madge’, which we need not inform the intelli-

gent reader is equivalent to 'hodge-podge'."

If he were around today, Carroll would have to look no further than Linear Wonderland to find a perfect mischmasch in the confusion surrounding precision op amps. Engineers are faced daily with a labyrinthic plethora of data sheets describing operational amplifiers of every variety—with some of Wonderland's wonders trying to suggest they can fill all your op amp needs.

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The most powerful 8-bit MC6809. It shrinks

Motorola's MC6809 drives down the high cost of software generation and does more for future systems than any other general-purpose 8-bit microprocessor.

While designed to handle high-level languages like PASCAL and BASIC, the MC6809 is also superbly efficient in assembly language applications. Efficiency means less code, and less code means lower costs. MC6809 speed and power are unbeatable, too. Not only that, the MC6809 is available right now.

Features team-up for efficiency.

More addressing modes than the other 8-bit MPUs, an optimized consistent instruction set enhanced by powerful 16-bit instructions, and uniquely versatile data manipulation on stacks work synergistically for increased software efficiency.

These features, plus 24 indexing submodes, promote the use of modern programming techniques like position independent code, re-entrancy and recursion. Auto-increment and auto-decrement indexing permit efficient block and string moves. Stack pointer indexing accommodates structured programming.

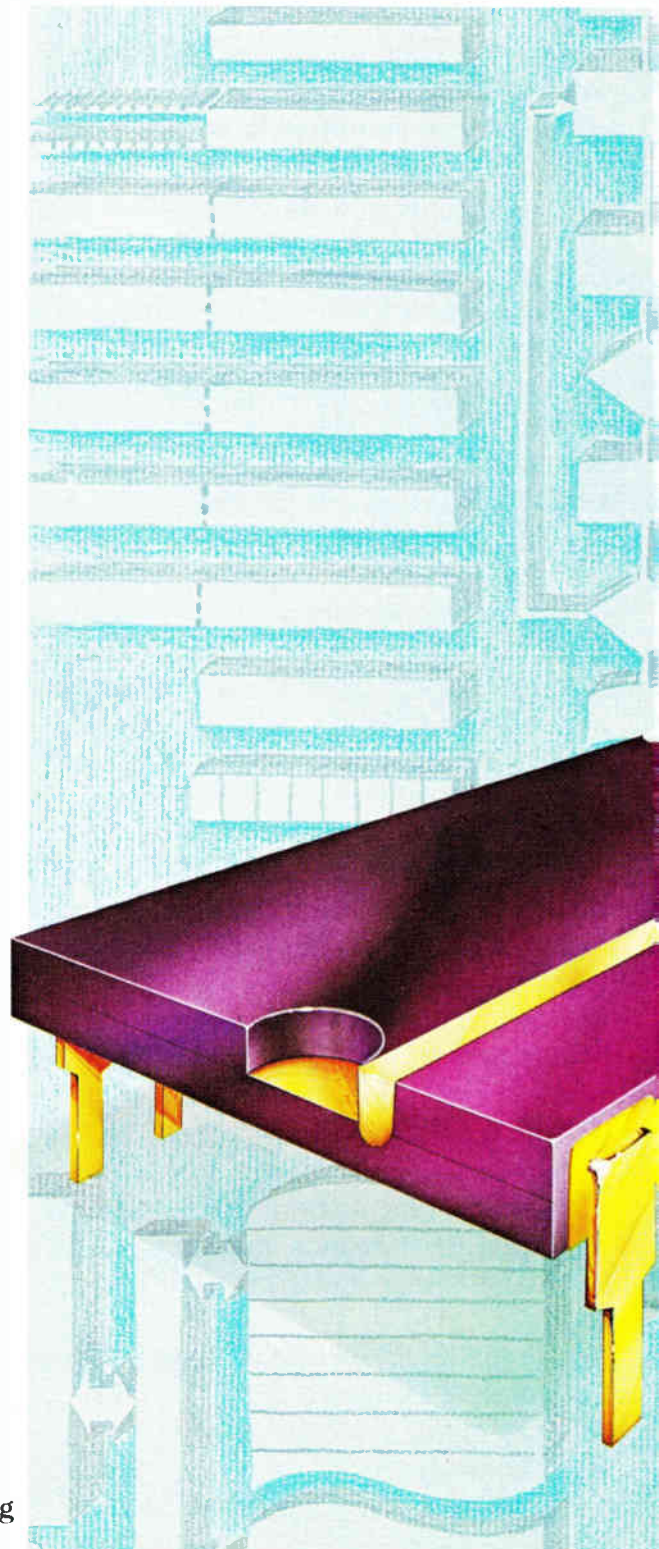
With these features you can develop a library of modular routines, even in ROM, for a variety of systems and at any convenient memory location.

Full M6800 family compatibility.

Full M6800 family compatibility is useful for the MC6809 in a variety of ways. For example, the widely benchmarked MC6800, recognized and respected for its performance, efficiency and ease of use, provides an ideal reference for comparison. Keeping its high performance in mind, see just how sensational the MC6809 is.

The MC6809 is significantly faster than the latest '6800. It takes only about one-third the time to run a comparable program with the MC6809 than it does with the 2-MHz '6800 version, and about one-fifth the time of the original MC6800.

Typically, less than two-thirds the program memory of the MC6800 is required with the MC6809, so byte efficiency is superior. Equivalent MC6809 programs use less than 60% of the instructions needed for the MC6800, cutting programming costs nearly in half.



general-purpose MPU. software costs.



M6800 family compatibility also means +5 V single-supply operation, and permits total usage of all the family I/O, peripheral control, communications and memory components.

Hardware designers can take advantage of the on-chip system clock generator, fast interrupt, interrupt acknowledge, memory ready, DMA request and the signals for multiprocessor synchronization. System designs generally require less external parts with the MC6809 than with other 8-bit or 16-bit microprocessors.

Although the memory address capability is actually greater than needed for many applications, a memory management unit is planned to meet the demand of new systems and future growth.

Hardware and software support.

Family compatibility pays off again, as Motorola's EXORciser® and EXORterm™ development systems support the MC6809 microprocessor. Both development systems are now available equipped with either the MC6809 or the MC6800 CPU module.

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"VAX offered us almost three times the address space of our 370/168."

*Bill Miller, Senior Systems Analyst
Chevron Geophysical Co., Houston, Texas*



Chevron Geophysical is heavily engaged in seismic data processing involving matrix operations on large arrays.

As Senior Analyst Bill Miller states the problem: "Our IBM systems, running on TSS, give 24 bits of true address space — for a maximum program size of 16 megabytes. But only 10 to 12 megabytes of this can be used by the programmer — and our application had grown to the point that TSS was simply cramping us.

"With the VAX-11/780, we know we can have application programs that use a full 32 megabytes as we're configured now — and it could be more if we wanted."

But Chevron didn't buy their VAX without first benchmarking it against the far more expensive 168.

Miller comments: "We developed a number of benchmarks to test specific areas of performance. On the average, the VAX CPU appears

to be about a third as fast as the 168, which is really quite impressive. And it's very possible that for certain applications, we may see a negligible loss of throughput over the 168, thanks to VAX's unique page clustering scheme."

And as far as system performance to date, Miller reports: "The VAX/VMS operating system has been remarkably reliable. The people at Digital have done a phenomenal job."

"VAX's true 32-bit addressing puts its potential capacity so far out, we don't have to worry about it."

*Dr. Edwin Catmull, Director,
Computer Graphics Lab
New York Institute of Technology,
Old Westbury, New York*

The Computer Graphics Lab at New York Institute of Technology is a leading research and production facility for computer animated commercial and educational films.

In Dr. Catmull's words, here's what brought NYIT to the VAX-11/780: "While spending years developing our capabilities with mini-computers, we





**“With a 22,000-point data base,
we really needed VAX’s
huge memory capacity.”**

*Peter Ackermans, Manager of Computer
Systems Engineering
CAE, St. Laurent, Quebec, Canada*

CAE Electronics Ltd., currently has thirteen VAX-11/780 systems under development for both flight simulation and supervisory power control.

Here again, VAX capacity was key. Systems Manager Peter Ackermans told us: “Our SCADA systems for the power market need to handle a 22,000-point data base. VAX’s large memory capacity and the VAX/VMS virtual memory operating system made it a very attractive machine.”

But speed was also important. “In flight simulators,” Ackermans continues, “top FORTRAN performance is essential, and on that score, VAX measures up well. Our FORTRAN programmers have also been impressed with the machine’s debug facility and file handling capabilities.”

Digital’s VAX-11/780, with its true 32-bit address space, has set a new standard for program capacity. This means that you can run large programs easily on VAX, with a potential for growth that’s unmatched in the industry.

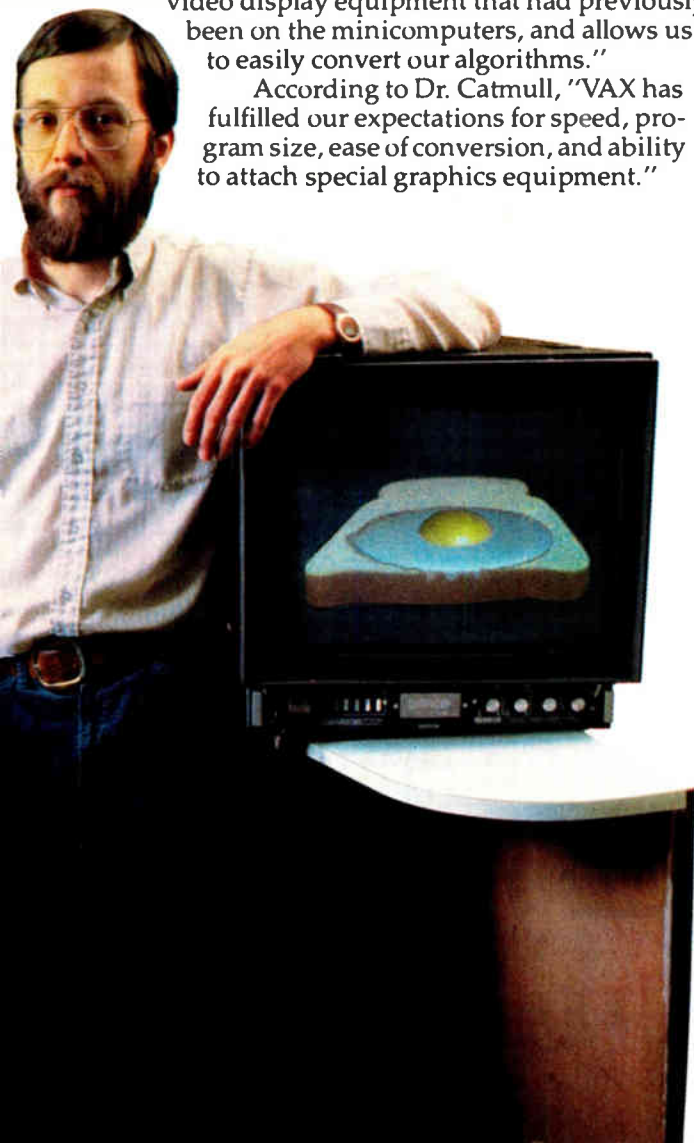
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continually ran into the problem of small address space. Our work demands the large address space we can get with a 32-bit machine. We were dealing with extremely large, randomly accessed data bases, and memory mapping is not the answer.”

Dr. Catmull continues, “The VAX UNIBUS lets us easily hook up a wide range of special video display equipment that had previously been on the minicomputers, and allows us to easily convert our algorithms.”

According to Dr. Catmull, “VAX has fulfilled our expectations for speed, program size, ease of conversion, and ability to attach special graphics equipment.”



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Field-programmable arrays: powerful alternatives to random logic

Bridging design gap, TTL-compatible logic family
is described in Part 1 of a two-part article

by Napoleone Cavlan and Stephen J. Durham, *Signetics Corp., Sunnyvale, Calif.*

□ With the steady growth of integrated circuit technologies, hardly a day goes by without the news that yet another chip has made scores of discrete TTL packages obsolete. Yet, though large-scale integration is packing entire system architectures onto a few chips, it is still impossible to complete a design without some discrete logic to hold the framework together.

The increase of LSI has thus created the need for efficient ways to bridge the gaps between large functional islands. Because of complexity, performance, or uniqueness, these bridges have evolved into nontrivial random-logic configurations that still rely on clusters of small- and medium-scale integrated circuits, whose fixed functions never quite fit the problem. Now Signetics

Corp. has attempted to meet the need with a field-programmable logic family.

The family spans three ranges of complexity: at the low end are the field-programmable gate arrays (FPGAs); covering the middle range are the more complex-logic arrays (FPLAs); and finally there are the logic sequencers (FPLSS). These last, most complex elements have built-in registers and enable the designer to proceed from state diagram directly to hardware. The family, summed up in the table on p. 110, is compatible with TTL and operates from a +5-volt supply.

The devices provide a powerful and compact alternative to random logic, replacing discrete gates, wires, and connectors, with significant savings in board space,

FIELD-PROGRAMMABLE LOGIC FAMILY									
Device	Organization	Device	Inputs	Outputs ⁽¹⁾	Chip enable (\overline{CE})	I_{CC} (max)	Delay (max)	Availability	Package ⁽²⁾
FPGA	• AND/NAND	82S102 82S103	16	9 OC 9 TS	yes	170 mA	35 ns	now	N
FPLA	• AND-OR/ NDR	82S100 82S101		8 TS 8 OC	no		50 ns	now	N, F
	• AND-OR • Self-enable output	82S106 82S107		8 OC 8 TS			70 ns	4Q79	N
FPLS	• AND-OR	82S104		8 OC	yes ⁽³⁾		90 ns	4Q79	N, F
	• Complement array	82S105							
	• 6-bit state register • 8-bit output register								

⁽¹⁾ OC = open collector TS = three-state
⁽²⁾ N = plastic F = Cerdip
⁽³⁾ \overline{CE} input may be optionally programmed as preset.

power, and cost. Moreover, since all devices can be programmed and modified in the field (as programmable read-only memories can) using readily available programming equipment, the logic can be changed to meet new customer requirements or specifications, or to recover quickly from design errors—after delivery to the field—without expensive printed-circuit-board retooling.

Programming options

Depending on their complexity, members of the programmable logic family have internal AND gates, OR gates, S-R flip-flops, true or complement buffers, and exclusive-OR (EXOR) gates. Those elements can be combined to perform single-level, double-level, and sequential logic functions—all by blowing fuse links.

There are other fuse options in output structures for the entire logic family, too, since either active-high or active-low functions can be generated without additional hardware or signal delay. Finally, the family is well suited to bus-organized environments such as microprocessor systems, since all its members offer, in addition to open-collector outputs, three-state outputs whose signals are in the high-impedance state until activated by a chip-enable input.

All the logic elements perform standard logic functions that can be represented by augmenting conventional logic symbols with a few new definitions so that they can represent multiple-input gates (see "How the FPLF defines logic," p. 111).

The gate arrays

The simplest member in the family is the field-programmable gate array, which performs single-level logic functions. The equivalent logic diagram for the FPGA is shown in Fig. 1. The two gate arrays currently available are open-collector (82S102) and three-state output (82S103) versions of the same array, which comprise nine NAND gates fuse-selectively connected to 16 common inputs by true/complement buffers.

Fuses in the FPGAs allow individual outputs to be complemented to AND, so that by proper manipulation of the input polarities, and by using De Morgan's theorem, AND, OR, NAND, and NOR logic functions can be easily implemented. The parts thus serve as universal logic elements that can be tailored to applications requiring random logic, as in fault monitors, code detectors, and address decoders for microcomputer systems with memory-mapped I/O.

The logic arrays

Devices performing two-level combinational logic functions are grouped into the field-programmable logic array (FPLA) category. These elements are a step up in complexity from gate arrays, capable of generating AND-OR, AND-NOR, and their De Morgan equivalents. There are at present two array types in the FPLA family, each with either open-collector or three-state outputs.

The equivalent logic diagram of the first array type, the open-collector output 82S101 (or three-state output 82S100), is shown in Fig. 2. The first level of logic in the device is made up of 48 AND gates fuse-connectable to any of 16 common inputs by true/complement buffers. The second logic level consists of eight OR gates—one per device output—each capable of being selectively coupled to any of the 48 gates. Finally, fusing options are included for generating true or complementary outputs.

The second logic array type, the 82S106/107, has nearly the same organization as the first. The exception is that an additional OR gate with fixed inputs has been added to generate an internal enable command for the output structure. That self-enable is generated whenever any of the AND gates become logically true, which occurs when the external input code matches the internal AND-gate program. In the absence of such a match, all device outputs are unconditionally disabled. The self-enable signal is available externally—the chip-enable input (\overline{CE}) pin on the 82S100/101 becomes an open-collector output called \overline{FLAG} . Because of this feature, the 82S106/107 can be viewed as a content-addressable programmable read-only memory, ideally suited to modifying data in large ROMs, as will be shown in the second part of this article.

Shared gates

Both array types benefit from the second level of logic. The advantage here is that the AND gates can be shared—OR gates can couple with up to 48 AND gates. Also, a key advantage of this arrangement over single-level logic is that it allows editing—disconnecting invalid AND terms from the OR array and replacing them with spare AND gates (Fig. 3).

Open-collector versions of both gate-array and logic-array devices can form wired-AND outputs in order to expand the number of AND gates available on a single chip. This solves the problem that is posed by applications exceeding the resources of a single device. The only restriction is that the expanded outputs have to be programmed to be active-low.

By far the most powerful members of the family are the field-programmable logic sequencers (FPLS), which add on-chip registers to arrays of AND and OR gates. The

How the FPLF defines logic

For the most part, schematic representation of logic in the field-programmable logic family follows conventional notation—the devices include AND, OR, and exclusive-OR (EXOR) gates, as well as set-reset (S-R) flip-flops and true or complement buffers. To simplify the representation of fuse-link programmability, however, the FPLF schematics use a matrix arrangement with cross-point coupling to represent intact fuse links.

For example, (a) in the figure shows a typical input and AND gate of a gate array. The square "solder dot" represents a fixed internal connection. Both the line from input A and the line from the output of the inverter intersect the vertical input line of the AND gate; in actuality, fuse links make both connections. An intact fuse link is represented by a round solder dot. Blowing either of the fuse links will determine whether the input to the AND gate is A, or its complement, \bar{A} . (Leaving both fuses intact holds the output of the AND low, whereas blowing both fuses results in a "don't care" situation, an output that is independent of either input.)

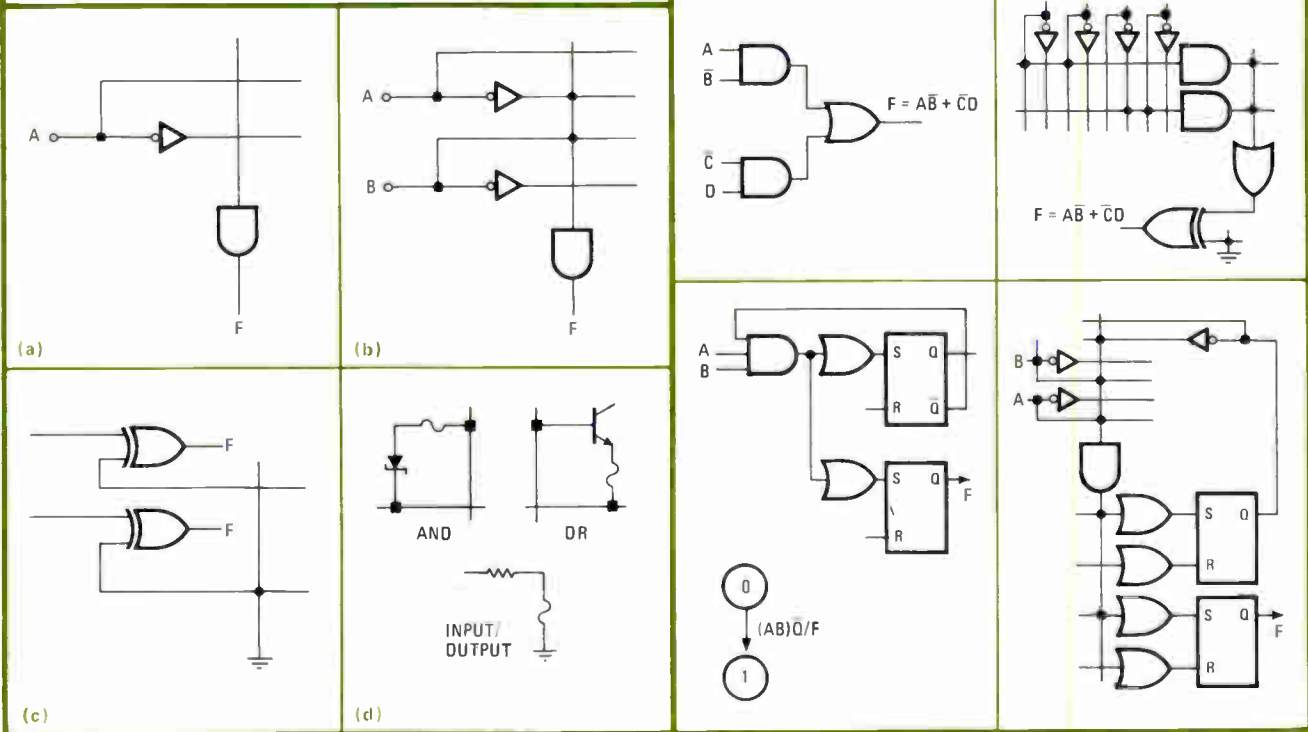
Extending the matrix and cross-point coupling approach a step further, (b) shows the configuration of a two-input AND gate. Since the input to the AND gate crosses the four lines of inputs A and B as well as their complements, the gate serves as a four-input AND while appearing to be a single-input gate. Since the members of the field-programmable logic family have 16 inputs intersecting each AND gate, the gates are actually 32-input devices; the number of inputs used is determined finally by the number of fuses left intact. Thus, in (b), solder dots (or

intact fuse links) create the logical equation $F = \bar{A}\bar{B}$.

The exclusive-OR gates on all outputs of the logic-family devices allow programming for either active-high or active-low output signals. As shown in (c), a fuse link grounding one of the two inputs of an EXOR gate results in an active-high output; blowing the fuse results in an output that is active-low.

The details of the fusing mechanisms are shown in (d). AND gates have a fuse in series with a Schottky diode, while OR gate fusing uses an npn transistor. The fuses for the true/complement input buffers and active-high/active-low outputs are in series with resistors.

The analogy between fixed and programmed logic is best shown by the examples in the table. The first example is typical of the single-level logic to which the gate array is applicable. The two-level logic of the second example is satisfied by the logic arrays. Finally, the registered state machine that executes the state transition of the third example is a candidate for the field-programmable logic sequencers.

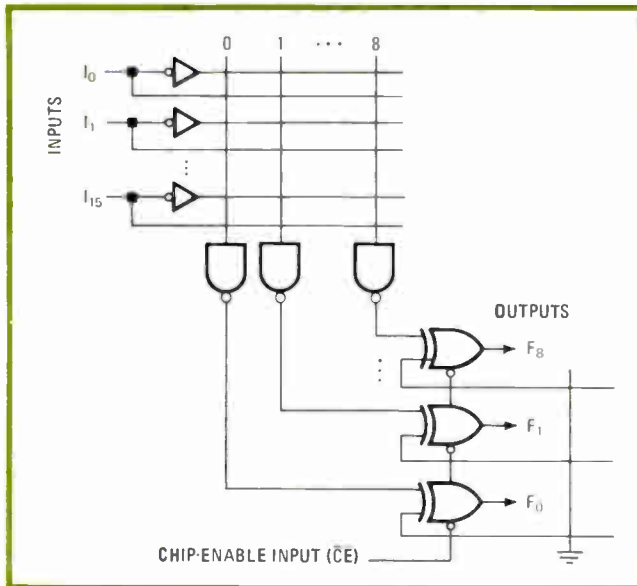


sequencers are actually self-contained state machines, since they can be programmed to perform any synchronously clocked logic sequence.

State machines, whose general structure is shown in Fig. 4a, usually take two forms: Moore machines, in

which the output is a function of the present state only; and Mealy machines, whose output is a function of both the present state and the present input.

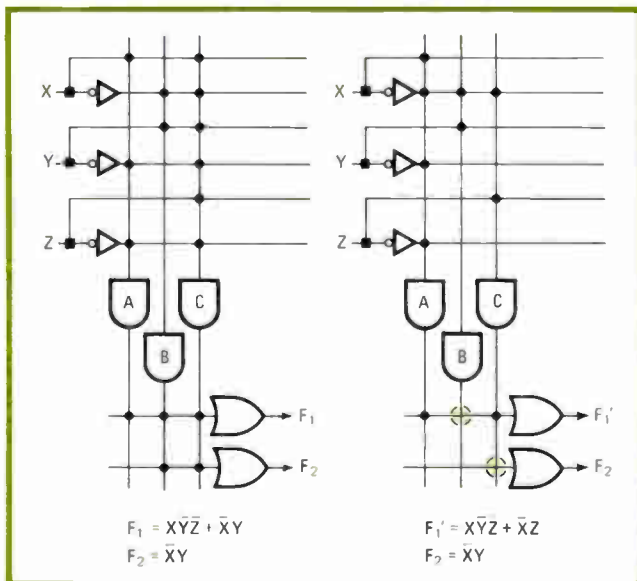
Figure 4b shows the basic architecture of the open-collector output 82S104 (or three-state output 82S105),



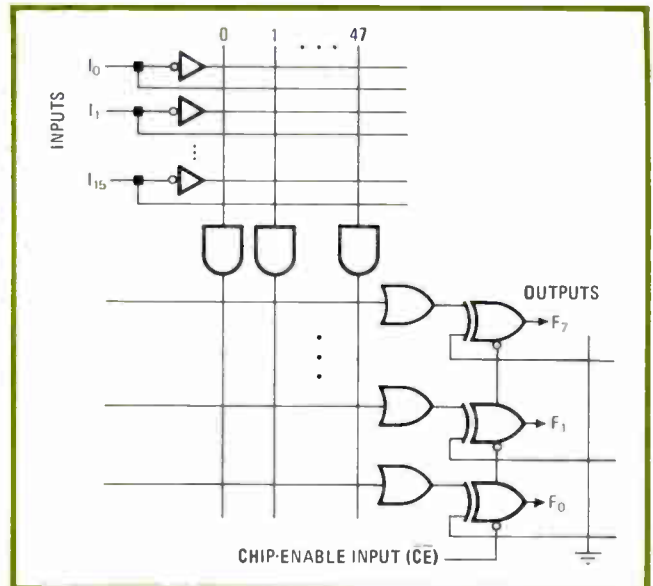
1. Gate array. The simplest device in Signetics' field-programmable logic is the gate array, capable of single-level logic. Any of 16 inputs can connect to nine NAND gates by true/complement buffers. Since complement outputs can be complemented to AND, manipulating De Morgan's theorem makes the device a universal logic element.

the first members of the FPLS family. With the FPLS, a user may program any logic sequence that can be expressed as a series of jumps between stable states triggered by a valid input condition I at clock time t. The number of states in the sequence depends on the length and complexity of the desired algorithm.

A typical state diagram is shown in Fig. 5. The state from which a jump originates is called the present state P, and that at which it terminates is the next state N. A jump always causes a change in state, but may or may not cause a change in the machine's output F.



3. Editing. The logic array's programmable OR gates allow sharing of AND gates, as with gate B at left. The OR array also allows easy editing of logic statements when design changes are made; note how spare gate C at right was used to modify output F_1 to F_1' .



2. Double deep. The field-programmable logic array carries out two-level combinational logic. The 16 inputs couple to 48 AND gates, which in turn connect to any of nine OR gates. Either true or complement outputs are provided.

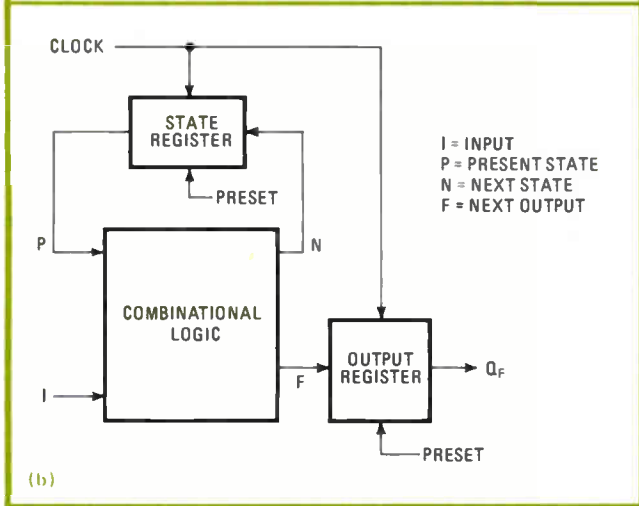
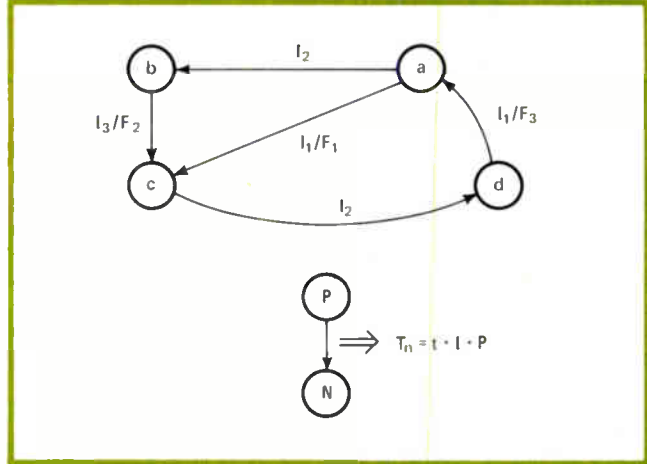
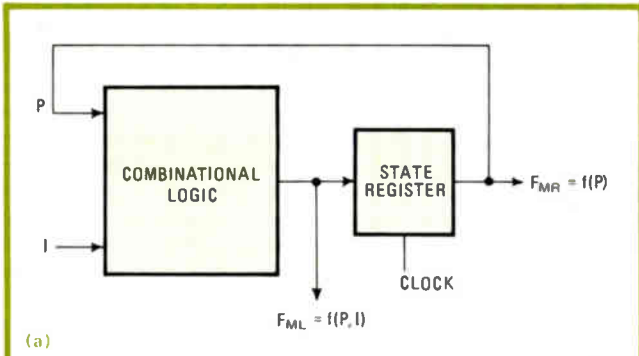
All states are arbitrarily assigned and stored in the state register, where the clock and next-state information from the combinational logic are the inputs. State jumps can occur only when transition terms are true. A transition term is, by definition, the logical AND function of the clock, present state, and valid inputs; hence, $T_n = t \cdot I \cdot P$. However, since the clock is actually applied to the state register, it may be removed from the equation. When T_n is true, a control signal is generated that, at clock time t, forces the contents of the state register from P to N and, if necessary, changes the contents of the output register.

FPLS organization

The architecture of the 82S104/105 is a natural extension of the static logic structure of the FPLA. It accepts 16 input variables and provides eight output functions. It has a 6-bit state register and an 8-bit output register; all the internal registers are automatically preset to logic 1 when power is applied. The FPLS provides for 48 transition terms, which can be selected to be either true or complementary.

A look at the equivalent logic diagram of the FPLS (Fig. 6) shows its extension of the static FPLA. The AND and OR gate arrays of the latter have been expanded to control the set and reset (S and R) inputs of six flip-flops (the state register) and to monitor the register's contents over an internal feedback path. Also, an independent 8-bit output register has been added to store output commands generated during state transitions and to hold the output constant during state sequences involving no output changes.

The AND array comprises 48 positive AND gates, each with 44 input connections from a set of true/complement buffers. The AND gates are used to form logic products of 16 external inputs (I_0 to I_{15}) with six present-state (P) inputs fed back from the state register. The gates are



5. State diagram. Example of a state diagram (a) with four states—A, B, C, and D. I_1 – I_3 are jump conditions, which trigger output changes F_1 – F_3 . A state change (b) gives rise to transition term T_n , which is logical AND of clock t , input I , and present state P .

4. State machine. A state machine (a) takes either a Mealy or Moore form. The architecture of the field-programmable logic sequencer (b) is that of a self-contained Mealy machine, where the output is a function of both the present state and the present input.

therefore called transition terms because, like the transition terms in state diagrams, they issue next-state commands.

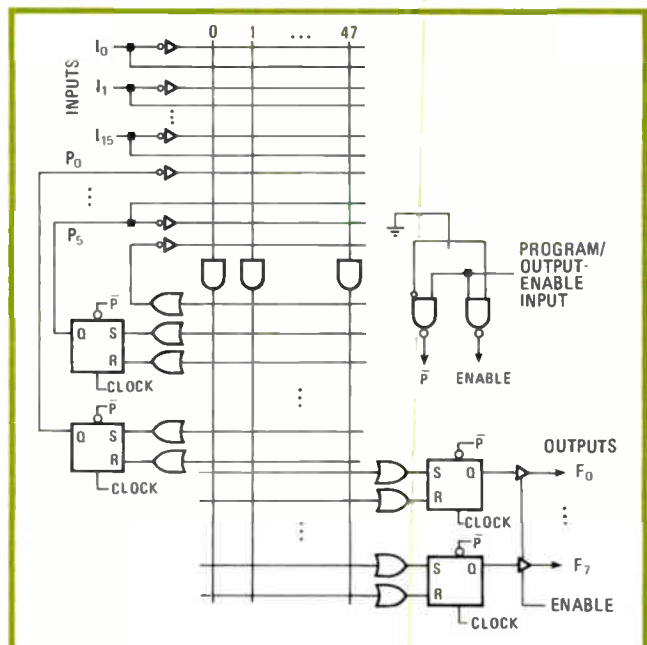
The OR array contains 28 positive OR gates, each with 48 input connections to all 48 AND gates. The outputs of the ORs drive the set and reset inputs of the 14 S-R flip-flops that are state and output registers.

The FPLS is made still more flexible by a complement array comprising a single 48-input OR gate that drives an inverter, which then feeds back into the AND array. The complement array forms a bridge between the AND and OR arrays for generating NAND functions of input-jump conditions; the user programs it in such a way as to suit each transition term.

De Morgan's theorem

De Morgan's theorem to reduce logic terms can be easily implemented with the complementary array so that the most use is made of the AND gates. For example, if the transition term is $T = (Q)(\bar{X} + \bar{Y} + \bar{Z})$, where Q is the output of the state register and \bar{X} , \bar{Y} , and \bar{Z} are inputs, three AND gates in the FPLS are required. However, De Morgan's theorem changes the transition term to $T = (Q) \bar{X}\bar{Y}\bar{Z}$, which requires only two AND gates.

The complementary array is also an efficient means of aborting a clocked sequence in the absence of valid jump conditions. As Fig. 7 shows, considerable minimization

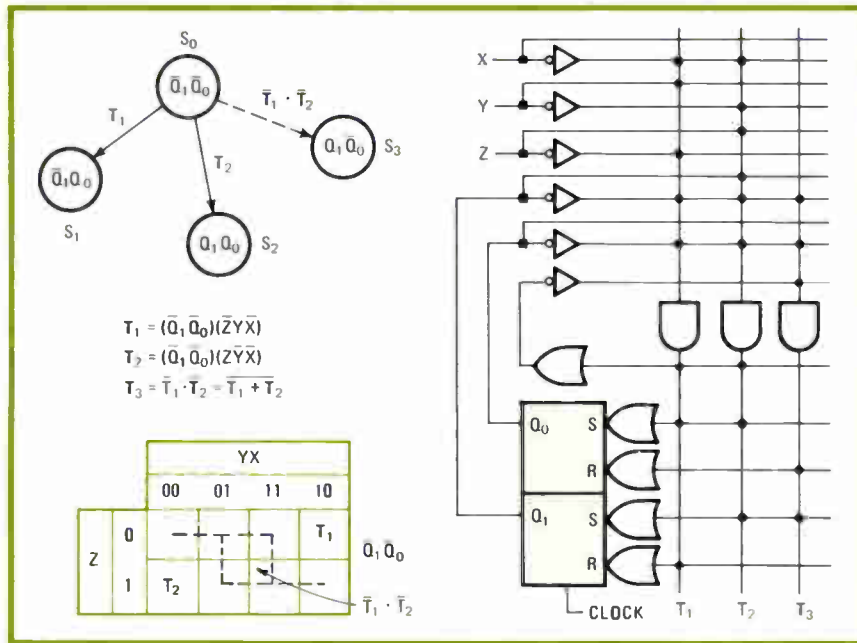


6. Sequencer. The field-programmable logic sequencer has 16 outputs, 48 AND gates, and 28 OR gates, plus 14 flip-flops that serve as state and output registers. Either an asynchronous preset input or an output-enable input is available as a programming option.

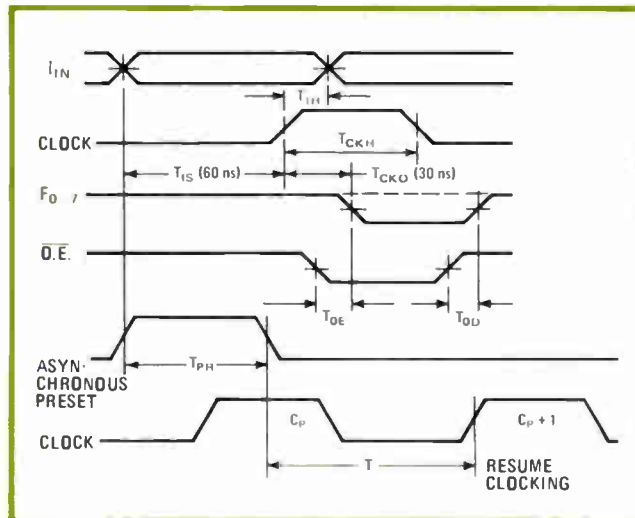
of AND gates is possible when the detection of valid jumps involves many complements of jump functions, especially as the number of variables increases.

All clocked S-R flip-flops that make up the state and output registers offer the option of asynchronous pre-setting to all 1s. The 64-state total that can be represented by the state register is adequate in most cases to chart algorithms involving fewer than 48 nonredundant transitions. The register accepts next-state commands (N) from the OR array and supplies present-state information (P) to the AND array.

The output register is similar to the state register, except it has eight states for servicing eight output functions. It accepts the next-output commands F_0 – F_7



7. Complementary. Use of AND gates in the FPLS is greatly reduced by the complement array, a single 48-input OR gate driving an inverter that feeds back into the AND array. In this example, the default jump from state S_0 to S_3 is reduced from three AND gates to a single gate T_3 .



8. Timing. Minimum clock duration for the FPLS is 20 nanoseconds. Minimum width of preset input, which overrides clock, is 40 ns. Normal clocking resumes with the first full clock pulse following a negative clock transition after the trailing edge of the present signal.

from the OR array and then reflects its contents to the device outputs through the buffered Q outputs of each of the flip-flops. Also, as an added feature to enhance fault isolation, driving input I_0 to +10 volts will route the contents of the state register (P_0 - P_5) directly to outputs F_0 - F_5 without any alteration of the contents of the output register. However, the feature is not recommended for use in a normal mode of operation (as in a Moore machine). This is because it increases the device's maximum current by 5 to 10 milliamperes and thereby lowers the maximum ambient temperature rating of the package by approximately 5°C.

As a final programming option in the 82S104/105, a pin can function as either an active-high asynchronous preset (pr) or an active-low output enable ($\bar{O}E$). The output-enable function forces all outputs to logic 1 (or to

high impedance in the 82S105) and is normally used when the device is sharing a bus. It does not inhibit clocking of the internal registers. The asynchronous preset option, on the other hand, is useful when the logic sequence requires an immediate state-independent return to initial conditions. The state register and output register can also be synchronously preset independently of one another by dedicating that function to one of the input variables in conjunction with a single transition term and a clock pulse.

Timing constraints

The maximum clock rate of the 82S104/105 can be inferred from its timing diagram (Fig. 8), which shows worst-case delays and setup requirements during a typical I/O cycle. Using stable external inputs as a reference, the device can be clocked after a minimum setup time of 60 nanoseconds. The next output (as well as the next internal state) will be valid 30 ns after the positive edge of the clock, giving a total I/O delay of 90 ns. Since both output enable and disable delays are also 30 ns, when the $\bar{O}E$ pin is used its signal's edge should occur prior to or coincidentally with the clock in order to avoid increasing I/O delays.

The asynchronous preset option includes a clock lockout feature that eliminates the potential hazard of spurious clocking. But, as the timing diagram shows, when using the lockout feature it is possible to miss one clock pulse, which may be prohibitive in some applications.

Applications

The second part of this article, to appear in the next issue of *Electronics*, will provide examples of applications for the gate- and logic-array devices. It will also describe in detail the development of a full-blown cartridge-tape drive controller built with a single logic-sequencer chip. The design example proceeds from flow chart to state-sequence diagram to hardware. □

Surface-acoustic-wave filters prove versatile in vhf applications

Today's photolithography mass-produces SAW devices that often outdo crystal and LC filters

by David Penimuri and D. P. Havens, *Rockwell International Corp., Collins Divisions, Newport Beach, Calif.*

□ Surface-acoustic-wave devices deserve their growing popularity. Upwards of four dozen distinct types are to be found today in systems ranging from satellite and spread-spectrum communications through radar on down to the consumer television set.

What has brought them out of the laboratory and onto the high-volume production line are the advances in integrated-circuit technology and photolithography. Micrometer-wide lines allow the exact physical reproduction of all the advantages long known to be inherent in surface acoustic waves.

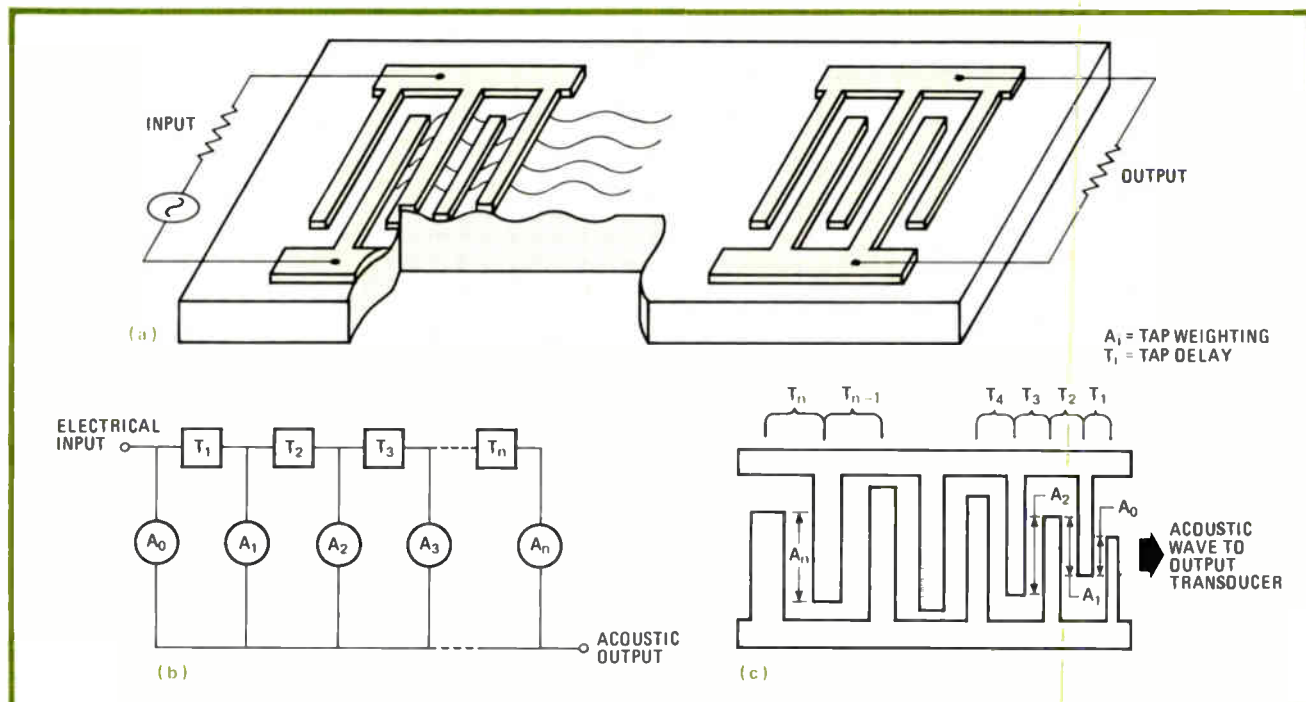
For instance, when propagating in crystalline solids—the usual case—these waves have low propagation losses, stable properties, and velocities so low that any component whose size is related to wavelength is inevitably compact. It is easy to modify their path of propagation and make connections to it. Also, the waves are nondispersive, so their key properties are insensitive to frequency, making a great variety of applications possible.

SAW devices by now include bandpass filters for radio-frequency receivers, TV intermediate-frequency amplifiers, frequency synthesizers, and channelized receivers and equalizers for digital data systems. Others serve as dispersive delay lines in linear frequency-modulated chirp radar, microscan receivers, and chirp-Z transformers, as tapped delay lines in biphase-coded waveform generators and correlators, and as convolvers with memory for programmable matched filters.

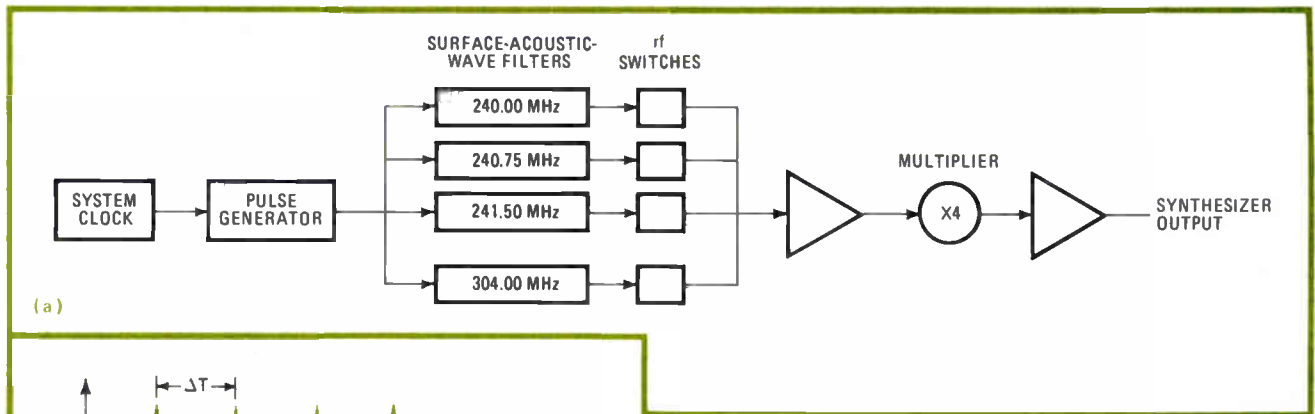
The pros and cons

Such proven versatility warrants the attention of every serious system designer. A discussion of several key applications will demonstrate what can and cannot be expected of SAW technology in practice.

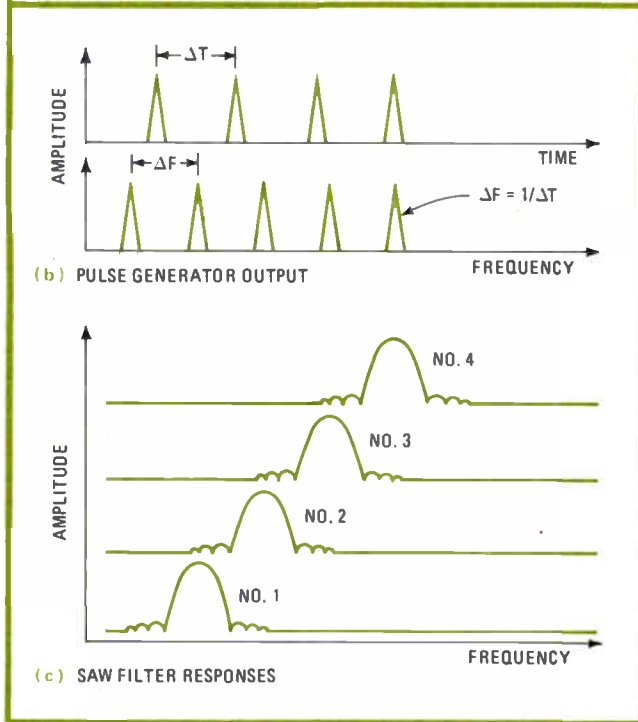
Most applications occur in the very high-frequency range—a characteristic of SAW filters that is due to the nature of the photolithographic techniques and piezoelectric materials used to fabricate them. Crystal and



1. Surface-acoustic-wave device. In the typical SAW device (a), the input signal is repeatedly delayed, weighted, and added to itself in the transducer (b). By varying the amount of delay and weighting on each tap (c), the phase and amplitude can be independently controlled.



(a)



(b) PULSE GENERATOR OUTPUT

(c) SAW FILTER RESPONSES

2. Fast hopper. A fast moving-frequency synthesizer can be built using SAW technology and digital logic (a). The pulse generator outputs (b) are frequency-sorted by means of a SAW filter bank so as to synthesize the desired output frequencies (c).

inductance-capacitance (LC) filters are well known and overlap the bandwidth and frequency range of SAW filters. But within the frequency region of 30 to 500 MHz and bandwidth range of 0.1% to 30%, only SAW filters simultaneously offer reproducibility, reliability, low cost, selectivity, and small size to the system designer.

SAW dice are made with the same techniques as other solid-state microelectronic devices, so that low cost and high repeatability are readily achieved. Once a SAW device has been designed and a mask produced, filters from one production lot to the next will have identical characteristics. LC and discrete crystal filters, on the other hand, require complex tuning procedures since inaccuracies in the tuning of the resonant frequencies and the coupling between sections cause variations between filters.

If phase linearity is required, the difference between SAW and the other technologies becomes even more pronounced. SAW filters are for the most part transversal devices. Therefore their phase and amplitude characteristics are independent, and they achieve phase linearity

simply by using symmetrical transducers. On the other hand, crystal and LC filters are longitudinal devices so they need compensating sections to achieve linear phase. These additional sections make them harder to tune. Moreover, they add to device size and cost and by increasing device complexity decrease reliability. If sharp amplitude response is required as well as phase compensation, LC and discrete crystal filters need still more electrical elements, further enlarging the package and the risk of device degradation or failure.

In contrast, a SAW device usually consists of a die and only one or two passive components to match or tune each transducer. The complexity of the specification seldom increases the number of tuning elements significantly. So, in SAW filters, reliability is not a direct function of the design difficulty.

All this is not to say that SAW filters are superior in every respect. As will become apparent, there are areas in which the competing technologies hold the advantage. These include insertion loss, stopband suppression, and initial design cost.

Lots of loss

The simplest and most common design for a SAW transducer uses one bidirectional input and one bidirectional output transducer. Because the transducers are bidirectional, 3 decibels of energy are inherently lost in each. More energy is lost—typically 20 dB—in the impedance mismatch needed to suppress reflections between the transducers. And while there are transducers with only 1 dB of insertion loss, they require three-phase matching networks and multilayered masks.

In theory, designs can be found that predict sidelobe levels (stop-band suppression) in excess of 80 dB for SAW filters. In practice, however, second-order effects tend to reduce this level considerably. For example, when sidelobe levels are required to be much below 40 dB, special techniques must be used, not all of which are applicable to all bandwidth ranges. Often, to achieve sidelobes of 50 dB or better, some other performance parameter must be sacrificed. This might be insertion loss, filter band-pass, shape factor, or cost.

The initial design cost for SAW filters usually runs higher than for other filtering techniques since photolithographic masks must be made. These can cost several thousands of dollars each, and a difficult design may need more than one mask to achieve the desired results.

So if only small quantities of a device are required and the desired frequency response is not difficult to achieve, it may be cheaper to use LC or crystal techniques. But for a more complex filter, depending on which parameters are critical, the initial design cost of LC, crystal, and SAW filters may be competitive. Which technology best fits the application depends on the application itself as well as volume and cost constraints.

Two SAW filters

Though a few surface-acoustic-wave filters are resonator in type, the vast majority are transversal. This mode of operation is readily explained.

In its simplest form, a transversal SAW filter has two transducers attached to opposite edges of a polished piezoelectric substrate. When an electrical signal is applied to the input transducer, it physically distorts the piezoelectric substrate surface, creating a series of traveling waves (Fig. 1a) much as a tossed pebble creates ripples in the surface of a smooth pond. As each wave reaches the output transducer, its mechanical energy is transformed back into an electrical signal.

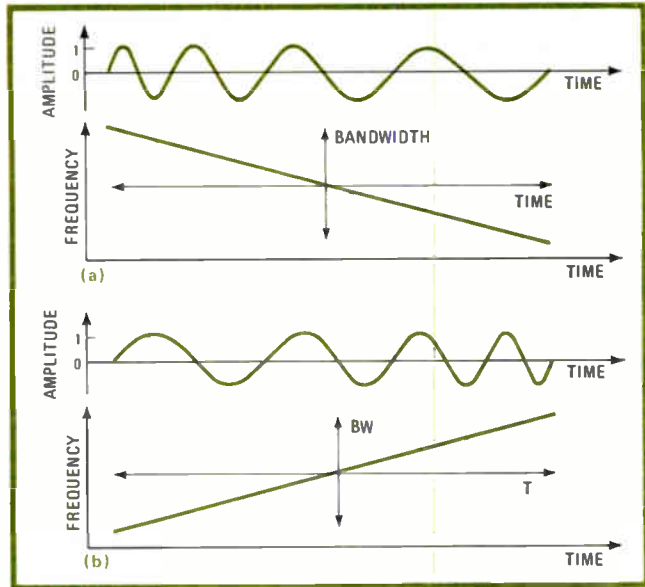
The signal-processing or -filtering characteristics of the device are determined by how the transducer converts the electrical signals into mechanical signals. A SAW transducer is made by depositing two sets of interdigitated electrodes of opposite polarities on the substrate. Each pair of neighboring and differently polarized electrodes acts as the source of a mechanical signal. Because this surface wave travels from one electrode pair to the next at a finite velocity, the signal is repetitively delayed and added to itself (Fig. 1b). This constructive or destructive signal adding determines the frequency and phase characteristics of the filter.

The amplitude of the mechanical signal created by one electrode pair relative to that of another can be controlled by varying the length of overlap of the electrodes—a technique of “weighting” a transducer known as apodization. When a surface-wave transducer is excited by an electrical signal, the amplitude of the signal along the transducer is closely related to the amount of the electrode overlap in that region. If the signal is an impulse, the impulse response of the filter is equal to the “spatial image” of the transducer.

What this means is that the electrical response to an impulse input as seen on an oscilloscope will have the same shape as the overlap function of the transducer. Since the relationship between impulse response and frequency is well known from such other fields as digital filter and antenna design, the same techniques can be used to find the proper impulse responses for the frequency and phase characteristics desired for a SAW filter. Once an impulse response is found, the SAW transducer is designed with the electrode overlap proportional to the impulse amplitude.

It is possible to optimize surface-wave filters for specific applications by trading off one device parameter for another. For example, insertion loss, cost, stopband levels and other design objectives can be readily interchanged. So it is important to decide which parameters are the most important.

Most often, the parameter that is easiest to sacrifice is



3. Chirp chirp. In a typical waveform transmitted by a chirp radar that is being operated at nearly maximum output power, the rf pulse has an instantaneous frequency that is linear with time (a). The impulse response of the receiver matched filter has a frequency-time slope that is the negative of the transmitted waveform (b).

cost. Given enough money, the most difficult specifications can be met. Temperature stability can be achieved with ovens, selectivity can be increased by cascading devices, and high operating frequencies can be achieved by using direct-writing electron-beam lithography systems. But it will seldom be possible also to sacrifice the space and power necessary for a temperature-regulating oven or the cascading of filters. Also, electron-beam systems are not yet a reality for production quantities of SAW devices. To minimize design and production cost, then, the designer must know the practical limits for SAW devices and the possible tradeoffs.

What's important

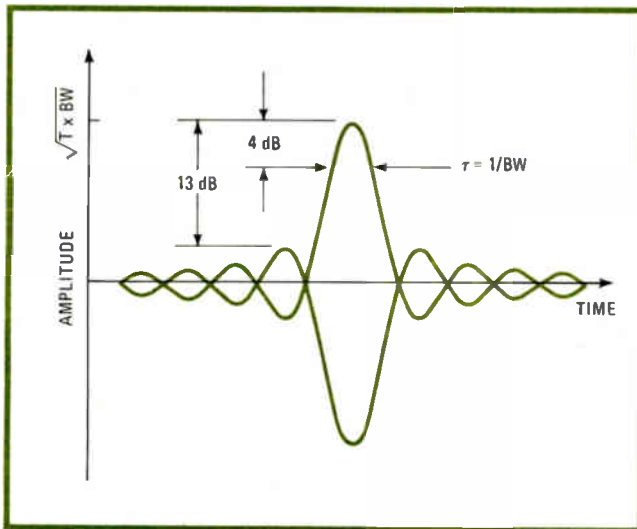
The most important filter parameters are usually center frequency and bandwidth. SAW devices have been made with center frequencies down to 2 MHz and above 2 gigahertz. But at the lower frequencies, die sizes become large, and at higher frequencies, the yields from photolithographic processes become unacceptably small. In general, frequency ranges for standard production devices go from about 20 MHz to 500 MHz.

Bandwidth limitations are determined in part by the device substrate. The two commonest substrate materials are lithium niobate (LiNbO_3) and ST-cut quartz.

Lithium niobate can achieve a large coupling coefficient but it has poor temperature stability: typical frequency shifts are -90 parts per million per $^\circ\text{C}$. So it is used mostly for wider-fractional-bandwidth devices. A reasonable range of bandwidths is from 3% to 50% of center frequency.

Quartz, on the other hand, has a zero temperature coefficient at room temperature but a low coupling coefficient. Minimum-loss filters can be fabricated for bandwidths below 4%.

Wider-bandwidth devices can be made on quartz, but



4. Compression. When a linear frequency-modulated pulse is compressed by SAW devices, the amplitude of the waveform has a well-defined $(\sin X)/X$ shape. It is easy to bring sophisticated techniques to bear to improve the critical parameters of this waveform.

there is a penalty of around 12 dB in insertion loss for each doubling of bandwidth over 4%. The constraining factor on the lower bandwidth limit is die length. A filter with a 100-MHz center frequency, 40-dB sidelobes, a 2:1 (40-to-3-dB) shape factor and a 0.1% bandwidth would require a die 4 inches long. And decreasing the shape factor to 1.5 to 1 doubles the length.

Quartz dice have been made up to 10 inches long. However, the quartz wafers used in volume production come in 2-by-2- to 3-by-3-inch sizes. So if the 3-in. wafer sets the maximum permitted length, the minimum bandwidth for low-cost filters falls between 0.1% to 0.4%. The exact value depends on shape factors, sidelobe level, and center frequency.

Dealing with nonlinearities

While transversal filters were originally created for applications where filter phase and amplitude need to be specified separately, it is impossible to arbitrarily specify these parameters for a SAW filter since nonlinearities are always present in them.

For example, the primary cause of phase nonlinearities is reflections between transducers, known as "triple transit." The reflections are due partly to mechanical impedance discontinuities on the crystal caused by the mass of the electrodes and partly to electrical loading effects of the terminating sections.

The reflections due to mechanical discontinuities can be controlled by splitting the electrodes. This causes the signal reflected from half of an electrode to add destructively to the signal reflected from the other half. But reflections caused by electrical discontinuities are not as easily handled. They must be controlled by intentional mismatching of the transducer electrical connections, despite the fact that the greater the mismatch, the higher the filter's insertion loss. So design tradeoffs are necessary. One result is a bandpass filter with a 2:1 shape factor and a bandwidth of 1.5 MHz, exhibiting 0.4 microsecond of delay ripple at 10 dB of insertion loss.

SAW devices are often used in military communication systems. In particular, they are found in the frequency synthesizers used in command, control, and communication (C³) systems that coordinate various weapon systems. For example, the Joint Tactical Information Distribution System (JTIDS), a digital communications system in its early stages of development, will be used by the U. S. Air Force, Navy, and Marine Corps to integrate each of their rather different C³ systems. The system is designed to provide a high-capacity, jam-resistant information network that will link sensors, weapons, observers, and controllers.

One JTIDS synthesizer

The basic data-encoding techniques proposed for the JTIDS include spread-spectrum concepts, which in some applications require fast frequency hopping. When such hopping must be done over a range of 960 to 1,215 MHz in steps of as little as 1 MHz at rates to 1 to 10 MHz, a lightweight, compact, low-power, fast-frequency-hopping synthesizer is a must. SAW bandpass filters and integrated semiconductor switching circuit technology can combine to satisfy all these requirements.

In one approach, the required fast-frequency-hopping synthesis is done in three stages (Fig. 2). First, a number of uniformly spaced frequencies of high spectral purity and stability is generated (for example, by using a periodic impulse driver). Then individual frequencies are selected with high isolation—spurious signals and adjacent frequencies must be suppressed by at least 60 to 65 dB. This selection may have to be made at a rate as fast as 10 MHz. Finally, the selected frequencies must be mixed or multiplied up to the required transmitter frequency band.

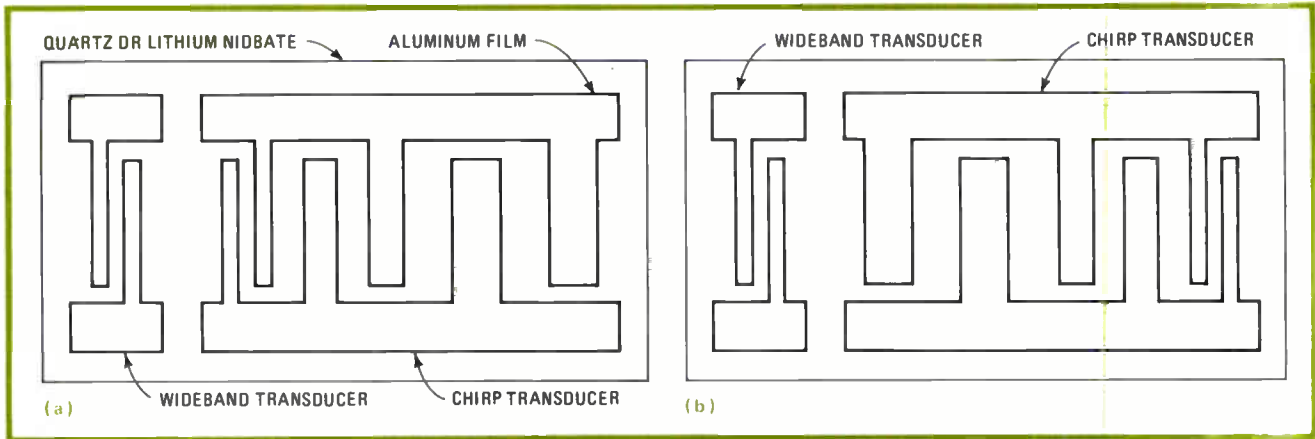
This design approach requires a bank of about 50 SAW bandpass filters with center frequencies of 240 MHz to 304 MHz spaced 0.75 MHz apart. It therefore has several disadvantages. For one, the cost of designing so many different SAW filters and fabricating numerous photo-masks is high. For another, the narrow bandwidth and high sidelobe suppression of these filters implies that they must be several inches long, which makes packaging a problem.

However, the advantage of the approach is that the accuracy and stability of the output frequencies are directly determined only by the accuracy of the system clock and pulse generator. Moreover, the high stability that is required of the pulse generator used in JTIDS synthesizers can be readily achieved by using a phase-locked-loop design.

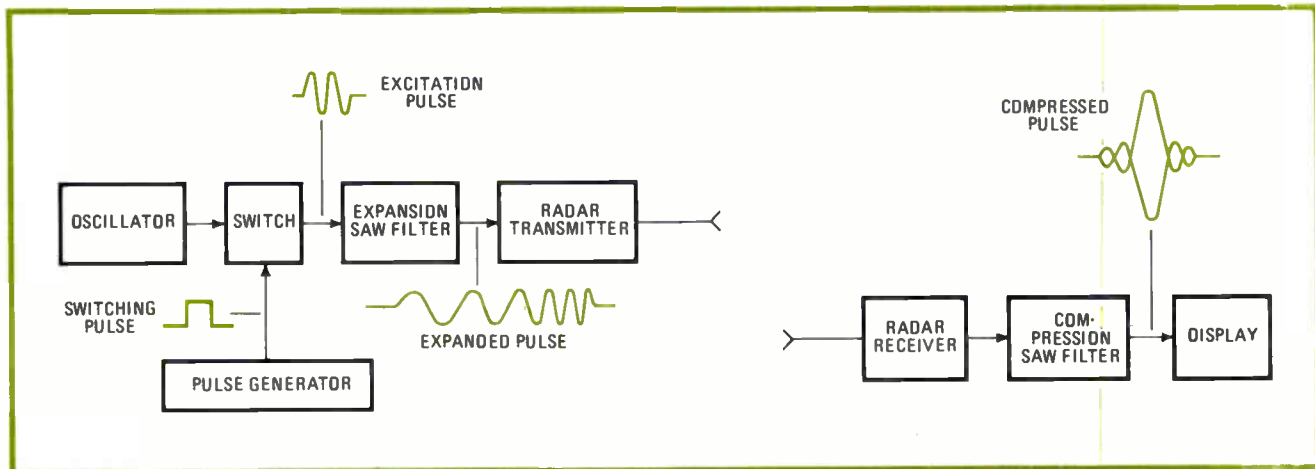
Another example

A typical filter intended for a similar synthesizer application is designed to pick 288 MHz from a series of frequencies spaced by 2 MHz. This means an initial developmental synthesizer with 8-MHz frequency spacing at L band.

Happily, the required spurious-level suppression of at least 60 dB is possible with present SAW technology. Also, advanced models of the SAW filter, with additional design techniques, allow suppression of spurious levels to greater than 70 dB.



5. Deposition. A SAW device has a thin aluminum pattern of interdigital electrodes on a polished substrate. The size and density of the electrodes in the chirp transducer determine the generated frequencies for both the down-chirp (a) and the up-chirp waveforms (b).



6. Simple radar. In a typical pulse-compression radar, the SAW devices play cost-saving roles in both the transmitter, where they expand the input pulse, and the receiver, where they compress the received signal. Modifying SAW electrode geometry reduces clutter level.

SAW filters are also attractive for use in the intermediate-frequency section of receivers and transmitters. The ability to specify amplitude and delay characteristics independently is especially important in digital communications systems where a constant, flat delay is required between input and output.

This feature was applied to good advantage recently in a mobile ground terminal for a military satellite communication system. The filter delay flatness of ± 150 ns required was not too difficult to achieve. The passband requirements, on the other hand, were more stringent. The system uses phase-shift-keying modulation, and the energy spectrum of the data is not flat across the frequency band but has a classic $(\sin X)/X$ shape.

If a filter shapes the amplitude characteristics of the incoming data so that the resulting output energy spectrum is flat, then intersymbol interference—a form of noise—can be reduced. The design of such a filter is straightforward when symmetrical transducers for flat delay are used along with established synthesis methods to achieve the necessary amplitude characteristics. The spectrum of the data filtering is then flat and the delay is not significantly distorted.

The motivation behind the development of linear frequency-modulated chirp radar has been to overcome

the peak power limit imposed on a radar system by the capability of the transmitter tubes. The demand for more range entails the use of longer signal pulses.

But the increased range demand is accompanied by a requirement to maintain the resolution of very short pulses. This conflict is solved by the use of matched filtering techniques in the receiver. Still, the bandwidth required to process the older narrow radar pulses is also required for the longer-duration matched-filter waveforms, since this parameter is determined by the range resolution specified for the radar.

Where the radar transmitter is operated at nearly maximum output power, the ideal waveform is one with constant amplitude. Here the instantaneous frequency and time are related by a straight line.

Dispersive delay

In the receiver, a matched filter (the compression filter) is used to compress the transmitted radio-frequency pulse. The compressor's impulse response is a waveform with a constant envelope in which the instantaneous frequency varies linearly with time but with a slope the opposite of the transmitted pulse (Fig. 3).

The compressor delays higher frequencies more than the lower ones. Thus, it will collapse or compress the



7. A pair. A typical 100-MHz expansion and compression filter pair may readily be implemented in dual in-line packages. Plastic or TO-8 cans are possible alternatives, depending on the application, while machined parts may be necessary for some custom designs.

original transmitted radar pulse into a single narrow pulse. The envelope of this compressed pulse (Fig. 4) is a $(\sin X)/X$ function. The width of the pulse τ , which determines the resolution of the radar, is measured at points on the pulse that are 4 dB below its peak value. Under the condition of a rectangular-envelope frequency modulation, the compressed pulse width τ is the reciprocal of the radar signal bandwidth BW .

The time-bandwidth product

An important figure of merit for a pulse-compression radar is the time-bandwidth product, $T \times BW$, where T is the dispersion time (the duration of the chirp waveform) and BW is the bandwidth. The peak amplitude of the pulse relative to the input is then given by $T \times BW$, the peak power is proportional to $T \times BW$, and the transmitted pulse is compressed in the receiver by a factor of $T \times BW$.

But the waveform of the compressed pulse is not particularly desirable for a radar system since the sidelobes of the $(\sin X)/X$ pulse are only 13 dB below the peak. Since these sidelobes are interpreted as spurious echoes by the radar, the dynamic range, or clutter level, of the radar is quite low. More advanced techniques of wave shaping in the receiver matched filter can, howev-

er, be employed in order to reduce these time sidelobes to more acceptable levels (greater than 25 dB).

A SAW implementation of these concepts is particularly simple (Fig. 5). One transducer has only a few electrodes and has a bandwidth much wider than the radar waveforms being processed. The other is a chirp transducer. Each chirp transducer basically produces a sampled version of the linear fm waveforms that are shown in Fig. 3, with two samples per cycle of each instantaneous frequency.

Putting the squeeze on

In the down-chirp case, a narrow rf pulse (width less than τ) is applied to the wideband transducer. The resulting surface-acoustic-wave pulse propagates to the left toward the chirp transducer and first excites the closely spaced high-frequency electrodes. As the acoustic pulse continues to propagate to the left, the farther apart lower-frequency electrodes are excited. Thus the output electrical signal, which is transmitted as a radar pulse, shifts from high to low frequencies.

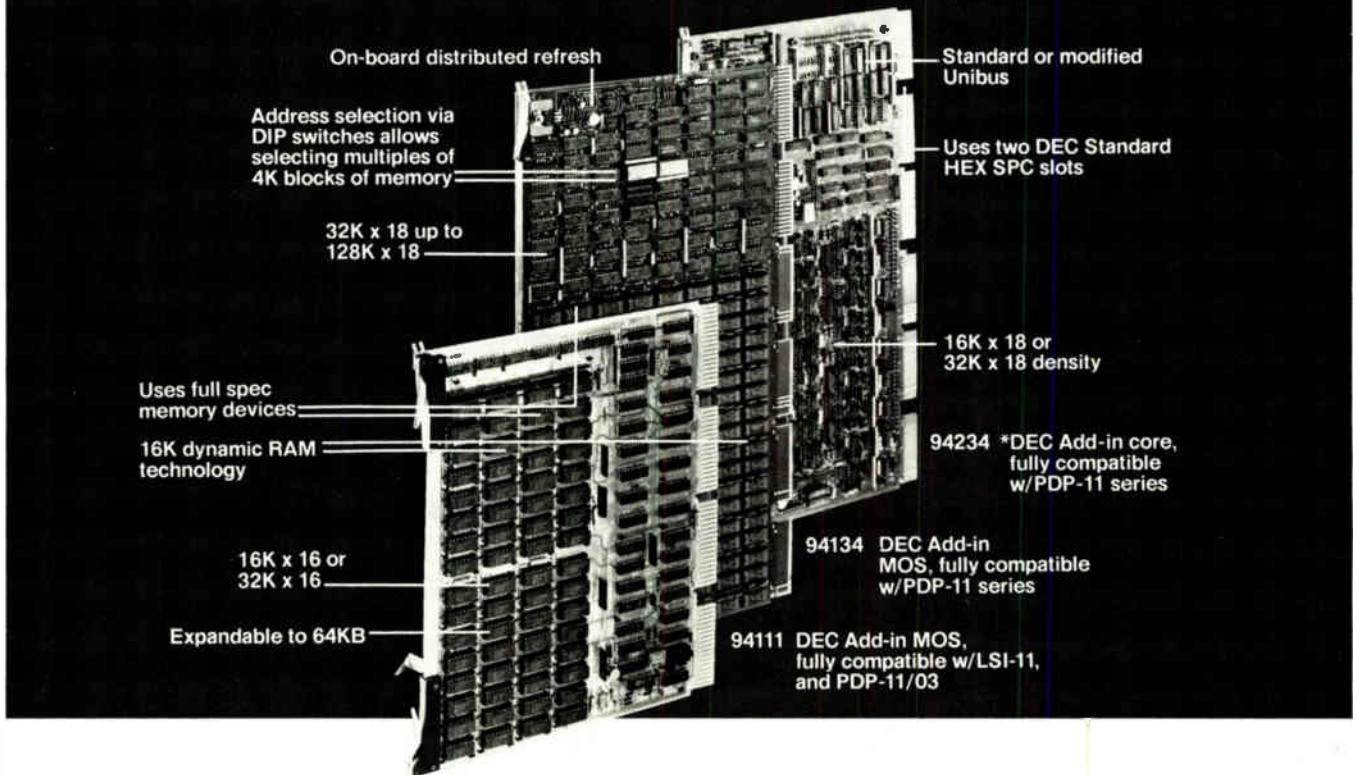
The reverse process occurs as the reflected radar pulse is converted into an acoustic wave in the wideband transducer of the up-chirp device. The high frequencies of the pulse must propagate the full length of the chirp transducer before high-frequency electrodes are encountered. They therefore experience the most delay. Likewise, the low frequencies enter the SAW device last but experience the least delay. Only when the complete waveform has propagated so that it coincides with the sampled version represented by the transducer electrodes does the filter generate a significant output signal. At the same time, τ seconds later, the waveform has propagated so that coincidence no longer holds, and the output quickly falls to the sidelobe level.

A typical pair of such linear fm chirp filters, manufactured by the Filter Products Group at Rockwell International Corp., was designed for a center frequency of 100 MHz, a bandwidth of 7.5 MHz, and a dispersion time of 10 μ s (Fig. 6). The excitation pulse is a short rf burst usually at the center frequency of the SAW filter. The output that results from the SAW expansion filter is used to modulate the transmitter. In the receiver, the rf echo is processed by the compression SAW filter.

As mentioned, the sidelobe level that occurs before and after the impulse as a result of using constant-amplitude expansion and compression filters leads to a -13 -dB clutter level. To improve the performance of the radar, the impulse response of the compression SAW filter is designed to weight the compressed pulse. With this approach it is relatively easy to achieve greater than -25 -dB time sidelobes by modifying the SAW transducer electrode geometry.

In one case where the impulse response of the SAW device is designed to approximate a Taylor weighting function, the compressed-pulse measured-time sidelobe level is -27 dB. This reduction is achieved by sacrificing some compressed pulse width. In fact, the measured width of the compressed pulse is about 25% wider than that predicted by the inverse bandwidth. The packaged 100-MHz filters are 2 by 1 by 0.19 in. and replace LC filters occupying several cubic feet (Fig. 7). \square

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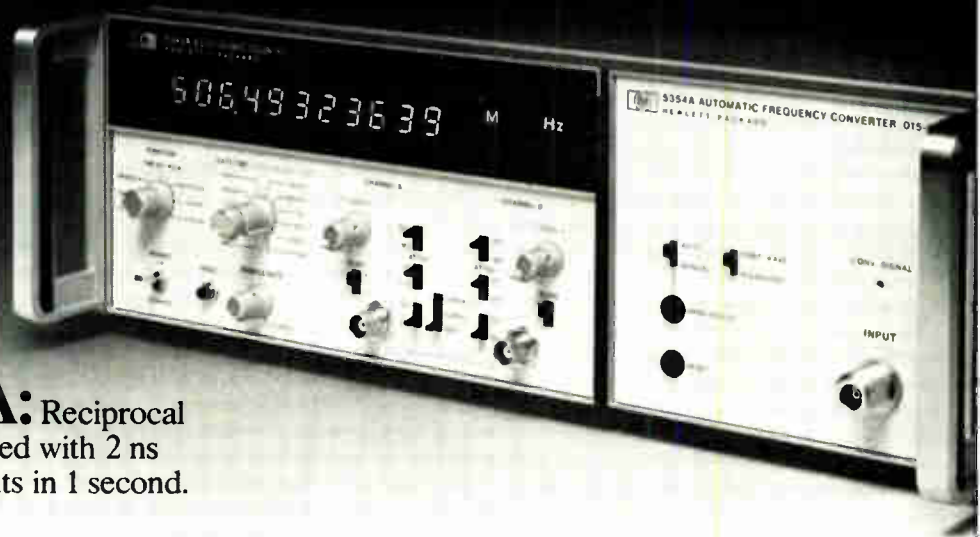
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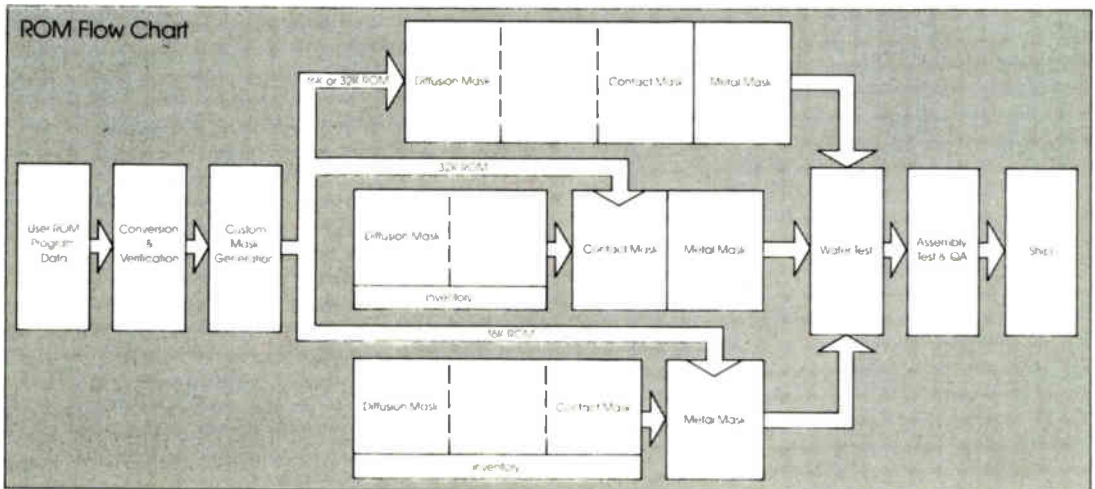
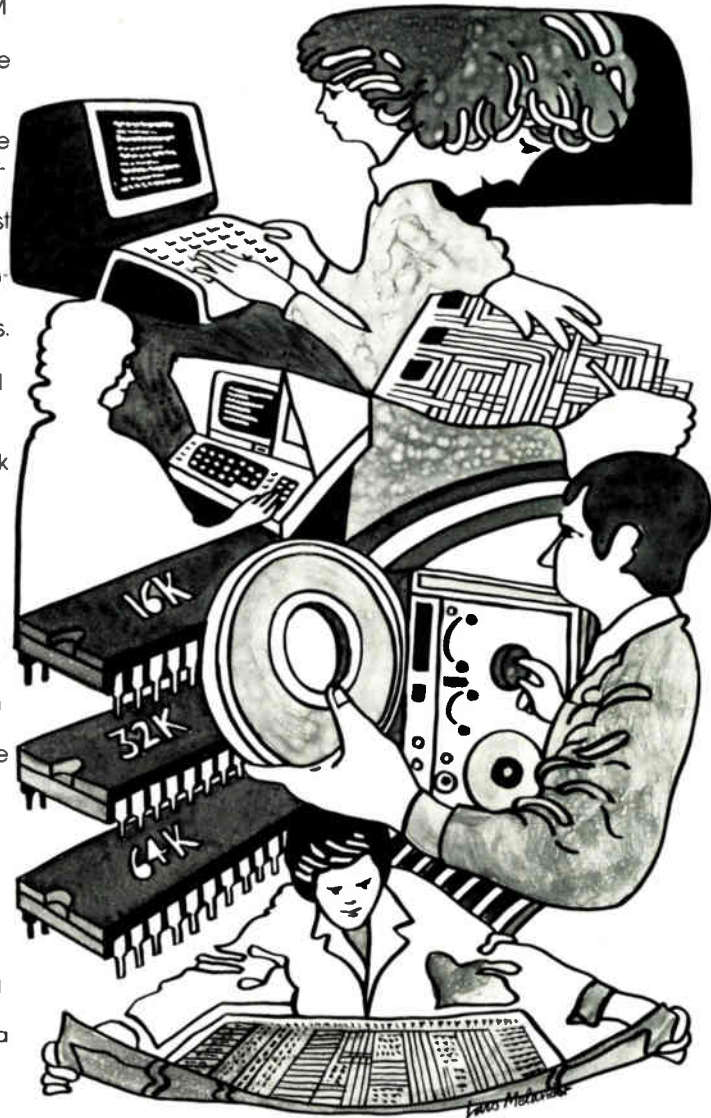
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Parallel processing with minicomputers increases performance, availability

Part 1 surveys the techniques and configurations currently in use

by Jerry Braun and George White, *Computer Automation Inc., Naked Mini Division, Irvine, Calif.*

With the costs of computer hardware dropping so rapidly these days, parallel processing is gaining ground as a hardware architecture—especially for minicomputer systems. And with the path lengths in large-scale integrated circuits like microprocessors nearing theoretical limits, such an approach may at some point become the only method of increasing the performance of a computer system.

This, the first part of a two-part article, examines the various approaches to parallel processing, with particular attention to their applicability to minicomputer systems. Part 2, in the next issue, will discuss parallel processing with Computer Automation's 4/10S slave processor.

□ The concept of using two or more computers in parallel to perform a given set of tasks has long been attractive. But the current prices and the performance characteristics of minicomputers are making these techniques increasingly economical. One of the most practical parallel-processing methods for enhancing the performance of a minicomputer system is to attach a second minicomputer as a peripheral, or slave, processor.

The term "parallel processing" refers to the ability of a computer system to perform more than one operation at a given instant. But with the concept gaining popularity, the phrase has been subject to varied interpretations and considerable misuse. For example, it is often used exclusively to refer to multiple central processing units (CPUs). But there are, in fact, methods of employing parallel processing within a single CPU.

"Multiprocessing" is another term that means different things to different people. As used here, multiprocessing systems are those configured with more than one CPU, a single integrated operating system, and shared resources such as memory and input/output devices.

Types of parallel processing

There are four general kinds of parallel processing: single instruction–single data stream (SISD), multiple instruction–single data stream (MISD), single instruction–multiple data stream (SIMD), and multiple instruction–multiple data stream (MIMD).

Most single computers in use today are SISD machines. This type of processor serially executes instructions that operate on a single stream of input data. Yet, within a single central processor there are various functions that can be completed in parallel to enhance system

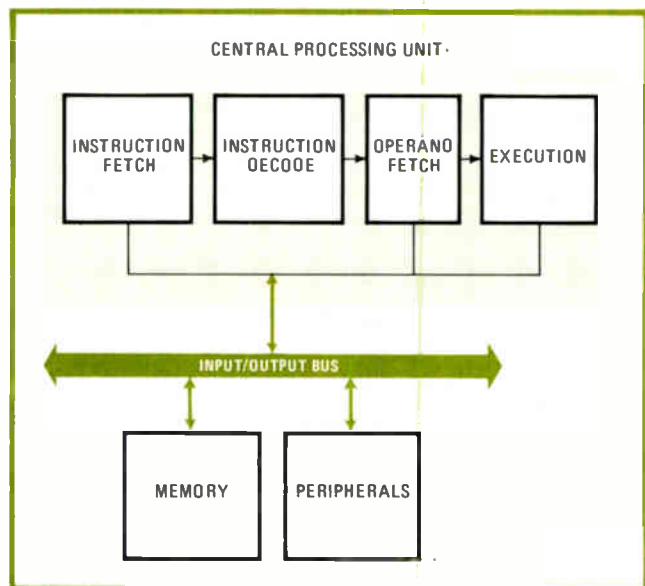
performance. Such a scheme, called pipelining, is illustrated in Fig. 1. One of the greatest benefits of instruction pipelining is its transparency to the user: when implemented properly, the performance of instructions can be increased significantly without affecting the code already written.

The actual execution of an instruction can be divided into four distinct parts. First, the instruction must be fetched from memory. Then, it must be interpreted, or decoded. Next, the operand or operands must be fetched from memory. Finally, the instruction must be executed.

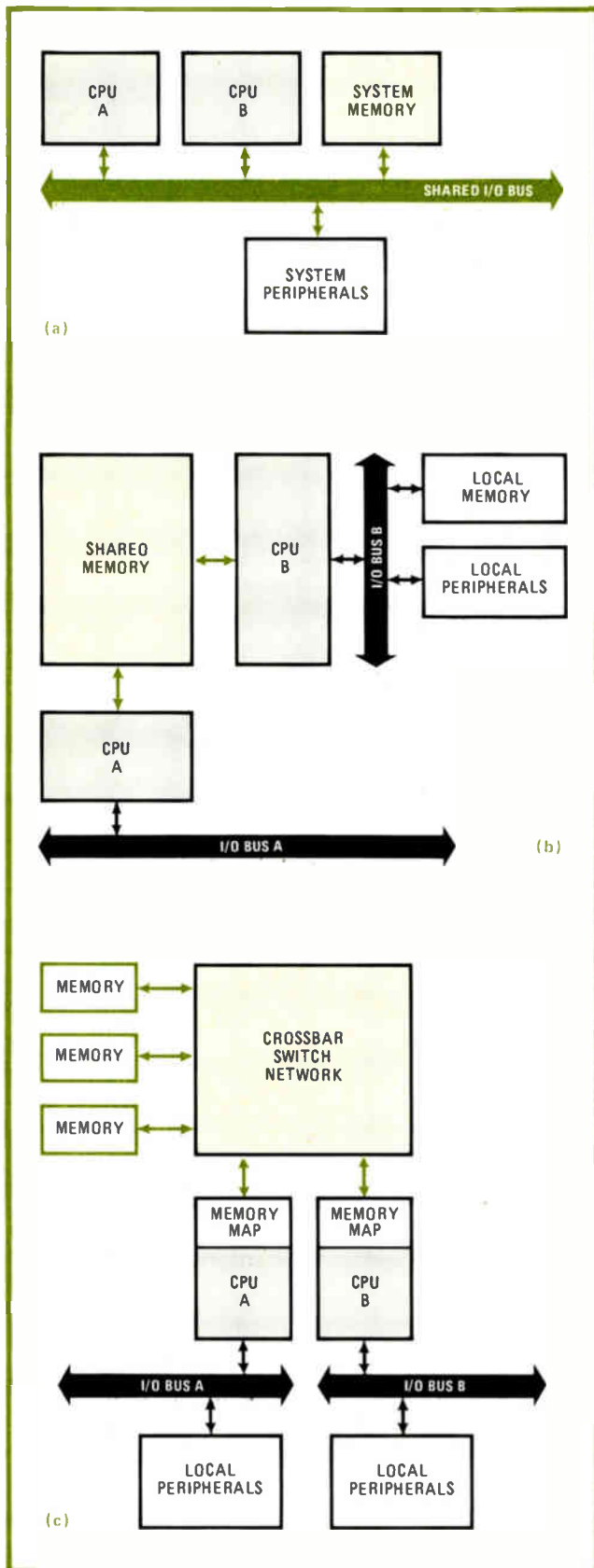
Pipelining

If all these operations are performed in parallel for successive instructions, as on an assembly line, the next instruction can be fetched while the first one is decoded, and so on. If the "pipe" can be kept full, the incremental time to complete an instruction can be reduced to just the execution time.

Examples of single-CPU machines using internal parallel processing include Digital Equipment's VAX-11/780, Data General's NOVA 4, and Intel's 8086 microproces-



1. Pipelining. While one instruction is being executed in an SISD central processing unit, others are being prepared in the pipeline that fetches instructions, decodes them, and gets the operands.



2. Share and share alike. Tightly coupled systems all share common memory but can access it either through a shared bus (a), a multiported memory system (b), or a crossbar switch network (c). Such systems generally also share an operating-system executive.

sor. SISD machines may be combined in various configurations to yield each of the other three types of parallel-processing machines.

The MISD approach, although it completes the symmetry of the types of parallel processing, is in reality highly impractical and therefore unlikely. The notion of performing multiple streams of instructions to operate in parallel on a single datum is, as far as can be seen, of no use. Thus such systems remain theoretical.

When an application calls for extremely fast calculation on vector data, an SIMD machine provides an excellent solution. Although this type of system initiates only a single instruction at a time, as does an SISD machine, the actual operations on the various data elements in a vector are performed in parallel by multiple arithmetic and logic units.

The complexity of SIMD machines, coupled with the requirement for extremely fast logic, usually dictates a very high price. Well-known examples of SIMD machines include the Cray-1 and Illiac IV. Such implementations fall well outside of the class of mini- or even megaminicomputers discussed here.

In general, the most common parallel-processing applications employ the MIMD approach. In particular, this type is the most appropriate for applying parallel processing to a minicomputer.

Multiples

An MIMD machine, as its name indicates, executes multiple streams of instructions in parallel, with each instruction operating on a separate set of data elements. Such a system generally consists of two or more central processors that are connected by one of several methods. Resources such as memory and I/O devices can be either shared by the CPUs or used privately by one CPU. Data regions can be shared or maintained separately, depending on the degree of interconnection, or coupling.

Because MIMD configurations consist of logically separate processors, existing processor and bus structures may be employed; in contrast, an SISD or SIMD machine generally must be designed as such from the beginning, with no possibility of change later. Furthermore, MIMD systems may contain mixtures of machines, each of which may be an SISD or SIMD processor.

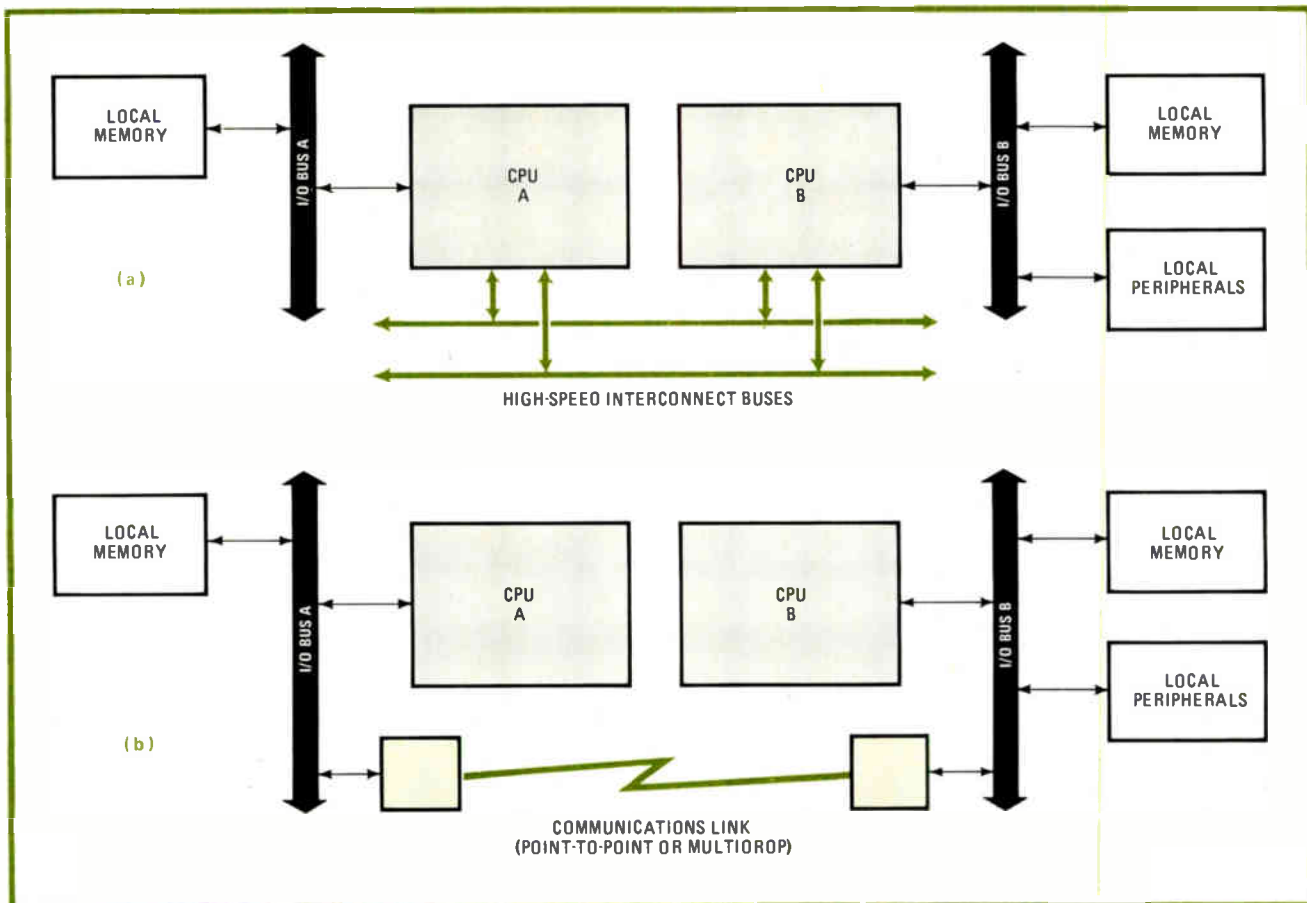
Carnegie-Mellon University's C.MMP experimental minicomputer is a good example of an MIMD system, as are the commonplace "smart" peripheral controllers.

MIMD architectures

The methods of interconnecting the processors in an MIMD system are varied and have software, as well as hardware, implications. The individual requirements of each application—be they, for example, high availability, enhanced performance, or distributed functions—dictate which of these methods will apply.

Most MIMD systems have one of four basic organizations, or architectures:

- Tightly coupled, in which two or more processors operate with shared memory and I/O.
- Loosely coupled, in which a high-speed bus or communications link connects multiple CPUs, each having its own memory.



3. Independently linked. Loosely coupled MIMD systems feature independent local memory and peripherals, but the central processing units are interconnected either by high-speed buses (a) or by slower, traditional communications links (b).

- Voting, in which at least three CPUs execute the same instructions and the results are compared—for applications requiring high availability.
- Peripheral processing, which provides fast handling of data by having one or more processors performing some of the host CPU's work—perhaps the most common form of MIMD parallel processing.

Tightly coupled

A key feature of tightly coupled systems is the sharing of a single memory among the various CPUs. Most tightly coupled systems also use a single shared operating-system executive to control the execution of tasks. Thus provisions for synchronization, interlocking, and interprocessor communication must be made in the hardware to accommodate a true multiprocessor operating system. The major difference between configurations is the method of accessing the memory.

The shared-bus approach (Fig. 2a) offers the advantage of free access to both memory and peripheral devices by each of the processors in the configuration. The disadvantage is seen in an environment where the combined activity of high-speed I/O and memory access exceeds the speed of the bus. In most minicomputers, where system buses operate at rates ranging from 1.5 to 5 megabytes per second, the aggregate activity can easily overburden the bus. In addition, not all bus designs can handle the arbitration required for multiple CPU masters

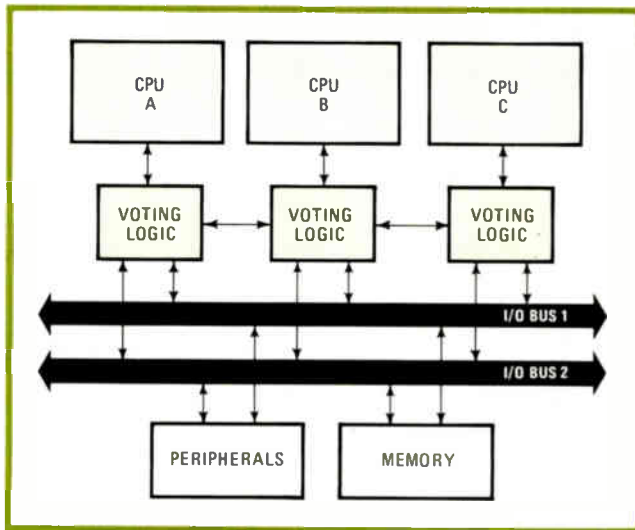
on the common bus. This capability must therefore be designed in initially.

A multiported, shared memory (Fig. 2b) can alleviate the problem of bus contention by allowing each CPU to retain its own I/O bus or buses. This leaves the memory itself as the only system element subject to contention. However, this remaining contention and the inherent costs of designing a multiport memory restrict the general utility of this approach.

The crossbar interconnecting scheme (Fig. 2c) is flexible and can be very fast. Memory and bus contention may be kept to a minimum through multiway interleaving. The expense and complexity of the crossbar network, however, have limited the number of such systems to date.

Loosely coupled

There are two very similar approaches to building a loosely coupled parallel-processing system. They have similar software ramifications but differ in potential speed. One configuration uses one very high-speed bus (or two, for redundancy) to interconnect a number of central processors (Fig. 3a). Each CPU has its own memory and a copy of the operating system. Peripheral devices are usually attached separately to each processor, but they may be multiported to allow for both shared data access and an alternative path in the event a CPU fails. The other configuration differs only in its use



4. Computing democracy. Voting parallel processors simultaneously perform the same instructions on the same data and then their results are compared by special logic. If one processor disagrees, it is "voted" out of the configuration and labeled for repair.

of a much slower communications link to tie the CPUs together (Fig. 3b).

One excellent example of a commercially available minicomputer-based system employing a loosely coupled architecture is Tandem Computers' T-16. If a buyer uses Tandem's operating system and software support, the company claims that there is no single point of failure. It must be noted that the software is a key element in ensuring such availability.

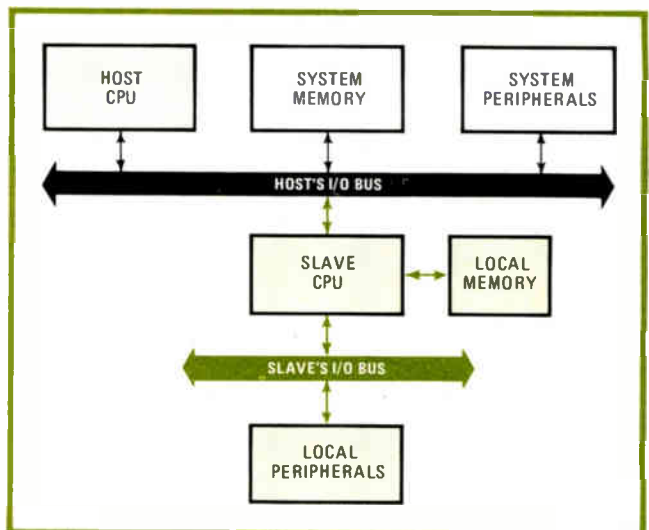
Distributed processing and networking also fall under the heading of loosely coupled parallel processing. Computer Automation's Virtual Network architecture for the SyFa Network Processing System is a prime example of the distribution of work load throughout an extremely loosely coupled network of computers.

There are certain unique classes of applications that require virtually uninterrupted system availability. In addition, all errors must be detected and either corrected or the faulty element removed. The voting architecture (Fig. 4) was designed to meet such stringent requirements. But this form of parallel processing offers no performance advantage over an SISD machine.

Voting processors

The voting architecture is actually a combination of the SISD and MIMD approaches in that there is generally only one instruction stream executed, but three or more separate processors execute these instructions simultaneously, with the results compared by special-purpose logic. The name "voting" is derived from this comparison: if any result differs, the erring CPU is "voted" out of the configuration. The remaining machines then continue operating until the faulty CPU is repaired.

Often a fourth CPU is kept on standby to replace an erring processor. Having a fourth unit available ensures that at least three CPUs will perform all calculations, since, if a second-stage error occurred, the use of only two processors would make it impossible to determine which one failed.



5. Peripheral slaves. Peripheral processors generally operate as slaves to a host processor but have their own memory, input/output bus, and peripherals. Using direct-memory-access techniques, they can also access the host's system memory or peripherals.

The expense involved in dedicating multiple CPUs to a single stream of instructions and data makes voting architectures a fairly rare phenomenon. They are used primarily for military and aerospace applications that cannot tolerate failures or even extremely short-term interruptions in computer equipment.

For minicomputers, peripheral processing is perhaps the most prevalent and practical approach (Fig. 5). Peripheral processors are commonly found in minicomputer systems—as device controllers, array processors, communications and I/O front ends, and even as system consoles. A major reason for their popularity is that few if any design changes in the CPU or bus structure are required for implementation.

Relative applicability for minis

Each of the interconnection techniques described above can be used to configure multiple-minicomputer systems of the MIMD type. However, some architectures are better suited for availability, some for performance, and others for dedicated I/O processing. In addition, there are wide variations in the relative difficulty of writing system and user's software (see the table).

Producing software for either a loosely or a tightly coupled system presents a set of unique problems. In loosely coupled systems, the problems revolve around communication, data transfer, software control, synchronization, and task partitioning. To improve performance the user must determine how to partition the task between the computers so that they can operate in parallel. The operating system must fully support the interprocessor communications necessary for performing this function.

In a tightly coupled system, the major software problems to overcome are synchronization, interlocking, and contention. At the same time, there should be no software implications in a voting system.

If a user is writing software for a peripheral processor, he will likely find an environment that is reasonably easy

RELATIVE MERITS OF PARALLEL-PROCESSING ARCHITECTURES

	Loosely coupled		Voting	Tightly coupled		Peripheral, or slave, processing
	High-speed bus	Communications link		Multipoint memory	Shared bus	
Performance enhancement	moderate	low	none	significant	significant	significant
Availability enhancement	high	high	highest	low	low	none
Additional software development costs	significant	moderate	none	significant	significant	low
Ease of application to existing systems	moderate	simple	very difficult	moderate	unlikely	simple

to work with. Control of a slave peripheral processor is generally the same as for any I/O device with direct memory access (DMA). A simple device driver is often sufficient to control its functions.

A tightly coupled multiprocessor has a distinct performance advantage over other architectures and is an excellent general solution. Because all resources are shared and directly accessible, they can be accessed and allocated much faster. Also, a shared memory is the fastest way to pass data between CPUs.

In addition, if a problem can be partitioned and is special-purpose, a peripheral processor may notably improve execution of the task. The low software and hardware expense, coupled with local memory and input/output capability, make this a superior solution in a dedicated environment.

For a computer to be successful as a highly available system, it should be able to survive any single failure without ceasing to operate. Neither peripheral-processor nor tightly coupled architectures are ideally suited to satisfy this requirement because the shared bus and memory are both potential single points of failure. In contrast, the loosely coupled system, if fully redundant, has proved to be an excellent architecture for extremely high-availability applications, although it is not the highest performing. The optimally available architecture, though, is the voting parallel processor.

Adaptability to existing systems

It is often impractical to design a parallel-processing system from scratch when a particular application arises. Instead, it is more economical to use parallelism with an existing computer and bus structure. The configurations discussed earlier vary from fairly simple to impossible to adapt to a traditional minicomputer.

A tightly coupled system can be difficult to construct and requires considerable investment of time and money because of the special hardware and software needed. In particular, the voting architecture is so heavily tied to

the internal design of the CPUs that a retrofit of a traditional mini is not possible. To repeat, an initial design is required.

For a loosely coupled system, the difficulty depends on the method of interconnection. Use of a communications line is reasonably simple, whereas use of a high-speed bus is more complicated.

Peripheral processing in minicomputers

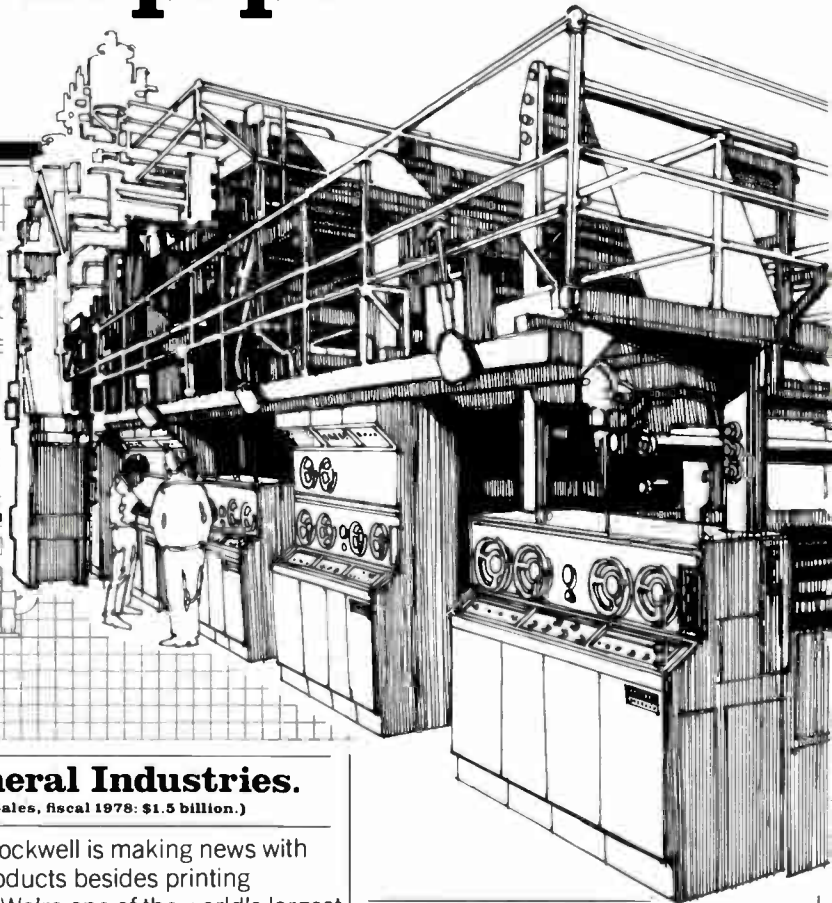
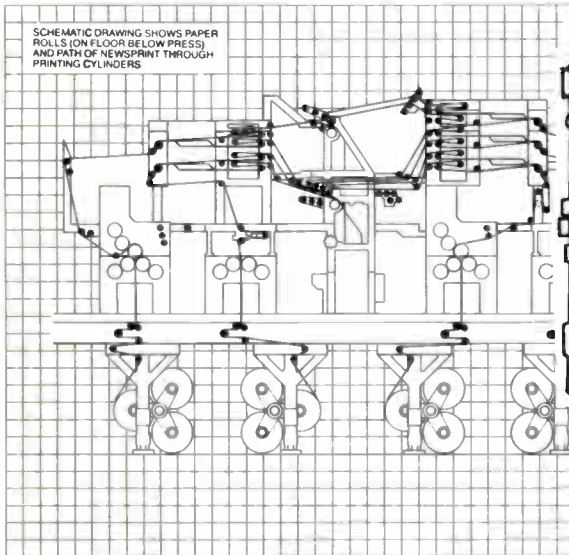
As noted, one of the most practical approaches for parallel processing using existing minicomputers is the peripheral-processing organization. Traditional minicomputer buses are based on the concept of a single CPU with multiple memories and multiple I/O controllers on a common bus. These bus structures typically require the CPU to occupy a particular bus slot; that unique slot receives and transmits bus signals in a manner peculiar to that processor. Adding extra, equal CPUs directly to that structure would not be feasible. But peripheral processing fits naturally into existing minicomputer organizations. The minicomputer system continues to have the single master CPU it originally had, with the peripheral processors being added to the bus in the same way as DMA I/O controllers are. Minicomputer buses are already set up to handle multiple DMA devices and allow them access to the shared system memory.

Many modern I/O controllers are in fact peripheral processors: they contain microprocessors and control I/O devices in smart ways that take a burden from the host CPU. Some of these controllers use 8-bit MOS microprocessors; others, which handle faster data rate devices, use bit-slice, microcoded logic.

Computer Automation's recently introduced 4/10S slave processor is one example of a general-peripheral processor [*Electronics*, May 24, p. 202]. This unit can be programmed by the user, whereas specialized I/O peripheral processors cannot. The design of the 4/10S and the implications of its programmability for users will be discussed in Part 2. □

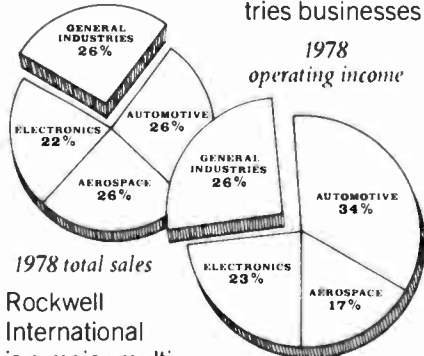
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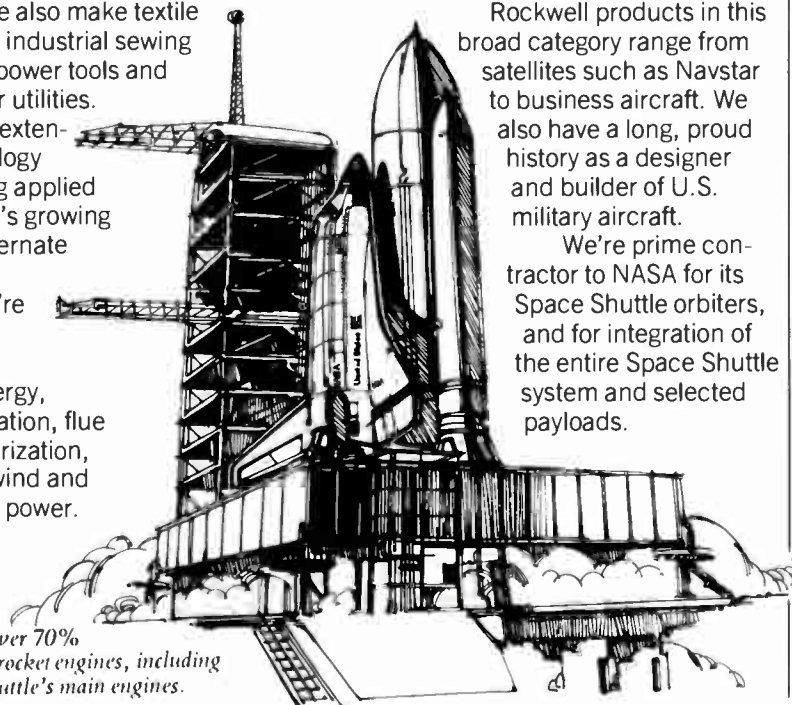
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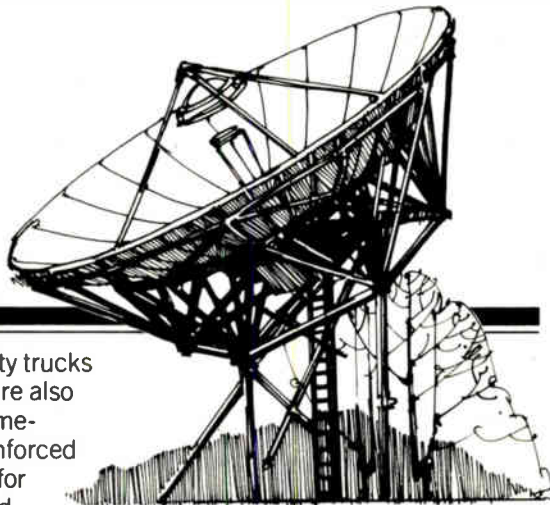
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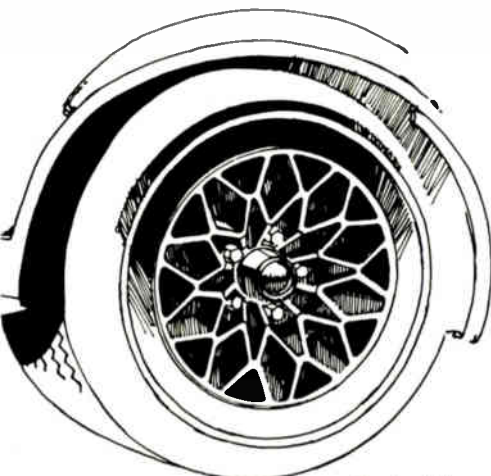


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Hyperbolic clock Inverts time

by Keith Baxter
New Haven, Conn.

Instruments designed to measure speed must contain circuits for converting a time function, t , to units of $1/t$ in order to calculate rate. This circuit aids in plotting the hyperbolic curve ($1/t$) using relatively few parts and, notably, having no need for logarithmic dividers.

As shown in the figure, a start pulse triggers transmission gate S_1 , initiating the measurement cycle. At that time, A_1 and A_2 are reset. Current I_1 thereupon charges C_1 linearly, and thus a ramp voltage is applied at the noninverting input of A_3 .

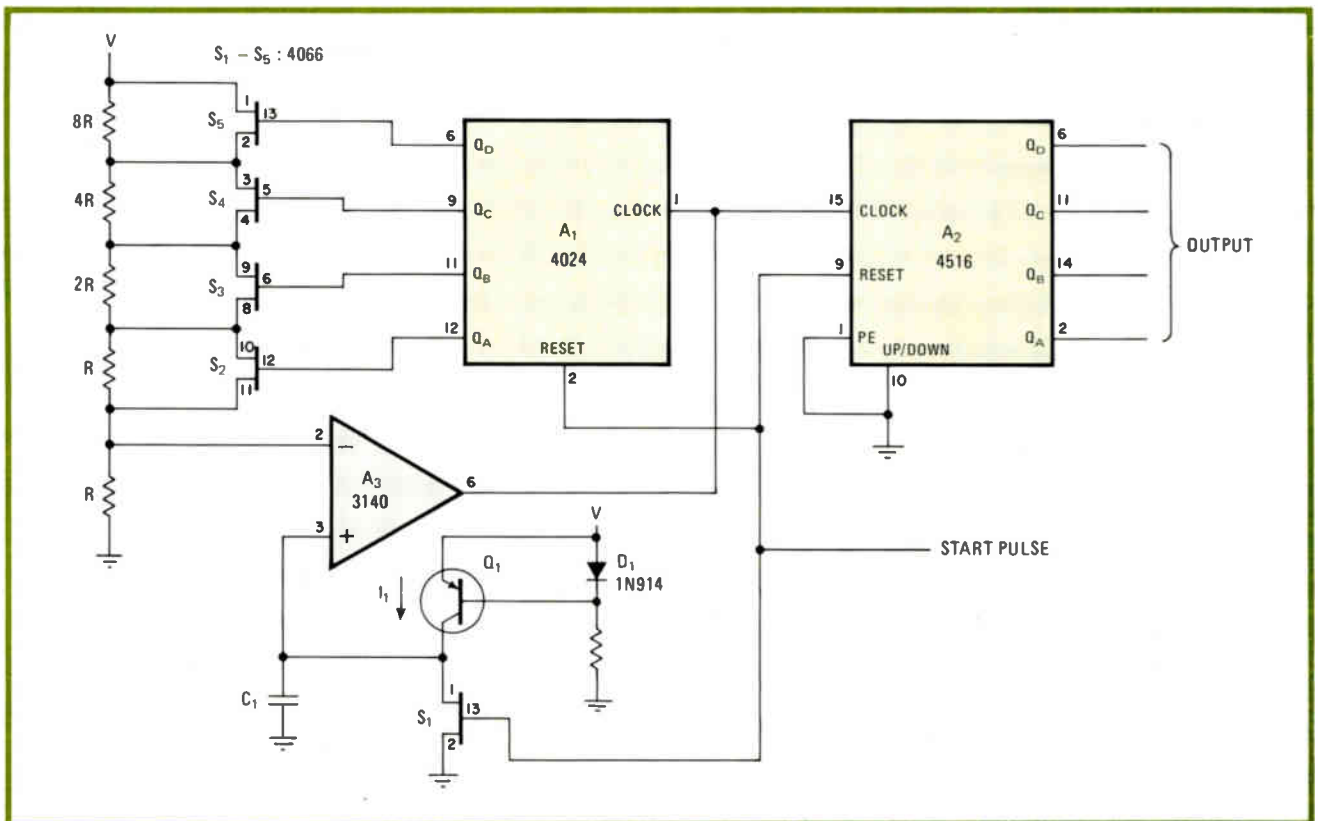
When the ramp voltage reaches $1/16$ volt, the potential at the lowermost tap on the resistor voltage divider A_3 moves high and advances counter A_1 . At this instant, the total elapsed time is $1/16 (C_1/I_1) V$.

Switch S_2 is then activated, so that the second resistor

in the ladder is shorted. Thus the voltage at the inverting port of A_3 increases to $1/15 V$. When the ramp voltage reaches this value, A_3 again moves high and fires A_2 . This action occurs at an elapsed time of $1/15 (C_1/I_1) V$. The process continues as A_1 counts to 15 in a binary sequence and either all combinations of the resistor ladder are shorted or the measurement cycle ends (start pulse held at logic 1). It is assumed the data will be stored in a latch prior to the start pulse, because A_2 will be reset. At that time, A_2 will have counted down with each clock from A_3 to provide an output corresponding to an elapsed time of $1/t (C_1/I_1) V$, where t may assume integer values from 1 to 15. Note that comparable circuit action cannot be realized easily with an astable multivibrator operating as a fixed-frequency source for stepping A_2 ; that is, the circuit is not performing a time-to-frequency conversion.

The contents of A_2 at the termination of the measurement cycle provide a direct indication of an object's speed. The factor $(C_1/I_1)V$ may be adjusted to 1 by suitable choice of component values or set to a multiplicative constant as required. Also, to reduce the voltage divider increment, the resistor ladder may be expanded by cascading counters and their appropriate circuitry. □

Time twist. Circuit inverts time function, t , to $1/t$ in order to measure speed. Note that unit does not perform a standard time-to-frequency conversion. Ramp voltage derived from current generator is compared with resistive-ladder voltage at A_3 , and A_1 - A_2 are clocked each time the ramp exceeds changing ladder potential. Output of down counter, A_2 , yields rate.



Optoelectronic alarm circuit is time-sensitive

by Forrest M. Mims III
San Marcos, Texas

Using an optoelectronic slot switch and a 556 dual timer operating as both a pulse generator and missing-pulse detector, this circuit generates an alarm when an opaque object blocks the light input for longer than a preset time interval. It has many applications and is especially useful when united with a slotted disk to monitor motor speed stroboscopically, indicating when the steady-state rotation rate is too high or low. It can also be used on the production line for checking the width of materials.

Generally, the output of the pulser periodically activates the light-emitting diode of the H13B1 switch. Other sensors may be used; Darlington photosensing

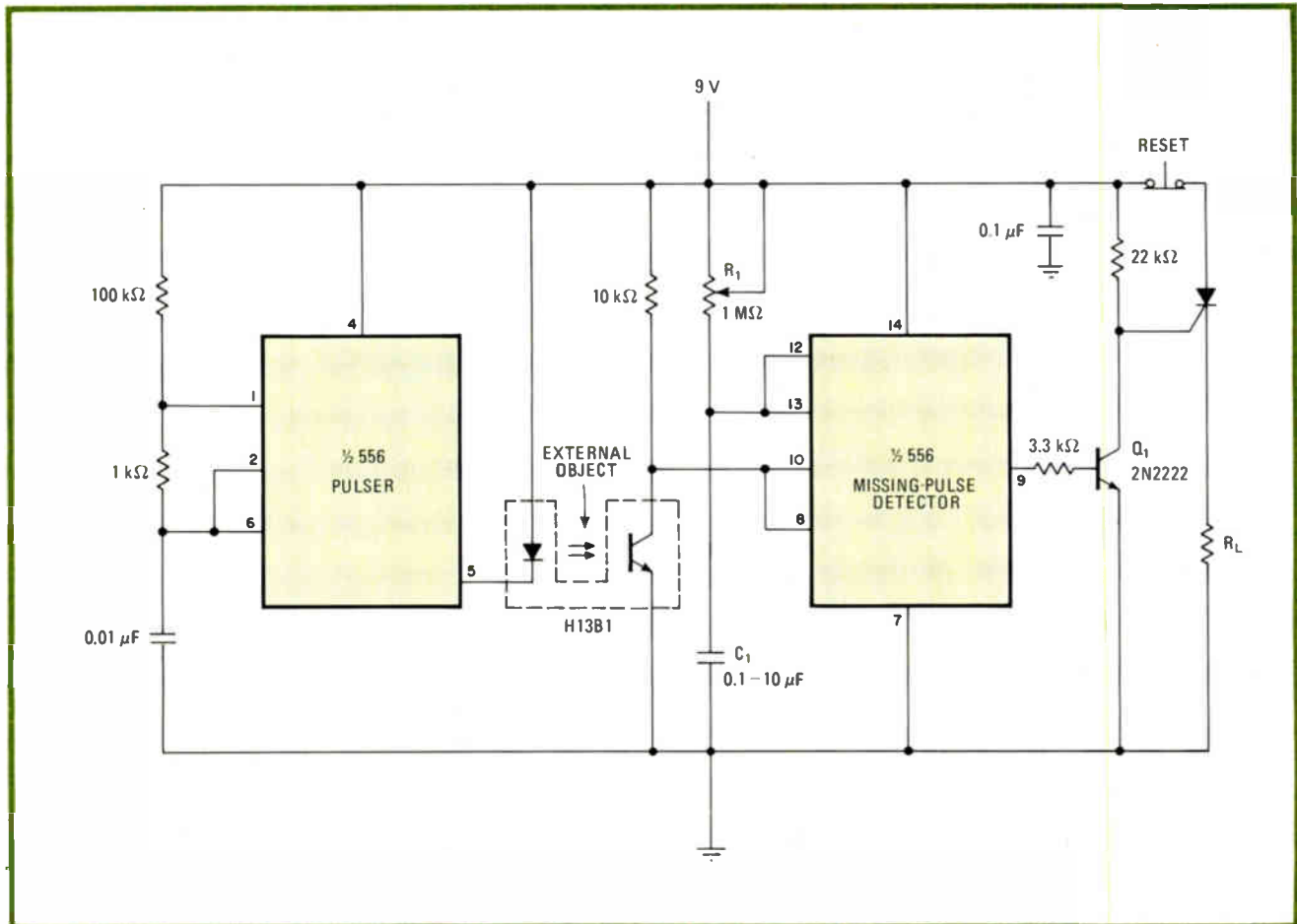
transistors, though, are the most sensitive. In this case, the pulser's operating frequency is set at 1.42 kilohertz, but it may be suitably selected by replacing the 100-kilohm resistor at pin 1 with a potentiometer.

As shown, the H13B1 is built with a slot of several millimeters separating its LED from the output phototransistor so that objects can be placed in the air gap between them. When the slot is not blocked, the phototransistor continuously resets the missing-pulse detector. Should the light path be blocked, pin 8 will remain high and the threshold voltage at pin 12 will fall at a rate determined by the adjustable R_1C_1 time constant.

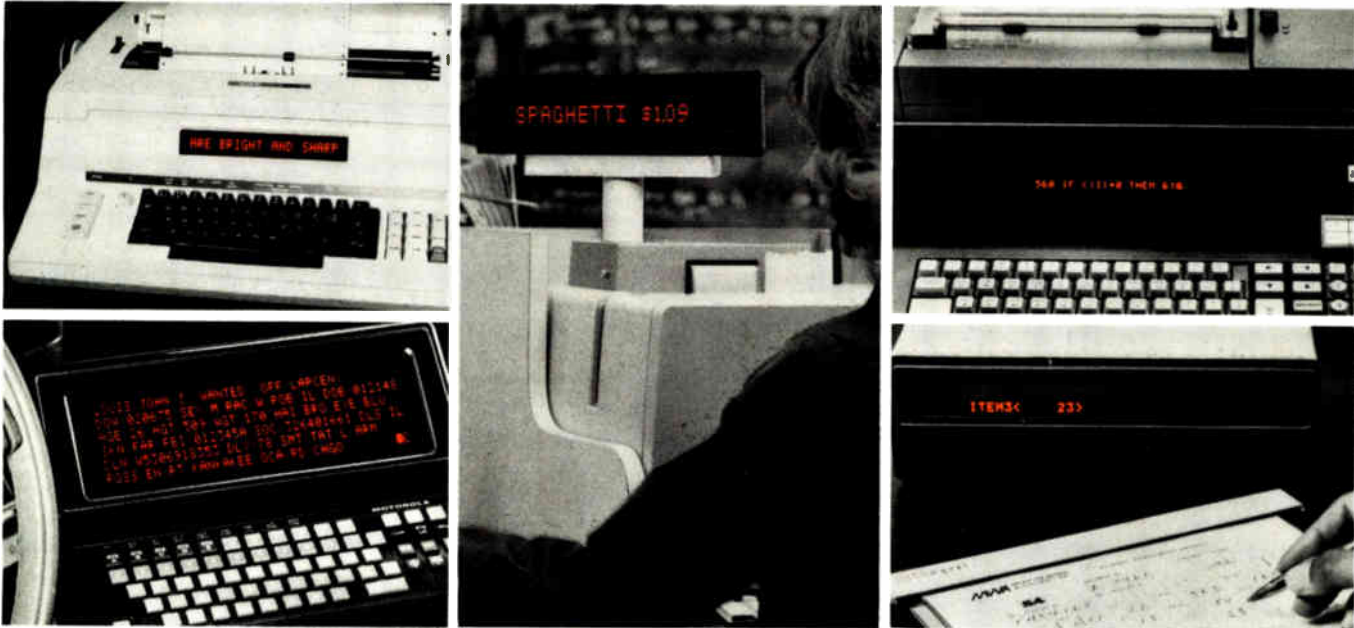
Depending on the value of this constant, which can be selected for delays from microseconds to seconds, the detector will generate a step voltage if it is not reset within that period. The signal is then inverted by Q_1 , which in turn fires the silicon controlled rectifier to drive the load, R_L .

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Light block. Pulser operating as astable multivibrator triggers LED in slot switch so that missing-pulse detector is periodically reset. Interruptions in light beam caused by external object cut off reset pulses, causing circuit to generate alarm if interval exceeds preset time.



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Burroughs

Scanner finds interrupts with highest and lowest priorities

by N. Bhaskara Rao
Department of Electrical Engineering, UVCE, Bangalore, India

In many multitask microprocessor applications, it is necessary to access not only the interrupt request of the highest priority, but the low-priority one as well. This scanning unit finds both for 14 priority-interrupt lines.

The scanning cycle is initiated when the output of counter A_1 reaches 1111, whereupon G_3 moves low and presets A_2 . Thus, A_1 begins to count down.

A_1 's output addresses A_3 , a 16-to-1-line multiplexer, to determine the priority lines requesting a program interrupt. Connected to the multiplexer's data inputs are 14 priority lines, arranged from the least significant (E_1) to the most significant (E_{14}).

When the counter steps through the location corre-

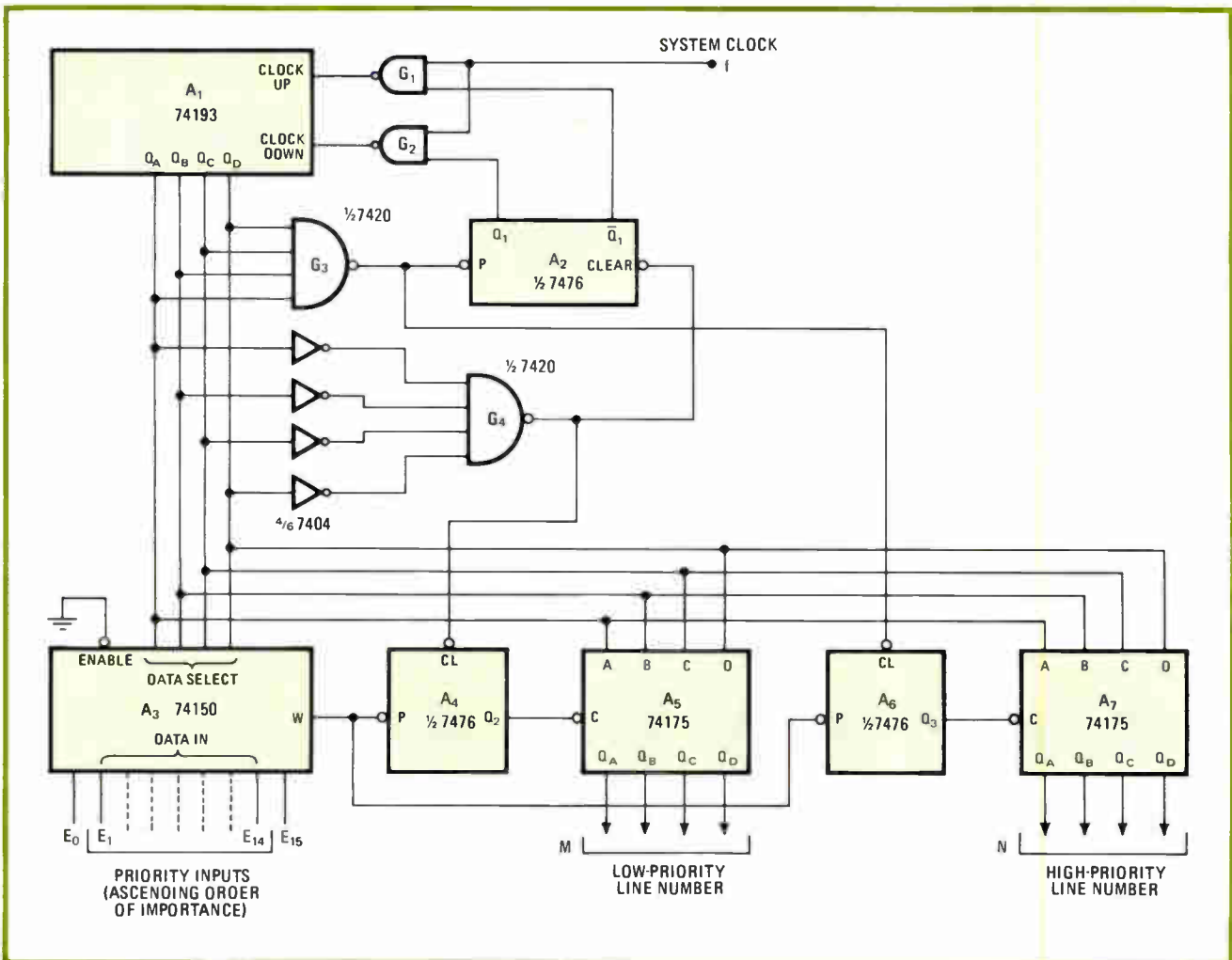
sponding to the first priority input at logic 1, A_3 's output (W) moves low and sets A_6 . Consequently, A_7 latches the counter's contents, which are the binary equivalent of the active priority input. This turns out to be the only priority input latched, because any succeeding output pulses from A_3 during the scanning cycle cannot effect the already active A_6 .

Note that A_5 latches the highest-priority line, too, but that is unimportant because the low-priority input is determined in the latter part of the scanning cycle and it is assumed that the system logic strobes A_5 and A_7 at the end of the cycle.

When A_1 reaches zero, G_4 moves low and clears A_2 and A_4 . A_1 then starts to count up. As the counter steps through the first active priority input, A_3 's output again moves low and A_5 latches the contents of the counter. Note that priority inputs E_0 and E_{15} are uncommitted so as to prevent a simultaneous generation of preset and clear signals to A_4 and A_6 under conditions where only E_0 or E_{15} would be active.

As A_1 reaches 15, A_2 is set and A_6 is cleared. The scanning cycle is then repeated. □

Line list. Scanning interface determines which of 14 interrupt requests to microprocessor have the highest and lowest priorities at any given time. Highest-priority line number as seen by 16-line multiplexer (bottom, left) is latched as bidirectional counter A_1 steps from 15 to 0; low-priority number is latched as counter moves back to 15. Both numbers are strobed by system at termination of scanning cycle.



Transparent memory ends conflicts over CRT control

Minimal added logic and faster random-access memory let controller update screen continuously, without blanking

by Lorne Trottier and Branko Matic
Matrox Electronic Systems Ltd., Montreal, Quebec, Canada

□ There exists a classic memory-contention problem common to all cathode-ray-tube displays. The problem arises when the display (refresh) memory must be accessed both by a CRT controller to refresh the screen and by a central processing unit to update the screen's information. The result: either the CPU's throughput is restricted or the screen flickers annoyingly when the refresh memory is accessed.

Transparent memory eliminates all such disturbances. The CPU can access the refresh memory at any time, the display is completely free of glitches, and the CPU is never hampered. And the method is entirely general: it does not rely on peculiar timing characteristics or a particular CPU. Thus, use with most microcomputers and minicomputers is permitted.

In a nutshell, transparent memory utilizes a clever multiplexing technique that permits nonconflicting concurrent access by both CRT controller and CPU. The concept has been incorporated into a series of 24-line-by-80-character alphanumeric video interface cards for the Intel iSBC-80 Multibus (also the National BLC bus), Digital Equipment Corp.'s PDP-11 and LSI-11/2 buses, the Motorola EXORCISER bus, and the S-100 bus.

Prior to transparent memory, the contention problem was dealt with in one of two ways. The first method, commonly known as the video random-access memory (VRAM) approach, shares the refresh memory between the CRT controller and the CPU via multiplexing circuitry and three-state buffers. With this arrangement, however, CPU accesses disconnect the refresh memory from the CRT controller and are visible as streaks or glitches on the screen. The interference can be eliminated by confining VRAM accesses to the horizontal or vertical retrace interval, but this severely restricts the frequency of screen updates.

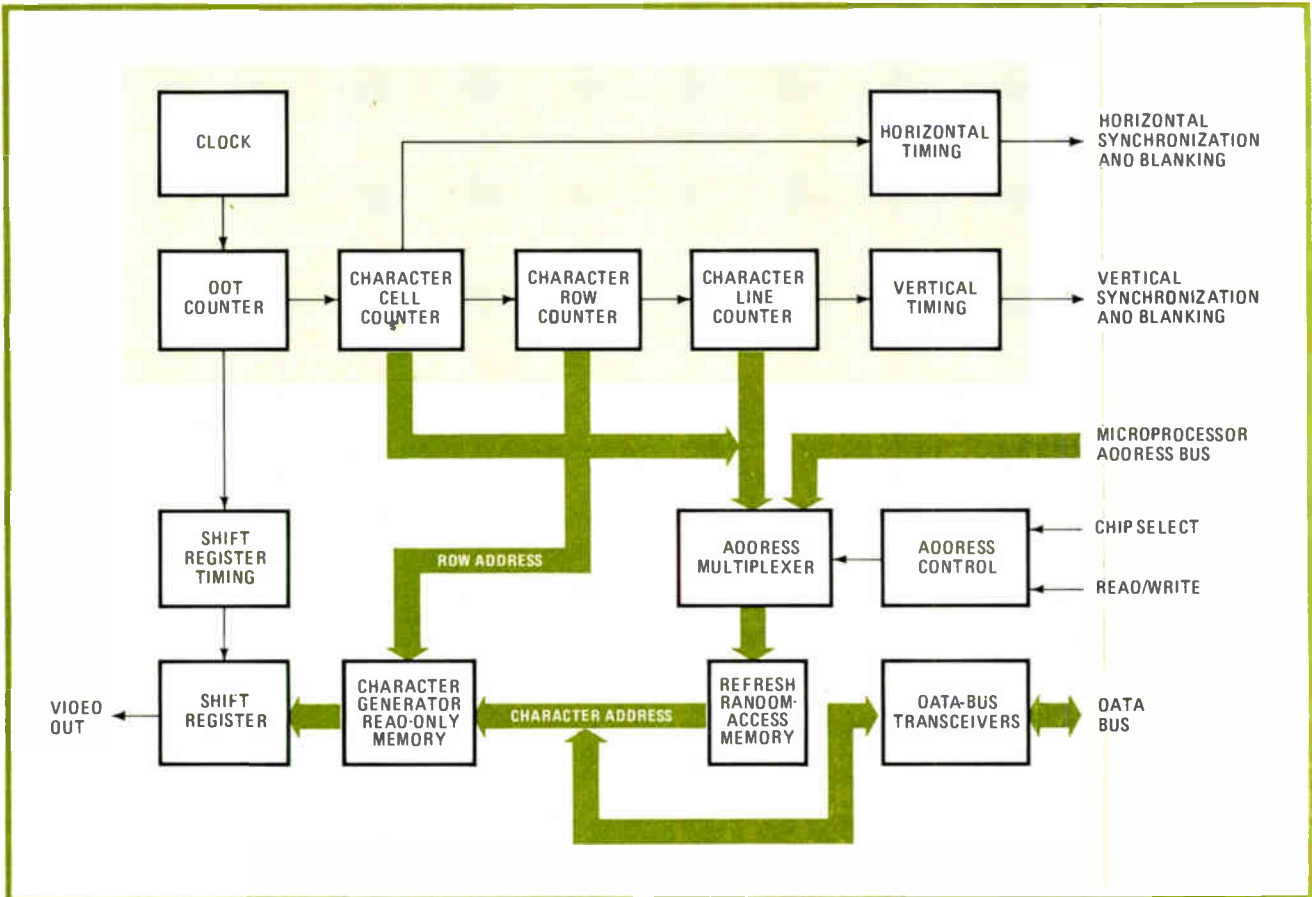
Another common solution is the direct memory access, or DMA, approach. In this case, the refresh memory is in the CPU's memory space. Unfortunately, the CRT controller must now force the CPU to halt whenever it needs access to the memory, a requirement that can cut system speed as the screen must be refreshed quite often.

Scanning CRT displays

To understand the operation of transparent memory in particular, it is first necessary to recall how standard alphanumeric CRT controllers in general operate.

The image of a raster-scanned CRT display is built up by generating horizontal lines across the face of the CRT. The electron beam starts in the upper left corner of the display, moving left to right and top to bottom so as to paint a series of zig-zag lines. The horizontal and vertical synchronization (sync) signals control beam's movement. When the beam reaches the end of a line, it is brought back to the beginning of the next line at a higher speed. During this retrace period, the electron beam is blanked so the retrace line is not visible. The pattern of lines traced is called the raster.

As the electron beam is moved across the face of the screen, the video signal controls the intensity of the beam, so that the phosphors light a desired image. In the case of alphanumeric displays, this is a simple on-or-off dot pattern.



1. **Video RAM.** With a video RAM, the refresh memory is shared between the CRT controller and the microprocessor. Unfortunately, accesses by the CPU interrupt refreshing and streaks can be seen on the screen. The sync generator, shown tinted, creates all timing signals.

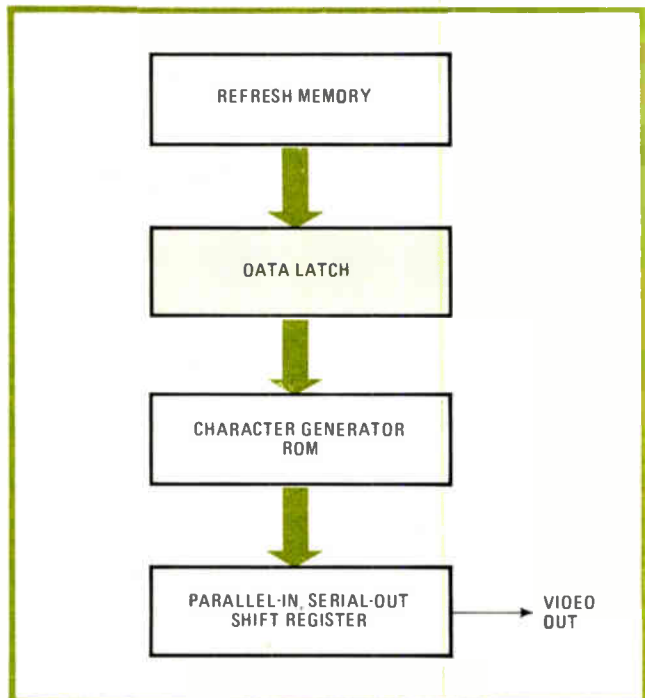
Standard CRT displays work with horizontal sweep rates of 15.7 kilohertz $\pm 10\%$ and vertical sweep rates equal to the local power-line frequency (60 hertz in North America, 50 Hz in Europe). There are normally 262 lines per complete raster scan (also known as the field) for 60-Hz displays and 312 lines for 50-Hz systems. For high-resolution applications, the number of displayed lines can be doubled by means of video interlacing. The penalty of interlacing is increased complexity and hence increased cost.

A video RAM circuit is shown in Fig. 1. The heart of this and of any CRT-display system is the sync generator (tinted), which provides all the sync and timing signals necessary to control the display.

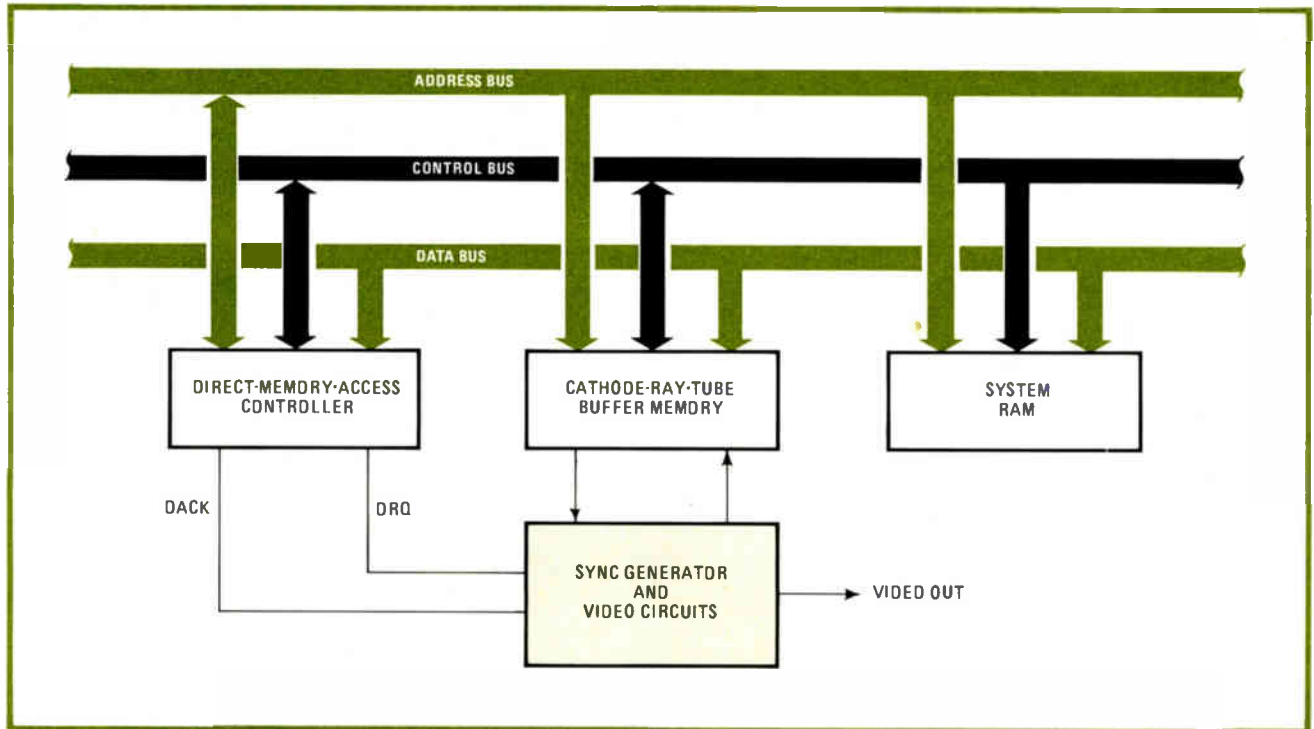
Sync generator design

To design a sync generator in the most straightforward manner, the CRT screen is divided into small cells. As in alphanumeric displays, each cell corresponds to one character position. The characters are generated by illuminating the proper combination of dots in the five-by-seven or seven-by-nine dot matrix that each cell contains. The patterns for each character are stored in a character-generator read-only memory.

The ROM requires two sets of input addresses: one to signify the character itself, the other the row of the character to be displayed. The character address is usually encoded in ASCII so that in this way a keyboard's



2. **Pipeline latch.** Without a register in between the refresh memory and the character-generator ROM, the time elapsed in a character cell's period equals the sum of the two memory devices' access times. With the latch, it is cut to the greater of the two.



3. Direct memory access. The refresh memory is directly addressable by the microprocessor in the DMA approach. However, the microprocessor is now responsible for refreshing the screen and is bogged down by the frequency with which this must be done.

output can be used directly to drive the ROM.

In a raster-scan display, the electron beam provides only a slice of each character, one row at a time, as it scans a line. The row outputs of the ROM are latched into a parallel-input, serial-output shift register, then shifted into the video-generation circuits in serial fashion, as shown in Fig. 1.

The shift register is clocked by the sync-generator dot counter. Before reaching the shift register, this clock signal is first fed into a dot counter. This counter divides the clock signal by the number of dots per character cell. The output of the dot counter also drives a character-cell counter that keeps track of the number of cells on the current line. This is determined by the number of characters per line plus 25% to allow for retrace.

Horizontal sync and blanking signals are decoded by gates (not shown) connected to the character-cell counter. This counter also provides a part of the display-memory address and feeds another counter that keeps track of the number of lines displayed for a particular cell. This character-row counter drives directly the row-address lines of the character-generator ROM.

The last noteworthy counter in the sync generator is the character-line counter. It is responsible for the number of character lines to be displayed, and its maximum-count value is set by that number plus 20% to 25% for vertical retrace. Vertical sync and blanking signals are also decoded off this counter's outputs as are the remaining address lines of the display memory.

All of the video information must be refreshed, and a block of static RAM sufficient to store at least one full page of data is usually used. Although charge-coupled devices, shift registers, or dynamic RAMs could be used for page storage, static RAMs usually offer the best

tradeoff in terms of their cost, size, and complexity.

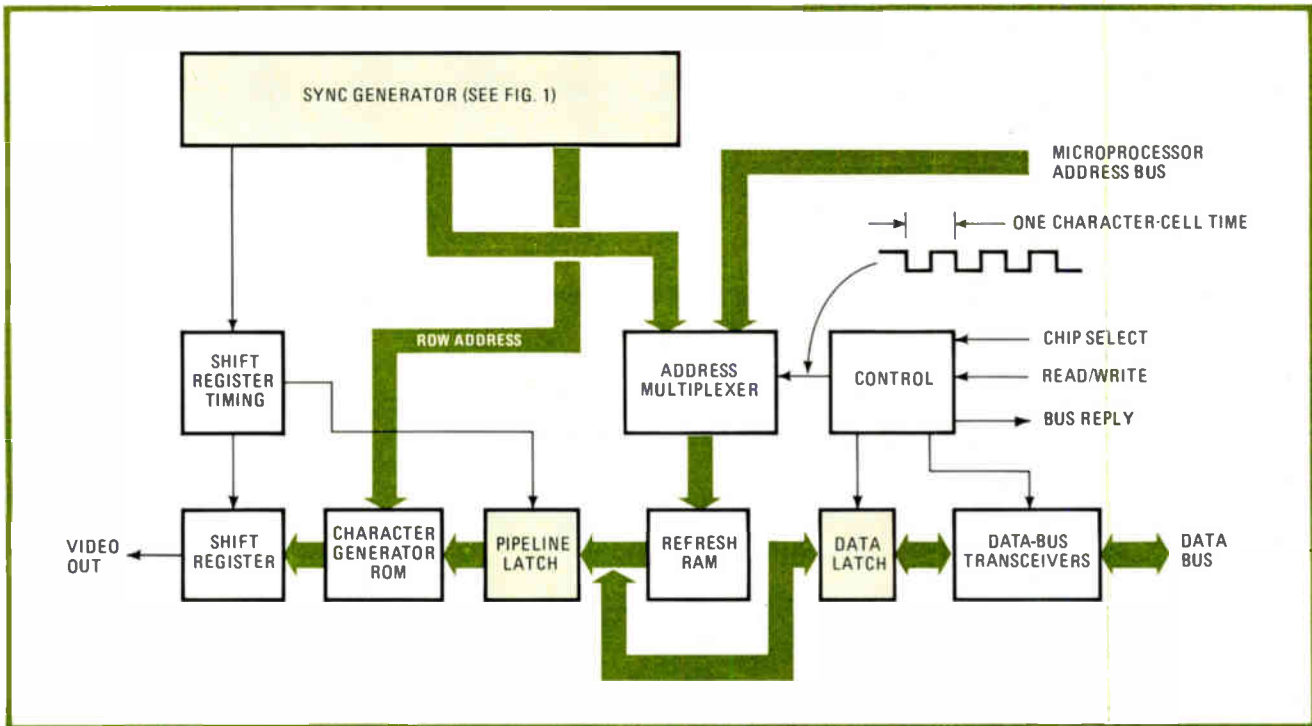
The column address of the refresh memory is controlled by the character-cell counter. On each horizontal line, a different slice of the same set of characters is scanned, and only the row-input addresses of the character-generator ROM change. When the character-row counter resets, the character-line counter can be interpreted as the row address of the page memory, because when the character-line counter is incremented, the electron beam starts to slice through another set of characters on a new line.

Time pressures

When a large number of characters is displayed per line (more than 48, for instance), memory speed is important. The greater the number of characters, the faster the dot clock and the higher the video bandwidth. Also, the time available to look up the ASCII-character code in the refresh memory and the character slice in the ROM becomes smaller.

The time available for such functions is known as the cell time. This is fixed by the time, in microseconds, of a line scan divided by the number of characters per line. In a pipelined organization, however, like that depicted in Fig. 2, cell time is reduced to the access time of either the refresh memory or the ROM, whichever is longer, rather than the sum of the two.

With the video-RAM approach, refresh-memory interfacing is simplest to implement and in fact is the basis for the transparent-memory design. Access to the refresh-memory address lines is controlled by a two-input multiplexer (refer to Fig. 1 again), thus allowing the memory to be switched between the sync-generator outputs and a microprocessor's address bus. The switch-



4. Transparent memory. The problems inherent in both the video-RAM and the DMA approach are neatly solved with the transparent-memory concept. The screen is never garbled and the CPU can run at top speed. The penalty is cost: a little extra, faster RAM is required.

ing is controlled by a single address line from the microprocessor, used as a chip-select signal. The memory data bus can also be connected to the microprocessor's data bus via three-state transceivers. The transceivers are, in turn, controlled by the microprocessor's read, write, and chip-select lines.

When the chip-select line is activated, the external system can take control of the RAM. This organization creates a display that looks like a RAM (hence the name video RAM) to the outside computer. Each character position on the screen corresponds to a particular memory location. This allows the designer to use the full instruction set of a microprocessor for purposes of display data manipulation.

With direct memory access, the refresh memory is part of the computer system's memory (Fig. 3). But this scheme, too, has pitfalls. The microprocessor is interrupted by refreshing of the screen, and when the display controller accesses the memory to refresh the data, it forces the microprocessor to relinquish control of the address and data buses to the DMA controller. The controller transfers information from the RAM to CRT buffer memory, which is read out by the sync generator and put on the screen.

While this method eliminates the interference problem of the video RAM, it is more complex and expensive to implement. In addition, when a DMA occurs, the processor must stop, slowing down any other CPU activities.

The transparent memory design, shown in Fig. 4, neatly solves all of the problems encountered with the VRAM and DMA methods. Though similar to the video-RAM interface, the memory is regularly and systematically made available to both the microprocessor and the sync generator.

The signal controlling the address-multiplexer switching is connected to a square wave derived from the sync generator dot counter, as shown in the figure. Each square-wave period equals one character-cell time, and during the second half of each cycle the RAM is connected to the sync generator address lines. RAM speed must be faster than half a cell time. During this same half cell time, the next character to be displayed is transferred from the RAM and stored in the pipeline latch.

The transparent memory schedule

During the first half of the character-cell time, the RAM is connected to the microprocessor address bus. It is during this time frame that data transfers from the microprocessor can occur. Write operations are straightforward, provided that the microprocessor holds the data stable on the data bus throughout the required half cell time. For read operations, a data latch must be added to retain the memory data longer than the half cell time during which it is available. The only requirement of the microprocessor is that it must have some form of wait or bus reply control line so that data transfers can be synchronized for the next available cell time. With 80 characters per line, this waiting time is equivalent to an access time of only 500 ns.

Because of its more complex multiplexing, transparent memory requires two to four more small- or medium-scale integrated TTL packages than does a standard video-RAM design. Also, the memory must be twice as fast as that used in the video RAM. In return for these modest penalties, the method elegantly solves the classic memory-contention problem. Moreover, the display is memory-mapped, which allows the CPU to use its full instruction set for display-data manipulation. □

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Three-line multiplexing cuts pin count of complex LCDs

Liquid-crystal displays with over 30 segments benefit from technique that cuts number of control lines by more than half

by Lynn T. Rees, *Motorola Inc., Government Electronics Division, Scottsdale, Ariz.*

□ Designers are finding many more uses for liquid-crystal displays than in digital watches and pocket calculators. Evolutionary developments are making these power-frugal, easy-to-read devices attractive for a wide variety of applications. But in cases where more than three or four display digits are called for, multiplexing schemes that drastically reduce the number of control leads needed by a liquid-crystal display (LCD) may be essential.






Two-line multiplexing [*Electronics*, May 25, 1978, p. 113] can cut the number of control leads approximately in half, but three-line multiplexing—often referred to as V/3 multiplexing—goes even further. For example, an eight-digit numerical display with each segment individually driven would require an integrated-

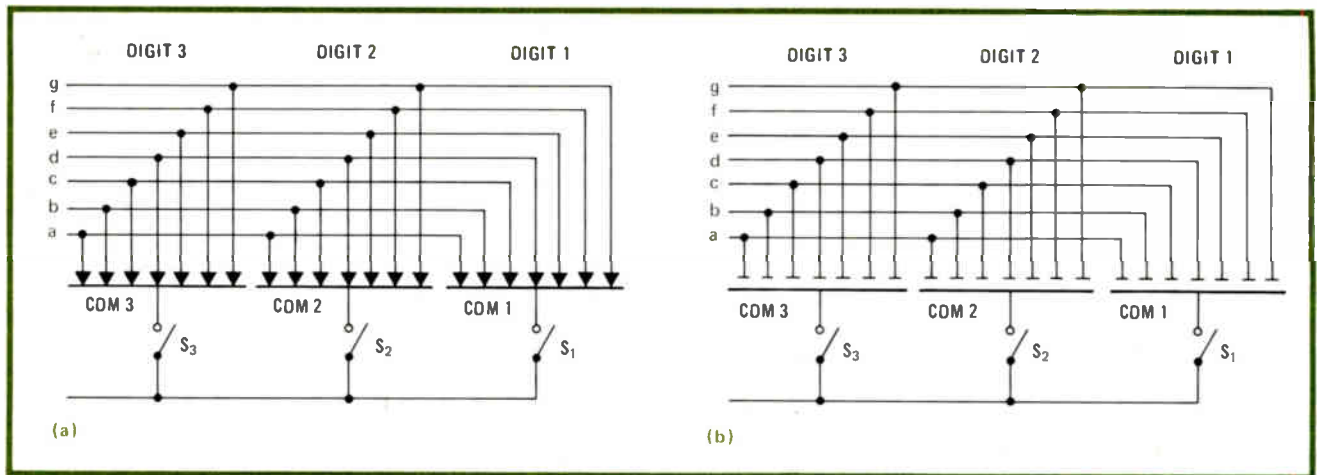
circuit driver with as many as 67 leads. This number of input/output pins is feasible, but may drive costs beyond acceptable limits. Three-line multiplexing can cut the number of required leads to 28. This reduces package size, lowers cost, and frees up chip leads for other functions. Table 1 lists lead requirements for various displays when they are unmultiplexed, two-line multiplexed, and three-line multiplexed.

How it works

The characteristics of LCDs make them somewhat more difficult to multiplex than light-emitting-diode (LED) displays. LCDs are sensitive to voltage, rather than current; hence they respond equally well to positive and negative signals. However, they must be driven by alter-

TABLE 1: LCD LEAD COUNT COMPARISON

Display	Individual segment drive	Two line multiplex	Three line multiplex
Two digits plus two annunciators 	19	11	10
3½ digits plus two annunciators 	29	16	14
4½ digits plus two annunciators 	37	20	17
6 digits plus two annunciators 	52	28	23
8 digits plus two annunciators 	67	33	28



1. LEDs and LCDs. The self-isolation of common-anode light-emitting diodes (a) makes simple multiplexing possible. The same circuit fails with a liquid-crystal display: capacitor-like segments (b) pass ac drive signals to common connection, activating wrong segments.

nating current and therefore cannot use diodes for isolation purposes. Furthermore, the optical threshold voltage varies with the viewing angle: at a given voltage, a display may appear to be off when viewed head on, yet be very visible when viewed from an angle.

The self-isolating characteristics of LEDs allow very simple multiplexing schemes to be used, schemes that do not work with LCDs. Figure 1a illustrates the common method of multiplexing a three-digit, seven-segment LED display. All drive signals are positive. No segment can light until one of the switches (S_1 , S_2 , or S_3) closes because the diodes block the current flow. When S_1 closes, the data on lines a-g activates digit 1 of the display; S_2 closes when the data on a-g is for digit 2, and likewise for S_3 .

Figure 1b depicts the same multiplexing scheme for a three-digit, seven-segment LCD. This circuit fails because each segment of each digit acts as a capacitor instead of a diode. The ac signals coming through on lines a-g couple through the segments to the common connection, causing segments in neighboring digits to turn on partially, regardless of switch positions.

The only way to selectively address LCD segments is through amplitude selection on a time-synchronized basis. This is accomplished by replacing each switch in Fig. 1b with a single line carrying its own continuous amplitude-varying waveform. In addition, the digital signals on lines a-g are exchanged for appropriate amplitude-varying waveforms.

Figure 2a depicts such a set of signals. The voltage across a segment is the difference between the voltage of the common-line signal and the voltage of the segment signal (Fig. 2b). As can be seen, the shape of the common waveforms in this three-line multiplexing circuit allow activated (selected) segments to be driven above threshold voltage only one third of the time. But an LCD responds to rms voltage rather than peak voltage, in normal usage. If V , the peak voltage, is 3 volts, then the rms value of the voltage across a segment is 1.91 V when it is on, and 1.0 V when it is off (see "V/3 multiplexing math," p. 144).

Note in Fig. 2 that the peak non-select voltage is one third the peak select voltage; thus the term V/3 multi-

plexing. But the ratio of select to non-select rms voltages is only 1.91:1, not 3:1 as one might infer from the term V/3. The maximum ratio of V_{on} to V_{off} (rms values) depends upon the multiplexing technique used.

This ratio is an important variable in optimizing a multiplexed LCD application. It impinges directly upon the relationship between the LCD's electro-optical response and the direction from which the display is viewed. Other variables that must be considered are the temperature range over which the LCD must be read without ambiguity, the response time required for updating the display, the supply voltage range, and the temperature coefficient of the supply.

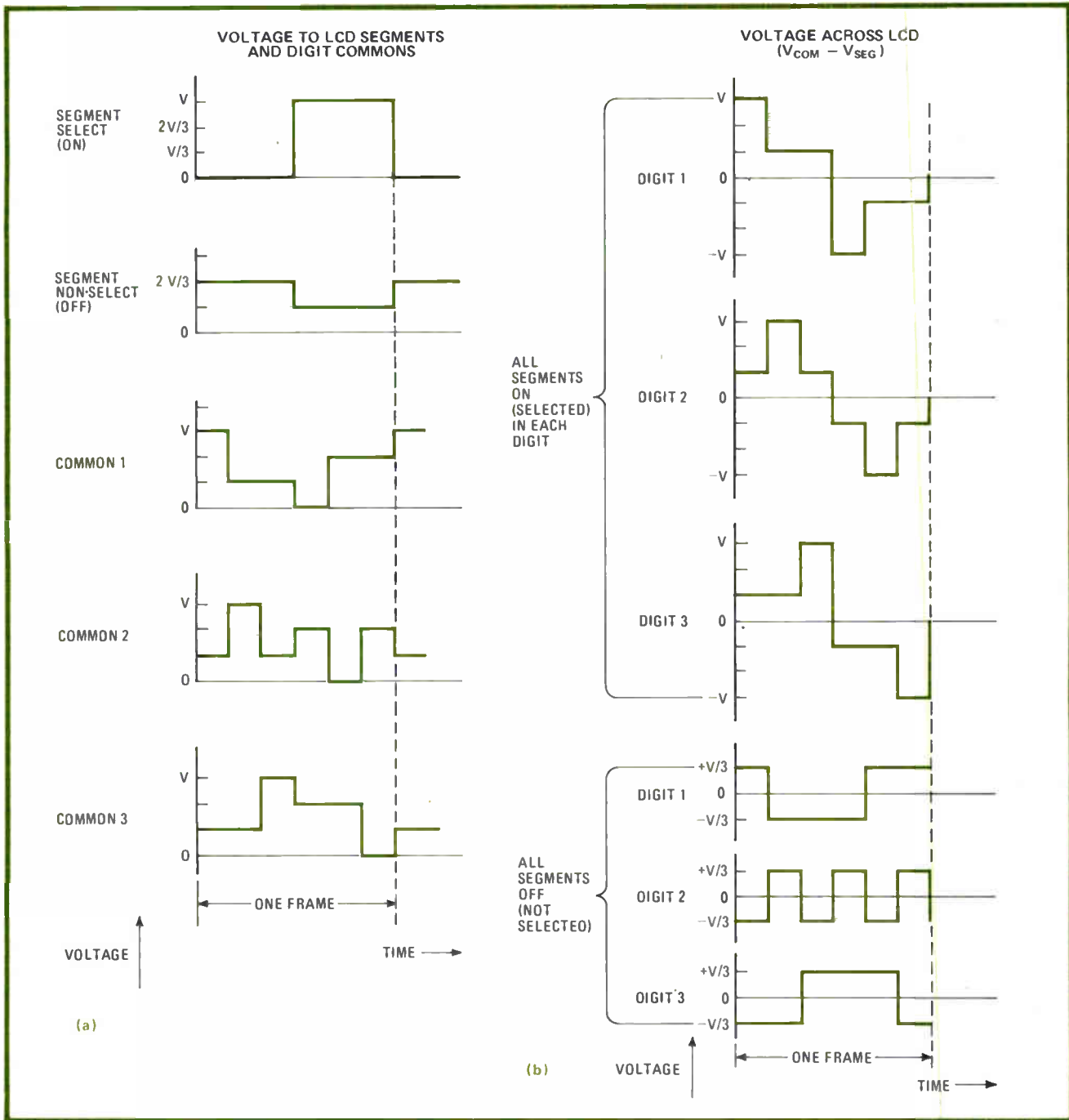
Electro-optical response

A liquid-crystal display is readable because of visual contrast between the activated segments and the background (including deactivated segments). Figure 3 is a simplified plot illustrating LCD contrast ratio vs. rms drive voltage. Note that both curves have a threshold point. If the drive voltage is kept below this point, the segment will appear to be off even though drive voltage is present. Curve A applies when one is viewing the display along the axis normal to its surface (normal axis viewing). Curve B applies when viewing the display from an angle (off-axis viewing). Note that the threshold point shifts: the display will turn on at a lower voltage when viewed from an angle than when viewed along the normal axis.

A V_{on} -to- V_{off} ratio of 1.91 is all that is achievable with V/3 multiplexing. In Fig. 3 it can be seen that although a 2.1 ratio is optimum, a 1.91 ratio will produce near-optimum performance.

Liquid crystal materials synthesized for different purposes respond at different operating voltages. All presently available LC materials would perform better with V_{on}/V_{off} greater than 1.91. V/3 multiplexing makes it especially important that the drive circuit supply a precise voltage, and that this voltage respond properly to temperature changes if the application so requires.

A supply voltage tolerance of $\pm 1\%$ at room temperature is highly recommended. The V/3 and 2V/3 voltages should be within ± 50 mv of their theoretical value



2. Signal subtraction. The waveform on each common line repeats itself in each new frame; display data arrives as on or off waveforms on segment-select lines (a). The voltage across a segment is the difference between its common and segment-select voltages (b).

(± 25 mV is recommended). Typically, the supply voltage will be between 3 and 8 v dc, depending upon the liquid crystal compound used.

When multiplexing LCDs, care should also be taken to compensate for adverse temperature coefficients. LCDs typically have a negative temperature coefficient of 10 mV/ $^{\circ}$ C for the curve of Fig. 3. Since a drive of 1.91 v rms puts operation on the sloping portion of the response curve, small voltage changes make a big difference. Operating the device over a temperature range of 50 $^{\circ}$ C would shift the curves by 0.5 volt. At 0 $^{\circ}$ C the display would only be 75% on, and at 50 $^{\circ}$ C it would not turn

completely off. Temperature compensation is clearly required. This is easily accomplished for wide-temperature applications. One simple solution is to use a supply voltage which tracks the LCD temperature curve.

In addition, LCD updating response slows down at low temperatures. When a character changes, the readability will be governed by the slowest event, which is usually the deactivation of previously activated segments. The maximum update rate and the minimum operating temperature are therefore interdependent. For example, a given liquid crystal material may operate satisfactorily at 10 $^{\circ}$ C with updating intervals of 1 second and just as

V/3 multiplexing math

The ratio of V_{on} to V_{off} is a critical factor in a multiplexed liquid-crystal display drive circuit: it is closely tied to the contrast ratio which makes the display visible (Fig. 3). For V/3 multiplexing that uses the waveforms shown in Fig. 2 (assuming a 33 1/3% duty cycle), the ratio of V_{on} to V_{off} may be derived as follows, where:

V = the peak voltage across a selected (on) segment
 V_{on} = rms voltage across a selected segment
 V_{off} = rms voltage across a non-selected segment

From any of the V_{off} waveforms in Fig. 2, it can be seen that the absolute value of the voltage at all points is $V/3$. Therefore the rms voltage V_{off} equals $V/3$.

The V_{on} waveforms are all symmetrical about the midpoint of a frame. Therefore the rms value of the first half is equal to that of the second half. One third of the time the voltage equals V ; two-thirds of the time the voltage is $V/3$. Thus the rms value of the waveform can be expressed as:

$$V_{on} = \left\{ \left(\frac{1}{3} \right) [1(V)^2 + 2(V/3)^2] \right\}^{1/2}$$

$$= \left[(V^2/3)(1 + 2/9) \right]^{1/2} = \left[(V^2/3)(11/9) \right]^{1/2}$$

$$= (V/3)(11/3)^{1/2} = 1.91(V/3) = 0.638(V)$$

Therefore $V_{on}/V_{off} = [1.91(V/3)]/(V/3) = 1.91$

For a general case of the V/3 drive scheme with n elements, a duty cycle of $1/n$, frame period T , and activated period T/n :

$$V_{off} = \left[(1/T)(V/3)^2(T) \right]^{1/2} = V/3 \quad \text{and,}$$

$$V_{on} = \left(\frac{1}{T} [V^2(T/n) + (V/3)^2(n-1)(T/n)] \right)^{1/2}$$

$$= V \left[(1/n) + (n-1)/(9n) \right]^{1/2} = (V/3) \left[(8+n)/n \right]^{1/2}$$

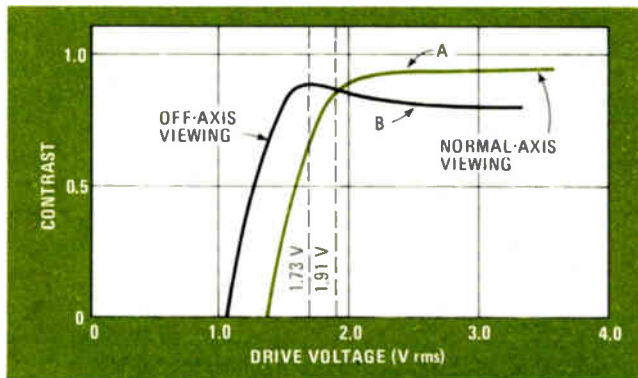
Therefore:

$$V_{on}/V_{off} = \left[(V/3) \left[(8+n)/n \right]^{1/2} \right] / (V/3)$$

$$= \left[(8+n)/n \right]^{1/2}$$

The value of V_{on}/V_{off} for V/3 multiplexing with various numbers of multiplexed elements (n) are:

n	2	3	4	7	9	14
V_{on}/V_{off}	2.24	1.91	1.73	1.46	1.37	1.25



3. Contrast response. The visual difference between a typical LCD segment and the background varies with applied voltage. Viewing head on yields curve A; lower voltages produce contrast visible from some angles. Curve B represents the most sensitive viewing angle.

well at 0°C with updating intervals of 2 seconds.

The manner in which LCDs are partitioned also dictates the multiplexing method implemented. Partitioning like that shown in Fig. 1 is satisfactory for two or three digits. This method becomes cumbersome, however, for more than three digits or when the digits are small (1/4-inch high). Consequently it is often more convenient to rearrange the LCD to multiplex by line instead of by digit.

Partitioning by line

In this technique, one line is made up of all the top sections of the digits, another of all the middle sections, and another of all the bottom sections. The three common lines extend the full length of the back plane of the LCD, and they are V/3-multiplexed. Drive voltages remain the same. Segment-select signals are supplied to all digits simultaneously, in synchronism with the common lines on the back plane. Three segment-select lines per digit on the front plane are required, yielding a

total of 27 input lines for an eight-digit display.

This method will drive a nine-segment character. A seven-segment display becomes eight segments when decimal points are included, leaving one segment unused. One possibility for the extra segment is an underscore line which would denote letters instead of numerals, allowing hexadecimal information to be displayed in microcomputer-based displays.

Multiplexed analog displays

These multiplexing schemes make analog LCD displays far more practical. Lead count is still high, but because the drive currents and voltages are so low, a single complementary-MOS integrated circuit can still drive a large number of elements. For example, a 60-lead IC can drive a 100-segment analog display using serial data input. This would make an attractive analog read-out for microprocessor-based systems. Sixty-lead ICs are very practical, evidenced by their profusion in low-cost hand-held calculators. LCD analog displays are readily achievable in either linear or circular shapes because of the relatively simple manufacturing process—so long as the outside shape of the display remains either rectangular or square.

Two-line (50% duty cycle) multiplexing, though it doesn't save as many leads, has a V_{on}/V_{off} ratio of 2.41. This extra voltage can be traded off for better display performance, looser tolerances in the display and its drive circuitry, wider temperature range, etc. Consequently, there are many applications—industrial, automotive, and in instruments—where two-line multiplexing should be considered because it still saves a significant number of leads. The voltage ratios are not the same as in V/3 multiplexing, but they are also compatible with C-MOS ICs. Temperature compensation is still necessary for most applications. Using a silicon diode may suffice, since it exhibits the correct temperature coefficient for many liquid crystal materials. □

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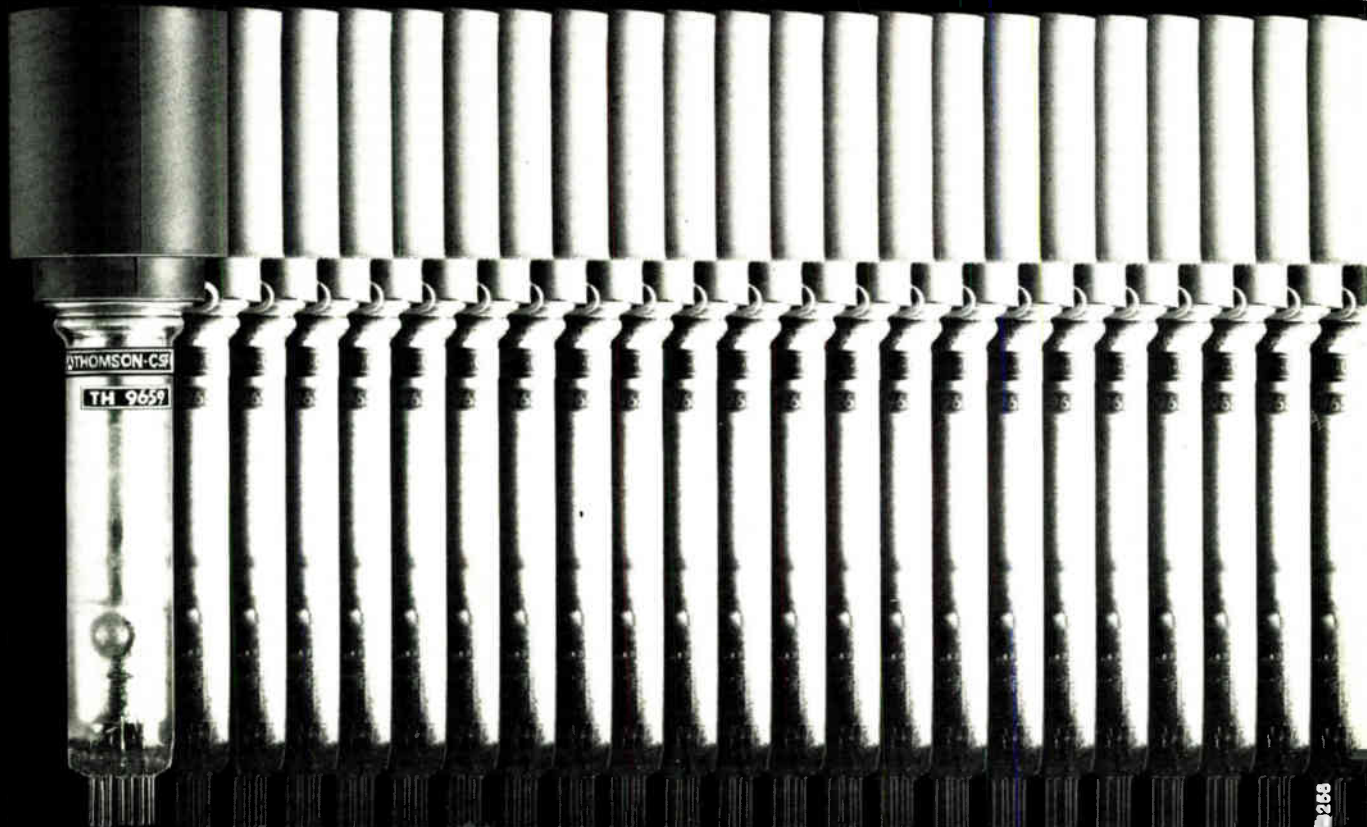
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Digital phase meter displays angles in degrees or radians

by Tagore J. John
Meerut, Uttar Pradesh, India

In this unit, the phase angle between two signals is measured and displayed digitally, and so the instrument is less costly than its counterparts that use precision linear circuits and expensive meter movements. The angle can be displayed in degrees, radians, or grads (400 grads = 360°). The accuracy of the instrument is ± 1 least significant count, independent of signal differences in amplitude or wave shape.

Generally, the reference and test signals are applied to channel A and channel B, respectively, as shown in the figure. Q_1 and Q_2 generate short pulses (i.e. less than 30 microseconds) to the counting logic as each signal passes upward through its zero-crossing point. To initiate the counting cycle, the logic circuit simply gates the output of an oscillator through to the 74192 counters on the

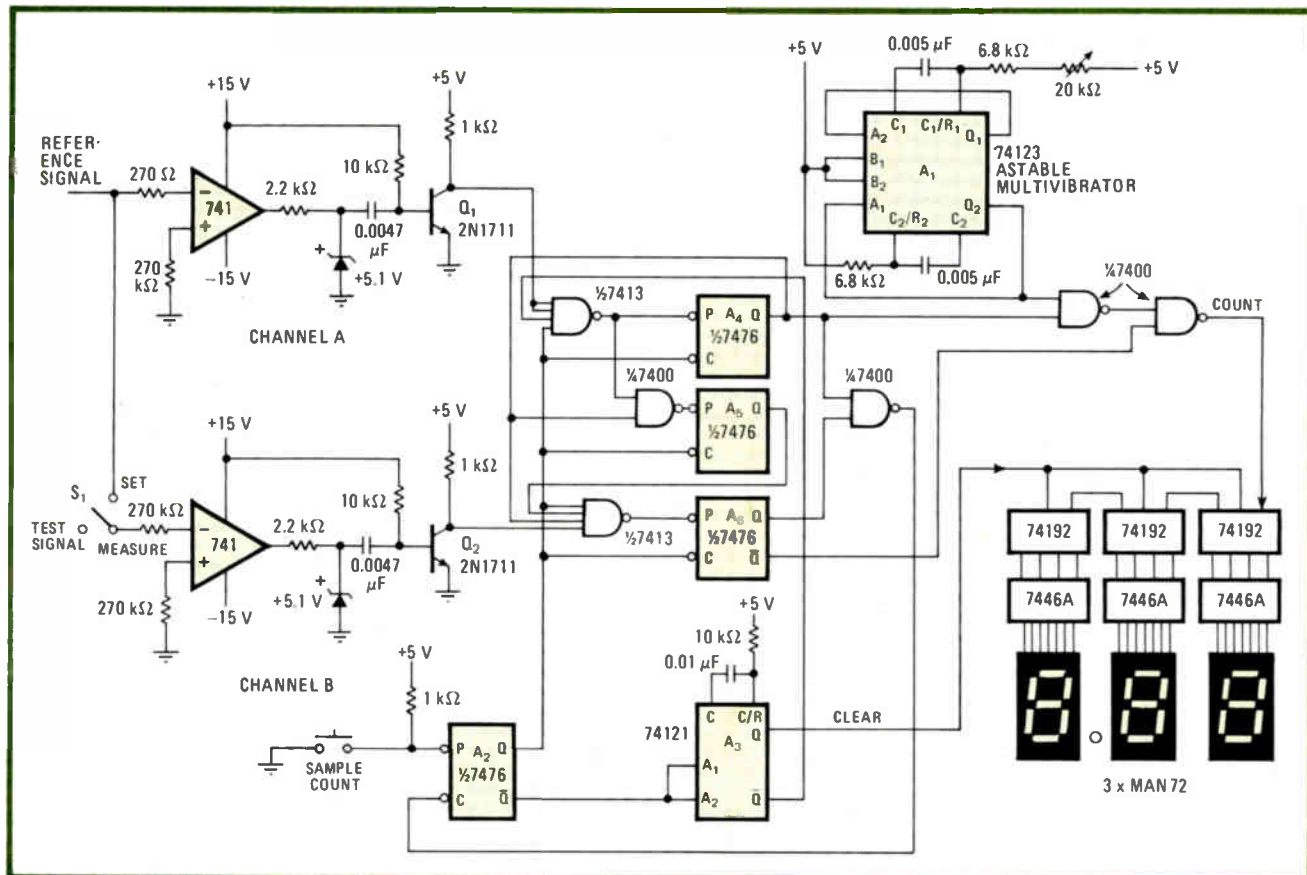
first zero-crossing pulse from Q_1 . The zero-crossing pulse from Q_2 terminates the count. The number displayed thus represents the phase difference expressed in the desired units, provided A_1 's frequency is appropriately selected.

The instrument is calibrated by placing S_1 in the set position, introducing a reference signal, and depressing the sample-count push button as A_1 is adjusted for a display output of 360 (if output in degrees is desired), 400 (in grads), or 628 (in radians).

In normal operation, depressing the sample-count push button initiates the count cycle. Flip-flop A_2 is preset and fires one-shot A_3 , whereupon the display is cleared.

Q_1 's first pulse sets flip-flops A_4 and A_5 and gates A_1 's output through to the 74192 counters. With a pulse from Q_2 , flip-flop A_6 is set, and the output of the NAND gate driving the counters is disabled. Meanwhile, A_2 is cleared in order that the unit may then be readied for a new sample count.

The phase angles will be displayed directly. Provision should be made, however, for activating the decimal point to the right of the left-most digit when radians are displayed. □



Digital differential. Phase angle between two signals is determined to within ± 1 least significant count. Using standard chips, angle is digitally measured and can be displayed in degrees, radians, or grads, provided frequency of counting oscillator, A_1 , is appropriately selected.

Single-step exerciser aids 8085 debugging

by Scott Nintzel
 Medtronic Inc., Minneapolis, Minn.

The ability to step through a microprocessor-based program is a virtual necessity during its debug and test phases. But certain processors, such as the 8085, require a minimum input frequency of 1 megahertz, so that stepping cannot be achieved merely by using a clock whose frequency corresponds to the rate at which the user wishes to move through the program. With two flip-flops, some logic, and a simple switch arrangement, however, single-stepping can be carried through without disturbing the basic operation of the processor.

Every 8085 instruction requires at least one machine cycle, each of which in turn consists of several parts known as T states. The first cycle of each instruction is referred to as the op code fetch cycle. Single-step operation can be attained by adding an integral number of waiting cycles or T_{wait} states to the op code fetch cycle with the single-step circuitry.

Operation is clarified in the figure and the timing

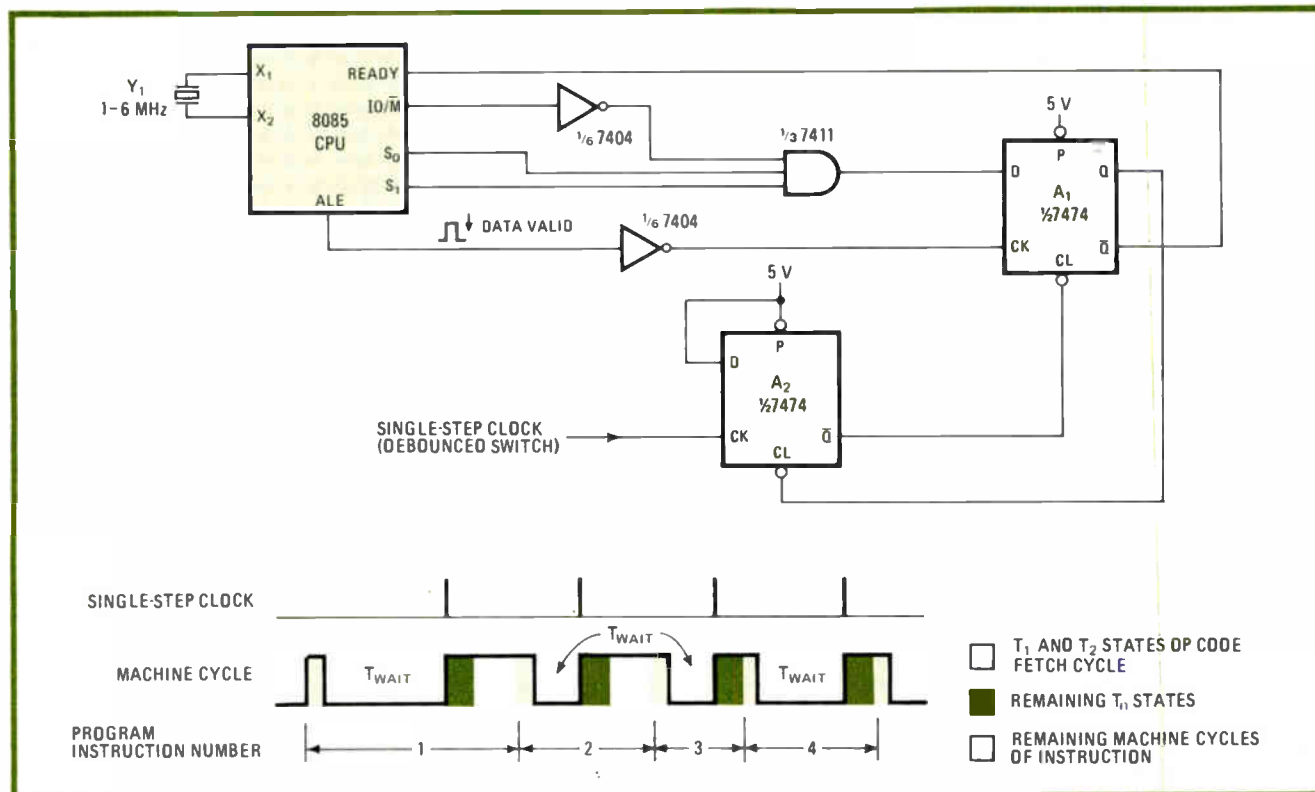
diagram. Immediately after a system reset, the central processing unit of the 8085 processes the first program instruction through state T_2 of the op code fetch. The address-latch enable (ALE) line then moves low.

Lines IO/\overline{M} , S_0 , and S_1 of the CPU are examined at this time. Because the 8085 is in the fetch portion of the cycle, IO/\overline{M} will be low and S_0-S_1 will be high, so flip-flop A_1 will be set. Thus the CPU's ready line will be brought low, and the 8085 will enter the wait state. Therefore, in the initial case, instruction 1 of the program will not be completed until a single-step command is received.

Then, A_2 clears A_1 , the ready line is brought high, and the remaining T_n states and machine cycles are executed, as are the T_1 and T_2 states of the next instruction cycle. At this time, the machine reenters the T_{wait} state and remains there until cleared, as discussed previously.

A debounced switch or slow-running clock made from gates can be used to generate the single-step command, and total chip count for the unit should not exceed three ICs. Note that A_2 is required to ensure that A_1 clears quickly enough to allow capture of the subsequent fetch cycle. Without A_2 , the pulse width of the single-step clock might be too long, and disturb the setting of A_1 . □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay \$50 for each item published.



Walking through. Simple single-step controller for debugging 8085 routines places CPU in wait state between program instructions. Processor is made to execute last part of one instruction and first part of next before halting, thereby advancing one location at a time.

Electronic sink simulates load for testing power supplies

by Henry Santana
Hewlett Packard Co., Loveland Instrument Division, Loveland, Colo.

The bank of bulky, high-power load resistors normally required to check the current-delivery capability of various power supplies can be eliminated by this programmable load. Able to simulate an equivalent resistance as low as a few milliohms and handle input powers up to 50 watts, this compact unit, which uses operational amplifiers and transistors to limit the amount of current it will sink, serves as a good general-purpose device for production-line testing. It can be built for \$40.

The idea behind the circuit is explained with the aid of (a). Neglecting the on-resistance of transistor Q_1 , and considering that a virtual ground exists between the inverting and noninverting inputs of operational amplifier A_1 :

$$V_1 = V_{in} = K\alpha V_2 \quad 0 < \alpha < 1 \quad (1)$$

where K represents the gain of A_2 , α is selected by a

potentiometer, and V_2 is a floating supply required to maintain the necessary bias on the control transistor. Also note that $V_2 = I_{in}R_a$. When this expression is substituted in Eq. 1, it is seen that:

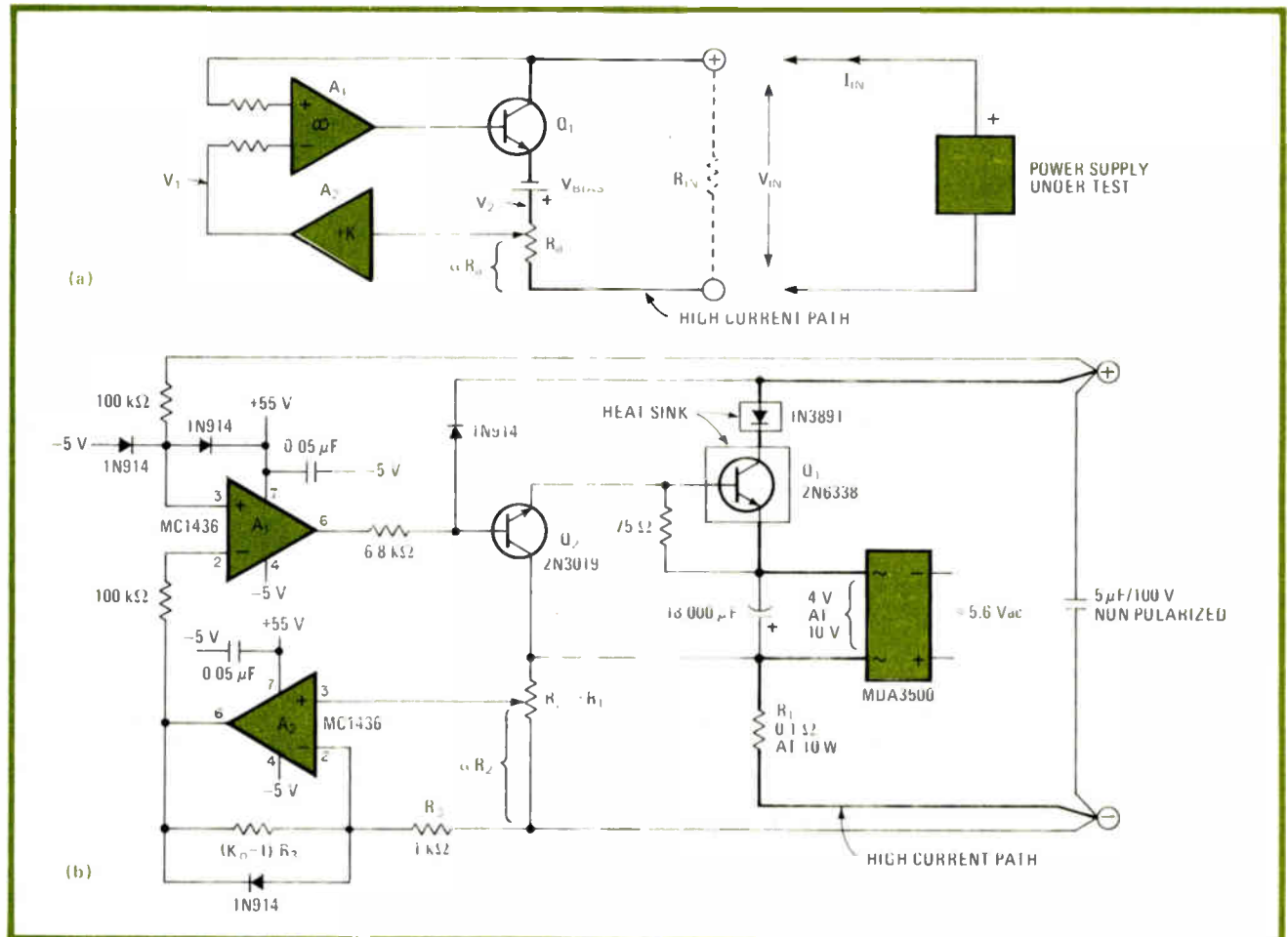
$$R_{in} = V_{in}/I_{in} = K\alpha R_a \quad (2)$$

and therefore the resistance seen by the power supply under test can be set by R_a .

The circuit required to implement the idealized configuration is shown in (b). High-voltage op amps are used for A_1 and A_2 to handle the large input potentials expected. Q_2 has been added in order to supply adequate drive current to the output (control) transistor. R_a in (a) is represented by R_1 and R_2 in (b), where the value of R_1 is made small in order to minimize the voltage (V_2) needed to bias the control transistor.

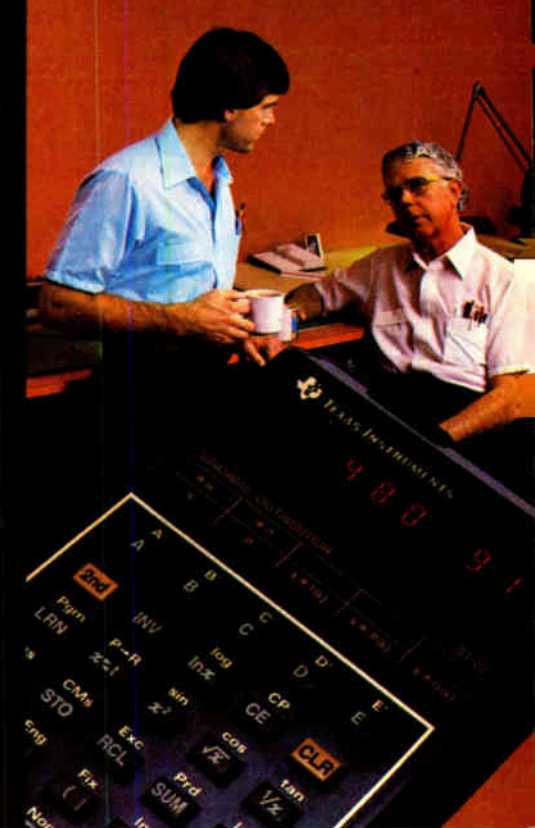
If the gain of A_2 is selected for $K = 500$, R_{in} can be made to vary from approximately 0 to 50 ohms. If R_2 can be selected digitally, any resistor value in this range can be automatically ordered up. The unit can withstand a maximum input voltage of 50 volts and input currents up to 10 amperes, though the maximum input power cannot exceed 50 watts, as mentioned previously.

The components in the path of high current should be mounted on suitable heat sinks, for the power dissipated is approximately $P_d = (5 + V_{in})I_{in}$. □



Equivalent resistor. Suitably configured op amp and power transistor combination (a) will function as a programmable electronic load. Practical implementation of idealized circuit is shown in (b). Unit handles a maximum power input of 50 watts.

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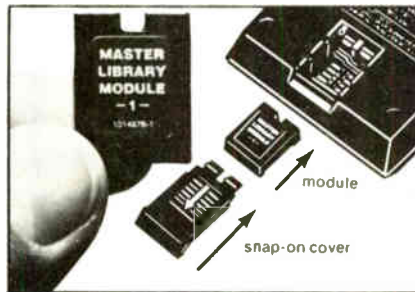
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Antenna group to exchange measurement ideas

The recently formed Antenna Measurement Techniques Association aims to bring together people from Government and industry who are interested in advancing the art of antenna evaluation. According to Joe Pape of Scientific-Atlanta Inc., Atlanta, Ga., the nonprofit organization "will serve as a forum for the interchange of information on the applications of advanced measurement techniques, antenna range design, measurement equipment, and the system-equipment interface." In the works is a **software pool that will be available to all members to assist them in developing programming for automatic systems.**

Meetings are to be held every six months, the first being scheduled for Oct. 17 and 18 in Atlanta. Anyone interested in becoming a member should write to Pape at 3845 Pleasantdale Rd., Atlanta, Ga. 30340, or call him at (404) 449-2354.

Resistor stabilizes gain of monolithic d-a converter

When a digital-to-analog converter having an R-2R ladder network must provide voltage multiplication of greater than 1, the gain is usually obtained by connecting a resistive-divider type of attenuator between an op amp at the converter's output and the converter's feedback resistor. But as Paul Brokaw of Analog Devices Inc. has found, there are several drawbacks to this approach. It makes the overall gain sensitive to the feedback resistance, and it causes gain drift because the divider's temperature coefficient does not match the monolithic device's. **Usually, too, gain must be adjusted over a wide range in standard applications** because the absolute value of the ladder resistors in the d-a converter vary significantly, although the R-2R ratios are very accurate.

But Brokaw, who is manager of Advanced Product Planning for the Norwood, Mass., firm's Semiconductor division, says that fortunately all the problems can be eliminated—you simply add a single compensating resistor in series with the analog reference source driving the converter. The resistor must have the value $R_1 R_2 / (R_1 + R_2)$, where R_1 is the part of the divider closest to the op amp, and its tempco should match the divider's. **Under these conditions, the converter's feedback resistor will not affect the gain**, which thus becomes $(R_1 + R_2) / R_2$, assuming the series resistance of the network is not substantially larger than the nominal value of the d-a's feedback resistance.

Classic databook of dielectric properties makes a comeback

The generations of microwave engineers who grew up with Emerson and Cuming Inc.'s classic guide to the properties of materials at microwave frequencies—the Dielectric Materials Chart—will be happy to know that it is being offered again. Newcomers to the microwave field will also welcome the chart, which plots **the dielectric constant versus dissipation factor (loss tangent) of more than 140 substances**, including plastic and ceramic foams, resins, and rod and sheet stock, as well as other artificial dielectric materials.

In addition, the chart contains a section on definitions that relate such variables as permittivity, index of refraction, loss factor, and wave impedance to the dielectric constant. The 11-color chart may be hung on the wall or folded and inserted in a standard notebook. For a free copy, write to the company, Canton, Mass. 02021.

-Vincent Biancomano

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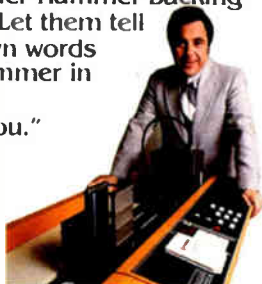
"A big thing is happening in the semiconductor equipment industry. Cutler-Hammer has put its resources behind the six companies that now make up the Cutler-Hammer group.

"In 1977 there were 800 equipment companies serving an \$800 million market. It's tough for our customers to do business with that many companies. In 5 years, our industry will have fewer, but larger suppliers. The nature of our business demands it. Our customers want it. And this consolidation is possibly the only way sufficient investment can be made to develop the products of the 80's.

"Cutler-Hammer provides more than money, facilities and equipment to our group. *It provides long-term commitment to the industry.* At the same time it seeks to maintain the individuality of each company. Ours is an innovative business. Our growth rests on the creativity of each company. Now those companies can concentrate on what they do best, and not have to devote their major energies to survival.

"Other companies in the Cutler-Hammer group have benefited from Cutler-Hammer backing in other ways. Let them tell you in their own words why Cutler-Hammer in their names is important to you."

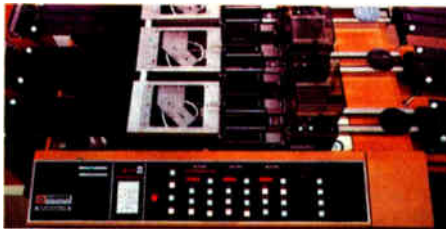
Ralph Miller, President, Kasper Instruments:



"At Kasper Instruments, the resources of Cutler-Hammer have let us strengthen our service and marketing teams, both for our own

products and for those of the other companies in the group whose products are natural partners with our own.

"We have also been able to put intensive development work into our major product lines. The Kasper wafer processing System 4000 now features microprocessor



control at each station, so the customer can choose either local microprocessor control at the station level, or centralized remote supervision and programming. The beginning of a System 4000 installation can be as limited as one stand-alone station or can be expanded to any complexity.

"Our Challenger 200 mid-current ion implanter, which is the standard of the industry, is available with a process parameter printout that records energy, dose, species, beam current and vacuum from actual system operation, as well as time, date, lot number and size, and wafer size.

"The Kasper 2001 Mask Aligner is established as the workhorse of the industry. It offers the highest standards of precision on wafers up to and including 4" diameter, in either manual or automatic mode."



Jack Salvador, President, Macrodata:

"The biggest leverage Cutler-Hammer has provided us is financial stability. Great as it is, the cost of product development is probably less than the cost of building a world-wide marketing and service organization. Because of the high rate of change of the technology, we must maintain a very high expenditure in the development of

our test systems. Before Cutler-Hammer provided the backing we needed, we had a difficult time maintaining the level of service our customers needed. Without Cutler-Hammer, we might not have survived.

"Yet we've always been leaders in test technology. Now we've leap-frogged the field with our M-1, the industry's first 25-MHz Memory Test System. And with Cutler-Hammer's support, we know the M-1 is just the first of a whole new generation of test systems.



"The area of cooperation within the Cutler-Hammer group provides an unusual sort of benefit for our customers as well as ourselves. Kasper is now putting microprocessors into various stations on the production line. We pioneered the general strategy of a central computer with a large number of testers. The feedback necessary in any closed loop system predominantly comes from test stations in a semicon production line. Now, as customers start to tie everything back into a central control system, they find that between Kasper and Macrodata we can provide a consistent, standard protocol to implement their control programming."

Shelley Detrick, President, Davis & Wilder Industries:



"We've only been a member of the Cutler-Hammer group since

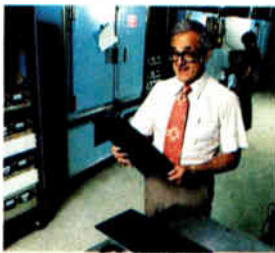
last September and we're already selling our plasma etchers and split-chamber vacuum coating systems at a rate 200% above last year.

"There are three reasons, really... most important, now we can serve big companies who were afraid we couldn't handle big orders. The second reason, Cutler-Hammer provided the working capital to really increase production. And just as important, we now have the advantage of Kasper's world-wide marketing and service organization.

"Now our customers know we can provide fast service on the east coast, for instance, where before we couldn't.

"Since we became a part of the Cutler-Hammer group, we've really been able to move our new Model 335 Plasma Etcher. It's revolutionizing plasma etching. It provides unheard-of selectivity, with stop ratios of 15:1, 20:1, 25:1 where competitive equipment has ratios of 5:1, 8:1, 10:1. And it attacks photoresist less than any other etcher, and perhaps most important, it has a much bigger capacity than other units. We can etch 35 wafers at a time at exceptionally high etch rates. That's productivity, and that's the name of the game."

Eli Goldfarb,
President,
Pacific
Reliability
Corp.



"The backing of Cutler-Hammer has allowed us to plan expansion on a more timely

accelerated basis without changing the way we operate. The sort of complete, top-level testing services that we offer is extremely costly to implement.

"We constantly try to stay at the forefront of the testing technology. We have DESC Certification and are equipped for MIL-STD screening not only because we do screening to government requirements but because this level of performance makes certain we can meet most customers' requirements with our normal operating procedures.

"With the ever increasing costs and other ramifications incurred by in-house as well as field failures, it is more important for manufacturers to screen out faulty units before assembly and shipping. The rapid growth in complexity of semiconductor devices requires access to technology as well as modern sophisticated equipment. In addition to our unusually thorough burn-in procedures, we do device characterization, environmental testing, and full electrical testing. We test, data log and provide data analysis for logic, memory, discrete and analog devices. Our experience and fully equipped facilities allow us to work with customers to meet normal and many unusual screening needs.

"The advantages of location within a concentration of device and OEM manufacturers are obvious. With the major portion of our business with semiconductor manufacturers we are able to keep up with the developing technology. With our knowledge and experience and the support of Cutler-Hammer, we can expand in an orderly manner while maintaining our level of performance."



Dr. Peter Rose,
President,
Nova
Associates:

"The impact of an organization of the stature of Cutler-

Hammer on a new company such as Nova is obvious. It immediately gives us substance.

"We may have certain individual reputations that might be appealing to our customers, but they always look beyond to the long-term stability and overall support that a company like Nova can bring to its products. It's a luxury to be a brand-new organization which nevertheless has the resources of a Fortune 500 company.

"It is exciting to be able to concentrate on development of an ion implanter which we believe will be a considerable advance on the state of the art. We expect to have the prototype in operation before the Semicon West show — it will be a low energy, high current implanter which will provide high throughput at high dose levels. In addition to offering marked advantages in production on the semiconductor line, it may also prove cost effective in solar cell production."

Greg Reyes: "In different ways, the support of Cutler-Hammer makes certain the successful future of every company within the Cutler-Hammer group. We foresee tremendous growth for our present members — and we're also looking for potential acquisitions in the months and years to come.

"We believe what is happening with the Cutler-Hammer group is a clear picture of things to come throughout our industry."

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Modular IC tester is easily optimized

Low-cost system may be set up for production testing or engineering characterization of microcomputers, memories, and other LSI devices

by William F. Arnold, San Francisco regional bureau manager

As microcomputers, memories, and other large-scale integration devices become more sophisticated, testing them becomes a tricky and expensive headache. Whether a user employs separate testers for engineering and production or combines those functions into one system, a company can face a bill totaling several hundred thousand dollars.

Now, by applying a modular hardware approach with full software programmability, Megatest Corp. believes that its new Q-II test system family combines testing muscle with low cost for both engineering and production. "The modular feature means that you can buy the tester you want," explains Jeff Hurn, director of marketing services. This means, for example, that to production-test programmable read-only memories a user would only need a \$42,000 Q-II test station and a \$10,000 ROM/PROM/E-PROM execution module.

To perform sophisticated engineering characterization in the development shop, a user only needs to add a \$28,000 Megahost computer to that \$52,000 production-test combination. The Megahost computer module contains a PDP-11/V03 minicomputer, a cathode-ray-tube display and hard-disk storage. Testing random-access memories is similar, using either a Q-II test station and a \$10,000 RAM execution module for production or an additional Megahost computer for engineering development applications.

Testing microcomputers or other complex logic chips requires some more hardware for the logic test system. "A full-blown stored-response, random-logic system costs

about \$104,000," Hurn says, totting up the Q-II test head, a \$4,000 printer, an \$18,000 logic pattern execution module, and a \$40,000 pattern host computer. An enhanced Megahost, the PHC contains a PDP-11/V03 minicomputer with hard-disk storage for 10.5 megabytes.

However, the pattern host computer can play host to up to four Q-II stations, which makes the system the industry's only distributed-host testing network, Hurn declares.

Moreover, the Q-II has the widest range of applications of any available general-purpose tester, Hurn says. To accomplish this, Megatest has taken the traditional stored-program testing method and made these improvements over more ex-

pensive general-purpose systems now on the market: a higher data-transfer rate for more efficient buffer memory overlays (a 4,096-deep-by-96-bit-wide buffer overlay in 4 ms); capacity for longer test sequences of up to 160,000 vectors without accessing the disk; and 24 timing generators, or 48 edges, which allows for testing complex specifications in fewer passes than competitors with limited strobes and clocks, Hurn says. These all increase throughput and vastly reduce programming effort, he says.

On the software side, Megatest employs a high-level, Pascal-based structured test language called QTL-II. All test functions are programmable, including the 48 timing edges, full dc parametrics, and





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New products

the stored and algorithmically generated test sequences.

The high-level software means that measured values can be logged into a central data base from multiple test systems in a straightforward simple syntax, Hurn says. Furthermore, it allows for complex analysis and simple display of test results, including the capability to generate data tables, histograms, and schmo plots so that users can quickly spot yield or detect trends.

"Our design philosophy from the start was that it [the test system] would be an engineering tester also," states Steve Watkins, design engineer. "This way you can take the engineering test programs and take them into production," he says. Also, the Q-II's low cost allows engineers to have more time on the system compared with more expensive competition, Watkins continues. He estimates that engineering cost could be cut to 20% to 30%.

The ROM/PROM/E-PROM module operates at an 8-MHz clock rate and can test up to 8,192-word-by-16-bit or 16,384-word-by-8-bit devices. It can test both standard and edge-activated parts.

The RAM module can test both static and dynamic parts up to 65,536 by 8 bits in capacity. Moreover, the 8-MHz module can handle multiplexed-address devices and all known refreshing schemes. It has 16-bit address generation and 8-bit data generation.

To aid customers who are switching from other test systems, Megatest will support the translation of existing test libraries over to the Q-II, Hurn says. The system is able to execute test patterns written for other systems, after computer-aided conversion, he says. Megatest will also supply free software updates for a year.

The Q-II is a multiprocessor system incorporating separate 8080As for the function module and the pattern generator and a 16-bit 8086 for the timing operations to handle fast arithmetic. First delivery is scheduled for July.

Megatest Corp., 2900 Patrick Henry Dr., Santa Clara, Calif. 95050 [338]

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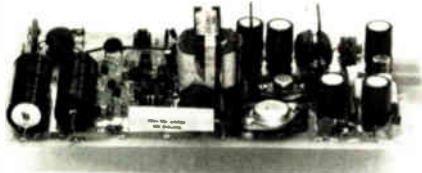
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New products

Instruments

Chart recorder is ultralinear

Multichannel unit uses light gates to expose paper, writes without overshoot

Engineers who must keep accurate records of low-frequency signals can now use a multichannel recorder that needs no compensation to maintain linearity. Capable of recording analog signals up to 5 kHz and square waves to 10 kHz, the HR-2000 Datagraph recorder employs a technology that does not have the problems of inertia and angular variations that must be accounted for in galvanometric and cathode-ray-tube oscillographs.

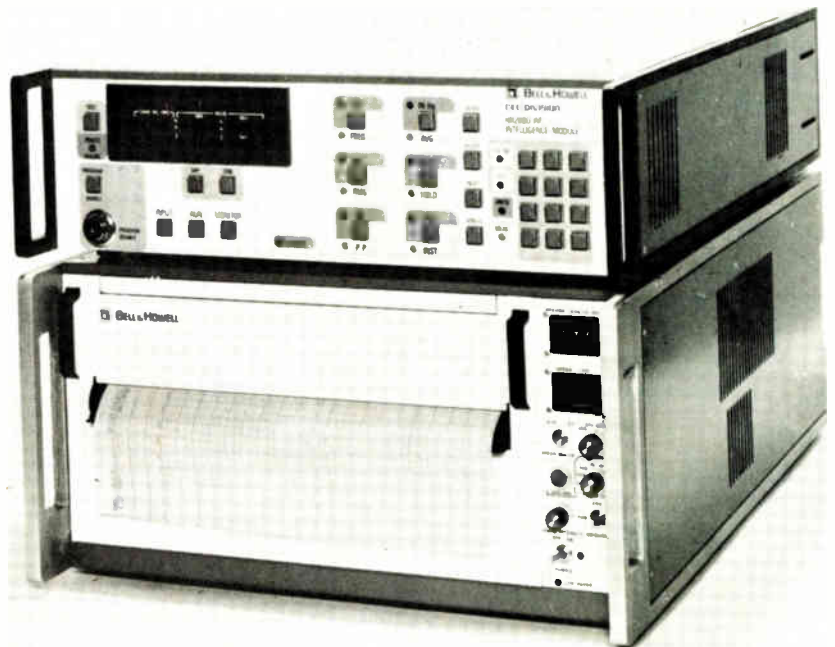
Instead of scanning a beam across the recording medium as in those techniques, the HR-2000 uses a tubular light source that is the same distance from the chart at every point along its length. Between this ultraviolet lamp and the photosensitive medium is a programmable gate

array that operates on a polarization principle. The solid-state array has 80 gates per inch; capable of being opened or closed in approximately 2 μ s, the gates are left open for a period of 20 μ s to fully expose the chart. To record the rise and fall portions of square waves, a series of adjacent gates can be operated simultaneously. Since the writing mechanism has no moving parts, overshoot and other inertia-related problems are completely eliminated.

This gated-light technique is used in both versions of the recorder, a 960-gate model that works with charts up to 12 in. wide and a 640-gate unit for records up to 8 in. wide. The units have a fixed sensitivity of 1 v/in. and an input impedance of 10 k Ω on each channel. Up to 28 channels can be accommodated.

Recordings can be made on ordinary direct-print chart papers of any standard width from 3½ to 12 in. Chart rolls may be 100 or 200 ft long, depending on paper thickness, and rolled with the emulsion on the inside or outside.

At the front panel, users can select chart speeds ranging from 0.01 to 129 in./s and a fixed-length record may be specified from 1 to 999 in. An internal chart take-up roll can be



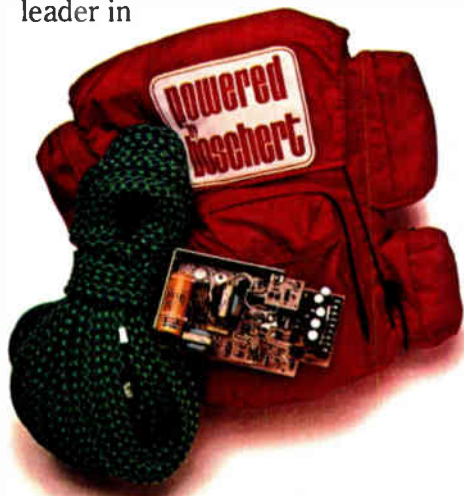
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New products

used for high-speed or long-duration recording. Grid lines, printed as data is recorded, are also selectable at the front panel and the recording process can be monitored as it occurs.

Shown atop the recorder is an optional data analyzer. This unit allows users to specify the scanning of up to 28 channels and to annotate the recordings with time of day, Julian date, full-scale value, and units of measurement.

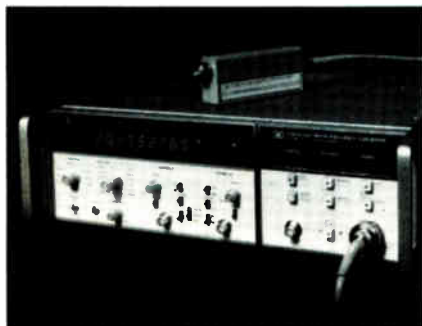
A basic 12-in. recorder with seven channels activated is priced at \$10,500; additional channels can be activated for an extra \$110 each. Delivery time is approximately 60 days.

Bell & Howell Co., CEC Division, 360 Sierra Madre Villa, Pasadena, Calif. 91109 [351]

Converter measures pulsed frequencies to 26.5 GHz

The model 5355A microprocessor-controlled frequency converter measures pulsed as well as continuous-wave frequencies up to 26.5 GHz. A plug-in for the model 5345A frequency counter, the 5355A will measure the average frequency in a burst, as well as pulse-repetition frequency, pulse width, and pulse-to-pulse timing, using the time-interval capability of the 5345A.

The 5355A measures pulsed signals as narrow as 60 ns, with an accuracy to within 3 kHz and a resolution selectable to within 100 Hz or better. The instrument's fm tolerance is 80 MHz pulsed and 60 MHz continuous wave. CW measurements range from dc to 26.5 GHz, with a -20-dBm sensitivity. The unit has a resolution of 1 Hz per second.



With automatic amplitude discrimination, the 5355A looks at only the largest signal in a complex spectrum. Other automatic operations that are provided through microprocessor control include signal acquisition, gate generation, and frequency averaging.

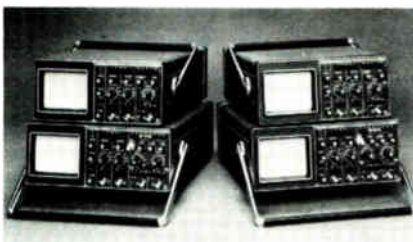
The 5345A counter sells for \$4,500, and the plug-in converter for \$4,150. Delivery takes 10 weeks.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [353]

35-MHz oscilloscopes sell for less than \$1,600

Two general-purpose, portable 35-MHz oscilloscopes are now available for digital and computer applications. The PM 3216 and PM 3218 both have a maximum sweep speed of 10 ns per division and a trigger hold-off capability that eliminates double triggering on digital signals, making it unnecessary to use the time base in its uncalibrated mode.

The instruments also have a 2-mv sensitivity over the entire 35-MHz



bandwidth, a trigger sensitivity of one division, and an external trigger sensitivity of 200 mv. The external trigger has a 10:1 attenuator, providing a broad dynamic range.

The PM 3216 is a dual-trace, single-time-base unit. The PM 3218, also dual trace, is a dual-time-base model that also has an alternate time-base display.

Each oscilloscope operates from any of the following line voltages: 110, 127, 220, and 240 v ac, for frequencies between 46 and 440 Hz. Alternatively, they will work off supplies of between 21 and 27 v dc. An optional battery power supply allows the user to operate the light-

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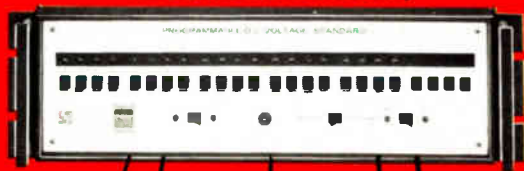
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The PM 3216, available this month, sells for \$1,345. The PM 3218, scheduled for delivery in September, will sell for \$1,595.

Philips Test & Measuring Instruments Inc., 85 McKee Dr., Mahwah, N. J. 07430. Phone (201) 529-3800 [354]

Fiber-optic meter measures current and optical power

As fiber-optic links become more popular, the need to measure electro-optical parameters—such as source optical power, cable output power, and detector responsivity—increases. The model FPM-1 not only functions as a meter for optical power, but also measures electrical current.

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The sensing head for optical power measurement has six interchangeable connectors and two single-fiber adapters, accepting fibers up to 1 mm thick. An adapter for detector measurements is available.

The unit operates on either 115 v or 230 v, at 50 to 400 MHz; an internal battery supply can be used in the field. The FPM-1, with a sens-





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200-2000 MHz 40 W CW
210-225 MHz 1 MW 5 uS
385-575 MHz 1.5 KW CW
400-700 MHz 1 KW .03 DC
950-1500 MHz 1 KW .06 DC
900-1040 MHz 5-10 KW .006 DC
1.2-1.35 GHz 500 KW 2 uS
1.5-9.0 GHz 150 W CW
3.2-3.3 GHz 10 KW .002 DC
2.7-2.9 GHz 1 MW 1 uS
3.1-3.5 GHz 1 MW 1.3 uS
2.7-2.9 GHz 5 MW 2-3 uS
4.4-5.0 GHz 1 KW CW
5.4-5.9 GHz 5 MW .001 DC
6 GHz 1 MW 1 uS
6.2-6.8 GHz 200 KW .37 uS
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9.375 GHz 40 KW 5-1-2 uS
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Electronics/July 5, 1979

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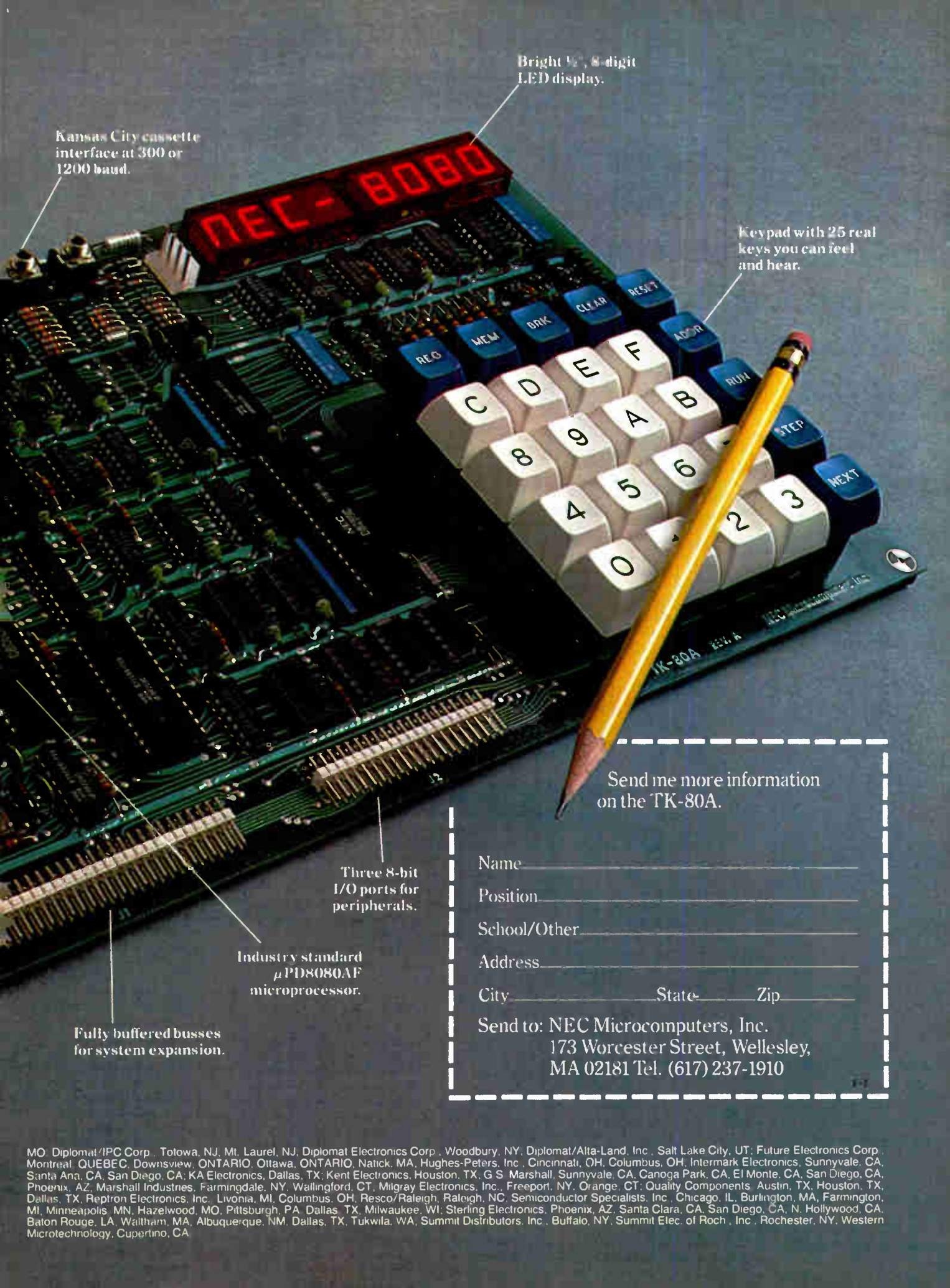
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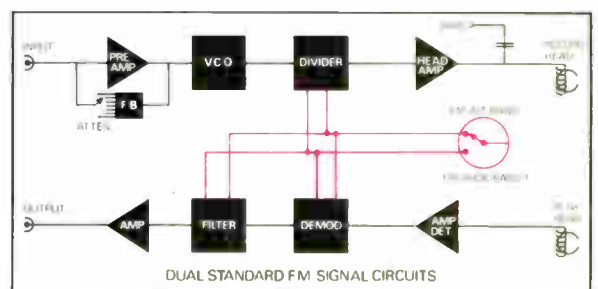
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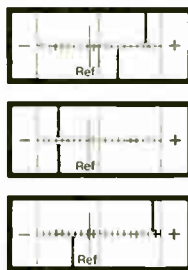
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New products

Power supplies

Switcher modules deliver 250 W

One military-grade module preprocesses the ac input, a second produces the dc

Powercube has been making miniature power modules to military specifications for years. But with its two new product families, the Billerica, Mass., subsidiary of the Unitrode Corp. has not only reached the 250-w output level, but also may have made custom power supply design a simple matter of picking the right modules.

Modular power supplies for military applications must perform two basic tasks, according to Powercube marketing manager, John C. Prestidge. First, they must take whatever basic power is available, whether direct current or alternating current at a wide variety of frequencies. They must filter out radio-frequency and other forms of interference and convert the electricity into a form that allows easy, low-loss distribution throughout a system. Second, the sanitized power must now be converted into dc at specific voltages. Powercube's new ASPG mod-

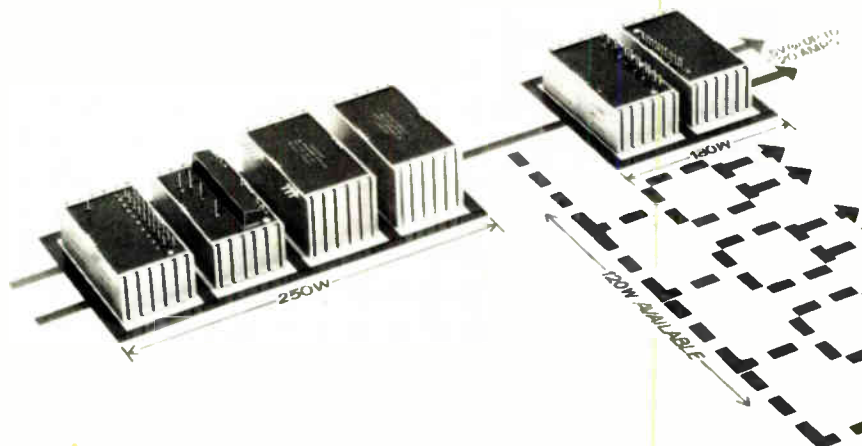
ules perform the first task; its new 5TR does the second.

Altogether, to bridge the gap from between something like raw 400-Hz basic aircraft power to the 5 v dc needed for logic applications, a user might select as many as six of these ASPG and 5TR modules, depending on current drain, electromagnetic compatibility considerations, the amount of filtering desired, and other requirements.

ASPG series modules accept either 115 or 220 v ac or 270 v dc from what may be electrically very dirty sources and turn it into a well-mannered 40-v peak square wave at from 20,000 to 40,000 Hz.

The ASPG-S1 and -S2 are always used together. The S1 and S2 combine the basics of an ac-ac converter: rectification, filtering, regulation (via a pulse-width switching regulator running between 20,000 and 60,000 Hz), and a 20,000-to-40,000-Hz inverter. These two modules are each 2 by 4 by 1.3 inches.

Together with these modules may be used either an S3 and S4 or an S5 module. The S3 includes high-pass and electromagnetic-interference filtering designed to bring the ASPG system into compliance with MIL-STD-461 on emi. The S4 simply includes extra filtering for better control of the square wave's superimposed ripple. The efficiency of an ASPG system, from S1 input to S4



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New products

or S5 output, is a nonderating 75%.

The S5 combines the functions of the S3 and S4 in a single large module. Instead of the 2 by 4 by 1.8 in. of the S3 and S4, the S5 measures 2.25 by 2.5 by 3.625 in.

The 20,000-to-40,000-Hz square wave generated by the ASPG units is converted into dc by the 5TR160 or 5TR200 regulated dc power convertors. Except for input voltage and output current specifications, the units are almost identical. The 5TR200 accepts 40 to 48 v ac peak and yields 20 A maximum; the 5TR160 accepts 40 to 55 v ac peak and delivers up to 16 A.

Both the -200 and -160 are mechanically divided into two modules, one containing rectification and filtering circuitry and the other a passive magnetic regulator. Output from both the -200 and -160 is 5 v dc $\pm 1\%$ with 100-mV maximum ripple.

Although this may seem high, Prestidge says the ripple is at frequencies above 20,000 Hz and thus can be removed with a relatively small capacitive filter, if desired. Line and load regulation are 50 mV.

The efficiency of the 5TR module sets is high at 78% over their -55° -to- $+100^{\circ}$ C temperature range. Efficiency does not derate with temperature, although there is a voltage temperature coefficient of $0.025\%/^{\circ}$ C. Combined efficiency of the ASPG and 5TR module systems is about 58.5%; while this is low compared to switchers available for commercial applications, Prestidge says it is a good figure for a mil-spec product, especially one as highly modularized as this and with such a wide operating temperature range.

Since the 5TRs do not absorb the full 250-w output of the ASPGs, notes Prestidge, there is power left for standard Powercube Cirkitblock modules with output voltages from ± 15 v dc on up. The square wave input is a common denominator among the Cirkitblock family, according to the company.

Prices for ASPG modules in lots of one to nine are: S1, \$308; S2, \$367; S3, \$80; S4, \$80; S5, \$160. The 5TR160 and 200 are priced

identically at \$450 in lots of one to nine. Delivery time is 10 to 12 weeks. Powercube, a subsidiary of the Unirode Corp., Eight Suburban Park Drive, Billerica, Mass. Phone John C. Prestidge at (617) 667-9500 [401]

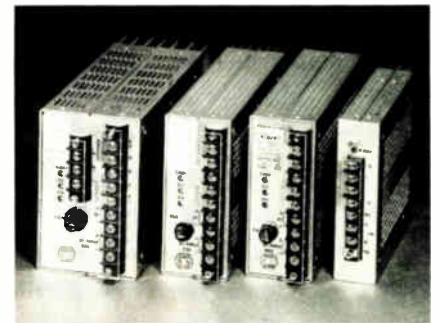
Dc-dc converter family delivers 30 to 125 W

Designed to accept inputs of 12, 24, or 48 v dc, units in the Kepco/TDK RMD series of power converters produce isolated, stabilized, controllable outputs between 5 and 28 v dc. The converters, which are adjustable over a range of -30% to $+10\%$ of their nominal output voltage, are offered in models with nominal power ratings from 30 to 125 w.

Efficiency is typically in excess of 70% and is no less than 65% to 70%, depending on model. Worst-case regulation for simultaneous rated changes in line, load, and temperature is 2.2% (1% typical). The units all have a maximum ripple and noise rating of 10 mV rms and a maximum peak-to-peak switching component of 100 mV. Peak-to-peak spike voltage to 10 MHz is rated at 1% of the output voltage + 50 mV.

Units in the RMD series feature remote error sensing, adjustable overvoltage protection, and remote turn-on by means of a TTL-level signal. The converters, which operate from 0° to 71° C, are covered by a five-year warranty. Prices range from \$216 for the 30-w devices to \$334 for the 125-w models. All versions are in stock.

Kepco Inc., 131-38 Sanford Ave., Flushing, N. Y. 11352. Phone Paul Birman at (212) 461-7000, Ext. 742 [403]



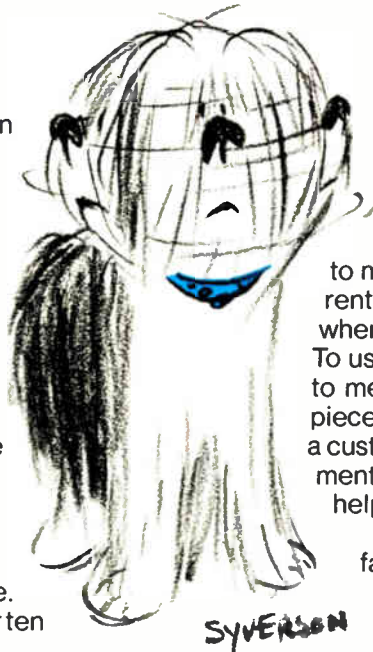
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Tektronix 465 Oscilloscope. BW 100 MHz; display 8 x 10; 5 mV/div to 5 V/div sens.; sweep rate 50 ns/div to 0.5 s/div; x10 magnifier; dual trace; delayed sweep; x-y operation.



Hewlett-Packard 8565A/100 Spectrum Analyzer. 0.01 to 22 GHz with internal mixer; 14.5 to 40 GHz with 11517 external mixer; 100 Hz and 300 Hz resolution bandwidth; Absolute Amplitude Calibration: -110 dbm to +30 dbm.

Brush 260 Strip Chart Recorder. 1 mV to 500 V; chart speeds 125 mm/sec. to 1 mm/min., incl. four event markers; pressurized ink; response: DC to 100 Hz.

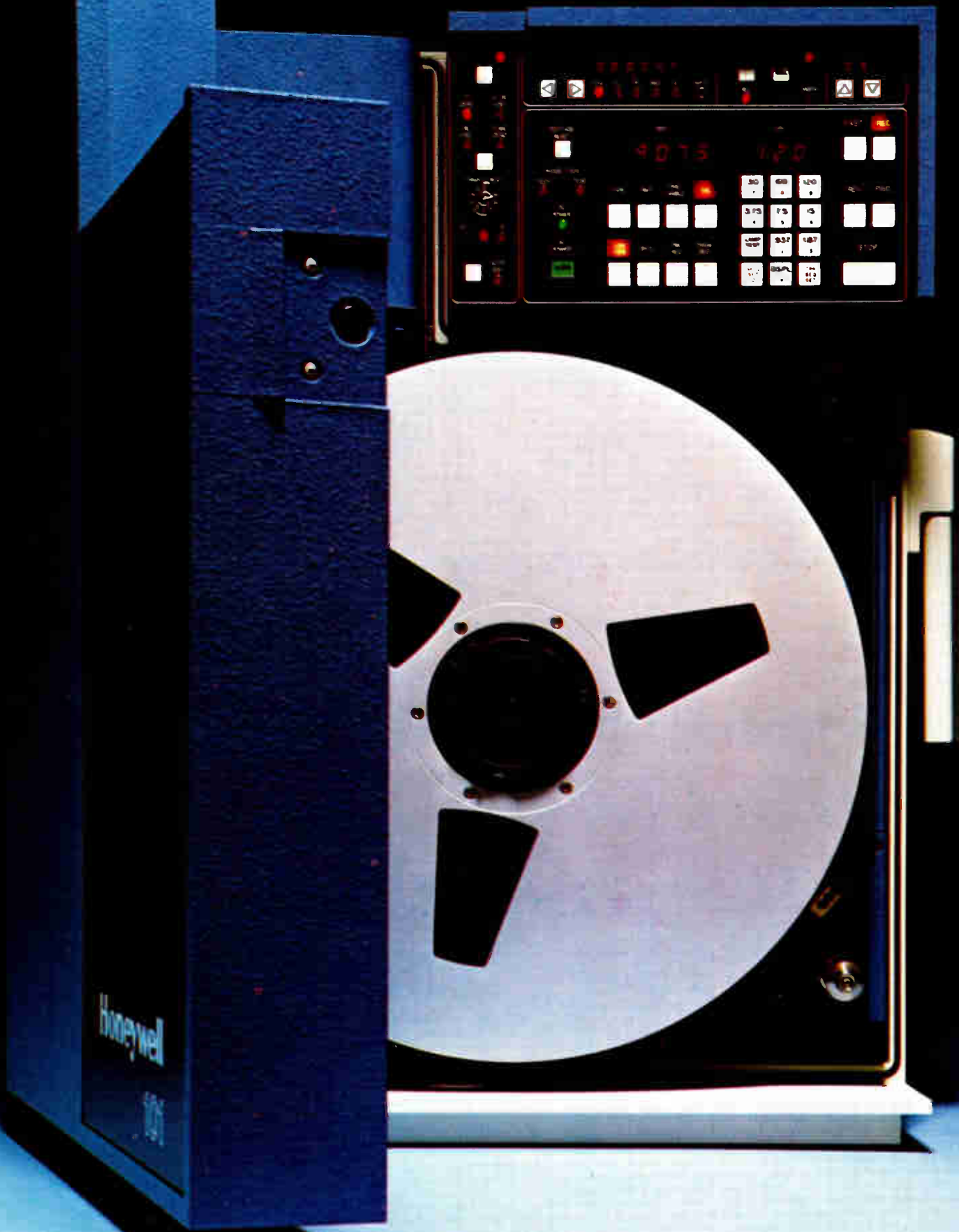


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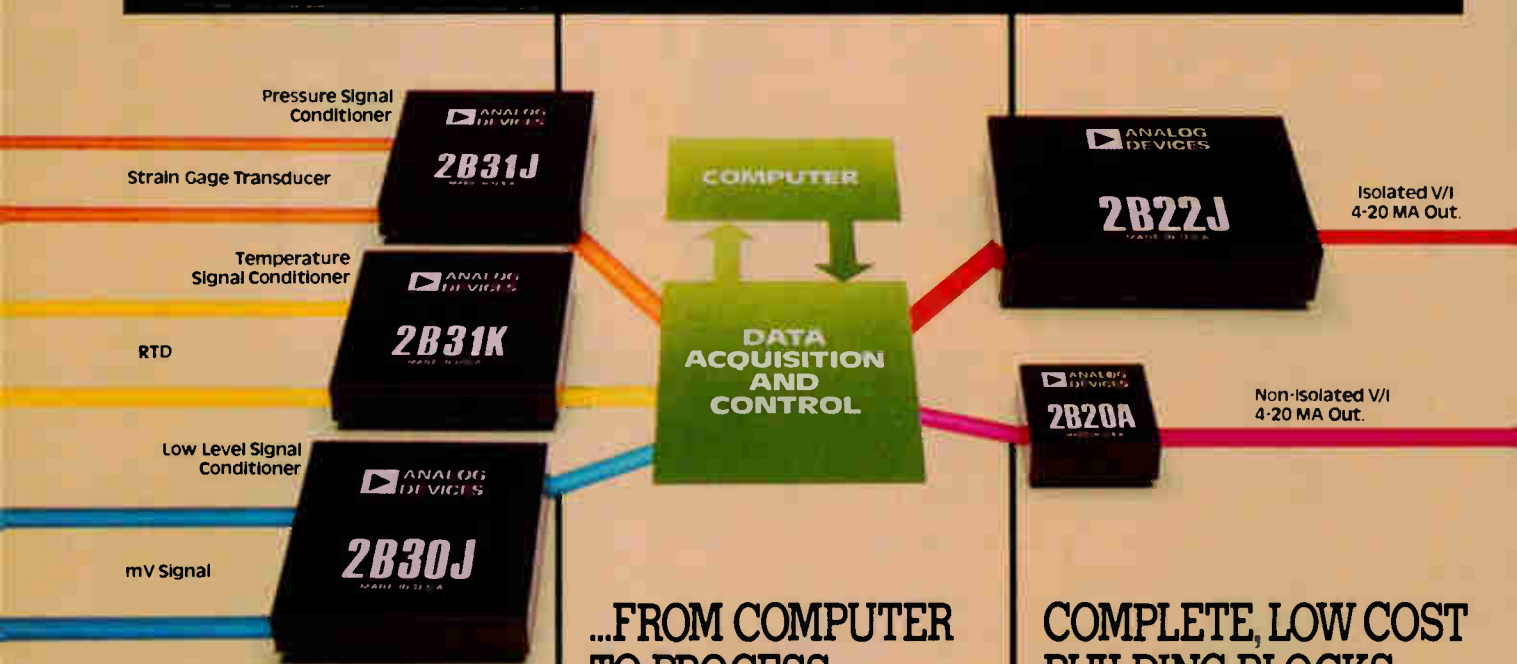
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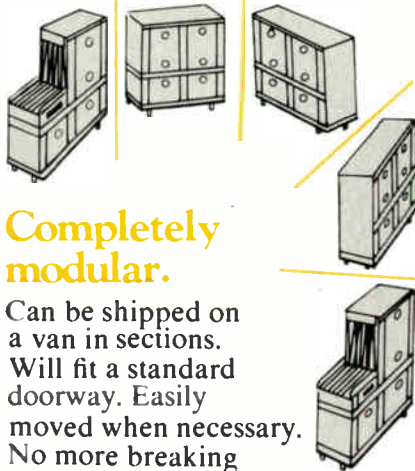
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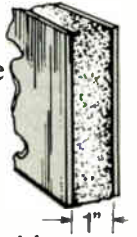
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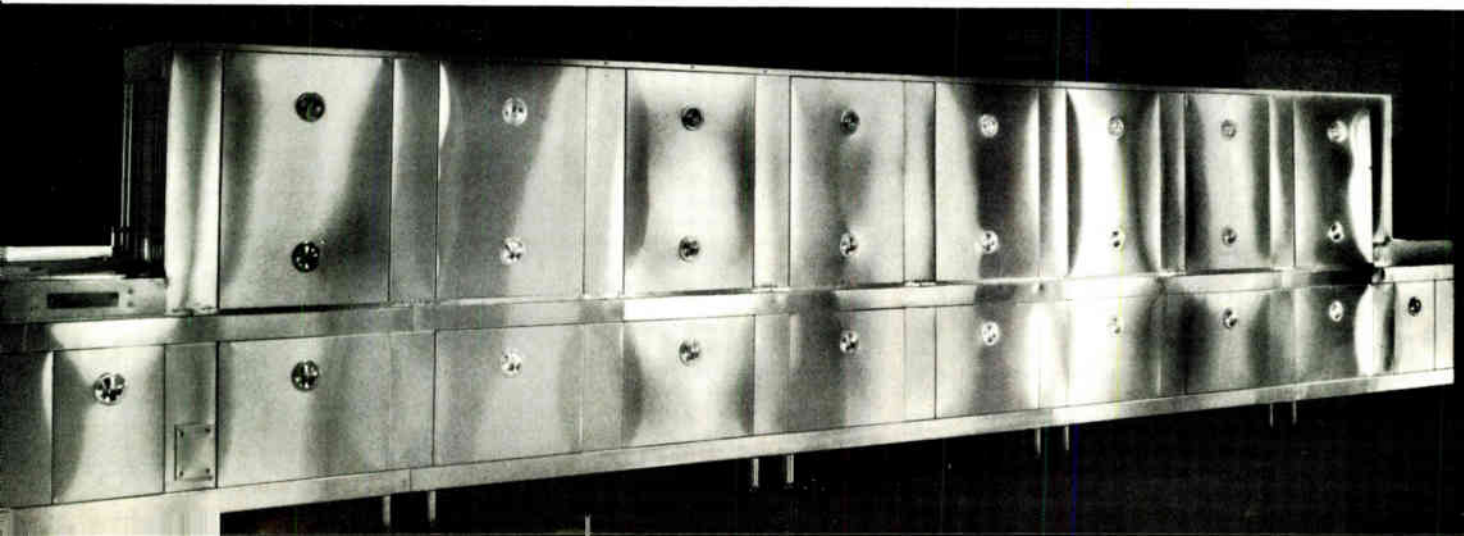
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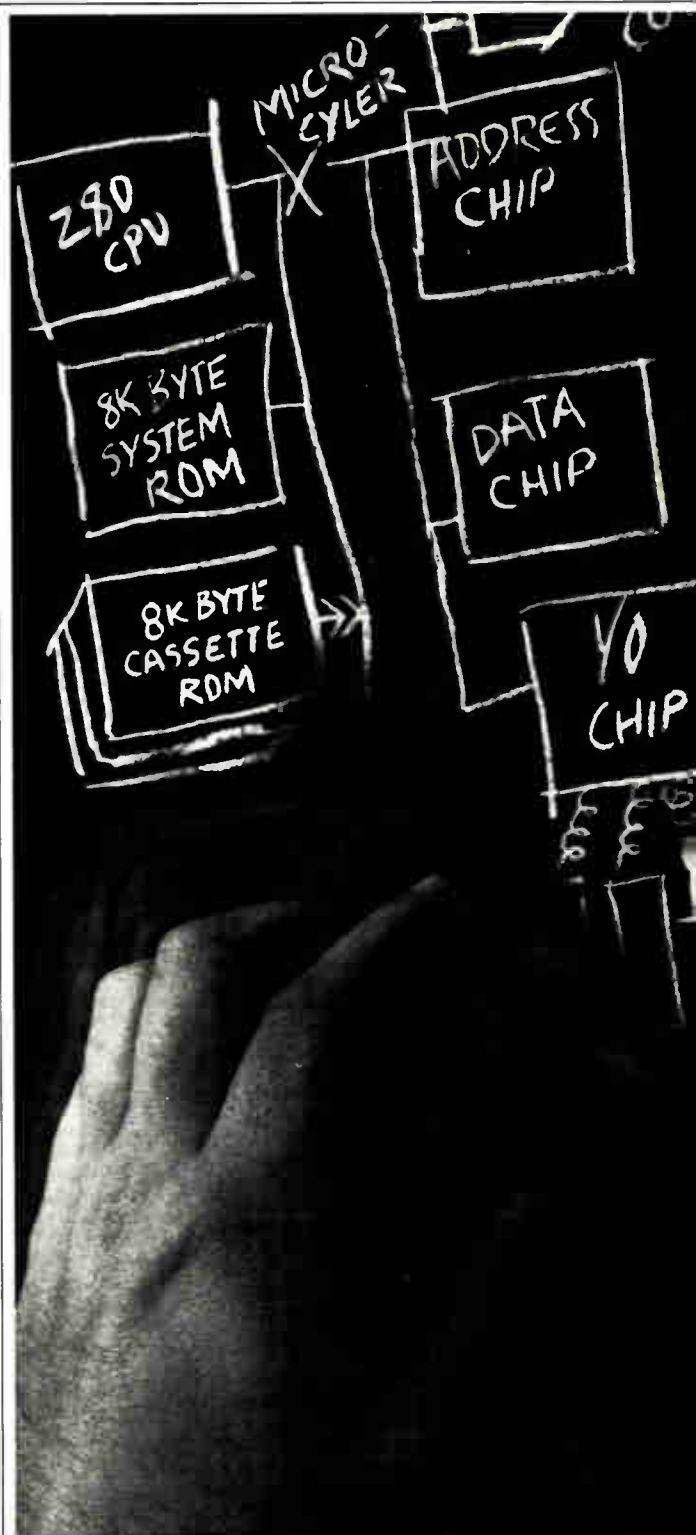
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only do half the job?"

you calculate the number of parts, board space, assembly time and testing involved in a standard approach, you're often better off with custom. And, if you're using a microprocessor-based system, you have the added expense of software development.

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You can get copies from us at AMI Custom III Marketing, 3800 Homestead Road, Santa Clara CA 95051. Phone (408) 246-0330. Or get in touch with one of these AMI sales offices: California, (213) 595-4768; Florida, (305) 830-8889; Illinois, (312) 437-6496; Indiana, (317) 773-6330; Massachusetts, (617) 762-0726; Michigan, (313) 478-9339; New York, (914) 352-5333; Pennsylvania, (215) 643-0217; Texas, (214) 231-5721; Washington, (206) 687-3101.

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Circle 183 on
reader service card

Computers & peripherals

Automating management

Software package works with data-collection terminals to gather factory information

What's good for worker productivity—automation—could be as good for management productivity. Taking a step in that direction is a new software package from Hewlett-Packard, which collects data from terminals on the factory floor.

Called Datacap/1000, the package is one of four that HP has unveiled for its 1000 series of mini-computers. Supporting three new industrial data-collection terminals, the models 3075A, 3076A, and 3077A, the Datacap software lets an unfamiliar user program how factory workers can activate the system,

what type of data the terminals are to collect, and how to validate that data. An appropriate response, either through the terminals' display or printer, can then be ordered.

"Factory data collection is in its infancy," says Carlos Avila, market development manager for HP's Data Systems division, Cupertino, Calif. "Up to now the terminals for the factory floor have been relatively expensive." But less expensive terminals such as HP's new units, which range in price from \$2,090 to \$4,230, are increasing the interest in such systems, he says.

To support the Datacap and other new software, HP has added RTE-IVB, a new version of its real-time executive operating system. Using a new session monitor, this system's software provides for what HP calls a more orderly management of the system's resources and improved typical terminal response time. In addition, the operating system's new time-slice capability lets several users at the same priority level share the computer and memory and even

programs, in a manner similar to time sharing.

Also supported by the new RTE-IVB operating system is a new vector instruction set designed to operate on HP's 1000 F-Series of computers. Using special Fortran language commands, operations on the rows and columns of a matrix (the so-called vectors) can be performed 4 to 10 times faster than before. For example, HP says a 100-by-100-element matrix can be inverted in 12.25 instead of 78.45 seconds, and matrices with up to 600 by 600 elements can be handled.

Finally, HP has expanded its Image/1000 data-base management system with an inquiry language called Quiry that lets nonprogrammers retrieve, alter, and report information with English-like commands. For distributed processing systems, the new Image software also lets various 1000 computer systems access the data bases on other computers in the system.

The new operating system is included in the price of new HP-1000 computer systems. The Image data base software, to be available in July, is priced at \$3,000, as is the Datacap/1000 software, which has a delivery time estimated between 8 and 12 weeks. The new Vector instructions for the F-Series computers sell for \$1,500 and will also be delivered in 8 to 12 weeks.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [361]



Band line printer
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Tired of noisy band line printers? Data Printer Corp. has the answer to that problem with a fully enclosed cabinet for its soon-to-be-shipped model 3901.

Printing at 1,100 lines of 48 characters per minute, this microprocessor-controlled peripheral has full line buffering as well as self-test capabilities. With line spacing of 6 lines per inch, the 3901 has a single line advance time of 25 ms and a slew speed of 15 inches per second. The

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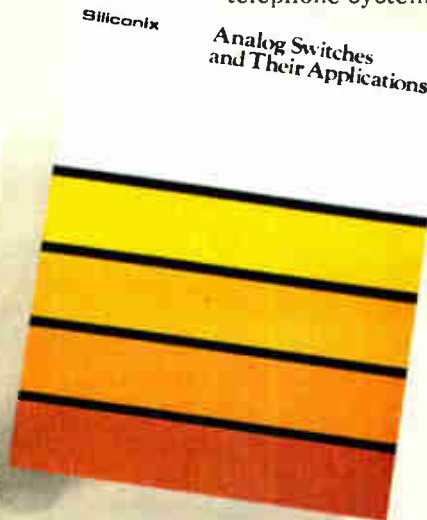
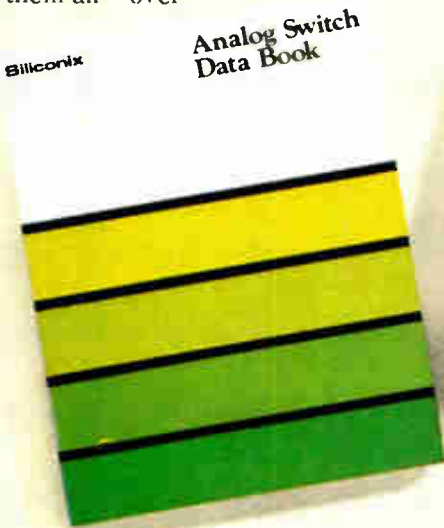
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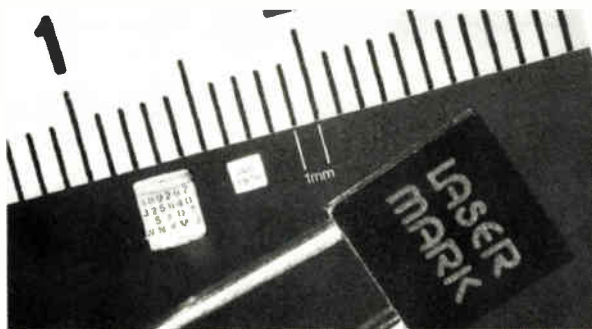
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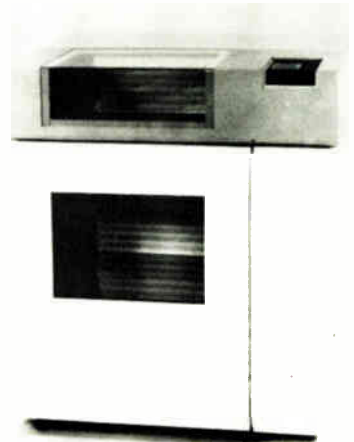
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New products



printer can handle one- to six-part forms ranging in width from 3 to 17.5 in. All inking is done through an operator-loadable cassette. The 3901 measures 40.5 by 32.5 by 27 in. and weighs 275 lb.

Price for the unit will start at about \$7,700 for OEM customers. Deliveries are scheduled to begin in the fourth quarter.

Data Printer Corp., 99 Middlesex St., Malden, Mass. 02148. Phone Pat Connolly at (617) 321-2400 [363]

TI's Omni terminal family grows by three

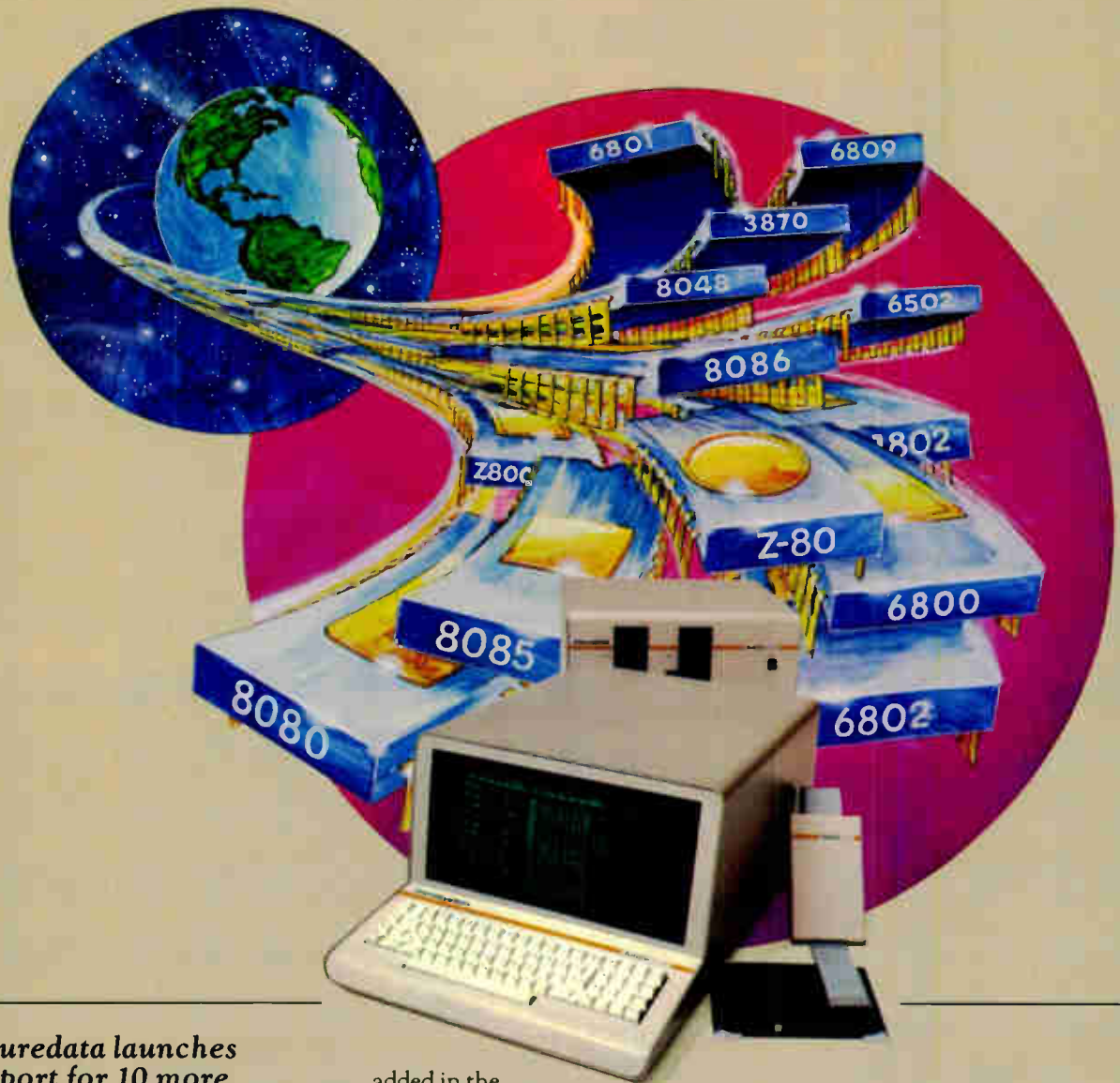
The Omni 800 electronic data terminal family now numbers five with the recent addition of three members: the model 820 receive-only (RO) printer, operating at a rate of 150 characters per second; and the model 825 keyboard-send-receive (KSR) and the model 825 (RO) printers, both operating at 75 c/s.

The 820 RO, a companion to the



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New products

previously introduced 820 KSR, functions at rates between 110 and 9,600 bauds. The terminal has a first-in/first-out buffer, storing up to 1,280 characters. Using bidirectional printing capabilities and a full ASCII character set, the 132-column-wide printer produces an original and five copies using a nine-by-seven-dot matrix character font.

The 825 RO and KSR units, although rated at 75 c/s, are easily upgradable to 150 c/s as user demand increases. These printers also have bidirectional printing capabilities, using a nine-by-seven-dot matrix font, as well as a full ASCII character set. (An ASCII/APL keyboard is optional for the 825 KSR.) Up to three copies and an original can be made. Both 825s operate at 110 to 600 bauds, communicate serial, asynchronous data, and use a 256-character buffer for data overflow protection.

Each 820 RO printer sells for \$1,995. The 825 KSR is priced at \$1,695 in singles, while the 825 RO costs \$1,565 for similar quantities. Deliveries are currently scheduled to begin in October.

Texas Instruments Inc., P. O. Box 1444, M/S 7784, Houston, Texas 77001. Phone (713) 937-2000 [364]

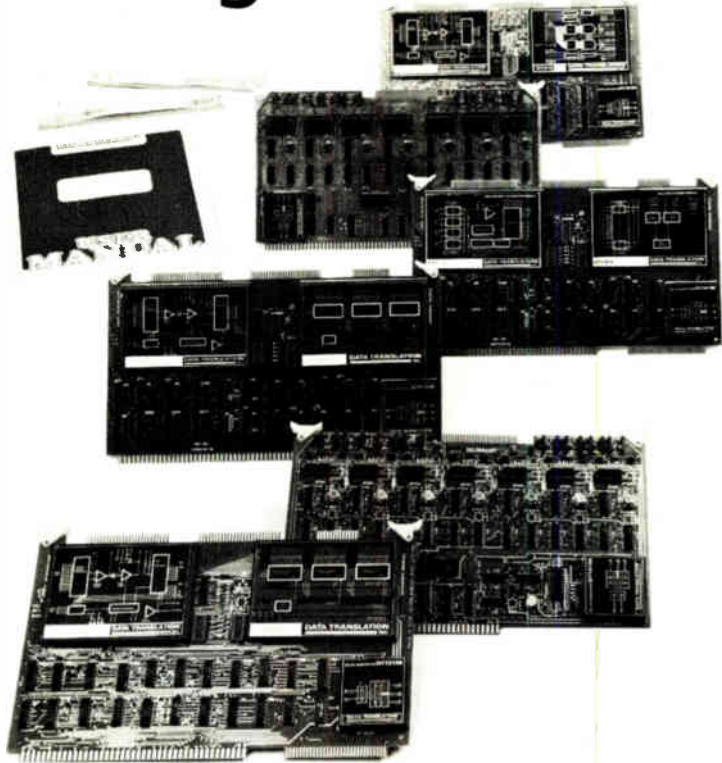
Add-in LSI-2 and LSI-4 memory modules for \$995

For users of Computer Automation's LSI-2 and LSI-4 minicomputers, Trendata/Standard Memories now has an add-in semiconductor memory module. Occupying a half-card slot in the chassis, the PINCOMM CS has a capacity of either 32,768 words by 16 bits or 16,384 words by 16 bits.

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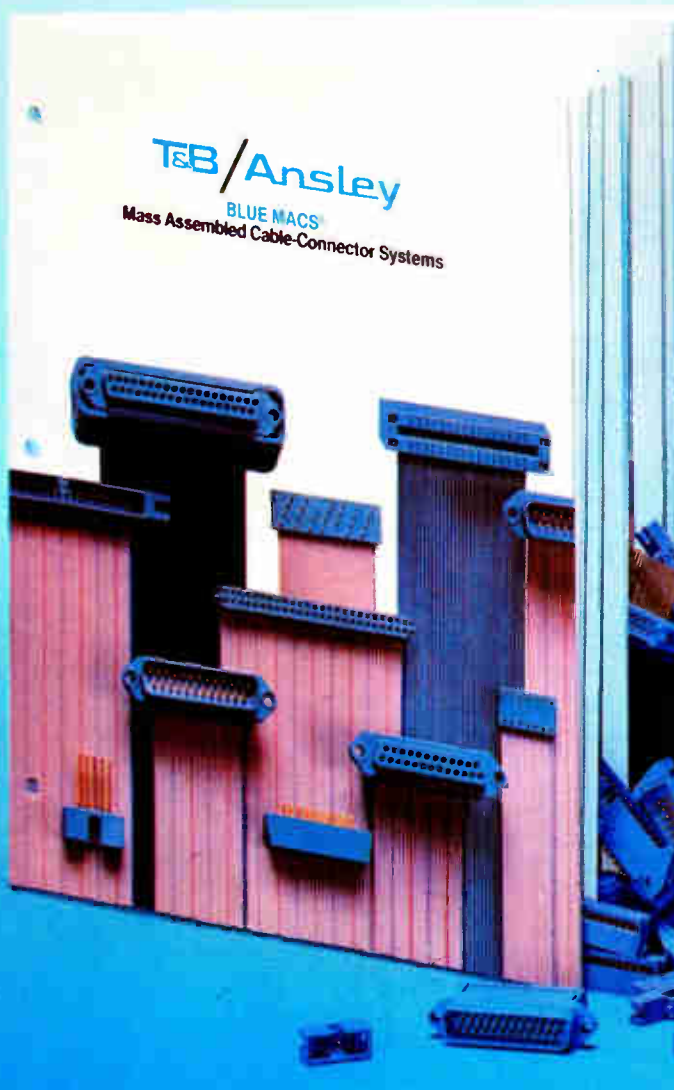
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Trendata Corp., 3400 W. Segerstrom Ave., Santa Ana, Calif. 92704. Phone Carl Peterson at (714) 540-3605. Or, in California, dial toll-free (800) 432-7271; outside California, dial (800) 854-3792 [365]

Memory board replaces MS11L and sells for \$4,670

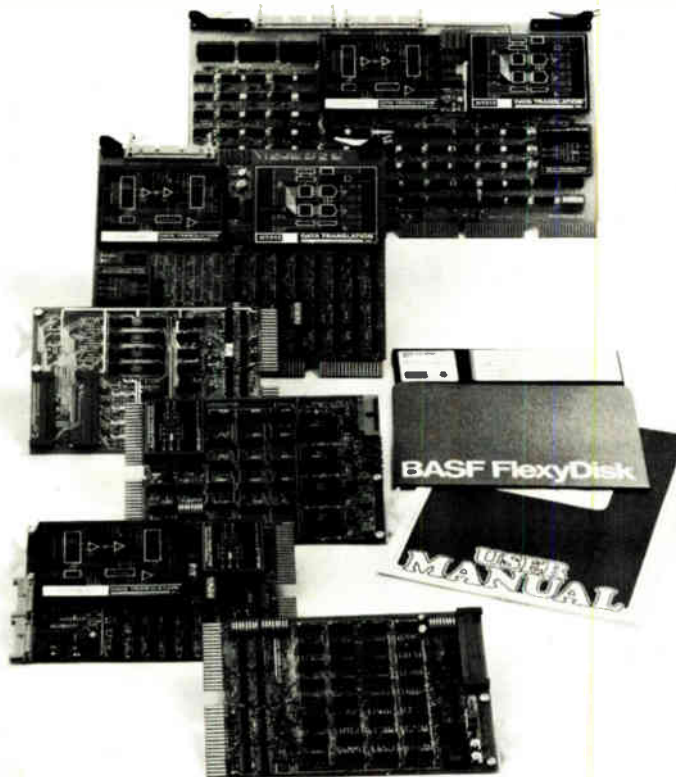
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Plessey Peripheral Systems, 17466 Daimler, Irvine, Calif. 92714. Phone Bill Perry at (714) 540-9945 [366]

Electronics/July 5, 1979



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D/A systems include: up to 8 analog outputs per slot, fast settling of 3usec to 12-bit accuracy, 25mA outputs for guaranteed cable driving, point plotting capability, DMA interface and read/write byte addressable registers.

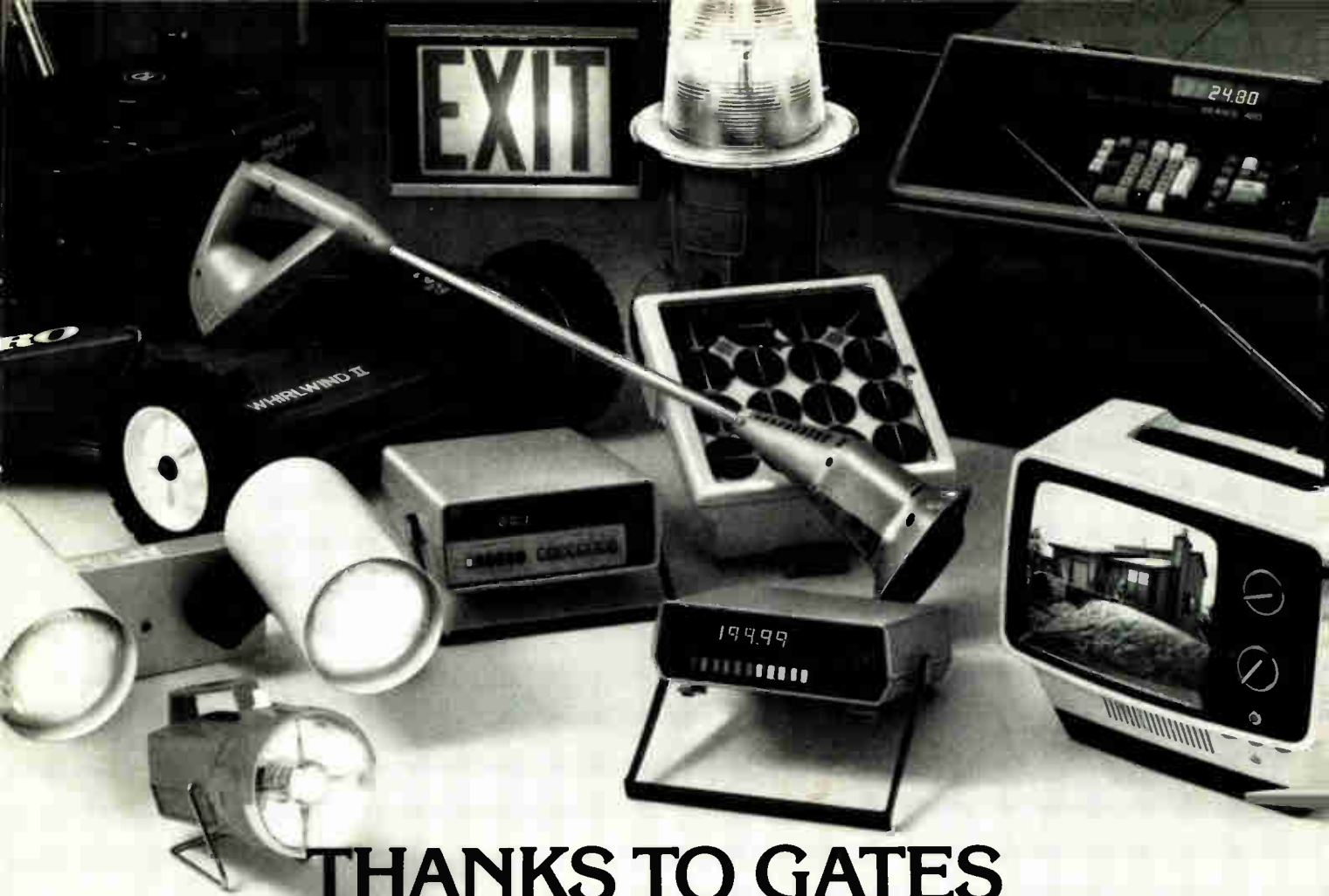
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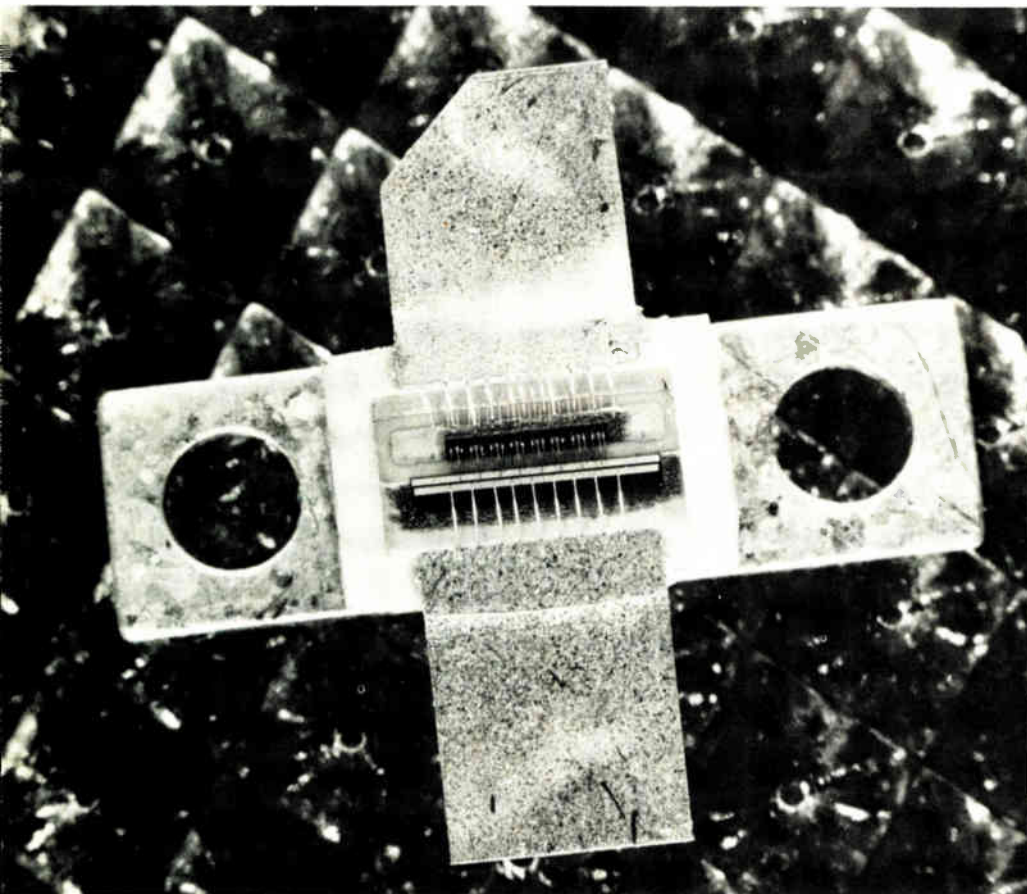
Internally matched Class A device has 20- Ω impedances, 7.5-dB gain, sells for \$200

A classic problem for designers of microwave power devices is that enlarging the chip to increase the output power also drops the impedance to as little as 1 to 2 Ω —hardly adequate in 50- Ω systems. External impedance-matching networks can, of course, be used. Unfortunately, when such networks are designed for impedance ratios of 25:1 to 50:1, they tend to waste power—not too happy a situation when the whole point of the exercise was to boost the output power.

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The result is that the 2.3L60 has an output of 6 W—about double that of competing devices—and impedance specifications, both input and output, of 20 Ω , which means considerably easier external circuitry to make it work in a system, Max says. “We’ve upped the gain and upped the power,” he says, comparing the 2.3L60’s 7.5-dB gain at 2 GHz with the 5- to 5.5-dB figure for 3-W devices at the same frequency.

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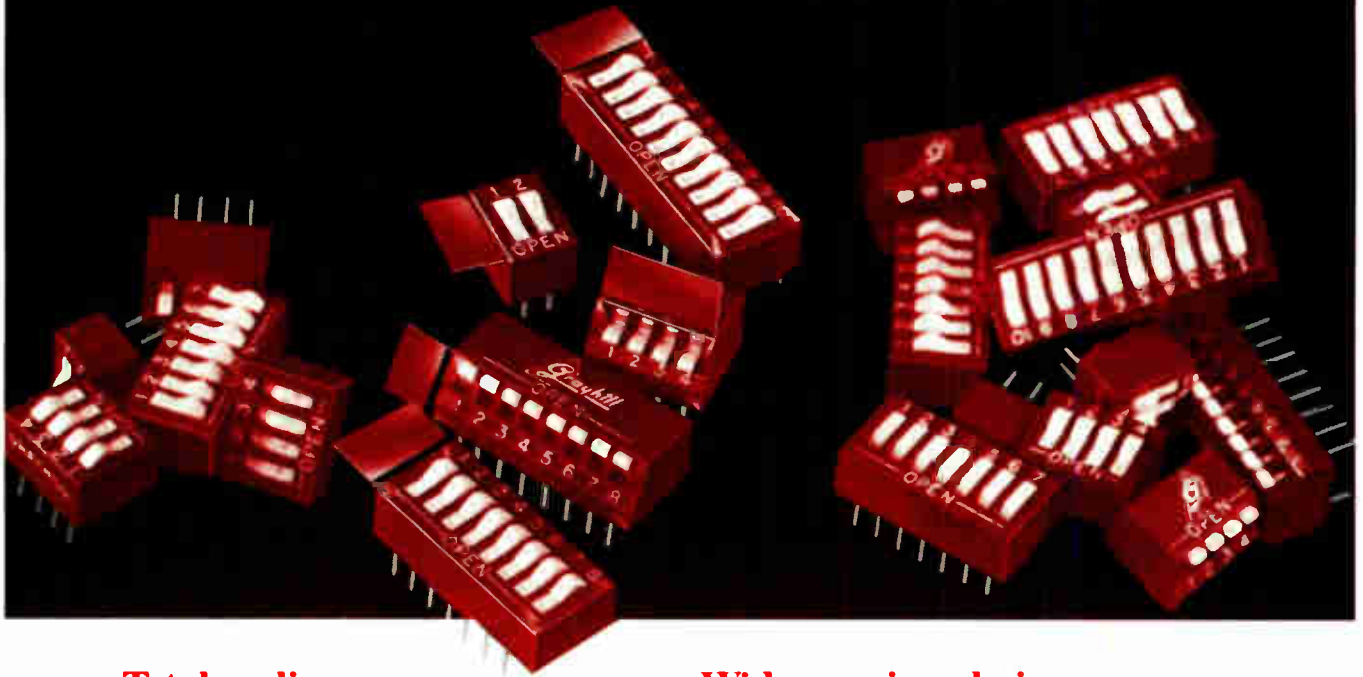
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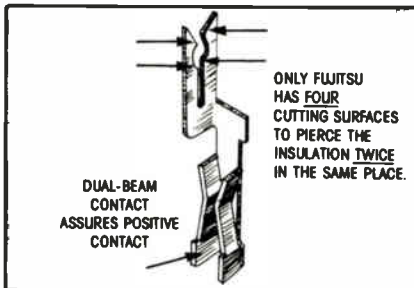
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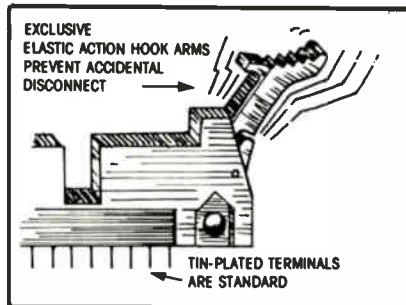
Flat cable connectors are easy enough to find. The trick is finding connectors that can handle every one of your needs consistently, conveniently and economically. Fujitsu flat cable connectors do it all. And they do it better than most.

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The FCN-700 series offers vertical, right angle and wire wrap plugs and open or closed covers for both end-cable and through-cable applications.

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AND RELAYS AND CAPACITORS AN

New products

the device higher gain and makes it easier to broadband, CTC, a subsidiary of Varian Associates, thinks the full Class A part will have ready applications in microwave relay, radio, and data-transmission networks. Moreover, one 6-w device is easier to use than two 3-w parts.

The 2.3L60 is characterized in a common-emitter configuration. It has a maximum power-dissipation rating of 35 W at a case temperature of 25°C. Maximum voltage and current specifications include a collector-to-emitter voltage of 45 V, an emitter-to-base voltage of 3.5 V, and a collector current of 2 A.

The price in 100 to 499 quantities is \$200 each—less than the cost of two 3-w devices at the same band, Max observes. Availability is now.

Communications Transistor Corp., 301 Industrial Way, San Carlos, Calif. 94070 [381]

System tests X.25-based software and hardware

The data-communications protocol of the 1980s may well be X.25, and engineers are now busily designing hardware and software for use with it. XPRT is a microprocessor-based development and diagnostic tool that will aid them in simulating X.25-based networks and terminals, monitoring communications lines, and validating protocol. The XPRT comes as a complete hardware and software package—no additional field programming is needed.

The unit tests data terminal equipment and full networks at three levels—electrical, link control, and data packet—by generating, displaying, and validating X.25 traffic. Regardless of data rate, equipment under test can be connected either locally or remotely, as long as the DTE/DCE can be externally clocked.

Functions in the simulator mode include user-specified or automatic frame generation, user-selectable frame display and validation, packet generation of and reporting of error conditions, and hexadecimal or octal notation.

Loopback testing and selective display of traffic over a line are some of the line-monitor features. The line speed, in the line-monitor mode, is switch-selectable at 300, 600, 1,200, or 4,800 bauds.

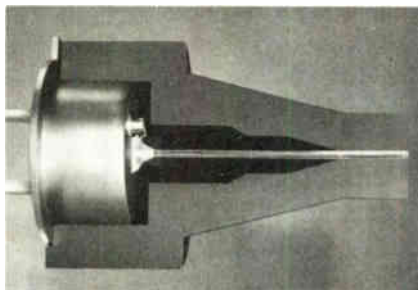
Housed in a 3.5-by-19-by-20-in. unit, the XPRT has an optional cabinet for desktop use. Other options include a video or teletypewriter control console. Single-unit prices start at \$15,000, with delivery scheduled to begin in September.

Tran Telecommunications Corp., 2500 Walnut Ave., Marina del Rey, Calif. 90291. Phone Phillip Black at (213) 822-3202 [383]

Fiber-optic connections get easier to make

The joint venture announced earlier this year between Motorola and AMP Inc. to develop a new fiber-optics packaging scheme has finally borne fruit. Motorola is now shipping a family of ferruled-plastic fiber-optic semiconductor components that when pressfit into an AMP connector, form a common alignment surface with the optical cable. The family consists of one solid-state light source and four detectors with different responsivities.

The infrared light-emitting diode (MFOE102F) has a typical power output of 70 μ W at 50 mA. The four detectors are a p-i-n photodiode (MFOD102F), a phototransistor (MFOD202D), a photo-Darlington transistor (MFOD302F), and a detector integrated with a preamplifier (MFOD402F). Their typical responsivity ratings/ μ W are 0.40 μ A, 100 μ A, 6,000 μ A, and 1.50 mV, respectively. Using the specially designed interconnection, perform-



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Twelve oscilloscopes, including nine benchtop models and three battery-powered portables, a curve tracer and a family of accessories are now available in the United States. Bandwidths range from 5 MHz to 25 MHz. Various models feature dual trace, delayed sweep, and storage modes.

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New products

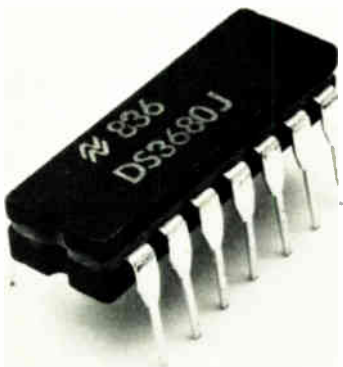
ance speeds of up to 20 megabytes per second and systems of 5 km in length are possible.

The emitter device is priced at \$40, while the p-i-n diode detector sells for \$33.50. The transistor and Darlington detectors sell for \$36.75 each and the IC detector-preamplifier for \$50. (All prices are for 1 to 24 quantities.) The five components are available as off-the-shelf items.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone Jim Herman at (602) 244-6900 [384]

Telephone relay driver uses -52-V battery supply

Engineers designing telephone relay systems often need to let logic signals drive relays whose batteries have ground references that differ from the logic power-supply refer-



ence. The DS3680, a quad relay driver with a 50-mA sink capability, operates with a high common-mode range— ± 20 v referred to the battery ground. It is intended for use with a standard -52-v battery supply, although any power supply ranging from -10 v to -60 v is usable.

The device, which can be interfaced with standard TTL or C-MOS logic, has internal inductive flyback protection. A clamp network within the driver outputs eliminates the need for an external network to reduce the high-voltage inductive backswing that occurs when the relay is turned off.

The DS3680 has a very low differential input current (typically 100 μ A) and therefore draws little power from the driving circuit. Differential inputs allow either inverting or non-inverting operation. Standby power is low, typically 50 μ W per driver, when the driver is off.

Available in either plastic or ceramic 14-pin dual in-line packages, the telephone relay drivers sell for \$3.38 each, in 100-piece quantities. Delivery is from stock.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone Kurt Siem at (408) 737-5712 [385]

Fiber-optic modules transmit at 2 megabytes per second

Electrically interfaced systems are being changed over to fiber-optic systems at a steady rate. Therefore it is not too surprising that yet another set of fiber-optic modules has been introduced for transmitting and receiving digital data. The CTM-100 (transmission) and the CRM-100 (reception) modules are fully integrated optical-to-electrical or electrical-to-optical transducers specifically designed for digital data transmission over a fiber-optic channel.

As part of an entire system, the devices can transmit at the rate of dc to 2 megabytes per second, non-return to zero. If separated by less than 500 meters, they will have an error rate of less than 1 in 10^9 .

Both modules have a built-in optically integrated connector, lessening alignment problems between the light source and the fiber. Designed to work with a TTL interface, the CTM-100 translates a TTL level input into an optical output source, and then the CRM-100 changes that input source back into a TTL signal.

The modules require a single +5-v power supply and will operate in either a synchronous or asynchronous format. In 1,000-piece quantities, each unit sells for \$190. Delivery time is within six weeks.

Canoga Data Systems, 6740 Eton Ave., Canoga Park, Calif. 91303. Phone Richard McCaskill at (213) 888-2003 [387]

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*Suggested U.S. list price



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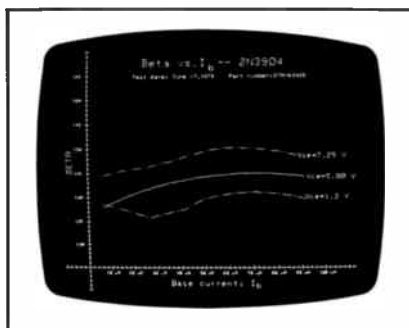
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The LM-25 and LM-80 fit the engineering environment as well as the production line. The systems are uniquely designed using a parallel back plane with an analog and digital bus for fast, direct communication between the power supplies and multimeters, and the system crosspoint matrix and Z80 microcomputer. All measurements can be made routinely to an accuracy of 1 part in 4000 (full scale) and contact capacitance has been minimized with full Kelvin and driven guard bus and matrix structure. Design engineers can quickly evaluate many design options and facilitate engineering characterization of all MOS and bipolar devices.

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to meet higher production testing requirements. Supported host computers manufactured by Digital Equipment Corporation, Hewlett-Packard Corporation and Data General Corporation include software programs for bidirectional data transfer and can control up to eight LM-25/LM-80's.

Checkout Experience

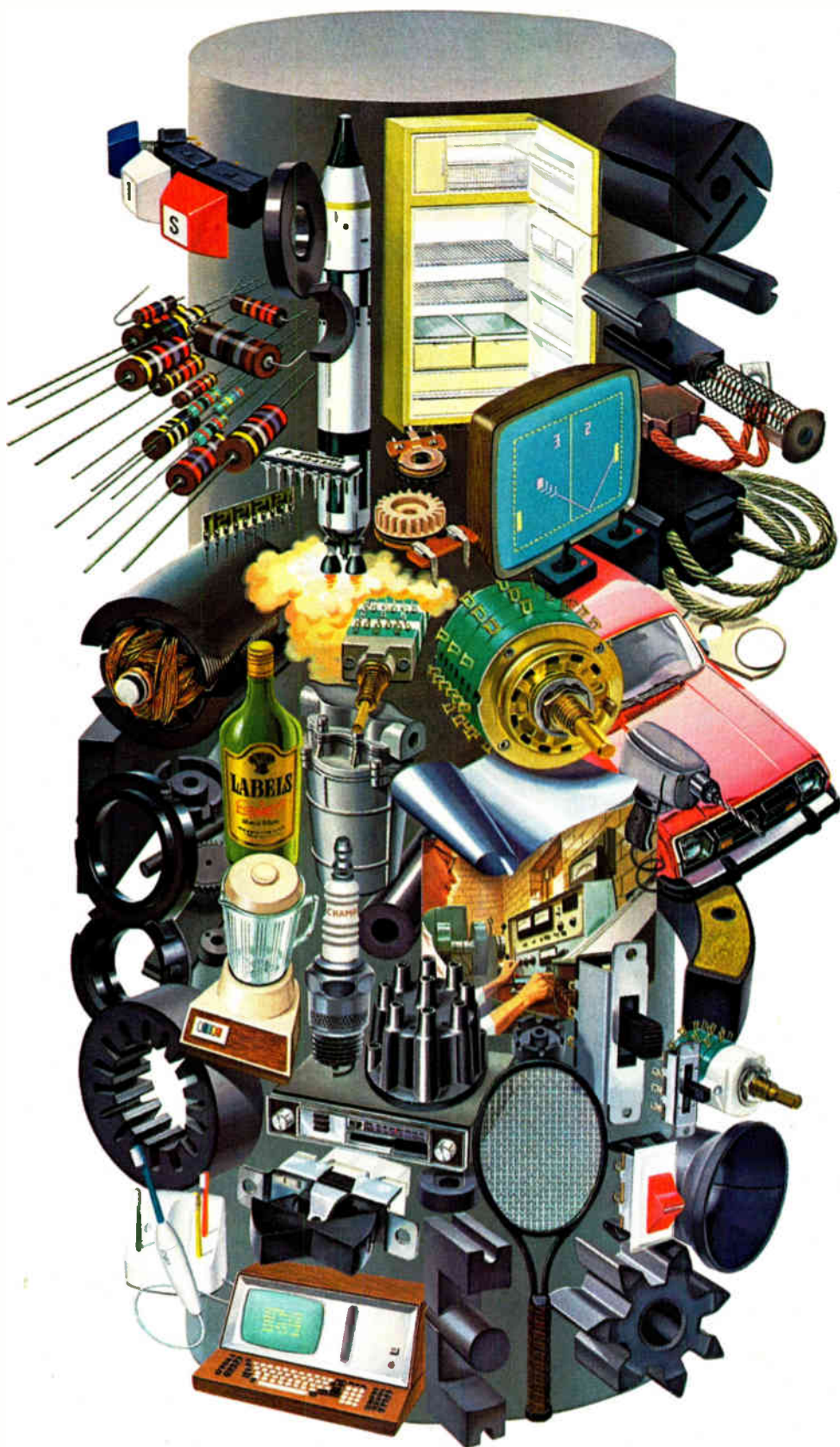
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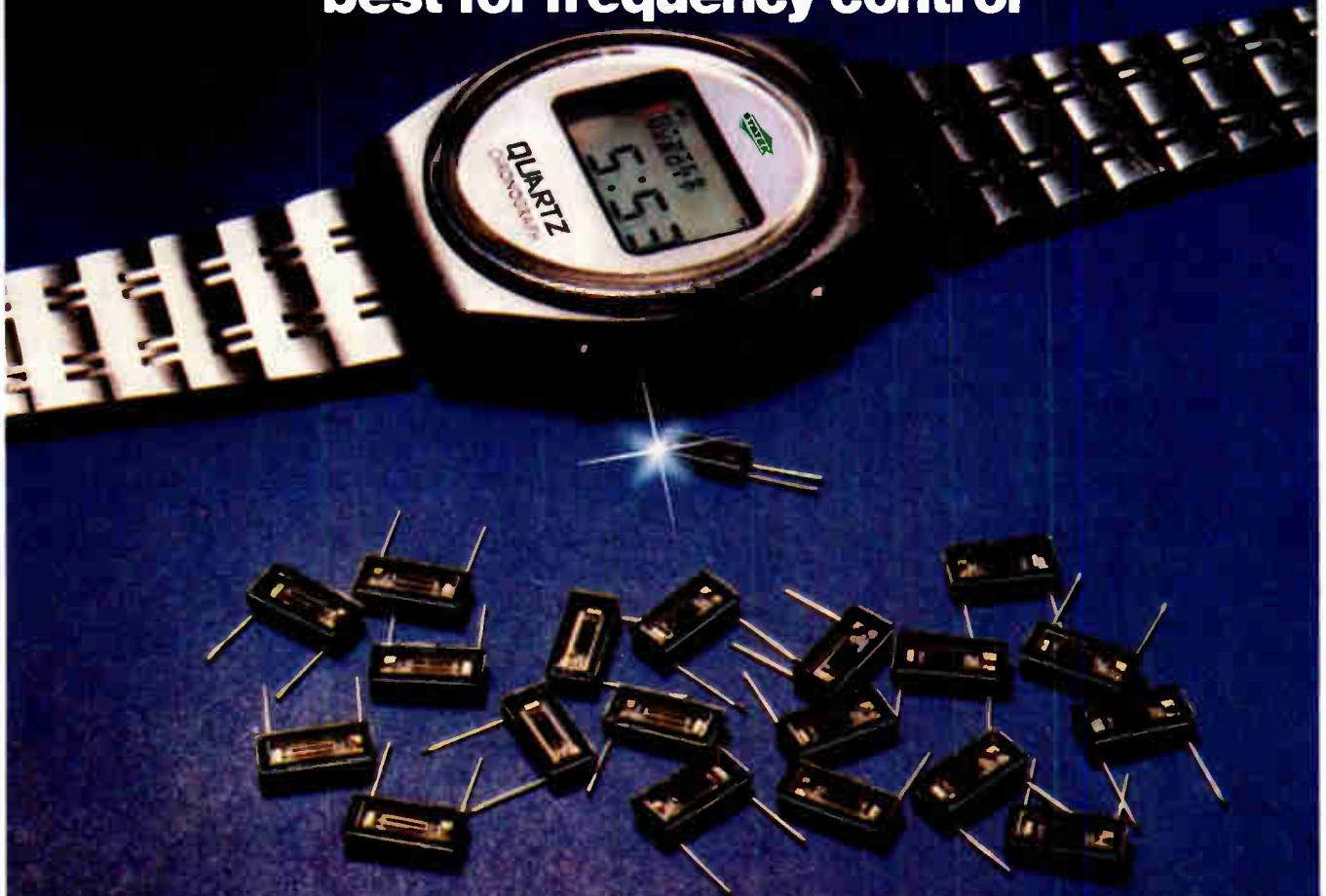
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Microcomputers & systems

System supports fast bit slices

Flexible microprocessor development unit tops 20 megahertz

Microprocessor development systems have come a long way in their short lifetimes. Despite their rapid rise from obscurity into fairly standard tools for debugging chips and software, they have nevertheless left some needs unfulfilled. One is the need for raw speed to emulate the fastest bipolar bit-slice processors. Another closely linked one is the need for a flexible configuration that permits users to work more intimately with the target logic.

Over the past few years, MDS consultant Bjorn Dahlberg found these to be such strong multiple user demands that he not only devised such prototype units for major

clients, but is now bringing out his own line.

The DS100 development system is a fast diagnostic tool for debugging programs ultimately intended for read-only memories, according to Dahlberg, who is president of his firm, Hilevel Technology Inc. With cycle speeds of 20 MHz and up, it is one of few such units that can emulate bit-slice processor systems, he says.

The unit accommodates the AMD 2900 family and its second sources, the Signetics 8X300 and 8X02 and the TI 74S181.

Flexible. To accommodate the varying word lengths and instruction sets common with bipolar logic, the DC100 will address 65,536 memory locations with word lengths up to 480 bits. This means the system can access more than 31 megabits—the product of the addressing range and the word width. The system's worst-case access time of 41 ns ensures that logic developed for the target product will be exercised at rates high enough to uncover almost any time-related problems before the code is permanently committed to

ROMs or PROMs, says Dahlberg.

The DS100 comes in two subsystems: the -1 remote unit, which contains the system control panel, a keyboard, a display, a power supply, and a microprogrammed microprocessor implemented in low-power Schottky TTL running at 2 MHz; and the rack-mounted -2 package, which houses the system's high-speed random-access read/write memory and control logic.

With these components split up, a designer can conveniently debug the microprogram at a desk while the fast logic is mounted close to the target machine. Programs are entered through the hexadecimal keyboard or downloaded via a standard RS-232 interface. Hilevel Technology supplies software to support program development on many major computer mainframes.

Several other control features ease the development cycle. A user may single-step a routine, run it continuously, or wait until a program stop address, or breakpoint, is encountered. The local unit's memory can be loaded from a cassette. An optional feature traces a program to read back an immediate history of operations, data-bus activity, or flag status.

The basic DC100 is supplied with the customer's choice of one of two memory modules: a 1,024-by-16-bit unit with an access time of 30 ns, or a 4,096-by-16-bit module rated at 45 ns. It sells for \$4,750. Additional memory modules go for \$2,250. Delivery requires from 30 to 90 days, depending on configuration.

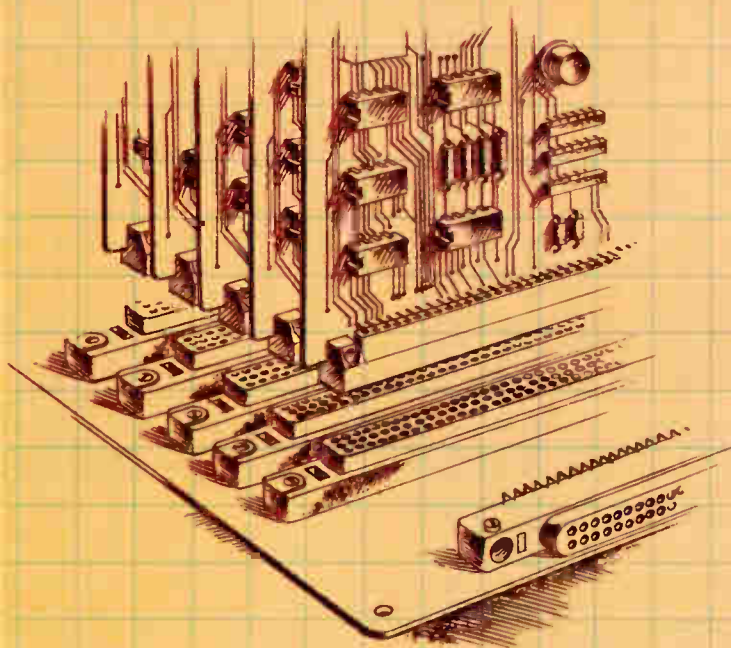
Hilevel Technology Inc., 3183 Airway Ave., Bldg. E, Costa Mesa, Calif. 92626. Phone (714) 549-4367 [411]



STD bus gets converter combo

The STD microcomputer bus was recently designed expressly for a new class of smaller plug-in modules. Last month, Analog Devices Inc. began showing the first STD module combining analog inputs and outputs. But packing 16 analog input

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Bendix Brush Connectors can streamline your printed circuit board designs. They don't require the extra board support necessary with conventional, higher mating force connectors and they eliminate the need for secondary actuation systems or procedures used with zero-insertion force connectors. Here's how:

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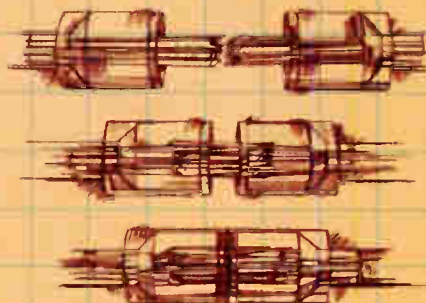
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For full information, call (607) 563-5302, or write The Bendix Corporation, Electrical Components Division, Sidney, New York 13838.

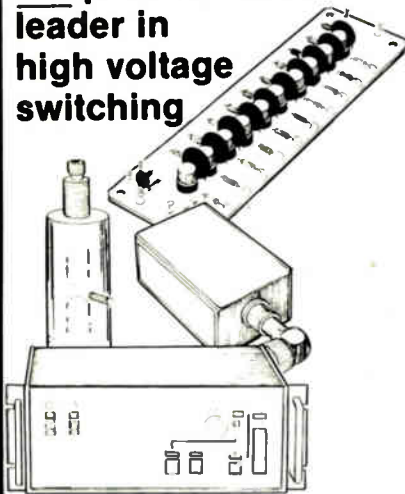


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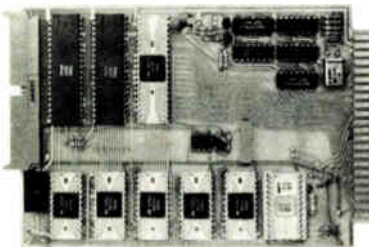
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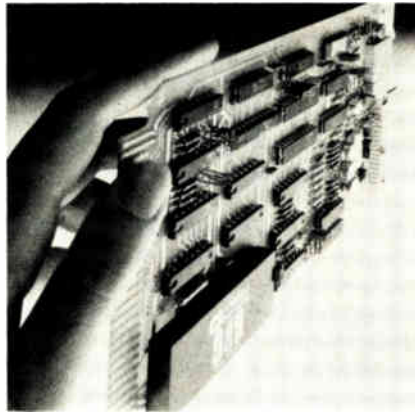
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channels and 2 analog output channels on a single 4.5-by-6.5-in. card was not easy. The solution was provided by two newly developed devices: an 18-pin monolithic 10-bit analog-to-digital converter [*Electronics*, April 13, 1978, p. 99] and a dc-dc converter that occupies an area of only 2 in.².

The STD module is the first board to use this particular a-d converter and, according to Barry Glasgow, marketing manager for microcomputer peripherals, the 10 bits suffice for the accuracy of most transducers. The chip, which is being sold separately as the AD571, is guaranteed monotonic from 0° to 50°C and has a maximum error rate of 0.15%. Also being sold separately is the dc-dc converter, the 949, with a \$145 price tag. This will supply up to 120 mA and can convert a +5-v microprocessor supply voltage into a ±15-v or +30-v one.

Another of the module's advantages is that it is memory-mapped, allowing data and commands to be transferred through a block of five contiguous memory locations, which may be placed anywhere in the processor's address space. The STD module sells for \$399.

Analog Devices Inc., Route 1 Industrial Park, Norwood, Mass. 02062. Phone Barry Glasgow at (617) 329-4700 [413]

Pascal and 8002 combine in microprocessor development

Program development may be enhanced by a Pascal programming

language now being offered for use with the Tektronix 8002 microprocessor development laboratory. The Pascal/8002 universal program development package is available for a license fee of \$2,000.

The user receives a comprehensive set of design aids, including a cathode-ray-tube screen-oriented text editor, a compiler, an assembler, a linking loader, and other utilities. The package aids in developing programs that can then be run on a variety of microprocessors.

An intermediate code, called P-code, is generated during the compilation process and can be adapted for use on microprocessors; it uses only about 30% to 50% as much storage space as machine languages for a typical 8-bit microprocessors.

Program segments are first written with the text editor and stored on floppy disks. The compiler then translates the programs into P-code format. The compiled programs can be executed and debugged on the 8002 development system hardware. The tested program segments are then finally linked together and transferred to the microprocessor under development.

The development package is available for immediate delivery.

Pascal Development Company, 10381 So. De Anza Blvd., Suite 205, Cupertino, Calif., 95014. Phone (408) 253-4280 [414]

Real-time multitasking operating system for 8086

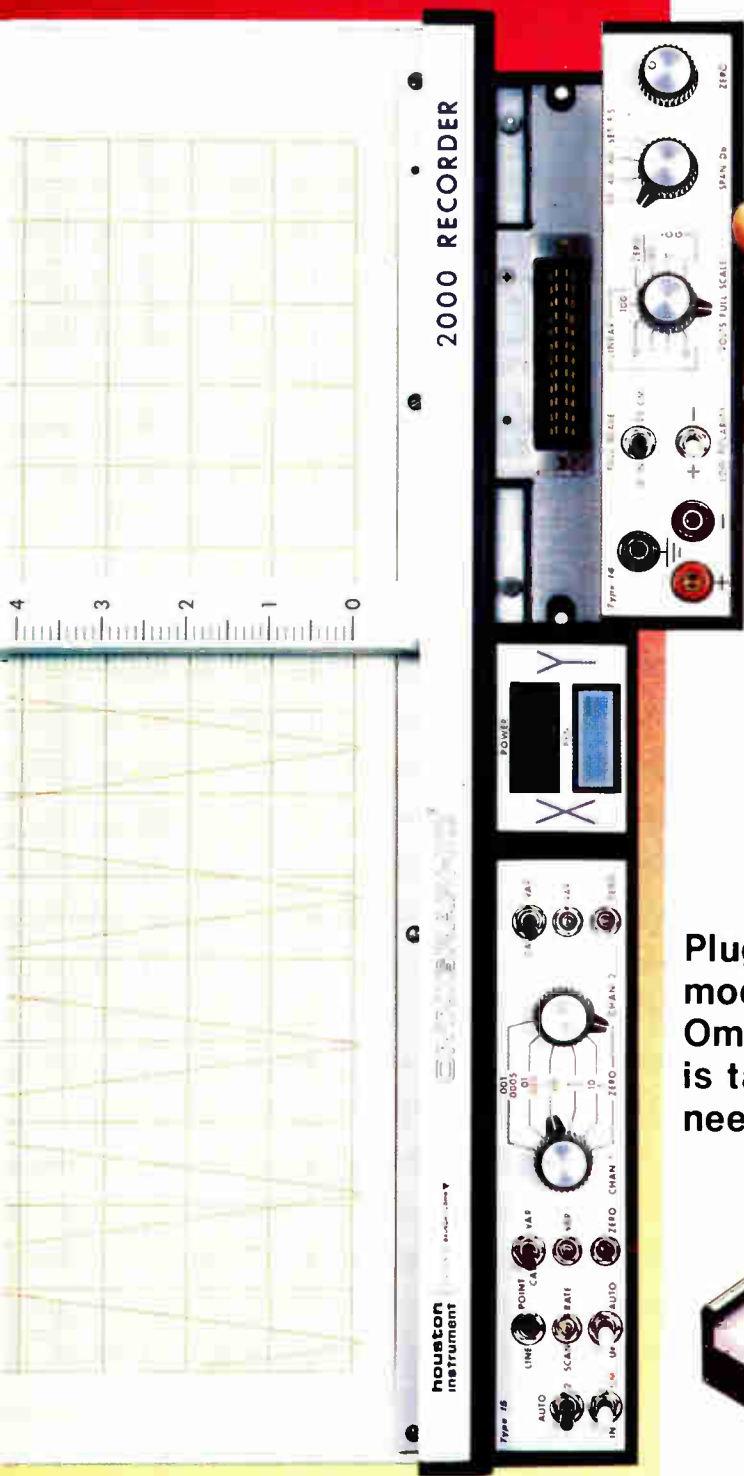
Marketing has begun for the MTOS-86, a real-time multitasking executive for the 8086 microprocessor. MTOS-86 facilities include memory management, an unlimited number of tasks, event flags, networking, and support for multiprocessor configurations.

MTOS-86, in object-language form, is priced at \$950; in source-language form it costs \$4,000. Customers may also purchase a user's manual for \$15.

Industrial Programming Inc., 9 Northern Blvd., Greenvale, N. Y. 11548. Phone (516) 621-8170 [415]

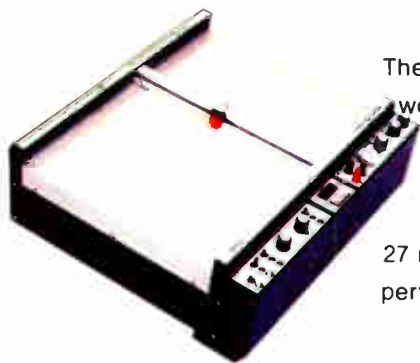
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HP adds workstations to HP300 mini . . .

Extending the ease-of-use features built into its HP300 minicomputer, Hewlett-Packard Co., Palo Alto, Calif., is adding the HP300 workstation. Identical to the cathode-ray-tube display system already integrated with the computer, **the workstation has eight "softkeys," whose control functions change according to the computer program, as well as a split-screen display and horizontal and vertical scrolling.** One mini can control two workstations, priced at \$12,500 each.

. . . and readles fiber-optic IEEE-488 bus link

For users of IEEE-488 bus links who worry about noise immunity or electrical isolation in their applications, Hewlett-Packard has developed the 12050A fiber-optic HP-IB bus link. **It converts the information on the 14-channel bus into a serial stream to be sent over a bidirectional fiber-optic cable and reconverts it into parallel form at the other end.** The system allows transmission up to 20 kilobytes per second over 100 meters with a 100- μ s response time to interrupts. Price of the converters at each end is \$1,950 apiece.

Perkin-Elmer offers Cobol for data processing

Strengthening its efforts in the large-scale commercial data-processing field, Perkin-Elmer's Computer Systems division, Oceanport, N. J., is introducing a transaction-processing software line called Reliance for applications programs written in Cobol. **The first package will be available next month in the U. S. for \$12,500 and contains data-management as well as transaction-processing software.** The automatic high-performance data manager includes automatic transaction rollback and record locking and unlocking; the integrated transaction controller supports as many as 128 terminals, running nine different tasks concurrently. Minimum configuration for this Reliance package is one of Perkin-Elmer's 32-bit processors, 256 kilobytes of main memory, and two 67-megabyte disk drives.

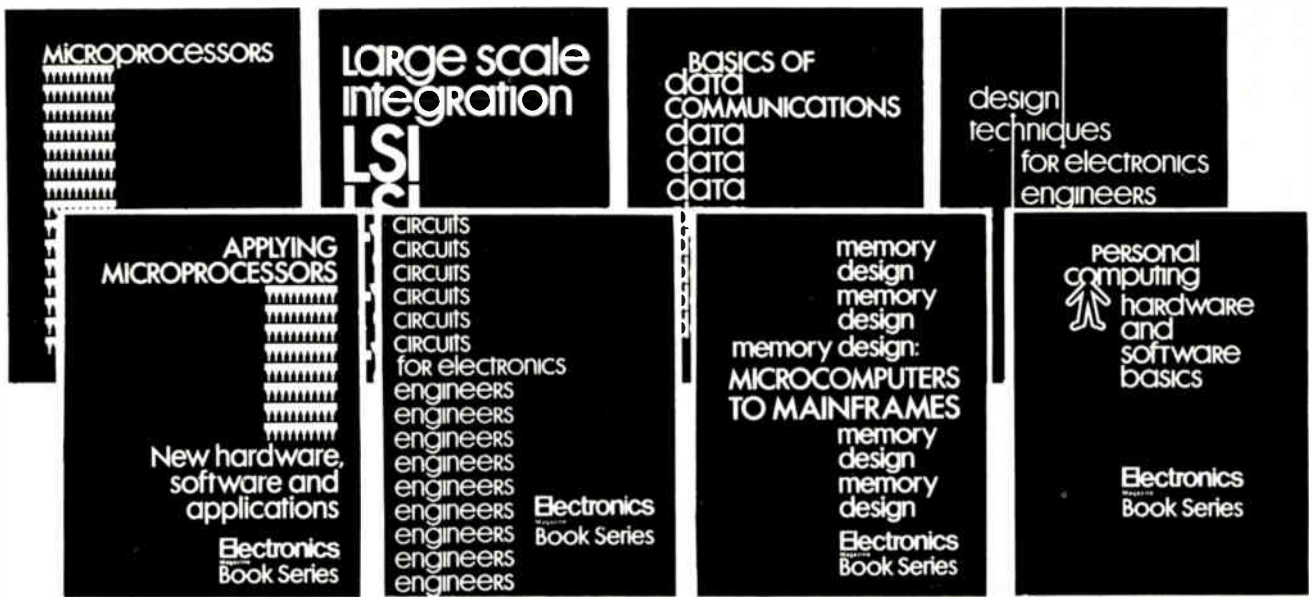
IR adds four members to power MOSFET family

International Rectifier Corp. of El Segundo, Calif., has expanded its family of power metal-oxide-semiconductor field-effect transistors with four new devices. They include the IRF350, a 400-v transistor with a continuous-current rating of 11 A, and the IRF150, a 100-v unit with a maximum on-state resistance of only 0.055 Ω . Each can dissipate 150 w continuously. Also included in the family are two 75-w units, one rated at 400 v and the other at 100 v.

Employing a planar pattern of hexagonal cells, the new MOSFETs are a refinement of the structure used for the IRF305, a 400-v, 5-A device unveiled six months ago [*Electronics*, Nov. 23, 1978, p. 235]. Prices are \$75 for the 150 and \$85 for the 350.

Computer Devices cuts prices on rebuilt printers

Computer Devices Inc. has lowered the prices on its rebuilt, telephone-compatible, lightweight printers. **The Burlington, Mass., company's 80-column model 1030 will now resell for \$1,085 (31.5% less), the 132-column model 1132 for \$1,985 (23% less).** Both units use a full 96-character ASCII font and run at up to 30 characters per second. In mint condition, the 1030 sells for \$2,785 and the 1132 for \$3,285.



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Mereco Products, 530 Wellington Ave., Cranston, R.I. 02910. Phone (401) 781-4070 [476]

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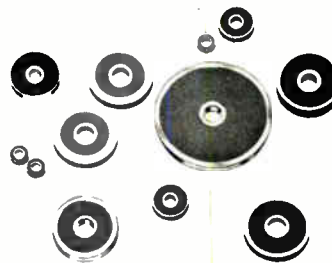
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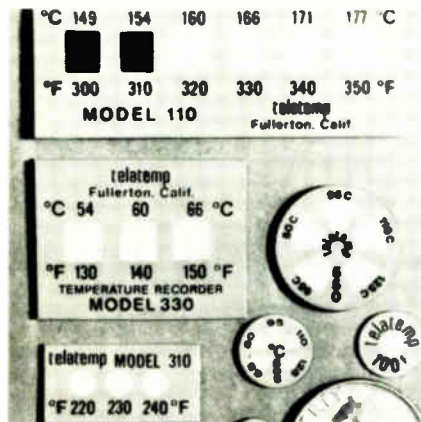
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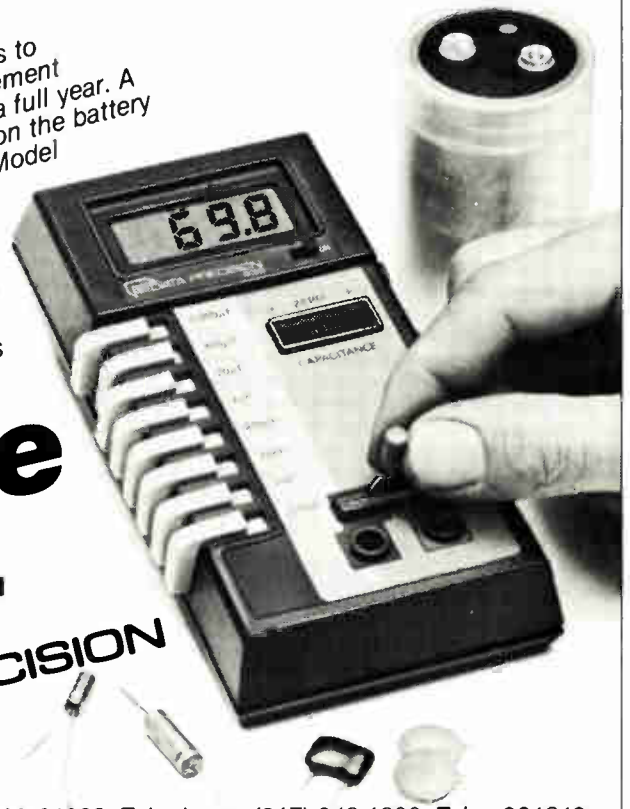


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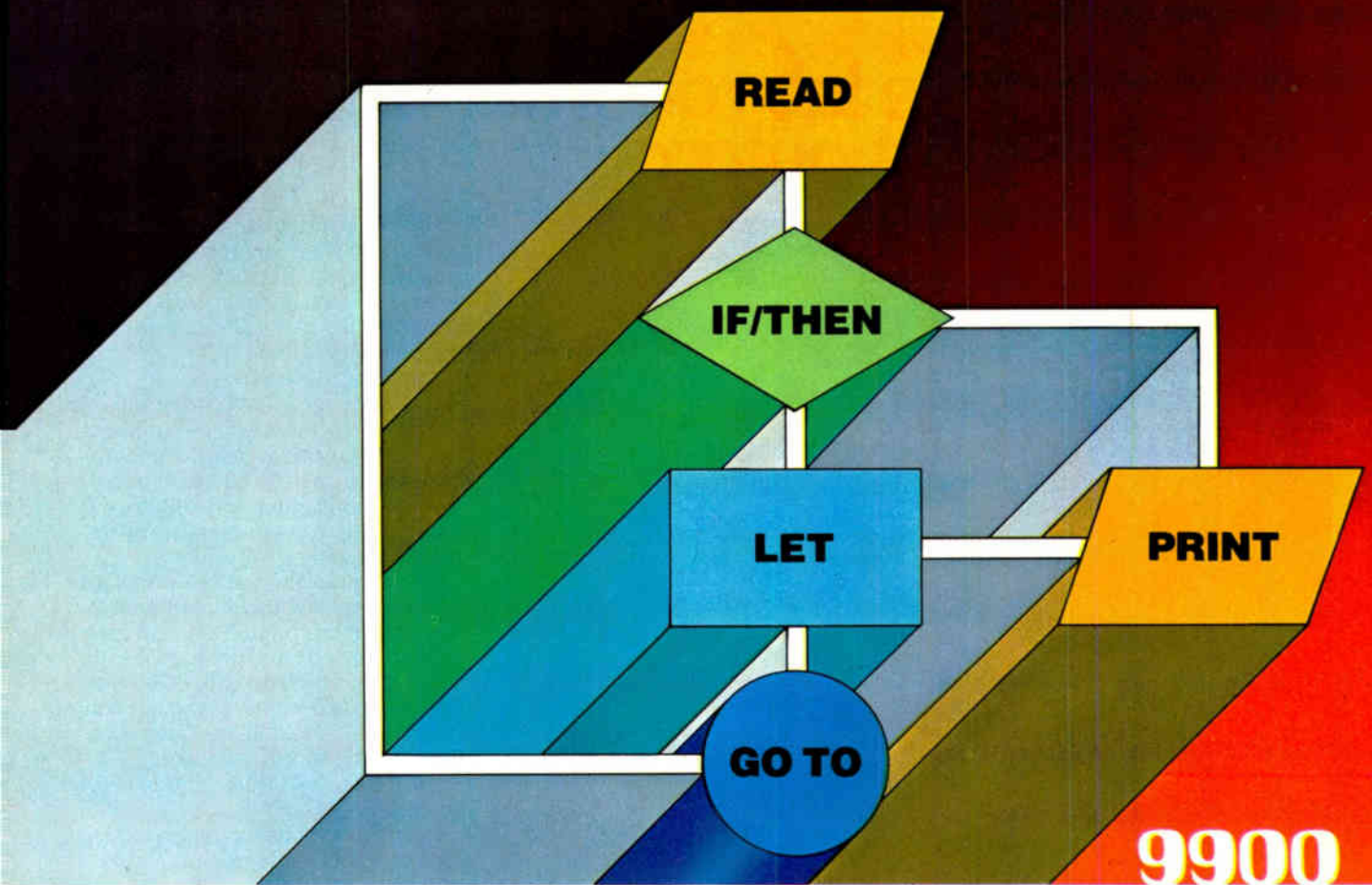
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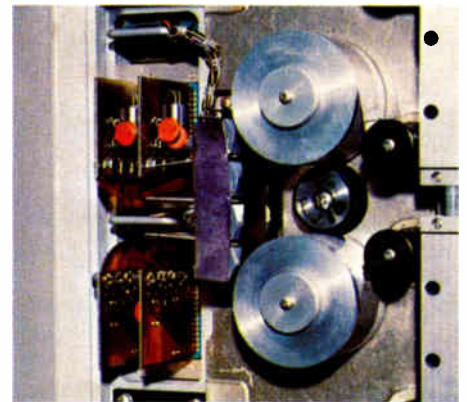
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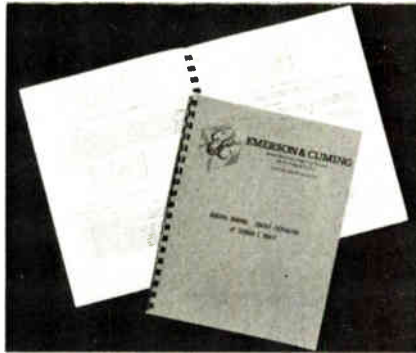
Solid-state relays. RS-443, "EIA/NARM Standard for Solid State Relays," by the Engineering Department of the Electronic Industries Association, determines and defines parameters needed to specify solid-state relays that use a single isolated input and are designed for switching ac lines up to 500 Hz in frequency, 300 V ac in voltage, and 50 A in current. RS-443 also develops uniform methods and techniques for measuring these parameters. A copy of the 67-page document is available for \$18.75 from the Standards Sales Office, Electronic Industries Association, 2001 Eye St., N. W., Washington, D. C. 20006. A free catalog of EIA and Jedec Standards and Engineering Publications is also available.

Integrated circuits. "COS/MOS Integrated Circuits Manual," CMS-272, provides detailed information on the design, operation, and application of COS/MOS digital integrated circuits ranging from simple gates to complex LSI devices. The 168-page manual begins with the fundamentals of complementary-symmetry MOS integrated circuits and then describes the circuit elements from which the more complex COS/MOS integrated circuits are developed. It gives the features and characteristics of the current RCA A- and B-series, as well as device-handling and -operating considerations. Design examples and performance data are given for COS/MOS devices in a wide variety of circuit applications such as astable and monostable multivibrators, crystal oscillators for digital timekeeping, shift registers and counters, display drivers, and digital frequency synthesizers. Copies of the manual may be obtained from RCA distributors or by sending \$5.00 to RCA Solid State Division, Box 3200, Somerville, N. J. 08876.

Wiegand effect. The "Wiegand Effect Design Guide" discusses the Wiegand effect magnetic-pulse technology and how it operates to produce voltage pulses ranging from 0.5 to 12 V with no external power source. The eight-page guide de-

scribes typical designs defining pulse output characteristics under symmetric and asymmetric drive modes. Several basic design configurations, together with drawings giving dimensions, are also included in Technical Bulletin No. 101. Sensor Engineering Co., 2155 State St., Hamden, Conn. 06517. Circle reader service number 423.

Adhesives. "Adhesive Bonding: Surface Preparation" by Leonard E. Rantz, technical services supervisor for the Dielectric Materials division of Emerson & Cuming Inc., discusses the purpose and importance



of surface preparation, theories of adhesion, requirements for a good bond, and general sequence of surface preparation. The 16-page brochure also contains several tables that list various metals, nonmetals, plastics, and elastomers that require surface preparation. Emerson & Cuming Inc., Canton, Mass. 02021 [424]

Solid-state relays. "Solid State Relays Applications Manual" contains relay definitions; sections on mounting techniques and relay packages; separate discussions of input and output electrical parameters; load considerations; a discussion of advances in the technology; and a comparison among solid-state relays, hybrid solid-state relays, and electromechanical relay components. A glossary of relay terms, as well as conversion factors for decimal, fractional, and metric equivalents, is also included in this 24-page manual. Hamlin Inc., Lake and Grove Sts., Lake Mills, Wis. 53551 [425]

Pascal. Outlined in a 34-page booklet by Tim Krouse, Electro Scientific Industries' system/software engineer, is a series of articles on the Pascal language. The booklet gives introductory concepts and program elements and presents a real-time implementation. Electro Scientific Industries Inc., 13900 N. W. Science Park Dr., Portland, Ore. 97229 [426]

Amplifiers. Specifications of single, dual, quad, and special-purpose amplifiers, along with a description of the Harris dielectric isolation process, are discussed in "Harris High Performance Operational Amplifiers Products Guide." A selection guide to amplifiers with a high slew rate, wide bandwidth, field-effect-transistor input, as well as low-power, dual high-performance, quad, and special-purpose models, is also provided in the 12-page guide. Harris Semiconductor, Dept. 53-035, P. O. Box 883, Melbourne, Fla. 32901 [427]

Enclosures. The 1979 "Off-the-Shelf Catalog" features illustrations, drawings, dimension tables, applications suggestions, options, and complete ordering information for electronic enclosures. Hundreds of off-the-shelf kits, parts, and accessories for rack-mounting and desk-top packaging systems are covered by this eight-page catalog. Under Techmar's warranty, shipping time is within three working days. The catalog, which includes a price list, may be obtained from Techmar Corp., 2232 South Cotner Ave., Los Angeles, Calif. 90064 [429]

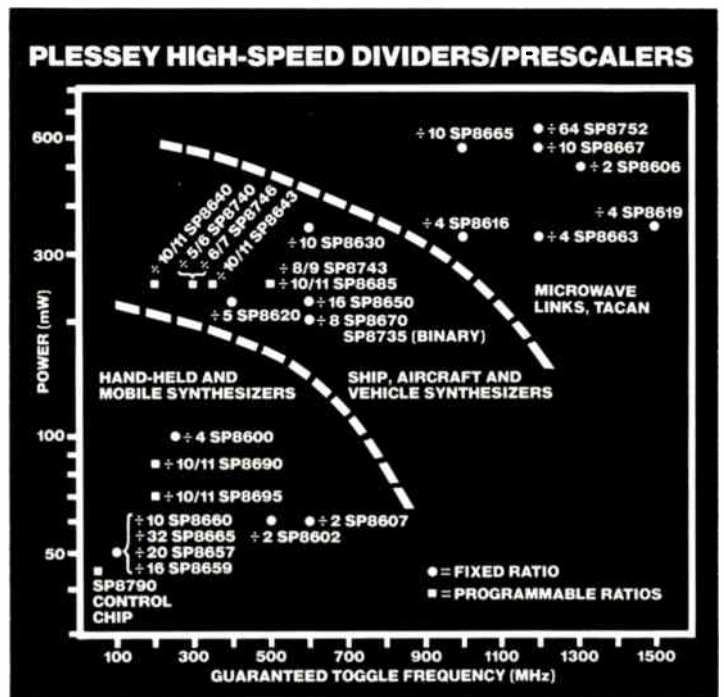
Metal powders. The selection and properties of precious metal powders are discussed in "Precious Metal Powders." This 14-page brochure presents single-metal powders; metal-oxide powders (palladium oxide and ruthenium dioxide); pseudo-alloy powders (binary silver palladium); and alloy powders (binary gold palladium and ternary gold palladium platinum). Copies of the brochure may be obtained from the Engelhard Customer Service, 2655, U. S. 22, Union, N. J. 07083 [428].

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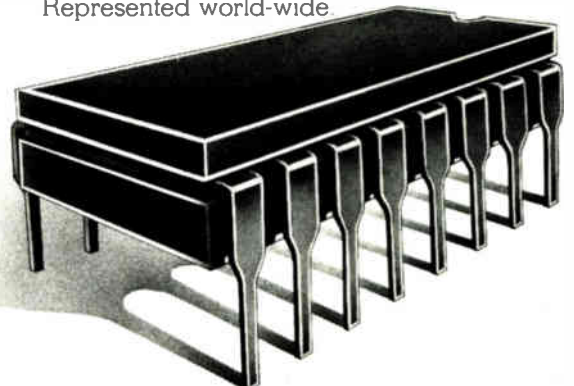
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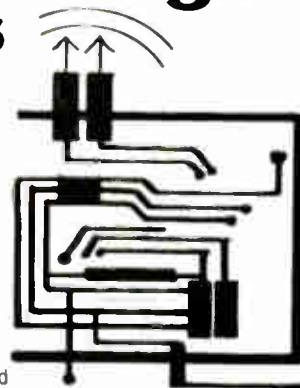
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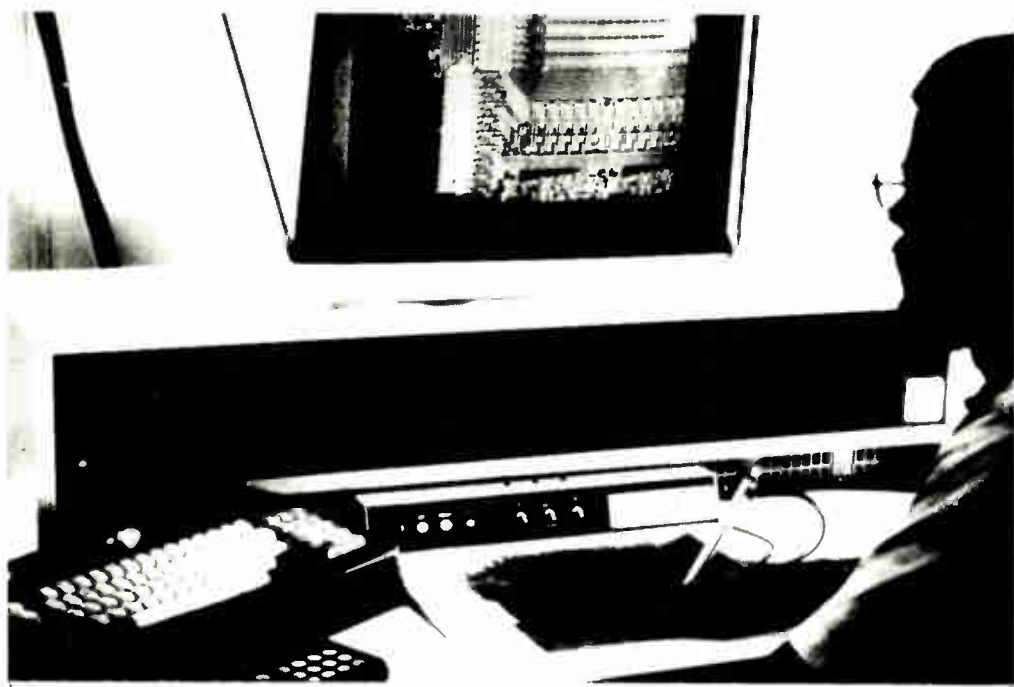
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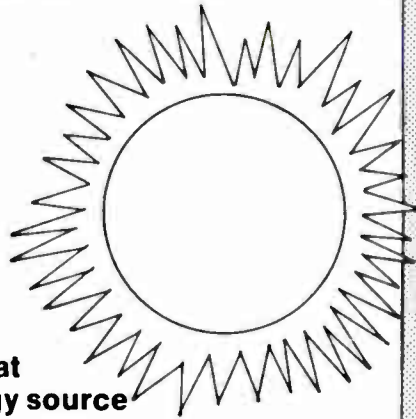
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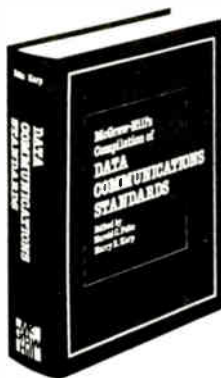
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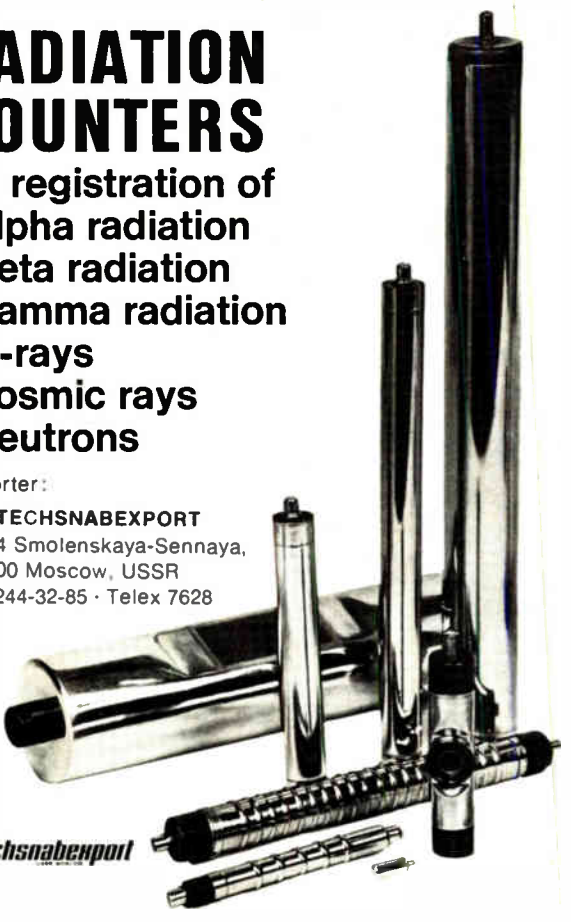
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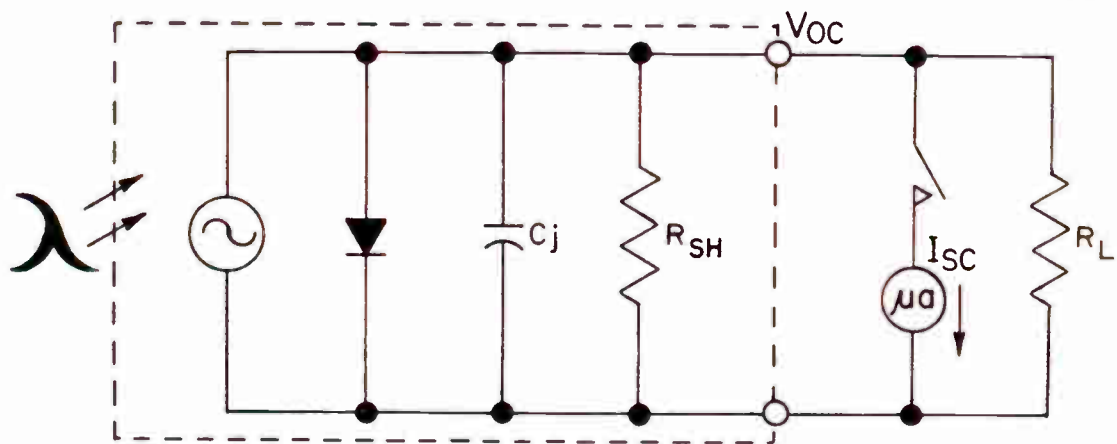
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