MARCH 1, 1979

LEAD TIMES GROW LONGER AS SEMICONDUCTOR DEMAND SOARS/91

Designing serviceability into microprocessor-based products/122

A faster Schottky logic family that cuts power loss/111

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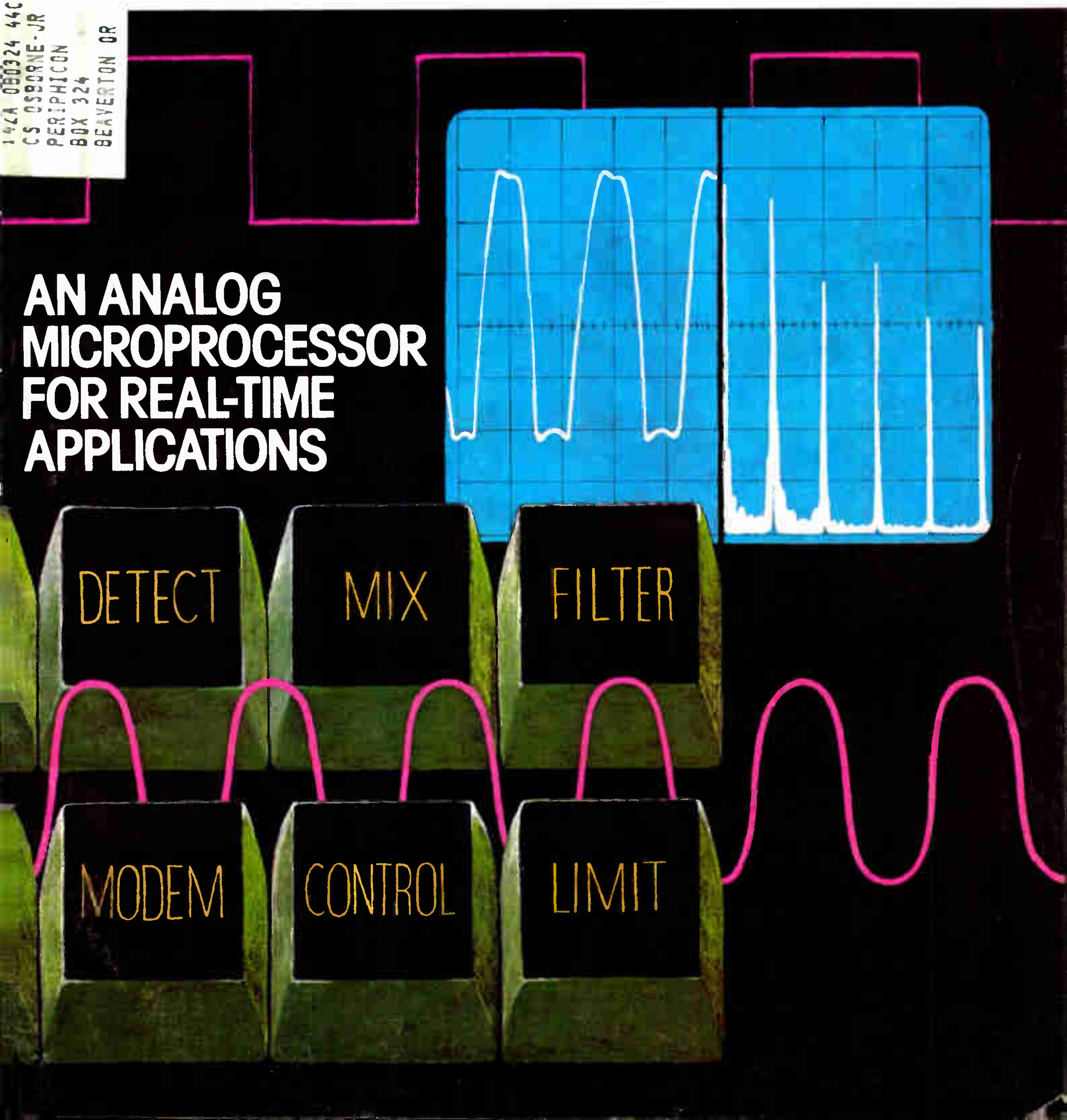

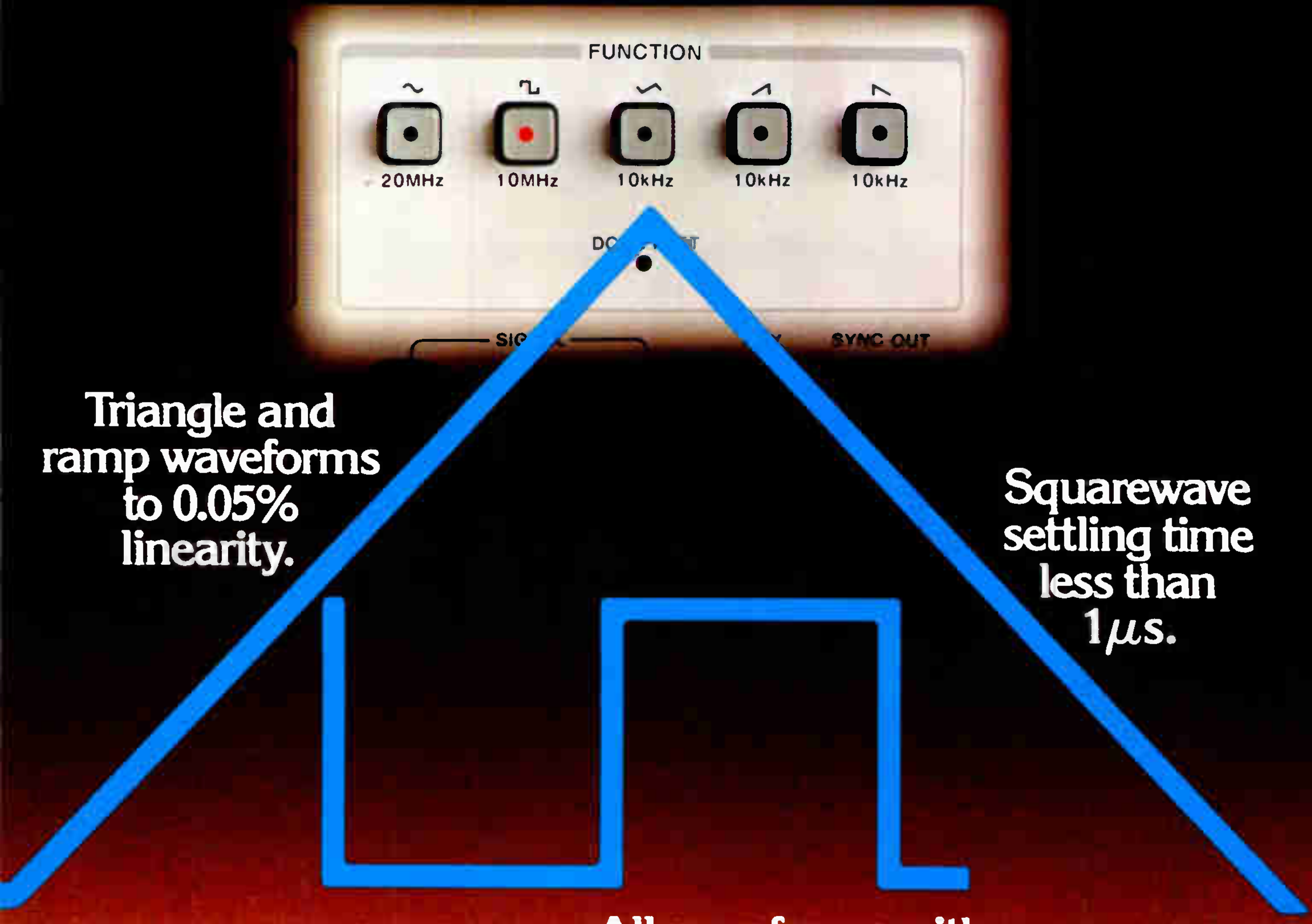

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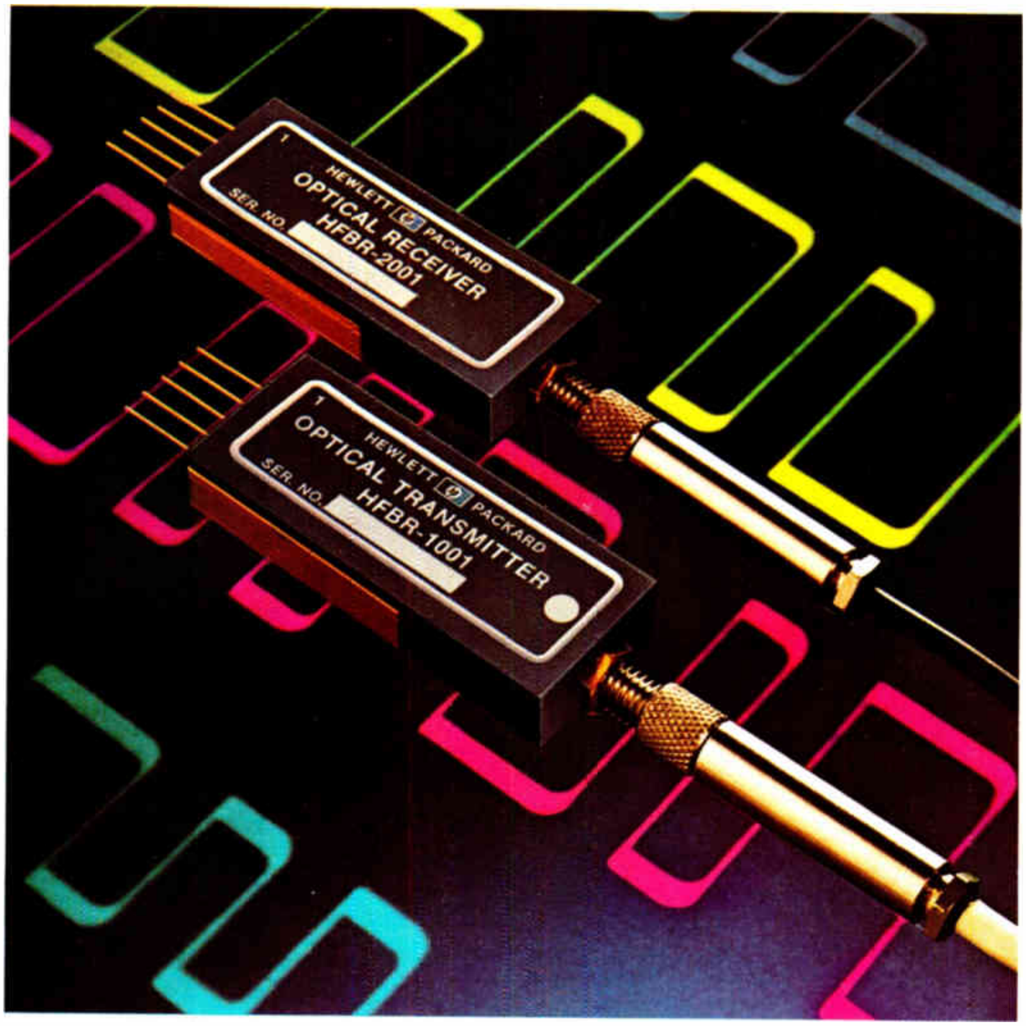

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Electronics

The International Magazine of Electronics Technology

Vol. 52, No. 5 • March 1, 1979

Highlights

Cover: A one-chip analog-signal processor, 105
Analog-to-digital and digital-to-analog converters surround a microcomputer specially designed to process signals in real time. A programmable memory customizes it for different telecommunications applications.
Cover is by Art Director Fred Sklenar.

Machines are learning to listen, 84
Researchers at Bell Labs have made headway with two systems that can reply to speech, provided the speaker talks only about airplane reservations or telephone numbers.

High-speed Schottky parts use little power, 111
Family of devices runs faster than standard Schottky transistor-transistor-logic parts but uses a quarter the power.

Remember the serviceman, 122
Mapping, signature analysis, and built-in diagnostics are all necessary in microprocessor-based systems designed with the serviceman's needs in mind.

. . . and in the next issue
A special report on the technology of the IBM System/38 . . . Forth, third in a series on high-level languages for microcomputers . . . the porcelainized-steel substrate.

Readers' comments

Read this

To the Editor: In your International Review, "Mail-sorting system reads typed addresses and verifies zip codes" [Dec. 21, p. 60], the discussion of machines used in France is incomplete.

CIT-Alcatel has also developed a LIPAP machine for the French postal service. A prototype was installed in Creteil [a small town on the outskirts of Paris] in May 1978.

It reads zip code and street address and marks the letter with two bar codes, as do the machines from Recognition Equipment Inc. It can read all fonts—typewriter, line printer, addressograph, and book print—that are used on French mail, and it handles 36,000 pieces per hour.

Joseph Pirollet
Villejuif, France

Smaller

To the Editor: The chip size of the SD1933 data-link controller is 236 by 196 mils, not 300 by 300, as indicated in my article ["Data-link control chip supports all three bit-oriented protocols," Jan. 18, p. 137]. It is, however, housed in a 300-by-300-mil package.

Bill Meronek
Western Digital Corp.
Newport Beach, Calif.

Corrections

Robert Field, former vice president of marketing at Zilog Inc., remains at the company as a consultant for marketing planning and strategy (News Briefs, Feb. 1, p. 48).

In "Coordinate converter aligns piezolectric positioner" (Feb. 1, p. 114), the resistor closest to the inverting input of A_2 must be connected directly to the x input, instead of to the output of A_1. The output of A_1 will then be $-(c+x)$, as shown.

1978 Index ready soon

The index of articles published in Electronics *in 1978 will be available shortly. For a copy, circle 340 on the reader service card.*

News update

■ The Federal Aviation Administration has started modifying the radar cathode-ray tube—commonly called plan view display—used by air-traffic controllers at some 20 en-route air terminals. The retrofit kit, consisting of a deflection yoke and amplifier, will cut power consumption by 36%, thereby greatly reducing the heat generated by the displays. The yoke allows a reduction in anode potential from 18 kilovolts to 14 kV, without increasing maximum spot size above 20 millimeters.

"Savings in power will be great: each PVD will use 450 fewer watts," says Leroy G. Walker, lead engineer for what the FAA calls its computer display channels. "The PVD will also be more reliable in terms of failure rates due to overheating," he adds.

Orwin Associates Inc., West Babylon, N. Y., is supplying the kits under a $1 million contract. It provides the deflection amplifiers and support documentation directly and has subcontracted for the deflection yokes from Display Components Inc., Littleton, Mass.

Pamela Hamilton

■ When the Seasat earth satellite, the first with a full complement of microwave sensors for monitoring ocean conditions, went down last October, there were a lot of unhappy engineers and scientists. For one thing, the bird had lasted only for 105 days [*Electronics*, Dec. 7, 1978, p. 36]. More important, even though an investigation into the failure produced reams of data for analysis, the initial finding blamed total failure of the power system on a "short circuit."

Now a more complete report has been issued. In it, the National Aeronautics and Space Administration faults the contractor, Lockheed Missile and Space Co., for not taking proper account of slip-ring failures in power supplies on other projects. Also, Seasat program policy is attacked for inadequate control and monitoring of the so-called standard bus that contained the electrical power subsystem that caused all the trouble.

Harvey J. Hindin

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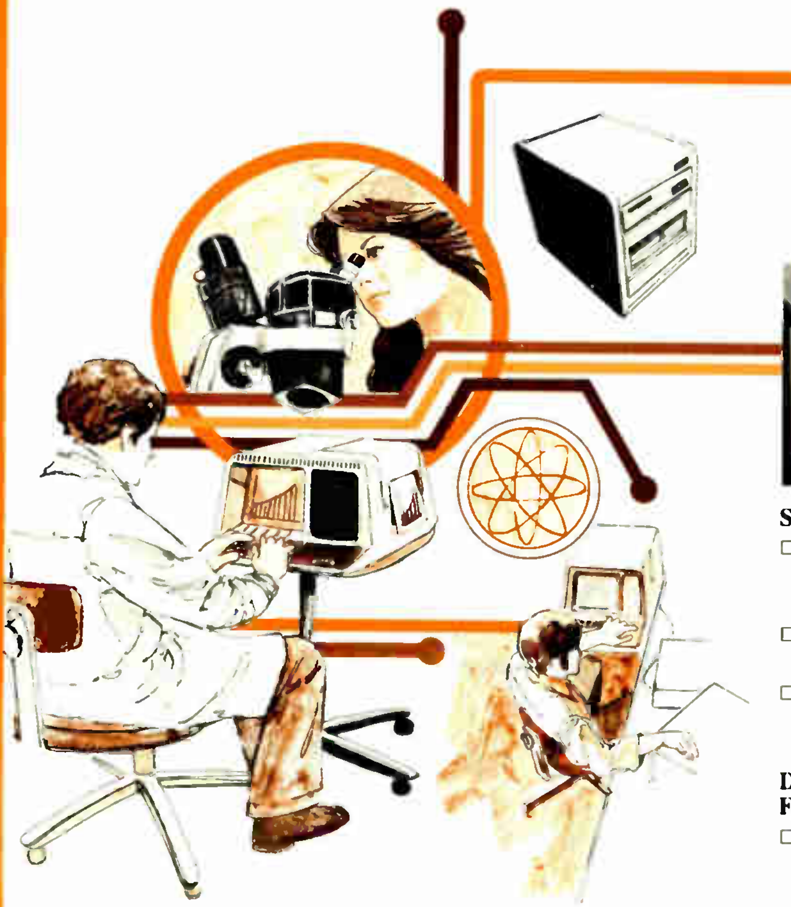

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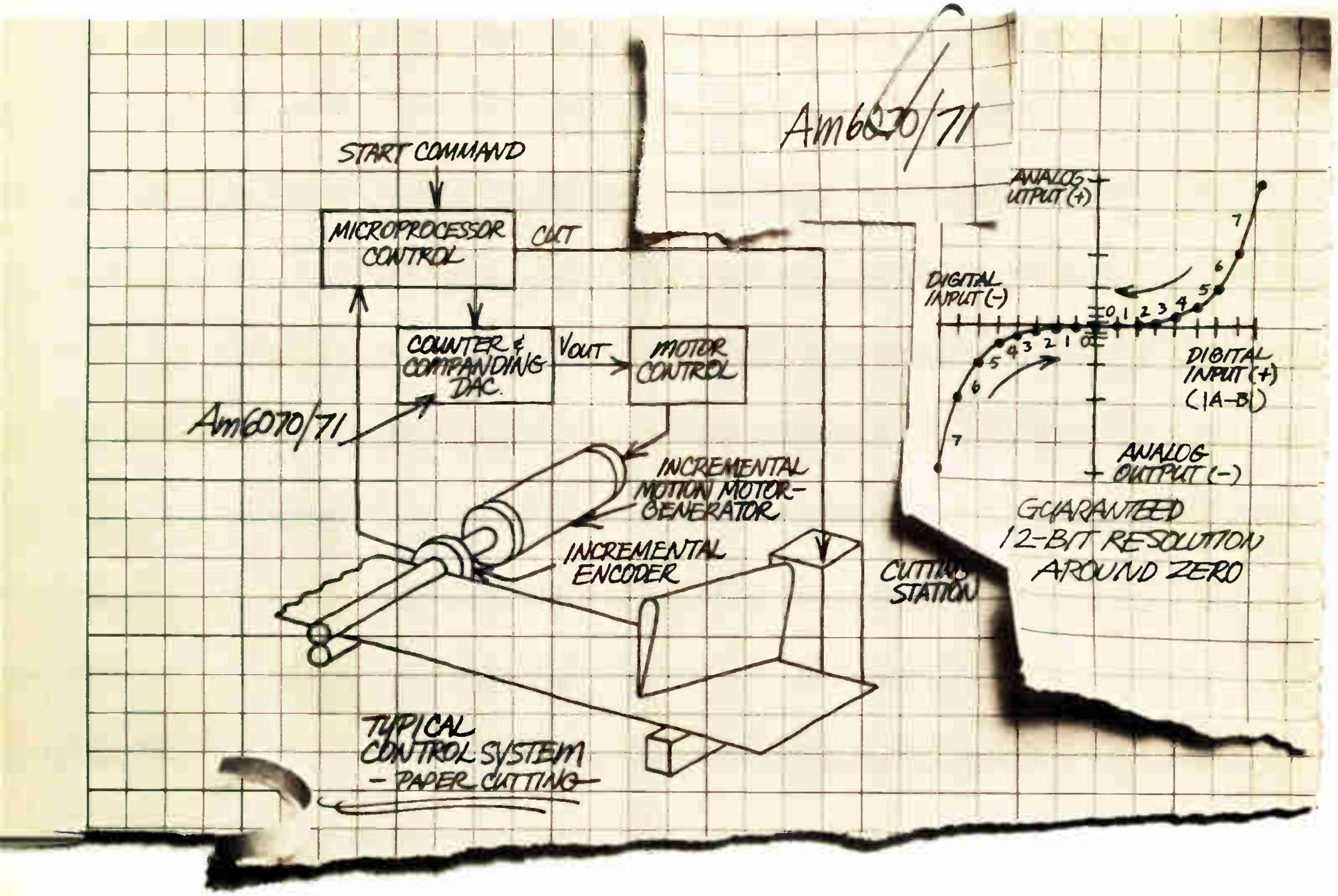

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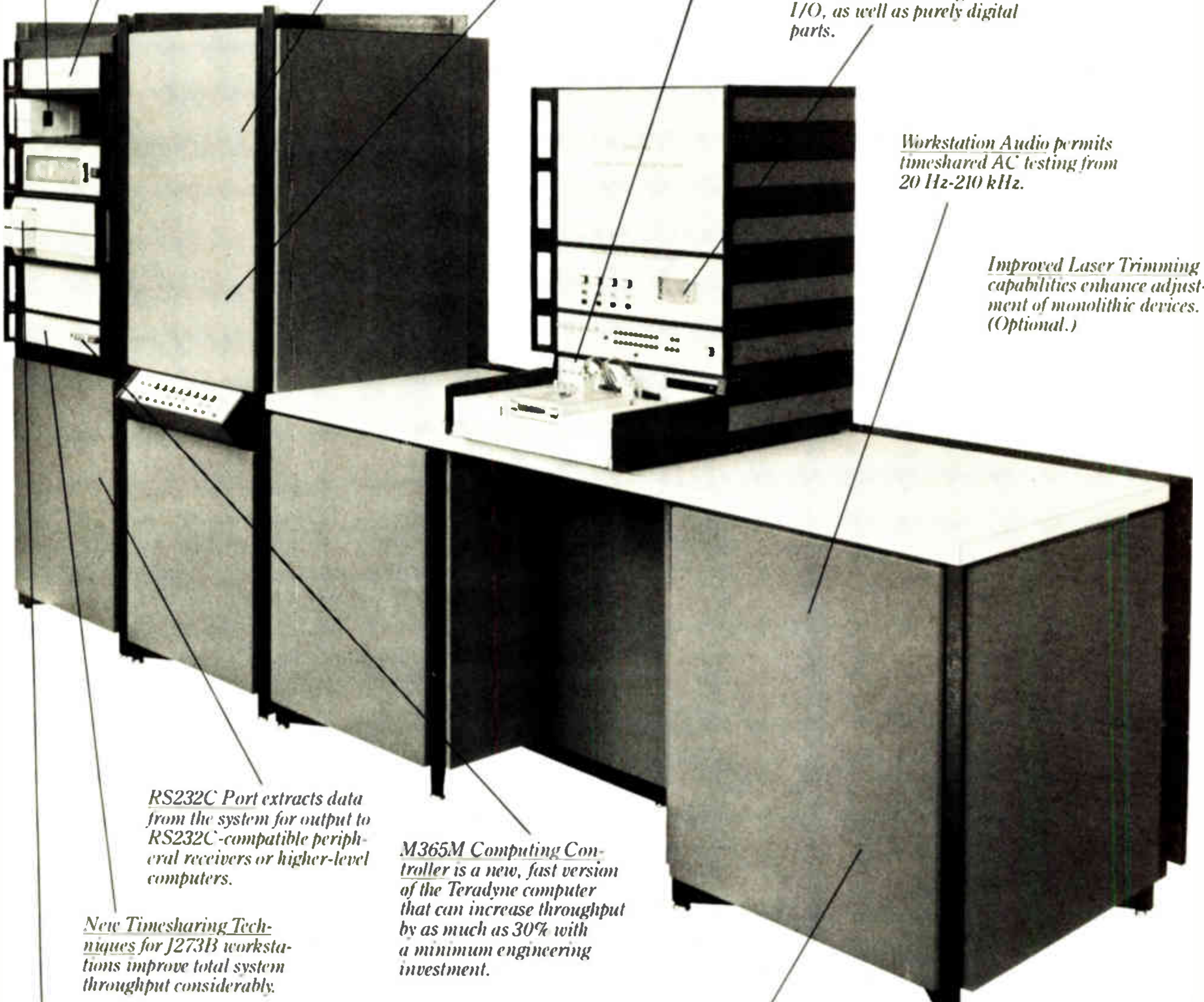

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People

Meshing words and data is Frederick Wang's goal

To Frederick A. Wang, it's a little like trying to avert the collision of two marching bands in full regalia heading toward each other. Newly appointed director of market planning and development at Wang Laboratories Inc., Lowell, Mass., Wang must figure out, first, how to keep in step and later on how to mesh two very successful product lines—one involving word processing, the other data processing.

"Integrated word- and data-processing systems are beyond the capability of people to accept today," says Wang, the 28-year-old son of company president An Wang. "It won't be until 1983 or 1984 that such systems will be accepted. The problem is what we should do with a dual product line in the intervening years."

Wang sees the two systems being integrated in two phases, beginning almost immediately with equipment already in the hands of users. "As they get familiar with the equipment, users will probably start connecting the two products themselves," he predicts. "They could, for example, set themselves up to shift data directly into memos being typed."

Wang sees his company, which had $198 million in sales last year, involving itself more and more in helping its customers integrate the systems. And by about 1983, word-processing gear will be routinely designed to handle the data-shifting function, he says.

He moves up to his new post from marketing director of word-processing equipment. He has been involved with many different phases of the company since graduating with a degree in applied mathematics in 1972. As the president's son, he even began working there at age 16. Wang sees himself now as a conductor of what he calls an orchestration of marketing people and those in research and development. Both groups will be involved with the companies who will be using the integrated products. And he wants Wang Laboratories to be slightly ahead of what those companies will need two to three years out.

Instructor. Teaching companies to be more efficient is also part of Wang's job.

He also finds himself faced with an educational challenge. The giant Fortune 1,000 companies who are his customers cannot be told simply to change their ways of doing things. Rather, they will have to realize for themselves the advantages of automating and combining secretarial and data-storage functions. Bringing them to that realization is part of Wang's job, too.

Trapnell to develop software for Amdahl

Software may no longer be taking a back seat at Amdahl Corp., the Sunnyvale, Calif., computer maker whose annual sales last year totaled $320 million. It recently added a vice president for software, Frederick M. (Fritz) Trapnell.

Amdahl's forte ever since it started nine years ago has been hardware: applying state-of-the-art circuitry to the production of computers that, while plug-compatible with big IBM machines like the 370/168, are both faster and cheap-

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New program. Software will start flowing from Amdahl early next year, says Trapnell.

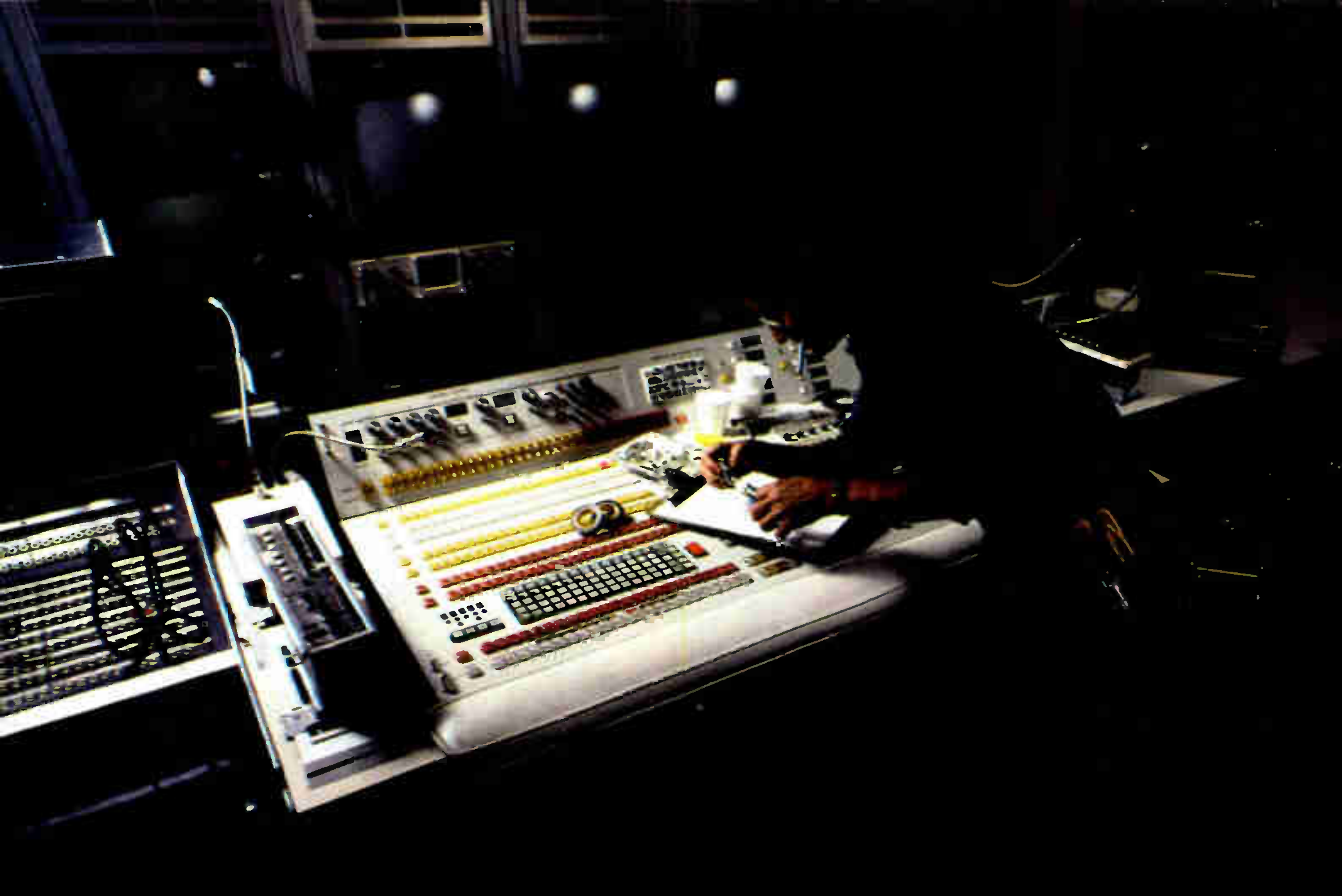
er. Its customers use IBM software.

Changing times. But Trapnell, and other industry observers, see the situation changing. IBM is starting to charge for what it has till now made available for a nominal charge or no charge at all. For example, with its new 4300 low-end mainframe [*Electronics*, Feb. 15, p. 85], IBM charges for much of the special-purpose software.

It looks, therefore, as if customers and plug-compatible makers may have to spend sizable amounts on software. (IBM may shift its revenue sources from a 95% to 5% split between hardware and software to 70% to 30%, industry sources say.)

"To keep up, we have to develop our own software," says Trapnell, who earlier in his career spent 10 years with IBM, becoming manager of the product development laboratory in Hursley, England, and assistant director of engineering for IBM World Trade. "We have to shift to remain competitive."

He also sees a new opportunity for Amdahl—introducing software products for markets IBM does not serve. "Beginning next year," says Trapnell, "a steady stream of software products" should start flowing from the growing group of software development people Amdahl is currently recruiting nationwide. □



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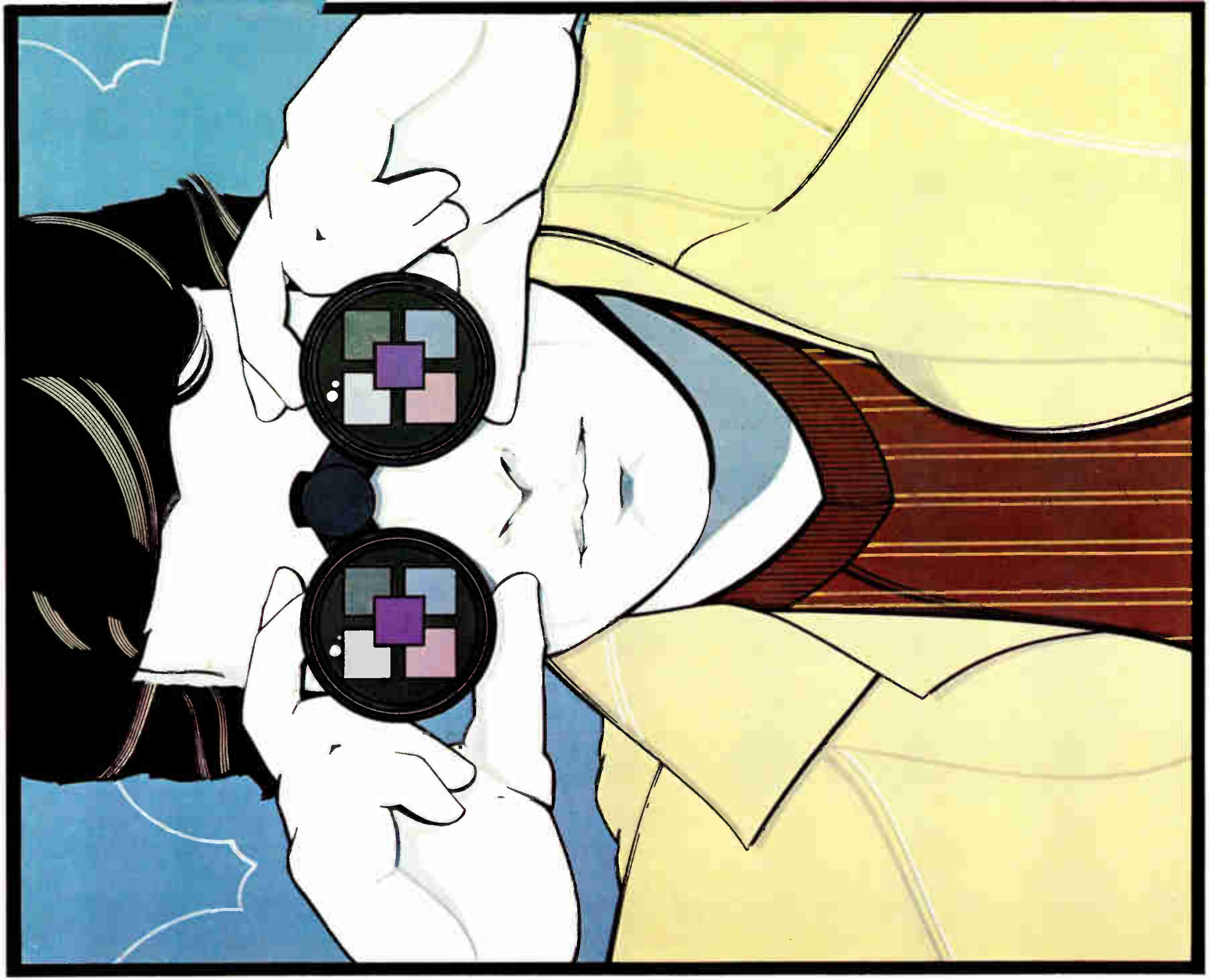

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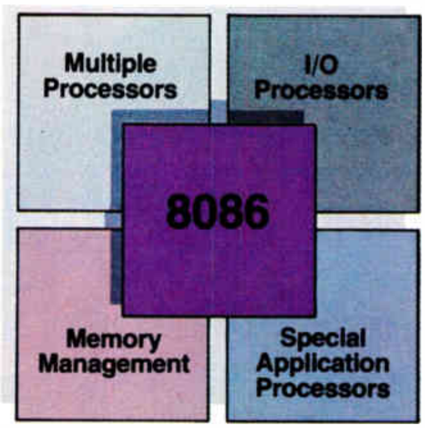

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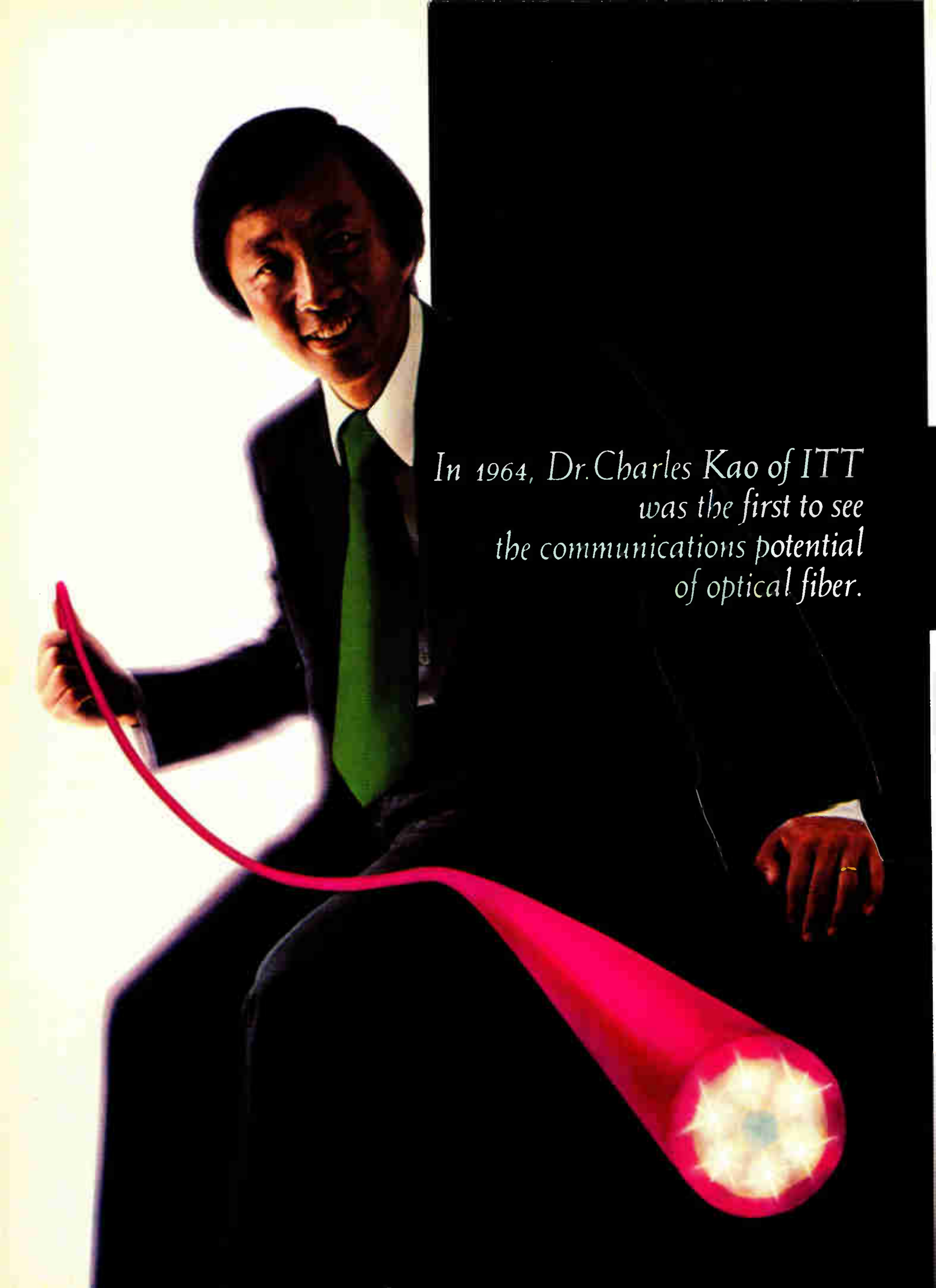
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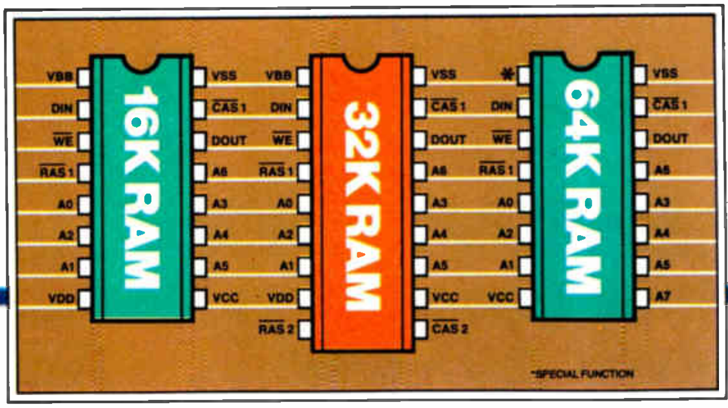

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When 64K RAMs are available, your 32K system can be totally compatible.

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You can design memory systems that interchange 4K, 16K, 32K and 64K dynamic RAMs. The MK4332, organized as 32K x 1, mounts two 4116s in leadless chip carriers connected to a standard 18-pin dual-in-line package. The two chips share common Address, Data In, Data Out, Write Enable and power pins. Separate RAS and CAS clocks for each 4116 are provided for easy device selection and control. The arrangement of all other pins is identical to the industry standard 16-pin configuration for 4K and 16K RAMs. The pin configuration is also compatible with Mostek's soon-to-be-announced 64K RAM, the MK4164.

Design in high performance.

Access time for the high density 4332 is a fast 200ns with a cycle time of just 375ns. Because both 16Ks feature an Edge-Activated™ selection mode, one chip remains in standby while the other is activated. This means the 4332 dissipates just 482mW while active and 40mW during standby. It allows a ± 10% tolerance on all power supplies (+ 12V, ± 5V).

Design with confidence.

With 16K RAMs in high volume production, you can be certain of 32K RAM availability. And alternate sourcing will soon be announced. You can count on Mostek's reliability. Mostek's 4116 quality standards set the pace for the industry. Every 16K RAM we ship is thoroughly tested to rigorous screens and stresses. With the same package dimensions as an 18-pin cerdip, the 4332 is compatible with your automatic handling and test equipment.

For more information on Mostek's 32K RAM, call your local Mostek representative or 214/245-0266 for location of the nearest sales office. Mostek Corporation, 1215 W. Crosby Road, Carrollton, Texas 75006. In Europe, contact Mostek Brussels; phone (32)02/660.25.68.

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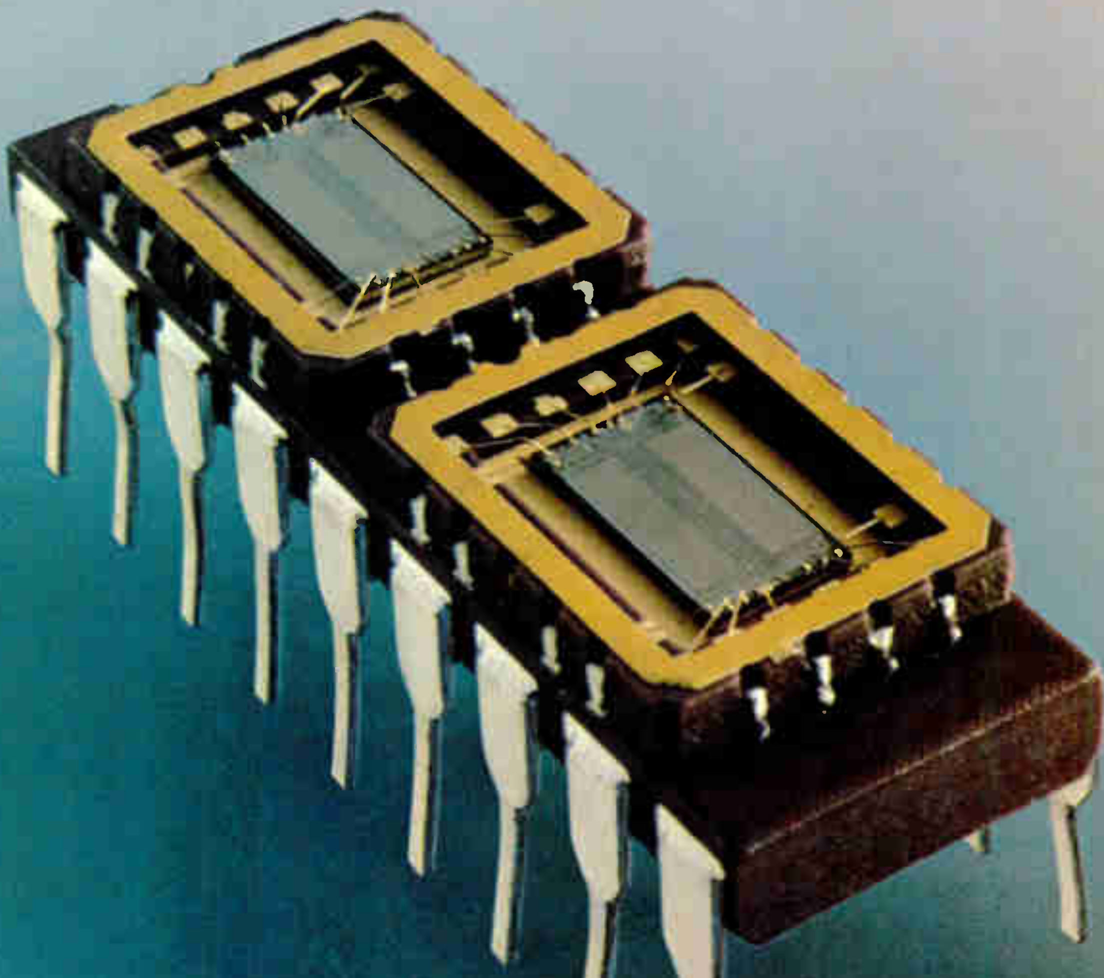

Meetings

Mid-Atlantic Computer Exposition, The Caravan Group (Newton, Mass.), New York Coliseum, New York, N. Y., March 13–15. Other Computer Expositions are scheduled for Chicago, March 27–29; St. Paul, April 3–5; San Francisco, April 17–19; Los Angeles, April 24–27; Houston, May 8–10; Charlotte, N. C., May 15–17; Pittsburgh, May 22–25; and Boston, May 29–31.

12th Annual Simulation Symposium, IEEE, Causeway Inn, Tampa, Fla., March 14–16.

Fifth Annual Conference and Exhibit on Industrial and Control Applications of Microprocessors, Information Gatekeepers Inc. (Brookline, Mass.), Sheraton Hotel, Philadelphia, March 19–21.

IECI '79—Industrial and Control Applications of Microprocessors, IEEE, Sheraton Hotel, Philadelphia, March 19–21.

Automatic Testing Deutschland and Test and Measurement Exhibition '79, Network/Watts Steadman Ltd. (London), and Gene Selven & Associates (Cupertino, Calif.), Rhein-Main-Halle, Wiesbaden, West Germany, March 20–22.

Eighth Annual Programmable Controllers Conference and Equipment Display, Engineering Society of Detroit, to be held at the society's headquarters, March 20–22.

Southwest Printed Circuits and Microelectronics Exposition, Industrial & Scientific Conference Management Inc. (Chicago, Ill.), Market Hall Convention Center, Dallas, March 21–22.

Corporate-Wide Packet-Switched Data Networks Seminar, Data Communications Magazine/McGraw-Hill Publishing Co. (New York), Capital Hilton Hotel, Washington, D. C., March 26–27.

Trends in On-Line Computer Control Systems, Institute of Electrical Engineers (London), University of Shef-

MOSTEK 3870

Because it takes 32 I/O lines to keep her contented.

"Dairy management is becoming more and more scientific. In our automated milking system, Mostek's 3870 controls three displays, numerous solenoids, a keyboard, a switchbank, valves and motors, and also provides a communications link to a larger computer." *Mike Wingert, Vice-President Engineering, Dairy Systems, Inc.*

Hewlett-Packard: "We use two 3870s in our 7225A Graphics Plotter because of their low cost, 2K ROM memory and interfacing ease. The result is an economical and highly versatile graphics plotter." *John Fenoglio, R&D Project Manager*

John Fluke: "The unique timer on Mostek's 3870 provides the one microsecond resolution our 2180A/2190A Digital Thermometer needs. The 3870 also replaces all digital IC's while allowing more features." *John Lund, Senior Design Engineer*

There are hundreds of applications using Mostek's 3870 single-chip microcomputer. Get information for your design by contacting Mostek, 1215 West Crosby Road, Carrollton, Texas 75006; phone 214/242-0444. In Europe, contact Mostek Brussels; phone (32)02/660.25.68.

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Meetings

field, Sheffield, UK, March 27–29.

29th Vehicular Technology Conference, IEEE, Arlington Park Hilton Hotel, Arlington Heights, Ill., March 27–29.

International Standard X.25 Interface Protocol for Packet Nets and Related Protocols Seminar, Data Communications Magazine/McGraw-Hill Publishing Co. (New York), Capital Hilton Hotel, Washington, D. C., March 28–29.

Southeastcon—1979 Southeastern Conference, IEEE, Hotel Roanoke, Roanoke, Va., April 1–4.

Acoustics, Speech and Signal Processing Conference, IEEE, International Inn, Washington, D. C. April 2–4.

Spring Conference, EIA, Shoreham Americana Hotel, Washington, D. C., April 2–5.

Technical Symposium East '79, Society of Photo-Optical Instrumentation Engineers (Bellingham, Wash.), Hyatt Regency Hotel, Washington, D. C., April 2–5.

22nd International Electronic Components Exhibition, Société pour la Diffusion des Sciences et des Arts (Paris), Parc des Expositions, Paris, April 2–7.

"The DOD FY '80 Research, Development, Testing and Evaluation Budget in Perspective," EIA conference, Shoreham Americana Hotel, Washington, D. C., April 3–5.

Specifications of Reliable Software, IEEE, Hyatt Regency Hotel, Cambridge, Mass., April 3–5.

Seminar on Microprocessor Applications, Continuing Education Program, Pratt Institute (Brooklyn, N. Y.), Essex House Hotel, New York, April 6.

International Symposium on Computer Architecture, Marriott Hotel, Philadelphia, April 23–25.

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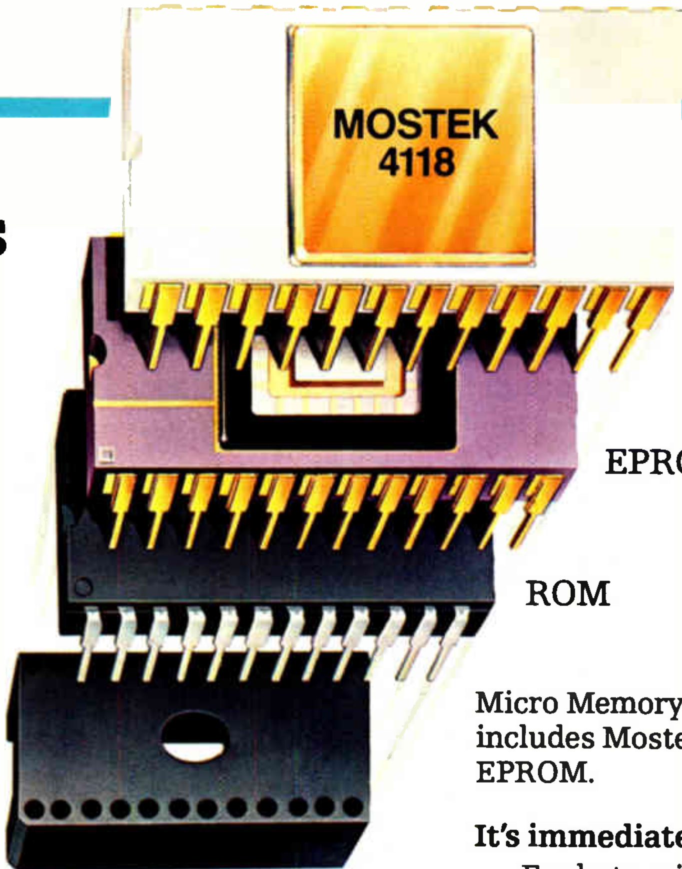

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With a pinout common to standard 24-pin ROMs, PROMs, and EPROMs, the 4118 still has more. Access time is a fast 120ns (max.) and power dissipation a low 200 mW (typ.). The 4118 is the newest addition to our compatible Micro Memory family which includes Mostek's 2716 EPROM.

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For byte-wide, memory applications requiring density, flexibility, and immediate availability, Mostek's 4118 is the one to choose. For the location of your nearest distributor, call 214/245-0266, Mostek Corporation, 1215 West Crosby Road, Carrollton, Texas 75006. In Europe contact Mostek Brussels; phone (32) 02/660.25.68.

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Editorial

Is that a cloud?

We don't think so, but could it be happening again? Are conditions in the semiconductor industry what they were just before the big slump of 1974–75?

For the answer, take a look at lead times. Then ask about double and triple ordering, inventory buildup, capacity, and the health of the venture capital industry.

Indications are that some of the pre-slump symptoms so familiar five or six years ago are beginning to recur, even though the industry now is better prepared and forewarned. For instance, inventories seem to be under better control. As reported in the Feb. 15 issue of *Electronics* (p. 48), distributors—caught between a crescendo of orders for semiconductors on one hand and the increasingly stretched-out delivery schedules on the other—are beginning to feel the strain. There is double ordering; one distributor estimates that for some key products perhaps 40% of the orders will vanish in double-order paper.

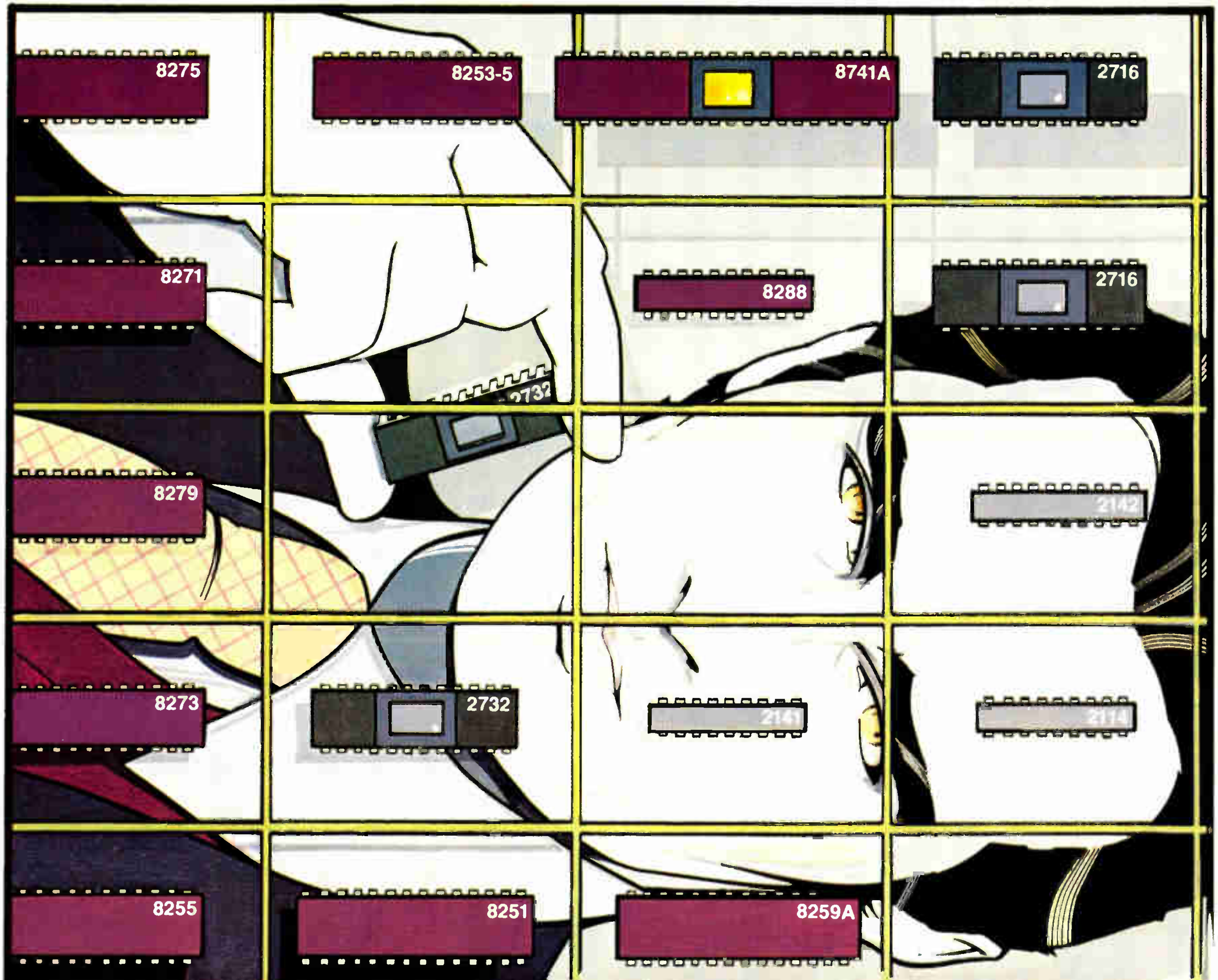
The pinch is tightest in the higher-technology devices—such as low-power Schottky, 4-K random-access memories, and some of the erasable programmable read-only memories. There seem to be no comparable problems with linear integrated circuits or complementary MOS devices, for example. This could indicate that manufacturers are underestimating the demand for the newer technologies. But some makers are letting go of established products to concentrate on new technologies. Result: trouble in both. However, lead times are also climbing on manufacturing parts such as lead frames and on capital equipment such as projection aligners and sputtering gear.

In light of all this, it's interesting to note remarks made by semiconductor executives at a meeting this month in Seattle of the Washington Purchasing Management Association. Charles E. Thompson, vice president of Motorola Inc.'s Semiconductor Group, warned purchasers not to ignore the signs. Run your business on "real customer demand," he continued, and watch inventories closely.

Speaking at the same meeting, George D. Wells, senior vice president of Fairchild Camera and Instrument Co., said that the semiconductor industry must "squeeze the amount of time it takes to get from sand to socket as hard as we possibly can." On the users' side, he recommended that more planning be done in order to give suppliers more advance information about needs.

Such remedies make sense and everyone knows about them, yet double ordering still exists when supplies get short. However much users may complain about it, perhaps the more workable solution is allocations, which a few companies are trying: everyone gets something and no one gets everything, so there's no need for double orders.

The situation has not reached the panic stage. Nevertheless, electronics firms would do well to stay alert and give themselves time to react.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8086 System Success.

Intel delivers EPROMs, RAMs and peripherals you need to start building on the Architecture of the Future.

Intel's powerful microprocessor, the 16-bit 8086, gives designers the architectural foundation to create a new generation of microcomputer solutions. The success of these system designs, though, depends on the performance and availability of compatible support components.

We understood this interdependence when, seven years ago, we invented the first microcomputer. At each step since then, our achievements in data memory, program memory and peripherals have anticipated the demands of higher performance microprocessors. Today's 8086 designs can take advantage of our full complement of compatible components to start building the systems of the future without delay.

Our EPROMs exist to support microprocessors

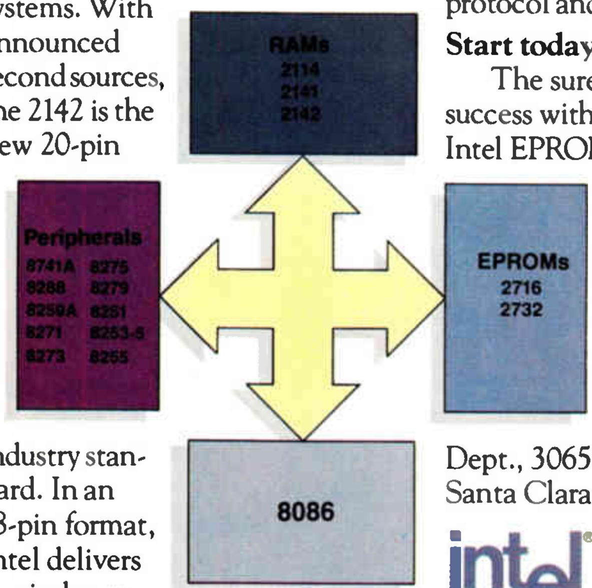
Key to practical microcomputer design is the EPROM. We invented these erasable and reprogrammable memories to make system prototyping faster and simpler. Now that the 8086 has extended the use of microprocessors to more complex data processing, the program flexibility of EPROMs is more important than ever.

Two Intel EPROMs, the 2716 16K and 2732 32K, are ideal devices for 8086 systems. Both were designed with high speed, 5-volt microprocessors in mind. And they're the only EPROMs that give designers two independent control lines to eliminate the possibility of bus contention in multiplexed and multiprocessor systems.

A RAM for every purpose

Intel delivers a variety of components to meet the data memory requirements of 8086 systems. Whether you're working in shared or multiple memory environments, Intel's family of 5-volt static RAMs gives you a full range of speed and power solutions.

Intel's 2142 (1K x 4), for example, is an ideal RAM for high performance systems. Because it has the same two-line control as our 2716 and 2732 EPROMs, the 2142 also simplifies design in high throughput, multiprocessor systems. With announced second sources, the 2142 is the new 20-pin industry standard. In an 18-pin format, Intel delivers the industry standard 2114, with access times to 200 ns and the proven performance of the most popular 4K RAM ever. For even higher speed and lower power, use our 2141. It's the 4K x 1 bit, high performance HMOS RAM that has speed versions to 120 ns, operating current as low as 40 mA active and standby current of 5 mA.



Building on 16-bit architecture

To get started quickly with 8086 designs, you can take advantage of the family of 28 interface and control components we've developed for Intel industry standard microprocessors. They include intelligent peripheral interfaces for keyboard display, communications devices and general purpose I/O peripherals. Intel controllers give you programmable command over floppy disks, SDLC/HDLC protocol and CRTs.

Start today

The surest path to system success with the 8086 is to specify Intel EPROMs, RAMs and peripherals. They're all here now. For detailed information on any of the above products, contact your local distributor. Or write Intel Corporation, Literature Dept., 3065 Bowers Avenue, Santa Clara, CA 95051.

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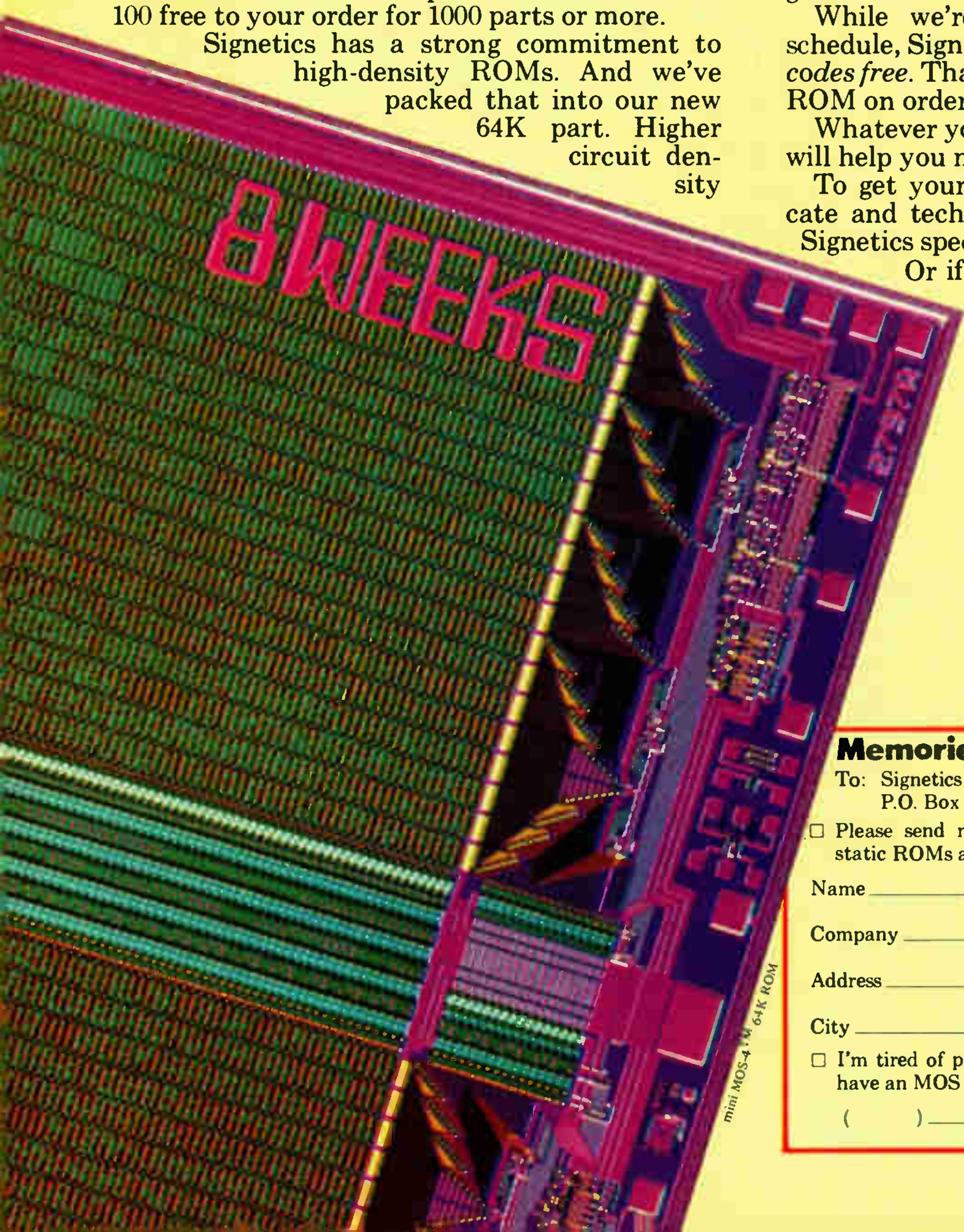

8WEEKS

Processor chip manages 8086 I/O functions

An input/output processor chip about to be released by Intel Corp., Santa Clara, Calif., is bringing the channel controller concept prevalent in large mainframe computers into the high-performance microcomputer world. Called the 8089, **the dedicated processor manages the input/output functions among peripherals and memory in real time, parallel with an 8086,** freeing the 16-bit microcomputer to perform calculations in large bus-oriented data-processing applications. Bus-compatible with the 8086 and other advanced microprocessors, the HMOS part will come in two speeds: a 5-MHz version with a direct-memory-access transfer rate of 1.25 megabytes per second and, later, an 8-MHz device with a 2-megabyte-per-second rate.

Beckman heats up DMM competition with five entries

Beckman Instruments Inc. hopes to charge into the handheld digital multimeter market with five 3½-digit models ranging in price from $100 to $190. Trying to catch onto the growing demand for handheld digital replacements for analog instruments, **the company has introduced two separate meter lines, one with two models aimed at hobbyists and the other with three models aimed at production or field service testing.**

The Fullerton, Calif., company's top-of-the-line meter, the RMS 3030, boasts the only true root-mean-square measurement capability available in these LCD-type, portable meters at present dominated by the John Fluke Manufacturing Co.'s 8020A. Four models feature instant continuity indicators and a 10-ampere maximum current range. All models have a 2,000-hour battery life.

Japan's exports up, imports down, says semiconductor report

Competing with Japanese semiconductor companies both domestically and internationally will become even tougher for U. S. and European companies, according to a survey of the Japanese semiconductor industry by BA Asia Ltd., a Hong Kong subsidiary of the Bank of America, San Francisco. The survey predicts that **Japan will have one third of the estimated $20 billion world semiconductor market in 1985** as its automated plants and the high technology from its very large-scale integration projects expand its domestic and international market shares. In the domestic market, semiconductor imports will fall as low as 10% by the mid-1980s, continuing a decline from 19% in 1977 to 17% of $2.7 billion domestic consumption in 1978, the report estimates. Between 1977 and 1978, integrated-circuit imports dropped from 26% to 23% and discrete parts fell to 19%. **U. S. companies accounted for 62% of Japan's 1978 imports,** while the U. S. market took about 40% of the value of Japanese exports in 1978.

National works on own Z80 version using C-MOS

The NSC800 microprocessor family that National Semiconductor has been discussing with customers on a disclosure-agreement basis is apparently built around a complementary-MOS processor that is plug-compatible with the 8-bit Z80. **National has whipped up an oxide-isolated two-level polysilicon process called Poly² C-MOS that it says performs with the speed of C-MOS-on-sapphire to attain the 1-μs instruction time of the 4-MHz Z80A.** Also building a 2.5-MHz version, National apparently feels there is life yet in the 8-bit design and that the price premium of a C-MOS version would be more than offset by the savings in power supplies and packaging—especially in the military and portable instrument markets.

Bubble memory conference highlights latest developments

The third annual International Colloquium on Magnetic Bubbles, which will meet March 13 to 15 at Indian Wells, Calif., will be the biggest yet—and the first to be sponsored by the Institute of Electrical and Electronics Engineers' Society of Magnetics. Highlights among the more than 14 invited papers and 36 contributed ones will include **new contiguous-disk devices from IBM (see p. 39); a bubble device that uses no coils from Bell Laboratories; and bubble-memory testing.** Next year's ICMB, meeting in September in Tokyo, will be sponsored by the Magnetic Society of Japan.

DOD may spend $750 billion by 1984 on laser weapons

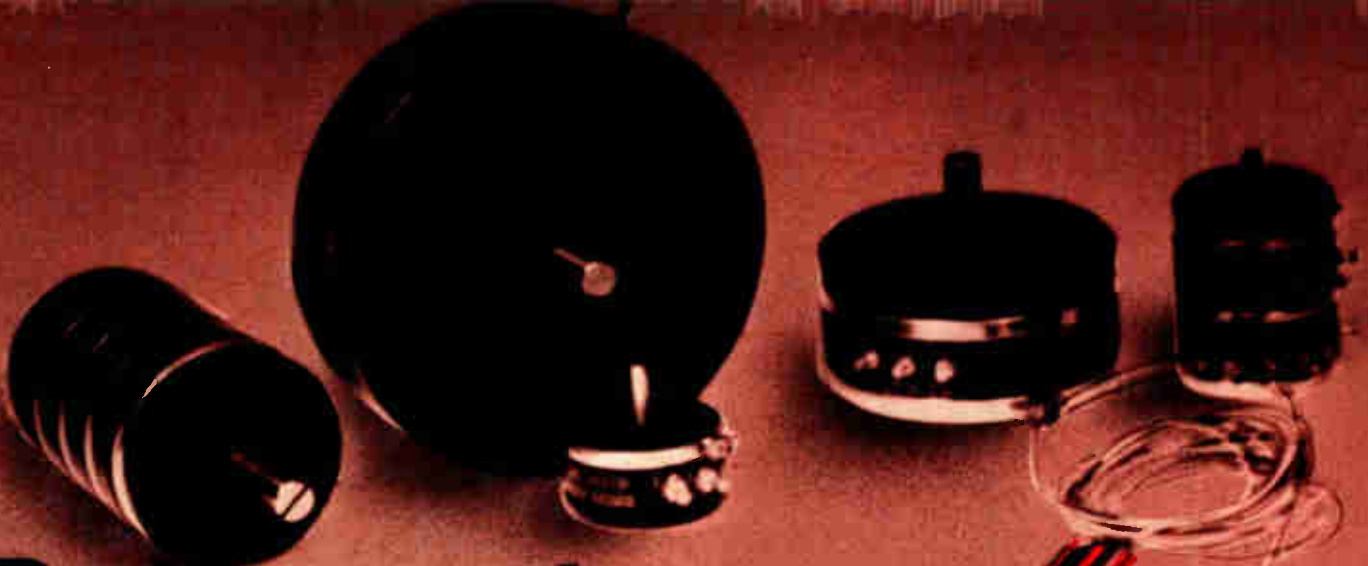
Despite futuristic make-believe in the movies, high-energy lasers and beam-particle generators are at least five years away from being weapons, according to a Defense Department official. But by 1984, $750 billion will be needed for laser development, predicts Ruth M. Davis, deputy under secretary of Defense Research and Advanced Technology. **To date, about $1 billion has gone into laser weapon R&D,** she told a session of the 1979 Winter Convention on Aerospace and Electronics held late last month in Los Angeles. "But no failures have occurred in the technology yet, only in delays in timing," she says. Particle-beam work, by contrast, still has "many uncertainties as a weapon," Davis adds.

Mostek forms military group to market memories

Militarized versions of the popular 2710 EPROM and the MK4801 static RAM will be the first new products out of Mostek Corp.'s recently formed military/high-reliability products group. Manager Glenn Carter says the 2716 erasable programmable read-only memory is to be introduced late this year, the MK4801 random-access memory early next. The Carrollton, Texas, company has only dabbled in the field previously but hopes, with a coordinated effort, an increased processing capability, and a broadened product line under the new group, **to boost its military and high-reliability billings to $4 million this year and $15 million by 1981,** up from 1978 billings of about $1 million. "We realize that military is not going to be an overwhelming part of Mostek's business, but it is significant and it is a market segment that we've chosen to attack," Carter explains. The MKB4116, which is among several Mostek products already offered to a limited number of customers in a militarized version, is expected to achieve qualification as a Joint Army Navy (JAN) device by mid-year, Carter says, the first Mostek part to do so.

DEC combines LSI-11, PDP-11/34 in microcomputer

Digital Equipment Corp. of Maynard, Mass., has designed a microcomputer having the architecture and instruction set of its PDP-11/34 minicomputer but using the LSI-11 bus and will begin shipping it this summer. **The new LSI-11/23 16-bit microcomputer can execute programs twice to four times as fast as earlier LSI-11s** and comes within 90% of a PDP-11/34 supplied without cache memory or hardware for floating-point math. Also, it is the first member of the LSI-11 family capable of handling DEC's own RSX-11M multiuser real-time operating system. Prices of the minimal system with 64-K RAM will start at $1,841 in quantities of 100.



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The LX0603D is a differential type transducer for use with non-ionic fluids to 30 psi.

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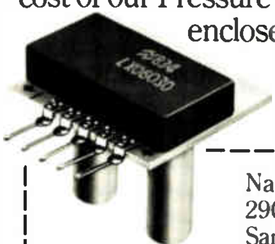

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New bubble approach shows the way to multimegabit chips

IBM proves feasibility of contiguous-disk technique; lower per-bit cost is possible using conventional lithography

With the fabrication of a 2,000-bit or so test chip, International Business Machines Corp. has shown that the best way to build multimegabit bubble chips might be with a new design approach—one employing so-called contiguous-disk bubbles. Compared with conventional bubble designs, the new scheme uses much smaller bubbles packed much closer together. However, it attains its higher density without fancy photolithography: the same photolithographic resolution needed conventionally is sufficient.

"Contiguous disks will show an immediate density advantage of an order of magnitude," contends Y. S. Lin, of IBM's Thomas J. Watson Research Laboratories in Yorktown Heights, N. Y. Pioneers in the development of magnetic-bubble memories, Lin and his colleagues will be discussing their technology in four papers to be presented at the International Colloquium on Magnetic Bubbles to be held in Indian Wells, Calif., March 12–15. To prove the technique's feasibility, they built the test chip with generator and transfer circuits and a unique bubble-stretching detector.

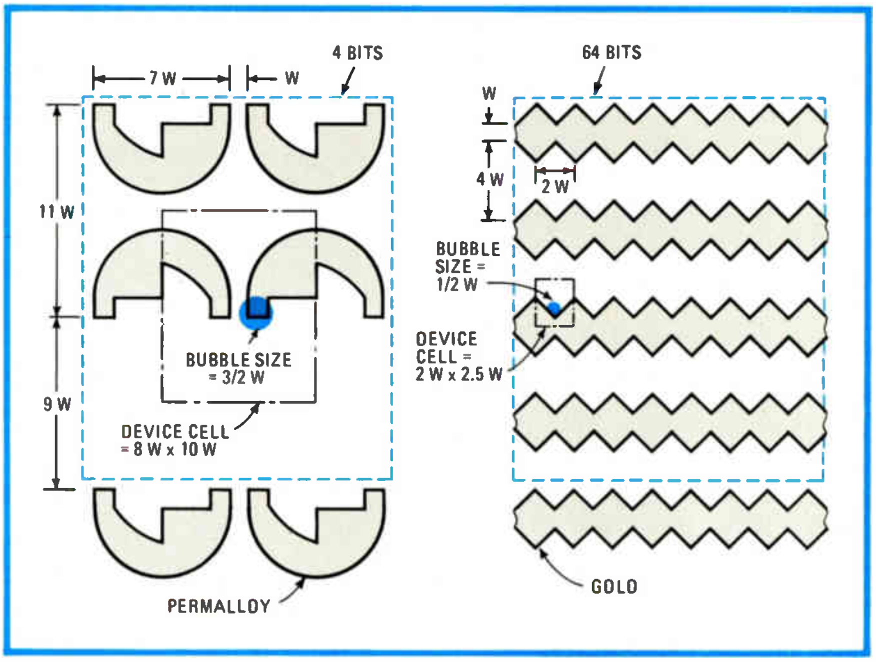
Thus far, the largest conventional chips made available commercially contain about a quarter of a megabit. By Lin's accounting, chips with about 2.5 megabits could be possible very soon. However, he declines to comment about IBM's plans for the technology.

The different approach receives its name from the shape of the patterns that guide the propagation of the bubbles. Rather than the individual chevron-shaped patterns common to all of today's bubble chips, contiguous disks rely on squiggly patterns along the chip that are shaped roughly like lines of pennies slightly overlapping one another (see p. 40). Because of this continuous-filament characteristic, contiguous disks do not need the critical interpattern spacing resolution: in fact, the resolution can be several times the bubble diameter.

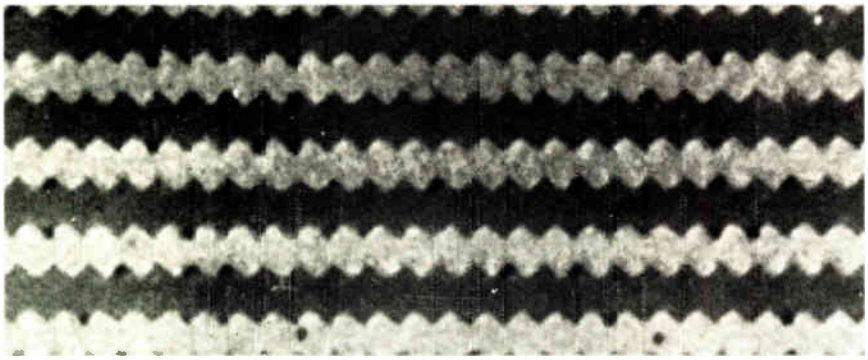
IBM has built a memory chip in a double-layer garnet structure using 1-micrometer bubbles that requires 2-μm lithographic resolution, which can be attained by optical lithography techniques with little difficulty. By comparison, chevron propagating structures would require finer features (actually the spacing between adjacent pattern islands) of one third to one half the bubble diameter.

Density. According to IBM, the storage density of 1-μm bubbles in a contiguous-disk chip is 25 million bits per square inch. With ½-μm bubbles, the density quadruples; that means that a chip of the size used for Texas Instruments Inc.'s 92-kilobit device could store 25 megabits—and still be built with conventional optical lithography.

Unlike conventional structures,



Denser. Contiguous-disk design (right) offers 16 times the bit density of conventional Permalloy C-bar (or similarly, an asymmetric-chevron) memory. Both propagating structures (tinted) have the same lithographic resolution, specified by the critical dimension, W.



Shapes to come. IBM's contiguous-disk bubble-propagating structure resembles a string of overlapping circles (light area). Circle diameter of 5 μm supports 1-μm bubbles.

which rely on the polarization of soft magnetic (usually Permalloy) patterns to push and pull the bubbles along, the propagating structures of contiguous disks are fabricated of gold. The gold actually acts as a mask, however, absorbing helium ions implanted to change the magnetic characteristics of the double-garnet substrate below.

In the presence of a rotating magnetic field (produced as in conventional bubble devices by a pair of orthogonal coils surrounding the chip), magnetized domain walls extend radially outward from the disk curves and rotate with the magnetic field to push the bubbles along as though they were caught in the blades of an electric fan.

Beyond their use for the next generation of bubble devices, contiguous disks have good long-term possibilities. The structure lends itself well to stacking layers—multiple double-garnet composites can be piled up—and therefore could be the basis for a long-awaited three-dimensional memory array with densities of hundreds of megabits. □

ISSCC

Intel to introduce n-channel RAM with power dissipation of C-MOS

Pressure from C-MOS chip makers, whose inherently low-power random-access memories are improving in speed and density, has driven Intel Corp. to make a choice. Instead of bolstering its modest line of complementary-metal-oxide-semiconductor parts, it has developed a competing lower power n-channel memory. The Santa Clara, Calif., manufacturer has a 4-K RAM design boasting a standby power dissipation of only about 40 microwatts.

Intel disclosed the design of its new RAM, available in a few months, at the International Solid State Circuits Conference in Philadelphia last month. (This review and the three that follow are based on information disclosed at the conference.)

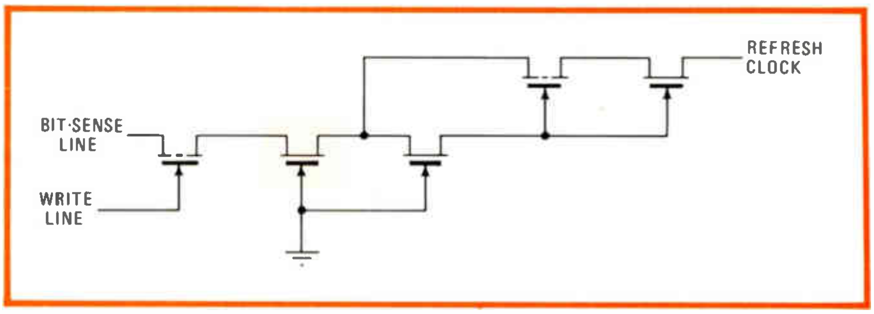
Intel's 4-K-by-1-bit model 2151 gets its low power consumption through several new circuit twists. For one, the part is pseudostatic, using dynamic data storage with a self-refreshing scheme that gives the device the appearance of an easy-to-use clocked static memory.

Also, the chip-enable buffer circuit, which powers down the device and translates TTL into MOS signal levels, dissipates no power in standby. Finally, an on-chip negative-bias voltage generator, which allows the part to operate off a single 5-volt supply, draws only about 5 microamperes—far less than that drawn by the usual charge-pump circuits.

Separation. Unlike other pseudostatic designs [*Electronics*, Feb. 15, 1979, p. 40], which combine an array of one-transistor dynamic cells with peripheral refreshing circuitry, Intel's part is based on a unique five-transistor cell that separates the refresh line from the read/write line. The internally generated refresh signal operates independently and asynchronously of the read and write signals, with no contention problem.

The cell is based on a design by H. J. Boll at Bell Laboratories, which has a cross-licensing arrangement with Intel. As diagrammed in the figure, the tinted depletion-mode transistor is the cell's storage capacitor, which must be refreshed. If the storage transistor is void of electrons (storing a 1), the rightmost transistor will be turned on, since its gate will be capacitively coupled high. Pulsing the refresh line high allows electrons that have leaked into the storage transistor to discharge through the adjacent enhancement-mode transistor, and thus the cell is refreshed.

If the storage transistor is full of electrons (storing a 0), the enhancement-mode transistor never turns on and no current is drawn from the refresh signal. No arbitration problem exists because refreshing can occur even while the cell's data is written over.



New cell. Transistor (tinted) serves as dynamic storage element in this five-transistor low-power RAM cell. Internal refreshing is oblivious to read or write operations.

The static chip-enable buffer requires an active-high signal, different from the active-low standard of 4-K RAMs. (Intel hopes to appease users by offering memory-decoding chips with active-high chip-enable outputs.) But with that and with several additional transistors to boost speed and provide logic-level translation, no current is drawn during standby.

The secret of Intel's back-bias generator is an efficient circuit with a slowly switching 200-microsecond clock to reduce current spikes.

Although the 2151 (and 2152, organized as 1-K by 4 bits) uses a five-transistor cell, Intel claims that it can build a chip significantly smaller than a static C-MOS one, which uses the standard six-element flip-flop. The Intel cell, at 1,400 square micrometers ends up in a 23,400-mil² chip. By comparison, the current 4-K part from Harris Corp. is 31,700 mil², and Toshiba Corp.'s is a whopping 48,400 mil². Hitachi Ltd. has built a 6147 that at 17,000 mil² is markedly smaller than Intel's part, but it mixes n-channel and bipolar technologies. □

Phase shifter goes full 360°, 8 to 18 GHz

A small, microwave-product development company in Farmingdale, N. Y., has developed an analog phase shifter for a military microwave application that has just about everything a designer could ask for—an extremely broad bandwidth of 8 to 18 gigahertz, linear electronic tunability, a full 360° of phase variation—all fitted into a single box.

This is what Samuel Hopfer of General Microwave Corp. has done for the phase shifter going into a target simulator that the Boeing Co. is putting together for the Naval Research Laboratory.

The device is also fast and accurate. Its phase shift is provided in less than a microsecond and even this figure can probably be improved by redesigning the electronic-tuning drive circuitry. Its accuracy is equivalent to that of an 8-bit device in the Boeing application—or 1.5° accuracy—and this figure, too, may be lowered—12 bits, or 0.1°, not being inconceivable according to Hopfer.

It is done with 24 high-quality-factor (Q) unpackaged varactor diode chips from Microwave Associates, Burlington, Mass. Hopfer is able to make the small, individual phase contributions from each varactor add in such a way as to yield the 360° of phase shift. First he calculated what the ideal varactor equation relating phase shift to varactor capacitance, which varies with voltage, should be.

Then, although the equation required for flatness and the actual varactor equation of course did not agree, he was able to approximate the needed relation by operating each varactor over only a small portion of its range. Finally, he put 24 of them in 18 hybrid circuits, which added their phases properly to provide the overall amount of phase shift. He wanted the overall device phase shift to be flat as a function of frequency, and he got what he wanted.

Chains. Hopfer actually uses two balanced chains of microwave hybrid circuits. Each chain has six of the hybrids arranged in three successive sections of two hybrids per section. Six more hybrids are used for signal-splitting and -combining functions. The circuitry is on microstrip transmission line—the technology of choice in the 8-to-18-gigahertz range so that microwave integrated-circuit procedures can be used.

No new microwave process technology was required, although Hopfer declines to discuss the design of the individual hybrids. "The varactor is the only device suitable for such an analog phase shifter at the present time," he says. Industry comment at the International Solid State Conference supported his view. Not only could the specification be obtained in no other way, but the 24 varactors required only a single tuning voltage. What's more, the full 360° shift was obtained by varying the voltage from −5.79 to −34.53 volts—a quite acceptable range. □

Photons switch phone switch

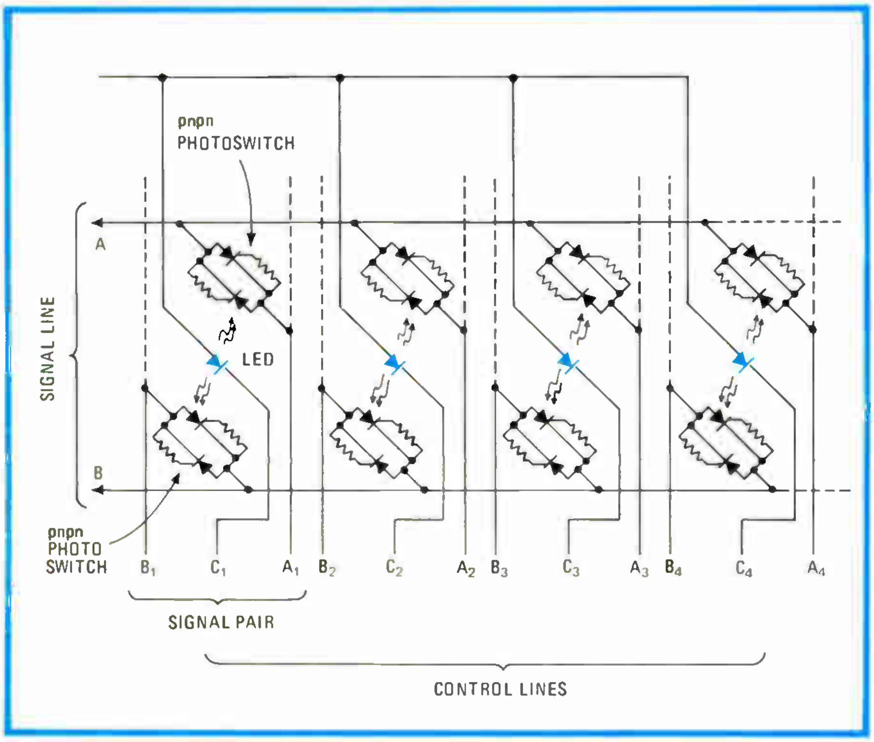
Price is the name of the game when it comes to the switching circuits used to route calls from one phone to another. Lower-cost switching matrixes, which developed from levers and bars into electromechanical and solid-state devices, are therefore always under study.

In the latest of these efforts, Haruo Marui of the Oki Electric Industry Co. of Tokyo, Japan, has built a switching matrix around light-emitting diodes and phototransistors. It not only promises low fabrication cost because of its integrated-circuit technology, but also has no noise between signal and control lines.

Marui and his co-workers Toshimasa Ishida and Kazuo Hagimura of Oki, along with Seiei Ohkoshi and Kotaro Kato of the Nippon Telegraph and Telephone Co. (also in Tokyo), revealed their work at last month's International Solid State Circuits Conference. With their switching array, a duplex voice line can be switched to any one of four channels, as shown on page 42. This is not a unique accomplishment. But the technique has major technical advantages over integrated-circuit approaches tried so far.

Past IC approaches used either low- or high-voltage current triggering of transistors to provide the signal paths. The transistors' intimately coupled switching and signal functions were poorly isolated, resulting in unacceptable noise. Moreover, because of inconvenient impedance levels it was difficult to connect the transistor and its circuitry directly to a telephone, or even to connect to it to perform simple maintenance tests.

Marui's design overcomes these problems. The signal path is switched by pnpn phototransistors actuated by a light pulse from a separate diode. Thus, isolation is perfect. In operation, a voice signal



Switch. Separate chips containing LEDs and phototransistors are used by Oki engineers in fabricating telephone matrix switch that isolates signal and control lines.

on line A–B may be switched to either of lines A_1–B_1 through A_4–B_4 by pulsing any of control lines 1 to 4, turning on an LED. When the LED fires, its two associated pnpn arrays conduct, allowing duplex transmission from signal lines A–B to, say, A_2–B_2.

There is no current leakage from the switching circuit into the voice channel to disturb conversation. In addition, the telephone can be connected directly as the impedances are either very low or very high.

The LED, made with liquid-phase epitaxy on a gallium-arsenide substrate, is designed to emit light in wavelengths matching the photosensitivity of the silicon-based phototransistor. The coupling efficiently allows for an LED triggering current of less than 20 milliamperes—a value easily compatible with low-cost transistor-transistor-logic circuits.

More work. "A one-by-four matrix was chosen as a convenient starting point but further work will be done to design two-by-four and four-by-four versions," Marui says. And it seems to him that other sizes could be made just as well.

At present, the LEDs and pnpn phototransistors are mounted on separate substrates because of difficulty in combining gallium-arsenide and silicon technology. "So the separate chips have to be carefully aligned for everything to work," Marui says. He expects production of the one-by-four matrix within a year.

"The near-term applications will be in line concentrators and private branch exchanges," Marui says. "Applications in switches with thousands of switching points will have to await further work on crosstalk and electrical loss, as well as reduction in the switching matrix capacitance."☐

LCD watch doubles as a heart monitor

Another digital wristwatch that measures heart rate is in the offing. Designed around a hybrid substrate that contains the timekeeping, display, and plethysmograph electronics, the watch promises to be much less expensive than the $500 version that Pulsar introduced two years ago [*Electronics*, April 28, 1977, p. 32], just before it dropped out of the digital watch market.

The key to the watch, which could sell for just $30 more than a regular liquid-crystal-display unit, is a custom micropower complementary-metal-oxide-semiconductor integrated circuit developed at Hughes Aircraft Co.'s Solid State Products division, Newport Beach, Calif. To measure heart rate, the user places an index finger on an optical sensor located on the face of the watch (see photo on p. 44).

"The circuit is similar to the one implemented in the Pulsar watch," says Lanny Lewyn, member of the Hughes technical staff, "only ours will prove to be much more reliable."

How it works. As in the earlier Pulsar design, measurement is done optically. A constant-current power transistor drives a light-emitting diode whose light reflects off the fingertip onto another photodiode. The heart-rate measurement relies on the slight increase in infrared light absorption by capillaries in the fingertip during the systolic pressure wave.

After any photocurrent from ambient light is canceled out, the signal current is sampled by a sample-and-hold capacitor and passed through a two-stage bandpass filter, while its steady-state component is removed by a second-order loop filter. The result is a simultaneously integrated and differentiated pressure waveform.

The filtered signal is then converted into a logic output by a discriminator feeding the LCD. Applying the fingertip at a soft and constant pressure will trigger a readout updated every 5 seconds. The average is thus one readout for every 5½ heartbeats.

The circuit uses six operational amplifiers, each measuring 0.25 by 0.41 millimeter and consuming 2.2 microamperes. Total current consumption of the 6.6-mm² chip is 18 μA, and the watch works off two standard 1.5-volt batteries.

As with its other watch parts, Hughes will only produce the chip

Circle 43 on reader service card

Time beats on. Sensor to measure heart rate is on the face of digital watch. The user puts an index finger over the sensor to get a reading displayed every 5 seconds.

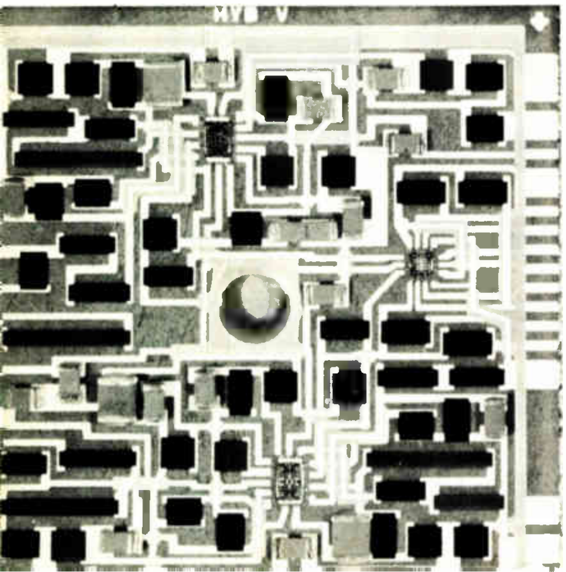
for watch makers to package and market in a finished product. However, the company would not reveal what companies plan to sell the heart-rate models. □

Packaging & production

Porcelain-on-steel makes progress

The world of hybrid circuitry may see a lot of a new kind of packaging as porcelain-on-steel technology, its materials problems behind it, moves into a new phase. Says Dan Wicher, a member of the technical staff at Singer's corporate R&D laboratory, Fairfield, N. J., "1979 will be a year of thorough reliability-testing of circuit modules built with this packaging technique." He likes the combination of materials for its low cost as substrates, suitability for large-area hybrids, good thermal properties, and mechanical strength.

Tester. Singer built this dual-channel d-a converter on a coated-steel substrate from Erie Ceramic Arts. It and other circuits are now being tested for reliability.



Circuits on coated steel are no longer confined to the simple screened-on patterns of conductors and resistors described in recent technical papers and articles on the subject. The photo below illustrates the kind of complex circuits Singer has built. It is a dual-channel, digital-to-analog converter fabricated using thick-film design-layout rules on a coated-steel substrate from Erie Ceramic Arts Co., Erie, Pa.

Singer also built the same circuit on a substrate from Alpha Metals Co., Newark, N. J. Each hybrid includes a multilayer conductor network, 58 thick-film resistors, 20 chip capacitors, and three integrated circuits. Formerly, circuits of this complexity were confined to thick- or thin-film hybrids on alumina. The demonstration circuits are only 1½ inches on a side, but substrates up to 8 by 12 inches are possible.

Singer is also assembling other, less complex modules with the same methods. They will be tested for long-term reliability. Wicher sees the new technology as particularly useful in consumer-interactive systems such as control panels, where display elements and circuit boards could be interconnected on larger boards of porcelainized steel. If its reliability testing is successful, the company plans to apply the package to consumer products. □

Components

Better heat detector goes commercial

A program at Martin Marietta Corp. initially aimed at developing pyroelectric infrared radiation detectors for the military is about six weeks away from bearing commercial fruit. That is when Optoelectronics Inc., a Petaluma, Calif., manufacturer of infrared detectors and accessories, will begin offering lithium tantalate detectors more sensitive than those so far commercially available.

"They're good for just about any application requiring a long-wavelength, uncooled infrared detector," says Victor Yen, marketing vice president at Optoelectronics, which has an exclusive license to make the devices. "We're looking at them for things like noncontact temperature measurement, gas analysis, and intrusion alarms."

Pyroelectric detectors employ a crystalline material that produces a change in electric charge when its temperature changes. Martin Marietta applies the detectors in "smart" military projectiles to detect artillery emplacements and tanks, for example, by sensing differences between the IR radiation of the target and its background.

The devices are extremely sensitive, producing a measurable current when exposed to incident radiant power levels as low as 5×10^{-11} watt, according to Norman E. Byer. He developed the detector with Anton van der Jagt at Martin Marietta Laboratories in Baltimore, which supplies the detectors to the Martin Marietta Orlando (Fla.) division that builds them into military systems.

Already used. Uncooled lithium-tantalate detectors are already being used commercially. With a relatively high Curie temperature of 610°C, they operate at higher temperatures than detectors made, for example, of tryglycine sulfate. The latter once had a major share of the market, only to be nudged aside by lithium-tantalate ones, Byer points out.

The new detectors are also less susceptible to microphonics than the earlier units. Also, they are less expensive and far less bulky than cryogenically cooled detectors, though not as sensitive.

Sensitivity of the new detectors, expressed as a normalized detectivity measured by a standard set of electro-optical test conditions, is an order of magnitude better than that possible with lithium-tantalate units now on the market, Byer says.

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Circle 45 on reader service card

photolithographic and ion-beam milling processes Martin Marietta developed for the military devices. Ion milling makes the detector head much thinner—2 to 5 micrometers thick vs 20 to 30 μm—than that of the earlier commercially detectors.

Essentially, the thinner detector heads have much less impedance than thicker ones. That means less noise as well as heightened sensitivity, according to Byer.

He also points out that the new detectors, which are rugged and can be polished and masked, can be fabricated with the photolithographic techniques used in the semiconductor industry. Thus, entire arrays can fit on a single wafer. As many as 25 individual detector elements have been made on one wafer, in an area 1.5 centimeters on a side, Byer says. A 44-element array was formed on a wafer about 1 cm in diameter. □

Computers

Race is on in 32-bit machines

A price/performance race is brewing in the world of 32-bit minicomputers—those large machines especially favored for scientific and engineering applications. Perkin-Elmer Corp.'s Computer Systems division, which, when it was known as Interdata, was one of the early competitors in the field, is introducing a new family of processors with improved performance for about half the price of its current line. And that means at about half the price of Digital Equipment Corp.'s VAX 11/780.

Moreover, compared with its older model 8/32, the new 3220, introduced last month, quadruples the amount of memory, increases the number of registers in the central processing unit, speeds up the CPU, and makes an optional cache memory available for the first time. A basic 3220 CPU with 256 kilobytes of memory lists for $33,500. With the optional cache memory, floating-point processor and user-writable control store, the price is $46,100. The 8/32 is tagged at $82,600.

A minimum working 3220 system with a half megabyte of memory, a 10-megabyte disk drive, operating system, and language compilers is priced at $88,600. A similarly configured VAX 11/780 comes in at around $167,000. Perkin-Elmer claims the 3220 outperformed the VAX in customer benchmarks, especially in Fortran programs.

With the 3220, Perkin-Elmer also switches for the first time to metal-oxide-semiconductor memory using 16-K chips. The result is a memory price of $32,000 a megabyte, down considerably from the $152,000 the company charges for ferrite core memory. The access path to memory is 32 bits wide, and the access time is 500 nanoseconds.

Up to 4 megabytes are directly addressable. The machine uses a 24-bit address, however, so it is expected that later members of the family will support up to 16 megabytes of memory.

An optional 1-kilobyte bipolar cache memory improves the effective access time to 340 ns, says David J. Preston, senior marketing specialist at the division in Oceanport, N. J.

One problem users complained about in the earlier 8/32 was the slow context switching—that is, the time it takes the CPU in a multiprogramming system to switch from performing one user's program to another's. During the switch, the CPU must save the contents of its registers in main memory and load in the value needed for the new program. To limit the unloading and loading of the registers, the 3220 has as standard, eight sets of 16 32-bit registers—an amount optional on earlier models. This amount allows the CPU to switch register sets.

To improve input/output, four of the eight sets are reserved for the four interrupt levels, once again saving a context switch before performing I/O.

The machine has 2,000 32-bit words of control store for the microcode that interprets the standard instruction set.

The 3220 is compatible with Perkin-Elmer's current software and uses the OS/32 real-time multitasking operating system. Programming languages available include Cobol. Available software includes the recently introduced global optimizing Fortran compiler [*Electronics*, Sept. 28, 1978, p. 198], the ITC transaction monitor, and ITAM data-communications package. □

Commercial

IBM introduces laser printer

Though the Office of the Future may not yet exist, high-speed and high-quality printers that churn out documents for the office's combination of word- and data-processing systems continue to arrive. The latest is from International Business Machines Corp.'s Office Products division in Boulder, Colo.—a $75,000 unit called an Information Distributor that uses a laser-based printing mechanism to combine print, copy, and communications.

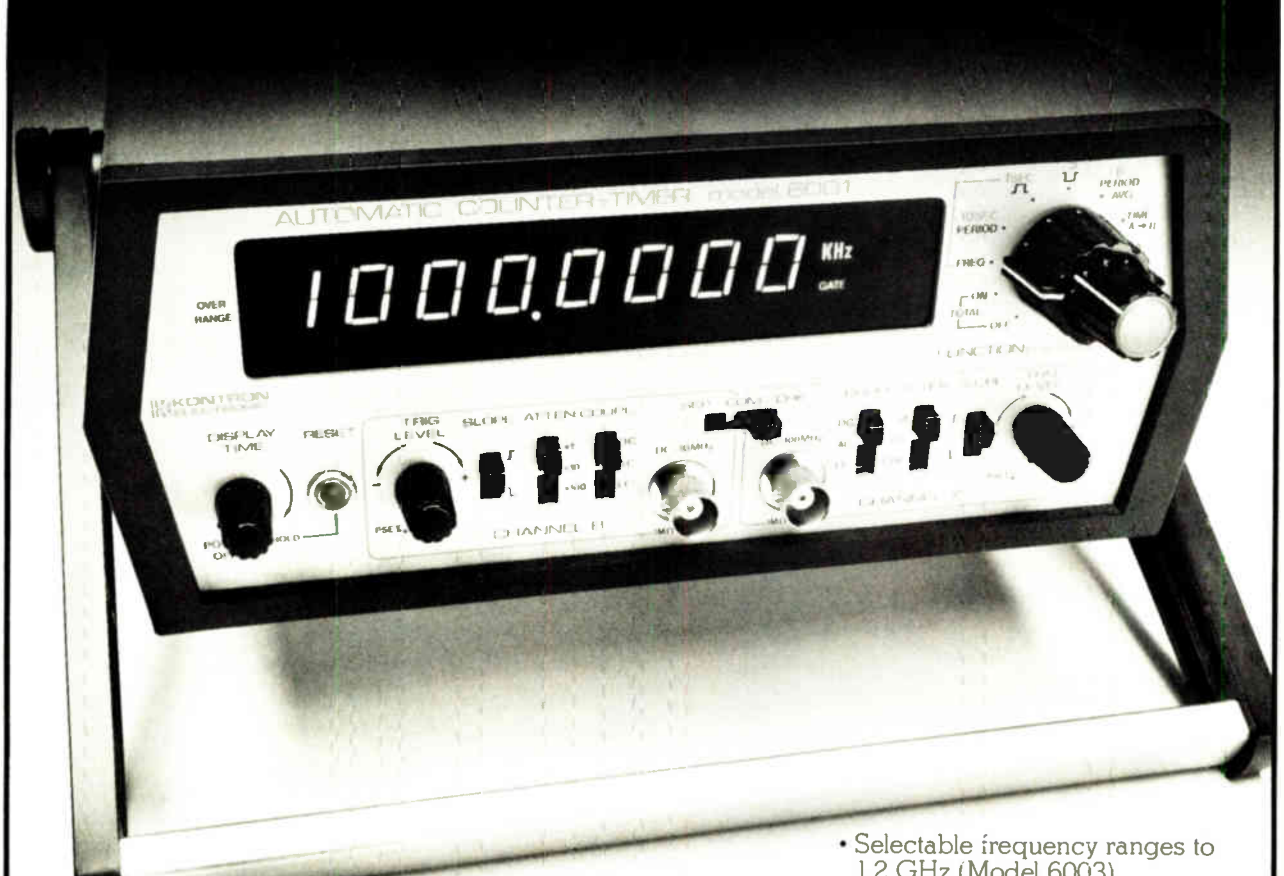
The new unit, the model 6670, prints as many as 36 pages a minute, working from magnetic cards or computer inputs. It joins the Image Printer from Wang Laboratories Inc. [*Electronics*, Dec. 21, 1978, p. 42], which prints 18 pages per minute and uses an electrophotographic nonimpact printing process, in the marketplace.

Wang just lowered the price of its machine from $35,000 to $31,000 and also dropped its copier feature. Despite the difference in selling price, basic lease rates are comparable, except for IBM's higher copy surcharge. Both machines will be shipped in the second quarter.

Quality. Nonimpact printing techniques are becoming increasingly popular because of their quietness and high print quality. Also, they are very flexible, forming characters from a matrix of overlapping dots. The programs for the type fonts can be stored in read-only memories and intermixed readily.

Up until recently, there were only two choices. Very high-speed

Model 6001 Autoranging Counter/Timer
with a programming option.



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News briefs

'We're still friends,' say AMD, Siemens

An amicable parting of the ways is how Advanced Micro Devices Inc. and Munich-based Siemens AG describe their decision to carve up their joint venture, Advanced Micro Computer GmbH. AMD wanted to focus AMC on microcomputer boards, whereas Siemens was pushing to expand that mandate. Complicating matters was the fact that Siemens plans to second-source Intel's 16-bit microcomputer, the 8086, while AMD plans to use the competing Zilog Z8000. It looks as though AMD will take over the joint operation at its home base in Santa Clara, Calif., and Siemens will take over the European operation. Siemens says the president of its Components division, Friedrich Baur, will stay on AMD's board. The parting in no way influences the interest Siemens has in AMD (it owns 20%), says Siemens officials. "If anything, cooperation with AMD could even intensify in the future," one says.

AT&T to buy telecommunications printer from DEC

That Teleprinter 1000 that some of AT&T's customers will be using is coming from Digital Equipment Corp.—one of the first major outside purchases by the communications giant. Based on the LA120 DECwriter III teleprinters [*Electronics*, Nov. 9, 1978, p. 189], the machine will have a second microprocessor added for text editing and executive writing, as well as 33,000 characters of internal bubble memory. The text-editing processor will become an option on the DEC machine later. Standard DECwriter features include smart bidirectional printing, variable font sizes, and multiple protocols. No price tag was announced for the multiyear contract covering several thousand Teleprinter 1000s, but a single DECwriter III sells for $2,600.

20,000-line-per-minute behemoths turn out 160-plus pages a minute but cost upwards of $250,000 (IBM's 3800 lists for $325,000, for example). The other choice is smaller and less costly ink-jet units that are much slower.

The laser in the 6670 is a helium-neon, continuous-wave type rated under 10 milliwatts. Through an optical system, it scans vertically a photoconductor wrapped around a drum. Turned on, it exposes what will be the white parts of the page, turning off where the characters form. As in a xerographic process, these unexposed areas pick up toner to print out on a sheet of paper.

Output. The company's Office Products division makes a point of the 6670's name—Information Distributor—because it has a variety of output options. Prominent among them are its abilities to serve as a remote high-quality printer in a computer-based network and to distribute information, either as documents or magnetic cards, to other stations in a point-to-point net.

It can communicate with any computer device that uses the Synchronous Data-Link Control, logical unit type 4, protocol of the firm's System Network Architecture. For a point-to-point net, it can link with any device using the 2770 Binary Synchronous Communications protocol, including IBM's Office System 6 products.

Of the two microprocessors in the unit, one controls the printing and copying processes and the other processes text and formats. The machine uses a 512-kilobyte diskette, with one side for system operation microcode and diagnostic programs and the other for variable data, such as the text and processing instructions. □

Business

Iranian crisis has mixed effects

Electronics firms riding high on the flying carpet of Iranian oil money are making an emergency landing,

Electronics review

as the continuing political crisis in that country sinks ambitious development plans dependent on the purchase of U. S. goods and services. However, the firms heavily involved report that until the past month or so they had received all the money due.

Many of the shah of Iran's U. S. purchases were of military equipment, where electronic gear is part, but not all, of the purchase price. On the other hand, the former government had an ambitious modernization program for the country's telecommunications system, and that was to incorporate the most advanced electronic techniques.

An immediate loser, then, is American Telephone & Telegraph Co., which had a $194 million contract to supervise the $145 billion telecommunications overhaul. Its subsidiary, American Bell International Inc., had devoted its brief existence to the Iranian contract. The collapse of the government that made the deal has sent most of ABII's 1,000-plus employees back to assignments in other AT&T operations.

Injunction. AT&T has moved in New York State Supreme Court for an injunction against any removal of funds by the new Iranian government from an escrow account in a U. S. bank. A spokesman says the firm has already received about $7 million from the $38.8 million, but is due another $25 million for work completed, plus $55 million in termination payments if the contract lapses. The shah's government reportedly deposited some $5 billion in such U. S. escrow accounts.

Some suppliers have contracts for other telecommunications work. The Palo Alto, Calif., components maker, Watkins-Johnson Co., is figuring a 39¢ cut in earnings per share because Iran owes it $1.2 million. General Telephone & Electronics Corp. reports that it has shipped—and been paid for—about half of the equipment in its $500 million contract for central office switches.

Electronics firms in the semiconductor, instrument, and computer sectors report minimal involvement with Iran. But on the military front, there is mixed news.

Litton Industries has an $800 million contract (about 35% electronics) for four destroyers. Two are near completion, and progress payments are up to date, but the contract is up in the air.

Cubic Corp. of San Diego has nearly completed an $18 million air combat training center for the Iranian air force, with $12.6 million in the till. The company is confident it can sell the system elsewhere if Iran does not accept delivery.

Another southern California firm with a big stake in Iran is Hughes Aircraft Co., which holds a contract for the AWG-9 weapons control system. Some 370 Phoenix missiles, part of that system, could alone bring in $83 million. As with many of the military programs, support and service contracts were potentially big money makers.

Aircraft makers, by and large, report minimal damage. Grumman Aerospace Corp. says it received over $2 billion for the 80 F-14s it delivered. Cancellations may come for the 160 General Dynamics F-16s and the 16 McDonnell Douglas RF-4s on order, but both firms can divert the production to other customers in line. As for the electronics-laden E-3A airborne warning and control system, Iran had not contracted to buy the seven that would have supplemented the U. S. and NATO buys. □

Industrial

Intel goes after industrial controls

With an eye to the mushrooming market for microcomputer-based industrial controllers, Intel Corp. is launching industrial packaging and peripherals for its family of iSBC single-board computers. The upcoming iCS 80 chassis offers special features that the Santa Clara, Calif., firm hopes will make it a bigger factor in a market now topping $150 million a year.

Available as complete systems or as a chassis kit, the iCS 80 attaches

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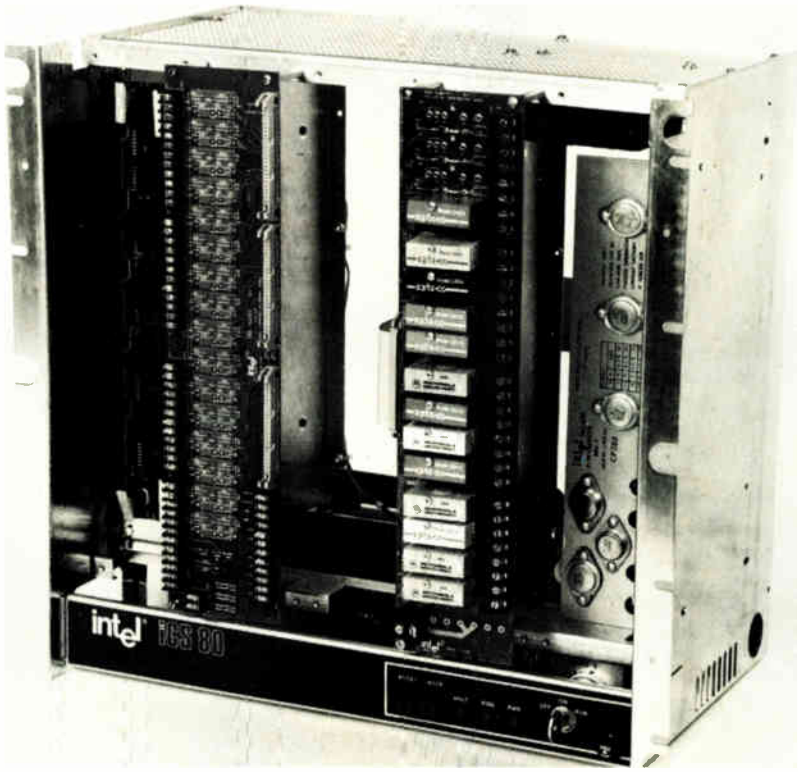

All together. Intel's new chassis will hold iSBC single-board computers and new signal-conditioning boards and other modules, mating with standard industrial-control packages.

to standard industrial control packages. At the same time, Intel is introducing a line of signal-conditioning boards aimed at further enhancing the iSBC's applicability to industrial environments.

Another semiconductor maker, Texas Instruments Inc., spotted this market five years ago and now has two separate controller families. Its Johnson City, Tenn., operation manufactures the 5TI sequential controller using transistor-transistor logic, as well as the more versatile Program Master 550 based on 16-bit 9900 microprocessors.

Prices. A stripped-down 5TI can be had for under $1,000 and prices for the new PM550 start at under $5,500. Fitting in between the two TI models are controllers using the 8080-based iSBC 80/05 and costing from about $2,375 up. A system based on the iSBC 86/12 with its 16-bit 8086 has more memory than the PM550 but no programmed functions and costs about $4,000.

Controller makers also can use any of the variety of Multibus-compatible analog and digital boards available from Intel and others. The iCS 80 chassis can accommodate from 4 to 12 Multibus-compatible boards, standing them vertically for more efficient cooling.

Intel already had a host of analog and digital input-output boards, but needed boards both to terminate heavy-gauge input lines and to filter out transients and noise before the signals are routed to the system, says Mike Maerz, marketing manager of Intel's OEM microcomputer systems operation in Aloha, Ore. They designed three such boards—iCS 910, 920, and 930—which provide analog, digital, and large-signal ac and dc terminations, respectively. A user can also tailor them to a signal's filter needs.

The chassis kit sells for $1,990 with the iSBC 635 power supply, which provides four voltages and a maximum 14 amperes from its +5-volt line. For $2,180, it comes with the 30-A, +5-V iSBC 640 power supply, aimed at more memory-intensive applications. Prices for the signal-conditioning boards range from $310 to $460. □

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FCC considering 900-MHz use for utilities

The Federal Communications Commission is considering a new allocation in the 952-to-960-MHz fixed-service band for various automation systems used by utilities. **The systems to be explored in the new Docket 79-18 would be used for remote automatic reading of electric meters, load management, environmental monitoring, and other operational functions.** The FCC says it wants initial comments by April 30, with replies one month later. The new proposal supersedes the dormant Docket 20-05 advanced nearly five years ago by Readex Electronics Inc. and Sangamo Electric Co. for remote meter reading. The concept was revitalized with the 1977 proposal of the Utilities Telecommunications Council, an industry group, to broaden the idea to include distribution automation. The FCC says it needs comments on standards to insure the compatibility of different systems operating in the same or adjacent areas. The commission is also interested in possible development of a common distribution automation communications net for utilities.

Commerce expected to approve NBS input/output standards

Insiders predict that the National Bureau of Standards' approval last month of the nation's first three input/output channel interface standards for all Federal computers—except weapons—will probably be upheld by Commerce Secretary Juanita Kreps, despite complaints from some mainframe makers. The I/O standards, derived from International Business Machines Corp.'s 360/370 series technology [*Electronics*, Aug. 31, 1978, p. 94] have upset such IBM competitors as Control Data Corp., Digital Equipment Corp., and Honeywell Information Systems. **They are trying to persuade Secretary Kreps to reject the NBS proposal** on the grounds that it is obsolete, a hindrance to innovation, and likely to open U. S. markets to Japan, where the IBM I/O standards are already in effect. The secretary seems unlikely to be swayed by these arguments, however, in view of congressional pressures favoring standards to enhance computer competition and reduce Government systems costs.

Wage insurance support weakens in Congress

Electronics workers whose employers abide by the 7% annual wage hike guidelines of the Carter Administration may never get to see the proposed Federal tax credit meant to take effect should inflation exceed that percentage. That's the word from Capitol Hill, where the soft support for the so-called Real Wage Insurance plan is getting softer—particularly in the crucial House Ways and Means Committee. **Committee Chairman Al Ullman (D., Ore.) is considering tabling the plan, sources say.** Opposition to the proposal, which would grant a 1% tax credit on the first $20,000 in wages for each percentage point of inflation past 7%, stems from its potentially higher cost. If prices rise 7.5%, for example, the U. S. Treasury would lose $2.5 billion in taxes, plus an equal amount for every percentage point above that level.

AT&T confesses software hurdle delays ACS

Major software problems would significantly delay introduction of American Telephone & Telegraph Co.'s controversial Advanced Communications Service (ACS), yet the company says it still wants Federal Communications Commission approval of its plan. **AT&T's mid-February disclosure that it is unable to meet the FCC deadline for filing ACS tariffs has created an uproar within the telecommunications industry,** with some ACS opponents hinting they will ask the Justice Department to investigate whether

AT&T committed a Federal crime by announcing the service prematurely last year [*Electronics*, July 20, 1978, p. 41] in order to stifle competition. The initial ACS plan is to use existing digital Bell System facilities to interconnect computers or intelligent terminals, regardless of make or function. The software challenge now "will require a significant further development effort previously unforeseen," AT&T admits, adding that it does not yet know how long that may take.

Survivable low-frequency system to be upgraded by Air Force

The Air Force has awarded $14.6 million to Westinghouse Electric Corp. to produce the initial classified modifications to air and ground radios of the 487L Survivable Low Frequency Communications System. The funding of the company's Defense and Electronic Systems Center, Baltimore, follows four months of successful operational tests of preproduction hardware. **The new support equipment increases the accuracy and reportedly doubles the range of the 487L,** developed in the mid-1960s by Westinghouse to provide national command authorities with survivable communications for use in nuclear warfare.

To ease exports, NBS will push study of emi

Attention is focused increasingly on the development of better measurements and standards for electromagnetic interference at the National Bureau of Standards, says director Ernest Ambler. **The reason: stiffening of some emi regulations in overseas markets that will affect more than $10 billion in U. S. exports in 1980, ranging from medical electronics to data-processing and telecommunications equipment.** Ambler says in his NBS budget presentation to Congress that the $1 million increase for emi studies in fiscal 1980 accounts for more than 10% of the bureau's proposed spending gain in its $96.5 million program.

Soviet ICs better than believed, Control Data claims

Russian integrated-circuit technology is not far behind that of the United States and far better than the Government has believed, according to Control Data Corp. The Minneapolis company, an advocate of relaxing export controls of technology sales to the Warsaw pact powers, **bases its assessment of Soviet ICs on the company's laboratory analysis of samples obtained by CDC officials.** CDC executives were scheduled to show circuit samples and detail their findings in Washington at the end of February.

Industry lobbying to stop extension of Renegotiation Board

Government electronics contractors are pushing hard to kill H. R. 2002, a bill now before the House Banking Committee introduced by Rep. Joseph Minish (D., N. J.) to extend the Renegotiation Board's life for two more years. Set up during the Korean conflict to recover "excessive profits," the board is scheduled to go out of existence at the end of this month following congressional action last fall. However, the White House has asked for $8.5 million to extend its life. **The American Electronics Association leads the drive to bury the Minish bill,** calling the board both obsolete and unnecessary in view of the "literally dozens of other important procurement safeguards that have been established" since the board's 1951 creation.

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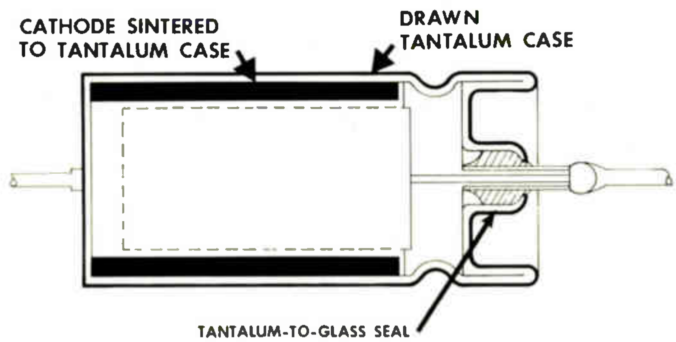

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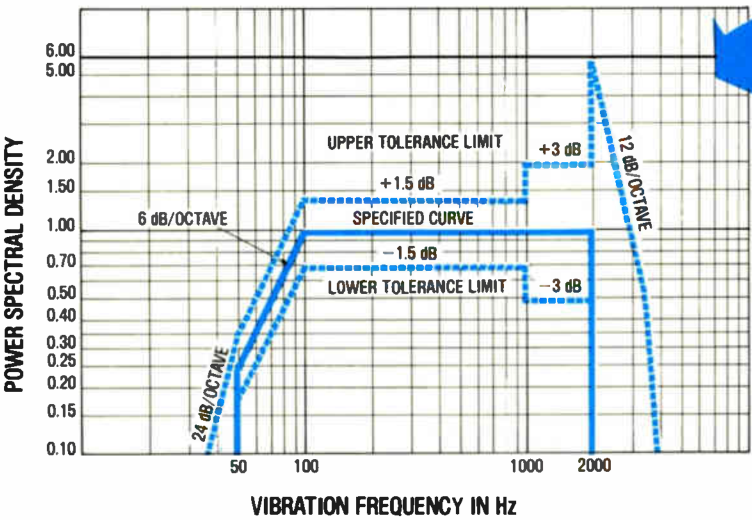

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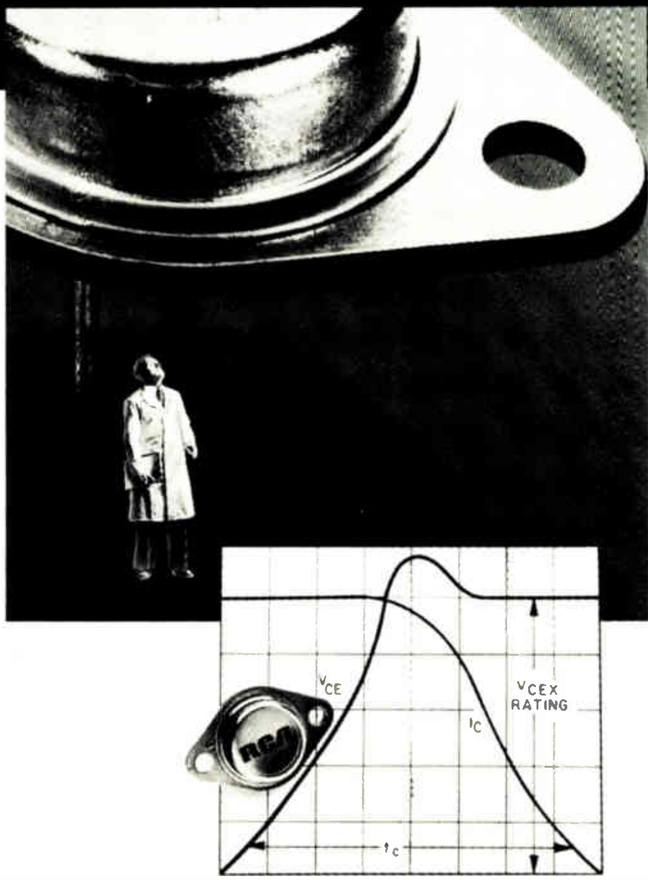

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2N6671 2N6672 2N6673	450 V 550 V 650 V	0.1 (25°C) 1 (125°C)	1 (25°C) 2 (125°C)	5A	0.4 (25C) 0.8 (125C)
2N6674 2N6675	450 V 650 V	0.1 (25°C) 1 (100°C)	1 (25°C) 2 (100°C)	10A	0.5 (25C) 0.8 (100C)
2N6676 2N6677 2N6678	450 V 550 V 650 V	0.1 (25°C) 1 (100°C)	1 (25°C) 2 (100°C)	15A	0.5 (25C) 0.8 (100C)

Switch Max Booklet 2M1217 gives you full details on how these new transistors are designed, made, tested and characterized. There's also a designer's guide chart suggesting optimum transistor types for typical switching power supply circuits.

Application Note AN-6741 describes the use of the RCA 2N6676 15-ampere SwitchMax power transistor as a driven pulse-width-modulated flyback converter stage, in a 20-kHz off-line power converter providing 340 watts output.

Application Note AN-6743 is a description and analysis of a 900-watt off-the-line half-bridge converter using two 15-ampere SwitchMax high-voltage power transistors. This Note, too, demonstrates the outstanding capabilities of SwitchMax in a typical switching application.

For all this information, contact your local RCA Solid State sales office or distributor. Or write RCA Solid State, Box 3200, Somerville, NJ 08876.

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Japan is deciding how much to open up NTT's purchases

The Japanese cabinet agreed on Feb. 20 to reach a decision before the end of the month on the portion of Nippon Telegraph and Telephone Public Corp.'s telecommunications equipment purchases to be opened to international bidding. The United States has been pushing for inclusion of NTT procurements in the category of government purchases open to foreign vendors. **During the 1977 fiscal year, NTT purchases totaled $3.13 billion,** with more than 96% supplied by designated vendors and less than 0.5% by overseas vendors.

Siemens will second-source Intel's 8086

Extending its existing technology agreement with Intel Corp. to the 16-bit microcomputer area, Siemens AG will second-source the California company's 8086 family of microcomputer products. **The West German firm will also offer all hardware and software development aids necessary to support the family.** The deal calls for Siemens to receive technology packages, including mask sets, from Intel. The U. S. firm, in turn, will get equivalent packages on certain 8086 products that Siemens will develop.

UK regulator stabilizes varying line voltages despite big drops

Many modern electronic appliances like television sets cannot tolerate the wide voltage fluctuations that can occur in developing nations. To **hold a 220/240-V power supply to within 6% of nominal for voltage swings from 145 to 255 V,** Gould Advance Ltd.'s Electronic Components division in Bishop's Stortford, Herts., has come up with a 500-W custom microcircuit-controlled line regulator based on a Ferranti Semiconductors uncommitted logic array. In operation, the regulator selects one of six triacs, each switching a transformer tap, to adjust the output voltage within one cycle. Efficiency is better than 96%. In addition to selling the complete unit, Gould plans to market the IC controller, which it says can be used in line-regulator systems of up to 5 kVA.

Mitsubishi enters fray against IBM's new mainframes

Mitsubishi Electric Corp. is the second Japanese company to start selling computers that compete with IBM Corp.'s 4300 series (see p. 68). Its Melcom Cosmo series model 700S and model 700III are said to offer somewhat higher performance than IBM's 4341. The firm claims that these are **the first medium-sized computers to offer a dual-central-processing-unit option,** which it says has 1.7 times the processing power of a single-processor CPU. The computers are designed for interactive processing and will support up to 128 (the 700III) or 64 (the 700S) work stations. They can also support remote terminals in a time-sharing system and are configured for distributed-processing systems using Mitsubishi's Multishare Network Architecture or IBM's Systems Network Architecture. Deliveries will start in June, with rental prices between $12,500 and $35,000 a month for the 700S and between $20,000 and $75,000 a month for the 700III; software costs extra.

Typewriter-transmitter from Switzerland has video screen

J. Bobst et Fils SA, Lausanne, Switzerland, has recently introduced a novel typewriter-transmitter. Called Scrib, the self-contained tele-editing device for writing, storing, and transmitting texts weighs some 8.5 kg and looks like a simple portable typewriter. Basically a microcomputer with magnetic cassettes, video screen, and miniprinter, it can be line- or battery-operated. The user can make any number of alterations, compare different versions of text, and keep a check on the number of characters typed. **The video screen can be split into two parts to allow drafting of a second version with the original text still on the screen.** The final version is stored on a minicassette and can be transmitted over the normal telephone system at 30 characters per second.

West Germany gets fiber-optic link for regular phone service

West Germany's post office, the Bundespost, has put into service what it says is Europe's first fiber-optic link for regular telephone communications. The 34-megabit-per-second system, developed by Siemens AG, covers the 15.4-km distance between exchange offices in Frankfurt and Oberursel. **It can simultaneously transmit up to 480 telephone channels over a pair of glass fibers each 0.1 mm thick.** Pulse-code-modulation equipment at the system's two terminals combines the 480 individual telephone signals into one time-multiplexed digital signal.

BPO's digital exchange moves into production phase

First production orders for the British Post Office's Advanced Digital 100 Extension CDSS 1 exchange are going to Plessey Communications and Data Systems Ltd. in Nottingham and GEC Telecommunications Ltd. in Coventry. **The local market for the CDSS 1, which features single-channel codecs, is expected to be $60 million per year** in early 1980s. Moreover, both companies have high export hopes for the product.

Meanwhile, Ferranti Semiconductors in Gem Mill, Lancs., now has first samples of the BPO-originated codec used in the CDSS 1. Its part is a alternative version of General Instrument Microelectronics Ltd.'s n-channel MOS codec chip, which has been in production for a year.

Addenda

CII–Honeywell Bull and Siemens AG have received a $120,000 contract from the European Commission, the executive body of the nine-nation European Economic Community, to develop a systems language for European computers. Over the next nine months, **the two firms will elaborate software to interface operating systems and applications programs among different makes of computers.** . . . The Japanese National Railways has started test runs of a prototype 10-car electric train featuring self-powered coaches with thyristor-chopper speed control and regenerative braking [*Electronics*, Sept. 1, 1977, p. 55 or 8E]. **The 30% to 40% energy savings expected with such trains is especially important now that oil from Iran is unavailable.** . . . Implementing the Orderly Marketing Agreement for color TVs recently reached with the U. S., **Taiwan's Board of Foreign Trade has allocated quotas among the leading manufacturers.** . . . West Germany's postal service, **the Bundespost, has decided to turn directly from automatic electromechanical switches to digital switching for long-distance telephone calls.** For short-haul traffic, though, it will continue to equip local exchanges with the analog EWS system. . . . **Saudi Arabia is negotiating with NV Philips Gloeilampenfabrieken of the Netherlands and Sweden's L. M. Ericsson to install an additional 250,000 telephone lines there,** a project originally planned for 1980–85. The new order could run from about $0.5 billion to $1 billion. . . . **The Swedish National Investment Bank has acquired near-bankrupt Luxor Industrie AB** [*Electronics*, Feb. 15, 1979, p. 92] for a symbolic 1 krona, or 23 cents. It is guaranteeing money for current operations.

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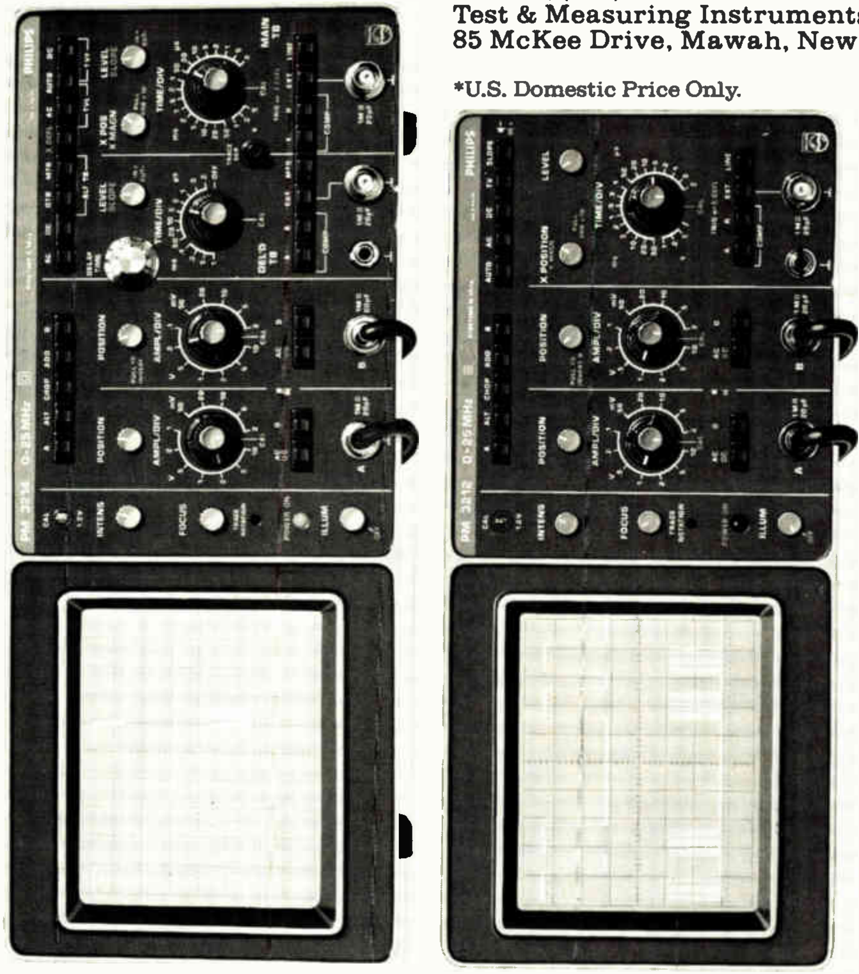

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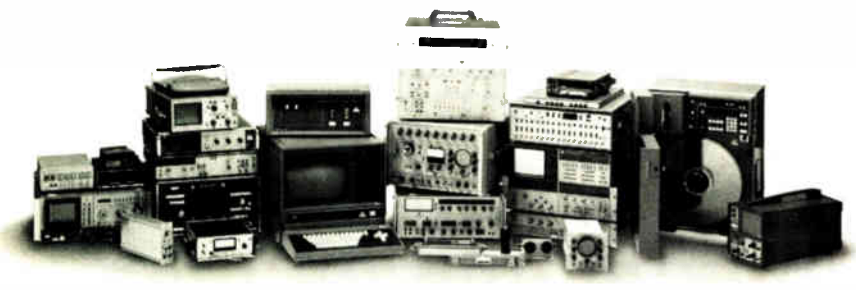

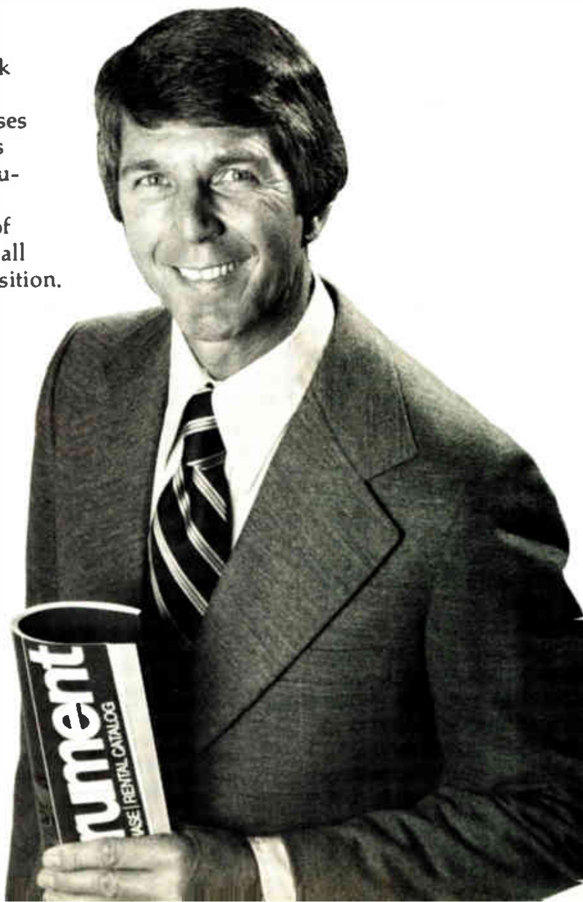

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Small firm has big ideas for multiple microprocessors

Proposed chip, with RAM, PROM, and I/O controllers, would be the basis for microcomputer arrays

The idea of assembling a number of conventional off-the-shelf microprocessors in parallel to create powerful computer systems has been arousing increasing interest in the semiconductor industry for some time. It has just been given a new twist with a proposal for a very large-scale integrated microprocessor designed for use in multiprocessor arrays.

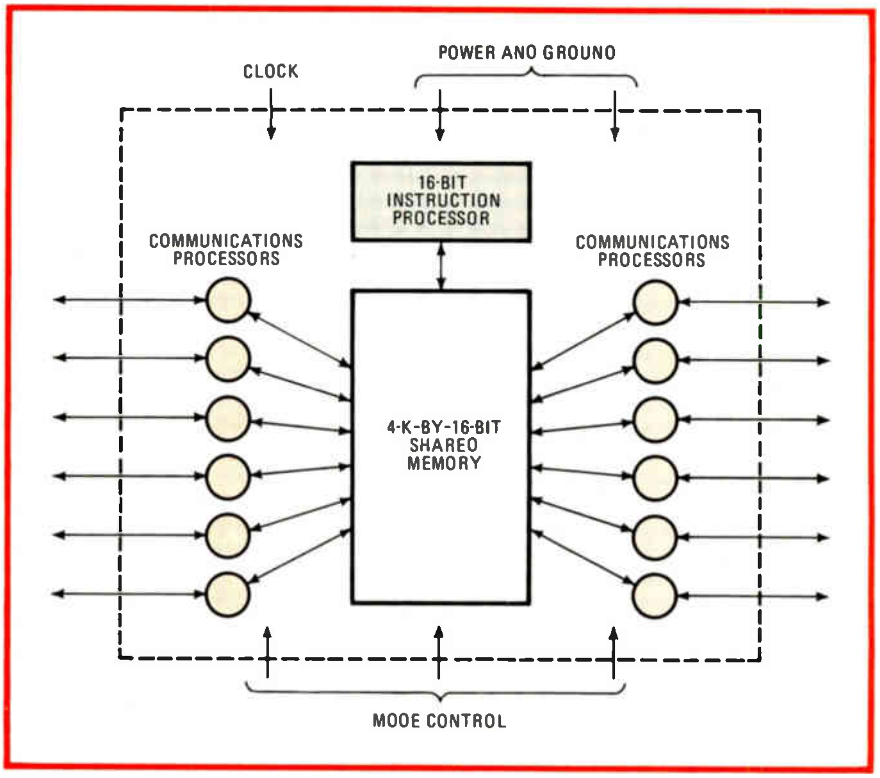
The proposal comes from Systems Designers Ltd., a small software and systems company in Camberley, Surrey, that is looking for backing or for a link with a semiconductor company to turn its two-year paper study into hard silicon.

Novel. The originality of its AMP—for adaptive microprocessor—lies less in the amount of circuitry on chip than in the way it is connected. Basically, all on-chip communication is through the memory block in what is termed a shared-store multiprocessor configuration. This is organized as 4,096 16-bit words and arranged in 256-word segments. Each memory segment may be programmable read-only or random-access memory. Numerous versions of the chip, with different PROM/RAM partitioning, are possible, according to Allen Croxon, a principal consultant at the company.

Any number of AMPs could be used to assemble computer systems ranging from small floppy-disk–based microprocessors to large on-line disk-based information retrieval systems. "The AMP could be used for random logic replacement or as a powerful systems building block," says Croxon, who adds that one big computer company "likes what we are doing."

Increasing capability. Fundamental to SDL's aspirations is the growing power of VLSI technology. It believes new computer architectures overcoming the communications limitations of present-day bus-oriented systems will be created by the ability to pack close to a quarter of a million devices on a chip.

On its 18-pin AMP chip, for example, SDL will pack 64 kilobits of variable memory, 12 simple communications processors—one associated with each data line—and a 16-bit instruction processor. That's beyond a microcircuit technology only now coming to grips with the 64-K RAM. But, says Croxon, the development time for a new microprocessor is such that the technology will be right when the firm is ready to commit to silicon. "For the 64-K RAM there are about 70,000 transistors per chip. By 1982 the industry will be able to achieve around 200,000 devices per chip, and we are targeting our part for 1982."



Adaptive. Twelve I/O processors buffer a 64-K memory from the outside world. A 16-bit instruction processor also has access to the combined RAM/PROM store.

The instruction and communications processors can only communicate with each other via the memory block using direct memory access. This could cause arbitration problems between simultaneous memory access requests. But, says Vic Stenning, who heads up software development on the project and has several years' experience on UK multiprocessor projects, including Demos [*Electronics*, Sept. 14, 1978, p. 92], "we have ideas on how to solve this."

Assigning lines. The communications processors can be programmed to allow all 12 data lines to work in concert or separately. Thus, the AMP can provide 12 independent serial data paths; or eight lines could provide byte-parallel interface, two lines a full-duplex serial interface, and the two remaining data lines could be used to establish handshaking protocols.

Says Croxon, "The AMP is a chameleon with an entirely general-purpose communications capability." Each processor can exchange data with its neighbor to complete a computation or can act as a communications channel transferring data between contiguous processors according to defined protocols. "This way," Croxon says, "you overcome the theoretical bandwidth limitations of bus-oriented computers."

Adding power. This communications flexibility could be exploited to put together a system of any required power by adding processing elements in regular arrays or dedicated networks. A problem would be split up, with one processor per computational process.

The AMP processor in fact comes into its own at the system level, says Croxon. He draws a distinction between his firm's homogeneous systems and conventional heterogeneous systems comprising a central processing unit and a family of special-purpose support chips.

Splitting program segments between processors instead of calling a sequence of subroutines into a time-shared central processor calls for a disciplined approach to software. One problem is the danger of a "deadly embrace" in which two processors simultaneously access each other. But, says Stenning, "New languages like Concurrent Pascal impose a hierarchic structure which makes it relatively easy to avoid this danger."

For the AMP operating system, SDL aims to use ADA, the U. S. Department of Defense–backed real-time language that features explicit concurrency, modular programmability, and strong typing. DOD backing should make the language well supported, Croxon argues. In fact, SDL is currently participating in an evaluation of the language for the UK Ministry of Defence.

But before it can get around to ADA operating systems for the AMP, the company must get the necessary support. Croxon believes they have taken their study far enough to show that problems of parallelism such as memory arbitration, data flow, and program segmentation can be overcome. Now he wants to turn his paper tiger into one that bites. ☐

Japan

NEC takes on IBM's new mainframe generation

It is only a few months since IBM Corp. introduced the System/38 and just a few weeks since it announced its 4300 series, both major steps in a new round of mainframe competition. But Nippon Electric Co. and its joint venture company with Toshiba Corp., NEC Toshiba Information Systems, have already answered with the ACOS system 250.

Claiming a 30% to 40% price/performance advantage for its units, NEC says that the System 250 model 40 is directly competitive with IBM's System/38 model 3, and the model 60 with the System/38 model 5 and the 4331 [*Electronics*, Nov. 9, 1978, p. 81, and Feb. 15, 1979, p. 63].

Selling. Improved hardware, improved software support, and, above all, improved architecture, with functionally distributed processing and implementation of the operating system in firmware and hardware, as well as in software—not to mention double the sales force deployed for the previous model—all are part of the strategy for selling the new, low-end ACOS 250.

The computers' main memory comes in 256-kilobyte increments up to 1 megabyte on the smaller model 40 and up to 2 megabytes on the larger model 60. All of it is available to the customer for his programs, whereas on some IBM machines, says NEC, system programs preempt about half the memory. In July, when deliveries first start, the 250 machines will use the same 16-K random-access memories that NEC is selling at a furious pace in the U. S.

The processors. The functionally distributed central processing unit includes four separate processors—five when a communications control processor is added. The four are an interior processor for performing user instructions; a supervisory processor whose functions include initialization, microdiagnosis, and console service; a file processor for disk and high-speed tape control; and a unit-record processor for all other peripherals, including floppy disks, line printers, and slower devices. Machine performance and convenience is also said to be enhanced by the ability to support up to 64 work stations.

The CPU's logic is made up of emitter-coupled-logic chips with 550 gates and a transistor-transistor-logic level at the device's pins. The controllers for each of the up to 12 input/output data channels are built with a 3,300-gate n-channel metal-oxide-semiconductor device that controls the handshaking protocol and data transfer.

The operating system is mainly firmware stored in 500 to 600 kilobits of high-speed bipolar programmable read-only memories. A few

SCIENCE/SCOPE

Hughes is one of two AMRAAM finalists selected by the Joint System Program Office at Eglin Air Force Base to participate in the validation phase of the Advanced Medium-Range Air-to-Air Missile program. The Hughes design provides track-while-scan, multi-shot, and launch-and-leave capabilities, even against severe electronic countermeasures. AMRAAM will replace the AIM-7 Sparrow, now in use with the U.S. Air Force and U.S. Navy. It will outperform Sparrow, yet be half the size and weight, and cost less. AMRAAM will be used with the F-14, F-15, F-16, and F/A-18 aircraft. The validation phase is expected to last 33 months, at which time the winning design will be carried into full-scale engineering development.

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Vast amounts of data gathered by the Pioneer Venus mission in just 90 minutes last December, though still being analyzed, have given scientists a dramatic glimpse of Earth's nearest planetary neighbor. Teams of investigators already are using their discoveries to refine their theories on the evolution of the solar system and on the forces that drive Earth's weather.

The mission consisted of two spacecraft designed and built by Hughes for NASA's Ames Research Center. One, the Multiprobe, sent four probes to the surface, one of which survived for more than 67 minutes before succumbing to the searing environment. The other, the Orbiter, continues to provide pictures and other data as it circles Venus every 24 hours.

Many of the Pioneer Venus findings confirmed scientists' predictions. The planet's intense surface temperature (850°F) and atmospheric pressure (91 times that of Earth's) seem certainly to be due to a formidable greenhouse effect caused by thick cloud layers trapping solar energy. Various instruments revealed that Venus has global weather patterns. Cloud temperatures are warmer at the equator and colder at the poles. There is even a whirlpool-like vortex in the polar clouds that provides down-motion of the atmosphere.

There were, however, surprises. Probe instruments detected several hundred times more primordial argon and neon gases than Earth has. They also found the smog-like atmosphere is free of particles from an altitude of 19 miles to the surface. Two night probes saw an unexpected glow, perhaps due to "chemical fires" caused by reactions of sulfur compounds in extreme heat near the surface.

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functions such as priority scanning and floating-point arithmetic are implemented in hardware.

The System 250 is optimized for Cobol. NEC says it performs on average 1.8 machine-language instructions per Cobol function, whereas IBM computers must perform about 3.5. Other languages, like Fortran and RPG, run at normal efficiency. An assembler is not supported.

Talking money. ACOS 250 prices are hard to compare with those of IBM's 4300 series because IBM has not yet started selling it in Japan. Low-end ACOS systems start at $3,500 a month for a three-year rental, with the top of the line extending to about $15,000 a month. But NEC has not yet released purchase prices.

The low-end system includes an ACOS 250 model 40 with 256 kilobytes of main memory, two fixed magnetic-disk units with a capacity of 80 megabytes each, one magnetic-tape unit with a data transfer rate of 30 kilobytes per second, one line printer with a speed of 370 lines per minute, a system terminal, and system software. In general, though, system software is not included in the hardware price.

In comparison, a typical IBM 4331 configuration with 1 megabyte of memory, two display stations, a printer, a 130-megabyte model 3310 disk drive, and a tape drive is priced in the U. S. at $3,572 a month on a 24-month lease. A 4341 configuration, containing 2 megabytes of memory, a 280-megabyte model 3340 disk drive and two 517-megabyte 3370 disk drives, four tape drives, a printer, card I/O units, and a communications controller, leases in the U. S. for $16,707.

Staying in place. Plans call for installing more than 2,000 systems during the next four years. At the same time, NEC and NTIS do not want to take back their more than 900 ACOS System 200 installations, which they are therefore willing to enhance with such modifications as the addition of up to 16 work stations.

Although in throughput the System 250 rivals or exceeds the larger ACOS System 300 and even approaches the System 400, it is not truly in the same class. These larger models feature virtual memory and can act as a host in time-sharing systems. Neither capability is built into the System 250, which is designed to act only as terminal in distributed processing systems.

But the enhanced throughput of the System 250 shows that the time is coming for the systematic revision of the ACOS line. Of course that revision would be needed anyway as IBM wheels out its 4300 and H series machines and others follow suit. □

64-K RAMs are on the increase in Japan

Although the ACOS 250 computers will use 16-K random-access memories initially, those shipped starting Jan. 1 will contain 64-K RAMs. Nippon Electric Co.'s Computer division hopes that the firm's Integrated Circuits division will be ready to supply single-5-volt 64-K chips similar to the one announced by Texas Instruments [*Electronics*, Sept. 14, 1978, p. 39]. Otherwise, the machines will be shipped with the two-power-supply 64-K RAMs it developed for Nippon Telegraph and Telephone Corp. (NEC is scheduled to deliver a communications controller using this part to NTT by the end of the year, and it is the custom in Japan to make first deliveries of a product developed jointly with NTT to NTT.) Still, the IC division plans to make a single-power-supply 64-K RAM its main product.

Meanwhile, Fujitsu Ltd. says it will use two-power-supply 64-K parts in its new computer, still in the works. This chip will be available after scheduled delivery in October also of a communications controller to NTT. However, Fujitsu is working all out to design a single-5-V RAM, even though it has been sending samples of the two-supply part to potential customers in the U. S. since early last year.

West Germany

Simple method uses peristaltic CCDs to display color slides on TV set

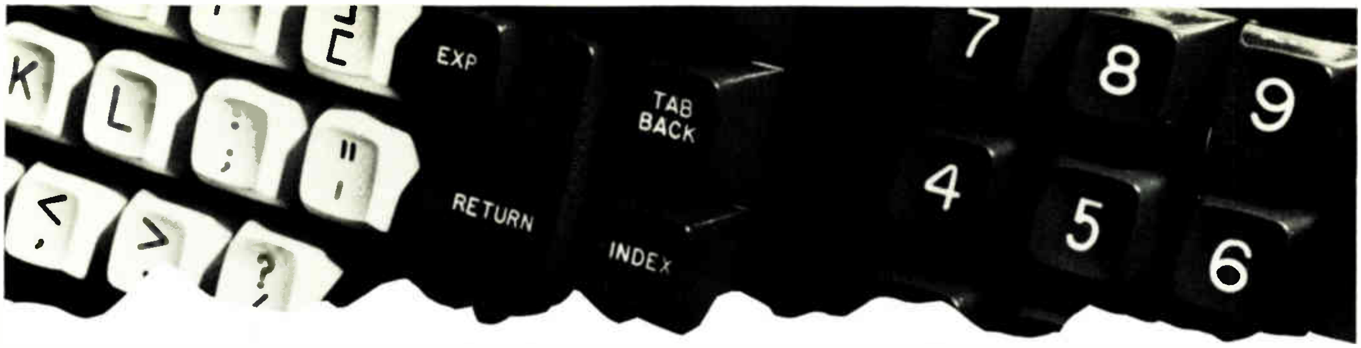
Valvo, the West German components-producing affiliate of the Dutch electronics giant NV Philips Gloeilampenfabrieken, has developed a simple method for showing color slides on a home TV screen.

Systems that show slides on TVs already exist, the most notable ones involving flying-spot scanning principles. But they require a high-voltage supply and are very bulky and expensive to maintain. Valvo's technique, in contrast, can be implemented with a few integrated circuits and simple electromechanical components, resulting in a low power requirement and a compact unit.

Sensitive. Basic to the technique are the sensors that detect one line of the image at a time. These sensors are CCD shift registers, each integrating 500 photosensitive elements. At their output, the sensors deliver a signal in serial form corresponding to the light distribution of the photo elements. After suitable processing, the signal is fed to the TV set to display the slide.

The line sensors use Philips' "profiled peristaltic," or "P^2," CCDs, developed a few years ago by the Philips Research Laboratories in Eindhoven, the Netherlands, and originally called simply "peristaltic" CCDs [*Electronics*, Sept. 4, 1975, p. 53 or 5E]. This P^2CCD, which is finding its first application in Valvo's slide-scanning technique, combines the advantages of both the highly doped surface CCD and the slightly doped bulk CCD—that is, the former's high charge-handling capacity and the latter's low transfer loss—in a single device that is claimed to be the fastest charge-transfer circuit.

In developing the slide-display



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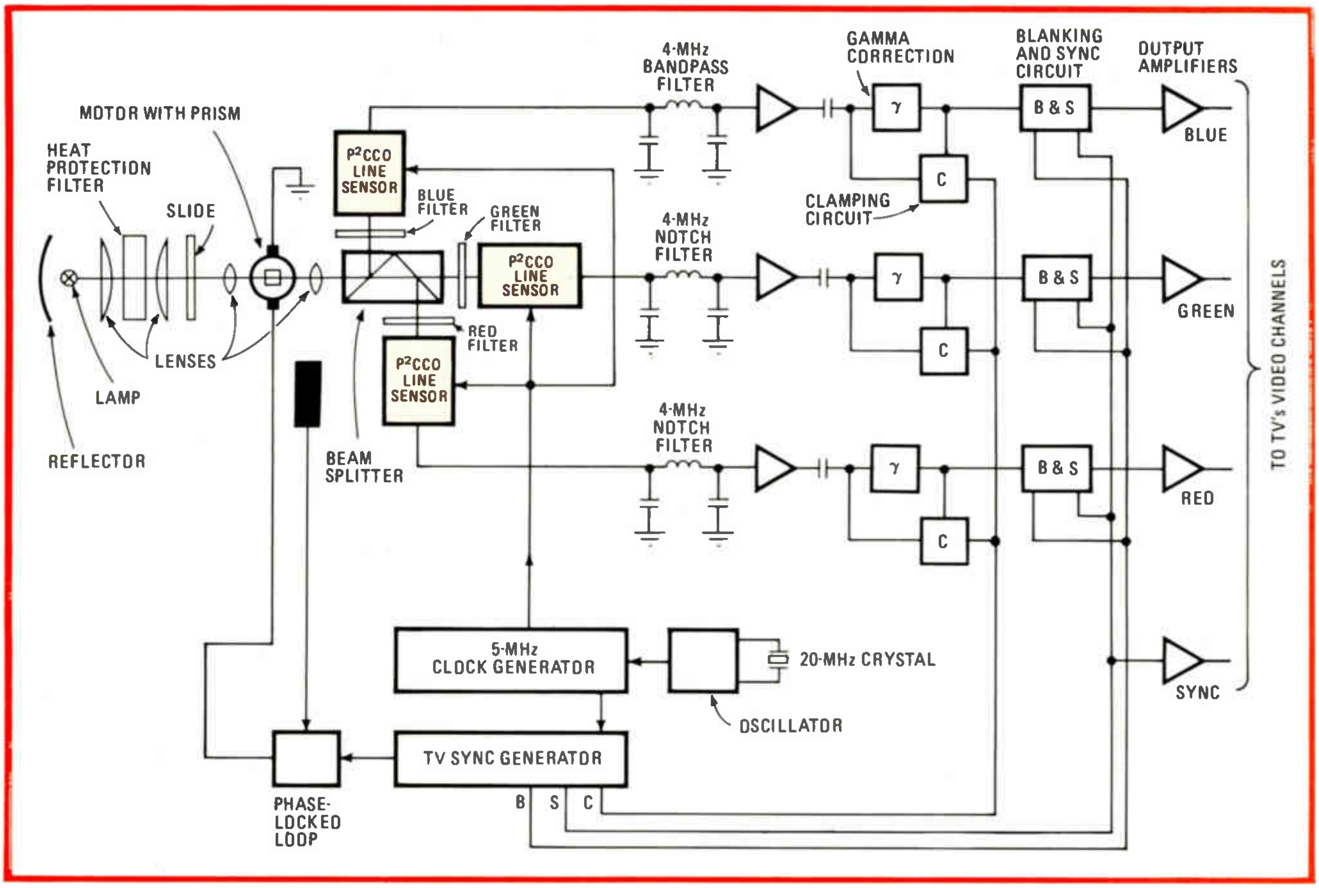

Slides on TV. Valvo uses a rotating four-surface prism to scan a slide's image. After color separation, a sensor for each color—a shift register containing 500 "profiled peristaltic" CCDs—picks up a line at a time. The signals are read out, then processed and fed to a TV for display.

system, Valvo's aim was to show customers a typical application of the scanning technique. Jörg Wölber, the principal engineer behind the effort, says a number of slide projector manufacturers have already shown interest.

In the experimental setup (see diagram), a 50-watt lamp illuminates the slide and projects its picture through a system of lenses onto a four-surface prism. The prism in turn projects each picture line through a three-way beam splitter onto the linear array of the photosensitive elements of three line sensors. Color filters between the beam splitter and the sensors effect the necessary color separation into blue, green, and red.

Scanning. The prism continuously rotates about a horizontal axis, thus scanning the picture vertically line by line. With the prism turning at 750 revolutions per minute, its four surfaces produce a total of 50 pictures per second. Driving the prism is a small motor whose speed is kept constant by a phase-locked loop. Five-megahertz clock pulses applied to the three line sensors ensure that the line content is correctly read in one horizontal scanning period of the TV set.

The blue, green, and red 4-MHz video signal output of each line sensor is filtered in an inductance-capacitance network to rid the output of any remaining clock pulses and harmonics. Each signal is then amplified and applied to a gamma correction network to adapt it to the curvature of the picture tube. After a sync generator has added blanking and synchronization pulses, the three video signals are again amplified and fed to the picture tube via the set's video channels.

The resulting experimental slide-scanning system produces high-quality pictures on an ordinary TV screen. At a recent demonstration in Hamburg, Valvo's home base, the pictures shown were of the same sharpness and brightness as those in formal TV reception.

Wölber concedes that the present setup has one major drawback: the three line sensors must be mounted with micrometer accuracy relative to each other to achieve precise line-by-line scanning. To eliminate this problem, the Valvo engineers are currently developing a single P² CCD chip, dubbed the Tricoli sensor, that has the three necessary linear arrays. They are also developing a corresponding color-separating device.

Valvo's method has other potential applications, Wölber points out. One would be in scanning movies and presenting them on a TV screen. Another would be in scanning banknotes and displaying them on a monitor for counterfeits. Still others are in machine tool systems, where the technique could be used for positioning workpieces. □

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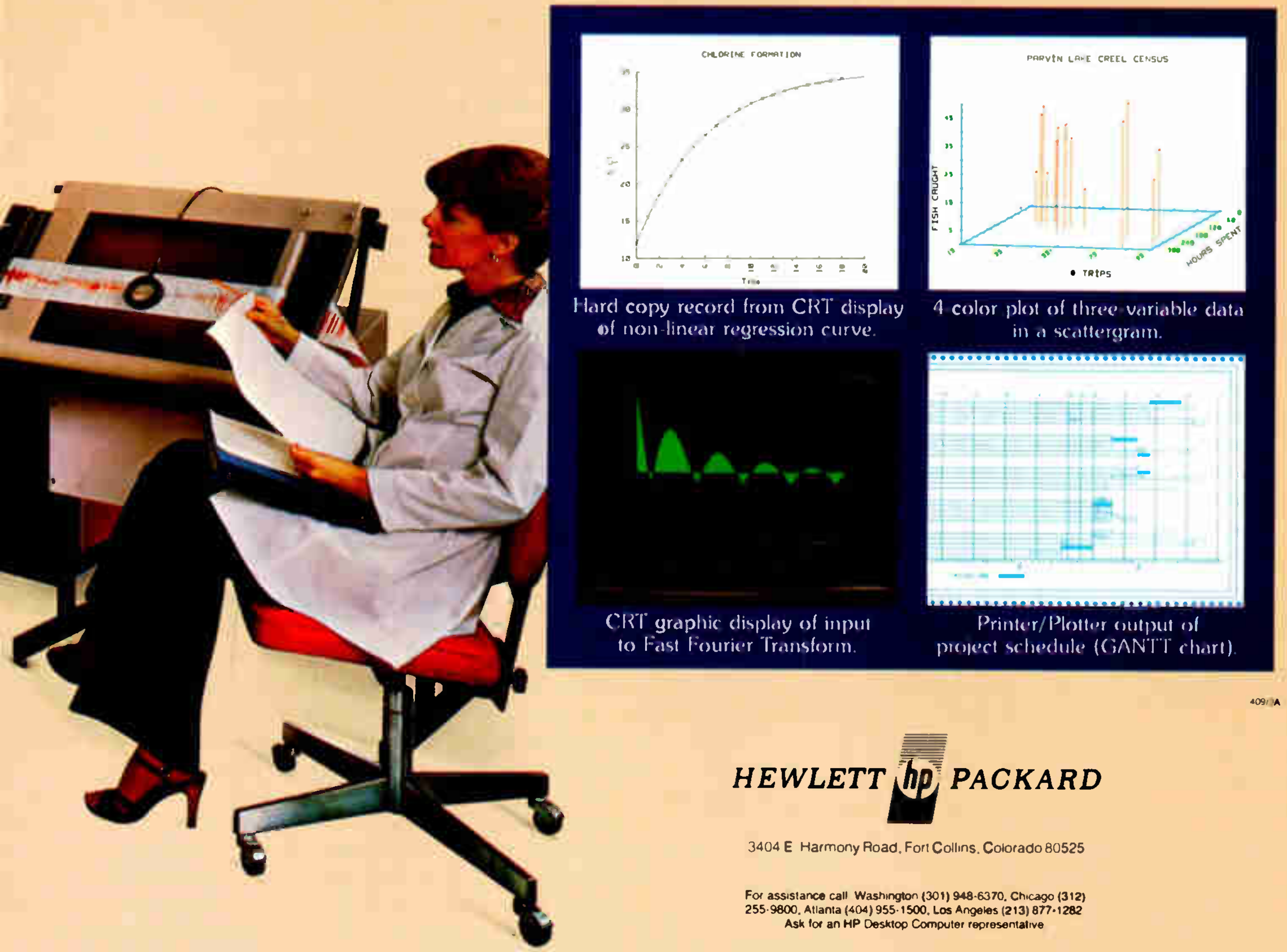

Hard copy record from CRT display of non-linear regression curve.

4 color plot of three-variable data in a scattergram.

CRT graphic display of input to Fast Fourier Transform.

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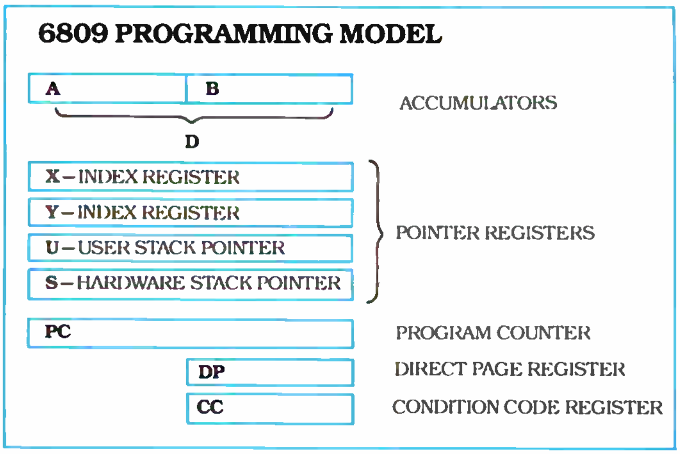

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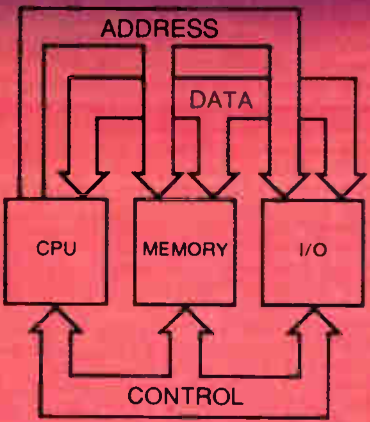

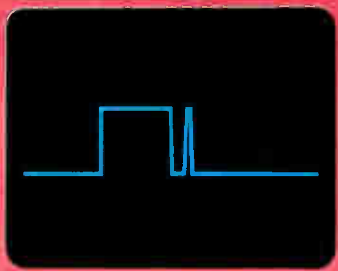

	1600A	1600S	1602A	1607A	1610A	1611A	1615A	1640A
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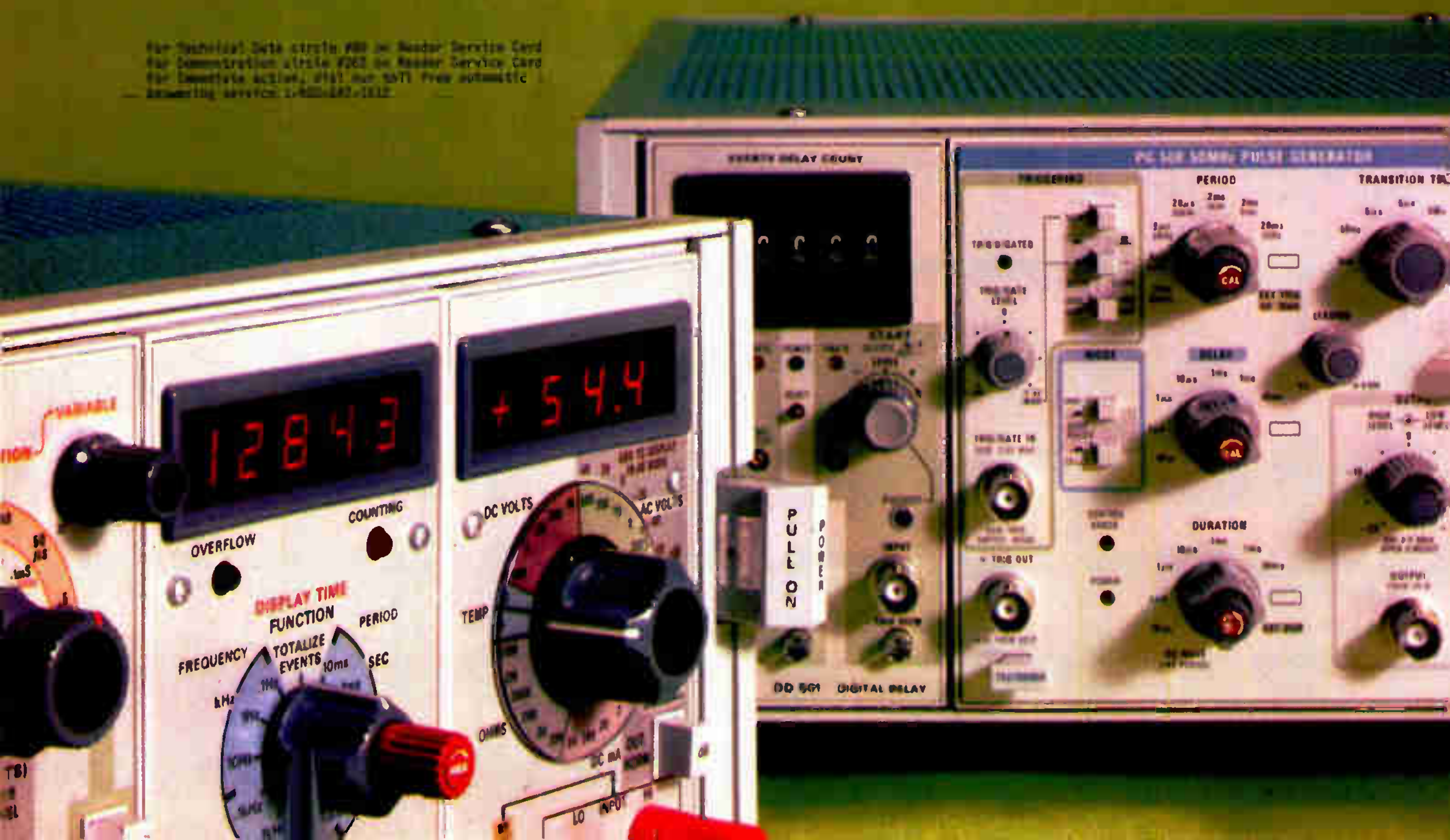

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IBM squeezes its imitators

New 4300 line, less expensive and more powerful, has makers of plug-compatible computers wondering where they fit

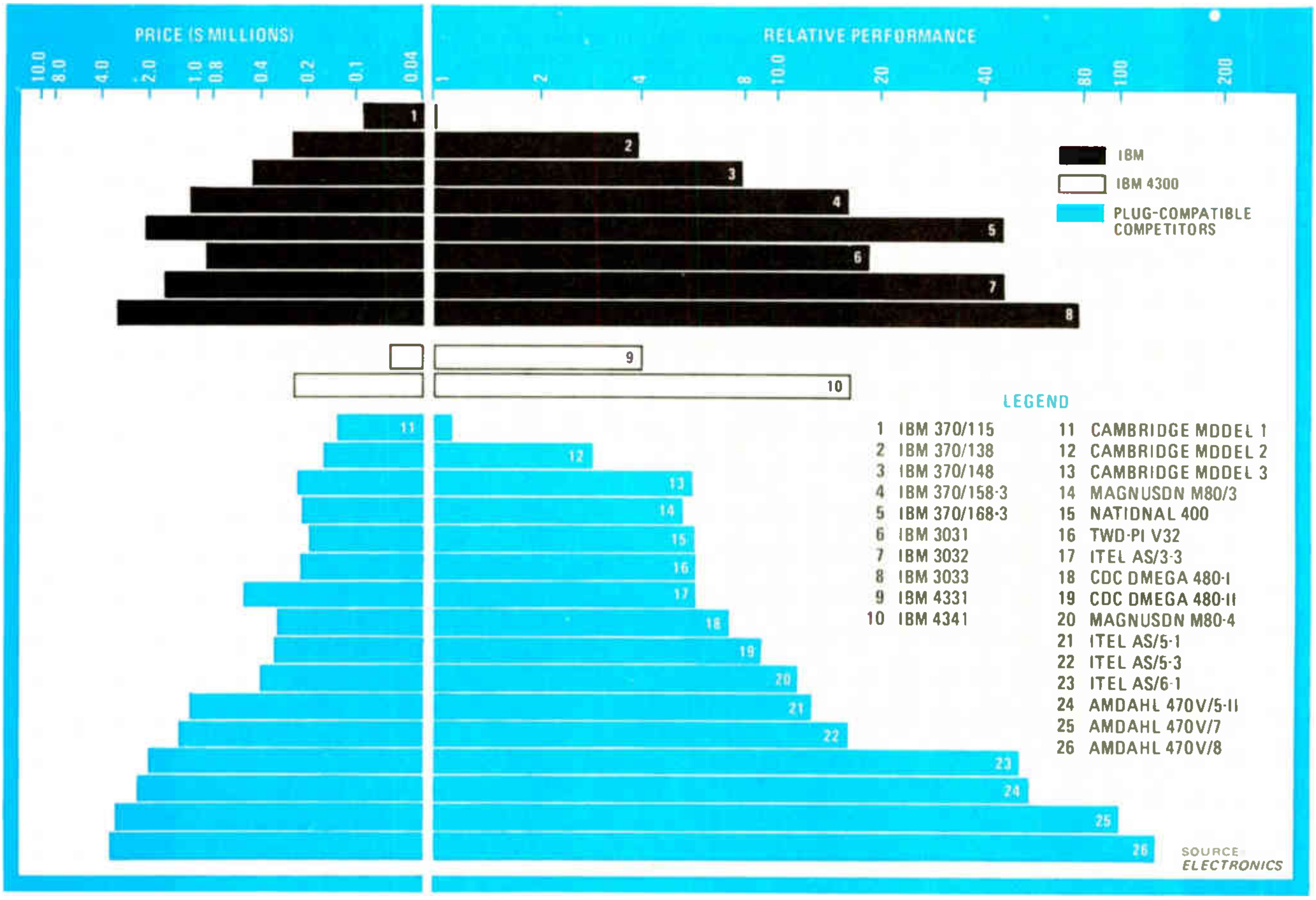
by Anthony Durniak, Computers Editor

International Business Machines Corp. is using a technological key to lock the door to the IBM-compatible market.

Already, the so-called plug-compatible manufacturers are taking countermeasures. But will their efforts be in vain?

Traditionally, these vendors use more modern technology than IBM to offer add-on memories, disk drives, terminals—and lately, entire computers—that can be interchanged with the IBM units, but offer better performance and lower prices. But in its new 4300 mainframes introduced a month ago [*Electronics*, Feb. 15, p. 85], IBM upgraded its semiconductors, resulting in more powerful units with dramatically lower price tags. Coupled with a startling $15,000-per-megabyte memory price and new disk drives, the 4300 will affect the entire spectrum of plug-compatible products. As one competitor says, "Instead of moving down the technology price curve a little at a time the way we did, IBM moved in one giant step."

Comparing the various units in terms of a relative performance scale drawn up by Datapro Research Corp., Delran, N. J., and their basic purchase price, the chart shows the large number of machines that offer more performance than IBM's System/370 models for the same or less money. The new 4300 computers are estimated to perform somewhere between the IBM 370/138 and 370/158 processors, the range most crowded with look-alikes. But as the chart indicates, their dramatic pricing reduces the advantage of the plug-compatible machines.



IBM spreads out the market. Relative performance vs price of System/370 and 4300 and the plug-compatible competitors shows how IBM has leapfrogged its rivals. Figures are based on composite estimates by Datapro Research Corp. and company claims.

Whether those machines can regain that advantage is in doubt. IBM put the technical screws on the competitors through its heavy use of microprogramming in the new computers.

Most competitors are confident that since their machines are for the most part microprogrammed, they can match IBM. But it is not yet clear what IBM uses the microcode for. Industry analysts expect much of the operating system, including the new single-level virtual memory management scheme, to be firmware. Since the 4300 processors have two modes of operation, it is suspected that the so-called native mode instruction set is different from the System/370's—requiring the competitors to write microcode to emulate the new instructions. And with the reduced price margin, it is not clear if they can finance the reverse engineering and programming effort.

Ready. Many competitors claim that they anticipated the timing and severity of IBM's actions and prepared for them. In Santa Clara, Calif., Magnuson Systems Inc. has already responded. "We'll take the same strategy as IBM—lower the price on the existing model and announce three new ones," says company president Joseph L. Hitt. The Magnuson M80/4 has been slashed by 25% to $295,000.

Hitt will not reveal where he plans to price the new units but notes that "There'll be a computer shortage for the next two years, so the usual pricing strategies don't apply."

Separate price. Kent Crombie, director of computer systems marketing at Cambridge Memories Inc., Waltham, Mass., the newest competitor in the game [*Electronics*, Sept. 14, p. 88], points to the large amounts of separately priced software IBM offers for the 4300. "The hardware is only going to be half the cost of the system. The total package pricing won't be as dramatic as it first seems."

Kenneth Fischer, chairman of Prime Computer Inc., the Framingham, Mass., company that markets minicomputers to IBM users, notes that even with reduced prices the established companies should be able to maintain an edge. "But for new companies, a smaller edge of say two to three times less is not big enough to cover startup costs and to fight the credibility problem with customers," he predicts.

Agreeing is Burt Hochfeld, director of plans and strategies for Telex Computer Products, Tulsa, Okla. Telex acquired an option to market Cambridge's computers, but Hochfeld says, "At this juncture I don't think we'll exercise that option. There's no question that IBM closed off the opportunity in the CPU-compatible area."

Perhaps more serious than their immediate threat, however, is what the 4300s portend. Industry observers view them as evidence that IBM's hardware pricing will be much more aggressive and that much of the new features will be optional extras in the form of separately priced software and firmware.

New rules? This could change the rules of the plug-compatible game. Instead of pure hardware competition, the vendors will have to step up their software efforts, both to imitate the new IBM functions and to offer alternatives. Already Amdahl Corp., which competes with the top of IBM's line, has established a software-development group to meet this challenge (see p. 14).

Another area fraught with technical question marks is the add-on memory business. Using its new 64-K random-access-memory chip, IBM has brought the price of memory down to $15,000 a megabyte. What's more, IBM put other functions on this custom chip that the add-on memory makers will have to match and most likely implement with extra circuitry.

Looking good. The only plug-compatible area that still appears promising is disk drives. As Robert C. Wilson, chairman of Memorex Corp., Santa Clara, Calif., says, "The new products reaffirm that rotating-disk technology will be the memory used in the next generation of computers."

Although the new 3370 drives use thin-film recording heads to double the recording capacity to 517 megabytes, increase the data transfer rate by 55%, and change the recording format, the vendors are confident they can imitate then. The change in the recording format may in fact increase their markets for two reasons. Since the new disk drives do not attach to the older System/370 mainframes, competitors have an opportunity to sell improved drives to that large installed base. Also, if they can find a way to use the old format yet work with the new 4300 operating system, they can eliminate the need for the user to reformat his data when upgrading his disk drives—a time-consuming and costly process.

Despite the specific technical concerns, makers of plug-compatible machines generally are confident that the 4300 will only help the market by expanding the overall demand for computers. □

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Communications

Voice recognition moves along

Researchers at Bell Labs have built a programmable system that can be used for plane reservations and directory assistance

by John G. Posa, Microsystems and Software Editor

If telephony could benefit from any science, it would be the science of human speech processing. So it is no wonder that Bell Laboratories researchers have been acquainting themselves with this field for years. But despite attempts to mimic human speech production with electronic hardware, few such systems have reached the commercial domain.

This is especially true of speech recognition systems, often said to be an order of magnitude more difficult to design than their counterparts, speech synthesizers.

For telephone use, demands appear to be the most stringent. The ideal recognizer would be capable of handling continuous speech, be speaker-independent, and be both accurate and fast (see "Recognizing recognizers"). Larry Rabiner and Aaron Rosenberg, technical staff members of the acoustics research department at Bell's Murray Hill, N. J., facility, have met these requirements with a single programmable word-recognition system.

Two versions. They have coded it (in Fortran) to pick out words in a spoken sentence, but the result is speaker-dependent. They have also modified it to be speaker-independent, but the system relies on isolated words. It seems all that is left to do is to combine the algorithms into one inexpensive system. That, of course, is easier said than done.

Recognizing recognizers

Speech-recognition systems can be characterized in a number of ways. They can be either word-oriented or phonetically based, for example. Systems geared around whole spoken words have stored in memory reference models or templates of the words in their vocabulary. These templates are assimilated during the machine's training period, whereby one or more speakers repeat the words. Their utterances are digitized, stored, and later used as the basis for judgment of the incoming speech. Phonetic systems are similar, except that in place of words they usually use phonemes, generally agreed to be the basic noises in human speech.

Recognition machines can also be either speaker-independent or -dependent, although some systems can be both. Speaker-independent systems, the more elegant, do not care who is doing the talking. Speaker-dependent machines can only be used by the individuals who trained them.

Word recognizers, too, can be speaker-independent. This is managed by training the system with a larger cross section of talkers to arrive at a flexible set of reference templates for each word. Incoming words are then compared with all the reference patterns for each word with the probability of success being related to the number of templates and the method by which they were obtained.

Finally, such systems may or may not accept continuous speech. For true continuous operation, the talker need not pause between words or give the machine any indication of beginnings or endings. It is left up to the system to discover what is valuable speech information and what is not.

The most recent work at Bell actually dates back about five years, when Fumitada Itakura took a leave from Nippon Telegraph and Telephone Public Corp. to do two years' research at the U. S. lab. Itakura is one of the most prominent names in speech research, for he formulated some of the basic principles of linear predictive coding, now heralded as the key to recognition and synthesis at low data rates. Texas Instruments Inc., for example, uses the coding in its Speak & Spell chip [*Electronics*, Aug. 31, 1978, p. 190].

To demonstrate continuous speech recognition, Rabiner, Rosenberg, and Itakura set up an airline flight-reservation system, still being improved. It is speaker-dependent and word-oriented and has a vocabulary of over 125 words associated with airline information. Names of cities, times of day, and other words like "fare," "nonstop," and "seat" are included in the machine's word list.

To operate the machine, a user picks up the phone and asks questions about flights. Responses come from a synthesized voice.

Cerebral approach. If in the course of a conversation the machine is asked, "How much is the fare?" it will first examine the very beginning of the question and develop a small table of words, time frames, and probabilities. The time frames are listed using two values, a beginning and an end, and the probability indicates the likelihood the associated word is in that time frame.

After the first table is constructed, the system bites off more of the sentence and builds a second table, using as its time-frame beginnings the end values developed in the first table. However, for each entry in a table, there will be several possibilities for the next word, so that each successive table grows almost exponentially in size, even when the ridiculous possibilities are ignored. When the machine is finished making all the tables, which takes under two minutes for this particular question, it adds up all the probabilities to find the most likely sentence. It is accurate more than 90% of the time for the words themselves, and over 70% correct for the entire sentence.

Rabiner and Rosenberg's latest version of the machine, created primarily by using a novel approach to the template-making process, is adapted to telephone directory assistance, and its big feature is that it works independently of the speaker. The system, which can understand most American dialects and some foreign accents, currently recognizes 39 spoken words. Twenty-six of the words are the enunciated letters of the alphabet, 10 are the numbers 0 through 9, and the remaining 3 are "stop," "error," and "repeat." To obtain a telephone number through the experimental system, the caller simply spells out the first five letters of the last name and the initials, pausing for at least a tenth of a second between the letters.

In training. The system uses three modes of operation. When it is being trained (mode 1), 100 test speakers, half male, half female, say each of the 39 words. The words are passed through an autocorrelation analyzer, which averages the input with a time-shifted version of the speech itself. The result of this averaging is a number of coefficients (9 for each 45 milliseconds of speech) used later to calculate a model of the speech patterns.

During the clustering process, the second mode, the coefficients for the same word from each speaker are compared to pinpoint any similarities. With the help of Steve Levinson, another Bell researcher, Labiner and Rosenberg discovered an interesting bonus during the clustering of the words: only a dozen coefficients (instead of a full 100) were required to recognize the speech of a broad population.

When the system is used, the caller's words are pitted against all 12 reference templates to find a match. This takes approximately 5 seconds per spoken letter, for a total of less than a minute for the entire name.

If the computer makes a mistake in judging a letter, it will look for a name that is not in the directory. Failing to find a match as it builds up a name form left to right, it substitues the next most likely letter and looks again. The combined efforts of the recognizer and this self-correcting strategy yield a system that is correct 97% of the time.

Labiner points out that an advantage of the Bell designs is that they are algorithmic in nature. "No heuristic logic is involved," he says, "the system can be used for one application one day and another the next, without changing anything except the program."

Although other groups at Bell Labs are studying linguistics in general, and phonemes in particular, for possible incorporation into the machines, the experimental Bell recognizers are all word-oriented. Also common to the systems is the hardware. For one thing, "They all make use of the telephone," boasts Rosenberg. The phones are not just connected directly to the system; it has its own extension, which the researchers dial up. The machines also rely on a Data General Eclipse S/230 computer and, for the fast multiplications, a MAP-200 floating-point array processor from CSP Inc., Burlington, Mass.

The researchers agree such equipment is overkill. For the speaker-independent system, for example, "you'd need a fast dedicated multiplier on the input, a microprocessor for the analysis process, and a bank of microprocessors for the comparisons with the reference templates," says Rabiner.

"It would require about one microprocessor for every 10 words in the vocabulary and one multiplier for every 40 words. It could probably be done with today's components for about $2,000, but nobody has really done a detailed hardware analysis."

Better. As for the future, Rosenberg states that efforts will continue to make recognition systems more capable: to have larger vocabularies, to be more speaker-independent, to be more natural to use, and to correct poor grammar.

Competent recognizers could be applied to several tasks, especially in the telephone system. Besides directory assistance, which would be beneficial in itself, people could dial a phone simply by saying the number they wished to reach. This would further reduce the number of mechanical components, possibly eliminating them altogether.

And when synthesis and recognition are used together, the possibilities are startling. Consider a system that would allow a conversation between people who do not speak each other's language—for example, a machine that could recognize English, translate it to French, then do the opposite in the other direction. Though he admits it is possible, Rosenberg adds, "You won't see that tomorrow." □

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Manufacturing

Lasers attract chip makers

Their precision in annealing the damage of ion implantation spurs research around the world

by Ben Mason, New York bureau manager, and Robert Brownstein, San Francisco regional bureau

Don't look now, but high-energy lasers may be about to invade semiconductor manufacture. If experiments in laboratories around the world bear fruit, laser heat may be used to anneal wafers after ion implantation (or to replace ion implantation itself), to enlarge the grain size of polycrystalline silicon, to trim devices such as zener diodes, and to form metal contacts. There are many other possible uses.

What makes all this possible is the precision of the laser beam, which heats only the small spot it hits and to a depth that can be fine-tuned. "The laser gives you another control knob," says Walter L. Brown, head of the radiation physics research department at Bell Laboratories' Murray Hill, N. J., installation.

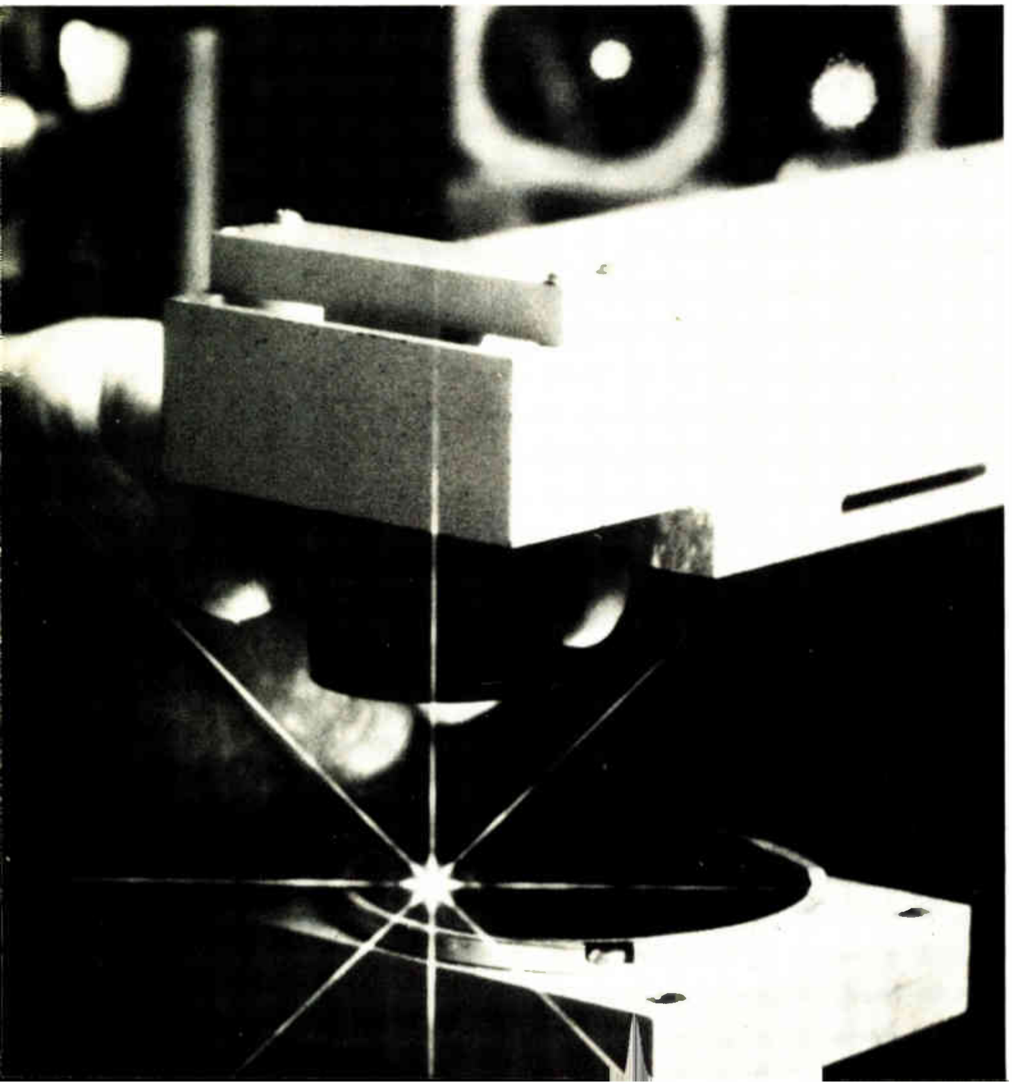
Control. It is not just a matter of controlling the time and area of the heating more precisely, he explains. "You also control the wavelength of light interacting with the wafer. So you're managing extra variables and getting extra flexibility."

The notion of using laser heat in semiconductor manufacture burst upon the research community in mid-1977. Among the labs investigating it are Bell in Murray Hill; the electrical engineering department at Stanford University; various semiconductor makers, including overseas manufacturers such as Siemens AG, NV Philips Gloeilampenfabrieken, Hitachi Ltd., and Plessey Ltd.; the Oak Ridge National Laboratories, run by Union Carbide Corp. for the U. S. Government; and Lockheed Missiles and Space Co.

No ovens. What sparked this interest were reports from the Soviet Union of preliminary work with lasers as an alternative to the oven-heating necessary to restore the single-crystal structure of silicon after its disturbance by high-energy ion implantation. This thermal annealing takes about 30 minutes at 1,000°C, and, while reforming the silicon, can curl the wafers.

Scanning a laser beam across the implanted areas of the wafers, or hitting an oxide-masked wafer with a beam that can cover from a third to all of the surface, appears much faster, perhaps less costly because of its speed. Whether or not this proves the case, "if the more expensive laser method gives a higher yield, the price of that method is secondary," says Eberhard Krimmel, head of the Munich research team investigating laser annealing for Siemens.

Investigators of laser annealing



Hot flashes. Neodymium YAG laser, in green portion of spectrum, pulses its spot onto silicon wafer at Western Electric lab.

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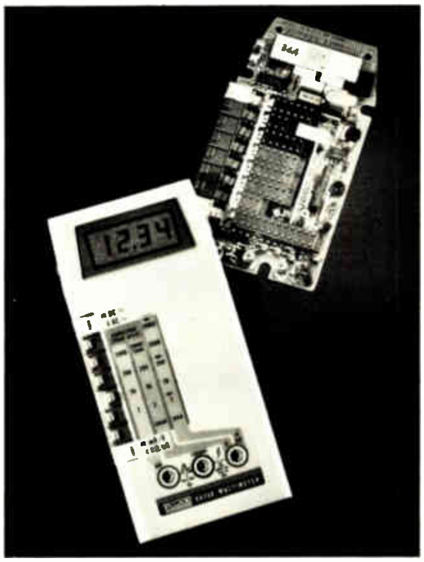

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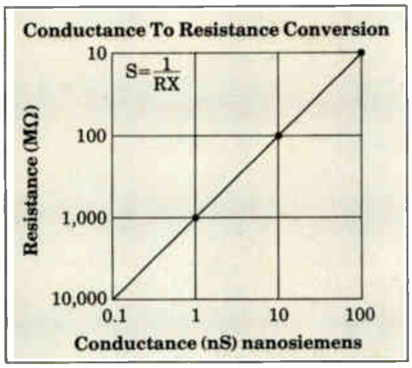

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seem generally to agree with Krimmel, although research is hardly far enough along for cost-accounting. However, diverse approaches are emerging from the labs.

A major question is whether to use the liquid or solid mode of laser annealing, and a related one whether to use pulsed- or continuous-wave lasers. The liquid mode actually melts the wafer surface to a carefully controlled depth, causing rehomogenization of the silicon and, as a bonus, activating the ion impurities better than oven annealing. The solid mode is more like the oven method, heating the wafer for over a millisecond to somewhat less than the melting point. It does not leave rough surfaces—sometimes a problem with the melting mode—but, unlike the liquid mode, depends on such factors as crystal orientation and the concentration and type of ion impurities, Brown says. The solid mode also requires more energy over a longer time, so it is more expensive.

Pulsed lasers. Most experimenters appear to be working with the liquid mode, the majority using Q-switched ruby or neodymium yttrium-aluminum-garnet-pulsed lasers to get the microsecond flash of energy necessary to melt the silicon. Scientists working on the solid mode, notably James F. Gibbons at Stanford University in Stanford, Calif., generally use a continuous-wave gas laser.

A big advantage of the laser is its selectivity: only wafer areas damaged by ion implantation need be treated. On the other hand, the beam in both pulsed and continuous-wave lasers is small in relation to the wafer, so it takes longer to anneal large areas. Plessey's Alan Clark Research Center in Caswell, England, is working with masking techniques that could cut the time.

Plessey puts down a silicon-oxide mask over the entire wafer, leaving windows where ion implanting takes place. Then it is possible for the laser beam to sweep across the wafer, annealing through the windows. With a big enough beam, an entire wafer could be annealed in two or three pulses—eventually, perhaps, with a single pulse.

Nor is silicon the only material under study. Thomson-CSF's central research lab in Corbeville, France, for one, is working with gallium arsenide.

If the big-beam method pans out, competitive throughputs may be obtained, says Siemen's Krimmel. "We are shooting for a throughput of one 3-inch wafer every 30 seconds, which matches that of typical ion-implantation equipment and is also the goal of other companies." That amounts to 60 every half hour; the wafer boat in an annealing oven typically handles 50 wafers.

One use of the single-beam that could answer researchers' prayers is in annealing photovoltaic silicon cells. A team led by Michael Lopez at Lockheed Missiles and Space Co., Sunnyvale, Calif., has succeeded in turning out 15% efficient solar cells using a conventional YAG laser with a 2-mil spot size. Oven-annealed cells reportedly are averaging 8%.

However, the DOE also wants to slash the cost of solar electricity from the present $11 per peak watt to 50¢, and the secret here is mass production of the cells. Since the entire wafer is implanted with ions to make the solar cells, a wafer-sized beam is the key, Lopez thinks. Lockheed will buy a laser with a 1-in. spot and a repetition rate of four pulses per minute—but lasers with beams even as big as the present 3-in. wafer diameter are still a dream.

Electron beams. Well beyond the dream state is a strong competitor of the laser for semiconductor applications. Pulsed electron-beam techniques are also under consideration for such tasks as annealing solar cells, and at least one company is readying equipment.

With laboratory work still the order of the day in laser annealing, some side effects remain to be fully investigated, says Bell Labs' Brown. For one, the rapid buildup of heat in the silicon may be creating point defects—atoms missing or out of place. The electrical effects of these defects are unknown at present, he says, and "modest heating following the annealing can dramatically reduce the defects."

A second side effect may be strain defects in the crystal created by the very small, very intense heat spot, Brown says. While it looks as if this effect will be no problem, investigation is far from complete, he reports.

It is not only single-crystal silicon that responds to the laser's heat. At Stanford, Jim Gibbons is using continuous-wave lasers to lower the resistance of polycrystalline silicon. Polysilicon is used for interconnection and ohmic contacts, where low resistance is crucial.

Gibbons increases the size of the material's grains, apparently by melting the surface with the cw beam. Most of the impedance is in the boundaries between the grains; the larger the grains, the fewer the boundaries. He reports typical results of a drop in sheet resistance of boron-implanted samples from 12.5 megohms per square centimeter to 269 ohms/cm^2.

Bell Labs has worked with polysilicon's grain size using the pulsed lasers at Western Electric Engineering Research Laboratory in Princeton. Walter Brown reports that sliding the pulsed spot across the surface caused the molten grains to orient themselves in the direction of the motion, further cutting resistivity. He says that Bell, as well as Gibbons, is investigating the possibility of growing the conducting path as one grain. Philips' research unit in Amsterdam and the Siemens team are also studying grain growth.

No more implantation. Most labs, in fact, are investigating several potential laser applications on semiconductor production lines. Among the uses under study at the Oak Ridge labs in Oak Ridge, Tenn., is bypassing the fussy and troublesome ion-implantation process.

"Ion implantation is very costly," says Rosa Young, a research staff member at the labs. "You can avoid it with electron-beam evaporation of a film of the doping material and a laser driving it in."

The Oak Ridge researchers are using pulsed lasers to melt the silicon surface with a power of 1.2 to 1.5 joules per square centimeter. Young expects that "any kind of painting or spraying technique" could replace the electron-beam evaporation, cutting costs even more. □

Additional reporting came from Arthur Erikson, Paris; John Gosch, Frankfurt; Kevin Smith, London; and Pamela Hamilton, Boston.

Solid state

Shortages have an air of déjà vu

Double ordering of semiconductors rakes up five-year-old coals, with worst pinches in high-technology devices

by Howard Wolff, Assistant Managing Editor

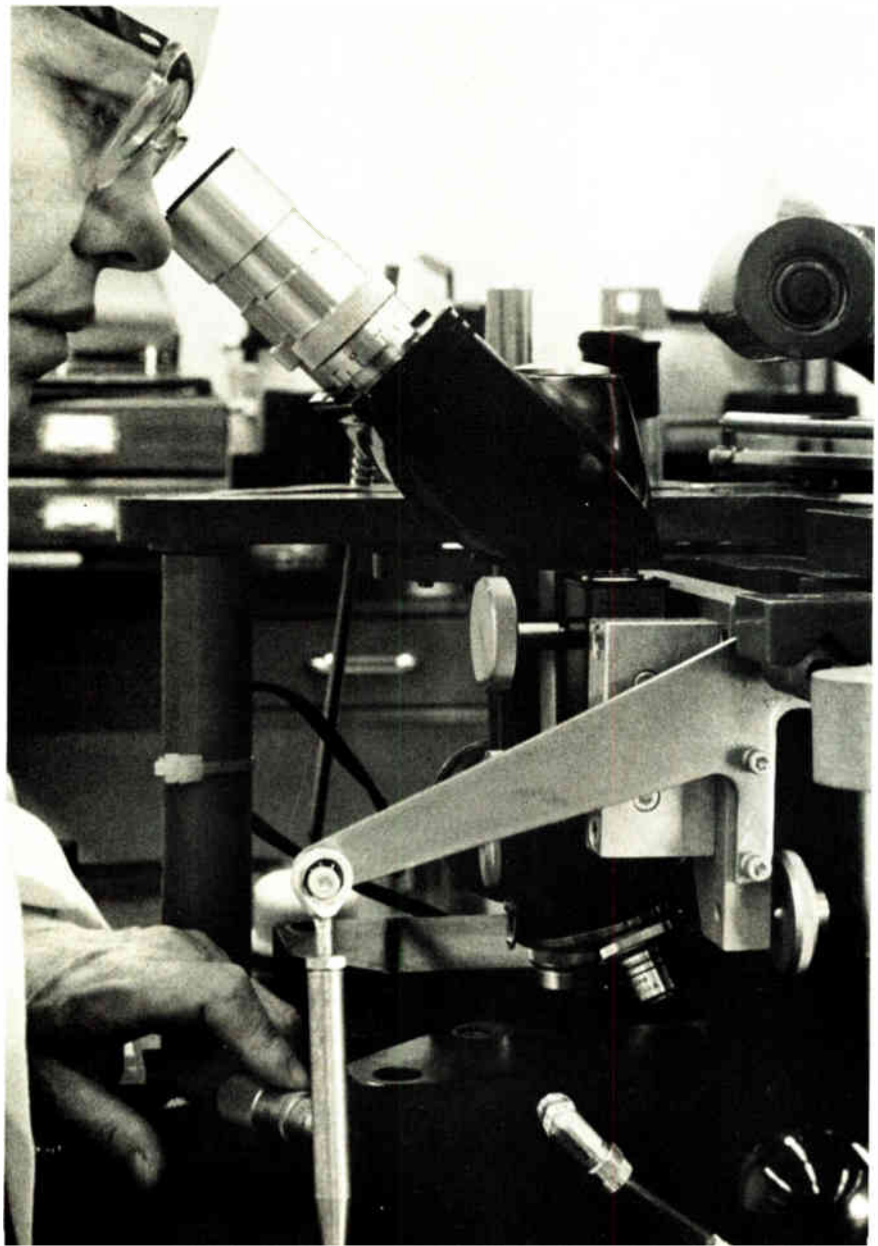
It hasn't reached the panic stage yet, but unprecedented demand for semiconductors has forced manufacturers to stretch delivery lead times and, in some cases, resort to allocation.

The result has been an outbreak of double ordering, the first since the bad old days of the 1974 slump, in which users place orders with several sources—distributors or manufacturers—to ensure eventual delivery. Most of the demand and shortage is in the high-technology products, with low-power Schottky integrated circuits singled out repeatedly. One Texas observer says that lead time is 40 to 52 weeks, and some manufacturers are refusing to take orders. He attributes the problem to Texas Instruments Inc. "because TI occupies about 42% of the market. And once they get into trouble, it shifts onto the balance of the market and it ain't long until nobody's got nothin'." Acknowledging the stretch, TI has put its customers and distributors on allocations for most transistor-transistor-logic parts as well as random-access and erasable programmable read-only memories. This program is very well received by customers, according to TI.

Wherever the shortage starts, the consensus is that not only is low-power Schottky being quoted at up to a year [*Electronics*, Feb. 15, p. 50], but the squeeze also is being put on standard Schottky parts. There, the lead time in some cases is nine weeks as opposed to five weeks only a month ago.

The ripple effect of such a situation is not being felt yet, but can't be too far behind. In Southern California, for example, where minicomputer manufacturers are big users of Schottky circuits, the delay in getting parts—now only up to 26 weeks—has not yet hurt. However, the feeling is that machine deliveries will be hard hit by the year's end.

Also vulnerable. Memory devices are not immune to the pinch. At Mostek Corp. in Carrollton, Texas, national sales manager Dick Konrad says, "Unquestionably, we will have to allocate some products" beginning this month. The primary products in



Trying to keep up. With demand for their products at a peak, semiconductor makers are working three-shift days to keep pace.

high demand from Mostek are 4,096- and 16,384-bit dynamic RAMs, 4-K static RAMs, and model 2716 E-PROMs. For the dynamic parts the lead time has stretched to 22 weeks; for the 4-K static devices it is at 16 to 18 weeks. As for the 2716s, since Mostek is just beginning to build them, the company has not made any long-term commitments, though "we could extend the lead time to six to nine months," says Konrad.

The reason for the shortages is not only production problems. In fact, manufacturers are turning them out at higher-than-ever rates. For example, Mostek says it is building 4-K dynamic RAMs at a pace exceeding its annual plan, while its 16-K parts production is right on schedule. It also has been running triple shifts for some time, and is bringing up a new fabrication line in Carrollton with a second one scheduled to be running by the end of the year.

National Semiconductor Corp. in Santa Clara, Calif., points to another aspect. Frank J. Barone, director of bipolar memory components, says that in short supply are wafers coming in one end and programmable ROMs going out the other. The wafer shortages began to appear three to four months ago, says Barone, and supplies are now 10% to 15% short.

Progammable ROMs began to stretch out before Christmas, when delivery was 4 to 6 weeks, until last month when the time stretched to 20 weeks. Barone attributes the shortage partly to 8- and 16-K programmables "getting into production and eating the capacity for 1- and 4-Ks. But when a 4-K comes out, it doesn't replace a 1-K."

What's next. Whether the situation gets as bad as it did five years ago "depends on whether the semiconductor manufacturers allow it to happen," says Mostek's Konrad. If the situation gets too bad, he intends to ask customers and distributors to cancel or reschedule their standing orders. That would have the effect of forcing users to scrutinize their orders to determine what they really need. □

COMPUTER LABS TEAMS UP

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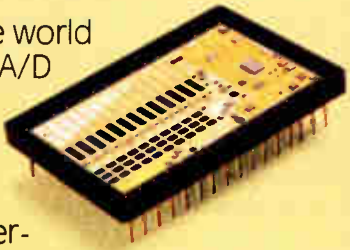

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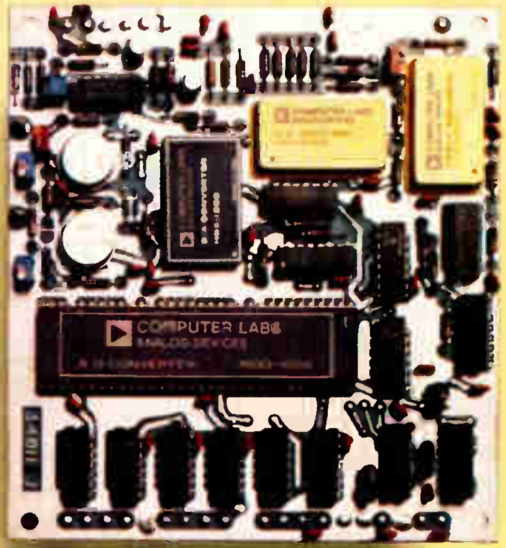

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Commentary

Equipment makers worry over VLSI

Anxious about technical and financial problems, semiconductor production firms feel the V in VLSI stands for Valium

by Larry Waller, Los Angeles bureau manager

Some disturbing thoughts about the arrival of very large-scale integration are now causing semiconductor equipment manufacturers to lose sleep. They are suffering from a bad case of future shock, because the future is now.

Certainly the equipment suppliers have it made this year. It looks as if these companies will breeze through 1979 as domestic and overseas customers continue to demand more and more lithography equipment, sputterers, and the like.

But the reason for sleepless nights is the glamour technology of the 1980s—very large-scale integration, perhaps the stiffest challenge these firms have had to meet. Their ingenuity and financial resources will be tested to the fullest to develop what amounts to a quantum jump, a brand-new generation of production equipment and materials. The nub of the problem is that the production machines of the 1980s must be able to turn out devices with line dimensions much smaller than today's 3 or 4 micrometers, at a price users can pay. Moreover, this equipment must be reliable in a production environment.

Hard realities. While the companies that supply the semiconductor industry with capital equipment have been worrying about the VLSI challenge, they apparently had not anticipated coming to grips with the problems quite so soon. This situation surfaced at the recent Semiconductor Equipment and Materials Institute (SEMI) annual conference in San Diego, Calif., where top consulting firms involved in the semiconductor industry warned attendees to get cracking.

Taking on the Japanese

In contrast with most U. S. business, head-butting on prices with the Japanese does not scare semiconductor production equipment makers. Executives of these and U. S. materials suppliers attending the SEMI meeting in San Diego agree they have about a 30% lower price advantage.

Surprisingly, the main reason, in the opinion of one Silicon Valley manufacturer, is that U. S. facilities use less labor; in addition, the appreciation of the yen helps. "We already beat them outside," this observer says, "and could do the same on their home ground if we could sell freely there." But prospects for lifting the trade restrictions that keep U. S. firms at a disadvantage are dim, he concedes.

"Forget this year, because you're already locked into it," one speaker advised. "Instead, focus your planning on 1981."

In fact, 1981 was labeled "your biggest transition ever" by veteran consultant Glen R. Madland, president of Integrated Circuits Engineering of Phoenix, Ariz. "A time cycle that takes longer to react to makes it imperative that planning start right now," he added. This admonition surprised many who had figured that there was time.

As if the technological problems are not enough, soaring costs are also a headache. One example is the new direct-step lithography system, which involves incremental scanning of the wafer rather than scanning the entire wafer at once. The direct-step method, while an improvement, costs up to four times more than the present lithographic method. It means that equipment firms will have to tout improved productivity to justify higher prices.

Broke. In the VLSI era, financing the equipment goes beyond the usual paying for R&D and capital expansion and must actually consider whether the customer can afford to buy. For example, Frederick L. Zieber, director of industry service for Dataquest, points out that in the early 1970s a $2 million fabricating module could turn out some $20 million worth of products. Today, however, it takes $10 million to acquire an equivalent module that at best can do $30 million in products largely because of the steep price declines in the semiconductor industry. Clearly the industry is reaching what seems to be the point of no return. In addition, the semiconductor firms are already strapped for capital from financing the explosive growth of the past three years.

The implications of all this advice to SEMI members of course go beyond this segment of the electronics industries. Essentially, the timetable for preparing for VLSI has moved up sharply in a period of tight capital. As a result, the entire industry has to reexamine its plans. Users expecting to design with VLSI may actually have to wait until capital expansion funding catches up with the technology. Therefore, the message to SEMI at San Diego was actually a message to the entire electronics community. □

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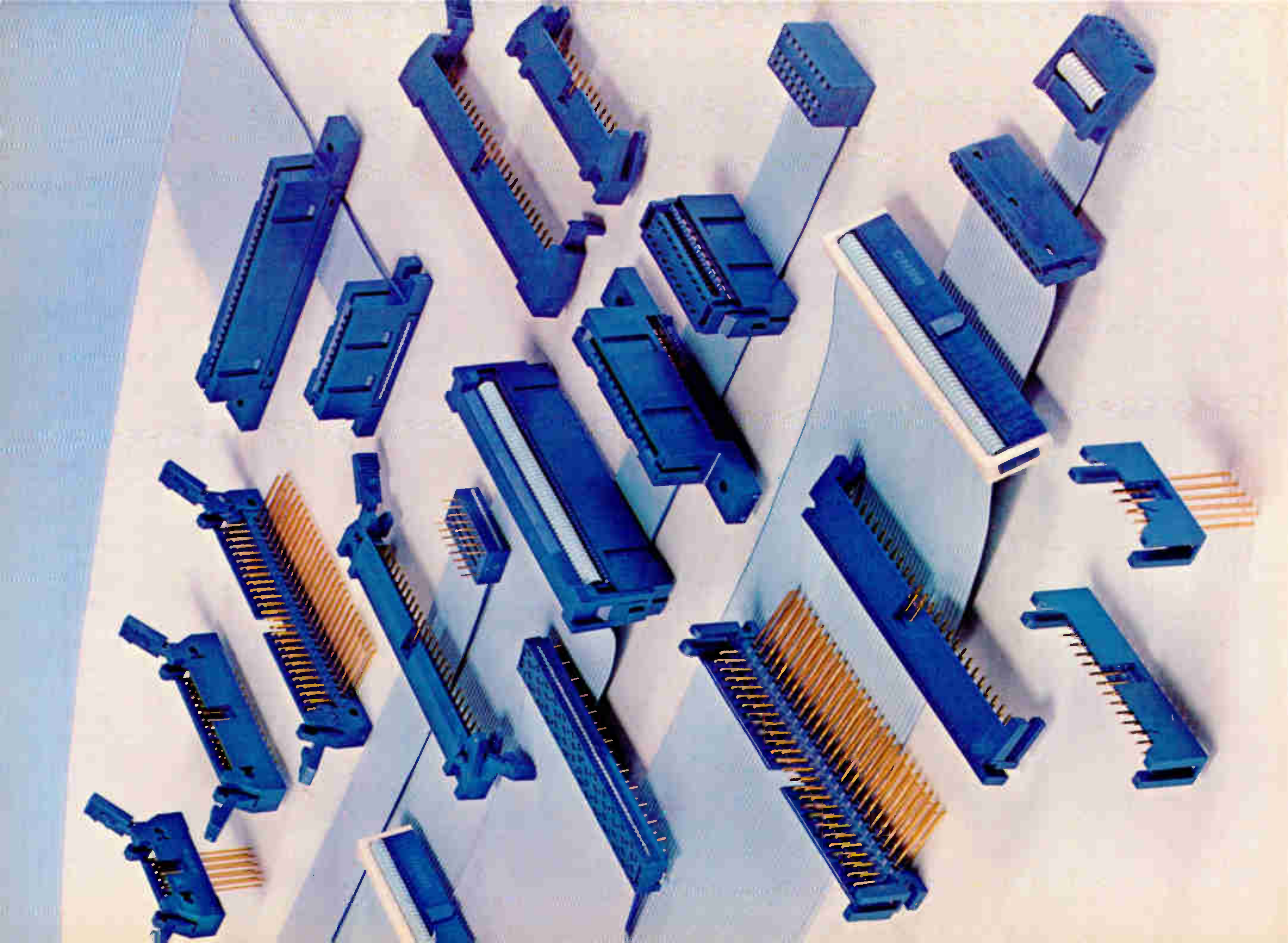

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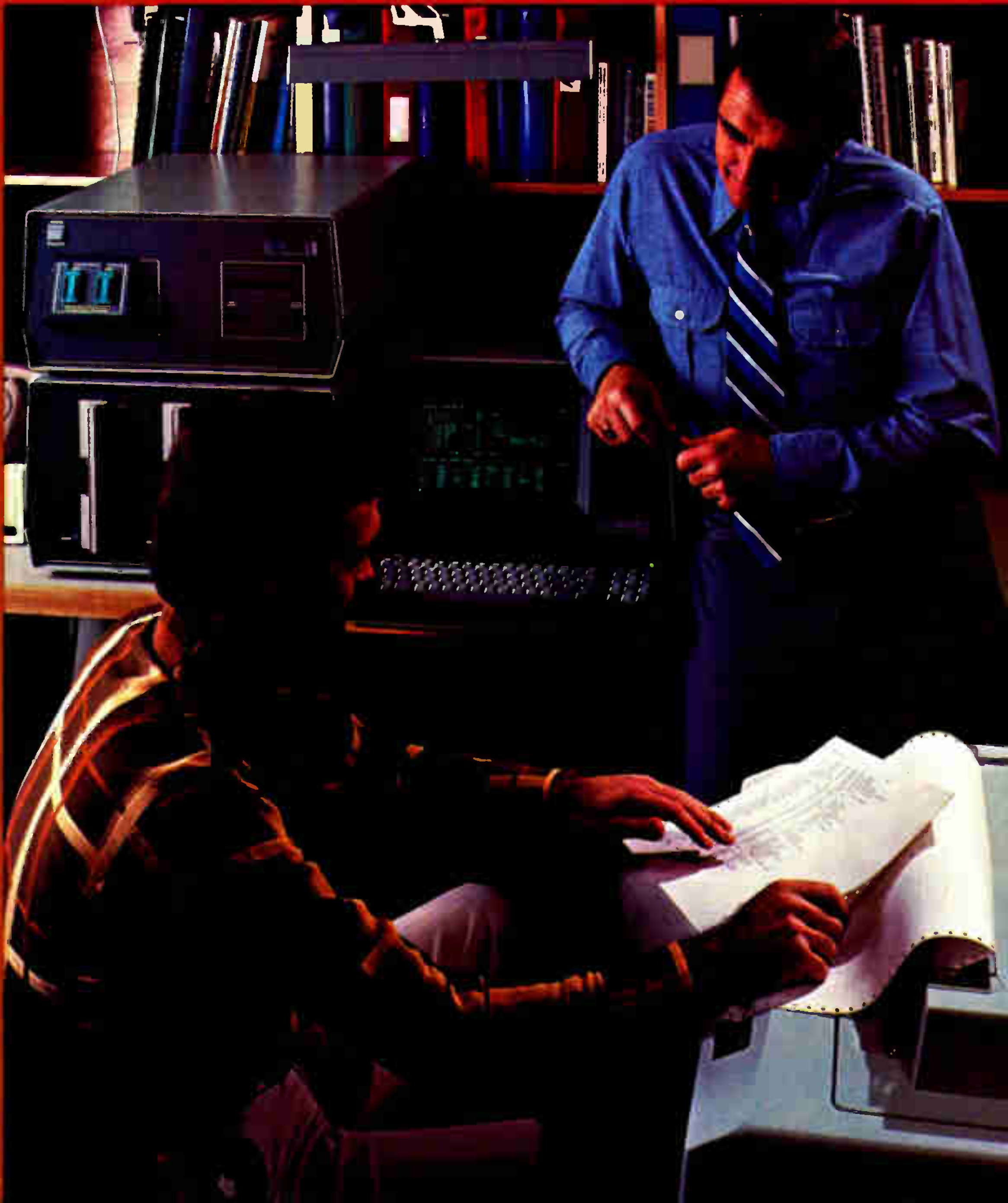

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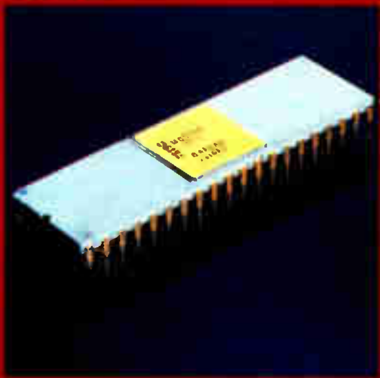

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Single-chip n-MOS microcomputer processes signals in real time

Analog inputs and outputs surround high-speed pipelining processor; user builds filters, oscillators, other analog systems with E-PROM software

by M. E. Hoff and Matt Townsend, *Intel Corp., Santa Clara, Calif.*

□ Digital processing of real-time analog signals, attractive because the waveforms can be manipulated like numbers under program control, has been confined to especially configured high-speed processors that can handle the calculations necessary. Now, just as the microprocessor put low-cost computing power into the hands of the logic designers, a device from Intel Corp. is offering analog system designers a new tool: programmability, in the form of its single-chip real-time signal processor, the 2920.

The chip was conceived out of a pressing need for a programmable circuit to serve the various protocols and modulating techniques used in telecommunications circuits. It combines analog-to-digital and digital-to-analog converters with a specially configured microcomputer to build a device with a unique instruction set, one capable of programming entire analog subsystems.

The kind of functions the 2920 can perform—filtering, modulating, detecting, limiting, mixing, and more—usually require lots of passive components, operational amplifiers, and other such discrete and linear devices. With few outboard components, the 2920 can build such complex devices as modems, equalizers, tone sources, and tone receivers; the 2920 can also be used for such nontelephonic applications as process controllers and motor or servomotor drivers.

Programmability is what gives the chip its great advantage: the contents of its on-board erasable programmable read-only memory (E-PROM) customizes it for each application.

Significant differences

The processor in the 2920 differs significantly from a conventional general-purpose microprocessor. There is some resemblance: it processes digital data from a conventional a-d converter at the chip's input and feeds the result to an output d-a converter. However, the kinds of calculations needed for signal processing differ greatly from those of data processing.

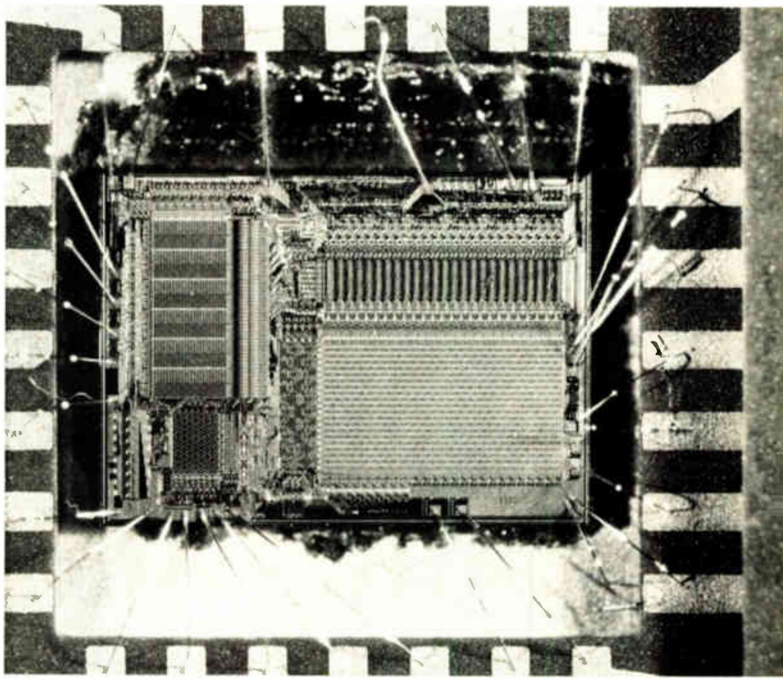
Moreover, since the operation is based on a real-time sampling system, the 2920 must run through its entire program each time it receives a data sample from the input a-d converter. The program execution time determines the sampling rate, and that in turn restricts the operation of the microprocessor in certain ways.

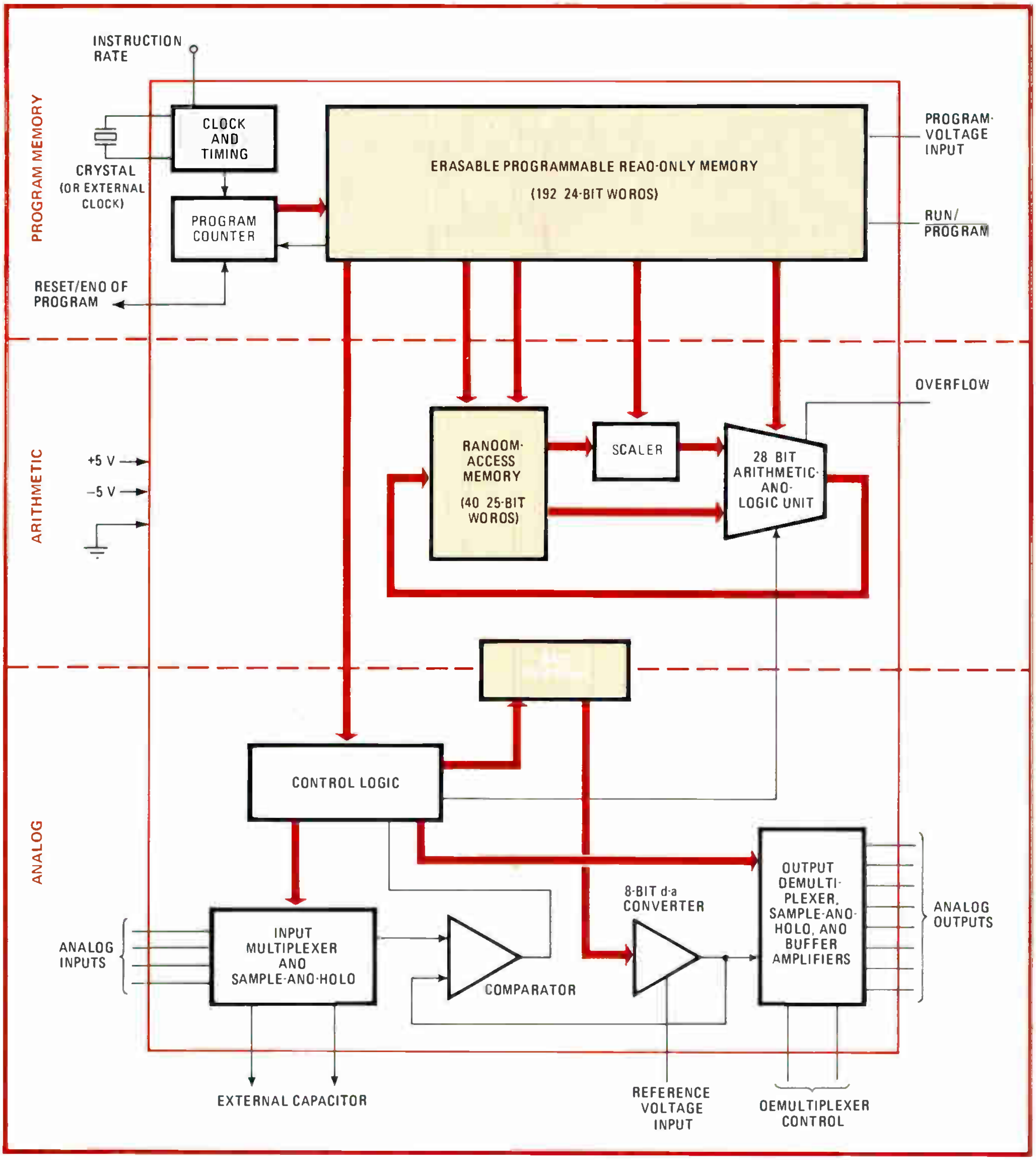
In general, a fixed rate is necessary because the characteristics of any simulated analog system are affected greatly by it—in fact, even small perturbations in sample rate can add intolerable noise to a system. Therefore, the time in which the 2920 runs through its program has perforce to be fixed.

Cut to fit

To achieve that, the 2920 executes each instruction in the same amount of time, regardless of the operation. Also, to ensure that the total program execution time will never vary, no conditional-jump instructions are in the instruction repertoire (save for the jump from the end of the program back to the beginning). Conditional

1. Analog microcomputer. Entire analog subsystems can be programmed with Intel's 2920 real-time digital signal processor. The 47,000-mil² device surrounds a special central processing unit with a-d and d-a converters, all under E-PROM program control.





2. Architecture. The 2920 is programmed with 24-bit instructions, up to 192 of which are stored in E-PROM. The digital section pipelines instructions to boost throughput and interfaces with the analog section through the data register, which appears as memory location.

operators, however, do allow logical operations to be carried out without any variation occurring in the program execution time.

Although these techniques do somewhat restrict programming, they establish a fixed sample rate, based on the time needed to execute one pass through the program. The rate can thus be computed simply as the instruction execution rate divided by the number of instructions in the program.

For digital processing of analog signals on a sampled basis, the microprocessor must be extremely fast if any decent bandwidth is to be attained. Nyquist's theory dictates that a continuous system can be accurately simulated on a sampled basis only if the sampling rate exceeds twice the highest frequency present in the signals being processed—and most practical situations call for an even higher sampling rate.

On top of that, since all the calculations associated

Simulating with sampling systems

The operation of the 2920 finds its basis in sampling theory, which states that a continuous function (or waveform) can be accurately represented by a train of periodic samples, as long as the sampling is done with high enough frequency. It is the high sampling rate required—and more difficult still, the immense computational grind between samples—that has restricted the digital processing of analog signals to full-blown machines. The 2920 solves the number-crunching problem with a pipelined architecture and a clever multiplication algorithm that requires many fewer circuits and steps than the shift-add algorithms with which most computers multiply numbers.

The RLC active filter shown below in A has a frequency response that produces a complex-conjugate pair of poles. The characteristics of the filter—its transfer function, gain, and pole locations—are given by the equations.

The continuous filter can be simulated by the sampling system in B. The circled Xs represent multipliers, the circled Σ is an adder, and the blocks with z^{-1} represent timing delays of one sample period. Coefficients β_1 and β_2 control the filter's frequency parameters, while coefficient G adjusts its gain.

The equations to the right of the figure give the simulated filter's response. Although a sampling system, the filter would simulate exactly the continuous function in A, were the sampling done at infinite frequency: coefficient $\beta_1 = 2e^{-aT}$ approaches the value 2 as the sample period tends to zero; similarly, coefficient $\beta_2 = -e^{-2aT}$ approaches -1. However, at finite sampling frequencies, small errors in those coefficients can cause significant changes in the characteristics of the filter, and all arithmetic must therefore be performed with high precision.

A general-purpose digital computer is able to simulate the sampling stage in B with three equations:

$$y_2 = y_1$$
$$y_1 = y_0$$
$$y_0 = \beta_1 y_1 + \beta_2 y_2 + Gx$$

where the variables to the left of each equals sign are assigned the values to its right. Note that each multiplication involves one variable and one value that is fixed by the design of the filter. Instructions in the 2920 are set up to add or subtract a variable from another where the first variable is scaled by a power of two. Thus a single instruction could take any of the following forms:

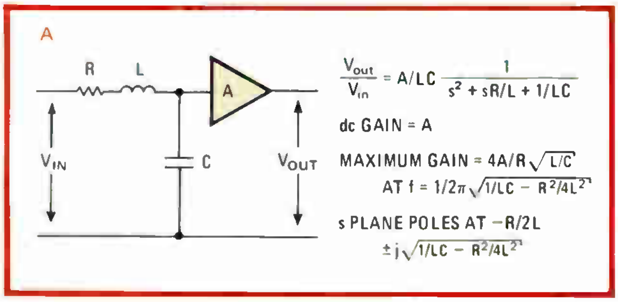
$$x = y(2^k)$$
$$x = x + y(2^k)$$
$$x = x - y(2^k)$$

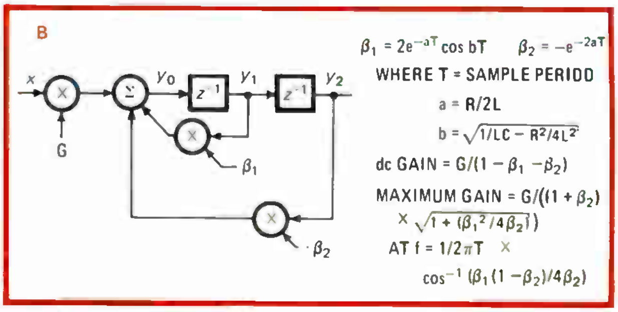
The usefulness of scaling by powers of two soon becomes clear. The coefficients can be expressed in sums and differences of powers of two, as in the examples:

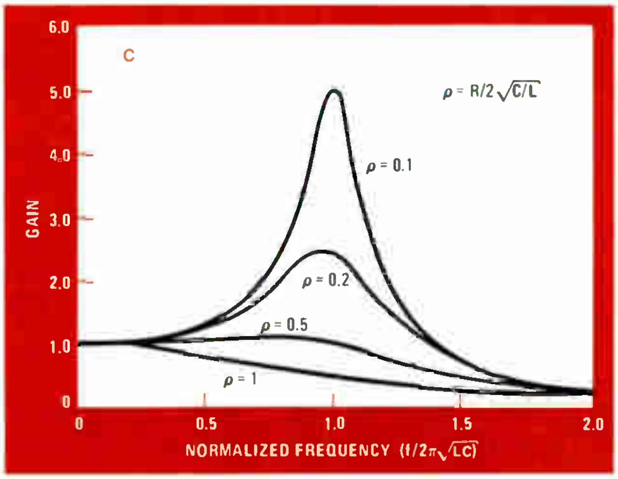
$$\beta_1 = 1.7656 = 2^1 - 2^{-2} + 2^{-6}$$
$$\beta_2 = -0.99414 = -2^0 + 2^{-7} - 2^{-9}$$
$$G = 0.00293 = 2^{-8} - 2^{-10}$$

which the 2920 can perform quickly and with a minimum of circuits. The filter stage of B is carried out directly with 2920 instruction in table D. A left-shift of 1 is equivalent to multiplying by 2^1, a right-shift of 6 multiplies by 2^{-6}, and so on. The mnemonics LDA, ADD, and SUB represent load, add, and subtract operating codes.

This method permits much faster multiplications by constants than a conventional shift-add multiplier could achieve. It is especially effective here because such multiplications dominate digital-filter calculations.

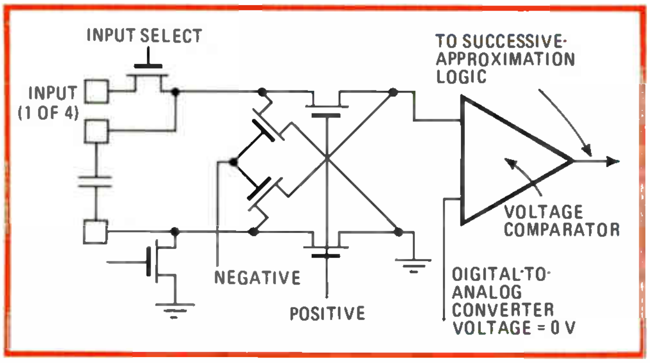




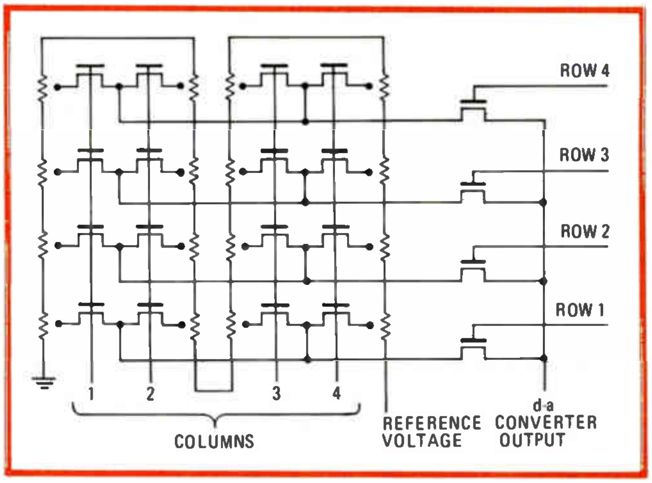


D: INSTRUCTION SEQUENCE FOR TWO-POLE FILTER

Instruction				Comments
Operation (3 bits)	Source (6 bits)	Destination (6 bits)	Shift (4 bits)	
LDA	y_1	y_2	none	equivalent to $y_2 = y_1$
LDA	y_0	y_1	none	equivalent to $y_1 = y_0$
LDA	y_2	y_0	left 1	
SUB	y_1	y_0	right 2	
ADD	y_1	y_0	right 6	now have $y_0 = \beta_1 y_1$
SUB	y_2	y_0	none	
ADD	y_2	y_0	right 7	
SUB	y_2	y_0	right 9	now have $y_0 = \beta_1 y_1 + \beta_2 y_2$
ADD	x	y_0	right 8	
SUB	x	y_0	right 10	now have $y_0 = \beta_1 y_1 + \beta_2 y_2 + Gx$



3. Sign bit. Adding a sign bit to basic 8-bit conversions yields 9-bit precision. The 2920 uses a flip switch to supply a correct-polarity signal from the sample-and-hold capacitor (left) to the comparator used for successive-approximation analog-to-digital conversion.



4. Folded ladder. The 2920's analog-to-digital converter uses a resistive ladder, folded into a square array. That configuration minimizes the effects of process inconsistencies and temperature across the surface of the chip, thus improving overall accuracy.

with the production of an output sample must be performed with each sample taken, the microprocessor must have an extremely high-speed number-crunching capability. Even a 10-kilohertz bandwidth, for example would require sampling at least at a 20-kHz rate, or once every 50 microseconds. A program of, say, 100 instructions, which was executed at a rate of 50 microseconds per sample, would require an average instruction-cycle time of 500 ns—a speed that few minicomputers can boast.

But the 2920 can do it all on a 47,000-square-mil chip (Fig. 1), which, moreover, is built with a standard n-channel metal-oxide-semiconductor process.

Divided in three parts

The 2920, as diagrammed in Fig. 2, divides into three major subsections: program memory, the arithmetic (or digital-processing) portion, and the analog input and output conversion section. The E-PROM program memory controls both the analog conversion and digital sections of the chip.

Four analog inputs enter and eight analog outputs leave the 2920. A multiplexer allows the four analog inputs to share the input sample-and-hold circuit. Analog-to-digital conversion is performed by successive approximation with the output d-a converter, which is the resistor-ladder type. A demultiplexer provides eight buffered outputs, each of which has its own sample-and-hold circuit. The data register links the analog sections to the digital portion of the chip.

Unusual arithmetic

The microprocessor in the 2920 comprises a two-port scratchpad random-access memory, a binary scaler, and an arithmetic-and-logic unit. (The data register used by the analog portion of the chip is actually part of the RAM, so that the processor sees the inputs and outputs as an address location in memory.)

Although the precision of the a-d and d-a converters is 9 bits, internal arithmetic is with 25-bit precision, since accommodating the buildup of small round-off error over time requires much higher precision in the intermediate calculations than for the final value. Should an arithmetic overflow occur, the processor saturates: in other words, it automatically and instantaneously replaces the result with the largest storable value.

To handle the arithmetic, each of the 40 locations in scratchpad RAM is 25 bits wide. Addressing, however, is with a 6-bit word; the additional 24 addresses select predetermined constants and the analog section's data register. To boost throughput, the RAM was designed with dual-port cells that can be addressed through either of their ports.

The E-PROM can store up to 192 instructions of 24 bits each. The instruction format has five contiguous fields: the digital operator, the source address, the destination address, the extent of shifting, and the analog operator. Such a wide word may be likened to a microprogram word in a computer with a control store, for it performs several operations at once. In this case, they are complete memory-to-memory operations.

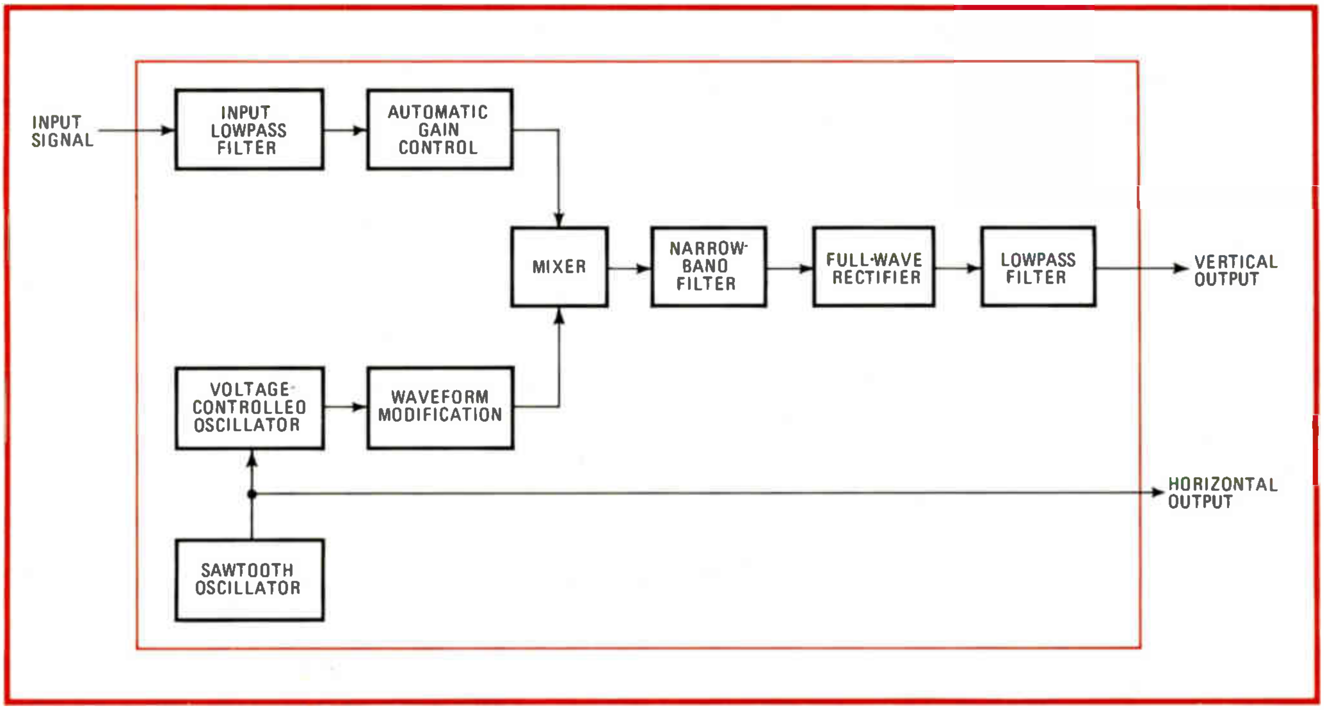
The lower limit

At the 2920's fastest operating speed, each instruction executes in 400 nanoseconds. The largest program the 2920 can handle—192 instructions—executes in 76.8 μs, and thus yields a minimum sampling rate of approximately 13 kHz. The worst-case bandwidth of the chip, according to Nyquist then, is about 6.5 kHz.

Shorter programs will, of course, provide higher sampling rates. Also, techniques like stacking multiple copies of a routine can boost the sampling frequency and hence the possible bandwidth.

To maximize speed of calculation, the 2920 signal processor uses pipelining techniques. Four instructions are fetched from E-PROM at once, and the fetch operation for the next four overlaps execution of the previous four instructions. Moreover, the arithmetic operations are equipped with carry-lookahead across the full width of the accumulator.

The arithmetic-and-logic unit (ALU) carries out such basic operations as data movement, addition, subtraction, absolute magnitude, and several logical operations. Each elementary machine instruction fetches two operands from the scratchpad RAM, passes the first through the binary scaler, performs the selected arithmetic func-



5. One-chip spectrum analyzer. The 2920's resources are sufficient for building an audio spectrum analyzer. The input signal is gain-controlled, then heterodyned with a swept oscillator; the detected sum signal drives the vertical input of an oscilloscope.

tion, and replaces the second operand with the results of the operation.

The key to the 2920's high-speed, high-precision arithmetic is the binary scaler. Unlike the usual shift-add multipliers, which require a cycle per bit, the 2920 uses sequences of scaled additions and subtractions (see "Realizing a complex-conjugate pole pair," p. 107) in multiplying variables by constants to reduce the number of cycles to about a third. (Since most filters used in analog applications are fixed, multiplications are usually by constants.)

The binary scaler modifies a value passing through it by in effect multiplying it by a power of two, or 2^k, where k ranges from +2 to −13. If, as a result, the product is greater than 25 bits (and hence too large for the RAM), the ALU saturates and provides a signal on its overflow output pin. The overflow output is useful during system debugging for determining when scaled variables are out of range.

Conditional options

Some of the ALU's basic operations can operate conditionally, using selected bits of the data register normally associated with a-d and d-a conversions. The multiplication or division of one variable by another is made possible by conditional addition and subtraction, respectively. Finally, conditional operations can perform logic and can generate discontinuous transfer functions.

The a-d and d-a conversions are given 9-bit precision with the addition of a sign bit. A flip-switch circuit, which is shown in Fig. 3, provides the double economy of appending the sign bit while at the same time allowing the 2920 signal processor to use only a single positive-voltage reference.

The d-a converter is built around the folded resistor string and switch array shown in Fig. 4. Folding the resistor string lessens the converter's sensitivity to temperature and process variations across the surface of the chip. That, coupled with the facts that processor timing is crystal-controlled, that the converter's accuracy is established by an external reference voltage, and that all internal calculations are digital, adds up to an analog subsystem that is far stabler than fully analog counterparts.

The resources of the 2920 are sufficient to provide the equivalent of up to 40 poles of filtering, or 20 complex-conjugate pole pairs. That amount is enough to put many complex analog systems, including a dual-tone multifrequency (DTMF), or Touch-tone, receiver on just a single chip.

The power of the 2920 is dramatized by an audio spectrum analyzer, which can display the frequency response of a circuit under test on an oscilloscope. One such analyzer is diagrammed in Fig. 5. It generates vertical and horizontal outputs for direct connection to the oscilloscope and uses heterodyning to mix the input signal with the signal from a swept oscillator.

Sequence of events

The input signal to be analyzed is first filtered with a simple external network to remove high-frequency components that could cause aliasing, or the generation of spurious signals. Once in the 2920, the signal passes through the equivalent of a two-pole low-pass filter for further band-limiting. Next it is modulated, prior to mixing, by an automatic gain control—simply a division algorithm whose divisor is derived by passing the absolute magnitude of the signal through a lowpass filter (to get the weighted average).

A second portion of the program simulates a pair of

6. Two poles. Spectral analysis of a simple second-order filter section centered at 400 Hz displays sharp bandpass characteristics. The two-pole filter uses 10 instructions of the 2920's E-PROM program memory, leaving 182 instructions for other filter functions.

MEMORY UTILIZATION FOR SPECTRUM ANALYZER

Module	Read-only memory words	Random-access memory words
Input filter	20	5
Automatic gain control	18	1
Sweep oscillator	5	1
Voltage-controlled oscillator	7	1
Waveform modifier	10	1
Mixer	12	0
Narrow-band filter	30	6
Rectifier	1	0
Lowpass filter	10	2
Total	113	17

oscillators, the first of which determines the spectrum scan rate—hence, the horizontal sweep frequency of the oscilloscope—and the second of which simulates a voltage-controlled oscillator (VCO) driven by the first. It is the second oscillator, swept through the range of interest, that beats against the input signal in the mixer.

Dealing with aliasing

Both oscillators produce linear sawtooth waveforms; but because the program computes sampled waveforms for these simulated oscillators, aliasing distortion could be a problem if harmonics in the sawtooth were to interact with the sampled frequency and produce spurious frequency components.

For that reason, the output of the second oscillator undergoes a nonlinear transformation in order to approximate a sinusoidal waveform. The 2920 performs the nonlinear transformation with a piecewise-linear approximation that combines absolute-magnitude functions and the effects of overflow saturation in the ALU. The first oscillator, it may be noted, needs no such transformation because it operates at such a low frequency that any harmonics high enough to react with the sample rate are insignificant.

Good mixer

The mixer uses a multiplication routine to combine the output of the second oscillator with the filtered, amplitude-controlled signal under analysis. The output of the multiplier contains sum and difference frequencies. Only the sum frequency is of interest for the analysis, and a narrow-band filter extracts it from the mixer's composite signal. The amplitude of the sum frequency corresponds exactly to the input signal level at a frequency determined by the difference between the center frequency of the narrow-band filter and the frequency of the VCO.

The 2920's absolute-magnitude algorithm performs in effect a full-wave rectification of the narrow-band filter's output. Finally, the signal is lowpass-filtered to drive the vertical display. Since both horizontal and vertical display outputs of the 2920 are delivered as sampled-and-held signals, some simple external filters may be used to smooth the display.

The filters used in the spectrum analyzer are single-pole or complex-conjugate-pole recursive sections. Multiple pole filters are simply cascades of basic sections. The 2920 can also simulate finite impulse-response filters, and can implement zeros either independently or between pole sections.

The analyzer has a frequency range of 300 Hz to 3 kilohertz, swept 10 times per second, with a resolution of about 100 Hz. The narrowband filter is centered at 4.5 kHz. The sampling rate is about 13 kHz.

Room to spare

The table shows the amount of program and scratch-pad memory allocated to each block for the given parameters. (Different parameters for the functional blocks in the analyzer might change the amount of 2920 memory used in each, however.)

Since the program does not occupy all the RAM and E-PROM available, more functions could be added or, alternatively, the sampling rate could be raised to as high as 20 kHz. As another option, multiple copies of input sampling and filtering algorithms could be inserted to increase the effective sampling rate, thereby allowing use of a simpler anti-aliasing filter external to the 2920 signal processor's front end.

The 2920 is scheduled for production in the latter part of this year. Since the chip is a microprocessor and then some, it must be supported at least as adequately as current digital microprocessors. Support plans call for an assembler and simulator that will be resident on the Intellec microcomputer development system.

Because the arithmetic associated with the design and optimization of digital filters is extremely complex, a design-aid software package capable of interactive filter design and automatic compilation into 2920 assembly language is also planned. Those packages will equip analog system designers with all the conveniences users of conventional microprocessors are by now accustomed to enjoy. □

Oxide isolation builds a better Schottky TTL

Three-stage low-capacitance circuit blends low power consumption with fast operation

by Bob Bechdolt, Dave Ferris, and Paul Griffith, *Fairchild Camera and Instrument Corp., Mountain View, Calif.*

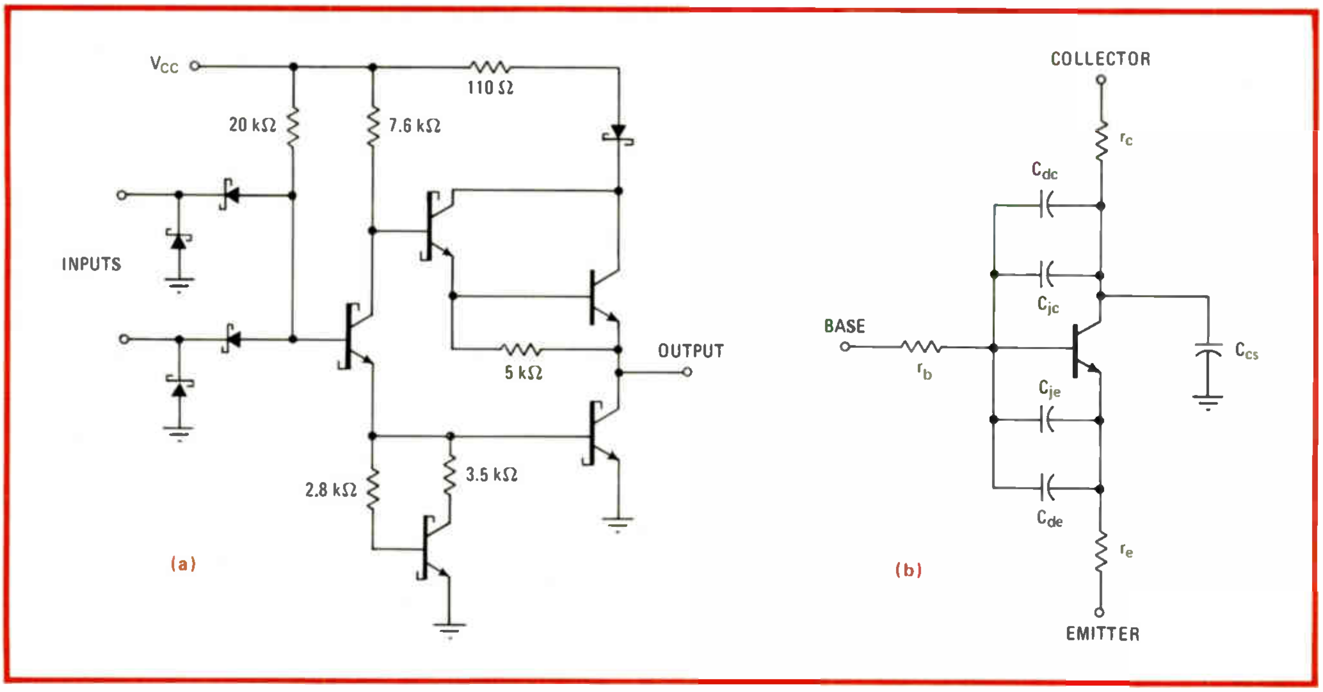
☐ In the bipolar logic derby, two Schottky transistor-transistor-logic families are the current favorites. The low-power version outruns conventional TTL with a lower power-delay product, but is not fast enough for some circuits. Standard Schottky components reign in these faster applications, but circuit density is handicapped by power consumption. Intended to supplant both, Fairchild's Advanced Schottky TTL (FAST) process technology yields parts that operate faster than standard Schottky and use just one fourth the power, making more complex designs possible.

The first 9 FAST parts are pin and functional equivalents of standard Schottky AND, NAND, OR, and NOR gates. The next 10 parts will be the data selector/multiplexers 74S151, -152, -157, and -158 and their three-state versions, 74S251, -252, -257, and -258. The remaining two chips will be the dual four-input multiplexer 74S352 and its three-state version, 74S353.

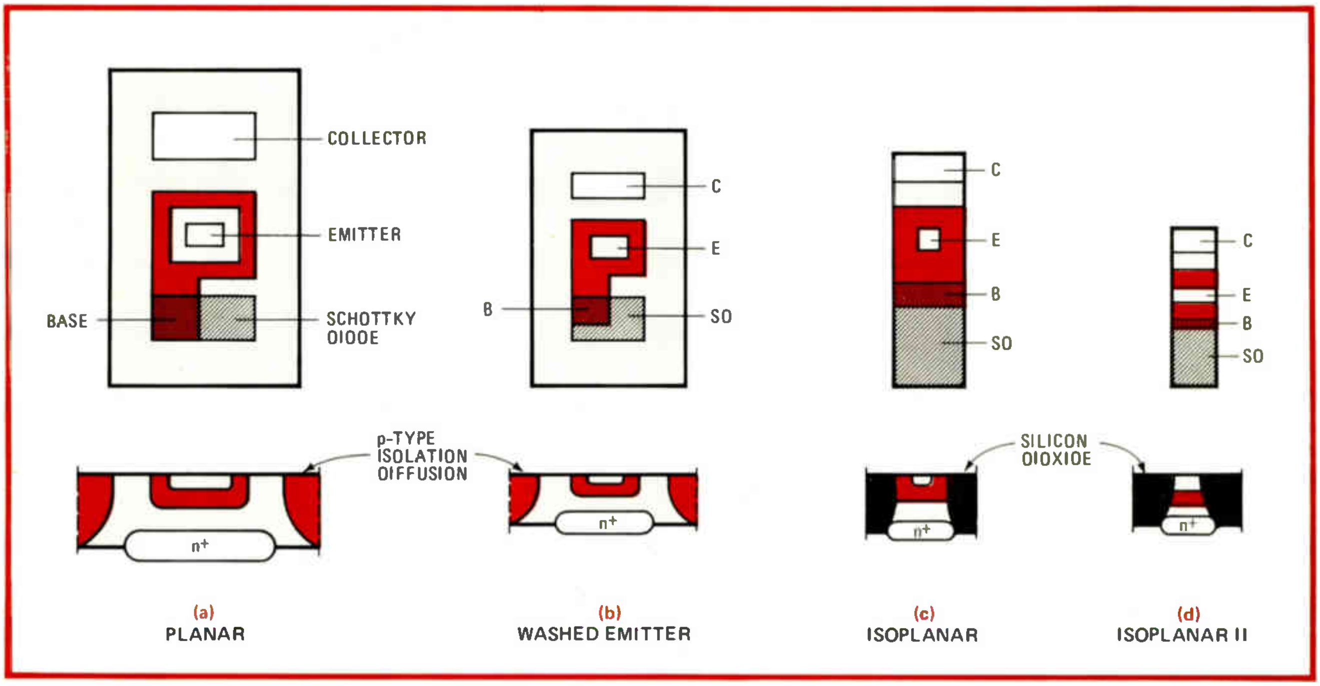
Designing a high-speed, low-power TTL family of this kind begins with a thorough analysis of the limiting factors of conventional circuits. This can be done by examining the impact of each transistor in a design. Figure 1a shows how a typical two-input NAND gate is currently realized with low-power Schottky-TTL technology. Total delay in such a circuit can be expressed in terms of charge-control effects, which describe the behavior of a transistor in terms of charge distribution, and space-charge capacitance.

Types of capacitance

Fixed charge and mobile charge each produce a specific type of capacitance. Ionized donor and acceptor impurities near the pn junctions create a stationary charge that results in space-charge-layer or junction capacitance. Figure 1b shows the equivalent circuit of a transistor when these parasitic effects are taken into consideration. The space-charge-layer capacitances of the base-collector and base-emitter junctions, C_{jc} and C_{je}, are directly proportional to the junction areas. The collector-substrate junction has a space-charge-layer



1. Parasitics. Shown in (a) is how a two-input NAND gate would be built with conventional low-power Schottky-TTL. The delay through such a circuit is due to the parasitic capacitance in the diode and transistor junctions. Shown in (b) is how the parasitic effects look schematically.



2. Going, going . . . Isoplanar technology (c) replaces the p-type isolation diffusion in conventional planar processes (a and b) with an oxide sidewall. In the isoplanar II process (d), the emitter terminates at the oxide wall of the isolation, greatly reducing size and parasitic effects.

capacitance, C_{cs}, proportional to the transistor's collector area. Because these junction capacitances are proportional to area, they are diminished when physical geometries are scaled down.

The diffusion capacitance, C_{de}, arises from the mobile minority carriers associated with forward current in the neutral base and emitter regions and the space-charge layers. It is proportional to both the forward transistor current and the forward transit time, τ_F, which is inversely related to the current gain-bandwidth product, f_T, of the transistor. The higher the f_T, the lower the forward transit time. Thus, C_{de} is low at low currents and is less significant on transistors having a high f_T.

Another parasitic effect

The mobile minority carriers associated with reverse current in the neutral base and collector regions and the space-charge layers generate the diffusion capacitance C_{dc}. It is proportional to the reverse (not forward) current and reverse transit time of the transistor. By Schottky-clamping the transistor properly, this reverse current can be substantially reduced and C_{dc} will be negligible. The Schottky diode, however, adds another capacitance, C_{jd} (not shown in Fig. 1b). The model for a Schottky-clamped transistor is therefore different from that shown in Fig. 1b in that C_{dc} is eliminated and C_{jc} is replaced by $C_{jc} + C_{jd}$.

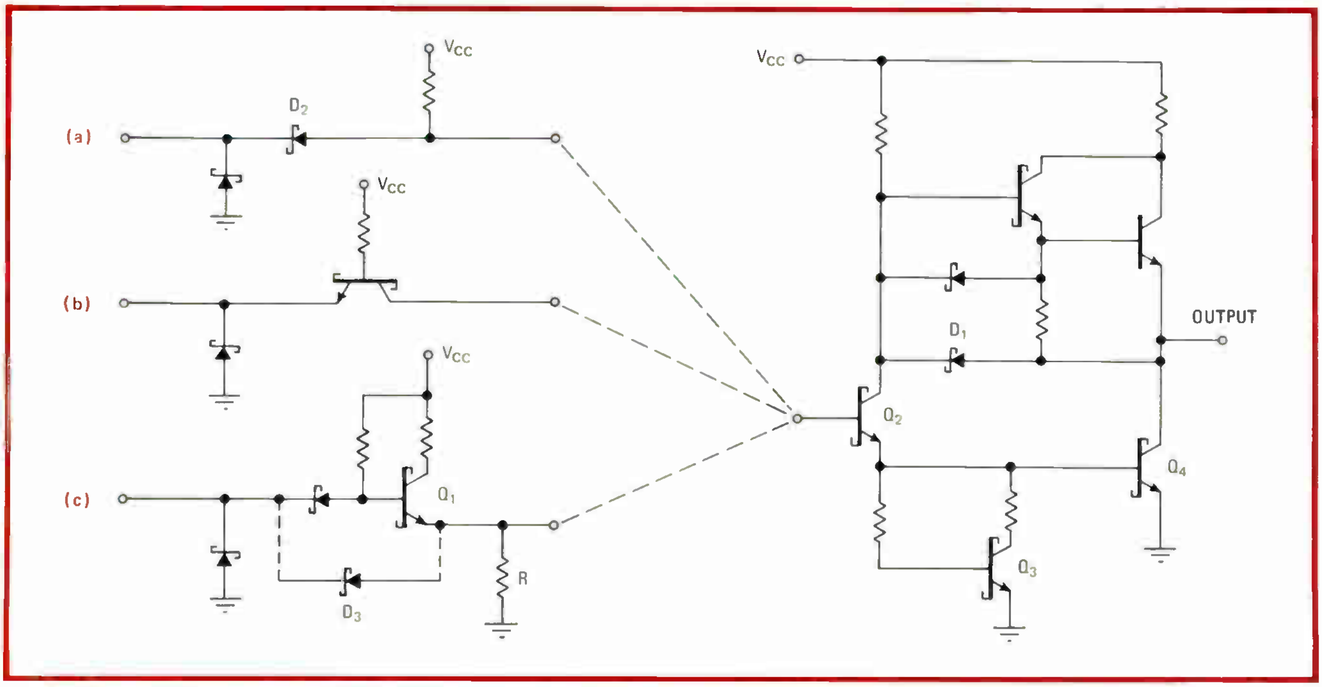
To turn on a Schottky-clamped transistor, the base-emitter junction must be forward-biased, requiring that the base current charge the capacitances C_{je} and C_{de}. As the transistor turns on, collector current flows and the collector voltage falls to its lowest or saturation value. The capacitances C_{jc}, C_{jd}, and C_{cs} are discharged through the transistor while this is happening.

Conversely, to turn off the transistor, the base voltage is reduced, creating a negative base current that flows out of the transistor and discharges C_{je} and C_{de}. As the transistor turns off, collector current stops flowing. Instead, the current supplied to the collector charges up the capacitances C_{jc}, C_{jd}, and C_{cs}.

The time required to charge a capacitor is proportional to the value of the capacitance and inversely proportional to the current charging it. One way to speed charging time is to increase the charging current. But the diffusion capacitance is directly proportional to the forward transistor current (which is all of the current in a Schottky-clamped transistor), so that the time required to charge the diffusion capacitance will be independent of the charging current and proportional only to the τ_F of the transistor. Consequently, adding more power to the circuit will help only until the time to charge the junction capacitance becomes small compared to the time required to charge the diffusion capacitance. Above this point, circuit delay is independent of power.

To decrease the delay at a given power level in the low-power region where the delay is inversely proportional to the charging current and proportional to the junction capacitance, the junction capacitance must be decreased. This implies a reduction of the area of the junctions, that is, devices with small geometries. In the high-power region the delay is proportional to τ_F and since τ_F is inversely proportional to f_T, transistors with very high f_T are desirable.

With the requirements for making high-speed TTL circuits established, namely small-geometry transistors with high current-gain–bandwidth products, the next step is determining how to best fabricate such devices. The planar process is a good starting point, since it is relatively simple and well-known. But it has one important disadvantage: planar devices are fairly large and cumbersome. The major problems in reducing the area of a planar transistor concern the lateral diffusion of the



3. Which input? Three basic circuit designs were examined to find the best. Circuits in (a) and (b) each use two stages of gain, while the circuit in (c) has a third stage, Q1. Each design has tradeoffs, but the three-stage type's high thresholds and noise immunity win out.

junctions and photolithographic misalignment.

Figure 2a shows the lateral geometry and cross section of a planar transistor. The minimum geometry is determined by several factors, including:

■ The smallest emitter-contact cut that can be defined with both mask- and wafer-production control.

■ The size of the emitter diffusion, which is determined by the amount of misalignment that can exist between the emitter contact and the emitter mask.

■ The size of the base, which must be large enough to contain the emitter and base contacts under worst-case misalignment.

■ The distance between the base contact and the emitter, which must be large enough to prevent contact should both be misaligned.

■ The minimum size of the n-type silicon "tub," which is determined by the side diffusion of both the p-type base and p-type isolation diffusions, as well as the possible misalignment of these two masks.

Only the area under the emitter in a planar transistor is active. All of the junction capacitances associated with the area outside the emitter are parasitic and they degrade the device's performance.

The conventional planar process is improved with the washed-emitter process (Fig. 2b). This exploits the emitter's side diffusion into the base and also uses the base oxide for junction passivation. As there is no need to leave any emitter oxide on the transistor after diffusion, the emitter is said to be washed free of oxide.

Misalignment between the emitter-contact cut and the edge of the emitter diffusion is eliminated, so the emitter can be as small as the smallest oxide cut that can be defined, and the parasitic area of the emitter outside of that cut is eliminated. Furthermore, the base region and the silicon tub can be reduced by the same amount as the emitter. Nevertheless, a significant amount of parasitic capacitance remains due to the areas of the base and the n-type silicon tub outside of the emitter contact. Although other improvements in photoprocessing can reduce the overall size of a planar transistor, a fundamental limit is reached: most of a planar transistor's capacitance is inherently due to parasitic effects.

Isoplanar speed

Isoplanar technology is a major departure from conventional planar processes in that it eliminates the p-type isolation diffusion and replaces it with an oxide sidewall. The lateral geometry and cross section of an Isoplanar transistor are shown in Fig. 2c. Since the oxide isolation is nonconductive, the base can overlap it without shorting to the p-type substrate, eliminating concerns about misalignment and side-diffusion between the isolation and the base. In effect, the base is self-aligning because, while the base mask may be made larger than the silicon tub, the base region itself is determined by the coinciding areas of the base mask and the silicon tub within the oxide isolation. A large reduction in the area outside of the base results, significantly reducing the collector capacitance of the device.

The greatest reduction in parasitic capacitance is achieved with the Isoplanar II process, whose structure is illustrated in Fig. 2d. The emitter terminates at the oxide wall of the isolation, reducing the parasitic base area outside of the emitter. Furthermore, since it is easier to print a long, narrow line on the masks and wafers than shorter lines of the same width, the emitter can be made smaller than on unwalled structures. The Isoplanar II process reduces collector area more than 70% when compared to the conventional and washed-emitter planar devices and more than 40% when compared to an Isoplanar transistor. Even more important for the high-speed performance of these transistors, the base-collector

TABLE 1: AC PERFORMANCE OF EXTERNAL NAND GATES

Capacitive load	Parameter	2-mW-per-gate test circuit	20-mW-per-gate test circuit
15 pF	Rise time (ns)	3.5	2.3
	Fall time (ns)	3.5	2.4
50 pF	Rise time (ns)	5.1	3.2
	Fall time (ns)	4.9	3.4

TABLE 2: BUFFERED INTERNAL-GATE RING-COUNTER DATA

Ring counter	Average power (mW)	Average propagation delay (ns)	Delay-power product (pJ)
A	1.6	3.05	4.88
B	2.4	2.19	5.26
C	4.2	1.70	7.14
D	7.7	1.59	12.24

capacitance of an Isoplanar II device is reduced by 60% compared to its planar and Isoplanar counterparts.

By combining these dramatic area reductions with the use of shallower junctions and enhanced processing, transistors having an f_T as high as 5 gigahertz have been fabricated. Such high f_T values and small geometries assure gates with faster operation at all power levels. Finally, experience gained in manufacturing the F100K emitter-coupled-logic family and recent innovations in electron-beam mask making and projection printing make the Isoplanar II technology especially suitable for high-volume manufacturing.

Two or three stages?

Next, attention was turned to selecting a circuit configuration that would both take full advantage of the improved characteristics of Isoplanar II technology and be fully compatible with other TTL circuits. Such a circuit should possess the lowest possible propagation delays at a reasonable power level. Voltage thresholds should be well within the specified limits for low- and high-level inputs (0.8 V and 2.0 V). An ideal design would also be able to drive highly capacitive loads.

Two basic circuit designs with two and three stages of gain were examined. The two-stage configuration has been commonly used for standard and low-power–Schottky TTL circuits. Two such types are shown in Fig. 3a and b; one uses a transistor on the input, the other uses a Schottky diode.

The transistor exhibits a higher dc-input characteristic (about 1.3 V) than the diode input (about 1.0 V), since the collector-to-emitter voltage of a saturated transistor is typically only 0.2 V while the forward voltage drop across a Schottky diode is about 0.5 V. Thus a transistor input has fewer low-level threshold and noise problems.

But other considerations favor the diode input. For one thing, a diode usually responds faster when the input changes because the junction capacitance of a diode helps transfer charge into or out of the base of the first-stage transistor, thus minimizing delay through the circuit. No such coupling occurs with the transistor input. Also, the capacitance of an input transistor's collector-substrate junction appears at the base of the first-stage transistor, slowing its response.

Another drawback of the transistor input is that it normally exhibits greater leakage current for high input voltages. Although Schottky-clamping the transistor helps, it also adds capacitance at the base of the first-stage transistor. Finally, a transistor input generally suffers from having a lower input breakdown voltage.

A typical three-stage circuit, shown in Fig. 3c, has one more gain stage (Q_1) than a two-stage circuit and a pn input diode rather than a Schottky diode. The additional stage of gain raises the dc-input threshold to about 1.5 V, considerably higher than that of the two-stage circuits. This increases the threshold margin above the required value (0.8 V for Schottky, 0.7 V for low-power Schottky), especially at high temperatures, and improves the low-level noise immunity. The two-stage circuit with a diode input requires a physically large diode to meet this specified minimum threshold. But the large junction capacitance associated with this diode further degrades the dynamic noise immunity, and the propagation delay of a multiple-input circuit. With a three-stage circuit, the threshold is high enough for a small diode to be used, improving noise immunity.

Both the two- and three-stage circuits have a diode, D_1, connected from the output to the collector of the phase-splitter transistor, Q_2. This minimizes delay when large capacitive loads are used. When the output goes from high to low, charge is coupled from the load capacitance through Q_2 into the base of the output transistor Q_4, thus helping to saturate Q_4.

Another tradeoff

The additional stage of gain in the three-stage circuit generally results in quicker high-to-low transitions. A lower amount of Q_1 base current saturates this transistor, causing Q_2 to turn on faster than in a two-stage circuit. This is particularly important for multiple-input NAND circuits, where the input is more capacitively loaded with the additional inputs.

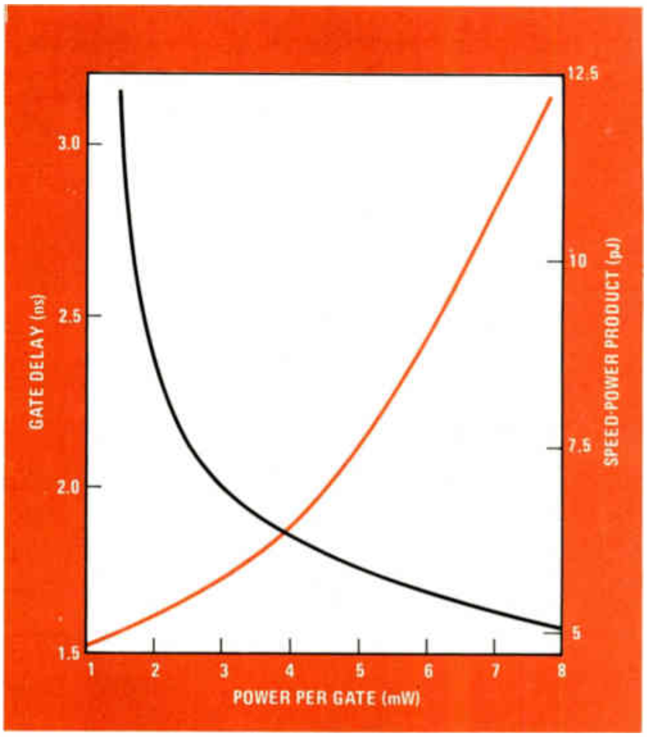
On the other hand, the three-stage circuit generally has a slower low-to-high transition. The base-discharge resistance, R, has a much higher impedance than input diode D_2 in the two-stage circuit, causing a slower discharge of Q_2. In AND, NAND, and inverting circuits, connecting a Schottky diode, D_3, from the base of Q_2 to the input, will provide a low impedance path to ground. Unfortunately, this solution cannot be used for OR and NOR gates. This disadvantage is partly offset by performing the OR function with Q_1, rather than at the phase splitter Q_2. The collector-substrate capacitances of the additional paralleled transistors needed to form an OR circuit will thus be added at a noncritical node (rather than at the collector of the phase splitter), and no degradation of the output rise time will occur.

Analysis has shown that two- and three-stage circuits have similar average gate delays. The three-stage circuit uses slightly more power because power is dissipated in resistor R, raising the speed-power product slightly. But its high noise immunity and high thresholds far outweigh this small disadvantage, so this configuration was chosen for high-speed TTL.

To measure the performance of the family, several evaluation circuits were designed using two-input NAND gates with three stages of gain having standard- and low-power-Schottky power levels. The dc characteristics were compatible with current standard and low-power-Schottky devices except that the low-power-Schottky evaluation circuits exhibited a 1.5-V typical threshold and the output short-circuit current, I_{OS}, was increased over standard and low-power Schottky levels to achieve better high-capacitive-drive capabilities. The ac performance is shown in Table 1.

Medium-scale integrated-type structures were also evaluated. Standard and low-power T-type flip-flops and ring counters were made having low-power Schottky thresholds and buffered outputs. The T flip-flops were tested with an 8-picofarad load capacitance using unbuffered clocks. Maximum toggle frequency, f_{max}, was measured for both circuit types. The results indicated a speed of 172 MHz for the low-power devices and 270 MHz for the standard ones.

The gates used to construct the ring counters were very similar to the one shown in Fig. 1 except that the Darlington transistor's collector was connected directly to V_{CC} and no clamping diodes were used. This is a conservative design and represents a configuration that might be used as a clock buffer to drive several flip-flops, an output-control gate for a three-state device, or as an



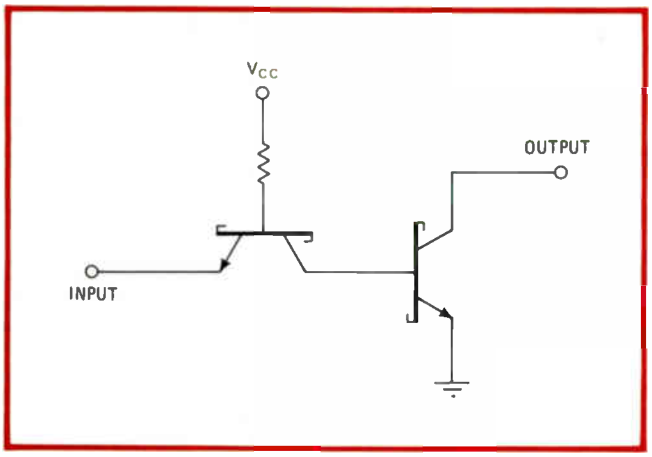
4. Best power. These curves illustrate that below 4 mW, the delay through a FAST gate shrinks rapidly as the power level rises. Above this power level, however, the delay-power product increases rapidly. A 4-mW gate dissipation therefore offers the best tradeoff.

TABLE 3: DC CHARACTERISTICS OF SCHOTTKY FAMILIES

Parameter		Schottky	Low-power Schottky	FAST
Input high voltage, V_{IH} (minimum)		2.0 V	2.0 V	2.0 V
Input low voltage, V_{IL} (maximum)		0.8 V	0.7 to 0.8 V	0.8 V
Input clamp-diode voltage, V_{CD} (maximum)		−1.2 V	−1.5 V	−1.2 V
Output high voltage, V_{OH} (minimum)	commercial	2.7 V	2.7 V	2.7 V
	military	2.5 V	2.5 V	2.5 V
	I_{OH}	−1 mA	−0.4 mA	−1 mA
Output low voltage, V_{OL} (maximum)	commercial	0.5 V (I_{OL} = 20 mA)	0.5 V (I_{OL} = 8 mA)	0.5 V (I_{OL} = 20 mA)
	military		0.4 V (I_{OL} = 4 mA)	
Input high current, I_{IH} (maximum)	at 2.7 V	50 μA/input	20 μA/input	20 μA/input
	at maximum input voltage	1 mA at 5.5 V	100 μA at 10 V	100 μA at 7 V
Input low current, I_{IL} (maximum)		−2 mA	−0.4 mA	−0.6 mA
Output short-circuit current, I_{OS}	(maximum)	−100 mA	−100 mA	−150 mA
	(minimum)	−40 mA	−20 mA	−40 mA

TABLE 4: PROPAGATION DELAYS OF FAIRCHILD'S SCHOTTKY FAMILIES

Family		Standard Schottky			Low-power Schottky			FAST		
Capacitive load	Device / Delay (ns)	Rise time	Fall time	Average	Rise time	Fall time	Average	Rise time	Fall time	Average
15 pF	Two-input NAND gate	3.3	3.8	3.55	5.3	5.7	5.5	3.1	2.4	2.75
	Two-input AND gate	4.5	5.0	4.75	8.0	7.8	7.0	3.9	3.5	3.7
50 pF	Two-input NAND gate	4.7	6.0	5.35	8.0	9.0	8.5	4.4	3.6	4.0
	Two-input AND gate	6.0	7.0	6.5	10.0	11.0	10.5	5.5	4.7	5.1



5. Beyond FAST. Measurements have indicated that gates like this one, which are simpler in design and internally unbuffered, exhibit delays which are less than a nanosecond. With such gates, circuits can be constructed to operate faster than 200 megahertz.

internal gate with a large fanout. Four power levels were evaluated, as shown in Table 2, and the results were used to construct the delay versus power and the delay-power product versus power curves shown in Fig. 4.

These curves indicate that below 4 mW, the delay decreases substantially as the power is increased. Above 4 mW, the delay decreases very little, causing the delay-power product to increase rapidly. Thus a 4-mW gate is the best tradeoff between delay and power.

A new family

Fairchild Advanced Schottky TTL (FAST) was developed on the basis of the analyses of an optimum technology and circuit configuration for a high-speed, low-power TTL family. FAST operates up to 75% faster than low-power Schottky while limiting power consumption to one quarter that of standard Schottky.

While dc characteristics of the FAST family standard Schottky are very alike, there are some important differences (Table 3). The maximum specified input-high current I_{IH} is 20 μA compared to 50 μA for Schottky, and the input-low current I_{IL} is 0.6 mA compared to 2 mA for Schottky. Coupled with the fact that the output-high and -low currents, I_{OH} and I_{OL}, are the same as Schottky, this results in a tripling of fanout capability.

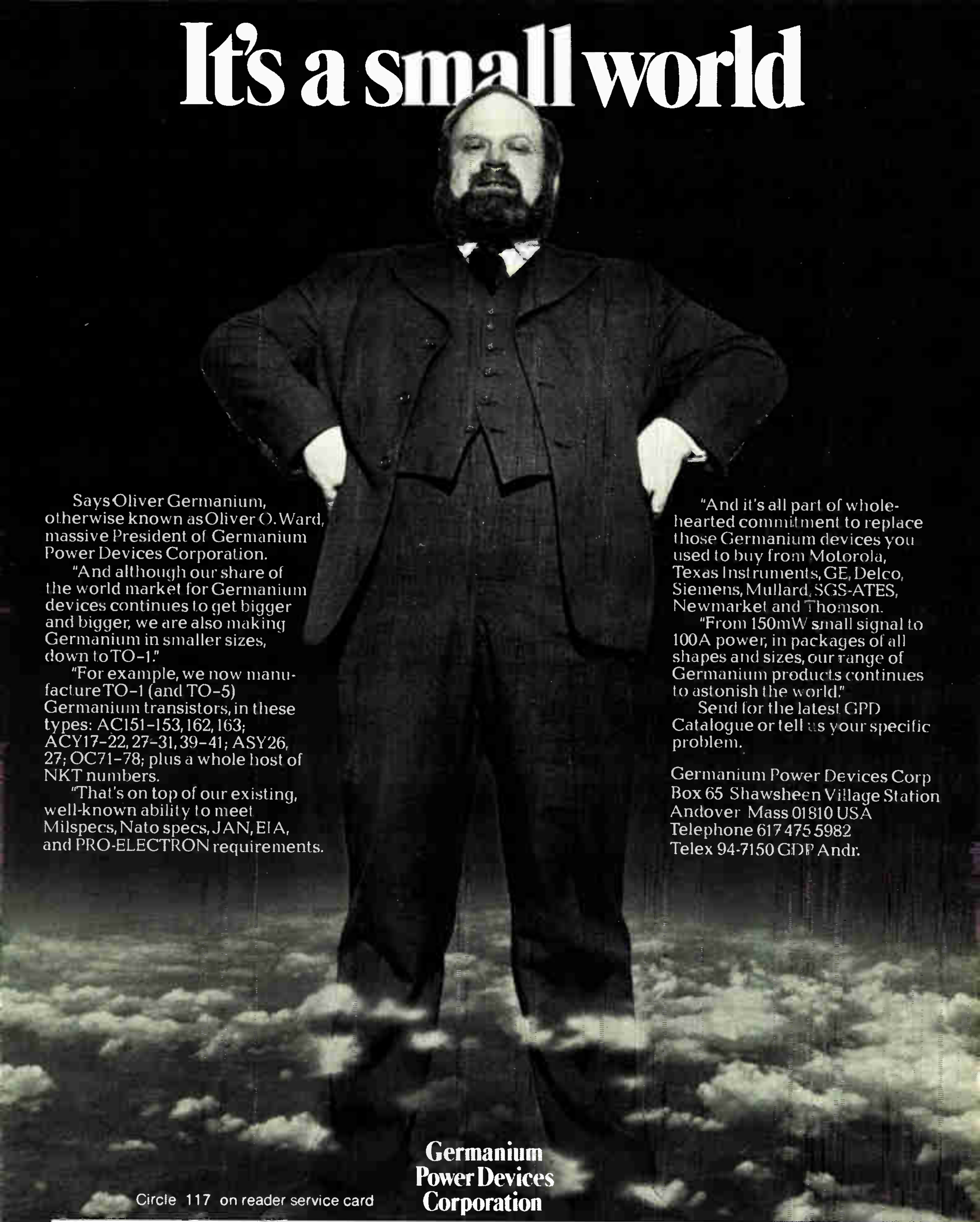
The maximum input current of a FAST device is lower, 100 μA at 7 V compared to 1 mA at 5.5 V for Schottky, because diode rather than transistor inputs are used. Consequently, unused inputs may be tied to the supply voltage to simulate a logic 1. The maximum short-circuit current is 150 mA for FAST, a value in between standard Schottky (100 mA) and the evaluation circuits (200 mA). Improved capacitive-load driving results, while the problem of fast-edge rates that might cause ringing is minimized. Because the three-stage circuit configuration was chosen, the guaranteed low-level input voltage, V_{IL} at a value of 0.8 V is easily met over the military operating range.

Typical ac characteristics of the FAST family are shown in Table 4, along with those of standard and low-power Schottky, for output loads of 15 and 50 pF.

Shorter delays

FAST devices have shorter gate delays than both low-power and standard Schottky. With 15-pF loads, the new family has average single inversion delays that are 800 ps (23%) faster than Schottky, and double inversion delays that are 1.1 ns (23%) faster. The 50-pF load results are even more impressive. Single inversion delays are 1.4 ns (26%) faster than Schottky, and double inversion delays are 1.4 ns (22%) faster. This illustrates FAST's improved line-driving capabilities.

The speed advantage of the FAST family is ideal for MSI and LSI circuits. Average delay for a buffered 4-mW internal gate, such as that used for the ring counters described earlier, is 1.7 ns. Measurements have shown that simpler, unbuffered internal gates, such as that shown in Fig. 5, have subnanosecond delays. Based on the results of T flip-flops for low and standard Schottky power levels, typical operating frequencies for flip-flops are well in excess of 200 MHz. □



C-MOS oscillator has 50% duty cycle

by Bill Olschewski
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Astable multivibrators built with complementary-metal-oxide-semiconductor gates suffer one major drawback—their duty cycle may vary from 25% to 75% because of the variations of each gate's switching-threshold voltage (V_{TH}). Variations in the V_{TH} can be canceled and the desired square-wave output therefore attained by adding a C-MOS inverter and three resistors to the basic circuit. The gate-resistor combination uses negative feedback to perform the compensation.

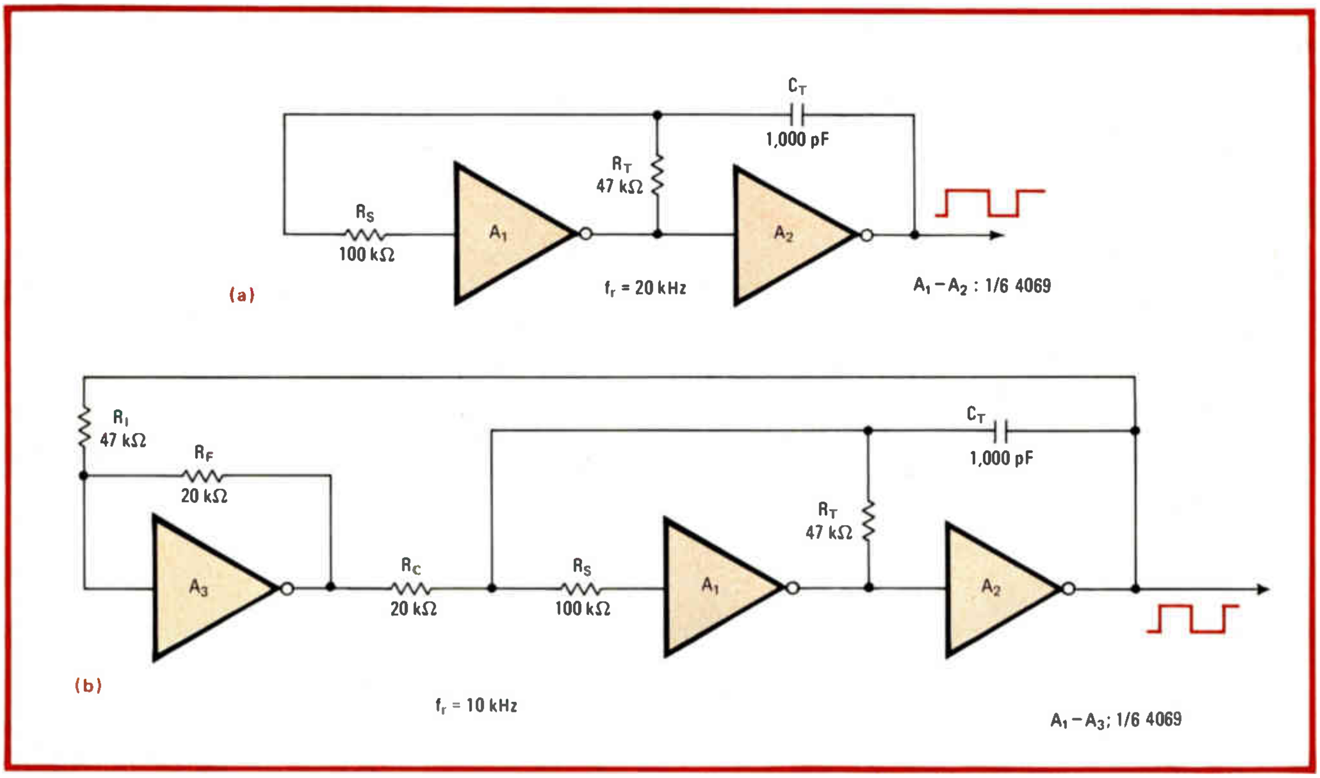
The standard astable multivibrator is shown in (a) of the figure. Running at a frequency ($f = ½R_TC_T$) that is almost independent of the individual gate used, the circuit nevertheless has an unpredictable duty cycle because of a V_{TH} that can vary by up to 40% on either side of $V_{DD}/2$, where V_{DD} is the supply voltage. If a 50% duty cycle is required, either this circuit must be followed by an edge-triggered flip-flop, or each circuit must be individually adjusted using two trimpots and a diode (see RCA application note ICAN-6267).

The circuit in (b) eliminates these drawbacks. Inverter A_3 creates a second negative-feedback path around A_1 (the signal flow through R_T constitutes the prime path). A_3 is operated at a low closed-loop gain, much like an operational amplifier working in the linear portion of its characteristic. As a result, A_3's inverted threshold voltage can be combined with the negative feedback voltage and injected into A_1. If the ratio R_F/R_I equals the ratio R_C/R_T, complete cancellation of threshold errors between A_1 and A_3 can be obtained. It is assumed that A_1 and A_3 are contained in the same package along with A_2 and that their V_{TH}s are essentially equal.

Since A_3's gain must be set so that its output will not saturate with a ±40% variation of V_{TH}, resistor values must be selected so that $R_I/R_F = 2.33$. At the same time, the correct gain for A_3 is set when $R_CR_I = R_FR_T$. In these circumstances, and ignoring stray and input capacitances, the multivibrator's operating frequency will be $f = 1/R_TC_T$ and the duty cycle will be 50%.

Note that the operating frequency, in this case 20 kHz, is twice that of the standard astable circuit using the same values of C_T, R_T, and R_S because of the second feedback path. □

Designer's casebook is a regular feature in Electronics. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.



Right on. Standard astable multivibrator using C-MOS gates (a) has unpredictable duty cycle because of variable switching-threshold voltages. Adding inverter and three resistors (b) creates second negative feedback path around A_1, forcing A_1 and A_2's switching point to half the supply voltage, so that 50% duty cycle is attained and square waves are produced.

Epitaxial phototransistor with feedback has fast response

by Vernon P. O'Neil
Motorola Inc., Discrete Semiconductor Division, Phoenix, Ariz.

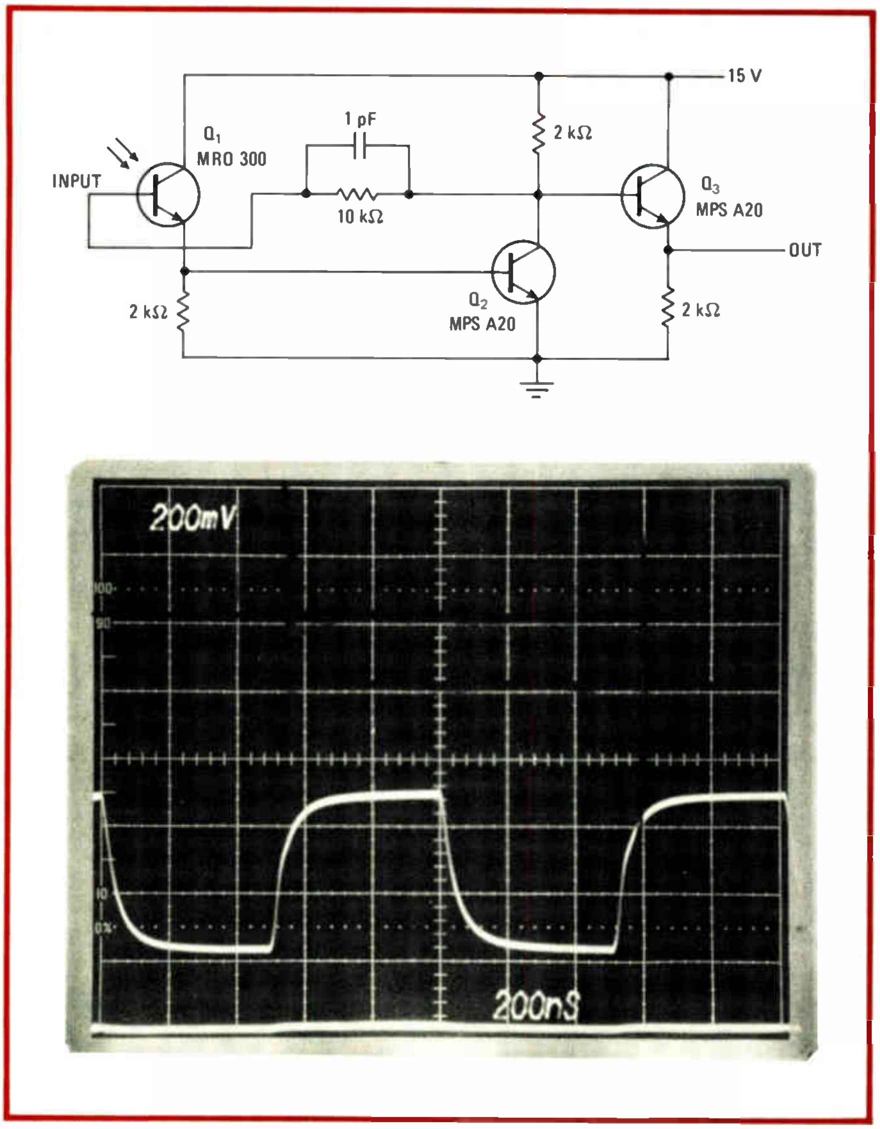
A high-gain negative-feedback loop will reduce the response time of an epitaxial phototransistor to 100 nanoseconds—a significant improvement over several schemes previously suggested.[1,2,3] Because of its construction, the epitaxial device all but eliminates the diffusion of carriers into its depletion region from the bulk collector region, which slows a conventional non-epitaxial phototransistor's operating speed. And added feedback reduces the input-signal swing across the collector-base junction to 1% of what it is normally, further reducing the input-capacitance charge and discharge times.

The MRD 300 phototransistor shown in the circuit has a typical rise time of 2.5 microseconds and a fall time of 4 μs if operated in the conventional emitter-follower configuration. In this modified circuit Q_2 serves as the feedback amplifier that keeps the base of the phototransistor at an almost constant voltage for changes in input-signal level. Thus the effective input capacitance that must be charged and discharged is reduced. Q_3 serves as a buffer. Note that using feedback that is negative enables the switching times to be maximally reduced without fear of creating instability (that is, oscillations can be generated with circuits using positive feedback).

With this circuit, both the rise time and the fall time of the phototransistor are reduced to 100 ns. The output voltage is equal to the product of feedback resistance (10 kilohms) and the collector-base photocurrent. The photograph shows a typical output waveform.

As for the phototransistor itself, it can be hard to determine from data sheets if one is epitaxial or not. The best way to find out is to consult the manufacturer. □

References
1. "Why not a cascode optocoupler?", Electronics, March 2, 1978, p. 132.
2. "Why not a cascode optocoupler? Here's why not", Electronics, April 27, 1978, p. 154.
3. "Bootstrapping a phototransistor improves its pulse response", Electronics, Aug. 17, 1978, p. 105.



Speedy. Collector-to-base capacitance of phototransistor Q_1 is reduced by employing epitaxial device (MRD 300) and high-gain negative feedback (Q_2), so that operating speed can be increased. Emitter-follower Q_3 provides low-impedance output. Photograph shows typical output response.

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Hybrid servo system minimizes hunting

by C. V. Rajaraman
ISRO, Trivandrum, India

Although the shunt comparator circuit of Vojnovic[1] is simple and tends to reduce the overshoot and hunting problems inherent in a high-speed digital servo system, difficulties may arise when the servomechanism is continually called upon to follow small changes in position. Digital subtraction circuits, on the other hand, will increase system stability but are more expensive and very complex. But the two most popular techniques for synthesizing the control circuit—the no-shunt comparator method and the aforementioned subtractor method—can be combined to form a hybrid system that is more accurate than the first and less complex and costly than the second.

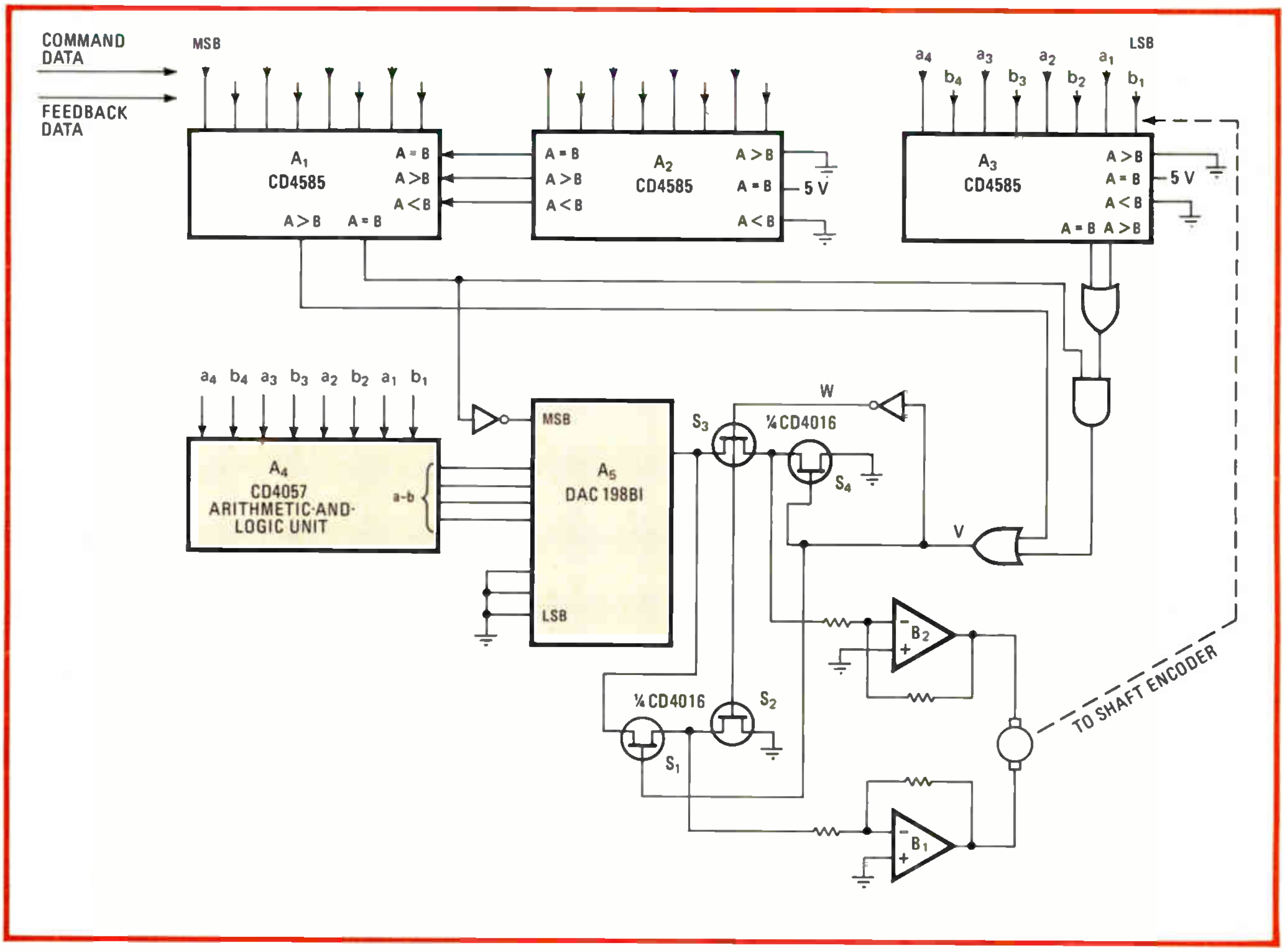
As shown in the figure, A_1 and A_2 compare lines 5–12 (the coarse bits) of a 12-bit command input with their feedback-data counterparts, which are derived from the motor position by a shaft encoder. Comparing the coarse bits in this manner enables the system to converge quickly on the desired position.

At the same time, the low-order (fine) bits of the command word are compared by A_3, and A_4 is programmed to find a~b, the difference between the two 4-bit binary words. The a~b result is then transformed into an equivalent analog signal by the digital-to-analog converter, A_5. Using the d-a converter allows a precise voltage to be applied to the motor, instead of the constant-magnitude (logic 1) signal that a comparator-type circuit would generate whenever there was an a~b offset of any value. Thus the motor has little tendency to overshoot its intended mark.

As for transferring the voltage from the converter to the motor, V moves high either when the coarse-bit comparison yields A = B and the state between the fine bits are such that A = B or A > B, or when just the coarse-bit comparison yields A > B.

Under these conditions, S_1 and S_4 turn on, and operational amplifier B_1 moves high to drive the motor. Under any other bit-comparison condition, W moves high and turns on S_2, S_3, and B_2, to drive the motor in the other direction. □

References
1. B. Vojnovic, "Shunt comparator stabilizes high-speed digital servo," Electronics, March 16, 1978, p. 149.



End of search. Comparators and subtractor in servo position motor without oscillations. Comparison of high-order bits enables motor to converge on desired location. Fine-bit comparison with a d-a converter resolves precise feedback voltages to minimize overshooting.

Designing a serviceman's needs into microprocessor-based systems

Mapping tells him where to start; signature analysis locates circuit nodes in trouble; diagnostics check operation

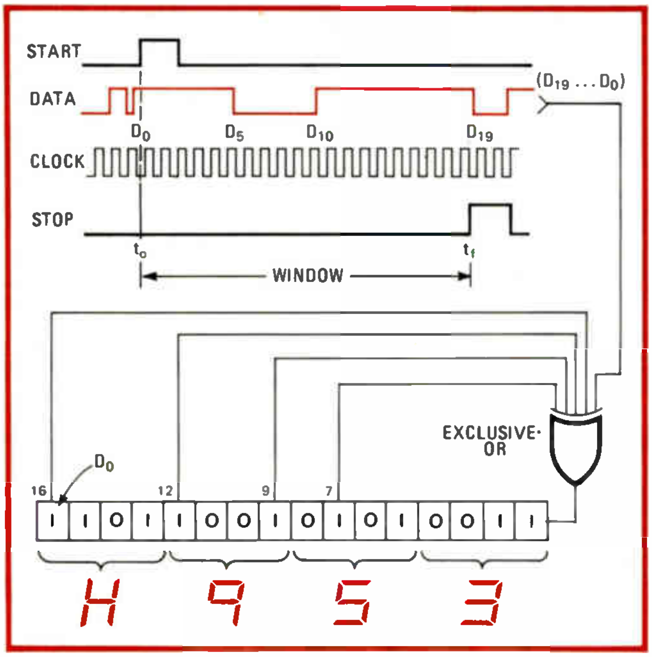
by Martin Neil and Randy Goodner, *Hewlett-Packard Co., Santa Clara Division, Santa Clara, Calif.*

☐ Mention the word "microprocessor" to a serviceman, and watch his face cloud over. He knows that the many advantages the chips offer to both manufacturer and user are coupled with new problems and challenges from his point of view.

There is a way to ease his job, and it is the familiar tack of designing serviceability into the product. However, many designers are unfamiliar with the special servicing requirements of microprocessor-based products.

Troubleshooting woes

Several characteristics associated with such designs present troubleshooting problems for traditional test equipment. One of these is that characterization of the circuitry is difficult because processor firmware often replaces hardware and its operation may be hidden in the software algorithm. A related problem is the dynamic operation of these products, where signals often are active for a few microseconds and then disappear. In a microprocessor-controlled keyboard, for example, checking for signal faults requires knowing when to look as well as where to look.



1. Signature analyzed. This 4-place hexadecimal signature is a compression of the 20-bit data stream entering the linear-feedback shift register. The unique character set, consisting of 0 . . . 9, 4, C, F, P, and U, allows use of a seven-segment display.

A third problem is that the bidirectional nature of the processor bus makes interpretations of address and data information very difficult. Compounding this is the buses's parallel structure, which has many devices ORed together, making for tedious fault detection. Furthermore, the test gear must contend with many operations, since newer instruments may have the processor going through a few thousand steps in a measurement cycle where earlier products usually required fewer than 100 operations.

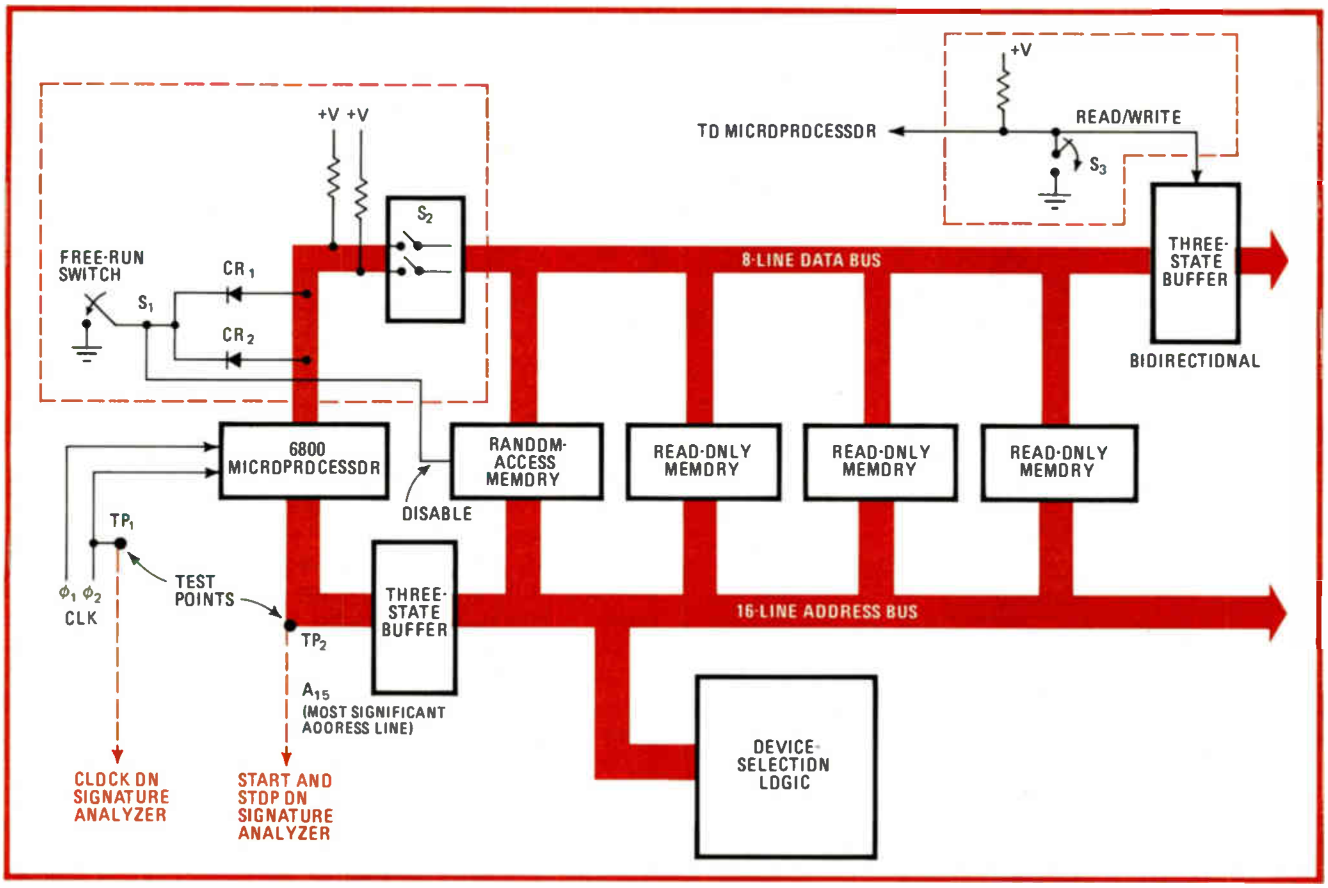
A partial solution to these problems is logic-state analyzers, which help trace the microprocessor's operating algorithm by following the sequence of machine states. Once the state in which the fault first appears is located, traditional test equipment comes into play in order to trace through the nested circuits seeking the component or components giving rise to the fault. However, this procedure can take much time and invariably requires a highly skilled serviceman.

Failures involving the microprocessor assembly and those assemblies that interface to the processor are extremely difficult to troubleshoot. In fact, it may be impossible to isolate these failures with traditional troubleshooting equipment and techniques. Hours of investigation may not determine whether the fault is a control failure originating in the microprocessor assembly, an interface failure, or a failure in some other assembly causing the measurement algorithms to hang up or branch to an incorrect program segment.

To chase the clouds away from the serviceman's face, the designers of microprocessor-based products must take a new look at designing in serviceability. They should look closely at three techniques that can overcome these troubleshooting problems: signature analysis, built-in diagnostics, and mapping. What follows is a discussion of these three, coupled with examples of how specific designs help the serviceman.

Signature analysis

Perhaps the greatest serviceability boon a designer can offer to the product's user is the capability to work with such troubleshooting tools as the HP 5004A signature analyzer. A relatively new technique, signature analysis



2. Open the loop. To implement free-running signature analysis, it is necessary to open the microprocessor assembly's feedback loop to prevent alterations to the free-run instruction. This can be done on the board itself by simply adding a few components.

uses data compression to reduce complex, serial data-stream patterns of any length at a circuit node to a unique four-digit hexadecimal signature [*Electronics*, March 3, 1977, p. 89].

Comparing the signature of a suspect circuit node with the empirically determined correct signature in the service manual will quickly verify circuit operation. The cause of an incorrect signature may be quickly discovered by probing designated nodes, observing good and bad signatures, and tracing the signal flow.

Besides the data from the circuit node, the 5004A needs three signals. A start signal initiates the measurement window during which data is clocked into a 16-bit linear-feedback shift register in the analyzer. A clock signal generated by the unit under test synchronizes the data with the signal analyzer. A stop signal terminates the measurement window, and the 16-bit residue in the shift register appears on the display as a 4-place hexadecimal signature (Fig. 1).

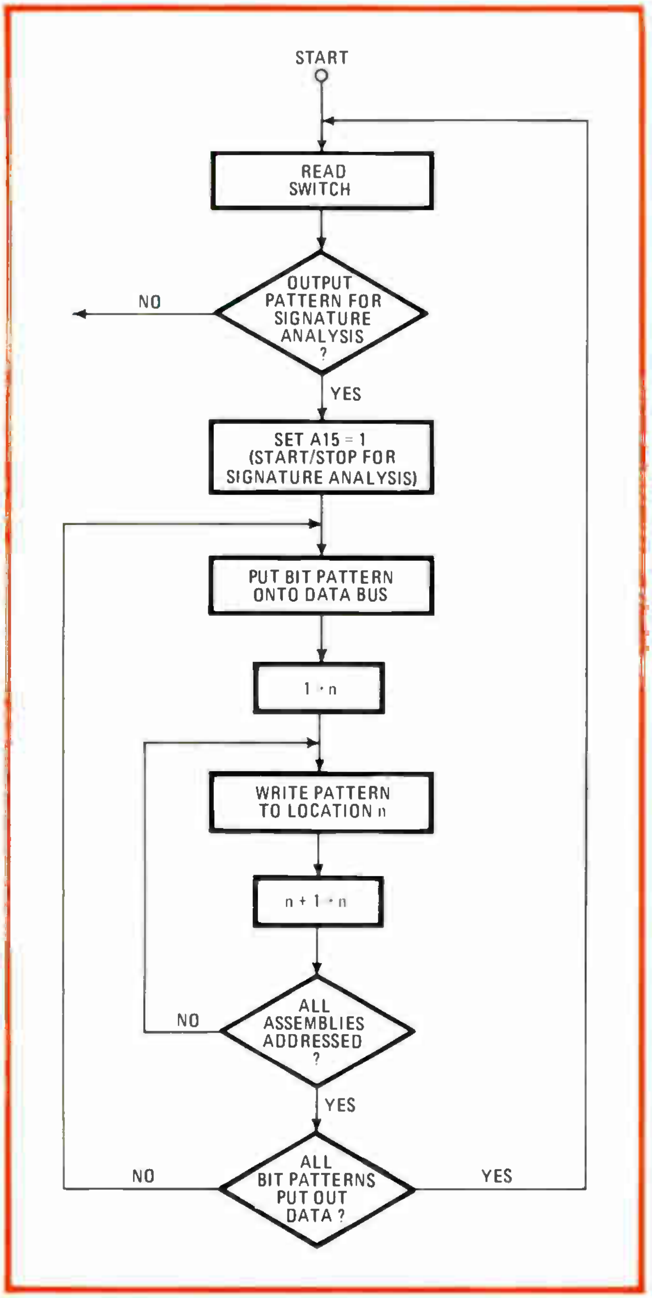
The free-running and software-driven modes are the two basic implementations of signature analysis in a microprocessor-based product. Free-running analysis forces the processor to cycle continuously through its entire address field with start/stop signals derived from the lines of its address bus. Software-drive analysis uses a stimulus program stored in read-only memory to generate the start/stop signals and to write repeatable data streams onto the data bus in order to test assemblies connected to the processor.

The free-running mode occupies no ROM space, while the software-driven mode typically requires something under 5% of this space. However, the software mode can exercise more of the product's circuitry. For thorough testing, both techniques may be implemented in the same product.

The HP 5342A microwave frequency counter is an example of efficient implementation of free-run signature analysis: only a few switches and pullup resistors need be added to the processor assembly. The outlined area in Fig. 2 shows the few components added.

Essentially, what free-run analysis checks is the operation of the kernel: the minimum configuration of microprocessor, ROM, and random-access memory needed to cycle through the entire address field. Grounding the free-run switch, S_1 in Fig. 2, and opening the data-bus switch, S_2, forces the processor into the free-run mode.

Grounding S_1 generates an instruction to clear accumulator B, incrementing the program counter by 1 and thus cycling the processor through its address field one step at a time. A NO OP instruction will perform the same function, but the CLR B instruction needs the minimum of added hardware: two diodes. Opening S_2 prevents incrementation of the program counter, while opening S_2 prevents the ROM output data from altering the free-run instruction. Consequently, the processor's address lines cycle repeatedly over the entire address field from 0000 to FFFF. Using the most significant address line (A_{15}) as start/stop signals and one phase of



3. Program-driven analysis. This program stored within a ROM generates the output patterns used to test the system in the program-driven signature-analysis mode. The most significant address bit A_{15} is set high to generate its start/stop signals.

the processor's clock as the clock signal will give repeatable, stable signatures for the address lines, ROM outputs and device-select outputs.

Switch S_3 enables the write buffer so that free-run signatures may be observed there. The read portion of the buffer cannot be checked with free-run analysis; it requires a logic pulser and logic probe.

Software-driven analysis

Exercising a special pattern stored in ROM will provide a more thorough signature analysis than will the free-run mode. This software-driven mode provides a pattern for the boards that are outside the kernel and therefore have no way of generating patterns. It allows troubleshooting of the input registers of devices accepting data from the microprocessor, and will often provide signatures for the circuitry responding to data in those registers.

A typical 8-bit output test pattern would start off with all 0s, go to all 1s, then continue with a walking 1 pattern (10000000, 01000000, . . . 00000001). The processor places the first byte of the pattern on the data bus and instructs a board to accept the byte in a specific location or register. For example, if the board has 12 locations, the processor will write the byte at all 12.

Once done, the processor sends the same byte to locations on the next board. After all locations on all boards have been loaded, the processor places the next byte on the data bus, and the process repeats.

One way to generate start/stop signals is setting the most significant address bit high at the beginning of the test program. With the test program in the lower half of the memory, the most significant address line, A_{15}, can be artificially toggeled at the beginning of the cycle simply by addressing a dummy location in the upper half of the memory. Figure 3 is a flow chart of the program for output pattern generation for this situation.

Program-driven signature analysis can also test inputs from boards that are not part of the kernel. An internal service switch can set the microprocessor to generate an input exercise. Such a test allows these boards to put latched data from every storage location onto the data bus for checking by signature analysis.

There are two primary points of concern in performing such a check of the read operation: determining by sequential elimination which board among many is malfunctioning and insuring that the circuits are properly initialized. Indeed, these concerns apply to both types of program-driven analysis and to free-run analysis as well. Moreover, they are part of a design checklist for designing in signature-analysis capability.

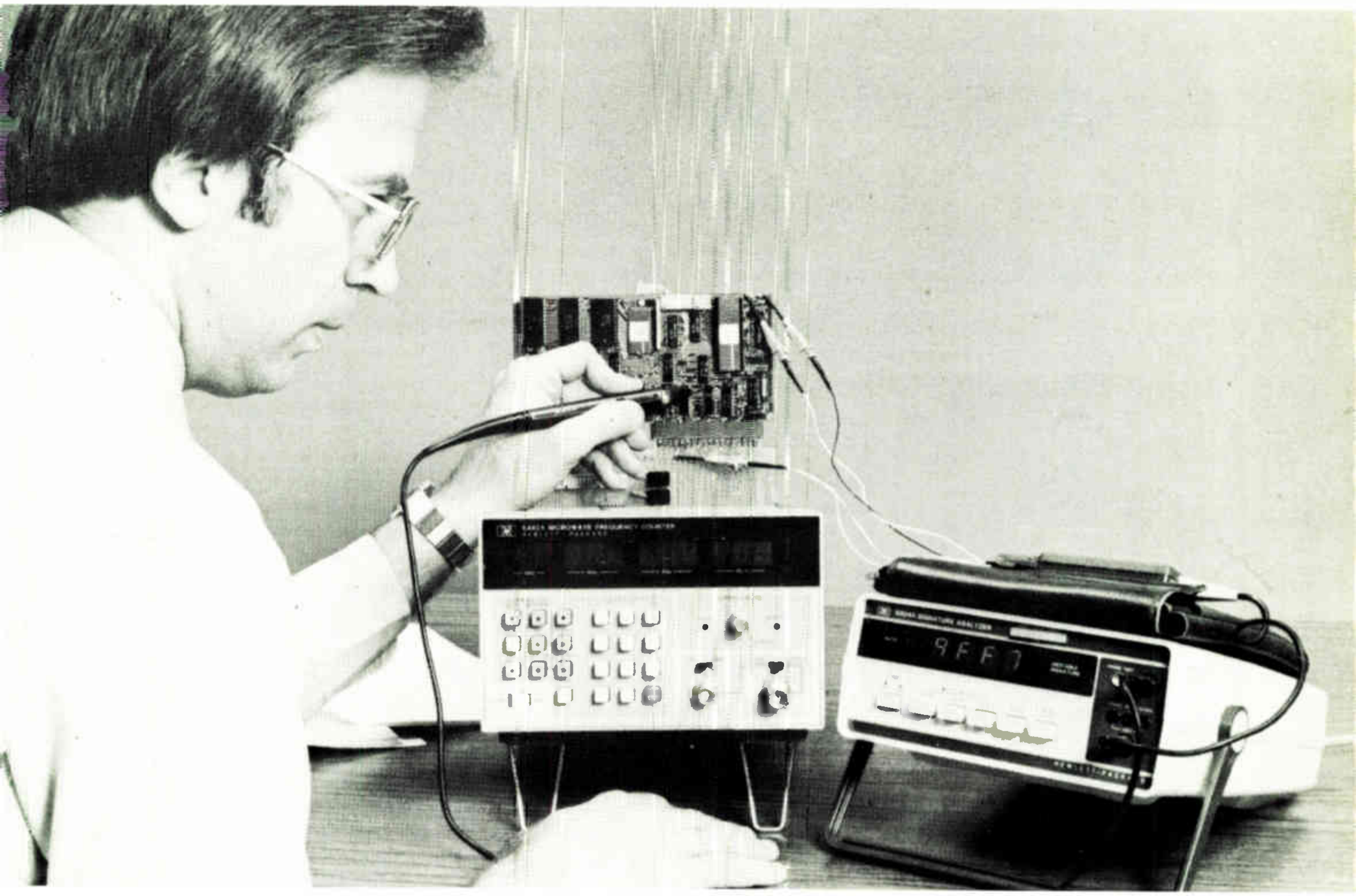
Design points to remember

Experience in designing microprocessor-based products that will work with signature analyzers suggests a list of six considerations that must be part of the design process. These six are:

- Distinguish the kernel.
- Provide a way to open local feedback paths.
- Insure initialization of the boards under test.
- Use address decoding to isolate ROM failures.
- Stabilize the signatures of three-state devices.
- Carefully document signatures.

The kernel should be on its own board, for one of the first steps in troubleshooting a malfunctioning system is to find out if the kernel free-runs. This test cannot be accomplished unless the kernel can be completely isolated (Fig. 4). If a separate board is not possible, then switches must be provided to isolate the kernel's components from the rest of the system.

A good case in point is a malfunction in which some device on the microprocessor's addresses and data buses continuously pulls a line high or low. It is not clear which device is malfunctioning. The solution is to attach to the kernel an extender board modified with isolating switches for the address and data lines (Fig. 5).



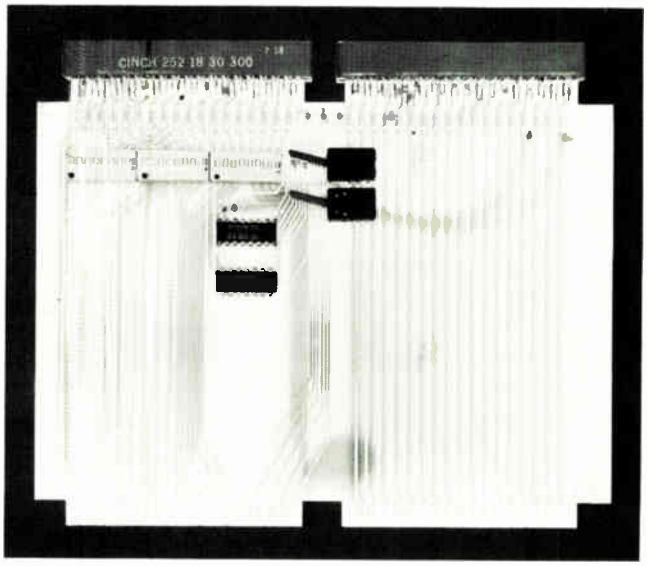
4. Shooting the kernel. An initial troubleshooting step is to isolate the kernel and check for signatures using the free-running mode, as shown. For a stuck node the rest of the system's boards may be added, one at a time, until a board causes a bad signature to appear.

To find the origin of stuck nodes on a product with an extender attached, the serviceman takes the signatures with all bus line switches closed. Then, on the lines giving incorrect signatures, he opens the extender-board switches and takes the signatures on their kernel side. A good signature on this side means that the bad signature on the other side is caused by a bad external device pulling that line high or low.

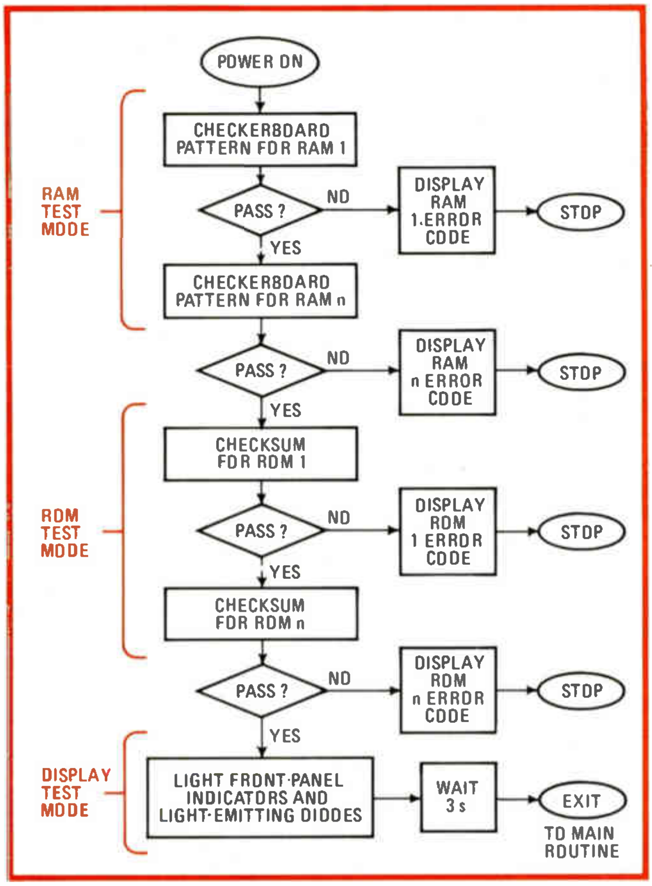
The next step is to determine which device is the bad one, and this can be a much simpler process if the designer puts each subsystem interfaced with the processor on its own board. Then the serviceman can simply add boards to the free-running kernel until the bad signature is seen again. He continues to use the extender board's switches to isolate stuck nodes.

A similar problem can occur with program-driven signature analysis that generates input tests. A read cycle involves all boards putting data on the bus, so it is necessary to test them in sequence by adding them one at a time to the kernel.

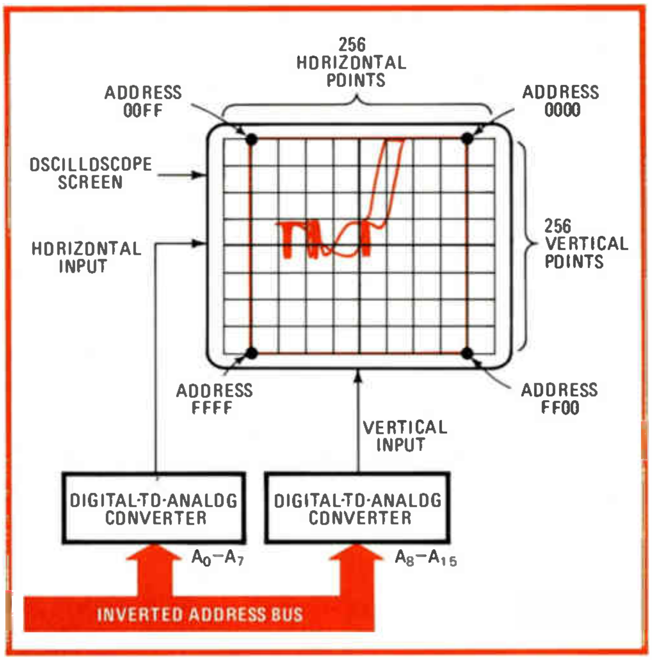
In this case, determining whether a particular board sends out data properly requires its isolation from other boards performing the same function. One tack is to pull all other boards putting out data, excluding the processor and ROM boards. Another tack is to isolate the board under test by an extender card with switches on the data lines. However, opening these switches does more than



5. Isolation. The modified extender board isolates the questionable boards' address lines and data lines from those of the bus. It also provides the serviceman with a manual reset capability and circuitry for address decoding (located near the board's center).



6. Power-on test. The diagnostic program charted describes a test routine for checking a system's RAMs, ROMs, and LEDs. The program is self-initiating at power-on and displays failure error codes. Internal switches or keyboard inputs can also start tests.



7. Mapping circuitry. Two 8-bit digital-to-analog converters provide oscilloscope mapping for a 16-bit address bus. This service aid can be built in or put on a separate board. The service manual must of course include maps of correctly operating systems.

isolate the board's data lines from the bus; it also removes the load supplied by the processor, and many switching power supplies will operate only with a full load. To compensate for this, the board needs another set of switches and some pullup resistors. With the switches, it is possible to select software designed to exercise only one board at a time.

Another way to isolate nodes is to operate the kernel in the free-run mode outside the instrument. To do this without an extender board, the serviceman may use jumpers to connect the supply, ground, and clock signal to the kernel. The designer can facilitate this procedure by providing easy access for the jumpers, such as test terminals.

The designer must provide the facility to open the feedback paths. If feedback is not broken when the signature-analysis program is sending a stimulus pattern to a device, then an error will propagate around the loop and all subsequent signatures will be wrong. It is a good idea to select an obvious feedback path to open, like the data bus of the kernel, where the added switches will interrupt the path.

Initialization of the boards under test is extremely important in signature analysis. Without initialization, consistent signatures cannot be guaranteed from one example of the product to another, or even in the same instrument from power-up to power-up. Some circuits initialize themselves with their own reset pulses after passing through one complete cycle. Otherwise, the designer must insure that the service manual documents an initialization procedure for the serviceman to follow.

Similarly, there must be provision for disabling asynchronous devices like monostables and interrupts. Also, multilayer boards should be avoided where there are bus lines going to several devices. It is difficult to use a current tracer with a multilayer board to discover which device is holding a bus line low or high.

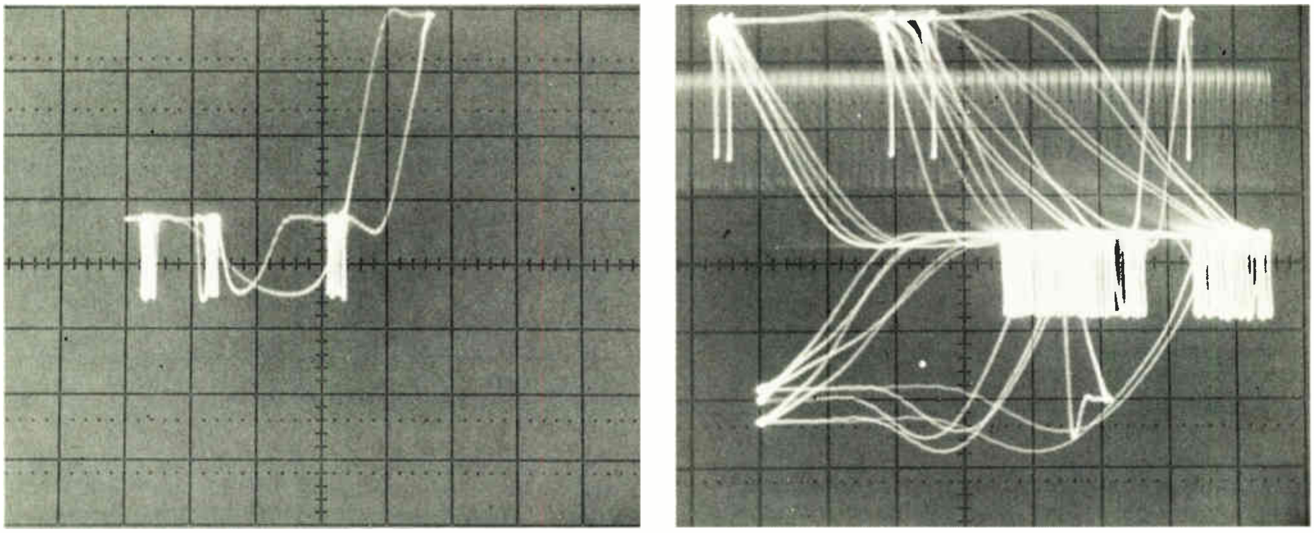
Spotting defective ROMs

The designer can facilitate isolation of a ROM failure by insuring that the address decoding circuitry is used to generate the measurement window for each chip. The chips shown added to the extender board in Fig. 5 perform this task. Then the start/stop signal for each ROM aligns with its first/last address, and the signatures appearing on the data bus come from only one device at a time (assuming that the output enables are working).

It also is important to provide for disconnection of the data bus when taking signatures on ROMs. In free-run analysis, other devices are being addressed and are putting out random data that results in erroneous signatures appearing on the bus lines.

Three-state devices can present a particular problem in obtaining stable, repeatable signatures. Nonrepeating signatures can occur if the start/stop window brackets the device's transition from high-impedance output to enable output when pullup resistors are absent.

To avoid this problem, pullup resistors should be on the board with the three-state device, not on some other board. Otherwise the extender board will need pullups to function when the board is isolated from the rest of the product. An alternative is to use address decoding that



8. Go/no-go pattern. The first map (a) indicates a properly operating system after the power-up diagnostic test. The second map (b) shows the same test on a similar system with the kernel malfunctioning. The serviceman checks the pattern, not individual points.

ensures the start/stop window only brackets the cycle time in which the three-state outputs are enabled.

Finally, it is up to the designer to provide the careful documentation of the signatures that will go into the service manual. Fortunately, there are several ways to insure that the signatures being read will be consistent from product to product.

The first step is to check that the signatures are stable and repeatable on several product samples. The second is to ensure that the signatures repeat when tested with different signature analyzers.

The most stringent test features reducing the clock frequency by 50%. This procedure should leave the signatures unchanged—otherwise there is a potential timing problem, probably due to excessive bus settling time and usually caused by the lack of pullup resistors on the bus lines. To reduce the clock frequency, all that is necessary is to pull the kernel out of the unit and to use an external pulse generator as a clock instead of jumpering the clock from the unit under test.

Moreover, it is important always to document the characteristic 1s signature for each new setup so that the serviceman can determine if the start/stop signals supplied to the signature analyzer are correct. This characteristic signature is obtained by placing the data probe on a transistor-transistor-logic high level that remains high during the start/stop window.

Designing a microprocessor-based product to work with signature analyzers is a giant step towards serviceability. However, the designer can do more to help out field service, and one important consideration to take into account is the inclusion of diagnostic subroutines.

Built-in diagnostics

Product-initiated self tests and user-callable tests are the two basic kinds of built-in diagnostics. Self-initiated routines are automatically exercised by the product every time some preset condition is met. A user-callable routine is exercised only when the serviceman selects it.

Figure 6 is an example of the flow chart of a self-initiated test. A convenient implementation point for such diagnostics is power-on. When the processor fetches its power-on address in ROM, a pointer causes program execution to begin with a check of RAM memory. In this routine, a checkerboard 1 and 0 pattern is written into each RAM and then read back. If this pattern is not identical to the one sent, the processor initiates display of an error code. In the HP 5370A universal time-interval counter, for example, a display readout of *Err 6.1* means that RAM 1 failed the check, while *Err 6.2* means that RAM 2 failed, and so on.

If all the RAMs pass the test, a ROM checksum test is next. The contents at each ROM location are added up until the final checksum is compared with the correct one—in this case, the sum in the first location of each ROM. An incorrect checksum will cause an error message on the display. In the 5370, *Err 7.1* means ROM 1 failed the checksum test, and so on. (Of course, this routine works only if that portion of ROM containing the diagnostic program is good.)

If all ROMs pass their checksum tests, the self-diagnostic program advances to a display check. All segments of the light-emitting-diode display and all front-panel lamps are lit briefly. These are, of course, just a few examples of the many kinds of checks that can be performed at power-on.

User-callable diagnostics

There are two basic ways for a designer to implement user-callable diagnostics. Some routines can be initiated by pressing the appropriate front-panel keys. Others can be selected by setting internal servicing switches to the appropriate codes. There are many choices as to which diagnostic routines to include, with the choice depending on the type of product.

One generally useful diagnostic routine is the algorithm-tracing program. The product goes through its usual operating algorithm but also displays mnemonic codes at key points.

For example, in the HP 5342A microwave frequency counter, striking SET, SET, 0 on the keyboard initiates a diagnostic program display in four points in the algo-

Design for serviceability check list

Taking into account the following field-service considerations at the initial design stage will realize several advantages. Service calls are shortened, redesigns are eliminated, extra equipment is not needed, and the manufacturer and customer see their costs reduced.

1. Are inputs and outputs protected from normal abuse?
2. Are light-emitting diodes used to advantage inside the instrument to indicate proper operation? For instance, a lighted LED could indicate a locked phase-locked loop, clock is present, power-supply voltage OK, etc.
3. Are components located far enough from integrated circuits to allow test clips to be placed on the ICs?
4. Can feedback be easily disabled for troubleshooting purposes? A good example would be a jumper wire that can be removed to break feedback between several ICs on a board. Sometimes feedback can be broken by pulling a board in the feedback loop.
5. Are display LEDs easy to replace?
6. Are there power terminals for logic-probe/pulser/current-tracer operation?
7. Are interconnecting cables long enough to allow operation of boards when placed on extenders?
8. Are boards independent? Avoid, if possible, a device on one board and its pullup resistor on another. If this is necessary for proper line termination, provide on the board a switchable pullup resistor for stand-alone testing.
9. Is it possible to manually force a node to a particular state for troubleshooting purposes?
10. Can the instrument be operated with any of its circuit boards removed, i.e. does the power supply require a certain load?
11. Are boards keyed so that they cannot be inserted incorrectly?
12. Have all three types of troubleshooting documentation techniques been considered? These are:

- Symptom cause: list symptoms and possible causes. This technique can be helpful when used with microprocessors that can display error codes when a specific failure occurs.
- Troubleshooting tree: test and branch based on results of test. A good tree requires more development time than any other approach since its developer must convince himself that the person following a fault through the tree will not get lost in a wrong branch.
- Growing the kernel: the instrument is exercised in a series of operating modes arranged in increasing levels of complexity so that each successive operating mode exercises a larger percentage of the instrument. By observing the first operating mode in the sequence that fails, it is possible to quickly limit the problem to those assemblies that are used in the failed operating mode but are not used in the previous modes that all passed.

rithm's operation. At the beginning of the sweep portion, *SP* is displayed, indicating that the instrument is sweeping its internal synthesizer for the desired intermediate frequency signal. When the signal is detected, sweeping stops and a *2* is displayed. Then the intermediate frequency is centered in the passband, the display shows *3*. To indicate determination of the harmonic number (the harmonic of the synthesizer that is mixing with the unknown to produce the intermediate frequency), the display shows *Hd*.

Yet another useful user-callable diagnostic that applies to many products is a keyboard/display check. Such a test gives the serviceman confidence in using the keyboard and display in other diagnostic checks.

To initiate this test, the serviceman hits SET, SET, 8 on the keyboard of the 5342A. The next key pressed fills the display with a unique character associated with that key. For example, pressing the 1 key results in a display reading of all 1s, and so on.

A go/no-go test

A third testing technique that can simplify servicing of microprocessor-based products is mapping, which helps the serviceman decide where to begin troubleshooting. In the 5370A time-interval counter, for example, the first check is of the kernel and associated buses, for they must be working in order to troubleshoot any of the counting circuits, the display, and the analog sections.

Mapping can quickly check the operation of the microprocessor and its communication with other boards in the unit without spending time to take signatures. However, it is a go/no-go evaluation, so when it indicates a bad kernel, signature analysis or some other technique must be used to isolate the failed component.

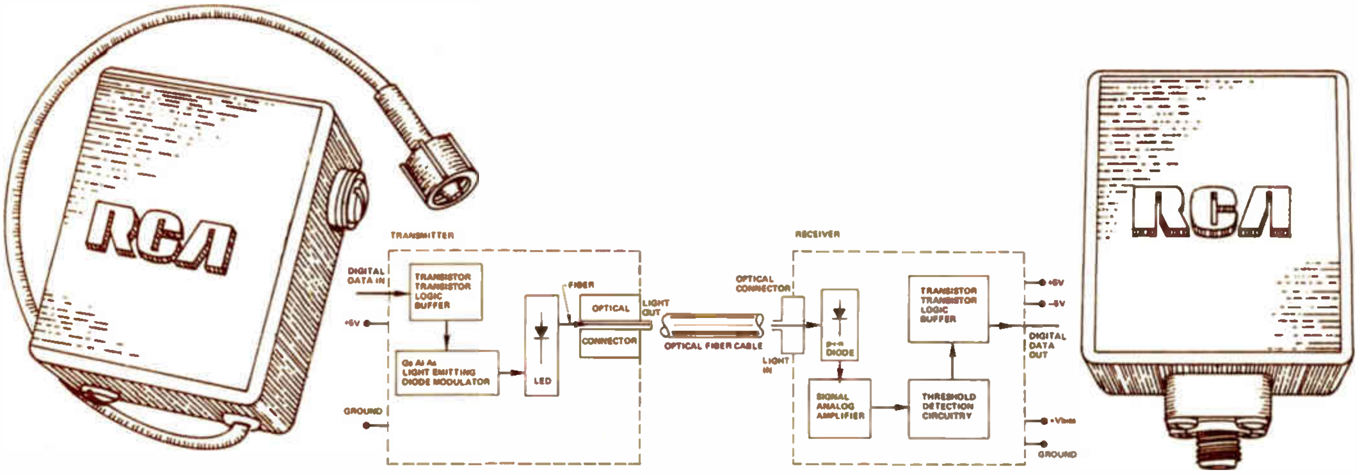
Essentially, mapping is a picture of the address bus, and the processor generates the picture as it performs its routines. In the 5370A, rather than connect a logic-state analyzer to all 16 lines of the address bus, two digital-to-analog converters on a special service board plug into the bus to supply analog levels to the X and Y inputs of an oscilloscope (Fig. 7). Each dot of the address matrix displayed by the scope represents an individual address. As the processor performs its programmed routines, these dots are connected together to form a map.

The 5370A is designed so that power-on with no input signal results in the map of Fig. 8a. The map appears after the microprocessor executes its power-up diagnostics of RAM, ROM, etc. It indicates that the kernel is working properly, that the data and address buses are clear and functional, and that the counter is waiting for an input signal to start the instrument.

It is important to realize that the serviceman is not looking for each dot of the map; he is interested just in the pattern. There are only 12 maps for the 5370A that he needs to be able to recognize. Documented in the service manual, they include such routines as: measurement in progress, start signal but not stop, free-run, read/write test patterns, trigger-level routine, reset, and display-rate hold.

If the scope shows any other pattern (Fig. 8b), then the processor has entered an undefined routine or is stuck in a portion of the algorithm. If the cause is suspected to be a board holding a line on the address bus low or high, boards can be removed one at a time until the proper map appears on the scope. Otherwise, it's on to signature analysis. ☐

Opening new frontiers with electro optics



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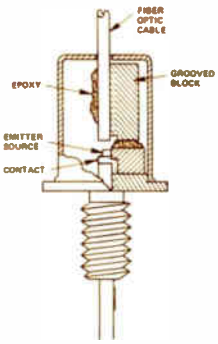

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NRZ coding	20	5	2	Mb/s
RZ coding	10	2 5	1	Mb/s
Min. peak optical output	100	100	100	μW
Receiver Module				
Input optical sensitivity	0 50	0 25	0 10	μW
Output digital signals—				
NRZ coding	20	5	2	Mb/s
RC coding	10	2 5	1	Mb/s

*Calculated bit error rate 10^{-9}

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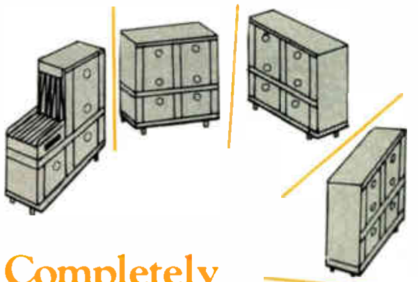

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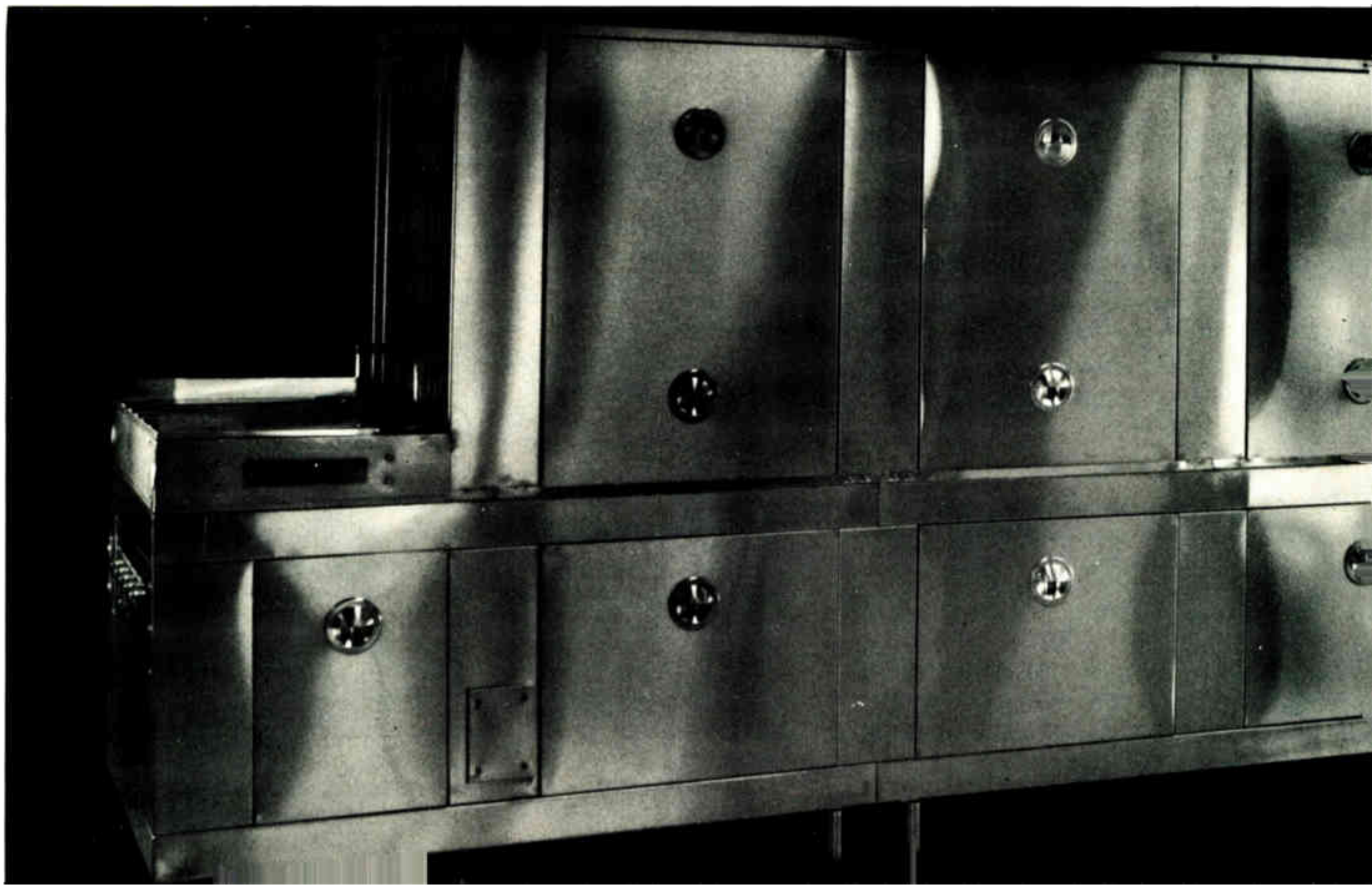

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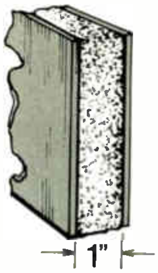

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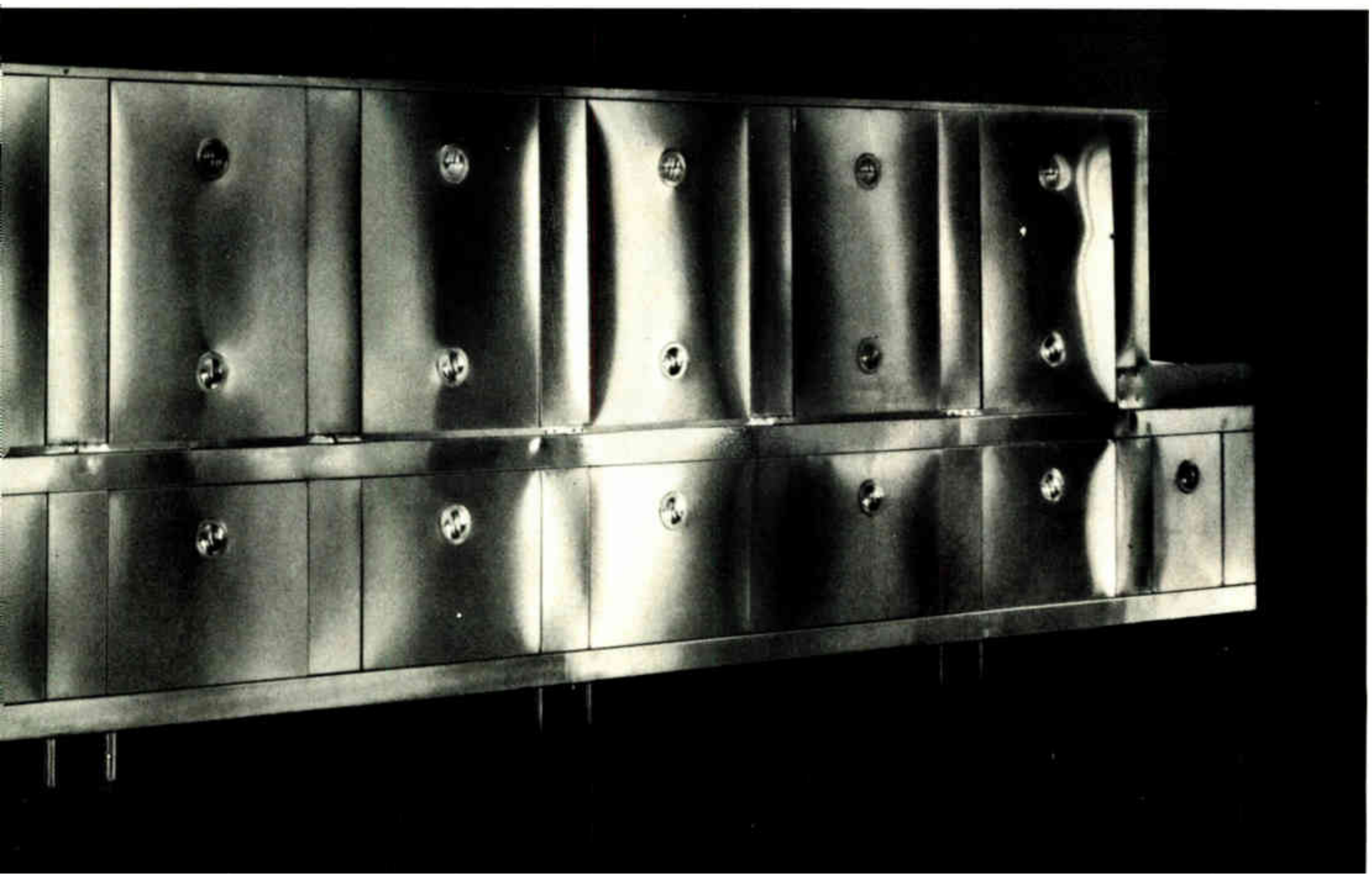

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Top-of-the-line sewing machines embroider from memory

High-density switch array, light-emitting diode display put user in touch with microcontroller

by Walter B. Hatfield, Donald R. Simon, and William H. Dunn, *The Singer Co., Fairfield, N. J.*

☐ Kitchen appliances were the first to benefit from replacement of mechanical components with electronics because the timing and speed functions being controlled were simple. But the more sophisticated operations of a sewing machine stalled the introduction of electronic control, requiring a design effort that stretched out development time and costs. The results, two top-of-the-line machines recently introduced by The Singer Company, combine innovations in touch-control technology with electronic intelligence to simplify manufacture and operation while adding functions that were never before available.

Electronic sewing machines are more reliable than all-mechanical models because they have fewer moving parts that can fail or wear out. Total parts counts go down, too. For example, the Touchtronic 2001* consumer sewing machine (Fig. 1) eliminated 350 parts—many of which were precision-made—of 1,100 in its immediate nonelectronic predecessor. Furthermore, electronic controls in both this machine and its industrial counterpart, the Centurion,* permit the use of automatic test equipment to speed and simplify assembly and test of the finished product and reduce the number of mechanical adjustments required.

Why sew electronic?

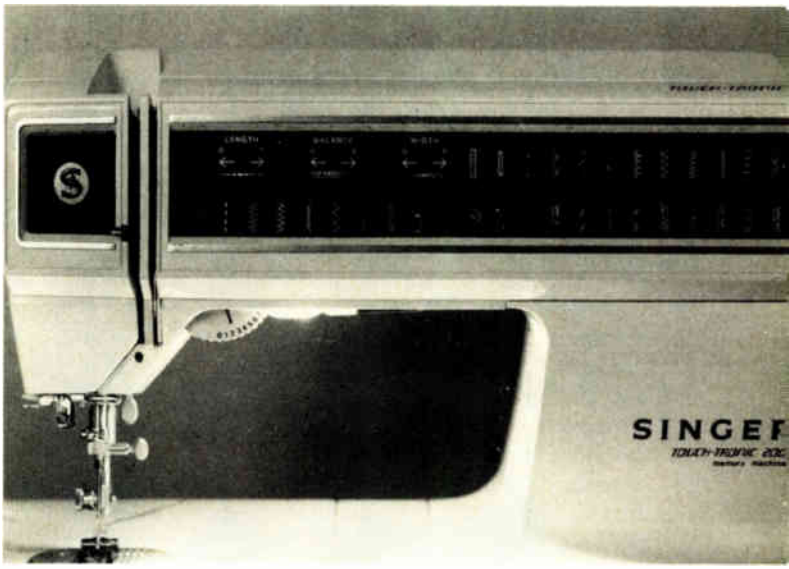
Elaborate mechanical machines have over 1,000 possible control setting combinations, set by panel switches, dials, and precision-made cams that control stitch pattern. Only a small percentage of these settings is useful, and in general this sophistication is lost to the user because controlling it is too complex. In the consumer machine, all settings except presser-foot pressure, thread tension, and power are made on a glass touch panel by a simple sequence of panel touches.

An important feature of electronic machines is that the internal logic can be preprogrammed to ignore inappropriate pattern modifications and prevent operator errors. For example, a straight-stitch pattern should always be set to zero width. Similarly, the balance control has no meaning for patterns without reverse stitches.

In these cases, and others, the panel override controls for stitch width (top left of the control panel in Fig. 1) are disabled, preventing changes in the stored stitch-width positions. Furthermore, the length override control in mechanical machines and in an earlier electronic machine provides only a single range of length modifications. But for any given pattern only a small portion of this range may be useful, requiring precise setting by the user. On the Touchtronic machine, the range of control is keyed to the selected pattern and implemented at moderate cost by six 5-by-20-bit lookup tables in read-only memory (ROM).

The override control is one example of how electronics enhances function while simplifying control. In the new machines electronics also permits:

- Greater pattern flexibility. Electronics removes mechanical restrictions on the number of stitches in a pattern. On mechanical machines, where stitch patterns are cut into the circumference of a replaceable cam, the practical limit to the number of stitches in a pattern is 24. Patterns can start or stop at only one point on the circumference, so the number of stitches in a pattern must divide integrally into 24. In an electronic machine, on the other hand, patterns always start and stop at their beginning. This makes pattern cycling possible wherein a



1. Smart machine. To choose a stitch pattern on this consumer sewing machine, the operator touches its symbol on the glass front panel. The three seven-segment LED digits indicate operator-selected modifications of basic stitch-pattern characteristics.

*A Trademark of The Singer Company

2. A stitch in time. The industrial model uses a microprocessor to speed repetitious work. In the learning mode, the machine records the stitch sequence and the speed of the operator. When switched to auto-sew, it repeats the sequence as the operator moves the material.

single command repeats an entire pattern.

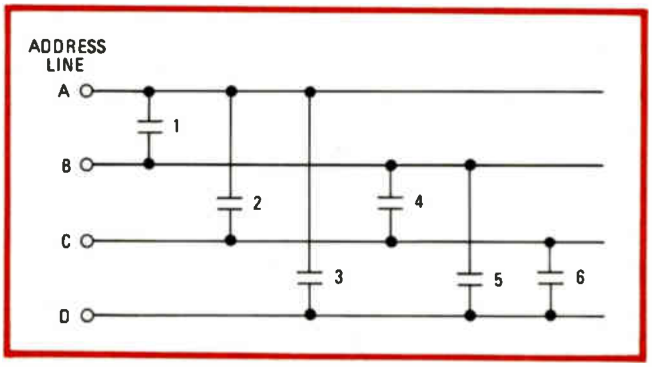
■ Longer patterns. The longest pattern in the Touchtronic machine has 59 stitches. The number of stitches in a pattern in an electronic machine is limited only by the amount of ROM allocated, at present requiring approximately 15 square mils of silicon per stitch. In Singer machines, each stitch is represented by an 11-bit word—5 bits for length, 5 bits for width, and 1 bit for control. The consumer machine contains 29 patterns with a total of 512 stitches.

■ Learning capability. The industrial machine, which is often used to perform the same task repeatedly, can be programmed to learn and repeat complete stitch sequences. Such data as speed of operation, the number of stitches between corners, and the time it takes the operator to reposition the material at each corner are recorded as the operator sews the pattern on a few samples. As an operator becomes proficient, the data base can be updated to reflect increased speed. When the machine is then switched from the learn to the auto-sew mode, it will repeat the stitch sequence stored in memory and the operator need only turn the work at corners. As with pattern lengths, the number of stitch sequences that can be stored is limited by the amount of memory, in this case random-access memory, allocated during design. To change any characteristic of a sequence, the operator enters the desired data through the unit's touch-control and display panel (Fig. 2).

Glass-front control panels are especially applicable to appliances since they have a modern look, are easy to clean and can contain operator instructions and decorative graphics. They are also inexpensive to manufacture, since an entire array of switches and low-cost thick-film decorative layers can be fabricated on a single substrate.

The glass panels used on the two electronic Singer sewing machines contain an array of touch-sensitive control switches. Each switch consists of two electrodes, which appear as a fixed capacitance across one of two matched transistors. A reference capacitance is connected across the other. Every 50 microseconds, both transistors are turned on and off while their discharge rates through the capacitances are measured.

When the operator touches a switch, the capacitance of his finger adds to the capacitance of the switch and



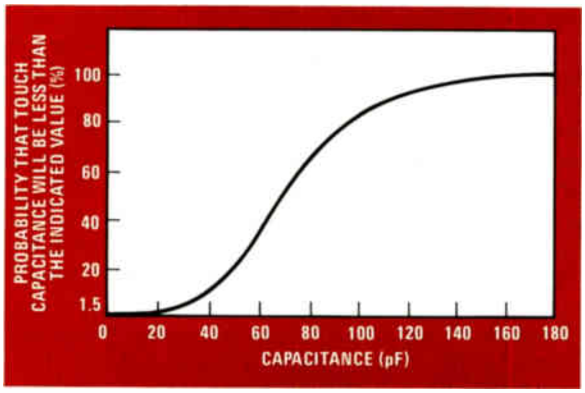
3. Which switch? To reduce the number of wires between the touch-switch array and the keyboard-interface chip, the two electrodes of each switch are connected to a unique pair of address pins on the chip. This coding scheme, shown schematically for six switches, allows N lines to address $(N^2 - N)/2$ switches.

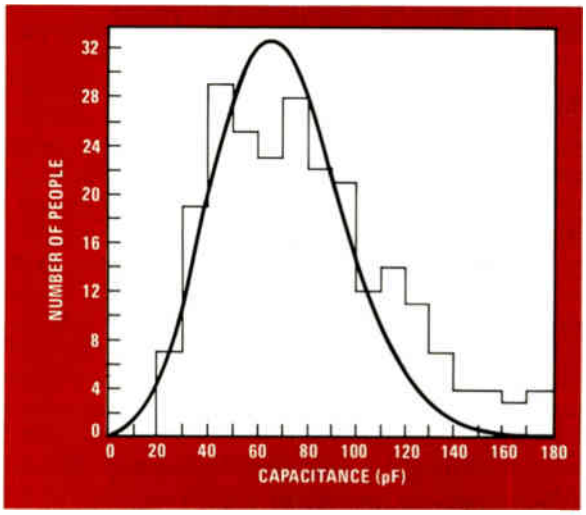
Capacitance by statistics

Since touch-sensitive switches are activated by human capacitance, they should be sensitive enough to respond to the touch of any operator, regardless of his particular capacitance characteristics. The switches should also activate reliably upon finger contact at various angles and pressures. Little information on the subject of human capacitance is available in technical literature, so Singer conducted its own study, using a test sample of 126 people.

The study found no correlation between capacitance and age, sex, physiology, apparel, cosmetics or medication. However, the range of capacitances fits a Poisson distribution with a variance of 7, as shown in the lower curve.

The upper curve is an integration of the lower distribution, and indicates the probability that an operator would fail to activate a touch switch with sensitivities between 0 and 180 picofarads. On the basis of the upper curve, the Touchtronic 2001 was designed to detect a minimum capacitive increment of 20 picofarads, which should occur for 98.5% of all touches.





lengthens the time constant across one of the transistors. This causes what is called a race condition, where the two transistors discharge at different rates, indicating selection of that switch.

In traditional touch-activation schemes, two thick-film electrodes on the rear of a glass panel are linked through a transparent thin-film counter electrode on the front. When the operator touches the counter electrode, he attenuates the voltage at the rear electrodes. The sensitivity of this kind of touch switch is a function of glass thickness as well as switch area. A typical touch-switch-activated microwave oven, for example, has a density of 0.7 switch per square inch.

Since a sewing machine is a relatively sophisticated appliance requiring a large number of operational controls, the touch control panel posed a density problem. For the Touchtronic machine, 41 switches had to be squeezed into a 20-square-inch panel. In the case of the Centurion machine, the required density is somewhat lower—1.25 switches per square inch. Two new approaches to touch activation succeed in achieving these high densities.

To remove the dependence on glass thickness, both electrodes of each switch are on the front of the glass substrate. The electrode patterns are etched in a transparent thin-film conductor, and then overlaid with a 1-mil-thick coating of glass for protection and aesthetics. (For an analysis of human capacitance characteristics, see "Capacitance by statistics").

A second innovation in touch-activation technique is the coding scheme used to address the switches (Fig. 3). Here the two electrodes of each switch connect to a unique pair of address lines on the custom keyboard-interface chip. This 2-of-N coding scheme allows N lines to address $(N^2 - N)/2$ switches. Once every 720 microseconds each address line is scanned. If the same pair of lines shows human capacitance increments on three successive scans, the operator is touching that switch.

The glass touch-panels are fabricated by laying down the transparent thin-film array of tin-oxide electrodes, two per switch, on one side of a soda-lime glass substrate. On the Touchtronic machine, nine thick-film layers then are applied to the front and rear of the substrate (Fig. 4).

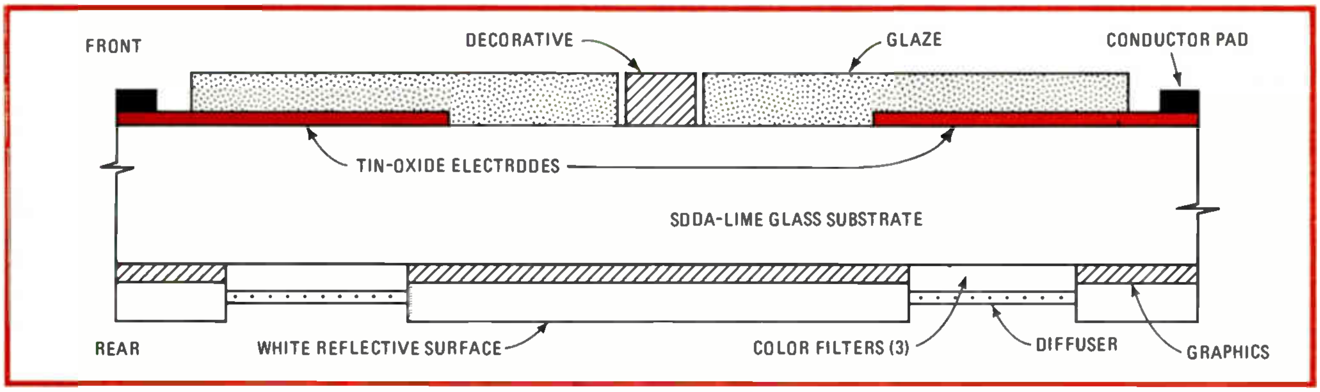
The first layer applied to the rear of the panel, the graphics layer, contains all the stitch-pattern symbols and machine status information. The position and color of this layer, that of the light-diffusing glaze layer and the color filters, and the optical density of the glass itself give the panels their blacked-out appearance.

The remaining thick-film layers serve more conventional purposes. On the front of the panel are a decorative layer (an orange stripe on the Touchtronic machine) and conductor pads for the tin-oxide electrodes. The rear of the substrate is overlaid with white reflective and diffuser layers that make the panel visually attractive when back-illuminated. Back-illumination of the area around a touch switch is possible only because there are no opaque thick-film electrodes on the rear of the panel.

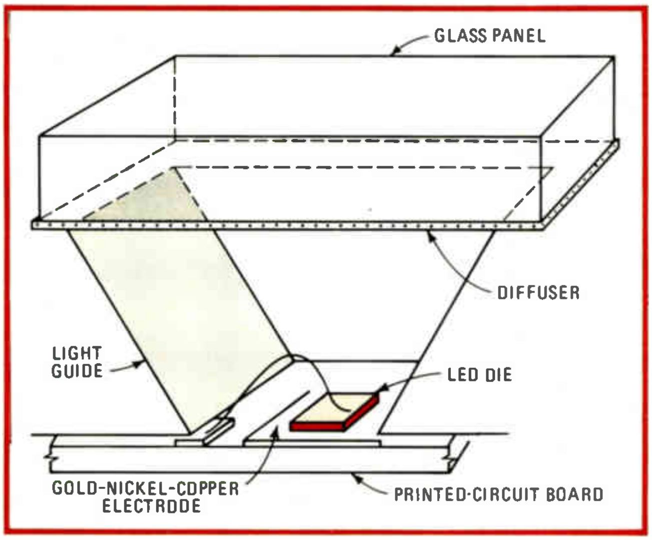
Lighting and displays

When the Touchtronic machine is first turned on, an array of incandescent lamps back-lights the various stitch options. If the operator selects a pattern for which the digital override controls are operational, a second array of incandescent lamps illuminates that portion of the panel.

The functional display elements of the Touchtronic machine are 55 light-emitting diodes. Of these LEDs, 21



4. Thick and thin. First step in the fabrication of the glass touch panels is deposition of the thin-film electrode array on the front of the substrate. Three thick-film layers then follow on the front and six on the rear. Absence of opaque layers on the rear allows back-lighting.



5. Spread out. The optical design and construction of the display converts the LEDs' bright spot outputs into softer, uniformly lit areas. Each die is epoxied to the printed-circuit board, then cured, wire-bonded, and coated for mechanical strength.

make up three seven-segment digital override functions—length, width, and balance. Of the remaining 34 LEDs, 28 indicate stitch patterns and 6 show machine functions.

Rather than incur the costs of purchasing and installing individual LED packages, Singer chose to package the LEDs as a hybrid array. Individual 10-by-10-mil LED dice are epoxied onto a printed-circuit board processed with gold/nickel/copper metalization, then cured and ultrasonically wire-bonded with aluminum-silicon wire 1 mil in diameter. Finally, the entire array is coated to give it mechanical integrity.

Figure 5 shows the optical design used to exploit the bright "spot" output of the LED. Each die is located at the bottom of a funnel formed by light guides. A diffuser at the top of the funnel on the rear of the glass substrate uniformly illuminates the display area.

The LEDs are driven directly from a custom large-scale integrated display chip. To minimize the number of pinouts and local heating, several different driving formats are used. The three seven-segment displays are time-multiplexed at 30% duty cycles; the 28 stitch-pattern LEDs are space-multiplexed in a five-by-six-dot matrix format; and the six machine-function LEDs are driven directly. The display chip also controls the incandescent lamps behind the digital override panel.

In the industrial machine, four five-by-seven-dot LED arrays display operational data, while switchable incandescent lamps illuminate fixed-format message areas. Here, the dead-front appearance of the panel and the illumination of only those options actually available help minimize operator distraction.

The electronic touch-panel assemblies for the Touchtronic and Centurion machines are fabricated at Singer's Controls division, headquartered in Schiller Park, Ill. Assembly involves the soldering of pins, using a standard infrared reflow process, between the glass panel and the printed-circuit board, which contains LEDs and incandescent lamps on its top surface and electronics at its rear. Each module is completed by inserting a light-pipe array between the glass panel and the printed-circuit board. This array enhances the forward radiation from the display devices and minimizes the leakage of light between elements.

Looking ahead

Prices of electronic controls and displays have now fallen to the point where they can be designed into top-of-the-line appliance models. But if electronics is to penetrate the large-volume models below the top of the line, further cost reductions will be needed. These reductions will result from optimized custom vs general-purpose LSI strategy, and from advances in packaging and fabrication technique. Areas currently being evaluated include the use of porcelain-clad steel-based hybrid circuits as a low-cost, high-reliability alternative to printed-circuit boards.

The cost of displays, too, must be reduced. Although individual LEDs cost only about 8 cents each in quantity, the large number of LEDs required for sophisticated appliances and the costs of light pipes and incandescent lamps make the display a major part of the cost of control. Lowest-cost displays will probably take the form of LSI-driven devices that can be batch-fabricated with the touch-switch and thick-film layers directly on the glass substrate. Integrated controllers with liquid-crystal displays that have been developed are still expensive, but this technology is a promising one for the future. □

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by Henry Davis, *American Microsystems Inc., Santa Clara, Calif.*

Label	Instruction		Comments
CORDIC	SLA	R1, 8	$A_0 = \theta \times 2^8$
	CLR	R2	X = 0
	LI	R3, 19898	$Y = 0.6072526 \times (2^{15})$
	CLR	R4	$X_0 = 0$
	MOV	R3, R5	$Y_0 = Y$
	CLR	R0	shift = 0 bits (i = 0)
	CLR	R6	zero counter
	NEG	R1	$A_i = -A_i$
L10	MOV	R1, R1	test sign of A_i
	JLT	L20	jump if negative to L20
	S	R5, R2	$X_i = X_{i-1} - Y_{i-1}/2^{i-1}$
	A	R4, R3	$Y_i = Y_{i-1} + X_{i-1}/2^{i-1}$
	S	@ARCTAN (R6), R1	$A_i = A_{i-1} - \arctan(½^{i-1})$
	JMP	L30	jump to L30
L20	A	R5, R2	$X_i = X_{i-1} + Y_{i-1}/2^{i-1}$
	S	R3, R3	$Y_i = Y_{i-1} - X_{i-1}/2^{i-1}$
	A	@ARCTAN (R6), R1	$A_i = A_{i-1} + \arctan(½^{i-1})$
L30	INC	R0	increment shift by 1
	INCT	R6	point to next arctan
	MOV	R2, R4	$R_4 = X_i/2^i$
	SRA	R4, R0	
	MOV	R3, R5	$R_5 = Y_i/2^i$
	SRA	R4, R0	
	CI	R0, 12	repeat until i = 12
	JNE	L10	
	B	*R11	
ARCTAN	DATA	11520	arctan (1) x 256
	DATA	6800	arctan (½) x 256
	DATA	3593	arctan (¼) x 256
	DATA	1824	arctan (1/8) x 256
	DATA	916	arctan (1/16) x 256
	DATA	458	arctan (1/32) x 256
	DATA	229	arctan (1/64) x 256
	DATA	115	arctan (1/128) x 256
	DATA	57	arctan (1/256) x 256
	DATA	29	arctan (1/512) x 256
	DATA	14	arctan (1/1,024) x 256
	DATA	7	arctan (1/2,048) x 256

☐ Real-time applications demand a speed and accuracy that microprocessors have been able to supply in only the simplest of such assignments. The 9900 microprocessor, though, does have both the necessary speed and an architecture and instruction set that allow sufficient accuracy for more difficult real-time applications.

One of the most important is signal processing. Virtually all signal-processing schemes require the calculation of sine and cosine values. After studying the 9900's instruction set, the initial decision might be to use a Taylor series expansion for these functions. In some cases, this approach will work well. But even if the multiplication can be performed quickly, a Taylor series is not efficient, since about 4½ other instructions can be executed in the amount of time it takes to perform one multiplication. Appropriate programming techniques, therefore, would yield faster results.

A better solution employs the coordinate rotation digital computer (Cordic) algorithm and scaled arithmetic. Widely used to generate sine and cosine functions in hand-held calculators, the two are handled easily by the 9900.

Scaled arithmetic is a form of floating-point arithmetic. But in this form a number is broken up into integer and fractional portions separated by a binary point, instead of being represented as a sign, mantissa, and exponent. The microprocessor's registers are similarly divided into two pieces, one for each portion of the number. In floating-point arithmetic, a general subroutine in the machine keeps track of the location of the decimal point; scaled arithmetic, however, requires the programmer to keep track of the binary point by scaling, or shifting the numbers to the proper place in the register. Although scaled arithmetic does not offer the precision or dynamic range of floating-point, it is faster and therefore useful in those real-time applications where the extra accuracy is not needed, but speed is critical.

Shifting and scaling

It is easier to perform scaled arithmetic operations on the 9900 because of its shift instructions. The shift operation is also valuable because shifting the contents of a register to the right has the same effect as dividing by a power of 2 and shifting left multiplies them by a power of 2. The shift-right and -left arithmetic instructions on the 9900 let any register be shifted by the amount contained in register 0 or a constant. This is very convenient, because now the exponent of 2 can be contained in register 0, so that the resulting shift is the same as multiplying or dividing by 2 raised to that exponent.

Based on the fact that any angle between 0° and 90° may be approximated by the sum or difference of a set of base angles, the Cordic algorithm uses scaled arithmetic to produce an accurate answer without multiplying. The set of base angles is defined by angle_i = arctangent $(1/2^{i-1})$; d_i is defined as the sign of the previous angle

1. Shifty. The Cordic algorithm calculates the sine and cosine of angle θ using only addition, subtraction, and shifting operations. Register 1 contains the scaled value of θ. After the 12 iterations, register 2 contains sine θ and register 3 contains cosine θ.

The 9900: a profile

Although not the first 16-bit microprocessor, the 9900 is one of the most powerful currently available. Produced by Texas Instruments Inc. as the TMS 9900 [*Electronics*, May 27, 1976, p. 99] and designed to be software- and hardware-compatible with TI's 990 minicomputer family, it is second-sourced by American Microsystems Inc. as the S9900. It is the only microprocessor to have a true memory-to-memory architecture. As a result of this architecture, computations may occur between registers, between registers and memory, or using the six possible addressing modes, between two memory locations.

The 9900 has more registers available to the user than most other microprocessors: 16 general-purpose and 15 index registers. Moreover, if 16 registers are not sufficient for an application, the 9900 has an instruction that will define a new set. Only 3 registers are contained in the processor itself: the program counter and the status and work-space registers (see figure). The 16 general-purpose registers are kept in memory.

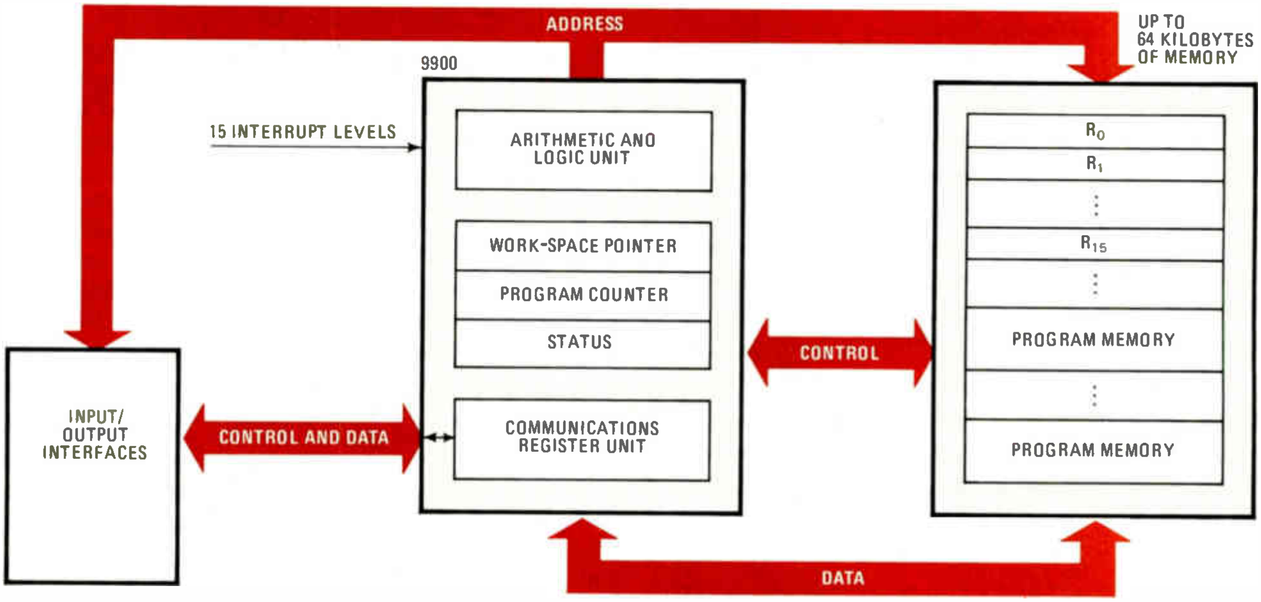
With 69 basic instructions and six addressing modes, the 9900's instruction set is considerably more complicated than the average microprocessor's. Yet rather than making the 9900 more difficult to use, the complexity of the instruction set makes programming easier. In fact the power and completeness of the instruction set produce such compact source code that programming time can be cut in half compared with that needed for other 8- and 16-bit microprocessors. What's more, programs written for the 9900 tend to be more readable, thus easing the burden of software documentation and maintenance.

Input and output on microprocessors generally rely on memory mapping or direct memory access. To these techniques the 9900 adds the easy-to-use communications register unit, which not only permits easier digital I/O, but also facilitates analog-to-digital conversion.

In addition, the family of components built around the 9900 increases the hardware designer's flexibility. Among the software-compatible special-purpose processors available are the 9980/81 8-bit data-bus processor and the 9940 microcomputer. The latter handles four interrupt levels and has 32 general-purpose I/O lines, 2 kilobytes of read-only memory, and 128 bytes of random-access memory on a single chip. The 9901 general-purpose I/O chip can support between 7 and 16 input/output lines with a software-programmable interval-event timer and decoding for 6 to 15 interrupt levels.

Two communications chips are available: the 9902 universal asynchronous receiver-transmitter, which comes in an 18-pin package and has programmable transmission rates; and the 9903 programmable synchronous communications controller, which supports all synchronous protocols with minor amounts of software.

The only additional circuitry needed to make the 9900 function is the 9904 four-phase clock-driver circuit.



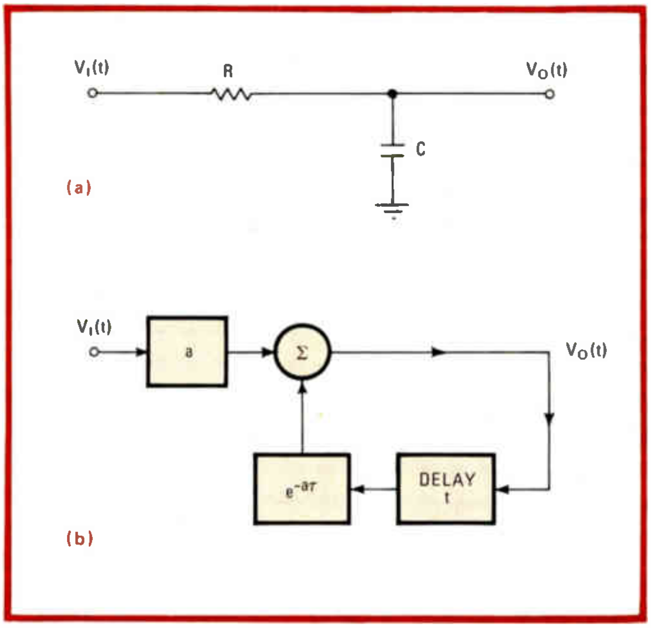
A_{i-1}; and $R_n = 1/\cos d_1A_1 \ldots \cos d_nA_n$. Generally, 12 iterations give enough accuracy, and at $n = 12$, R_n is a constant and equals 1.647. Letting the starting terms $A_0 = -$(the given angle θ), $X_0 = O$, and $Y_0 = 1/R_n = 0.60725$ and letting i go from 1 to 12, the algorithm may be stated as:

$$X_i = X_{i-1} - d_i \times Y_{i-1}/2^{i-1}$$
$$Y_i = Y_{i-1} + d_i \times X_{i-1}/2^{i-1}$$
$$A_i = A_{i-1} - d_i \times \arctan 1/2^{i-1}$$

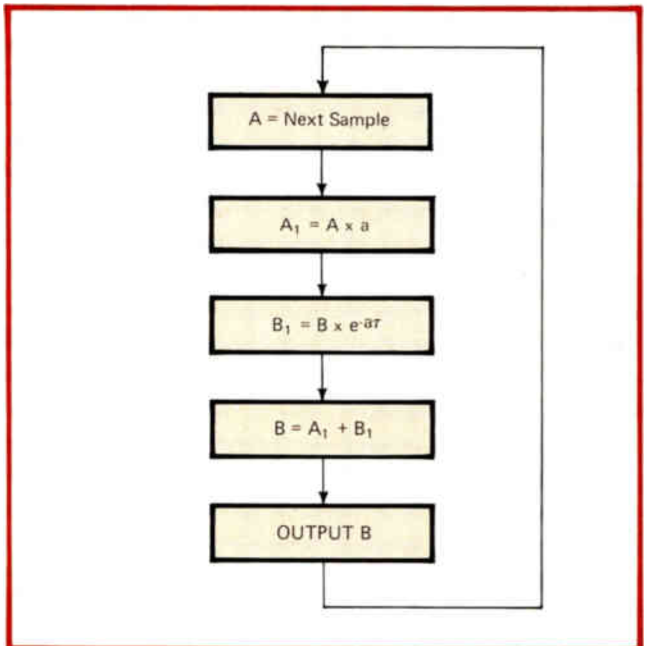
If the arctangents are stored in a table, only shift, add, and subtract instructions are required to implement the algorithm. The 9900 does this readily, since its instruction set already includes 16-bit arithmetic and it can perform a variable shift. After the 12 iterations, X_{12} = sine θ and Y_{12} = cosine θ. Figure 1 shows the complete Cordic algorithm and the table of base angles.

By using the computational power of the 9900 with appropriate algorithms like Cordic, other real-time functions such as digital filtering can be performed at rates not possible with other microprocessors. Optimal digital Wiener filters and Kalman and other theoretically optimal filter methods are practical with the 9900.

As an example of a simple digital filter algorithm,



2. Low-pass. Digital filtering is one of the real-time applications the 9900 is well suited for, especially theoretically optimal filter methods. This simple low-pass filter (a) can be represented by the digital filter (b), where a is the filter characteristic and τ is the sampling interval.



Instruction		Comments
LI	R12, AD	point to a-d converter
LDCR	R1, 11	get 11 bits
MPY	@A, R1	$A_1 = A \times a$
MPY	@EAT, R3	$B_1 = B \times e^{-a\tau}$
A	R1, R3	$B = A_1 + B_1$
LI	R12, DA	point to d-a converter
STCR	R3, 11	output data
IDLE		wait for next sample

3. Digitized. This flow chart and the corresponding 9900 code implement a digital low-pass filter. Once again, scaled arithmetic is used for the filter characteristic a and $e^{-a\tau}$. This program allows a sampling rate of up to 19,200 samples per second.

consider the low-pass filter of Fig. 2. The Laplacian notation for the transfer function of this filter in terms of the complex frequency s is given by:

$$G(s) = \frac{V_O(s)}{V_I(s)} = \frac{1/sC}{R + 1/sC} = \frac{1}{1 + sCR} = \frac{a}{a+s}$$

where the filter characteristic a = 1/CR. This characteristic is approximately equal to 2s when s is the upper 3-decibel frequency of the filter.

Because $V_I(t)$ is an impulse function at time t = 0, $V_I(s) = 1$ and $G(s) = V_O(s)$. The problem of finding G(s) is thus reduced to obtaining the output of the filter when the input is an impulse. Solving for G(s) yields $G(t) = ae^{-a\tau}$ where τ is the sampling interval. Because $V_I(t)$ is a sampled function, only $V_O(t)$ at 0, τ, 2τ . . . $n\tau$ is of interest. Using the transformation:

$$L\{\delta(t-\tau)\} = e^{-st}$$

$V_O(t)$ becomes $V_O(s)$ and:

$$G(s) = ae^{-a\tau}e^{-s\tau} = ae^{-2s\tau} + \ldots ae^{-n\tau}e^{-ns\tau}$$

The sum of this geometric progression is:

$$G(s) = \frac{a}{1 - e^{-a\tau}e^{-s\tau}}$$

Because this form is not very suitable for computers, G(s) is rewritten as:

$$V_O(s) = aV_I(s) + e^{-a\tau}V_O(s)e^{-s\tau}$$

Figure 3 shows the computer implementation of a general low-pass digital filter. Note that both the filter characteristic a and $e^{-a\tau}$ are constants and could be changed by the program during execution, thereby allowing the output signal-to-noise ratio to be optimized.

In order to minimize the program, the input, a, and $e^{-a\tau}$ are assumed to be scaled and less than 1. The throughput of the program allows a maximum sample rate of 19,200 samples per second and may be increased by utilizing memory-mapped input/output techniques for transmitting and receiving data.

Changing the addition to a subtraction and negation combination yields a high-pass digital filter. Appropriate combinations of these filter functions yield bandpass and notch filters with lower sampling rates.

In computer and microcomputer systems, the control of I/O devices often requires real-time processing. The 9900 lends itself to these applications, too, because of its communications register unit, or CRU. Data is transmitted and received by the unit in serial form using three dedicated processor lines. Special CRU instructions permit the transfer of data fields ranging from 1 to 16 bits in length. Because variable-length I/O fields are easily manipulated, I/O interfaces having simplified circuit layouts, increased density, and lower component costs can be easily designed.

Controlling I/O

For example, controlling the push buttons and other switches used in the majority of input devices can account for up to half of the code in an applications program. Typically, the state of a switch is sensed and the appropriate action initiated under software control.

These switches may be sensed as groups or individually and may be context- or sequence-sensitive.

Many microprocessors allow sensing only in groups, thus requiring software to determine the switch responsible for the signal. For example, one instruction may get the switch data, another may mask off the undesired bits, and a third may test for equivalence with a specific bit pattern.

A single 9900 CRU instruction—test bit (TB)—however, can test the status of any single CRU I/O line and set or reset the status register's equal bit based on the state of the switch. Conditional jumps—jump if equal (JEQ) and jump not equal (JNE)—are then used to transfer control to the appropriate section of the program.

Particularly important is the fact that this method requires no program registers or memory locations in order to test individual bits. The companion instructions for single-bit CRU output are: set the bit to 1 (SBO) and set the bit to 0 (SBZ). Like the TB instruction, they require no work-space memory.

To determine the bit affected by any of these instructions, add twice the displacement in the operand field to register 12. The result is an address that is twice the logical address, because the least significant bit of the address bus is internal to the processor.

Though the single-bit CRU instructions help optimize software and hardware for sampling individual switches, it is often desirable to obtain the state of multiple switches. By using a single instruction, store CRU (STCR), any number of bits from 1 to 16 may be transferred to a register or memory, with the location of the starting bit defined by register 12.

For example:

```
        LI      R12,BEG
        STCR    R1,3
```

will transfer 3 bits from the CRU starting at BEG to register 1. Using these two instructions, only minimal hardware and software are needed to meet virtually all input requirements.

Driving printers

Probably the most popular output device in many applications is the dot-matrix printer. It, too, is easily supported using CRU techniques and appropriate software. Microprocessor systems often have surplus time when results are to be printed. By using this time, component count and peripheral complexity may be significantly reduced.

The main responsibility of software for a printer driver is to turn specific lines on and off for predetermined intervals. To accomplish this, software timing loops can be used. Software timing is based on the fact that each instruction requires a specific amount of time to be executed based upon a fixed clock cycle. The accuracy of the timing is proportional to the accuracy of the processor clock. The latter is usually accurate enough for software timing, but some applications may require crystal-controlled clocks for repeatability from unit to unit.

Switch debouncing provides a simple example of software timing. Because a switch may bounce for up to 40 milliseconds after first contact, the program must ensure that the switch is not resampled during this time.

Label	Instruction		Comments
PRINT	SBZ	DRIVE	start head moving
P10	TB	POS 1	wait until position 1
	JNE	P10	
	LI	R7, DEDB	margin delay and debounce
P20	DEC	R7	
	JNE	P20	wait
P30	LI	R2, 5	5 columns
	MOVB	*R1+, R3	get characters into R3
	SRL	R3, 8	put into lower byte
	ANDF	R3, 73F	limit to ASCII uppercase
	MPY	R2, R3	get displacement
	AI	R4, TAB	R_4 = table index
P40	MOVB	*R4+, R3	R_3 + next column of dots
	SRL	R3, 8	
	LDCR	R3, 9	
	LI	R7, 45	300-µs timer for on time
P50	DEC	R7	
	JNE	P50	R_7 = 0 at exit
	LDCR	R7, 9	clear drivers
	LI	R7, IDG	inter-dot wait (typically 1.2 ms)
P60	DEC	R7	
	JNE	P60	
	DEC	R2	next dot column
	JNE	P40	continue until 5 columns
	LI	R7, ICG	inter-character wait (typically 1.2 ms)
P70	DEC	R7	
	JNE	P70	
	DEC	R8	all characters out?
	JNE	P30	continue until done
P80	TB	POS 1	wait until home position
	JEQ	P80	
	SBO	DRIVE	stop head
	RT		return

4. Print out. To drive a five-by-seven-dot matrix printer, this program takes advantage of software timing. The loops at lines P20, P50, P60, P70, and P80 provide the necessary pauses between dots and characters and allow head movement across the carriage.

For example:

```
L10   TB    SWITCH
      JEQ   L10
```

makes the processor wait for the switch transition. Following that code with:

```
      instructions:        execution period:
      LI    Rx,2000        ;12 cycles
L20   DEC   Rx             ;10 cycles
      JNE   L20            ;10 cycles repeated 2,000 times
```

makes the processor wait for $20 \times 2{,}000 + 12$ cycles, or 13.33 ms assuming a 3-megahertz clock rate. This loop could of course be fine-tuned and shortened by the amount of time consumed by the minimum path back to the sampling routine, thus increasing throughput.

The second requirement for the printer driver is to translate from ASCII to an appropriate dot code. Assumed in this program is standard coding for a five-by-seven-dot matrix in the program data segment. Figure 4 illustrates a basic printer driver; options for error detection may be easily added in the appropriate sections. □

Measuring an op amp's common-mode impedance

by James P. Ary and R. W. Stow, *California Institute of Technology, Pasadena, and Ohio State University, Columbus*

To measure a differential amplifier's common-mode input impedance using the conventional partial-deflection method,[1] a resistor on the order of 10^8–10^{14} ohms must be placed in series with the input port to be checked. But the insertion of such a large resistance, which is used to create small signal-voltage differences across the differential inputs, causes errors in measurement. For one thing, dc offset currents are generated, and, for another, there is pickup from unwanted signal sources.

But, by taking advantage of the normally high common-mode rejection ratio (CMRR) of the op amp, a resistor whose value is several orders of magnitude lower can be used, and the common-mode impedance can be measured more easily and accurately.

As shown in the figure, the common-mode input impedance, Z_{icm}, is the impedance of the parallel combination of effective resistance, R_i, and capacitance, C_i, between either input of a differential amplifier and common ground. To measure the Z_{icm} of the inverting side of the amplifier with this method, a resistor, R_s, is placed between the two input leads, instead of (as in the partial-deflection technique) in series with the input to be measured. A forcing function, e_i, is then applied to the noninverting input terminal.

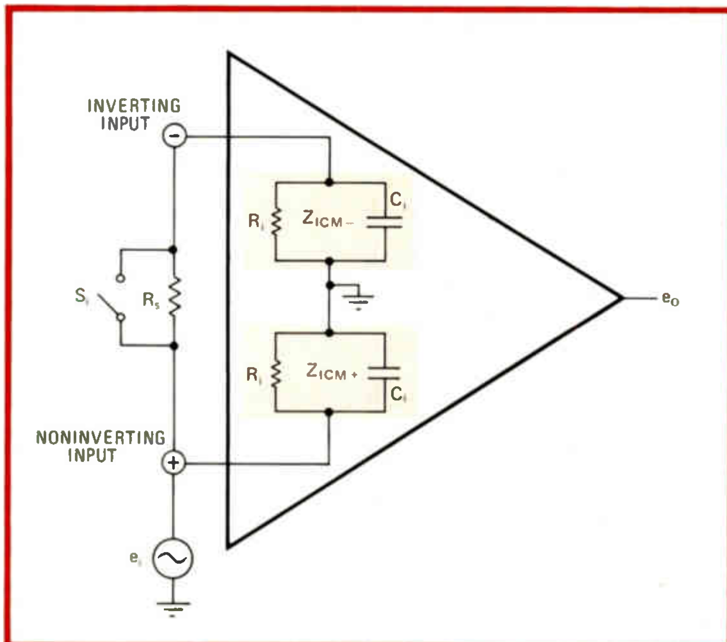
The voltage at the inverting input, e_i', is thus e_i minus the voltage drop (IR drop) across R_s. The difference voltage is amplified, and so the voltage at the output is $e_o' = A(e_i - e_i')$, where A is the amp's differential voltage gain.

If the CMRR of the op amp is known and is high enough to make the output voltage with S_1 closed (e_o) much smaller than that with S_1 open (normally both conditions will hold), then R_i can be determined accurately. It will also be necessary for the frequency of the sine-wave input signal to be low enough to make the input reactance, X_{ci}, much larger than R_i. If all these conditions are met, then:

$$e_o' = A(e_i - e_i')$$
$$e_i' = e_i R_i/(R_i + R_s)$$
$$e_o' = Ae_i R_s/(R_i + R_s)$$

If R_s is selected so that $R_i > R_s > R_i/(\text{CMRR} - 20\text{ dB})$, then from the equation for e_o', $R_i = Ae_iR_s/e_o'$. Assuming e_o' can be accurately measured, R_i can be measured for values of up to 10^{10} ohms with 10% accuracy for CMRR = 100 dB and R_s = 1 megohm.

To determine C_i, the frequency of e_i' must be increased to a value where e_o' rises at a rate of 20 dB per decade but below the point where the op amp's recognized bandwidth and output level are exceeded. Then $X_{ci} = Ae_iR_s/e_o'$, or $C_i = e_o'(2\pi fAe_iR_s)$. To determine R_i and C_i at the noninverting port, it is only necessary to



COMMON-MODE DATA: 741 OP AMP

Test conditions: $A = 100$, $e_i = 1$ V, $R_S = 1$ MΩ

Frequency (Hz)	e_o' (V) Inverting input	e_o' (V) Noninverting input	e_o (V)
1.0	0.06	0.06	0.002
3.2	0.06	0.06	
10.0	0.06	0.07	0.002
32	0.105	0.11	
100	0.32	0.32	0.005
320	0.98	0.92	
1,000	3.05	3.05	0.041
R_i (GΩ)	1.7	1.4	
C_i (pF)	4.9	4.6	

Accurate. Common-mode impedance can be measured more accurately than with conventional partial-deflection method by using a relatively low-value source resistor, R_s, in shunt with op amp's input, to create the required differential voltage. High common-mode rejection ratio of op amp makes this technique possible. Table shows representative data for determining R_i, C_i values for 741 op amp.

place the signal source at the inverting input and repeat the measurements.

The accompanying table lists representative output-voltage value versus e_0 and input frequency for a differential circuit using 741 amps. Included are the corresponding values of R_i and C_i. The uncertainty in the values is equal to the ratio of e_o to e_o', provided $R_s << Z_{icm}$ at the test frequencies. Note that R_i and C_i take into account leakage resistance and lead capacitance of the mounted amplifier. For FET-input amplifiers, R_s is raised to 100 megohms and the driving frequency is lowered to 0.01 Hz or less. For measuring R_i up to 10^{14} ohms, simple shielding of the amplifier will suffice. □

References

1. G. E. Tobey, J. G. Graeme, and L. P. Huelsman, "Operational Amplifiers," McGraw-Hill, New York, N. Y., 1971, Appendix B.

Calculator notes

HP-67/97 tracks communications satellites

by D. C. Mitchell

Milan, Mich.

Tracking the movements of beacon and communications satellites is extremely easy with this HP-67/97 program. Given the various orbital parameters, which include the satellite's equatorial crossing longitude and time, its inclination, its height above earth, and the period of revolution, the program will compute where the object is at any time with respect to an observer on earth.

Working on a set of six equations that are expressed in spherical coordinates, the calculator quickly solves a problem too cumbersome to do by hand. Although the equations are based on the satellite's orbit being circular, the results generated are adequate for all but extremely elliptical orbits.

Knowing the satellite's inclination, ψ, or the angle of the orbit with respect to the earth's equator, the program finds the subsatellite latitude (the latitude on earth corresponding to the satellite position directly overhead) from:

$$L_s = \sin^{-1}[\sin(360\tau/P) \sin \psi] \quad (1)$$

where τ is measured from the time the satellite crosses the equator and P is the satellite's revolution period. The longitude of the subsatellite point is then found:

$$\lambda_s = \cos^{-1}[\cos(360\tau/P) \div \cos L_s] + \tau/4 + L_e \quad (2)$$

where L_e is the equatorial-crossing longitude. For satellite inclinations of less than 90°, the term $\tau/4$ must be preceded by a minus sign, instead of the plus sign that is shown in Eq. 2.. 145

Once λ_s has been calculated, the angle between the line joining the center of the earth and the observer and the line joining the center of the earth and the subsatellite point is determined:

$$\theta = \cos^{-1} [\sin L_o \sin L_s + \cos L_o \cos L_s \cos(\lambda_s - \lambda_o)] \quad (3)$$

where L_o and λ_o are the observer's latitude and longitude, respectively. Equations 1 through 3 enable finding the azimuth and elevation of the satellite:

$$A = \cos^{-1}\left[\frac{\sin L_s - \sin L_o \cos\theta}{\sin\theta \cos L_o}\right] \quad (4)$$

and

$$E = \tan^{-1}\left[\frac{\cos\theta - (R/R+h)}{\sin\theta}\right] \quad (5)$$

where R is the radius of the earth, equal to approximately 6,369 km at latitudes of 45° or so, h is the mean height of the satellite, and 0° azimuth is understood to be north, increasing in the clockwise direction.

To check the program, consider the Oscar 7 satellite, used for radio-amateur communication, that had ψ = 101°, P = 115 minutes, and H = 1,460 km when it crossed the equator at longitude 67.2 W on Jan. 19, 1979, at 00:24:16 Greenwich Meridian Time. Keying in the known data and the local longitude and latitude information for Milan, Mich. (42 and 83 respectively), generates the azimuth-elevation data shown for 1-minute intervals. Note the satellite is below the horizon during times when the elevation angle is negative. The distance, d, given by:

$$d = [(R+h)^2 + R^2 - 2(R+h)R \cos\theta]^{1/2} \quad (6)$$

is the direct-line path from the observer to the satellite, not the Great-Circle distance. □

Engineer's notebook is a regular feature in Electronics. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.

OSCAR 7 TRACKING DATA

τ	A (°)	E (°)	d (km)	L_s (°)	λ_s (°)
0.2416	157.0436	−8.0126	5529.8384	0.0000	67.1200
0.2516	156.5726	−5.1635	5177.8256	3.0422	68.0252
0.2616	156.4909	−2.2138	4824.2432	6.0843	68.5357
0.2716	156.3917	0.4553	4469.9527	9.1302	69.4527

HP-67/97 SATELLITE-TRACKING PROGRAM

Line	Key	Line	Key	Line	Key	Line	Key
001	f LBL A	044	f cos	087	×	130	RCL 8
002	STO A	045	RCL 0	088	2	131	f sin
003	h RTN	046	f cos	089	×	132	f x < 0
004	f LBL B	047	÷	090	RCL 4	133	GTO 01
005	STO B	048	g cos^{-1}	091	g x[illegible]	134	h R↓
006	h RTN	049	h RCI	092	RCL 5	135	3
007	f LBL C	050	4	093	RCL 4	136	6
008	STO C	051	÷	094	+	137	0
009	3	05?	+	095	g x^2	138	h x ⇄ y
010	6	053	RCL A	096	+	139	−
011	0	054	+	097	h x ⇄ y	140	STO 9
012	h x ⇄ y	055	STO 2	098	−	141	GTO 02
013	÷	056	3	099	f √x	142	f LBL 1
014	STO C	057	6	100	STO 6	143	h R↓
015	h RTN	058	0	101	RCL 3	144	STO 9
016	f LBL D	059	−	102	f cos	145	f LBL 2
017	STO D	060	x > 0	103	RCL 4	146	h RCI
018	h RTN	061	STO 2	104	RCL 4	147	.
019	f LBL E	062	RCL D	105	RCL 5	148	0
020	STO E	063	f sin	106	+	149	1
021	h RTN	064	RCL 0	107	÷	150	×
022	g LBL a	065	f sin	108	−	151	RCL B
023	STO 4	066	×	109	RCL 3	152	h H.MS+
024	h RTN	067	RCL D	110	f sin	153	DSP 4
025	g LBL b	068	f cos	111	÷	154	f -x-
026	STO 5	069	RCL 0	112	g tan^{-1}	155	RCL 9
027	h RTN	070	f cos	113	STO 7	156	g →H.MS
028	g LBL c	071	×	114	RCL 0	157	f -x-
029	STO 1	072	RCL 2	115	f sin	158	RCL 7
030	h RTN	073	RCL E	116	RCL D	159	g →H.MS
031	f LBL 0	074	−	117	f sin	160	f -x-
032	RCL C	075	STO 8	118	RCL 3	161	RCL 6
033	h RCI	076	f cos	119	f cos	162	f -x-
034	×	077	×	120	×	163	RCL 0
035	f sin	078	+	121	−	164	g →H.MS
036	RCL 1	079	g cos^{-1}	122	RCL 3	165	f -x-
037	f sin	080	STO 3	123	f sin	166	RCL 2
038	×	081	f cos	124	RCL D	167	g →H.MS
039	g sin^{-1}	082	RCL 4	125	f cos	168	f -x-
040	STO 0	083	×	126	×	169	f ISZ
041	RCL C	084	RCL 4	127	÷	170	GTO 0
042	h RCI	085	RCL 5	128	g cos^{-1}	171	R/S
043	×	086	+	129	STO 9		

Registers	
R_0	L_S
R_1	ψ
R_2	λ_S
R_3	θ
R_4	R
R_5	h
R_6	d
R_7	E
R_8	$\Delta\lambda_S$
R_9	A

Labels	
A	L_e
B	τ
C	$360\tau/P$
D	L_o
E	λ_o
I	$\Delta\tau$

Instructions

- Key in program
- Enter satellite's equatorial longitude and time, period of revolution
  (L_e), A, (τ), B, (P), C
  Equatorial crossing longitude is to be expressed in degrees; time in hours. minutes seconds; period in minutes
- Specify latitude and longitude of observer, radius of earth
  (λ_o), D, (L_o), E, (R), f, a
  Latitude and longitude is to be expressed in degrees, radius in kilometers
- Enter satellite's height and inclination
  (h), f, b, (ψ), f, c
  Height is to be expressed in kilometers, inclination in degrees
- Press R/S to run

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Engineer's newsletter

Noninteger powers yield gracefully to theory

For 10 years it has been a lot of tedious, grinding work **to calculate the output signal amplitudes and phases to be expected whenever multiple inputs are applied to a nonlinear noninteger power-law device,** whether a varactor diode or any other solid-state device with a depletion-layer capacitance.

Now two researchers at the University of Queensland in St. Lucia, Queensland, Australia, have succeeded in reducing the problem to a calculation from known mathematical functions. Gary B. Price and Peter J. Khan of the Department of Electrical Engineering developed a mathematical theory from a varactor multiplier problem they ran into and have come up with a procedure that has "general applications in the analysis of nonlinear phenomena," to quote them. For detailed information, write Price and Khan at the university. Alternatively, a short summary of their ideas is given in the January Proceedings of the Institute of Electrical and Electronics Engineers.

Make and keep your own microcomputer

"Come on down to the microcomputer workshop," say the people at Intel Corp. of Santa Clara, Calif. Given during the day or evening for the next six months at locations throughout the country and with work at the introductory, intermediate, and advanced levels, **the hands-on sessions are based on the 8080 central processing unit and the enhanced 8085.** Further information on the details of the schedule is available from Judy Corson at (408) 987-8003.

Torque-tuning made as easy as 1–2–3

These days, few practicing electrical engineers are well trained in **the ins and outs of fractional horsepower motors, gear motors, and motor controls.** But "use of these components is constantly on the upswing," says Royal J. Bodine of the Bodine Electric Co. So, to help designers make knowledgeable decisions early in the design cycle, his company has printed a fourth edition of its 210-page handbook on such matters. With 19 chapters, 14 appendixes, a glossary, diagrams, and an index, it's probably all you will ever need to know about the subject if you are not actually working in the field. It's available for $3.50 in the U. S. or $4.50 elsewhere, from the company at 2500 W. Bradley Pl., Chicago, Ill. 60618.

The who, what, when, where, and why of broadcasting

Would-be buyers and would-be sellers of transmitters, receivers, and all other radio and television broadcasting equipment are brought together from around the world in the listings of the Directory of World Broadcasting. **The names and addresses of companies, their chief products, governmental authorities, and broadcasting stations for every country from Afghanistan to Zambia** are included. The cross-indexed 210-page volume is available from B. S. O. Publications, P. O. Box 1, 41 High St., Wivenhoe, Colchester 0079EA, UK.

Harvey J. Hindin

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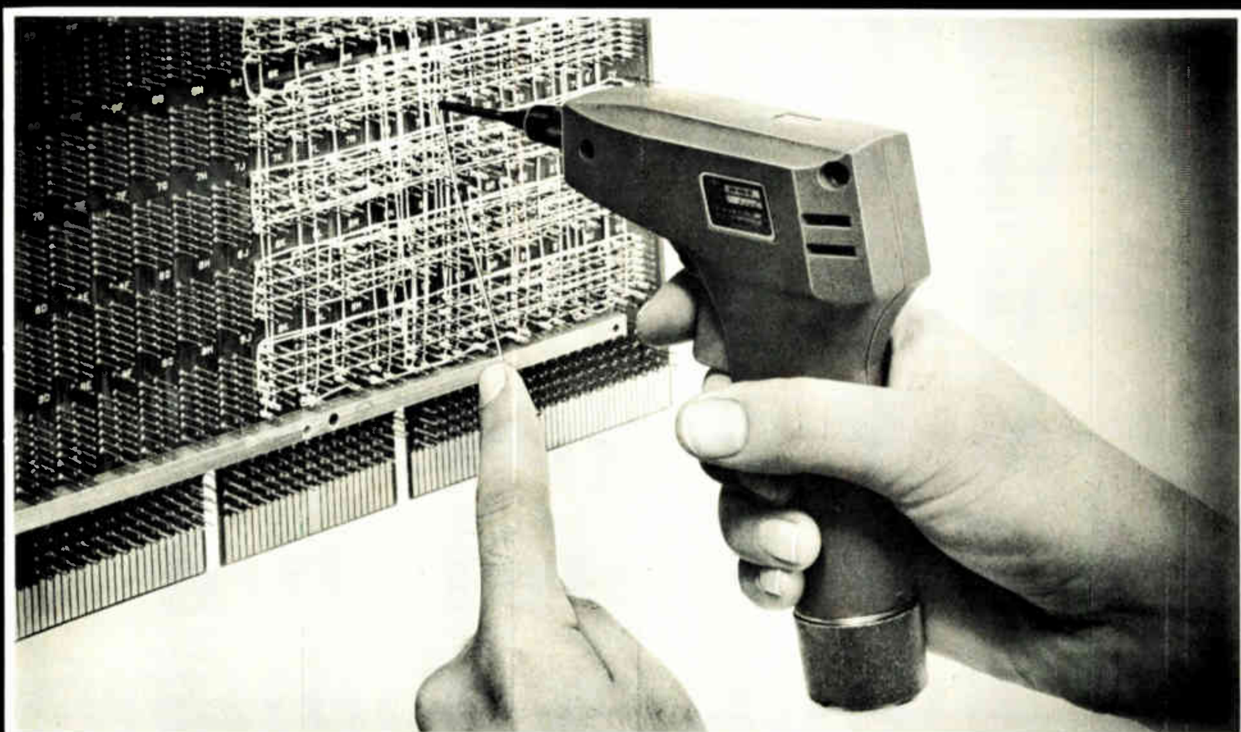

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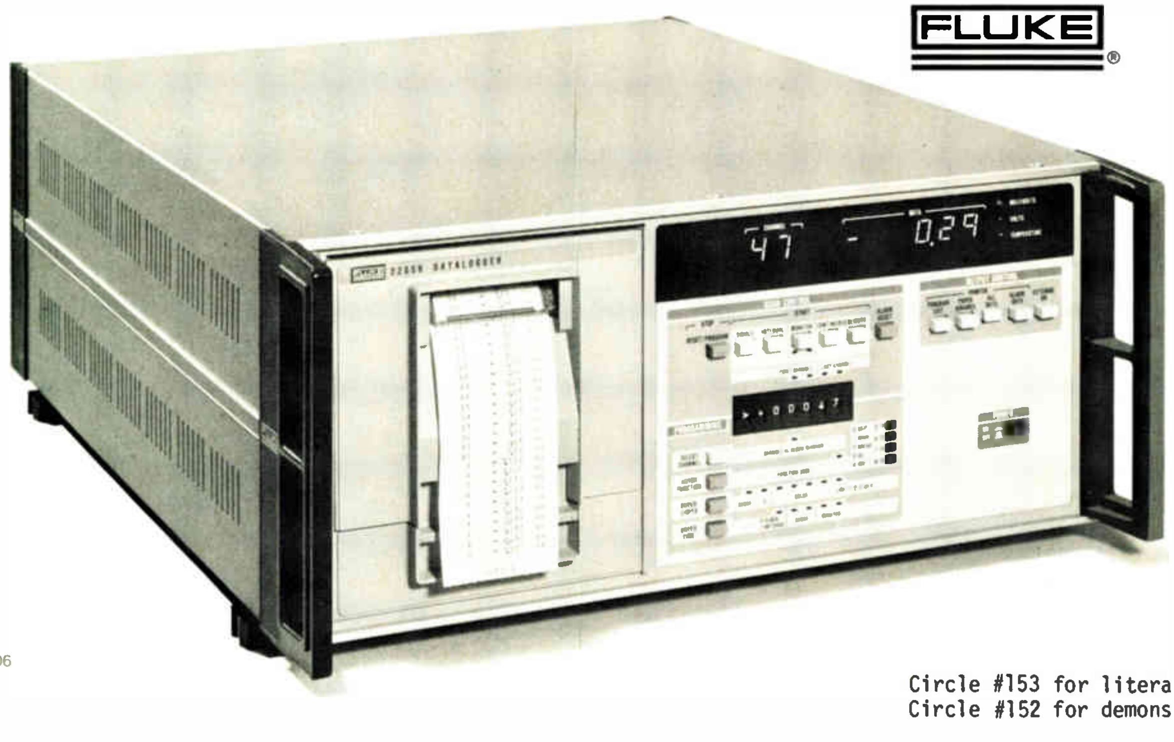

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Circle #153 for literature
Circle #152 for demonstration

Modem modules fill custom needs

2,400-b/s unit is built from one transmitter and two receiver modules to which terminal designers add circuitry for dc control signals

by Larry Waller, Los Angeles bureau manager

Since data modems tie so closely into the booming telecommunications equipment business, among others, it might be expected that a standard product line to fill numerous needs would be already on the scene. To the contrary, most terminal and other equipment manufacturers still go the custom-built route, primarily producing multichip hybrid affairs, packaged on boards.

Designers now have another choice, however, with the emergence of a synchronous 2,400-bit-per-second three-module modem from Rockwell International Corp. "Our R24 modem essentially integrates all the custom options into one standard product," says Donald R. Gibson, product marketing manager for telecommunications at Rockwell Microelectronics Devices, Anaheim, Calif.

Ripe. "The performance standards of modems have been mature for some time," he adds. But shrinking board modems down to three packages to increase the density and decrease the required power entails designing with a higher content of large-scale integrated devices.

Rockwell itself has been building custom modems for some time with logic chips fabricated with its p-channel metal-oxide-semiconductor process. This experience in custom modems gave it an understanding of what a standard line should do. "Before," explains Gibson, "we made them fit into a specific space," after a designer of terminals, for example, had completed everything else. "It seems the last thing people would worry about was the power supply and the modem."

Rockwell's new modem is a single standard product, but it comes in three modules—one for the transmitter and two for the receiver—which can be easily integrated into almost any design, even to the extent of being put on different boards. It can meet a wide variety of functional requirements with a small amount of external circuitry, needed mainly to apply dc control signals to the modules.

In each of the two receiver modules, all receiving and decision-making functions are implemented in two LSI devices, while in the transmitter module all transmitting tasks are done by one chip. Discrete integrated circuits perform filtering, conversion detection, and other functions. One receiver module measures 2.75 by 2.75 inches with 15 pins; the second is 2.75 in. by 3.50 in. with 31 pins; and the transmitter is 2.75 by 2.75 in. with 39 pins. All three stand 0.5 in. high and together take up less than 25 in.^{2} In contrast, a 2,400-b/s custom board made by Rockwell covers about 50 in.^{2}

With a minimum of interface circuitry, the R24 modem can be configured to operate either on dedicated unconditioned telephone lines or over a nationwide switched tele-

New products

phone network. Possible operating modes, says Gibson, are half-duplex with the switched network or a two-wire private line and full-duplex using a four-wire line. The 2,400-b/s modem is compatible with specifications of either the Bell 201 data sets for U. S. transmission standards or can conform to those of the CCITT recommendation V.26 for the rest of the world.

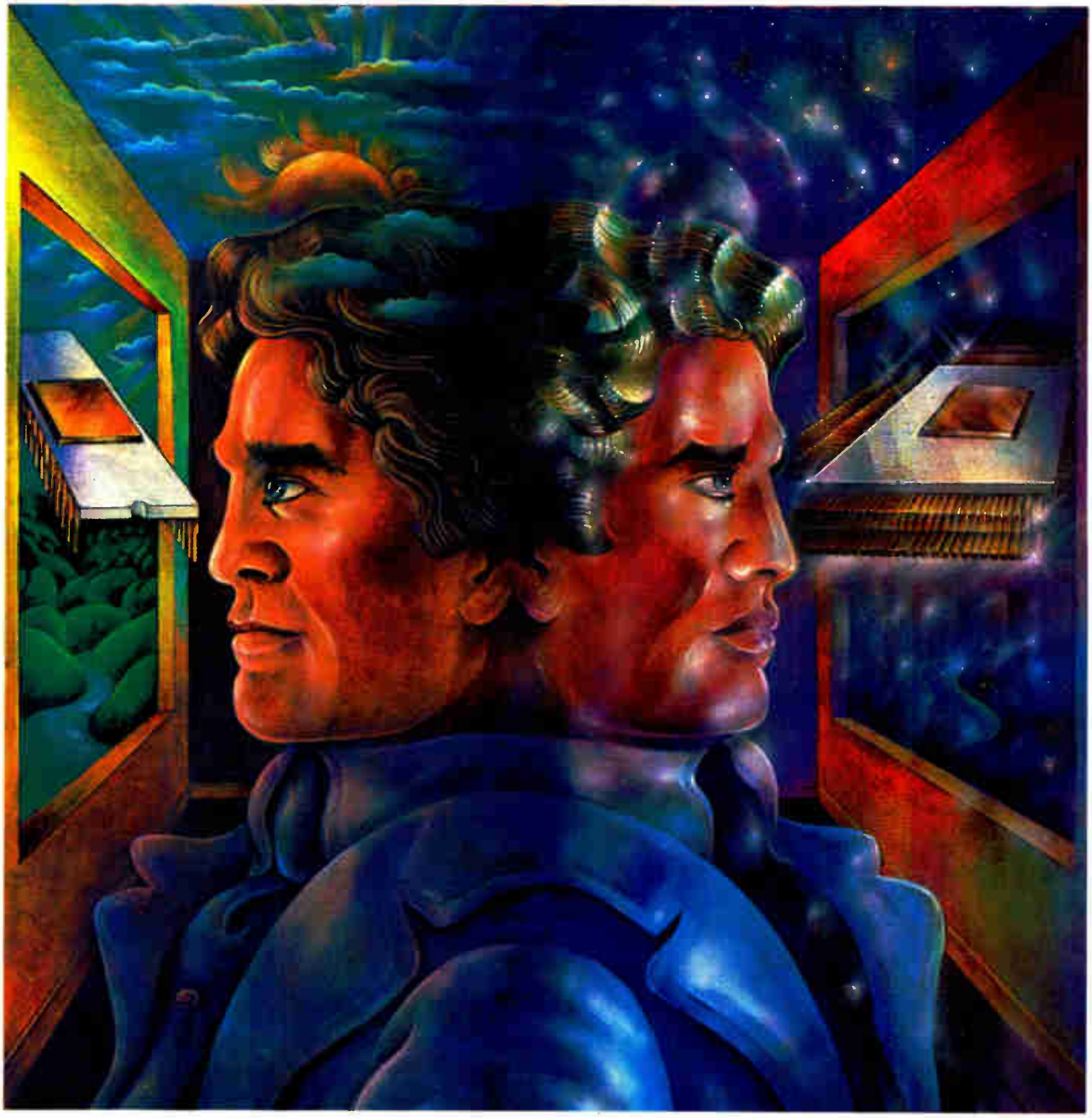
The modem uses differential phase-shift-keyed modulation. When it operates at 2,400 b/s, it employs four phases; for 1,200-b/s operation, it switches to two. In both cases, the modem works at a carrier frequency of 1,800 Hz ±1 Hz with a signaling rate of 1,200 bauds ±0.01%. The transmitted spectrum is spread over the band from 600 Hz to 3 kHz. The transmitting power level can be set between 0 and −43 dBm.

Maximum power dissipation of the R24 is 3 W. The power comes from three supplies: 100 mA at +5 V, 75 mA at +12 V, and 125 mA at −12 V. All three supplies must be regulated to within ±5%. The modem will work from 0° to 60°C and can be stored from −40° to +80°C. It can withstand exposure to a relative humidity of 90% at 50°C for 250 hours. Its altitude range is from 0 to 10,000 feet.

Each module is encased in a plastic package for plugging into standard connectors or wave-soldering onto a printed-circuit board. Pin spacing is on 100-mil centers. For the convenience of designers who wish to try out different test configurations, the R24 modules also come on an optional prefabricated evaluation board for an extra $50.

Rockwell is supplying prototypes, gradually building to full production by June. The present $550 price will come down then, but final pricing has not been set, says Gibson. Also, the simplicity and low price are expected to open up new applications, with energy management and process control having the most potential.

Rockwell International Corp., Microelectronic Devices, Telecom Subsystem Marketing, P. O. Box 3669, Anaheim, Calif. 92803. Phone (714) 632-5535 [338]



If you can't decide between an LSI & VLSI tester,

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You probably don't think you need a true 120-pin test system right now. Few companies do. But you will. Maybe sooner than you think. And, in the meantime, why spend all that money for a mere dedicated tester that won't meet your long term testing needs.

The Sentry VIII with its 120 fully programmable I/O pins will meet today's LSI requirements, and be ready to take on your VLSI testing later. But, let's take a look at some of the things the Sentry VIII can do for you right now.

Testing complex devices? The Sentry VIII will routinely perform precise characterization of microprocessors, peripheral chips, bit slices, RAMs, ROMs, shift registers, UARTs and digital hybrids in technologies such as NMOS, PMOS, CMOS, SOS, ECL, TTL, and I^2L.

Multiple pass testing? Chances are, you're occasionally forced to do some multiple pass testing of complex multi-pin devices. Well, the Sentry VIII can eliminate that extra pass. It has the ability to change any pin or timing assignment (input, output or format) on the fly. That can represent a tremendous improvement in throughput and can save as much as 50% of your testing time.

Still testing devices one at a time? By multiplexing the 120 fully programmable I/O pins on the Sentry VIII you can test two, even three, LSI devices simultaneously. Another 50% to 60% savings in test time.

And you can save even more. To provide lower operating costs, the Sentry VIII features multi-task (foreground/background) software for simultaneous compiling, editing and testing; a CPU that provides 50 to 200% faster throughput; a sequence processor to handle high complexity devices; and a pattern processor to tackle the largest memories.

Still don't think you're ready for a true 120-pin tester? Maybe you'd better think again.

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FAIRCHILD

Circle 155 on reader service card

Intel rams bipolar memory makers

Company's latest static H-MOS read/write memories—a 1-K RAM and a 4-K unit—beat bipolar devices in speed as well as power

by Raymond P. Capece, Solid State Editor

Ever since it introduced the 2102 1-K random-access memory in 1972, Intel Corp. has been chasing the speed of bipolar RAMs with its metal-oxide-semiconductor designs. Now, the Santa Clara, Calif., company, whose H-MOS process already leads the MOS makers' pack with the fastest 1-K and 4-K statics—the 45-ns 2115A and the 55-ns 2147—is offering the 2115H and 2147H that, with guaranteed access times of 20 and 35 ns, respectively outperform their bipolar counterparts.

The 1-K-by-1-bit 2115H, like earlier 2115 designs, is pin-compatible with Fairchild Camera and Instrument Corp.'s 93415A, the industry-standard 1-K bipolar RAM. But as the table shows, the 2115-3 MOS counterpart of the 30-ns Fairchild part offers the same speed while dissipating less power. The big news is the 2115H-1, which at about the same power as the 93415A offers a maximum access time of 20 ns—marking the first time that an MOS memory has had a rated access time lower than that of the bipolar device it aims at replacing.

The H-MOS II process scales channel lengths to 2 μm and gate oxide thicknesses to 400 Å, thus reducing parasitic capacitances and boosting drive currents with no increase in power consumption. Gate delays approach 400 ps, and power-delay products 0.5 pJ. Depletion-mode transistor loads are used in Intel's six-transistor static cells, each of which occupies an area of 3 mil².

The 2115H, available in four versions—20, 25, and 35 ns at power dissipations of 656 mW, and 30 ns at 525 mW—is surely a blow to bipolar RAM makers, who have concentrated most of their effort on reducing the power dissipation of their parts. "Now they not only have to cut power," says Barry Cox, marketing manager for Intel's Aloha, Ore. memory-components division, "they'll have to work on the speed as well."

Fairchild's most recent enhancement of its 1-K and 4-K bipolar RAMs has indeed been a power reduction. The 93L415 (also offered by Signetics Corp. as the 82L510) and 93L471 cut power by about a third, but at a sacrifice in speed: the parts are only available with 45-ns access times.

COMPARISON OF 1,024-BY-1-BIT RAMs

Parameter	Bipolar	MOS	
	(93415A)	(2115H-1)	(2115H-3)
Maximum address-access time (ns)	30	20	30
Maximum power dissipation (mW)	814	656	525
Output sink current (mA)	16		
Package	Standard 16-pin		

Sources: Intel and Fairchild

Already, one semiconductor manufacturer has clearly acknowledged the MOS encroachment on bipolar territory: National Semiconductor Corp. has scrapped plans to supply the 93415 and will instead concentrate on emitter-coupled-logic RAMs, which will have access times of 10 ns or better. But Frank Barone, director of National's bipolar memories division, which makes RAMs and programmable read-only memories, concedes that not even ECL is secure: "Actually, the only bipolar memory area that's safe right now is fusible-link PROMs."

Intel's 2147H is a faster version of the 55-ns part the company introduced in mid-1977. The 4,096-by-1-bit device will be available in two versions: the 2147H-2 with a maximum access time of 35 ns, and the 2147H-3 at 45 ns. Both versions dissipate a maximum of 945 mW but power down to a standby level of 158 mW within one cycle after the chip is deselected. That reduction is not available in Fairchild's 93471, which dissipates 893 mW, and is especially advantageous in large memory systems where most RAM chips are idle; the savings in power consumption, according to Intel, can be as large as 85%.

Samples of both the 2115H and the 2147H are available now. Availability of the 1-K devices through distributors will begin in April, while the 4-K parts can be had in May. Pricing of both parts is available upon request.

Intel Corp. 3065 Bowers Ave., Santa Clara, Calif. 94301 [339]

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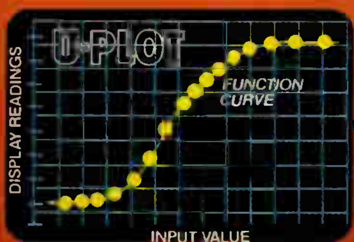

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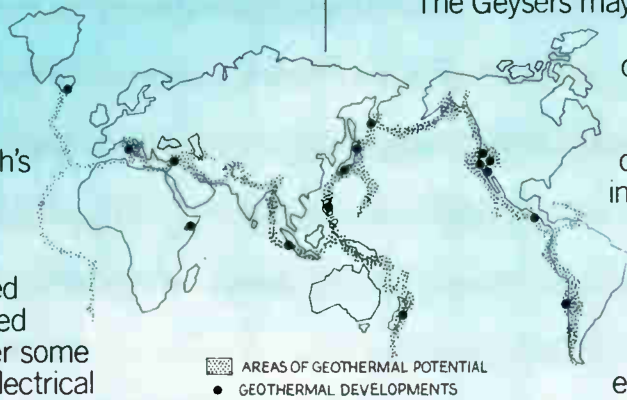
In northern California, the natural heat of the earth is being harnessed to serve the energy needs of man. Natural steam, heated by the molten rock below the earth's crust, is being tapped, extracted and piped to power some of the electrical generators that help light up San Francisco, 90 miles to the south.



The place is called The Geysers, and it's part of a pioneering effort by Union Oil Company of California to make geothermal energy a practical alternative to expensive imported oil.

The Geysers may be an unorthodox power source, but it has one thing in common with every other branch of the energy industries: the need to maintain good, reliable communications, no matter how remote or primitive the site.

At The Geysers, as in many places around the world, the solution to that problem is Motorola communications.

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THE EARTH, THE SEA AND THE SUN.

systems and subsystems, among which are pagers that tell a man he's wanted on the phone; closed-circuit video monitoring systems; and alarm and control systems that not only tell when something is going wrong, but also when everything is working right.

In the North Sea, a Motorola microwave system will provide a data and voice-communication link that will help one person control six unmanned oil-production platforms. He'll be able to check pressures and flow rates, regulate meters, pumps and motors, all by touching a few buttons.

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Motorola has made the apparently impossible happen by taking radio communication underground into deep-shaft coal mines.

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Motorola's preeminence in energy-industry communications is as much a matter of people as of technology. We made an early and total commitment to solving energy-industry communications problems, not merely as suppliers but as participants.

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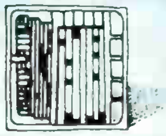

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Data acquisition

LSI-11 users reap bounty of boards

Latest series of I/O cards featuring popular compatibility are priced from $250 to $495

The harvest continues in input/output boards compatible with the LSI-11 and LSI-11/2 microcomputers. As a follow-up to the introduction of two boards last month [*Electronics*, Feb. 15, p. 170], Adac Corp. now has five more readied for market. Included in this array are: a general-purpose timer card (1601/GPT), a 16-input multiple-interrupt card (1616/MIC), optical pulse input (1604/OPI) and pulse output controller (1604/POC) cards, and a transistor-transistor-logic digital card (1620TTL). Each board is a dual-width size—8.5 by 5 in.—and is fully compatible with Digital Equipment Corp.'s microcomputer series: the LSI-11, LSI-11/2 and PDP-11/03.

The general-purpose timer card is software-programmable to operate at one of seven clock frequencies: 1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz (these are crystal-controlled), a user's external clock input, or an event line of 50/60 Hz. The 1601/GPT has five modes of operation: single-count, recurring-count, system monitor, watchdog timer, or timer. Each can be selected by software or by wire jumpers. "The watchdog feature is especially useful if the software 'hiccups'," says Richard B. Plummer, chief engineer. "If there's a sudden power surge or high noise gets into the system, the system can be rebooted and reinitialized automatically." The 1601/GPT will sell for $495 in quantities of one to four.

The 1616/MIC extends the interrupt capability of the DEC microcomputer series within the LSI-11 bus ("Q" bus) architecture. The multiple interrupt card accepts inputs from up to 16 external devices, passing them through a priority encoder before requesting an interrupt on the LSI bus. Priority is given on the basis of a predetermined order. Provision on the card for optical coupling, if used, gives a throughput time of 50 μs. In small quantities, the card sells for $450.

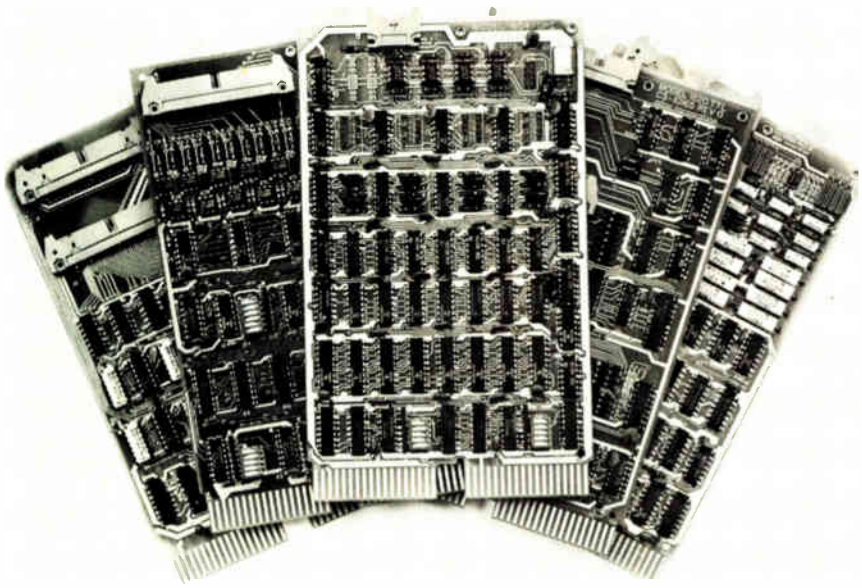
The 1604/OPI can count input pulses from up to four different sources and has four 16-bit counter circuits that operate independently. Double buffering allows present-state or last-full-count readings to be taken. If the optical coupling option is selected, the board will operate at 10 kHz; if not, operation is at 20 MHz. Particularly well suited for rotation/pulse applications, the 1604/OPI sells for $250 (two channels) or $395 (four channels) in small quantities.

A companion card for the pulse input card, the 1604/POC pulse output controller card has up to four pulse output channels, which can be customer-configured. (Pulse and up/down control configuration is also possible.) Two input lines with noise filters can function as limit switches or in other sensing capacities. Pulse width and spacing ranges are from 10μs to 10 ms, with the range selectable by wire-wrapped jumpers and the adjustment made by potentiometers. The price for the two-channel model is $250; the four-channel one is $395 (in small quantities).

The 1620 TTL digital card is designed to work with Adac's direct-memory-access card (the 1620 DMA) and has a 16-bit latched input data register, as well as control circuitry. Price is $350 in quantities of 1 to 4.

Delivery of all boards is 30 days after receipt of order.

Adac Corp., 70 Tower Office Park, Woburn, Mass. 01801. Phone (617) 935-6668 [381]



Precision v-f converters eschew enigmas

The correct answer to the riddle, "When is a guaranteed spec not a guaranteed spec?" is quite frequently, "When it is not 25°C." Since an engineer who has based his design on parameters that turn out to be grossly temperature-dependent seldom finds this answer amusing, two high-precision voltage-to-frequency converters are being introduced that take specsmanship very seriously—the 10-kHz model 4731 and the 100-kHz model 4733.

Both hybrid units are characterized by guaranteed specifications

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Circle 162 on reader service card

over the operating range from −55° to +125°C and the subset range of −25° to 85°C. Over the wider range, the converters have a maximum full-scale nonlinearity of ±0.03%; in the narrower range, ±0.005%. Both units have a dynamic range of 100 dB, can handle positive, negative, and differential inputs, and are processed to MIL-STD-883 specifications.

The 4731's full-scale factor is stable to within ±50 ppm/°C over the broader temperature range and this specification is guaranteed for a cold start; typically, the cold temperature coefficient is on the order of 10 ppm/°C, and for the narrower range the guaranteed coefficient is 25 ppm/°C cold. Values for zero offset stability are ±100 μV/°C, broad range, and ±20 μV/°C, narrow range.

The 100-kHz 4733's full-scale factor stabilities, given in the same manner as for the 4731, are 50 ppm/°C, 15 ppm/°C, and 30 ppm/°C, respectively. Zero offset stability is the same as that for the 4731.

In singles, the 4731 is priced at $125, the 33 at $135. Fully processed to MIL-STD-833 with burn-in and temperature cycling, the respective prices rise to $165 and $175. All units are available from stock.

Teledyne Philbrick, Allied Drive at Rte. 128, Dedham, Mass. 02026. Phone Wah Fea Ng (last name pronounced Eng) at (617) 329-1600 [384]

D-a hybrid performs fast 4-bit conversions

The DAC-HU4B is a high-speed hybrid digital-to-analog converter whose full-scale, 24-mA output settles to within 0.1% of final value in just 25 ns. Although specifically designed as half of a two-stage, 8-bit a-d converter system—it readily mates with Datel's ADC-HU3B—the 4-bit converter can also be used in high-speed, intensity-modulated cathode-ray-tube displays.

The converter's 15 input lines, compatible with 10,000 series emitter-coupled logic, each control a fast current switch, so the unit responds to what is called "thermometer scale" inputs—inputs that increase sequentially from all 0s to all 1s. Alternatively, input lines can be tied together in an 8-4-2-1 grouping so that it will work with complementary-binary-coded inputs.

Maximum integral and differential linearity errors are within 0.1% of full scale. The differential linearity temperature coefficient is ±15 ppm/°C, as is that for gain.

The converter is housed in a 32-pin package and is offered in versions that operate over military, industrial, or commercial temperature ranges. In quantities of 1 to 24, the DAC-HU4B ranges in price from $125 to $209.

Datel Systems Inc., 11 Cabot Blvd., Mansfield, Mass. 02048. Phone Eugene Murphy at (617) 828-8000 [383]

S-d converter digitizes flux-gate compass output

Conversion of gyro flux-gate compass data into digital form has proven difficult because such compasses deliver 800-Hz outputs that consist primarily of a series of spikes. Furthermore, this latitude-dependent output voltage can vary from 50 to 370 mV.

Now, by means of a proprietary design, the model 1625 synchro-to-digital converter can be used to compensate for dynamic voltage variations and extract signal data from the output spikes. The converter provides 10-bit resolution and is accurate to within 124 arc minutes.

A transformer isolates the reference from the input, and separate analog and digital grounds are provided to minimize ground-loop problems. The 3.125-by-2.625-by-0.42-in. converter needs +5- and +15-V sources and meets the reliability specifications of MIL-STD-883B. It is priced at $500.

Transmagnetics Inc., 210 Adams Blvd., Farmingdale, N. Y. 11735. Phone Fred Haber at (516) 293-3100 [385]

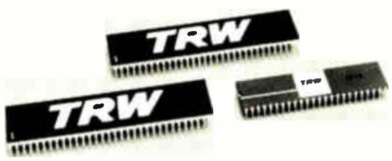

Digital signal processing is here

TRW takes another step in digital signal processing

NOW, A COMPLETE FAMILY OF MULTIPLIER / ACCUMULATORS

We've developed an entire family of high-performance monolithic multipliers with built-in accumulators. They're TTL devices in VLSI technology and are just the ticket for many applications of digital signal processing, including low-cost optical character recognition.

Because they displace a whole rack of sophisticated hardware, our multiplier/accumulators (MAC) can help small computer systems perform highly complex correlation functions. You can use these correlation functions to recognize the written word, the printed word and visual images of all sorts. Once recognized and captured, you can subject the characters to various computer manipulations, and even translate them into other languages.



You simply use one of our multiplier/accumulators to multiply a digitized image against a repertoire of anticipated patterns stored in memory. A high degree of correlation results in a numerically high product; a lack of correlation reduces the product value. You set upper and lower thresholds on the accumulated result and you vary the thresholds according to your required degree of flexibility or security.

Because our devices feature on-chip accumulators that store the sum of many previous comparisons, you simply read out the accumulator's contents and compare its value to the numerical thresholds stored inside the CPU. This makes optical character recognition go or no-go—what used to be an extremely complex and costly correlation process is now a piece of cake.

We have 16-, 12- and 8-bit number-crunching chips that grind pairs of numbers together to produce millions of products each second. Our TDC-1010J, for instance, is a 16x16-bit chip that produces a 32-bit product and a 35-bit sum in a mere 115 nsec. (It's designed to operate in a continuous, pipeline mode so the accumulator's operation is transparent—once the first product is generated, it produces more products and adds them to the previous sum.) The TDC-1010J can accumulate products up to 35-bits in length. It accepts data in either unsigned magnitude or two's complement notation. It offers three individual device pins for controlling the chip's three-state outputs, and of course, all its signals are conventional TTL levels. It's packaged in a standard, 64-pin DIP and uses just 3½ watts.

In addition to the 16-bit MAC, our second generation family also includes a new, 12-bit multiplier/accumulator—the TDC-1009J. It operates twice as fast as the original TDC-1003J—just 95 nsec for a complete 24-bit product plus a 27-bit accumulated sum. Like the 16-bit MAC, the TDC-1009J is packaged in a standard, 64-pin DIP. It uses just 2½ watts.

TDC-1008J is the designation of our 8-bit multiplier/accumulator. It generates a 16-bit product and a 19-bit accumulated sum in a snappy 70 nsec, uses only 1.2 watts and is housed in a standard, 48-pin DIP.

For increased flexibility, all our new MACs feature control pins that defeat the accumulators and allow them to operate as conventional, n-by-n-bit multipliers. Even more than that, they all feature on-chip input and output registers; their accumulators have the ability to subtract as well as add; they provide a useful pre-load function that lets you set the accumulator contents to any value and they all run on +5 volts only. All our multiplier/accumulators are radiation hard.

The pricing on our family of multiplier/accumulators is very low: in hundreds, the TDC-1010J is priced at $205; the TDC-1009J is $120 and the TDC-1008J, just $70.

Like all TRW LSI Products, our multiplier/accumulators are available from stock through Hamilton/Avnet. For more information, send in the coupon or talk to one of our digital signal processing experts at 213/535-1831.

TRW LSI Products
An Electronic Components Division of TRW Inc.
P. O. Box 1125
Redondo Beach, CA 90278

Please send data sheets on the new family of multiplier/accumulators.

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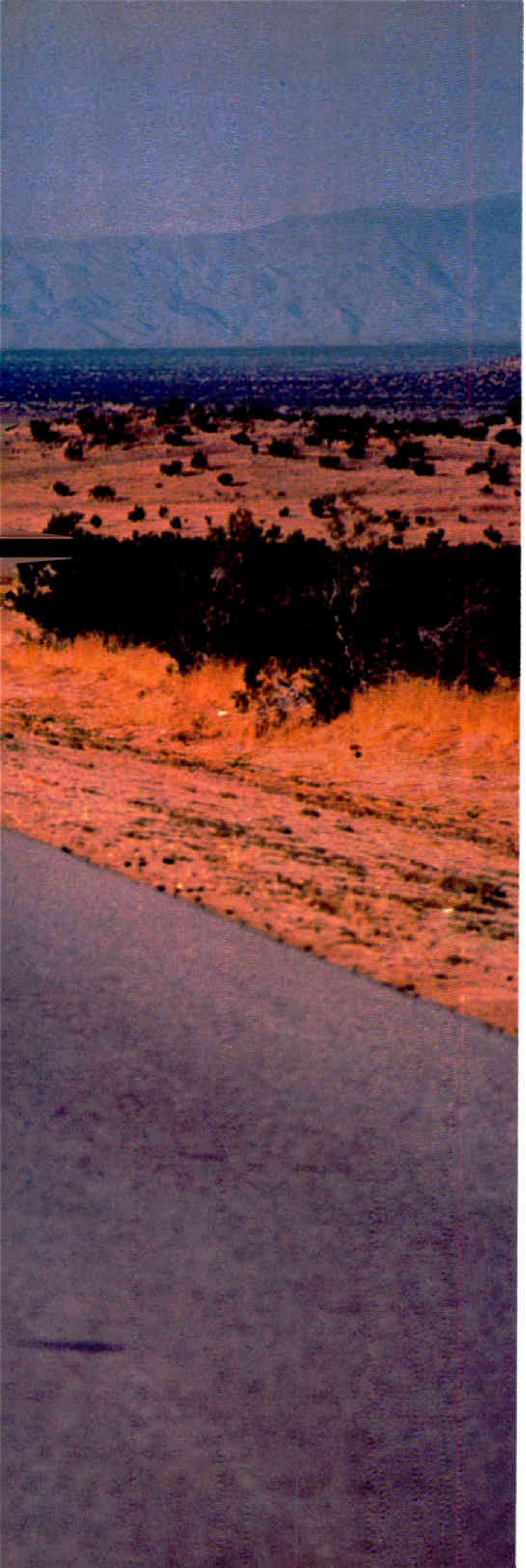
We know exactly what's happening to the
OEM computer inside this truck's 140° interior.
Absolutely nothing.



Industrial

IC's output goes up in smoke

Chip contains most of the circuitry needed to form a photoelectric smoke detector

Smoke-detector circuitry has been around for some time now. Most engineers would probably have little difficulty designing a reasonably reliable photoelectric unit with a handful of discrete components, but putting the works into a single 16-pin dual in-line package is another matter. Cherry Semiconductor has done it; its model CS-179 is an integrated circuit requiring a minimum of external components to form a complete detector: a 9-V battery, an infrared-emitting diode, a photodiode, a horn, a potentiometer, and a few timing resistors and capacitors.

A timer in the CS-179 generates a 22-ms pulse every 15 s. This pulse simultaneously energizes the IRED and the amplifier, detector, and logic circuitry connected to the photodiode. If the optical attenuation between the IRED and the photodiode rises above the threshold set by an external potentiometer, the logic circuitry interprets the event as a smoke signal.

To minimize the probability of false alarms, two consecutive clock pulses must yield smoke signals before the CS-179 will go into its alarm state. In this state it both energizes the horn and increases the timer frequency from 1/15 Hz to 1 Hz. The second change is desirable because the alarm will not stop until the unit receives two consecutive no-smoke signals, reducing the time required to respond to the absence of smoke from 30 s to 2 s.

In its normal monitoring state, the CS-179 checks the battery voltage under load during every IRED pulse. When it determines that the battery needs replacing, it sends a 22-ms pulse to the horn every 30 s.

As with all products from Cherry Semiconductor, the CS-179 is the outgrowth of a large-quantity custom order. As it is strictly a large-quantity item (50,000 pieces and up), its price is determined by negotiation.

Cherry Semiconductor Corp., 99 Bald Hill Rd., Cranston, R. I. 02920. Phone (401) 463-6000 [373]

Single kilowatt-kilovar monitor replaces two units

Digital displays not only look better than analog ones, they can save panel space, too. This solid-state digital kilowatt-kilovar monitor combines both readouts in one unit with no moving parts.

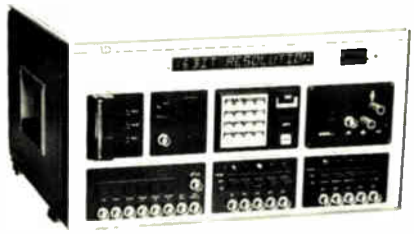
Also available as a single-function display, the unit has a solid-state multiplier with linearity adjustable to within 0.1% and 0.43-in.-high

light-emitting diodes. Six models match single-phase and balanced or unbalanced three-phase lines carrying up to 300 kilowatts/kilovars. Maximum error is 0.5% of range, ±1 digit, from 47 to 60 Hz. Size is 4.74 by 3.25 by 5.50 in., and requires a 4.125 by 3.125 in. cutout.

Electro Industries, 316 Westbury Ave., Carle Place, N. Y. 11514. Phone (516) 621-6652 [377]

Pulse sequencer is programmable in English

Intended for use as an industrial or laboratory counter-timer, the Z8253A Computer Stimulator gen-



erates five transistor-transistor-logic–level digital pulses and one stepped analog wave form in any of 999 sequences. Individual pulse durations range fron 2 μs to 9,999 seconds, with four-digit resolution and 0.02% uncertainty.

To store a pulse pattern, the user keys in the desired sequence, period, duration, and amplitude of the pulses after each parameter appears on the unit's 16-character orange neon alphanumeric display. Each sequence need not be fixed: any parameter may be tagged, so that it follows any other pulse parameter automatically.

The Z8253A uses a Z80A microprocessor and 8 kilobits of random-access memory expandable to 32 kilobits, connected via a modified S-100 bus. The unit measures 8.75 by 17 by 12.75 in. Prices start at $4,990.

Micro Data Collection, P. O. Box 115, Novato, Calif. 94947. Phone (415) 883-9255 [373]

Switching servo amplifiers control motors precisely

Accuracy is the name of the game in incremental-motion systems. When used with appropriate feedback elements, either of two new switching servo amplifiers can give designers the precision they need.

The 40- and 75-V models each have continuous current ratings that are adjustable from 0 to 7 A. Peak current, which is limited automatically for 0.5 second and then folded back, is also adjustable, over a range of 0 to 20 A.

The switching frequency of these pulse-width-modulated amplifiers is 5 kHz regardless of load; frequency

ANNOUNCING THE OPTIMATE EXPERIMENTER'S KIT FROM AMP.

With this one kit you can put your mind in high gear with all the elements necessary to design as many as six different workable data links ranging from 1 kilo-bit to 1 mega-bit—all TTL or CMOS compatible.

The AMP Optimate Experimenter's Kit gets you out of the parts procurement business and back into the design business. Cables...emitters...detectors... connectors...crimper...instructions—everything is in the kit. There's nothing extra to buy.

You actually design and experiment with active devices made by Motorola Semiconductor Products, Inc. as well as with a whole array of AMP fiber optic connectors, cable and p.c. boards. The kit includes instructions for making as many as six TTL- and CMOS-compatible low frequency data links operational to 45 meters or more. Components are also suitable for use with lower loss cables (not supplied.)

Active devices in the kit
These include pin photo diodes, phototransistors, photodarlington transistors and infrared emitting diodes. Components include numerous integrated circuits serving as amplifiers, buffers, inverters, receivers and comparators.

Six transmitter and six receiver PC boards are part of the package. Transmitter circuits range from one-kilobit to one-megabit capacity. Receivers can be one, two or four-channel, one kilobit to one-megabit capacity.

Complete set of AMP Optimate connectors
The heart of the kit—and the primary reason you can now design commercially feasible, repeatable fiber optic data links—is the AMP Optimate connector. It makes terminations simple, quick and accurate. Optimate connectors use a resilient material which insures centering to a degree previously unattainable. Precise, accurate polishing—once difficult—is fast, troublefree and easy, thanks to a simple polishing bushing that comes with the kit.

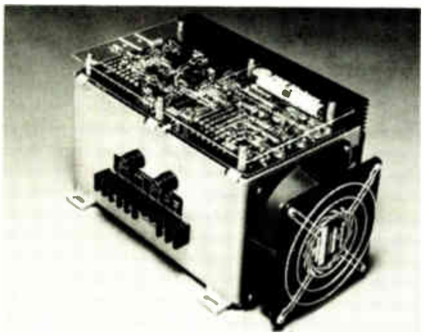
Just three steps to a precise fit
That's all it takes with the Optimate connectors in the kit:
1. Assemble with a few parts
2. A simple proven crimp
3. Then accurate polishing

Connectors for every problem
You will soon see that the AMP Optimate connector solves three basic problems quite neatly and precisely:
- Coupling of the light source to the fiber optic cable
- Splicing cables
- Coupling the fiber optic cable to the photodetector.

Innovative crimping tool
Every kit includes this unique tool which enables you to attach cable to connector accurately and permanently. The AMP crimping tool will not release until a certified, repeatable crimp is made.

Complete instructions
Nothing is left to chance. You get an experimenter's guide on system characteristics and complete instructions for constructing and experimenting with up to six fiber optic systems.

ORDER NOW. SEE BACK PAGE.



response at rated power is dc to 1 kHz. Four-quadrant operation allows acceleration and deceleration in either direction. Both models include fault-protection circuitry to prevent damage from short circuits, from logic-supply failures, and from thermal overloads.

Each unit is 7 in. wide, 11.125 in. long, and 6.06 in. high. The power transformer is optional.

PMI Motors, 5 Aerial Way, Syosset, N. Y. 11791. Phone Hans Waagen at (516) 938-8000 [374]

Circular plastic pot measures shaft angles

The model AP 55 Anglyzer is a 360°, infinite-resolution plastic potentiometer with 0.1% uncertainty, which makes it suitable for many shaft-position readout applications that now use absolute encoders.

The unit's solid-state switching system combines dual internal signals into a single analog output ramp to eliminate the dead zone inherent in conventional pots. Elastomer damping of the metal multi-finger wipers prevents contact bouncing at speeds up to 6,000 rpm.

The AP 55 needs a ±10- to 15-V dc supply (available from the firm, as is a 3 ¾-digit display) and a stabilized reference for direct dc analog

output. A 3.5-V reference gives a full-scale readout that corresponds to 360°.

Total system price for the Anglyzer, power supply, and digital display is under $500 in single quantities.

Waters Manufacturing Inc., Longfellow Center, Wayland, Mass. 01778. Phone (617) 891-1227 [375]

Interface routes traffic in data-acquisition systems

The SL111 ASCII interface supervises data flow between computers, peripherals, and analog scanners in industrial data-acquisition systems. Designed for half-duplex serial ASCII transmissions, the interface can service up to 160 analog channels.

Communication between the SL111 and any processor or terminal with an RS-232-C port or 20-mA current loop is implemented by a simple protocol. A single-letter prefix to each byte identifies it as a command to read or write data or to start a channel measurement, as a system "busy" signal, or as actual data.

The interface contains an 8748 microprocessor and optical isolators to minimize ground loops. Included in nonvolatile memory are a command-error analysis routine and a self-diagnostic subroutine that checks internal circuitry and external transmission lines. Internal jumpers allow selection of baud rate (110, 300, 600, 1,200, 2,400, 4,800 or 9,600 bauds), parity (odd, even, or none), and word length (5 to 8 bits). The unit price is $698.

The San Diego Instrument Laboratory, 7969 Engineer Rd., San Diego, Calif. 92111. Phone (714) 292-0646 [376]

Demand recorder alerts users to need for load shedding

Designed to reduce electrical demand charges, the model DTR-400 demand recorder incorporates an alarm that is activated when a thumbwheel-selected threshold is exceeded, enabling users to shed load.

The recorder works on a sliding demand interval that permits checking of any demand period. It accepts inputs from standard utility pulse initiators at switch-selectable rates of 0.1, 0.2, and 0.4 or 1, 2, and 4 contact closures per second and provides a chart récording of maximum demand during the selected interval. The DTR-400 will record for up to 756 hours on a single roll of paper.

The model DTR-400 is priced at $795 and delivery is from stock to six weeks.

North Hills Electronics Inc., Glen Cove, N. Y. 11542. Phone Herb Marx at (516) 671-5700 [378]

Computers & peripherals

Pocket terminal sells for $495

Priced for small businesses, data-entry device provides up to 8 kilobytes of storage

Key to optimizing the use of data-processing equipment for inventory control is increased point-of-entry automation. One growingly popular means to accomplish this is the use of hand-held data-entry terminals that can be carried through the aisles of, say, a retail outlet. But at a price of $1,000 per unit, only large retailers and distributors have been able to afford them.

Aimed at the potentially large market that smaller stores can provide, Norand Corp.'s Sprint 100 is priced at just $495 in single quantities—a price that includes 4 kilobytes of random-access storage. According to George Chadima, chairman of Norand, it took some special design effort to make the pocket-sized, 13-oz, Sprint's price correspondingly small.

"To meet our design goals," he states, "we had to use a combination of microprocessor and memory chips that provided the appropriate blend of complementary-metal-oxide-semiconductor and n-channel MOS technologies." While Chadima admits that the 2½-by-1⅛-by-7-in. terminal's brain is a custom-designed 8-bit microcomputer, he will reveal no details about its memory other than to say it is made up of volatile units that are not charge-coupled devices. An undisclosed amount of read-only memory holds the microprocessor's operating program while random-access storage is expandable up to 8 kilobytes.

Acoustic-coupler circuitry is integrated into the Sprint so that, with a separately attached acoustic muff, orders can be transmitted over telephone lines to a central facility, such as a warehouse. A touch-sensitive panel, rather than a standard keyboard is used to enter data, which is displayed on a 12-character, light-emitting-diode display. Deliveries of the unit, with a full one-year warranty, have just begun, according to Chadima.

Norand Corp., 550 2nd St. S. E., Cedar Rapids, Iowa 52401. Phone (319) 366-7611 [361]

Processor gets boost in storage and software

Users of the 1500 dispersed processor can now enhance their systems operation by adding more diskette storage, increased user memory, and new communications software.

The 1500 now supports two diskette drive subsystems for a total of 1 megabyte of on-line storage. Each subsystem houses two disk drives and uses single-density diskettes for storage. A complete 1-megabyte system sells for $8,975; upgrading 1500 processors to this capacity costs $3,675.

Memory capacity has been increased from 32 kilobytes to 60 kilobytes. The 60-K 1500 sells for $7,900. The older 32-kilobyte machine can be upgraded by using the field-installed memory-upgrade kit that sells for $1,920, with an installation fee of $125. The 1500 processor with 60-K memory and 1 megabyte of storage sells for $10,895.

The new 2780 emulator software is able to work with both the 32- and 60-kilobyte versions of the 1500. The CC278015 emulates IBM's 2780 data-communications terminal using the 1500's integral synchronous communications interface. The software permits communications to take place coincidentally with other operations. The CC278015 is included with all new 1500s; present users may license the emulator for a one-time fee of $20.

The price of new 1500s also includes operating system and other software.

Datapoint Corp., Attn: Product Marketing (M71), 9725 Datapoint Dr., San Antonio, Texas 78284 [364]

Intelligent disk subsystems are compatible with Massbus

Designed as its first end-user products, two disk storage subsystems from Microcomputer Systems Corp. are plug-compatible with Digital Equipment Corp.'s Massbus I/O controller. Designated the MSC-05 and MSC-06, the units can replace DEC's RP-04, RP-05, and RP-06 disk drives with their storage capacities of 88 megabytes (the 04 and 05) and 176 megabytes (the 06). According to the manufacturer, the new subsystems are more efficient because their architecture centralizes data-transfer management, making the system into an "intelligent peripheral."

Although the architecture of the MSC differs from that of DEC's disk drive, its performance remains similar because both are based on a stan-

dard industrial disk drive. The subsystems can be added to an installation without changing its existing operating system. In hybrid systems that employ both types of drives, disk packs from one type of drive may be interchanged with those from the other type storage unit.

In addition, a dual-port option on the MSC-05 and -06 subsystems gives two different computers access to the disk drive at the same time. Another feature of the MSC system is that it is upward-compatible; it will be able to accommodate upgrading of the operating-system software to achieve higher throughout.

A set of supplementary in-line and off-line diagnostics has been included on the MSC-05/−06 to test the microprocessor control logic and any other drive of the MSC subsystem. Any attached drive may be diagnosed while the others continue normal operations.

According to company president James Toreson, MSC plans to market their replacement product at 15% to 25% less than the DEC-supplied subsystem, depending on the quantity of drives ordered.

Microcomputer Systems Corp., 432 Lakeside, Sunnyvale, Calif. 94086. Phone Jim Toreson (408) 733-4200 [363]

Firmware increases speed of intelligent printing system

Three firmware packages permit the IPS-7000 intelligent printing systems to produce up to 160 dot-matrix characters per second. The 7001, 8, and 9 firmware packages

THE BEST-KEPT SECRET IN OPTO-ISOLATORS.

70% of all industry standard opto-isolator types can be found at Litronix.

Not too many folks know Litronix has one of the broadest lines of opto-isolators around. We've told you about our LED displays and lamps, photodetectors, IR diodes, et al. But we haven't said much about our opto-isolators. Until now.

We have almost two dozen single channel couplers. Two dual couplers. And our exclusive quad coupler. Listed below are the more popular types.

Our pricing is aggressive. And there's our tech support. We'll duplicate exotic test conditions, do parameter guarantees, and even help you trouble shoot.

So say the secret word (Litronix), and cash in on the best opto-couplers around. Litronix, 19000 Homestead Road, Cupertino, CA 95014. (408) 257-7910.

Part Number	Current Transfer Ratio %	Voltage	Description	No. of Channels
IL-1	20	2500	Photo Transistor	1
IL-5	50	2500	"	1
IL-15	6	1500	"	1
IL-74	12.5	1500	"	1
4N25	20	2500	"	1
4N26	20	1500	"	1
4N27	10	1500	"	1
4N28	10	500	"	1

Part Number	Current Transfer Ratio %	Voltage	Description	No. of Channels
4N32	500	2500	Photo Darlington	1
4N32A	500	2500	"	1
4N33	500	1500	"	1
IL-100	1000	2500	High Speed 75 nS	1
IL-101	1000	1500	High Speed 200 nS	1
ILCT6	20	1500	Photo Transistor	2
ILD74	12.5	1500	"	2
ILQ74	12.5	1500	"	4

litronix

AN AFFILIATE OF SIEMENS

THE LIGHTS FANTASTIC

Circle 179 on reader service card

New products

combine a 160 c/s matrix printer and an 8-bit microcomputer complete with random-access and programmable read-only memory.

The IPS-7001 prints 64 ASCII characters in a five-by-seven-dot matrix format; the IPS-7008 and IPS-7009 each print a 96-character set in a nine-by-seven-dot matrix. The 7001 and 7008 each offer a 500-character buffer; the 7009, a 3,500-character circular buffer. The 7008 and 7009 include a programmable vertical-format control, which allows printing of either six or eight lines per inch.

The 7001 is priced between $2,130 and $2,250 depending on quantity; price ranges for the 7008 and 7009 are $2,180 to $2, 325 and $2,230 to $2,410, respectively.

Dataroyal Inc., Main Dunstable Road, Nashua, N. H. 03060 [365]

Floppy-disk supports different drives and formats

The DFDC11 is an LSI-11–compatible, floppy-disk controller. It can support a variety of floppy-disk drives and data formats including 5.25-in. mini and 8-in. regular disk drives, either single- or double-headed and single- or double-density, in both IBM and non-IBM formats.

The DFDC11 is self-contained on a single, dual-width, Q-bus–compatible card that includes the drive controller, direct-memory access controller, and 256-word programmable read-only memory. Designed to compete with the DEC RX02/RXV21 system, it is said to offer up to 25% more storage in any given drive configuration. However, since it does not emulate the DEC machines, special software handlers are needed.

In single quantities, the DFDC controller sells for $1,200. The DZ-HS system software sells for $200, and the DZ-H software, for systems already equipped with another RT-11 device only, sells for $100. Delivery time is 30 to 45 days.

Andromeda Systems Inc., 14701 Arminta St. #J, Panorama City, Calif. 91402 [366]

See for yourself why design engineers specify more CTS cermet resistor networks than any other make.

There is one large overriding reason. Reliability!

Each CTS SIP and DIP network is 100% value and tolerance tested before shipment. And, with more than 1 billion element hours of extended load life testing, CTS resistors have exhibited a failure rate of only 0.00047%/1,000 hours @ a 95% confidence level.

CTS networks are built reliable...using top quality materials, precision screening equipment, proprietary cermet formulations and computer controlled lasers for fine tolerance adjustment. Terminals are anchor-locked into the substrate for maximum mechanical and electrical reliability.

CTS has been a leader in custom designed circuits for over 15 years. Ask us about customizing your special network requirements or choose from 400 standard part numbers available off the shelf from authorized CTS distributors.

For the utmost in cermet network reliability, quality and availability, you can't choose a better network source than CTS. Send for your free samples and resistor network catalog today. Write CTS of Berne, Inc., 406 Parr Road, Berne, Indiana 46711. Telephone: (219) 589-8220.

CTS CORPORATION
ELKHART, INDIANA

A world leader in cermet and variable resistor technology.

Microcomputers & systems

MicroNOVAs get redesigned

Latest generation stays competitive by increasing performance, saving space

To stay alive in the microprocessor world, manufacturers have to keep packaging more functions and greater performance into less and less space. Hot from the drawing board, two microcomputer families being introduced by Data General represent a redesign of the microNOVA family, from chip through board to box. Fully compatible with earlier microNOVA architectures, the MP/100 is being billed as low-cost and highly functional, and the MP/200 is said to offer three times the performance of the current microNOVA.

A new single-chip 16-bit microprocessor, the MN602 is an enhancement and replacement for the MN601 [*Electronics*, March 4, 1976, p. 133], the chip set currently implemented in the microNOVA series. Housed in a 40-pin package, the new processor is an n-channel metal-oxide-semiconductor device that implements the full 16-bit NOVA architecture. It has a real-time clock, hardware stack, frame pointer, hardware multiplication and division, 16-level priority interrupts, and standard as well as high-speed (2-megabyte/s throughput) data channels. Up to 128 kilobytes of memory can be supported by the 602, and an asynchronous memory bus allows programmable read-only memory, erasable PROM, and random-access memory to be addressed. On board is an integral power monitor and industry-standard voltages of ±5 and +12 V are supported.

"The MN602 is the basis for the entire MP/100 family," says Edward Zander, manager for microproducts marketing. The 100 is a system processor unit on a 7.5-by-9.5-in. board; in residence are the MN602, a full asynchronous interface with full modem control, automatic program load, an external real-time clock, and a soft control panel which allows any ASCII console to supervise program execution.

The MP/200 family offers higher performance than current microNOVA products: a 16-bit addition can be done in 0.8 μs and a full 16-bit multiplication in 4.9 μs. Direct memory access is at 3.7 megabytes/s. The 200 uses an extended NOVA instruction set with low byte, store byte, sign multiply, and sign divide. "The MP/200's CPU," observes Zander, "has architecture very similar to the MN602, but it's implemented with a bipolar process."

Being offered with these processors are three new memory boards: 32-kilobyte and 64-kilobyte RAM boards, and a 16-kilobyte PROM board. Offered with the MP/200 is an optional Basic Control Board with automatic program loading, asynchronous interface with full modem, virtual console, automatic start after power failure, real-time clock, and the soft control panel. The MP/100 and MP/200 interface with all microNOVA peripherals.

The 100 and 200 can be housed in a newly designed, eight-slot chassis; a single card holds an entire power supply and can be supplied with the chassis. Four-slot cages for use by other equipment manufacturers and a new half-bay cabinet are also being offered.

The new microNOVAs will be sold in chip, board, and package form. Some representative prices follow. The model 100-602, which is the official designation for the MN602 chip, is priced at $56.10 each for 100 or more. The model 8521-F two-board MP/100 computer includes an asynchronous interface, automatic program loading, 32 kilobytes of memory, and sockets for 32 kilobytes of E-PROM; it sells for $1,500 in unit quantity.

The 8671-D, a board-level MP/200 computer with asynchronous interface and 64 kilobytes of memory, is priced at $2,250 in singles. An MP/100 packaged system, the model 9062, with 64 kilo-

bytes of memory, an asynchronous interface, an eight-slot chassis, a power supply, a Dasher TP1 printer, a 10-megabyte hard-disk subsystem, and a half-bay cabinet goes for $14,600. Delivery takes 90 days.

Data General Corp., Route 9, Westboro, Mass. 01581. Phone (617) 366-8911 [391]

Portable analyzer tests in-circuit microprocessors

The AQ8080Z microprocessor analyzer is a cost-effective alternative to in-circuit emulators and cathode-ray-tube logic analyzers. Being compact, self-contained, and portable, it is excellent for product development, production testing, and field service. Different clip-on probes make the AQ8080Z compatible with all 8080, 8085, and Z80 systems.

These probe clips are fully buffered and attach directly to the microprocessor in the system under test.

The user may examine or modify all memory locations, input/output ports, and internal registers, including the program counter and stack pointer. Data may be transferred to or from any I/O port to help isolate faults in peripheral devices. Programs may be single-stepped, by machine cycle or instruction, or the execution speed can be continuously adjusted to 4,000 steps per second.

Debugging features of the AQ8080Z include breakpoint and real-time monitor functions that can be set to respond to read or write operations for memory references, I/O references, or memory references coincident with external events. The microprocessor address lines are monitored during program execution, and the AQ8080Z can halt execution when a specified breakpoint address occurs. Alternatively, activity at the specified address can be monitored to count the number of times the address was accessed or check the data associated with the address and the status of the specific machine cycle (real-time monitor).

If a Z80 is under scrutiny, the AQ8080Z can be used to examine its background or alternate register set. A light-emitting diode reminds the user which set he has chosen. The instrument can also examine the Z80's index registers, IX and IY.

The AQ8080Z microprocessor analyzer, complete with clip-on PRB80/Z80 probe, sells for $2,795.

AQ Systems Inc., 1736 Front St., Yorktown Heights, N. Y. 10598. Phone (914) 962-4264 [399]

Intel supports 8086 with hardware and software

A microprocessor without development tools is like a fish out of water—dead. So it's no surprise that Intel Corp. has followed the mid-1978 introduction of its 16-bit 8086 with a comprehensive package of languages and utilities and an in-circuit emulator.

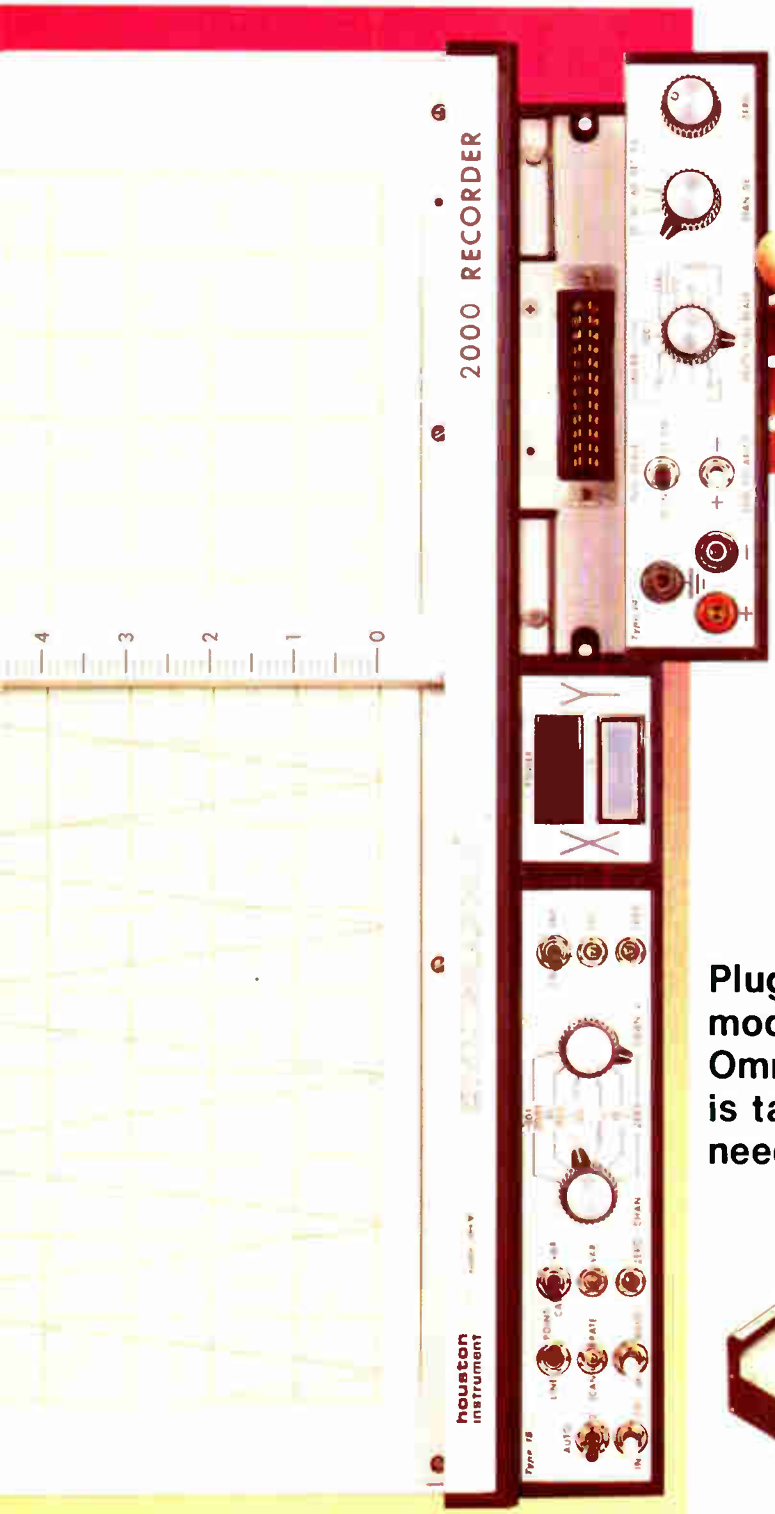
With the MDS-311 software package, programs can be designed in the structured high-level language PL/M-86 or in ASM-86 assembly language. Also, using a program called CONV-86, 8080 or 8085 assembly code is converted into 8086 assembly code to feed ASM-86. The package thus allows the 8086 to be fully upward-compatible with its 8-bit predecessors.

Both the assembler and PL/M-86 compiler produce relocatable object modules, and MDS-311 contains relocation and linkage facilities—LOC-86 and LINK-86—for positioning and combining these modules. Alternatively, a QRL (quick relocate and link) device allows the designer to test an individual module before it is assimilated into a larger program.

Finally, MDS-311 provides a library manager and a converter for translating object code into hexadecimal symbolic-object code. The library manager lets programmers create, maintain, and store assembled or compiled programs, modules, or routines for later linking. The code converter translates absolute machine code into much more easily readable symbolic hexadecimal code.

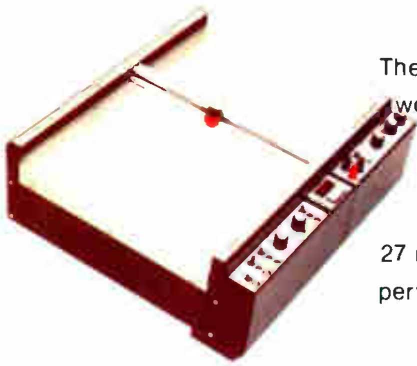
The in-circuit emulator, ICE-86,

When your applications change,



this recorder changes with them

Plug in your choice of modules and the Omnigraphic® Model 2000 is tailored to your need



The Omnigraphic Model 2000 is the world's best known most versatile X-Y recorder. The basic building block is a rugged die cast metal mainframe. A choice of 27 modules enables the recorder to perform in virtually any application.

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has both hardware and software components. The hardware connects an Intellec development system with the user's prototype circuitry by means of a cable and a buffer box, replacing the user's 8086 for debugging and testing. The software consists of Intellec debugging commands, which control the user's software to isolate problems.

In addition to cable, the ICE-86 hardware consists of the buffer box and three Multibus boards, containing circuits for program trace, control, and interface between the control central processing unit and buffer box.

With ICE-86, the user is allowed to make symbolic reference to PL/M statements, input/output ports, variables, procedures, memory address, and data. Moreover, ICE-86 allows command macroinstructions to be created. According to Steve Goodfellow, marketing manager for 8086 development support, "You can write a string of commands, even with conditional statements like IF and REPEAT. When you're done, you can give it a name, store it on disk, and access it whenever it's needed."

To accommodate the 8086's megabyte address range, user programs can be put on disk in the Intellec system and ICE-86 will take care of getting them. "ICE-86 will go out and get whatever page of memory your code is on," says Goodfellow. "Obviously this takes longer, but in a software debug environment, it's really effective."

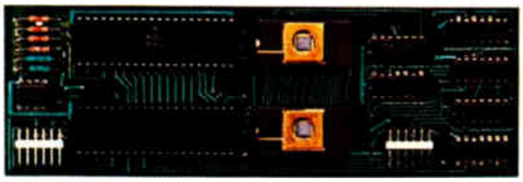
ICE-86 also features breakpoints and a trace routine that can both be started and stopped under program control. Trace memory stores up to 1,023 frames, each containing 20 addresses or data lines. ICE-86 software will automatically disassemble the results of a trace as well as program memory, converting binary object code into more readable assembly-language mnemonics.

Both products are available now. MDS-311 costs $3,400 and includes diskettes, manuals, and one year of updates. ICE-86 sells for $5,500.

Intel Corp., 3065 Bowers Ave., Santa Clara, Calif. 95051. Phone Carl Buck at (408) 987-6723 [393]

Once you compare our new 191 digital multimeter to ordinary 5½-digit DMMs, we think you'll readily agree that it outclasses its class. For good reason.

The 191 is a ±200,000-count DMM capable of 0.004% accuracy and 1μV/1mΩ sensitivity. It delivers unsurpassed accuracy, faster, because firmware in the 6802-based μcomputer has replaced slower, less precise analog circuitry.



Displayed data is updated at the fastest rate of digit change readable by the human eye—4 conversions per second. Settling time of 0.5 seconds is easily half that of the 191's nearest competitor.

The μP combines both charge-balance and single-slope conversion techniques. Every displayed reading is automatically corrected for zero and gain drift.

If you've ever had to contend with the frustration of potentiometer zeroing, you'll appreciate the 191's null function. Automatic arithmetical correction of residual error is standard. With a touch of the button you can buck out any in-range signal, large or small.

A year from now you'll own one or wish you did.

You don't need low-level noise either. So the 191 automatically suppresses it. The 191's non-linear digital filter is entirely free of dielectric absorption and leakage problems associated with analog techniques. On the 200mV and 200Ω ranges, the filter effectively attenuates noise by displaying a running average of the 8 previous readings. Yet it instantly displays input changes of 10 digits or more.

Another exclusive of the 191 is 2 and 4-terminal measurement from 1mΩ to 20MΩ across six ranges. Simply adding two more sense leads automatically enables Kelvin measurements. No changing input terminal links or even pushbutton settings.

And, finally, since μP design reduces component count, the 191 requires less servicing and calibration, increasing reliability and stability.

At $499 without plug-in ACV, the 191 is today's performance/value leader in 5½-digit DMMs. A year from now most people will agree.

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Circle #252 for literature

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Components

Triacs need little power

Cheap high-voltage switches can be driven directly by microprocessor output levels

With the market for microprocessor-based appliances exploding, the need for low-cost, low-power ac switching devices is also expanding rapidly. Unitrode Corp. is answering this need with the IB200 series of low-current triacs, designed to operate with microprocessor or optically coupled signals. "This triac can be driven directly from a logic source," says Carl L. Uretsky, market manager for appliance and control. The unit can control the current to such medium-power devices as lamps, solenoids, and relays.

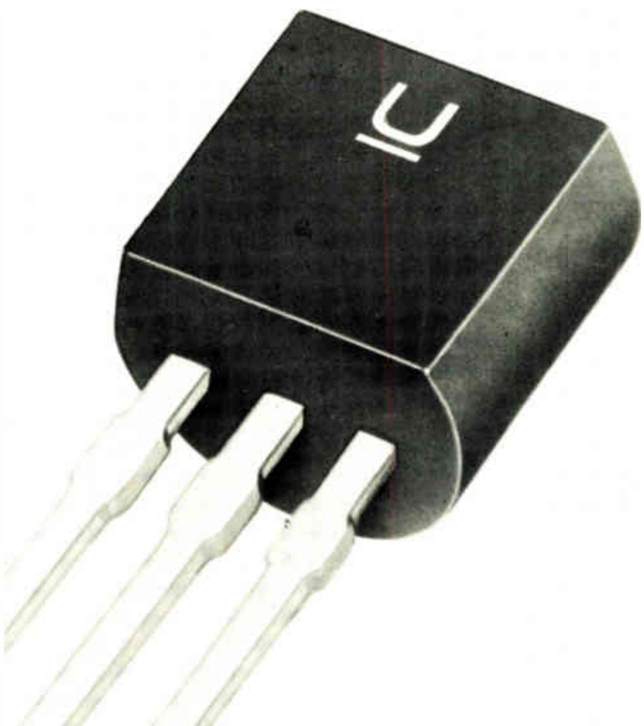
Units in the IB200 series are housed in plastic TO-92 packages and rated to handle a load current of 800 mA rms. The nonrepetitive surge rating is 8 A. Gate sensitivity is typically 2 mA (5 mA maximum) in the first and third quadrants and 10 mA maximum in the second and fourth.

The series comprises three units: the IB200, IB400, and IB600, with respective voltage ratings of 200, 400, and 600 V. These high voltage ratings are attributable in part to the mesa construction of the devices. "The mesa construction enables the triac to work at 750 V typically, and very reliably at 600 V," says Uretsky. The units have a maximum on-state voltage drop of 1.8 V.

The required gate-trigger voltage is a maximum of 2V for the first and third quadrants and 3 V for the second and fourth.

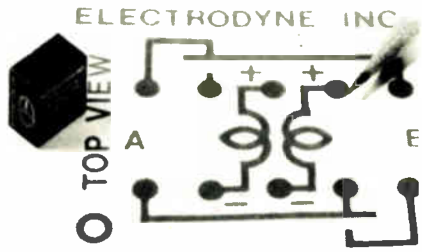
Uretsky expects the triacs, which can operate from −55° to +110°C, to be used in many nonmilitary areas, especially in appliance and automobile control. "The IB200 series has been designed to fill the gap between microprocessor controls and the power-output requirements of future industrial and commercial products." He says that present industrial applications are mainly in energy-management systems. Prices for the series in 10,000-piece quantities are: 24¢ for the IB200, 28¢ for the IB400, and 45¢ for the IB600. Delivery time is six to eight weeks.

Unitrode Corp., 580 Pleasant St., Watertown, Mass. 02172. Phone Joe Pappalardo at (617) 926-0404 [341]



Power switching relay spends only 6 μJ per latch

Series 15 magnetic latching relays interface directly with microprocessors to switch power devices such as lamps and solenoids. The most sensitive version in the dual-coil, double-pole, double-throw series consumes only 200 microjoules of energy in performing a single operation.



The relays provide 1,000 V rms isolation between the driving coils and the contacts, which are rated for up to 300 V dc at 1 A. Units within the series have 570-Ω coils for use with transistor-transistor logic or 1,850-Ω coils for complementary-metal-oxide-semiconductor circuitry.

The series 15 relays come in dual in-line packages with pins spaced on a 0.1-by-0.3-in. grid. The devices are small, too, with an overall height of only 0.420 in. In 1,000-piece quantities, they are priced at $4.50 each, and delivery time is four to six weeks.

Electrodyne Inc., 11200 S. E. 21st St., Milwaukie, Ore. 97222. Phone A. Sprando at (503) 654-0711 [343]

Optocouplers isolate high-speed logic to 7,500 V

Compatible with 5-V logic, the MOC5005 and MOC5006 optocouplers work at high speeds. The

5005 has turn-on times of 420 ns typical and 700 ns maximum; the 5006, 225 ns typical and 350 ns maximum. Both units provide peak isolation of 7,500 v.

The output of each UL-listed device, when operating at the specified speed, is driven low by a 16-mA input that turns on a gallium-arsenide infrared-emitting diode (IRED). The IRED is optically coupled to a high-speed integrated detector; when the diode goes off, the detector's output goes high.

The optocouplers work from a 5-v power supply from which they typically draw 2.5 mA when there is no input current and 4.0 mA when there is. Typical outputs are 0.35 v low and 4.75 v high.

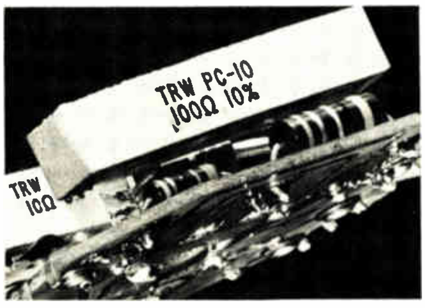
The MOC5005 and MOC5006 come in six-pin dual in-line packages and, in lots of 100 or more, are priced at $2.40 and $2.70 respectively. Delivery is from stock.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone Hank Schroeder at (602) 244-4556 [344]

Fireproof resistors fit printed-circuit boards

Designed for printed-circuit board mounting, the fireproof PC series meets EIA specification RS-344 for insulated, fixed, wirewound resistors. The resistors are wound on a glass-fiber core filled with nonflammable inorganic material and sealed in a ceramic case. They are available with 3-, 5-, 7-, or 10-W ratings.

Ranging in value from 1 to 400 Ω for 3-W units and to 1,200 Ω for 10-W units, resistors in the series have tolerances of ±5% and ±10%. Their standard temperature coeffi-



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cient is 400 ppm and dielectric strength is rated at 600 V ac. In 1,000-piece quantities resistors cost from 6.4 to 8.5c each and delivery time ranges from approximately four to six weeks.

TRW/IRC Resistors, P. O. Box 1860, Boone, N. C. 28607. Phone W. C. Robbins at (704) 264-8861 [345]

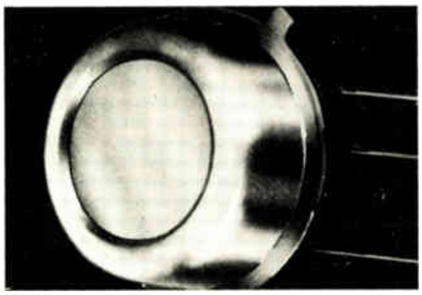
Detector senses radiation in infrared-to-soft-X-ray band

The model 400 is a pyroelectric infrared detector whose sensing element is a thin crystal wafer of lithium tantalate—a substance able to maintain uniform response for extended periods of time. The unit is housed in a TO-5-type package that can be supplied with windows of various materials; when used with a beryllium window, the unit can detect soft X rays.

For an input of 10.6-μm wavelength and a chopping frequency of 10 Hz, the sensor has a specific detectivity of 4.4×10^8 cm-Hz$^{1/2}$/W. Because the sensor has an input resistance greater than $5 \times 10^{12}\ \Omega$, it must be used with an external, impedance-converting circuit composed, for instance, of a junction field-effect transistor and a megohm-range resistor. The 400 has a voltage responsivity of 600 V/W at 10 Hz and its output rise time is 0.2 ms. Temperature coefficient is specified at +0.2%/°C.

In quantities of 100, the model 400 is priced at $15 and delivery is from stock.

Eltec Instruments Inc., P. O. Box 9610, Central Business Park, Daytona Beach, Fla. 32020. Phone Douglas Armstrong at (904) 252-8294 [346]



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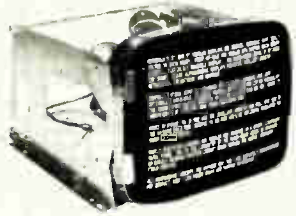
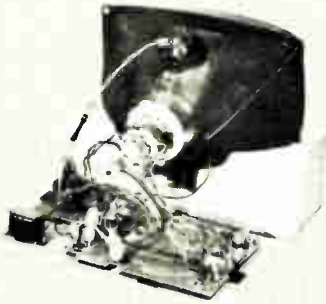
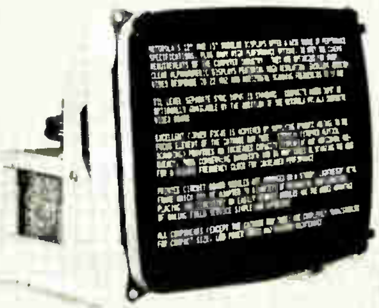


M1000/M2000 series 5-inch and 9-inch display modules. These highly reliable displays testify to the effectiveness of measured rather than calculated MTBF. Samples of every complete Motorola CRT display module are life-tested for a minimum of 10,000 hours at 55°C. Customers report some of our displays logging more than 40,000 hours and still going strong.



M3500 series 12-inch display modules in chassis or kit form (shown). Cost saving, plus no metal boundaries to inhibit your own layout.

MD3000 series 12-inch display modules. Between the MD3000 and M3500 series, you can have your 12-inch display in any of several ways: chassis or kit, separate sync TTL level, composite video or direct drive inputs, choice of standard EIA phosphors, choice of scan frequencies, with or without anti-reflective faceplate.



MD4000 series 15-inch display modules. Up to 3,440 upper and lower case characters in a 7 x 9 dot matrix. Every line is sharp . . . even in the corners. StepScan™ 22 MHz bandwidth and customer adjustable dynamic focus are standard in the MD3000 and MD4000 series. If looks on the screen are important—and when aren't they?—a Motorola display is what you want.

The M4408 15-inch module displays a full page horizontally (132 x 46) or vertically (96 x 66, shown). High character density and low cost, too—raster scan technique with standard TTL logic interface gives you economy twice: once in purchase price and again in design costs. A technology leader.

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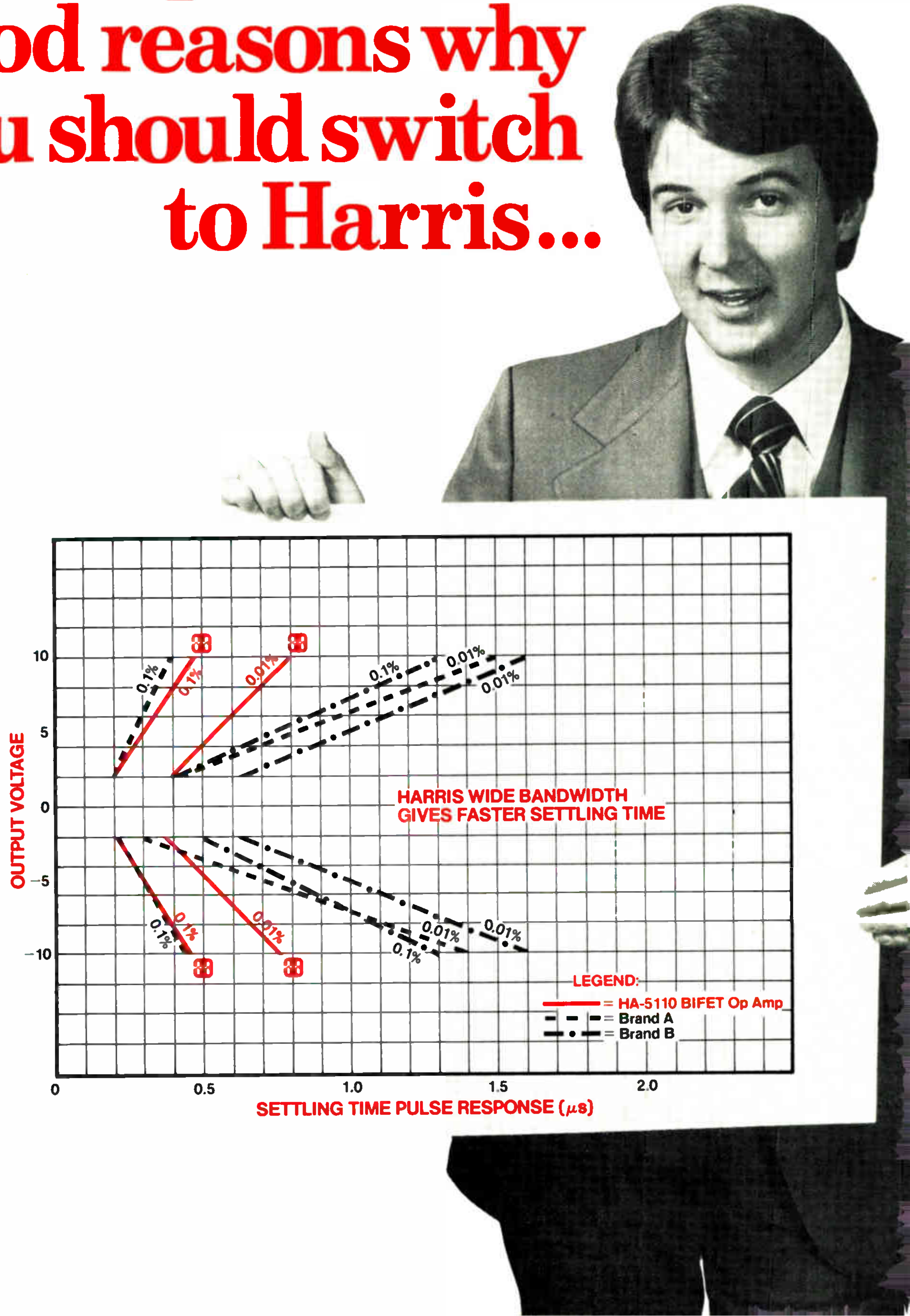

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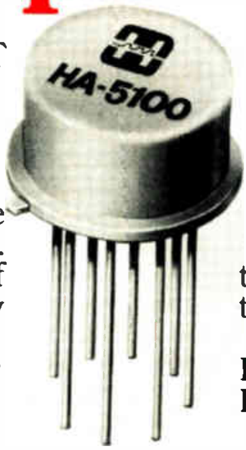
2. Faster settling time
3. More stable over temperature."



New Harris HA-5100 and HA-5110 BIFET Op Amps offer unmatched dynamic performance and accuracy at costs beginning at $3.50 each (100-piece quantities)!

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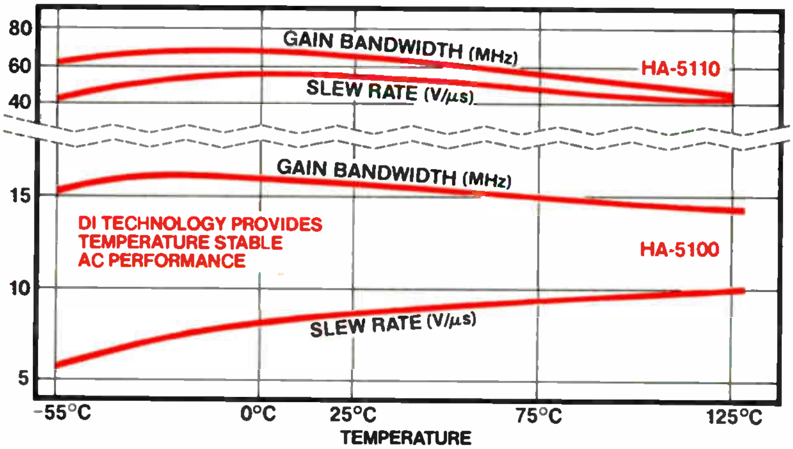
Or write: **Harris Semiconductor Products Division, Box 883, Melbourne, Florida 32901.**

HA-5100/5110 Ac Parameters/Temperature



Harris BIFET Op Amp Performance

PARAMETERS	TEMP	UNITS	5100-2 (−55° to +125°C)	5100-5 (0° to +75°C)	5105-5 (0° to +75°C)	5110-2 (−55° to +125°C)	5110-5 (0° to +75°C)	5115-5 (0° to +75°C)
V_{OFFSET} (MAX)	+25°C	mV	1.0	1.0	1.5	1.0	1.0	1.5
I_{BIAS} (MAX)	+25°C	pA	50	50	100	50	50	100
	FULL	nA	10	10	20	10	10	20
SLEW RATE (MIN)	+25°C	V/μs	8	8	6	40	40	35
G.B.W.	+25°C	MHz	18	18	8.5	60	60	80
SETTLING TIME[1]	+25°C	μs	1.7	1.7	2.0	0.85	0.85	1.0

[1]Settling Time to 0.1%, 10 V step.

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The new 200 Series sockets are here with all the reliability and performance that you've come to expect from Augat, but at a surprisingly low price.

These new sockets have been designed to meet or exceed all the requirements of the new military specification for dual-in-line sockets, MIL-S-83734.

The 200 Series features beryllium copper side-wipe contacts for maximum mechanical and electrical performance, as well as maximum IC lead-to-contact mating surface. Low-profile construction with end and side stackability means efficient use of board space. Standoffs molded into the insulator provide clearance for proper cleaning. A closed bottom eliminates solder wicking without the use of a wafer.

The Augat 200 Series is available in all popular sizes, from 8 through 40 pins. And they're available now—from all of Augat's worldwide distributor locations.

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Semiconductors

Chip decodes and drives four digits

Low-power C-MOS circuit comes in versions for LCDs and LED displays

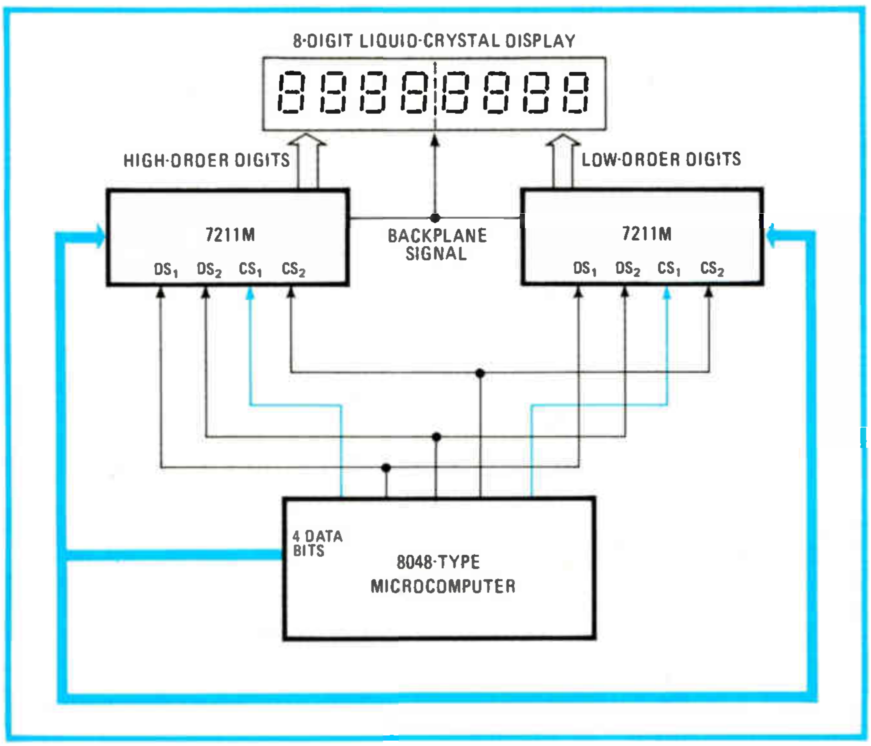
Designers of portable microprocessor-based instruments with liquid-crystal displays will now be able to decode binary display information directly from the data bus and drive four digits of LCD using only a single integrated circuit—Intersil's 7211M. One of a family of eight new devices, the 40-pin complementary-metal-oxide-semiconductor IC needs no external components for its backplane oscillator. What's more, it uses hardly any power—250 μW maximum from a 5-V supply.

According to its designer, Roger W. Fuller, the chip is designed to exploit the trend toward smart, portable instrumentation. "It's more important to limit the number of power-consuming parts in these kinds of instruments than in instruments tied to supply lines, because of their dependence on battery power," he explains. "That's why we decided to make a low-power chip that could drive four digits and needs no random logic to interface to a microprocessor."

If more than four digits are needed, a user can cascade two or more 7211s by connecting their backplane pins, thus keeping them synchronized while they drive the extra displays (see diagram).

The microprocessor chooses when to write a 4-bit word from its data bus into the 7211's input latch by pulling low the two chip-select pins, CS_1 and CS_2. This enables a second latching circuit, the 2-bit digit select, to lock in the position code. On a rising edge of either chip-select pin, a 7-bit output latch (one of four selected by the position code) sends its pattern to a 7-bit display driver. The pattern sent to the driver is different for different members of the C-MOS decoder/driver family.

Cascade. When more than four digits are needed, two or more 7211s may be cascaded by connecting their backplane pins, thus ensuring that they are synchronized.



For all members, the first 10 4-bit codes are displayed as the seven-segment numerals 0 through 9. An A version of the 7211M will decode the binary equivalents of decimals 10 through 15 as a dash, letters E, H, L, and P, and a blank. Units without the A suffix will decode them as the standard hexadecimal characters A through F.

In addition to the standard and A versions, Intersil also makes two versions for interfacing liquid-crystal displays for non-bus-oriented circuits. These units, which lack the M suffix, have the same output circuitry as the M units, but lack the input chip- and digit-select logic. The user instead matches the position of a character with its multiplexed 4-bit binary-coded-decimal input by controlling the four separate digit-select lines with external random logic.

The four additional units of the family differ from the first four only in that they are designed to drive light-emitting-diode displays instead of LCDs. The LED circuits carry the numerical designation 7212. Like the 7211, the 7212 operates from a single 5-V supply. However, when displaying all eights, it typically draws 200 mA, compared to a maximum of 50 μA for the 7211.

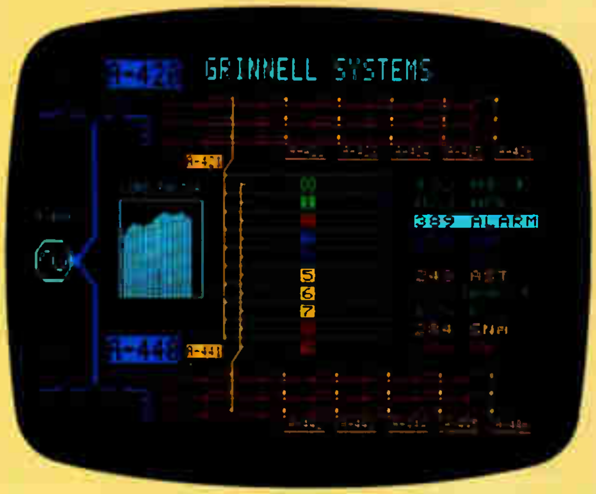
In quantities of 100 or more, the 7211 units with their built-in backplane oscillators sell for $5.60 each. The corresponding price for the 7212 devices is $3.45. The parts are all available now.

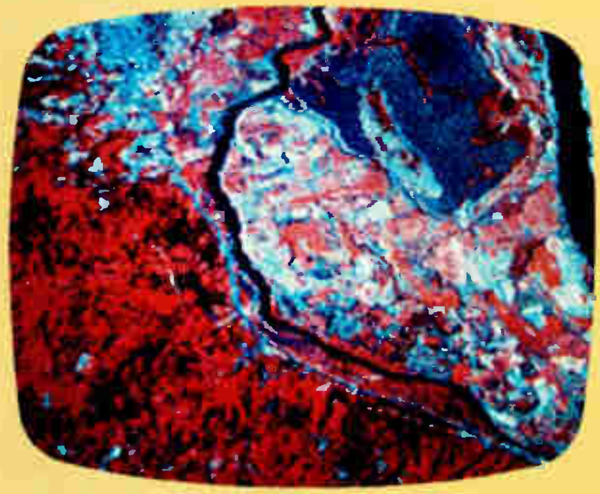
Intersil Inc., 10900 N. Tantau Ave., Cupertino, Calif. 95014. Phone (408) 996-5000 [411]

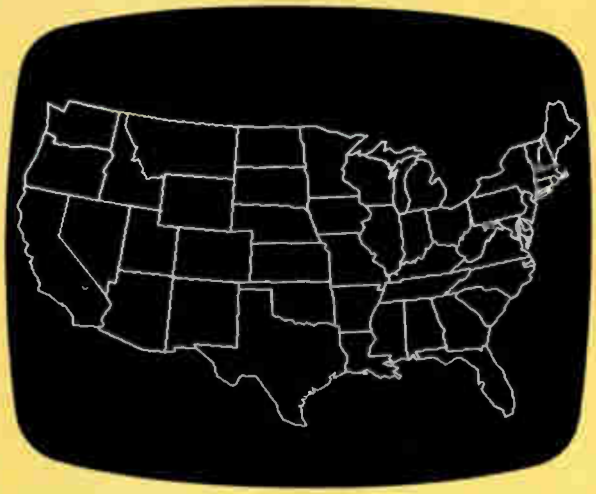
Op amp has 150-MHz gain-bandwidth product

Current-output digital-to-analog converters are always faster than their voltage-output equivalents, whose speed is limited by output operational amplifiers. Harris's latest operational amplifier should therefore be especially welcomed by makers of high-speed d-a (and a-d) converters. Designated the model

Grinnell has your display...







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GRINNELL SYSTEMS

2986 Scott Boulevard, Santa Clara, California 95050 (408) 988-2100

Circle 199 on reader service card

New products

HA-5190, the monolithic unit has a gain-bandwidth product of 150 MHz and a slew rate of 200 V/μs. Settling time to within 0.01% of final value is 100 ns for a 5-V step—a big plus for fast d-a conversion applications.

The op amp has an offset voltage of 5 mV and an input noise-voltage specification of 15 mV/Hz$^{1/2}$ at 1 kHz. In small quantities, the 5190 sells for $28.90. The 5195-5, which covers the 0°-to-75°C range, is $8.60.

Complementing the op amp is the HA-4950, a fast comparator that can be used to make fast, high-precision analog-to-digital converters. Scheduled for introduction in a few months, the 4950 can resolve 100-μV differentials in 100 ns—fast enough for high-speed 12-bit a-d converters.

Harris Semiconductor Products Division, Box 883, Melbourne, Fla. 32901 [413]

Power transistors exhibit high transition frequencies

The SLPT series consists of matched pnp and npn transistors that work linearly to supply power at high frequencies. As such, they are suited for fast high-power switching and high-power audio applications.

The devices have transition frequencies of up to 100 MHz at 1 A and dc current gains of from 40 to

280. They are available with collector-to-emitter voltages up to 150 V dc, collector currents of 10 A, and power of 120 W at junction temperatures up to 150°C. In quantities of 1,000 or more, they are priced from 55¢ to $3.50 each.

Panasonic, One Panasonic Way, Secaucus, N. J. 07094. Phone (201) 348-7276 [415]

Single-supply RAM looks static to system

First in a series of memories that will eventually allow users to upgrade systems from 1 kilobyte to 8 in the same socket, the MK4816 is a byte-wide 16-K dynamic read/write memory (RAM). Although dynamic, the RAM has an on-board bias generator and can work from a single 5-V supply. Furthermore, on-chip refresh circuitry lets users supply refresh signals from microprocessors so that the RAM appears static; there is an auto-refresh feature for battery backup operation.

The 31,000-square-mil chip dissipates only 150 mW and provides access times of 150 ns in the high-speed version and 300 ns in the slower unit. In lots of 100, the faster unit sells for $48.05 and the slower for $35.16. Both come in 28-pin dual in-line plastic packages.

Mostek Corp., 1215 W. Crosby Rd., Carrollton, Texas 75006. Phone (214) 242-0444 [414]

Microwave transistors push power in series or shorts

Intended for use in microwave transmission systems, a single transistor and a series of devices operate at frequencies around 2GHz. The single transistor, the TRW 2020, works in the 1.0-to-2.3-GHz band and delivers up to 20 W. Its output is fully protected against power reflection due to a short or open circuit; in 100s, it is priced at $151.73.

The MRAL-2023's optimum operation is in the band from 2,000 to 2,300 MHz. The series consists of four transistors with power ratings of 1.5, 3, 6, and 12 W respectively. Phase-tracking characteristics vary little from one to another, so there is little power loss when they are used in combination. In 100s, unit prices range from $38.25 to $169.79 depending on power output.

TRW Semiconductors, 14520 Aviation Blvd., Lawnsdale, Calif. 90260 [416]

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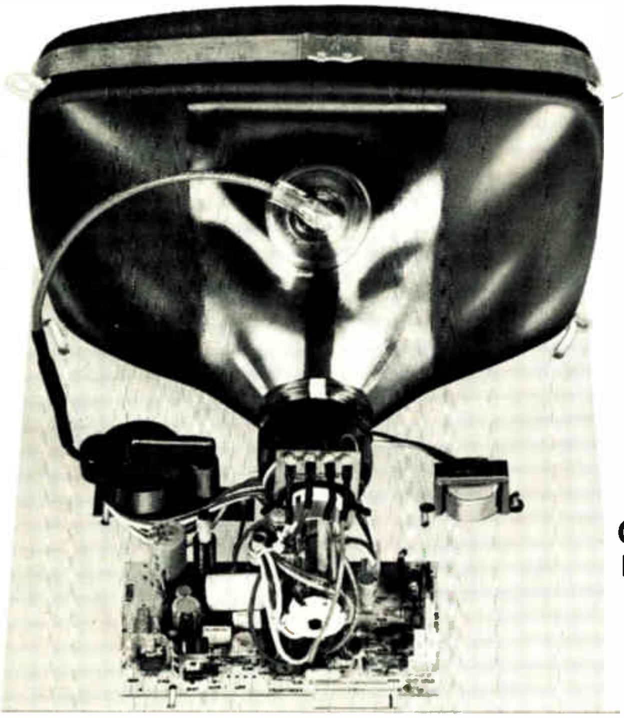

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Our EGR, TAS and TPS position-sensors perform smoothly, accurately and noise-free for up to 250 million cycles. They feature RESISTOFILM (U.S. Patent #3,457,537), a hard, smooth conductive plastic film which is bonded to a flexible high-temperature substrate.

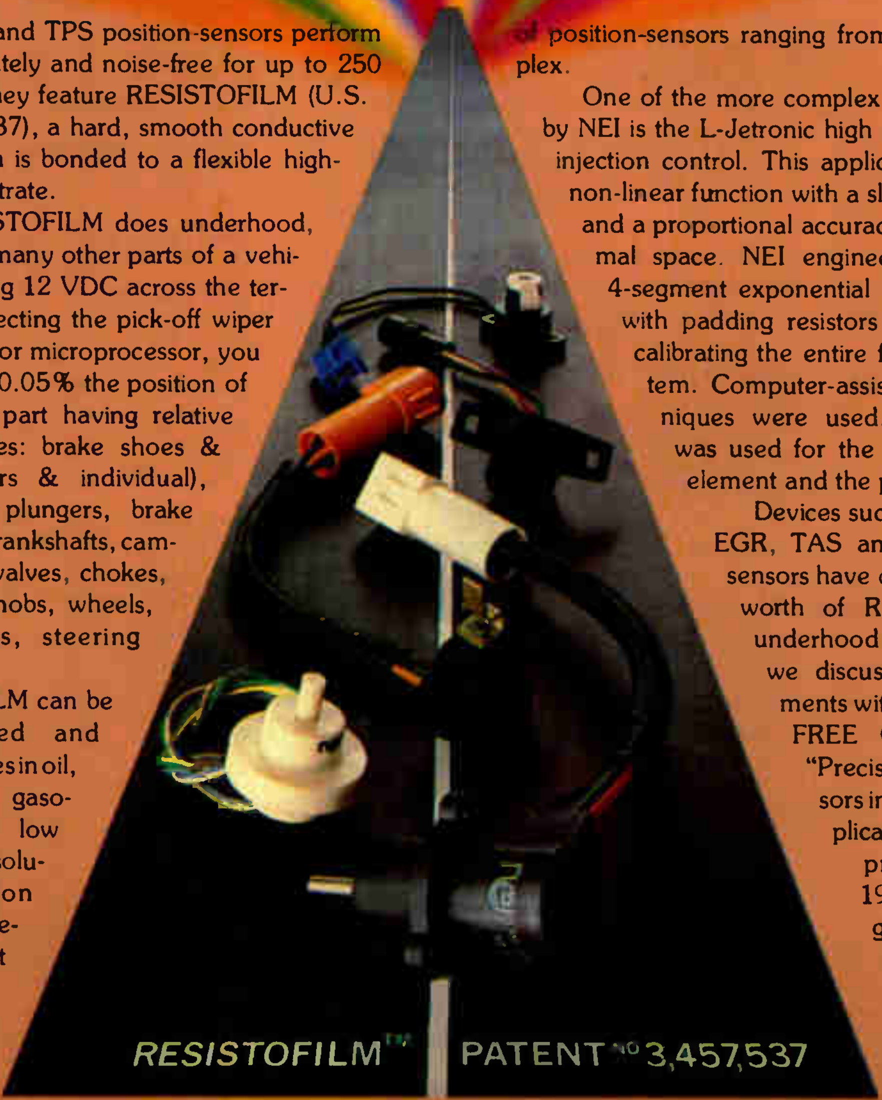
What RESISTOFILM does underhood, it can also do in many other parts of a vehicle. By connecting 12 VDC across the terminals and connecting the pick-off wiper to your indicator or microprocessor, you can sense within 0.05% the position of any automotive part having relative motion. Examples: brake shoes & cylinders (masters & individual), shock absorber plungers, brake pedals, pistons, crankshafts, camshafts, throttles, valves, chokes, floats, springs, knobs, wheels, gears, antennas, steering wheels..........

RESISTOFILM can be flexed, punched and bonded. It operates in oil, diesel fuel, and gasoline. It features low noise, infinite resolution, multi-million cycle life, tight linearity, and low cost in volume production. It can improve the performance of position-sensors ranging from simple to complex.

One of the more complex devices supplied by NEI is the L-Jetronic high performance fuel injection control. This application required a non-linear function with a slope ratio of 40:1 and a proportional accuracy of 1% in minimal space. NEI engineers developed a 4-segment exponential function element with padding resistors which allow for calibrating the entire fuel injection system. Computer-assisted design techniques were used. RESISTOFILM was used for the variable resistive element and the padding resistors.

Devices such as this and our EGR, TAS and TPS position-sensors have demonstrated the worth of RESISTOFILM in underhood applications. May we discuss other requirements with you?

FREE ON REQUEST: "Precision Position-Sensors in Automotive Applications," a paper presented at the 1978 SAE Congress & Exposition by William Wheeler, Laboratory Manager, NEI R&D Dept.



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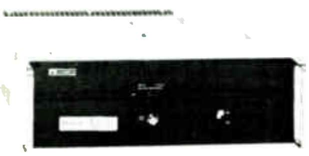

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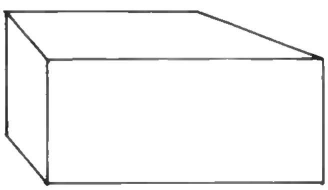

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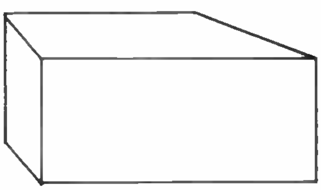

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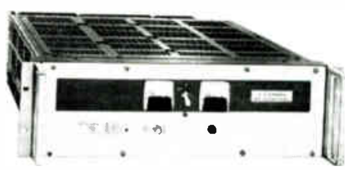
38% Efficiency
$1374

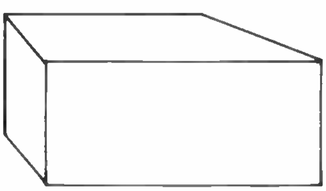


LXS-G
110/220 VAC INPUT

38% Efficiency
$773

LXS-7
110/220 VAC INPUT

1965-66



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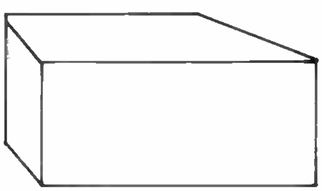
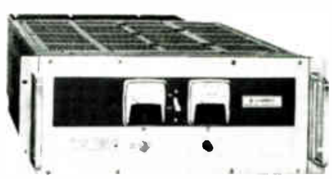


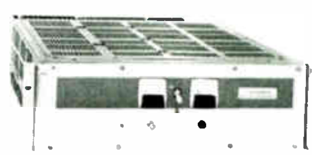
NO EQUIVALENT

35% Efficiency
$1528



LM-H
110/220 VAC INPUT

35% Efficiency
$962



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LGS-5
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70% Efficiency
$345

LJS-12
110/220 VAC
130-160 VDC INPUT

70% Efficiency
$285

LJS-11
110/220 VAC
130-160 VDC INPUT

70% Efficiency
$230

LJS-10
110/220 VAC
130-160 VDC INPUT

60% Efficiency
$160

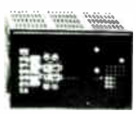
LJS-13
110/220 VAC
130-160 VDC INPUT

LINEAR

38% Efficiency
$641

LXS-EE
110/220 VAC INPUT

38% Efficiency
$372



LXS-D
110/220 VAC INPUT

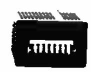
38% Efficiency
$321

LXS-CC
110/220 VAC INPUT

38% Efficiency
$234

LXS-C
110/220 VAC INPUT

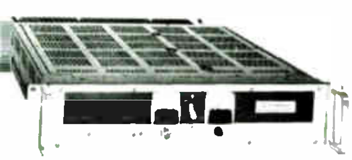
38% Efficiency
$195



LXS-B
110/220 VAC INPUT

LINEAR

35% Efficiency
$762



LM-F
110/220 VAC INPUT

36% Efficiency
$521

LM-EE
110/220 VAC INPUT

36% Efficiency
$412

LM-E
110/220 VAC INPUT

36% Efficiency
$326

LM-D
110/220 VAC INPUT

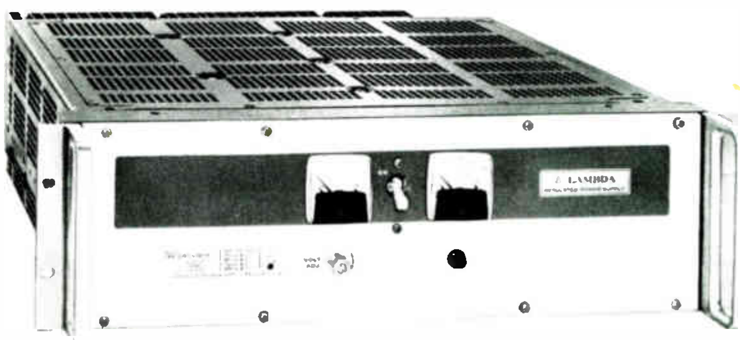
36% Efficiency
$207

LM-C
110/220 VAC INPUT

HERE'S WHY LAMBDA'S SWITCHING

LINEAR

LGS-EE-5-OV-R



LXS-G-5-OV-R

SWITCHING		LINEAR
5 Volts ± 5% ADJ	**VOLTAGE**	5 Volts ± 5% ADJ
110 A	**CURRENT**	110 A
4 15/16″ x 7 1/2″ x 16 1/2″	**SIZE**	5 3/16″ x 19″ x 16 1/2″
26 lbs	**WEIGHT**	90 lbs
70%	**EFFICIENCY**	33%
1100 Watts Max	**POWER INPUT**	2200 watts max
Digital Meter Std.	**METERS**	Analog Meter Std
OV Built In	**OV PROTECTION**	OV Built In
$773	**PRICE**	$1374

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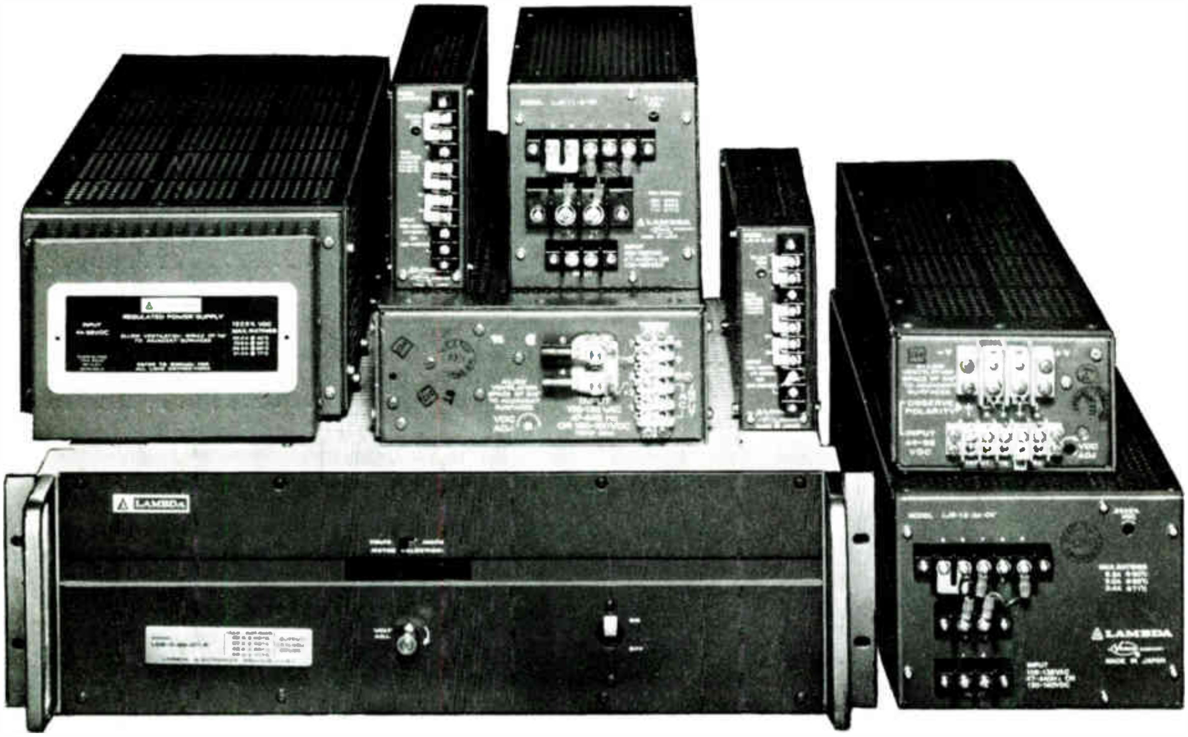


	LAMBDA SWITCHING POWER SUPPLIES	COMPETITORS' SWITCHING POWER SUPPLIES
• 5 year guarantee	Yes	No
• Tested and meets MIL STD 810C	Yes	No
• Meets MIL I 6181D EMI conducted	Yes	No
• 10 package sizes	Yes	No
• Convection cooled, no fans or blowers needed	Yes	No
• One day delivery	Yes	No
• Built in OV protection	Yes	No
• Efficiency greater than 70%	Yes	No
• Digital Meter Standard	Yes	No
• High reliability through new advanced hybrid & monolithic Lambda semiconductors	Yes	No

LG SERIES
ENVIRONMENT ENGINEERED

LGS-G

LGS-F

LGS-EE

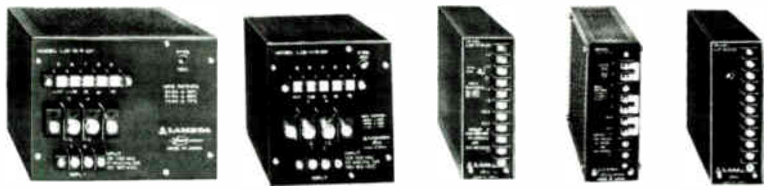
LGS-6

LGS-5

CHECK THESE FEATURES

- 91 models, 5 package sizes
- up to 200 amps, up to 28 volts
- input 20.5-32, 44-58 VDC as well as 105-132 VAC/187-242 VAC/ 205-265 VAC
- hi-reliability obtained thru new advanced circuitry
- less than 120 components for LGS-5
  less than 140 components for LGS-6
  less than 160 components for LGS-EE
  less than 180 components for LGS-F
  less than 200 components for LGS-G
- convection-cooled, no fans or blowers needed
- meets mil spec MIL-I-6181D EMI conducted
- meets MIL-STD-810C
  1) Low Pressure — Method 500.1, Procedure I.
  2) High Temperature — Method 501.1, Procedure I & II.
  3) Low Temperature — Method 502.1, Procedure I.
  4) Temperature Shock — Method 503.0, Procedure I.
  5) Temperature — Altitude — Method 504.1, Procedure I. Class 2 (0°C operating)
  6) Humidity — Method 507.1, Procedure I.
  7) Fungus — Method 508.1, Procedure I.
  8) Vibration — Method 514.2, Procedures X & XI.
  9) Shock — Method 516.2, Procedures I & III.
- efficiency up to 75%
- density up to 1.2 watts/cu in
- 5 year guarantee
- serviceability—designed for ease of field repair
- built-in OV shuts down inverter and crowbars output voltage
- power failure hold-up time
- fungus proofing standard
- 20 KHz switching
- vacuum varnished impregnated transformer
- hermetically sealed Lambda semiconductors
- listed in UL recognized component index
- CSA certified

LJ SERIES
50,000 HOURS MTBF DEMONSTRATED*



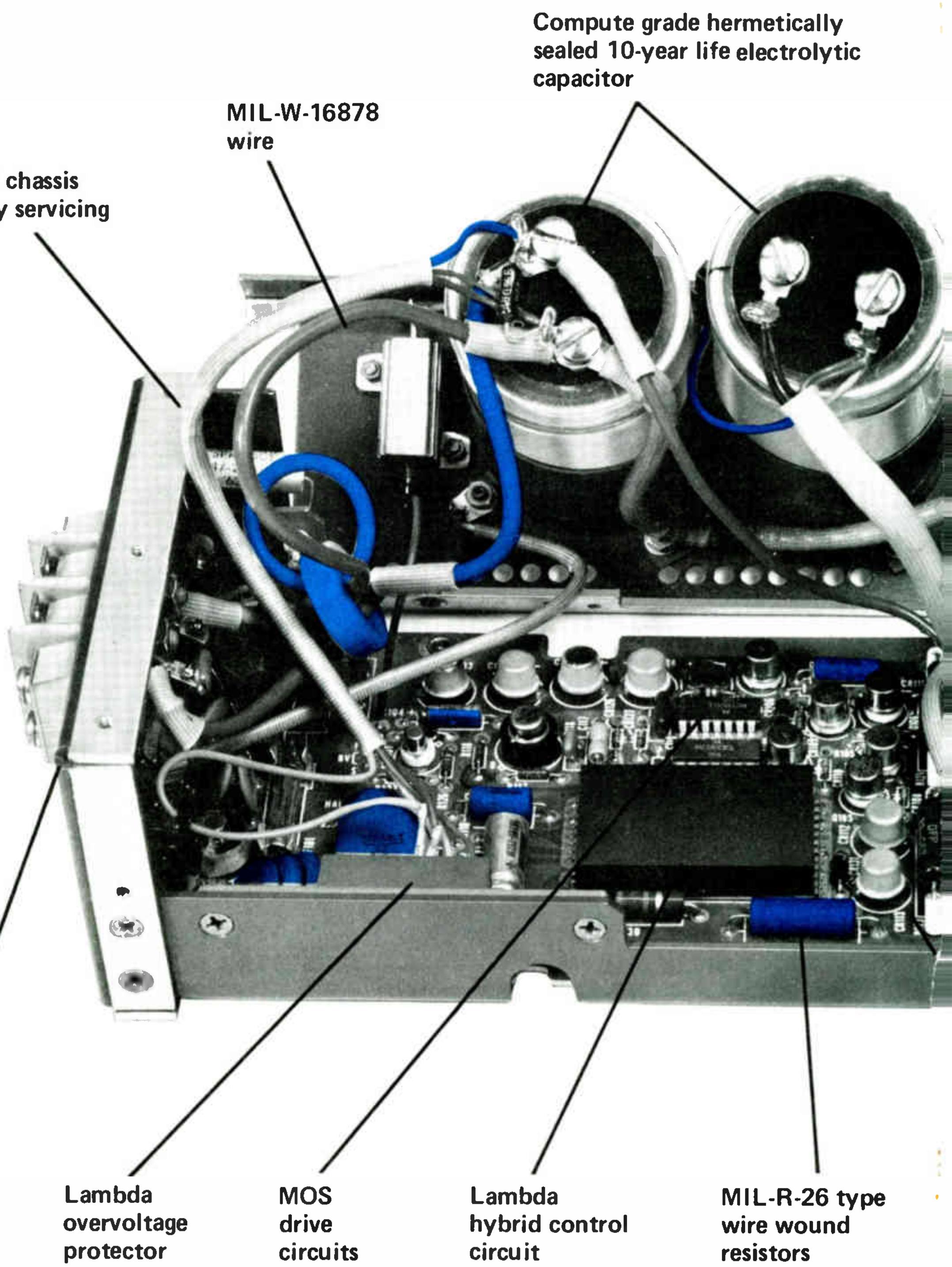
LJS-12 LJS-11 LJS-10 LJS-13 LJT-14

CHECK THESE FEATURES

- 57 models, 5 package sizes
- up to 30 amps, up to 28 volts
- 20 KHz switching
- built-in OV shuts down inverter and crowbars output voltage
- efficiency—greater than 70%
- convection-cooled, no fans or blower necessary
- remote shutdown
- serviceability—designed for ease of field repair
- power failure hold-up time: 16 msec
- AC input 105-132/187-265 VAC
- reg-0.4%
- ripple—10 mV rms
- listed in UL recognized component index
- guaranteed for 5 years
- Single and triple output models

*CONDITIONS: FULL LOAD–40°C RATINGS–115 VOLTS AC INPUT–CONFIDENCE LEVEL: 60%

HERE'S WHY λ LAMBDA LG SERIES THE MOST ADVANCED SWITCHING



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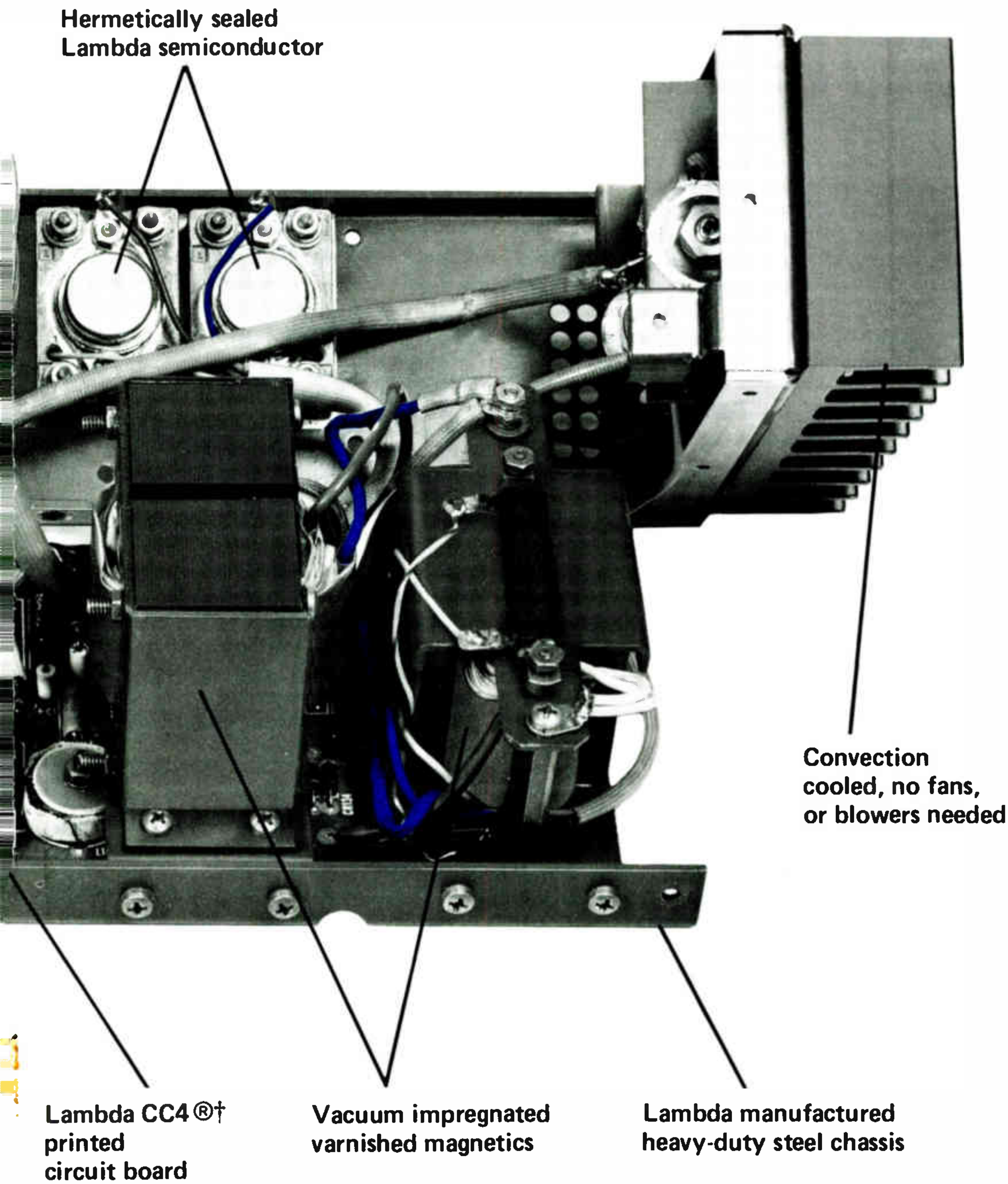


Voltage and Current Ratings

AC INPUT 105-132 VAC STANDARD

5 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	MAX AMPS AT AMBIENT OF 40 C	50 C	60 C	71 C	PKG SIZE	DIMENSIONS (inches)	PRICE
LJS-13-5-0V	0.4%, 0.4%	10	5.0	5.0	4.0	2.8	13	4 3/4 X 1 25/32 X 6 5/16	$ 160
LJS-10-5-0V	0.4%, 0.4%	10	10.0	10.0	8.0	5.5	10	4 3/4 X 1 25/32 X 7 15/16	230
LJS-11-5-0V	0.4%, 0.4%	10	20.0	20.0	16.0	11.0	11	4 3/4 X 4 5/16 X 7 15/16	285
LJS-12-5-0V	0.4%, 0.4%	10	30.0	30.0	24.0	16.5	12	4 3/4 X 6 1/4 X 7 15/16	345
LGS-5-5-0V-R	0.1%, 0.1%	10	45.0	38.0	31.0	21.0	5	3 3/16 X 4 15/16 X 14 5/8	476
LGS-6-5-0V-R	0.1%, 0.1%	10	70.0	61.0	51.0	38.0	6	3 3/16 X 7 1/2 X 15 1/8	642
LGS-EE-5-0V-R	0.1%, 0.1%	10	110.0	100.0	86.0	72.0	EE	4 15/16 X 7 1/2 X 16 1/2	773
LGS-F-5-0V-R	0.1%, 0.1%	10	150.0	135.0	116.0	95.0	F	3 1/2 X 19 X 14	1125
LGS-G-5-0V-R	0.1%, 0.1%	10	200.0	180.0	155.0	130.0	G	5 3/16 X 19 X 14	1404

6 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40 C	50 C	60 C	71 C	PKG SIZE	DIMENSIONS (inches)	PRICE
LJS-13-6-0V	0.4%, 0.4%	10	4.1	4.1	3.3	2.3	13	4 3/4 X 1 25/32 X 6 5/16	$ 160
LJS-10-6-0V	0.4%, 0.4%	10	8.3	8.3	6.6	4.5	10	4 3/4 X 1 25/32 X 7 15/16	230
LJS-11-6-0V	0.4%, 0.4%	10	16.7	16.7	13.3	9.2	11	4 3/4 X 4 5/16 X 7 15/16	285
LJS-12-6-0V	0.4%, 0.4%	10	25.0	25.0	20.0	13.7	12	4 3/4 X 6 1/4 X 7 15/16	345
LGS-5-6-0V-R	0.1%, 0.1%	10	38.0	33.0	26.0	18.0	5	3 3/16 X 4 15/16 X 14 5/8	476
LGS-6-6-0V-R	0.1%, 0.1%	10	60.0	56.0	49.0	36.0	6	3 3/16 X 7 1/2 X 15 1/8	642
LGS-EE-6-0V-R	0.1%, 0.1%	10	100.0	90.0	80.0	65.0	EE	4 15/16 X 7 1/2 X 16 1/2	773
LGS-F-6-0V-R	0.1%, 0.1%	10	127.0	114.0	98.0	81.0	F	3 1/2 X 19 X 14	1125
LGS-G-6-0V-R	0.1%, 0.1%	10	170.0	151.0	132.0	109.0	G	5 3/16 X 19 X 14	1404

12 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40 C	50 C	60 C	71 C	PKG SIZE	DIMENSIONS (inches)	PRICE
LJS-13-12-0V	0.4%, 0.4%	15	2.0	2.0	1.7	1.1	13	4 3/4 X 1 25/32 X 6 5/16	$ 160
LJS-10-12-0V	0.4%, 0.4%	15	4.2	4.2	3.4	2.3	10	4 3/4 X 1 25/32 X 7 15/16	230
LJS-11-12-0V	0.4%, 0.4%	15	8.	8.3	6.6	4.5	11	4 3/4 X 4 5/16 X 7 15/16	285
LJS-12-12-0V	0.4%, 0.4%	15	12.5	12.5	10.0	6.8	12	4 3/4 X 6 1/4 X 7 15/16	345
LGS-5-12-0V-R	0.1%, 0.1%	15	24.0	20.0	16.0	11.0	5	3 3/16 X 4 15/16 X 14 5/8	476
LGS-6-12-0V-R	0.1%, 0.1%	15	37.5	35.0	30.5	23.0	6	3 3/16 X 7 1/2 X 15 1/8	642
LGS-EE-12-0V-R	0.1%, 0.1%	15	60.0	53.0	46.0	38.0	EE	4 15/16 X 7 1/2 X 16 1/2	773
LGS-F-12-0V-R	0.1%, 0.1%	15	79.0	71.0	61.0	50.0	F	3 1/2 X 19 X 14	1125
LGS-G-12-0V-R	0.1%, 0.1%	15	105.0	95.0	85.0	70.0	G	5 3/16 X 19 X 14	1404

15 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40 C	50 C	60 C	71 C	PKG SIZE	DIMENSIONS (inches)	PRICE
LJS-13-15-0V	0.4%, 0.4%	15	1.6	1.6	1.3	0.9	13	4 3/4 X 1 25/32 X 6 5/16	$ 160
LJS-10-15-0V	0.4%, 0.4%	15	3.3	3.3	2.6	1.8	10	4 3/4 X 1 25/32 X 7 15/16	230
LJS-11-15-0V	0.4%, 0.4%	15	6.7	6.7	5.3	3.7	11	4 3/4 X 4 5/16 X 7 15/16	285
LJS-12-15-0V	0.4%, 0.4%	15	10.0	10.0	8.0	5.5	12	4 3/4 X 6 1/4 X 7 15/16	345
LGS-5-15-0V-R	0.1%, 0.1%	15	18.7	16.5	13.2	9.0	5	3 3/16 X 4 15/16 X 14 5/8	476
LGS-6-15-0V-R	0.1%, 0.1%	15	30.0	28.0	24.5	20.5	6	3 3/16 X 7 1/2 X 15 1/8	642
LGS-EE-15-0V-R	0.1%, 0.1%	15	47.0	42.0	36.0	30.0	EE	4 15/16 X 7 1/2 X 16 1/2	773
LGS-F-15-0V-R	0.1%, 0.1%	15	69.0	57.0	49.0	40.0	F	3 1/2 X 19 X 14	1125
LGS-G-15-0V-R	0.1%, 0.1%	15	85.0	75.0	65.0	55.0	G	5 3/16 X 19 X 14	1404

20 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40 C	50 C	60 C	71 C	PKG SIZE	DIMENSIONS (inches)	PRICE
LJS-13-20-0V	0.4%, 0.4%	15	1.2	1.2	1.0	0.7	13	4 3/4 X 1 25/32 X 6 5/16	$ 160
LJS-10-20-0V	0.4%, 0.4%	15	2.5	2.5	2.0	1.4	10	4 3/4 X 1 25/32 X 7 15/16	230
LJS-11-20-0V	0.4%, 0.4%	15	5.0	5.0	4.0	2.7	11	4 3/4 X 4 5/16 X 7 15/16	285
LJS-12-20-0V	0.4%, 0.4%	15	7.5	7.5	6.0	4.1	12	4 3/4 X 6 1/4 X 7 15/16	345
LGS-5-20-0V-R	0.4%, 0.4%	15	13.5	11.5	9.3	6.3	5	3 3/16 X 4 15/16 X 14 5/8	476
LGS-6-20-0V-R	0.1%, 0.1%	15	23.0	21.5	18.5	15.5	6	3 3/16 X 7 1/2 X 15 1/8	642
LGS-EE-20-0V-R	0.1%, 0.1%	15	34.0	30.0	26.0	22.0	EE	4 15/16 X 7 1/2 X 16 1/2	773
LGS-F-20-0V-R	0.1%, 0.1%	15	48.0	43.0	37.0	30.0	F	3 1/2 X 19 X 14	1125
LGS-G-20-0V-R	0.1%, 0.1%	15	62.0	55.0	48.0	40.0	G	5 3/16 X 19 X 14	1404

24 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40 C	50 C	60 C	71 C	PKG SIZE	DIMENSIONS (inches)	PRICE
LJS-13-24-0V	0.4%, 0.4%	15	1.0	1.0	0.8	0.6	13	4 3/4 X 1 25/32 X 6 5/16	$ 160
LJS-10-24-0V	0.4%, 0.4%	15	2.1	2.1	1.7	1.2	10	4 3/4 X 1 25/32 X 7 15/16	230
LJS-11-24-0V	0.4%, 0.4%	15	4.2	4.2	3.3	2.3	11	4 3/4 X 4 5/16 X 7 15/16	285
LJS-12-24-0V	0.4%, 0.4%	15	6.3	6.3	5.0	3.4	12	4 3/4 X 6 1/4 X 7 15/16	345
LGS-5-24-0V-R	0.1%, 0.1%	15	11.5	9.9	7.9	5.4	5	3 3/16 X 4 15/16 X 14 5/8	476
LGS-6-24-0V-R	0.1%, 0.1%	15	20.0	19.0	16.0	13.0	6	3 3/16 X 7 1/2 X 15 1/8	642
LGS-EE-24-0V-R	0.1%, 0.1%	15	30.0	27.0	23.0	19.0	EE	4 15/16 X 7 1/2 X 16 1/2	773
LGS-F-24-0V-R	0.1%, 0.1%	15	41.0	32.0	37.0	26.0	F	3 1/2 X 19 X 14	1125
LGS-G-24-0V-R	0.1%, 0.1%	15	54.0	48.0	42.0	35.0	G	5 3/16 X 19 X 14	1404

28 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40 C	50 C	60 C	71 C	PKG SIZE	DIMENSIONS (inches)	PRICE
LJS-13-28-0V	0.4%, 0.4%	15	0.9	0.9	0.7	0.5	13	4 3/4 X 1 25/32 X 6 15/16	$ 160
LJS-10-28-0V	0.4%, 0.4%	15	1.8	1.8	1.4	1.0	10	4 3/4 X 1 25/32 X 7 15/16	230
LJS-11-28-0V	0.4%, 0.4%	15	3.6	3.6	2.0	2.0	11	4 3/4 X 4 5/16 X 7 15/16	285
LJS-12-28-0V	0.4%, 0.4%	15	5.4	5.4	4.3	3.0	12	4 3/4 X 6 1/4 X 7 15/16	345
LGS-5-28-0V-R	0.1%, 0.1%	15	9.6	8.2	6.6	4.5	5	3 3/16 X 4 15/16 X 14 5/8	476
LGS-6-28-0V-R	0.1%, 0.1%	15	17.5	16.5	14.5	12.0	6	3 3/16 X 7 1/2 X 15 1/8	642
LGS-EE-28-0V-R	0.1%, 0.1%	15	25.0	23.0	20.0	16.0	EE	4 15/16 X 7 1/2 X 16 1/2	773
LGS-F-28-0V-R	0.1%, 0.1%	15	35.0	32.0	28.0	23.0	F	3 1/2 X 19 X 14	1125
LGS-G-28-0V-R	0.1%, 0.1%	15	46.0	42.0	36.0	30.0	G	5 3/16 X 19 X 14	1404

Voltage and Current Ratings

DC INPUT 20.5-32 VDC STANDARD

5 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE (mV RMS)	MAX AMPS AT AMBIENT OF 40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5-5-C-OV-R	0.1%, 0.1%	10	35.0	31.0	25.0	16.5	5	3 3/16 x 4 15/16 x 15	$535
6 VOLTS ± 5% ADJ									
LGS-5-6-C-OV-R	0.1%, 0.1%	10	29.0	26.0	21.0	14.0	5	3 3/16 x 4 15/16 x 15	$535
12 VOLTS ± 5% ADJ									
LGS-5-12-C-OV-R	0.1%, 0.1%	15	15.0	13.5	10.0	7.0	5	3 3/16 x 4 15/16 x 15	$535
15 VOLTS ± 5% ADJ									
LGS-5-15-C-OV-R	0.1%, 0.1%	15	13.0	11.0	8.0	5.6	5	3 3/16 x 4 15/16 x 15	$535
20 VOLTS ± 5% ADJ									
LGS-5-20-C-OV-R	0.1%, 0.1%	15	10.5	9.0	7.0	4.5	5	3 3/16 x 4 15/16 x 15	$535
24 VOLTS ± 5% ADJ									
LGS-5-24-C-OV-R	0.1%, 0.1%	15	8.5	7.5	6.0	3.9	5	3 3/16 x 4 15/16 x 15	$535
28 VOLTS ± 5% ADJ									
LGS-5-28-C-OV-R	0.1%, 0.1%	15	7.5	6.8	5.4	3.5	5	3 3/16 x 4 15/16 x 15	$535

DC INPUT 44-58 VDC STANDARD

5 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE (mV RMS)	40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5-5-D-OV-R	0.1%, 0.1%	10	40.0	32.0	25.0.	16.5	5	3 3/16 x 4 15/16 x 15	$476
LGS-6-5-D-OV-R	0.1%, 0.1%	10	60.0	53.0	45.0	36.0	6	3 3/16 x 7 1/2 x 15 1/8	655
LGS-EE-5-D-OV-R	0.1%, 0.1%	10	90.0	85.0	73.0	54.0	EE	4 15/16 x 7 1/2 x 16 1/2	832
6 VOLTS ± 5% ADJ									
LGS-5-6-D-OV-R	0.1%, 0.1%	10	35.0	28.0	21.5	14.0	5	3 3/16 x 4 15/16 x 15	$476
LGS-6-6-D-OV-R	0.1%, 0.1%	10	50.0	46.0	41.0	35.0	6	3 3/16 x 7 1/2 x 15 1/8	655
LGS-EE-6-D-OV-R	0.1%, 0.1%	10	78.0	67.0	56.0	42.5	EE	4 15/16 x 7 1/2 x 16 1/2	832
12 VOLTS ± 5% ADJ									
LGS-5-12-D-OV-R	0.1%, 0.1%	15	17.5	14.0	10.8	7.0	5	3 3/16 x 4 15/16 x 15	$476
LGS-6-12-D-OV-R	0.1%, 0.1%	15	31.0	28.0	24.0	18.0	6	3 3/16 x 7 1/2 x 15 1/8	655
LGS-EE-12-D-OV-R	0.1%, 0.1%	15	39.0	33.5	28.0	21.0	EE	4 15/16 x 7 1/2 x 16 1/2	832
15 VOLTS ± 5% ADJ									
LGS-5-15-D-OV-R	0.1%, 0.1%	15	14.0	11.0	8.6	5.6	5	3 3/16 x 4 15/16 x 15	$476
LGS-6-15-D-OV-R	0.1%, 0.1%	15	25.0	23.0	20.0	15.0	6	3 3/16 x 7 1/2 x 15 1/8	655
LGS-EE-15-D-OV-R	0.1%, 0.1%	15	32.0	28.0	23.5	17.5	EE	4 15/16 x 7 1/2 x 16 1/2	832
20 VOLTS ± 5% ADJ									
LGS-5-20-D-OV-R	0.1%, 0.1%	15	11.5	9.3	7.1	4.6	5	3 3/16 x 4 15/16 x 15	$476
LGS-6-20-D-OV-R	0.1%, 0.1%	15	19.0	18.0	16.0	12.0	6	3 3/16 x 7 1/2 x 15 1/8	655
LGS-EE-20-D-OV-R	0.1%, 0.1%	15	26.0	22.5	18.5	14.0	EE	4 15/16 x 7 1/2 x 16 1/2	832
24 VOLTS ± 5% ADJ									
LGS-5-24-D-OV-R	0.1%, 0.1%	15	9.8	7.8	6.1	3.9	5	3 3/16 x 4 15/16 x 15	$476
LGS-6-24-D-OV-R	0.1%, 0.1%	15	16.0	15.0	13.0	10.0	6	3 3/16 x 7 1/2 x 15 1/8	655
LGS-EE-24-D-OV-R	0.1%, 0.1%	15	21.5	18.5	15.5	11.5	EE	4 15/16 x 7 1/2 x 16 1/2	832
28 VOLTS ± 5% ADJ									
LGS-5-28-D-OV-R	0.1%, 0.1%	15	8.7	7.0	5.4	3.5	5	3 3/16 x 4 15/16 x 15	$476
LGS-6-28-D-OV-R	0.1%, 0.1%	15	14.0	13.0	11.0	9.0	6	3 3/16 x 7 1/2 x 15 1/8	655
LGS-EE-28-D-OV-R	0.1%, 0.1%	15	19.5	17.0	14.0	10.5	EE	4 15/16 x 7 1/2 x 16 1/2	832

Voltage and Current Ratings

AC INPUT 187-242 VAC STANDARD

5 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	MAX AMPS AT AMBIENT OF 40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5V-5-OV-R	0.1%, 0.1%	10	43.0	36.5	28.0	15.0	5	3 3/16 x 4 15/16 x 15	$533
LGS-6V-5-OV-R	0.1%, 0.1%	10	63.0	55.0	46.0	34.2	6	3 3/16 x 7 1/2 x 15 1/8	719

6 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5V-6-OV-R	0.1%, 0.1%	10	37.0	32.0	23.0	13.0	5	3 3/16 x 4 15/16 x 15	$533
LGS-6V-6-OV-R	0.1%, 0.1%	10	54.0	50.4	44.1	32.4	6	3 3/16 x 7 1/2 x 15 1/8	719

12 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5V-12-OV-R	0.1%, 0.1%	15	23.0	19.0	15.0	7.0	5	3 3/16 x 4 15/16 x 15	$533
LGS-6V-12-OV-R	0.1%, 0.1%	15	34.0	31.5	27.4	20.7	6	3 3/16 x 7 1/2 x 15 1/8	719

15 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5V-15-OV-R	0.1%, 0.1%	15	18.5	16.0	12.0	6.0	5	3 3/16 x 4 15/16 x 15	$533
LGS-6V-15-OV-R	0.1%, 0.1%	15	27.0	25.2	22.0	18.4	6	3 3/16 x 7 1/2 x 15 1/8	719

20 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5V-20-OV-R	0.1%, 0.1%	15	12.6	10.8	8.7	4.6	5	3 3/16 x 4 15/16 x 15	$533
LGS-6V-20-OV-R	0.1%, 0.1%	15	20.7	19.3	16.6	13.9	6	3 3/16 x 7 1/2 x 15 1/8	719

24 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5V-24-OV-R	0.1%, 0.1%	15	11.5	9.9	7.9	3.9	5	3 3/16 x 4 15/16 x 15	$533
LGS-6V-24-OV-R	0.1%, 0.1%	15	18.0	17.1	14.4	11.7	6	3 3/16 x 7 1/2 x 15 1/8	719

28 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5V-28-OV-R	0.1%, 0.1%	15	9.6	8.0	6.0	3.3	5	3 3/16 x 4 15/16 x 15	$533
LGS-6V-28-OV-R	0.1%, 0.1%	15	15.7	14.8	13.0	10.8	6	3 3/16 x 7 1/2 x 15 1/8	719

AC INPUT 205-265 VAC STANDARD

5 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5V1-5-OV-R	0.1%, 0.1%	10	43.0	36.5	28.0	15.0	5	3 3/16 x 4 15/16 x 15	$533
LGS-6V1-5-OV-R	0.1%, 0.1%	10	63.0	55.0	46.0	34.2	6	3 3/16 x 7 1/2 x 15 1/8	719

6 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5V1-6-OV-R	0.1%, 0.1%	10	37.0	32.0	23.0	13.0	5	3 3/16 x 4 15/16 x 15	$533
LGS-6V1-6-OV-R	0.1%, 0.1%	10	54.0	50.4	44.1	32.4	6	3 3/16 x 7 1/2 x 15 1/8	719

12 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5V1-12-OV-R	0.1%, 0.1%	15	23.0	19.0	15.0	7.0	5	3 3/16 x 4 15/16 x 15	$533
LGS-6V1-12-OV-R	0.1%, 0.1%	15	34.0	31.5	27.4	20.7	6	3 3/16 x 7 1/2 x 15 1/8	719

15 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5V1-15-OV-R	0.1%, 0.1%	15	18.5	16.0	12.0	6.0	5	3 3/16 x 4 15/16 x 15	$533
LGS-6V1-15-OV-R	0.1%, 0.1%	15	27.0	25.2	22.0	18.4	6	3 3/16 x 7 1/2 x 15 1/8	719

20 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5V1-20-OV-R	0.1%, 0.1%	15	12.6	10.8	8.7	4.6	5	3 3/16 x 4 15/16 x 15	$533
LGS-6V1-20-OV-R	0.1%, 0.1%	15	20.7	19.3	16.6	13.9	6	3 3/16 x 7 1/2 x 15 1/8	719

24 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5V1-24-OV-R	0.1%, 0.1%	15	11.5	9.9	7.9	3.9	5	3 3/16 x 4 15/16 x 15	$533
LGS-6V1-24-OV-R	0.1%, 0.1%	15	18.0	17.1	14.4	11.7	6	3 3/16 x 7 1/2 x 15 1/8	719

28 VOLTS ± 5% ADJ

MODEL	REGULATION (line load)	RIPPLE mV (RMS)	40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (Inches)	PRICE
LGS-5V1-28-OV-R	0.1%, 0.1%	15	9.6	8.0	6.0	3.3	5	3 3/16 x 4 15/16 x 15	$533
LGS-6V1-28-OV-R	0.1%, 0.1%	15	15.7	14.8	13.0	10.8	6	3 3/16 x 7 1/2 x 15 1/8	719

SPECIFICA..IONS OF ..G SERIES

DC output

voltage range shown in tables

Regulated voltage

regulation line . . . . 0.1% for 105 to 132 VAC, 187-242 VAC, 205-265 VAC
regulation load. . . . . 0.1% for 0 to full load
ripple and noise . . . . 10mV RMS, 35 mV p-p for 5 and 6V units
15mV RMS, 100mV p-p for 12 thru 28V units
remote programming resistance . 1000 ohms/volt
remote programming voltage . . volt per volt

Temperature coefficient . . . . 0.03% per°C

AC input

line . . . . 105-132 VAC, 47 440 Hz

power . . . . 360 watts max. at 0.6 P.F. for LGS-5
750 watts max. at 0.7 P.F. for LGS-6
1100 watts max. at 0.6 P.F. for LGS-EE
1350 watts max. at 0.7 P.F. for LGS-F
1800 watts max. at 0.7 P.F. for LGS-G

DC input . . . .

20.5-32 VDC, LGS-5-C packages only. Input voltage specs. comply with minimum usable voltage for lead acid batteries.
44-58 VDC "D" models only.
145 VDC ± 10%, LGS-5, LGS 6 packages only.

Efficiency . . .

64% minimum except LGS-EE-D and LGS-6-D which are 60% minimum and LGS-5-C which is 55% minimum.

Soft-start circuit: (LGS-6,LGS-6V,LGS-EE,LGS-G,LGS-F only)

limits in-rush current at turn-on.

Ambient operating temperature

continuous duty 0° to 71°C.

Storage temperature range

−55°C to +85°C

Overload protection

Electrical

pre-set electronic current limiting at factory. Internal failure protection by means of line fuse.

Thermal

by self-resetting thermostat (when properly mounted).

Overvoltage protection

built-in fixed overvoltage protection standard on all units. When a pre-set voltage is exceeded, the overvoltage protector crowbars the output and removes the inverter drive.

EMI

Conducted – conforms to MIL-I-6181D.

Radiated – see graphs for performance.

Cooling – convection cooled.

DC output controls

simple screwdriver voltage adjustment over the voltage range. For LGS-F, and G output voltage adjustable by means of potentiometer on the front panel.

Metering (LGS-F, LGS-G only)

digital panel meter monitors output voltage/current by means of a Volt/Amp selector switch

Input and output connections

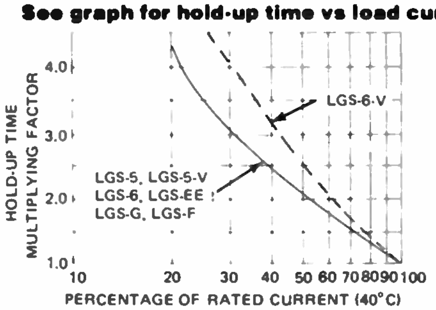
by heavy duty barrier strip; heavy duty studs on all LGS-6, EE, F and G.

Mounting

two mounting surfaces, three mounting positions for LGS-5
one mounting position for LGS-5V, 6, 6V, 6D, EE, EE-D, F and G.
For LGS-5-C and 5D models derate current 10% for mounting positions in which the radiator fins are not vertical.

Power failure

See graph for hold-up time vs load current on all units. (Except LGS-C and LGS-D models).



HOLD UP TIME AT 100% RATED 40 C CURRENT IN MILLISECONDS

MODEL \ SERIES	LGS 5 LGS 5 V	LGS 6	LGS EE	LGS 6 V	LGS G	LGS F
5 OV H	16 5	18 0	16 5	24 0	16 5	16 5
6 OV H	16 5	17 5	9 4	23 0	16 5	16 5
12 OV H	5 0	3 0	9 3	7 0	1 0	4 0
15 OV H	5 0	4 5	8 3	8 0	2 0	4 0
20 OV H	5 0	6 0	5 0	10 0	6 9	2 0
24 OV H	5 0	2 0	2 5	8 0	5 0	0 5
28 OV H	5 0	1 0	7 0	8 0	5 0	0 5

Hold-up times as a function of load current.

Remote sensing

provision is made for remote sensing to eliminate effects of power output lead resistance on DC regulation.

Fungus proofing

all units are rendered fungi inert.

Military Specifications

The LGS series has passed the following tests in accordance with MIL-STD-810C. (LGS-F, LGS-G presently under test)

1) Low Pressure – Method 500.1, Procedure I.
2) High Temperature – Method 501.1, Procedure I & II.
3) Low Temperature – Method 502.1, Procedure I.
4) Temperature Shock - Method 503. 1, Procedure I.
5) Temperature – Altitude – Method 504.1, Procedure I. Class 2 (0°C operating)
6) Humidity – Method 507.1, Procedure I.
7) Fungus – Method 508.1, Procedure I.
8) Vibration – Method 514.2, Procedures X & XI.
9) Shock - Method 516.2, Procedures I & III.

MIL-1-6181D – Conducted and radiated EMI with one output terminal grounded.

Physical Data

Package Model	Size (inches)	Weight Net (lbs)	Weight Ship (lbs)
LGS 5	3 3/16 x 4 15/16 x 15	13 1/2	15
LGS-6	3 3/16 x 7 1/2 x 15 1/8	20	23
LGS-EE	4 15/16 x 7 1/2 x 16 1/2	26	31
LGS-F	3 1/2 x 19 x 14	38	48
LGS-G	5 3/16 x 19 x 14	42	52

Options

AC input

For LGS-EE, F, and G models only
For LGS-5, LGS-6 see page 12

Add Suffix	For Operation at:	Price Qty 1-14	Price Mixed Models Qty 15 & up	Price Single Model Qty 15 & up
–V	187-242VAC * 47-440Hz	12% or $30†	12% or $30†	10% or $30†
–V1	205-265 VAC 47-440Hz	12% or $30†	12% or $30†	10% or $30†

*derate 10% for V option only † whichever is greater

Accessories

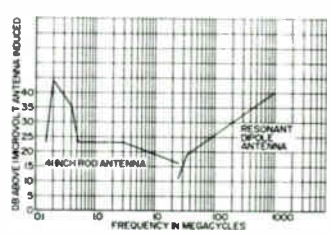
Rack adapters and chassis slides see catalog.

Guaranteed for 5 years

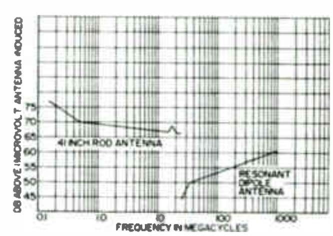
5 year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of 5 years.

UL/CSA

Listed in UL recognized components index; CSA certified (LGS-F, LGS-G presently under test).



Narrow band (cw) radiated interference limits



Broadband and pulsed cw radiated interference limits

SPECIFICATIONS OF LJ SERIES

DC output

voltage range: refer to tables

regulation, line	0.4% for line variations from 105-132 VAC., 0.3% for LJT
regulation, load	0.4% for load variations from 0 to full load, 0.7% for LJT
remote programming resistance	1000 ohms/volt nominal (Except LJT-14)
remote programming voltage	volt/volt (Except LJT-14)
ripple and noise	10mV rms, 50 mV p-p for 5V and 6V models; 15 mV rms, 100 mV p-p for 12V to 28V models, except for LJT. For LJT, ±12V, 15mV rms, 70mV p-p.
temperature coefficient	0.03%/°C
power failure	output will remain within regulation for 16 msec after power failure.

AC input

line	105-132 VAC 47-440 Hz
hold-up time	16 msec min at low line and full load, and V_O max.
Shutdown signal	AC output of 6.3V available in case of power failure. (for LJT only)

DC input

145 VDC ± 10% (not for V option units)

Overshoot

no overshoot on turn-on, turn-off, or power failure

Efficiency

greater than70% (60% FOR LJS-13) with advanced 20 KHz switching circuitry.

Ambient operating temperature range

continuous duty from 0°C to 71°C with load current ratings as shown in tables. No derating 0° to 50°C

Storage temperature range

-55°C to 85°C

Overload protection

Electrical

external overload protection: automatic factory preset electronic current limiting circuit limits the output current thereby providing protection for the load as well as the power supply.

internal failure protection: provided by fuse.

Input and output connections

heavy duty terminal block on front of chassis.

Controls

DC output controls

simple screwdriver voltage adjustment over the voltage range

Remote sensing

provision is made for remote sensing to eliminate effect of power output lead resistance on DC regulation. (Except LJT-14)

Remote shutdown

capability of remote on-off control for either positive ground or negative ground output.

Overvoltage protection

built in fixed overvoltage protection on all model outputs.

Mounting

One mounting surface.

Options

AC input

Add Suffix	For Operation at:	Price Qty. 1-14	Price Mixed Models Qty. 15 and up	Price Single Model Qty. 15 and up
–V	187-265 VAC 47-440 Hz	12% or $30**	12% or $30**	10% or $30**

**whichever is greater

See Physical Data below for sizes of "V" option power supplies — The "V" option supplies sizes are larger than equivalent standard power supplies.

Physical Data

Package Model	Weight (lbs.) net	Size (inches)
LJ-13	1.6	4 3/4 X 1 25/32 X 6 5/16
LJ-13-V	2.0	4 3/4 X 1 25/32 X 7 15/16
LJ-10	2.0	4 3/4 X 1 25/32 X 7 15/16
LJ-10-V	3.0	4 3/4 X 1 25/32 X 9 1/16
LJ-11	5.5	4 3/4 X 4 5/16 X 7 15/16
LJ-11-V	7.0	4 3/4 X 4 5/16 X 9 1/16
LJ-12	7.0	4 3/4 X 6 1/4 X 7 15/16
LJ-12-V	8.5	4 3/4 X 6 1/4 X 9 1/16
LJT-14	3.6	5 1/8 X 2 11/64 x 8 13/16

Finish

gray, Fed. Std. 595 No. 26081.

Listed in Underwriter's Laboratories Recognized Components Index.

Guaranteed for 5 years

5 year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of 5 years.

TRIPLE OUTPUT Switching Power Supply

New

MODEL	REGULATION (line, load)	RIPPLE (mV RMS)	ADJ. VOLT. RANGE VDC	MAX AMPS AT AMBIENT OF 40°C	50°C	60°C	71°C	PKG. SIZE	DIMENSIONS (inches)	PRICE
LJT-14-5152	0.3%, 0.7%	10mV	5± 10%	10.0	10.0	7.0	4.0	14	5 1/8 x 2 11/64 x 8 13/16	$385
		15mV	±12± 10%	1.0	1.0	0.7	0.4			

For complete specifications see page 14

World's First Line of 20 KHz Wide Range Switching Power Supplies

New

LES-F-01-OV

OUTPUT RATINGS FOR LES-F SERIES

MODEL	REGULATED OUTPUT VOLTAGE	MAX. OUTPUT CURRENT AT T AMB 40°C	50°C	60°C	71°C	PRICE
LES-F-01-OV	0 – 7.5V	100A	83A	66A	47.5A	$1200
LES-F-02-OV	0 – 18V	47.5A	41A	32.5A	23.5A	1100
LES-F-03-OV	0 – 36V	24A	20.4A	16.5A	12A	1000
LES-F-04-OV	0 – 60V	15A	12.8A	10.3A	7.5A	1200

Note: Maximum output current applies over entire output voltage range.

45% smaller by volume and 46% more amps per dollar than equivalent SCR switching power supply

Outstanding Features

Designed to meet military environment MIL-STD-810C

Digital Meter Readout

Convection cooled, no fans or blowers

Constant voltage/constant current

Guaranteed 5 Years

Overvoltage protection — built in on all models

Condensed Specifications of LE Series

Regulated voltage

regulation line .... 0.02% + 2 mV for line variations from 105 to 132 vac (or 187 to 242 vac on 'V' options, 205 to 265 vac on 'VI' options).

regulation load .... 0.02% + 2 mv (LES-F-01, 02) 0.02% + 4 mv (LES-F-03, 04) for load variations from 0 to full load.

remote programming resistance .... 200 Ω/volt nominal

remote programming voltage .... volt/volt

ripple and noise .... 10 mv-rms; 50 mv pp for LES-F-01
15 mv-rms; 100 mv pp for LES-F-02,03,04

temperature coefficient ...... (0.02% + 50 μv)/°C

Constant current

(current regulated line and load) automatic crossover.

voltage range .... As shown in table.

current range .... 5% to full load current.

regulation line .... 0.5% + 50 mA (LES-F-01, 02) 0.5% + 20 mA (LES-F-03, 04) line variations from 105 to 132 vac (or 187 to 242 vac on 'V' opts, 205 to 265 vac on 'VI' opts).

regulation load .... 0.5% of $I_{(max)}$ for load changes from 5% to rated DC voltage.

AC input

line .... 105-132 vac (47-63 Hz) standard input (derate output current by 5% at 50 Hz)

power .... 1250 watts max at 0.6 P.F. at maximum output voltage, high line.

efficiency .... Minimum 60% at maximum output voltage.

soft start circuit .... Limits inrush current at turn on to 200% of full load peak current.

input current .... 25A rms max.

Ambient operating temperature

Continuous duty from 0°C to 71°C with appropriate deratings (40°C to 71°C—see table).

Overload protection

Thermal

By self resetting thermostat

Electrical

External overload protection—adjustable, automatic, electronic current limiting circuit limits output current to preset value. Current limiting settability to 105% of rated current via front panel adjust.

Overvoltage protection

Built in, adjustable overvoltage protection standard on all sets. When preset voltage is exceeded, the overvoltage protector crowbars the output and removes the inverter drive. See table for OV range on each unit.

Weight

net: 40 lbs
ship: 50 lbs

Size

Standard F package size 3 15/32" x 19 x 16 1/2" (H x W x D)

Products newsletter

Intel fills performance niche

Intel Corp., Santa Clara, Calif., plans to introduce its 8088—an 8-bit microprocessor with a 16-bit internal structure—at the Paris components show in April. The part is in effect an 8-bit version of the 8086 16-bit machine. It fits between the older 8-bit 8085 and the more advanced 8086 by offering **double the typical throughput of the 5-MHz version of the 8085 and about 75% of that of the 8086.** The 8088 executes the 8086 instruction set while retaining the multiplexed 8-bit bus interface of the 8085. Major application areas targeted by Intel include systems with low parts counts and high volume, upgrades from 8085-based designs, and byte-oriented equipment such as word processors and terminals.

Teradyne extends range of linear test system

Users of Teradyne Inc.'s J273 linear test system can now check out very high-frequency components with it, thanks to an optional new vhf synthesizer. Designated the M544-09, **the add-on covers the frequency range from 10 to 312 MHz and sells for $18,000.** The Boston company is also offering a vhf plug-in with a self-calibrating loop—the TL879—for $6,000. Socket adapters and a standard test package should also be available in the near future.

Synertek due out with CRT controller chip

Synertek Inc., Santa Clara, Calif., is getting ready to introduce its SY6545 cathode-ray-tube controller chip, which will interface with both the 6500 and 6800 families of microprocessors and **help simplify designs of intelligent terminals and personal computers.** Pin-compatible with Motorola's 6845 CRT controller, the Synertek device has an added feature: a transparent scheme for addressing read/write random-access memories that operates in either an interleaving (for simplified software) or a retrace-blanking (for simplified hardware) mode, according to Gary J. Summers, microprocessor group director.

The plastic version of this 40-pin unit, the SYP6545, will sell for $21 each for 100 or more; in the same quantities, the ceramic equivalent, the SYC6545, will go for $29.40. Samples should be ready in March, with production scheduled to follow by June.

Nine arrays ready, six need more work

The nine simplest programmable array logic devices (PALs) planned by Monolithic Memories Inc. are now available from the company's distributors, according to John Birkner, product manager for the Sunnyvale, Calif., firm [*Electronics*, July 6, 1978, p. 46]. MMI is still working on some process problems in the remaining six products, Birkner says.

Watch chip has large repertoire

Though some semiconductor makers are deemphasizing watch chips, American Microsystems Inc. expects to deliver about $2 million worth of its new model S3000 this year. The programmable C-MOS unit can directly drive six digits and 12 other indicators on a liquid-crystal clock face. What's more, **the silicon-gate device needs only an inexpensive quartz crystal for a reference oscillator and includes a voltage doubler and tripler that provide the high-voltage drive for the display.** According to the Santa Clara, Calif., company, the S3000, which is now available in sample quantities, will sell for less than $4 each in lots of 100,000.

Electrotechnical standards. The 1979 edition of the "Catalog of Publications" put out by the International Electrotechnical Commission contains a comprehensive list of all international standards as of Dec. 31, 1978. This 200-page catalog lists them in numerical order along with a short description of each. It is available in either English or French. The catalog sells for about $5.50 or 9 Swiss francs and can be obtained from the International Electrotechnical Commission, 1 rue de Varembe, 1211 Geneva 20, Switzerland.

Vacuum interrupters. Described in a 20-page catalog is a line of vacuum interrupters with voltage ratings from 5 to 38 kilovolts rms and fault current ratings up to 33,000 amperes rms, that are useful in industrial and rf-transmission applications. The catalog discusses their high speed, long life, and high dielectric recovery; it contains ordering information and specifications, which include mechanical data, mechanical requirements, and life. International Telephone and Telegraph Corp., Jennings Division, Marketing Department, 970 McLaughlin Ave., San Jose, Calif. 95122. Circle reader service number 422.

Selection chart. Listed on a chart are 30 bridge rectifiers with ratings between 1.5 and 30 amperes. The information includes the average rectifier current, operating temperature, peak surge rating, and type of connector used with each device. Electronic Devices Inc., Sales Manager, 21 Gray Oaks Ave., Yonkers, N. Y. 10710 [424]

Microwave components. Designed for engineers as a reference to a line of microwave components, the guide contains information on beam-lead diodes, capacitors, packaged diodes,

gallium-arsenide diodes, and gallium-arsenide field-effect transistors made with metal-semiconductor technology. Texas Instruments Inc., Inquiry Answering, P. O. Box 225012 (Attn: CL-392) MS-308 Dallas, Texas 75265 [423]

Minicomputer accessories. More than 800 minicomputer accessories, including line-printer ribbons, printwheels, computer paper, and products designed for data security and

protection, are described in a 64-page catalog. Several new items are also detailed in the 11th edition of the publication. Minicomputer Accessories Corp., Dept. P-10, 130 South Wolfe Rd., Sunnyvale, Calif. 94086 [425]

Test instruments. Described in a seven-page catalog are 10 different instruments that measure the plating and coating thickness of a material on any type of industrial or electronic component. The catalog provides a short discussion of each instrument along with a list of its features. The instruments use either the beta-backscatter, microresistance, eddy current, or electromagnetic induction test methods. UPA Technology Inc., 60 Oak Dr., Syosset, N.Y. 11791 [426]

Components. A 756-page catalog describes more than 100,000 electronic components from various companies. Electrical and physical specifications are provided for semiconductors, resistors, capacitors, potentiometers, circuit breakers, transformers, and other related electronic products. Newark Electronics, 500 N. Pulaski Rd., Chicago, Ill. 60624 [427]

Instrumentation tape recording. Designed for engineers and scientists who must evaluate, select, and use recording equipment, "Modern Instrumentation Tape Recording," a 140-page handbook, describes and explains the various elements in tape-recording systems. Some of the topics discussed are the physics of magnetic tape recording, direct recording of analog signals, frequency-modulation and digital recording of analog signals, selecting and specifying instrumentation tape recorders, and signal, format, and calibration standards. The handbook also includes line drawings, block diagrams, flow charts, oscilloscope photos, and other illustrations. The booklet is available for $6. EMI Technology Inc., 100 Research Dr., Stamford, Conn. 06906

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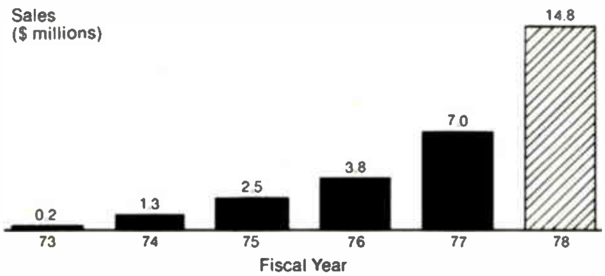

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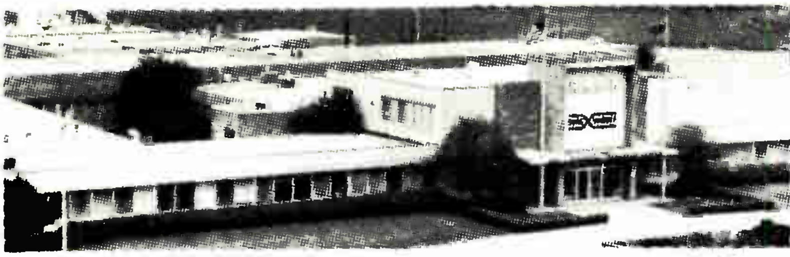

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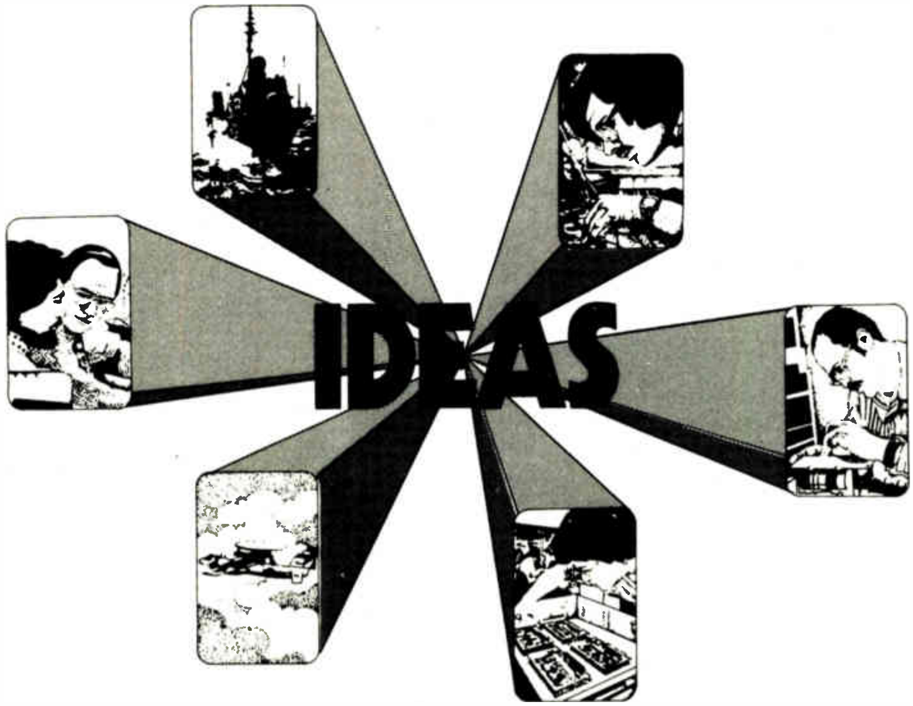

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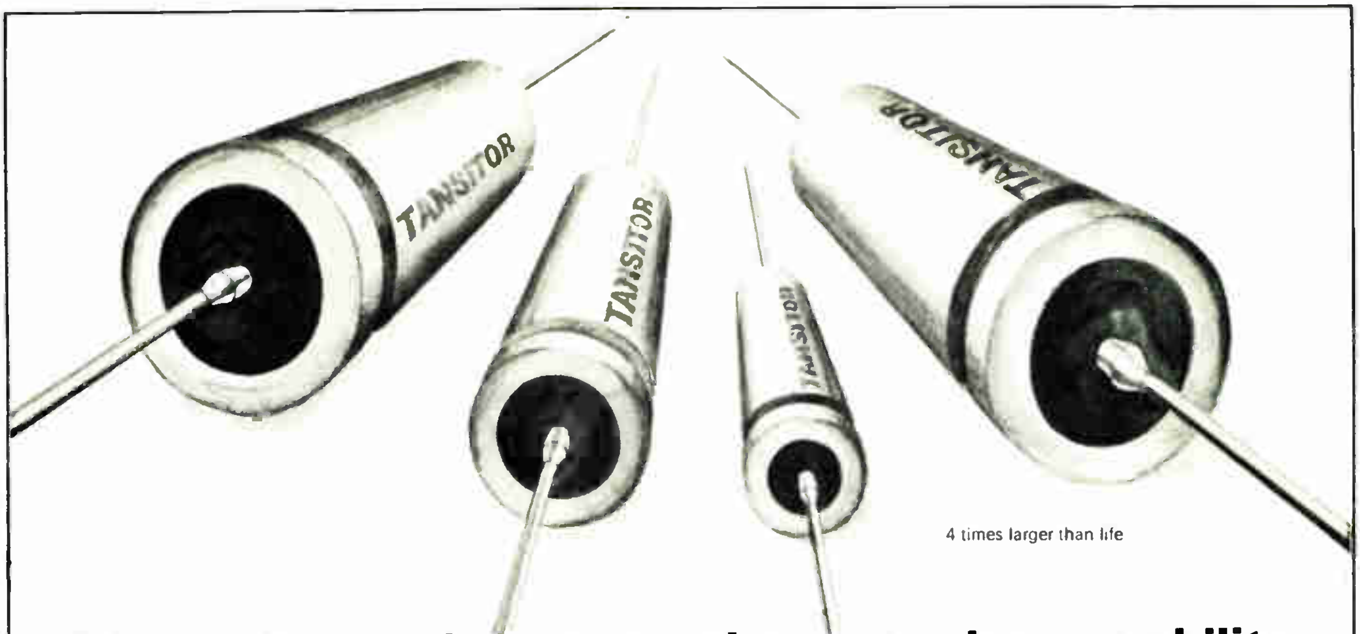

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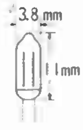

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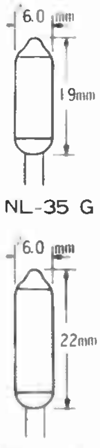

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10 25 40 55	70 85 100 115	130 145 160 175	190 205 220 235	250 265 342 357	372 387 402 417	432 447 462 477	492 507 712 954
11 26 41 56	71 86 101 116	131 146 161 176	191 206 221 236	251 266 343 358	373 388 403 418	433 448 463 478	493 508 713 956
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14 29 44 59	74 89 104 119	134 149 164 179	194 209 224 239	254 269 346 361	376 391 406 421	436 451 466 481	496 701 716 959
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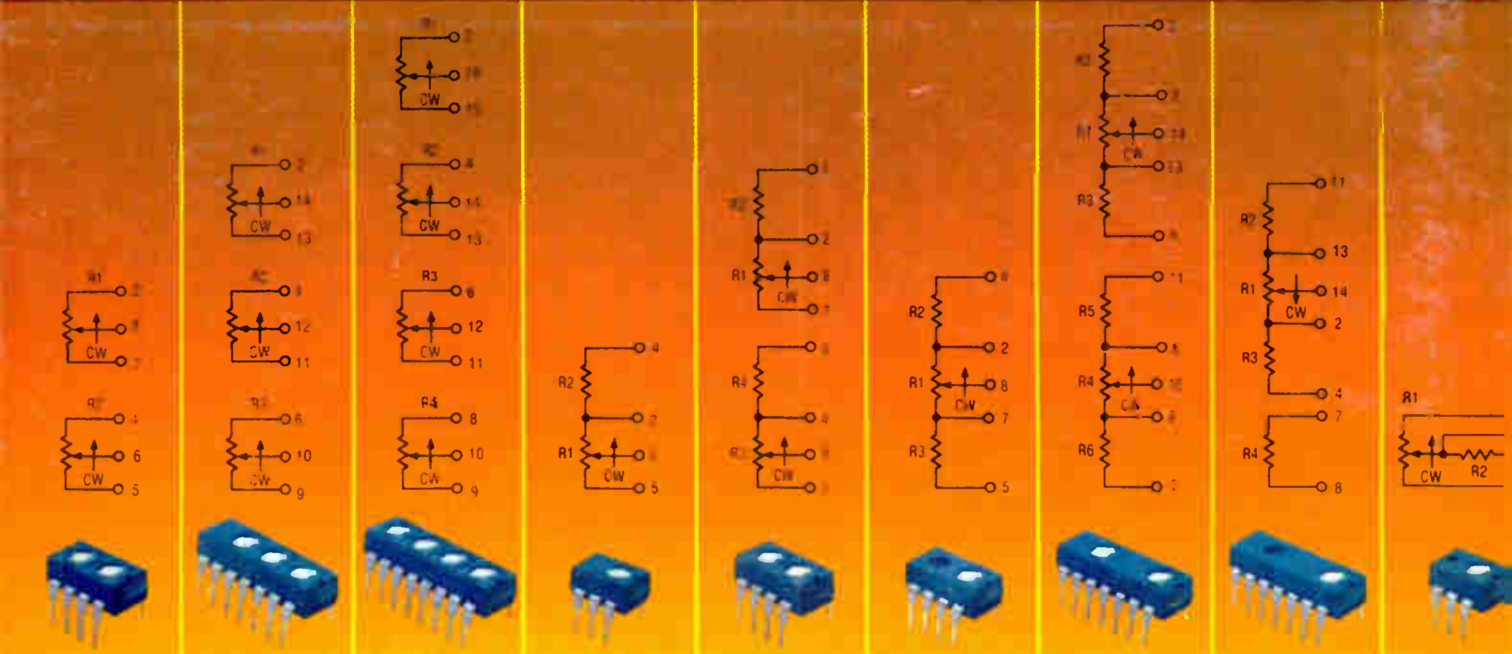

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