AUGUST 17, 1978

DUAL-PORT MEMORY HIKES I/O CONTROLLER BOARD THROUGHPUT/107

Bit-slice families, part 2: A look at the microcontrollers/96

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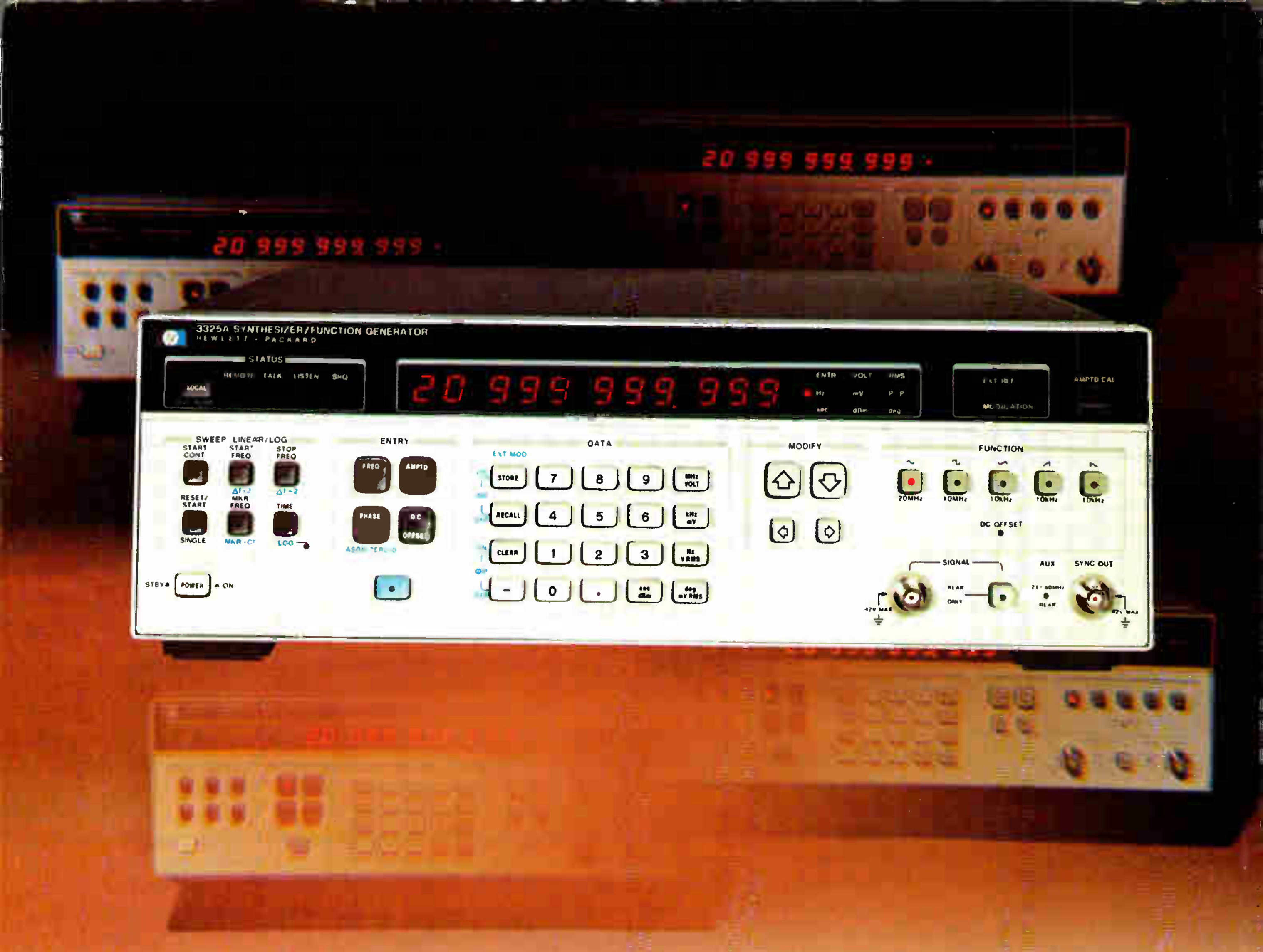

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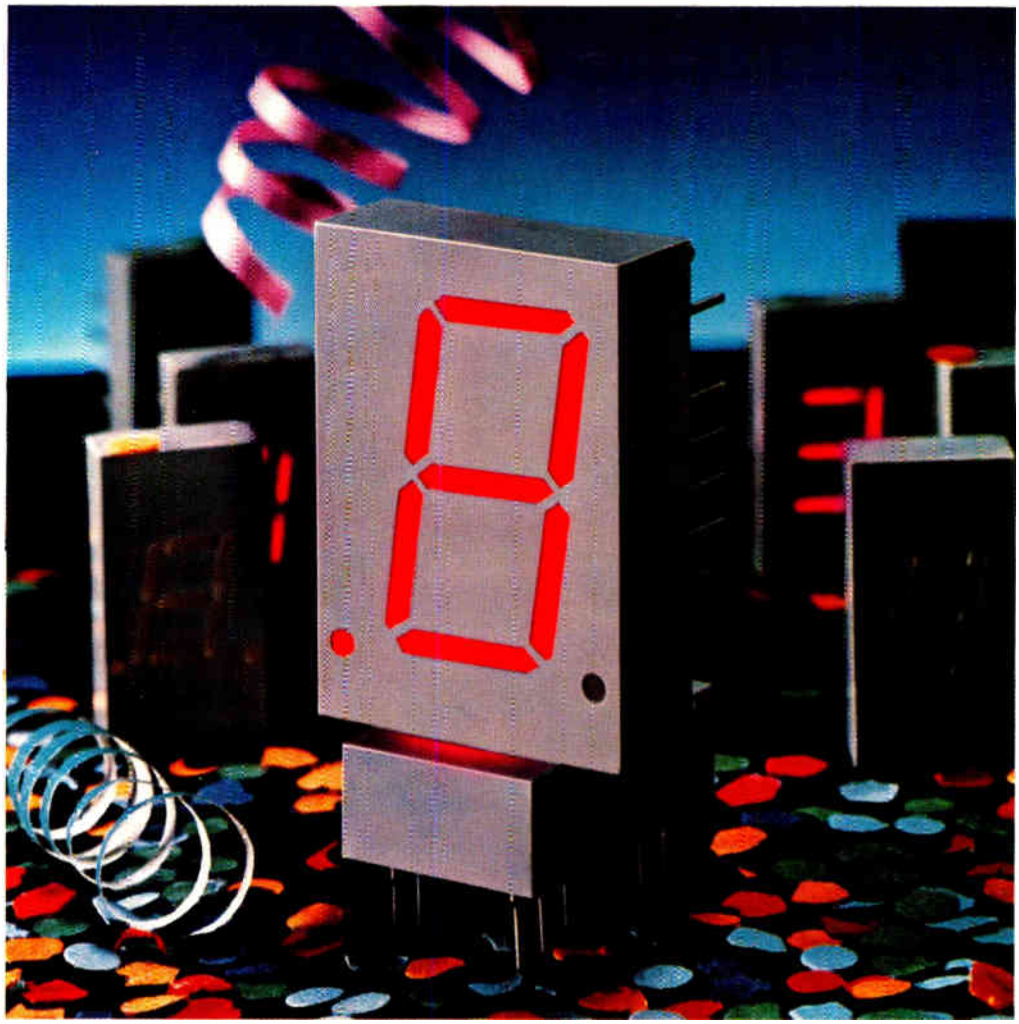

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Electronics
The International Magazine of Electronics Technology
Vol. 51, No. 17 • August 17, 1978

Highlights

Cover: Network cuts development system costs, 89
By sharing one disk and one printer among eight designers, a multistation microprocessor development system slashes the per-station cost of these expensive items. Moreover, each designer can be working with a different microprocessor.

Cover is by Robert Strimban.

Follow the rising yen, 78
With the Japanese government under pressure to hike imports in order to whittle away at $29 billion of foreign reserves, there's an opportunity growing for enterprising foreign manufacturers, including those in the electronics industries. This Probing the News is the inaugural of an occasional commentary on special areas of interest from *Electronics'* worldwide staff of reporters.

Bit-slice microcontrollers compared, 96
What could better follow last issue's rundown of bit-slice processor elements than a survey of the equally necessary microcontrollers? These comparisons will help designers pick their way through the maze of options available to them.

I/O throughput jumps with dual-port memory, 107
A random-access memory on a new input/output controller is also accessible from the system bus because of its dual port. Thus the controller looks like just another memory board to the host microprocessor, which can dump or receive data in much larger chunks than with I/O boards that have no dual-port RAM.

In the next issue . . .
The annual Wescon preview . . . speech synthesis on a chip . . . a new 8-bit one-chip microcomputer.

Electronics

Publisher's letter

While it's not unusual for *Electronics'* readers to contact authors of our articles to discuss the fine points, it is rare for such a contact to turn into a business. But that's what happened to Paul Page and Bruce Gladstone, now the heads of Futuredata and the coauthors of the cover article (p. 89) on a multistation microprocessor development system.

Gladstone wrote an article for *Electronics* on microprocessor applications that appeared back in 1973 when he was consulting for Varitel Inc. in Sherman Oaks, Calif. At the time Page was a computer systems designer working on a research project at the University of California at Los Angeles. Page read Gladstone's article and called him to talk about microprocessors.

This conversation eventually led to several joint consulting jobs. In 1975, when Varitel went belly up, the two formed a company to design a microprocessor development system. And in 1977 that operation became Futuredata: the result of a phone call to an author.

Another pair of authors in this issue are Tom Adams and Scott Smith. Part 2 of their evaluation of bit-slice microprocessor families (p. 96) takes a look at the microcontrollers that sequence instructions. By the way, Adams never worked for Raytheon, as we erroneously said in the last issue. Actually, he had been at the Applied Research Laboratories of the University of Texas from 1966 until recently. "But I was using bit-slices in a Navy submarine project to interface sonar equipment with Raytheon computers," he says.

Co-author Smith adds that, although their experience with bit-slices ran parallel, they were working independently and didn't meet until a mutual friend brought them together to prepare a general paper on the subject for a local IEEE Computer Society conference. That meeting led to our article.

During his many years in Japan as our Tokyo bureau manager, Charlie Cohen has seen many American companies enter the Japanese domestic market. Some have been successful, such as Texas Instruments and IBM in electronics and Kodak and Polaroid in photography. Some have been failures.

Thanks to the currency difference created by the rising value of the yen, there are opportunities now for American manufacturers to succeed in Japan, Charlie points out. He describes the topsy-turvy economic situation in Japan in Commentary, a new feature inaugurated in this issue (p. 78).

We plan to run these personal observations of our editors whenever a subject merits analysis. Certainly the situation in Japan merited a Commentary, and Charlie Cohen is in a unique position to sort out the complexities.

"One thing that's clear in all the seeming confusion of the last year," he remarks, "is that the Japanese market is freer than it has ever been."

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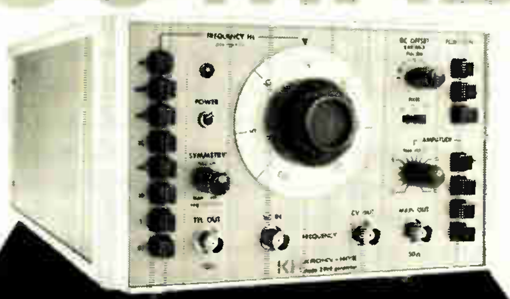

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Readers' comments

More help for the handicapped

To the Editor: Having read the interesting articles "Communicator aids palsy victims" [May 1, p. 42] and "Communicators help the handicapped" [June 8, p. 94], I feel that you and your readers should know that a very useful communication system has been developed at the Electronics Laboratory of the Technical University of Denmark and has been manufactured for about two years by ELMI A/S, Copenhagen.

This communicator, called the Vidialog system, enables all types of motor-handicapped persons to write and draw on common TV screens by use of an interface, which can be adapted to each individual handicap. Vidialog is particularly suited for communication with patients who, regardless of etiology, have become severely motor-handicapped or even paralyzed, either for life or temporarily, and for teaching and communicating with spastic children.

Via the interface unit, the motor-handicapped person can select characters from a character display, which is shown on the upper part of the TV screen. Writing errors can easily be corrected, and the written text may be edited.

Virtually every imaginable type of interface may be connected to the Vidialog system. Even almost totally paralyzed patients will be able to use a touch-operated control, a suck/blow contact, or an eye-wink detector. Spastic persons with violent and involuntary movements may use an area selector consisting of a plate with five sectors, which are to be touched with a stick or a special glove. Patients suffering from muscular dystrophy may use an isotonic joystick, an easily moveable stick.

A particular alphabet display on the TV screen corresponds to each interface unit. In each display, the letters are organized in such a way that those most frequently used are nearest to the starting position, optimizing the writing speed. The correct alphabet is automatically displayed on the screen when the interface unit is connected to the control unit.

Via a keyboard, a teacher or instructor can write on the TV screen or make corrections. All functions, including the recording of alphabet displays or words, are carried out from the keyboard.

It is also possible to make simple figures and drawings on the TV screen and to make drawings on a transparency placed on the screen, which has proved useful in teaching and communicating even in the case of retarded spastic children.

In your June 8 article, Mr. Derek Rowell says his Unicom "is the first unit for the handicapped that will allow messages to be edited." As mentioned above, the Vidialog system already has this feature.

Björn Jarkler
Electronics Laboratory
Technical University of Denmark
Lyngby, Denmark

Reflections

To the Editor: Users of Mr. McDonald's microwave setup ["Mismatched waveguide calibrates VSWR scope display," June 22, p. 146] may experience difficulty in measuring values of less than 1.5 or so for the voltage standing-wave ratio. Because in many commercial systems the maximum VSWR must be well below this number, such a configuration will have limited usefulness, the reason being that the input VSWR of commercial attenuators will be much too high to permit accurate calibration of the test setup at the low VSWR values. The VSWR values for the best attenuators I could find by glancing through catalogs, was 1.2-to-1 to 1.5-to-1, and some were higher.

I suggest that the attenuator be placed before the directional coupler so that the VSWR of the attenuator will not make the calibration inaccurate. The attenuator will then read return loss directly.

L. Quick
Chester, N. J.

Correction

Before you rush to order Nippon Electric Co.'s new 64-K read-only memory, be advised that the quantity price is $50 each, not the $1.50 listed on page 65 of the Aug. 3 issue.

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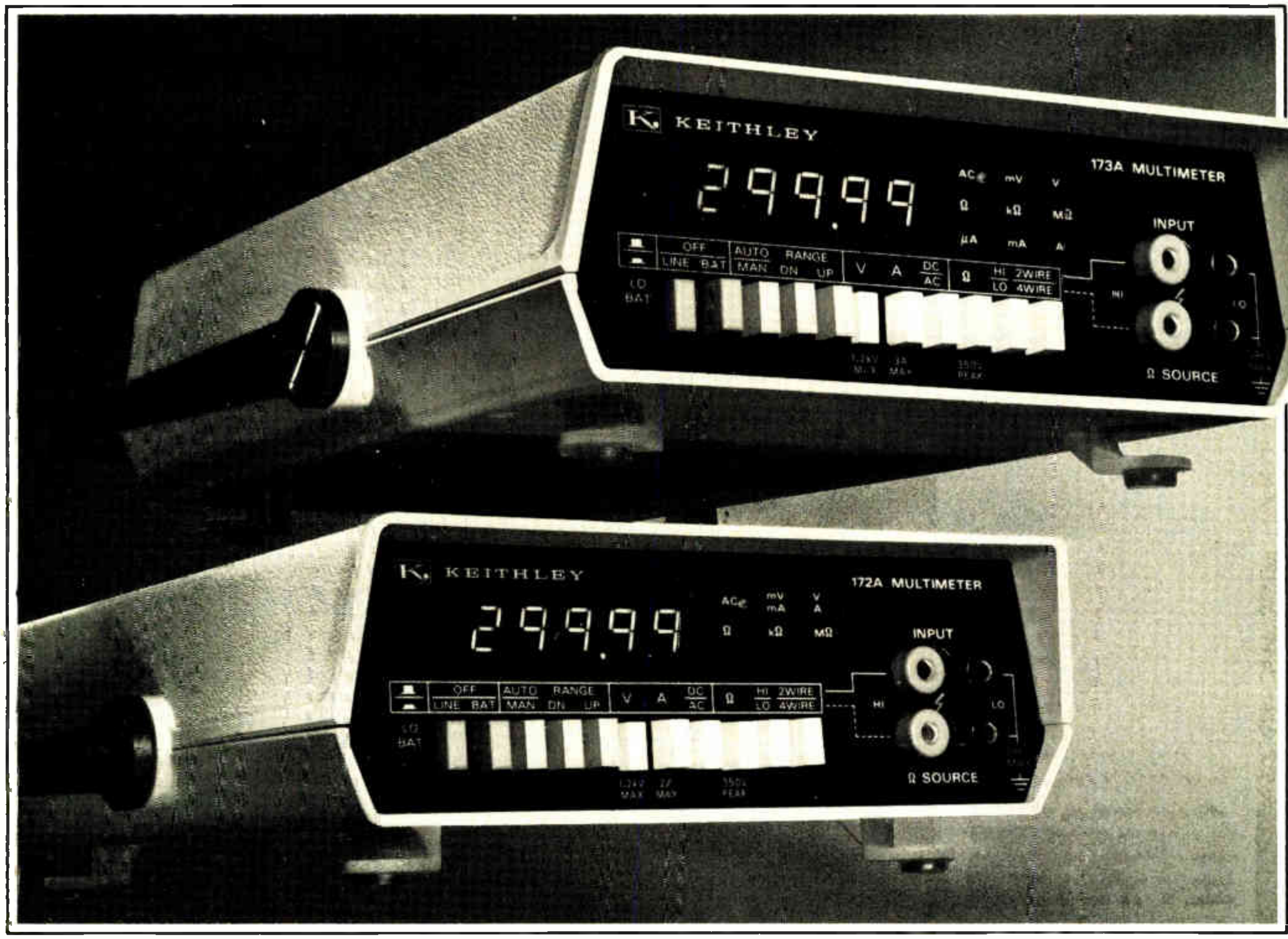

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News update

■ General Telephone & Electronics Corp. of Stamford, Conn., is stepping up research into flat-panel displays, "an area that could lead to the next generation of television sets," predicts a spokesman for the corporation.

To work with its engineers on the necessary development, GTE has signed a three-year contract with Lucitron Inc. of Chicago. Lucitron is the research organization recently established by three former Zenith Radio Corp. scientists [*Electronics*, July 6, p. 50].

According to George Konkol, president of GTE's Consumer Electronics group, the objective is to develop a technology for producing the kind of flat, thin displays that will be suitable for large-screen color television and other commercial applications.

He adds that Lucitron will be working closely with GTE Laboratories in Waltham, Mass., and with GTE Sylvania television and picture tube engineers in Batavia and Seneca Falls, N. Y.

Lucitron president Joseph Markin hopes to have a 3-inch-thick panel with a 5-inch diagonal available for demonstration shortly. Planned for the early 1980s are displays that will measure more than 25 inches diagonally across and will have prices upwards of $5,000.

■ RCA Corp. is becoming more aggressive about selling its personal computers. Its Electro-Optics and Devices division in Lancaster, Pa., which recently took over the marketing of the company's home computers, has lowered the price of the Video Interface Processor [*Electronics*, March 31, 1977, p. 94]. As a result, a fully assembled black-and-white VIP now costs $249 instead of $299.95.

In addition, the division is planning to bring out a related product about once a month. Supplements will include a fully alphanumeric keyboard, a low-cost printer, and a color version of VIP with better sound.

Bruce LeBoss

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CA3140	0V to $(V^{+}-3V)$	1V to $(V^{+}-3V)$ $R_L=2K\Omega$	50pA	9V/μsec	Op Amp
CA3160	0V to $(V^{+}-10V)$	10mV to $(V^{+}-10V)$ $R_L=\infty$ 10mV to $(V^{+}-3V)$ $R_L=2K\Omega$	50pA	10V/μsec	CA3130 with internal compensation
CA3240	0V to $(V^{+}-3V)$	1V to $(V^{+}-3V)$ $R_L=2K\Omega$	50pA	9V/μsec response time	Dual CA3140
		V_{IO}			
CA3290	0V to $(V^{+}-3.8V)$	20mV	50pA	100V/μsec	Dual Comparator

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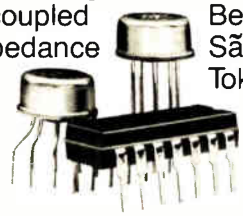

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People

SOS microprocessors due soon, says RCA's Ahrons

It used to be that the extra price charged for silicon-on-sapphire circuits had a lot of people deciding not to buy them. But that price premium is going by the wayside, and the accelerated interest in SOS that should result is part of the reason Richard W. Ahrons is back where he put in much of his professional life—at RCA Corp. Indeed, he is at the Solid State division in Somerville, N. J.

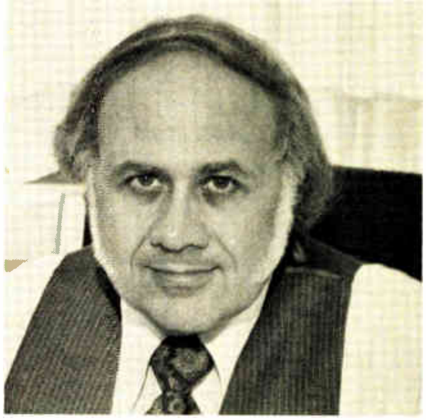
RCA has developed its sapphire-ribbon-growing capability to such an extent that SOS devices will be as low in cost as those produced on bulk silicon, according to Ahrons, who has just taken on the newly created post of manager of microprocessor and memory product marketing and support engineering. At RCA this means complementary-metal-oxide-semiconductor technology; in microprocessors, it means its 1800 family, as well as upcoming 8048 and 8085 designs it obtained in a licensing agreement with Intel Corp. [*Electronics*, April 13, p. 41].

"The price would be the same independent of whether the part's on sapphire or on silicon," says Ahrons, holder of a Ph.D. with a double major in communications and computers.

Hence, for RCA there's no point in making the devices on bulk silicon, he continues. Using the sapphire substrate offers higher-frequency C-MOS circuits with higher noise immunity and wider temperature range than is possible on a silicon substrate.

The SOS microprocessors, the first to be marketed, will start to be available by the end of the year in sample quantities, Ahrons says. A single-chip 1804 with an expandable memory will come first, with an 8085 due in the first quarter of 1979.

"I see a great future for the C-MOS microprocessor and its low-power capabilities, and especially so when it's built on a sapphire substrate," predicts Ahrons, who rejoins RCA after spending three years at Motorola Semiconductor in Austin, Texas, primarily as manager of C-MOS market planning and applications. Earlier, he spent 10 years at RCA's Sarnoff Research Center and 5 years at the Solid State division, leaving in 1969 after becoming manager of advanced applications and devices.



SOS man. Ahrons sees no premium for C-MOS microprocessors on sapphire.

RCA is in the forefront of C-MOS microprocessor development, "and our plans are to stay that way," he says. "It's the reason I came East."

Repackaging is as important as technology: Jud Gilbert

Innovation doesn't necessarily come from novel changes in circuitry, according to Jud Gilbert, Prentice Corp.'s new vice president of engineering. Coming up with a fresh approach to functionality and packaging can be as innovative as designing in the latest technology, the 38-year-old executive believes.

Gilbert hopes to exploit this philosophy to make small and medium-sized time-division multiplexers and port-contention devices more beneficial to the user. "Small TDMs are getting smarter, just like the big 150-channel types, because they are being designed with microprocessors. But instead of making the small [4- or 8-channel] TDMs in modular fashion, they are more like black boxes," explains Gilbert, who previously managed product lines at Racal-Milgo Inc. and General DataComm Industries Inc. The upshot is

People

Adapter. Small units may benefit from big system design, Gilbert says.

that they are hard to service and prone to obsolescence, he says.

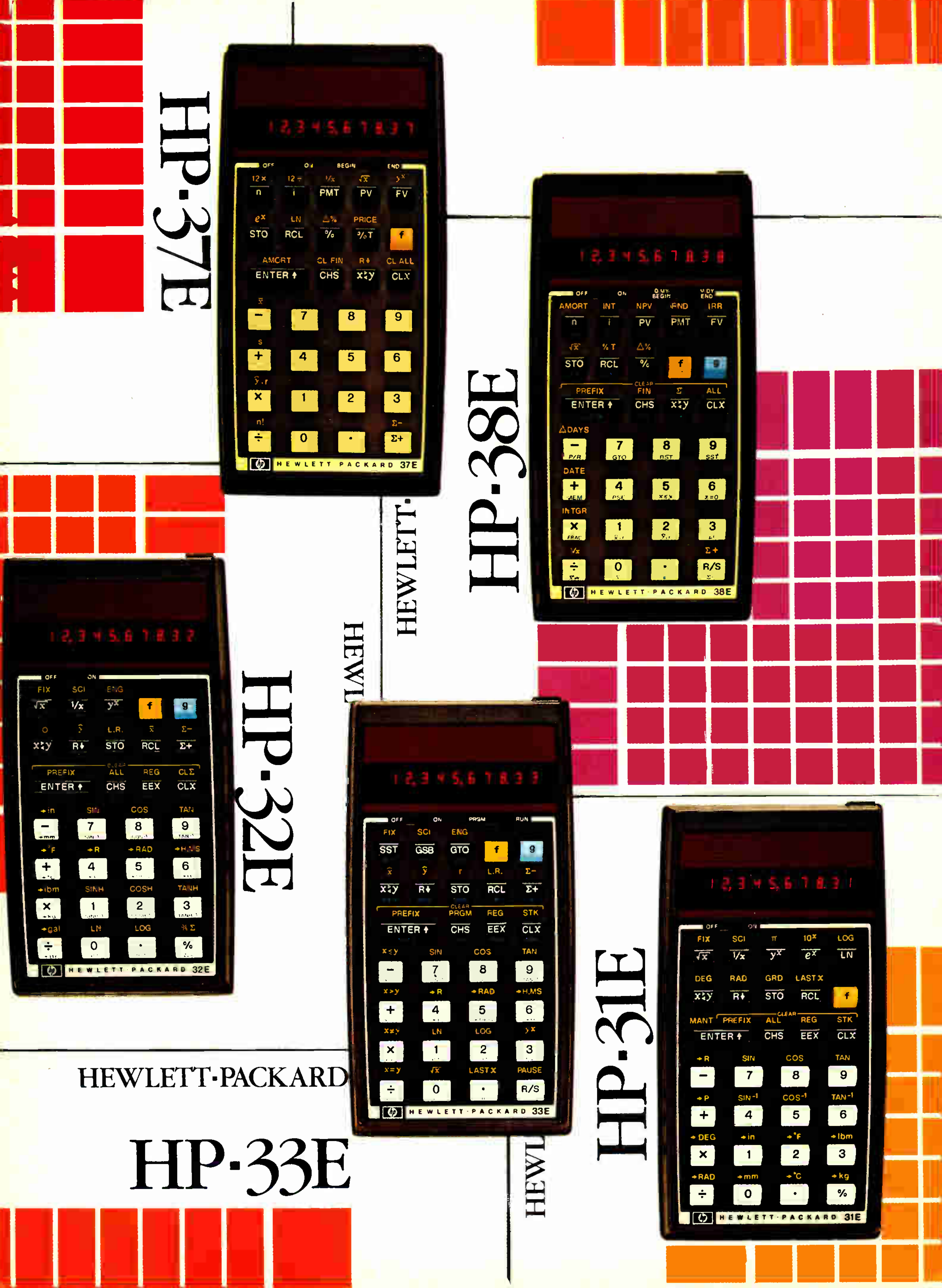
Modular adaption. Instead, Gilbert would like to adapt the modular architecture of medium and large multiplexing systems to the smaller ones. "This would not require circuitry changes, only a change in packaging," he asserts.

For port-contention devices, which manage the access of a number of lines to a smaller number of ports, Gilbert envisions being able to replace the switching algorithms. His choice for a replacement is one similar to that used by the telephone company.

Until now, the Palo Alto, Calif., firm has scratched out a small niche in the telecommunications market with low-speed modems, inexpensive short-haul (up to 5 miles) modems, and frequency-division multiplexers. Moving into TDMs and PCDs takes an infusion of expertise.

"That is one of the reasons I was appointed," Gilbert says. "Prentice viewed my background in high-speed modems, TDMs, and terminals as a good complement to its engineering group's expertise in the other areas." Can this small company, with $4 million a year in sales, develop both these new products?

"If we do the job right, there's no reason why we can't," Gilbert maintains. "The hardware is nearly identical; the bulk of the development will be firmware and software." □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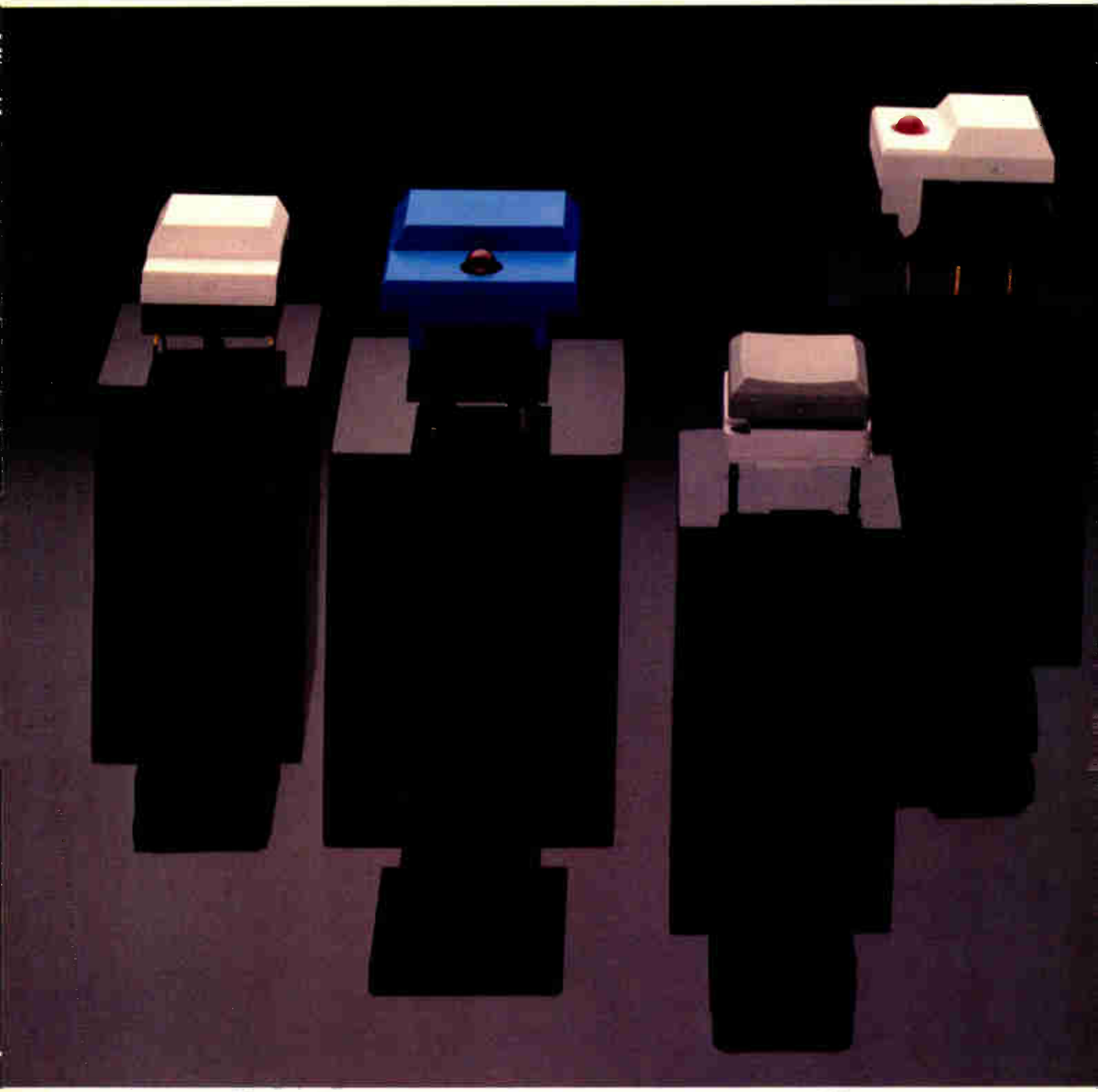


Ask for switches by our

Editorial

Doing more business in Japan

Hakuraihin is a sweet-sounding word to the Japanese. It literally means a product that has arrived by boat, and its existence underscores a long-held fondness in Japan for foreign-made products. Now the rapidly rising value of the Japanese yen seems to be encouraging "pacific overtures," as Admiral Perry phrased it, in the way of increased American sales to Japan.

There is even some confidence these days that the U. S. will be able to negotiate more favorable tariff rates for certain electronics products imported by Japan — integrated circuits, computers, and peripheral equipment — as a further stimulus to trade. The question is: will the electronics companies make the most of the situation?

A few well-known companies have taken the risks and accepted the headaches of doing business in Japan and are now in a position to increase their market shares. These established firms have learned that the Japanese market is a difficult one in which to get started. It is not a market for short-term or one-shot deals. To make a go of things in Japan requires good planning and determination, which is why many American companies will pass up the opportunity presented. The commitment required may be too great in view of the rather flat market today in Japan, with its tough domestic competition.

Nevertheless, the opportunity exists for all-out marketing tied to solid engineering support, two of the U. S. electronics industries' strengths. It has been a long time since Admiral Perry's famous black ships opened up Japan to increased trade. Maybe the time has come for the electronic black boxes from America to do the same.

Toward a high-level language

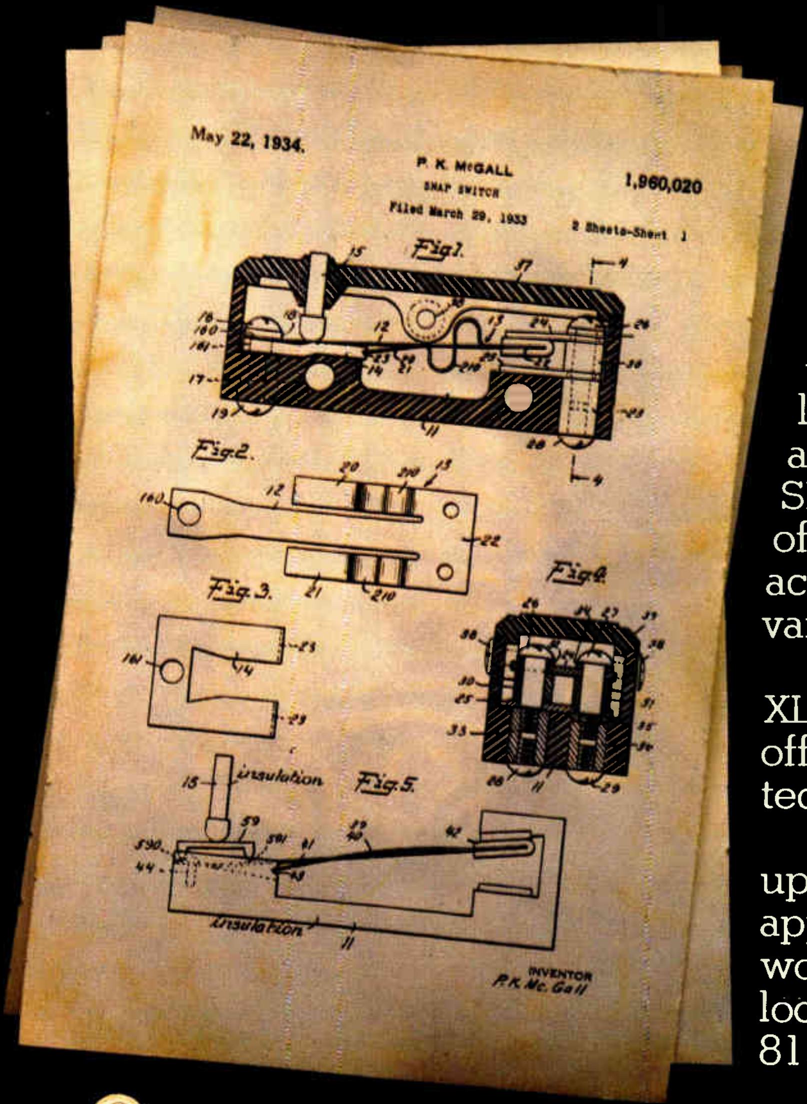
The Department of Defense's effort, the DOD-1 program, to develop a standard high-level language is entering its final phase. Two firms, Intermetrics in Cambridge, Mass., and CII-Honeywell Bull, a French affiliate of Honeywell Inc. in Minneapolis, have been encouraged to complete the languages they have been working on and to deliver compilers by next spring.

Neither company is obviously the leader. Both proposals have advantages and disadvantages, although Intermetrics might have an edge because the company has delivered other compilers to DOD. The main need is for the project to proceed without delay because the language could have a major impact on the software of the 1980s.

It will be the first time that DOD will have a highly readable language. "In the past, the languages have been too machine-dependent and oriented toward writability," an industry spokesman points out, adding "it will cut down on the cost of program development and maintenance." This point makes sense because a look at software expenditures shows maintenance is on top. So the language is targeted at easing the software cost problem.

DOD-1 may not be the answer to all the Pentagon's software problems, but it's a good, practical start. The language has an excellent chance for success. Its worth will be appreciated inside and outside DOD.

Since we made them first, we know how to make them last.



Back when we invented the basic snap-action switch, it was the only product we made. But it wasn't all we had to sell.

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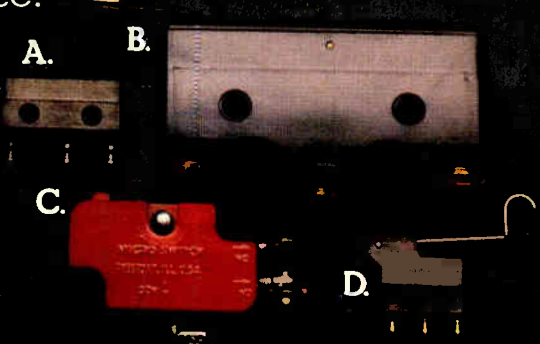

A. Type SM–invented 1950.
B. Type BZ–invented 1932.
C. Type V3–invented 1945.
D. Type SX–invented 1958.

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Meetings

Eighth European Microwave Conference, Microwave Exhibitions and Publishers Ltd. (Sevenoaks, Kent, England), Hotel Meriden, Paris, Sept. 4–8.

CompCon 78—17th IEEE Computer Society International Conference, Capital Hilton Hotel, Washington, D. C., Sept. 5–8.

Fiber Optics and Communications Exposition, Information Gatekeepers Inc. (Brookline, Mass.), Hyatt Regency O'Hare Hotel, Chicago, Sept. 6–8.

International Machine Tool Show 1978, National Machine Tool Builders' Association (McLean, Va.), McCormick Place, Chicago, Sept. 6–15.

Wescon/78 Show and Convention, Electronic Conventions Inc. (El Segundo, Calif.), Los Angeles Convention Center, Los Angeles, Sept. 12–14.

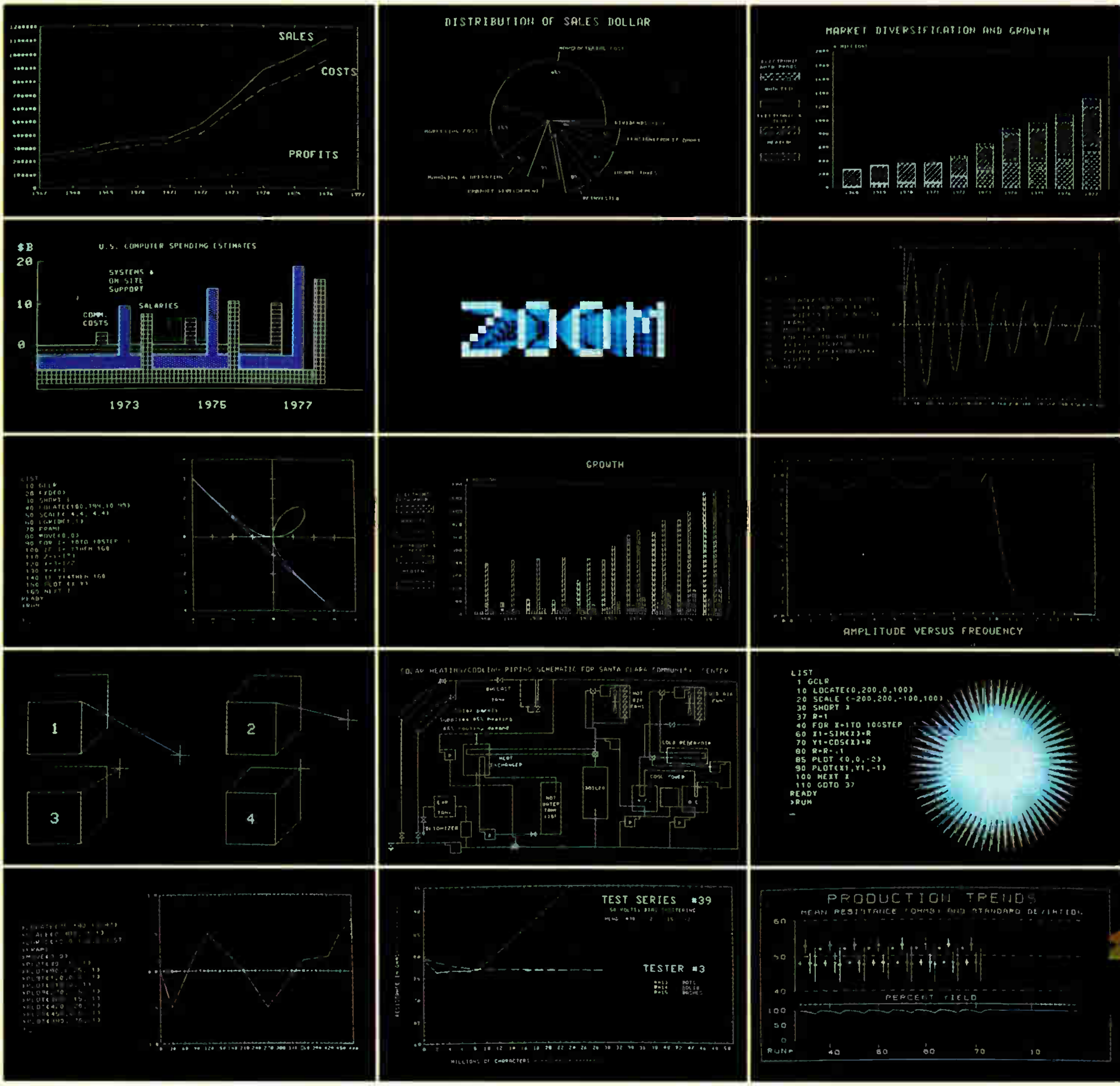
ECOC—Fourth European Conference on Optical Communications, IEEE Italian Section (for information, contact Istituto Internationale Comunicazioni, Genoa), Genoa, Italy, Sept. 12–15.

Conference on Information and Systems Theory Used in Digital Communications, IEEE German Section (for information contact VDE-Zentralstelle Tagungen, Frankfurt), Technical University, West Berlin, West Germany, Sept. 18–20.

ESSCIRC 78—Fourth European Solid State Circuits Conference, IEEE Benelux Section (for information contact ESSCIRC 78, Delft University of Technology, Delft), Tropen Instituut, Amsterdam, the Netherlands, Sept. 18–21.

Sixth Computer-Aided Design and Computer-Aided Manufacturing Conference and Exhibition (CAD/CAM VI), Society of Manufacturing Engineers (Detroit), Hyatt House, Los Angeles, Sept. 19–21.

Graphics. Without



graphics software.

You just lost your last excuse for sticking with alphanumerics. Because with HP's new 2647A Intelligent Graphics Terminal, you get graphics without digging into your CPU's software.

A picture's worth a thousand numbers.

On an alphanumeric terminal, your data's just a screen full of numbers. But with the 2647A you can plot tabular data as a bar graph, or a pie chart, or a linear or logarithmic line graph. Quickly, with just a few keystrokes.

Now you can really see your data, not just look at it.

What's more, with the 2647A you can zoom in and out. Pan right, left, up, down. Selectively erase. Shade important areas to make them stand out. Use a rubber-band line to make a quick sketch.

Without any help from your programming department.

It's more than smart.

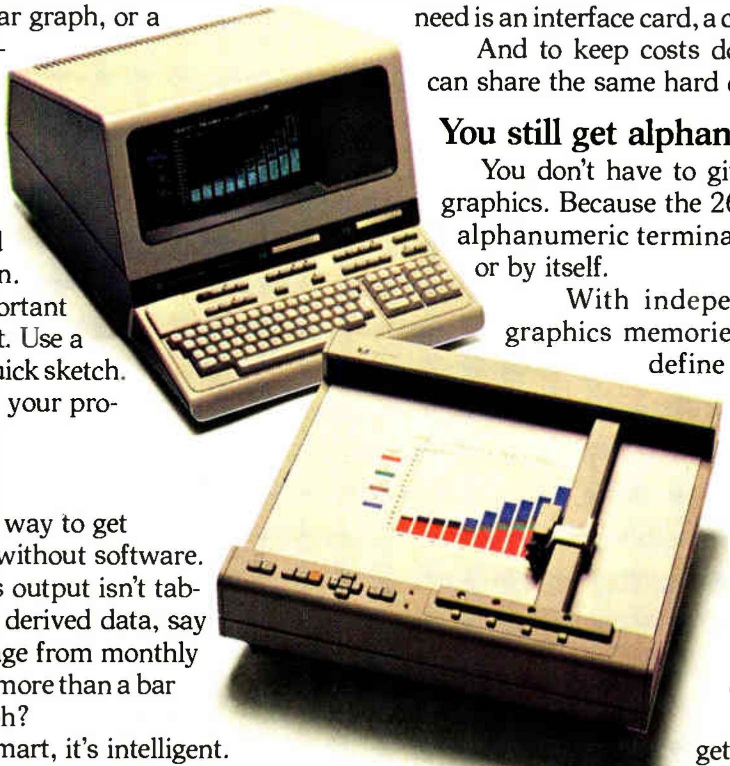
The 2647A's the smart way to get graphics from tabular data without software.

But what if your CPU's output isn't tabular? Or if you'd like to plot derived data, say a three-month moving average from monthly sales figures? Or if you need more than a bar graph, pie chart or line graph?

The 2647A's not just smart, it's intelligent.

You can program it to reformat data from your CPU, or to compute more data, in easy-to-write BASIC. And you can program it in AGL, our high-level graphics language extension of BASIC. Its powerful commands, such as FRAME, AXES, LABEL, LOCATE and PLOT, put sophisticated graphics at your fingertips.

Either way, your program runs on the 2647A without any help from your CPU.



Hard copy's easy.

How do you get graphics into your briefcase?

The 2647A makes graphics as portable as alphanumerics. It interfaces easily with our 9872A Four-Color Plotter (which can even make overhead transparencies), and with our 7245A Thermal Plotter-Printer. All you need is an interface card, a cable and the peripheral itself.

And to keep costs down, more than one 2647A can share the same hard copy peripheral.

You still get alphanumerics.

You don't have to give up alphanumerics to get graphics. Because the 2647A's also a programmable alphanumeric terminal for interactive use on-line or by itself.

With independent alphanumeric and graphics memories. Eight soft keys you can define to do several steps with a single keystroke. A bright, easy-to-use, high resolution display. And built-in dual cartridge tape drives for 220K bytes of mass storage.

Best of all, the 2647A with full memory and data communications interface costs only $8300.*

Which makes it easy to get the picture.

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Alice: *"Where's the best place to begin?"*
Hatter: *"At the beginning."*

Charles Dodgson, better known by his pen name, Lewis Carroll, was born 100 years too soon. He would have loved the electronics industry.

A well-known mathematician and logician whose writings on symbolic logic contributed to the development of Boolean logic, he was fond of expressing logical thought in illogical situations. For example, consider this exchange at the famous Tea Party in *Alice in Wonderland:*

> "Take some more tea," the March Hare said to Alice.
>
> "I've had nothing yet," Alice replied, "so I can't take more."
>
> "You mean you can't take *less*," said the Hatter, "it's very easy to take *more* than nothing."

PMI would have offered Carroll a job as a design engineer, since the Mad Hatter's logic expresses our approach to linear circuits:

"The *more* there is of ours, the *less* there is of theirs."

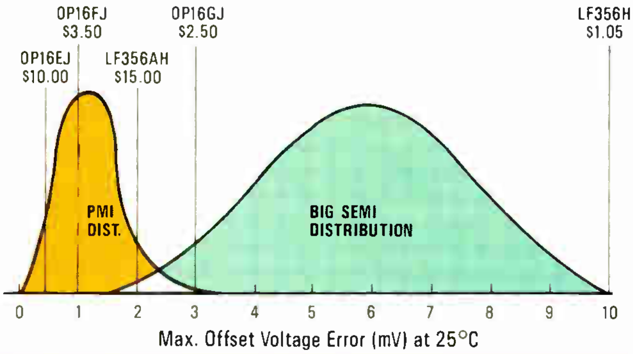
Translated, that means the superior quality of our linears results in a lower reject rate, so the user needs *less* of our product to get more for his money.

Carroll also liked to take very illogical thoughts and express them in a way that made them seem logical, as in *Through the Looking Glass* when the White Rabbit reads a poem:

> "They told me you had been to her
> And mentioned me to him:
> She gave me a good character
> But said I could not swim."

That thought is very well written but makes no sense at all. With that kind of talent, Carroll could have commanded top dollar as an advertising copywriter for any of the Big Semi companies, where they always manage to come up with a lot of reasons for buying linear IC's besides the most important reason; precision performance.

EXAMPLE: 0-70°C BIFET OP AMPS-100 Pc US OEM PRICES NOTED



If Lewis Carroll were writing his nonsense stories today, his "Wonderland" might well be the nonsensical world of linear integrated circuits. Alice might be a purchasing agent lost in a maze of confusing product claims from the Mad Hatter (sales manager for one of the Big IC houses) and the March Hare (the industry's largest linear distributor).

You'll meet them all in the next few months—as well as Tweedle Dum and Tweedle Dee, the Mock Turtle, and even the frumious Bandersnatch—as PMI leads you through some New Adventures in Linear Wonderland. It's a topsy turvy place where "miraculous" products appear mysteriously in print and disappear just as mysteriously when you try to find them, like the Cheshire Cat. A place where buyers are talked into believing that what they get is what they like, instead of the other way around, as even the Mad Hatter knows it should be. And, above all, a place where races are run with price instead of performance so that the winner is often the runner who never begins, as the Dodo explained to Alice.

Along the way, you'll also meet PMI's linear products. The op amps, comparators, multiplexers, voltage references, D/A converters, and sample-and-hold amplifiers whose *precision* performance boosted our sales 65% in 1977 while the linear market grew by only 28%. ("O frabjous day! Calooh! Callay!")

You'll find out how we achieve precision performance by using manufacturing steps some other companies don't feel is worth it, such as the use of silicon nitride passivation and zener zap trimming, giving us a sharp competitive performance edge. ("Off with their heads!", as the Queen would say.)

Does all that precision cost more? Yes and no is the logical answer to that, remembering that in Linear Wonderland more is often less. A few pennies more invested in quality components results in a better quality system with less problems for the OEM.

That's why PMI is committed to quality, which leads us to the real key to our success: we only enter races we know we can win. That's the reason we never enter a second source race unless we've found a way to get substantial improvement in performance. It's also why we don't get into jelly bean counting races and only run against the Big Semi companies when we know our LOWEST grade is equal in performance to their HIGHEST grade. We already know what Alice had to learn: "It's easier to win when no one else begins."

So come through the looking glass into Linear Wonderland with PMI. To get you started, we've published a new short form catalog of PMI's Linear Wonderland products. This will give you an overview of all the exciting precision linears which you will be reading about soon. Just fill in the coupon and ask for your "PMI Guide to Linear Wonderland."

Carroll's Wonderland was a place where you had to run as hard as you could just to stay in one place.

"If you want to get somewhere else, you must run at least twice as fast as that," the Queen told Alice.

PMI is dedicated to running fast enough to get ahead and stay ahead in Linear Wonderland.

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8E5031

TRW brings out 6-bit a-d converter for nonbroadcast video

Encouraged by the success of its one-chip, 8-bit analog-to-digital converter in the broadcast television market, TRW's LSI Products division is bringing out a version at a lower price with less resolution for nonbroadcast video applications. **The 6-bit resolution TDC 1014J consumes only ¾ W, yet does video-speed conversion without need for an external sample-and-hold circuit.** It's sold in a 24-pin ceramic dual in-line package and features a 30-MHz sample rate. The device requires only a single command to digitize an analog waveform between 0 and −1 V. On chip are 63 strobed comparators, encoding logic, and a 6-bit data latch with TTL outputs. The price for 100 or more is $186 per unit, compared with $550 to $600 for the 8-bit converter. With sales of over 1,000 units in its first two months, the 8-bit device is the hottest item for the Redondo Beach, Calif., division.

TI soups up I²L microprocessor, adds MOS 8-bitter

The SBP9900 microprocessor, Texas Instruments Inc.'s 16-bit processor built with integrated-injection logic has become the SBP9900A to denote an increase in speed from 2 to 3 MHz. Refinements in the input/output section, including the use of some multilevel logic, are chiefly responsible for the improvement, according to the Houston Digital Circuits division. **Meanwhile, the MOS 9900 family has a new addition: The TMS9985, which is an 8-bit version aimed at the high-performance 8-bit market dominated by Intel's 8085.** Available for sampling next month, the 9985 looks internally much like a 9900 but has 256 bytes of random-access memory on board plus an 8-bit-wide data path. It's housed in a 40-pin plastic package.

Datapoint upgrades processor, starts software field tests

To increase the capability of its entry-level equipment, Datapoint Corp. is doubling the cathode-ray-tube display to 1,920 characters, increasing the memory to 64 kilobytes, and coupling the processor with two double-density floppy drives for a total of 1 megabyte of diskette storage. The new processor, due out next month, will be called the 1800 and can stand alone or be used as part of the San Antonio, Texas, firm's ARC network architecture. **A key use for the larger screen size on this unit and the recently introduced 3800 and 6000 gear is in word-processing applications.** Datapoint is currently field-testing an improved version of its Scribe word-processing software. The new version is expected to be introduced before the end of the year, along with an in-house-built daisy-wheel printer.

Mostek readies dynamic RAM that's pseudo-static

It's got the size and price of a dynamic random-access memory, but it looks and behaves like a static one. That's the 4816, the new 2,048-by-8-bit RAM that Mostek Corp., Carrollton, Texas, will be providing samples of soon. Though built with single-element dynamic cells, the 29,000-mil² die contains on-chip refresh counter circuits. **Thus it refreshes itself in the power-down state but needs external refreshing when accessed.** Small for a 16-K RAM, the n-channel device is more like a 4-K static in size. It has a 100-ns access time typically and is designed for 5-V operation. Sample quantities are due in November, according to the firm.

Electronics newsletter

Programmable VCR, color cameras added by RCA

Confident that industry shipments of video-cassette-recorder units will pick up substantially in the second half of 1978, RCA Corp. is expanding its line of SelectaVision products with the addition of two new players and two home video color cameras. **A VCT400 player, carrying an optional retail price of $1,275, can be preprogrammed to record up to four television programs on different channels during a seven-day period.** It is made to RCA specifications by Matsushita Industrial Co. of Japan, as is a new $1,075 VCT201 player having an electronic timer that allows the user to preset not only the time and channel for unattended recording, but also the time at which recording should end.

Fourth fiber-optic test system set in Canada by GT&E

General Telephone & Electronics Corp.'s tests of fiber-optic communications systems will shift into high gear later this year with the company's fourth field installation in 15 months. **The latest link, to be placed in the regular Vancouver, British Columbia, telephone network, will carry up to 672 separate conversations on two fibers—one for each transmission direction.** The 4.4-mile no-amplifier route through existing underground ducts will be tested for a year at least and will provide GT&E with more data on reliability and economy to add to that previously obtained in California, Hawaii, and Belgium.

Energy-storing solar cell uses low-cost materials

Researchers at Optel Corp. in Princeton, N. J., are developing a photoelectrochemical solar cell that not only converts solar energy to electricity when the sun is shining but, uniquely, stores energy at the same time. Unlike most solar cells that use expensive single-crystal materials or photocrystalline substrates, the Optel cell uses three photo-anodes made with relatively inexpensive cadmium-selenide thin films. **One anode stores electrical energy during solar irradiation and can be connected to a common electrode to provide electricity during periods of darkness.** Backed by some $250,000 over a three-year period from Grumman Aerospace Corp. of Bethpage, N. Y., Optel thus far has achieved solar conversion efficiences of 3% to 5%, says Satyen K. Deb, director of research and development.

SMC signs patents license with Western Electric

Adding to the prestige of a patent portfolio that already includes licenses granted to IBM Corp., Texas Instruments Inc., and ITT, Standard Microsystems Corp., of Hauppauge, N. Y., has entered into an agreement with Western Electric Co. of New York. The accord provides for the worldwide nonexclusive cross-licensing of each firm's present semiconductor technology patents and any they apply for during the next five years. But this agreement is different: **the pact also calls for Western Electric to pay financial considerations to Standard Microsystems,** a move that is believed to be a first for the AT&T subsidiary. Most major semiconductor makers, on the other hand, are paying royalties to Western Electric. Included in the exchange is SMC's Coplamos patent covering structures in high-speed, high-density n-channel MOS devices, as well as Western Electric's patents relating to diffusion and oxidation in semiconductors and to the basic MOS and silicon-gate MOS transistor structures.

THE THRIFTY LP2 PRINTER. THE OPTIONS COME STANDARD.

Data General's new 180 cps, logic-seeking bidirectional printer. It's more competitive so it makes you more competitive. Packed with a lot of standard features that cost you extra on other printers. Like forms control, vertical and horizontal tabbing, variable character sizes, a 7 x 9 matrix, plotting under software control and international fonts. Now, no matter what goes into your computer system, it can come out economically on a Data General Dasher LP2. Call for additional information. Or send for our brochure.

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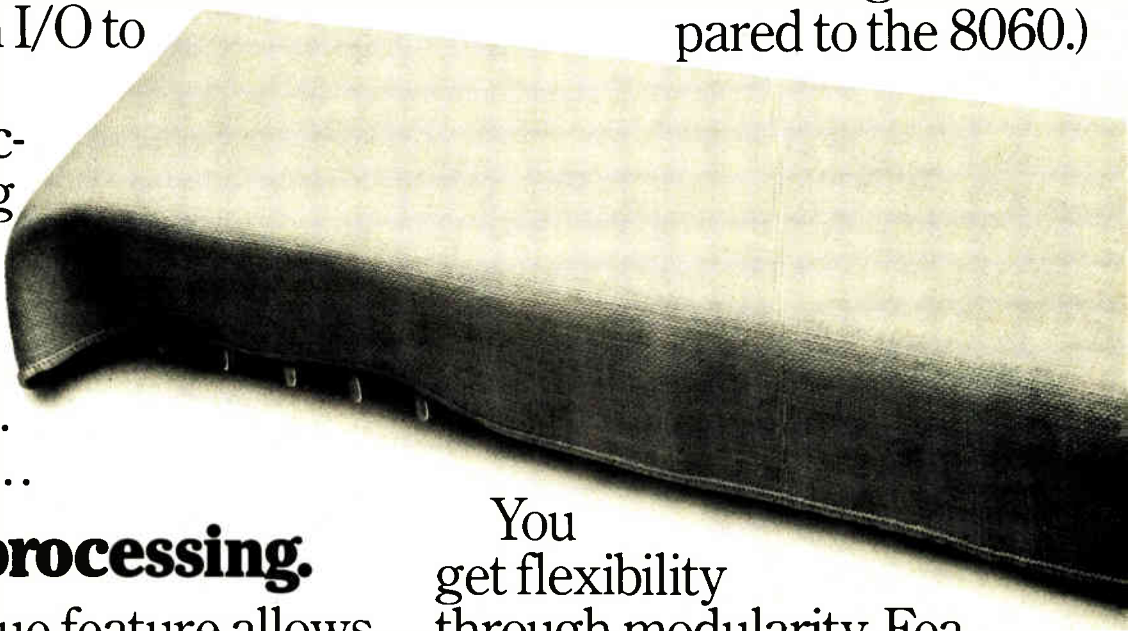
EX817

Presenting our 32-



In four parallel 8-bit chips.
Our 8060 microprocessor allows common memories and common I/O to be shared by multiple processors strung together like Christmas lights via a common bus.
In a word...

Multiprocessing.

This unique feature allows one 8-bit microprocessor application to be split into more easily manageable parts. So the whole job is easier.
Software development is easier. And cheaper.
What makes all this possible is built-in control circuitry and cycle interleaving.
The result is a machine more powerful than any single CPU system. (And even if there *were* a single CPU system this powerful, it would cost an arm and a leg compared to the 8060.)

You get flexibility through modularity. Features can be added to your system by just adding on an additional CPU rather than rewriting the whole program.
And serial I/O facilities allow several self-contained 8060 systems (with memory) to be bussed together.
But multiprocessing is just one of the appealing features of the 8060 (a member of the SC/MP family.)

bit microprocessor.

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The 8060 uses NIBL BASIC language. In one 8K x 8 ROM.

This chip interprets English-like commands. Instead of a complex program, you can write simple Dick-and-Jane instructions such as A×B=C, which also reduces software costs.

Since NIBL is an interpreter, there's no expensive development system needed. All you need is the 8060 and the NIBL ROM.

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To turn the 8060 into a system just add one chip.

This results in a system more powerful than a one-chip system, but at a price competitive with a one-chip system. The chip is INS8356, which combines a 2K x 8 ROM, 128 x 8 RAM, and I/O.

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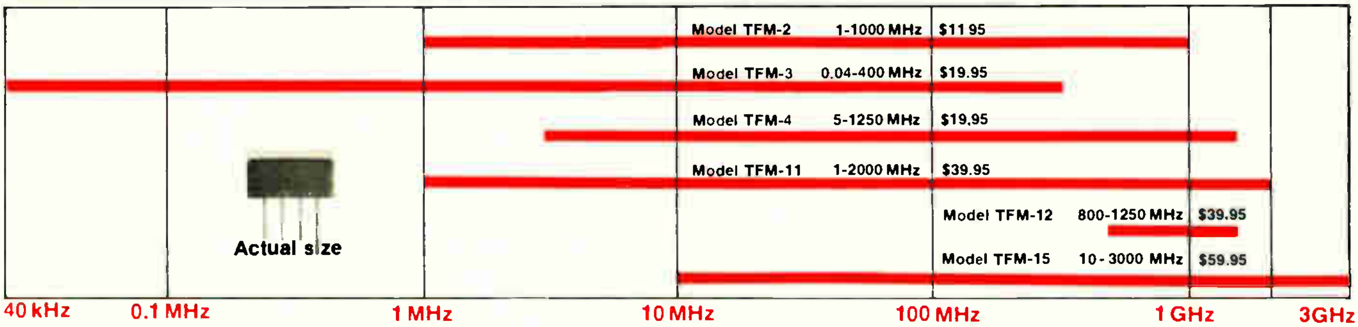

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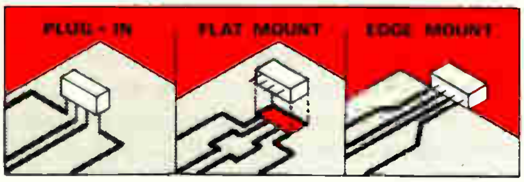

	Frequency Range, MHz			Conversion Loss, dB				Isolation, dB													
				One Octave From Band Edge		Total Range		Lower Band Edge To one Decade Higher				Mid Range				Upper Band Edge To Octave Lower					
								LO-RF		LO-IF		LO-RF		LO-IF		LO-RF		LO-IF			
Model No.	LO	RF	IF	Typ.	Max.	Typ.	Max	Typ	Min	Typ.	Min	Typ.	Min.	Typ.	Min	Typ.	Min	Typ.	Min.	Quantity	Price
TFM-2	1-1000	1-1000	DC-1000	6.0	7.5	7.0	8.5	50	45	45	40	40	25	35	25	30	25	25	20	6-49	$11.95
TFM-3	04-400	04-400	DC-400	5.3	7.0	6.0	8.0	60	50	55	40	50	35	45	30	35	25	35	25	5-49	$19.95
TFM-4	5-1250	5-1250	DC-1250	6.0	7.5	7.5	8.5	50	45	45	40	40	30	35	25	30	25	25	20	5-49	$19.95
TFM-11	1-2000	1-2000	5-600	7.0	8.5	7.5	9.0	50	45	45	40	35	25	27	20	25	20	25	20	1-24	$39.95
TFM-12	800-1250	800-1250	50-90	—	—	6.0	7.5	35	25	30	20	35	25	30	20	35	25	30	20	1-24	$39.95
*TFM-15	10-3000	10-3000	10-800	6.3	7.5	6.5	9.0	30	20	30	20	30	20	30	20	30	20	30	20	1-9	$59.95

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R 32/Rev A

Bubble memory chips now able to pack in quarter million bits

TI announces it will have samples of chip for $500 in fourth quarter; Rockwell, Fujitsu ready chips as well

The bubble memory business is escalating, and in the forefront, at least right now, is Texas Instruments Inc. It says it will have samples of a quarter-million-bit memory for $500, to go along with its older 92-kilobit chip, in the fourth quarter of the year. Waiting in the wings is Rockwell International Corp., whose similar-size memory is slated to be introduced at next month's Wescon.

Japan's Fujitsu Ltd. expects to announce a 256-kb memory, as well as smaller 64-kb-plus memories, sometime this autumn. However, it will not produce the larger unit in quantity right away. Hitachi Ltd., on the other hand, expects to be in volume production with 64-kb units by November. Waiting to see how things go is Nippon Electric Co., which has considered announcing a 64-kb product this autumn but may opt for the bigger memory instead, depending on how the market looks. In England, Plessey Microsystems Ltd. says it will have bubble memories in the fall (see p. 63).

Despite the jump in memory capacity, even higher capacity chips are needed before bubbles will replace or augment their oft-mentioned target—rotating disk memory. Bubbles are faster than disks and, with no moving parts, should be more reliable. Right now, they are also more expensive. But, if the bubble makers prove to be reliable sources of the new parts, a whole range of new kinds of products could be in the offing.

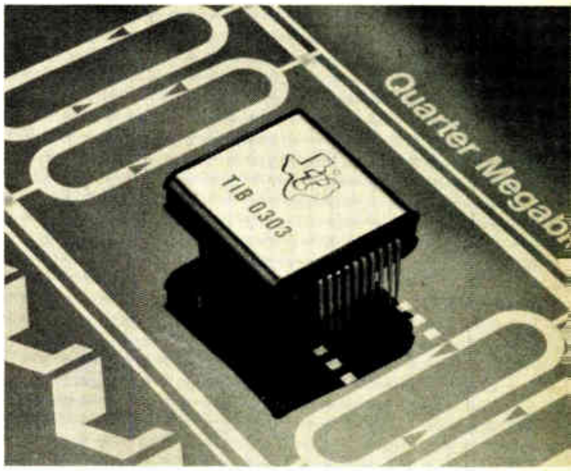
"Strictly replacing anything is not how [the bubble memories] will sell," says Michael Valek, manager of the bubble memory department at TI in Dallas. "Its true potential will come in the creation of new equipment where nothing else will do as well. The bulk of applications just have not been thought up yet."

Example. Valek cites as an example of such innovation the portable typewriter-sized terminal with printout, the Silent 765, that TI introduced at the beginning of the year. This terminal uses the company's bubble memories with 92 kilobits of storage. (TI also announced that it was cutting the price of its 92-kb units in half—to $100 each in 100-piece orders—and that it was producing about 5,000 a month.)

But for users of the large rotating memory stores, bubble memories are still off in the future. Bell Laboratories, which received the first patent on bubbles back in the 1960s and has been building four-chip quarter-megabit packages that store digitized speech, needs much more capacity per chip.

"We're experimenting now with 8-micrometer circuit periods," says Joe Geusic, head of magnetics at Bell, "and we're looking beyond that to 4 μm." That means Bell is eyeing 4-megabit devices. (Circuit period is a measure of the size of the basic bubble-propagating structure. For the TI device, for example, the period is now 16 μm.)

Computer companies, too, are concerned with the bubbles. IBM Corp., for one, is working on two



Bubbles. TI's quarter-million-bit memory and its magnetics will come in a 20-pin dual in-line package, 1.2 by 1.2 inches.

new approaches that will not be ready until the mid-1980s. IBM is aiming at 1- and eventually 4-Mb chips. They are sidestepping a direct reduction in geometry using techniques called contiguous disks and bubble lattices. "Both offer the ability to manipulate smaller bubbles with today's photolithographic capabilities," explains Clifford Cullum, manager of memory and storage research at IBM.

Contiguous disks rely on ion implantation instead of deposited permalloy shapes to guide the bubble. Higher densities are achieved essentially with an overlapping cell design. Bubble lattices are a whole new ball game. Closely packing the bubbles in hexagonal arrays will yield a tenfold increase in density, according to Cullum.

As for innovations, TI's Valek is hopeful that designers will get started now, particularly in the 200,000-to-300,000-bit area that

Here's the architecture

In building a quarter-million-bit bubble memory device, Texas Instruments has departed radically from the approach it used in the 92,000-bit major-minor-loop device introduced a year ago. Instead, it uses a block-replicate architecture that greatly reduces memory cycle time over the major-minor-loop approach. Also, the shape of the permalloy structures that chart the 3-micrometer-diameter bubble's course over the garnet substrate has been altered so that it requires less stringent mask tolerances. Minimum feature geometry is 1.8 μm; for the 92-kb chip, 2.25 μm. The big new chip dissipates 0.9 watt. Its controller will be compatible with TMS9900 series and TMS8080 microprocessors and will operate from a single 5-volt supply over 0° to 50°C.

The block-replicating approach to architecture used in TI's new TIB0303 has several other advantages over the major-minor-loop approach, which relies on the serial transfer of bits from smaller loops to a large one that has the mechanism for bubble detection, creation, and annihilation. The device stores data in 252 loops, each with a 1,137-bit capacity, or a total of 286,524 bits.

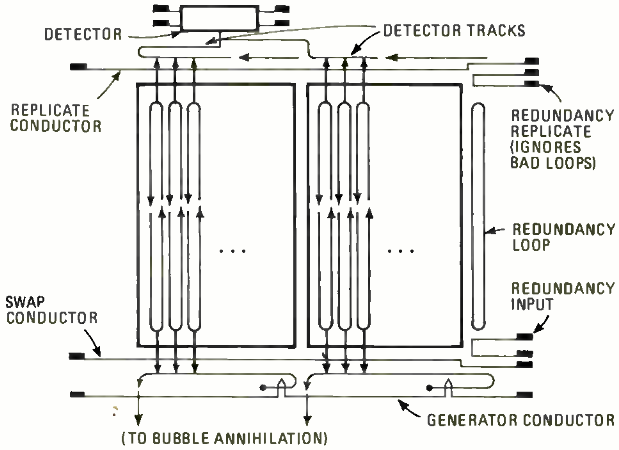
Rather than having a major loop, however, the TIB0303 has two master lines for detection (detector tracks) and separate write tracks for bubble generation. By porting the minor loops at both ends (see figure), an entire track can be duplicated into the detector track without removing data from the minor loop. This cuts down cycle time from 12.8 milliseconds in the 92-kb device to 12.5 microseconds and gives the TIB0303 an average access time of 7.3 ms when operated at 100 kilohertz.

What's more, the data rate in the block-replicated device is the same as the drive-coil current frequency—not half, as it is in a major-minor-loop approach. The reason is that the TIB0303 splits data into odd and even bits, which are merged in the detector tracks for reading. The merging operation eliminates the need for double bubble spacing and thus allows replication of bubbles—as one is read, the other returns to the minor loop.

Finally, the block-replicating structure permits a dedicated loop for redundant loop masking. Since the design of the TIB0303, like that of other bubble devices, allows for full storage capacity, the bad loops—in this case, as many as 28 failed minor loops—must be masked out; the quarter-megabit chip uses a dedicated loop to carry out the masking function, and the resulting storage will be a minimum of 254,688 bits.

The bubble memory uses an asymmetrical chevron shape for the deposited permalloy patterns. The new shape not only has bubble propagation characteristics superior to those of earlier T-bar and chevron designs, says TI, but also has less critical interpattern spacings and is thus more easily produced with standard photolithographic techniques.

To the $500 price of the bubble memory itself, built on a 365-by-340-mil chip, is added the cost of peripheral and controller circuits. TI will supply a discrete implementation of the interface circuits on a printed-circuit board, along with the memory. With it will come a schematic for the controller; it will be implemented on a board about two months later. Circuits implemented on individual integrated circuit chips will come during the first half of 1979. TI declines to discuss the price of these chips at present.



falls below floppy disks and above semiconductors. Products could come as early as 1980, if not sooner.

But his firm may have to overcome some hard feelings on the part of users promised the 92-kb devices by TI, which has had trouble delivering. "We just sent someone down to plead for parts," says George W. Fink, vice president of marketing at Data Systems Design Inc., Santa Clara, Calif.

Creative Strategies International, a San Jose, Calif., market researcher says Data Systems Design's experience is not unique. "They [TI] had generated a lot of enthusiasm about bubbles, but it started to slip as problems with reliability and delivery became evident," says CSI president Larry J. Wells. New companies like Rockwell, Fujitsu, and Nippon Electric in the field should boost the enthusiasm again.

Valek concedes TI had trouble putting the 92-kb device into production after it made pilot quantities late in 1976. But the problems were overcome early this year, he says. As for problems making the larger chip, he doubts there will be any. "We learned our lessons with the 92-kb chip," he says. "We're using the same materials, reactors, and test facilities. The only thing we change is the photomasks." □

Communications

Uhf users object to FCC spectrum plan

Everyone agrees that aeronautical and maritime mobile communications need more space in the ultra-high-frequency spectrum than the crowded 4.6 megahertz they now occupy. But industry users and the Federal Communications Commission's uhf task force in its new report are far apart on how much more will be needed to meet projected de-

mands by the century's end.

Users want ten times more bandwidth for a total of 50 MHz—30 for aeronautical services and 20 for maritime. The FCC task force says a total of 12.2 MHz will be more than enough to do the job—if industry takes advantage of new and emerging technologies to make more efficient use of the spectrum.

The recommendation is creating "a furor within the industry," says the FCC's Raymond Wilmotte, the task force coordinator. After some 18 months of study, the task force also proposes implementing its plan with three levels of service, labeled A, B, and C. Level A systems would be modifications of hardware now in use, and level B would use available things like vhf single sideband to conserve spectrum and computers to automate functions like channel selection, call setup and disconnect, and transmitter identification. Level C systems, using things like digital signals to conserve spectrum, would evolve from emerging new technology, the task force says, and would operate in yet another spectrum segment.

Time and costs. One challenger to the recommendations is Aeronautical Radio Inc., popularly known as Arinc, the Annapolis, Md., company that operates the communications net used by the nation's airlines. Such services now occupy 3.2 MHz in the 118-to-136-MHz band. The FCC's Wilmotte says expanding this to a total of 5.8 MHz with 1 MHz more for existing services and another 1.6 MHz for radically new communications systems would be adequate to the year 2000 "because of the considerable expertise and excellent record of Arinc in planning and implementing systems."

Arinc's Hillyard Smith, external affairs director, disagrees. "Dr. Wilmotte doesn't tell us where all this new technology is going to come from," he notes. Moreover, multiple frequencies such as Wilmotte proposes would require developing either multimode or duplicate airborne radios. Not only does Arinc believe this too costly, but, Smith says, "there is no room. Even the racks on a [Boeing] 747 are full." Moreover, he contends, the time required to implement such an effort and gain international approval would eat up more years than the plan allows.

The task-force's example of a level B system using single sideband instead of frequency modulation to conserve bandwidth comes under fire from Nate Steele, an Arinc engineering executive. Noting that existing air-mobile communications employ some a-m bands, Steele says, "I can see how you could interleave SSB among fm channels, but trying to interleave a-m–equivalent channels in existing bands doesn't seem technically feasible."

Seaside. For the civil maritime mobile service, the task force proposes expanding the existing 1.4-MHz allocation in the 150-to-174-MHz band by another 5 MHz to meet end-of-the-century requirements. To match the 10% annual growth rate of recreational-boating uhf radio licenses, as well as the slower-growing commercial service on inland and coastal waterways, the task force proposes allocating more channels at both vhf and uhf.

The seven-member FCC has yet to budget time for consideration of the aeronautical and maritime mobile issues, Wilmotte says. Resolving the problems posed by the task-force's recommendations is likely to be even more difficult because the unit has been disbanded by the new chief of the Office of Plans and Policy to which it originally reported. That management move reassigned Wilmotte to the Safety and Special Services Bureau, which oversees mobile communications, and gave the Broadcast Bureau responsibility for the uhf broadcast recommendations of the task force. □

Solid state

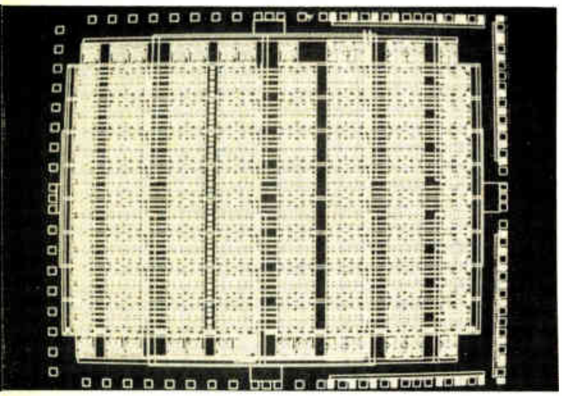
Macrocells ease ECL design chore

Single-chip arrays of emitter-coupled-logic gates have plenty going for them: blazing speed, monolithic reliability, and flexibility—provided the system designer is competent to configure the uncommitted gates into the functions he needs. Many cannot because the idiosyncracies of ECL make connecting individual gates into the desired logic patterns extremely tricky. Also, even in arrays that work, a high percentage of gates often goes to waste.

So Motorola Inc. is proposing something rather different—what it calls a macrocell array to free users of the tedious business of dealing with the gates individually. In this array, the gates are arranged into standard logic functions so that the designer need only be concerned with connecting functions in the right configuration. As many as 48 logic functions may be selected from a library of 54.

Like a pc board. "Prospective users tell us it reminds them of designing a printed-circuit board," claims Ronald Lipinski, marketing manager of ECL products at the Integrated Circuit division's bipolar operation in Phoenix. "They put gate-array functions as cells on the chip in the same way components are put on a pc board."

Although competing firms are committing to gate arrays [*Electronics*, March 30, p. 39], Motorola is going the macrocell direction because, based on experience with ECL



Designing cell. Mask used in macrocell array is shown displayed on cathode-ray tube. Each rectangle is a functional cell.

that dates back to the 1960s, it is convinced that designers need short cuts. "We provide the tools for routing the functions on a master-slice chip," Lipinski says.

Terming the macrocells a major Motorola product, the marketing official sees it paying off in cost savings and faster design turnaround for users. "For $40,000 we supply everything to get 10 prototype working parts in only 12 weeks." In 1,000-piece production lots, finished circuits should cost about $35 each, as against $100 to $150 and 12 months for comparable custom large-scale integrated devices in other processes, according to Lipinski.

The macrocell comes on a 200-by-200-mil chip that holds about 720 gates, organized into 48 15-gate cells, 32 input buffer cells, and 26 output cells. Besides the 54 logic functions, any of which the customer may select for any of the 48 cells, Motorola offers a choice of 13 input and 17 output patterns. "We know the logic size is right and there are plenty of routing channels," Lipinski says.

Typical functions. Some typical chip functions designed into the macrocells are 8-bit arithmetic/logic units capable of adding in 12 to 13 nanoseconds, adder-accumulators, and 8-by-8-bit 2-ns multipliers that are fully expandable to 16-by-16 and 32-by-32 elements on one chip. Lipinski claims that the Motorola approach achieves a much higher component utilization, on the order of 90% to 95% of the array, than when gates are hooked together.

At present, the company has finished its chip design and is in the midst of characterizing the logic parts for its library of functions. Some time in the first quarter of 1979, the program will start. At that time, those who want even faster response can use an interactive graphics terminal as an input to the macrocell program. By connecting it with Motorola's master computer, a designer could tap the function library in real time, lay out the routing pattern on the screen, and transmit the finished circuit specification. □

Consumer

Microprocessors help to mix and slice

They won't usually admit it, but appliance makers do resort to "innovations" that have more promotional appeal than substance to set themselves apart from competitors. This may be the motive behind Hamilton Beach's decision to put microprocessors in both a food processor and a blender, introduced last month at the National Housewares Exposition in Chicago.

"Space-age dependability" and "world's first computerized small appliance" are samples of phrases being used to advertise the products. But there is little a microprocessor can be called on to do in appliances that just mix and slice. Both machines have a metric-to-English calculator for converting recipe amounts such as liters to cups or teaspoons to milliliters. But all functions are still controlled one at a time by pushing buttons, as in conventional appliances.

Added features. According to Hamilton Beach, a Waterbury, Conn., division of Scovill Manufacturing Co., the microprocessor control, built around a TMS1000 4-bit chip from Texas Instruments Inc., adds to the reliability and safety of the appliances. This enhancement comes because of a new keyboard—from TI's Klixon line—being used in place of ordinary push buttons. Foods may sometimes drip down into the push buttons and short out circuits, even giving the user a shock, claims Hamilton Beach.

Not so with the new models. Because there is hardly any mechanical travel with the Klixon board, it can be sealed with a thin protective elastomeric sheet. By applying the memory in the microprocessor, it now takes three key pushes in the right sequence to start the blender, for example, making it more child-proof than machines that use one button to start.

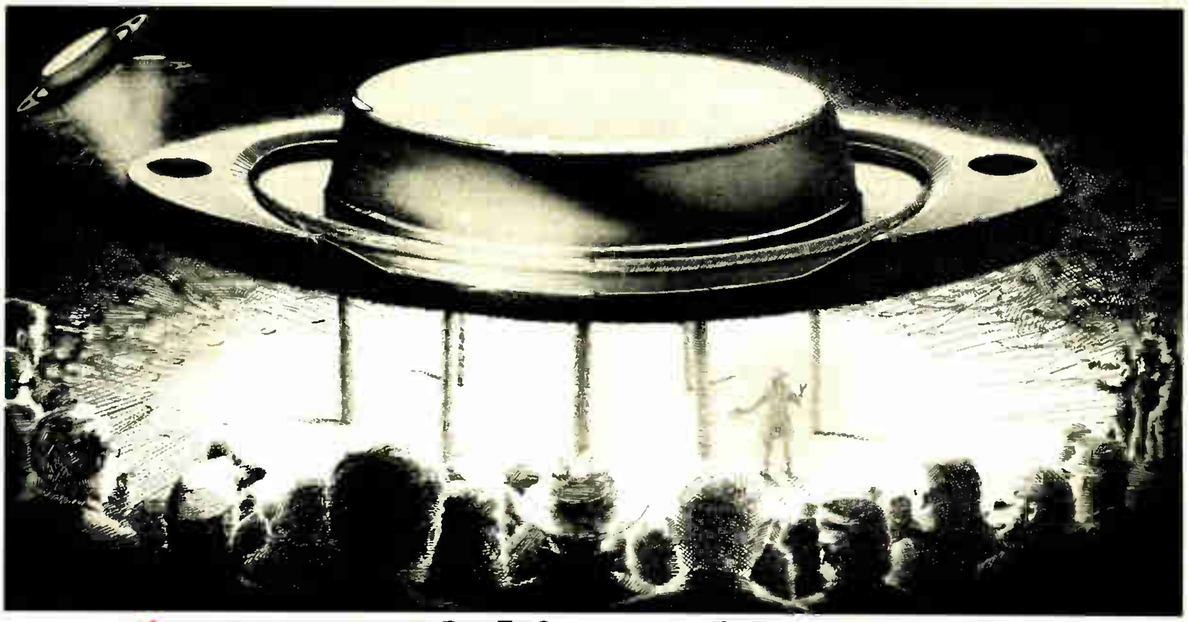
The TMS1000 chip has 2 kilobits of semiconductor memory, divided equally between random-access and read-only. A triac power control links the chip to the motor. A three-digit light-emitting-diode display presents the metric-to-English conversion figures as well as each speed command and the time it is supposed to run.

The units will also turn themselves off if they operate longer than about two minutes. Hamilton Beach aims to standardize the electronic package, perhaps adding it to other small appliances, "if these sell well," says Clifford M. Helton, product manager for new programs.

He says the firm plans to produce

World's first. Food processor controlled by 4-bit microprocessor has flat keyboard, sealed to protect it against dirt.

5 AMP SWITCHING REGULATOR



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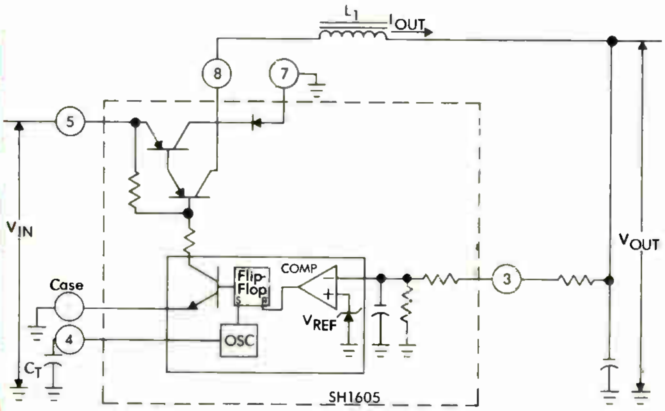

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50,000 blenders a month and 20,000 processors, which may vary depending on demand. Both units are priced high in their marketplaces—the blender at $69.95 and the processor at $159.95. □

Computers

IBM reorganization suggests new units

Last week's split of IBM Corp.'s large-computer manufacturing branch into two parts signals more than just a reorganization. It is a sign that two future mainframe systems are nearing introduction, say industry analysts who follow the giant computer firm.

The reorganization of the System Products division creates the Data Systems division, which the company says will have "development and manufacturing responsibility for large complex systems with primary emphasis on high-performance products," and the System Products division, which will handle intermediate-performance products.

What does the reorganization mean? Chairman Frank T. Cary says only that it "will provide additional management focus on marketplace requirements in an environment of changing technology, increasing competition, and rapid growth."

Agreement. A hearty second to that reasoning comes from John McManus, a securities analyst with New York–based Shearson Hayden Stone Inc. "IBM realized how unresponsive it's been" in countering the recent spate of software-compatible mainframes, he says.

McManus and other industry analysts divine future product plans in the change. Coming up, they say, is what is being called the E series, which reportedly would offer improved performance over the System/370 models 115 through 148, yet at the same or reduced prices. Next will be the high-performance H series, expected to supplant the 370/158 up to the 3033 processors, says Robert T. Fertig, vice president of Advanced Computer Techniques Corp., New York.

"It's clear that IBM is getting ready to launch the E and H series and created two divisions to handle the later phases of development and manufacturing," says Fertig, who just finished overseeing a study on "IBM Systems in the 1980s." He expects the E series to be unveiled in the first quarter of 1979, with the H series to follow about 18 months later.

Reversal. The latest reorganization is a reversal of the 1960s consolidation that created the Systems Products division to manufacture the architecturally similar System/360 and 370 lines, notes Gideon Gartner, vice president and partner in Oppenheimer & Co., also in New York. "It signals the fact that they'll be going in two different directions now," he remarks.

IBM is naming John E. Bertram, vice president for development and manufacturing of the former System Products division, as president of the Data Systems division. Jack D. Kuehler, former assistant group executive of the Data Processing Product group, is now president of the System Products division. □

Microcomputers

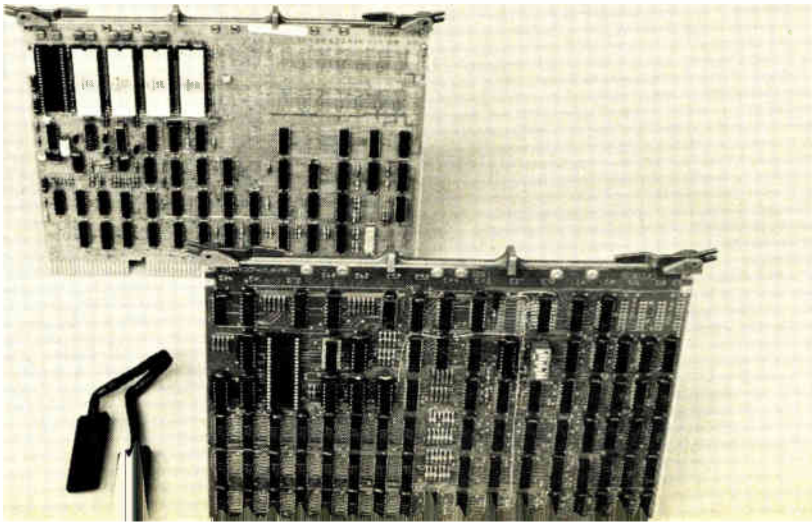
Digital Equipment Corp. offers kit that allows microprogramming of LSI-11

Users of the ubiquitous LSI-11 will soon have a new feat to boast of: with an optional program board that Digital Equipment Corp. is offering for its microcomputer, they will be able to design their own instruction sets. Of course, creating the special instructions, or microprograms, requires a great deal of software expertise. Used to the fullest, however, it allows a microcomputer to execute complex routines and mathematical operations at speeds that challenge mainframe computers' standard software.

"Over the last eight years, microprogramming has been offered to mainframe and minicomputer users," says Michael I. Titelbaum, engineering manager in DEC's Small Systems Engineering division in Maynard, Mass. "Now it can be done at the microcomputer level."

The upgrading does not come cheaply. Included in the kit—priced at $2,195—are two boards: a writable-control-store module and a new LSI-11 central-processing-unit board. The combination ensures that the sockets on both of the boards match up, not always possible if the control store were merely added to an LSI-11. A computer with the microprogramming capability and

Microprogrammable. New board, bottom, that brings microprogramming to DEC's LSI-11 microcomputer connects by cable to chip set on the microcomputer's main board, top.



16-K memory costs about $1,800 more than an LSI-11 with the same amount of memory, or $3,490.

But the cost can be worth it, according to DEC, because microprogrammability in a microcomputer narrows the gap between it and minicomputers, giving it a better chance than ever of chipping away at minicomputer markets.

For example, with microprogramming, number-crunching chores can be done on a general-purpose microcomputer, not just on a higher-performance—and higher-priced—minicomputer. This capability can also be extremely useful for users having unique data types. "They might have 27-bit words, or it might be that they don't use ASCII characters," Titelbaum says. Still others may need a repetitive function, like a fast Fourier transform, to be performed quickly for an image- or speech-processing application.

Optional board. The optional board for the LSI-11 contains 1,024 24-bit words of random-access memory, which stores the user's microcode while giving him read-only or read/write access. The board has a 40-pin socket that is mated by an interconnecting cable to a similar socket on the LSI-11 main board.

The socket on the host board is next to the four 40-pin chips in the LSI-11 chip set, which comprises a data chip, a sequencing chip, and two 512-word-by-22-bit read-only memories. The ROMs store the microcode for the PDP-11 instruction set; in effect, the option adds more ROM for more instructions.

As it happens, it was not just fortuitous that engineers at Digital Equipment found they were able to outfit their LSI-11s with the optional writable control store, says Titelbaum, who maintains that the option was planned from the outset of the LSI-11 design. "Most of our competitors just don't have an architecture that is extendable," he says. "The option was designed into the LSI-11 chips—it's not an afterthought."

The microcoding is easily implemented by anyone who knows the PDP-11 architecture. "The basic

News briefs

FCC orders reduction in uhf noise in TV sets

The Federal Communications Commission has ordered a two-step reduction in the maximum uhf noise generated within a TV receiver. The noise figure is now 18 decibels. In the 6-to-1 ruling, the FCC ordered it cut to 14 dB in the first phase and to 12 dB in phase two—with a warning that a later reassessment based on new information might drop the second stage to 10 dB.

The reduction to 14 dB becomes effective with all new models submitted for certification after Oct. 1, 1979, and for all sets built two years after that date. The FCC believes the lower figure is achievable without raising costs or inhibiting the use of electronic (push-button) tuners. The second-phase cutback to 12 dB would affect all new models submitted for certification after Oct. 1, 1982, and those manufactured two years later.

Set makers have 30 days to respond to the August 4 order. However, the Electronic Industries Association's consumer products engineering chief, E. M. Tingley, says it may submit a petition for reconsideration to the FCC. The accuracy of noise level measurements is already being challenged, he notes.

Although no FCC member opposed the first-stage reduction (Docket 21010), commissioner Robert E. Lee dissented, "because I think the 12-dB standard represents more wishful thinking" by those advocating parity with vhf standards.

The FCC order warned that its investigation into uhf reception was far from ended, calling its action the beginning of one of the "most important actions this commission has embarked upon—a fundamental reassessment of television reception."

Office automation to almost triple in five years

The market for automated office equipment, including personal computers for office use, word-processing systems, and private automatic branch exchanges, will soar from $3.7 billion in 1977 to $9.1 billion by 1982, according to Creative Strategies International. Not surprisingly, the market research firm says that IBM Corp. is best poised to dominate the market because it has the short-run capability of combining software for data and word processing with stand-alone minicomputer-based systems and, except for Xerox, is the only one that has developed strategies for the total "office of the future."

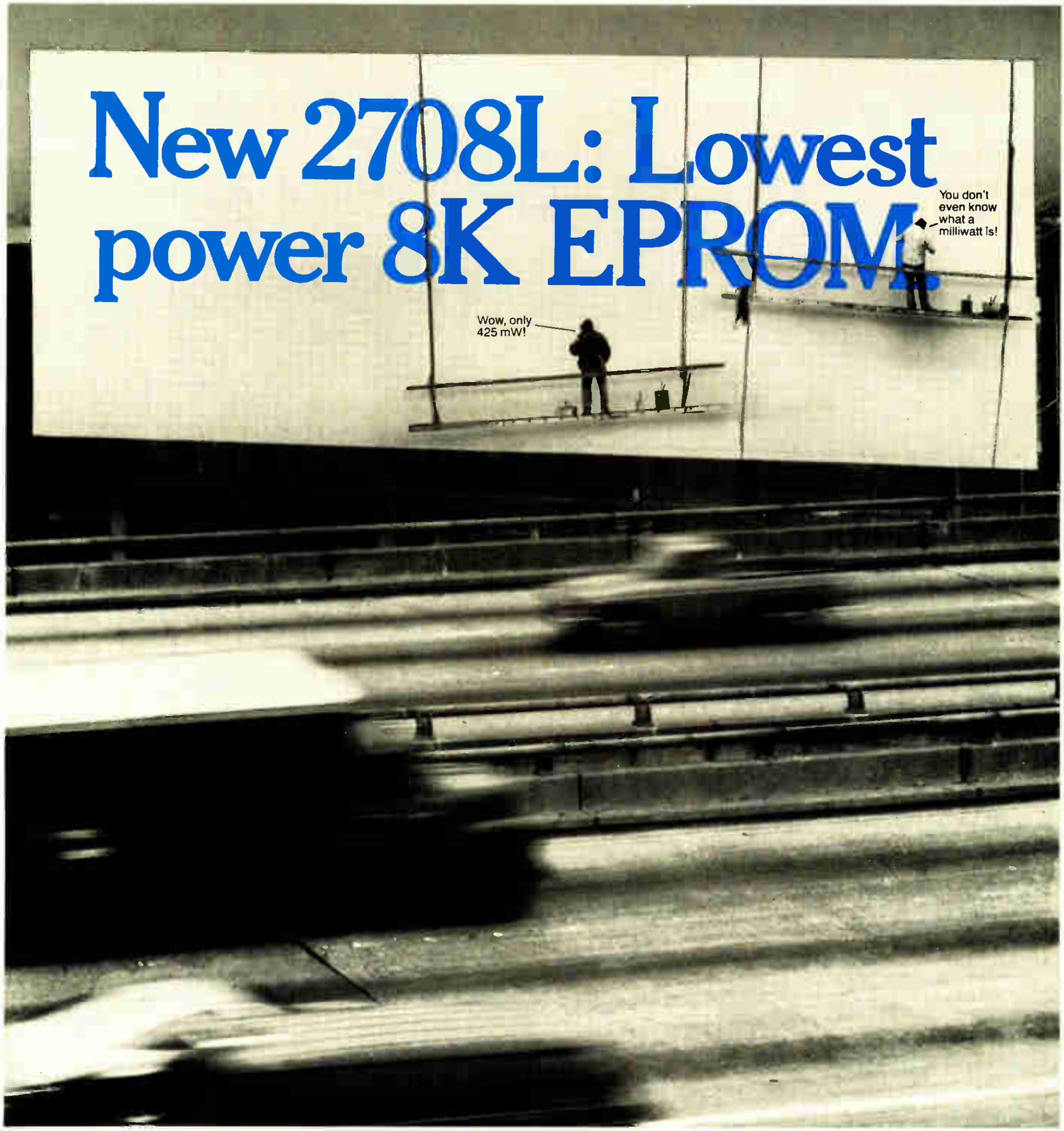
Moreover, of the more than 100 companies active in the field, only Burroughs, Eastman Kodak, Exxon, IBM, 3M, and Xerox are committed in a broad range of automated office products, the San Jose, Calif., research firm says. The big question mark is AT&T, which could become a factor depending on automation features it puts into its proposed digital data network [*Electronics*, July 20, p. 41], CSI says. Its market breakdown from 1977 to 1982 sees personal computers jumping from $13 million to $360 million, sold and leased word-processing systems growing from $807 million to $3 billion, and PABXs rising from $160 million to $490 million.

IBM, Xerox end all litigation, exchange licenses

International Business Machines Corp. and Xerox Corp. have agreed to exchange paid-up worldwide licenses under all present patents and those applied for during the next five years. The pact covers all products of both firms, including IBM's computer lines, and ends 12 separate suits between the two companies. In addition, IBM will make a $25 million payment to Xerox as part of the accord.

Northern Telecom acquires 87% of Data 100

Through a tender offer made by its wholly owned subsidiary Northern Telecom Computers Inc., the Canadian telecommunications equipment giant Northern Telecom Ltd. has acquired about 87% of data terminals maker Data 100 Corp. of Minneapolis. The Montreal-based firm previously held a 31% interest in Data 100, which posted 1977 revenues of about $138 million.



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architecture is very simple, using 16-bit words. The instructions look very much like PDP-11 macrocode," he says, referring to the instruction set used in DEC's popular minicomputer.

Titelbaum adds a word of caution, however, to those who want to get into microprogramming. "It's a sophisticated process that we think is best tackled by the PDP-11 or LSI-11 user who's familiar with the architecture. Although we provide microprogramming support, some users will be advised against the option." □

Photovoltaics

Roof shingle has solar cells built in

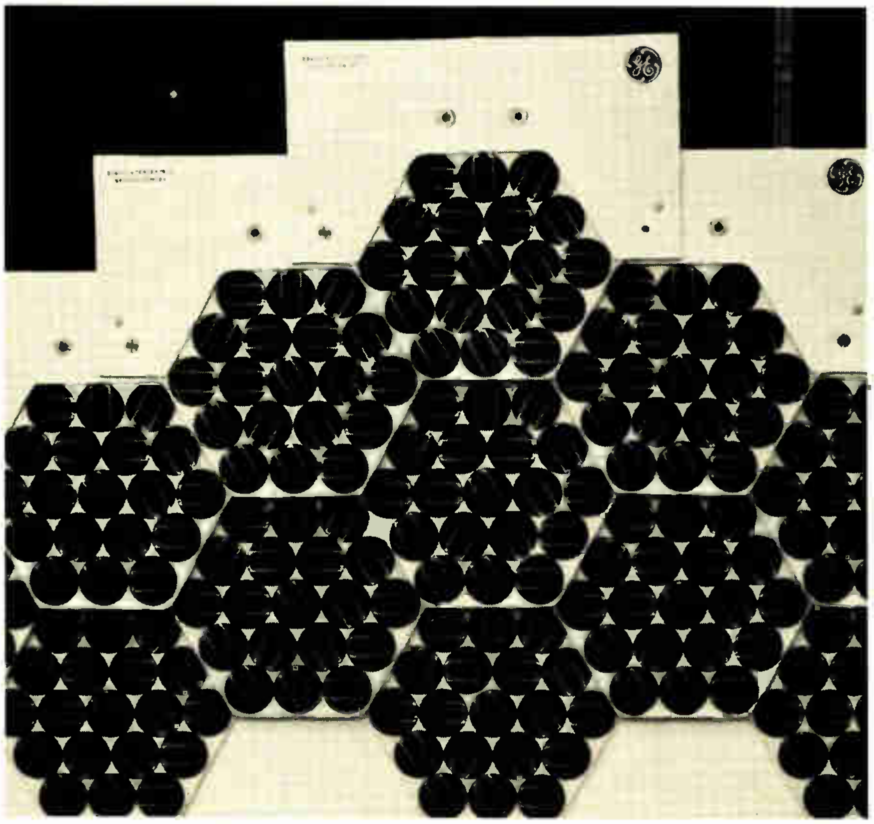
A roof overhead, plus the electric bill paid. Sounds like part of the American dream, a part that General Electric Co., at least, is trying to make come true by combining specially developed roofing shingles with photovoltaic solar cells.

GE has put together 52 solar-cell shingles and shipped them for testing to California's Jet Propulsion Laboratory, according to Neal F. Shepard, Jr., manager of the electronics company's effort at its Space division in Valley Forge, Pa. The shingles were developed under a year-long, $200,000 contract with JPL as part of the Department of Energy's low-cost silicon solar-array project.

Shepard says a hexagonally shaped array of 19 silicon cells supplied by Solarex Corp. bonded to each of the 52 shingles generated a maximum average power of 98 watts per square meter.

However, GE does not plan to remain idle while JPL conducts its tests. The firm is considering several opportunities for designing a roofing system for large public buildings that would use the combination shingle, a spokesman says. Although it

Shingles. Roof shingles from General Electric have hexagonally shaped areas, each containing 19 silicon solar cells. Power output hits average of 98 watts per meter.



cannot give a cost for the shingle right now, because so few have been produced, the company perceives a possible 1985 market, provided the price can hit the dollar-a-watt target that is the aim of the Department of Energy program. Regardless of their price, about 1,900 of the shingles, used on an all-electric home in the southwestern U. S., could supply the house with 90% of its electricity free if credit were given for excess power fed back to the local utility, according to GE.

Moreover, the homeowner would have a watertight roof for his home for at least 15 years. A conventional rigid solar-cell module subject to buffeting by winds and requiring additional roof supports would not be needed.

Cells. Bonded to each rectangular shingle, made of synthetic rubber, is a hexagon of strong, heat-tempered clear glass containing 19 solar-cell disks, each with a diameter of 53 millimeters. The disks are at least 0.5 mm apart, achieved with assembly tooling. An embossed glass cover plate is bonded to the top. The upper half of the silicon hexagon's underside is then bonded to the top of the shingle.

The hexagonal shape permits the modules to be butted against each other when the shingles are laid in the conventional overlapping manner with roofing nails. Solder-plated copper buses within each shingle overlap and interconnect the modules. A machine screw and flat washer develop a high-pressure contact, Shepard says. An insulating sleeve around the screw prevents electrical contact so the exposed screw head and washer remain electrically neutral.

Although GE has shipped its solar-cell shingles to JPL for testing, Shepard says the company wants the contract extended for a few more months to analyze and study the product further. One variation might be to ensure that sunlight incident on the embossed glass cover is trapped in the cell by repeated internal reflections. The light could then be absorbed by the active solar-cell surface, rather than wasted. □

HP improves SOS

When Hewlett-Packard Inc. designed a 16-bit microprocessor around its own complementary-MOS-on-sapphire technology [*Electronics*, May 26, 1977, p. 99], it achieved a high-speed 12-volt device whose performance rivaled bipolar designs. Now, at next month's Wescon, HP engineers will describe a partial redesign of the same chip that adds a 5-volt power supply so that the device can work with the large number of transistor-transistor-logic parts available.

Though slightly larger and slower than the first-generation device, the new part has a maximum operating speed of 5 megahertz and a maximum power dissipation of between 500 and 600 milliwatts and is made with 4.5-micrometer instead of 6-μm design rules. A key feature is a TTL–C-MOS converter circuit to translate the incoming 5-V signals to the internal 12-V levels that is essentially a current-source–loaded, common-gain amplifier followed by a buffer inverter. The new 16-bitter is destined for HP patient monitoring systems and data terminals.

Displays

LCDs aim at supermarkets, banks

Fast becoming the most popular look for digital wristwatches, liquid-crystal displays are taking aim at bigger things—signs that flash the day's money-saving specials at the local supermarket or carry special messages in banks and restaurants.

The company pushing these new applications is Transparent Conductors Inc., a seven-year-old firm in Goleta, Calif., specializing in large-area LCD signs for such uses as advertisement, scoreboards, and elevator readouts. It has developed a 20-inch-wide display holding a single line of 16 1.7-in.-high LCD characters. The alphanumeric characters

Electronics review

Message maker. Sixteen-character alphanumeric LCD unit from Transparent Conductors stores up to 64 lines of text.

can be changed every 2 seconds, directed from a 1-kilobit random-access memory that stores 64 lines of text. The 10-pound "message box" is 4 in. high and 6 in. deep. The letters, backlit by a 15-watt lamp, can be read up to 50 feet away over a 160° viewing angle, according to Bernard Feldman, the company's president.

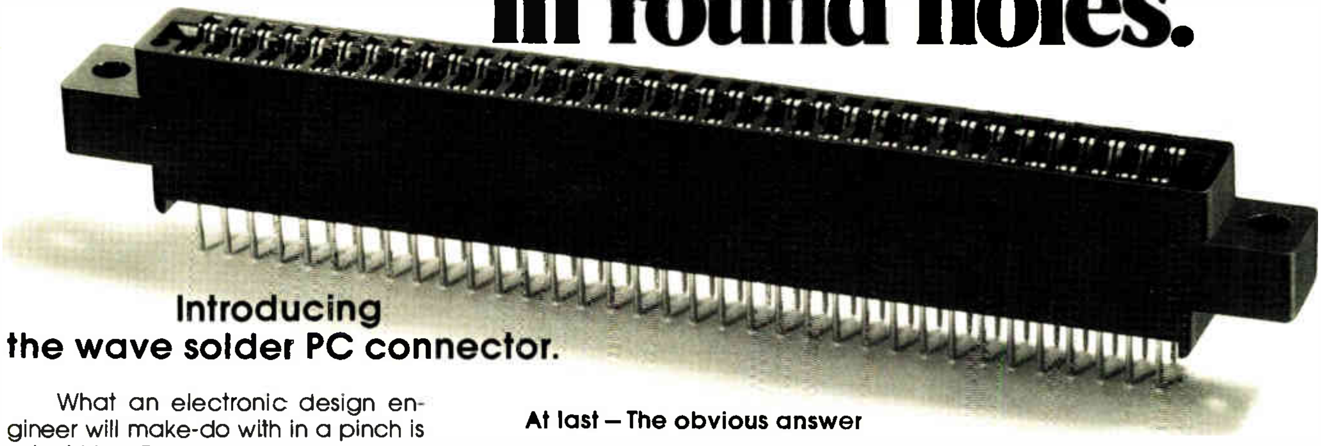
Easy to program. The biggest problem the firm had, he says, was making it easy for the decidedly nontechnical people who would use the display to program it. The solution is a typewriter-like keyboard in a programming unit the size of a small suitcase.

The company also uses 11-segment characters instead of the usual LCD-character design of 14 segments. The reason, simply, is that fewer segments mean more characters in the same space. "We can get 16 characters on the 18½-in.-wide by 3-in.-high display glass, which is a gain of 3 characters over the 14-segment ones," he says. The use of fewer segments also simplifies the drive electronics. All components are off the shelf, including complementary-metal-oxide-semiconductor drive circuits from RCA Corp.

Sample quantities of Transparent Conductors' model 216 display, which was completed this spring, sell for $990; the programmer, with a connecting cable that plugs into the display, is $240 more. A cassette programmer, with which programming could be handled at a central location, is $335.

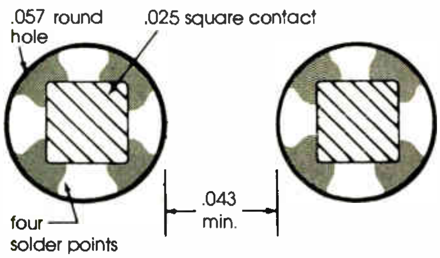
About 25 to 30 samples have been sold to potential users, including banks, the U. S. Postal Service, telephone companies, and McDonald's fast-food chain, Feldman says. Each unit, which requires 1.5 W besides

No more square tails in round holes.



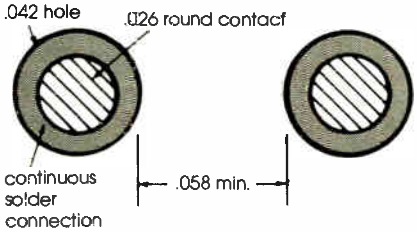
Introducing the wave solder PC connector.

What an electronic design engineer will make-do with in a pinch is astonishing. For example — converting wire wrap* PC connectors to wave solder.



How it's done: you saw off the square .025" tail and push it through a .057" round hole in the PC board. You get only 4 contact points for solder. And there's room for only one tracing between holes. But, so what... it works.

At last — The obvious answer



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15 w for the lamp, has a battery backup to preserve its memory in case of a power failure. □

Patents

Japan grants TI a calculator patent

The Japanese Patent Office has issued a patent to Texas Instruments Inc. that covers the bulk of miniature electronic calculators. According to TI, "The patent is for personal-sized battery-operated calculators which have their main electronic circuitry on a single integrated-circuit chip." The Japanese patent is based on U. S. Patent #3,819,921, granted to the Dallas firm in June, 1974. Inventors of the TI calculator are Jack S. Kilby, Jerry Merryman, and Jim Van Tassel. The unit's integrated-circuit chip could perform addition, subtraction, multiplication, and division.

Negotiations soon. "We will start negotiations [for licensing and royalties] with major calculator manufacturers in Japan quite shortly," says TI group vice president Morris Chang in Dallas. TI will have the right to claim royalties retroactively to Aug. 24, 1974, the date the calculator invention was published by the Japanese Patent Office. The number of single-chip calculators produced in Japan since then number more than 75 million. Major Japanese calculator manufacturers like Sharp, Casio, and Canon have so far declined comment.

As with the "very significant royalties" derived over the last 10 years from the Japanese for TI's semiconductor patents, any revenues paid to TI will depend on individual negotiations, Chang says, and these could lead to exchanges of licenses as well.

TI has licensed calculator companies in the U. S. for about the last three years. The revenues derived so far are confidential, Chang says, but he points out that "the weight [of production] has definitely shifted to Japan." □

EIA position on components certification gets Justice support

The Justice Department has bolstered the negotiating position of the U. S., represented by the Electronic Industries Association, in calling for nondiscriminatory participation by all countries in a new International Components Certification System [*Electronics*, Nov. 10, 1977, p. 50]. **Known as IECQ, the International Electrotechnical Commission system is being sponsored initally by 17 of the 43 commission member countries to simplify worldwide components trade.** The IECQ system would certify product quality and performance, much as the U. S. applies military specifications domestically. A fourth and perhaps final draft of IECQ rules is expected to be adopted at a November meeting in Geneva with the goal of implementing the system on July 1, 1979. Assistant Attorney General John Shenefield says EIA proposals for nondiscriminatory access do not appear to raise antitrust questions. But proposals by France and Germany limiting certification to IECQ member countries do raise serious questions of discrimination under U. S. antitrust laws, he adds.

FCC turns down primary-instrument plan promoted by AT&T

The primary-instrument concept that would have required the first telephone in any installation to be provided by the carrier has been killed by the Federal Communications Commission. The issue produced strong opposition from the telecommunications suppliers and Federal government users [*Electronics*, May 25, p. 58]. **Rejecting telephone companies' arguments that PIC was needed for effective service testing and line maintenance,** the FCC order observes that a customer-provided telephone could serve just as well as PIC for testing. On the maintenance side, the FCC concludes PIC is unnecessary since "the Bell System generally has no program for preventive maintenance" but simply repairs or replaces telephones when customers report trouble. Customers would be unlikely to let their own phones go unrepaired any more than they would neglect repairs of "other important services such as the furnace, the refrigerator, or the television set."

Controversy arises over Postal Service's role in electronic mail

Although the U. S. Postal Service says it could not implement an estimated $2 billion electronic message service until 1990, the Government is already concerned over a lack of Federal policy regulating this service. **At issue is whether the USPS should be permitted to compete in this market with private industry.** The Postal Service is awaiting completion of a $2 million system definition study due this fall from RCA Corp. Henry Geller, chief of the National Telecommunications and Information Administration in the Commerce Department, warned at a Senate hearing on postal reform that competition by the USPS with private industry in electronic mail raises multiple regulatory and economic issues requiring policy decisions soon. Geller appears to favor private development of the market. The Communications and Computer Industry Association is strongly against a USPS role in electronic mail and opposes congressional approval of any USPS resarch and development program, claiming it would make postal monopoly of this new field an accomplished fact.

Washington commentary

Military spending: the potential for chaos grows

President Jimmy Carter's inability to produce effective programs to cope with a number of national problems is no secret. National energy policy, tax reform, and his promise to limit the size and raise the productivity of the Federal bureaucracy are among the more obvious examples. Less well-known, however, is that Carter's difficulties in those areas may be submerged come January by a new and larger problem generated by the fiscal 1980 military budget.

Federal budget planners now have their first military spending requests in hand. They total some $8 billion more than the tight $135 billion ceiling set by the White House for the Office of Management and Budget. "The numbers themselves don't surprise anyone," says one senior budget official. "These first figures are always high. What is troubling, though, is that no one is sure where the reductions should come. We are not getting firm guidance from the President."

Carter's inconsistency

What troubles military spending planners is the same thing that concerns Washington's military electronics industry specialists: the inconsistency of Carter policies in some areas and their total absence in others.

Last January, for example, the President proposed a $126 billion military budget package that emphasized revitalization of the North Atlantic Treaty Organization in Europe. Since then, however, the White House has taken an ever harder line with the Soviet Union. One consequence is that the second round of Strategic Arms Limitation Talks designed to produce new controls on intercontinental ballistic missiles has gone nowhere. Thus the Air Force is getting Defense Department support for a costly construction program to dig extra ICBM silos that will let it move its missiles around secretly to make them less vulnerable to attack. If, say, two of every three silos are empty, Russia would still be obliged to attack all of them to guarantee destruction of U. S. retaliatory power. Such an attack, program advocates say, would be militarily and economically impractical. The Air Force estimates its effort would cost $20 billion and wants $1 billion to start research and development in fiscal 1980.

Program opponents—and they are growing in number—contend the effort is not worth the investment in terms of the limited additional security it would provide. Moreover, some budget analysts believe it cannot be done without cutting back on other commitments that would make a more positive contribution to military technology. "We are still committed to strengthening NATO," says one. "The budget cannot support NATO and the 'hidden missile' program, too." The White House has yet to decide on which course to pursue, and planners are nervous. They have but four months in which to complete the budget proposals.

Turning toward Congress

Military electronics suppliers are nervous, too. "If the Air Force gets $1 billion in R&D money for new ICBM silos in the new budget, I can see a lot of useful electronics programs being put on hold," complains one corporate figure in Washington who asked for anonymity. "My company specializes in avionics and ground support systems that make a positive contribution to defense. This multiple silo idea is madness. If the Air Force estimates now it will cost $20 billion, that probably means it will eventually cost $40 billion. I hear that R&D in the second year alone will jump to $5 billion. We want Congress to stop it."

Congress is listening to such complaints with increasing attention. Jimmy Carter's inability to make hard choices and effectively promote them on Capitol Hill has stimulated Congress to move into that vacuum. It represents the continued reawakening of Congress to its own responsibilities and potential that began with Richard Nixon and Watergate. Where prior Congresses were renowned for cutting White House military budget requests, this Congress has increased outlays for two consecutive years. Whether or not its choices were wise is not the issue here. Excepting Carter's energy program, the Congress has managed, rightly or wrongly, to act where the President has not.

The President's problems will be compounded if he cannot provide consistent budget guidance to military planners responsible to the White House. Military electronics lobbyists and other special interests recognize this and are turning increasingly to a Congress that itself is looking for guidance. That may be good news for those companies whose proposals succeed. But it is bad news for budget planners at the Pentagon and the Office of Management and Budget anxious to make the right choices and come up with a balanced program. When military leaders begin setting their own priorities and fighting amongst themselves to achieve them, the country—and its confused NATO allies—expects action on the part of its commander in chief. So far, it has not seen it.

Ray Connolly

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For complete technical data, write for Engineering Bulletin 3459 to: Technical Literature Service, Sprague Electric Company, 35 Marshall Street, North Adams, Mass. 01247.

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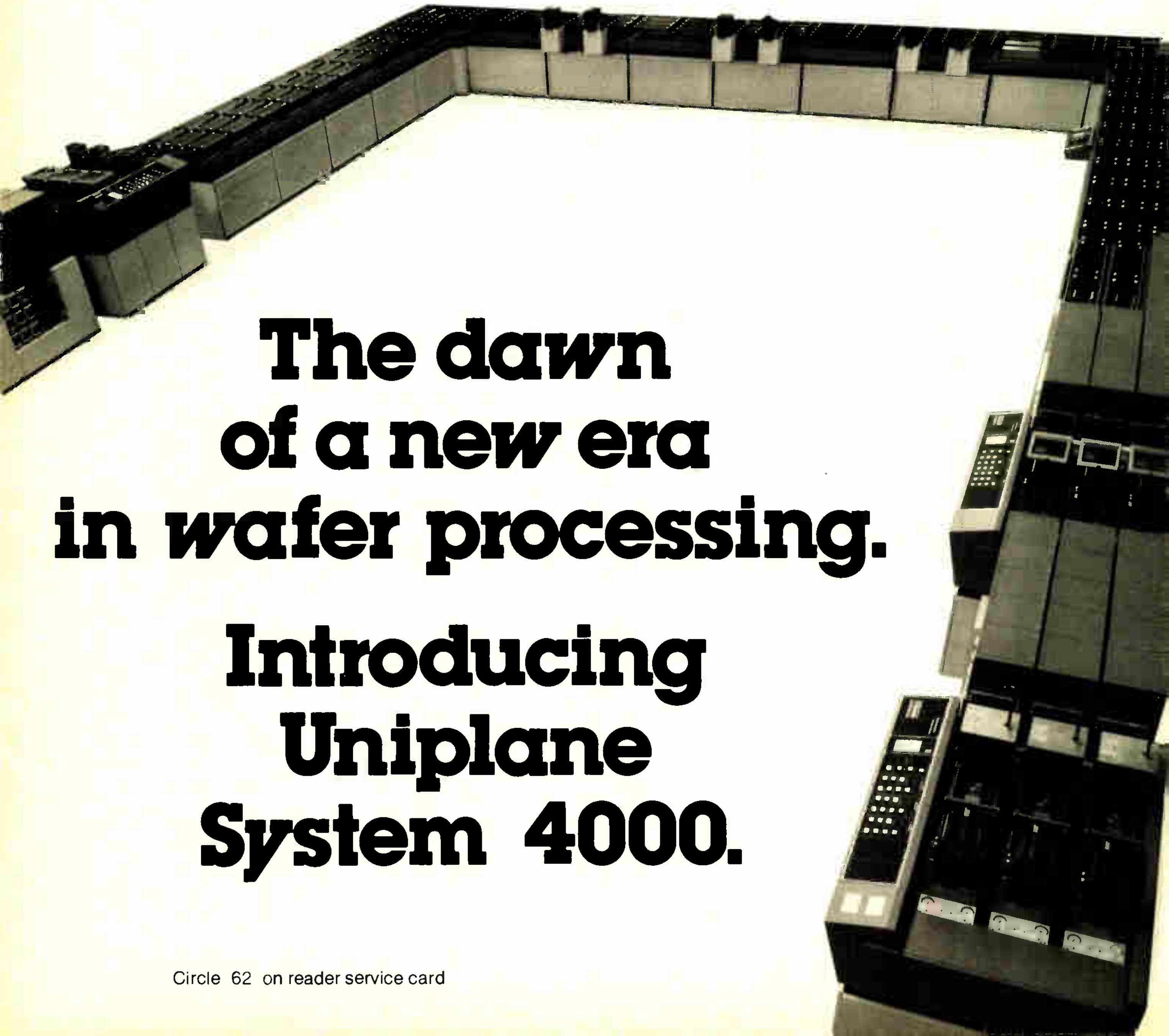

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International newsletter

GEC and Fairchild plan joint production in UK

Fairchild Camera & Instrument Corp. and the UK electrical giant General Electric Co. Ltd. will establish a high-volume manufacturing unit for n-channel MOS integrated circuits, to be on stream by early 1980. With ownership split equally, the UK plant will be used by Fairchild as a European production base and by GEC to manufacture price-sensitive standard products like its Teletext/Viewdata chip set. (GEC Semiconductors will remain a separate operation but with access to Fairchild technology, initially to its n-MOS design rules). **First products will be Fairchild microprocessors and memories including charge-coupled-device serial memories.** These CCD memories will mesh with GEC's capability in analog and imaging CCD devices. Both companies see the new plant as a stepping stone to collaboration on a broader front: in a separately announced deal, for example, the GEC subsidiary Marconi Avionics Ltd. can now incorporate Fairchild CCD cameras in its television systems.

Plessey plans volume production of bubble memories

Computer makers will soon have another source for commercial volumes of bubble memories: Plessey Microsystems Inc., which expects to be in full-scale production of its 64-kilobit PD 064-S1 by the end of the year. **The Towchester, England, firm also plans to release first details on its 256-kilobit memory in November.** The move to commercial production, assisted by newly available government aid for start-up costs, puts Plessey into a burgeoning field, now paced by Texas Instruments, but with other American and Japanese firms poised to jump in (p. 39).

MOS tetrode goes to 1,000 MHz for uhf TV tuners

Siemens AG is introducing a metal-oxide-semiconductor tetrode with an operating frequency of up to 1,000 MHz that makes it an excellent substitute for bipolar transisters in uhf TV tuners. Compared to tuners with bipolar devices, those with MOS tetrodes exhibit better large-signal characteristics, which lessen cross-modulation, Siemens says. **Designated the BF960, the tetrode features an 18-dB power gain and low noise, typically 2.8 dB at 800 MHz.** At that frequency, the input and output capacitances are smaller than 2 and 1 pF, respectively. The BF960's high operating frequency, about double that of most MOS components offered for consumer use, results from a refined n-channel technology that includes 2-μm design rules, Siemens says. Available now, the tetrodes cost about $1 apiece in lots of 1,000 or more.

Honeywell to sell its own computers in Japan

Honeywell Information Systems Inc. of Minneapolis is moving to boost its Japanese market penetration above 1% by taking charge of its marketing there and by adding minicomputers to its Japanese offerings. The firm is setting up a marketing subsidiary, in which it will have 80% of the equity. **The remaining 20% will belong to Mitsubishi Office Machinery Co., which has sold Honeywell's computers** along with those from Mitsubishi Electric Corp. and Fujitsu Ltd. The move by the American firm may signal the start of a do-it-yourself movement among American electronics manufacturers (p. 78). The company will take over a customer base largely of farm cooperatives, which bought systems from the French computer maker Machines Bull, now part of the French firm CII-Honeywell Bull. When Honeywell Information Systems took over Machines Bull, it inherited the Japanese operation.

It's boom times for West Germany's computer firms . . .

Scoring growth rates of well over 20%, computer firms in West Germany are enjoying boom times reminiscent of the 1960s. Production and sales of electronic data-processing equipment rose nearly 28% last year, and the upward trend is continuing, reports H. J. Bohn, head of the data processing section of the Frankfurt-based Electrical Industry Association. **During the first quarter of this year, incoming orders climbed 23%, while sales jumped by more than 24% and production by a whopping 38%.** Behind the boom, the association says, is the West German industry's drive to streamline operations and raise productivity in order to offset the rising labor costs and thus to remain competitive on world markets.

. . . and also for European VCR sales

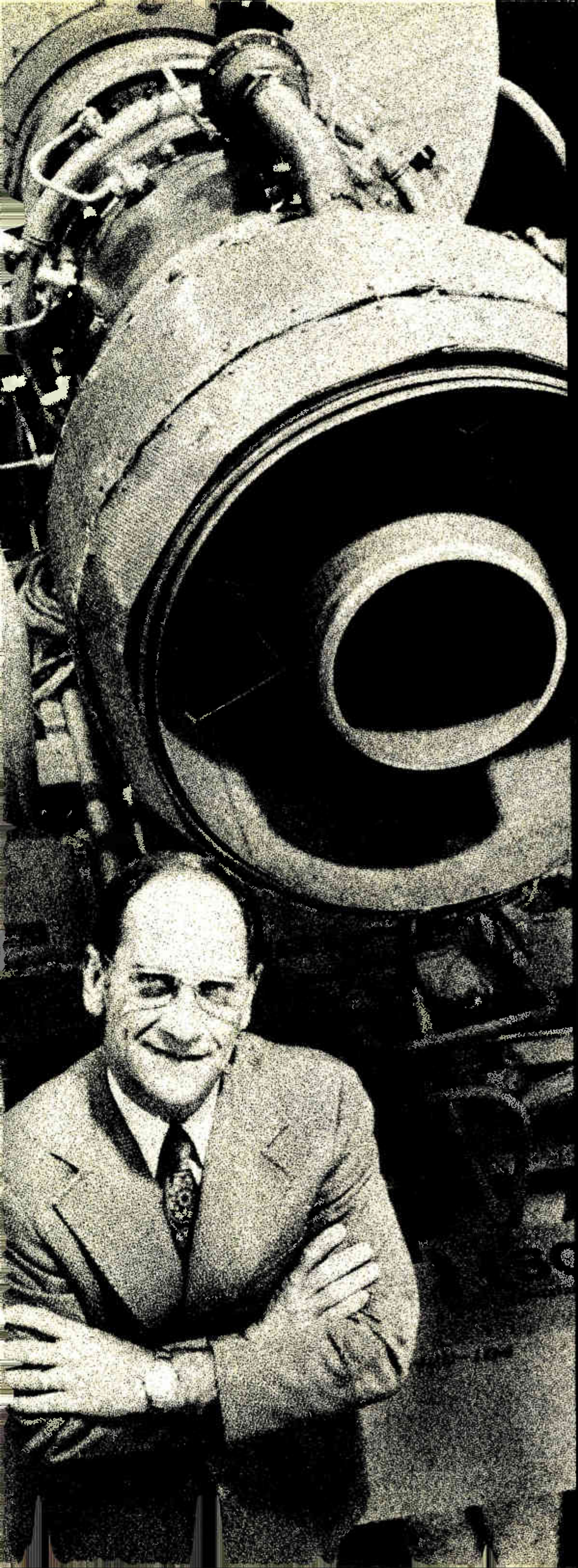
Entertainment-electronics producers in Western Europe are hard-pressed to keep up with the demand for video-cassette recorders. For example, Philips reports that **during the past five months orders have far outstripped the supply,** and other firms say they, too, are having trouble keeping dealers stocked. Thus far the giant Dutch company has sold more than 300,000 of its VCR and VCR-longplay recorder systems in Europe.

STL developing single-mode diode for fiber optics

Another laser diode with a single transverse mode of vibration has been developed, this one from Standard Telecommunications Laboratories Ltd., the Harrow, England, ITT research center. Such a diode will be a key element in the development of long-haul fiber-optic communications systems **because it permits a wider range of signal amplitude than do conventional diodes** that have light outputs switching between differing types of transverse operating modes and thus producing kinks in the output's radiated power. STL's device has a heterostructure of gallium-aluminum-arsenide and gallium-arsenide stripes and a 25-to-35-mA threshold current, four times lower than that of production devices. It has a 10-mw kink-free output, better than three times that of a similar device, using some STL patents, from Mitsubishi Electric Corp. [*Electronics*, July 6, p. 39].

16-K RAMs proliferate in Japan

Fine-pattern, dynamic 16-K random-access memories are becoming a habit in Japan: two new ones are joining the recently announced Hitachi Ltd. device [*Electronics*, Aug 3, p. 65]. One, from NEC, has a maximum access time of 120 ns, and 4-μm minimum line widths and effective channel lengths. The company is using it in memories in the DIPS-11 model 20 computer built for the Nippon Telegraph and Telephone Public Corp. to rent to its data-processing customers. Pin-compatible with the Mostek 4116 and other three-power-supply devices, the new RAM will soon be announced as the μPD416D-5. **Both devices were developed in the ongoing LSI memory project of the NTT's Musashino Electrical Communication Laboratory, Nippon Electric Co., Hitachi, and Fujitsu Ltd.** The other new RAM is an experimental device, but uses technology similar to that of Hitachi's commercial product. The technology, developed for 64-K RAMs, include 2-μm minimum line widths and effective channel lengths, and the resultant device runs off two power supplies +5 V and −2 V. Hitachi generates the negative voltage on chip; it also trades off a design better suited to production for slightly slower speed.



"We saved $42,000 by cutting down redrawing time the first year we switched to reprographic techniques."

Earl Lind, Graphics Supervisor Solar, an International Harvester Group, San Diego.

"Solar makes gas turbines. Big ones. And they are shipped all over the world. Generally, each customer orders a slightly different version of the basic engine.

"Before we switched to reprographic techniques, we would redraft the entire drawing, even if the change was no more than 10%. Now we make a blowback from microfilm or create a same-size photo copy, opaque unwanted detail, then redraft as required. Or—if the changes are going to be minor—we reproduce it on wash-off film and let the drafter wet-erase what is not wanted and then draw in the new details.

"We figure—even with the limited mechanized processor we had when we first went to reprographics—that we saved $42,000 in engineering drafting time the first year. And that saving was in spite of the fact that we had to start up a new facility and hire two technicians to run it.

"Later we installed a Kodak Supermatic processor and relocated our drafting reproduction area next to our photo lab and copy camera area. As a result, we've found that we're saving about 50% of the processing time for the photo lab and the copy camera facility. Everything we turn out—from publicity photos to engineering drawings—is going through the Supermatic processor."

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Send for more details about Solar's use of reprographic techniques, plus, a complete listing of Kodak products and other applications. Write: Eastman Kodak Company, Graphics Markets Division, Dept. R04804, Rochester, N.Y. 14650.

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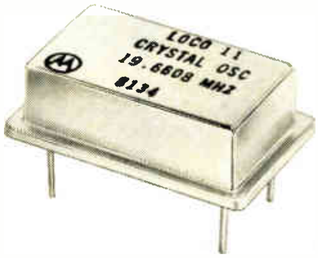

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Circle 66 on reader service card

CCD filter reverses structure to hike performance

Parallel-in/serial-out integrated design has better frequency range and spurious rejection

Taking a different tack from other designers of integrated low-pass filters based on charge-coupled devices, a Siemens AG engineering team is developing a parallel-in/serial-out design. This reversal of the conventional CCD filter configuration simplifies construction and improves frequency performance.

The applied signal is sampled at the input of each CCD element instead of at the device input. Since the outputs now are summed within the CCD itself, no separate output differential amplifier is needed, points out Karl Knauer, a member of Hans-Jörg Pfleiderer's team.

What's more, the Siemens device couples a higher frequency range to attenuation and noise characteristics at least as good as those of other configurations. It also offers a better solution to the rejection of frequencies in the regions containing clock-frequency multiples.

Uses. Integrated CCD filters are replacing bulky discrete filters used, for example, in telephone equipment to reduce speech frequencies to 3 to 4 kilohertz. While not appreciably impairing intelligibility, such a reduced bandwidth greatly simplifies equipment engineering. The new Siemens design is still under development, however, so it will be some time before it goes to market.

The device uses double polysilicon technology and has a filter area of 1 square millimeter, excluding the drive circuitry. The electrode length checks in at about 10 micrometers.

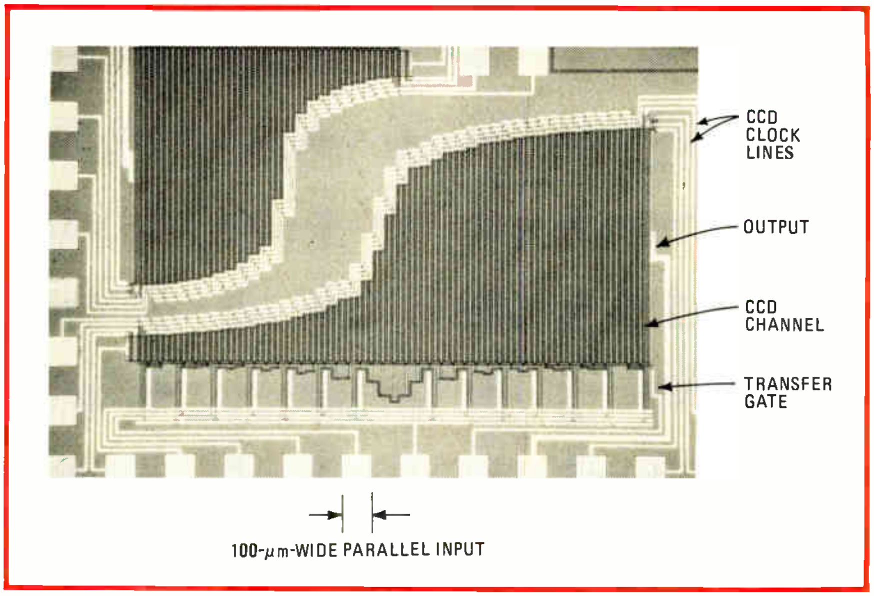
Operating at clock and transfer gate frequencies of 12 and 24 kHz respectively, the CCD filter shifts the charge packets individually through its 43 elements towards the output. There, the charge is picked off either directly or it is applied to a source follower, also on chip, where it is tapped off as a voltage signal.

The Siemens device is a low-pass filter with a ±0.5-decibel attenuation in the 0-to-3.4-kHz passband. The stopband, which starts at 4.6 kHz, has an attenuation of almost 30 dB. Thus the signal power there is reduced to less than 1/1,000 of its beginning value.

With a 3-volt input signal, the noise for a frequency window of 300 hertz is 80 dB below the signal amplitude. That represents a signal-to-noise ratio of about 70 dB for an effective noise bandwidth of 1.7 kHz, while harmonic attenuation is 40 dB. Both these values roughly correspond to those in other CCD filter configurations, Knauer says.

Performance. Much improved, though, is the frequency performance of the new filter. With conventional versions using the serial-input scheme, the input frequency is limited by the CCD clock frequency. With the new parallel signal-input approach, on the other hand, the input frequency can be n times higher than the clock frequency, where n is the number of electrodes per element, Knauer points out. Thus, the filter can process signals of much higher frequency with no increase in clock frequency.

The higher input frequency helps



Reversal. Low-pass charge-coupled-device filter brings in signals in parallel and samples them at the input of each CCD element. Outputs are then summed within the CCD itself.

implement a novel method for rejecting unwanted clock-frequency multiples. For a given number of CCD elements and for a constant clock frequency, the number of inputs per element—and hence the input frequency—can be increased.

Because it prevents signals around the clock frequency from entering the filter, increased frequency allows a filter design that can suppress undesirable frequencies without having to go to additional circuitry, Knauer says. Such compensatory circuitry, obviously, would only consume valuable space on the chip. □

Great Britain

23 symbols digitize speech in modeling mode that plots them on a two-dimensional array

Digital encoding of speech may take a giant stride forward if a still-experimental time-encoding technique from Bath University lives up to its first promise. Its developers say it could pack four speech channels into a conventional 64,000-bit-per-second digital link. Moreover, where voice quality of less than the international standards is acceptable—military or mobile-radio applications, for example—it could achieve 5,400-b/s data rates at a cost much less than that of other coding techniques. Eventually, high-reliability digital voice communications could be achieved in as small a bandwidth as 5 kilohertz, the pair believes.

Developed by Brig. Reginald King of the UK army and William Gosling of Bath University, the still-experimental technique [*Electronics*, Aug. 3, p. 66] would have applications in voice synthesis, speaker verification, and word recognition, as well as in telecommunications.

Prototype. Computer simulations of the patented technique (see "The proliferation of digital speech encoding") have been carried out at Bath on a PDP-8 minicomputer, and the next step is a prototype system comprising an analog-to-digital converter, a buffer store, a microprocessor, and a read-only memory. The developers have just come up with a new coding technique that needs refining, so that it may take 18 months to reach the hardware stage.

The new technique evolved when King, director of army telecommunications of the Ministry of Defence, accepted a research fellowship at Bath University last year. He set out to identify those elements in a speech waveform that carry high information content, with his experiments centered on breaking down speech into naturally occurring segments and then classifying these.

King discovered that every second of male speech has around 900 segments, each occurring between successive real zeroes of the waveform. As described in "The proliferation of digital speech encoding," he represents them with 200 basic types, such as half-sine waves. With a mapping technique, he was able to reduce these 200 shapes to 23 symbols, each of which can be represented by a 5-bit word.

The encoder spews out a new word after every zero crossing, producing around 900 a second, so the basic data rate is 4,500 b/s. If speech is to be modulated for loudness, an 8-bit word defining amplitude can be added after every eight symbols, giving a 5,400-b/s data rate. Each data word received calls up the corresponding waveshape from a read-only memory, and this is

The proliferation of digital speech encoding

There's a baseball saying that "you can't tell the players without a scorecard," and it applies to the fast developing field of speech digitizing as well. One basic way to convert speech into a digital format is to encode the entire waveform by some technique such as pulse-code modulation. Because telephone companies are already investing in PCM, it has high visibility.

However, PCM requires a wide bandwidth to store all the bits necessary to faithfully reproduce the speaker's exact waveform. Thus much attention is going to various bandwidth-compression techniques, many of which start with new ways of encoding speech. Among these techniques are the new Bath technique, linear predictive coding [*Electronics*, June 22, p. 39], and formant tracking voice coding (a frequency-domain technique, rather than a time-domain process like the other two).

Essentially these three approaches are modeling techniques, which assume a predictable, relatively narrow frequency band of speech to be encoded. Such an assumption works well with speech.

The Bath technique reconstructs the original waveform from its constituent segments. It works because a single symbol can represent groups of similar speech segments with little signal distortion. Each segment is categorized by its duration and shape.

Duration is represented on a logarithmic scale so that short intervals are transmitted more accurately in absolute terms, but an approximately constant fractional accuracy is maintained for both long and short intervals. Segment shapes are compared with a catalog of shapes arrived at by trial and error after considerable research. "The problem is that the ear is not phase-sensitive, so shapes which look different on the oscilloscope may sound the same when heard," says Brig. Reginald King, who is codeveloper of the new Bath coding technique.

By itself, the Bath technique would give around 200 different possible combinations of wave shape and duration. However, King and codeveloper William Gosling found that these 200 symbols can be reduced to just 23 symbols by plotting time quantization on one axis of a computer's two-dimensional array and a list of shape categories on the other. A limited alphabet of symbols distributed uniformly over the plane can then be used to represent groups of naturally occurring symbols to which they are nearest.

clocked out in accordance with the encoded duration to reconstruct the original waveform.

The transmitted speech is sufficient for military applications because it gives high intelligibility and provides voice recognition, but it does not meet international telecommunications standards. While this will require the interleaving of additional amplitude-defining words and a larger alphabet of symbols, Gosling is confident that the standard could be met with a 16,000-b/s data rate. Thus four voice channels could be packed into the 64,000-b/s channel links that telephone companies are using for pulse-coded-modulated digital voice transmissions.

Cheaper. Previous research with linear predictive coding and formant tracking vocoders (which rely on the energy peaks in speech patterns to reproduce the frequencies) has succeeded in reducing the telecommunications bit rate to 2,500 b/s, but at a high price, says King. The Bath technique allows encoding in real time with little more than a microprocessor, whereas the other techniques require an extremely fast, and expensive, minicomputer.

The technique also lends itself to several voice-processing procedures. For example speech can be slowed or speeded by as much as 20% without change of pitch or intelligibility or loss of speaker recognition. Thus the Donald Duck quality of the speech of helium-breathing divers can be processed out. But for Gosling, whose primary interest is in mobile-radio communications, the biggest promise the technique holds out is achieving high-quality digital voice transmission for the 5-kHz channel spacing projected to supersede the UK's current 25-kHz allotment. □

Japan

Toshiba raises the electron-beam ante with automatic scaling, three exposure modes

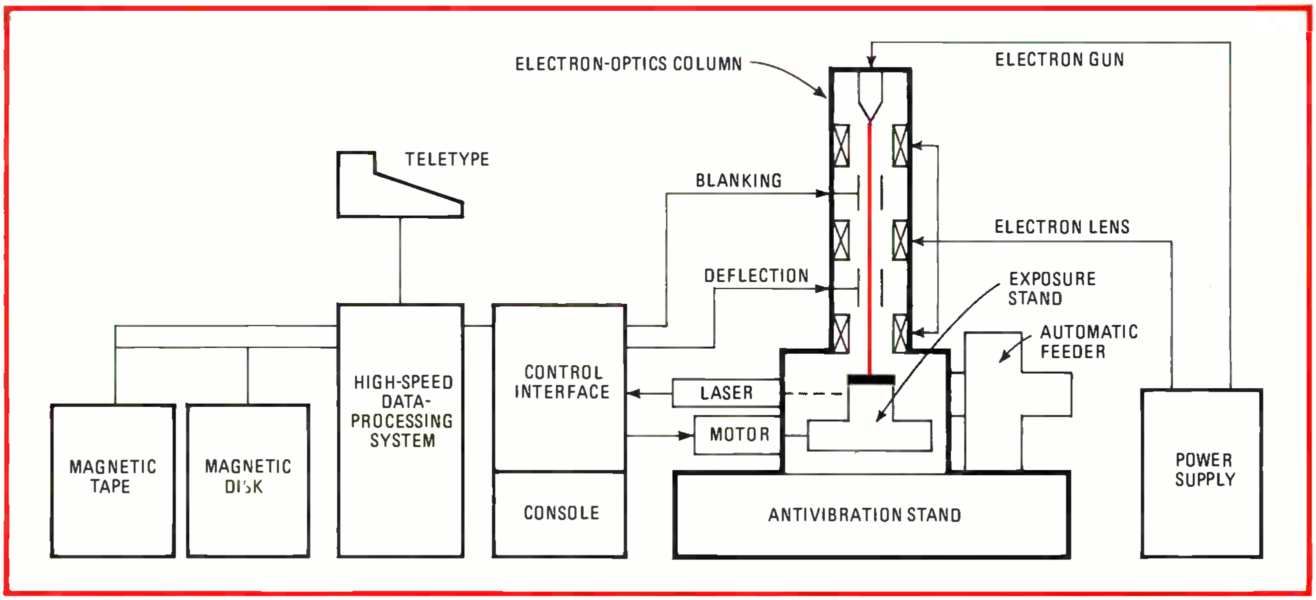
Weighing in just as the race in the electron-beam lithography systems is starting, Toshiba Corp. seeks to outdistance its American rivals with features that add flexibility to its new $2 million-plus machines. With these, the Tokyo-based firm thinks it can win a respectable 30% of its estimate of a worldwide market for 100 systems.

Back of the Japanese company's confidence are two features in particular: automatic scaling of the lines being exposed on a mask or a reticle and a choice of three minimum line widths in exposure.

Development of the new electron-beam exposure system [*Electronics*, Aug. 3, p. 65] was carried out at Toshiba's research and development center, with commercial systems being fabricated by affiliate Toshiba Machine Co., a Tokyo manufacturer of machine tools and industrial machinery. The EBM-105 enters a marketplace occupied by two American firms' units, which are derived from Bell Laboratories' electron-beam systems.

Scaling. Automatic scaling makes it easy to change mask dimensions without a complete redesign. It works by making incremental changes in the spacing and length of lines on the scanning raster that the electron beam follows as it traces the pattern on the mask or reticle.

The user simply feeds in the scaling factor, and the only difference from his point of view is that the machine runs a bit slower or faster. Scaling is provided over a −30%-to-+20% range. In the 1-micrometer line mode, it is in 10% steps; in the



On target. Toshiba's new electron-beam lithography system offers automatic scaling of lines being exposed, which permits easy changes of mask or reticle dimensions, and a choice of three minimum line widths in exposure. Scaling is provided over a range from −30% to +20%.

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Instantaneous Forward Voltage @ 3.0A:
1.0V @ 100°C
Capacitance @ 12V DC (Max.): 58 pF
Single Cycle Surge Current: 75A
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Types: 1N6079, 80 & 81 *(Trr 30ns)*
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2-μm mode, it is in 5% steps. Moreover, the scaling ratio can be changed for each raster, which has a scan width of 128 or 256 μm.

Three exposures. As with the U. S. machines from Varian Associates' Extrion division and Etec Corp., the Toshiba system has exposure modes with 1- and 2-μm minimum line widths. Accuracy in the 1-μm mode is ± 0.1 μm, and the time required to write a area 100 millimeters on a side is 208 minutes.

In the full-wafer mode appropriate for today's semiconductor technology, the minimum line width is 2 μm with an accuracy of ± 0.13 μm. The time to write a 10,000-square-millimeter area is 58 min.

The added 4-μm mode is intended for making reticles of single chips at about 10 times the speed possible with optical-pattern generators. For these reticles, intended for step-and-repeat projection printing, accuracy is ± 0.15 μm. Time for a 10,000-mm^2 area is 34 min.

Toshiba's American competitors seem not at all fazed by the EBM-105. Of the automatic scaling feature, John A. Doherty, senior research engineer at Extrion in Gloucester, Mass., says "It's a relatively straightforward process. In fact, we should have something like it on our own systems within a few months." He also questions the need for the 4-μm exposure mode, saying, "Extrion has the ability to generate reticles at a normal resolution now, and we are working on one with a resolution of 1 μm."

A spokesman for Etec in Hayward, Calif., balked at discussing features and specifications. But Peter L. Wolken, director of marketing for the industrial products division, did say that Etec's MEBES is not a rigidly fixed design and "more advanced capabilities are continually being developed for it." Of Toshiba's prediction of a market share of 30%, he notes that his firm has a big leg up because it has 10 machines in place, including three in Japan.

Looking to the future, Toshiba will accept special orders for systems making 6-inch masks that can work with 5-in. wafers. Another bonus of the new Toshiba unit is its ability to mix several patterns or variations on a single pattern on the same mask without loss of speed. This feature can be especially useful during developmental work. □

France

Integrated drivers keep lamps alight

The reliability demands that industry places on electronics are nowhere more evident than in signaling applications, where, for example, an indicator lamp *must* work. And there's no better way to boost reliability than a well-designed integrated lamp driver, figures the Sescosem division of Thomson CSF.

The division has already launched a family of integrated drivers for a supply range of 12 to 30 volts, which is finding considerable use in applications in nuclear and conventional electric power plants. Now it is expanding its family and beginning to offer it internationally for a more diversified group of applications.

Advantages. With integrated drivers, it is easy to provide current limiting and thermal protection, says Sescosem engineer Pierre Eliaers. "If a conventional approach is used [to current limiting], you have to use a big output transistor to protect the circuit. This would be an integrated circuit in itself and also would be expensive," he says.

Another advantage, of course, is size. A printed-circuit board with discrete components occupies more than three times the area of Sescosem's integrated versions.

Apart from lamp driving, the Grenoble division sees the family driving relays and step motors, where its comprehensive short-circuit protection will be valuable. Other applications could include lamp driving with built-in alarm blinking, deferred switching with up to a 30-second delay, and serving as a power comparator.

With the 1607 family, Sescosem has emphasized good short-circuit protection and thermal-shutdown procedures. The family members are all monolithic drivers that have input stages based on the well-known 741 operational amplifier with high gain and input impedance.

The devices are essentially blow-out-proof, Sescosem says. To keep peak output current down to a safe value, they have internal or external resistors at the output stage. A current rise increases the voltage across the resistor, and above 0.6 v, a transistor diverts the current.

Thermal shutdown is effected by a group of transistors that cause the output to drop to zero when the temperature rises above 150°C following a short circuit. When the temperature rises, the voltage across a resistor increases and creates a current in a transistor. This current turns on another transistor, and its current biases an output transistor, which diverts current.

A small positive feedback in one of the transistors provides hysteresis of the thermal-shutdown circuitry. The device changes its on/off state over a range of once every 4 seconds to twice a second. Thus it does not vacillate rapidly between on and off during a long-lasting short circuit.

Members. Now available as samples are two new family members, the TDE 1647 CM and the TDE 1617 CM. The 1647 can withstand a short circuit between power supply and output, useful for testing a lamp during maintenance. The similar 1617 integrates the resistor that limits the current.

To be available in samples this fall is the integrated-resistor TDE 1627 CM, which will have a light-emitting diode to signal a thermal shutdown. Moreover, the circuit will not reopen until it has been reset externally.

Other family members, intended mainly for lamp driving, are the original TDE 1607 CM to handle lamps up to 6 watts, the ESM 1607 G for 2-to-3-w lamps, and the TDE 1637 CM to handle peak voltages of 50 v up to 10 milliseconds. In volume orders, all the devices cost between $1.50 and $2, and all are compatible with most semiconductor technologies. □

Will atomic particles communicate?

Modulated beams of neutrinos offer the possibility of secure, nonstoppable communications systems

by Harvey J. Hindin, Communications & Microwaves Editor

How about a point-to-point telecommunications system so secure it can't be jammed short of blowing up the transmitter or receiver? Or how about a communications signal so intense it cannot be stopped by any known means and can travel through the earth in a straight line from one side to the other?

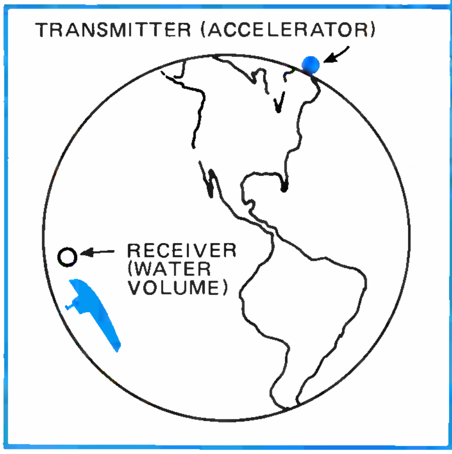
The possibility of developing such a system exists, built around modulated beams of neutrinos, those extremely energetic atomic particles generated by proton accelerators (see "A very particular particle"). Such a system could provide the U. S. Navy with a secure mode of communication with its submarines.

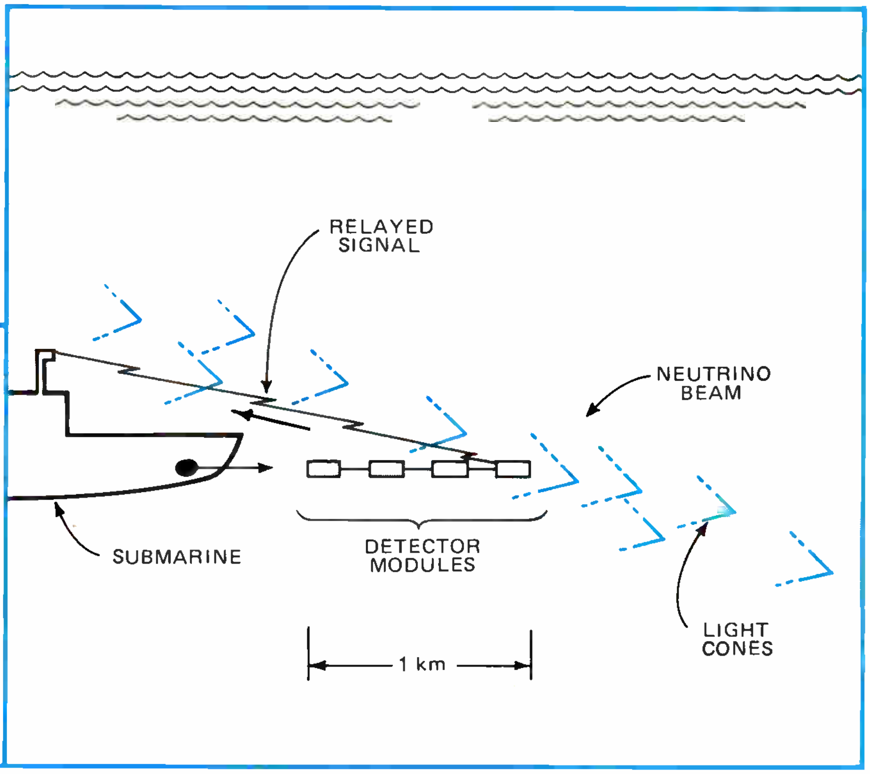
Though no one will comment, the neutrino-beam system could possibly place the Navy's proposed Project Seafarer, a much—criticized and much-delayed system that would need a vast area in northern Michigan for its low-frequency antennas. Another possibility is to build a transmitter in a command post deep in solid rock—a hardened site that would have no effect on the transmission of neutrinos.

Even a prototype of the neutrino-beam system is anywhere from 5 to 10 years away. But concepts for its design are beginning to emerge. Interestingly, the upper limits on the data rate are a subject of disagreement between the two groups of prime researchers supported by the Office of Naval Research.

One group of investigators is at the Naval Research Laboratory in Washington, D. C.,; the other is at Western Washington University in Bellingham, Wash. Both groups envisage a transmitter consisting of a high-energy proton accelerator—like the 400-billion-electronvolt unit at the Fermi National Accelerator Laboratory in Batavia, Ill. It could be modified to produce a narrow neutrino beam having a divergence as small as 1 milliradian that could be aimed at a detector half way around the world. This detector must be located deep within a huge volume of water becauce neutrinos can only be detected indirectly, from the radiation they emit upon striking the neutrons or protons of water molecules.

The accelerator would produce a neutrino beam every 8 seconds by





Repeaters. Acoustic, radio or laser repeaters might relay signals carried on neutrinos from submerged photodetectors to a submarine, thus achieving practical surface-to-underwater communications.

slamming a high-energy proton beam into an aluminum target. This produces unstable particles that decay into muon neutrinos and other particles. If bending magnets are used to deflect the proton beam properly, the resulting muon neutrino beam can be precisely pointed through the earth to the distant detection site. The photomultiplier detectors would be mounted on clear plastic plates enclosing a huge cube of water.

The data rate. Albert Saenz and his co-workers at the Naval Research Laboratory have carried out quantitative studies considering neutrino beams both from the present Fermi lab accelerator and from the coming upgraded version dubbed Tevatron, which is designed for proton energies of 1 teraelectronvolt (tera = 10^{12}).

They find, in one case, that rates of 10^4 signal counts an hour, sufficient for a 2-bit-per-second communications link, should be achievable using the Tevatron and detectors surrounding 10^8 tons of water. The path length was assumed to be 10,000 kilometers.

In one configuration, Saenz's system would require about 1,000 detector modules in a synchronous detector scheme more than 700 meters below the water surface. His calculations indicate a 15-bit binary message could be sent during the 8-second accelerator cycle.

Saenz hopes to complete his feasibility studies soon and then make "modest experiments" over 5 to 10 km at Fermi, using a specially designed communications device to modulate the neutrino beams. He estimates that ultimately tens to hundreds of bits a second are possible.

In a communications system proposed by Peter Kotzer and his colleagues at Western Washington University, however, many fewer detectors would do the job. Only four modules containing three photodetectors each would be needed, Kotzer says. These would be strung out at intervals along the center line of a cylindrical water target, 10 meters in radius.

Kotzer says a message bit rate of 53.1 megabits a second is possible in principle if the target is made as large as 10^{10} or 10^{11} tons. He is testing detection modules in the open ocean and feels that the next logical step is simulation tests at Fermi.

Both scientists are quick to note that the differences between their data rates depends on their assumptions. The modulation scheme, the accelerator power and spectrum assumed, the synchronization method, allowable error rate, water clarity, and detector volume are all variables, among others. And after all, long-distance tests have not yet been made. "We really won't know for sure until we do it," they both point out.

An important characteristic of the neutrino beams is that they can be precisely aimed to hit their targets—divergences are like those of lasers. It is estimated that they can pass straight through the whole earth with less than 1% attenuation.

Neutrinos cannot be stopped because they are so energetic, move at almost the speed of light, and almost never interact with other matter. Furthermore, there are no sidelobes or scattering considerations, and they are not affected by nuclear radiation or solar activity.

Making it work. Obviously, there are many problems to solve before the system is practical. Clearly an accelerator in the U.S. is conceivable for use as a generator. But where do you put remote receivers and how do you set them up? Also, a potential enemy would surely know of their presence.

Unfortunately, for all the schemes proposed, the received data rate is directly proportional to the detector volume and the cube of the neutrino energy. This means bigger transmitters and more water to get more information. Reduced volumes are only possible if the data rate can be low or the generator characteristics can be altered to provide more neutrinos in a given time.

In any case, the detectors are hard to fit into a cramped submarine. One possible scheme is to have the submarine sail into the volume of water at which the beam has been aimed. It then sends out receivers through its torpedo tubes, and the message is then relayed back over a short distance.

Alternatively, an acoustic neutrino receiver—a hydrophone-like device—could be placed in the water as a relay link. This receiver would also provide phase information translatable into intelligence.

If nothing else, a system with a simple Morse-code modulation and a low data date might be used for an unstoppable doomsday missile-launch message in the event of a global thermonuclear war. □

A very particular particle

Neutrinos are electrically neutral subatomic particles with presumed zero rest mass. They were postulated by Nobel prize winner Wolfgang Pauli in 1930 to satisfy the law of conservation of energy and momentum in a nuclear beta—particle decay problem. Their small size and lack of a readily observable interaction with matter has made them difficult to detect, and they were not found experimentally until 1956.

It has been determined that there are two neutrino types—the so-called electron neutrino and the muon neutrino. It is not clear that these particles are independent of each other. An as-yet unproven postulate holds that neutrino oscillations—a transition from muon type to electron type—can occur when the muon neutrinos travel large distances.

If the muon neutrinos are made to hit nucleons—neutrons or protons in the nucleus of the atoms in a large tank of water—they cause Cerenkov light to be emitted. This is the same light observed as a blue glow in the water surrounding nuclear reactor cores. It is detectable by a photomultiplier receiver.

Detection must take place far enough below the surface of the water so the photomultipliers will not be counting muon neutrino noise signals resulting from sunlight and cosmic rays. Bioluminescent flashes may also be a problem, and it is not known what effect neutrino oscillations over the typical 1,000-to-10,000-kilometer paths might have on detection efficiency.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Solid state

ECL memories speeding to market

Push of emitter-coupled-logic RAMS into mainframe applications pits it against popular metal-oxide-semiconductor versions

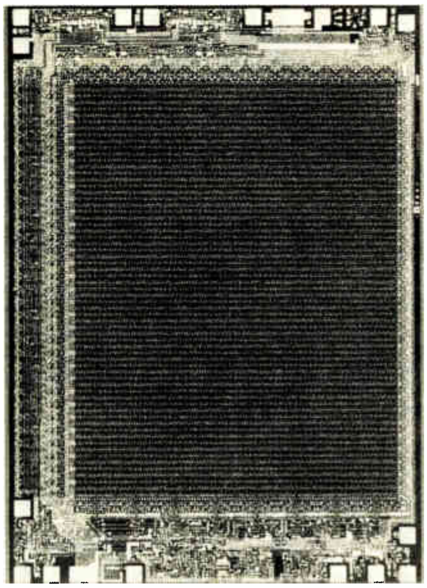
by William F. Arnold, San Francisco regional bureau manager

As the access times of n-channel MOS static RAMs drop, bipolar makers might begin to fear for their transistor-transistor-logic memories. But they have a strong ace up their sleeves: emitter-coupled logic. The push of ECL into the next generation of mainframe computers is now fueling a market for comparable random-access memories. With the growing market come new devices and suppliers to offer users the blinding speed that bipolar technology currently enjoys *vis à vis* metal oxide semiconductors.

For example, there are 265-by-4-bit ECL RAMs in production or on tap that feature 7-to-10-nanosecond access times. And Fairchild Camera & Instrument Corp., Mountain View, Calif., considered the market leader, calls its 35-ns 4-K devices the fastest 4-Ks ever made and expects to lower those specifications to 20 ns typical and 30 ns maximum by next year.

Also, in early 1979, Motorola Semiconductor Products Inc., Phoenix, plans to have a 4,096-by-1-bit RAM in the 25-ns range, and Fujitsu Ltd. from Japan is readying a 25-ns 1,024-by-4-bit RAM for sample quantities in October.

Competition grows. These three firms will not have the market to themselves. National Semiconductor Corp., Santa Clara, Calif., which makes mainframe computers for Itel Corp., declares that it is committed to becoming an ECL memory house. Within a month it plans to launch a 1-K-by-1 RAM in the 25-ns range and will follow that with other ECL parts. Signetics Corp., Sunnyvale, Calif., in collaboration with the French Philips' subsidiary, RTC, says it has a fairly aggressive plan to enter the marketplace, beginning the end of this year with a 15-to-20-ns 1-K-by-1 RAM.



Such speed works well in cache memories and variable control stores in conjunction with the central processing unit in the coming medium- and large-scale mainframe computers. Fast RAM control stores also make a hit with mainframe designers who switch from programmable-read-only-memory control stores. Add-on memory makers also show interest in the parts. Further, because of its access times, ECL is finding uses in such applications as on-line radar processing, data encryption, telecommunications, and intelligent terminals.

"It looks like ECL is finally coming to pass," observes Steve Steward, product marketing manager for static memories for Fairchild's LSI group. "Today, all medium and large computers are going ECL and it's opened up opportunities for a lot of ECL memories."

Steve Jasper, strategic marketing manager for Signetics' bipolar memory division, says that two to three years ago ECL was hard to justify: although it was faster than TTL parts on a component level, its marginally increased speed did not match the development cost. Now, with the emergence of ECL gate arrays [*Electronics*, April 27, p. 83], system speeds become impressive with ECL devices.

Solid gains. Of course, the ECL memory market is still a long way from matching the dollar value of MOS versions. Fairchild's Steward estimates this year's ECL memory market at $10 million to $20 million world wide and says it should continue to grow from 15% to 20% a year for several more years. Signetics' Jasper thinks that ECL RAMs alone will do $30 million by 1981.

A more bullish estimate comes from Frederick L. Zieber, vice president at Dataquest Inc., Menlo Park, Calif., a market research firm. He charts the market at less than $20 million last year, of which two thirds were RAMs, about $35 million this year, and more than $50 million in 1979. By contrast, he notes that the TTL memory business is $100 million this year, or close to $200 million if PROMs are included.

To the charge that ECL devices are larger and dissipate more power than MOS ones, Fairchild LSI applications manager Bruce Threewitt points out that its 4-K RAMs measure only 17,000 square mils. Next-generation cell sizes are less than 1 square mil right now and the speed-to-power ratio is close to MOS statics'. □

Commentary

Selling Japan

This may be the moment for American electronics companies to push their way into Japan, now the land of the rising yen

by Charles Cohen, Tokyo bureau manager

Japan is a strange country in which the mechanisms of the marketplace stop working in difficult times, observes the head of the research department of one of the island nation's largest banks. It would be hard to find a better capsule description of the state of the Japanese economy in recent months. Look at what has happened. The value of the yen compared with the U. S. dollar has soared out of sight, yet Japan continues to pile up foreign-exchange surpluses. Contrary to usual economic thinking, the level of imports is not climbing, nor are imported consumer goods decreasing in price.

Modern Japan has been a net importer of raw materials and fuel and an exporter of manufactured goods ever since the Meiji period of the late 19th century. After the 1973 oil crises, it put even more effort into exports, to pay for fuel, raw materials, and food. But by 1976, Japan was succeeding all too well. Exports increased much faster than imports, and foreign reserves piled up. The floating yen rose, slowly at first, until last September when it started soaring.

More government money. For its part, the Japanese government promised other governments that it would encourage the growth of its domestic economy and pushed through two supplemental appropriations bills last year to give it a boost. At least one, and probably two, appropriations are also scheduled for this year. But still exports continued apace and Japan's foreign reserves increased to their present level, which has topped $29 billion.

Although Japan's manufacturers

have long since outgrown their reputation for poor-quality merchandise, they have never graduated into the Rolls Royce class either. To a large extent they have followed a high-quantity, low-margin policy. In many industries the margin has been sufficient to support entire companies and even entire industries with no domestic market. The recent boom in citizen's band radios is a good example.

Even some famous companies are primarily export-oriented; for instance, 57% of Sony Corp.'s sales are overseas. Other manufacturers have been eager to export products usually sold on the home market provided the price is sufficient to pay direct costs plus a portion, not necessarily all, of indirect costs. The goal of these manufacturers is to boost volume and bring down overall cost per unit.

Popularity. This approach is especially popular today when domestic demand is sluggish, business is needed to keep employees at work, and the high exchange rate of the yen is pressuring prices. Besides cutting their own margins, manufacturers are demanding and getting price reductions from suppliers, who must bear the brunt of hard times, like it or not.

On the other hand, Japan's importers of manufactured goods tend to be a different breed of cat. During most of the period since World War II, imports have been limited by foreign-exchange quotas. Also, Japanese importers were allowed to establish sole-agency relationships with foreign suppliers and prevent others from importing the same product. The upshot has been that importers have acquired a monopoly mentality and tended to price goods at levels that would just enable them to sell a year's quota in a year rather than increase consumption with lower prices. Historically, foreign goods have had a reputation for quality and snob appeal, so that prices could be kept high. (There is even a Japanese word that has a very favorable connotation, *Hakuraihin*, which literally means a product that has arrived by boat.)

Quotas no longer exist for most products, but importers have not changed their stripes. They are still content to maintain an exclusive image and sell small quantities at high markup.

The situation in commodities is also astonishing. Beef imports, for example, are both limited in supply and subject to a $3.25-per-kilogram surcharge, ostensibly to obtain funds to promote the domestic beef industry! Newspapers often speculate about where the money is going, but nobody seems to know.

The amounts involved are substantial—per month the sums are more than government support for Japan's research and development project in very large-scale integration, which peaks in 1978 at 10 billion yen for the year. On the other hand, imports of fuels and raw materials continue to be low because of the low level of the economy.

Floating yen. Thus, the opportunity to reduce the monetary reserve is being bypassed, and in fact, the government has resisted pressure from trading countries to decrease it. Instead, leaders have counted on the floating exchange rate to bring trade into balance, which has clearly not happened. It is anybody's guess where the value of the yen will go from here, but there are some estimates that it could possibly hit as high as 160 yen to the dollar from the present level in the 180s. Nobody expects a quick return to the "normal" 220–240 range.

Exports could run at constant value until the end of September, because many export contracts run that long, further swelling Japan's reserves and bringing more pressure on the yen. It may be almost impossible for many companies and even whole industries to make new contracts for the second half of the Japanese fiscal year, which starts in October. It could lead to numerous bankruptcies.

But there are opportunities in all

this for American companies. Although Japanese importers have operated with a monopoly mentality, American manufacturers who control imports of their own products are taking advantage of the situation to decrease prices and increase market share.

Kodak recently marked down its color negative film enough to force Fuji and Konica to cut prices, too. Hewlett Packard's joint venture, Yokogawa–Hewlett Packard, claims to have made price cuts totaling 40% during the past year.

American semiconductor manufacturers generally have somewhat higher prices in Japan than in the U. S. because of demands for higher-quality devices, more service, and the costs of importing. That and the fact that they are continually cutting prices makes the effects of the exchange rate change hard to read, but industry observers say that the American manufacturers have been giving a good part of the exchange savings to Japanese customers in the form of lower prices.

Easing trade. Another potential bright spot for American electronics companies is the promise of favorable trade agreements. A Ministry of International Trade and Industry official says that Japan has in principle reached agreement with the U. S. on tariff cuts for integrated circuits and computers and terminals—though implementation will have to await multilateral agreement, especially with members of the European community. [*Electronics*, Aug. 3, p. 59].

Despite a marketplace that defies classic economics, manufacturers thinking of entering the Japanese market might find that now is the best time to take the plunge. Even though the market overall is not growing at a great rate, the exchange rate is extremely favorable. Japanese manufacturers are likely to be groggy from the loss of export markets and their need to support an excessive labor force. And banks are loaded with money that they want to lend at low interest rates—starting at a prime rate of 3.75%. □

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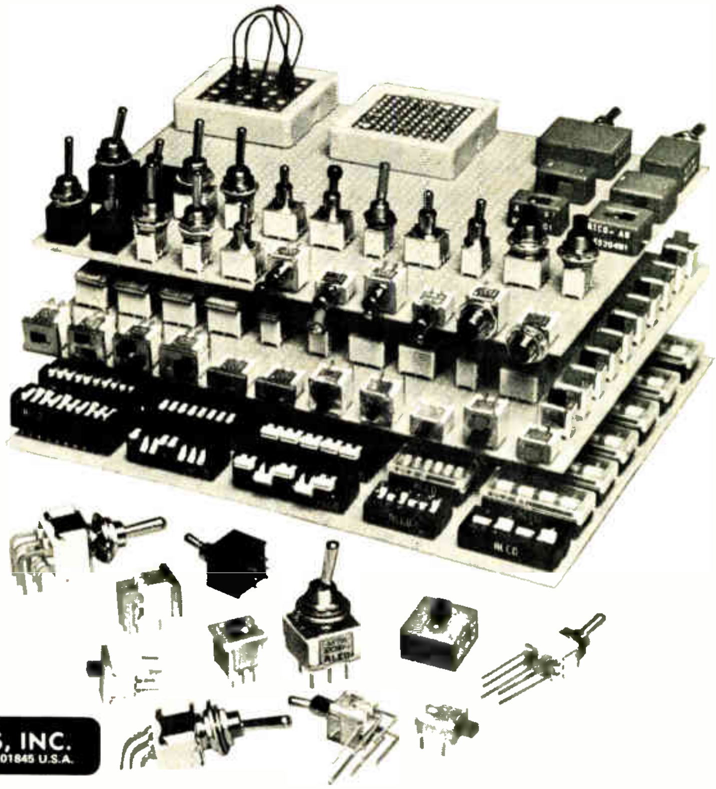

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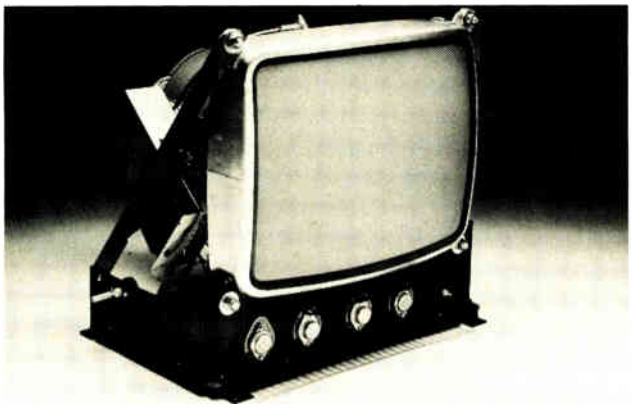

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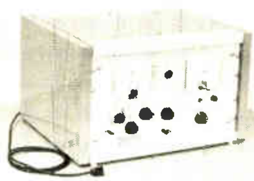

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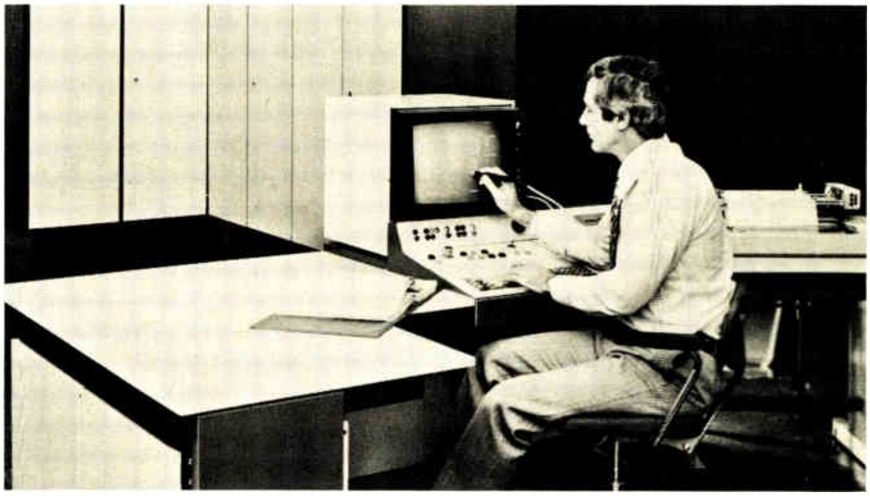
Computers

Eastern Europe steps up EDP efforts

Seven-country R&D program is aimed at a new series of machines to replace aging third-generation models

by John Gosch, Frankfurt bureau manager



From East Germany. The EC1055 medium-sized computer is the East German contribution to the Socialist bloc's ES-2 project. It is half the size of the EC1040, which it replaces. Designed with virtual memory, it includes a full line of peripherals.

Although hardly noticed by the West, Eastern Europe's seven-country council for mutual economic cooperation (Comecon) is putting its development effort behind a new line of computers that promises to give the Socialist bloc more clout and greater self-sufficiency in the data-processing field than it achieved with its first joint-effort series. Succeeding the third-generation ES-1 series [*Electronics*, Sept. 25, 1972, p. 72], the new "third-and-a-half" generation ES-2 family adds higher speed, a larger memory capacity, and more computing power to the group's present systems.

Participating in the ES-2 project are newcomer Romania and six oldtimers: Bulgaria, Czechoslovakia, East Germany, Hungary, Poland, and the biggest contributor, the Soviet Union. (In addition, Cuba is also participating.) Whereas Czechoslovakia and East Germany are each developing ES-2 systems on their own, the others are getting a helping hand from brother Russia. Romania is chipping in with peripherals only.

Major effort. Just how big the second ES project will turn out to be is difficult to pin down at this time, East Bloc officials say, but they are certain it will outrank the ES-1 program in both magnitude and yield. Not only that, but it may well develop into Eastern Europe's biggest joint-engineering effort, dwarfing even the Interkosmos space research program in which nine countries are participating.

Plans for the ES-2 series date back to 1973, when the four-year ES-1 development phase was coming to an end. A group of computer specialists from different Socialist countries conceived the idea and defined the goals for a successor family in terms very much like those of their capitalist counterparts.

"The targets are a better price/performance ratio, a wider range of applications, and the ability to transfer ES-1 programs to the new series," explains Ludek Vilner, who is deputy director of the research institute for mathematical machines located in Prague.

All in the family. Hungary is responsible for the EC1015, a small-sized computer at the low end of the ES-2 family. Czechoslovakia's contribution is the EC1025, also a small-class system. Next in line are three medium-sized machines: the EC1035, which Bulgaria is building in concert with the Soviet Union, the EC1045, a Polish-Soviet venture; and the EC1055, which East Germany is handling on its own.

Finally, there are two large machines, the EC1060 and EC1065, both from the Soviet Union. In addition, each country will develop and manufacture a number of ES-2 peripherals.

Far along are East Germany's EC1055, publicly shown for the first time in March, and Czechoslovakia's EC1025, due for deliveries toward the end of this year. Designed and developed at the Prague research institute, the 1025 is now going through its domestic tests. The international tests, conducted by the East European intergovernmental board for computer engineering, will get underway by September. The latter tests are to determine a model's compatibility and to find out how well it adapts to various tasks and applications. Also well along is the Bulgarian-Soviet EC1035.

Less is known about the USSR's progress on the large machines. The

ES1060 was originally claimed to have a capability of 3 million operations per second. That figure was subsequently reduced to 1.5 million and is now set at 1.3 million, according to the latest reports. There has been no official word of progress on the ES1065 other than a reference to an advanced system that will have a capacity of 5 million operations per second. On the whole, the Soviets have made slow headway on all their computer programs.

What's new. The ES-2 computers are different from their forerunners in architecture, hardware structure, efficiency, and performance. The prime architectural change is the use of a virtual memory that, in effect, considerably extends the operational storage capacity. As for the hardware structure, the new systems are modular with the various modules using a standardized interface.

Further, the ES-2 designers have given more attention to remote data-processing and time-sharing applications. The new machines also use a greater number of channels, employ block multiplexed data-transfer methods, and feature specialized processor modules that permit the use of board multiple processors. Testing and diagnostic software have been extended, too.

As for software, the East Germans, together with the USSR, have developed a new operating system, the OC6-EC, for the bigger ES-2 models. It is tailored to support the virtual memory, the block multiplexing channels, and other functional groups, as well as the ES-2 peripherals. The operating system comprises control programs, service programs, and language translators. The last are available for machine-oriented assemblers and the problem-oriented programming languages PL/1, Fortran, Algol, and Cobol. The Czechs have an operating system, the DOS3, designed for their computer at their research institute. This system can be used with all ES-2 computers up to the EC1045 model. However, the individual country can decide to use its own operating system.

Typical of the ES-2 family's low-end computers is Czechoslovakia's EC1025, the successor to the third-generation EC1021 of the ES-1 series. Its central processor consists of four to six independent modules, one or two main-storage modules, and an interrupt-control module.

Modular. This modular construction allows users to arrange the system to suit their application. It also permits the processing of instructions, the execution of commands and diagnostic operations, as well as communications with peripherals, to be carried out simultaneously. Each module is controlled by a microprogram in a control store.

The central-processor modules use transistor-transistor-logic integrated circuits, and the internal store employs large-scale integrated TTL devices. The latter will be replaced by metal-oxide-semiconductor circuits in future models. Accommodating the ICs are two-, four-, and eight-level printed-circuit boards, with the eight-level boards containing up to 60 ICs. At present, the 1025 contains some ICs from abroad, primarily from the Soviet Union, but eventually all will be home made.

An example of the ES-2 family's medium-sized systems is East Germany's EC1055, intended for commercial and scientific and technical applications. The machine, which can perform up to 450,000 operations per second, succeeds the country's EC1040 of the ES-1 series. Its cycle time is 1.2 microseconds.

The 1055's central processor is only half the size of the 1040's. This reduction, say officials of the country's electronics giant, Kombinat Robotron, is due in part to the use of MOS components in the operational store and of highly integrated TTL devices in the control and I/O units.

The computer's control unit uses the microprogrammed control concept, with microprogram memory of the partially loadable type. That memory has a capacity of 8,000 instructions, each with 65 bits. The cycle and access times are 400 and 140 nanoseconds, respectively. The 1055 has a maximum of four block-multiplexed and two byte-multiplexed channels, and the system's virtual-memory concept enables the user to resort to a memory providing up to 16 million bytes. □

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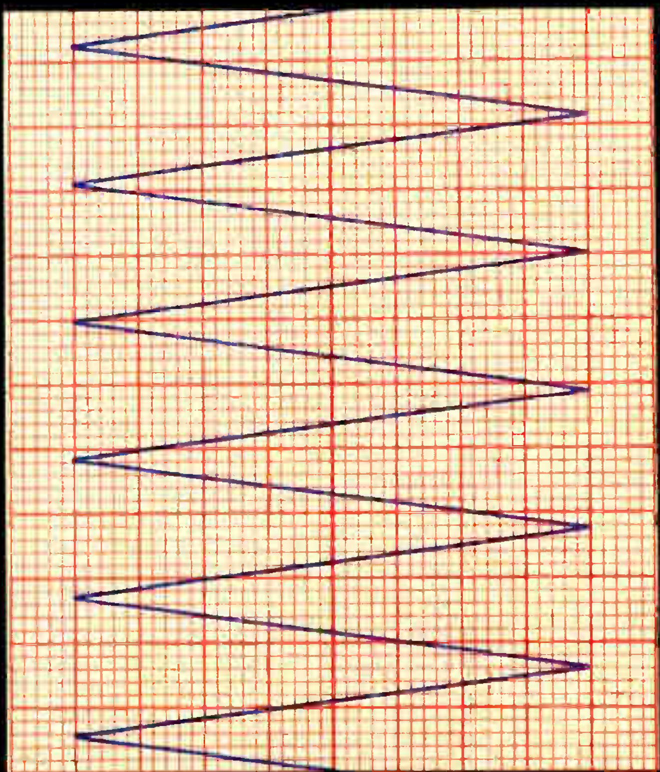

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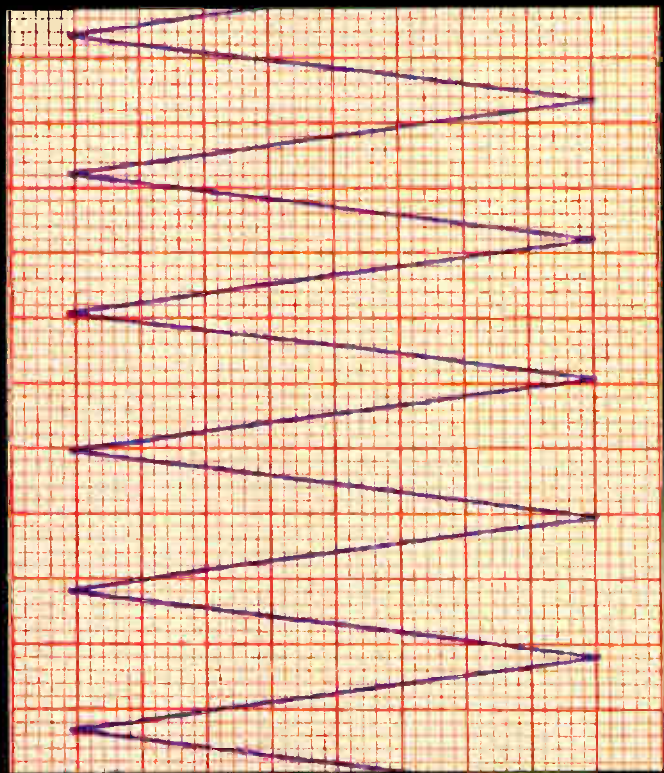

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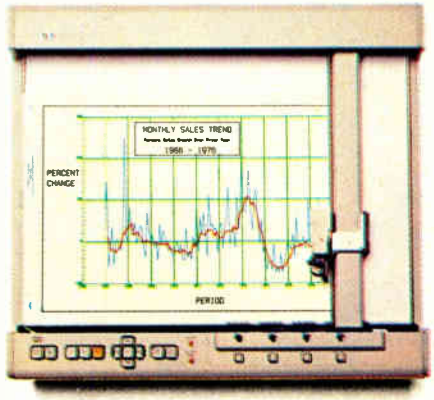

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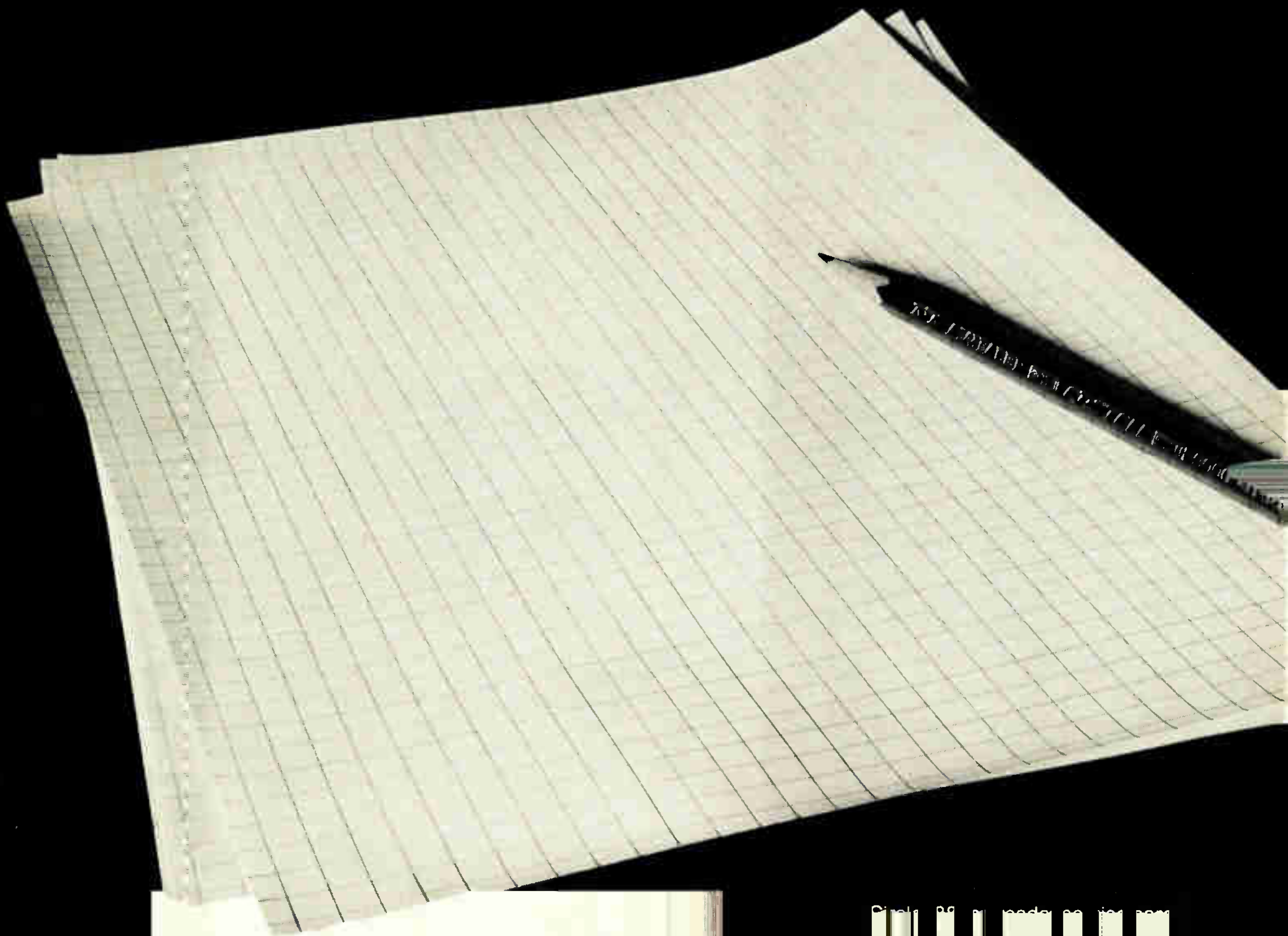


Distributed processing slashes development system's cost

Multistation network shares disk and printer among up to eight designers working with assorted microprocessors

by Bruce Gladstone and Paul Page, *Futuredata Computer Corp., Los Angeles, Calif.*

☐ No designer in a well-managed company has to line up to get at an oscilloscope. But he usually has to wait for access to a microprocessor development system, because few companies can afford an adequate number of systems now that per-station costs have risen to $15,000 to $30,000. Worse yet, most development systems are dedicated to a single manufacturer's microprocessor chips, even though many companies have already elected to use processors from a variety of makers in their products.

To blame for those prohibitive prices is the expensive but generally underutilized equipment attached to each station—the printer and the mass-storage device. The Futuredata multistation distributed microcomputer development system is unique in sharing these resources among up to eight stations. It is also unique in using distributed processing for such a purpose.

The stations in the new Futuredata system can each operate with a different microprocessor (8080, 8085, 8086, 6800, 6802, or Z-80 at present). Called Advanced Microcomputer Development Stations, up to eight of these AMDS terminals can be linked through a network control processor to one or more dual double-density double-sided disk memory units and to one or more medium-speed printers.

Each terminal has its own microprocessor central processing unit, up to 64 kilobytes of on-board memory, an 80-by-24-character cathode-ray-tube display with keyboard, and a wide range of optional enhancements. The network processor, besides controlling access to the disk unit and printer, provides either exclusive or shared access to files, freeing of active files when a station is powered down, and queuing of printing requests. Since each station is totally independent of the others, the system is crashproof.

A typical microcomputer laboratory installation, capable of supporting eight designers simultaneously, each developing products with different processors, can now be configured at a per-station cost of $7,694.

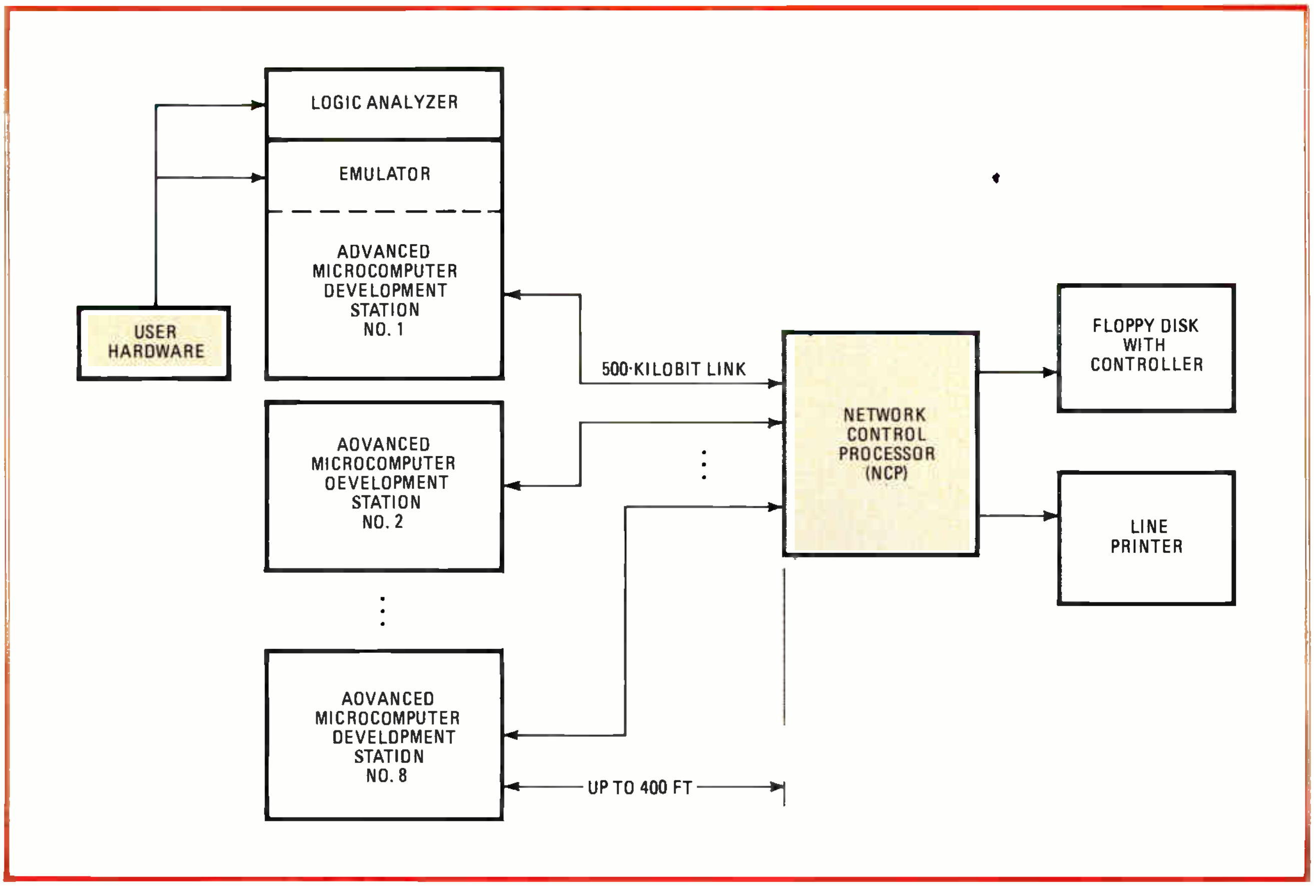
Why not time-sharing?

Other attempts to pool resources in microcomputer development systems have been made. But they have used time-sharing, not distributed processing, and therefore shared the central computing function and nothing else. The Tektronix 8001 emulation system, for example, relates to a large mainframe in a time-sharing mode, and in the Mupro development system the central microprocessor is time-shared.

The main reason for sharing the system processor and

TABLE 1: THE FUTUREDATA MULTISTATION DEVELOPMENT NETWORK

FEATURES	RESOURCES
An ultra-high speed serial data link capable of transmitting 50 kilobytes per second over a single twisted-pair cable at a distance of 400 feet	Sharable: disk mass memory, printer
A unique disk-sharing algorithm that gives many users access to the same low-cost floppy-disk mass storage	
A communications protocol that is very simple and requires minimum overhead	Possibly sharable: memory, processor
An Advanced Microcomputer Development System (AMDS) terminal that supports real-time processor emulation to 5 MHz	
A large local memory that dramatically reduces the frequency of disk requests	Nonsharable: keyboard, display, emulator*, logic analyzer*
Common hardware used for both the development terminals (AMDSs) and the network control function	
A high-level interface to the disk operating system that further simplifies the communications network	*normally required only for hardware debug



1. Shared resources. Unique distributed processing approach allows up to eight users to work independently; each satellite station can support a different processor type. Network control processor governs access to the disk unit and printer.

its memory has been the high cost of these elements. But the advances in semiconductor technology have changed all that and made it economical for the Futuredata system to give each user his own (micro)processor and a large local memory.

The need for control

In most microprocessor development projects, the designer needs complete control of the processor to use resources like interrupts and direct-memory access facilities. This is often in conflict with the requirements of an effective time-sharing system. In fact, once cost is no barrier, a separate processor and memory in each nonsharable element prove to be a necessity.

One designer's activity should not impinge on that of other designers', and in some cases, the designers will be working with different processor types. A general-purpose development network must allow each designer to have his own target processor.

Sharing memory can also be an inconvenience. Having his own memory space allows a designer to allocate memory space to his development task just as he wants. In addition, 16 to 64 kilobytes of random-access memory available locally greatly reduces the demands he has to make on the shared mass-storage device. If in editing a source program, for example, a substantial edit buffer is available on a nonshared basis, then the communication burden on the network and the number of disk requests will be greatly reduced.

In the Futuredata network (Fig. 1), the satellite AMDS stations are connected directly to the network control processor in a star configuration. The NCP in turn is connected to the disk(s) and printer(s) and runs a network control program to share these resources between the AMDS stations.

The AMDSs and the NCP communicate over a high-speed serial link and use common hardware. Thus, any AMDS may assume the network control function—in fact, it can even function on a stand-alone basis if connected directly to a disk or tape mass-storage unit. Such modularity and interchangeability mean that the network can easily be reconfigured to accommodate additional AMDSs or disks. It can also be easily switched to temporarily remove any nonfunctioning equipment.

The development station

The Futuredata AMDS station (Fig. 2) provides all of the nonshared resources that the microcomputer system design engineer or programmer needs. In the stand-alone configuration already mentioned, it is equivalent to present Futuredata microcomputer development systems and similar to the Intel, Tektronix, Motorola, and Zilog development systems. But as part of the network, it communicates at high speed with the NCP through a 50-kilobyte/second serial I/O port.

The station's most noticeable feature is a 12-inch-diagonal CRT display having 24 lines of 80 upper- and lower-case characters and also offering blinking fields,

How the disk-sharing algorithm was determined

A successful disk-sharing rule should allow several simultaneous users a reasonable response time without excessive overhead to switch processes. Disk performance can be judged by analyzing its critical parameters, which are:

T_S = average seek to new tracks = 100 ms

T_L = average latency period to access first sector = 167 ms/2 = 83.5 ms

T_N = latency between sectors during sequential reads or writes = 167 ms/7 = 24 ms

(The Futuredata disk operating system allows seven sectors to be read or written every revolution for an overall rate of 42 sectors per second.)

B = number of bytes per sector = 128

Insight into the problem can be gained from a look at two extreme cases. First, assume each disk request results in one sector transfer, so that there will be one seek and one latency delay period. Then each transfer will take 100 + 83.3 ms for a rate of 698 bytes/s. At the other extreme, if each AMDS operation goes to completion, seek overhead is reduced by fast transfer of sequential sectors. This unshared transfer rate would be 42 sectors/s × 128 bytes/sector = 5,376 bytes/s and would improve performance by 5,376/698 or 7.7:1—but some AMDS requests would have to wait an excessive time for service while long requests from other stations were reaching completion. Clearly, the best solution is to transfer several sectors per request but limit the amount of data transferred per request.

The transfer rate (TR) and average delay (AD) are:

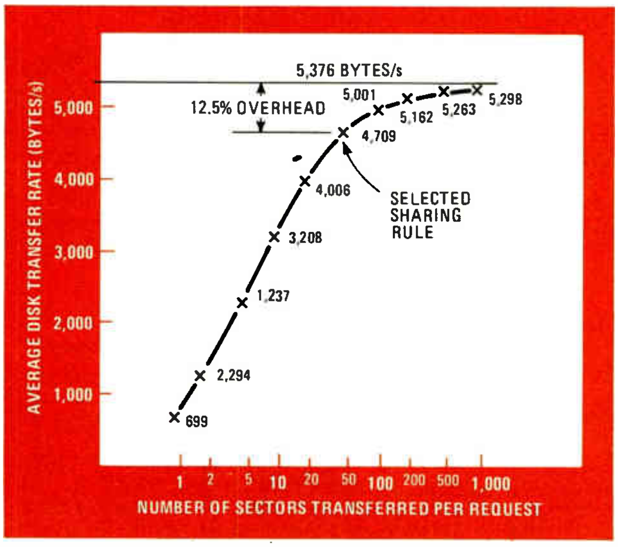
$$TR = (N \times B)/[T_S + T_L + T_N(N-1)] = 128\,N/[0.1 + 0.083 + 0.024(N-1)]$$

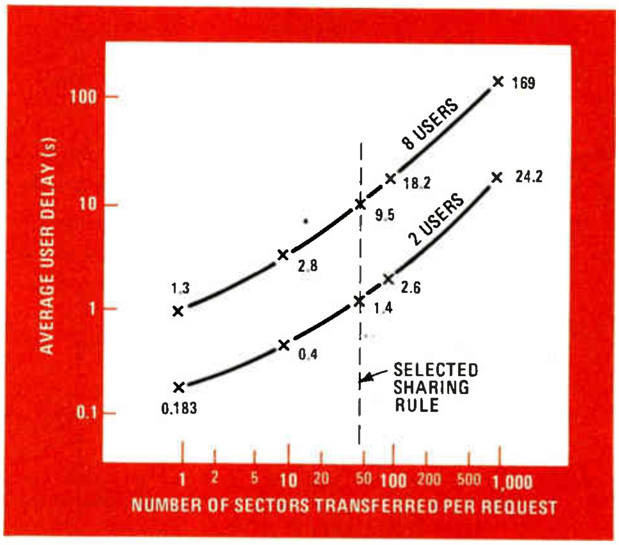
where N is the number of sectors per transfer, and

$$AD = (S-1)[T_S + T_L + T_N(N-1)] = (S-1)[0.1 + 0.083 + 0.024(N-1)]$$

where S is the number of stations requesting service

As the figures show, a maximum of 50 sectors per transfer introduces an overhead penalty of 12.5% and yields a delay of less than 9.5 s with eight users.



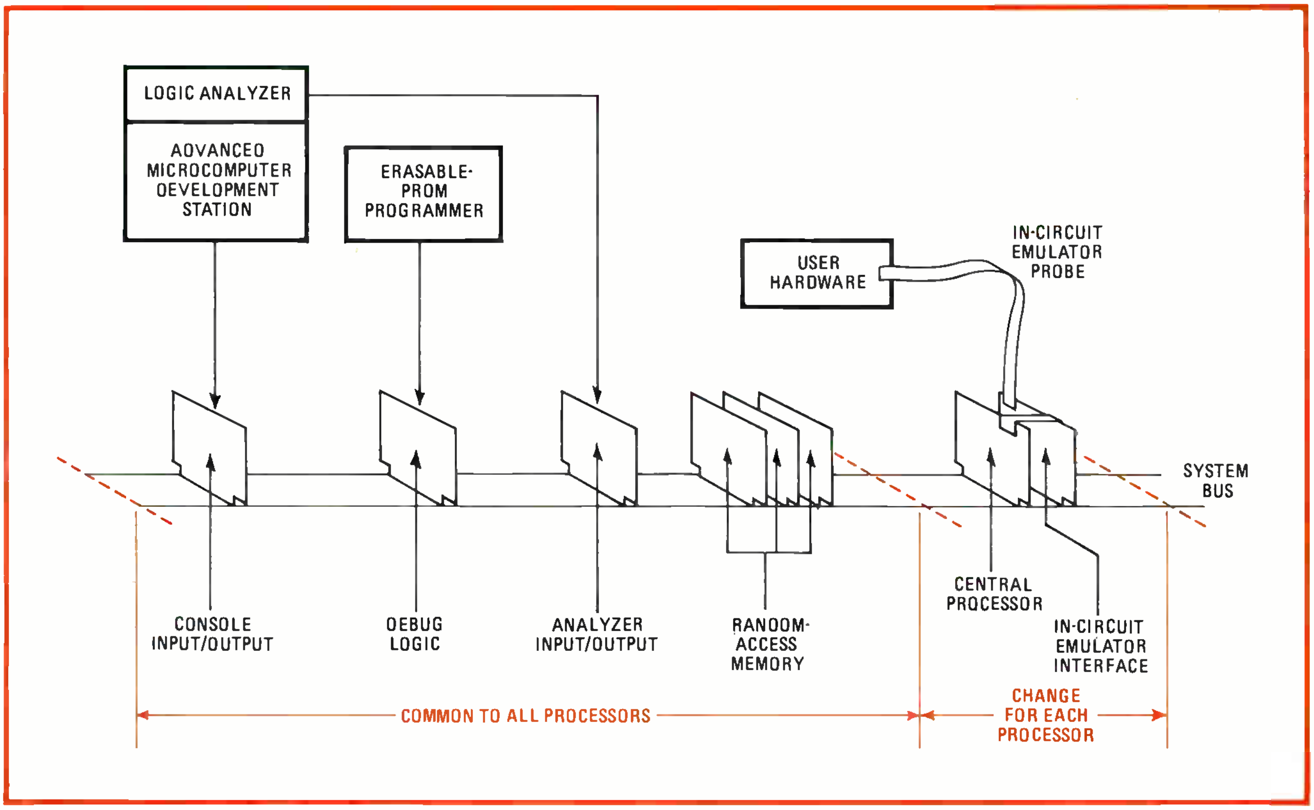


reverse video, underlining, highlighting, and line graphics. Beneath this is a 64-key upper- and lower-case keyboard with cursor control keys, edit function keys, system control keys, and "n" key rollover in a Selectric layout. The target 8- or 16-bit microprocessor may be either an 8080, 8085, Z-80, 6800, 6802, or 8086. Within the cabinet are circuit boards containing from 16 to 64 kilobytes of dynamic or static RAM; the 200-nanosecond static RAM allows real-time emulation of microprocessors up to 5 megahertz.

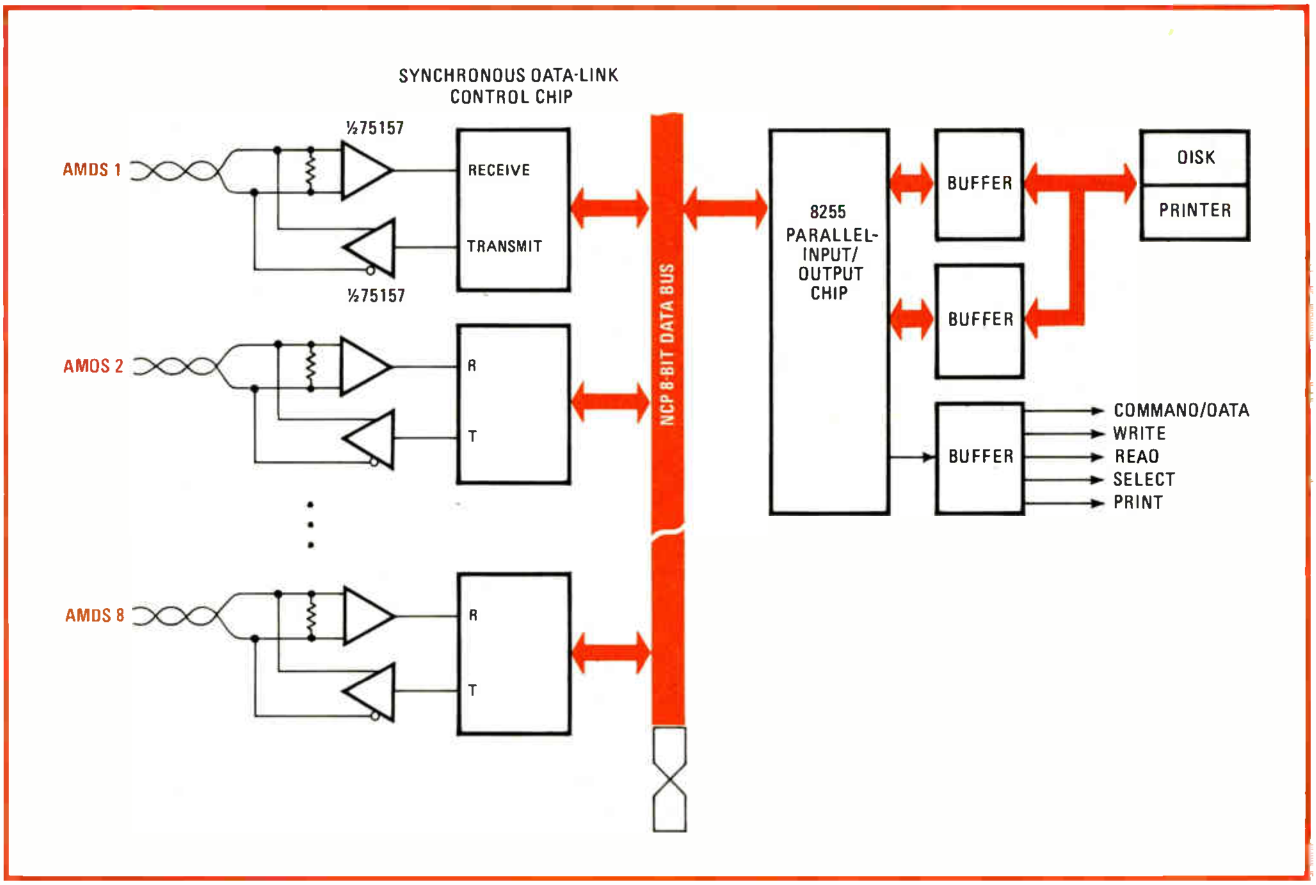
Optional emulators for 8080, 8085, Z-80, 6800, 6802, and 8086 devices enable the AMDS user to debug both hardware and software in the actual user environment. The optional 48-bit logic analyzer allows analysis of microprocessor-based systems using as many as 24 address lines and 16 data lines. Three relational breakpoints may be set up to detect such conditions as address match, address greater or less than a selected value, data match, instruction fetch, input/output request, or combinations of these conditions. The user can store up to 256 bus transactions, which can be qualified to store only events of interest, such as all outputs to a particular I/O port. Counters are included to allow multiple passes through a loop, windowing of the trace to provide information before and after the interrupt event, and time or cycle counting from event to event.

The software

Futuredata system software includes system monitors, editors, debuggers, relocating macro-assembler, linking editors, compilers, and utilities. These programs run on the AMDS exactly as on a stand-alone system directly connected to a disk and printer. The only difference in the network environment is that disk and printer requests are buffered through the high-speed link to the NCP and that I/O operations to the disk may take somewhat more time since simultaneous accessing of the disk unit may be occurring with more than one AMDS.



2. Advanced development station. Besides a 12-inch display and keyboard, the terminal also features 16 to 64 kilobytes of static or dynamic RAM, a choice of six target machines (so far), and optional attachments such as in-circuit emulator and 48-bit logic analyzer.



3. Network interface logic. The card containing the electronics shown enables any AMDS it is installed in to perform the network control function. As the network control processor, the station then uses the appropriate software to handle all disk requests and printing tasks.

The shared disk facility consists of two or more double-density, double-sided flexible disk drives and an integral controller. Each controller can address up to four drives, and the NCP can address up to four controllers, for a total of 16 megabytes of mass storage. The data rate of the double-density disk drives is 80 kilobytes per second. The high-speed positioning mechanism allows track-to-track stepping of 3 milliseconds and an average access of 110 ms. These specifications describe a high-performance, low-cost disk facility built around 2 to 16 megabytes of random-access mass storage.

The network control processor

The NCP, although the heart of the system, uses exactly the same hardware as an AMDS. Thus, the network is self-sparing, since any AMDS can assume the network control function. The NCP can form a stand-alone system when used only with floppy disks and printer resources. Otherwise, it has high-speed serial links to every satellite AMDS. When controlling a network, the NCP executes a network control program that allocates the disk and printer resources on a shared basis (Fig. 3). To provide all of the facilities of a full development system, the NCP must respond to a series of high-speed disk commands. This is done using an I/O control block transmitted from the AMDS to the NCP. The parameter control block specifies the type of disk request and disk file name as the primary pieces of information. The types of request are given in Table 2.

In a sharable environment, there will be cases when several of the AMDS stations make disk requests at the same time. Since servicing each disk request on a first-come, first-served basis could cause frequent disk seeks, adding unnecessary overhead to the system, the following scheme was devised. Users are granted disk accesses on a round-robin basis. The user granted the last disk access will retain control of the disk until no new request is received from him within the 24-ms delay time between sequential sectors or a track seek is required to access the next sector or 50 sectors (one track) have been transferred.

As a result of the algorithm implementing this scheme (see "How the disk-sharing algorithm was determined"), no user can hold the disk for more than 1.23 seconds. Thus, a network with eight users has a worst-case response time of less than 10 seconds. In addition, the printing tasks can be easily interleaved into the disk queue. The outputs from the assemblers and compilers are routed to disk files, for the network algorithm to read into memory and transfer to the printer as part of the round-robin task schedule. (This is the familiar "spooling" technique used in many systems.)

Other functions carried out by the NCP are: to enable AMDS users to send messages for operator intervention; to provide a local operator with network status information; to allow for the initialization of diskettes; to control the creation of system files; and to execute central diagnostic procedures.

The system recognizes two file types: public and private. Public files are read-only and cannot be deleted. They include the assemblers, compilers, editor, and utilities, and may be read by more than one station simultaneously. Private files are nonsharable read/write files and are accessible by only one station at a time. The NCP handles the bookkeeping that is necessary to enforce these rules.

TABLE 2: DISK REQUESTS

CREATE a new file with a specified name and length
OPEN the selected file for input/output
CLOSE the selected file
DELETE the selected file and return the space to the free list
RENAME the selected file
CHANGE ATTRIBUTES of the selected file (Files can be public, write-protected, private, source, object or system.)
READ data from the selected file
WRITE data to the selected file
FREE SPACE not used by the selected file and return it to the free list
QUEUE FILE for printing on the system printer

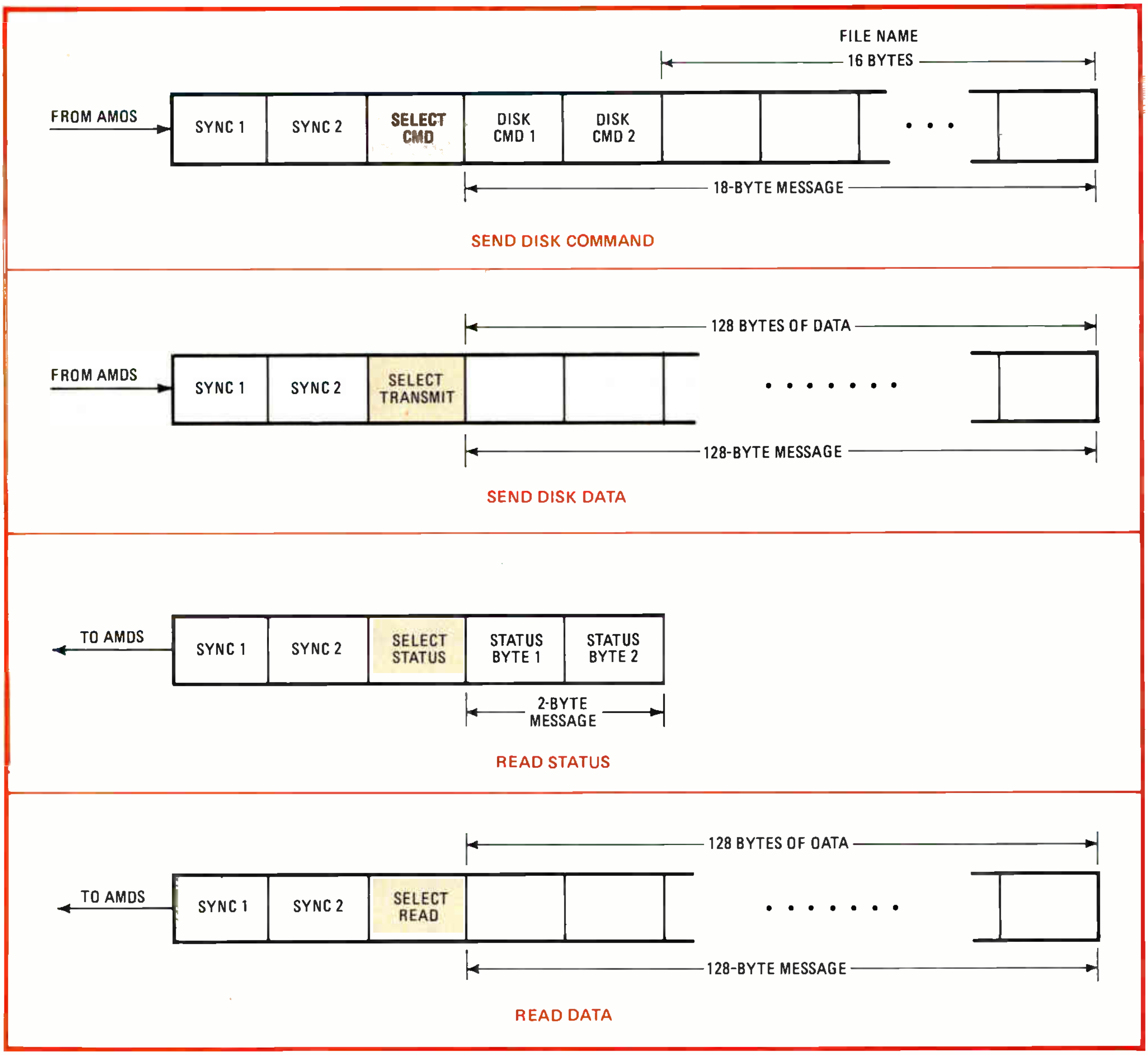
The high-speed data link uses universal synchronous/asynchronous transmitter/receiver chips. These allow bisynchronous communications at speeds up to 1 megabit/second over a shielded, twisted-pair cable. Using standard differential line-driving techniques (RS-422), it is possible to send serial data up to 400 feet at 500 kilobits/second with no intersymbol interference and a minimum pulse width greater than four times the rise time (this is a conservative design rule that results in no transmission problems). The biphase modulation allows the data to be self-clocking.

A useful feature of the Usart chips is their ability to hold the last transmitted character indefinitely, for it greatly simplies the design of network control function if requests can be held until the NCP can get to them. Thus the AMDS station's request for service is a single-byte message to the NCP. When received at the NCP, this is held in the receive buffer until it can be serviced. Also, a received-data-available flag is set that the NCP can test. This is crucial to the operation of the NCP since it is clearly impossible for a microprocessor to service eight 500-kilobit lines simultaneously. By using 1-byte service requests, each AMDS is taken care of in turn without loss of information.

Possible requests

There are various types of service requests that an AMDS can make of the NCP. Many are control functions that affect the directory on the disk. Examples are CREATE, DELETE, RENAME, and OPEN. These functions go to completion since they are rapidly done with minimum disk activity and because directory updates cannot be made by more than one user at a time. The NCP also has to respond to requests to read and write to open files. In this case the sharing algorithm is invoked.

Typically, in requesting for service, an AMDS gets into the round-robin queue by sending a 1-byte service request to the NCP. This byte is encoded to flag the type of request (READ, WRITE, READ DIRECTORY, etc.) and is held in the NCP Usart buffer until the NCP can test that channel. When the NCP does respond, it sends status information to the AMDS, which can then continue the



4. Protocol. Communications are initiated by a command request from a development station. All messages consist of two sync bytes—a header byte indicating the type of information to follow, plus the data. Transmissions of predefined lengths greatly reduce the network burden.

communication process with the disk.

The communications protocol has been greatly simplified because the types of messages sent are minimal, allowing both ends of the communications link to be precisely defined. Typically, the messages to be sent back and forth over the communications link are:

- Commands sent by an AMDS to the NCP, invoking the disk functions previously described and sent as a 18-byte-long parameter control block describing type of request and file name.
- Write data sent from an AMDS to a disk file in 128-byte-long blocks.
- Data read from the disk file to the AMDS in 128-byte blocks.
- Status information sent from the NCP to the AMDS in 2-byte blocks indicating both hardware status and data transfer status such as error conditions, end-of-file conditions, file protection status and disk status.

All communications are initiated by a command request from an AMDS (Fig. 4). Such a request consists of the two sync bytes, a header byte indicating that a command follows, and the 18 command bytes. Both ends of the link know which end will transmit and which will receive. Transmissions then follow a predetermined pattern until an exception condition (error, EOF, etc.) occurs, at which time AMDS can send a command requesting a status read, to close the transaction.

This is a very effective protocol because the limited nature of the task keeps overhead to a minimum. The ability to predefine the lengths of all types of transmissions greatly reduces the network burden.

The high speed of the communications link allows most requests from the AMDS to be handled quickly. This means that the disk queue will rarely have many tasks to act upon. In most cases, the user will be using data in his own memory and will have no active requests. □

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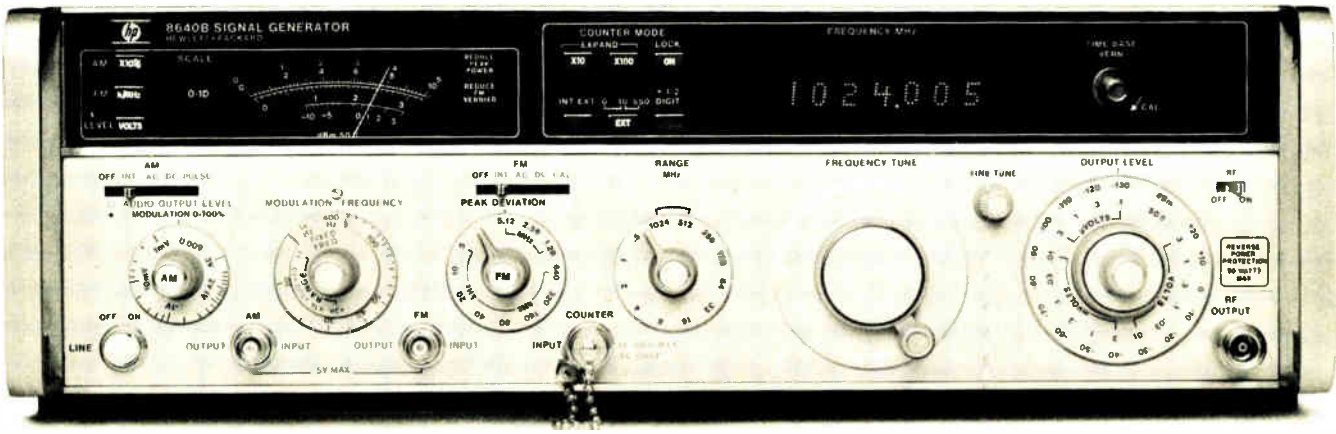

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How bit-slice families compare: Part 2, sizing up the microcontrollers

by W. Thomas Adams and Scott M. Smith,*
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☐ When they need speed in a microprocessor design, most engineers think first of a bit-slice approach. But comparative data on the various bit-slice chip families has been hard to come by.

This two-part article should help designers pick their way among the maze of options available. Part 1, which appeared in the last issue of *Electronics*, focused on the processor elements of six bit-slice families. Part 2 will cover the equally necessary microcontrollers, as well as assorted special-purpose chips and programming aids.

The microcontroller sequences a bit-slice system's instructions. Models available today include Texas Instruments Inc.'s SN74S482, Advanced Micro Devices Inc.'s Am2909, Am2910, and Am2911, Motorola Inc.'s very fast MC10801, Monolithic Memories Inc.'s 67110, Intel Corp.'s 3001, Signetics Corp.'s 8X20, and Fairchild Camera and Instrument Corp.'s 9408.

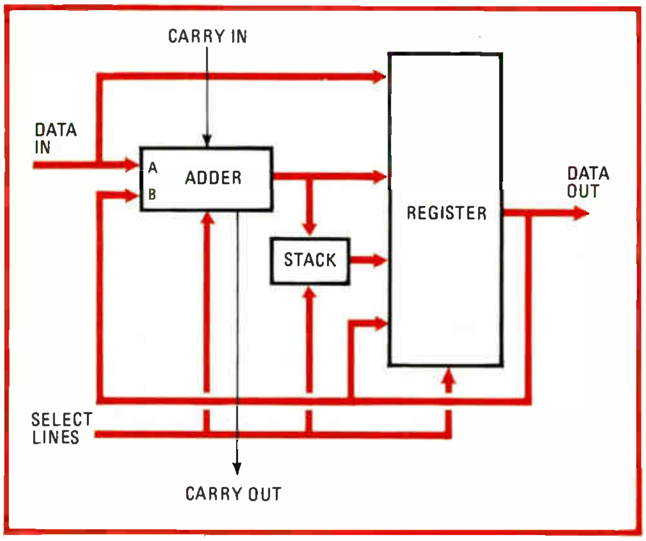
Alternative philosophies

Microcontroller designs may follow one or other of two distinct philosophies. The first is one in which several parts are cascaded to address a reasonably sized control memory, the part being referred to as a microprogram control element. The second is actually not a bit-slice approach, but one in which a single package, called the microprogram control unit, houses all the circuitry required to address anywhere from 512 to 4,096 control memory words, depending on the device. In the latter approach, the address space may be increased by paging techniques, but not by cascading devices. (A paged memory is one that is divided into blocks, which in this case are equal to the length of microcontroller's address space. The current working block or page is selected by a register set under program control, but not by any of the internal next-address modes of the microcontroller.) A table summarizing the characteristics of the microcontrollers will appear in the next issue.

A simple but extremely flexible microprogram control element is Texas Instruments' SN74S482 (Fig. 1). Each of the 74S482's major components has separate control lines, which the designer may encode to select the next microinstruction. The provision of a full adder rather than a simple incrementer allows relative addressing, a feature unavailable in any other microcontroller. Unlike the other microcontrollers, however, the 74S482 lacks three-state outputs on its memory address port. Housed in the 300-mil, 20-pin dual in-line package, the 74S482 occupies relatively little circuit board area.

As indicated in Fig. 2, the Advanced Micro Devices' Am2909 and Am2911 are identical except for the separate register input and the OR inputs that the 2909 offers. Eliminating those features on the 2911 allows it to be packaged in a 300-mil, 20-pin DIP instead of the 2909's 600-mil, 28-pin DIP. Both microprogram control elements, like TI's 74S482, have no inputs for instructions, but rather have a series of control lines for the various internal functions that the designer must encode for the next instruction function.

AMD offers a microprogramming handbook that provides considerable insight into the use of the 2909 and 2911 and some other related devices. However, to be



1. Simple microcontroller. Although Texas Instruments' SN74S482 microcontroller element appears simple, it is very flexible. While other sequencers have incrementers to select the next microinstruction, the 74S482 has a full adder, which permits relative addressing.

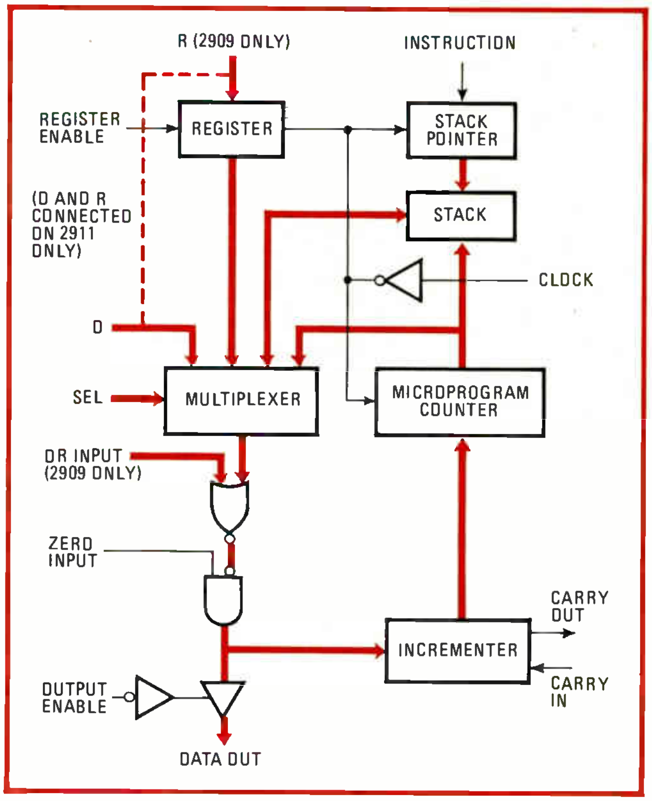
*Both authors are now at IBM Corp., Office Products Division, Austin, Texas described later is AMD's new microprogram control unit, the Am2910, which makes the 2909 and 2911 practically obsolete for all applications except those requiring control memories in excess of 4,096 words.

Fastest

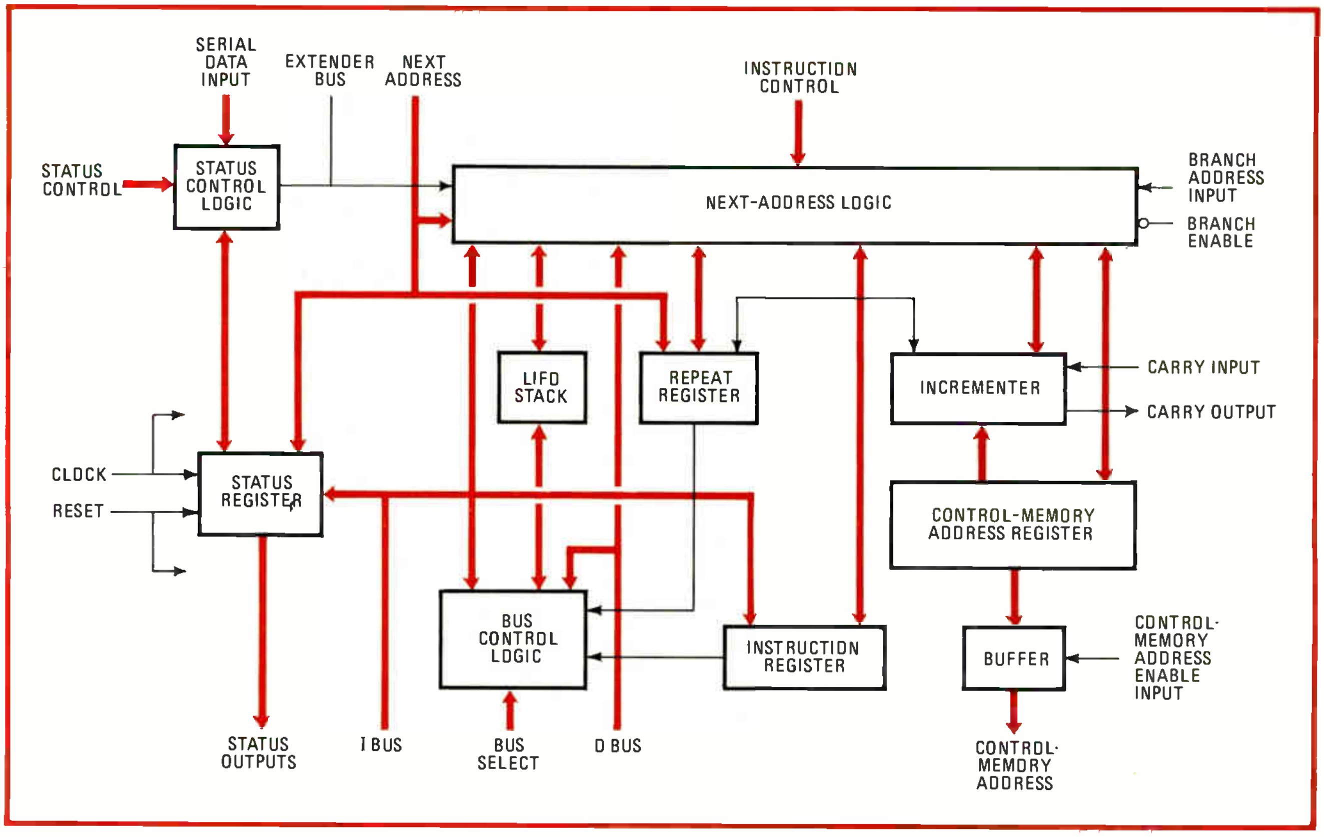
Motorola's MC10801 (Fig. 3) is unique among the microcontrollers for a number of reasons. It is the only emitter-coupled-logic sequencer available, so that in terms of clock frequency alone it is the fastest device available. But the 10801 also has architectural features that further increase its throughput potential. A repeat register allows single instructions or subroutines to be executed a specified number of times without the usual sequence of decrement loop count, test for zero, and branch or increment on test result. Microinstructions are saved, thus increasing throughput, and no register in the processor array is needed for the loop count. The 10801 provides internal storage for status information, which may be used to determine the outcome of conditional instructions. The status bits are also available through an output port for use elsewhere in a system.

An internal instruction register allows the operational code of the next macroinstruction to be loaded during execution of the current one. This register is loaded from one of the two system I/O buses connected to the 10801; these I/O buses may also be used to externally expand the 10801's last-in, first-out subroutine-linkage stack. As can be inferred, the 10801 is a complex, powerful device.

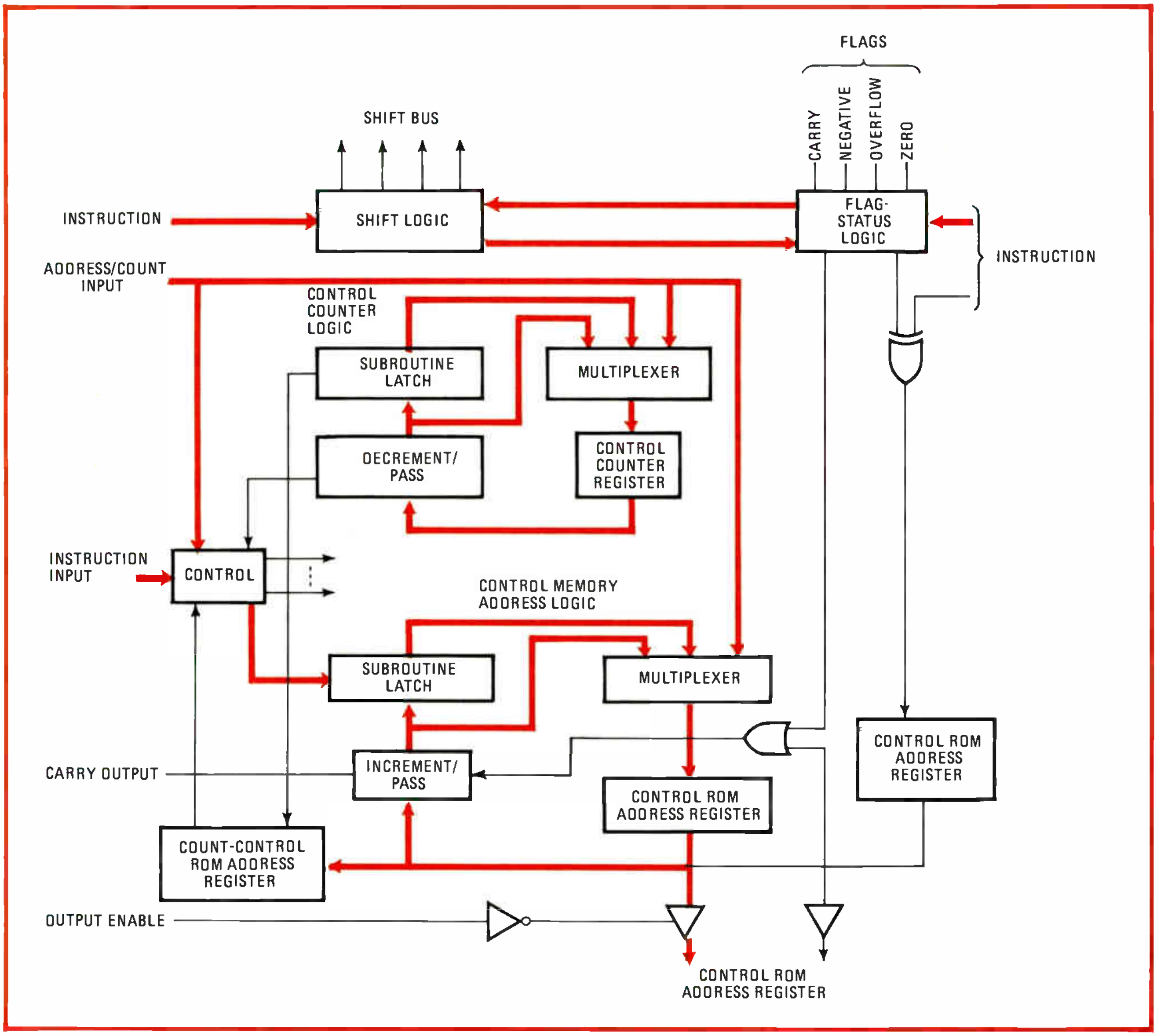
The many options available to the 10801's user are clearly explained in Motorola's excellent data sheet on



2. Two of a kind. The only difference between Advanced Micro Devices' Am2909 and Am2911 microcontroller elements is the elimination of separate register and OR inputs on the latter. Both have control-line inputs in lieu of an instruction input.



3. Fastest sequencer. Aside from the fact that it is the only all-emitter-coupled-logic microcontroller, Motorola's MC10801 has features that increase its speed potential. One example is the repeat register, which lets subroutines be reiterated without the normal looping sequence.



4. Not a slice. Monolithic Memories' 67110 is not cascadable—it is a microcontroller unit with an addressing capability of 512 words. While it is based on a program counter, branching is to even-odd pairs in memory and requires care when microcode is being modified.

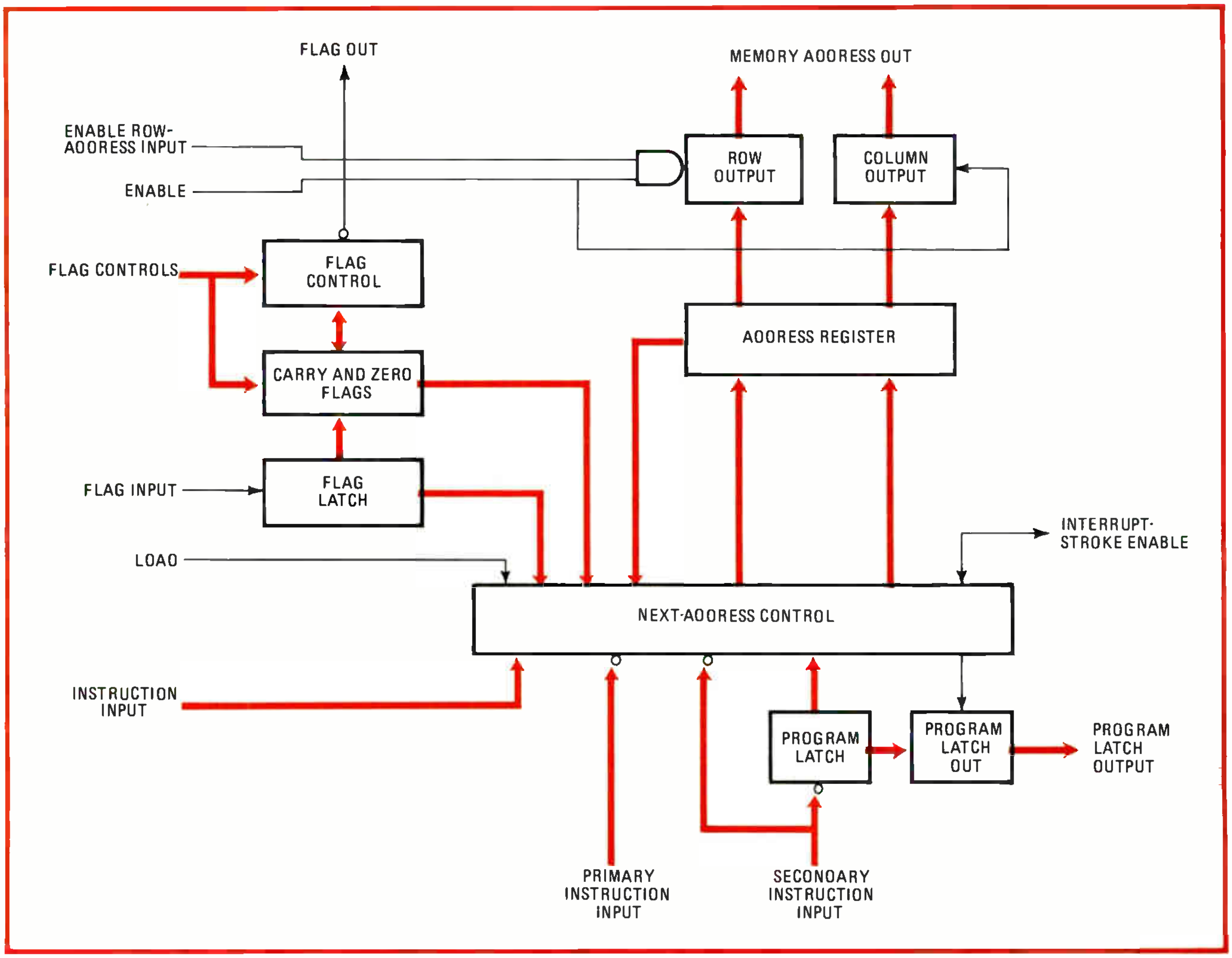
the device. Again, as with the 10800, direct mixing of the 10801 and transistor-transistor-logic bit-slice parts is not recommended. The 10801, being a good high-performance part, is recommended for use in high-speed minicomputer and signal-processor applications, though a few controller applications may also require it.

Shown in Fig. 4 is Monolithic Memories' 67110, a microprogram control unit with an addressing capability of 512 words. Its basic addressing scheme is based on a program counter; however, the least significant bit is handled such that a conditional branch to either location of the next even-odd address pair may be executed without the use of the microinstruction next-address field, thus often freeing that field for other uses. When this addressing scheme is employed, note that care must be taken in writing and modifying microcode to ensure that all even-odd branch pairs are in fact stored in even-odd address pairs.

The 67110 offers an internal looping capability not found in most microcontrollers, which allows it to execute a program loop a specified number of times without the usual sequence of decrementing the counter, checking for zero, and branching or incrementing on test result. The single-level subroutine capability in the 67110 is rather limited, however. Internal storage for various processor-element array flags is provided, as is the ability to condition the next-address selection on the stored or current value of any of those flags. Although the number of control lines seems high, several are required to select the flag bit used in carrying out conditional operations.

Probably more than any other factor, the choice of whether or not to use the 67110 depends upon whether or not the designer likes the pairwise branching scheme.

Another microprogram control unit with a 512-word address capability is the Intel 3001 (Fig. 5). Its addressing scheme, however, is unique. The 512-word address space is defined as a 32-row-by-16-column matrix; a set



5. Unique addressing. Intel's 3001 also has a 512-word addressing capability. Only seven instruction control lines are needed; a set of branch instructions allows jumps from a given address to a fixed subset of the address space that is a function of that address.

of branch instructions allows jumps from any address to a fixed subset of the address space that is a function of the given address.

With this technique, only seven instruction-control lines are required. No branch address input is needed other than that needed to obtain macroinstruction starting addresses. While this approach can reduce the width of the control memory, it can also complicate the debugging and modification of microcode.

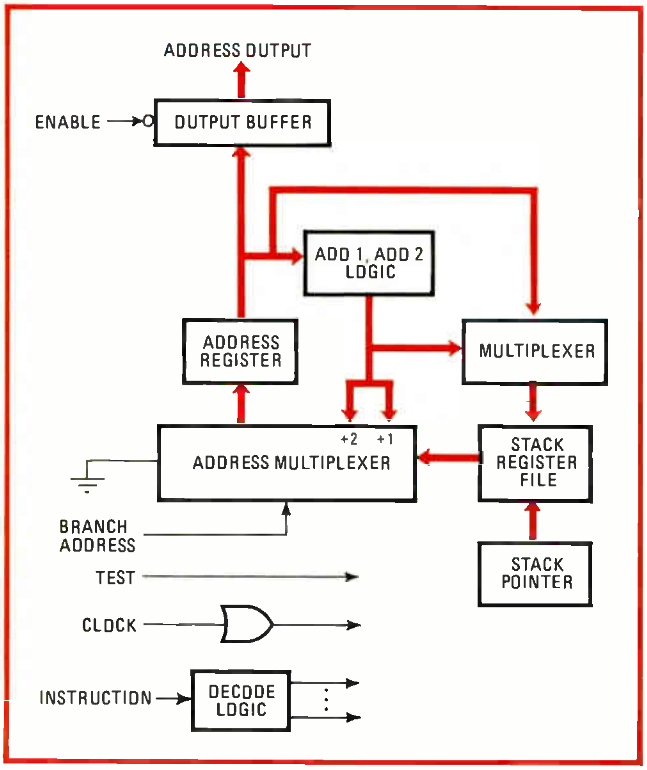
Undoubtedly, the greatest weakness of the 3001 is its lack of an internal subroutine capability, though the device can be wired externally to provide for single-level subroutines. Like the 67110, the 3001 provides storage for several flags associated with the processor-element array that can be used in conditional branching.

Simple but capable

The Signetics 8X02 (Fig. 6) is a microprogram control unit with a 1,024-word address space. Though it appears simple, it is a capable device. A program counter is used for the basic addressing mode. Like most microcontrollers that use a program counter, the 8X02 can branch to an address specified on its branch-address input port. However, it provides several instructions that minimize use of the branch-address input, thus freeing that microinstruction field for other purposes much of the time.

For instance, a skip command allows incrementing the program counter by two rather than one on a true-test input. Also, two other instructions allow program loops to be executed, again without use of the branch-address input—the address of the loop entry point is merely placed on the last-in, first-out stack normally provided for subroutine linkage. (Note that this looping capability is not the same as that referred to in the table, since the number of times the loop is executed must be counted externally in the 8X02.) Housed in a 28-pin dual in-line package, the 8X02 offers more performance per square inch of circuit board area than most other microcontroller devices. It is an excellent choice for all but the highest-performance applications.

Fairchild's 9408 is a 10-bit-wide microprogram control unit that is based on a program counter. Its block diagram (Fig. 7) reveals several useful features. There are four flip-flops for storing input test flags to be used in conditional branches. (The only criticism of this arrangement is that, though there is a separate strobe for the register group, there is no provision for loading one flag without disturbing the other three.) In addition to



6. Capable. Signetics' 8X02 microcontroller unit has a 1,024-word address space. Like others that use a program counter, the 8X02 has a branch-address input; however, several commands, like skip and looping commands, save on branch microinstructions.

the basic branch address input, the 9408 control unit has an alternative source for the three least significant bits of the branch address. This alternative source is used in an eight-way branch instruction that can, for example, decode macroinstruction op codes in just a single microinstruction.

The 9408's control-memory address output may be driven either by the program counter for nonpipelined operation or by the program counter's input multiplexer for pipelined operation. Implemented with Fairchild's version of I^2L, Isoplanar integrated injection logic, the 9408 is a slower device than the TTL microcontrollers. Also, although its power dissipation is relatively low compared to the TTL devices, it lacks the user-programmable speed/power dissipation feature of TI's I^2L processor element, the SBP0400.

Three in one

As can be seen by comparing it with the Am2911 (Fig. 2), AMD's Am2910 (Fig. 8) essentially consists of three cascaded 2911s and an instruction-decoding programmed logic array on one chip. The auxiliary register in the 2910 is also a counter with a zero detector, and the last-in, first-out stack is five words deep. In addition to decoding instructions, the PLA provides three output signals that can be used to enable any of three sources to the 2910's D inputs.

The register/counter in the 2910 may be used to store a branch address that is to be used later in a double-address jump or a subroutine call; as a counter, it is used to count down the number of times a program loop has been executed and to cause a loop exit when the count equals zero. The beginning address of a loop may be pushed onto the LIFO stack as the loop is entered, thus allowing the top-of-loop address to come from the stack rather than from the direct data inputs.

The 2910 has a unique three-way branch instruction that is useful at the end of loops. If the input test condition is true, incrementing the program counter causes an exit from the loop. But if the test condition is false, the loop counter is decremented and the program branches to the top of the loop until the counter is zero, and then branches once more to the address specified on the direct input lines.

The 4,096-word address space in the 2910 is more than enough for the vast majority of applications. The part offers most of the next-address selection modes provided by the other devices and is housed in a single 40-pin DIP.

Two other sequencer-type devices—Fairchild's 9406 program stack and AMD's Am2930 program control unit—might be used as microprogram controllers, but are marketed primarily as macroinstruction sequencers. Both parts are bit-slice designs, and perhaps their single most significant difference from the microcontrollers is the depth of their LIFO stacks—16 or 17 levels compared to the 4 or 5 levels of typical microcontrollers. The 2930 is the more capable of the two devices, since it has in addition to an incrementer a full adder that permits a number of relative-addressing options.

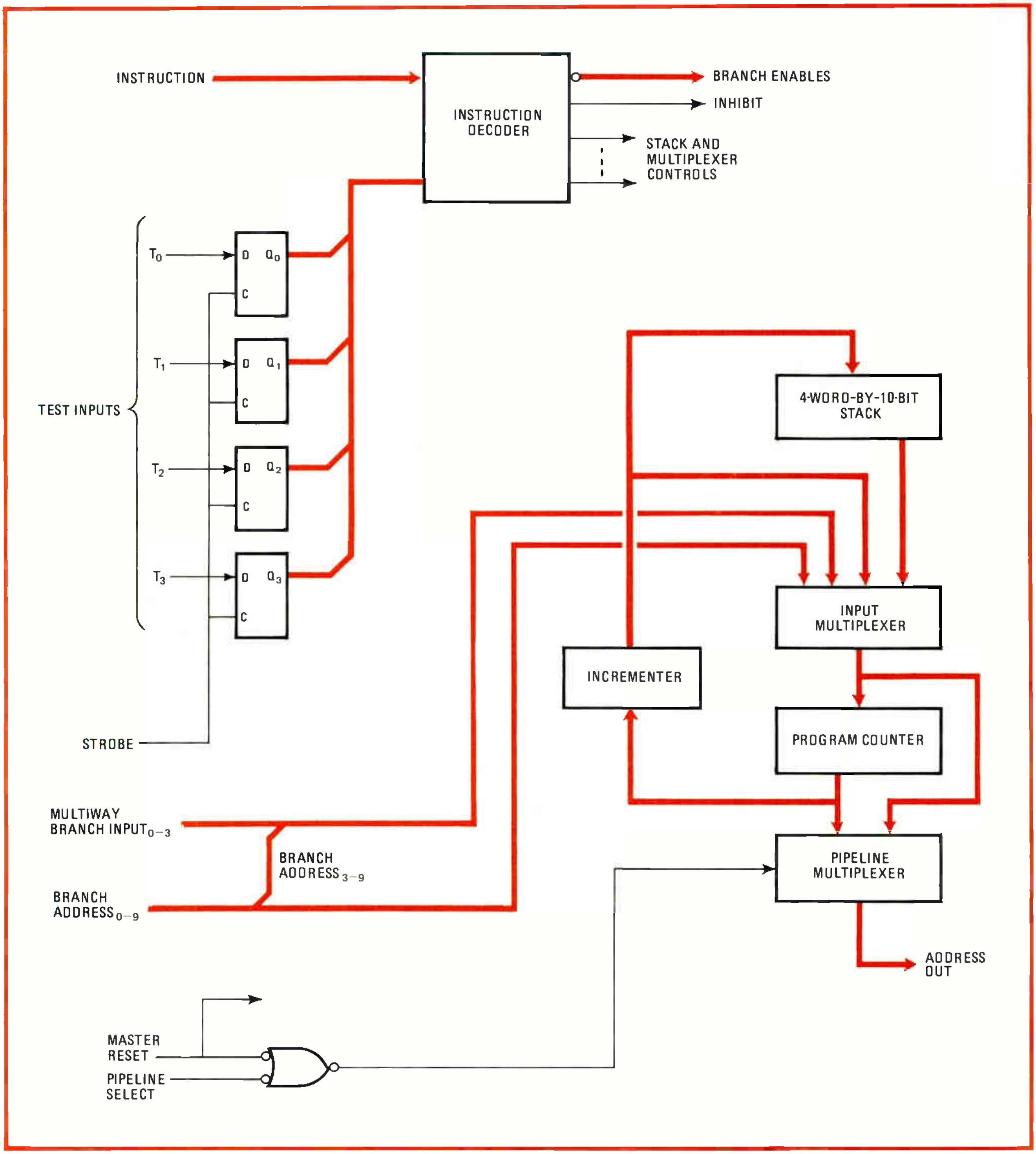
Special-purpose devices

Several manufacturers provide as part of their bit-slice families special-purpose devices that perform some unique function. Space does not allow us to cover all of the special-function devices available, but here are a couple of the more significant examples.

The addressing and controlling of system memory is one function for which two special purpose-devices have been built. They are Fairchild's 9407 data-access register and Motorola's 10803 memory interface unit, both of which may be used to remove the burden of interfacing with system memory from the processor-element array, thus increasing system throughput. Intel and AMD each offer circuits for vectored priority-interrupt encoding, which aids the microcontroller in interrupt handling. Motorola's MC10802 timing function device supplies 10800-based designs with a number of useful timing features. Among other functions, the 10802 can be programmed to generate from two to four clock phases, any of which may be doubled in length to compensate for a slow data path without slowing down the other phases.

Design support

One of the more important aspects of designing with bit-slice microprocessors—particularly to new users—is the design support provided by the manufacturer. Such support consists of literature (including data sheets and application notes), direct assistance from the manufacturers' applications engineers, software (primarily microassemblers), and hardware, including kits and development systems. The quality and quantity of literature varies gretly among manufacturers. One reason for



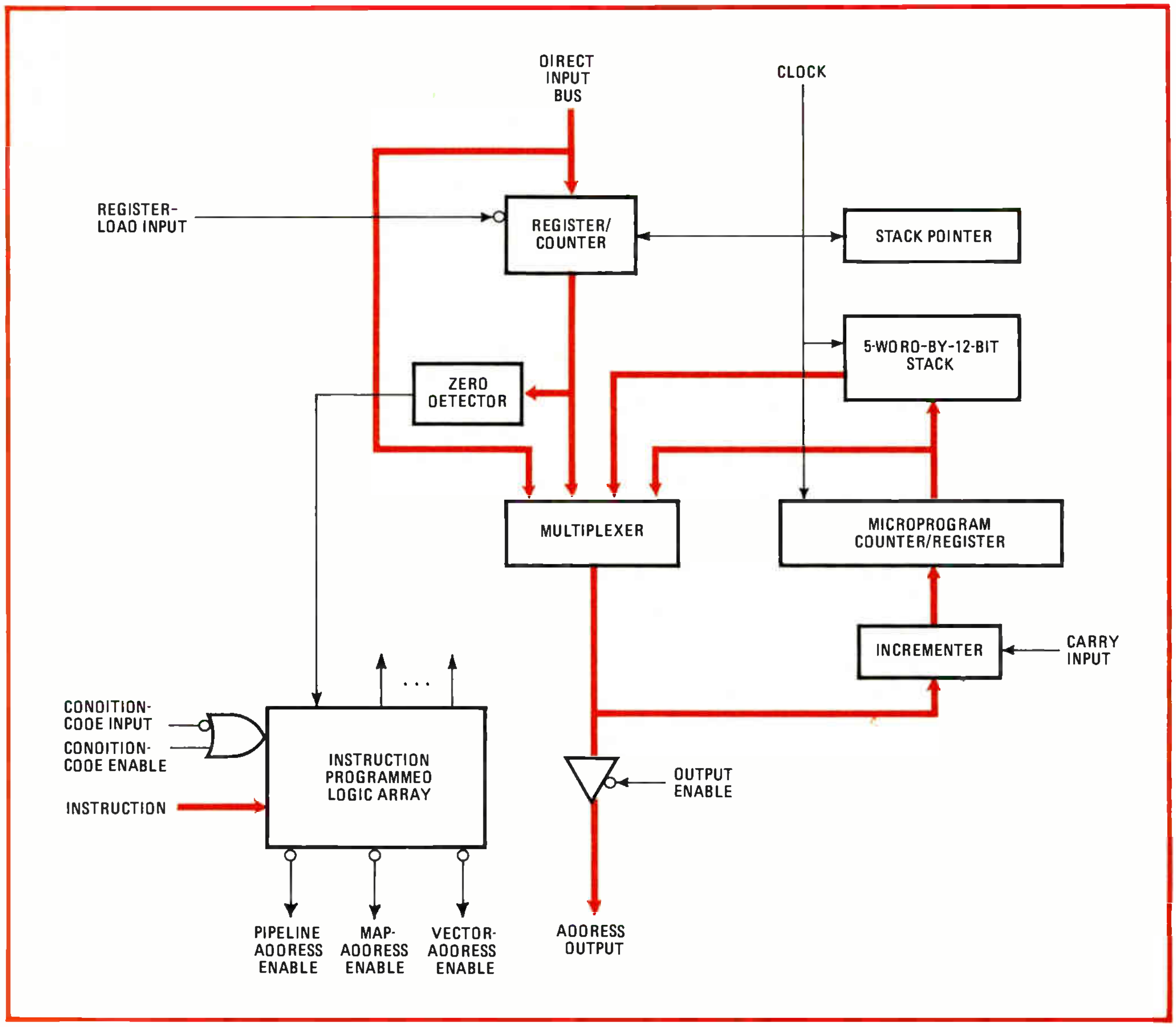
7. I²L controller. Fairchild's 9408 microcontroller has a 10-bit-wide address capability and features that include an 8-way branch instruction and flip-flops for storing branch-test flags. Though slower than other controllers, the integrated-injection-logic device requires less power.

the popularity of AMD's 2900 family has been the excellent literature provided with it. The application notes from AMD have had the most detailed design information. Intel and Motorola also supply excellent applications literature.

The direct assistance provided by the various manufacturers is much harder to evaluate since the quality of advice received is at least as much, if not more, a function of the individual applications engineer than it is a function of the manufacturer he represents.

Software support for the bit-slice microprocessors consists of operating systems for hardware-development systems and cross-assemblers. Intel, AMD, and Raytheon have offered cross-assemblers for quite a long time. Those programs let the user define an assembler to fit his own application.

Intel provides such a program in Fortran, and AMD and Raytheon, as well as Intel, are supported by



8. 4-K address space. Advanced Micro Devices' Am2910 essentially comprises three Am2911s and an instruction-decoding programmed logic array. Control memories larger than the 2910's 4,096-bit address space will require cascadable sequencers like the 2909 or 2911.

programs over various commercial time-sharing networks.

The assembler can be a most cost-effective tool in the development of bit-slice microprocessor designs since the programmer can write, debug, and document his microcode in a much clearer form in the mnemonics of assembly language than in 1s and 0s of machine language. As an alternative, he may define his own assembler on a data-processing system.

Hardware support

Fairchild and AMD offer hardware support in the form of kits with printed-circuit boards, on which the user can build a demonstration bit-slice microprocessor system. The kits, which sell for a few hundred dollars, aid those with little microprogramming or bit-slice experience.

Intel, AMD, and Motorola, among others, offer some form of hardware development system. The systems basically allow the user to assemble microcode for a bit-slice design in a resident MOS microprocessor and to load this code into random-access memory (called a read-only memory simulator in this application), which is connected to the system under development in place of its own microcode memory. The hardware development system allows modification of the microcode in RAM and tracing of the execution of microcode and also supplies traps for specified code sequences under microaddress or external hardware control, among other functions. AMD's System 29 also provides a framework for housing the hardware under development. It should be noted, however, that the microcode execution using these development systems is in general at a speed below normal. Moreover, these systems are not inexpensive, so the purchaser should have enough development work to justify their cost.

If a hardware development system is not available, the designer must provide his own scheme for easily altering the contents of the microcode memory during the debug phase. A general-purpose logic analyzer can, of course, be used to trace microcode execution. □

Tuning-meter muting improves receiver's squelch response

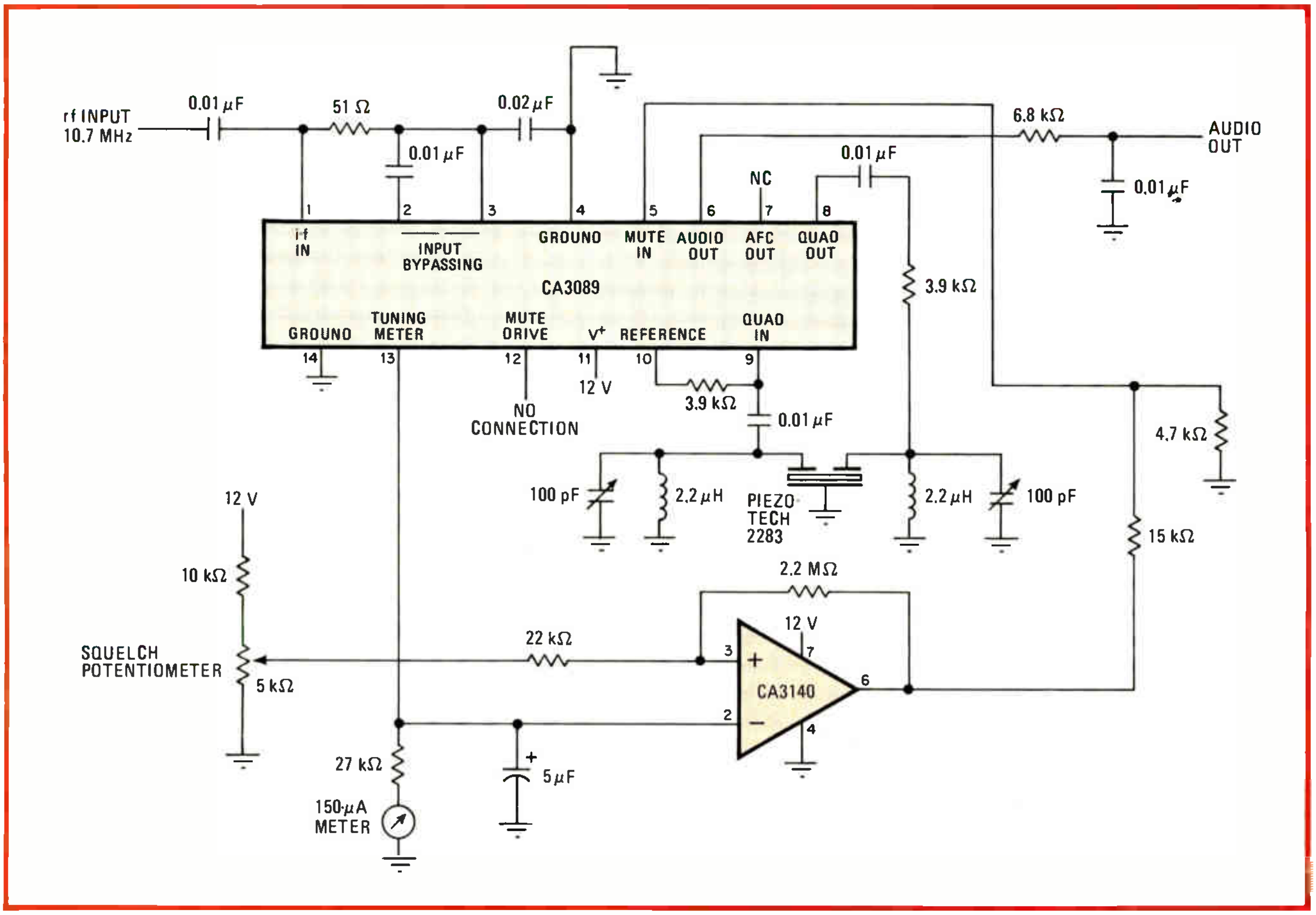
by Albert Helfrick
Aircraft Radio and Control Division, Cessna Aircraft Co., Boonton, N. J.

Although the CA3089 FM/IF system offers the advantages of one-chip simplicity, good limiting capability, high gain, and excellent linearity when used in wideband fm-broadcast receivers,[1] its audio-channel muting performance, and thus its squelch response, suffer in narrow-band applications, especially at low signal levels. Utilizing the output voltage from the device's tuning-meter port to drive the audio-muting control circuit through an operational amplifier greatly improves squelching, particularly for signals whose amplitudes are barely detectable.

The circuit configuration of a typical limiter-discriminator designed for a modulation deviation of ±5 kilohertz is shown in the figure. As in many discriminators, a crystal serves for the high-Q tuned circuit and so makes possible the high audio recovery required in a narrow-band configuration.

The internal muting action of the CA3089, though sufficient for wideband service, lacks the speed and precision necessary for narrowband operation, because the system's effectiveness is a function of the characteristics of the detector's frequency-determining elements connected to pins 8, 9, and 10, as well as the gain distribution of the entire receiver. Narrowband receivers usually make full use of the system's available sensitivity by having as much gain as possible before the detector so that limiting occurs on noise, and the small-bandwidth characteristics of the CA3089 circuit are similar. At low signal levels, this limiting causes the squelch circuit to be almost useless. In some of the recommended circuits for frequency discriminators, the squelch circuit will not operate at all.

Driving the mute-control amplifier from the tuning-meter port (pin 13) instead ensures that the tuned circuit and the chip's gain distribution have no effect on squelch



Silence. Circuit derives voltage for squelch-control amplifier from CA3089's tuning-meter port, whose output is linear over 5 to 10,000 μV. Op amp provides gain for surefire operation. Configuration provides positive squelch response, even at low signal levels, by bypassing the combined nonlinear response of tuned circuit and mute-drive circuit internal to the CA3089.

operation. The meter-output voltage, taken from the unit's three intermediate-frequency amplifiers and their level detectors, has a constant characteristic—that is, it is independent of the tuned circuit used. In fact, the response is virtually linear for input signals ranging from 5 to 10,000 microvolts.

The high input impedance of the low-noise CA3140 op-amp comparator will not load down pin 13, and its gain enables the squelch circuit to operate in a surefire manner. The CA3140 is used as a comparator with a variable threshold set by the squelch potentiometer, as shown. A voltage divider at its output ensures that no more than about 5 volts can be applied to port 5—anything higher would cause latchup in the CA3089, which might cause excessive power dissipation.

The CA3140 can operate with a common-mode voltage equal to that of the negative supply, and it may therefore be operated from the same power source as the CA3089. □

References
1. J. Brian Dance, "One-chip for demodulator has improved response," *Electronics*, Dec. 22, 1977, p. 78.

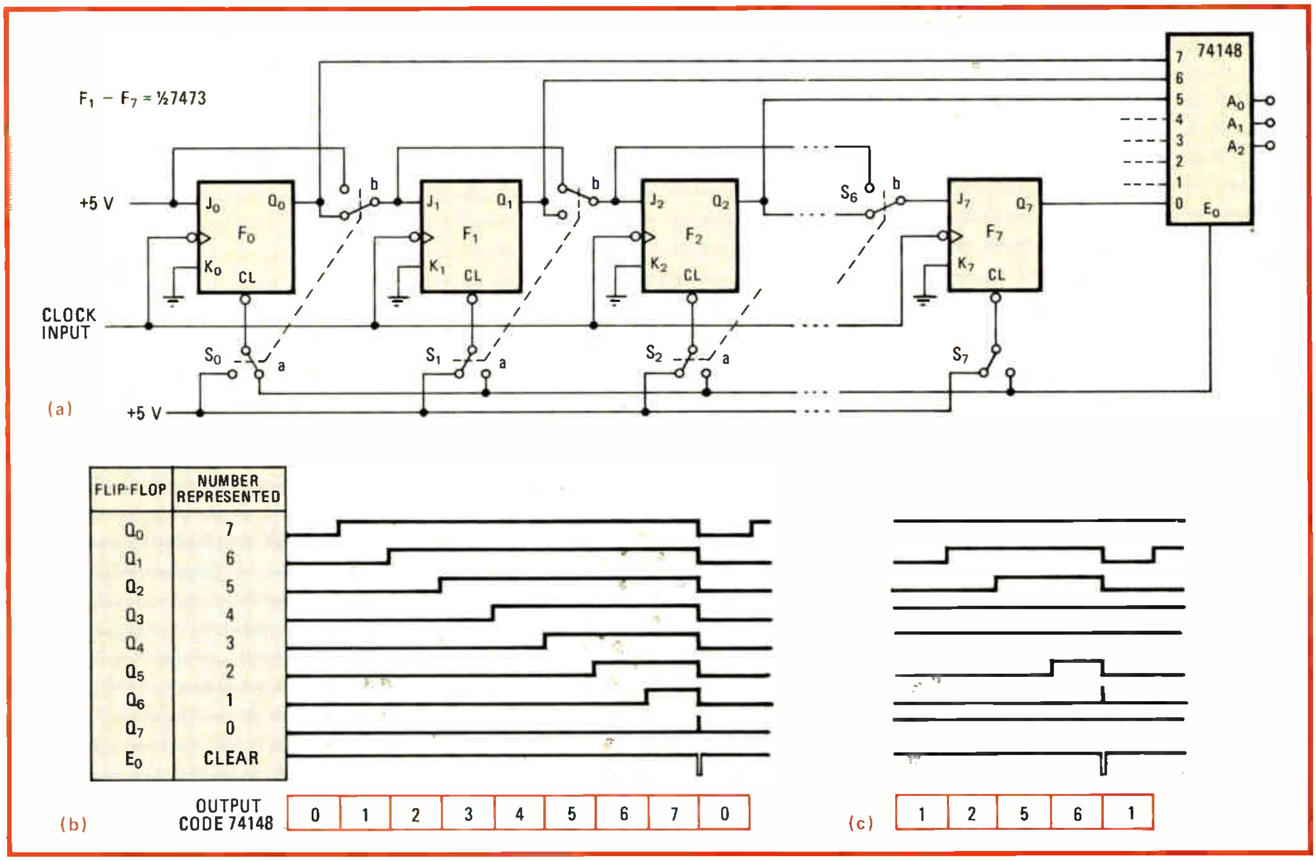
Cascaded flip-flops set periodic-sequence generator

by Carlos Correia and Cidálio Cruz
University of Coimbra, Portugal

This circuit, which generates a periodic sequence of nonconsecutive binary numbers, will serve well as an address generator in multiplexed data-communications systems. Using several J-K flip-flops whose outputs drive a priority encoder, the circuit produces a selectable, monotonically increasing output code having zero dead time (no lag) between numbers. Implementing this circuit is far simpler than modifying a standard binary-counter circuit, which is more useful in applications where the numbers to be generated are consecutive.

As shown in (a), a double-pole, double-throw switch is required for all but the last flip-flop desired, which requires a single-pole, double-throw switch. In this case, seven flip-flops are used—thus the numbers 0 through 7 can be generated.

When each flip-flop is active (Q disconnected from the J port of its succeeding 7473 flip-flop and its clear port connected to E_0 of the 74148), the sequence generator will advance in order from 0 through 7, as shown in (b). At the end of the sequence, when all inputs to the 74148 are high, E_0 moves high, clearing all flip-flops and



Chosen order. Periodic-sequence generator (a) produces selectable, monotonically increasing binary output code (b) having zero dead time. Any number can be omitted from the sequence (c) by using double-pole, double-throw switches to disconnect Q output of the flip-flop corresponding to that number from succeeding flip-flop and bringing its clear port to 5 V.

initializing the sequence at its first number.

Note that any number can be omitted from the sequence by connecting the Q output of the flip-flop that corresponds to that number to the J port of the next flip-flop and then connecting its clear port to 5 volts. For instance, the sequence 1, 2, 5, 6, seen in (c), is generated by disabling flip-flops 3, 4, and 7.

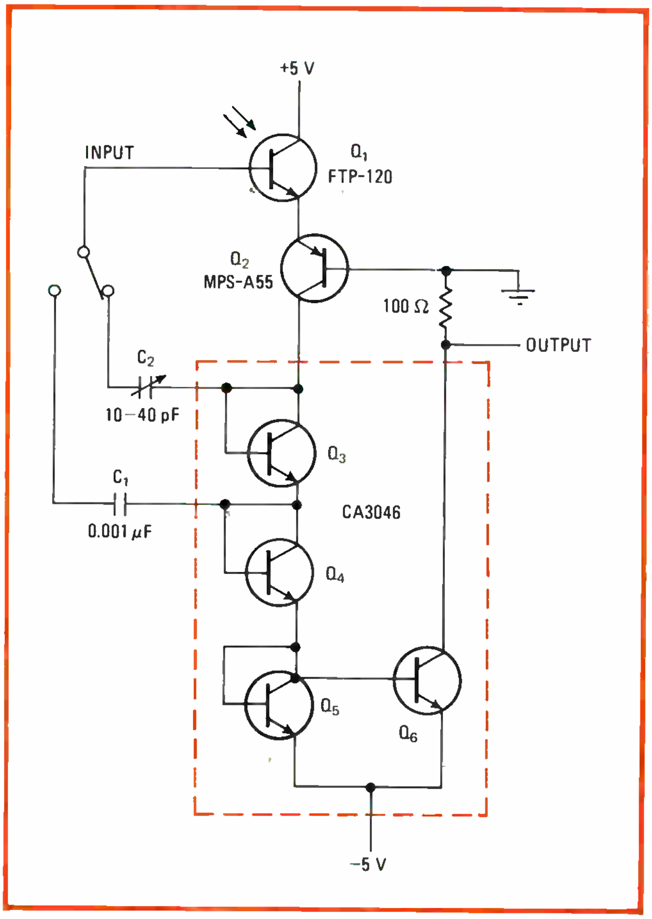
A sequence having a maximum word length of 10 can be generated if a 74147 is used in place of the 74148. However, the E_0 signal is not available in the former device, and therefore to derive that signal each input of a 10-lead NAND gate must be connected to all flip-flops, with its output connected to the switches.

The maximum clock rate is determined by the propagation delay times encountered by the signal that clears the flip-flops. For the circuit shown, the delay time is about 95 nanoseconds, which yields a maximum clock rate of 1 megahertz. If Schottky flip-flops are used, the delay is 44 ns, corresponding to a clock rate of approximately 2.2 MHz. □

Bootstrapping a phototransistor improves its pulse response

by Peter J. Kindlmann
Engineering and Applied Science Dept. Yale University, New Haven, Conn.

Although the operating speed of a phototransistor cannot be improved simply by connecting a second one in the cascode configuration [*Electronics*, March 2, p. 132, and April 27, p. 154], its response may be improved by employing a standard transistor in a bootstrap circuit in order to reduce the effective value of the phototransistor's junction capacitance. By introducing bootstrap feedback to the base of the input optodevice, the switching speed of a cascode-connected phototransistor can be increased by as much as 10 times over that of a uncompensated one.



Compensation. Junction capacitance of Q_1, which is not sufficiently reduced despite cascode connection (Q_1, Q_2), is greatly lowered by applying feedback to base. This allows a rapid discharge of Q_1's base-to-emitter capacitance during signal conditions, which acts to increase the phototransistor's high-frequency response.

Phototransistor Q_1 and Q_2, a pnp transistor, form the conventional cascode arrangement, as shown in the figure. Generally, when an input signal is detected, the photocurrent step produced begins to charge the capacitance associated with Q_2's base-emitter and base-collector junctions. The voltage across the base-emitter junction has a magnitude comparable to that across Q_2's base-emitter junction, and therefore a way must be found to compensate for the two V_{be} drops produced, in order to ultimately reduce the effective junction capacitance of the phototransistor.

In theory, the V_{be} drops may be cancelled by making use of the pn drops across two forward-biased diodes of comparable transconductance. Here, diode-connected transistors Q_3–Q_5, which are part of the CA3046 transistor array, are available for use. Using the CA3046 ensures that these transistors will be closely matched.

Feedback from Q_4's collector to Q_1's base through C_1 constitutes the normal bootstrap path, supplying an in-phase current to Q_1's base. This causes a rapid charge of the junction capacitance, and therefore the input photocurrent sees a lower value of capacitance than actually exists. Because Q_1 has a β of several hundred, its base-emitter transconductance is less than that of the lower-β devices, Q_4 and Q_5, used in the feedback path. As a result, the amount of feedback is well below unity loop gain (undercompensated condition).

By using Q_3, however, with feedback applied through C_2, an additional pn drop is gained and compensation becomes almost perfect. For a given quiescent photocurrent, C_2 should be adjusted to a value just above that which will cause oscillation in the circuit.

Fairchild's FTP-120 (Q_1) has a typical rise time and fall time of 18 microseconds when used in the typical emitter-follower configuration specified for a 100-ohm load. With C_1-path compensation, the switching time is about 5 μs. With C_2-path compensation, the switching time is about 2 to 3 μs. □

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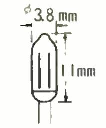

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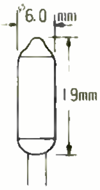

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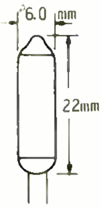

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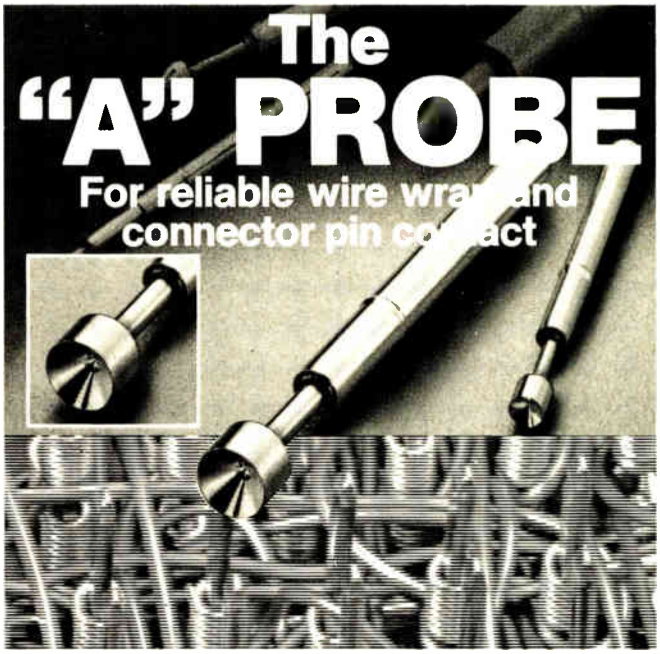

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Dual-port RAM hikes throughput in input/output controller board

On-board random-access memory, accessible from system bus, makes input/output controller subsystem look like just another memory board to the host microprocessor

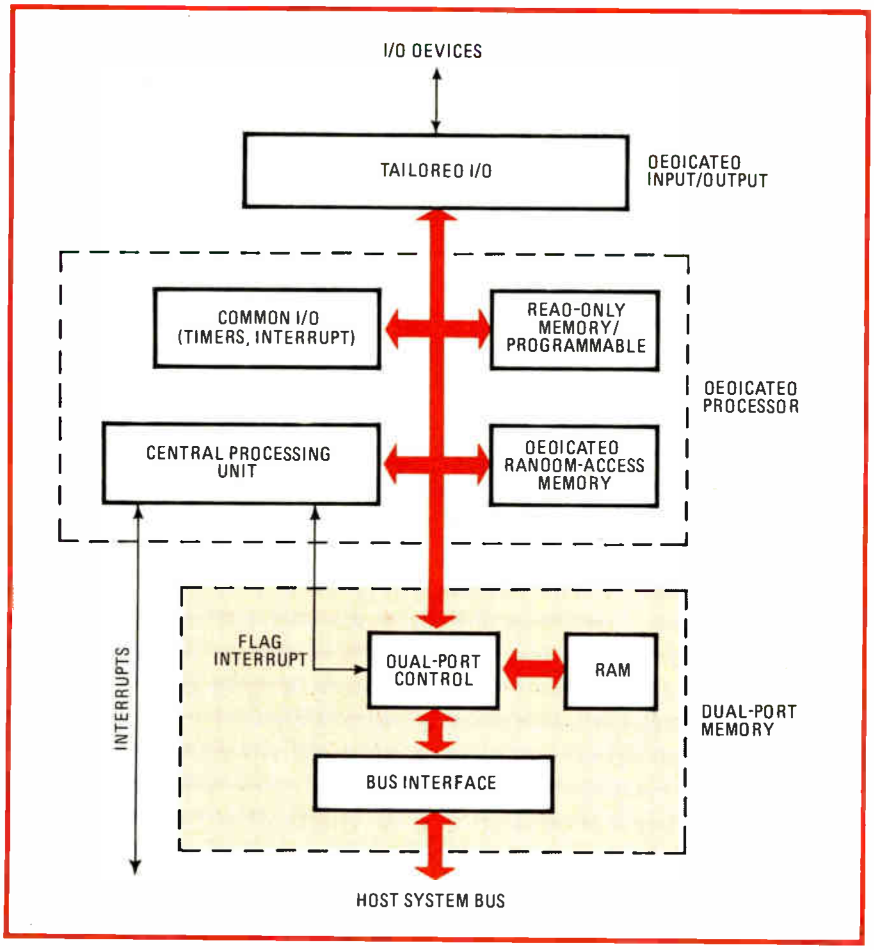
by Craig Kinnie and Michael Maerz, *Intel Corp., Santa Clara, Calif.*

☐ Input/output controllers based on microprocessors step up throughput in microcomputer systems by relieving the host processor of tedious, time-consuming control tasks—and a new design concept that increases the processing capability of this subsystem promises to hike throughput even more. It will cut the host intervention needed to transfer data and to run the controller.

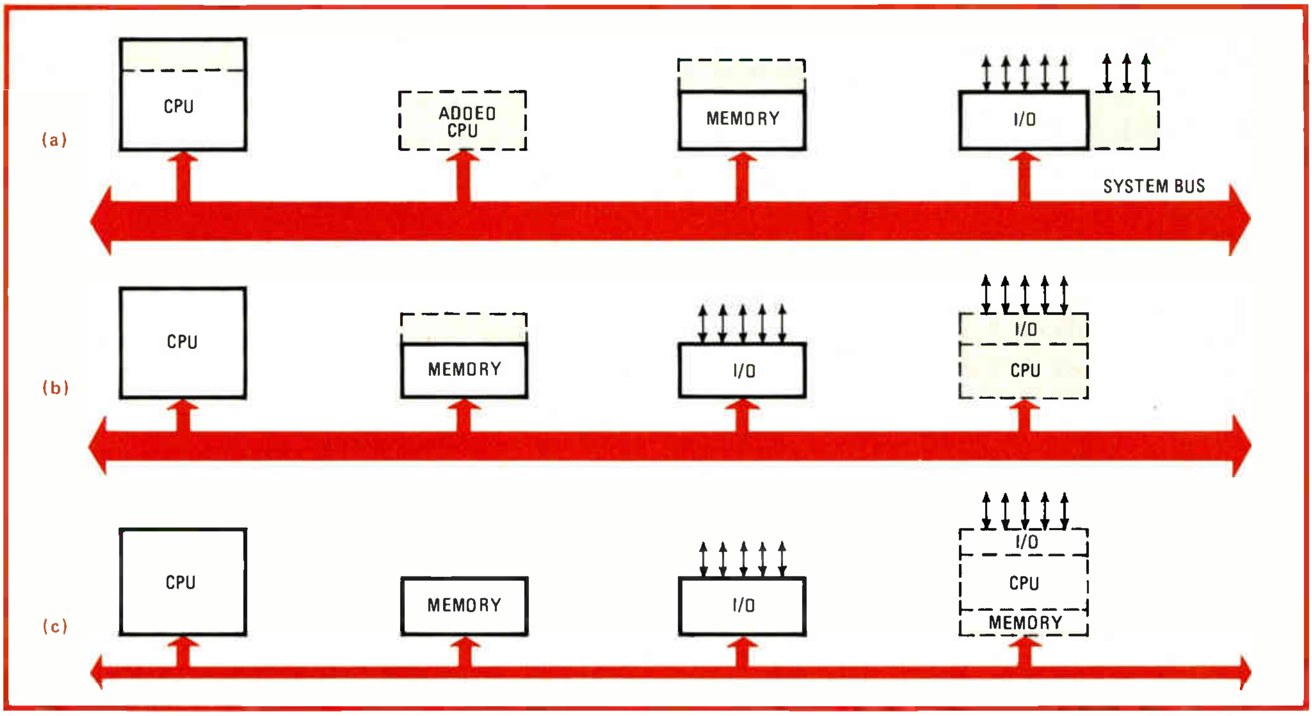
In this configuration, all communications between the host processor and the controller are handled through a section of dual-port memory that resides in the controller subsystem. This setup allows more efficient transfer of large blocks of data from the I/O device to the system without contention over access to the system bus. It also simplifies interprocessor communications because the subsystem controller appears to the host processor simply as an additional RAM board.

Although this concept allows the subsystem to remain dedicated to its I/O control function and to assume a subservient role to the host processor, it has more processing power than previous generations of such controllers. Hence it has been dubbed the intelligent-slave concept by Intel, which applies it in the iSBC 544 intelligent communications controller.

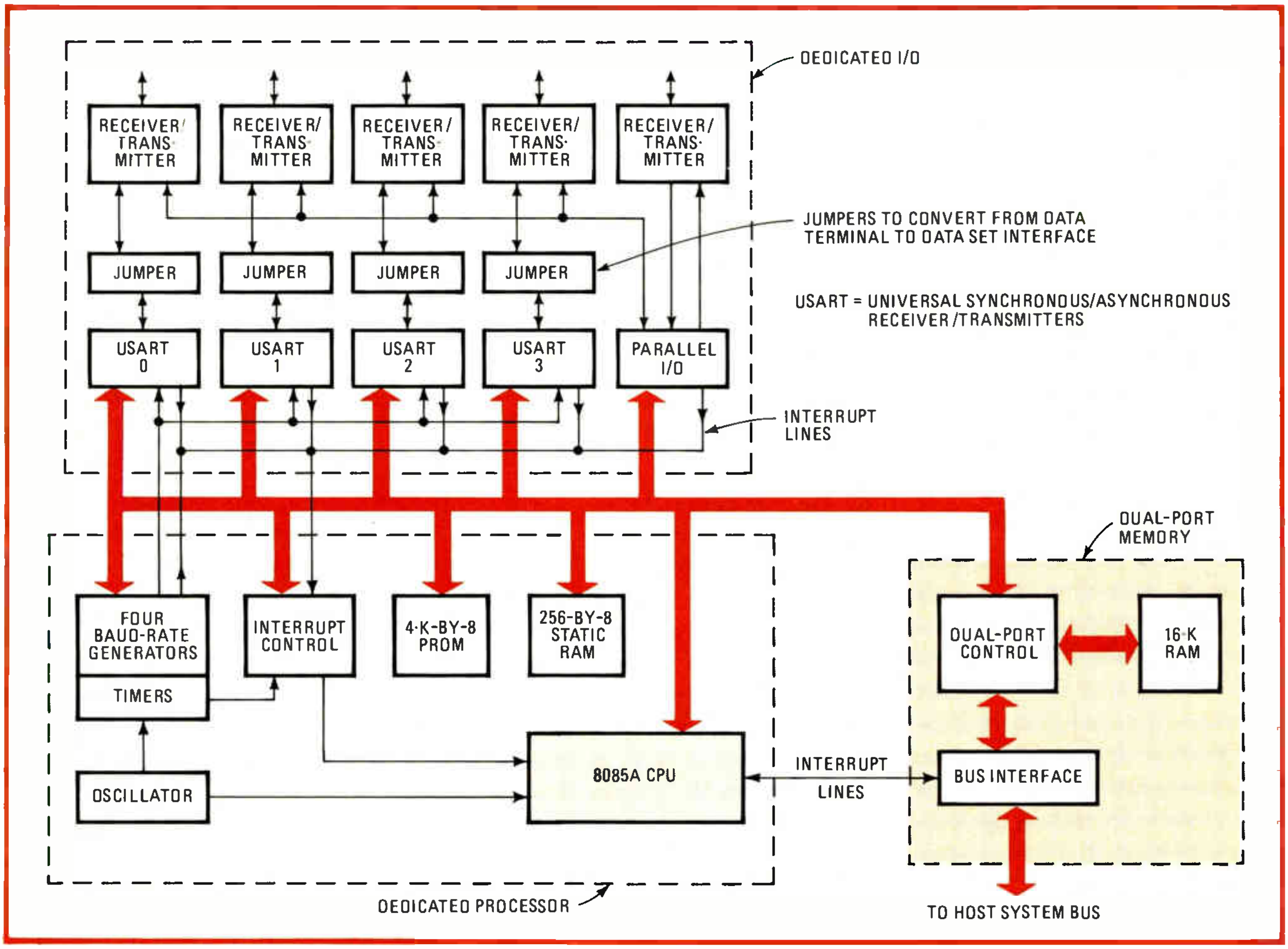
The new subsystem architecture is divided into three major sections: dedicated I/O, dedicated computer, and dual-port memory (Fig. 1). The dedicated input/output,



1. Heart of memory. New controller architecture includes the dedicated input/output circuitry and dedicated processor of an intelligent peripheral controller, but its heart is the dual-port random-access memory.



2. Performance advantages. In adding a real-time task to an existing real-time system, the load on the system bus is significantly reduced over the traditional multitasking approach (a) or the intelligent controller approach (b) by the intelligent-slave controller approach (c).



3. The 544. Based on the 8085A microprocessor with 4 kilobytes of PROM and 16 kilobytes of RAM, the subsystem is designed as a communications controller with four synchronous/asynchronous buffered serial I/O channels, and a 10-bit parallel I/O interface.

Dual-port RAM also shows up in new single-board computer

The concept of a dual-port read-write memory used in the iSBC-544 communications board is also employed in another new Intel product: its latest single-board computer, the iSBC-80/30. A dual port makes the 80/30's random-access memory directly accessible by the on-board 8085A central processing unit via internal busing without tying up the external system bus, the Multibus. At the same time, it also makes the RAM directly accessible by any other boards, like direct-memory-access controllers or other one-board computers that may be tied to the Multibus.

Moreover, the 80/30 adds its dual-port bus to the earlier iSBC computers' pair of buses: an internal bus, which hooks the CPU to peripheral chips and read-only-memory program storage and the system bus, over which the CPU and other boards communicated with RAM. Eight bits wide, the new bus is connected to a pair of buffer registers that coordinate, thus making the RAM accessible either by the internal bus or the system bus.

The objective is throughput: the CPU has priority in access to the on-board RAM. But since the access is not over the Multibus system bus, which might be tied up, there is no waiting. From the viewpoint of other system boards, the system bus is accessible a greater percentage of the time.

With the incorporation of 16 kilobytes of memory on the 80/30, Intel had little choice but to move to the dual-port, triple-bus architecture. The reason is that few system designs require more than 16 kilobytes, so in many applications all boards will be demanding access to the 80/30's memory over the Multibus. The CPU had better have priority to its RAM, through its own private line, lest the queue for the system bus bog down throughput.

The 80/30 also packs lots of extras, in addition to the total 16,384 bytes of read/write memory built with 2116 16-K dynamic RAMs. A pair of ROM sockets provide 4,096 bytes of program storage if fitted with 16-K erasable programmable read-only memories like the 2716. When pin-compatible 32-K erasable PROMs are available, program storage can be extended to 8 kilobytes.

Also on board is a socket for Intel's universal peripheral interface chip, the 8041 (or 8741 erasable-PROM version), which can function as a slave processor to drive peripheral devices. An 8251A universal synchronous/asynchronous receiver/transmitter is included for serial communications, and the 80/30 also boasts three 16-bit programmable timers. The 24 programmable input/output lines are brought out to sockets that accept quad line-drivers or -terminators for interfacing.

Ray Capece

consisting of the necessary peripheral chips, timers, buffers, and interface integrated circuits, tailors the controller to the application's I/O requirements.

The dedicated computer consists of a general-purpose microprocessor, electrically programmable read-only memory, dedicated RAM, timers, interrupt logic, and the decode and chip-select logic. The size and speed of the central-processing unit can be tailored to match the requirements of the dedicated I/O section.

The dual-port memory is the heart of the architecture and sets it apart from traditional approaches to intelligent controllers and multiprocessing. Passing all commands and data between the system and the controller's processor through this memory offers a number of significant advantages.

First, the dedicated computer's performance can be optimized for its applications. Its software always operates at full speed, since all required memory and I/O resources are immediately accessible on the board, without indeterminate delays caused by other system activity on the bus. This accessibility is especially important in real-time systems, since it allows the controller's performance to remain constant even though system bus activity may change.

Secondly, the architecture presents a consistent and convenient interface between the host CPU and all the controllers in the system, regardless of function. Because the controllers' dual-port RAM looks to the host CPU like just another location in system memory, the hardware and software problems associated with connecting multiple processors together are reduced to interfacing a number of identical intelligent memory locations.

Also, the architecture offers a degree of protection for the data in memory. The subsystem computer and software can only alter that portion of system memory that resides in its own dual-port memory section. In contrast, traditional intelligent controllers have access to the entire system RAM and, should a malfunction occur, can destroy all of that memory.

System performance advantages

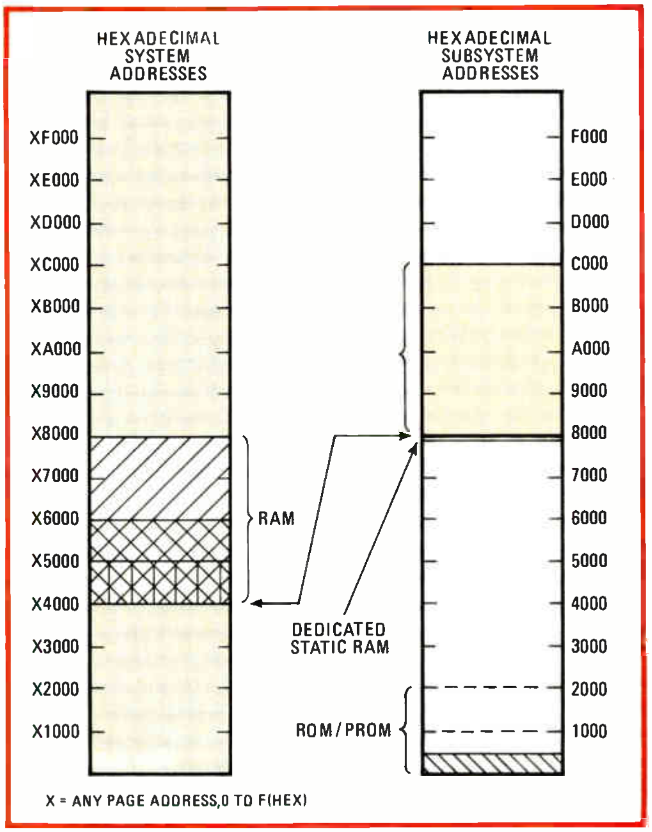
Because all processing assigned to the new controller's CPU takes place off the system bus, its architecture offers important performance advantages to the system. These advantages come from the appearance of the processed data blocks in system memory without consuming any system resources or bus time.

The advantages of this approach are best demonstrated by comparing it to alternative means of adding a real-time task to an existing real-time system. In this case, the new task requires additional CPU, memory, and I/O resources.

The traditional multiprocessor approach of Fig. 2a expands CPU resources in one of two ways: software utilization of reserve capacity in the existing processor, or adding another processor. In either case, memory and I/O increments generally will be required.

The primary disadvantages of this approach are the increased complexity of the system software and the increased load on the system bus. Both will slow the existing real-time system unless it has been designed with adequate reserve. The system bus must also provide sufficient capacity for the incremental memory-execution and data-transfer operations. This additional bus load will also require that the primary real-time task can tolerate CPU delays due to bus contention.

The intelligent-controller approach of Fig. 2b has gained widespread use since the advent of the micropro-



4. Memory mapping. The variable system memory addresses are always mapped into the on-board address of 8000HEX, providing software independence for the subsystem and the host.

TABLE: EIA RS-232-C SIGNALS PROVIDED AND SUPPORTED

Carrier detect	Receive clock
Clear to send	Receive data
Data set ready	Ring indicator
Data terminal ready	Transmit clock
Request to send	Transmit data

cessor. This approach combines the CPU and I/O increments onto a single module that usually includes direct-memory-access transfer logic. In some cases the execution memory for the CPU is included.

This approach lessens the bus-loading problem since the I/O data transfers and some memory-execution cycles take place off the system bus. However, both CPUs' programs will have to tolerate delays caused by increased bus contention. Increased software sophistication is the primary disadvantage of this approach, much as with the multiprocessing approach of Fig. 2a.

The intelligent-slave approach of Fig. 2c can be viewed as a logical extension to the intelligent-controller approach. Combining the CPU, I/O, and memory increments creates a single module that has a minimal impact on the existing system software and bus loading. What's more, the subsystem can operate at full capacity without regard to other system activity. It can be programmed outside the primary system and then added with minimal impact on the system software or performance.

A limitation of the approach is the inability of the subsystem to transfer data into portions of the system memory space that reside off its board. This problem is minimized by the ability of the controller's RAM to serve as a substantial portion of the entire memory space addressable by the system. In this light, the on-board processor can be viewed as having a DMA capability limited to a portion of the system's address space.

In a system with more than one of the new controllers, the system CPU handles any data that must be transferred from one to another. Applications involving the transfer of large blocks of data would be best served by a central block-transfer device elsewhere on the bus.

The advantages offered by the new approach in this example of adding onto an existing system are just as applicable to a ground-up design. This modular approach to configuring real-time multiprocessing systems simplifies hardware and software design, as well as system integration.

While the primary design objective of the new architecture is operation in a multiprocessing system, it can provide significant utility as stand-alone processors. Thus these controllers incorporate a second mode of operation called the limited bus-master mode.

In this mode of operation the new controller can be used like a single-board computer as long as it is the system's only master of the bus. It can be connected to standard memory or I/O expansion boards to enhance its capability. It can even be used to drive other such controllers as long as they are used in the subsystem mode. This dual operational mode will allow the new controllers to serve a broad range of applications.

Communications first

Communications applications present complex processing requirements and an inherent real-time nature, so it is logical that a communications processor be the first of these new controllers to be marketed. The iSBC 544 intelligent communications controller can serve as a flexible front end to an iSBC system or as a cost-effective stand-alone processor configured as a terminal cluster or line concentrator. Its design (Fig. 3) incorporates an 8085A CPU, 16 kilobytes of dual-ported dynamic RAM, 4 kilobytes of PROM, programmable interrupt control, three interval timers, four programmable baud-rate generators, four synchronous/asynchronous buffered serial I/O channels, and a 10-bit parallel interface compatible with a Bell 801 automatic calling unit.

The dual-port memory block basically consists of the 16-kilobyte bank of random-access memory, which is accessible from either the system bus or the on-board processor through the dual-port controller. This memory block provides the primary means of communication between the system and the on-board 8085A. The port to the memory, which looks to the system bus like any other RAM card belonging to the system, features full 20-bit addressing and a typical access time of 600 nanoseconds.

The interface's address-decode logic allows switching of the base address of the iSBC 544 to any 4-kilobyte boundary in the host system's address space. In addition, the user may reserve 8, 12, or 16 kilobits of the 544's memory for use by the on-board processor only. This reserved memory is not accessible from the system bus and does not occupy any system address space. The only restriction is that all of the unreserved memory reside in the same 64-K address page of the system memory.

This memory division can be a significant advantage in large 8-bit microcomputer systems. Only that portion of the controllers' memory needed to pass data between CPUs must be made accessible to the system. The remaining buffer and execution memory does not consume any system address space.

The net result is an increase in the system's overall memory capacity. For example, a microcomputer system that would usually be limited to 64 kilobytes of memory has a total memory capacity of over 190 kilobytes when driving seven 544s.

Address maps and interrupts

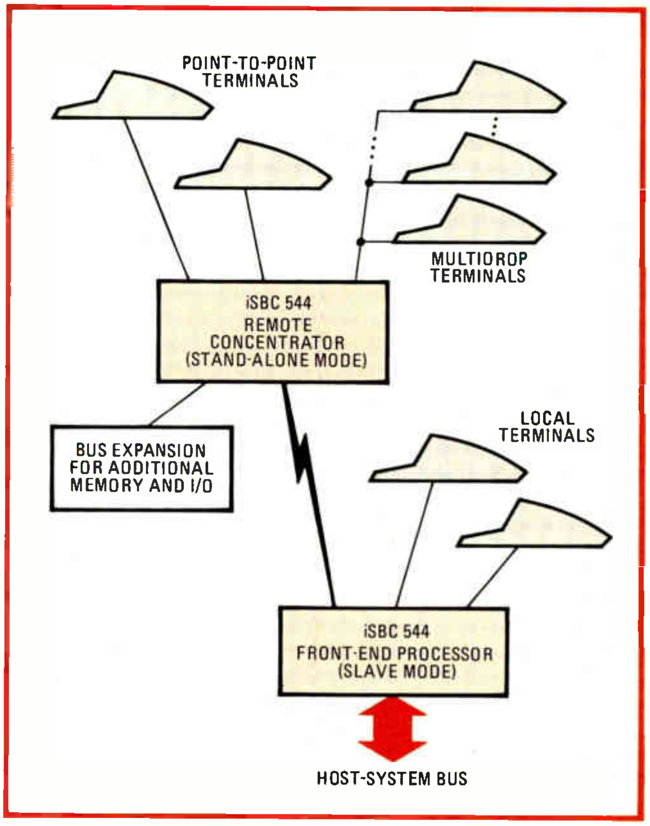
To the on-board processor, the base address of its memory is fixed at 8000HEX. Furthermore, all on-board addresses are fixed, so that multiple 544s operating on the same system bus can be running identical programs regardless of their base address on that bus. This capability necessitated the address-mapping logic to transform addresses from the system bus into the equivalent in the on-board address space starting at location 8000HEX (Fig. 4).

The address-mapping logic also implements the flag-interrupt feature. It provides an interrupt to the on-board processor whenever a byte is written into the 544's base address from the system bus, and a read from the on-board processor to the base address clears the interrupt. Since each 544 in a system has a different base address in that system's RAM, it also has a unique interrupt. This flag-interrupt capability is a key element in establishing a protocol for communications between the host CPU and the subsystems' processors.

The dual-port control logic is responsible for resolving contention over access to the memory and is designed to optimize the performance of the subsystem CPU. Unless the system bus has initiated a memory cycle before the on-board processor requests memory, that CPU runs at full speed. The maximum delay that can be encountered is one memory cycle. The arbitration logic actually reserves the memory for the on-board processor before it generates the necessary commands. This advance reserving guarantees that the on-board CPU will suffer minimum intervention from system bus accesses.

When the iSBC 544 is used in the stand-alone limited bus-master mode, the dual-port logic is disabled and the bus interface buffers are turned around to drive onto the bus. This reversal allows the on-board central-processing unit access to the memory of other subsystems or I/O expansion boards on the system bus.

The dedicated computer is built with an 8085A CPU operating at 2.76 megahertz, between 2 and 4 kilobytes of PROM and ROMs or 8 kilobytes of ROM using 2332 mask-programmable parts, 256 bytes of static RAM, two 16-bit and one 14-bit interval timers, and a 8259 programmable interrupt controller for individual receive or transmit interrupt inputs for each serial port.



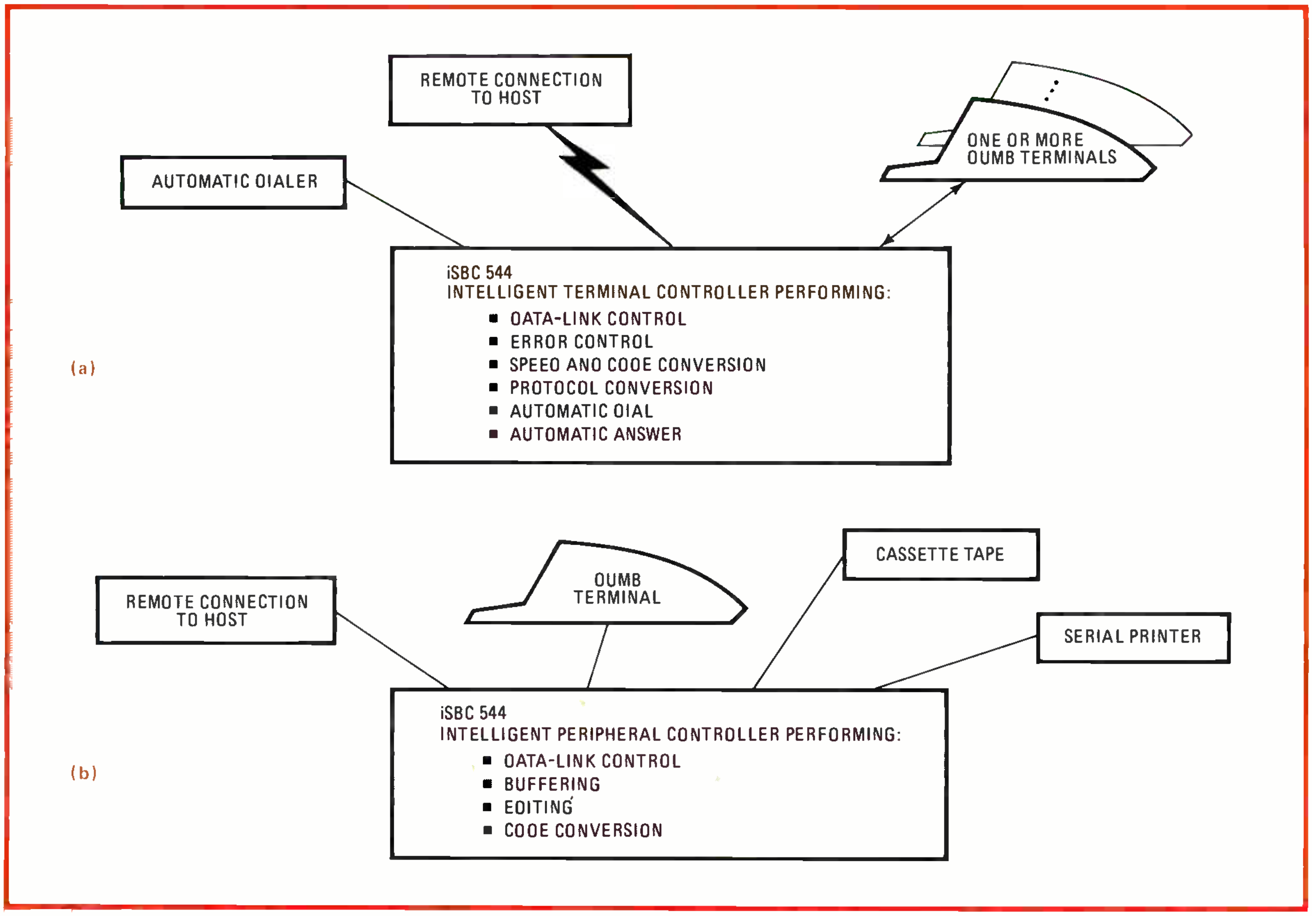
5. Communications applications. Two typical applications of the new iSBC 544 would be as a front-end communications processor to a microcomputer system and as a remote concentrator to a series of point-to-point or multidrop connected terminals.

Special command-decode logic was added to the CPU to allow it to operate at maximum speed independent of other system activity. There are 21 sources of interrupt on the 544, including the separate transmit and receive interrupts for each port and separate timer interrupts. In addition to receiving an interrupt from the system, the 544 can also send an interrupt to the system bus via the 8085A's serial-output data line.

Since this controller is intended for communications applications, latched interrupts are provided directly to the CPU for loss of carrier and ring indicator for all four I/O ports. The ring-indicator and carrier-detect lines can also be monitored through the parallel port.

Dedicated I/O

The dedicated-I/O section of the 544 provides a high degree of flexibility and programmability. This results primarily from the inclusion of four 8251A universal synchronous/asynchronous receiver/transmitters. These devices are programmable for synchronous or asynchronous mode, character size, parity bits, stop bits, and baud rates. Data, clocks, and control lines are buffered with RS-232-C–compatible drivers and receivers to four 26-pin card-edge connectors. Each port is configured as a data-terminal interface, but may be converted to a



6. From slave to master. In its stand-alone mode, the 544 can operate as a bus master and be configured as an intelligent terminal controller connecting dumb terminals to a data link (a) or as a peripheral controller connecting RS-232-C-compatible units to the terminal (b).

data-set interface by changing a single jumper-plug assembly. The ports support most RS-232-C signals (those that are listed in the table).

A programmable baud-rate generator is also provided for each port. The range of baud rates available is 75 to 56 kilobits per second. The generators are implemented with 8253 programmable interval timers, which receive a jumper-selectable input frequency of 1.84 or 1.23 MHz. In addition, one of the CPU's interval timers can be converted to baud-rate operation and jumpered to any port to provide it with split-speed operation.

The 544 also provides a parallel port with four RS-232-C buffered input lines and six RS-232-C buffered output lines. This port is configured to interface to most automatic calling units but may be used as a general-purpose I/O port. It is implemented with an 8155 programmable peripheral interface that also provides the 256 bytes of static RAM and the 14-bit timer.

Applications

A likely common use of the 544 as a subsystem is as a front-end processor or terminal multiplexer (Fig. 5) in an iSBC system. The 544 performs all communications-related functions such as format control, code conversion, data-link control, error checking, data compression, and protocol management. It can handle multiple protocols, line speeds, and data formats.

All the system processor sees are the processed data blocks that appear in system memory. An automatic dialer could be added to provide a dial-up connection to a host processor or network.

Also shown in Fig. 5 is another 544 used in its limited bus-master mode as a remote concentrator and terminal controller. The line and memory capacity of the remote concentrator can be increased by the addition of standard iSBC memory and I/O expansion boards.

The intelligent-terminal controller shown in Fig. 6a is a prime example of a 544 used in the stand-alone mode. It can connect one or more dumb terminals to a data link and provide the necessary buffering, code conversion, and data-link control. It could also connect a terminal that happens to communicate in a different protocol to a new network or to more than one network.

The iSBC 544's multiple serial lines do not have to be used for communications. They can also be used to connect RS-232-C–compatible peripherals to the terminal (Fig. 6b). In this configuration, the 544 can provide message editing and formatting, bulk storage, and hard-copy output.

As this last application suggests, the 544 is the vanguard of a family of intelligent I/O controllers that will add tremendous increases in throughput and versatility to the iSBC line of single-board computers. The basic architecture will simplify the task of developing multiprocessing hardware and software solutions that will overcome throughput limitations. □

Understanding precision crystal time bases

by Lee Myers, *John Fluke Manufacturing Co., Mountlake Terrace, Wash.*

☐ Precision crystal time bases are the heart of a wide variety of test and measurement instruments. Frequency counters and synthesizers in particular depend on them to meet increasingly stringent demands for accuracy and stability. In addition, instruments like oscilloscopes and pulse generators have started using precision timing to broaden their range of applications.

The basic control element of a precision time base is the quartz crystal itself. In its natural formation, the crystal has a hexagonal cross section and terminates longitudinally in a point. From the base crystal, thin slices, or plates, are cut, having the property that each plate will resonate when excited by an alternating voltage tuned to its natural frequency. This frequency is primarily a function of the plate's thickness and original lattice orientation, or "cut," in the base crystal. Unfortunately, for high frequencies the plates are so thin that they are difficult to cut, as well as very fragile.

Crystals may also be operated at odd mechanical overtones of their natural frequency. (The odd mechanical overtone of a crystal, although not exactly equal to the odd harmonic of the natural frequency, is very close to it.) A major factor to consider in choosing an overtone crystal is its number of spurious vibrating modes, which increase with plate thickness and degrade the crystal's performance.

Types of cut

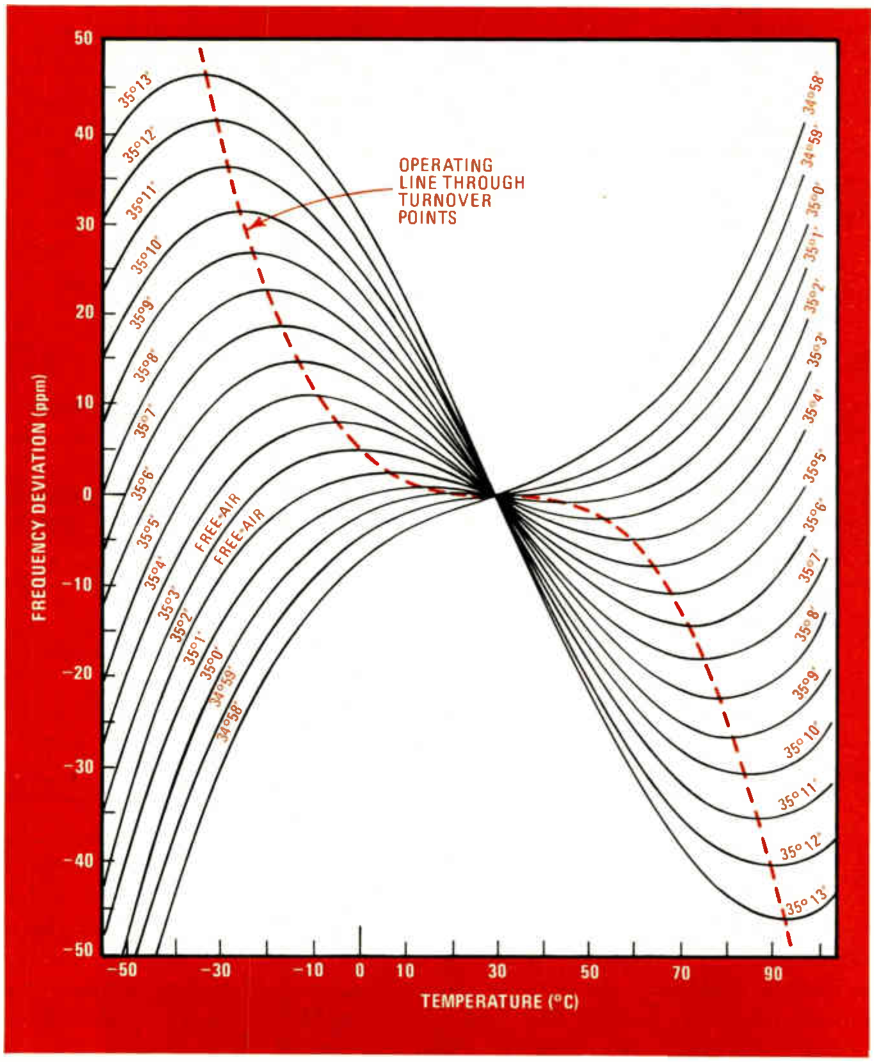
The cut angle of a crystal also determines the long-term frequency stability and basic temperature characteristics of the time base. Several cut types are available, and the designer can select the one that will best meet the frequency and stability specifications required. The AT-cut crystal has a frequency range of 1 to 150 megahertz and is the type most often used in time bases (10 MHz being the most popular choice) because of its frequency and temperature characteristics. The curves in Fig. 1 relate the performance of several AT cuts in terms of the frequency deviation versus temperature for a nominal frequency of 10 MHz.

Once cut to the appropriate angle, the crystal is processed and mounted in a metal or a glass container (Fig. 2). The container may be sealed with either glass or solder and evacuated or filled with an inert gas.

The packaged crystal may then be used in any of a variety of time bases depending on the end performance requirements. There are three basic types, listed in order of increasing frequency stability and price (see table):

- Simple, or "free air," time bases, in which the ambient temperature noticeably affects crystal performance.
- Temperature-compensated crystal oscillators (TCXOs),

This is part 3 of the continuing "Microseconds and megahertz" series, which is designed to bring engineers up to date on the latest techniques of time and frequency measurement. Part 1, which appeared in the March 30 issue, pp. 81–88, covered the use of digital counters and timers. Part 2, in the June 22 issue, pp. 138–144, discussed methods of eliminating time-base errors from oscilloscope measurements. Follow-up articles will describe other modern instruments like microprocessor-controlled spectrum analyzers and triggering oscilloscopes.



1. AT type. A crystal's frequency stability depends on the cut angle and the operating temperature, as illustrated by the family of curves generated by crystal cuts for a nominal frequency of 10 MHz. Varying the cut angle by a few minutes changes the performance significantly.

which utilize an electrical network to regulate the frequency as ambient temperature varies.

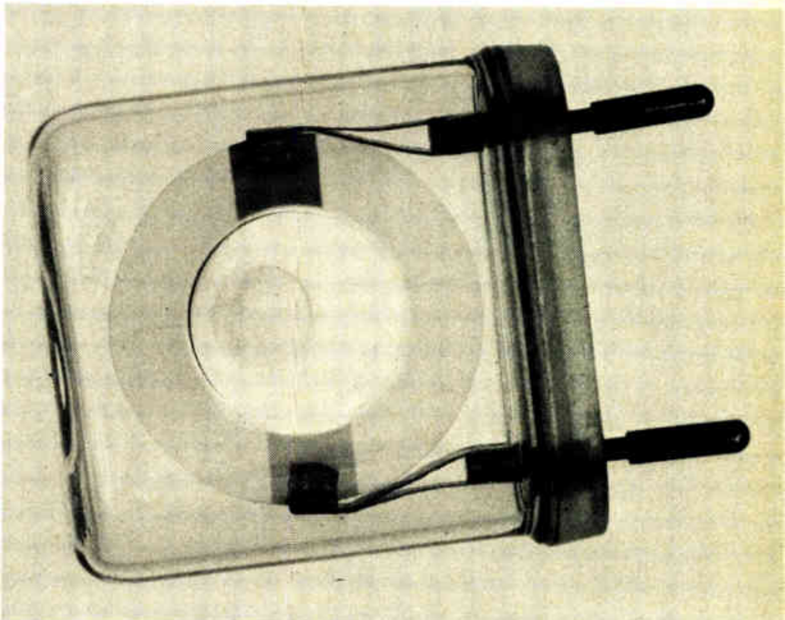
■ "Ovenized" time bases, which have an internal heating element to provide a controlled operating temperature higher than the external ambient temperature.

Free-air time bases

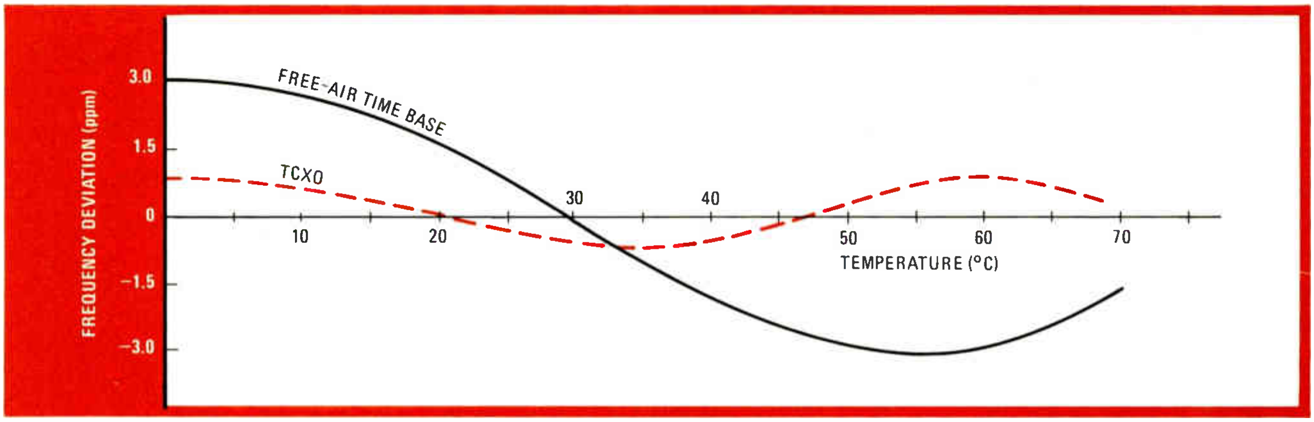
The free-air type of time base, as the name implies, does not rely on an external temperature-compensating circuit or an oven to achieve its overall performance. It is used when moderate performance and small size at low cost are required.

Proper oscillator design and crystal cut angle will yield moderate temperature stability. For an AT-type crystal used in a free-air time base, cut angles of 35°2′ and 35°3′ are typical. A temperature dependence of ±5 parts per million (±50 hertz for a 10-MHz crystal) over the 0°-to-65°C range is readily obtainable, with ±2.5 ppm over a range of 0° to 50°C the optimum available at a reasonable cost.

A free-air time base's aging rate, that is, the rate at which the crystal drifts off frequency, is determined almost solely by the crystal's characteristics. Cleanliness in processing, the type of mount, and the type of seal all affect the final drift performance. Typically, an initial



2. Free-air package. In order to limit environmental influences, the crystal is mounted and sealed either in a glass container, shown here, or in a metal one. Glass-enclosed crystals tend to increase in frequency with aging; a decrease occurs with metal enclosures.



3. Improved stability. The performance of a TCXO is superior to that of a free-air time base in terms of both maximum deviation from and tracking of the nominal frequency over a wide temperature range. A total yearly drift of less than ± 1.0 ppm can be expected for TCXOs.

COMPARING TIME BASES

	Free-air	TCXO	Ovenized
Frequency-drift factors			
Aging rate	$\pm 5 \times 10^{-7}$ per month	$\pm 3 \times 10^{-7}$ per month	$\pm 5 \times 10^{-9}$ per day
Temperature (max shift, 0° – 50° C)	$\pm 5 \times 10^{-6}$	$\pm 2 \times 10^{-6}$	$\pm 1 \times 10^{-8}$ per °C*
Line voltage (max shift, 10% change)	$\pm 1 \times 10^{-7}$	$\pm 1 \times 10^{-7}$	$\pm 1 \times 10^{-9}$
Warm-up time (until deviation is $\leqslant 1 \times 10^{-8}$ ppm)	not specified	not specified	20 min
Relative price	X	X + $150	X + $550

* Refers to oven temperature.

aging rate of 0.5 ppm/month can be expected, and this figure declines substantially with time in operation.

Temperature-compensated crystal oscillators bridge the gap between free-air time bases and expensive, higher-performance ovenized ones. They are possible because a crystal's resonant frequency may be altered by placing a reactance in series with the crystal, and therefore a temperature-sensitive impedance can be used to compensate for frequency drift.

TCXOs

Once the cut has been made for the desired variation over the specified temperature range, the crystal is placed in a thermal test chamber and its actual frequency variation with temperature is plotted. With the aid of computer analysis, circuit parameters are selected that will counteract as closely as possible the crystal's inherent frequency variation with temperature.

Compensation schemes using analog, digital, and hybrid circuits are available, with some employing microprocessor control. The great majority, however, use analog techniques, the two most common being the thermistor-varactor compensation and the temperature-compensating capacitor network. The choice depends primarily on the operating conditions inside the instrument containing the time base. Typical temperature dependences of ±0.5 to ±2 ppm from 0° to 70°C may be obtained at reasonable cost.

The aging rate of a TCXO is largely dependent on crystal quality, as is the case with free-air time bases. Usually, crystals with an initial aging rate of less than 0.3 ppm/month are used in TCXOs, and total yearly drift can be less than ±1.0 ppm.

Because of the imperfect cancellation of temperature effects, the time base's final plot of frequency vs temperature will vary from unit to unit. Figure 3 illustrates the frequency drift of a temperature-compensated crystal oscillator compared with that of a free-air time base over a typical temperature range.

The advantages of a TCXO are good temperature performance, small size, fast warm-up, and low power consumption at a moderate price.

Calibration of TCXOs, however, can be a problem. Since the oscillator will almost always be embedded in an instrument with a 5°-to-15°C heat rise, calibration at room temperature requires careful calculation based upon the known frequency-temperature characteristics for that TCXO.

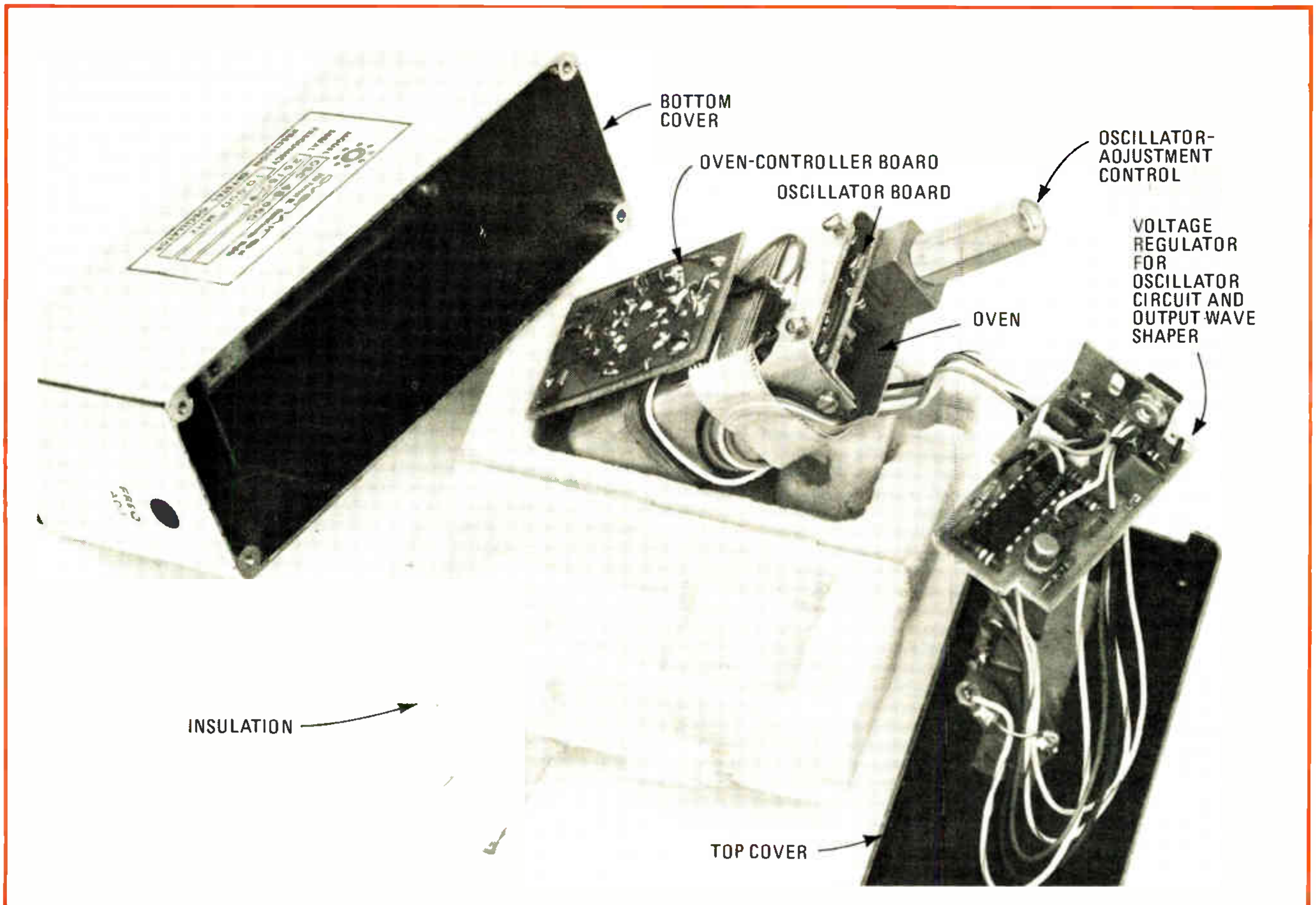
Calibration methods

A more common method, which eliminates the need to account for the heat rise, is to operate the instrument at a known ambient temperature (usually 25°C) and to adjust the frequency to an offset, both specified by the time-base manufacturer. The manufacturer then guarantees that the TCXO will meet specifications across the full temperature range.

Both calibration methods leave a lot to be desired from the customer's standpoint. Calculating heat rise is complicated and providing a fixed ambient temperature is difficult to do outside a well-controlled calibration laboratory. But the instrument manufacturer can elimi-

What to look at in considering a crystal time base's performance

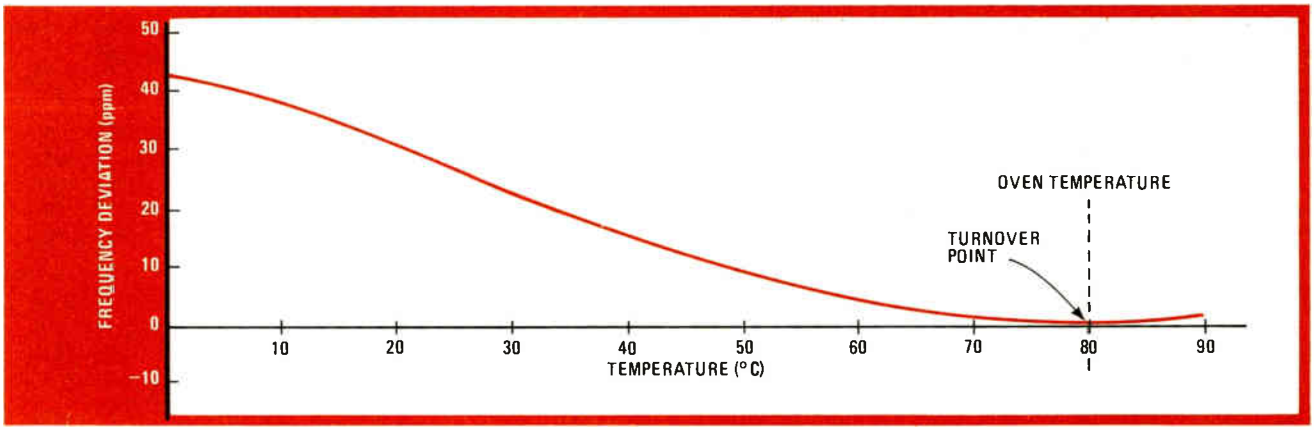
Aging rate	the rate at which a crystal drifts off frequency with time
Power-supply dependence	the amount of frequency variation with change in line or battery voltage
Restabilization	the time it takes an oscillator to return to a given aging rate following a period of nonoperation
Retrace error	the offset (after warm-up) from the frequency prior to turn-off, when an oscillator is turned off for a period of time and then turned back on
Shock, vibration, humidity, and gravitational dependence	the amount of frequency variation resulting from, respectively, shock, vibration, humidity, and the physical positioning of the time base
Short-term stability	the amount of frequency variation during short periods of time due to random frequency fluctuations—typically specified at 1 or 10 s; in synthesizer applications, it may be specified as phase noise
Temperature dependence	the amount of frequency variation with change in temperature.



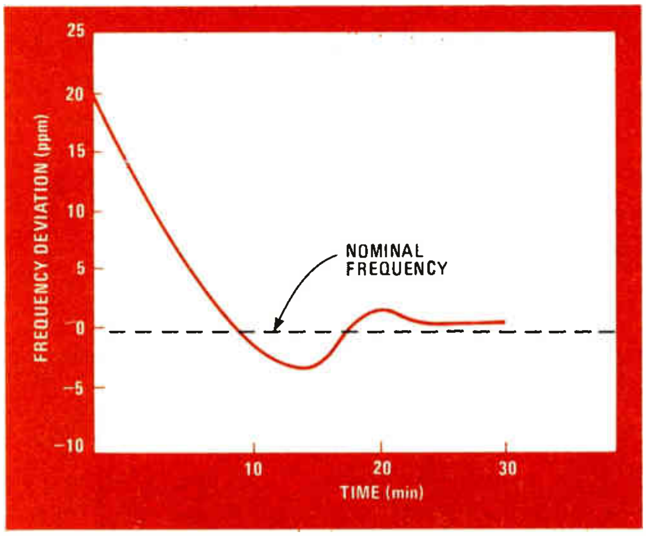
4. Ovenized time base. Both the crystal-oscillator board and the temperature-controller board are insulated to minimize outside thermal influences. The voltage-regulator–wave-shaper board is mounted outside the insulation to limit additional heating and to provide dissipation.

nate these problems by using a time base with a tighter tolerance and specifying that calibration of the instrument be performed at any ambient temperature between, for example, 20° and 30°C. The instrument with its high-performance TCXO should then meet specifications across the full temperature range.

Ovenized time bases use a controlled-temperature oven to insulate the crystal from ambient temperature changes (Fig. 4). The crystal itself is cut at a high angle so that the higher temperature bend in the curve, called the turnover point (see Fig. 1 again), is at the operating temperature of the oven. The oven temperature is set 10° to 15°C above the highest temperature ever expected at the location of the time base within the instrument, and



5. Hot operation. An ovenized time base can be expected to track its nominal frequency exactly upon reaching and maintaining the designated operating temperature. Ovens typically maintain the specified temperature to within 0.2°C to provide superior performance.



6. Warm-up. Although frequency deviation decreases significantly as warm-up time approaches the 30-minute mark, it may take much longer, even days or weeks, to return to the specified aging rate (restabilize) if the oscillator has been off for months.

the oscillator is adjusted to be exactly on frequency at that oven temperature (Fig. 5).

Ovenized time bases offer outstanding temperature stability because of tight thermal control of the crystal. An oven crystal will generally vary about 1 part in 10^8/°C if the oven has been set to within ±1°C of its turnover point. Ovens typically maintain temperature to within about 0.2°C to provide superior performance. Therefore temperature stabilities as good as ±5 parts in 10^9 from 0° to 50°C can be expected.

Other considerations

However, because ovenized time bases have extremely good temperature stability and aging rates, a variety of considerations that are unimportant in free-air time bases and TCXOs become significant.

For one, since the crystal is to be operated at an elevated temperature, its frequency at initial turn-on will be far off the intended operating frequency. As can be seen in Fig. 5, an ovenized oscillator with an internal temperature of 25°C at turn-on will start out 25 ppm off frequency, because the oscillator has been designed and adjusted to be on frequency when the crystal is at the designated 80°C operating temperature. As the oven and crystal warm up, this offset decreases, as shown in Fig. 6.

After initial warm-up, other factors emerge. Restabilization, or the time it takes for the oscillator to reach its specified aging rate, must be known so that the user can calculate total drift. The time depends primarily on how long the oscillator was off before power-up: the longer the oscillator is off, the longer it will take to reach its specified aging rate. This period can be as much as several weeks if the oscillator has been off for months. In practice, typical aging rates for an ovenized time base will range from 1 part in 10^8 per day to 5 parts in 10^{10} per day, depending on the type of crystal used. (Note that restabilization refers to the return to the aging rate and says nothing about return to frequency.)

Frequency retracing

Frequency retracing defines how closely an oscillator will return to its original frequency after a lengthy on time and a specified off time and subsequent warm-up period. A typical retrace specification might be: "The time base will return to within 1 part in 10^8 of previous frequency following a long period of operation, 2 hours off, and 5 hours subsequent warm-up."

Retrace errors and restabilization times both must be carefully taken into consideration when deciding whether to use an ovenized time base or a TCXO. If the time base is to be turned off for long periods and expected to perform quickly on turn-on, a TCXO may be a better choice.

Time-base literature rarely gives specifications for deviations caused by shock and vibration. Since a shock of 20 g for 15 ms or a vibration of 5 g can cause typical frequency variations of 1 to 2 parts in 10^8, such effects can be especially significant when calibrating an ovenized time base.

Typically, an instrument containing a time base is unplugged, shipped to a calibration laboratory, adjusted to frequency, unplugged, reshipped, and finally plugged in again and operated. The possibilities of shock- and vibration-induced errors in this cycle are numerous and can easily defeat the entire calibration effort. Therefore proper calibration should include special handling of the instrument. □

Digital sample-and-hold speeds a-d conversion time

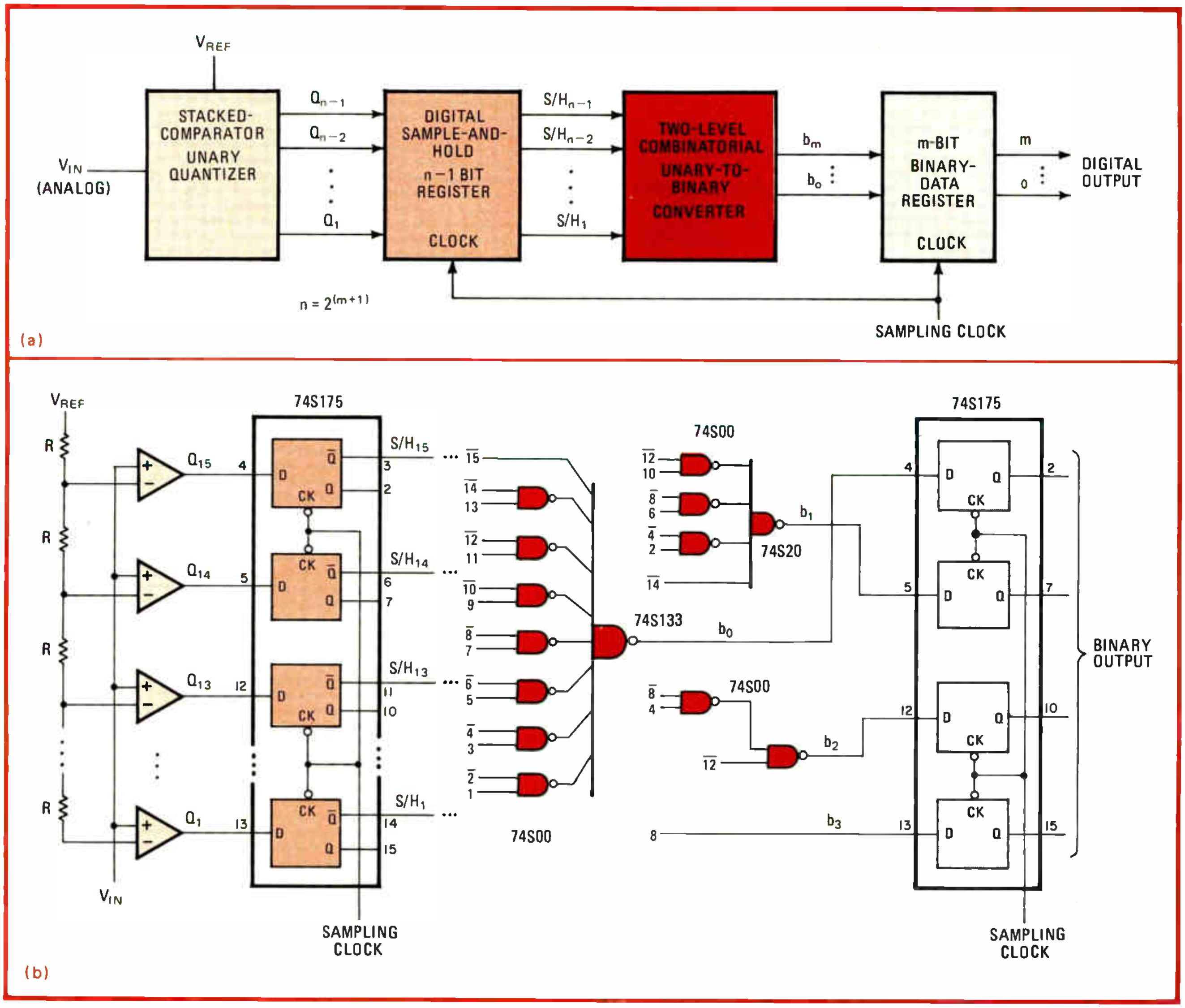
by T. L. Sterling
Massachusetts Institute of Technology, Cambridge, Mass.

A set of comparators and latches serves as the sample-and-hold quantizer for this analog-to-digital converter. As a consequence, the circuit offers a faster conversion time than those converters using standard, relatively slow and expensive sample-and-hold units that work on the principle of storing a sampled voltage on a capacitor.

In this circuit, the analog signals are immediately transformed into a digital signal by the comparators, then stored by the latches, and finally converted into binary form with combinational logic. This scheme saves the extra time required by a counting-type encoder to change the analog signal to its binary equivalent.

This stacked-comparator technique, as it is called, is especially convenient in high-speed, small-word applications, where it provides reasonable accuracy. The overall system is shown in (a), with the actual circuitry for a 4-bit a-d converter shown in (b).

The comparators convert an analog-input signal into a digital signal with a resolution proportional to the number of threshold voltages in the comparator circuit. The output line of any comparator will move high when



Jammed pipeline Analog-to-digital converter (a) that uses comparators and latches for sample-and-hold quantizer can perform fast conversions at relatively low cost. Comparators and latches perform parallel, or jam, transfer of unary (base-1) data (b) as previous sample is processed by output register (pipeline operation). Unary-to-binary converter uses combinational logic.

the analog signal amplitude exceeds its associated threshold voltage.

The cumulative output of the 15 comparators is a unary (base-1) representation of the quantized signal. As the input signal varies, only one output line can change at any one instant. This setup provides a maximum error of one digit when sampled, which is equivalent to an error of one least significant digit of a binary-signal representation. Furthermore, because the output of the quantizer closely tracks the analog input (the delays are slight and constant for each comparator), it is possible to simultaneously sample the output of all comparators using digital storage elements. The sampling and storage of data are provided by a high-speed clock and a set of 74S175 high-speed latches, respectively. One flip-flop is required for each output line that is sampled.

The unary data stored in the latches is converted to a binary-equivalent number with the aid of combinational logic and stored in the output register. The numbers at the input to each gate refer to the inverted (or noninverted) outputs of the sample-and-hold flip-flops. Both sets of latches are loaded simultaneously. This is a serial, or pipeline, configuration, but no time is lost in processing one sample at a time, because the input and output latches process two consecutive samples, n + 1 and n, respectively, independently of each other.

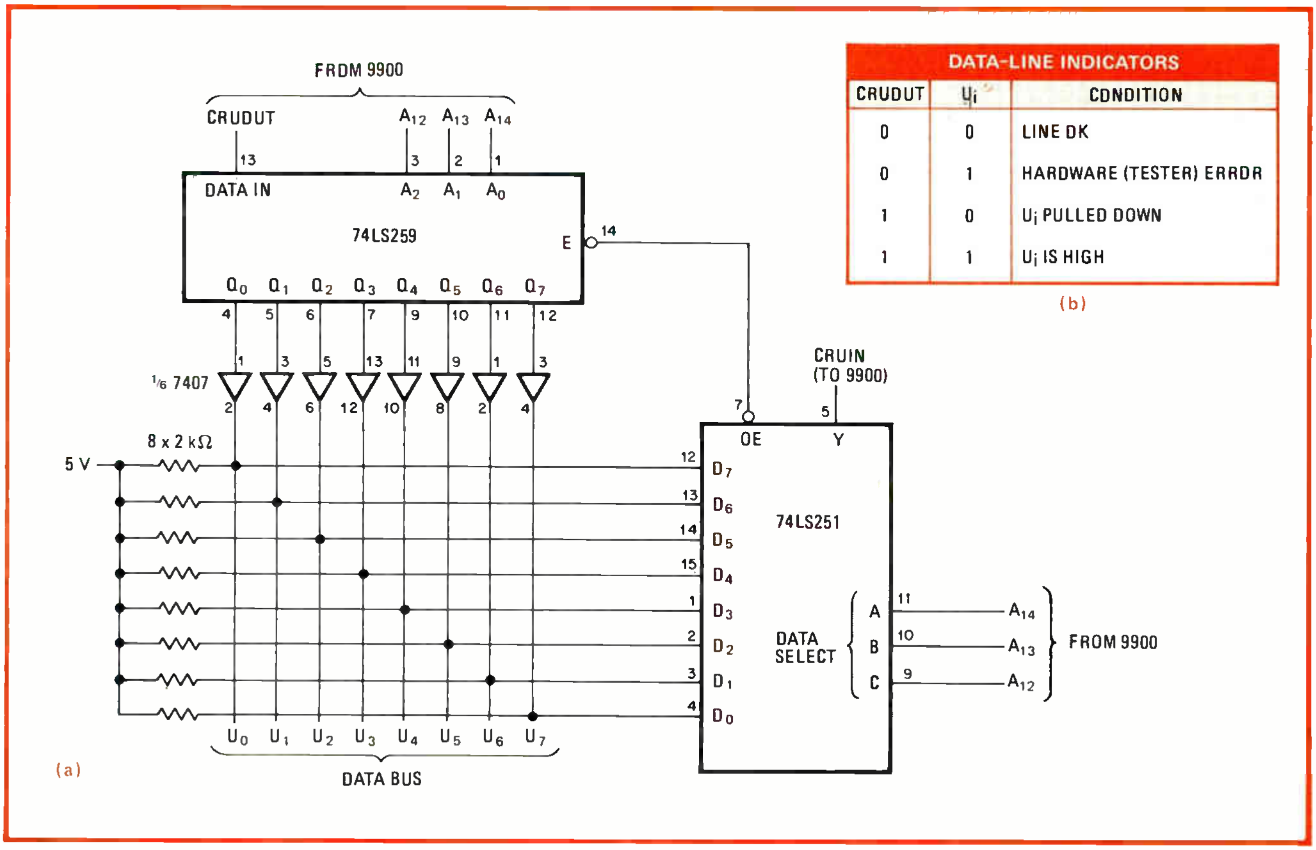
The sample rate is limited by the propagation delay of the two registers and the unary-to-binary converter. For the devices shown, a typical clock rate is 40 nanoseconds plus the delays imposed by circuit-layout capacitance. □

9900 simplifies design of bidirectional I/O module

by Henry Davis
American Microsystems Inc., Santa Clara, Calif.

By combining standard addressing and multiplexing logic with the unique interface structure of the AMI 9900 microprocessor, a truly bidirectional input/output module may be realized. This read/write unit is especially suited to digital test systems, but it will find applications in many general-purpose systems as well because of its low cost and the ease with which it can be interfaced with the microprocessor.

Design of the bidirectional module is simplified because the structure of the 9900's communications-register unit makes it possible to handle the data-bit stream efficiently with a minimum of software. The CRU supplies up to 4,096 input and output bits that can be directly accessed and may be addressed either individually or in fields of 1 to 16 bits. The 9900 employs three



DATA-LINE INDICATORS

CRUOUT	U_i	CONDITION
0	0	LINE OK
0	1	HARDWARE (TESTER) ERROR
1	0	U_i PULLED DOWN
1	1	U_i IS HIGH

(b)

1. Two-way street. Bidirectional I/O interface uses standard TTL addressing and multiplexing logic (a). The 9900's architecture simplifies both hardware and software. I/O can detect several output-line states, notably pull-down conditions due to short circuits on data bus (b).

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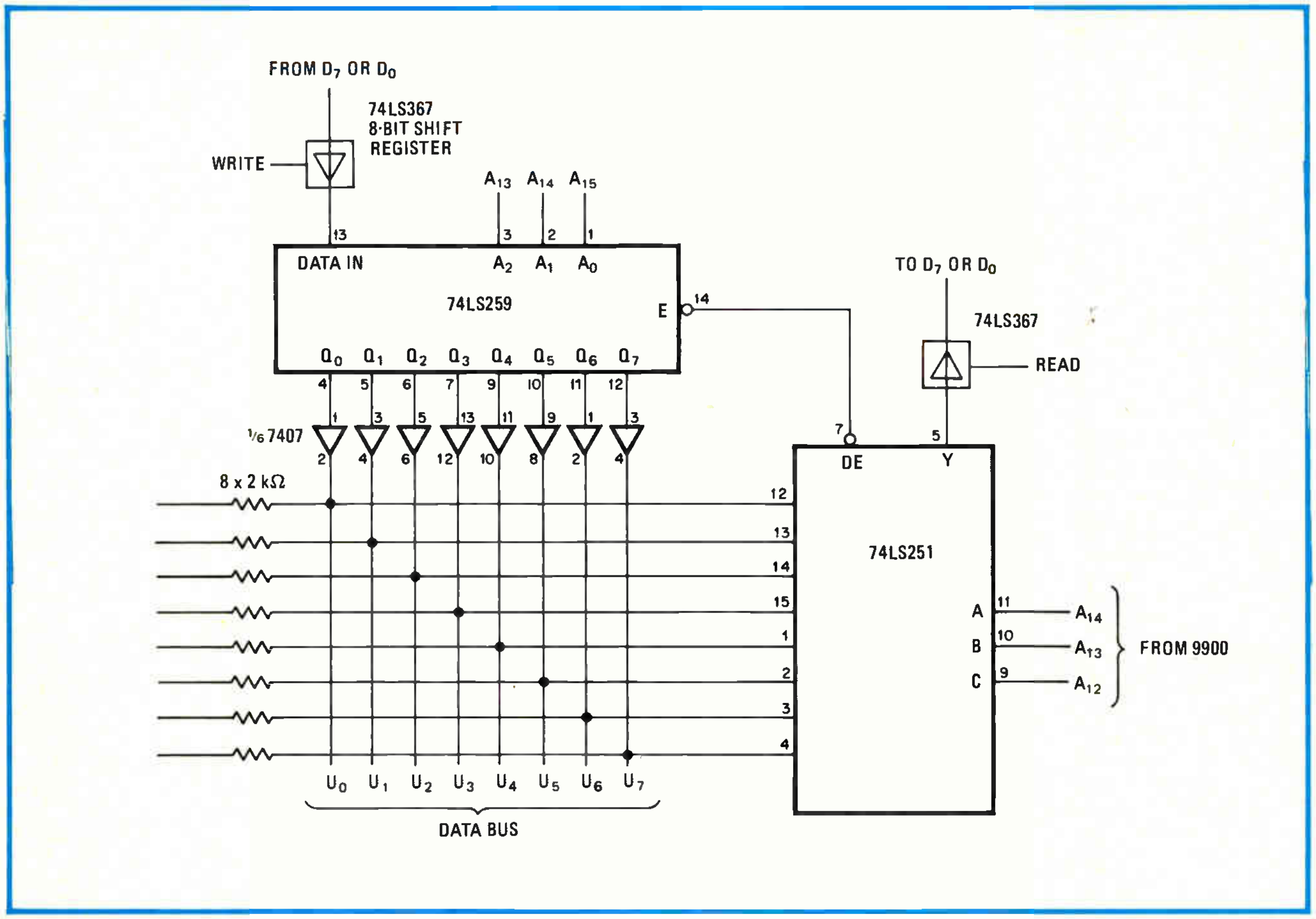

2. Easily mated. I/O unit can interface with other processors, such as the 6800. Software requirements will be more stringent, however; they must provide for serial-to-parallel and parallel-to-serial conversions. Also, each bit must be mapped into one byte.

dedicated I/O pins (CRUIN, CRUOUT, and CRUCLK) and has 12-bit capability (lines A_3–A_{14}) of the address bus for interfacing with the CRU system. The processor instructions controlling the CRU (SBZ, SBO, TB) can respectively set, reset, or test any bit in the CRU array or move the bits between memory and CRU data fields.

In the circuit example in Fig. 1a, the 9900 is used to perform an 8-bit parallel-to-serial conversion for data that is to be written on the data bus, from the microprocessor through the 74LS259 addressable latches. During all read operations, the 9900 converts the serial data stream emanating from the 74LS251 eight-channel multiplexer (which receives the bus data) into a parallel word so that it may be processed.

As for the software, the bit instructions SBZ, SBO, and TB control a single processor-to-I/O data line, selecting the address corresponding to the bit desired and executing the required bit setting or bit test, as the case may be. Multibit transfers are implemented by the processor using the LDCR and STCR instructions.

Whether in the read or write phase, the starting address of the CRU field to be transferred should first be loaded into the base-address register. This address is the least significant bit of the CRU field to be acted upon by the software. Next, data should be transferred in the appropriate direction (system memory to I/O interface or interface to memory) by reading or writing each I/O line in succession, under automatic processor control. The LDCR output of the CRU initializes the shift of the desired field from the memory to the I/O, through a register in the 9900, if in the write phase. The bits corresponding to the field to be transferred are then shifted out onto the CRUOUT line, which is connected to the 74LS259. The noninverting, open-collector buffers (7407s) protect the latches from short circuits on the data bus.

To use the I/O module for read-in, a logic 1 (high) must be written onto the corresponding output line to be examined (from the processor through the 74LS259). This will cause the 7407 to be pulled low if the data bus line is at logic 0. The CRUIN line can then be read using the STCR instruction.

The CRUIN line may be used to verify an output condition, making it easy to detect short circuits on the data bus. The procedure is to set all lines high, lower each in succession, and then read the lines to check for multiple lows. The table (Fig. 1b) outlines the various input/output conditions.

The circuit may be easily modified to work with other processors. For instance, Fig. 2 depicts such an arrangement for the 6800 microprocessor. A greater burden is placed upon the software here, because the program must perform the serial-to-parallel and parallel-to-serial conversions. □

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Circle 123 on reader service card

Engineer's newsletter

Lossy chokes could sap gate speed

On this page on June 22, Iklil Kayihan suggested that vhf noise on TTL power supply lines could be damped using lossy chokes. But D. S. Walton of Icthus Instruments Ltd., Gateshead, Tyne and Wear, England, disagrees. He says that noise voltages on a system's supply lines are caused by changes in a gate's output, causing rapid changes in current demand—**on the order of 50 mA in as little as 1 ns.** This demand must be met rapidly, or else the gate speed and thus system speed will suffer.

Walton notes that any inductance inserted between the gate package and the decoupling capacitor opposes any rapid change in current demand and so actually does slow down the gate. Rather than add more inductance, his recipe for low-noise power distribution more or less follows the conventional approach—use a large enough decoupling capacitor (1 μF or so per package) to meet the transient current demand without introducing a significant voltage drop. The stray inductance between capacitor and package should also be held to a minimum.

Washer lets you trim component leads uniformly

Trimming component leads on a wired pc board need not be a messy job. Jim Macdonald of Commercial Engineering Associates in Princeton, N.J., has come up with two neat schemes for trimming them exactly.

His simplest tool is just a small washer with a handle soldered on at an angle, similar to a dentist's mirror. He places the washer over the leads on the circuit card, rests a cutter against the washer, and then snips the leads. This method is fine when just a few leads need be trimmed.

For a crowded card with many components, a spacer board that drops over all the leads is preferable to a washer. This is simply a blank card that is drilled to the same pattern of holes as the wired circuit board or boards. Its holes are enlarged a few drill sizes to fit over the leads easily and accommodate the solder surrounding them.

Conferences offer update on data communications

Are you deep into data communications? Three conferences sponsored by Data Communications magazine could help you. On Nov. 6 and 7 at the Peachtree Plaza, Atlanta, Gilbert Held, the chief of data communications for the U. S. Civil Service Commission, will talk about "Understanding Data Communications Network Components." He will **describe 23 components used in data networks, how each operates and where it can best be used.** On Nov. 8 through 10, at the same location, a conference on Network Management and Tech Control will be led by John Nuwer, supervisor of data transmission for Atlantic Richfield, and Al Marshall, director of data communications of the Texas State Department of Human Resources.

The Integrated Data/Voice/Facsimile Communications Conference, to be held on Dec. 11–13 at the New York Hilton Hotel in Manhattan, will feature five speakers from Network Analysis Corp., Great Neck, N. Y., who will discuss "Getting Ready for the '80s."

Registration fees for the conferences range from $395 to $595. For more information, contact McGraw-Hill's Conference Group, 1221 Avenue of the Americas, Room 3667, New York, N. Y. 10020 or call (212) 997-4930.

Jerry Lyman

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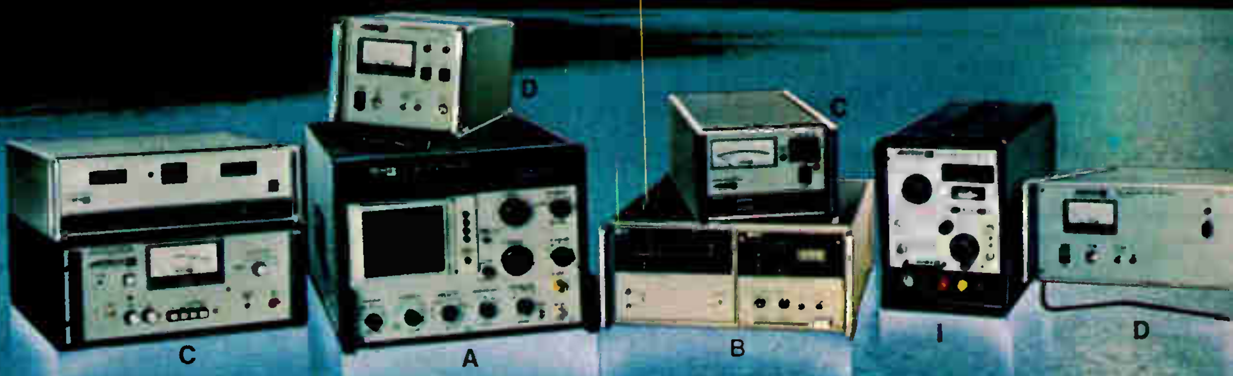

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GENERAL ELECTRIC

LED arrays stack uniformly

5-by-7 dot matrixes are available in red, orange, yellow, and green; maintain 0.1-in. spacing even when stacked end to end or side by side

by William F. Arnold, San Francisco regional bureau manager

Design engineers have had a hard job finding standard arrays of light-emitting diodes that are easily stacked or strung into attractive, readable displays. Itac Corp.'s new line of five-by-seven-dot-matrix LED arrays in red, orange, yellow, and green could end their search.

The packages are the first arrays that can be stacked end to end and/or side by side for use as continuous-area displays of various lengths and widths, and are the first such devices offered as standard products using reflector technology, according to president Dan Davis. "I think the significance is the versatility they give the designer," he says. "They let the designer make a continuous string of a display to make alphanumeric segments or build up an X-Y screen in a dot matrix."

The arrays each consist of 35 LED reflector areas arranged in a five-by-seven format on 0.1-in. centers. Reflector-area diameter is 80 mils, and the entire array is housed in a dual in-line package that measures 0.5 by 0.7 in.

Each dot segment can be driven by a current as low as 2 mA, although 10 mA is a more typical figure. The 5700 series comprises row-cathode and row-anode units in all four colors, for a total of eight units.

The importance of the end-stacking property is that it lets the arrays be made into continuous Times Square–type displays in which characters appear to float across from one array to another, explains Robert McLaughlin, applications manager. Other standard matrix arrays are discrete-character displays, which means that in multiple-array

configurations the character jumps from one array to another—very hard on the eyes, he says.

An attractive feature of the package design, Davis notes, is that the walls of the package are designed so that when the arrays are stacked or strung, they give the impression of a continuous display. The diodes along the edge of one package are the same distance from their counterparts on the other as from their own package mates. The fact that the walls of the package do not protrude above the display surface also helps maintain a clean appearance.

Potential applications cover a host of display uses, such as computers, games, appliances, point-of-sale equipment, instruments, telecommunications, graphical display, word processing, microprocessor display, industrial controls, audio electronics, and medical instrumentation. Davis mentions that a possible military application would use "a scanner to pick up information in the front of the vehicle and have the information displayed on a panel inside the vehicle." Other technologies, such as gas-discharge or liquid-crystal displays, "just aren't rugged enough," he says, noting that they depend on glass-to-metal seals.

There is no fundamental limit on the size of a display made up of 5700 series arrays, Davis says. One must simply be prepared to supply the necessary power and to provide for the necessary cooling. Practically speaking, however, he thinks they make the most sense in 16-, 32-, and possibly 40-character rows. In panels, he says that 8- or 10-unit panels give "a nice matrix format."

The arrays are driven like any conventional display, McLaughlin explains. This means using a read-only-memory decoder plus clocks for a discrete digit or a ROM decoder plus a buffer store for a panel. If a microprocessor has an on-chip seven-segment display driver, as some oven controllers do, then it can drive up to eight arrays. If not, conventional peripheral drive circuitry can be used.

The 5700 series has a maximum power dissipation, at an ambient temperature of 25°C, of 350 mw per element; a storage and operating temperature range of −20° to +80°C; and a continuous forward current of 20 mA per element. Prices, for lots of 1,000 or more, are $5.75 each for the red arrays and $7.60 each for the others. Units are available for immediate delivery. Itac expects prices to drop below $3 each for very large quantities; it also expects to announce second sources and offers the devices in custom assemblies with and without drivers and logic.

Itac Corp., 2045 Martin Ave., Suite 203, Santa Clara, Calif. 95050 [338]

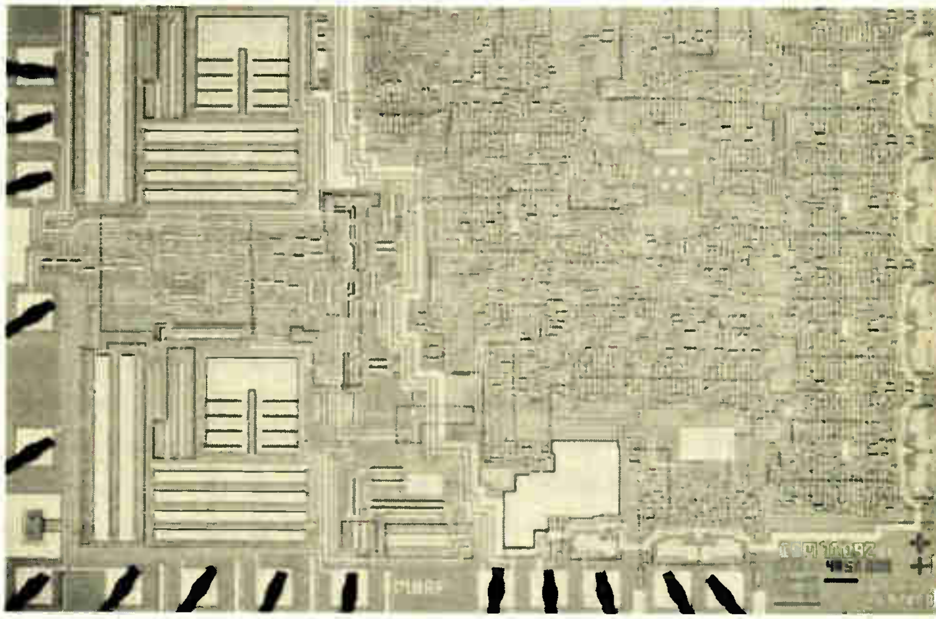
A-d converter likes microprocessors

C-MOS device has three-state output, UART control logic, an on-chip reference, and a 100-piece price of $10

In launching its latest 12-bit analog-to-digital converter, Intersil notes that the ICL7109 is the first 12-bit, single-chip a-d converter specifically oriented toward a wide variety of microprocessor data-logging applications.

Though chock full of features, what makes the 7109 significant is its three-state output, which allows it to be interfaced directly with microprocessor data buses that are 8 bits wide or wider. And for remote data-transmission applications, the 7109's handshaking capability means it can be directly interfaced with universal asynchronous receiver/transmitters.

"The 7109 will sequence through two 8-bit bytes either synchronously or on demand from the microprocessor to the UART," explains Roger Fuller, applications engineer, "and no additional components are needed because the device has on-board logic to control the UART." Therefore, if a designer is logging temperature, pressure, humidity, light intensity, or any other real analog variable, Intersil believes that the 7109 provides a one-chip solution, straight to the data bus.



Not only does the unit save money by eliminating the need for other components, but its own price is low, too, notes Skip Osgood, data-acquisition products manager. The 7109 costs only $10 in lots of 100 or more—about half the price of its nearest competitor, he states.

Other features of the complementary-metal-oxide-semiconductor device include true differential input for noise rejection, a zero drift of less than 1 μV/°C, nonlinearity of less than 0.01%, an input impedance of 1 TΩ, and a conversion rate of 0.1 to 15 conversions per second. And, since it is a C-MOS device, power consumption is less than 10 mW. Also of note is the fact that it employs dual-slope integration.

When in the byte-organized parallel mode, the 7109 can interface directly with the data buses of such popular microprocessors as Intel's 8080 and 8048, Motorola's MC6800, and Intersil's own 6100. There are 14 data output lines, providing 12 bits of magnitude plus polarity and out-of-range bits. These output lines can be grouped in two 8-bit bytes, each of which is activated by its own byte-enable signal. In the handshaking mode, the 7109 has two inputs so that it can sequence through two bytes either synchronously or on demand without the use of external components.

For the analog section, Intersil was able to use the experience gained from the popular 7106/7107 3½-digit a-d converter to produce tight specifications. Among them are a true polarity at zero for precise null detection and a typical input current of 1 pA. The true differential input helps keep the noise level below 15 μV peak to peak and is useful when it comes to measuring the output of load cells, strain gages, and other bridge-type transducers.

Although the 7109, like the 7106, has its own voltage reference, Fuller says Intersil will advise its customers that it is better to use an external reference. The only external circuitry needed is the "usual RC network" and a crystal for the oscillator, he says. The 122-by-135-mil chip comes in a 40-pin package of either plastic or ceramic and will be available in late September.

Intersil Inc., 10710 N. Tantau Ave., Cupertino, Calif. 95014 [339]

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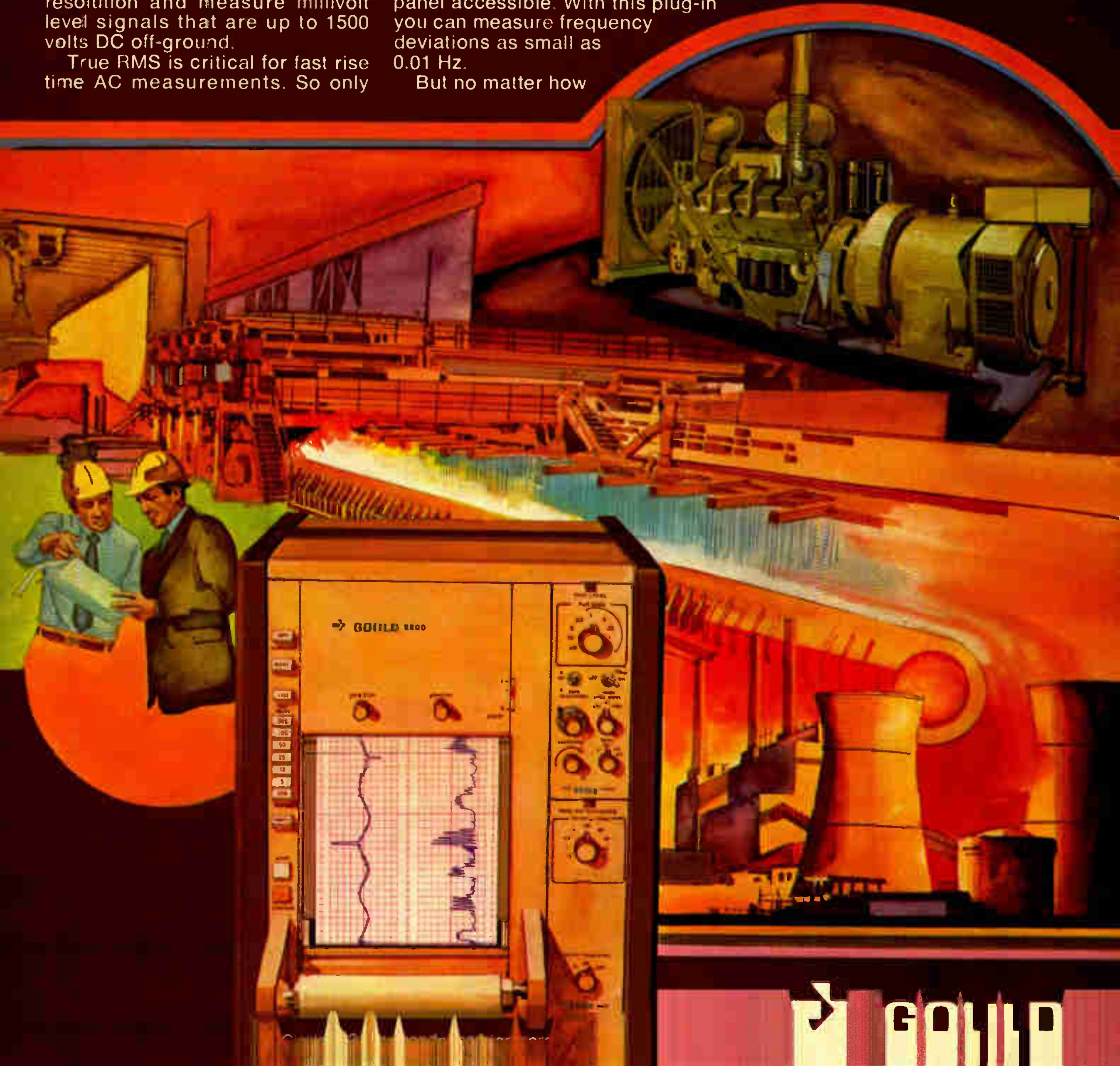
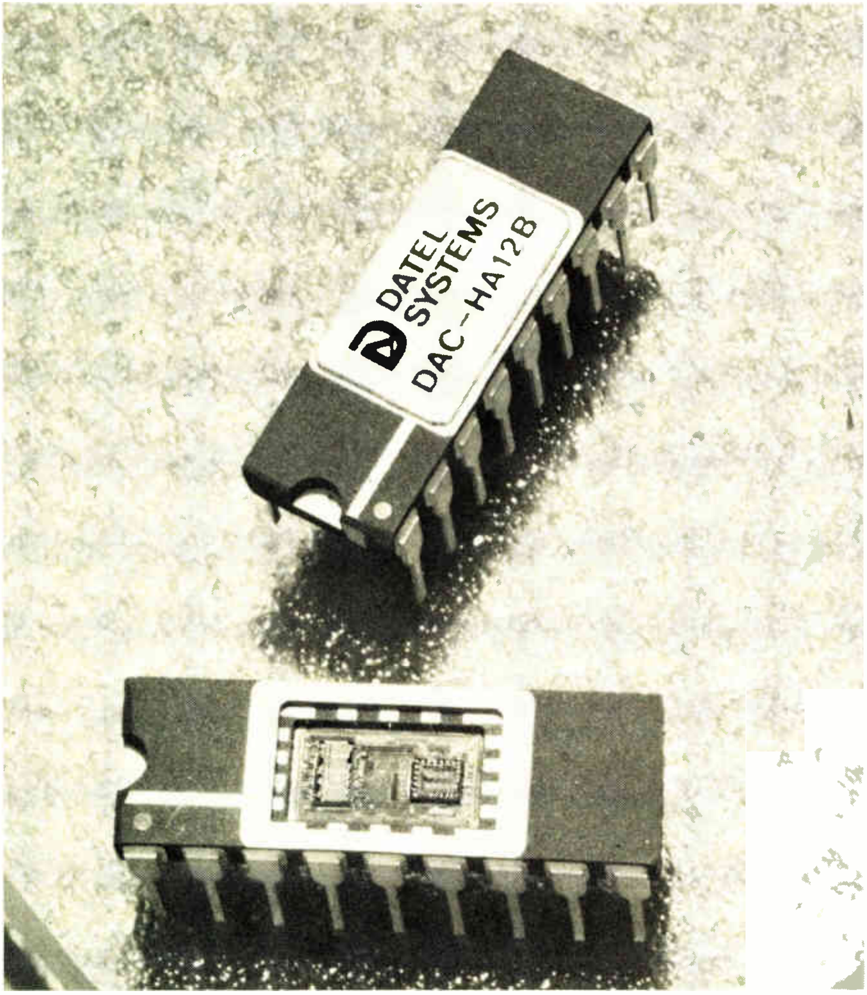


Data acquisition

D-a converter spans 20 MHz

Hybrid unit comes in both binary and BCD versions with power-supply option

A bandwidth that stretches all the way to 20 MHz is only one aspect of Datel Systems' latest hybrid multiplying digital-to-analog converter that should prove intriguing to system designers. They will also like the 12-bit unit's input and power-supply options—different versions accept binary or binary-coded-decimal inputs and run off 5- or 15-v supplies.



The DAC-HA12 uses three chips: two complementary-metal-oxide-semiconductor switches and an R-2R ladder network. Key to its large bandwidth capability is low internal capacitance, achieved mainly by precise laser trimming of the ladder network.

"By using a hybrid," observes Eugene Zuch, product marketing manager, "we have much tighter control over the resistance in the network than with monolithics. We also get a much tighter spec on input resistance." Whereas most similar units have input resistances that can vary by as much as 100%, the DAC-HA12's input resistance is 10 kΩ ±30%. To get the binary and BCD versions, the networks are trimmed differently.

It is the treatment of resistance that also accounts for the unit's low temperature coefficients and nonlinearities. "The resistors are put on one glass substrate and track one another very closely," Zuch observes. The maximum and typical gain temperature coefficients are 5 ppm/°C and 2 ppm/°C, respectively. Differential nonlinearity is within ±¼ least significant bit typically and ±½ LSB maximally. For a full-scale change in digital input, the output current settles to within ½ LSB in a maximum of 5μs. Unlike other multiplying d-a converters that offer users a single power-supply range (typically 5 to 15 v), the DAC-HA12 is offered in both a standard 5-v supply model and an optional 15-v model. Wayne E. Marshall, senior project engineer, explains that, "with a single option, if the device is run down to 5 v, the C-MOS channel resistance almost doubles. That can throw off calibration, increase the temperature coefficient, and ruin linearity." Ranges for the 5- and 15-v supplies are 3 to 7.5 v and 7.5 to 20 v, respectively. A current-limiting resistor in the supply circuitry prevents the unit from drawing too much power.

The DAC-HA12 comes in an 18-pin dual in-line package and three temperature ranges: commercial, industrial, and military. In those ranges, quantities of 1 to 24 are priced at $52, $73, and $104 each, respectively. Delivery is within four weeks.

Datel Systems Inc., 1020 Turnpike St., Canton, Mass. 02021. Phone Eugene Murphy at (617) 828-8000 [371]

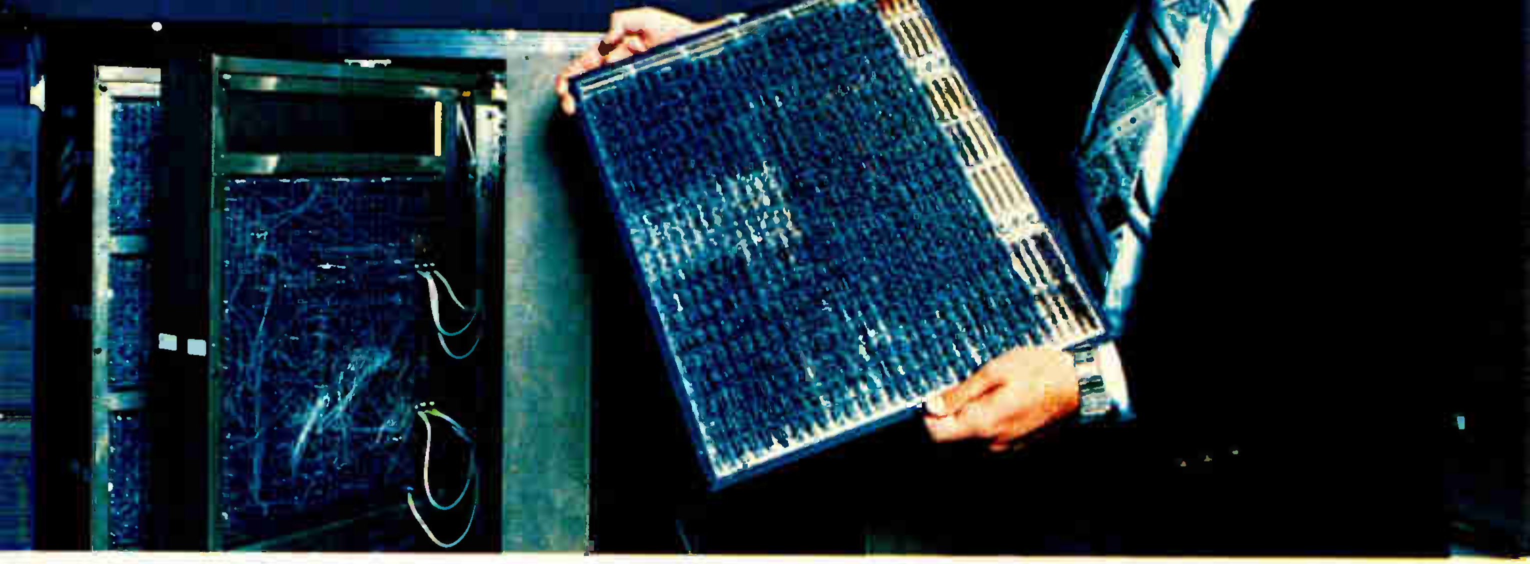
Data-logging meter measures temperature, too

Sometimes a 4½-digit multimeter is not just a 4½-digit multimeter. The 3467A, for instance, includes an automatic scanner for its four channels, a thermal printer that can record readings at selectable intervals, and the capability of mathematically manipulating data as it is acquired. Thus, according to Hewlett-Packard, it is a logging multimeter.

Like other autoranging multime-

"AUGAT PANELS CUT OUR DEVELOPMENT TIME FROM YEARS TO MONTHS."

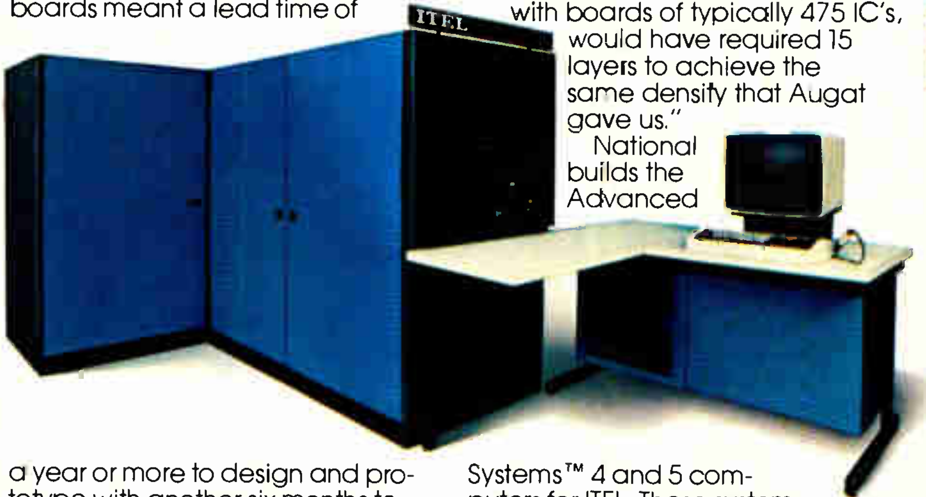
Bob Spencer, General Manager Exsysco,
Large Computer Division of National Semiconductor



The dynamics of the computer industry demands that manufacturers capitalize on opportunities during the limited lifespan of the "current" technology. That's why initial development time is crucial. One sure way to cut that time is with Augat Wire-Wrap* panels. Bob Spencer explains: "Multi-layer boards meant a lead time of a year or more to design and prototype with another six months to get into production. With Augat boards, we reduced this cycle to a few months and started production the day we approved the prototype. Augat also gave us a flexibility to make circuit changes during the development cycle without causing delays."

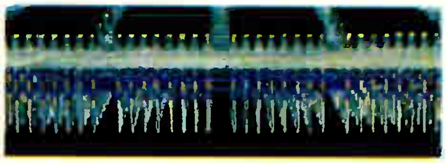
Time isn't the only consideration—cost is also critical. "The expense to design and develop dozens of different, large multi-layer boards can easily run into the hundreds of thousands of dollars, not to mention staffing and equipment. The Augat approach drastically reduced these costs allowing us to concentrate our resources on other critical design elements."

Packaging density is also vital in evaluating interconnection alternatives. "The multi-layer approach, with boards of typically 475 IC's, would have required 15 layers to achieve the same density that Augat gave us."



National builds the Advanced Systems™ 4 and 5 computers for ITEL. These systems must offer high reliability. "As the temperature inside a computer goes up, the reliability goes down. Augat boards reduce the temperature problem because Wire-Wrap pins are excellent radiators."

The benefits also carry into the field. "Thanks to Augat boards, service engineers can make any required changes using simple tools. And because the boards are designed with sockets, we make repairs or upgrade systems quickly by pulling the old chips and plugging in new ones. We also eliminated the cost and logistics of stocking hundreds of different, completed PC boards. Now we simply stock IC's."



How would Bob Spencer rate the performance of Augat Wire-Wrap panels? "Excellent! Our system uses high speed ECL throughout. Augat's patented logic panel, combined with unique automatic wiring from Augat's Datatex subsidiary, performs with no noise or transmission problems."

Throughout the computer industry, you'll find Augat boards at work in all kinds of logic applications delivering high speed performance and system flexibility at dramatic cost and time savings.

For further information, call Len Doucet at 617-222-2202. Or write Augat, Inc., 33 Perry Avenue, Attleboro, Massachusetts 02703.

*Registered Trademark Gardner-Denver Company

AUGAT®

Augat interconnection products, Isotronics microcircuit packaging, and Alco subminiature switches.

Circle 133 on reader service card

New products

ters, the 3467A can measure resistance from 200 Ω to 20 MΩ, dc voltage from 20 mv to 350 v, and true-rms ac voltage from 200 mv to 250 v. But unlike most other DMMs, it can also make temperature read-

ings directly in degrees Celsius or Fahrenheit by using a thermistor of specified type whose measurements the instrument linearizes.

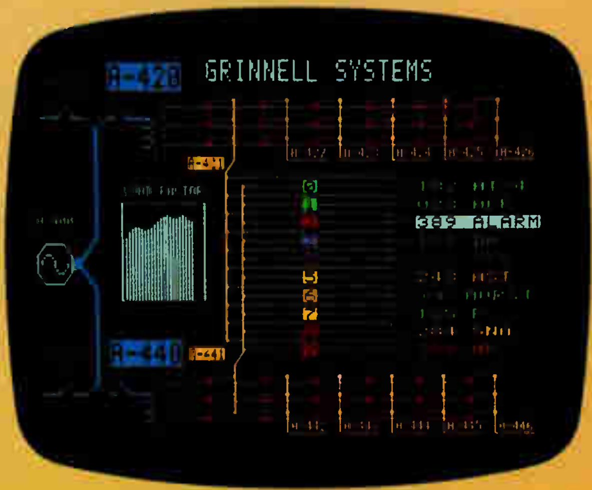
The 3467A also has a diode-testing mode in which it supplies a 1mA constant current to forward-bias diodes without damaging them.

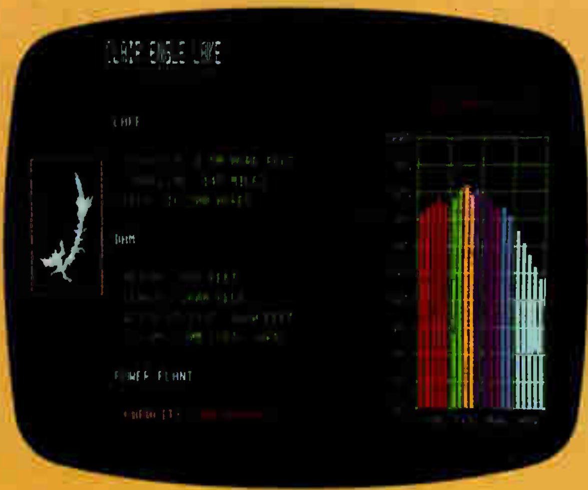
Channels 1, 2, and 3 of the unit are designated X and channel 4 is designated Y. Any or all of the channels can, at one time, make readings in one of the four measurement parameters; if temperature is selected, however, channels 3 and 4 can also be set at the same time to read either voltage or resistance.

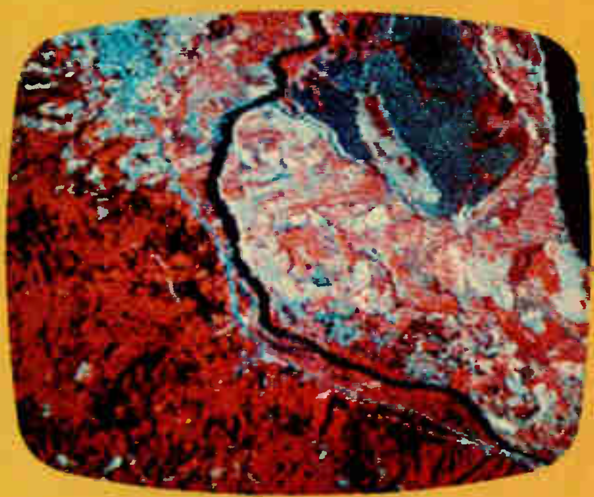
Selecting one of the five math functions—difference, percentage difference, multiplication, division, or decibels—causes the X-channel readings to be mathematically adjusted by the Y-channel value, which may be an actual input or a manually entered constant. In the temperature-plus-other-function mode, the math-function selection affects channel 3 only.

Data logging and channel scanning can be accomplished either manually or automatically; in the automatic mode, unattended readings can be taken and printed out for a maximum of 24 hours. Readings can be made at any one of 32 discrete intervals from 1 second to 3 hours, depending upon the time needed for measurement and the

GRINNELL DISPLAYS:







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GRINNELL SYSTEMS

2986 Scott Boulevard, Santa Clara, California 95050 (408) 988-2100

Circle 135 on reader service card

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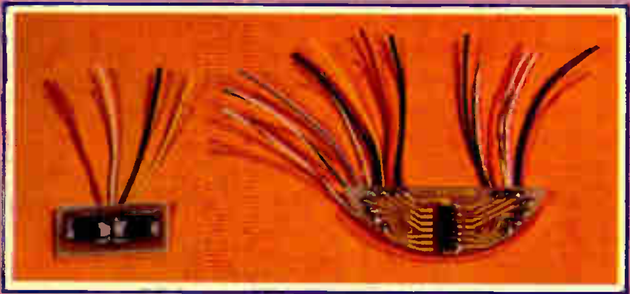
(A)



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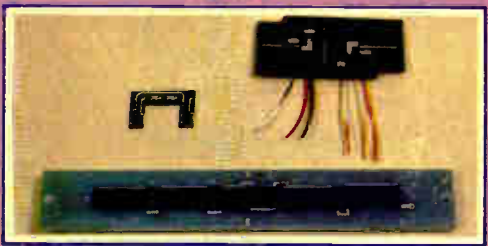

(E)

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Circle 136 on reader service card

user's desired sampling rate.

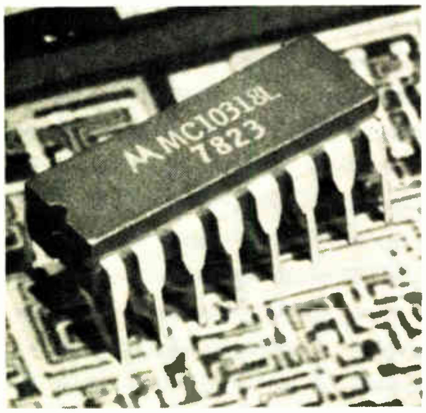
The 3467A is priced at $2,200. Delivery starts this month.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [373]

8-bit d-a converter has fast settling time

The MC10318 is an 8-bit digital-to-analog converter that has a settling time of just 10 ns. Accurate to within ±½ least significant bit and monotonic over a 0°-to-70°C range, the unit can operate in systems with data rates higher than 25 MHz.

Inputs are compatible with emitter-coupled logic for direct interfacing with high-speed processing systems. Operating from a −5.2-V supply, the d-a converter's complementary outputs can produce 51 mA full scale over a compliance range of −1.3 to 2.5 V, and dissipation is typically less than 500 mW. Maximum nonlinearity is ±0.19% of full scale.



With its rapid settling time, the device should find its way into high-speed instruments, digital displays, and storage oscilloscopes, as well as being used in radar processing and television broadcast applications. It comes in a 16-pin ceramic dual in-line package, is available from stock, and is priced at $26 in quantities of 100 and up.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 244-6900 [374]

Components

Crystal unit can be triggered

100-MHz clock generator synchronizes in 55 ns; has 100-ps maximum jitter

The Zepher C-1000, a triggerable clock-pulse generator, provides a solution to the most critical problem in frequency measurement—phasing of the time base. It repeatedly produces a 100-MHz coherent reference signal when triggered by random inputs at rates of up to 20 MHz or more. Maximum jitter between an external trigger and the first clock pulse is ±100 ps.

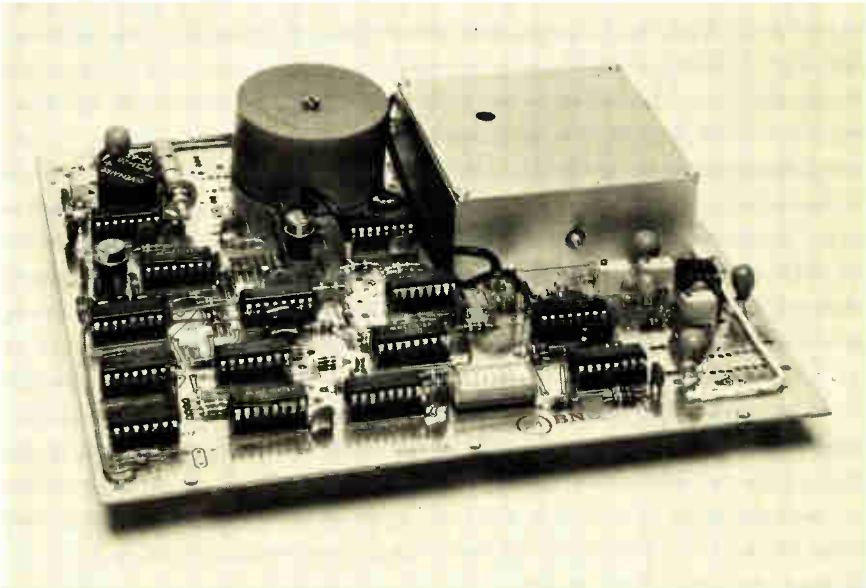
The unit is based on a clock-to-trigger locking scheme that employs two oscillators, one to maintain accuracy over an extended time period and the other to establish precise coherence with the random pulse. The first, a crystal-controlled oscillator with good long-term stability, is coupled to the second, a voltage-controlled oscillator that produces the 100-MHz output. The VCO can be stopped and restarted as well as phase-locked to the crystal-controlled oscillator.

After an input trigger with a minimum pulse width of 10 ns arrives, the VCO is stopped for about 30 ns and restarted 55 ns after trigger arrival, so that the output is synchronized with respect to the trigger. Within 1 μs of this initial synchronization, the accuracy and phase of the VCO's output is compared with that of the crystal oscillator. Any phase difference between the two oscillators is maintained until a succeeding trigger changes it.

In addition to the main 100-MHz output, the C-1000 provides two other signals: a 28-ns wide pulse that occurs 12 ns after triggering and a 12-ns wide pulse that starts 38 ns after triggering. These can be used for auxiliary synchronizing, triggering, or reference purposes.

The unit's frequency instability due to aging is within ±0.2 ppm per week; within the 0°-to-50°C range, instability due to temperature variation is less than 1 ppm. As supplied, the C-1000 is input- and output-compatible with emitter-coupled-logic circuitry and is triggered by the positive slope of the random pulse. But, with minor circuit adjustments, the input can be transistor-transistor-logic–compatible and triggering can be initiated by negative slope.

Logical applications for the Zepher include real-time signal processing, radar, radio navigation, automatic test equipment—in short,



any system that requires rapid synchronization of time base to unpredictable events. For applications that demand greater stability, an optional circuit board is available that allows the C-1000 to be phase-locked to an ultra-stable 1- or 10-MHz external source.

The clock generator requires ±5-v and ±12-v supplies. Priced at $990, it is deliverable in 45 days.

Berkeley Nucleonics Corp., 1198 Tenth St., Berkeley, Calif. 94710. Phone Ed Buchs at (415) 527-1121 [341]

Precision operational amplifier is no drain on system

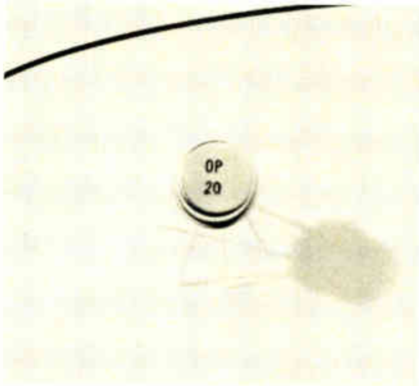
The many different characteristics and uses of operational amplifiers make working with them intriguing and challenging. But despite all the differences, most designers would agree that the one thing they do not want in an operational amplifier is large power consumption. And the thing that they do want most is precision.

The OP-20 fulfills those desires. The monolithic operational amplifier operates at power-consumption levels as low as 175 μW. Offset voltage, thanks to zener zapping, is typically 100 μV, and the input-offset-voltage temperature coefficient is only 1 μV/°C. Input bias current is typically 15 nA.

The device offers an open-loop gain of over 10^6 and can deliver an output current of 1 mA. Common-mode rejection ratio and power-supply rejection ratio both are 110 dB. Furthermore, the OP-20 can operate from a single 3-v to 30-v supply or, alternatively, from a ±1.5-v to ±15-v supply.

The unit's low power needs suggest it for use in many applications, for example, battery-powered instrumentation in process control and portable test equipment of all types. Because the common-mode input range includes ground, it can be used with devices having ground-referenced inputs, such as thermocouples and strain gauges.

Prices for the amplifier, available



in either a TO-99 case or in an 8-pin miniature dual in-line package, begin at $2.20 each in quantities of 100 and up, with delivery from stock. The individual 45-by-68-mil chips may also be obtained.

Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, Calif. 95050 [343]

Military isolating cube blocks up to 2,100 V

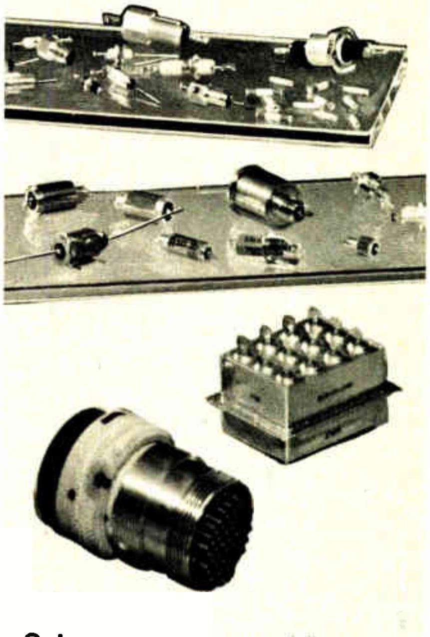
The 801-1 is an optical isolator consisting of a gallium-arsenide light-emitting diode, a silicon photodiode, and a high-gain npn transistor. The 0.37-by-0.37-by-0.23-in. device, called the Iso-cube, provides isolation of 2,100 v dc, or 1,500 v rms. It has a transfer ratio of 140% and a minimum output of 40 v.

The Iso-cube meets the specifications of MIL-S-19500 and comes in a hermetically sealed package. For 1,000 units or more, the 801-1 is priced at $12.80 apiece.

Teledyne Relays, 3155 W. El Segundo Blvd., Hawthorne, Calif. 90250. Phone (213) 679-2205 [347]

Trimmer lets user turn it around

The Type D cermet trimmer can face any way the designer wants on a printed-circuit board. The ⅜-in.-diameter single-turn unit has eight terminal options and a resistance range from 10 Ω to 2.5 MΩ. It is rated at 0.5 w at 70°C.



Circle 139 on reader service card

New products

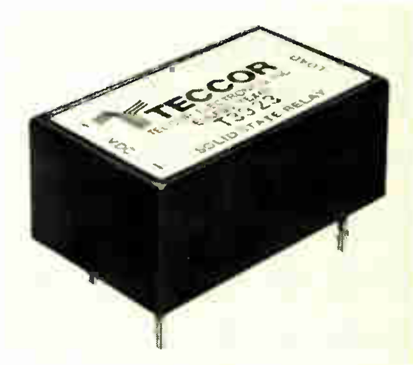
From 500 Ω to 2.5 MΩ, the trimmer offers a temperature coefficient of resistance of less than 35 ppm/°C typically. In quantities of 1,000 or more, individual units are priced at 42 cents. They are available from distributors' stock.

Allen-Bradley Co., Electronics Division Marketing Dept., 1201 S. Second St., Milwaukee, Wis. 53204 [346]

Small solid-state relay wrestles big currents

The 3000 series printed-circuit-board zero-crossing relay, which will be featured at its manufacturer's Wescon exhibit, is an optically coupled device measuring 0.55 in.^{3} Yet it is rated at 3 A for a free-air ambient temperature of 55°C without heat sink.

Both 120- and 240-V ac units are



available, with prices ranging from $4.50 to $7.65 each for orders of 100 to 999.

Teccor Electronics Inc., 1101 Pamela Dr., P. O. Box 669, Euless, Texas 76039. Phone (817) 267-2601 [348]

Circle 141 on reader service card

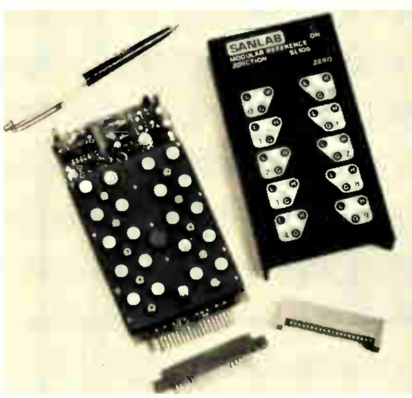
psi and within 1.25% up to 5,000 psi. Resolution is 0.3% of full scale, and temperature effects are less than 0.01%/°F from −65° to 275°F.

Environmentally, the unit can withstand a maximum sinusoidal vibration of 35 g at 2,000 Hz, a steady-state acceleration of 100 g along any axis, and a shock of 100 g for 11 ms along any axis. Prices for the unit, which weighs less than 3 oz without fittings, begin at $578.10 in single quantities.

Gulton Industries Inc., S-C Division, 1644 Whittier Ave., Cosa Mesa, Calif. 92627. Phone Tony Trafford at (714) 642-2400 [353]

10-channel junction has precise silicon reference

As experienced designers have learned, good thermocouple thermometry requires an accurate, highly linear, stable thermometer bonded to a carefully designed thermal shunt. The SL101 is an isothermal 10-channel junction that employs an aged silicon sensor, adjusted and sealed at the factory, to provide junction-temperature data. With compensation coefficients supplied



by the manufacturer and any of various data-acquisition modules currently available, a computer can accurately read and compensate for thermocouples of any type or mix.

The reference circuitry's output is 1 mV/°C, accurate to within ±1% and stable to within ±0.1% per year. Its zero point can be set by the user. The unit accepts shielded wires as large as AWG 14 and provides internal isothermal transition to copper conductors. Users may choose either ribbon or solder-eye edge connectors.

The 6.10-by-3.14-by-1.12-in. junction is priced at $195 each in quantities of three.

San Diego Instrument Laboratory, 7969 Engineer Rd., San Diego, Calif. 92111. Phone (714) 292-0646 [354]

Proximity switch ignores very large fields

Designed so that it may be used with ac input modules of programmable controllers, the completely encapsulated 9853 is a solid-state proximity switch immune to fields such as those generated by the 20,000-A secondary winding of transformers used in resistance welding guns.

With a mild-steel target measuring 25 by 25 by 2mm, the unit has a sensing range of 14 mm ±10%. Coupled with its 3.5-by-1.3-by-1.3-in. size, this range suggests the unit for use as a replacement for conventional limit switches in a wide variety of applications.

Input voltage is 115 V +10%, −15% at 50 to 60 Hz; its output rating is 40 VA at 115 V. The switch may be ordered with either a three-wire connector or an integral two-wire cable with an opening to accept ½-in. conduit. Priced at $60 singly, it is available from stock.

Industrial Solid-State Controls Inc., 435 W. Philadelphia St., P. O. Box 934, York, Pa. 17405. Phone (717) 848-1151 [355]

Microcomputers & systems

Development tool is a computer

Designed for the 8080 family, unit features software that lets tyro write programs

Is it a microprocessor development system with the personality of a small-business computer or a microcomputer with development system capabilities? "It's both," National Semiconductor Corp. says of Starplex, its major new product for the upcoming Wescon/78.

Designed primarily as a development system for an 8080A microprocessor or 8080-based single-board computer, Starplex has other general-purpose features that National's microcomputer systems group hopes will attract a share of the $500 million small-business computer market, too.

Aimed at sharply cutting hardware and software development time, Starplex can be used by novice programmers as well as veterans, according to John Jones, series 80 product line manager. Special-function keys help beginners develop code quickly, but experienced operators can use standard keyboard entry, if they prefer. Prompts and error messages are in plain English to further reduce frustrations for first-time users.

Editing, which Jones claims is usually the most time-consuming development task, got special attention from the Starplex design team. "Depressing the edit key initiates the Starplex editor, displaying a menu into which the programmer enters the file name and other editor control," Jones explains. All editing functions are carried out using a single keystroke, and the system manages the mass-storage file.

The system is built from three board-level computer products, each containing an INS8080A microprocessor. The central processing unit is based on the BLC 80/20, the cathode-ray-tube–keyboard controller on the BLC 8229, and the floppy-disk controller on the BLC 8221. The three microprocessor-based boards and the 64-kilobyte random-access-memory board all are attached to the central BLC system bus.

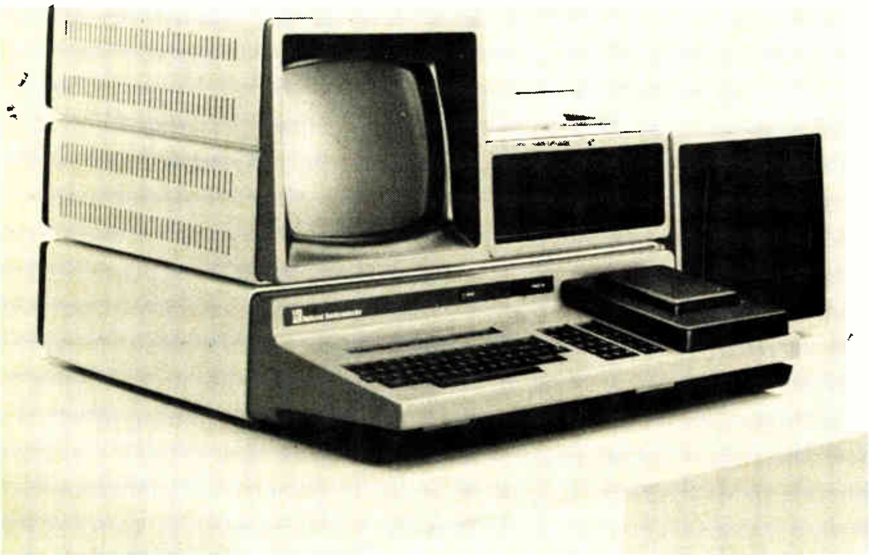
One immediate advantage of this triple-microprocessor scheme is that it lessens the overhead task load on the CPU. Another is that it provides direct-memory-access capabilities for both the CRT and the disk controllers. The 80-character-by-24-line CRT and the 94-key keyboard are linked by ports to the 8229. The dual floppy-disk drive, with its 512-kilobyte capacity, is similarly linked to the 8221.

The BLC 80/20 CPU has an RS-232-C serial communications port and also interfaces with a 50-character-per-second thermal printer. The entire system is housed within a console that measures 25 by 16 by 26 inches, but the CRT, printer, and disk drives may be removed and placed alongside the keyboard and card cage module.

Starplex, as described, will sell to original-equipment manufacturers in October for $13,800 singly or $8,200 in 100-and-up quantities. A programmable read-only-memory programmer, in-circuit-emulator, and additional floppy-disk drives are available, as are assemblers for Pace and 8060 microprocessors. Jones says that an assembler for the Z80 microprocessor will be offered sometime later.

National will market all Starplex systems through original-equipment manufacturers and will not undertake end-user sales or servicing. The reason, according to Jones, is that the potential market includes service organizations, manufacturing plants, hospitals, retail stores, and the like, which National does not have the resources to service.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051 [381]



Converter board brings microprocessor to reality

The M6800 Exorciser microcomputer system can be made to control the real world for only $560—the price of the model ST-6800DA4A. The product is a four-channel digital-to-analog conversion board that slips directly into the microcomputer's card slot and is completely compatible with its bus.

The board offers 12-bit binary resolution with a maximum nonlinearity of ±½ least significant bit. For a 20-v step output, settling time to within $\pm 1/2$ LSB is 4 μs; full-scale output-voltage ranges of 0 to 5 V, 0 to 10 V, -5 to 5 V, and -10 to 10 V can be provided. Output impedance is 50 mΩ, and the board is capable of delivering a 5-mA output.

The ST-6800DA4A draws 1.2 A from the microcomputer's power bus. Its on-board dc-to-dc converter provides the linear circuits with $\pm$15-V. Delivery is from stock.

Datel Systems Inc., 1020 Turnpike St., Canton, Mass. 02021. Phone Ron Petrelli at (617) 828-8000 [385]

"Have computer, will travel"

For the programmer who doesn't get around enough, there is now a computer that comes packed in a 22-by-14-by-7-in. suitcase. Called the Micral V, the 40-lb unit consists

of an 8080-type central processing unit, 32-K random-access memory expandable to 64-K, 1-K erasable programmable read-only memory, a 480-character alphanumeric display, a keyboard, a minifloppy drive, a 32-character-per-line printer and interface, and a power supply.

Standard software includes an advanced business-oriented Basic language, BAL; an ANSI Fortran IV compiler is available as an option. Also optional is a double-density minifloppy drive. In quantities of 50, Micral V is priced at $6,250, and delivery time is 90 days.

R2E of America, 3406 University Ave., S. E., Minneapolis, Minn. 55414. Phone Ron Larsen at (216) 562-9908 [387]

Exchange rates kill power-supply deal

The dramatic decline of the dollar-to-yen ratio has caused **cancellation of the exclusive buy-resell agreement under which Semiconductor Circuits Inc., Haverhill, Mass., was to have been the sole U. S. distributor of certain models in the TOPS series of power supplies** made by Tohritsu Tsushim Kogyu Co. of Japan [*Electronics*, July 6, p. 153 and July 20, p. 170]. Commenting on the situation, C. Kimball Martin, SCI vice president for sales and marketing, said, "Since neither SCI nor Tohritsu controls international currency valuations, we are deeply frustrated, but angry at no one."

Microcomputer system is aimed at educators

Unlike similar systems, which are intended for use by engineers, **Signetics' Instructor 50 microcomputer learning aid is aimed at students and first-time users.** Included in the $350 price are a user's manual and an introductory course in microcomputers and programming. Built around a 2650 microprocessor, the Instructor 50 contains 512 bytes of random-access memory and a monitor program stored in 2 kilobytes of read-only memory. A built-in cassette interface provides a convenient port for program loading to the RAM. Although primarily designed for educational purposes, according to Joseph E. Doll, product marketing manager, the unit can serve as the kernel of a larger system. It will be available from stock next month from the Sunnyvale, Calif., corporation.

Solar battery prices drop again

Valvo GmbH, Philips' West German components-manufacturing subsidiary, **will slash the price for the Philips BPX47A solar battery for the second time this year, reducing it an additional 25% to about $350** for the 11-W unit. The Hamburg-based firm says that this makes solar-power generation economically viable for such consumer applications as isolated cottages, sailing yachts, and other sites located far from conventional sources of electricity.

Intellec II package supports Z80A

Relational Memory Systems Inc., San Jose, Calif., the firm that offers users of the Intel MDS 800 a Z80 development capability [*Electronics*, April 27, p. 183], now **offers users of the Intellec series II a support package that includes Z80 SPICE (Super ICE)—an in-circuit-emulation adjunct for the high-speed Z80A microprocessor.** The hardware/software package, which sells for $2,950, also has a relocatable macro-assembler that operates with the ISIS II operating system.

Scope inverter doesn't stress CRTs

Unlike most dc-to-ac inverters, which have square-wave outputs, a new inverter power supply from Hewlett-Packard **has an output with the same crest factor as a sine wave—1.4.** Designed to power the 1700 family of oscilloscopes, the new inverter achieves this ratio of peak value to rms value by letting its output go high for 25% of a cycle, go to zero for 25%, go low for 25%, and return to zero for the remaining 25%. Because it makes no sudden swings from the high value to the low one, **it puts less stress on the CRT elements than do inverters with square-wave outputs.** The model 1112A sells for $900.

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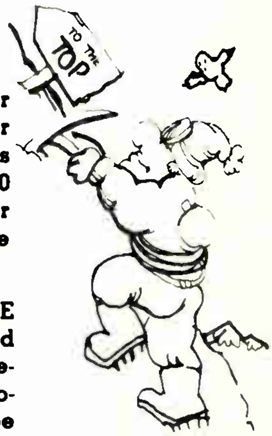

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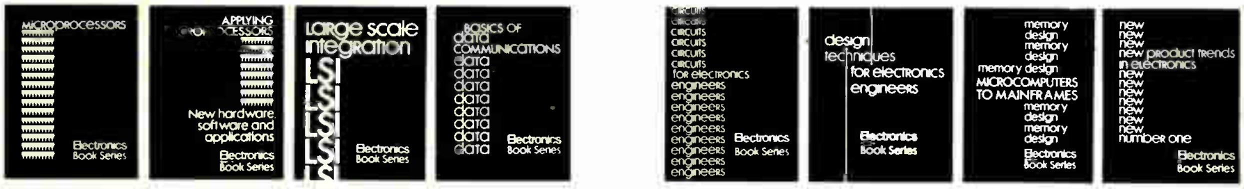

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New, Auto-Insert DIP and SIP Trimmers . . .

And slash your total on-board costs!

Only Bourns delivers both DIP and SIP trimmers for high volume, auto-insertion applications. Machine insertion reduces your production costs and increases productivity. Production costs are slashed from as high as 10 cents to as low as 0.3 cents per insertion! Trimmers can be auto-inserted at least 30 times faster than by hand!

Use Your Standard IC Insertion Equipment — If you already have equipment for auto-insertion of DIP — IC's, you can use the same equipment to insert DIP trimmers. Bourns Model 3099 DIP trimmers have identical height and lead spacing as standard IC's. Or, if you need to purchase insertion equipment, the payback can begin at 3,000,000 insertions!

Meet the New SIP Space Saver — Bourns recently introduced the world's first SIP trimmer — the Model 20. Auto- or hand insertable, the Model 20 cermet trimmer saves precious board space with no sacrifice in performance. Featuring .100-inch spacing and a low board profile of .185-inches, it occupies only 50% of the space used by conventional ¾-inch rectangular trimmers.

Both DIP's and SIP's feature stable, infinite resolution cermet elements with a low temperature coefficient of 100 ppm/°C. They are sealed to withstand industrial cleaning processes and are available in 18 standard resistance values ranging from 10 ohms to 5 megohms.

Backed by the Bourns reputation for leadership, performance and quality at cost-effective prices, Bourns DIP and SIP trimmers can slash total on-board costs and increase productivity. Call or write today for information on the Bourns family of auto-insertable trimmers.

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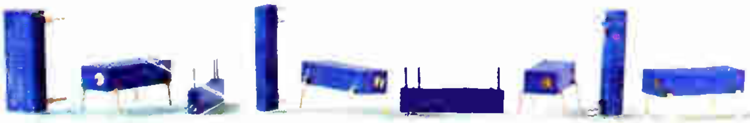

For Immediate Application—Circle 120 For Future Application—Circle 220