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Sundial courtesy of Frank's Antique Clock Shop, San Jose, California.

The World's First LED Displays You Can View in Bright Sunlight.

Now available from Hewlett-Packard are displays designed for high ambient conditions. These seven-segment displays optimize the contrast between the digit segments and the background. A specially designed P-N junction and larger top contact metallization permit operation at high peak currents. This feature enhances display light output and permits strobed operation of long display strings. Combined with proper filtering these displays can be used under high ambient lighting as bright as 10,000 footcandles!!!

Available in High Efficiency Red and Yellow, the HDSP-3530/4030 series are designed for use in outdoor terminals, gas pumps, airplane cockpits, instruments, weighing scales, agricultural instrumentation and point-of-sale terminals.

The High Efficiency Red (HDSP-3530/3730 Series) displays are priced at $2.05* (7.6mm/0.3") and the Yellow (HDSP-4030/4130 Series) displays are $2.25* (10.9mm/0.43") in quantities of 1000.

For immediate delivery, call any franchised HP distributor. In the U.S. contact Hall-Mark, Hamilton/Avnet, Pioneer-Standard, Schweber, Wilshire or the Wyle Distribution Group (Liberty-Elmar). In Canada, call Hamilton/Avnet or Zentronics, Ltd.

*U.S. Domestic Prices Only.

01803

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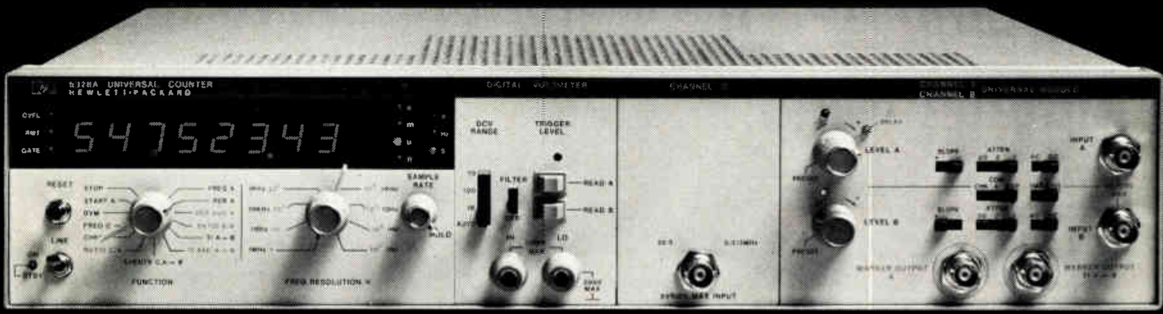
HP 5328A Universal Counter. The Right Performance At The Right Price.



If you're looking for a medium priced universal counter with the capability to do just about any counting job and the versatility demanded by tough systems applications, look no further.

For only $1300* the HP 5328A Universal Counter is a basic 100 MHz/100ns instrument that expands to meet your needs. Optional modules let you expand its capabilities to 512 or 1300 MHz and 10 ns time interval.

You can select an optional built-in DVM (single-ended or full floating, 10 μv to 1000v) for accurate determination of trigger levels and for external digital voltage measurements. Only HP offers it.

Other options let you make use of an ultra-stable time base and HP Interface Bus Operation including full remote control of the counter and the DVM.

Sound good?

There's more information available for you on the HP 5328A Universal Counter and the full line of sophisticated HP electronic counters.

Just call your nearby HP field office or write for our new electronic counter brochure.

*U.S. Domestic price only.

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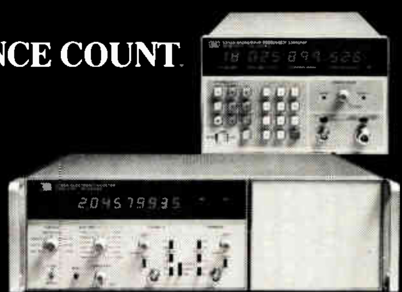
HP: MAKING EXPERIENCE COUNT.



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Circle 2 on reader service card

Electronics

The International Magazine of Electronics Technology

Vol. 51, No. 7 • March 30, 1978

Highlights

Cover: Measuring time and frequency, 82
The accurate measurement of time and frequency is a basic engineering tool. Using new technology, today's sophisticated counter-timers, oscilloscopes, and spectrum analyzers produce faster, more precise data than ever before. But there are pitfalls. Part 1 of this new series tells how to make accurate measurements with digital counters and timers (p. 84).

Cover by Art Director Fred Sklenar.

Government actions damage trade, says AEA, 76
The Administration's proposal to end deferral of U. S. taxes on income earned abroad ultimately harms the trade balance, argued Edwin Zschau of the American Electronics Association (formerly WEMA) before a Congressional committee this month. And high capital gains taxes are scaring vital venture capital away from high-technology companies, he added.

Here come the big, new 64-K ROMs, 94
The latest generation of read-only memories uses assorted technologies, varied pinouts, and are sometimes dynamic instead of static. Designers from three companies describe why and how they optimized their devices for speed (p. 96), density (p. 99), or for compatibility with other chips, especially microprocessors (p. 104).

And in the next issue . . .
Preview of the Electronic Components Conference . . . a special report on magnetic-bubble and charge-coupled memories . . . a high-performance monolithic analog-to-digital converter . . . software on silicon: the implications of large ROMs.

Electronics

EDITOR-IN-CHIEF: Kemp Anderson

Publisher's letter

Is the Golden State of California losing some of its glow for electronics firms? That would seem to be the case for some of the West Coast firms, at least when it comes to planning for expansion.

The main problems, described in the Probing the News story starting on page 74, are the high cost of housing for engineers moving to California and heavy taxes, including an inventory levy that, critics say, is particularly hard on small, high-technology companies with shops full of expensive test equipment.

Our West Coast bureau managers, Larry Waller in Los Angeles and Bill Arnold in the San Francisco Bay area, found a number of discontented company executives with more than the usual complaints about taxes and rising costs. Their reports indicate that the headaches are real enough to cause some of these electronics companies to seek new sites for locating plants. As the story points out, it's not exactly an exodus but a new look at where to locate facilities.

Lamenting the conflict many highly industrialized states have faced concerning business taxes, one California state official notes, "Everybody wants to come here for the advantages—weather, educational system, technology pool, and so on, but they want to be taxed like a state that doesn't provide as much."

When is a thousand not a thousand? When the subject is semiconductor memories. When the first 1,024-bit read-only-memory-on-a-chip was called a 1-k device, no one objected, nor was there any difficulty with its 4,096-bit (4-k), 8,192-bit (8-k), or even 16,384-bit (16-k) successors. A conventional engineering roundoff coupled with the convenient binary progression made sense.

But the simple rationalization breaks down now that we're reaching the 65,536-bit level. Most of the industry is talking happily of 64-k devices, discarding 1,536 bits.

But it's offensive to our editors to have a term mean one thing to one group and another to another, so they've come up with a compromise: beginning in this issue, most notably in the special report on big ROMS starting on page 94, K stands for 1,024 and k stands only for 1,000.

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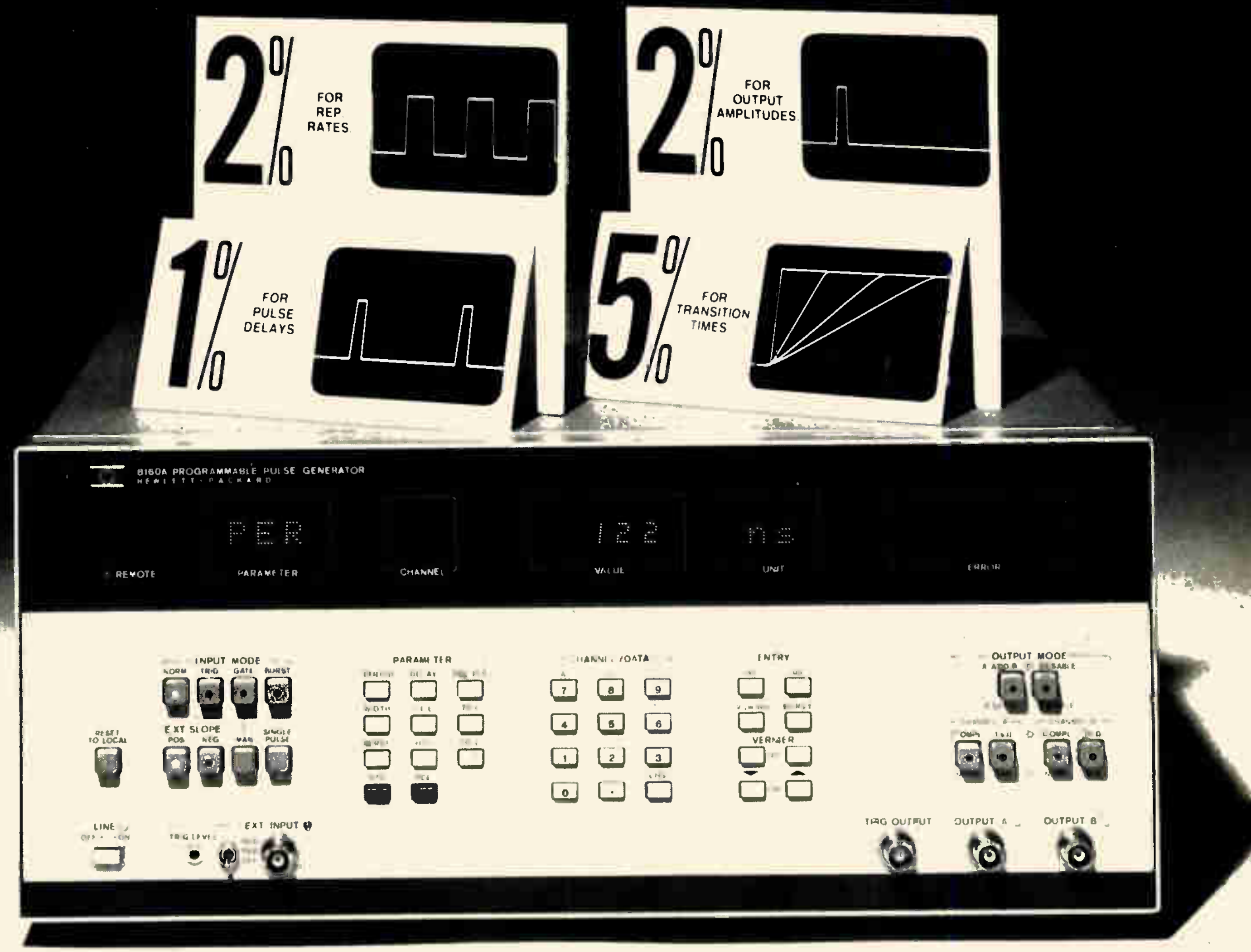
Now microprocessor control lets you quickly program pulse parameters with accuracies of...



HP's new 8160A—the first microprocessor-controlled pulse generator—gives you the versatility, high accuracy and programming capability that's needed for precise control of pulse parameters. Its 50 MHz frequency range with 20V amplitude capability makes the 8160A an ideal solution when you need accurate, consistent pulses for IC qualification, automatic testing or breadboard check out. The 8160A is easy to set up and quick to program too, for greater testing throughput.

In automatic test systems, the 8160A can be controlled by computer or computing controller via the HP-IB*. Programming is easy using the 8160A front-panel mnemonics. Or, the HP-IB "learn mode" can scan and store front-panel settings automatically.

Manually, you set up the 8160A using convenient front-panel push buttons and you can store up to nine complete front-panel setups for quick recall. A vernier lets you change values without time-consuming data reentry. The 8160A even alerts you to incompatible entries.

Add to all of this such features as counted burst, internal/external triggering, synchronous gating and two-channel output option, and you have a versatile pulse generator for a variety of testing needs. One that speeds your setups, delivers high-quality signals for precise testing and boosts your testing throughput—all for $11,000**. (two-channel option is priced at $4,800**).

Contact your local HP field engineer today for complete details of this high-peformance pulse generator.

* HP's implementation of IEEE Standard 488-1975.
** Domestic U.S.A. price only.

088/4

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THE FAMILY.

There's a 256-bit, a 1K, a 2K and a 4K with output latches. Choose open-collector or three-state outputs. All have the same electrical characteristics. All are programmable from the same card set.

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In the family you'll find an Am29774/75, the world's first 512 x 8 registered PROM.

Make room for it. 35% less room. It's a 22-pin part. It's 35% smaller than 24-pin counterparts.

Here's yet a third first: easy pipelined microprogramming. The Am29774/75 has edge-triggered full master/slave registers built right into each output, eliminating an external 20-pin octal register and saving another 20% in board area.

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People

Caution. In Seely's view, no semiconductor house can survive on just one technology.

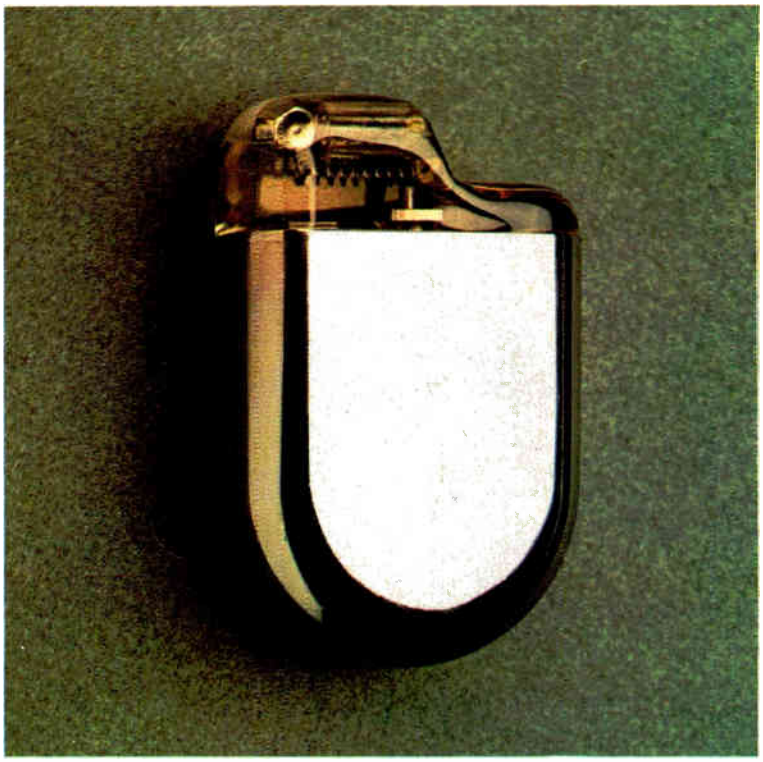
in V-MOS. "It has the edge over everything else in achieving denser chips," he says. Unlike other MOS memories, which have each cell's transistor and storage capacitor on the surface, V-MOS has the storage capacitor underneath and only the transistor on top, and that saves space. "In the world of miniaturization of silicon area, this makes all the difference," Seely says.

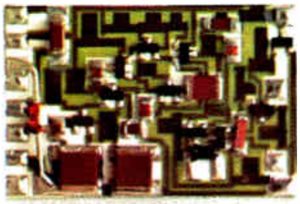
Besides memories already available as samples—two fast 4,096-bit static V-MOS random-access memories (see p. 116)—Seely will launch two other hot V-MOS items for the microcomputer market, an 8-K static RAM and a 16-K erasable programmable read-only memory.

More than one. But, Seely says, "no house can survive as a one-technology supplier, especially one like AMI that does more than half its business on a custom basis." Thus the company, with sales last year of $71 million, will introduce products such as complementary-MOS versions of its 4-K and 8-K static memories and, for the appliance market, a C-MOS version of its proprietary S3000 one-chip microcomputer. Although he declines to give any details, he also alludes to programs under way for "super-high-density C-MOS and n-channel MOS devices."

Seely is also enthusiastic about the telecommunications market [*Electronics*, March 16, p. 46]. "There's a customer at the end of every telephone line that could use some of our devices," he says. "And at the other end, there's the telephone office, so it's a large market at either end."

Instrumenta vitae





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Magneti Marelli is one of the largest producers of electric and electronic systems and has been manufacturing standard or custom made thick-film hybrid circuits for over five years.

Magneti Marelli is happy to allow its customers to take advantage of its complete design capabilities and production facilities at competitive prices.

Magneti Marelli can manufacture hybrid circuits for a wide range of applications including:
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- consumer market
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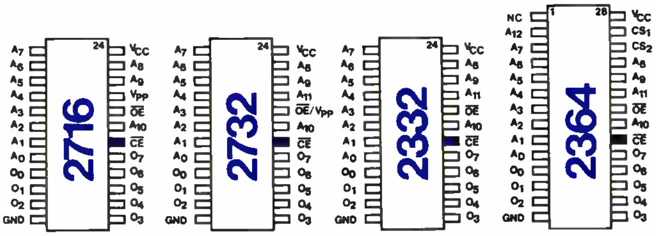
64K ROMs designed computer compatibility.

Second, the 2332 and 2364 are compatible with our 2716 industry-standard 16K EPROM and will be compatible with our 32K EPROM when it is introduced. Again, Pin 18 is the key. Note that Pin 18 performs the same power control function on all devices. So you can prototype with EPROMs and go directly to high density ROMs for production.



	16K EPROM	32K ROM/EPROM	64K ROM
Organization	2Kx8	4Kx8	8Kx8
Active Icc (max)	100 mA	40 mA	40 mA
Standby Icc (max)	25 mA	15 mA	15 mA
Access Time (max)	350-450 ns	300 ns	300 ns

Engineering the 2332 and 2364 for microcomputer system compatibility led us to the third important advance—the end of bus contention problems. In new multiplexed microprocessor systems, such as the MCS-85 and MCS-86, the Output Enable (Pin 20) needs to be independent of the Chip Enable (Pin 18) which is the power control and selection function. So the 2332 and 2364 have an Output Enable ($\overline{OE}$) for independent control of the data bus, with no possibility of multiple device selection. And input latches on all Edge-Enabled devices allow direct interface with new multiplexed microprocessors.

Low power is essential to meet today's design requirements. We've achieved low power in our 32K and 64K ROMs that can't be matched by fully static parts. Active current of the 2332 and 2364 is 40 mA (maximum). And Intel's Edge-Enabled devices have the added benefit of using Pin 18 for the power control function. So standby current is automatically reduced to 15 mA (maximum).

To get complete details on this important and complex subject, send for our 2332/2364 applications note AP-30, "Applications of Intel's 5V EPROM and ROM family for microcomputer systems." It provides board layout recommendations, system design applications, timing diagrams, function explanations and discusses PL/M modular software compatibility. Write: Intel Corporation, Literature Dept., 3065 Bowers Avenue, Santa Clara, CA 95051. Or for samples of these new parts, contact your local Intel representative.

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Circle 19 on reader service card

A North American alliance?

The chairman and chief executive officer of Northern Telecom Ltd., Robert C. Scrivener, has proposed an interesting economic development plan. At a recent talk before the Ontario Economic Council, the communications equipment company executive made a case for Canadian firms to invest in the United States.

In fact, Scrivener practices what he preaches, for Northern Telecom has been active in the U. S. market for some time and has already acquired production facilities in this country. Outlining his reasons, Scrivener states:

"These tendencies [U. S. investment by Canadians] suggest strongly that we start thinking of a North American alliance as the prime position for our national industrial objectives and strategies, and that we in North America start to prepare ourselves for the onset of the international and intercontinental trade battles of the '80s."

He then goes on to identify some of the factors that make Canadian research, production, and marketing involvement in the "lower 48 states" attractive. In general, economic conditions north of the border mirror those in the United States and may in some respects be more burdensome. For example, the high wage levels, high cost of materials, taxes, and government regulation at home all contribute,heavily to Canadian interest in operating abroad, in the United States.

Knowing these facts, the U. S. should not be surprised if Canadian electronics firms take Scrivener's suggestions seriously. Indeed, cooperation among Canadian and U. S. firms, such as that between Northern Telecom and Intersil, could lead to a beneficial North American alliance in electronics technology.

Distributors look to the future

Considering their importance in the proliferation of electronics into new applications and industries, distributors have not received uniform attention from the manufacturers that supply them.

While some companies have developed strong distributor programs emphasizing mutual profits, others have squeezed these middlemen into difficult positions. Therefore, any discussion of the distributor mentality must put part of the responsibility for the cause of its manifestation—high volume with low profits—on suppliers.

It is time to rethink the role of distributors in this industry, a task that must involve both the distributors themselves and the product suppliers. Essentially, the industry needs policies that will be to the advantage of both.

Suppliers need to become more aware that service is as important as volume and that service implies higher costs. Distributors are coming to realize that they stretch themselves too thin financially by trying to carry too many lines each of which has marginal profits.

For example, as distributors are required to purchase microprocessor development systems in order to serve their customers, operating costs have climbed. These costs need to be accounted for, and this means that margins on product lines should increase to compensate the distributors.

If the cost of getting a new line into the marketplace has increased for manufacturers, it has also jumped for distributors. If anything should alter the distributor's strategy of the fast turnover dollar, that fact should.

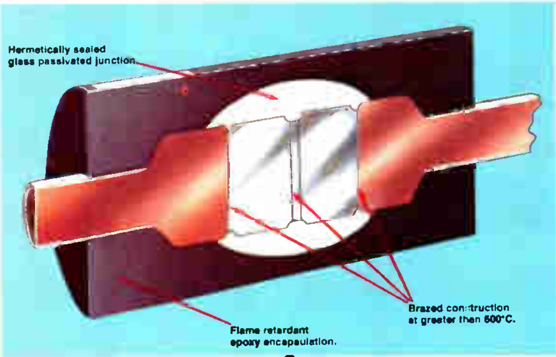
Ford uses General Instrument

...Quality Cars Start with Quality Parts.

At Ford Motor Company, quality is a lot more than something to talk about in TV commercials—it's a *rule* that applies to every aspect of building fine cars and trucks.

So when Ford needs rectifiers, the choice is quality—General Instrument Superectifier.

Not only does Superectifier assure Ford owners of long dependable service, but it eliminates costly failures due to the stresses of automated assembly techniques, *helping Ford to keep costs down*.



It's easy to see why Ford selected Superectifier, just look at its patented construction.

- Metallurgically Bonded, at greater than 600°C, at both the leads and the junction.
- Hermetically Sealed, glass passivated junction.
- Flame Retardant, UL Listed epoxy encapsulation.

Not everyone needs the kind of quality Ford requires, but everyone can afford it—because with Superectifier the premium is on quality not price.

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Don't limit Mostek's new tone dialers and tone receivers to the telephone.

Limit them to your imagination.

Applications for Mostek TONE II™ integrated tone dialers and the new MK 5102 integrated tone receiver are limitless. These two CMOS integrated circuits now create a multitude of possibilities for digital communications and control applications. Previously, these applications were impractical because of system design complexity and the resulting high system cost. But now, with encoding and decoding functions integrated onto single IC's, you can unleash your imagination.

Start with these facts: Mostek tone generators and tone receivers use the economical TV color crystal for reference. Both operate using the world-recognized TOUCH TONE* DTMF system. Both meet or exceed most standards for stability, distortion and timing. Both are microprocessor compatible and are in volume production today.

Additional features of the MK 5102 include 5-Volt ± 10% power requirement latched three-state outputs with data valid strobe, low pre-filtering requirements and superior talk-off protection — all in a 16-pin package. The MK 5087 through MK 5091 TONE II™ dialers provide simple, low-cost solutions for a wide variety of circuit designs ranging from fixed supply to direct phone line applications.

There's more information on Mostek's communications products. Contact Mostek at 1215 West Crosby Road, Carrollton, Texas 75006. Telephone:(214)242-0444. In Europe contact Mostek GmbH, West Germany Telephone: (0711) 701096.

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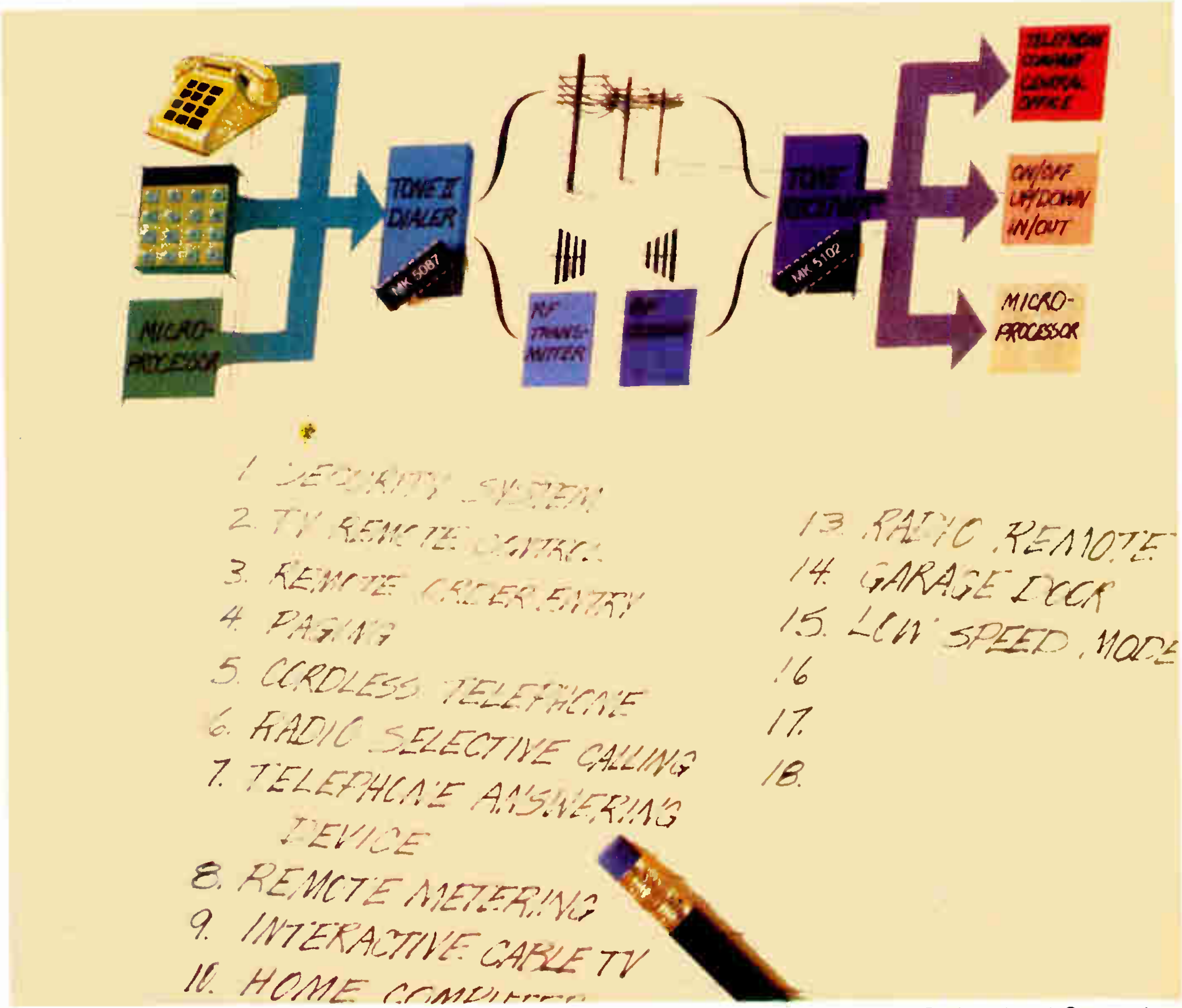

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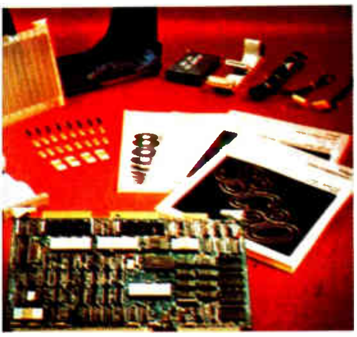

'rototype Systems
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A highly reliable computer is the result of the manufacturer setting rigid quality assurance standards and — more important — meeting those standards at each point in the design and manufacturing cycle... at the wafer level, at the component level, at the board level, and at the system level. The establishment and implementation of high design and quality assurance standards has resulted in an exceptionally high (73,000 hr. MTBF at 25°C for SBC 80/10A) reliability rate.

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Intel maintains the largest staff of Field Applications Engineers in the microcomputer industry. These engineers are available worldwide to help you with your system design and configuration requirements. Regularly scheduled Intel hardware and software training courses and workshops are held throughout the world. The Intel SBC 80 and SYSTEM 80 product line is stocked and supported by an international distribution network.

Circle 169 on reader service card

intel®'s Family of Single Board Computers
The growing requirement for low cost microcomputer systems for OEM and volume end user applications was the motivating factor in Intel's introduction of the first Single Board Computer — the SBC 80/10 — in February 1976. The SBC 80 family has grown rapidly to meet the varied requirements of the marketplace. Four new Single Board Computers and three fully packaged SYSTEM 80 microcomputer systems have been introduced. A large variety of compatible memory boards, digital I/O boards, communications boards, analog I/O boards, mass storage systems, power supplies, system prototyping kits, cardcage and backplane assemblies, and comprehensive documentation have all been added to the expanding product line. The Intel MULTIBUS was developed to tie the entire family together and has evolved as the industry standard bus architecture. The SBC 80 and SYSTEM 80 products are also supported by a growing array of Intel software, including the RMX/80™ Real-Time Multi-Tasking Executive, ISIS-II Operating System, PL/M-80 high-level systems programming language, assemblers, text editors and In-Circuit Emulation debug and diagnostic packages ...all designed to support the modular, efficient requirements of microcomputer systems.

The intel® MULTIBUS
The Intel MULTIBUS was designed to maximize system throughput for SBC 80 based applications. The bus architecture supports multi-master systems (those requiring multiple Single Board Computers, DMA boards, disk controller boards) with serial or parallel priority schemes, eight levels of vectored interrupt, addressing of up to 64 K bytes of memory and 512 8-bit I/O ports. An asynchronous bus clock is provided to allow masters of different speed to share common bus resources. Bus transfers can proceed at rates up to 5-million bytes per second. The MULTIBUS enables multiple processors to work together to share services and give optimized configuration capability, as well as autonomous operation in a system environment.

For more information on Cost Effective Microcomputer Systems, contact:
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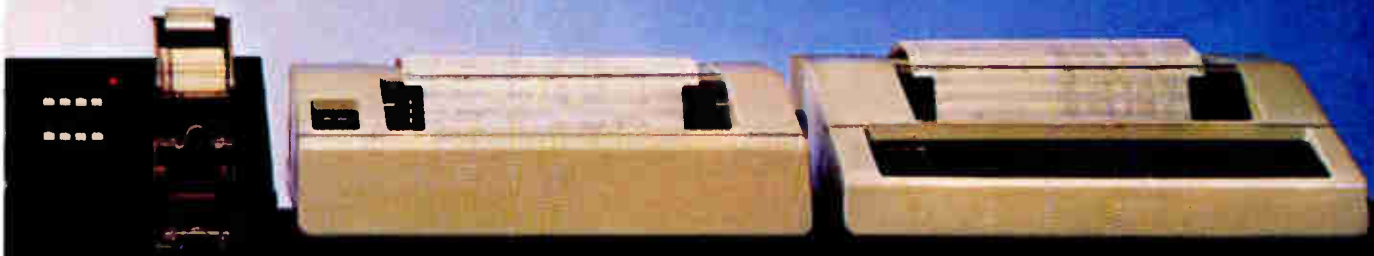

The HP 7260A Optical Mark Reader is a flexible transmission link to your computer. It reads both pencil marked and punched cards, transmits at up to 2400 baud, and with its two RS232C or CCITT V.24 connectors can easily form an integral part of a low-cost RJE station.

We've made hard copy easy with our microprocessor controlled HP 2631A Printer and HP 2635A Printing Terminal. The easy-to-read 7x9 dot matrix meets the 128-character USASCII Standard, allows true underlining and descenders, and prints six-part forms. A long-life drop-in cartridge makes ribbon-changing easy, and the Character Expand/Compress mode gives you three ways to print.

Both the HP 2635A Printing Terminal and the 2631A Printer zip along at 180 cps in both directions. The microprocessor determines the optimum print path. A high-speed slew speeds up printing columnar data, and the long-life, self-aligning print head makes for a quick change. Both have self-test features for quick verification of operational status.

These Hewlett-Packard terminals are compatible with all the major interface standards and work with computers from a range of manufacturers. They come with full HP support, service, training, and documentation.

To find out more about these (and others) in our growing line of terminals, call the HP office listed in the White Pages. Or send us the coupon. If you don't see exactly what you're looking for here, let us know. There are plenty more where these came from.

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Circle 31 on reader service card

Array processor from Data General crunches numbers

The first array processor to be offered by a minicomputer manufacturer will be introduced this week by Data General Corp. The AP/130 will handle complex signal processing in acoustic and radar signal analysis, tomography, seismic data processing, communications, and speech analysis. It takes the Eclipse S130 and adds **floating-point capability to produce the required digital signal at high speeds.** The machine incorporates a 1,024-element, fast-Fourier-transform, complex-number array that can perform operations called butterflies—four multiplications and six additions. It does 5,120 of them on either an ordered pair of 32-bit floating-point data or a 1-K FFT in 8.75 milliseconds—an average of 585,000 butterflies per second on 64-bit data. With the standard Eclipse microcomputer, the AP/130 performs both 32- and 64-bit operations using Fortran V. A typical configuration will sell for just under $60,000 and delivery is 90 days.

Peripheral controller marks Ampex' entry into market

Traditionally a supplier of tape and disk drives to original-equipment manufacturers, Ampex Corp.'s Data Products division will surprise some manufacturers of minicomputer peripheral controllers next week when it introduces its DC-1000 controller at the Mini/Micro '78 Conference on April 18 in Philadelphia.

According to Mike Kirby, senior product manager, the strategy for the new controller ($7,500 in volume quantities) is to gain a greater profit share **by moving closer to the end users with value-added adjuncts to the traditional line of tape and disk drives.** Kirby cites the DC-1000's firmware-resident microdiagnostics as the unit's key feature, but adds that this self-testing and diagnostic routine is only one of the advantages of the custom bit-slice microprocessor architecture. The controller can relieve the host's central processing unit and main memory of most of the tasks involved in disk-processing subroutines. Moreover, the built-in processor permits the DC-1000 to operate in conjunction with up to four disk drives and up to four CPUs.

Tektronix MDS now uploads and downloads

Tektronix Inc. has broadened the appeal of its 8002 universal microprocessor development system with a software feature that helps cut design costs: source data from a host computer can be "downloaded" (moved from computer to terminal) to the 8002 and "uploaded" back to the host computer over standard RS-232-C lines. Among the advantages are that **a central data base can be shared among several Tektronix units** and that separate design teams can interact through a central computer to design a common system. The new program is becoming a standard feature on the $9,950 8002, which supports Intel 8080A and 8085A, Motorola 6800, Texas Instruments TMS9900, and Zilog Z80A microcomputer families.

Intel to announce production codec at Paris show

Signs that the telecommunications market is heating up for chip makers will become stronger when Intel Corp. announces **production availability of its single-chip n-MOS codec** at the Paris components show, April 3–8. Intel's codec converts voice signals into pulse-code-modulated digital signals for switching or transmission on a PCM link and converts the digital signals to voice at the other end. At the show, Intel will display the 2911 A-law version for European companding standards but it also has the 2910

1024 (One Thousand Twentyfour) Instructions with the New Infrared Remote Control System from ITT Semiconductors

We have always considered it essential to apply our worldwide know-how to trend-setting developments.

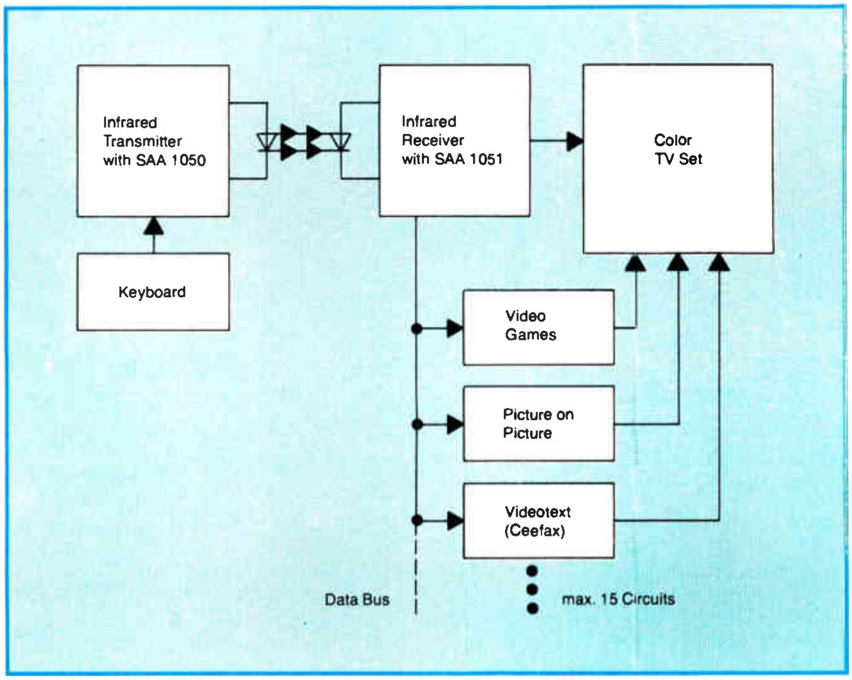
In the early 1970s it was already known that a color TV set could best be adjusted for an optimum picture from only the right viewing distance. The first remote controls using heavy cables appeard on the market. And then came the wireless but expensive and delicate controls.

We found the ideal solution... thanks largely to our expertise gained in developing those now legendary tuning diodes for controlling analog and digital signals in a TV set. (Meanwhile, a diode tuner fitted with our integrated circuit SAA 1021 can be used also for fully electronic channel selection.)

In those days we started looking for new control concepts... and we developed our 30-channel ultrasound remote control system SAA 1024/25, a system that has become the most popular in Europe today and has propelled INTERMETALL, our German based activity, to the top position among European producers of MOS devices for consumer applications. Together with our partners in the TV Industry we have continually expanded our knowledge and refined our technologies so that we can now present our highly flexible and long lived

Infrared Remote Control System SAA 1050/51

Technical Features:
- transmission system for 64 individual instructions, all assignable to 16 different addresses, giving a total of 1024 instructions
- transmitter IC SAA 1050 in CMOS technology
- receiver IC SAA 1051 in silicon-gate P-channel technology, a specialized microprocessor
- signal transmission by pulse-code modulated infrared light
- long transmission distance
- high noise immunity through integrated interference suppression circuit
- long life of transmitter battery
- four operation options for the receiver IC
- only one transmitter for 16 pieces of equipment or addresses



Block Diagram of the new Infrared Remote Control System with the Integrated Circuits SAA 1050 and SAA 1051

The dialogue and cooperation with our customers has borne fruit; our new transmission system is just what the industry wants.

The ongoing know-how exchange with our partners has shown that a revolutionary control system such as ours must also be capable of controlling features in the audio and video field that are still in the early stages of development, for example intelligent TV games, teletext, viewdata, remote programming of high-fidelity equipment, etc.

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Why Are We Any Different?

We're an ultra engineering-oriented company with a strong commitment to product reliability, integral accuracy, stability over time and temperature and innovative solutions to customer problems. And we know, that to really solve your problem it takes more than block diagrams. It takes experience; it takes what you might call a "green-thumb" in data acquisition systems.

Superior Data Acquisition Systems must provide solutions to customer problems, measurement techniques and specific microcomputer requirements and purposes. And that is what Analogic does, provides solutions qualitatively and innovatively over a broad line of products. Maybe that's why Analogic is, by far, the world's largest designer and manufacturer of microcomputer Data Acquisition Systems.

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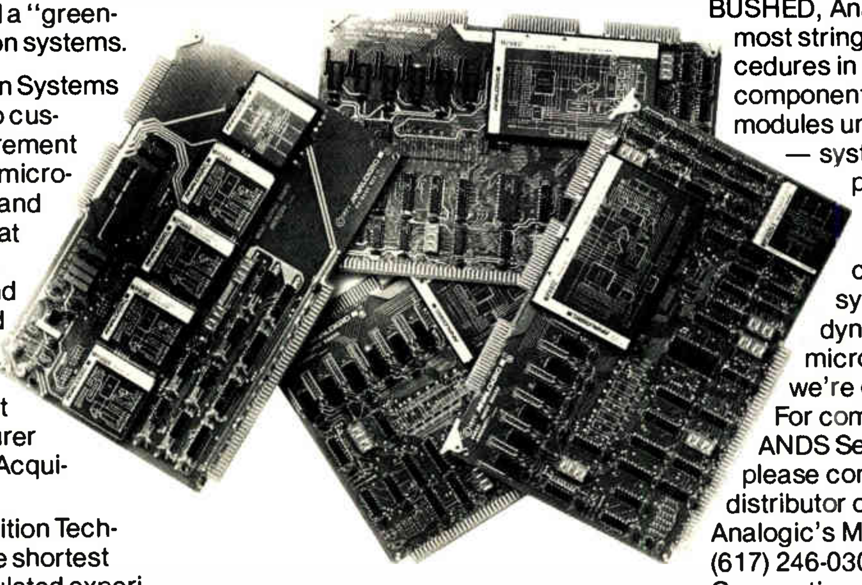

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Circle 37 on reader service card

Gate arrays taking over in logic using ECL

Fairchild and Motorola are applying LSI arrays to extend their families of SSI and MSI standard logic

Emitter-coupled logic, though the fastest semiconductor technology around, has fallen behind other logic forms in the general move to large-scale integration. Designers who needed ECL's all-out speed together with maximum flexibility were forced to choose medium-scale logic families or even discrete parts.

Changing this picture is the introduction of ECL gate arrays—uncommitted sets of LSI functions tailored by the final metalization to particular applications. Two suppliers of ECL logic are taking this new tack: Fairchild Camera and Instrument Corp., with a 250-function standardized array of gates compatible with its three-year-old F100K family, and Motorola Semiconductor, supplying an approximately 700-function ECL gate array compatible with its 10K family. Motorola also supplies the industry's only ECL microcomputer—a 4-bit-slice family of LSI parts called the 10800.

Two features. The new gate arrays, also called uncommitted logic arrays, combine two usually contradictory features: volume production for low cost, and the custom flexibility of accommodating many different functions that discrete and medium-scale logic provide. In consequence, the computer manufacturer may replace 10 to 15 discrete components with one LSI part in such applications as error correction, accumulators, memory interface logic, and other random logic.

Fairchild teamed with Control Data Corp. in developing its new logic. The first arrays are going into CDC's upcoming Star 100A high-performance scientific computer. But the two companies will also offer the arrays commercially. A customer would lay out the array of gate functions using a software design package contained in CDC's Cybernet time-shared network, according to Anthony Vacca, manager of circuits, memories, and packaging for CDC's Advanced Research Laboratories in Minneapolis. Tape would be generated, which Fairchild would use to make the final masks.

The two companies believe they have solved the problems inherent in a gate-array approach—the relative inefficiency of circuit design with a fixed gate structure, and the relatively large chip size thanks to the large ECL structures. Fairchild's Isoplanar 2 process, in which oxide isolation defines the edges of transistor bases and emitters, creates a fairly dense chip. (It measures 130 by 173 mils.) And unlike other software design aids developed on minicomputers, CDC designed its software package on the giant 7600 supercomputer, according to Vacca. Consequently, typically more than 90% of the gates—there are 168 per chip—can be used in a custom-designed array, many more than with other design tools, he says.

The gate array has another important advantage, according to Thomas A. Longo, vice president and chief technical officer at Fairchild's Mountain View, Calif., headquarters: a quick turnaround time from

Semiconductor makers aim at gate arrays

Computer mainframe designers have their eyes on gate arrays, high-speed large-scale integrated parts that provide a semicustom solution to the problems of using high-speed logic. Though fast, discrete parts and small- and medium-scale logic parts can bog down a system with interconnect, dissipation, and speed problems. But computers employ so many different logic functions that it is generally not economical to go with LSI.

The gate array approach lets a chip maker crank out in volume an LSI chip of unconnected cells or gates arranged in a standard pattern that can be customized into particular functions with the interconnecting metalization. Gate arrays lower component count, maintain speed, and increase reliability. The trick is to design the basic cell or gate pattern so that the maximum number are available for the various logic functions.

Besides the Fairchild–Control Data announcement, Fujitsu and Motorola supply proprietary emitter-coupled-logic gate arrays of up to 100 gates on a chip that come in more than 100 logic combinations. Siemens in West Germany has announced a 144-gate ECL array. And in the United Kingdom, Plessey has introduced a 144-gate array, Ferranti has one in its unique collector-diffusion isolation process, and ICL, the computer house, has announced a 400-gate ECL array that will be made by Motorola, Philips, and Plessey Semiconductors [*Electronics*, March 16, p. 63].

design to part of two to three months. Further, the gate array saves board space and reduces the number of interconnections by a factor of three or four, he continues.

In addition, although ECL is noted for high power dissipation, Vacca says that "on a per-gate basis you don't pay a price for the LSI." Ten to 15 equivalent F100K parts would dissipate between 500 and 700 milliwatts each, compared with 4 watts or less for a gate array, he says. He estimates that each Star computer will use about 2,500 gate arrays in 14 logic functions.

Specs. The price could be about $10 in hundred-and-up quantities, says Fairchild. Specifications include gate propagation delays of 750 nanoseconds typically, flip-flops with toggle frequencies in excess of 500 megahertz, and speeds of more than 5 gigahertz.

Motorola's ECL gate arrays will be supplied on a 200-by-200 mil chip that offers a designer the equivalent of 650 to 700 10K compatible gates. Typical internal delays of 1.0 ns with typical output speeds of 1.5 ns make the chips fast enough for most current ECL applications.

The chip, samples of which will be available by the end of the year, is organized in 48 multigate cells which can be configured in series-gated structures. There are 30 output buffers and 32 extra input logic buffer gates for interfacing the chip with a wide variety of functions. The chip dissipates 3.75 w at 5.2 v in a standard package. □

Fiber optics

Air Force develops its own interfaces to lower cost of switching to light beams

Aiming ultimately to substitute optical data links for the myriad hardwire interconnections within its aircraft, the Air Force has decided to develop its own interfaces to connect light emitters and receivers with logic circuitry. It is doing so for a reason not usually associated with Government procurement: it believes it can get a lower price by designing the interfaces to its own specifications.

"The hybrid techniques used to date [by industrial companies] have resulted in modules too big and too expensive for even the Government," says Gary D. Gaugler, project engineer at the Air Force Avionics Laboratory's Microelectronics branch at Wright-Patterson Air Force Base, Dayton, Ohio. "So we decided to apply a little [bipolar] LSI muscle."

The result will be devices that, Gaugler hopes, will also be of interest to a broad industrial base. "We think the modules will eventually sell for $25 each in reasonable procurement quantities of 500 to 1,000 units," he says, noting that commercially available hybrid and discrete modules of comparable performance from a variety of vendors are tagged at $500 to $1,500 [*Electronics*, Feb. 16, p. 154].

So far the Air Force has received two kinds of chips. One is a constant-current light-emitting-diode driver, while the other is a receiver chip that amplifies the signal from a photodiode detector and provides a digital output. They were developed under a $139,000 contract by a team of engineers from Honeywell Inc.'s Solid State Electronics Center, Plymouth, Minn., and Spectronics Inc., Richardson, Texas.

Modules coming. The next step is to build the chips into pluggable transmitter and receiver modules. The modules will house one of the two large-scale integrated circuits plus, for the transmitter, an LED, several small bypass capacitors, and a connector for joining the LED to a fiber-optic cable. A receiver will contain its IC plus a photodiode detector and automatic gain control, coupling, and bypass capacitors. Each module will fit in a package 0.5 inch square and 2 inches long.

Bids on contracts to fabricate the modules are due in April. But the chips themselves will be available earlier. Fabricated by Honeywell but marketed by Spectronics, a noted supplier of optoelectronics components, they will be offered in sample quantities next month for approximately $100 each. The price for production quantities could fall to $10 within a year, Gaugler estimates. Honeywell, however, has more than just an interest in selling chips: it can use them in its own industrial control and computer systems.

Gaugler believes the chips will be the first high-performance, monolithic transmitter and receiver interfaces available off the shelf. "They were designed general-purpose enough to fit into a myriad of military and industrial systems," he says. Used together in a Manchester-coded, point-to-point system, they are guaranteed to operate up to 10 megabits per second, "although they can easily run about 15 Mb/s, and up to 20 Mb/s in some systems," Gaugler adds. Inputs and outputs are compatible with transistor-transistor-logic levels, and the devices can be powered by a single 5-volt supply, ±10%. They are qualified for the full −55°C to +125°C military temperature range.

Pin possibilities. The circuits sport a lot of extras, as well. Three pins on the transmitter chip's 14-pin ceramic package can be used to program the LED drive current anywhere from 25 milliamperes to 125 mA. Currents outside these limits may be set with an external resistor to tailor the device to different LEDs and cable lengths. All circuitry is compensated on chip for temperature and voltage changes, and the transmitter includes a prebiasing circuit that keeps the LED biased at about 15 microamperes, ensuring a fast and linear LED rise when the drive pulse comes.

The receiver contains a low-noise preamplifier with automatic gain control, a post amplifier with two limiting stages, and a comparator stage that drives a Schottky-clamped digital output. All this fits on a chip that is roughly 80 mils square. The chip also contains its own regulated power supplies and will handle input photocurrents ranging from 125 to 500 nanoamperes; a minimum of 250 nA will produce a worst-case bit error rate of 10^{-8}. □

Electronic warfare

Signal detector uses an optical memory

Grumman Aerospace Corp. is turning to optical techniques for a critical electronic-warfare chore: identifying the sources of the myriad electronic signals confronting aircraft in a battle zone. It hopes to do the identification automatically by comparing the signals hitting the aircraft with electronic signatures stored in a holographic memory.

Lab system. A laboratory system of what it calls an Emitter Recognizer, put together with Grumman's own funds, has been built at the company's facilities in Bethpage, N. Y. Another system has been built in a van, and Grumman plans to demonstrate it this summer in an effort to attract funding from the military.

The firm's approach, in which radio-frequency signals are converted to optical ones to be analyzed quickly in real time, follows along the path being taken by other researchers in the field [*Electronics*, Dec. 22, p. 29]. Moreover, the Air Force Avionics Laboratory at Wright-Patterson Air Force Base, Dayton, Ohio, is about to award a contract for a new type of optical analyzer for identifying rf signals in an electronic-warfare environment.

Bragg cell. The Grumman system operates with the rf signals acquired by a conventional aircraft receiver, according to Robert Brandstetter, project engineer in the Optics and Displays Equipment Design group. Fed to a power amplifier, the signals are used to drive an ultrasonic light modulator—a Bragg-cell piezoelectric transducer—which converts the rf signal to an acoustic wave that modulates a laser beam.

So far in the system, the signals have been handled in a fairly common manner—Bragg cells are typically used to modulate a laser beam. However, the beam then travels through a lens that produces a Fourier transform of the light signals. Thus, the system now has a spatial distribution of the incoming signals, with frequency and amplitude represented by position and intensity.

The result is a light beam "whose spatial frequency is a function of the incoming rf frequencies," Brandstetter says.

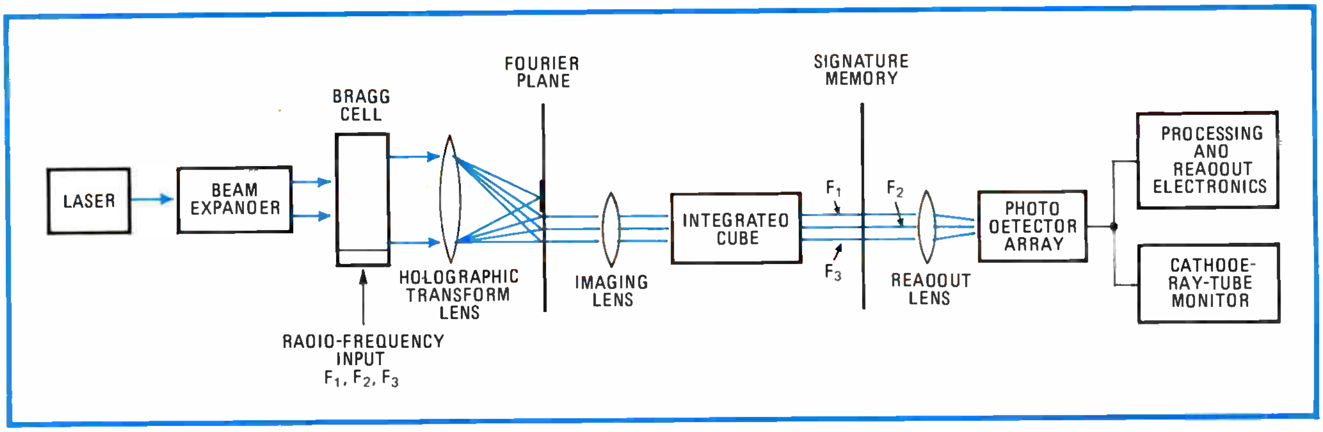
In the prototype, the transform lens is a holographic matrix that replicates the transform by the number of lens elements it contains. The matrix, used because the dimensions of the elements can be easily controlled, yields many identical signal readouts for comparison with signatures of known emitters stored in an optical holographic memory.

This memory, made of a transparent photosensitive polymer from Du Pont, holds as many as 500 separate signatures in individual holograms, according to Brandstetter. The holograms contain patterns of interference lines previously produced by modulating the index of refraction of the material with the frequencies common to each of the emitters the military will be concerned about. Each signature—in effect, a filter—passes only the set of incoming frequencies characteristic of a particular emitting source. Behind each signature hologram are arrays of photodetectors positioned to align with each spectral element.

Match sensors. When the incoming signals contain the discrete frequencies common to a signature in the memory, the match is picked up by the photodetectors: elements like photodiodes or charge-coupled devices. The outputs of these then go to processing electronics that identifies the source of the signals.

The system can also be programmed to respond automatically to foreseeable threats. "We can send out jamming signals and threat warnings," says Brandstetter, "or we can automatically take evasive actions."

Any unknown signal received can be used to update the filter bank. If there is no correlation between an incoming set of signals and a stored signature, the system triggers a proprietary optical device, called an Integrated Cube, to add a reference



Analyzer. Emitter Recognizer from Grumman Aerospace compares Fourier transforms of radio-frequency signals that have been converted to light with signatures of emitters stored in a holographic memory. Matches can be read out and processed automatically.

Companies

Signetics eyes $200 million level

When Philips took over control of Signetics Corp. from Corning Glass Works in the spring of 1975, the semiconductor maker's sales had reportedly fallen to about $100 million. Clearly the company was in trouble. The bottom had fallen out of its 54/74 bipolar standard logic market—the company's bread-and-butter product line—and its proprietory non-industry-standard 2650 microprocessor had not made much headway against the 8080 and 6800 microcomputer families.

To make matters even worse, Signetics had not penetrated the potentially huge market in 4,096-bit dynamic random-access memories. Indeed, its best showing was in the much smaller cache and bipolar buffer memories, a market dominated by Fairchild Semiconductor.

Three years later, the picture has changed dramatically. Under the sympathetic eye of the giant Philips Gloeilampenfabrieken of the Netherlands and with major capital infusion for new technology that is beginning to pay off, Signetics ended 1977 with over $170 million in sales, or 35% over 1976. And Jack Halter, executive vice president and director of marketing, looks for the company to reach the $200 million level by the end of this year.

"Our relationship with Philips has been extremely rewarding," Halter says. "Having a supportive parent who understands both the technology and the market is gratifying. We have been able to position ourselves in new technology and product development to participate in the major growth of the semiconductor industry over the next few years."

MOS the key. To do this, the Sunnyvale, Calif., company, which has highly regarded bipolar lines in memory, standard logic, and other large-scale integrated circuits, must of course turn it around in metal oxide semiconductors. "We recognize," says Halter, "that a major portion of growth will be in MOS—memory, microprocessors, and dedicated LSI—and we're well into a massive program to develop the products needed for this market."

Memory program. To back this up Halter has revealed a memory development program for the next two years that is unsurpassed by any in the industry. On the list are 64-K dynamic random-access memories, 32-K and 64-K erasable programmable read-only memories, 128-K and 256-K ROMs, 8-K and 16-K static RAMs, and 8- and 16-K electrically alterable metal-nitride-oxide-semiconductor ROMs.

In the near term are the industry-standard 2114-type 4-K statics, the 4116-type 16-K dynamics, 32- and 64-K ROMs, and 16- and 32-K erasable PROMs, many already in the sampling stage.

In computer and related products, Signetics is now supplying, in addition to its own 2650-based central processor unit and peripheral parts, the 8080 family, including central processing units and 8080 peripherals, as well as one-chip microprocessors such as the 8048 parts. □

Industrial applications of microcomputers lag

Although microcomputer chips and boards are available in great quantity throughout the industrial electronics field, it has apparently taken longer than expected to develop high-volume applications for them. This is the report from last week's 4th Annual Conference and Exhibit on Industrial Applications of Microprocessors held in Philadelphia. Three reasons are cited for the delay: programming difficulties, a confusing plethora of microprocessor parts, and fear of the difficulty and expense of testing.

"Industrial OEMs often enter the microcomputer market at the chip level," says Alan Swartz, a sales representative for Digital Equipment Corp., Maynard, Mass., supplier of the LSI-11 board microcomputer. "They go out and buy a development system and find that programming is much more difficult than they were first led to believe."

Original-equipment manufacturers of such things as process, numerical, and white-goods controllers all contribute to the market's delayed takeoff, notes Walt Luciw, an advanced-circuits design engineer at Sperry Univac, Blue Bell, Pa. He applies microprocessors to Sperry products and finds himself in a continuing design dialogue with other OEMs. "Everybody's waiting for the Nirvana of a chip that's going to solve all their problems. The result is many months' slippage before getting into high-volume production."

Moreover, heretofore unexposed to microcomputers and automatic test systems, industrial OEMs "are scared by what they hear about microprocessor reliability and test-system costs," says Robert P. Szpila, marketing manager for test systems at GenRad Corp. Concord, Mass. "It's an educational problem. Industry looks at the expense of a large-scale system for testing microprocessors and says it's too costly. They don't realize it's important to spend a few extra dollars to provide diagnostic testing in a high-volume environment. They are used to having technicians test their boards and don't want to do it any other way." What's more, he continues, some "industrial manufacturers don't really understand what they are testing nor how to develop test programs."

Industrial

Laser radar tunes in air pollutants

Pollution is just about everywhere, but for organizations trying to do something about it, the hard part is finding out exactly how much there is. Enter Stanford University, which has developed a new kind of laser radar that accurately measures average air pollution over a distance of eight miles or pinpoints the location of a cloud or source of pollution up to two miles away.

The development is attracting the interest of the Environmental Protection Administration, as well as industrial groups such as the electric utility industry, according to physics professor Robert L. Byer, who heads the project at Stanford, which is located in Palo Alto, Calif. The EPA would be able to check pollution coming out of tall smokestacks with equipment on the ground, and that includes keeping tabs on clandestine polluters who might be discharging wastes at night. Among the pollutants that can be detected are sulfur dioxide, freon, carbon dioxide, ethylene, carbon monoxide, and water vapor.

Compared with other laser techniques, such as ultraviolet tunable dye lasers or low-power diode lasers that need a fixed retroreflector, the Stanford system has several advantages, Byer says. It operates in the infrared, where it can detect most of the air pollutants, and it is also safe for eyes. It needs no fixed retroreflector and can operate in daylight. Also, the laser radar is much easier to use than wet-chemistry methods, which rely on air samples.

Problems. To get the system's performance, Stanford turned to on-campus expertise in crystal growing, nonlinear optics, and laser sources to solve two major problems, Byer says. It designed a new kind of neodymium-doped yttrium-aluminum-garnet laser with an unstable resonator to achieve a higher output power of 70 millijoules, 1,000 times better than earlier infrared lasers, he says. To tune it in the infrared range, the designers improved the crystal for better line-width control.

The system operates by firing the laser light at the pollutant molecules and then measuring the absorption in the path along which the light travels as it is reflected back to a 16-inch telescope at the laser. Each pollutant absorbs coherent light at a different frequency within the 1.4-to-4-micrometer range of the infrared laser, and the laser is tuned sequentially to each of the absorption frequencies characteristic of the expected pollutants.

PDP-11 analysis. From the light reflected back to the telescope, the system, built around a PDP-11 minicomputer, analyzes which frequencies are absorbed, gauged against a nonabsorbed reference frequency. For sulphur dioxide, for example, concentrations can be determined to 1 part in 1 million over a 1-kilometer path; for methane, 1 part per billion over a 100-meter path.

Topographic reflections. Instead of special reflectors, the system relies on reflections from "topographic targets like grass, hillsides, buildings, or aerosols suspended in the atmosphere," explains Max Garbuny, a consultant at Westinghouse Electric Co.'s Research and Development Center, Pittsburgh. He asserts that Westinghouse made the first experiments on this "differential absorption spectroscopy" using an infrared tunable laser in 1973. Westinghouse has worked closely with Stanford, he points out, and is in putting together a similar laser system for the National Aeronautics and Space Administration's Langley Research Center.

Stanford's system is tuned by rotating lithium-niobate crystals in front of the neodymium-doped YAG 1.06-μm pump source. The reflected light is received by a liquid-nitrogen-cooled standard IR photodetector at the telescope. After preamplification, the signals are fed to a Computer Laboratories Inc. 12-bit, 5-megahertz analog-to-digital con-

Japan's electron-beam effort challenges U. S.

Japan's efforts to pull ahead of the United States in electron-beam exposure technology for fabricating masks for very-large-scale integrated circuits are revealed in two new units: a raster-scan unit built for the LSI Cooperative Laboratory by Tokyo Shibaura Electric Co. (Toshiba) and a vector-scan unit developed by the Musashino Electrical Communication Laboratory of the Nippon Telegraph and Telephone Public Corp. and Hitachi Ltd. Both of these machines can fabricate masks with smaller line dimensions at speeds comparable to those commercially available units built in the U. S. The raster-scan unit can expose patterns with minimum line width of 1 micrometer on a 100-by-100-mm area in 180 minutes. The vector unit can expose 1-micrometer lines on a 50-by-50-mm area in about 40 minutes.

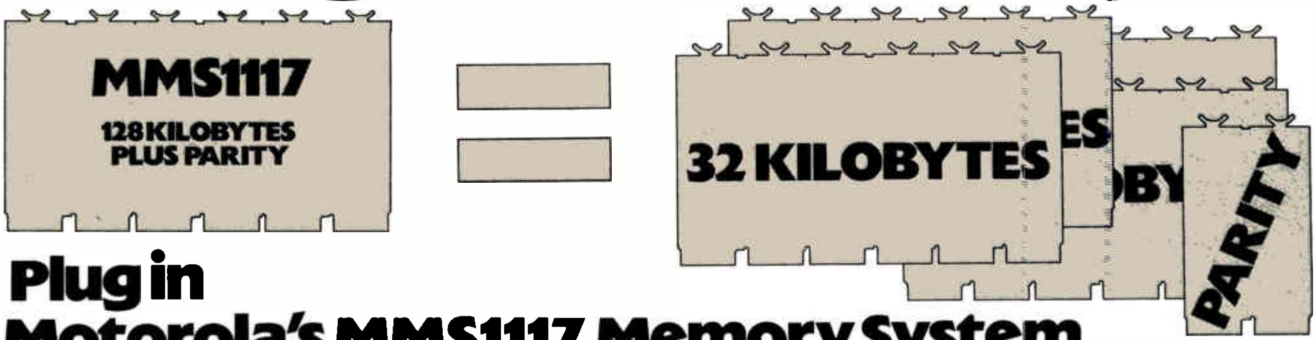
The Cooperative Laboratory's unit is an improved version of a system developed earlier by Toshiba. Changes include a much higher-intensity electron source for faster writing speed, a laser-interferometer–controlled writing table with increased mobility and higher precision, and a larger computer control unit containing a 160-megabyte magnetic-disk pack.

When operating with a 0.25-μm-diameter spot, the electron beam can write over an area of 0.27 square centimeter with a peak beam current of about 200 nanoamperes. Use of a lanthanum boride cathode allows for several times the current density of the tungsten hairpin emitters used in commercial systems from the Bell-licensed ETEC Corp. and Extrion division of Varian Inc. Still, cathode life is said to be a long 2,500 hours.

Because of the high beam density of the new system, it is feasible to use a positive resist of polymethylmethacrylate (PMMA), which is better than other resists even though it suffers from low sensitivity. As an overall display of system performance, the Cooperative Laboratory showed a pattern on a silicon wafer for a 16-bit microprocessor with 10,000 elements that it shrunk from a 5.6-by-5.6-mm area to fit on a chip measuring 1 by 1 mm. The minimum line width on the mask is 1 μm. However, no one is saying the chip will operate, merely that photolithography is feasible.

The NTT/Hitachi vector-scan system can handle individual areas of 2 by 2 mm, with the table moving between adjacent scan areas. It is theoretically more efficient than raster-scan units, because only areas requiring exposure need be processed rather than the entire mask. But the larger scan area requires a lens with greater focal length and smaller apertures. Nevertheless, the greater efficiency of vector scan and its ability to vary the scan speeds between 0.001 and 1 meter per second bring the unit writing speed up to a level comparable with that of a raster-scan unit for average patterns. Toshiba says it will start selling its raster-scan system early next year. Hitachi is not saying when it will.

For high-density "universal" PDP-11* storage, with parity...



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Now it's easy and inexpensive to add in high-density, high-speed PDP-11 compatible memory with parity features. Motorola's MMS1117 memory system provides total electrical and mechanical compatibility with 10 different UNIBUS* PDP-11 processors; the new 11/60, plus 11/04, 11/05, 11/10, 11/34, 11/35, 11/40, 11/45, 11/50, and 11/55. Just plug it into any new "Hex SPC" slot.

MOTOROLA SEMICONDUCTOR MEMORY SYSTEMS

System	Organization	Description
MMS1110 MMS1110-1 MMS1110-2 MMS1110-3	16K x 16 12K x 16 8K x 16 4K x 16	Add-in for LSI-11 systems
MMS1116	16K x 16	Add-in for PDP-11/05, 11/10, 11/35, 11/40 and 11/45 systems
MMS1118 MMS1118-1 MMS1118-2	16K x 18 12K x 18 8K x 18	Add-in for PDP-11/04, 11/34 systems
MMS3400	32K x 18 or 64K x 9	For 3400N systems
MMS68102 MMS68102-1 MMS68102A MMS68102A-1	16K x 8 8K x 8 16K x 9 8K x 9	Battery backup for M6800 and other synchronous systems; pin compatible with EXORcisert micromodule
MMS68103 MMS68103-1 MMS68103A MMS68103A-1	16K x 8 8K x 8 16K x 9 8K x 9	Hidden refresh for M6800-based systems.
MMS68104	16K x 8	For MEK6800D2 Kit
MMS80810 MMS80810-1	32K x 8 16K x 8	For 8080A-based systems; pin-compatible with SBC 80/10

A fully populated MMS1117 is a whopping 128 kilobytes, and options include systems of 96, 64, and 32 kilobytes, priced appropriately lower. Parity options are on-board parity plus controller, parity data only, or no parity. All are available for each of the three system speed options.

128 Kilobyte MMS1117

Read Access Time Typical	Price 1—5
370ns	$4,305
420ns	$3,920
470ns	$3,530

The MMS1117 interfaces to all 18 bus address lines. Starting address can be selected, via switches, to fall on any 4K word boundary between 0 and 124K. The MMS1117 imposes one UNIBUS load regardless of memory size or parity option. Despite the density and speed of the MMS1117, power requirements are low. A fully populated 128 kilobyte system with parity and controller operates at the following rates: 5 V ±5% @ 3.0 A (typ), +15 V @ 0.2 A standby and 0.7 A continuous maximum access, −15 V @ 0.03 A.

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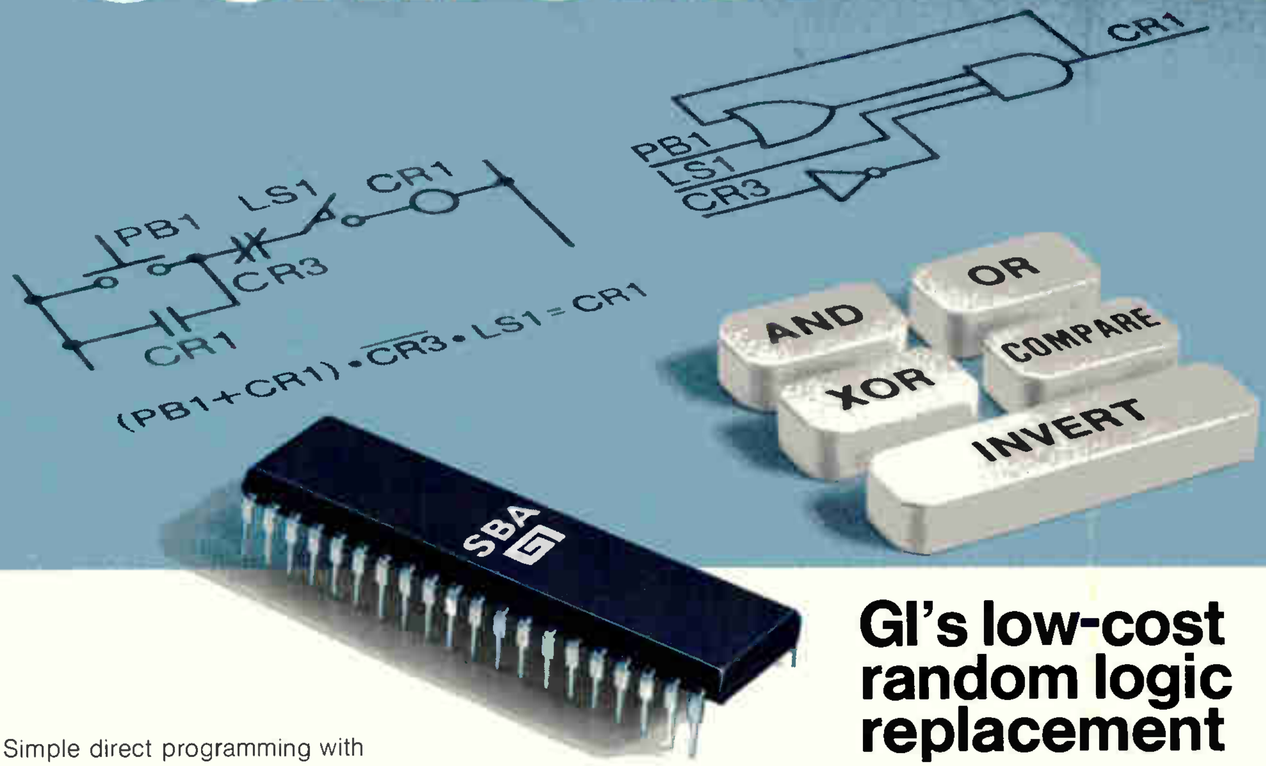
Circle 45 on reader service card

The SBA Programmable Controller



GI's low-cost random logic replacement

Simple direct programming with logic statements, and a low price tag are leading features of GI's new SBA. Sequences are written using familiar Boolean logic equations as a "programming language." Now you can program timing and control functions in a range of products.

The single-chip, one-bit SBA microcomputer has 30 TTL compatible pins that can be assigned as inputs, outputs, or multiplexed input/outputs. And a 1023-word memory stores your program. A logic unit teamed with a 16-element stack interacts with a 120-element read/write memory to produce programmed outputs a term at a time.

A cost-effective alternative to 4-bit and 8-bit microprocessors, the SBA performs decision-oriented tasks efficiently at millisecond speeds.

As for applications, consider using the SBA in process timers and monitors, machine controllers, security or telecommunication systems. The SBA will do wonders for electronic games and household appliances. What's more, you can put the SBA to work converting and processing routine data in microprocessor-based systems.

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Washington newsletter

Congress moves to restore strategic R&D funds to Navy . . .

Navy research and development for strategic and tactical programs—already budgeted to rise 11.6% to $4.49 billion in fiscal 1979 and another 6% to $4.76 billion the next year—**may show an even bigger jump now that the House and Senate Armed Services Committees have proposed additions** to strategic program funds. Money for such efforts, including the new, larger Trident missile-launching submarine, had been budgeted by President Carter for a 21% cut to $682 million in the coming fiscal year, to be followed by a further 17% reduction to $563 million in fiscal 1980. Even if those cuts are more than restored, though, tactical programs are as usual expected to account for more than half the Navy R&D outlays: they are to climb more than 21% to $2.49 billion next fiscal year before stabilizing in fiscal 1980 with an inflation-offsetting increase of 8% at $2.69 billion.

. . . but tactical sea control, ASW top Navy priorities

Tactical sea control programs with a high electronics content continue to be the largest item on the Navy's budget for tactical R&D. Spending for that area is scheduled for an increase of one third to $1.4 billion in fiscal 1979 followed by a 22% jump to $1.75 billion a year later. Land warfare, communications, and combat integration are also scheduled for significant increases, while aircraft R&D is the only category scheduled to decline, dropping 4% to $785 million next year and a further 17% to $647 million in fiscal 1980. Reflecting Navy concern with Russia's expanding submarine fleet, **antisubmarine warfare R&D outlays will nearly double to $396 million over the next two years,** including a 61% hike to $333 in fiscal 1979 from present levels.

Postal Service denied monopoly on electronic mail

The U.S. Postal Service won't have a monopoly on electronic mail systems development with mandated annual R&D spending of 2% of postal revenues—an estimated $200 million in 1980. That's the effect of changes in legislation after complaints from congressional and industry leaders that it threatened continued competitive development of the technology.

The Computer and Communications Industry Association and other opponents of the measure had two fears: **that the Postal Service would lock itself in with a major contractor** like AT&T or IBM in order to meet the massive increase in R&D spending it could not handle in house, and that "private express" laws limiting the mails to the Postal Service would make electronic mail a part of that monopoly.

NRL develops device failure detection method

A four-man Naval Research Laboratory team headed by George A. Haas has developed a technique to examine semiconductor failure and imperfection mechanisms. Named LEER (low-energy electron reflections), the technique relates bulk and surface electronic properties in electronic-device materials.

Haas says that by using an incident electron beam of 10 V or less, his team achieved **the first simultaneous but separate measurements of the two components of a semiconductor's work function**—the energy difference between the Fermi level inside and the vacuum level outside. The two components are the position of the conduction band with respect to the Fermi level, a bulk property, and the electron affinity, a surface property, Haas explains.

Japan moves ahead in TV broadcast satellites

The United States has few peers when it comes to technological innovation. Yet it is often slow to follow its development of new techniques with real-world applications leading to the creation of major new markets. Direct-broadcast satellites are perhaps the most recent example.

These systems relay high-quality, high-power television signals to small, low-cost ground receivers in remote areas. They got their start with the 1974 launching of Applications Technology Satellite 6 by the National Aeronautics and Space Administration. Two years later, NASA orbited the joint U. S.-Canada Communications Technology Satellite, at present used mainly by the Canadians to bring TV to its provinces in the west and far north. Now Japan has picked up on the ATS-6 and CTS technologies for a new satellite called BSE (for medium-scale broadcasting satellite for experimental purposes) and is ready to begin direct broadcasting from it of two color TV signals to homes on its remote islands and Okinawa. Just launched by NASA for Japan's space agency, the BSE was built by General Electric Co. under contract to Tokyo Shibaura Electric Co. Japan estimates it can turn out the necessary home antennas with diameters as small as 1 to 1.6 meters (3.3 to 5.2 feet) for as little as $200.

America's slow progress

Commercial use of direct-broadcast satellites in the U. S., meanwhile, is not scheduled to begin before the 1980 launching of Satellite Business Systems Inc.'s first system [*Electronics*, Oct. 13, 1977, p. 32]. Designed and built by Hughes Aircraft Co., it will use the same 12-to-14-gigahertz frequencies as Japan's BSE and is intended for business and Government users. Unattended ground stations on a customer's premises will have both transmitting and receiving capabilities and cost an estimated $474,000. The system, developed by SBS, a joint venture of Aetna Life & Casualty Co., Comsat General Corp., and IBM Corp., is clearly a far more sophisticated system than Japan's receive-only BSE package. The closest American equivalent to Japan's system is the Corporation for Public Broadcasting's use of transponders on Western Union's Westar I satellite, which earlier this month started distributing TV signals to 24 public television stations in the southeastern U. S. using large receive-only terminals at the various station sites.

In contrast, Japan, on completion of its BSE experiments, will have the technology in hand to develop and sell low-cost TV ground terminals to developing markets throughout the world, and that is a matter of concern to long-range planners in U. S. agencies involved with technology and trade. "There are enormous untapped markets for television in just about every country in Africa and Latin America," notes one Government trade specialist. "Few of these countries have land-line telephone systems that can be used for TV transmission. Satellites are a natural for them. Anyone who can sell them a satellite system with inexpensive ground antennas will not only make money with its initial system but will realize an even greater potential by creating a market for TV sets where there was none before." Admittedly, these new markets are still some years away from realization. Nevertheless, the potential is there, and, as the same market planner observes, "with the U. S. and Europe putting the squeeze on TV exports by Japan, it must find new markets if it is going to effectively maintain its production capability in the home islands."

Problems of motivation

The close cooperation of Japan's government and industry is being cited once more as one reason why Japan is taking the lead in developing direct-broadcast systems for TV. Japan's geography, with its remote islands, is another. "We don't have that kind of problem in America," explains one broadcast network specialist in Washington, "so the commercial market has never developed. Most everyone uses telephone lines for TV signal transmission." While there are legislators in large, sparsely populated states like Arizona and Wyoming who dispute the adequacy of land lines for TV signal transmission, they have not altered the *status quo* in the U. S. TV transmission market. Lacking any strong public demand for change, the slow-moving Federal Communications Commission—an agency not concerned with developing overseas markets—has had no reason to even consider direct-broadcast satellites for commercial television.

Thus Japan now has the edge in developing inexpensive antennas for receiving satellite TV signals at home. The fact that the satellites themselves originated in the U. S. is of less importance; the market for them is minuscule compared with the potential market for antennas and TV receivers that will use them. If the U. S. is to capitalize on its direct-broadcast technology in new markets throughout the world, it cannot continue to concentrate its efforts only on costly, state-of-the-art systems like those of SBS and ignore the potential of simpler systems like Japan's BSE. **Ray Connolly**

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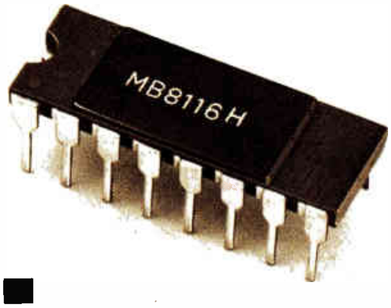

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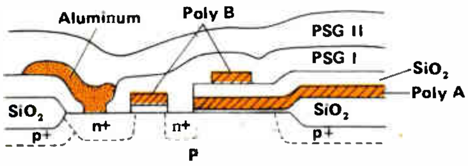

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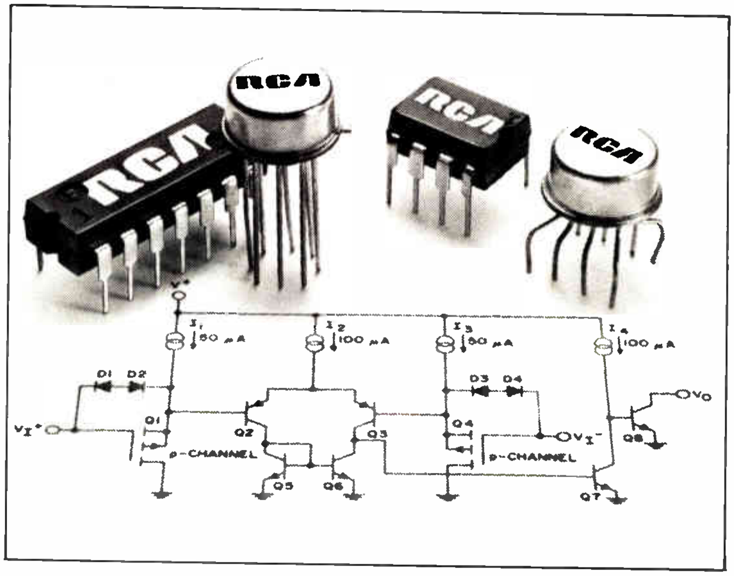

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Circle 54 on reader service card

International newsletter

East Germans show electron-beam mask system . . .

The products shown at East Germany's Leipzig Fair this month **point to the high level of sophistication attained by the Socialist Bloc in some areas of IC production equipment.** One is an electron-beam pattern generator that its developers claim matches similar systems made in the West. Built at the renowned East German optical-equipment maker VEB Carl Zeiss of Jena and developed in cooperation with Soviet specialists, the ZBA-10 system is said to produce resist masks with pattern structures smaller than 1 μm and at a positioning accuracy of about 0.1 μm.

. . . and universal single-barrel repeater

Also shown was another product of Carl Zeiss of Jena, a universal single-barrel repeater for fabricating masks used in manufacturing integrated circuits and large-scale ICs. The X-Y table of the UER, the initial letters of the German words for universal single-barrel repeater, **is controlled by a laser distance-measuring system** that ensures an image-positioning accuracy of better than 0.1 μm. Designed for the laboratory and mass production, the UER allows fabrication of masks used to transfer patterns on wafers up to 4 in. in diameter.

Siemens to use 16-K RAMs in mainframes

Watch for Siemens AG to join the still-small league of firms marketing computer mainframes that incorporate 16-K random-access memories. The RAMs will turn up in the company's 7.760 computer, a large universal system that will start being delivered in May.

Meanwhile, the German firm's electronic components group in Munich is pushing the development of its 64-K RAMs. **Siemens designers are banking on V-channel MOS technology,** whereas most other semiconductor producers are considering the double-polysilicon-gate techniques they use in 16-K RAMs for their 64-K work. Siemens expects to have its first 64-K V-MOS devices ready as samples toward the end of this year.

Britons develop a rugged single-mode cable

Researchers at Standard Telecommunications Laboratories in Britain have moved closer to the development of long-haul fiber-optic telecommunications links slated for the 1980s by producing a single-mode fiber-optic cable rugged enough to withstand normal cable-laying procedures. The low-loss, step-index fiber used was demonstrated in the laboratory four to five years ago, but its 4-μm core diameter (outer diameter with cladding is 100 μm) required the development of cabling techniques that would prevent its optical properties from being changed by the pulling procedure.

The attenuation of the cable is 2.8 dB at 0.87 μm, the wavelength of current gallium-aluminum-arsenide heterojunction lasers. This permits an information capacity of over 40 Gb/s. But the performance improves even further to 1.7 dB/km at 1.1 μm.

Italians draft space program aimed at TV

Although the "back again" Giulio Andreotti government in Italy still has to work out how much money it can spend, it does know fairly well what it wants to do in space over the next five years. Under a draft program that has been approved by the ministries concerned, **the strictly national effort will go in heavily for telecommunications.** The key project: a satellite for direct broadcast of television programs to rooftop antennas, using the 20-to-30-GHz band.

Despite a planned step-up in funds for the domestic effort, some 60% or more of Italian space spending will be channeled to the international programs run by the European Space Agency. Italian space officials maintain they are not getting a fair return for their contributions to the agency and hope to improve the balance by selling to ESA, for use in its Meteosat program, the backup unit for the Sirio experimental communications satellite that was launched last summer from Cape Kennedy.

Olivetti to show word processor

C. Olivetti, the Italian leader in data-processing and office equipment, **has moved a notch closer to an electronic typewriter.** The company plans to introduce at the mid-April Hanover Fair in West Germany a desktop word processor that includes a typewriter keyboard, a light-emitting-diode display for making corrections, a 30-character-per-second daisy-wheel printer, a minidisk unit for recording letters, and 8,000 words of user memory, all under control of an Intel 8080 microprocessor.

Olivetti expects to price the processor, designated the TES 401, at between $5,000 to $6,000. The unit can stand alone or be linked to other word processors for electronic mail.

Big array processor to be installed for UK research

Britain's International Computers Ltd. is in the final stages of negotiation with the UK's computer board for universities for the delivery early next year of a computer that can outperform today's supercomputers in dealing with major number-crunching tasks. The machine, **a 64-by-64 array of simple processing elements** distributed throughout the memory module of a 2900 system, is destined for Queen Mary College, London, where it will be used to provide a service bureau to British universities and research establishments. In addition, government agencies like the Science Research Council and Social Science Research Council are expected to fund software development aimed at establishing how best to exploit parallel processing. ICL already has a prototype 32-by-32-element array working.

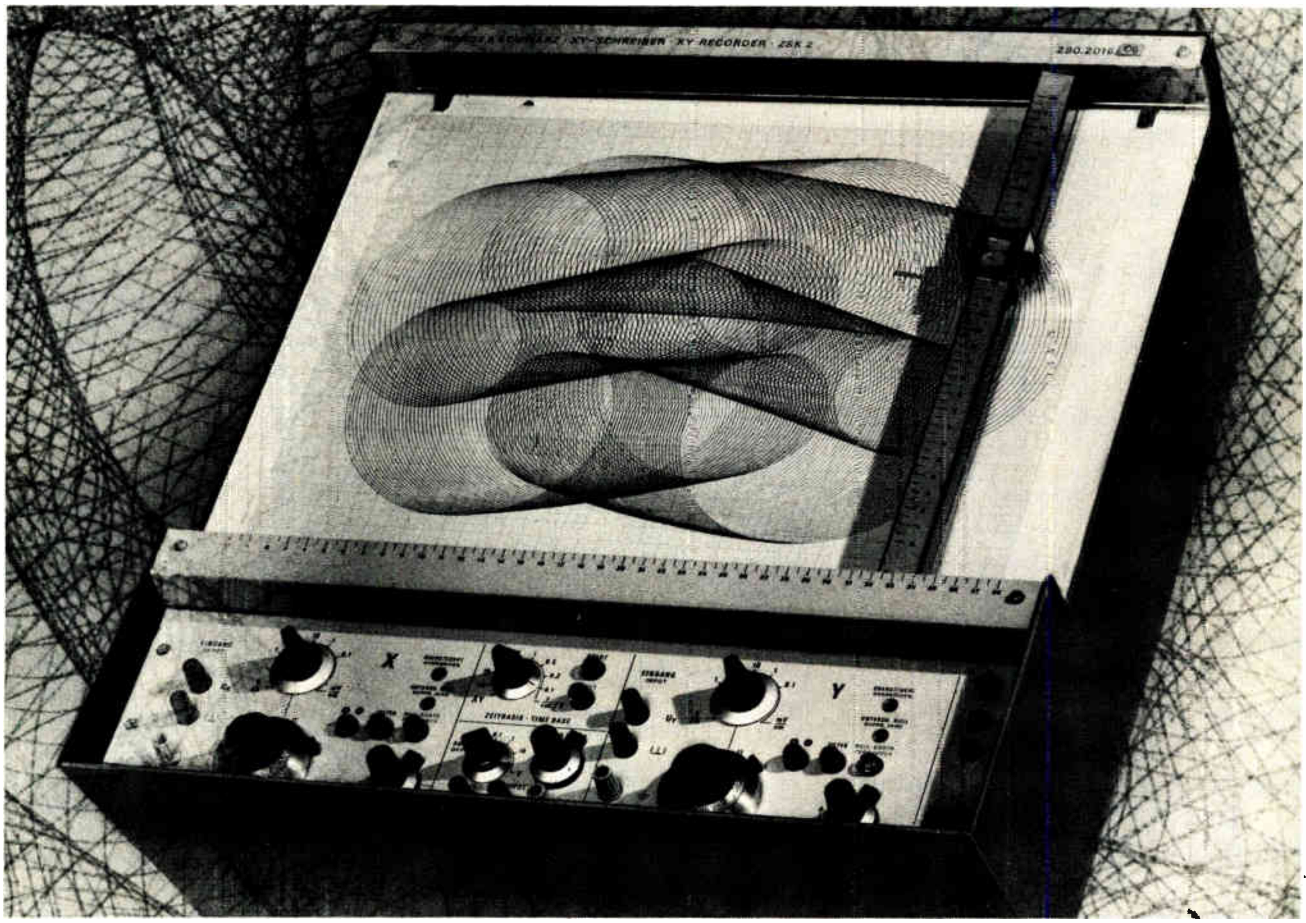
Japan Victor's VCR selected by Nordmende

After thorough tests of a number of video cassette recorder systems, Nordmende, a big entertainment electronics producer in West Germany, has selected the Victor Co. of Japan's Video Home System as the one it will sell and may eventually produce. **The reason: low tape costs and the compact design of the drive mechanism.** Nordmende, which recently became an affiliate of France's Thomson-Brandt, will go to market with Victor-produced systems during the upcoming quarter. The two-hour recorder will sell for below $1,460.

Addenda

The specter of the nationalization of the French electronics industry has disappeared with the victory of the ruling Right coalition in the French legislative elections. The unexpectedly large majority for the Right in the assembly **may be the signal for the signing of Franco-American deals destined to restructure the French integrated-circuit industry** [*Electronics,* Feb. 16, p. 65]. . . . Thomson-CSF's semiconductor division **will have a 16-K RAM in production by the end of the year,** says the firm's management. The RAM will be pin-for-pin-compatible with the Mostek 4115. But Thomson's plans could be changed if the French government decides that another firm should concentrate on the 16-K RAM market when it finally reveals its grand design for IC-industry restructuring.

New recorder family: precision priced right



For XY and YT plots there's now the recorder ZSK 2 in five different models so you can choose exactly the right one for your application, and at the right price.

ZSK 2 works on the principle of a self-balancing potentiometer. This gives minimal non-linearity (0.1%) and guarantees good reproducibility (0.05%). The high writing speed of >110 cm/s on both axes combined with fast acceleration produces superior dynamic characteristics. Deflection factors calibrated between 10 μV/cm and 11 V/cm, electronic limiting of the writing area for DIN A3 and A4 plus governable zero offset make operation easier, whilst inputs for remote control and ratio recording mean greater variety of use.

The models differ in their inputs:

Universal model 02
Sensitivity 10 μV/cm; floating input amplifiers with guard; timebase generator.

Standard model 04
Sensitivity 5 mV/cm; differential amplifiers for both inputs.

Lab model with timebase 06
Sensitivity 100 μV/cm; floating input amplifiers; timebase generator; offset-voltage source.

Lab model 08
Sensitivity 100 μV/cm; floating input amplifiers.

System model 10
Sensitivity 100 mV/cm; direct inputs Z_{in} 20 kΩ.

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Sony unveils CCD color camera for home TV

Developers seek to improve sensitivity and push price down into $1,000 region for fall 1979 market debut

Engineers at Sony Corp. have developed a charge-coupled-device color video camera for home use that presents a dual challenge. First, cameras built around vidicons are just coming on the market, but once they have set the market in motion, this rival model could push them out of the picture. Second, Sony believes that its CCDs will have wide applications in high-density memories, signal processing, and logic.

The camera is the first of its kind for which a tentative introduction date has been set—autumn 1979 [*Electronics*, March 16, p. 64]. Previously, RCA Corp. showed engineering models of a color CCD camera intended for the audiovisual market at an audiovisual show in Houston [*Electronics*, Jan. 19, p. 33]. The biggest tasks now faced by Sony's development team are to improve its camera's sensitivity so that it matches that of vidicon models, and to bring its price down to the $1,000 level.

The camera uses three CCD sensors for the three primary colors. Each has 226 picture elements horizontally by 492 vertically, for a total of 111,192. However, Sony engineers have developed a spatial offset technique that they claim doubles horizontal resolution: sensors for blue and red are offset by half the picture element pitch with respect to the sensor for green, giving the equivalent of 452 elements horizontally by 492 vertically.

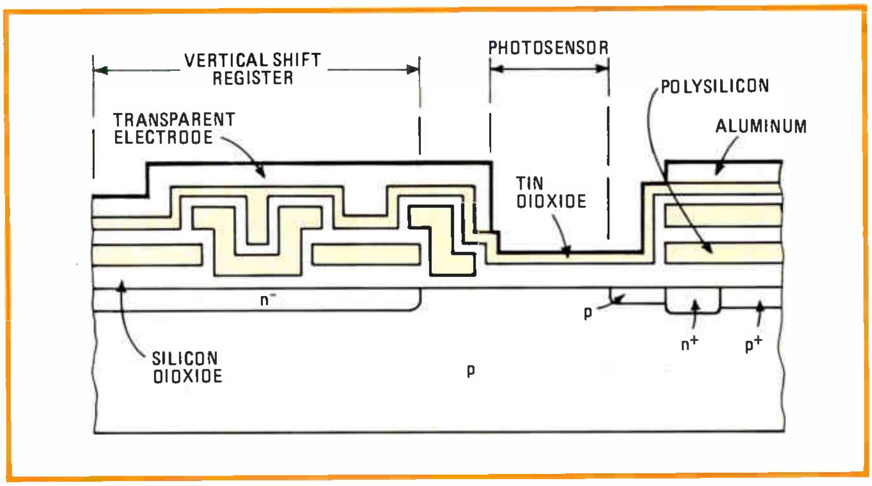
Interline transfer. The CCD area sensor is arranged in the so-called interline transfer configuration. Like other CCD area pickups, each element's photosensor is a small metal-oxide-semiconductor capacitor. Between each column of elements there is a CCD vertical shift register, and at the bottom of the chip there is a horizontal shift register connected to an output amplifier. The MOS photosensors generate and store a charge proportional to the light incident upon them. At a given instant in time, the charge from all the picture elements in the frame is transferred to the CCD vertical shift registers. These in turn transfer their signals one horizontal line at a time to the horizontal shift register, from which the signals are then read out in serial mode.

Each image-sensing chip measures 10.3 by 9.1 millimeters and is sealed in a 24-pin ceramic dual in-line package with a window. The effective sensor area on the chip is 8.8 by 6.6 mm, the same size as the target in ⅔-inch vidicons, permitting use of the same inexpensive color-separation optics and zoom lenses.

Dimensions. Each unit cell pattern measures 36 micrometers horizontally by 13 μm vertically. Of this, less than a quarter, or about 100 μm^2 out of 468 μm^2, is used as the MOS capacitor photosensor. One plate of the capacitor is the p substrate; the other is the thin, transparent, conductive layer of tin oxide overlying the oxide layer.

Portions of the cell where light sensitivity is not desired are covered with a thin aluminum layer, both to shield them and to reduce connection resistance. The transfer gate, vertical shift register, and horizontal shift register have polysilicon electrodes. The two-phase clock drive used with shift registers is conventional.

An n^+ drain and a p region unite to prevent blooming, which might



Getting the picture. Sony's charge-coupled-device chip is 10.3 by 9.1 mm. It houses 226 horizontal by 492 vertical elements; a spatial offset doubles the horizontal resolution.

self-timer, and provides a battery check. The camera is completely battery-powered. Canon estimates that the required 6-volt battery is sufficient for 15,000 exposures, but voltage is not a critical figure. □

France

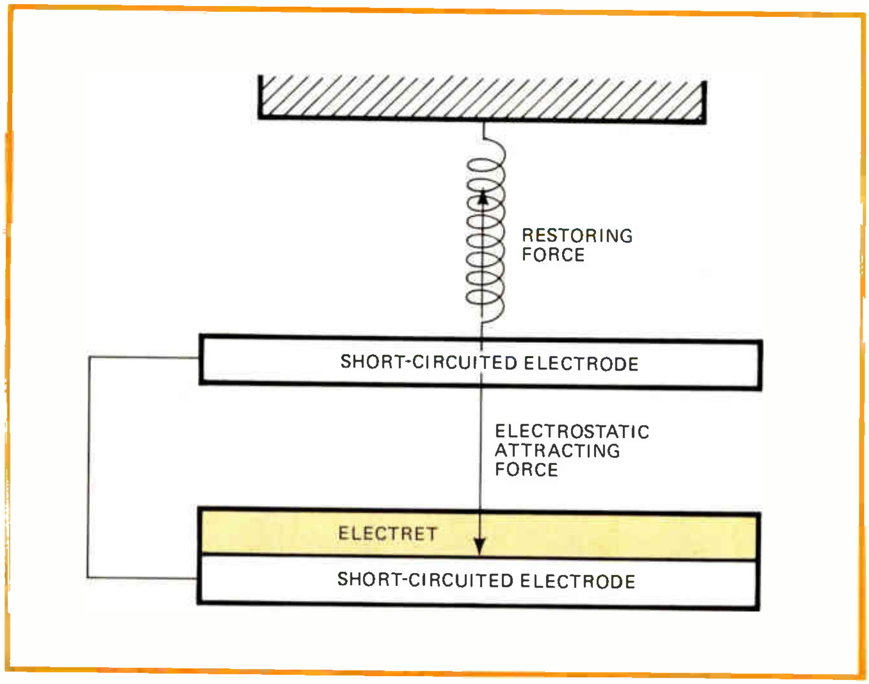
Paris lab develops $20 dosimeter

A French laboratory has come up with an electret-based ionizing-radiation detector incorporating an audible alarm and inexpensive enough for the consumer market. "The unit could sell for less than $20, and this would still include a large profit margin," says Jacques Lewiner, head of the general electrical lab of the Ecole Supérieure de Physique et de Chimie Industrielles, which is owned by the City of Paris.

Lewiner believes that the dosimeter costs at least an order of magnitude less than competitors offering both an audible alarm and a means of measuring the amount of radiation received. Such a device would allow all people living near nuclear installations to check for themselves just how much their environment is or is not being contaminated. Also, there are obvious uses for personnel involved in nuclear work.

Currently there are two main types of radiation dosimeters: those measuring received doses of radiation, and those giving an instant reading of radiation intensity. The first category includes radiation-sensitive photographic film devices, radio fluorescent glass that emits light proportional to the dose absorbed, and dosimeters with ionization chambers—electrometers whose charge decreases as a function of the radiation dose. The first two cannot be read directly by the user, and the electrometer approach is expensive, fragile, and subject to accidental discharge, Lewiner claims. Moreover, none of these methods gives an alarm in case of sudden irradiation.

The second category includes



Everyman's dosimeter. Simplicity of ionizing-radiation detector developed by City of Paris–owned laboratory means that it could sell for as little at $20.

Geiger counters. They tend to be expensive and bulky and always need a high-tension supply.

According to Lewiner, the new unit offers cheapness, reliability, ruggedness, and accuracy, together with both alarm and dose-measurement facilities. Moreover, it needs no power supply except at the moment the alarm is sounded and so can use low-power watch batteries.

The new unit is extremely simple. Lewiner's lab has acquired considerable expertise in the use of electrets; its alarm is triggered by the changes in electrostatic force that occur when an electret is subjected to ionizing radiation.

Using a magnet. The dosimeter works this way: an electret is placed between two short-circuited electrodes and bonded to one of them. If a restoring force (Lewiner uses a magnet) is exerted on the bonded electrode, it will remain in contact with the electret only as long as the restoring force remains less than the electrostatic attracting force. When the external electric field decreases under the effect of ionizing radiations, the intensity of the electrostatic force also decreases until, when it has dropped enough, the bonded electrode moves away from the electret and actuates an alarm.

Measurement of the absorbed dose may be made at any time. By applying a voltage between the electrodes, it is possible to set up an electric field canceling the field of the electret. The value of the voltage is directly proportional to the dose absorbed. Another method is to incorporate a classical photographic dosimeter, sensitive to X, gamma, and beta radiations.

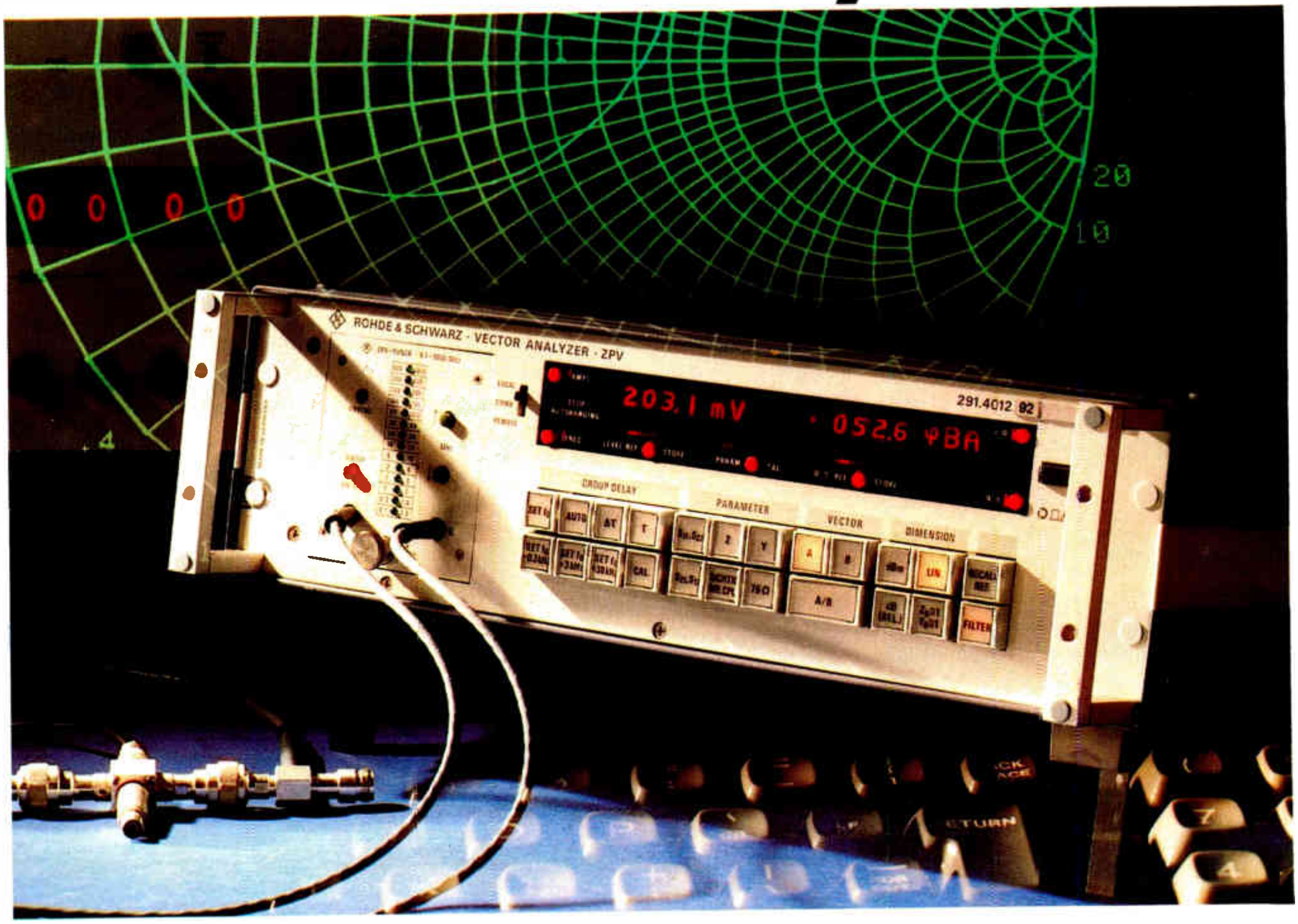
The unit is extremely small and can be worn in the pocket or as a brooch in the form to be presented at the Paris components show in April. It measures 70 by 45 by 8 millimeters and weighs 35 grams complete with batteries. □

Great Britain

Government funds CAD sales effort

To help sell university-developed computer-aided design schemes, the UK's National Research and Development Corp. is supplying a hitherto-lacking sales expertise. One of the

Going new ways:
vector analyzer ZPV



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Circle 158 on reader service card

IR amplifier, receiver ICs introduced for remote-control uses

by John Gosch, Frankfurt bureau manager

Amplifier boosts weak signals by 100 dB, while receiver extends control to four analog functions

Remote-control systems that use infrared signals are the target of two optoelectronic devices to be unveiled by Siemens AG at the Paris Components show next week. One is an amplifier for IR signals and the other is an IR receiver circuit.

Built around the newly developed integrated circuit TDA4050, the amplifier (see photograph) makes it easier to lay out infrared remote-control systems that must operate in large rooms or over longer-than-normal distances. Often, unless the signal source in such a system uses many IR-transmitting diodes, the light power arriving at the receiving end of the control link is too weak to be useful. But the Siemens amplifier allows the IR transmitter—for example, an SAB3210 transmitter IC with a peak output current of 1 ampere—to guarantee good reception of signals modulated onto an IR beam as far as 30 meters from the pick-up diode. The amplifier thus makes it possible to, say, operate a slide projector from the opposite end of a large conference room or to open and close a garage door from the end of a driveway nearly 100 feet long.

The infrared receiver IC extends the command capabilities of remote-control systems. Dubbed the SAB4209, the device can control four analog functions, one more than its forerunner, the SAB3209. Thus the device can be used to remotely control not only the picture brightness of a TV set, its color saturation and receiver volume, but also its picture contrast.

Operation of the amplifier is straightforward. A receiver diode picks up and demodulates the weak IR light, then feeds its output, the command signals, to the TDA4050. This bipolar circuit, integrated on a 4-mm² chip, amplifies the signal in two stages. One boosts it by 77 dB and the other by an additional 23 dB, giving a total of 100 dB. The signal is then strong enough for most remote-control tasks.

Chief characteristic of the TDA4050, says Günter Krämer, a product manager for consumer ICs at the Munich-based company, is its high control voltage range. It is about 70 dB and allows signals of widely differing amplitudes to be processed. Also, since the control voltage is regulated, oscillations are avoided that could occur on the chip as a result of the circuit's high gain.

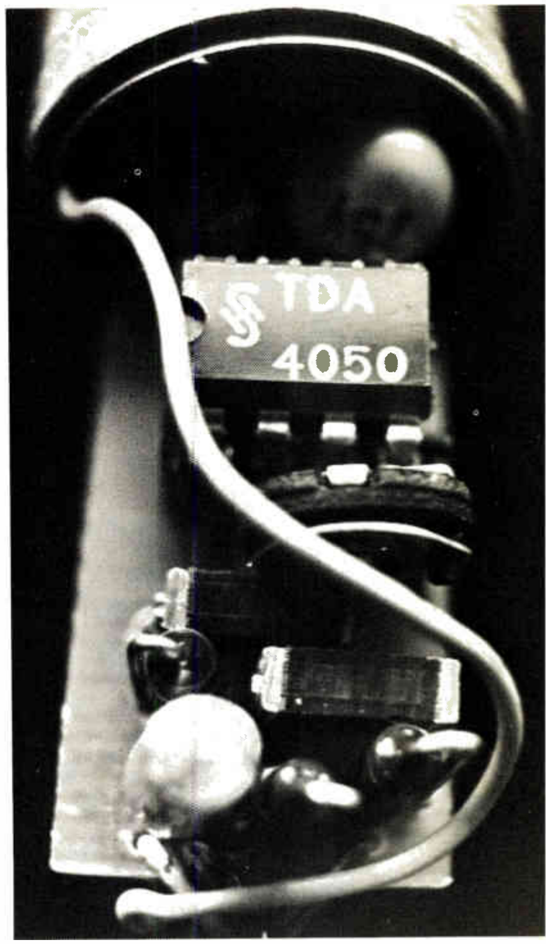
Further, because of its high level of integration, the device needs little peripheral circuitry to do its job, Krämer explains. The TDA4050 has been adapted especially to IR control systems. The chip comes in an 8-pin dual in-line plastic package and operates off supply voltages of 7.5 V to 15 V and in −15°C to 100°C environments. Its current consumption is about 9 mA.

The complete amplifier includes the receiving diode, the TDA4050, and peripheral components, but is also available singly. Its unit price will be "less than $1.25 in large quantities," Krämer says.

As for the IR receiver, another application besides TV sets would be in stereo sound equipment. In addition to volume, bass, and treble—the SAB4209 makes it possible to remotely control a fourth parameter, like speaker balance.

The device's serial data bus allows it to be used with systems like Teletext in a TV receiver or digital tuning in a radio or TV set. Additionally, the circuit processes enough commands to be able to tune a TV receiver to 16 different channels.

As Max Huber, also a consumer

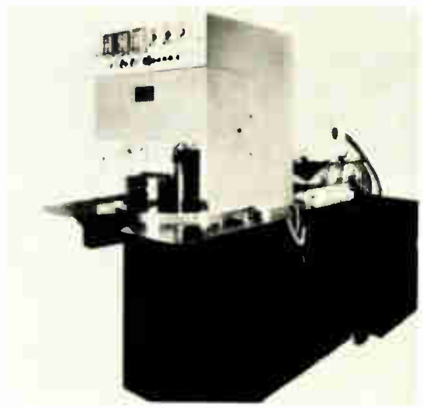


New products international

IC product manager at Siemens, explains it, the extra control capability is achieved by designing the chip to handle 120 commands, twice as many as its predecessor, the SAB3209. Each command consists of seven bits (one start bit and six information bits).

Using MOS depletion technology, the circuit comes in an 18-pin dual in-line plastic package. It operates off a supply of 11 to 16 V and dissipates about 500 mW. The chip size is approximately 14 mm². The circuit's unit price, Huber says, will be around $4 in large quantities.

Siemens AG, 8000 Munich 1, P. O. Box 103, West Germany [441]



A thermoplastic injection machine encapsulates coils and similar parts in a single operation at rates between 3 and 4 units per minute. The work table has two stations: while coil cores are loaded at one, plastic is injected at the other. Aviaplastique, 68 rue Lecourbe, 75015 Paris, France [463]

A linear power amplifier has an instantaneous bandwidth of 1 GHz. Gain ranges from 22 to 40 dB, flat within ±1 dB. Power ratings can be 1, 2.5, or 4 W, fully protected against overloads and mismatches. SCD-Nuclétudes, BP 117, 91400 Orsay, France [464]

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Sensitivity (rms)	20 mV	20 mV	10 mV	10 mV	10 mV	10 mV	10 mV	10 mV	20 mV	20 mV	20 mV	50 mV 1 mV
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Circle 163 on reader service card

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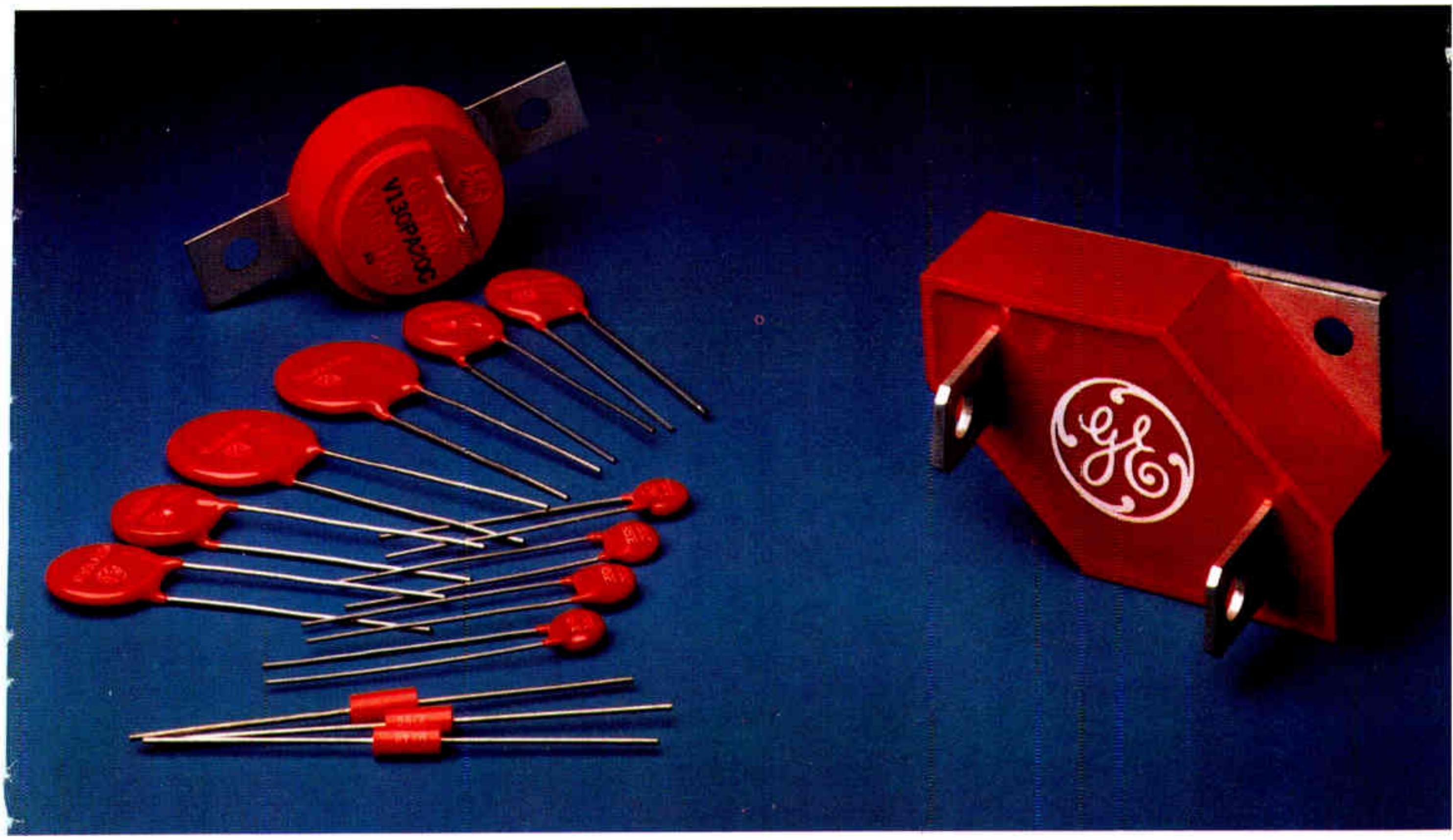

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GENERAL ELECTRIC

MOS ROM competition heats up

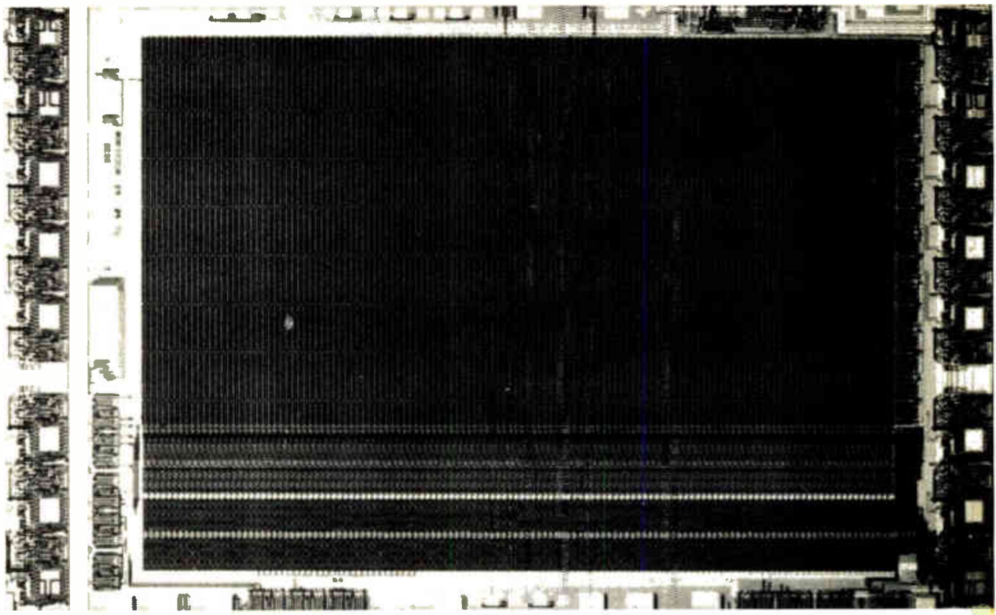
Spurred by microprocessor revolution, pinout options are growing with two standards to choose from now and a third promised

by Larry Armstrong, Midwest bureau manager

After years of shuffling along as the sleepiest segment of the memory market, read-only memories are beginning to present more of a challenge to both manufacturer and user. Late last fall, the metal-oxide-semiconductor ROM market started to splinter with the advent of Mostek Corp.'s innovative, high-performance 64-K part. Now Intel Corp. is challenging the other suppliers with controversial changes in both performance and pinouts of all its memories denser than 32-K bits [*Electronics*, Feb. 16, p. 44].

By the end of this year, users will be facing two distinct standards for big ROMs and erasable programmable ROMs. Manufacturers will be grouped around either the so-called Jedec pinout, promulgated last year by the Joint Electron Devices Engineering Council, or the newer pin configuration that Intel plans to use for virtually all new memories for the next four years. Then, some time next year, there is bound to be a third standard, an 18-pin version with multiplexed address and data pins—a space-saving, lower-cost mate for the multiplexed-bus microcomputers that are coming shortly from Intel, Motorola, and Zilog.

Differences. Further, performance variations will abound in each camp; both manufacturers and users disagree over whether the power savings to be gained with the new dynamic-periphery parts make it worth scuttling their easy-to-use, fully static designs. Mostek pioneered edge-activation techniques for an early static random-access memory and decided to require timing signals for its 64-K ROM as well. Now Intel has endorsed the concept: starting with 32-K ROMs and erasable PROMs, all its new parts will be edge-enabled.



All in the family. What TI, as well as other makers of ROMs, is aiming for is pin- and performance-compatible memory families. Shown is TI's 32-K erasable PROM.

Lurking behind the upheaval in the seemingly staid ROM and erasable-PROM markets is Intel's long-term strategy for memories, a plan that strives to match a system's memory components to each other and to microprocessors as well. Nor does the plan stop at ROMs: "Also coming, in the same pinout and with the same performance, are static RAMs," says Larry Jordan, marketing strategist for ROMs at Intel's Components division in Santa Clara, Calif., "and we see a number of other functions that fit into the same family."

In its 32-K ROMs and erasable PROMs, Intel has preserved compatibility with its existing 24-pin 16,384-bit products, though it has turned to a 28-pin package for 32-K and larger erasable PROMs, and for 64-K ROMs and up (see p. 104). "If the customer lays out his board for 28-pin packages, he can change his product's options—for custom Cadillacs and upgrades—without changing its printed-circuit board," Jordan explains. But Intel's upward path deviates from the pin configuration that is used in 32-K and 64-K parts already introduced by or available as samples from, among other producers, American Microsystems, Electronic Arrays, General Instrument, Mostek, Motorola Semiconductor, National, and Texas Instruments.

Pinout. The pinout difference is dictated by Intel's desire for an output-enable pin that, when hooked to a microprocessor, allows the

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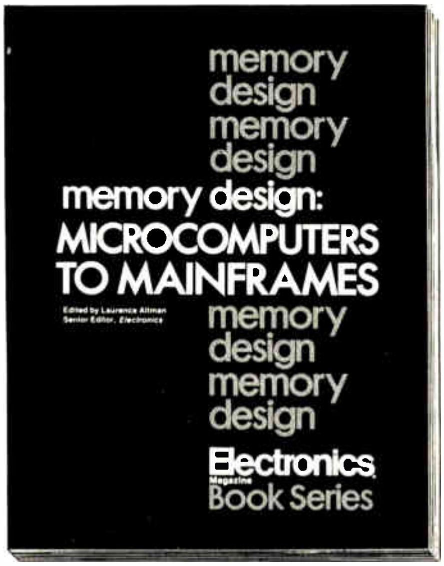

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telecommunications market has grown largely through acquisitions. In late 1976, it acquired Telecommunication Systems of America in Memphis, Tenn., a sales organization through which Northern is directly selling its SL-1, a large digital private-branch exchange, to major institutions and corporations. That same month, it acquired Cook Electric Co. of Chicago, a $30 million producer of telephone hardware. And earlier this year, Northern paid $23 million for Danray Inc. of Richardson, Texas, a producer of PABX and tandem switch equipment that is aiming for sales of $30 million to $40 million this year.

"We want a full line of telecommunications products not just for the regulated carrier market in the U. S., but also for the private systems market," says Scrivener, who sees the total telecommunications market expanding by as much as 25% annually. "We intend to acquire in the U. S. telephone company products and plant capacity as we require it—telco products that we are not now making in Canada and plant capacity as our sales grow."

Acquisitions. However, over the past year, Northern has also made a number of investments and acquisitions in the U. S. computer terminal and semiconductor industries. For example, Northern bought RCA Corp.'s 7.5% interest in Intersil Inc. of Santa Clara, subsequently boosting its holding in the semiconductor maker to 24%. That investment, says Scrivener, ensures the exchange of proprietary information for downstream planning and product development. "Everybody is looking over their shoulders and across the Pacific to the Japanese. This is part of our strategy for future developments, to have the LSI we need to put into our products and keep our whole processes competitive."

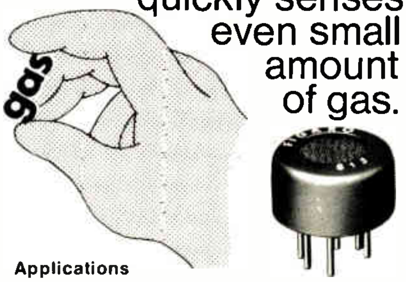
By the middle of next month, Northern hopes to have wrapped up its second investment in a computer-terminal manufacturer. It is negotiating to buy, for about $77 million in stock, Sycor Inc. of Ann Arbor, Mich., a producer of distributed data-entry and -processing terminals and related peripheral equipment. Earlier this year, Northern paid $15 million for a 12% interest in Data 100, a producer of cathode-ray-tube terminals in Minneapolis. The Canadian firm already has boosted its holdings in Data 100 to 19% and has the option of increasing its ownership to 35%.

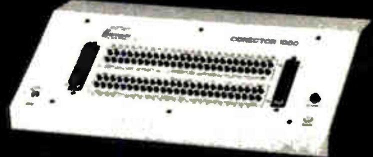
"It is not unlikely that there will be more acquisitions on the intelligent terminals side," says Scrivener. But this is likely to be after the summer, after Northern has sorted out its plans and strategies for Sycor and Data 100. These acquisitions, Scrivener adds, are to keep Northern in the market for what he calls the office of the future. Possible acquisitions in this area include manufacturers of other equipment that before long will be attached to the network as part of the total information system. Adds Scrivener, "This has high priority in our approach."

Digital market. Meanwhile, Northern also is banking on the success of its expanding line of digital switching and transmission equipment. "We have a lot of ability to put together for various types of customers very cost-effective all-digital networks," claims Scrivener. Also, he notes, the "all-digital" market is very large and now includes the Bell System, because of recent developments and their requirement to buy more from other than Western Electric. Yet another potentially large market exists for the E-phone, a totally electronic telephone handset now undergoing field trials and slated for possible introduction in the U. S. by mid-1979.

Scrivener is optimistic, too, about expanding Northern's business outside North America. While he sees such sales growing at least 20% and better, they are not likely to account for more than 10% of sales. "We're not going to build a lot of plants around the world," he insists. Rather, Northern's plan for expansion offshore is to license manufacturers who have the entrée to what he describes as the private telecommunications clubs around the world, or Northern will take a minority joint-venture position with local partners.

As for pursuing huge international orders, Scrivener wants to avoid that because "they are too risky and it would require us to commit too many of our resources away from the North American market." □





Regions

Is California losing its glow?

Inventory taxes and the high cost of real estate drive electronics executives to expand outside the state

by William F. Arnold, San Francisco bureau manager, and Larry Waller, Los Angeles bureau manager

To judge by the long lists of woes recited by many California electronics executives, the Golden State no longer wants them. Indeed, since business rebounded from the 1975 recession, there seems to be a marked interest among these firms in expanding both out of state and off shore rather than in the epicenters of electronics: the San Francisco Peninsula in the north and Los Angeles in the south.

To compile specific data on the trend—which some industry sources claim is nothing new—the American Electronics Association (formerly WEMA) is surveying its California members. Some answers are expected by May, says Ryal R. Poppa, AEA director and chief executive at Pertec Computer Corp. in Los Angeles.

While high taxes and stringent regulations that make it "too difficult to do business in California," as one executive says, are a longstanding gripe, several fairly recent developments make operating a company there even tougher, particularly in high-technology fields. The one most frequently singled out by industry executives is the soaring value of California property, which took off in 1974 and shows little sign of leveling off. Not only do electronics firms pay property taxes that are double or triple the levy of the early 1970s in some cases, but soaring home prices throughout the state have cut off the supply of out-of-state engineers and technicians.

The drying up of this vital source of professional personnel has a serious impact on the plans of a number of firms. Typical is Computer Automation Inc., founded and located in Irvine, the heart of booming Orange County. Its president, David H. Methvin, charges, "California is the third worst state for business behind only New York and Massachusetts."

Sensitive subject. On the tax question, always a touchy subject, California comes close to levying the stiffest total including corporate income, property, and inventory. According to figures compiled by Pertec, its 9% stands sixth in corporate income rates, behind the 12% of leader New York State-New York City. Others in order behind New York are Arizona, Connecticut, the District of Columbia, and Pennsylvania. The Massachusetts total is 5% [*Electronics*, Jan. 5, p. 112].

In property taxes alone, California taxes a very high $16.70 per $100 of assessed valuation, behind only Massachusetts at $18/$100. But the list does not stop there, for California firms pay an inventory tax every March 1 on materials, finished goods, and production equipment. Also, local divisions of companies headquartered elsewhere have to pay a "unitary tax."

But it is the inventory tax, although not as high as income and property, that slams high-technology firms, claims Methvin. Since it covers production equipment, companies that use such advanced gear as computer-based manufacturing and testing get hit the hardest. For instance, Methvin's firm manufactures printed-circuit-board testers in one division for outside sale and uses them itself in great numbers in its minicomputer operation. "The state taxes these on the basis of which is higher, cost or market value, so we get hit on the $100,000 price tag rather than the $50,000 cost."

San Francisco is No. 2 in living costs

A recent survey of 15 comparable major urban areas shows why electronics companies have a tough time recruiting out-of-state engineers: mortgage payments on the San Francisco Peninsula are easily the highest of the 15. Including such items as insurance, real-estate taxes, other taxes, and transportation, the peninsula area came in second behind pricey lower Connecticut but ahead of lower New York State, Chicago, Minneapolis, and Portland, among other areas.

The survey, which excludes food and clothing costs, was performed by Runzheimer Affiliated Services of Rochester, Wis., a firm specializing in comparing living costs for corporations. Although the survey was pegged to a $39,000 executive with a wife and two dependent children, president Rufus Runzheimer says the costs would be roughly proportional for an entry-level engineer or a research director.

The survey's total annual standard costs for lower Connecticut-Westport came to $28,799. In second through sixth place were San Francisco-Burlingame, $27,014; lower New York State-Rye, $26,927; Chicago-Winnetka, $26,587; Minneapolis-Edina, $24,574; and Portland-West Slope, $22,341. Dallas-Richardson was 13th with $19,667 followed by Atlanta-East Point, $19,373, and Jacksonville, Fla., $18,284.

Sacramento to act

The laments of California businessmen evidently have been heard in the State Capitol at Sacramento, where both Gov. Edmund G. Brown Jr. and legislative leaders are pushing for changes. Brown lists inventory tax relief high among his priorities this year, and a chief aide responsible for legislative liaison told *Electronics:* "We'll have an inventory tax relief bill in 30 to 60 days. We have the support. The question is what form it will take."

The high cost of housing on the San Francisco Peninsula is the main reason Intel Corp. is relocating its Memory Components division and the single-board-computer part of its Microcomputer Systems division to Portland, Ore., says Gordon Moore, president. "It's the principal problem in trying to grow in the Bay area," he says, because young engineers from out of state are frightened off by the stratospheric house prices.

Housing, the tax environment, and the unavailability of professional people are making it hard for electronics companies to prosper in Silicon Valley, agrees Floyd Kvamme, vice president and general manager of National Semiconductor Corp., Intel's Santa Clara neighbor.

"The real issue in California is housing" Kvamme says. "I'm told that if you eliminate the housing parameters, things like food, clothes, and transportation aren't that bad out here—the problem is getting into a house," meaning the down payment and monthly payments.

But Kvamme also criticizes high California taxes, particularly state capital gains taxes, which he understands to be worse than others. "The whole tax environment is, in Zschau's words, killing off or at least wounding the golden goose," he declares, referring to testimony before Congress by Edwin V. M. Zschau, chairman of System Industries Inc. in Sunnyvale, representing the AEA [*Electronics*, Feb. 16, p. 42]. "California should take a look and ask if it's not doing the same thing as Massachusetts in killing off high-technology companies," he says. □

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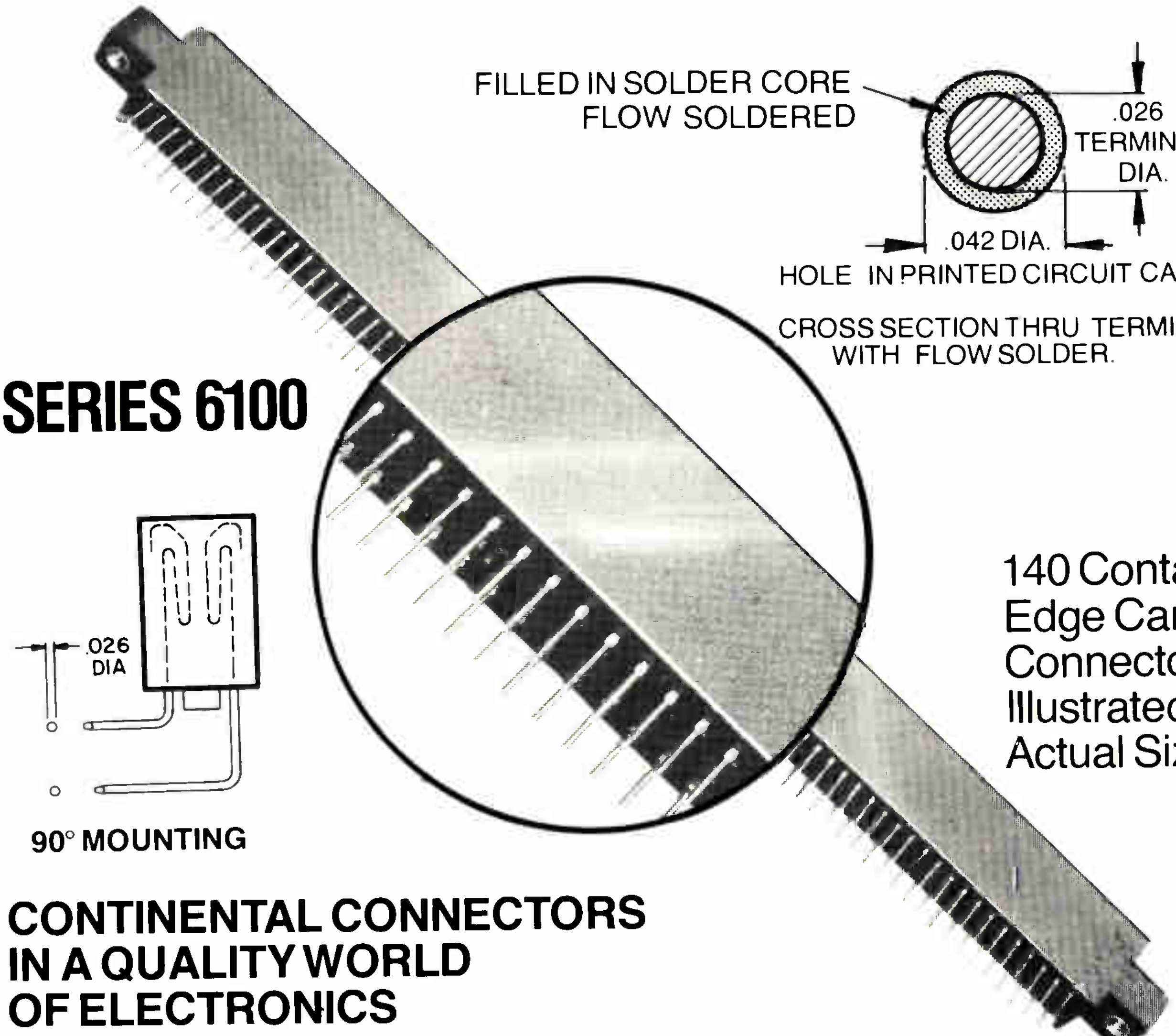

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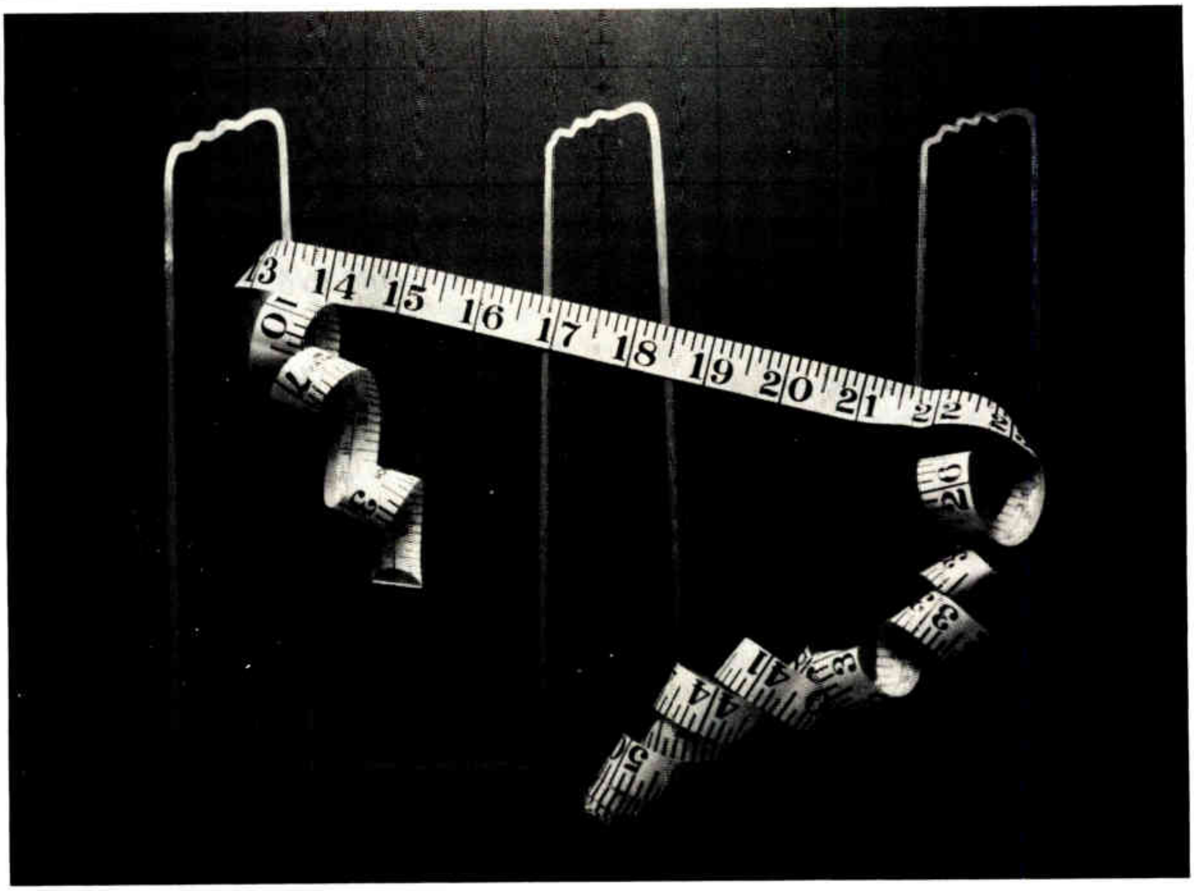


Microseconds and megahertz: a new measurement series

by Stephen E. Scrupski,
Instrumentation Editor

In recent years, instruments for measuring time and frequency have made significant advances that have raised them to an unprecedented level of sophistication. The stream of innovations has included counter-timers that adjust their trigger levels; oscilloscopes that measure time intervals precisely; and spectrum analyzers that perform measurements directly and display results on the screen, using the displayed spectrum primarily for reference rather than as the basis for measurement itself. There have also been improvements in frequency sources, like the triggered phase-lock oscillator from Hewlett-Packard.

As engineers are well aware, these changes have been largely the result of the fast pace set by digital circuits. By now, though, semiconductor makers are concentrating more on the circuit density and less on the speed of their chips, so there has been a corresponding let-up in the frequency race among instrument manufacturers—today's oscilloscopes, for instance, perform quite well for the applications. So it seems as good a time as any to survey the time- and frequency-measurement field and see what the changes mean to the engineer.

Developments here, in counters and spectrum analyzers as well as oscilloscopes, make an interesting contrast to developments in digital multimeters and other voltage, current, and resistance instruments. Great strides have been made in the basic technology

Part 1

Making accurate measurements with counters and timers

by Jan van der Windt and Jan Ericsson,
Philips Electronic Industries, Järfälla, Sweden

☐ In principle, a digital counter is just a box that counts the number of events occurring during a precisely defined time interval. But in practice, it has to be quite complex if it is to deal at all accurately with rapid trigger events like sine-wave zero crossings in frequency measurements or clock pulses in time-interval measurements made on high-speed digital circuits.

In fact, some of today's counters are already using microprocessors. But even the less sophisticated require their users to have some grasp of how their logic, counting, and input conditioning circuitry operate.

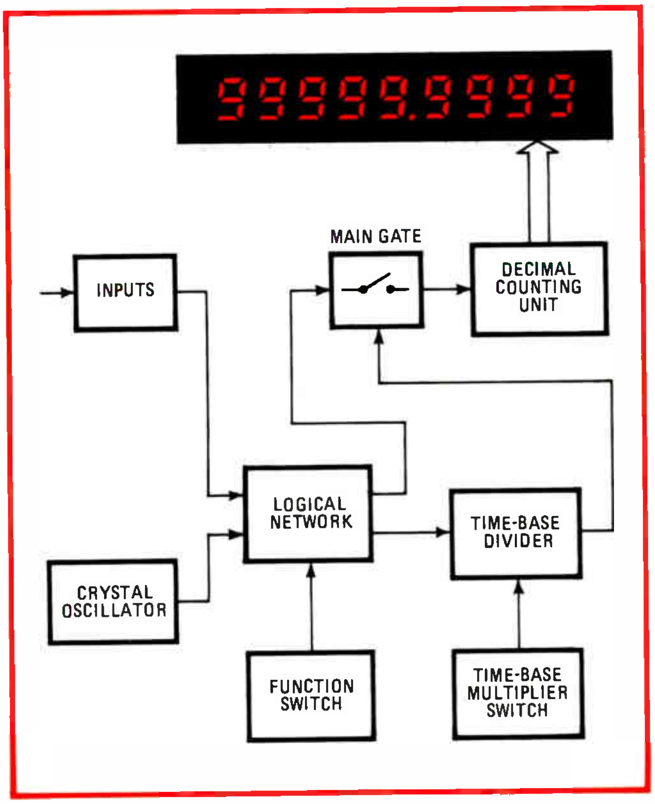
The instruments have come a long way since the 1950s, when the first digital counters were developed to totalize random counts in nuclear radiation measurements. Those were bulky machines that needed 100 or so vacuum tubes and had odd-looking displays, since neither the Nixie tube nor the light-emitting diode had yet been invented. But more compact, transistorized versions appeared in the late 1950s, and by the late 1960s diode-transistor and transistor-transistor logic had started the decline in prices and the improvement in performance that the microprocessor is currently showing every sign of continuing.

In today's typical counter, the signal to be measured is connected to input circuitry that converts it to standard logic levels (Fig. 1). Then it is routed through a logic network along a path that varies with the parameter to be measured—frequency, period, time interval, and so on. Of these the most basic is frequency.

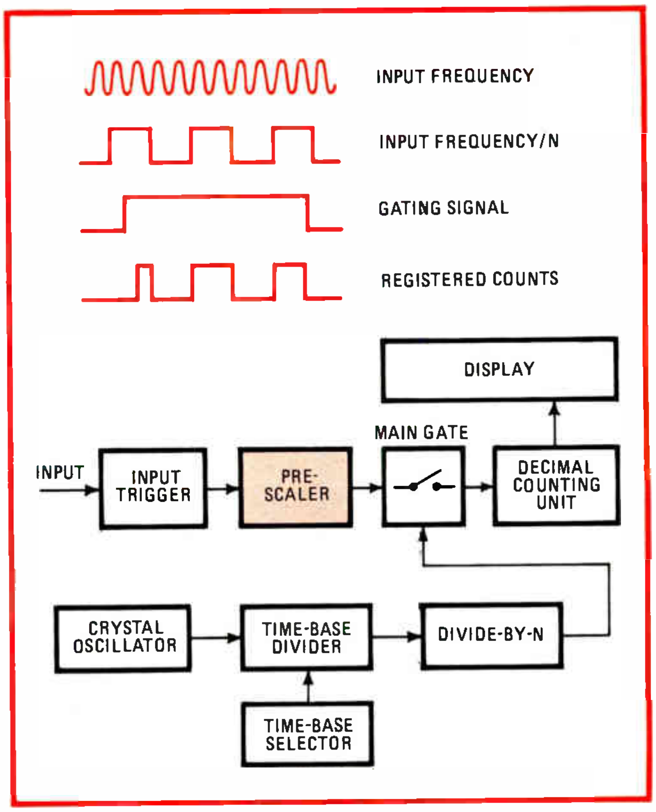
Measuring frequency

The simplest way to measure frequency is to pass the unknown signal through the main gate as it opens and closes in response to an accurate time-reference gating signal. This gating signal is set by the time-base selector, normally in decade steps, and is derived from the crystal oscillator by a time-base divider. The output from the main gate is a number of pulses that directly represents the frequency of the input signal, since the gate time is a decimal fraction or multiple of 1 second.

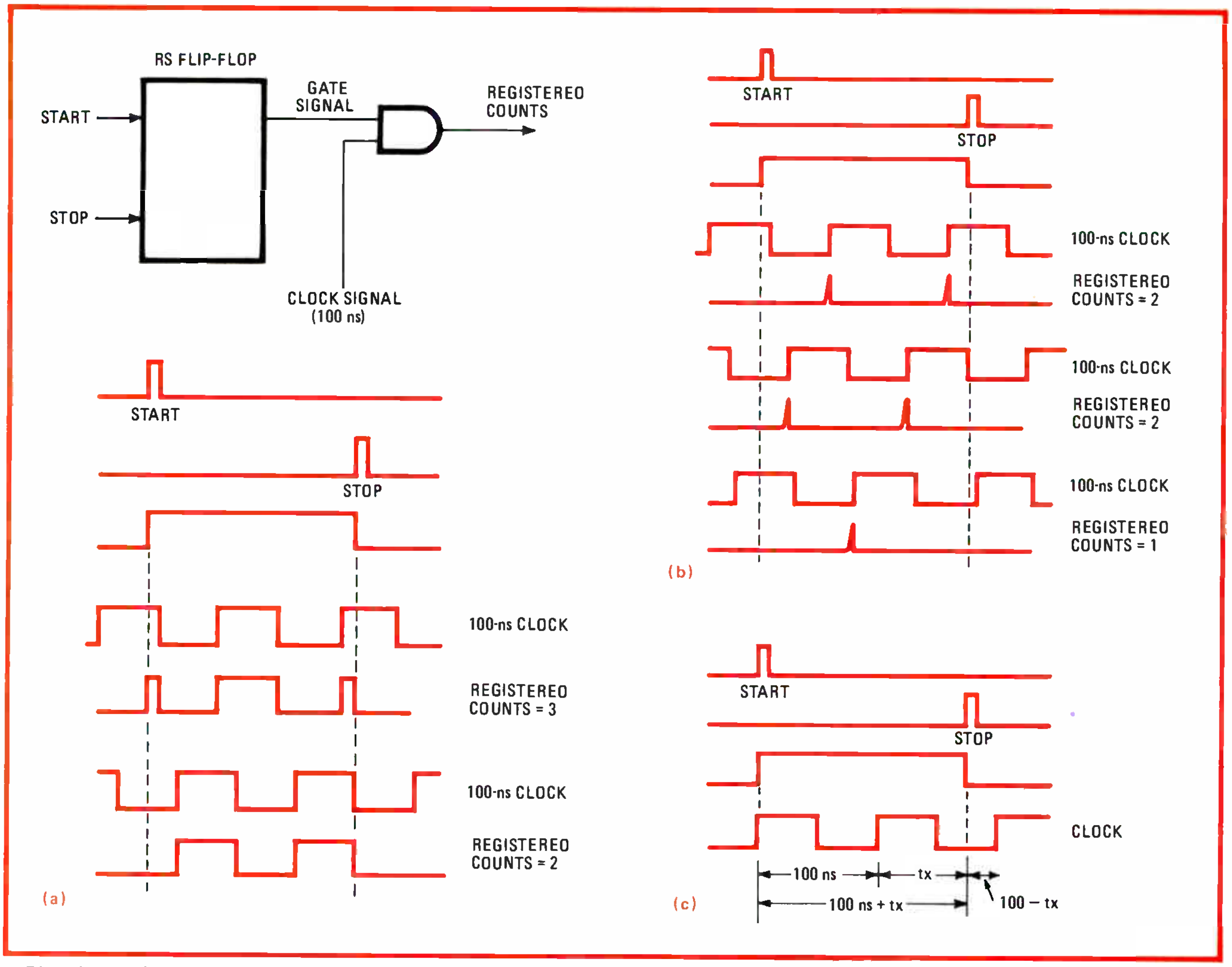
The pulses are counted by and stored in the decimal counting unit. When a measurement has been



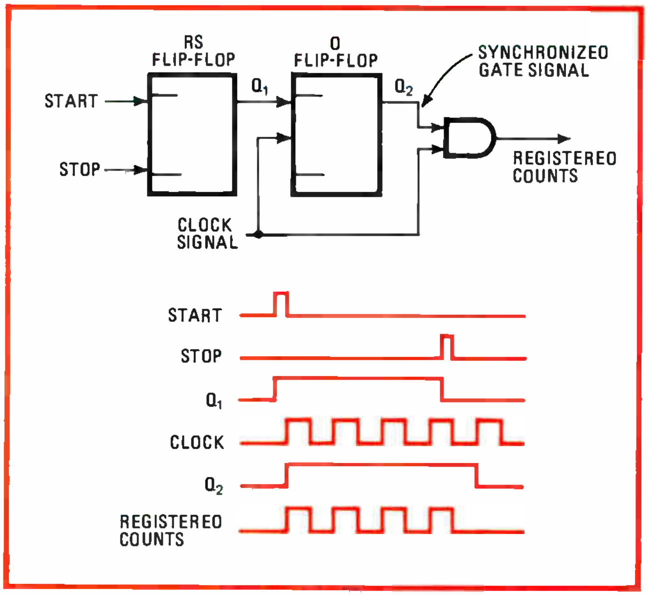
1. Basic counter. To measure frequency, inputs are converted to standard logic levels and enter the main gate, which is held open for a preset time by the time-base divider circuit. The gate's output is a number of pulses corresponding to the input frequency.



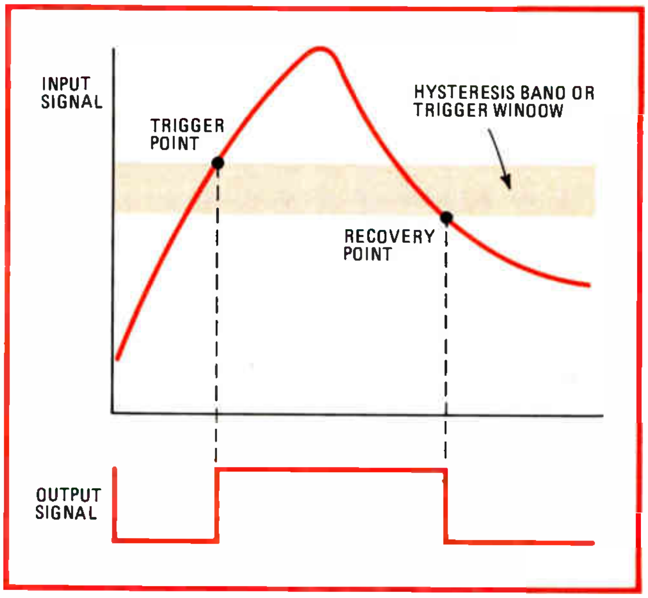
2. Prescaled counting. For inputs beyond the frequency range of the basic counting circuits, prescaling is used. Input signals are divided in frequency by a known factor by the prescaler and counted, and the resulting pulses are multiplied by the same factor.



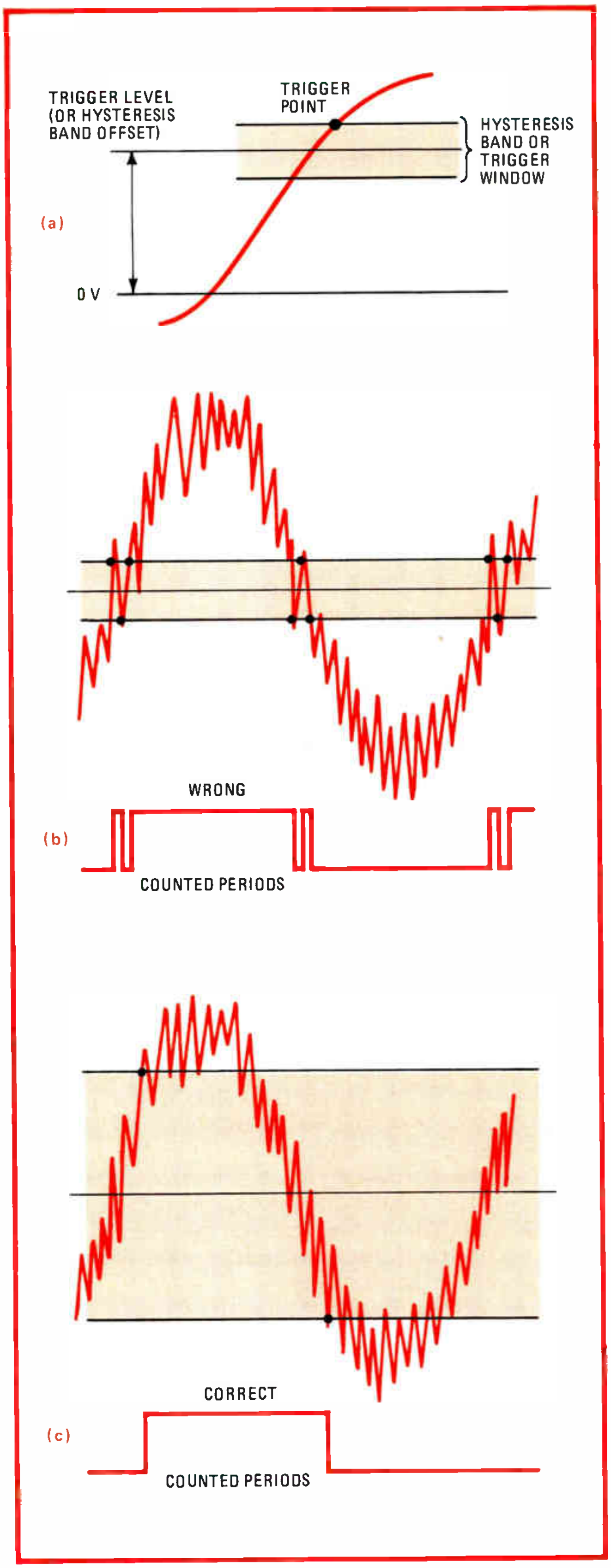
3. Time intervals. Measuring brief time intervals, clock pulses may be truncated by the gate, and when that happens, errors will result (a). A more accurate technique is to count leading edges of clock pulses (b) and then use interval averaging (c).



4. Synchronized gating. A circuit that acts on the edges of the clock pulses can be implemented with two flip-flops. The circuit thus responds to almost zero-width start and stop pulses and can be used to measure events shorter than the clock period.



5. Hysteresis effects. Hysteresis in the trigger circuits results in a voltage difference between trigger and recovery points. The range between the upper and lower thresholds is the hysteresis voltage, which must be taken into account with complex input signals.



6. Spurious counts. Triggering does not occur at the specified trigger level, but rather at the top of the hysteresis band (a). If the hysteresis band is narrow, a noisy signal will make extra transitions (b). Input attentuator can expand hysteresis band (c).

completed, the display is updated with the new result.

A universal counter/timer allows other measurements besides frequency counting. In the period, or duration, mode, the input signal is routed to open and close the main gate, and the number of gated clock pulses is registered in the decimal counting unit. These clock pulses represent time units—normally 100 nanoseconds each, since the oscillator in most cases operates at 10 megahertz. In the time-interval mode, start and stop inputs open and close the main gate.

Direct-gated, prescaled, or converted

This direct-gating method of frequency measurement has limitations, however. It is possible with present technology to make a direct-gated counter up to 1,000 MHz, but it is seldom done, since 1,000-MHz main-gate and decimal-counting circuits are very expensive.

A more economical solution is to divide, or prescale, the incoming frequency down to a frequency that can be handled with standard transistor-transistor- or emitter-coupled-logic circuitry. The prescaling can be done with any factor—4, 8, 10, and so on—but the number of periods per second that result is now only a specific fraction of the unknown frequency (Fig. 2).

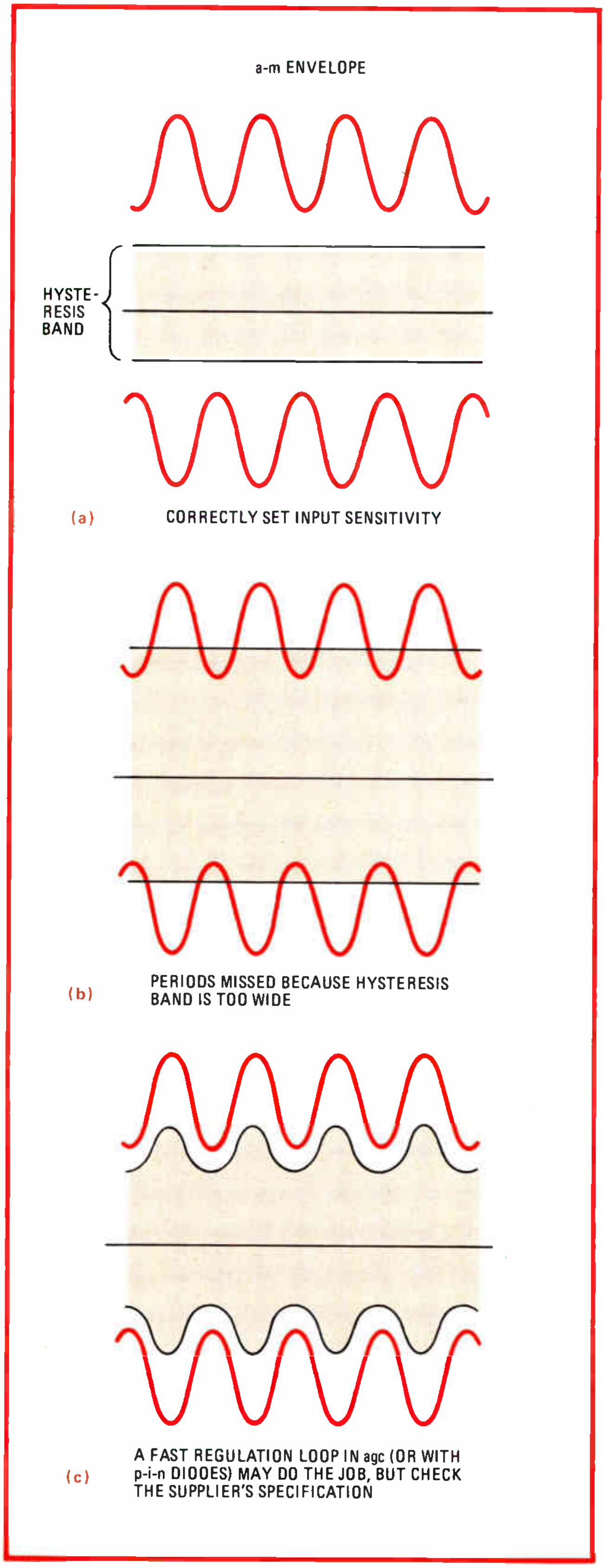
To obtain the proper result, the counted pulses must be multiplied by the prescaling factor. Seemingly the easiest way to do this is to count the pulses during a fixed time interval, usually a multiple of a gate time used with direct gating. But then either resolution or measuring time must be sacrificed, since the resolution—the number of pulses counted—depends on the gate time. A given frequency produces 10 times as many pulses in 1 second as in 0.1 second.

On the other hand, even directly gated counters have to pay for a meaningful resolution by using a very high-stability oscillator. Their ability to produce a measurement of 500 MHz ±1 hertz is only meaningful if their time base has an accuracy on the order of 10^{-9}. For this reason, 500-MHz direct gating is mostly restricted to high-speed systems counters, such as the HP5345A and the Philips PM6650, while 1,000-MHz direct gating has not been used at all. With present technology, prescalers up to 1.5 gigahertz are possible, while new gallium-arsenide field-effect-transistor developments may raise this upper limit to 4 GHz or so within a few years.

To count even higher frequencies, the kind of conversion techniques found in a radio receiver are employed. The commonest use transfer oscillators and heterodyne converters. With the manual transfer-oscillator technique, and with appropriate radio-frequency hardware for the mixer, it is possible to measure frequencies even higher than 300 GHz. With the automatic-heterodyne or automatic-transfer oscillators, the frequency range is normally limited to around 30 GHz.

There are two types of time-interval measurements: single (one-shot) and repetitive. A one-shot time interval can, of course, only be measured in the single time-interval mode, so that resolution is limited by the counter's clock frequency. Medium-priced counters mostly have a resolution of 100 ns, but more sophisticated counters have single-time resolutions of 10 ns or less.

If the time interval to be measured is from a repetitive



7. Amplitude modulation. If the signal is amplitude-modulated, the a-m envelope should enclose the hysteresis band (a). A hysteresis band that is too narrow (b) will result in uncounted periods. An alternative is automatic regulation of the hysteresis band (c).

signal, the time-interval average technique can be used. Today this is even found in some medium-class counters, such as the Philips PM6622 and HP5308.

If an engineer tries to measure a time interval of 175 ns with the normal single time-interval function, and if the counter has an internal clock frequency of 10 MHz (equal to 100-ns resolution), the result will be either two or three counts, depending on the phase relation between the time interval and the clock. The problem is that the gate signal sometimes truncates the clock pulses at the start and stop of the measurement, and a fast enough counter will count these truncated pulses, producing an error of more than 1 count (Fig. 3a).

Averaging over several intervals will not improve the accuracy of the measurement. The answer is to count only the leading edge of the clock pulses (Fig. 3b), which makes it possible to deduce a much more accurate count. The time interval can be expressed as $(100n+t_x)$ns, where n is an integral number of 100-ns-interval clock pulses and t_x is a fractional part, less than 100 ns (Fig. 3c). At least one clock edge will be counted during each interval, and the probability of counting a single additional count is proportional to the time t_x.

Edge-sensitive counting

For instance, in the foregoing example, the probability of counting two input pulses during the 175-ns interval is greater than its counting one pulse. In fact, there is a 75% probability for two counts and only 25% probability for one count. With 10,000 measurements, 2,500 will produce one count and 7,500 will produce two counts. Thus the total will be 17,500 counts, which is divided by 10,000 to give 1.75 counts. Since the clock interval is 100 ns, this corresponds to 175 ns.

Several circuits can implement an edge-triggering system. The simplest synchronizes the gate signal with the clock signal (Fig. 4), acting on the edges of the clock pulses. It corresponds to virtually zero-width pulses and can measure time intervals much shorter than the clock period. Resolution and accuracy is improved by a factor of $N^{1/2}$, where N is the number of averages taken.

Time-interval averaging can be used if:

- The signal is repetitive.
- The repetition frequency is not synchronous with the internal clock or a subharmonic of the internal clock.
- There is a minimum time between the stop and a start of the next interval, normally on the order of one or a few pulses of the internal clock.

To fully exploit the potential of time-interval averaging, start and stop channels must be accurately matched as to both rise time and propagation delay. Then this technique can measure even 100-ps time delays.

The specified accuracy of any counter represents a maximum attainable value, since noise, distortion, interference, and input-control setting errors can all falsify the count. In today's frequency counters, the counting circuitry uses standard TTL, ECL, and/or metal-oxide-semiconductor digital integrated circuits, which can only count input signals having the right pulse form and amplitude—in other words, the right logic levels.

In practice, though, measurements must be made on all types of signals, with amplitudes that may range from a few millivolts to many volts and waveforms that may vary from a clean sharp pulse to a distorted sine wave. This variability is reduced to the required uniform shape by input signal-conditioning circuits like attenuators, amplifiers, and limiters. But the conversion is inevitably imperfect and often leads to significant errors. In fact, it is often the sophistication of the input signal conditioning, rather than the quality of the time-base crystal oscillator, that determines the counter's accuracy.

Hysteresis

Correct triggering, in particular, is dependent on the signal-conditioning circuits. It requires proper use of the hysteresis of the trigger circuit (Fig. 5). This circuit's function is to produce a step response, or pulse output, at the point when a gradually changing input signal crosses a certain threshold value. This threshold value, however, is higher for increasing than decreasing input voltages, and the range between the lower and upper threshold limit is the hysteresis voltage.

In a plot of input-voltage characteristics versus time, the hysteresis voltage appears as a band, or trigger window. (But note that because of input amplifiers, the hysteresis voltage band is lower at the counter's input than at the actual trigger circuits.) The width of the hysteresis band is the same as the counter's input sensitivity in peak-to-peak millivolts. For example, an input sensitivity specification of 10-mv root mean square can have a typical value of 6-mv rms, which equals a hysteresis voltage of 18 mv peak to peak. An input attenuation, by reducing the signal amplitude, in effect makes the hysteresis band wider and the counter less sensitive to false triggering. Thus, a flat frequency characteristic implies a constant hysteresis band for all input frequencies—but note that some counters do specify deteriorated sensitivities at maximum operating frequency.

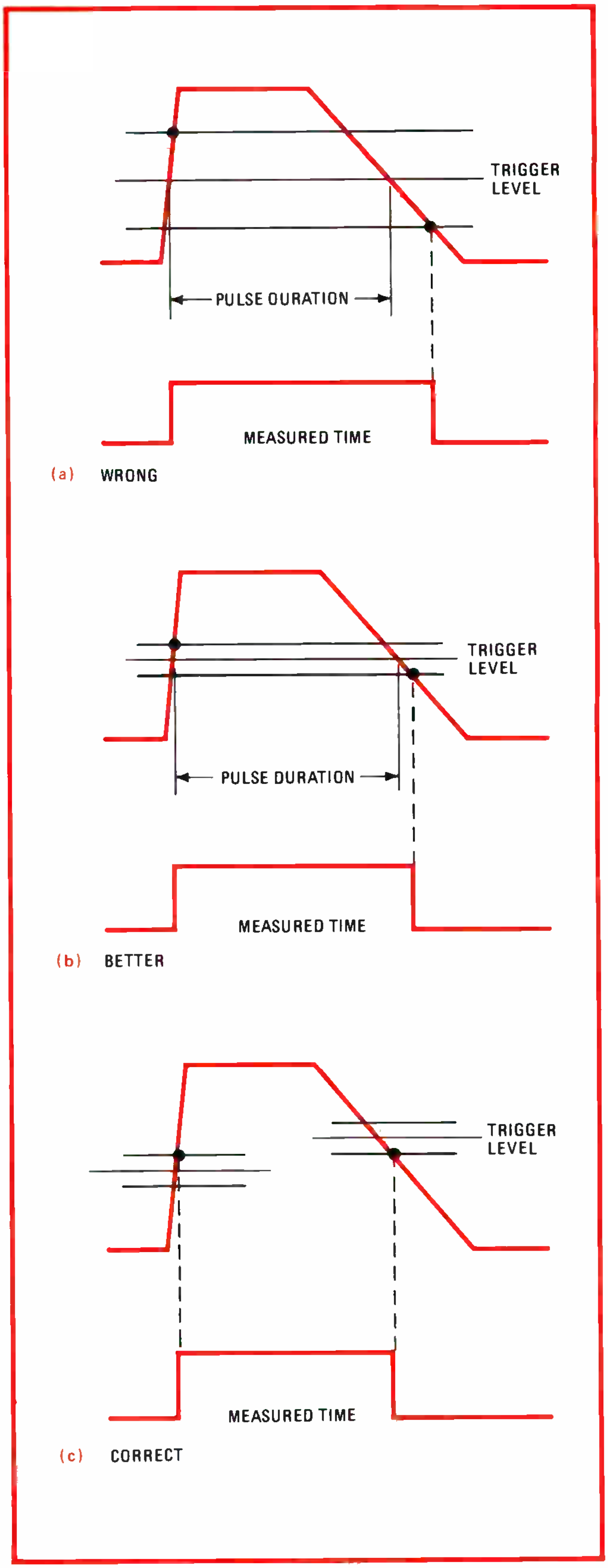
Incidentally, triggering does not occur at the trigger level, but at the trigger point (Fig. 6a). The trigger level is the hysteresis-band offset.

Although counters are used to measure both frequency and time interval, these two different measurements have contradictory requirements when it comes to avoiding spurious counts. For instance, frequency measurement needs continuously variable attenuators, and time-interval measurement does best with none.

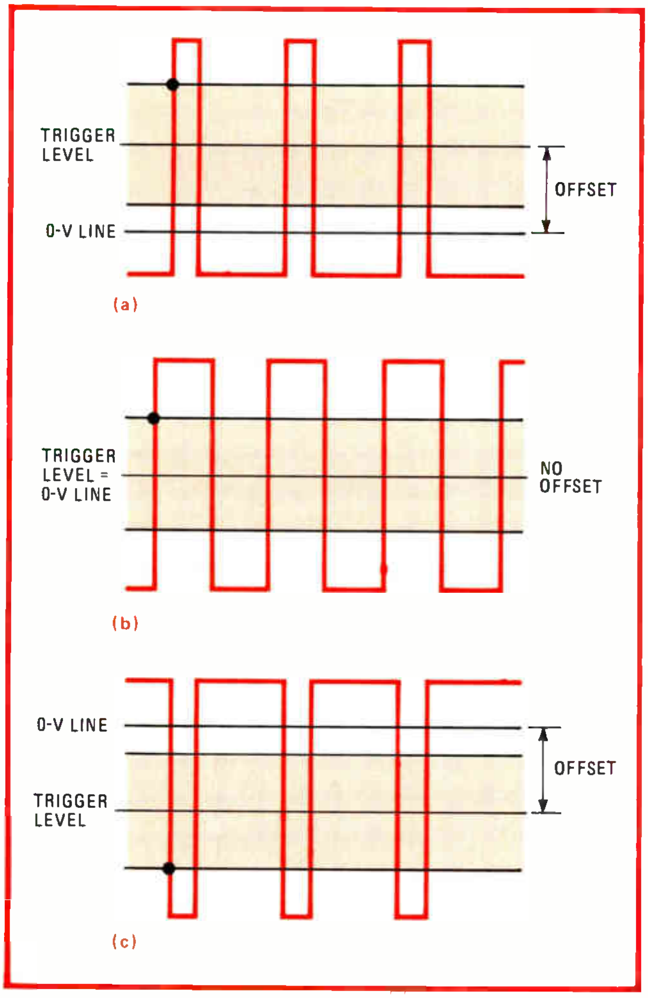
In measuring the frequency of a given input signal more sensitivity than is needed for correct triggering is undesirable. Otherwise, noise, distortion, or interference may cause the input signal to cross the hysteresis band more than once per period (Fig. 6b). But with input attenuation, the band can be expanded, so that noise with an amplitude below the hysteresis voltage does not trigger the input (Fig. 6c). Because of this, the hysteresis band is sometimes called the noise-immunity band.

How much attenuation?

A hysteresis band of about 50% to 70% of the peak-to-peak input signal usually is ideal. Since input signals can have any amplitude, continuously variable input attenuation is generally best. This can be obtained with potentiometers up to about 100 MHz, with automatic-gain-control circuits up to about 1 GHz, and with p-i-n



8. Slope variations. Different slopes of the edges of input signals can cause variations in triggering. Here, the narrower the hysteresis band, the less the error. But the errors can be compensated for by offsetting trigger levels with half the value of the hysteresis band (c).



9. Changing duty cycles. The trigger level should be variable if frequency-measurement inputs are to have high or low duty cycles. The trigger level offset then can track the inputs to assure that no pulses are missed during the counting process.

diode attenuators up to about 10 GHz. The last of these also tolerates overloads better than agc circuits do.

More specifically, when only unmodulated sine waves are to be measured, all types of continuous controls are suitable. But to measure the frequency of amplitude-modulated signals, potentiometers are best, because they allow precise setting of the signal level so that no period is missed (Fig. 7). Since potentiometers are limited to 100 MHz, automatic regulating systems are used with p-i-n diodes or agc circuits for higher frequencies.

Time-interval measurements, on the other hand, demand a narrow hysteresis band. By means of slope selection and trigger-level setting, the trigger point may be positioned at any point on the signal slopes. Different signal slopes at the start and stop trigger points cause different delays between the trigger-level crossing and the actual trigger point (Fig. 8). A narrower hysteresis band will be crossed in a shorter time, reducing differences in delay. Thus, to minimize trigger errors, an input attenuator should not be used. However, the counter's basic trigger-level dynamic range, say -2.5 V to $+2.5$ V, often makes the use of an attenuator necessary for signals of higher amplitude. To know what the new offset range is when using an attenuator, it is necessary to have a fixed device with a known attenuation factor, even though it degrades the trigger delays.

Virtual elimination of the hysteresis band is possible by means of automatic compensation of the hysteresis voltage. When making time-interval measurements, the actual trigger level is compensated, or shifted, by half the value of the hysteresis band—the voltage shift is negative after selection of a positive trigger slope, positive for negative slopes. These autocompensation networks are found in more elaborate counters, such as the HP5327 and the Philips PM6650.

If frequency measurements are to be made on sine-wave signals only, fixed ac-coupling and center-crossing triggering is best, being economic, stable, reliable, and, through elimination of extra controls, easy to operate. But if pulsed signals with a very high or low duty factor are involved, some trigger level offset facility is needed. This might take the form either of a variable control or a switchable fixed offset.

Frequency, or repetition-rate, measurements on pulses with a changing duty cycle are even more remote from the simple frequency meter. For this type application, a dc-coupled input stage plus continuous trigger-level control is needed (Fig. 9). An operator finds it hard to optimize settings using two variable potentiometers simultaneously, one to control trigger-level offset and the other for attenuation. So instead, this type of input has a fixed-step attenuator (i.e. $\times 1$, $\times 10$, $\times 100$). It is at this point that counters intended for more general applications start to sacrifice noise immunity.

Counter-timer considerations

In counter-timers capable of measuring frequency and time intervals, two inputs are needed to define the opening and closing of the main gate. These inputs are usually dc-coupled, while a trigger slope selector is added to trigger on either positive or negative slopes.

In low-speed counter-timers, to economize on input circuitry, the stop channel often has a lower speed than the start channel, which also is used for frequency measurements. This need not be a drawback if the stop channel's rise time is better than the ± 1 digit error corresponding to clock resolution (usually ± 100 ns).

Faster counter-timers featuring time-interval averaging are able to measure times much shorter than the ± 1 clock pulse. This kind of resolution makes much heavier demands on the input channel performance. The matching of the start and stop channels becomes of the greatest importance. If the propagation delays or rise times of the two channels are at all different, a time error is added. This error cannot be eliminated by averaging, since it recurs in every sample.

The best way to check channel matching is to measure the time difference in their outputs. A power splitter and two cables of equal length should supply the same pulse to both channels. Also, the two trigger levels should be set equally. To ensure this, both levels should be preset to 0 V, with an internal short circuit to ground, and then a very fast pulse crossing 0 V from a negative to a positive voltage should be applied. Good timer-counters will show a deviation of much less than 1 ns. □

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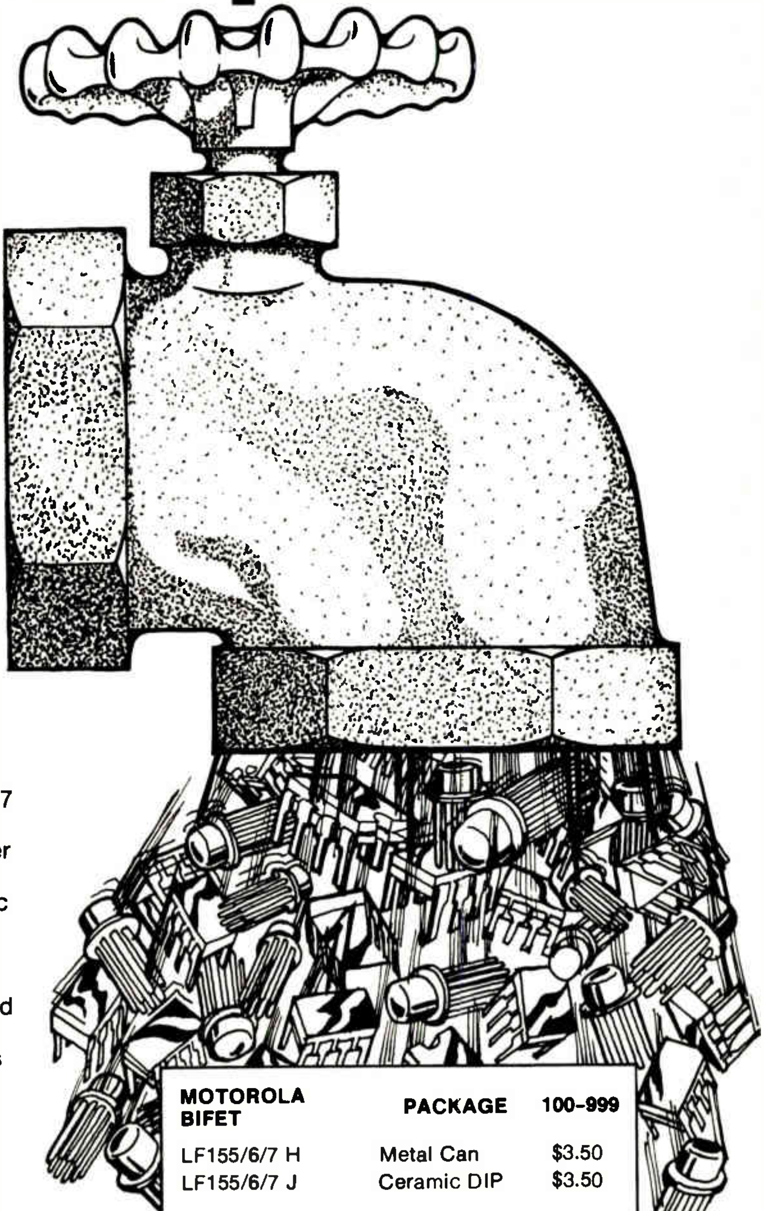

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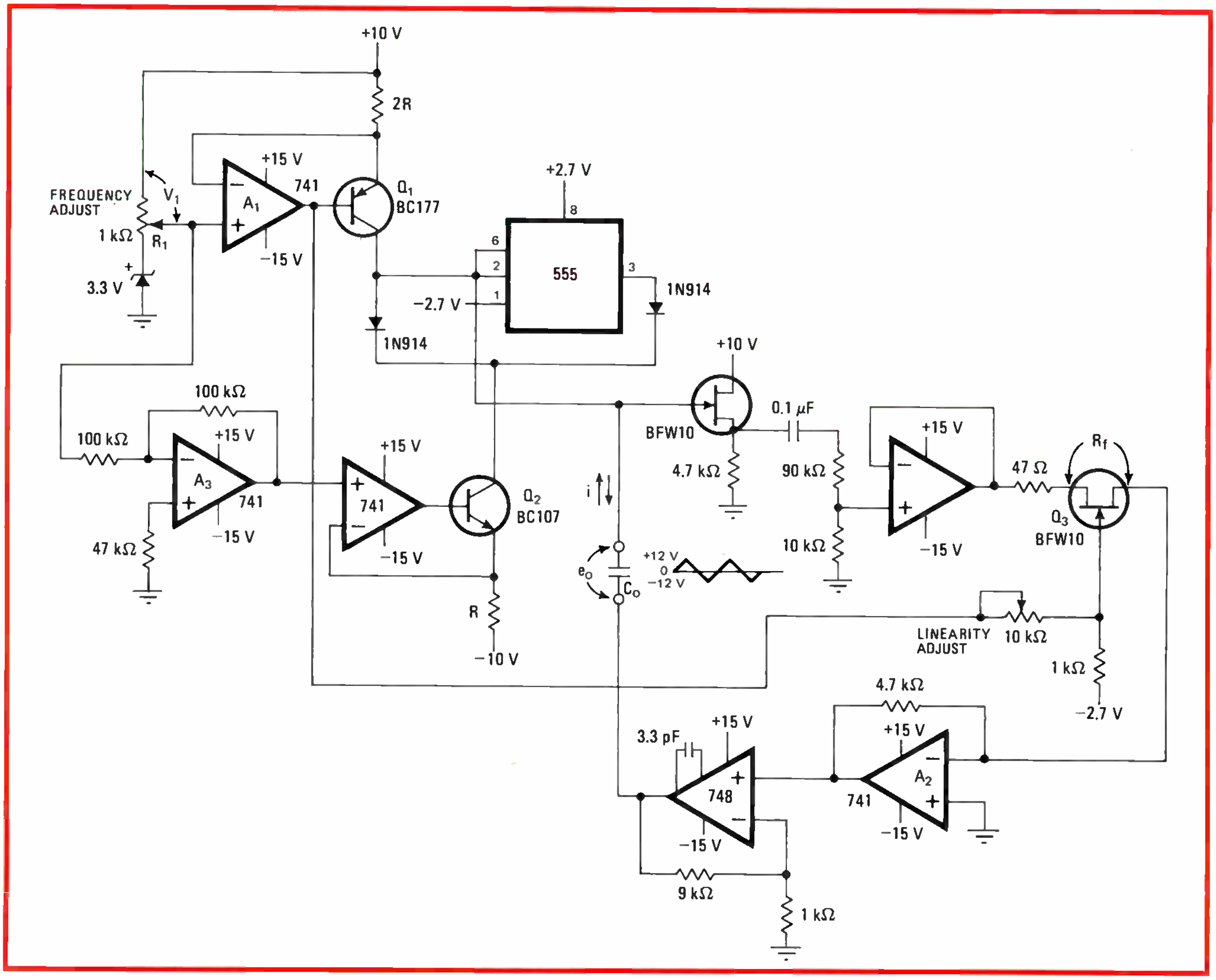
Capacitance multiplier extends generator's sweep ratio

by A. D. Teckchandani
Eastern Electronics Ltd., Faridibad, India

Most low-frequency function generators can produce triangular waves over a frequency range of 100 to 1 by using the standard method—constant-current charging and discharging of a fixed-value capacitor. But the sweep ratio, or the ratio of the maximum to the minimum output frequency, can be extended to 500 or more by varying the magnitude of the current from the generators and the capacitance simultaneously. Using one potentiometer both to control the current source directly and to adjust the capacitance by means of a capacitance-multiplier circuit allows a greater frequency range, because the ratio of current to capacitance is varied over a wider range.

The frequency, or rate, at which a capacitor charges or discharges is directly proportional to the magnitude of the current from the generators and inversely proportional to the capacitance; that is, $f = Ki/C$, where K is a constant. This circuit expands the sweep ratio by ensuring that an increase in i is accompanied by a decrease in C, and vice versa.

The circuit shown below is so configured that the current sources formed by stages A_1, Q_1, and Q_2 aid in determining both the oscillation rate of a 555 timer, wired as a double-ended comparator (Schmitt trigger), and the amplitude of the current through timing capacitor C_o. The frequency of oscillation is also determined by stages Q_3 and A_2 and is equal to:



Greater range. Simultaneous variation of current-source (A_1, Q_1, Q_2) magnitude and capacitance charged by source extends generator's sweep ratio. R_1 adjusts current source directly; capacitance is varied by means of capacitance multiplier (A_2, Q_3).

$$f = 1.5i/VC = i/3.6C$$

for $V = 5.4$, where:

V = supply voltage of 555

$C = C_o(1+|A_v|)$

$A_v = 4{,}700/(47+R_f)$ = voltage gain of A_2

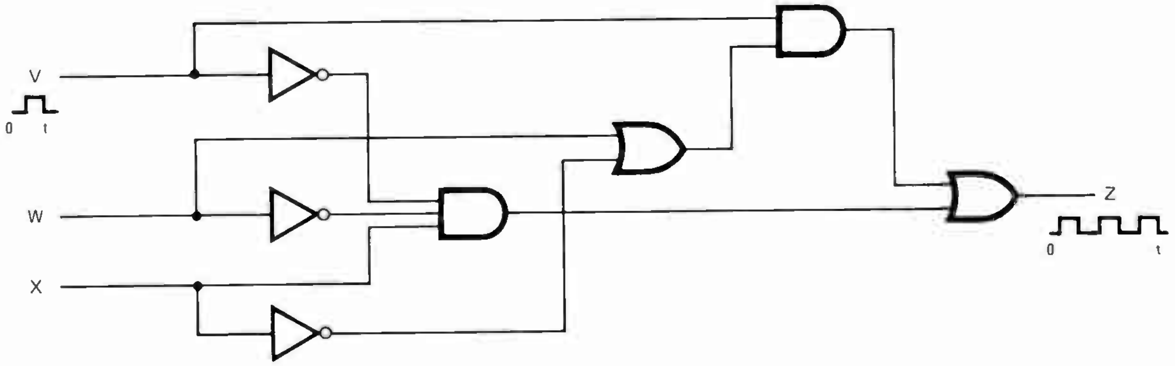
R_f = on resistance of Q_2.

R_1 controls i, the current value being equal to $(10-V_1)/2R$. R_f is controlled by the voltage appearing at the gate of Q_3, which in turn is controlled by A_1 and ultimately R_1. Therefore, when there is an amplification in the A_2–Q_3 loop, the effective capacitance at the output of Q_1 increases by A_vC_o. (The phenomenon of output capacitance increasing with active-device gain was first observed in the Miller effect). Capacitance multiplication is thereby achieved by varying R_1.

The frequency range of the triangular waves that can be produced by this circuit varies from about 10 cycles to approximately 5,000 cycles. ☐

MORE TO FREQUENCY MULTIPLIER

As readers may have noted in R. J. Patel's article in the previous issue, "Frequency multiplier uses combinational logic" [Designer's Casebook, March 16, p. 119], the function $Z=V(W+\overline{X})+\overline{V}\overline{W}X$ cannot be implemented with just two AND gates and three inverters, as was diagrammed in Fig. 1. The correct implementation is shown below.



Digital interpolator extends number of synthesizer channels

by Jo Becker
University of Stuttgart, Institute of Biomedicine, Stuttgart, Germany

The extensive modifications needed to increase a commercial or already built frequency synthesizer's channel-generating capability over a given range can be a designer's nightmare. But the addition of only a counter and a few gates will multiply the synthesizer's channel capacity 5 to 10 times—and does so almost without touching the basic circuit.

The technique used for channel multiplication may be understood with the aid of a block diagram of a typical frequency-modulated synthesizer (a). Here, the voltage-controlled oscillator generates 80 carrier frequencies, or channels, in the 133.3-to-135.275-megahertz band, where the channel separation is 25 kilohertz. The channel spacing is determined by the value of f_a. The output frequency is:

$$f_o = f_q + Nf_a$$

where f_q is generated by a local crystal oscillator and N, an integer, is selected by a binary-coded-decimal switch array and a suitable BCD adder, plus a variable frequency divider and a standard feedback circuit that uses a phase-locked loop. An additional BCD switch array control makes it possible for the synthesizer to generate a frequency, f_o, such that:

$$f_o = f_q + (N+M)f_a$$

and this option is useful in cases where the synthesizer is employed in a receiver circuit to generate separate transmitting and receiving frequencies.

To enable the VCO to oscillate at frequencies between the channels, noninteger values of N or M must be generated, and therefore it is necessary to connect the interpolator (b) to the basic synthesizer circuit. The interpolator circuit simply uses a MM74C90 counter and two inverters to convert the divide-down signal, f_b, into a bi-quinary code in order to modify the BCD output of the MC4560 adder, the device that is primarily programmed by the switch array.

When the bi-quinary patterns, represented by f_d, are

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By: Dr. Thomas A. Brubaker, Colorado State University

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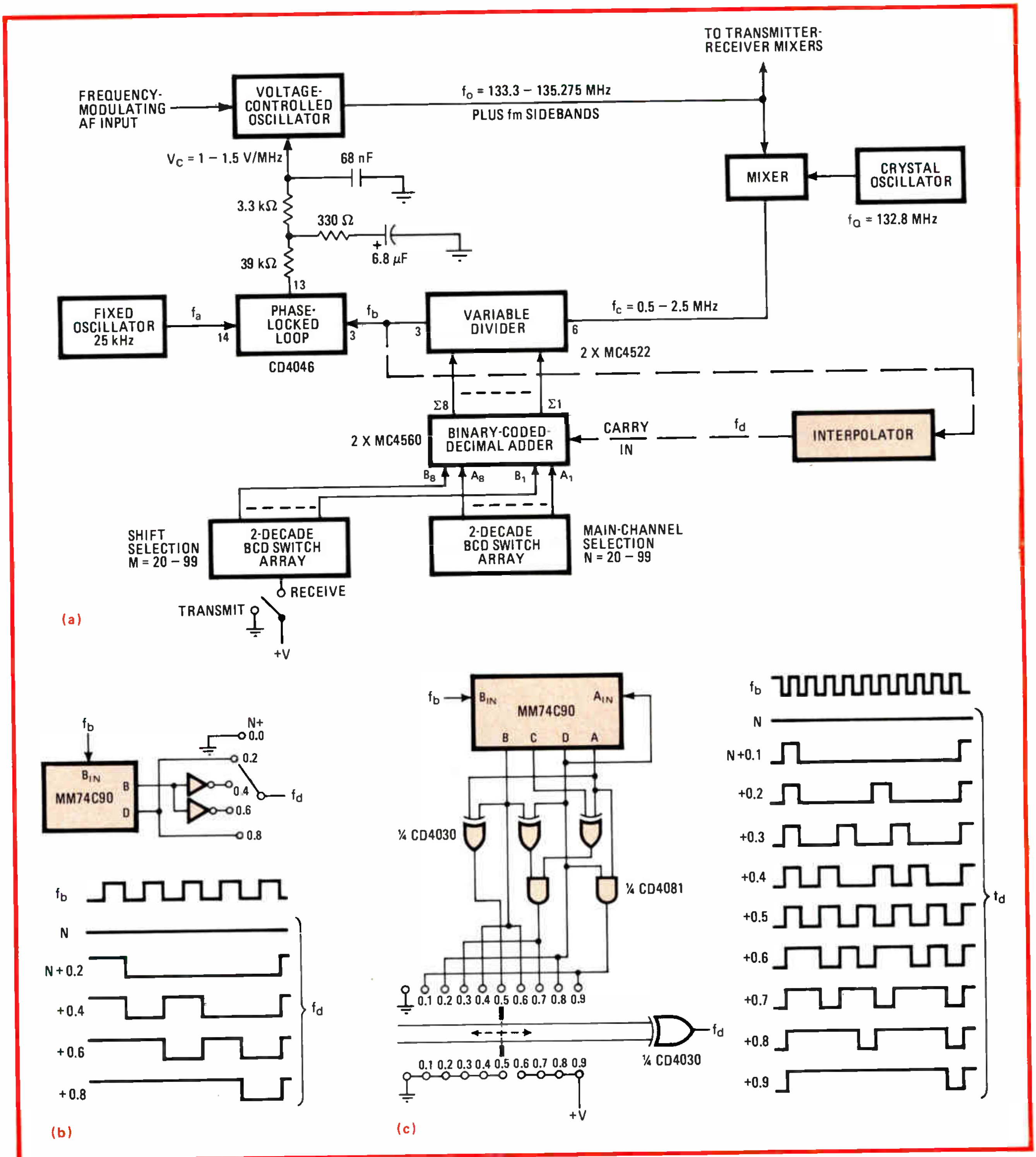


Increased density. Typical frequency synthesizer shown generates 80 channels, spaced 25 kHz apart, in the 133.3-to-135.275-MHz range (a). Number of channels in the given band may be increased by 5 by adding only one bi-quinary counter and two inverters (b). Channel multiplication can be extended to 10 if a few more gates are added (c). N values are selected with a rotary switch and an exclusive-OR gate.

introduced to the carry-in port of the 4560, the average value of N produced per given time interval is selectable throughout the range N + 0.0 to N + 0.8 in increments of 0.2, enabling 400 channels with 5-kHz spacing to be generated by the VCO. The instantaneous value of N changes, of course, and therefore the phase-locked-loop filter shown at the output of the 4046 (a) is required to ensure that there will be minimal ripple in the control voltage, V_c. V_c will thus be smoothed sufficiently to prevent spurious signals from being generated between adjacent 5-kHz frequencies.

A second circuit (c) uses the interpolation technique to increase the number of channels to 800, spaced 2.5 kHz apart. □

Cell layout boosts speed of low-power 64-K ROM

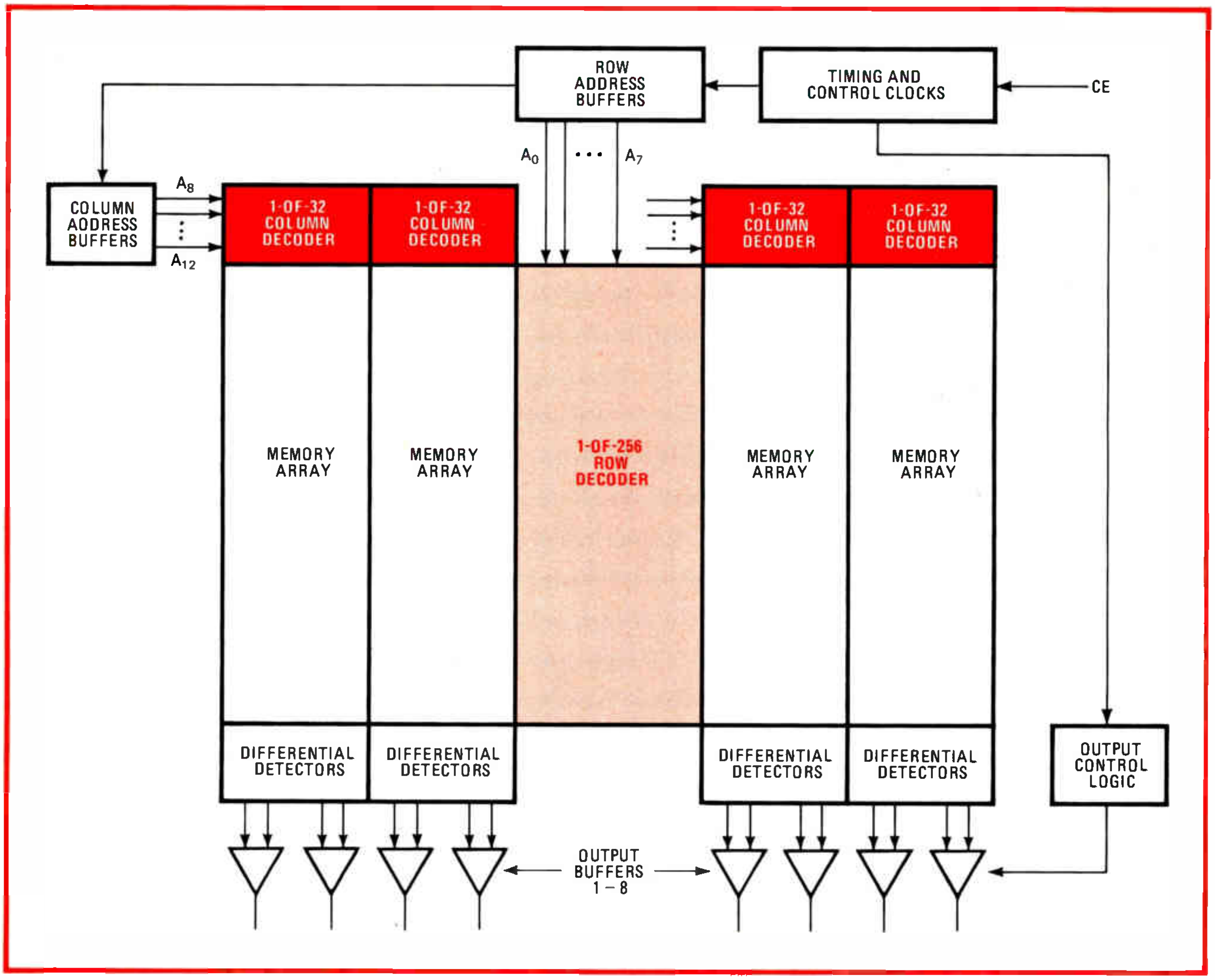
by Dennis R. Wilson,
Mostek Corp., Carrollton, Texas

A 64-K MOS read-only memory has been developed that sets a new high for ROM density and performance. Thanks to a layout that shares elements among many cells and a dynamic peripheral circuit design that reduces power and increases speed, this chip operates typically with access times of 80 nanoseconds and power dissipations of 150 milliwatts. That's the best speed-power performance yet offered by any ROM of any size.

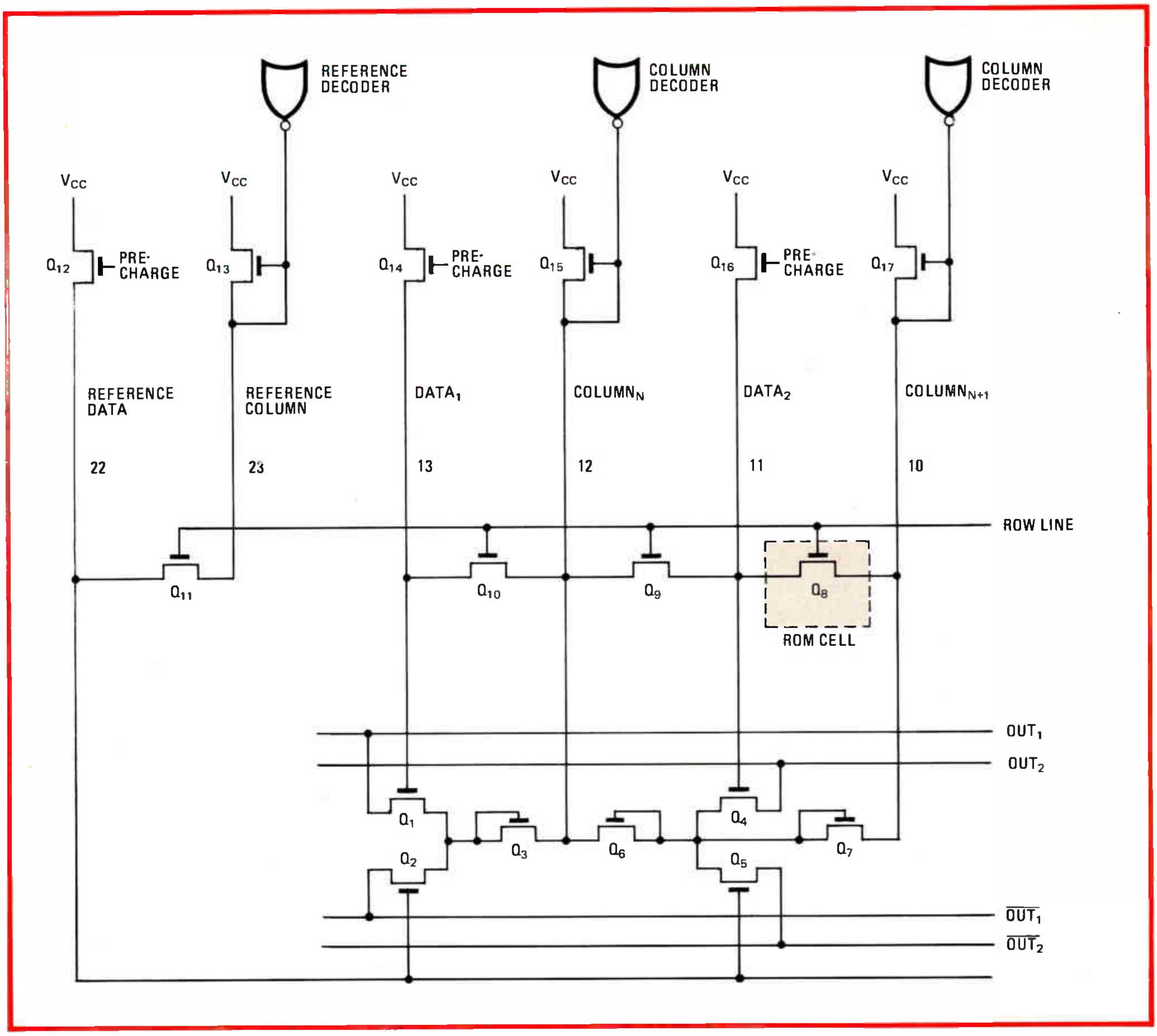
Suddenly, the digital system designer, accustomed to typical metal-oxide-semiconductor ROM performance in the 350-ns and 500-mw range, has new options. He can replace a 16,384-bit part with a new 64-K one and get a fourfold increase in data for fixed-storage applications yet never worry about data-entry access times being too slow, even for the fastest MOS computer system. Moreover, the new MOS ROM is as fast as any bipolar device, so where real-time data access is needed, as in front-end signal-processing systems, the designer need no longer turn to the more expensive and more power-consuming bipolar devices.

In short, all high-speed ROM applications can now be handled by one low-cost 5-volt MOS part. Microprogram storage, which previously used bipolar ROMs, can now be implemented with the higher-density and lower-power 64-K memory. Turnkey minicomputers that currently use core memories for nonvolatile program storage can now also use the fast-access ROM. What is more, as the microprocessor market expands and the central processing units available operate at greater speeds, the new ROM can provide direct compatiblity with these parts up through 10 megahertz. In addition, the 64-K density allows very high-level languages to be used to further enhance microprocessor performance.

The MK 36000 is organized as 8,192 words of 8 bits each, a configuration best suited for the most popular byte-oriented computer systems. The memory array (Fig. 1) is divided into four 16,384-bit quadrants, each



1. The organization. The chip, organized as 8,192 8-bit words, is divided into four memory arrays, each of which contains the data of two outputs. The column decoders provide 1-of-32-column selection, while the row decoders supply 1-of-256-row selection.



2. Sharing. Each ROM cell shares both the output row line and decoded virtual grounds with other cells in its row. This arrangement saves space as well as making processing less complex, since only one half a contact is needed per cell.

containing the data for two outputs. The column decoders, shown at the top of each quadrant, provide the required selection of 1 of 32 columns, and the row decoders, located down the center of the chip, provide the required 1-of-256-row selection.

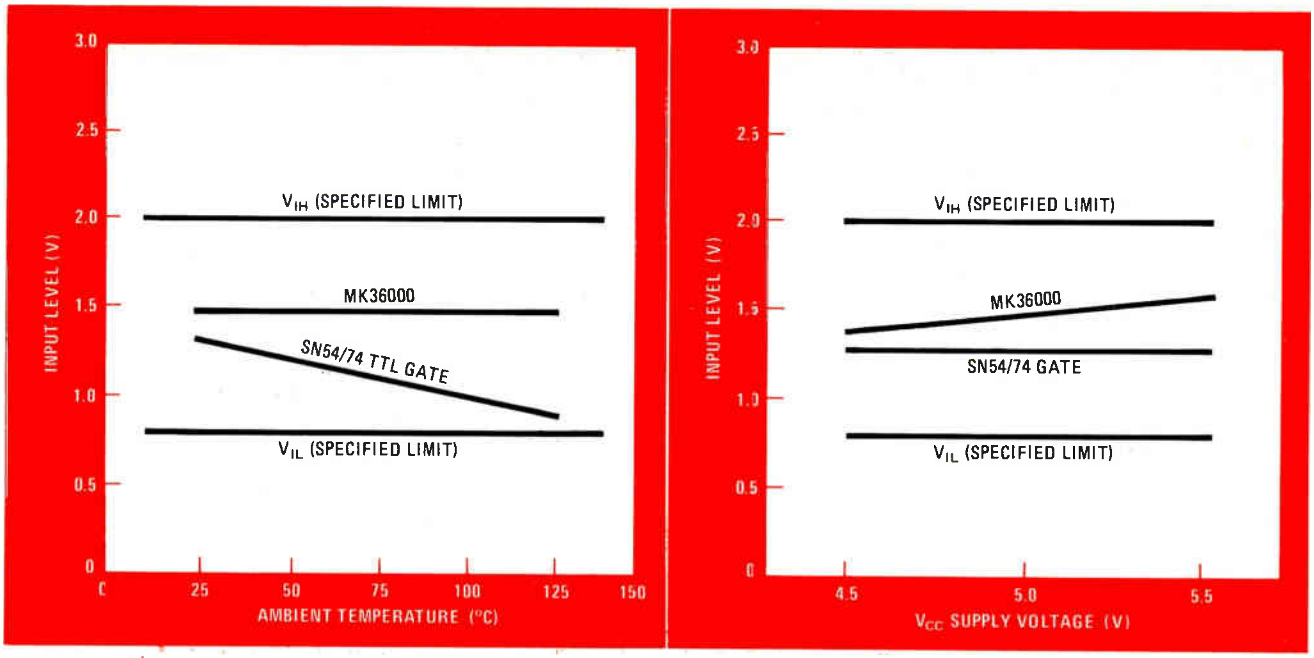
Sharing

The cell-layout sharing scheme is illustrated in Fig. 2, where the ROM cell designated Q_8 is shown sharing with other cells along the row not only the cell's outputs to the row line but also the vertical decoded ground lines between cells. That arrangement results in a great reduction in both cell area (0.25 mil^2, compared with 0.54 mil^2 for conventional cells) and process complexity (only one half contact per memory cell).

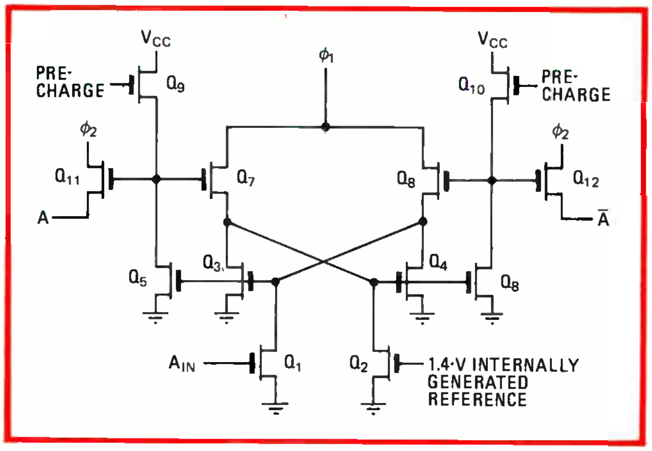
The chip is of course built with the standard static single-transistor ROM cell used for the last few years in high-density ROMs. However, dynamic, or clocked, circuitry has been chosen for the peripheral sections of the chip: decoders, sense amplifiers, and output buffers. It is these clocked circuits that save power, since they are activated only when the chip is in operation and data is valid. Otherwise they are turned off and dissipate no power.

Internal clocking is completely invisible to the user. In fact, a single transistor-transistor-logic-level clock is all that is needed to activate the chip. The negative-going edge of the chip-enable signal initiates a sequence of internal dynamic clocks. The first clock latches the address signals, followed by clocks that activate the selected row and column, transfer data differentially to latching flip-flops in the output buffers, and finally drive the push-pull static output stages (shown in the lower section of Fig. 2).

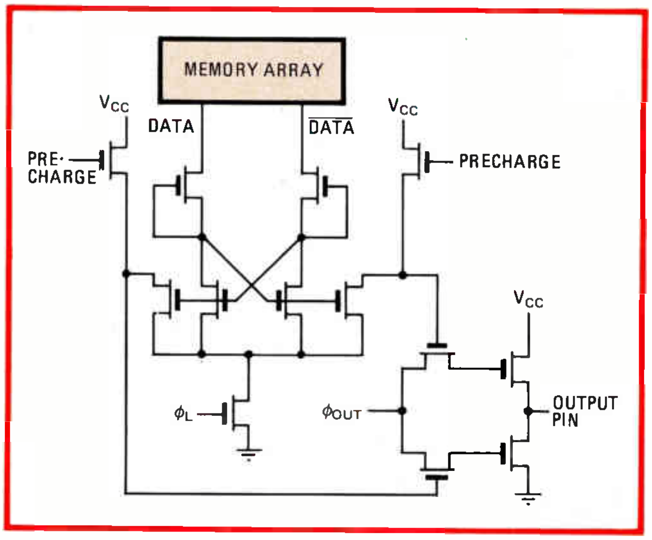
Unique to 36000 is an automatic precharge sequence. When data becomes valid at the output, a sequence of clocks automatically recovers all the internal circuitry except for the chip-enable input stage and the static



3. Proper level. The 64-K 36000 ROM is extremely easy to use. Its trip levels are well within the capability of standard transistor-transistor-logic gates over the entire commercial range of ambient temperature and supply voltage.



4. Input buffer. A logic signal is provided by the difference current between Q_1 and Q_2. The difference allows the cross-coupled device, Q_3 and Q_4, to be latched on the positive edge of the CE ϕ_1 clock. This signal in turn determines whether the logic is a 1 or 0.



5. Outputs. This differential sensing scheme detects the array information and passes it to the output stage. The circuit, which does not need to wait for full MOS logic levels, is similar to the input buffers in its ability to resolve signals of very small magnitude.

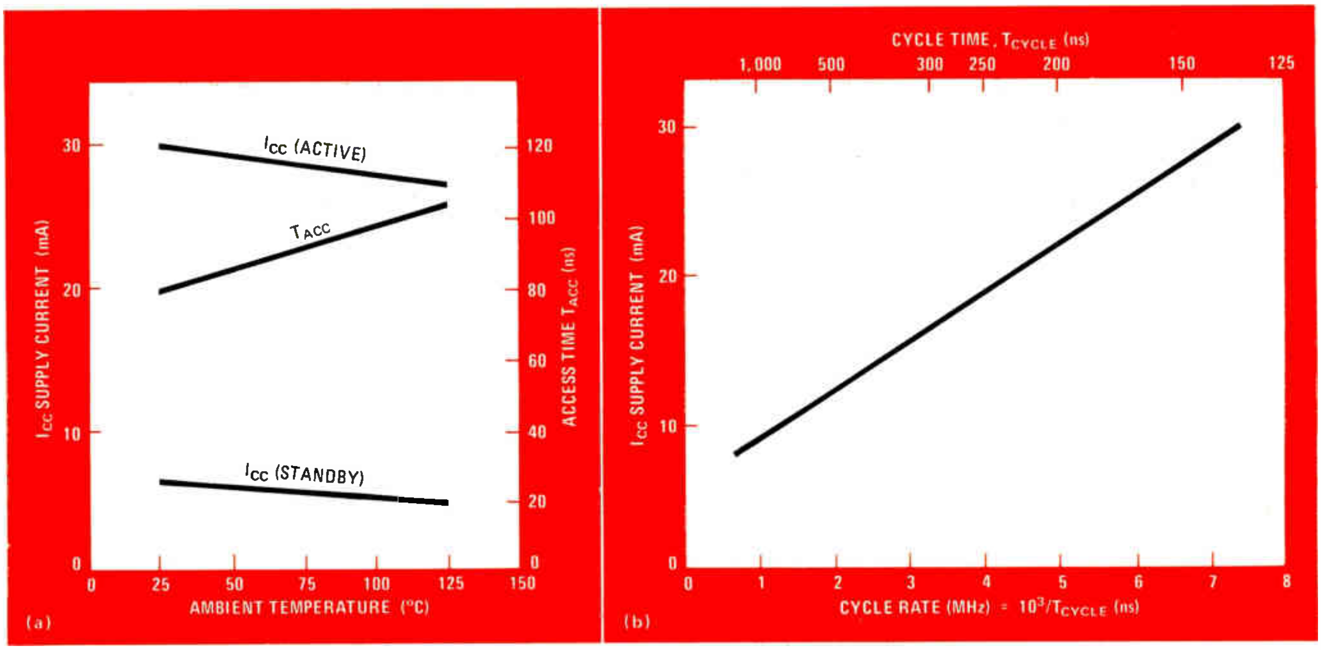
output buffers. This automatically places the ROM in a low-current mode similar to a chip-enable standby mode, further reducing operating power.

Additional benefits

A clocked peripheral approach for the ROM design provides other benefits besides power savings. For example, the high-resolution dynamic sense amps are used to provide TTL compatibility on address inputs. The ROM guarantees a minimum logic 1 voltage level, V_{IH}, of 2.0 v and a maximum logic 0 voltage level, V_{IL}, of 0.8 v.

If the ROM is to be used as a replacement for TTL parts, an important consideration is how well the input-level trip point tracks within the available V_{IH}–V_{IL} window as a function of temperature, power supply, and process changes. Variations in input trip levels for both power supply and temperature for the MK 36000 and a typical TTL gate are illustrated in Fig. 3. The resolution of the input buffer at any one operating point is typically on the order of a few millivolts, allowing ample room for process variations.

The input circuit used to provide TTL compatibility is shown in Fig. 4. The input signal is provided by the difference current between Q_1 and Q_2 in comparing the address input level and the reference level. This difference allows the cross-coupled device, Q_3 and Q_4, to latch on the positive edge of the ϕ clock, and this data determines whether the true or the complement address goes to a valid high state. The chip-enable clock input is the only input requiring a static stage to begin the clock chain. The switching threshold of this stage was designed



6. Tough performer. The chip's access time in the worst case is 100 ns, with typical readings as low as 80 ns at room temperature. Current dissipation is well below 30 mA (a), whereas at very long cycle times, the supply current approaches the 10-mA standby level (b).

to be independent of device thresholds and to provide characteristics similar to those of the dynamic input buffers that offer significant power savings.

Differential sensing scheme

After dynamic decoding takes place, row and column clocks are generated to read data out to the array. A differential sensing scheme (Fig. 5) is used to detect array information. The scheme enhances speed by eliminating the wait for full MOS logic levels to develop. Moreover, the circuit used is similar to the input buffers in its ability to resolve signals of very small magnitude, resulting in large internal noise margins. Typically, the output sinks and sources 16 milliamperes at 0.4 and 2.4 volts, respectively, to ensure adequate drive capability.

The advantages of applying advanced circuit techniques to standard n-channel processing become apparent from the chip's performance characteristics (Fig 6). Active and standby currents of typically less than 30 mA and 10 mA, respectively, lead to chip power dissipations that are one third of that typically dissipated by fully static ROMs. Moreover, the dynamic peripheral circuitry of the 36000 is frequency-dependent, so that as longer cycle times are used, the power approaches that of the standby value (Fig. 6b). In addition, dynamic circuit design techniques increase the speed threefold—from Fig. 6a, the worst-case access time (at 125°C) is seen to be typically 100 ns. □

V-MOS configuration packs 64 kilobits into 175-mil² chip

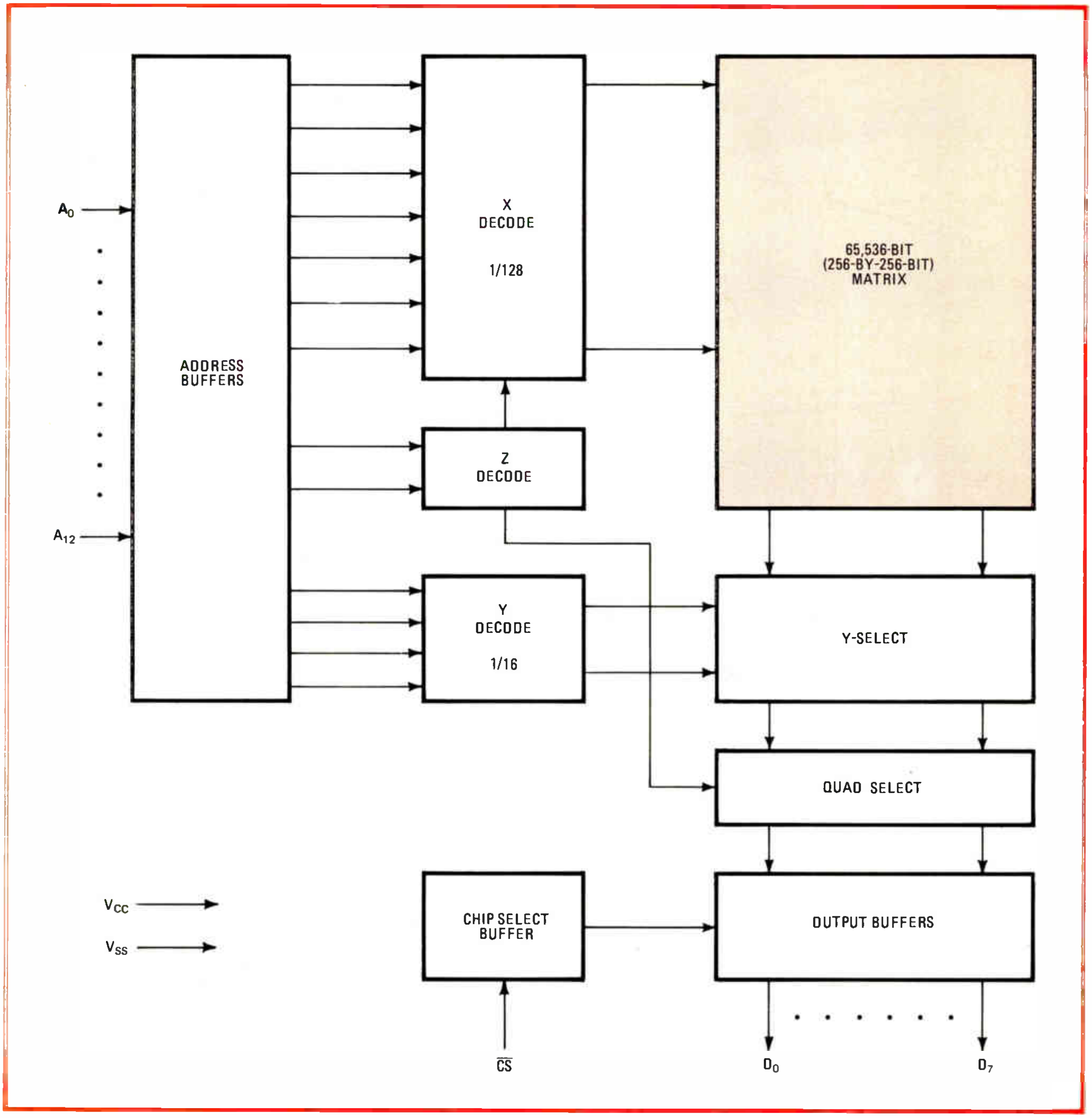
by Terry Holdt and Robert Yu,
American Microsystems Inc., Santa Clara, Calif.

Since a microprocessor system is only as good as its program, the growing sophistication of such systems is making increasingly tough demands on their read-only memories. The new systems are more powerful and have broader input/output capabilities, so they need bigger, more capable ROMs. Right now, most of the more complex applications need between 2 and 8 kilobytes of memory storage, which opens the way to a single-chip 8-kilobyte ROM that can satisfy the performance requirements of such systems.

The S4264, a 64-K read-only memory that packs 8 kilobytes of memory into a chip less than 175 mils square, is intended to satisfy the increasing memory demands of more complex microprocessor systems. Designed and implemented with high-density common-source V-groove metal-oxide-semiconductor technology (see "It's all in the groove," p. 101), this fully static design operates from a single 5-volt supply. Since it contains both memory array and sensors on chip, no chip-enable pulse is needed. The 8,192-by-8-bit ROM, only marginally larger than most 16-K ROMs on the market, can replace four of these chips and cut system power consumption by more than half.

Program size important

There are other answers to the demand for more program memory. Some of the new low-end single-chip microcomputers come replete with 1 to 2 kilobytes of resident ROM, as well as a scratch-pad random-access memory. Another answer is the combination chips that integrate RAM, ROM, and I/O in order to cut the number



1. Block diagram. The 64-K read-only memory, S4264, makes use of three decoders to decode the 256-by-256 memory matrix into an 8,192-by-8-bit organization. The chip-select signal is buffered directly to the output stage to assure very fast chip-select times.

of system components. However, both approaches are limited by the size of the program that can be accommodated. The single-chip big ROM packs in the bits, and it can offer significant savings in space and costs because it packs them into one package.

Aimed at microprocessor applications, the new 64-K memory was organized as 8,192 by 8 bits because the 8-bit organization is by far the most popular, and because 8-K pages of words satisfy most users' needs. Moreover, the ROM is totally static and allows the system designer to use only a 5-V system without having to compromise speed or power. It has transistor-transistor-logic compatibility and can sink high output currents.

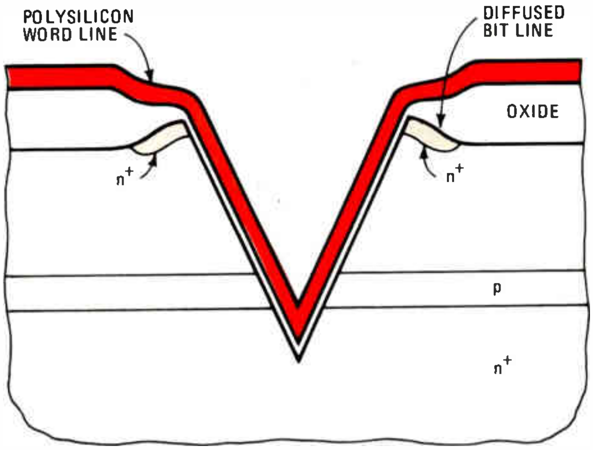
Typical access times of 250 nanoseconds and power dissipation of 500 milliwatts make it suitable for most high-speed microprocessor systems. However, even the worst-case access times of 350 ns and power dissipation of 750 mW guarantee better performance than is obtainable with available 16-K ROMs. For a summary of the primary features of the S4264, including typical electrical parameters, see "Taking the measure of the S4264" on page 104.

Extremely simple timing requirements for the 4264 minimize the number of constraints placed on the systems designer. For example, both address and output signals are unlatched. Most microprocessors already

It's all in the groove

Each V-groove metal-oxide-semiconductor cell of the S4264 is defined by the orthogonal intersection of a diffused bit line and a polysilicon word line. The source region of the read-only-memory transistor, which resides at the base of the V groove, is common to the entire array of cells. Since it requires no surface area on the silicon chip, the resultant savings in space makes possible the smallest ROM cell in current production—only 11.6 micrometers on a side.

The advantage in size for common-source V-MOS technology in implementing high-density ROM arrays is obvious, but its space saving does not stop there. The same high density can shrink decoders for ROMs, random-access memories, programmable ROMs, and microprocessors with on-chip data and program storage. In V-MOS, these decoders are NOR gate arrays that are binary-count-decoded so that the appropriate cell is accessed with a given address.



have latched addresses, and popular 16-K RAMs have no output latches; thus an unlatched-output 64-K ROM should prove popular for systems requiring both a mix of ROM and dynamic RAM. Since the chip-select input is a normally low-going signal during $\overline{CS}$ time, it permits expansion of the memory array and allows selecting individual chips when the outputs are wire-ORed.

The V-MOS approach provides superior drive capability from the memory cell, even with heavy loading on both bit lines and common-bus lines at good speed. As a result, only a simple inverter buffer circuit is needed to sense the bit-line swing.

Planar n-channel MOS transistors are used only for pass gates, push-pull circuitry, and the three-state output-buffer load devices. Also, the use of implanted resistors as load elements for the rest of the circuitry means that implant modifications can achieve a range of speed and power tradeoffs.

Chip layout is quartered

A distinctive feature of the 4264 design (Fig. 1) is the internal organization. The circuit is divided into four 16-K quadrants, each of which has a 128-by-128 memory matrix decoded into 2 kilowords of 8-bit depth. Since each quadrant is a separate entity, a power quad-select concept is useful. During chip select, only one quadrant is activated; the other three are automatically put on a standby mode and dissipate essentially no power.

The address buffers amplify the address input and generate the address complements. These signals are then fed into the X, Y, and Z decoders, which decode the 256-by-256 memory matrix into the 8-K-by-8-bit organization. The X decode is the access to the word line, and the Y decode is the access to the bit line. The Z decode is the access to the quadrants and transfers a particular bit to one of a common set of eight bit-sense lines.

A final stage of output buffering converts the internal levels to TTL-compatible output signals. The chip-select signal is buffered directly to the output stage, which results in a very fast $\overline{CS}$ access time.

The X decoder is designed so that the word line is activated only in the selected quadrant. Instead of using a single 1-of-128 decoder, two 1-of-64 NOR decoders operate on the appropriate word line from either side of the quadrant. This approach resolves the layout pitch problem between decoder and memory cell and allows optimization of the ROM design around the access time of the word line.

Extra programmability a plus

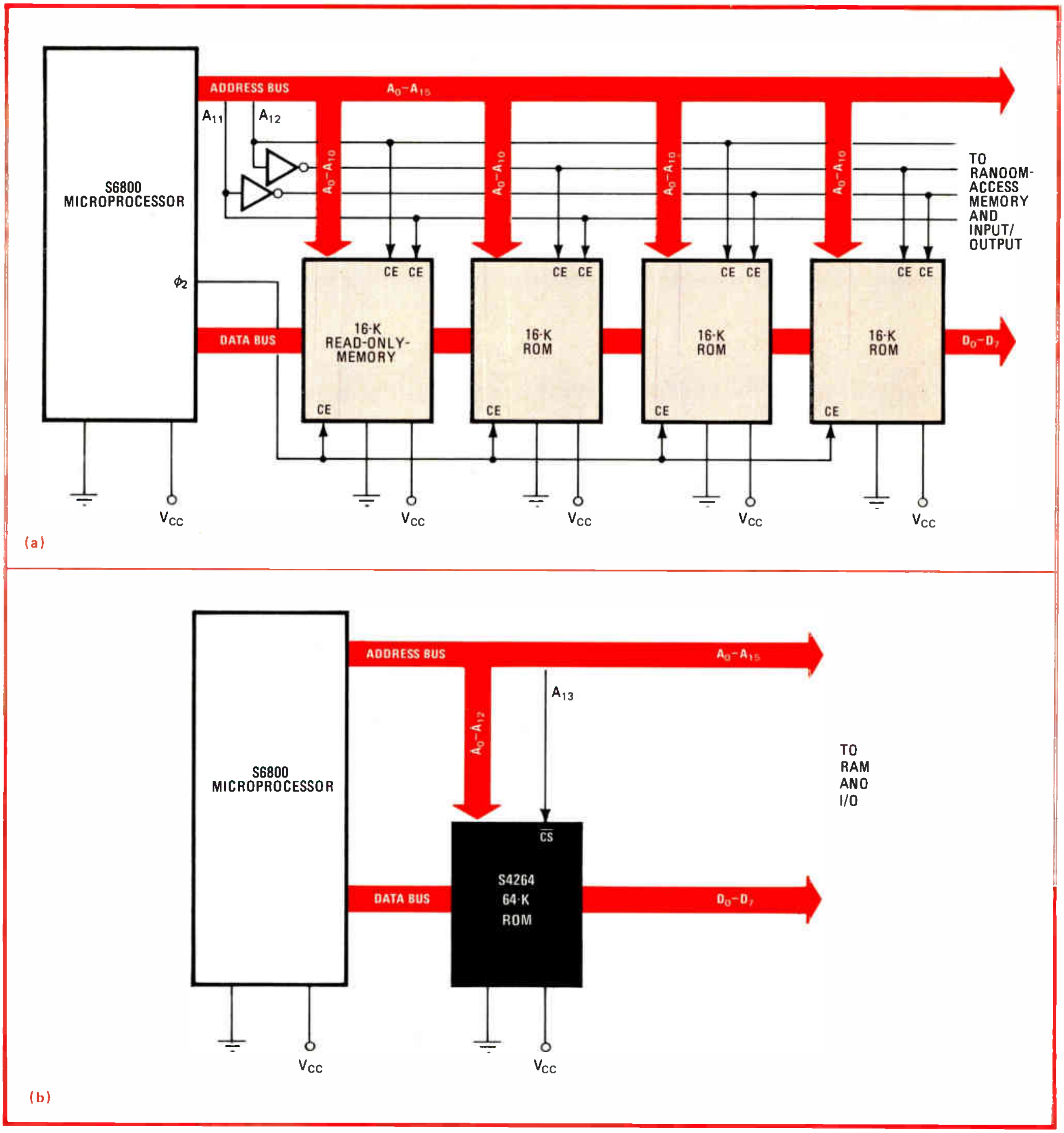
With 65,536 bits of ROM on a single chip, the user can fit added programmability into a smaller space with less power dissipation and more reliability than with 16-K chips. All this adds up to higher performance at a lower price per bit at the systems level.

Figure 2 contrasts two layouts of a typical S6800 microprocessor application requiring 8 kilobytes of program memory: using four 16-K ROMs (a) and using a 64-K ROM (b). Space savings on a typical printed-circuit board housing the memory will be more than the savings in package area alone. The pc interconnections composing the bus structure take considerable board space, and the address bus, 8-bit-wide data bus, and control bus can all be cut back.

Purely from the point of view of saving space, the 64-K ROM comes out ahead when more than 2 kilobytes of program memory are required (Fig. 3). The active address lines (those having access to the true memory cells instead of just acting as decoded chip selects) number 13 for the 8-kilobyte range of the 64-K device vs 11 for the 2-kilobyte range of the 16-K chip. But this increase is offset by the requirement for only one $\overline{CS}$ line in the 64-K unit.

Program space is condensed

This savings in program-memory space should not be regarded lightly. Often the area reductions of large memories are associated only with large RAM arrays, where a small savings in package size (16 vs 22 pins) or increased bit count per package (16-K vs 4-K) is multiplied many times. While it is true that this space savings is more dramatic as the data bit count increases, the exploding use of microprocessors is accelerating the need for condensed program memory as well. For example, consumer applications such as programmable games and hand-held instruments do not demand megabits of



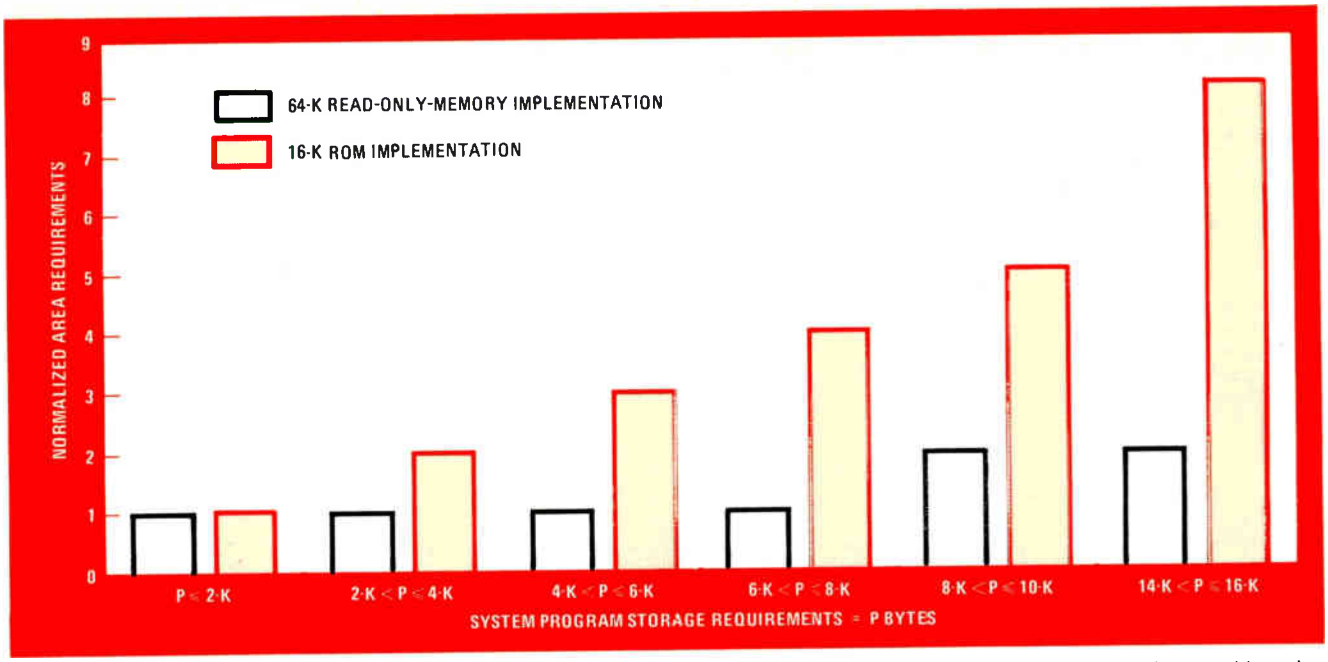
2. Small and simple. When built with 16-K ROMs (a), a typical microprocessor system with 8 kilobytes of program memory requires more packages and bus interconnections than when it uses a 64-K ROM (b). Fewer interconnections alone account for a large savings in area.

memory, but they are very sensitive to the integrated-circuit package count and the space required to house these components.

Just as dramatic, and often more important, than space savings is the reduced cost of using 64-K ROMs for larger memory requirements. Here the savings in IC support hardware will be significant (Fig. 4). On the basis of the cost of sockets for 24-pin ICs and pc-board support costs, a 64-K ROM may run as much as $1.65 more than four 16-K units and still be cost competitive.

From a system standpoint, it makes economic sense to use 8 kilobytes of ROM even before the program requirements dictate it. For example, a 5-kilobyte program implemented with 16-K chips runs $1.10 more in socket and support costs than a 64-K implementation. Thus a designer could pay this amount plus three times the unit price for 16-K ROMs to get a 64-K device with no increase in system costs. Of course, even if the 64-K memory sells for somewhat more than this tradeoff cost, he could use it for the 5-kilobyte program and have the built-in ability to move easily to 8 kilobytes when necessary.

Deciding to move up to the 64-K level depends on

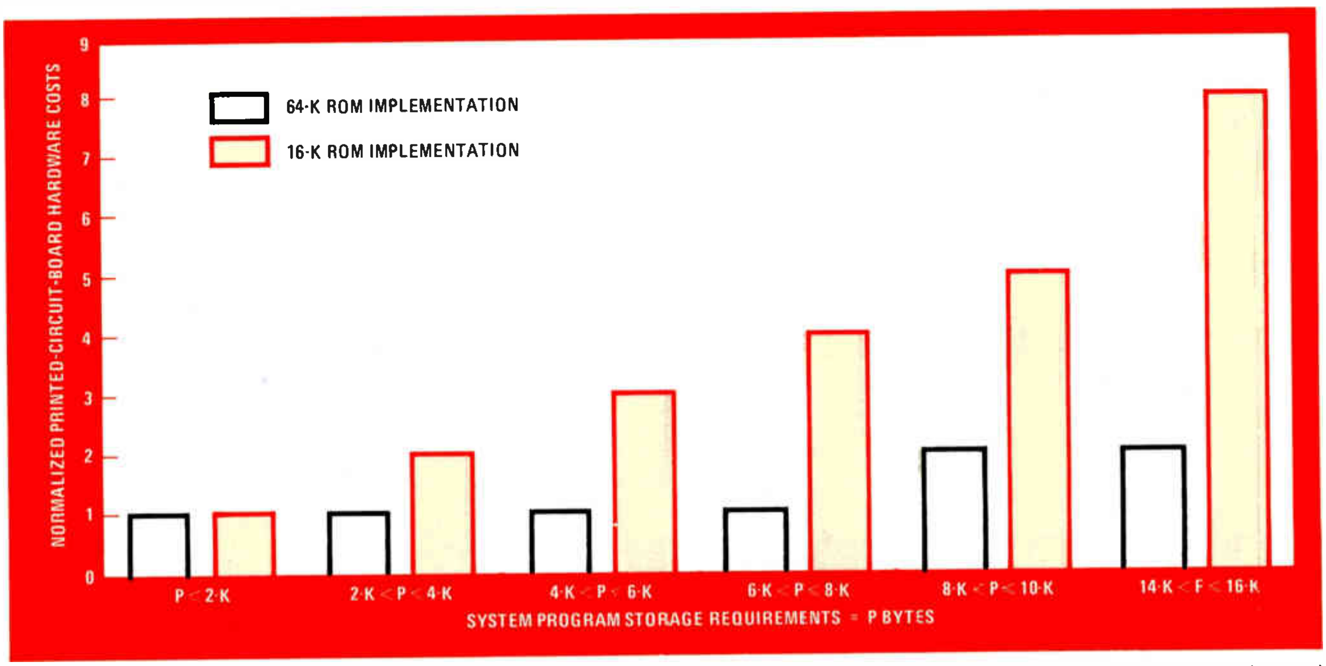


3. Saving space. If more than 2 kilobytes of memory storage is required, a considerable amount of pc board space can be saved by using one 64-K ROM instead of several 16-K chips. The area is normalized to the space required for a single 16-K ROM—about 1.6 square inches.

other considerations, as well. For one, a manufacturer of a large number of systems with a program content of less than 6 kilobytes may elect to stay with 16-K ROMs. A company producing systems in lesser volume, where the pc board costs are high, may well decide to take advantage of the savings in system hardware and space of the 64-K ROM, even though he will not make immediate use of all the memory available. However, in applications where more than 6 kilobytes of program memory are needed, a single 64-K chip is the way to go.

Yet another cost advantage for the 4264 is the economy of a single IC for 8 kilobytes of memory. The 30,000-square-mil V-MOS chip is only 50% larger than most 16-K devices currently available. From the standpoint of silicon area used, a single 64-K ROM in V-MOS occupies only 38% of the equivalent area required for four 16-K units. While the percentage yield of the larger 64-K memory will be less for a given wafer size than for a smaller chip, the cost for four 16-K devices will be much greater than that of a mature 64-K ROM.

What's more, package and assembly costs drop 75%, resulting in a substantial savings in final system cost to



4. Comparing costs. The difference in hardware costs between four sockets and a single one is estimated at $1.65, a figure that can be used as a measure of the cost per component in a memory system. Chart shows cost of using 16-K and 64-K ROM vs memory requirements. Hardware costs are normalized to the cost of board support plus that of the socket for a single 24-pin IC. Cost of the IC is not included.

Taking the measure of the S4264

Here is a summary of key features and electrical parameters for the S4264 V-groove read-only memory:

- Pin-compatible with 2708 8-K PROM, with three pins redefined to reach addressable 8 kilobytes.
- Organized as 8,192 by 8 bits.
- Fully static: no clocks required.
- Fast access time: 250 ns.
- Low power dissipation: 500 mW.
- Three-state output, which can be OR-tie-compatible.
- Single power supply: 5 V ±5%.
- TTL-compatible inputs and outputs:
  V_{IH} = 2.0 V min
  V_{IL} = 0.8 V max
- High output-current capability:
  V_{OH} = 2.4 V (I_{source} = 5 mA)
  V_{OL} = 0.4 V (I_{sink} = 10 mA)

the user. This savings is far from trivial since much of the IC component cost lies in the parts and labor required to assemble all the components.

Besides space and cost advantages, the 64-K ROM offers other benefits as well. For one, power is effectively quartered on a per-bit basis relative to 16-K ROMS.

The ability of V-MOS technology to produce single-cell memory structures of extreme density will provide not only 128-K and 256-K ROMs, but very large erasable programmable ROMs and dynamic RAMs as well. Although multitransistor-cell static RAMs do not benefit from the use of V-MOS as much as do single-cell memories, such techniques nevertheless provide smaller static cells than are available now with other technologies.

Further reductions

The cell size of the 64-K ROM still represents 5-micrometer technology, but V-MOS lends itself to scaling down just as planar technologies do. Operating V-MOS static RAMs have been developed with layouts that can further reduce chip size by at least 20%, using optical reduction techniques.

This feature of V-MOS has not been pursued so far, because the die sizes of the products are competitive with existing chips fabricated with other technologies. V-MOS development continues and, with only minor reductions in line width and spacing, a 128-K ROM will occupy the same area as does a 64-K ROM processed in current planar technologies. □

Dense, interchangeable ROMs work with fast microprocessors

by Robert Greene,
Intel Corp., Santa Clara, Calif.

The recently introduced 2332 and 2364 read-only memories double and quadruple the density of today's 16-K devices by using an adaptation of Intel's H-MOS process. Moreover, being functionally compatible with each other, earlier members of the same family, and the new high-performance microprocessors, they eliminate the need for redesign of the memory portion of a microprocessor system each time the firmware changes.

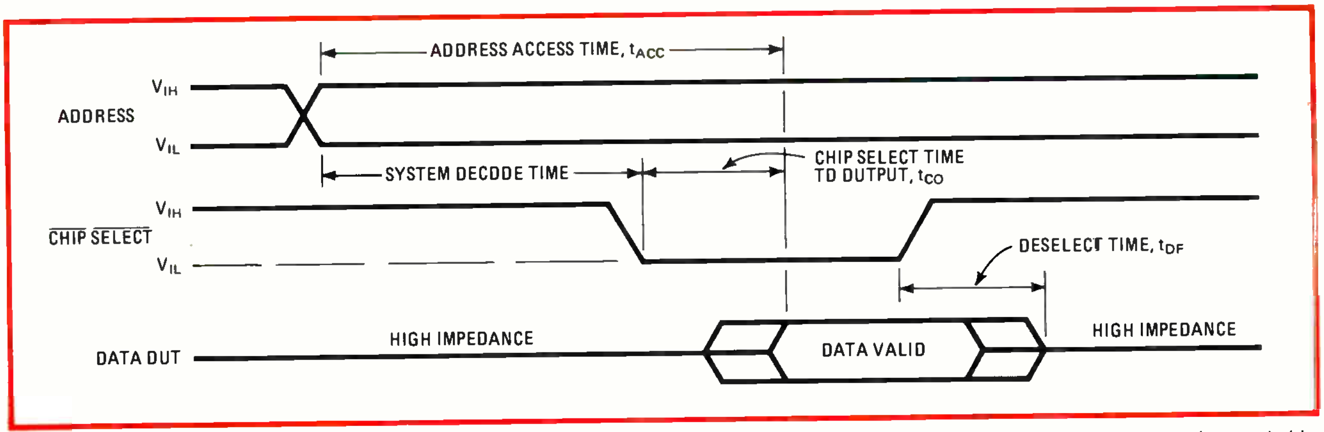
In other words, the fast new 32-K and 64-K memories, including the planned 32-K erasable programmable ROM, are interchangeable with existing Intel 5-volt ROMs and erasable PROMs. In addition, their power consumption is substantially less than that of the earlier devices, and their performance levels are compatible with those of such microprocessors as the 5-megahertz 8085A-2 and the 8086. To give the figures, the new ROMs are specified at a maximum access time of 300 nanoseconds and a maximum power-supply current rating of 40 milliamperes active and 15 mA standby.

Evaluating performance

By performing better, microcomputers are placing an ever-increasing burden on the performance and system flexibility of their related memory components. For example, take the first microcomputer, the 4004, its companion 1702A 2,048-bit erasable PROM and 1302 2-K ROM counterpart. With the 1702A, the chip select time to output, t_{CO}, is only 100 nanoseconds shorter than the total address access time, t_{ACC}, of 1,000 ns (Fig. 1). Performance of this order is good enough for 4004 4-bit microprocessors, but it is entirely inadequate for the byte-oriented memory-intensive, multitask environment of the 8080-type processors. For this kind of job, a system designer had to move up to the 8080-compatible erasable PROM 2708 or ROM 8308 types, which with their t_{ACC} of 450 ns and t_{CO} of 120 ns give the processor a handsome 330 ns to address external memory and perform such housekeeping tasks as decoding.

Though fast enough, the 8,192-bit 2708 and 8308 device types as well their next-level 16,384-bit 2716 and 2316E counterparts have another problem. They have only one chip-select control function ($\overline{CS}$) and therefore raise the possibility of bus contention whenever they are used in a multiprocessor configuration or in a high-performance microcomputer system in which the central processing unit must control a wide variety of intelligent peripherals. Inadvertent changes in the state of the CPU address lines can result in the unwanted selection of more than one device at a time. Such a state of affairs is particularly bothersome when a series of devices are vying for the bus's attention, as is increasingly the case in large systems.

True, system designers have for years been plagued with bus contention. So there exists a variety of system configurations for making sure that one memory device is off the bus before another is selected. As indicated earlier, with small static ROMs such as the 1702A or 2708, for example, it is traditional to connect high-order system address lines to a decoder and use the difference between t_{ACC} and t_{CO} to provide time to select the correct device (Fig. 2). This scheme allows the decoder an



1. Good enough. The 2,048-bit 1702A read-only memory, which has a differential of only 100 ns between total address access time and chip select time to output time, performs well enough for microprocessors like the 4004, but not for today's high-throughput multitask devices.

adequate margin to perform its function without limiting the overall device access time.

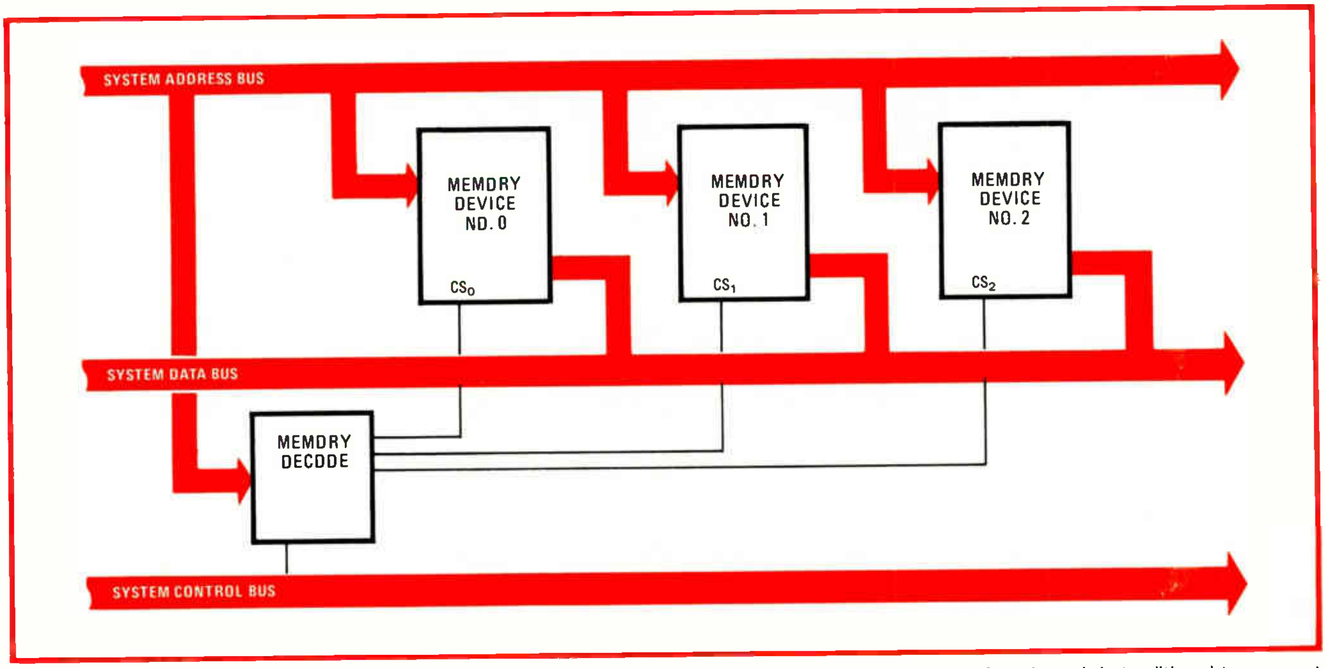
But this scheme does not work for large multimemory systems, where one device could have a longer deselect time (t_{DF} in Fig. 1) than the others. If this happens, and if fast external decoders are used in the system, it would be possible for two devices to be selected at the same time, as indicated by the shaded area in Fig. 1, Then if one memory happens to be reading a data high and the other a data low, their output transistors would in effect produce a short circuit—hardly a desirable situation.

Another bus contention problem is more subtle. As previously indicated, there is only one control function available on the 2708, and it must double as a chip select and an output enable. Thus any inadvertent changes in the state of the high-order address lines (which are inputs to the decoder) will change the device that is selected as well as enable the output. Bus contention again results, because the deselected device cannot get off the bus before the selected one is on the bus.

One theoretical solution to this problem of bus contention is to specify the device output parameters—chip select to output time, t_{CO}, and data float time, t_{DF}—such that there is a small margin in the region of 20 ns during which the user is assured that the output bus will be in a high impedance state. In reality, this does not work, as the bus curves out of the high impedance state almost immediately upon $\overline{CS}$ going true even though valid data is not available until the level of t_{CO}.

Intel's new generation has solved this problem of bus contention by having an independent output-enable function built right into the chip. This eliminates the need for the external devices that have had to be employed to confine bus contention to a particular card. As shown in Fig. 3, pins have been provided for ushering the data onto and off the microprocessor bus (output enable), and automatic power control is provided by way of the chip-enable function.

Moreover, these parts have access times short enough for the newest and fastest microcomputers. Access time



2. Time enough. In small static-ROM systems, to give the device's decoder enough time to perform its functions, it is traditional to connect system address lines to the decorders and use the difference in time between access and output for chip select.

Telling static from clocked devices

How can it be determined whether a memory is static or clocked? Examine the data sheet waveforms. If cycle time is equal to access time, the device is completely static. If the cycle time is not equal to access time, a portion of the device is dynamic, or clocked (sometimes called edge enabled). Note that the chip-enable nomenclature can be applied to completely static devices as well as to those that have dynamic periphery.

Another solution is to determine whether or not CE can be held true while addresses are changed. If new data is produced for each successive address without toggling CE, the device is completely static. If the data does not change, at least a portion of the device is dynamic.

Another difference between static and clocked devices involves the chip-select function. In a completely static device, $\overline{CS}$ is always functionally the equivalent of output enable, but in edge-enabled devices this is not always true. For example, both the chip select shown on pin 27 of the edge-enabled 2364 and the addresses are latched in by the falling edge of the chip-enable signal. This chip-select signal need not be maintained as a stable signal throughout the entire memory access cycle. With completely static devices, on the other hand, it must remain stable throughout the entire memory cycle.

of the 32-K and 64-K devices is specified as 300 ns maximum from the falling edge of the chip-enable signal ($\overline{CE}$). A selected version of the 32-K erasable PROM, the fastest member of the family, achieves a maximum access time of 150 ns for those microprocessor-based systems that require extremely high performance. Likewise, a selected version of the 2716-2758 carries a standard access time of 350 ns.

Figure 3 shows the pinout configurations of this expanded 5-volt family of erasable PROMs and ROMs. To take advantage of the modular compatibility offered by the family, the functional compatibility of device pins 18, 19, 20, and 21 must be understood.

First examine the compatibility of the two oldest members of the family, the 8-K 2758 and the 16-K 2716. Pin 18 functions as a chip-enable, $\overline{CE}$, being used to enable the clocked circuitry in the new devices, as it is the pin that substantially affects the power dissipation of the device.

Pin 19 is A_{16} for the 2716 and must be held at V_{IL} for the 2758. Pin 20 is the independent (for $\overline{CE}$) output enable, and pin 21 is the V_{PP} (V_{CC} for read-only applications) connection.

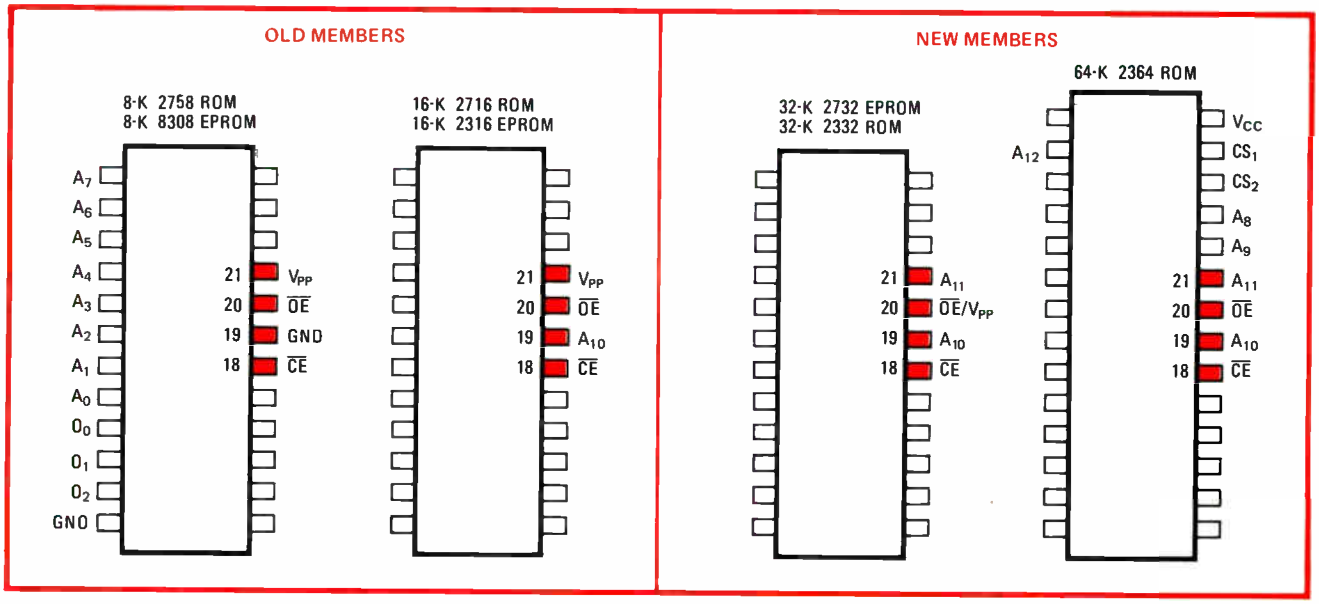
In this arrangement, the programming voltage for the erasable PROM enters through pin 21, V_{PP}, which is normally connected to pin 24, V_{CC}, for read-only applications, and pin 19 is either connected to ground or to address pin A_{10}.

The expanded family

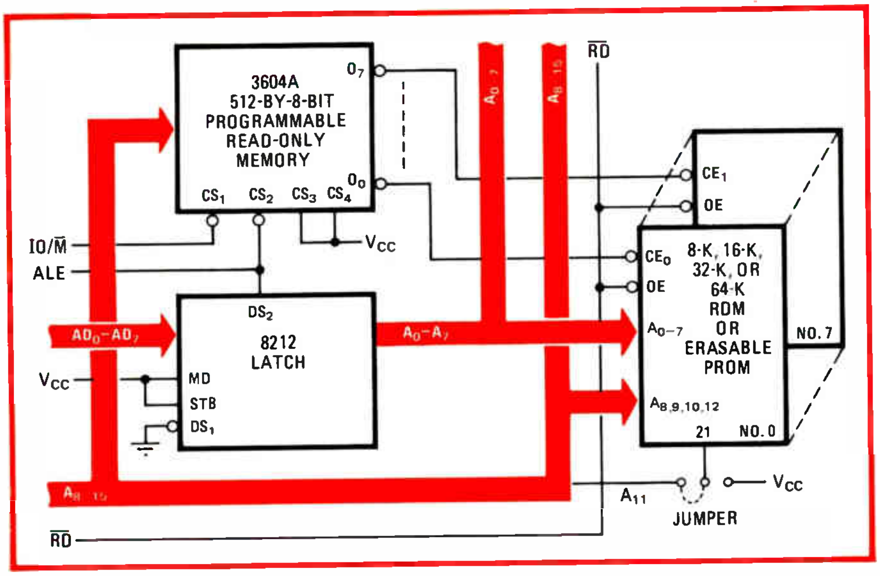
The new members of the family are the 28-pin 64-K 2364 ROM and the 24-pin 32-K devices, which have identical pinouts in both ROM (2332) and EPROM (2732) versions and so are interchangeable. They are designed with pin 18 as the chip-enable function providing the signal for precharging the active periphery of the devices.

Pin 19 remains an address pin, A_{10}, while pin 20, as before, stays an output-enable $\overline{OE}$. Again, OE is the function that allows independent control of data entering and leaving the output bus.

As the diagram of the 32-K 2732 and 2332 devices indicates, the erasable PROM's programming voltage, V_{PP}, is now multiplexed with $\overline{OE}$ on pin 20. To address the additional bits that are required as the density increases from 16 to 32 kilobits and the devices remain compatible, pin 21 becomes the address pin A_{11}, making it the only pin to require special consideration when designing a system to accept 5-V-only 8-, 16-, 32-, and 64-K devices equally well. With the 8-K and 16-K devices, pin 21 must be connected to V_{CC}, whereas with



3. A compatible family. The pin configurations of the 5-volt ROM and erasable PROM family—from the 8-K 2758 to the soon-to-arrive 64-K 2364—are functionally compatible, allowing members of the family to be interchanged with virtually no changes in board layout.



4. System flexibility. This 8085-based microcomputer system can have its ROM capacity expanded to a maximum of 64 kilobytes of ROM or reduced to 1 kilobyte simply by changing one card-level jumper and the ROM memory map.

the 32-K and higher-density devices, it must be connected to A_{11}. Here, system designers can treat pin 21 as an address line when designing their memory array, and by allowing for a single board-level jumper, can use the 8-K and 16-K devices or the 32-K and 64-K devices.

The last device shown in Fig. 3 is the densest member of the family, the 64-K 2364 ROM. Like the 32-K devices, it is a clocked or edge-enabled part, but unlike the 32-K designs, it is packaged in a 28-pin package, to retain functional compatibility with the other members of the family. Note, however, that the lower 24 pins are the same in both 32-K and 64-K devices. Thus, if CS_2 (pin 26) of the 2364 is mask-coded to be active high and connected to V_{cc}, and if the jumper provision for pin 21 is included on the card as described above, any member of the family can be plugged into the same 28-pin socket—1, 2, 4 or 8 kilobytes—without there being any need for card redesign or modifications.

This overall family compatibility is perhaps the greatest benefit of these new ROMs and erasable PROMs. A common printed-circuit board can be designed that, without needing to be redesigned in each case, allows the use of ROMs or erasable PROMs of different densities to accommodate smart as well as dumb terminals, or to adapt to new and more powerful software packages.

System realization

A block diagram of a system embodying all of the concepts discussed above is presented in Fig. 4. This configuration is implemented with the 8085 microprocessor and can be either expanded to a maximum capacity of 64 kilobytes (512 kilobits) of ROM or reduced to 1 kilobyte (8 kilobits) simply by changing one card-level jumper and the ROM. In the design, an open-collector bipolar PROM is used for the chip-enable decoder: it allows complete flexibility of ROM or erasable PROM placement on the system memory map.

Shown in the diagram is an 8212 address latch; but since the edge-enabled 32-K and 64-K ROMs or erasable PROMs contain internal address latches, the 8212 package is optional when using edge-enabled devices and is shown in order to achieve maximum flexibility. Note also 28 pin sites are used, again to offer total system flexibility at no added burden to the system.

System decoding is conditioned by the processor's $IO/\overline{M}$ output, which is the 8085 control signal that accommodates overlapping memory and I/O configurations. The decode is controlled by the 8085's address-latch-enable signal, the one that provides demultiplexing of the eight address/data lines.

Indeed, the only restriction on the configuration is that the PROM used for the decoder must be of the open-collector output variety to assure that the CE input is maintained high or low. At the same time, the read signal, $\overline{RD}$, from the microprocessor is connected to all of the erasable PROM or ROM output-enable pins, which are in turn connected in order to provide the direct output control that solves the output bus-contention problem discussed earlier.

With this type of architecture, the processor always retains control over the memory. It is not the memory but the processor that determines which memory device is to be selected and also when the data of the selected device will appear on the data bus.

Power supply requirements

As for power supply requirements, all members of the compatible ROM and erasable PROM family operate from a single 5-V source, but the nature of the load presented by each is somewhat different. The older 2716 and 2758 devices require a maximum 100-milliampere active and 25-mA standby current, while the 32-K and 64-K devices require a maximum of only 40-mA active and 15-mA standby current.

The current waveform for a single 2332 package shows typical I_{CC} levels of less than 10 mA during standby and approximately 20 mA while active. Current transients at the beginning and end of the cycle, which are caused by the clocked periphery being activated and in preparation for the next cycle, are easily accommodated by the use of approximate decoupling capacitors, such as a small high-frequency 0.1-μF capacitor located at every other device, with additional bulk decoupling located near the edge of the array. □

One-shot and counter multiplex pulse-width encoders

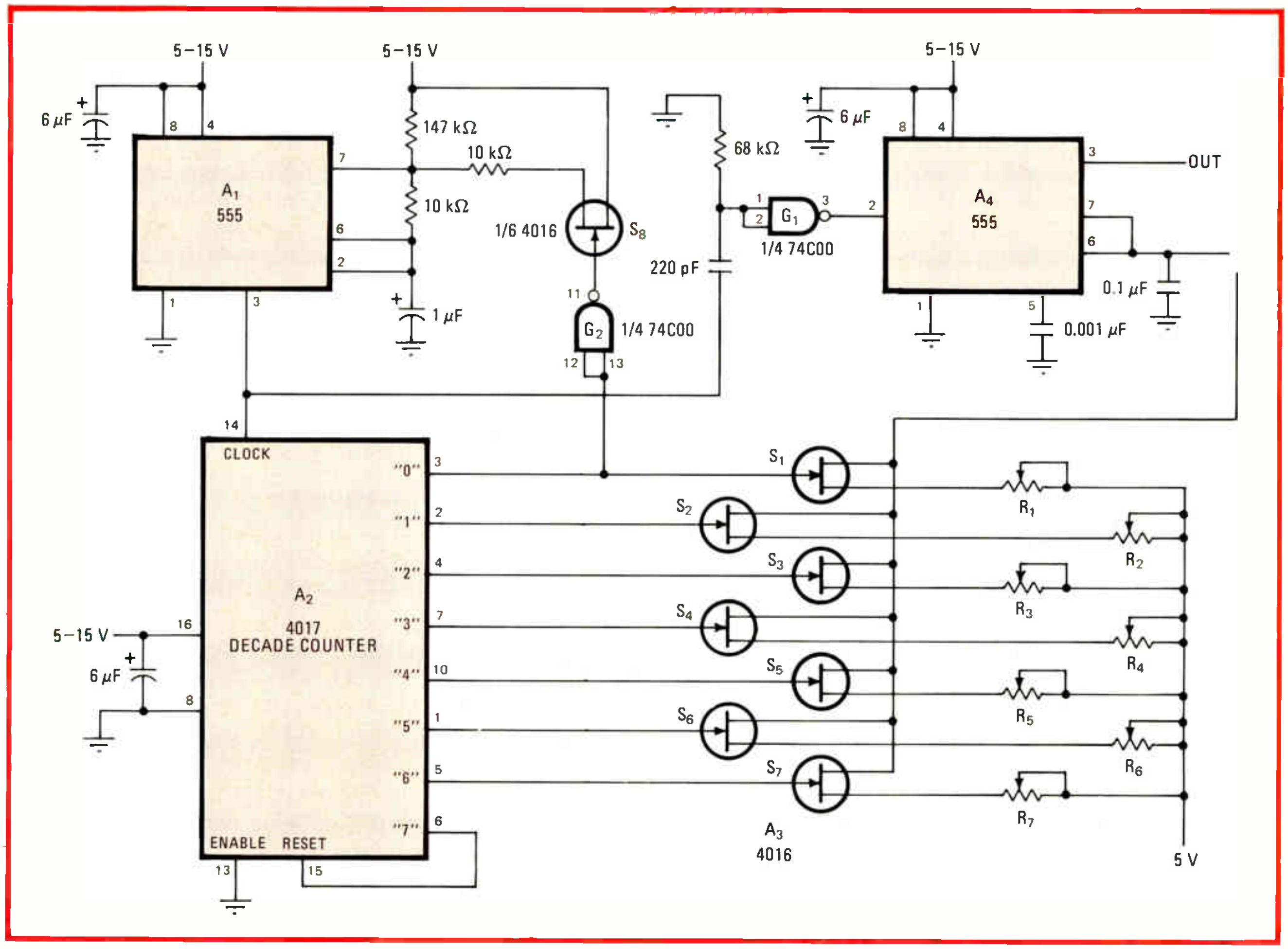
by John Mann
Kalamazoo College, Physics Department, Kalamazoo, Mich.

Combining a seven-channel multiplexer and encoder, this circuit generates seven pulses in sequence, each of which has a length proportional to a control resistance in the timing network of a monostable multivibrator. The circuit can function as a seven-channel pulse-width modulator if the respective control resistances themselves vary proportionally with audio-input voltages and the multivibrator operates in the kilohertz region. Otherwise, it can serve as a master-timing generator in synchronous data systems.

The circuit may be broken into two parts—the section comprising A_1, A_2, and A_3, along with control circuits that provide the multiplexing function, and the output section, A_4, which transforms R_1–R_7 into a proportional pulse width. The positive-going edge of the master clock, A_1, generates a square-wave output that advances the 4017 decade counter, A_2, and at the same time fires A_4. As the counter advances, analog field-effect-transistor switches S_1–S_7 place resistors R_1–R_7 in the timing network of A_4, and the one-shot's on time varies accordingly. The RC network at the input to G_1 is needed to differentiate the clock pulse so that the 555 is driven with a short-duration (15-microsecond) trigger signal.

When the counter reaches the seventh numerical position, it is reset. Consequently, the 4017 returns to numerical position 0, which is channel 1, and G_2 turns off analog switch S_8, lengthening the on time of A_1. Thus, end-of-pulse-train synchronization is achieved. The entire scanning process is then repeated.

With the timing components shown, A_1 oscillates at a rate of 40 hertz, generating three seven-bit pulse trains



Complete encoder. Circuit samples and multiplexes seven-channel data simultaneously. A_1–A_3 sequentially scans all channels, each of which has a control resistor (R_1–R_7) that determines duty cycle of one-shot A_4. Circuit can be used as seven-channel pulse-width modulator if each R_i can be made to vary proportionally to an audio-input voltage.

per second. This rate can be increased easily by decreasing the value of timing capacitance in A_1 and A_4.

The circuit can also be modified to generate up to nine pulses simply by wiring the two remaining channels of the counter into the circuit. Numerical position 9 (pin 11) of the 4017 is then used to reset the counter. Of course, one analog switch and one control potentiometer per channel are also required. □

Calculator notes

SR-52 finds group delay for Cauer filter

by Ron McGuire
ESL Inc., Vienna, Va.

The group delay of a filter—the delay time as measured for a collective band of frequencies passed through the network—is important to circuit designers. But although group delay information is easily obtained for most modern filters, it is not readily available for the often-used Cauer type. This SR-52 program finds the group delay of the Cauer type having a pole constellation with up to one real- and seven complex-pole pairs.

The Cauer filter has become popular because it is useful in synthesizing canonical networks (networks having the minimum number of elements). For example, $Z(s) = (s^2+1)/(s^3+2s)$ may be expressed as $Z(s) = 0.5/s + 4/s + 0.5/s$, and so a simple T filter can be built having 2-farad capacitors as the arms of the T and a 0.25-henry inductor in the center.

In any general network, if the transfer function of the network is known, then the pole-zero constellation is known. In particular, the phase angle of the network at a given radian frequency is the sum of the vector angles of the zeros minus the sum of the vector angles of the poles, as shown in the figure. Usually, only the poles of the network are of consequence in determining filter stability, and this is true for determining group delay also.

Knowing that the impedance function of the filter is described by a continuous fraction enables the phase angle of the network at a given frequency to be written as:

$$\theta(\omega) = K + \tan^{-1}\frac{\omega}{\sigma_o} + \sum_{n=1}^{N} \tan^{-1}\frac{\omega-\omega_n}{\sigma_n} + \tan^{-1}\frac{\omega+\omega_n}{\sigma_n}$$

where:

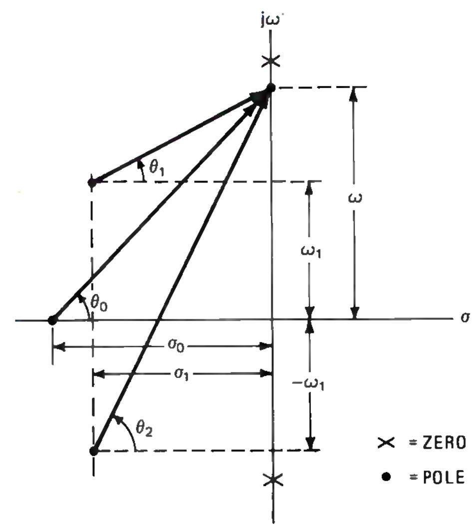
K = a network constant and is a function of the network zeros
ω = the frequency of interest
σ_o = the real pole
σ_n = the real part of complex pole n
ω_n = the absolute value of the imaginary part of complex pole n
N = the number of complex pole pairs.

The group delay may then be immediately written as:

$$\frac{d\theta(\omega)}{d\omega} \equiv t_g = \frac{\sigma_o}{\sigma_o^2+\omega^2} + \sum_{n=1}^{N} \frac{\sigma_n}{\sigma_n^2+(\omega-\omega_n^2)} + \frac{\sigma_n}{\sigma_n^2+(\omega+\omega_n)^2}$$

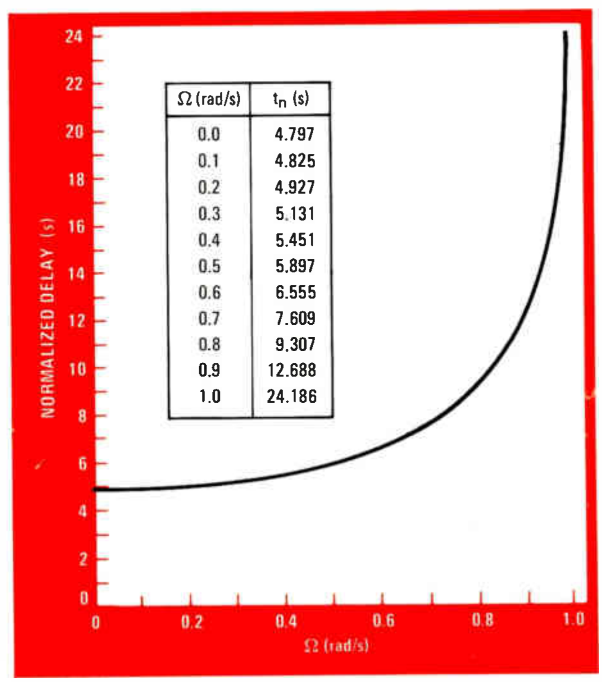
and this is the equation that the calculator solves.

Consider an example where the requirements for a low-pass filter are defined such that the group delay is to be less than 300 microseconds from 300 to 3,200 hertz and the filter is to have an upper cutoff frequency, f_c, of 3,700 Hz. Further assume that the passband ripple is to



(a)

$$t_g \equiv \frac{d\theta(\omega)}{d\omega} = \frac{\sigma_0}{\sigma_0^2+\omega^2} + \sum_{n=1}^{N} \frac{\sigma_n}{\sigma_n^2+(\omega-\omega_n)^2} + \frac{\sigma_n}{\sigma_n^2+(\omega+\omega_n)^2}$$



Ω (rad/s)	t_n (s)
0.0	4.797
0.1	4.825
0.2	4.927
0.3	5.131
0.4	5.451
0.5	5.897
0.6	6.555
0.7	7.609
0.8	9.307
0.9	12.688
1.0	24.186

(b)

Group delay. Pole-zero constellation defines transfer function of all networks, is all important to understanding derivation of group delay for Cauer filters (a). Values of normalized delay for problem discussed in text are tabulated (b).

be less than 1 decibel peak to peak and that the out-of-band rejection is to be greater than 20 decibels at 4 kilohertz, greater than 40 dB at 4.5 kHz, greater than 60 dB at 5 kHz, and greater than 80 dB at 14 kHz. The pole locations for such a filter can be determined by reference to the proper sourcebooks.[1] For this case, the poles are:

$\sigma_0 = 0.5618$
$\sigma_1 = 0.4636 \qquad \omega_1 = 0.5105$
$\sigma_2 = 0.2794 \qquad \omega_2 = 0.8319$
$\sigma_3 = 0.1335 \qquad \omega_3 = 0.9835$
$\sigma_4 = 0.0383 \qquad \omega_4 = 1.0402$

These values are stored in the appropriate registers as detailed in the program instructions. A delay time is found for each normalized frequency such that $\Omega = f/f_c$. After the results are tabulated, the denormalized group delay is found by:

$$t_g(\Omega) = [t(f_u/f_c) - t(f_l/f_c)]/2\pi f_c$$

and in this case it is:

$$t_g(\Omega) = \frac{t(3{,}200/3{,}700) - t\,(300/3{,}700)}{2\pi(3{,}700)}$$

$$= \frac{(10.8 - 4.9)s}{2\pi(3{,}700)} = 254 \text{ microseconds}$$

Thus the filter meets the group delay specification. □

References

1. Christian, Erich, and Eisenmann, Egor, "Filter Design Tables and Graphs," John Wiley & Sons, New York, 1966.

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.

SR-52 GROUP DELAY PROGRAM

Locations	Codes	Keys	Comments
000 – 005	46 11 43 00 00 40	*LBL A RCL 00 *x^2	
006 – 012	42 00 09 43 01 08 40	STO 09 RCL 18 *x^2	
013 – 019	44 00 09 43 00 00 55	SUM 09 RCL 00 ÷	$\dfrac{\sigma}{\Omega^2 + \sigma^2}$
020 – 023	43 00 09 95	RCL 09 =	
024 – 029	42 01 09 43 00 08	STO 19 RCL 08	
030 – 032	85 09 95	+ 9 =	find σ_n, clear temporary register, store σ_n^2 in register 09
033 – 036	42 01 07 36	STO 17 *IND	
037 – 043	43 00 08 40 42 00 09	RCL 08 *x^2 STO 09	
044 – 048	43 01 08 75 36	RCL 18 – *IND	find $\Omega - \Omega_n$ store $\sigma_n^2 + (\Omega - \Omega_n)^2$ in register 09
049 – 053	43 01 07 95 40	RCL 17 = x^2	
054 – 057	44 00 09 36	SUM 09 *IND	
058 – 061	43 00 08 55	RCL 08 ÷	
062 – 065	43 00 09 95	RCL 09 =	
066 – 069	44 01 09 36	SUM 19 *IND	
070 – 073	43 00 08 40	RCL 08 *x^2	
074 – 080	42 00 09 43 01 08 85	STO 09 RCL 18 +	
081 – 086	36 43 01 07 95 40	*IND RCL 17 = x^2	$\dfrac{\sigma_n}{\sigma_n^2 + (\Omega + \Omega_n)^2}$
087 – 090	44 00 09 36	SUM 09 *IND	
091 – 094	43 00 08 55	RCL 08 ÷	
095 – 098	43 00 09 95	RCL 09 =	
099 – 104	44 01 09 43 01 07	SUM 19 RCL 17	
105 – 107	75 01 95	– 1 =	
108 – 113	42 01 07 43 00 08	STO 17 RCL 08	
114 – 116	75 01 95	– 1 =	
117 – 122	42 00 08 75 01 95	STO 08 – 1 =	
123 – 126	80 00 03 06	*if pos 036	display t_g (Ω)
127 – 130	43 01 09 81	RCL 19 HLT	

Instructions

1. Key in program
2. Enter real pole value:
   (σ_0), STO 00
3. Enter the real part of each pole pair:
   (σ_1), STO 01, (σ_2), STO 02, ... (σ_7), STO 07
4. Specify the number of complex pole pairs:
   (N), STO 08
5. Enter the imaginary part of each pole pair:
   (ω_1), STO 10, (ω_2), STO 11, ... (ω_7), STO 16
6. Specify the desired normalized frequency at which the group delay distortion is to be found:
   (Ω), STO 18
7. Press A to find the normalized delay distortion, entering Ω and N for each delay calculation
8. Find $t(\Omega_u) - t(\Omega_l)$. Divide answer by $2\pi f_c$ to find the denormalized group delay

Registers

R_{00}	σ_0
$R_{01} - R_{07}$	$\sigma_1 - \sigma_7$
R_{08}	N
$R_{10} - R_{16}$	$\omega_1 - \omega_7$
R_{18}	Ω

Keeping up to date takes time

Did you ever wonder how many hours per week the average engineer spends reading technical material? And what is his greatest obstacle to keeping up to date technically? A survey of 75% of RCA's engineers, group leaders and managers, reported in the Oct./Nov. 1977 issue of the RCA Engineer, gives some interesting answers to these and related questions on engineers' information needs.

For instance, at RCA's facilities, **engineers average 11½ hours per week during and after working hours reading material relevant to their job and career.** Group leaders read the same type of material about 2½ hours more per week, and managers average 2 hours more than the leaders. Engineers do a little over 50% of their reading during work hours, and all three groups do more than 50% of their reading only for job-related technical and RCA business categories. All three categories of engineers at RCA agree that the primary obstacle to adequate reading for keeping up to date is insufficient time, both at work and outside of work.

Finally, engineers, leaders and managers rated themselves rather differently on how well they keep up with the state of the art. Engineers were pessimistic, only 28% placing themselves above average, and 35% placing themselves below average. This contrasts with leaders and managers—62% of the leaders and 57% of the managers saw themselves as above average and only 6% and 9% respectively as below.

How to generate a hyperbola with a d-a converter

Want to assemble a hyperbolic-function generator for less than $10? Precision Monolithics' AN-23 application note describes how **extended-range hyperbolic functions of the form A/X and −A/X can be generated** with a low-cost bipolar–field-effect-transistor operational amplifier and a high-speed multiplying digital-to-analog converter. Though focused on hyperbolic-function generation, the note points up generally how a d-a converter can be configured with feedback to generate functions. For further information, contact Don Soderquist, Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, Calif. 95050.

Why fine-resolution pc boards use plasma cleaning

As the width of lines and spaces on flexible and rigid printed circuitry continues to shrink below 1 mil, yields may drop if standard methods of removing film resist are used. So a few hybrid and flexible circuit firms are now borrowing a technique from the integrated-circuit industry—plasma removal of the resist. To a cloud of ionized gas ions, even 0.5-mil-wide lines and spaces are no problem since **10-to-20-micrometer features are regularly cleaned in this way during IC manufacturing.**

Tape teaches how to cool hot equipment

One undergraduate course in thermodynamics is no preparation for the practical problems of cooling electronic equipment. A good basic training in this subject is available in a 60-minute audiotape cassette and an 18-page booklet with design formulas and graphs, available free from Cooling Courses, P. O. Box 11534, Palo Alto, Calif. 94306. Topics covered at the engineering level are **heat conduction, mounting interfaces, choice of heat-transfer methods, radiation, natural convection, forced-air cooling, choice of fans,** air-cooling fins, cooling of cabinets, forced-liquid cooling, evaporation cooling, and thermal measurement techniques. **Jerry Lyman**

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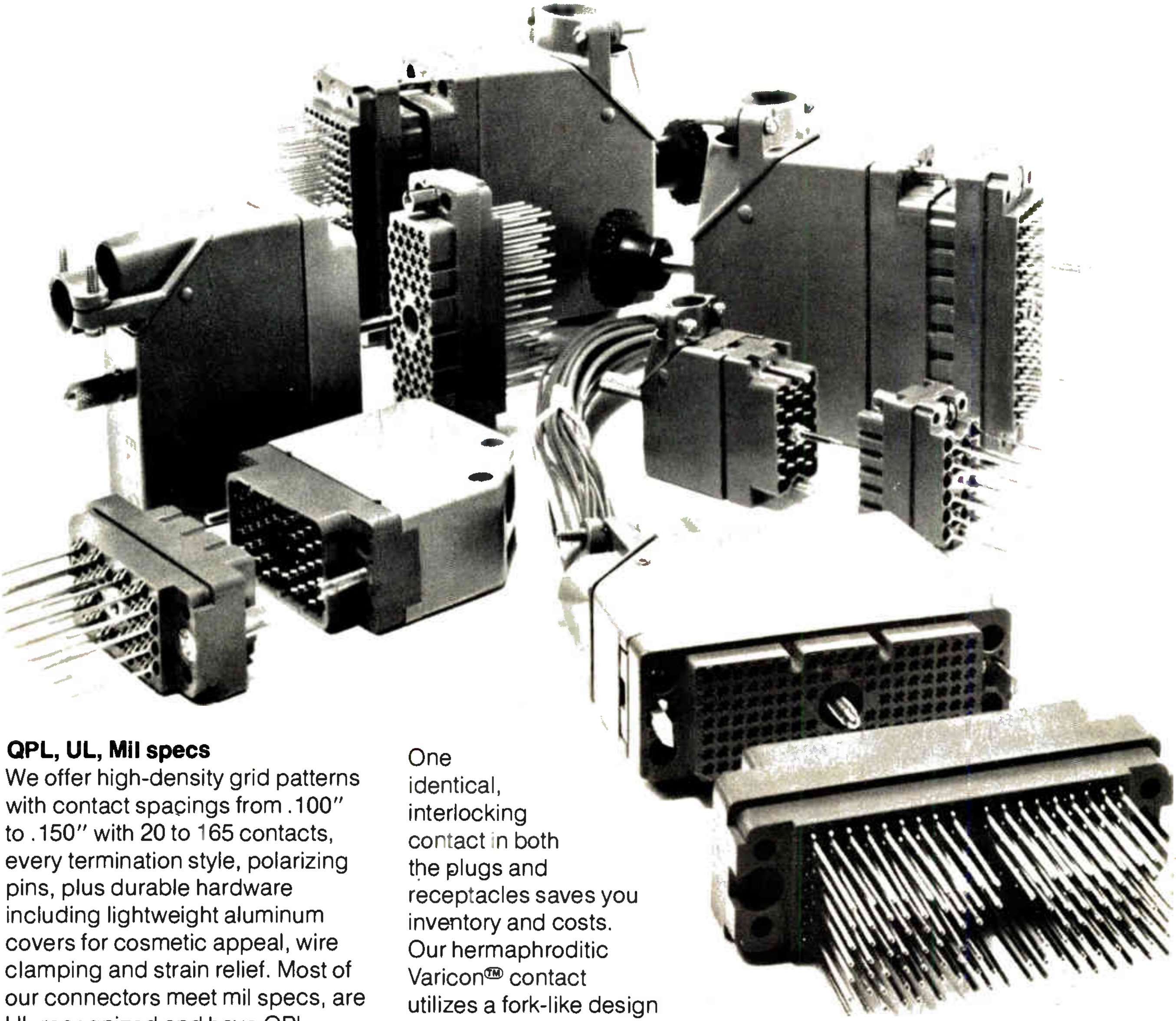

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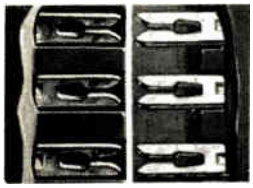

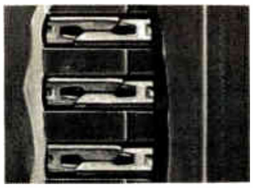

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Hybrid a-d unit breaks 2-μs barrier

Successive-approximation device in 36-pin DIP converts 12 bits in 1.8 μs; companion track-and-hold amplifier has 120-ns acquisition time

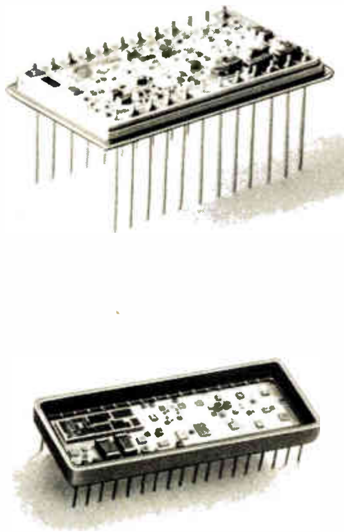
by Mike Riezenman, New Products Editor

They're not cheap, but the ADH-8516 analog-to-digital converter and the ADH-050 track-and-hold amplifier form the smallest 12-bit, 2-μs data-acquisition subsystem available today. And they're not only small, they're tough. Each of the hybrid circuits is hermetically sealed in a double-width (0.6-inch pin spacing) metal dual in-line package and processed to MIL-STD-883, class C. (Screening to class B is available as an option.)

Actually, the ADH-8516 has a typical conversion time of 1.8 μs with 2 μs specified as maximum. For applications in which the user is able to sacrifice resolution for additional speed, the converter can be short-cycled to as little as 8 bits for a typical conversion time of 1.2 μs. Previously, this kind of speed was available only in much larger converter modules fabricated with discrete circuitry.

Among the converter's many pin-programmable features are three-state outputs for microprocessor interfacing, a choice of internal or external clocking, several triggering modes, and a choice of six input-voltage ranges: 0 to +5 v, 0 to +10 v, 0 to +20 v, −2.5 to +2.5 v, −5 to +5 v, and −10 to +10 v. For all ranges the maximum allowable voltage is 1.5 times full scale.

The 8516 may be pin-programmed as a retriggerable or nonretriggerable converter. In the former mode, if a start-conversion command is received during a conversion, the ongoing conversion is aborted and a new one is started. In the latter mode, such commands are ignored until the ongoing conversion is completed. There is also a continuous-conversion mode in which the unit will begin a cycle as soon as the previous one is finished.



Fast. The ADH-050 track-and-hold amplifier (top) and the ADH-8516 analog-to-digital converter form a compact package that can acquire data to a resolution of 12 bits at a 450-kHz rate.

Key specifications of the converter include a maximum linearity error of 0.012% of full scale, a linearity-error temperature coefficient of 2 parts per million per °C, a typical gain error of 0.2% of full scale (trimmable to zero), a gain-error temperature coefficient of 20 ppm/°C, and a typical power consumption of 1.8 w. The unipolar input ranges have a typical offset error of 5 mv with a temperature coefficient of 15 μv/°C. For the bipolar ranges the figures are 10 mv and 50 μv/°C, respectively. Two operating-temperature ranges are offered: 0°C to 70°C and −25°C to +85°C.

Required power supplies are ±15 v ±3% and +5 v ±5%. Typical current drains are 23 mA from the +15-v supply, 40 mA from the −15-v supply, and 175 mA from the 5-v supply. In small quantities, the basic ADH-8516 sells for $395.

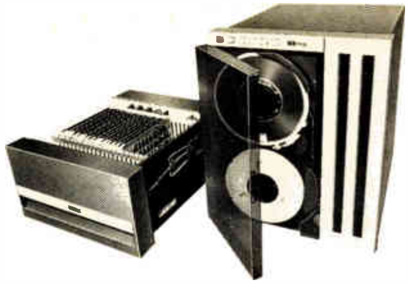
Designed to work with the a-d converter, the ADH-050 track-and-hold amplifier is a hybrid circuit that comes complete with an input buffer amplifier and a 33-pF hold capacitor. The unit has a maximum acquisition time of 120 ns (100 ns typical), a maximum aperture delay uncertainty of 500 ps, and a 25°C droop rate of no more than 1 mv/μs. This droop rate doubles for every 10°C rise.

For users who need a lower droop rate, the model ADH-051 has a 150-pF hold capacitor. This cuts the droop rate to 0.2 mv/μs while raising the maximum acquisition time to 600 ns. The larger capacitor also cuts the small-signal bandwidth of the track-and-hold stage from 15 MHz to 3.5 MHz and reduces its slew rate from 200 v/μs to 80 v/μs. It does not affect the buffer amplifier, which has a small-signal bandwidth of 5 MHz and a slew rate of 60 v/μs.

The amplifier, it should be noted, need not be used. It can be connected as a high-impedance voltage follower, as a differential amplifier, as a single-ended amplifier, or not at all.

The ADH-050 operates from −55°C to +110°C and sells for $325 in small quantities. Like the a-d converter it is available from stock to eight weeks.

ILC Data Device Corp., Airport International Plaza, Bohemia, N.Y. 11716. Phone (516) 567-5600 [338]



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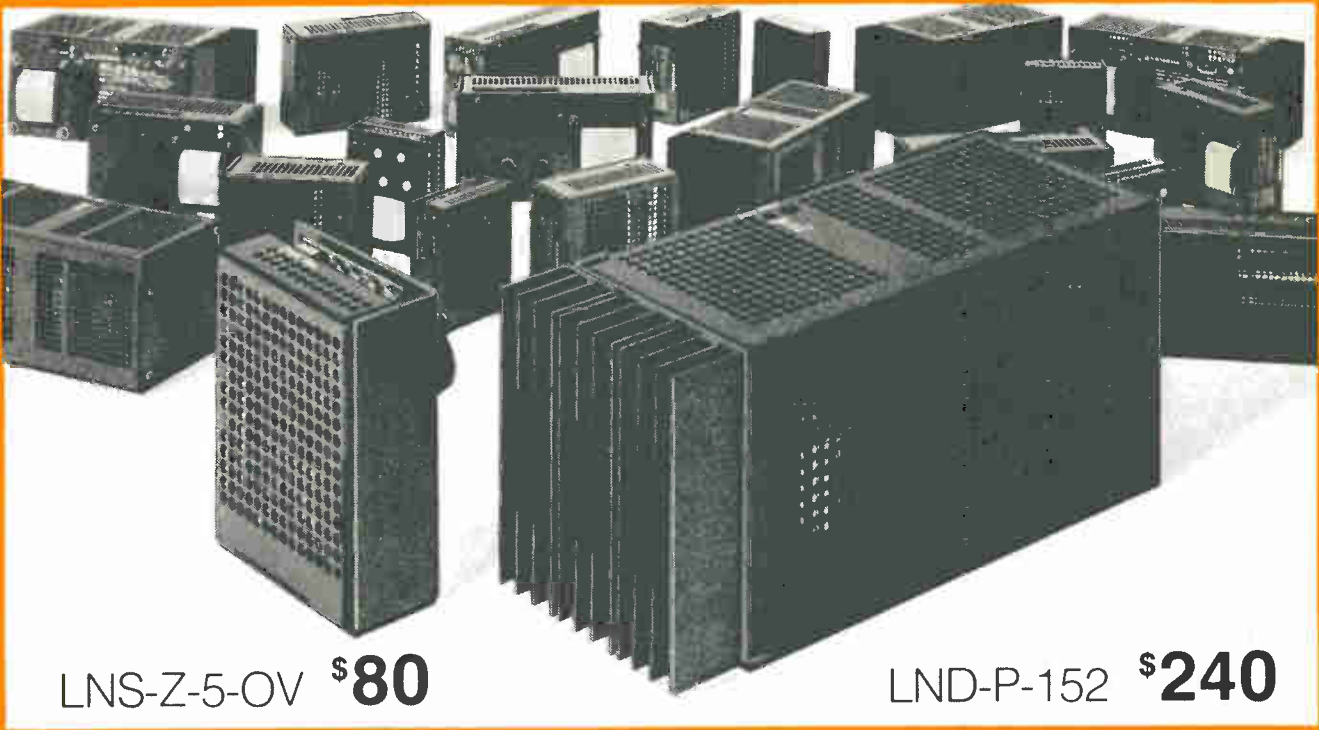

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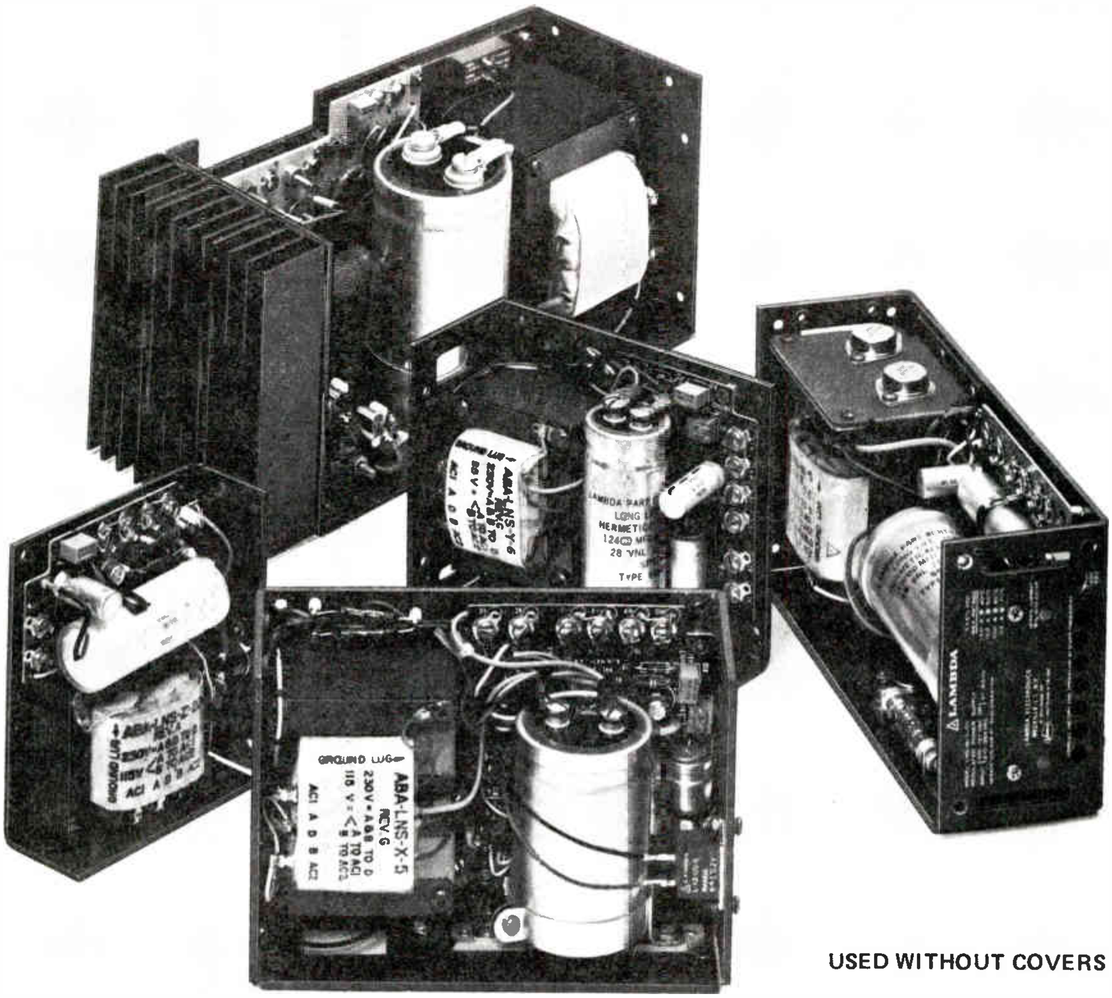

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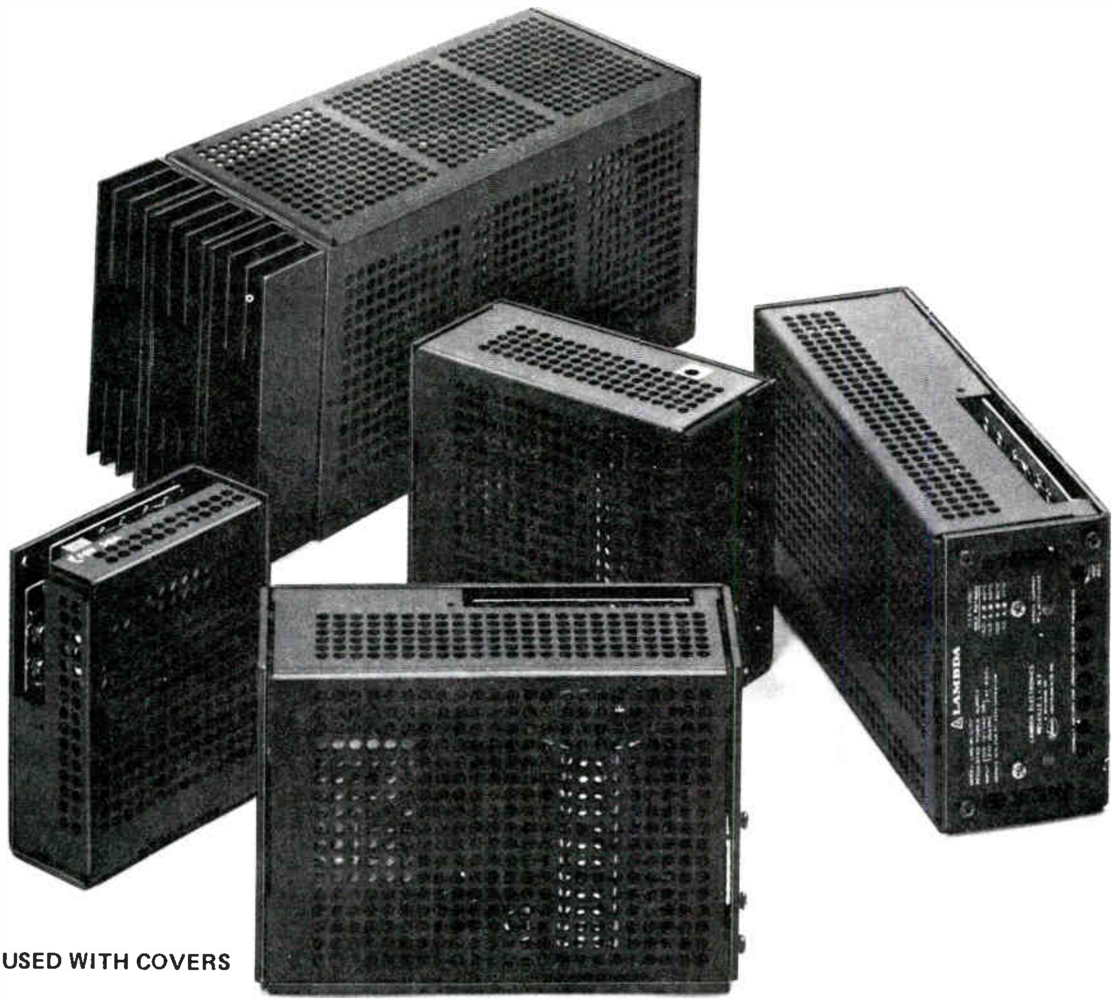

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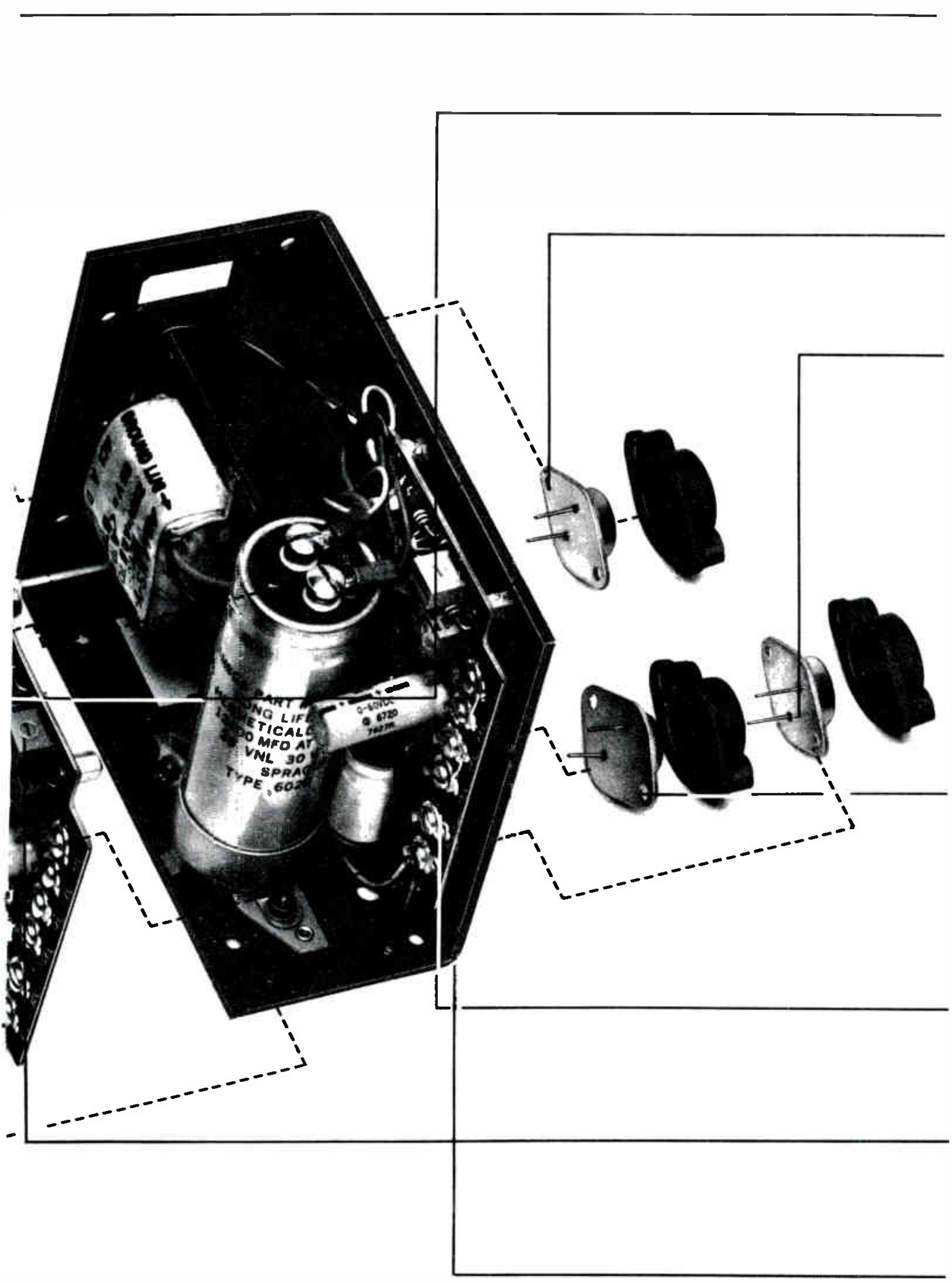

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DUAL OUTPUT

5 VOLTS ± 5% ADJ, 9V-12V ADJ

MODEL	REGULATION (LINE OR LOAD)	RIPPLE (RMS)	VOLT. VDC.	(1) MAX CURRENT AMPS AT 40°C	50°C	60°C	71°C	PKG SIZE	DIMENSIONS(2) (INCHES)	PRICE
LND-X-MPU (3)	0.1%	1.5	5±5%	7.0(5.95)	6.0(5.11)	4.7(4.0)	3.2(2.72)	X	7 x 4 7/8 x 2 7/8	$172
			9—12	1.2(1.02)	1.1(0.94)	1.0(0.85)	0.8(0.68)			
LND-P-MPU (3)	0.1%	1.5	5±5%	14.0(13.3)	12.2(11.59)	10.0(9.5)	7.5(7.13)	P	11 x 4-7/8 x 4-13/32	245
			9—12	2.5(2.38)	2.2(2.09)	1.8(1.71)	1.35(1.28)			

± 15 VOLTS TO ± 12 VOLTS ADJ — DUAL TRACKING

MODEL	REGULATION (LINE OR LOAD)	RIPPLE (RMS)	VOLT. VDC.	40°C	50°C	60°C	71°C	PKG SIZE	DIMENSIONS (INCHES)	PRICE
LND-Z-152	0.15%	1.5	±15 to	0.6(0.54)	0.55(0.5)	0.45(0.41)	0.3(0.27)	Z	4 7/8 x 4 x 1 3/4	$ 85
			± 12	0.6(0.54)	0.55(0.5)	0.45(0.41)	0.3(0.27)			
LND-Y-152	0.1%	1.5	± 15 to	1.4(1.20)	1.2(1.02)	0.9(0.77)	0.6(0.51)	Y	5 5/8 x 4 7/8 x 2 5/8	120
			± 12	1.2(1.02)	1.1(0.94)	0.8(0.68)	0.5(0.43)			
LND-X-152	0.1%	1.5	± 15 to	2.5(2.13)	2.1(1.79)	1.6(1.37)	1.1(0.94)	X	7 x 4 7/8 x 2 7/8	150
			± 12	2.3(1.96)	1.9(1.62)	1.4(1.2)	0.9(0.77)			
LND-W-152	0.1%	1.5	± 15 to	3.3(3.0)	3.1(2.8)	2.6(2.34)	2.0(1.8)	W	9 x 5 x 2 7/8	170
			± 12	3.1(2.8)	2.8(2.52)	2.3(2.07)	1.6(1.44)			
LND-P-152	0.1%	1.5	± 15 to	5.3(5.04)	4.7(4.47.	3.9(3.71)	2.9(2.76)	P	11 x 4-7/8 x 4-13/32	240
			± 12	4.6(4.37)	4.0 (3.80)	3.3(3.14)	2.5(2.38)			

SINGLE OUTPUT

MODEL	REGULATION (LINE OR LOAD)	RIPPLE (RMS)	(1) MAX CURRENT AMPS AT 40°C	50°C	60°C	71°C	PKG SIZE	DIMENSIONS(2) (INCHES)	PRICE
5 VOLTS ± 5% ADJ									
LNS-Z-5-OV	0.15%	1.5	3.0(2.7)	2.7(2.4)	2.3(2.1)	1.7(1.5)	Z	4-7/8 x 4 x 1-3/4	$ 80
LNS-Y-5-OV	0.1%	1.5	6.0(5.4)	5.1(4.6)	4.2(3.8)	3.1(2.8)	Y	5-5/8 x 4-7/8 x 2-5/8	115
LNS-X-5-OV	0.1%	1.5	10.0(8.5)	8.9(7.6)	7.3(6.2)	5.3(4.5)	X	7 x 4-7/8 x 2-7/8	140
LNS-W-5-OV	0.1%	1.5	14.0(11.9)	12.2(10.4)	10.0(8.5)	7.5(6.4)	W	9 x 5 x 2-7/8	175
LNS-P-5-OV	0.1%	1.5	22.0(20.9)	19.5(18.53)	16.5(15.68)	13.0(12.35)	P	11 x 4-7/8 x 4-13/32	220
6 VOLTS ± 5% ADJ									
LNS-Z-6	0.15%	1.5	2.5(2.25)	2.2(2.0)	1.9(1.7)	1.4(1.3)	Z	4-7/8 x 4 x 1-3/4	$ 75
LNS-Y-6	0.1%	1.5	5.6(5.0)	4.9(4.4)	4.0(3.6)	2.9(2.61)	Y	5-5/8 x 4-7/8 x 2-5/8	110
LNS-X-6	0.1%	1.5	9.5(8.1)	8.4(7.15)	7.1(6.0)	5.0(4.25)	X	7 x 4-7/8 x 2-7/8	130
LNS-W-6	0.1%	1.5	13.0(11.0)	11.2(9.5)	9.3(7.9)	6.8(5.9)	W	9 x 5 x 2-7/8	165
LNS-P-6	0.1%	1.5	20.5(19.48)	18.1(17.2)	15.3(14.54)	12.0(11.4)	P	11 x 4-7/8 x 4-13/32	200
12 VOLTS ± 5% ADJ									
LNS-Z-12	0.15%	1.5	1.7(1.55)	1.6(1.45)	1.5(1.4)	1.3(1.2)	Z	4-7/8 x 4 x 1-3/4	$ 75
LNS-Y-12	0.1%	1.5	4.0(3.6)	3.5(3.15)	2.9(2.6)	2.2(2.0)	Y	5-5/8 x 4-7/8 x 2-5/8	110
LNS-X-12	0.1%	1.5	6.5(5.5)	5.5(4.7)	4.5(3.8)	3.3(2.8)	X	7 x 4-7/8 x 2-7/8	130
LNS-W-12	0.1%	1.5	8.5(7.2)	7.2(6.1)	5.9(5.0)	4.2(3.6)	W	9 x 5 x 2-7/8	165
LNS-P-12	0.1%	1.5	14.0(13.3)	12.4(11.8)	10.0(9.5)	7.3(6.94)	P	11 x 4-7/8 x 4-13/32	200
15 VOLTS ± 5% ADJ									
LNS-Z-15	0.15%	1.5	1.4(1.3)	1.3(1.62)	1.2(1.1)	1.0(0.9)	Z	4-7/8 x 4 x 1-3/4	$ 75
LNS-Y-15	0.1%	1.5	3.4(3.1)	3.1(2.8)	2.6(2.35)	2.0(1.8)	Y	5-5/8 x 4-7/8 x 2-5/8	110
LNS-X-15	0.1%	1.5	5.5(4.7)	4.8(4.1)	3.9(3.35)	2.8(2.4)	X	7 x 4-7/8 x 2-7/8	130
LNS W-15	0.1%	1.5	7.7(6.55)	6.7(5.7)	5.5(4.7)	3.8(3.15)	W	9 x 5 x 2-7/8	165
LNS-P-15	0.1%	1.5	12.0(11.4)	10.6(10.1)	8.5(8.1)	6.3(6.0)	P	11 x 4-7/8 x 4-13/32	200
20 VOLTS ± 5% ADJ									
LNS-Z-20	0.15%	1.5	1.0(0.69)	0.85(0.77)	0.65(0.59)	0.45(0.41)	Z	4-7/8 x 4 x 1-3/4	$ 75
LNS-Y-20	0.1%	1.5	2.7(2.45)	2.5(2.25)	2.0(1.08)	1.3(1.2)	Y	5-5/8 x 4-7/8 x 2-5/8	110
LNS-X-20	0.1%	1.5	4.4(3.75)	3.6(3.1)	2.6(2.2)	1.6(1.4)	X	7 x 4-7/8 x 2-7/8	130
LNS-W-20	0.1%	1.5	6.1(5.2)	5.2(4.4)	4.2(3.6)	3.0(2.6)	W	9 x 5 x 2-7/8	165
LNS-P-20	0.1%	1.5	10.0(9.5)	8.9(8.46)	7.5(7.13)	5.5(5.23)	P	11 x 4-7/8 x 4-13/32	200
24 VOLTS ± 5% ADJ									
LNS-Z-24	0.15%	1.5	0.9(0.81)	0.75(0.68)	0.6(0.55)	0.4(0.36)	Z	4-7/8 x 4 x 1-3/4	$ 75
LNS-Y-24	0.1%	1.5	2.3(2.1)	2.1(1.9)	1.7(1.5)	1.1(1.0)	Y	5-5/8 x 4-7/8 x 2-5/8	110
LNS-X-24	0.1%	1.5	3.8(3.25)	3.2(2.75)	2.4(2.0)	1.4(1.62)	X	7 x 4-7/8 x 2-7/8	130
LNS-W-24	0.1%	1.5	5.4(4.6)	4.6(3.9)	3.7(3.1)	2.5(2.1)	W	9 x 5 x 2-7/8	165
LNS-P-24	0.1%	1.5	9.0(8.55)	8.0(7.6)	6.7(6.37)	5.0(4.75)	P	11 x 4-7/8 x 4-13/32	200
28 VOLTS ± 5% ADJ									
LNS-Z-28	0.15%	1.5	0.8(0.75)	0.65(0.6)	0.5(0.45)	0.35(0.32)	Z	4-7/8 x 4 x 1-3/4	$ 75
LNS-Y-28	0.1%	1.5	2.0(1.8)	1.8(1.65)	1.5(1.35)	1.0(0.9)	Y	5-5/8 x 4-7/8 x 2-5/8	110
LNS-X-28	0.1%	1.5	3.4(2.9)	2.9(2.5)	2.2(1.5)	1.2(1.0)	X	7 x 4-7/8 x 2-7/8	130
LNS-W-28	0.1%	1.5	4.7(4.0)	4.0(3.4)	3.2(2.75)	2.2(1.9)	W	9 x 5 x 2-7/8	165
LNS-P-28	0.1%	1.5	8.0(7.6)	7.1(6.75)	6.0(5.7)	4.5(4.28)	P	11 x 4-7/8 x 4-13/32	200

NOTE: 1. Rating in Parenthesis for LN Series when cover is used
2. Dimensions include cover
3. Includes OV protection on both outputs (5V OV trip point is 6.6 ± .2V fixed; 9—12V OV trip points is 13.7 ± .4V fixed)

SPECIFICATIONS OF LN SERIES

DC Output

Voltage range shown in tables

Regulated Voltage

regulation, line ..... 0.1% (0.15% for LN-Z)
regulation, load ..... 0.1% (0.15% for LN-Z)
ripple and noise ..... 1.5mv RMS, 5mV pk-pk with either positive or negative terminal grounded.
temperature coefficient .... 0.03% /°C
remote programming resistance .... 200 ohms per volt nominal
remote programming voltage .... volt per volt

AC Input

line .... 105-127 VAC, 210-254 VAC (by transformer tap change) 47-440 Hz. Consult factory for operation at frequencies other than 57-63 Hz.
Efficiency (Typical) . . 30%-5V and 6V models, 42% 12V and 15V models, 49%-20V, 24V and 28V models. 42% for LN duals except LND-MPU which are 34%.

Ambient Operating Temperature Range

Continuous duty from 0° to +71°C with corresponding load current ratings for all modes of operation.

Storage Temperature Range

–55°C to 85°C

Overload Protection

Electrical

External overload protection, automatic electronic current limiting circuit limits the output current to a preset value, thereby providing protection for the load as well as the power supply.

Thermal

Thermostat – automatically reset when overtemperature condition is eliminated.

Overshoot

No overshoot on turn-on, turn-off or power failure.

Overvoltage Protection

Overvoltage protection module crowbars output when trip level is exceeded – standard on all 5V models and both outputs of models LND-X-MPU and LND-P-MPU. For other models see back cover.

Input and Output Connections

Heavy-duty screw terminals on printed circuit board.

DC Output Controls

Simple screwdriver adjustment over the entire voltage range.

Tracking Accuracy (Dual Tracking Models Only)

3% absolute voltage difference, 0.2% change for all conditions of line, load and temperature.

Remote Sensing

Provision is made for remote sensing to eliminate effect of power output lead resistance on DC regulation.

Mounting

Three Mounting surfaces, three mounting position. One mounting position for LN-P models.

Convection Cooled

No external heat sinking or forced air required.

Transformer

MIL-T-27C, Grade 6; Electrostatic shield; 4000 VAC input/output isolation.

Isolation Rating

Minimum 10 Megohm isolation from DC to ground at ground at 1000 VDC.

Fungus Proof

No fungi nutrient material used.

Military Specifications

The LNS series has passed the following tests in accordance with MIL-STD-810C:

1) Low Pressure – Method 500.1, Procedure I.
2) High Temperature – Method 501.1, Procedure I & II.
3) Low Temperature – Method 502.1, Procedure I.
4) Temperature Shock – Method 503.0, Procedure I.
5) Temperature – Altitude – Method 504.1, Procedure I. Class 2 (0°C operating)
6) Humidity – Method 507.1, Procedures I & II.
7) Fungus – Method 508.1, Procedure I.
8) Vibration – Method 514.2, Procedures X & XI.
9) Shock – Method 516.2, Procedures I & III.

MIL-I-6181D – Conducted and radiated EMI with one output terminal grounded.

Physical Data

Package Model	Weight Lbs. Net	Weight Lbs. Ship	Size Inches
LN-Z	3	3-1/4	4-7/8 x 4 x 1-3/4 (w/cover) 4-7/8 x 4 x 1-5/8 (w/o cover)
LN-Y	5	5-1/2	5-5/8 x 4-7/8 x 2-5/8 (w/cover) 5-5/8 x 4-7/8 x 2-1/2 (w/o cover)
LN-X	7-3/4	8-1/4	7 x 4 7/8 x 2-7/8 (w/cover) 7 x 4-7/8 x 2-3/4 (w/o cover)
LN-W	9	9-1/2	9 x 5 x 2-7/8 (w/cover) 9 x 4-7/8 x 2-3/4 (w/o cover)
LN-P	14	15-1/2	11 x 4-7/8 x 4-13/32 (w & w/o cover)
LND-P	15-1/2	17	11 x 4-7/8 x 4-13/32 (w & w/o cover)

Finish

Gray, Fed. Std. 595 No. 26081.

UL/VDE

Designed for listing in UL Recognized Components Index.
Designed for listing in VDE Index.

Accessories

Overvoltage protectors (standard on 5V models and models LND-X-MPU and LND-P-MPU).

Guaranteed for 5 Years

5-year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of 5 years.

6 Amp Monolithic OV Protectors
$5.00 Qty 1 $3.40 Qty 1000

TO-3 PACKAGE, NO EXTERNAL COMPONENTS NEEDED

LAMBDA OVERVOLTAGE PROTECTORS
L-6-OV, L-12-OV, L-20-OV, L-35-OV Series

General Description

The Lambda overvoltage protector prevents damage to the load caused by excessive power supply output voltage due to improper adjustment, improper connection, or failure of the power supply. Load protection is accomplished automatically by effectively short circuiting the output terminals of the power supply when a preset limit voltage has been exceeded. The trip-point limit voltage cannot be adjusted. To reset overvoltage protector, remove AC input to power supply allow overvoltage protector to cool, and reapply power.

Overvoltage Protector Performance Specifications

PARAMETER	SYMBOL	L-6-OV SERIES MIN	MAX	L-12-OV SERIES MIN	MAX	L-20-OV SERIES MIN	MAX	L-35-OV SERIES MIN	MAX
On State Current	I_{OC}	–	6A	–	12A	–	20A	–	35A
On State Voltage	V_{DC}	–	2.5V	–	1.3V	–	1.4V	–	1.6V
Non-Repetitive Peak Surge Current*	I_p	–	70A	–	200A	–	260A	–	350A
Standby Current	I_S	–	25mA	–	5mA	–	5mA	–	5mA
Operating Temperature (Blocking)**	T_{CB}	-40°C	+100°C	-40°C	+100°C	-40°C	+100°C	-40°C	+100°C
Operating Temperature (Conducting)***	T_{CC}	-40°C	+150°C	-40°C	+140°C	-40°C	+140°C	-40°C	+140°C
Storage Temperature	T_S	-40°C	+150°C	-40°C	+125°C	-40°C	+125°C	-40°C	+125°C
Power Dissipation @ 25°C Derate @ 1.5W/°C above 50°C	P_D		150 Watts						
Thermal Resistance	$R_{\theta JC}$		1.0°C/W						

*For sinusoidal current duration of 8.3 milliseconds max.

**Case temperature for overvoltage protector in non-conducting or "OFF" state.

***Case temperature for overvoltage protector in conducting or "ON" state. Power must be removed and case temperature allowed to drop to 100°C before application of output voltage.

The overvoltage protector must be mounted on external heat sink to maintain case temperature below rated limit. When the overvoltage protector is used with a Lambda power supply, the power supply chassis acts as the heat sink. The L-12-OV, L-20-OV, L-35-OV, overvoltage protector is supplied with mating connectors for pins on overvoltage protector (+V and -V engraved on unit).

OVERVOLTAGE PROTECTORS

NOM SUPPLY VOLTAGE (VOLTS)	TRIP POINT VOLTAGE^ (VOLTS)	6 AMP MODELS	PRICE QTY 1	QTY 100	QTY 250	QTY 1000	12 AMP MODELS	PRICE QTY 1	QTY 100	QTY 250	QTY 1000	20 AMP MODELS	PRICE QTY 1	QTY 100	QTY 250	QTY 1000	35 AMP MODELS	PRICE QTY 1	QTY 100	QTY 250	QTY 1000
5	6.6 ± .2	L-6-OV-5	$5	$4	$3.75	$3.40	L-12-OV-5	$11	$8	$7.50	$6.80	L-20-OV-5	$16	$11.20	$10.50	$9.50	L-35-OV-5	$20	$14.40	$13.60	$12.30
6	7.3 ± .2	L-6-OV-6	5	4	3.75	3.40	L-12-OV-6	11	8	7.50	6.80	L-20-OV-6	16	11.20	10.50	9.50	L-35-OV-6	20	14.40	13.60	12.30
9	10.5 ± .4	L-6-OV-9	5	4	3.75	3.40	L 12 OV 9	11	8	7.50	6.60										
10	11.0±.5	L 6 OV 10	5	4	3.75	3.40															
12	13.7 ± .4	L-6-OV-12	5	4	3.75	3.40	L-12-OV-12	11	8	7.50	6.80	L-20-OV-12	16	11.20	10.50	9.50	L-35-OV-12	20	14.40	13.60	12.30
15	17.0 ± .5	L-6-OV-15	5	4	3.75	3.40	L-12-OV-15	11	8	7.50	6.80	L-20-OV-15	16	11.20	10.50	9.50					
18	20.5±1.0	L 6 OV 18	5	4	3.75	3.40															
20	22.8 ± .7	L-6-OV-20	5	4	3.75	3.40	L-12-OV-20	11	6	7.50	6.80	L-20-OV-20	16	11.20	10.50	9.50					
24	27.3 ± .6	L-6-OV-24	5	4	3.75	3.40	L 12-OV-24	11	6	7.50	6.80	L-20-OV-24	16	11.20	10.50	9.50					
28	31.9 ± 1.0	L 6 OV-28	5	4	3.75	3.40	L-12-OV-28	11	6	7.50	6.80	L 20-OV-28	16	11.20	10.50	9.50					
30	33.5 ± 1.0						L-12-OV-30	11	8	7.50	6.80	L 20-OV-30	16	11.20	10.50	9.50					

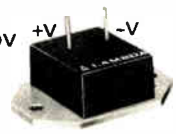
^VOLTAGE TOLERANCE MAINTAINED OVER 0-71°C DUE TO POWER DESIGN

TO 3

L6 OV

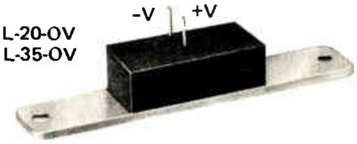
MONOLITHIC

L-12-OV



1-1/2 x 11/16 x 3/4 (inches)

L-20-OV
L-35-OV



3-3/8 x 15/32 x 19/32 (inches)

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Tel. 215 279-5644

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←Circle 121 on reader service card

is transistor-transistor-logic-compatible, and has three-state data outputs. Also, the operations mode, baud rate, and synchronous character of the unit can be changed through the use of external control.

This chip can be used in such equipment as telephone systems, modems, and cathode-ray-tubes and other types of terminals. The μPD379 is priced at $16 each in 100-unit quantities.

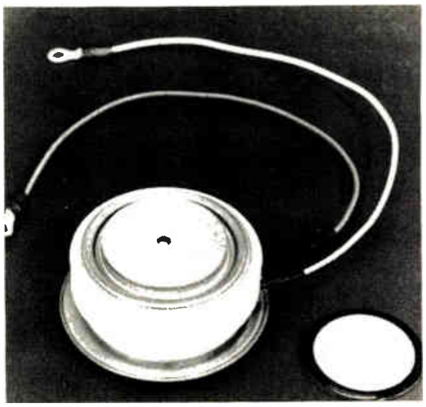
NEC Microcomputers Inc., 5 Militia Dr., Lexington, Mass. 02173. Phone (617) 862-6410 [412]

Two fast-switching SCRs rated at 10 and 25 μs

Motor controls and uninterruptible power supplies are the major applications for which two fast-switching silicon controlled rectifiers have been developed. One switches in 10 μs and has ratings of 100 to 800 V, 400 to 475 A average current. The other switches in 25 μs and is rated at 350 A average current and at voltages up to 1,200 V.

Applications for the 10-μs SCR include ac motor control and electric-vehicle chopper controls. Unit price of the 400-A, 800-V device is $288.50 in quantities of 1 to 9.

The 25-μs device can be used for induction-heating and motor control inverters. The 350-A, 1,200-V device is priced at $326.25 each in quantities of 1 to 9.



Semiconductor Div., Westinghouse Electric Corp., Youngwood, Pa., 15697. Phone (412) 925-7272 [413]

Monolithic 10-bit converter has 250-ns settling time

Intended for use in one- and two-quadrant multiplying circuits, one-quadrant dividers, digitally controlled attenuators, and fast fixed-reference digital-to-analog converters, the model DAC-IC10BC monolithic 10-bit d-a converter achieves a 250-ns settling time for a full-scale output change. Linearity is ±½ least significant bit typical and ±1 LSB maximum. Any external reference current programs the scale factor and may be varied over a 4-to-1 range. Output current is 0 to 4 mA with an output voltage compliance of −2.5 V to +0.2 V.

Power supply requirement is +5 V and −15 V with a typical power dissipation of 220 mW. Price is $10.95 in 1–24 quantities, and availability is from stock.

Datel Systems Inc., 1020 Turnpike St., Canton, Mass. 02021. Phone (617) 828-8000 [415]

Solderless process yields durable SCRs

Thanks to a construction process developed in West Germany, a new series of silicon controlled rectifiers boasts test results of 200,000 thermal cycles versus an average of only 10,000 cycles for similar devices.

The FMC series 240 and series 300 are produced with a free-floating-silicon construction designed by FMC licensee Brown Boveri & Cie. Because it is a solderless technique, the flatpack SCRs do not fail as quickly as soldered devices from thermal fatigue. The series 240 is rated at 255 A, 400 A rms, and has a case tempco of 87°C. Comparable figures for the series 300 are 300 A average, 470 A rms, and 87°C.

User can choose a dv/dt rating including a full 1,000-V/μs or 200-, 300-, or 500-V/μs performance. Prices for the series 240 (200 V/μs) begin at $105 in quantities of 1 to 4 and for the series 300 (200 V/μs),

$110 in quantities of 1 to 4. Delivery is immediate.

FMC Semiconductor Products Division, 800 Hoyt St., Broomfield, Colo. 80020. Phone (303) 469-2161 [414]

7.5-A power transistors rated up to 400 V

Three power transistors, models XGSQ7530, XGSQ7535, and XGSQ7540, feature a V_{CEO} of 300 V, 350 V, and 400 V respectively. These devices are both current-gain- and saturation-voltage-rated at 7.5 A. Peak collector current is 15 A.

Switching speeds are typically less than 1 μs at 7.5 A, while collector saturation voltages are typically 0.3 V. Applications include high-speed switching, power conversion, converters, inverters, and Class C and D amplifiers. The devices are packaged in TO-66 metal cases.

Prices for 1–99 quantities are $5.85 XGSQ7530, $6.25 for the XGSQ7535, and $7.10 for the XGSQ7540. In quantities of 100–999, prices are $4.65, $5, and $5.65 respectively. Delivery is from stock.

General Semiconductor Industries Inc., 2001 W. 10th Pl., Tempe, Ariz. 85281. Phone Jim Williams at (602) 968-3101 [417]

Darlington transistors geared for industrial motors

Three monolithic Darlington transistors, SVT6060, 6061, and 6062, are aimed at high-speed power circuits that operate at switching frequencies of 10 kHz and higher. They have a dc current gain of 30 at 15 A and peak collector current of 25 A. Rise time is 0.4 μs, and fall time is 1.0 μs. Junction temperature range is $-50°$ C to $+150°$ C, and power dissipation is 96 W.

The SVT6060 sells for $5 to $6 in quantities of 100 to 999. Delivery is from 4 to 8 weeks.

Electronic Components Division of TRW Inc., 14520 Aviation Blvd., Lawndale, Calif. 90260. Phone (213) 679-4561 [416]

Data handling

Basic interpreter aimed at hardhats

Programming in high-level language gets 8080-based systems running quickly

Most process-control engineers will welcome any aid in adapting to microprocessor-based controls. Now help is available for those building 8080-based controllers: they can do all their programming in a high-level language and avoid assembly-language altogether by using a Basic interpreter geared toward process control.

Xybasic, sold through the Mark Williams Co., Chicago, Ill., has two parts: a 7-kilobyte interpreter with built-in editor, and a 5-kilobyte compiler/run-time package, which lets programs be put directly into programmable read-only memory. After loading Xybasic into a development system or microcomputer, the user simply writes a program and then debugs it interactively at a terminal in Basic.

Without a high-level programming aid, the normal process requires writing the program in the 8080's mnemonic code, loading it into an editor and then into an assembler, and assembling, reloading, executing, and finally debugging it. Any changes require repetition of all the above steps.

With the Xybasic package, however, all that is needed is to load the interpreter into the microcomputer (from either paper tape, cassette tape, or floppy disk), run through a short initial dialog, type in the program in Basic, and execute it. If a bug is found, the program can be changed and executed again without the need for any additional loading.

Besides the standard Basic commands, Xybasic has many features that make it especially useful for process control. In such applications, which often involve a lot of switching on and off of valves at several locations, a high-level language must permit easy bit manipulation and access to ports and registers at the machine level—and Xybasic does that. PEEK and POKE commands let the user examine and modify any locations in the computer's memory. IN and OUT commands allow input and output at the machine level. Each individual bit on any port can be looked at with the SENSE command.

A DELAY command, not found in standard Basic, lets real-time delays be built into a program and can save the cost of adding a real-time clock to a computer system. Another aid is Xybasic's software-interrupt feature. For example, if a process is to be heated to a certain temperature, an interrupt can be inserted that continuously monitors a digital thermometer. The program will automatically shut down the heat once it reaches the desired temperature, which is entered at the keyboard.

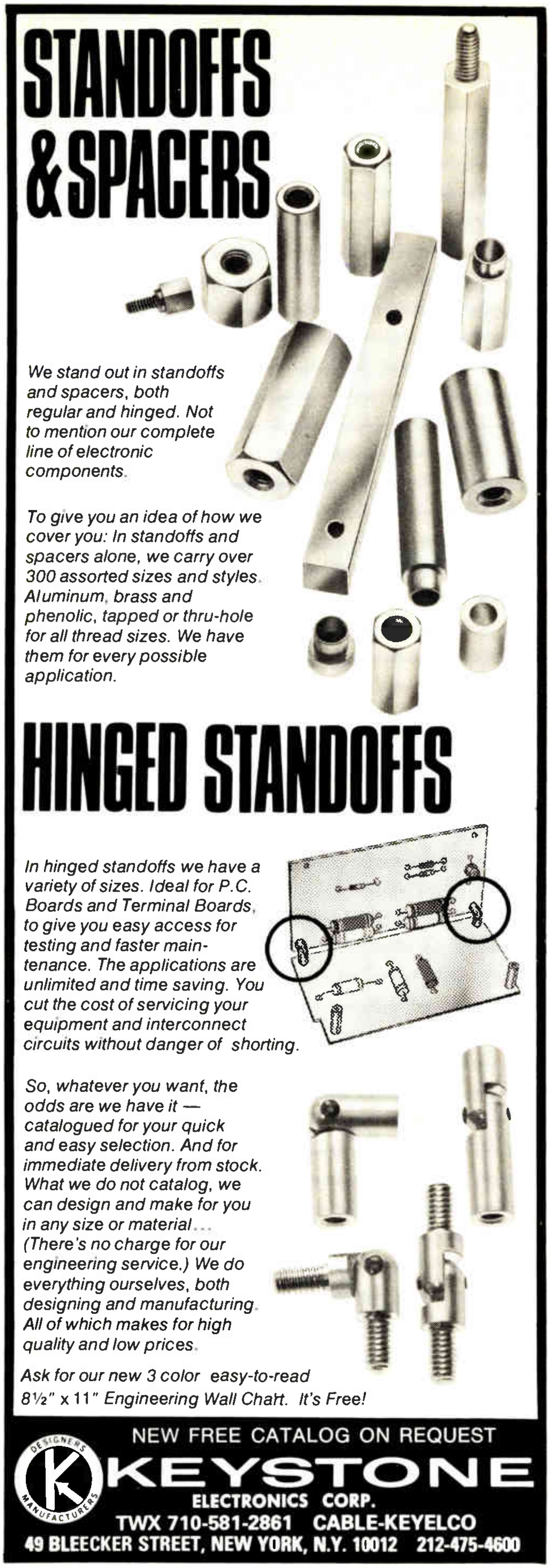
Xybasic incorporates a powerful direct mode that makes the computer behave almost like a calculator, yielding instant responses. Normally, a program is written with numbered statements and then executed. But with the direct mode, each command is executed immediately after it is typed in, making it a quick means of testing and debugging. In the direct mode a value can be put into or read from an I/O port directly.

Xybasic is available immediately at $295 each for the interpreter and compiler/run-time package. The manual can be bought for $20.

Mark Williams Co., 1430 W. Wrightwood Ave., Chicago, Ill. 60614. Phone (312) 472-6659 [361]

Distributed computer system emphasizes communications

The level 66/DPS is a large-scale distributed-processing system with a 64-kilobyte minicomputer-based integrated network processor that accepts up to 96 communications lines. The communications-oriented computer, in its basic configuration, includes twin information processors in one cabinet, a single systems control unit, an input/output multiplexer, and 1 megabyte of main memory. A single operating system controls both information processors. The price of the basic system is $957,215 with a monthly maintenance fee of $3,350. The same system is available on a five-year lease for $23,405 per month. Main memory can be added in increments



of 512 kilobytes to the 2-megabyte level, then in 1-Mbyte increments to a maximum of 8 Mbytes.

Honeywell Information Systems, 200 Smith St., Waltham, Mass. 02154. Phone (617) 890-8400, Ext. 3247 [363]

Add-on memory board stores 5 megabytes

Claimed to be the industry's largest add-on memory system, the MK 8600 is a versatile memory chassis with a total capacity of 5 megabytes. Intended both for mainframe add-on and for disk replacement, the chassis uses Mostek's MK 8000 memory card. Standard access time is 250 ns with a cycle time of 450 ns. Units with access times below 200 ns are available on request.

The MK 8600 chassis can be configured to hold up to 16 MK 8000 boards, each of which can provide from 16,384 18-bit words to 131,072 24-bit words. In addition there are four slots for I/O boards and such features as byte control, busable addresses and data, and a choice of either inverted or noninverted data.

For applications that do not require the 5-megabyte capacity of the MK 8600, Mostek is offering the 1-megabyte MK 8601. The units have a delivery time of 60 days. Price depends upon size and speed of memory and on interface requirements.

Mostek Memory Systems, 1215 West Crosby Rd., Carrollton, Texas 75006. Phone Bill Smith at (214) 242-0444, Ext. 2554 [364]

Communications

Fiber-optic links work to 20 MHz

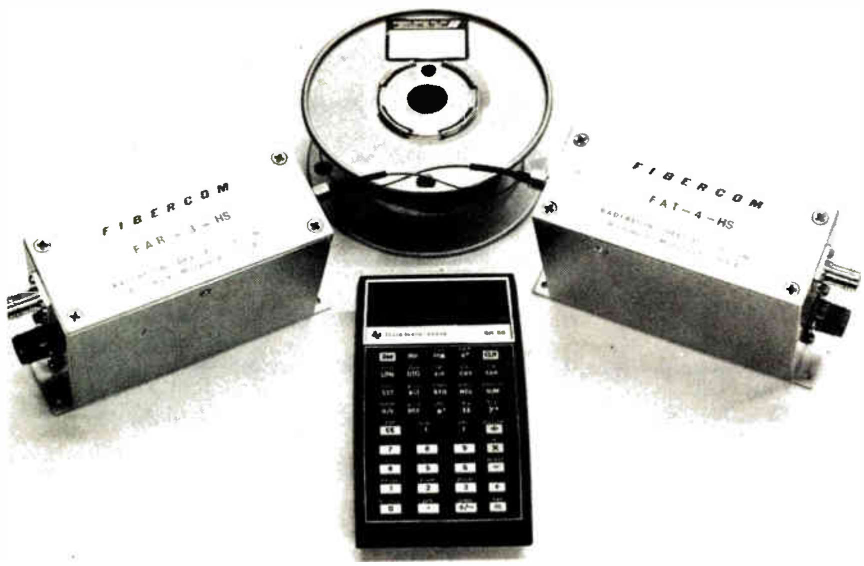
For use over distances of a few meters to about a kilometer, a family of fiber-optic analog links can operate at frequencies of 10 Hz to 20 MHz. Key specifications of the system are a minimum signal-to-noise ratio of 50 dB at a peak-to-peak input of 1 V, 1% maximum nonlinearity, 5% maximum pulse overshoot, and gain flatness within ±1 dB.

The standard models operate from a line voltage of 115 V at 40 to 400 Hz, but dc-powered models are also available. These require only a single supply in the range of +15 to +24 V. Units in the Fibercom line are well suited for applications in baseband color TV transmission, pulse monitoring, and the distribution of standard time and frequency signals in noisy environments.

Various nonstandard models with different optical wavelengths and power levels are available, as is a model with high-impedance input circuitry in the transmitter for use with oscilloscope probes. Users who want to exploit the system's full 20-MHz bandwidth must buy the optional high-speed photodetector. A variety of light- and heavy-duty single-fiber optical cables is also available.

The basic system, without cable, sells for $725. It is available from stock to four weeks.

Radiation Devices Co., P. O. Box 8450, Baltimore, Md. 21234. Phone (301) 628-2240 [401]



19,200-b/s modem operates over 25-mile wire links

Com-Link III is a short-haul modem that operates at strap-selectable speeds of 2,400 to 19,200 bits per second over wire circuits up to 25 miles long. The synchronous modem achieves its 25-mile range by combining automatic adaptive equalization with delay modulation. It has an error rate of less than 1 in 10^5.

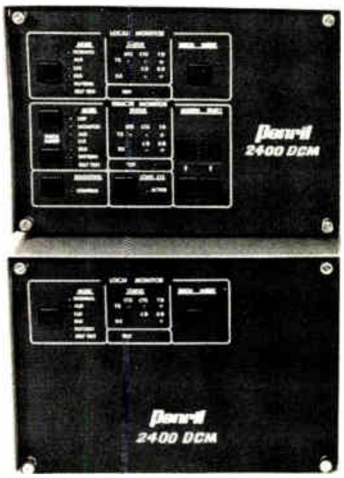
The new modem, which can be used in point-to-point and multipoint data-communications systems, is exceptionally easy to test. A remote test feature allows an operator at either end of a point-to-point line to put the line into a digital loopback mode for fault isolation without involving anyone at the other site. A built-in test-pattern generator and error detector allow fast modem checks on site.

Powered by a 4-W wall-plug-in transformer, the modem measures 1.75 inches high, 8 in. wide, and 12 in. deep. Its standard transformer operates on ac line voltages of 105 to 125 V.

Racal-Milgo Inc., 8600 N. W. 41st St., Miami, Fla. 33166. Phone (305) 592-8600 [403]

Modems include diagnostic and control functions

Designed to provide inexpensive control of a communications network, the 2400 DCM is a 2,400-bit-per-second synchronous modem with extensive built-in diagnostic and control circuitry. The circuitry, which is contained in both the master and remote-site modems, provides in effect a secondary channel for testing and control without interfering with mainstream transmission. Standard features of the 2400 DCM include a built-in test-pattern generator and detector, an RS-232-C interface, and compatibility with Bell System model 201B



and model 201C data sets.

The master 2400 DCM sells for $1,600; the remote unit is priced at $1,300. Delivery time is 60 days.

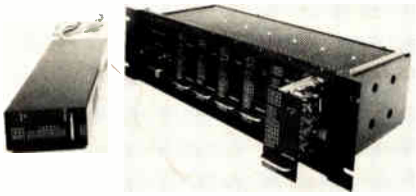
Penril Corp., 5520 Randolph Rd., Rockville, Md. 20852. Phone (301) 881-8151 [404]

Low-speed modem features automatic answering

A two-wire modem for the automatic answering of computer call-ups, the P-113D is an asynchronous unit that operates at data rates of 0 to 300 bits per second. It can be used in both half- and full-duplex modes and can be connected to the two-wire dial-up network through a 97A or 97B jack; a data-access arrangement (DAA) is not required.

The frequency-shift-keying modem transmits at levels from −3 to −12 dBm, programmable by a resistor in the 97B jack. Its receiver sensitivity is −48 dBm. The mark frequency is 2,225 Hz; the space frequency is 2,025 Hz.

The P-113D provides complete built-in diagnostics: the front panel has nine light-emitting-diode indicators that continually report operating status. A board-only version of the modem, which comes with a front panel but no case or power supply, sells for $250. A stand-alone version, complete with circuit board



and power supply, costs $370. The board-only unit measures 2 in. by 4 in. by 7.5 in. The stand-alone model is a cabinet 2.5 in. by 4.5 in. by 11.5 in. Delivery time is 45 days.

Prentice Corp., 795 San Antonio Rd., Palo Alto, Calif. 94303. Phone (415) 494-7225 [406]

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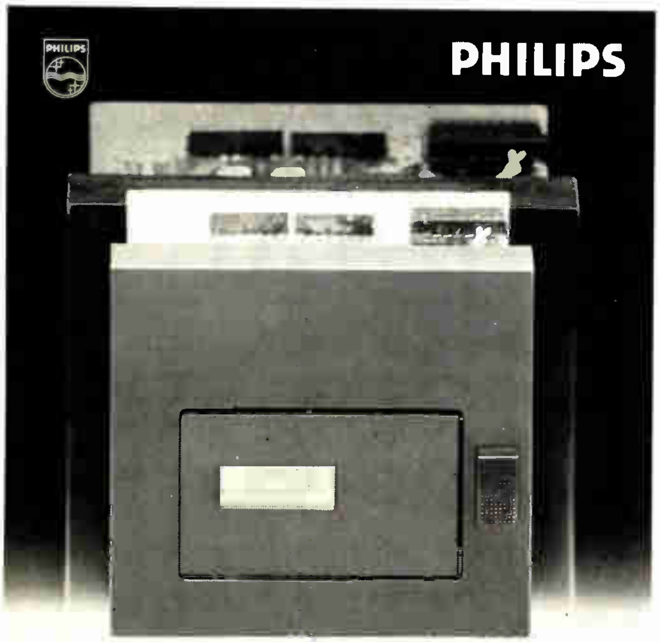

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How to draw diagrams faster

Graphics package has repertoire of more than 50 one-keystroke symbols

Having first created PC50, an interactive software package for the low-cost computer-aided design of printed-circuit-board layouts [*Electronics*, July 7, 1977, p. 127], Second Source Industries now adds the SC50 package for drawing schematic diagrams.

The package, designed for use with a Tektronix 4051 graphics system and a 4662 X-Y plotter, offers the user more than 50 IEEE/ANSI symbols, each at the touch of a single key. Positioning each symbol is simply a matter of manipulating the model 2005 joystick cursor control and hitting the required key.

A library of frequently used subcircuits, such as standard operational amplifier configurations, can be created by first drawing the subcircuits and then placing them in cartridge or disk memory. Once such a library is created, the user can greatly expedite diagram generation, as he will be able to manipulate and display whole segments (called objects) rather than discrete symbols. A step-and-repeat feature allows the designer to duplicate objects automatically, as may be necessary in a memory schematic diagram with its many identical cells.

A complete and corrected diagram is transferred from display screen to paper by the X-Y plotter when it is given a print command. The diagram can also be stored on tape or disk for later revision, if necessary.

Besides aiding in the creation of the drawing itself, the SC50 automatically provides a parts list from the reference designators placed on the diagram. These lists can be stored by part number, component value, vendor number, or other references.

Michael Smith, Second Source's general manager estimates that a user could complete schematic diagrams up to 10 times faster with the SC50 than by conventional manual methods. According to Smith, the user is free to change drawing scales and to use the system's zoom capability for easier drawing of dense circuit areas. He further points out that the system meets all pertinent military specifications for drawing schematic diagrams.

The entire system, which includes the Tektronix 4051 and 4662, an add-in memory, the model 2005 joystick, the model 2903 EE drafting read-only-memory pack, and the SC50 software and user's manual sells for approximately $416,335. The SC50, joystick, ROM pack, and add-in memory, for those who already have the Tektronix equipment, are priced at $44,640.

Second Source Industries, 735 Addison St., Berkeley, Calif. 94710. Phone (415) 848-6600 [391]

Unit drills holes in glass and ceramics

The Accu-Drill 3300 kit is a drilling system that includes all the equipment and materials (except diamond drills) needed to drill holes with diameters from 5 to 113 mils in fired ceramics and glass. The principal application of the kit is expected to be in hybrid-circuit development, where engineers want to avoid waiting for their ceramics suppliers to provide them with the custom tooling needed to make the hole patterns in the unfired material.

The kit consists of a high-speed drill press capable of speeds up to 30,000 rpm; a soft, machinable ceramic slab, which is used as a temporary backing plate during drilling; and a supply of Crystalbond 509 adhesive for bonding the workpiece to the soft ceramic plate. After drilling, the adhesive is easily removed with acetone.

The kit is priced at $495, and a model with an X-Y micrometer stage accurate to within 1 mil goes for $875. The diamond drills sell for an average of $42 each, with the exact price varying with drill size. Deliveries can now be made from stock.

Aremco Products Inc., P. O. Box 429, Ossining, N. Y. 10562. Phone Herbert Schwartz at (914) 762-0685 [395]

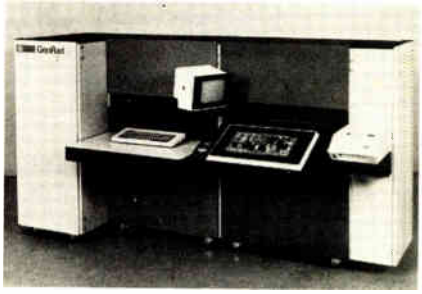
Automatic system tests emitter-coupled logic

Designed specifically to test ECL 100 K devices, the S-3280 automated semiconductor test system can also handle other fast current-mode-logic circuits. The unit's pin drivers can swing 2 v in less than a nanosecond when working into a 50-Ω load. On the measurement side, the S-3280 uses a sampling head per pin up to a limit of 64 channels. Sampling head rise time is 75 ps.

Tektronix Inc., P. O. Box 500, Beaverton, Ore. 97077. Phone Mike Bonham at (503) 644-0161, Ext. 1201 [394]

In-circuit tester generates most of its own programs

Given a simple tabular description of the topology of a circuit board plus a listing of component values and tolerances, the software in the GR 2270 can generate from 75% to 80% of the test program needed to perform a complete in-circuit test of the board. The 2270 uses an LSI-11 microcomputer to set up guarded component measurements automati-



cally and to generate printed repair messages in simple English. Shorts and opens, as well as missing, wrong, faulty, reversed, and incorrectly seated parts, are all identified in one pass and described in the repair message.

Key to the operation of the 2270 is its vacuum-operated bed-of-nails fixture, which can handle up to 1,024 pins. Users may select any number of pins, from zero to the maximum, provided the selection is in multiples of 16. The basic system sells for $65,000.

GenRad Inc., 300 Baker Ave., Concord, Mass. 01742. Phone (617) 369-4400 [393]

24-conductor cable made for IEEE-488

A Underwriters Laboratories–recognized 24-conductor cable with molded-on, stackable, male-female connectors is designed to be used in instrument bus systems that meet IEEE standard 488-1975. The cable has a delay time of 5.2 ns per meter and a capacitance of about 115 pF per meter. It is available in 1-, 2-, 4-, 8-, and 16-m lengths and in bulk (without connectors). Delivery of the cable, in any of these lengths, is from stock.

Belden Corp., 2000 S. Batavia Ave., Geneva, Ill. 60134 [396]

Die positioner–sorter operates automatically

The model 123 computerized die-positioning and -sorting machine moves semiconductor dice under a microscope following a programmed inspection pattern. The number of rows, columns, and inspection points within the die, the center spacing, and the dwell time at each point all are keyboard programmable. The machine includes a picker with memory that removes dice rejected by the operator, at a preselected point clear of the microscope. It sells for $6,950, plus optics.

Mechanization Associates, 153 E. Evelyn Ave., Mountain View, Calif. 94041 [397]

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