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MARCH 2, 1978

**THE NEW DIMENSION FOR MINICOMPUTERS: 32 BITS/73**

V-channel FETs vying with bipolars for rf power applications/ 105

DIP delay lines entice logic designers/ 114

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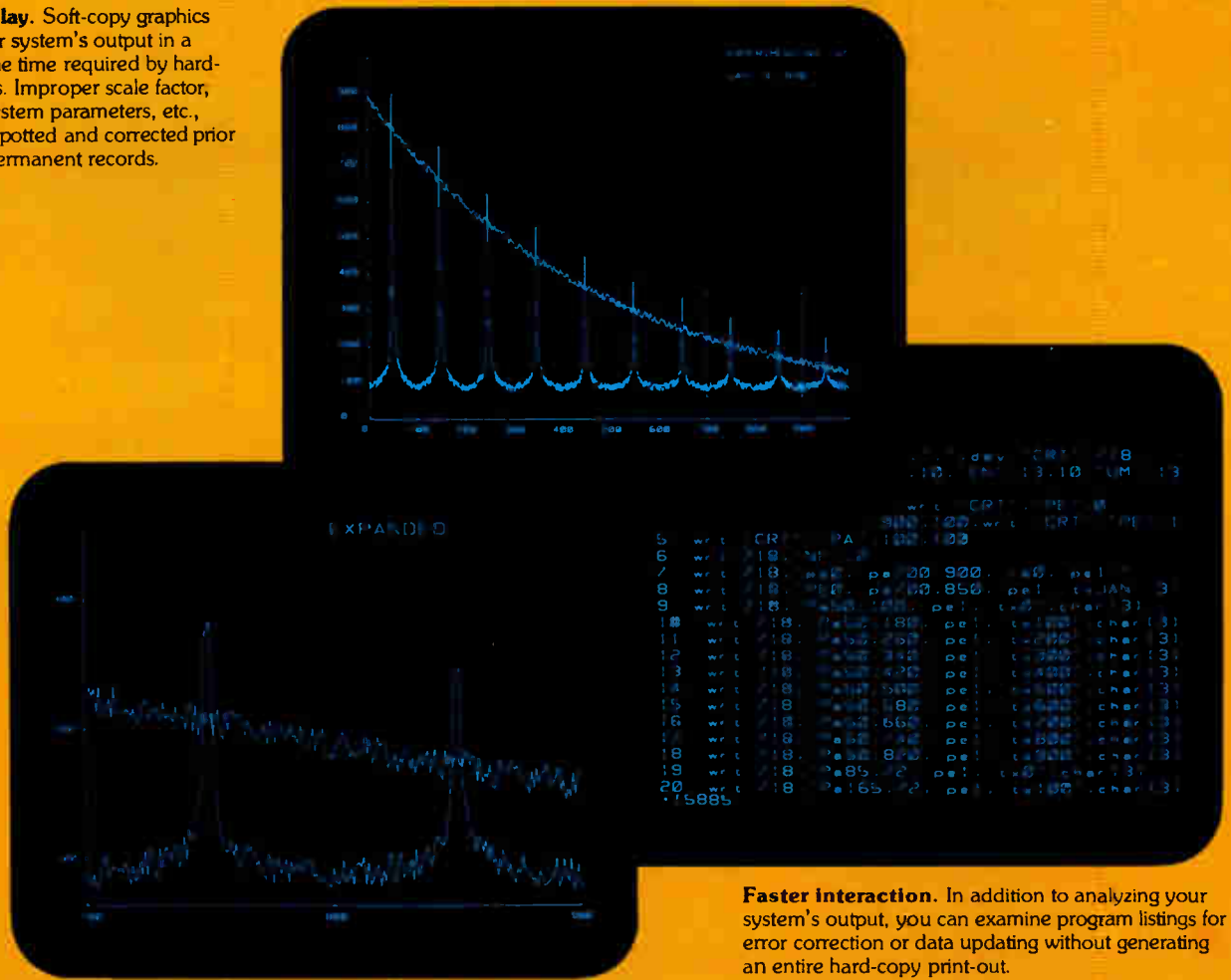
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# HP's new Graphics Translator brings the speed of soft-copy graphics to **HP-IB** systems.

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**Faster interaction.** In addition to analyzing your system's output, you can examine program listings for error correction or data updating without generating an entire hard-copy print-out.

**Faster decisions.** You can view a normal display plus an expanded display in much less time than it usually takes for one hard-copy output. That means faster analysis, quicker decisions and less paper usage.



With HP's new 1350A Graphics Translator and one or more of HP's electrostatic CRT displays, you can more efficiently display system data . . . evaluate results . . . and interact to make changes.

Soft-copy graphics can save you reams of paper plus the time required to generate it. And the 1350A gives you added flexibility. You can selectively erase data, blank portions of a display and even repetitively flash specific graphic areas or alphanumeric characters on the screen to draw attention.

Programming is easy with controllers such as HP's 9825A. The 1350A can drive at least ten electrostatic displays and

provides four different presentations on multiple displays simultaneously.

Look into HP's new 1350A, priced at \$3,450\*\*, for analytical instrumentation or engineering analysis systems. It's also ideal for HP's Data Acquisition and Network Analysis Systems; in fact, wherever you need high-resolution graphics of HP-IB data. An optional RS-232 interface is available for use with other digital systems. Call your local HP field engineer for complete details.

\*HP's implementation of IEEE Standard 488-1975.

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Cover by Associate Art Director Charles D. Ciatto

### 16 or 32 bits: the choice for mini makers, 73

As 32-bit minicomputers make their way into the product arena, some manufacturers are holding at the 16-bit level. At issue: is the bigger word length necessary for better performance?

### Vertical geometry hikes FET power, 105

Power applications at radio frequencies are now open to field-effect transistors, thanks to a V-channel configuration. The nonplanar arrangement of the electrodes avoids parasitic capacitance in these applications.

### Self-diagnosis cuts repair time, 121

In digital control systems for process applications, the microprocessor controller can also be programmed to troubleshoot circuit and system faults, for a repair time of a few minutes. Another in the Microprocessors in Action series.

### And in the next issue . . .

Expanding an oscilloscope into a general-purpose tester . . . a microprocessor development system expands . . . microprogramming a minicomputer for fast signal processing.

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An important aspect of reliability, at least in an industrial context, is ease of maintenance. For Ralph G. Foose, manager of advanced systems for Industrial Nucleonics Corp. in Columbus, Ohio, who is the author of the latest article in our Microprocessors in Action series (p. 121), reliability was something he learned almost from childhood on.

"My father was director of quality assurance for NASA Kennedy Space Center," Foose reports, "and he pounded reliability into me."

So it was hardly surprising that Foose the younger built on Foose the elder's views when he became a designer of process-control equipment. To the industrial user, he figures, a system seems reliable if it can be kept running more or less continuously—infrequent but catastrophic failures are not what is wanted. So Foose programs his microprocessor-based systems with fault diagnostics that cut repair time to a matter of minutes.

"As energy conservation becomes vital, process control will be more important," he states. "It will be essential to have equipment that is reliable and easy to maintain, especially during periods when power consumption is reduced by fuel

shortages. My own plant has been cut back due to a coal shortage."

Once again *Electronics* has won a Jesse H. Neal Award for Editorial Achievement from the American Business Press, an association of magazine publishers. We're particularly proud because it recognizes the best staff-written article in our publication bracket.

This year's award went to Larry Altman, solid state editor, and Charlie Cohen, Tokyo bureau chief, for an article developed with editor-in-chief Kemp Anderson on "The gathering wave of Japanese technology" [*Electronics*, June 9, 1977, p. 99]

Also honored were copy editors Margaret Eastman and Ben Mason and art director Fred Sklenar, the key support people needed in any article. As chief editor Anderson says, there's considerable satisfaction in having the writers, the copy desk, and the art department recognized as a team for this kind of achievement.



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We have a challenging position available for an electronics engineer who can combine aggressive curiosity, writing ability, and technical knowhow into a rewarding career as an editor on *Electronics* magazine in New York. Candidates should have a BSEE and preferably a year or two's experience in digital design and microprocessor applications. We offer excellent salary and fringe benefits. Send your résumé to the Executive Editor, *Electronics*, 1221 Avenue of the Americas, New York, N. Y. 10020.

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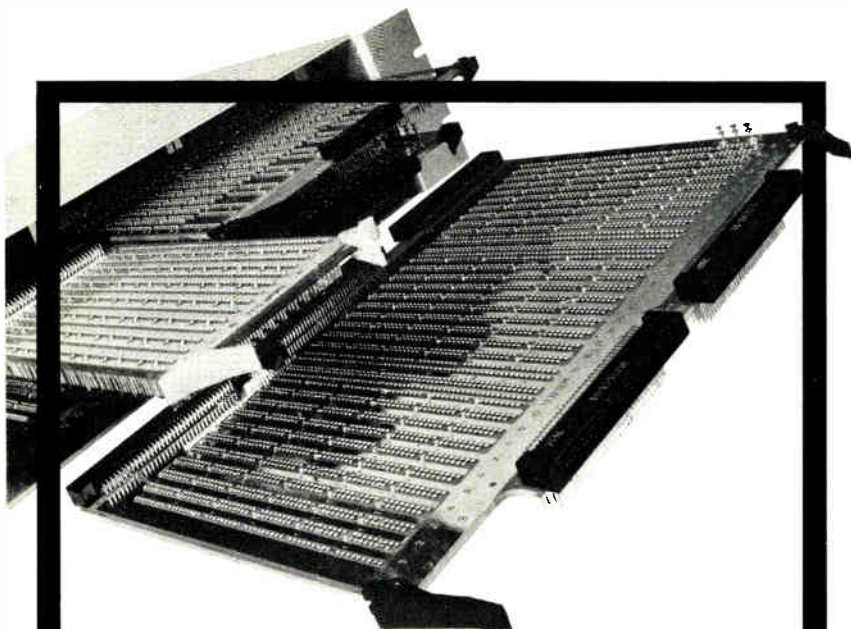
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## Readers' comments

### Turned off

**To the Editor:** I agree there is horrendous apathy among members of the Institute of Electrical and Electronics Engineers [Editorial, Nov. 24, p. 12]. From personal experience, I can see why.

Fees went up and up, and the only real benefit of membership was to be asked to buy reprints and listen to talks. Since I joined in 1958, the help the institute has provided in finding jobs has gone down, not up (fortunately, I've never needed help).

For years, I wrote notes. For years, I voted in every election. Finally, in disgust, I quit—and told them why. Never once did I get a reply. Never once did the institute try to answer my questions or get me back as a member.

Peter Lefferts  
San Martin, Calif.

### Simpler, cheaper

**To the Editor:** Messrs. Gilmore and Snipes' solution to driving a trailer's lights from a new car's separate turn and brake signals [Designer's Casebook, Aug. 18, p. 116] seems involved and expensive. The same results can be achieved with only four diodes and much less wiring.

Connecting the car's left-turn and brake signal lines to the trailer's left signal light and its right-turn and brake signal lines to the trailer's right signal light, each through a forward-biased diode, does the trick.

Dennis Snyder  
Melbourne, Fla.

### Already here

**To the Editor:** Your Electronics Newsletter of Dec. 22 [p. 25] did not mention that a double-density metal-oxide-semiconductor floppy chip is now available.

Western Digital has completed all orders for samples and is now in high-volume production. We left the encoding-decoding portion outside the chip, enabling it to perform all types of double-density, as well as single-density, encoding.

George Gregoire  
Western Digital Corp.  
Newport Beach, Calif.



# Fast Relief

## for digital troubleshooting headaches

Banish those troubleshooting headaches with signature analysis, the new technique from Hewlett-Packard that lets you troubleshoot microprocessor products right down to the faulty component. In production. In the field.

With signature analysis, that enormous floating inventory of expensive boards and modules moving in and out of service can be cut dramatically.

Signature analysis is positive. There is no hit or miss about it. Conceivably you could even eliminate the need to partition your product for modular service.

### A simple concept.

The HP 5004A Signature Analyzer converts lengthy bit streams at any node in the circuit into short, four-digit, hexadecimal "signatures."

Just activate a digital exercise routine in the circuit under test and compare the bit stream signature at each data mode with the known good signatures previously written into your manual.

Digital signal tracing



becomes as simple as analog tracing used to be. But more accurate. So accurate that it catches almost every possible fault, including many that can be detected in no other way. It once again becomes realistic to think of field or production troubleshooting to the component level by technicians.

### Design it in or retrofit.

The savings in service costs and inventory are well worth the effort of designing with signature analysis in mind. In some cases, it could even pay you to "retrofit" by developing a signature manual for your existing equipment.

It's a fascinating—and very workable—concept. Amazingly the price of the HP 5004A Signature Analyzer that makes all this possible is a low \$990\*.

To help you take advantage of this breakthrough we've prepared Application Note 222 — "A Designer's Guide to Signature Analysis." It's yours for the asking. Just contact your nearest HP field sales office or write.

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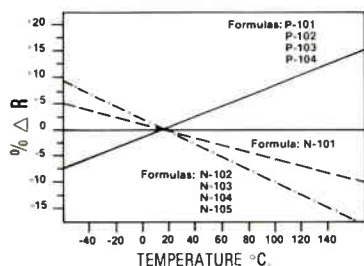
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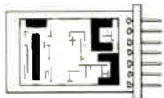
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## News update

■ Hughes Aircraft Co. of Canoga Park, Calif., says it has demonstrated the feasibility of developing an Advanced Medium Range Air-to-Air Missile, or Amraam, that packs higher performance into a smaller airframe. To be compatible with the Air Force's F-15 and F-16 fighters, as well as the Navy's F-14 and F-18, Amraam would provide a "launch and leave" capability—the fighter need not guide the missile to the target—and the option of firing at several targets simultaneously.

Hughes is one of several contractors competing to build the follow-on missile to Raytheon Co.'s AIM-7F Sparrow [*Electronics*, Jan. 20, 1977, p. 25]. "We have demonstrated the viability of building a follow-on to Sparrow with approximately half the size and much greater performance capability," says Vitaly Bloom, Hughes program manager. Hughes' design is completely solid state and digitally controlled. "By taking advantage of the latest digital technology and micro-miniaturization of the electronics," he continues, "the design packages a very complex missile into a small airframe and achieves greater reliability and availability than that of any currently operational air-to-air missile."

■ RCA Corp. has halted production of its Studio II monochrome programmable games, the type that attaches to a television receiver, while it reviews its position in the video game business. The move comes less than nine months after RCA began national distribution of Studio II [*Electronics*, May 26, 1977, p. 83] and, according to an RCA spokesman, "was the result of what was generally a disappointing Christmas season for programmable video games."

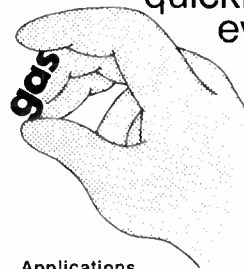
The Studio II, based on RCA's own CDP 1802 8-bit microprocessor, was produced at the firm's facilities in Swannanoa, N. C. "Cartridges for the games continue to be manufactured," the spokesman says, and "design and development work for future video game products is continuing at a reduced level."

**Bruce LeBoss**

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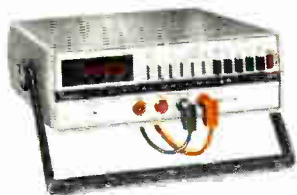
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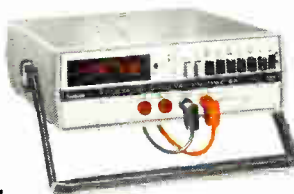
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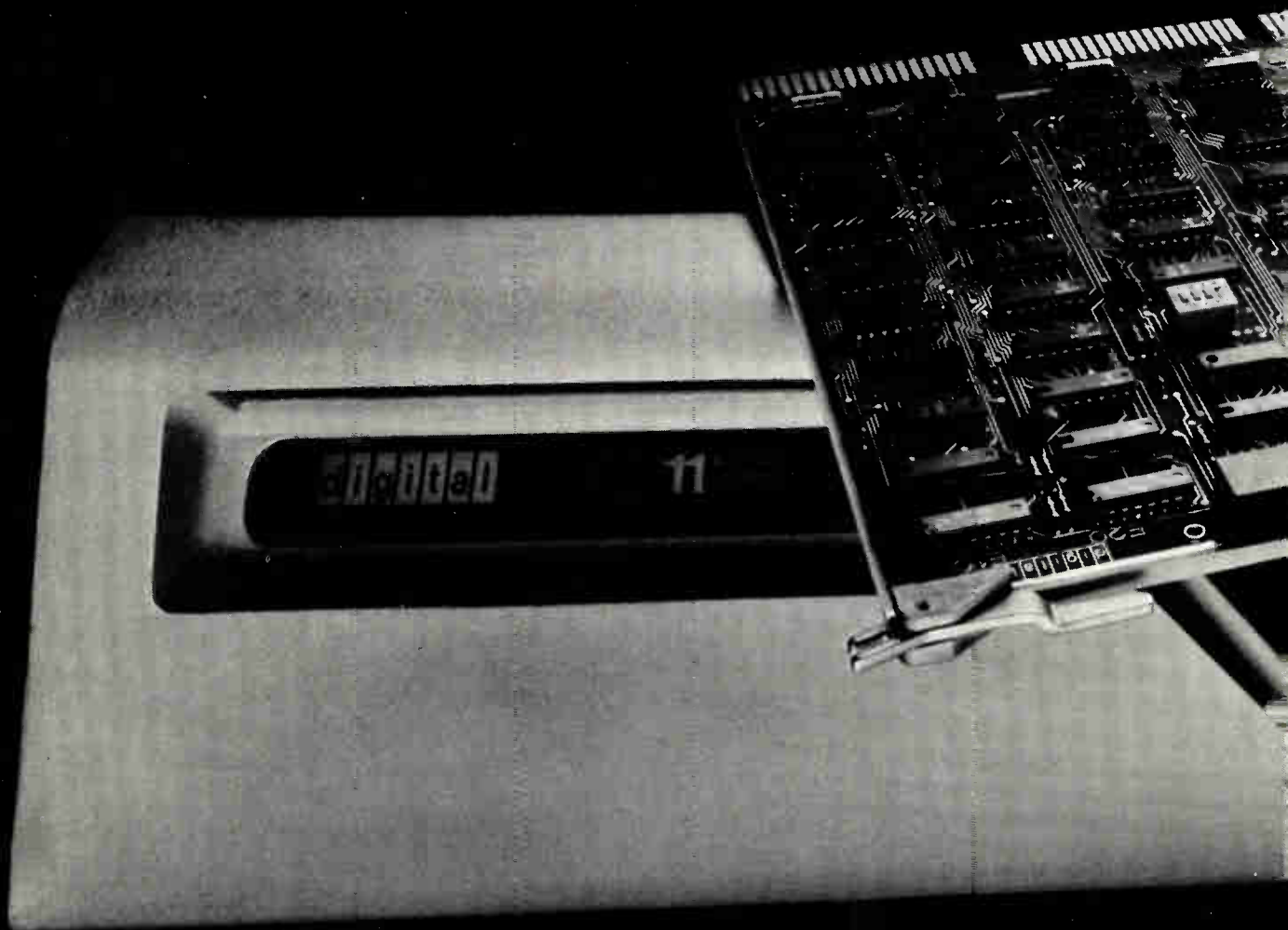
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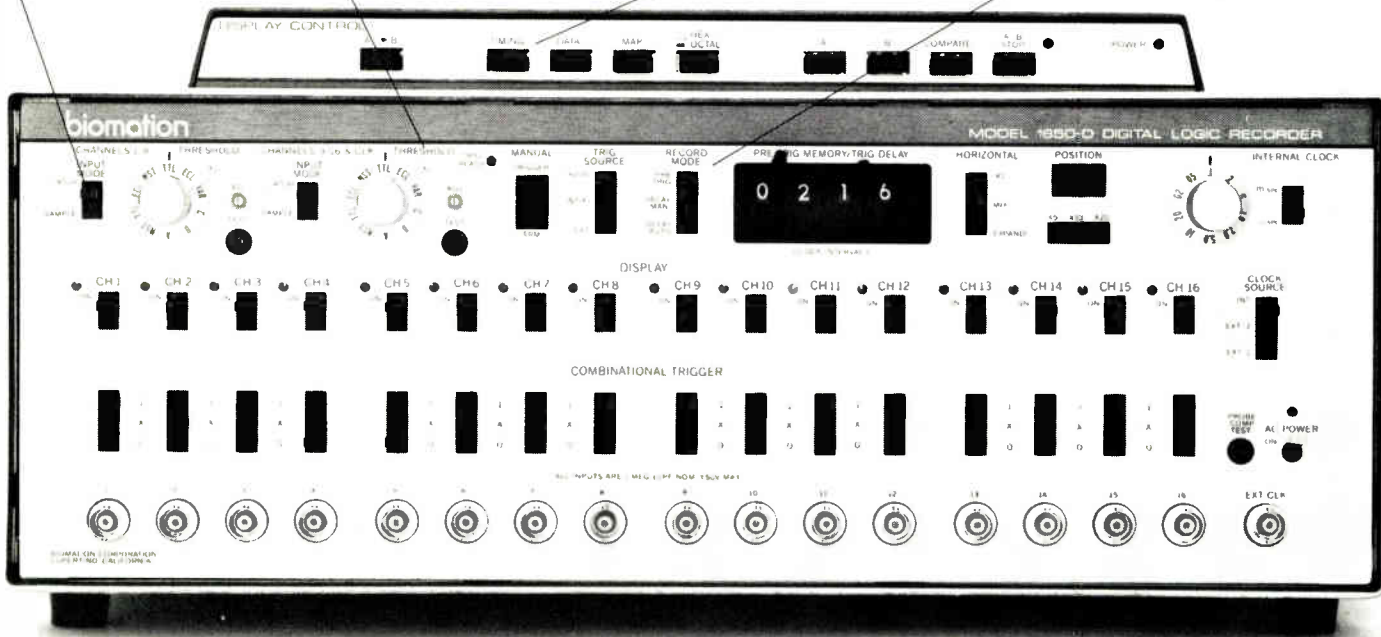
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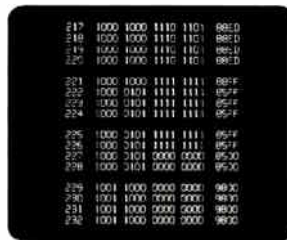
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**People**

GCA's E-beam lithography has Piwczyk at the helm

When Bernhard Piwczyk (pronounced piv-check) came to GCA Corp.'s division in Burlington, Mass., last December, he knew little about the company "except that they made very good equipment." Now, the 36-year-old Piwczyk hopes to use that reputation for quality semiconductor-processing gear to steer the division into the new world of electron-beam lithography.

As manager of the Advanced Lithography department, a newly created group, Piwczyk is charged with developing an electron-beam system that will write directly on semiconductor wafers and bringing it to market by 1981. He intends to skip the intermediate step of building a mask-projection system, the approach taken by the company Piwczyk just left—the Extrion division of Varian Associates Inc., Gloucester, Mass. Extrion is also at work on a direct-wafer-exposure system [*Electronics*, Feb. 2, p. 14] and will be on the market ahead of GCA.

But Piwczyk is not bothered about being late. "The market for direct writing on the wafer won't really develop before 1981 because optical systems with wafer steppers can meet the requirements for 2-micrometer line widths until then," he says. The GCA division introduced such an optical photorepeater for direct wafer exposure last year [*Electronics*, Aug. 4, 1977, p. 115]. "I have no doubt that some semiconductor manufacturers will be satisfied with resolutions of 2 to 3 micrometers for the next 10 years, so there won't be any widespread acceptance of electron-beam lithography overnight," Piwczyk continues.

**Eventual need.** But Piwczyk recognizes the eventual need for submicrometer resolutions, and his first task at GCA was to decide which approach to take. After looking at several, including the Bell Laboratories Ebes electron-beam exposure system adopted by Extrion and Etec Corp. of Hayward, Calif., he decided that the variable-aperture technique,



**On the way.** Direct writing on a wafer will not be in demand before 1981, Piwczyk says.

which does not use Bell's raster scan and is being espoused by IBM Corp., "can solve the submicrometer challenge elegantly."

Piwczyk plans to use only the more promising elements of his experience with the Ebes system at both Extrion for a year and, earlier, for eight years at Bell Northern Research Laboratories in Canada. "I've been able to set out unencumbered by a historical approach, and we're in a good position as an established equipment supplier to the semiconductor industry."

Beck designs games with development system

Once games started to be built around microprocessors, someone was bound to do it. And Stephen Beck, an electronic consultant in Berkeley, Calif., has done it—he has used a microprocessor development system to help design nonvideo games.

The result of his effort went on view last month at the Annual Toy Fair in New York [*Electronics*, Feb. 16, p. 51], in the Star Wars Electronic Laser Battle game from Kenner Products Co. in Cincinnati. He used his own Microgame devel-



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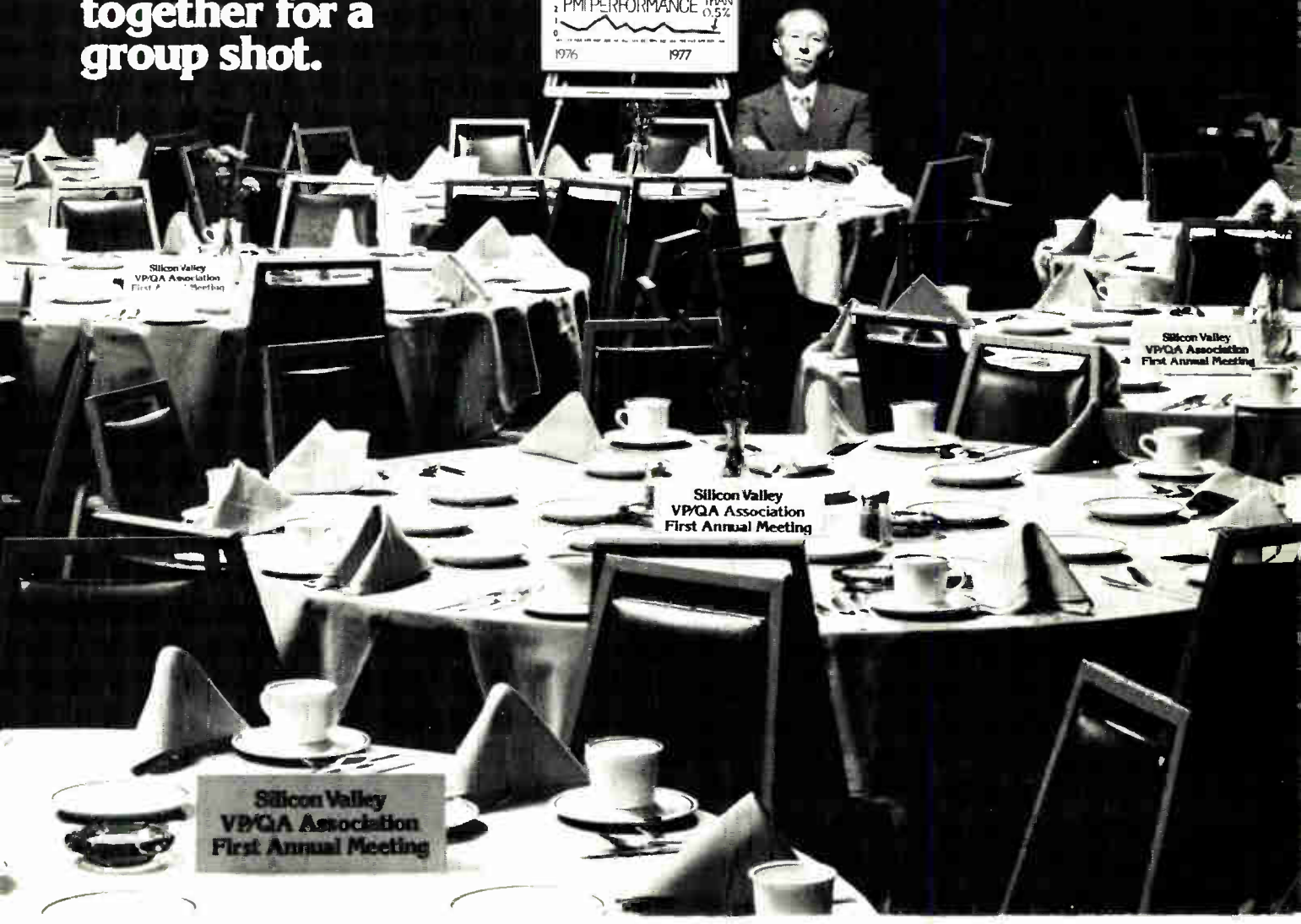
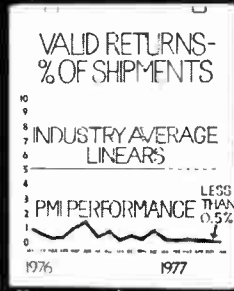
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**ITHACO**

opment system to speed up the game-designing process as soon as the project got past the breadboard stage.

**Fast turnaround.** "I developed my own Microgame assembly language with which I can implement an electronic game concept in a minimal amount of time and deliver workable prototypes to a manufacturer," says the 28-year-old electrical engineer. His system is essentially an adaptation of Intel Corp.'s well-known MDS 800 system.

Beck says it took him just three months to convert a breadboard design on two printed-circuit boards, which had already been made for Kenner, into one 40-pin TMS 1000 microprocessor and two 16-pin memory chips from Texas Instruments Inc. This period included all the work necessary for the delivery of working production prototypes. Ordinarily, a year would have been needed for this procedure, one that involves many hardware changes as the game is fine-tuned for the marketplace.

With this development system, "all changes are made in software before working parts are committed," he says, adding that he is able to update erasable programmable read-only memories in just one day. The key is his assembler, which can handle all the basic game functions, including switches, light-emitting-diode patterns, sound generation, and timing. According to Beck, the Microgame treats all functions as a class, "so you can weave together an operating program in a minimum time."

**Perception.** What comes next? More games and toys, of course, says Beck, who is now designing six other electronic marvels. "Imagination is the only limitation to what can be done," he maintains. "I don't see electronic toys or games as frivolous things. They challenge skills, create stimuli, test reactions, and make more fun."

Ultimately, he believes, that little microprocessor inside each of the new breed of games could "have a big effect on the way the public perceives computers in their lives."

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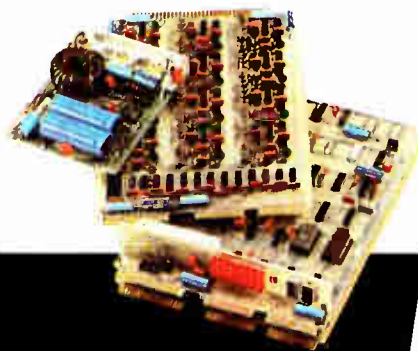
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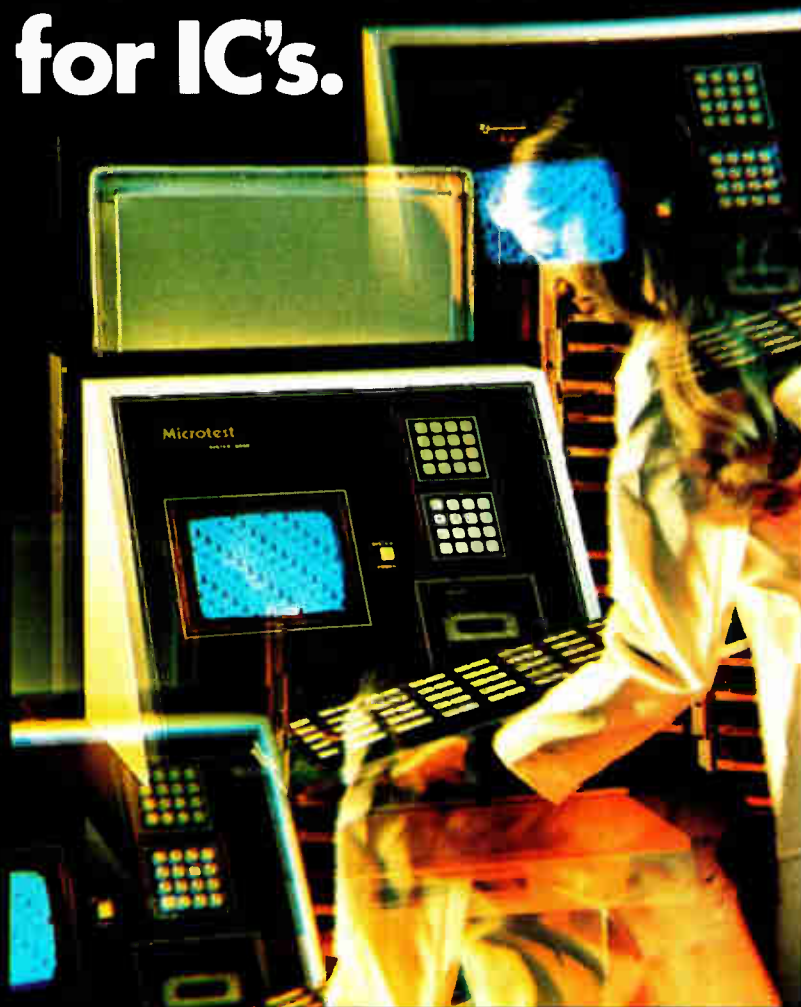
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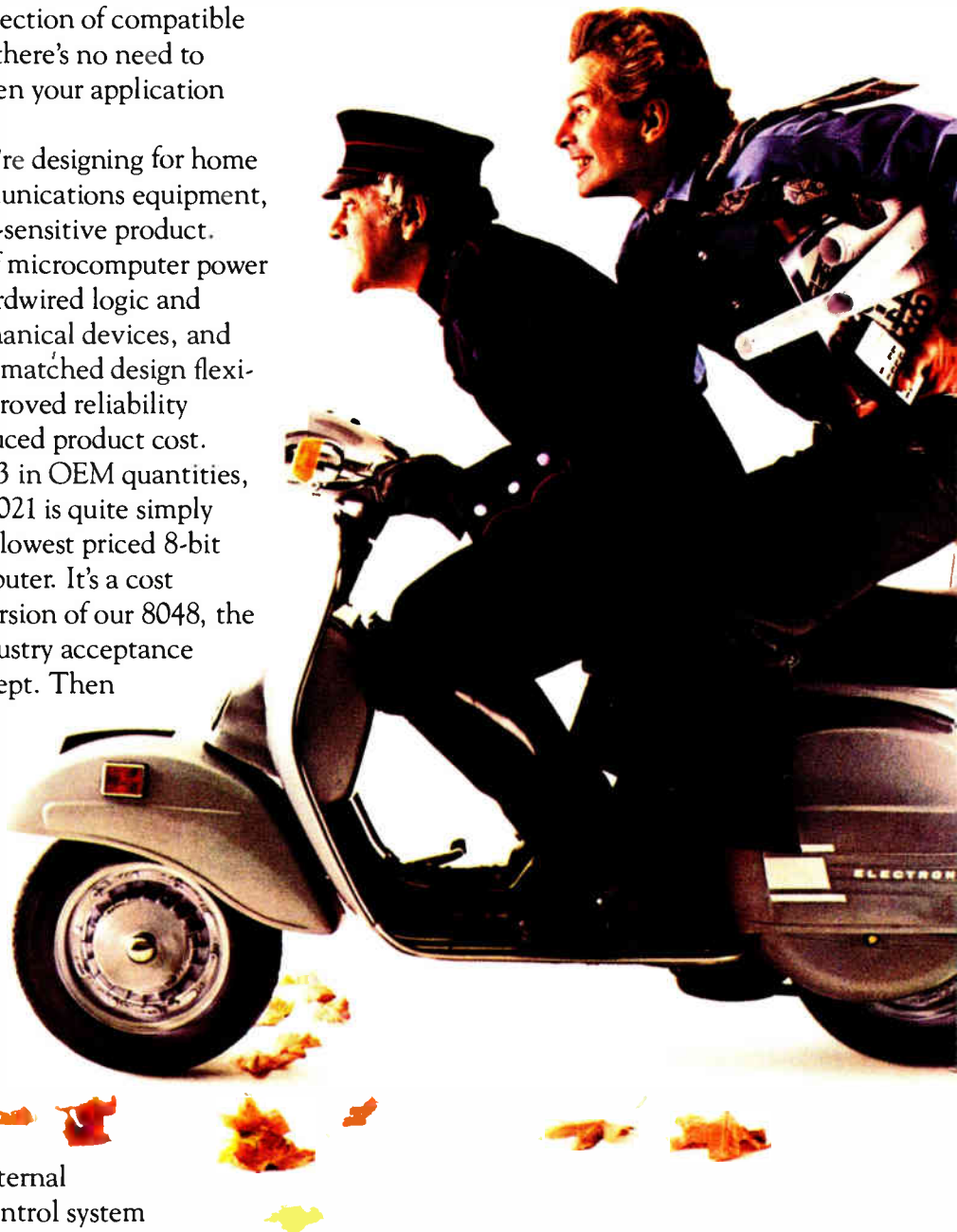
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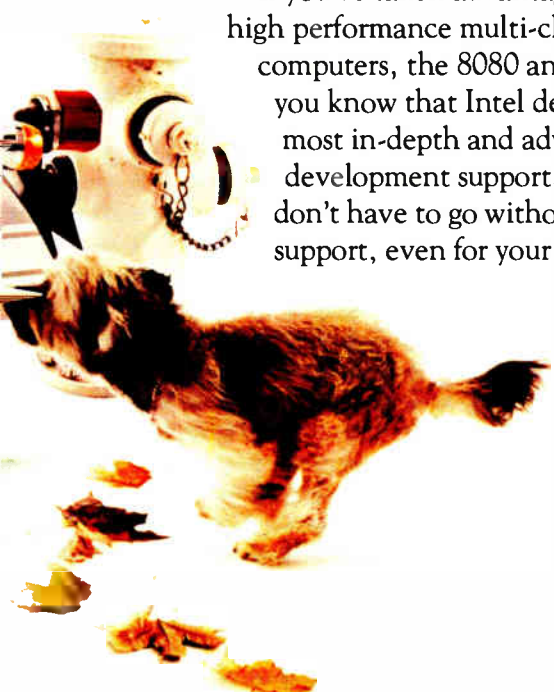


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8035*	(External)	64 Bytes	27	96	40 Pin
8049*	2K Bytes ROM	128 Bytes	27	96	40 Pin
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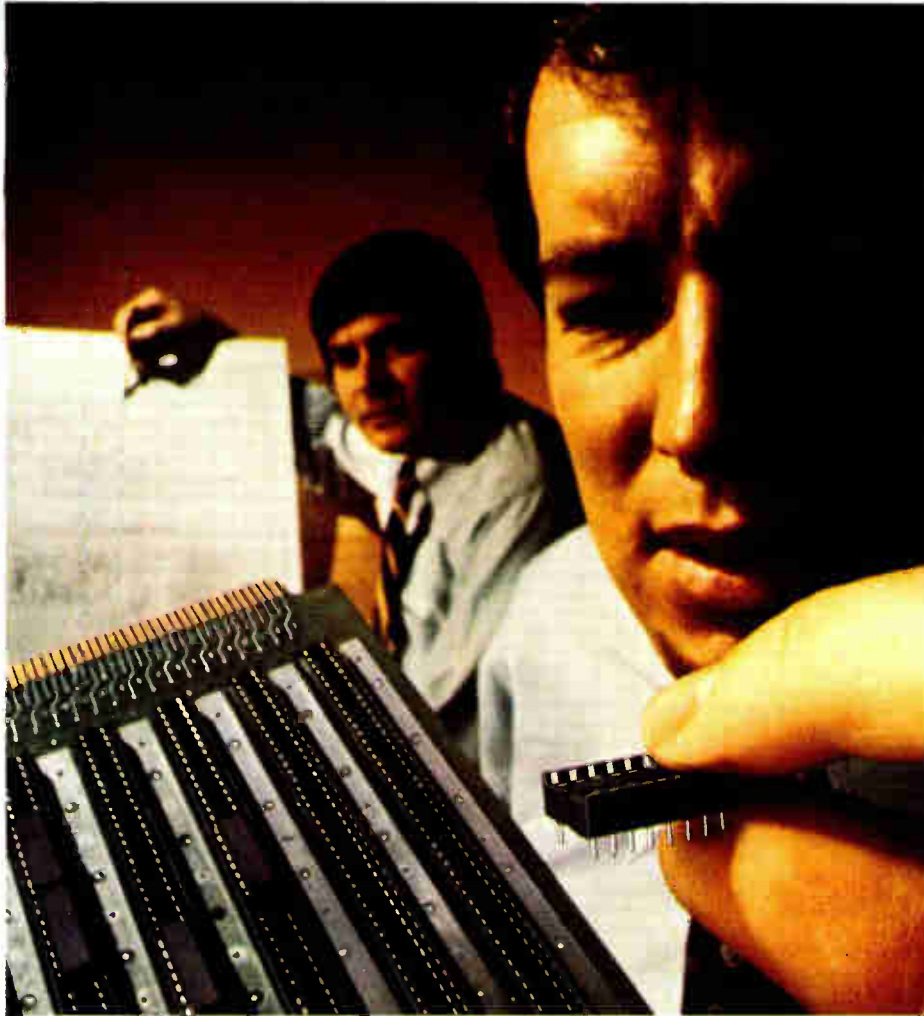
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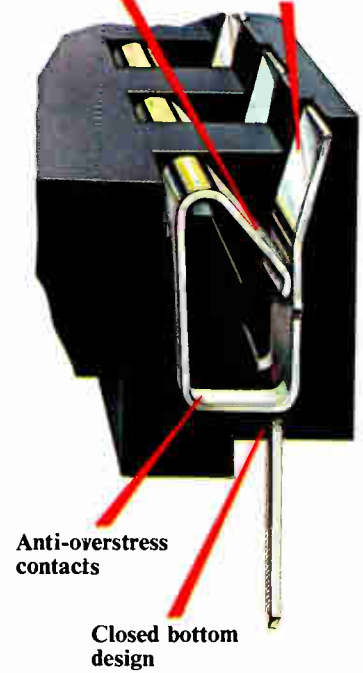
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## Britain's contrived controversy on MLS

The winding road to world acceptance of a single technological standard might be somewhat less torturous if such decisions were left to the international community of engineers. At least they can usually agree in the end on a given set of specifications. But often their conclusions, the result of years of research, development, and testing, are misinterpreted and then distorted by competing corporate managements obliged to turn a profit and politicians anxious to protect their nation's pride.

A classic example of the problem exists in Washington over the adoption of an international standard for a microwave landing system, now scheduled for a final vote in April at the International Civil Aviation Organization meeting in Montreal. It seemed a foregone conclusion that the organization would adopt the time-reference scanning-beam MLS developed and competitively tested in a program that began in 1971 and last year was recommended by its All-Weather Operations Panel for adoption. That vote was taken after a thorough assessment of all proposals, including the doppler MLS proposed by the British Civil Aviation Authority, a non-government body, and developed by the Plessey Corp. with the assistance of American subcontractors.

But now everything seems to be changing because of what Federal Aviation Administrator Langhorne Bond charges is a "vicious campaign" by Plessey lobbyist Michael Lehrman "using the press and other news media to deliberately mislead and confuse the world aviation community" about the American MLS program. Bond demonstrated uncharacteristic but justifiable anger in assailing the British efforts during MLS hearings earlier this month before the House Subcommittee on Government Activities

and Transportation [*Electronics*, Jan. 19, p. 57]. He took care to note that Plessey lobbyist Lehrman, when registering as an agent for a foreign interest, specified that his single goal was "to reverse the U. S. Government position proposing time-reference scanning-beam technology for the ICAO MLS standard." Charging Lehrman with "distortions of the truth," Bond labelled the British effort "a last-ditch stand in attempting to overturn, in favor of doppler MLS, the results of the long and arduous ICAO process."

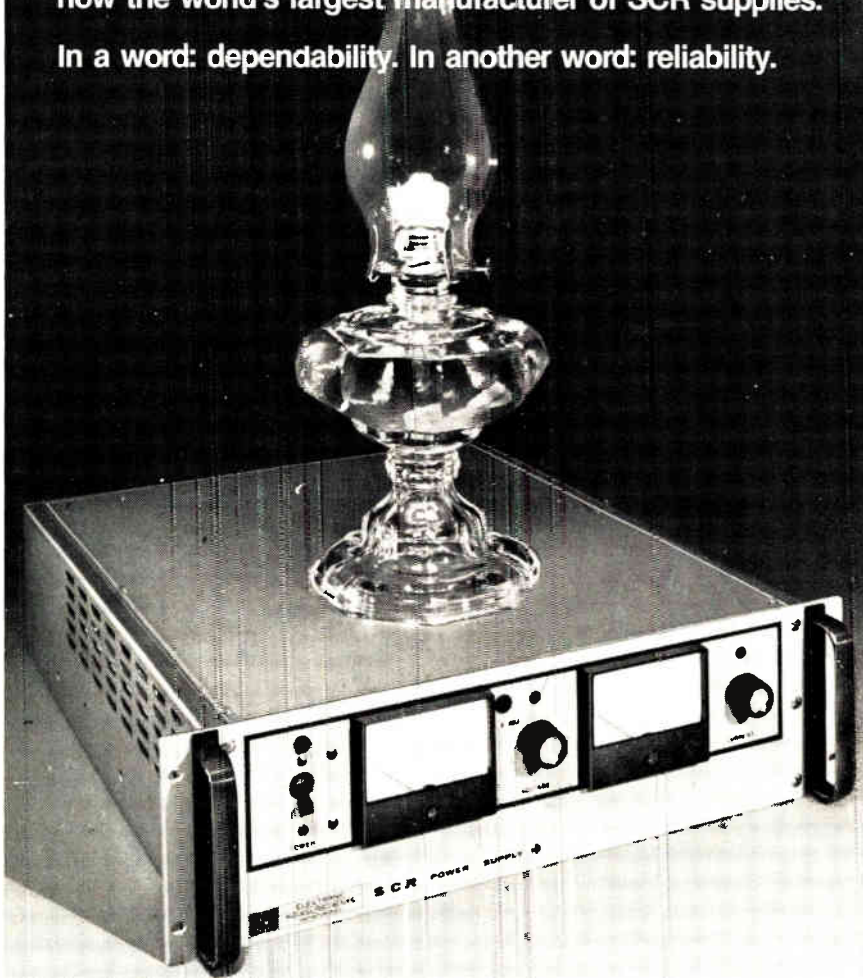
The Federal Aviation Administration's effort on MLS over the years has been an open process. It spent \$40 million, evenly split, on developing and evaluating both the scanning-beam and the doppler technique before pushing ahead with the former and spending an additional \$80 million on its development and testing, compared to only \$9 million by the British. The agency has developed a whole family of preproduction time-reference scanning beam models, while Britain has but one custom-built doppler MLS, Bond points out. Indeed, the agency turned over much of its doppler MLS hardware to Britain for its program.

At worst lobbyist Lehrman's campaign may produce a postponement of ICAO's April adoption of its scanning-beam MLS as the next world standard. But, if the organization sticks to the extensive assessments and recommendation of its multinational All-Weather Operations Panel, it must stay with its original choice. Even the Soviet Union has come out in favor of the American approach. All Britain will have done is to slow down the process of international standardization for its own interests, encouraging the continued proliferation of expensive Towers of Babel to confound world aviation.

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## Meetings

**Industrial Applications of Microprocessors, IEEE, Sheraton Hotel, Philadelphia, March 21-23.**

**Workshop on Moisture Measurement Technology for Hermetic Semiconductor Devices, Defense Advanced Research Projects Agency and National Bureau of Standards, Gaithersburg, Md., March 22-23.**

**28th Vehicular Technology Conference, IEEE, Regency Hotel, Denver, Colo., March 22-24.**

**AAMI Annual Meeting & Exhibit Program, Association for the Advancement of Medical Instrumentation (Arlington, Va.), Washington Hilton Hotel, Washington, D. C., March 29-April 1.**

**Metric Planning Forum, American National Metric Council (Washington, D. C.), Atlanta Hyatt Regency Hotel, Atlanta, April 2-5.**

**Symposium on Automatic Imagery Pattern Recognition, National Bureau of Standards and EIA, NBS, Gaithersburg, Md., April 3-4.**

**Industry/Joint Services Automatic Test Equipment Conference and Workshop, EIA, American Electronics Association (formerly WEMA), et al., Town and Country Hotel, San Diego, Calif., April 3-7.**

**21<sup>ème</sup> Salon International des Composants Electroniques, Société pour la Diffusion des Sciences et des Arts (Paris, France), Paris, April 3-8.**

**Communications '78 International Exposition, IEEE et al., National Exhibition Centre, Birmingham, England, April 4-7.**

**NAB Convention and International Exhibition, National Association of Broadcasters (Washington, D. C.), Las Vegas Convention Center, Las Vegas, Nev., April 9-12.**

**Seminar on New Components for Optical Communications, IEEE, Stevens Institute of Technology, Hoboken, N. J., April 10.**

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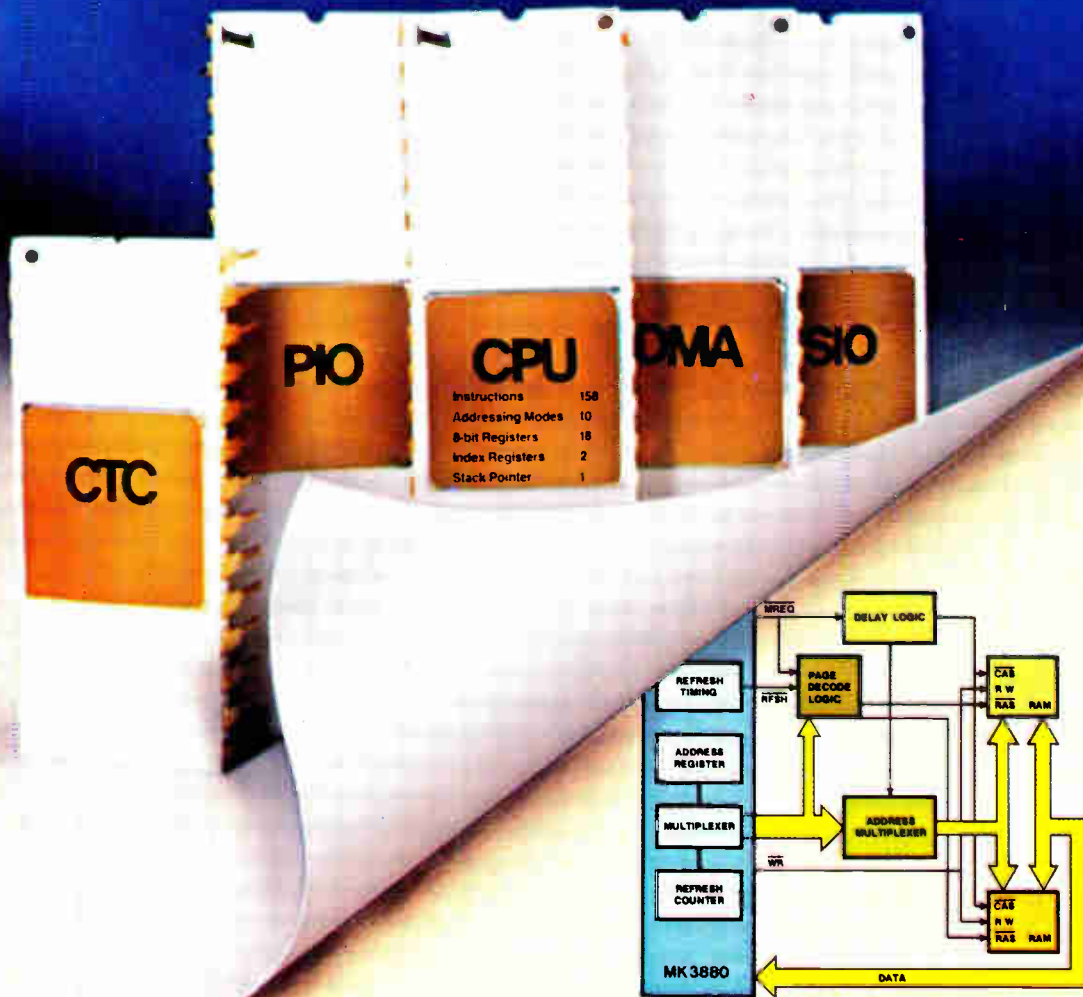
Powerful features make Mostek's Z80 the best 8-bit microcomputer available. The Z80 CPU interfaces directly with standard dynamic memories and provides both refresh and timing signals. The results: easier system design with fewer components. The Z80 is software compatible with the 8080A yet has 80 additional instructions. Other features are: powerful I/O block transfer capability; extremely fast interrupt response; and a memory block transfer ability that moves up to 65K bytes with a single instruction.

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3882 Counter Timer Circuit; MK 3883 Direct Memory Access Controller; and the MK 3884 Serial Input/Output Controller. The 3880, 3881 and 3882 are available now with the DMA and SIO to be sampled soon. All components operate on a single +5 Volt power supply.

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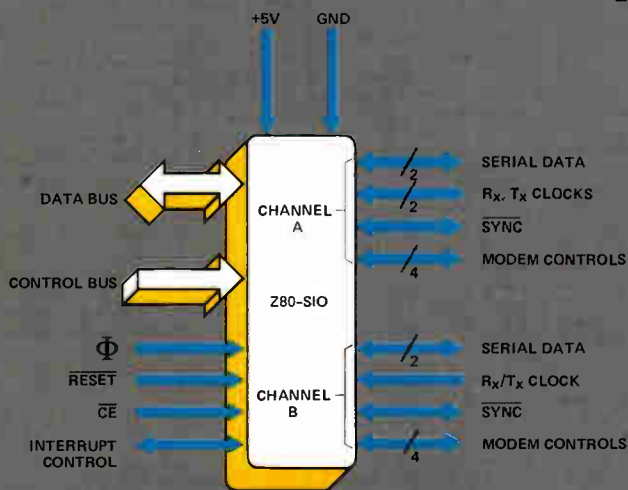
ter, Fluke Trendar Corp., 630 Clyde Ave. Mountain View, CA 94043. Europe: Fluke (Nederland) B.V., P.O. Box 5053, Tilburg, The Netherlands. Phone: (013) 673973. Telex: 52237.



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# Two Powerful Peripherals from Zilog:

## The Z80™ Serial Input/Output

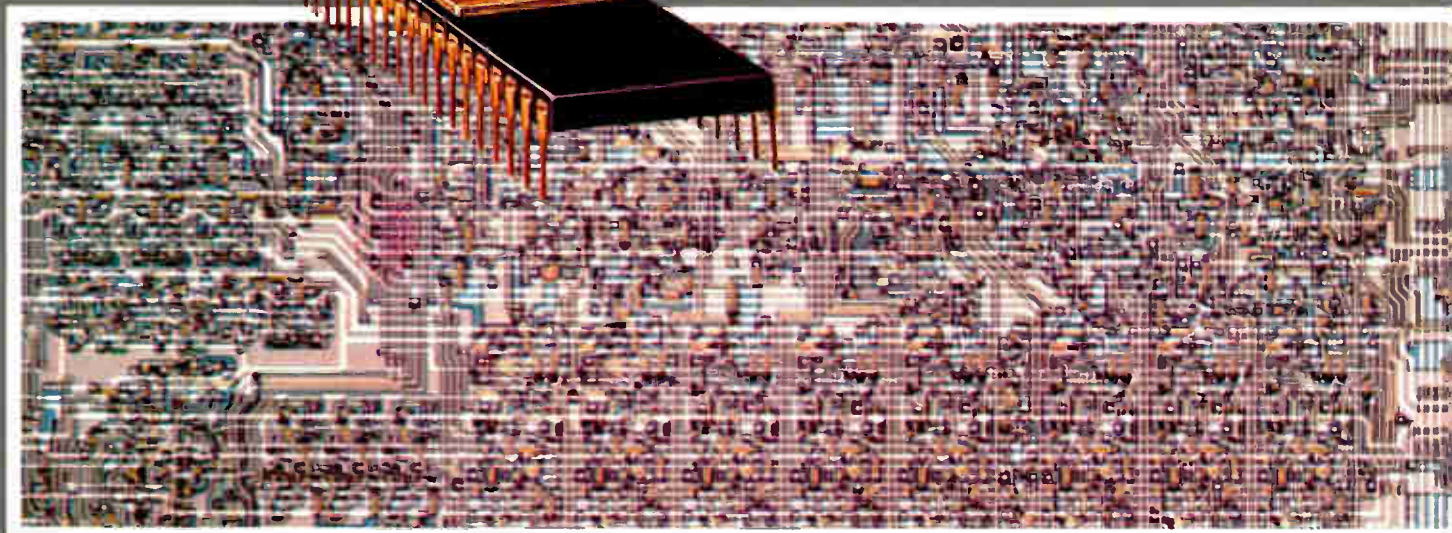


The Z80-SIO is the world's first dual-channel, multi-protocol serial communications interface circuit. It represents a significant technological advance in LSI microcomputer peripherals by supporting all common serial data communication techniques with a single, N-channel (+5V) 40 pin device. The Z80-SIO achieves unheard of levels of logic density and functional integration.

(Over 10,000 transistors on a 200 mil chip.)

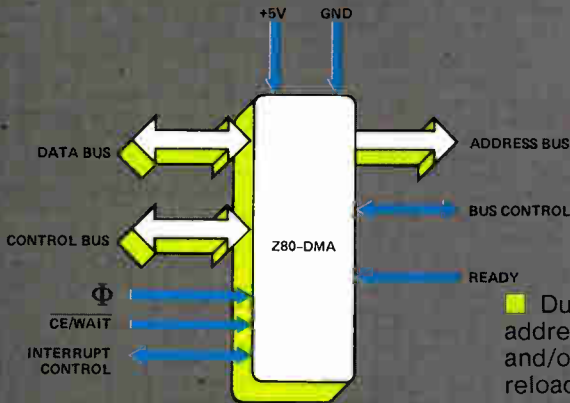
As with all Zilog Z80 peripheral components, the Z80-SIO supports the "Daisy-Chain" interrupt structure of the Z80-CPU for fast, powerful interrupt processing with no additional hardware overhead. The Z80-SIO can also be easily interfaced to other 8-bit and 16-bit microprocessors.

- Two independent, full-duplex channels with modem controls.
- Data Rates—0-550k bits/second (2.5 MHz Z80) • 0-880k bits/second (4.0 MHz Z80A)
- Asynchronous Modes • Programmable bits/character, stop bits • clock factor • Break detection/generation • Parity, overrun and framing error detection
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- SDLC/HDLC Modes • Comprehensive frame-level control • -field residue handling • CRC generation/checking





# The Z80™ Direct Memory Access

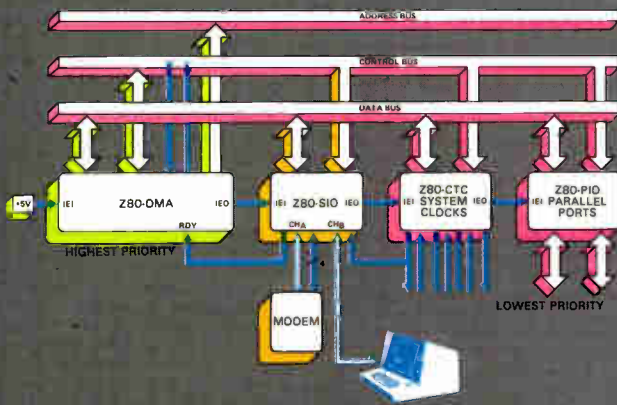


The Z80-DMA is designed to optimize the efficiency and speed of data transfers within microcomputer systems. Its unique, dual address operation provides the systems designer with features and flexibility far beyond that of any other type of DMA controller. The Z80-

DMA functions as a high-speed transfer processor, assuming complete system bus control in its "master" role. The Z80-DMA can be easily cascaded by on-chip features, operates off a single +5V supply and is packaged in a 40 pin DIP.

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- Programmable operating modes, starting addresses, block lengths, port timings, increment/decrement/fixed
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- Automatic parameter reload
- Complete status read operation
- No additional hardware overhead

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This diagram illustrates the power, functional integration and ease of interface of Zilog's Z80 peripheral component family that dramatically reduces the number of chips you need. It represents the peripherals section of a high speed communications processor.

The system bus is common throughout with memory, Z80-CPU and peripherals sharing as a common resource. The interface between all peripherals and the bus is direct with no additional logic required.

Interface to "outside" communications is through a MODEM device to the Z80-SIO. All necessary Modem controls are provided directly by the Z80-SIO and data is transferred under Z80-DMA control for message-structured buffering. The second channel of the Z80-SIO is devoted to an asynchronous CRT terminal.

Note the baud rate generation for the terminal interface comes directly from the Z80-CTC and is completely software programmable. Other system clocks are generated by the remaining channels of the Z80-CTC. Parallel interfaces to other input sources or

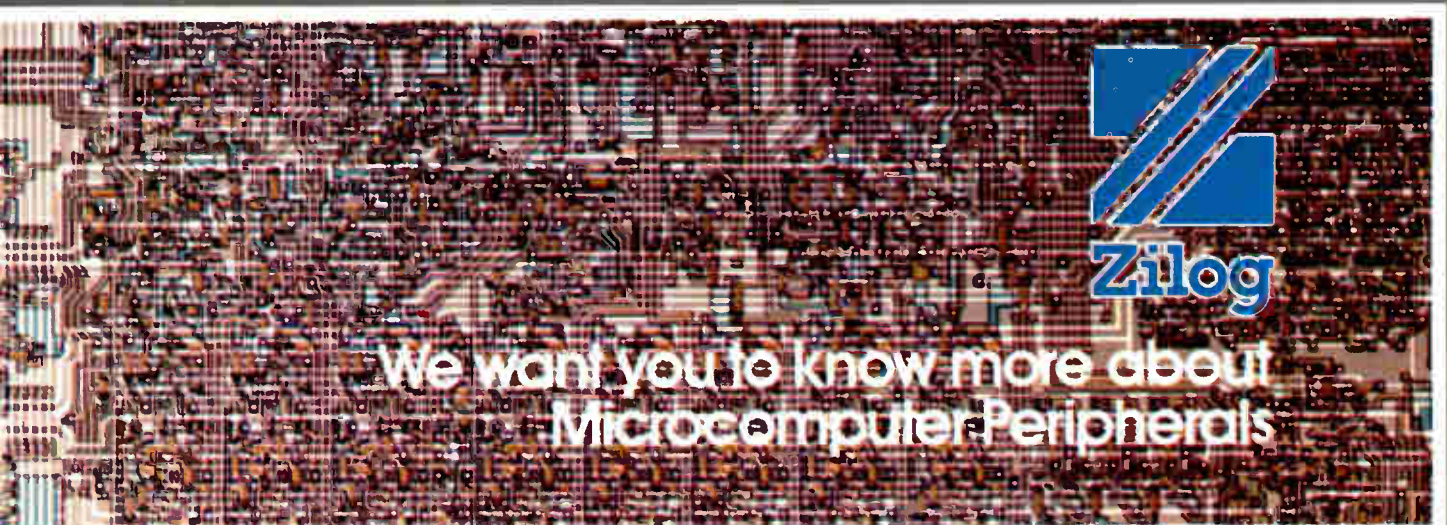
indicators are interfaced via the Z80-PIO.

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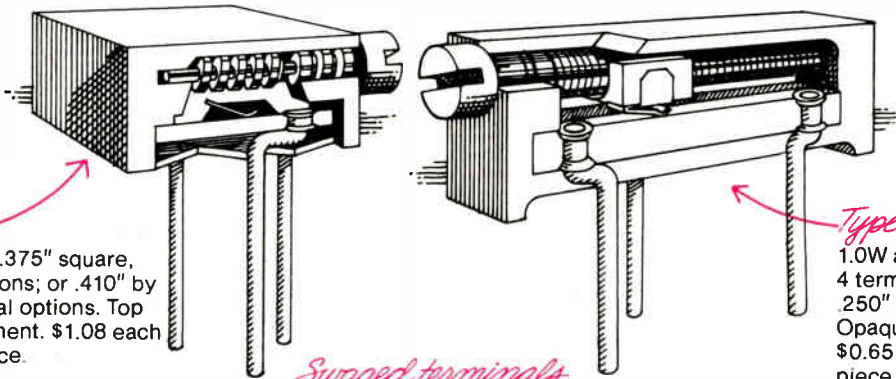
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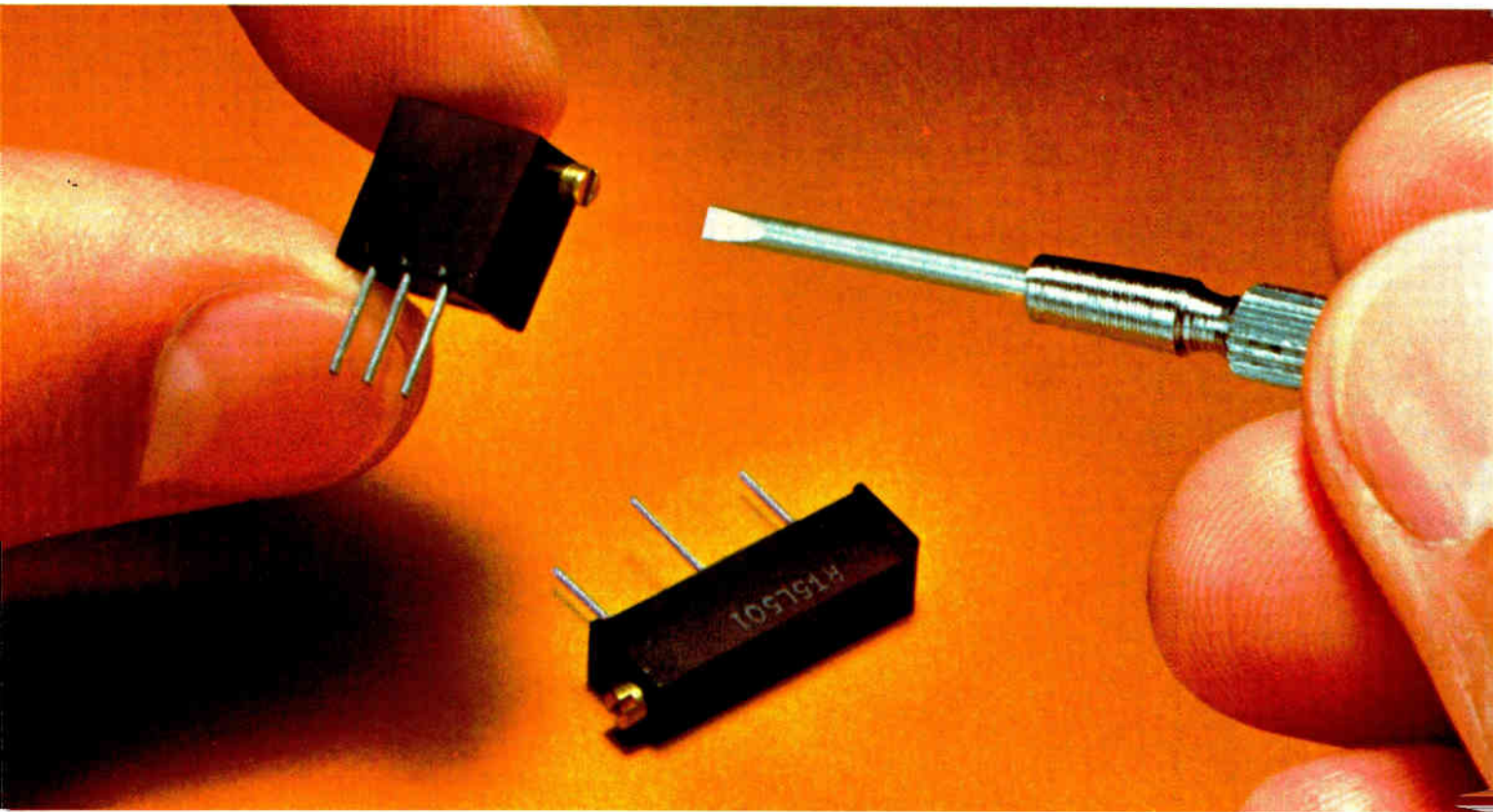
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## **Fujitsu 65-k RAM, headed for U.S., has lofty goals**

The 65-k dynamic random-access memory from Fujitsu Ltd. that will hit the U. S. market, probably by the end of this year, **will offer surprisingly high performance** for a first-cut prototype part if semiconductor designers for the computer manufacturer meet their target specifications. Those goals are: access time, 110 ns; cycle time, 300 ns; two-power-supply operation at +7 and -2 v; operating power dissipation, a low 250 mw; and a standard 16-pin multiplex ceramic package. Fujitsu is using a 2- $\mu$ m-channel two-level polysilicon-gate cell design and an ultrasensitive (30-mv) sense amplifier to get the job done. Moreover, the die size is impressively small at 33,500 mil<sup>2</sup>.

## **Consultant sees IBM on brink of diversification**

IBM Corp. could soon start a new wave of diversification, says International Resource Development Inc. of New Canaan, Conn., an independent management consulting firm. The firm perceives a strong and growing possibility that **"price deterioration will bring to a halt the growth in computer user spending** and will force IBM to reach far outside traditional market areas in order to maintain its forward momentum." IBM, the report continues, "may be expected to introduce numerous minicomputer- and microcomputer-based controls and instruments in the next 10 years."

## **SMC, TI complete microprocessor royalty deal**

Fattening its already comprehensive licensing portfolio, Standard Microsystems Corp. of Hauppauge, N. Y., has made a royalty-bearing agreement with Texas Instruments Inc. **providing for the second-sourcing of specific microprocessor and microcomputer peripheral products.** Covered in the worldwide, nonexclusive pact are: SMC's CRT 5027 video timing and control chip, a high-speed, high-density n-MOS large-scale integrated controller circuit for cathode-ray-tube terminal applications; TI's TMS 9980 single-chip central processing unit with an 8-bit data bus; and TI's TMS 4732, a 32,768-bit n-MOS read-only memory.

## **Low-power, 1-chip microprocessors coming from TI**

Anticipating strong demand for a low-power version of its TMS 1000 series low-end one-chip microcomputer, Texas Instruments Inc. will soon be offering the family in a 1-MHZ complementary-MOS design. **It dissipates a mere 15 mw when operating and 50  $\mu$ w when standing by.** Like the original parts, the c-MOS line will have various input/output and memory configurations, ranging from 1,024 to 2,048 bytes of on-chip read-only memory and 64 to 128 4-bit words of on-chip random-access memory. Motorola also intends to supply c-MOS 1000s. At the same time, Intersil is planning a low-power c-MOS version of Intel's 8048 microcomputer.

## **Data-retrieval system recognizes its master's voice**

Development work is under way at Centigram Corp., Sunnyvale Calif., on a microprocessor-based voice-recognition system able to recognize continuous speech. A version of the system, obeying one-word spoken commands, was demonstrated late last month at DataComm 78 in Washington, D. C. When told to do so, it searched the files of the New York Times Information Bank some 200 miles away and seconds later displayed abstracts of the selected topic on a cathode-ray-tube terminal. **Called Mike, it "learns" its 16-word vocabulary by generating a pattern through a spectrum analysis process and storing it in a designated memory location.** It then compares the patterns of each word it hears against those

stored in memory. When an acceptable match is found, Mike transmits a string of characters associated with that word to the information bank. Centigram's president George Glaser says that other companies also are busy developing terminals able to recognize continuous speech rather than just discrete words.

## **Control system with 16-bit processor due from Analog**

Look for Analog Devices Inc. of Norwood, Mass., to continue its policy of vertical integration in analog data systems. This month, the firm's Instruments and Systems Group is introducing what it calls a real-world measurement and control system **that is aimed at laboratory automation and industrial process applications**. Dubbed Macsym, the system contains a 16-bit digital processor, accommodates up to 16 analog or digital input/output cards, and offers up to 32 kilowords of memory. It uses a single or dual floppy-disk drive for program and data storage, plus a standard teletypewriter as a console for writing and running programs.

## **Teradyne to unveil 5-MHz tester for micro boards**

A high-speed tester, able to handle the vast majority of microprocessor boards, is being introduced at Nepcon West by Teradyne Inc. of Boston. Labeled the L135, **the 5-MHz system uses guided probing to detect faults at the component, rather than bus, level**. An outgrowth of the L125 system, the tester runs off Teradyne's M365 controller and can be integrated with its P400 automatic programming system. A typical test configuration will sell for \$175,000 to \$200,000.

## **Instrument blends scope and logic analyzer features**

A new type of instrument, the digital testing oscilloscope, which combines the features of a time-domain logic analyzer and a storage oscilloscope, is being introduced by Biomation Corp., Santa Clara, Calif. It also serves as a go/no-go comparison tester, using an integral magnetic-tape cartridge drive to store and play back reference logic traces, which can be compared with signals picked up from a system under test. The instrument, the model DTO-1, **looks like a conventional oscilloscope, but its operation is almost totally digital**. A 6800 microprocessor makes decisions during comparison testing and controls conversion of analog signal traces.

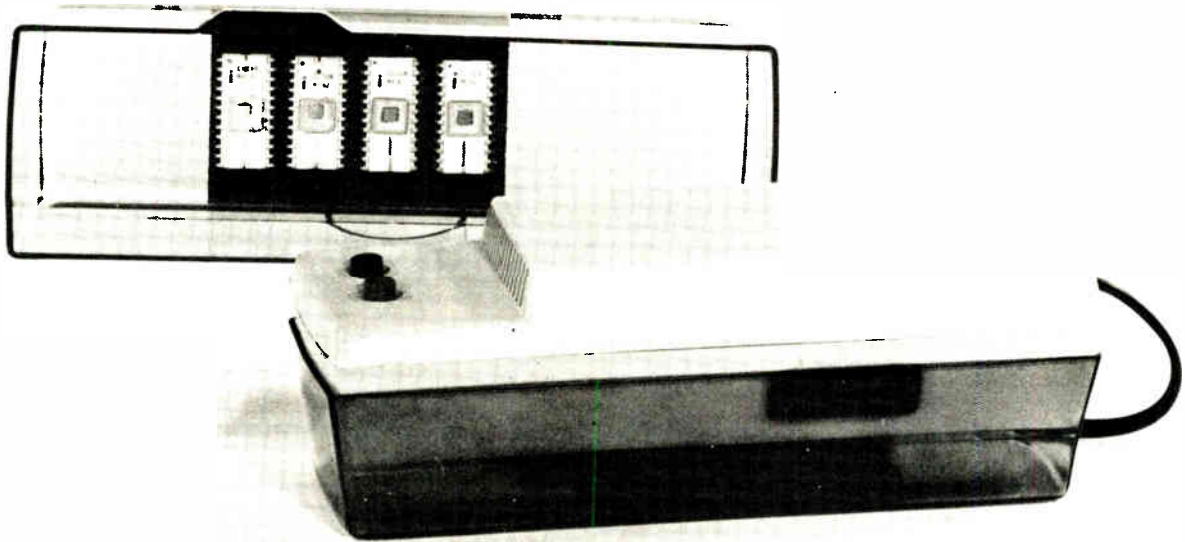
## **IEEE board chooses electron slate**

In an unusual action, the board of directors of the Institute of Electrical and Electronics Engineers has bypassed the choices of its own nominations committee to select its slate. Chosen to run for president is **Jerome J. Suran, manager of the General Electric Electronics Laboratory and currently IEEE vice president of education activities**. The nominee for executive vice president is Leo Young of the U. S. Naval Research Laboratory. The move is a swing toward proponents of strong professional activities, since both men were early supporters of such projects.

## **Addenda**

Litton Industries' Advanced Circuitry division has come up with a semiadditive circuit-board process that uses a ductile copper less likely to crack after thermo cycling, **but gives the line definition of additive processing**. . . . Citing the high living costs of the San Francisco peninsula, Intel Corp. **is moving its Memory Components division and the operation that builds single-board computers to Portland from Santa Clara**.

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SBC 80/10A	X	or	X	X		\$495
SBC 80/20-4	X	or	X		X	\$825

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Then it dawned on us that it was a mighty big jump from our 80/10 to the other guy's 80/20-4. That maybe you might not need to go that far.

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BLC 80/11	X	or	X	X			\$470
BLC 80/12	X	or	X		X		\$495
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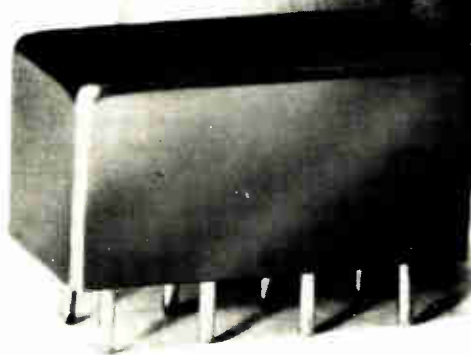
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Yes, a two-year guarantee for hermetically sealed DBM's is now a reality... made possible by an accelerated-life diode screening program adopted at Mini-Circuits.

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Freq. range (MHz) LO - 0.5-500, RF 0.5-500, IF dc-500

Conversion loss (dB)	Typ.	Max.
One octave from band edge	5.5	7.0
Total range	6.5	8.5
Isolation (dB)	Typ.	Min.
Lower band edge to one decade higher	LO-RF 50	45
Mid range	LO-IF 45	35
	LO-RF 45	30
	LO-IF 40	25
Upper band edge to one octave lower	LO-RF 35	25
	LO-IF 30	20

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Signal, 1 dB compression level + 1 dBm

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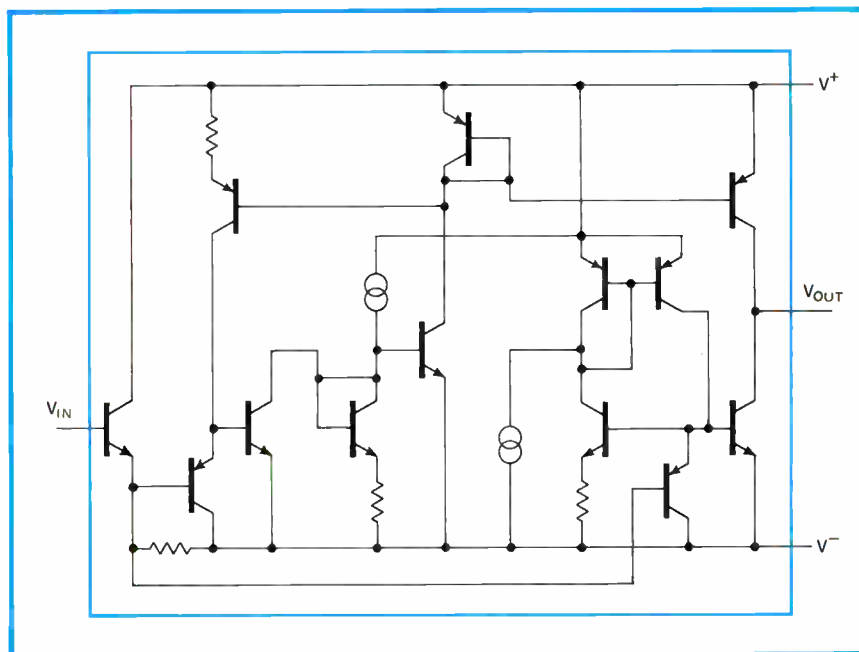
## New process makes possible 1-volt linears

Developed by Robert Widlar of op amp fame, bipolar process will be used in product coming by June

In another breakthrough, Robert Widlar, the father of the modern integrated operational amplifier, has invented a 1-volt linear process that may open up an entire new range of applications for analog technology. Under contract to National Semiconductor Inc., Widlar uses conventional bipolar linear processing to achieve operation from 1-volt supplies. This is in contrast to recently developed metal-oxide-semiconductor processes that, while operating at voltages in the 3-v range, cannot provide the linear performance needed in a range of data-conversion and signal-conditioning applications.

According to Brent Welling, director of marketing for linear integrated circuits at National in Santa Clara, Calif., "our first product based on Widlar's new low-voltage linear technology is targeted for the first half of the year. The new chip will be the first of a family based on his technique that we will push over the next 12 months." Although Welling will not disclose the nature of the first product, industry sources speculate that it will be a general-purpose operational amplifier or a voltage reference or voltage regulator, perhaps.

**The significance.** For good linearity, most analog chips require a relatively high supply voltage, typically 15 v, as compared with the 5-v-or-lower supply of digital circuits. This



**Low voltage.** Class B amplifier on a single chip shows feasibility of building low-voltage linears with standard bipolar processing. Circuit operates from a 1.1-volt supply.

means that digital designs incorporating even just one analog function are likely to require an extra power supply, which adds to cost and takes up valuable real estate.

National's new line of parts, while operating from only 1 v, will still offer the high performance traditionally delivered by bipolar linears. Such a breakthrough will mean precision devices that can be operated off a trickle voltage from a digital supply or even powered by a single nickel-cadmium battery. So designers will have the option of easily adding one or more analog functions to their microprocessor-based or other digital systems without the bother of an extra integrated-circuit supply for the linear chips.

Employing bipolar linear processing, Widlar has shown the feasibility of fabricating low-voltage analog chips, such as op amps, comparators, voltage regulators, and even voltage references. Key to the new technology is a circuit technique for lowering the emitter-base voltage of linear transistors and the inclusion of a current-boosting circuit to increase gain and improve linearity.

**First device.** Widlar, who retired from National several years ago and is now a consultant living in Puerto Vallarta, Mexico, has initially built a class B amplifier and a voltage reference. Operating from a total supply voltage of just 1.1 v, the amplifier (see schematic above) can deliver  $\pm 10$  milliamperes to a load at a saturation voltage of  $\pm 200$  milli-

volts, with the collector-emitter breakdown voltage of the output transistors ranging from 60 to 80 v. Similarly, the reference operates from less than 1 v, providing a 200-mv output that drifts less than 0.1% over a range of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

Noting that linear circuits are still ripe for technological innovation, Welling indicates that Widlar has "other irons in the fire" that also could lead to National chips. □

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**Automotive**

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## Dashboard driven by microprocessor

Cadillac's trip computer, which calls for a drastic redesign of the auto dashboard, is hitting the road as a high-ticket electronic option of the first-on-the-block variety. And General Motors Corp. and its Delco Electronics division are betting that the gadget, called the Seville trip computer, will pave the way for more critical underhood electronics.

The trip computer and its roughly \$1,000 price tag were unwrapped at last week's Chicago Auto Show. A dashboard information center for Cadillac's \$15,000-class Seville automobile, it replaces speedometer, fuel gauge, and clock displays with three groups of two, two, and four digits made up of 100-volt orange gas-discharge displays. Using a dash-mounted, 12-button keyboard, the driver can also call up 11 other functions, including average and instantaneous fuel economy, driving range on remaining fuel, arrival time at a predetermined destination, and engine speed and temperature.

**Production experience.** "We won't sell enough trip computers at this price even to pay for our engineering—no more than 4,000 this model year," admits Robert J. Templin, chief engineer for GM's Cadillac Motor Car division, Detroit. "But it's by far the most sophisticated electronics ever in a car, and we needed it to get some production experience on the road—with minimum interference on critical safety

systems" he explains. "In succeeding years we'll add more functions, and it will fast become an important auto subsystem." Those functions may include control of such operations as carburetion, fuel injection, exhaust-gas recirculation, spark-timing selection, transmission, and cruise control.

There is no question the trip computer, built around Motorola's five-chip M6800 microcomputer, is overdesigned for its task. Future versions should see it replaced by Motorola's two- and one-chip designs, and eventually by a custom processor that Motorola and Delco are developing for General Motors.

The 10-chip system is built largely with standard M6800 parts, including microprocessor, read-only and random-access memories, two input/output chips, and display drivers. Custom chips handle further I/O and clocks. It is all built on five boards: three—processor, I/O, and high-voltage power supply—are housed behind the glove box, and two more are behind the speedometer and clock displays. Fuel consumption is determined by counting pulses from the Bendix Corp. pulse-modulated fuel injectors standard on Cadillac Sevilles. That gives the computer much greater accuracy than the \$100 fuel-metering systems sold by auto aftermarket firms, which rely on fuel-flow sensors. But it also limits the system's use to the 50,000 Sevilles sold each year. □

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**Components**

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## Hall-effect chip comes on film reel

Texas Instruments Inc. gave users a peek at its Hall-effect sensor effort last fall when its first device was introduced in a three-lead plastic transistor package. Now it is clear that the Dallas firm has bigger plans for the semiconductor switching technology than simply position sensing. It has just started supplying samples of a second Hall-effect switch [*Electronics*, Feb. 16, p. 35], this time in a tiny, epoxy-encapsu-

lated package mounted on a reel of Kapton film.

The magnetically activated switch on its film-carrier package is aimed squarely at the high-volume keyboard manufacturers that can afford the automated assembly equipment the sprocketed-film package demands. And though TI declines comment, keyboard manufacturers see the boards with the new parts competing head on against those from Honeywell Inc.'s Micro Switch division, the firm that in 1968 first applied the 99-year-old Hall-effect principle to keyboards. Today, Micro Switch dominates the high end of the keyboard market, estimated last year at \$172 million by market researcher Gnostic Concepts Inc., Menlo Park, Calif. The noncontact Hall-effect switching technology is valued for its long life, extremely high reliability, on-chip signal conditioning, and transistor-transistor-logic-level output.

**Own use.** The new switch also fuels rumors that TI may build alphanumeric Hall-effect keyboards for itself. They would not only replace Micro Switch keyboards used in its computer peripherals but would also probably be used in the personal computer products TI is now developing.

Micro Switch concedes that TI's move may mean competition. At present, the Freeport, Ill., firm is virtually the only source of Hall-effect keyboards, although Hall devices are sold by a handful of other firms, including Sprague, Siemens, and Panasonic. Micro Switch points out that there is more to a Hall-effect key switch than just the chip: besides the sensor, each requires a magnet mounted on the switch plunger in such a way that it passes, and activates, the Hall chip with each keystroke. In addition to fully assembled keyboards, Micro Switch sells Hall-effect key modules, which include chip, magnet, plunger, spring, and housing. These sell for about 40 cents in the tens-of-thousands volume original-equipment manufacturers order.

Although TI will not yet reveal its large-volume pricing, a source at

## Here comes the chip

One of the keys to stripping the cost out of a Hall-effect keyboard is the sensitivity of the on-chip Hall sensor; the greater the sensitivity, the smaller the magnet required to activate it. The output of the new Texas Instruments device, called the TL171, will switch within a 250-gauss positive or negative magnetic field, about one third less than the device TI introduced last fall. It will switch back typically with 100 gauss in the other direction. "We build the Hall sensor in four segments," explains John D. Spencer, applications engineer for TI's Linear Products department. "Each is a Hall-effect sensor by itself, but the four are wired together so that the effects of thermal and mechanical stresses to the chip cancel out." TI has also used on-chip temperature-compensation techniques to protect the device's sensing circuitry, constant-current source, and voltage reference against the effects of changes in temperature.

The Hall device is also the firm's first catalog product offered on reels of film. TI calls the new package TI-TAC, for tape-assembled components; the technique was developed by General Electric Co. under the Minimod label and acquired by TI in 1972. The chips are gang-bonded to tin-plated copper leads on a 17.5-millimeter-wide Kapton film and then encapsulated with liquid epoxy. The sprocketed film is made much like flexible printed circuits: the leads are defined in a series of lamination, photoresist, expose, develop, etch, and tin-plate operations.

another keyboard manufacturer suggests that the TI product will make possible a new and cheaper Hall-effect keyboard design because of the manufacturing possibilities it offers: the fully tested and packaged chip can be automatically applied directly to a printed-circuit board, which is then mounted beneath a mechanical switch assembly. "That's bound to offer a cost savings that Micro Switch doesn't have," he says. In contrast, the Honeywell division builds its chips into individual, sealed switch modules that are ganged together on a pc board.

The new switch is different from TI's earlier plastic-packaged version

and will command a slight premium over the original's 34-cent price tag in lots of 1,000 and up, says Delbert Whitaker, marketing manager for the firm's linear products department. Both high-performance switches combine a silicon Hall-effect sensor, signal-conditioning and hysteresis-tailoring circuitry, and an output transistor on a single chip. But TI has tightened the new device's specifications so that a smaller magnet will trigger the switch. It also has added a fourth pin so that the switch can be inhibited with a strobe signal, a technique widely used in keyboards to prevent more than one keystroke at a time. □

### At the ISSCC

## Combined MOS and bipolar chip yields fast, low-power RAM

Over and above the scheduled program, record-breaking throngs at last month's International Solid State Circuits Conference in San Francisco heard a flurry of late-breaking developments. They included a mixed digital process for fast, low-power memories, as well as two methods for integrating power

devices onto silicon (see the next two stories).

The digital large-scale integrated process puts complementary-metal-oxide-semiconductor, n-channel MOS and standard bipolar transistors on the same chip. The result: a 4,096-bit static random-access memory with an access time typically of 43

nanoseconds and a power dissipation of 100 milliwatts. This speed-power performance is five times that of new 4-k static devices built with either n-MOS or bipolar techniques.

By mixing the technologies, designers from Hitachi Central Research Laboratory optimize the operation of each portion of the memory. They use n-MOS in the memory array to optimize cell switching speeds, C-MOS in the peripheral decoding and sense-amplifier circuits to minimize power dissipation, and bipolar npn transistors to boost the output signals to transistor-transistor-logic levels for driving high-capacitance loads.

The Hitachi cell is built with the standard static cross-coupled n-MOS flip-flop configuration coupled with high-resistivity polysilicon loads. The compact cell size—1,120 square micrometers—is about half that of existing n-MOS depletion-load cells.

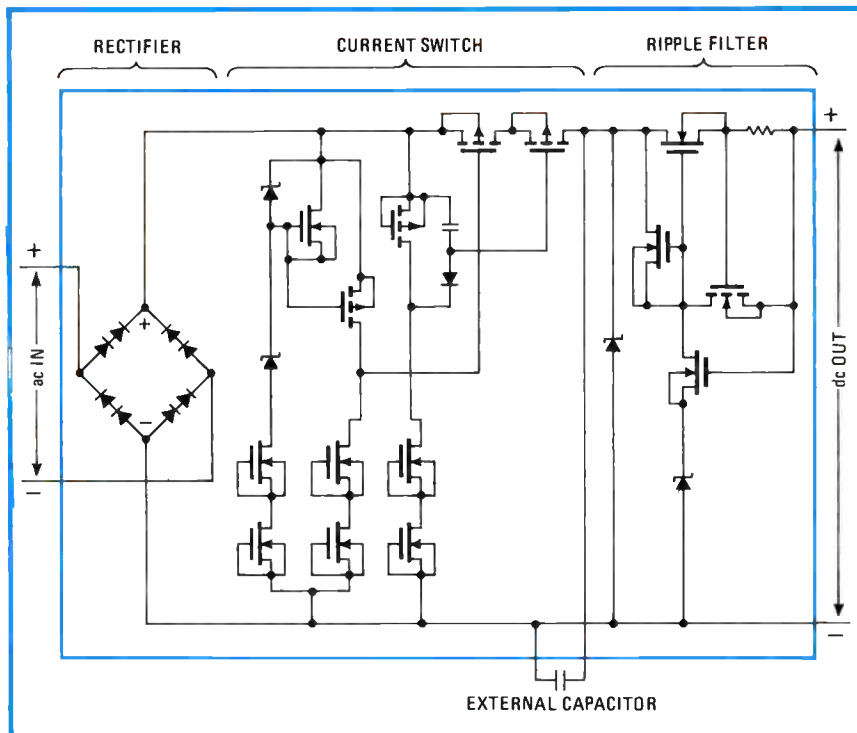
On the other hand, the C-MOS sense amp, which consists of an n-MOS differential pair with p-channel MOS loads, not only saves power with its low-current operation but also results in nice high-voltage output swings.

## Monolithic supply powered by 110 V

In power devices, West Germany's Siemens AG has developed a monolithic power supply that can operate directly from 110-volt ac lines. The new chip, which was also described at the ISSCC meeting in San Francisco, replaces at least a score of discrete components, which tend to be both expensive and, certainly, considerably more bulky.

Getting dielectric isolation from a sapphire substrate, Siemens is using what it calls epitaxial silicon films on insulators to build the monolithic supply. Not intended to compete directly with large supplies, the unit may be used in low-power applications requiring under 1 watt and where isolation from the line is not necessary.

The chip itself, as shown in the



**On a chip.** Power supply, integrated by Siemens on a single chip of sapphire to operate from a 110-volt ac source, contains conventional elements like the bridge rectifier, current switch, and ripple filter. The chip produces a 10-V dc output and up to 10 milliamperes of current. Ripple voltage is held to less than 100 millivolts. The external capacitor is about 15 microfarads.

schematic at the top of the page is designed much like a conventional supply circuit comprising a diode bridge rectifier, a current switch, and a ripple filter. Accepting a 110-v ac input, the chip produces a 10-v dc output at up to 10 milliamperes of output current. Ripple voltage is held to less than 100 millivolts, and efficiency is better than 30%. The chip requires only a single external capacitor, typically of about 15 microfarads.

**Bridge rectification.** Chip operation is straightforward. The diode bridge converts the ac line voltage into a rectified pulsating dc voltage. To increase voltage capability, Siemens cascades the diodes and has achieved breakdown voltages of more than 500 v with a pair of series-connected implanted diodes.

The current switch loads the external capacitor and keeps power dissipation low. At the heart of the switching circuitry are p-channel tetrodes that provide the increased breakdown voltage and high conductance needed for switching. To build

them, Siemens uses a thick-stepped oxide, implanting dopants into the silicon to extend the drain region. With this type of construction, breakdown voltage is typically as high as 180 v.

The ripple filter portion of the circuit includes a series regulator. For overload protection, this section is able to provide current limiting for output currents that are in excess of 12 mA.

## Trimos combines triac, MOS devices

Another innovation in power at ISSCC comes from California's Stanford University, which has developed a way to put signal and power devices on one and the same piece of silicon.

Called Trimos, the new technology permits integrating an insulated-gate triac with metal-oxide-semiconductor components, inviting a host of new applications in crosspoint

switching, output stages, and power control.

Trimos is actually a merged device based on double-diffused MOS technology—two high-voltage D-MOS transistors are merged around a common drain. Contact is made to the source and diffused channel of each D-MOS device, forming symmetrical anode and cathode contacts. The shared gate metal forms the unit's control electrode.

In its on state, the Trimos device exhibits a dynamic resistance of less than 10 ohms and can pass currents on the order of amperes. A simple shunt switch, in the form of a conventional MOS transistor, can be fabricated adjacent to the Trimos unit for switching it out of its on state or inhibiting it from triggering. Without such a bypass structure, the Trimos device typically has turn-on and turn-off times on the order of 200 nanoseconds, and its single-pulse dv/dt capability exceeds 1,000 volts per microsecond. □

## Military

### Signal processor goes programmable

Some of the latest large-scale integrated-circuit technology is being exploited by engineers at Sanders Associates Inc. in a versatile and unprecedented architecture for military signal processors. Usually, these processors are hard-wired computers dedicated to a single function, like beam forming, filtering, or fast Fourier transforms, in sonar, radar, electronic countermeasures, and other equipment.

**On the fly.** But the Ocean Systems division of Sanders, in Nashua, N. H., is taking a more general-purpose approach with its programmable processor element. The P<sup>2</sup>E, as Sanders calls it, is intended for future military aircraft, ships, and submarines and can be programmed on the fly to perform any of those specialized functions for which it has been microprogrammed. It competes with hard-wired machines in pro-

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	82S230	512x4 (OC)	82S129	256x4 (TS)	
	82S231	512x4 (TS)	82S114	258x8 (TS)	
	82S215	512x8 (TS)	82S130	512x4 (OC)	
	82S280	1024x8 (OC)	82S131	512x4 (TS)	
	82S281	1024x8 (TS)	82S115	512x8 (TS)	
	82S290	2048x8 (OC)	82S140	512x8 (OC)	
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54S201		256x1 (TS)	82S2708	1024x8 (TS)	
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cessing speed, and its programmability should make it attractive for a variety of missions.

**Outgrowth from ASW.** The division developed the processor as an outgrowth of an acoustic data processor it furnishes for the Navy S-3A anti-submarine warfare aircraft and for Canada's CP-140 ASW patrol plane. In a typical ASW mission, the patrol craft "seeds" an ocean area with sonobuoys, which telemeter the sonar signals they receive back to the plane.

In a central station aboard the aircraft, the data is processed to extract the information that could indicate the presence of a hostile submarine. Fast Fourier transforms could, for example, be performed on the received signals to transform data from the time domain to the frequency domain, and pulse compression might also be included to sharpen the signals that turn out to be of interest. Radar and ECM signals, among others, would be dealt with by the programmable processor in a similar fashion.

But to date, these functions have been performed by unprogrammable, hard-wired number crunchers, because programmability would compromise the speed of a serial machine, says Gilbert R. Dostie, a member of the technical staff and principal investigator on the program. The programmable processor element, in contrast, can be programmed to switch between functions as a result of commands coming from either a manual input or a larger central processor.

**Minimal interrupts.** The P<sup>2</sup>E's processing speed is not hurt by programmability because it uses high-speed logic and memory working in parallel in a distributed, pipelined organization. While one instruction is being executed, the next is being fetched. Dostie says further that this type of organization was chosen because of its ability to process at high speed with a minimal number of interrupts. Data circulates through multiple buses from memory through the multiplier and adders and back to memory. And more than one programmable ele-

ment can be linked in parallel to split the data processing among the various channels.

Each arithmetic unit has an extremely fast multiplier, two adders, and a 16-word scratchpad memory. The multiplier is a single-chip LSI device that performs a 16-bit, 2's complement multiplication in 175 nanoseconds. The system's program controller uses Schottky transistor-transistor-logic bit-slice sequence-control chips, and the external bulk memory is implemented in metal-oxide-semiconductor 16,384-bit random-access memories. The design will accommodate larger RAMs when they become available. A first-in, first-out register serves as the input buffer to the P<sup>2</sup>E. Input data is accumulated until it is needed, so that the pipeline opera-

tion is not interrupted to dump data into memory.

The benchmark Dostie uses to illustrate the processor's speed is a fast Fourier transform. A P<sup>2</sup>E with a single arithmetic unit does a 1,024-point FFT with 250,000 frequency bins in 1 second, or about as fast as a hard-wired machine of equal size, he says. A working prototype that has been built at Sanders Associates fits on six or seven circuit boards measuring 6½ by 7 inches. To do the processing job aboard the S-3A, the new processor could fit in just half of the older unit's nine racks. Summing up, Dostie says, "We tried to let the processing functions dictate the architecture and took advantage of whatever we could gain from using smart algorithms and the latest LSI chips." □

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## Military's eye set on commercial microprocessors for its programs

Designers of the next wave of military electronic systems are pushing to take advantage of fast, low-cost microprocessors flooding out of semiconductor houses. All three services, in fact, have programs to employ commercial processors as computing elements, they reported in Los Angeles last month at Wincon '78, the Institute of Electrical and Electronics Engineers' 19th annual Winter Convention on Aerospace and Electronic Systems.

The cost benefits of using commercial microprocessors, instead of ones designed to survive costly and time-consuming military qualification testing, are pointed up by comments of one Government engineer now in the process of considering which device to choose for his own program: "The great thing is that all four we're looking at are off-the-shelf products with good performance for our jobs."

**Qualifying delays.** But the impetus to put commercial processors into military hardware runs squarely up against the hurdle that slowed such a move in the past: qualifying devices to military specifications may take

years. At this year's Wincon, however, speakers from the Department of Defense virtually ignored the qualification question. At the same time, they urged designers to use the latest technology industry provides, as did William J. Perry, under secretary of defense, research, and engineering.

In perhaps the oldest and hence best-known program, the Air Force Avionics Laboratory is working toward putting a processor in each of the sensing elements of its Digital Avionics Information System [*Electronics*, Feb. 6, 1975, p 76]. A so-called hot-bench system, DAIS is used for testing new avionics components and systems.

"We think we can apply the distinct advantages of microprocessors to make DAIS more flexible and cheaper," says Frank Scarpino, acting chief of the Systems Technology branch at Wright-Patterson Air Force Base in Ohio. The Air Force intends using the processors in systems like inertial navigators, radars, and fire controllers to make computations at the sensor rather than multiplexing data back to mini-

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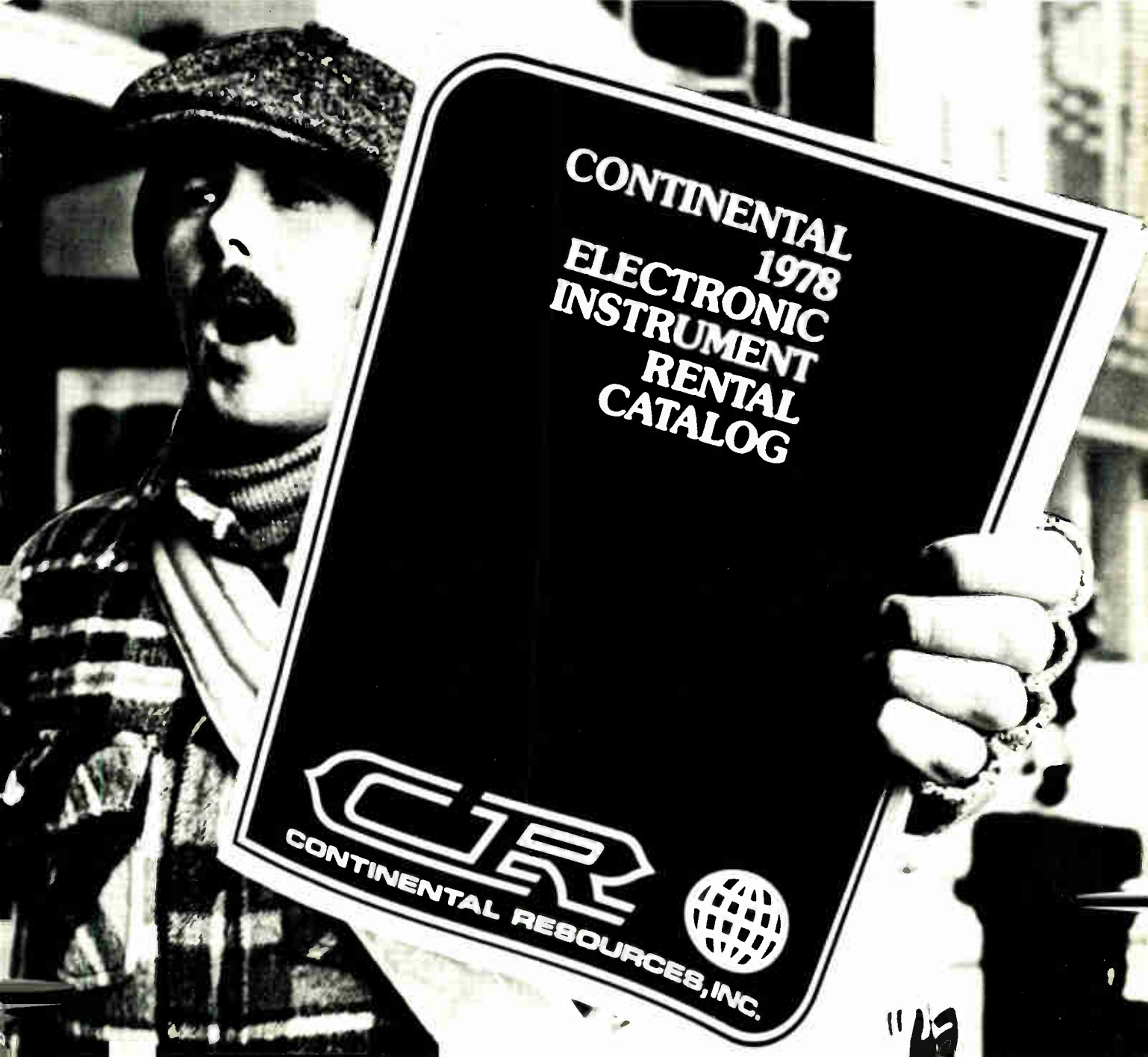
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computers at a central processor.

The next step will come within a few months when Scarpino hopes to select from among commercially available chips, "probably bit slices," to build processor hardware. The major task is making sure processor instructions and architecture are compatible with DAIS support software, he says. To rush ahead without such standardization invites "problems so bad as to boggle the mind," he warns.

**Signal sorting.** For its part, the Navy sees microprocessors helping solve perhaps one of the toughest electronic warfare problems, airborne sorting and identification of radar signals in dense electromagnetic environments. To this end, the Naval Research Laboratory, Washington, D. C., is building an airborne three-processor array for signal sorting, according to Laird Moffett, head of the Systems Analysis section of the Tactical Electronic Warfare division.

"Present computers simply do not have the power to deal with a density reaching 700,000 pulses per second from 420 radar emitters clocked in a recent combined sea-engagement-amphibious-landing maneuver," he says. Electronic warfare systems have to sort and analyze these signals for warnings, countermeasures, and surveillance. Moffett expects the three-processor array, employing bipolar bit-slice 2900 devices from Advanced Micro Devices Inc., to be finished in 1979.

**Programmable sensor.** The Army already has microprocessor-based hardware being tested. In the Remotely Monitored Battlefield Sensor System, or Rembass [*Electronics*, April 14, 1977, p. 77], tactical sensor packages have model 1800 complementary-metal-oxide-semiconductor microprocessors made by RCA Corp., which is also the system's prime contractor. The sensors process detected data to identify targets. The Army intends to use one basic sensor that can be programmed through its microprocessor to recognize many types of targets, including people, tanks, and cars.

"We learned our lesson in South-

## News briefs

### FCC studies proposal to ease uhf crowding

The Federal Communications Commission UHF Task Force has proposed a way of meeting the increased demand for spectrum in the crowded ultrahigh-frequency band without going beyond available technology. Now being studied by the FCC, the proposal recommends a narrow-band system using single-sideband instead of frequency modulation and implemented with a frequency and amplitude compandor that compresses voice signals into a 2.5-kilohertz bandwidth instead of the 15 to 30 kHz now required. As a result, as many as 10 times the present number of channels could be fitted into existing mobile radio bands, reports the task force.

### Producer of photovoltaic solar cells sold

Needing capital to compete, the privately held Sensor Technology Inc. of Chatsworth, Calif., a producer of photovoltaic solar cells, has been sold to Aspro Inc. of Westport, Conn., for an undisclosed amount. A maker of power transmission systems, Aspro has agreed to make a multimillion dollar investment in new equipment and for Sensor Technology president Irvin Rubin to continue to run the 200-employee firm under a five-year contract. Successful in landing major parts of the Department of Energy's low-cost silicon cell program, the firm is supplying 40 kilowatts of cells under the latest DOE 190-kW cell purchase [*Electronics*, Dec. 8, p. 36].

### Electronics mergers up 8% in 1977

Mergers in the electronics industry rose from 60 in 1976 to 65 last year, an 8% increase, reports W. T. Grimm & Co., Chicago-based merger consultants. Of the industry's total, 39 or 60% were divisional or partial in nature, up from the 53% of the 1976 total that were sales of divisions, subsidiaries, product lines, or 10% or more of a company. For transactions involving electronics companies last year, cash was the favorite means of payment, and publicly held sellers accounted for 30 transactions.

### TI receives basic patent for microcomputer

The U. S. Patent and Trademark Office has awarded Texas Instruments Inc. of Dallas a basic patent for the microcomputer, invented by Michael J. Cochran and Gary W. Boone. The patent, No. 4,074,351, is based on a one-chip silicon device about a fifth of an inch square, typically with more than 20,000 transistors or related elements, that was the first integrated circuit to contain all the essential computer functions: program and data memory, arithmetic unit, control, and input/output circuits.

### SDC to build LA's police communications system

Systems Development Corp. of Santa Monica, Calif., has topped Motorola Inc.'s Communications division in the competition to supply the City of Los Angeles with a police emergency communications network. The \$28.5 million system will employ simultaneous digital and voice transmission to all of its approximately 800 mobile units, which will be equipped with digital terminals and receivers, as well as portable radios that officers can unplug and use away from the vehicles.

### Exxon unveils 'intelligent' typewriter

A line of modular electronic typewriters intended to bridge the gap between standard electric typewriters and low-end word processors has been introduced by Exxon Enterprises Inc., the new-business development arm of Exxon Corp. in New York. Called Qyx, the intelligent typewriters are based on the Z80 8-bit microprocessor from Zilog Inc., another Exxon affiliate. Prices range from \$1,390 for a Level 1 machine to \$9,100 for a Level 5 typewriter and options that include: two removable floppy-disk memories; a single-line, 24-character light-emitting-diode display for text editing; and a communications link for talking to other Qyx units and word-processing display terminals from Vydec, another Exxon company.



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Photograph of Andromeda Galaxy, courtesy of Lick Observatory. Photograph has been reversed for composition.

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east Asia, that we had too many kinds of sensors," explains Donald K. Keehan, leader of the Battlefield Sensor group for the Army's Mobility Equipment Command. He notes excellent test results to date and predicts the Army sensor with its processing capabilities could also find civilian security applications. □

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**Computers**

---

## English trying new architecture

The internal organization of the digital computer has not changed for a great many years: a fast central processor fetches programs, instructions, and data from a dumb memory. But this architecture is being challenged by a small logic design and systems company in England that is working on an associative computer in which data is processed in memory.

The company is Icthus Instruments Ltd. in Gateshead, near Newcastle. It says it is 12 months away from having its first system—a small processor to be used for optimizing routes traveled by a numerically controlled drilling machine—built with conventional integrated-circuit logic. The five-year-old company was funded last November with a modest \$13,000 grant from the Advanced Computer Technology group, of the British government's Department of Industry, to pay for half of a four-month feasibility study. It hopes for more money for the hardware.

**Theoretician.** The driving force behind the effort is 42-year-old Ivor Catt, a computer theoretician and consultant to Icthus. He proposes an associative processor that breaks down the division between memory and processor and performs microinstructions in memory to which simple control logic is added. (He calls the processor Property 1A after its patent designation in Britain.) With this basic associative-processor-and-memory element, Catt would eliminate, in one stroke, the

## Integrating it all on a wafer

A complete serial associative processor based on Ivor Catt's ideas might ultimately be fabricated on a single 3-inch-diameter semiconductor wafer. At least, this is the goal of a project at Middlesex Polytechnic, a university in Enfield, Middlesex, funded for the past two years by the British government's Advanced Computer Technology group. Because the processor is made up by stringing together shift registers to which special logic sections are added, the result could be serial associative or random-access memories with million-bit capacities.

Each system would be built up of as many as hundreds of basic building-block arrays. Each array would contain, for example, 1,000-bit shift-register-like structures controlled by a separate instruction line. The array would also have a return bus for data in the shift register and instruction lines. In addition, it would contain address circuitry for connection with adjacent arrays, and pads for wire bonding to external circuits. Metalization grids would provide common clock and supply lines, and fusible links would allow supply voltage shorts to be isolated.

In selecting good arrays and their interconnections, the first array would be tested by applying a 1,000-bit test pattern and comparing input and output. If the array is good, it addresses an adjacent array and both are tested in series. Arrays are added and tested until a sufficiently long chain is assembled. If an array is bad, the last good array is instructed to address an adjacent array until it finds a good one. The test algorithm, stored in an external control chip, starts the array assembly automatically on switch-on.

The interarray switching logic and array assembly concept has been proved on breadboard models with discrete logic by R. C. Aubusson at Middlesex Polytechnic. Now, the design of a metal-oxide-semiconductor shift register incorporating interarray switching logic has also been completed by Plessey Semiconductors. It will be packaged conventionally to prove the logic and is to be developed to produce a wafer-scale integrated device.

fetching and returning of data and instructions between memory and central processor that occupies much of the computer's time and sets a limit on its performance.

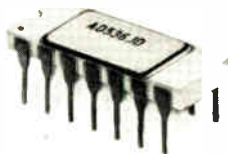
Moreover, the basic element may be applied to associative and random-access memories. Besides saving time and boosting throughput, the use of similar associative elements multiplied through a system would lend itself to low-cost modular construction and, ultimately, to large-scale integrated fabrication on a silicon wafer (see "Integrating it all on a wafer," above).

**Structure.** Catt sees a computer structure made up of a long chain of shift registers through which data words are clocked like the coaches of a railroad train. Each register incorporates gating logic tied to a fast control line. The control line, used for transmitting commands, reading data in and out, and generally manipulating data and instructions, is the key to the computer's operation. The arrangement is analogous

to a two-line railroad siding, with points at regular intervals allowing data to be switched from fast to slow lines. Currently, the logic executes eight microinstructions. In addition to read, write, and interchange instructions, they include logic ANDING, 1's complementing, and end-around carry.

The gating logic can also be used to close any shift register, thus trapping data in a recirculating store while other data words pass by. Another important feature is that subroutines stored on the slow line can be read into the fast line to interact with data upstream. Moreover, sets of data can be made to interact on fast and slow lines.

The drill router that Icthus is building will be made up of a loop of serially connected elements of 256, 512, or 1,024 bits, but the size and number have not yet been chosen. A simple microcomputer made up of a few standard logic packages will control the transfer of data and programs that are going into and



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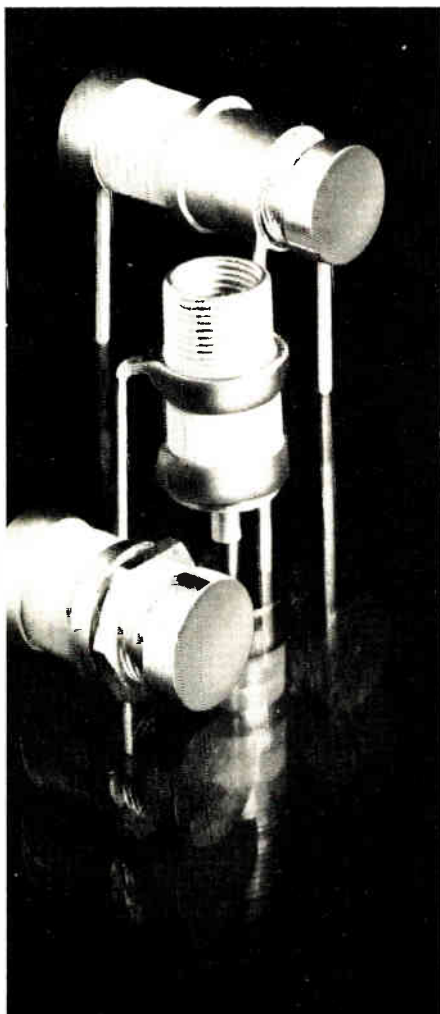
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## Electronics review

out of the processor loop.

Configured as an associative memory, the control logic on each memory register performs match-and-read, match-and-write, and match-interchange instructions between a stored data word and instruction words that are streamed past it. To keep the control logic to a minimum, matching is carried out serially by clocking the data word and the instruction synchronously through bit-comparison logic. This logic tracks bit matches and carries out the gating operation, according to the instruction, when a word match exits. When there is a match, an inhibit flag is set in the instruction that allows the data word to be clocked out. The instruction is then recirculated until no more matches are found.

When the chain is organized as a random-access memory, stored data words are identified, not by a fixed memory address as in a conventional RAM, but by a 10-bit identifier tag assigned to each data word as it is clocked into the system. Read, write, and exchange operations are then activated by an instruction transmitted down the fast line, which incorporates 2 command bits, a 10-bit identifier tag or mask, and a 32-bit data space. All data words are serially compared with the incoming instruction word. □

## Companies

### Optoelectronics

#### Litronix' forte

What has changed at Litronix Inc. since Siemens AG, West Germany's electronics giant, acquired 80% of the Cupertino, Calif., firm last October for \$7.5 million? To let people know, David James, the company's new head, came to New York last month and met with members of the press.

"People were wondering what had happened to us out there," says the 33-year-old Englishman, who took over in December as both vice president and chief operating officer.

"We are now a solid-state optoelectronic company with MOS and bipolar IC capabilities."

Litronix is a prime example of a semiconductor company that reached for the consumer product star and fell back to earth with a thud. "We are completely out of consumer products, which caused substantial losses in 1976 and 1977," he continues. "We even sold our quartz-crystal and printed-circuit-board manufacturing facilities."

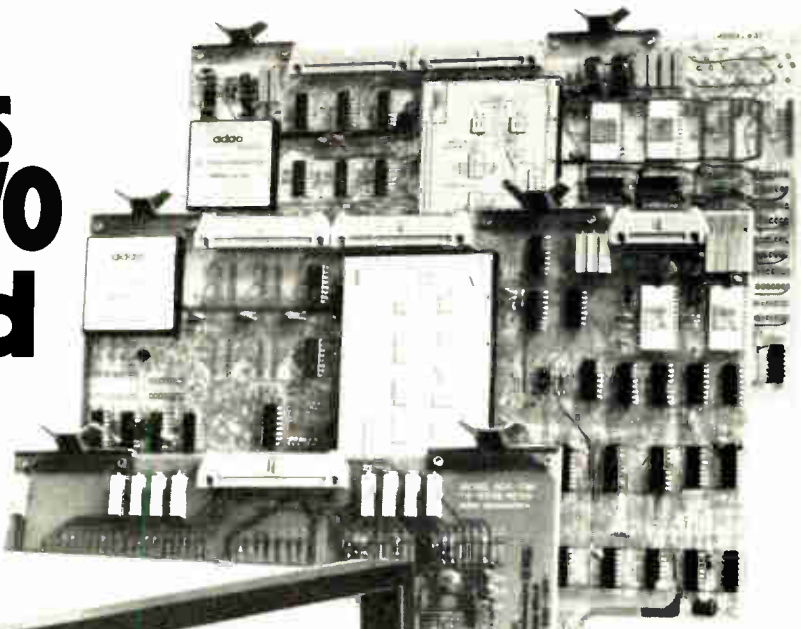
Instead, "our strategy is to integrate logic into the [optoelectronic] display and try to regain for the company the market share it lost when our resources were aimed at calculator and watch products." He has been involved in this strategy at least since August, when he became Siemens' man in Cupertino, commuting between there and Munich.

From a high of \$52 million in 1975, sales last year, which still included some consumer products, were down to approximately \$15 million. James expects to do better this year but will not say when the company will turn a profit.

**Intelligent displays.** He is very interested now in what he calls intelligent displays—alphanumeric displays that include a complementary-metal-oxide-semiconductor chip housing all the decoding and driving logic. Litronix has had a 0.160-inch-high display like this since April and will introduce other sizes shortly. The firm learned a lot building MOS circuits for its watches and clocks, he says, and will apply this expertise wherever it can.

James sees Litronix, with 250 employees in the U.S. and 1,600 more offshore (compared with a high of 4,500 in its calculator and watch heyday), moving in three product directions: display devices, light-emitting-diode lamps, and opto-isolators. To improve the brightness of its displays, Litronix will introduce gallium phosphide, "a technology Siemens has spent a lot of money developing." The firm will likely be applying Siemens' technology elsewhere, too. "We'll also be adding new materials in our lamps and increasing the isolation voltage

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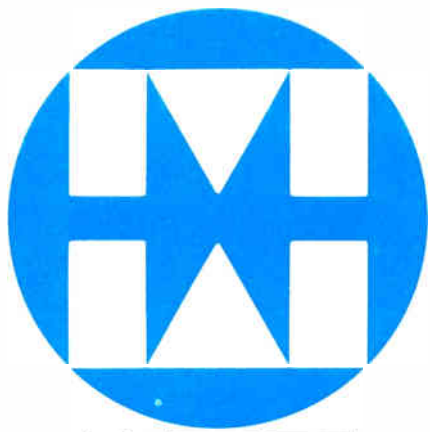
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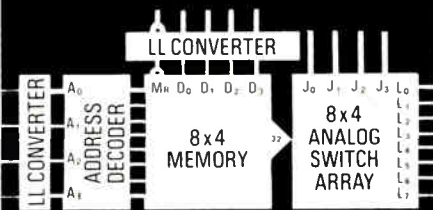
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## Electronics review

of the opto-isolators," he says.

"We've doubled the size of our engineering capability," James continues. "We're taking out ideas people had kept in desks and on the back of envelopes for years. And we're investing to support our manufacturing operations, and we will also be distributing Siemens' line of optoelectronic components." □

## TI management shift looks to future

As the Dallas dust settles around Texas Instrument Inc.'s recent management reshuffling, it is evident that president J. Fred Bucy is trying to do more than solve a few nagging problems in the firm's semiconductor business. TI announced the changes without any clarification whatsoever, and has so far avoided further comment on the strategy it is pursuing.

However, TI insiders, as well as the firm's competitors, view the reorganization as the means for positioning the executives needed for the firm to hit its avowed \$10 billion sales goal by the late 1980s. That game plan steps up the development of new products by both the consumer group and the seemingly stagnant MOS division and intensifies marketing efforts to squeeze more out of maturing bipolar and discrete product families. TI's sales and earning for its fiscal year ending December 31, 1977 set a record—\$117 million net profit on \$2 billion worldwide sales.

Maybe the most attention-getting move is the switch of C. Morris Chang to group vice president in charge of consumer products. It should quell the recent rumors that TI's top semiconductor executive was searching for a new job, perhaps one with the competition. It is unlikely that the 46-year-old Chang is being exiled to direct the smaller, Lubbock-based group for a "cooling-off period," as some TI-watchers have suggested. Rather, his solid technological footing should insure that future consumer products are poised

at the cutting edge of technology, now that TI's brand awareness and distribution channels for its calculators and watches are well entrenched.

To boost disappointing sales in Europe, group vice president Stewart Carrell who headed consumer products is moving back to Nice, France, to take over TI's European semiconductor group. But as the first top-level TI manager in Europe, he also picks up business responsibility for all TI subsidiaries there, as well as a new TI-Europe division set up to market in countries where TI has no manufacturing facilities.

Bucy split TI's Semiconductor group in order to install a senior manager in Europe, and he has given the responsibility for the U. S., Japan, and the Far East to senior vice president James L. Fischer. And since the problems in the U. S. are centered around MOS products, Fischer has brought process-savvy assistant vice president Bernard H. List along with him to run all of the MOS operations.

**MOS view.** Both Fischer and List move from engineering management jobs on Bucy's corporate staff. Their earlier proximity to Bucy undoubtedly will give the TI president a direct channel to the MOS product departments, including TI's less-than-successful MOS microprocessor and memory efforts. Late last year, the MOS operation was split into three parts, with managers moving in from bipolar departments to head up the new memory and microprocessor departments. It is now felt that Fischer's and List's strong technical backgrounds are needed to put the MOS activities on track to product innovation. Fischer was formerly manager of corporate development, and List was manager of TI's corporate engineering center.

Also involved in the shift and reflecting a need for a stronger marketing orientation for maturing product lines, vice president Charles M. Clough has taken over bipolar and discrete semiconductor operations, reporting to Fischer. Clough was manager of marketing for the semiconductor group. □

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## Washington newsletter

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agreement" whereby Japan agreed to limit color TV exports to the U. S., but will risk a significant breakdown in the international negotiations over the General Agreement on Tariffs and Trade (GATT) at Geneva this year and produce retaliatory actions.

### **FCC drops tests of new CBs; cites improvements**

The Federal Communications Commission has dropped its requirement for 100% sampling of new 40-channel citizens' band radio models. The radios swamped its laboratory division when the rule was imposed nearly two years ago. The FCC says it is dropping the test because it has seen "a gradual improvement in the performance of equipment supplied by all manufacturers." The commission will now test samples of transceivers purchased at retail, invoking the 100% rule and other enforcement actions only against manufacturers whose CBs are in noncompliance.

In a separate action, the FCC wants comments from the telecommunications industry and the public by May 1 and replies by June 5 on an investigation of ways to improve communications services for the more than 13 million deaf and hearing-impaired persons in the U. S., indicating dissatisfaction with the "very slow speed" and the incompatibility of existing teleprinter terminals now in use with standard communications computer systems.

### **Two tactical systems move to production at Ford, Litton**

New emphasis on airborne tactical weapons is evident with two Air Force production contracts to Ford Aerospace and Communications Corp. and Litton Industries Inc. Ford's Aeronutronic division, Newport Beach, Calif., is getting nearly \$48.5 million for initial production over four years of **149 Pave Tack pods for day-and-night target acquisition and laser designation for weapons delivery.** Pave Tack, to be used on the F-4E, RF-4C, and F111-F fighters, is an advanced version of Ford's Pave Knife successfully used in Southeast Asia.

Another award by the Air Force's Aeronautical Systems division gives Litton's Amecon division, College Park, Md., more than \$430 million for production of the first 19 programmable, broadband passive sensors for airborne tactical reconnaissance by the RF-4C. The AN/ALQ-125 system called Terec—for tactical electronics reconnaissance sensor system—automatically spots enemy ground-based radars used by mobile surface-to-air missiles and other weapons.

### **Airborne radars seen enhanced by NRL technique**

The performance of airborne radars used to detect and track moving airborne targets may be improved by the development of a new displaced-phase-center antenna technique by the Naval Research Laboratory's Tomos L. ap Rhys. The researcher has applied for a patent for the antenna motion compensator, which is expected to permit detection of smaller targets at greater ranges than those now used for airborne early-warning and antisubmarine warfare. The ap Rhys technique compensates for the phase change in signals scattered from fixed objects as a result of the antenna's movement and cancels them. **This is achieved, he says, by employing electronics to move the antenna both parallel and normal to its boresight direction** so that the antenna operates as if it were stationary in space. Other NRL researchers are studying the application of fiber optics to underwater sound detection.



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## SAW delay line brings a new balance to rf voltage-controlled oscillators

Sometimes compromise is the name of the game, and that is why SAW voltage-controlled oscillators will be winners in radio-frequency applications, thinks Plessey Semiconductors. Backing up its belief, the Plessey Co. division is demonstrating a 456-megahertz surface-acoustic-wave VCO with a wide 2.5-MHz tuning range.

Heart of the component is a SAW delay line, whose great advantage as a resonator is that its Q can be chosen to give the best possible compromise of tuning range and stability for a particular application.

Inserted into the feedback loop of a conventional integrated-circuit amplifier, the delay line determines and stabilizes the oscillator frequency, while additional amps (see figure) ensure that there is enough loop gain to sustain oscillation. The demonstration VCO is intended for mobile radio transmitters and includes a frequency-controlling phase shifter, which is actually a voltage-controlled variable delay. In the demonstration circuit, this delay is made up of a lumped-element equivalent of a 3-decibel transmission-line coupler. Thus, a 5-volt control signal will modulate the oscillator's center frequency by 1.25 MHz.

The SAW oscillator provides a balanced engineering compromise between precision quartz-crystal oscillators and conventional lumped LC oscillators, says Ron Towns, product group manager for radio communications and radar circuits at the Semiconductor division of the Ilford, Essex, firm. He sees its use spreading to the instrumentation fields and to radio-link and fm telemetry applications from such uses as military electronic-countermeasure systems.

The most common oscillator in radio equipment is a resonating bulk quartz crystal, because of its high precision. Above 25 MHz, however,

overtone crystals or frequency multipliers are necessary to generate the higher frequencies, and these techniques greatly increase circuit complexity. Moreover, the greater stability of these oscillators means that they cannot readily be frequency-modulated, so they have limited use as transmitters.

In contrast, the frequency of a lumped-circuit oscillator can be readily pulled to provide any range of modulation. However, the midfrequencies of such devices are prone to drift. Thus there is a big gap, which Plessey aims to plug with custom-designed SAW-device technology.

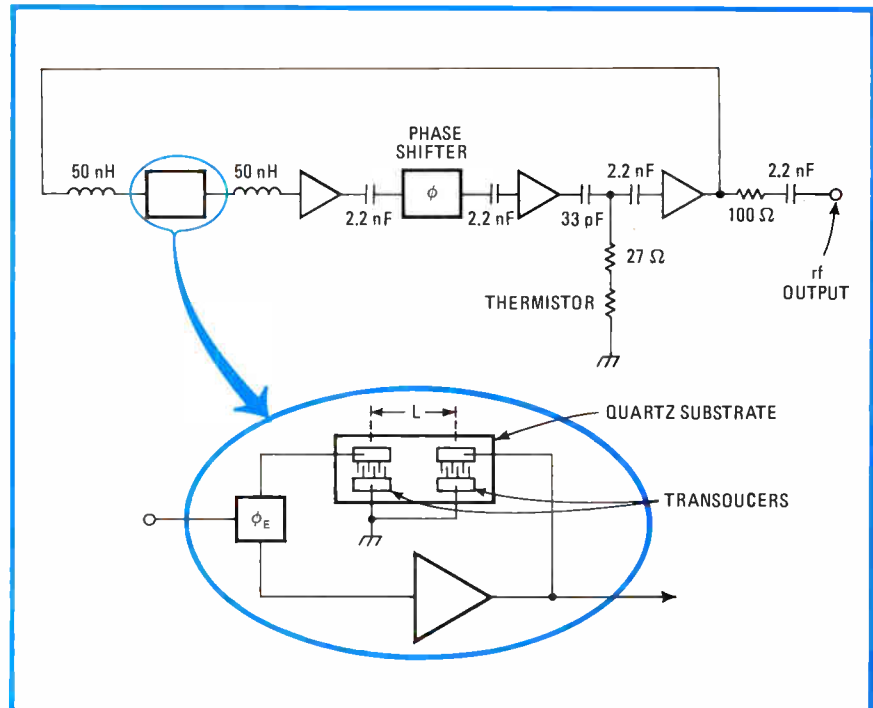
The SAW delay line in the oscillator consists of a polished quartz substrate on which are two aluminum interdigitated transducers made with standard photolithographic techniques. When one transducer is excited by an rf signal within its passband, it will generate substrate

surface waves, received after a short delay by the second transducer.

The delay line has an amplifier connected between its input and output. The circuit oscillates if the amp gain is greater than the delay-line loss, with the oscillation frequency occurring in the bandpass region of the delay. The precise frequency is determined by the fixed phase delay in the SAW line and the variable phase shift in the circuit.

**Stability.** Since the SAW delay line is built on quartz, it is very stable—more so than the variable delay, which is made up of varactor diodes, inductors, and capacitors. For maximum stability then, the SAW delay should be much longer than the variable delay.

If the SAW fixed delay's length, L in the figure, is made greater than about 400 wavelengths by adding interdigitated fingers, then the system's frequency stability can be



**Good vibrations.** Plessey voltage-controlled oscillator will resonate if the gain of the amplifiers in the feedback loop is greater than the loss in the SAW delay line (in circle).

enhanced. This increase is possible because phase shifts arising from temperature or component drifts become negligible in comparison with the fixed delay. Consequently, the SAW device determines system frequency, and since it is fabricated in highly stable quartz, the frequency can be maintained precisely. However, this scheme limits the tuning angle to no more than 0.2% of the tuning range.

Thus, designing with SAW delay lines becomes an exercise in tradeoffs. A long delay line is equivalent to a high-Q resonator, which gives a stable, low-noise oscillator. A short delay line, on the other hand, can be pulled over a larger frequency range, but at the expense of less stability and more noise. □

### Japan

## Twin film diaphragms cancel mike noise

The noise of mechanical vibration that plagues the built-in microphones of cassette tape recorders will be not even a mild annoyance in future Panasonic units. The reason is a mike design, from parent company Matsushita, that uses a piezoelectric polymer film for a double-diaphragm setup that cancels noise.

Present cassette recorders have electret diaphragms that are about 23 micrometers thick, so that noise caused by vibration is relatively high. To keep it as unobjectionable as possible, the amplifier is throttled. Thus sensitivity generally is somewhat low, while the tape is noisy during playback.

While a significant improvement in sensitivity can be realized with an external microphone, the new built-in mike will permit a substantial improvement, along with a reduction in noise to the point where it is not noticeable, Matsushita engineers say. Below 500 hertz, where the energy of mechanical vibration is concentrated, noise reduction is at least 30 decibels, better than electret mikes in common use today. The

## Around the world

### CII-Honeywell Bull says business is booming

Provisional results are in for the first full year of operation for France's hope in the computer field, and they are heartening news for supporters of CII-Honeywell Bull. President Jean-Pierre Brulé is reporting last year's total receipts rose to \$780 million. This represents a 14% increase over comparable figures drawn from Compagnie Internationale pour l'Informatique, HB, and combined operations in 1976. Orders grew even faster: according to Brulé, they were up 33%. Moreover, the year's profits will be about \$30 million, albeit after government direct aid of about \$90 million.

However, the firm, formed in mid-1976 from CII and Honeywell Bull [*Electronics*, May 29, 1975, p. 48], still faces strong challenges to its survival. Not least of these is the performance of its major competitor, IBM France, which was a key reason for CII-HB's formation.

The year's results do show that the firm managed to pull back some of the French market share from IBM. His Paris-based firm's share of the home market rose more than 14% overall, Brulé says, a figure several points above market growth. IBM France boosted exports by 24%, but managed only a 5.4% rise in the French market. Public-sector orders almost stagnated, according to Jacques Lemonnier, president of IBM France. These figures undoubtedly mean a rise in CII-HB's market share of about 27% and a drop in IBM's share of about 50%.

Not only were orders won in the public sector in France—as might be expected with the heavy government backing—but they also showed up in private buys worldwide. The spate of private-sector wins reinforces Brulé's argument that the company is not heavily dependent on the \$800 million program of government orders in the four years up to 1980. "Eighty percent of our business comes from the private sector," he says. Of course these figures apply to operations worldwide; the firm is a little more cagey on the public/private split within France. On the basis of Brulé's figures, public-sector turnover could be more than 40% of the \$350 million home receipts.

However, the company still has a long way to go. Next year the direct government aid will be cut two thirds to about \$31 million, and Brulé acknowledges that staying profitable will be a difficult challenge. Still, the 33% order increase last year probably will be translated into about a 20% increase in shipments in 1978, a jump that will help the profits at least a little.

new design, optimized for broadband operation at ultrasonic frequencies, will also be used for remote-control applications like television hand-held control units.

The Matsushita design capitalizes on research into the use of polyvinylidene fluoride. Besides having excellent piezoelectric properties when properly processed, it can easily be made as thin films, thus opening the way to use as diaphragms.

**Shape.** The new diaphragms are bowed, so that they compress during one half cycle of the sound wave and stretch during the other. If they were flat, each half cycle would stretch them, generating a double-frequency output.

The double-diaphragm setup gives about the same output as an electret mike, for a sound wave of the same intensity. The back-to-back arrange-

ment, together with the configuration of the sound inlets, assures that entering sound waves either compress or stretch both diaphragms simultaneously—giving twice the output of a single diaphragm. However, mechanical vibration moves both in the same direction, compressing one while stretching the other, and the equal but opposite polarity voltages cancel.

The noise-canceling microphones were developed at the Acoustic Research Laboratory of Matsushita Electric Industrial Co. in Osaka. They are scheduled to go into production this fall at subsidiary Matsushita Electronic Components Co., initially for in-house applications. Later on, they will come on the market with prices taking into account the superior performance, the company says. □

# The only way to measure wet films is with light. And it's the safest way...wet or dry.

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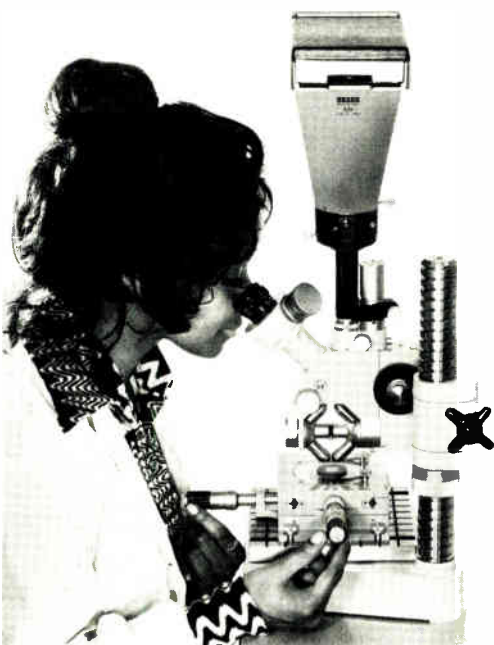
The Zeiss Light-Section microscope uses a razor-edge beam of light to clearly profile the surface of thick-film hybrids, integrated circuits, or other semiconductor components. Then, by fine-tuning a reference line coupled to a micrometer, with  $\frac{1}{2}$  micron divisions, you can easily obtain direct readings of heights and widths ranging from 1 micron to approximately 400 microns. Even an inexperienced technician can learn how in minutes.

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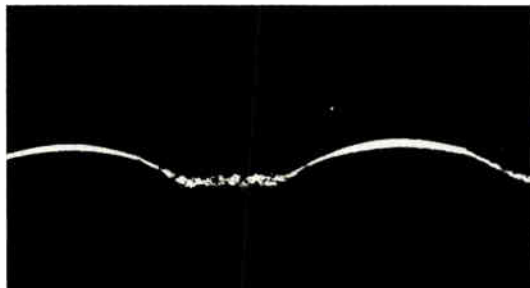
Because there's no physical contact with the surface, there's no chance of damage or false readings. And the built-in camera gives you Polaroid® photo records, as shown below. These examples demonstrate the microscope's versatility. To find out about its economy, ease of use, and accuracy, write or call today.

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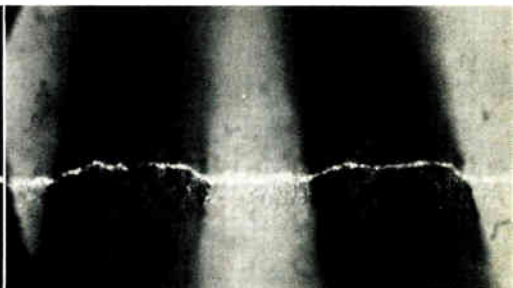
**Carl Zeiss, Inc., 444 5th Avenue, N.Y., N.Y. 10018** (212) 730-4400. Branches in: Atlanta, Boston, Chicago, Columbus, Houston, Los Angeles, San Francisco, Washington, D.C. In Canada: 45 Valleybrook Drive, Don Mills, Ont., M3B 2S6. Or call (416) 449-4660.



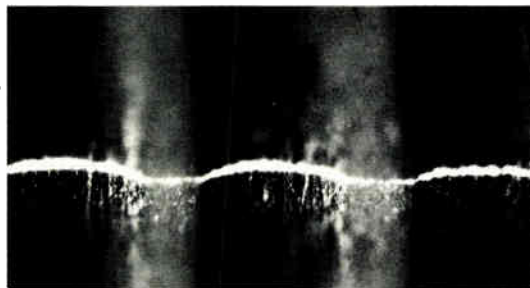
Learning to use the amazingly accurate Light-Section Microscope is a matter of minutes.



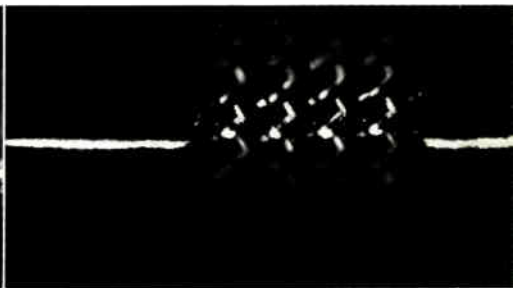
Measuring a thick-film conductor print in the wet state means no waste of substrates.



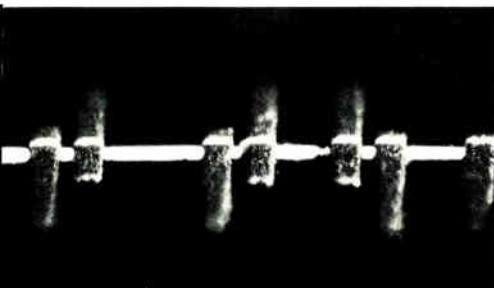
Measuring a dried print to determine if the deviation is within acceptable limits.



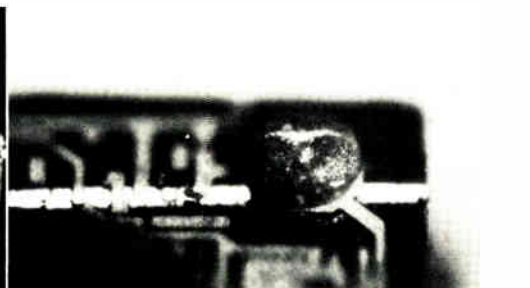
Checking the thickness of a fired print.



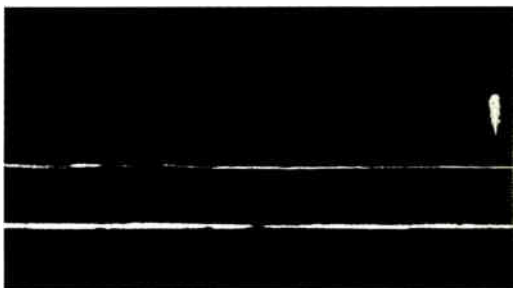
Measuring the emulsion thickness of a thick-film screen.



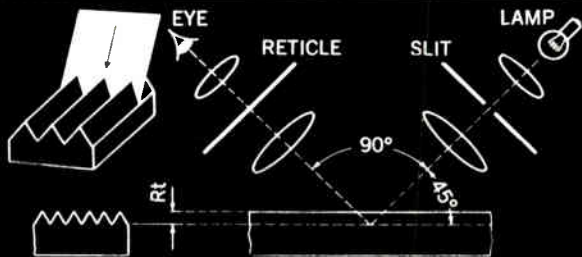
Beam leads on integrated circuits. Height and cross-section are measured.



Flip-chip bumps. Measurement of height and cross-section.



Transparent foil, 71 microns thick.



Principle of the Zeiss Light-Section Microscope.

Photomicrographs courtesy Mr. R. Atkinson, Affiliated Manufacturers, Inc.

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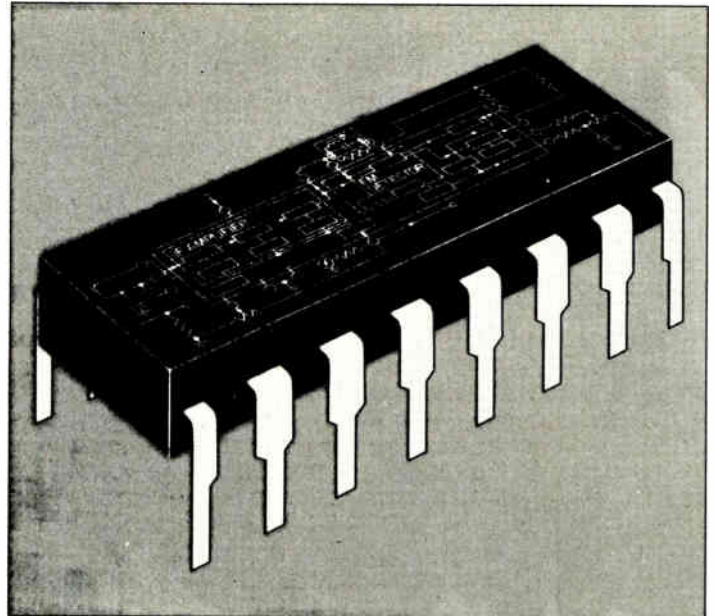
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# RCA

Circle 32 on reader service card

# International newsletter

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## **Large bubble memory is only 4.5 by 5.1 mm.**

Investigation of commercial production of a compact 270,675-bit bubble memory is under way at the Musashino Electrical Communication Laboratory of the Nippon Telegraph and Telephone Public Corp. The lab's experimental 4.5-by-5.1-mm chip is smaller than many earlier bubble memories of a quarter the capacity. **Keys to the size reduction are a bubble diameter of only 1.5  $\mu\text{m}$  and fine-pattern asymmetric chevron propagation elements** with minimum line widths and line spacing of 1  $\mu\text{m}$ . The configuration consists of 270 minor loops of 1,021 bits per loop, plus a writing major line at one end of the loops and a reading major line at the other end. Single-purpose write and read gates are less complex than the read-write gates used with a major-minor-loop configuration, thus making possible the small gates required for a high-density memory.

## **Big deal on In West Germany for TV-game chips**

West Germany's Valvo is getting set to deliver the first batch of game chips in a deal that indicates the growing size of the European TV-game industry. The order, from the electronic game producer Interton in Cologne, "could eventually attain multimillion dollar proportions," says a Valvo marketing official. **The Hamburg-based firm's chip set is a European version of the new game-computer chip set from fellow Philips' subsidiary Signetics Corp.** of Sunnyvale, Calif. [*Electronics*, Feb. 2, p. 51]. The microprocessor circuitry is part of an add-on unit that Interton, one of the Continent's leading game producers, will market shortly.

## **MNOS nonvolatile devices operate from -12-V supply**

Plessey Semiconductors in Swindon is introducing the first three in a family of metal-nitride-oxide-semiconductor nonvolatile logic and memory products operating from a standard -12-v supply. Other nonvolatile MNOS devices require nonstandard supplies of around 30 v to drive and trap the charge in the oxide-nitride interface of the storage transistor. **The new products are a quad latch, a four-decade counter, and a 64-by-4-bit memory.** The Novol devices mix conventional MOS and MNOS devices on the same chip; the MNOS transistors store data for periods up to a year. All inputs and outputs are compatible with TTL and complementary MOS. In addition to standard devices, Plessey plans to exploit its ability to mix technologies on chip in the custom market, which still accounts for over half its business.

## **Register-to-register add time for CPU put at 0.6 $\mu\text{s}$**

Nippon Electric Co. is claiming the "world's fastest" title for its 16-bit one-chip CPU's register-to-register addition time of 0.6  $\mu\text{s}$ . The central processing unit is part of the  $\mu\text{COM-1600}$  MOS microprocessor system that will be available in samples in the third quarter. Initially, sales will be in Japan only, but the company expects to sell chips in the U. S. too. **Support will include an assembler ready about the same time as the CPU and a compiler and a simulator scheduled for the end of year.** The new chips will be attractive in applications such as computer front-end processors and on-line terminals that until now required bit-slice processors, the firm says. The one-chip CPU,  $\mu\text{pd768b}$ , has about 15,000 short-channel silicon-gate n-MOS transistors on a 6.2-by-6.8-mm chip. The basic gates use enhancement-depletion transistors, with enhancement transistors having an effective channel width of about 3.5  $\mu\text{m}$ .

### London tests eyed on data service for motorists

Trials of a broadcast traffic-information service planned eventually to cover the United Kingdom may begin within a few months in the London area. The proposed service would ultimately require a network of 75 very-low-power transmitters spread over the country transmitting on the same frequency and in sequence to minimize mutual interference. Each would relay traffic conditions in its area alone from a central control room. **The car receiver would be an inexpensive, fixed-frequency, ceramic-tuned integrated-circuit unit targeted at \$20 in volume production** and much less if combined with the car radio. When activated by an fm alert tone, it would mute the car radio and transmit the a-m road-traffic message. The UK system still needs a frequency assignment from the International Frequency Registration Board.

### Subnanosecond CML circuitry in the works for French computers

RTC (La Radiotechnique-Compelec), the major components-producing company for the Philips group in France, has started to develop a family of subnanosecond current-mode-logic circuits for computer manufacturer CII-Honeywell Bull. **The circuits will be designed by CII-HB and fabricated with RTC's Subilo technology**, which uses fully-walled-emitter oxide-isolated cells. The firm says about 30 functions will be developed by varying the metalization for five basic arrays.

### Bipolar chip is made with self-aligned process

The newly developed Japanese polysilicon self-aligned process is used in a low-power subnanosecond bipolar 8-bit microprocessor with 1,600 current-mode-logic gates. Internal gates operate with a low 0.6-picojoule power-delay product (0.9 ns, 0.67 mw). Three-level metalization and 120-pin gang bonding help give a very high packing density of 170 gates per square millimeter. **In the PSA process, all contacts and first-level interconnections are fabricated in a single polysilicon layer before formation of the base-emitter junctions.** No margin for alignment of contacts is required because of the self-aligning feature. In addition, lateral shrinking of the polysilicon pattern by selective thermal oxidation gives fine patterns. Development is being undertaken jointly by the Musashino Electrical Communication Laboratory of the Nippon Telegraph and Telephone Public Corp. and the Nippon Electric Co., with actual fabrication by NEC.

### Addenda . . .

Cannon Inc. of Japan is introducing an automatic-exposure 35-mm camera **controlled by a microprocessor built around programmable logic arrays.** An earlier camera from the firm [*Electronics International*, July 8, 1976] uses digital circuits for analog control functions. . . . Texas Instruments' terrain-following and mapping radar for the all-European Tornado multirole combat aircraft **will be manufactured under license in Europe in a complex deal** involving firms in West Germany, Britain, and Italy. However, Great Britain plans to use a Marconi-Elliot all-British design in its air-defense version of the Tornado/MRCA [*Electronics*, July 3, 1972, p. 68]. . . . Without waiting for the results of Viewdata trials that begin this summer, **the British Post Office is pushing forward the date** for the start of public service one year to 1979. . . . Thomson-CSF's semiconductor division, Sescosem, **plans to introduce its first standard modem chip by year's end.** As well as serving in telephone applications, the monolithic modulator/demodulator is intended for low-cost serial memories as in hand-held terminals and for home computers with cassette memories.



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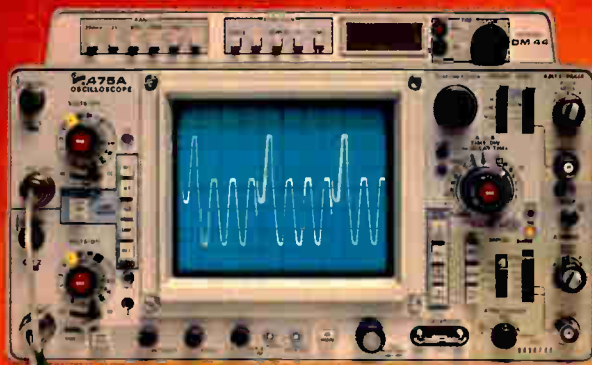
To order a TEKTRONIX Portable Oscilloscope, contact your Tektronix Field Engineer. He can also arrange for a demonstration and provide complete specifications. Or for our latest Portable Oscilloscope Brochure, write: Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077. In Europe: Tektronix Limited, P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

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475A DM44



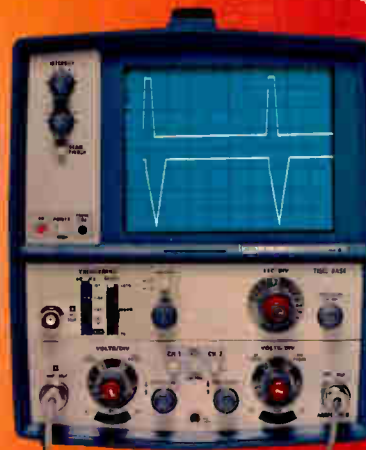
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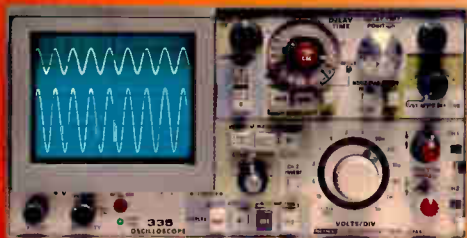
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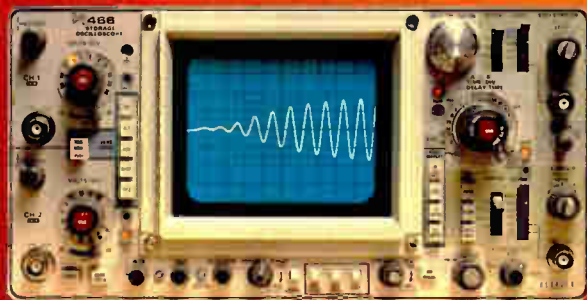
T912



T922



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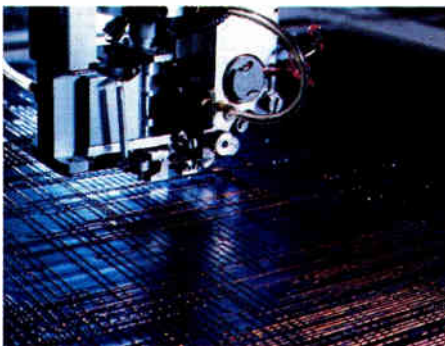
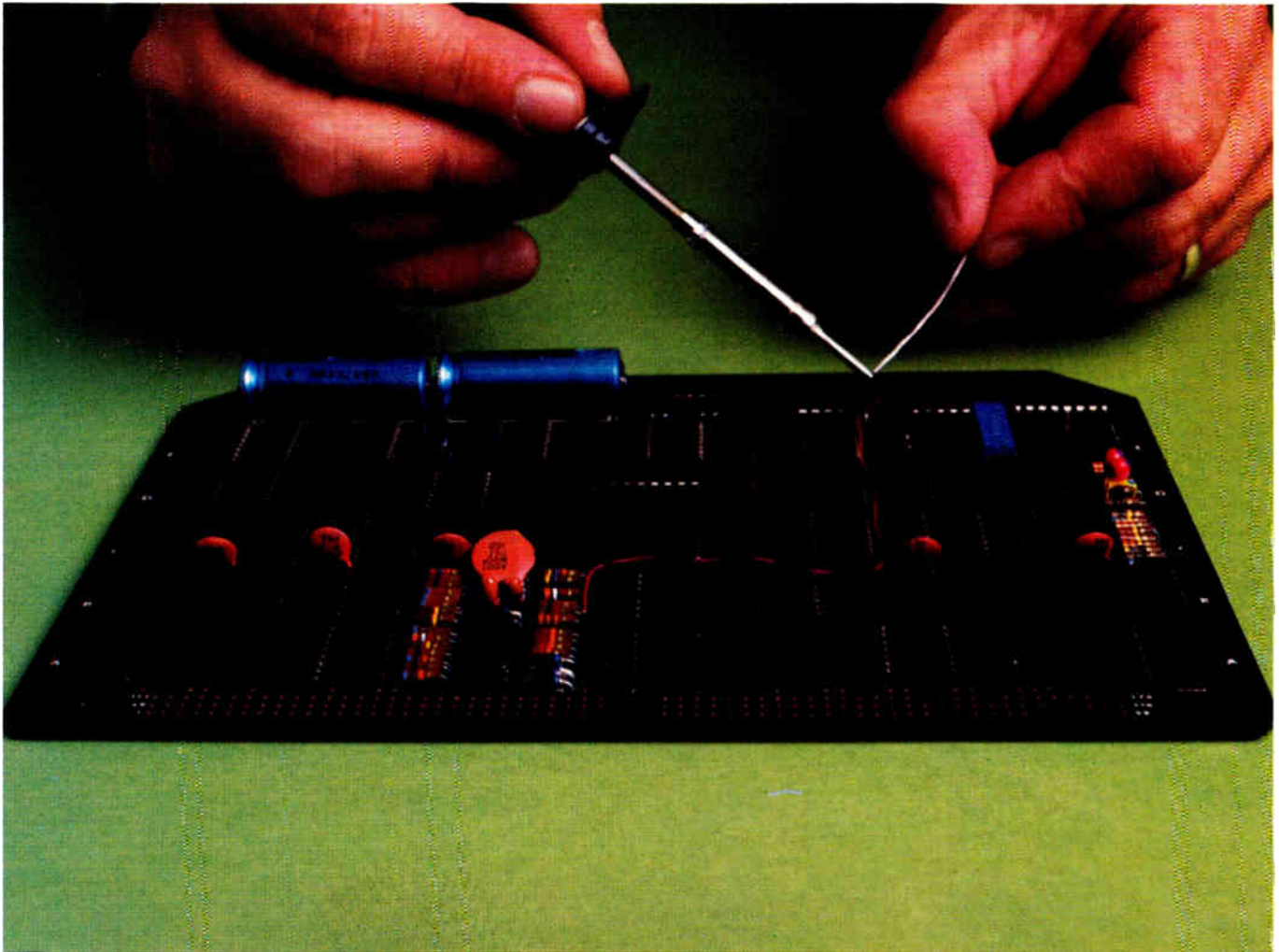


465M

	Product	Bw	Dual Trace	Delayed Sweep	Fastest Sweep Rate	Other Special Features	Price*
Storage Models	466	100 MHz @ 5 mV/div	yes	yes	5 ns/div	3000 div $\mu$ s stored writing speed	\$4750
	464	100 MHz @ 5 mV/div	yes	yes	5 ns/div	110 div $\mu$ s stored writing speed	3995
	434	25 MHz @ 10 mV/div	yes		20 ns/div	Split-screen storage	3150
	314	10 MHz @ 1 mV/div	yes		100 ns/div	Only 10.5 lbs.	2385
	214	500 kHz @ 10mV/div	yes		1 $\mu$ s/div	Only 3.5 lbs.	1475
	T912	10 MHz @ 2 mV/div	yes		50 ns/div	Low-cost bistable storage	1300
Nonstorage Models	485	350 MHz @ 5 mV/div	yes	yes	1 ns/div	Widest bw in a portable	5075
	475A (New)	250 MHz @ 5 mV/div	yes	yes	1 ns/div	High-performance 250-MHz portable	3450
	475	200 MHz @ 2 mV/div	yes	yes	1 ns/div	Highest gain-bw in a portable	3100
	465	100 MHz @ 5 mV/div	yes	yes	5 ns/div	Cost effective for 100-MHz bw	2225
	465M (New)	100 MHz @ 5 mV/div	yes	yes	5 ns/div	Triservice standard 100-MHz scope	2275
	455	50 MHz @ 5 mV/div	yes	yes	5 ns/div	Cost effective for 50-MHz bw	1795
	335	35 MHz @ 10 mV/div	yes	yes	20 ns/div	Only 10.5 lbs.	1895
	326	10 MHz @ 10 mV/div	yes		100 ns/div	Internal battery	1995
	323	4 MHz @ 10 mV/div			500 ns/div	Only 7 lbs.	1445
	221	5 MHz @ 5 mV/div			100 ns/div	Only 3.5 lbs.	995
	213	1 MHz @ 20 mV/div			400 ns/div	DMM Oscilloscope @ 3.7 lbs.	1475
	212	500 kHz @ 10 mV/div	yes		1 $\mu$ s/div	Low cost for dual trace & battery	1050
	T935	35 MHz @ 2 mV/div	yes	yes	10 ns/div	Low-cost delayed-sweep model	1395
	T932	35 MHz @ 2 mV/div	yes		10 ns/div	Variable trigger-holdoff	1125
	T922	15 MHz @ 2 mV/div	yes		20 ns/div	Low-cost dual-trace scope	850
T922R (New)	15 MHz @ 2 mV/div	yes		20 ns/div	Rackmount version of T922	1175	
T921	15 MHz @ 2 mV/div			20 ns/div	Lowest-cost TEKTRONIX Portable	695	
Time Interval Readout	DM44	Optional, factory-installed, direct numerical readout of time intervals and DMM functions for the 464, 465, 466, 475, and 475A					445

\*U.S. sales prices are F.O.B. Beaverton, OR. For price and availability outside the United States, please contact the nearest Tektronix Field Office, Distributor or Representative. Prices are subject to change without notice.

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All wires are exposed in the typical Multiwire board. To make a change, use a blade to cut the conductor that you want to correct, and remove a portion of the wire to avoid bridging. Then, just solder in a jumper wire and

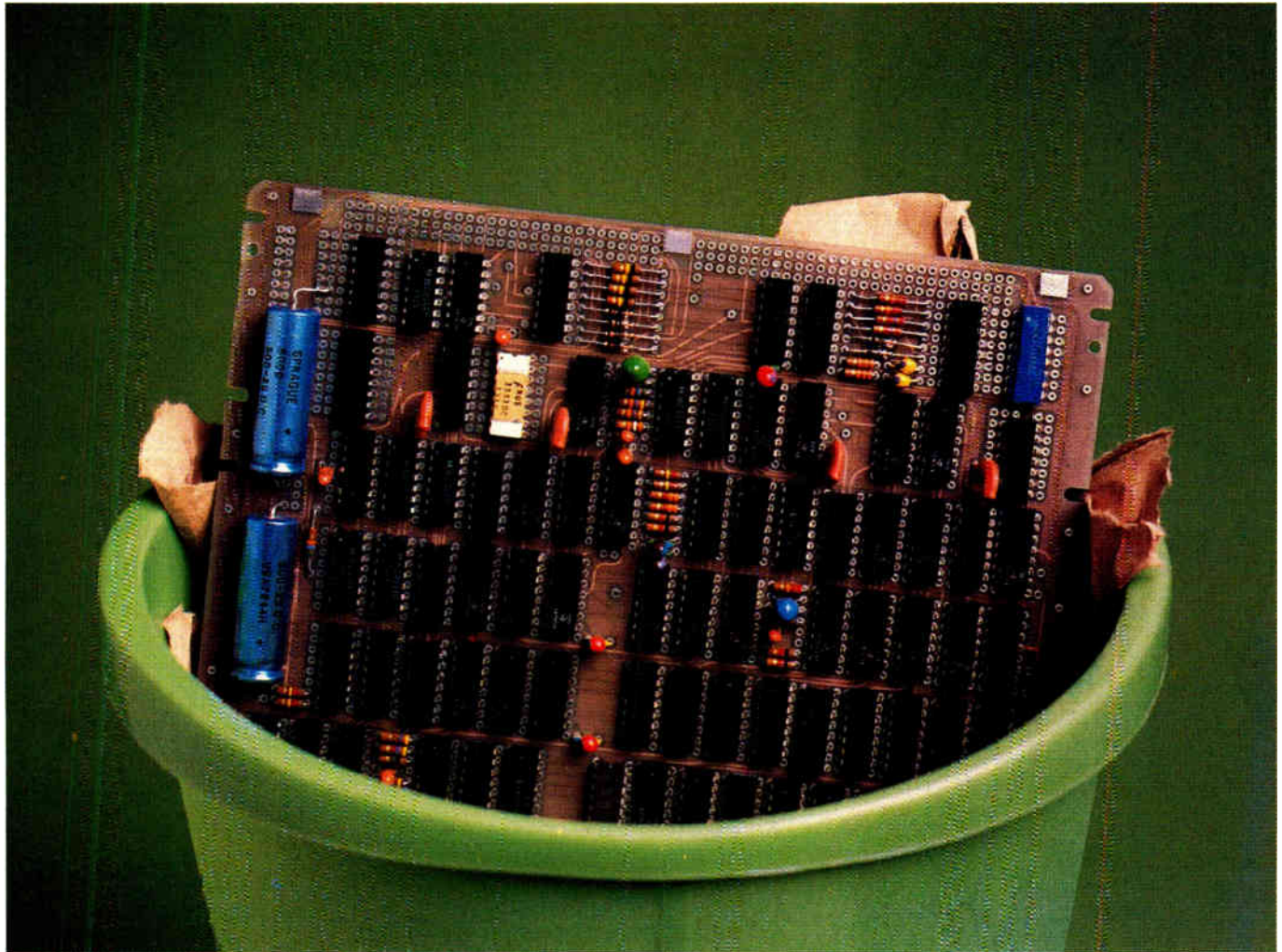
fasten down with epoxy or urethane.

Changes in Multiwire boards can easily be accomplished in minutes by field service technicians.

Multilayer changes, of course, are an entirely different story. Corrections are difficult at best and frequently impossible. As one engineer familiar with multilayer puts it: "Corrections . . . are something of a disaster."

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# Multilayer: Field discardable.



is simply unsoldered; the plated-through holes stand up just as well if not better than regular PC board holes. With multilayer, however, a soldering iron often lifts the land off the board, with many ensuing problems.

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Circle 72 on reader service card

## 32-bit minis face stiff competition

Manufacturers, citing cost and availability of software, are not rushing to follow example of DEC's new VAX system

by Lawrence Curran, Boston bureau manager

When Digital Equipment Corp. introduced its VAX-11/780 computer last fall [*Electronics*, Nov. 10, 1977, p. 36], it seemed that adoption of a 32-bit architecture by the minicomputer leader would hasten the move by others to 32 bits. It's too early to tell if that is going to happen, but the most significant minicomputer introduction since VAX—Data General Corp.'s Eclipse M/600—indicates there is no headlong rush to 32 bits.

The 16-bit M/600, with its fast interleaved memory design and innovative input/output management system [*Electronics*, Feb. 2, p. 40], shows that there are still ways to wring performance out of 16-bit architectures that probably will sustain them as the biggest revenue producers right through the 1980s. Officials at DEC, in Maynard, Mass., do not dispute that; however, what may be one of the most important things about VAX is pointed out by former employee David Nelson, now director of research for Prime Computer Inc., the fast-growing Wellesley Hills, Mass., mini maker.

Nelson maintains that DEC's backing of 32 bits eliminates one more distinction between minicomputers and mainframes. "Word length is one of the many machine parameters that no longer make a difference, like the use of RAM memories and the ability to execute Fortran," in distinguishing the two, Nelson says. While other minicomputer manufacturers have offered 32-bit machines for some time, including Prime, Interdata Corp., and Systems Engi-

neering Laboratories, DEC's endorsement suggests to Nelson that the mini industry will not be judged lacking against mainframes in data-word and memory-address-field versatility. "Now we have to bite the bullet and go back to the functionality issue," he asserts.

Whether the architecture is 16 or 32 bits, Nelson says, functionality means serving more users who have complex data-processing problems that demand substantial amounts of virtual memory address space. However, 16-bit advocates think they have ways to continue improving functionality, and just about every major mini maker cites machine and software costs as the considerations that will govern the choice between 16- and 32-bit machines.

Richard Clayton, DEC's vice president for computer system develop-

ment, sums it up this way: "If the customer's problem is easily solvable with less than 500,000 bytes of memory, a 16-bit machine will be about 30% less costly than a 32-bit machine, given the same technology, and that's the real answer to the 16- or 32-bit argument."

**Logical spots.** Weighing cost vs problem-solving ability vs existing software suggests certain logical application areas for 32 bits. In Oceanport, N. J., James Kerns, product manager for data communications at the Interdata subsidiary of Perkin-Elmer Corp.'s Data Systems Group, says the first and still largest market by dollar volume for 32-bit machines has been the scientific-computation community, "the Fortran people who have large programs and large amounts of data to be processed quickly." A particularly



**Not convinced.** Data General's John Scanlon believes 16-bit machines can equal the functionality of 32-bit minicomputers.

## Probing the news

representative application within that market has been seismic data analysis, which Kerns says needs the 64-bit accuracy that can be obtained by running a 32-bit machine in the double-precision mode.

At Systems Engineering Laboratories, Fort Lauderdale, Fla., product-marketing director Samuel Bosch adds a few more uses. He says real-time data acquisition and control in applications such as electrical-power-plant monitoring is better suited to 32-bit machines because their larger direct-memory-access capability take half the memory accesses required for a 16-bit unit.

**Real-time uses.** His firm's 32-bit machines have also penetrated such real-time markets as telemetry data gathering. "An attribute of 32 bits is that you can have both 32- and 64-bit buses, which lend themselves to higher data rates in NASA and military rocket and missile launches, where you have to gather as much data as possible from an expensive launch and do it fast in real time," Bosch says.

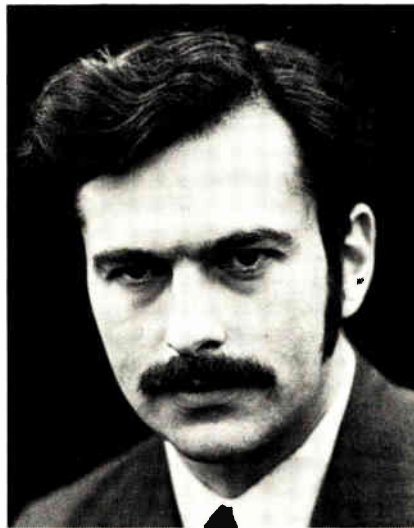
Taking a different 32-bit tack from most in that camp is Neal Young, director of market planning at General Automation Inc., Anaheim, Calif. The company does not yet have a 32-bit machine, but is considering the possibility. Young does not think the unit needs to be more expensive than a 16-bit mini. "All today's applications can be done on 32-bit machines, and maybe cheaper," he asserts.

A few 16-bit advocates refuse to concede that 32-bit machines are necessarily more powerful. One of them is E. David Crockett, engineering manager at Hewlett-Packard Co.'s General Systems division, Palo Alto, Calif. He recognizes only one application area in which 32-bit units have an edge: matrix manipulation in large arrays, but "all the average commercial users couldn't care less," he says, because they do not need that feature. "I think the whole thing of a 32-bit machine is a merchandising scheme and little else," he declares.

John Scanlon, Data General's product marketing manager for pro-

cessor products, Westboro, Mass., is not as blunt as Crockett, but is not ready to make any concessions, either. He cites areas in which a 32-bit organization could theoretically offer more benefits, "but the fact is that we can achieve equal functionality with a 16-bit internal organization." The areas are central-processor execution speed, input/output speed, instruction length, and especially increased memory addressability with a wider access field.

He says that better logical design, more efficient memory management—including interleaving of the memory modules on a 16-bit bus and incorporation of richer 32- and 48-bit instruction words in the main processor and 64-bit floating-point



**The answer.** DEC's Richard Clayton says the key to the decision is cost if customer needs less than 500,000 bytes of memory.

instructions in an extended arithmetic unit—plus incorporation of a separate I/O processor, can all help to equal or better the speed of 32-bit machines. Those are some of the features of the Eclipse M/600.

Another mini maker still successfully carrying the 16-bit banner is Computer Automation Inc., Irvine, Calif., where Larry Lotito is marketing manager for the mini division. He says 16-bit performance is more than adequate for now, with the key being the user's knowing exactly what he wants to do. "If you have specific applications, we can design the memory access to use capacity most efficiently, mostly through byte manipulation," he says.

Up north in Santa Clara, officials at Tandem Computers Inc. are also convinced that 16-bit minis will be around for a long time. Gary Sabo, manager of market support, sees two trends. One is that minis will become multiprocessors performing parallel processing. "That's the way to get horsepower," he says, whether the architecture is 16 or 32 bits. The other trend is that 16-bit units will probably change form, with more of them based on microprocessors.

The biggest obstacle to near-term wider acceptance of 32-bit minis is the software hurdle. DEC's intention for the VAX line is to offer the kind of performance that IBM/370 users get, according to Peter Christy, a staff consultant, "and we've got to be able to offer that same breadth of software support." DEC's Clayton adds that the software has to include a Cobol compiler, which is in the works, "because we perceive that VAX's use as a commercial system is important to its success."

Data General's Scanlon probably summarizes the software challenge best when he says that where tens of man years might be needed to get a new 32-bit machine up and running with minimal software, the time required to write operating systems, multiple compilers, file-system management, and diagnostic software for peripherals is measured in hundreds of man years.

**Economies count.** That's why "16 bits will prevail for quite a long time," he says. "Sixteen-bit machines will account for the major revenues in the minicomputer industry, certainly through 1985 and probably all of the 1980s." The real action in the minicomputer industry now is in machines selling for from \$10,000 to just under \$100,000, he asserts, with average selling prices of \$30,000 to \$40,000.

As Prime's Nelson puts it, "It's very hard to kill a machine in the minicomputer industry." Good evidence of that is the fact that DEC continues to improve on the 12-bit PDP-8 line, which one former company official says had accounted for between \$70 million and \$80 million in revenues a few years ago. Most people in the industry attribute that penetration to the vast accumulation of PDP-8 software. □



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Microprocessors

## Will MDS be the universal tool?

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With market for systems expected to reach \$100 million in 1980, introduction of Intel's low-priced Series II may hasten day

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by William F. Arnold, San Francisco bureau manager

Although it's too early to tell whether microprocessor development systems will become as numerous as oscilloscopes on designer's benches, one thing is clear: they are sparking a skyrocketing market. Late last month that market got a further major boost with the introduction of the Intellec Series II low-priced family by Intel Corp., Santa Clara, Calif., already the generally acknowledged leader in the field (see "Intel turns it on," p. 77).

Industry estimates vary, but many think the 1978 market will reach \$80 million. That figure, up from about \$50 million in 1977, is expected to soar to \$100 million by 1980. An even more bullish estimate comes from Leonard Call, manager of product marketing for microsystems for Motorola Inc.'s Semiconductor Group in Phoenix. He thinks the 1978 figure will be nearer \$90 million. Moreover, business is so strong that it should grow at a 25% to 30% annually compounded rate for the next three or four years, he says. Motorola is generally conceded to be one of the top three in the MDS market with Intel and Tektronix Inc.

Generally agreeing with Call, Galen Wampler, industry analyst with market-research firm Prime Data, San Jose, Calif., estimates this year's market at between \$85 million and \$95 million, growing to \$100 million next year, and soaring to \$125 million to \$150 million in 1980.

Wampler's estimates show Intel shooting from \$20 million in 1976 to \$40 million in 1977 and probably to about \$50 million this year. Motorola probably will do about \$12 million this year, up from \$6 million in 1976 and \$8 million to \$9 million last



**Developers.** Futuredata founders Bruce Gladstone (left) and Paul Page with their Universal MDS. Page, the firm's president, says customers tend to buy several systems.

year. Tektronix is assumed to have had \$4 million in sales in 1977, its first year in the business, and could do about \$10 million this year. Texas Instruments Inc. should rise to \$5 million this year from \$3 million.

Obviously fueling the surging MDS market is the explosion of microprocessor applications. Design engineers need the development systems to design and debug their prototype software and hardware before they commit to production systems.

Other factors strengthen the market. A cofounder of the small, young Los Angeles firm of Futuredata (formerly Microkit), Paul Page explains that companies are buying several development systems because they recognize that "you can't make a \$30,000 designer wait around to use a \$10,000 MDS."

Also hiking sales figures is the popularity of MDS options, says James H. Gibbons, manager of the

central marketing group for up-and-coming Zilog in Cupertino, Calif. Although Zilog's development system is a powerful package for a basic price of \$8,990, the average selling price is going up because "people tend to higher and higher options at initial purchase, and with these tickets you can get into the \$12,000-to-\$15,000 range."

**Two outlooks.** The marketplace is dividing into opposing camps, explains Arnold Karush, product manager for logic development products at Tektronix in Beaverton, Ore. One serves those users who, committed to design in one particular microprocessor, buy that maker's MDS. The other targets development systems toward users who may want to use microprocessors from several semiconductor houses in their designs. In the first camp fall Intel, Motorola, Zilog, Rockwell, and National. In the second are Tektronix,

## Intel turns it on

For Intel Corp., the new Intellec Series II family of microprocessor development system products shows the advantage of being a leading large-scale integration house. By packing a lot of LSI parts into the development systems, it was able to improve performance and lower the cost from its current MDS 800 systems, the most popular in the marketplace, says Sam Sadtler, product line manager.

The series, which comes in three software-compatible products, is designed to support Intel's current microprocessors and upcoming ones, too, Sadtler says. The 210 low-end system will sell for \$3,250, compared with \$4,500 for the comparable MDS 800 unit. Targeted for small 8080 and 8085 systems, the 210 includes its own 8080A-2 microprocessor, read-only-memory-based assembler and text editor, 32,768 bytes of random-access memory and 24 kilobytes of ROM.

Midline is the 220 with its integrated cathode-ray-tube display, keyboard, single-density floppy disk, and a six-slot multiplus card cage. Its price is \$7,245, as against more than \$10,000 for the MDS 800 equivalent, Sadtler says. Chockfull of LSI devices, the 220 features the 8080s, an 8271 floppy-disk controller, 2875 CRT controllers, and 2716 memory chips, he says.

Due out in May is the high-end 230 with a price tag of \$12,900, versus about \$15,000 for the comparable MDS 800. This powerful unit has two double-density floppy diskettes, 65,536 bytes of RAM and a detachable typewriter-style keyboard with upper- and lower-case characters and cursor controls. It includes more than 1 million bytes of on-line storage and can support an overall total of 2.5 million bytes.

Mupro, Futuredata, and, most likely, Hewlett-Packard Co.—when it eventually enters the fray.

Looking at the business, H. R. Anderson, manager of product planning for Rockwell's Microelectronic Device division, Anaheim, Calif., sees "a polarization with interesting repercussions, starting now and in full swing by 1979."

In this confrontation, the first camp's strategy is direct and clear-cut. "My charter is to support Intel silicon," declares Intel's Sam Sadtler, by offering a range of software-compatible systems that are easily upgradable to support Intel's range of microcomputers—in short, everything possible to make sure the user stays with Intel products. Chip makers like to think that they have a better chance in the MDS market than instrument makers that offer general-purpose systems, because, as Motorola's Call puts it, "we're in the best position to understand and serve device technology."

Not so fast, counters Tek's Joseph McCarthy, marketing manager for logic development products. As the market fragments into more and more different kinds of chips, only general-purpose development systems "don't lock customers into one chip family," he states.

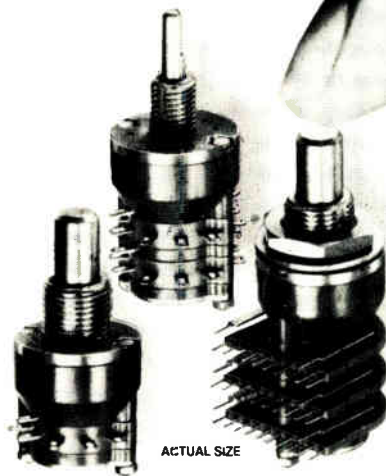
And makers of general-purpose systems can support individual chip sets just as well as the chipmakers, McCarthy says, pointing to Tek's worldwide sales and service network. Through various channels of information, a general-purpose supplier learns the ins and outs of an individual microprocessor as it comes into the market, he says.

**Eying Intel.** As for Intel's new line, reaction is mixed. It seems to be an effort to better fight Tek's 8001 and 8002 systems, observes William Hading, marketing manager for microprocessor development systems for National Semiconductor Corp., which is readying a new system to follow the UDS-1 it brought out last year. Industry analyst Wampler thinks Intel is trying to protect and gain market share among users of Intel microprocessors. However, competitor McCarthy of Tektronix asserts that the new series will only slow the decline in Intel's market share.

What Hewlett-Packard is up to also concerns industry marketers because the MDS market is a natural one for the giant instrument and computer maker. Although HP is characteristically silent about its plans, competitors expect it to bring out a system later this year. □

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Avionics

# It's high noon for MLS shoot-out

British working feverishly to gain reversal of decision making U. S. scanning-beam approach the future standard

by Ray Connolly, Washington bureau manager

Britain is fighting what looks like its last battle in a technological war with the United States. At stake is a new international standard for microwave landing systems for the mid-1980s and beyond. They would replace outmoded instrument landing systems using vhf/uhf frequencies that were first adopted in 1949.

Microwave systems, with their 120° scanning beams, have long been recognized as the answer to air-traffic problems at congested world airports that are often surrounded by high-rise structures or mountainous terrain. Unlike the limited frequencies and straight and narrow flight paths of ILS, the all-weather MLS system permits curved approaches by aircraft, using a scanning beam with broader coverage in both azimuth and elevation.

Britain began its war nearly three years ago when the U.S. Federal Aviation Administration rejected the doppler technique invented and patented in the UK in favor of a time-reference scanning-beam approach. The decision came after a \$40 million investment and two years studying the competing technologies. The FAA has invested another \$80 million developing and testing its choice with Bendix Corp. in Baltimore and Texas Instruments Inc. as its principal contractors [*Electronics*, Feb. 20, 1975, p. 78].

Following extensive evaluation of the two proposals, an International Civil Aviation Organization panel of international experts recommended adoption of the U.S. system as the next world standard. A final vote on the matter is scheduled during a

three-week ICAO meeting in Montreal beginning April 4.

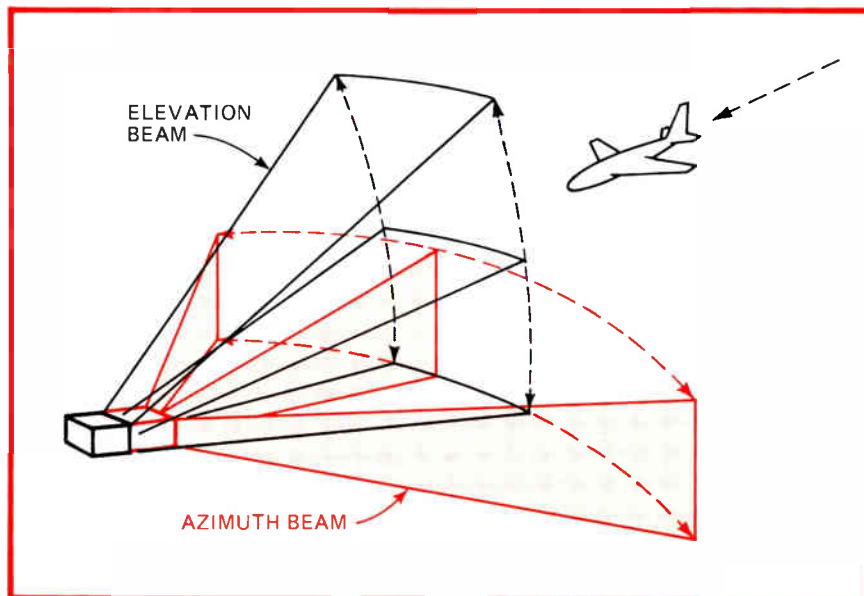
With the U.S. standing to win an estimated \$1.5 billion world market over the next decade, Britain has been lobbying furiously to overturn the FAA choice and stall an ICAO decision. So far, the campaign has generated more heat than light, straining relations between the two allies.

Those strains peaked last month during hearings called "to clear the air" by Rep. John Burton (D., Calif.), chairman of the House Government Operations transportation subcommittee. What troubles an angry FAA is that a final ICAO decision may be postponed until the U.S.-UK controversy cools down. In fact, pressure is mounting in the FAA and other Federal agencies in favor of unilaterally adopting a national standard, a suggestion that is sure to add fuel to the technological fires.

**U.S. policy.** That proposal never came up at the Burton hearings, since U.S. policy is to abide by the ICAO decision, one expected, sooner or later, to be in the favor of the time-reference scanning-beam approach. At the Burton committee hearings, however, the FAA and its consultants strongly attacked the efforts of Britain's lobbyist Michael Lehrman to overturn the U.S. choice. The Americans said he was leveling "deliberately misleading" and "untrue" charges.

Lehrman, who has achieved the status of super-lobbyist since his successful effort to obtain U.S. landing rights for the Concorde supersonic transport, is employed by Plessey. The British firm is developer of the doppler system under

**To and fro.** Time-reference scanning beam MLS, favored by the FAA over doppler, has two sets of beams scanned rapidly back and forth for azimuth and up and down for elevation.



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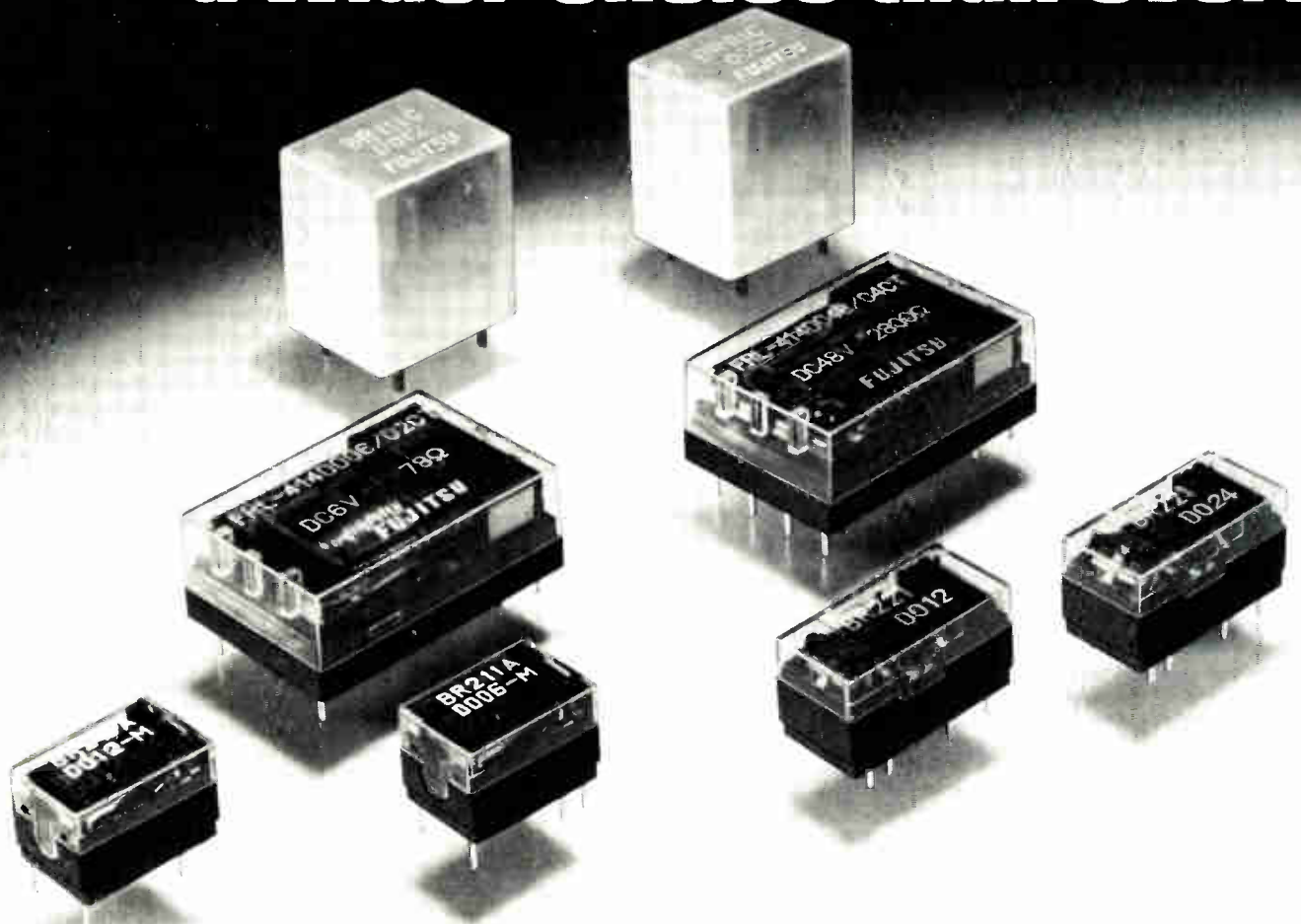
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## Probing the news

contract to the British Ministry of Defence, with the support of the UK's Civil Aviation Authority, a non-government body. Lehrman, who gets \$120,000 a year plus expenses from Plessey, also acknowledged employing the technical consulting services of Charles Varnell at a time when the latter was also consulting for ITT Gilfillan, a proponent of doppler MLS in the FAA competition.

ITT's stake is clear. Charles Earp of its Standard Telecommunications Laboratories in Britain invented doppler MLS and holds basic patents on the technique. The FAA cites the ICAO panel's observation that no similar patents exist on hardware that could hike the U.S. system's cost through royalties or licensing arrangements.

Even before the addition of projected ITT royalties, the doppler system's avionics and ground equipment costs are more than those of the U.S. choice, the ICAO panel reported. Measured in 1976 dollars,

the U.S. avionics for the basic 200-channel, C-band system for small airports would cost \$4,651, or 8.5% less than a doppler system, while the \$125,235 ground equipment price tag is 5% cheaper. For larger commercial transport systems, U.S. avionics costs of \$38,371 are only \$200 under those of the UK system, although ground equipment costs of \$441,810 are 5% cheaper.

Moreover, the ICAO panel concluded that scanning beam has greater growth potential for the future, since it can be modified to cope with a 360° azimuth and it has greater auxiliary data capability. Also favoring the U.S. system was ICAO's judgment that it is more reliable than doppler. The "soft failure characteristic" of phased-array antennas—which the FAA is still updating—"can withstand a number of independent failures in the radiating elements and associated rf feed network without significantly affecting guidance quality," the ICAO panel concluded. "Further, the isolation of individual transmitter malfunctions is somewhat more straightforward" than with doppler. □

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## Hazeltine's new Compact

Hazeltine Corp., a strong early advocate of doppler MLS, has been converted to time-reference scanning-beam techniques, developing a new phased-array antenna for the system that the Federal Aviation Administration is ready to buy. Called Compact—for cost-minimized phased-array circuit technique—an engineering model of the system was flight-tested by the FAA a year ago following investigation of phased-array potentials by the Naval Research Laboratory under an agreement with the FAA. Frank Frisbie, chief of FAA's approach and landing R&D, says the contract now in negotiation would be "a production prototype for major jetport long-runway operation."

Several years ago, the Greenland, N. Y., company went to court to get an injunction against further scanning-beam work by the FAA and lost [*Electronics*, Feb. 20, 1975, p. 78]. Later, Hazeltine's Harold Wheeler worked with the British on a doppler-system redesign to eliminate multipath problems that showed up in early computer simulation tests. Multipath occurs when radio signals, taking multiple paths in travelling from transmitter to receiver, are reflected off buildings and other objects, arriving at different times at the receiver. After the British system redesign, Frisbie told the congressional subcommittee, "this multipath phenomenon had been altered but not eliminated."

With its conversion to scanning beam, Hazeltine is manufacturing a small community MLS system on its own, using the compact antenna for both elevation and azimuth functions. This, says Frisbie, "seems clear proof that they too are convinced of Compact performance, and is evidence that this [antenna] is inexpensive enough even for a small community application." The FAA division chief's statement was in reply to what he called false statements by Plessey lobbyist Lehrman that FAA tests showed that "overall static data on the Compact was disastrous."

Companies

## Norden, at 50, is feisty again

New emphasis on systems, focus on military work only, and exclusive minicomputer license lead to resurgence

by Bruce LeBoss, New York bureau manager

For Norden Systems Inc., life is beginning again at 50. The principal electronics subsidiary of United Technologies Corp., the once moribund firm is bursting with activity in its golden jubilee year. And as though to celebrate that anniversary, the former division and another subsidiary, Dynell Electronics Corp., have just been consolidated.

In Norwalk, Conn., Norden cut its teeth as a supplier of bombsights for U. S. military aircraft. Over the years it developed an expertise in air-to-ground radar and airborne displays and became one of the largest U. S. defense contractors. By 1972, the firm had about 3,400 employees and an estimated \$100 million in revenues, mostly from major contracts for the F-111D fighter's displays and C-5A transport's radar, as well as the A-6E all-weather attack plane's radar. How-

ever, the next few years were lean. Norden's major production programs tapered off, efforts to pick up commercial business bore little fruit, and employment tumbled to 900 by 1975. That was when Peter L. Scott came on the scene as president, and the firm has been ascending ever since.

"Soon after I arrived, it became obvious to me that the division's capabilities are oriented to the military market," says Scott. Thus, he decided it would "go military all the way." This meant redirecting some management talent that had diversified toward the commercial market and pruning several operations, such as selling Terminal Communications Inc., a \$30 million firm.

Scott's second key decision was to change Norden from a product- to a systems-oriented company. "Practically all of our past work involved

data gathering and processing. Thus, it was a logical extension of our innate skills to enter the military minicomputer field."

To get into that business, the firm had two options: either develop its own standard computer or license technology from an existing minicomputer maker. It chose licensing. Says Scott, "We won, competing against some very big names, a license agreement from the world's best-known and largest manufacturer of minicomputers, Digital Equipment Corp."

In February 1976, DEC licensed Norden to militarize, make, and market its small but highly successful commercial PDP-11 family. Nine months later, Norden introduced its initial offering, the middle-of-the-line PDP-11/34M [*Electronics*, Nov. 25, 1976, p. 50]. It has since expanded the line with militarized versions of the LSI-11 single-board micro-computer and high-end PDP-11/70.

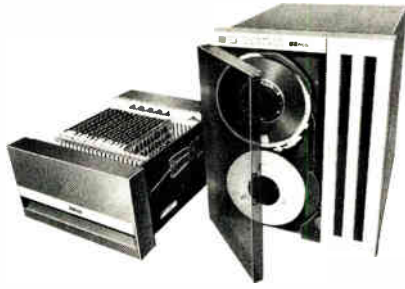
**New areas.** The military computer was the key to Scott's overall plan to broaden its basic product line, which had been quite narrow. For starters, he found two new growth areas, automated battlefield systems and shipboard surveillance and fire-control system. He also expanded the scope of the firm's airborne weapons delivery systems.

In its pursuit of automated-battlefield-systems business, Norden licensed technology from Marconi Space and Defence Systems Ltd. of England. With it, the firm won a



**Pilot.** Norden's president since 1975, Peter L. Scott (right) had been a vice president of NCR Corp. He is shown with Harold L. Ergott, vice president for computer products.





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## Probing the news

\$6.2 million contract to develop the microprocessor-based Battery Computer System for the Army [*Electronics*, Oct. 14, 1976, p. 77]. The BCS is an artillery computer for individual gun batteries.

The firm was selected over Litton last fall to supply the fire-control system for Vought Corp.'s version of the U. S. Army's General Support Rocket System. Vought and Norden are pitted against a Boeing-Teledyne team in a competition to develop the rapid-fire artillery rocket system. The Army will pick one team to produce the system, scheduled to enter service in the early 1980s. The total program could be worth upwards of \$1 billion.

Perhaps equally successful is Norden's thrust into shipboard systems. Norden first won a few contracts to supply modification kits that increase the display capability of radars used on U. S. Navy ships. It then competed against IBM, Sperry Univac, Litton, Hughes, and others and was chosen by the Applied Physics Laboratory of Johns Hopkins University to develop a system to computerize the radars of Navy combat vessels.

**All ahead full.** Meanwhile, the firm is pushing to win additional shipboard business. Last fall, the Navy awarded it a \$2.3 million contract to develop a new radar system that will be based on standard electronic module technology. More recently, Norden teamed with GE's Electronic Systems division and Dynell Electronics for studies leading to development of a new generation of radar systems for Navy ships.

In airborne weapons delivery, the firm is developing a radar-guided weapons systems. This development represents an expansion of airborne activities beyond the traditional radar and displays.

Apparently, Scott saw something he liked when surveying Dynell, a maker of shipboard radar systems. He subsequently brokered United Technologies' purchase of Dynell, in Melville, N. Y., for about \$21 million in cash. It will add about \$25 million to Norden's estimated \$50 million in 1977 sales. □

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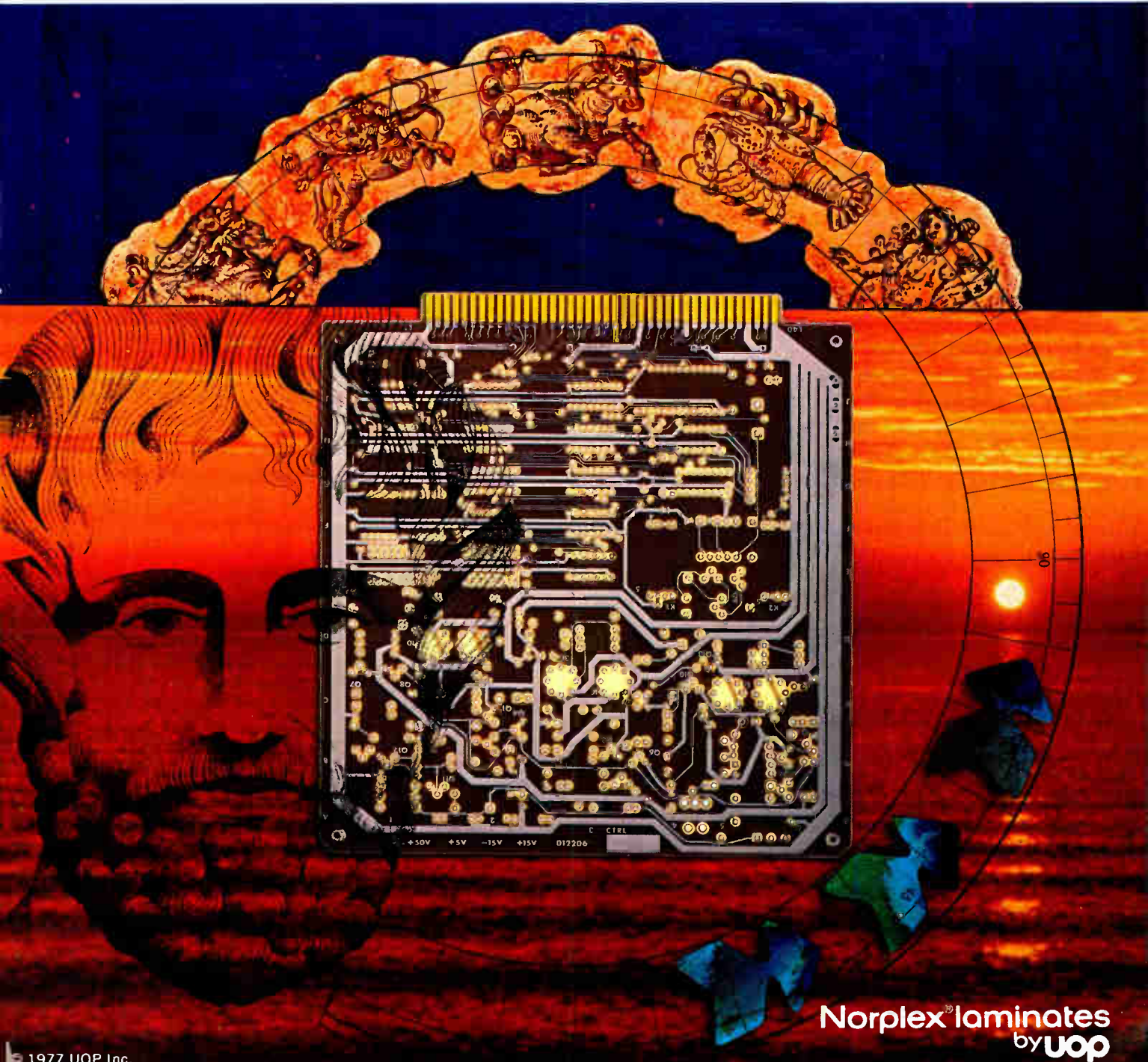
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Companies

# ITT cements Black Forest connection

With move of Semiconductor Group's headquarters to Freiburg other changes are being made to strengthen market position

by John Gosch, Frankfurt bureau manager

It seems odd for an American semiconductor producer to move its headquarters to Europe. But for the Semiconductor Group of the International Telephone and Telegraph Corp., the move at the beginning of this year from New York to Freiburg, West Germany, made sense. After all, as Heinz F. L. Roessle, group general manager for ITT Semiconductor worldwide, points out, the group's strength is primarily in Europe.

For the American firm, Europe has always been the place where most of the action is. In some countries, its share of the integrated circuits market is as high as 15%. In West Germany, Freiburg-based Intermetall GmbH, the group's biggest facility, rates among the leading semiconductor producers. But back in the U. S., ITT Semiconductor is not even among the first 10.

Also testifying to the group's strength in Europe are sales and employment figures. Of total sales estimated at \$155 million last year, Europe accounted for about \$120 million, and Intermetall alone for some \$100 million. About 3,000 persons of the group's 3,500 employees are in Europe, 2,000 of them at Intermetall. So with Intermetall the biggest—and most profitable—facility, Freiburg, a quiet cathedral town on the southern fringes of the Black Forest, was the logical site for the group's headquarters.

**Aiming high.** Now that the move has been completed, Roessle's long-range goal is to push ITT Semiconductor from being an average performer to a position "among the world's top five semiconductor producers." His near-term target is an

annual growth rate of about 20%, which is better than the predicted industry average. That would lift the group's sales from last year's \$155 million to almost \$400 million within the next five years.

To reach that goal, Roessle and his management team are revising the group's product mix, investments, and sales and marketing activities. Basically, though, the group's three major manufacturing centers—Lawrence, Mass., and Footscray, England, as well as Freiburg—will continue to produce the devices most in demand in their respective market areas.

At Lawrence, the mainstay will still be discrete devices, for years a

**Boss at Freiburg.** Heinz Roessle, who heads ITT Semiconductor, wants to push it into position among the world's top five.



profitable activity there because of the big commercial and military markets in the U. S. At Footscray, the emphasis will be on memories, because of the expertise the British facility has gained in producing circuits for Britain's strong computer industry. At Freiburg, the accent will continue to be on consumer devices to cash in on Western Europe's and especially West Germany's, lucrative and expanding entertainment and consumer electronics markets.

But some product lines will be contracted, or even abandoned, while others will be expanded. Commodity transistor-transistor-logic families, long an unprofitable activity that finally led to the demise of ITT Semiconductor's operation in West Palm Beach, Fla., last year, will be discontinued. On the other hand, "we will expand the power sector in Lawrence and will also do more in transistors there," says Roessle.

**Additions.** To be added to the U. S. facility's line of diodes, rectifiers, triacs, and thyristors will be power transistors and more triac families to toughen ITT's stance in the power marketplace. The power transistors will be n-channel and p-channel devices fabricated with V-channel metal-oxide-semiconductor technology.

With a wider range of power devices and highly automated assembly lines to increase the Lawrence plant's output, Roessle is confident ITT can increase its share of the American market for discrettes. "We also want to penetrate deeper into the U. S. market for consumer integrated circuits," he says. As in the past, these circuits

will come from Freiburg. But eventually, Roessle hints, consumer integrated circuits, including large-scale types, may be produced in the U. S.

As for Footscray, accounting for the bulk of memory production is the 4,096-bit dynamic random-access memory, the ITT4027. While this device is already being marketed on a worldwide basis, production of the 16,384-bit ITT4416 RAM is starting, with first samples already available. Both devices use a state-of-the-art MOS process and second-source Mos-tek Corp.'s 4027 and 4116 memories. On the drawing boards are 65,536-bit RAMS of ITT's own design.

Roessle's plans for Intermetall call for maintaining its lead in consumer products. Claiming to be the largest manufacturer in Europe of consumer MOS ICs, Intermetall aims to produce about 10 million such circuits this year. The total number of bipolar as well as MOS consumer ICs targeted for 1978 is well over 50 million. For discrettes, Intermetall's production goal this year is 1.25 billion devices.

**Marketing changes.** Roessle's marketing world extends far beyond the areas bordering the Atlantic. "Japan is looking more and more attractive to us," he says. Because of the strong TV set production there, Japan "is the place for consumer ICs, and that's why we must direct our marketing thrust also toward that country." Roessle does not "exclude the possibility of eventually producing consumer circuits right in Japan if the situation calls for it."

All this will require "substantial investments in the future," he says. Earmarked this year for upgrading production lines, for new design and development labs, and for new production equipment is \$15 million, up 20% from last year.

The bulk of those investments will be at Intermetall. Now under construction is a \$3.5 million design lab with electron-beam lithography equipment for mask making, and a new factory for large-scale and very-large-scale integrated circuits that is equipped with machinery for processing 4-inch wafers

Assisting Roessle will be a number of executives who have come up through the ranks at various ITT companies in Germany, dubbed the Black Forest gang by their U. S. and

British colleagues. Roessle himself, at 48 a 30-year ITT veteran, will report to Douglas Stevenson, vice president, ITT-Europe, who recently received responsibility for ITT's worldwide electronics and industrial components activity, an activity that will account for more than \$1.7 billion this year.

A key figure at ITT Semiconductor will be Ljubomir "Lubo" Micic. Operating out of Freiburg, he will

serve as director of worldwide marketing and business development. In the U. S., the top ITT Semiconductor manager will be Gerald Bellis, director of discrete operations in Lawrence. Herbert Renner will continue as technical director worldwide, and Gerry Thomas as general manager of UK operations. As in the past, Robert Stasek, a native of Austria, heads ITT Semiconductor's facilities in continental Europe. □

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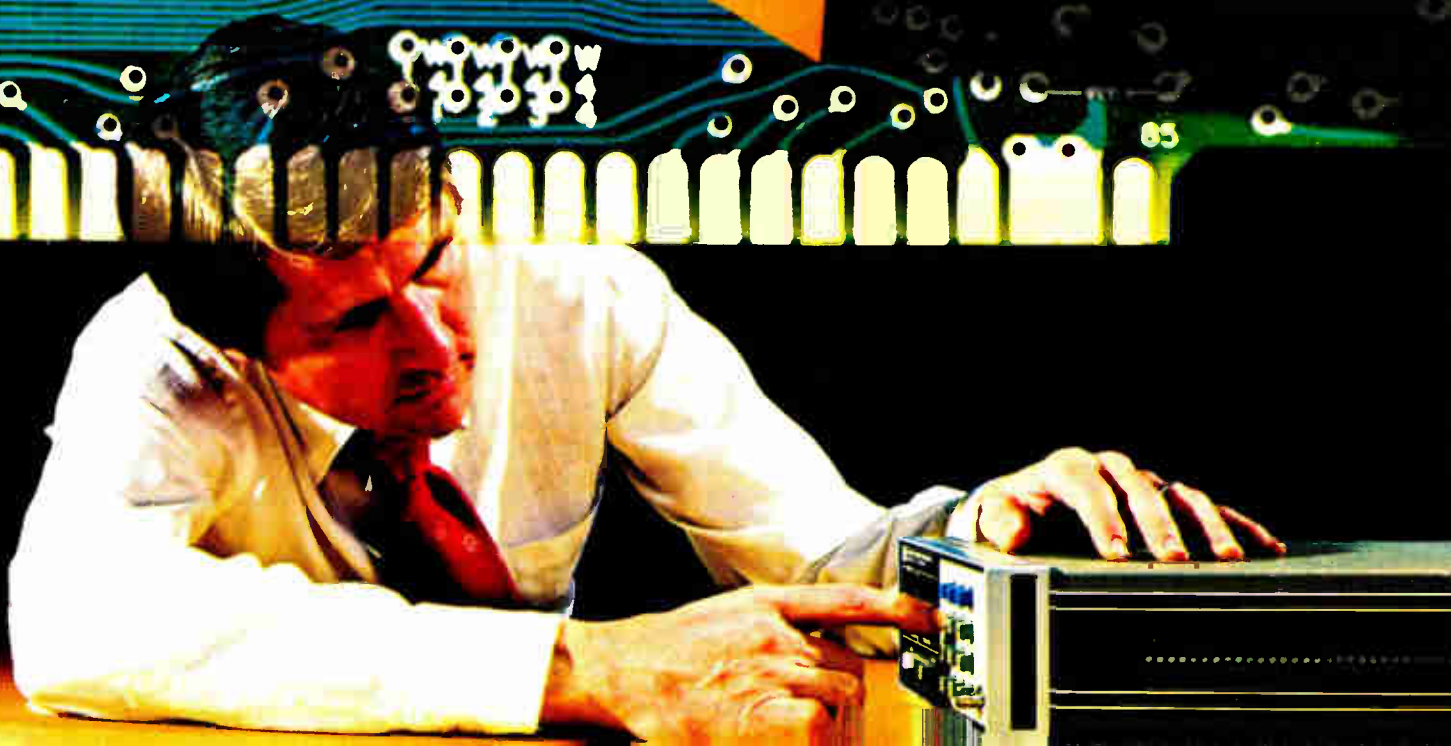
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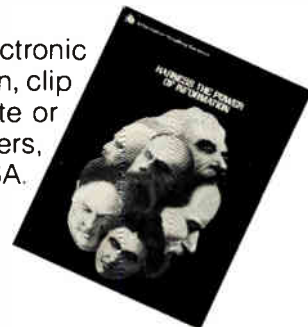
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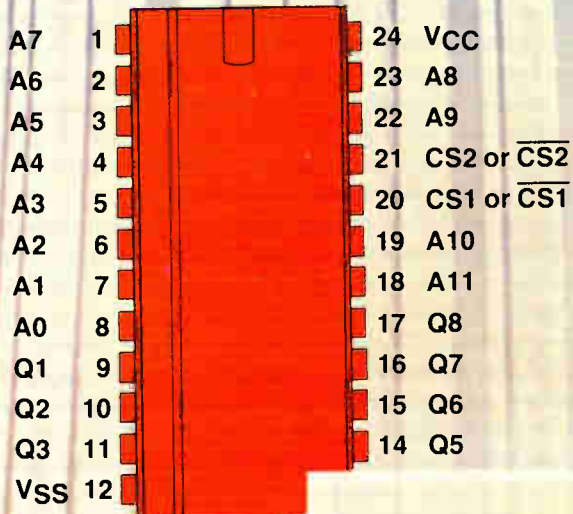
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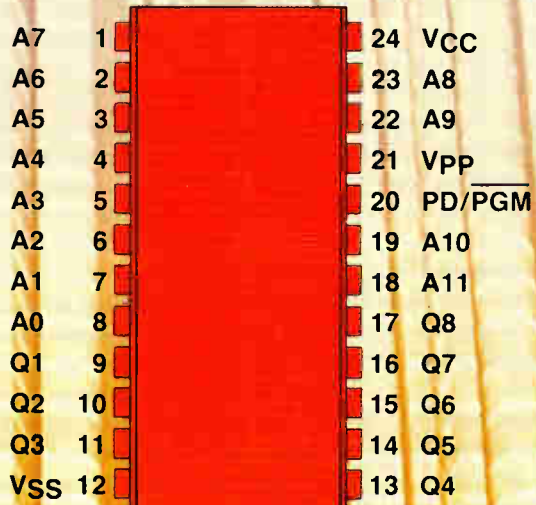
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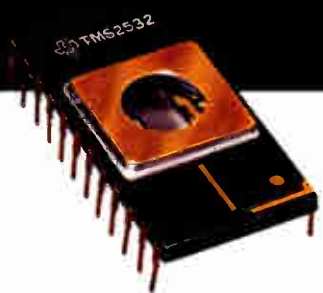
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### TMS 2532 32K EPROM



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With applications now demanding more and more memory in the same size space, the new TMS 2532 is both practical and economical. Because TI offers a plug-in 32K ROM for volume production. Because system upgrading is a snap—the TMS 2532 is pin-compatible with 8K and 16K 5-volt models.

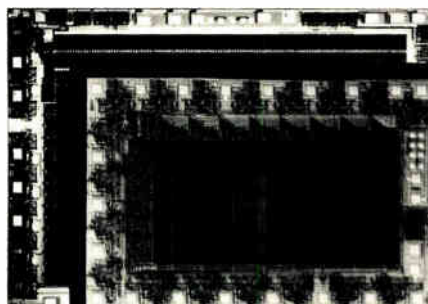
In addition, there is less assembly cost. Greater board density. Improved reliability. And, the TMS 2532 is a dollar saver compared to 8Ks and 16Ks.

### Easy programming

Designed for facilitating rapid program changes in high-density, fixed-memory applications, the new TMS 2532 features speedy programming. A single TTL level pulse is all that's needed for simple in-system programming.

Any location can be programmed in any order. Either individually, in blocks, or at random. Which cuts programming time to a minimum. Existing EPROM programmers can do the job.

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***MORE MEMORY CAPACITY** results from state-of-the-art design techniques that keep the TMS 2532 EPROM chip only slightly larger than an 8K chip (foreground).*

### Fully static operation

Like all EPROMs from TI, the new TMS 2532 continues the fully static tradition that makes designing much easier. There are no clocks. No timing signals. No hassles. Cycle time equals access time.

### Low-power operation

The TMS 2532 also sets new standards in energy saving. At 840 mW maximum power (worst case— $T_A = 0^\circ\text{C}$ ), it uses less power than a 2708. Yet has four times the memory capacity. And when the TMS 2532 is deselected, it automatically assumes a low power mode—50 mW typical.

### Matching 32K ROM

When programming is finalized and you're set for volume produc-

tion, you can readily switch over to TI's TMS 4732, a 32K mask-programmable, production-proven read-only memory.

It's a direct plug-in for the TMS 2532. Note on the illustration that they utilize practically identical pin configurations. In fact, when you order the TMS 4732, merely specify that Pin 20 be active low (CS1) and Pin 21 be active high (CS2) to achieve plug-in compatibility.

### Wide-choice EPROM family

With the addition of the TMS 2532, TI now offers you a broad selection of compatible EPROMs. All available in 24-pin packages. All having speeds of 450 ns. All sharing the same production-proven N-channel process. All having the same basic pin configuration. Which paves the way for increasing memory capacity in the future should your needs so dictate.

This wide-choice EPROM family includes the 8K TMS 2708, the low-power 8K TMS 27L08, and the cost-effective 16K TMS 2716 (see table below). And more members are on the way.

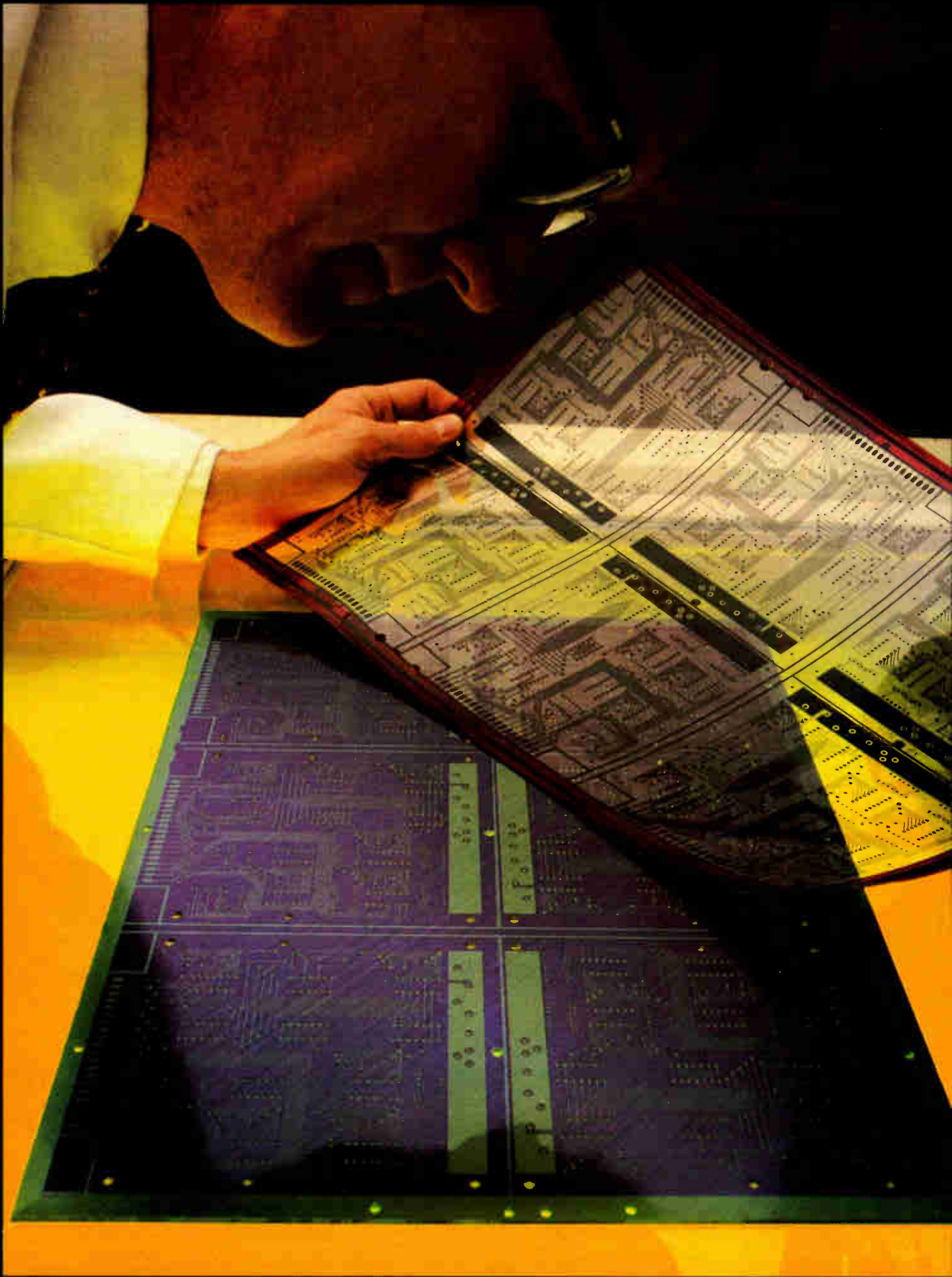
For additional information on the first 32K EPROM, as well as on other family members, write Texas Instruments Incorporated, P. O. Box 1443, M/S 669, Houston, Texas 77001.



## TI's Growing EPROM Family

Device	Complexity	Organization	Operating Supplies	No. of Pins
TMS 2708	8K	1K x 8	+12 V, $\pm 5$ V	24
TMS 27L08	8K	1K x 8	+12 V, $\pm 5$ V	24
TMS 2716	16K	2K x 8	+12 V, $\pm 5$ V	24
TMS 2532	32K	4K x 8	+5 V	24

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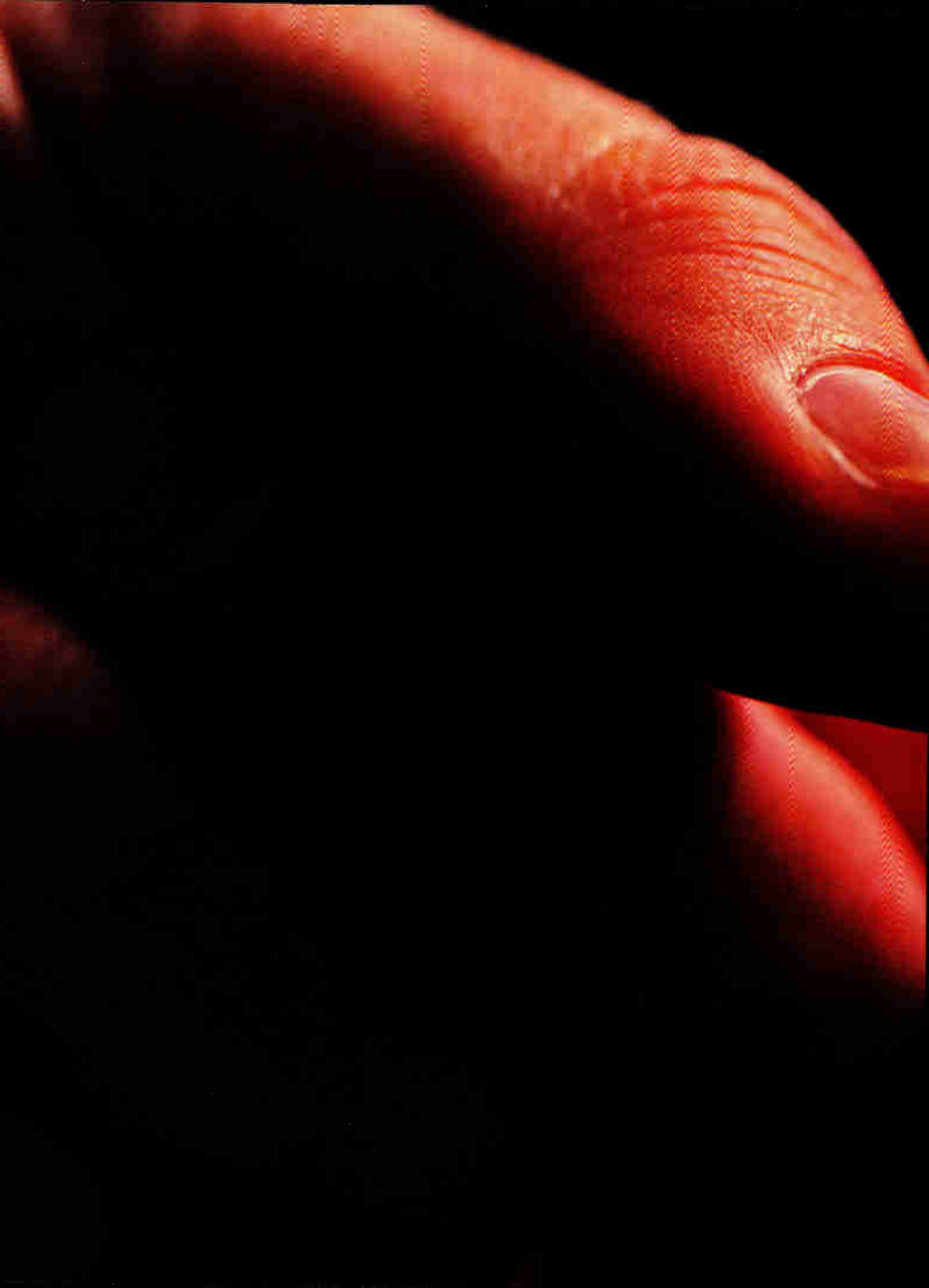
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# A sweeping statement about our Model 2002:



# Why and how users test microprocessors



by Stephen E. Scrupski, *Instrumentation Editor*

□ In electronics, as in everything else, tradeoffs are unavoidable. Thus, in the case of microprocessors, their inherent complexity allows them to replace boardfuls of hardwired logic, but also brings with it a problem that grows as usage increases: how to adequately test such complex devices before they are installed on a printed-circuit board.

Semiconductor manufacturers test all devices at least twice—at the wafer-probe stage, to weed out obviously bad devices, and at final testing, where the packaged devices are given more extensive checks (see “How semiconductor firms test,” p. 100). Nevertheless, significantly more than 1% and sometimes as much as 5% of incoming metal-oxide-semiconductor microprocessors fail the tests performed in users’ plants. For example, at Tektronix Inc., Beaverton, Ore., rejection rates run about 2% to 3%, according to Ted Olivarez, an engineer in the incoming inspection department. (For its tests, the department uses Tektronix’s own S-3260 computer-controlled system.)

Since the cost of troubleshooting a completed microprocessor-based board is estimated at from \$50 to \$75,

users who produce a significant number of them are being forced to confront a difficult testing process. In addition, they are faced with a choice among microprocessor testers that vary widely in price and capabilities.

### Testing problems

Microprocessors are far more difficult to test than semiconductor memories, themselves no easy testing chore. Memories are regularly structured devices and can be checked with a series of repetitive bit patterns, which are not difficult to generate. Microprocessors, on the other hand, are sequential-logic devices with complex internal structures and many internal data paths. Information is transferred back and forth within the chip from any of several locations to other locations under control of the microprocessor’s program. In actual operation, components and supplies will drift and, if certain timing paths are critical, force the device out of operation. Consequently, the timing of the various output signals, as well as all instructions, must be checked as the supply voltage is changed.

Moreover, the fact that a microprocessor works with



**1. Sentry.** The Sentry series of automatic testers from Fairchild Systems Technology includes computer control unit (background), programming stations (left and right), and multipin test heads (foreground). Shown is the latest in the series, the Sentry VIII.

one program does not necessarily mean that it will work with another, where, say, timing requirements on the input and output are more critical. Therefore, when a program is changed—for example, upgraded to redesign a product—the test program for the microprocessor must be similarly changed.

Further complicating the testing problem is the fact that, with second-sourcing, differences between similar parts from different manufacturers exist. It is worth noting that there are two types of second sources: those that use the same masks as the original or very similar ones, and those whose devices are only functionally similar and whose mask sets are significantly different. Differences have been found, for example, in the way flags are set and reset in 8080s from such suppliers as Intel Corp., Advanced Micro Devices Inc., and Nippon Electric Co. The test program, therefore, must take into account the source of the microprocessor.

Also, semiconductor makers regularly change designs and masks slightly to improve yield, and these modifications often cause functional changes that may appear as failures in incoming inspection. For this reason, most major users have begun to demand advance notice of any mask changes.

### Testing varies

The amount of testing performed on each device by semiconductor makers and users varies. The semiconductor firms, who claim to know their own devices better than anyone else, test each one with a series of test patterns typically about 1,000 clock cycles long. However, users have found that, typically, patterns up to 10 times longer are needed to fully weed out bad parts.

For example, a diagnostic program for the 8080 from Fairchild Systems Technology, San Jose, Calif., for its Sentry VII tester, is about 11,000 clock cycles long and exercises all of the 8080's 243 unique instructions with a total of 1,377 instruction tests. Some instructions are checked only once, because they are completely internal

to the chip, but others are exercised many times to check their effect on various flag bits.

The difference in volumes of devices handled by semiconductor makers and users contributes to the differences in test-sequence length. With each of thousands of devices going through final testing, it is obviously economically imperative for semiconductor makers to reduce the testing time of individual devices. Users, however, deal in much smaller volumes and thus can afford to perform more tests—in fact, they operate under a different economic imperative: avoid installing a marginal device that could fail in the field.

“Semiconductor manufacturers really don't do much testing, which puts a burden on the user,” says A. J. Strumar, director of product-assurance engineering for minisystems and terminal operations at Honeywell Information Systems Inc.'s Billerica, Mass. plant. “A good test typically takes between 15 and 30 seconds,” he continues, “and this limits the amount of testing a semiconductor maker can afford to do.”

Semiconductor firms test so as to present their parts in the best light and typically run a 1-second test on a device, says Richard McCaskill, product manager at Macrodata Inc., Woodland Hills, Calif. Some do not even run the full instruction program, he claims. In contrast, Macrodata runs tests of about 15 seconds for each device in its testing-service operation.

### What some users do

Honeywell, a major user of microprocessors, has made large investments in testers. According to Strumar, the company began using microprocessors with no incoming test program and ran into failure rates as high as 60% in an occasional lot. As a result, it bought several Fairchild Sentry VIIs to test incoming parts. Now it performs ac, dc, and functional tests on every device.

Despite experiences such as Honeywell's, it is nevertheless true that many low-volume users currently perform no incoming inspection on microprocessors.



Hewlett-Packard Co.'s Santa Clara (Calif.) division, for example, uses the 6800 in several new instruments but does not find it necessary to perform incoming tests. Instead, it simply plugs the device into the board and then tests the full board with a logic-board tester.

Full-board testing is also relied on at Racal-Dana Instruments Inc., in Irvine, Calif., for the 4004 microprocessor, which it uses in the series 9000 counter-timer. According to quality control manager Louis Lang, Racal-Dana has found that in fact the read-only memory chips fail more often than the central processing unit, and the volumes are low enough that they can afford to troubleshoot the whole board.

Before choosing a testing approach or a tester, users must decide whether testing is necessary at their own level of usage. If it is, a user may decide to engage a testing service to perform incoming inspection, rather than undertake its own testing. (The cost of such services generally runs about 50 to 75 cents per device.)

Users must test for dc, ac, and functional parameters. The first include such factors as leakage, output on-off impedance, and power dissipation, and three-state-logic characteristics. Ac and functional tests are then run for speed, instruction-processing characteristics, and so forth. At the same time, these tests must also check for pattern sensitivities.

### Pattern sensitivities

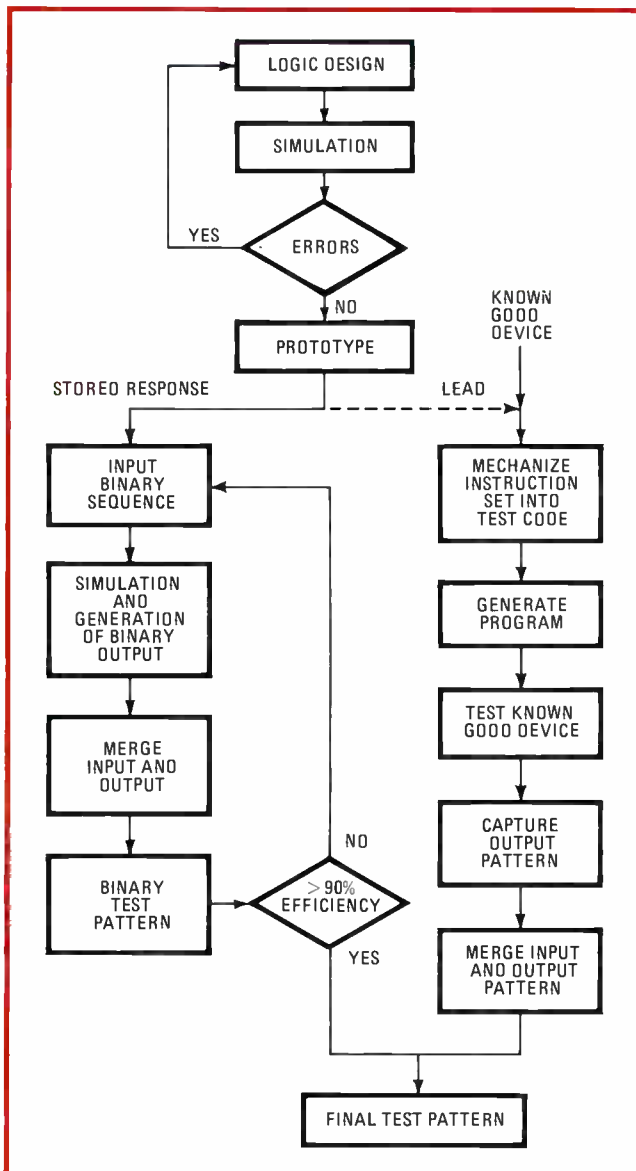
Sensitivities to input bit patterns, which are common in memories, also show up in microprocessors in the form of sensitivities to certain instruction sequences. Pattern sensitivities arise as a result of capacitive coupling paths and voltage drops. Since MOS microprocessors are dynamic devices—that is, charge is temporarily stored and nodes are precharged—certain sequences may not allow enough time to complete charge transferrals.

In a memory, the regularity of the structure allows some prediction of the worst-case sensitivities, whereas the microprocessor is so complex that such prediction is next to impossible. Therefore pattern sensitivities generally must be empirically discovered for each device and for each mask-set iteration.

Often they are discovered during systems tests, after the microprocessor has been installed on a board. When a system fails, troubleshooting procedures sometimes point to the microprocessor. If so, the device should be tested by itself with the same sequence of patterns used to test the full system. Then, the user must rewrite the incoming test program to include this sequence, in order to catch such sensitive devices before production. Alternatively, the design of the program may be changed, but this is rarely done because in most cases the program has already been written and debugged.

One of the major reasons for a microprocessor's failure is related to its speed. Setup and hold times on the data bus, for example, are often critical parameters. Marginal data setup times, relating to the circuit's ability to precharge internal nodes before the next clock pulse, may cause some devices to lose data.

Thus, there are three basic requirements for a tester: it should be able to generate pattern sequences; it should be able to vary electrical parameters, such as timing



**2. Test pattern development.** Test programs for Fairchild Sentry are developed in two basic ways at Rockwell Microelectronics: by computer simulation and by LEAD (learn, execute, and diagnose), which uses a known good device.

edges, logic levels, bias voltages, and loading, to permit worst-case testing; and it should be able to run tests at speeds equal to, greater than, or less than the actual system operating conditions.

### Four methods

There are four approaches or techniques used in testing microprocessors: in-system, comparison, algorithm-based, and stored-response testing. The first two are home-grown approaches sometimes employed by low-volume users. The last two, on the other hand, are techniques that are employed in commercial testers. A fifth approach, full-board testing with logic-board testers, is sometimes employed by low-volume users, as was mentioned earlier. Logic-board testers, however, are designed to check out complex, multicomponent assemblies as completed units; they are not best suited to

## How semiconductor firms test

Three groups are involved in microprocessor testing: the tester companies, the users, and the semiconductor manufacturers. Each has its own set of problems: tester makers are competing with one another for sales to the other two groups and thus are continually striving to improve testing technology; users recognize that inattention to device testing could mean costly in-plant repairs or even more costly field service calls; whereas semiconductor manufacturers want to maintain a reputation for reliable devices but also recognize that more tests on each device lengthen testing time and increase overhead costs.

The semiconductor manufacturer, as the source of the devices, is in the key position of the chain. The amount of testing that he does determines to a great extent the amount of testing that users will have to do. Therefore it is worth looking at how some typical semiconductor makers—Rockwell International's Electronics Devices division, Newport Beach, Calif.; Intel Corp., Santa Clara, Calif.; Motorola Semiconductor division, Austin, Texas; and Texas Instruments Inc., Houston—perform their tests on microprocessors.

Rockwell uses Fairchild Sentry VII's, as well as in-house testers, and the company is now evaluating the Megatest unit as a potential supplement to the Sentry systems in testing its larger-volume devices, such as the type 6500 microprocessor.

The test program used by Rockwell is typical of much of the industry. First, a continuity test detects devices with open pins and indicates the integrity of the tester's contacts. When operating with automatic handlers, the continuity test is repeated a number of times to allow for contact settling. The clock is then characterized for those microprocessors that have on-board clocks. Such characterization is necessary so that the tester may learn the clock timing in order to simulate the clock during functional testing.

Functional logic tests then are performed at the worst-case operating conditions—high voltage—low frequency and low voltage—high frequency. The tests are also guard-banded—specifications are tightened up to simulate testing at high temperatures.

A number of parametric tests are run, and a stress test is performed to promote reliability by accelerating the failure of weak devices. The test program provides instructions for automatic placement of parts in appropriate bins and also for data reduction.

Both the Megatest and the Sentry systems are used at Intel Corp. for production testing of microprocessor chip families. Intel owns eight Sentries, which it uses to characterize all new devices and to serve as production testers for about the first year of each new device's production life. It then shifts over to Megatest Q8000 units for production tests. Intel has about 20 Q8000s, using them for all stages of production, including wafer sorting and final testing of packaged devices.

Motorola Semiconductor also has several Sentry units for final testing of its 6800 family and is considering using the Megatest in wafer-probe testing. Manager of micro-computer testing Fred Toewe says he is yet to be convinced that a dedicated bench-top tester can perform full worst-case tests without in some way compromising accuracy, in contrast with a Sentry. Therefore, Toewe says, the Sentry will still be used for final tests.

With the Sentry, Motorola performs full testing to guar-

antee ac, dc, and functional specifications. However, Toewe notes that it is almost impossible to write a test program that guarantees that 100% of the nodes within a device have been checked for a stuck-at-1 or a stuck-at-0 fault. Test programs aimed at exercising a device fully are written by Motorola device designers, based on their familiarity with a device. The inputs are run through a computer that simulates the device and generates the expected outputs from the inputs set up by the device designers. The output responses are then stored in the Sentry for comparison during testing.

In the lifetime of the 6800, there have been two basic pattern-generation efforts. The first resulted in a pattern about 1,300 test cycles long, which was used for two years, with two or three touch-ups during that time. Motorola then made a new effort and shortened the test time to 850 cycles, while maintaining the same level of testing integrity. Two additions to the second effort were made subsequently.

With the 6800 specified to operate at any clock frequency between 100 kilohertz and 1 megahertz, the 850 cycles thus can take anywhere from 850 microseconds to 8.5 milliseconds. However, Toewe says, each device is actually in the test socket for much longer than that—about 2 to 3 seconds—since tests are repeated: each device is checked above and below the frequency range to ensure guard bands and is also checked at different voltages and with different waveforms.

Texas Instruments tests its 16-bit 9900 microprocessors with internally built testers but uses the Tektronix S-3260 for engineering evaluation of new devices in the family. Test patterns are developed by the designers and, as at Motorola, fed through a computer program that simulates the operation of each internal node of the device. According to TI's Roger Fisher, design and engineering manager for the 9900 series, the goal in designing the test patterns is to reach between 90% and 95% of the nodes that may be stuck at 1 or 0.

More than 10,000 test patterns are applied to each device. In wafer probing, the device is usually tested at a single voltage, whereas in final tests the patterns are repeated at several different voltages and at all timing specifications. Although the device is characterized on the Tektronix system and then tested on an internal TI system, the correlation between the two tests is better than 1%, according to Fisher.

For its TMS1000, a 4-bit controller-type microprocessor with on-chip read-only and random-access memory, TI uses its own testers. The testers are similar to the Sentry, according to Robert McKenna, TI's product engineering manager for the TMS1000 line. Designated ATT-2 by TI, they are used at both wafer probe and final testing, spending up to about 10 to 12 seconds on each device. The goal is to exercise between 90% and 95% of the nodes, McKenna says.

Since the devices have on-chip ROMs, whose contents are specified by the users, each customer's device must be checked with different test patterns. To help develop the test programs on a fast-turnaround basis, TI uses the same computer-aided design routines that set up the ROM mask patterns to develop portions of the test program.

TI now is talking with manufacturers of commercial testers to come up with a similar, lower cost tester for users, to improve correlation.

testing individual devices on the board. (See "What about board testers?" p. 104.)

In in-system testing, the microprocessor is plugged into the full board, which is in turn installed in the final system, and the final system is then tested. This approach is probably the least expensive and requires no extensive software investment, since its logic sequences are exactly those encountered in system operation. However, it cannot classify devices and generally cannot diagnose failures, points out Herbert Thaler, senior systems designer at Adar Associates, Burlington, Mass., who discussed all four methods succinctly at last October's Semiconductor Test Symposium in Cherry Hill, N. J. Also, it can perform few tests at specification margins, and it cannot test for stress.

Although this approach simplifies testing, it does have pitfalls. Microprocessors, of course, are made by batch processing, and consequently their operating properties are statistically distributed among each batch. Since system voltages and other parameters will drift once the unit is in the field, an installed microprocessor that originally fell near the edge of the distribution curve may turn up a failure.

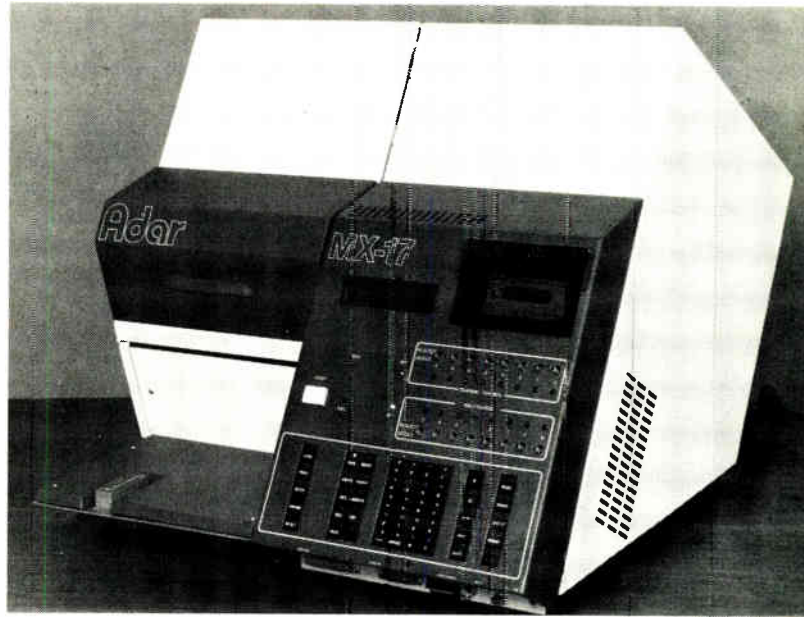
Also, in-system testing implies the use of a socket, rather than soldered connections. But the reliability of sockets is still questioned by many users. Vibration during shipping can easily loosen contacts on socketed packages, according to Honeywell's Strumar. "The main reason for using a socket in testing," he says, "is to make fault isolation easier. It's better to get smarter and be sure a device is good before inserting it."

Comparison testing, in its simplest form, consists of driving the reference and the device under test from a common source into fixed comparators. Programmable drivers and sensors can also be added. Both suffer, however, from the fact that the reference and the device under test share the same timing; consequently, any variations of parameters to which one wants to subject the device must also be applied to the reference, which means that the reference must be the best possible device of its type available.

### Commercial techniques

Algorithm-based testing reduces the device's operation to an algorithm, which is programmed into the tester's computer; the tester then uses the algorithm to calculate, or generate, the expected response from the inputs that are being applied. This technique has been highly successful in memory testing, since it offers the ability to generate logic sequences at high speeds and can be readily combined with variable parametric testing. However, it is difficult to program and requires detailed knowledge of both the device and the algorithm. But most important, it is simply not practicable for testing microprocessors, since an algorithm for such a complex device can only be developed at enormous expense.

In stored-response testing, a programmer determines the expected response from predetermined inputs and stores them, along with the inputs, in the tester's memory. The tester refers to its memory to pull out the inputs and feed them to the device being tested, and then to compare the test results with the stored responses.



**3. Bench-top tester.** The Adar Associates MX-17 tester uses a reference device as a source for the test pattern for the device under test. The tape cassette (upper right) is used to store programs and to change test conditions on line.

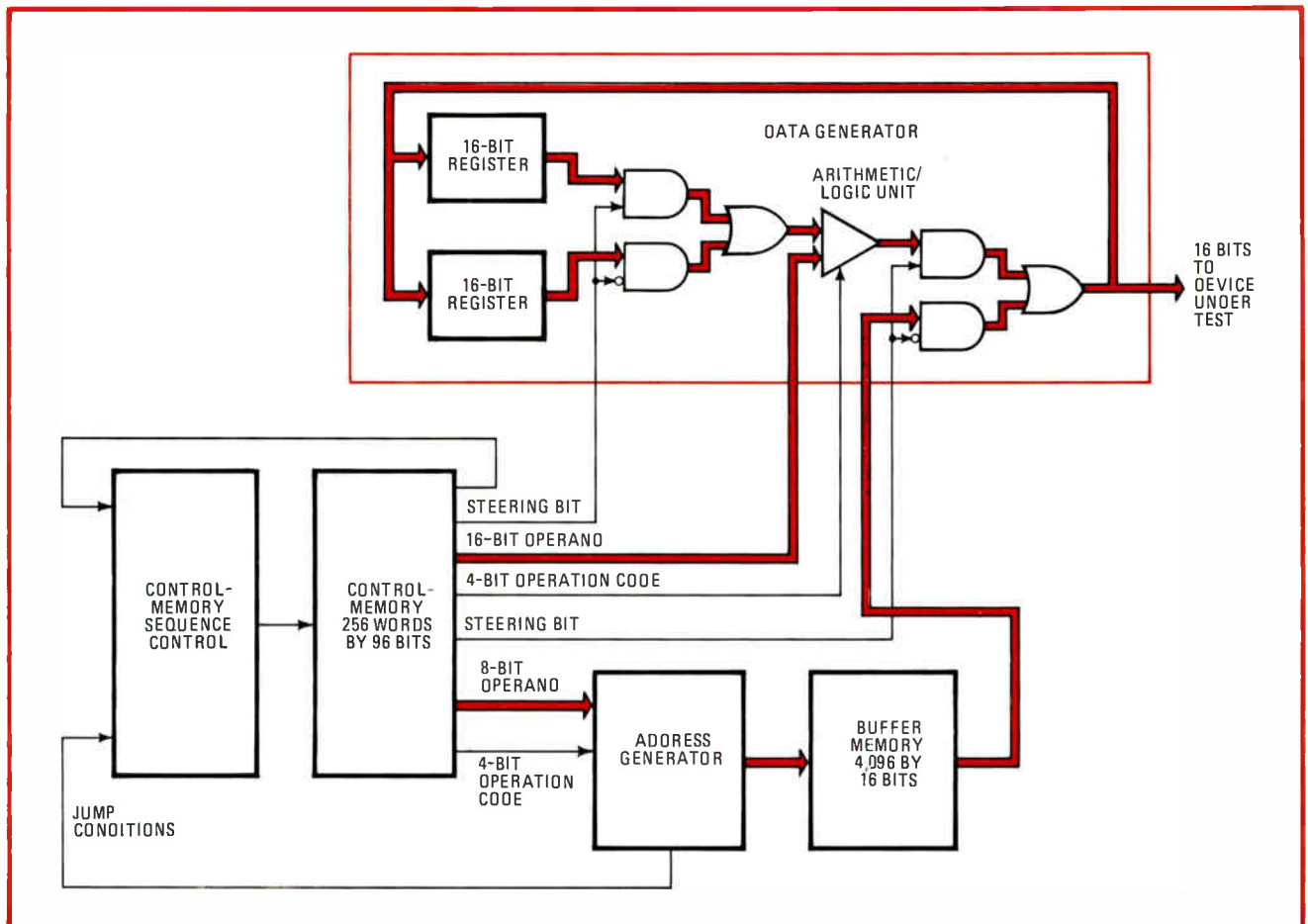
Conceptually, this technique is simple, but it is usually expensive in practice. To keep the storage buffer costs to a reasonable level, sophisticated software or hardware involving looping, semi-algorithmic subroutines, pattern partitioning, and other techniques are required. Most testers using this technique also require additional computer, disk, and related hardware.

### Testers: what is available

Most testers have been designed for the semiconductor manufacturer rather than for the user. The former needs the tester for a great deal of detailed device-characterization studies and to collect a lot of data to analyze production trends. Major users also characterize devices to monitor their suppliers, but many smaller users will simply want go/no-go tests made to their specifications for their own applications.

Until recently, commercial device testers were primarily large, expensive, computer-controlled systems. These large systems can be programmed to operate as either stored-response or semi-algorithmic testers. Because they are software-driven, they offer a great deal of flexibility in the tests they can perform, and because they are computer-controlled, they can collect and reduce massive amounts of data. But these advantages are reflected in their high cost—typically well above \$200,000. Lower-cost systems—\$100,000 or less—are also available; and even lower-cost bench-top test systems—starting at about \$30,000—are appearing. The bench-top testers require less programming, but they are much less flexible.

Semiconductor makers in particular have made considerable investments in computer-controlled testers, using the tester to characterize new devices as well as to test them during production, as was noted earlier. However, many of them are now examining more dedi-



**4. Pattern processor.** Micro Control's model M-10AT tester uses a pattern processor to generate complex data patterns. Control memory feeds operands and control functions to data generator and address generator, and arithmetic/logic unit generates final patterns.

cated testers that, although they lack the flexibility of computer-controlled systems, can do more specialized jobs well. Of course, because of the high volumes of similar devices that must be tested, such testers are particularly feasible in a semiconductor plant.

### The large systems

Fairchild's Sentry series of testers is generally acknowledged to be the most widely used large system in the U. S., having been introduced in time to take advantage of the boom in large-scale integration, although other large systems, such as the Tektronix S-3260 and the Macrodata MD-501, offer similar capability. Until a year ago, more Sentries had been installed by semiconductor manufacturers than by users, according to Richard Barr, director of marketing for the series. Now, he estimates that 40% of Sentry testers are in semiconductor plants, while users account for about 60%.

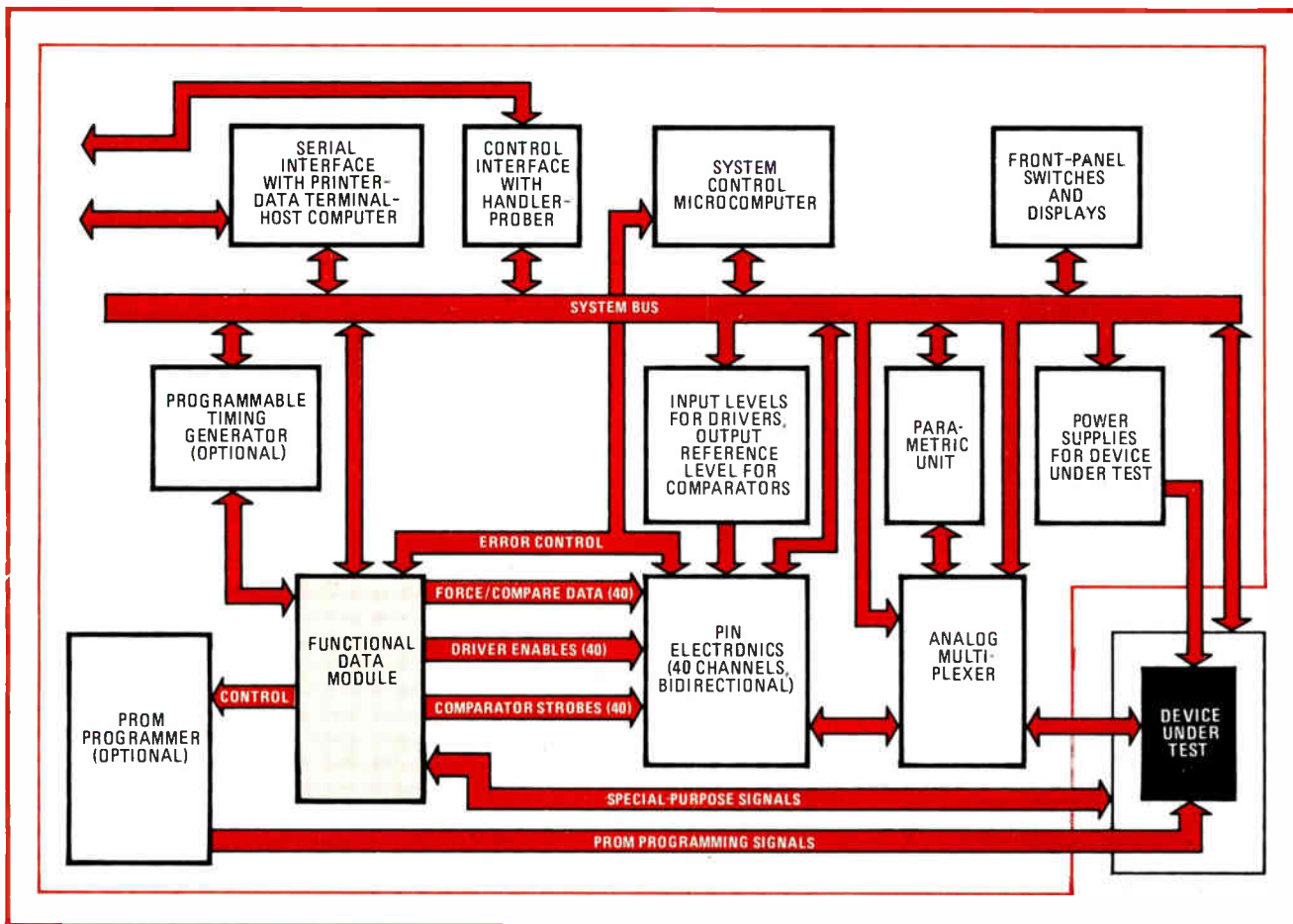
The latest system intended for microprocessors is the Sentry VII, introduced in September 1976. (The Sentry VIII, introduced in 1977, is basically an outgrowth of the Sentry VII with about twice the capacity. With its 120-pin testing capability, it is intended for very-large-scale integrated devices.) Cost starts at about \$200,000 and can run to more than \$400,000.

The Sentry VII is controlled by the company's own FST-2 24-bit minicomputer. It performs functional tests

by driving the microprocessor with inputs at rates up to 10 megahertz—sufficient for almost every microprocessor available today (about the only microprocessor with a faster rate is the Ferranti F100L, which runs at 15 MHz). It can handle up to 60 programmable pins on the test head, and each pin can be made to act as a 50-ohm data driver or output comparator, a clock input, a dc bias supply, a dc test output, or a bidirectional input-output pin. Thus, with a Sentry, a user can fully check out a device for its dc and ac performance and then its functionality, by having the computer vary the supply voltage and the timing of the input waveforms and analyze the effects on the outputs.

Although the Sentry has a large internal memory, long test patterns take up space in the disk memory, resulting in lost time when the smaller local memory must be reloaded from the disk. Fairchild uses two means to eliminate this problem. First, the Sentry computer runs in the direct-memory-access mode whenever data is transferred, which helps increase throughput. The real gain in speed in testing microprocessors, however, is with the Sentry's control sequence processor, which can execute subroutines that need be stored only once and can thus compress the test pattern needed to fully check out a microprocessor.

Other large systems have similar processors. (Tektronix calls its unit the pattern processor.) These units



**5. Low-cost tester.** Diagram of Megatest Q8000 (photo on p. 97), which is built around a functional data module, a duplicate of the device under test, that generates the test pattern. Various dc and ac parametric tests also can be performed.

generate the test patterns with a semi-algorithmic action. With the Sentry tester, compression ratios of approximately 3.5 : 1, for example, can be obtained for use with the 8080 microprocessor. Such a ratio allows the Sentry to store the test program totally within its 4-kilobyte high-speed memory.

The Tektronix S-3260, introduced about five years ago, runs at 20 MHz and can handle a total of 128 pins, with up to 64 inputs and 64 outputs. For each pin, it can have 1,024 bits of random-access memory and 1,024 bits of shift-register memory. The two memories are used with the pattern processor to compress data patterns—for example, a routine can be stored in the RAM, and data in the shift register. This saves storage space, since, as in the Sentry, instructions need only be stored once in the RAM and can be referenced over and over again by the pattern processor, whereas changeable data is loaded into the shift register.

Macrodata's MD501 is a computer-controlled tester selling for \$300,000 to \$450,000. The system operates at 10 MHz and can handle up to 64 fully programmable input-output channels. It uses a RAM buffer to serve as a control memory to generate test patterns algorithmically for the microprocessor under test. Macrodata's McCaskill notes that an 8080 can be subjected to about 1 million tests with less than 1,000 patterns stored in the RAM. The unit also has eight output strobes, which allow

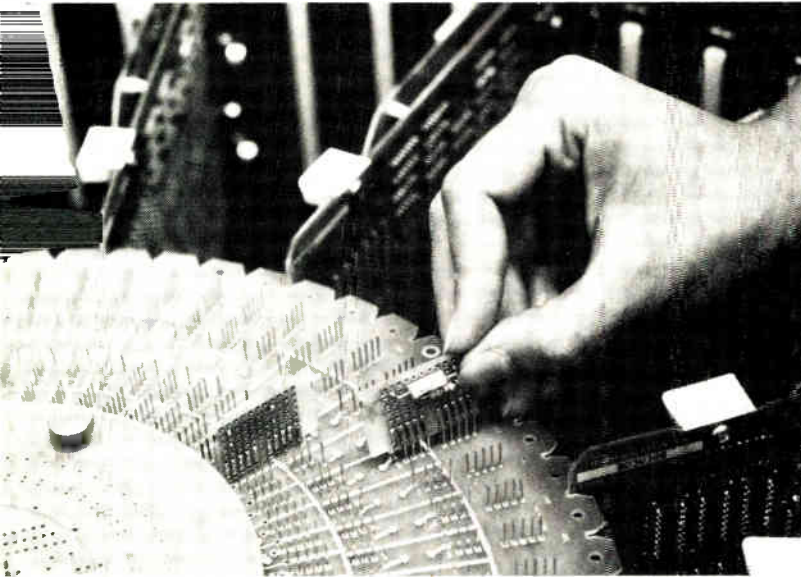
it to check complex devices with many different timing conditions on their outputs.

Macrodata also has a lower-priced system, the MD154, that is essentially a subset of the 501. Costing \$150,000 to \$250,000, it does not have the 501's universal pin electronics and full package of computer software, but it does have all other features.

A smaller system, the model M10A from Micro Control Inc., Minneapolis, may herald a new generation of microprocessor-based, lower-cost testers. The tester is built around the 8080 as its processor and generates algorithmic patterns at rates up to 10 MHz, with a floppy disk as mass memory. At less than \$100,000, it cannot be compared with the larger systems, since it requires changing the performance boards for each device to be tested, rather than being completely software-controlled, and does not have the full range of software offered by the larger systems. However, as with any programmed system, it can vary dc voltages, timing, and the like, under software control.

### Bench-top testers

At the lowest end of the equipment spectrum is the Q8000 from Megatest Corp., Sunnyvale, Calif. This bench-top tester uses a reference device, identical to the one under test, that acts as a dedicated pattern generator. The reference device eliminates the need to store the



**6. Test board.** Tektronix S-3269 automated test system can handle up to 64 input and 64 output pins on the device under test. Circuitry behind each pin is programmable to serve as supply, input, or output line. Shown is a portion of the test head.

input test patterns in memory or generate them algorithmically, as is done in the larger systems. Although this approach resembles the comparison method of testing, where a known good device is driven with the same input pattern as the device under test and the results compared, it differs in that the reference serves as the pattern generator.

With this approach, a program about 2.5 kilobytes long can generate a 1-million-clock-cycle test, which would require about 40 megabytes in a stored-response

### What about board testers?

Systems tests for logic-board assemblies containing such large-scale integrated components as microprocessors generally do not replace incoming inspection. However, logic-board testers cannot be ignored in the overall microprocessor testing question. If usage is small enough, such testers can be used to weed out bad devices at the same time that they check out the full board. But unless they have some automated diagnostic capability, the problem remains of troubleshooting the faulty board, which is a significant step up in complexity compared with a microprocessor.

Many of the considerations for microprocessor testers also apply to board testers. Board testers should be able to run at the rated speed of the microprocessor, and the test programs should fully exercise the microprocessor, as well as the surrounding circuitry. Preparation of such test programs is one of the most difficult aspects of using the testers, and tester manufacturers have invested extensively in software aids to help the test engineer.

Major manufacturers of logic-board testers aimed at microprocessor-based boards include Computer Automation Inc., Data Test Corp., Fluke/Trendar Corp., Genrad Co., Instrumentation Engineering, Membrain Ltd., Systron Donner Corp., and Teradyne Inc.

test, according to Megatest president Stephen Bisset. In addition, the device under test can be programmed in its own assembly language.

Megatest's approach, however, has one drawback: it requires a separate reference device, with associated circuitry, for each different device to be tested. Each circuit package, or functional data module, as Megatest calls it, costs \$3,000 to \$5,000, and thus the system's basic price of \$30,000 can quickly escalate if a large number of different devices are to be tested. Nevertheless, those users with a small mix of incoming devices, say, 10 different ones, can obtain a test system for significantly less than most computer-controlled testers.

Functional tests with the Q8000 are relatively simple. After it is written, the program is stored in a read-only memory, which is installed in the functional data module along with the duplicate reference microprocessor. The reference device is run one clock cycle ahead of the device being tested, and its inputs and outputs are latched so that its timing will be independent of the device under test. Therefore the reference device need not be a "gold standard"—a device known to be good under all conditions. If the reference device fails, Bisset notes, it will be evident from the resulting series of failure-condition indications for the device being tested.

The Adar Associates model MX-17, introduced in October and starting at \$37,500, is similar to Megatest's system in that it also uses a duplicate of the device under test to generate the test pattern for functional tests. Adar calls its approach "conditioned natural-environment testing," because the duplicate microprocessor generates the logic sequences in the natural environment—that is, the programming language—of the two devices.

Adar's tester, although similar to Megatest's, uses a cassette tape drive, rather than ROM storage, thus increasing programmability. Under program control, it can set up both bias, logic-level, and threshold voltages and timing conditions such as strobe and clock positions. Program control allows these parameters to be quickly changed on line, either from the keyboard or the cassette, or as a function of the test itself. Thus, in semiconductor production, the system can easily be used for sorting devices and also aids in data-logging the exact values of the results.

Software control also is used to set up test-program branch conditions, which tell the tester which program to proceed to after a failure. Similarly, the pattern sequence is software-loadable in RAM and can be modified on line. Adar also offers programmable interrupt signals that can be presented to the device under varied conditions, in varied sequences, and at varied times during an instruction cycle.

In the future, such low-cost testers will undoubtedly find their way into many users' incoming test departments, despite the decreased flexibility resulting from having to change the reference module for each different device to be tested. Such changes would be made infrequently in semiconductor plants, where, because of its low cost, the tester can be dedicated to a single device; and as more semiconductor manufacturers adopt these testers, users will have an added incentive to employ similar equipment, to help correlate test results. □

# Vertical geometry is boosting FETs into power uses at radio frequencies

V-channel field-effect transistor permits simple biasing, along with offering good thermal stability and linearity; nonplanar arrangement of device electrodes avoids parasitic capacitance in power applications

by Stephan Ludvik, *Communications Transistor Corp., San Carlos, Calif.*

□ A rapidly developing new technology is pushing field-effect transistors beyond their traditional low-power uses into power applications at radio frequencies, long the domain of bipolar transistors. Called V-FET or V-MOS, the new metal-oxide-semiconductor technology



employs vertical device geometries, rather than the planar structure commonly found in integrated circuits. This configuration boosts the output power of FETs beyond 100 watts at megahertz frequencies.

The power levels developed by the new V-channel FETs are the same order of magnitude as those of bipolar transistors with equivalent active areas. In fact, commercially available V-FET devices suitable for rf amplifier applications are now capable of producing a saturated output power in excess of 125 w with current-handling limits approaching 20 amperes.

At radio frequencies, V-FETs offer a number of attractive performance advantages. Because they draw virtually no dc input power, biasing schemes can be very simple. Also, they have no problems with thermal runaway, unlike bipolars which require careful ballasting and design layout. With increasing temperature, the transconductance of V-FETs decreases, because of the reduction in carrier mobility. Although this negative temperature coefficient provides thermal stability, it does theoretically limit the ultimate power capability.

Linearity is excellent, too, the result of the FET transfer characteristic that in most cases shows a square-law dependence. In fact, short-channel devices like V-FET structures have even more linear transfer functions because of the effects of velocity saturation in the conducting channel. Indeed, in single-sideband applications where good linearity is particularly crucial, the vertical-channel transistors have high-order intermodulation distortion products that are 5 to 10 decibels lower than those of bipolar transistors.

Since field-effect transistors are majority-carrier devices, they traditionally have offered better noise performance than bipolar transistors, particularly in low-power applications. This advantage over bipolars actually holds only at frequencies well above the

1/f noise region, which may be several megahertz. When 1/f noise is especially critical, probably the best choice for the active devices is junction FETs, rather than the insulated-gate versions such as V-FETs.

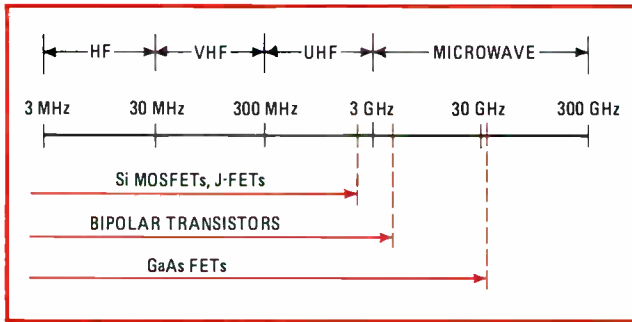
Although bipolars and V-FETs have similar output impedances, they differ substantially in input impedance. In some situations, the high input impedance of vertical-channel devices can mean relatively simple input matching. If the application involves octave or multi-octave bandwidths, their large input capacitance does present matching difficulties, although good amplifier performance can still be obtained. The table lists advantages and disadvantages of V-FETs in rf uses.

From a performance standpoint, the usable high-frequency limit (Fig. 1) of silicon FET devices such as the V-channel structures is probably in the range of 2 to 4 gigahertz. Beyond this, bipolar transistors and gallium-arsenide FET structures are the likely devices, with the transition from bipolars to GaAs FETs occurring somewhere between 8 and 10 GHz. In the overlapping frequency regions where more than one type of device may be applicable, the optimum choice is determined by such factors as cost, noise performance, reliability, and the like. In general, silicon power FETs are becoming commercially available in the high-frequency, very-high-frequency, and low ultra-high-frequency regions.

Making rf power V-FETs requires many of the processes common to standard MOS fabrication, in which the critical stage is forming the thin gate oxide and ensuring it is free from mobile ion contamination. This oxide, which lies along the sides of the V channel,

V-FET PERFORMANCE FEATURES

Advantages	Disadvantages
Good linearity	Gate-oxide damage at breakdown
Simple dc biasing	Threshold-voltage drift with contamination
High input impedance	High saturation voltage
Excellent thermal stability	High input capacitance
Low noise	



**1. Where V-FETs fit in.** The usable-frequency limit of silicon field-effect transistors such as V-FETs is probably 2 to 4 gigahertz. For higher frequencies, the likely devices are bipolar transistors and gallium-arsenide FETs, with the latter dominating above 8 to 10 GHz.

controls the current flow through the device.

In the vertical-channel structure (Fig. 2), two of the device electrodes are on the top surface, while the substrate acts as the third electrode. This nonplanar electrode arrangement permits the interconnection of large-area devices with less parasitic capacitance, thus making possible devices for power applications. Bipolar power transistors do not require special vertical structures, since their natural mode of current flow is vertical.

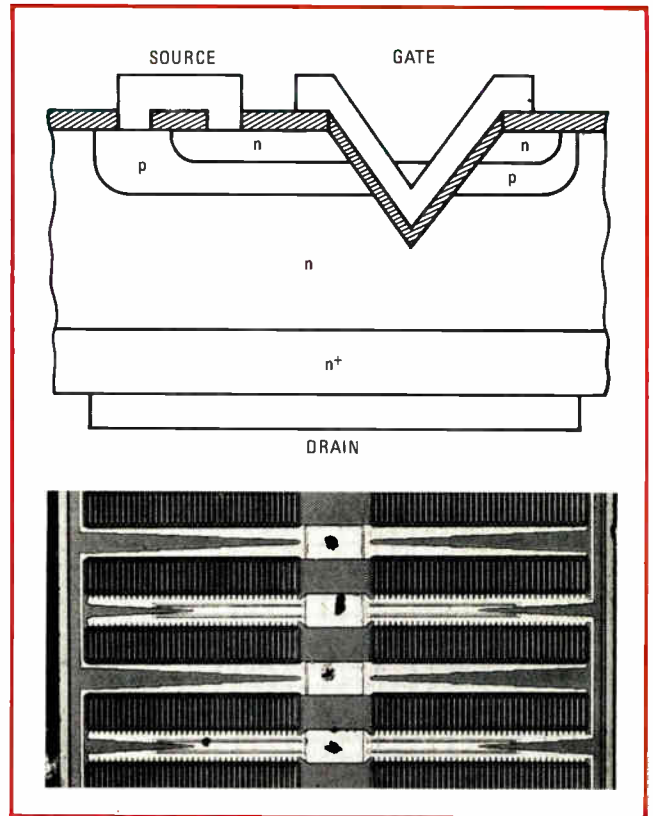
A key advantage of V-channel technology is that the frequency-determining element, the gate length, is fixed by a diffusion process, permitting easy realization of micrometer and even submicrometer gate lengths. In contrast, the critical dimension of most conventional surface-oriented FET devices is fixed by photolithographic processes in which 1- $\mu\text{m}$  dimensions are difficult to achieve over large wafer areas. However, lateral diffusion methods have reduced gate lengths in planar double-diffused MOS devices.

Preferential etching of silicon surfaces forms the vertical channel. This process is used extensively for making dielectrically isolated integrated circuits, as well as high-density memories built with v-MOS structures. Essentially, the horizontal dimension of the etch window and the angles between the crystallographic planes of silicon determine the shape of the groove. The singular advantage of preferential etching is that standard planar processing can be used to perform the gate metalization.

For reliable high-power FETs, another important consideration is the metalization scheme. The v-FET devices described here make use of an alloy metal system that employs copper doping to provide good electromigration characteristics and silicon doping to reduce the effects of aluminum-silicon dissolution. Such metalization systems have proved reliable in bipolar applications.

The photograph in Fig. 2 shows a portion of the chip for a 100-w 175-MHz v-FET having an overall die size of 80 by 173 mils. Since there is a transistor on either side of the V channel, the effective gate width is approximately twice the total gate contact length. Extra diodes, visible through the contact metalization, are placed between the source and the drain to improve device ruggedness. Additional diodes may also be connected to the input between gate and source to reduce vulnerability to static charge, which can damage the gate oxide.

Since a considerable body of design knowledge exists



**2. Inside look.** The V-FET's nonplanar electrode arrangement permits the interconnection of large-area devices with little parasitic capacitance. To improve ruggedness, extra diodes (visible through the contact metalization) are placed between source and drain.

for applications based on high-power bipolar transistors, it is convenient to transfer these techniques to designing with rf power FETs. For example, one parameter that can readily be estimated for class B or class C amplifier operation is load impedance ( $R_L$ ), which is largely determined by output power ( $P_o$ ) and supply voltage ( $V_{DD}$ ):

$$R_L = \frac{\eta(V_{DD} - V_{SAT})^2}{2P_o}$$

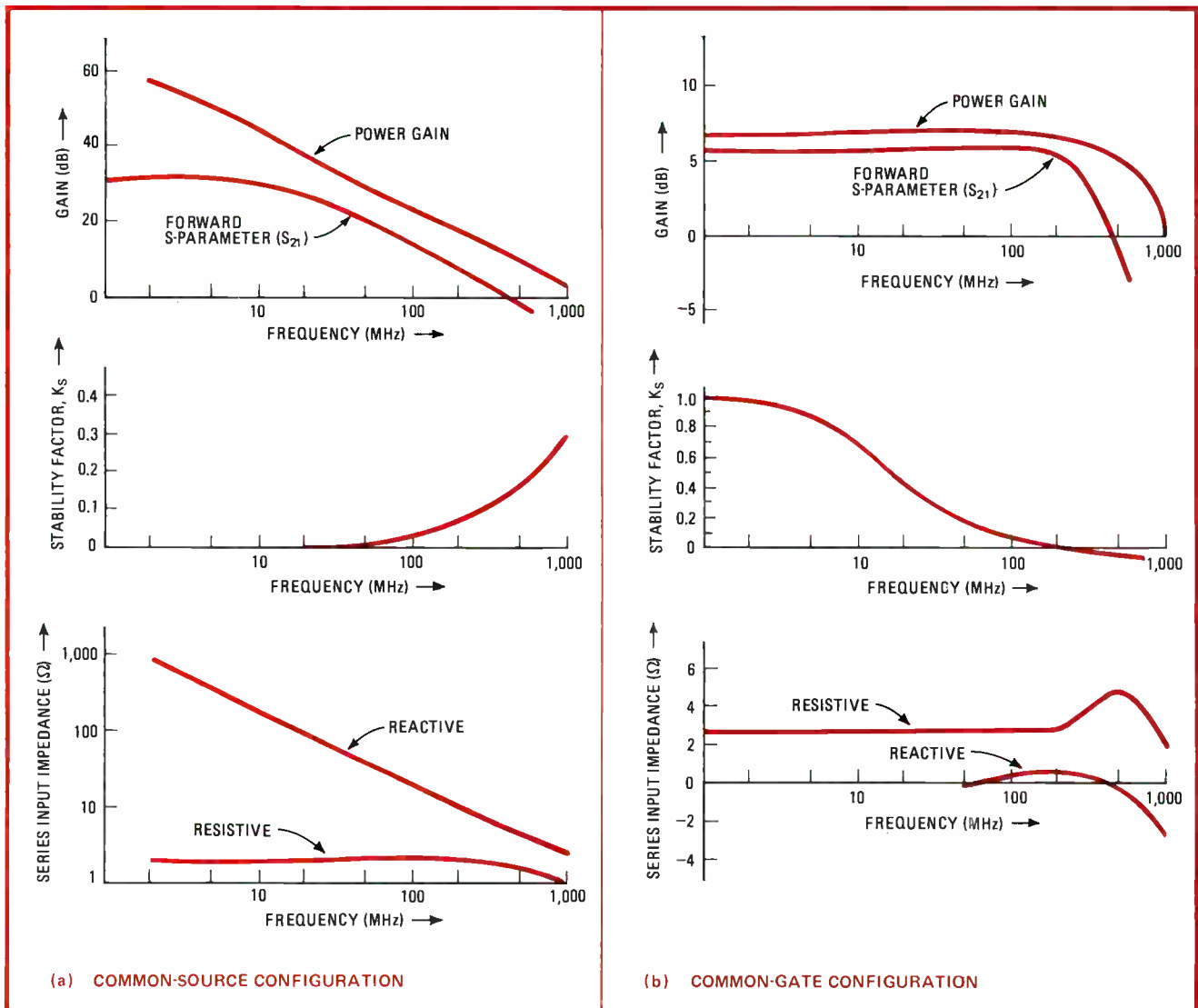
where the factor  $\eta$  depends on the saturation voltage ( $V_{SAT}$ ) of the device. This factor is typically 0.8 for bipolar transistors, but is 0.7 for FET devices because of their higher saturation voltage. For a 100-w vertical FET operating from a 28-volt supply, the value of  $R_L$  is approximately 2.7 ohms. Thus a parasitic series inductance as small as 4 nanohenries produces a reactance equal to  $R_L$  at about 109 MHz. Therefore, any series load inductance could influence device stability, quite apart from its effect on output matching.

### Common-source seems best

At this time, the common-source configuration seems to be the most useful for rf power FETs. The common-drain connection not only is more susceptible to unstable operation, but also requires special drive circuitry since its voltage gain is less than unity. On the other hand, common-gate operation has better stability characteristics than common-source, but its gain is lower.

Figure 3 compares the common-source (a) and





**3. Operating modes.** On the whole, the common-source configuration (a) seems to be the most useful for V-FETs, especially above 100 megahertz, where its stability is good. Below 100 MHz, common-gate biasing (b) is the more stable, and its input impedance is flat, too.

common-gate (b) configurations for a 25-W V-FET operating into a 12.5-Ω load. The most striking aspect of the common-source connection is its large impedance variation. The input reactive component changes by almost three orders of magnitude from 1 to 1,000 MHz. In contrast, the common-gate connection results in an input impedance that is fairly flat with frequency. Below 100 MHz, the common-gate configuration is the more stable; whereas the reverse is true at higher frequencies.

A couple of circuit examples will help to illustrate the use of V-FETs in rf amplifiers. The first circuit (Fig. 4) is an hf amplifier having an operating frequency of 30 to 88 MHz and developing a saturated power output of 125 W from a 28-V supply. The two V-FETs are housed in conventional rf packages.

Increasing the supply voltage to 45 V raises the output power to 250 W at the 1-dB compression point, with an efficiency of better than 50%. Although the common-source configuration used here results in poor input match, good gain flatness can still be obtained. Employing a combination of lumped-element and trans-

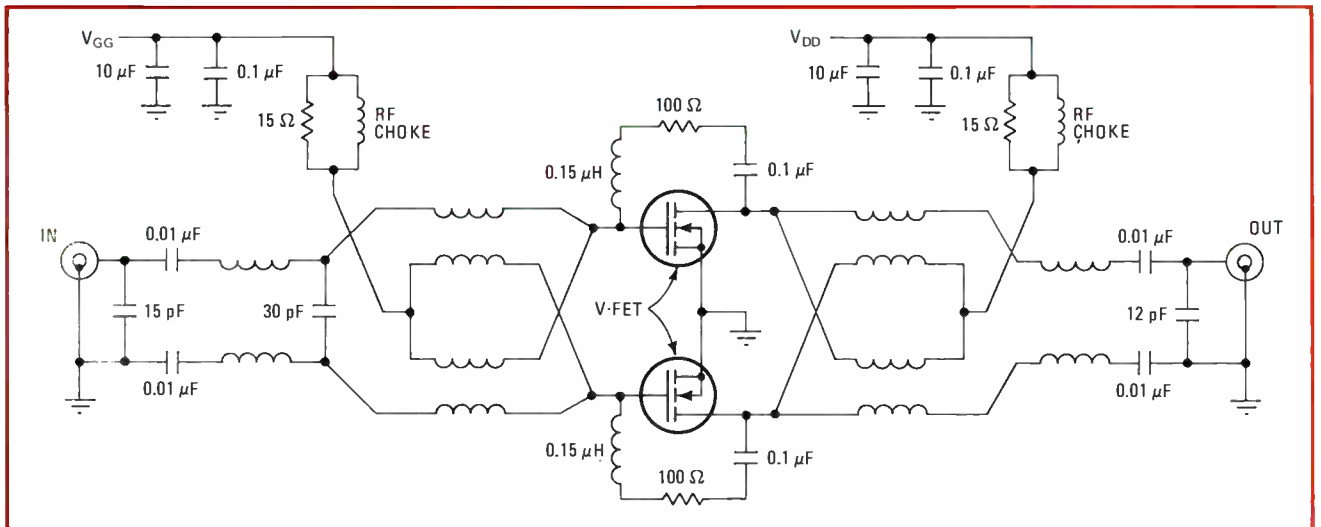
former matching networks should further improve matching and circuit performance.

The second circuit (Fig. 5) shows a vhf linear amplifier operating in the 170-to-230-MHz band used for European television systems. In this case, the V-FETs are mounted in a common-source configuration using a balanced package, which minimizes lead inductance. As with the hf amplifier, broadband transformers again provide input and output matching.

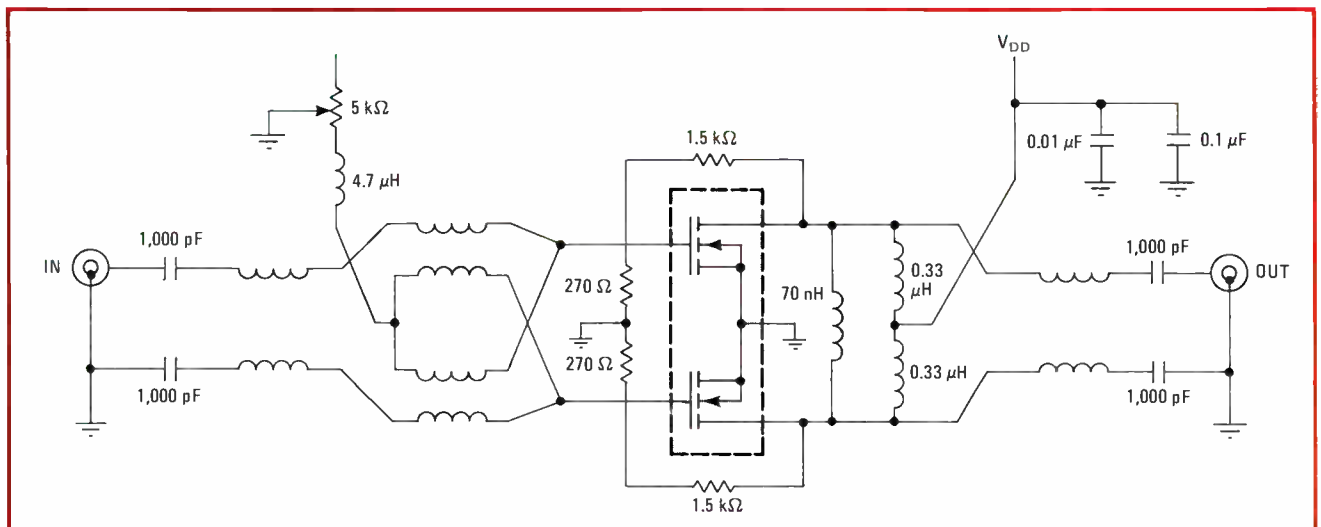
#### Return loss drops

In contrast to the circuit in Fig. 4 though, a lower input return loss can be obtained, since the reactive part of the V-FET input impedance is considerably reduced at vhf. At a power level of 16 W, this circuit's distortion is comparable to that of an amplifier built with the best available bipolar devices of a similar size.

Reliability data on rf V-FETs is still being gathered, but preliminary results from accelerated high-temperature life tests indicate that failure rates will be similar to those of bipolar transistors. At elevated temperatures of



**4. For hf.** Built with a pair of V-FETs housed in conventional rf packages, this amplifier delivers a saturated power output of 125 watts over a frequency range of 30 to 88 megahertz. The common-source connection results in poor input match, but gain flatness is good.



**5. For vhf.** Operating over 170 to 230 megahertz, this amplifier employs two V-FETs, connected in a common-source configuration and mounted in a balanced package to minimize lead inductance. For a 16-watt output, both distortion and input return loss remain low.

about 270°C, the V-channel devices have operated in excess of 1,000 hours with no catastrophic failures.

The observed degradation in performance is associated with the dissolution of the aluminum contact into the silicon surface, resulting in increased contact resistance and leakage from source to drain. (Identical contact-dissolution behavior holds for bipolar transistors with the same metallization scheme.) Electromigration phenomena appear to be of secondary importance, and they can be controlled by proper selection of the composition of the metal and by the adjustment of the cross-sectional area in the direction of electron flow.

#### Diode placement a key

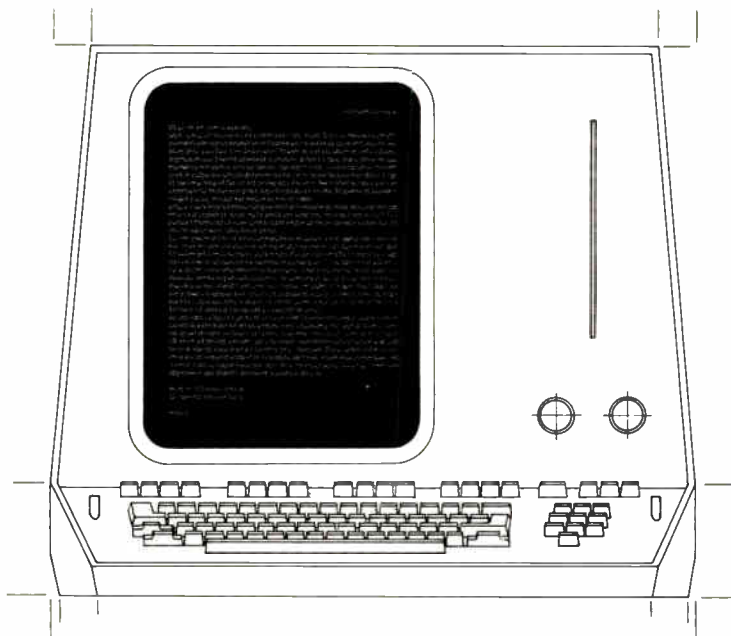
A problem unique to insulated-gate FET devices is breakdown and contamination of the thin gate oxide. As mentioned, placing input diodes between the gate and source reduces the vulnerability of this oxide to catastrophic breakdown. Also, careful process control can keep oxide contamination to a minimum, as well as

restrict drifts in threshold voltage to acceptable limits.

A short-term failure mode especially important for an rf device is its ability to withstand load mismatch, a capability often called VSWR (voltage-standing-wave-ratio) ruggedness. In circuits where oscillations are avoided during mismatch, V-FET amplifiers exhibit excellent ruggedness characteristics, primarily because of their thermal shutdown, which is due to the absence of secondary breakdown and decreasing transconductance with increasing temperature.

More precise data on the long-term performance of vertical-channel devices must still be compiled. But device lifetimes are likely to be quite good.

In sum, V-FETs are potentially important in rf power applications. Since they are relatively new, further development will undoubtedly make them a significant factor in such designs. As it stands, the availability of both FET and bipolar rf power devices gives engineers a wider range of active-device tools with which to improve circuit performance and simplify circuit design. □



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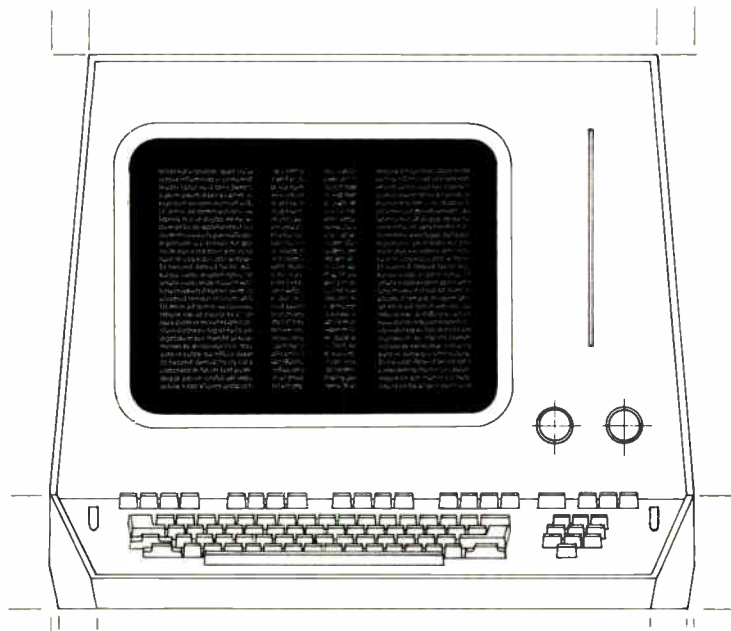
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## Programmed module automates transducer's linearization

by C. Viswanath  
Indian Institute of Science, Bangalore, India

As a consequence of its unusual transfer function, the Analog Devices 433 J/B programmable multifunction module finds wide use in performing vector operations, generating trigonometric functions, raising a number to an arbitrary power, and linearizing the response of transducers used in medical and industrial electronics.

The module's transfer function is:

$$e_o = \frac{10}{9} V_y \left( \frac{V_z}{V_x} \right)^m = P \quad 0.2 \leq m \leq 5.0$$

Programming of the exponent,  $m$ , contained in the transfer function, which is necessary to generate the required operations, is done more quickly and accurately with a digital-to-analog converter and two field-effect transistors than with a potentiometer, the component most often used. Digital selection of the exponent is particularly useful where an automatic test sequence must be generated from a microprocessor to multiplex several transducers, each requiring a different  $m$ . With this circuit, the value of  $m$  may be adjusted throughout the entire specified range, in increments of 0.1.

A circuit used for transducer linearization is shown in the figure. The technique used for linearizing a transducer's transfer function ( $Q$ ) is to control  $m$  so that it varies inversely with the known exponent ( $n$ ) contained within the transducer's characteristic equation. Thus, when the output voltage from the transducer  $(V_z)^n$  has been processed by the 433 J/B, the effects of  $m$  and  $n$  on the output voltage will cancel each other (as a result of multiplying  $P$  and  $Q$  to obtain  $e_o$ ), and the entire transfer function is then simply expressed by:

$$e_o = K V_z$$

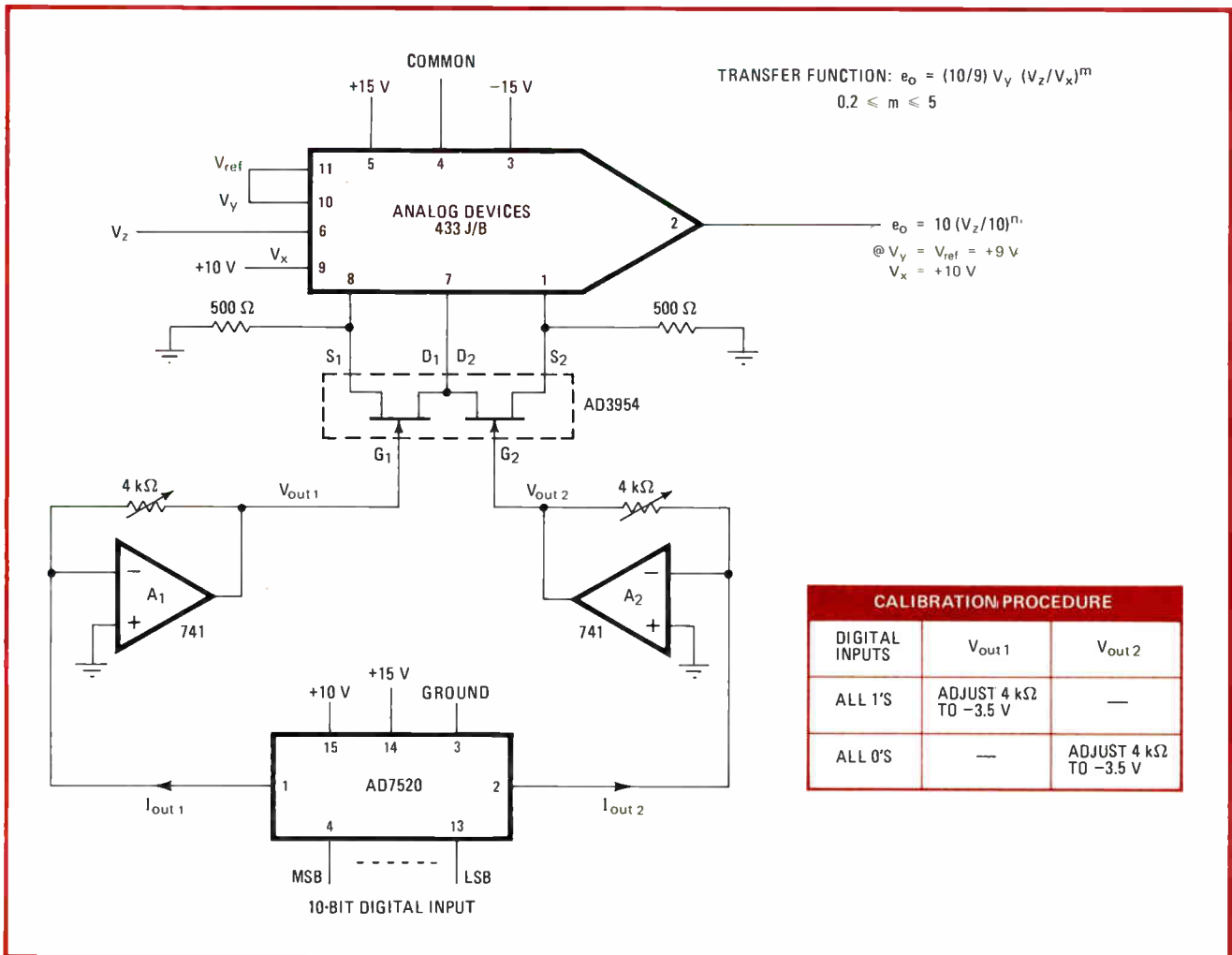
The value of  $m$  is programmed by controlling the resistance between pins 1, 7, and 8 of the 433 J/B by means of the AD3954 dual-FET stage and the 10-bit AD7520 d-a converter. The combination of the converter and the dual FETs is thus intended to serve as a digitally controlled potentiometer.

Two binary-weighted current sources, the magnitudes of which are dependent on the 10-bit input and the sum of which is constant (equal to  $I_{out1}$  plus  $I_{out2}$ ), drive operational amplifiers  $A_1$  and  $A_2$ . The magnitude of  $I_{out1}$  and  $I_{out2}$  are determined by the reference voltage at pin 15 of the converter.

$A_1$  and  $A_2$  convert the currents to voltages  $V_{out1}$  and  $V_{out2}$ , respectively, and drive the gates of the dual FET. The FETs operate as voltage-controlled resistors and are

PROGRAMMING OF EXPONENT M

M	DIGITAL INPUT	
	MSB	LSB
0.2	0000000000	
0.3	0000010100	
0.4	0000101010	
0.5	0001000000	
0.6	0001010100	
0.7	0001101010	
0.8	0010000000	
0.9	0010010100	
1.0	0010101010	
1.1	0011000000	
1.2	0011010100	
1.3	0011101010	
1.4	0100000000	
1.5	0100010100	
1.6	0100101010	
1.7	0101000000	
1.8	0101010100	
1.9	0101101010	
2.0	0110000000	
2.1	0110010100	
2.2	0110101000	
2.3	0111000000	
2.4	0111010100	
2.5	0111101010	
2.6	1000000000	
2.7	1000010100	
2.8	1000101010	
2.9	1001000000	
3.0	1001010100	
3.1	1001101010	
3.2	1010000000	
3.3	1010010100	
3.4	1010101010	
3.5	1011000000	
3.6	1011010100	
3.7	1011101010	
3.8	1100000000	
3.9	1100010100	
4.0	1100101010	
4.1	1101000000	
4.2	1101010100	
4.3	1101101010	
4.4	1110000000	
4.5	1110010100	
4.6	1110101010	
4.7	1111000000	
4.8	1111010100	
4.9	1111101010	
5.0	1111111111	



**Exponent programming.** Programming of constant  $m$  in 433 J/B's characteristic equation is quicker and more accurate with a d-a converter and FETs that operate as voltage-controlled resistors than with a potentiometer. This circuit linearizes the response of transducer voltage  $V_z$  if the 433 J/B is programmed so that  $m$  is the inverse of exponent value  $n$  contained in the transducer's transfer function.

selected to provide good tracking throughout the 0-to-3.5-volt input-voltage range.

If all 10 bits of the AD7520 are set to logic 1, corresponding to an  $m$  value of 5.0,  $I_{out1}$  will equal 1 milliamper, and  $I_{out2}$  will equal 0. Thus  $V_{out1}$  should be set to a full-scale output (-3.5 v), and  $V_{out2}$  should be

set to 0. Similarly,  $V_{out1}$  must be set to 0, and  $V_{out2}$  to -3.5 v, when all inputs are set to logic 0, corresponding to an  $m$  of 0.2. The 4-kilohm potentiometers are provided for calibration purposes.

The table outlines the inputs to the d-a converter required for any value of  $m$  from 0.2 to 5. □

## Dc-dc power supply has reference-unit stability

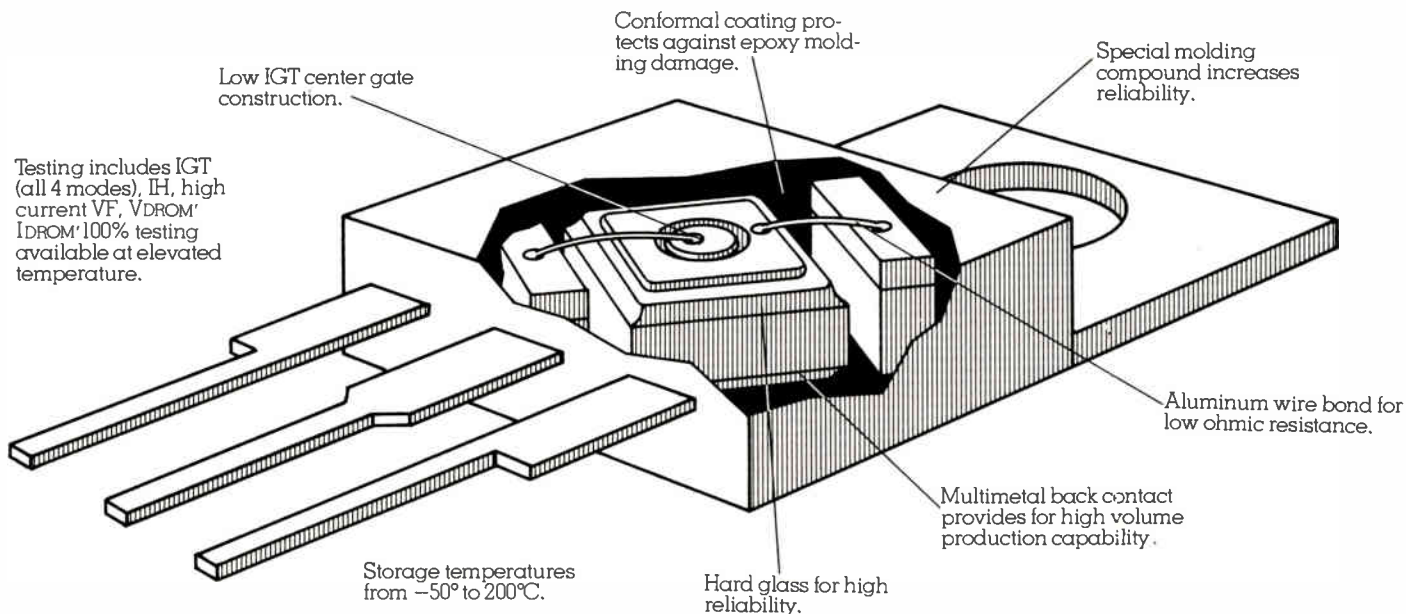
by J. Brian Dance  
North Worcestershire College, Worcs., England

The stability of the voltages generated by adjustable dc-dc power supplies is usually no greater than  $\pm 100$  millivolts, even when the voltages are derived from fixed-voltage regulators. In cases where extreme stability is sought, it is best to design a circuit that

utilizes a voltage-reference source instead. Such a circuit, shown in the figure, can provide a 0-to-20-volt output that is within  $\pm 5$  millivolts of the set value and virtually independent of the current drawn by the load. The supply delivers a maximum of about 1.5 amperes, has a built-in thermal shutdown safeguard, and is protected against short-circuit conditions.

The Precision Monolithics REF-01 voltage reference unit in the circuit provides an extremely stable 10 v across a 10-turn helical potentiometer,  $R_1$ , as shown in the figure. This pot, which has a calibrated vernier, sets the output voltage, which will always be equal to twice the value of any voltage derived from the reference source. The linearity of the potentiometer is 0.1%, and

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this ensures that the output voltage may be set to within a few millivolts of its desired value. For verniers with a scale of 0 to 10, the output voltage will be equal to twice the vernier reading once the entire circuit is calibrated.

$R_2$  is included in the circuit for trimming purposes. It is used to calibrate  $R_1$  at an output voltage of 10 v. If the gain-controlling elements in the circuit,  $R_3$  and  $R_4$ , are close-tolerance components, trimming may be neglected. If  $R_2$  is omitted, and  $R_3$  and  $R_4$  have a 5% tolerance, the voltage at pin 6 of the REF-01 will be within 50 mv of 10 v.

The slider arm of  $R_1$  drives the noninverting port of the LM358 operational amplifier, which operates in the linear region even though it uses only a single-source supply. The gain between the input of the op amp and the output of the circuit is equal to  $1 + (R_3/R_4)$ . Thus the voltage appearing at the output of the LM295K amplifier is twice the value of the voltage appearing at the input of the op amp; since the input voltage is a function of a stable reference, the output voltage is also stable.

The LM295K, although shown as a single transistor element in the figure, is actually a high-gain linear power amplifier. Its open-loop gain is 1 million, and it is capable of delivering a maximum of 1.5 A to the load.

$C_1$  and  $C_2$  are added to the circuit to ensure that power-line input-voltage glitches do not appear at the

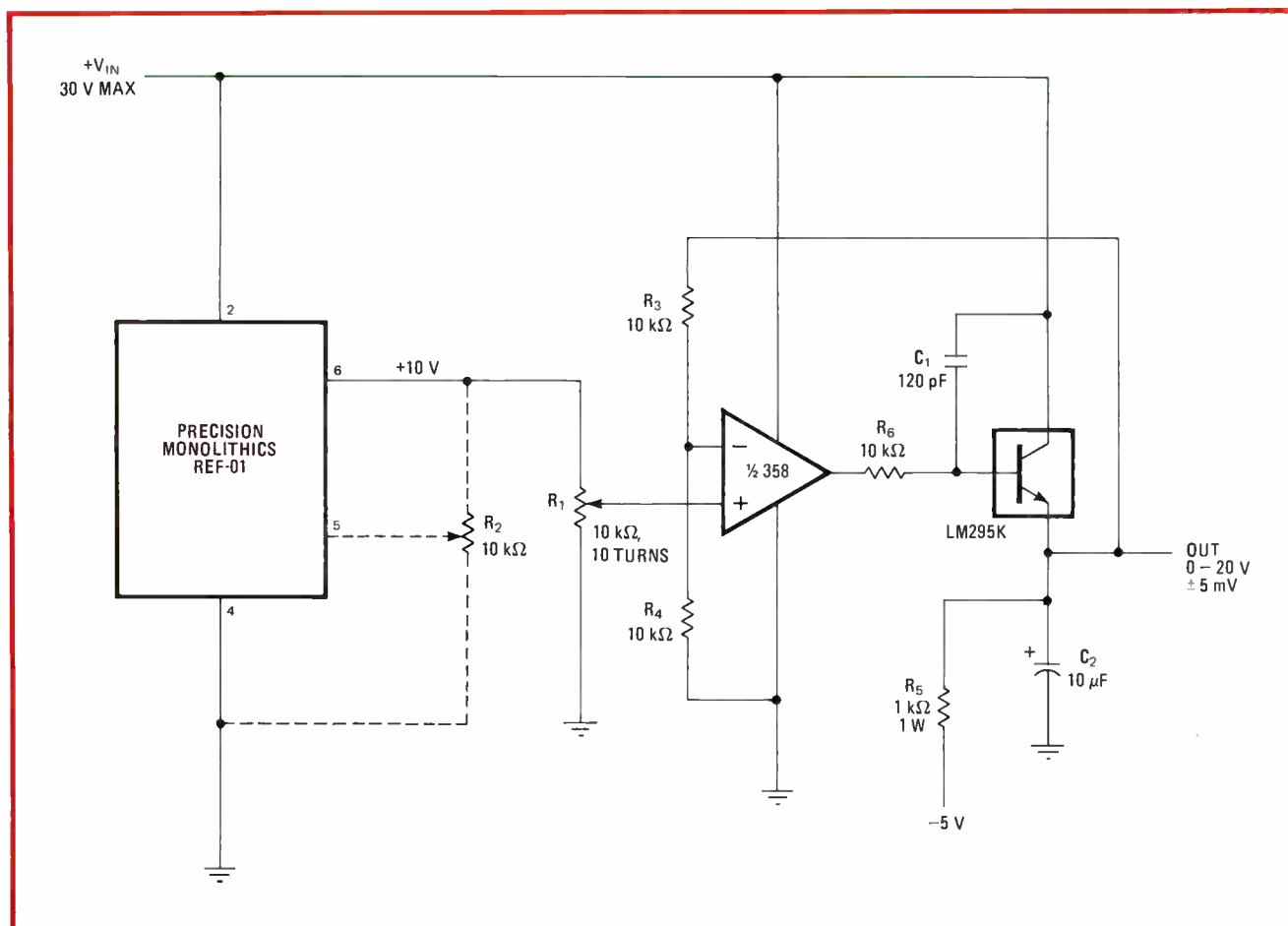
output or cause unwanted oscillations.  $R_5$  provides a path for the amplifier's quiescent current flow; if it is omitted, the output voltage will climb to 9 v at  $R_1$ 's minimum setting. The use of a  $-5$ -v bias supply can be avoided if  $R_5$  is connected to ground, but the minimum output voltage will rise to approximately the product of the quiescent current (5 mA maximum) and  $R_5$ .

The 358 amplifier operates in the linear region even if the voltage at the inverting port falls to zero. Most op amps, however, require bias from a dual supply (positive and negative voltages) in order to operate in the linear region, and this fact should be considered when contemplating the use of a different op amp.

A current of 1 A taken from the output port produces a voltage change of less than 1 mv. A change of 10 v on the power-line input voltage results in only a 10-mv change at the output, and this figure can be reduced even further by placing a suitable resistor in series with pin 2 of the REF-01 and the supply voltage and connecting a 15-v zener diode from pin 2 to ground.

The temperature stability of the circuit has not been measured, but, depending on the class of REF-01 used, it will lie in the range of 3 to 20 parts per million per °C. Output noise at very low frequencies is extremely small. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay \$50 for each item published.



**Precision.** Rock-stable voltage reference source enables generation of extremely stable output voltages. Current and voltage produced by REF-01 source is independent of load current demands; thus output voltage, once set, will not vary more than  $\pm 5$  millivolts.

# Easy impedance matching opens the digital door to analog delay lines

Widely available new models, designed for simple interfacing, can replace complex arrangements of logic gates; a few basic rules are the guide to practical implementation

by Larry Garde, *Magnetic Peripherals Inc., Minneapolis, Minn.*

□ A new breed of delay line is attracting digital designers, for the units are designed to minimize the interface impedance-matching considerations that proved so resistant to solution in earlier attempts at logic applications. Moreover, the new lines boast incremental tappings and come in the familiar 14- and 16-pin dual in-line packages, rather than the bulky, oddly shaped packages of earlier models. Thus, it is much easier to make use of their inherent large bandwidth to process such discontinuous-boundary waveshapes as digital and switching signals.

## A standard product

The tapped delay lines in DIPs are widely available and can replace complex arrangements of logic gates. They can drive or be driven by transistor-transistor logic, emitter-coupled logic, and other digital families that are capable of delivering sufficient drive current. Happily, a knowledge of only a few basic rules is required for practical implementation of these devices.

Several manufacturers now make what may be regarded as the industry-standard tapped delay line. The table gives typical characteristics for versions that introduce a signal delay of 10 to 150 nanoseconds. No matter who the maker or what the delay time, cost is about \$12 apiece, dropping to \$3 in lots of 1,000 or more.

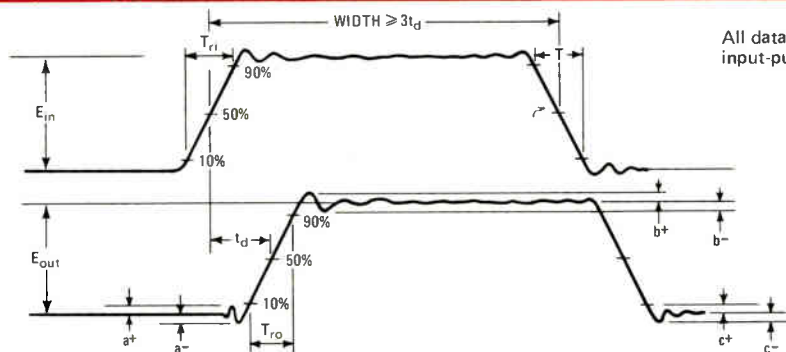
Standard delay lines have either a 50- or 100-ohm characteristic impedance, suited for ECL or TTL respectively. They require terminating resistors, which first were mounted on the printed-circuit board, external to the delay line. However, this arrangement often created more problems with capacitive loading, reflections on the line, and so on. Now many of the standard delay lines have built-in terminators.

For the units that still require add-on termination, a single resistor or the Thevenin-equivalent (two-resistor) arrangement may be used. The two-resistor termination is designed to reduce the current load on the unit driving the delay line.

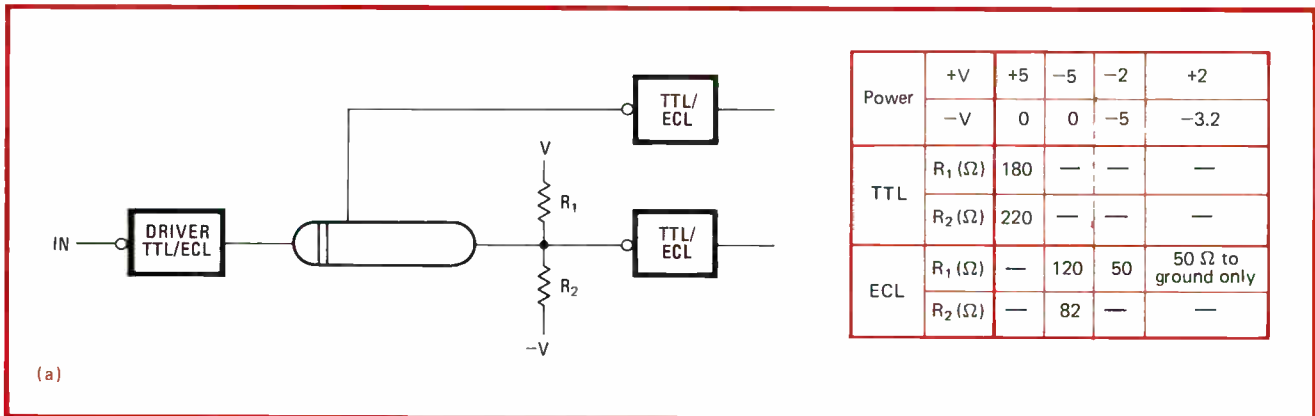
Delay lines may be customized to provide a desired set

TYPICAL DELAY-LINE CHARACTERISTICS

$t_d$ Total delay (ns)	$t_t$ Tap delay (ns)	Maximum rise time (ns)		Dc resistance input to output ( $\Omega$ )	Distortion (%)			Impedance ( $\Omega$ )	Total attenuation (%)	Total temperature coefficient delay (ppm/ $^{\circ}$ C)
		Input $T_{ri}$	Output $T_{ro}$		Prepulse (a)	Pulse (b)	Postpulse (c)			
10 $\pm$ 1.0	1.0 $\pm$ 0.25	3.0	5.0	1.0	$\pm$ 13	$\pm$ 13	$\pm$ 13	100 $\pm$ 10% 50 $\pm$ 10%	2	100 (0 $^{\circ}$ -85 $^{\circ}$ C)
20 $\pm$ 2.0	2.0 $\pm$ 0.25	3.5	7.0	1.0	$\pm$ 12	$\pm$ 12	$\pm$ 12			
30 $\pm$ 2.0	3.0 $\pm$ 0.3	3.5	7.3	1.5	$\pm$ 10	$\pm$ 10	$\pm$ 10			
50 $\pm$ 2.5	5.0 $\pm$ 0.5	5.0	11	2.5	$\pm$ 15	$\pm$ 15	$\pm$ 15			
100 $\pm$ 5.0	10 $\pm$ 1.0	6.5	23	1.4	$\pm$ 13	$\pm$ 13	$\pm$ 13			
150 $\pm$ 7.5	15 $\pm$ 1.5	8.0	30	1.7	$\pm$ 13	$\pm$ 13	$\pm$ 13			







of tapings, but they are readily available in a wide range of delays varying from 10 to 500 ns. The taps are usually spaced at  $T/10$  increments, where  $T$  is the overall delay at the line. The overall delay accuracy to be expected for lines having a specified delay greater than 50 ns is 5%, with a tap accuracy of 10%. For lines of less delay, overall accuracy varies from 7% to 10%, and tap accuracy varies from 10% to 25%.

The overall line errors are not cumulative at the taps, however. Thus, if a 100-ns line has been designed to have 10 equally spaced taps, the actual delay may vary from 95 to 105 ns, but each tap will be calibrated to within  $\pm 1$  ns of its 10-tap increment.

The latest development in delay lines in DIPS is one with built-in TTL drives, TTL interface chips driving each output pin, and internal terminating resistors. While such a design eases interface problems, its quantity cost is about three times that of the standard, noninterfaced types. Thus it pays to know the ground rules for interfacing the standard delay lines.

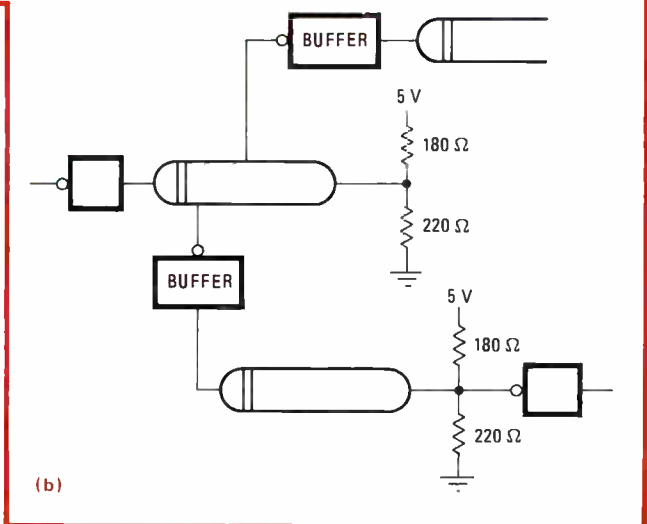
#### Four considerations

The questions that must be answered when designing digital applications of delay lines are often more practical than theoretical. At least, they are of a sort whose answers are not directly provided by the manufacturer. Fortunately, learning the design guidelines is not difficult, and other information can be gained by careful measurements and experience.

To begin with, TTL and ECL present somewhat different interfacing problems. Also, certain precautions must be taken when cascading delay lines. Third, it is necessary to find the equivalent capacitance produced by external wiring across a delay line's tap in order to determine the loading effect, or alternatively it is necessary to determine the maximum length of the external wiring connecting a tap to a logic element. Finally, other characteristics of the standard delay lines, not listed in the table, may be design considerations.

#### The proper interfacing

One or more taps of the delay line usually face the inherently asymmetrical input circuit of a TTL device, yet this logic element has a minimal effect on delay-line loading. During the logic 1 input condition, a TTL gate presents an impedance above 50 kilohms. This impedance is so far in excess of the 100-Ω terminating imped-



**1. Termination.** Two-resistor, or Thevenin-equivalent, arrangement (a) reduces the load on TTL or ECL drivers while providing 99-ohm termination for a 100-ohm delay line (TTL-driven) or 50-ohm termination for a 50-ohm line (ECL-driven). When cascading delay lines from intermediate taps, buffers are required (b), since it is necessary to avoid unwanted reflections caused by mismatching.

ance of the delay line that it causes little loading. During the logic 0 condition, input impedance is about 4 kΩ, so there is virtually no loading. The Schottky-TTL gate's input impedance is about 45 kΩ during the logic 1 state and about 2.8 kΩ during the logic 0 condition.

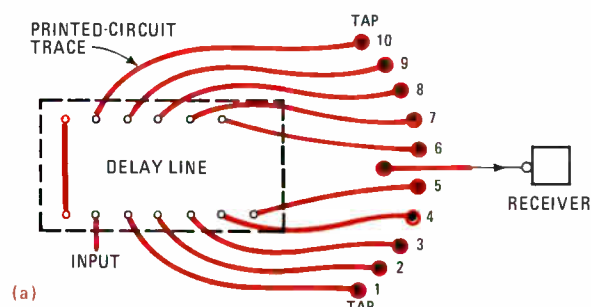
Asymmetrical loading will become a problem when more than three Schottky gates or more than four standard TTL gates are driven by the delay line. Three Schottky loads will increase the signal's rise and fall times about 2% at the output of a 100-ns delay line, and four standard loads will increase the times about 10%.

When terminating a delay line in any TTL application, the best approach is a 180-Ω resistor and a 220-Ω resistor connected in series between the positive supply and ground with their junction connected to the input of the delay line (Fig. 1a). This method limits the load current of the delay-line driver to 30 milliamperes, and it provides a 99-Ω termination for the delay line.

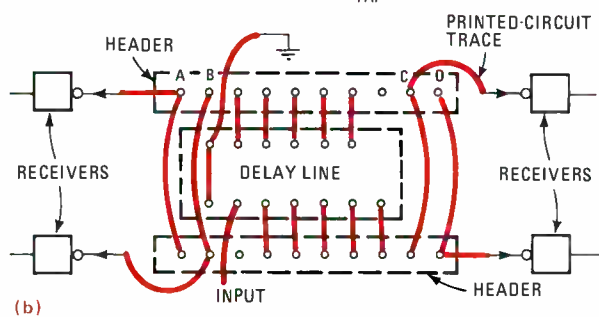
For ECL powered by a single -5-volt power source, 82-Ω and 120-Ω resistors configured the same way provide suitable termination. When the ECL is powered by such dual supplies as -5 v and -2 v, a single 50-Ω resistor between the output of the delay line and the

## Making connections

The physical connections between a delay line and any logic element pose no particular problems, but there are choices to be made. An inexpensive method is first to bring all taps to plated-through holes on the printed-circuit board and then to connect flexible jumpers (not shown) from each gate input to the desired tap point. The holes can be arranged in a semicircle, as shown in a.



(a)



(b)

NOTE: ALL VIEWS FROM CIRCUIT SIDE OF BOARD

-2-v source will do. When using +2 v and -3.2 v, a single 50-Ω resistor between the delay line's output and ground will suffice.

When it comes to driving a standard 100-Ω delay line, the choice is clear. Buffered Schottky-TTL gates can handle more current and have shorter propagation times than standard TTL, and using these gates is the best choice. Tipping the balance in their favor are their high current capability and a cost below that of ECL. It is best to use ECL elements to drive 50-Ω delay lines.

### The trick in cascading

A related termination problem is the cascading of delay lines. Cascading results in an increase in the output signal's rise and fall times according to:

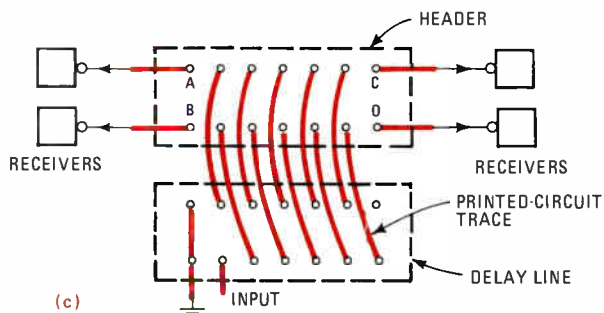
$$t_r = (t_{in}^2 + t_1^2 + t_2^2 + \dots + t_n^2)^{1/2}$$

where  $t_r$  is the total rise or fall time,  $t_{in}$  is the rise (or fall) time of the input signal, and  $t_1 \dots t_n$  is the respective rise (or fall) time of each delay line. Note that the rise and fall times of any individual delay line vary directly as its length.

When cascading delay lines from intermediate taps, a buffer (Fig. 1b) will prevent unwanted reflections caused by mismatch. The buffer removes the loading effect without causing any signal distortions.

Determining maximum lengths for external wiring and the related capacitance across a tap can be a simple

Two other methods use terminal blocks, or headers, installed next to the delay line (b and c). There is easy connection between the header's solder pins and each tap by pc-board traces. While more expensive than the first method, these approaches are more convenient from a production standpoint, save board space, and reduce stray capacitance because of their shorter leads.



(c)

job. The maximum wire length between a tap and a gate can be found if the impedance of the delay line and the delay time are known. For the purposes of illustration, assume a microstrip configuration where the foil (trace) is separated from a ground plane by 0.03 inch of pc-board material. The capacitance of the wire under these conditions is known to be 2 picofarads per inch.

### Some calculations

The capacitance across a given delay line of impedance  $Z_0$  and delay  $t_d$  is given by:

$$C = 100 t_d / Z_0$$

where  $C$  is given in picofarads if  $t_d$  is given in nanoseconds, and  $Z_0$  is measured in ohms.

For a typical case where  $t_d = 10$  ns and  $Z_0 = 100$  Ω,  $C$  will be 10 pF. A 0.5-in. wire of the type described above presents a 1-pF load to the delay line. This capacitance, which is 10% of  $C$ , would become significant as viewed by any of the 10 taps along the line.

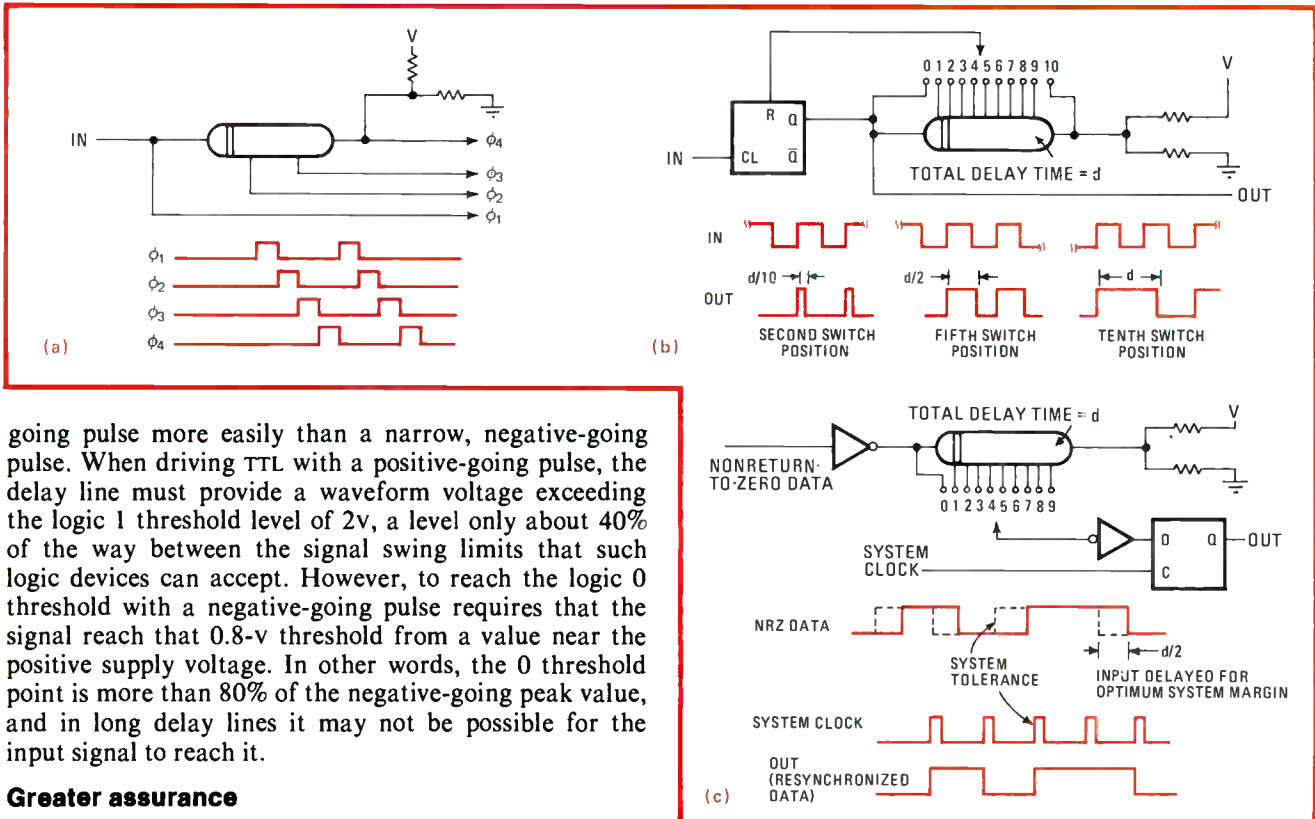
Similarly, a 150-ns delay line would have an equivalent capacitance of 150 pF. In this case, a wire as long as about 7 in. (a 14-pF load) could be connected to a tap before response would be noticeably affected.

There are several other points to consider when designing analog tapped delay lines in DIPs into digital applications. These arise from delay-line characteristics that show up in use.

Applying a voltage at any point on a delay line has no effect on its delay properties if the delay line does not contain a ferrite core. Of course, the voltage may itself affect the input signal or its driver adversely.

Temperature changes have a relatively small effect on delay time, amounting to about 2% over the range from 0°C to 85°C. However, the effect on rise and fall times over the same range amounts to more than 15%. These figures were determined experimentally from tests on a 100-ns delay line.

The standard delay line handles a narrow, positive-



going pulse more easily than a narrow, negative-going pulse. When driving TTL with a positive-going pulse, the delay line must provide a waveform voltage exceeding the logic 1 threshold level of 2v, a level only about 40% of the way between the signal swing limits that such logic devices can accept. However, to reach the logic 0 threshold with a negative-going pulse requires that the signal reach that 0.8-v threshold from a value near the positive supply voltage. In other words, the 0 threshold point is more than 80% of the negative-going peak value, and in long delay lines it may not be possible for the input signal to reach it.

**Greater assurance**

Using a positive-going pulse where possible provides greater assurance that the output pulse will have sufficient amplitude to drive the gates. Moreover, the variation of the pulse width at the delay line's output taps will be minimized because the effective rise and fall times as measured at the 40% point are less than at the 80% point.

Signal degradation is no problem with ECL, because such logic elements supply high drive currents. Thus the length of the delay line will minimally affect the waveform properties.

The pulse frequency has an effect on the delay line's output only if the frequency is so high that a given pulse is distorted because of reflections on the line caused by a previous pulse. The width of the narrowest pulse that can be delayed by a particular delay line and still achieve at least 85% of its original amplitude can be shown to be:

$$t_p = t_R + \frac{(t_f - t_r)}{2}$$

where  $t_p$  is the input signal's pulse width measured between its 50% amplitude points,  $t_R$  is the delay line's rise time measured between the 10% and 90% amplitude points,  $t_f$  is the input signal's fall time measured between the 90% and 10% amplitude points, and  $t_r$  is the input signal's rise time measured between the 10% and 90% amplitude points. When  $t_f$  and  $t_r$  are equal, the minimum width of an input pulse must of necessity be equal to the delay line's rise time if it is to pass to the output relatively undistorted.

Delay lines may be put to good use in any area of logic circuit design where timing relationships are important or where the time interval involved is less than the system clock period. Thus, phase-delay circuits, pulse

**2. Applications.** Analog delay lines have large bandwidth; thus they may be used to process digital waveforms. A basic phase-delay circuit (a), a pulse shaper (b), or a data resynchronizer (c) may be constructed often more simply than all-digital networks.

formers, and data resynchronizers are perhaps best implemented with a delay line. Examples of these circuits are shown in Fig. 2.

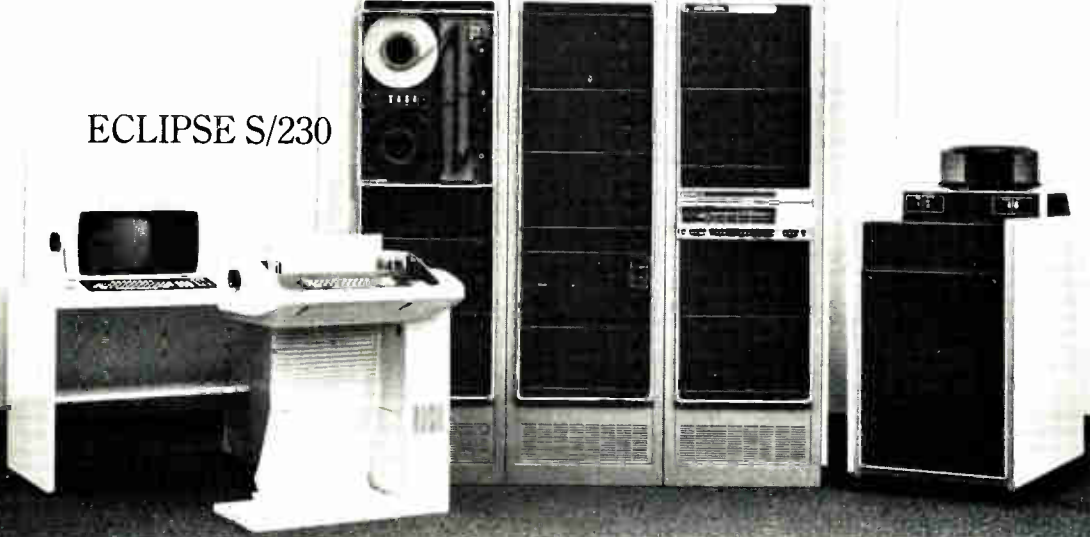
**Simpler solution**

The fact that the delay line was conceived for analog applications does not impede its usefulness in these digital applications. For example, the all-digital solution to the simplest circuit of Fig. 2, the phase-delay circuit, will be far more complex than need be. To obtain the total delay time required, either the delay time through many gates will have to be used, or else a clocked digital shift register arrangement will be needed.

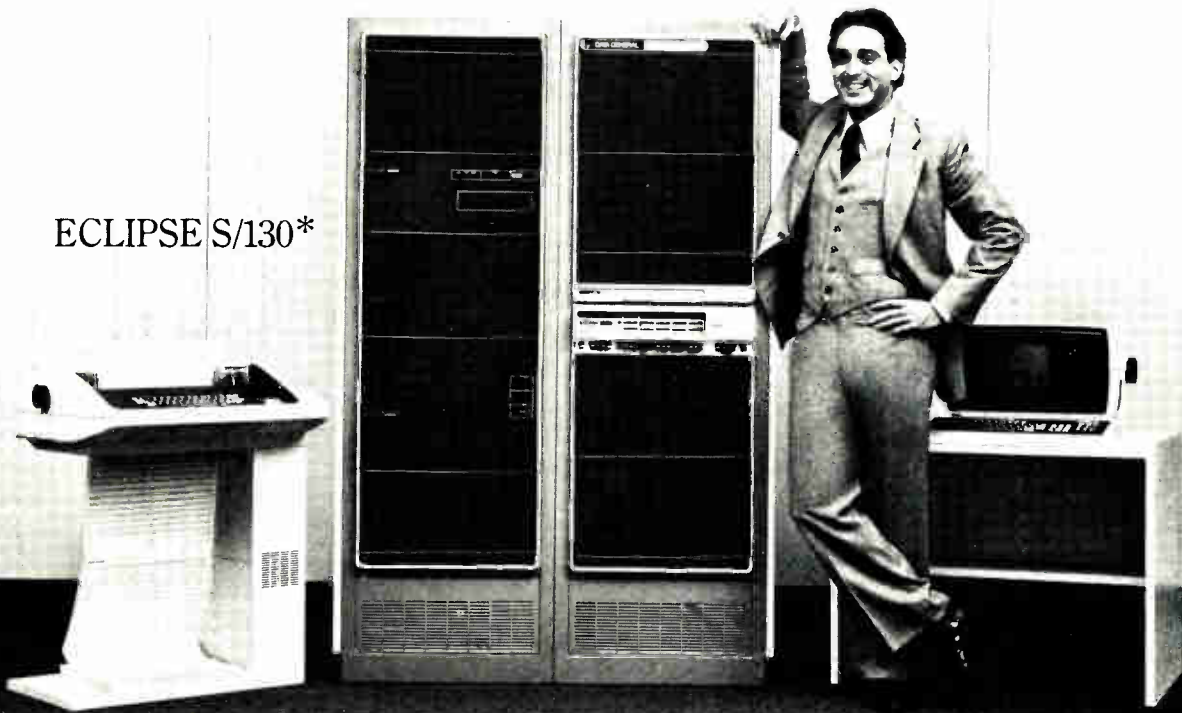
As clock times get shorter, it will become necessary with either method to consider individual logic-gate propagation times. The futility of using such circuits will soon become apparent. For example, a standard 7400 TTL inverter has a typical propagation time of 10 ns, but a maximum of 20 ns. Therefore, the total propagation time through a string of such gates is almost impossible to calculate accurately even with the several excellent approximation equations that exist. If a clocked shift register is used instead of the delay line, the timing problems do not disappear, and, in addition, the circuit becomes complex.

This is a perfect example of where a delay line with selectable taps should be used. The all-digital solutions to the other two circuits present similar problems, so delay lines are the best route for similar reasons. □

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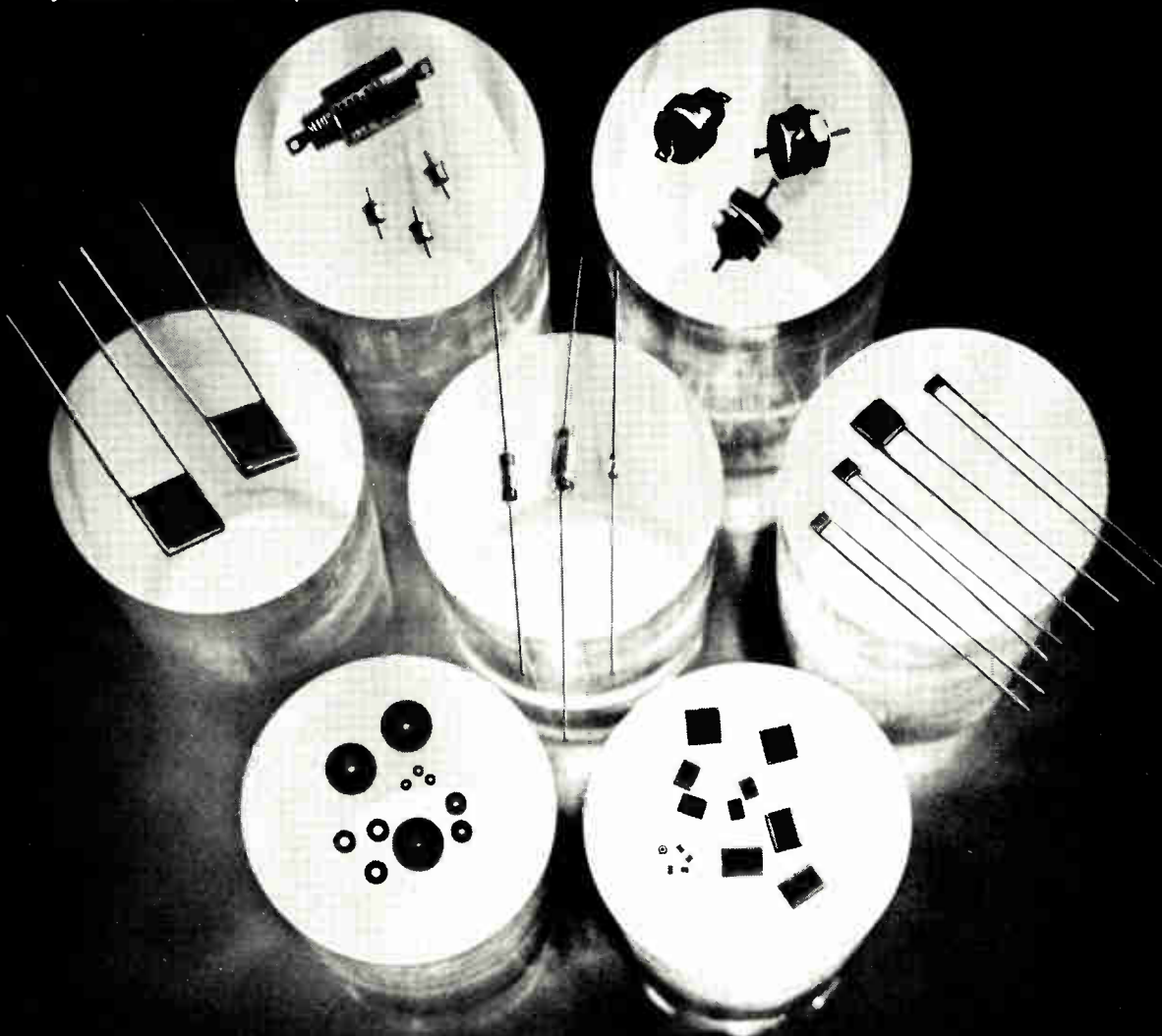
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## Module minimizes repair time of process-control systems

by Ralph Foose  
*Industrial Nucleonics Corp., Columbus, Ohio*

Today a great many industrial processes cannot run efficiently without sophisticated digital control systems—and often stop running entirely when this control equipment goes down. If uptime is to be maximized at reasonable cost, therefore, a process-control system's mean time to repair must be considered as significant as its mean time between failures, and its maintenance requirements should affect its design all the way from its architecture on down to the details of its electronic circuitry.

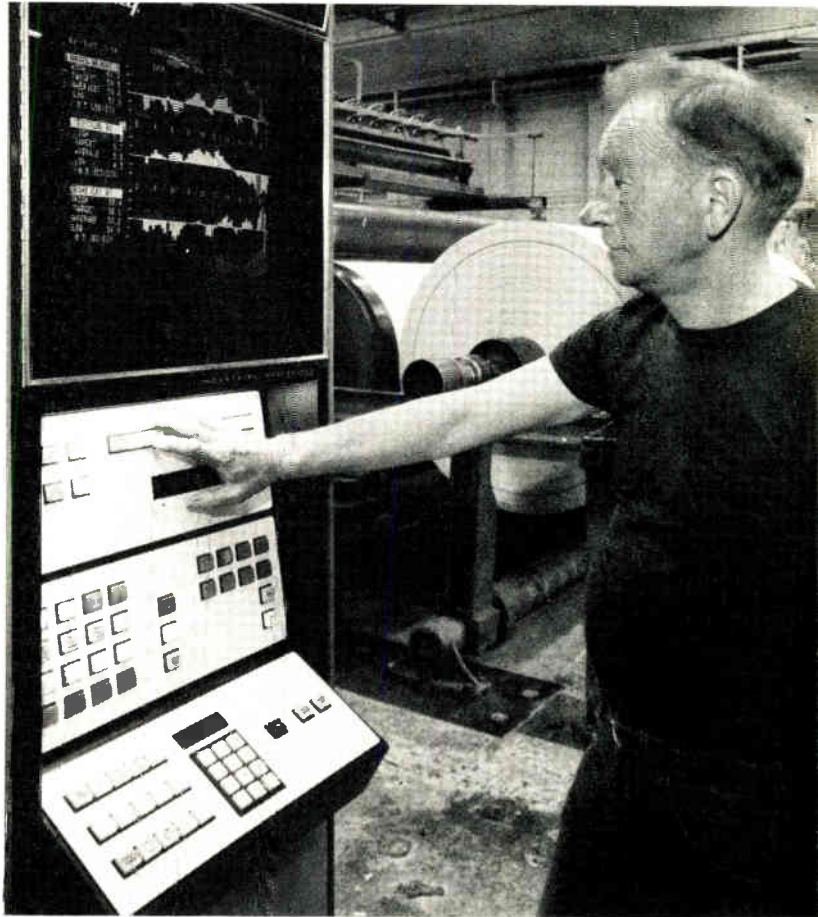
One of the best ways of minimizing a system's repair time has always been to go to easily replaceable modules for each system function. A microcomputer-based system, though, improves on this approach: it can be designed to automatically diagnose its own circuit and system faults down to the module level and to notify the operator which module is the faulty one.

Indeed, a programmable microcomputer module (PMM) built around an 8080 microprocessor has achieved a mean time to repair of only a few minutes, despite the complexity of the process-control equipment it generally runs. Using its special software diagnostics, even an untrained operator takes less than a minute simply to test all the PMM's modules.

### Why the stress on diagnostics

Usually, the time it takes to identify what has caused the failure of a system of any complexity is much longer than the time it takes to repair the fault and verify the system's functionality. In modular electronic equipment, more especially, finding the faulty module often takes 90% of the total repair time and typically requires the highest level of expertise from repair personnel. But both the time and the expertise required can be significantly reduced through use of comprehensive diagnostics. These savings are especially significant in computer-based equipment, in which the ability to execute a diagnostic algorithm is inherent as a result of the properties of the computer itself.

That still leaves the designer with the job of deciding how diagnosable his system is to be since he has to trade this feature off against reliability, cost, and similar factors. This decision can only be made in terms of an overall maintainability philosophy. Will skilled technicians maintain the system? Will assemblies be repaired on site? What percent of possible failures must the diagnostics identify? How much added cost will be allowed to meet diagnosability goals? This last question



**1. Programmable microcomputer module.** Based on an 8080 microprocessor, the PMM can control all the parameters of an industrial process, as shown above in a paper mill. Each PMM can run fault-diagnostic tests on all of its own modules in less than a minute.

is often not identified during detailed design of the electronics but can be significant. In the case of the PMM, a design objective of automatic testability of 80% of the circuitry for 10% above basic cost was set.

### System description

Pictured in Fig. 1, the PMM can serve as a stand-alone computer in a process-control system. Alternatively, it can interface process input and output data to another computer—a Honeywell Level 6 minicomputer—in a hierarchically structured, two-level distributed-processing system. A typical two-level structure has many PMMs clustered around the minicomputer. Each PMM is programmed to run multiple tasks with a multi-tasking real-time executive. All operate asynchronously and are polled by the minicomputer for their data.

Many of the systems so far built around the PMM provide a set of scanning measurements of sheet processes, of the kind to be found in paper making. The measurements are made with the aid of infrared, nuclear

## The repairability-reliability tradeoff

The availability of a process-control system can be roughly quantified by expressing its uptime as a percentage of the time it is fully functioning, or:

$$\left(1 - \frac{\text{MTTR}}{\text{MTBF}}\right) 100$$

This equation offhand suggests a system should combine the shortest possible mean time to repair (MTTR) with the longest possible mean time between failures (MTBF).

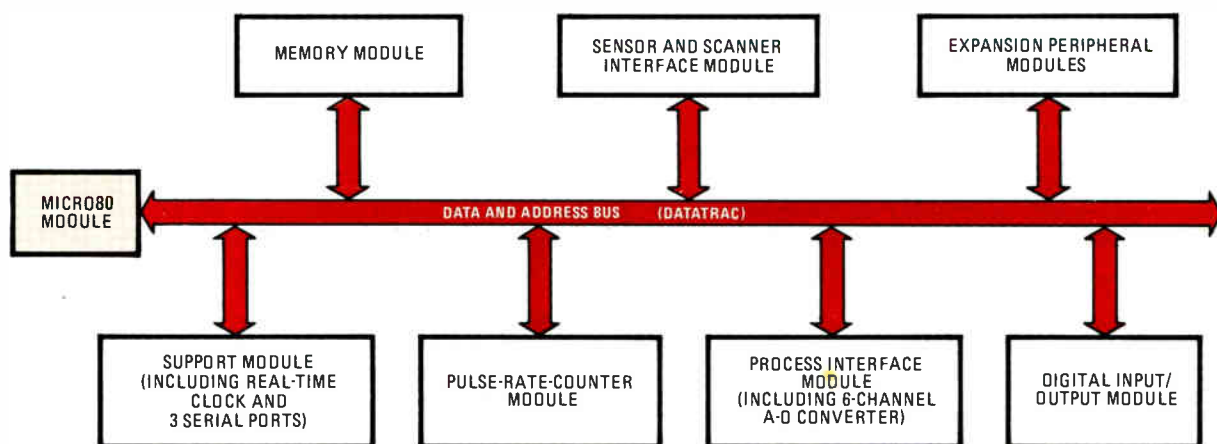
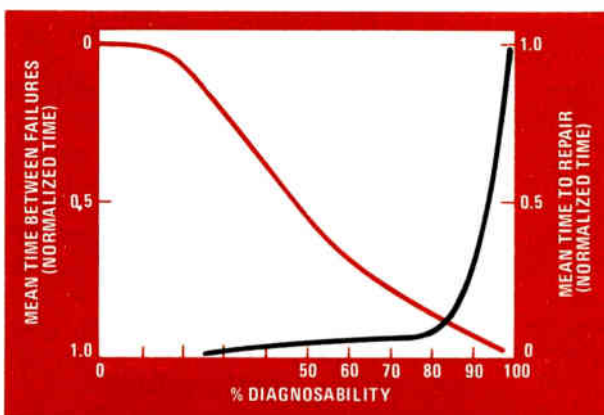
But on weighing how to achieve the greatest system availability, the designer inevitably finds these two goals in conflict. Either he can design a system to be quickly diagnosable and repairable (have a short MTTR), or he can design it to fail seldom (have a long MTBF). For, as components are added to circuitry specifically to support a diagnostic function, the system's overall reliability, or MTBF, declines sharply.

Cost considerations are a further complication: users would be unable to justify the price they would have to pay for a sophisticated process-automation system with an MTBF of 60,000 hours.

The degree to which designing for a short MTTR sets limits to the MTBF varies both with the complexity of the electronic function involved and with the precise length desired for the MTTR. The figure shows a typical interaction for complex electronic modules. Evidently, a goal of

30% to 50% built-in diagnosability carries only a small MTBF penalty. But obtaining something close to 100% diagnosability significantly compromises the MTBF.

At this point, the designer's overall system-maintenance philosophy (number of technicians presumed available, desirability of on-site repair, etc.) will determine the degree of diagnosability for which he should aim. To meet the demands placed on process-automation systems, though, a useful target generally falls somewhere between 80% and 90%.



**2. Data flow.** Heart of the PMM is its Micro80 module—a printed-circuit board bearing a 8080 microprocessor, 1 kilobyte of RAM, 7 kilobytes of ROM, and bus control circuitry. It is linked to other PMM modules by a 16-bit data bus allowing for later substitution of a 16-bit processor.

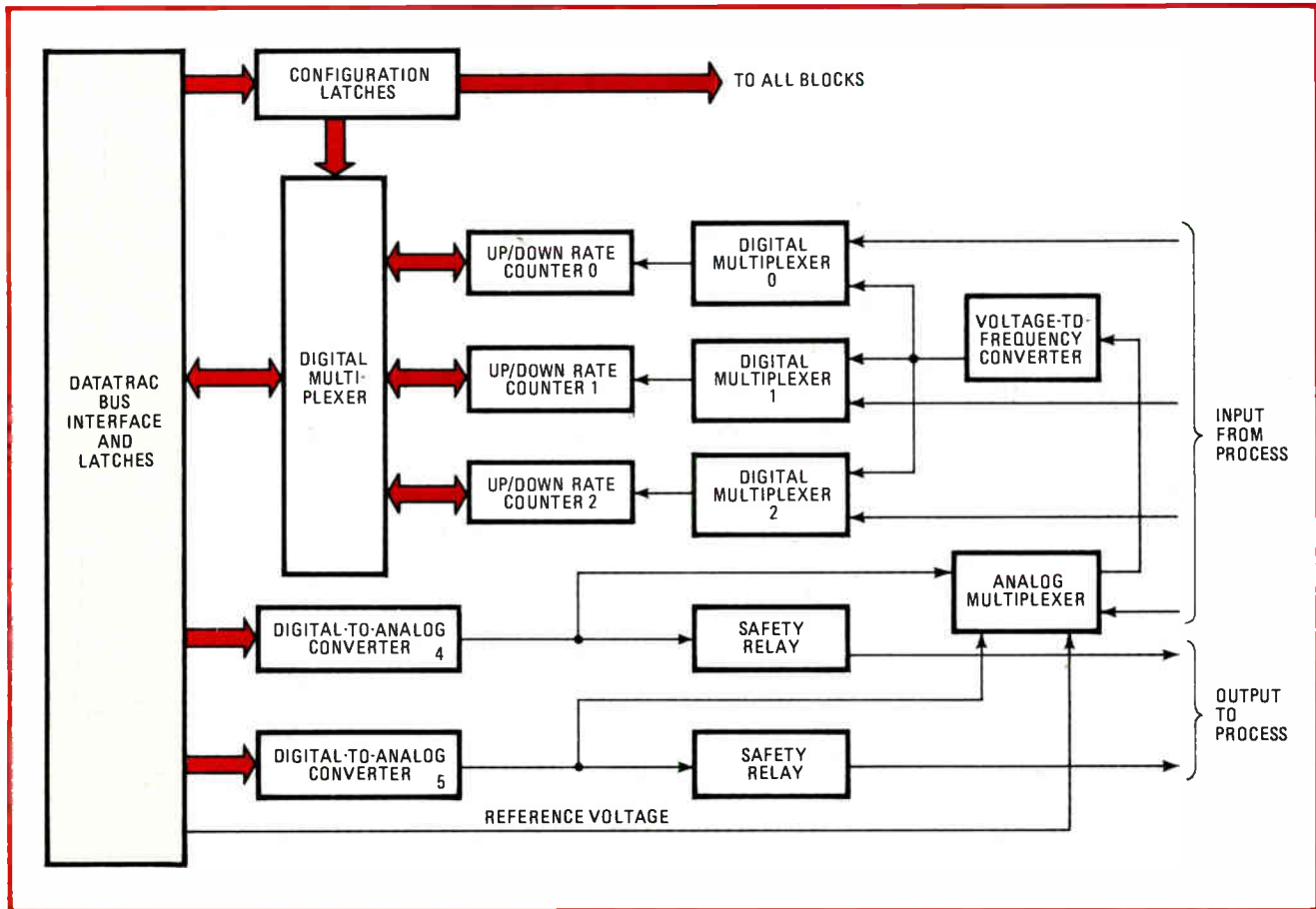
decay, X-ray, and magnetic sensors. In such a setup, the 8080 microprocessor within the PMM:

- Provides positioning control and logic for each scanning mechanism.
- Processes signals from sensors to extract the desired

information (on weight, moisture, thickness, etc.).

- Processes other analog and digital I/O data.
- Communicates with the minicomputer.
- Handles operator interface processing and control for push buttons, lamps, and numeric displays.





**3. Count down.** This modular pulse-rate counter can be automatically tested by the PMM's software. The module is tested each time power is turned on or if a momentary switch is opened on the microprocessor board. Faults are indicated visually and stored.

■ **Handles system and process diagnostics.**

The microprocessor is part of the Micro80 module, one of several subassemblies or modules that make up the PMM (Fig. 2). Mounted on the Micro80 printed-circuit board alongside the 8080 microprocessor are 1 kilobyte of random-access memory, 7 kilobytes of programmable read-only memory, and bus control circuitry. The PMM's other boards include a memory module, interface modules with the sensor-scanners and the process itself, and communications boards.

**On the track**

Handling all communications between these modules is a bus structure called Datatrac (a registered trademark of Industrial Nucleonics). The data bus is set up for 16-bit data, and all data transfers are two bytes wide, to allow for future expansion by incorporation of a 16-bit microprocessor into the Micro80 module.

Various plug-in modules link the Datatrac bus to external devices. Each contains several generalized functions that the system designer can decide to use in any one of several configurations, selecting the appropriate

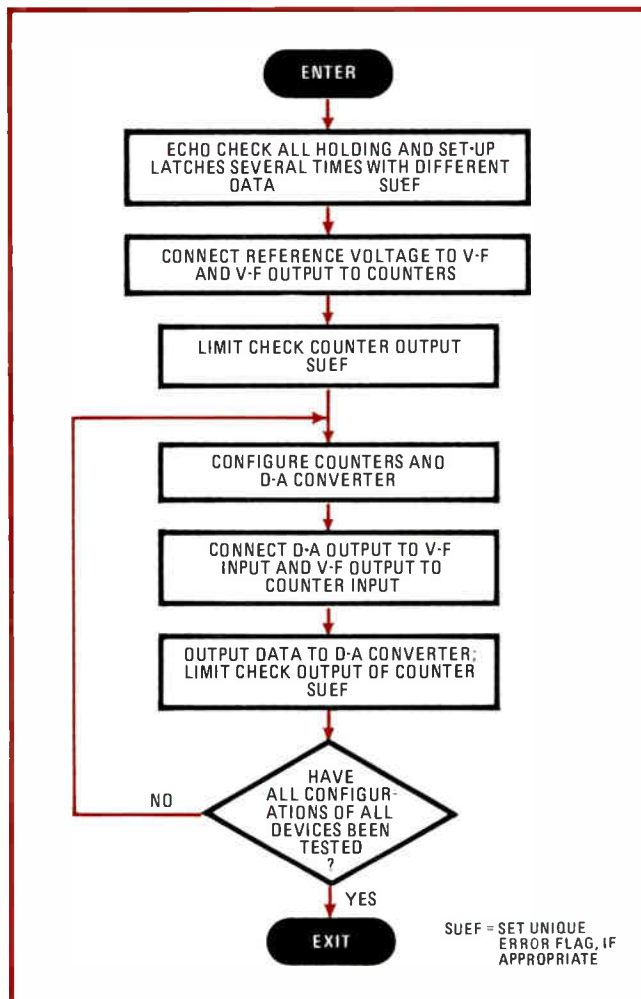
one at the time of system initialization. For instance, it is possible to configure the analog-to-digital converter in the process interface module to function as either a unipolar or a bipolar 12-bit a-d converter.

Since most of the subassemblies making up the PMM are manufactured in house, vital considerations are the cost, availability, reliability, and longevity of the components selected, plus the existence of multiple suppliers. Several microprocessors were evaluated in this light, and the 8080 had the edge in the time frame during which the design was in progress.

An additional factor was the popularity of the 8080, which has stimulated many sources to produce assemblers, simulators, and other tools for system development and production use.

**Diagnostic considerations**

The primary fault-isolation tool in a PMM is a package of software, some or all of which is stored in a programmable ROM. This PROM exercises the various hardware modules and reports go/no-go results visually, in addition to storing detailed data on any faults it finds for



**4. Self-diagnosis.** The generalized flow chart of the exerciser software for the pulse-rate counter indicates the testing sequence for its counters, digital-to-analog converters, and voltage-to-frequency converter. Note the error flags (SUEF) set at critical test points.

later retrieval. The set of exercises is automatically executed on the hardware whenever power is turned on and whenever a momentary switch on the Micro80 board is operated. The visual readout indicates the physical location of any module found to be faulty.

For this diagnostic approach to be maximally effective, four principles of system design must be followed in the development stage. First, the system must be partitioned onto pc boards *by function*, such that each replaceable module contains one or more easily tested functions. Second, the modules during testing must not produce outputs that could adversely affect the other modules or the process. Third, the partitioning of the system functions must ensure a testing sequence in which each module is tested only by previously checked-out hardware. Fourthly, diagnostic needs must be carefully balanced with other system design considerations, such

as cost and the mean time between failures (see "The reparability-reliability tradeoff," p. 122).

A good example of what its diagnostic software does for the PMM is its method of checking out its memories. When the PROM is being loaded at the time of system manufacture, a cyclically redundant code is used to generate a parity check word for each kilobyte of read-only memory. This check word is then stored at the end of the 1-kilobyte block. The exerciser for this module recomputes this check word, compares it to the one stored at the end of the memory segment, and thus verifies the integrity of memory.

#### Another diagnostic example

More unusual techniques are necessary to diagnose a typical process-I/O module automatically. These techniques are best illustrated by describing in some detail a pulse-rate counter module and its exerciser.

This module contains 2 digital-to-analog converters, 3 counters, and 1 voltage-to-frequency converter. Figure 3 is a block diagram of the pulse-rate counter module's major functional blocks. The 16-bit counters can be separately configured as count up, count down and interrupt, or pulse-rate counters. The 10-bit current-output d-a converters can be separately configured to have a range of either  $\pm 50$  milliamperes or  $+20$  mA. The safety relays are normally open.

The testability of this module is attributable to the following factors:

- The contents of the configuration latches can be preset and verified by the microprocessor.
- Each counter can be preset and verified by the diagnostic program.
- The d-a converter outputs can be disconnected from the process and multiplexed into the v-f converter.
- A known reference voltage can be multiplexed into the v-f converter.
- The v-f converter output can be connected to any or all of the counter inputs.

The generalized flow chart for the exerciser software associated with the pulse-rate-counter module is shown in Fig. 4. This program is called for by, and returns to, a master program that oversees the entire PMM checkout.

The flow chart and block diagram indicate that almost all hardware in the pulse-rate-counter module can be tested by the diagnostic software. Error flags set by this exerciser are passed on to the calling program, which in turn stores the information and drives the display mentioned previously.

Methods similar to those employed in this module exerciser are used to test all modules in a PMM, with the result that, as noted, a fully equipped PMM can be tested in less than 1 minute. As for the original design objective—making 80% of the hardware automatically testable for only 10% added cost—an analysis of all PMM modules reveals that it was achieved and is practical. □

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of 70MHz and a slew rate of  $25V/\mu\text{sec}$ .

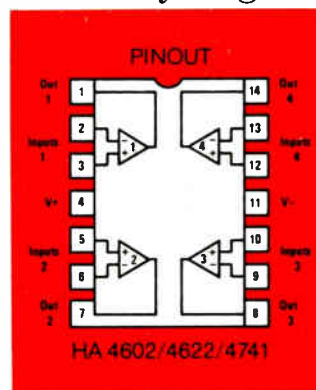
**Performance/Price.** Impressed with this high performance? You'll be just as impressed by the price. For military use the HA 4622-2 and HA 4602-2 cost \$9.90. For commercial, the HA 4625-5 and the HA 4605-5 cost \$4.95 (100-up prices).

**Economy Too.** For those of you more inclined to go the economy route, there's our very popular HA 4741 quad op amp. With its superior bandwidth of 3.5MHz, slew rate of  $1.6V/\mu\text{sec}$  and input voltage noise of  $9\text{NV}/\sqrt{\text{Hz}}$ , it offers a lot of amp for the money. For instance, the HA 4741 for military usage costs just \$4.60, while

the HA 4741 for commercial costs \$2.15 in ceramic, and \$1.65 in epoxy (100-up).

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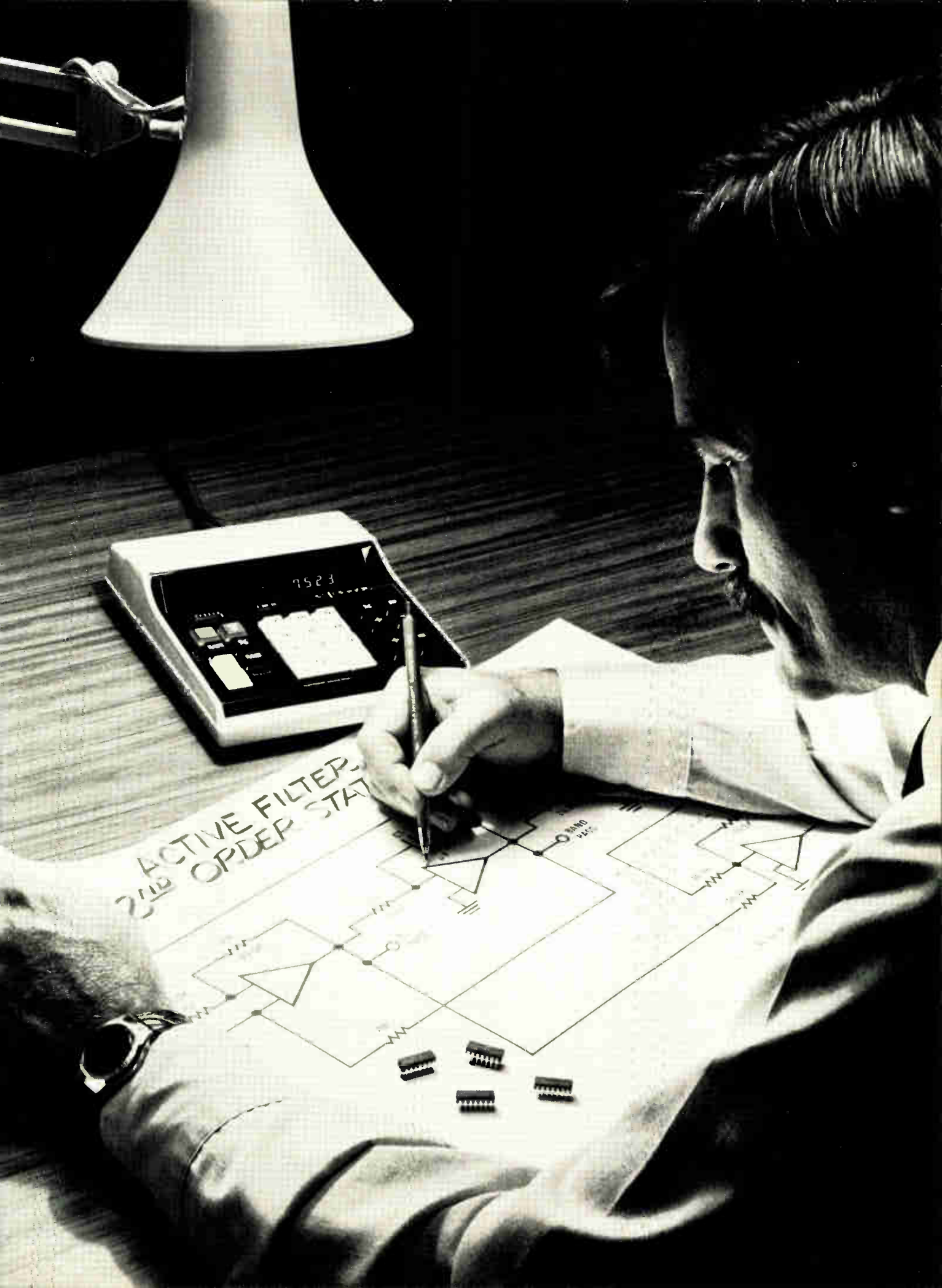
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## Interfacing an auto-ranging DVM to a microprocessor

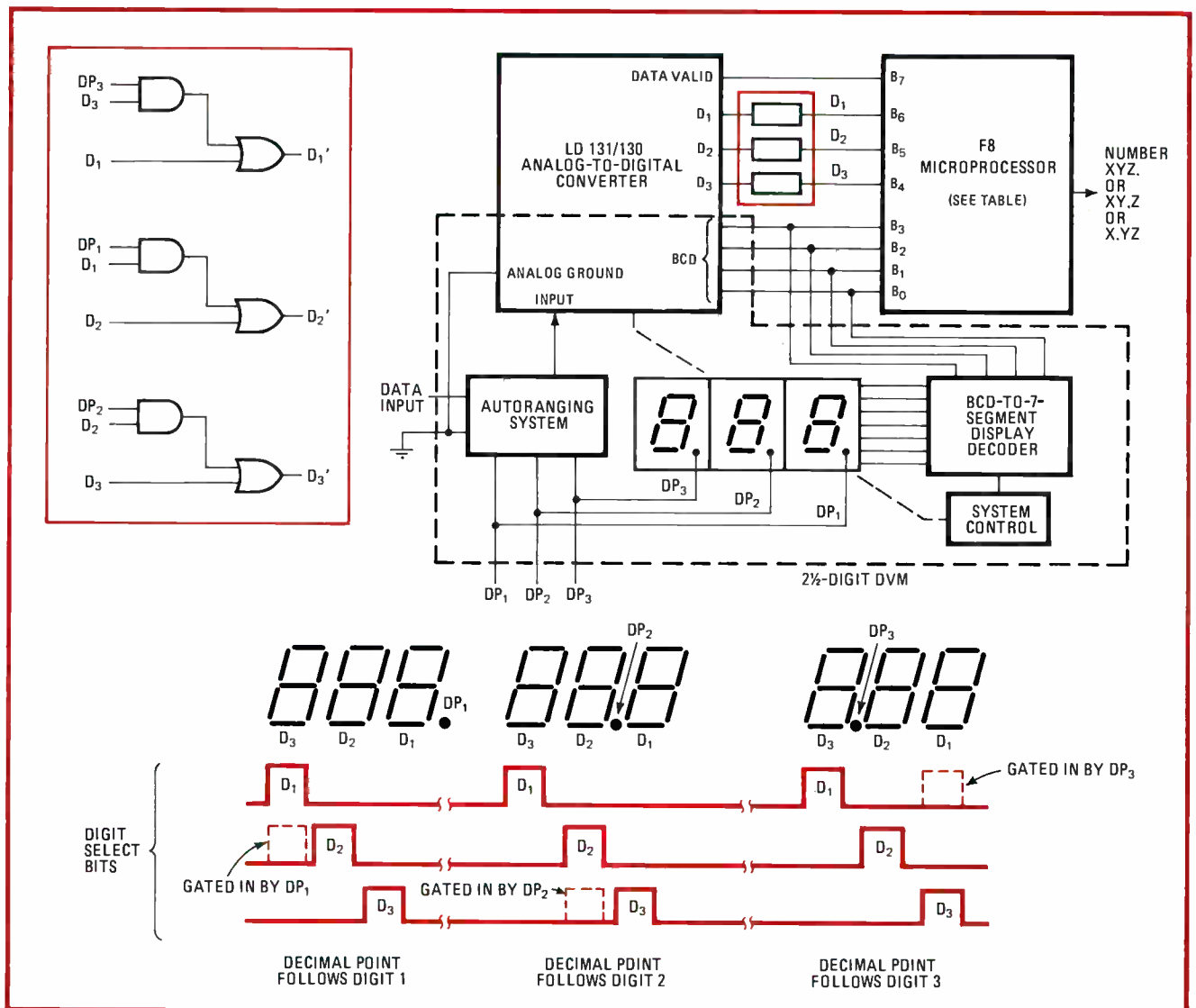
by Steve Hui and John Richartz  
Tektronix Inc., Beaverton, Ore.

Several logic gates and a few bytes of instructions provide all the hardware and software needed for building an interface between an auto-ranging digital voltmeter and a microprocessor. This circuit enables an 8-bit processor to read the magnitude of any voltage measured by a 2½-digit DVM. The accompanying deci-

mal-point information contained in the input data is recovered with a combination of AND and OR gates and a simple program.

The hardware portion of the system is shown in the figure. The auto-ranging DVM circuit contained within the dotted line is a standard data system. Generally, any data introduced to the DVM is first converted by the LD131 analog-to-digital converter into binary-coded-decimal form, one digit at a time, in order to drive the display decoder and thus the numeric displays. The decimal-point data is introduced into the displays directly by means of lines DP<sub>1</sub>-DP<sub>3</sub>.

However, when the F8 8-bit microprocessor reads any data generated by such a system, the decimal-location information cannot be directly introduced into it because



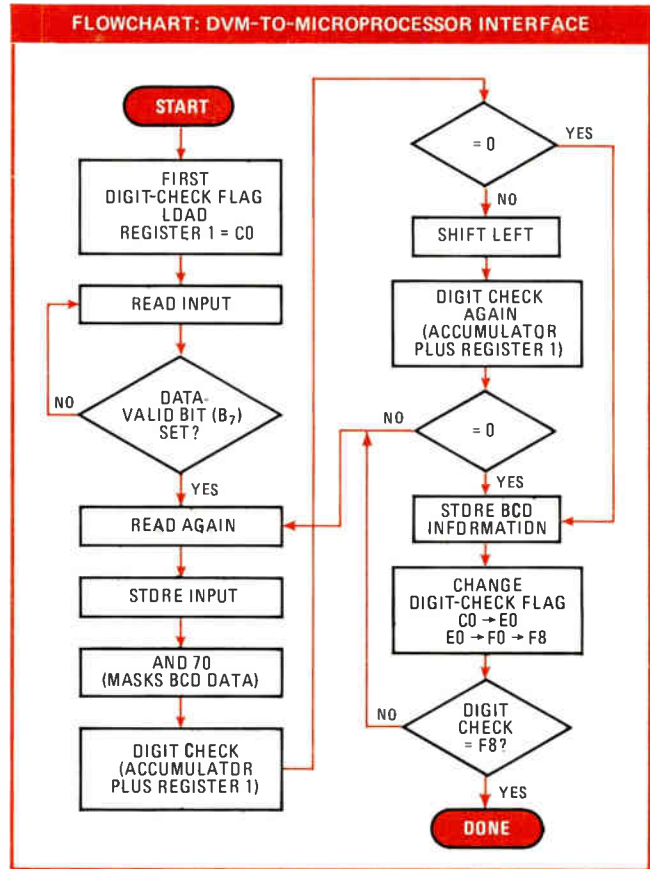
**Interface.** Several logic gates and small program will unite auto-ranging DVM to microprocessor. Decimal-point information is recovered at output of F8 by connecting each digit-select line (D<sub>1</sub>-D<sub>3</sub>) of a-d converter to two port bits of F8 through AND-OR gate interface, and by using simple software to detect resultant conditions shown in timing diagram. A storage scope helps check the digits' movement through the circuit.

there are too few input ports available. An obvious solution might be to use a 16-bit microprocessor, but this is not efficient, either from a device-cost or a programming standpoint.

But although decimal-point data cannot be placed on the BCD data lines (B<sub>0</sub>–B<sub>3</sub>) of the F8, the information may be placed on lines B<sub>4</sub>–B<sub>6</sub>. B<sub>4</sub>–B<sub>6</sub> would otherwise perform their single function—accepting command data from the LD131's digit-select lines (D<sub>1</sub>–D<sub>3</sub>), which enables the processor to read the digits in sequence. Now, however, each digit-select line with a gated-in decimal-point signal is coupled to two ports on the F8, not just one as before, in the manner apparent from the module (see left of figure). This hardware connection enables a simple program to be written for the F8 that will separate the digit-data from the decimal-point data.

As indicated by the timing diagram, if the decimal point occurs after the least significant bit (digit 1), lines D<sub>1</sub> and D<sub>2</sub> assume a logic 1 state during the digit-1 time interval; if the decimal point occurs after digit 2, lines D<sub>2</sub> and D<sub>3</sub> move to logic 1 during the digit-2 interval; if after digit 3, lines D<sub>1</sub> and D<sub>3</sub> go high. In other words, if the decimal point occurs after digit *i*, then lines, *d<sub>i</sub>* and *d<sub>i+1</sub>* move high at the same time (for *i* = 3, *i* + 1 = 1).

The software should be written so as to easily recognize the unique output condition for each decimal point location as described above. It can do so by performing several rapid comparisons of the data lines, to determine which of them are simultaneously high. The flow chart given in the table outlines the algorithm used. □



## Waveform integrator averages over variable elapsed times

by Ron Vogel  
Northern Illinois University, Industry and Technology Department, De Kalb, Ill.

Finding the long-term average voltage of a waveform is much more difficult when the signal averaging must be done over a variable rather than a fixed time. But the average value of any signal sampled over an interval of 1 minute to 2 hours can be found easily with this circuit, which performs the task with the aid of an integrator-oscillator, an up-down counter, and a digital-to-analog converter. The basic transfer function relating output voltage  $V_o$  to input voltage  $V_{in}$  at time  $t$ :

$$V_o = \frac{1}{t} \int_0^t V_{in}(t) dt \quad (1)$$

is generated when feedback is implemented and when circuit constants are selected with care.

For the circuit to perform integration, a simple feedback loop is required. A voltage-controlled oscillator is used to drive an up-down counter in this circuit, and the counter, in turn, has an effect on the VCO frequency. The frequency of the VCO is determined by  $V_{in}$  and reference voltage  $V_{ref}$ . The oscillator is so configured that its

output frequency (point A) is:

$$f_o = \frac{K_1 V_{in}}{V_{ref}} = \frac{K_1 (V_{in} - V_{out})}{V_{ref}} \quad (2)$$

where  $K_1$  is a constant. Thus the up-down counter increments at a rate of  $f_o$  when  $V_{in}$  is positive and decrements at the same rate when  $V_{in}$  is negative.

The contents of the counter at any time  $t$  is therefore:

$$B = \int_0^t f_o dt = K_1 \int_0^t \frac{V_{in} - V_o}{V_{ref}} dt \quad (3)$$

Now, the ramp- and output-voltage equations are:

$$V_{ref} = K_2 t \quad (4)$$

$$V_o = K_3 B \quad (5)$$

where  $K_2$  and  $K_3$  are, respectively, the initial amplitude of the ramp and the proportionality constant of the d-a converter.

When Eq. 4 is substituted into Eq. 3 and thence into Eq. 5, and when circuit constants are selected so that  $K_1 K_3 = K_2$ , then:

$$V_o = \int \frac{V_{in} - V_o}{t} dt \quad (6)$$

Differentiating and rearranging this equation yields:

$$V_o + t \frac{dV_o}{dt} \equiv \frac{d}{dt} (V_o t) = V_{in} \quad (7)$$

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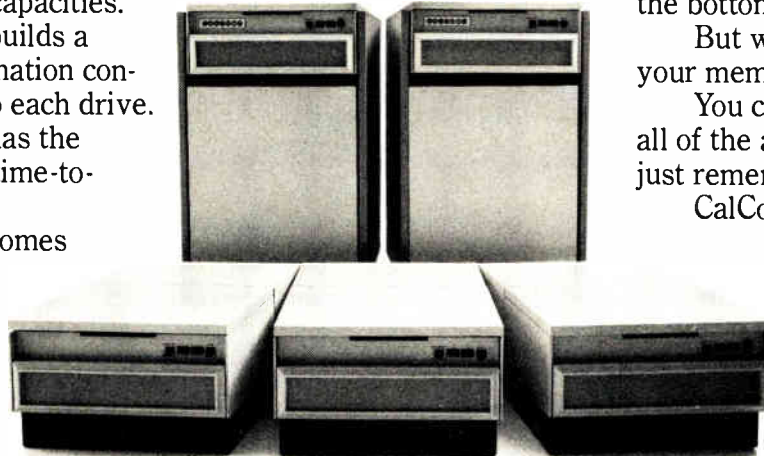
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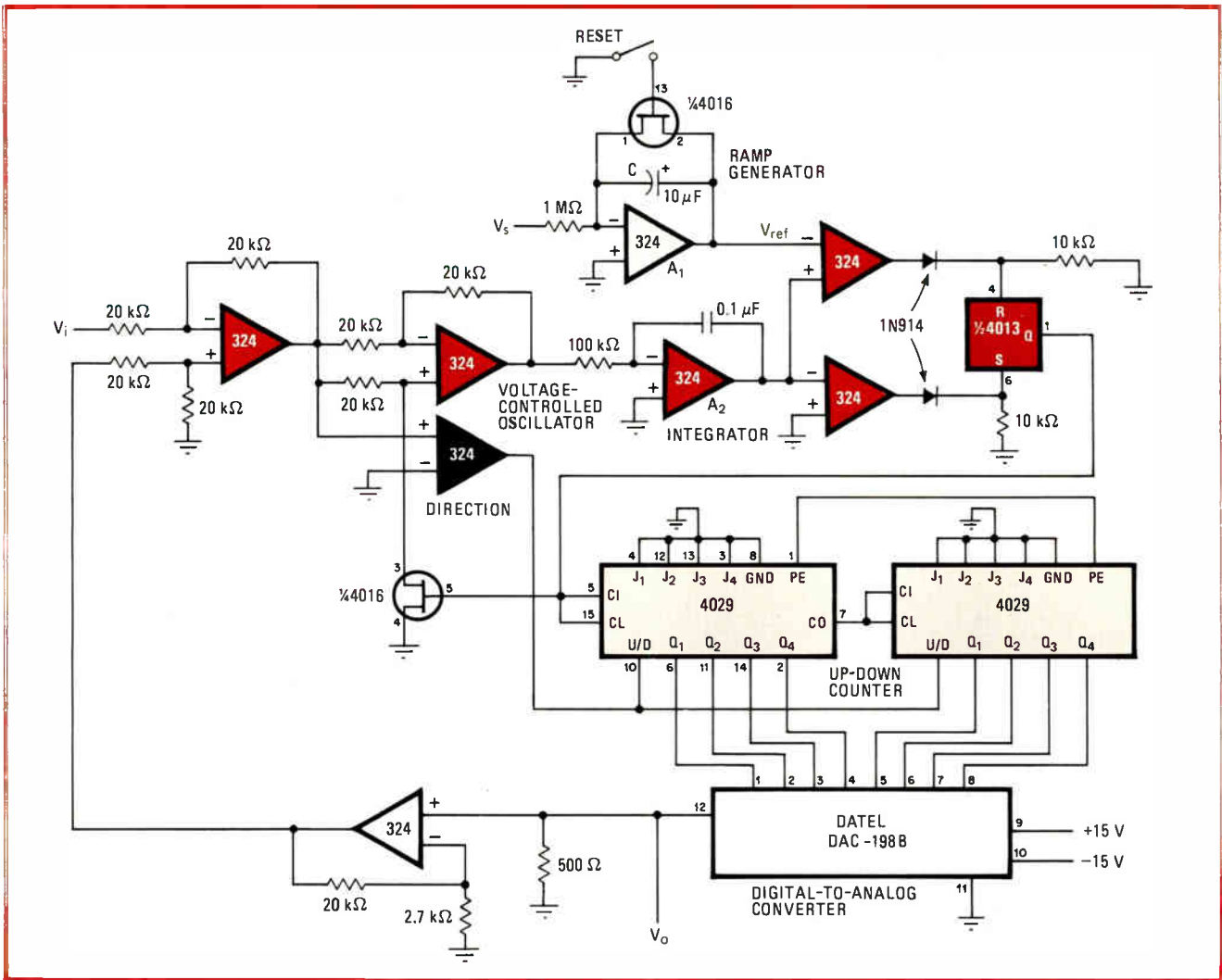
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**True average.** Circuit finds average voltage of waveforms sampled over interval of 1 minute to 2 hours. Averaging time is determined by C. Averaged voltage is in digital form at the output of the up-down counter, in analog form at the output of the d-a converter.

and this equation reduces to Eq. 1 when integrated.

The actual circuit uses all standard components. The ramp generator ( $A_1$ ) is a standard integrator circuit, which is reset at the start of a timing interval. In this application, however, the integrator requires a low-leakage integrating capacitor. A maximum integration time of 1 hour can be achieved with a 10-microfarad capacitor and an integrator input voltage of 0.03 volt.

The voltage-controlled oscillator is somewhat unusual. Any input voltage, positive or negative, will cause integrator  $A_2$  to ramp in the positive direction starting from the initial  $V_{in}$  potential and will also drive the 4013 flip-flop high. The logic 1 generated at the Q output will increment or decrement the counter. When the ramp voltage from  $A_2$  reaches  $V_{ref}$ , the flip-flop will be reset, generating a feedback voltage that causes  $A_2$  to ramp in the negative direction at the same rate it rose. When the ramp reaches ground potential,  $A_2$  prepares to integrate  $V_{in}$  once more. The instantaneous value of  $V_{in}$  is again introduced into the integrator, and the process is repeated until the ramp generated by  $A_2$  fails to reach the signal produced by  $A_1$ , which is slowly rising toward the positive supply voltage; this will be recognized as the

end of the sampling interval. The contents of the 4029 counter or Datal 198B d-a converter can, of course, be observed at any time. The averaged voltage will be in digital form at the output of the counter or may be obtained in analog form at the output of the d-a converter.

In practice, the minimum value of  $V_{ref}$  should always be above ground potential. The lower limit, in general, will be determined by the response time and frequency capability of the particular vco used. The ramp slope can then be selected so that  $V_{ref}$  will be less than the supply voltage for the longest averaging time expected. Of course, since  $V_{ref}$  cannot start from zero, an error will be observed at the output when the analog signal is first processed (that is, for small values of  $t$ ).

The highest frequency at which the vco can cycle is 10 kilohertz. At this rate, the maximum measurement error will be 1% after 2 minutes if the maximum averaging time is 1 hour. Accuracy will improve with time and will be directly proportional to the vco frequency. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay \$50 for each item published.

## Why not a cascode optocoupler?

In solid-state optocouplers, which are being used increasingly in analog as well as digital circuits, the speed of response and gain are mostly governed by the photosensor, either a photodiode or phototransistor. Couplers with phototransistors provide a high transfer ratio (gain), but there's a loss in speed due to Miller feedback capacitance. So instead, high-speed optocouplers often use a photodiode followed by high-speed amplifiers.

But S. Ashok of Rensselaer Polytechnic Institute's electrical and systems engineering department points out that an overlooked alternative, **one that could improve speed of optocoupler circuits while maintaining gain, is the cascode configuration.** In this configuration the collector of the phototransistor is tied to the emitter of the cascode output transistor while the base of the latter is tied to a constant voltage source, reducing the Miller capacitance significantly. The load is connected to the collector of the cascode output transistor. So far as Ashok is aware, no one manufactures such an optocoupler.

## Back to the kitchen for a new circuit substrate

Are you looking for a low-cost substitute for hybrid alumina substrates or epoxy-glass pc boards? Porcelainized steel, long familiar in appliances, could well be it. **In terms of a complete circuit, porcelainized steel at 23 cents compares with a printed-circuit board at \$1.00 and an alumina-based circuit at \$1.60.** In terms of bare material, a 4-by-4-inch piece of porcelainized steel costs 12¢ while an identically sized piece of alumina costs \$1.39. The new substrate would be useless as a circuit board without conductors, resistors, dielectrics, and an overglaze, of course. So Electro Materials Corp. of America, Mamaroneck, N. Y., has already developed modified screenable thick-film materials of the types mentioned, which can be fired onto the porcelain-covered steel.

## Watch out for hot plastics

If you are designing with subminiature switches, don't forget that soldering could damage them. Switches that will be mounted on a printed-circuit board rather than a panel require plastic parts that can resist high temperatures. For instance, engineers at Alco Electronic Products in North Andover, Mass., recently designed a plunger insulator with a steel shaft and a polyamide tip for a new pc-mounted subminiature slide switch. This tip was perfectly satisfactory mechanically and electrically but melted when the switch was soldered at 600°F. Alco's solution was to mold the tip out of a Du Pont material called Vespel. Made from KS aramid and polyimide resins, **Vespel has a temperature limit of 900°F.**

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Jerry Lyman



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Buffered Translator	Open Construction Base Mounted			X
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Preset Indexer	Packaged	X	X	X
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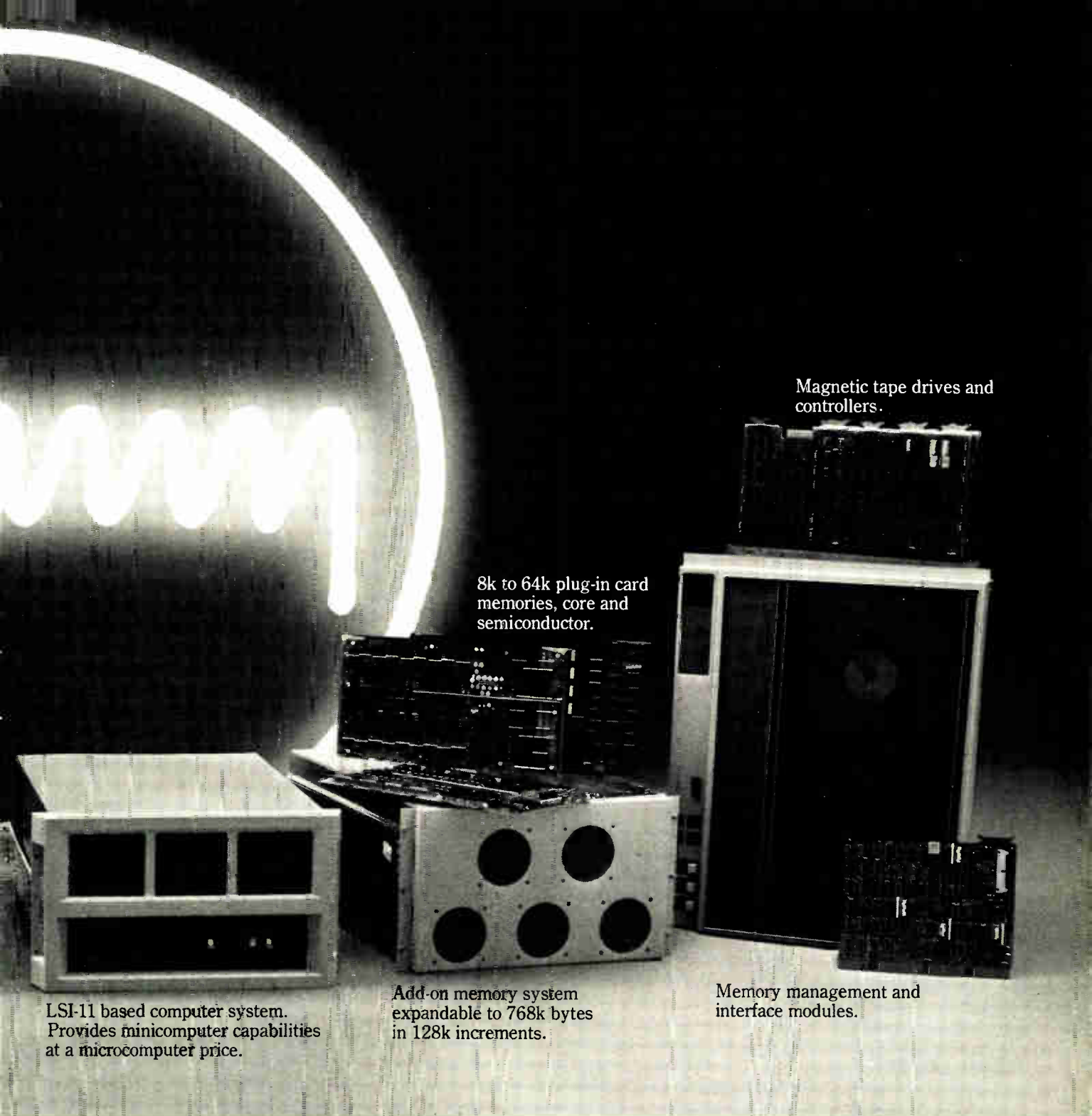


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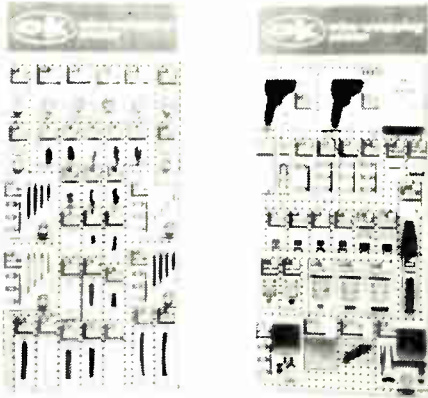
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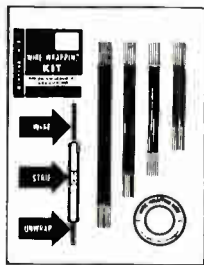
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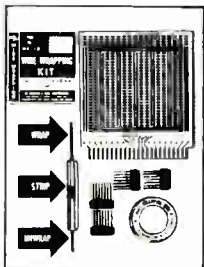
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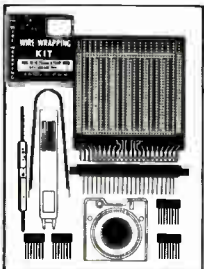
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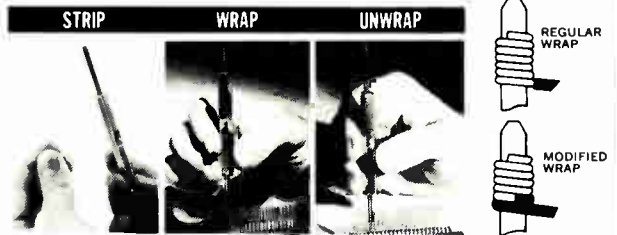
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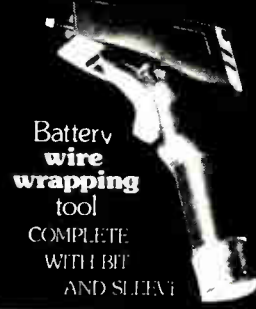


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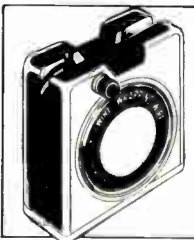
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30 AWG White Wire 4" Long	30 W 50 040	\$1.23
30 AWG Red Wire 4" Long	30 R 50 040	\$1.23
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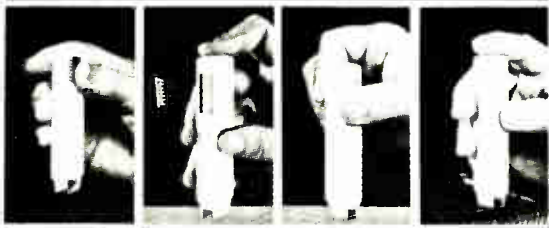
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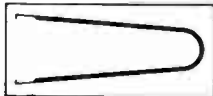
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The 4 x 4.5 x 1/16 inch board is made of glass coated EPOXY Laminated and features solder coated 1 oz. copper pads. The board has provision for a 22/44 two sided edge connector, with contacts on standard .156 spacing. Edge contacts are non-dedicated for maximum flexibility.



The board contains a matrix of .040 in. diameter holes on .100 inch centers. The component side contains 76 two-hole pads that can accommodate any DIP size from 6-40 pins, as well as discrete components. Typical density is 18 of 14-Pin or 16-Pin DIP's. Components may be soldered directly to the board or intermediate sockets may be used for soldering or wire-wrapping.

Two independent bus systems are provided for voltage and ground on both sides of the board. In addition, the component side contains 14 individual busses running the full length of the board for complete wiring flexibility. These busses enable access from edge contacts to distant components. These busses can also serve to augment the voltage or ground busses, and may be cut to length for particular applications.

Hobby Board    H-PCB-1    \$4.99

### PC CARD GUIDES



TR-1 consists of 2 guides precision molded with unique spring finger action that dampens shock and vibration, yet permits smooth insertion or extraction. Guides accommodate any card thickness from .040-100 inches.

QUANTITY - ONE PAIR (2 pcs.)

Card Guides    TR-1    \$1.89

### PC CARD GUIDES & BRACKETS

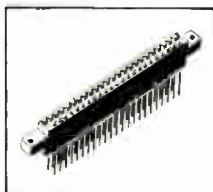


TRS-2 kit includes 2 TR-1 guides plus 2 mounting brackets. Support brackets feature unique stabilizing post that permits secure mounting with only 1 screw.

QUANTITY - ONE SET (4 pcs.)

Guides & Brackets    TRS-2    \$3.79

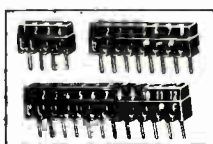
### PC EDGE CONNECTOR



44 Pin, dual read out, .156" (3.96 mm) Contact Spacing, .025" (0.63 mm) square wire-wrapping pins.

P.C. Edge Connector    CON-1    \$3.49

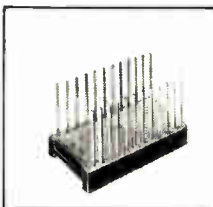
### P.C.B. TERMINAL STRIPS



The TS strips provide positive screw activated clamping action, accommodate wire sizes 14-30 AWG (1.8-0.25mm) Pins are solder plated copper, .042 inch (1mm) diameter, on .200 inch (5mm) centers.

4-Pole	TS- 4	\$1.39
8-Pole	TS- 8	\$1.89
12-Pole	TS-12	\$2.59

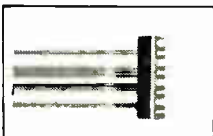
### DIP SOCKET



Dual-in-line package, 3 level wire-wrapping, phosphor bronze contact, gold plated pins .025 (0.63mm) sq., .100 (2.54mm) center spacing.

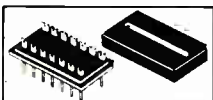
14 Pin Dip Socket	14 Dip	\$0.79
16 Pin Dip Socket	16 Dip	\$0.89

### RIBBON CABLE ASSEMBLY SINGLE ENDED



With 14 Pin Dip Plug 24" Long (609mm)	SE14-24	\$3.55
With 16 Pin Dip Plug 24" Long (609mm)	SE16-24	\$3.75

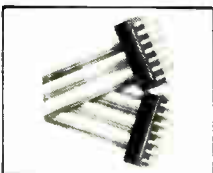
### DIP PLUG WITH COVER FOR USE WITH RIBBON CABLE



14 Pin Plug & Cover	14-PLG	\$1.45
16 Pin Plug & Cover	16-PLG	\$1.59

QUANTITY: 2 PLUGS, 2 COVERS

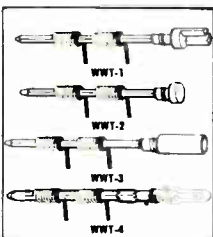
### RIBBON CABLE ASSEMBLY DOUBLE ENDED



With 14 Pin Dip Plug -2" Long	DE 14-2	\$3.75
With 14 Pin Dip Plug -4" Long	DE 14-4	\$3.85
With 14 Pin Dip Plug -8" Long	DE 14-8	\$3.95
With 16 Pin Dip Plug -2" Long	DE 16-2	\$4.15
With 16 Pin Dip Plug -4" Long	DE 16-4	\$4.25
With 16 Pin Dip Plug -8" Long	DE 16-8	\$4.35

### TERMINALS

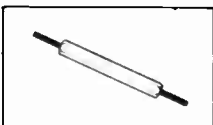
- .025 (0.63mm) Square Post
- 3 Level Wire-Wrapping
- Gold Plated



Slotted Terminal	WWT-1	\$2.98
Single Sided Terminal	WWT-2	\$2.98
IC Socket Terminal	WWT-3	\$3.98
Double Sided Terminal	WWT-4	\$1.98

25 PER PACKAGE

### TERMINAL INSERTING TOOL



For inserting WWT-1, WWT-2, WWT-3, and WWT-4 Terminals into .040 (1.01 mm) Dia. Holes.

INS-1    \$2.49

### WIRE CUT AND STRIP TOOL



Easy to operate... place wires (up to 4) in stripping slot with ends extending beyond cutter blades... press tool and pull... wire is cut and stripped to proper "wire-wrapping" length. The hardened steel cutting blades and sturdy construction of the tool insure long life.

Strip length easily adjustable for your applications.

DESCRIPTION	MODEL NUMBER	ADJUSTABLE "SHINER" LENGTH OF STRIPPED WIRE		Price
		INCHES	TO INCHES	
24 ga. Wire Cut and Strip Tool	ST-100-24	1 1/4"	1 3/4"	\$ 8.75
26 ga. Wire Cut and Strip Tool	ST-100-26	1 1/4"	1 1/2"	\$ 8.75
26 ga. Wire Cut and Strip Tool	ST-100-26-875	7/8"	1 1/8"	\$ 8.75
28 ga. Wire Cut and Strip Tool	ST-100-28	7/8"	1 1/2"	\$11.50
30 ga. Wire Cut and Strip Tool	ST-100-30	7/8"	1 1/2"	\$11.50

THE ABOVE LIST OF CUT AND STRIP TOOLS ARE NOT APPLICABLE FOR NYLON OR TEFLON INSULATION

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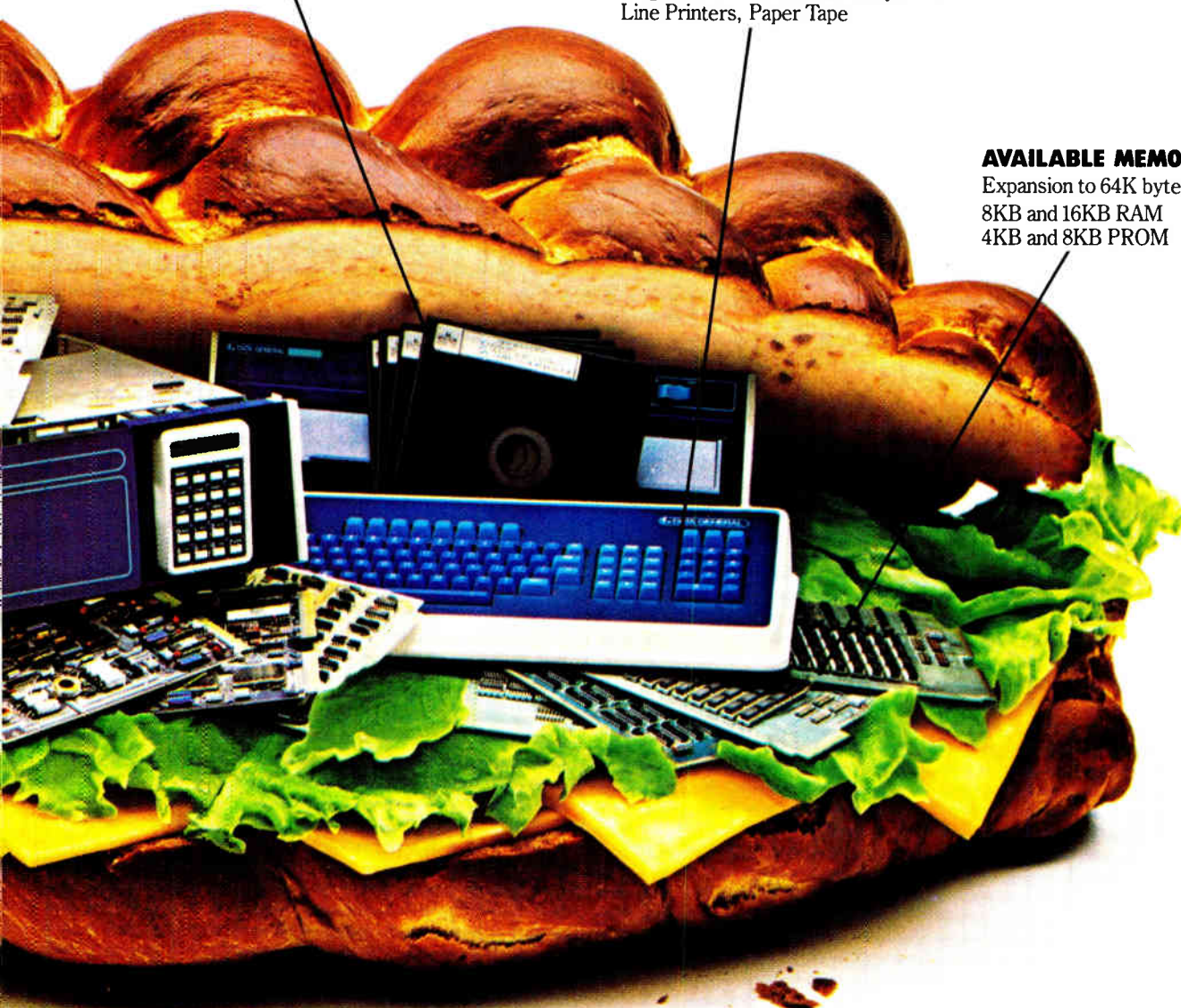
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## New products

notes, opens up a wide range of applications for the unit in digitally controlled gain or attenuator circuits, synchro-to-digital converters, and ratiometric low-power converters, as well as digitally controlled power supplies.

Requiring only a single +15-v power supply, the AD7541 draws a maximum supply current of 2 mA, making it suitable for battery-operated and other low-power equip-

ment. Its inputs are scaled to interface with either transistor-transistor or C-MOS logic levels. For the device's current output, settling time is 500 ns typically, 1  $\mu$ s maximum. At 10 kHz, feedthrough error is less than  $\pm 1/2$  least significant bit.

Key to the unit's high performance and small size—the chip measures just 100 by 82 mils—are its double-layer metalization, ion-implanted critical geometries, and laser

wafer trimming of its on-chip thin-film resistors. Housed in an 18-pin plastic or ceramic dual-in-line package, the AD7541 is pin-compatible with the AD7521, an earlier 12-bit part offering up to 10-bit accuracy.

In all, the AD7541 comes in six different versions, consisting of three temperature grades and two linearity grades, either  $\pm 0.01\%$  (12 bits) or  $\pm 0.02\%$  (11 bits). The commercial parts, the JN and KN versions, are

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intended for operation over the temperature range of 0°C to 70°C, and they sell for \$11 and \$12 apiece, respectively, in quantities of 1,000 and up. The AD and BD versions, which are priced respectively at \$15 and \$16 each in the same quantities, are the industrial parts for operation from -25°C to +85°C. Intended for the military temperature range of -55°C to +125°C, the SD and TD versions sell for \$44 and \$49 per

device, respectively, also for quantities of 1,000 or more.

In the near future, says Van Aken, the Limerick facility intends to make available for purchase a buffered version of the AD7541 for micro-computer applications, as well as a buffered version of its newly released AD7523, an 8-bit multiplying current-output d-a chip selling for only \$2 in 1,000-and-up lots [*Electronics*, Feb. 16, p. 182]. Sample quantities

of any version of the AD7541 are available from stock.

For sales engineering information, the company suggests contacting Jeff Riskin, an applications engineer at the firm's semiconductor facility located at 829 Woburn St. in Wilmington, Mass. 01887. The telephone number is (617) 935-5565.

Analog Devices Inc., Route 1 Industrial Park, P. O. Box 280, Norwood, Mass. 02062. Phone (617) 329-4700 [338]

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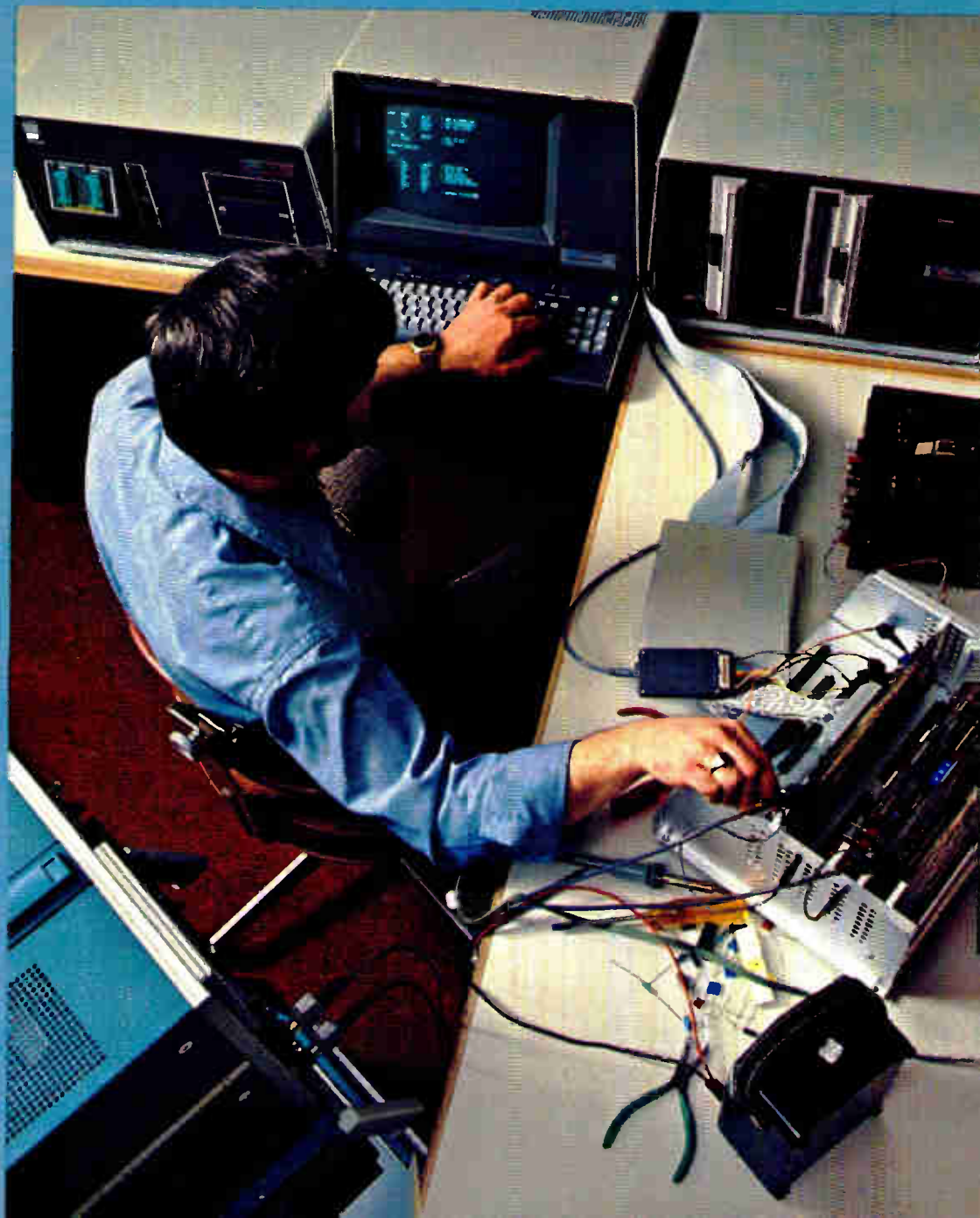
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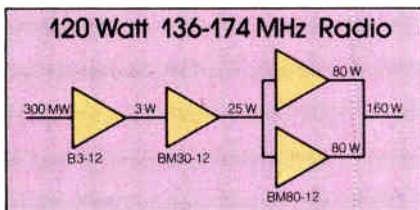
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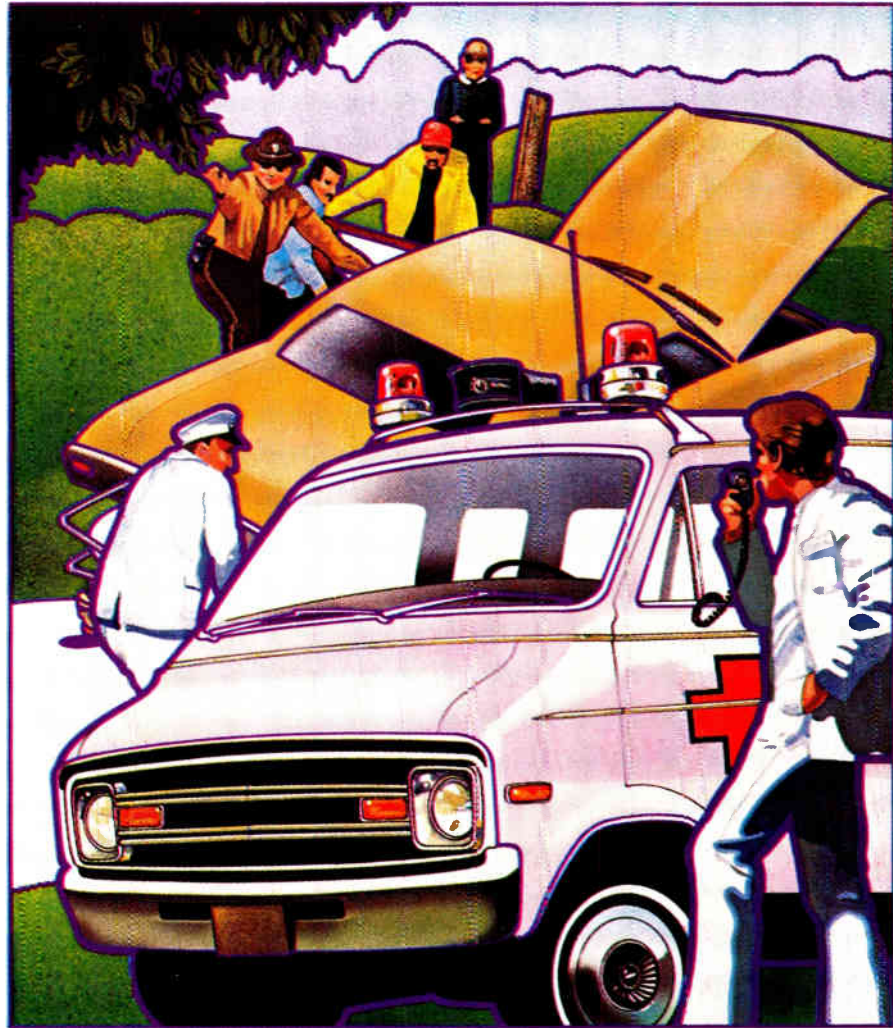
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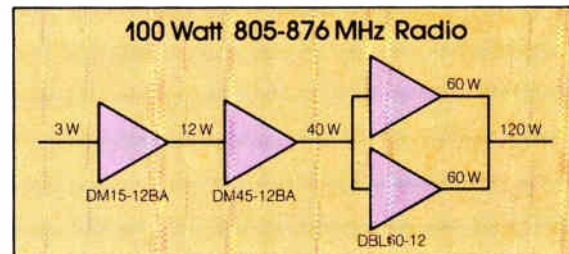
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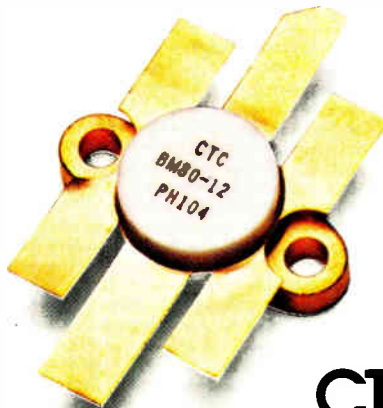
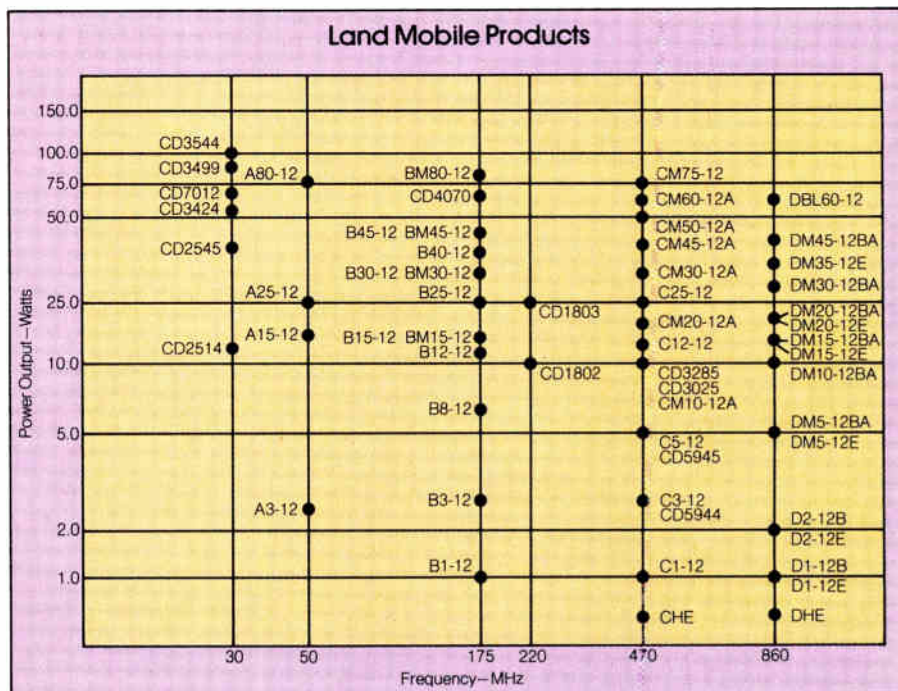


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## New products

Packaging & production

### Laser trimmers get faster

Teradyne's latest system has a peak rate of about 50,000 resistors an hour

With manufacturers of thick-film hybrid microcircuits wanting ever-faster throughput in trimming the resistors and networks on a substrate, the W411 laser-trim system from Teradyne Inc. is aimed squarely at a ready market [*Electronics*, Jan. 19, p. 33]. In a recent simulation of production conditions, the W411 hit a peak rate of more than 50,000 resistors trimmed in an hour. Teradyne officials say that translates into more than \$400 worth of shippable parts per hour.

Engineers at the Boston-based manufacturer of test and manufacturing equipment for microelectronic parts and circuit boards concentrated on several factors to boost the throughput of the W411 over that of its previous fastest machine, the W311C. Chip Thayer, product manager for Teradyne's laser trim group, says the big contributors to the higher output are reductions in time

taken in loading and handling parts, trimming, beam positioning, and testing and measuring.

Handling and loading time are cut by putting a larger work table on the new system. The table can accommodate nine substrates measuring 2 by 2 in. instead of the four for the earlier unit. "That cuts handling time about in half," Thayer says.

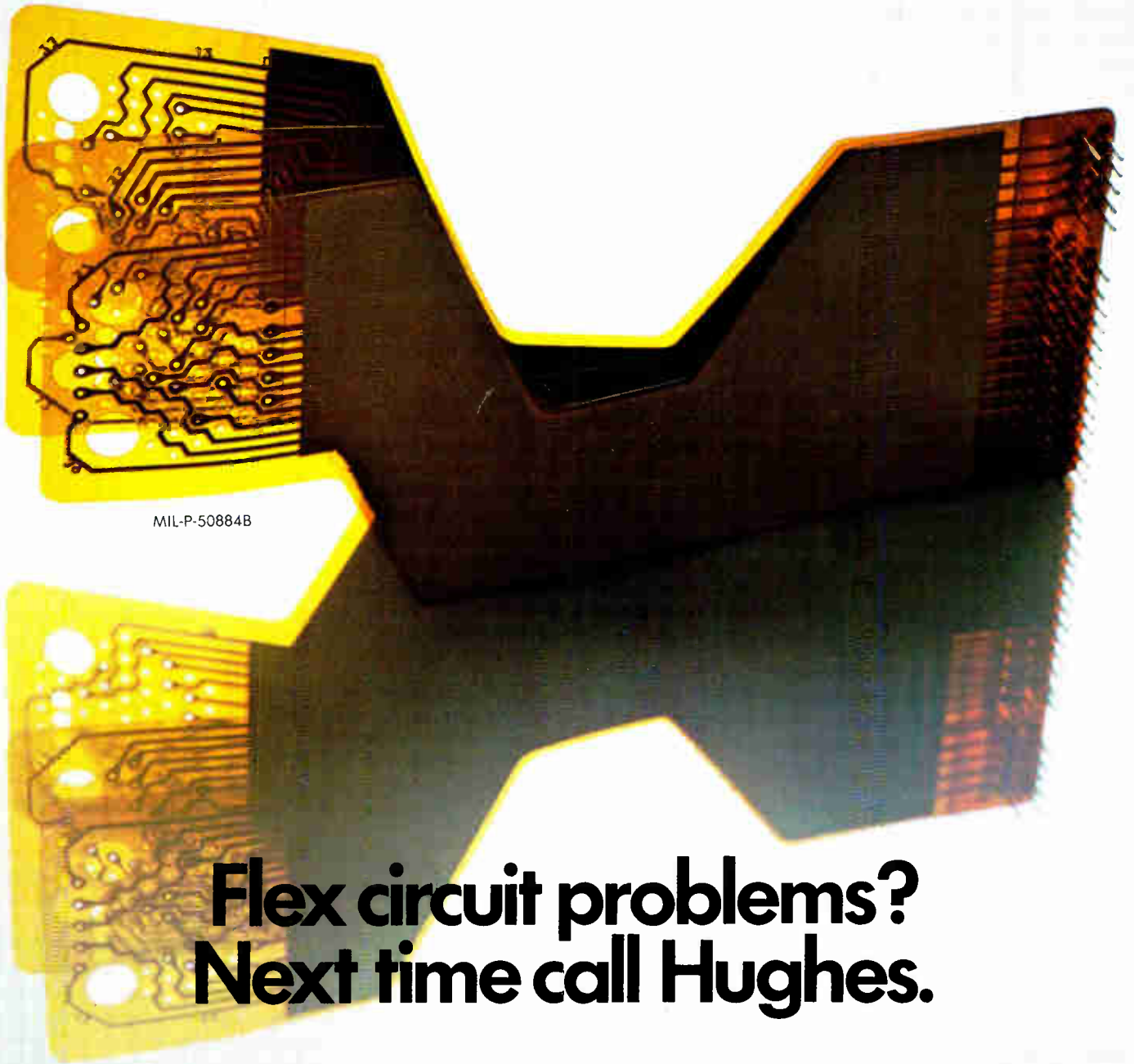
Actual loading time has not changed between the two systems, but the larger work table on the new unit means loading time is spread over a larger number of parts. Furthermore, use of only a step-and-repeat handler on the W411 maximizes handling speed. The earlier system offers a choice of two slower handlers as well as the step-and-repeat device.

Trimming time has been reduced by using a neodymium-YAG laser that delivers 5.5 w of power in the fundamental mode vs 2.5 w for the older system. Thayer says the more powerful laser has a higher energy density, permitting faster cutting.

The W411 incorporates the galvanometer beam positioner used in later versions of the W311C, which reduces beam-positioning settling time by a factor of three to four compared with an earlier beam positioner. The new positioner will withstand acceleration forces of 400 g, twice that of the W311C, which doubles the beam's traveling speed.







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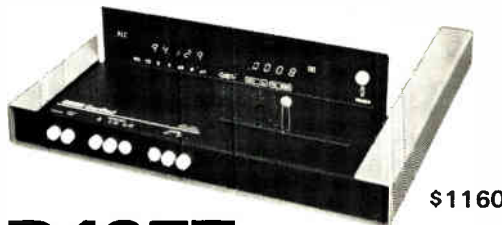
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### New products

The faster movement and settling times are illustrated in representative cycle times to trim a multiple-serpentine resistor array with 350 cuts. Excluding handling time, the W411 does that job in 6.7 seconds vs 24 seconds for the earlier beam positioner.

The W411 uses the same measurement instrumentation—a precision resistance bridge—as its predecessor, but the new system has a faster computing controller that speeds the computations made for the pretest and final test measurements. The controller also contributes to trim speed by permitting increased laser pulse-repetition rates.

Menu programming is a feature of the W411, as in its predecessor. "This permits anyone familiar with resistor trimming to set up a job quickly," says Thayer. The operator is presented with a set of commands from which he can choose on the cathode-ray-tube display, and is stepped through the job by being asked questions about such parameters as final resistance values, and length and direction of cuts. When the questions are answered, the job is ready to be debugged and run, or can be stored on a magnetic-tape cartridge for later use.

The trim system is expected to be priced above \$100,000. Orders will be accepted by the company early in the second quarter.

Teradyne Inc., 183 Essex Street, Boston, Mass. 02111. Phone Chip Thayer at (617) 482-2700 [391]

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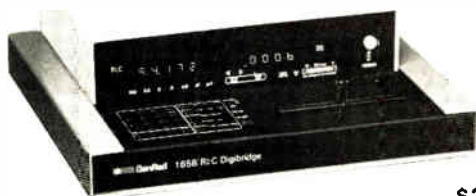


Circle 151 for literature  
Circle 229 for demonstration



GEORG SIMON OHM

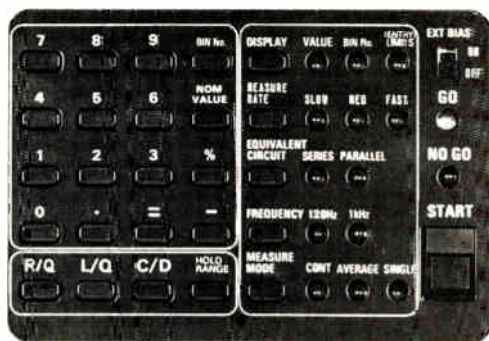
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- 0.1% accuracy for R, L, and C.
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- Five full-digit display for R, L, and C. Four full digits for D and Q. All numbers go to 9.
- Wide measurement ranges allow testing a greater number of component types.



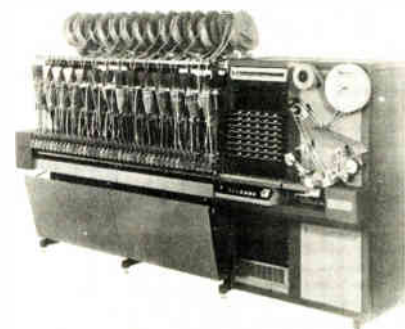
U.S.A. price only



**GenRad**

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### New products



axial form. The memory of the 2595's controller can store multiple sequencer programs, with instant access to any one. Programs can be edited on line to add or delete components, and new programs can be generated in a few minutes.

The sequencer automatically centers the components as they feed into the retaping unit. If a component is missed, the machine will stop and will display the number of the component-dispensing head so that an operator can replace it from a convenient makeup tray. Lead wires are trimmed by air-driven cutters that can shear 35-mil steel wire.

The basic 20-station sequencer has a floor outline of 2.83 by 7.96 feet. Each additional 20-station module adds 3.33 feet to the long dimension.

Universal Instruments Corp., Box 825, Binghamton, N. Y. 13902. Phone (607) 772-7522 [393]

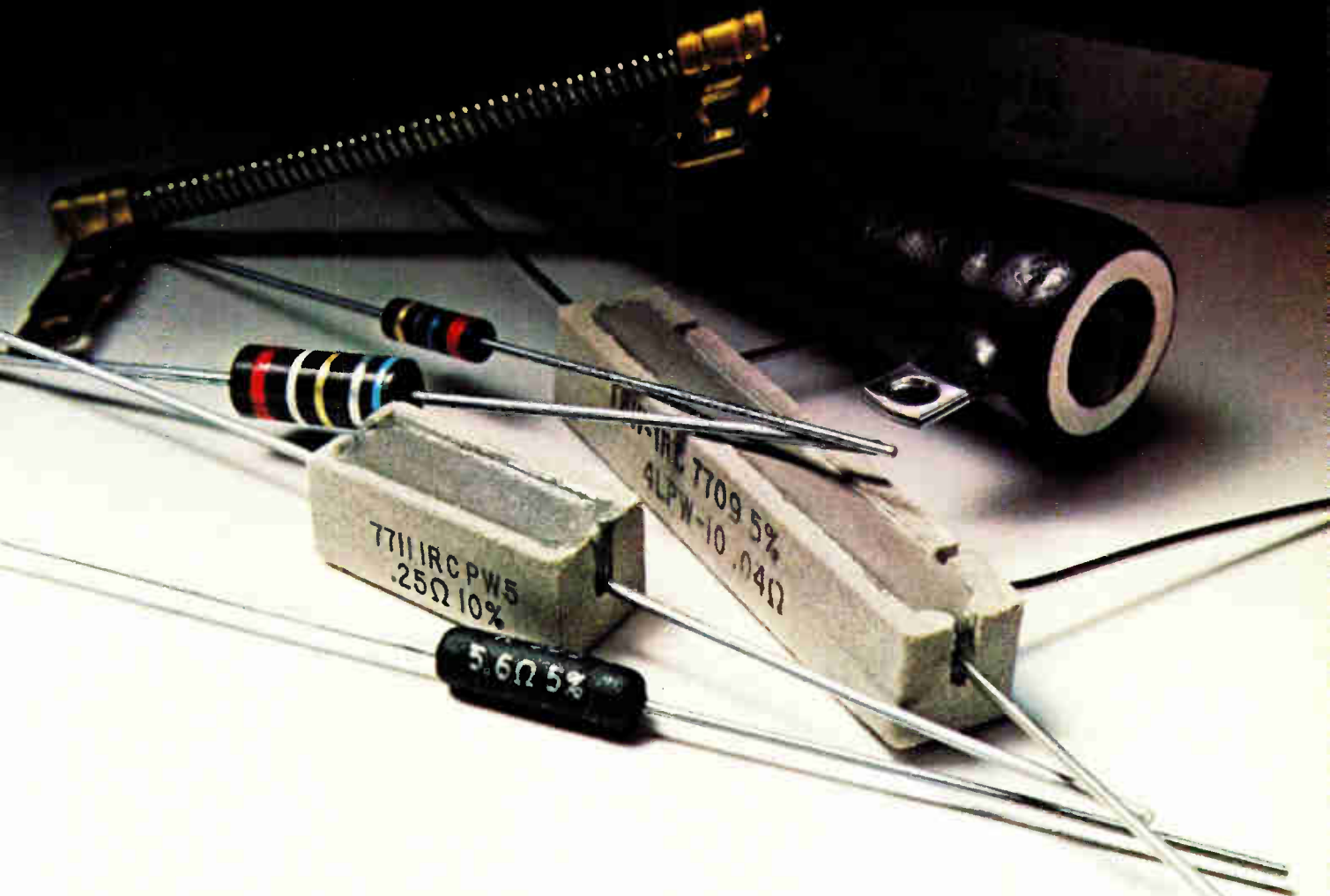
### Analog IC tester handles regulators to 5 A and 50 V

An automatic test system for analog integrated circuits (often called linear ICs by people who forget what "linear" means) provides rapid and precise testing of standard, special, and even unique devices. Among its unusual attributes is its ability to test voltage regulators at voltages to 50 v and currents to 5 A. Designated the model 1740, the system has a repertoire that includes operational amplifiers, differential amplifiers, sense amplifiers, comparators, and phase-locked loops.

The test limits, test conditions,

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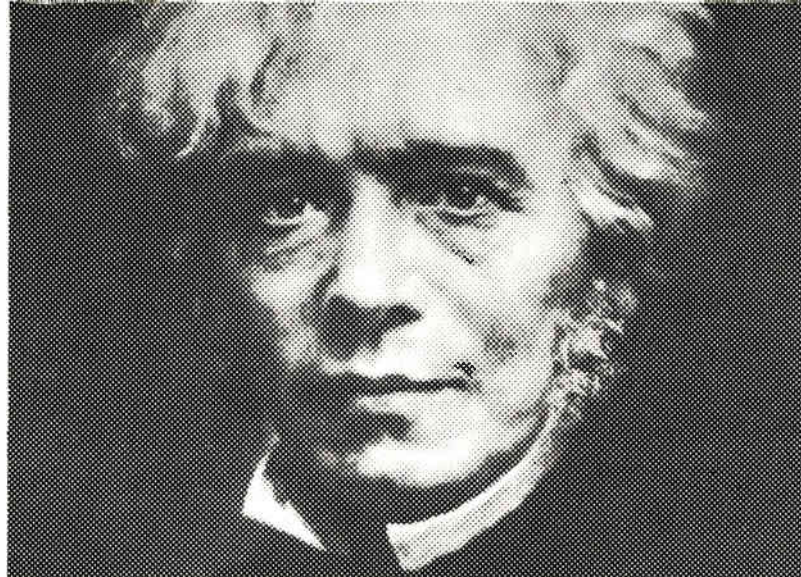
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- Automatic self-check/diagnostics on power-up.
- Five full-digit display for L and C. Four full digits for Q, D, R and G. All numbers go to 9.



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 **GenRad**

Circle 150 on reader service card

### New products



and any necessary special circuitry for testing any specific IC are all contained on a program board for the IC in question. Most limits and conditions are established by means of resistors. When 1% resistors are used, the nominal testing inaccuracy is 3%. When 0.05% units are employed, it drops to 1%.

Program boards can be prepared by the user or ordered from the factory. Factory-supplied boards include an error-analysis sheet.

In addition, the 1740 can be supplied with such options and accessories as a transfer-function analyzer, a manual programmer, and various adapters, extenders, cables, etc. The basic unit sells for \$8,950 and has a delivery time of eight weeks.

GenRad Inc., 300 Baker Ave., Concord, Mass. 01742. Phone (617) 369-4400 [394]

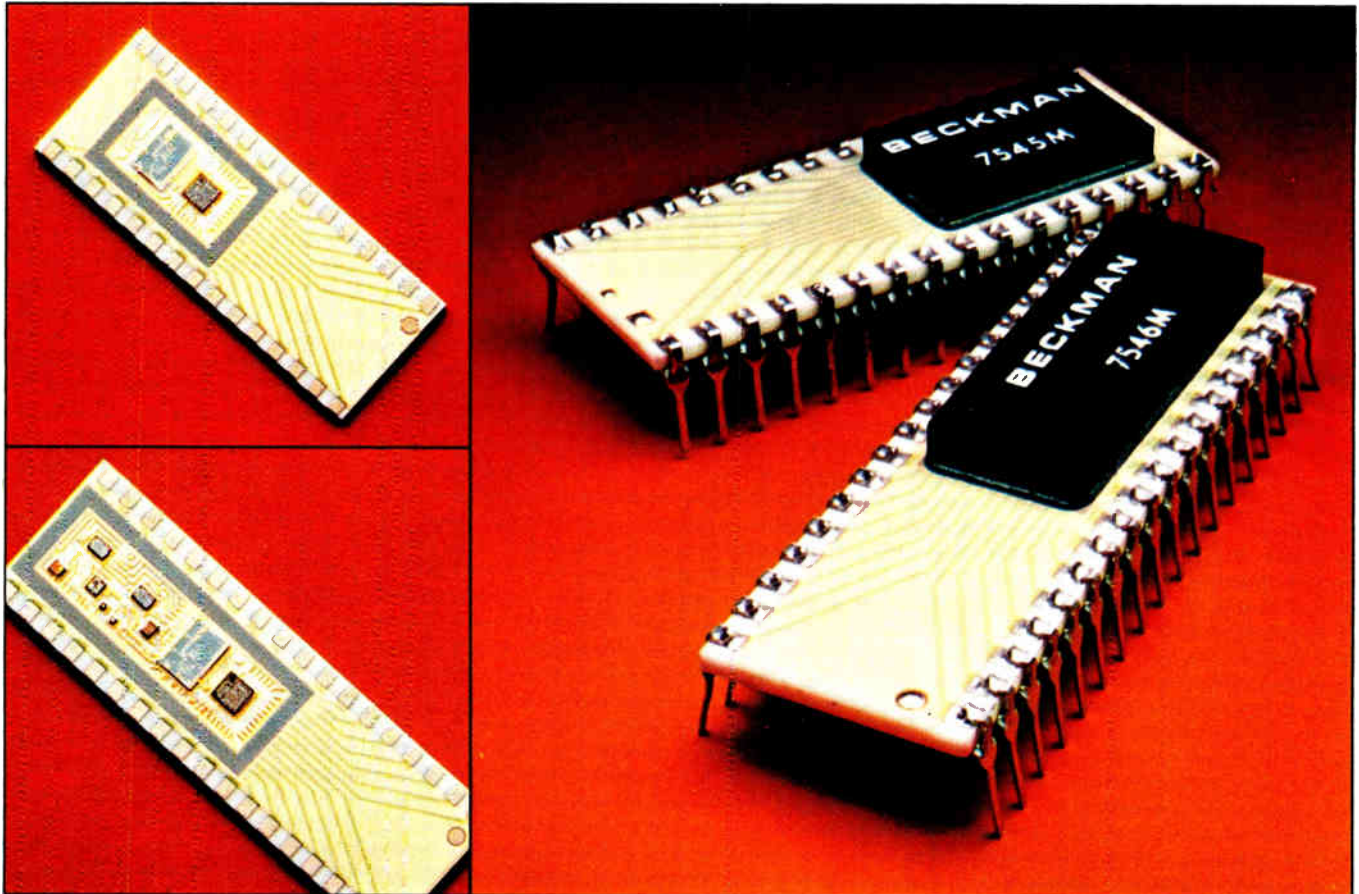
### Dynamic burn-in system holds up to 7,200 ICs

The System 6000 is a microprocessor-controlled dynamic burn-in integrated-circuit life-test system that is made up of two main components: a thermal chamber, better known as a test oven, and a control console, which the firm is calling the 6050 programmer-controller.

The chamber, which can function alone without the control console, holds up to 36 burn-in tray units in six functionally independent zones. Each tray holds as many as 200 ICs, depending upon configuration and type. The chamber includes a temperature controller and the system power supply.

The control console has a tape

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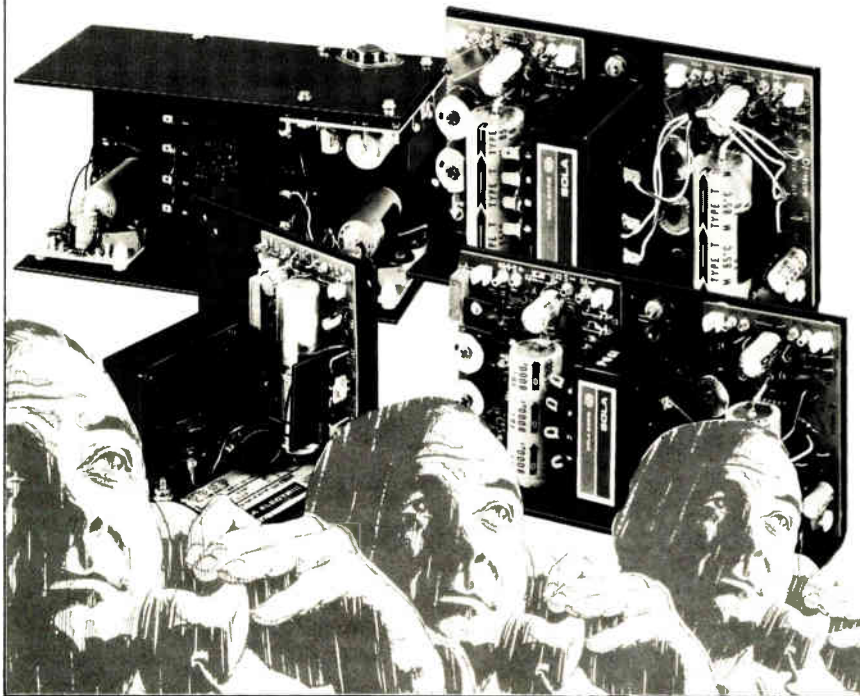
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## New products

cassette memory, a keyboard input, a cathode-ray-tube display, and an ambient-temperature test station for burn-in trays. Put the two pieces together and you can perform anything from simple static burn-in testing to complex dynamic measurements on the latest in very-large-scale integrated circuitry. Variable-power-supply, driver, and timing modules, all operating under microprocessor control, adapt the 6000 to any specified burn-in test. The system is available now.

Microtest Systems Inc., 1188 Bordeaux St., Sunnyvale, Calif. 94086. Phone (408) 745-7000 [395]

## Miniature connector works from $-65^{\circ}\text{C}$ to $+200^{\circ}\text{C}$

Designed with a scoop-proof feature that prevents contact damage in blind-mating applications, the KJL miniature circular connector meets the requirements of MIL-C-38999 and operates at temperatures from  $-65^{\circ}\text{C}$  to  $+200^{\circ}\text{C}$ . The connector is intended for use in demanding applications where small size, light weight, scoop-proof design, high contact density, and high reliability are key factors.

A total of 58 crimp, snap-in contact arrangements are available to accommodate from 3 to 128 contacts using wire sizes from AWG 16 through AWG 28. The gold-plated copper-alloy contacts are held in place by the a rear-release retention system. This approach uses a multiple-tine metal clip housed in a one-piece plastic insert.

KJL connectors are sealed by an interfacial seal with individual raised and tapered barriers around each pin contact, a peripheral seal, and a multiple-ripple wire-sealing grommet. Hermetic receptacles are also available. A typical price for a five-contact plug and receptacle is \$45.54 per mated pair in lots of 50 or more. Delivery time is 15 weeks.

International Telephone and Telegraph Corp., Cannon Electric Division, 666 East Dyer Rd., Santa Ana, Calif. 92702. Phone R. L. Harmon at (714) 557-4700 [396]



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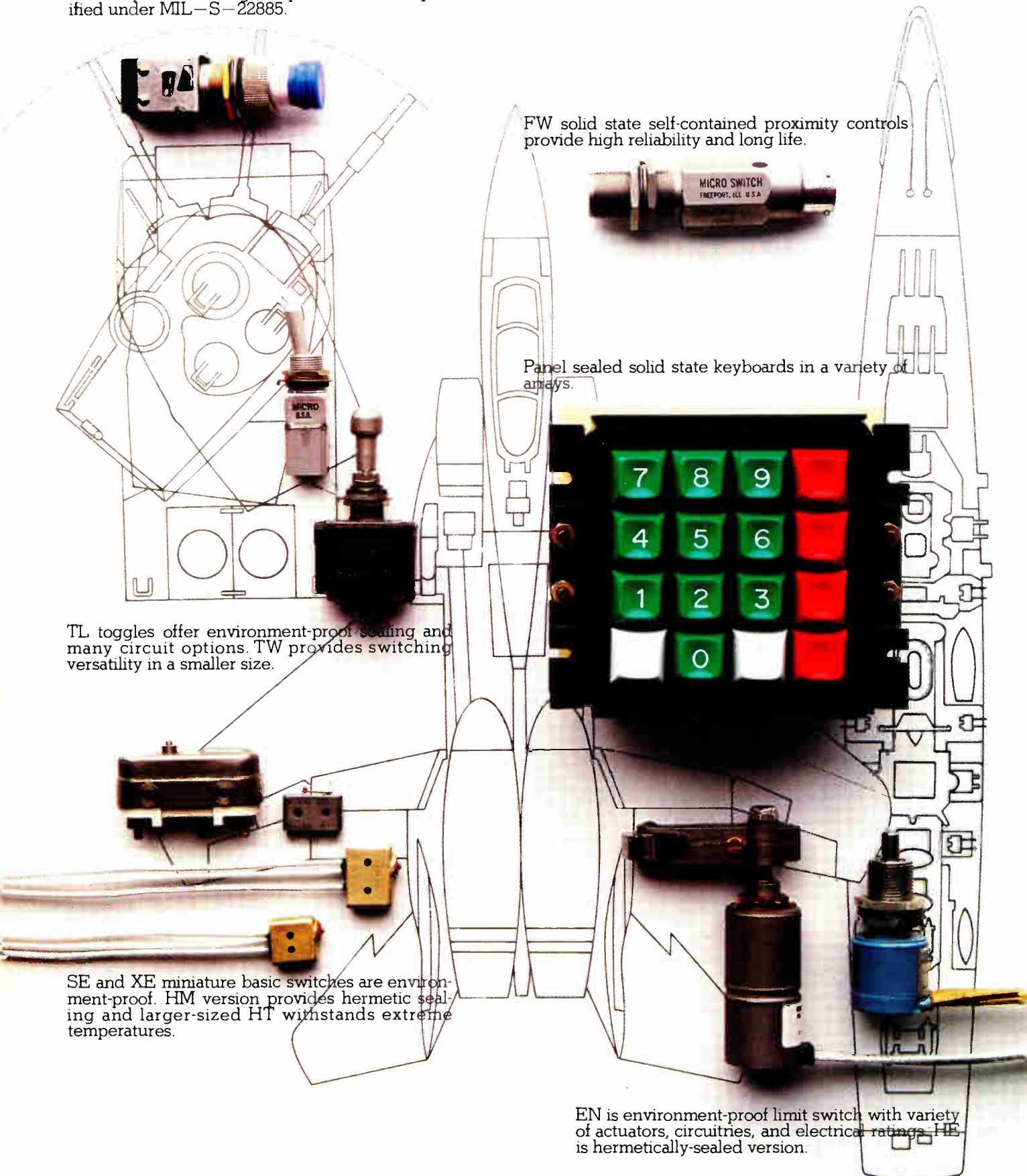
FW solid state self-contained proximity controls provide high reliability and long life.

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TL toggles offer environment-proof sealing and many circuit options. TW provides switching versatility in a smaller size.

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MICRO SWITCH also makes toggles with a variety of locking configurations and different-shaped levers, including colored tab levers. Integrated Wire Termination System is also available.

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## New products

Subassemblies

### Switcher supplies 25 W

Quad-output switching supply measures 2.5 by 4 by 6 in. and sells for only \$80

In selecting power supplies, the conventional viewpoint holds that switching types are good for 300-w aerospace applications or 150-w computer peripheral applications, but that they are too costly, noisy, and unreliable to compete with tried and true linear supplies at lower power levels. Now, however, Boschert Inc. says it is time to take a fresh look at the situation.

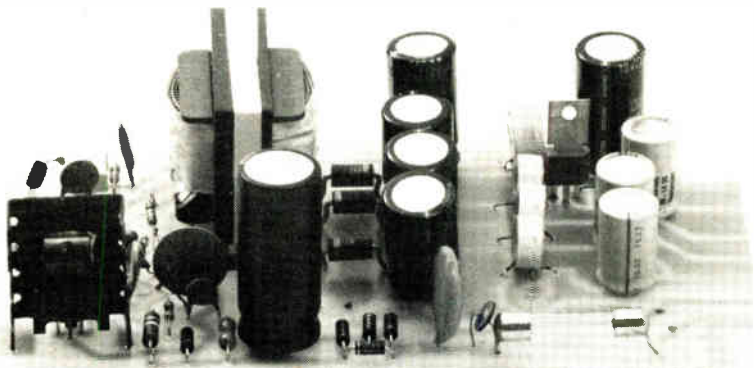
The company is introducing a 25-w switching power supply that challenges linear designs in terms of weight, size, and cost, according to Robert J. Boschert, president. Called the OL25, the new switcher is aimed at such applications as the low end of the microprocessor market, low-end cathode-ray-tube-display terminals, desktop calculators, or "almost any

piece of low-end electronic equipment that requires 25 watts," says Richard A. Keller, research and development engineering manager.

Because conventional series-regulated linear supplies dissipate about as much energy in the form of heat as they deliver to the load, they are only 30% to 50% efficient, Boschert points out. Moreover, the power is processed at 60 Hz, which not only can interfere with CRT circuitry, but also requires the use of large, heavy transformers and bulky filter capacitors, he adds.

In contrast, switching supplies are 70% to 80% efficient. Since they operate at 20 kHz, they require smaller transformers and filter capacitors. Their control circuitry, though, is more complex than that of a linear supply. For the designer, therefore, the choice may involve tradeoffs, as a linear does have some superior specifications—although the OL25 switcher is less sensitive to variations in line voltage, more immune to ac interruptions (making it ideal for microprocessor applications), and basically insensitive to changes in line frequency.

Preliminary specifications show that the OL25 is as good as, if not better than, most linears in a number



## New products

of parameters, according to Keller. Input line regulation is  $\pm 0.2\%$  maximum, input voltage range is 95 to 130 v rms, input frequency range is 47 to 440 Hz, and efficiency is typically 65%. Should a blackout occur, the unit's output remains within specification for a hold-up time of 16 milliseconds. For the +5-v output, the overvoltage-protection trip point is  $6.25 \pm 0.75$  v.

The tradeoffs begin in cross-regulation between outputs and in the unit's noise and ripple of 2% peak to peak, says Keller. Centering, which depends on the level of the output voltage, varies from  $\pm 5\%$  maximum for outputs of less than 40 v to  $\pm 2$  v for outputs of 40 v or more. All of these specifications, however, can be tightened on an extra-cost basis.

Boschert says the OL25, which

has four outputs terminated with a barrier strip, is smaller than comparable linears—it measures only 2.5 by 4 by 6 in. What's more, it is nine times lighter. The outputs are +5 v at 3.5 A,  $\pm 12$  v at  $\pm 0.5$  A, and -5 v at 0.5 A. The output voltages can be tailored to meet OEM requirements, up to  $\pm 40$  v on each output except the +5-v output.

To get the performance, Boschert employs a flyback design similar to that used in television sets or in automobile ignition systems, Keller says. "The significant point is that there's only one power switch and one power rectifier for each output," he adds. This proprietary concept minimizes cost and the number of magnetic parts and increases reliability. As Keller puts it, the underlying philosophy is "if a part's not there, it can't fail."

Price in 100-unit quantities will be about \$80 when delivery begins in April.

Boschert Incorporated, 384 Santa Trinita Ave., Sunnyvale, Calif. 94086 [381]

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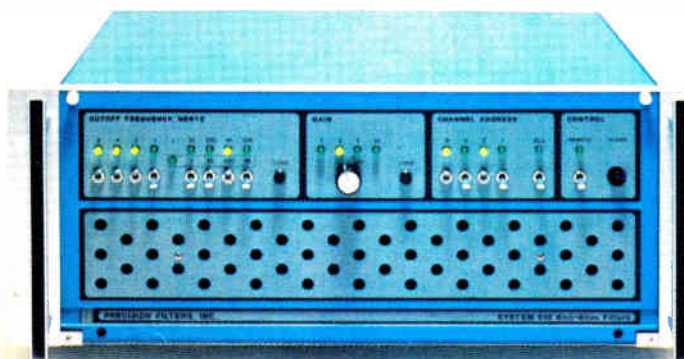


phase match is  $\frac{1}{2}^\circ$ , with worst case of  $2^\circ$ . You get performance that used to require a custom instrument, without paying a custom price. Call Don Chandler, 607-277-3550, or write for complete specs and a demonstration.



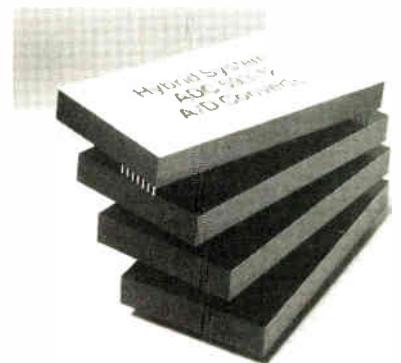
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12-bit, 4- $\mu$ s, hybrid a-d converter sells for \$199

The ADC593-12 is a 12-bit analog-to-digital converter with a typical conversion time of 3.5  $\mu$ s (4  $\mu$ s maximum) and a guaranteed throughput rate of 250 kHz. Accurate to within 0.0125%, the converter sells for \$199 in small quantities. Versatility is provided by three selectable digital output codes and four selectable input-voltage ranges. The unit's temperature coefficient of gain is no



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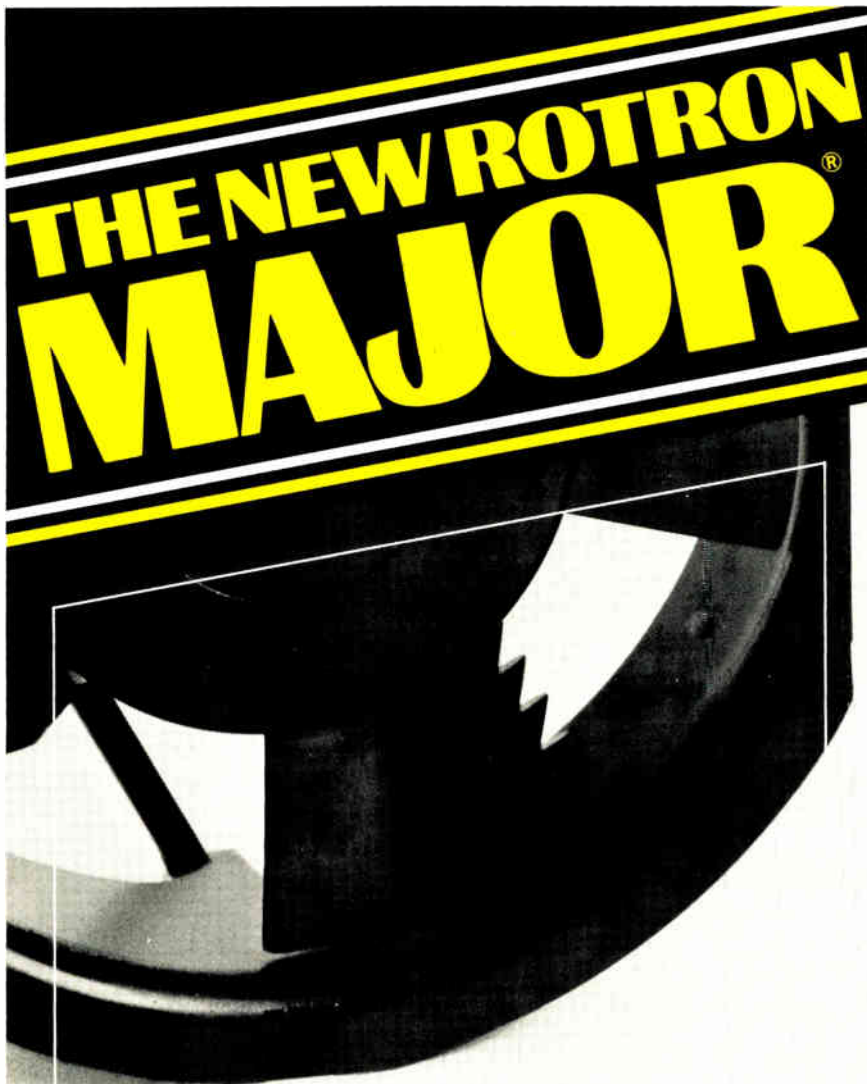
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### New products

more than 30 ppm per °C, and monotonicity is maintained from 0°C to 70°C.

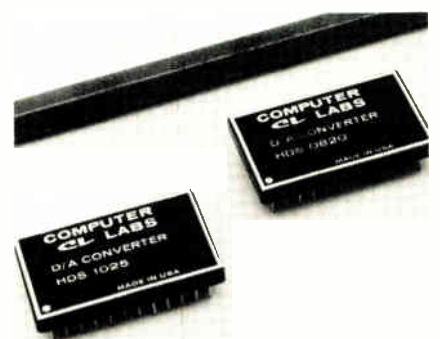
The unit is a complete successive-approximation converter: it includes a digital-to-analog converter, a clock, a comparator, a reference source, and a successive-approximation register. Its overall dimensions are 2 by 4 by 0.4 inches. Delivery is from stock.

Hybrid Systems Corp., Crosby Drive, Bedford, Mass. 01730. Phone Larry Lauenger at (617) 275-1570 [383]

### \$119 d-a converter offers 25-ns, 10-bit performance

Although it carries a small-quantity price tag of only \$119, the HDS-1025 digital-to-analog converter is an extremely fast 10-bit unit: it settles to within 0.1% of full scale within a maximum of 25 ns in its current-output mode. In its voltage-output mode, with a 75-Ω load, the settling time is 35 ns.

A companion converter, the HDS-0820, offers 8-bit resolution and a settling time to within 0.4% of full scale of 20 ns. Priced at \$109, it has a 75-Ω voltage-mode settling time of 30 ns to within 0.4%



Both converters are laser-trimmed hybrids capable of putting out 10 mA. They feature a power consumption of 750 mw and a total volume of 0.166 cubic inch. Both are housed in 24-pin dual in-line packages. For extremely high reliability, the converters are available with processing and screening to MIL-STD-883,

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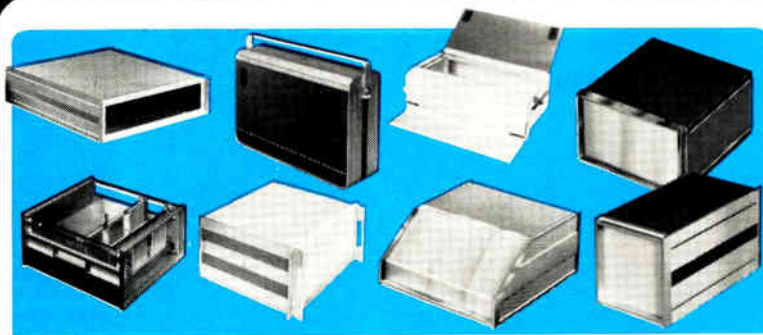
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## New products

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A matched pair of fast 8-bit data-acquisition-system components—a hybrid sample-and-hold amplifier and a hybrid analog-to-digital converter—together provide a throughput rate of 900,000 conversions per second. The SH-8518 video sample-and-hold unit has a 25-ns acquisition time, a 60-ps aperture uncertainty time, and a 20-MHz sampling rate. Its maximum linearity error is 0.05% and its droop rate is 1 mV/μs. The self-contained unit contains a FET buffer amplifier.

The ADH-8512 a-d converter is a successive-approximation unit with a conversion time of 1 μs and a maximum nonlinearity of 0.2%. It can be pin-programmed for six input-voltage ranges and can deliver

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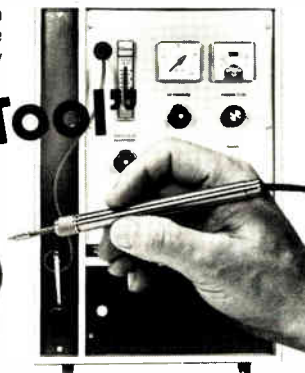
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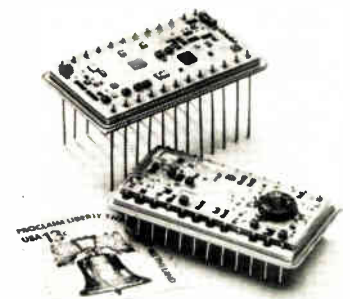
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its digital output in either parallel or serial form.

Both modules are supplied in hermetic 24-pin dual in-line packages. Each is processed to MIL-STD-883, class C; screening to class B is available as an option. In small quantities, the SH-8518 sells for \$255, and the ADH-8512 goes for \$310. Delivery is from stock to eight weeks.

ILC Data Device Corp., Airport International Plaza, Bohemia, N. Y. 11716. Phone (516) 567-5600 [385]





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## New products

Semiconductors

### Chip generates 16 colors

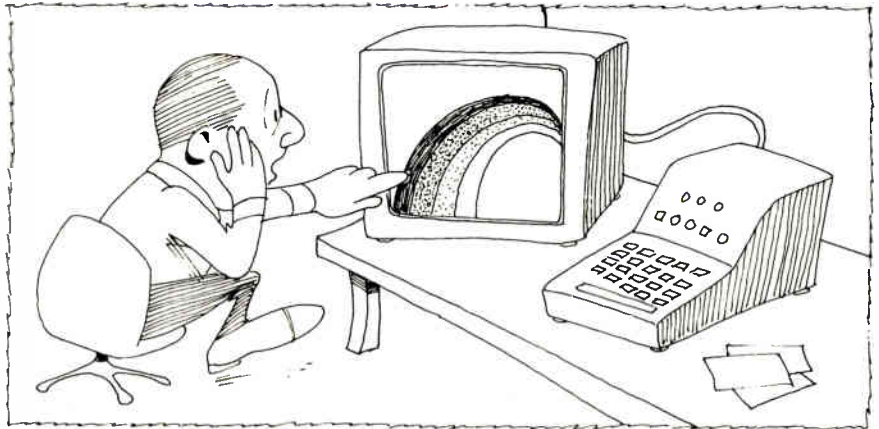
IC accepts digital codes and NTSC timing signals, delivers composite video

A single-chip video circuit that allows designers to create simple color terminals for alphanumeric or graphics displays is being readied for the market by Signetics Corp. Called a digital video summer, the device accepts standard NTSC television timing signals (composite sync, blanking pulse, and color burst flag) and a 4-bit binary code to produce a 16-color composite video signal.

According to Werner Hoeft, section manager for TV audio products, what this means is that a terminal designer can plug the circuit into any standard NTSC color chassis, hook it up to almost any transistor-transistor-logic input circuitry, and have an inexpensive display. Also, time is saved because the designer does not have to build a new chassis circuit, and the number of parts reduced because the chip replaces a number of components often needed for color terminals.

Although the video summer was originally designed for Signetics's new TV game chip set [*Electronics*, Feb. 2, p. 51], the company eyes applications in home computers and in business and analytical applications, where the terminals display distribution graphs or sales and inventory figures. It will work in "color display terminals where you want to generate color graphs from a digital circuit," Hoeft says. Additionally, it will generate true guaranteed colors, has the 75-ohm video-line drive capability required by most terminals, and will work with any microprocessor for intelligent terminal applications, he says.

Because the color reference signals are controlled by the digital signals, a user can program his



colors and luminance levels to meet his particular needs. The sharpness and clarity of the colors generated by the chip are due partly to the high, 3.58-MHz operating speed. The 3.58-MHz color subcarrier frequency is generated internally using an external crystal as the frequency reference. That speed, which effectively equals the NTSC standard for color sets, eliminates color transients or flicker.

Helping, too, is the fact that the chip operates almost entirely in an analog mode, so that the voltage needed to switch from one color to another is kept very low. No more than 200 mV is needed to switch from one color to another, leading to fast switching and no transients, Hoeft explains.

In operation, the four binary control signals enter the on-chip logic decoder, which acts like a digital-to-analog converter in changing them into 16 analog signals. These signals feed a luminance and a color generator. The color generator, which also is under control of the 3.58-MHz oscillator and the phase-shift network, consists of 16 nonsaturated analog switches and a resistor network for phase-switching the color inputs to yield the correct color output. A summing network combines the color, luminance, and synch signals to produce the composite color signal.

The 16-pin package, which has a part number of NE549, has a maximum supply voltage of 16 v, a minimum voltage on any pin of -0.3 v and a maximum input voltage of 14 v. Storage temperature

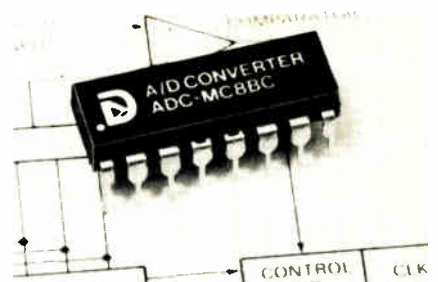
ranges from -65°C to +150°C, and the ambient operating temperature is 0°C to 70°C.

Samples of the NE549 are available now, with full production due by July. Expected prices are \$3 apiece in 100-and-up quantities and \$1.50 to \$2 each in lots of 50,000 or more. Mullard Ltd., a Philips subsidiary in the United Kingdom, is developing a version for the European PAL television broadcasting standard.

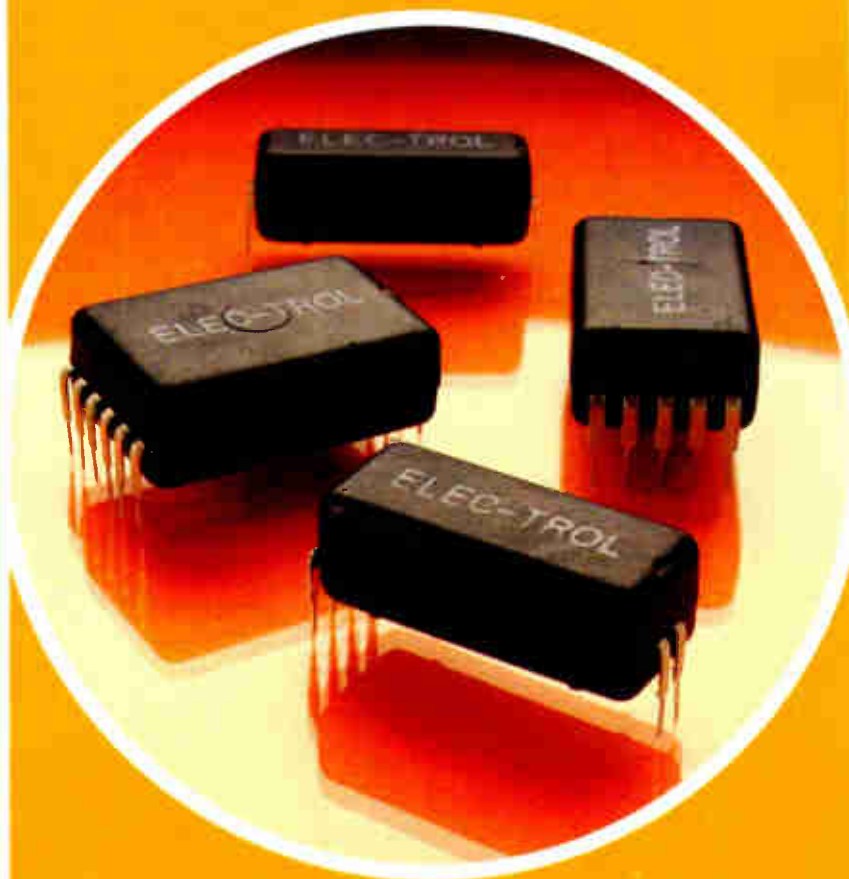
Signetics, a subsidiary of U. S. Philips Corp., 811 Arques Ave., Sunnyvale, Calif. 94086 [411]

### D-a converter plus two ICs equals an a-d converter

Take the ADC-MC8B—an inexpensive, monolithic, 8-bit digital-to-analog converter—add to it a comparator integrated circuit and a quad two-input Schmitt-trigger NAND gate, and you have an 8-bit analog-to-digital converter. The unit contains its own reference source and binary counter, plus a ladder network of diffused resistors, eight current switches, and a logic input



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These low-cost units feature hermetically-sealed dry-reed switches with switching capability from dry-circuit to 10-watts. Available with standard terminal spacing 0.1" X 1.0" and 5-48VDC coils, the units come in sizes 0.310" to 0.630" W X 0.335" H X 0.950" L. Options include magnetic shielding, electrostatic shielding, and contact run-in for one million operations. Offered in Forms 1A through 4A.

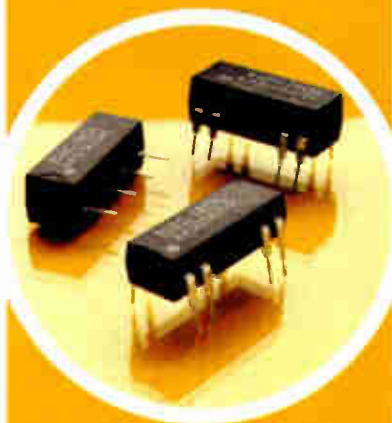
For more information use the reader service card, or contact your local distributor, representative, or the factory direct.

Elec-Trol, Inc., 26477 N. Golden Valley Road, Saugus, CA 91350, (213) 788-7292, (805) 252-8330. TWX 910-336-1556.

# ELEC-TROL

Circle 166 on reader service card

# ELEC-TROL DIP REED RELAYS



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Elec-Trol offers its complete product line of reed and solid state relays worldwide.

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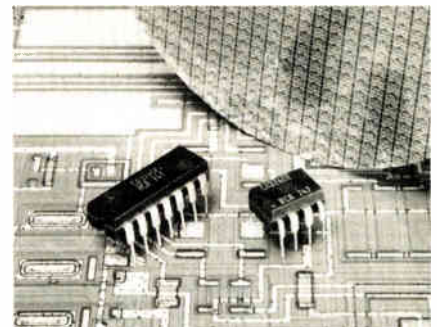
## New products

select switch. This last feature allows a single control signal to determine whether the current switches accept the output from the binary counter (a-d mode) or the external digital inputs (d-a mode). As a d-a converter, the ADC-MC8B has a settling time, for a full-scale change, of  $2 \mu\text{s}$  to within half a least significant bit. In its other mode, it has a conversion time of  $500 \mu\text{s}$ . A commercial version, housed in a plastic dual in-line package for operation from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ , sells for \$8 in lots of 1 to 24. A military version, in a ceramic DIP, operates from  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  and sells for \$14 in the same quantities. Delivery is from stock.

Datel Systems Inc., 1020 Turnpike St., Canton, Mass. 02021. Phone Eugene L. Murphy at (617) 828-8000, Ext. 141 [413]

## Dual bi-MOS op amps have high input resistance

Featuring input resistances on the order of 1.5 teraohms, the CA3240 and CA3240A bipolar-metal-oxide-semiconductor operational amplifiers have, respectively, maximum input offset voltages of 15 mV and 5 mV, maximum input offset currents of 30 pA and 20 pA, and maximum input currents of 50 pA and 40 pA. The op amps, which are dual versions of the standard CA3140 bi-MOS devices, have a supply-voltage range of 4 to 36 V and a common-mode input-voltage range that can be swung 0.5 V below the negative supply rail. Both of the new dual units are available in two housings—8-pin and 14-pin dual in-line packages—and are pin-compatible with the industry standard 747/1458



# Smart buy.

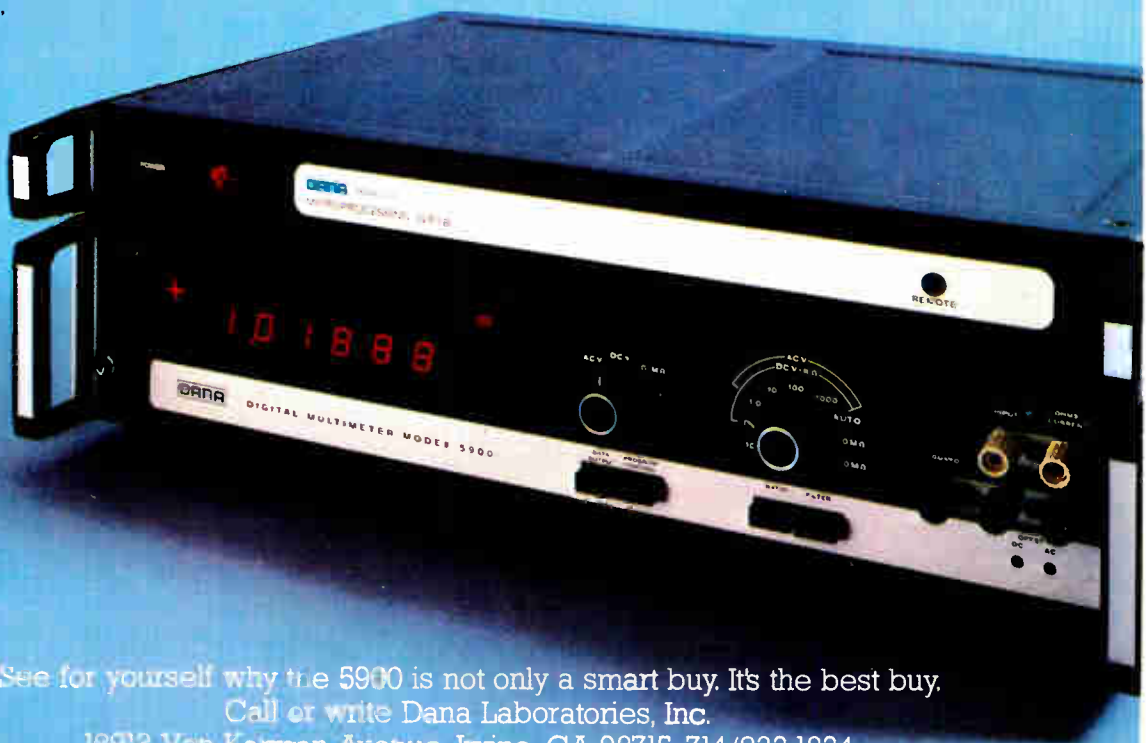
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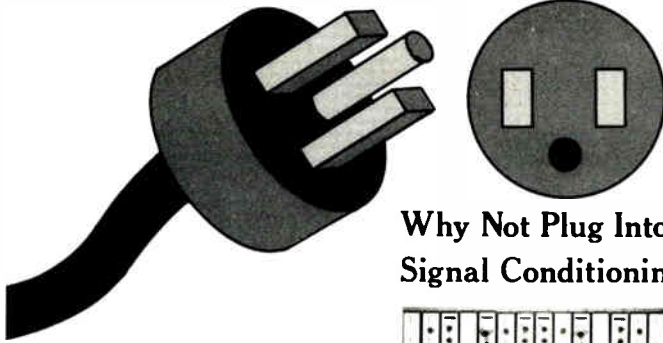
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### New products

types in similar packages. In hundreds, prices range from 61¢ each for an 8-pin 3240 to \$1.73 for a 14-lead 3240A DIP. Unmounted chips sell for 55¢ each in hundreds. Delivery is from stock.

RCA Solid State Division, Box 3200, Somerville, N. J. 08876. Phone (201) 685-6423 [414]

### SCRs operate at junction temperature of 150°C

The 325PAH series of high-power SCRs consists of six units designed for operation at junction temperatures as high as 150°C. The six units have a nominal root-mean-square current rating of 510 A, an average current rating of 325 A, and peak reverse voltage ratings from 500 to 1,200 v. They are housed in compact hockey-puck packages with a diameter of 1.6 inches.

The 325PAH devices are suitable for phase-control applications such as dc motor drives, power supplies, and input rectifiers for uninterruptible power supplies. In quantities of 100, they cost from \$44.85 to \$87.65 depending upon voltage rating and other specifications. Delivery is from stock to four weeks.

International Rectifier, Semiconductor Division, 233 Kansas St., El Segundo, Calif. 90245. Phone (213) 322-3331 [416]

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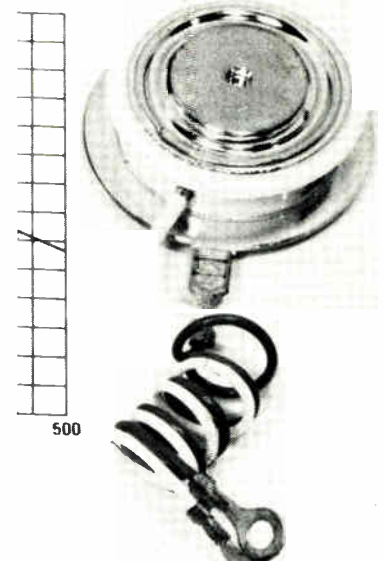
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Circle 171 on reader service card

## New products

Data handling

### Printers cost less, do more

Electrostatic units use 8048 microcomputer to form characters and do graphics

Now that most manufacturers of electrostatic line printers are marketing units with printing heads controlled by microprocessors, competitive pressures are spurring even better performance at lower prices. Among the first to introduce such a printer [*Electronics*, Jan. 22, 1976, p. 40], Axiom Corp., Glendale, Calif., is now bringing out two improved models, one selling for as low as

\$450 in quantities of 100 or more.

"Nineteen seventy-seven saw such a lowering of prices in the printer market that to stay afloat we had to rethink the electronics to reduce our costs," says Simon Harrison, vice president of marketing at Axiom. The firm's key decision in the redesign was to upgrade its Intel 4004 microprocessor to an Intel 8048 controller, allowing a two-thirds reduction of the electronics part count and far greater operating flexibility. "Not only is the one-chip controller much cheaper than the six we used before, but in addition, simplified design permits easier manufacturing," Harrison says.

The company uses the same chip in both the EX-801 Microprinter and the MicroGraphics unit, and both desktop printers now offer many performance features that previously were options or not available.

These include RS-232-C/20-milliampere serial input; a 256-character multiline asynchronous input buffer, which is expandable to 2,048 characters, making possible taking an entire page from a cathode-ray-tube terminal in about 1 second; software selection of three character sizes for 80-, 40-, or 20-column printing, and the ability to mix them on a line for emphasis; and reverse printing, where light characters are formed against a dark background. As an \$85 option, 2 kilobytes of user-programmable read-only memory may be added to convert both models into intelligent printers. With this option, the printer can operate a point-of-sale terminal or an electronic scale, to cite just a couple of examples, with no need for an external microcomputer.

The EX-801 printer is a stand-alone unit with case, power supply, parallel and serial interfaces, character generator, and built-in self-tester. It operates at up to 160 characters per second on 5-inch-wide electrosensitive paper, ready for plugging into virtually any system, Harrison says. The EX-820 graphics unit, which also works as a line printer, can mix alphanumeric ASCII fields and graphics on any line. A user defines the size of each graphic field in software, choosing from four preprogrammed horizontal-dot resolutions of up to 128 dots per in. The vertical dot resolution is fixed by the paper-feed mechanism at 65 dots per in. Automatic histograms can also be generated.

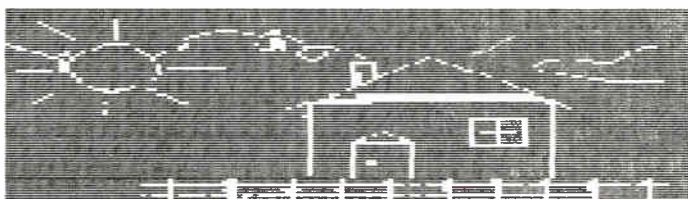
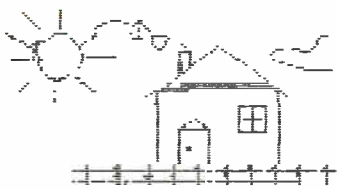
Both new printers are 11 in. wide, 4¼ in. high, and 12 in. deep and weigh 12 pounds, including a 230-foot roll of electrostatic paper. The printhead mechanism is self-adjusting and has a field-proven mean time between failures of 11.6 million lines. Additionally, the EX-820 graphics printer is available as a 5¼-in.-high unit for mounting in a standard 19-in. rack.

The EX-801 sells for \$655, the EX-820 for \$795, for one unit. For quantities of 100 and up, the prices are \$450 and \$555, respectively. One new market likely to open is among computer hobbyists, who have been

AXIOM ANNOUNCES THE MICROGRAPHICS ERA  
THIS IS A SAMPLE OF THE PRINTOUT FROM AXIOM'S LATEST PRINTER

THE EX-820

GRAPHICS ARE EASY



SO ARE HISTOGRAMS

1950	19.9
1960	25.4
1970	31.8
1980	27.6
1990	28.3

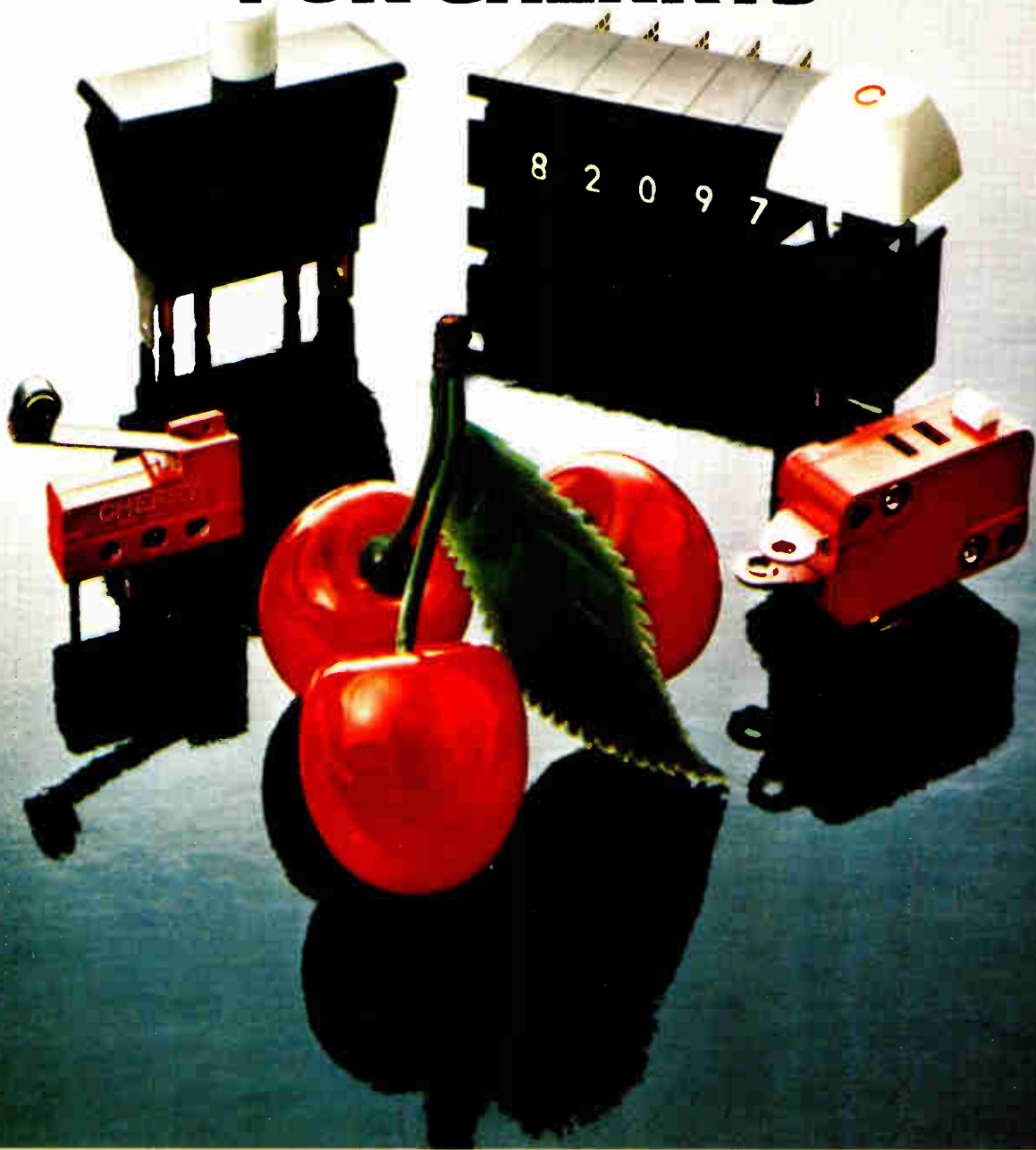
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This can have the same effect as UNDERLINING or changing COLOR

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Circle 173 on reader service card

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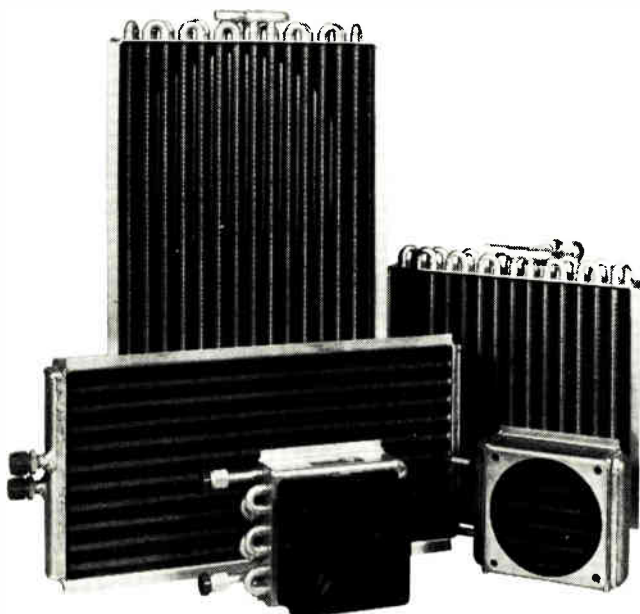
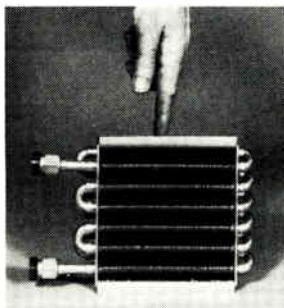
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## New products

looking for a dependable printer priced under \$500, Harrison says.

Delivery times differ slightly. They are 21 days for the EX-810, 30 days for the EX-820.

Axiom Corp., 5932 San Fernando Rd., Glendale, Calif. 91202. Phone (213) 245-9244 [361]

## Distributed data-processing system is easily expanded

The Sycor 405 distributed data-entry and -processing system can be purchased for less than \$20,000 in a typical configuration, making it suitable for first-time users. At the same time, it has been designed for easy expansion, so that its capabilities can grow with the needs of the user. Functionally compatible with the larger Sycor 445, the new computer can be conveniently connected to other 405 and 445 processors through the company's Sycorlink networking facility. Users can use



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The 405 provides up to 64,000 bytes of main memory, 2 megabytes of flexible-disk storage, two 2,000-character video data stations, a magnetic-tape drive, and a bidirectional matrix or line printer. Three programming languages are available: Cobol, Basic, and TAL 2000. A typical 405 configuration with 48,000 bytes of main memory, 500,000 bytes of flexible-disk storage, one data station, one Sprinter printer, and a communications

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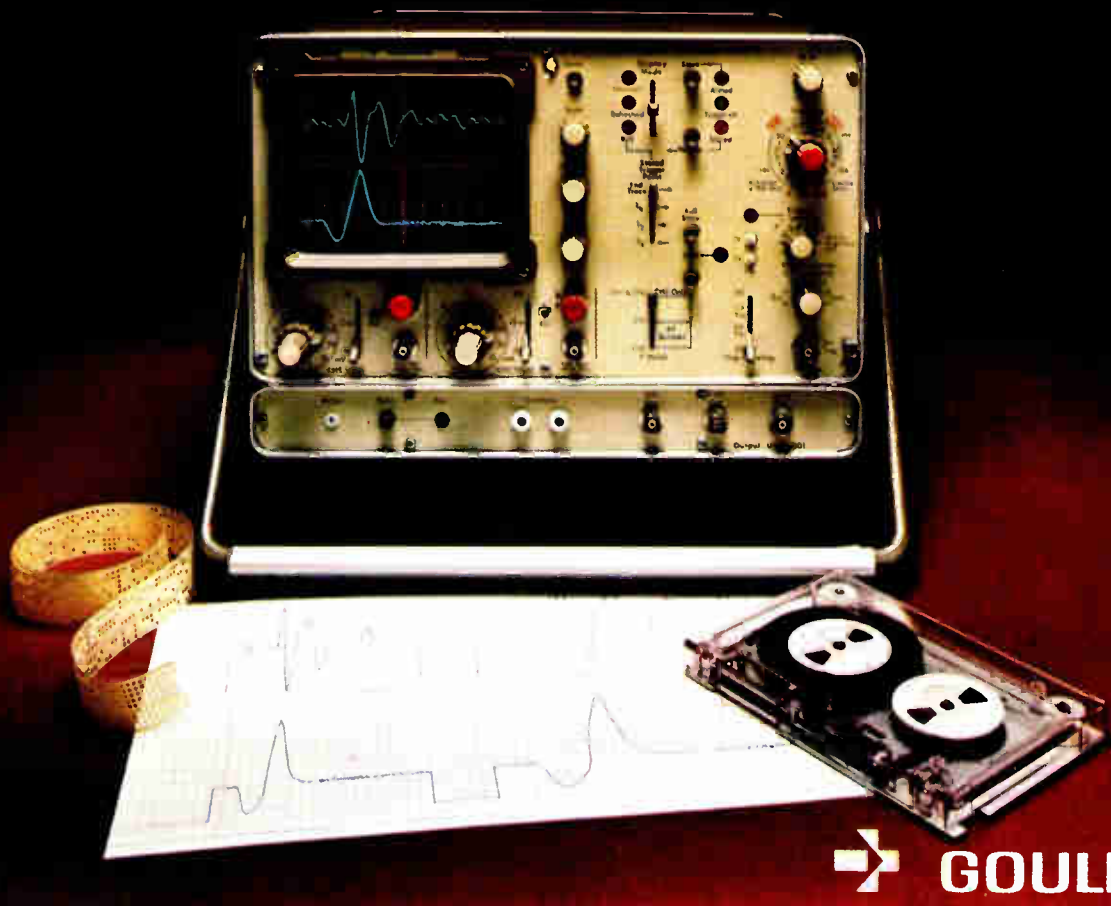
frequencies there is no irritating flicker or C.R.T. glow.

Rated at 10 MHz for conventional operation the OS4000 utilizes an 8 bit x 1024 word RAM, with a sampling frequency of 1.8 MHz. Normal/refreshed/roll modes are standard.

With a multitude of new applications in general electronics, medical electronics, research laboratories and transducer related measurement situations, Gould's OS4000 simply outclasses every tube storage scope on the market. But even though the OS4000 represents a step forward in storage scope technology, it is both easy to use and extremely affordable.

For more information contact Gould Inc., Instruments Division, 3631 Perkins Ave., Cleveland, OH 44114. In Europe contact Gould Advance LTD., Roebuck Rd., Hainault, Essex, CB10 1EJ, England.

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Circle 176 on reader service card

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## New products

adapter sells for \$19,850. It can also be leased for various terms; a typical rate is \$497 a month for a two-year lease, including maintenance. Initial deliveries of the 405 data system are scheduled for the third quarter of this year.

Sycor Inc., 100 Phoenix Dr., Ann Arbor, Mich. 48104. Phone Larry Bobrowski at (313) 995-1265 [363]

## Smallest DEC Datasystem incorporates video processor

Digital Equipment Corp.'s smallest, cheapest Datasystem—the Datasystem 308—is intended to fill the data-processing needs of small businesses that need only a single terminal. Built around DEC's PDP-8-based video data processor, the 308 is offered in configurations with prices from \$12,600 to \$18,000. A typical system consists of the video data processor, 32 kilobytes of main memory, a dual floppy-disk system, and a minidesk.

Digital Equipment Corp., Maynard, Mass. 01754. Phone Joseph C. Nahil at (603) 884-5101 [364]

## Fast dual diskette drive stores 3.2 megabytes

Capable of storing up to 3.2 megabytes of unformatted data, the model 299 diskette drive is a two-head-per-disk, two-disk unit that can write and read on both sides of two 8-inch diskettes. Data can be encoded in single or double density. The drive uses a voice-coil positioning system of the type employed on large disks to achieve an average access time of 33 ms, which the manufacturer claims is five to seven times faster than drives positioned by stepper motors. The four-headed drive is 4.38 inches wide, 8.72 in. high, and 15.4 in. deep. In small quantities, it sells for \$1,595. Deliveries are scheduled for the second quarter.

PerSci Inc., 12210 Nebraska Ave., West Los Angeles, Calif. 90025. Phone (213) 820-3764 [365]

# **NOW!** **GP-IB** **SPOKEN** **HERE.**

IEEE-STD-488

**Lambda LF Series**  
**power supplies for**  
**automatic test**  
**equipment**



MODEL  
LF-9-04-GPIB

**Also available**  
**in BCD or ASCII**  
**programming**

**Guaranteed**  
**for 5 years**

# SPECIFICATIONS OF LF-9-04-GPIB

## DC output

Volt (VDC)	MAX AMPS AT AMBIENT OF		
	40°C	50°C	60°C
0 to ± 49.95	1.98	1.8	1.6

## Output range

X1 range	± 9.99V in 10 mV steps
X10 range	selected automatically (0- to ±49.9 V in 100 mV steps)

## Source or sink

1.98 amps continuous

## Regulated voltage

regulation line	0.01% – for line variations 105-132VAC (see AC input option)
regulation load (all ranges)	0.01% – for load variation of 0 to full load.
ripple and noise	X1 range 2.0 mV pk pk max X10 20 mV pk pk max
temperature coefficient	Voltage X1 range .005%/°C + 35 μV/°C X10 range .005%/°C + .215 mV/°C Current All ranges 500 μA/°C

## Constant current operation

Current Range	1% to 99% of full scale
Regulation line	1 mA max
load	20 mA max

## AC input

105-132VAC, 47-440Hz. For 187-242 or 205-265 VAC see AC input option.

## Ambient operating temperature range

continuous duty from 0° to 60°C with load current ratings shown in table.

## Storage temperature range

-55°C to +85°C

## Basic accuracy

(at 25°C, 115VAC input and no load)	<u>Voltage</u>
	X1 range: 3 mV X10 range: 30 mV
	<u>Current</u>
	All ranges: 10 mA

<b>Resolution</b>	<u>Voltage</u>
	X1 range: 10 mV X10 range: 100 mV
	<u>Current</u>
	All ranges: 20 mA

## Transient response

1.2 msec to within .05% of full scale for 90% load change

## Overshoot

Worst case overshoot 1 volt under any conditions

## Input Data Format:

Data is entered in bit-parallel, byte-serial format as specified by IEEE Std. #488. The 24 programming bits contain 12 bits BCD voltage programming, 8 bits BCD current programming and one bit each for gain, polarity and mode. The valid data format is ASCII.

## Programming time:

see graphs on next page

## Data Loading:

Logic levels ("0" ≥ + 2.0V; "1" ≤ + 0.8V) and interface requirements are as specified in IEEE Std. #488.

## Data Input Lines:

DIO-1 thru 8 as specified in IEEE Std. #488.

## Control Lines:

ATN, EOI, IFC, NRFD, NDAC, DAV, SRQ, REN\* as specified in IEEE Std. #488. All control and data input lines are accessed through 24-pin GPIB connector on back panel. The SRQ line is activated by a current overload condition while in constant voltage mode or overvoltage limit condition while in constant current mode. Mode of operation programmed with mode bit.

\*REN is not a usable function for the LF-GPIB and is terminated in a logical "0".

## Cooling

Convection-cooled, no heatsinks or blower necessary

## Mounting positions

one mounting position on horizontal plane  
Input/output connections through heavy duty barrier strip and connector

## Physical data

Model (Package 9)	Size (inches)	Weight	
		lbs net	lbs ship
LF-9-04-GPIB	4 15/16 x 7 1/2 x 14 5/8	20	22

## Options

### AC input

Add Suffix	for operation at:	Add to Price
-V	187-242 VAC, 47-440 Hz	12%
-V <sub>1</sub>	205-265 VAC, 47-440 Hz	12%

## Accessories:

rack adapters LRA-10, LRA-11. Overvoltage protectors, chassis slides, blank panels.

## Guaranteed for 5 years.

5 year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of 5 years.

# SPECIFICATIONS OF LF-9-04

## DC output

	MAX AMPS AT AMBIENT OF:		
Volt (VDC)	40°C	50°C	60°C
0 to ± 49.95	1.98	1.8	1.6

## Output range

- X1 range: ± 9.99V in 10 mV steps
- \*X5 range: ±49.95V in 50 mV steps
- X10 range: ASCII only – selected automatically(0- ±49.9 V in 100 mV steps

## Source or sink

1.98 amps continuous

## Regulated voltage

regulation line.....	0.01% – for line variations 105-132VAC (see AC input option)
regulation load .....	0.01% – for load variation of (all ranges) 0 to full load.
ripple and noise.....	X1 range: 2.0 mV pk-pk max *X5 range: 10 mV pk-pk max X10 (ASCII): 20 mV pk-pk max
temperature coefficient .....	Voltage X1 range: .005%/°C+35 μV/°C *X5 range: .005%/°C + 0.115 mV/°C X10 range: (ASCII only) .005%/°C + .215 mV/°C
	Current All ranges: 500 μA/°C

## Constant current operation

- Current Range: 1% to 99% of full scale
- Regulation line . . . . . 1 mA max
- load . . . . . 20 mA max

## AC input

105-132VAC, 47-440Hz. For 187-242 or 205-265 VAC see AC input option.

## Ambient operating temperature range

continuous duty from 0° to 60°C with load current ratings shown in table.

## Storage temperature range

-55°C to +85°C

## Basic accuracy

(at 25°C, 115VAC input and no load).....	<u>Voltage</u> X1 range: 3 mV *X5 range: 15 mV X10 range: 30 mV (ASCII only)
	<u>Current</u> All ranges: 10 mA

<b>Resolution</b> .....	<u>Voltage</u> X1 range: 10 mV *X5 range: 50 mV X10 range: 100 mV (ASCII)
	<u>Current</u> All ranges: 20 mA

## Transient response

1.2 msec to within .05% of full scale for 90% load change  
\*BCD only

## Overshoot

Worst case overshoot 1 volt under any conditions

## Input data word:

A 24 Bit data word is used comprising of 12 bits BCD voltage programming, 8 bits BCD current and one bit each for gain, polarity and current limit override. Data word may be accepted in 3, 2, or 1 sequential segments of 8, 12, 24 bits, or ASCII to make up the 24 bits. Current is programmed as a percentage of full scale.

## Programming time:

see graphs on next page

## Data validity

10 μsec

## Data loading

Logic Levels—all 0 to +5V. One CMOS load per line. Compatible with TTL or DTL

Interface requirements:

- CMOS – direct
- DTL – direct
- TTL – direct, with a 10K pull up resistor on each data line to +5V bus.

## Control lines

- One TTL or DTL buffer per line
- Data Flag – CMOS input
- Zero Override – requires sinking of 15mA, compatible with DTL or TTL buffers
- Final Transfer Pulse – CMOS input

## Output flags

1. Current Limit Flag – optical coupler, conducting when in current limit.
2. Busy Ready Flag – open collector, logic zero when ready to accept new data.

## Cooling

Convection-cooled, no heatsinks or blower necessary

## Mounting positions

one mounting position on horizontal plane  
Input/output connections through heavy duty barrier strip and connector

## Physical data

Model (Package 9)	Size (inches)	Weight	
		lbs net	lbs ship
LF-9-04	4 15/16 x 7 1/2 x 14	20	22

## Options

### AC input

Add Suffix	for operation at:	Add to Price
-V	187-242 VAC, 47-440 Hz	12%
-V <sub>1</sub>	205-265 VAC, 47-440 Hz	12%

## Accessories:


rack adapters LRA-10, LRA-11. Overvoltage protectors, chassis slides, blank panels.

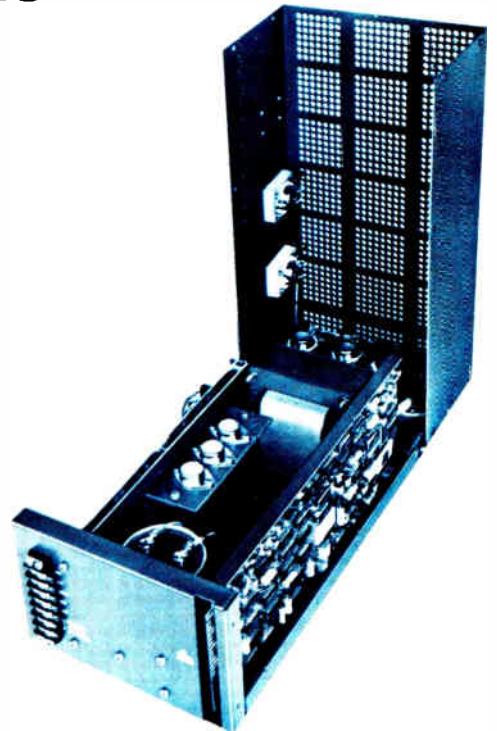
## Guaranteed for 5 years.

5 year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of 5 years.

# THE MOST ADVANCED AUTOMATIC TEST EQUIPMENT POWER SUPPLIES ON THE MARKET TODAY

## LF-9-04 power supply LF-9-04-GPIB power supply

Now  Lambda offers two power supplies for your automatic test equipment power supply requirement. It provides plus or minus 0-50 volts at 2 amperes DC with the following features:



### Features

LF-9-04		LF-9-04-GPIB	
8, 12, or 24 bit BCD programming or ASCII programming	current limit flag	IEEE Standard 488-75 interconnector bus ASCII programming	ripple—20 mV pk-pk on 50 Volt range
0.01% regulation, line or load	busy ready flag	0.01% regulation, line or load	optical isolation
A 2 msec programming time for full voltage compliance	Current limit programming	A 2 msec programming time for full voltage compliance	Current limit programming
15 mV accuracy for 50 V BCD programming	current over-ride	30 mV accuracy for 50V of ASCII programming	zero adjust
30 mV accuracy for 50V of ASCII programming	zero over-ride	Resolution 100 mV at 50 V	worst-case overshoot—1 volt
Resolution 50 mV (BCD) at 50 V; 100 mV for ASCII	inverted/noninverted input	100% sinking capability	transient response—1.2 msec
100% sinking capability	zero adjust	ripple—10mV pk-pk (BCD) on 50 Volt range; 20 mV for ASCII	unique digital circuitry designed with CMOS
ripple—10mV pk-pk (BCD) on 50 Volt range; 20 mV for ASCII	worst-case overshoot—1 volt	optical isolation	
	transient response—1.2 msec		
	unique digital circuitry designed with CMOS		

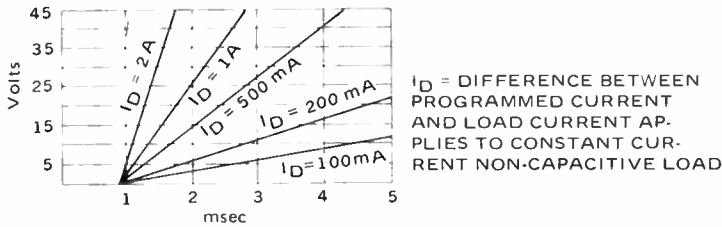
### Ordering Information

Model	Price	Model	Price
LF-9-04	\$1000	LF-9-04-GPIB	\$1200

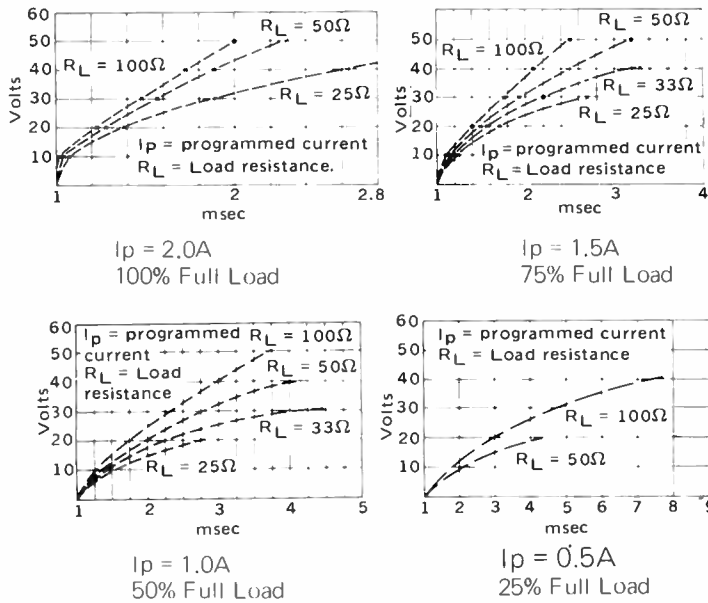


# SPECIFICATIONS OF LF-9-04, LF-9-04-GPIB

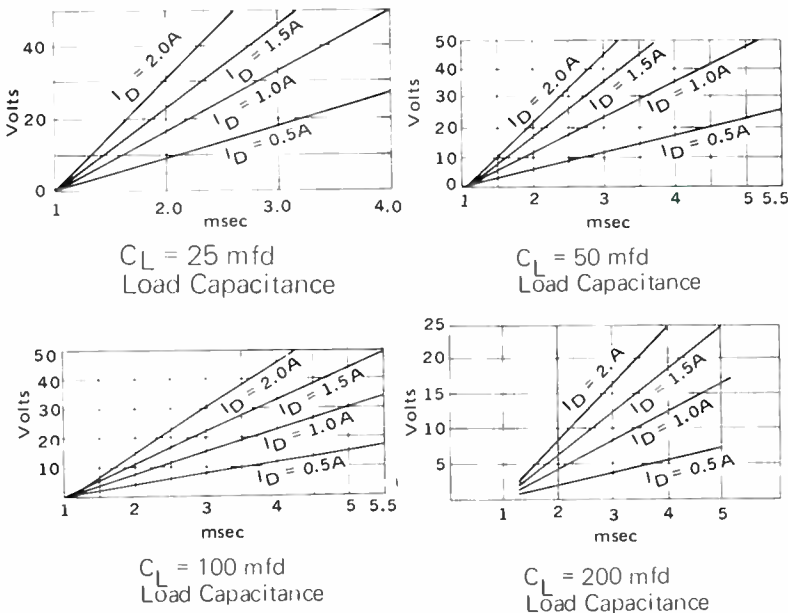
## Programming Time mSec Vs Programmed Voltage Step (Constant Current Load)



## Programming Time mSec Vs Programmed Voltage Step (Resistive Load)



## Programming Time mSec Vs Programmed Voltage Step (Capacitive Load)



$I_D$  = Difference between programmed current and constant load current.

## DEFINITION OF TERMS:

### Resolution:

Minimum programmable change

### Basic Accuracy:

Maximum deviation from programmed value at 25°C constant temperature, 115 VAC and no load.

### Programming Time:

Time, after data entry, required for the supply to settle within 0.05% full scale.

### Data Flag:

Customer generated 3.3  $\mu$ sec minimum pulse, beginning at least 2  $\mu$ sec after date is presented, to signal that data is available and ready for processing.

### Final Transfer Pulse:

Customer generated 2  $\mu$ sec minimum pulse beginning at least 300  $\mu$ sec after first data flag, to transfer data from input shift register into storage and the DAC's. This pulse is internally generated by the system for ASCII.

### Data Validity:

Minimum time for which data must remain present after data flag.

### Transient Response:

Time required for supply to return to within 0.05% full scale of programmed value, for 90% change of load.

### Overshoot:

Magnitude of voltage by which output may exceed programmed value or fall below zero volts during turn-on, turn-off, voltage to current limit crossover or current limit to voltage crossover and programming.

### Zero Override:

Input signal pulse programs output of power supply to zero volts. This signal is also activated when input data plug is pulled out. Zero override is a system feature that may be utilized in an emergency by forcing the output to zero volts from any previous state. When in that mode the output will be kept at zero  $\pm$  50 mV max. While the output ripple will be limited to 15 mV pk-pk max.

### Output Flags:

System generated signal, available to the user through the input data connector.

# SUMMARY OF THE IEEE STD. #488

## See Specifications of LF-9-04-GPIB

IEEE Standard #488 specifies a system for the interconnection of as many as 14 pieces of test equipment on a single 24-wire bus controlled by a central processing unit. The bus consists of 8 bidirectional data lines, 8 command lines and 8 ground lines. Data is transferred along the bus via a specific 3-wire "handshake" process. This process greatly reduces the possibility of lost data since any one operation must be confirmed by all addressed units before the following operation may commence.

The address system allows the controller to identify the units which are to transmit or receive data while allowing the other units on the bus to function uninterrupted. The service request (SRQ) line provides each module on the bus with the ability to inform the controller if a particular condition in that module warrants attention or service.

Listed below are the designations of the 8 command lines and a brief function description for each:

- 1. ATN (ATTENTION)** - This line is used to call the attention of all units on the bus (i.e., all units are listening). All command instructions must be given under this signal.
- 2. IFC (INTERFACE CLEAR)** - This line is used to set the interface—parts of which are contained in all units on the bus—at a known quiescent state.
- 3. SRO (SERVICE REQUEST)** - This line provides a means for each unit on the bus to indicate to the controller that a condition exists which may require attention or service.

- 4. EOI (END OR IDENTIFY)** - This line is used to indicate the end of a particular multiple-byte transfer sequence.
- 5. REN (REMOTE ENABLE)** - This line is used to select between two alternate sources of device programming data (i.e., computer control or local control).

The remaining three commands comprise the three-wire "handshake" process. This process utilizes interlocking command sequences to transfer each data byte across the interface. These sequences can only proceed at the rate of the slowest addressed unit on the bus, thus assuring that all units on the bus can completely assimilate the data.

- 6. DAV (DATA VALID)** - This command is used by the "talker" to indicate that the data on the DIO signal lines is valid and ready to be processed.
- 7. NRFD (NOT READY FOR DATA)** - This line is used by the "listeners" on the bus to indicate whether or not they are ready to process the next byte of data.
- 8. NDAC (NOT DATA ACCEPTED)** - This line is used by the "listeners" on the bus to indicate that the data on the line has been processed and can now be removed.

### Consult Factory For:

- Application information using BCD as input format.
- Application information using IFC as an emergency shutdown.

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Materials

## **Foamed plastic resists flames**

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Structural resin can cut the assembly costs of computers and peripherals

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A new thermoplastic foam resin that meets the flammability requirements of UL bulletin 478 and NFPA-75, is opening the door to design and cost reductions in the large-computer field. The material, General Electric's Lexan FL 1800, is finding its way into such applications as the housings of data input stations, large line printers, free-standing tape drives and rack-mounted electronics.

These systems usually reside in a enclosed computer room. Earlier engineering structural foams such as

Lexan FL 900, Valox, and Noryl are already in use on the housings of plastic-cased computer peripherals and minicomputers that go in an office environment where the stricter flammability specs of UL 478 do not apply.

These structural-foam assemblies have been banned from the computer room by the UL requirement that plastics used there must have a flame spread index ( $I_s$ ) of less than 50. Lexan FL 1800 has an  $I_s$  of 25, and it is the only foamed plastic approved for use in a computer room. The new plastic is a UL 95-0/6V material, has an oxygen index of 52% and a heat-distortion temperature of 290°F, and can stand a falling ball impact of 40 ft-lbs.

Structural foam molding is a form of injection molding: the foam is achieved either by introducing inert gas directly into the melt or by preblending the resin with a chemical blowing agent. When the mixture is shot under pressure into the

mold, the gas expands within the plastic material producing an internal cellular structure, as well as a tough external skin.

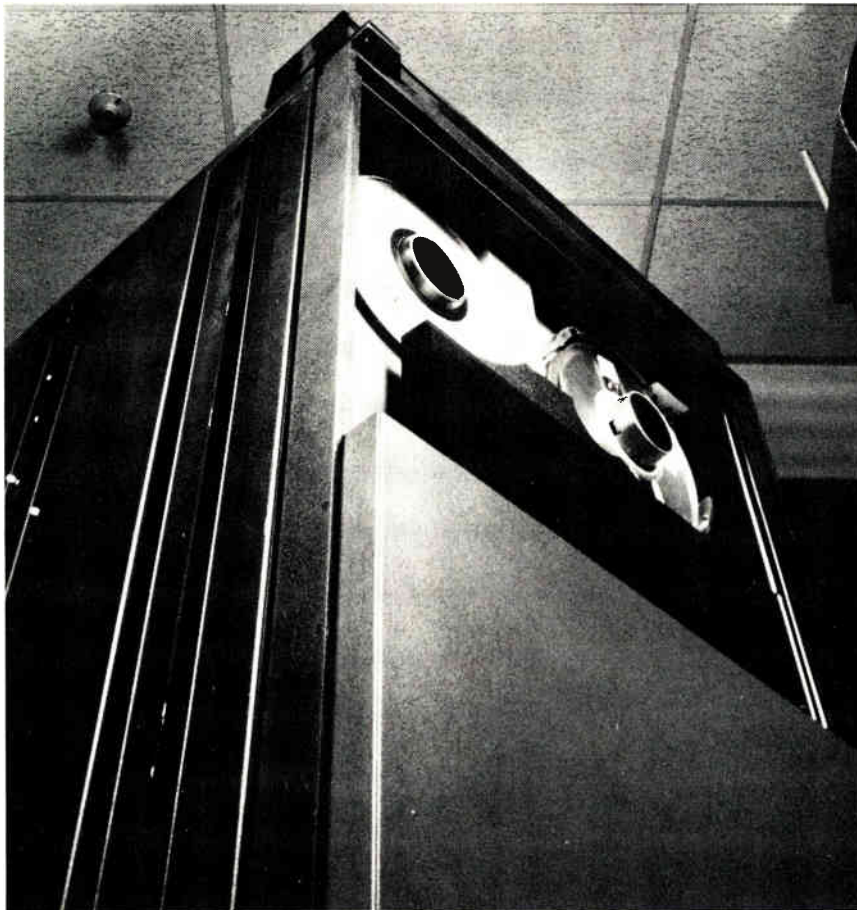
Such materials have seven times the rigidity of an equal weight of steel. Compared to an equivalent weight of solid plastic, foam will have twice the rigidity. However, where foamed plastics really pay off is in manufacturing simplicity and cost reduction.

For instance, an eight-part data-module drive-cover assembly made from metal can be replaced with only two structural-foam parts. Thus replacement of metal by foamed plastic results in a significant saving to the end user—as much as 50% reduction in some cases.

The new material costs \$147 per pound in truckload quantities. A GE spokesman says that there appears to be a 60-million-pound potential for foam resins in computer-room applications, at which the new material is presently targeted.

Structural Foam Resins, Plastics Division, General Electric, One Plastics Avenue, Pittsfield, Mass. 01201 [475]

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## **Thermally stable epoxy holds optical fibers together**

Epo-Tek 330 is an all-solids two-part epoxy formulation that is especially well suited for optoelectronics applications. When used to bundle optical fibers, for example, it holds them together as a stable unit as they are ground and polished to an optically smooth finish. The formulation is particularly resistant to high temperatures: at 350°C, weight loss under thermogravimetric analysis is 10% in air at a 20°C/minute scan rate.

Other key specifications include a viscosity of 354 centipoises at 25°C, a lap shear strength of 2,050 pounds per square inch, and a tensile strength of 10,000 lb/in.<sup>2</sup>. For a 2.65-micrometer wavelength, a 1.5-mil thickness of the material has a spectral transmission of 84.9%.

The epoxy has a room-temperature pot life of 8 hours and a 150°C cure time of 5 minutes. Curing

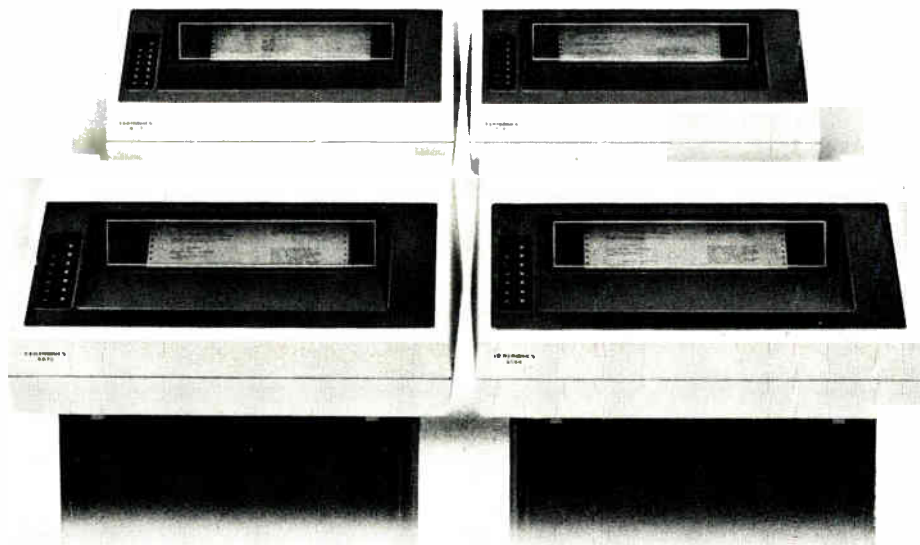
# Does 85% commonality make Centronics' line printer family the best?

**NO.** Centronics 6000 series band printers have much more to offer than just high parts commonality; technical features like an operator-changeable print

band with a choice of EBCDIC character sets and microprocessor control, for example. Four models—providing superior print quality and a range of print speeds—75, 150, 300 and 600 lpm, plus design simplicity that provides exceptional reliability and makes the 6000 series a true family of low priced, fully formed character line printers.

And, as with Centronics' matrix printers and teleprinters, the 6000 series is backed by the largest worldwide service organization of any printer company, and Centronics' reputation for reliability.

Write or call for complete 6000 series information. Centronics Data Computer Corp., Hudson, NH 03051, Tel. (603) 883-0111.



**CENTRONICS® PRINTERS**  
**Simply Better**

# Revolutionary cooling extrusion cuts size and cost in half.

Here is the first in a new series of unique cooling extrusions from Wakefield.

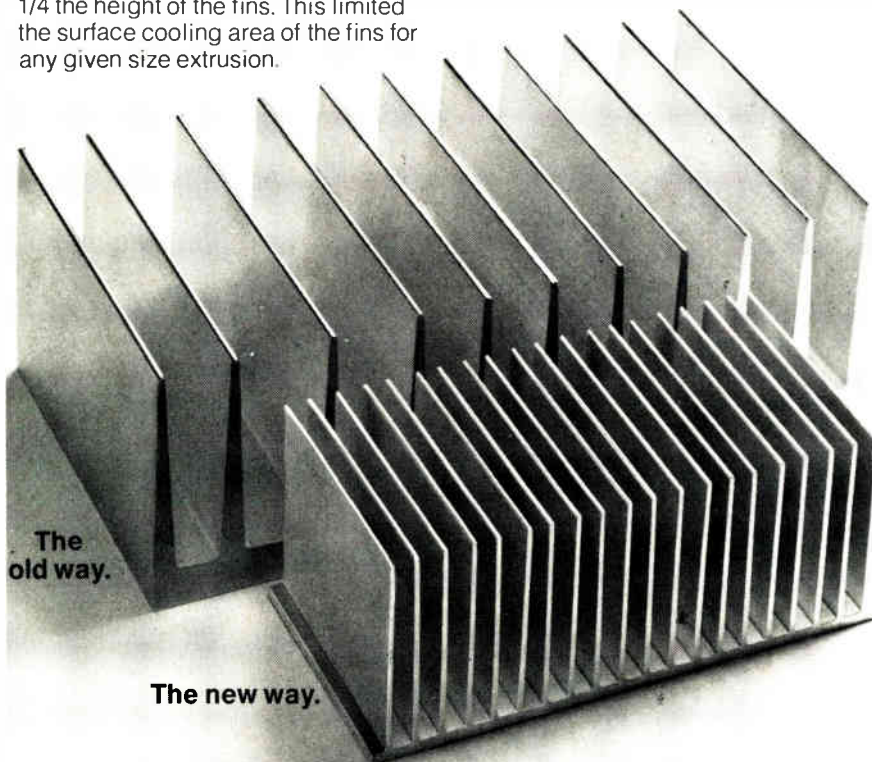
A totally different design concept called "High Fin Density" allows Extrusion 5113 to give the same cooling performance as devices needing nearly twice as much space.

And because of substantial material savings, the 5113 is half the price of the larger units—only \$1.10 per inch.

Until now, the space between fins of an extrusion could be no less than 1/4 the height of the fins. This limited the surface cooling area of the fins for any given size extrusion.

"High Fin Density" has changed all this by reducing the space between fins to as little as 1/10 their height. The result is a tremendous gain in cooling efficiency with 130 sq. in. of cooling surface per linear inch of extrusion.

Knowledgeable people say this is the most significant breakthrough in the history of cooling devices. But then, what would you expect from the leader? Write or call for full details.



**WAKEFIELD ENGINEERING INC.**

77 AUDUBON ROAD, WAKEFIELD, MA 01880 (617) 245-5900  
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## New products

completeness can be verified by observing the material's color change from clear amber to bright red. It is available in 1-lb evaluation kits for \$16.60.

Marketing Dept., Epoxy Technology Inc., P. O. Box 567, Billerica, Mass. 01821. Phone (617) 667-3805 [476]

## Copper desoldering wick has flux coating

To enhance its effectiveness as a desoldering aid, a copper wick is manufactured using a vacuum technique that deoxidizes the copper braid while applying a smooth coating of noncorrosive flux. The result is a wick that absorbs solder almost



instantly when it is applied to a defective joint and then touched with a soldering iron. Offered in widths of 1/16, 3/32, and 1/8 inch, each 66 in. long, the wick is available from stock.

Multicore Solders, Westbury, N. Y. 11590 [477]

## Thick-film conductor paste adheres well to alumina

A glass-free silver conductor paste develops a reactive bond at the surface of 96% alumina that results in high adhesion strengths for screen-printed patterns in thick-film-circuit manufacture. Called Vit-Au-Less 4055, the paste yields

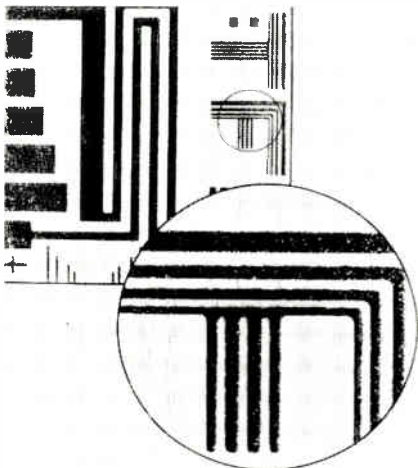
# Another breakthrough in cooling extrusion size and cost.

Here is the latest of the "High Fin Density" extrusions from EG&G Wakefield Engineering. Extrusion 5206 is the smallest and most economical of these remarkable cooling devices to be announced thus far. With a price of only \$1.00 per inch, this unit is less than half the price of competitive types with the same cooling capacity.

The skyrocketing cost of aluminum is creating a real need for a more efficient extrusion design. That's why Wakefield developed "High Fin Density" extrusions. By reducing the space between fins to as little as 1/10 their height, these revolutionary units have double the cooling efficiency of competitive types using substantially more aluminum.

And for the very ultimate in cooling efficiency, try the Series FCA-880. Combining two 5206 Extrusions in a package, it gives even more cooling performance for the amount of space required.

So if you want to cut your cooling costs, or the space required, write or call Wakefield. It pays to do business with the leader.



patterns with surface resistivities from 1.0 to 1.3 milliohms per square. Using 22-gauge wire soldered to 100 mil<sup>2</sup> pads, the material achieves a 90° peel strength of 15 to 20 pounds. For cleanliness and ease in handling, it is supplied in plastic syringes and cartridges. It sells for 64 cents a gram in production quantities.

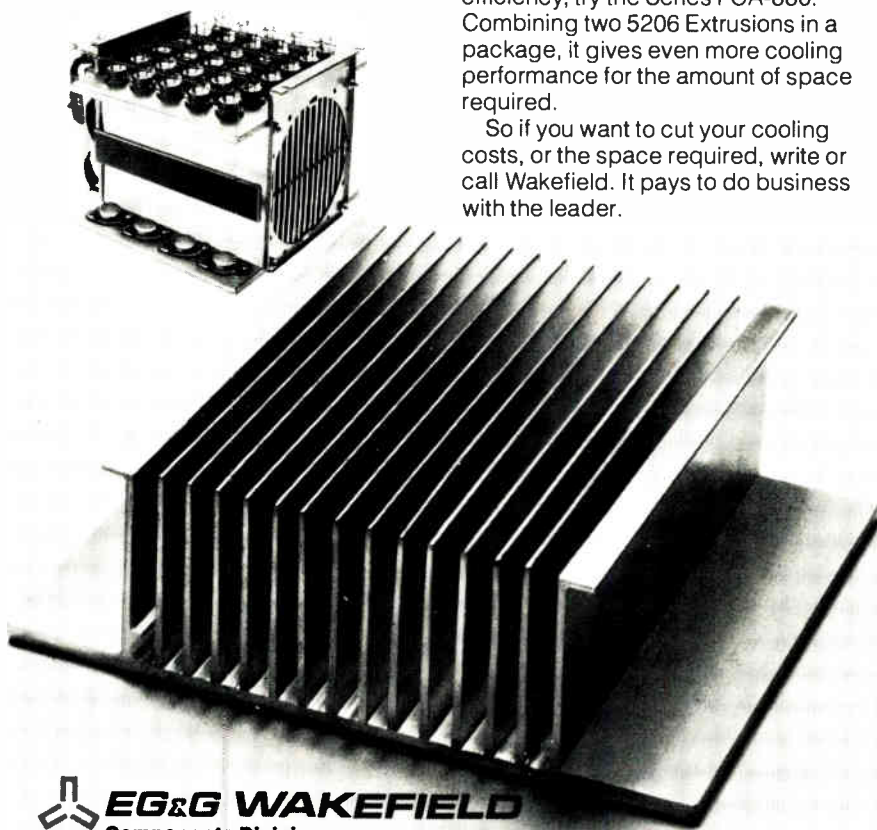
Thick Film Systems Inc., 324 Palm Ave., Santa Barbara, Calif. 93101. Phone (805) 963-7757 [478]

## Conductive grease-caulk protects against corrosion

Eccoshield CO is a conductive grease that is effective both as a lubricant for sliding metal-to-metal surfaces and as a caulking compound for static metal-to-metal joints. In both applications, it provides electrical continuity for the rejection of electromagnetic interference and protection against chemical corrosion. It also will not enter into electrolytic corrosion reactions.

The material has a volume resistivity of less than 100 ohm-cm—adequate for many shielding applications. If needed, other, more expensive, Eccoshield formulations are available with resistivities below 1 milliohm-cm. Eccoshield CO sells for \$15 a pound in quantities of 1 to 4 pounds and for \$6.70 a pound for lots of 5 pounds or more. Delivery is from stock.

Emerson & Cuming Inc., Canton, Mass. 02021. Phone 617 828-3300 [479]



**EG&G WAKEFIELD**  
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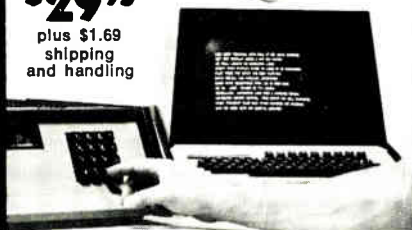
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Because the filament is of a low-voltage, high-current design, it is extremely rugged and easily maintains its position relative to the lens. Rated filament life is 5,000 hours.

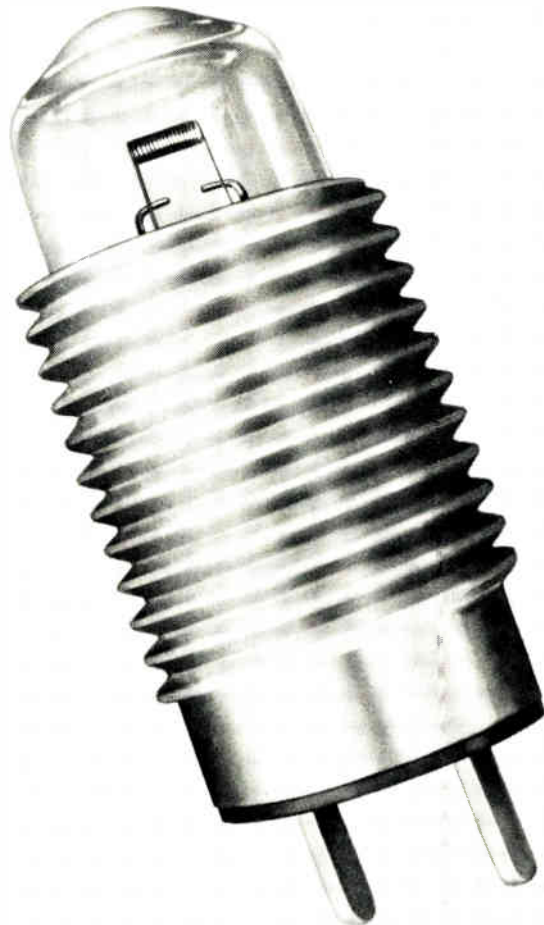
The C-6 filament is 1.1 mm in diameter and 1.2 mm long.

The L8006 has a 1/2-20 UNF-2A base. It sells for \$4.10 and is available from stock.

Gilway Technical Lamp, 272 New Boston Park, Woburn, Mass. 01801. Phone (617) 935-4442 [341]

**Sealed potentiometer  
is only 0.1 inch high**

Excluding its adjustment caps, the model 3391/92 sealed potentiometer measures only 0.1 inch high and 0.172 in. in diameter. The single-turn unit is aimed at use in such miniature circuitry as hearing aids, paging systems, hand-held probes, and hybrid circuits. The unit is offered in a range of nine resistances from 1 to 500 kΩ with both linear and audio tapers. It has a power-





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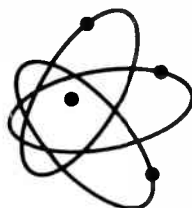
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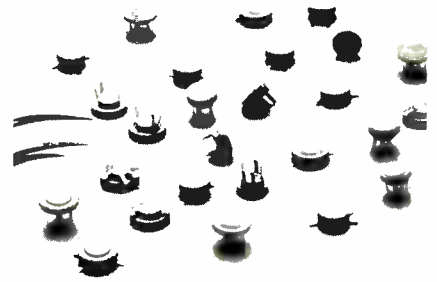
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**EAC** Electronic Applications Company

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El Monte, California 91734  
213/442-3212 TWX 910/587-3351

### New products



dissipation rating of 50 mw, and a switch with a positive detent is available as an option.

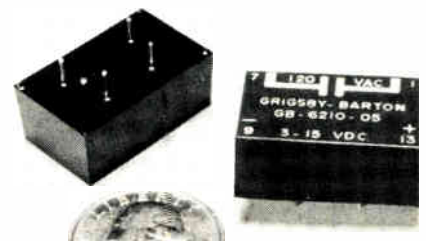
The potentiometer element is of conductive plastic for long life and good stability. Its standard resistance tolerance is 20%, and the potentiometer's contact-resistance variation is no more than 3%. Rotational life averages 50,000 cycles.

The model 3391 has a flat adjustment cap with a diameter of 0.3 in. The model 3392 has a separate domed adjustment cap with a diameter of 0.24 in. Both units sell for \$4.46 each for 1,000 or more. Delivery time is four weeks, with some units available from stock.

Trimpot Products Division, Bourns Inc., 1200 Columbia Ave., Riverside, Calif. 92507. Phone (714) 781-5320 [343]

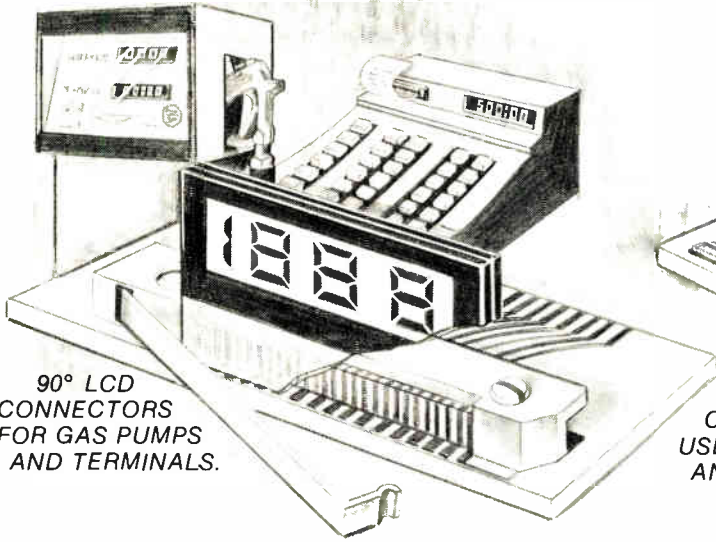
### Solid-state relay fits 14-pin DIP socket

The GB6000 series of solid-state relays has printed-circuit terminals spaced to fit into a socket for a 14-pin dual in-line package. Its rugged epoxy-encapsulated case measures 1.13 by 0.68 by 0.48 inches. The units have optically coupled inputs that provide input-output isolation of 2,500 v ac. Models capable of

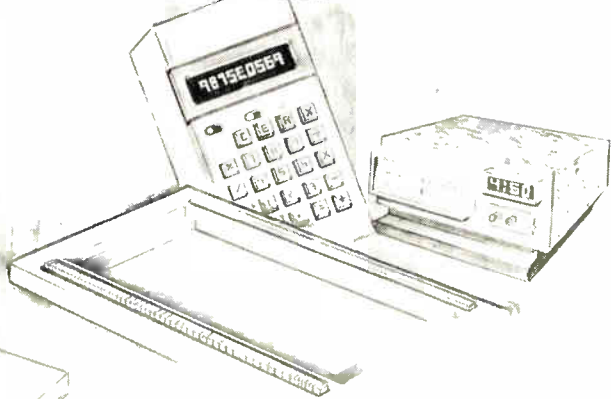




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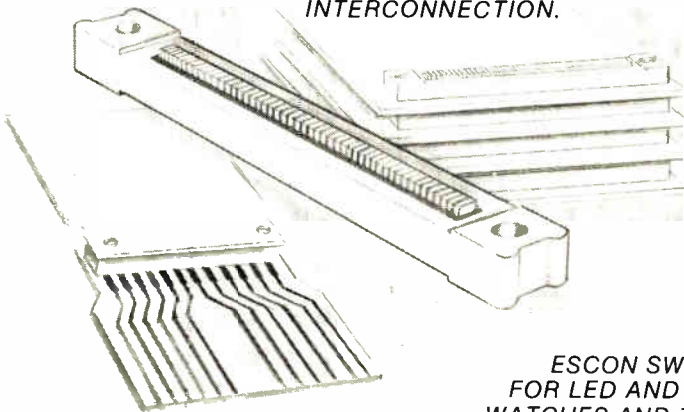


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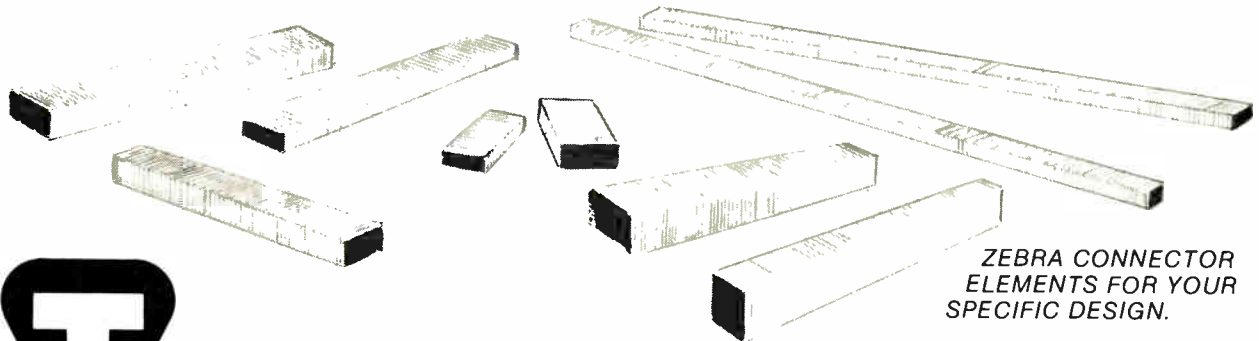


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## New products

handling 1.0 and 1.5 A at 120 v ac are offered. In 1,000-and-up quantities, the 1-A model sells for \$4.25. Delivery time is four to six weeks.

Gordos/Grigsby-Barton Inc., 1000 North Second St., Rogers, Ark. 72756. Phone (501) 636-5000 [344]

## Sealed push-button switch mounts on pc board

Designed for use on printed-circuit boards, the TL 360 series momentary-contact push-button switch is a subminiature device that is completely sealed in a silicone-rubber boot. With a diameter of only 0.36 inch and a thickness of only 0.16 in.,



the switch can be used in cramped quarters on computer boards, in radio equipment, and in other demanding situations. Good for at least 50,000 operating cycles, the switches sell for less than 25¢ each.

Standard Grigsby Inc., 920 Rathbone Ave., Aurora, Ill. 60507 [346]

## Modular switches can be custom-built by the user

Rotary switches in the Versatrol line give the user the option of making his own switches from a collection of standard parts, of buying standard units and modifying them, or of buying customized switches from the factory. The building-block approach is said to combine versatility with economy by allowing a great number of switch designs from an

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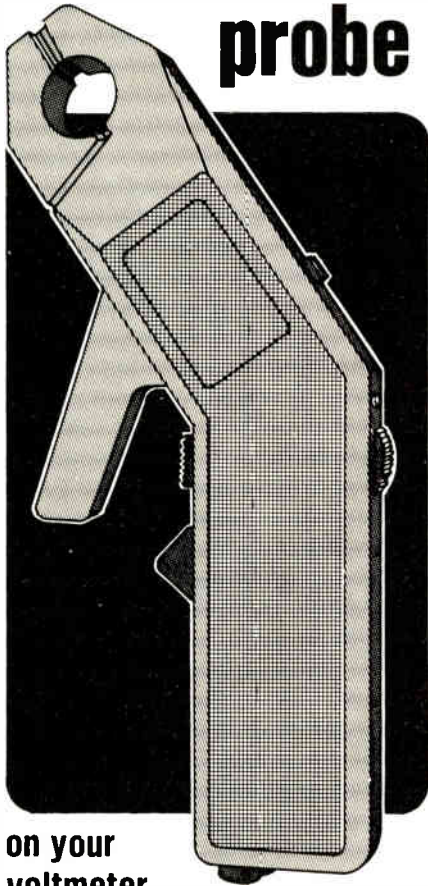
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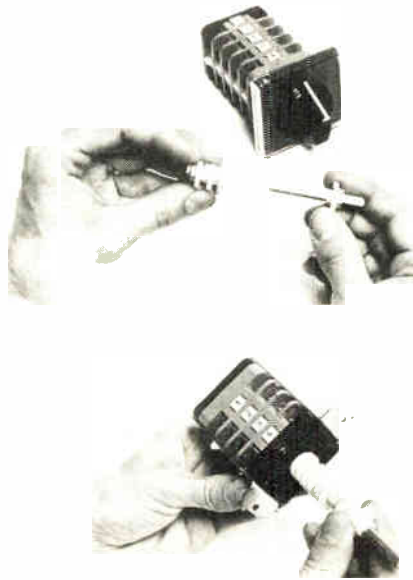
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## New products



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Cogenel Inc., Entrelec Division, Two Ram Ridge Rd., Spring Valley, N. Y. 10977. Phone (914) 425-7460 [345]

## TOPICS

### Components

**Licon, Division Illinois Tool Works Inc., Chicago, Ill.**, has added several features to its popular series 05 lighted push-button switches. These include single-pole, double-throw momentary-action switching and spdt maintained-action switching. Both switching actions have been added to the incandescent as well as the light-emitting-diode switches... **Potter & Brumfield Division of AMF Inc., Princeton, Ind.**, has redesigned its R50 series printed-circuit-board relays so that they may now be completely immersed in cleaning fluid. They can now be mounted on boards and cleaned along with other components, thus eliminating the need for two cleaning operations.

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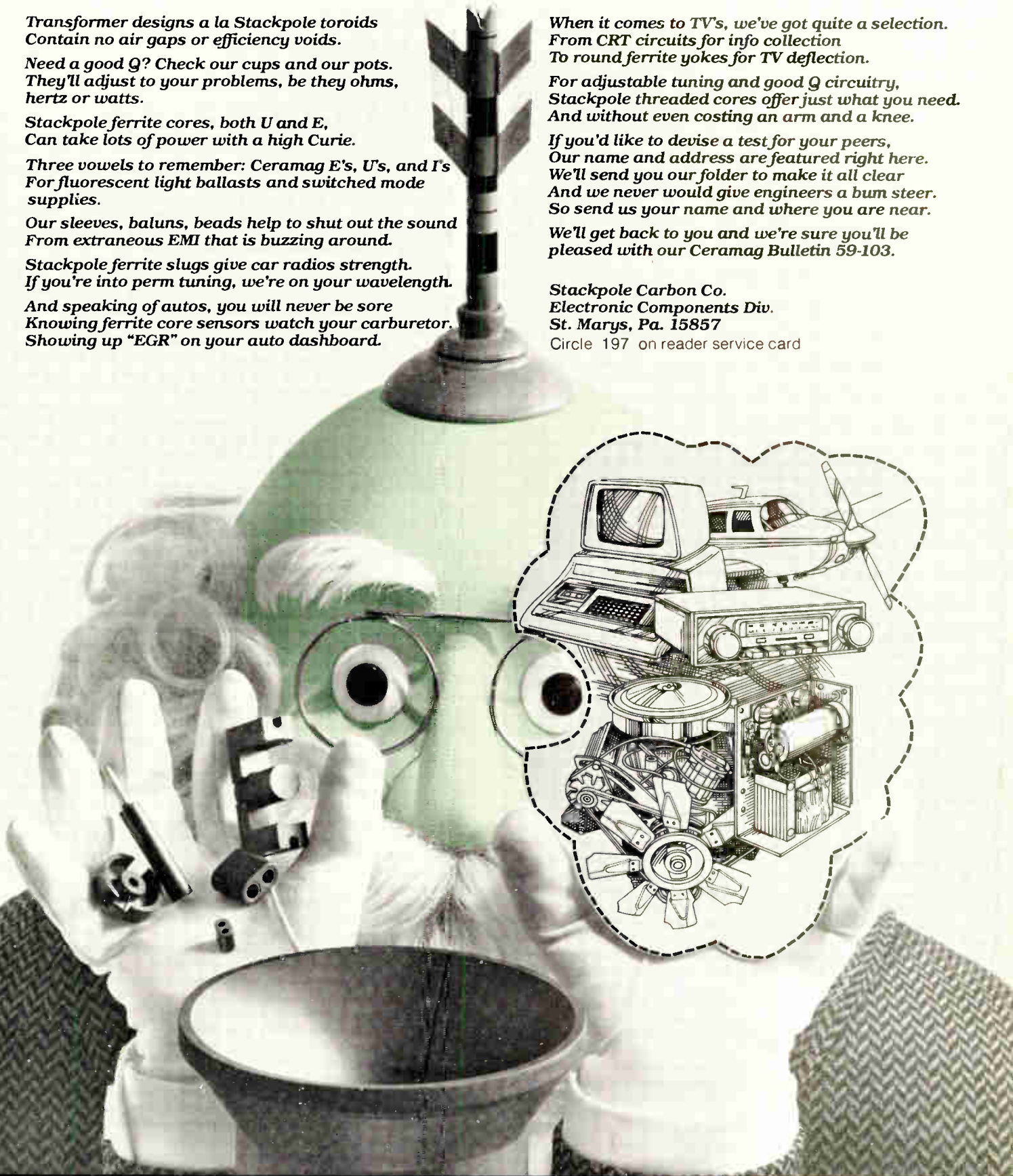
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**Stackpole Carbon Co.  
Electronic Components Div.  
St. Marys, Pa. 15857**

Circle 197 on reader service card



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Communications

## Improved fm i-f circuit includes meter drive

The CA 3189E is an improved version of RCA's popular CA 3089E intermediate-frequency system for fm receivers in high-fidelity, automotive, and other communications applications. Key advantages offered by the new chip are provision of a signal for the direct driving of a tuning meter; externally programmable recovered audio level; externally programmable automatic-gain-control threshold and voltage; deviation muting, which is combined with conventional signal-to-noise-level muting; an on-channel step-control voltage; and a S/N ratio in excess of 70 dB. The CA 3189E further contains internal power supply regulators that maintain nearly constant current drain over the voltage supply range of 8.5 to 16 v dc.

Basic features of the older chip, which are retained in the new one, include a three-stage limiting amplifier, a doubly balanced quadrature fm detector, an audio amplifier, an

automatic-frequency-control drive circuit, and S/N muting. Housed in a 16-lead plastic dual in-line package, the CA 3189E sells for \$1.88 each for quantities of 100 or more. Delivery is from stock.

RCA Solid State Division, Box 3200, Somerville, N. J. 08876 [401]

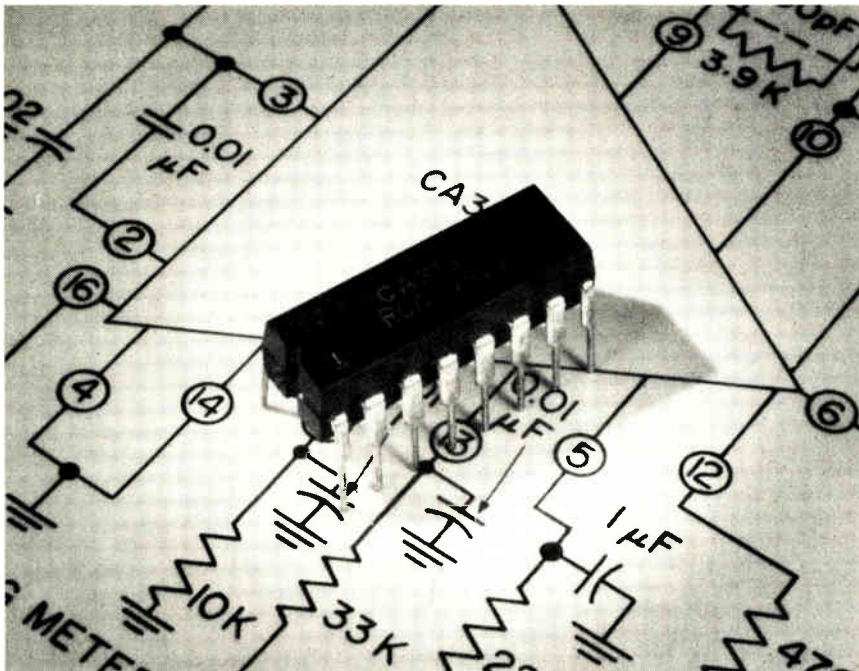
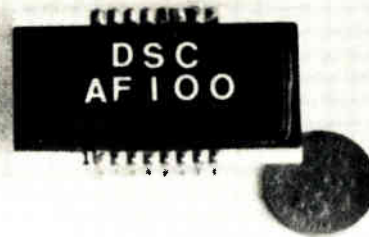
## Circuits encode, decode two-tone dialing signals

The model DTE-100 and AF-100 dual-tone encoder and dual-tone separation filter are a pair of hybrid circuits that include much of the circuitry needed for a dual-tone multifrequency (DTMF) signaling system. The DTE-100 encoder produces all 16 tone pairs in the standard Touch-Tone frequency plan. It

contains a voltage regulator and a ceramic oscillator. Intended for use in remote-control and data-acquisition systems as well as in mobile radio communications, it requires no external components. Key specifications include: frequency drift of no more than 0.25% from  $-55^{\circ}\text{C}$  to  $+80^{\circ}\text{C}$ , 900 mv rms composite output into 600  $\Omega$ , 1.7 dB of high-frequency pre-emphasis, operation from supply voltages of +7 to +20 v dc, power consumption of 100 mw. The unit measures 2 by 2 by 0.5 inches and sells for \$24.95.

The AF-100 filter is a dual RC active filter that separates the low-frequency group of DTMF tones (697 Hz through 941 Hz) from the high-frequency ones (1,209 Hz through 1,633 Hz). Contained in a 16-pin dual in-line package, it provides a minimum of 30 dB of separation between groups while keeping in-band deviation to a maximum of 1.5 dB. The filter draws  $\pm 2.5$  mA from a  $\pm 12$ -v supply and operates from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ . It sells for \$32. Like the DTE-100, the AF-100 is available from stock to three weeks.

Data Signal Corp., 40-44 Hunt St., Watertown, Mass. 02172. Phone (617) 926-5080 [403]



## Bit-error-rate test set

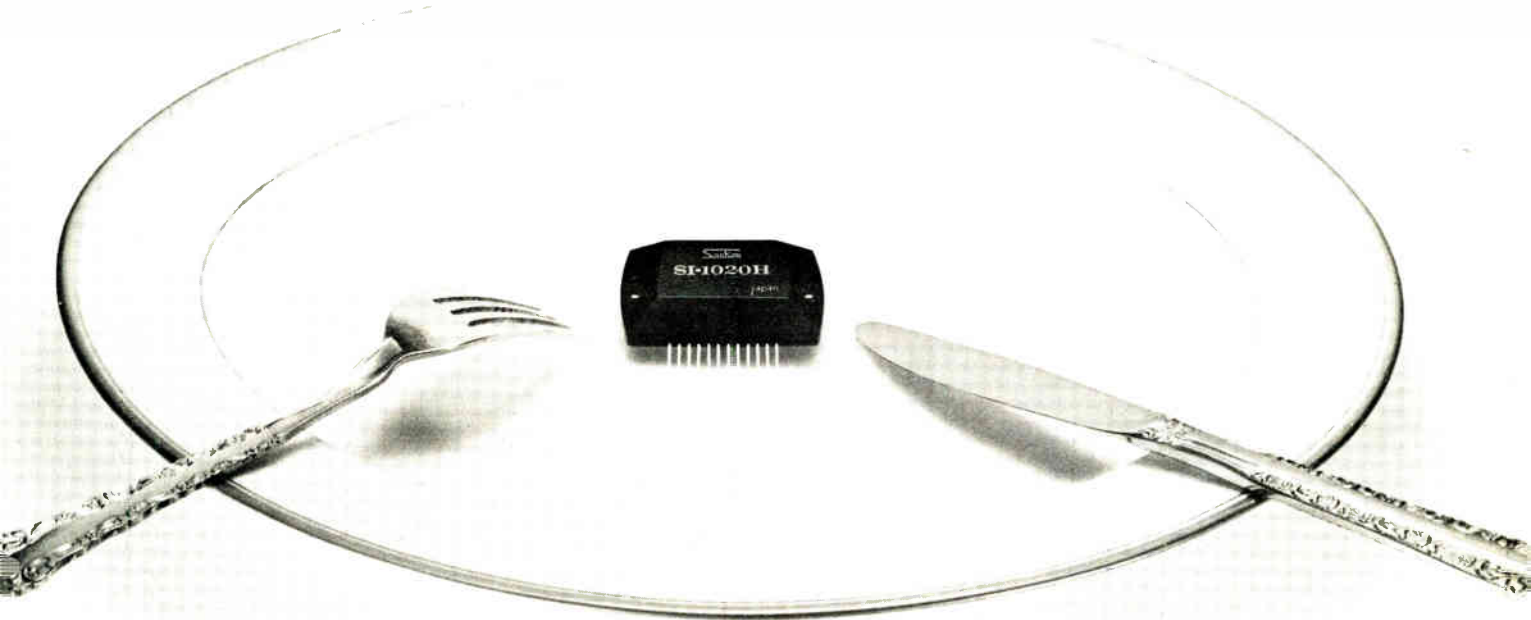
operates from 1 to 325 MHz

The MN-301 transmitter and MB-301 receiver comprise a bit-error-rate test set capable of operating over the frequency range from 1 MHz to 325 MHz. The transmitter generates two pseudorandom sequences: a short one with a length of 127 bits per frame and a long one of 32,767 bits per frame. A test mode is also provided to generate a 11001100 . . . pattern, which can be used as a synchronization and alignment signal when adjusting the receiver data-clock phase. Provision is made for both internal and external error insertion. In the internal mode, the transmitter will automatically insert 2 error bits per 100 bits of data. The errors will occur in 2 consecutive bits.



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Maximum rms Output Power		20W	25W	30W	25W per channel
Supply Voltage		$\pm 23V$ ( $\pm 20V^{**}$ )	$\pm 25V$ ( $\pm 22.5V^{**}$ )	$\pm 27V$ ( $\pm 24.5V^{**}$ )	$\pm 25V$ ( $\pm 22.5V^{**}$ )
Maximum Harmonic Distortion	$G_V = 26.5dB$ rated output 20kHz	0.2% (0.2% <sup>**</sup> )	0.15% (0.3% <sup>**</sup> )	0.15% (0.3% <sup>**</sup> )	0.15% (0.3% <sup>**</sup> )
Feedback		30dB Fixed Gain †	External	External	External
Frequency Range	$-1dB, P_o = 1W$	20Hz to 100kHz			
Power Bandwidth	THD = 0.2%, $-1dB$	10Hz to 20kHz			
Idling Current		30mA @ $V_{CC} = \pm 30V$	45mA @ $V_{CC} = \pm 30V$	30mA @ $V_{CC} = \pm 34V$	50mA @ $V_{CC} = \pm 32V$
Typical Output Noise Voltage	with recommended Power Supply, $R_g = 10k \text{ ohm}$ $G_V = 26.5dB$	0.7mV	0.4mV	0.4mV	0.4mV
Output Quiescent Voltage	Rated $V_{CC}$	100mV Maximum			
Allowable Output Short Time	Specified operation condition	2 seconds			
Operating Temperature	The temperature of heat sink	$-30 \sim 100^\circ C$			
Storage Temperature		$-30 \sim 120^\circ C$			

\* 2 channels \*\* For 4 ohm Load



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NL-8S

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NL-21 G

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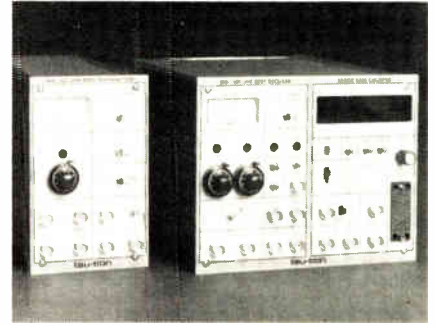
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Circle 233 on reader service card

## New products



The MB-301 receiver generates its own pseudorandom sequences, which are identical to those generated by the transmitter. Thus, once the two units are synchronized, the receiver can count errors all by itself. It features automatic synchronization, variable threshold adjustment, and a four-digit counter and display. The display can show total errors or bit error rate. The counter also has a binary-coded-decimal output for driving an external printer.

Pricing is as follows: the units are both plug-ins, which fit into a main-frame that provides power supplies and cooling and sells for \$985. The MN-301 transmitter sells for \$4,895 and the MB-301 receiver sells for \$8,140.

Tau-Tron Inc., 11 Esquire Rd., North Billerica, Mass. 01862. Phone (617) 667-3874 [404]

## Double-balanced mixer covers 10 MHz to 1.5 GHz

Intended primarily for radio-frequency signals in the 1.0-to-1.5-GHz range, such as FACAN signals, the model MD-152 is a double-balanced mixer that operates from 10 MHz to 1.5 GHz. The unit has a typical midband isolation, for both rf to local oscillator and LO to intermediate-frequency, of 40 dB. Midband conversion loss is typically 6 dB, with a single-sideband noise figure within 1 dB of the conversion loss. The two-tone intermodulation ratio is typically 85 dB at 500 MHz with -30 dBm at each input and a 50-MHz i-f. Housed in a standard TO-8 plug-in package, the wideband mixer sells for \$39 in quantities of 1 to 49.

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Cut assembly costs.

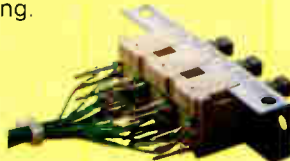
MPS switches may be mounted on the front panel, and are designed for automatic wave soldering installation and PC board cleaning. Insert molded terminals prevent flux and solder wicking and contact contamination. Integral PC board stand-offs provide for efficient board cleaning.

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## Available options.

Optional installations include ganged assemblies, front-panel mounting and wire-wrapping.



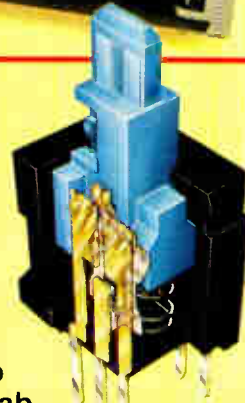
All MPS pushbutton switches are built to Centralab's highest quality standards (see specifications at right). They're priced as low as 41 cents in 1,000 quantity. For full technical details, samples and quotation, call (515) 955-3770, or write to the address below.

  
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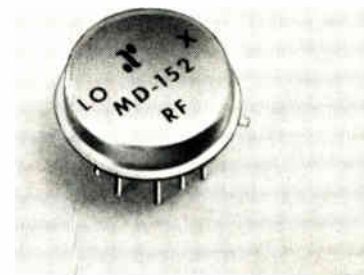
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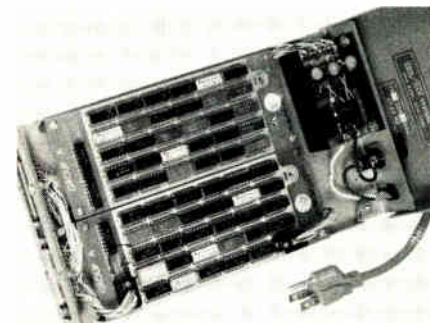
Availability is from stock.

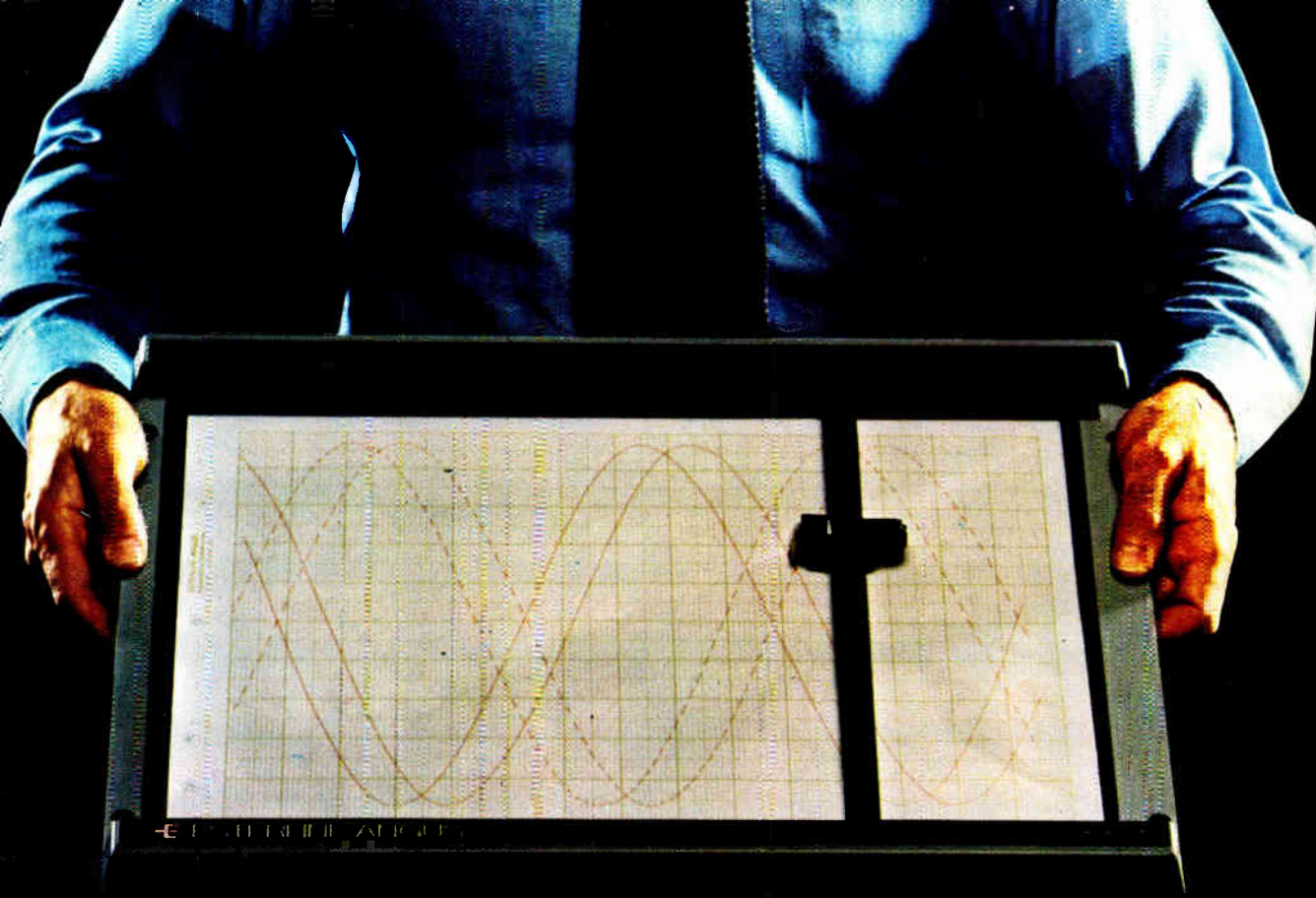
Anzac Electronics, 39 Green St., Waltham, Mass. 02154. Phone James P. Leonard at (617) 899-1900 [405]

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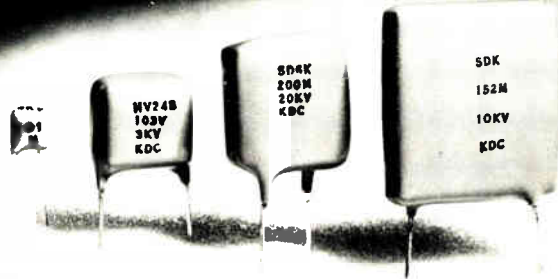


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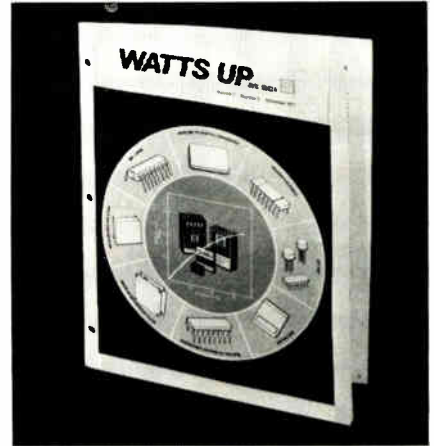
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**Power supply applications.** A 12-page journal discusses power supply decoupling, preloading, and input-transient suppression methods. It also includes descriptions of new ac-



dc and dc-dc power supplies. An attached postage-paid form is provided. Semiconductor Circuits Inc., 306 River St., Haverhill, Mass. 01830. Circle reader service number 421.

**Design data.** Technical data sheets on 18 operational amplifiers and 22 analog function modules are given in an 89-page catalog. The catalog lists all specifications, dimensions, pin connections, and external circuit connections. Optical Electronics Inc., P. O. Box 11140, Tucson, Ariz. 85734 [422]

**Specification.** The Institute for Interconnecting and Packaging Electronic Circuits is offering a new specification, IPC-S-815, "General Requirements for Soldering of Electrical Connections and Printed Board Assemblies." The specification defines the approved materials, methods, and inspection criteria. It includes information on terms and definitions, materials, components, presoldering tools and equipment, soldering preparation, and quality assurance. In addition, there are sections on component lead forming and attachment, and machine reflow and nonreflow soldering. Copies can be obtained at \$5 each for nonmembers and \$3 each for members. IPC, 1717 Howard St., Evanston, Ill. 60202

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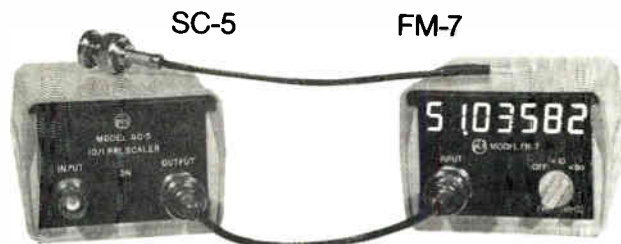
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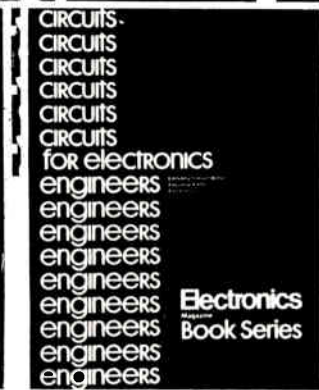
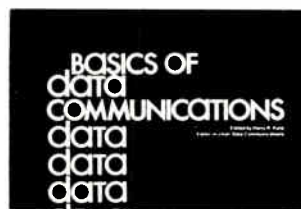
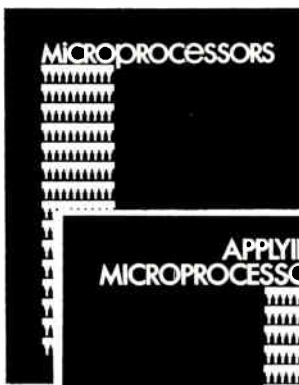
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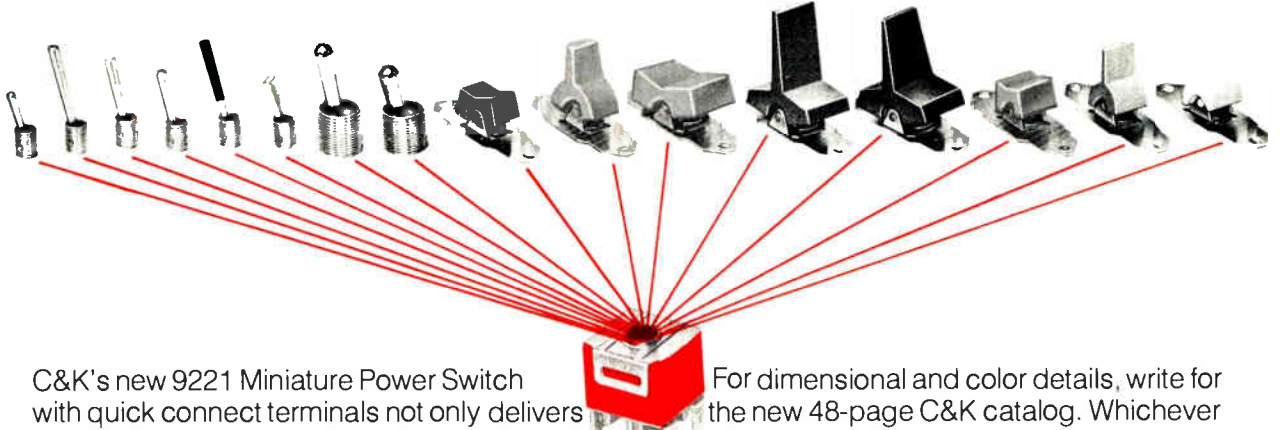
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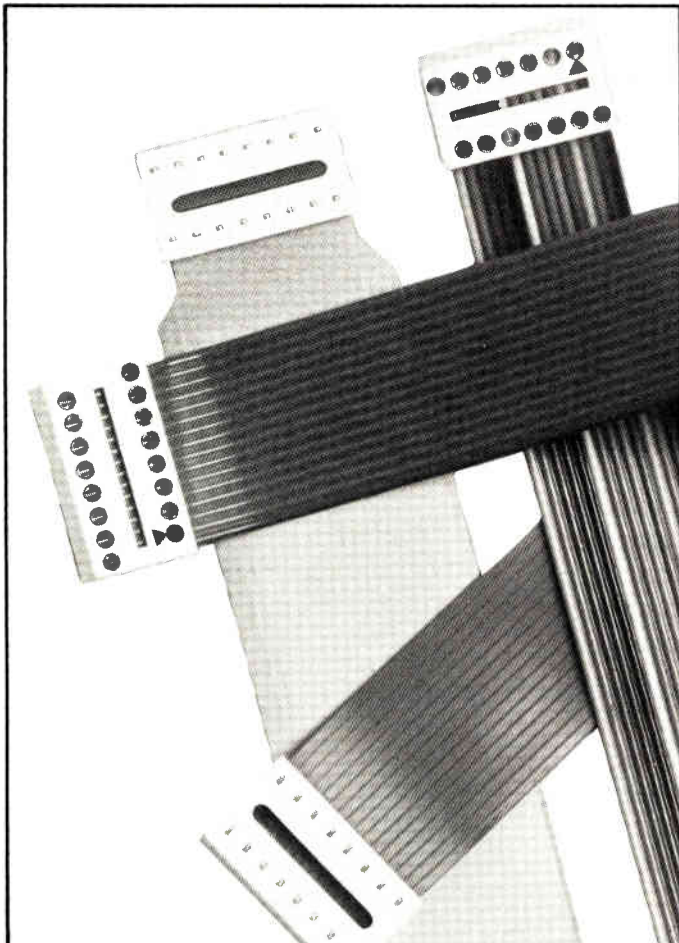
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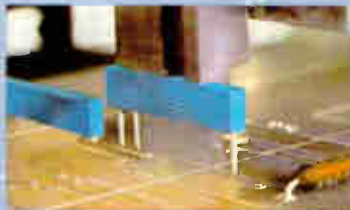
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