JULY 8, 1976

DEDICATED CHIP FAMILY TAKES ON MICROCONTROLLER JOBS/84

A hardware-oriented approach to microprocessor programming/93

How to minimize rfi problems with ac relays/101

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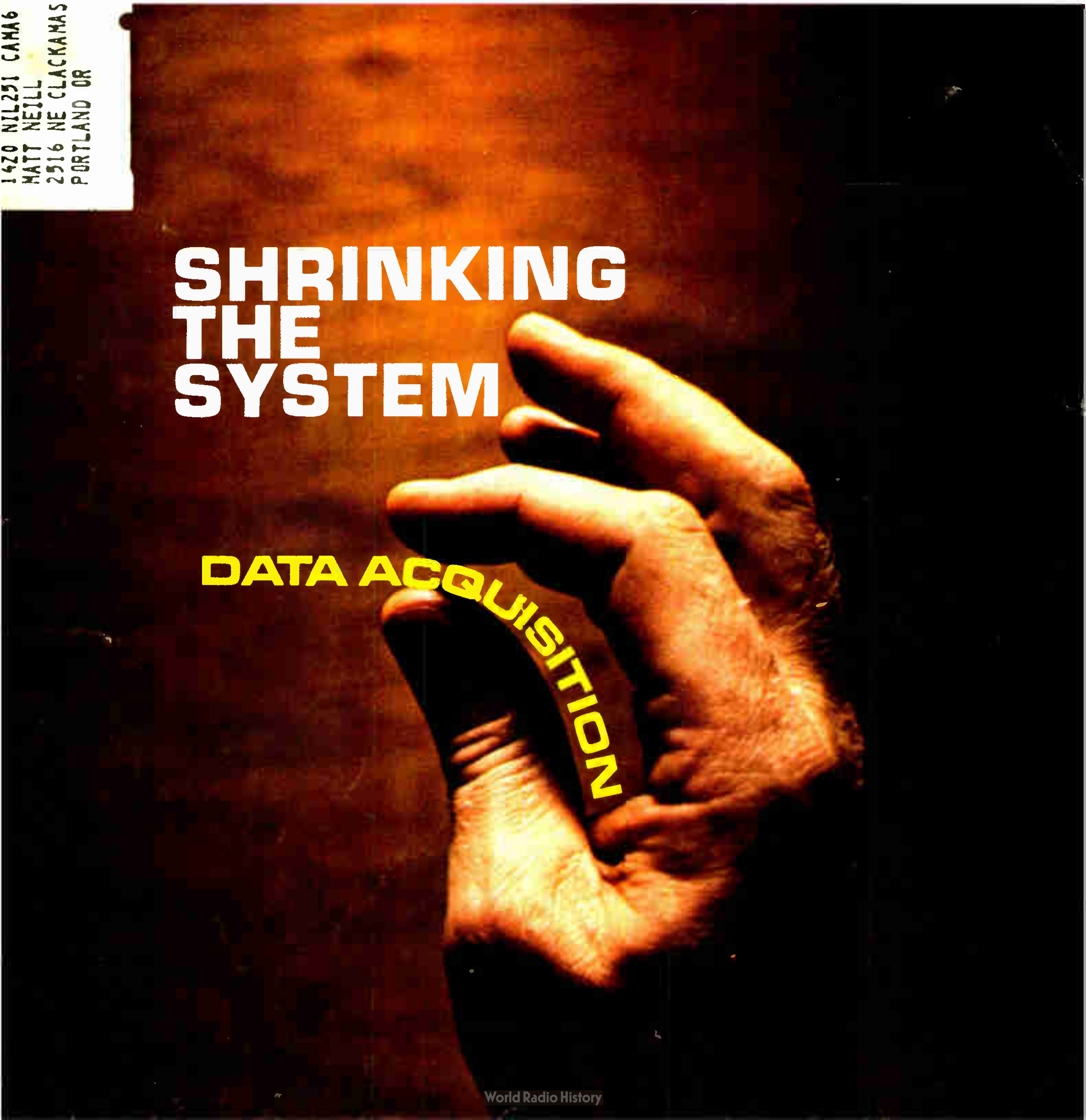

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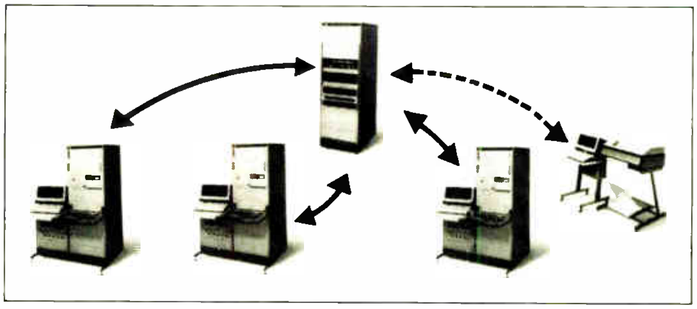

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Circle 1 on reader service card

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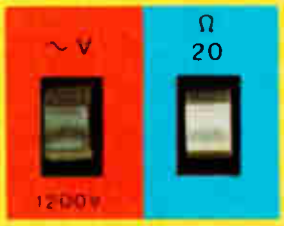
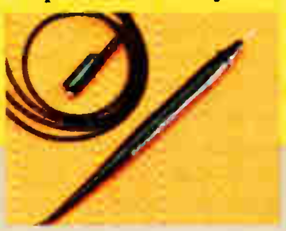
Autoranging and manual modes,

Wide measurement ranges,



And touch-hold probe accessory.



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Circle 2 on reader service card

Electronics

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Highlights

The cover: Data acquisition in a DIP is a reality, 77
Thin-film hybrid technology shrinks an 8-bit eight-channel data-acquisition system into a single, 32-pin, dual in-line package. The device is an excellent interface element between the digital world of the microprocessor and the real analog world.

Cover photograph is by Art Director Fred Sklenar.

Avionics on target for Space Shuttle, 59
The avionics hardware for NASA's Space Shuttle Orbiter is nearly completed, with no major hitches that might delay the September rollout of the first of these reusable manned spacecraft.

Low-cost chips aim at dedicated control, 84
A family of microcontroller chips makes it possible to substitute a single large-scale integrated chip for the relays, springs, gears, and timers usually used in low-speed, high-volume control systems in the home and on the job.

Writing programs is like designing hardware, 93
The process of writing and debugging a program for a microprocessor closely resembles that of designing and debugging hardware, and so following similar procedures enables the engineer to be his own computer programer.

And in the next issue . . .
A special report on hybrid circuit technology . . . a technical update on bar-graph displays.

Electronics

Publisher's letter

Programing of microprocessors is worlds apart from wiring up a breadboard. Right? Not so, says Pro Log Corp.'s Ed Lee, who, in the article that starts on page 93, details what he calls the "surprising similarities between hardware design and microprocessor programing."

Indeed, says Lee, an engineer "can build on his hardware background and write and debug a program just as efficiently as he can wire up and debug a breadboard." And he has a lot of experience to back up his position. An MIT graduate who set out for the West Coast when he graduated in 1958, he is at once an engineer and a businessman busily going through his second experience in founding a company. Pro Log, Monterey, Calif., was started by Lee in 1972 after he left MSI Data Corp., where he had been one of three founders.

Lee says that Matt Biewer, an engineer whom he first met at Electrodata, Pasadena, developed the engineering approach to microprocessor design that is described in the article. That was in 1972 when he began working with the first microprocessor out on the market, the Intel 4004. Biewer is now engineering manager for Pro Log, while Lee serves as president and marketing director.

Lee expresses strong opinions about the 4004, although it has been upstaged by a host of newer devices. He notes that the 4004 is still selling more units per month than the 8080.

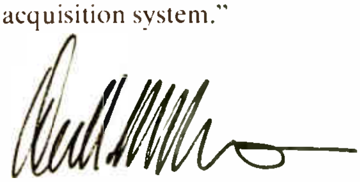
Lee is particularly sensitive to the problems of field-service personnel. "A good chip should not have more than 50 instructions, or else the field guy won't understand it."

A lot has happened to data-conversion products in the nine years since Robert Calkins first starting designing them. He's seen data converters evolve from rack-mounted boxes to encapsulated modules to hybrid circuits to monolithic chips. And now, through thin-film hybrid technology, a complete data-acquisition system has been put in a single dual in-line package. Calkins, manager of circuit technology, headed the design team at Micro Networks for this device and, with Arthur Berg Jr., wrote the article that starts on page 77.

"Data conversion intrigues me because we live in an analog world, but we do so many things digitally in electronics. Developing these products that communicate between the two worlds is exciting."

As in the past, the future of thin-film hybrids, Calkins believes, is closely tied to the development of monolithic chips. The MN7100 data-acquisition system, for instance, became feasible because high-quality monolithic eight-channel multiplexers, as well as 8-bit digital-to-analog converters, are available today.

Calkins predicts that within a year a good-quality monolithic 12-bit d-a converter will emerge, making possible a 12-bit hybrid data-acquisition system in a DIP. And when microprocessors become available in unpackaged chip form, "then there will be the so-called smart data-acquisition system."



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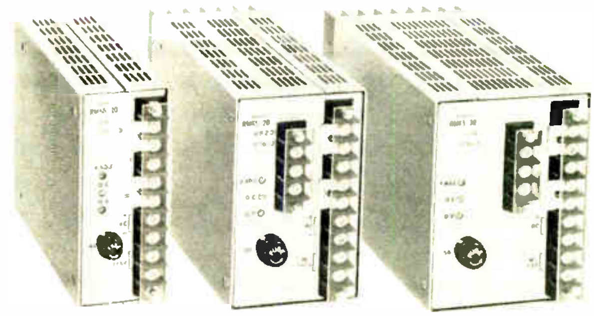

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Reader's comments

80% of data business continues

To the Editor: In the International Newsletter item on Mullard Research Laboratories' microprocessor-based optical character reader [May 13, p. 55], the sentence, "Parent Philips, which has left data processing . . . ," surprised us.

We have said that we intend to stop production of medium and large computers because cooperation within Unidata was no longer maintainable. This represents 20% of our Data Systems division's turnover. So 80% of its activities will continue: office and small business computers, data-entry equipment, minicomputers, and terminals.

J. W. M. Martinot
N. V. Philips Gloeilampenfabrieken
Eindhoven, the Netherlands

Of duty cycles and stability

To the Editor: It may be worth noting that, in the 1973 Signetics 555/556 timer-application booklet, page 15 shows a circuit, producing a 50% or less duty cycle that is by no means complex or unstable—shortcomings raised in the first paragraph of "IC timer circuit yields 50% duty cycle" [May 13, p. 95].

In the Signetics circuit, a diode conducting towards ground is connected across pins 6 and 7, making the charge and discharge resistors independent of each other at any duty cycle. The upper resistor charges the capacitor through the forward-biased diode, while the lower resistor discharges the capacitor with the diode back-biased.

R. J. Isaacs
Clinical Research Centre
Harrow, Middlesex, Great Britain

■ **The author replies:** *Obviously, this particular circuit is not one of the ones I noted as having such shortcomings. However, in the circuit that I described, the timing capacitor charges and discharges through a single timing resistor that may be varied to change the frequency of operation without changing the circuit's established 50% duty cycle. To accomplish this in the Signetics circuit, both timing resistors must be replaced with a dual potentiometer having precise tracking characteristics.*

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Our LSI-11, the machine on the left, makes getting into microcomputers easy.

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But if you want things even easier, you can buy your LSI-11 in a box, complete with power supply and fans. It's called the PDP-11/03, it's the one in the middle, and it costs just $2495 in single quantities.

Easiest of all, especially for complex systems development, is the PDP-11V03 on the right. It gives you a roll-around cabinet with an 8K LSI-11 in a box, an RXV-11 Dual Floppy Disc Drive and bootstrap for mass program storage, and our RT11 operating system — plus your choice of video or hard-copy keyboard terminal. It sells for a low package price of just $10,450 in single quantities.

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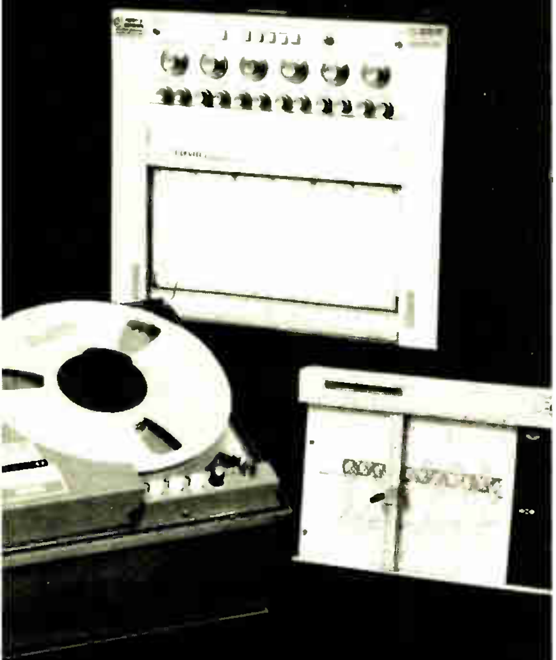


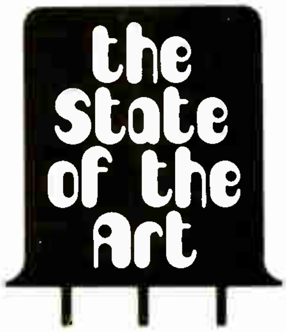
News update

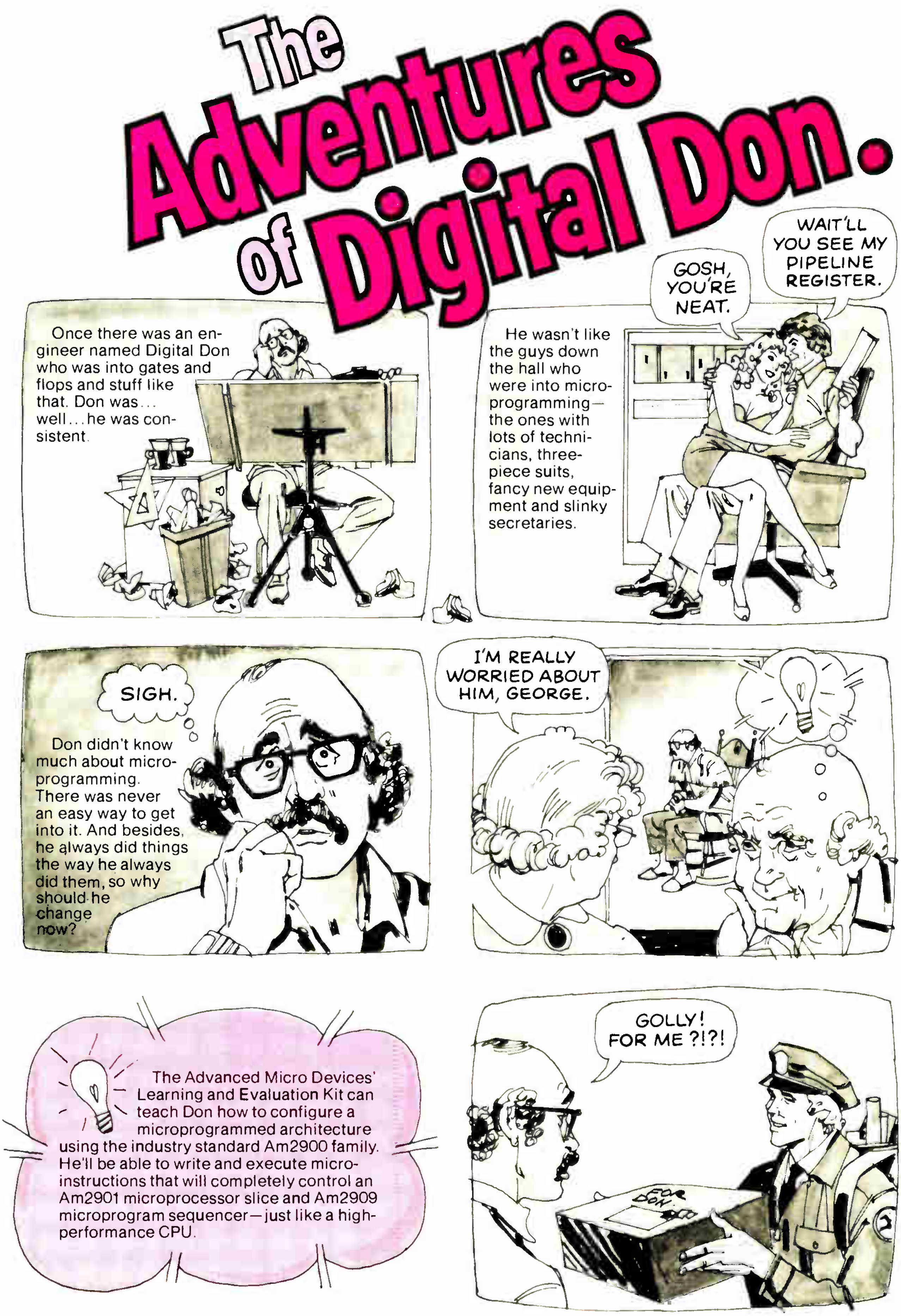
■ Pioneering California legislation that would have given engineers in that state the rights to their own inventions has gone back to the drawing board. The bill has been killed by the State Senate's Judiciary Committee, but it will be reintroduced during the next legislative session. However, the new measure will have one major change: it will apply only to engineers who work independently on inventions on their own time and outside company premises.

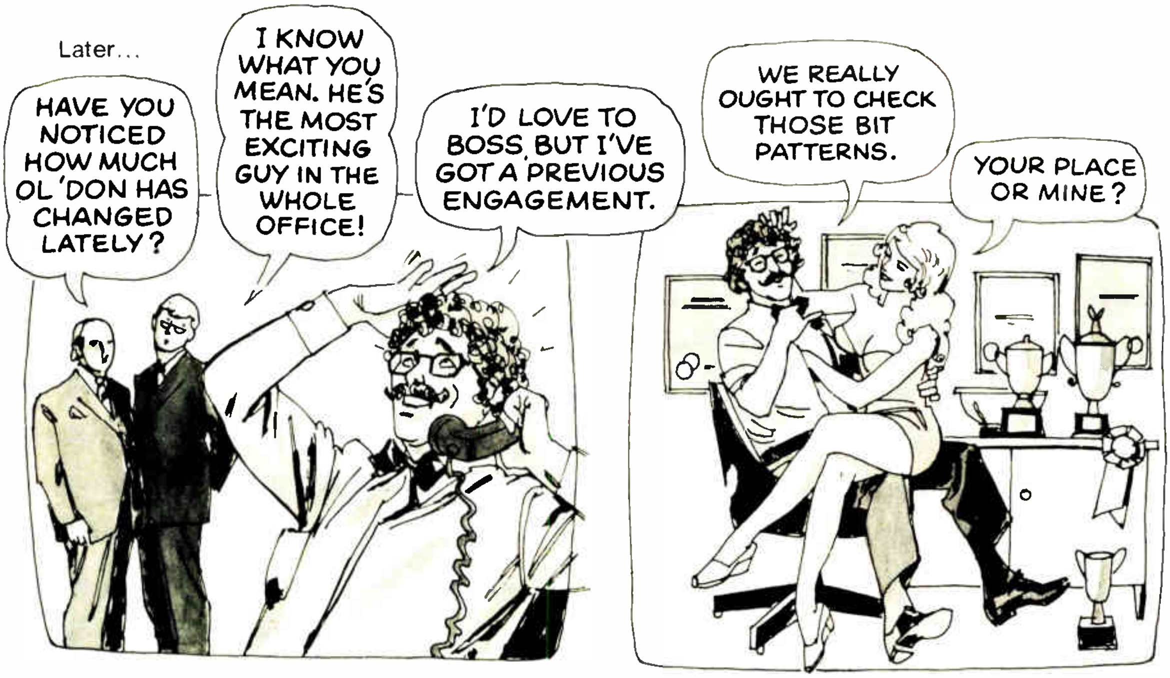
The legislation that died in committee provided that an employee may patent his invention unless his employer establishes interest in it within four months [*Electronics*, May 13, p. 72]. In that case, the two parties would have to get together and agree on payment: failing that, says the bill, remuneration would be set by a court. The bill's failure in committee probably was caused in part by its weakness, but it wasn't helped by strong industry opposition. For example, companies ranging in size from General Electric and Westinghouse to Atari Inc., a maker of video games, opposed the measure, as did the influential Association of Motion Picture and Television Producers.

■ The time for a digital wristwatch circuit using a resistance-capacitance, rather than a crystal, oscillator may have passed. The circuit, developed by Exar Integrated Systems Inc. of Sunnyvale, Calif., in conjunction with a major watch manufacturer, would have used integrated injection logic in a one-chip design with retail price goal of less than $30 [*Electronics*, July 10, 1975, p. 29].

But Exar was forced to discontinue its work last fall after the customer that had asked for the work decided there was a more economical way to do it, a decision shaped mainly by a drop in the price of crystals. And, as Alan Grebene, Exar's vice president for engineering, points out, the project was undertaken strictly as a one-customer effort.




The Adventures of Digital Don.
Once there was an engineer named Digital Don who was into gates and flops and stuff like that. Don was... well... he was consistent.
He wasn't like the guys down the hall who were into microprogramming—the ones with lots of technicians, three-piece suits, fancy new equipment and slinky secretaries.
GOSH, YOU'RE NEAT.
WAIT'LL YOU SEE MY PIPELINE REGISTER.
SIGH.
Don didn't know much about microprogramming. There was never an easy way to get into it. And besides, he always did things the way he always did them, so why should he change now?
I'M REALLY WORRIED ABOUT HIM, GEORGE.
The Advanced Micro Devices' Learning and Evaluation Kit can teach Don how to configure a microprogrammed architecture using the industry standard Am2900 family. He'll be able to write and execute microinstructions that will completely control an Am2901 microprocessor slice and Am2909 microprogram sequencer—just like a high-performance CPU.
GOLLY! FOR ME ?!?!
FOR DON



The Am2900K1 Learning and Evaluation Kit.

It's terrific. For only $289.00 you can master the basic theory and application of microprogramming. Here's what you get:

A read/write memory storing up to 16 microinstructions driving a pipeline register. From the pipeline register, the microinstructions control: an Am2901; circuits for logical and arithmetic shift and rotation; and the Am2909 sequencer that selects the next microinstruction address. Sixteen sequence control functions are built in, including conditional branch, loop, jump to subroutine and return. Built-in display logic makes nearly every point in the system available at an LED display.

The Kit includes forty IC's, LED's, switches, resistors, decoupling capacitors, PC board and a really comprehensive manual covering assembly instructions, theory and experiments. The only thing you need to add is a 5-volt power supply.

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Circle 259 on reader service card

Editorial

Interfacing instruments—and engineers

The headache of lashing instruments together into a test system has been eased a bit by the growing acceptance among the world's instrument makers of a standard interconnection method. The instrument interface bus has been promulgated as an IEEE standard, has been adopted by the American National Standards Institute, and is close to final acceptance by the International Electrotechnical Commission.

While engineers who are familiar with the intricacies of the standard aren't unanimously in favor of the interface bus, nevertheless, for bench-top test setups, the approach greatly streamlines the meshing of instruments to the test job at hand—and the retailoring of the instrument assembly to the next job. Because it is aimed at that kind of job-by-job instrumentation change, and to small-volume and calculator-based test systems, the standard has had little impact on the big, commercial dedicated test systems.

Yet, while the interface concept is fairly straightforward, some engineers have complained that the standards document is unnecessarily complex. In particular, some engineers who have had experience with interfacing test systems to computers consider the instrument interface standard harder to work with than the computer interface documentation.

It would be regrettable if the progress in coordinating the communication of data between instruments should falter because of a communications gap in its documentation. Since the concept has now gained some degree of initial acceptance, this is the time for the IEEE Standards group that established the standard in the first place to consider revising the document. Such a revision, both clarifying the more complicated areas and incorporating the experience of those who have had time to utilize the concept, would accelerate adoption of a valuable technological tool.

IEEE tightens voting process

Now that the IEEE election is officially a three-man race for president and a two-man contest for executive vice president and in addition involves two highly controversial constitutional amendments dealing with dues increases and publicizing future propositions, it is encouraging that the ballot preparation, handling, and tabulation procedures have been tightened.

When we wrote a year ago that these procedures should not be an issue and suggested that the institute set up a contract with an independent third party to run the entire balloting, our view was that the vote counting should be above suspicion. Now the Institute of Electrical and Electronics Engineers has gone a long way toward satisfying this ideal, though it has stopped short of turning over the entire operation to a third party.

Instead, a nationally known guard service will monitor every step of the ballot operations, from printing to mailing to return. Pre-punched ballots will be used, so that the returns will be machine-counted, the results stored on magnetic tape, and the tapes kept by the guard service until the totals are run off at the end of the voting period.

Two of the steps most vulnerable to cheating have been eliminated. First, the guard service will pick up the mail at a special post office box and deliver a day's worth of processing to the IEEE facility in Piscataway, N.J. So the ballots will be in the possession of the outside guard except when being tabulated. Second, because of the pre-punched cards, there will be no need to key-punch cards from marked ballots, which could be a source of error or suspicion.

This system is not perfect—but it is a great improvement over the loose kind of operation that was used in previous IEEE elections.

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Silent operation.
Gone are the clatter and problems associated with mechanical printers. Rather than using ink, ribbons or chemicals, EPN3000 printheads indicate by heat. On readily available thermal paper. Silently. With alphanumeric capability.

Typical of the series (see box) is the 12-column, 60-dot EPN3112 shown above. Using high-reliability beam leads, the EPN3112 consists of twelve silicon chips each with five dot mesas. A 5x7 character matrix is produced by a series of horizontal "dot lines", sequenced with a seven-step vertical paper movement to produce a "character line".

Series EPN3000.

Type	Dimensions	Description
EPN3300	.40 x .60 in	7-dot column printer
EPN3100*	.435 x .892 in.	4-column, 20-dot line printer
EPN3112	1.360 x .892 in	12-column, 60-dot line printer
EPN3600	.626 x .819 in	5 x 7 matrix printer

*Stackable to any length.

The new EPN4000 series continuous dot line printers will be introduced in the 3Q of 1976, featuring the EPN4050 50-dot printer, stackable to any length.

Built-in EPN3100/3112 electrical interconnections and blocking diodes allow electrical strobing and reduce both number of external connections and peak power requirements. In fact, peak current per dot is so low (on the order of 170 to 250 mA) that series EPN3000 is ideal for portable, battery-powered applications.

TI-3100, 3112 and 3300 printheads are designed for pressure contact to a standard flexcircuit. And the small, .435 x .892 in. EPN3100 is dimensionally controlled to permit side-by-side mounting of multiple units.

Rapid operation.
To print one dot line takes 25 to 50 ms, depending on pulse width and supply voltages.

Reliable operation.
Proven in the field for two years, EPN3100 reliability is greater than 12,500 operating hours MTBF (90% confidence level). At a normal operating rate of 6,000 character lines per hour—that's 75 million character lines (MPBF).

Thermal line printers are available in various dot matrices to accommodate varied printer requirements. And TI can also supply all the logic and drive circuitry necessary for your application.

Series EPN3000 printheads. The solid state solution to ribbons, springs and hammers. For data sheet and applications note, write: Texas Instruments Incorporated, P.O. Box 5012, M/S 308, Dallas, Texas 75222.

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People

IR's Cooper is setting out to add many new products

"I'm not standing on the sidelines, urging them on anymore," remarks David Cooper, named last month to head the new Electronic Products Group at International Rectifier Corp.'s reorganized Semiconductor division. For the past four years, he had been keeping an eye on the business side of things as IR's engineering vice president.

Cooper's new group handles the low-power (35 amperes and down) product line—the transistors, zeners and rectifiers—seen as the fastest-moving part of the discrete-semiconductor market. Growth rates, according to Cooper, are between 17% and 25% annually, twice that of higher-power devices.

And Cooper, who figures International Rectifier stands third in number of low-power discrete products behind RCA Corp. and Motorola Semiconductor, is glad he's no longer on the sidelines. He's looking forward to a determined assault on the two leaders.

His division will challenge RCA and Motorola "across the board," he asserts. And it will do so by moving up in numbers from approximately 75 to 200 products, featuring new Schottky rectifiers in current ranges of 8 to 60 amperes, by the end of the year. International Rectifier could quadruple low-power discrete sales within a year to 18 months, he predicts. The devices made by his division accounted for about 30% of 1975's $42 million semiconductor volume for International Rectifier.

Hard-glass edge. The edge, he maintains, is IR's hard-glass-passivated-chip technology that offers lower leakages and higher reverse voltages. "We'll be into voltage ratings that other people either don't make or don't make well," he says, wishing to dispel the image of his company as "a conservative high-power house making good devices with amp ratings in the hundreds."

Cooper's division had product expansion in mind before a May company restructuring. Weak demand for high-power rectifier devices over the past year had hit hard, causing declining sales and the first red ink for semiconductors in 12 years. His Electronic Products Group, together with groups devoted to power discretes, power integrated circuits, military devices, and optoelectronics, were carved out of what had been International Rectifier's umbrella Semiconductor division. It's hoped that the new and smaller groups will be able to focus on customers' needs better.

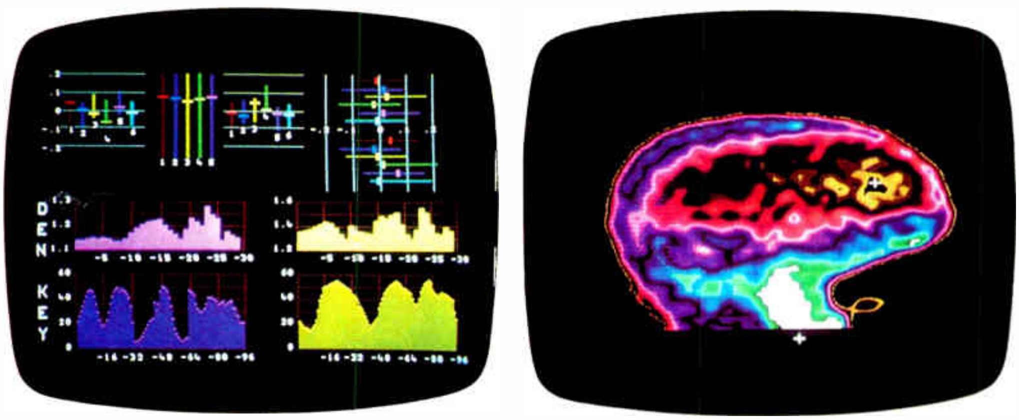
Add-on. The goal for David Cooper's electronics group is 200 products by year's end.

Pepper is out to match monolithics to converters

Robert S. Pepper doesn't believe in job-hopping, but he got an offer from Analog Devices Inc. that he says he couldn't refuse. He's the new director of research and development at Analog Devices' Semiconductor division, Wilmington, Mass., which makes linear bipolar integrated circuits.

He assumed the post recently after serving six months in the Advanced Electronics Laboratory of Raytheon Co.'s Missile Systems di-

RM 9000. The totally modular graphics and imagery system from Ramtek.



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The RM 9000's modular design provides long-range benefits as well. As your applications change or grow, so can your Ramtek Imager. A comprehensive list of options, such as grey-scale, color, and graphics generation, are simple plug-in modules. This enhances the cost effectiveness of the RM 9000 by permitting the addition of specific options as needed.

Functional, reliable, maintainable.

The RM 9000 series is the first raster scan graphics and imagery system to be totally microprocessor controlled. Implementation of a higher-order user language minimizes programming costs without sacrificing system throughput. Reliability is the direct result of intensive testing of components and systems prior to shipment as well as the exclusive use of solid-state components and printed circuit construction throughout the systems. As a result, no special preventive maintenance measures are required. In fact, your Ramtek Imager can be pre-programmed with a self-diagnostic capability.

You need to know more.

To fully appreciate the RM 9000's capability, you need more details. Call or write Ramtek Corporation, 585 N. Mary Ave., Sunnyvale, CA 94086. (408) 735-8400

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vision. "I left Raytheon for an outstanding opportunity to return to my first love," says the articulate Pepper, who spent 11 years producing hybrid data converter products at Sprague Electric Co. "And that's working on precision analog circuits in an R&D group."

He's particularly excited about pushing monolithic integrated circuits further into the world of the precision data converters and computational circuits and amplifiers that supplies Analog Devices' bread and butter. The company earns more than $30 million a year.

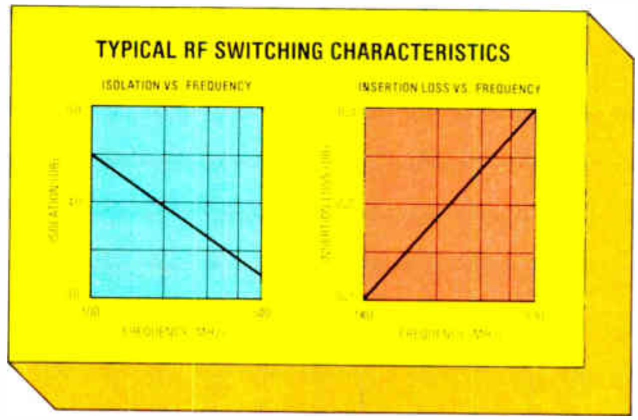
Combining processes. "I think the monolithic technology has most of the things the hybrid people have in their bag of tricks." Thus, he's looking for ways to combine monolithic processes on a single chip to optimize circuit performance the way hybrid-module makers can. One way he's investigating is to use ion implantation to make bipolar devices with field-effect-transistor front ends. This bi-FET technique allows independent control over dopants for the junction FET's pinchoff and breakdown characteristics. "That's tough to do if you have to dope the JFET at the same time you diffuse the bipolar transistors," Pepper points out.

Analog Devices has its chips ion-implanted by an outside service now, but there are plans to buy an implanter, he says. Similarly, he's evaluating computer-aided-design systems for mask layout to get the exact resistor and transistor matching required in the precision circuits. "We've sent some masks and layouts out for cutting via digitized inputs with good results. And we're evaluating whether CAD is cost-effective."

But while Analog must know how to interface well with microprocessors, which are fueling the vigorous growth in the data-converter market, Pepper isn't tempted to make the microprocessor itself. Says he, "We want to capitalize on the things we really do well, and we don't want to do anything that will limit our growth by diluting our efforts."

TO-5 RELAY UPDATE

The world's smallest RF relay



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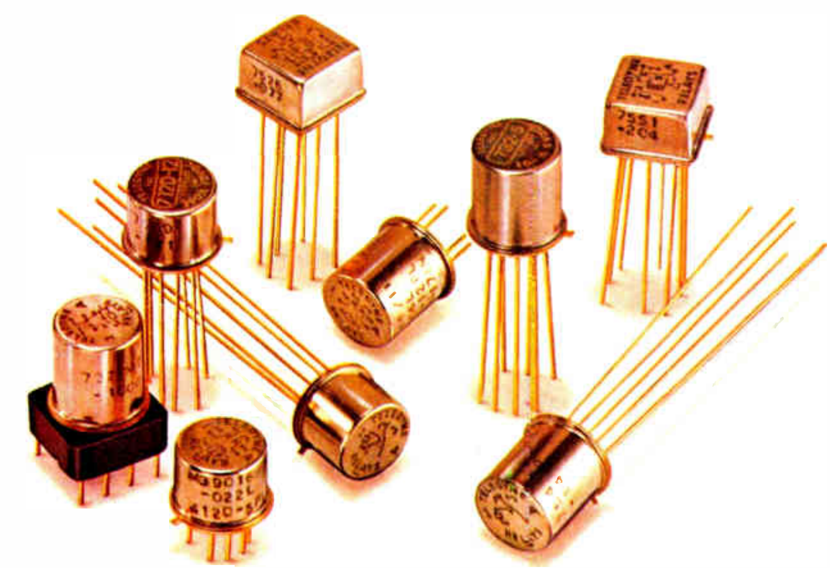

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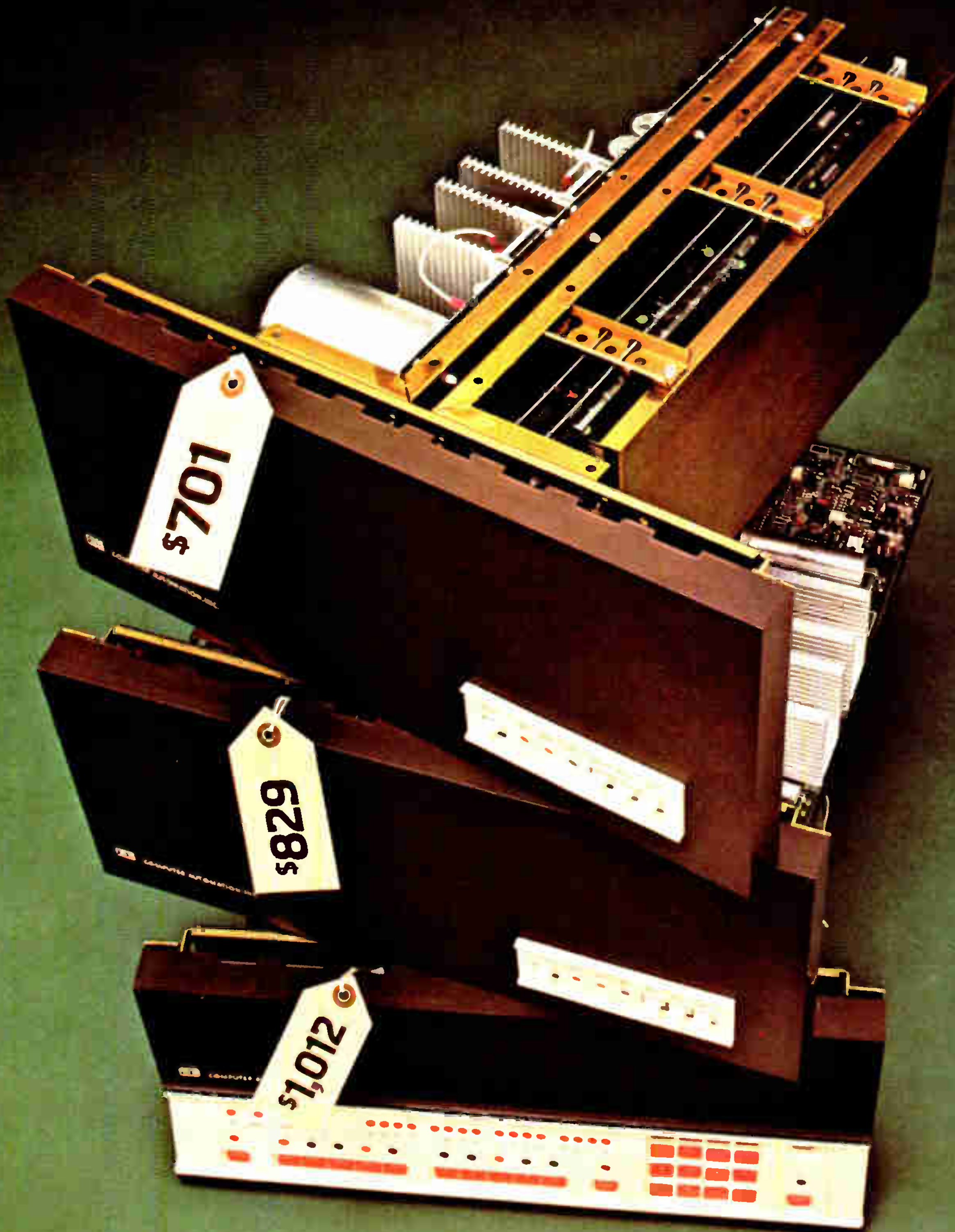

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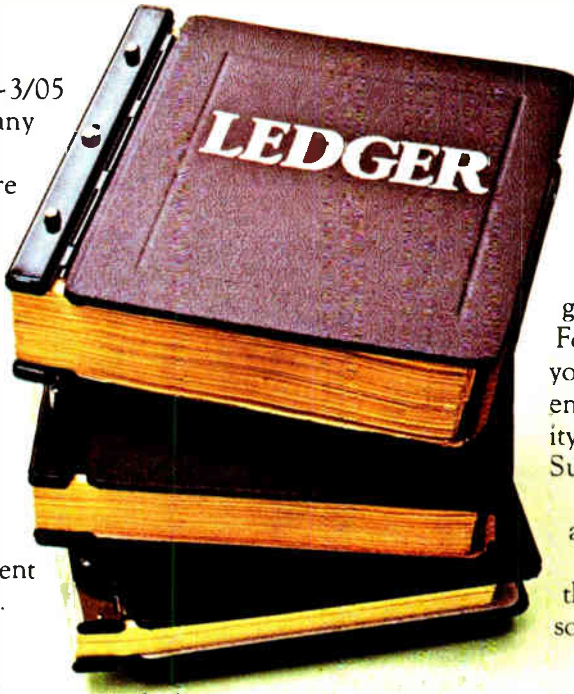

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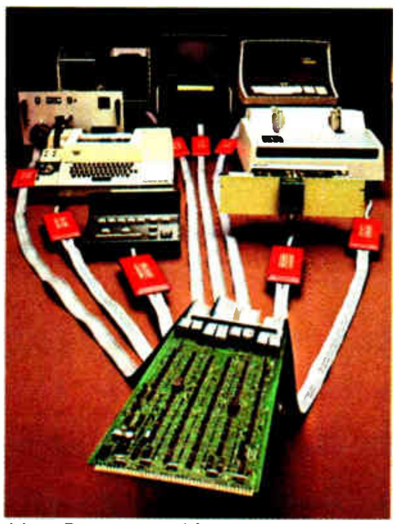

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Meetings

International Omega Association Meeting, IOA (Arlington, Va.), Sheraton National Motor Hotel, Arlington, Va., July 27–29.

Nuclear and Space Radiation Effects Conference, IEEE, University of California, San Diego, July 27–30.

1976 Joint Automatic Control Conference, IEEE *et al.*, Purdue University, Lafayette, Ind., July 27–30.

International Conference on Computer Communication, International Council for Computer Communication, Royal York Hotel, Toronto, Canada, Aug. 3–6.

Distributed Data Processing Conference, American Institute of Industrial Engineers, Jack Tar Hotel, San Francisco, Aug. 3–6.

IFIP Congress 77, International Federation for Information Processing, Four Seasons Sheraton Hotel, Toronto, Canada, Aug. 8-12.

Conference on Algorithms for Image Processing, Engineering Foundation (New York, N.Y.), Franklin Pierce College, Rindge, N.H., Aug. 8–13.

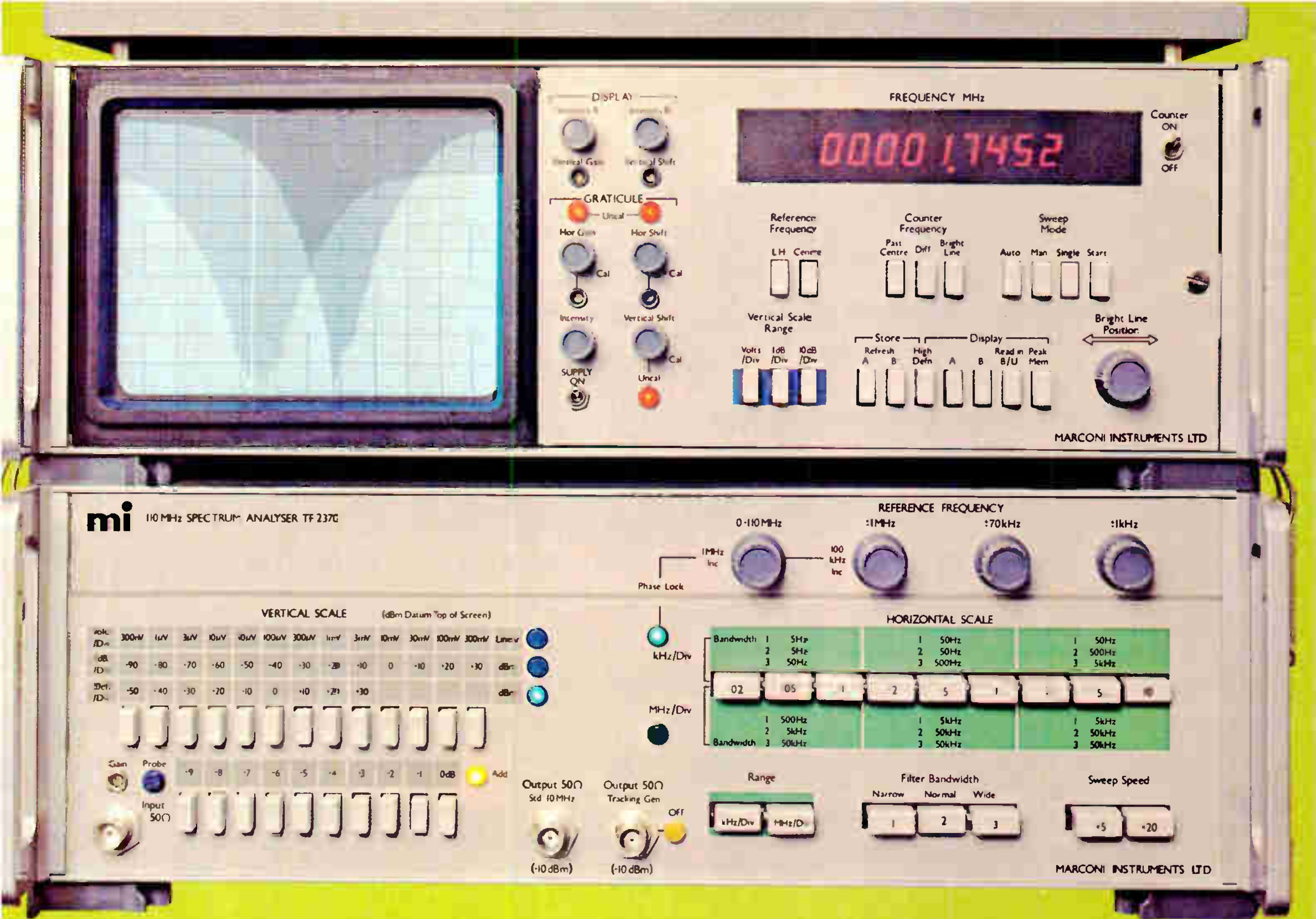
Symposium on Control in Transportation Systems, IFAC, IFIP, and IFORS, Ohio State University, Columbus, Aug. 9–13.

Symposium on the Simulation of Computer Systems, National Bureau of Standards and ACM, NBS, Boulder, Colo., Aug. 10–12.

Nordic Laser and Electro-optics Conference, Nolec '76, Chalmers University of Technology, Gothenburg, Sweden, Aug. 10–12.

20th Annual SPIE Technical Symposium and Instrument Display, Society of Photo-Optical Instrumentation Engineers, Town and Country Hotel, San Diego, Aug. 23–27.

Compcon 76 Fall, IEEE, Mayflower Hotel, Washington, D.C., Sept. 7–10.



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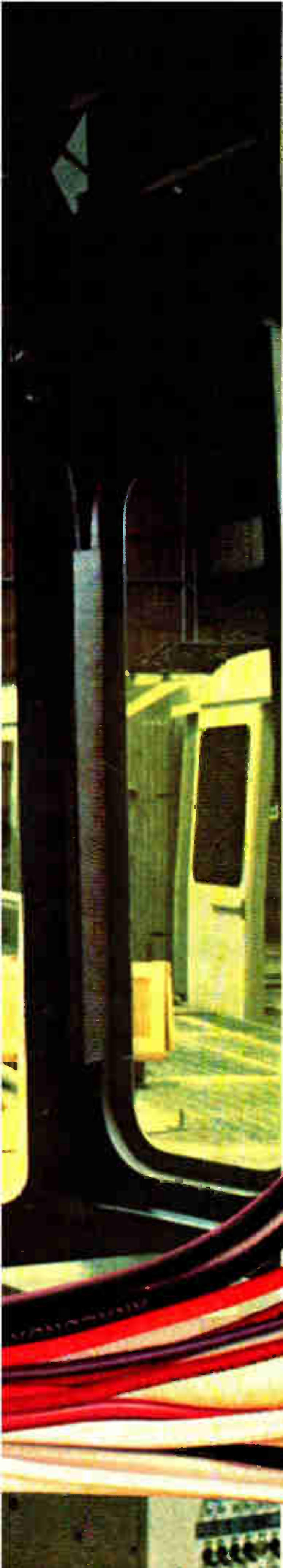

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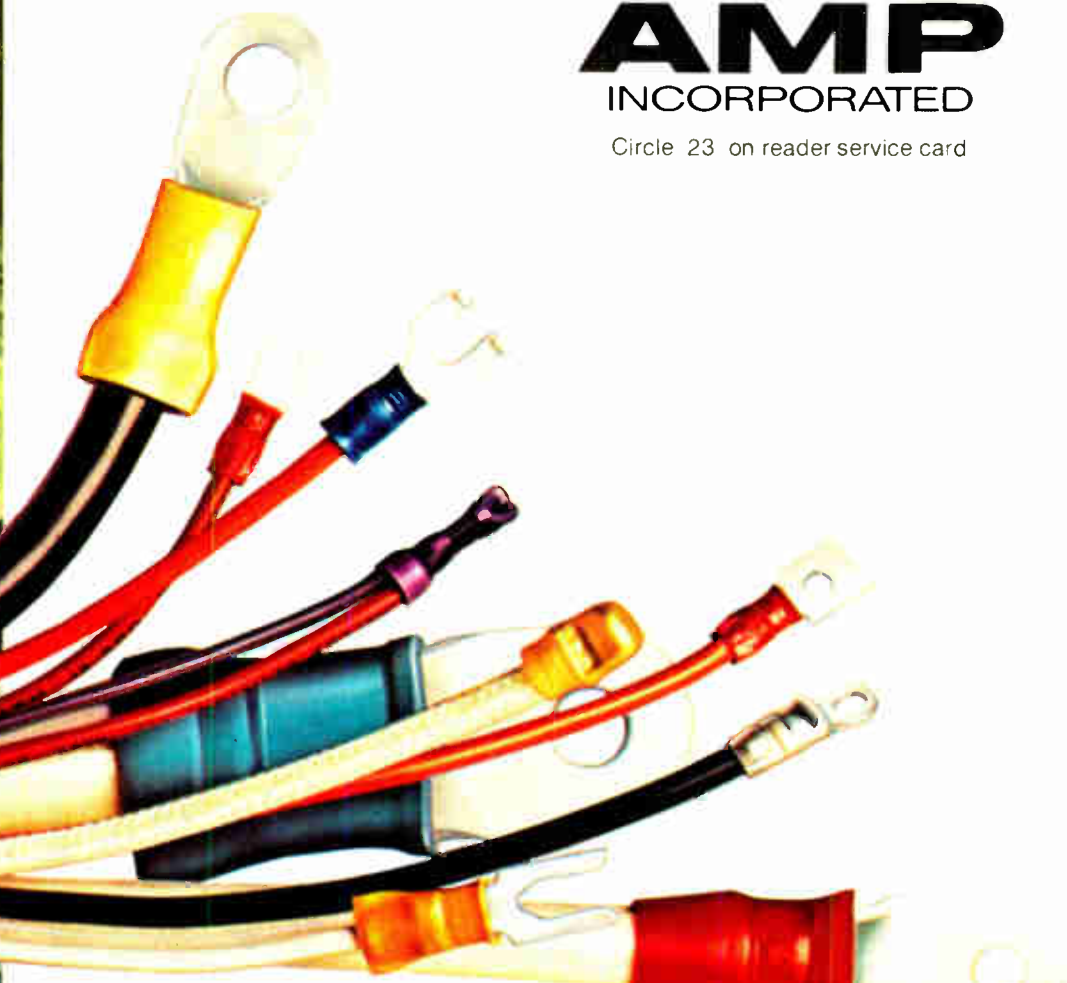

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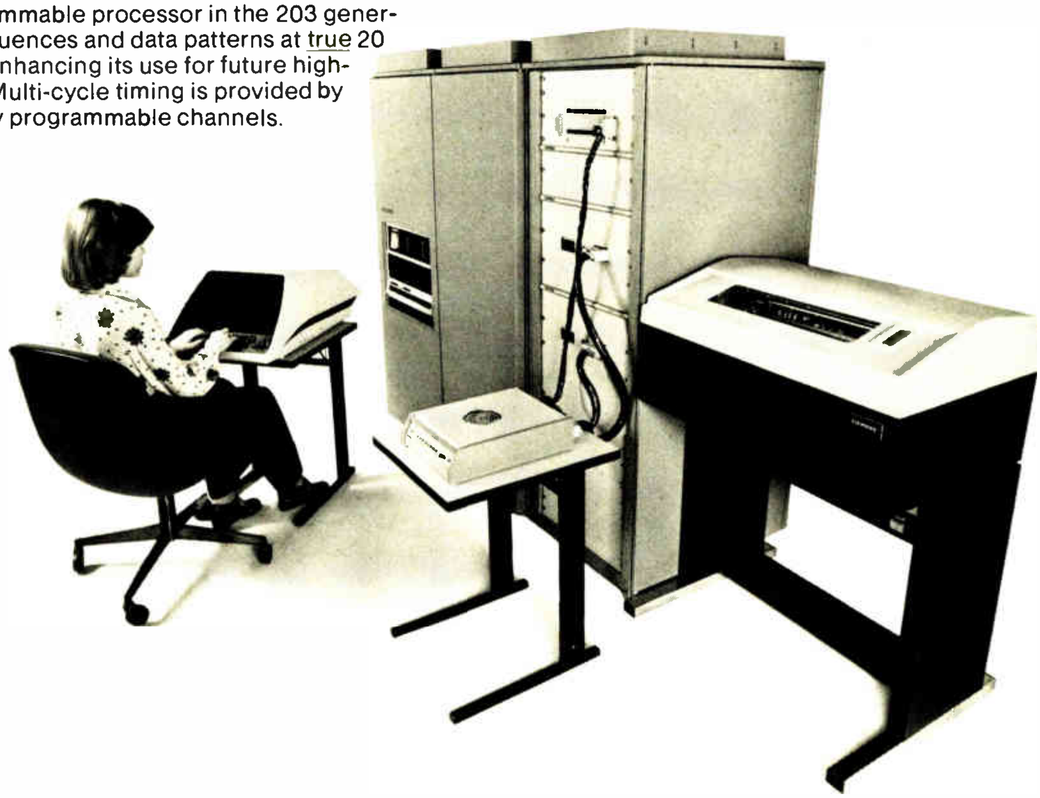


Electronics newsletter

One-chip controller to join 6800 line

What Intel did for the 8080 microprocessor family with its new 8048 controller chips, Motorola now plans to do for its 6800 with a one-chip controller. Although Motorola is not disclosing details at this time, **the 6802, which is scheduled to appear in the second quarter of next year,** will have an 8,192-by-1-bit read-only memory, 256 bits of random-access memory, and enough input and output capability on the chip to allow it to serve either as a stand-alone controller in high-volume applications or as a peripheral controller in larger 6800-based systems.

New IBM 370s double performance of 135 and 145

For its new models 138 and 148 in the System/370, IBM has almost doubled the performance of predecessors 135 and 145—but kept the same price. The new models also use the same 2-kilobit MOS memory chips as the models 158 and 168 to give each twice the total capacity available in the earlier models—the 138 can handle 1 megabyte, the 148 2 megabytes.

The new models, which will sell for $350,000 to $859,000, **appear to be taking on the steadily upward-expanding minicomputer systems,** such as the Digital Equipment Corp. DEC system 20 and the Data General Eclipse 300. However, implications for the next generation of IBM machines—the Future System, 380, or whatever it will be called—are still unclear. Speculation is that these new models actually may be members of that generation in disguise. "There may be more under the hood here than is immediately apparent," says Frederick Withington, resident IBM analyst at A.D. Little & Co.

Gillette to retail LED watches in drugstores

Competition in the already torrid electronic-watch market will heat up considerably in September when the Gillette Co. takes the wraps off 14 light-emitting-diode models **in drugstores and other retail-counter displays in 12 major U.S. markets.** The company's Appliance division in Boston is marketing the watches. Modules are supplied by Integrated Display Systems Inc., Montgomeryville, Pa. [*Electronics*, April 29, p. 36]. The watches range in price from $39.95 to $75.

National cuts cost of sample-hold chip

The high cost of linear components for data-acquisition systems gets a hammering from National Semiconductor's new sample-and-hold chip. At $3.65, **it is about a third the price of other monolithic sample and holds and about a fifth the price of hybrid and module versions.** To be supplied in three temperature versions, the LF 198, LF 298 and LF 398, the chip uses the same combination of bipolar and junction-FET technology that's found in the firm's latest operational amplifiers.

Specifications are comparable with those of more expensive circuits built with dielectric isolation. As a unity-gain follower, it has an acquisition time of 20 microseconds with an external hold capacitor of 0.01 microfarad, or as low as 5 μs with a 0.001-μF hold capacitor. Gain accuracy is typically 0.002%. The bipolar input stage blesses the device with an offset voltage of only 3 millivolts and input bias current of 25 nanoamperes, while the p-channel JFET output stage is responsible for its large, 150-kilohertz bandwidth and low output noise. Samples are available now, and production is scheduled to start in 8 to 10 weeks.

Electronics newsletter

Sanders puts IBM's SNA into terminal

Sanders Associates last week became the first computer-terminal manufacturer besides IBM **to demonstrate the IBM-introduced systems network architecture** (SNA) which includes synchronous data-link control, for teleprocessing networks. At the same time, the Sanders' Data Systems group, Nashua, N.H., announced that its model 8170 CRT terminal is being offered with the SNA option at a purchase price of $1,000 vs $2,030 for the SNA-equipped IBM 3270 terminal. First deliveries are expected next year. Sanders officials look for demand to quicken as SNA becomes the standard computer communications technique by 1980.

Tek outbids HP for $10 million scope contract

Tektronix Inc. in Beaverton, Ore., is in line to win a $10 million-plus contract, having underbid Hewlett-Packard Co.'s Colorado Springs division on 100-megahertz oscilloscopes meeting a new triservice specification, MIL-0-83225A. **Tek's winning bid of $1,283 for a modified model 465 scope was well below the $1,740 bid by HP,** which offered a modified model 1740.

TI to offer 65-k CCD memory

Texas Instruments' entry into the charge-coupled-memory market will be a 65-kilobit chip, the level of complexity that most observers feel **has a chance to capture some of the disk- and drum-replacement market,** as well as find auxiliary applications in the computer-memory hierarchy. The TI chip, with prototypes expected by the end of the year, has a serial-parallel-serial loop configuration in 32 2,048-bit loops.

HP continues to add to new DMM line . . .

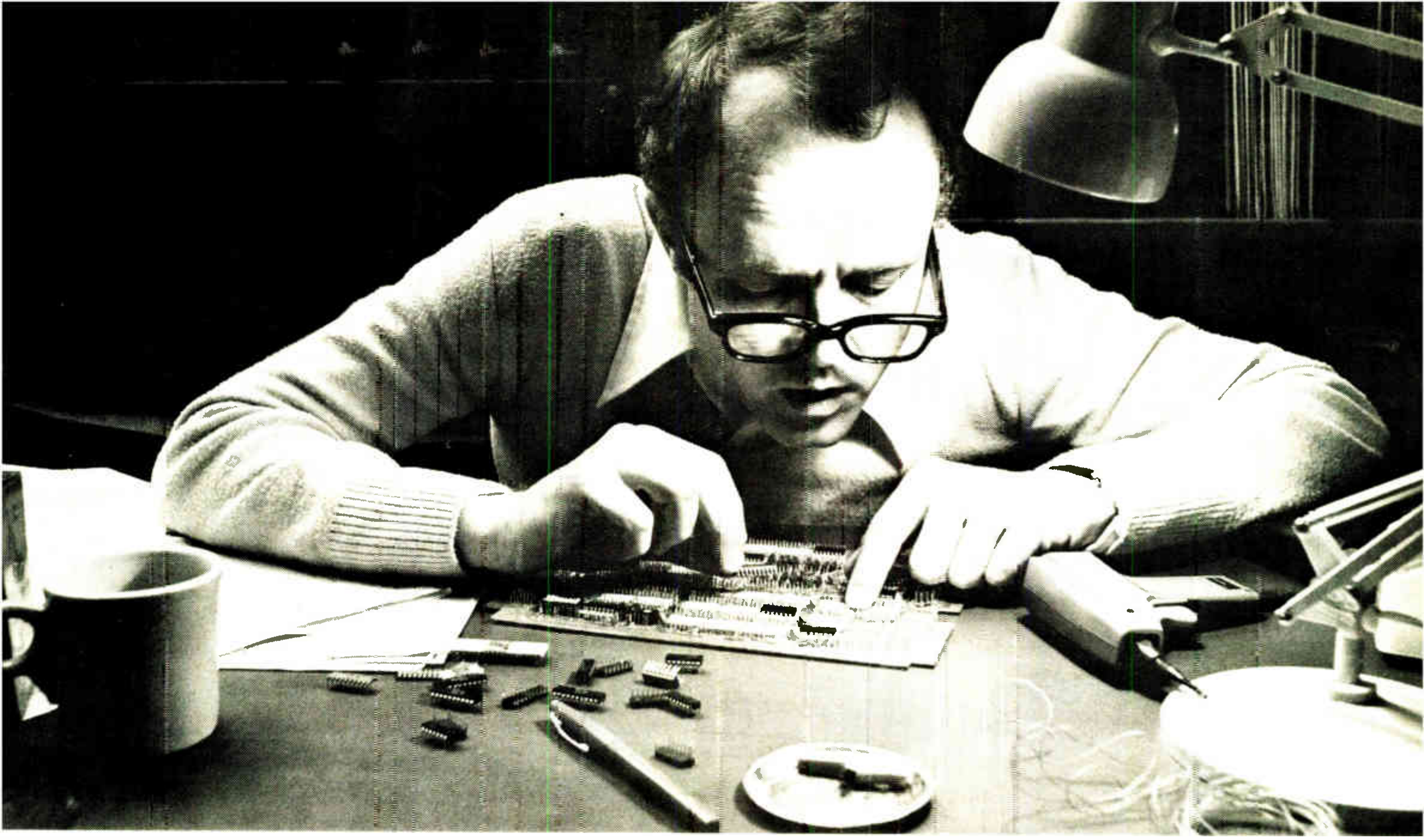
Battling to establish as strong a competitive position in digital multimeters as it enjoys in most other product lines, Hewlett-Packard Co. of Palo Alto, Calif., is offering yet another instrument—a 5½-digit unit for systems applications. Designed around an in-house-built microcontroller, the model 3455A **is the fourth new DMM from HP's Loveland Instrument division since the 4½-digit model 3465A was introduced a year ago.**

. . . as it develops an analyzer for microprocessors

At HP's other Colorado plant, the Colorado Springs division is expanding its line of digital-circuit test equipment with a microprocessor analyzer **that displays the activity on data and address buses in several notations**—binary, hexadecimal, or decoded into English. Initial versions of the model 1611A will handle circuits based on either 6800-type or 8080-type microprocessors, and users can convert the instrument from one device type to another in about 15 minutes. With a target price of $5,500, the instrument may be ready this fall.

Teradyne designs linear-IC tester with easy programing

Watch for Teradyne Inc. to introduce by the end of the year a tester for linear integrated circuits. The instrument offers the same ease of programing as the J401 TTL-IC test system, introduced at the Electro/76 show in May. Thomas B. Newman Jr., product manager for the Semiconductor Test division in Boston, says any engineer who can read a device data sheet can learn to program the J401 in only 30 minutes. **The linear-IC tester** will probably cost about the same as the J401—less than $40,000.



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Circle 29 on reader service card

Rotary switch is stamped out of metal matrix

Potentially low-cost unit has contacts and terminals in one metal piece; samples due from Oak later this year

Perhaps the most labor-intensive component in today's electronic equipment—the rotary switch—has had most of the labor designed out of it by Oak Industries.

Now in limited production, the switch is in the final phase of market research, says Dean Bach, director of product planning for the firm's Switch division in Crystal Lake, Ill. Late last month, the first parts reached a few major customers, although sampling isn't scheduled until later this year. Full cost savings won't be realized until tooling is installed, perhaps by next summer, Bach says. Then, the switch should sell for 25% to 40% less than its traditional counterpart.

"In building the traditional rotary, we must pick up each [contact] clip individually and place it on the stator," Bach says. "There's nothing we can do to make it cheaper, except by changing the material in the dielectric and the contacts."

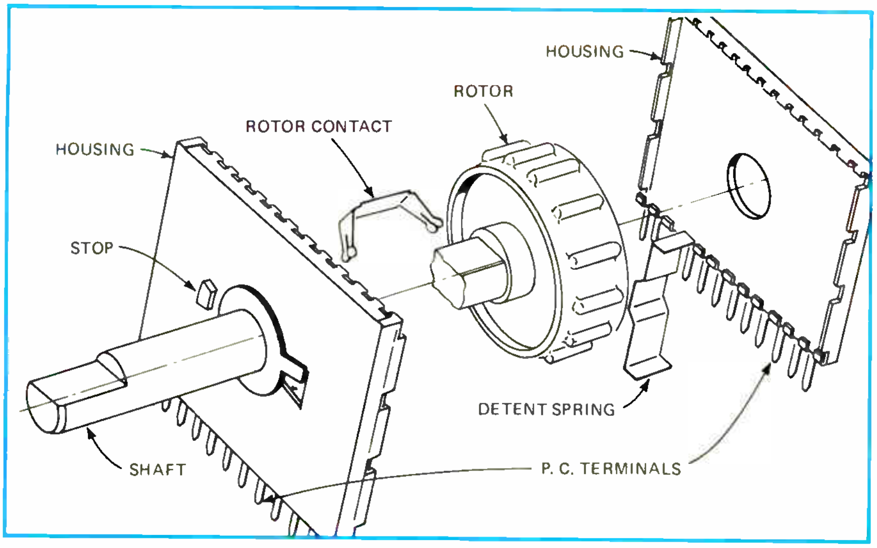
Metal stamp. In contrast, all contact surfaces, conducting paths, and terminals in Oak's new design are stamped from a single piece of metal, eliminating the need for assembling a myriad of tiny pieces by hand. "We hope to be able to pour raw material in one end and get completed, tested, switches out the other," Bach says.

Moreover, the capability for 100% electrical testing is inherent in the switch design, unlike the traditional rotary switch. "In rotaries, as we start ganging sections together, the test procedure becomes expensive," Bach says. "The whole switch is littered with clips that we have to hook wires to. So we don't electrically test unless the customer wants it and is willing to pay for it."

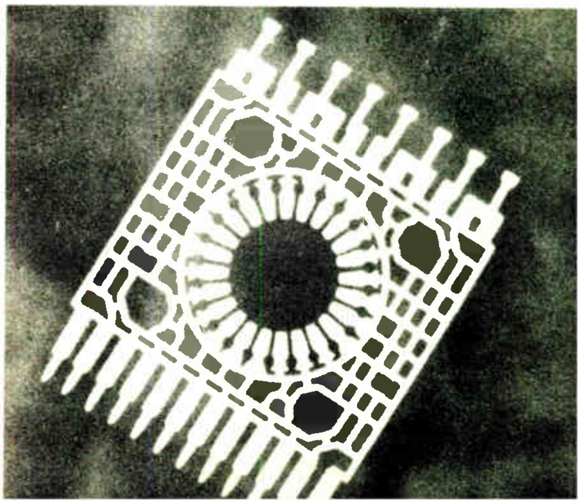
The new switch can be tested using probes or sockets as part of the production process. Even without testing, the switch is bound to be better, says Bach: since the switching pattern is die-stamped, there are no clips to be omitted or hung in the wrong place, usually the largest cause of error.

The switch consists of two metal matrix plates heat-staked to identical halves of an injection-molded plastic housing, as shown in the diagram below. "You might call them plastic printed-circuit boards," says Bernard J. Golbeck, Oak's director of engineering. "Sandwiched between them is a plastic rotor with holes that carry the switch contacts that effect the connections between the two metal plates."

The rotor, which also serves as a dust shield enclosing the switching area, has bumps molded on its periphery. These bumps bear against



New style. Metal matrix, below, contains the contacts, conducting paths and terminals for Oak Industries' rotary switch. Cut to specifications, one matrix is fastened to front housing, a second to the rear housing.

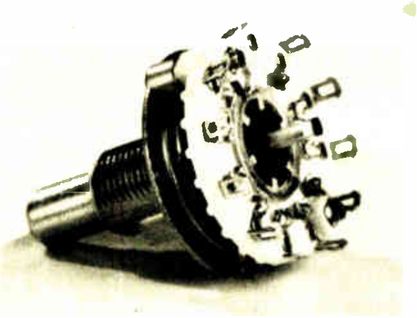


metal detent springs that are carried by the plastic housing.

"We start with strip stock and punch the holes in the matrix as it progresses through the die to get the switching characteristics we want," Golbeck says. Extra metal is punched away from the matrix to make special configurations, he says. Even shading—the making or breaking of poles in desired sequences—can be accomplished by removing part of the matrix to get wider or narrower contact surfaces. Contact rating and resistance is determined by the materials used. Golbeck expects that maximums will be around 1 ampere at 28 volts dc or 0.5 A at 110 V ac.

Switch stops are also programable. Oak starts with a fingered metal washer and bends the fingers to engage molded projections on the housing that stop the rotation.

Joined halves. The two halves of the housing can be riveted, screwed, or heat-staked together. The terminals emerge from the top or bottom edges of the finished switch and can be of pc board, wire-wrapped, solder, or quick-connect types, alone or in combination. The terminals are on 100-mil centers in two rows 300 mils apart, the same as dual in-line integrated-circuit packages. "And if all the terminals are on one side of the switch, the other side can carry an IC or seven-segment readout package," Golbeck adds.


Obsolete? Each wiring terminal in conventional rotary switch must be handled individually, adding to the unit's cost.

The first switch that Oak plans to tool will be a 2- to 12-position rotary switch with either shorting or nonshorting circuit patterns. By adding flexible, bifurcated, wiping contacts to the rotor, switch types will range from one-pole, 12-throw through six-pole, double-throw. The switch housing will measure 1.3 by 1.25 by 0.45 inches deep. Two sections can be ganged together for binary-coded-decimal outputs. □

Memory

Fairchild readies 65-k CCD chip for mass-memory marketplace

Upstaging disks and drums with semiconductor memories will be no piece of cake because the movable electromechanical types are so cheap—millicents and less per bit. But some semiconductor-memory suppliers are trying to find the range with 65-kilobit charge-coupled devices.

Currently only 9,000- and 16,384-bit CCDs are commercially available, principally from Fairchild Semiconductor and Intel Corp. But Fairchild is hoping to jump in first with the 65,536-bit size.

Says Frank Rittiman, manager of metal-oxide-semiconductor products, "We'll begin fabrication of our first 65-k CCDs in September and make samples available for evaluation by selected customers in October." Texas Instruments also has a 65-k CCD in development (see page 28).

SPS format. Fairchild's new memory, designated the CCD 465, is configured in a serial-parallel-serial, or SPS, fashion, unlike the line-addressable (or Laram) format of its 16-k CCD 450 or the serpentine or synchronous structure of its 9-k CCD. "We picked that structure," says Rittiman, "because it offers the best performance combination for serial mass memory, and that's where we're aiming this device. It has got to be cheap, so we've traded off some speed for high packaging density and low power."

The 4,096-by-1-by-16-bit SPS memory consists of a single horizontal register of 64 bits, to which several vertical registers connect. Data enters the horizontal register and, after filling it, transfers in parallel to the vertical elements. After shifting through the vertical registers, the data recombines in a second 64-bit-wide horizontal unit. Internally, the register is organized into 16 blocks in which the bits are advanced simultaneously.

As for speed, switching time between blocks is about 50 to 100 nanoseconds, while access to a single bit on the average is 500 microseconds, at a clock rate of 4 megahertz, with the worst case being 1 millisecond. "That may appear slow compared to random-access memories," says Rittiman, "but it is in fact comparable to most of today's disks and drums."

Fairchild is keeping the costs low on its new device by fitting the 65,000 bits of memory, plus peripheral circuitry, on a chip only 33,000 square mils in size. Moreover, in the read/write or read/modify/write modes, the four-phase four-power-supply device consumes only 400 milliwatts at 4 MHz. In the power-down mode, this drops to 70 mW at 1 MHz, while in the high-speed search mode it consumes 300 mW at 4 MHz.

How this SPS 65-k CCD memory differs from Fairchild's synchronous and line-addressable CCDs is explained by Bruce Threewitt, MOS applications manager. In synchronous devices all bits shift at the same frequency, in a serpentine fashion from input to output. In a line-addressable CCD, a MOS selection matrix is connected to sequential CCD shift registers, so that the matrix may read, write, or refresh information in any chosen register. However, in the serial-parallel-serial CCD, data fills a horizontal register and then shifts in parallel through vertical registers at a slower rate.

"Obviously, each kind of configuration has a particular optimum application," points out Threewitt. "For example, the Laram's low clock capacitance and fast access time make it a prime candidate for fast-access auxiliary memories. The serpentine structure, on the other hand, can operate over a wide range of the frequencies suited to data-buffering applications." □

Military

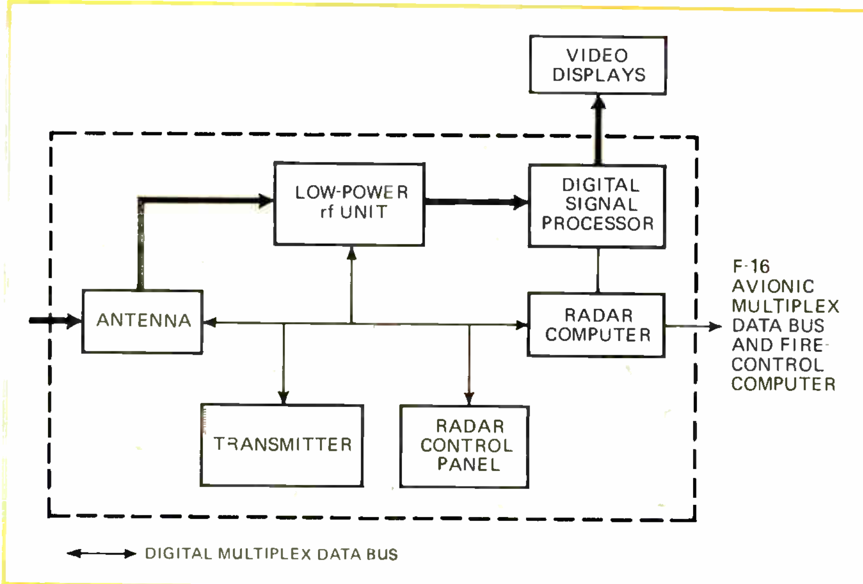
Westinghouse starts on F-16 radars

Balancing design-to-cost approaches with modern digital technology, Westinghouse Defense and Electronic Systems Center, Baltimore, has begun full-scale development of the radar for the F-16 air combat fighter.

Under a $36 million subcontract from the Air Force's prime contractor, General Dynamics Corp., Fort Worth, Texas, Westinghouse will begin delivery in December of 12 radars for flight test and evaluation. Initial orders for the plane are expected to run close to 1,000, including 650 for the Air Force and another 348 for four NATO countries that will be produced in part in Europe [*Electronics*, June 10, p.45].

The new radar, designed for a one-man crew in both air-to-air and air-to-surface weapons-delivery roles, is touted by Westinghouse as one more successful application of lessons learned from the in-house development of its WX series of digital airborne radars. The company credits its WX design-to-cost program as the basis for its other major airborne radar effort, the Electronically Agile Radar intended for the Air Force bomber fleet [*Electronics*, May 27, p. 40]. Price tag for production models of the 260-lb, F-16 radar is $250,000, the firm says.

Savings. Typical of the design-to-cost approach is the use of software-controlled processing to eliminate the usual need for a radar receiver guard channel and associated circuitry. "Digital clutter rejection and other digital postprocessing techniques subtract ground discretes and area returns from the sidelobes, eliminating the potential source of false alarms without a guard channel," a Westinghouse official explains. "This results in a major cost reduction, less complexity, lower weight, plus increased reliability."



Replaceables. Five of the six line-replaceable units in the Westinghouse F-16 radar are interconnected by a digital multiplex bus. The sixth, the digital-signal processor, is connected to the radar computer by a separate high-speed data bus.

Westinghouse also expects its built-in test circuitry to eliminate the need for flight-line test equipment, thereby reducing the system's support costs. Basic performance parameters of the radar are monitored continuously by its control computer through a digital bus, shown in the diagram above. Each line-replaceable unit (LRU) is tested automatically, assuring the pilot "with a confidence level of 95% that no malfunctions exist," according to the developers. When a malfunction is detected, the built-in test routine isolates 95% of the failures to a particular LRU. Goal for the production radar is a mean time between failure of at least 100 hours.

Six modules. In deriving the F-16 radar from its WX-200 radar series, Westinghouse settled on six line-replaceable modules consisting of the antenna, transmitters, low-power rf unit, digital signal processor, radar computer, and radar control panel.

A planar-array antenna, mechanically gimballed in two axes, was chosen for its good gain and low sidelobes in all scan angles, which provide an air-to-air search area of ±60° in both azimuth and elevation, as well as three air-to-surface operating modes—beam mapping, Doppler beam sharpening to improve map resolution, and as a navigation beacon.

The low-power rf unit contains a receiver protector, low-noise parametric amplifier, receiver, analog-to-digital converters, stable local oscillator, and the system clock generator. All analog processing of the radar return signal occurs here. Westinghouse expects to cut costs, weight, and the number of interconnections in this module by using microwave integrated circuits on microstrip to fabricate the first mixer and the first intermediate-frequency stage of the receiver.

The transmitter LRU contains an air-cooled traveling-wave tube (TWT), a solid-state grid pulser, high-voltage power supplies, regulators, and protection and control circuit. Except for a final TWT output tube, the entire transmitter is solid-state.

Clutter rejection and other radar signal processing is performed by the digital signal processor with standard integrated circuits. Large-scale-integrated devices are used when commercially available. Custom LSI devices were avoided for cost and availability reasons.

The radar computer configures the radar system for the various operating modes, directs the digital signal processor to add symbols to the video output, makes calculations and routes data to the fire control computer, handles interfaces with other F-16 avionic systems and other LRUs in the radar, and controls the self-test functions. □

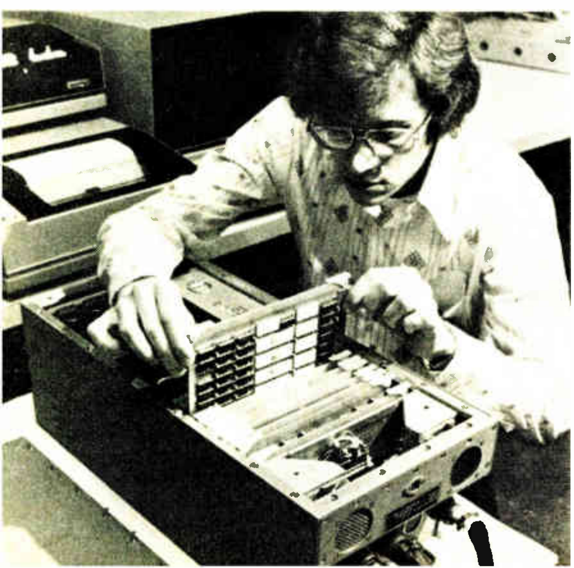
DAIS gets first of test-bed computers

Working on another avionics project for the Air Force, Westinghouse is delivering the first contractor hardware for the Digital Avionics Information System, which will eventually put digital cockpit controls in fighter aircraft, has arrived at the Air Force Avionics Laboratory.

Westinghouse Electric Corp., Baltimore, one of four DAIS contractors, has delivered the first four of the 14 high-speed computers that the Air Force will use in what it calls a "hot-bench" configuration—actually a test bed for various digital avionics equipment for future aircraft [*Electronics*, Feb. 6, 1975, p. 76].

Under the $1.2 million contract, the Westinghouse computers will operate with 16-bit words at speeds of 375,000 operations per second as well as handling 32-bit, 8-bit, or single-bit increments. The DAIS processor and its read-only memory use off-the-shelf, large-scale integrated circuits. The capacity of the core memory is 64,000 16-bit words.

Ready. Worker at Westinghouse Electric Co. inserts an LSI-memory card in one of the high-speed computers to be used in the Air Force Digital Avionics Information System.



Multiprogram. The DAIS processor derives from the Westinghouse EP—for extended performance—Millicomputer family, a class of machines from which the firm's Defense and Electronic Systems Center is getting much mileage.

A derivative machine using all-semiconductor memory for speeds up to 950,000 operations per second is the processor being developed for another Avionics Laboratory program, the Electronically Agile Radar [*Electronics*, May 27, p. 40]. Other variations serve shipboard and airborne fire control in the Navy's Harpoon and Condor missiles, the Defense Meteorological Satellite and Helios satellite programs, as well as the F-16 search, track and navigation radar, the AN/AWG-10A missile-control system for the Phantom F-4J, and the AN/ALQ-131 countermeasures pod.

The DAIS program recently completed the selection of its last major contractor with the $2 million award to Hughes Aircraft Co., Culver City, Calif., for delivery of two sets of cockpit controls and displays during a 26-month period [*Electronics*, May 27, p. 44]. Earlier awards have been made to IBM Corp., Huntsville, Ala., for developmental and service test models of a multiplex subsystem, and to Intermetrics Inc., Cambridge, Mass., for mission software. □

Trade

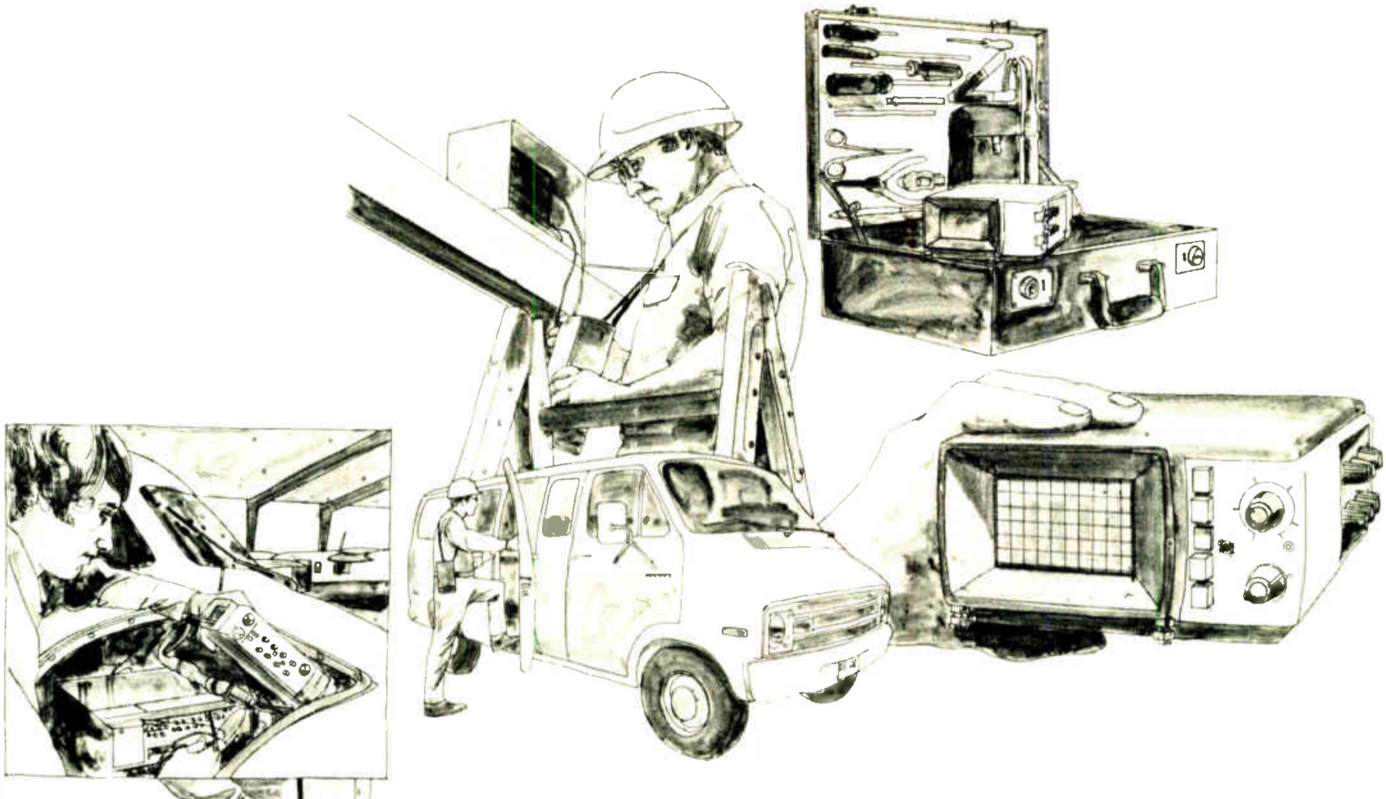
Industries say no to DOD export OK

Six high-technology trade associations have warned Congress against permitting the Department of Defense to control U.S. commercial export policy for their industries. "In a civilian government such as ours, the control and administration must reside apart from the military," said Peter F. McCloskey, president of the Computer and Business Equipment Manufacturers' Association. He is urging rejection of the recommendation by the Defense Science Board task force on technology transfer that DOD, rather than the Commerce Department, set policies for controlling export of technology. The task force was chaired by J. Fred Bucy, chairman and chief executive of Texas Instruments [*Electronics*, April 15, p. 38].

In issuing his warning before the House Committee on International Relations last month, McCloskey was acting as spokesman for the Joint High Technology Industries Group, an informal organization set up to present a coordinated response to changes being considered by Congress in the Export Administration Act of 1969. Without congressional action, the law will expire Sept. 30. The *ad hoc* group consists of the CBEMA, the Electronic Industries Association, Wema, and associations representing manufacturers in aerospace, general aviation, and machine tools.

Six changes. Beyond urging easing of the proposed Pentagon control of high-technology exports, the industry associations were united in recommending that any new export rules adopted by the House include "with some additions and clarifications" the six sections of S. 3084's Title I, already approved by the Senate Banking Committee. These sections in the Senate bill, designed to accelerate Government action on export applications, would:

- Permit applicants to review documentation before the Commerce Department forwarded it for approval to the Coordinating Committee (Cocom), made up of the NATO nations and Japan. This review would make certain the documents accurately described the technology or goods for which a license was being sought.
- Change the criteria for placing a nation on the "controlled list," so



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For Technical Data circle 34 on Reader Service Card

For Demonstration circle 35 on Reader Service Card that factors other than communist or noncommunist status would be included. Such considerations would include potential friendship with the U.S. and willingness to control transshipments of U.S. exports.

- Increase from two years to four the terms of the industry technical-advisory committees that report to Commerce and require Commerce to consult with the committees on Cocom and other issues. If Commerce were to reject their advice, the department would be required to notify the committees within a reasonable period and explain why.
- Require that Commerce explain to an exporter both the statutory and technical reasons for a license denial to ensure that technical evaluations have been correct.

Speed urged. The industry group also urged Congress to continue monitoring Commerce Department efforts to cut to 90 days the time taken to process export licenses. "Merely adding personnel will not solve the problem within an agency," it pointed out, "unless those additional personnel are trained and technically qualified."

Moreover, McCloskey says that rules against inter-industry communications among committee members, designed to preclude violations of antitrust laws, should be relaxed to achieve "a more efficient, expert, and balanced advisory role." And because technology changes so fast, McCloskey would halve to nine months the time proposed for a Commerce Department report to Congress on export controls.

In calling for these and other changes—including a complete rewrite of export regulations to make them easier to understand—McCloskey acknowledges that Congress may want to consider "a simple nine-month extension of the current Export Administration Act to June 30, 1977," as an interim measure to permit full consideration of the many proposals. □

Companies

Merger of AMS and Intersil dictated by the cost of developing technology

The proposed merger of Advanced Memory Systems Inc. of Sunnyvale, Calif. ($32 million in annual sales) and Intersil Inc. of nearby Cupertino ($25.5 million) underlines what has become increasingly evident to the semiconductor industry: it's practically impossible for small-to-medium-sized manufacturers, no matter how solid they appear, to compete with large manufacturers in high-technology mainstream products, such as microprocessors and memories.

"Large-scale-integrated-circuit technology has turned our industry upside down," says Orion L. Hoch, president of AMS and the man set to become president of the merged company, which will bear the name Intersil Inc. "The sheer complexity of the devices that must be developed mean a company has got to finance a large-scale research and development effort and maintain a high-level production facility just to stay even, much less move ahead. There's just no way a $20–30 million company can keep up with a $100–200 million-a-year company like, say, Intel, even by pouring 15% to 20% into R&D."

Size. Sheer complexity of IC technology requires bigness to compete, says Hoch.

At first blush, the proposed merger seems an ideal fit, with few overlapping product areas, at least in the memory area. AMS has a strong n-channel metal-oxide-semiconductor technology with a wide range of peripheral, mainframe, and add-on static and dynamic MOS memory products. And the firm is a second source to both of National's 18-pin 4,096-bit random-access memory devices, while Intersil supplies Motorola's 22-pin 4-k RAM.

But, as principally a supplier of add-on memories to its own system's division, and with little component capability, AMS' growth appeared to many to be extremely vulnerable. It was feeling pressure from such memory-system newcomers as Intel and National. Even worse, IBM may be getting ready to enter the add-on business.

Intersil's emphasis on component product development and marketing is a good match for AMS' MOS technology, and its high-speed bipolar and low-power complementary-MOS memories fill a very obvious gap in the AMS product spectrum. The new company will also inherit Intersil's strong position in linear ICs for the data-acquisition and instrumentation market.

Products needed. In microprocessors, however, the picture is cloudy. AMS has agreed to second-source Signetics' 2650 processor chip, but has apparently not committed itself to build peripheral microprocessor or software development products.

Likewise, Intersil's proprietary 6100 C-MOS family of PDP-8-compatible microprocessor parts appears to be aimed at rather specialized military and low-power markets. Thus, the new company still must develop a mainstream n-MOS processor family or become a second source to one if it intends to penetrate the fastest-growing segment of the market in LSI-computer-based equipment.

A still more negative note is the financial situation of Intersil, which for the fiscal year that ended Dec.

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SOC 5-6	B	5V	6.0	4.9	3.8	54
SOC 5-10	C	5V	10.0	8.0	6.5	67
SOC 12-1.6	A	12V	1.6	1.3	1.0	32
SOC 12-4.0	B	12V	4.0	3.0	2.5	54
SOC 12-6.0	C	12V	6.0	5.0	4.2	67
SOC 15-1.5	A	15V	1.5	1.2	1.0	32
SOC 15-3.0	B	15V	3.0	2.6	2.2	54
SOC 15-5.0	C	15V	5.0	4.2	3.5	67
SOC 24-1.0	A	24V	1.0	.75	.55	32
SOC 24-2.2	B	24V	2.2	1.9	1.6	54
SOC 24-3.5	C	24V	3.5	2.9	2.4	67
SOC 28-0.8	A	28V	0.8	.64	.45	32
SOC 28-2.0	B	28V	2.0	1.7	1.4	54
SOC 28-3.1	C	28V	3.1	2.6	2.0	67

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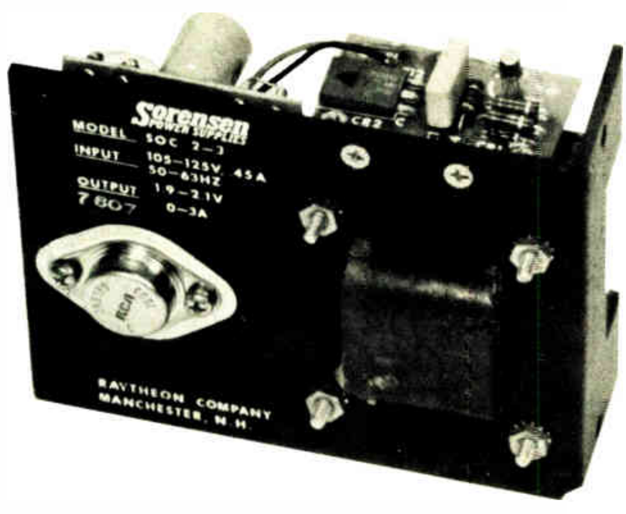

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31, 1975, had a loss of $2.5 million.

Hoch expects that if the current quarterly rates remain roughly the same for both companies (in the first quarter, $18 million for AMS and $7 million for Intersil), the merged Intersil could come close to the magic $100 million by the end of 1976. And if that occurs, says industry observers, look for some more companies to consider similar "marriages of convenience." □

Stein to attack yields at Motorola Semi

When Alfred J. Stein takes over Motorola's Integrated Circuit division next week, his top priority is a basic one: improving wafer yields.

"That certainly is a major reason for selecting Al," confirms John R. Welty, vice president and group executive of the company's Semiconductor Group. Stein, who was named vice president and general manager on June 25 after a widely publicized search, joins Motorola Semiconductor Products in Phoenix after 18 years with Texas Instruments.

Motorola's IC operations have had continuing silicon-processing problems, Welty says, particularly in metal-oxide-semiconductor production at the Austin, Texas, facility opened less than a year ago.

Not solved. At a financial analysts' meeting Oct. 31 of last year, Welty first reported yield problems [*Electronics*, Nov. 13, p. 96]. Other officials since then have said these were solved. But industry reports have held otherwise.

At TI, Stein earned a reputation as that company's top hand for starting new plants and straightening out troubled ones. His most acclaimed feat probably was the development from 1968 to 1971 of TI's bipolar operation in Houston, from initial plant layout to construction.

Earlier, Stein had established a TI facility to build solid-state logic circuits for IBM and started European IC production for the Texas company in Bedford, England. His most recent TI post was general manager of all North American discrete-component operations.

While IC division personnel are said to be showing the usual apprehension in awaiting a new boss, Welty believes Stein will be "well received by the troops"—in addition to his record in plant startup and "achieving exceptional yields, he is a manager who has developed highly motivated organizations."

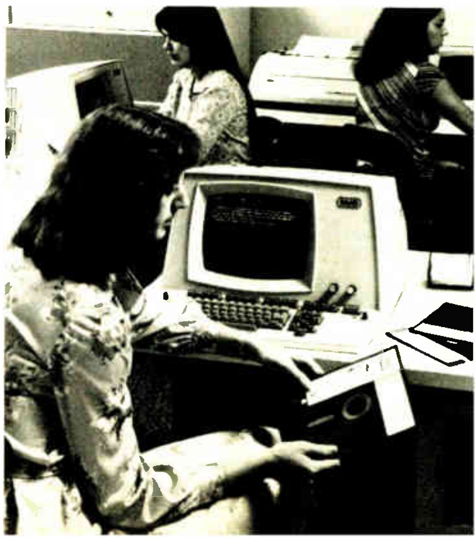
Having a full-time manager is itself expected to help the morale of the division, which was split off from the Discrete Components division in October. Robert R. Heikes, vice president and assistant group executive, has been the acting general manager. □

Commercial

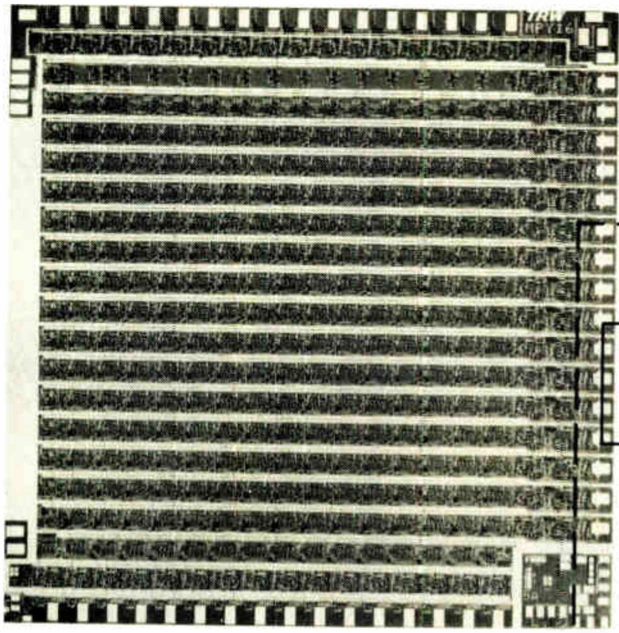
CRT terminals hit word processing

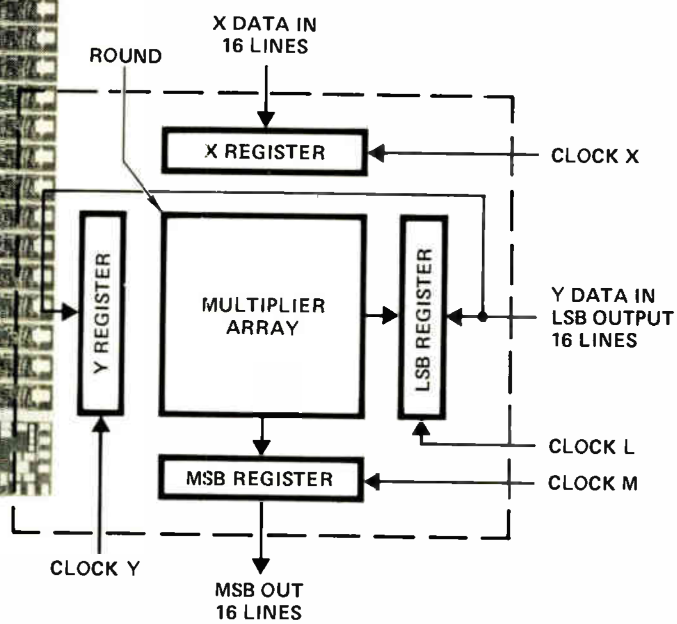
Word-processing—automation of the office—is getting a raft of new text-preparation and editing systems built around cathode-ray-tube displays. The new combinations of electronic displays and keyboards are also leading the various competitors to hope for a larger share of the word-processing business, now 83% dominated by IBM Corp.'s Office Products division. Reason: IBM

Word handler. Cathode-ray-tube display enables the operator to see the editing process being carried out in this $12,000 Word Processor 10 with its floppy-disk store and printer from Wang Laboratories.



16-Bit Multiplier 200 Nanoseconds





The first monolithic-bipolar, 16 x 16-bit multiplier (MPY-16) is now available from TRW. It's fully TTL-compatible, too. A single MPY-16 package can replace as many as 50 MSI/TTL packages, eliminating 2 x 4 multipliers.

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All input and output data – internally latched...three I/O ports (16 bits/port) for highest throughput speed – 200 ns typical...single port operation at reduced speed – 300 ns with separate clock controls. Full adder cells on the 16 by 16-bit multiplier array use the sequential add algorithm. A round control is available.

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TRW ELECTRONIC SYSTEMS DIVISION

has not seen fit to announce its own CRT display system as expected.

Although more expensive than the automatic typewriters, the CRT machines offer greater versatility—they're easier to edit with, for example, because each page shows up on the display screen. At least, that was the pitch of exhibitors at the recent International Word Processing Conference in New York, as more than a dozen companies sought to expand the CRT word-processing market. It's estimated that about 12,000 to 15,000 of these terminals will be installed this year compared

News briefs

Israeli firm building respiratory instrument

Elscint Inc. of Hackensack, N.J., the U.S. manufacturing and marketing subsidiary of Israeli-based medical instrument producer Elscint Ltd., is building a new electrooptical instrument for predicting whether or not a newborn infant will suffer from Respiratory Distress Syndrome (RDS). This condition may kill upwards of 16,000 infants in the U.S. and a few hundred thousand worldwide this year. The $12,000 fetal-lung-maturity analyzer is actually a bench-top polarization fluorimeter that uses sensitive electro-optics to measure the relative concentrations of elements in fetal fluids. Moshe Ben-Porath, general manager of the U.S. firm, says the instrument uses "a cheap calculator chip" to determine the ratio of absorption to emission of light in a fluid sample and then digitally display the results. Ben-Porath says he expects his firm to sell several hundred of the instruments next year and eventually reach a peak of about 1,000 units per year.

ICL sets availability of field-upgrade kits

International Computers Ltd., the British manufacturer competing in the U.S. computer market, has targeted next January for initial deliveries of field-upgrade kits that will enable users of its earlier 2903 computer to enhance the system's performance capabilities to that of ICL's new 2904. This is designed to compete with IBM System/370 models 115 and 125, as well as Sperry/Univac's 9030. The 2904 offers a 50% increase in the speed of instruction execution over the 2903, a memory range—32 kilowords to 96 kilowords of 24 bits each—that is twice that of the 2903, new software, and a greater selection of design configurations and peripherals. The cost of the field-upgrade kit and associated peripherals will be about the difference between the typical purchase price of the 2903 ($150,000) and the 2904 ($300,000), says Eli Hiller, acting president of ICL (U.S.A.) in New York.

Optel cuts staff drastically

Optel Corp., the Princeton, N.J., manufacturer of liquid-crystal displays and watch products, has dropped its employment level from 460 to 125 in the wake of its filing for protection from creditors under Chapter XI of the Federal bankruptcy laws. The firm was reported $1.2 million in the red in the first quarter of 1976, following a $4 million loss last year. However, president Gerald Heller says the firm's R&D program, which through the years has never been translated into profits, will continue uncut. This includes R&D for liquid-crystal and electrochromic displays, with a major effort centering around chromatic liquid crystals using a new dye process to remove the angle sensitivity of the traditional displays.

NBS sets July 19-20 for pacemaker workshop

The National Bureau of Standards has responded to the request of cardiac pacemaker manufacturers troubled by issues of product reliability and scheduled a two-day workshop on the subject. The July 19–20 meeting at NBS headquarters, Gaithersburg, Md., is titled "Reliability technology for cardiac pacemakers." Separate sessions will include discussion of parts reliability, leak rate and moisture measurements, batteries, and leads. NBS says queries should be directed to workshop coordinator Elaine C. Cohen at (301) 921-3625.

Need a simple tachometer system?

For indication only... the 300 Series system.

The 300 Series tachometer has earned a reputation for accuracy unsurpassed by any other analog tachometer. Whether you want to measure how fast, or how many, a 300 Series tach combined with an Airpax magnetic pickup, gear and meter gives you the perfect solution. The price? $251.65.

For indication and industrial signal output... the 300 Series system.

The 300 Series tachometer can also be set up to provide industrial signal output, such as 4-20mA. Because of its rugged design, you can use it in almost any industrial environment. The price? $286.65.

For indication and switching... the 300 Series system.

Need under-speed/overspeed protection? The 300 Series switching tachometer will sound the alarm whenever the speed strays beyond your preset limits. With Airpax magnetic pickup, gear and meter your system is complete. The price? $286.65.

You can order your Airpax 300 Series tachometer to handle whatever functions you require. That's versatility. You can even specify your tach with a wide variety of enclosures. But no matter what your needs are, no one gives you more tachometer for the money.

For more information, circle our number on the reader service card, or give us a call if you're in a hurry. We're standing by ready to assist you.

g3

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Circuit Breakers and Glass Seals, Cambridge Division, Cambridge, Md.
Broadcast T.V. Equipment, American Data Corp., Huntsville, Ala.

to 110,000 electromechanical text-editing machines. But the trend is definitely toward the CRTs at prices ranging from about $12,000 for a stand-alone terminal and typewriter-style printer to around $30,000 to $45,000 for a terminal, multiple printers, and communications options. A full-fledged system for a big company installation could cost $75,000 or more.

In the CRT lineup, there are conflicts, however. For one, the programing and storage of data generated for and by the typist at the CRT keyboard can be handled either by floppy disks—one or two to a unit—or by magnetic-tape cassettes. For another, the processing-control chores can be done by either a set of microprocessors or a minicomputer/shared-logic arrangement, depending on how much performance capacity the user wants.

Competitors. The companies now going into this market include:

- Wang Laboratories, Tewksbury, Mass., which has just announced a three-part CRT family, the Word Processor 10, 20, and 30, each built around a network of three Intel 8080 microprocessors. The memory is a floppy disk.
- Lexitron Corp., Chatsworth, Calif., which has announced a proprietary fast-access cassette tape-drive that has close to the highest speeds for accessing pages with a floppy disk and can store 125 pages. The Tape II drive transfers almost six 8,000-character pages at 580 kilobits per second. The firm's new Model 921 Videotype Text Processor uses four 8080 microprocessors.
- Vydec Inc., Florham Park, N.J., which has CRT models that use floppy disks. These systems do not have microprocessors, although the separate communications option employs an 8008 processor. Strongly committed to the disk, Vydec is presently investigating use of the "flippy," or two-sided floppy disk.
- Daconics, Sunnyvale, Calif., subsidiary of Xerox, which uses a completely different display in its shared-logic Visual Type system—a gas-plasma, flat-screen display with panels supplied by Owens Illinois and Burroughs. The characters are red/orange, and the display package is much slimmer than the cathode-ray tube. Daconics is offering a large screen that displays 44 lines at a time and a smaller desktop screen for reviewing correspondence a single line at a time.
- Redactron Corp., Hauppauge, N.Y., now a Burroughs subsidiary, which has added a CRT system, Redactor II, using an 8080 for each input/output, the printer, and the display. Since it uses tape cassettes, it's compatible with the company's installed base.

What of IBM and the CRT? The Office Products division will have such a display or one like it, but is not saying when. "In the long run," comments Jack Wirts, vice president of sales, "I'm not sure how useful the CRT would be. IBM's main concentration is on the 'principal' [manager] rather than only the secretary. And I'm not sure how much more efficient and productive the CRT will make the principal." □

Medical

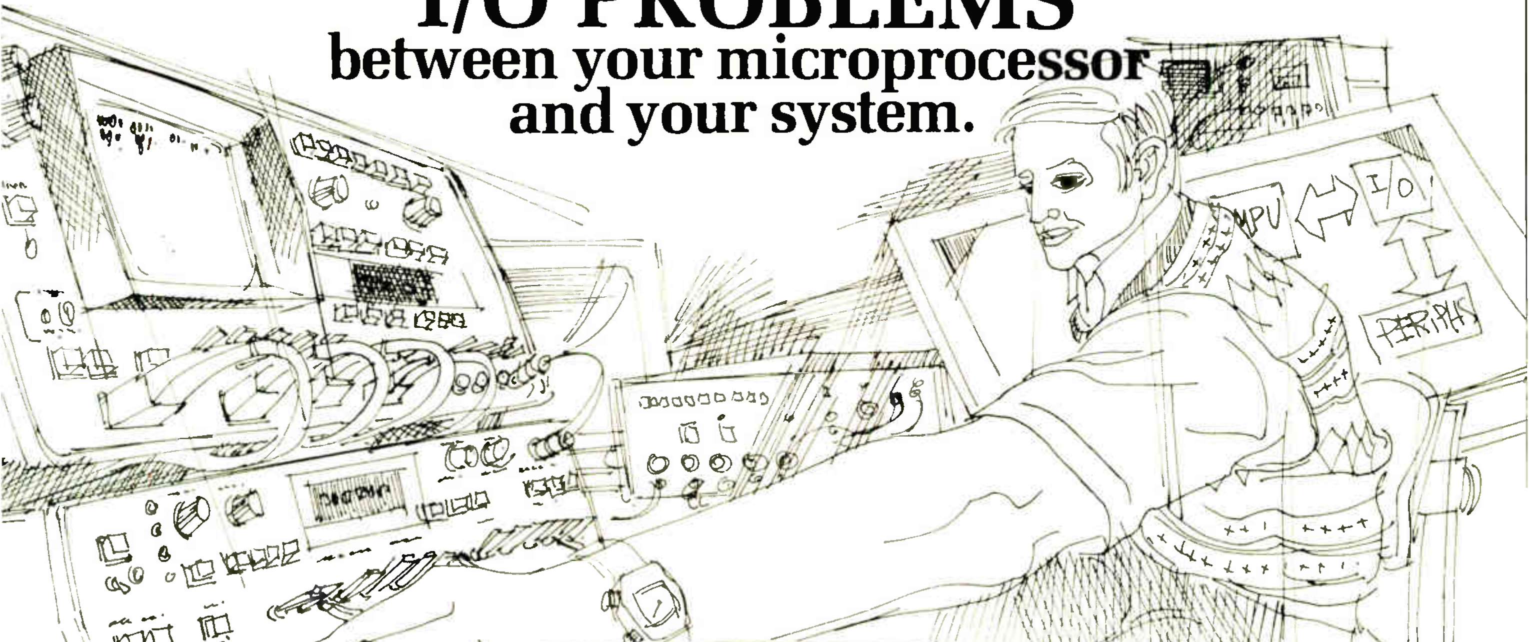
Shock waves break kidney stones

Putting its experience with high-pressure shock waves to use, the West German aerospace company Dornier System GmbH in Friedrichshafen has come up with a noninvasive method for breaking up kidney stones. In the new technique, a shock wave is directed from outside the body onto the kidney stones. When this wave hits the stones, they disintegrate to be expelled from the body naturally.

Years away. Dornier has successfully applied its method to dogs with implanted stones, but the company cautions that several years of further animal tests are still necessary before the technique can be used with humans.

A great deal of expertise has been accumulated since the early 1960s when Dornier began investigating the effects of shock waves traveling

Let's talk about solving
I/O PROBLEMS
between your microprocessor and your system.

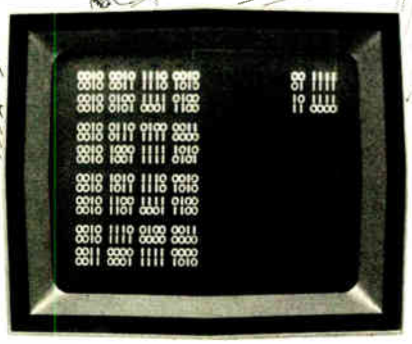


Just determining whether or not you have an I/O problem can be a major undertaking... I know, I've been there too. We call communication with the microprocessor "handshaking," but sometimes information transfer, especially across an I/O port, reminds me more of "armwrestling."

Analysis of data transfer across an I/O port can be very tricky. The microprocessor and the peripheral may have independent system clocks, or the peripheral may be asynchronous. There may be a parallel-to-serial data transformation, or vice-versa. The systems may require a common trigger to interact properly. How do you verify all that? And how do you determine that the instructions are being received and executed properly?

About the only way I know that you can really be sure everything is working right (without spending an excessive amount of time) is to look at it on an HP 1600S Logic State Analyzer. Then it doesn't matter whether you have independent system clocks going. Or whether part of the system is asynchronous.

The HP 1600S lets you display two separate tables of data on one



Microprocessor Address Bus, Data Bus and I/O input and output data are displayed simultaneously on the HP 1600S screen.

screen, so you can look at program flow right alongside the input and output states of the I/O port. That way there's no question about correct sequencing – or about data flow in either direction.

Confidence in your system design and operation will be high. I mean, when you can actually look at all those data buses, read their information flow, and see that it's all perfect – that's confidence!

What's more, if you do find a problem, the HP 1600S will help you pinpoint it more quickly than any other way I know. It can help you put an end to armwrestling within your microprocessor systems.

The HP 1600S, at $7100*, is one of the biggest timesavers you'll ever find. You should learn more about it. HP has arranged a number of seminars around the country to make that possible. Find out how you can attend the one in your area by calling your local HP field engineer. He can also supply you with complete spec sheets and application notes detailing the use of mapping for troubleshooting minicomputer and microprocessor systems. You'll discover an exciting new concept in digital troubleshooting.

*Domestic U.S.A. price only.

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Electronics review

through solid bodies in an effort to find new high-stress combinations of materials for aerospace and related applications. In the course of this work, the researchers' attention turned to determining the effects that shock waves would have on living objects.

The present project, which is being carried out in cooperation with two medical institutes in Munich, is sponsored by West Germany's Ministry for Research and Technology as part of its program for "research and technology in the service of health." The $600,000 project is scheduled to run for four years—from 1974 through 1977. It's certain, though, that it will be extended well beyond the end of next year, comments a Dornier official.

Noninvasive. Unlike other methods of disintegrating kidney stones, the Dornier treatment keeps "hands off." For example, one painful and difficult technique requires a catheter or a probe to be inserted through the urethra to the bladder or to the vicinity of the kidney, the stones then being broken up by ultrasound. But in the new method, a shock wave is focused from outside the body onto the stone, which is broken up by the pressure produced by the wave.

Shock waves, in contrast to ultrasonic waves, last for an extremely short time—around 1 microsecond—and are characterized by a pressure amplitude as high as several kilobars (or several thousand atmospheres). To disintegrate a kidney stone, a single microsecond wave is adequate.

Generation. The wave is produced by a hydrospark discharge produced in the focus of a hollow ellipsoid. The application of this therapy, of course, necessitates accurate location of the stones, either by X-ray methods or by ultrasound echoing techniques.

Dornier says the tests of the shock waves to date have caused no intolerable damage to any animal's organs. Future work will seek to consolidate present results through further animal tests and also to carry out long-term observations. □

NATIONAL ANTHEM

"ALL THE NEWS THAT FITS"

A Review of New Products and Literature from National Semiconductor • No. 3, May, 1976

UPWARD-compatible 4K, 8K, and 16K Static ROMs

Fabricated using N-channel enhancement- and depletion-mode silicon gate technology, our three-member family of static ROMs is ideally suited to a wide range of uses such as table look-up, microprogramming, random logic synthesis, control logic, etc.

The MM5238 (512 x 8), MM5242 (1024 x 8), and MM5246 (2048 x 8) are TTL/DTL-compatible and operate from a single +5 V supply. They feature a 500-ns (max.) access time, full decoding, and true static operation.

In addition, the MM5238/5242/5246 have programmable Chip Select inputs that control their Tri-State® outputs, which means that bus interfacing and memory expansion is simple indeed.

SC/MP: a Simple to use Cost-effective/Microprocessor

National's single-chip SC/MP marks the birth of a new generation of microprocessors. As the first, *low-cost* true microprocessor, SC/MP needs only one memory chip (any standard ROM, PROM, or RAM) to form a complete, fully programmable, general-purpose microprocessor system.

And this system, because of its low cost, is ideally suited to replace "sheet metal" logic in toys and games, traffic controls, home appliances, vending machines, home and building security and environment controls, on-board automotive computers, and so on.

SC/MP's features make it all happen: 8-bit data handling is combined with 16-bit addressing; an on-chip clock simplifies system design; a serial I/O port makes for easy interfacing; built-in flags and jump conditions simplify control tasks; an interrupt structure that gives fast response to asynchronous events; a delay instruction to simplify timer systems. And all of these are supported by a set of 46 control-oriented instructions.

Getting started with SC/MP is super simple. Aside from the CPU chip itself, we offer two kits. The basic kit includes all ICs, firmware, discretes, and mechanical hardware to let you explore SC/MP's capabilities. The SC/MP LCDS (Low-Cost Development System) goes further, and includes a keyboard, a display, more memory, etc.—it's a complete microcomputer, in fact, which lets you rapidly develop and debug programs, and experiment with interrupts and interface structures.

Three New 4K Static RAMs In Two Organizations, Two Lead Counts

We've got a family of ion-implanted N-channel, silicon gate, non-refresh RAMS that'll satisfy a great number of you 4K read/write users out there.

While all three family members share the same operating specs, the organizations, package pin-outs, and lead functions differ. The MM5255, for example, is organized 1024 x 4, has four common I/O ports, and is housed in an 18-pin DIP. The MM5256, also 1024 x 4, has four input pins, four output pins, and is in a 22-pin DIP. The MM5257, with its 4096 x 1 organization, has, of course, one input pin and one output pin, and is packaged in an 18-pin DIP.

All the parts are TTL compatible and operate from a single +5 V supply. These RAMS feature fast access (250 ns), a standby mode controlled by the Chip Enable (standby power is less than 200 mW typ.), low operating power (less than 400 mW typ.), and on-chip address and data registers.

You can sample the MM5255/5256/5257 next month (June), and have production quantities in the third calendar quarter of this year.

8-bit ADCs Combine Low Cost, High Performance

A new, National-proprietary ladder design is the key to the low, low price/performance ratio of our MM4357/MM5357. There simply is nothing comparable on the market at anything near the prices we've put on these monolithic ADCS—less than $8.00 each in 100-piece lots!

The MM4357, for example, is fully spec'd over the military temperature range—and there are many, far more costly ADCS around that cannot make such a claim. While the MM5357 is for commercial (0°–70°C) temperature range uses, both ADCS feature ±5 V or 0–10 V input ranges, no missing codes, high input impedance (100 MΩ, min.), ratiometric conversion, TTL compatibility, built-in output latches, and Tri-State® outputs.

Key specifications include 8-bit resolution, ±½-LSB linearity (a "B" version loosens this spec slightly), 40-μs (max.) conversion speed, and clocking rates from 5 kHz to 2 MHz. Supply voltages required are +5 V and −12 V. The MM4357/MM5357 are available in both cavity and molded 18-pin DIPS.

INTERFACE CIRCUITS IN HIGH-DISSIPATION MOLDED DIPS

National's new, high-dissipation DIPS use a copper lead frame, rather than the common Kovar lead frames. And this means increased power dissipation capabilities *with* improved reliability and increased part life.

If this sounds a bit too much like eating your cake and having it still, consider this: a circuit that in a Kovar lead frame is limited to a 625-mW dissipation in a 75°C ambient can, with a copper lead frame, dissipate 938 mW in the same ambient. Put another way, at a dissipation of 625 mW, a device in a Kovar lead frame will have a junction temperature of 150°C, while in a copper lead frame the junction temperature will drop to 125°C.

At last count, we've switched 45 interface parts to this wondrous package—dual peripheral drivers (including CMOS-compatible types), RAM interfaces, relay drivers, clock drivers, core memory drivers, etc. (See our Interface Data Book for specific thermal ratings.)

And by the way . . . If you think you can get similar high-dissipation parts from the competition, better forget it. Because there *isn't* any.

Bi-FET™ Sample/Hold:

Fast Acquisition, Ultra-High Accuracy, Low Droop Rate

The headline tells the story. National's BI-FET™ technology, which combines FET and bipolar devices on the same chip, first yielded fantastic new op amps (*National Anthem* No. 1, January 1976). Now BI-FET technology yields new sample-and-hold circuits: dc gain accuracy of 0.002% (typ.) in a unity-gain follower configuration; acquisition times as low as 6 μs to 0.01% with a 1000-pF hold capacitor; droop rates as low as 5 mV/minute with a 1-μF hold capacitor!

We're talking about our LF198/298/398, which eliminate input/output feedthrough in the hold mode even for signals equal to the supply voltages—±5 V all the way to ±18 V. In addition, these parts feature a single-pin input offset adjustment that does not degrade input offset drift; an input impedance of 10^{10} ohms, which means that high source impedances will not degrade accuracy; a bandwidth sufficient to allow stable insertion of these circuits within the feedback loop of 1-MHz op amps; and a TTL/PMOS/CMOS-compatible logic input . . . all contained in a little, 8-pin, TO-5 metal can.

PROCESSOR IS CALCULATOR-ORIENTED

Looking for a versatile, low-cost, dedicated or custom-programmable calculator or control system? We've got it! Our MM5799 contains all system timing functions, all arithmetic and logic functions, all RAM functions (384 bits), and all control ROM functions (1536 microinstructions 8-bits wide, 10-μs/microcycle) that you'll need to implement a variety of small control and microprocessor systems.

A single MOS/LSI chip, the MM5799 can scan 56 keyboard switches, or you can enter BCD data words. Its eight outputs present information in either a BCD or a seven-segment-plus-decimal-point format, and four additional latched outputs give you encoded digit-timing information. Further, a serial-in port and a serial-out port let you expand the basic RAM store and interface to peripherals.

And speaking of peripherals and extra storage, our MM5788 printer interface, DS8664 Series oscillator and decoder/drivers, MM5785 RAM interface, and MM2102 and MM74C930 1-K static RAMS are a perfect match to an MM5799-based system.

A special purpose microprocessor, our MM5799 uniquely bridges the gap between the overkill of general purpose processors and inflexible, costly, custom LSI.

Universal Timer Circuit

The MM5865 is a new timing circuit ideal for use in stop watches, kitchen and oven timers, event timers/counters, rally and navigation timers, etc. Its single chip contains all the logic required to control the timer's two 4-digit counters, to compare them, to blank leading zeros, and to cascade another MM5865.

Input-pin functions start, stop, reset, and set the counters, and determine which of the timer's seven functions is to be performed, the display resolution (0.01, 0.1, 1.0 sec., or external clock), and the divide modulo.

The MM5865's seven functions are start/stop with total elapsed time, start/stop with accumulative event time, split, sequential with total elapsed time, rally with total elapsed time, program up-count, and program down-count. The circuit uses either a 32.8-kHz crystal or an external clock, and is packaged in a 40-pin molded DIP.

High Voltage, High Slew Rate Op Amps

Unique characteristics of our LM144/344 op amps include operation from ±4 V to ±36 V, a 30-V output swing capability, a slew rate of 30 V/μs (typ.) and an externally compensated power bandwidth of 120 kHz (both at $A_V \geq 10$), a low input-bias current of 8 nA (typ.), an input offset current of only 1 nA (typ.), and a high voltage-gain of 100k (min.).

With specs such as these, the LM144/344 increase both accuracy and useful frequency range in many existing applications. The LM144, for example, is a direct replacement for the LM101A, and can replace other general purpose op amps as well.

The LM144 operates between −55° and +125°C; the LM344, intended for less severe supply voltage and temperature environments, is spec'd from 0° to +70°C. Both parts are available in a 14-pin cavity DIP, a 10-lead flat pack, and an 8-pin TO-5 can.

How to symmetrically limit the output of an op amp

A common way to symmetrically limit the output of an op amp is to use back-to-back Zeners across the feedback resistor. One of our readers, realizing that this is not the best way to do things, has asked us for a better way, and also wants to know what to expect from an op amp when symmetrical limiting is attempted by tying back-to-back Zeners from the output to ground, making use of the amp's current-limiting characteristics. Since we suspect that a great many of you are perplexed by the same problem, here are our answers.

Answering the last question first: we do not recommend clamping an op amp's output. Current limiting in an op amp is provided to protect the amp against short-circuit currents, which otherwise would destroy the amplifier. But short-circuit currents are not well defined, nor is the recovery time of the amplifier from such conditions. Further, positive and negative current-limiting may not be symmetrical. Thus, using the current-limiting characteristics to limit an output signal really is an attempt to make ill-defined internal parameters yield a well-defined external result. Not a good idea.

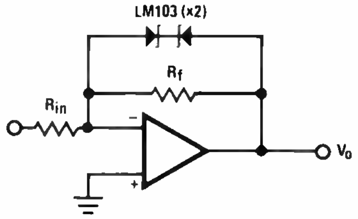

Figure 1.

In the current-limited mode the op amp's feedback loop opens, which forces the internal biases away from their nominal values. Some amps may take several milliseconds to recover, in addition to the recovery time of the external feedback component itself. If the amp is connected as an integrator, for example, the recovery time may be several minutes.

If you're still not dissuaded from clamping the amp's output, consider the radical increase in power dissipation in such a situation. This increases chip temperature, which degrades the op amp's dc parameters.

Now let's get back to back-to-back limiting. Figure 1 shows a typical circuit. It suffers from a lowered high-frequency corner (thanks to the Zener's capacitance), Zener leakage across R_f at low and medium voltages, asymmetrical limiting, and possibly even soft limiting if the Zeners have poor knees. At low voltages, use of our LM103 active Zener improves things, but only to a certain extent.

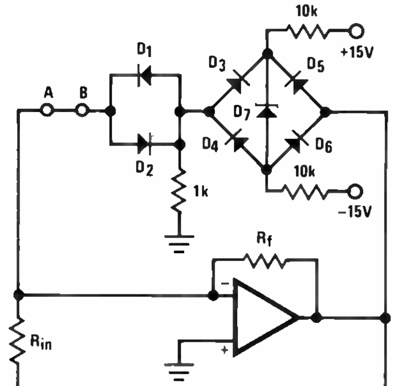

Figure 2.

Figure 2, however, improves limiting, and in fact performs quite well. Here, the diodes do not add much capacitance across the feedback resistor. And all diode leakages are absorbed by the 1-kΩ resistor. *D7* will be, typically, a 9.1-V Zener for an 11.8-V limit. At V_0 = 10 V, leakage will be less than a nanoamp; but at ±11.8 V the limiting circuitry will conduct more than 2 mA. As the same Zener conducts for both polarities of the input, output symmetry is very good.

For most applications, *D3* through *D6* can be low-capacitance, fast-recovery 1N914s. But operation at elevated temperatures may require the use of low-leakage types, such as 1N457s or FD300s. (*D7* isn't critical; it never turns off, so its capacitance and knee characteristics are unimportant.)

For super-critical low-leakage applications, add an extra stage of resistor-diode network between points *A* and *B*. For non-critical work, you can delete *D1* and *D2*.

A Review of New Products and Literature from National Semiconductor

C

NATIONAL ANTHEM

"ALL THE NEWS THAT FITS"

SC/MP HANDBOOK TELLS ALL!

Amply illustrated, the 65-page *SC/MP Technical Description* matches SC/MP's applications-oriented design in that the text stresses applications and how-to-use information.

Opening with a discussion of SC/MP's general features and support components, the *SC/MP Technical Description* proceeds to a detailed description of the CPU chip, and from there to SC/MP's application cards. SC/MP's Development Systems are also described. Based on SC/MP's CPU, the Development Systems are powerful tools for the prototyping and use of SC/MP-based control systems.

To order a copy of the *SC/MP Technical Description*, send a check for $3.00 (California residents add 6% sales tax) payable to National Semiconductor. Direct your order to Marketing Services/520.

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LARGEST-DISPLAY CLOCK MODULES NOW AVAILABLE

The outstanding feature of our new MA1010 electronic clock module is its stand-out display: a 0.84-inch, 4-digit, LED display with mitred corners, which shows hours and minutes; a blinking colon indicates seconds. There's nothing else as large, as readable, or as attractive on the market. We repeat: *nothing*. You've just got to see this one to believe it.

The module is complete on a single, 1.75 x 3.75-inch PC board, and all connections are at the bottom of the card. You add only a power transformer and switches to complete a pre-tested digital clock ideal for clock radios, desk and wall clocks, alarm clocks, TV/stereo clocks, instrument panel clocks, etc.

Timekeeping may be from 50 or 60 Hz, and you may choose a 12-hour or 24-hour format. Features include alarm ON, PM, and power failure indicators, an alarm output that drives an 8-Ω speaker, sleep and snooze timers, fast and slow set controls, and a display brightness-control output (you determine the method of control appropriate to your design). Direct (non-mux'd) LED drive eliminates RFI. Use of the module allows a low-cost, extremely compact clock design.

Prototyping quantities of the MA1010 module are already available, and volume production quantities will be available in June.

Support for AT&T rises in Congress; CWA joins fight . . .

The pace of activity continues to intensify around the Congress on the Consumer Communications Reform bill, the telephone industry's move to eliminate competition for the established carriers [*Electronics*, June 24, p. 65]. **Support in the House has increased nearly 20% in two weeks, and now numbers 150 representatives,** with nearly 90 of them Democrats. In the Senate, Howard Baker (R., Tenn.), a ranking minority member of the Commerce Committee, which will have hearings on the bill next year, wants creation of either "a national commission to supply the missing analysis" of issues in the bill this year or "a study which would employ an independent contractor to report to the committee."

Lobbying on the legislation also is increasing. The 475,000-member Communications Workers of America, a union representing telephone workers, has voted to support the bill and called for a congressional letter-writing campaign. CWA president Glenn E. Watts says he expects added support from the union's parent, AFL-CIO. But the Computer and Business Equipment Manufacturers Association opposed the bill in a letter to all members of Congress, calling for continuation of the present national telecommunications policy. Association president Peter McCloskey wrote all members in late June that the nation must have "a uniform national policy which will permit the least costly manufacture, distribution, installation, and use of computerized equipment in all of the states. The Bell bills are specifically designed to frustrate" that policy.

. . . as lobbyist says companies "can't lose"

While final enactment of the AT&T-sponsored legislation is not expected for at least another year, the telephone companies eventually "are going to win," according to a leading telecommunications industry analyst. Directors of the Computer Industry Association were told at their June meeting by Drexel, Burnham & Co.'s Harry Edelson that an AT&T lobbyist advised him that **"they can't lose even if the bill loses."** Edelson explained that "if it doesn't go through, consumer communications costs will go up by $7.50 [per month] per household by 1985. So, if the bill loses, AT&T can then increase consumer rates and say, 'Well, we tried our best. We tried to get this bill through to protect you from this.'"

Cost analysis slips Arinc selection of PLIN contractor

Aeronautical Radio Inc. has slipped until the end of summer its selection of a contractor to improve and expand its private-line intercity network, known as PLIN, which the company operates for the nation's air carriers. The planned June decision was put off, Arinc says, **to permit more time to analyze the widely varying price proposals** from the four bidding teams headed by American Telephone & Telegraph Co., Computer Sciences Corp., RCA American Communications, and Rockwell International's Collins Radio. Technical evaluations have been completed.

U.S. sales peaked at $36.4 billion in 1975, EIA says

Total 1975 U.S. electronics sales reached $36.4 billion, 1.5% higher than in 1974. Gains in communications, industrial, and government products **offset declines in consumer products and selected passive and active components,** including replacements. The record volume reported by the Electronic Industries Association put the communications and industrial market at $18.7 billion, up 5.5% from 1974, while government purchases rose 9.4% to $12.1 billion. Consumer-product sales of $4.8 billion were off 21.5% from the 1974 level, while selected new components decreased 23.1% to $3.5 billion. Component replacement sales of $791 million were off 17.6%.

Biological effects of EMR needs more study, office says

Federal research to determine what biological effects electromagnetic radiation from telecommunications will have on man and his environment **needs additional funds in order to reach conclusive results.** That is the judgment of the White House Office of Telecommunications Policy in its fourth annual report to Congress on "Control of Electromagnetic Pollution of the Environment."

Although existing programs are progressing in several agencies, OTP's acting director, John Eger, says no conclusive results on biological effects of EMR have been reached. "Recent public speculation on the hazards of EMR can and must be verified or denied only on the basis of systematic scientific analysis," Eger asserts. "Not to have sound information is only to invite controversial debate," he said, "and perhaps raise serious threats to our efficient use of the spectrum."

Datran broke, still searching for a buyer

Debt-ridden Data Transmission Co., the Vienna, Va., special common carrier, is still looking for a merger partner and more outside bank financing, **but with no indications of success.** "Continuing substantial cash deficiencies and operating losses" of Datran and its majority owner, Wyly Corp., make it impossible to generate internally "the additional capital to carry Datran to profitability" in the digital-transmission-service market, according to chairman Sam Wyly. Datran's start-up costs of about $90 million are divided between Wyly Corp. ($43 million) and Haefner Holding AG of Switzerland ($47 million).

Intelsat approval of 10-meter antenna seen spurring sales . . .

The International Telecommunications Satellite Organization has, after prolonged study, adopted standards for a small earth station with an antenna 10 meters in diameter. The move leads industry suppliers to forecast **a surge in sales of the new Standard B stations, particularly among developing nations.** Acceptance of the smaller stations, Intelsat says, is a result of development of single-carrier-per-channel (SCPC) hardware. Such hardware allows traffic to be routed on a circuit-by-circuit basis, rather than in large groups or bundles, thereby minimizing the satellite-capacity loss associated with small antennas.

Intelsat has approved digital SCPC/pulse-code-modulation/phase-shift-keyed equipment for the stations, but says it expects to approve alternative equipment in the near future using SCPC/frequency modulation, as well.

. . . digital TDMA set for 1979 tests prior to adoption

New digital equipment for medium and heavy satellite-communications traffic using time-division-multiple-access/digital speech interpolation (TDMA/DSI) is scheduled for field trials in 1979, Intelsat reports. Assuming successful tests of TDMA/DSI hardware, **Intelsat plans to begin using it operationally in the early 1980s** with Standard A earth stations in the Atlantic Ocean region.

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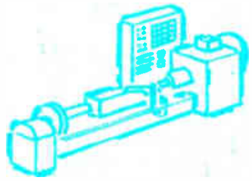

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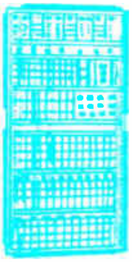

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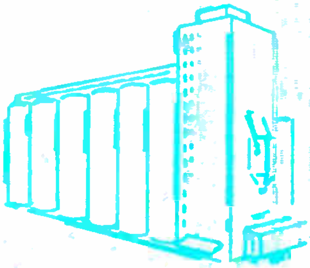

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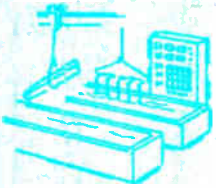

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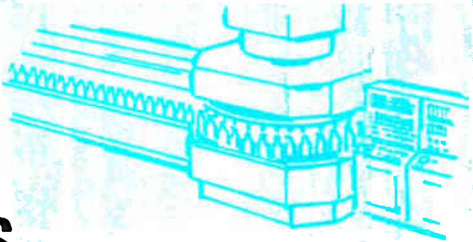

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I²L chip enables size and weight cuts in digitally controlled Canon camera

Digital circuits, including integrated injection logic, help control the analog functions that provide automatic operation and precise exposure calculation in a new camera, while replacing about 300 mechanical parts. The AE-1 35-millimeter single-lens-reflex camera developed by Canon Inc. sells in Japan for about $167 without a lens. Top shutter speed is 1/1,000 second.

Using I²L technology in all of the logic circuits keeps power drain low and facilitates fabrication of analog and digital elements on one large-scale integrated circuit. What's more, Canon designed the camera from scratch to accommodate the electronic controls, which are mounted on a flexible printed circuit that provides both substrate and interconnections. The circuit is sandwiched inside the top and sides of the case.

Size and weight of the camera were minimized by elimination of about 20% of all the mechanical parts. The remaining mechanical components are arranged in modules to simplify assembly and help keep the price low.

Operation. After setting the film speed, the photographer merely sets the desired exposure time, focuses, and shoots. The aperture is set automatically—with or without flash. The shutter speed for electronic flash is automatically set at the optimum 1/60 second. If the flash capacitor has not had time to charge after the previous shot, the aperture is calculated on the basis of ambient light. The approximate aperture is indicated in the viewfinder. Control of the aperture is essentially analog, but storage of exposure data is digital. If either the electronic circuits or the 6-volt silver-oxide battery fails, the camera is inoperable.

The camera contains four semiconductor packages. Two are bipolar integrated circuits from Texas Instruments, one is a silicon photosensor and preamplifier from Toshiba on two chips, and the last is a transistor that switches current to the camera circuits when the first of two switches is actuated by partially depressing the camera button.

One of the bipolar ICs, only 3 millimeters square, contains about 1,200 elements, about half of which are made with I²L digital technology, and the rest with linear. This device contains a 20-stage frequency divider and drivers for the light-emitting diodes. The second bipolar IC, of several hundred elements, contains most of the high-power circuits. These include the ultra-stabilized power supply, solenoid drivers, and other linears.

The preamplifier chip in the photosensor package is essentially a bipolar operational amplifier with an MOS-field-effect-transistor input stage. It also includes feedback to achieve logarithmic transfer characteristics. This technique keeps the signal-to-noise ratio high. □

Around the world

British digital fuel-injection system is precise

A precise digital fuel-injection system built around two custom-designed chips is being road-tested by the Lucas Electrical Co. for introduction on passenger cars in the near future. The preproduction version comfortably meets the tough pollution-control laws of Europe and the U.S. A plug-in replacement for analog controls, the system is even said to comply with the stringent 1977 California emission standards. The first technical details of the system were presented in early July at the Automobile Electronics Conference, sponsored by the Institution of Electrical Engineers in London. The system, which works with conventional analog sensors, pinpoints engine speed, manifold pressure, and temperature better than does analog control. The digital system, made with collector-diffusion-isolation technology, plots 16 points along an engine's speed curve, in contrast to only five for an analog unit. And it also continuously interpolates eight manifold pressure points into its quick response to engine demands.

Microprocessors analyze tumor thermograms

Affordable real-time analysis of thermograms for noninvasive diagnosis of breast tumors is in sight. At the University of Zurich's Institute for Biomedical Engineering, a group is well along on a microprocessor version of a medium-computer system developed there to evaluate thermograms in real time. The computer-analyzed thermograms are coded to 8-bit accuracy on a video display in 16 color levels, measured with 0.2°C resolution. The second-generation system is expected around September. The price of the on-line processor and display will run about $16,000 (the spectrograph proper, from Uthe Technology International of Sunnyvale, Calif., sells for between $30,000 and $40,000). Three microprocessors and a charge-coupled-device memory chip replace a PDP 11/40 central processor from Digital Equipment Corp. The hardware includes a 28,000-word-by-16-bit core memory, a disk memory, a memory for the video display, and a Ramtek GX-100A color-display unit. A 16-bit Texas Instruments 9900 microprocessor chip is connected by a 16-bit bus to a display processor built around a Motorola M6800 chip. This 8-bit processor will control a 256-by-256-bit CCD refresh memory for the display monitor. Color coding comes from a look-up table, also based on a Motorola M6800 microprocessor.

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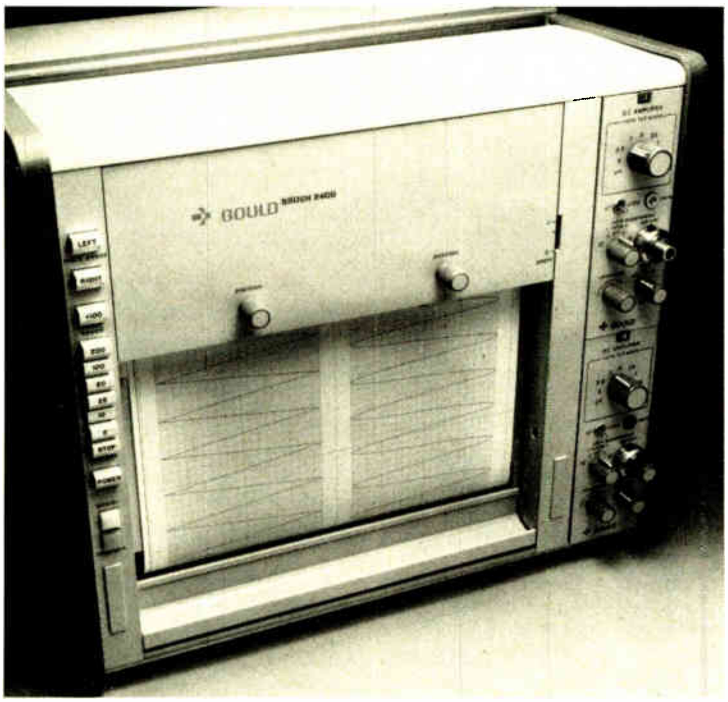

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Fujitsu develops bubble RAM to vie with rotating type

Fujitsu Ltd., which for about a year has been operating an experimental bubble random-access memory with a capacity of 10,000 bits per chip, is now developing one that has eight times that capacity. Although the company won't estimate a completion date, it says **the price of a module containing 16 of the 80-kilobit chips will be competitive with that of rotating memories of similar 1.28 megabit capacity.** What's more, efforts will continue to drive the price below that level.

The chips, which measure 4.9 by 5.5 millimeters, will be configured in coils of four chips each, with four coils to a module. The access time will be 0.9 to 1 millisecond. The 10,000-bit chips, which have an access time of 1.6 millisecond, measure 3.3 by 4.3 mm. A memory consists of 20 chips in a single coil for a capacity of 200 kilobits. Although the memory is now available, few orders are expected because of the high price.

Satellite carries digital color-TV signals in UK

In a step toward replacing analog fm transmission in the United Kingdom, the first digital PAL color and sound signals have been transmitted through an Intelsat-4 satellite. The trial, conducted jointly by the British Post Office and the British Broadcasting Corp., tested equipment developed by both. A multiplexed signal of 60 megabits per second, consisting of a digital PAL video signal of either 44.3 or 53.2 Mb/s with a sound channel of 2,048 kilobits per second, was split into two 30-Mb/s parallel streams plus a clock signal.

These streams were fed into a differentially encoded quadrature phase-shift-keyed modulator, whose output was up-converted to super-high frequency, amplified, and transmitted to the satellite by means of a transponder with a bandwidth of 36 megahertz. **Although high-quality pictures were received, the BBC says that more research is needed to find the optimum bandwidth for transmission** before it will replace its extensive analog fm equipment.

French instrument uses ultrasound to find brain damage

A small French medical-electronics company called Codimex is marketing a $20,000 ultrasonic instrument that can match an expensive brain scanner in spotting some kinds of brain damage. Instead of using computer mapping as brain scanners do, Codimex's instrument analyzes the echoes that develop inside a skull when ultrasonic probes are held against it to locate brain zones where the blood flow is abnormal. Echo signals from 16 selectable intracranial zones are sorted out electronically. **Such damage as lesions, vasculopathies, and hematomas are located by comparing oscilloscope traces for the selected zone, the symmetric zone, and the summed traces across the brain.**

Germany starts its electronic centers for switching data

After lengthy preparation, West Germany's Bundespost has embarked on its EDS program to blanket the country with a grid of electronic data-switching systems by the end of this decade. **The 24 EDS systems, to be located in 18 cities, will form the hubs in the integrated tele-typewriter and data network** for which the Bundespost has earmarked more than half a billion dollars from now through 1980. The modular program-controlled exchange system will accommodate future requirements, including the ever-growing volume of data traffic.

International newsletter

4-bit microcomputer is faster, cheaper than predecessors

The 69 instructions of a 4-bit-microprocessor family introduced by Nippon Electric Co. cut in about half the execution time of previously available systems with only 40 to 50 instructions. Moreover, at $40 each in lots of 1,000, the two-chip μcom-41 is about 30% less expensive than three-chip microprocessors. One chip in the minimum set of two is the microprocessing unit, and the other contains semiconductor random-access and read-only memory. The ROM has a capacity of 2,048 8-bit words, and the RAM's capacity is 128 4-bit words. The μcom-41 interfaces directly with a 64-key keyboard and a 16-digit display, but an interface chip is needed to add ROMs, RAMs, and a printer controller. **NEC does not intend to export the μcom 41 because software routines are not in English, and there is no second source.**

French allocation for phones exceeds defense spending

In an effort to renovate its outmoded telephone system, the government-run Postes et Télécommunications (PTT) has been allocated a huge $12.6 billion in France's 1977 budget—24% more than this year's allocation and more than the government is devoting to defense. The money will go toward adding 1.7 million lines next year, compared to the 900,000 that were installed in 1975. The bulk of the telephone expansion will be undertaken by the French electronics group Thomson-CSF, with the Metaconta system made by its new subsidiary, le Matériel Téléphonique.

Code change could speed digital phone transmission

By simply changing the digital coding, the British Post Office could boost the speed of its emerging per-second telephone-trunk system, which operates at 120 megabits a second, to the higher continental rate of 140 Mb/s. That claim is being made by Standard Telephones and Cables, which is apparently putting the proposal on the back burner while it supplies the BPO with its 120-Mb/s equipment.

For the higher rate, STC says, repeater spacing would be unchanged, and only **relatively minor modifications would be required for the automatic-gain-control circuits, dependent regenerative repeaters, and supervisory systems within the repeaters.** Also, the coding of digital information would have to be changed so it could be sent between repeaters from 4 binary bits to 3 ternary bits or from 6 binary to 4 ternary bits.

Addenda

Intermetall GmbH has started sending to several large television-receiver manufacturers samples of a pair of MOS integrated circuits that digitally tune color-TV sets by voltage synthesis. The German member of the ITT semiconductor group says it will begin by year's end full production of the set, consisting of the SAA 1020 memory IC and the SAA 1021 control IC. . . . Motorola has reached an agreement with France's Thomson-CSF subsidiary, Sescosem, **to second-source its M6800 microprocessor.** The two companies will also exchange microprocessor information. . . . **Hitachi Ltd. has begun selling microprocessor kits compatible with Motorola's M6800,** as well as memory chips that duplicate products from Motorola, Intel, Texas Instruments, and others. The Japanese company wants Motorola to second-source several chips that it supplies. . . . Rockwell International has begun negotiating a cross-licensing agreement with an **unidentified Japanese company that will second-source such products as its PPS-4 and PPS-8 microcomputers.**

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Shuttle avionics gets on its mark

$600 million worth of equipment set to go when first orbiter is rolled out in September, says Rockwell Space division

by Larry Waller, Los Angeles bureau manager

No show-stoppers have popped up yet to cause delay in developing the avionics hardware for the September rollout of the first Space Shuttle orbiter, NASA's major remaining manned space program. "That in itself worries us," quips S. Z. Rubenstein, the associate chief engineer for the avionics at Rockwell International's Downey, Calif., Space division. The value of all orbiter avionics is set at 21%, or about $600 million, of the total $2.9 billion NASA contract, under which the division is building two spacecraft for 1980 delivery.

The Space Shuttle is intended as a relatively inexpensive transportation system for delivering vehicles carrying up to 65,000 pounds of payload into near-earth orbit. The orbiter will save money by being reused for as many as 100 missions. The shuttle is aimed at a low-cost goal that, if achieved, could offer dramatic reductions in the economics of putting space vehicles of all types into orbit. Its cost per pound of payload is projected at $160, for example, against present probable costs of about $700 and the Apollo mission figure of nearly $3,000.

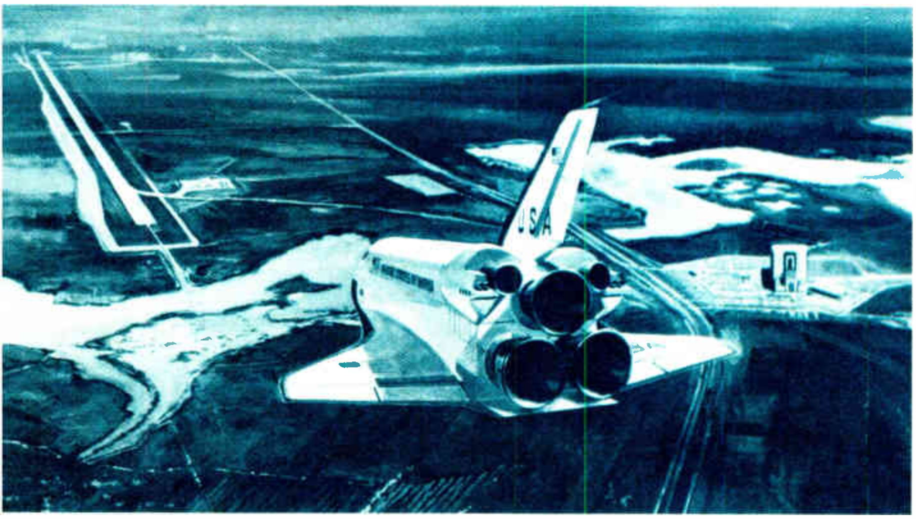
Besides IBM, Sperry Rand, and Cutler-Hammer, other avionics contractors include: Honeywell, for the flight-control subsystem and radar altimeter; Singer Co.'s Kearfott division, which supplies the inertial measurement unit; Bendix Corp.'s navigation and control group for air speed, velocity, and surface-position instrumentation; and Rosemount Inc., which builds temperature sensor equipment and indicators.

The challenge to build a single avionics system that can perform four greatly different manned flight-control functions is unprecedented, Rubenstein says. "It has to fly a craft that goes up like a rocket booster, orbits in space for up to 30 days as a space lab at 18,000 miles an hour, returns to earth as a re-entry vehicle, and lands like an airplane." Landing the orbiter without power at 250 miles per hour with only one chance to hit a 150-foot-wide, 15,000-foot-long runway has never been tried before, the Rockwell engineer notes.

Modifications. Because of reliability requirements and cost constraints, "we tried to put it together with off-the-shelf hardware wherever possible," he says. The result is that about 70% of the avionics equipment consists of modifications of proven designs, and the remaining parts and technology are "mature." None of the subsystems presents serious development problems. But "integrating them is the major job," points out Rubenstein. The complexity of the mission, combined with the need for triple redundancy, puts 1,753 avionics black boxes in each orbiter. These alone weigh about 6,000 pounds, and wiring and interconnections add 6,000 pounds more.

One subsystem that breaks new ground is a fly-by-wire digital flight control that grew out of earlier NASA programs. The digital control eliminates all electromechanical control linkages, substantially reducing weight while meeting the 99.999% reliability goal set for this critical equipment. In operation, all signals between pilot controls and numerous actuator systems go through the central digital computer. For the first time in a manned

Going home. Artist's conception shows Space Shuttle orbiter making landing approach. The reusable craft is to be launched and landed at Kennedy Space Center and Vandenberg AFB



space program, no manual backup is provided.

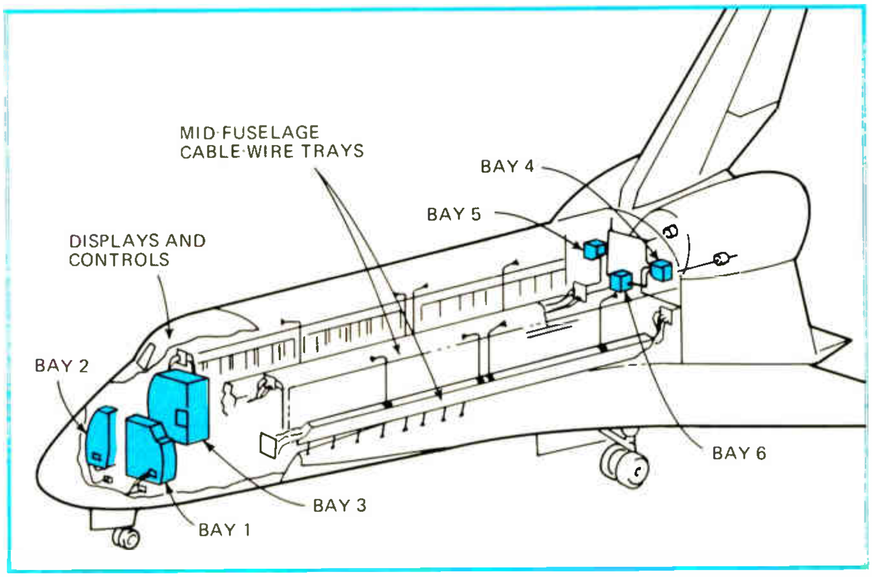
Rubenstein explains that the orbiter fly-by-wire is quadruple-redundant, operated simultaneously with four AP-101 computers. An identical, but separately wired, AP-101 provides a fifth level of redundancy. Consisting of IBM hardware integrated by Rockwell, this computer is capable of performing 400,000 to 500,000 operations per second. An IBM systems engineer on the program claims the hardware is "99% proven in other machines." Each computer has access to 64,000 words of core memory, divided into 40,000 words in the central processing unit and 24,000 words in the input/output processor.

Interconnections. In testing, a "good surprise" to Rubenstein has been the performance of the mammoth wiring assembly, which amounts to 90,000 separate wire segments and 220 harnesses. About 600 pounds of wiring were eliminated by using multiplexer/demultiplexers to send data between controls and instrumentation located in forward and aft sections of the orbiter. These units, which utilize hybrid integrated circuits, are built by Sperry-Rand Corp.'s Flight Systems division.

Avionics equipment is divided into six bays, three forward and three aft. For environmental reasons, controls, communications, and computer hardware are in the forward pressurized crew section near displays and guidance sensors. Supporting electronic driver equipment is mounted in the rear bays near aerosurface and engineer actuators.

Rockwell received the breadboards late in 1974, Rubenstein recalls, and started "hanging black boxes together in early 1975." This promptness permitted thorough testing in a full system configuration of components that are virtually inaccessible in the final assembly.

All flight-control hardware is now installed on the first orbiter, and subsystem checkout is being completed for the September delivery to NASA at Edwards Air Force Base, Calif. There, further system tests



Packed away. Cutaway drawing shows locations of six bays containing avionics equipment. Controls, communications, and computer hardware are in forward pressurized crew section

will proceed before early next year when the orbiter in the initial phase of flight tests will be flown while attached to the top of a special Boeing 747 jet. After that, the orbiter will be launched from the 747 for landings.

Under a $2.8 million contract with Rockwell, Cutler-Hammer's AIL division supplies the on-board navigation sets for the microwave-scanning-beam landing system. The sets include distance-measuring equipment, interrogator, and receiver/decoder units. The AIL division also builds the ground-based equipment for NASA.

Basically a more accurate version of one developed for U.S. Navy aircraft carriers, a microwave scanning beam in the system provides flat wide coverage sweeping the landing sector to about 40,000 feet from the runway and up to 10,000 ft in altitude. Coded pulses from the ground transmitter identify the beam's angle in real time, and a receiver in the shuttle avionics decodes these pulses to determine a precise flight track. Position data, such as azimuth and elevation angle and distance, are supplied by the navigation sets to the orbiter's computer, which continuously corrects the flight path. The landing system is said to be the most accurate ever built.

Hurdle. The next major hurdle for shuttle avionics is development of the full communications subsystem. That project poses some problems, Rubenstein admits, especially in interfacing, not only with the ground stations, but also several different satellites. TRW Systems of Redondo Beach will soon be named a major subcontractor for this equipment.

The equipment must be able to handle 1 megabit per second of wideband data plus 72 kilobits per second of digital data in the up-link. From the orbiter down, the need is to accommodate 52 megabits per second of digital, or 4.2 MHz of analog data simultaneously with 2 Mb/s of digital data, or 4.2 MHz of analog simultaneously with 2 Mb/s of digital data. In the first space flights, two-way S-band radio equipment will provide links for both voice and data. Later, a Ku-band radar will be added for rendezvous with passive satellites, plus another Ku-band link for wideband data exchange with tracking and relay satellites.

About 1,000 people are working on shuttle avionics at Rockwell, a figure termed by Rubenstein as "about a third the number for the same job on Apollo." In addition to building the two shuttles, Rockwell is systems integrator, a task NASA itself performed for Apollo. The major subsystems, about 200 of them, and components in the avionics are supplied to Rockwell by 50 outside contractors. □

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1974			
NMOS	MW7001ID	CMOS	CD4039AD
CMOS	CD4036AD	CMOS	CD4061AD
1975			
SOS	MWS5001D	SOS	MWS5501D
SOS	MWS5040D	SOS	MWS5540D
1976			
Now . . .			
NMOS	MW4050D	NMOS	MW4060D
NMOS	MW4050DVI	NMOS	MW4060DVI
NMOS	MW4050DV2	NMOS	MW4060DV2
Coming . . .			
NMOS	MW4051	SOS	MWS5001A
NMOS	MW4101	SOS	MWS5580
NMOS	MW4104	CMOS	CD40024
NMOS	MW4111	CMOS	CD40032
NMOS	MW4112	CMOS	CD40061

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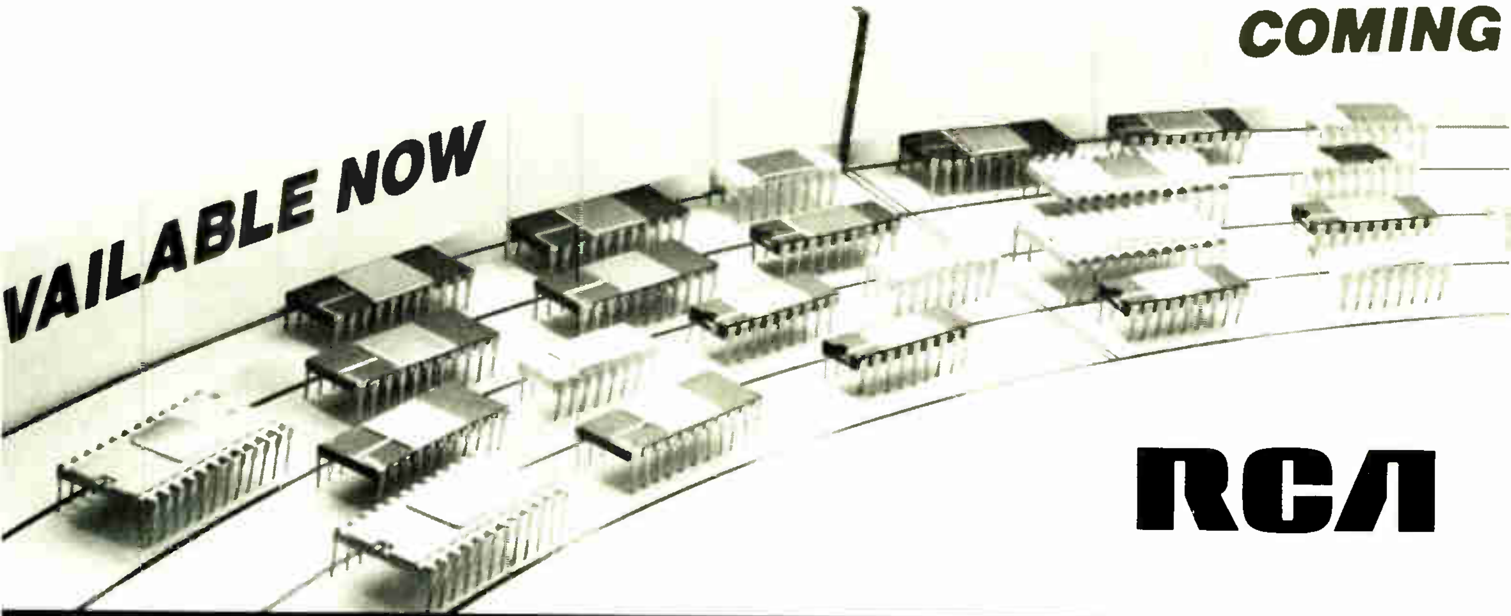

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Computers

Island trip boosts reliability

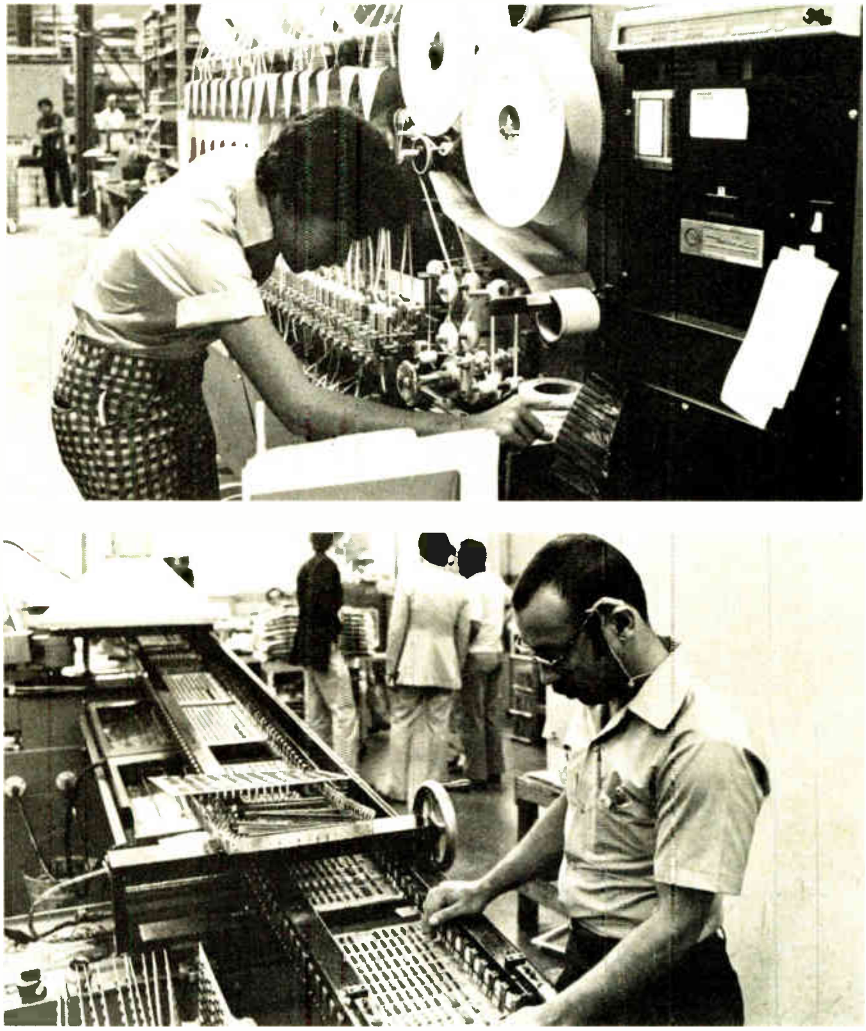
DEC's test facility in Puerto Rico helps keep failure rate of LSI-11 microcomputer to 0.006% in first six months

by Lawrence Curran, Boston bureau manager

The low field-failure rate of Digital Equipment Corp. LSI-11 microcomputers underscores the importance of DEC's substantial investment in a sophisticated test system in Aquadilla, Puerto Rico, where it enjoys a flexible tax holiday and wages lower than those on the mainland. A little more than six months after DEC began shipping the board-level microcomputers, only 63 of more than 3,000 LSI-11s shipped to date have been returned as defective. Robert Van Naarden, product manager for component computers in the Components group at Marlboro, Mass., says that only 20 of those returned were faulty—a failure rate of 0.006%.

"We don't have any control over the environment where the LSI-11 will be used," Van Naarden points out, because DEC's OEM customers mount the boards in their own cabinets as they see fit, not always providing the nearby fan cooling that DEC designs into its boxed minicomputers.

That's why the LSI-11 goes through a rigorous checking sequence, beginning in Marlboro with tests of the four-chip microprocessor set supplied by Western Digital Corp., for which DEC is its own second source. After visual and gross-leak inspections, the chip set is cycled 50 times from -40 C to +150 C, is put through a thermal-intermittent test in which it's allowed to cool from 100 C while electrical continuity is checked, and then electrically tested on a Tektronix 3260 system. The latter runs 100% functional and electrical tests "with every diagnostic that can be run on the chip," says Steven



On their way. Top photo shows computer diodes being unrolled from shipping reels, while in bottom photo memory board is loaded onto belt of a wave-soldering machine

Teicher, manager of the Small Systems group in Maynard, Mass. There's also a short 30-volt stress test.

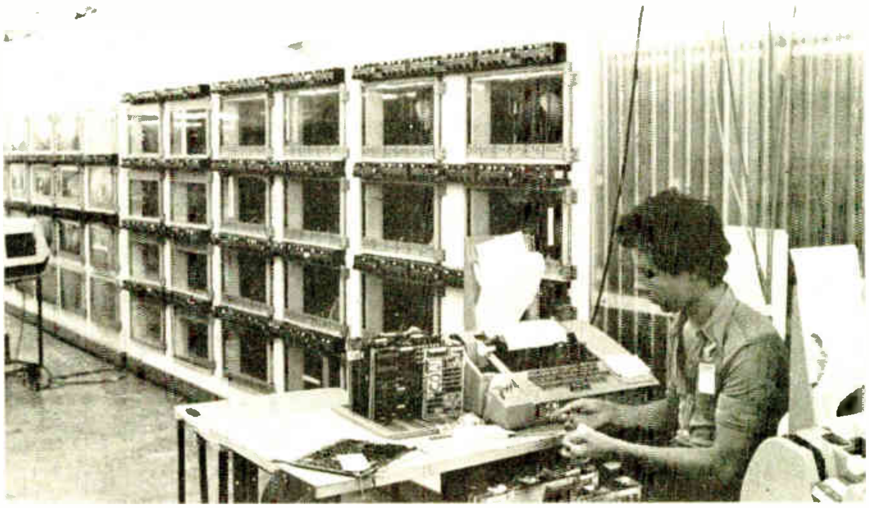
Island tests. The units that pass those tests are then shipped to Puerto Rico, where DEC employs 2,200 persons at two sites. The 4-kilobit random-access memories are inserted onto boards at San German, on the island's west coast. That facility produces 5,000 stuffed boards per day, for the LSI-11 and DEC minicomputers, as well. From San German, the LSI-11 boards go some 20 miles up the coast to Aqua-

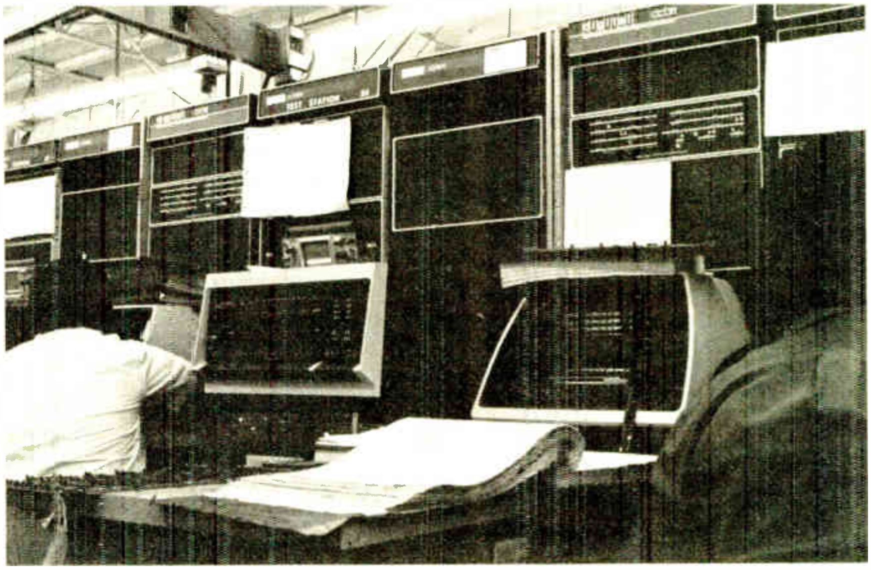
dilla, where the rest of the chip set is inserted, and the final obstacle course is run.

The Aquadilla system-assembly and test facility is run by three PDP-11/40 computers that essentially control the entire plant through 500 serial-data lines. The API (automatic product-test) system puts the LSI-11 and other DEC computers through their paces, beginning with a GenRad 1792 logic tester that isolates LSI-11 faults to a single line of the board. Faults detected here usually turn out to have been caused by imperfect wave-soldering of connections or something other than device failures, and Teicher says that almost everything that fails this station can be repaired. Boards with faults are shunted aside at each of the Aquadilla test stations for repair, then returned to the test flow.

Checking repairs. A "quick-verify" station is next. There, the API system puts the board through further diagnostics to check the repairs. The boards then go to a bank of temperature chambers for thermal cycling between 0 C and 55 C while the LSI-11 runs through its instruction set. This step can take 16 to 24 hours, and technicians can alter the test script dictated by the API.

Thermal cycling is followed by a final acceptance and quality-control station, at which another quick verification under power makes sure that all tests and repairs have been made and that the board is still working properly. Finally, the LSI-11 board is packaged for shipment back to Marlboro, along with the full-box computers that have gone through the Aquadilla plant, including the PDP-11/03, the cabinet-housed versions. □





Station to station. Top photo shows loaded board being functionally tested to pinpoint faulty IC. In center, thermal chambers in background cycle LSI-11 and other DEC computers from zero to +55 C while the computer is put through its instruction set and diagnostic routines by automatic product test system. In bottom picture technicians monitor progress of LSI-11 testing at the company's Aquadilla, Puerto Rico testing facility.

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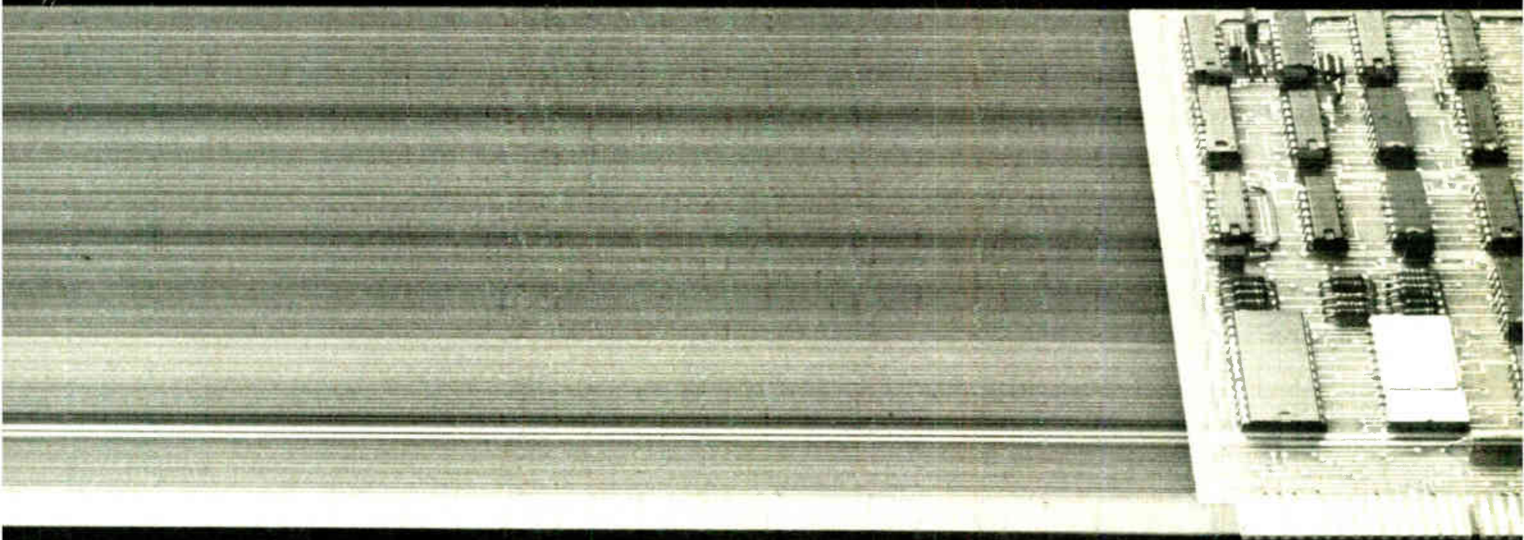

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Consumer electronics

Coming: programable video games

Fairchild's VES awaits type approval, while Admiral's Videospond concept waits until the time is right

by Gerald M. Walker, Consumer Electronics editor

Relatively simple paddle-type video games have hardly hit the market, but the TV industry is already getting psyched up about the next generation—programable games that will be based on microprocessors.

For instance, the generally acknowledged hit at the recent Consumer Electronics Show in Chicago was the Fairchild Video Entertainment System (VES) developed by the company's Consumer Products group and produced by its Exetron division. Even game-company competitors admitted that VES was a major attraction. The reason is obvious: the hockey/tennis/ping-pong types of games being built around single hard-wired LSI chips are no match for the microprocessor-controlled system in variety of games and sheer playability.

While the Fairchild games were drawing enthusiastic players, the Admiral group of Rockwell International was privately demonstrating the capabilities of its microprocessor TV system, called Videospond. However, unlike Fairchild, Admiral has emphasized that Videospond is not yet a product for sale, but a concept to be developed when the time is right. And the Fairchild game has not received type approval from the Federal Communications Commission for attachment to a TV antenna.

But Fairchild thinks the time is right. "We think that unless consumers can get the programability and 'play value' of a microprocessor-based system, they are buying obsolescence," says Greg Reyes, vice president and general manager of Fairchild's Consumer Products group.

High-level gamesmanship. Fairchild's VES uses microprocessor and digitally encoded cartridge-loaded tapes to program a variety of games. By year's end, five will be on sale

However, others in the games arena feel that there will be too distinct product lines—the high-end programables and the low-end single-chip models. Scott Brown, marketing director for National Semiconductor's Consumer Products division, reports that the company's new three-game model, Adversary, which sells for $99.95, will be joined next year by a programable game. "But the National programable game will use a dedicated microprocessor and have a complete library of selections available from the beginning," he adds.

The Fairchild programable uses a four-chip F-8 microprocessor set with additional random-access memory and video-modulator circuits. However, by next year, the VES will probably be sporting a dedicated microprocessor, according to the company. The present model, which consists of a console for the top of the TV set and attached joystick controls, will retail in the $100-to-$150 neighborhood.

Its main feature is the $20 Videocart cartridges, which are digitally encoded tapes that program the various games. By the end of the year there will be five Videocarts, offering 10 games and four mathematics quiz games.

In addition, there are two games built into the console: tennis and hockey. But, with the microprocessor in control, this version of tennis and hockey is far more challenging than the low-end video games. The joystick that controls the paddles rotates players, as well as moving them anywhere on the playing surface. Not only is there on-screen scoring, but, in the hockey mode, it's possible to put a time limit on play and have overtime periods in case of a tie during regulation play. During all the games, elapsed time of play is shown on the screen.

One of the fascinating features of the games in the first Videocart is Doodle. The joystick is used to control a four-video-line cursor to "draw" with three colors (red, blue, and green) selected on the console. In addition, there's Quadra-Doodle, in which the processor forms random, kaleidoscopic patterns on the screen. No matter what the game, it is possible to freeze the action indefinitely if there is an interruption or if the players decide to switch back to watching broadcast television programs.

Keyboard, too. Admiral's Videospond, designed around Rockwell's PPS-8 microprocessor is estimated to cost just under $1,000. This system is really more of a home computer than a game, although it will be possible to play games if desired. Being an interactive system, Videospond has both joysticks and a keyboard that operates in two modes for inputs. It is programed by digitally encoded audio cassettes. These cassettes are also used to record, store, and play back information, as well as for programing the PPS-8.

In demonstrations during the Consumer Electronics Show, Videospond performed in four distinct modes: programed instruction; information storage with text editing; "prompting" calculation, such as figuring out the proper diet and exercise required to reach an individual's ideal weight, and highly sophisticated entertainment—such as drawing color pictures on the screen and storing them on the cassette—and thought games played against the computer. In the drawing setup, it's possible to program a "palette" of colors for composing the picture. And this system can even perform elementary animation accompanied by audio commentary.

"We feel that the microprocessor in the home can do many more tasks, but it will take a full library of program tapes, and that takes time and money," says William Slater, director of research and development for Admiral. □

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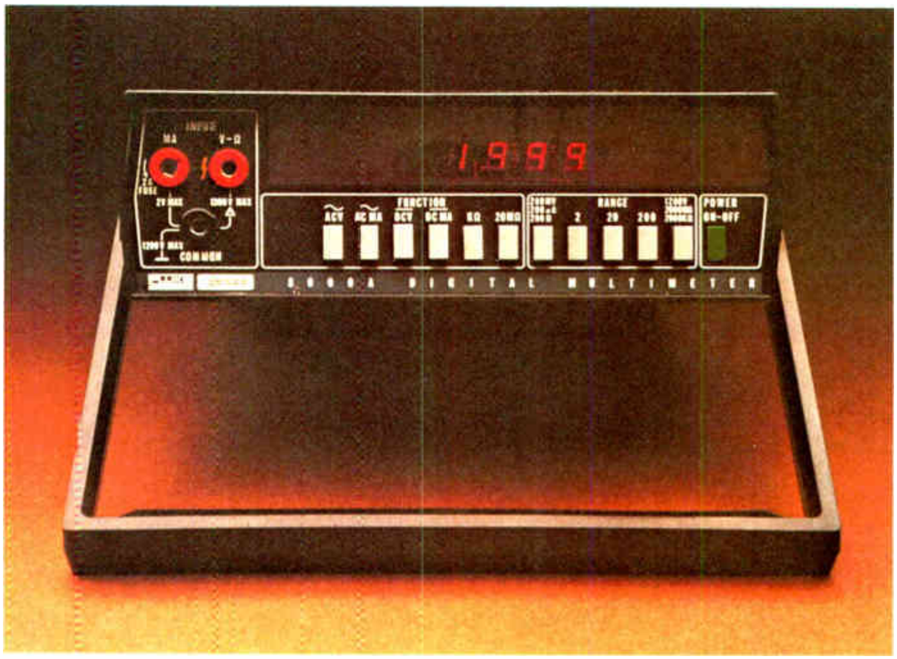

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Memories

Semiconductors add system share

But core houses say they can hold their 75% or 80% of business in OEM memory systems, despite onrush of new competitors

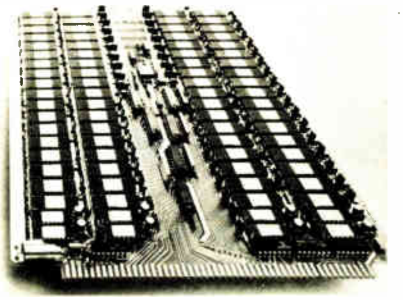
by Stephen E. Scrupski, Computers Editor

"Our OEM business is growing," says Intel Corp.'s Richard Egan, general manager of the Memory Systems division. "It's now twice what it was a year ago, and we expect it to double again in the next six months." That's typical of the bullish outlook of the men who run the rapidly growing memory-system divisions of semiconductor houses. The list, including Intel, National Semiconductor, Advanced Memory Systems, Electronic Memories and Magnetics, and Monolithic Systems, will probably grow as more semiconductor makers eye the burgeoning market.

Don Miller, National's marketing manager for memory-system products, for equipment manufacturers, puts that market in perspective when he points out that although there is a lot of interest in the IBM add-on market, the OEM business will far exceed it. He pegs it as three to four times bigger, and growing. And semiconductor makers like to point out that memories are, after all, essentially supercomponents—units with address lines on one end and read-write lines on the other, and that's all the technology that most users care about.

The market has fuzzy boundaries. Its major segments are memory boards sold to terminal makers and the like, complete memory chassis sold to major systems houses that also buy minicomputers to assemble into specialized systems, and add-on or add-in memories for existing minicomputers that may be sold to end users. The value of the systems side of the OEM memory business is estimated by Miller at $400 million in 1975. Of that, he says, about $150 million was bought outside as memory systems. And of the $150 million, semiconductor memories accounted for 20%. In 1976, he says, that total will reach about $200 million, with semiconductors increasing their share to 25% to 30%, or $50 million to $60 million.

But the makers of the rival core systems aren't being frightened away. Their strength is firmly on two major factors: conservatism among big users and the need for data retention when power is shut down—nonvolatility. Few doubt that once the 16,384-bit random-access memories come on stream in a year or two the 400% step-function increase in density may be too tough for the core memories to compete with. But the cores still are battling at the 4-k RAM level. Not only that, but core makers promise a few more tricks—production innovations to lower cost—to keep themselves in the market for a while.



On a card. This in-40 from Intel's five-year-old Memory Systems division can carry 16 kilowords by 18 bits, or 32 by 9.

Core makers like to point to the "integrity" of the data in a core memory when they make comparisons with semiconductor versions. Al Sroka, marketing manager for core-maker Ampex, points to the need for error correction in semiconductor memories as evidence of questionable integrity.

The semiconductor manufacturers counter such arguments by pointing out that, in large memories, the extra bits needed for error correction do not add much to the cost, while battery backup in case of power failure is regularly provided—and more users are accepting it.

In fact, Monolithic Systems, is building a line of complementary-MOS memories with batteries built into the boards for small systems.

Error correction, however, is only a transitory obstacle for semiconductor memories, says Gary Anderson, marketing manager for OEM memories at Intel. "Eventually, the reliability of semiconductor memories will demonstrate that error correction is unnecessary, except for the long word lengths where the overhead is so much smaller that the penalty can be easily absorbed."

But if the makers of core and semiconductor systems have anything in common, it's their fascination with the bottom line. Both are now selling for about the same prices—0.25 cent a bit, with 0.3 cent typical for memories of 16,364 words by 16 bits. But Ampex's Sroka doubts that semiconductors can hit that 0.3-cent mark in small quantities—100 boards or so. In those cases, says Sroka, 0.38 cent would be closer to typical. And, he adds, cores are down to 0.15 cent per bit in the larger sizes—256,000 words by 20 bits—with the 0.1-cent level in sight within a year to 18 months. □

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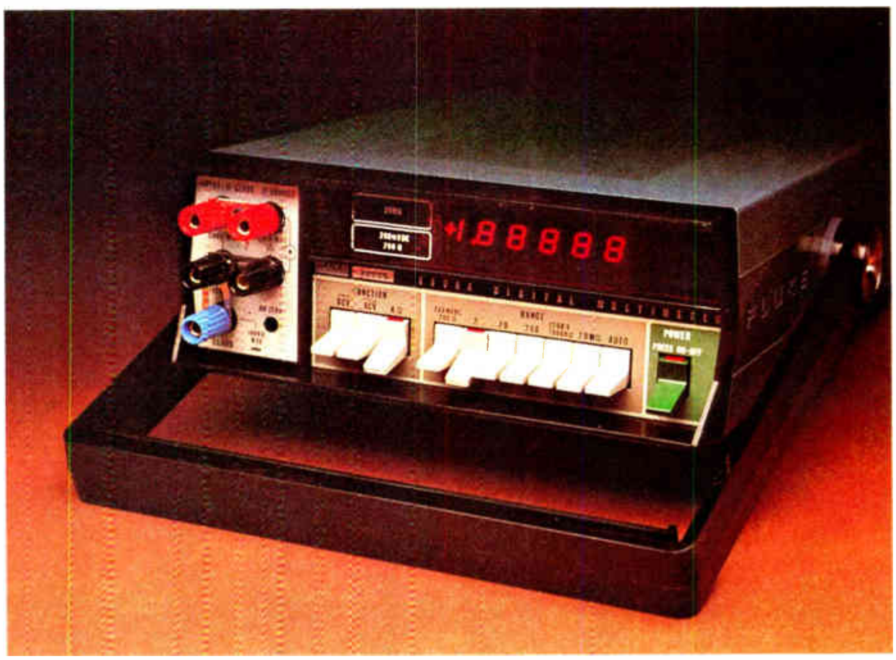

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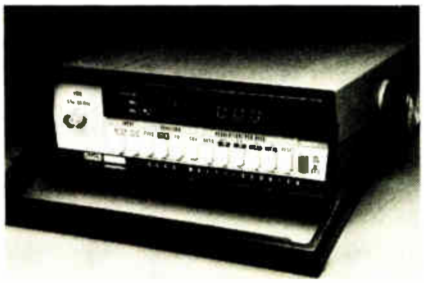

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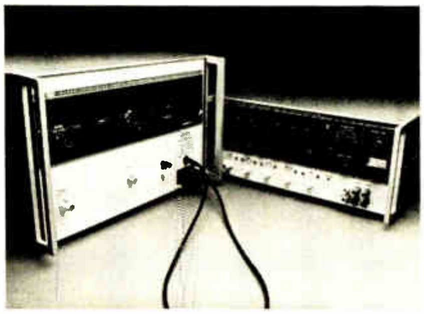

5200A AC Calibrator and 5205A Power Amplifier

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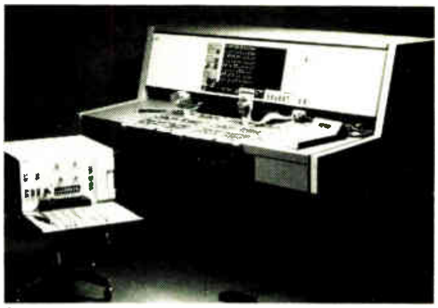

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Data acquisition in a DIP shrinks systems

Thin-film hybrid technology provides inexpensive single package for digitizing 8 analog input signals

by Robert Calkins and Arthur Berg Jr.,
Micro Networks Corp., Worcester, Mass

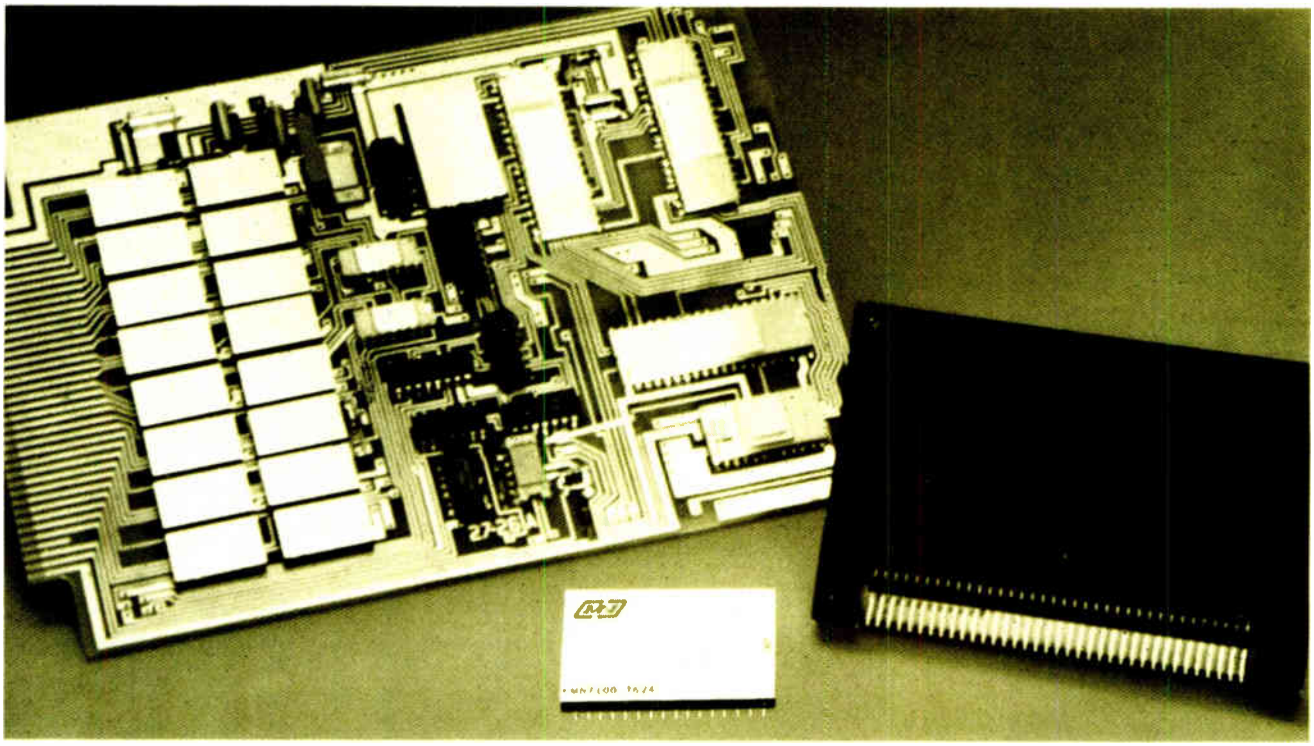
☐ Treating a data-acquisition system as a plug-in building block, much like an operational amplifier, is no longer merely a designer's dream. While these systems have shrunk in the past year from one or more pc boards to hand size, the application of thin-film hybrid technology now has made possible a complete eight-channel device in a single 32-pin dual-in-line package.

System design made easier

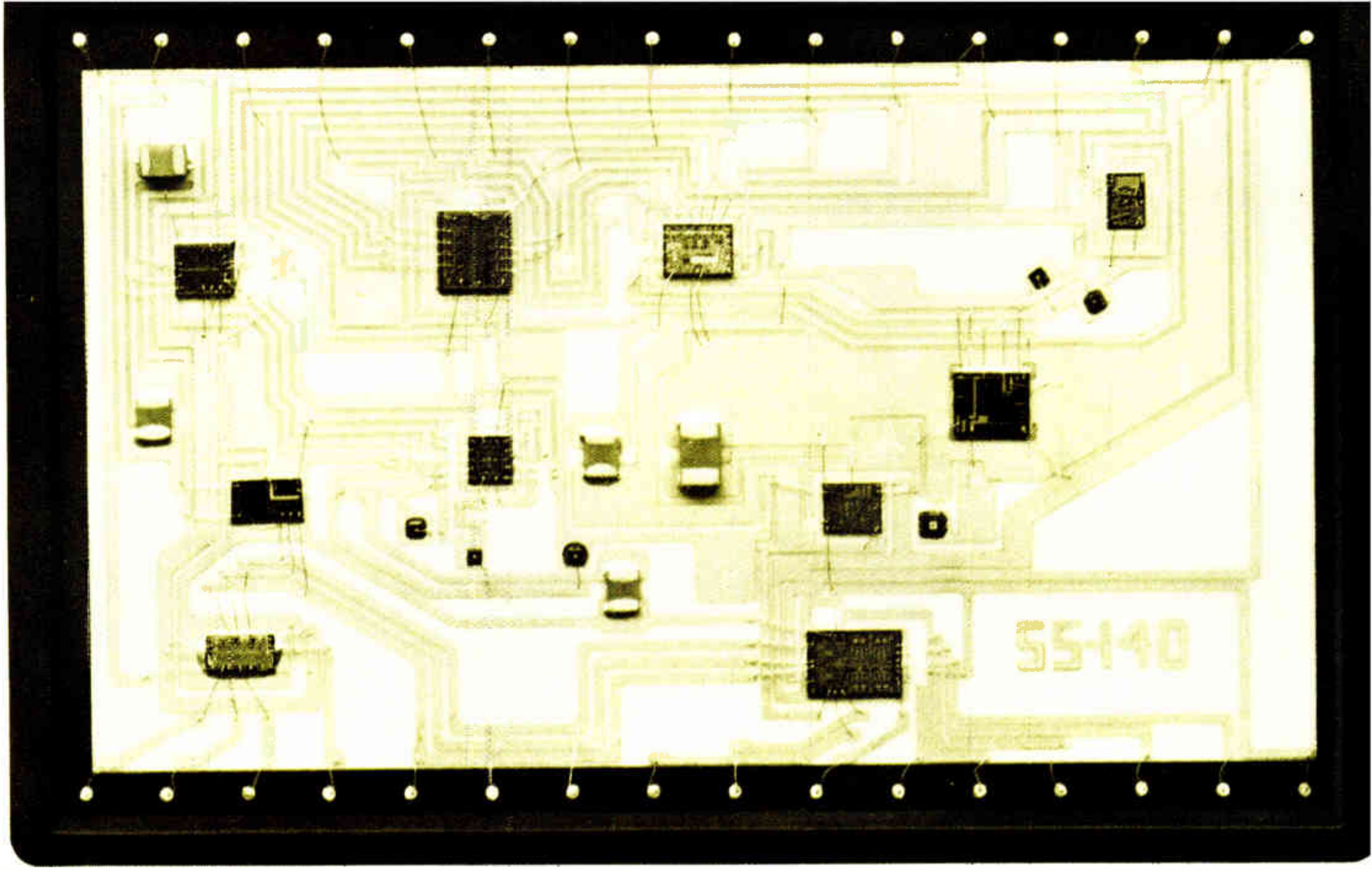
Aside from the obvious space savings, such a hybrid greatly simplifies the design of data-processing systems and often can result in considerable cost reduction. It effectively brings a systems function down to the component level.

Ideally, the data-acquisition end of a monitoring, control, or communications system should be no larger than the digital circuitry or computer it supports. And, if the microcomputer is to realize its full potential, then input/output interface systems must be developed to the same degree of sophistication as the microcomputer itself.

Because of its package and performance compatibility with the integrated-circuit microprocessor, this system-in-a-DIP is an excellent interface element between the processor's digital world and the analog world of



Size dwindles. Only a year ago, a multichannel data-acquisition system required an entire pc board. Then 16-channel 12-bit systems became available as hand-sized modules. And now a complete eight-channel 8-bit system has been squeezed into an IC-compatible DIP.



1. Uncovered. Inside the 32-pin DIP of the MN7100 data-acquisition system is a 21-chip, thin-film hybrid circuit that can multiplex, sample and digitize eight analog inputs. The device even includes integral clock, control logic and voltage-reference source.

transducers and other sensors. Like the microprocessor, the new device, the MN7100, is suitable for a broad variety of applications, including industrial process control, scientific measurement, automotive instrumentation, medical electronics, energy management, and geophysical exploration for vitally needed energy resources.

Within its package of 1.11 by 1.71 by 0.19 inches, the system packs plenty of data-handling power. It accepts eight channels of analog data, multiplexes and samples them, and then converts them to computer-compatible digital signals. All this data manipulation is accomplished with a total system linearity error of only ±0.2%, and all eight channels are digitized within a period of 88 microseconds.

Additionally, the device not only generates its own clock signals, but also contains all necessary control logic and voltage-reference sources. What's more, since it is fully calibrated at the factory, the user only has to apply the three power-supply voltages (±15 volts and +5 V) to have an operating unit. With appropriate external circuitry for logic control and analog-switching, the device's input capacity can be expanded to handle as much as 256 channels of information.

Drawing comparisons

The 8-bit, eight-channel format of the MN7100 provides sufficient speed and accuracy for most commercial and industrial applications at an attractively low price. Less resolution would exclude the unit from many applications, whereas greater resolution would provide better linearity at greater expense, while offering only modest performance advantages for most applications.

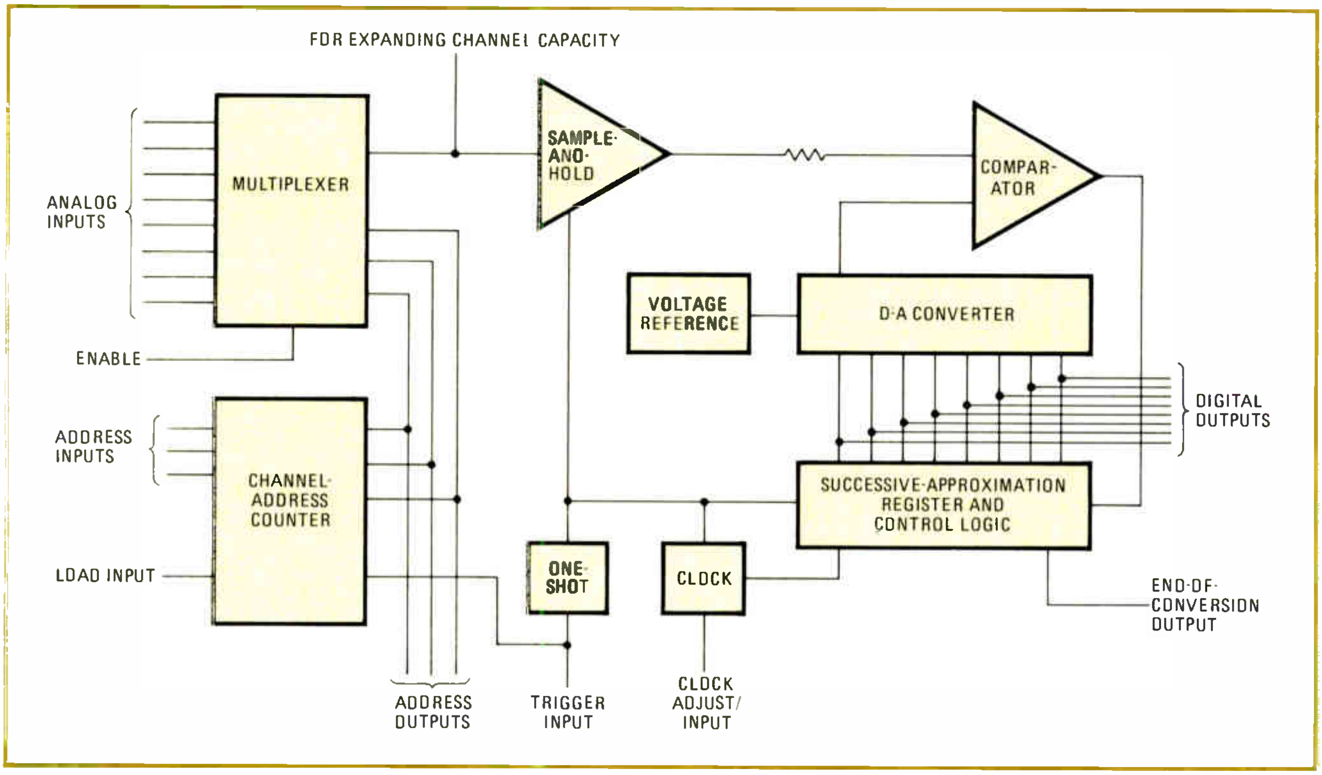
Compared to its hand-sized modular counterparts, the device provides 8-bit resolution with a maximum accuracy error of ±0.4%, as opposed to 12 bits and ±0.02% maximum error. Its eight-channel capacity is exactly half that of the larger units. However, it is about 20 times smaller and consumes about one-third the power. Moreover, the modular systems are generally priced from about $300 to $600 apiece, whereas the MN7100 is $195 each in small quantities, dropping to $140 each in 100-unit lots.

The 32-pin DIP housing is the smallest configuration that gives adequate input/output terminations and control points. Inside the package is a hybrid thin-film circuit (Fig. 1), built with eight commonly available IC chips, six diode chips, a pair of thin-film resistor networks, and five ceramic-chip capacitors.

Fabricating a system with thin films

At this time, to realize such a component monolithically would require a design too complex for adequate chip yields and sufficiently low pricing. Thin-film hybrid technology, on the other hand, permits the part to be fabricated at reasonable cost, while keeping package size comparable to that of a monolithic approach.

The fabrication process begins with evaporation of a thin film of gold onto a ceramic substrate, which is also the insert for the final package. The gold is then masked off and selectively etched away, creating the interconnect pattern and the chip bonding pads. These chips, the zener and signal diodes, require electrical contact to the substrate. Therefore, they are eutectically



2. The works. Circuit operation of the MN7100 is fairly conventional. The desired input channel, selected via the address counter, is fed to the sample-and-hold amplifier by the multiplexer. When the sample-and-hold changes from track to hold mode, the signal is digitized by the a-d converter, which is composed of the d-a converter, the comparator, the voltage reference, and the logic register.

bonded in place at their appropriate mounting sites.

Next, all the other chips are mounted with epoxy, and the entire substrate is then epoxied to the package. Ultrasonically bonding gold wire from point to point makes the electrical connections between the chips and the interconnect pattern and between the pattern and the package leads.

Now the part is ready for functional laser trimming—that is, a laser beam trims the resistor networks while the circuit is powered up. Besides compensating for all errors simultaneously, functional trimming produces a device that is ready to plug in and use without the need for external trimmer potentiometers. Furthermore, it guarantees full interchangeability between units. After laser trimming, the package is hermetically sealed, and the complete assembly is put through a final stabilization bake.

Because of its hybrid construction, the MN7100 is the smallest self-contained data-acquisition system that is commercially available. However, the circuit techniques the device employs are not unusual—in fact, they are similar to those of most conventional data-acquisition systems.

Examining circuit operation

The block diagram of Fig. 2 shows the major circuit elements of the system. Up to eight analog input signals, over the range of ±10 V, can be fed into the analog multiplexer, which is eight single-pole, single-throw complementary-metal-oxide-semiconductor analog switches.

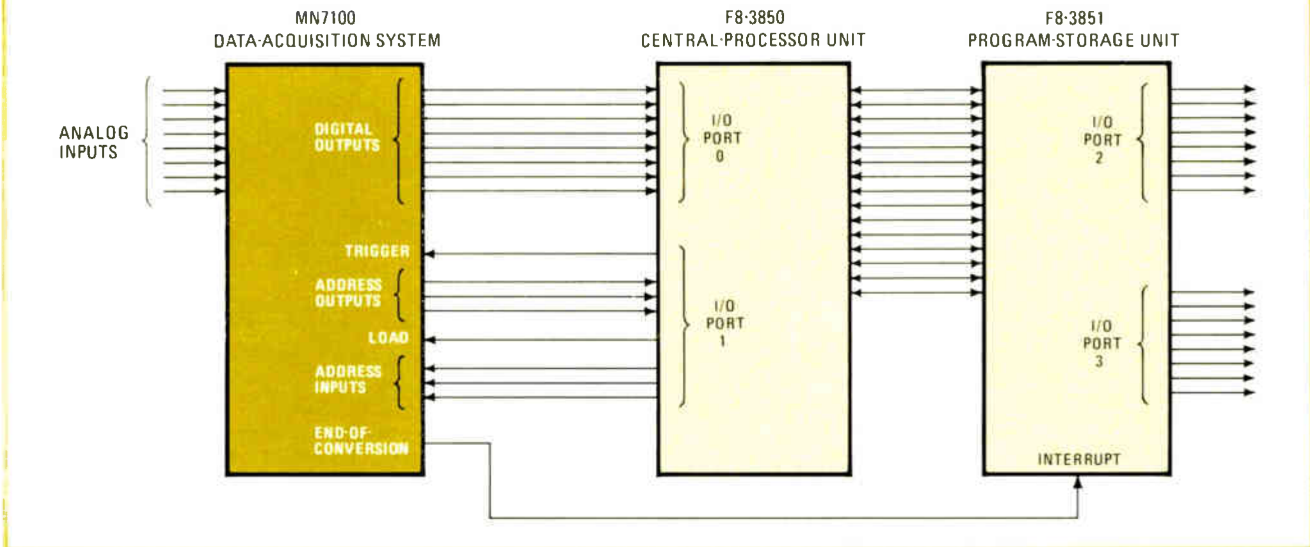
The input channel to be interrogated is selected via the channel-address counter and is then applied to the sample-and-hold amplifier by the multiplexer. A trigger pulse updates the address counter, and the one-shot fires. When the one-shot times out, the sample-and-hold amplifier switches from track to hold mode, and the control logic initiates the analog-to-digital conversion.

The a-d converter is an 8-bit, successive-approximation type made up of the digital-to-analog converter, the comparator, the voltage reference, and the successive-approximation register. Once the conversion is complete, the register supplies an end-of-conversion signal indicating that the output data is valid and that the system is ready to digitize a new analog input.

If a logic low is applied to the counter's load input,the multiplexer operates in a random mode, and the counter's outputs are set by the channel-address inputs. For sequential-mode multiplexer operation, a logic high is applied to the load input, and the counter maintains its count until it is incremented by a negative-going pulse edge at the trigger input. Besides being tied to the multiplexer, the outputs of the address counter connect with external pins, thereby enabling the user to determine which input channel is being digitized.

The one-shot is formed by half of a dual monostable multivibrator, a thin-film resistor, and a ceramic chip capacitor. The negative-going pulse edge of the trigger input updates the channel-address counter and triggers the one-shot, changing its output from a logic high to a logic low. This puts the sample-and-hold amplifier into its track mode and disables the internal clock to reduce noise during acquisition of the analog signal.

About 5 μs after triggering, the one-shot output re-



PROGRAM INSTRUCTIONS

Description	Mnemonic Codes	Operation
Select channel to be digitized and set load to logic high	LR A, 5 AI 08 OUTS 1	Enter subroutine. Read address of channel to be interrogated from scratch-pad location 5 into accumulator. Add accumulator with 000010000. Load contents of accumulator into I/O port 1.
Trigger MN7100 to read and convert selected channel	AI 80 OUTS 1 CLR OUTS 1	Add accumulator with 1000 0000. Load accumulator into I/O port 1. Clear accumulator. Load accumulator into I/O port 1.
During conversion period	POP	Return to main program. Receive interrupt from end-of-conversion signal.
Read and store digitized data	INS 0 LR 3, A	Read digitized data form I/O port 0 into accumulator. Store data from accumulator in scratch-pad location 3.
Read and store channel address	INS 1 NI 70 LR 4, A	Read port 1 into accumulator. AND with 0111000. Load accumulator in scratch-pad location 4.
Process digitized data	POP	Return to main program.

3. Microprocessor hookup. Connecting the MN7100 to microprocessor chip sets is easy—especially if the set, like the one here, has a bidirectional I/O port that can be dedicated to a data-acquisition system. Program instructions for the device also are simple

turns to logic high, switching the sample-and-hold amplifier from track to hold mode, resetting the a-d converter, and restarting the system clock. The rising edge of the first clock pulse then starts the data-conversion process.

The internal system clock uses the other half of the dual monostable multivibrator, wired to operate in the self-retriggered mode. The user can vary clock frequency, which is normally 1.5 megahertz, with an external resistor or capacitor. The internal clock may be forced into synchronization with an external clock by using the package pin provided.

With the internal 1.5-MHz clock, conversion time for the full 8 bits is on the order of 5μs, with linearity of better than ±½ least significant bit. The a-d converter provides the digital output in eight parallel lines.

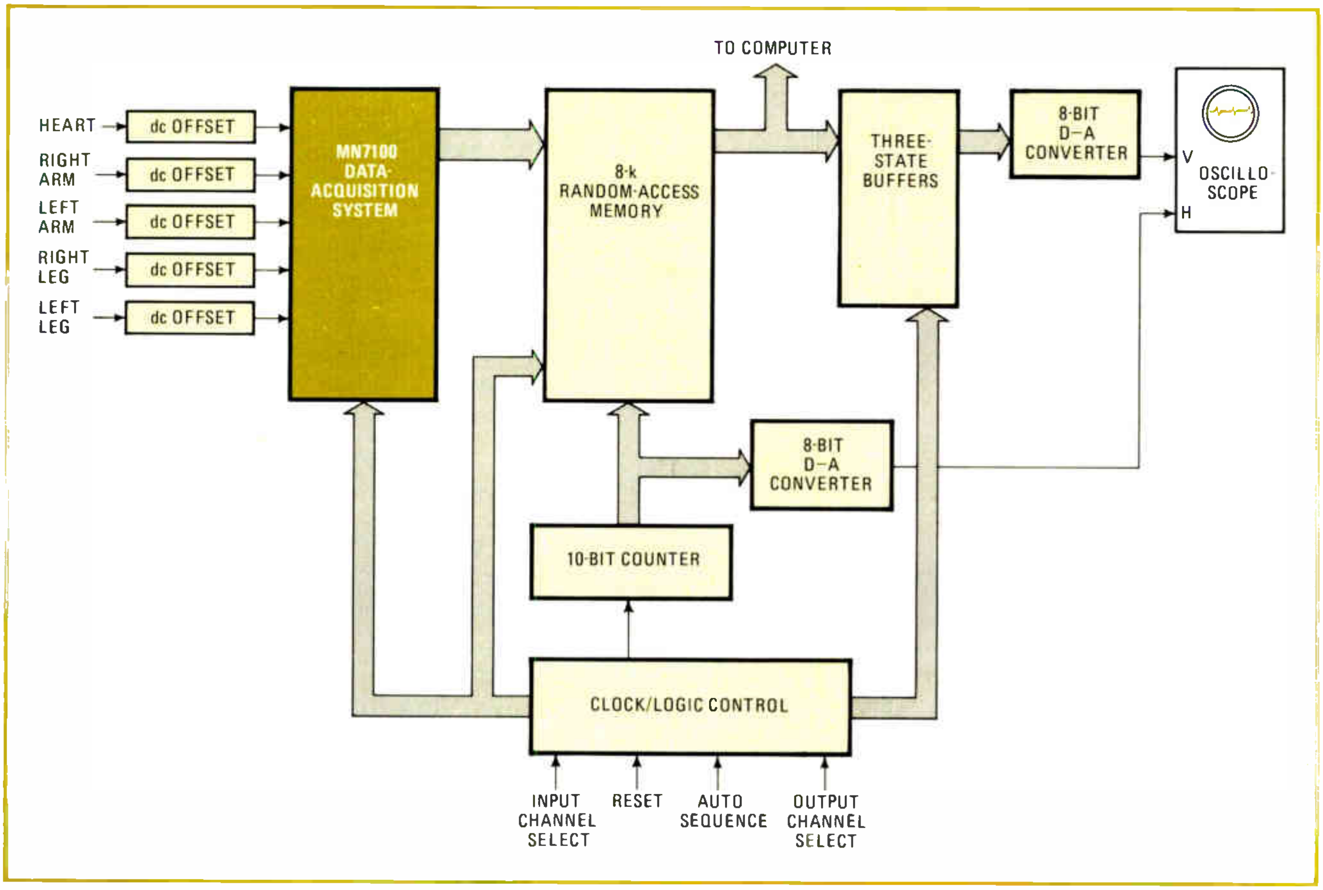
Where errors come from

In any data-acquisition system, there are several sources of error. For example, the multiplexer has three potential error contributions: crosstalk between channels, leakage to ground or the positive power-supply line, and the series on-resistance of the analog switches. With the multiplexer selected for the MN7100, none of these errors is significant, and the total effect on system accuracy is less than 0.006%. Also, unlike other multiplexers, this one is free of latch-up problems and is protected against input overvoltages.

Gain variation, feedthrough, droop (discharge of the holding capacitor), bias currents loading the multiplexer switches, and input offsets are the factors that contribute to error in the sample-and-hold amplifier. Of these, the principal factor in the MN7100 is input offset, which is minimized through functional laser trimming, so that the total error is less than 0.1%.

In the converter section, possible error sources include the d-a converter, the scaling resistors, the comparator, and the zener reference. All are negligible except for that of the zener, whose error is trimmed out at room temperature. It only contributes significantly with changes in temperature.

However, the total zener variation with temperature



4. Waveform analysis. With the MN7100, digital techniques can be used to analyze and display analog waveforms. In this biomedical application, various points of the body are being monitored and displayed on the oscilloscope to ascertain variations in the heart muscles.

is less than 100 parts per million per degree celsius. Other sections of the device are temperature-dependent to a lesser extent—the d-a converter drifts less than 50 ppm/°C, the comparator less than 30 ppm/°C, and the sample-and-hold amplifier less than 20 ppm/°C.

When choosing a data-acquisition system, the designer has several choices to satisfy the needs of a particular application. Depending on linearity, speed, and resolution requirements, he or she can select from a number of card-based units, hand-sized modules, or the DIP-housed hybrid MN7100. The other alternative is to design and build a system from discrete components.

Assembled units vs in-house designs

But in-house assembly is probably the worst choice, unless extremely large volumes are contemplated and the designer has considerable experience with data-acquisition systems. The pitfalls of purchasing and carrying in inventory 20 to 25 different types of components, the cost of testing and calibration fixtures, the inevitable expense of board repair, and the possibility of design oversights will all take their tolls.

On the other hand, the choice of an assembled pc-board or modular unit is far more convenient. The buyer is not only relieved of purchasing and stocking components but is also generally getting a reasonable design with the bugs already removed. The disadvantages associated with both card and modular units are the board space consumed, the relatively high cost and the field adjustments needed because of long-term drift or when replacing units.

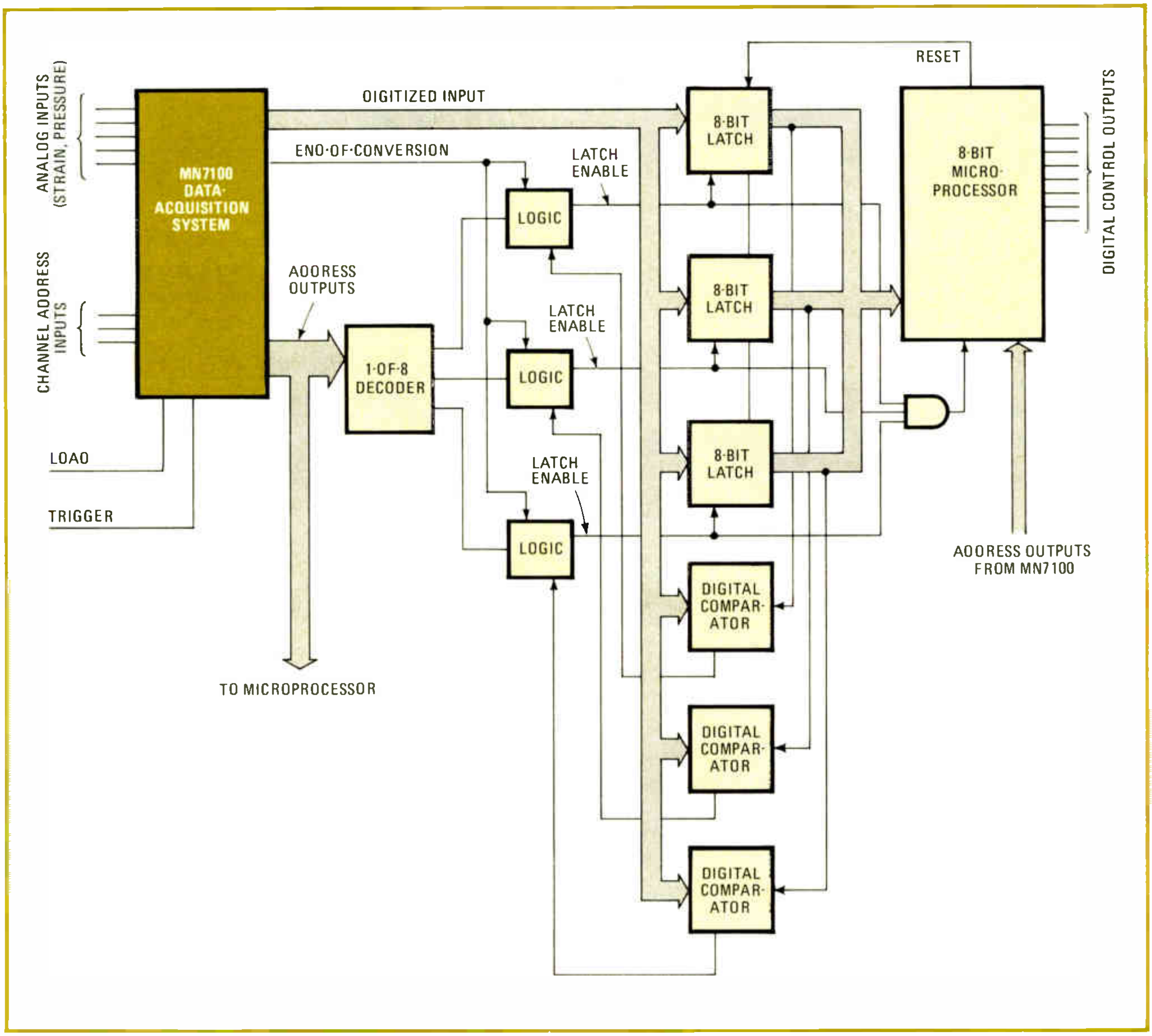
Interfacing with microprocessors

As mentioned, the MN7100 is compatible with popular microprocessor chip sets. Figure 3 illustrates how easily it can be interfaced with one such family, Fairchild's F8 chip set, which includes the 3850 central-processing unit and the 3851 program-storage unit.

Unlike some other microprocessors, the F8 system has multiple bidirectional I/O ports, so that additional latches or three-state buffers are not needed to interface with the data-acquisition system. However, if the microprocessor selected does not provide an I/O port that can be dedicated to the data-acquisition system, three-state buffers must be added.

In the example of Fig. 3, the CPU sends the address of the selected channel to the MN7100, which then interrogates and digitizes that channel. The CPU reads the digitized data, as well as the channel-address number, and stores them in its scratch-pad memory for further processing.

With or without an associated microprocessor, the possible applications for the device are numerous. Nowadays, even analog data is almost always processed digitally because digital computational circuitry has developed to a much higher level of sophistication than its analog counterpart. Furthermore, digital processing is many times faster than analog, and digital circuit blocks



5. Searching for peaks. The highest signal values are often of interest, particularly in noise studies and in machine-tool control when peak applied forces must be limited. The MN7100 permits digital signal comparisons, as part of microprocessor loop.

need not be calibrated periodically like analog ones.

Often, the same basic circuit technique can be used for a variety of different applications. For instance, the circuit of Fig. 4 is a multipurpose, real-time digital-analysis system for processing and displaying analog signals. Here, it is being used for a biomedical application—monitoring various points of the body to determine the variations in the action of the heart muscles. But it could also be used as an ignition system analyzer or to analyze other low-frequency analog waveforms.

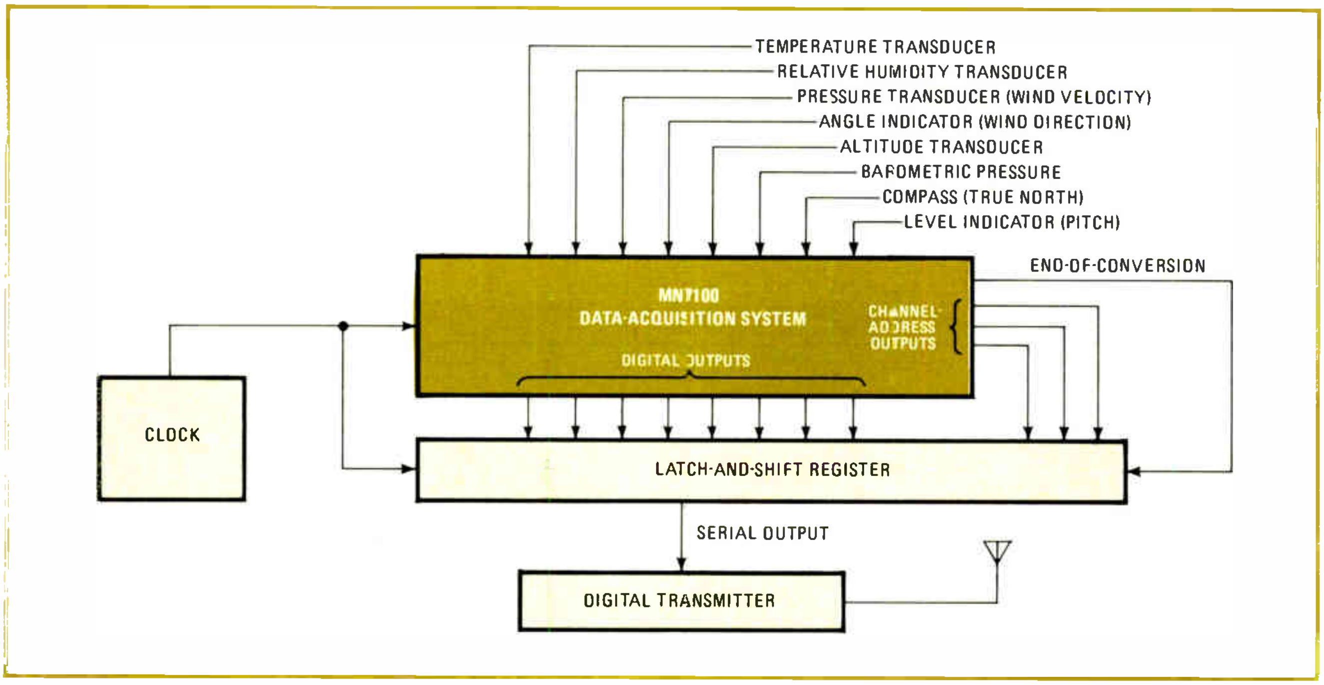
Analyzing analog waveforms

No matter the application, such a digital analysis system must have the ability to freeze an analog input at a number of arbitrary positions, hold that information without degradation, and store it in memory. After retrieval of the information, the necessary digital manipulations can be performed to obtain the desired answer and display it on the oscilloscope.

With the MN7100, it's possible to build this system on a single pc board measuring only 4 by 6 inches, at a cost of about $250 excluding the scope. If the system were put together from discrete components, another board would be needed just for the data-acquisition section, and costs would increase 200% or more, depending on how expensive design time and testing become.

The circuit operation of this waveform analysis system is straightforward. When the system receives a reset command or when power is first applied, a slow clock pulse (about 0.05 hertz) activates the data-acquisition system and updates the counter. The digitized analog inputs are then stored in the memory, which has eight sections, each of which is capable of holding 1,000 bits.

When the memory is full, the logic-control circuit initiates a command that increases the clock frequency (say, to 10 kilohertz) and switches the memory from write mode to read mode. The counter now drives both the memory and the d-a converter, whose output is ap-



6. Digital transmission. Data is frequently sent in digital rather than analog, form to take advantage of faster speeds and simpler systems designs. Here, on board a weather balloon, the MN7100 translates atmospheric and position information to a digital transmitter.

plied to the horizontal channel of the scope, so that the memory-clock rate and the horizontal-sweep rate of the scope are the same.

The displayed outputs can be examined visually and easily compared. The system also provides a computer access for more extensive waveform analysis than is possible visually. Through mode selection, the memory can be placed in its read-only state, displaying the output waveform repetitively for detailed visual analysis.

In this circuit, a dc-offset stage has been added to permit adjustment of the position of the vertical output on the scope. Three-state buffers simplify data distribution, minimizing the number of d-a converters needed to drive the scope.

Detecting peak values

Another application for the MN7100 is illustrated in Fig. 5, which shows the device as part of a multichannel, peak-value detection system. Although this particular system is intended for machine-tool control, such a setup can be used for such tasks as analyzing noisy signals to find the peak values of the system parameters.

Machine-tool control is an important part of stamping or forging operations used to produce bolts, nuts, cooking ware, flashlight battery cases, bullets, and the like. In these operations, large amounts of force are applied momentarily. To increase tool-bit life and thereby keep fabrication costs down, manufacturers often monitor the peak value of the applied force so as to limit it. Since the stamping is usually in several sequential steps, with different tool bits in many planes, the outputs of several strain gages, pressure transducers, or both must be monitored.

The circuit operates in a random or sequential channel-address mode, which is controlled by the status of the MN7100's load input. Initially, the three 8-bit latches are reset to zero, and the desired channel selected. The device then samples, holds, and encodes the addressed analog channel. When the end-of-conversion signal from the device goes low, the digitized input is compared with the signals stored in the latches. The outputs of the digital comparators are then gated by means of the logic blocks with the decoded channel-address outputs from the 1-of-8 decoder.

If the digitized input is greater than its corresponding stored signal, the appropriate latch will be strobed, and the new peak value will be transferred. No strobe pulse is generated when the digitized input is less than the stored signal. The outputs of the latches, therefore, indicate the highest peak values that occurred for a given time period. These latch outputs can now be fed to the minicomputer or microprocessor controlling the stamping operation.

Watching the weather

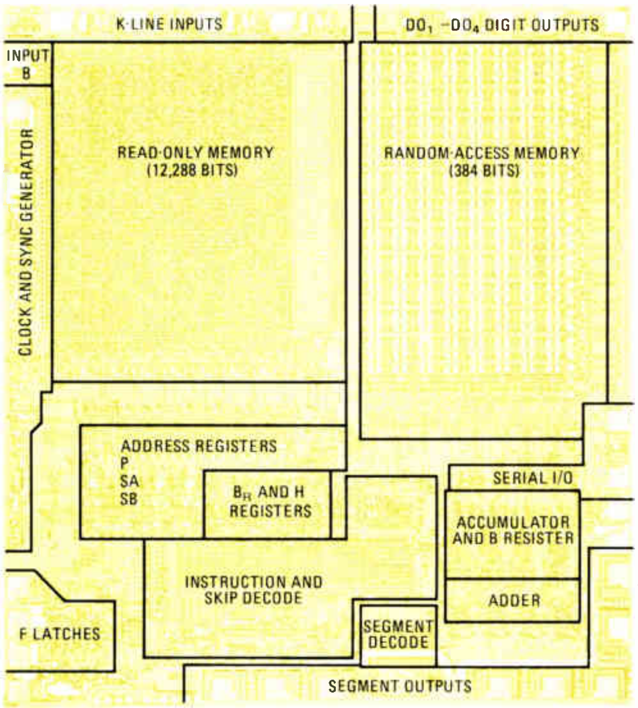
Because of its compactness, the device lends itself to applications where size and weight are major considerations. Moreover, since it is hermetically sealed, it can withstand fairly hostile environments. An application that takes advantage of both attributes is digital transmission of weather data from a balloon.

As shown in Fig. 6, such parameters as wind velocity and direction, air temperature and humidity, altitude, and atmospheric pressure are sensed by transducers and digitized by the MN7100. The parallel digital signal outputs, as well as the channel-address outputs, then go to the latch-and-shift register for conversion to serial format. This serial signal next goes to the digital transmitter for relay to a ground station. Since the channel-address data is included in the information supplied to the shift register, the transmitted weather data can be fully identified. □

Processor family specializes in dedicated control

Just one or two chips contain all the microcontroller elements needed in low-speed, high-volume applications like appliances or credit checkers

by Alan Weissberger, Jack Irwin, and Soo Nam Kim,
National Semiconductor Corp., Santa Clara, Calif.



1. Calculator-derived processor. Part of a new family of dedicated microcontrollers is the MM5799 programable calculator chip. Designed for quick-turnaround applications, it contains all system timing, arithmetic and logic, control-ROM, and RAM functions.

□ The designer of small, dedicated control systems, who otherwise would like to use an LSI design and save his company some money, often finds general-purpose microprocessors too powerful for his needs and the development of custom devices too drawn out. It's for his relatively low-speed, high-volume, quick-turnaround needs that a new family of dedicated microcontroller chips has been designed.

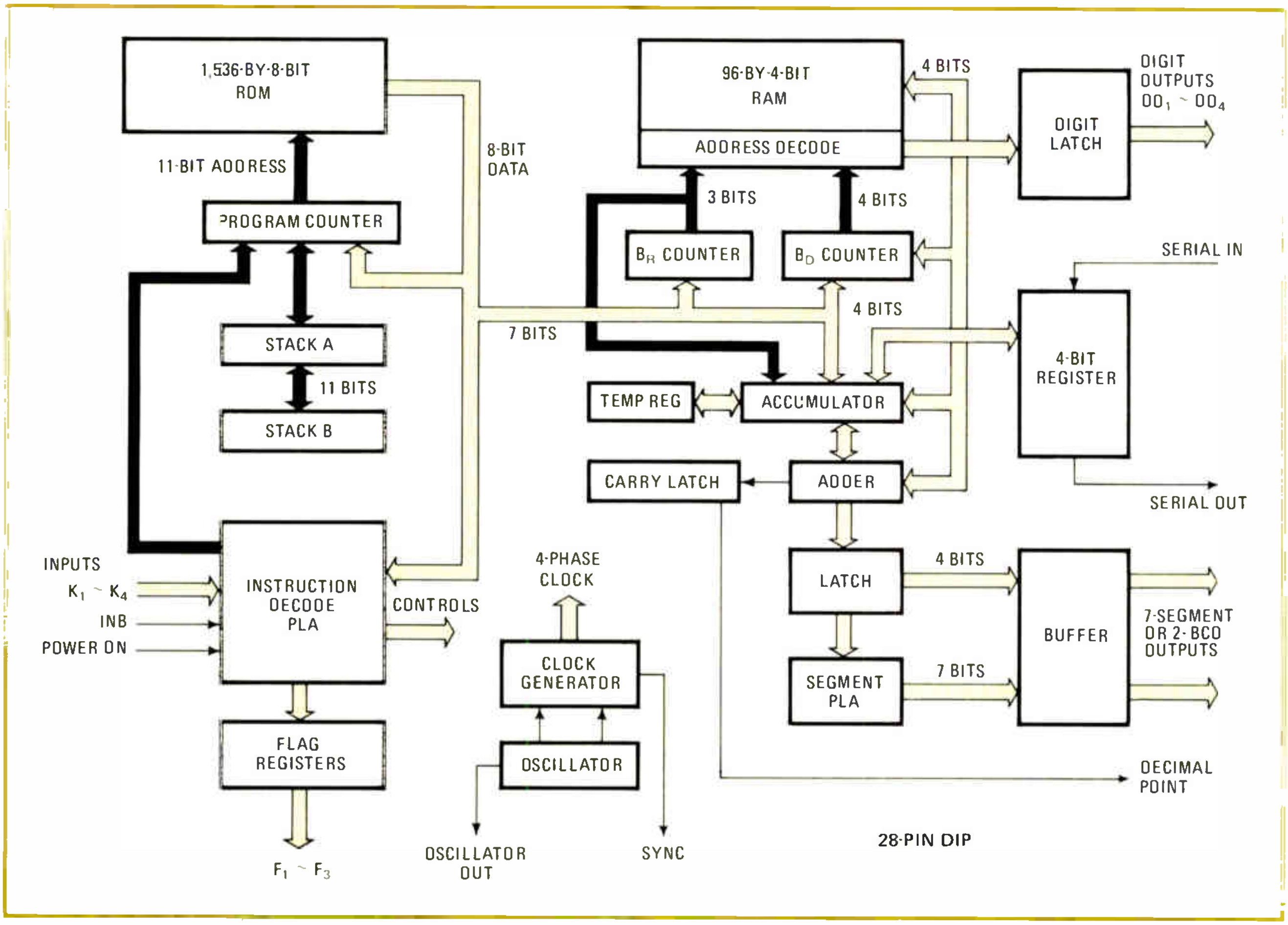
Fabricated from tried-and-true p-channel metal-oxide-semiconductor technology, they have an instruction time of 10 microseconds and can operate from a single 9-volt voltage supply. More important, they contain all that is necessary for most dedicated controls: clock generator, central processing unit, read-only and random-access memories, parallel inputs and programable outputs, plus a variety of single-bit input/output ports all under program control. In fact, they can by themselves take direct control of keyboards, displays, analog-to-digital and digital-to-analog converters, motors, valves, relays, and similar devices. Yet they cost less than $10 apiece in good volume.

With this family, it's possible for the first time to substitute a large-scale integrated circuit for the relays, springs, gears, and timers usually used in low-cost dedicated control systems. A general-purpose microprocessor would be uneconomical for these applications, since it would represent only a very small fraction of the total solid-state cost by the time all the necessary interface circuits, bus controllers, clock generators, ROM, and RAM had been selected and mounted and interconnected on a printed-circuit board. On the other hand, a custom LSI part needs high production volume to justify its development costs, and even then, the long lead time, lack of flexibility, test development problems, and loss of control of proprietary designs are deterrents in today's highly competitive markets.

But with the microcontroller chip, all kinds of dedicated control jobs can be done quickly and cheaply. Appliance controllers, smart instruments, remote sensing equipment, dedicated process controllers, gas pumps, frequency tuners, telephone dialers, automatic scales, line-printer controllers, credit checkers, vending machines all fall within its capability. Moreover, low-power, portable or battery backup systems will also find the microcontroller chips extremely attractive, owing to their single-voltage operation, very low power dissipation (120 milliwatts), and compatibility with complementary-MOS logic.

A different architecture

A typical member of the family is the MM5799 microcontroller (Fig. 1). Because the single chip contains all the elements of a little computer system—arithmetic/logic unit, ROM, RAM, and I/O circuitry—its architecture is radically different from that of general-purpose microprocessors. The functional elements of the chip are arranged in two groups: control ROM and processor (Fig. 2). The data inputs, ROM instruction store, and control logic are clustered on the left; the outputs, RAM data store, and arithmetic/logic unit are on the right. The ROM holds 1,536 8-bit instructions, while the RAM accommodates 96 digits of 4 bits each.



2. Clusters. Functions of the MM5799 fall into two groups, with control-ROM-related functions shown on the left and RAM-related functions on the right. Each memory has a separate data bus and address bus—a major departure from conventional microprocessor architecture.

Each memory maintains a separate address control register, address bus, and data bus—a major departure from the design of a general-purpose microprocessor, in which a common bus serves as the address control for accessing both ROM and RAM. In the microcontroller, however, the duplication of buses and registers conserves on-chip ROM space by eliminating the need to specify the RAM data address for each instruction. Moreover, since the RAM is configured as a matrix, with address control consisting of register and digit coordinates (B_R and B_D counters), access to on-chip data requires no additional peripheral address circuits. Automatic increment/decrement memory operations provide efficient string data processing.

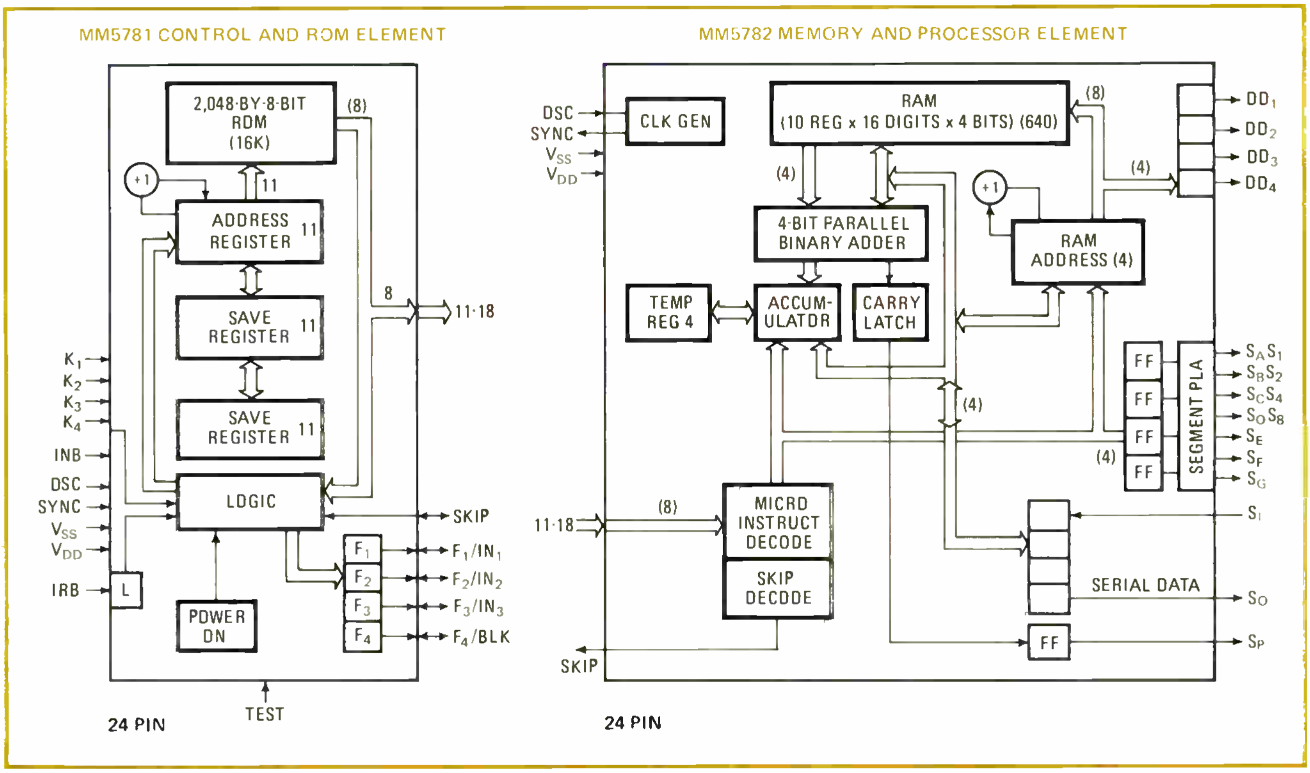
Besides the RAM for data storage, the processor section contains the RAM address register, address decode logic, an accumulator, a temporary register for intermediate results, an adder and carry latch, and a programable logic array for converting binary-coded-decimal inputs to 7-segment outputs. Eight parallel latched outputs are available as binary, BCD, or as a seven-segment-plus-decimal-point output that is kept under program control.

The decimal-point output may also be used by the programer as a general-purpose flag. On-chip buffers enable the eight outputs to drive light-emitting-diode displays directly. Alternatively, the 4-digit line outputs (DO_1–DO_4) may be used with external decoder/driver buffers to switch digits in a multiplexed display, or to drive scan keyboards, or to specify a 4-bit address for up to 16 input or output devices, or to output 4-bit data to any of eight devices without external decoding.

A 4-bit shift register, together with serial input and serial output ports, provides a serial I/O facility for expanding the data-storage capacity of the chip or for in-

TABLE 1: COMPARISON OF THREE PROCESSORS

	MM5781/82	MM5799	MM5734
ROM bit size	2-k x 8	1.5-k x 8	630 x 8
RAM bit size	160 x 4	96 x 4	55 x 4
ROM expandability	Up to 8-k x 8	No	No
RAM expandability	Yes – 4-k +	Yes	No
Cycle time	10 μs	10 μs	14 μs
Flag outputs	3	3	1
Sense inputs	K_1 ~ K_4, Inb, irb	K_1 ~ K_4, Inb	K_1 ~ K_4, Inb
Temporary register	Yes	Yes	No
Single supply operation	7.9 V ~ 9.5 V	7.9 V ~ 9.5 V	7.9 V ~ 9.5 V
Supply current	81 – 7 mA, 82 – 15 mA	17 mA Typ	14 mA Typ
Oscillator	Ext	Int, ext	Int, ext
Keyboard interface	Direct	Direct	Direct
Serial input/output	Yes	Yes	No
Digit output	4 bit	4 bit	9 line decoded
Display drive digit	Needs decoder-driver	Needs decoder-driver	Direct drive
Segment output	BCD or 7 seg + DP	BCD or 7 seg + DP	BCD or 7 seg + DP
Display drive for segment	Needs driver	Direct drive	Direct drive



3. Added power. Two-chip microcontroller carries more internal ROM and RAM capacity than one-chip versions, making more powerful control systems possible. Program storage and control fit on the MM5781 program chip, with processing and RAM storage on the MM5782.

terfacing it with a variety of peripheral chips in larger, memory-rich systems. The serial input and output ports may also be used for detecting or generating pulse-train signals, a feature that is valuable in many instrumentation systems. In these cases, the sync control synchronizes external logic by serving as a timing pulse output, occurring once per instruction.

In the control-ROM section, in addition to the ROM, there are four parallel inputs, a testable sense input, three bidirectional control flags (F_1–F_3) for use as inputs or outputs, a program counter, a two-word stack for nested subroutine calls, and an instruction-decode programable logic array. Finally, there's an external oscillator as an optional input for clocking systems containing more than one controller chip.

And, for more powerful systems, a two-chip set, the MM5781 and MM5782, carries more internal ROM and RAM (Fig. 3). The 5781 program chip contains the con-

Why the microcontroller?

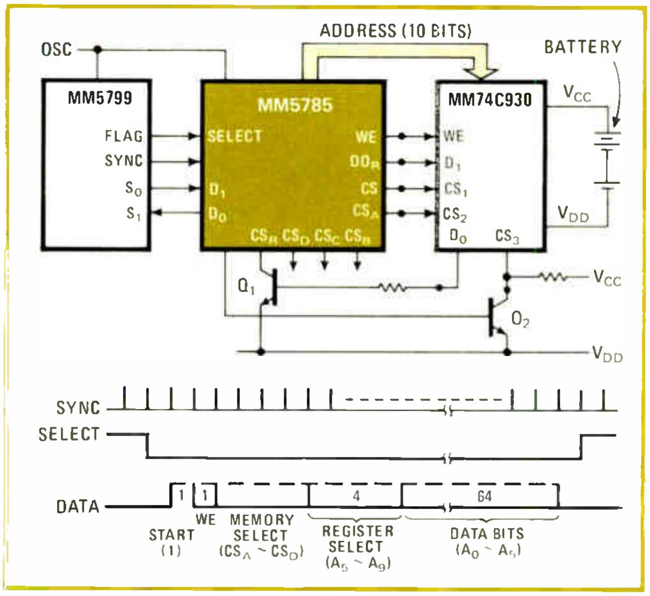
Requiring fewer components at the system level, the dedicated microcontroller offers several advantages over general-purpose microprocessors. It:

- Reduces the cost and complexity of hardware by providing ROM, RAM, clock generation, and I/O circuits on chip. Costs of chassis, wiring, and power supplies are similarly reduced.
- Improves reliability and noise sensitivity by making interconnections internal.
- Simplifies incoming inspection and test because fewer parts are involved. System testing also becomes less expensive for the same reason.
- Provides a low-cost man-machine interface by controlling keyboards and displays directly, without the help of external components.

The accompanying table compares system parameters for microcontrollers, microprocessors, and custom LSI approaches. System design with microcontrollers is less costly than with microprocessors, even though chip development time and costs are slightly higher. This is because with the microcontroller the ROM control program resides on the chip, and the designer must totally debug his program before committing to a ROM mask pattern. However, tighter design rules may produce a better end product.

Another effect of the microcontroller's on-chip ROM is that a fairly high product volume is necessary to justify the mask tooling charges for the custom ROM program. For this reason the microcontroller chips will be most effective in low-cost high-volume applications.

	General-purpose microprocessor	Custom LSI	Calculator-oriented processor
Development time	Short	Long	Short + 1 month
Development cost	Low	High	$600 more
System cost	High	Low	Low
System component count	Large	Small	Small
Flexibility	Good	Poor	Pretty good
System testing	High	High	Low



4. **Expansion.** Although designed to be self-contained, the controllers can be expanded by being linked to standard 1,024-bit RAMs through the MM5785 RAM interface elements. Schematic and timing diagram show how this works for the MM5799 controller.

TABLE 2: MICROCONTROLLER SUPPORT CHIPS	
MM5785	RAM interface to MM5782, MM5799 interfaces up to 4 MM74C930-type RAMs directly.
MM5788	Printer interface to MM5782, MM5799 interfaces to Seiko printers with up to 20 column outputs.
MM2102	1,024-by-1-bit n-MOS RAM.
MM74C930	1,024-by-1-bit C-MOS RAM.
DS8863	MOS to 8-LED digit driver, 500-mA sink, open collector output.
DS8664	4-bit decoder-driver, 14 digit outputs, 80-mA sink, open-collector output, built-in oscillator, low battery sense, blank output.
DS8665	Same as DS8664 except emitter-follower output, 8 mA source (to be used with DS8692).
DS8666	Same as DS8664 except 8 outputs are emitter followers and 6 outputs are open collectors.
DS8692	8-npn-transistor array, 350-mA sink.
DS8874	2-input 9 output shift driver for low-cost calculator-display digit driver.

trol-ROM element, consisting of 2,048 or 4,096 bytes of ROM for program storage, the ROM address, control logic, and various input/output functions. The 5782 memory and processor element contains the arithmetic/logic unit, instruction-decode PLA, 160 by 4 bits of RAM for data storage, a RAM-address register, address and data outputs, and serial I/O ports. The amount of ROM storage can be expanded to 16,384 bytes by using four ROM chips.

On the other hand, for very simple systems, there is the lowest-cost processor chip, the MM5734. Here, ROM and RAM sizes are smaller (630 bytes and 55 by 4 bits respectively), yet the chip contains all the functions needed for many controller applications. Table 1 compares the three processor systems.

Expanding the system

Although these chips have been designed to operate as self-contained controllers, they can be used with standard memory to implement larger systems. For example, data storage can be expanded by adding standard 1,024-by-1-bit RAMs, together with the MM5785 RAM interface element. The serial input and output ports on the 5799 single-chip system or the 5782 part of the two-chip system are then used to transfer bit-serial data to and from the 5785.

Indeed, each MM5785 can interface directly with up to four 74C930 C-MOS RAMs or MM2102 static n-channel MOS RAMs. Here, by using the digit timing signals as chip-select inputs to the interface element, it's possible to accommodate 14 MM5785s per system (or over 14-k 4-bit bytes of data memory).

The schematic and timing diagram of Fig. 4 illustrates how RAM storage may be expanded for the 5799 controller chip. The 5785 RAM interface element and the 5799's serial input and output ports are used to transfer bit-serial data. One to four 1,024-by-1-bit RAMs (74C930 or 2102) may be directly interfaced to the 5785.

The 74C930 C-MOS RAM is shown in the figure. Up to 16 RAMs may be interfaced, requiring only that the chip select outputs are decided by a 4:16 decoder.

To start a data transfer, the selected input of the 5785 must first be enabled. Any decoded digit output available may be used. Once the chip is enabled, it expects 10 consecutive control bits, followed by 64 data bits. A bit is transferred to or from the 5799 controller in its cycle time of 10 microseconds.

The 10 control bits consist of 1 start bit, 1 write-enable, 4 memory-select, and 4 register-address bits. Four bits specify the 1 to 16 registers that are to be addressed. Data into the memory is directly output on the DO_R line. Data from the memory is inverted through transistor Q_1 and input to the CS_R terminal. An internal inversion occurs with the 5785 RAM interface to produce true data for the controller chip on the DO line.

When battery backup is used for the external RAM, as shown in the schematic, the output of the 5785 prevents RAM data destruction during system power up or down. The output signal, which turns on transistor Q_2, pulls the CS_3 input low, thus disabling the 74C930.

Besides the RAM interface element, the microcontroller chip family contains other support components (Table 2). The MM5788 printer-interface element, for instance, drives Seiko drum printers, while the various display decoder/drivers can satisfy the output requirements for most commonly configured controller applications and also provide an oscillator for systems requiring accurate timing signals.

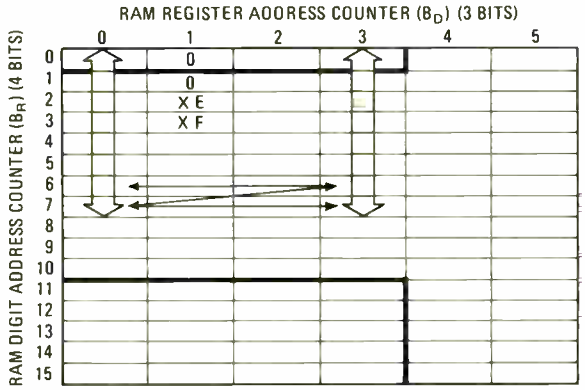
Help in programing

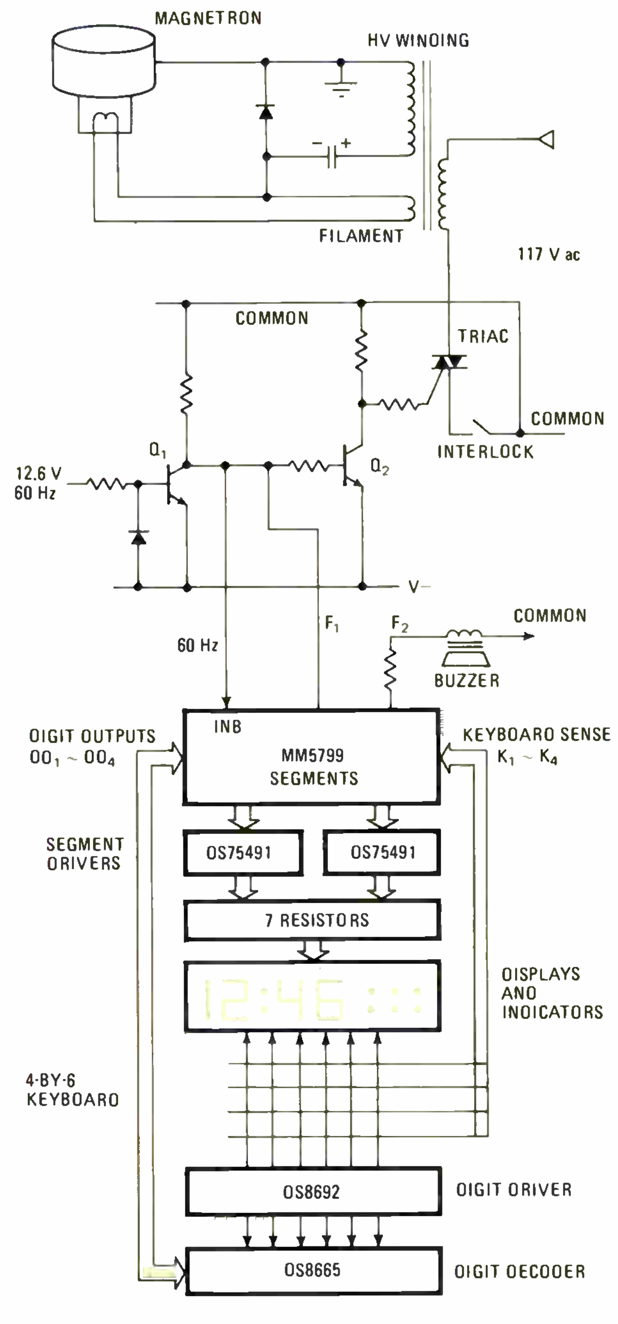
For users who need it, full software support is available, including an assembler, simulator, and sample program routines. (In review, the assembler converts the assembly-language or source code into machine code, which is then executed by the software simulator. Meanwhile, the simulator commands all of the control sequencing and display formatting. Also, the simulator controls the RAM output registers and provides snapshot

Programing the microcontroller

The separate ROM and RAM architecture of the microcontroller chips makes programing very efficient. Many instructions perform multiple operations. For example, instructions for manipulating data between RAM and accumulator also update the RAM address registers (B_R and B_D) and skip if the digit count has reached a specified value. Moreover, when RAM memory is accessed, no separate RAM addressing instructions are required, except at the beginning of the routine when the address registers are initialized by a single instruction. This feature permits efficient coding of program loops operating on data consisting of strings of digits.

A typical RAM memory map (for the MM5799) is shown in the accompanying figure. There are 96 digits, with 4 bits per digit. Separate RAM address registers B_R (3-bit) and B_D (4-bit), are used to address registers and digits respectively. This map is organized as 6 registers by 18 digits. A mask option will reconfigure the RAM's registers and digits to the user's specification. For example, the RAM might be configured as 10 registers by 10 digits with 4 digits available as miscellaneous flags.





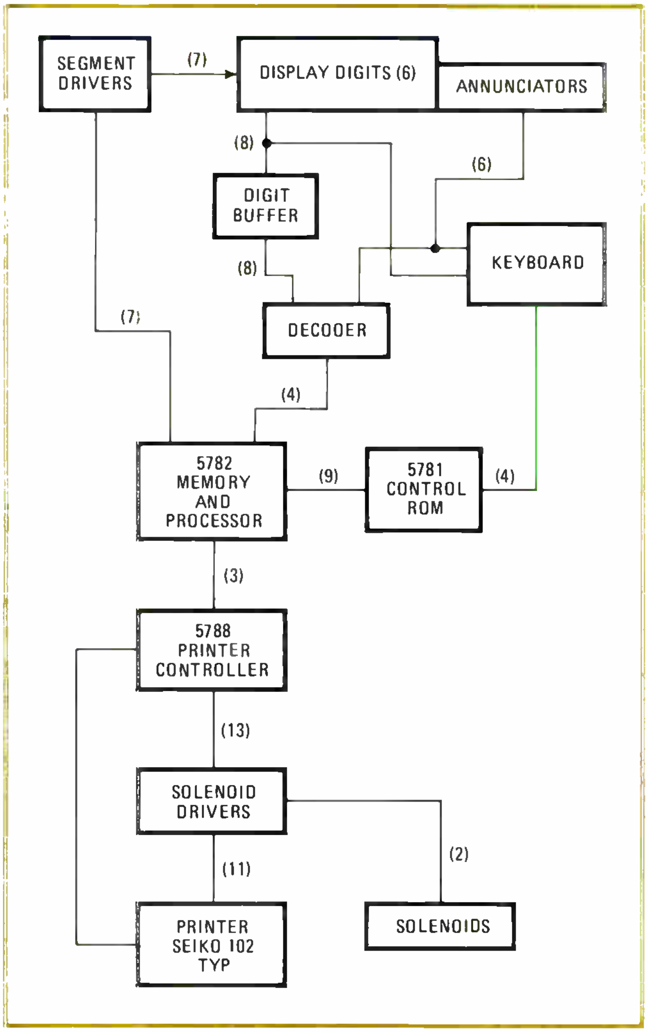
5. What's cooking? This microwave-oven controller shows the efficiency of design with a dedicated microcontroller. Relatively few components are needed to achieve, virtually automatically, all the timing and control functions involved in household cooking.

traces at key points within the program routine.)

For real-time checkout, an IMP-16P microprocessor prototype system can be used as an in-circuit emulator. A logic board containing the RAM data store reproduces the chip's control and timing functions and holds the sockets for the user's PROM program. A shared memory interface board is loaded and edited by the 16P and used as the program store for the chip being emulated. This gives the user a fast means of debugging his control program. He can alter the code through the IMP-16P front panel, set flag bits in the instruction memory to trigger an oscilloscope, dump and compare the contents of the edited and original instruction memory, print out an instruction sequence with a specified address range, or search for a particular instruction or bit pattern within the given address range. Indeed, the IMP-16P can even be used to program the PROMs that go onto the emulator board so that it can be placed in the actual system environment, thus freeing the 16P for other tasks.

To illustrate the efficiency of the microcontroller chips, members of National Semiconductor's digital-applications laboratory developed a microwave-oven controller around them. Defrosting and cooking time, temperature, and power duty cycles are controlled by the processor from a panel keyboard, while cooking status is shown by a LED display.

Operation is virtually automatic. The cook, having decided on a particular oven function, enters a four-digit number representing time and then punches a function key representing the intended operation. This activates the appropriate instructions—each function has its own four-digit register in the RAM. Moreover, if the cook depresses a function key without first entering



6. Cashing the chips. Only nine IC parts are required for an electronic-cash-register system with many desirable features for retail applications. With slight modification, the machine's six-digit LED display can be changed to a high-voltage gas-discharge display.

the digits, the contents of that particular function register are displayed. In the cooking mode, the remaining time and the particular cooking stage are displayed.

The system is shown in Fig. 5. It consists of the MM5799 processor chip, a bank of four LEDs, six indicator lamps, appropriate display drivers, a keyboard, power triac, and miscellaneous discrete components. The circuit drives the ½-in. LED displays and six indicator lamps. If 0.1-in. LED displays are acceptable, the chip can drive them directly, saving some money by eliminating the two DS5491 segment drivers and the DS8692 digit driver and in fact needing only a digit decoder/driver IC to make up a complete system.

The signal that drives the triac comes from one of the chip's flag outputs, F_1. When F_1 goes high, the triac's driver transistor D_2 turns on and pulls current from the gate of the triac. The triac turns on and provides power to the magnetron transformer. The magnetron is turned on and off at a specified duty cycle, which the cook can program into the system through the keyboard. When he or she selects the 50% duty cycle, for instance, the magnetron will turn on for 15 seconds and turn off for 15 seconds as program control raises and lowers F_1.

The 12.6-volt, 60-hertz signal is squared and driven to the sense input terminal to provide a time-base reference. The program senses a low-to-high transition to this input and then increments an internal RAM timer. This timer provides the time-base signals for all function counters and the real-time clock. It also acts as a reference frequency for display multiplexing and keyboard scanning.

To provide a flicker-free display and maintain timekeeping, the various real-time control functions in the main program are divided into small program segments with execution times of 1 to 2 milliseconds. The display is multiplexed, and the sense input is scanned in between these program segments. Digit and segment outputs are latched on the processor chip, so that they remain active and capable of driving the display during the execution of each program segment.

An electronic cash register

A natural application for the microcontroller chip is the cash register, where only nine ICs can implement a system (Fig. 6) that has myriad of features: nonresettable grand total (9 digits); five department totals (6 digits); charge; refund; received on account (cash in); paid out (cash out); tax computation and total; cash in drawer; receipt of journal tape; customer count (3 digits); multiplication; void and clear for entry errors; read and reset (X and Z), and date with month, day, and year.

The cash register's display has six digits for all working registers. This is enough for most cash-register transactions, with some margin for inflation over the useful life of the machine. While a fixed decimal point is assumed for U.S. operations, it could be left off for certain foreign applications. In fact, the machine covers the equivalent of a several-thousand-dollar purchase in most monetary systems.

The display in Fig. 6 uses 0.6-inch LED digits, but a high-voltage gas-discharge display could also be accommodated if the high-current LED drivers were exchanged for their high-voltage equivalents. For annunciator indication of various machine conditions, such as change due, entry, tax, and so on, a pair of LED lamps in series backlights each legend.

Data processing takes three chips plus six drivers (again, see Fig. 6). The three chips are the MM5782 memory and processor element, the MM5781 program control element, and the MM5788 printer interface.

Since the large 0.6-in.-LED digits require more current drive than standard decoder chips, a high-current DS8666 has been chosen to provide it and also to perform the oscillator/decoder function. Segment drive is provided by the 75491s. And DM8863s are used to provide hammer and solenoid drive from the printer-interface chip.

The layout for the cash-register system demonstrates two methods for displaying data output. For numeric value, six digits are provided by using internal seven-segment encode. For binary memory-value outputs, eight digit positions are available, and any combination of 32 (8-by-4) lamps may be activated. □

TTL decade counter divides pulse train by any integer

by T. Durgavich and D. Abrams
Abrams Associates, Arlington, Mass

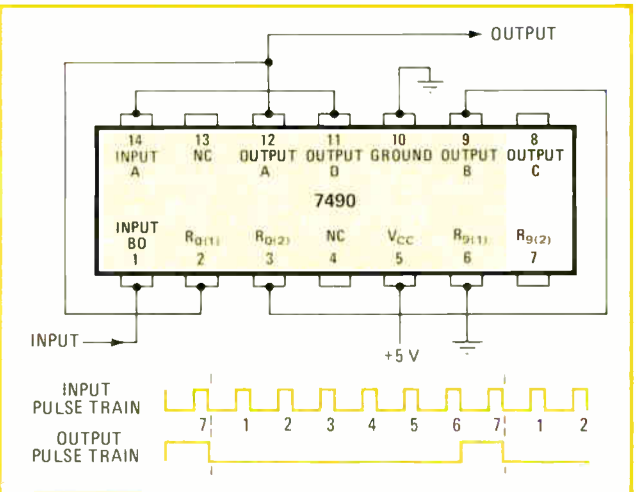
In many applications a pulse train must be divided by a fixed integer. For example, digital clocks often divide the line frequency by 60 to obtain a 1-hertz output, and time-base generators divide a crystal oscillator frequency down to several stable low-frequency outputs. If the integer is 10 or less, just one 7490 TTL decade-counter can handle the division.

Usually frequency division in TTL circuits is accomplished by using binary counters and logic gates. To divide by N—i.e., to get one output pulse for every N input pulses—the logic gates are connected so that the counter is reset when the N^{th} pulse is counted. The most significant bit is used as the output, because it makes the high-to-low clocking transition only once for every N input pulses. If it is necessary to have an output pulse of a specific length, then a monostable may be triggered when the N^{th} pulse is detected.

The disadvantage of this division technique is that, even for divisors less than 10, two ICs are required—a binary counter and a gate. But a pulse train can be divided by any integer between 2 and 10 by use of just one 7490 TTL decade-counter IC, owing partly to its divide-by-2 and divide-by-5 stages and partly to its internal ANDed reset, which lets it reset only when both pin 2 and pin 3 are high.

The counter can be made to reset on any count from 2 to 10 by appropriate connections of the pins. The necessary interconnections for each value of N are shown in the table.

For example, if division by 7 is desired, the 7490 is wired as shown in the figure. The input and output pulse trains for this configuration are also shown. If a larger division is required, it's only necessary to cascade several stages together, provided the divisor has factors that are all less than 10. □



Divide-by-7 circuit. A 7490 TTL decade-counter integrated circuit, when connected as shown here, produces one output pulse for every seven input pulses. Because the divide-by-2 stage follows the divide-by-5 stage, the seventh count is a non-BCD code and can be detected by the internal two-input NAND gate to reset the counter. Other connections permit division by any other integer up to 10.

OPERATION OF 7490 IC AS A DIVIDE-BY-N COUNTER

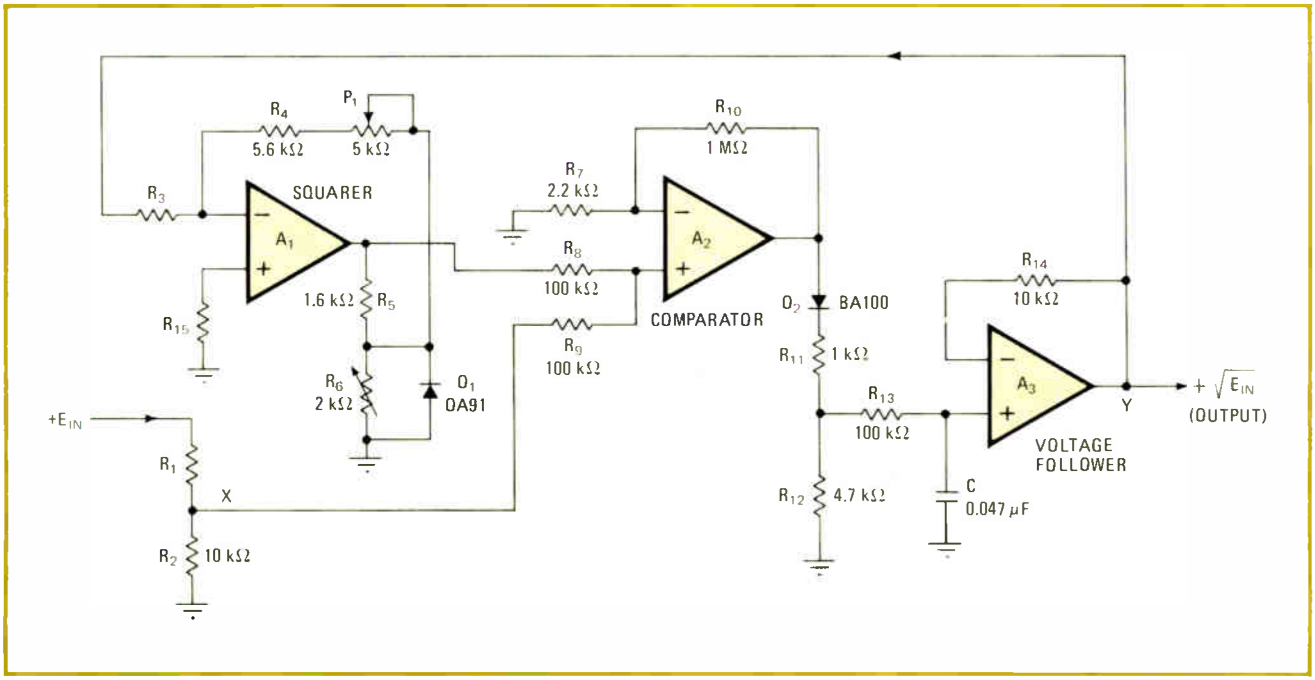
DIVISOR N	INPUT PIN NO.	OUTPUT PIN NO.	EXTERNAL CONNECTIONS
2	14	12	PIN 2 OR 3 LOW
3	1	8	PIN 8 TO PIN 2 PIN 9 TO PIN 3
4	1	8	PIN 11 TO PINS 2 AND 3
5	1	11	PIN 2 OR 3 LOW
6	14	8	PIN 12 TO PIN 1 PIN 9 TO PIN 2 PIN 8 TO PIN 3
7	1	12	PIN 11 TO PIN 14 PIN 12 TO PIN 2 PIN 9 TO PIN 3
8	14	8	PIN 12 TO PIN 1 PIN 11 TO PINS 2 AND 3
9	14	11	PIN 12 TO PINS 1 AND 2 PIN 11 TO PIN 3
10	14	11	PIN 12 TO PIN 1 PIN 2 OR 3 LOW

Analog square-root circuit handles wide input range

by W.V. Dromgoole
Christchurch, New Zealand

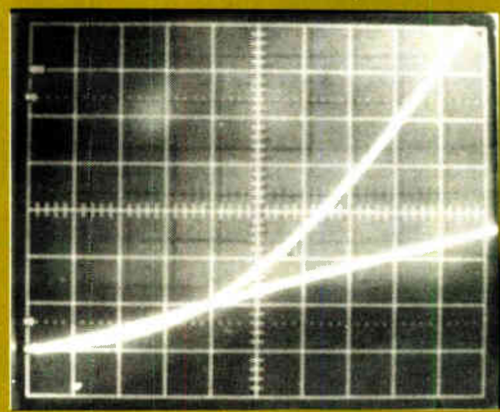
A square-root circuit is frequently needed for linearizing the output from transducers that have a square-law response. It also finds many applications in analog computations. The design described here produces a square root with accuracy within 1% for input voltages in the range from 0 to + 100 volts.

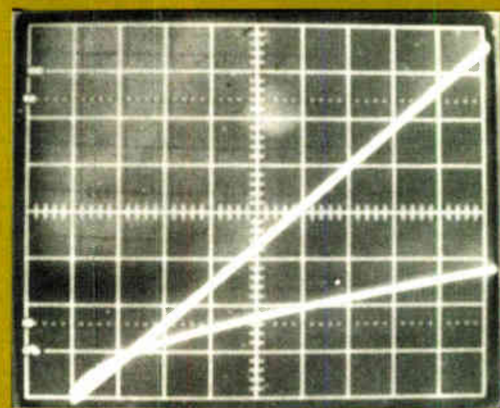
As shown in Fig. 1, the circuit has three operational-amplifier stages: a squarer using op amp A_1, a compara-



1. Getting to the root. Output from three-op-amp circuit is square root of input. Comparator A_2 balances input with square of output to produce the root. Accuracy within 1% is achieved through good square-law characteristic of diode D_1 in feedback loop of squarer A_1, plus adjustment of scaling and tracking controls P_1 and R_6. Voltage follower A_3 buffers voltage across capacitor.

2. Two views of operation. In (a) the upper trace is a square-law input, and the lower trace is the linear output from the circuit of Fig. 1. In (b) the upper trace is a linear input, and the lower trace is the square-root output. Crossovers in photos occur at input of 1 volt.


(a)


(b)

tor using op amp A_2, and a voltage follower using op amp A_3. It operates by comparing the scaled input voltage to the square of the voltage that is fed back from the output of the circuit. When the two are equal, the output voltage must be the root of the input.

The positive input voltage at point X is applied to the noninverting terminal of the comparator through resistor R_9. The comparator's output goes positive and charges the capacitor C; the capacitor voltage is buffered by the voltage follower and applied to the inverting input of the squarer by means of the scaling resistor R_3.

Because of the approximate square-law characteristics of diode D_1 (modified in curvature by R_6) in the feedback loop of the squarer, the output from A_1 is the square of the voltage at its inverting input; it is negative because of the inversion. This negative output drives the noninverting input of the comparator through R_8. When the magnitude of this voltage equals that from point X, the comparator output goes negative, and C discharges through R_{13} and R_{12}. (The function of diode D_2 is to prevent the comparator from putting negative charge on C.)

Thus the comparator automatically modifies the voltage on C to maintain the output of the follower and the input to the squarer at $+V_{IN}^{1/2}$ (Fig. 2). It is connected as a noninverting high-gain amplifier that responds to voltage changes very rapidly without producing any sawtooth components at the output. Swept voltage tests made with an oscilloscope show that the response time of the comparator is less than 10 milliseconds and is free of jitter.

The circuit may be set up for any $V_{IN(MAX)}$ from 10 to 100 volts by adjusting resistor R_1 so that the maximum voltage at point X is 10 V. Since R_2 is 10 kilohms, the value of R_1 in kilohms is ($V_{IN(MAX)}$ – 10). The value of R_3 in the squarer circuit is made 10 $V_{IN(MAX)}^{1/2}$ kilohms.

Typical values are:

$V_{IN(MAX)}$ (volts)	R_1 (kΩ)	R_3 (kΩ)
10	0	31.6
50	40	71
100	90	100

Potentiometer P_1 is adjusted to make the voltage at point Y exactly equal to $V_{IN(MAX)}^{1/2}$. Finally, resistor R_6 is trimmed to provide the best square-root tracking, P_1 being readjusted as R_6 is varied.

To minimize offset error, resistor R_{15} should be equal to the resistance of the combination of R_3 in parallel with R_4 and P_1. Since (R_4 + P_1) is much smaller than R_3 on any range, however, R_{15} may be made 6.8 kΩ as a good compromise. Diode D_1 should be chosen to have a resistance of about 160 Ω for an applied voltage of 0.8 V. The type 741 op amps use a ±15-V power supply, decoupled with 0.1-microfarad ceramic capacitors at the voltage-input points. □

Tail-biting one-shot keeps car-door light on

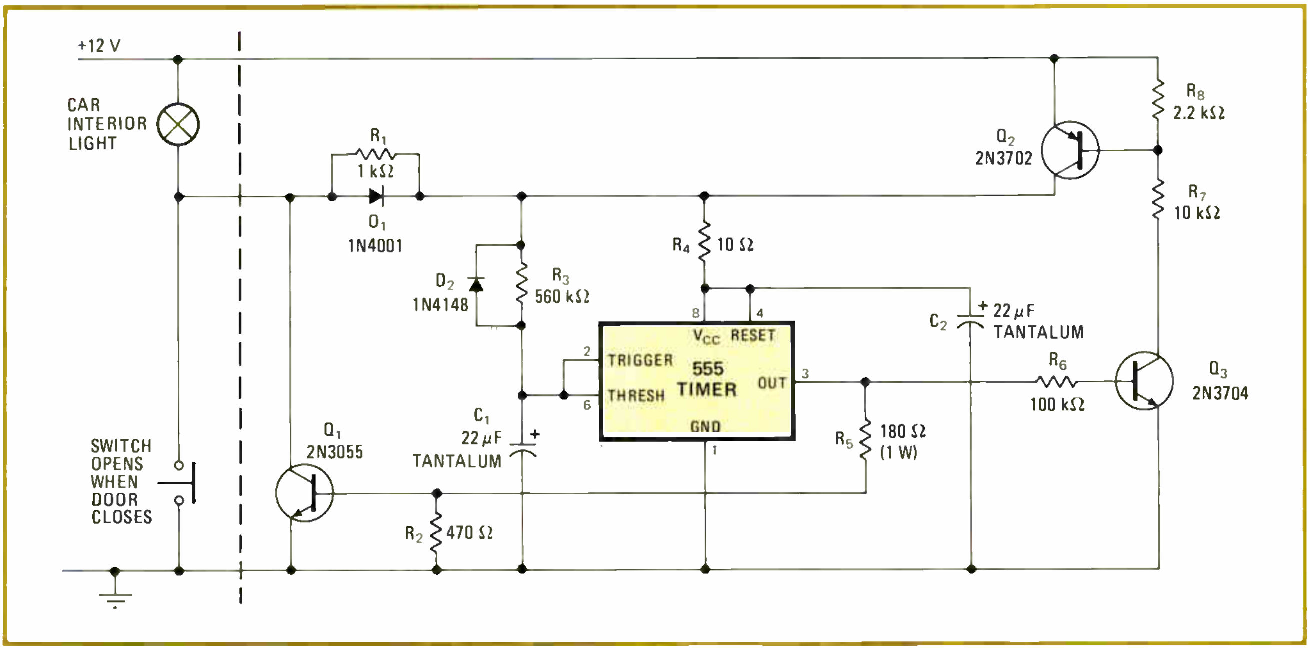
by B. D. Redmile
Salisbury, Rhodesia

A one-shot multivibrator that drives the same line it is sensing is useful for such applications as burglar alarms and switch-action delays because it can be fitted at any point in the circuit. Full reliability of the original circuit is retained, since connection of the one-shot across it does not break it. In the arrangement shown in the schematic, a 555 timer keeps the interior light of a car turned on for 10 seconds after the car doors are closed.

In the idle condition (door closed, light off), the 12-volt line charges capacitor C_1 and supplies power to the 555. The current drain is only about 10 milliamperes, so the light does not go on. The threshold terminal of the 555 is held high by R_3, so its output is low and all the rest of the circuit is off. When a door is opened, the light goes on in the usual way and the power to the one-shot is removed. Capacitor C_1 then discharges rapidly through D_2 and R_1.

When the door is closed and the lamp starts to turn off, power flows to the 555. With C_1 discharged, the threshold terminal is at low voltage, so the output goes high. This turns on transistors Q_1, Q_2, and Q_3. Q_2 maintains power to the 555 while Q_1 furnishes a path for current to flow to keep the light on. After a delay set by C_1 charging through R_3, the 555 output goes low, restoring the circuit to its idle state.

The combination of C_2 and R_4 prevents transients on the battery supply from damaging the 555 or prematurely terminating the one-shot high output pulse. □



Holds the light. When car door closes, output current pulse from 555 timer turns on transistor Q_1 to keep interior light on for about 10 seconds. This type of one-shot arrangement, driving the line that is sensed, can be added at any point in the circuit. It is useful in alarm systems, process controls, automatic machinery, safety circuits, and convenience circuits such as this one.

When programing microprocessors, use your hardware background

The analogies between hardware and software design procedures can be a guide through the programing maze

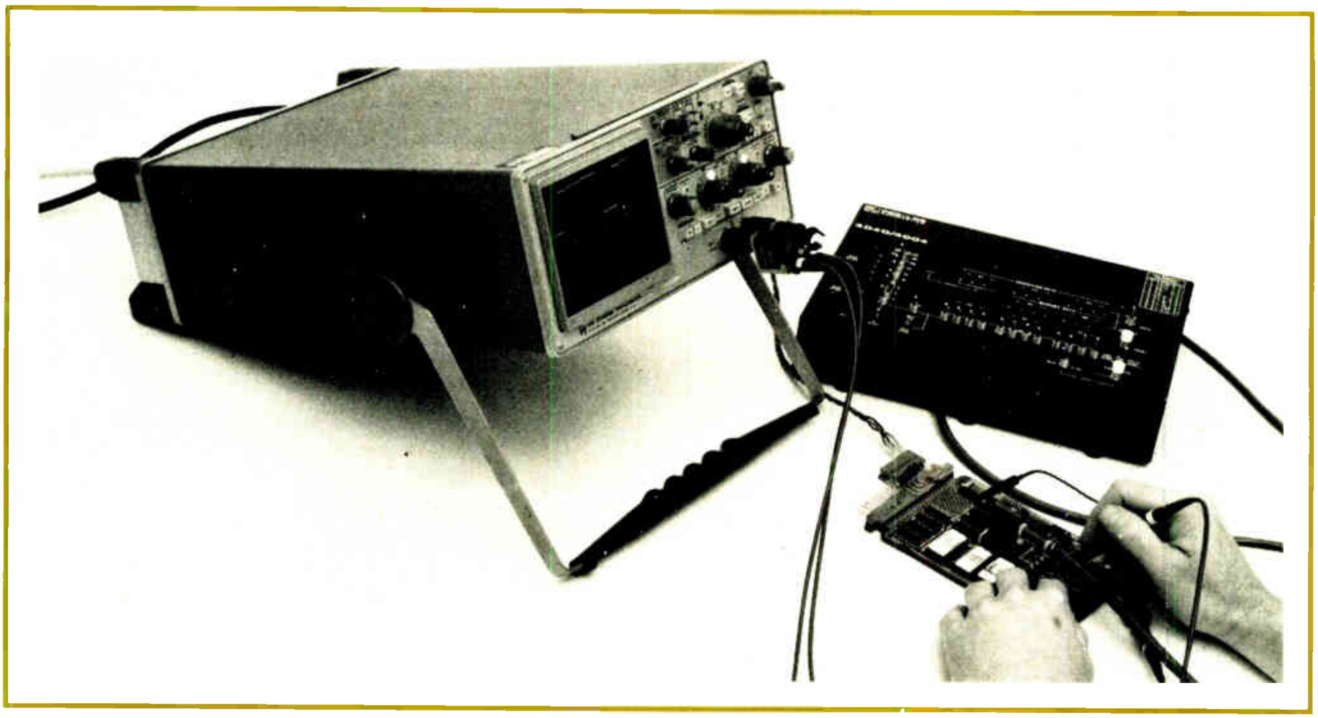
by Ed Lee, Pro Log Corp Monterey Calif

☐ To make a success of designing most microprocessor-based control systems, an engineer doesn't need to become a computer programer. Once he has recognized the surprising similarities between hardware design and microprocessor programing, he can build on his hardware background and write and debug a program just as efficiently as he can wire up and debug a breadboard.

In this approach, the engineer lists his instructions to the microprocessor on one or more program-assembly forms, which combine the functions of a circuit schematic and an assembly print or wire list. Then he writes the instructions into the microprocessor's control memory—at this stage a programable read-only memory, the equivalent of a circuit breadboard. Finally, he tests the PROM, altering it and the program-assembly form in parallel, until he can plug the fully debugged version into its socket in the overall system prototype.

At all points, the human element is taken into account. The program-assembly forms contain plenty of room for corrections, so that their layout need never be jumbled confusingly, as inevitably happens with computer printouts. Hexadecimal coding of the PROM is used because the mind finds binary code a nightmare and even octal not distinctive enough. Easily memorizable or mnemonic coding explains each hexadecimal instruction, making it easy for manufacturing, test, and field engineers, as well as design engineers, to understand what is happening in detail. A final comments column on the form documents the significance of each program step.

The technique has worked successfully with many important system designs. One of the most complex was a heart-monitoring system, designed and built three years ago. This system monitored, recorded, and analyzed several heart waveforms, did real-time signal averaging, had automatic gain control, and was entirely operated by an Intel 4004 microprocessor. The program was



Debugging. The final stage in the design of a microprocessor system is to see if the program works as it was designed to. Here, an oscilloscope and a system analyzer are being used to debug a system whose program is in a PROM, equivalent to a circuit breadboard.

about 3,200 instructions long, but even so it took two engineers, working in parallel on different parts of the design, less than 600 manhours to write and debug it and also debug most of the hardware.

The circuit-design sequence

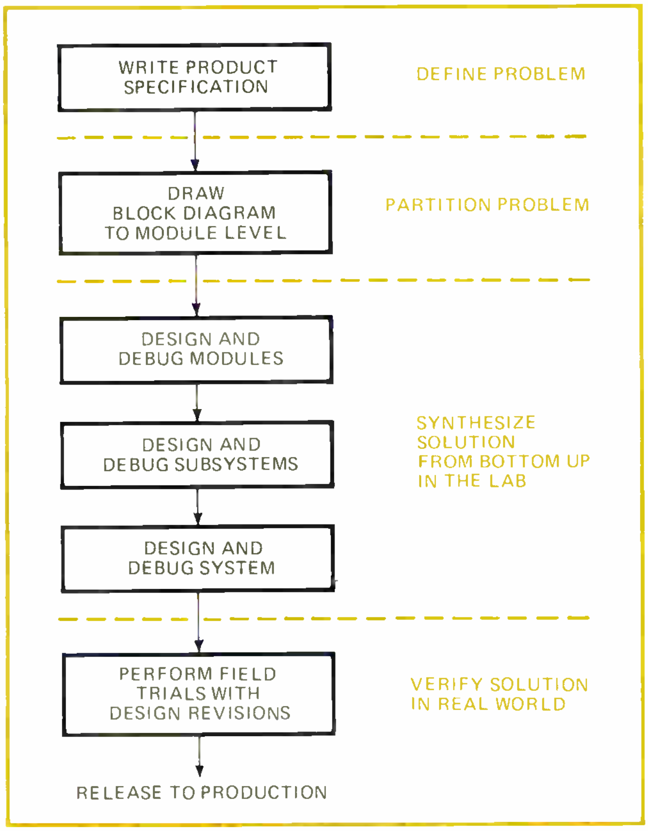
In designing any electronic system, the main task is not to build a breadboard in the laboratory, but rather to create a set of documents from which people in manufacturing and field service can build and maintain the equipment. To produce that documentation, a designer of, say, a hardwired-logic system would typically follow the steps shown in Fig. 1. From the product specification—the basic definition of the problem—he uses block diagrams to break the design problem into bite-sized chunks, which can be more easily comprehended and solved individually. The design-and-debug process he does first at the module level, then the subsystem level, and then the system level. Finally, the field trials are used to verify his solution in the real world.

A more detailed look at the design-and-debug sequence used by the design engineer at each level is given in Fig. 2. The engineer first converts his conceptual design into a schematic—his language for visualizing solutions. Each of the schematic symbols represents the function of a particular type of hardware. A good schematic is a visual tool (Fig. 3); the symbols are grouped and properly labeled to show clearly how the components interact. White space, labels, right-left conventions for inputs and outputs—all help the designer and anyone else who uses the documents. Schematics, in fact, are not drawn just for the designer but are intended to aid manufacturing, test, and field-service personnel.

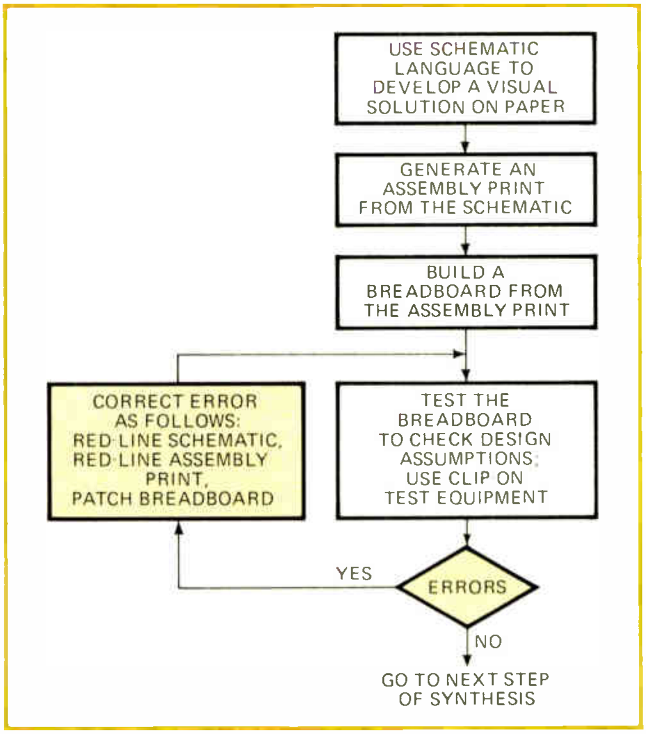
From the schematic he generates an assembly print, a wire list, or both. The assembly print maps the actual layout and wiring of hardware. The engineer then builds a breadboard and tests it to verify his design assumptions. In testing, he usually hangs his schematic and assembly print on the wall next to his workbench. On the workbench are the breadboard, the test equipment with clip-on leads, power supplies, and the interface-exercising circuitry.

Once the testing starts, errors are soon discovered. In correcting one, the wise engineer follows a fixed routine. He "red-lines" it on the schematic, in the white space near the part of the circuitry involved with the change; then he red-lines the assembly print, and finally he patches to reflect the red line. In this way he keeps his documentation in lockstep with his hardware. (Note that patching is easy when a schematic is drawn with white space and the hardware is laid out with room for patches.) This debugging cycle is repeated many times during a normal design and can be started and stopped at any point without loss of time. Finally, field trials are made not only to test the design in the real world, but also to assure that the product specification has been met.

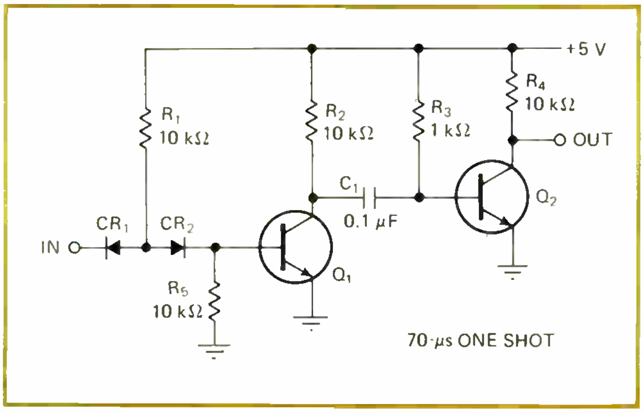
Within a microprocessor-based system, the microcomputer (microprocessor plus memory plus input/output circuits) takes its place alongside the other modules or subsystems. Like any other black-box logic ele-



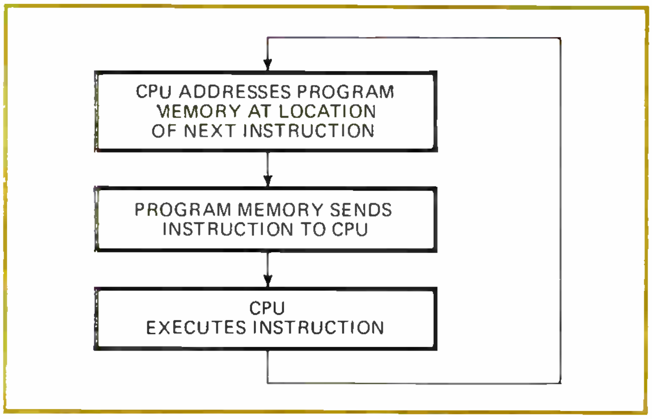
1. Scientific approach. When designing hardware, most engineers use a regular approach, working from the original product specification. One of the keys to successful designs is partitioning the problem into easily solved modules and subsystems.



2. Check it out. In designing and debugging a hardware module, an engineer typically concentrates on the error-correction stage, in which the schematic and assembly prints are redlined and the breadboard patched to account for the changes.



3. Schematic conventions. In a typical engineering schematic, the component symbols are labeled and arranged to show how they interact. Each symbol and notation has a function in helping understand how the actual hardware works.



4. Instruction cycle. To execute one instruction, a microprocessor typically goes through three fundamental steps—addressing memory, extracting the instruction from memory, and performing the operation. A typical cycle takes about 11 microseconds.

ment, it is wired to them through its input gates and output latches (flip-flops). But, unlike other black boxes, the engineer does not wire up components inside it but simply puts specific coding into the control memory, a ROM or PROM. Functions such as noise rejection, switch-bounce elimination, and the assignment of meanings to the various contacts are all performed by the stored control program. In fact the microcomputer does everything any other black box with the same number of inputs and outputs might do—from timing, making decisions, and doing arithmetic to converting codes, linearizing curves, and storing data.

(Note, however, that the data memory within the microcomputer is generally no more than a few hundred bits of register storage. If the designer wants to store more data, it is far more cost-effective to put data memory outside the microcomputer as one or more input/output modules. Also, since the internal workings of the system are sequential in time, a clock is necessary to step the system along.)

Read-do interaction

The system operates through the interaction of the microprocessor and the program memory in a read-do cycle. When power is turned on, the microprocessor (or central processing unit) reads the first code word in program memory, interprets its meaning, and does what it is told. When it finishes the first operation, it reads the next line and does that, and so on. The microprocessor reads program memory in the same way humans have been trained to read instructions on a sheet of paper. We read by directing our eyes to a particular line, sensing the symbols, mentally applying meaning to these symbols, and then acting on the basis of the meaning. (A problem with microprocessors is that each type interprets the same set of symbols differently just as alphabetic symbols take on different meanings in French, Italian, and English.) We automatically read and do the next line, without being told, unless the line we're reading tells us to, say, go to the bottom of the page five and read a footnote before proceeding to the next line (equivalent to a subroutine instruction).

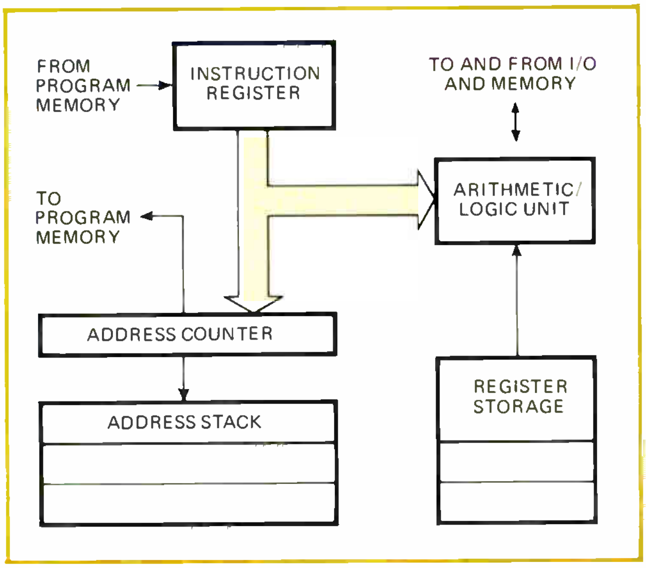
Figure 4 shows a typical sequence (instruction cycle) that the microprocessor system must run through to perform a task. A system using the Intel 4004, a single 4-bit microprocessor, for example, takes eight clock cycles to complete the sequence: three cycles for the 4004 to send a 12-bit address to program memory in 4-bit bytes, two cycles for the program memory to send back the 8-bit instruction in 4-bit bytes, and three cycles for the 4004 to decode and execute the instruction. Each instruction cycle takes about 11 microseconds. Some instructions require more than one instruction cycle to define and execute. For example, the program memory might contain a lookup table (to, say, linearize a curve or multiply two decimal digits). To take one 8-bit word and translate it into another 8-bit word using the lookup table takes two instruction cycles with the 4004.

The circuitry inside the 4004 CPU chip is shown in terms of its functions in Fig. 5. The address counter controls which line of program memory is to be read next; it starts at 000 and counts up. The instruction register and related decoding gates interpret the 8-bit word from the program memory and cause things to happen. The arithmetic/logic unit and the register storage cells comprise read/write memory elements, in which data can be manipulated by instructions. The address stack enables the CPU to return to the main program after it has performed a program module called a subroutine. The judicious use of subroutines is essential to the bottom-up synthesis approach described below.

The programing parallels

For each step in the hardware design process, there is a corresponding element in the microprocessor programing process (Fig. 6). Just as the block diagram is used to partition the hardware into bite-sized chunks, so a flow chart is used to partition the program into byte-sized sequences. The schematic language is equivalent to the mnemonic coding—they both help the engineer to conceptualize a solution. The wire-list or assembly-print coding is equivalent to the hexadecimal program coding—they all tell how to organize actual hardware elements to produce the desired system.

A schematic with its related assembly print is equivalent to a program-assembly form. These are the docu-



5. Inside the 4004. In the Intel 4004 4-bit microprocessor, the address counter accesses the next instruction from memory, and the instruction register then controls the ALU. Read/write memory elements make up the ALU and the register storage cells.

ments that show both the functional and hardware implementation of the design, and they are key documents for manufacturing and maintenance. A component such as a resistor is equivalent to a microprocessor instruction—both perform a specific indivisible function in the system. A module or subsystem (a specific configuration of components) is equivalent to a subroutine (a specific configuration of instructions) since both perform specific complex functions when used in the system.

The engineering breadboard or prototype is equivalent to a programable ROM—each is the hardware implementation of the design used to prove (test) the correctness of the design concept and the design documentation. The Wire-Wrap gun or soldering iron is equivalent to the PROM programer—each is an instrument used by a person to configure hardware (a breadboard or a PROM) on the basis of the documentation (assembly prints or program-coding forms). The oscilloscope is equivalent to the clip-on tester—both are temporarily attached to equipment to see what is going on for the purpose of debugging, and both are removed when not in use.

Figure 7 shows the design process for a microprocessor-based system that combines the hardware and microprocessor elements.

The basic procedure

A flow chart is a tool for describing a sequence of events with as few as two symbols—a box for a process and a diamond for a decision. Once it has generated bite-sized program modules, these modules can be synthesized visually with mnemonic coding.

The successful use of mnemonic symbols for synthesis depends partly on their own degree of obviousness and standardization and partly on clarity and consistency in organizing them visually on paper (allowing white space, following conventions, and labeling properly). A properly designed program-assembly form, such as the one in Figs. 8a and 8b, helps immeasurably with their organization.

Here, the mnemonics (operation and operand) columns, together with the comments and label columns, have the function of a schematic. For instance, the entry in the label column has the same function as the "70-μs one-shot" circuit title in Fig. 3, and each label appears only once in a system at the beginning of the group of instructions that form that program module.

In short, the schematic portion of the program-assembly form is in no way used by the microprocessor—it is there solely to help people visualize the functioning of the system, either when designing or when servicing it, and should therefore be organized to minimize the education problem. This calls for documentation standards and symbology that in itself is as obvious as possible. Ideally, the symbology should be standardized industrywide and as independent of specific microprocessors as possible. Unfortunately, vendors now have suggested almost as many different sets of mnemonics as there are microprocessors. These shown here are Intel's for its 4004 and 4040 CPU chips.

The assembly-print portion of Figs. 8a and 8b is in the hexadecimal column. The coding in this portion corresponds to the actual coding of the program as read by the microprocessor. Coding is completely dependent on the characteristics of the microprocessor used in the system. Figure 9 shows the hexadecimal coding related to specific mnemonics for the 4004 CPU.

In normal operation, the microprocessor sequences through the hexadecimal instructions from the top down. Some instructions act like components, some like connecting wires, and some like components linked to a wire (Fig. 9). Component-like instructions cause the microprocessor to do something—load a register (FIM) or add two numbers (ADD). Instructions that act like wires cause the processor to go from place to place (module to module) in the program (JUN, JMS, BBL). The conditional-type instructions act as both components and wires (JCN and ISZ), since they perform an evaluation and then a jump in the program.

Once the designer understands the functions symbolized by the mnemonics, he groups the mnemonic symbols on paper to achieve the functions of a module or subroutine. A subroutine can be viewed, for example, as equivalent to a 5-volt power supply. If an engineer designs a system using 30 transistor-transistor-logic chips, these chips all use +5 V, but he builds only one 5-V supply and provides a power wire and a ground return to each chip from that supply. The JMS instruction performs the function of the power wire, while BBL is the ground return. JMS (1 sec) in Fig. 8a, for example, indicates the program should go to the (1 sec) subroutine in Fig. 8b and at the end of that subroutine, BBL automatically sends the processor back to the main program at line 00D—JMS (SET).

Each subroutine module should be visually obvious, and therefore its label (in the label column) is at the top and white space (unused lines), which can also be used for coding in later corrections, is left above and below the module.

Equally important is the documentation shown in the comments column of the schematic. (Failure to document comments is known as job security in data processing, but in engineering, it's known as sloppy documentation.) The comments are vital to debugging, since they explain to the design engineer, as well as to manufacturing, test, and field-service personnel, what the program is doing to affect the hardware. They should not be too detailed or suffer from the common mistake of explaining how the program works on an instruction-by-instruction basis. They should give clear indications of where in the program keys are set, displays are loaded, time intervals are generated, etc. Note the simple explanations followed by the arrows to show the block of instructions required to perform each of the system functions. (The test technician or engineer can get his understanding of the detail from the dictionary of Fig. 9).

After the program schematic has been generated, the instruction column is coded in hexadecimal. The address columns represent locations in the program memory. Coding the instruction column is equivalent to generating a hardware wire list, since this coding is put in the PROM to configure the hardware. One does the coding with the aid of a lookup table (a partial table is shown in Fig. 9). After a while, engineers find they can do most coding from memory at an average rate of more than 10 lines per minute.

Note again that address and instruction coding should be in hexadecimal, not in octal or binary. The reason is simple—hardware debugging requires a humanly comprehensible code that enables a person to readily relate the events occurring in a given interval of time to what he sees on a piece of paper. Binary code is unhelpful, and octal code does not provide a specific character for specific time slots for 4-bit or 8-bit microprocessors. Thus, hexadecimal is the best compromise, since one character represents 4 bits, and most instructions are 8 bits; that is to say, they are two hexadecimal characters.

A particular application

The programs shown in Figs. 8a and 8b are part of a time-of-day clock. The system hardware includes the 4004 microprocessor, six digits of latching display (two for hours, two for minutes, and two for seconds), and two keys to enable an operator to set the time display to correspond to real time. When the power is turned on, the display comes up showing 12:00:00. If the operator depresses the first key, the hours count up once a second until he releases the key. If he depresses the other key, the minutes count up once a second.

Figure 8a describes the main program in three ways—as it affects the system (in the comments section), its functional operation at the instruction level (under the mnemonics columns), and as it is coded in program memory to enable the microprocessor to perform the functions (under the hexadecimal column).

The instruction column shows the hexadecimal coding contained in each location in program memory. The locations are identified in this case by three hexadecimal characters, the first defining a page address, and the last two a line address within the page. They

HARDWARE ◀	▶ PROGRAM
BLOCK DIAGRAM	FLOW CHART
SCHEMATIC LANGUAGE	MNEMONIC CODING
WIRE-LIST OR ASSEMBLY-PRINT CODING	HEXADECIMAL CODING
SCHEMATIC AND ASSEMBLY PRINT	PROGRAM-ASSEMBLY FORM
COMPONENT	INSTRUCTION
MODULE OR SUBSYSTEM	SUBROUTINE
BREADBOARD OR PROTOTYPE	PROM
WIRE-WRAP GUN OR SOLDERING GUN	PROM PROGRAMER
OSCILLOSCOPE	CLIP-ON TESTER

6. The duals. Each step or element in the hardware-design process has an equivalent in the writing of a program. An engineer accustomed to modular design of hardware can use much of his experience when writing programs for microprocessors.

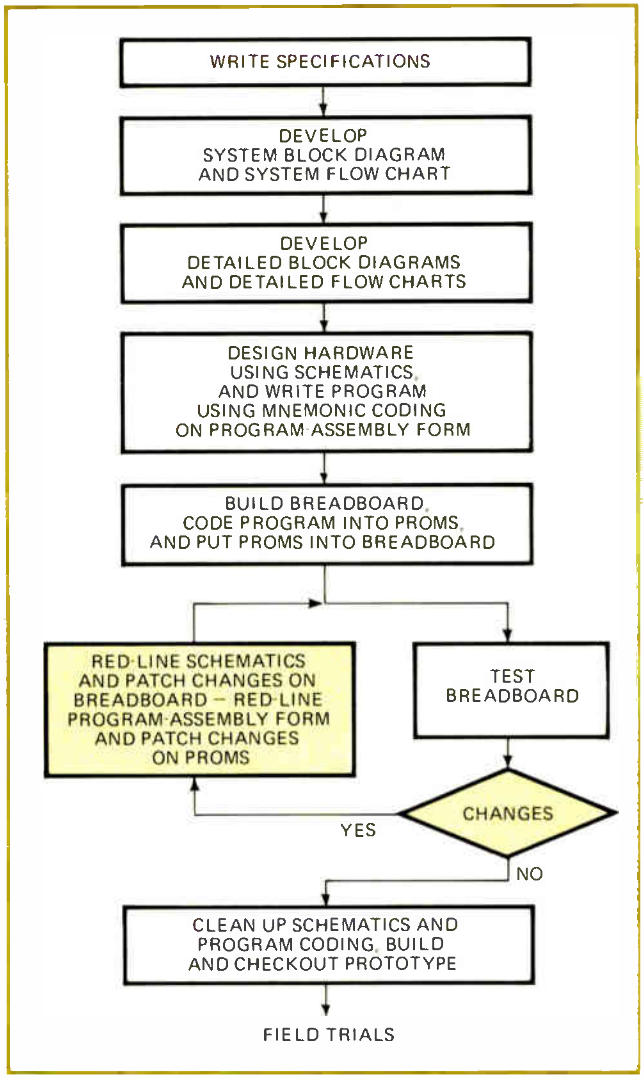
correspond to the addresses A_1, A_2, and A_3 in Fig. 9

The overall system operation is readily understood by reading the statements in the comments section in their normal sequence. Power turn-on automatically starts everything at the top. The first thing that happens is that the display digits are cleared, then the initial display time of 12:00:00 is set into microprocessor memory at the memory locations shown on the adjacent register map. Then the program shifts the memory contents to the display, waits 1 second, checks the set keys to see if they are closed, increments the time count in memory by 1 s and then jumps back to repeat the sequence, starting with the loading of the memory contents to the display.

Each of the major events, except the initializing of memory, is accomplished by a subroutine. This is evident from the mnemonics column in which JMS occurs repeatedly. The primary reason for using subroutines in this case is to make the program humanly easy to understand, not to save code. Subroutines are read by the microprocessor just as we read footnotes in a report. The JMS instruction is coded by the designer to send the microprocessor to the location where the subroutine starts. At the end of the subroutine, the BBL instruction says "go back to the place in the program whence you came." The CPU remembers where it came from because address information is stored in its address stack at the time the JMS was executed.

Figure 8b illustrates one of the subroutines in the program. This subroutine is a time-delay module and is functionally equivalent to the circuit shown in Fig. 3. The module has two parts. The first part (lines 0E4 to 0E7) sets the time delay, just as the RC network in the one-shot circuit sets its time delay. The second (0E8 to 0EF) actually produces the delay time by sending the microprocessor into a series of counting loops that require the preset time for their execution. When it completes the counting, the microprocessor reaches the BBL instruction (0F0).

This subroutine is executed through the two-line JMS instruction, coded at lines 00B and 00C in Fig. 8a. This



7. Program design. The procedure for writing a microprocessor program is similar to that of designing hardware. For every step in hardware design, there is an equivalent step in program organization, so hardware and software elements appear together.

instruction has two parts—the hexadecimal 5 stored at 00B tells the processor both that it is about to execute a subroutine and that the last hexadecimal character on this line and the two characters on the next line will tell it where that subroutine is stored. After reading line 00C, the microprocessor loads the address it has read, 0E4, into the address counter, and simultaneously pushes the old contents, 00C, out of the address register and into the address stack. On the next instruction cycle it reads the code at line 0E4 and thus begins to execute the subroutine. When it finally comes to line 0F0 it sees the code C0 which instructs it to take the data in the address stack 00C, move it into the address register, and increment it 00D. The microprocessor next reads the program at 00D and continues in sequence from there.

Consider now the following request for changes in system performance. The time of day at which the clock comes on when power is applied is to be 3:27:15, and the clock is to count five times a second rather than once a second. This documentation makes it easy to see where the changes should be made. The time is set during the initialization. In fact, from the comments and the register map it is clear that the hours are set at line 004, the minutes at line 006, and the seconds at 008. Simply changing program code at these locations is enough to change the initial time. It is also clear that the rate of count is controlled in the "wait 1 second" function and that lines 0E5 and 0E7 are the ones to change to alter the delay time.

Trial run

Once the program "schematic" and "wire list" have been properly documented in the comments column, it's time for the debugging phase. The equivalent of a breadboard is a programable ROM. The most useful PROM for this purpose is the 1702A, which is erasable and also readily available. The 1702A PROM has 256 (or, in hexadecimal, FF) 8-bit words.

The tool used to code the PROM is a programer, which is equivalent to a soldering iron. The programer has four basic operations—list, program, duplicate (with corrections), and verify. When a PROM is coded for the first time, the program mode is used. In this mode, the programer enters the data through the keyboard into the PROM (the instrument automatically keeps track of addressing). Only two keyboard entries per line of code are required, and the 256 lines of code in a 1702A can be manually coded from the assembly form in less than 15 minutes.

If a systematic, modular method of program synthesis is being used, the operator will probably never code more than 60 or 70 instructions at a time. For example, he would code the (1 sec) module of Fig. 8b in less than a minute. Once the basic code is in the PROM, the duplicate mode is used to make corrections or new PROMs. In the duplicate mode, the original PROM is put in the master socket, a blank PROM is put in the copy socket, and the changes—the red lines—are keyed in through the keyboard. The programer then writes in a corrected copy of the 1702A PROM in less than 30 seconds.

Once the new PROM is coded, it is placed in the microprocessor system at the workbench, and breadboard testing begins. The program-assembly form is taped on the wall, one page of forms per PROM. At the workbench are the oscilloscope, power supplies, voltmeter, and another piece of test equipment, such as the system analyzer shown in the lower center in Fig. 10.

The system analyzer clips onto the microprocessor chip in the microcomputer breadboard. It has a built-in logic that enables it to observe the system without affecting its operation. Because it clips directly onto the CPU chip, it observes everything that flows into or out of the chip—program addresses, instructions coming back from PROM, and data as it is being manipulated by the CPU.

The primary characteristic of the system analyzer is its ability to synchronize on any step of the program. For example, to observe the time-delay subroutine in action, the user sets up the address switches to the appropriate program address and observes the display lights, which show everything going on whenever that instruction is executed by the CPU. The analyzer also

HEXADECIMAL				MNEMONIC		TITLE 12 HOUR CLOCK DATE
PAGE ADR	LINE ADR	INSTR	LABEL	INSTRUCTION OPERATION	INSTRUCTION OPERAND	COMMENTS
0	0 0	00		NOP		
	1	50		JMS		
	2	60			(CLR DISP)	
	3	2E		FIM	P7	SET TO 12 O'CLOCK
	4	12		1	2	HOURS
	5	2C		FIM	P6	
	6	00		0	0	MINUTES
	7	2A		FIM	P5	
	8	00		0		SECONDS
	0 9	50	CLOCK	JMS		SHOW TIME
	A	BE			(DISPLAY)	
	B	50		JMS		WAIT 1 SEC
	C	E4			(1 SEC)	
	D	50		JMS		SET CLOCK PER KEY INPUT
	E	20			(SET)	
	F	50		JMS		COUNT TIME BY 1 SEC
0	1 0	80			(COUNT)	
	1	40		JUN		
	2	09			CLOCK	
	3					
	4					
	5					
	6					

INDEX REGISTER MAP

		REG PAIR		
E	HOURS	P7	HOURS	F
C	MIN	P6	MIN	D
A	SEC	P5	SEC	B
8	DISPLAY	P4	DISPLAY	9
6		P3		7
4		P2		5
2	Δ	P1	Δ	3
0	Δ	P0	Δ	1

HEXADECIMAL				MNEMONIC		TITLE 12 HOUR CLOCK DATE
PAGE ADR	LINE ADR	INSTR	LABEL	INSTRUCTION OPERATION	INSTRUCTION OPERAND	COMMENTS
0	E 0					
	1					
	2					
	3					
	E 4	22	(1 SEC)	FIM	P1	1 SECOND DELAY - INITIALIZE
	5	F5		F	5	MSD
	6	20		FIM	P0	
	7	00		0	0	LSD
	E 8	70	Δ	ISZ	R0	DELAY TIMING OPERATION
	9	E8			Δ	
	A	71		ISZ	R1	
	B	E8			Δ	
	C	72		ISZ	R2	
	D	E8			Δ	
	E	73		ISZ	R3	
	F	E8			Δ	
0	F 0	C0		BBL	0	
	1					
	2					
	3					
	4					
	5					
	6					

8. Typical program. A program for a 12-hour clock (a) uses jump (JMS) instructions to call subroutines, such as the 1-s delay, (b).

HEX CODING	MNEMONIC		DESCRIPTION OF OPERATION
	OPR	OPA	
0 0	NOP		No operation
1 C_x A_2 A_1	JCN	C_x LABEL	Jump on condition C_x to the program-memory address A_1, A_2, otherwise continue in sequence.
2 P_x0 D_2 D_1	FIM	P_x D_2 D_1	Fetch immediate from program-memory data D_1, D_2 to index register pair P_x.
4 A_3 A_2 A_1	JUN	LABEL	Jump unconditional to program-memory address A_1, A_2, A_3.
5 A_3 A_2 A_1	JMS	LABEL	Jump to subroutine located at program-memory address A_1, A_2, A_3. Save previous address (push down in stack).
7 R_x A_2 A_1	ISZ	R_x LABEL	Increment and step on zero. Increment contents of register R_x, if result is not 0 go to program-memory address A_1, A_2, otherwise step to the next instruction in sequence.
8 R_x	ADD	R_x	Add contents of register R_x to accumulator.
C D_x	BBL	D_x	Branch back one level in stack to the program-memory address stored by a prior JMS instruction. Load data D_x to accumulator.

9. Dictionary. A partial listing of instructions for the 4004 microprocessor shows the mnemonic, the hexadecimal code, and the operations performed by the device. Some instructions act like components; some like connecting wires; some like components and wires

generates a scope synchronization pulse at the same time. If something goes wrong, an oscilloscope can be used to see if it is a hardware or timing, rather than a program, problem.

The system analyzer and an oscilloscope are usually all that are necessary to debug microprocessor-based hardware. If a program error is found during test, the user red-lines the documentation (mnemonics and comments, then the hex coding) and uses the original PROM and the programer to create a duplicate PROM, but with all the red-lined corrections. (Note this luxury, one that the hardware designer doesn't have: the old PROM is untouched, until erased with an ultraviolet light, and is available in case the new red lines do not work).

Repeating the process

The process is repeated at subsystem and system levels. For the 12-hour clock system, the instructions in Fig. 8a were all that were written and debugged at system level. At system level, the whole program can be taped on the wall. The modules are visually obvious and sequenced in PROMs according to convention, with the main program at the beginning of the first PROM and with subroutines placed after the main program. Because of white space, the modules are highly visible and do not move around on the paper when corrections are made. Corrections are placed in the white space near the module affected. Because of stability of location, the designer becomes familiar with the positions of modules in the program and develops a system understanding far greater than that allowed by reams of computer printout, whose listings shift around each time the program is reassembled. Once the system program is debugged, the modules may be moved to eliminate unused programable memory, but often even this is not necessary, or desirable.

Once the design is complete and systems are shipped, they can be tested in the field simply by clipping on the system analyzer and an oscilloscope. The field-service technician needs only the program-assembly form, properly documented, and the hardware schematics and

10. At the bench. Microprocessor systems—both hardware and software—can be checked out easily once the program has been fully documented, using the formats shown in Fig. 8 and a hardware system analyzer as shown here

assembly prints to successfully accomplish the tests.

This design-debug procedure for programing microprocessors is better suited than either computer-aided design or simulation in a random-access memory to the bulk of real-world controls. Most of these controllers require fewer than 2,000 instructions, and for this size of program, CAD does little to improve the design approach and a lot to separate the design engineer from intimate knowledge of his hardware.

As for RAM simulation, it is highly vulnerable to human error. But the use of program-assembly forms, together with a PROM, forces the documentation to stay in step with the hardware throughout the design process and makes it visually useful to the engineer, test technicians, and field-service personnel. Power can be turned off the breadboard mockup of the microprocessor at any time in the design-debugging cycle and turned back on to pick up instantly where the designer left off. No time is wasted loading and dumping programs. The old breadboard can be maintained until the new breadboard is proven. (Many times a fix does not work and the designer wants to get back to the way it was.) With this method, he simply plugs in his last PROM. Old PROMs are erased only when the designer is satisfied with the corrections.

More efficient still, two or more engineers can work in parallel, at two or more workbenches, on two or more modules and simply tie the modules together at subsystem or system level if they have standardized documentation. Moreover, the test equipment can go into the field to modify actual operating systems. □

Rfi generation is a factor when selecting ac-switching relays

by Allan Q. Mowatt, Th[illegible] J Relays Inc., Reading, Mass.

☐ Relays are commonly used in alternating-current circuits to switch loads such as motors, tungsten lamps, and power supplies. An inevitable consequence of the selection of the tried-and-true electromechanical relay is the problem of radio-frequency interference, and so solid-state relays have come into prominence.

As a rule, electromechanical relays are the cheapest type. However, because of their inherent bounce during contact closure and opening, they can generate large switching transients, which manifest themselves as rfi. As a result, solid-state relays, which have no moving parts and so are free of bounce, are often chosen for those applications where rfi must be held down to a minimum.

For even more rfi reduction, many solid-state relays contain zero-crossover circuitry that delays their turn-on until the sinusoidal voltage applied to the load reaches 0. This delay could be as long as the entire first half-cycle of the driving waveform. Zero-crossover (also called zero-switching) relays are generally at least 30% more expensive than standard solid-state versions. In applications involving relatively low load currents, they do not improve performance appreciably more. However, they do have a place in high-ampere, high-speed switching.

Rfi and electromechanical relays

One cause of electromagnetic radiation at radio frequency is contact arcing during switching. Another source of interference-causing radiation is transient-induced voltage created by the relay coil when its energizing circuit is interrupted.

Characteristically, this interference is impulsive in nature and extends through a wide spectrum of frequencies. Hence, it is often referred to as broadband impulse interference. Figure 1 shows the considerable rfi typically generated by an electromechanical relay controlling an ac induction motor.

The closing of a set of relay contacts is invariably accompanied by contact bounce, which occurs when the interfaces separate as a result of the closing impact of the spring structures. When the contacts are carrying a current of greater than several hundred milliamperes at above 100 volts, abrupt signal changes occur in the contact leads, creating interference that is both conducted along these leads and radiated from them. Although these changes can be illustrated as a series of solid pulses, each pulse is actually a burst of rf oscillations across the contact gap.

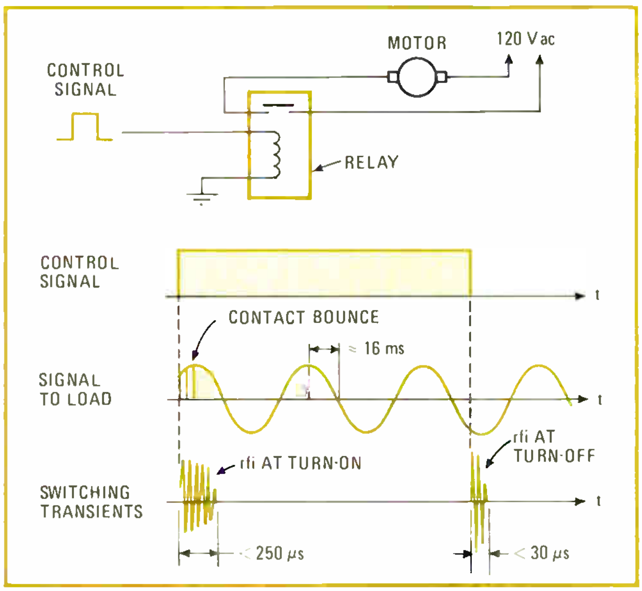
Conducted interference can be regarded as a noise signal that is coupled directly or capacitively to another location in the system. The conductor over which the noise impulse is carried can act like an antenna wire, thereby creating radiated interference.

The magnitude of the low-frequency components of this interference depends on overall pulse duration, while the high-frequency magnitude is related to the rise and fall times of the pulses. For a typical electromechanical relay, the average pulse width is about 30 microseconds. However, because contact bounce during switching usually involves a train of pulses, rfi can occur for 250 μs or longer. The slopes of the rise and fall portions of the rfi pulses are generally determined by the RLC transient behavior of the relay and load circuit.

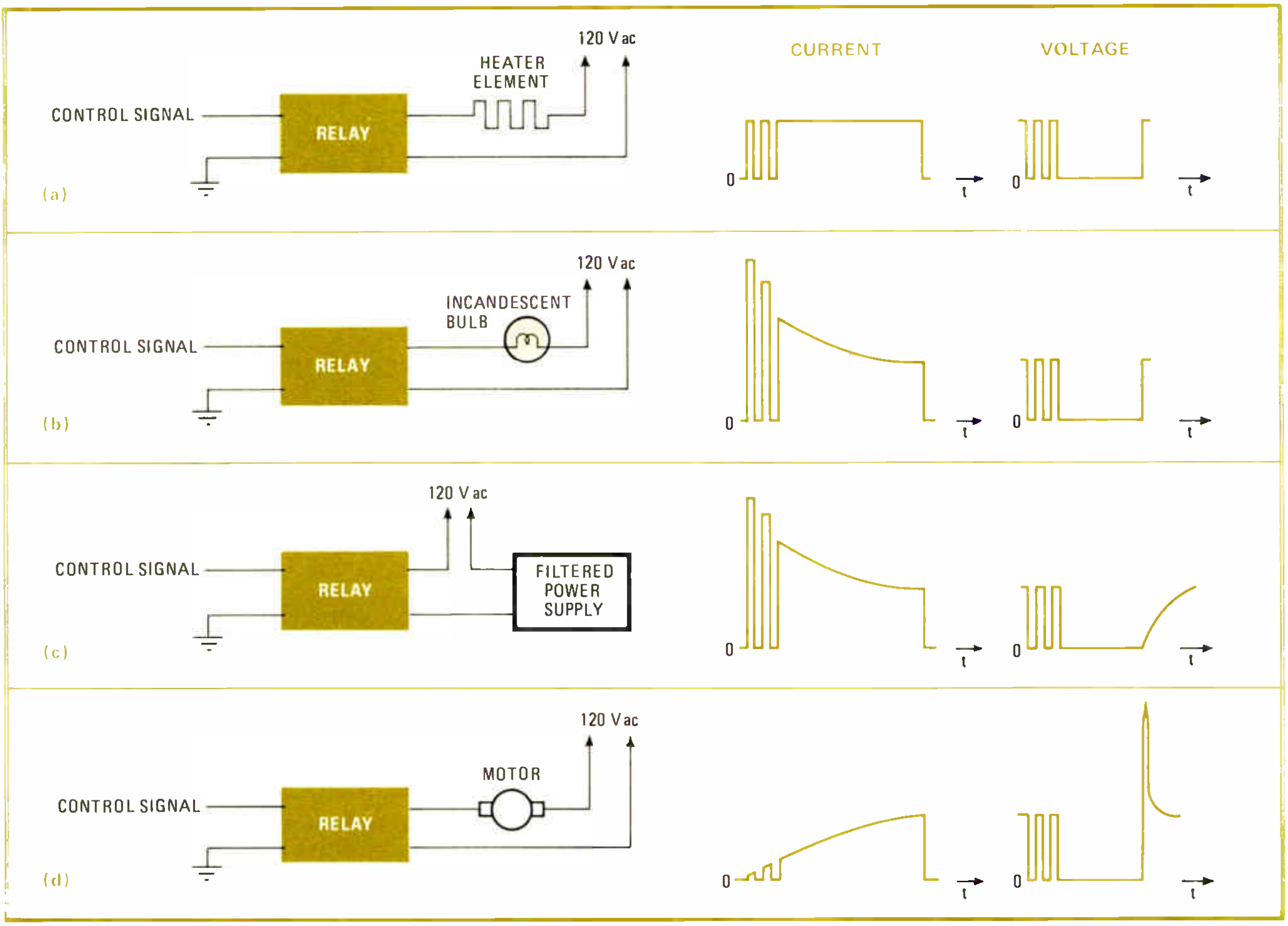
Figure 2 shows the contact bounce that occurs during closure of an electromechanical relay for various types of loads. Current and voltage waveforms are given for a purely resistive load (a), a tungsten-lamp load (b), a primarily capacitive load (c), and a primarily inductive load (d). In the last case, the largest voltage spike occurs, not upon closure because of contact bounce, but upon opening when load current is interrupted.

Consequences of contact opening

Needless to say, rf oscillations can be particularly severe during interruption of current to an inductive load. Figure 3a depicts the shape of the contact discharge-voltage waveform when steady-state current is less than the minimum required to produce arcing, while Fig. 3b



1. Severe rfi. When an electromechanical relay is used to control an ac induction motor, considerable rfi is generated when the load is switched on, as well as when it is switched off. The tinted areas of the timing waveforms indicate the on portions of these signals.



2. Contact bounce vs load. In an electromechanical relay, contact bounce occurs when the load is switched on. The extent to which bounce disrupts load current and load voltage depends on the load itself, whether it is a heater element (a), an incandescent bulb (b), a power supply (c), or a motor (d). In the latter case, the largest switching spike is produced upon contact opening, not contact closure.

shows this voltage when the current is greater than the minimum for arcing. Moreover, similar oscillations, caused by bounce and brief separation, can occur at contact closure.

The high-frequency oscillations—or "showering" effect—are produced when the inductive load current charges the contact capacitance to a level sufficient for arcing. The arc discharges the capacitance; the inductive current reverses, and so the cycle continues until all of the inductive energy is dissipated.

The radiated element for contact opening of this interference is broadband, with peaks and nulls occurring all the way from 10 to 1,000 megahertz, as indicated in Fig. 4a. The amplitude of the radiation and its location in the frequency spectrum depend on the load current and such layout factors as wiring, shielding, and the capacitance to ground.

The spectrum of conducted interference for contact closure typically resembles the plot of Fig. 4b. This conducted rfi has the frequency distribution of a step function—that is, a continuous spectrum of noise with an amplitude that decreases with frequency at the rate of 20 decibels per octave.

Like an electromechanical relay, a solid-state relay containing a thyristor output switch (whether a triac or back-to-back silicon controlled rectifiers) generates a transient at turn-on. This transient occurs when power is first switched on to an ac load at a point where the driving sine wave is well above 0.

The spectrum of conducted interference for a solid-state relay is generally the same as that shown in Fig. 4b for an electromechanical relay. But there the similarity ends.

No contact bounce

In a solid-state relay, there is no contact bounce, no arcing, and consequently no lengthy showering period during which broadband rf oscillations are produced. Since the relay's thyristor output usually switches on in less than 1 μs, the resultant rf oscillatory period is only about 5% of the time of a single contact bounce of an electromechanical relay.

Standard solid-state relays are available in several versions (Fig.5). They can be transformer-isolated (a) or optically isolated with either a photo-transistor (b) or a string of photo-SCRs (c) when very high blocking voltage is needed. Zero-crossover models, like the one shown in Fig. 6, contain additional control circuitry and usually employ a phototransistor optical coupler for isolation.

Zero-crossover solid-state relays can perform a function not possible with electromechanical relays—

through special circuit configurations, they guarantee that relay turn-on for resistive loads occurs only near the zero crossing of the voltage sine wave. Even if the relay is signaled to fire when the voltage sine wave is at or near its peak value, turn-on is delayed until the next zero crossing.

The operation of a zero-crossover circuit is relatively simple. In the relay of Fig. 6, the state of transistor Q_1 is governed by the control signal applied to the optical coupler, while the state of transistor Q_2 is essentially determined by the level of the driving voltage. If either of these transistors is saturated, the SCR cannot fire because its gate is clamped to ground.

The entire circuit is always off at the zero crossing of the driving sine wave. With no control signal present, transistor Q_1 goes into saturation once the voltage at the anode of the SCR exceeds 1 volt. Transistor Q_2 saturates a little later, when this voltage reaches approximately 5 V. The SCR, therefore, never fires without a control signal being applied.

If the control signal is present at the next zero crossing, transistor Q_1 remains off, no matter the level of the driving voltage. However, transistor Q_2 stays off only until the SCR's anode voltage reaches 5 V. This means that both Q_1 and Q_2 are off for a brief time, permitting the SCR to fire and trigger the triac, so that the load switches on.

In essence, then, transistors Q_1 and Q_2 create a brief firing window at the beginning of each half-cycle, between about 1 and 5 V. If the relay is signalled to turn on at a later point in the cycle, it must wait until the next window occurs—when both Q_1 and Q_2 are off.

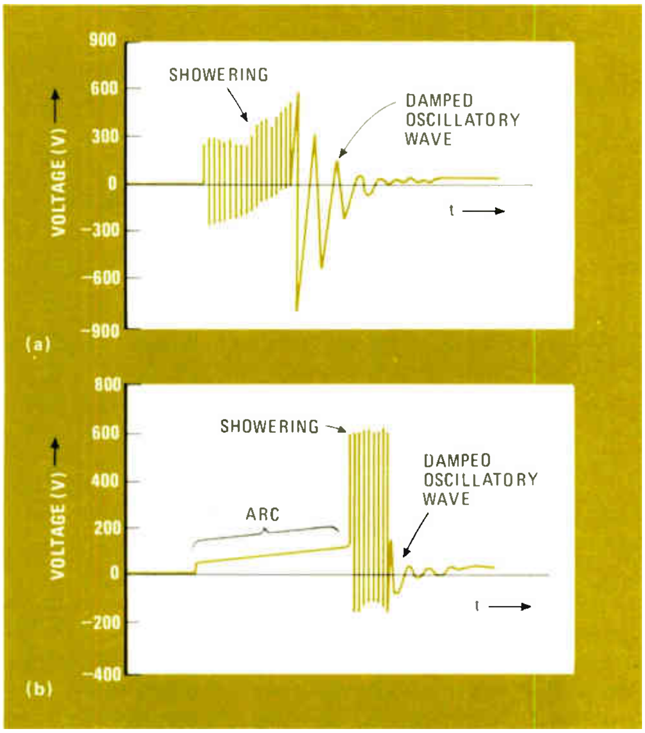
However, it should be noted that zero-switching relays trigger at the voltage zero crossing, not the current zero crossing. Because of the phase shift caused by highly inductive loads, the two crossovers don't coincide. Therefore, zero-switching relays are best suited to resistive loads in applications where their performance is not degraded by a leading or lagging power factor.

These relays were originally intended for variable-power ac applications as a noise-free substitute for phase control. Consequently, it is often assumed that a standard solid-state relay must generate rfi similar to that of variable-power phase control. To the contrary, a phase-controlled thyristor circuit turns on late in the cycle, producing an rfi pulse each half-cycle (see "Phase control and rfi").

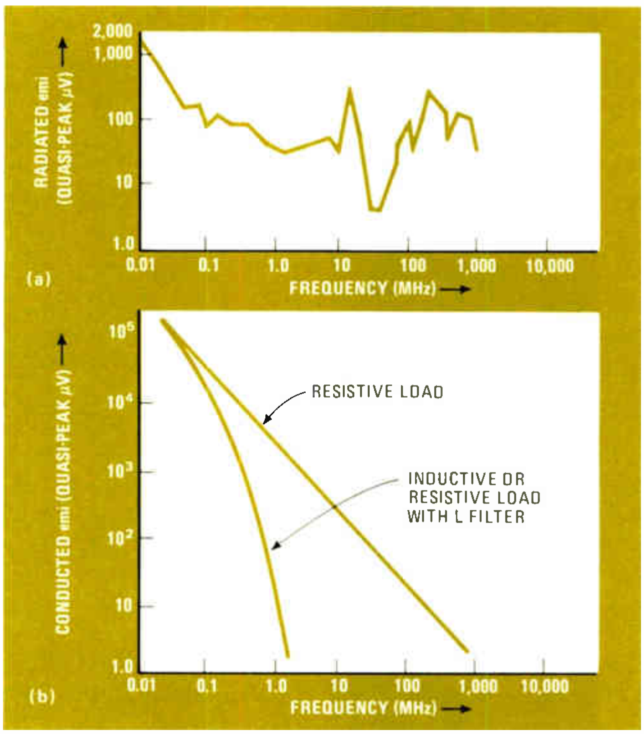
The small amount of rfi generated in a standard solid-state relay occurs only upon initial closure, during the first half-cycle of conduction. For all subsequent half-cycles, turn-on takes place near voltage 0, so that essentially no rfi is produced.

But what about turn-off, the equivalent of contact opening for an electromechanical relay? It is during contact break that an electromechanical relay generates the most significant levels of rfi, especially when interrupting current to an inductive load.

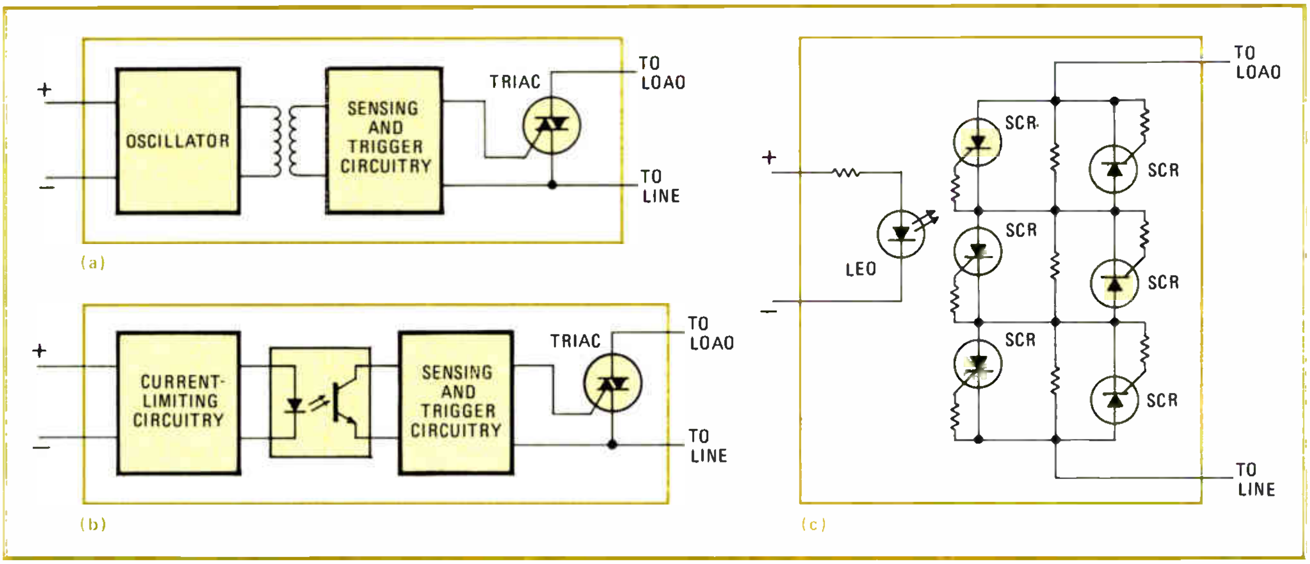
However, the thyristor-output solid-state relay could not be better in terms of turn-off rfi—the amount generated is immeasurably small. A thyristor is inherently a



3. Rfi and contact break. Unwanted switching spikes are particularly severe when an electromechanical relay switches off an inductive load. The contact voltage breaks up into a series of sharp spikes that eventually damp out. This high-frequency showering takes place even if there is no arcing (a). When arcing does occur, (b), the amplitude of the spikes becomes substantially higher



4. Jagged spectrum. With electromechanical relays, both contact opening and closure create interference that is radiated directly, as well as being conducted along lead wires, which then act like antennas and also radiate rfi. Radiated interference (a) is highly erratic, especially from 10 to 1,000 MHz. In contrast, conducted interference (b) exhibits a continuous spectrum of noise.



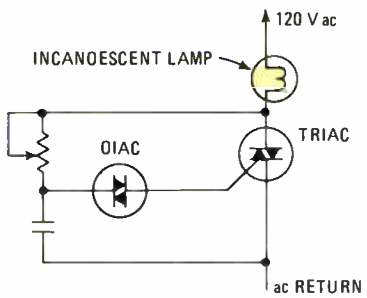
5. Standard solid state. Because they don't include optional zero-crossover circuitry, standard solid-state relays are generally about 30% less expensive than their zero-switching counterparts. Here, three versions are shown: transformer-isolated (a) and optically isolated with either a phototransistor (b) or a chain of photo-SCRs (c). The latter configuration is used to obtain very high blocking voltage.

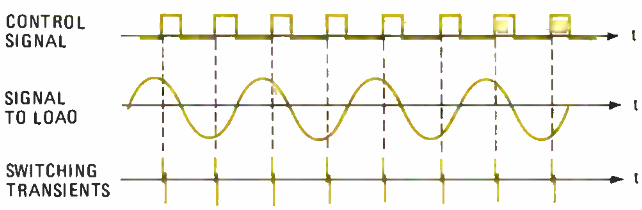
Phase control and rfi

Phase control is a widely used circuit technique for varying the root-mean-square power to an ac load. The approach is simple, but noisy, with a transient generated every time the load receives power—approximately 120 times a second.

In the circuit here, the diac and the triac are controlling the power to a tungsten-lamp load. During each half-cycle of the ac line, the capacitor charges towards the peak line voltage until the diac's breakdown voltage is reached. The capacitor then discharges through the diac, creating a trigger pulse that fires the triac. The resistor sets the point at which the triac conducts in each half-cycle.

Every time the triac turns on, radio-frequency interference occurs, as shown in the timing diagram. This rfi manifests itself as an audible 120-hertz buzz at virtually all points in the amplitude-modulated broadcast range. An unfiltered 600-watt lamp dimmer adjusted for low brilliance is a good example of the a-m hum induced by phase control.





zero-crossover device for turn-off: after the gate signal has been removed, it will not turn off until its anode current has decreased to about 0. From the standpoint of turn-off, there is no difference between a zero-crossover solid-state relay and a standard one.

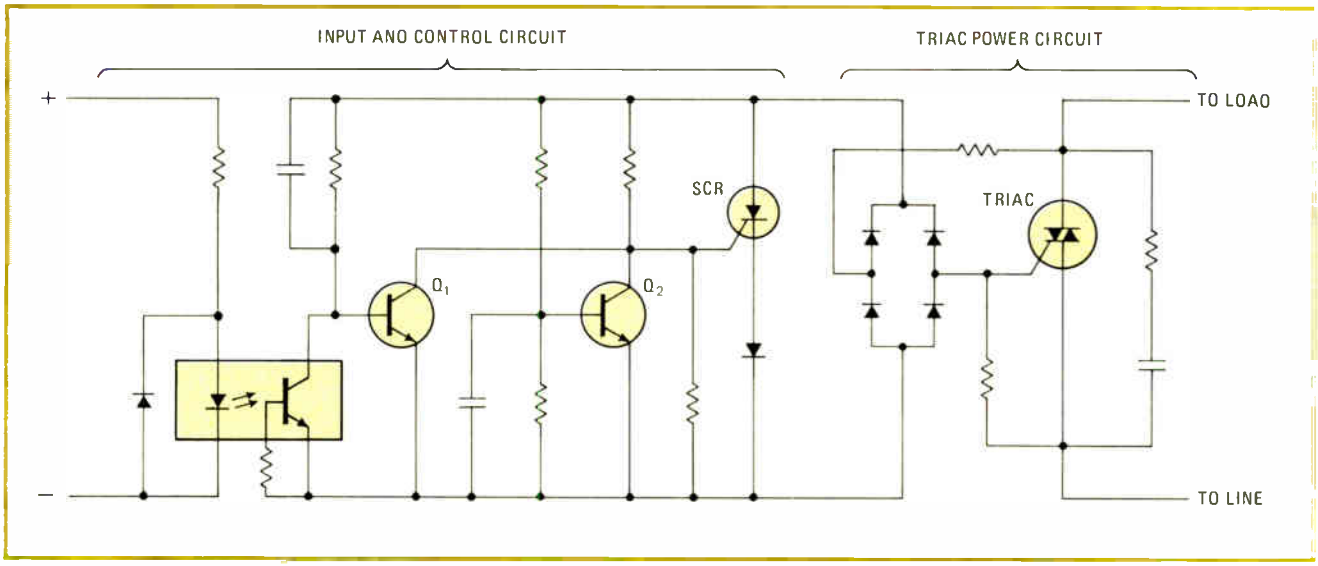
When to use zero crossover

Figure 7 compares the rfi created by both types of solid-state relays for the same control signal. Either type greatly reduces the total rfi produced during turn-on. In a zero-crossover relay, additional circuits are employed to delay turn-on in the first half-cycle of operation until the zero crossing of the voltage sine wave. For all subsequent half-cycles, operation is identical to a standard solid-state relay.

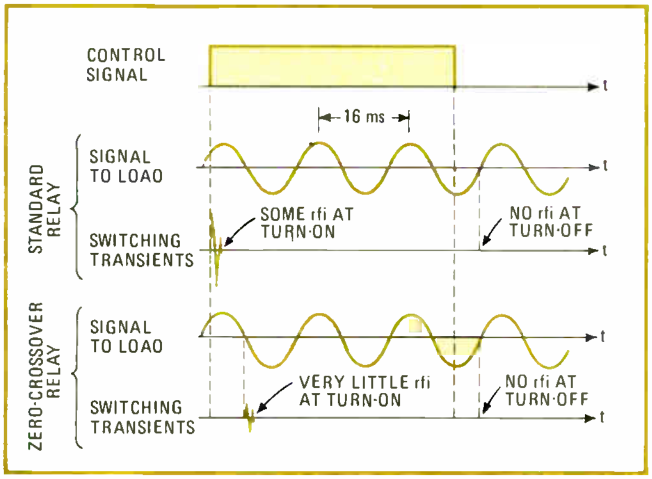
Such rfi-suppression similarities between the two relay types raises the question of the value of zero-crossover switching. However, it definitely has its place in applications where even the slightest random rfi pulse cannot be tolerated or for constant, 10-to-20-closures-a-minute switching of loads of more than a few amperes.

Zero-crossover turn-on can also be of value in certain applications where relatively high currents of 25 A or more and fairly high voltages of 440 V ac or greater are switched repetitively. In such applications, the output thyristor can be forced to dissipate an excessive amount of power at turn-on. If the thyristor is fired when the voltage sine wave is at its maximum amplitude, the voltage across the device drops from the peak line value down to approximately 1 V. At the same time, device current abruptly rises from 0 up to its peak load value.

As the voltage and current are changing levels, there



6. Zero-voltage switch. Special circuitry in zero-switching solid-state relays delays device turn-on until the driving-voltage sine wave crosses 0. In this Motorola circuit, there is a brief turn-on window between 0 and 5 V when transistor Q_1 is off, permitting the SCR to fire and trigger the triac. As long as Q_1 is on, the gate of the SCR is held at ground potential, thereby preventing it from conducting.



7. Solid-state comparison. With or without zero-crossover, solid-state relays generate only a fraction of the rfi produced by electromechanical units. Although zero-crossover versions create less rfi at turn-on than standard models, both types essentially eliminate rfi at turn-off. This is because each employs a thyristor output, and a thyristor is inherently a zero-crossover device for turnoff.

is a point at which device dissipation (the product of voltage and current) reaches a maximum. Depending on thyristor design, excessive turn-on dissipation can cause failure under long-term use.

Minimizing dissipation

To minimize the peak turn-on dissipation, conduction should occur as close as possible to the zero-crossover point. This can be achieved with zero-crossover switching, which ensures that turn-on occurs at the point of minimum power dissipation. As with rfi, turn-on dissipation becomes a factor in applications involving constant high-speed switching of high-current loads.

Zero switching is often regarded as a good technique for extending the life of incandescent (tungsten-filament) lamps, particularly in applications where they flash on and off. It is commonly believed that, if lamp turn-on is at the zero voltage point, the filament is subjected to a reduced initial surge current, thereby lowering the thermal stress to which it is subjected. However, thermal fatigue is not really the cause of lamp failure. With today's lamps, fatigue usually occurs long after the lamp has met its specified life requirements.

The two principal factors that do contribute to lamp failure are filament evaporation and mechanical shock, in which the filament is actually broken. Reducing the root-mean-square voltage driving the lamp will slow the evaporative process. The problem of mechanical shock can be dealt with through the use of filament support structures or mechanically stronger filament materials, like tungsten-rhenium.

Although repetitive on/off switching does degrade the life of fluorescent lamps, it has no measurable effect on the life of incandescent lamps. So, longer incandescent-lamp life does not result from zero-switching.

Since ac switching circuits encompass a broad variety of tasks, there's plenty of room for all three relay technologies—electromechanical, standard solid-state, and zero-crossover solid-state. Electromechanical relays will remain the choice when inexpensive multipole switching is needed or if heat-sinking limitations exist. Standard solid-state relays will eventually be cost-competitive with electromechanical types. Right now they can offer the advantages of logic compatibility, as well as improved reliability. And, of course, zero-crossover relays will continue to address the really tough switching problems. □

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Engineer's notebook

Users of microprocessors sometimes need to display a hexadecimal number that represents an address or shows the status of a process [see "Large hexadecimal display is legible from afar", June 10, p. 129]. Many readers have suggested arrangements for showing hex numbers with a standard seven-segment display. A couple of interesting techniques are described in the two following articles.

PROM converts binary code for hexadecimal display

by Franklin E. Withrow III
Massachusetts Institute of Technology, Cambridge, Mass

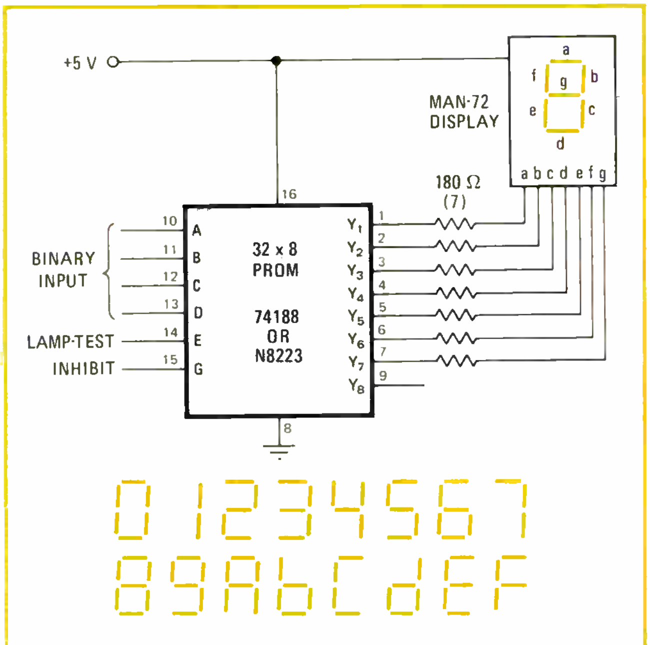
When designing and developing microcomputer systems, most engineers automatically include rows of lights to present information in binary format. However, when debugging the system, it can be frustrating and time-consuming to translate the binary data displayed into the hexadecimal format that many assemblers use. With a programable read-only memory and a seven-segment display, binary-to-hexadecimal conversion can be performed simply by hardware at very little cost over that of a binary display.

Usually, seven-segment displays are used to display only the numerals 0–9. In addition, they can also display the needed hexadecimal characters A–F; however, not all letters can be represented in upper case. The figure shows the segment patterns displayed for each hexadecimal digit. One caution that must be exercised is to note the difference between the number "6" and the letter "b".

To implement the hexadecimal-to-seven-segment decoder, a 74188 or N8223 PROM is used. Since the device has open-collector outputs, the light-emitting diodes in the display can be driven directly with a suitable current-limiting resistor. The PROM outputs should not be allowed to sink currents greater than 12 milliamperes. Each of the seven segments in the display is driven by a separate output of the PROM (one output is unused). The schematic for a single hexadecimal digit is given in the circuit diagram.

Locations 0–15 of the PROM are used to store the information that performs binary-to-hexadecimal conversion. For each word, a 0 in a bit position turns on the display segment at the output; if the bit is a 1, the segment is off. If locations 16–31 are left unprogramed (all 0s), the most significant address line performs a lamp-test function. When this line is high, a word in the range 16–31 is addressed and all segments of the display will light.

The PROM should be programed in accordance with the procedure outlined on the device's data sheet. An automatic programing machine, which reads punched cards that tell it the desired output word for each address, does the programing in seconds. The bit pattern and function table for the decoder are given in the accompanying table. ☐



TRUTH TABLE AND PROGRAM FOR THE HEXADECIMAL DISPLAY

INHIBIT	LAMP TEST	B8	B4	B2	B1	DISPLAY	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8
							PROGRAM IN MEMORY							
0	0	0	0	0	0	0	0	0	0	0	0	0	1	X
0	0	0	0	0	1	1	1	0	0	1	1	1	1	X
0	0	0	0	1	0	2	0	0	1	0	0	1	0	X
0	0	0	0	1	1	3	0	0	0	0	1	1	0	X
0	0	0	1	0	0	4	1	0	0	1	1	0	0	X
0	0	0	1	0	1	5	0	1	0	0	1	0	0	X
0	0	0	1	1	0	6	0	1	0	0	0	0	0	X
0	0	0	1	1	1	7	0	0	0	1	1	1	1	X
0	0	1	0	0	0	8	0	0	0	0	0	0	0	X
0	0	1	0	0	1	9	0	0	0	1	1	0	0	X
0	0	1	0	1	0	A	0	0	0	1	0	0	0	X
0	0	1	0	1	1	b	1	1	0	0	0	0	0	X
0	0	1	1	0	0	C	0	1	1	0	0	0	1	X
0	0	1	1	0	1	d	1	0	0	0	0	1	0	X
0	0	1	1	1	0	E	0	1	1	0	0	0	0	X
0	0	1	1	1	1	F	0	1	1	1	0	0	0	X
1	X	X	X	X	X	(OFF)	1	1	1	1	1	1	1	1
0	1	X	X	X	X	8	0	0	0	0	0	0	0	X

1 = HIGH   0 = LOW   X = DON'T CARE

Remember the hex symbol. Binary inputs to the PROM produce a seven-segment representation of hexadecimal-code symbols. The PROM costs about $3, and can be programed quickly at practically no cost if an automatic programing machine is available.

Decoders convert binary code for hexadecimal display

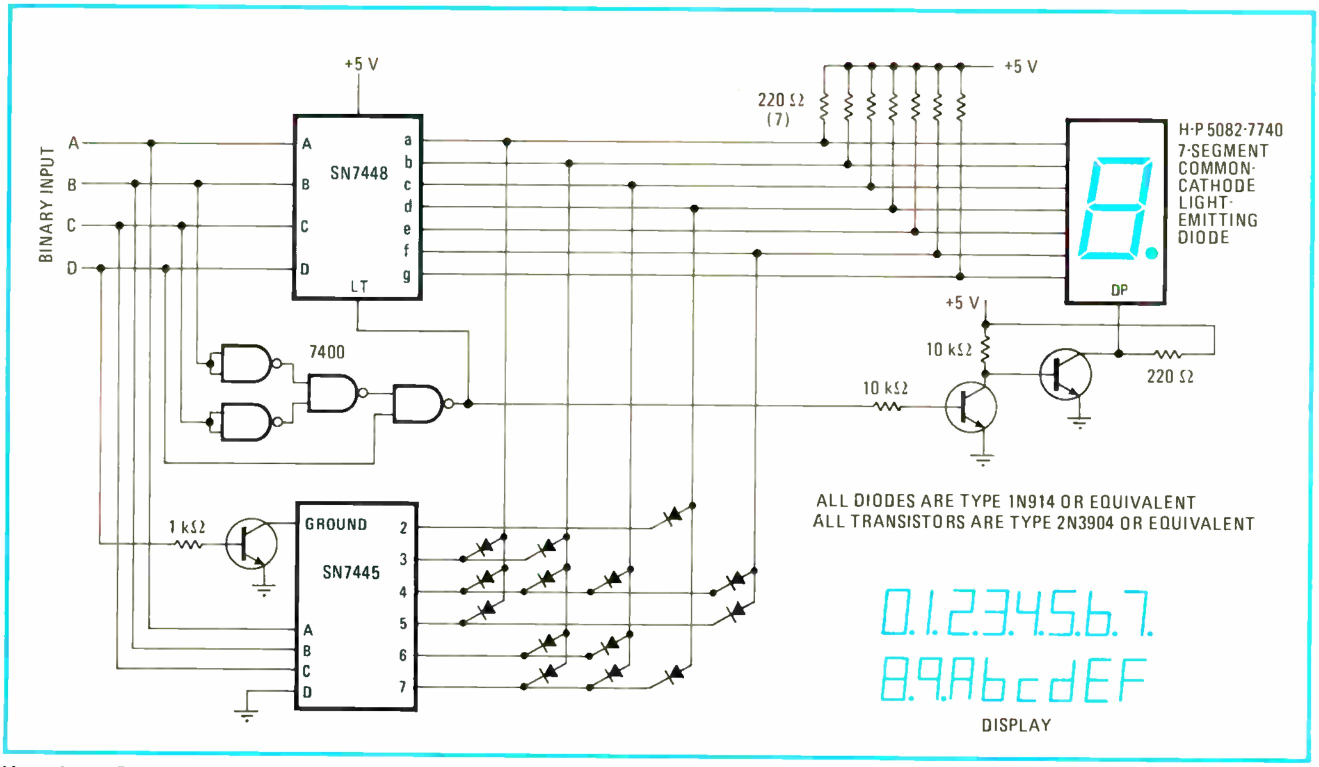
by Robert F. Starr
National Oceanographic Instrumentation Center, Washington, D C

Hexadecimal code symbols can be shown cheaply and easily on a regular seven-segment display by two decoder/drivers and some logic circuitry. To keep the hex digits A through F completely recognizable, the circuit described here generates both upper-case and lower-case letters. The 7448 seven-segment decoder/driver displays a symbol for "6" that is identical to a "b". Therefore, the decimal point of the display is activated for the numbers 0 through 9, and extinguished for the letters A through F.

The circuit operation is quite straightforward. For binary inputs to the 7448 from 0000 to 1001 (0 to 9), the 7448 functions normally, displaying the appropriate digit on the light-emitting-diode display. As soon as the binary input exceeds 1001, the LT (Lamp test) input on the 7448 is brought low, lighting all segments, and extinguishing the decimal point (DP) on the LED. In addition, as soon as the D input (most significant bit) on the 7448 goes high, the 7445 binary-coded-decimal-to-decimal decoder/driver turns on.

With the D input of the 7445 grounded, the device sees only the three least significant bits of the input. When the binary input is 1011, for example, the 7445 sees a 011 (3) and brings the 3 output low. This output is decoded by the diode matrix, which turns off segments a and b of the LED display, forming a "b" on the display. The process is similar for all other binary inputs from 1010 to 1111 (A, c, d, E, and F).

An H-P 5082-7740 LED display is shown here, but other types can be used. For most of the larger displays, it may be necessary to pull the seven-segment lines to ±5 volts through 220-ohm resistors to achieve the desired brightness. □



Hex signs. Binary inputs produce hexadecimal code on a standard seven-segment display with this circuit. To emphasize distinctions between numerals and letters, a decimal point is activated for numbers 0 through 9, as shown. Cost of parts (not including LED display) is less than $5. For more than one digit, the inputs can be multiplexed. Pull-up resistors may not be required for small displays.

Electronic load aids power-supply testing

by M.J. Salvati
Sony Corp. of America, Long Island City, N.Y.

An electronic load for testing the static and dynamic characteristics of small- to medium-sized power supplies can be assembled for a parts cost of about $12. The tests include voltage regulation (by either static or dynamic techniques), ripple vs current drain, transient response, and temperature vs current drain.

The device can provide a static (dc) load of 1–250 milliamperes or a dynamic (ac) load of up to 1 ampere

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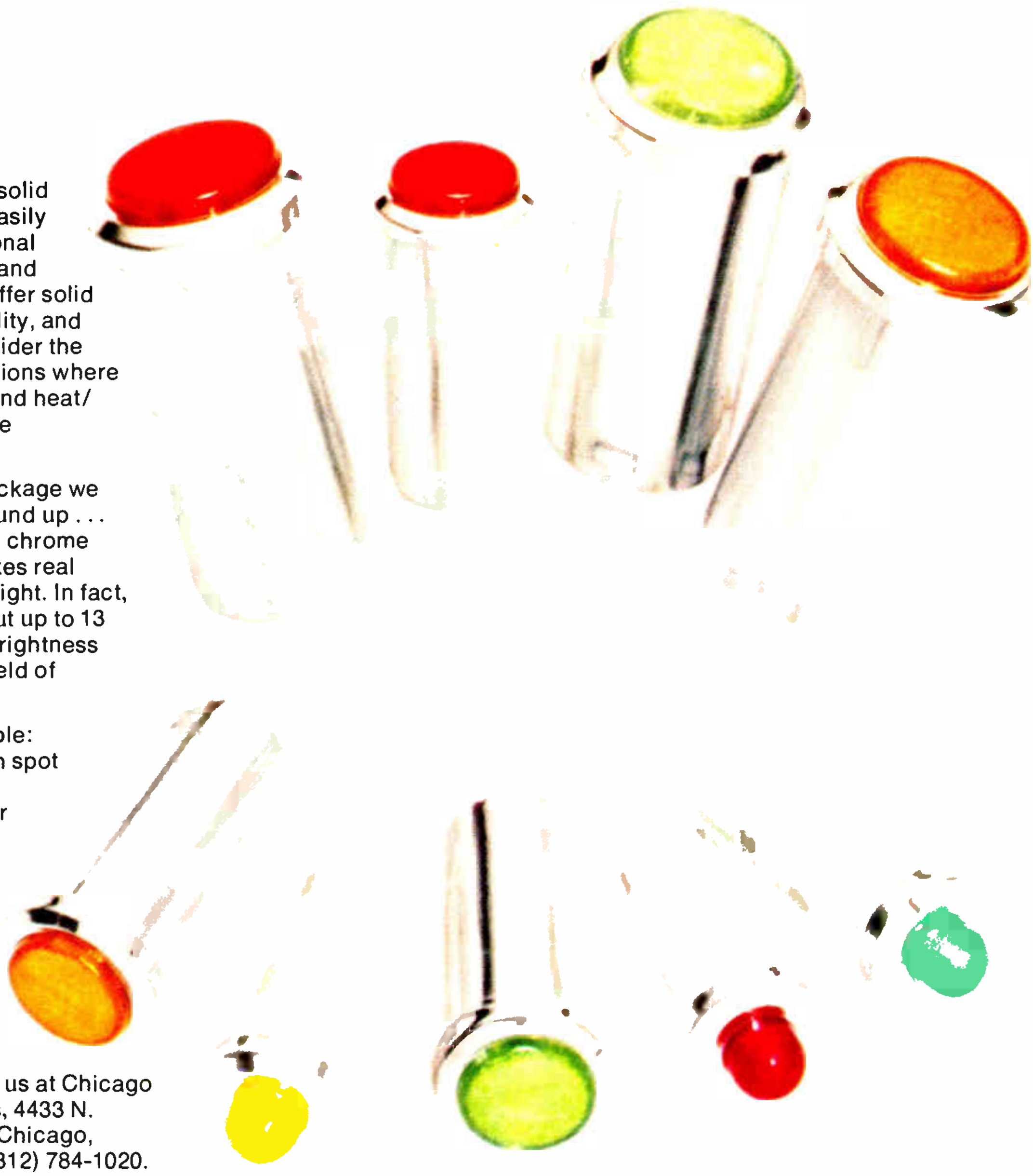

Yes. We call it the ULTRALITE.

These high-efficiency solid state indicator lights easily rival current conventional models for brightness and efficiency. Plus, they offer solid state longevity, durability, and low-power drain. Consider the advantages in applications where life, shock, vibration, and heat/ power consumption are crucial factors.

The key is a unique package we designed from the ground up . . . from chip to functional chrome housing. The result takes real advantage of the LED light. In fact, our larger lamp puts out up to 13 mcd! And along with brightness comes an incredible field of indication up to 160°.

Three sizes are available: standard LED, .30-inch spot diameter, and .40 spot diameter. Order with or without resistors. Colors are red, amber and green. Options include voltage, current, lenses. and more.

ULTRALITE! You really have to see it to believe it. Contact us at Chicago Miniature Lamp Works, 4433 N. Ravenswood Avenue, Chicago, Illinois 60640. Phone (312) 784-1020.

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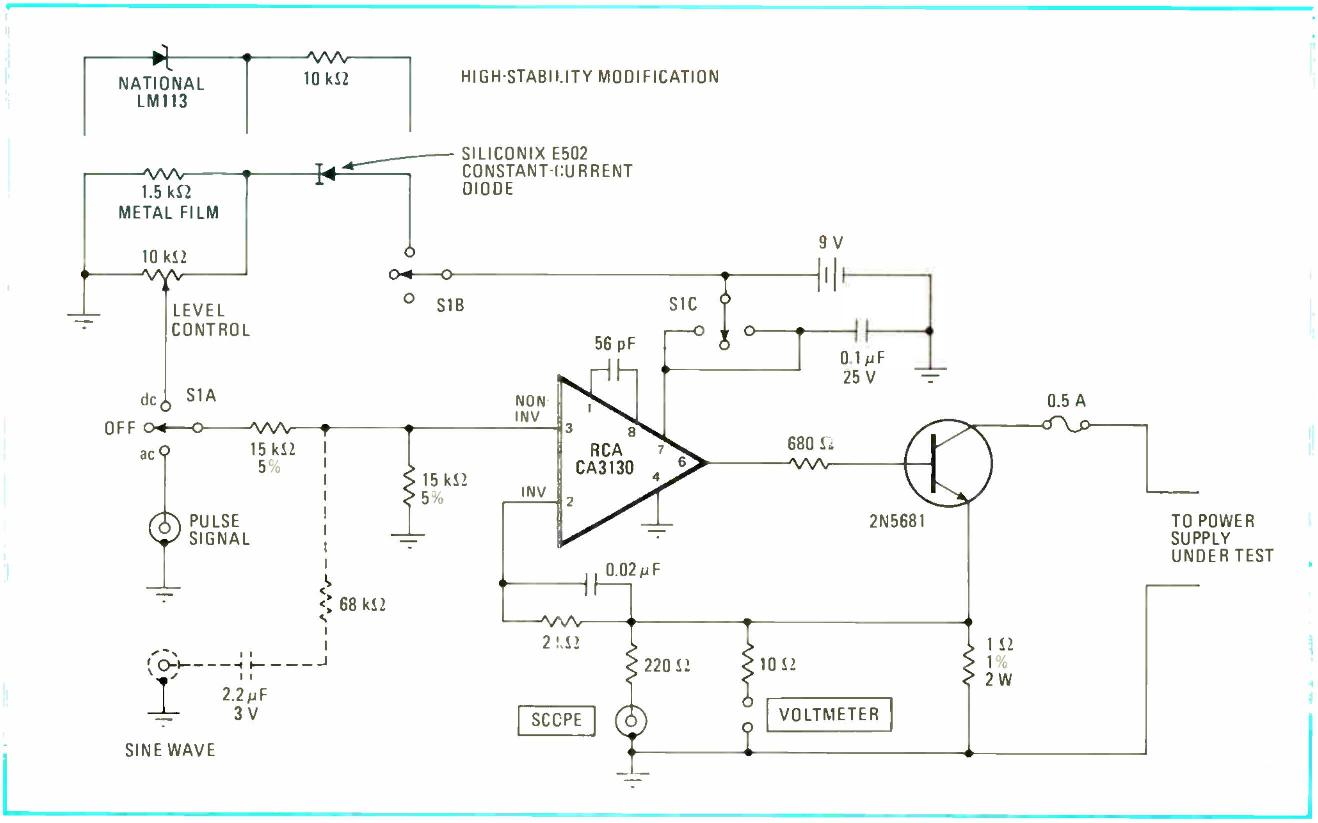

1. Electronic load. Characteristics of a power supply are tested with this circuit, which controls current delivered by the supply. Regulation, ripple, transient response, and temperature effects can be measured at currents up to 1 A peak or 0.25 A dc and voltages of 1.5 to 100 V.

peak current on power supplies with output voltages anywhere from 1.5 to 100 volts. The current drain in either mode is independent of output voltage of the power supply under test. The pulse-repetition rate in the ac mode can reach 30 kilohertz for a fast-rise pulse and 200 kHz for a sine wave. The average power dissipation is limited to 3 watts continuous and 5 W intermittent because of the small size of the switched transistor shown in the circuit diagram of Fig. 1. A higher-power transistor can be used if necessary, but switching speed may suffer.

As the diagram shows, the tester is essentially a variation of the classic current sink, one that can be modulated and in which the load current through the transistor is controlled by the CA3130 operational amplifier. The ability of the CA3130 to work from a single supply with ground-referenced input and its very low current drain allow the tester to be powered by a single 9-V transistor-radio battery. Because the device is self-powered, it can be used for testing very-low-voltage power supplies.

A switch at the input of the op amp selects either dc or pulsed operation of the supply. The dc mode uses an E502 constant-current diode in the reference-voltage source. It draws only 0.43 mA from the battery, and has a temperature coefficient close to zero. The voltage thus dropped across the level-adjustment potentiometer is very stable. If even greater stability is desired, the E502 and 1,500-ohm resistor can be replaced by the more expensive but superior LM113 voltage-reference diode and 10-kilohm resistor as shown in the diagram. The modification shown in dashed lines allows superposition of sine-wave modulation on the dc bias for tests of output impedance vs frequency.

2. All packed up and ready to go. Complete electronic load circuit, including the 9-volt battery that powers it, is housed in a standard 3-by-2-by-5¼-inch aluminum box. Connectors can be seen.

The current level is set by means of the level control in the dc mode and monitored by a dc voltmeter or a dc scope. The peak current level in the pulsed (ac) mode depends on the input-signal amplitude, and is monitored on a scope. The ratio of output current to input signal in this mode is 1 A/2 V peak. The conversion ratio at the scope and voltmeter terminals is 1 mV/mA in either mode. □

Engineer's Notebook is a regular feature in Electronics. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.

A new round of 3½-digit multimeters is beginning to bow

Look for a surge of introductions of 3½-digit multimeters over the next few months. The new round has already been kicked off by Data Precision's $189 model 175 [*Electronics*, June 10, p. 44] and Hewlett-Packard's $335 model 3435A [*Electronics*, June 24, p. 125]. **Large-scale integration and low-cost, but accurate, analog-to-digital converters are bringing the price down.** They also allow the addition of features that make the units easier to use, such as auto-ranging combined with accurate readings and HP's "hold" feature, with which the user can press a button on the probe to hold the reading on display.

Pc boards can use low-cost plastic found in high-impact cases . . .

Polysulfone, a low-cost, strong plastic that is used in high-impact cases for calculators and instruments, can also be used as a reliable substrate for pc boards, according to G. F. Jacky of Tektronix, Beaverton, Ore. He says his company used about 9,000 sq. ft. annually of copper-clad polyphenelene-oxide material (PPO), which costs $15 to $30 a square foot. By switching to plated polysulfone and using a semiadditive process, **the company was able to save about $10,000 a month while maintaining an 80% yield on the boards.** The polysulfone is even available in sheet form at most hardware stores.

. . . and can be cleaned by CO_2 pellets

Cleaning pc boards by sandblasting often creates further clean-up problems when you have to dispose of the blasting medium. But solid CO_2 pellets, says Calvin C. Fong of Lockheed-California, Burbank, can work as well as sandblasting in removing rosin flux and other contaminants, **and they conveniently disappear as they melt.**

RC combination lifts shift registers out of all-zero mode

One of the problems in generating pseudorandom sequences with shift registers, such as for white-noise tests, is that the shift register can occasionally get into an all-0 mode. However, there's a simple way to avoid this, says Matt Fichtenbaum of GenRad, Concord, Mass. **Instead of making a direct connection of the feedback path to the shift-register input, use a series capacitor and tie the shift-register input to positive voltage through a resistor.** If the shift register assumes an all-0 state so that the feedback line stays low, the capacitor will charge up through the resistor and eventually pull the input high, sending a logic 1 into the register to start it on its pseudorandom sequence again. Fichtenbaum says an RC combination of 1 megohm and 0.22 microfarad works nicely with a 200-kilohertz clock.

Motorola Semiconductor puts data sheets onto microfiche

Motorola Semiconductor Products Inc. has come up with a novel way to furnish its product data with a minimum of paper—provided you have access to a microfiche viewer. **Every month, technical data for all products described in Motorola's Semiconductor Data Update publication will be put on microfiche and sent free to interested engineers.** If you need a hard copy of one of the data sheets, you can get it from a Motorola sales office. But, if you must have hard copies of all the data sheets, you must subscribe for $12 a year.

Stephen E. Scrupski

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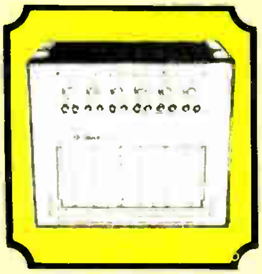
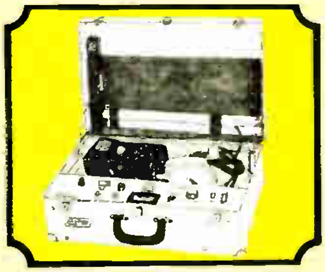
Switch to No.1

Circle 111 on reader service card

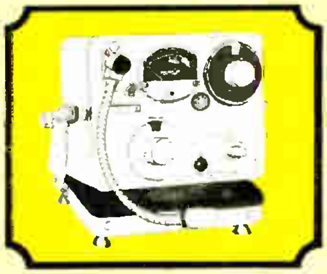
The Ten Most WANTED INSTRUMENTS



Brush Oscillograph 260

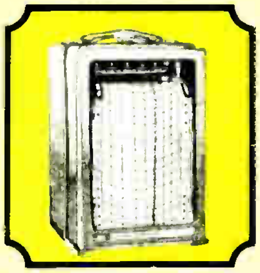


Associated Research
Fault Finder



General Radio
Sound Level Analyzer

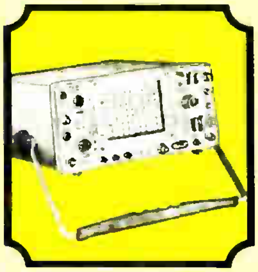
Honeywell Tape Recorder



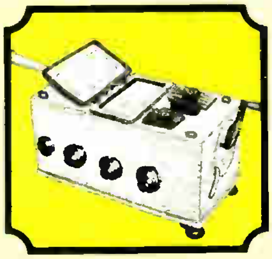
Esterline Angus Chart Recorder

Associated Research
Insulation Tester

Kaye Data Acquisition System



Tektronix Oscilloscope



Biddle Megger

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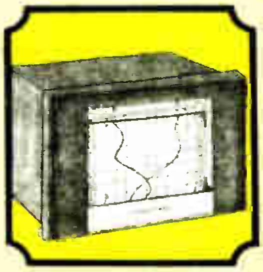

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Potentiometer is linear within 2%

Sensing probes for real-time laser-trimming are key to semi precision pot; Bourns also develops 10-turn precision unit and others for model 80 family

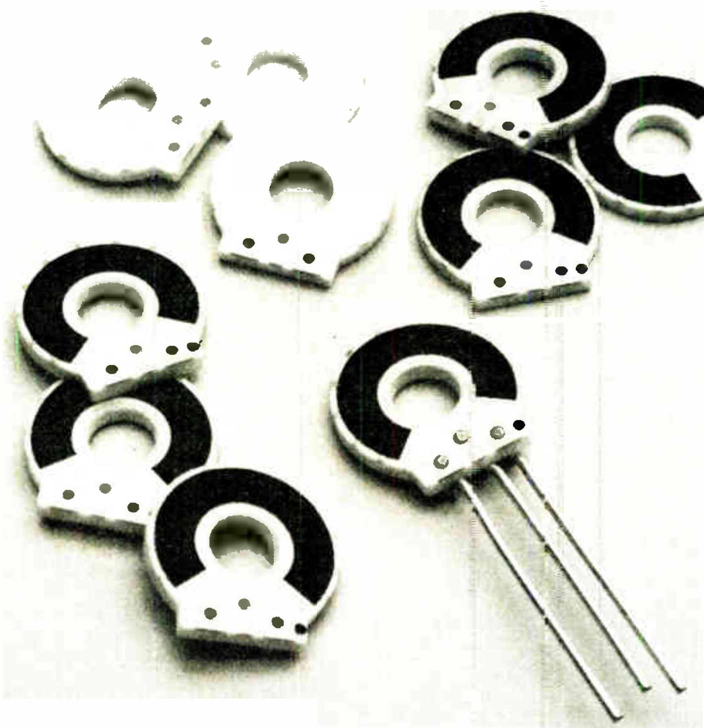
by Larry Waller, Los Angeles bureau manager

Instrument designers have usually had two options when choosing standard single-turn potentiometers: precision models offering linearity within 0.5% to 1% or cheaper units in the 5% range. This amounted to a gap in available potentiometer product lines reflected in a price of $5 per unit at the precision level down to $1 for the high-volume industrial units.

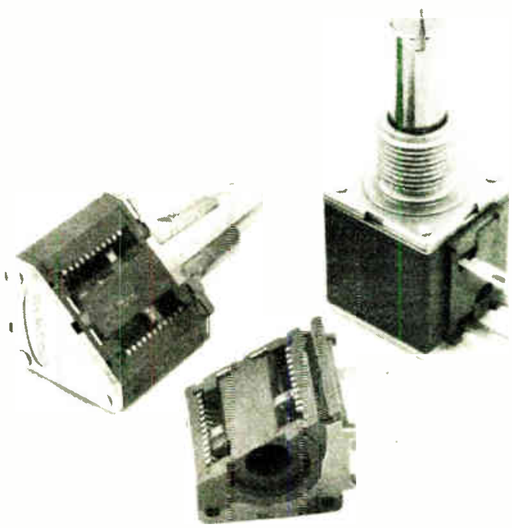
To fill what it says is a promising niche in the market, Bourns Inc. has developed a "semiprecision" potentiometer, to be introduced in August. This unit, the model 87/88, offers zero-based linearity within 2%. It uses a cermet element and sells for $2.50 each in 10,000-piece orders. A conductive plastic model, providing linearity within 3%, costs $2 each in comparable quantities.

Manufacturing a potentiometer combining these price-performance features is described by Ken Leebelt, product manager for control and precision,as "more evolutionary than anything else." The key is an innovative production technique. Fixed-contact sensing probes measure basic linearity and resistivity precisely enough so that laser trimming can take place in real time. This replaces moving contacts and hand-trimming that is slower and less accurate. "We've had the concept for several years," Leebelt remarks, "but what we had to do was develop the equipment to build it."

To enable simultaneous probing and laser-trimming of the potentiometer element, Bourns engineers developed a new way of determining its exact position by putting 10 reference taps or voltage pickoffs, on the outside diameter of the sub-



Before and after. Photo above shows cermet elements of Bourns model 87/88 semiprecision potentiometer. Elements are shown before (upper left) and after they have been laser-trimmed in a novel production technique



Squared away. At right is the 10-turn precision potentiometer from the model 80 family. Shown here both as a complete unit and in cutaway form, the new device is housed in a square, instead of the usual round, package to allow for closer spacing.

strate. "We print them at the same time the end terminals are put on," says Del Singleton, a senior engineering specialist, who led the design effort. "By doing this, we know precisely where each of the taps is located in relation to the element." Using these taps as fixed-contact points not only eliminates sensing-measurement and positioning errors, but also the uncertainty of where the end terminals are located.

Singleton says that further refining the process could hold nonlinearities "down to the 1% area." But Leebelt observes that since the semiprecision gap will be filled by the new model, market demand might not actually justify such an improvement.

Other features of the 87/88 cermet model include a 3% resistance tolerance in a range from 250 ohms to 2.5 megohms; theoretical electrical travel of 250° ±5°; roll-on, roll-off of 0.25%; and rotational life of 100,000 cycles. Specifications for the conductive plastic element are similar, except for a resistance tolerance of 5%. Both types are in packages that measure ⅝ inch square.

Another new model in the Bourns 80 line is a 10-turn precision pot that has square packaging instead of the usual round shape. The model 83/84 (odd number for printed-circuit mounting, even number for solder lugs) measures 0.675 in. square as against the usual 0.875-in. diameter, allowing almost ¼-inch closer spacing in panel applications. It sells for about $4 in quantities of 1,000. The board-mounting feature, which Leebelt calls "the first available on a precision pot," is offered as an additional way to cut assembly costs. The 83/84 has a resistance tolerance of ±5% and independent linearity within ±0.25%. Rotational life is rated at 1 million shaft revolutions.

Rounding out current new products is the model 85/86 control and switching potentiometer, priced at about $2.05 each in quantities of 1,000.

With two other new potentiometers in the model 80 family reaching the market in late summer, Bourns is pursuing its goal of marketing a compatible family for all applications, Leebelt says. An important feature designed into the entire family is "consistency of tactile feel"—with shaft-torque control varying only 0.3 to 2.0 ounce-inches unit-to-unit. Up to four modules can be ganged on a concentric shaft, with this torque range still maintained, he claims.

Bourns introduced the first of its model 80 family last year, and sales are ahead of projections, Leebelt says, particularly to instrument firms and builders of professional audio equipment. A company official predicts that the 80 family will account for a substantial portion of Bourns's total potentiometer sales in the next two years.

Bourns Inc., Trimpot Products Division, 1200 Columbia Ave., Riverside, Calif. 92507. Phone (714) 684-1700 [338]

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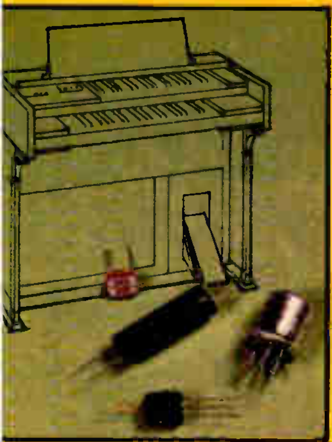
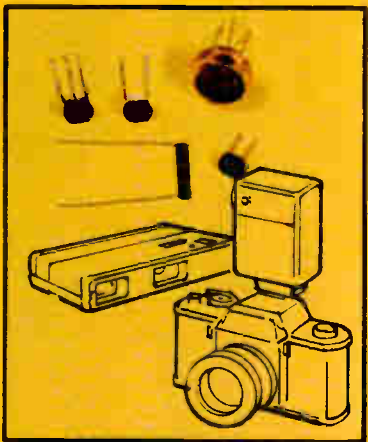


Electronic Organs

ED or lamp/LDR Vactrols for au- io, and CdS cells for swell pedal ontrols.



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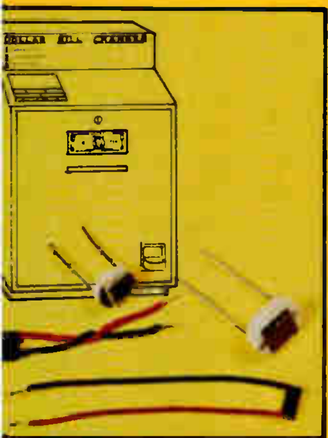
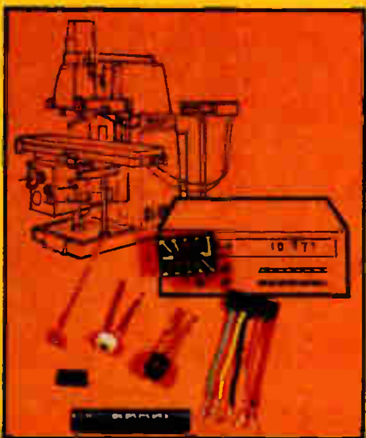


Dollar Bill Changers

ilicon photovoltaic cells analyze ptical characteristics.



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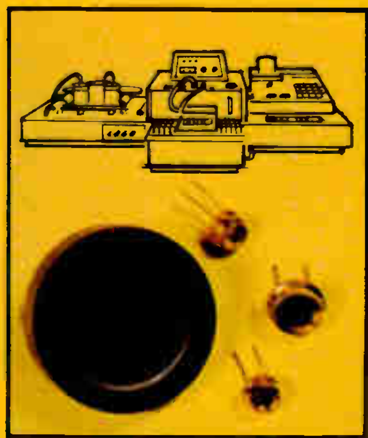

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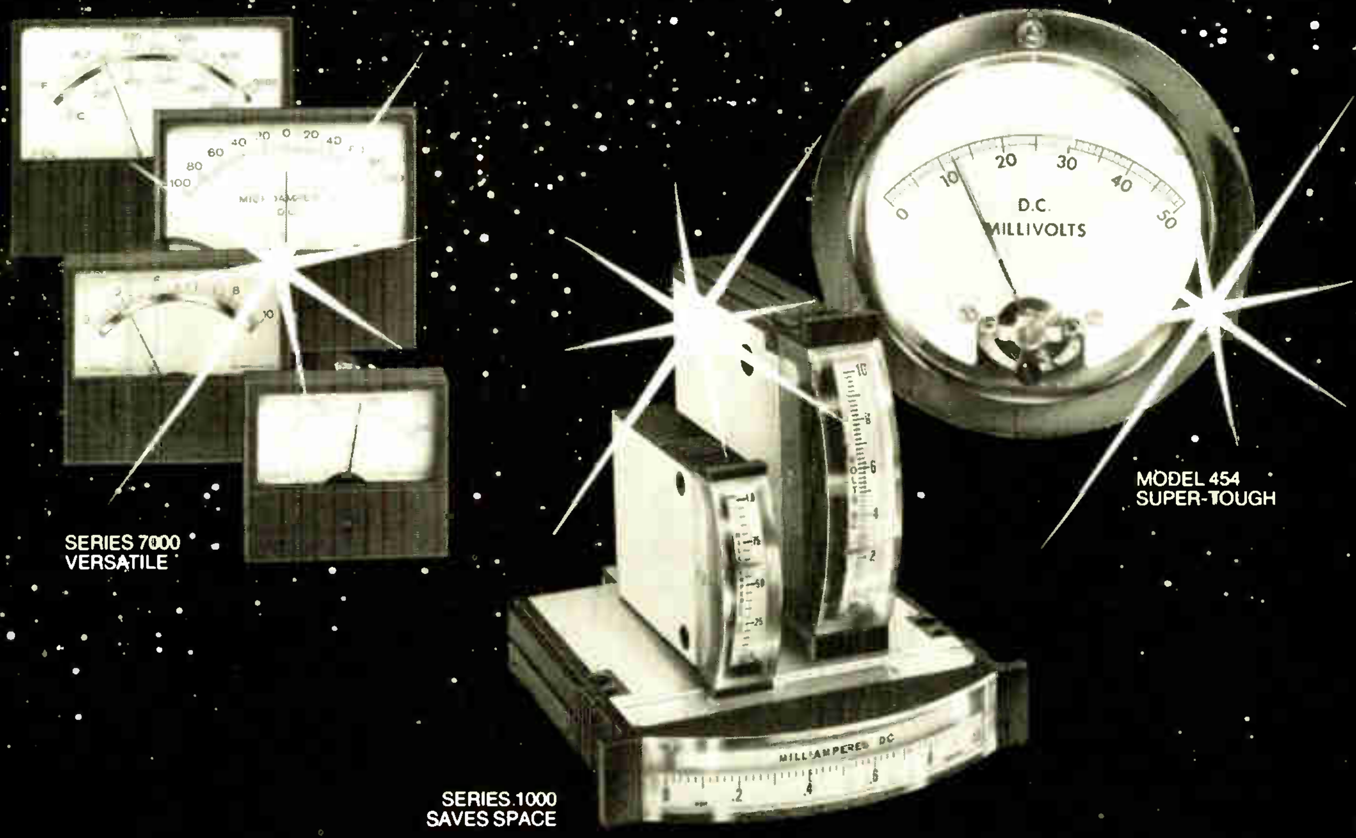

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LFE CORPORATION Process Control Division

Smart memories speed processing

Novel architecture permits general-purpose processor and interface modules to handle radar, sonar, other signals in computerized network

by Lawrence Curran, Boston bureau manager

Signal processing of data such as radar or sonar signals is usually done with hard-wired processors dedicated to each portion of the task, ranging from sophisticated filtering to fast-Fourier transforms. Now a company with considerable experience in such signal processing has developed a system design that allows less specialized processors to do those tasks in a network that also employs an intelligent hierarchical memory system.

Signal Processing Systems Inc.'s new Compass line is a set of memory, and processing, and input/output modules that can be connected into networks of increasing capability. Each network contains one host computer, such as a Digital Equipment Corp. PDP-11 model, for which SPS provides the interface to the Unibus structure, plus the company's own SPS-41 or SPS-81 processors. The firm will also supply interfaces to other host computers.

Joseph Fisher, president of SPS, points out that a fast-Fourier transfer alone might require a full second to complete in a PDP-11, and 35 milliseconds in a CDC 6600, while it can be done in a millisecond or less in the Compass system.

It's the design of the smart memory hierarchical architecture that Fisher feels makes the Compass family particularly powerful and flexible. Typically, the system uses various-sized fast memory modules as well as the host computer's memory. (The company sells only semiconductor memories with its systems, but can connect them to the host-computer memory even if it employs core storage.)

An intelligent interface—hard-wired logic associated with the memory that controls addressing of data—lies between the memory and the I/O processor and arithmetic processor. It generates memory addresses for data coming from the arithmetic processor, thus freeing the I/O processor of that task and allowing it to concentrate on its own major functions—formating of data coming in and out of the arithmetic processor and certain decision-making functions. With the smart interface, the I/O and arithmetic and memory accessing can proceed independently and in parallel, speeding the system.

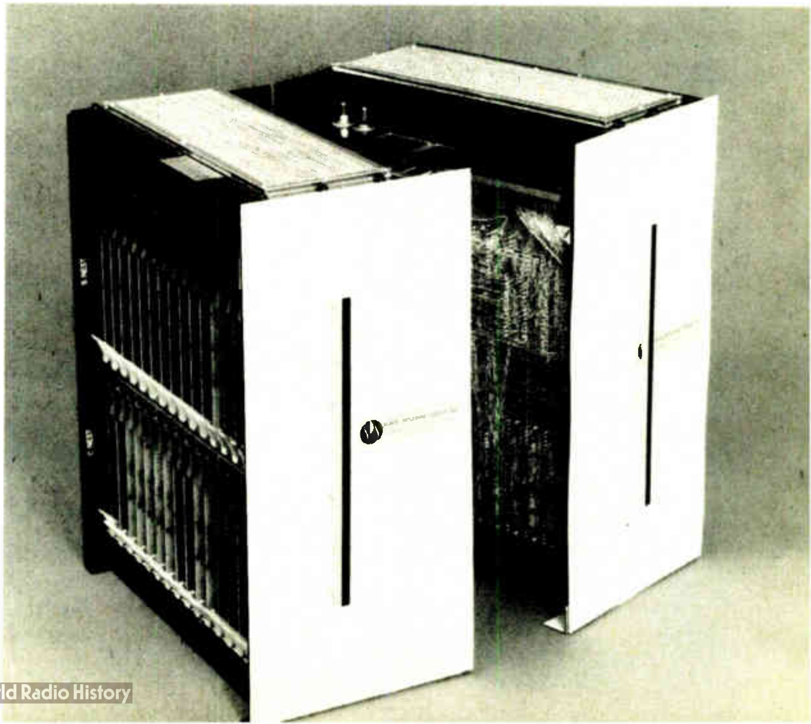
A typical Compass system might include, in addition to the host processor, two to four of the company's SPS-41 or SPS-81 processors, two large memory modules, and one or two smaller memory modules per processor that are faster than the large memory modules. The larger ones will hold up to 256,000 words of 32 bits and offer access times of 500 nanoseconds. All memory modules are arranged in pages, and the smaller memories can have access as quickly as 167 ns, with as little storage as 1,024 words.

Generally, Fisher says, the smaller memories are dedicated to a given processor within this network, which might be performing recursive filtering calculation. "But the programs that access it are the same as those that access the big memories," he notes.

Fisher says of the Compass system's mechanical design—a clamshell structure accommodating one to four nests of 20 (see photo) to 40 circuit boards in each side of the clamshell: "We get a lot of modularity but there's not a lot of cabling that would cut into speed."

A minimal system, consisting of one memory module, a processor module, an I/O module and a host-interface module, plus a 6-megahertz 32-bit-wide bus, will sell for $27,000 and can be expanded as the user's needs grow. Delivery of the Compass system will begin next January.

Signal Processing Systems Inc., 223 Crescent St., Waltham, Mass. Phone (617) 891-0400 [339]



Components

Reed relays handle 20 watts

Reed relays are not usually thought of as power devices, although some are rated for 10 watts or more. However, the R series of reed relays from Arrow-M Corp. can handle up to 20 W at 1 ampere, and some versions are equally well suited for use in dry circuits with signal levels as low as 100 microamperes.

The key to this kind of performance is the contact design. In conventional reed relays, a pair of reed blades is suspended inside a sealed glass capsule. In contrast, the series R devices use only a single reed blade in conjunction with a separate pair of stationary contacts. The contact assembly forms a single-pole double-throw switch (form C contact arrangement).

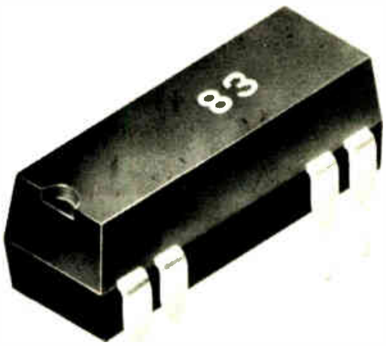
The new units, which are about the same size as conventional glass-encapsulated reed relays, are supplied in gas-filled sealed plastic housings. Designed for a billion mechanical operations, the series R devices are quite sensitive—their pull-in power requirement is in the range of 40 to 100 milliwatts, enabling them to be driven directly by a transistor.

Magnetically shielded versions provide protection against electromagnetic interference. Both latching and nonlatching models are available.

In quantities of 1,000, prices of the relays start at $2.11 each. Delivery is from stock to within six weeks after receipt of order.

Arrow-M Corp., 250 Sheffield St., Mountainside, N.J. 07092 [343]

Three-pole reed relay fits in standard DIP

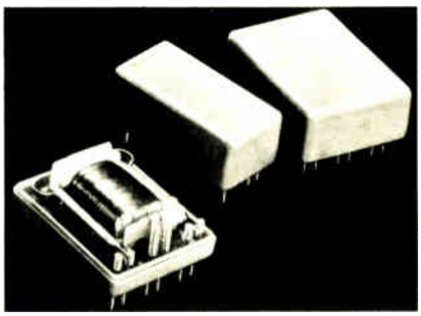


Believed to be the first reed relay housed in a dual in-line package to offer three poles, the series 83 uses a standard eight-pin TO-116 terminal grid to fit all standard DIP sockets. Because it has three poles, compared with a maximum of two for previous units, the series 83 reduces required printed-circuit board space and per-pole cost. Contact rating is 10 watts with a maximum switching voltage of 100 volts dc and a maximum switching current of 0.5 ampere. Three standard coils are available: 150 ohms for 5-volt applications, 450 Ω for 12-V, and 750 Ω for 24-V dc.

Gordos Corp., 250 Glenwood Ave., Bloomfield, N. J. 07003. Phone Stephen Kunnmann at (201) 743-6800 [344]

Low-profile relay is rated from dry circuit up to 10 A

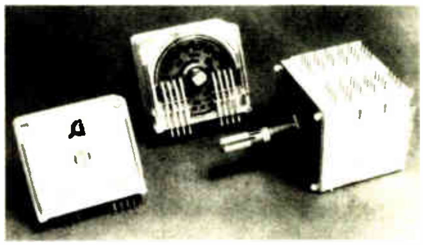
Offered in both single-pole, double-throw and double-pole, double-throw configurations, a low-profile subminiature relay uses unusual multiple convoluted contacting surfaces for ratings from dry circuit up to 10 amperes ac (resistive load) depending upon voltage. The series 1475 DC flat-pack devices are engineered for use on printed-circuit boards with 0.6-inch spacing between boards. Terminal spacing is on a standard 0.1-in. grid. The relays can be wave- or hand-soldered at up to 650°F for a normal soldering time without damage. The spdt version measures 1.105 by 0.605 by 0.437 inches, while the dpdt unit measures 1.105 by 0.905 by 0.437 in.



Guardian Electric Manufacturing Co., 1550 West Carroll Ave., Chicago, Ill. 60607 [347]

Logic switch has up to 60 programed positions

Designed as an alternative to conventional rotary switches for the manual switching of complex binary codes, the P/rel (for programable rotary encoded logic) switch is fully programable up to 60 detent positions. Special features include modular stacking for multilayer operation and snap-together construction. A specially processed printed-circuit disk provides full programing to any truth table and allows the use of any code.



Standard Grigsby Inc., Sales Dept., 920 Rathbone Ave., Aurora, Ill. 60507. Phone (312) 897-8417 [346]

Five-ampere aircraft relay weighs only 0.44 ounce

A relay for switching aircraft power (28 volts dc and 115/200 V ac at 400 hertz) is rated at 5 amperes and weighs only 0.44 ounce. The two-pole, double-throw model E205 measures 0.81 by 0.41 by 0.64 inches in its simplest mounting configuration. A companion unit, the model E405, is similar except that it is a four-pole device measuring 0.81 in. wide instead of 0.41 in. and weigh-

ing 0.85 ounce. Both units have a maximum operating time, at 25°C, of 7 milliseconds, and a maximum release time of 5 ms. Life at rated load is at least 100,000 operations.

Deutsch Relays Inc., 65 Daly Rd., East Northport, N. Y. 11731. Phone (516) 864-6000 [345]

Front-panel DIP switches have toggle-type actuators

Designed specifically for front-panel applications, the Toggle-DIP is a DIP switch that can be operated without having to use a ballpoint pen or similar small, pointed object. Life-rated at 50,000 operations at logic levels or 25,000 operations at 125 milliamperes and 30 volts dc, the switches are offered in single-pole, double-throw and double-pole, double-throw configurations. A single Toggle-DIP may contain from one to four spdt switches or one or two dpdt switches. The toggle-type actuators are on 0.2-inch centers in the spdt version and on 0.4-in. centers for the dpdt. Typical 100-piece pricing for the Toggle-DIP is $2.73 each for the four-switch spdt unit and $2.80 each for the two-switch dpdt version. Prototype quantities are available from stock; delivery time for production quantities is six to seven weeks.

Grayhill Inc., 561 Hillgrove Ave., La Grange, Ill. 60525. Phone (312) 354-1040 [348]

Thumbwheel switch is only 0.35 inch wide

First in a series of thumbwheel switches designed to save panel space, the model T35-02A is 0.35 inch wide, has a black gloss finish with white dial characters 0.16 in. high, and provides binary-coded-decimal output. The T35 series thumbwheels may be ordered individually or in assemblies of several switches ganged side-by-side. An assembly of 40 switches complete with end caps uses only 1 by 12 in. of front-panel space. List price of the

Circle 121 on reader service card

T35-02A is $3.25. In lots of 2,000, this drops to $2.15 each.

Cherry Electrical Products Corp., 3600 Sunset Ave., Waukegan, Ill. 60085. Phone V. Maida at (312) 689-7702 [349]

Seven-segment incandescent display is 0.25 inch high

Housed in a Pinlites mini-DIP package, a seven-segment incandescent readout is 0.25 inch high. Units in the MD-4 series can be installed directly into printed-circuit boards or plug-in sockets. Model MD-430 is a three-volt unit that draws only 8 milliamperes and delivers 1,400 foot-lamberts. Model MD-440, a 4-V unit, draws 12 mA and radiates 9,000 foot-lamberts at rated voltage. A 5-V model, the MD-450, is rated at 9,000 foot-lamberts, draws 12 mA, and is suited for direct drive from logic power sources. Special characters including plus/minus, colons and decimal points are available. The MD-4 units have an overall package size of 0.312 in. deep, 0.375 in. high and 0.275 in. wide.

Refac Electronics Corp., P.O. Box 809, Winsted, Conn. 06098. Phone Walter Gillis at (203) 379-2731 [350]

TOPICS

Components

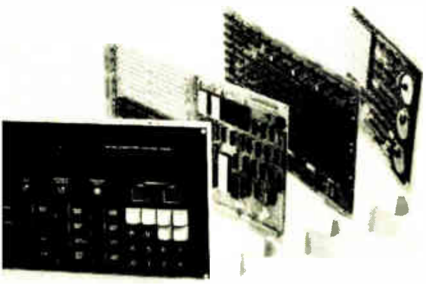
Vanguard Electronics, Inglewood, Calif., developers of the Magna Q chip inductor, have announced the Mini-Magna Q, a chip inductor that is only 75% the size of the earlier component. . . . **Spectrol Electronics Corp., City of Industry, Calif.,** has introduced a low-profile knob-adjustment option for all seven 0.375-inch-square single-turn trimmers in its model 63 cermet line. . . . **Vishay Resistive Systems Group, Malvern, Pa.,** is offering a new version of its 1202 precision trimmer with an extended range from 5 ohms to 20 kilohms. The 1202 trimmer uses Vishay's proprietary Bulk-Metal process for low noise, infinite resolution, and tight stability.

Microprocessors

Upgrading with same hardware

Microcomputer provides continuity from earliest steps of system development

Hardware continuity, from development through system production, is an important cost and time factor in the building of microcomputer-based systems. That's why a microcomputer from Monolithic Systems



Corp., the 8080+ development station, gives the system designer this continuity from the earliest phases to the final product.

Based on the Intel 8080A microprocessor, the development station allows system designers to gain an education in microprocessors, experiment in the laboratory, develop a prototype system, and go into production using the same hardware base at all stages. Priced at $1,976, the development station is a fully assembled microcomputer that requires only a +5-volt and +12-v supply to be fully operational.

It includes Monolithic's 8080+ microcomputer with control panel and wire-wrapping section, a dynamic random-access memory with 16,384 8-bit words, 512 words of alterable read-only memory, and the 8080+ operating system, which includes a resident assembler, an editor, and a teletypewriter software/hardware interface. The operating system is contained in 4,096 8-bit words of writable ROM.

Debugging capability is provided by the control panel, which has a hexadecimal-entry keyboard, 16 function-control keys, status indicators, and a 4-digit hexadecimal address/data display. With the addition of a Teletype terminal, programs can be loaded by paper tape, and the user can program in mnemonic codes. The standard development station provides 14,000 words of usable RAM, 2,000 of which are required by the operating system. Additional complementary MOS nonvolatile or dynamic RAMs can be added, up to 65,000 words.

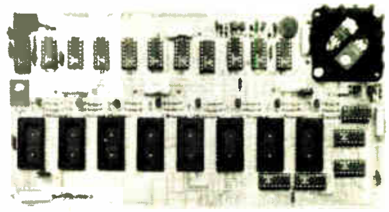
A novel capability of the development station is the C-MOS writable ROM, which allows the user to load development programs as though he were working with RAM, then strap out "write access," to get, in effect, a programed ROM. Battery backup provides data retention for up to three months without system power.

The heart of the system, the single-board microcomputer, includes a 5-by-7-inch wire-wrapping area for customizing designs in development or production. More than 150 software programs are available. Delivery time of the 8080+ development station or components is two weeks.

Monolithic Systems Corp., 14 Inverness Dr. East, Englewood, Colo. 80110. Phone Bill Phillips at (303) 770-7400 [411]

Programer plugs into microcomputer

Designed to program the widely used 2704 and 2708 read-only memories, a programer designated the Bytesaver is plug-compatible with the Altair 8080 and the Imsai 8800 microcomputers. Since the Bytesaver plugs directly into the microcomputer, the user can transfer program content from the microcomputer's random-access memory to the programable ROM. As an ad-



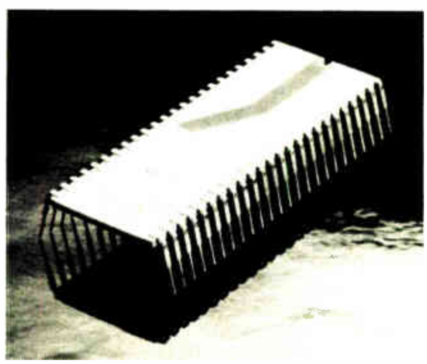
ditional convenience, the Bytesaver can store programs—it will hold up to eight PROMs, either 2704s or 2708s. Since the 2708 holds 1,000 bytes, the Bytesaver can give the microcomputer up to 8-k bytes of PROM storage. This answers the need in microcomputers for enough memory to hold a variety of programs in languages such as Basic.

Cromemco, One First St., Los Altos, Calif. 94022. Phone (415) 941-2967 [412]

Bipolar microprocessor offers 250-ns cycle time

An improved bipolar microprocessor from Scientific Micro Systems provides a minimum system cycle time of 250 nanoseconds—long enough to fetch, decode, and execute any instruction. As a result, the SMS 300 microprocessor can execute 4 million instructions per second. The original SMS unit had a 300-ns cycle time.

The faster cycle time permits direct control of double-density floppy disks, the company points out. Also, the processing power of the SMS 300 allows firmware control of such functions as calculation of the cyclic-redundancy-check character and disk formating, which usually require additional inte-



New products

grated circuits in the system.

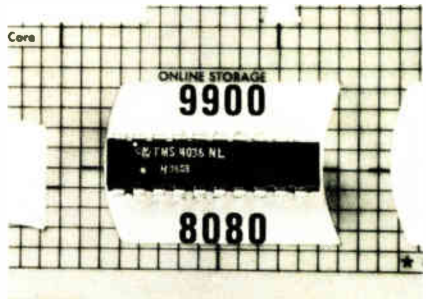
SMS is also introducing two input/output interface units, the SMS 362 and 363. Both offer external clocking and input latches that operate asynchronously with microprocessor timing. The SMS 362 and 363 enable the central processing unit to be directly connected with up to 4,096 I/O lines. The SMS 362 has tri-state outputs while the SMS 363 has open-collector outputs.

In quantities of 100, the price of the microprocessor is $90 each and that of the I/O interface units, $8 each. Delivery time is 30 days.

Scientific Micro Systems Inc., 520 Clyde Ave., Mountain View, Calif. 94043 [413]

Static RAM designed for microprocessors

An n-MOS static random-access memory developed by Texas Instruments consists of 64 8-bit words, a type of organization that makes it ideal for byte-oriented CPU systems like the TMS 8080 or TMS 9900, says Ed Huber, a marketing manager at TI. Designated the TMS 4036, the RAM was designed to provide a minimum cost-per-package count for terminal and controller systems requiring 128 words or fewer of random-access memory. Like the TMS 8080 and 9900, it has a common I/O bus that is fully TTL-compatible. The address, read/write control, output-enable, and chip-enable are also TTL-compatible. The TMS 4036 comes in a 20-pin, 300-mil-wide plastic or ceramic dual in-line package rated for operation from 0°C to 70°C. There are three speed ranges—1 microsecond, 650



nanoseconds, and 450-ns access and read-or-write cycle times. In 100-piece quantities, prices start at $5.67 each.

Texas Instruments Inc., Inquiry Answering Service, P.O. Box 5012, M/S 84, Dallas, Texas 75222 (Att. TMS 4036) [415]

Microcomputer includes programing keyboard

A keyboard entry system permits the user of Diversified Technology's Cosmos microcomputer to enter ASCII and assembly language without additional interface equipment. Other characteristics of Cosmos include low-power C-MOS technology, which makes it suited to battery operation and bus-oriented design. The unit is available complete or in a kit that includes the central processor, input/output circuitry, a 256-byte random-access memory, a clock, a keyboard interface, a display, and a motherboard. Many options are available.

Diversified Technology, P.O. Box 213, Ridgeland, Miss. 39157. Phone (601) 856-4121 [414]

Development center is also computer, smart terminal

A microcomputer development center, called the AMI 6800, combines into a single configuration a system for hardware and software design of microcomputer-based systems, a general-purpose data-processing system, and an intelligent communications terminal. The multifunctional and modular system includes a special-purpose cathode-ray-tube terminal with extensive microcircuitry and a dual-drive floppy-disk subsystem with more than 500,000 bytes of on-line data storage. A 16-position card cage and power supply are contained in the CRT chassis. Price of the 6800 is $10,500.

American Microsystems Inc., 3800 Homestead Rd., Santa Clara, Calif. 95051. Phone (408) 246-0330 [416]

Instruments

Counter spans 5 Hz–225 MHz

Use of standard case helps lower price of portable instrument

In the largest segment of the instrument market—portable units for field service and the laboratory bench—the trend this year has been toward lower costs. One way to cut the cost of portable instruments is to

standardize on packaging hardware for an entire line, including digital multimeters, counters, and so on. Even relatively small instrument suppliers can keep their prices low by adopting this approach, as exemplified by Ballantine Laboratories [*Electronics*, June 24, p. 42].

The second Ballantine instrument to use the firm's new standard package is the model 5725B frequency counter, a six-digit instrument with direct count to 225 megahertz. Priced at $295, the 5725B follows the model 3028A, a 3½-digit multimeter in the same ABS plastic case.

The frequency counter is designed for general-purpose application in industrial, communications, and laboratory-type measurements. It has a nonblinking display of 0.43-inch-high orange light-emitting diodes and a single switch for selection of readings in hertz, kilohertz, or megahertz over the range from 5 Hz to more than 225 MHz.

The single input to the 5725B covers the instrument's entire frequency range, with a nominal sensitivity of 50 millivolts. Sensitivity is adjustable with a screwdriver through a small hole in the front panel.

The instrument's input impedance is 1 megohm, shunted by 25 picofarads. Maximum input is 250 V rms from 10 Hz to 1 kHz, decreasing to 10 V rms for signals above 10 kHz.

The model 5725B provides frequency, totalize, and ratio capabilities, with resolution from 1 kHz to 0.1 Hz available by means of four selectable gate times. Readout to full resolution is made in 1 second, and selective-signaling audio tones may be measured to 0.1-Hz resolution in 10 seconds.

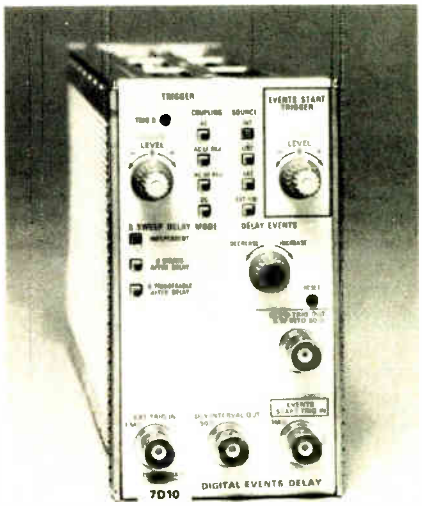
The instrument's internal time base can be derived from the built-in 1-MHz crystal clock or from an external frequency standard. The built-in oscillator has an aging rate of less than 2 parts per million per month and a temperature-induced drift of less than 5 parts in 10^7 from 0 to 40 °C.

The Ballantine model 3028A digital multimeter, priced at $279, offers six functions and 30 ranges. Rms response in ac voltage and current modes adds less than ±(1% of reading + 1 least-significant digit) error for waveforms of up to 10% distortion and 110 kHz in frequency. Frequency range is 15 Hz to about 200 kHz.

Ballantine Laboratories Inc., P.O. Box 97 Boonton, N.J. 07005. Phone (201) 335-0900 [351]

Digital events-delay unit plugs into Tektronix scopes

Operating in both the digital and analog domains, the 7D10 digital events-delay unit from Tektronix is a plug-in for the company's 7000 series oscilloscopes. In the digital domain, the 7D10 enables the user to identify transient locations or incorrect logic-state locations. Using the plug-in with a logic analyzer like the 7D01 [*Electronics*, April 29, p. 121], the operator can expand the



effective memory of the analyzer or delay the action of the memory by a specific number of digital words. In the delay-by-events mode, the 7D10 will count from 1 to 10^7 arbitrary trigger events, periodic or aperiodic, and deliver an output after the preselected count has been reached. In the analog domain, the 7D10 can be used to eliminate jitter or wow in mechanical systems. Price of the plug-in is $925, and delivery time is 10 weeks.

Tektronix Inc., P.O. Box 500, Beaverton Ore 97077. Phone (503) 644-0161 [353]

Interface coupler provides IEEE bus compatibility

Any electronic instrument can be made compatible with the IEEE 488 bus by use of the model 4880 interface coupler from Data Works Instrumentation. The IEEE 488 bus lets a user connect many instruments into a system by linking them with standard cables, eliminating custom interfaces. The 4880 coupler is available in three configurations: as a talker, where the coupler takes

the output of an instrument and puts its readings onto the 488 bus; as a listener, where the coupler takes commands from the bus and uses them to operate stimuli or output devices from the 488 bus; and as a device for connecting or controlling instruments, such as programable digital voltmeters, in a bidirectional manner (talker/listener). Delivery time is three to four weeks.

Data Works Instrumentation, 9748 Cozycroft Ave., Chatsworth, Calif. 91311. Phone Jerry Mercola at (213) 998-8985 [354]

Line of test instruments designed around LSI circuit

Application of large-scale-integrated-circuit technology has resulted in a two-year warranty being offered with a line of instruments marketed by the Data Tech division of Penril Corp. The family of instruments (see photo) includes counters, counter/timers, and an automatic a-m/fm modulation meter. The instruments are designed around an LSI device with the equivalent of 5,000 components on a chip.

Standard features include rfi-shielded enclosures, LED readout, 10-millivolt sensitivity, input circuitry with automatic gain control, and a crystal stability within 3 parts in 10^7 per month.

Penril Corp., Data Tech Division, 2700 S. Fairview St., Santa Ana, Calif. 92704. Phone Bill Miller at (714) 546-7160 [357]

Microprocessor controls wide-range LCR meter

Because the model 296 auto LCR meter is microprocessor-controlled, optional features cost less and become simple plug-in accessories, according to the meter manufacturer, Electro Scientific Industries Inc. The instrument, which measures inductance, resistance, capacitance, and conductance, also calculates dissipation and quality factors.

A programable-limits option allows up to 10 comparison values to be set for multiband sorting, and deviations can be displayed as a percentage or in units. The addition of the IEEE 488-1975 interface option makes the unit suitable for automatic component-testing.

Standard features of the model 296—which is priced under $5,000—include autoranging, dual frequency (1 kilohertz and 120 hertz), two test-voltage/current levels, and two 4½-digit readouts.

Electro Scientific Industries, 13900 N.W Science Park Dr., Portland, Ore. 97229 [355]

Programable synthesizer covers 1 kHz to 80 MHz

For applications that include automatic testing, a frequency synthesizer from the PRD Electronics division of Harris Corp. is programed by binary-coded-decimal input. This permits the functions of the digital frequency controls to be performed remotely. These functions are compatible with standard positive-true resistor-transistor-, diode-transistor-, and transistor-transistor-logic circuits.

The synthesizer, designated the PRD 7838, covers the range from 1 kilohertz to 80 megahertz in 1-hertz steps with an output level of 10 millivolts to 1 volt rms into 50 ohms.

The stability of the synthesizer when locked to the internal frequency standard is 1 part in 10^6 per month, with an optional standard of 5 parts in 10^9 per day. Typical spurious outputs are −70-dB nonharmonic and −40-dB harmonic. Price of the PRD 7838 is $3,498, and delivery time is two months after receipt of order.

Harris Corporation, PRD Electronics Division, 6801 Jericho Turnpike, Syosset, L.I., N.Y. 11791. Phone (516) 364-0400 [356]

Industrial

System runs 16 chromatographs

Microprocessor-based network collects outputs, processes and displays data

Using a hierarchical network of microprocessors, Spectra Physics has developed a low-cost data system, the SP4000, that provides complete control and status reporting for up to 16 gas or liquid chromatographs. The multichannel system collects the output of each chromatograph, computes the results, and produces both a plot and alphanumeric data on a thermal printer/plotter.

Richard Henry, product manager, claims that the SP4000's low-cost microprocessor technology, combined with Spectra-Physics' applications programs for data reduction and reporting, results in a data system that is approximately half the price of comparable products. A dual-channel system is priced at $12,000, a 4-channel one at $18,000, and a 16-channel system at $57,600.

Each chromatograph, which communicates with the system through a plug-in data interface, may be located up to 1,000 feet from the central processor. The data interface, which contains a Rockwell PPS-4, a 4-bit microprocessor, displays status information and controls automatic samplers. It also acquires the output signals from the chromatograph, converts them from analog to digital format, and transmits them via a bidirectional bus to the main central processing unit, an Intel 8080.

The 8080 performs most calculations, stores programs in read-only and random-access memories, and stores data in RAMs. Off-line data storage can be added by means of an optional floppy disk. Through a priority-interrupt scheme, the 8080 can control up to 16 data interfaces and 16 printer/plotters while concurrently performing integration, post-run calculations, and report preparation for up to 16 chromatographs. After the CPU has processed the data, the results are returned to the data interface for readout on the printer/plotter.

A cathode-ray-tube display and alphanumeric keyboard at the CPU are used for file manipulation and programing. To communicate with the system, users apply simple commands specifically designed for chromatograph users. No special programing knowledge is required. A plug-in keyboard can also be connected to the data interface for data retrieval and manipulation at the chromatograph.

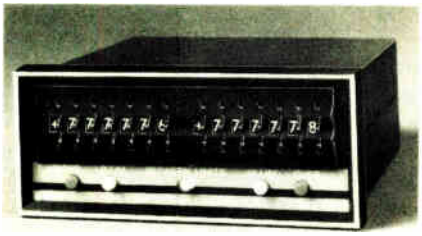
The SP4000 comes with base-line-correction algorithms, post-run calculations, and report formating programs to make up a complete data system. Any chromatograph network, new or old, can be automated with this system. Deliveries of the SP4000 will begin in August.

Spectra-Physics, 2905 Stender Way, Santa Clara, Calif. 95051. Phone Richard Henry at (408) 249-5200 [371]

Fast set-point comparators supervise process limits

It takes only 500 nanoseconds for the Datel 8400 series set-point comparators to perform a full comparison between 6-digit binary-coded-decimal inputs and the process limits displayed on the front panel. Applications for the 8400 series include sorting, batching, and automatic test equipment. In most cases, the job includes transmitting comparison outputs to system controllers.

The high-speed, panel-mountable digital comparators indicate limit status by means of front-panel lamps and logic outputs. A key fea-



ture is the set of comparison-logic outputs that are available at the rear connector—using gatable, latchable, open-collector transistor-transistor logic. This forms a data bus that enables the 8400 series comparators to interface with a central process computer. For additional versatility, the comparison-logic outputs can be multiplexed onto buses with 4, 8, 16, or 24 wires.

Optional relay boards controlled by the comparison-logic outputs enable the comparator to drive pumps, motors, and other power equipment. Dc-powered models of the comparator are priced at $335 for one to nine; ac-powered models, $399. Delivery time is four to six weeks.

Datel Systems Inc., 1020 Turnpike St., Canton, Mass. 02021. Phone Lawrence D. Copeland at (617) 828-8000 [373]

Retro-reflective modules provide photoelectric control

Designed for use in applications that have access to a regulated power supply of 24 volts dc, PEDM retro-reflective control systems are suited for interfacing with computers, programers, counters, and exter-

New products

nal-control relays. They offer a transistor output of 100 milliamperes at 24 V dc. Each unit consists of an infrared light-emitting diode as an invisible light source, a fast-response silicon phototransistor as sensor, a visible LED for alignment, and solid-state circuitry for transmitter, receiver, and output. The invisible light source is modulated for use in high ambient light. The visible LED monitors the industrial operation and glows briefly each time the control unit is activated.

Frost Controls Inc., One Angell Rd., Cumberland, R.I. 02864. Phone (401) 728-5950 [374]

Rate indicator displays speeds and ratios, too

Using complementary-MOS LSI circuitry, the series 7970 rate indicator from Veeder-Root measures and displays shaft speed, linear speed, production rate, or flow rate. Combined with any of a wide range of input sensors or signaling devices, the 7970 displays such information as revolutions per minute, feet per second, and gallons per minute. In addition to indicating absolute rates and speeds, the 7970 measures the numerical ratio between two independent sources—a factor that is valuable in synchronizing the drive systems of production and process machines. Operating on 115 volts ac, 50/60 hertz, an internally synchronized time base in the unit opens an input-signal gate for a precise time period. Impulses are

counted while the gate is open. Gate time, which is factory-set for 1 second, can be varied in the field from 0.16 to 60 seconds by internal switches. Other models are available for operation at 230 V ac and for applications requiring extra high speed or high resolution.

Veeder-Root Co., Hartford, Conn. 06102. Phone (203) 527-7201, Ext. 422 [375]

Surge suppressor reacts in 50 nanoseconds

Responding in 50 nanoseconds, a transient-surge suppressor called Volt-guard shunts to ground all spikes or damaging electricity. No field adjustments are required on the solid-state unit, which is simple to install. It protects equipment within 60 feet, electrically suppresses contact-arcing, and prevents damage to electronic circuitry. Applications include protection of computer systems and peripherals. Ac models are available in single phase up to 277 volts and in three-phase versions up to 550 V.

Sherron & Co., 201 Powell Mill Road, Suite C-103, Spartanburg, S.C. 29301. Phone (803) 576-0167 [376]

TV camera built to operate under adverse conditions

An environment-resistant, self-contained television camera, the model 2820B, offers automatic operation, remote control, 40,000:1 automatic light range, and solid-state construction. The 2820B has a sealed housing with integral heaters that permit operation in temperatures down to −40°C. The housing is tamper-proof, and no controls are exposed. Designed for monitoring and surveillance operations, the camera furnishes usable pictures with only 0.01 lumen per square foot of highlight illumination on the image-pickup-tube faceplate.

Cohu Inc., Electronics Division, Box 623, San Diego, Calif. 92112. Phone (714) 277-6700 [379]

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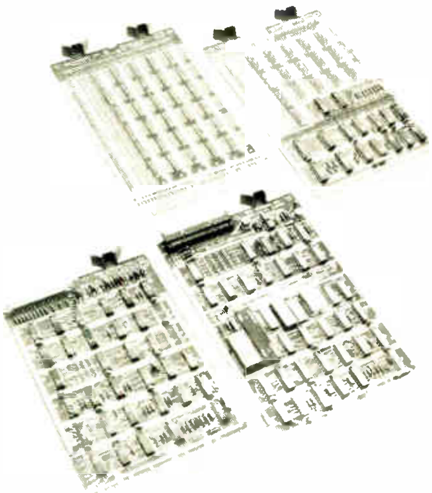

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Seven magazines in Japan communicate with management and professional engineers in the Japanese electronics industry. But only one influences so many influentials. That's us, Nikkei Electronics.

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Here's something to think about: If you were Japanese, you'd probably be reading us right now. That's simply because 57.4% of our readers, like yourself, are in a position to directly influence company purchasing decisions. Even more important, 31% of this group are *solely* responsible for the purchasing decisions. And 57.2% of our subscribers are either engineers or executives of Japan's largest 100 electronics or electronics-related manufacturers. Where the big purchasing decisions are made.

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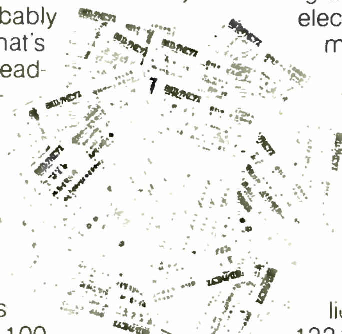

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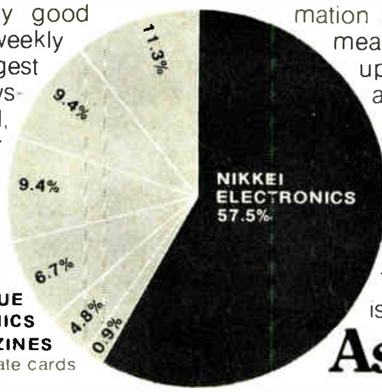

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Nikkei Electronics: Ask anybody who can read us.

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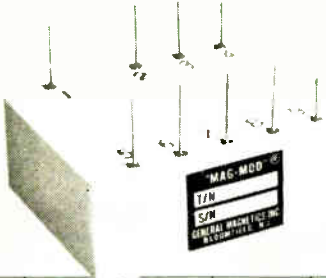
Solid State Sine-Cosine Synchro Converter

This new encapsulated circuit converts a 3-wire synchro input to a pair of d-c outputs proportional to the sine and cosine of the synchro angle.

- Complete solid state construction.
- Operates over a wide temperature range.



UNIT	DMD 1436-1	DMD 1430-1	DMD 1403-2	DMD 1361-6	DMD 1361-4	DMD 1193-4	DMD 1361-8	DMD 1446-1	DMD 1193-5	DMD 1193-6	DMD 1361-10	DMD 1472-2
L-L SYNCHRO INPUT (VRMS)	11.8	90	95	90	11.8	11.8	11.8	11.8	11.8	11.8	11.8	90
FREQUENCY (Hz)	400	400	60	400	400	400	400	400	400	400	400	60
FULL SCALE OUTPUT (VDC)	±10	±10	±3	±3	±3	±10	±10	±10	±10	±10	±10	±10
OUTPUT IMPEDANCE	<1Ω	<1Ω	<1Ω	<1Ω	<1Ω	<1Ω	<1Ω	<10Ω	<1Ω	<1Ω	<1Ω	<1Ω
L-L INPUT IMPEDANCE	>10K	>30K	>5K	>30K	>5K	/5K	>5K	>5K	>5K	>5K	>5K	>5K
REFERENCE VOLTAGE (VRMS)	26	115	115	115	26	115	26	115	115	115	26	115
ACCURACY SIN/COS (+25°C)	±6MIN	±6MIN	±6MIN	±6MIN	±6MIN	±6MIN	±6MIN	±0.5%	±6MIN	±6MIN	±6MIN	±6MIN
FULL TEMPERATURE RANGE ACCURACY SIN/COS	±15MIN	±15MIN	±15MIN	±15MIN	±15MIN	±15MIN	±15MIN	±0.5%	±15MIN	±15MIN	±15MIN	±15MIN
D.C. SUPPLY (VDC)	±15	±15	±15	±15	±15	±15	±15	±15	±15	±15	±15	±15
D.C. SUPPLY CURRENT	<30MA	<30MA	<30MA	<30MA	<30MA	<30MA	<30MA	<30MA	<30MA	<30MA	<30MA	<30MA
BANDWIDTH	>10Hz	>10Hz	external set	>20Hz	>5Hz	>10Hz	>10Hz	>10Hz	>2Hz	>40Hz	>5Hz	external set
SIZE	1.1x3.0 x1.1	2.0x2.25 x1.4	1.1x3.0 x1.1	1.5x1.5 x0.6	1.85x0.85 x0.5	2.01x2.25 x1.4	0.85x1.85 x0.5	2x2.25 x1.4	2x2.25 x1.4	2x2.25 x1.4	2.15x1.25 x0.5	1.1x3.0 x1.1
NOTES	–	dual channel unit	–	–	–	dual channel unit	–	dual sine output	dual channel unit	dual channel unit	–	–
TEMPERATURE RANGE	−40°C to +100°C	−40°C to +100°C	−40°C to +100°C	−40°C to +100°C	−40°C to +100°C	−40°C to +100°C	−40°C to +100°C	−40°C to +100°C	−40°C to +100°C	−40°C to +100°C	−40°C to +100°C	−40°C to +100°C

High Precision Analog Multipliers

PRODUCT ACCURACY (MCM 1519-1) ± ½% OF ALL THEORETICAL OUTPUT VALUES OVER FULL MILITARY TEMPERATURE RANGE OF −55 C TO +125 C. ZERO POINT ERROR FOR ANY INPUT COMBINATION IS ± 2MVRMS

Features:

- No external trims required
- Distortion free AC output over entire dynamic range
- Linearity, product accuracy and zero point virtually unaffected by temperature
- All units are hermetically sealed and are not affected by external fields
- High analog product accuracy and wave quality allows dual multiplier assemblies to be matched with 1% of point over the specified temperature range
- Full four quadrant operation
- Package size, power supply requirements and other specs. may be altered to your exact requirements at no extra cost.

Specifications:

- Transfer equation: Eo=XY/10
- X & Y input signal ranges: 0 to ±10V PK
- Maximum zero point error (X=0; Y=0 or X=±10; Y=0 or X=0; Y=±10): 2MVRMS
- Input impedance: Both inputs 20K min.
- Full scale output: ±10V peak
- Minimum load resistance for full scale output: 2KΩ
- Output impedance: 1Ω
- Short circuit duration: 5 sec.
- Frequency response characteristics (both inputs) 1% amplitude error: DC to 1200 Hz (min.) 0.5 DB Amplitude error: DC to 3500 Hz min. 3 DB point: Approx. 10K hz Roll off rate: 18 DB/octave
- Noise Level: 5MV PK-PK @ 100K Hz approx.
- Operating temp. range: See chart
- Storage temperature range: -55°C to +125°C
- DC Power: ±15V ±1% @ 30MA
- Dimensions: 2″ x 1.5″ x .6″

Type No.	Product Accuracy	Operating Temperature Range
MCM 1519-1	± 0.5%	−55 C - +125 C
MCM 1519-2	± 0.5%	−25 C - +85 C
MCM 1519-3	± 0.5%	0 C - +70 C
MCM 1520-1	± 1.0%	−55 C - +125 C
MCM 1520-2	± 1.0%	−25 C - +85 C
MCM 1520-3	± 1.0%	0 C - +70 C

Precision AC Line Regulator

Total Regulation 0.15% Max.

Features:

- Low distortion sinusoidal output
- Regulation control better than ten times superior to commercial AC voltage regulators transformer product lines
- No active filters or tuned resonant circuits employed resulting in immunity to line frequency changes
- 6.5 watt output level
- Small size
- Output set to ±1% accuracy — this includes initial set point plus line, load, frequency and temperature changes
- Foldback short circuit protection provided resulting in protection against overloads and short circuits of any duration
- Low profile package with straight pins makes the unit suitable for PC board mounti
- (unit is hermetically sealed)
- Transformer isolation betwee all power inputs and the outputs.

*Other units available at different power levels. Information will be supplied upon request.

Specifications Model MLR 1476-2:

- AC input line voltage: 115V RMS ±20% @ 400 Hz ±20%
- Output: 26V RMS ±1% (for any condition)
- Load: 0 to 250 MA, RMS
- Total regulation: ±0.15% maximum (any combination of line, load or frequency)
- Distortion: 2% maximum
- AC input line current: 100 MA. max. at full load
- DC power: ±15 V DC ±5% @ 15 MA. max.
- Phase angle: 1° max.
- Temp. Range: -40°C to +85°C
- Case Material: High permeability nickel alloy
- Terminals: Glass to metal hermetic seal pins

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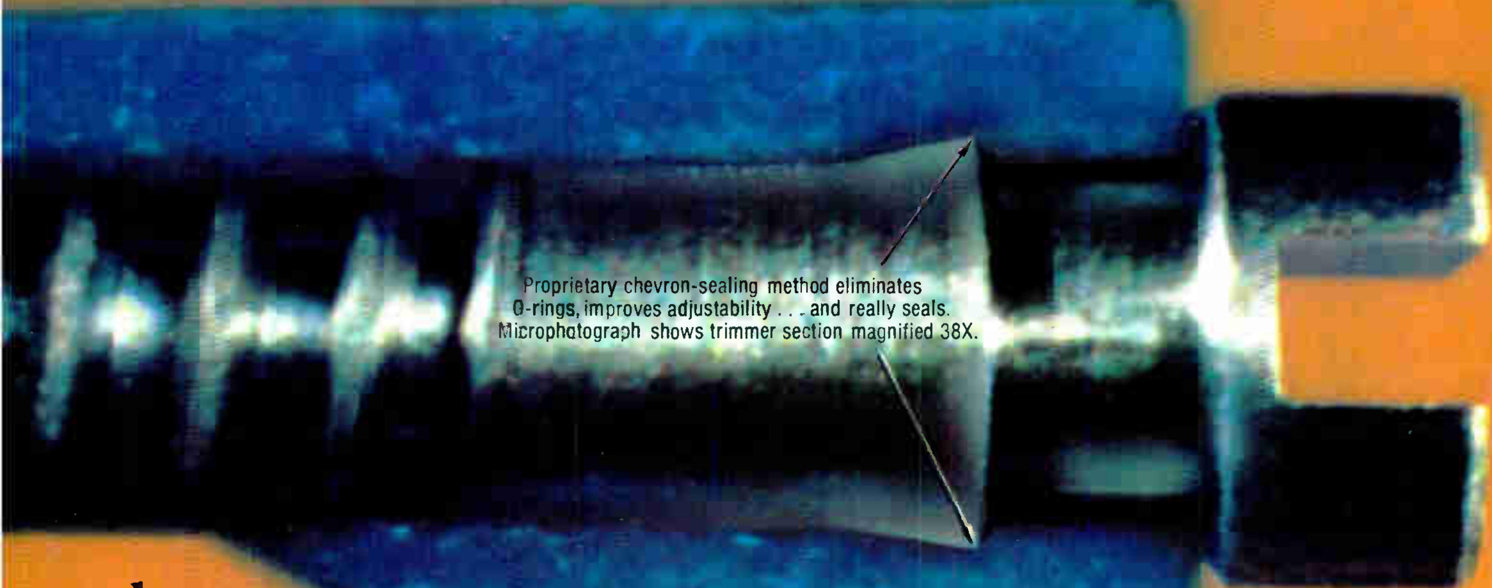
Circle 138 on reader service card

Better trimmer adjustability from a better way to seal . . .



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Bourns multi-turn trimmers adjust quickly, accurately, without the windup and springback problems associated with many trimmers sealed with O-rings . . . because there are no O-rings in the Bourns design.

We use a proprietary, press-fit chevron sealing technique that really works. No need for O-rings . . . therefore faster, more precise trimming without the bothersome rubber-band effect. Our secret is precision molding, closely held machining tolerances . . . and a few other tricks we've picked up since we invented the trimming potentiometer in 1952. Bourns trimmers stay sealed when others fail. We know. We've tested them all. Dip-test one yourself. We'll provide the sample.

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Send for a copy of our new engineering report on TRIMMER PERFORMANCE. Tell us about your application, and we will provide any qualification samples that best suit your needs. Bourns quality and reliability are available at ordinary prices . . . off-the-shelf from nearly 100 local distributor inventories, plus our largest-ever factory stock.

TRIMMER PRODUCTS, **TRIMPOT PRODUCTS DIVISION,** BOURNS, INC., 1200 Columbia Avenue, Riverside, California 92507. Telephone 714 781-5320 — TWX 910 332-1252.

Swage-Bond™, a revolution in trimmer reliability

Exclusive Swage-Bond process virtually eliminates pin termination failure and provides a marked improvement in tempco consistency. The P.C. pins are secured through the trimmer substrate, with a high-pressure compression swage on top and bottom sides. The pressure locks pins solidly into element. and thoroughly bonds them to the termination material. Compare with less reliable clip-on termination designs.

Wrap-around wiper for better setting stability

Multi-fingered, wrap-around wiper delivers more consistent, more reliable performance. Unique design significantly reduces CRV fluctuations and open circuit problems due to thermal and mechanical shock by maintaining a constant wiper pressure on the element. Compare the ruggedness of Bourns design with the common "heat-staked" wiper designs. Compare performance. Specify Bourns.

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Circle 901

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The micro package is .060" in diameter and permits the assembly of arrays utilizing .100" centers. The intermediate package has a flange diameter of .098" which permits its use for small space applications and ease of product handling.

All units are hermetically sealed with either glass windows or glass lenses. The lenses provide a narrow angular response of $\pm 17°$ while the windows provide an angular response of $\pm 35°$.

All Clairex phototransistors and photodarlingtons are 100% tested for light current (I_L) at a stated irradiance . . . either per the standard Clairex specification, or per your special requirements. In addition, most Clairex units are tested to a minimum and maximum light current (I_L) limit . . . normally a 3:1 spread.

Because Clairex has specialized in opto-electronics since 1953, we probably stock the phototransistor or the photodarlington with the characteristics that you need.

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